Title : Final Project for ECE 253
Name : Accelerometer based Ball Game on Nexys4 with LCD & VGA as display
Purpose : Understand the design & application of an accelerometer with VGA & LCD interface.
Team : Rahul Vishwakarma
Pooja Venkatesh Kadam
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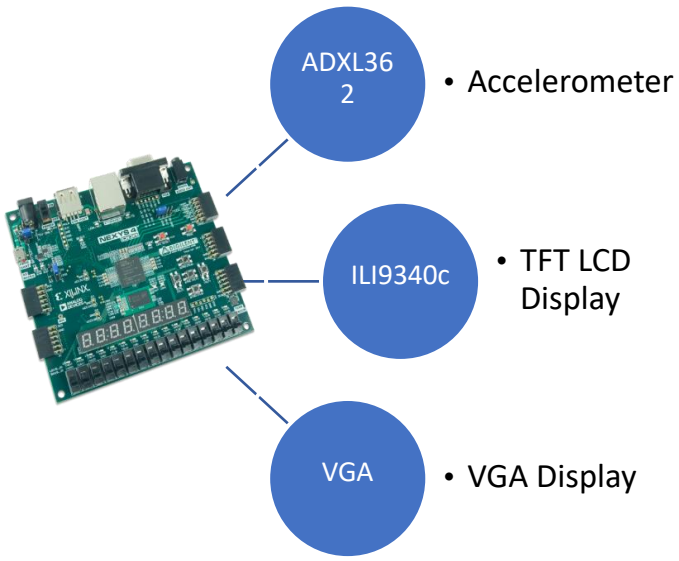
Goal

Use a Nexys 4 DDR development board to Implement an accelerometer controlled ball game, and visualize the game on an LCD or VGA display.

Components

The Nexys4 DDR board is a complete, ready-to-use digital circuit development platform based on the latest Artix-7™ Field Programmable Gate Array (FPGA) from Xilinx®. The Nexys4 DDR is compatible with Xilinx's new high-performance Vivado®Design Suite. This enabled us to create MicroBlaze™ embedded soft processor-based designs in an RTL project.



There are three major components that needs to be interfaced to the Xilinx Nexys 4 DDR FPGA board.

Accelerometer: The ADXL362 is available as part of the stock Nexys 4 DDR board.

TFT LCD Display: The display part ILI9340c with 240x340 pixel display is integrated with the Nexys board over SPI and GPIO interface.

VGA Display: A computer monitor with standard VGA is connected to the on-board VGA connector.

(1a.) Components used in project

RTL project will consist of the soft-core Microblaze processor running on the Nexys4 DDR development board with Artix 7 FPGA chip from Xilinx. Some interfaces like VGA, needed a custom IP package.

Source Code: The Games C SDK source code is available in the bubble.zip archive. Also attached is the VGA AXI interface HDL code.

Game

The ball game allows the user to leverage the tilting motion of the Nexys 4 board to navigate a ball displayed on the LCD screen in real-time. A motion sensed game play is achieved in the project.

- A red ball is placed on the screen
- The game initializes a stage with various rectangular hazards
- Boards tilting motion shall guide the ball in that direction
- The movement of the ball can be observed on the screen
- User should use the tilting motion to guide the ball, while avoiding the hazards
- If the ball hits a rectangular hazard, then the game is over
- When the ball reaches the finish marker the game is won

The entire board is used as a joystick that can be tilted right, top to move the ball in those directions.

(2b.) Image of the LCD screen with a ball

The accelerometer detects the rotation and provides the magnitude as well as direction of the movement. This is translated to a shift in the ball on the screen. Larger the tilt larger is the shift of the ball in that direction. The shift on the ball is computed based on the magnitude of the acceleration in four directions. The direction of the ball movement is being decided by the sign of the input x and y coordinates of the accelerometer. Using VGA controller, we are displaying the game maze on the LCD screen.

The figure below displays the game maze on the LCD screen.

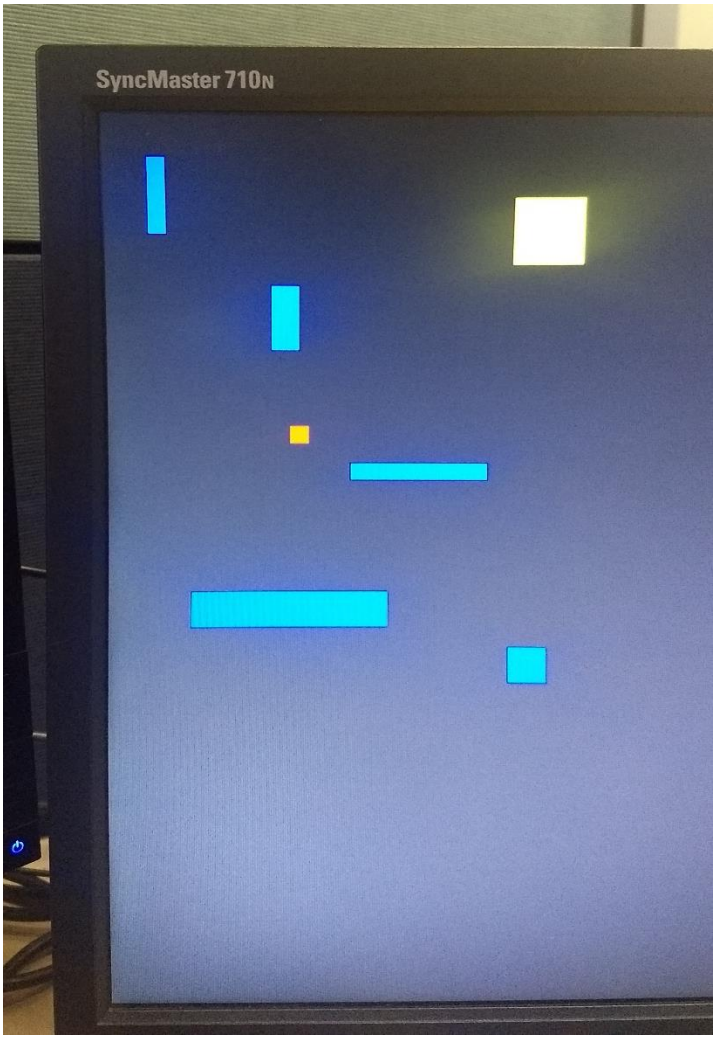


Fig 2C. Game Background Displayed on VGA Monitor

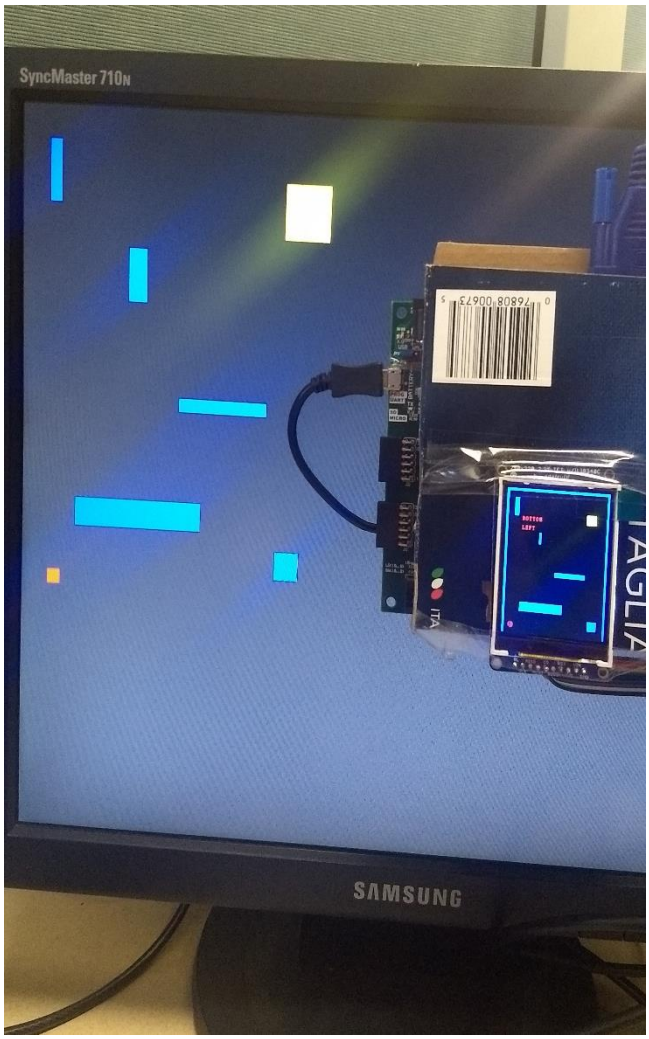


Fig 2D. Game synced on LCD & VGA

The ball game logic writes simultaneously to LCD as well as VGA monitor. The movement of the ball can be seen in both the places at the same time. The game logic maintains the state of the ball and the winning position in the memory mapped registers which are read by VGA controller as well as the LCD interface. The ball movement and winning position is driven via C code in the SDK based on the direction feeds from the accelerometer. A fixed background map is created separately for the VGA in Verilog and for LCD in the SDK.

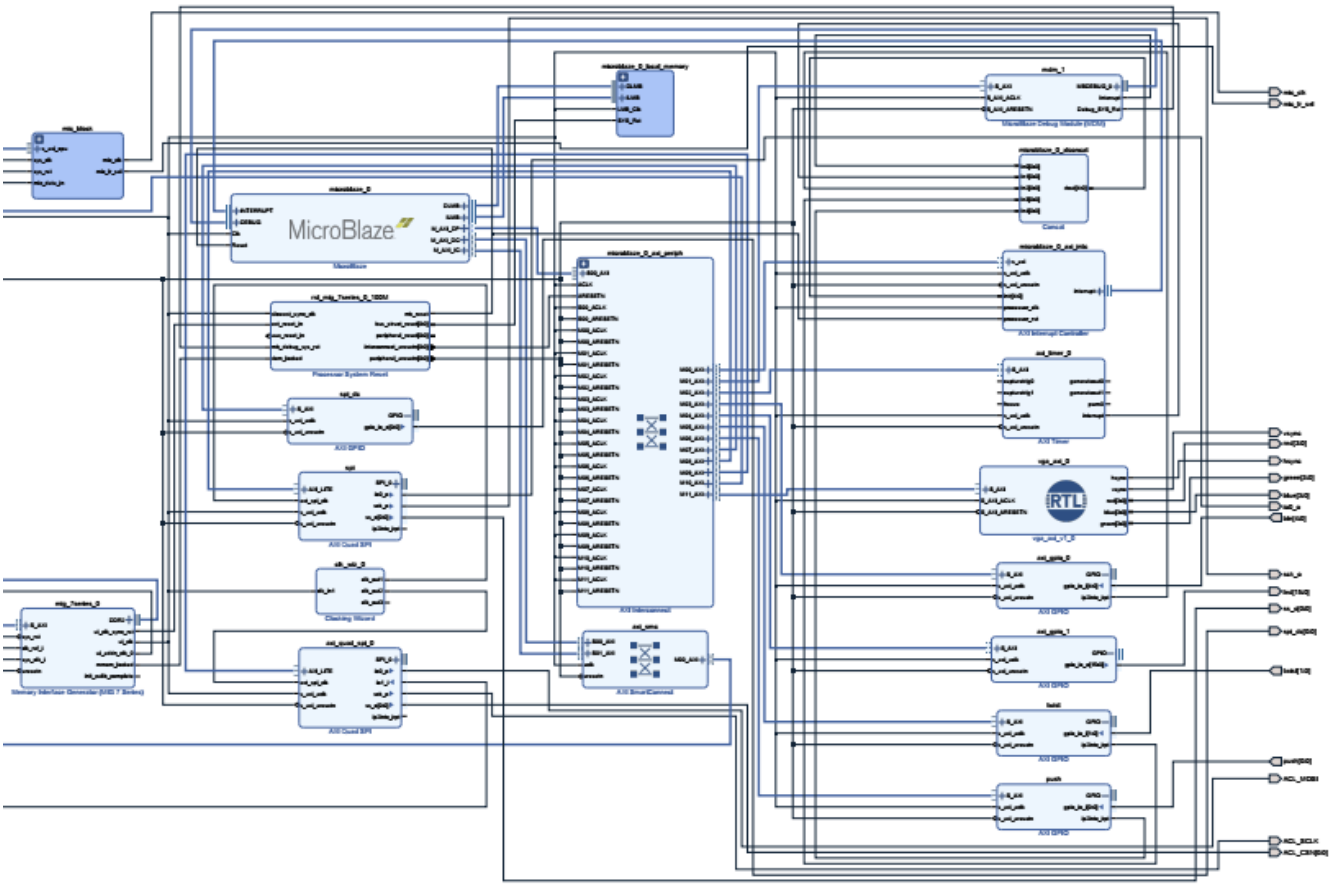
Methodology

Overview

We will create an RTL project using the **Vivado 2017.2** design suite from Xilinx. The Microblaze IP core is configurable, and permits creation of a system with different memory sizes, clock speed and # of pipeline stages. We use the Vivado design Suite to create hardware designs and to export the hardware to the **Xilinx SDK**, where we can then develop **C** programs to run on our custom designed processor.
The Vivado Design Suite provides tools to help a system designer understand the resources used in their design. We will be adding various peripherals like ADXL362, LCD and VGA IP block to the microblaze based design.

Design

A view of the design complete with various AXI, SPI and AXI Quad SPI interfaces to the VGA, LCD and ADXL362 modules respectively. The below design also consists of push buttons, LED and rotary encoder over GPIO interface.

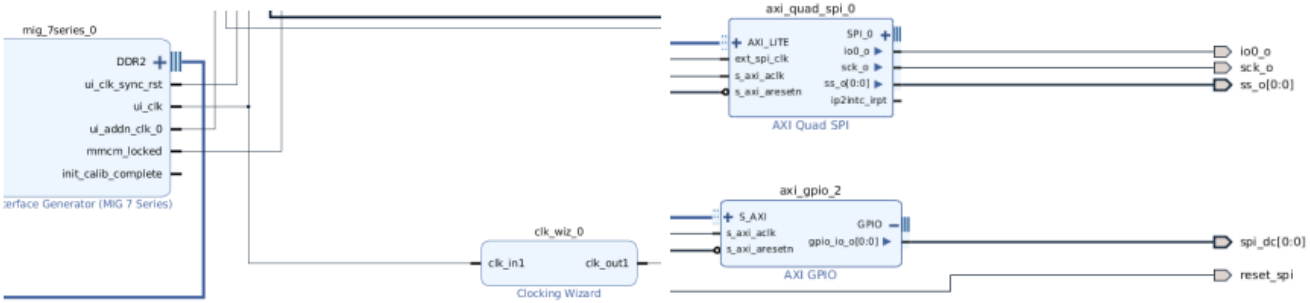


(3a.) Complete Block Design with Accelerometer, LCD and VGA IP Package

The ADXL362 is an ultralow power, 3-axis MEMS accelerometer that consumes less than 2 µA at a 100 Hz output data rate and 270 nA when in motion triggered wake-up mode. The ADXL362 includes bus keepers on all pins that can be configured as digital inputs: MOSI, SCLK, CS, INT1, and INT2. Acceleration and temperature measurements are converted to 12-bit values and transmitted via SPI using two registers per measurement

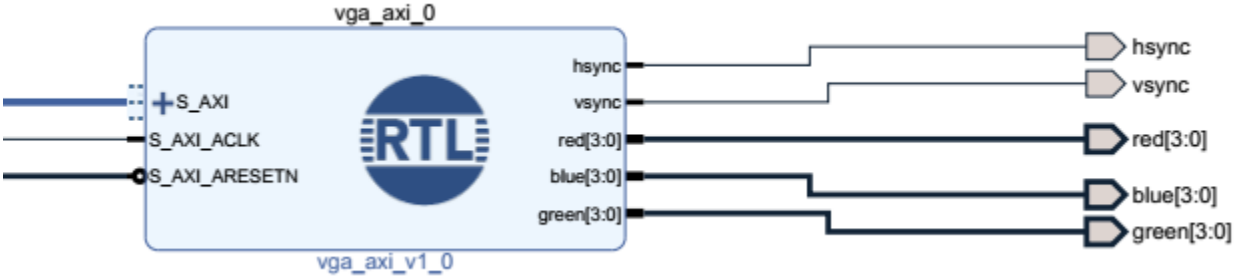
(3b.) Design of the ADXL362 AXI SPI package

The LCD peripheral uses a SPI digital interface. A SPI interface to handle the communication with the peripheral's microcontroller (ILI9340/ILI9341) could be implemented using software bit-level protocol coding or by making use of a hardware FSM peripheral controller. The benefit of software is program level flexibility, while a hardware interface allows for a much higher speed interface (5Mb/s = 10MHz clock in this case). An additional GPIO sets the 'Data/Command' value for the Display



(3c.) Design of the LCD SPI & GPIO module

We are using a custom AXI memory-mapped VGA module. The 'vga_axi_v1_0' is a AXI-wrapped IP developed with the Xilinx Vivado IP Packager tool. The purpose of this, is to provide a memory-mapped interface to the Nexys 4 DDR's 4-bit VGA interface. The advantage of having a memory-mapped interface, of course, is to completely abstract the hardware from a software application.



(3d.) Design of the custom VGA AXI IP package

The VGA AXI IP Package is customized using the create and package new IP feature of Vivado. An AXI interface was created using the tool which contained the following Verilog module.

```
vga_b vga(
    .clk(S_AXI_ACLK),          // 100 MHz clock
    .clr(S_AXI_ARESETN),       // CPU reset pin
    .hsync(hsync),             // Horizontal sync counter
    .vsync(vsync),             // Vertical sync counter
    .red(red),
    .green(green),
    .blue(blue),
    .ball_x(slv_reg0),         //Slave reg0 mapped to BASEADDR 0x44A30000 + 0
    .ball_y(slv_reg1),         //Slave reg1 mapped to BASEADDR 0x44A30000 + 4
    .ball_s(slv_reg2),
    .winbox_x(slv_reg3),
    .winbox_y(slv_reg4),
    .winbox_s(slv_reg5)
);
```

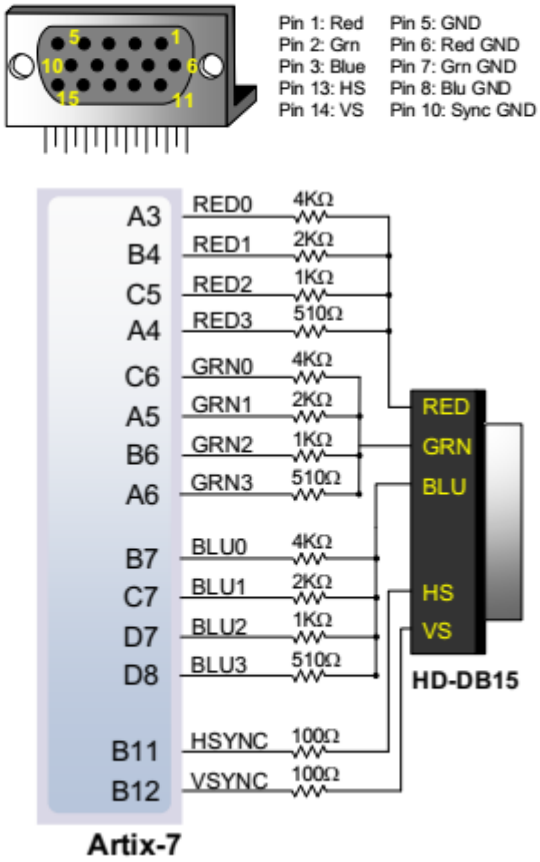
The Clock is divided by 4 within the vga_b module to obtain the required 25MHz pixel clock needed to drive the VGA signals over the 640x480 display.

Symbol	Parameter	Vertical Sync			Horiz. Sync	
		Time	Clocks	Lines	Time	Clks
T_S	Sync pulse	16.7ms	416,800	521	32 us	800
T_{disp}	Display time	15.36ms	384,000	480	25.6 us	640
T_{pw}	Pulse width	64 us	1,600	2	3.84 us	96
T_{fp}	Front porch	320 us	8,000	10	640 ns	16
T_{bp}	Back porch	928 us	23,200	29	1.92 us	48

(4a.) Signal Timing for 640x480 VGA

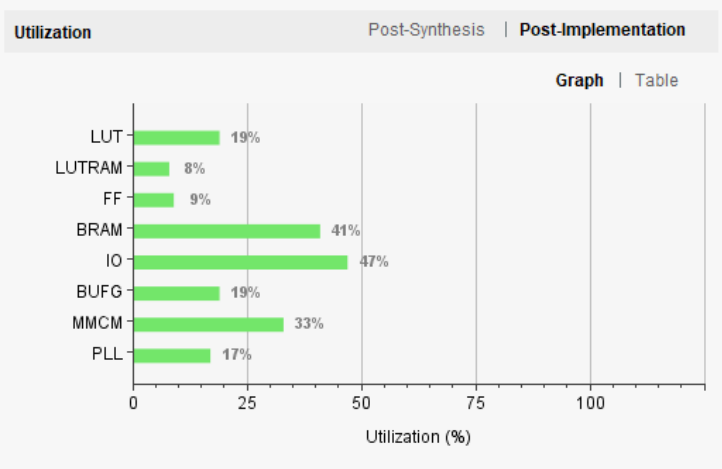
The Nexys4 DDR board uses 14 FPGA signals to create a VGA port with 4 bits-per-color and the two standard sync signals (HS – Horizontal Sync, and VS – Vertical Sync). An AXI interface is created in the FPGA to drive the sync and color signals with the correct timing in order to produce a working display system.

Registers 0 to 31 are mapped to this AXI interface and is capable of reading/writing to this memory. The slave registers 0 and 1 are used to draw the location of the ball in the game.



(4a.) Nexys 4 DDR VGA Interface

Summary



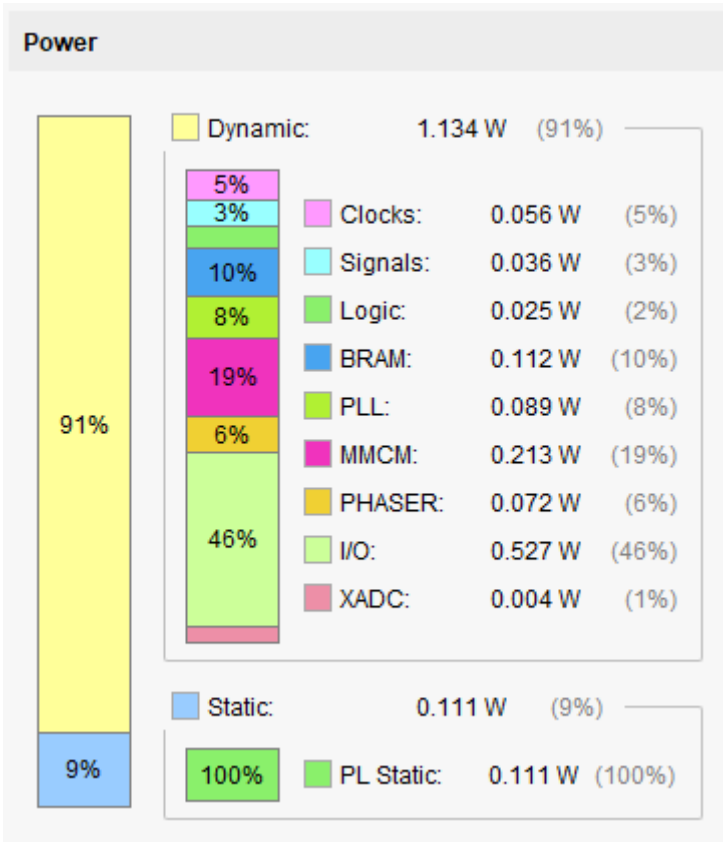
Timing

Worst Negative Slack (WNS):	0.675 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	39702

Implemented Timing Report

(3a.) Left: Report Utilization Table
(3b.) Right: Timing Report

The design's utilization is relatively less even when we have multiple components on the block.



Power

Total On-Chip Power:	**1.245 W**
Junction Temperature:	**30.7 °C**
Thermal Margin:	54.3 °C (11.8 W)
Effective ϑJA:	4.6 °C/W
Power supplied to off-chip devices:	0.633 W
Confidence level:	Low

(3c.) Power Summary

This provides the consumption of power by various components in the FPGA.

Result

We could demonstrate the accelerometer based game on an LCD and VGA display. The ball positions changed in the four directions and by avoiding the blue hazard blocks we were able to reach the yellow winning position in the game.