EC344 Term Project

Design and simulate a Current Mirror based differential amplifier in 180 nm CMOS process technology for the specifications given in the table below.

- Power supply = 1.8 V.
- Input Common-mode Voltage = 900 mV
- $V_{DS,sat}$ for the input transistors can be in the range 200-300 mV. Other transistors it can be 100-200v mV.
- Tail current should be derived from a 20 µA current source using current mirror.
- DC Gain ≥ 35 dB
- Phase Margin ≥ 60º
- Slew rate ≥ 40 V/µs when driving a load capacitance is 1 pF.

1. Plot the frequency response of the amplifier showing DC gain, UGB and Phase Margin.
2. Show that the design meets the specifications.
3. Find the CMRR (use AC analysis to find the differential gain and common-mode gain)
4. Use the OTA as a voltage follower circuit. Test the circuit for a differential input of 100 mV peak-to-peak, 1kHz sine wave. What is the gain of the voltage follower? Is there any deviation from the expected value? Why?
5. Design an inverting Schmitt Trigger circuit using the OTA (you designed) for UTP=1 V and LTP=0.8 V. The feedback resistors should be chosen such that the worst case current drawn from the OTA by the feedback network is about 10% of the tail current.
   Test it for an input 0.9 V + 0.9 sin(2000πt).

Note: Do not use the transistor current or gm equations while designing. These equations are highly approximated equations (as already been told in the class)