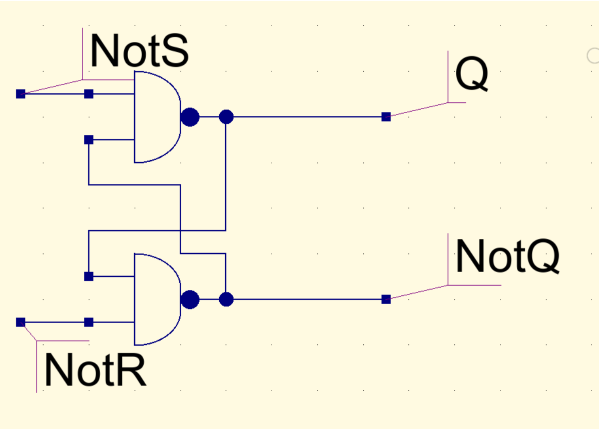
Physics 314, fall 216
Lab 3: Flip-flops

Part 1: Simple flip-flops from NAND gates

1. Basic NAND SR latch



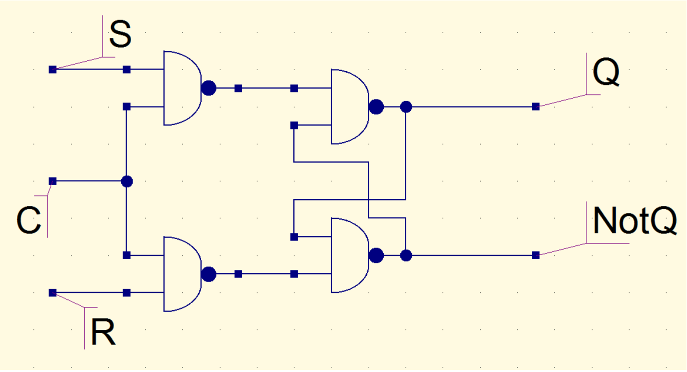
Build the circuit at right. Use the switches to provide the inputs (S and R). Drive one of the lamps with the Q output, and another lamp with the $\bar{Q}$ output. Experimentally determine the function table. A partial version is shown below the figure. Note that for some values the output may depend on the history as well as on the current values of the inputs. Be sure to look for and record the dependence on history. This means not only trying to fill in the ?'s, but looking for outputs that do or don't depend on the order in which the inputs were set or when they switch.

NotS	NotR	Q	NotQ
0	0	?	?
0	1	1	0
1	0	0	1
1	1	?	?

Starting with both inputs high, try bringing one input low to set Q, and then repeatedly switch that input between high and low. Does the output change? How is this behavior useful in debouncing switches?

2. Clocked (gated) SR latch from NAND gates

Build the circuit at right. Again, use the switches as the inputs, and drive one lamp with the Q output and another lamp with the $\bar{Q}$ output. Use one of the debounced pushbutton switches as the clock. (Take the output from the side of the switch such that the output value is high when the button is depressed and low when the button is out.)



Experimentally determine the function table (include clock value as part of the table). Again, look for and record any history effects.

Can you tell how the flip-flop is triggered? That is, when can the output change? (Anytime, only when the clock is high, only when the clock is low, when the clock is switching from low to high, or when the clock is switching from high to low?)

Part 2: Using flip-flops

3. <u>7474: D-type positive-edge-triggered flip-flop with preset and clear</u>

Wire the flip-flop up in a way that will let you test the function table in the attached datasheet. You may want to use the "debounced" pushbutton switch for the clock input. Use the outputs Q and $\overline{Q}$ to drive lamps.

Experimentally verify the function table on the data sheet.

Under what clock conditions can the output change in response to the signal at the D input? Why is this called a "positive-edge-triggered" flip-flop?

Try connecting the clock to the logic (bouncy) switch instead of the debounced pushbutton. How does that change the triggering? What's going on here?

4. <u>Divide-by-two, divide-by-four counters with D-type FFs</u>

Connect $\overline{Q}$ to D (as well as to the lamp) and set $\overline{PRE}$ and $\overline{CLR}$ high. Predict what will happen to the outputs when the flip-flop is clocked. Try it out—what happens? Explain why the circuit behaves as it does.

Now connect the CLK input to the function generator on the breadboard. Set the function generator to a low-frequency (on the order of a few Hz) TTL signal. Watch the blinking lights!

Increase the frequency into the kHz range. Look at the signals at CLK and at Q using separate channels of the oscilloscope. Sketch the two waveforms carefully, with scales indicated on your sketch. What's the relationship between the clock frequency and the output frequency? Explain how this "divide-by-two" counter works.

Use the HP function generator to look at the signals at high frequency. Try to measure the propagation time of the flip-flop and compare it with datasheet values.

Figure out how to make a divide-by-four counter using two D-type flip-flops and feeding $\overline{Q}$ from the first flip-flop to CLK of the second one. Try it out. When you're successful, sketch the circuit diagram and the output and CLK signals.

Reduce the frequency of the clock and monitor the outputs with lamps—can you see the counter counting up in binary?

This kind of counter (in which the output of one flip-flop is used to clock the next flip-flop) is called a *ripple counter*.