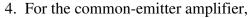
Topics: transistors, op-amps

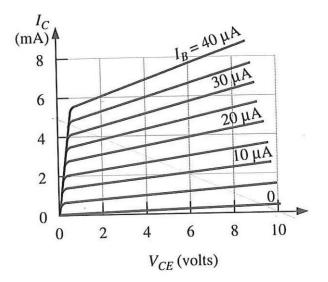
Reading: my notes, supplementary info on transistors (see website)

## Reading questions:

- 1. For the transistor whose characteristic curves are shown at right,
- a) Roughly what is the value of  $\beta$  (or h<sub>FE</sub>) at V<sub>CE</sub> of 4 volts, say.
- b) If the power rating of the transistor  $P_{max}$  is 0.05 W, is there any region of the curves shown for which  $P_{max}$  would be exceeded? (Power dissipated by a BJT  $\sim$   $V_{CE}I_{C.}$ ) Explain. Also, shade in roughly the region where  $P_{max}$  is exceeded.



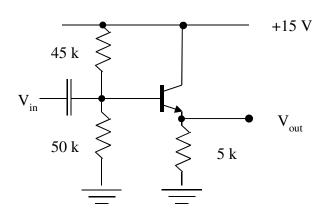
- i) Is there voltage gain (that is, is  $v_{out}/v_{in}$  much different from 1)? If so, what does the gain depend on?
- ii) If the voltage at the base rises by 0.1 V, what does the voltage at the emitter rise by?
- iii) Is the output signal inverted with respect to the input signal?



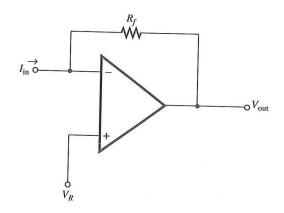
- 5. For the emitter follower (a.k.a. common collector),
- i) is there voltage gain (that is, is v<sub>out</sub>/v<sub>in</sub> different from 1)? If so, what does the gain depend on?
- ii) If the voltage at the base rises by 0.1 V, what does the voltage at the emitter rise by?
- iii) Is the output signal inverted with respect to the input signal?

Problems: (assume that all transistors are npn silicon, like the 2N3904)

- 1) This is an emitter follower with the base biased quiescently above ground so that a single supply can be used without clipping negative input signals.
- a) Find the expected quiescent values of V<sub>B</sub>, V<sub>E</sub>, and V<sub>C</sub>.
- b) Find the expected quiescent values of  $I_B$ ,  $I_E$ , and  $I_C$  (hint: start with  $I_E$  and assume  $\beta$ =100).
- c) Check to make sure that the quiescent  $I_B$  is small compared to the quiescent current through the 50k resistor. Why is it important to design the circuit so that this is the case?
- d) For roughly what range of  $V_{in}$  (+ and ) is the output free from clipping?
- e) Would you need the 45k and 50k resistors if you had a 15V power supply as well as a +15V supply available? Why?



- 3. a) What does the circuit at right do (Assume  $V_R=0$ )? Explain using the golden rules of op-amps.
- b) What is the maximum current that can be measured (without saturating the op amp) in the figure at right if  $R_f$  is 10 M? Assume  $\pm 15$  V supplies are being used to power the op amp.

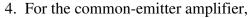


Topics: transistors, op-amps

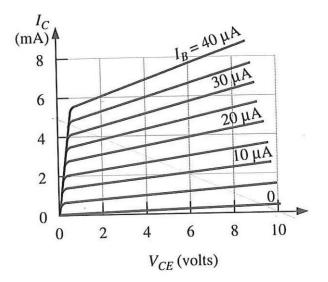
Reading: my notes, supplementary info on transistors (see website)

## Reading questions:

- 1. For the transistor whose characteristic curves are shown at right,
- a) Roughly what is the value of  $\beta$  (or h<sub>FE</sub>) at V<sub>CE</sub> of 4 volts, say.
- b) If the power rating of the transistor  $P_{max}$  is 0.05 W, is there any region of the curves shown for which  $P_{max}$  would be exceeded? (Power dissipated by a BJT  $\sim$   $V_{CE}I_{C.}$ ) Explain. Also, shade in roughly the region where  $P_{max}$  is exceeded.



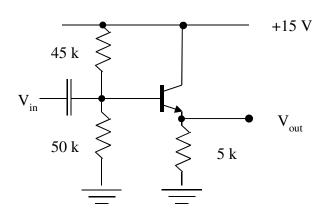
- i) Is there voltage gain (that is, is  $v_{out}/v_{in}$  much different from 1)? If so, what does the gain depend on?
- ii) If the voltage at the base rises by 0.1 V, what does the voltage at the emitter rise by?
- iii) Is the output signal inverted with respect to the input signal?



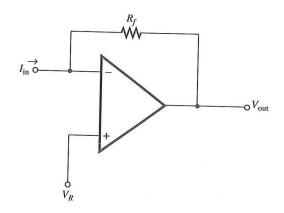
- 5. For the emitter follower (a.k.a. common collector),
- i) is there voltage gain (that is, is v<sub>out</sub>/v<sub>in</sub> different from 1)? If so, what does the gain depend on?
- ii) If the voltage at the base rises by 0.1 V, what does the voltage at the emitter rise by?
- iii) Is the output signal inverted with respect to the input signal?

Problems: (assume that all transistors are npn silicon, like the 2N3904)

- 1) This is an emitter follower with the base biased quiescently above ground so that a single supply can be used without clipping negative input signals.
- a) Find the expected quiescent values of V<sub>B</sub>, V<sub>E</sub>, and V<sub>C</sub>.
- b) Find the expected quiescent values of  $I_B$ ,  $I_E$ , and  $I_C$  (hint: start with  $I_E$  and assume  $\beta$ =100).
- c) Check to make sure that the quiescent  $I_B$  is small compared to the quiescent current through the 50k resistor. Why is it important to design the circuit so that this is the case?
- d) For roughly what range of  $V_{in}$  (+ and ) is the output free from clipping?
- e) Would you need the 45k and 50k resistors if you had a 15V power supply as well as a +15V supply available? Why?



- 3. a) What does the circuit at right do (Assume  $V_R=0$ )? Explain using the golden rules of op-amps.
- b) What is the maximum current that can be measured (without saturating the op amp) in the figure at right if  $R_f$  is 10 M? Assume  $\pm 15$  V supplies are being used to power the op amp.

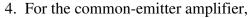


Topics: transistors, op-amps

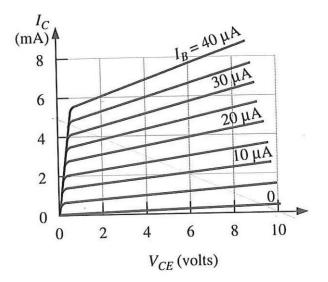
Reading: my notes, supplementary info on transistors (see website)

## Reading questions:

- 1. For the transistor whose characteristic curves are shown at right,
- a) Roughly what is the value of  $\beta$  (or h<sub>FE</sub>) at V<sub>CE</sub> of 4 volts, say.
- b) If the power rating of the transistor  $P_{max}$  is 0.05 W, is there any region of the curves shown for which  $P_{max}$  would be exceeded? (Power dissipated by a BJT  $\sim$   $V_{CE}I_{C.}$ ) Explain. Also, shade in roughly the region where  $P_{max}$  is exceeded.



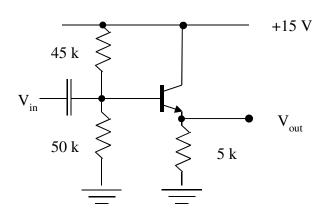
- i) Is there voltage gain (that is, is  $v_{out}/v_{in}$  much different from 1)? If so, what does the gain depend on?
- ii) If the voltage at the base rises by 0.1 V, what does the voltage at the emitter rise by?
- iii) Is the output signal inverted with respect to the input signal?



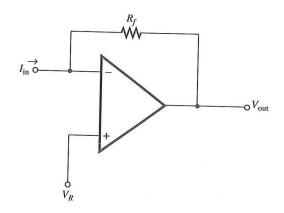
- 5. For the emitter follower (a.k.a. common collector),
- i) is there voltage gain (that is, is v<sub>out</sub>/v<sub>in</sub> different from 1)? If so, what does the gain depend on?
- ii) If the voltage at the base rises by 0.1 V, what does the voltage at the emitter rise by?
- iii) Is the output signal inverted with respect to the input signal?

Problems: (assume that all transistors are npn silicon, like the 2N3904)

- 1) This is an emitter follower with the base biased quiescently above ground so that a single supply can be used without clipping negative input signals.
- a) Find the expected quiescent values of V<sub>B</sub>, V<sub>E</sub>, and V<sub>C</sub>.
- b) Find the expected quiescent values of  $I_B$ ,  $I_E$ , and  $I_C$  (hint: start with  $I_E$  and assume  $\beta$ =100).
- c) Check to make sure that the quiescent  $I_B$  is small compared to the quiescent current through the 50k resistor. Why is it important to design the circuit so that this is the case?
- d) For roughly what range of  $V_{in}$  (+ and ) is the output free from clipping?
- e) Would you need the 45k and 50k resistors if you had a 15V power supply as well as a +15V supply available? Why?



- 3. a) What does the circuit at right do (Assume  $V_R=0$ )? Explain using the golden rules of op-amps.
- b) What is the maximum current that can be measured (without saturating the op amp) in the figure at right if  $R_f$  is 10 M? Assume  $\pm 15$  V supplies are being used to power the op amp.

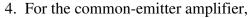


Topics: transistors, op-amps

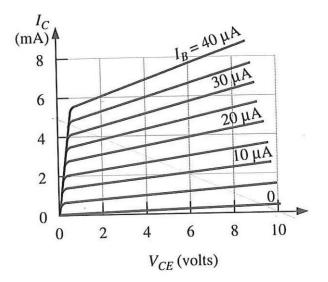
Reading: my notes, supplementary info on transistors (see website)

## Reading questions:

- 1. For the transistor whose characteristic curves are shown at right,
- a) Roughly what is the value of  $\beta$  (or h<sub>FE</sub>) at V<sub>CE</sub> of 4 volts, say.
- b) If the power rating of the transistor  $P_{max}$  is 0.05 W, is there any region of the curves shown for which  $P_{max}$  would be exceeded? (Power dissipated by a BJT  $\sim$   $V_{CE}I_{C.}$ ) Explain. Also, shade in roughly the region where  $P_{max}$  is exceeded.



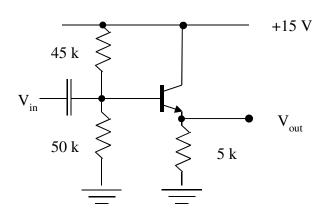
- i) Is there voltage gain (that is, is  $v_{out}/v_{in}$  much different from 1)? If so, what does the gain depend on?
- ii) If the voltage at the base rises by 0.1 V, what does the voltage at the emitter rise by?
- iii) Is the output signal inverted with respect to the input signal?



- 5. For the emitter follower (a.k.a. common collector),
- i) is there voltage gain (that is, is v<sub>out</sub>/v<sub>in</sub> different from 1)? If so, what does the gain depend on?
- ii) If the voltage at the base rises by 0.1 V, what does the voltage at the emitter rise by?
- iii) Is the output signal inverted with respect to the input signal?

Problems: (assume that all transistors are npn silicon, like the 2N3904)

- 1) This is an emitter follower with the base biased quiescently above ground so that a single supply can be used without clipping negative input signals.
- a) Find the expected quiescent values of V<sub>B</sub>, V<sub>E</sub>, and V<sub>C</sub>.
- b) Find the expected quiescent values of  $I_B$ ,  $I_E$ , and  $I_C$  (hint: start with  $I_E$  and assume  $\beta$ =100).
- c) Check to make sure that the quiescent  $I_B$  is small compared to the quiescent current through the 50k resistor. Why is it important to design the circuit so that this is the case?
- d) For roughly what range of  $V_{in}$  (+ and ) is the output free from clipping?
- e) Would you need the 45k and 50k resistors if you had a 15V power supply as well as a +15V supply available? Why?



- 3. a) What does the circuit at right do (Assume  $V_R=0$ )? Explain using the golden rules of op-amps.
- b) What is the maximum current that can be measured (without saturating the op amp) in the figure at right if  $R_f$  is 10 M? Assume  $\pm 15$  V supplies are being used to power the op amp.

