Physics 314, fall 2016
Lab 2: Gates, logic families

Lab book philosophy: Remember: Record raw measurements with units and conditions under which they were measured (including circuit diagram showing how & where measurements were made).

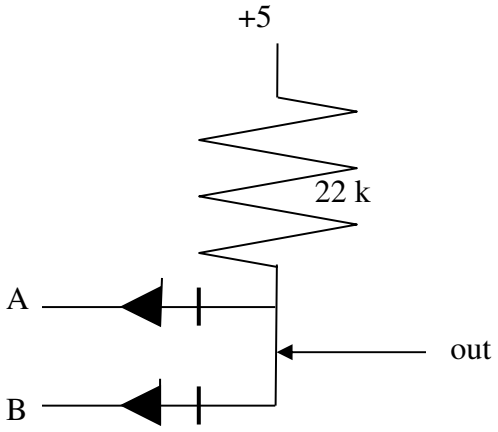
Important: Digital circuits can be destroyed if incorrect power supply values are used, or if a signal "outside the supplies" is applied to any of the inputs. The TTL chips we'll mostly be using should be powered from +5V only.

0. Getting ready to use the breadboard

Check the breadboard +5 V power supply to make sure it's within a few tenths of a volt of +5.0 V. (See me if it's not.)
Play around with the logic switches and logic indicators (lamps) on the breadboard so you see how they work.

1. A simple gate

For the following "gate circuit," record voltages and logic levels for all possible input combinations.



Based on your measurements, which one of the standard gates is this?
(A practical TTL gate follows this basic logic stage with bipolar transistor buffers that provide fast and clean switching between logic levels.)

2. TTL NAND gates

Find a datasheet for the 74LS00 online and print it out for use as a pinout reference.
a) Use the switches on the breadboard to provide 0 or +5 V to the two inputs of one of the NAND gates of a 74LS00. Record voltages and corresponding logic levels for all possible input combinations. Do your results agree with what you expect?

b) Disconnect both inputs to the NAND and note the output logic level. What input does the TTL think it "sees" when the input floats? Note: it's generally not good practice to leave an input floating—stray voltages make the input unpredictable, and CMOS chips actually use more power if the input is floating.

3. Using NAND gates to generate other logic functions

Use NAND gates to make each of the following logic functions. For each, sketch the circuit you set up and verify that the truth table is what you expect it to be.

a) Make an AND gate, that is, light one of the LEDs only when both inputs are high. (Hint: how can you make a NOT from a single NAND?)

b) Make an OR gate.

c) Make an XOR gate. (Hint: you can do it with 4 NANDs.)

4. XOR as half-adder

Leave the 4-NAND-gate version of the XOR set up. Show that the carry bit is what you expect it to be if using the XOR as a half-adder.