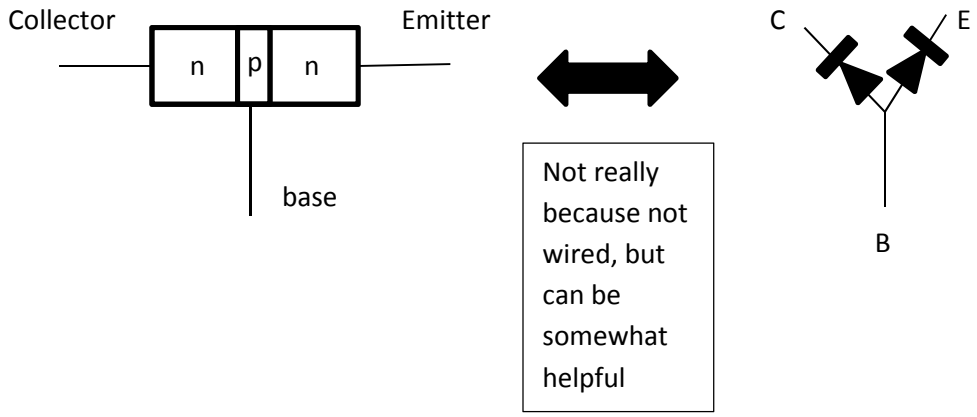
Transistors
The diode was our first semiconductor device, and our first significantly non-linear device, but all the devices we've seen up to now are passive. They can't add any power to a signal.

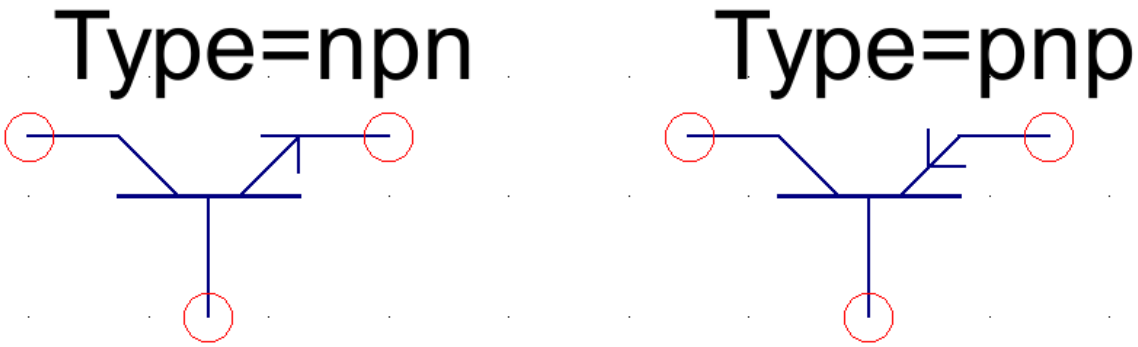
Transistors, on the other hand are classified as active. They can add power to a signal (amplify it), but it's not free, the added energy has to be supplied by an external source (power supply). The thing about devices like transistors is HOW they let you add power: it is in a controlled way.

There are several types of transistors. The two most common ones are: Bipolar Junction Transistors (bjt's) and Field Effect Transistors (FET's).

We will focus on Bipolar Junction Transistors – 3 layer semiconductor npn or pnp. These two types have similar behavior, opposite polarity in how voltages usually applied.



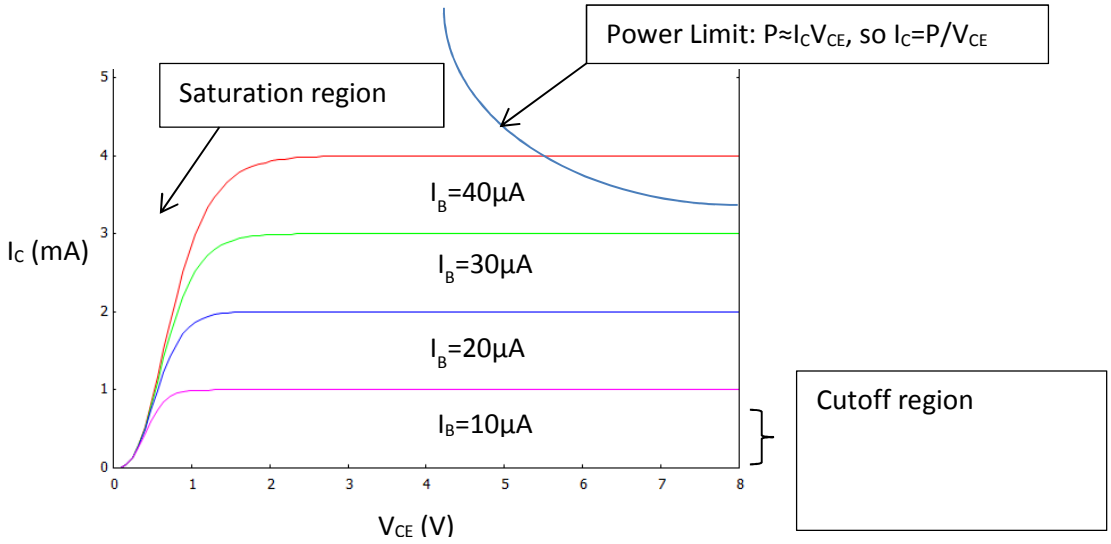
Note: that the base is drawn thing because it is physically thin as well.
Symbols: Emitter is lead with the arrow. The base points down in the fig. below.



Transistors are extremely versatile and can be used in many ways, with different biasing schemes (ways that DC voltages are applied).
Usually, the BE (base-emitter) is forward biased: $V_{BE}=V_B-V_E=0.6$ V (Silicon; 0.2 V Germanium).
The CB (collector-base) is usually reverse biased.
Electrons from the emitter flow into the base. Because the base is so thin, the influx of electrons changes its charge carrier density allows a much larger current to flow from collector to emitter. The net effect is that the bjt acts like a current controlled current valve: A small base-emitter current controls a large collector-emitter current.

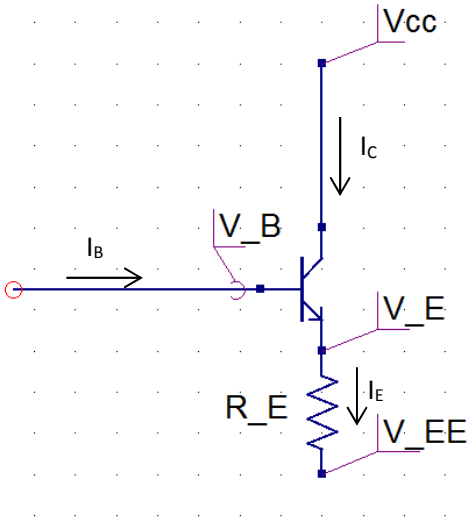
Bjt's are often characterized by the ratio of the currents involved: $\beta=i_C/i_B$. This ratio is sometimes also known as h_{FE}. β is largish. Depending on the transistor it can be in the 50-300 range.
Conservation of charge tells us in addition that $i_B+i_C=i_E$, such that another parameter can be defined: $i_C=\alpha i_E$. And you can easily tell $\alpha\leq 1$.

Because transistors are 3 terminal devices, they do not have simple I-V curves. Instead, they have families of curves. Typically for a bjt, you will see something like the curves below which shows collector current (I_C) vs. V_{CE} for a number of different base currents. That is, each curve has one base current and the graph shows how collector current varies with V_{CE} for that base current. In principle, there are an infinite number of these since any base current is possible. In practice, we usually try to map out some appropriate/useful chunk of parameter space.



In the saturation region, V_{CE} is as low as it can be and still get some I_C: CE is like a short (almost). V_{CE} in saturation is usually a couple tenths of a volt.
Above the cutoff region, right of saturation region and below the power limit is the active/linear region. Here small changes in I_B make proportionately larger changes in I_C. Ideally the characteristic curves are horizontal and parallel. In real life, they usually slope up slightly and diverge from each other as V_{CE} increases.

Simple circuit/analysis example:

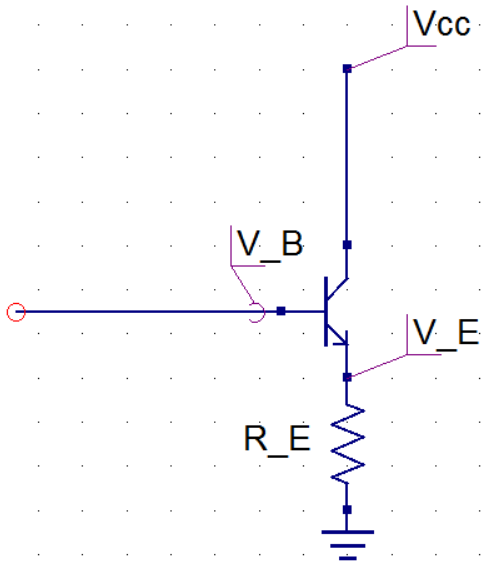


To be in the linear/active region of the characteristic curves, these conditions must apply:

V_{CE}>0.2 V (not in saturation region)
V_{BE}≈0.6 V (forward bias on V_{BE})
V_{CC}≥V_C , V_E≥V_{EE} ("between the rails"—i.e. between the limits of the external power supply).

We further more would like to not melt our transistor so $I_C V_{CE}$≤ Power Limit.

Single-sided supply version (V_{EE}=ground)

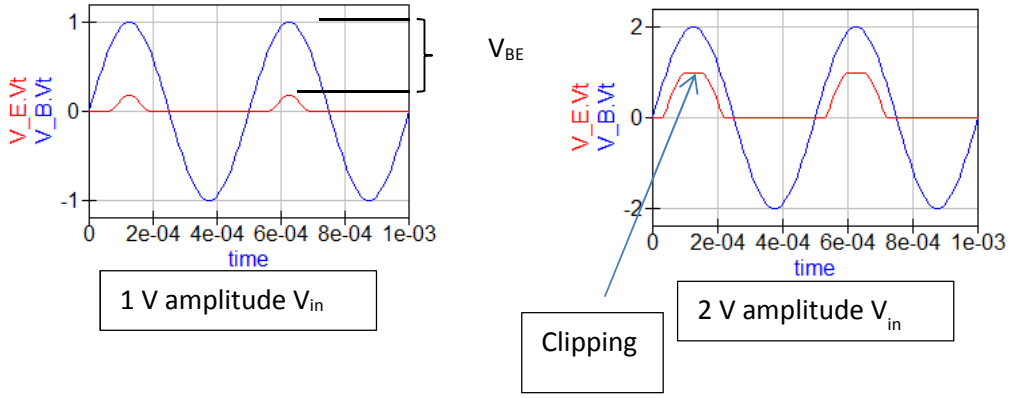


Want VBE≈0.6 V, and since VE≥0, VB>0.6 V for transistor to be "on".
If V_B<0.6 V, I_B=0, so I_C=0 and I_E=0. If I_E=0, V_{RE}=0 and so V_E=V_{out}=0V.

On the other hand, when transistor IS on, V_E=V_B-0.6V. We say the V_E *follows* V_B. While is is shifter by 0.6V, changes in V_B appear as equal sized changes in V_E. Remember that capital V's and I's are DC values and lower case is time varying. Since variations in V_B appear with equal size on V_E, we have a voltage gain of 1.

In addition, V_E<V_C-0.2V.
so, V_{in}-0.6<V_C-0.2V
and V_{in}<V_C+0.4V
so if V_{in}>V_{CC}+0.4V (in this ckt V_C=V_{CC}), transistor is full on (in saturation region) and following behavior no longer happens—output voltage maxed out=> clipping/distortion.

Input/output:



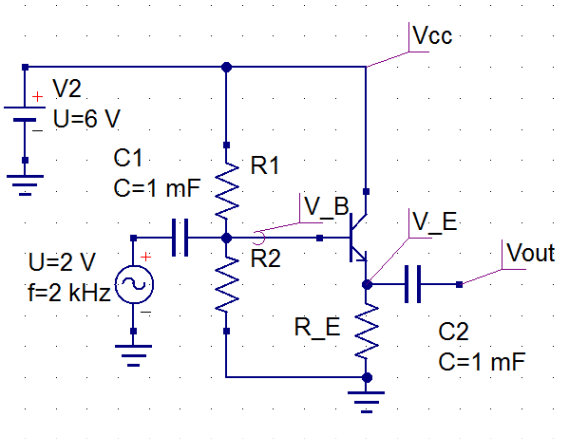
Voltage gain of 1 doesn't sound like we improved anything, why do this? Two reasons.

Current: remember that $I_C=\beta I_B$. So even though v_E is no bigger, more current can flow than I_B. So we have a power gain, even if not a voltage gain.

Relatedly: We have effectively made a high input impedance device (I_B small) with a low impedance output (I_C large). We'll see more about this in lab.

Now, an obvious problem in this case is negative going input signals turn the transistor off (actually, any below 0.6V!). So the output only follows V_{in} if it is bigger than this. Not so helpful. One fix we will see in lab is to make V_{EE} below zero. If it is enough below zero that V_{in} is always $\geq V_{EE}+0.6$, the transistor will not shut off.

Another way, which introduces good biasing schemes is to employ blocking capacitors to isolate the DC operating voltages on the transistor from the DC value of the input signal. This is obviously only useful for AC amplifiers since we are basically throwing away any DC part of the input. But, if you look back at the characteristic curves, it's obvious why we had trouble. The BE junction is like a diode. Current can only go one way through it, so the circuit above is doomed to fail for low/negative I_B. So to fix that we have to move the place where the transistor operates when no input signal is applied (called the quiescent point) to where I_B is above zero so that variations up OR down in the input can change the output without having the transistor shut off. Here's a circuit to do that. Don't panic, it's not that bad!



Here's how to think about analyzing this. If this transistor had the characteristic curves shown earlier, pick a quiescent point in the middle of the active region. Say, I_B=25uA, I_C=2.5mA. That's where we want things with no V_{in}. Since this is a follower, if we want to deal with input signals that are symmetric around zero, we want V_E to be about ½ way between the rails, so that it has the most wiggle room up and down. This also means we want V_B to be about 0.6 V higher than ½ way between the rails. So R1 and R1 are doing this—they are a voltage divider!

Conditions on R1, R2: 1) $R2/(R1+R2)=(V_{CC}-V_{EE})/2 + 0.6V$
2) We want to keep I_B and variations in it from loading down the voltage divider (which would cause V_B to droop, defeating the purpose). So….10x rule: want the current down the divider to be 10x bigger than I_B. Thus $(V_{CC}-V_{EE})/(R1+R2)>>I_B$.

R1 and R2 also affect both the input and output impedance of the circuit (more later).

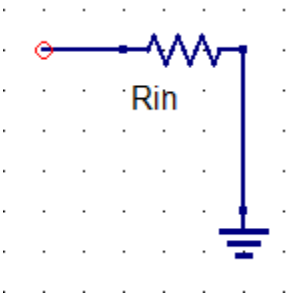
So, for the chosen quiescent point, I_C=2.5mA and $I_E \approx I_C$, so we have $R_E=V_E/I_E$. So if V_{CC}=10V and V_{EE}=0V, then R_E=5V/2.5mA=2k.

Condition 2) above says $V_{CC}/(R1+R2)$=0.25mA (10x rule) so R1+R1=40k

Condition 1) above says 5.6V=10V*R2/(R1+R2)=10V*R2/40k so R2=22.2k and R1=17.6k

Impedances of Follower

We think of anything whose input impedance we are interested in knowing as being modeled like this:



So the input impedance is defined by how much current flows when a given voltage is applied. This is really the same as when we think about it being part of voltage divider and looking at the voltage droop. Same physics, only now we think about calculating, rather than measuring for the follower.

Furthermore, in this case, we will focus on the AC characteristics, not the DC values. This reflects most of the use we will be making of these circuits, but it requires a slightly different approach to thinking about the impedance:

Looking back at the original circuit, imagine tweaking v_{in} (=v_B) up and down , v_E moves by the same amount. As a result, the current through R_E (I_E) moves proportionately: $\Delta I_E = \frac{\Delta V_E}{R_E}$. But$\Delta I_B = \frac{\Delta I_E}{\beta}$, so $\Delta I_B = \frac{\Delta V_E}{\beta R_E}$. If we identify $\Delta I_B = i_B$, we can write $v_{in} = Z_{in} i_{in} = \frac{Z_{in}\Delta V_E}{\beta R_E} = \frac{Z_{in} v_{in}}{\beta R_E}$ and then $Z_{in} = \beta R_E$. So, the input impedance is β times R_E. Since β is big, this can make the input impedance large—which we generally like (remember the rule of 10x). A common use for a follower is as the first thing a sensor with a high output impedance sees, this keeps the sensor output from drooping.

If the follower has a load, we see a weakness in this simple version. The load is in parallel with R_E, so the input impedance changes depending on what the load the follower is driving is. There's also a small contribution that arises due to an effective resistance (r_E) associated with the BE junction, so a fuller description is $Z_{in}=r_E+\beta R_E \| R_{load}$.

How about the output impedance for the emitter follower? Similarly, we model this as a Thevenin voltage in series with some R_{Th}. $v_{Th}=v_{OC}=v_E=v_{in}$. So we need i_{SC}. But, we already know this. If we short the output to ground, the max current that flows is i_E which is just βi_B. So what is i_B?

$$i_B = \frac{v_B}{r_S + Z_{in}} = \frac{v_B}{r_S + \beta R_E}$$

where r_S is the resistance of the source that is supplying the input to the follower. But, when the output is shorted, $R_E=0$ so then $i_B = \frac{v_B}{r_S}$.

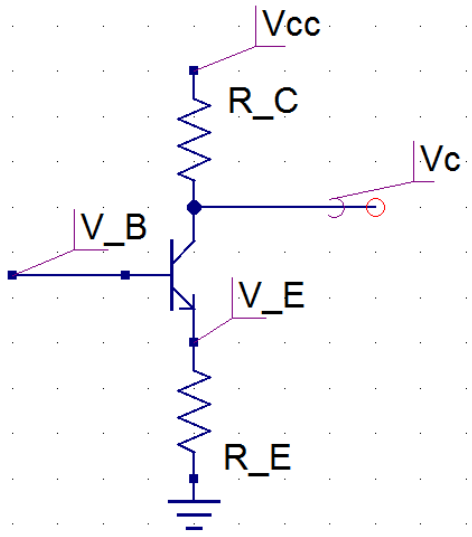
Finally $R_{Th} = \frac{v_{Th}}{i_{SC}} = \frac{v_{in}}{\beta i_B} = \frac{v_{in} r_S}{\beta v_B} = \frac{r_S}{\beta}$. So the output impedance is β times smaller—just what we want to drive loads without drooping. Again, if we take into account the effective resistance of the BE junction, that's in series with this so

$Z_{out} = \frac{r_S}{\beta} + r_E$.

Later, when we add a bias network we would have to include the bias network resistors in parallel with r_S. And again, the dependence of the output impedance on the source resistance is not optimal.

The net effect of the follower then is to add power to the signal and to transform the impedance.

Ok, so the emitter follower had current gain, but no voltage gain. To get voltage gain, we need a different configuration.
Common emitter amplifer.



DC:
$V_E=V_B-0.6V$
$V_C=V_{CC}-I_CR_C$
$I_E=V_E/R_E$

AC:
$v_E=v_B$

$\Delta V_C=\Delta(V_{CC}-I_CR_C)$
Since V_{CC} (and R_C)is constant, its Δ is zero so we have
$v_C= -i_CR_C$ (note negative!)
since $i_C\approx i_E=v_E/R_E$

together, $v_C = -v_E \frac{R_C}{R_E}$

$v_C = -v_B \frac{R_C}{R_E}$, since v_C is v_{out} and v_B is v_{in}. So $-R_C/R_E$ is the voltage gain. The negative means it is an inverting amplifier: a tweak of v_{in} up, makes a tweak of v_{out} down.

Impedances?
Input: Same as an unloaded emitter follower (same process to analyze).
Output:
Connect R_L from V_C to ground. $i_{out} = v_{out}/R_L$.
$v_{out}=-R_C(i_C+i_{out})$
so
$i_{out} = \frac{R_C(i_C+i_{out})}{R_L}$
And then solve for i_{out}:
$i_{out} = \frac{-R_Ci_C}{R_L+R_C}$

Back to $v_{out}=-R_C(i_C+i_{out})= -R_C(i_C+v_{out}/R_L)$

Solve for v_{out}:
$v_{out} = \frac{-R_Ci_C}{R_L+R_C}R_L$.
Now, imagine load goes to infinity (this is v_{OC}): $v_{out}\rightarrow -i_CR_C$.
As load goes to zero (short) $v_{out}\rightarrow 0$.

Then
$i_{out} = \frac{-R_Ci_C}{R_L+R_C} = \frac{v_{OC}}{R_L+R_C}$, and notice that as $R_L\rightarrow 0$ (short circuit) $i_{out}=v_{OC}/R_C$. By inspection, we see this says that $R_{Th}=R_C$! Whew!