PHY6226

Zigbee 3.0 (IEEE 802.15.4) System on Chip

Key Features

- High-performance Low-power 32-bit processor with SWD
- Memory
  - 128KB-8MB in-system flash memory
  - 64KB SRAM, all programmable retention in sleep mode
  - 4-way instruction cache with 8KB Cache RAM
  - 96KB ROM
  - 256bit eFuse
- 22 General Purpose I/O pins
  - GPIO status retention in off/sleep mode
  - configurable as serial interface and programmable IO MUX function mapping
  - All pins can be configured for wake-up
  - All pins for triggering interrupt
  - 3 Quadrature Decoder(QDEC)
  - 6-channel PWM
  - 2-channel PDM/I2C/SPI/UART
  - 4-channel DMA
- DMIC/AMIC with microphone bias
- 8-channel 12bit ADC with low noise voice PGA
- 6-channel 32bit timer, one watchdog timer
- Real timer counter (RTC)
- Power, Clock, Reset Controller
- Flexible Power management
  - Operating Voltage range 1.8V to 3.6V
  - Embedded buck DC-DC and LDOs
  - Battery monitor
- Power consumption
  - 0.3uA @ OFF Mode (IO wake up only)
  - 1uA @ Sleep Mode with 32KHz RTC
  - 13uA @ Sleep Mode with 32KHz RTC and all SRAM retention
  - Receive mode: 4mA @3.3V power supply
  - Transmit mode: 4.6mA (0dBm output power) @3.3V power supply
  - MCU: <60uA/MHz
- RC Oscillator hardware calibrations
  - Internal High/Low frequency RC osc
  - 32KHz RC osc for RTC with +/-500ppm accuracy
  - 32MHz RC osc for HCLK with 3% accuracy
- 2.4 GHz transceiver
  - Compliant to Zigbee 3.0
  - Sensitivity: -103dBm@Zigbee 3.0 250Kbps data rate
  - TX Power -20 to +10dBm in 3dB steps
  - Single-pin antenna: no RF matching or RX/TX switching required
  - RSSI (1dB resolution)
  - Antenna array and optional off-chip RF PA/LNA control interface
- AES-128 encryption hardware
- Link layer hardware
  - Automatic packet assembly
  - Automatic packet detection and validation
  - Auto Re-transmit
  - Auto ACK
  - Hardware Address Matching
  - Random number generator
- Operating temperature:
  - -40˚C ~+85˚C (Consumer)
  - -40˚C ~+105˚C (Industrial)
- RoHS Package: QFN32(4mm x 4mm)
- Applications: wearables, beacons, home and building, health and medical, industrial and manufacturing, retail and payment, data transmission, PC/mobile/TV peripherals, internet of things (IoT)

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2021.7	1.0	The following content has been added, updated or corrected: • **Maximum MSL** parameter updated: “Moisture Sensitivity Level: 3”.

Table of Contents

1 Introduction 1
2 Product Overview 2
2.1 Block Diagram 2
2.2 Pin Assignments and Functions 3
2.2.1 PHY6226 (QFN32) 3
2.2.1.1 Pin Assignment 3
2.2.1.2 Pin Functions 4
3 System Block 5
3.1 CPU 5
3.2 Memory 5
3.2.1 ROM 7
3.2.2 SRAM 7
3.2.3 FLASH 7
3.2.4 eFuse 7
3.2.5 Memory Address Mapping 7
3.3 Boot and Execution Modes 8
3.3.1 Boot Loader 8
3.4 Power, Clock and Reset (PCR) 9
3.5 Power Management (POWER) 9
3.6 Low Power Features 11
3.6.1 Operation and Sleep States 11
3.6.1.1 Normal State 11
3.6.1.2 Clock Gate State 11
3.6.1.3 System Sleep State 11
3.6.1.4 System Off State 11
3.6.1.5 UVLO 11
3.6.2 State Transition 12
3.6.2.1 Entering Clock Gate State and Wake-up 12
3.6.2.2 Entering Sleep/off States and Wake-up 12
3.7 Interrupts 12
3.8 Clock Management 13
3.9 IOMUX 14

3.10 GPIO 16
3.10.1 DC Characteristics 17
4 Peripheral Blocks 18
4.1 2.4GHz Radio 18
4.2 Timer/Counters (TIMER) 18
4.3 Real Time Counter (RTC) 18
4.4 AES-ECB Encryption (ECB) 18
4.5 Watchdog Timer (WDT) 18
4.6 SPI (SPI0, SPI1 Two Independent Instances) 19
4.7 I2C (I2c0, I2c1 Two Independent Instances) 19
4.8 UART (UART0, UART1 Two Independent Instances) 19
4.9 DMIC/AMIC Data Path 19
4.9.1 Filter Chain Design 21
4.9.2 Auto Mute Process 22
4.9.3 Digital Gain Control 22
4.9.4 Voice Compression 22
4.10 Pulse Width Modulation (PWM) 22
4.11 Quadrature Decoder (QDEC) 24
4.12 Key Scan (KSCAN) 24
4.13 Analog to Digital Converter (ADC) with Programmable Gain Amplifier (PGA) 24
4.13.1 PGA Path 25
4.13.2 ADC Path 25
4.13.3 ADC Channel <3:0> Connectivity 27
5 Absolute Maximum Ratings 29
6 Operating Conditions 30
7 Radio Transceiver 31
7.1 Radio Current Consumption 31
7.2 Transmitter Specification 31
7.2.1 Zigbee 3.0 TX 31
7.3 Receiver Specification 31
7.3.1 Zigbee 3.0 RX 31
7.4 RSSI Specifications 33
8 Glossary 34
9 Ordering information 35

9.1 Chip Marking Example 35
9.2 Chip Marking Rule 35
10 Package dimensions 36
11 Sample Application and Layout Guide 37
11.1 Sample Application (QFN32) 37
11.1.1 With DCDC 37
11.1.2 Without DCDC 38
11.2 Layout Guide 38
11.2.1 Placement 38
11.2.2 Bypass Capacitor 38
11.2.3 Layer Definition 39
11.2.4 Reference clock and trace 39
11.2.5 Power line or plane 39
11.2.6 Ground Via 39

1 Introduction

PHY6226 is a System on Chip (SoC) for Zigbee 3.0 applications. It has high-performance low-power 32-bit processor with 64K retention SRAM, 128KB-8MB flash, 96KB ROM, 256bit efuse, and an ultra-low power, high performance, multi-mode radio. Also, PHY6226 can support Zigbee with security, application and over-the-air download update. Serial peripheral IO and integrated application IP enables customer product to be built with minimum bill-of-material (BOM) cost.

2 Product Overview

2.1 Block Diagram

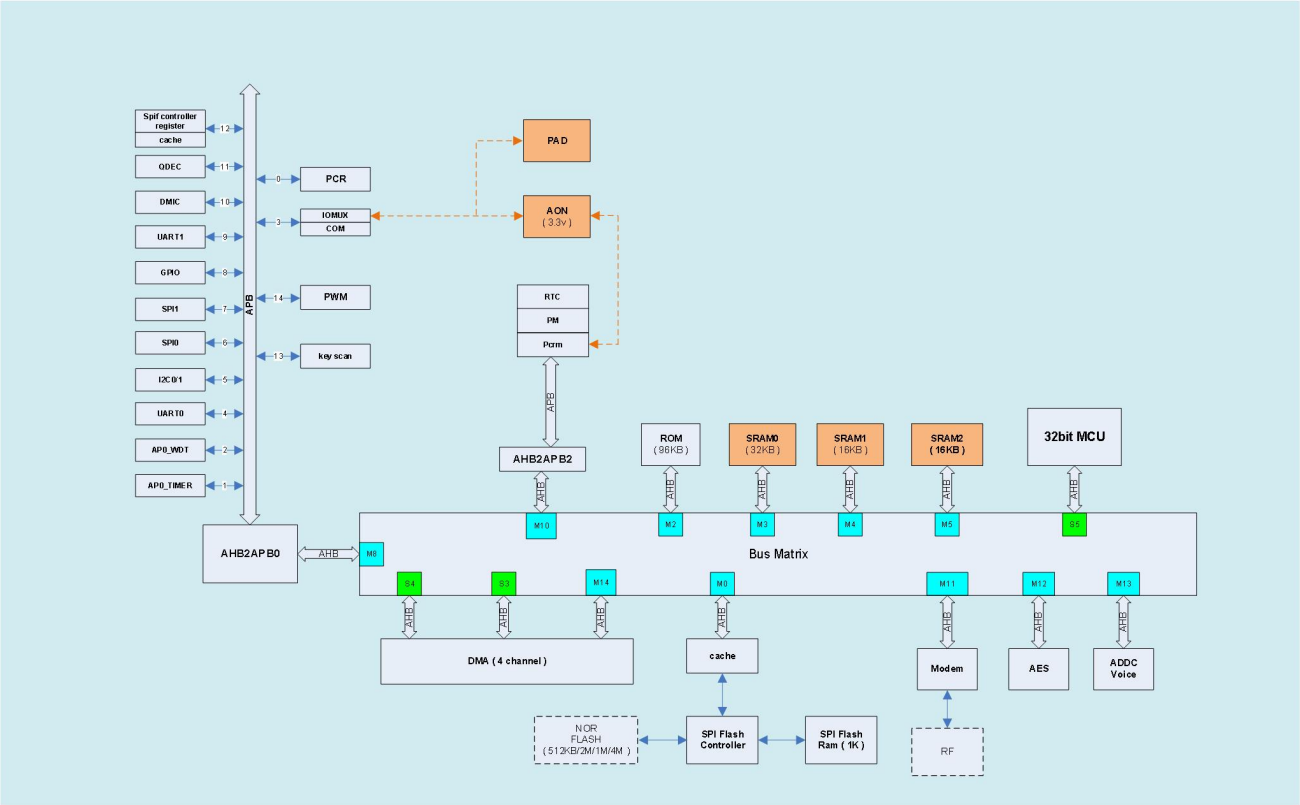


Figure 1: PHY6226 block diagram

2.2 Pin Assignments and Functions

This section describes the pin assignment and the pin functions for the package type of QFN32.

2.2.1 PHY6226 (QFN32)

2.2.1.1 Pin Assignment

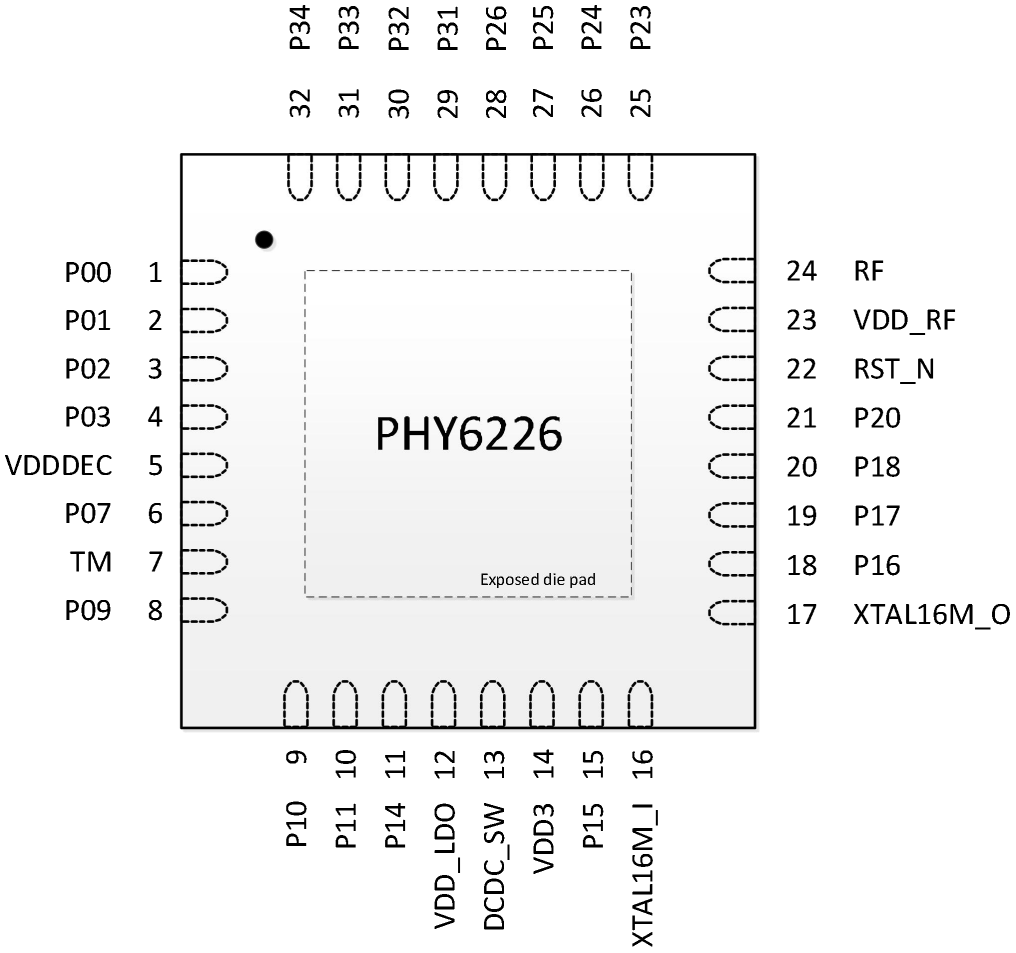


Figure 2: Pin assignment – PHY6226 QFN32 package

2.2.1.2 Pin Functions

Pin	Pin name	Description
1	P0	GPIO 0
2	P1	GPIO 1
3	P2/SWD_IO	GPIO 2/SWD debug data inout
4	P3/SWD_CLK	GPIO 3/SWD debug clock
5	VDDDEC	1.2V decoupling pin
6	P7	GPIO 7
7	TM	test mode enable
8	P9	GPIO 9
9	P10	GPIO 10
10	P11/AIO_0	GPIO 11/ADC input 0
11	P14/AIO_3	GPIO 14/ADC input 3
12	VDD_LDO	Internal LDO power supply/DCDC feedback
13	DCDC_SW	DCDC output
14	VDD3	3.3V power supply
15	P15/AIO_4	GPIO 15/ADC input 4/ micbias output
16	XTAL16M_I	16MHz crystal input
17	XTAL16M_O	16MHz crystal output
18	P16/XTAL32K_I	GPIO16/ 32.768KHz crystal input
19	P17/XTAL32K_O	GPIO17/ 32.768KHz crystal output
20	P18/AIO_7	GPIO 18/ADC input 7/ PGA negative input
21	P20/AIO_9	GPIO 20/ADC input 9/ PGA positive input
22	RST_N	reset, active low
23	VDD_RF	power supply decoupling for RF transceiver
24	RF	RF antenna
25	P23/AIO_1	GPIO 23/ADC input 1/micbias reference
26	P24/AIO_2	GPIO 24/ADC input 2
27	P25/AIO_8	GPIO 25/ADC input 8
28	P26	GPIO 26
29	P31	GPIO 31
30	P32	GPIO 32
31	P33	GPIO 33
32	P34	GPIO 34

*Note： All gpio support 1M/150kΩ pull up, 150kΩ pull down.

Table 1: Pin functions of PHY6226 QFN32 package

3 System Block

The system block diagram of PHY6226 is shown in **Figure 1**.

3.1 CPU

The PHY6226 has a high-performance low-power 32-bit processor. The CPU, memories, and all peripherals are connected by AMBA bus fabrics.

The CPU will play controller role in Zigbee modem and run all user applications.

3.2 Memory

PHY6226 has total 96KB ROM, 64KB SRAM, 128KB-8MB FLASH and 256bit efuse. The physical address space of these memories is shown in **Figure 3**.

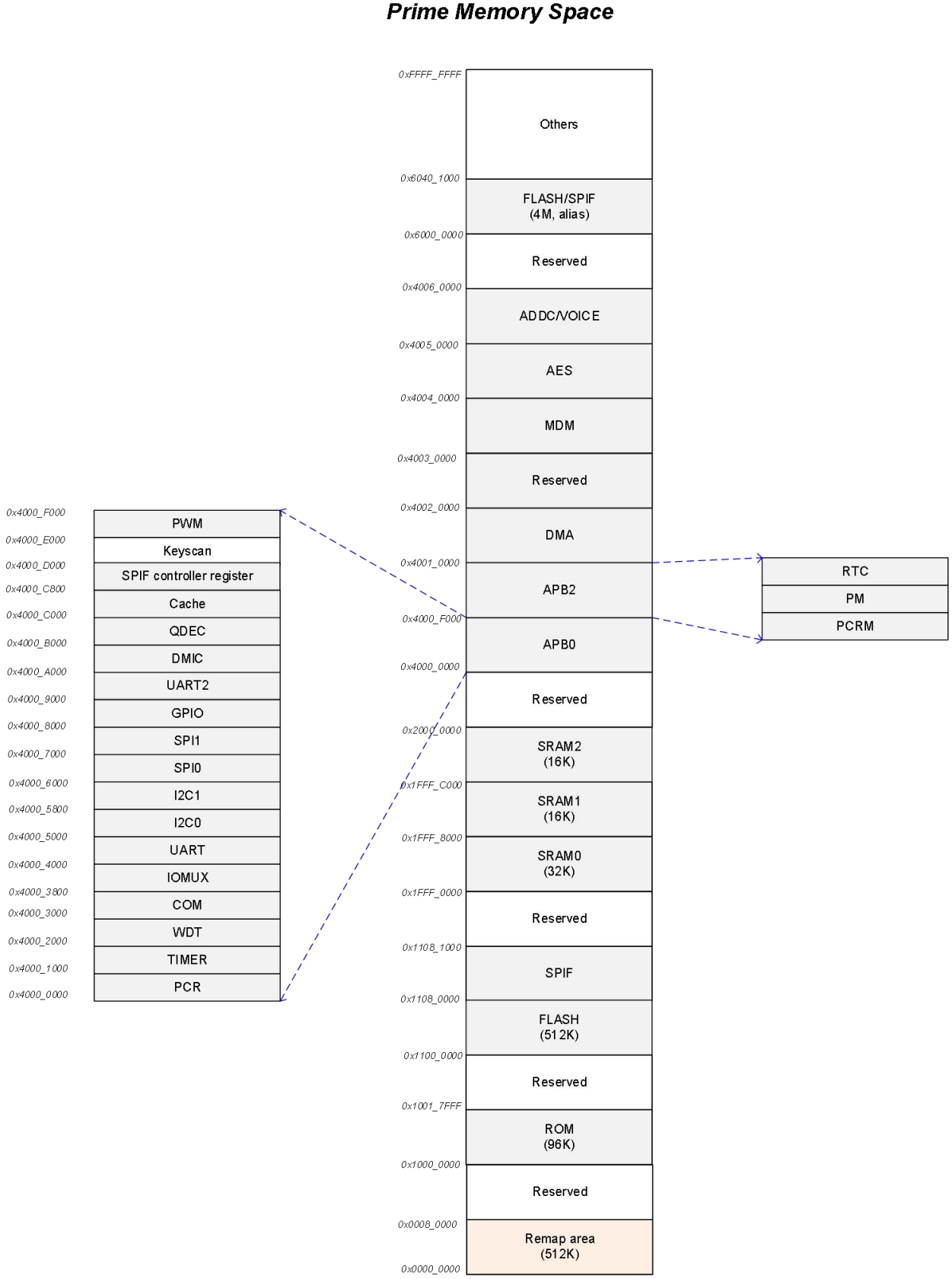


Figure 3: PHY6226 memory space

3.2.1 ROM

PHY6226 has 1 ROM.

	SIZE	CONTENT
ROM	96KB	Boot ROM. Protocol stack. Common peripheral drivers. ATE AT command.

Table 2: List of ROM

3.2.2 SRAM

PHY6226 has 5 SRAM blocks. All 5 SRAM blocks have retention capability, which can be configured individually. Normal operating voltage is 1.2V, and the voltage is adjustable at retention. All SRAM blocks can be used to store program or data.

	SIZE	CONTENT
SRAM0	32KB	
SRAM1	16KB	
SRAM2	16KB	
SRAM_BB	4KB	
SRAM_cache	8KB	

Table 3: List of SRAMs

3.2.3 FLASH

The size of FLASH can be 128KB to 8MB. Supports single-wire, 2-wire, and 4-wire reading, 2 wire reading mode by default. For FLASH greater than 4MB, supporting indirect addressing is needed.

3.2.4 eFuse

PHY6226 integrates 256bits internal nonvolatile one-time programmable EFUSE storage. With a serial interface, 1-bit can be programmed at one clock in program mode and 1-bit can be read at one time in read mode.

3.2.5 Memory Address Mapping

Name	Size（KB）	Master	Physical Address
ROM	96	32-bit	1000_0000~1001_7FFF
RAM0	32	32-bit	1FFF_0000~1FFF_7FFF
RAM1	16	32-bit	1FFF_8000~1FFF_CFFF
RAM2	16	32-bit	1FFF_D000~1FFF_FFFF
FLASH	512	32-bit	1100_0000~1107_FFFF 6000_0000~603F_FFFF

Table 4: Memory address mapping

3.3 Boot and Execution Modes

Only in CP Chip form, the chip enters CP boot mode after power on. ROM1 is then aliased to the 0x0 address and the chip program starts from ROM1.

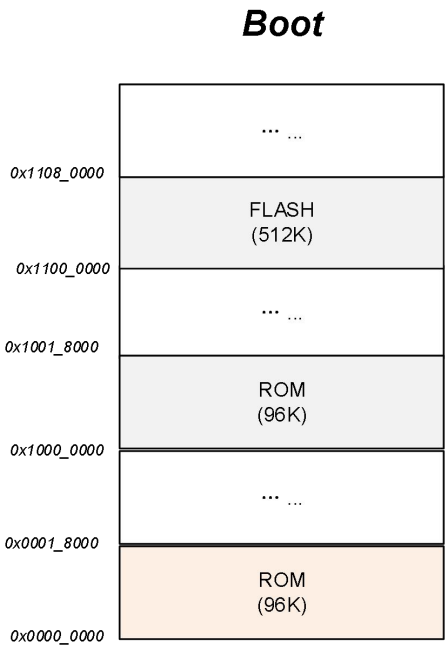


Figure 4: PHY6226 boot mode

3.3.1 Boot Loader

The boot loader in the ROM has the basic structure as shown below. The content in the FLASH should be specifically defined to allow boot loader to identify whether the FLASH content is valid, as shown in the example below. If the FLASH is valid, the ROM boot loader will put the chip in the normal mode and start normal program execution. If the FLASH is not valid, the boot loader will enter FLASH programming mode.

Address	Variable	Content
0	PRODUCT_MODE	Identify the chip mode
4	CODE_BASE	The base address of the code
8	CODE_LEN	The length of the code
C	BOOT_MODE	Identify mirror or FLASH mode

Table 5: Flash content example

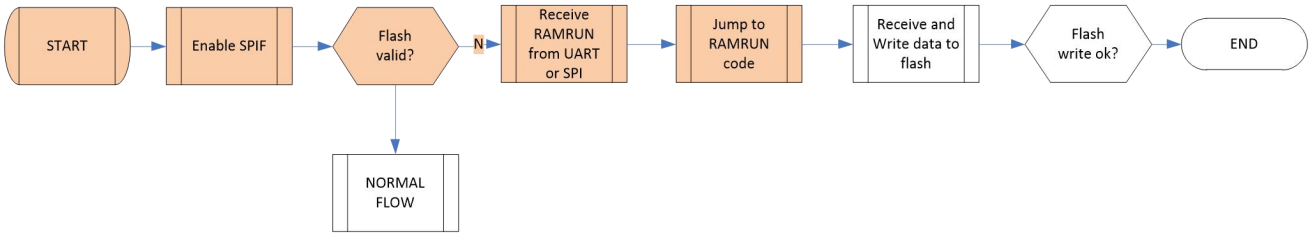


Figure 5: Bootloader flow

3.4 Power, Clock and Reset (PCR)

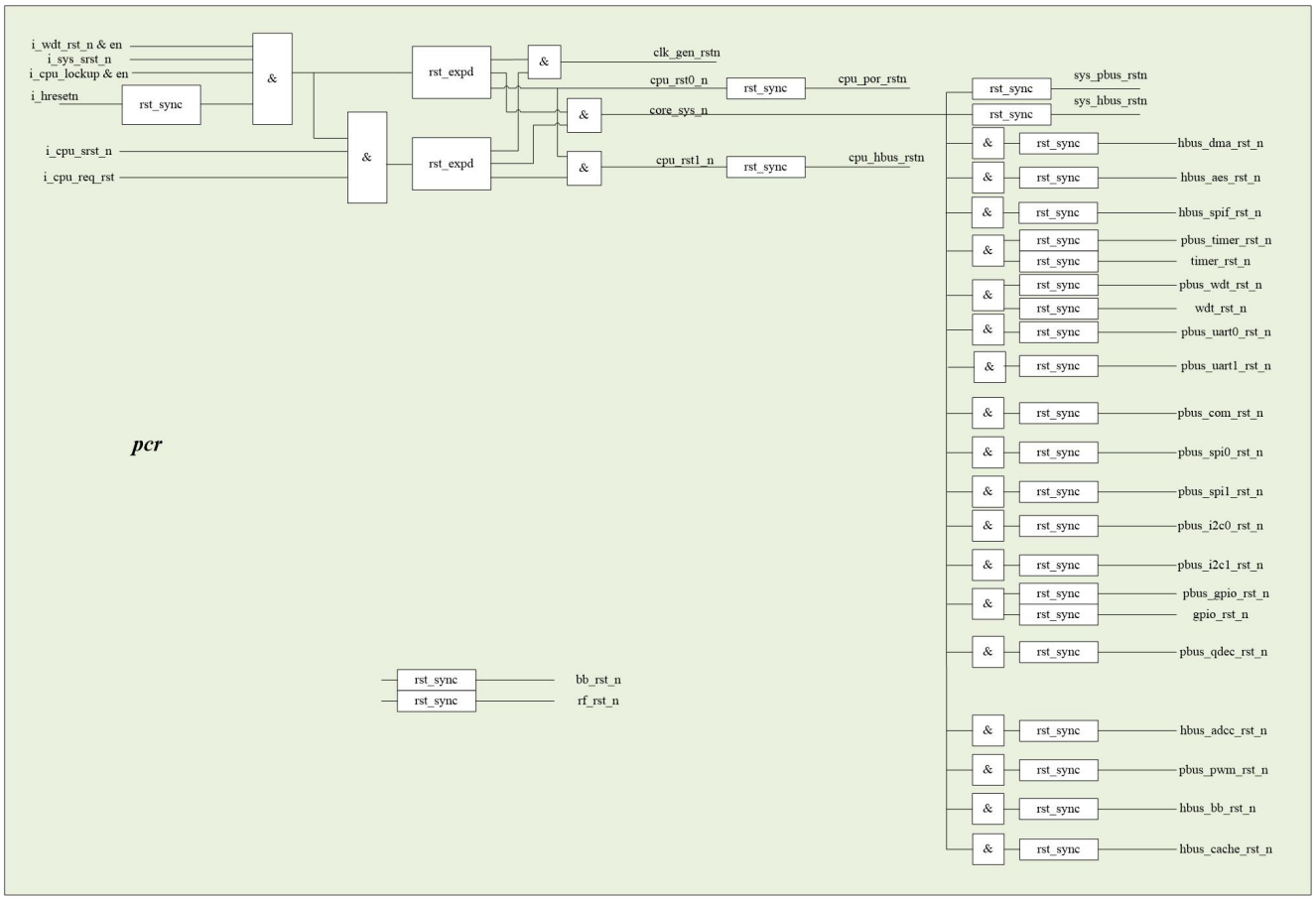


Figure 6: PHY6226 power, clock and reset

3.5 Power Management (POWER)

The power management system is highly flexible with functional blocks such as the CPU, radio transceiver, and peripherals saving separate power state control in addition to the System Sleep mode and OFF modes. When in System Normal mode, all functional blocks will independently be turned on depending on needed application functionality.

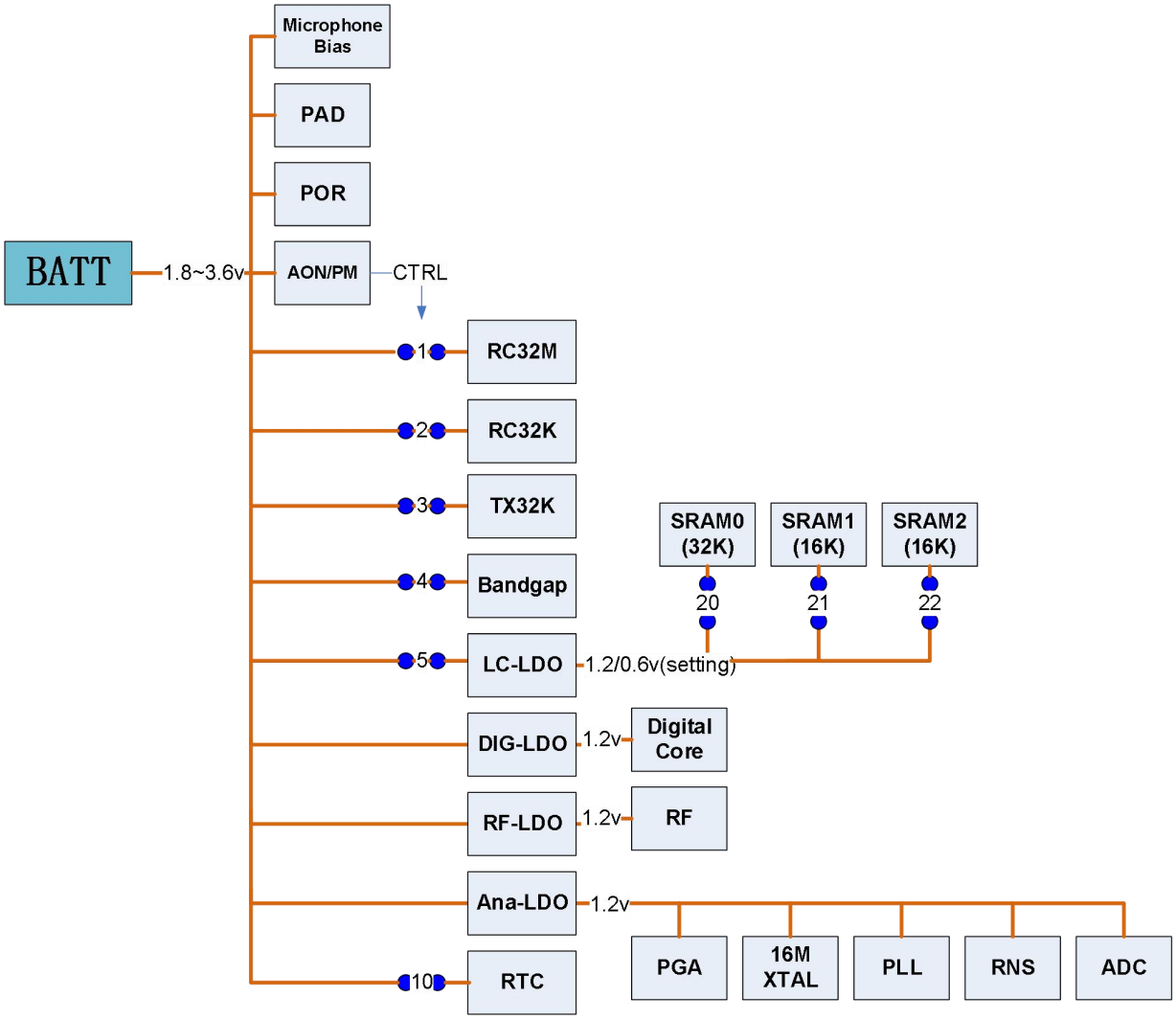


Figure 7: Power system

The following diagram is Normal, Sleep and Off mode. Switches are optional depending on user's request.

Switch	Normal	Sleep	Off
1RC32M	On	Off	Off
2RC32K	On	Optional	Off
3XT32K	On	Optional	Off
4bandgap	On	Off	Off
5LC-LDO	On	On	Off
10RTC	On	Optional	Off
20SRAM-32K	1.2v	0.6v	0
21SRAM-16K	1.2v	0.6v	0
22SRAM-16K	1.2v	0.6v	0

Table 6: Flash Switches of different power modes

3.6 Low Power Features

3.6.1 Operation and Sleep States

3.6.1.1 Normal State

3.6.1.2 Clock Gate State

The CPU executes WFI/WFE to enter clock gate state. After wake-up from clock-gate state, the CPU continues to execute the program from where it stopped. The wake-up sources includes interrupts and events. The wake-up sources are configured by the software according to applications.

3.6.1.3 System Sleep State

The wake-up sources include:

- IO
- RTC
- RESET
- UVLO reset

3.6.1.4 System Off State

The wake-up sources include：

- IOs
- RESET
- UVLO reset

3.6.1.5 UVLO

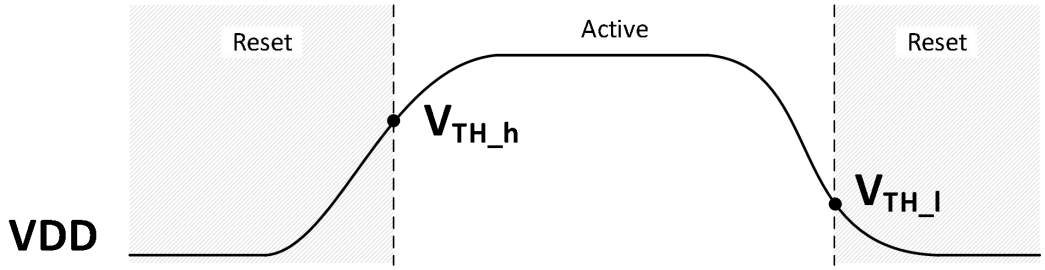


Figure 8: UVLO reset

VDD > VTH_h, release reset; VDD < VTH_l, enter reset.

VDD	Min.	TYP	Max.	Unit
V_{TH_h}	1.7	1.74	1.78	V
V_{TH_l}	1.63	1.66	1.69	V

Table 7: UVLO

3.6.2 State Transition

3.6.2.1 Entering Clock Gate State and Wake-up

CPU executes WFI/WFE.

3.6.2.2 Entering Sleep/off States and Wake-up

The PM registers identify whether the CPU is in mirror mode or FLASH mode before sleep or off, and record the remap and vectors. The CPU configures the corresponding PM registers to put the chip into sleep mode. After wake-up, the chip enters boot mode to execute boot code in the ROM. The ROM code checks the mode before sleep/off and the remap information, perform corresponding configurations, and starts to execute the program.

3.7 Interrupts

Interrupt Name	MCU Interrupt Number
	0
MCU(coretime irq)	1
	2
	3
bb_irq	4
kscan_irq	5
rtc_irq	6
cpcom_ap_ipc_irq	7
apcom_ap_ipc_irq	8
	9
wdt_irq	10
uart0_irq	11
i2c0_irq	12
i2c1_irq	13
spi0_irq	14
spi1_irq	15
gpio_irq	16
uart1_irq	17
spif_irq	18
dmac_intr	19
timer_irq[1]	20
timer_irq[2]	21
timer_irq[3]	22
timer_irq[4]	23
timer_irq[5]	24
timer_irq[6]	25
	26
	27
aes_irq	28

Interrupt Name	MCU Interrupt Number
adcc_irq	29
qdec_irq	30
	31

Table 8: Interrupts

3.8 Clock Management

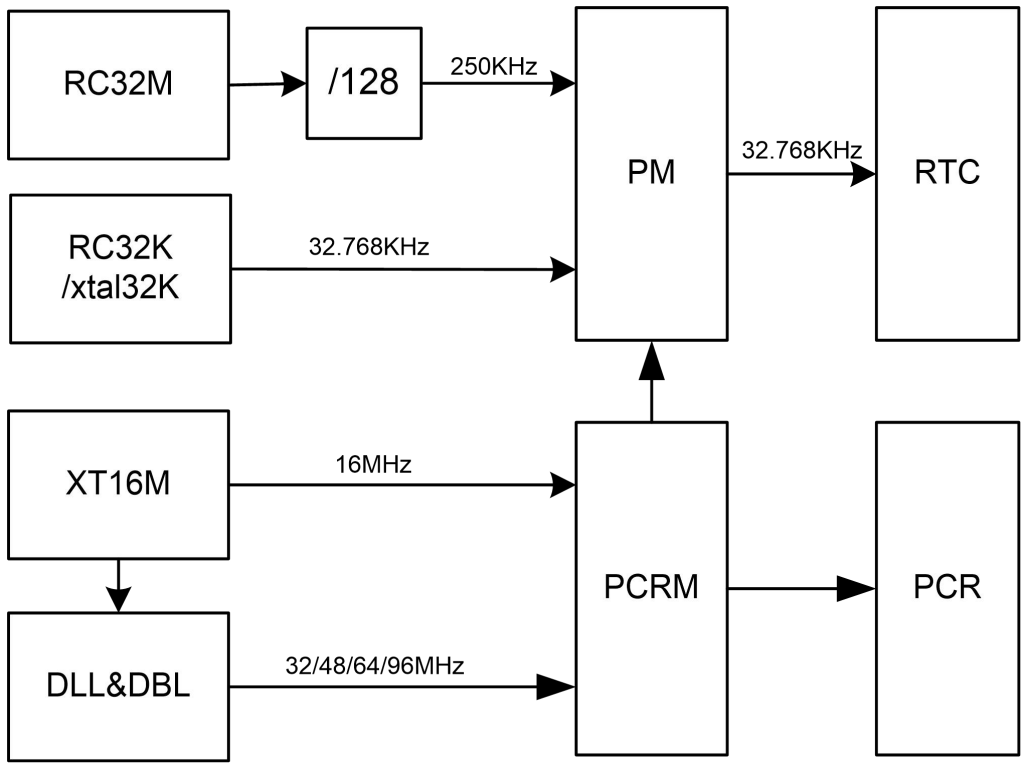


Figure 9: Clock management

There are two crystal clock sources: 16MHz crystal oscillator (XT16M) and 32.768kHz crystal oscillator (XT32k), of which the 32.768k crystal oscillator is optional. There are also two on chip RC oscillators: 32MHz RC oscillator (RC32M) and 32kHz RC oscillator (RC32k), both of which can be calibrated with respect to 16MHz crystal oscillator. If 32.768kHz crystal is not installed, RC32k oscillator would be periodically calibrated and used for RTC. At initial power up or wake up before XT16M oscillator starts up, RC32M is used as the main clock. An on-chip DLL generates higher frequency clocks such as 32/48/64/96MHz.

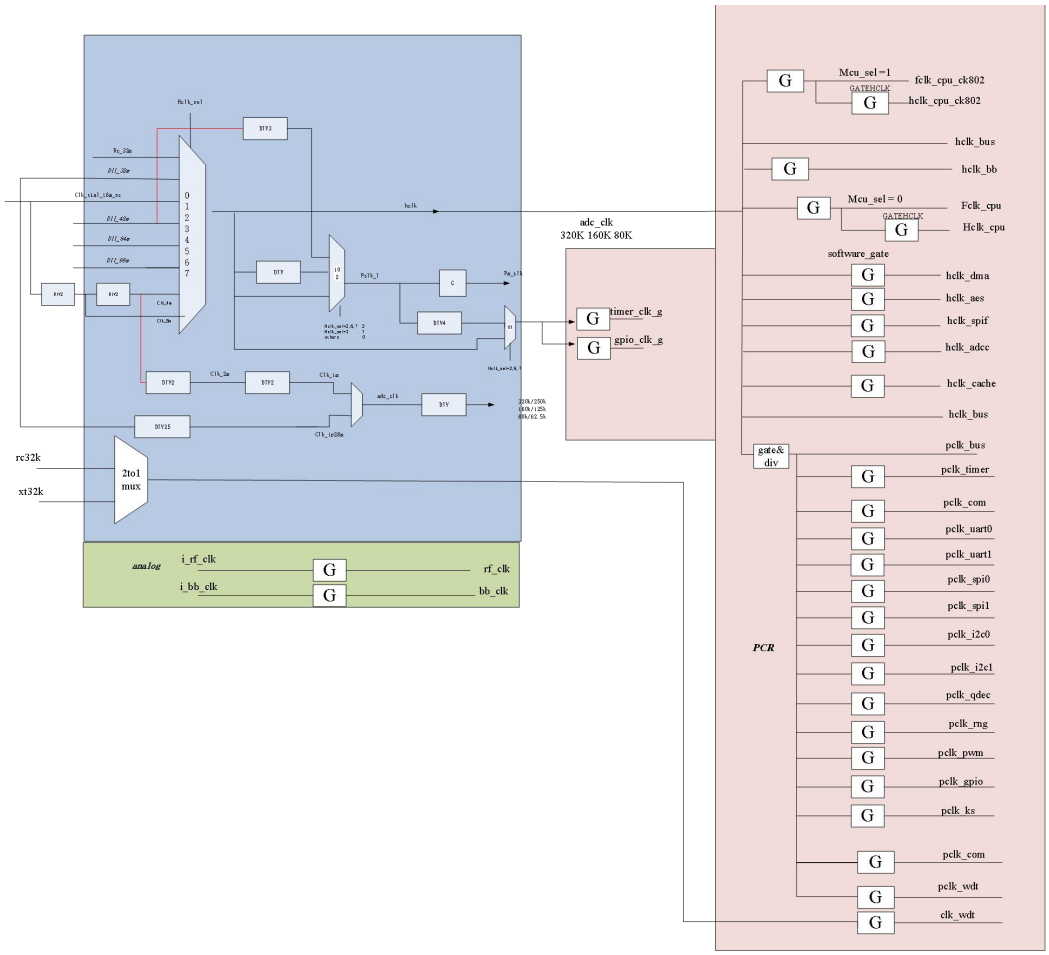


Figure 10: Clock structure diagram

3.9 IOMUX

The IOMUX provides a flexible I/O configuration, as the ports of most of the peripherals can be configured and mapped to any of the physical I/O pads (I/O at die boundary). These peripheral modules include I2C 0-1, UART0-1, PWM 0-5, SPI 0-1, Quadrature Decoder etc. However for other specific purpose peripherals, their IOs mappings are fixed when they are enabled. These specific purpose peripherals include JTAG, analog_ios, GPIOs and key scan.

Figure 11 below shows the IOMUX functional diagram.

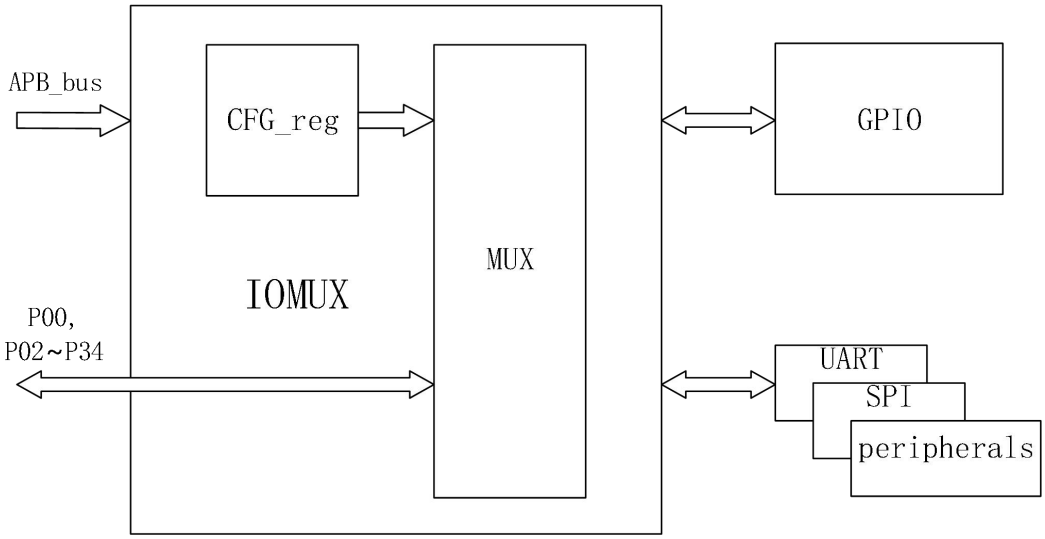


Figure 11: IOMUX structure diagram

There are 34 configurable pads which are from P00 to P07 and from P09 to P34. P08 pad is assigned for TM pin which is a test mode pin. The table blow shows the mapping of the peripheral IOs that can be mapped through IOMUX. These include I2C 0-1, UART 0-1, PWM 0-5, SPI 0-1, Quadrature Decoder, 1.28MHz clock and dmic_out.

On the other hand, there are also special purpose peripherals, whose IOs are fixed to certain physical pads, when these peripheral functions are enabled. These special purpose peripherals include: JTAG, analog I/Os (ADC inputs), GPIO, and key scan. When they are enabled, their IOs are mapped to physical pads according to the following table.

#	QFN32			Name
0	GPIO_P00	GPIO		mk_in[0]
1	GPIO_P01	GPIO		mk_out[0]
2	GPIO_P02	SDW_IO		mk_in[1]
3	GPIO_P03	SDW_CLK		mk_out[1]
4	GPIO_P07	GPIO		mk_in[10]
5	TEST_MODE			
6	GPIO_P09	GPIO		mk_out[4]
7	GPIO_P10	GPIO		mk_in[4]
8	GPIO_P11	GPIO	analog_io[0]	mk_out[11]
9	GPIO_P14	GPIO	analog_io[3]	mk_out[2]
10	GPIO_P15	GPIO	analog_io[4]	mk_in[2]
11	GPIO_P16	XTALI(ANA)		mk_out[10]
12	GPIO_P17	XTALO(ANA)		mk_out[9]
13	GPIO_P18	GPIO	analog_io[7]	mk_in[5]
14	GPIO_P20	GPIO	analog_io[9]	mk_out[5]
15	GPIO_P23	GPIO	analog_io[1]	mk_in[6]
16	GPIO_P24	GPIO	analog_io[2]	mk_out[3]
17	GPIO_P25	GPIO	analog_io[8]	mk_in[3]
18	GPIO_P26	GPIO		mk_out[8]
19	GPIO_P27	GPIO		mk_in[9]

20	GPIO_P31	GPIO	mk_out[7]
21	GPIO_P32	GPIO	mk_in[7]
22	GPIO_P33	GPIO	mk_out[6]
23	GPIO_P34	GPIO	mk_in[8]

Table 9: Peripheral IO mapped through IOMUX (special purpose)

In the IOMUX table above, the first column is the IO pad mapping in default mode, when no IOMUX function is selected and no special purpose peripherals such as analog IO, GPIO<0:3>, key scan, are enabled. In this mode, pin<0:3> are used for JTAG.

When analog IOs are enabled, pins<11:15>, <18:20> are connected to internal analog IOs. More specifically, analog_io<0:4><9> are connected to ADC inputs, analog_io<7,8> are connected to PGA inputs.

In JTAG mode, data output for JTAG test mode is mapped to P00; data input for JTAG test mode is mapped to P01; mode control input for JTAG test mode is mapped to P02; clock input for JTAG test mode is mapped to P03.

3.10 GPIO

The General Purpose I/Os are a type of peripheral that can be mapped to physical I/O pads and programmed by software. The flexible GPIO are organized as PORT A. PortA has bi-direction 18 bit lines, e.g., GPIO_PORT A[22:0]. With default setting, physical pads: P00-P34 are connected to PortA. When all GPIOs are enabled, as described in the IOMUX table in IOMUX section.

All PortA pins can be configured as bi-directional serial interface, by selecting as input or output direction, and their corresponding data can be either read from or written to registers. All PortA and pins support wake-up and debounce function, but only 18 PortA pins support interrupt.

Each GPIO pins can be pulled up to VDD3 or pulled down to ground by adding pull up or pull down resistors to have default functions/states.

For more detailed info, please refer to “PHY62xx GPIO Application Notes”, in software SDK document folder.

#	QFN32	Default MODE	Default IN_OUT	IRQ	Wakeup	ANA_IO
0	GPIO_P00	GPIO	IN	√	√	
1	GPIO_P01	GPIO	IN	√	√	
2	GPIO_P02	SWD_IO	OUT	√	√	
3	GPIO_P03	SWD_CLK	IN	√	√	
4	GPIO_P07	GPIO	IN	√	√	
5	TEST_MODE					
6	GPIO_P09	GPIO	IN	√	√	
7	GPIO_P10	GPIO	IN	√	√	
8	GPIO_P11	GPIO	IN	√	√	
9	GPIO_P14	GPIO	IN	√	√	ADC_CH2P_P14
10	GPIO_P15	GPIO	IN	√	√	ADC_CH3N_P15

#	QFN32	Default MODE	Default IN_OUT	IRQ	Wakeup	ANA_IO
12	GPIO_P17	XTALO(ANA)	ANA		√	
13	GPIO_P18	GPIO	IN	√	√	ADC_CH0P_P18
14	GPIO_P20	GPIO	IN	√	√	ADC_CH3P_P20
15	GPIO_P23	GPIO	IN	√	√	ADC_CH1P_P23
16	GPIO_P24	GPIO	IN	√	√	ADC_CH2N_P24
17	GPIO_P25	GPIO	IN	√	√	ADC_CH0N_P25
18	GPIO_P26	GPIO	IN	√	√	
19	GPIO_P27	GPIO	IN	√	√	
20	GPIO_P31	GPIO	IN	√	√	

Table 10: PHY6226 GPIO Application Notes

3.10.1 DC Characteristics

TA=25℃, VDD=3 V

PARAMETER	TEST CONDITIONS	Min.	TYP	Max.	Unit
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.4			V
Logic-0 input current	Input equals 0 V	-50		50	nA
Logic-1 input current	Input equals VDD	-50		50	nA
Logic-0 output voltage, 10-mA pins	Output load 10 mA			0.5	V
Logic-1 output voltage, 10-mA pins	Output load 10 mA	2.5			V

Table 11: DC Characteristics

4 Peripheral Blocks

4.1 2.4GHz Radio

The 2.4 GHz RF transceiver is designed to operate in the worldwide ISM frequency band at 2.4 to 2.4835 GHz. Radio modulation modes and configurable packet structure make the transceiver interoperable with Zigbee 3.0 protocol implementations.

- General modulation format
    - FSK (configurable modulation index) with configurable Gaussian Filter Shaping
    - OQPSK with half-sine shaping
    - On-air data rates
    - 250kbps
- Transmitter with programmable output power of -20dBm to +10dBm, in 3dB steps
- RSSI function (1 dB resolution, ± 2 dB accuracy)
- Receiver sensitivity
    - -103dBm@Zigbee 3.0 250Kbps data rate
- Embedded RF balun
- Integrated frac-N synthesizer with phase modulation

4.2 Timer/Counters (TIMER)

The implementation can include a 32-bit SysTick system timer, that extends the functionality of both the processor and the NVIC. When present, the NVIC part of the extension provides:

- A 32-bit system timer (SysTick)
- Additional configurable priority SysTick interrupt.

General purpose timers are included in the design. With the input clock running at 4Mhz.

4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24 bit COUNTER, 12 bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

4.4 AES-ECB Encryption (ECB)

The ECB encryption block supports 128 bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption.

4.5 Watchdog Timer (WDT)

A count down watchdog timer using the low-frequency clock source (LFCLK) offers configurable and

robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.

4.6 SPI (SPI0, SPI1 Two Independent Instances)

The SPI interface supports 3 serial synchronous protocols which are SPI, SSP and Microwire serial protocols. SPI wrapper contains one SPI master and one SPI slave. They are logically exclusive. Only one block is alive at a time. The operation mode for master mode and slave mode is controlled by PERI_MASTER_SELECT Register in COM block.

bit	Reset value	Definition
1	0	SPI1 is master mode when set
0	0	SPI0 is master mode when set

Table 12: PERI_MASTER_SELECT Register bit definition (base address = 0x4000_302C)

4.7 I2C (I2c0, I2c1 Two Independent Instances)

This I2C block support 100Khz, and 400Khz modes. It also supports 7-bit address and 10-bit address. It has built-in configurable spike suppression function for both lines.

4.8 UART (UART0, UART1 Two Independent Instances)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in HW up to 1Mbps baud. Parity checking and generation for the 9th data bit are supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pin out and enables efficient use of board space and signal routing.

4.9 DMIC/AMIC Data Path

The voice in interface supports one analog MIC (SAR-ADC) and two digital MIC (L+R), different output sample rate (64KHz, 32KHz, 16KHz and 8KHz), and different voice compress algorithm. For the Digital MIC, PDM signal is sampled at 1.28MHz(4x320KHz). L channel is sampled at raising edge, R channel is sampled at falling edge. For PCM-LOG and CVDS, output data rate is 64Kbps (8KHz x 8bit).

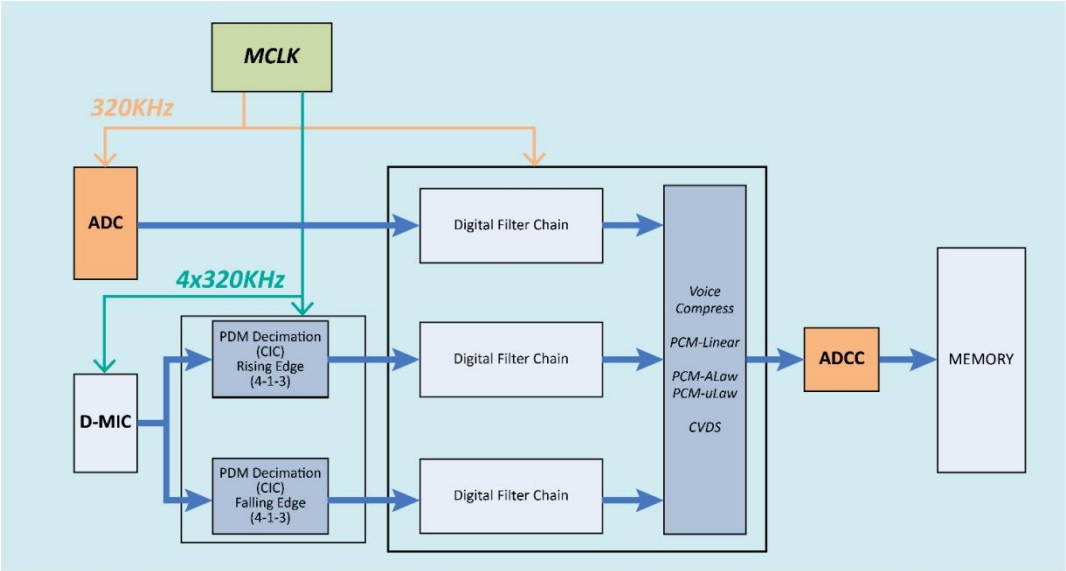


Figure 12: Block Diagram of Voice In Interface

Base address: 0x4005_0000

OFFSET	TYPE	RESET	NAME	DESCRIPTION
0x00			**ADCC voice enable**	
[31:1]	—	31'b0	reserved	
[0]	RW	1'b0	Enable	Setting this bit to “1” will enable voice core work
0x08			**ADCC reserved reg**	
[31:0]	—	32'b0	reserved	
0x0C			**ADCC voice control 1**	
[31:23]	—	9'd0	reserved	
[22:16]	RW	7'd40	gain_ctrl	Vocie Process Gain control,+-20dB, Step is 0.5dB. Voice_gain = (gain_ctrl-40)*0.5dB gain_ctrl with in[0 80]
[15:14]	—	2'd0	reserved	
[13:12]	RW	2'd2	encode_mode	Voice compress encode mode sel: 0:pcm a-law 1:pcm u-law 2:cvsd 3:bypass
[11:10]	—	2'd0	reserved	
[9:8]	RW	2'd0	voice_sel	Voice Process Output Rate Sel: 0:64Ksps 1:32Ksps 2:16Ksps 3:8Ksps
[7]	RW	1'b0	fir filter bandwidth	1:4K,0:8K
[6]	RW	1'b0	pcm_au_sel	pcm encode，1:a-law 0：u-law
[5]	RW	1'b0	lr_sel	
[4]	—	1'b0	reserved	
[3:2]	RW	2'd1	notch_bw	Dc Notch Filter BW

				0:bypass the DC Notch filter Other: one order high pass iir filter 1:a(n)+a(n-1)* (1-1/2^14) 2:a(n)+a(n-1)* (1-2/2^14) 3:a(n)+a(n-1)* (1-3/2^14)
[1]	RW	1'b0	plry_sel	Adc input polarity selection 0:voiceIn-2048 1:2048-voiceIn
[0]	RW	1'b0	mic_sel	DMIC and AMIC selection: 0:AMIC 1:DMIC
0x10			**ADCC voice control 2**	
[31]	—	1'd0	Reserved	
[30:20]	RW	11'd64	gain_max	Max Gain in auto mute process
[19:16]	—	4'd6	gain_maxbw	Max Gain BW in auto mute process
[15:14]	RW	2'd0	reserved	
[13:8]	RW	6'd9	amut_gdut	Auto mute adjust duration
[7:4]	RW	4'd0	amut_gst2	Auto mute gain increasingstep
[3:0]	RW	4'd1	amut_gst1	Auto mute gain increasingstep
0x14			**ADCC voice control 3**	
[31]	—	1'b0	Reserved	
[30:20]	RW	11'd55	amut_lvl2	Auto Mute Stop Level
[19]	—	1'b0	reserved	
[18:8]	RW	11'd10	amut_lvl1	Auto Mute Start Level
[7:1]	—	7'b0	reserved	
[0]	RW	1'b0	amut_byps	Bypass automate function
0x18			**ADCC voice control 4**	
[31:16]	—	16'd0	Reserved	
[15:8]	RW	8'd48	amut_alvl	Adaptive Mute Level control: 0: disable adaptive Mute level Other: Mute level1 = adpPower+amut_lvl1 Mute level2 = adpPower+amut_lvl2 adpPower is estimated over (amut_alv1<<amut_win1) samples
[7]	—	1'd0	reserved	
[6:4]	RW	3'd3	amut_beta	Voice Level Estimation filter bandwidth(one order low pss iir filter):
[3:0]	RW	4'd10	amut_winl	Voice Level estimation window length: samples = 1<<amut_winl

Table 13: ADCC Voice

4.9.1 Filter Chain Design

For D-MIC input, PDM Decimation (CIC) will convert the 1-bit PDM signal to 12 bit PCM signal. And the sample rate will be converted from 1.28MHz to 320KHz. The output data of the PDM Decimation

will be connected to the Digital Filter chain.

For the A-MIC input, SAR-ADC will convert the signal to 12bit 320KHz digital samples. The Digital Filter chain will process the data same as the D-MIC path.

The Output sample rate of the Digital filter chain is programmable. 64KHz, 32KHz, 16KHz, 8KHz. The maximum value of the sample's bit-width is 16bit.

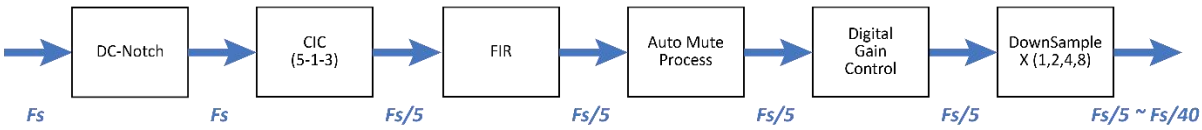


Figure 13: Digital Filter Chain

4.9.2 Auto Mute Process

Signal Level Estimate will check the input signal level with configurable window size. Mute threshold can be updated according to the signal level estimation or being configured by the register. There are two thresholds, one for MUTE_ON, another for MUTE_OFF. Gain step of MUTE_ON and MUTE_OFF can be configured individually.

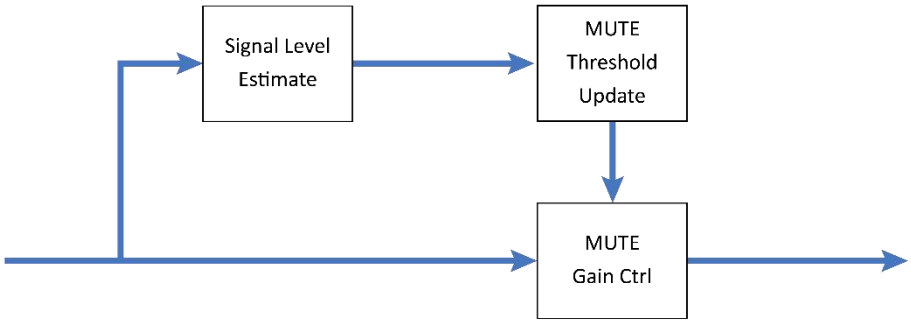


Figure 14: Auto Mute Process

4.9.3 Digital Gain Control

Digital gain is implemented by one Look up table. The gain error has been controled within 0.05dB.

4.9.4 Voice Compression

PCM-LOG support u-Law and a-Law. According to the ITU-G711 standard. The input data is 13~14bit @ 8KHz. The output data is 8bit @ 8KHz, 64Kbps. Also, it support 64Kbps CVSD according to the BT standard. Its Input is 16bit @64KHz, and its output is 1bit @ 64KHz. PCM-Linear is for the raw data without compression.

4.10 Pulse Width Modulation (PWM)

PHY62xx supports 6 channels of Pulse Width Modulation (PWM) outputs. PWM outputs generate

waveforms with variable duty cycle or pulse width programmed by registers. And each of the 6 PWM outputs can be individually programmed. Their duty cycles are controlled by programming individual counters associated with each channel.

The master clock is 16MHz. For each PWM outputs, first there is a prescaler (pre-divider) with division ratio of 2 to 128 (only 2^N division ratios are supported), followed by another 16bit counter with programmable max count, denoted as top_count. When the 16bit counter counts from 0 to top_count, it resets back to 0. So the frequency of the PWM is given by:

Freq_PWM = 16MHz / (N_prescaler * N_top_count);

A threshold counter number can be programmed, when the 16bit counter reaches the threshold, PWM output toggles. So the duty cycle is:

Duty_cycle_PWM = N_threshold/N_top_count;

The polarity of the PWM can also be programmed, which indicates output 1 or 0 when counter is below/above the threshold. A PWM waveform vs counter values are illustrated in the following **Figure 15**, where the polarity is positive. Also in this case the counter ramps up and then resets, we call it “up mode”.

There is also a “up and down mode”, where the counter ramps up to count_top and then ramps down, instead of reset.

As discussed above, the key register bits for one PWM channel are: 16bit top_count, 16bit threshold count, 3bit prescaler count, PWM polarity, PWM mode (up or up/down), PWM enable, and PWM load enable (load new settings). All 6 PWM channels can be individually programmed by registers with addresses from 0x4000_E004 to 0x4000_E044. In addition, one should enable registers 0x4000_E000<0><4> to allow all PWM channels can be programmed. For details please refer to documents of PHY62xx register tables.

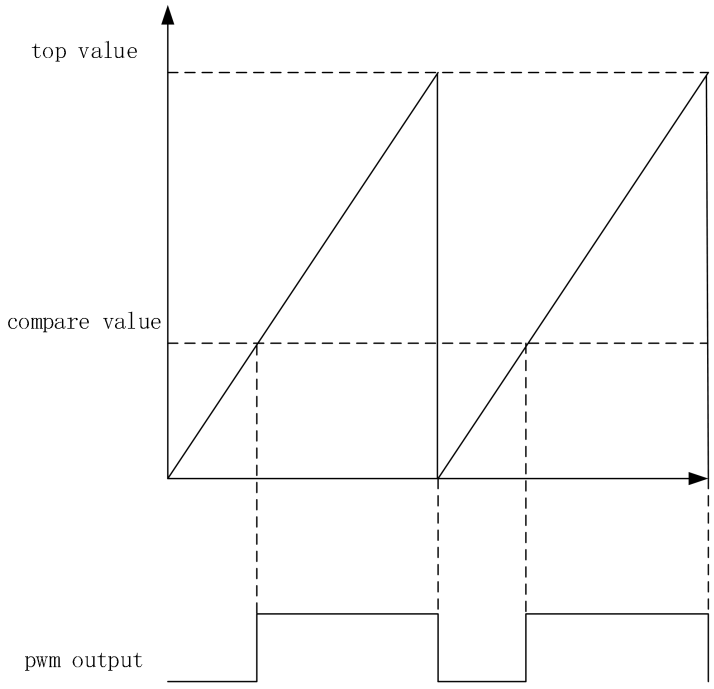


Figure 15: PWM operation

4.11 Quadrature Decoder (QDEC)

The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals with input debounce filters. It is suitable for mechanical and optical sensors. The sample period and accumulation are configurable to match application requirements. The quadrature decoder has three-axis capability and index channel support. It can be programmed as 4x/2x/1x count mode.

4.12 Key Scan (KSCAN)

Keyscan supports key matrix with upto 16 rows by 18 columns. Each individual rows or columns can be enabled or disabled through register settings. GPIO pins can be configured to be used for key scan. A few key scan Parameters can be set through registers, including polarity (low or high indicating key pressed); support multi-key-press or only single-key-press; de-bounce time (the time duration a key press is deemed valid) from 0 to 128mS with 255us step.

A valid key press can trigger an interrupt when keyscan interrupt is enabled. After a keyscan interrupt is serviced, writing 1 to the interrupt state register bit can clear the state bit.

The keyscan has a manual mode and an auto mode. For manual mode, when a keyscan interrupt is received, it is upo the MCU/software to scan the keyscan output pins and check the input pins, to determine which keys have been pressed. Manual mode is relatively slow and need CPU to process. On the contrary, in automode keyscan will automatically scan the output/input pins, and store the row/column info corresponding to the key pressed into read only registers, then trigger an interrupt for software to retrieve key press information.

4.13 Analog to Digital Converter (ADC) with Programmable Gain Amplifier (PGA)

The 12bit SAR ADC has total 10 inputs. Among them, there are two for PGA inputs, and two differential inputs for the on-chip temperature sensor. The other six inputs can be programmed to 4 pair differential inputs or six single-ended inputs. There is a manual mode with which the ADC can be configured to convert a specific input in single-ended or differential and with a specific ADC clock rate. There is also an auto sweep mode, namely all enabled input channels can be swept automatically in order by the ADC and the converted data will be stored at corresponding memory locations.

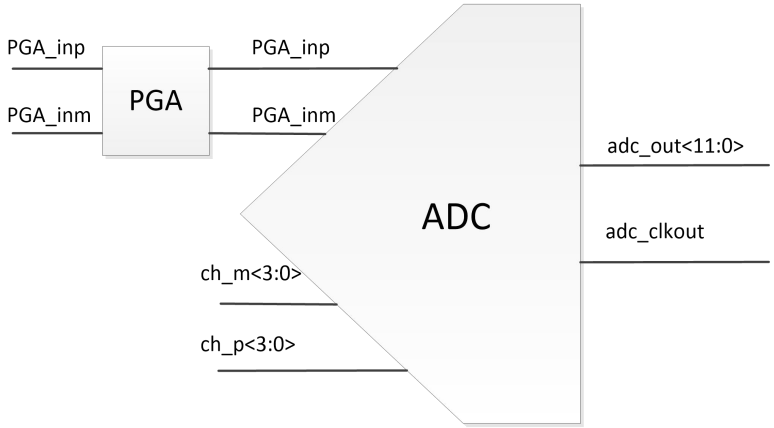


Figure 16: ADC

4.13.1 PGA Path

The PGA provides 42dB gain range from 0dB to 42dB in 3dB steps.

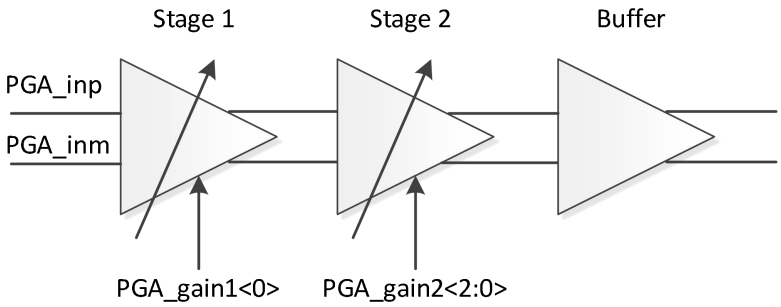


Figure 17: PGA path

pga_gain1<0>	Stage1 gain (v/v)	pga_gain2<2>	pga_gain2<1>	pga_gain2<0>	Stage2 gain (v/v)
0	5	0	0	0	37/4
1	15	0	0	1	36/5
		0	1	0	35/6
		0	1	1	34/7
		1	0	0	33/8
		1	0	1	32/9
		1	1	0	31/10
		1	1	1	30/11

Table 14: PGA gain

Set PGA_SEenable to “1”, PGA will be set to Single-ended mode by pulling the PGA into its Common-mode voltage.

4.13.2 ADC Path

By default the ADC is configured in manual mode. In this mode, the ADC clock rate can be configured to 80k/160k/320k sample per second. Select the pair of inputs and configure it to differential or singled-ended (positive or negative). By default it is differential. After enabling, the ADC will take samples with the configured clock rate and store the data to a channel dependent memory location. For each channel a memory size of 128Byte is allocated, when it is full an interrupt bit will be flagged. Each sample of 12bits takes 2 Byte memory space.

ADC can also be configured into auto channel sweep mode by setting the “adc_ctrl_override” bit to 0, with which the enabled channels will be sampled in the configured order automatically. The ten ADC input channels can be configured by programming their corresponding registers. Their configurations include sampling time, enable/disable, differential/single-ended, and continuous sampling/single-shot, based on the following register table. The sampled data is stored in the corresponding memory locations as in manual mode.

Base address: 0x4000_F000

0x6C	ADC_CTL0	Register Description
[31:16]	auto mode config temp sense, differntial inputs	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	auto mode config PGA inputs, differential inputs	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x70	**ADC_CTL1**	**Register Description**
[31:16]	auto mode config input A, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	auto mode config input A positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x74	**ADC_CTL2**	**Register Description**
[31:16]	auto mode config input B, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	auto mode config input B positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x78	**ADC_CTL3**	**Register Description**
[31:16]	auto mode config input C, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

[15:0]	auto mode config input C positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

Table 15: ADC channel configurations

4.13.3 ADC Channel <3:0> Connectivity

ADC	Hardwired	Single	differential	note
aio<0>	gpio<11>	√	Input B negative	
aio<1>	gpio<23>	√	Input B positive	micphone bias reference voltage
aio<2>	gpio<24>	√	Input C negative	
aio<3>	gpio<14>	√	Input C positive	
aio<4>	gpio<15>	√	Input D negative	micphone bias
aio<5>	gpio<16>			32K XTAL input
aio<6>	gpio<17>			32K XTAL output
aio<7>	gpio<18>		Input A positive	pga in+
aio<8>	gpio<25>		Input A negative	
aio<9>	gpio<20>	√	Input D positive	pga in-

Table 16: ADC channel connectivity

Aio<9:7,4:0>can be selected through an analog Mux by programming aio_pass<7:0> and aio_attn<7:0>. For example, register 0x4000_F020<8><0> set to 01, then Aio<0> is connected to ADC input B negative.

0x4000_F020		Register Description
[15 : 8]	Attenuation ctrl	attn[7:0]. analogIO control for {aio<9>, aio<8>,aio<7>,aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass through 10 attenuate to 1/4 11 NC

[7 : 0]	pass ctrl	pass[7:0]. analogIO control for {aio<9>, aio<8>,aio<7>,aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass through 10 attenuate to 1/4 11 NC note: analog IO sharing gpio<11>/aio<0> gpio<23>/aio<1>/micphone bias reference voltage gpio<24>/aio<2> gpio<14>/aio<3> gpio<15>/aio<4>/micphone bias gpio<16>/aio<5>/32K XTAL input gpio<17>/aio<6>/32K XTAL output gpio<18>/aio<7>/pga in+ gpio<25>/aio<8> gpio<20>/aio<9>/pga in-

Table 17: analog Mux

5 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which PHY6226 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the PHY6226. **Table 18** specifies the absolute maximum ratings for PHY6226.

Symbol	Parameter	Min.	Max.	Unit
Supply voltages				
VDD3		-0.3	+3.6	V
DEC			1.32	V
VSS			0	V
I/O pin voltage				
VIO		-0.3	VDD + 0.3	V
Environmental				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		3	
ESD HBM	Human Body Model Class 2		2	kV
ESD CDMQF	Charged Device Model (QFN32, 4x4 mm package)		500	V
Flash memory				
Endurance			100 000	write/erase cycles
Retention			10 years at 40 °C	
Number of times an address can be written between erase cycles			2	times

Table 18: Absolute maximum ratings

6 Operating Conditions

The operating conditions are the physical Parameters that PHY6226 can operate within as defined in **Table 19**.

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD3	Supply voltage, normal mode	1.8	3	3.6	V
tr_VDD	Supply rise time (0 V to 1.8 V)			100	ms
TA					
	Operating temperature (consumer)	-40	27	85	°C
	Operating temperature (Industrial)	-40	27	105	°C

Table 19: Operating conditions

7 Radio Transceiver

7.1 Radio Current Consumption

Parameter	Description	MIN	TYP	MAX	UNIT
Tx only at 0dBm	with internal DC-DC @3V		4.6		mA
Rx Only	with internal DC-DC @3V		4		mA

Table 20: Radio current consumption

7.2 Transmitter Specification

7.2.1 Zigbee 3.0 TX

Parameter	Description	MIN	TYP	MAX	UNIT
RF Max Output Power			10		dBm
RF Min Output Power			-20		dBm
Output power, highest setting	Delivered to a single-ended 50 Ω load through a balun		9		dBm
Error vector magnitude	At maximum output power		2%		
Spurious emission conducted measurement	f < 1 GHz, outside restricted bands		-43		dBm
	f < 1 GHz, restricted bands ETSI		-65		dBm
	f < 1 GHz, restricted bands FCC		-76		dBm
	f > 1 GHz, including harmonics		-46		dBm
	Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)				

Table 21: Zigbee 3.0 TX

7.3 Receiver Specification

7.3.1 Zigbee 3.0 RX

Parameter	Description	MIN	TYP	MAX	UNIT
Receiver sensitivity	PER = 1%		-103		dBm
Adjacent channel rejection	Wanted signal at -82dBm, modulated interferer at±5 MHz, PER = 1%		40		dB
Alternate channel rejection	Wanted signal at -82dBm, modulated interferer at±10 MHz, PER = 1%		53		dB
Channel rejection, ±15 MHz or more	Wanted signal at -82dBm, undesired signal is IEEE802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1%		59		dB
Blocking/desensitization,5 MHz from upper band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		66		dB

Parameter	Description	MIN	TYP	MAX	UNIT
Blocking/desensitization,10 MHz from upper band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Blocking/desensitization,20 MHz from upper band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		66		dB
Blocking/desensitization,50 MHz from upper band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		70		dB
Blocking/desensitization,-5 MHz from lower band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		64		dB
Blocking/desensitization,-10 MHz from lower band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Blocking/desensitization,-20 MHz from lower band edge	Wanted signal at -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		67		dB
Blocking/desensitization,-50 MHz from lower band edge	Wanted signalat -97dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		68		dB
Spurious emissions, 30 to 1000 MHz	Conducted measurement in a 50 Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		>200		dBm
Spurious emissions, 1 to 12.75 GHz	Conducted measurement in a 50 Ω single-ended load. Suitable for systems targeting compliance with –62 dBm GHz EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		100		dBm
Frequency error tolerance	Difference between center frequency of the received RF signal and local oscillator frequency		+-1		ppm
RSSI dynamic range			40		dB
RSSI accuracy			53		dB

Table 22: Zigbee 3.0 RX

7.4 RSSI Specifications

Parameter	Description	MIN	TYP	MAX	UNIT
RSSI Dynamic Range			70		dB
RSSI Accuracy	RSSI Accuracy Valid in range -100 to -30dBm		+/-2		dB
RSSI Resolution	Totally 7bit, from 0 to 127		1		dB
RSSI Period			8		us

Table 23: RSSI specifications

8 Glossary

Term	Description
AHB	Advanced High-performance Bus
AHB-AP	DAP AHB Port for debug component access thru AHB bus
AMBA	Advanced Microcontroller Bus Architecture
AON	Always-on power domain
APB	Advanced Peripheral Bus
APB-AP	DAP APB Port for debug component access thru APB bus
BROM	Boot ROM
DAP	Debug Access Port
ETM	Embedded trace module
FPU	Floating Point Unit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound, Integrated Interchip Sound
ITM	Instrumentation Trace Macrocell Unit
JTAG	Joint Test Access Group (IEEE standard)
JTAG-AP	DAP's JTAG Access Port to access debug components
JTAG-DP	DAP's JTAG Debug Port used by external debugger
J&M	Jun and Marty LLC
MPU	Memory Protection Unit
NVIC	Nested vector Interrupt Controller
PCR	Power Clock Reset controller
POR	Power on reset, it is active low in this document
RFIF	APB peripheral to interface RF block
SWD	Serial Wire DAP
SoC	System on chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access memory
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver and Transmitter
WDT	Watchdog Timer

Table 24: Glossary

9 Ordering information

9.1 Chip Marking Example

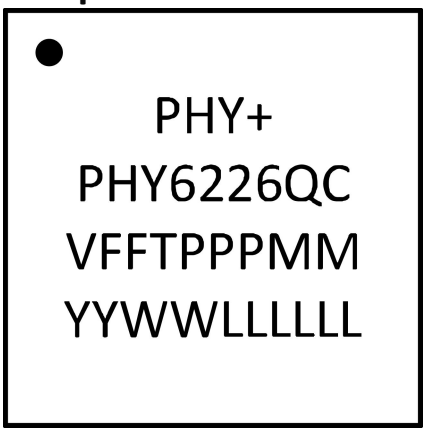


Figure 18: Chip Marking Example

9.2 Chip Marking Rule

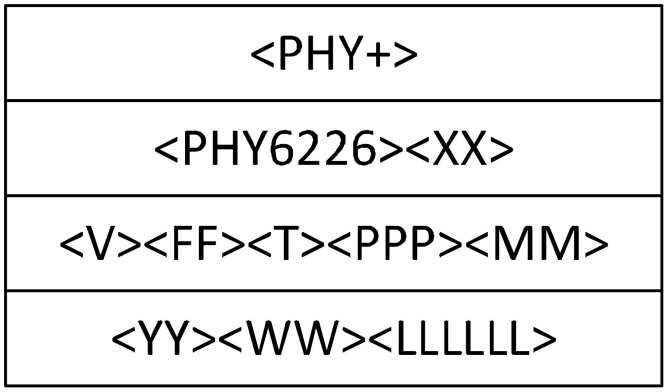
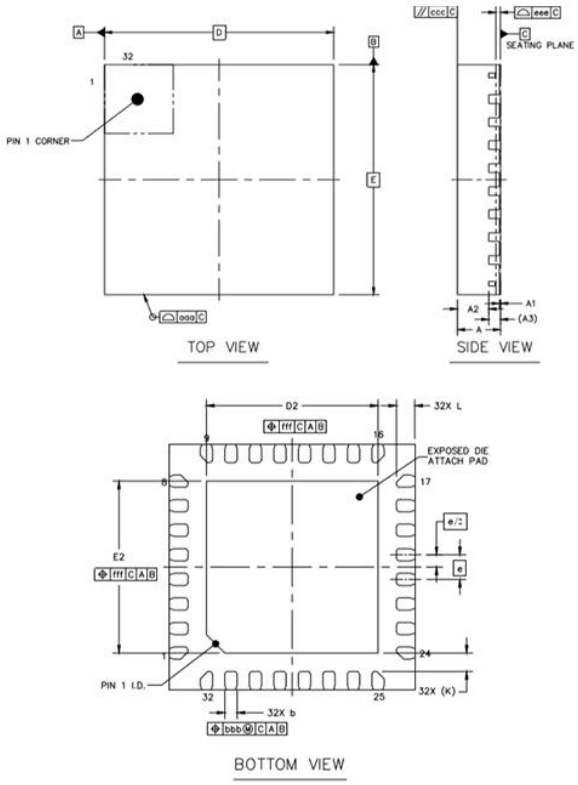


Figure 19: Chip Marking Rule

Abbreviation	Definition and Implemented Codes
<PHY+>	PHYPLUS MICROELECTRONIC
<PHY6226>	PHY6226 Product
<XX>	Package Type
<V>	Supply Voltage
<FF>	Flash Size
<T>	Operating Temperature
<PPP>	Product Information
<MM>	Manufacturer Information
<YY>	2-digital Year Code
<WW>	2-digital Week Code
<LLLLLL>	6-digital Wafer Lot Code

Table 25: Chip Marking Rule

10 Package dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	2.7	2.8	2.9
	Y	E2	2.7	2.8	2.9
LEAD LENGTH		L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

Figure 20: QFN32 package dimensions

Note: dimensions are in mm, angels are in degree.

11 Sample Application and Layout Guide

11.1 Sample Application (QFN32)

11.1.1 With DCDC

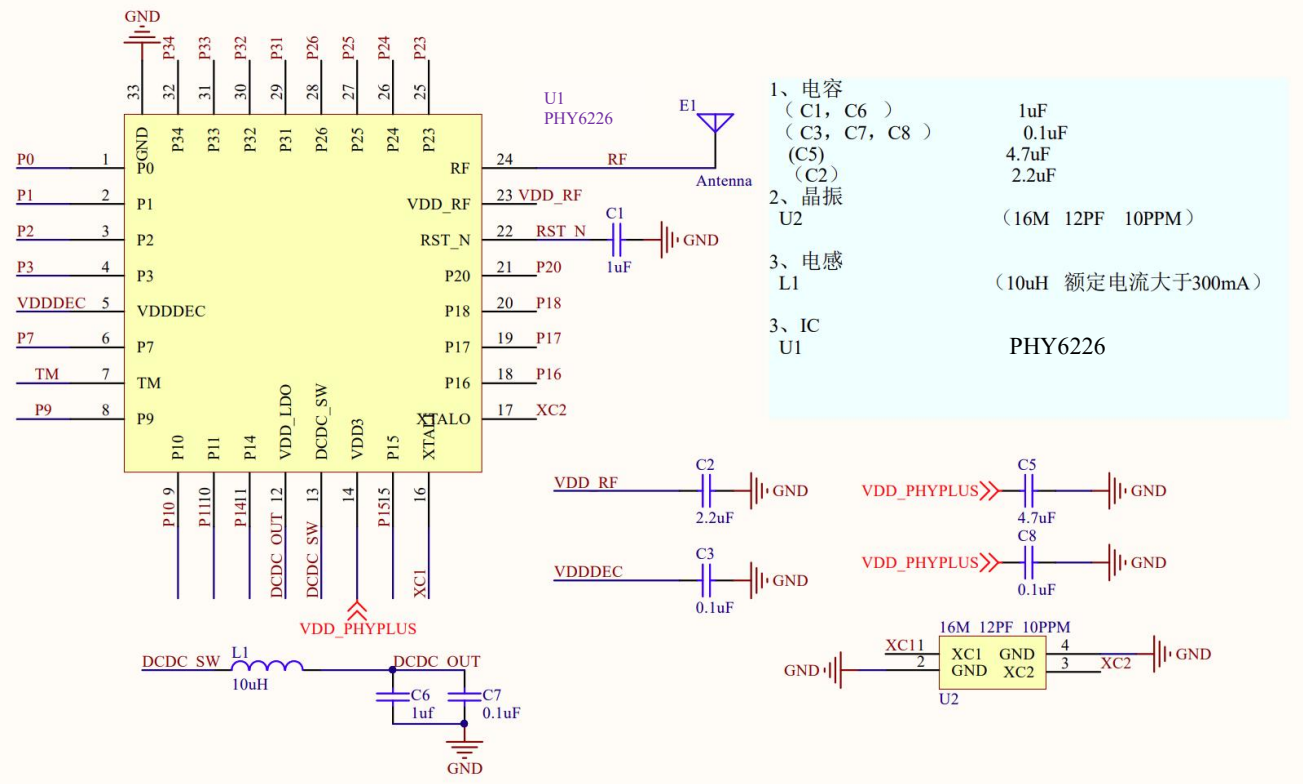


Figure 21: Sample application of QFN32 with DCDC

* If RF TX output power > 5dBm, C2=4.7uF

11.1.2 Without DCDC

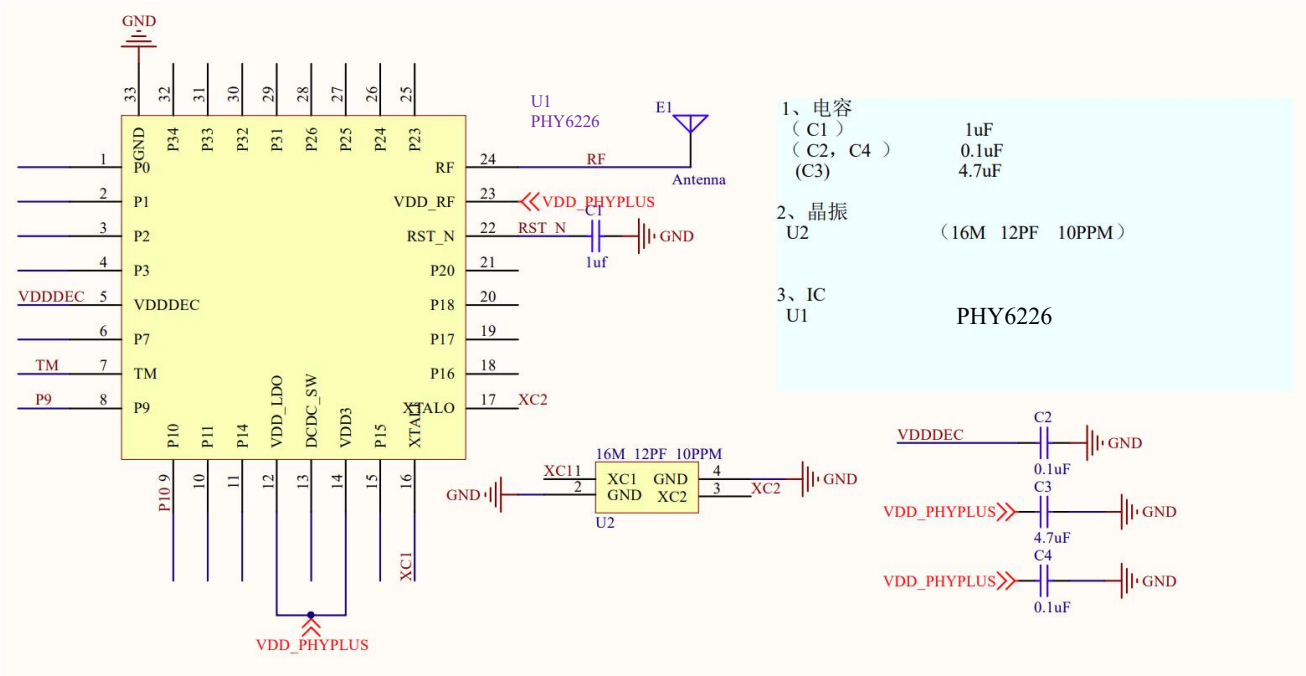


Figure 22: Sample application of QFN32 without DCDC

11.2 Layout Guide

11.2.1 Placement

1. RF matching/Loop filter leading to antenna should be isolated from any other AC/DC signal as much as possible;
2. Xtal/OSC clock is a noise source to other circuits, keep clock trace as short as possible and away from any important area;
3. LDO's are sensitive and could be easily contaminated, care should be taken for the environment;
4. Antenna is the main RF radiation point, other important blocks should be shielded or away from this area.

RF traces

1. Define RF line width with given dielectric thickness (thickness of PCB dielectric layer to ground plain) to achieve 50ohm impedance; this is mainly for the RF line connecting to matching/loop filter and antenna.
2. Differential traces should be kept in the same length and component should be placed symmetrically;
3. Certain length of RF trace should be treated as part of RF matching.

11.2.2 Bypass Capacitor

1. Each VDD pin needs a bypass capacitor to release chip internal noise and block noise from power supply.
2. For power traces, bypass capacitors should be placed as close as possible to VDD pins.
3. Use one large and one small capacitor when the pin needs two capacitors. Typically the capacitance of the larger capacitor is about 100 times of that of the smaller one. The smaller capacitor usually has better quality factor than the larger one. Place the larger capacitor closer to

the pin.

4. The capacitors of Loop filter need to have larger clearance to prevent EMC/EMI issue.
5. Ground via should be close to the Capacitor GND side, and away from strong signals.

11.2.3 Layer Definition

1. Normally 4 layer PCB is recommended.
2. RF trace must be on the surface layer, i.e. top layer or bottom.
3. The second layer of RF PCB must be “Ground ” layer , for both signal ground and RF reference ground , DO NOT put any other trace or plane on second layer, otherwise “antenna effect” will complicate debug process.
4. Power plane generally is on the 3rd layer.
5. Bottom layer is for “signal ” layer.
6. If two layer PCB is used, quality will degrade in general. More care needs to be taken. Try to maximize ground plane, avoid crossing of signal trace with other noise lines or VDD, shield critical signal line with ground plane, maximize bypass capacitor and number of ground vias.

11.2.4 Reference clock and trace

1. Oscillator signal trace is recommended to be on the 1st layer;
2. DO NOT have any trace around or across the reference clock (oscillator) trace.
3. Isolate the reference clock trace and oscillator by having more GND via around.
4. DO NOT have any other traces under the Oscillator.

11.2.5 Power line or plane

1. Whether to use power plain or power line depend on the required current, noise and layout condition. For RF chip, we generally suggest to use power line to bring power into IC pin. Line has parasitic inductance, which forms a low pass filter to reduce the noise traveling around PCB.
2. Add more conductive via on the current source, it will increase max current limit and reduce inductance of via.
3. Add some capacitor alone the power trace when power line travels a long distance.
4. DO NOT place power line or any plane under RF trace or oscillator and its clock trace , the strong clock or RF signal would travel with power line.

11.2.6 Ground Via

1. Ground Via must be as close to the ground pad of bypass capacitor as possible , too much distance between via and ground pad will reduce the effect of bypass capacitor.
2. Having as many ground via as possible.
3. Place ground via around RF trace, the RF trace should be shielded with via trail.