PHY6230

Bluetooth Low Energy (BLE)/ Proprietary 2.4GHz System on Chip

Key Features

- 32-bit Processor (Max 64MHz) with SWD
- Memory
  - 64KB ROM
  - 8KB Retention SRAM
  - 16KB OTP
  - EEPROM (optional)
- 19/11/3 General Purpose I/O Pins
  - Configurable as serial interface and programmable IO MUX function mapping
  - All pins can be configured for wake-up
  - All pins for triggering interrupt
  - 3 Quadrature Decoder (QDEC)
  - 6-channel PWM
  - 1-channel I2C
  - 1-channel SPI Master
  - UART
  - SWD
  - USB 2.0
- 10-channel 12-bit ADC
- 4-channel 32-bit Timer, 1 Watchdog Timer
- Real Timer Counter (RTC)
- Power, Clock, Reset Controller
- Flexible Power management
  - Operating voltage range 1.8V to 5.0V
  - Support lithium battery charging
  - Embedded LDOs
  - Battery monitor: support low battery detection
- Power Consumption
  - 0.7uA@OFF Mode (IO wake up only)
  - 2uA@Sleep Mode with 32KHz RTC
  - Receive Mode: 10mA@3.3V Power Supply
  - Transmit Mode: 10mA (0dBm output power) @3.3V Power Supply
- RC Oscillator Hardware Calibrations
  - 32KHz RC osc for RTC with +/-200ppm accuracy
  - 32MHz RC osc for HCLK with 3% accuracy
- BLE
  - Bluetooth SIG 5.2
  - Support Master & Slave
- 2.4 GHz Transceiver
  - Support BLE 5.0 RF PHY 1Mbps/2Mbps
  - Proprietary 500K Protocol Stack
  - FSK with configurable Gaussian filter (configurable modulation index)
  - Sensitivity:
    -96dBm@BLE 1Mbps data rate
    -93dBm@BLE 2Mbps data rate
  - Tx power -20 to +10dBm in 3dB steps
  - Single-pin antenna: no RF matching or Rx/Tx switching required
  - RSSI (1dB resolution)
- AES-128 Encryption Hardware
- Operating Temperature: -40˚C ~+125 ˚C
- RoHS Package: SSOP24/SOP16/TSSOP8

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1 Introduction

PHY6230 is a System on Chip (SoC) for Bluetooth® low energy and proprietary 2.4G applications. It has high-performance low-power 32-bit processer with 8KB retention SRAM, 64KB ROM, 16KB OTP, and an ultra-low power, high performance, multi-mode radio. Also, PHY6230 can support BLE with security and application. Serial peripheral IO and integrated application IP enables customer product to be built with minimum bill-of-material (BOM) cost.

2 Product Overview

2.1 Block Diagram

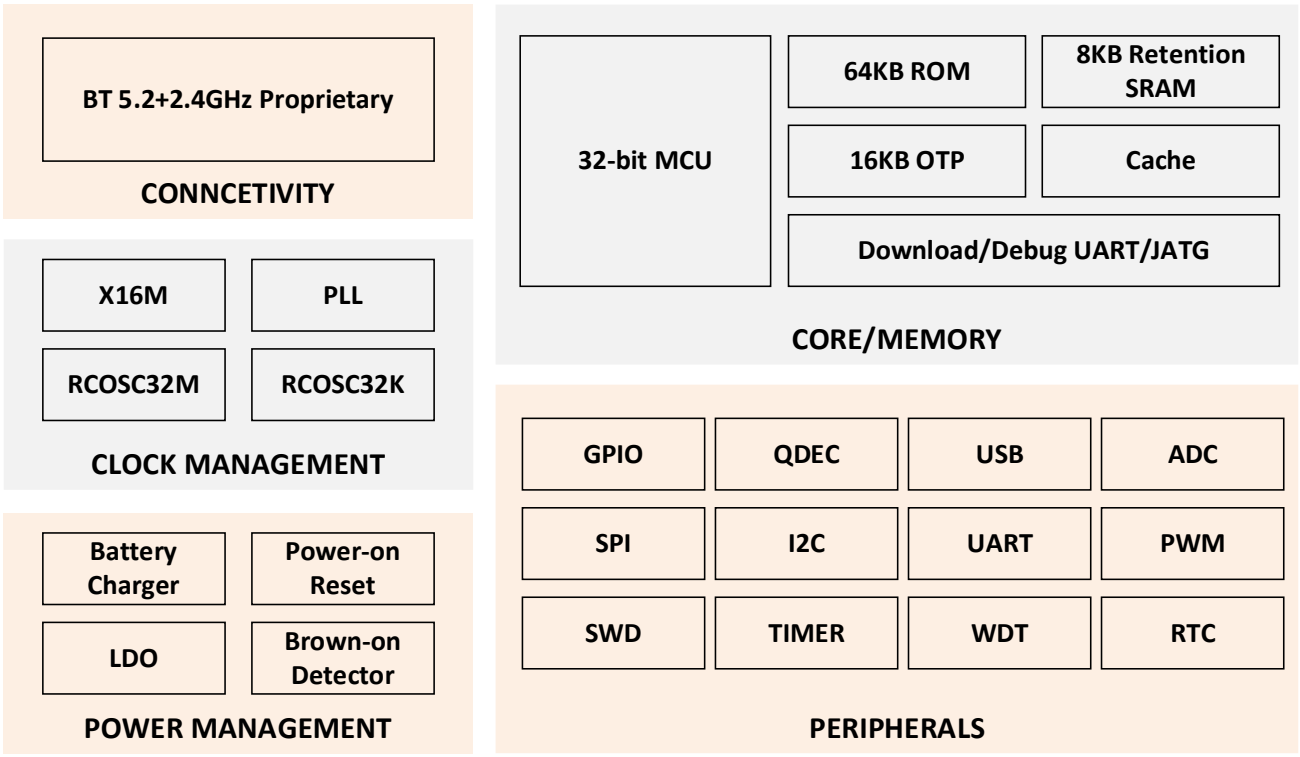


Figure 1: PHY6230 Block Diagram

2.2 Pin Assignments and Functions

This section describes the pin assignment and the pin functions for the package types of SSOP24, SOP16 and TSSOP8.

2.2.1 PHY6230 (SSOP24)

2.2.1.1 Pin Assignment

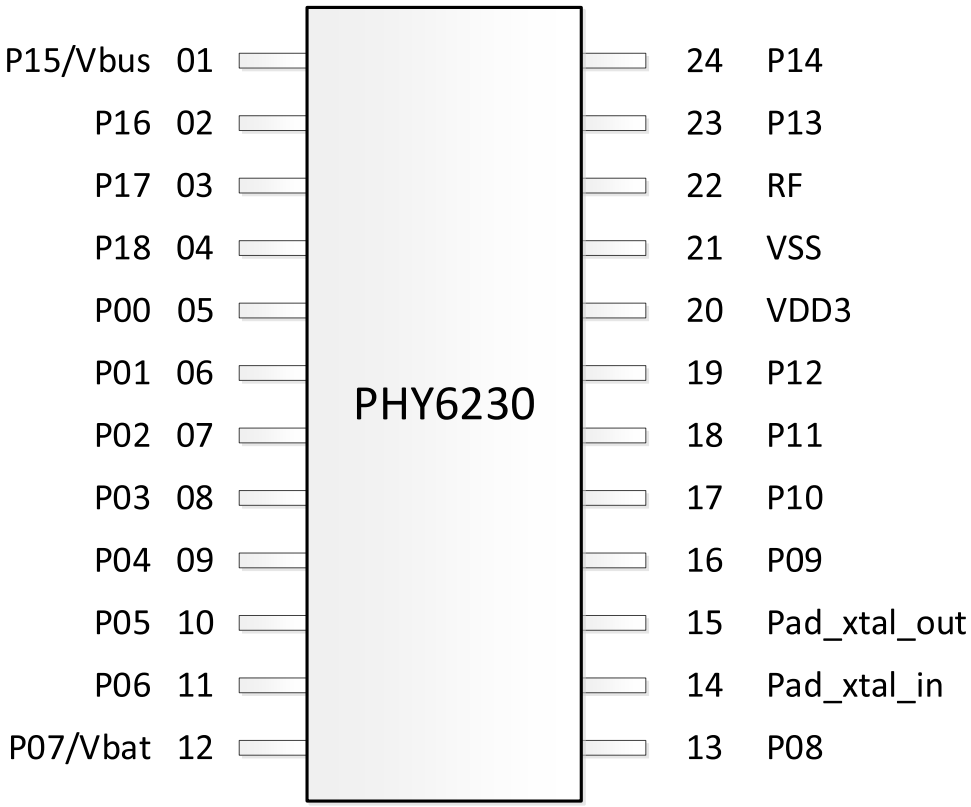


Figure 2: Pin assignment – PHY6230 SSOP24 package

2.2.1.2 Pin Functions

Pin	Pin name	Description
1	P15/Vbus	GPIO 15/Vbus
2	P16	GPIO 16
3	P17	GPIO 17
4	P18	GPIO 18
5	P00	GPIO 00/USBDP
6	P01	GPIO 01/USBDM
7	P02/SWD_IO	GPIO 02/SWD debug data inout
8	P03/SWD_CLK	GPIO 07/SWD debug clock
9	P04	GPIO 04/ADC input 0
10	P05	GPIO 05/ADC input 1
11	P06	GPIO 06/ADC input 2/USBDP
12	P07/Vbat	GPIO 07/Vbat/ADC input 3/USBDM

Pin	Pin name	Description
13	P08	GPIO 08/ADC input4
14	Pad_xtal_in	16MHz crystal output
15	Pad_xtal_out	16MHz crystal input
16	P09	GPIO 09/ADC input 5/UART_Tx
17	P10	GPIO 10/ADC input 6/UART_Rx
18	P11	GPIO 11/ADC input 7
19	P12	GPIO 12
20	VDD3	3.3V power supply
21	VSS	GND
22	RF	RF antenna
23	P13	GPIO 13
24	P14	GPIO 14

Table 1: Pin functions of PHY6230 SSOP24 package

2.2.2 PHY6230 (SOP16)

2.2.2.1 Pin Assignment

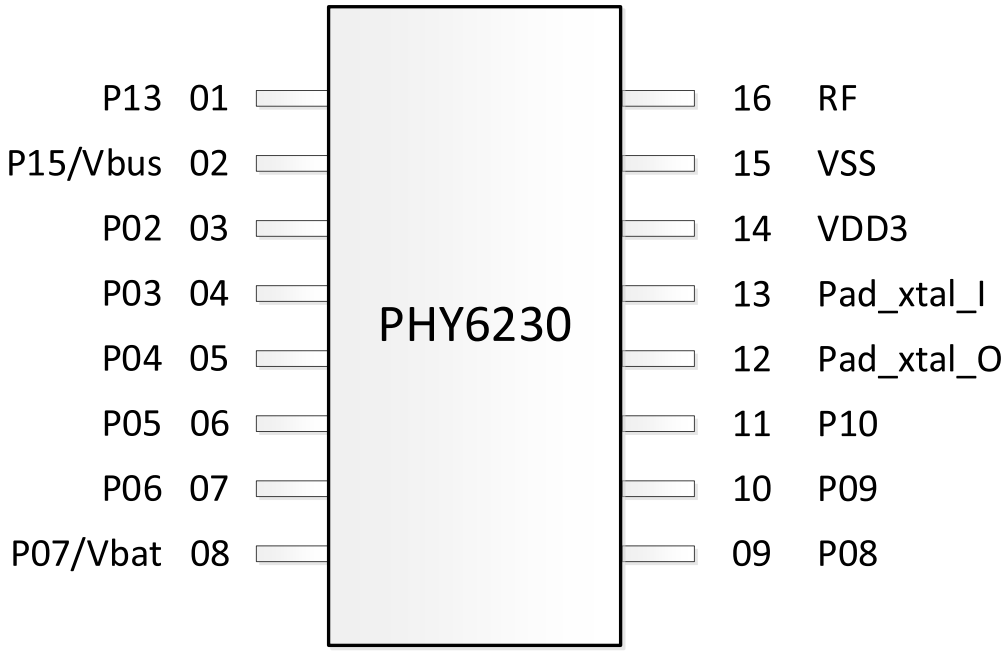


Figure 3: Pin assignment – PHY6230 SOP16 package

2.2.2.2 Pin Functions

Pin	Pin name	Description
1	P13	GPIO 13
2	P15/Vbus	GPIO 2/SWD debug data inout GPIO 15/Vbus
3	P02/SWD_IO	GPIO 02/SWD debug data inout
4	P03/SWD_CLK	GPIO 07/SWD debug clock
5	P04	GPIO 04/ADC input 0
6	P05	GPIO 05/ADC input 1

Pin	Pin name	Description
7	P06	GPIO 06/ADC input 3/USBDP
8	P07/Vbat	GPIO 07/Vbat/USBDM
9	P08	GPIO 08/ADC input 4
10	P09	GPIO 09/ADC input 5/UART_Tx
11	P10	GPIO 10/ADC input 5/UART_Rx
12	Pad_xtal_out	16MHz crystal output
13	Pad_xtal_in	16MHz crystal input
14	VDD3	3.3V power supply
15	VSS	GND
16	RF	RF antenna

Table 2: Pin functions of PHY6230 SOP16 package

2.2.3 PHY6230 (TSSOP8)

2.2.3.1 Pin Assignment

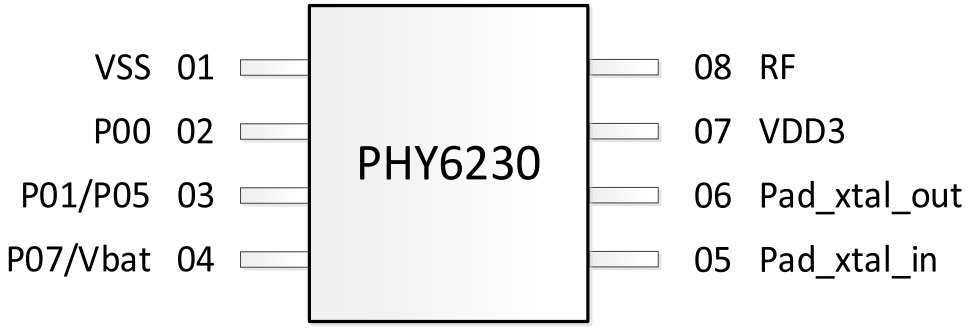


Figure 4: Pin assignment – PHY6230 TSSOP8 package

2.2.3.2 Pin Functions

Pin	Pin name	Description
1	VSS	GND
2	P00	GPIO 00/USBDP
3	P01/P05	GPIO 01/GPIO 05 /USBDM
4	P07/Vbat	GPIO 07/Vbat/ADC input 3//USBDM
5	Pad_xtal_in	16MHz crystal input
6	Pad_xtal_out	16MHz crystal output
7	VDD3	3.3V power supply
8	RF	RF antenna

Table 3: Pin functions of PHY6230 TSSOP8 package

3 System Block

The system block diagram of PHY6230 is shown in **Figure 1**.

3.1 CPU

The PHY6230 has a high-performance low-power 32-bit CPU and 512-byte Cache. The CPU, memories, and all peripherals are connected by AMBA bus matrix.

The CPU will play controller role in BLE modem and run all user applications.

3.2 Memory

PHY6230 has total 64KB ROM, 8KB SRAM and 16KB OTP. The physical address space of these memories is shown in **Figure 5**.

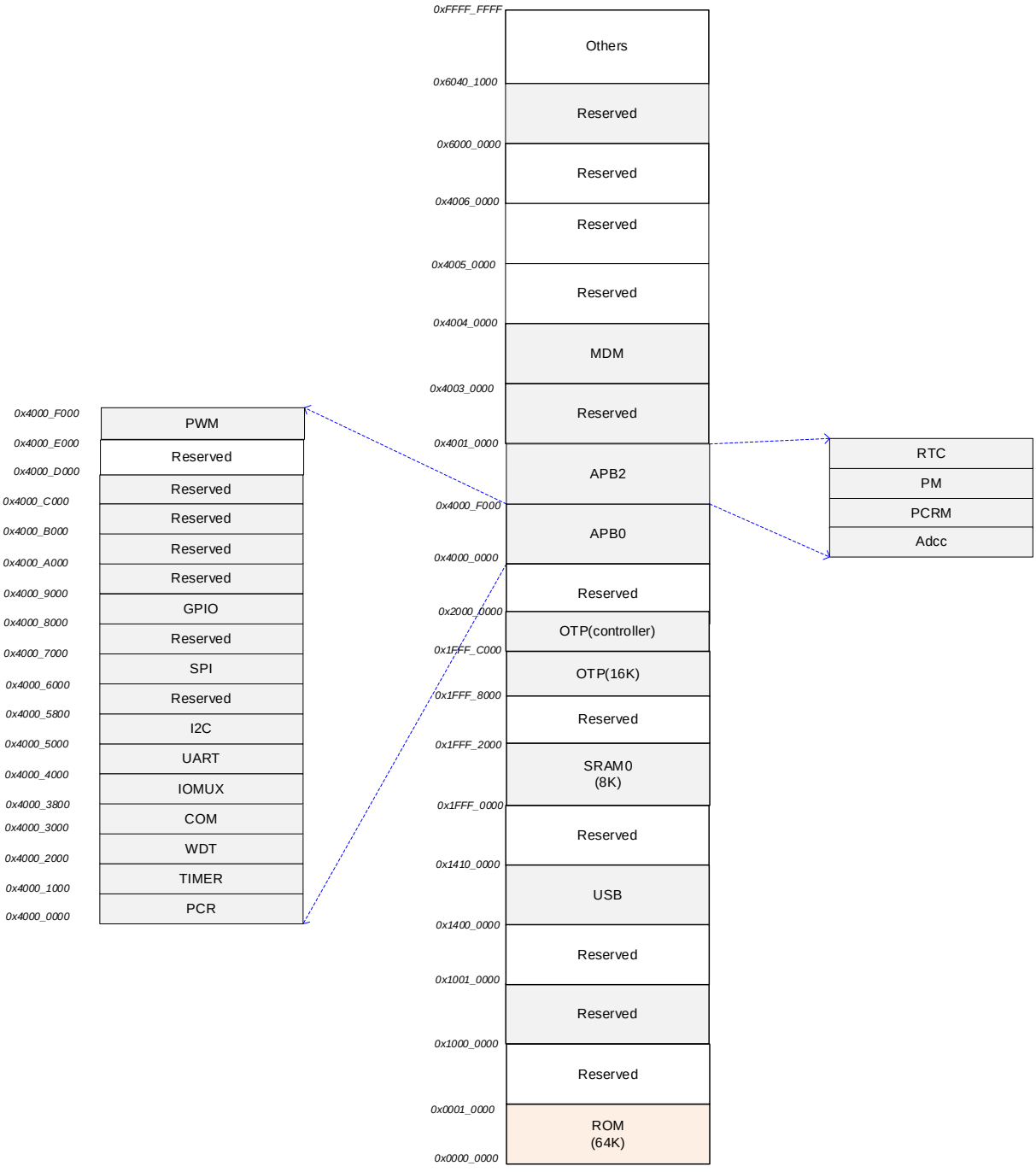


Figure 5: PHY6230 Memory Space

3.2.1 ROM

PHY6230 has 1 ROM.

	SIZE	CONTENT
ROM	64KB	Boot ROM. Protocol stack. Common peripheral drivers. ATE AT command.

Table 4: List of ROM

3.2.2 SRAM

PHY6230 has 1 SRAM blocks. The SRAM block have retention capability, which can be configured individually. Normal operating voltage is 1.2V, and the voltage is adjustable at retention. The SRAM block can be used to store program or data.

	SIZE	CONTENT
SRAM0	8KB	

Table 5: List of SRAM

3.2.3 OTP

The OTP is an antifuse based technology, which is capable for security code storage. This IP programming voltage is generated from an internal charge pump. The main memory is organized as 4,096 by 32 bits. The OTP cell design will provide a low cost logic process OTP approach compared with alternative approaches. The OTP is programmed by 1.2V, 3.3V power supply.

3.2.4 Memory Address Mapping

Name	Size （KB）	Master	Physical Address
ROM	64K	MCU	0000_0000~0000_FFFF
SRAM	8K	MCU	1FFF_0000~1FFF_1FFF
OTP	16K	MCU	1FFF_8000~1FFF_BFFF
RAM_BB	1K	MCU	

Table 6: Memory address mapping

3.3 Boot and Execution Modes

Only in CP Chip form, the chip enters CP boot mode after power on. ROM1 is then aliased to the 0x0 address and the chip program starts from ROM1.

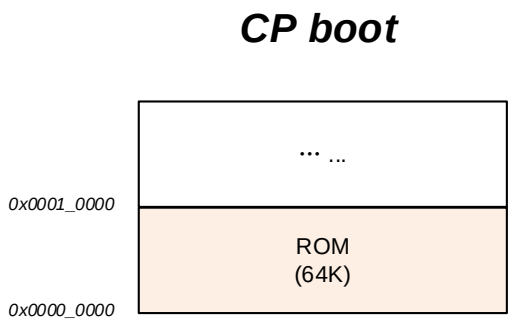


Figure 6: PHY6230 boot mode

3.4 Power, Clock and Reset (PCR)

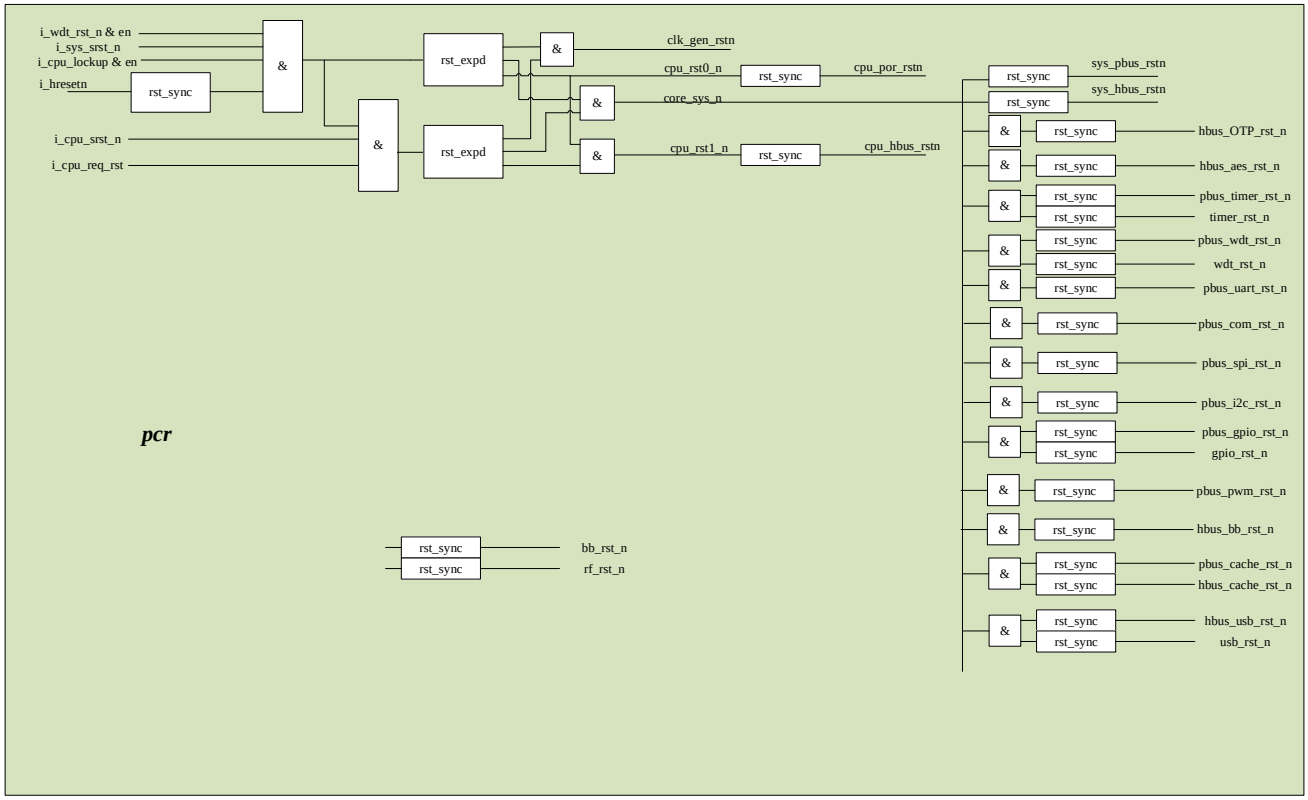


Figure 7: PHY6230 power, clock and reset

3.5 Power Management (POWER)

The power management system is highly flexible with functional blocks such as the CPU, radio transceiver, and peripherals saving separate power state control in addition to the System Sleep mode and OFF modes. When in System Normal mode, all functional blocks will independently be turned on depending on needed application functionality.

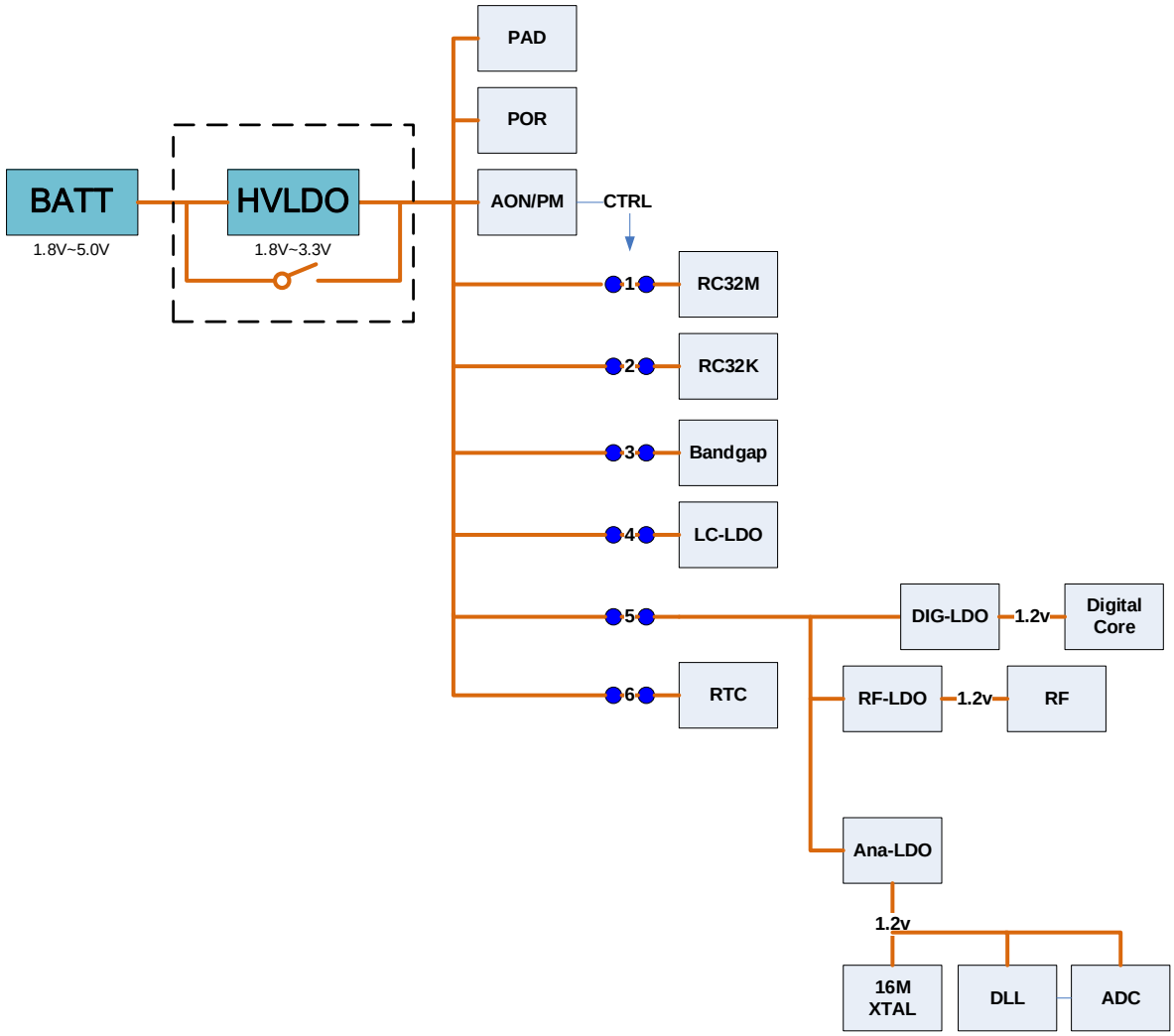


Figure 8: Power system

The following diagram is Normal, Sleep and Off mode. Switches are optional depending on user's request.

#	Switch	Normal	Sleep	Off
1	RC32M	On	Off	Off
2	RC32K	On	Optional	Off
3	bandgap	On	Off	Off
4	LC-LDO	On	on	Off
5	DIG-LDO	On	Off	Off
6	RTC	On	Optional	Off

Table 7: Switches of different power modes

3.6 Low Power Features

3.6.1 Operation and Sleep States

3.6.1.1 Normal State

3.6.1.2 Clock Gate State

The CPU executes WFI/WFE to enter clock gate state. After wake-up from clock-gate state, the CPU continues to execute the program from where it stopped. The wake-up sources includes interrupts and events. The wake-up sources are configured by the software according to applications.

3.6.1.3 System Sleep State

The wake-up sources include:

- IO
- RTC
- RESET
- UVLO reset

3.6.1.4 System Off State

The wake-up sources include:

- IOs
- RESET
- UVLO reset

3.6.1.5 UVLO

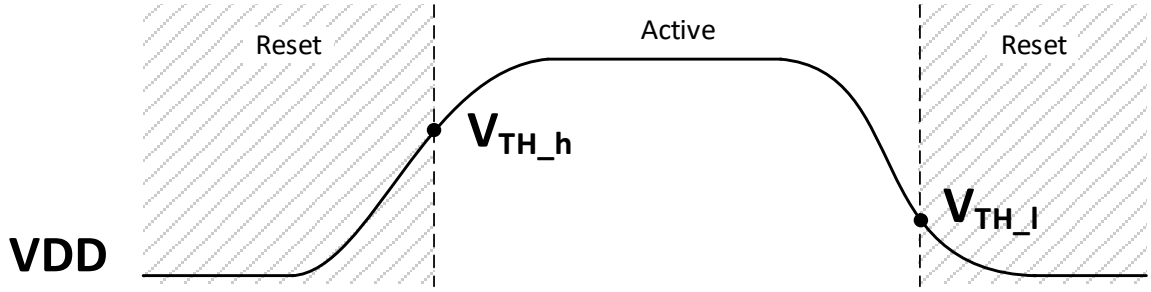


Figure 9: UVLO reset

VDD > VTH_h, release reset; VDD < VTH_l, enter reset.

VDD	Min.	TYP	Max.	Unit
V_{TH_h}	1.7	1.74	1.78	V
V_{TH_l}	1.63	1.66	1.69	V

Table 8: UVLO

If power supply VDD rises more than 0.6V within 100us, power monitor will trigger a whole chip reset event.

3.6.2 State Transition

3.6.2.1 Entering Clock Gate State and Wake-up

CPU executes WFI/WFE.

3.6.2.2 Entering Sleep/off States and Wake-up

The PM registers identify whether the CPU is in mirror mode or FLASH mode before sleep or off, and record the remap and vectors. The CPU configures the corresponding PM registers to put the chip into sleep mode. After wake-up, the chip enters boot mode to execute boot code in the ROM. The ROM code checks the mode before sleep/off and the remap information, perform corresponding configurations, and starts to execute the program.

3.7 Interrupts

Interrupt Name	MCU Interrupt Number
	0
	1
	2
otp_irq	3
bb_irq	4
	5
	6
	7
	8
	9
wdt_irq	10
uart_irq	11
i2c_irq	12
	13
spi_irq	14
	15
gpio_irq	16
Xtal_irq	17
Dll_irq	18
	19
timer_irq[1]	20
timer_irq[2]	21
timer_irq[3]	22
timer_irq[4]	23
	24
	25
otgtop_irq	26
otgtop_rf_irq	27
aes_irq	28
adcc_irq	29
	30
Hclk_mux_done	31

Table 9: Interrupts

3.8 Clock Management

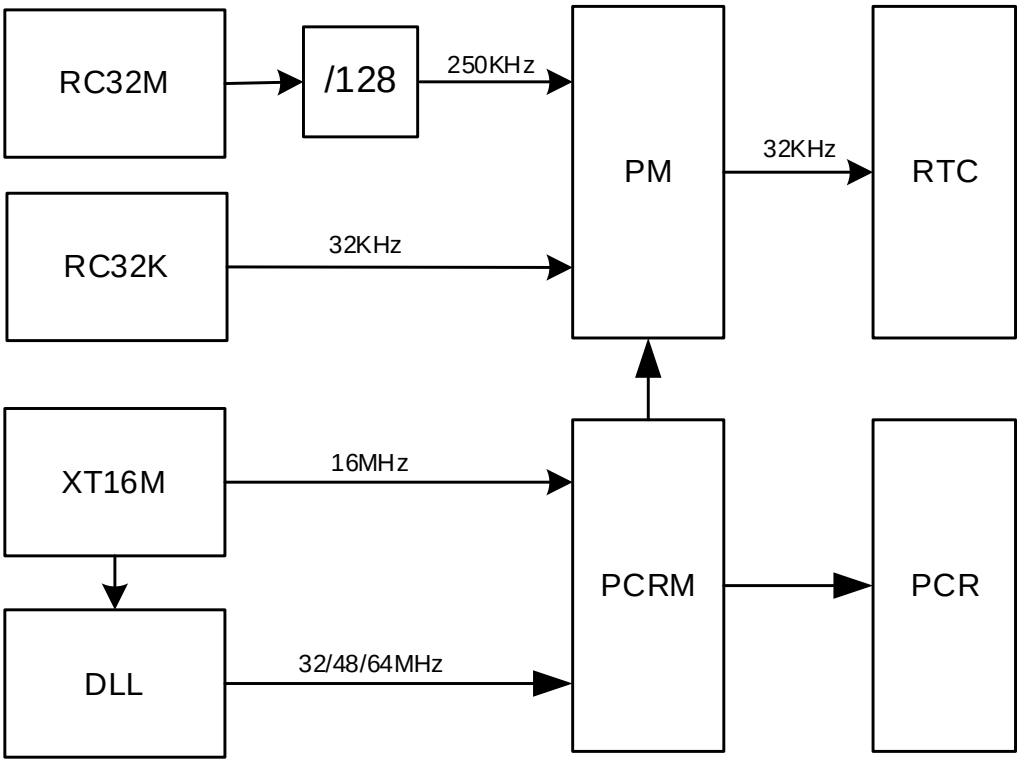


Figure 10: Clock management

There is only one crystal clock sources: 16MHz crystal oscillator (XT16M). There are also two on chip RC oscillators: 32MHz RC oscillator (RC32M) and 32kHz RC oscillator (RC32k), both of which can be calibrated with respect to 16MHz crystal oscillator. At initial power up or wake up before XT16M oscillator starts up, RC32M is used as the main clock. An on-chip DLL generates higher frequency clocks such as 32/48/64MHz.

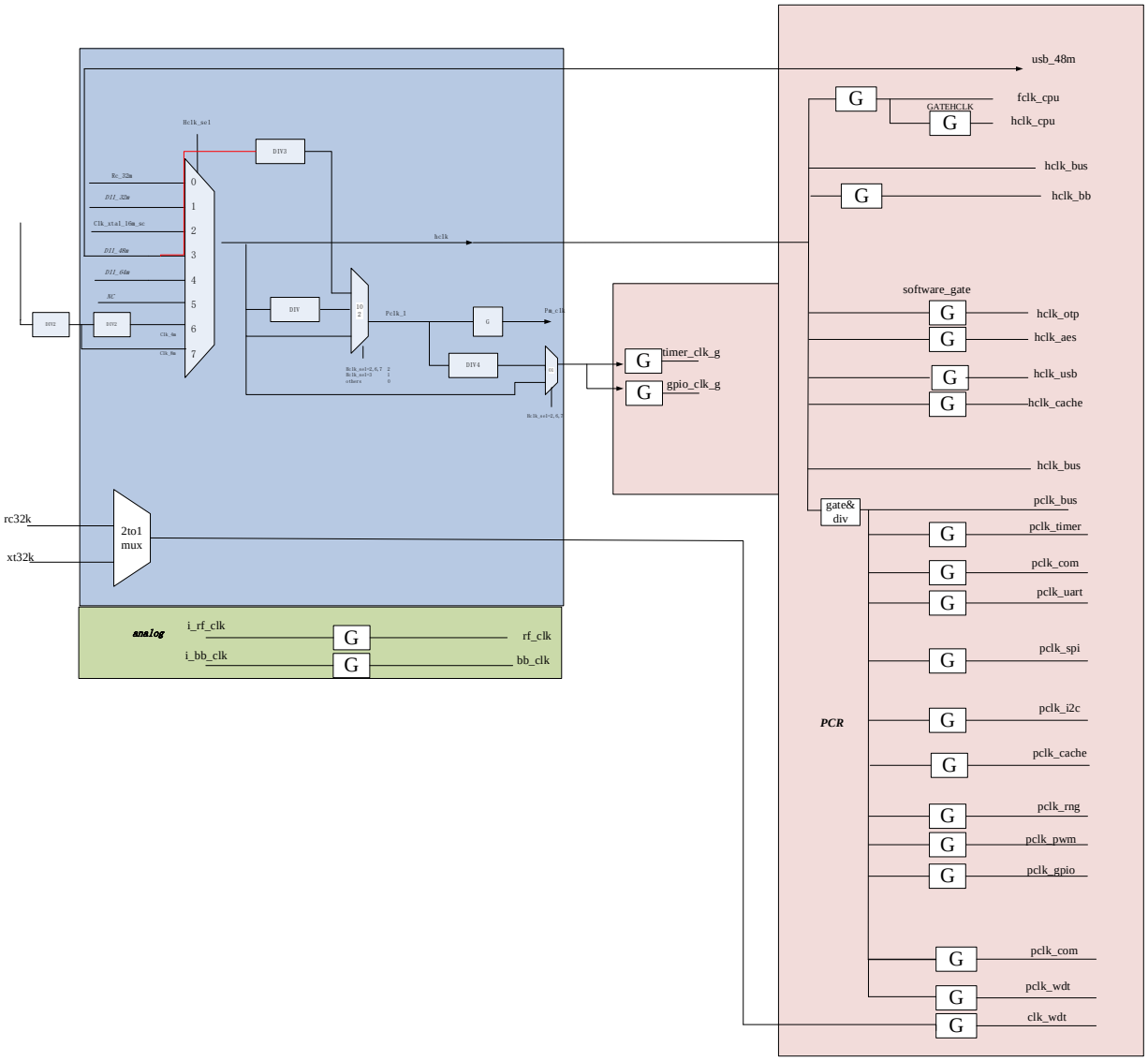


Figure 11: Clock Structure Diagram

3.9 IOMUX

The IOMUX provides a flexible I/O configuration, as the ports of most of the peripherals can be configured and mapped to specific physical I/O pads (I/O at die boundary). These peripheral modules include I2C, UART, USB, PWM 0-5, SPI, etc. However, for other specific purpose peripherals, their IOs mappings are fixed when they are enabled. These specific purpose peripherals include SWD, analog_ios and GPIOs.

Figure 12 below shows the IOMUX functional diagram.

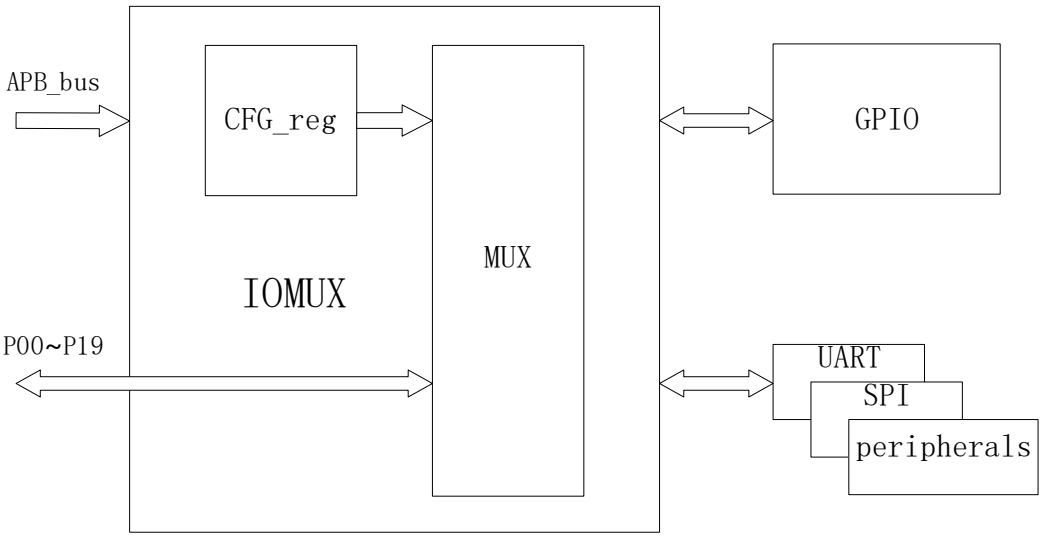


Figure 12: IOMUX structure diagram

There are 20 configurable pads. The table blow shows the mapping of the peripheral IOs that can be mapped through IOMUX. These include I2C, UART, PWM 0-5 and SPI.

On the other hand, there are also special purpose peripherals, whose IOs are fixed to certain physical pads, when these peripheral functions are enabled. These special purpose peripherals include: SWD, analog I/Os (ADC inputs) and GPIO. When they are enabled, their IOs are mapped to physical pads according to the following table.

#	PHY6230	Normal Mode (p8=0@reset active)				
0	GPIO_P00	GPIO	USBDP	pwm0	uart_tx	
1	GPIO_P01	GPIO	USBDM	pwm1	uart_rx	
2	GPIO_P02	SWD_IO	GPIO	spi_rx	pwm0	uart_tx
3	GPIO_P03	SWD_CLK	GPIO	spi_ssn	pwm1	uart_rx
4	GPIO_P04	GPIO	iic_scl	spi_sck	analog_io[0]	uart_tx
5	GPIO_P05	GPIO	iic_sda	uart_tx	analog_io[1]	uart_rx
6	GPIO_P06	GPIO	pwm2	USBDP	analog_io[2]	
7	GPIO_P07	GPIO	pwm3	USBDM	analog_io[3]	
8	GPIO_P08	GPIO	pwm4	rf_rx_en	analog_io[4]	
9	GPIO_P09	GPIO	uart_tx	iic_scl	analog_io[5]	
10	GPIO_P10	GPIO	uart_rx	iic_sda	analog_io[6]	
11	GPIO_P11	GPIO	pwm5	rf_tx_en	analog_io[7]	
12	GPIO_P12	GPIO	spi_rx	pwm2	dbg_mux[0]/pclk_l_div4	
13	GPIO_P13	GPIO	spi_ssn	pwm3	dbg_mux[1]/clk_rc32k	
14	GPIO_P14	GPIO	spi_sck	pwm4	iic_scl	
15	GPIO_P15	GPIO	spi_tx	pwm5	iic_sda	
16	GPIO_P16	GPIO	uart_tx	rf_tx_en	spi_sck	
17	GPIO_P17	GPIO	uart_rx	rf_rx_en	spi_tx	
18	GPIO_P18	GPIO	pwm0	iic_scl	spi_rx	
19	GPIO_P19	GPIO	pwm1	iic_sda	spi_ssn	

Table 10: Peripheral IO mapped through IOMUX (special purpose)

3.10 GPIO

The General Purpose I/Os are a type of peripheral that can be mapped to physical I/O pads and programmed by software. The flexible GPIO are organized as PORT A. PortA has bi-direction 20 bit lines, e.g., GPIO_PORT A [19:0]. With default setting, physical pads: P00-P19 are connected to PortA. When all GPIOs are enabled, as described in the IOMUX table in IOMUX section.

All PortA pins can be configured as bi-directional serial interface, by selecting as input or output direction, and their corresponding data can be either read from or written to registers. All PortA and pins support wake-up and debounce function, and all pins support interrupt.

Each GPIO pins can be pulled up to VDD3 or pulled down to ground by adding pull up or pull down resistors to have default functions/states.

For more detailed info, please refer to "PHY623x GPIO Application Notes", in software SDK document folder.

#	PHY6230	Default Mode		Default IN_OUT		Pull up/dn		IRQ	Wakeup
		Burning	Boot	Burning	Boot	Burning	Boot		
0	GPIO_P00	GPIO	GPIO	IN	IN	Floating	Floating	√	√
1	GPIO_P01	GPIO	GPIO	IN	IN	Floating	Floating	√	√
2	GPIO_P02	SWDIO	SWDIO	IN	IN	Floating	Floating	√	√
3	GPIO_P03	SWDCLK	SWDCLK	IN	IN	Pull dn	Pull dn	√	√
4	GPIO_P04	UART_Tx	GPIO	OUT	IN	Pull up	Floating	√	√
5	GPIO_P05	UART_Rx	UART_Rx	IN	IN	Floating	Floating	√	√
6	GPIO_P06	GPIO	GPIO	IN	IN	Floating	Floating	√	√
7	GPIO_P07	GPIO	GPIO	IN	IN	Pull dn	Pull dn	√	√
8	GPIO_P08	GPIO	GPIO	IN	IN	Floating	Floating	√	√
9	GPIO_P09	GPIO	GPIO	IN	IN	Floating	Floating	√	√
10	GPIO_P10	GPIO	GPIO	IN	IN	Floating	Floating	√	√
11	GPIO_P11	GPIO	GPIO	IN	IN	Floating	Floating	√	√
12	GPIO_P12	GPIO	GPIO	IN	IN	Floating	Floating	√	√

Table 11: PHY6230 GPIO Application Notes

3.10.1 DC Characteristics

TA=25℃, VDD=3 V

PARAMETER	TEST CONDITIONS	Min.	TYP	Max.	Unit
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.4			V
Logic-0 input current	Input equals 0 V	-50		50	nA
Logic-1 input current	Input equals VDD	-50		50	nA
Logic-0 output voltage, 10-mA pins	Output load 10 mA			0.5	V
Logic-1 output voltage, 10-mA pins	Output load 10 mA	2.5			V

Table 12: DC Characteristics

4 Peripheral Blocks

4.1 2.4GHz Radio

The 2.4 GHz RF transceiver is designed to operate in the worldwide ISM frequency band at 2.4 to 2.4835 GHz. Radio modulation modes and configurable packet structure make the transceiver interoperable with *Bluetooth*® low energy (BLE) protocol implementations.

- General modulation format
  - FSK (configurable modulation index) with configurable Gaussian Filter Shaping
  - On-air data rates
  - 1Mbps/2Mbps
- Transmitter with programmable output power of -20dBm to +10dBm, in 3dB steps
- RSSI function (1 dB resolution, ± 2 dB accuracy)
- Receiver sensitivity
  - -96dBm@1Mbps BLE
  - -93dBm@2Mbps BLE
- Embedded RF balun
- Integrated frac-N synthesizer with phase modulation

4.2 Timer/Counters (TIMER)

The implementation can include a 32-bit SysTick system timer, that extends the functionality of both the processor and the NVIC. When present, the NVIC part of the extension provides:

- A 32-bit system timer (SysTick)
- Additional configurable priority SysTick interrupt.

General purpose timers are included in the design. With the input clock running at 4Mhz.

4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24-bit COUNTER, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

4.4 AES-ECB Encryption (ECB)

The ECB encryption block supports 128-bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption.

4.5 Watchdog Timer (WDT)

A count down watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep

periods for low power applications and when the debugger has halted the CPU.

4.6 SPI

The SPI interface supports 3 serial synchronous protocols which are SPI, SSP and Microwire serial protocols. The SPI is master only.

4.7 I2C

This I2C block support 100Khz, and 400Khz modes. It also supports 7-bit address and 10-bit address. It has built-in configurable spike suppression function for both lines.

4.8 UART

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with up to 1Mbps baud. Parity checking and generation for the 9th data bit are supported.

4.9 Pulse Width Modulation (PWM)

PHY6230 supports 6 channels of Pulse Width Modulation (PWM) outputs. PWM outputs generate waveforms with variable duty cycle or pulse width programmed by registers. And each of the 6 PWM outputs can be individually programmed. Their duty cycles are controlled by programming individual counters associated with each channel.

The master clock is 16MHz. For each PWM outputs, first there is a prescaler (pre-divider) with division ratio of 2 to 128 (only 2^N division ratios are supported), followed by another 16bit counter with programmable max count, denoted as top_count. When the 16bit counter counts from 0 to top_count, it resets back to 0. So the frequency of the PWM is given by:

Freq_PWM = 16MHz / (N_prescaler * N_top_count);

A threshold counter number can be programmed, when the 16bit counter reaches the threshold, PWM output toggles. So the duty cycle is:

Duty_cycle_PWM = N_threshold/N_top_count;

The polarity of the PWM can also be programmed, which indicates output 1 or 0 when counter is below/above the threshold. A PWM waveform vs counter values are illustrated in the following **Figure 13**, where the polarity is positive. Also in this case the counter ramps up and then resets, we call it “up mode”.

There is also a “up and down mode”, where the counter ramps up to count_top and then ramps down, instead of reset.

As discussed above, the key register bits for one PWM channel are: 16bit top_count, 16bit threshold count, 3bit prescaler count, PWM polarity, PWM mode (up or up/down), PWM enable, and PWM load enable (load new settings). All 6 PWM channels can be individually programmed by registers with addresses from 0x4000_E004 to 0x4000_E044. In addition, one should enable registers 0x4000_E000<0><4> to allow all PWM channels can be programmed. For details please refer to documents of PHY623x register tables.

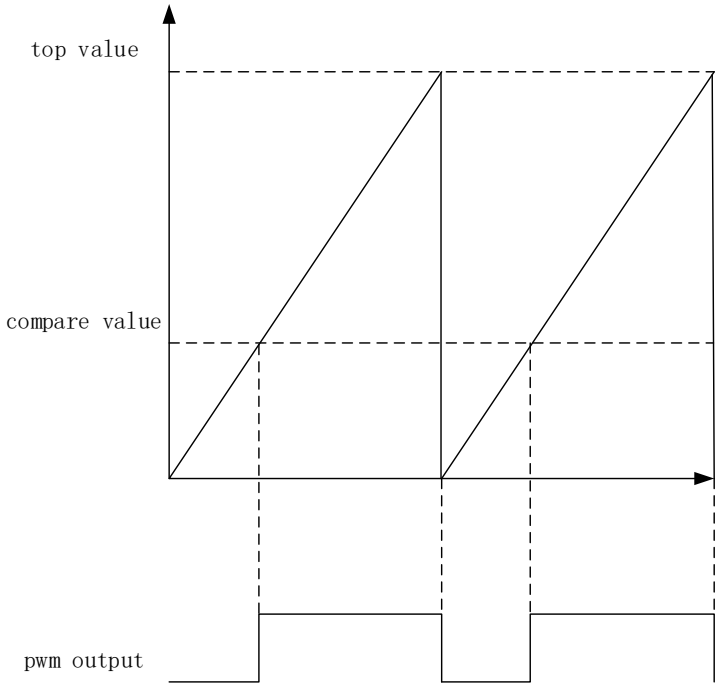


Figure 13: PWM operation

4.10 USB Controller

The USB controller is compatible with the full speed(FS) and low speed(LS) USB specification. It provides 8 endpoints: EP0 IN/OUT supports input and output control data transfer;EP1~EP7 IN/OUT support input and output interrupt data transfer; In addtion,EP7 supports input isochronous data transfer.

4.11 Analog to Digital Converter (ADC)

The 12bit SAR ADC has total 10 inputs. Among them, there are two for VDD3 and VBAT detection, and 8 channel for external IO input, which can be programmed to 4 pairs of differential input or six single-ended inputs. There is a manual mode with which the ADC can be configured to convert a specific input in single-ended or differential and with max 320KHz ADC sampling rate.

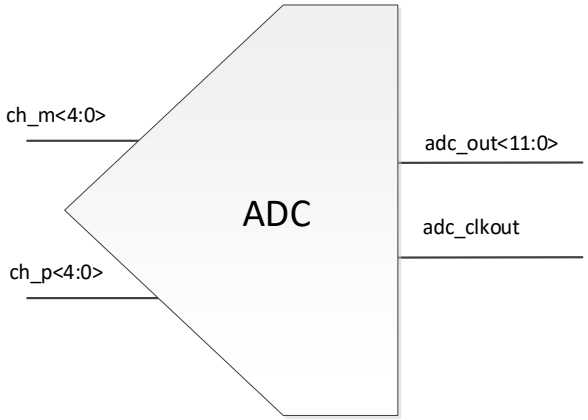


Figure 14: ADC

4.11.1 ADC Channel <3:0> Connectivity

ADC	Hardwired	Single	differential	note
aio<0>	gpio<4>	Chsel1:N		
aio<1>	gpio<5>	Chsel1:P		
aio<2>	gpio<6>	Chsel2:N		
aio<3>	gpio<9>	Chsel2:P		
aio<4>	gpio<10>	Chsel3:N		
aio<5>	gpio<11>	Chsel3:P		
aio<6>	gpio<12>	Chsel4:N		
aio<7>	gpio<13>	Chsel4:P		
aio<8>	Vdd3/4	Chsel0:N	-	
aio<9>	Vbat/5	Chsel0:P	-	

Table 13: ADC channel connectivity

Aio<9:7,4:0>can be selected through an analog Mux by programming aio_pass<7:0> and aio_attn<7:0>. For example, register 0x4000_F020<8><0> set to 01, then Aio<0> is connected to ADC input B negative.

0x4000_F020		Register Description
[15 : 8]	Attenuation ctrl	attn[7:0]. analogIO control for {aio<9>, aio<8>,aio<7>,aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass through 10 attenuate to 1/4 11 NC
[7 : 0]	pass ctrl	pass[7:0]. analogIO control for {aio<9>, aio<8>,aio<7>,aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass through 10 attenuate to 1/4 11 NC note: analog IO sharing gpio<4>/aio<0> gpio<5>/aio<1> gpio<6>/aio<2> gpio<9>/aio<3> gpio<10>/aio<4> gpio<11>/aio<5> gpio<12>/aio<6> gpio<13>/aio<7> VDD3/4/aio<8> VBAT/5/aio<9>

Table 14: analog Mux

5 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which PHY6230 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the PHY6230. **Table 15** specifies the absolute maximum ratings for PHY6230.

Symbol	Parameter	Min.	Max.	Unit
Supply voltages				
VDD3		-0.3	+3.6	V
Vbus		-0.3	+5.5	V
Vbat		-0.3	+5.5	V
DEC			1.32	V
VSS			0	V
I/O pin voltage				
VIO		-0.3	VDD + 0.3	V
Environmental				
Storage temperature		-40	+125	℃
MSL	Moisture Sensitivity Level		3	
ESD HBM	Human Body Model Class 2		2	kV
ESD CDMQF	Charged Device Model (SSOP24, SOP16 and TSSOP8 package)		500	V
Flash memory				
Endurance			100 000	write/erase cycles
Retention			10 years at 40 ℃	
Number of times an address can be written between erase cycles			2	times

Table 15: Absolute maximum ratings

6 Operating Conditions

The operating conditions are the physical Parameters that PHY6230 can operate within as defined in **Table 16**.

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD3	Supply voltage, normal mode	1.8	3	3.6	V
Vbus	Supply voltage	4.5	5	5.5	V
Vbat	Supply voltage	3.0	3.7	5.5	V
tr_VDD	Supply rise time (0 V to 1.8 V)			100	ms
TA	Operating temperature	-40	27	125	°C

Table 16: Operating conditions

7 Radio Transceiver

7.1 Radio Current Consumption

Parameter	Description	MIN	TYP	MAX	UNIT
Tx only at 0dBm	@3V		10		mA
Rx Only	@3V		10		mA

Table 17: Radio current consumption

7.2 Transmitter Specification

Parameter	Description	MIN	TYP	MAX	UNIT
RF Max Output Power			10		dBm
RF Min Output Power			-20		dBm
OBW for BLE 1Mbps	20dB occupy-bandwidth for BLE modulation 1Mbps		1100		KHz
OBW for BLE 2Mbps	20dB occupy-bandwidth for BLE modulation 2Mbps		2300		KHz
FDEV for BLE 1Mbps	Frequency deviation for GFSK modulation 1Mbps	160		250	KHz
FDEV for BLE 2Mbps	Frequency deviation for GFSK modulation 2Mbps	320		500	KHz

Table 18: Transmitter specification

7.3 Receiver Specification

7.3.1 RX BLE 1Mbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 1Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-96		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		7		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB

Parameter	Description	MIN	TYP	MAX	UNIT
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 19: RX BLE 1Mbps GFSK

7.3.2 RX BLE 2Mbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 2Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-93		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		-5		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		9		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		30		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		40		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 20: RX BLE 2Mbps GFSK

7.4 RSSI Specifications

Parameter	Description	MIN	TYP	MAX	UNIT
RSSI Dynamic Range			70		dB
RSSI Accuracy	RSSI Accuracy Valid in range -100 to -30dBm		+/-2		dB
RSSI Resolution	Totally 7bit, from 0 to 127		1		dB
RSSI Period			8		us

Table 21: RSSI specifications

8 Glossary

Term	Description
AHB	Advanced High-performance Bus
AHB-AP	DAP AHB Port for debug component access thru AHB bus
AMBA	Advanced Microcontroller Bus Architecture
AON	Always-on power domain
APB	Advanced Peripheral Bus
APB-AP	DAP APB Port for debug component access thru APB bus
BROM	Boot ROM
DAP	Debug Access Port
ETM	Embedded trace module
FPU	Floating Point Unit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound, Integrated Interchip Sound
ITM	Instrumentation Trace Macrocell Unit
JTAG	Joint Test Access Group (IEEE standard)
JTAG-AP	DAP's JTAG Access Port to access debug components
JTAG-DP	DAP's JTAG Debug Port used by external debugger
J&M	Jun and Marty LLC
MPU	Memory Protection Unit
NVIC	Nested vector Interrupt Controller
PCR	Power Clock Reset controller
POR	Power on reset, it is active low in this document
RFIF	APB peripheral to interface RF block
SoC	System on chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access memory
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver and Transmitter
WDT	Watchdog Timer

Table 22: Glossary

9 Ordering information

9.1 Chip Marking Example

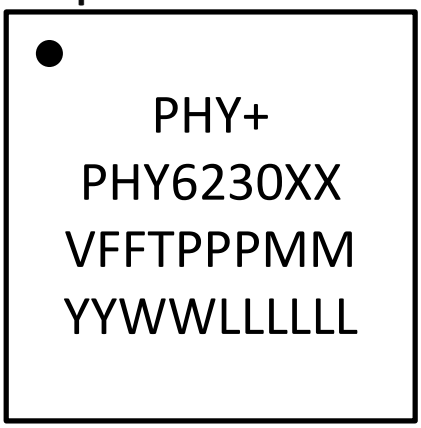


Figure 15: Chip Marking Example

9.2 Chip Marking Rule

<PHY+>
<PHY6230><XX>
<V><FF><T><PPP><MM>
<YY><WW><LLLLLL>

Figure 16: Chip Marking Rule

Abbreviation	Definition and Implemented Codes
<PHY+>	PHYPLUS MICROELECTRONIC
<PHY6230>	PHY6230 Product
<XX>	Package Type
<V>	Supply Voltage
<FF>	Flash Size
<T>	Operating Temperature
<PPP>	Product Information
<MM>	Manufacturer Information
<YY>	2-digital Year Code
<WW>	2-digital Week Code
<LLLLLL>	6-digital Wafer Lot Code

Table 23: Chip Marking Rule

9.3 Order Code

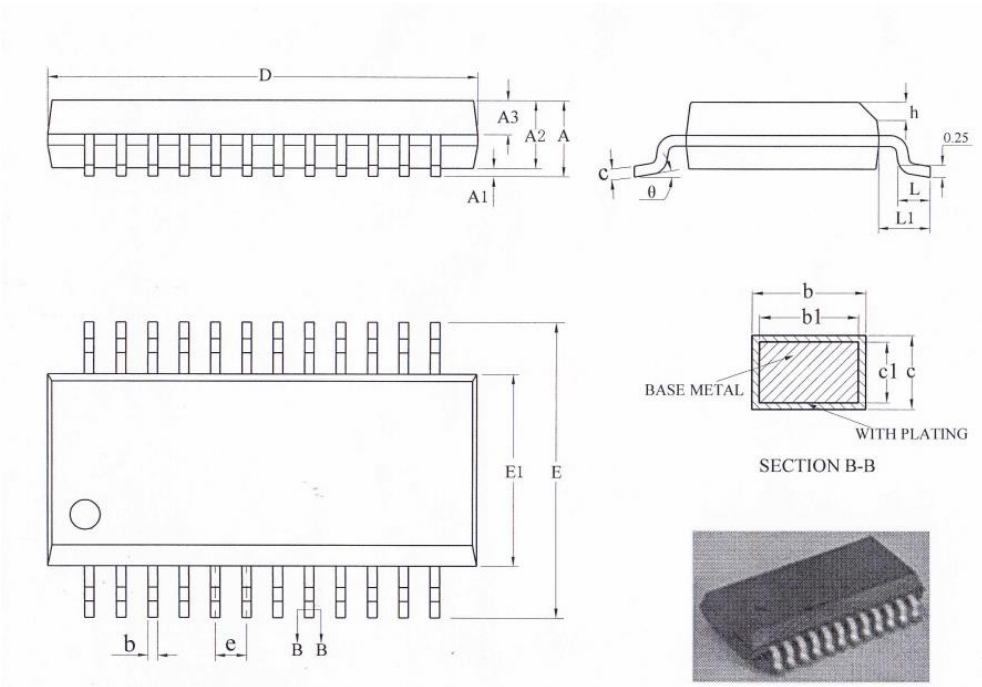
Part No.	Package	Supply Voltage	Operating Temp. (°C)	Flash	Packing	Quantity			
						ea /tube	tube /inner	inner /case	ea /case
PHY6230SD-W00C	SSOP24	1.8~5.5V	-40~125	NA	Tube	50	100	10	50000
PHY6230SC-W00C	SOP16	1.8~5.5V	-40~125	NA	Tube	50	100	10	50000
PHY6230SF-W00C	TSSOP8	1.8~5.5V	-40~125	NA	Tube	100	120	6	72000

Table 24: Order Code

10 Package Dimensions

Note: dimensions are in mm, angels are in degree.

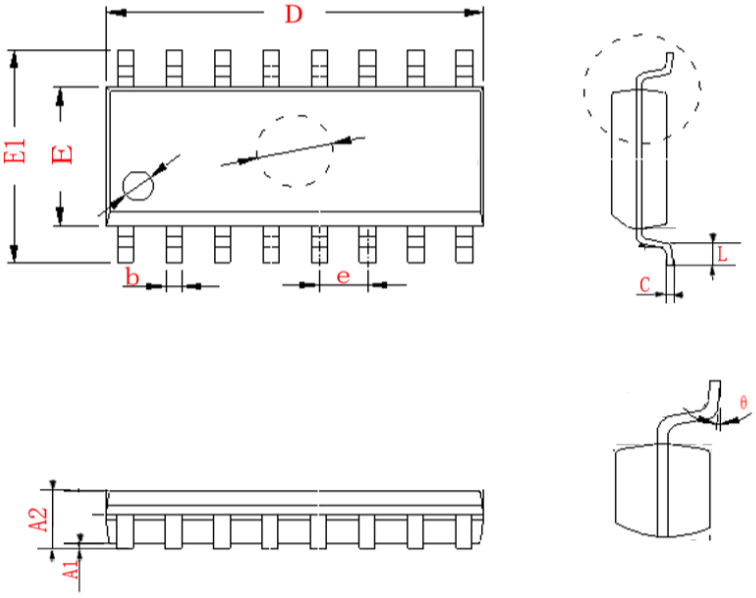
10.1 SSOP24



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 17: SSOP24 Package Dimensions

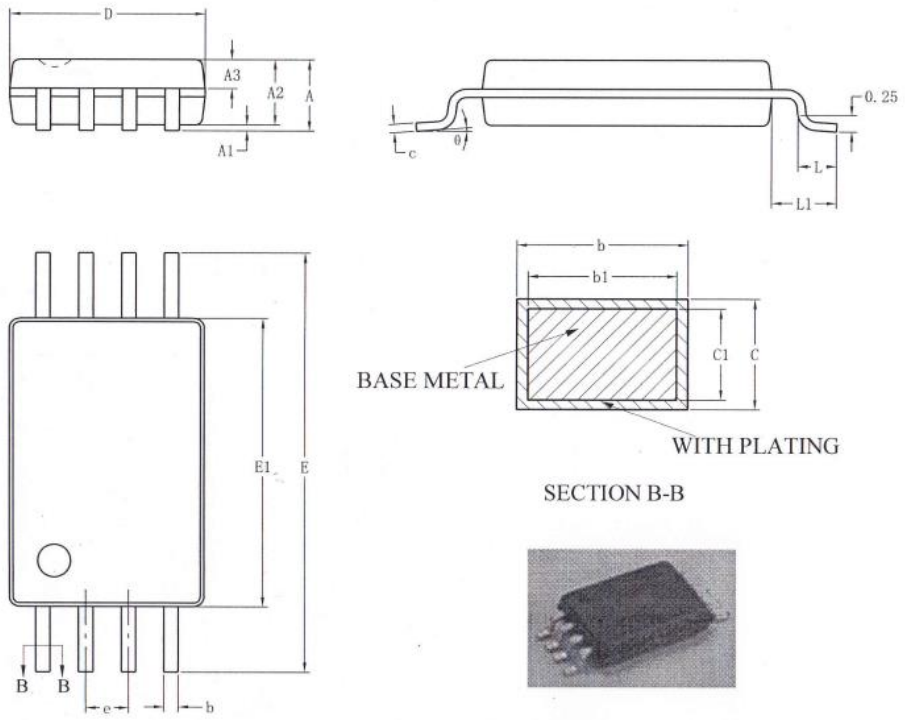
10.2 SOP16



SYMBOL	MILLIMETER	
	MIN	MAX
A1	0.1	0.25
A2	1.25	1.55
B	0.33	0.51
E	3.8	4
E1	5.8	6.2
D	9.8	10.2
E	1.27BSC	
C	0.17	0.25
L	0.4	1.27
θ	0°	8°

Figure 18: SOP16 Package Dimensions

10.3 TSSOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	2.90	3.00	3.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	8°

Figure 19: TSSOP8 Package Dimensions

11 Sample Application and Layout Guide

11.1 Sample Application

11.1.1 SSOP24

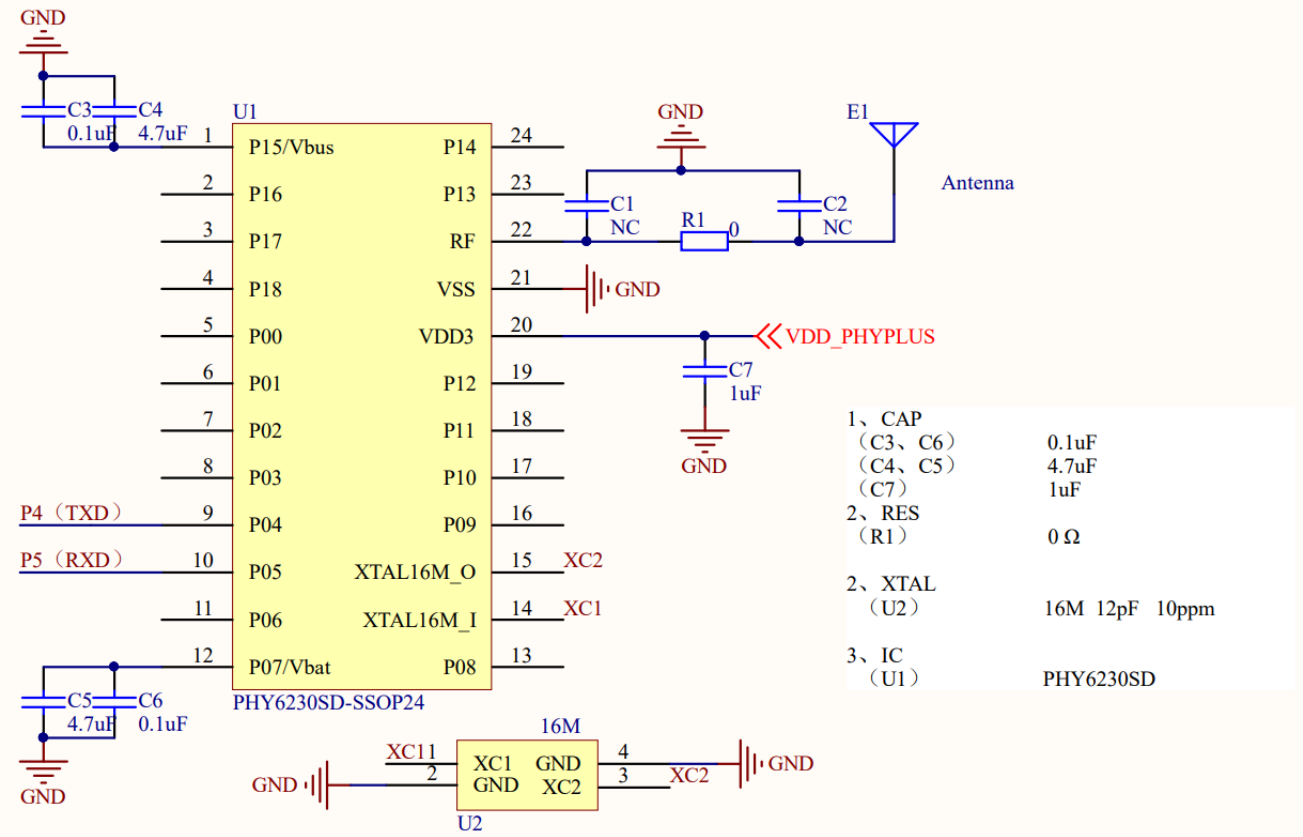


Figure 20: Sample Application of SSOP24

11.1.2 SOP16

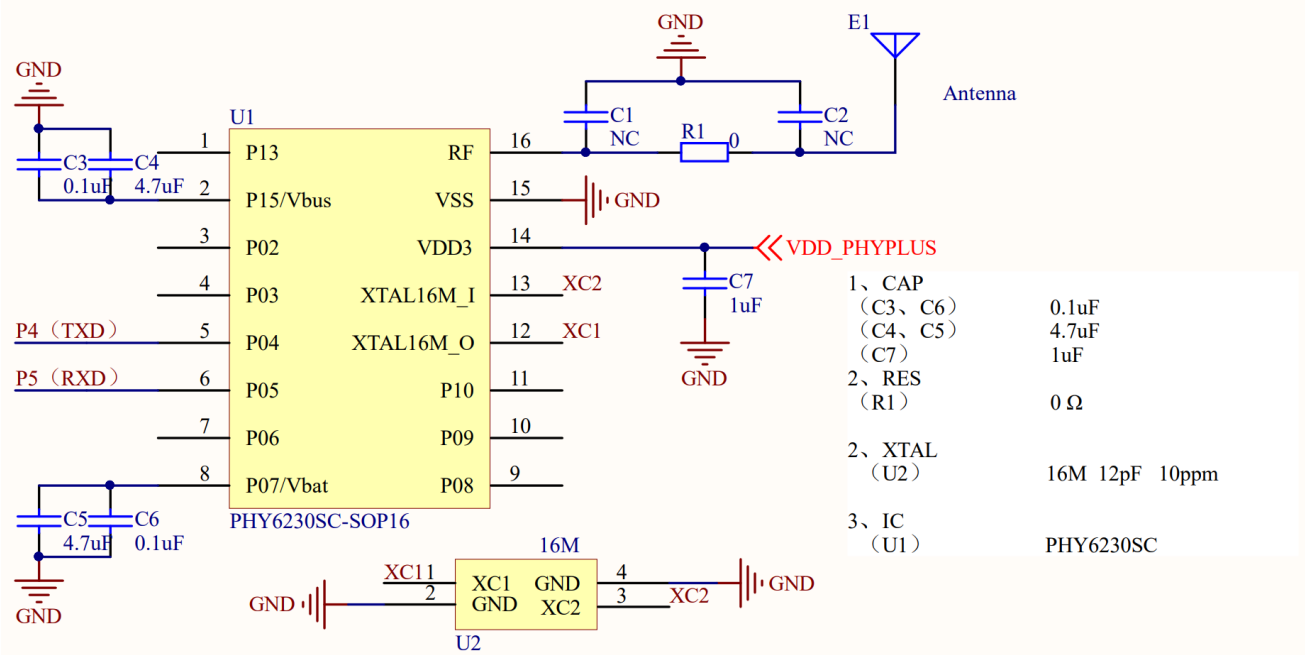


Figure 21: Sample Application of SOP16

11.1.3 TSSOP8

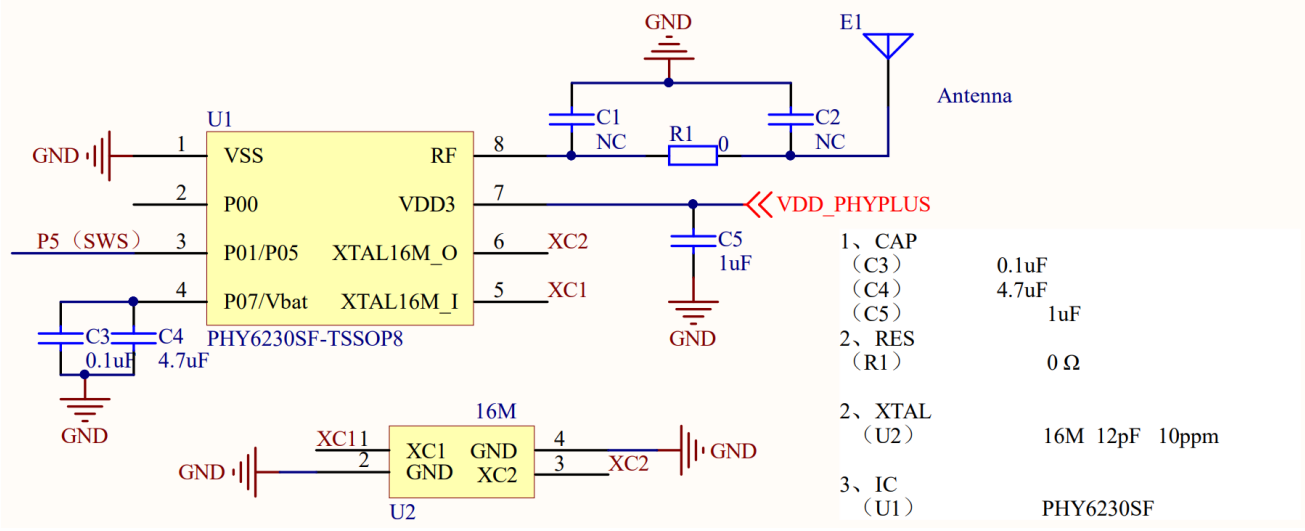


Figure 22: Sample Application of TSSOP8

11.2 Layout Guide

11.2.1 Placement

1. RF matching/Loop filter leading to antenna should be isolated from any other AC/DC signal as much as possible;
2. Xtal/OSC clock is a noise source to other circuits, keep clock trace as short as possible and away from any important area;
3. LDO's are sensitive and could be easily contaminated, care should be taken for the environment;
4. Antenna is the main RF radiation point, other important blocks should be shielded or away from this area.

RF traces

1. Define RF line width with given dielectric thickness (thickness of PCB dielectric layer to ground plain) to achieve 50ohm impedance; this is mainly for the RF line connecting to matching/loop filter and antenna.
2. Differential traces should be kept in the same length and component should be placed symmetrically;
3. Certain length of RF trace should be treated as part of RF matching.

11.2.2 Bypass Capacitor

1. Each VDD pin needs a bypass capacitor to release chip internal noise and block noise from power supply.
2. For power traces, bypass capacitors should be placed as close as possible to VDD pins.
3. Use one large and one small capacitor when the pin needs two capacitors. Typically the capacitance of the larger capacitor is about 100 times of that of the smaller one. The smaller capacitor usually has better quality factor than the larger one. Place the larger capacitor closer to the pin.
4. The capacitors of Loop filter need to have larger clearance to prevent EMC/EMI issue.
5. Ground via should be close to the Capacitor GND side, and away from strong signals.

11.2.3 Layer Definition

1. Normally 4 layer PCB is recommended.
2. RF trace must be on the surface layer, i.e. top layer or bottom.
3. The second layer of RF PCB must be "Ground " layer , for both signal ground and RF reference ground , DO NOT put any other trace or plane on second layer, otherwise "antenna effect" will complicate debug process.
4. Power plane generally is on the 3rd layer.
5. Bottom layer is for "signal " layer.
6. If two layer PCB is used, quality will degrade in general. More care needs to be taken. Try to maximize ground plane, avoid crossing of signal trace with other noise lines or VDD, shield critical signal line with ground plane, maximize bypass capacitor and number of ground vias.

11.2.4 Reference clock and trace

1. Oscillator signal trace is recommended to be on the 1st layer;
2. DO NOT have any trace around or across the reference clock (oscillator) trace.
3. Isolate the reference clock trace and oscillator by having more GND via around.
4. DO NOT have any other traces under the Oscillator.

11.2.5 Power line or plane

1. Whether to use power plain or power line depend on the required current, noise and layout condition. For RF chip, we generally suggest to use power line to bring power into IC pin. Line has parasitic inductance, which forms a low pass filter to reduce the noise traveling around PCB.
2. Add more conductive via on the current source, it will increase max current limit and reduce inductance of via.
3. Add some capacitor alone the power trace when power line travels a long distance.
4. DO NOT place power line or any plane under RF trace or oscillator and its clock trace , the strong clock or RF signal would travel with power line.

11.2.6 Ground Via

1. Ground Via must be as close to the ground pad of bypass capacitor as possible , too much distance between via and ground pad will reduce the effect of bypass capacitor.
2. Having as many ground via as possible.
3. Place ground via around RF trace, the RF trace should be shielded with via trail.