

| DIMENSION | Index [0] | Index [1] | Index [2] | Index [3] | Index [4] | Index [5] | Index [6] | Index [7] | Index [8] | Index [9] |
|--------------------------|-----------|--------------|-------------------|---|---|---------------------------------|-----------|-----------|-----------|-----------|
| 0: Width | 1 | 2 | 4 | 8 | | | | | | |
| 1: Fetchspeed | 1 | 2 | | | | | | | | |
| 2: Scheduling | In-order | Out-of-order | | | | | | | | |
| 3: RUU Size | 4 | 8 | 16 | 32 | 64 | 128 | | | | |
| 4: LSQ Size | 4 | 8 | 16 | 32 | | | | | | |
| 5: Memports | 1 | 2 | | | | | | | | |
| 6: L1 D\$ Sets | 32 | 64 | 128 | 256 | 512 | 1024 | 2048 | 4096 | 8192 | |
| 7: L1 D\$ Ways | 1 | 2 | 4 | | | | | | | |
| 8: L1 I\$ Sets | 32 | 64 | 128 | 256 | 512 | 1024 | 2048 | 4096 | 8192 | |
| 9: L1 I\$ Ways | 1 | 2 | 4 | | | | | | | |
| 10: Unified L2 Sets | 256 | 512 | 1024 | 2048 | 4096 | 8192 | 16384 | 32768 | 65536 | 131072 |
| 11: Unified L2 Blocksize | 16 | 32 | 64 | 128 | | | | | | |
| 12: Unified L2 Ways | 1 | 2 | 4 | 8 | 16 | | | | | |
| 13: TLB Sets | 4 | 8 | 16 | 32 | 64 | | | | | |
| 14: L1 D\$ Latency | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | |
| 15: L1 I\$ Latency | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | |
| 16: Unified L2 Latency | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |
| 17: Branch Predictor | Perfect | NotTaken | Bimodal, 2K entry | 2 Level GAp: 1 8-entry history, four 256 entry bimodal tables | 2 Level PAg: 4 8-entry histories, one 256 entry bimodal table | Combined (Tournament predictor) | | | | |