3. Introduction to the Nexys 4 FPGA Board:

Please review Nexys 4 details from your first week of lab/lecture material dir pdf pdf .avi .

4. FPGA Design Flow:

Please refer to your first week's lab on Nexys 4: Xilinx_project_synthesis_on_Vivado .pdf .mp4

5. Prelab: (Refer to the first paragraph of nexys4_rm.pdf for the first two questions)

Q 5. 1: Circle the family and device category of the FPGA used on Nexys4 board? (1pt)

7 Series		UltraScale		UltraScale+	
Spartan-7	Artix-7	Kintex UltraScale	Virtex UltraScale	Kintex UltraScale+	Virtex UltraScale+
Kintex-7	Virtex-7				

Q 5. 2: Google "CSG324 @Xilin.com" and find what is CSG324 in the part number of the device used on Nexys-4? (1pt)

❑ Speed grade ☑ Package ❑ Serial number ❑Model number

Q 5. 3: The **state memory** is usually implemented using: (2pts)

❑ And-Or gates
❑ RAM
☑ flip-flops
❑ latches

Q 5. 4: We will implement the detour signal controller using One-Hot state assignment method. How many D-flip-flops are needed to implement the controller? (2pts) 7

On power-on reset (i.e when power is first applied to the system), how many Flip-Flops are preset? 1 (1pt) and how many are cleared? 6 (1pt)

In the schematic `ee254l_detour.sch` (on page 11), next state logic for which state(s) is complete? (2pts)

IDLE, L12, L123

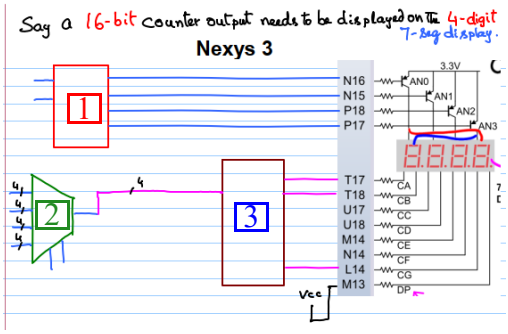
Next State Logic (NSL) is purely a combinational (*combinational/sequential*) circuit. (2pts)

Output Function Logic (OSL) is purely a Combinational (*combinational/sequential*) circuit. (2pts)

Q 5. 5: Refer to the figure on the right, reproduced from this pdf, suggesting a way to display the output of a 16-bit binary number as a 4-digit hexadecimal number going from 0000 to FFFF on the 4 SSDs of a Nexys-3 board.

Name the three components and also state whether it is a combinational logic or a sequential logic.

1. 2/4 Decoder (combinational)
2. 4/1 mux (combinational)
3. Hex to SSD converter (combinational)



Now, if we want to display the output of a 32-bit binary counter as an 8-digit hexadecimal number going from 0000 0000 to FFFF FFFF on the 8 SSDs of a Nexys-4 board, what three components you intend to use?

1. 3/8 Decoder
2. 4bit wide 8/1 mux
3. Hex to SSD converter

Do you believe that one of the above two displays is brighter. _____ Yes / No.

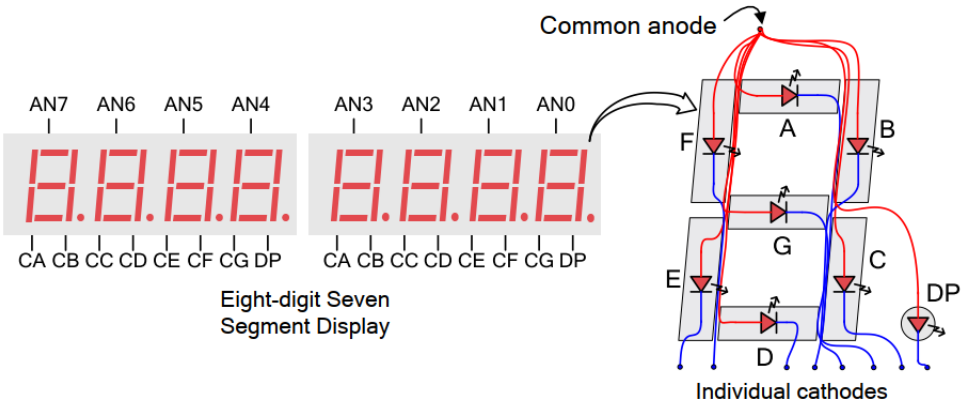
If you said "Yes", then which is brighter? A (A/B).

A= 16-bit counter display on the 4 digits of Nexys-3, B= 32-bit counter display on the 8 digits of Nexys-4

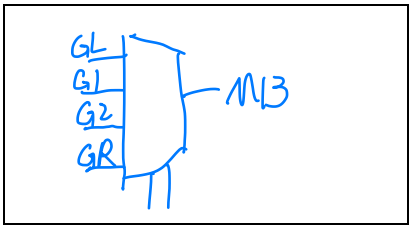
Why? Because the frequency is higher

Q 5. 6: In the above diagram, VCC (= 3.3 volts = a constant logic 1) was tied inside the FPGA to the DP (via pin M13) to make all (one dot point/all dot points) continuously off (to be on/to be off)

Q 5. 7: Though we do not perform fractional arithmetic needing to display a dot point (such as the dot point in 23.42 or 1.234) in this course, it is possible to do so as the so called SSDs (Seven Segment Displays) contain actually 8 segments per digit including the dot point.



In a revised detour lab, suppose that you are given a Nexys-3 board with all singular LEDs removed. You are asked to use the four dot points on the 4 SSDs to represent the 4 groups of lights, GL, G1, G2, and GR. Show (on the side) **the needed additions** to control pin M13 in the figure in the above Q 5.5 to achieve this.



7. Lab Report:

Name:_____	Date: _____
Lab Session: _____	TA's Signature: _____

For TAs: Pre-lab (10): _____	Schematic completion (70): _____	Report (out of 20): ___
Comments:		

Q 7. 1: Refer to Xilinx UG616.What are the two different D-flip-flops that are used in this lab? What is the difference between them? (2pts)

FDP (output High when power applied)

FDC (output low when power applied)

Q 7. 2: Name 2 more D-flip-flops that are available in the Xilinx library UG616 (and have enable pins) and briefly explain how are they different from the ones that are used in this lab.(8pts)

FDR (set output low on positive clock edge)

FDS (set output High on positive clock edge)

Q 7. 3: Which pin of the FPGA is connected to the **BtnC** on the Nexys 4 board? Refer to the reference manual for the Nexys 4 or the .xdc file of Nexys 4 (see files in the dir) . (4pts)

E16

Q 7. 4: Which three special buffers are needed for signals that connect to the input and output devices (including the on-board clock generator) ? Give their names and whether they are needed to connect inputs or outputs or both. (6pts)

BUFGP (Both)

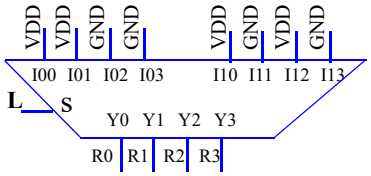
OBUF (Output)

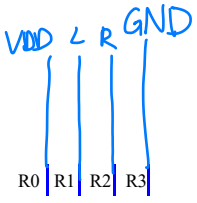
IBUF (input)

Q 7. 5: The frequency of the clock entering the FPGA is 100MHz. Notice that we are dividing the input clock by using counters. Calculate the frequency of the divided clock (`DIVCLK[25]`) that triggers the detour signal state machine. (5pts)

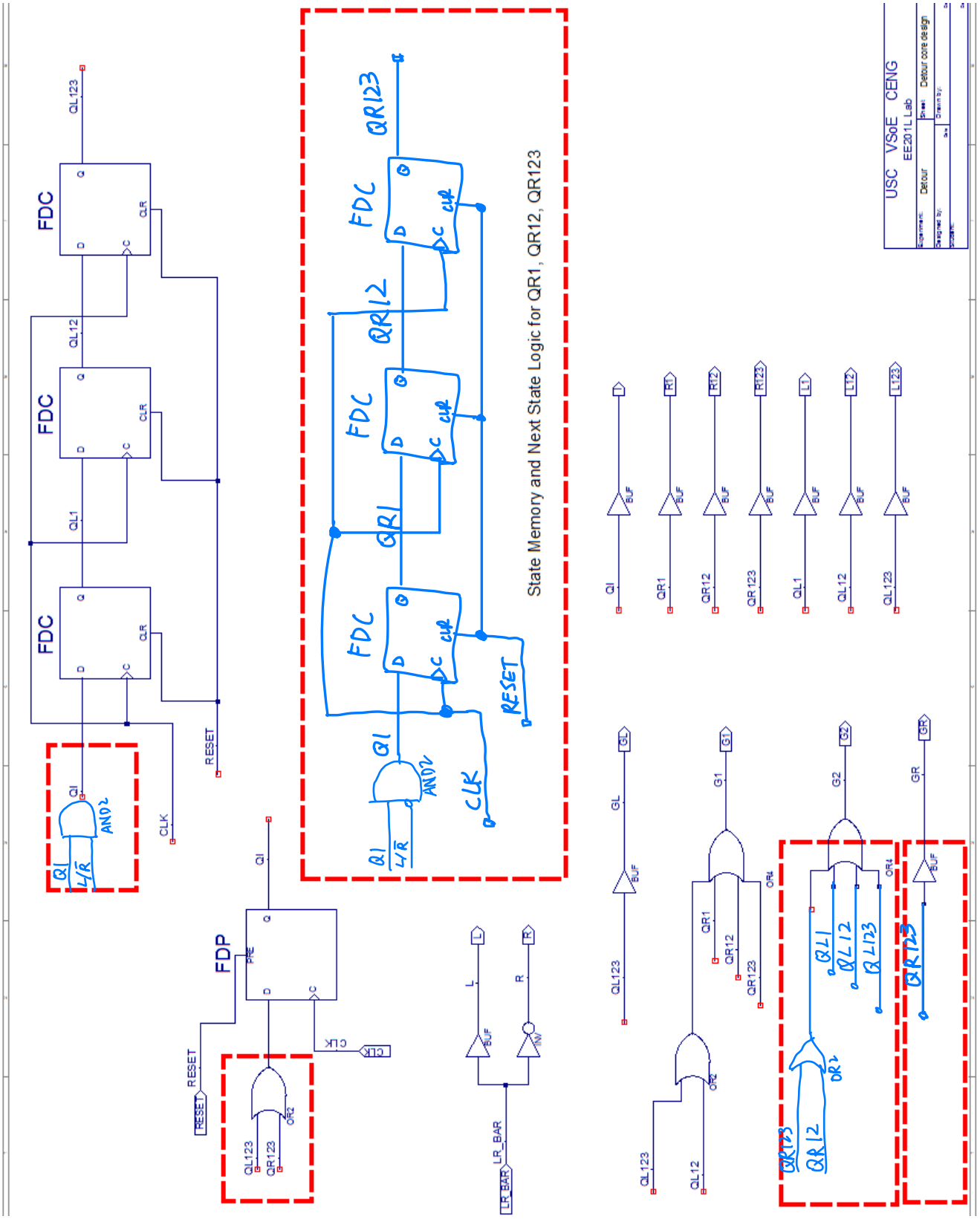
$\frac{100MHZ}{2^{26}} = 1.49\ HZ$

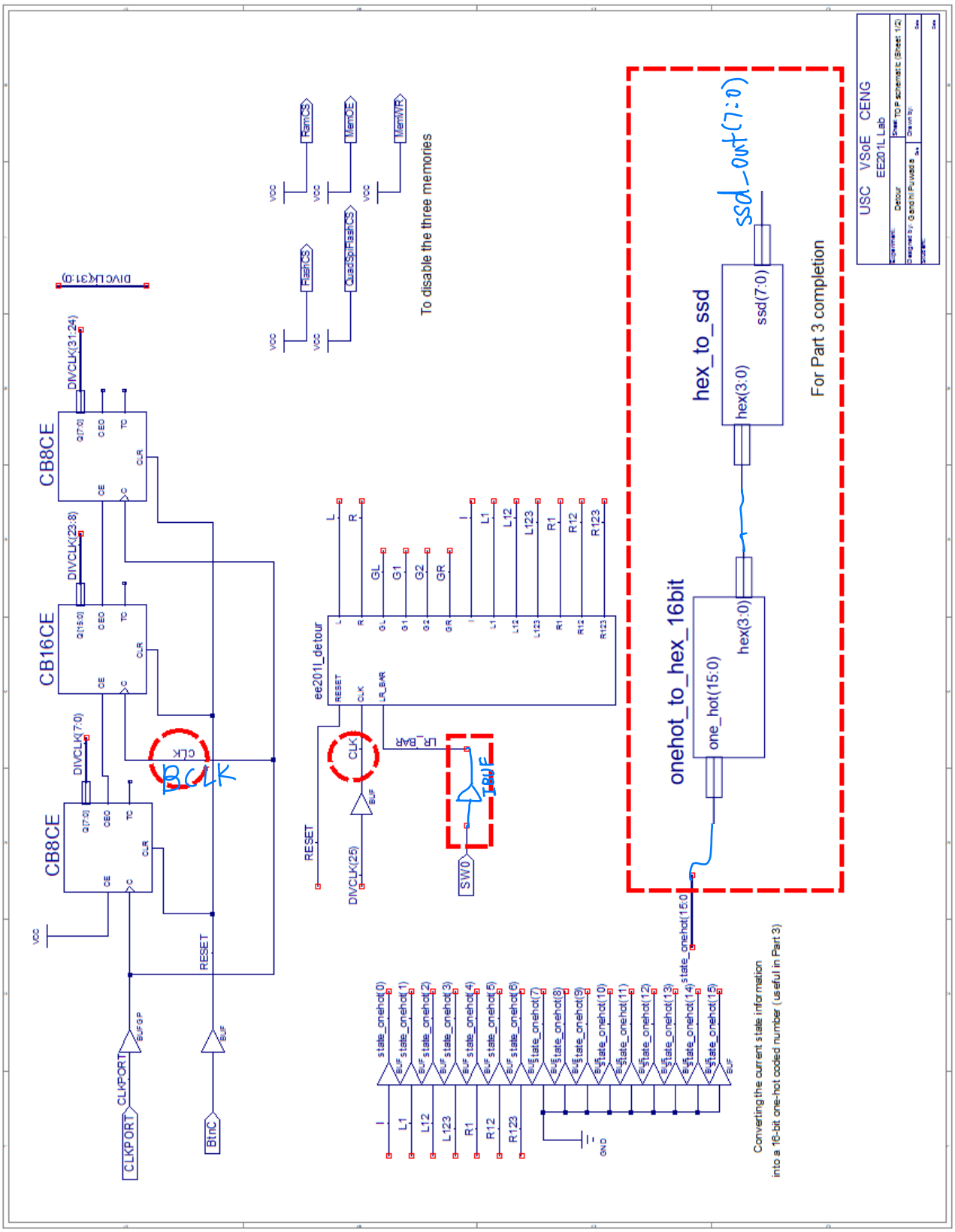
Q 7. 6: Here, L (for Left) and R (for Right) are always opposite to each other. Can you optimize (simplify) the 4-bit output R0 R1 R2 R3 generating combinational logic on the side? Try to avoid the expensive 4-bit wide 2-to-1 mux by tying either **VDD** or **GND** or **L** or **R** as appropriate to each of the four outputs.Note: Since **R** = ~**L**, instead of generating **L_Bar** by inverting **L**, you can use **R** wherever you need **L_Bar**.

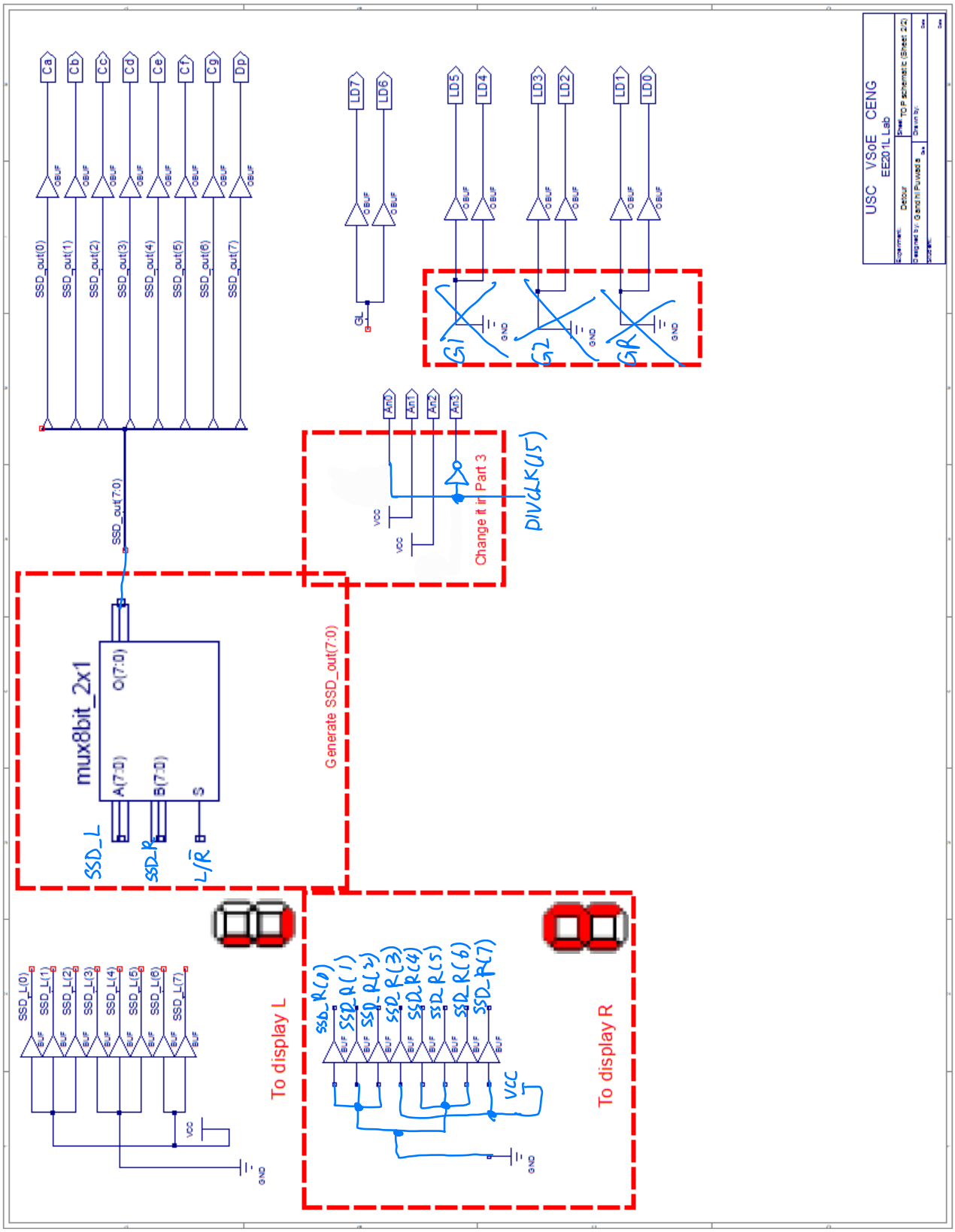




Based on the above, you suggest that you could have avoided mux 8 bit 2x1 8-bit wide 2-to-1 mux in the second page of the top schematic.

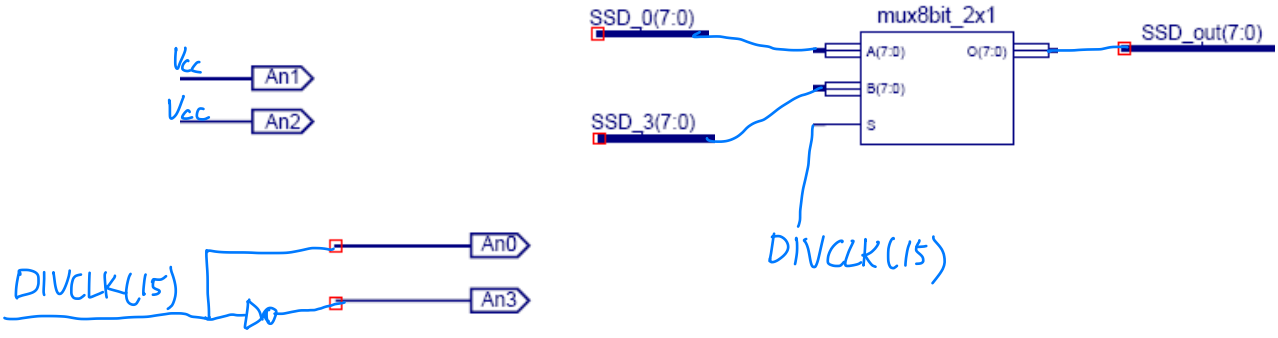

State Memory and Next State Logic for QR1, QR12, QR123
USC VSoE CENG
EE201L Lab
FDC
FDP
AND2
OR2
OR4
BUF
INV
RESET
CLK
LR_BAR


USC VSoE CENG
EE201L Lab
To disable the three memories
FlashCS
QuadSpiFlashCS
RamCS
MemOE
MemWR
CB8CE
CB16CE
CB8CE
DIVCLK(31:24)
DIVCLK(23:8)
DIVCLK(7:0)
DIVCLK(31:0)
CLK
BCLK
RESET
CLKPORT
BtnC
ee201l_detour
LR_BAR
IBUF
SW0
DIVCLK(25)
hex_to_ssd
hex(3:0)
ssd(7:0)
ssd_out(7:0)
onehot_to_hex_16bit
one_hot(15:0)
state_onehot(15:0)
For Part 3 completion
Converting the current state information
into a 16-bit one-hot coded number (useful in Part 3)

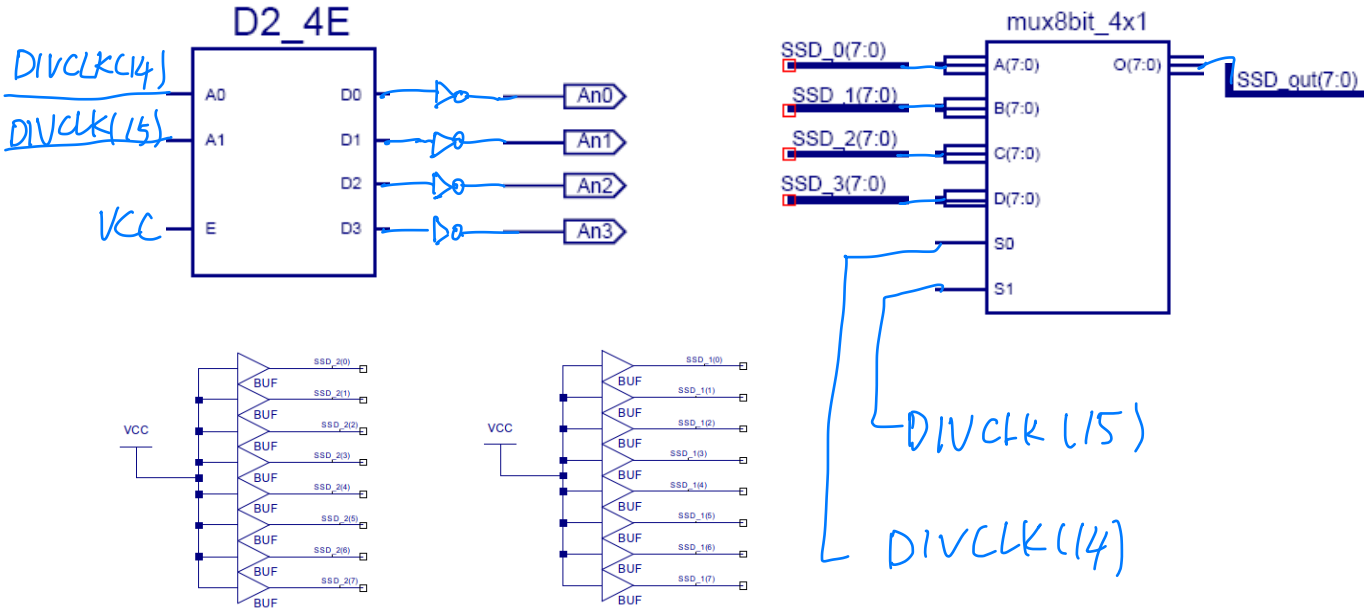

USC VSoE CENG
EE201L Lab
Ca
Cb
Cc
Cd
Ce
Cf
Cg
Dp
LD7
LD6
LD5
LD4
LD3
LD2
LD1
LD0
SSD_out(0)
SSD_out(1)
SSD_out(2)
SSD_out(3)
SSD_out(4)
SSD_out(5)
SSD_out(6)
SSD_out(7)
SSD_out(7:0)
GL
G1
G2
GR
An0
An1
An2
An3
Change it in Part 3
DIVCLK(15)
mux8bit_2x1
O(7:0)
A(7:0)
B(7:0)
S
SSD_L
SSD_R
L/R
Generate SSD_out(7:0)
To display L
To display R
VCC
GND

Part 3 On this page generate only Anode and Cathode controls.

Method #1: Permanently disable **`AN1`** and **`AN2`**. Then activate **`AN0`** and **`AN3`** alternately at a reasonable speed *(neither too fast nor too slow,* your TA will help*)* while sending the correct 7-segment (actually 8-segment) signals (**`Ca-Cg`**) to the SSDs. You need a 8-bit wide 2-to-1 mux for this. You might use `DIVCLK(15)` to alternately enable one of **`SSD0`** or **`SSD3`** to accomplish this.



Method #2: Instead of permanently disabling **`AN1`** and **`AN2`** (as in Method#1), let us send **`Ca-Cg,Dp=11111111`** to the 8 cathodes (remember these are active low so this will blank the displays). Now we need to activate the 4 anodes, one at a time in sequence, while sending the corresponding 8-segment information to the cathodes with a 8-bit wide 4-to-1 mux.
You can use perhaps `DIVCLK(15:14)` for this purpose.



You can use a 2x4 decoder such as the above **`D2_4E`** . Look up the Xilinx library UG616 for the D2_4E decoder to check if the enable input is active high or low and the outputs are active high or active low. We also provided you with the 8-bit wide 4x1 mux shown above. The diagrams on pages 18/29 to 20/29 (section 9.1 on Seven Segment Display) of the Nexys 4 reference manual will help you in understanding the scanning operation. **Celebrate the completion of your lab!**