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CPE 301 - 1104
Assignment # 3
9/30/2016

Assignment Description:

This lab involved building two different memory modules by rearranging two 16x4 memory chips and their surrounding wiring: a memory module with 32 words consisting of 4 bits each and a memory module with 16 words consisting of 8 bits each. This also involved rigging up switches for address select and data input, and a button to switch between read and write mode. We tested the modules by writing and then reading specified words of data at specified addresses, verifying the results on the scope (noting that the output from the chips was the complement of the data input, and we had to invert the scope results to get a matching answer).

Problems Encountered:

While I personally felt I had a good understanding of the theory of the lab, in practice I found building the boards a difficult and messy process. Due to general confusion our group implemented the board in the order described by the lab document, instead of the opposite order recommended by the TA, which did not help matters.

As a consequence I spent most of the lab building and verifying the results for the first board (messily, as you shall see), and ran out of time to build the second. I then built most of the second board at home on my own time. Without the time/space constraints of the lab I was able to do a neater job, with a calmer understanding of what was going on. I then brought the board back to the lab, added the chips, and tested it for correctness. While my theoretical understanding is good I think and was firmed up by the process, my board building was definitely exposed as a bit on the slow side.

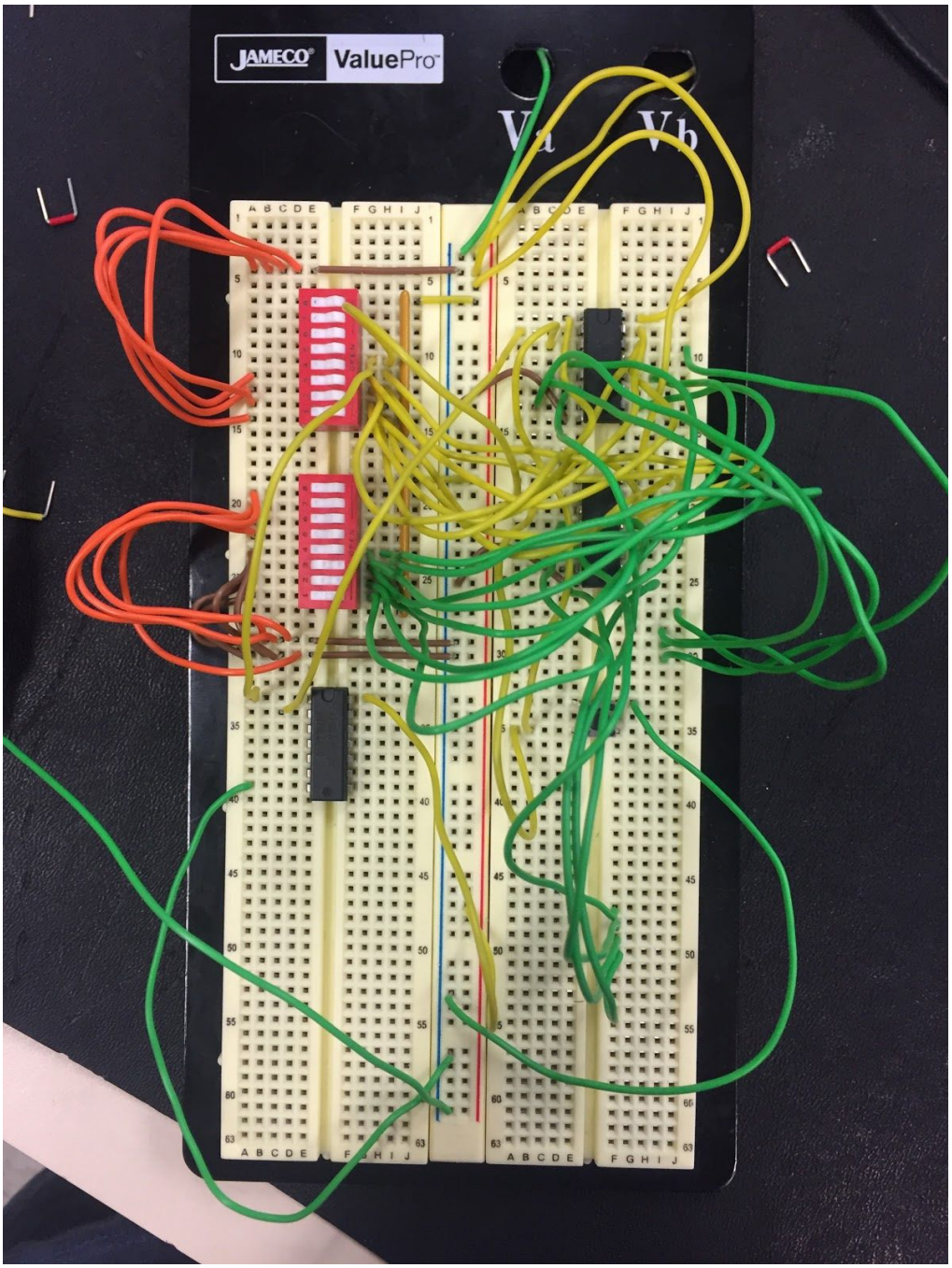
Lessons Learned:

Firmed up my understanding of the idea behind different ways to organize separate chips to make memory modules with different dimensions. It’s one thing to see and “get” a diagram and another thing to implement it I suppose. Further review and practice at practical board building was gained, and probably needed in my case! In fact you can see the benefits of this practice between my terribly messy first board and my more sane second one. Sorry about that!

Description of Completed Lab:

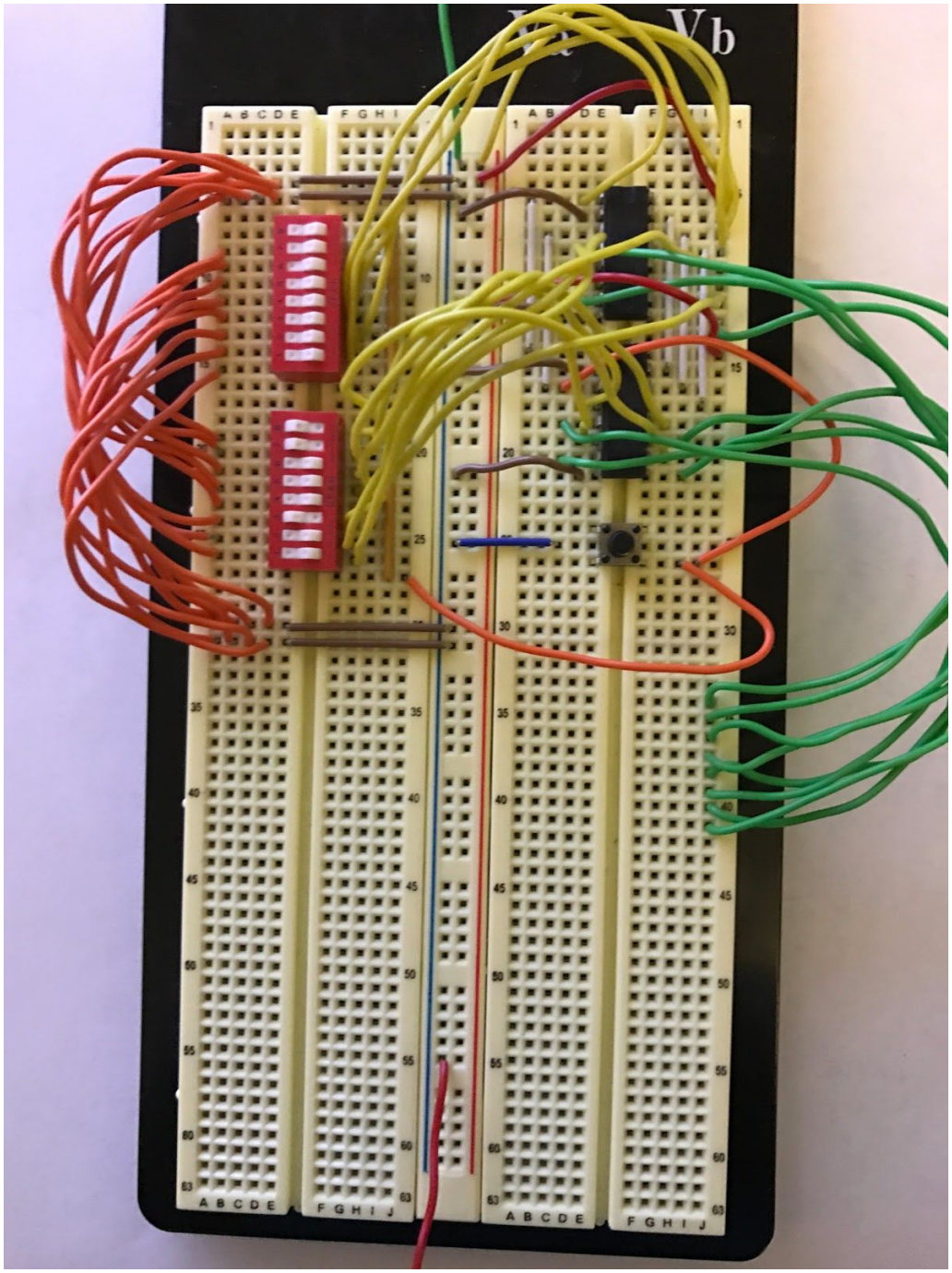
Board 1 (32x4):

Once again, sorry for the messy board. It did work though. Shown here mid-testing. Board could have been improved by routing the 4 outputs from each of the two chips to the same location, since only one chip was selected and active at any given time. Note: as the lab document said, the output read on the scope was the complement of the input data. Once the scope value was inverted the input and output matched.



Board 2 (16x8):

Hopefully this board is significantly more readable. Shown here mid-testing. Note: as the lab document said, the output read on the scope was the complement of the input data. Once the scope value was inverted the input and output matched.



Questions

In both cases the memory chips were volatile- when the board was powered off and on again any previously written data was not retained. This was to be expected considering we were working with RAM chips.