## Zilog Z80 instruction set x3 x8 x0 x1 x2 x4 x5 **x6 x**7 x9 хA хC хD хB хE хF LD (BC),A INC BC INC B RLCA LD A, (BC) INC C DEC C **RRCA** NOP LD BC,d16 DEC B LD B,d8 EX AF, AF ADD HL,BC DEC BC LD C,d8 0x1 7 6 1 4 6 4 3 10 1 1 1 4 2 7 1 1 11 1 7 1 1 4 1 2 7 1 4 ----V0-----V1---Y0X-0C --YHX-0C ----V0-----V1---Y0X-0C RRA DJNZ r8 LD DE, d16 LD (DE),A INC DE INC D DEC D LD D,d8 RLA JR r8 ADD HL, DE LD A, (DE) DEC DE INC E DEC E LD E,d8 1x 13/8 10 2 7 1 2 12 1 7 11 --Y0X-0C ----V0-----V1---YHX-0C ----V0-----V1---Y0X-0C LD L,d8 JR NZ, r8 LD HL, d16 LD (a16), HL INC HL INC H DEC H LD H,d8 DAA JR Z,r8 ADD HL, HL LD HL, (a16) DEC HL INC L DEC L CPL 2x 12/7 3 6 1 4 2 12/7 11 2 7 2 10 3 16 1 1 1 4 1 3 16 1 1 1 4 ----V0-----V1-SZYHXP-C --YHX-0C ----V0-----V1---Y1X-1-LD SP,d16 LD (a16),A LD (HL), d8 LD A,d8 JR NC, r8 INC SP INC (HL) DEC (HL) SCF JR C,r8 ADD HL,SP LD A, (a16) DEC SP INC A DEC A CCF 1 11 1 11 3x 2 12/7 3 10 3 13 1 6 2 10 1 4 12/7 1 11 3 13 1 6 1 4 1 4 2 7 ----V0-----V1---Y0X-01 --YHX-0C ----V0-----V1--YHX-0C LD B,C LD C,D LD C,H LD B,B LD B,D LD B,E LD B,H LD B,L LD B, (HL) LD B,A LD C,B LD C,C LD C,E LD C,L LD C, (HL) LD C, A 4x 1 4 4 7 1 4 1 4 1 4 4 1 4 1 7 1 4 LD D,C LD D,A LD E,B LD E,H LD E,L LD E, (HL) LD E,A LD D,B LD D,D LD D,E LD D,H LD D,L LD D, (HL) LD E,C LD E,D LD E,E 5x 4 1 4 1 4 1 4 1 1 4 4 1 4 1 4 1 1 4 1 1 1 4 1 7 1 LD H,C LD H,E LD H,L LD H,A LD L,B LD L,C LD L,H LD H,B LD H,D LD H,H LD H, (HL) LD L,D LD L,E LD L,L LD L,(HL) LD L,A 6x 1 4 1 4 1 4 1 4 1 4 1 4 1 7 1 4 1 4 1 4 1 4 1 1 4 1 4 1 7 1 4 LD (HL),B LD (HL),E HALT LD (HL),C LD (HL),D LD (HL),H LD (HL),L LD (HL),A LD A,B LD A,C LD A,D LD A,E LD A,H LD A,L LD A, (HL) LD A, A 7 x 1 4 1 1 4 4 1 4 1 7 ADD A,B ADD A,C ADD A,D ADD A,E ADD A,H ADD A,L ADD A, (HL) ADD A,A ADC A,B ADC A,C ADC A,D ADC A,E ADC A,H ADC A,L ADC A, (HL) ADC A, A 8x 1 4 1 4 1 4 1 4 1 4 1 7 1 4 1 4 1 4 1 4 1 4 1 4 1 7 1 4 SZYHXV0C SBC A,B SBC A,D SBC A,H SBC A,L SBC A, A SUB B SUB C SUB D SUB E SUB H SUB L SUB (HL) SUB A SBC A,C SBC A,E SBC A, (HL) 9x 1 4 1 4 1 4 1 4 1 4 1 4 1 4 1 7 1 4 1 4 1 4 1 4 1 4 1 4 1 7 1 SZYHXV1C AND B AND C AND D AND E AND H AND L AND (HL) AND A XOR B XOR C XOR D XOR E XOR H XOR L XOR (HL) XOR A 4 1 4 4 7 SZY1XP00 CP L OR B OR C OR D OR E OR H OR L OR (HL) OR A CP B CP C CP D CP E CP H CP (HL) CP A Вx 1 4 7 4 4 1 4 7 1 1 1 4 1 4 4 1 SZYHXV1C SZYHXV1C SZY1XP00 SZY1XP00 SZY1XP00 SZY1XP00 SZYHXV1C SZY1XP00 SZY1XP00 SZY1XP00 SZY1XP00 SZYHXV1C SZYHXV1C SZYHXV1C SZYHXV1C SZYHXV1C ADD A, d8 PREFIX CB RET NZ POP BC JP NZ,a16 JP a16 CALL NZ,a16 PUSH BC RST 00H RET Z RET JP Z,a16 CALL Z,a16 CALL a16 ADC A,d8 RST 08H 3 1 11 2 3 17/10 Cx 11/5 1 10 3 10 3 10 17/10 7 1 11 11/5 10 3 10 X X 3 17 2 7 1 11 SZYHXV0C X SZYHXV0C OUT (d8),A RET NC POP DE JP NC,a16 CALL NC, a16 PUSH DE SUB d8 RST 10H RET C EXX JP C,a16 IN A, (d8) CALL C,a16 PREFIX DD SBC A,d8 RST 18H Dx 11/5 10 10 11 17/10 11 11 11/5 10 17/10 X 7 11 X SZYHXV1C SZYHXV1C PUSH HL RET PO POP HL JP PO, a16 EX (SP), HL CALL PO, a16 AND d8 RST 20H RET PE JP (HL) JP PE, a16 EX DE, HL CALL PE, a16 PREFIX ED XOR d8 RST 28H Ex 11/5 10 19 17/10 11 2 11 11/5 1 4 10 17/10 X X 7 3 10 7 1 3 4 2 1 11 SZY1XP00 SZY1XP00 PREFIX FD RET P POP AF JP P,a16 DI CALL P,a16 PUSH AF OR d8 RST 30H RET M LD SP,HL ΕI CALL M,a16 CP d8 RST 38H JP M,a16 Fx 11/5 10 3 10 1 4 17/10 1 11 2 7 1 11 11/5 1 6 10 1 4 17/10 X X 2 7 11 SZYHXPNC SZY1XP00 SZYHXV1C **Prefix CB** x0 x1 x2 x3 x4 x5 **x6 x**7 **x8** x9 хA хB xCхD хE хF RLC B RLC E RLC H RLC L RRC B RRC C RRC H RRC L RLC C RLC D RLC (HL) RLC A RRC D RRC E RRC (HL) RRC A 0x 2 2 8 2 8 2 8 2 2 8 2 8 2 2 2 15 2 8 8 2 2 2 2 8 15 2 SZY0XP0C RL B RL C RL D RL E RL H RL L RL (HL) RL A RR B RR C RR D RR E RR H RR L RR (HL) RR A 1x 2 8 8 2 2 8 15 2 2 8 2 2 2 15 2 SZY0XP0C SLA B SLA C SLA D SLA E SLA H SLA L SLA (HL) SLA A SRA B SRA C SRA D SRA E SRA H SRA L SRA (HL) SRA A 2x 2 8 8 2 15 2 15 SZY0XP0C \*SLL L \*SLL B \*SLL C \*SLL D \*SLL E \*SLL H \*SLL (HL) \*SLL A SRL B SRL C SRL D SRL E SRL H SRL L SRL (HL) SRL A 2 8 3x2 8 2 8 2 8 2 8 2 8 2 15 2 8 2 8 2 8 2 8 2 8 2 8 2 15 2 8 SZY0XP0C BIT 1, (HL) BIT 0,B BIT 0,C BIT 0,D BIT 0,E BIT 0,H BIT 0,L BIT 0, (HL) BIT 0,A BIT 1,B BIT 1,C BIT 1,D BIT 1,E BIT 1,H BIT 1,L BIT 1,A 4x 2 8 2 12 2 8 2 8 2 12 2 8 2 8 2 8 2 8 2 8 2 8 2 8 SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-BIT 2,B BIT 2,C BIT 2,D BIT 2,E BIT 2,H BIT 2,L BIT 2, (HL) BIT 2,A BIT 3,B BIT 3,D BIT 3,H BIT 3, (HL) BIT 3,C BIT 3,E BIT 3,L BIT 3,A 5x 2 8 2 8 2 8 2 8 2 8 2 12 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 12 2 8 2 8 SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-BIT 4, (HL) BIT 4,B BIT 4,C BIT 4,D BIT 4,E BIT 4,H BIT 4,L BIT 4,A BIT 5,B BIT 5,C BIT 5,D BIT 5,E BIT 5,H BIT 5,L BIT 5, (HL) BIT 5,A 2 8 2 8 6x 2 8 2 8 2 12 2 8 2 8 2 8 2 8 2 12 SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-BIT 7, (HL) BIT 6,B BIT 6,C BIT 6,D BIT 6,E BIT 6,H BIT 6,L BIT 6, (HL) BIT 6,A BIT 7,B BIT 7,C BIT 7,D BIT 7,E BIT 7,H BIT 7,L BIT 7,A 7 x 2 8 2 8 2 12 2 8 2 8 2 8 2 12 2 8 2 8 2 8 2 8 2 8 SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-RES 0,C RES 0,E RES 0, (HL) RES 0,B RES 0,D RES 0,H RES 0,L RES 0,A RES 1,B RES 1,C RES 1,D RES 1,E RES 1,H RES 1,L RES 1, (HL) RES 1,A 8x 2 8 2 8 2 8 2 8 2 8 2 8 2 15 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 15 2 8 RES 2,B RES 2,C RES 2,D RES 2,E RES 2,H RES 2,L RES 2, (HL) RES 2,A RES 3,B RES 3,C RES 3,D RES 3,E RES 3,H RES 3,L RES 3, (HL) RES 3,A 2 8 2 8 9x 2 8 2 8 2 8 2 8 2 8 2 15 2 8 2 8 2 8 2 8 2 8 2 8 2 15 2 8 RES 4,B RES 4,C RES 4,D RES 4,E RES 4,H RES 4,L RES 4, (HL) RES 4,A RES 5,B RES 5,C RES 5,D RES 5,E RES 5,H RES 5,L RES 5, (HL) RES 5,A 2 8 2 8 2 8 2 8 2 8 15 2 8 2 8 2 8 2 8 2 8 2 8 15 2 8 Ax 2 8 2 RES 6,E RES 6, (HL) RES 7,B RES 7,C RES 7,D RES 7,E RES 7,H RES 7,L RES 7, (HL) RES 7,A RES 6,B RES 6,C RES 6,D RES 6,H RES 6,L RES 6,A Вx 2 8 2 8 2 8 2 8 2 8 2 15 2 8 2 8 2 8 2 8 2 2 8 2 8 2 15 2 8 2 8 SET 0,B SET 0,C SET 0,D SET 0,E SET 0,H SET 0,L SET 0, (HL) SET 0,A SET 1,B SET 1,C SET 1,D SET 1,E SET 1,H SET 1,L SET 1, (HL) SET 1,A Cx 2 8 2 8 2 8 2 8 2 8 2 8 2 15 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 15 2 8 SET 2,B SET 2,C SET 2,D SET 2,E SET 2,H SET 2,L SET 2, (HL) SET 2,A SET 3,B SET 3,C SET 3,D SET 3,E SET 3,H SET 3,L SET 3, (HL) SET 3,A 2 8 2 8 2 8 2 8 2 8 15 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 15 2 8 $\mathbf{D}\mathbf{x}$ 2 8 2 SET 4,B SET 4,C SET 4,D SET 4,E SET 4,H SET 4,L SET 4, (HL) SET 4,A SET 5,B SET 5,C SET 5,D SET 5,E SET 5,H SET 5,L SET 5, (HL) SET 5,A Ex 2 8 2 8 2 8 2 8 2 8 2 15 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 15 2 8 2 8 SET 6,B SET 6,C SET 6,D SET 6,E SET 6,H SET 6,L SET 6, (HL) SET 6,A SET 7,B SET 7,C SET 7,D SET 7,E SET 7,H SET 7,L SET 7, (HL) SET 7,A Fx 2 8 2 8 2 8 2 8 2 2 8 2 2 8 2 8 2 2 2 8 2 8 2 8 15 8 2 8 2 15 **Prefix DD** x1 x2 **x**3 x5 **x**7 **x8** x9 x0x4 **x**6 хA хC хD хE хF \*LD BC,d16 \*LD (BC),A \*INC BC \*INC B \*DEC B \*RLCA \*EX AF, AF \*LD A, (BC) \*INC C \*DEC C \*RRCA \*NOP \*LD B,d8 ADD IX, BC \*DEC BC \*LD C,d8 0x2 8 2 11 3 11 2 ----V0---Y0X-0C --YHX-0C ----V1-----V0-----V1---Y0X-0C \*DJNZ r8 \*LD DE,d16 \*LD (DE),A \*INC DE \*INC D \*DEC D \*LD D,d8 \*RLA \*JR r8 ADD IX, DE \*LD A, (DE) \*DEC DE \*INC E \*DEC E \*LD E, d8 \*RRA 3 17/12 2 8 2 8 1x 4 14 2 11 2 8 3 11 2 15 2 11 2 8 2 8 3 11 2 10 2 8 3 16 2 10 ----V0-----V1---Y0X-0C --YHX-0C ----V0-----V1---Y0X-0C LD (a16), IX \*LD IX1,d8 \*JR NZ, r8 LD IX,d16 INC IX \*INC IXh \*DEC IXh \*LD IXh,d8 \*DAA \*JR Z, r8 ADD IX, IX LD IX, (a16) DEC IX \*INC IX1 \*DEC IX1 \*CPL 2 8 2x 2 8 16/11 4 14 4 20 2 10 2 8 2 8 3 11 16/11 2 15 4 20 2 10 2 8 2 8 3 11 ----V0-----V1-SZYHXP-C --YHX-0C ----V0-----V1---Y1X-1-LD \*LD A, d8 \*JR NC, r8 \*LD SP,d16 \*LD (a16),A \*INC SP INC (IX+r8) DEC (IX+r8) \*SCF \*JR C,r8 ADD IX,SP \*LD A,(a16) \*DEC SP \*INC A \*DEC A \*CCF (IX+r8),d83x 3 16/11 4 14 4 17 2 10 23 23 2 8 16/11 2 15 4 17 2 10 2 8 2 8 3 11 2 8 4 19 ----V0---Y0X-01 --YHX-0C --YHX-0C ----V1-----V0-----V1-\_\_\_\_\_ -----\*LD B, IX1 \*LD B,B \*LD B,C \*LD B,D \*LD B,E \*LD B, IXh LD B,(IX+r8) \*LD B,A \*LD C,B \*LD C,C \*LD C,D \*LD C,E \*LD C, IXh \*LD C, IX1 LD C, (IX+r8) \*LD C,A 4x 2 8 2 8 2 8 2 8 2 8 3 19 2 8 2 8 2 8 2 8 2 8 2 8 2 8 3 19 2 8 2 8 \*LD D,D \*LD D, IXh \*LD D, IX1 LD D, (IX+r8) \*LD D,A \*LD E,B \*LD E,C \*LD E,E \*LD E, IXh \*LD E, IX1 LD E, (IX+r8 \*LD D,B \*LD D,C \*LD D,E \*LD E,D \*LD E,A 3 19 5x 2 8 2 2 8 2 2 8 3 19 2 8 2 8 2 2 2 2 8 8 \*LD IXh,B \*LD IXh,C \*LD IXh,D \*LD IXh,E LD IXh, IXh \*LD IXh, IXl |LD H, (IX+r8) \*LD IXh,A \*LD IX1,B \*LD IX1,C \*LD IX1,D \*LD IX1,E LD IX1,IX1 LD L,(IX+r8) \*LD IX1,A 6x 2 2 2 2 2 3 2 2 8 2 8 2 2 2 2 2 2 8 19 8 8 3 19 LD (IX+r8),A LD (IX+r8), B LD (IX+r8), C LD (IX+r8), D LD (IX+r8), E LD (IX+r8), H LD (IX+r8), L \*HALT \*LD A,B \*LD A,C \*LD A,D \*LD A,E \*LD A, IXh \*LD A, IX1 LD A, (IX+r8) \*LD A,A 7 x 3 19 3 19 3 19 3 19 3 19 3 19 2 8 3 19 2 8 2 8 2 8 2 8 2 8 2 8 3 19 2 8 ADD A, ADC A, \*ADD A,B \*ADD A,C \*ADD A,D \*ADD A,E \*ADD A, IXh \*ADD A, IXl \*ADD A,A \*ADC A,B \*ADC A,C \*ADC A,D \*ADC A,E \*ADC A, IXh \*ADC A, IX1 \*ADC A,A (IX+r8)(IX+r8)8x 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 3 19 3 19 SZYHXV0C SBC A, \*SUB D \*SBC A,D \*SBC A,A \*SUB B \*SUB C \*SUB E \*SUB IXh \*SUB IX1 SUB (IX+r8) \*SUB A \*SBC A,B \*SBC A,C \*SBC A,E \*SBC A, IXh \*SBC A, IX1 (IX+r8)9x 2 8 2 8 2 8 8 2 8 19 2 8 2 8 2 8 2 8 2 8 3 19 SZYHXV1C AND (IX+r8) XOR (IX+r8) \*AND B \*AND C \*AND D \*AND E \*AND IXh \*AND IX1 \*AND A \*XOR B \*XOR C \*XOR D \*XOR E \*XOR IXh \*XOR IX1 \*XOR A Ax 2 8 2 8 2 8 2 2 8 19 2 8 2 8 2 8 2 8 2 8 3 19 2 8 SZY1XP00 \*OR B \*OR C \*OR D \*OR E \*OR IXh \*OR IX1 OR (IX+r8) \*OR A \*CP B \*CP C \*CP D \*CP E \*CP IXh \*CP IX1 CP (IX+r8) \*CP A 2 8 2 8 Bx 2 8 2 8 2 8 3 19 2 8 2 8 2 8 2 8 2 8 2 8 3 19 SZY1XP00 SZY1XP00 SZY1XP00 SZY1XP00 SZY1XP00 SZY1XP00 SZY1XP00 SZY1XP00 SZYHXV1C SZYHXV1C SZYHXV1C SZYHXV1C SZYHXV1C SZYHXV1C SZYHXV1C SZYHXV1C \*RST 00H \*POP BC \*CALL NZ,a16 \*PUSH BC \*ADD A,d8 \*RET \*JP Z,a16 \*CALL Z,a16 \*CALL a16 \*ADC A,d8 \*RST 08H \*RET NZ \*JP NZ,a16 \*JP a16 \*RET Z PREFIX DDCB Cx 2 15/9 2 14 4 14 4 14 21/14 2 15 3 11 2 15 2 15/9 2 14 4 14 X X 4 21/14 4 21 3 11 2 15 SZYHXV0C X SZYHXV0C \*JP NC,a16 \*OUT (d8),A \*CALL NC,a16 \*SBC A,d8 \*RET NC \*POP DE \*PUSH DE \*SUB d8 \*RST 10H \*RET C \*EXX \*JP C,a16 \*IN A, (d8) \*CALL C,a16 \*PREFIX DD \*RST 18H Dx 2 15/9 2 14 4 14 3 15 21/14 2 15 3 11 2 15 15/9 2 8 4 14 3 15 21/14 X X 3 11 2 15 SZYHXV1C SZYHXV1C \*RET PO POP IX \*JP PO,a16 \*CALL PO,a16 PUSH IX \*AND d8 \*RST 20H \*RET PE \*JP PE,a16 \*EX DE,HL \*CALL PE,a16 \*PREFIX ED \*XOR d8 \*RST 28H JP (IX) EX (SP), IX 2 15 15/9 2 14 21/14 2 15 3 11 2 15 15/9 2 8 14 2 8 21/14 3 11 Ex 2 4 14 23 X X SZY1XP00 SZY1XP00 \*DI \*RST 38H \*RET P \*POP AF \*JP P,a16 \*CALL P,a16 \*PUSH AF \*OR d8 \*RST 30H \*RET M LD SP, IX \*JP M,a16 \*EI \*CALL M,a16 \*PREFIX FD \*CP d8 2 15/9 2 14 2 15/9 Fx 2 8 21/14 2 15 3 11 2 15 2 10 4 14 2 8 3 11 2 15 4 14 21/14 X X SZYHXPNC SZY1XP00 SZYHXV1C -----\_\_\_\_\_ -----**Prefix DDCB** x3 **x**7 x8 x1 x2 x4 x5 **x**6 x9 хA хC хD хE x0хB хF \*RLC B \*RLC C \*RLC D \*RLC E \*RLC IXh \*RLC IX1 RLC (IX+r8) \*RLC A \*RRC B \*RRC C \*RRC D \*RRC E \*RRC IXh \*RRC IX1 RRC (IX+r8) \*RRC A 0x 12 12 3 12 3 12 3 12 3 12 23 12 12 12 12 12 12 12 23 12 SZY0XP0C \*RL B \*RL C \*RL D \*RL E \*RL IXh \*RL IX1 RL (IX+r8) \*RL A \*RR B \*RR C \*RR D \*RR E \*RR IXh \*RR IX1 RR (IX+r8) \*RR A 1x 12 3 12 3 12 4 23 3 12 12 4 23 3 12 SZY0XP0C \*SLA B \*SLA C \*SLA D \*SLA E \*SLA IXh \*SLA IX1 SLA (IX+r8) \*SLA A \*SRA B \*SRA C \*SRA D \*SRA E \*SRA IXh \*SRA IX1 SRA (IX+r8) \*SRA A 2x 3 12 3 12 3 12 3 12 4 23 3 12 3 12 3 12 3 12 3 12 3 12 4 23 3 12 3 12 3 12 3 12 SZY0XP0C \*SLL B \*SLL C \*SLL D \*SLL E \*SLL IXh \*SLL IX1 SLL (IX+r8 \*SLL A \*SRL B \*SRL C \*SRL D \*SRL E \*SRL IXh \*SRL IX1 SRL (IX+r8) \*SRL A 3 12 3x 3 12 3 12 3 12 3 12 3 12 23 3 12 12 3 12 12 3 12 3 12 3 12 4 23 12 SZY0XP0C BIT 0, BIT 1, \*BIT 0,IX1 \*BIT 0,B \*BIT 0,C \*BIT 0,D \*BIT 0,E \*BIT 0,IXh \*BIT 0,A \*BIT 1,B \*BIT 1,C \*BIT 1,D \*BIT 1,E \*BIT 1,IXh \*BIT 1,IX1 \*BIT 1,A (IX+r8)(IX+r8)3 12 3 12 4x3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 20 4 20 SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-BIT 2, BIT 3, \*BIT 2,IX1 \*BIT 2,B \*BIT 2,C \*BIT 2,D \*BIT 2,E \*BIT 2,IXh \*BIT 2,A \*BIT 3,B \*BIT 3,C \*BIT 3,D \*BIT 3,E \*BIT 3, IXh \*BIT 3, IX1 \*BIT 3,A (IX+r8)(IX+r8)5x 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 20 4 20 SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-BIT 4, BIT 5, \*BIT 4,B \*BIT 4,C \*BIT 4,D \*BIT 4,E \*BIT 4,IXh \*BIT 4,IX1 \*BIT 4,A \*BIT 5,B \*BIT 5,C \*BIT 5,D \*BIT 5,E \*BIT 5, IXh \*BIT 5, IX1 \*BIT 5,A (IX+r8)(IX+r8)3 12 6x 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 20 4 20 SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-BIT 6, BIT 7, \*BIT 6,B \*BIT 6,C \*BIT 6,D \*BIT 6,E \*BIT 6,IXh \*BIT 6,IXl \*BIT 6,A \*BIT 7,B \*BIT 7,C \*BIT 7,D \*BIT 7,E \*BIT 7, IXh \*BIT 7, IX1 \*BIT 7,A (IX+r8)(IX+r8)7 x 3 12 12 3 12 12 12 3 12 3 12 12 3 12 12 3 12 12 3 12 12 4 20 4 20 SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-RES 1, RES 0, \*RES 0,B \*RES 0,C \*RES 0,D \*RES 0,E \*RES 0,IXh \*RES 0,IX1 \*RES 1,B \*RES 1,C \*RES 1,D \*RES 1,E \*RES 1, IXh \*RES 1,IX1 \*RES 1,A \*RES 0,A (IX+r8)(IX+r8)8x 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 4 23 -----------------------------------RES 2, RES 3, \*RES 2,B \*RES 2,C \*RES 2,D \*RES 2,E \*RES 2,IXh \*RES 2,IX1 \*RES 3,C \*RES 3,D \*RES 3,E \*RES 3, IXh \*RES 3, IX1 \*RES 2,A \*RES 3,B \*RES 3,A (IX+r8)(IX+r8)9x 3 12 3 12 3 12 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 4 23 RES 4, RES 5, \*RES 4,B \*RES 4,C \*RES 4,D \*RES 4,E \*RES 4, IXh \*RES 4, IX1 \*RES 4,A \*RES 5,B \*RES 5,C \*RES 5,D \*RES 5,E \*RES 5, IXh \*RES 5, IX1 \*RES 5,A (IX+r8)(IX+r8)Ax 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 4 23 ---RES 6, RES 7, \*RES 6, IXh \*RES 7,D \*RES 7,IX1 \*RES 6,C \*RES 6,B \*RES 6,D \*RES 6,E \*RES 6, IX1 \*RES 6,A \*RES 7,B \*RES 7,C \*RES 7,E \*RES 7,IXh \*RES 7,A (IX+r8)(IX+r8)Bx 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 4 23 ----------SET 0, SET 1, \*SET 0,B \*SET 0,C \*SET 0,D \*SET 0,E \*SET 0,IXh \*SET 0, IX1 \*SET 0,A \*SET 1,B \*SET 1,C \*SET 1,D \*SET 1,E \*SET 1,IXh \*SET 1, IX1 \*SET 1,A (IX+r8)(IX+r8)3 12 3 12 Cx 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 4 23 SET 2, SET 3, \*SET 2,B \*SET 2,C \*SET 2,D \*SET 2,E \*SET 2,IXh \*SET 2,IX1 \*SET 2,A \*SET 3,B \*SET 3,C \*SET 3,D \*SET 3,E \*SET 3,IXh \*SET 3, IX1 \*SET 3,A (IX+r8)(IX+r8)Dx 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 4 23 -----\_\_\_\_\_ --\_\_\_\_\_ SET 4, SET 5, \*SET 4,E \*SET 4,B \*SET 4,C \*SET 4,D \*SET 4, IXh \*SET 4,IX1 \*SET 4,A \*SET 5,B \*SET 5,C \*SET 5,D \*SET 5,E \*SET 5, IXh \*SET 5, IX1 \*SET 5,A (IX+r8)(IX+r8)Ex 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 4 23 ---------------SET 6, SET 7, \*SET 7,D \*SET 6,B \*SET 6,C \*SET 6,D \*SET 6,E \*SET 6,IXh \*SET 6, IX1 \*SET 6,A \*SET 7,B \*SET 7,C \*SET 7,E \*SET 7,IXh \*SET 7, IX1 \*SET 7,A (IX+r8)(IX+r8)3 12 3 12 Fx 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 4 23 **Prefix ED** x0 x1 x2 x3 x4 x5 x7 x8 x9 хB хC хE хF **x6** хA хD \*NOP 0x2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 \*NOP 2 8 2 8 2 8 2 8 2 8 2 8 1x 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 2 8 2 8 \_\_\_\_\_ \*NOP 2x 2 8 2 8 2 8 2 8 2 8 2 2 2 8 2 2 2 8 2 8 2 8 2 8 2 8 8 2 8 \*NOP 2 8 3x 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 OUT (C),B SBC HL,BC LD (a16),BC NEG RETN IM 0 LD I,A IN C, (C)OUT (C),C ADC HL, BC LD BC, (a16) \*NEG RETI \*IM 0 LD R,A IN $B_{r}(C)$ 2 12 4 20 2 12 4x 2 12 2 15 2 8 2 9 2 12 2 15 4 20 2 14 2 8 2 9 2 8 2 14 2 8 SZX0XP0-SZXHXV1C SZXHXV1C \_\_\_\_\_ SZX0XP0-SZXHXV0C SZXHXV1C \_\_\_\_\_ \*RETN SBC HL, DE \*NEG \*RETN IM 1 LD A,I IM 2 LD A,R IN D,(C)OUT (C),D LD (a16), DE IN E, (C)OUT (C),E ADC HL, DE LD DE, (a16) \*NEG 5x 2 12 2 15 2 2 8 2 9 2 12 2 4 20 2 8 2 9 2 12 20 8 2 14 2 12 15 8 2 14 SZX0XP0-SZXHXV1C SZXHXV1C SZY0XP0-SZX0XP0-SZXHXV0C SZXHXV1C SZY0XP0-OUT (C),H SBC HL, HL LD (a16), HL \*NEG \*RETN \*IM 0 RRD IN L, (C) OUT (C),L LD HL, (a16) \*NEG \*RETN \*IM 0 RLD IN H, (C) ADC HL, HL 6x 2 12 2 12 2 15 4 20 2 8 2 14 2 8 2 18 2 12 2 12 2 15 4 20 2 8 2 14 2 8 2 18 SZX0XP0-SZXHXV1C SZXHXV1C SZX0XP0-SZX0XP0-SZXHXV0C SZXHXV1C SZX0XP0-\*IN (C) \*OUT (C),0 SBC HL,SP LD (a16),SP \*NEG \*RETN \*IM 1 \*NOP IN A,(C)OUT (C),A ADC HL,SP LD SP, (a16) \*NEG \*RETN \*IM 2 \*NOP 2 8 2 12 2 12 2 15 4 20 2 12 2 15 7 x 2 8 2 14 2 8 2 8 2 12 4 20 2 14 2 8 2 8 SZX0XP0-SZXHXV1C SZXHXV1C SZX0XP0-SZXHXV0C -----SZXHXV1C \_\_\_\_\_ \*NOP 8x 2 8 2 8 2 8 2 8 8 2 8 2 2 2 8 2 8 2 2 8 2 8 2 8 2 2 8 2 8 \*NOP 9x 2 2 2 2 2 8 2 8 2 2 2 2 2 2 8 2 8 2 2 INI OUTI \*NOP \*NOP \*NOP \*NOP IND \*NOP \*NOP \*NOP \*NOP OUTD LDD CPD LDI 2 16 2 8 2 2 16 2 2 8 8 2 16 2 2 16 2 2 8 2 8 8 Ax 16 2 16 8 2 16 16 2 --X0XV0-SZXHXV1-SZXHXV1-SZXHXV1---X0XV0-SZXHXV1-SZXHXV1-SZXHXV1-OTIR \*NOP \*NOP \*NOP \*NOP LDDR \*NOP \*NOP \*NOP \*NOP LDIR CPIR INIR CPDR INDR OTDR Вx 21/16 21/16 21/16 21/16 2 8 2 21/16 21/16 21/16 2 8 2 8 2 8 2 8 2 8 21/16 2 8 --X0XV0-SZXHXV1-SZXHXV1-SZXHXV1---X0XV0-SZXHXV1 SZXHXV1-SZXHXV1-\*NOP \*NOP Cx 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 \*NOP 2 8 2 8 2 8 2 2 8 2 8 2 2 2 8 8 2 2 8 2 8 2 8 8 Dx 2 8 8 2 2 \*NOP Ex 2 8 2 2 8 8 2 2 2 2 2 2 8 2 8 2 8 8 2 8 2 8 2 2 8 8 8 2 8 \*NOP 2 8 Fx 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 2 8 2 8 2 8 2 8 2 8 2 8 2 8 8 **Prefix FD** x0x1 x2 **x**3 x4 x5 x6 **x**7 **x8 x9** хA хB хC хD хE xF \*NOP \*LD BC,d16 \*LD (BC),A \*INC BC \*INC B \*DEC B \*LD B,d8 \*RLCA \*EX AF, AF ADD IY, BC \*LD A, (BC) \*DEC BC \*INC C \*DEC C \*LD C,d8 \*RRCA 0x 2 11 2 11 2 2 15 3 11 2 14 2 10 ----V0-----V1---Y0X-0C --YHX-0C ----V0-----V1---Y0X-0C \*DJNZ r8 \*LD DE, d16 \*LD (DE),A \*INC DE \*INC D \*DEC D \*LD D, d8 \*RLA \*JR r8 ADD IY, DE \*LD A, (DE) \*DEC DE \*INC E \*DEC E \*LD E, d8 \*RRA 17/12 2 11 2 8 3 11 8 2 11 2 8 3 11 8 1x 4 14 2 10 2 8 2 3 16 2 15 2 10 2 8 2 3 ----V0---Y0X-0C ----V1---YHX-0C ----V0-----V1---Y0X-0C \*JR NZ, r8 LD IY,d16 LD (a16), IY INC IY \*INC IYh \*DEC IYh \*LD IYh,d8 \*DAA \*JR Z, r8 ADD IY, IY LD IY, (a16) DEC IY \*INC IY1 \*DEC IY1 \*LD IY1,d8 \*CPL 2 8 2 8 2x 16/11 4 14 4 20 2 10 2 8 2 8 3 11 16/11 2 15 4 20 2 10 2 8 2 8 3 11 ----V0-----V1-SZYHXP-C --YHX-0C ----V0-----V1---Y1X-1-LD \*JR NC, r8 \*LD SP,d16 \*LD (a16),A \*INC SP INC (IY+r8) DEC (IY+r8) \*SCF \*JR C,r8 ADD IY, SP \*LD A,(a16) \*DEC SP \*INC A \*DEC A \*LD A, d8 \*CCF (IY+r8),d83 2 8 3x 16/11 4 14 4 17 2 10 23 3 23 2 8 16/11 2 15 4 17 2 10 2 8 2 8 3 11 4 19 --Y0X-01 --YHX-0C \_\_\_\_\_ \_\_\_\_\_ ----V0-----V1-\_\_\_\_\_ \_\_\_\_\_ ----V0-----V1--------YHX-0C \*LD B,B \*LD B,C \*LD B,D \*LD B,E \*LD B, IYh \*LD B, IYl LD B,(IY+r8) \*LD B,A \*LD C,B \*LD C,C \*LD C,D \*LD C,E \*LD C, IYh \*LD C, IYl LD C, (IY+r8) \*LD C,A 2 8 2 8 3 19 2 8 2 8 4x 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 3 19 2 8 \*LD D, IYh \*LD D, IYl \*LD D,B \*LD D,C \*LD D,D \*LD D,E LD D,(IY+r8) \*LD D,A \*LD E,B \*LD E,C \*LD E,D \*LD E,E \*LD E, IYh \*LD E, IYl LD E, (IY+r8) \*LD E,A 5x 2 8 2 8 2 8 2 8 2 8 2 8 3 19 2 8 2 8 2 8 2 2 2 8 2 8 3 19 2 8 8 8 \*LD IY1, IY1 LD L, (IY+r8) \*LD IYh,C \*LD IYh,D \*LD IYh,A \*LD IY1,B \*LD IYh,B \*LD IYh,E \*LD IYh, IYh \*LD IYh, IYl LD H, (IY+r8) \*LD IY1,C \*LD IY1,D \*LD IY1,E \*LD IY1, IYh \*LD IY1,A 2 8 2 8 6x 2 8 2 8 2 8 2 8 2 8 2 8 3 19 2 8 2 8 2 8 2 8 2 8 3 19 2 8 \*LD A,A LD (IY+r8),B LD (IY+r8),C LD (IY+r8),D LD (IY+r8),E LD (IY+r8),H LD (IY+r8),L \*HALT LD (IY+r8),A \*LD A,B \*LD A,C \*LD A,E \*LD A, IYh \*LD A, IYl LD A, (IY+r8) \*LD A,D 19 3 19 3 19 3 19 3 19 3 19 2 8 3 19 2 8 2 8 2 8 2 8 2 8 2 8 3 19 2 8 7 x 3 ADD A, ADC A, \*ADD A,B \*ADD A,E \*ADD A,C \*ADD A,D \*ADD A, IYh \*ADD A, IYl \*ADD A,A \*ADC A,B \*ADC A,C \*ADC A,D \*ADC A,E \*ADC A, IYh \*ADC A, IYl \*ADC A,A (IY+r8)(IY+r8)8x 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 2 8 8 2 8 2 8 3 19 3 19 SZYHXV0C SBC A, \*SBC A,D \*SUB B \*SUB C \*SUB D \*SUB E \*SUB IYh \*SUB IYl SUB (IY+r8) \*SUB A \*SBC A,B \*SBC A,C \*SBC A,E \*SBC A, IYh \*SBC A, IYl \*SBC A, A (IY+r8)9x 2 8 2 8 2 8 2 8 2 8 3 19 2 8 2 8 2 8 2 8 2 8 2 2 2 8 3 19 SZYHXV1C \*AND B \*AND C \*AND D \*AND E \*AND IYh \*AND IYl AND (IY+r8) \*AND A \*XOR B \*XOR C \*XOR D \*XOR E \*XOR IYh \*XOR IY1 XOR (IY+r8 \*XOR A Ax 2 8 2 8 2 8 2 8 2 8 2 8 2 8 3 19 2 8 2 8 2 8 2 8 2 8 2 8 3 19 SZY1XP00 \*OR B \*OR C \*OR D \*OR E \*OR IYh \*OR IYl OR (IY+r8) \*OR A \*CP B \*CP C \*CP D \*CP E \*CP IYh \*CP IY1 CP (IY+r8) \*CP A 2 8 2 8 2 8 2 8 2 8 2 8 2 8 3 19 2 8 2 8 2 8 2 8 2 8 2 8 3 19 2 8 Bx SZY1XP00 SZY1XP00 SZY1XP00 SZY1XP00 SZY1XP00 SZY1XP00 SZY1XP00 SZY1XP00 SZYHXV1C SZYHXV1C SZYHXV1C SZYHXV1C SZYHXV1C SZYHXV1C SZYHXV1C SZYHXV1C \*CALL Z,a16 \*CALL a16 \*RET NZ \*JP NZ,a16 \*CALL NZ,a16 \*PUSH BC \*ADD A,d8 \*ADC A,d8 \*RST 08H \*POP BC \*JP a16 \*RST 00H \*RET Z \*RET \*JP Z,a16 PREFIX FDCB Cx 15/9 14 14 14 21/14 15 3 11 2 15 15/9 14 14 X X 21/14 21 3 11 2 15 SZYHXV0C SZYHXV0C \*RET NC \*POP DE \*JP NC,a16 \*OUT (d8),A \*CALL NC,a16 \*PUSH DE \*SUB d8 \*RST 10H \*RET C \*EXX \*JP C,a16 \*CALL C,a16 \*PREFIX DD \*SBC A,d8 \*RST 18H \*IN A, (d8) 2 15/9 21/14 Dx 2 14 3 15 2 15 3 11 2 15 2 15/9 2 8 4 14 3 15 21/14 3 11 2 15 14 SZYHXV1C SZYHXV1C \*PREFIX ED \*RST 20H CALL PE, a16 \*RET PO POP IY \*JP PO,a16 \*CALL PO,a16 PUSH IY \*AND d8 \*RET PE JP (IY) \*JP PE,a16 \*EX DE,HL \*XOR d8 \*RST 28H EX (SP), IY 21/14 2 8 2 8 2 15/9 2 14 2 15 3 11 2 15 2 15/9 4 14 4 21/14 X X 3 11 2 15 Ex 4 14 2 23 SZY1XP00 SZY1XP00 \*DI \*CALL P,a16 LD SP, IY \*PREFIX FD \*RET P \*POP AF \*PUSH AF \*OR d8 \*RST 30H \*RET M \*JP M,a16 \*EI \*CALL M,a16 \*RST 38H \*JP P,a16 \*CP d8 Fx 2 15/9 2 14 4 14 2 21/14 2 15 11 2 15 15/9 2 10 4 14 2 21/14 X X 3 11 2 15 SZYHXPNC SZY1XP00 SZYHXV1C **Prefix FDCB** x3 x1 x2 x5 **x**7 x8 x9 хA хC хD хE хF $\mathbf{x}\mathbf{0}$ x4 **x6** хB \*RLC E \*RLC IYh \*RRC B \*RRC D \*RLC B \*RLC C \*RLC D \*RLC IY1 RLC (IY+r8) \*RLC A \*RRC C \*RRC E \*RRC IYh \*RRC IYl RRC (IY+r8) \*RRC A 3 12 3 12 3 12 3 12 3 12 3 12 0x 3 12 3 12 3 12 3 12 3 12 3 12 4 23 3 12 3 12 4 23 SZY0XP0C \*RR A \*RL B \*RL C \*RL D \*RL E \*RL IYh \*RL IY1 RL (IY+r8) \*RL A \*RR B \*RR C \*RR D \*RR E \*RR IYh \*RR IYl RR (IY+r8) 1x 3 12 3 12 3 12 3 12 3 12 3 12 4 23 3 12 3 12 12 3 12 3 12 3 12 23 3 12 3 12 SZY0XP0C \*SLA B \*SLA C \*SLA D \*SLA E \*SLA IYh \*SLA IYl SLA (IY+r8) \*SLA A \*SRA B \*SRA C \*SRA D \*SRA E \*SRA IYh \*SRA IYl SRA (IY+r8) \*SRA A 3 12 2x 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 3 12 3 12 4 23 3 12 3 12 12 3 12 SZY0XP0C \*SLL B \*SLL C \*SLL D \*SLL E \*SLL IYh \*SLL IYl SLL (IY+r8) \*SLL A \*SRL B \*SRL C \*SRL D \*SRL E \*SRL IYh \*SRL IY1 SRL (IY+r8) \*SRL A 3 12 3 12 3 12 3 12 3x 3 12 4 23 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 3 12 SZY0XP0C BIT 1, BIT 0, \*BIT 0,B \*BIT 0,C \*BIT 0,D \*BIT 0,E \*BIT 0, IYh \*BIT 0, IYl \*BIT 0,A \*BIT 1,B \*BIT 1,C \*BIT 1,D \*BIT 1,E \*BIT 1, IYh \*BIT 1, IYl \*BIT 1,A (IY+r8)(IY+r8)4x3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 20 4 20 SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-BIT 2, BIT 3, \*BIT 2, IYl \*BIT 2,B \*BIT 2,C \*BIT 2,D \*BIT 2,E \*BIT 2, IYh \*BIT 2,A \*BIT 3,B \*BIT 3,C \*BIT 3,D \*BIT 3,E \*BIT 3, IYh \*BIT 3, IYl \*BIT 3,A (IY+r8)(IY+r8)5x 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-BIT 4, BIT 5, \*BIT 4, IY1 \*BIT 4,B \*BIT 4,C \*BIT 4,D \*BIT 4,E \*BIT 4,IYh \*BIT 4,A \*BIT 5,B \*BIT 5,C \*BIT 5,D \*BIT 5,E \*BIT 5, IYh \*BIT 5, IYl \*BIT 5,A (IY+r8)(IY+r8)6x 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 20 4 20 SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-BIT 6, BIT 7, \*BIT 6,B \*BIT 6,C \*BIT 6,D \*BIT 6,E \*BIT 6,IYh \*BIT 6, IYl \*BIT 6,A \*BIT 7,B \*BIT 7,C \*BIT 7,D \*BIT 7,E \*BIT 7, IYh \*BIT 7, IYl \*BIT 7,A (IY+r8)(IY+r8)7 x 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 20 4 20 SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-SZY1XU0-RES 0, RES 1, \*RES 0,E \*RES 0,A \*RES 1,C \*RES 0,C \*RES 0,D \*RES 0, IYh \*RES 1, IYh \*RES 1,A \*RES 0, IY1 \*RES 1, IY1 \*RES 0,B \*RES 1,B \*RES 1,D \*RES 1,E (IY+r8)(IY+r8)8x 3 12 12 3 12 12 3 12 3 12 3 12 3 12 3 12 12 3 12 3 12 3 12 3 12 4 23 4 23 RES 3, RES 2, \*RES 2,B \*RES 2,C \*RES 2,D \*RES 2,E \*RES 2, IYh \*RES 2, IY1 \*RES 2,A \*RES 3,B \*RES 3,C \*RES 3,D \*RES 3,E \*RES 3, IYh \*RES 3, IY1 \*RES 3,A (IY+r8)(IY+r8)3 12 9x 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 4 23 RES 4, RES 5, \*RES 4,B \*RES 4,C \*RES 4,D \*RES 4,E \*RES 4, IYh \*RES 4, IYl \*RES 4,A \*RES 5,B \*RES 5,C \*RES 5,D \*RES 5,E \*RES 5, IYh \*RES 5, IYl \*RES 5,A (IY+r8)(IY+r8)3 12 3 12 3 12 Ax 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 4 23 \_\_\_\_\_ \_\_\_\_\_ \_\_\_\_\_ RES 7, RES 6, \*RES 6,B \*RES 6,C \*RES 6,D \*RES 6,E \*RES 6, IYh \*RES 6,A \*RES 7,B \*RES 7,C \*RES 7, D \*RES 7,E \*RES 7, IYh \*RES 6, IYl \*RES 7, IYl \*RES 7,A (IY+r8)(IY+r8)Bx 3 12 3 12 3 12 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 4 23 \_\_\_\_\_ SET 0, SET 1, \*SET 0,C \*SET 0,D \*SET 0,E \*SET 0, IY1 \*SET 1,D \*SET 0,B \*SET 0, IYh \*SET 0,A \*SET 1,B \*SET 1,C \*SET 1,E \*SET 1, IYh \*SET 1, IYl \*SET 1,A (IY+r8)(IY+r8)3 12 3 12 Cx 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 4 23 4 23 SET 2, SET 3, \*SET 2,B \*SET 2,C \*SET 2,D \*SET 2,E \*SET 2, IYh \*SET 2, IYl \*SET 2,A \*SET 3,B \*SET 3,C \*SET 3,D \*SET 3,E \*SET 3, IYh \*SET 3, IY1 \*SET 3,A (IY+r8)(IY+r8)Dx 3 12 12 12 12 3 12 3 12 12 3 12 3 12 3 12 3 12 4 23 23 SET 5, SET 4, \*SET 4,D \*SET 4, IY1 \*SET 5, IY1 \*SET 4,B \*SET 4,C \*SET 4,E \*SET 4, IYh \*SET 4,A \*SET 5,B \*SET 5,C \*SET 5,D \*SET 5,E \*SET 5, IYh \*SET 5,A (IY+r8)(IY+r8)3 12 12 3 12 3 12 3 12 Ex 3 12 3 12 3 12 3 3 12 3 12 3 12 3 12 3 12 3 12 4 23 23 SET 6, SET 7, \*SET 6,B \*SET 6,C \*SET 6,D \*SET 6, IYh \*SET 6, IYl \*SET 7,B \*SET 7,C \*SET 7,D \*SET 7,E \*SET 7, IYh \*SET 7, IYl \*SET 6,E \*SET 6,A \*SET 7,A (IY+r8)(IY+r8)3 3 12 Fx 3 3 12 3 12 3 12 3 12 12 3 12 3 12 3 12 3 12 3 12 3 12 3 12 12 4 23 4 23 Prefix Group 8-Bit Load Group 16-Bit Load Group Exchange, Block Transfer, Search Group 8-Bit Arithmetic and Logical Group Duration of conditional calls and returns is different when action is General-Purpose Arithmetic and CPU Control Group INS reg ← Instruction mnemonic taken or not. This is indicated by two numbers separated by "/". The ← Duration in cycles 16-Bit Arithmetic Group Length in bytes → 2 8 higher number (on the left side of "/") means duration of instruction Rotate and Shift Group SZYHXPNC ← Flags affected when action is taken, the lower number (on the right side of "/") Bit Set, Reset and Test Group means duration of instruction when action is not taken. Jump Group Call and Return Group Input and Output Group Undocumented Instructions (not useful aliases) Flags affected are always shown in S Z Y H X P/V N C order. If flag is marked by "0" it means it is reset after the instruction. If it is marked by "1" it is set. If it is marked by "-" it is not changed. If it is marked by "S", "Z", "Y", "H", "X", "P/V", "N" or "C" corresponding flag is affected as expected by its function. Flag P/V behaves like even parity flag when marked "P" and like overflow flag when marked "V". Undocumented instructions are marked by \* in front of the their name. If they are useful they are put into particular instruction group marked by cell background color, if they are mere aliases for other instruction they are marked by grey background. In combinations of prefixes the only useful ones are DDCB and FDCB. DDED and FDCB and FDCB. prevails. d8 means immediate 8 bit data d16 means immediate 16 bit data **a16** means 16 bit address r8 means 8 bit signed data, which are added to program counter or index registers (IX or IY) Registers **Main register set:** Alternate register set: Flag register (F) bits: 15 ... 8 7 ... 0 7 ... 0 15 ... 8 F (flags) F' (flags) A (accumulator) A' (accumulator) C'В $\mathbf{C}$ B' E'D E D'**S** - Sign Flag H H' **Z** - Zero Flag I (interrupt vector) **Y** - Y Flag (undocumented) R (memory refresh) **H** - Half Carry Flag **X** - X Flag (undocumented) 15 ... 0 **P** - Parity / Overflow Flag IX (index register) IY (index register) **N** - Add / Substract Flag SP (stack pointer) **C** - Carry Flag

PC (program counter)