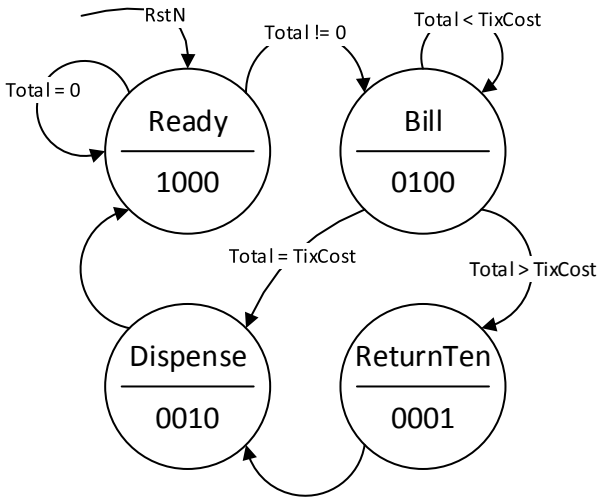
FSM State Transition Diagram



Notes: [1] State encodings chosen to correspond to state output

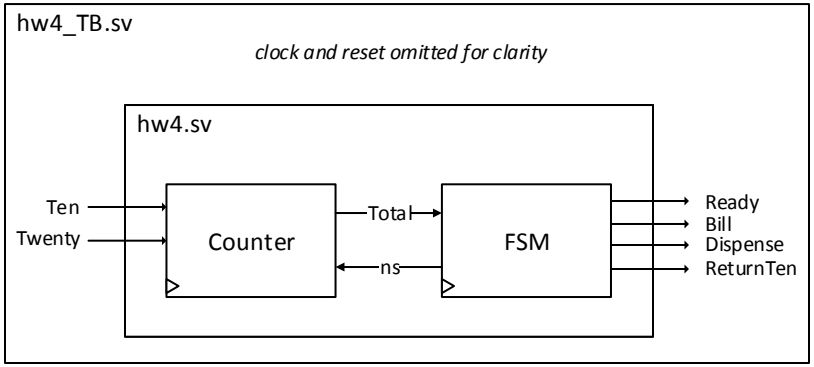
[2] Ouputs are in the form {Ready, Bill, Dispense, ReturnTen}

State Transition Table			
PS[1]	Total	NS	Outputs[2]
Ready	= 0	Ready	1000
	!= 0	Bill	1000
Bill	< TixCost	Bill	0100
	> TixCost	ReturnTen	0100
	== TixCost	Dispense	0100
ReturnTen	X	Dispense	0001
Dispense	X	Ready	0010

Design Assumptions:

There is an external controller responsible for generating valid inputs.
Inputs will never be asserted at the same time.
Inputs will only be asserted when either the Bill or Ready signals are also asserted.
Inputs should only be asserted for one clock cycle at a time: multi clocks = multi bills
Output signals need only be asserted for one clock cycle.

Block Diagram



All Valid Input Combinations for a Single Transaction

Circles show total

Lines show inputs