ECE 571
Introduction to SystemVerilog
Spring 2015
Homework 2

The primary objective of this this assignment is to re-acquaint you with sequential logic modeling in Verilog and to increase the level of complexity you address in your testbench.

Using the modules you created and verified in Homework 1 as a basis, create a module to perform 16-bit "staggered addition". Your module will accept two 16-bit addends along with a carry input and produce a 16-bit sum with a carry output.

The staggered add is a pipelined addition. During the first cycle, the input operands are captured in registers. In the second cycle, the least significant 8 bits of the operands are added. During the third cycle the most significant 8 bits of the operands are added, along with the carry out produced by the result of the previous addition. The results are stored in output registers during the fourth cycle.

Create a testbench to verify your staggered adder.

Correctness, clarity, reusability, and maintainability count.

Submit your Verilog code for your design modules and your testbench via D2L. Include a brief README file to indicate how the modules/testbench should be compiled and simulated.