ECE 571
Introduction to SystemVerilog
Spring 2015
Homework 1

The primary objectives for this assignment are to:

- Ensure you can use a System Verilog tool set – either that provided on the PSU MCECS computing environment or one that you're able to access at work or at home

- Reacquaint you with simple combinational logic modeling in Verilog

Create a behavioral dataflow style combinational model for a 4-bit expandable carry lookahead adder along with a testbench to thoroughly verify your model. Recall that a behavioral dataflow model uses only continuous assignment statements. Model your design to have a propagation delay of 5ns. Use the design outlined in class.

Using the 4-bit adder module you created and verified, create an expandable 8-bit adder and thoroughly verify it.

Correctness, clarity, reusability, and maintainability count.

Submit your Verilog code for both design modules and your testbenches, via D2L. Include a brief README file to indicate how the modules/testbench should be compiled and simulated.