Team 10

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FPGA Clapping Pattern Detector

Critical Design Review

Goal:

Detect and reject certain clapping patterns and provide visual feedback.

Outline

- Results of architecture alternatives (3 slides)
- Updated architecture block diagram (3 slides)
- Next steps: plan for final design review (2 slides)
- Schedule progress: milestones/risks met (1 slides)
- Percentage of work completed by each member (1 slide)

Results of Architectural Alternatives - Clap Detection

Clap detection design choices:

- Threshold is minimal area
- Filters require multiplication which increases area rapidly

Final Design Choice:

- Automatic thresholding by comparing with moving average
- Checking for sudden high amplitudes
- Removing false positives by thresholding on number of samples

Reason:

- Smaller area

Results of Architectural Alternatives - Min not zero

Min_not_zero design choices:

- Recursively instantiated comparison tree, comparing two at a time (faster)
- Two at a time until checked entire bank (slower, less area)

Final Design Choice:

- Two at a time is less area, time is not important with a MHz clock compared to millisecond human clapping time

Reason:

- Smaller area

Results of Architectural Alternatives - Pattern Checker

Pattern match checker design choices:

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Final Design Choice:

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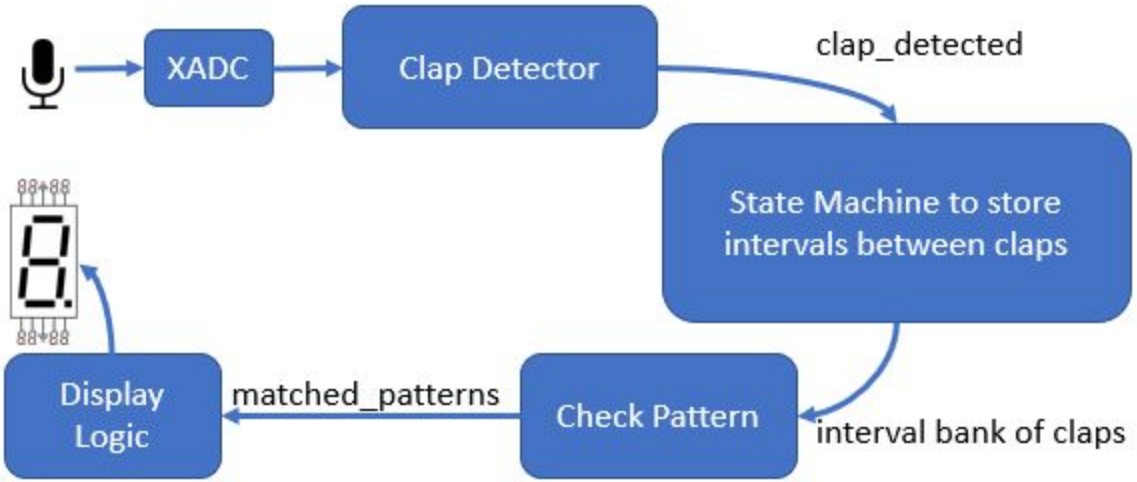
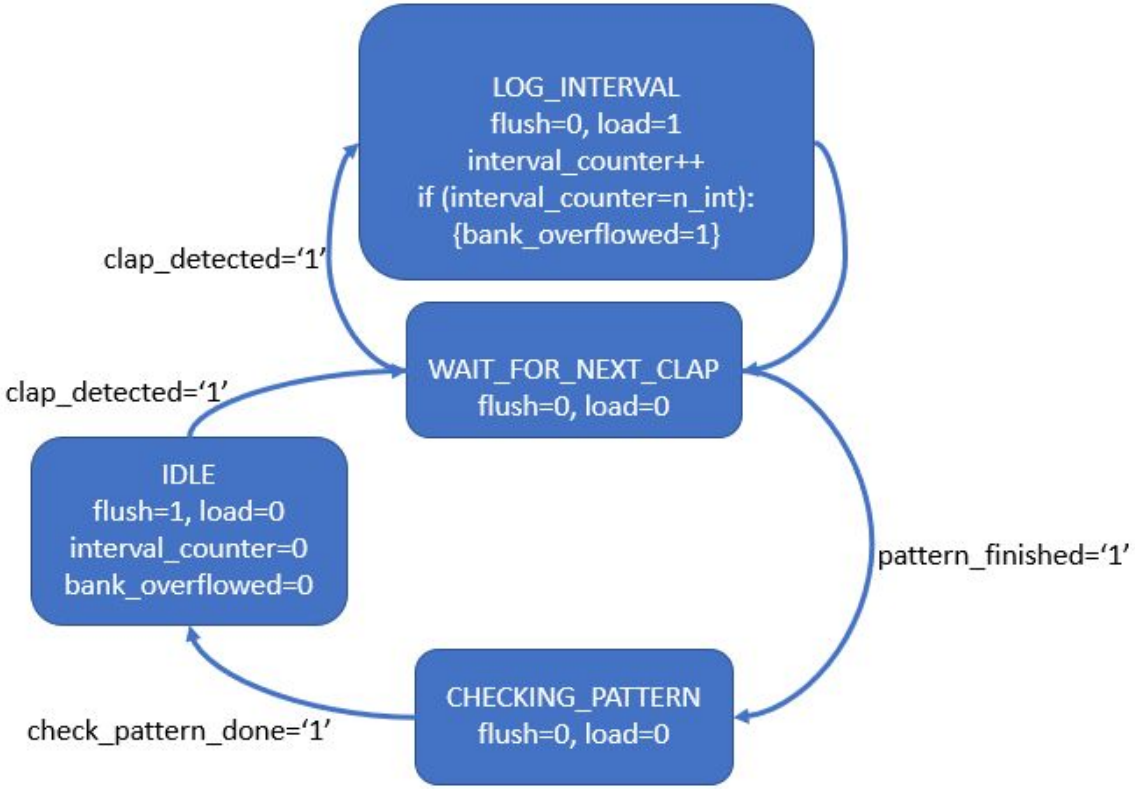
Reason:

- Smaller area

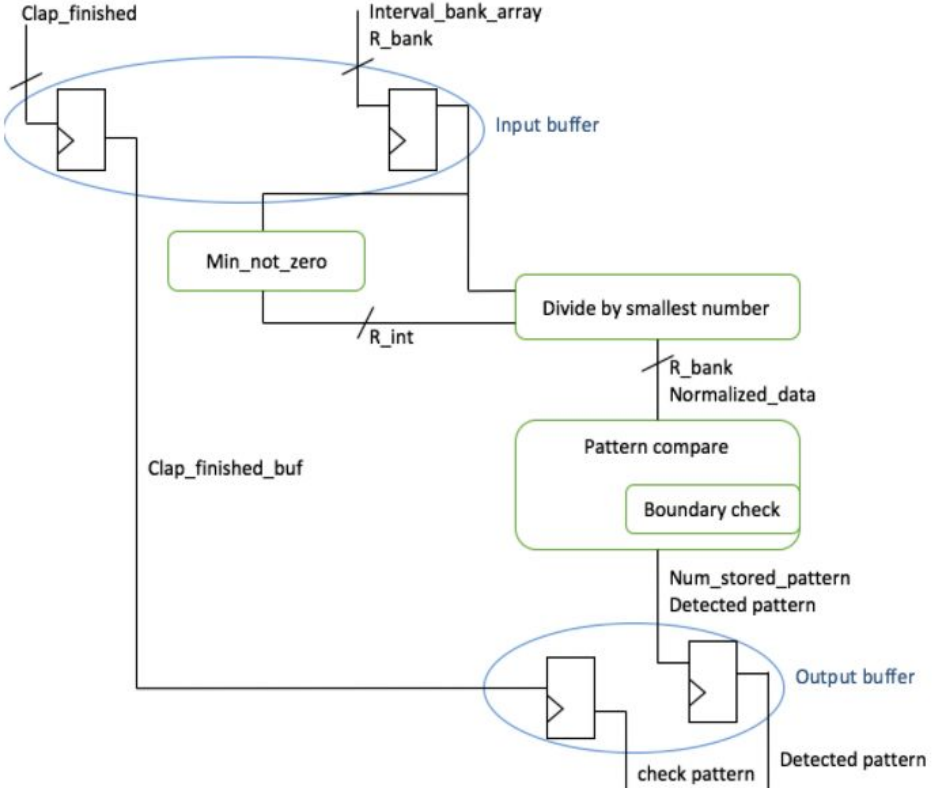
Updated Architecture - Top Level



Updated Architecture - State Machine



Updated Architecture - Checking Pattern



Final Design Review Plan

- Finish high level modules that instantiate the individual modules
- Test out full pattern checking system w/ testbench
- Integrate microphone & clap detector with LED shift register visual feedback and program Basys3 to test

Final Design Review Plan

- Integrate state machine and pattern checking into previous design for a full system test
- Program final design on Basys3 board
- Try out different clap patterns
- tune/adjust for human error and microphone error

Schedule Progress

Finished all individual modules except:

- clap_detector VHDL implementation
- Min_not_zero
- Divide_by_min (normalization)

Next up is integration

Individual Member Work Completion

Team member	Progress	Still Needed
Will	divider, finished 7-segment controller	Testbench divider, integrate 7-seg display control with state machine
Philip	Finished shift register & testbench, finished state machine & testbench	Assist & integrate other modules into higher level diagrams
Matt	Finished single pattern check & testbench	Pattern storage, Check with all stored patterns
Vasundhara	Implemented clap detection algorithm, wrote test bench for it in Python	Implementation in VHDL, optimization

Questions?