FPGA Clapping Pattern Detector

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Description:

The design will parse a stream of audio samples taken from a microphone fed into an analog input to a Basys3 FPGA. The main goal is to detect and reject certain clapping patterns and display visual feedback based on the pattern detected.

Preliminary Design Ideas:

Visual Feedback:

A LED will be lit every time a clap is detected.
After a period of no detected claps (T_SILENCE= 2 seconds), the pattern will be processed and display visual feedback via LEDs and 7-segment display (sseg):

- If the pattern is valid, the pattern number (0-F) will be displayed on the leftmost sseg, while the other three ssegs will be off. (ex: “ “)
- If the pattern is not valid, all four 7-segment displays will display F’s (“FFFF”)
- During the process of detecting a pattern all 7-segment displays will be off. (“ “)
- The last detected pattern message (or invalid pattern message) will still be displayed during idle until the next clap pattern begins.

Pattern Detection:

- Upon the first clap, the processor goes into a state where it records the time between successive claps until more than T_SILENCE occurs and counts the number of claps (Max clap pattern length: 32 time periods)
- Combinational logic is attached to the registers storing the time between claps to calculate if they match a valid clap pattern (maybe pipeline this)
    - details on this are still being discussed but will probably be based on measuring the “rate” (least common multiple of the intervals?) of the clap and then using that to decode the pattern

Bonus (if time allows):

- Add a new state to allow user to record valid clap patterns and be stored on the FPGA.
- Train a small neural net to replace(replicate?) the clap detection by just amplitude

Deliverables:

- Test pattern detection procedure (using a higher level language such as Python)
- Use VHDL to detect peak amplitudes from a clap and light an LED
- Log time between claps and periods of silence (probably use a counter)
- Use VHDL to implement sseg display feedback (probably a state machine)
- Use VHDL for pattern detection procedure (combinational logic, might pipeline if needed)
- Demonstration/video of clapping a valid pattern and it’s number being displayed