We have uploaded a list of Projects from which you could make a selection. One person from each team will send me a mail indicating Choice #1,2 and 3 for their project. We want to evenly distribute the projects. If you already have a topic, please send me a mail with a brief description of the project. The deadline for this is **10/22/2017 11:59 pm.**

We will choose a topic for you based on your selections. Obviously, we cannot guarantee that you will get your first choice. You will also be given a team number.

Also, keep in mind that at each stage, we might select a couple of teams to present their progress. This will not be graded.

After the topics are finalized, there will be four stages in the Project. Assignments will be created on T-Squares corresponding to all the four milestones.

1. **Abstract: Deadline => 11/2/2017**
   Submit a Document which includes the Project Title and Team Members. Also, include the team number. The document should list the deliverables of your project. Note that the topics are of varying difficulty and will be graded accordingly. You should choose your topics (while providing the 3 choices) based on your confidence, interests and feasibility of the projects. The degree of completion will also be considered while grading. So, it is fine even if you choose an easy topic and finish it to the maximum extent possible. Note that this part of the project will not be graded. We will use the deliverables in this report for grading of the subsequent stages. Only one team member must submit the abstract. Since the topics that we have provided are broad, you can select the features that you would like to implement in your project.
2. **Preliminary Design Review: Deadline 11/9/2017 ;25% of Grade**
   For the second stage, you must submit a Presentation which should include the following
   i. Project Title and Team Members
   ii. Project Team Number
   iii. Project Code Functionality and Description of individual Components (1-2 Pages)
   iv. Optimizations you plan for any sub-systems if applicable (1-2 Pages)
   v. Timeline for the Project and Work Assignments for each team member (1 Page)
   vi. How does the team member plan to complete his or her tasks (1 page) Risks and Plans taken to mitigate them (1 page).
   vii. Description of Prior work by Others in the area and excerpts from their results. (3 pages) – Cite the full references.
   viii. Your expected results. (1-2 pages)

   Also, Attach a zip folder for the VHDL files and testbench. It is fine if you have not completed the code yet. You should also submit the reference design/files used by the testbench for comparison. The reference design could be in C or Matlab or any higher level. The test vectors and other relevant details should also be provided in the zip folder. Only one member of the team should upload the presentation and zip folder.

3. **Critical Design Review: Deadline 11/16/2017 ;35% of Grade**
   For the third stage, you must submit a Presentation which should include the following
   i. Results of architectural alternatives - area, throughput (3-4 pages of description).
   ii. Chip architecture/memory design if applicable (2-3 pages).

iii. Plan for Final Design Review (2-3 pages)
iv. Schedule, Milestones & Status/Risks Met. (1-2 pages).
v. Identify the percentage of the assigned work that has been completed by each member.

The submission should contain a zip folder which includes VHDL files and testbench with the updated higher-level design files. The ZIP Folder should also include test vectors and screenshots showing verifications/simulations.

Only one member of the team should upload the presentation and zip folder.

4. **Final Presentation: 40% of Grade Deadline 11/30/2017; 40% of Grade**

For the fourth stage, you must submit a Presentation which should include the following

i. Final Design Architecture (1-2 pages)
ii. Code Components (2 pages)
iii. Test Vectors
iv. Integration and Test Results (Functional & Timing) -4-5 pages describing process and results
v. Details about the throughput and the maximum frequency the design can be run at.
vi. Area, Power and Timing Details.
vii. Details about FPGA implementation – 2 pages
viii. Lessons Learned.
ix. Identification of contributions by team member in the project. How much work was done by each member and what was his/her major contribution?

For the Final Phase of your project, you should also submit a report which contains the Project Title, Names of the Project Members, Introduction of the Topic, Architecture, Implementation Battles, Work Distribution, Details about the test bench, Functional simulation Results, Area and Power results and finally an appendix which includes all the codes (Design, Testbench and Higher-Level Code). Only one member of the team should upload the report and the presentation. For the Final Phase, we will have presentations from all the teams along with project demos.