Three-Phase Dual Active Bridge Converter Design Considerations

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***Abstract* — In three-phase dual-active-bridge (DAB) converter, the zero-voltage-switching (ZVS) range, DC capacitor ripple current and converter efficiency are significantly impacted by the selectable system parameters, including transformer turn ratio n, switching frequency f and leakage inductance L_k. The converter performance also varies with different operation conditions, i.e., input voltage, output voltage and output power level. Therefore, these parameters need to be carefully selected to achieve optimized performances. In this paper, a comprehensive study of the parameter selection for the three-phase DAB converter is conducted under different operation conditions. A new parameter fL is defined to reduce the analysis from 3 dimensions to 2 dimensions, which simplifies the analysis of transformer turn ratio significantly. Furthermore, the effective operating area (EOA) of f and L_k are defined for feasible transformer designs. The current stress of switches and DC capacitors are studied in the EOA to help determine the range of f and L_k. Finally, the converter total loss and efficiency are analyzed at full and half load with different input and output voltages. The converter parameter (n, f, L_k) can be selected using ZVS and efficiency criteria. The tradeoff between high efficiency, wide ZVS area and low capacitor ripple current can be achieved accordingly.**

***Keywords*—Effective operating area; planar transformer; three-phase DAB converter; zero voltage switching.**

I. INTRODUCTION

In recent years, the bidirectional dual-active-bridge (DAB) converter becomes attractive in electric vehicle and hybrid electric vehicle applications because of its bidirectional power flow, galvanic isolation, high efficiency, and zero-voltage-switching (ZVS) [1], [2]. It is also widely used in energy storage system, DC power distribution system and smart grids [3], [4]. Compared to single-phase DAB converter, three-phase DAB converter has higher power capability and lower ripple current on both input and output side, which leads to lower capacitor volume and thus higher power density [5], [6].

Fig. 1 illustrates the basic configuration of a three-phase DAB converter [5]. A three-phase high frequency transformer or three single-phase transformers are connected between the AC link of two three-phase active bridges. Three symmetrical inductors (corresponding to the leakage inductance L_k) connected on the high voltage (HV) side of the converter are used for power transfer between primary and secondary side.

Phase shift modulation is the commonly used strategy for DAB converter, and it shows good performance at nominal operating condition. However, in practice, the DC link voltage may vary with the batteries connected on low voltage (LV) and/or HV side of the converter. When the voltage ratio between primary and secondary side mismatches the transformer turn ratio, hard switching may occur and lead to excessive switching loss, especially at partial load.

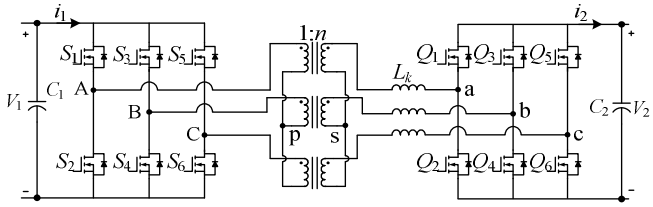

Fig. 1 Schematic of three-phase DAB converter.

For single-phase DAB converter, advanced modulation strategies have been proposed to overcome the drawback of phase shift modulation, including extended-phase-shift [7], dual-phase-shift [8] and phase-shift plus pulse-width-modulation [9]. These advanced modulations require phase shift between the two half bridges in the same H-bridge, and thus the duty cycle of the AC voltage applied to the transformer can be controlled lower than 50%. In three-phase DAB converter, however, each phase has one half bridge, and the phase shift between three phases are fixed at 120°, which makes the advanced modulation strategies not applicable. Other improvements about the three-phase DAB are also studied recently. For example, in [10] and [11], the application of six-leg half bridges on the primary side enables variable duty cycle control. In [12], asymmetrical duty cycle control between upper and lower switches is proposed to introduce triangular and trapezoidal current mode into the converter, which helps extend soft switching range at light load and large voltage variations. Nevertheless, they increase the complexity of hardware topology or transition control among different operation modes, which is less desired in industry applications.

The behavior of DAB converter varies under different operating conditions (corresponding to different LV and HV DC voltage and output power level), and they should be considered when designing a DAB converter. The converter behavior is determined primarily by the parameters of the converter, including transformer turn ratio n, switching frequency f, and leakage inductance L_k. Some optimization methods have been proposed and applied to single-phase DAB converter. For example, the selectable parameters (f, n) or (f, L_k) are studied in [13], [14] to achieve the tradeoff between converter efficiency and volume. In this paper, a comprehensive study of the impact of all the selectable parameters (n, f, L_k) on three-phase DAB performances, including ZVS range, converter efficiency and capacitor ripple

current, are conducted. It provides a comprehensive parameter selection guideline for the three-phase DAB converter design.

II. Operating Principle of Three-Phase DAB Converter

During operation, six-step line-to-neutral voltages are applied on both side of the transformer. Due to the phase shift ϕ between primary and secondary side, the voltage difference across L_k enables power transfer. The corresponding voltage and current waveforms are shown in Fig. 2. Since the operating waveform is symmetrical in both directions [15], this paper only considers power transfer from primary to secondary side (P > 0). When $\phi \le \pi/3$, the relationship between the phase shift and transferred power is given as

$$P = \frac{nV_1V_2}{12\pi^2 fL_k}\cdot\phi(4\pi - 3\phi) \tag{1}$$

From (1), the output power increases with phase shift ϕ. At a desired power P, ϕ can be calculated as (2). Detailed analysis and expressions of $\pi/3 < \phi \le 2\pi/3$ can be found in [14].

$$\phi = \frac{2\pi}{3}\left(1 - \sqrt{1 - \frac{9fL_kP}{nV_1V_2}}\right) \tag{2}$$

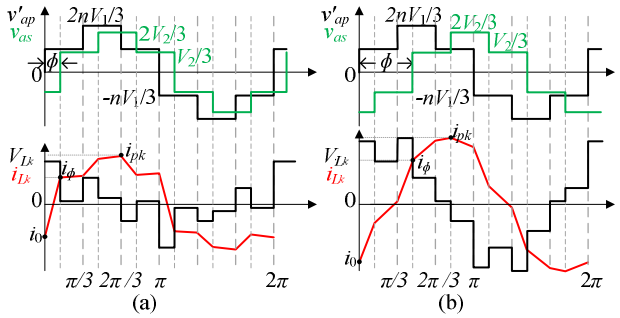

Fig. 2 Operating waveforms of three-phase DAB converter: (a) $\phi \le \pi/3$, (b) $\pi/3 < \phi \le 2\pi/3$.

In this paper, a three-phase DAB converter is designed as an example, and the specifications are listed in Table I.

Table I Specifications of the three-phase DAB converter

Primary DC voltage (LV)	V_1	48 V (42 - 60 V)
Secondary DC voltage (HV)	V_2	400 V (350 - 450 V)
Maximum power	P_N	10 kW

III. Key Influence of Turn Ratio

The parameters f and L_k have a common influence on the converter performance. In this paper, a new parameter fL is defined to simplify the analysis. The impacts of n and fL on the ZVS boundary, RMS current and ripple current are studied, respectively.

$$fL = f \cdot L_k / fL_{base} \tag{3}$$

where, $fL_{base} = 7n_{\max}V_{1\min}V_{2\min}/72P_N$, $n_{\max} = 11$.

The converter needs to operate in a wide voltage and power range. To reduce computation efforts, 3 different LV side voltages, 3 HV side voltages and 2 different power ratings are chosen to represent different operation conditions.

$$\vec{V_1} = [42,\ 48,\ 60]^T \text{ V},\ \vec{V_2} = [350,\ 400,\ 450]^T \text{ V},\ \vec{P} = [5,\ 10]^T \text{ kW}$$

A. ZVS *Boundary*

ZVS turn-on can be achieved when the anti-paralleled diode is conducting [15], [16], which correspond to negative current i_0 and positive current i_ϕ in Fig. 2.

$$\begin{aligned} i_0 &= \frac{2(V_2 - nV_1) - 3V_2\phi/\pi}{18fL} \le 0 \\ i_\phi &= \frac{2(V_2 - nV_1) + 3nV_1\phi/\pi}{18fL} \ge 0 \end{aligned} \tag{4}$$

At full load, ZVS is desired at any combination of V_1 and V_2. In order to find the worst case that limits ZVS area, maximum value of i_0 and minimum value of i_ϕ among all the 9 combinations of V_1 and V_2 are considered. Substituting (2) into (4), the partial derivative of i_0 and i_ϕ with respect to V_2 or V_1 are given as (5).

$$\begin{aligned} \frac{\partial i_0}{\partial V_2} &= \frac{2 - 9fLP/nV_1V_2}{18fL\cdot\sqrt{1 - 9fLP/nV_1V_2}} > 0 \\ \frac{\partial i_\phi}{\partial V_1} &= -\frac{n\cdot(2 - 9fLP/nV_1V_2)}{18fL\cdot\sqrt{1 - 9fLP/nV_1V_2}} < 0 \end{aligned} \tag{5}$$

From (5), i_0 increases monotonically with V_2, and the maximum value of i_0 happens at $V_{2\max}$ (= 450 V); i_ϕ decreases monotonically with V_1, and the minimum value of i_ϕ happens at $V_{1\max}$ (= 60 V). A visualized solution of the ZVS condition of LV bridge is solved at different V_1 with $V_2 = V_{2\max}$; similarly, the HV bridge ZVS condition is solved at different V_2 with $V_1 = V_{1\max}$. The results are shown in Fig. 3, where the feasible range of n and fL which guarantees ZVS is highlighted. Therefore, the optional value of turn ratio n is 7 or 8.

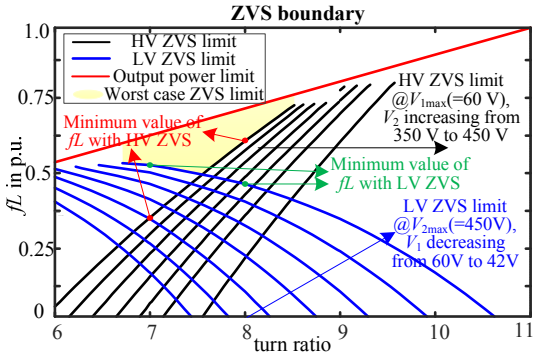

Fig. 3 LV and HV ZVS boundary at different V_1 and V_2.

B. RMS *current*

At full load, the averaged RMS current of switches I_{rms_sw} at 9 voltage combinations are studied with respect to n and fL, and the results are demonstrated in Fig. 4. According to Fig. 4, at fixed turn ratio n, as fL increases, the RMS current decreases first and reaches a minimum value, but the RMS current increases back as fL approaches its maximum. With fixed fL, the averaged RMS current is slightly higher when n = 7.

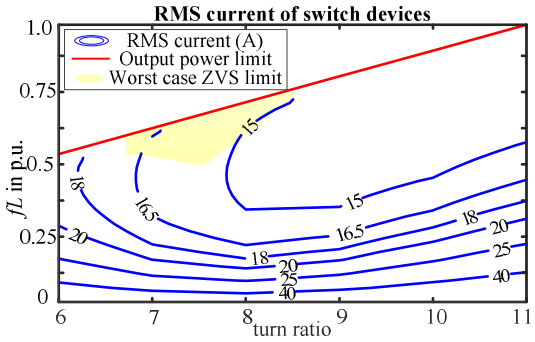

Fig. 4 Averaged RMS current at different n and fL under full load.

C. Ripple Current of DC Link Capacitor

The DC link capacitors smooth DC link voltage and absorb the ripple current. The design of the capacitor is based on the maximum ripple current at all voltage conditions. The RMS values of the capacitor ripple current are calculated by

$$I_{rms\_c1}=\sqrt{I_{rms1}^2-I_{DC1}^2},\ I_{rms\_c2}=\sqrt{I_{rms2}^2-I_{DC2}^2} \tag{6}$$

where, I_{rms1} and I_{rms2} are the RMS values of the input current i_1 and output current i_2, as shown in Fig. 1, the average values of i_1 and i_2 are calculated as $I_{DC1} = P/V_1$, $I_{DC2} = P/V_2$. Details of how to calculate I_{rms_sw}, I_{rms1} and I_{rms2} can be found in [14].

For given values of (n, fL), the maximum ripple current of LV and HV side are computed under different input and output voltages. The results are illustrated in Fig. 5. At a given turn ratio n, the ripple current on both side decreases as fL increases. The minimum value is approached as fL approaches its maximum, which is limited by the power rating. When n = 7, lower current ripple is achieved on the LV side; when n = 8, lower current ripple is achieved on the HV side.

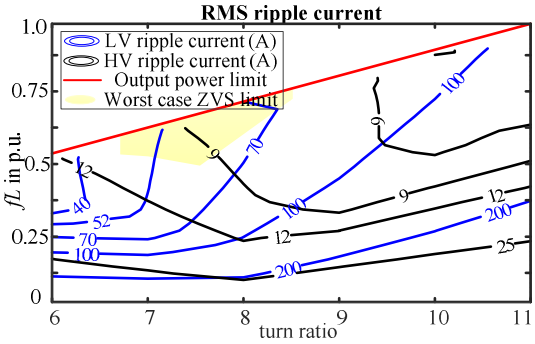

Fig. 5 Worst case LV and HV ripple current at different n and fL.

In summary, when n = 7, wider HV side ZVS range and lower LV side capacitor ripple current are achieved; when n = 8, wider LV side ZVS range and lower HV side ripple current are achieved. Additionally, the average RMS current of the switches and transformers is also lower when n = 8.

IV. Effective Operating Area

A. EOA Limited by Transmission Power

The upper limit of fL is specified by (3) to ensure the maximum power capability, i.e.

$$f\cdot L_k \le \frac{7\cdot n\cdot V_{1\min}V_{2\min}}{72P_N} \tag{7}$$

The power constraint is illustrated by the red hyperbolic curve in Fig. 6 (a) and (b) respectively, corresponding to n = 7 and 8. The feasible range of f and L_k that meets the power requirement locates on the left side of the power limit curve.

B. EOA Limited by Transformer design

The transformer power capability is usually estimated by area product (AP) method [17]. In this design, planar core E64 with material N87 from EPCOS is selected and three single-phase transformers with 4.2 kVA rating each are needed. The transformer design is usually constrained by maximum flux density $B_{\max}$, core loss density $p_{v\max}$ and current density J, which are given in (8) – (10).

$$B_m=\frac{V_1}{9fA_e}\le B_{\max} \tag{8}$$

$$p_v=Kf^{\alpha}B_m^{\beta}\le p_{v\max} \tag{9}$$

$$A_s=\frac{I_{rms\_tf}}{J}\le A_w\cdot K_u/2 \tag{10}$$

where A_w and A_e are the core window area and effective area, A_s is the cross section of designed winding. The core loss coefficient K, α, β can be obtained from datasheet, and $\alpha < \beta$.

To avoid influence of the voltage drop on the leakage inductor, the flux density is calculated by LV side voltage V_1 in (8). From (8) and (9), the turn ratio n has no impact on the flux density and core loss density constraint. However, the turn ratio n affects the transformer RMS current I_{rms_tf} in the current density constraint in (10), and the transmission power limit in (7). This results in difference of the EOA range at different n.

The effective operation areas of the transformers with turn ratio n = 7 and 8 are illustrated by the shaded area in Fig. 6 (a) and (b), respectively. It is observed that EOA is smaller when n = 7, due to the difference in transmission power limit.

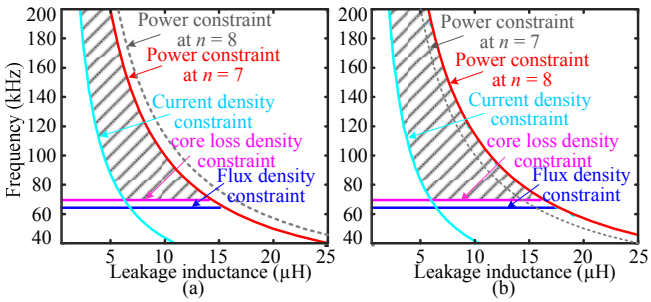

Fig. 6 EOA limited by transformer design at (a) n = 7 and (b) n = 8.

C. Switch and Capacitor Current Stress Analysis

The peak and RMS current of the switches are investigated under 9 different operating voltages, and the highest values are plotted in Fig. 7. Consistent with the analysis in section III B, the RMS and peak current decrease as the product of f and L_k increases, and the minimum values are achieved close to the power limit curve. It is also observed that n = 7 has slightly higher peak current and RMS current compare to n = 8. However, within the EOA, the difference is less than 10%.

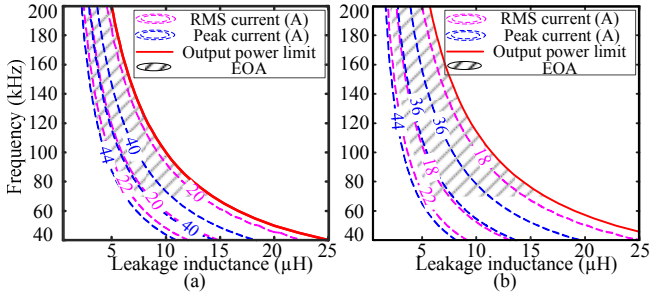

Fig. 7 Switch current stress analysis at (a) n = 7 and (b) n = 8.

By taking the maximum value of the ripple current among 9 operation voltages at full load, the ripple current contour at n = 7 and 8 are plotted in Fig. 8 (a) and (b), respectively. Corresponding to Fig. 5, the LV and HV ripple current decreases as the product of f and L_k increases and reaches a minimum as it approaches the power limit curve. From Fig. 8, when n = 7, the ripple current of LV side is much lower than n = 8, while the ripple current of HV side is slightly higher.

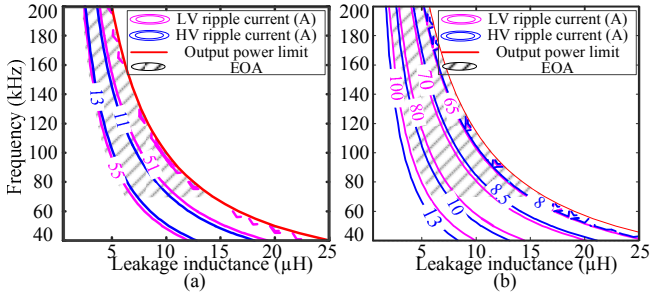

Fig. 8 Capacitor ripple current analysis at (a) n = 7 and (b) n = 8.

V. Main Losses and Converter Efficiency

From the analysis above, it is still difficult to justify the exact values of the parameters that feature better performance. Therefore, more detailed analysis of the converter efficiency is needed to determine the turn ratio n and values of f and L_k.

A. Power Loss of Switches

Conduction loss in power MOSFET can be calculated using the on-state resistance $R_{DS(on)}$ and the drain to source current i_D. The average conduction loss can be calculated by (11) [18]. In this case, the conduction loss generated by the body diode of the MOSFET is small enough to be neglected.

$$P_{cond} = \frac{1}{T}\int_0^T \left(R_{DS(on)} \cdot i_D^2\right) dt = R_{DS(on)} \cdot I_{rms\_sw}^2 \tag{11}$$

When the switches are not operated under ZVS condition, the switching loss cannot be neglected. The turn-on and turn-off losses in the MOSFET and its body diode can be calculated by linear approximation of the MOSFET switching process.

$$\begin{aligned} E_{onM} &= E_{onMi} + E_{onMrr} = U_{DS} I_{DSon} \cdot \frac{t_{ri} + t_{fu}}{2} + Q_{rr} U_{DS} \\ E_{offM} &= U_{DS} I_{DSoff} \cdot \frac{t_{ru} + t_{fi}}{2} \\ E_{onD} &\approx E_{onDrr} = \frac{1}{4} Q_{rr} U_{DS} \end{aligned} \tag{12}$$

where, t_{ri} (t_{ru}) and t_{fu} (t_{fi}) are the current (voltage) rise time and voltage (current) fall time during turn-on (turn-off) transition, respectively, Q_{rr} is the reverse recovery charge of the diode, U_{DS} is the DC voltage, E_{onM} and E_{offM} are the turn on and turn off energy loss of the MOSFET; and E_{onD} is the turn on energy loss of the body diode [18].

Therefore, the total switching loss in the MOSFET and the anti-paralleled diode are calculated by the product of switching energies and switching frequency, which is given by

$$P_{sw} = (E_{onM} + E_{onD} + E_{offM}) \cdot f \tag{13}$$

At full load, the total switching loss of 9 operating voltages are calculated. The switching loss at nominal condition (V_1 = 48 V, V_2 = 400 V) and two extreme cases (V_1 = 42 V, V_2 = 450 V and V_1 = 60 V, V_2 = 350 V) are given in Fig. 9 for n = 7 and 8. At nominal operating voltage (V_1 = 48 V, V_2 = 400 V), there is no switching loss within the entire EOA. When V_1 = 42 V, V_2 = 450 V, hard switching happens at LV side ((a), (b)), and the switching loss increases slowly when the operation area moves away from the power limit. However, when V_1 = 60 V, V_2 = 350 V, hard switching happens at HV side ((e), (f)), the switching losses are dramatically higher and increase with the switching frequency. Due to the significant high switching loss on HV side, it is obviously more important to achieve ZVS on HV side.

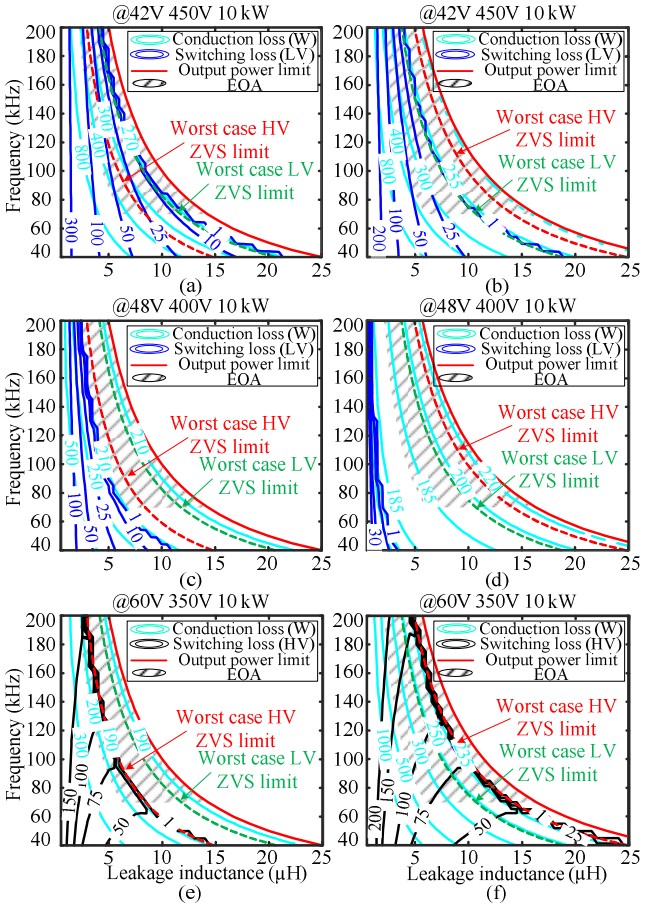

Fig. 9 Conduction and switching loss under 3 operating voltages at (a, c, e) n = 7 and (b, d, f) n = 8.

B. Transformer Loss

By substituting the flux density in (8) to (9), the core loss of three transformers can be calculated by

$$P_c = 3 \cdot K \frac{1}{f^{\beta-\alpha}} \left(\frac{V_1}{9A_e} \right)^{\beta} \cdot V_{core} \tag{14}$$

The transformer copper loss can be calculated by

$$P_w = 3 \cdot I_{rms\_tf}^2 \cdot R_{ac} \tag{15}$$

where R_{ac} is the AC resistance of the windings by taking eddy current effect into consideration [19].

The transformer losses under nominal operating voltage at n = 7 and 8 are shown in Fig. 10 (a) and (b), respectively. The core loss increases as f decreases, and it is independent of the turn ratio. The copper loss is proportional to the square of RMS current. Within EOA, the transformer total losses increases as f decreases, and don't change much with L_k. The losses at other operating voltages have similar trend, thus not given here.

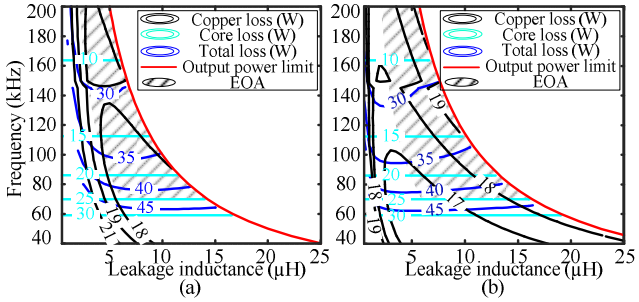

Fig. 10 Transformer losses under nominal voltage at (a) n = 7 and (b) n = 8.

C. Efficiency

Other losses in the converter such as DSP controller, gate driver and auxiliary inductor losses are much smaller and considered negligible. Therefore, the converter efficiency under different operating voltages are calculated and plotted in Fig. 11 and Fig. 12 corresponding to n = 7 and 8, respectively.

The efficiency analysis results of n = 7 under different voltage combinations are illustrated Fig. 11 (a, c, e) when the converter is fully loaded. The EOA can be divided into 2 sections by the ZVS boundary, and they are marked as **A1** and **A2**. In zone **A1**, ZVS is guaranteed on both LV and HV side and the ripple current is lower than 51 A. In zone **A2**, ZVS is achieved on HV side while hard switching happens on LV side. The ripple current is also higher (55 A) than zone **A1**. Though there are switching losses at the LV side, the converter losses are dominated by conduction loss of the switches. Zone **A2** has slightly higher efficiency compared to zone **A1**. The efficiency distribution is also analyzed at half load, which is depicted in Fig. 11 (b, d, f). At half load, the efficiency is slightly higher in zone **A1**. Hard switching happens on HV side and switching loss increases with frequency, which reduces the converter efficiency greatly at higher frequency (see as (f)).

The efficiency analysis results of n = 8 under different voltage combinations are illustrated Fig. 12 (a, c, e) when the converter is fully loaded. The EOA in Fig. 12 is divided into 3 sections by ZVS limit curve, and they are marked as **B1**, **B2** and **B3**. ZVS is realized on both side in zone **B1**, and LV ripple current is lower than 65 A. In zone **B2**, hard switching happens at HV side at some operating voltages and ripple current is up to 70 A. Zone **B3** is beyond the LV ZVS limit, where ZVS cannot be guaranteed on both LV and HV side. The highest efficiency may happen at zone **B3** (see as (a), (c)) when V_1 = 42 V, V_2 = 450 V and V_1 = 48 V, V_2 = 400 V, where ZVS is achieved at HV side. However, the ripple current is much higher (80 A or more), which results in larger capacitor volume. The efficiency increase is not significant in zone **B3** compared to zone **B1** and **B2**. When hard switching happens at HV side (see as (e)), much lower efficiency is observed in zone **B3**. At half load, if ZVS can be achieved on both side (see as (b, d)), the highest efficiency can possibly be achieved in all three zones. However, when V_1 = 60 V, V_2 = 350 V (see as (f)), the switching losses are much higher at half load. The highest efficiency is achieved in zone **B1** at relatively lower frequency.

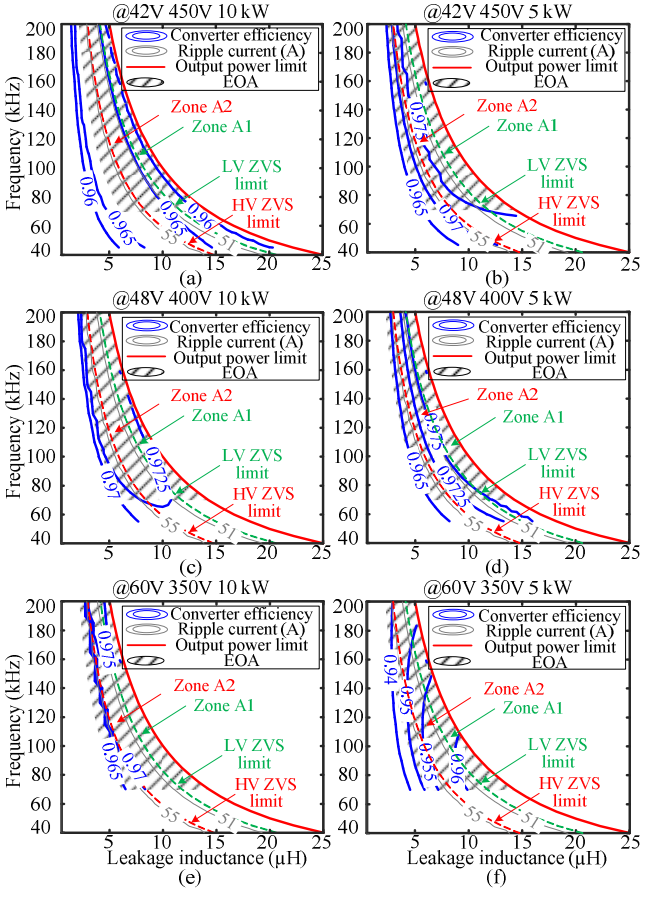

Fig. 11 Converter efficiency at n = 7 under full load and half load.

Combining the analysis above, n = 7 leads to lower ripple current in the whole EOA range compared to n = 8. When n = 7, the highest efficiency of the system is comparable to that of n = 8, and low efficiency can be avoided at V_1 = 60 V and V_2 = 350 V at half load. Lower ripple current (51 A) is also achieved at the same time. Hence n = 7 is preferred as the transformer turn ratio. The parameters f and L_k are chosen in zone **A1** and close to the boundary of zone **A1** and **A2**. In this particular design, L_k = 8 μH, f = 100 kHz, the efficiency approaches its maximum at most operating conditions.

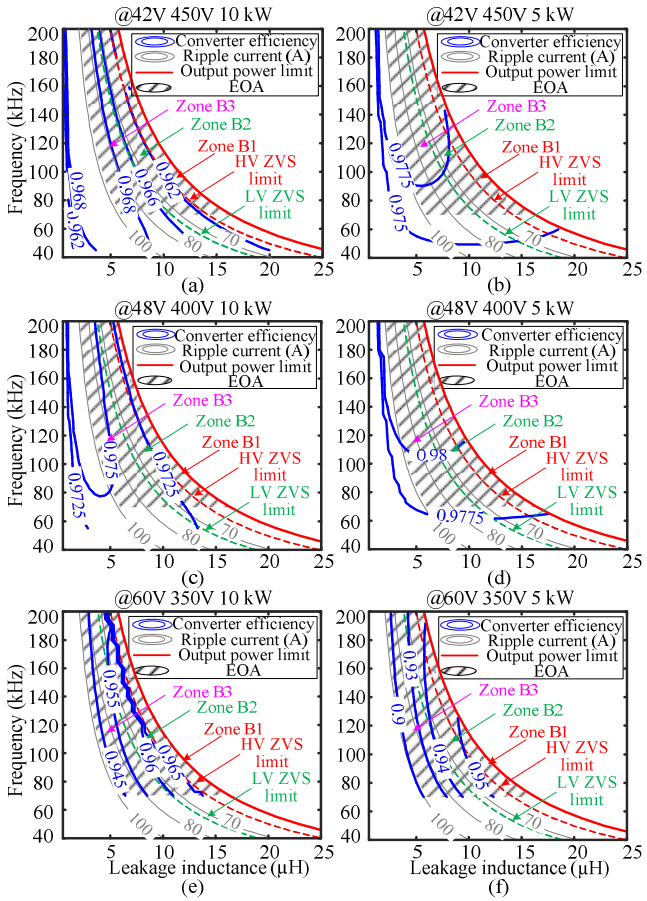

Fig. 12 Converter efficiency at $n = 8$ under full load and half load.

VI. Conclusion

This paper presents comprehensive design considerations of three-phase DAB converter by studying the impact of parameters (n, f, L_k) on the converter performance, including ZVS range, capacitor ripple current and system efficiency. A new parameter fL is defined to simplify the analysis from 3 dimensions (n, f, L_k) to 2 dimensions (n, fL). Based on this, the impact of transformer turn ratio n on ZVS range, RMS current and ripple current are analyzed and feasible values of n are determined. The EOA of f and L_k are defined according to the transformer design. In the EOA, the losses and efficiency analysis shows that HV side switching loss is much more significant compared to LV side and should be avoided at any operating voltage. Finally, the feasible range of f and L_k is determined using the criteria of ZVS, efficiency and capacitor ripple current. The analysis shows that high efficiency can be achieved in a wide operation range. The tradeoff between converter efficiency and capacitor ripple current is achieved.

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