Fast Average Current Mode Control of Dual-Active-Bridge DC-DC Converter using Cycle-by-Cycle Sensing and Self-Calibrated Digital Feedforward

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***Abstract*— The Dual-Active-Bridge (DAB) dc-dc converter is commonly used in isolated and bi-directional applications. The use of high-speed Analog to Digital Converters (ADCs) in high-bandwidth current mode controllers is costly for on-chip implementation. Furthermore, inductor current sensing is susceptible to interference from switching noise and can cause false over-current protection triggers. The DAB converter also has a slow response time using conventional linear PI compensators. Two solutions are demonstrated to tackle these challenges: 1) a cycle-by-cycle analog integrator with synchronous reset for input current averaging to mitigate noise susceptibility and eliminate the need for oversampling ADCs, and a 2) feedforward based controller with self-calibration to drastically decrease the settling time of the DAB converter for large step transients. The proposed system is implemented on a 500W, 95.9% efficient DAB converter prototype. The results show a 600× improvement in response time compared with the traditional PI based average current mode control.**

I. Introduction

The Dual-Active-Bridge (DAB) dc-dc converter is a popular choice for applications requiring isolation and bi-directional power flow beyond 200 W [1]–[5]. The DAB topology features soft-switching, excellent transformer utilization and simple phase shift control. There are many applications such as automotive [1], [6] and energy storage [7]–[9] that require a high conversion ratio, as well as fast transient response to ensure reliable line and load regulation. The trend towards miniaturization through high-frequency operation with wide-band gap devices and reduced energy storage in the passive elements makes fast dynamic response even more critical. The traditional digital Proportional-Integral (PI) average current mode control scheme, as shown in Fig. 1 [10], has slow dynamic performance and requires a costly high-speed over-sampling ADC for the current loop. The need for over-current protection leads to the use of more complex current mode control algorithms [11]. Two practical solutions, well-suited for low-cost on-chip implementation, are proposed to tackle the limitations of traditional DAB controllers: 1) a cycle-by-cycle analog integrator with synchronous reset for input current averaging to mitigate noise susceptibility and eliminate the need for oversampling ADCs, and a 2) feedforward based controller with self-calibration to drastically decrease the settling time of the DAB converter for large step transients.

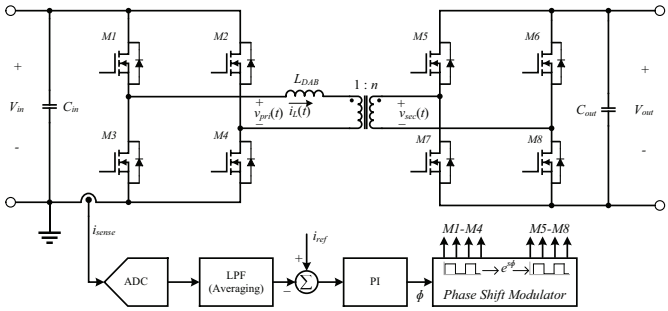


Fig. 1. DAB dc-dc converter with conventional PI based average current mode control.

II. Cycle-by-Cycle Averaged Current Mode Control

In this work, an analog integrator is used to measure the DAB converter's average input current, which is the main control variable in battery fed applications, on a cycle-by-cycle basis. For on-chip implementation, the sensor can be implemented using a transconductance amplifier that integrates the voltage across R_{sense} and charges the capacitance C_1, as shown in Fig. 2. The integrator output, $v_{int}(t)$, is reset at the end of each switching cycle.

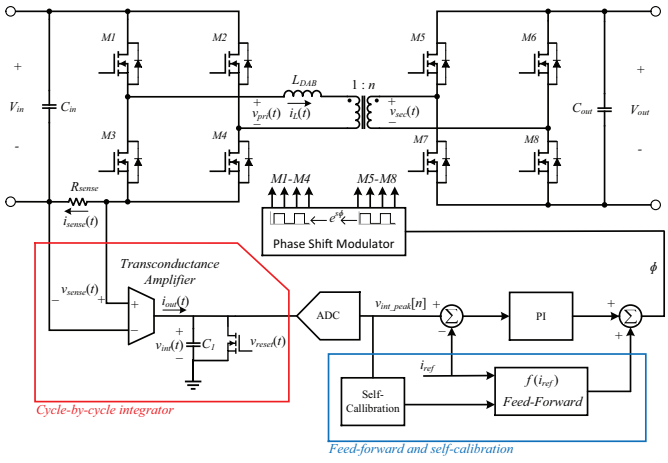


Fig. 2. Proposed controller for the DAB converter, which includes an integrator, feedforward controller, and a self-calibration module.

The DAB inductor current, $i_L(t)$, and the sensed current, $i_{sense}(t)$ are shown in Fig. 3 for two switching cycles. During the first switching cycle, $i_{sense}(t)$ is integrated and $v_{int}(t)$ ramps up. Right before the end of the switching cycle, $v_{int}(t)$ is sampled by a low-cost ADC. At the start of the next switching cycle, $v_{reset}(t)$ is asserted, which resets $v_{int}(t)$. The peak voltage, v_{int_peak}, which is proportional to the average input current, is thus sampled at a rate of $f_s/2$, synchronous with the phase shift modulator block. In contrast to [12], this method drastically improves noise immunity due to averaging, while also eliminating the need for ADC sample rates above f_s (over-sampling) as in [11], [13]. Cycle-by-cycle over-current protection is also achieved with no false triggers.

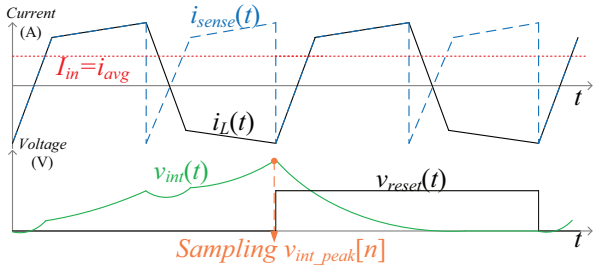


Fig. 3. Key waveforms of the proposed cycle-by-cycle current integrator.

The sampled integrator voltage, $v_{int\_peak}[n]$, is digitally compared with the reference average input current, i_{ref}. In practice, i_{ref}, would be controlled by a low bandwidth outer voltage loop which is not the main focus of this paper.

A. Feedforward Controller

To improve the response time of the controller having a linear PI compensator, a digital feedforward branch is introduced to predict the required value of phase-shift for a given reference average input current. Other studies on predictive control directly sample the inductor current as well as the input and output voltages once per cycle, which is prone to noise [12], [14]. To implement the feedforward controller, the relationship between the DAB converter phase-shift and the averaged input current is needed. The ideal relationship between the phase-shift, ϕ, and the steady-state power, P_{DAB}, is given by:

$$P_{DAB} = \frac{V_{in}V_{out}}{n\omega_s L_{DAB}}\phi\left(1-\frac{|\phi|}{\pi}\right), \tag{1}$$

where ω_s is the switching frequency and L_{DAB} is the DAB converter inductance [15]. Dividing (1) by V_{in} and rewriting in terms of ϕ results in:

$$\phi = \frac{\pi}{2} \pm \sqrt{\frac{\pi^2}{4} - \frac{\langle I_{in}\rangle \pi \omega_s L_{DAB}}{V_{out}}}, \tag{2}$$

which can be linearly approximated by:

$$\phi = m\langle I_{in}\rangle_{Ts} + E, \tag{3}$$

The approximation of (3) is used to implement the $f(i_{ref})$ function in Fig. 2. $\langle I_{in}\rangle_{Ts}$ represents the average input current over one switching cycle which is considered as a variable. The slope and offset parameters, m and E, are updated through self-calibration. The theoretical and experimental relationships between ϕ and $\langle I_{in}\rangle$ is demonstrated in Fig. 4. Due to hardware limitations, the maximum current that can be drawn is 10 Amps.

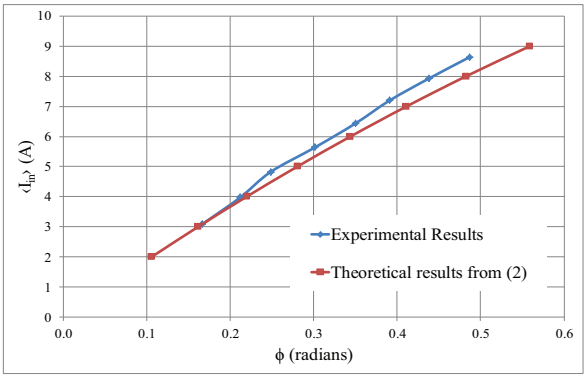


Fig. 4. Comparison between the theoretical and experimental relationship between ϕ and $\langle I_{in}\rangle$.

The small-signal model for the proposed scheme is approximated by cascading the first order transfer function of the DAB converter from ϕ to $\langle I_{in}\rangle$ with the transfer function of the integrator from $\langle I_{in}\rangle$ to v_{int}:

$$\frac{V_{int}(s)}{\Phi(s)} = \frac{1}{sL_{DAB}}.\frac{V_{int}(s)}{I_{in}(s)}, \tag{4}$$

The transfer function of the integrator depends on the specific implementation. In this study, V_{in} and V_{out} are assumed to be well regulated by upstream and downstream power stages, respectively.

B. Self-Calibration for Robustness to Parameter Variations

Component variations, particularly the transformer leakage inductance, can reduce the approximation accuracy of (3), which leads to poor dynamic response. To mitigate this effect, a self-calibration technique is proposed to periodically update the slope and offset parameters, m and E, to account for component and temperature variations. The self calibration process is performed in four steps:

1) The converter is run in open-loop with a fixed phase-shift.
2) v_{int_peak} is sampled every switching cycle.
3) A delay of 300 μs is asserted to ensure current dynamics have subsided.
4) The final sample of v_{int_peak} is stored and compared with the pre-calculated v_{int_peak} at that particular phase-shift.
5) The parameters m and E are then adjusted according to the difference between the pre-calculated and last measured v_{int_peak}.

The representation of (2) for two different inductance values and the pre and post-calibrated $f(i_{ref})$ is shown in Fig. 5. By updating the m and E parameters in (3), the self-calibration

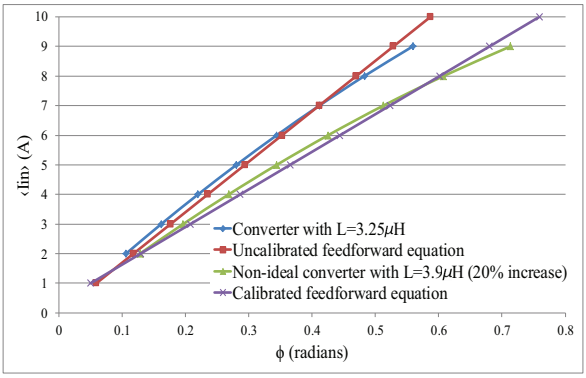


Fig. 5. Effect of the calibration process on (3) for a converter with 20% increase in the inductance value.

process will ensure that the $f(i_{ref})$ equation best fits the actual ϕ-$\langle I_{in}\rangle_{Ts}$ characteristic of the converter, which aids in the improvement of dynamic response. Note that in the targeted application, namely an ac nano-grid with multiple battery storage elements [16]–[18], the system can easily tolerate the occasional current fluctuations caused by this calibration process.

III. Implementation and Experimental Results

The controller is tested using a custom 500W DAB converter prototype with a SiC based secondary bridge at a switching frequency of 125 kHz and a duty cycle of 50%. Other main specifications of the DAB converter prototype are presented in Table I. The presented cycle-by-cycle average current mode control is mainly targeted for on chip implementation, however, as a proof of concept, the integrator is implemented using an op-amp having a unity gain bandwidth of 50MHz in an inverting integrator configuration. A MOSFET in series with a resistor is used to discharge the integrator capacitor.

TABLE I

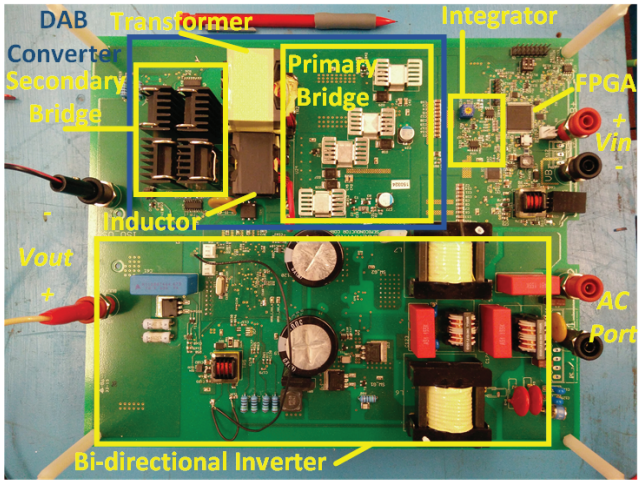
DAB converter prototype specifications

Parameter	Value	Unit
Input voltage, V_{in}	50	V_{DC}
Output voltage, V_{out}	400	V_{DC}
Input Capacitance, C_{in}	374	μF
Output Capacitance, C_{out}	300	μF
DAB Inductance, L_{DAB}	3.25	μH
Transformer turns ratio, n	8	
Peak Power	500	W
Peak efficiency (301 W)	95.9	%
Switching frequency, w_s	125	kHz
Primary side MOSFETs	IPB017N08N5, Infineon OptiMOS 5, 80 V, 120 A, 1.7 mΩ	
Secondary side MOSFETs	C2M0160120D, CREE SiC, 1200 V, 19 A, 160 mΩ	

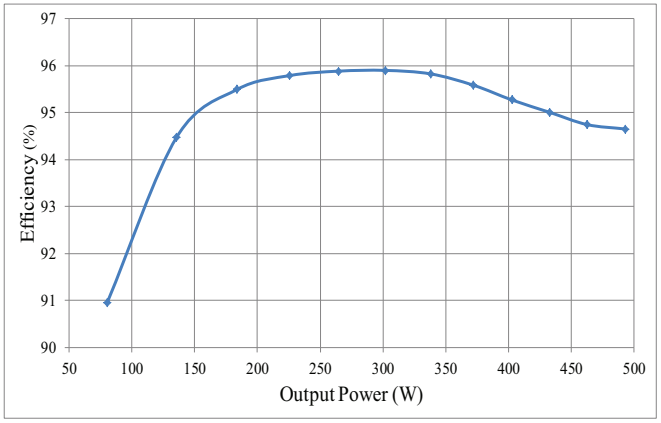
The DAB converter prototype, which is part of a four-quadrant micro-inverter, and the measured efficiency curve are shown in Figs 6(a) and (b), respectively. A peak efficiency of 95.9% is achieved at 301 W. The main waveforms of the proposed cycle-by-cycle current controller is presented in Fig. 7, which is similar to the theoretical waveforms shown in Fig. 3. It must be noted that, in the experimental setup, $v_{int}(t)$ is sampled every other switching cycle as opposed to the suggested cycle-by-cycle method. This is to ensure the complete discharge of the integrator capacitor, C_1, and to more clearly demonstrate the integrator operation. However, the setup can be made to operate in a cycle-by-cycle fashion by either:

1) reducing the value of C_1 and MOSFET series resistance, or
2) by reducing reset and integration times and not discharging C_1 completely.

The improvement in response time of the proposed control scheme is shown in Fig. 8. The PI compensator coefficients were adjusted to avoid significant current overshoot.



(a)



(b)

Fig. 6. (a) 500W DAB converter prototype, as part of a four-quadrant micro-inverter for AC nano-grids. (b) Measured Efficiency

The key converter waveforms during the calibration process are shown in Fig. 9. The inductor current, $i_L(t)$, and $v_{int}(t)$ are demonstrated as the converter is operated in open-loop during which v_{int_peak} is sampled every other cycle. Once current dynamics subside, after waiting for 300 μs, the last measured v_{int_peak} value is stored. The open-loop portion of the calibration phase is completed and the slope and offset

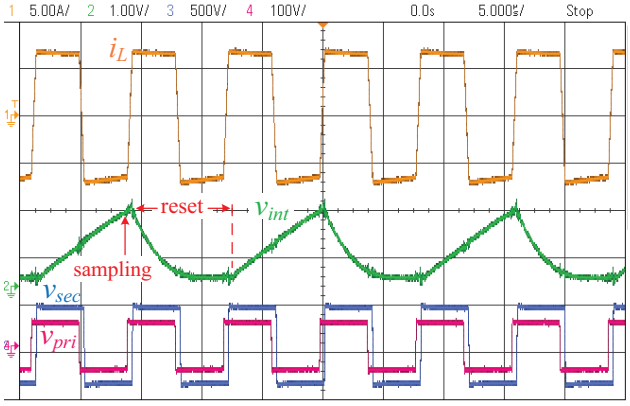


Fig. 7. Steady-state operation of the converter at 320 W output power, showing the integrator operation similar to Fig. 3.

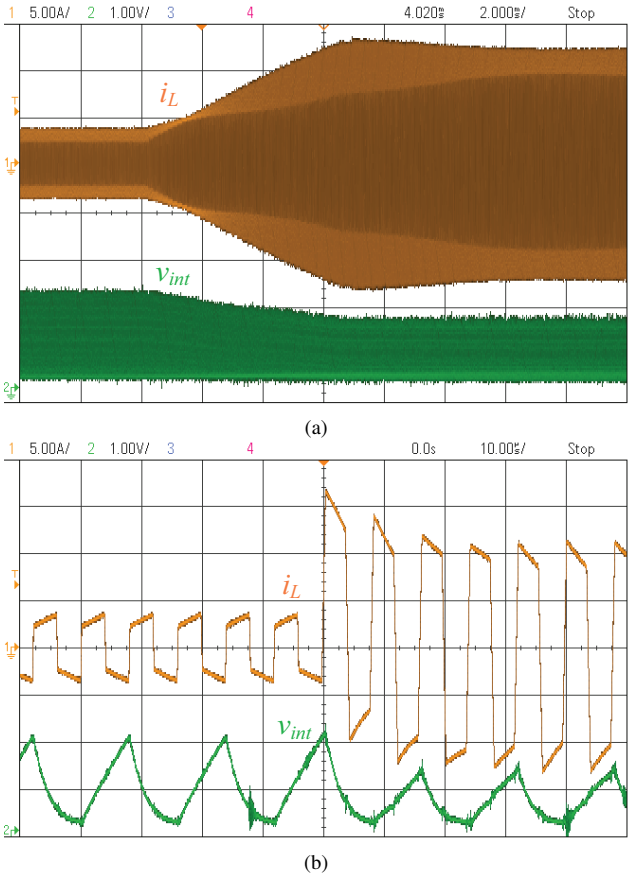


Fig. 8. (a) Average input current reference step response from 2.9 A to 9.3 A for the optimized conventional PI controller (Response time = 16 ms), and (b) for the feedforward based controller (response time = 24 μs).

parameters are kept constant at the scaled value proportional to the difference between the last measured and expected values of v_{int_peak}.

To investigate the effectiveness of the self-calibration feature, the response time of the system to an average input current reference step from 2.9 A to 9.3 A was measured for two different sets of m and E parameters in (3). The first set corresponds to a converter with 20% lower value for L_{DAB} and the second set corresponds to the updated m and E parameters after self-calibration. The result proves a reduction in response time of more than 15 μs, as shown in Fig. 10.

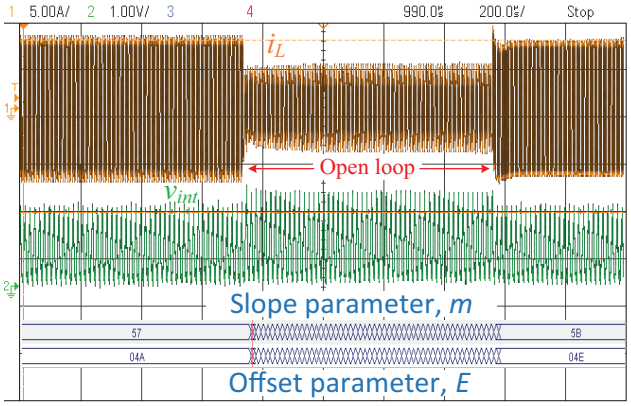


Fig. 9. Converter waveforms during the calibration process. The parameters m and E keep updating after every sample of v_{int_peak} until the last open-loop switching cycle.

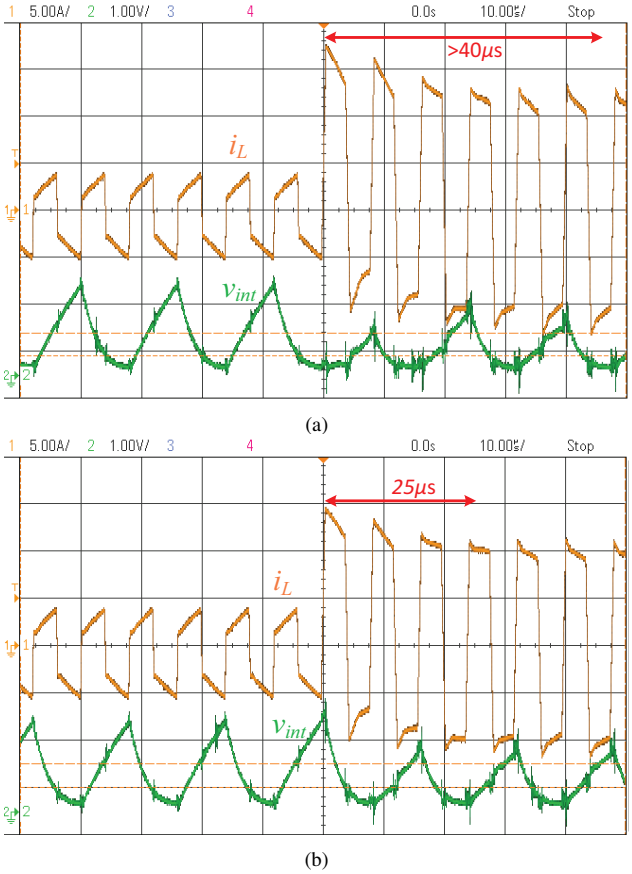


Fig. 10. (a) Average input current reference step response from 2.9 A to 9.3 A for the controller with m and E parameters corresponding to a converter with 20% lower value for L_{DAB} (Response time = more than 40 μs), and (b) for the controller with updated m and E parameters after calibration (response time = 25 μs).

IV. Conclusions and Future Work

This paper presents a cycle-by-cycle average current mode controller with a feedforward branch to enhance the dynamic performance of the DAB converter. The cycle-by-cycle analog integrator is implemented with discrete components as a proof of concept, however this technique is intended for on-chip controller implementation. By approximating the relationship between ϕ and $\langle I_{in} \rangle$ the self-calibrating feedforward branch is implemented and verified, which results in a drastic 600x improvement in response time of the DAB converter. The significance of the self-calibration feature is also investigated by comparing the response time of the converter under component variations.

Acknowledgements

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