A Three-Phase Soft-Switched High-Power-Density dc/dc Converter for High-Power Applications

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Abstract—**Three dc/dc converter topologies suitable for high-power-density high-power applications are presented. All three circuits operate in a soft-switched manner, making possible a reduction in device switching losses and an increase in switching frequency. The three-phase dual-bridge converter proposed is seen to have the most favorable characteristics. This converter consists of two three-phase inverter stages operating in a high-frequency six-step mode. In contrast to existing single-phase ac-link dc/dc converters, lower turn-off peak currents in the power devices and lower rms current ratings for both the input and output filter capacitors are obtained. This is in addition to smaller filter element values due to the higher-frequency content of the input and output waveforms. Furthermore, the use of a three-phase symmetrical transformer instead of single-phase transformers and a better utilization of the available apparent power of the transformer (as a consequence of the controlled output inverter) significantly increase the power density attainable.**

Introduction

THE AREA of high-power-density dc/dc converters has been an important research topic, especially for switched-mode power-supply applications rated at up to 500 W. The needs of the next generation of aerospace applications require extremely high-power densities at power levels in the multikilowatt to megawatt range. The implications of realizing high-power density and low-weight systems at these power levels have rarely been addressed. This paper examines considerations for the selection of topologies that can realize the low-weight constraints that are of primary importance.

Recognizing that higher switching frequencies are the key to reducing the size of the transformer and filter elements, it is apparent that some form of soft-switching converter with zero-switching loss is required if system efficiencies and heat sink size are to be maintained at a reasonable level. By far the most attractive circuit so far has been the series resonant converter (SRC) [1]. Using thyristors with a single LC circuit for device commutation and energy transfer, the topology is extremely simple in realization and offers the possibility of power densities in the 0.9–1.0 kg/kW range at power levels up to 100 kW.

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The following problems can be identified with the SRC. Thyristor commutation requirements demand higher current ratings from the devices and higher VA ratings from the LC components. Thyristor recovery times significantly slow down the maximum switching frequencies attainable. Snubber inductors and RC networks are needed to effect current transfer without encountering a diode recovery problem. Capacitive input and output filters have to handle ripple currents at least as large as the load current. Although switching frequencies in the 10-kHz range yield dramatic reduction in converter size when compared to conventional hard-switching circuits, it is clear that systems operating at similar frequencies and with lower component ratings are potentially capable of even higher power densities.

This paper proposes a new soft-switching dc/dc converter topology suitable for high-power applications. Soft-switched converters are characterized by intrinsic modes of operation that allow an automatic and lossless resetting of the snubber elements through an appropriate recirculation of trapped energy. The capability to eliminate losses associated with the snubber now permit the use of oversized snubbers resulting in dramatically lower device-switching losses, even at substantially higher frequencies. Examples of soft-switched dc/dc converters are the parallel output SRC operated above resonance [2], the pseudo-resonant converter, the resonant pole [3], [4], and all quasi-resonant converters [5]–[7]. For multiquadrant operation and for dc/ac inverter applications, typical examples of soft-switched topologies are the resonant dc/link inverter and the quasi-resonant current mode or resonant pole inverter [8]. The proposed circuit utilizes the resonant pole as the basic switching element for both input and output devices and yields substantial benefits in power density and operating characteristics.

Soft-Switched DC/DC Converters

The preferred dc/dc converter topology for high-power applications has been the full-bridge circuit operated at constant frequency under a pulsewidth control strategy. The topology features minimal voltage and current stresses in the devices, minimum VA rating of the high frequency transformer, as well as low ripple current levels in the output filter capacitor. The power density levels that can be reached are limited by peak and average device-switching losses, transformer leakage inductances, and output rectifier reverse recovery. The factors above constrain the maximum frequency attainable, and thus the smallest size possible, given the state of the art in component technology. Most of the resonant converters reported in literature

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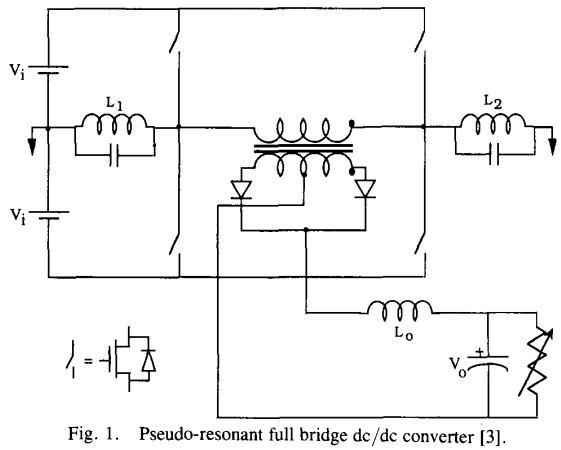


Fig. 1. Pseudo-resonant full bridge dc/dc converter [3].

attempt to tackle one or more of the problems listed, typically at the expense of substantially higher component stresses [5]–[7]. For high-power operation, that is unacceptable. Soft-switching variations of the full-bridge converter are thus the most favored topologies.

The pseudo-resonant dc/dc converter proposed in [3] is shown in Fig. 1. It uses capacitive snubbers and can be designed with device stresses approaching that of the conventional full bridge. However, the circuit uses the transformer as a voltage transfer element, and the interactions of its leakage inductance (L_{lk}) and the output rectifier are unresolved. The maximum switching-frequency limit is reached when the energy lost due to L_{lk} and the peak-diode reverse-recovery current become unacceptable.

Transferring the output filter inductance to the ac side completely changes the operating characteristics of the circuit [3]. As shown in Fig. 2(a), the inductance L_o is now in series with the transformer leakage inductance L_{lk}. Further, energy trapped in ($L_{lk} + L_o$) during reverse recovery is now transferred to the load in a lossless manner. This implies that a further increase in switching frequency may be possible. It can also be shown that the additional inductors L_1 and L_2 required in the previous circuit (Fig. 1) are no longer absolutely essential, since adequate control range can be obtained at constant frequency while maintaining soft switching for all devices. Operating waveforms for this single-phase phase-shifted dc/dc converter (Topology A) are shown in Fig. 2(b). It can be seen that soft switching is obtained by ensuring that device turn-on only occurs when its antiparallel diode is conducting. The biggest problem with this circuit seems to be the high ripple current in the output filter capacitor. For low-voltage high-current power supplies, this is a very important consideration. For high-power high-voltage aerospace applications, it is not seen to be a major problem because power densities obtainable with multilayer ceramic capacitors are at least as good as with inductors.

It has been proposed in [9] that the diode recovery process is akin to the existence of an active device in antiparallel with it. Observing that the circuit in Fig. 2(a) naturally handles the diode reverse recovery process, it is proposed that the diodes be replaced by active devices as shown in Fig. 3(a) [10]. Many high-frequency converters already use synchronous rectifiers in essentially the same location. The converter can now be operated with a simpler control strategy in which the input and output bridges generate square waves that are phase shifted from each other. In keeping with our philosophy, regions of operation can

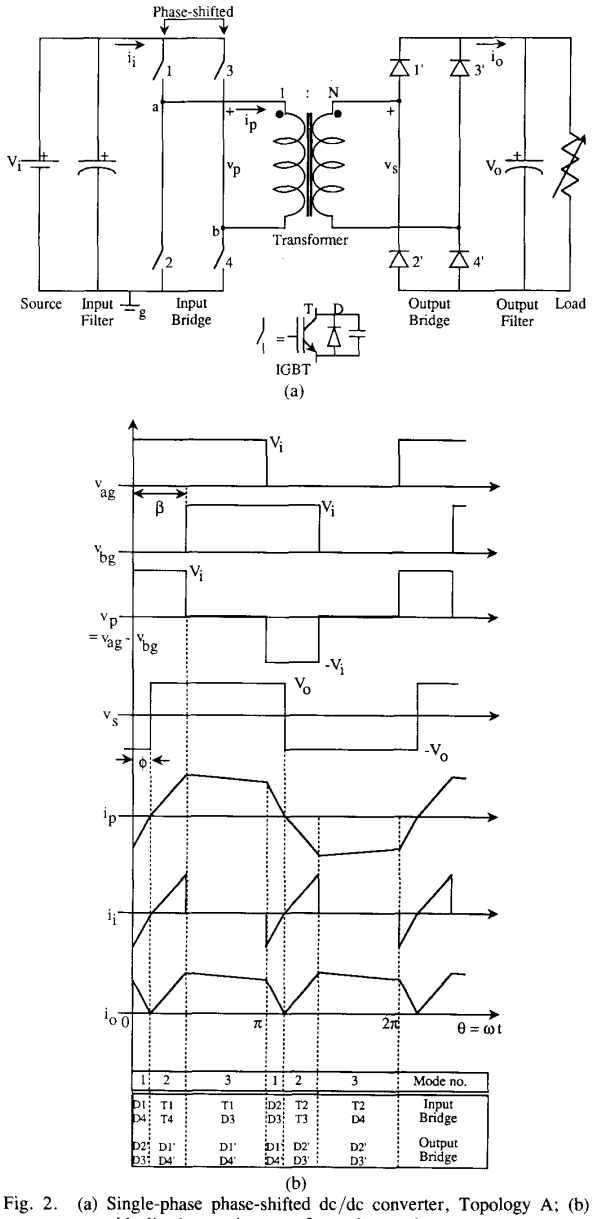
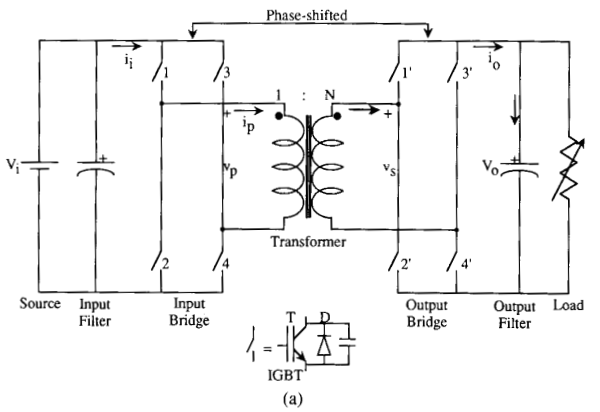


Fig. 2. (a) Single-phase phase-shifted dc/dc converter, Topology A; (b) idealized operating waveforms for topology A.

be identified that permit soft switching of all devices in both bridges. Fig. 3(b) shows operating waveforms for the single-phase dual-bridge dc/dc converter topology (Topology B).

The circuit in Fig. 3(a) can be extended to a polyphase version. The three-phase dual-bridge circuit (Topology C) is shown in Fig. 4(a). Again, examining the modes of operation for the converter, it is possible to identify regions where both sets of switches experience soft switching. As in the case of the single-phase dual-active bridge converter, both bridges generate quasi-square-waves phase shifted from each other. It should be noted that the soft-switching transition is actually resonant in nature [3], [8] but is assumed to be almost instantaneous for the derivation of first-order operating characteristics. The three-phase dual-active bridge converter has substantially lower filter



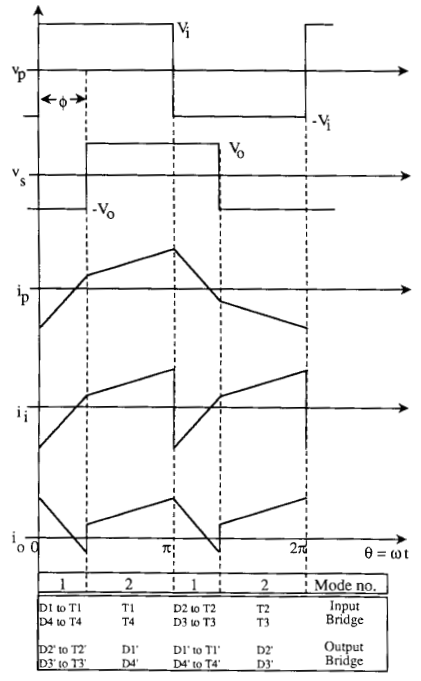
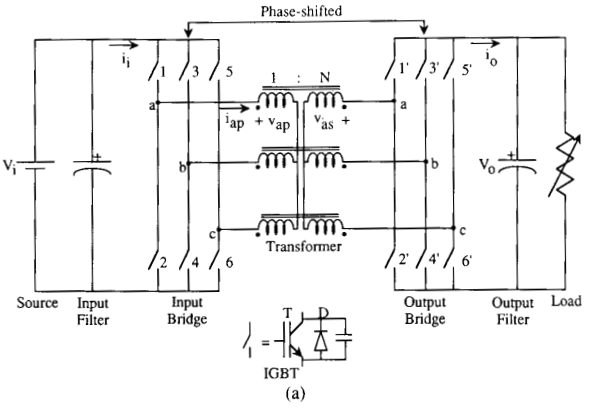


Fig. 3. (a) Single-phase dual active bridge dc/dc converter, Topology B; (b) idealized operating waveforms for topology B.



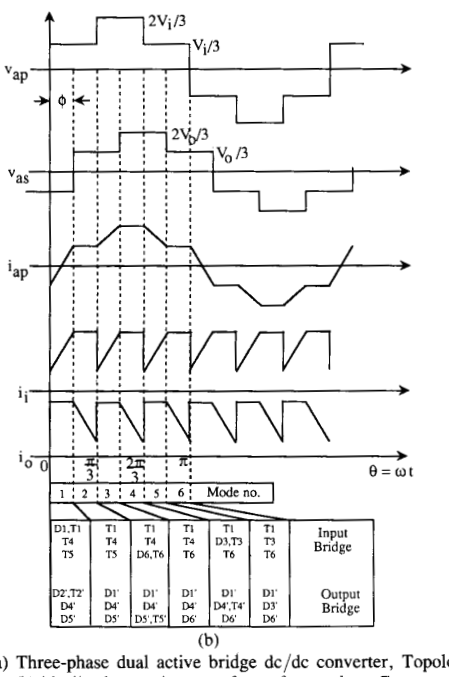


Fig. 4. (a) Three-phase dual active bridge dc/dc converter, Topology C; (b) idealized operating waveforms for topology C.

ratings when compared to its single-phase counterpart. Consequently, it has the potential of realizing the highest power density.

It should be noted that all three converters, denoted Topology A, B, and C for circuits in Figs. 2, 3, and 4, respectively, exhibit desirable properties with regard to parasitics such as device storage time, transformer leakage inductance, and diode reverse recovery. It is shown in the paper that transformers, which use the leakage impedance as an energy transfer element, have the potential of reaching higher power densities. Although this technique has been used extensively at lower power levels, it has been felt that the higher VA rating of the composite transformer was an unacceptable penalty at higher power levels. It will be shown that the resulting increase in switching frequency more than compensates for the increased VA rating, allowing substantial reduction in the overall size of the converter. The use of dual-active bridges also yields unexpected gains in power density, as will be shown, and permits bidirectional power flow. Analysis in the paper is restricted to unidirectional power flow only.

Analysis of the Single-Phase Converters

Topology A

In order to derive the operating characteristics of the three dc/dc converters, it is assumed that the transfer of current from device to diode on turn-off is instantaneous. The actual switching locus depends on the value of snubber capacitance C used and the current level. For a typical device such as a bipolar junction transistor (BJT) with a current fall time t_f and a turn-off current I_m, the device energy loss per switching cycle can be found approximately to be [11]

$$E_{sw} = \frac{I_m^2 t_f^2}{24C}. \tag{1}$$

Since there are no turn-on or snubber dump losses, C can be

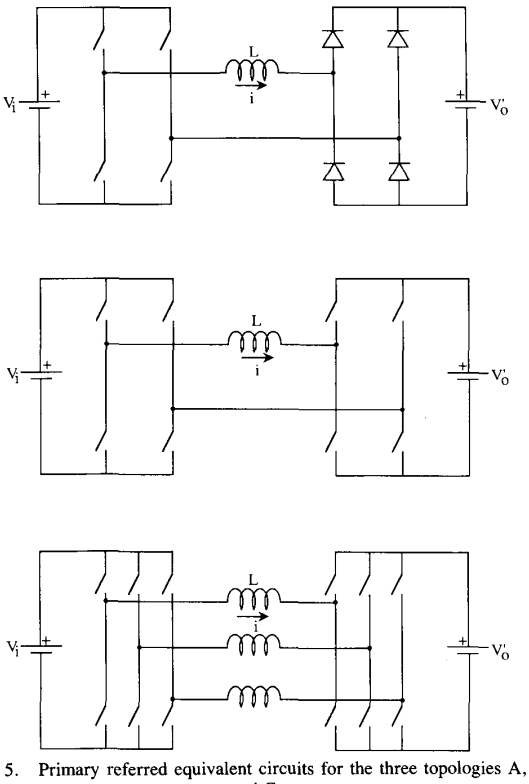


Fig. 5. Primary referred equivalent circuits for the three topologies A, B, and C.

made fairly small while retaining a fast-switching characteristic and low-device losses, simultaneously. This justifies the assumption of a fast, almost instantaneous switching transition for analysis over a full cycle.

The primary-referred equivalent circuits for the three converters are shown in Fig. 5. Replacing the transformer with a leakage inductance L simplifies circuit analysis. For Topology A, three operating modes can be identified as shown in Fig. 2(b). The phase shift between the two bridges is ϕ, dependent on L and the load. The equivalent voltage applied across the load is V_{ab} and has pulsewidth β, where β is the controlled phase shift between the two resonant poles of the input bridge. The inductor current i as a function of $\theta = \omega t$, where ω is the switching frequency, is as follows. In Mode 1,

$$i(\theta) = \left[\frac{V_i + V_o'}{\omega L}\right]\theta + i(0) \tag{2}$$

where V_i, V_o' are input and primary-referred output dc voltages and $i(0)$ is the initial current at $\theta = 0$. Mode 1 ends at $\theta = \phi$. In Mode 2,

$$i(\theta) = \left[\frac{V_i - V_o'}{\omega L}\right](\theta - \phi) + i(\phi). \tag{3}$$

Similarly, the current in Mode 3 can be found to be

$$i(\theta) = \left[\frac{-V_o'}{\omega L}\right](\theta - \beta) + i(\beta). \tag{4}$$

At the end of the half cycle $i(\pi) = -i(0)$. Solving for $i(0)$, we can obtain the complete current waveform. The soft-switching constraints require that the device be conducting at turn-off. From Fig. 2(b) this implies that $i(\pi) \geq 0$. Further, given the output rectifier it is clear that $i(\phi) = 0$. Using the preceding relationships,

$$\phi = \frac{1}{2}(\beta - d\pi). \tag{5}$$

In addition, since $\phi \geq 0$, we get

$$\beta - d\pi \geq 0 \tag{6}$$

where

$$d = \frac{V_o'}{V_i}. \tag{7}$$

The parameter d represents the primary-referred dc voltage gain of the converter, often referred to as the dc conversion ratio. From $i(\theta)$ and the converter switching functions, the supply or output average current can be found to yield power transfer at a given β, d, and ω. This is found to be

$$P_o = V_i I_i = \frac{dV_i^2}{4\omega L}\left[2\beta - \pi d^2 - \frac{\beta^2}{\pi}\right] \tag{8}$$

where I_i is the average value of $i(\theta)$. Input and output filter-capacitor rms current ratings can also be calculated from $i(\theta)$. Peak device voltage and current ratings are also easily found. The kVA rating of the transformer is calculated as

$$(\text{kVA})_T = \frac{1}{2}\left[v_{\text{pri(rms)}} i_{\text{pri(rms)}} + v_{\text{sec(rms)}} i_{\text{sec(rms)}}\right], \tag{9}$$

which can be derived as (neglecting magnetizing current)

$$(\text{kVA})_T = V_i\left[\sqrt{\frac{\beta}{\pi}} + d\right] I_{\text{rms}} \tag{10}$$

where I_{rms} is the rms value of $i(\theta)$. Operating characteristics for Topology A are calculated based on the principles listed previously and are shown in Fig. 6. All quantities have been normalized to the following base:

$$\text{voltage base } V_b = V_i$$

$$\text{current base } I_b = \frac{V_i}{\omega L}$$

$$\text{power base } P_b = V_b I_b = \frac{V_i^2}{\omega L}. \tag{11}$$

Fig. 6(a) depicts the range of control possible with variation of β while maintaining soft-switching operation for all four input devices. For each value of d the output power is shown over the soft-switching region. The locus of the minimum power for each d defines the soft-switching boundary corresponding to $\beta = d\pi$. It is seen that maximum power transfer occurs at $\beta = 180°$ and $d = 0.58$. Fig. 6(b) shows a variation of the transformer kVA versus the power output P_o. It is seen that at the design point (maximum power transfer), the $P_o/(\text{kVA})_T$ ratio is approximately 0.64 pu.

Topology B

A similar analysis can be carried out for Topology B. This converter has only two modes of operation. The two bridges are presumed to operate with controlled phase shift ϕ. The current $i(\theta)$ is once again given by (2) and (3) for Modes 1 and 2,

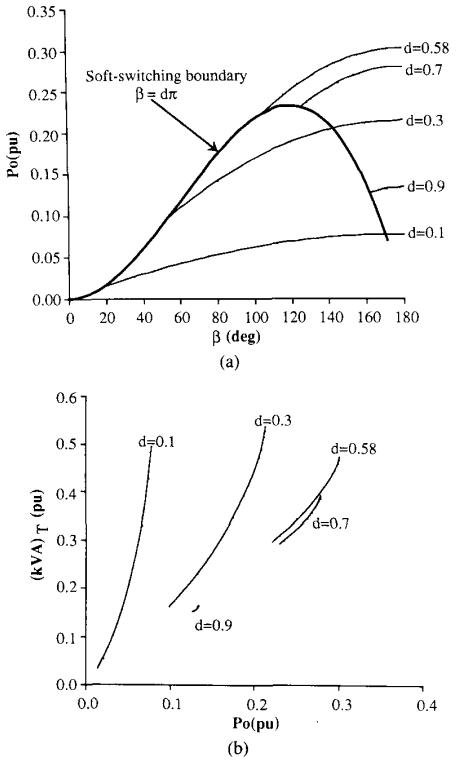


Fig. 6. (a) Output power versus β, with d as parameter for topology A; (b) transformer kVA versus output power, with d as parameter for topology A.

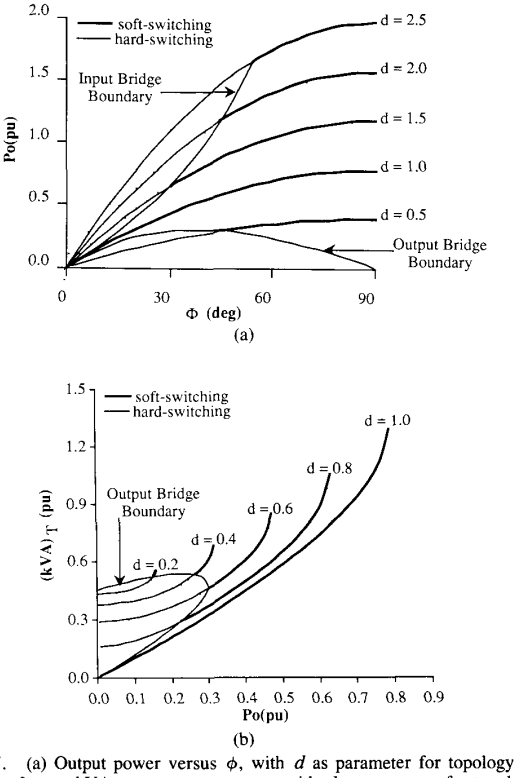


Fig. 7. (a) Output power versus ϕ, with d as parameter for topology B; (b) transformer kVA versus output power, with d as parameter for topology B.

respectively. The boundary conditions now dictate that $i(0) = -i(\pi)$ at the end of Mode 2. Solving for $i(\theta)$, the output power P_o and transformer kVA are given as

$$P_0 = \frac{V_i^2}{\omega L} d\phi\left[1 - \frac{\phi}{\pi}\right] \tag{12}$$

$$(\text{kVA})_T = V_1[1 + d] I_{\text{rms}}. \tag{13}$$

The constraints, which define soft-switching boundaries, can now be specified for the input and output bridges to be $i(0) \leq 0$ and $i(\phi) \geq 0$, respectively. These constraints enclose the desired operating region for the converter. Exceeding the first constraint results in natural commutation of the input bridge devices and gives snubber dump. For the output bridge, the constraint equation corresponds to diode bridge operation.

Fig. 7(a) shows the variation of normalized P_o as a function of ϕ for different values of d. The input bridge and output bridge boundaries enclosing the soft-switching region are shown. For $d = 1$ it can be seen that ϕ can vary over the entire range of 0–90°, giving control from zero to full power. The curves corresponding to $d > 1$ represent boost operation.

Fig. 7(b) plots the transformer kVA against the output power for various values of d. The output bridge boundary, corresponding to the output diode bridge, is identical to that in Fig. 6(b) (for Topology A) with $\beta = \pi$. An interesting feature of Topology B can be brought to light by examining the minimum transformer kVA (0.475 pu) required for transferring the maximum output power (0.302 pu) on the diode bridge boundary. For the same kVA the output power can be increased to 0.422 pu at $d = 1$ with dual-active bridges. This gives us a transformer utilization (defined as $P_o/(\text{kVA})_T$) of 0.89, an improvement of 40%.

Compared to normal hard-switched converters with $P_o/(\text{kVA})_T$ ratios approaching unity, this may seem to be very poor transformer utilization. However, if the switching frequency for the proposed converter can be made substantially higher, actual size/weight could be much lower. Transformer sizing will be examined in greater detail later in the paper. It is apparent that along with further gains in transformer power density, a significant reduction in input/output filter size and ripple current rating will result from selecting the three-phase dc/dc dual-bridge converter.

Analysis of the Three-Phase dc/dc Converter

The circuit schematic of the new three-phase dual-bridge soft-switching ac-link dc/dc converter is shown in Fig. 4. The proposed converter consists of two three-phase inverter stages, each operating in a six-step mode with controlled phase shift. Using two active bridges not only permits bidirectional power flow, but also allows control at a fixed frequency. The ac-link transformer is Y–Y-connected and is three-phase symmetric with the leakage inductances used as energy transfer elements.

In the following analysis, it is assumed that the primary and secondary resistances of the transformer can be neglected and the turns ratio is 1:1. Fig. 8 shows the schematic of the three-phase symmetric transformer. Using the relationship $i_a + i_b + i_c = 0$ for Y-connected transformers, the transformer equa-

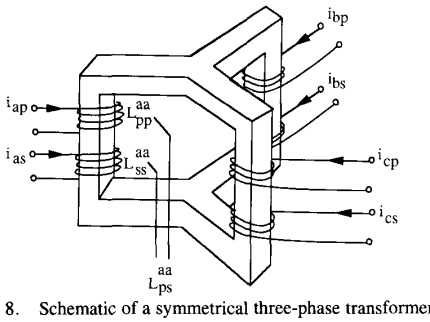


Fig. 8. Schematic of a symmetrical three-phase transformer.

tions can be derived to be

$$V_{ap}(t) = L_{pl}\frac{di_{ap}}{dt} + \left[L_{pp}^{aa} + L_{pp}^{ab}\right]\frac{di_{ap}}{dt} + \left[L_{ps}^{aa} + L_{ps}^{ab}\right]\frac{di_{as}}{dt} \quad (14)$$

and

$$V_{as}(t) = L_{sl}\frac{di_{as}}{dt} + \left[L_{ss}^{aa} + L_{ss}^{ab}\right]\frac{di_{as}}{dt} + \left[L_{sp}^{aa} + L_{sp}^{ab}\right]\frac{di_{ap}}{dt} \quad (15)$$

where V_{ap} and V_{as} are the primary and secondary voltages for the a-phase, L_{pl} and L_{sl} the primary and secondary leakage inductances, L_{pp} and L_{ss} are self-inductances, and L_{ps} and L_{sp} are the mutual inductances between the appropriate phase windings given by the superscript notation used.

Using properties of a symmetric transformer and defining

$$L_m = L_{ss}^{aa} + L_{ss}^{ab} = L_{pp}^{aa} + L_{pp}^{ab}, \quad (16)$$

one can derive

$$\sigma(L_m + L_{sl})\frac{di_{as}}{dt} = V_{as}(t) - \frac{L_m}{L_m + L_{pl}}V_{ap}(t) \quad (17)$$

$$\sigma(L_m + L_{pl})\frac{di_{ap}}{dt} = V_{ap}(t) - \frac{L_m}{L_m + L_{sl}}V_{as}(t) \quad (18)$$

where σ is a leakage factor given by

$$\sigma = \frac{(L_m + L_{sl})(L_m + L_{pl}) - L_m^2}{(L_m + L_{pl})(L_m + L_{sl})}. \quad (19)$$

The value of σ is typically a small number around the ratio of the leakage to the magnetizing inductance.

Equations (17) and (18) are the basic equations that govern the current in the circuit. Further assuming that $L_{sl} = L_{pl} \ll L_m$ (for 1:1 turns ratio), then (17) and (18) reduce to

$$L_\sigma\frac{di_{as}}{dt} = V_{as}(t) - V_{ap}(t) \quad (20)$$

$$L_\sigma\frac{di_{ap}}{dt} = V_{ap}(t) - V_{as}(t) \quad (21)$$

where

$$L_\sigma = \sigma(L_m + L_{sl}) = \sigma(L_m + L_{pl}) = (L_{sl} + L_{pl}). \quad (22)$$

The simplified single equivalent circuit reduces to that shown in Fig. 5(c) with $L = L_\sigma$. It can be seen that with the preceding assumptions, $i_{as} = i_{ap} = i(\theta)$.

In order to calculate the three line currents, the classic six-step line-to-neutral voltage waveform is assumed for both the primary and secondary windings. The difference between the two voltages is applied across L. Six modes, corresponding to different driving voltages, can be identified over a 180° conduction cycle. Using the property of a balanced three-phase set and $i_a + i_b + i_c = 0$, one can obtain full information by calculating two currents over 1/3 of a period. Solving for $i(\theta)$ over a half period 0 to π,

for $0 \le \theta \le \phi$

$$i(\theta) = i(0) + \frac{V_i(1+d)}{3\omega L}\theta \quad (23)$$

for $\phi \le \theta \le \pi/3$

$$i(\theta) = i(\phi) + \frac{V_i(1-d)}{3\omega L}(\theta - \phi) \quad (24)$$

for $\pi/3 \le \theta \le \phi + \pi/3$

$$i(\theta) = i\left(\frac{\pi}{3}\right) + \frac{V_i(2-d)}{3\omega L}\left(\theta - \frac{\pi}{3}\right) \quad (25)$$

for $\phi + \pi/3 \le \theta \le 2\pi/3$

$$i(\theta) = i\left(\phi + \frac{\pi}{3}\right) + \frac{V_i(2-2d)}{3\sigma L}\left(\theta - \phi - \frac{\pi}{3}\right) \quad (26)$$

for $2\pi/3 \le \theta \le 2\pi/3 + \phi$

$$i(\theta) = i\left(\frac{2\pi}{3}\right) + \frac{V_i(1-2d)}{3\omega L}\left(\theta - \frac{2\pi}{3}\right) \quad (27)$$

for $\phi + 2\pi/3 \le \theta \le \pi$

$$i(\theta) = i\left(\phi + \frac{2\pi}{3}\right) + \frac{V_i(1-d)}{3\omega L}\left(\theta - \frac{2\pi}{3} - \phi\right). \quad (28)$$

Equating $i(0) = -i(\pi)$ and solving, we obtain

$$i(0) = \frac{V_i}{3\omega L}\left[\frac{2\pi d}{3} - d\phi - \frac{2\pi}{3}\right]. \quad (29)$$

Using $i(\theta)$, the supply-side dc-link current can be reconstructed using the input bridge switching function and is shown in Fig. 4(b). From this, the average output power is calculated to be

$$P_0 = \frac{V_i^2}{\omega L}d\phi\left[\frac{2}{3} - \frac{\phi}{2\pi}\right]. \quad (30)$$

The above results apply for $0 \le \phi \le \pi/3$.

For $\pi/3 \le \phi \le 2\pi/3$, a similar set of equations can be derived. The average output power for ϕ in this range can then be found to be

$$P_o = \frac{V_i^2}{\omega L}d\left[\phi - \frac{\phi^2}{\pi} - \frac{\pi}{18}\right]. \quad (31)$$

Based on $i(\theta)$, the important parameters such as the transformer kVA, input and output capacitor ripple current, and peak device stresses can be found. The transformer kVA, for instance, is

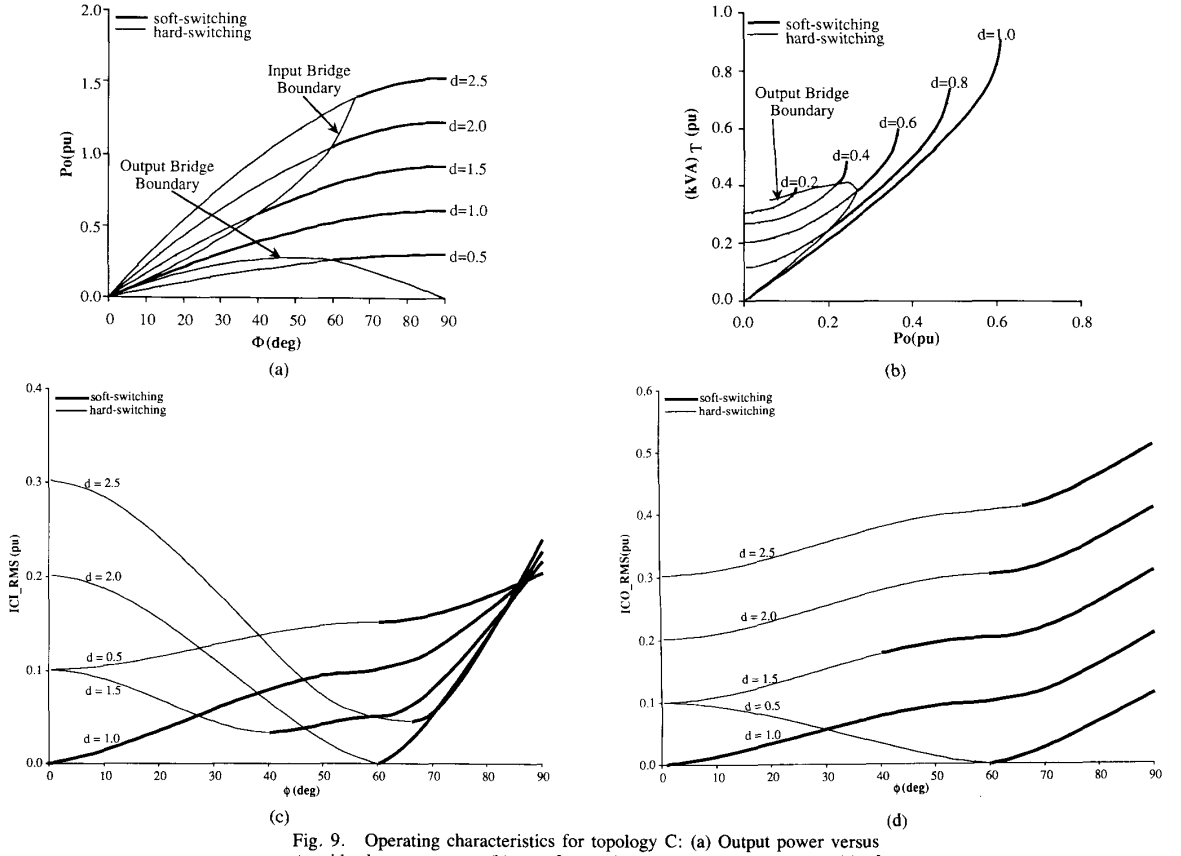


Fig. 9. Operating characteristics for topology C: (a) Output power versus ϕ, with d as parameter; (b) transformer kVA versus output power, with d as parameter; (c) input filter capacitor r.m.s. current versus ϕ, with d as parameter; (d) output filter capacitor r.m.s. current versus ϕ, with d as parameter.

calculated as in (9) and can be reduced to

$$(\text{kVA})_T = \frac{V_i(1+d)I_{\text{rms}}}{\sqrt{2}}.$$

Fig. 9(a) is similar to Fig. 7(a) and shows the variation of P_0 as a function of ϕ for different values of d. Once again, the curve for $d = 1$ shows wide range of control, i.e., from zero power for $\phi = 0$ to maximum power for $\phi = \pi/2$. The output bridge boundary corresponds to the soft-switching locus for a diode output bridge. This locus is derived by finding the value of $\phi = \phi_c$ such that $i(\phi_c) = 0$. For $0 \le \phi \le \pi/3$ this yields the lower boundary d_l:

$$d_l = 1 - \frac{3\phi}{2\pi}. \tag{32a}$$

The upper boundary governs the transition for the input bridge between natural commutation and soft switching. This corresponds to the relationship $i(0) = 0$, which yields d_u:

$$d_u = \frac{1}{1 - \dfrac{3\phi}{2\pi}}. \tag{32b}$$

For $\pi/3 \le \phi \le 2\pi/3$, the lower and upper boundaries are obtained to be

$$d_l = \frac{3}{2} - \frac{3\phi}{\pi} \tag{33a}$$

$$d_u = \frac{1}{\dfrac{3}{2} - \dfrac{3\phi}{\pi}}. \tag{33b}$$

Fig. 9(b) shows the kVA rating of the transformer for $0 \le d \le 1$ as a function of the output power. The locus corresponding to output diode bridge operation is also plotted. Once again, it can be seen that for the maximum power transfer point (0.267 pu) on the output bridge boundary (pertaining to the output bridge operating as a diode bridge) the minimum transformer kVA required is 0.391 pu, which gives a transformer utilization of 68%. Now, for the same transformer kVA, the output power can be increased to 0.351 pu at $d = 1$ by virtue of an active output bridge. The transformer utilization has thus been increased by 31%.

Fig. 9(c) and 9(d) shows the ripple current in the input and output capacitor filters as a function of d and ϕ. It will be seen that for $d = 0.5$ and $\phi = 60°$, the output current ripple goes to zero. At the maximum power transfer point $P_0 = 0.46$ pu, $\phi = 50.1°$ and the output current ripple is 0.095 pu while the input current ripple is 0.0925 pu. For lower values of d, the

output current ripple increases. However, under all conditions, the ripple is substantially smaller than for either of the single-phase converters. Clearly, given the operating range of the converter, an optimization is possible that yields the smallest total filter size.

The analysis of the two dual-bridge converter topologies has yielded interesting and fairly counterintuitive results in terms of overall system power density. It is not clear whether the resulting system, using transformer leakage inductances,gives higher power density than a conventional hard-switched dc/dc converter in which the leakage elements are parasitics. In order to examine these issues better, a fundamental component model of the system is invoked and analyzed next.

Fundamental Model Analysis

Conceptually, each of these circuits can be viewed as an inductor (the transformer leakage inductance) driven at either end by a controlled square-wave voltage source. The voltage sources are phase shifted from each other by a controlled angle ϕ. To simplify the analysis, the square-wave voltage sources are replaced by their fundamental components. Fig. 10 shows the fundamental model. Note that this model can also be treated as a per phase model for Topology C. The model is identified to the familiar synchronous-machine equivalent circuit and may be expected to demonstrate similar properties. The inductance L is analogous to the series inductance of the machine. The input (V_{fi}) and output (V'_{fo}) voltage sources can be viewed as the internal EMF and terminal voltage, respectively. The angle ϕ is commonly referred to as the torque angle. Since all circuit quantities are sinusoidal at a single frequency (the switching frequency), a phasor analysis can be carried out. The steady-state current phasor I through the inductor is given as

$$I = \frac{V_{fi} - V'_{fo}}{X_L} \tag{34}$$

where

$$V_{fi} = V_{fi}\langle 0\rangle$$
$$V'_{fo} = V'_{fo}\langle -\phi\rangle$$
$$X_L = j\omega L$$

and where ω = switching frequency. Note that for a square-wave input voltage of peak amplitude V_i, the rms fundamental component V_{fi} is given as

$$V_{fi} = \frac{2\sqrt{2}\ V_i}{\pi}.$$

Similarly, for the output,

$$V_{fo} = \frac{2\sqrt{2}\ V_o}{\pi}.$$

Hence, the output power is given as

$$\begin{aligned} P_o &= \mathrm{Re}\left[V'_{fo} I^*\right] \\ &= \frac{V_{fi} V'_{fo}}{\omega L}\sin(\phi) \\ &= \frac{V_{fi}^2}{\omega L} d \sin(\phi) \end{aligned} \tag{35}$$

where

$$d = \frac{V'_{fo}}{V_{fi}}.$$

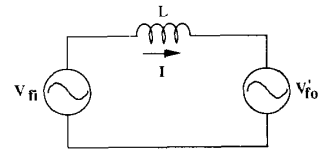


Fig. 10. Fundamental model of the dual bridge dc/dc converter.

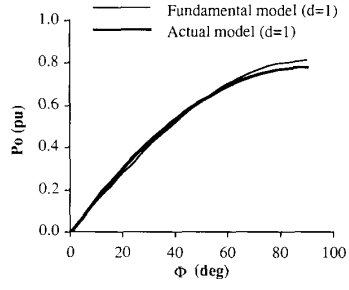


Fig. 11. Comparison of the output power versus ϕ, at $d = 1$, from the fundamental model and actual model.

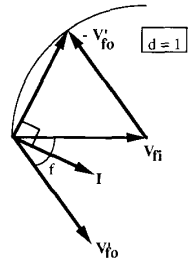


Fig. 12. Phasor diagram for the fundamental model illustrating the relative positions of the current and voltage phasors for soft switching at $d = 1$.

Equation (35) is identical to that for a synchronous machine. Fig. 11 shows a plot of the fundamental output power (normalized to the power base defined in (11) for $d = 1$. The actual output power for Topology B for $d = 1$ is also shown on the same figure. The good correlation justifies the validity of the fundamental model.

To appreciate the relationship between ϕ and d for soft-switching conditions, phasor diagrams based on the fundamental model can be very helpful. Again, as a reminder the soft-switching constraints dictate that the inductor current I lags the input voltage V_{fi} and leads the output voltage V_{fo}'. For instance, Fig. 12 shows the phasor diagram for $d = 1$. As ϕ is varied over the range 0–$\pi/2$, the current phasor, I always remains between the phasors V_{fi} and V_{fo}', thus satisfying the preceding soft-switching constraints for this entire range of ϕ. This conforms to our actual model.

Considering the issue of transformer size may also be easier in the fundamental model. First, let us evaluate the transformer kVA based on the fundamental model (for Topology B) from (9):

$$(\mathrm{kVA})_T = \frac{V_{fi}^2(1+d)}{2\omega L}\sqrt{d^2 - 2d\cos(\phi) + 1}. \tag{36}$$

Assume that for a given $(\mathrm{kVA})_T$, transformer size is inversely proportional to the frequency, given the core material. Given the task of designing a transformer for a conventional hard-switched dc/dc converter, one chooses $d = 1$ and L small for maximiz-

ing transformer utilization. This implies a small value for $\phi = \phi_h$. If this transformer is designed for frequency $\omega = \omega_h$, then from (35) and (36), one can derive

$$\omega_h L = X_L = \frac{V_{fi}^2}{P_o} \sin(\phi_h) \tag{37}$$

$$(\text{kVA})_{T(h)} = P_o \sec\left(\frac{\phi_h}{2}\right). \tag{38}$$

This is approximately equal to P_0 since ϕ_h is assumed small. Thus the transformer size for hard switching will be proportional to S_h, where

$$S_h = \frac{(\text{kVA})_{T(h)}}{\omega_h} = \frac{P_o}{\omega_h} \sec\left(\frac{\phi_h}{2}\right). \tag{39}$$

Similarly, examining the soft-switched converter, we can see that maximum power transfer occurs at $\phi = \phi_s = \pi/2$ and $d = 1$. Under these conditions and at a frequency ω_s, we find for the same ratings

$$\omega_s L = \frac{V_{fi}^2}{P_o} \tag{40}$$

$$(\text{kVA})_T = \sqrt{2}\, P_0 \tag{41}$$

$$S_s = \frac{(\text{kVA})_{T(s)}}{\omega_s} = \frac{\sqrt{2}\, P_o}{\omega_s}. \tag{42}$$

Comparing the sizes of the two transformers, we can see that

$$\frac{S_s}{S_h} = \frac{\sqrt{2} \sin(\phi_h)}{\sec\left(\frac{\phi_h}{2}\right)} \tag{43}$$

Since typical values for ϕ_h are in the 2°–10° range, it can be seen that significant reduction in transformer size is possible by switching to a scheme where the leakage inductances are the current transfer elements. This comparison is further strengthened when the losses resulting from interaction of diode reverse recovery and leakage inductance are considered for a current-source-output dc/dc converter.

Comparison of Proposed Converters

The three converters proposed have been presented in detail including sufficient information for the development of operating characteristics. In order to better compare the three topologies, Table I presents the detailed specifications for various components based on the equations and curves presented in the paper. The design is denormalized so as to conform to a specification of 50 kW with an input voltage of 200 Vdc, an output voltage of 2000 Vdc, and a switching frequency of 50 kHz. Optimum design points for each of the topologies are shown in the table

Examining peak device stresses, the three-phase dual bridge offers the lowest ($V_{ce}I_c$) stress at (1.17 *load kW) as opposed to a factor of 3.45 for Topology A. However, Topology B shows a slightly higher stress at 1.19 pu. Moreover, in Topology C the peak-device turn-off current is lower than the peak current in the transformer. Similar conclusions are seen from the transformer kVA ratings. Topology A exhibits poorest transformer utilization and very high current stresses. The total input and output filter requirements are seen to be lowest for Topology C, as expected, because of the higher ripple frequency. Overall, Topology C seems to be the most viable option for the application. However, the biggest disadvantage is the practical realization of a three-phase symmetrical transformer with identical leakage inductances in each phase [12]. Moreover, it requires two additional devices on each bridge as opposed to Topology B.

TABLE I
Summary of Component Stresses
(P_o = 50 kW; V_i = 200 Vdc; V_o = 2000 Vdc; f = 50 kHz)

	Topology A	Topology B	Topology C
d	0.58	1	1
β(°)	180	—	—
ϕ(°)	—	28.78	35.41
Device Specs.			
Input Bridge			
No. of Active Devices	4	4	6
Peak voltage (V)	200	200	200
Peak current (A)	861.48	297.57	293.46
$V_{pk} * I_{pk}/P_o$	3.45	1.19	1.17
Output Bridge			
No. of Active Devices	4 (diodes)	4	6
Peak voltage (V)	2000	2000	2000
Peak current (A)	50.68	29.76	29.35
$V_{pk} * I_{pk}/P_o$	2.03	1.19	1.17
Transformer Specs.			
1:N	1:17	1:10	1:10(Y-Y)
Peak pri. volts (V)	200	200	133/ph
Peak pri. amps (A)	861.48	297.57	293.46
RMS pri. amps (A)	497.52	281.4	197.29/ph
Peak sec. volts (V)	2000	2000	1333/ph
Peak sec. amps (A)	50.68	29.76	29.35
RMS sec. amps (A)	29.27	28.14	19.73/ph
kVA	78.64	56.28	55.7
P_o/kVA	0.64	0.89	0.89
L (μH)	0.77	1.1	0.89/ph
Filter Specs.			
Input			
Cap. volts (Vdc)	200	200	200
Cap. RMS amps (A)	429.75	129.15	48.43
kVA	85.95	25.83	9.69
Output			
Cap. volts (Vdc)	2000	2000	2000
Cap. RMS amps (A)	14.63	12.92	4.84
kVA	29.26	25.83	9.69
Operation	1-Quadrant	2-Quadrant	2-Quadrant

A value of L has been specified in order to attain the desired specifications. The actual choice of ω and L will depend on the core material and detailed transformer design. It is anticipated that limitations on transformer size minimization will be imposed by the weak scaling factors that govern how the leakage inductances reduce with size as operating frequency is increased. Although it has been shown that the dual-bridge converters are inherently capable of higher power density, Topology A has many desirable characteristics. For higher output voltages, where active devices may be unable to operate, diode rectifiers may be the only alternative along with topology A. Further, for applications where the reliability or cost penalties of additional gate turn-off devices is unacceptable, again Topology A may be the only viable option.

Experimental Results

An experimental proof-of-concept unit based on the proposed Topology B was fabricated in the laboratory using bipolar junction transistor as the switching device. The unit was rated for 1 kW for a switching frequency of 20 kHz. Fig. 13 shows the primary and secondary voltage and the primary current

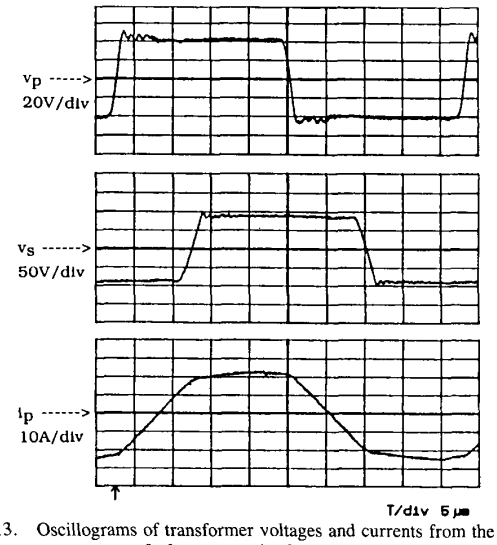


Fig. 13. Oscillograms of transformer voltages and currents from the 1-kW proof-of-concept unit of topology B.

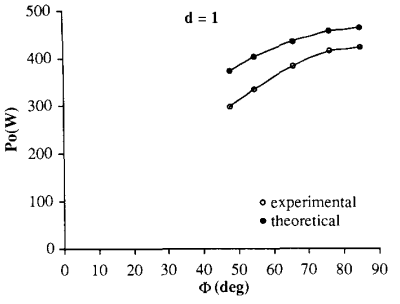


Fig. 14. Comparison of the experimental and theoretical output power versus ϕ characteristic at $d = 1$ for topology B.

waveforms for $d = 1$. The waveforms demonstrate the soft-switching capabilities for all the devices on both the bridges. Fig. 14 shows the variation in the output power with phase shift. The trend in the experimental curve is seen to closely match that of the theoretical. Output power increases as phase shift increases.

Conclusion

Three new dc/dc converter topologies suitable for high-power-density high-power applications have been presented in this paper. All three circuits operate in a soft-switched manner, making possible a reduction of device switching losses and an increase in switching frequency. Along with soft switching, all proposed circuits utilize the leakage reactance of the ac-link transformers as active current transfer elements and eliminate problems of interaction between these leakage inductances and diode reverse recovery. The dual-bridge topologies are also capable of buck-boost operation and bidirectional power flow, although that aspect has not been analyzed in detail in this paper.

The current transfer mode of operation makes it easier to parallel multiple modules for extending the power capacity of the system. The use of a three-phase ac-link system dramatically reduces the capacitor ripple currents, making it possible to use high-power-density multilayer ceramic capacitors. The dual-bridge converters are also seen to offer an unexpected gain in the power density attainable as a result of the controlled action of the two bridges. Since the snubbers used are purely capacitive, these would supplement the internal device capacitance, giving a clean power structure. The total number of system components is also seen to be minimal—the input and output filter capacitors, two bridges, and one transformer. All device and component parasitics are seen to be used favorably.

The dual-bridge topologies proposed have the most favorable characteristics including:

- small number of components
- low device and component stresses
- zero (or low) switching losses for all devices
- small filter components
- high efficiency (no trapped energy)
- bidirectional power flow
- buck-boost operation possible
- low sensitivity to system parasitics
- parallel operation possible as a result of current transfer.

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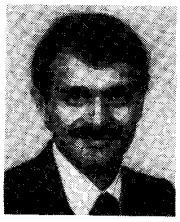

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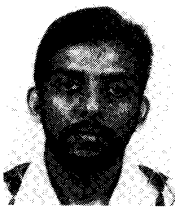

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