Group 5: a33abdul saflatou mosobase y433wu

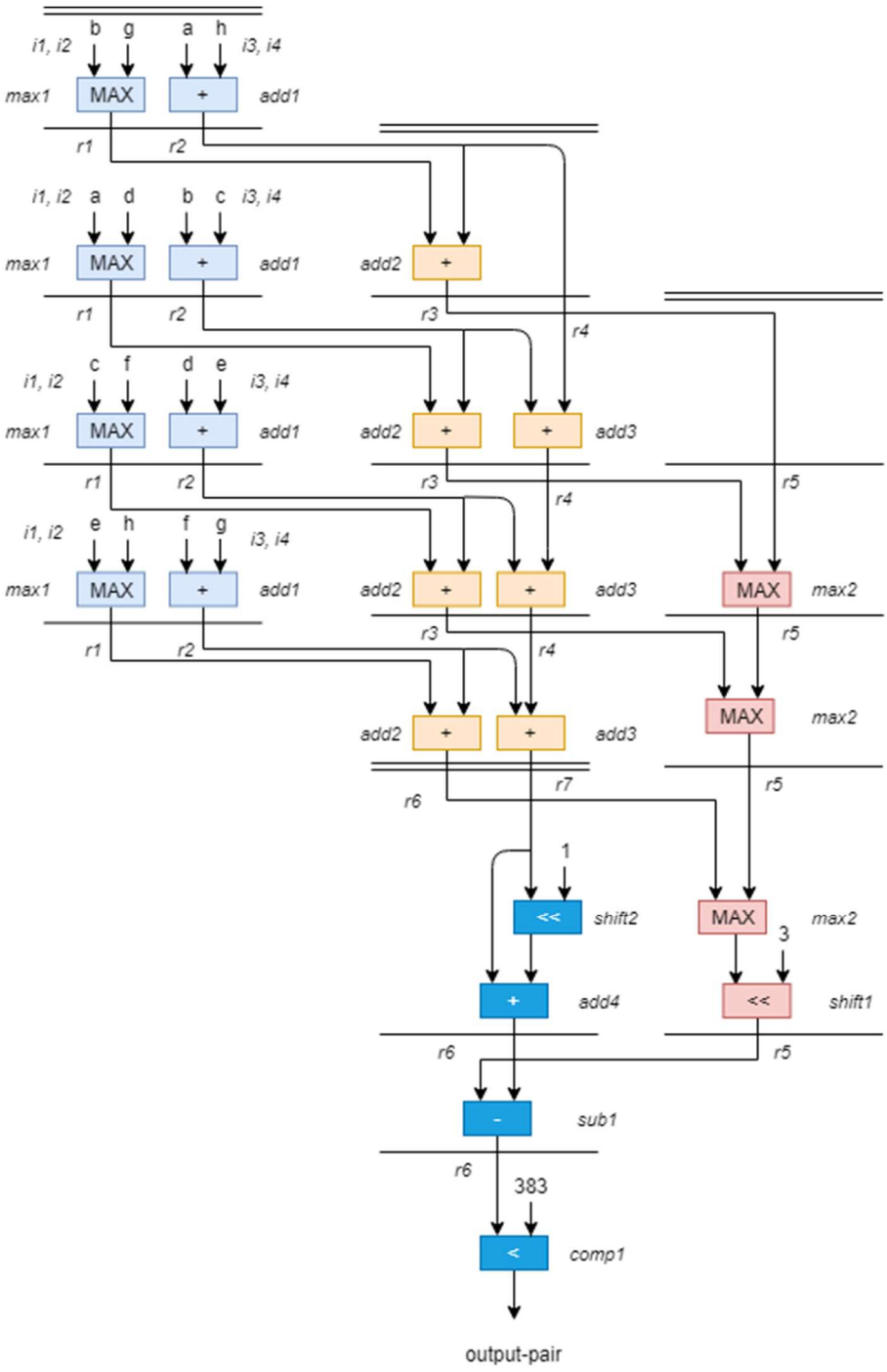

Fig-1: Dataflow Diagram Prelim Design

As demonstrated in Fig-1, we use overlap pipelining in our design. Each color represents a stage in the design.

Group 5: a33abdul saflatou mosobase y433wu

Slowest Operation:

We estimated that possible slowest operation(s) in our design are

- MAX operation (max1) + add operation
- MAX operation (max2) + shift operation
- Subtract operation

In addition, max2 does more comparisons than max1 due to the increasing bit size of input source to the MAX-operator.

Clock period:

$$Clock\ Period = FLOP + \max(MAX1 + ADD, MAX2 + SHIFT, SUB1)$$

Latency:

7

Throughput:

$\frac{1}{4}$

Datapath resources:

Inputs	4	Outputs	1
MAX operators	2	Shift operators	2
Adders	4	Subtracters	1
Registers	7	Comparator	1

Estimated Total Areas:

Notes:

1. Suppose 1 LUT for each register. 7 LUT for registers in total.

Stage 1 (light blue)

- All cycles have same configuration. For each cycle:
  - Need “mux on 1 input (treat `max` output as `sel`) with 8-bit wide data (1 adder)”: 16 LUT
  - Need “no mux with 8bit wide data (1 max)”: 4 LUT
- Total: 16 + 4 = 20 LUT

Stage 2 (light yellow)

- Suppose we use the most bit adders (last cycle of stage 2) for all cycles
- Need “no mux with 9-bit wide data”: 9 LUT, and “no mux with 11-bit wide data”: 11 LUT
- Total: 9 + 11 = 20 LUT

Stage 3 (light red)

- Shift operation does not take up extra area or delay time
- Cycle 2,3,4 needs "no mux with 10-bit wide data (1 max): 7 LUT
- Total: 7 LUT

Stage 4 (blue)

- Cycle 1 needs "no mux with 13-bit wide data (1 adder)": 13 LUT
- Cycle 2 needs "no mux with 14-bit wide data (1 subtractor)": 14 LUT
- Cycle 3 needs "no mux with 14-bit wide data (1 comparator)" : 8 LUT
- Total: 35 LUT

In total, we estimated that we need 20+20+7+35+7 = 99 FPGA cells

Optimality Goal:

High performance, with as less area as possible

Optimality Score:

- Assume our system meet functionality requirements
- Assume clock period = 2.41 ns (from 14-bit subtractor)

$$\text{Optimality} = \text{Functionality} \times \frac{Clock\ Speed}{Area} = 1000 * \frac{\frac{1}{2.41ns}}{99} = 1000 * \frac{414.9MHz}{99} = 4190$$

How Calculation Were Done:

1. List all formulas for the priority list: W, NW, N, NE, E, SE, S, SW.
    a. For example:
        i. $W = 5 \cdot (a + g + h) - 3 \cdot (b + c + d + e + f)$
        ii. $NW = 5 \cdot (a + b + h) - 3 \cdot (c + d + e + f + g)$
2. Group directions that have common signals and optimize by using provided equations
    a. For example:
        i. $W = 8 \cdot (a + g + h) - 3\big((a + g + h) + b + c + d + e + f\big)$
        $NW = 8 \cdot (a + b + h) - 3\big((a + b + h) + c + d + e + f + g\big)$
        ii. $\max(W, NW) = 8 \cdot (\max(b, g) + (a + h)) - 3 \cdot ((a + g + h + b) + c + d + e + f)$
3. Combine all formulas from step 2, we derived final equation:

$$8 \cdot \max[\max(b, g) + (a + h), \max(a, d) + (b + c), \max(c, f) + (d + e), \max(e, h) + (f + g)] -$$

$$3 \cdot (a + b + c + d + e + f + g + h)$$