2019 CAD Contest: LEF/DEF Based Global Routing
(Invited Paper)

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***Abstract*—In advanced nodes, routing has become more and more complicated. The ISPD-2018 and ISPD-2019 Initial Detailed Routing Contests [10][11] were held to bridge the detailed routing gap between academia and industry by releasing benchmarks using industry tool and libraries. The industry-standard LEF/DEF-based benchmark suite has inspired a new generation of large-scale academic implementations of detailed routing frameworks considering complex design rules. At the same time, efforts such as the OpenROAD [1] and the IEEE CEDA DATC Robust Design Flow (RDF) [3][8] projects aim to provide full RTL-to-GDS flows as the basis for academic research and improved academic-industry interfaces; the former project is moreover developed as open source. In these efforts, routing is clearly one of the most important stages. The ICCAD-2019 LEF/DEF-based open-source global routing contest revisits the global routing topic treated in the ISPD-2007 and ISPD-2008 contests [12][13], encouraging researchers to contribute open-source global routers that are industry-proven and well-correlated in advanced-node designs.**

I. Introduction

In advanced technology nodes, routing has become more and more complicated. There are not only hundreds of new vendor-dependent and foundry-dependent design rules, but also deep integration of design stages. Normally, routing is divided into two stages, global routing and detailed routing. In global routing, the routing resource is divided into 3D grids, each at a scale of tens of tracks in a given routing layer. A coarse routing is performed in a 3D grid graph to obtain an optimized topology and layer assignment considering routing resources. Later, the detailed routing stage realizes all physical wiring shapes, given the global routing solution as guidance.

The ISPD-2018 and ISPD-2019 Initial Detailed Routing Contests [10][11] were held to bridge the detailed routing gap between academia and industry by releasing benchmarks using industry tool and libraries. These contests' industry-standard LEF/DEF-based benchmark suites have inspired a new generation of large-scale academic implementations of detailed routing frameworks considering complex design rules.

The ISPD-2018 and ISPD-2019 contests have led to several new academic detailed routers. Dr. CU [4] [5] uses a sparse grid graph to store routing objects and prevent design rule violations; a minimum-area-captured path search is used to avoid minimum area violations. The work of [14] proposes a negotiation-based ripup-and-reroute flow. As reported in [9], TritonRoute uses a layer-by-layer mixed integer linear programming-based approach. Although still lagging behind any commercial products, these works have built a solid foundation for future academic research. In these contests, all global routing solutions are given as *route guides* generated from the commercial tool, with pre-optimized routing topology, congestion and timing. Similar to the advances in ISPD-2011, ISPD-2014 and ISPD-2015 contests as compared to ISPD-2005 and ISPD-2006 contests, where placers were required to additionally consider global and detailed routing, a natural extension of the detailed routing contest is to consider global routing as well. A modern global router should be optimized to correlate well with the detailed router. To achieve that tight correlation, accurate resource modeling considering pin accesses, existing power delivery networks (PDNs), blockages and design rules is increasingly required.

Recently, to encourage design data (and code sharing) in the EDA world, as well as provide a solid foundation for academic research and academia-industry interactions, both the IEEE CEDA DATC Robust Design Flow (RDF) [3][8] and the OpenROAD project [1] envision complete RTL-to-GDS flows. Especially, the OpenROAD project aims to enable an open platform, and ultimately a no-human-in-the-loop RTL-to-GDS infrastructure. In the OpenROAD project, the main place-and-route stages consist of (mixed-size) global and detailed placer RePlAce [6], with foundry node-tested timing-driven and congestion-driven capabilities; a clock-tree synthesis tool based on the generalized H-tree [7]; a global router and a detailed router TritonRoute [18]. This flow has achieved zero design rule violations for selected 65nm foundry node designs.

To further integrate and improve the OpenROAD or any other RTL-to-GDS academic flow, a better global routing framework is of clear interest, since the global router serves as an important bridge between *pre-route* and *post-route* stages. In pre-route stages, an ultra-fast global router is the key to enable frequent and accurate parasitic extraction and timing analysis in the placement-and-optimization loop. In route and post-route stages, correlation increasingly requires the global router to understand various physical contexts and design rules. This is especially true in advanced nodes, where the addition of multiple patterning, trim metals, complicated over-the-cell blockages and hundreds of new design rules make resource modeling much harder than in mature nodes.

In light of the above, we host the ICCAD-2019 global routing contest to address real-world challenges and, for the first time, directly encourage codes to be released under a permissive open-source license [19][20]. The contest highlights are listed below:

- To the best of our knowledge, this is the first global routing contest with "resource abstraction" in the to-do list for contestants, rather than given as capacity and edge adjustments. The benchmark suite is selected and derived from ISPD-2018 and ISPD-2019 Initial Detailed Routing contests, using industry-standard LEF/DEF formats. Contestants need to figure out pin accesses and various blockage effects based on physical metal shapes and design rules – all from the raw inputs – to achieve accurate resource modeling.
- To the best of our knowledge, this is the first global routing contest that uses an academic detailed router as part of the evaluation process. Rather than comparing abstracted overflow metrics, we directly compare detailed routing results obtained using the latest version of an ISPD-2019 contest winning detailed router, with official ISPD-2018 and ISPD-2019 contest metrics to encourage better correlation to the end of the flow.
- This contest provides incentives to encourage code release under a permissive open-source license.

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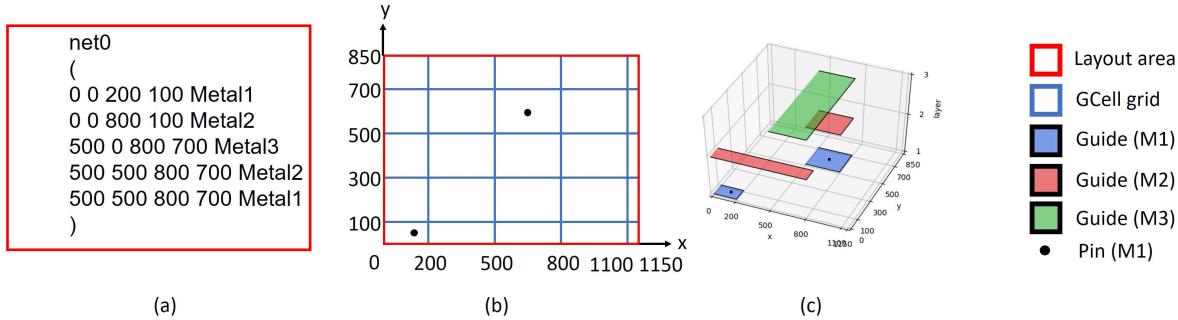

Fig. 1. Illustration of route guide: (a) route guide for *net0*; (b) 2D view of GCELLGRID and two pins of *net0*; and (c) 3D view of the route guides for *net0*.

The remainder of this paper is organized as follows. Section II provides an overview of problem description and contest requirements. Section III presents benchmarks. Section IV describes evaluation methodology. Section V details the open-source bonus and concludes the paper.

II. Overview

In this section, we provide an overview of the contest, including the problem description, input and output formats, and output requirements.

A. Problem Description

In global routing, the routing region is divided into rectangular grid cells (*GCells*). Based on the given GCells, the global router could build a coarse-grained 3D routing graph. Capacities and various constraints could be assigned to the edges and vertices in this 3D routing graph so that overall routing topology and layer assignment can be optimized considering routability, timing, crosstalk, power, etc. In this contest, to simplify the problem, we assume that a placement solution is already well-optimized for multiple metrics (e.g., timing, power, etc.). The global router only needs to provide a 3D global routing solution optimizing wirelength, via count, routability, pin accessibility, etc. to ensure design rule check (DRC) convergence with minimized disturbance of net topology during detailed routing.

For each testcase, the global router starts with a placed design, and generates a global routing solution. The global routing solution is then detail-routed by an academic detailed router and evaluated by official ISPD-2018 and ISPD-2019 evaluation scripts.

B. Input

For each testcase, the inputs are placed DEF and LEF files. The DEF file includes CORE/ROW/TRACKS/GCELLGRID definitions, placed COMPONENTS, fixed SPECIALNETS and unrouted NETS. The LEF file includes MACRO definition and technology information. Unlike the ISPD-2018/2019 contests, in this global routing contest, we specify GCells by utilizing the definition from the DEF GCELLGRID section. Figure 2(a) describes the GCELLGRID section, and Figure 2(b) illustrates the defined 2D GCELLGRID. Compared to previous global routing contests [12][13], one major difference lies in how the global router models the resource. In ISPD-2007 and ISPD-2008 global routing contests, testcases come with already-abstracted capacity and adjustments. However, the abstraction itself is one of the key components in an industry router. Thus, in this contest, contestants need to understand pin shapes, cell obstructions and pre-routed (wide) PDN nets in order to obtain the most precise resource modeling. Moreover, resources could also be adjusted given different LEF rules and vias to better correlate with the detailed router.

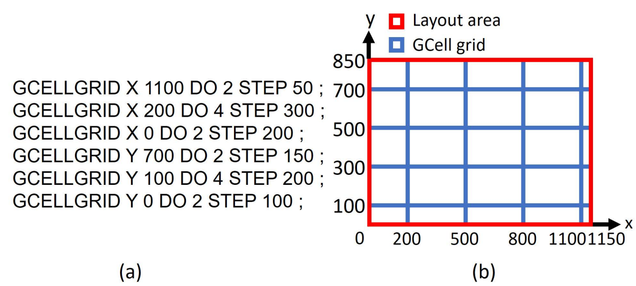

Fig. 2. GCELLGRID: (a) definition and (b) illustration.

C. Output

The output file format follows the ISPD-2018/2019 route guide format. This choice of output format is intended to enable seamless integration with academic detailed routers developed for the ISPD-2018/2019 contests.

In the route guide format, the global routing solution for a net consists of several guides. Each guide is a rectangle on a specific metal layer, covering one or multiple contiguous GCells. To be consistent with our GCELLGRID definition, we make the following restrictions to each guide:

- If a GCell is covered by a guide, the guide *must* cover that entire GCell area, and *not* just part of that GCell area.
- *Only* guides on metal layers (i.e., TYPE ROUTING in LEF) are needed. Guides on via layers (i.e., TYPE CUT in LEF) are skipped.

A global routing solution for a net is considered to be valid if

- All pins (i.e., instance terms and IO terms) of the net are covered by its guides. Here, "covered by" means that for each pin of the net, at least one shape of the pin and one guide of the net are on the same metal layer, with *non-zero* overlapping area.
- A connected graph can be derived for the net given the global routing solution. Pins and guides correspond to vertices in the graph. An edge exists between two guides if either of the following two conditions is satisfied: (i) they touch each other on the same metal layer with *non-zero* overlapping length or area; (ii) they are on neighboring metal layers with a *non-zero* overlapping area (projected to x-y plane). An edge between a guide and a pin exists if the pin is covered by the guide.

Figure 3 illustrates four possible scenarios relevant to the above definitions. In Figure 3(d), if the right guide extends into the left guide, they are also considered connected due to non-zero overlapping area.

TABLE I
BENCHMARK INFORMATION.

Benchmark	#std	#blk	#net	#pin	#layer	GCell
ispd18_test5	71954	0	72394	1211	9	15×15
ispd18_test8	191987	16	179863	1211	9	15×15
ispd18_test10	290386	0	182000	1211	9	15×15
ispd19_test7	359746	16	358720	2216	9	15×15
ispd19_test8	539611	16	537577	3221	9	15×15
ispd19_test9	899341	16	895252	3221	9	15×15
ispd18_test5_metal5	71954	0	72394	1211	5	15×15
ispd18_test8_metal5	191987	16	179863	1211	5	15×15
ispd18_test10_metal5	290386	0	182000	1211	5	15×15
ispd19_test7_metal5	359746	16	358720	2216	5	15×15
ispd19_test8_metal5	539611	16	537577	3221	5	15×15
ispd19_test9_metal5	899341	16	895252	3221	5	15×15

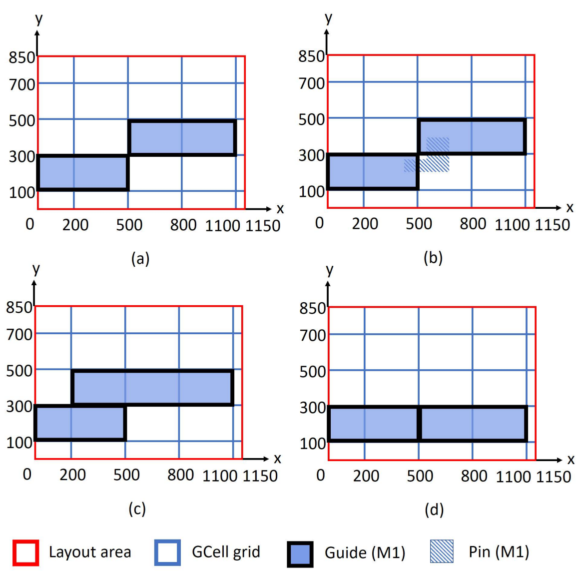

Fig. 3. Illustration of guide connectivity: (a) guides are disjoint due to zero overlapping length; (b) guides are connected due to pin feedthrough; (c) guides are connected due to non-zero overlapping length along horizontal direction; and (d) guides are connected due to non-zero overlapping length along vertical direction.

A global routing solution is considered to be valid if the solution is valid for all of the nets. Figure 1 illustrates the route guide syntax, and 2D and 3D views, for one valid route guide solution of a net, $net0$.

III. BENCHMARKS

Six medium to large testcases are selected from ISPD-2018 and ISPD-2019 benchmark suites as the *released* contest testcases. The route guide files are removed and GCELLGRID definitions are added. These designs range from 72K nets to 895K nets in 32nm technology and cell libraries. Another six testcases are derived by restricting the number of metal layers, with IO pins redistributed only on the lower metal layers to form the *hidden* testcases. These hidden testcases have fewer routing resources, thus putting more stress on the router.

For each testcase, to form the GCELLGRID we extract the most common guide offset and guide widths (in both directions, separately) across all metal layers from the ISPD-given route guide file. The most common offset is set as the starting coordinate of the first GCell. The most common widths are set as the width and height of each GCell to form regular GCell patterns. The first and the last grid lines are always adjusted so that they align with the die boundary, thus covering the entire routing region.

Table I summarizes the statistics of each testcase. GCell size is described in units of Metal2 pitch. Testcases use 32nm cell library and technology, but may have slightly different design rules. Testcases may have 2D pin shapes, standard cell and macro blockages, and pre-routed non-default-width PDN with via arrays. We believe the above benchmark suite covers a wide range of scenarios observed in industry designs.

IV. EVALUATION

In previous global routing contests, results were mostly evaluated at the end of global routing, by generic metrics such as total overflow, max overflow and global routing wirelength. While these metrics can be obtained directly from the global routing solution, such evaluation may not correlate well with a specific detailed router and technology, especially when blockages, vias and design rules need to be modeled more precisely throughout the flow. To better evaluate and bridge the gap between global routing and detailed routing, we evaluate the solution at the end of detailed routing. Specifically, the global routing solution is detail-routed using the latest version of the ISPD-2019 contest-winning detailed router Dr. CU [16], and evaluated and ranked following similar criteria as in the ISPD-2018 and ISPD-2019 contests. A valid global routing solution requires that the detailed router generates a detail-routed DEF with no open nets.

After detailed routing, each solution is evaluated using *Cadence Innovus Implementation System* [15] and ISPD-2018/2019 evaluation scripts to obtain a raw score. The raw score is a weighted sum of all entries listed in Table II, representing the quality of the detailed routing solution.[1]

The final scaled score for each testcase is calculated using Equation (1). The non-deterministic penalty $np = 0.03$ is applied if the global router generates different route guides among a total of three runs. In such a case, the median scaled score is used. The runtime factor rf is applied to scale the raw score according to Equation (2). rwt is the sum of global and detailed routing runtimes. mwt is the averaged sum of global and detailed routing runtimes across all teams. Equations (1) and (2) are the same as in the ISPD-2019 contest except that the runtime now takes both global and detailed routing into account.

[1] According to the ISPD contest metric, number of shorted metal / cut is not applied in ISPD-2018 testcases. The weights for total number of single-cut vias are 2 and 4 for ISPD-2018 and ISPD-2019 testcases, respectively. Total number of multi-cut vias is not applied because the detailed router used for evaluation does not generate multi-cut vias.

TABLE II
EVALUATION METRICS.

Metric	Weight
Shorted metal / cut area	500
Number of shorted metal / cut	500
Number of min-area violations	500
Number of parallel run length violations	500
Number of EOL spacing violations	500
Number of cut spacing violations	500
Number of corner spacing violations	500
Total length of out-of-guide wires	1
Total number of out-of-guide vias	1
Total length of off-track wires	0.5
Total number of off-track vias	1
Total length of wrong-way wires	1
Total number of single-cut vias	2 / 4
Total length of wires	0.5

$$scaled\_score = raw\_score \times (1 + np + rf) \tag{1}$$

$$rf = \min(0.1, \max(-0.1, 0.02 \cdot \log_2 \frac{rwt}{mwt})) \tag{2}$$

V. OPEN-SOURCE BONUS

To the best of our knowledge, the ICCAD-2019 global routing contest is the first physical design contest that awards an open-source bonus if teams release their code under a permissive open-source license [19][20] before, or at the time of, the announcement of results. In this particular aspect, the contest is enlightened by the initial efforts made in the OpenROAD project [1][17] towards an open-source and end-to-end silicon compiler. The development of this flow has numerous technical and cultural challenges. The end-to-end flow not only needs to integrate every individual stage from RTL to GDS, but also needs to be built upon a unified platform (database) to support timing, power and parasitic analysis. In this way, the OpenROAD project largely differs from any individual academic work. We see the present global routing contest and the OpenROAD project as sharing a common underlying philosophy:

- The individual tool needs to support industry-standard contents, either through platform APIs or direct LEF/DEF file inputs instead of academic formats [2]. The problem abstraction and heuristic decisions depend on the raw input data, as part of the tool flow, rather than as part of the inputs.
- The tool needs to be designed to be robust given a wide variety of input syntax.
- The algorithm needs to be developed towards a good outcome at the end of the flow, rather than a good intermediate solution at the end of the individual tool stage.

Given the above, we believe that an open-source global router contest, using LEF/DEF based inputs and evaluated with academic detailed router, is one of the first steps for collaboration towards an open platform for both commercial and non-commercial users and researchers around the world.

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