NEXTW

ECM-XF

EtherCAT Master Controller

Description

ECM-XF is a cost-effective EtherCAT master chip. It is connected to the master terminal through the SPI interface to help users achieve EtherCAT communication, reaching a minimum DC cycle time of 125us and maximum 128 EtherCAT Slaves. The minimum DC cycle time is 125us and the ability to connect up to 128 slave stations. It has a variety of peripheral IO, interrupt and application function, suitable for PLC controller, robot controller and various automation controllers.

Feature

EtherCAT

- Supports maximum 128 EtherCAT Slaves
- Supports minimum 125us DC cycle time
- Supports DCM Master Shift mode

Ethernet MAC Controller

- 100 Mbps data transmission
- Supports RMII interface

SPI Interface

- Supports full duplex slave mode
- MSB first transfer fashion
- Clock frequency up to 96 MHz

GPIO

- 20 general purpose inputs/outputs
- I/O pins can be configured as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode.

QEI

- a set of Quadrature Encoder Interface
- 32-bit
- 24MHz input frequency

DAC

- 1 Digital-to-Analog output
- Supports 12-bit output mode
- Rail to rail settle time 8us.

ADC

- 1 Analog-to-Digital input
- ADC clock frequency is up to 72 MHz
- Sampling rate is up to 5.14 MSPS
- 12-bit resolution

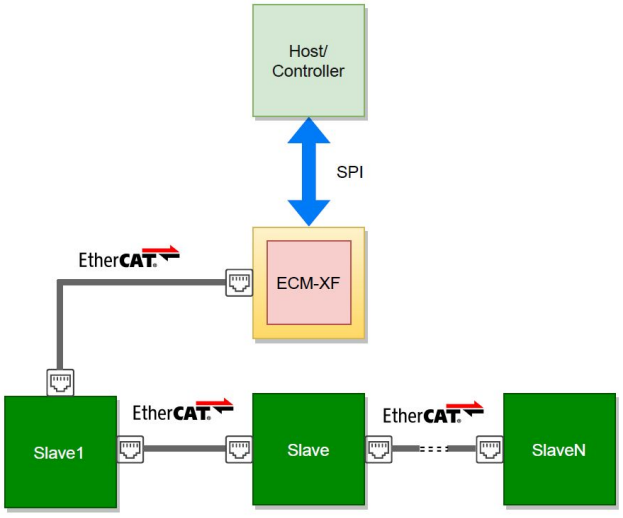
Temperature

- Operating Temperature -40℃ ~ +105℃

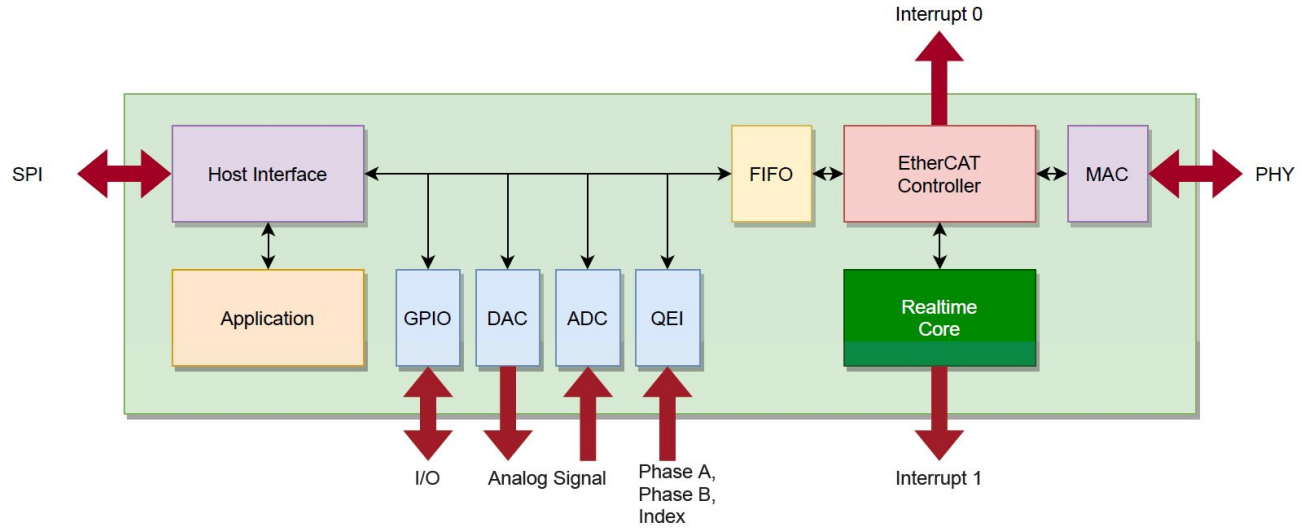
Application

PLC / CNC
Robot
Automation

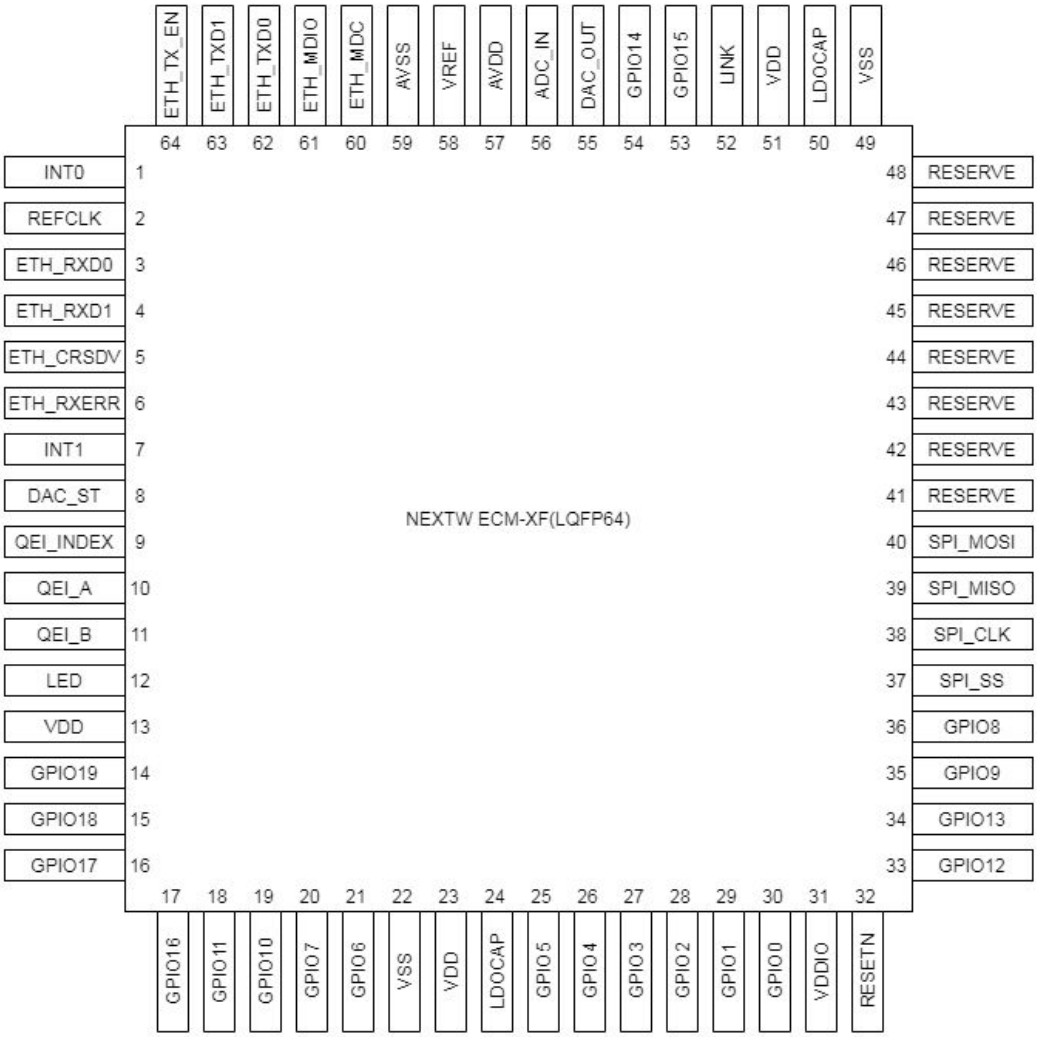
Typical Applications Diagram



Block Diagram



Pinout Diagram



Signal Description

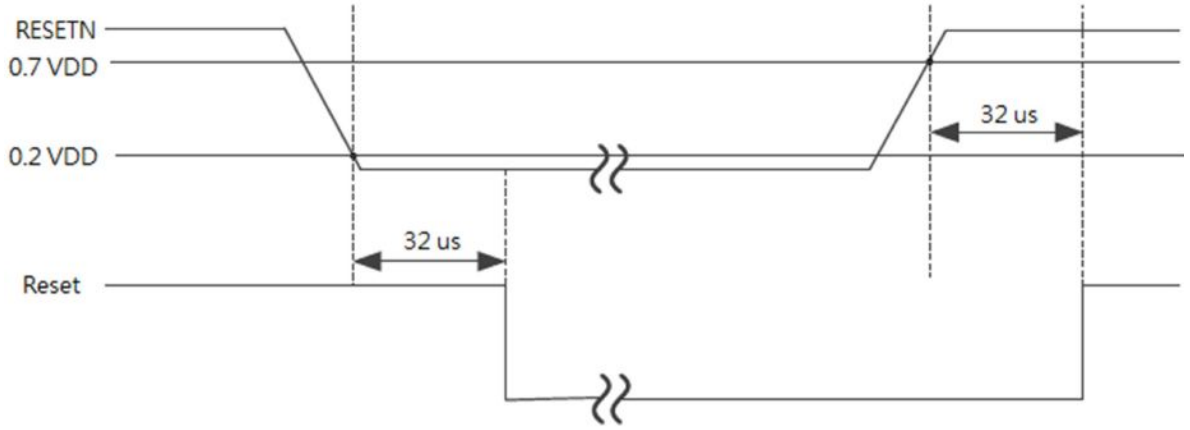
Pin	Name	Type	Description
1	INT0	O	Interrupt out pin 0.
2	REFCLK	I	EMAC RMII reference clock input pin.
3	ETH_RXD0	I	EMAC RMII receive data bus bit 0.
4	ETH_RXD1	I	EMAC RMII receive data bus bit 1.
5	ETH_CRSDV	I	EMAC RMII carrier sense/receive data input pin.
6	ETH_RXERR	I	EMAC RMII receive data error input pin.
7	INT1	O	Interrupt out pin 1.
8	DAC_ST	I	DAC external trigger Input.
9	QEI_INDEX	I	Quadrature Encoder Interface Index
10	QEI_A	I	Quadrature Encoder Interface Phase A.
11	QEI_B	I	Quadrature Encoder Interface Phase B.
12	LED	I/O	LED output.
13	VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
14	GPIO19	I/O	General purpose digital input/output pin19.
15	GPIO18	I/O	General purpose digital input/output pin18.
16	GPIO17	I/O	General purpose digital input/output pin17.
17	GPIO16	I/O	General purpose digital input/output pin16.
18	GPIO11	I/O	General purpose digital input/output pin11.
19	GPIO10	I/O	General purpose digital input/output pin10.
20	GPIO7	I/O	General purpose digital input/output pin7.
21	GPIO6	I/O	General purpose digital input/output pin6.
22	VSS	P	Ground pin for digital circuit.
23	VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
24	LDOCAP	P	LDO output pin.
25	GPIO5	I/O	General purpose digital input/output pin5.
26	GPIO4	I/O	General purpose digital input/output pin4.
27	GPIO3	I/O	General purpose digital input/output pin3.
28	GPIO2	I/O	General purpose digital input/output pin2.
29	GPIO1	I/O	General purpose digital input/output pin1.
30	GPIO0	I/O	General purpose digital input/output pin0.
31	VDDIO	P	Power supply for I/O ports.
32	RESETN	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
33	GPIO12	I/O	General purpose digital input/output pin12.
34	GPIO13	I/O	General purpose digital input/output pin13.
35	GPIO9	I/O	General purpose digital input/output pin9.
36	GPIO8	I/O	General purpose digital input/output pin8.

37	SPI_SS	I	SPI slave select pin.
38	SPI_CLK	I	SPI serial clock pin.
39	SPI_MISO	O	SPI MISO (Master In, Slave Out) pin.
40	SPI_MOSI	I	SPI MOSI (Master Out, Slave In) pin.
41	RESERVE	-	-
42	RESERVE	-	-
43	RESERVE	-	-
44	RESERVE	-	-
45	RESERVE	-	-
46	RESERVE	-	-
47	RESERVE	-	-
48	RESERVE	-	-
49	VSS	P	Ground pin for digital circuit.
50	LDOCAP	P	LDO output pin.
51	VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
52	LINK	I	Ethernet 100M Link Connection.
53	GPIO15	I/O	General purpose digital input/output pin15.
54	GPIO14	I/O	General purpose digital input/output pin14.
55	DAC_OUT	O	Digital to analog output.
56	ADC_IN	I	Analog to digital input.
57	AVDD	P	Power supply for internal analog circuit.
58	VREF	P	Voltage reference.
59	AVSS	P	Ground pin for analog circuit.
60	ETH_MDC	O	EMAC RMII PHY Management Clock output pin.
61	ETH_MDIO	I/O	EMAC RMII PHY Management Data pin.
62	ETH_TXD0	O	EMAC RMII Transmit Data bus bit 0.
63	ETH_TXD1	O	EMAC RMII Transmit Data bus bit 1.
64	ETH_TX_EN	O	EMAC RMII Transmit Enable output pin.

FUNCTIONAL DESCRIPTION

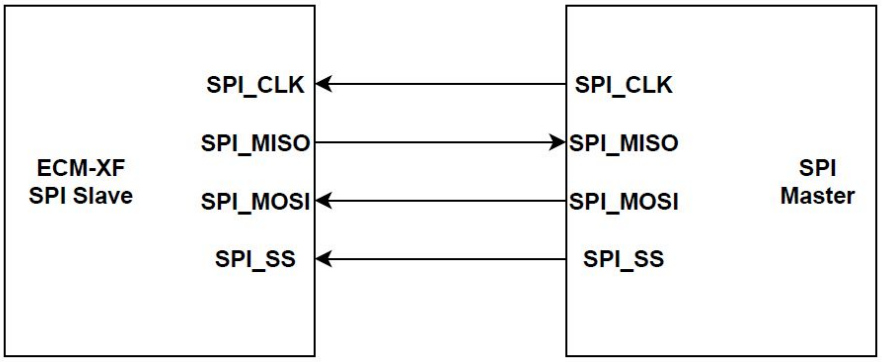
Reset

A reset signal by pulling low RESETN pin can be used to reset system at any time. When the RESETN voltage is lower than 0.2VDD and the state keeps longer than 32 us, the ECM-XF will be reset. It will be in reset state until the RESETN voltage rises above 0.7VDD and the state keeps longer than 32 us.

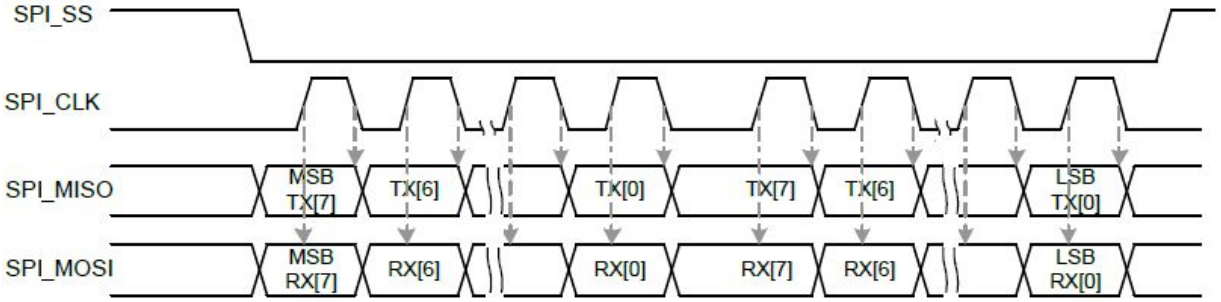


SPI

ECM-XF supports full duplex transfer in the slave mode with the 4-wire bi-direction interface.

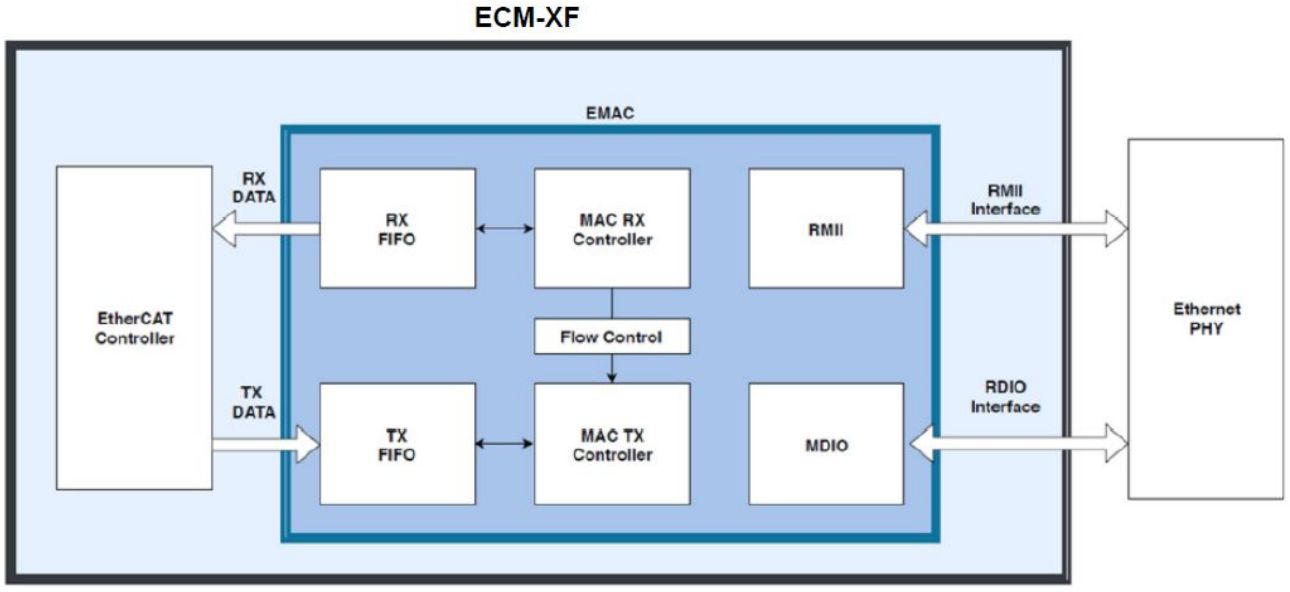


ECM-XF transmits/receives data with the most-significant bit (MSB) first. The edge of SPI clock to transmit/receive is shown below.



Ethernet MAC Controller

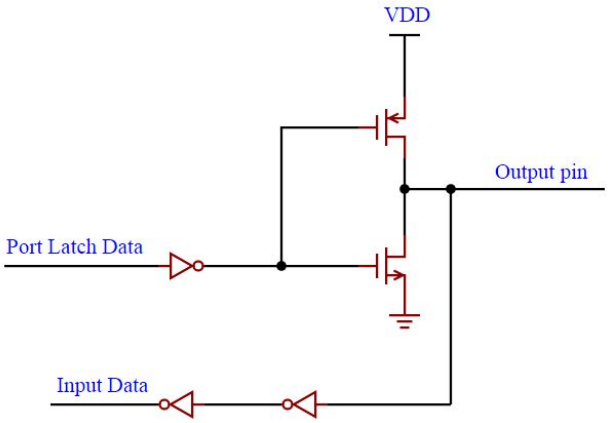
The EMAC controller of ECM-XF supports Reduced MII (RMII) interface to connect with external Ethernet PHY and provides TX/RX data transfer to the EtherCAT controller internally.



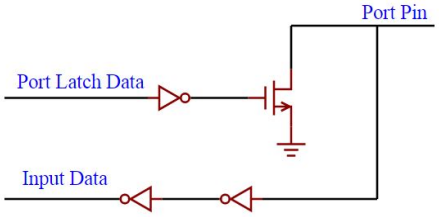
GPIO

ECM-XF has 20 general purpose pins. I/O pins can be configured as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. Users can control the LOW or HIGH level outputs by the host interface. ECM-XF also has 20 general purpose input/ouput pins with high impedance. When input signals are LOW or HIGH level, users can get the values through the host interface.

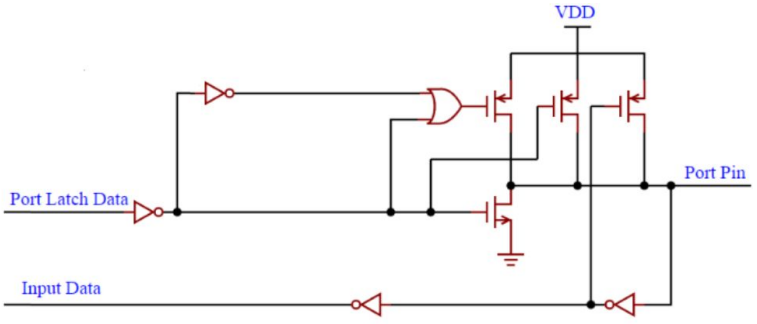
Push-pull Output Mode



Open-drain Mode



Quasi-bidirectional Mode



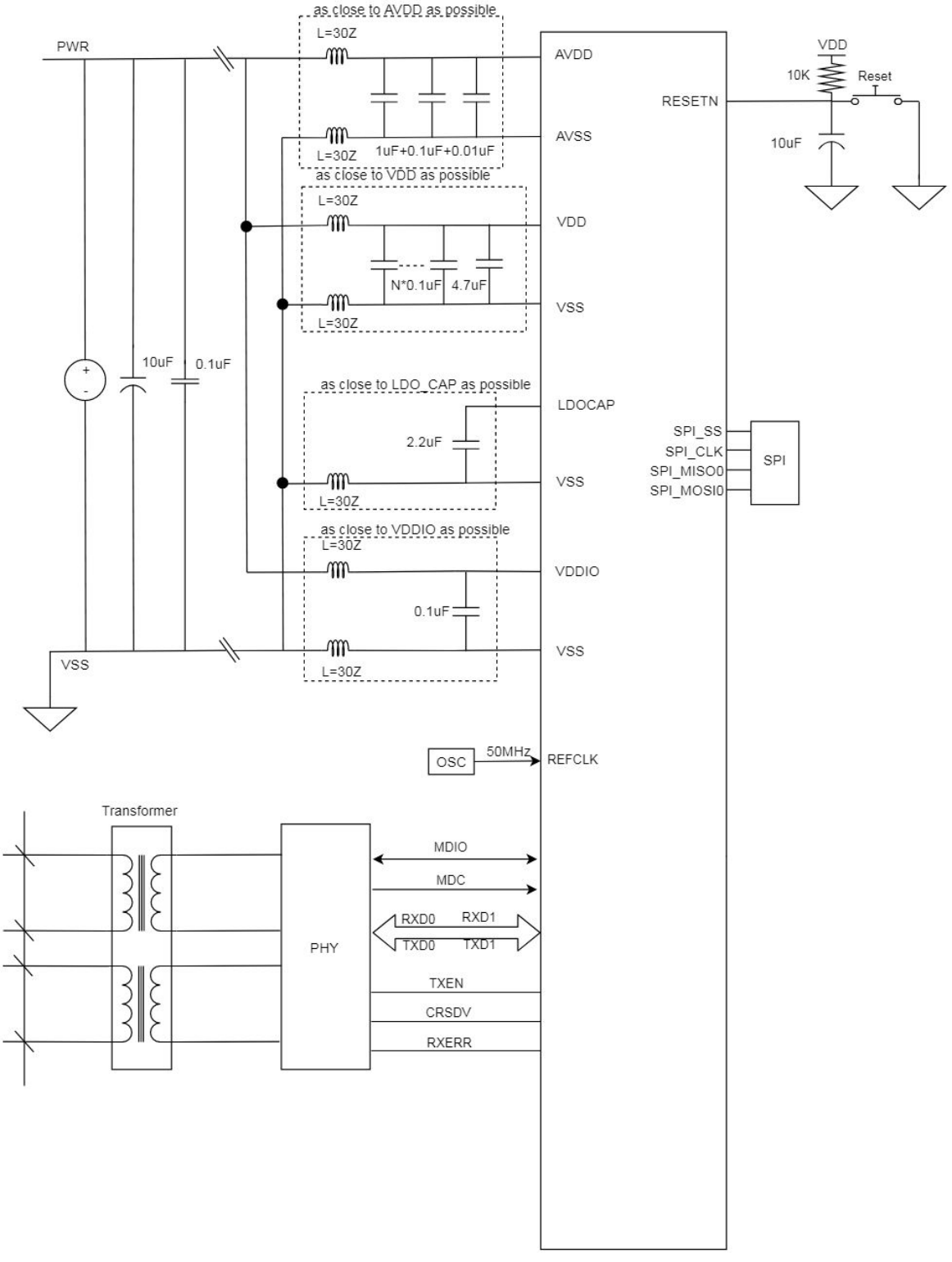
LED Indicator

The LED Indicators can show the state of SPI CRC Error.

LED	L	Initial power on or CRC Error.
	H	if SPI is connected and CRC NO Error.

L: Low, H: High

APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS

Voltage Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VDD	Operation voltage	1.8	3.3	3.6	V
VDDIO	Power supply for GPIO	1.8	3.3	3.6	
LDO_CAP	LDO output voltage	1.08	1.2	1.32	
VREF	Reference supply voltage	1.5	-	AVDD	
AVDD	Analog operation voltage	1.8	-	3.6	V

Current Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
IDD	Maximum current into VDD		200	mA
IDDIO	Maximum current into VDDIO		100	
ISS	Maximum current out of VSS		100	

Analog Characteristics

DAC

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
NR	Resolution		12		bit
VO	Output Voltage	0.2	-	AVDD - 0.2	V

ADC

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
NR	Resolution		12		bit
VIN	ADC channel input voltage	0	-	VREF	V

DC Characteristics

GPIO

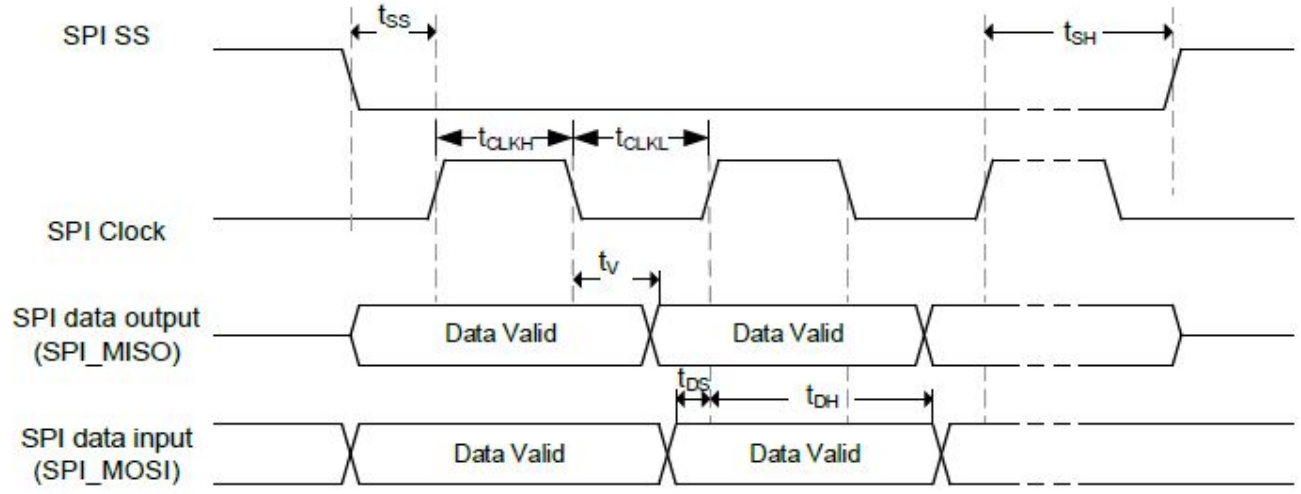
PARAMETER	MIN	TYP	MAX	UNIT	Test Conditions
Input Low voltage			0.8	V	VDD = VDDIO = 3.6 V
Input High voltage	2			V	VDD = VDDIO = 3.6 V
Output source current		-18		mA	VDD = VDDIO = 3.3 V
Output sink current		17		mA	VDD = VDDIO = 3.3 V

RESETN

PARAMETER	MIN	TYP	MAX	UNIT	Test Conditions
Negative going threshold (Schmitt input),			0.3 VDD	V	VDD = 3.3V
Positive going threshold (Schmitt Input)	0.7 VDD				VDD = 3.3V
Internal RESETN input filtered time pin pull up resistor		50		KΩ	
RESETN input filtered time		32		us	

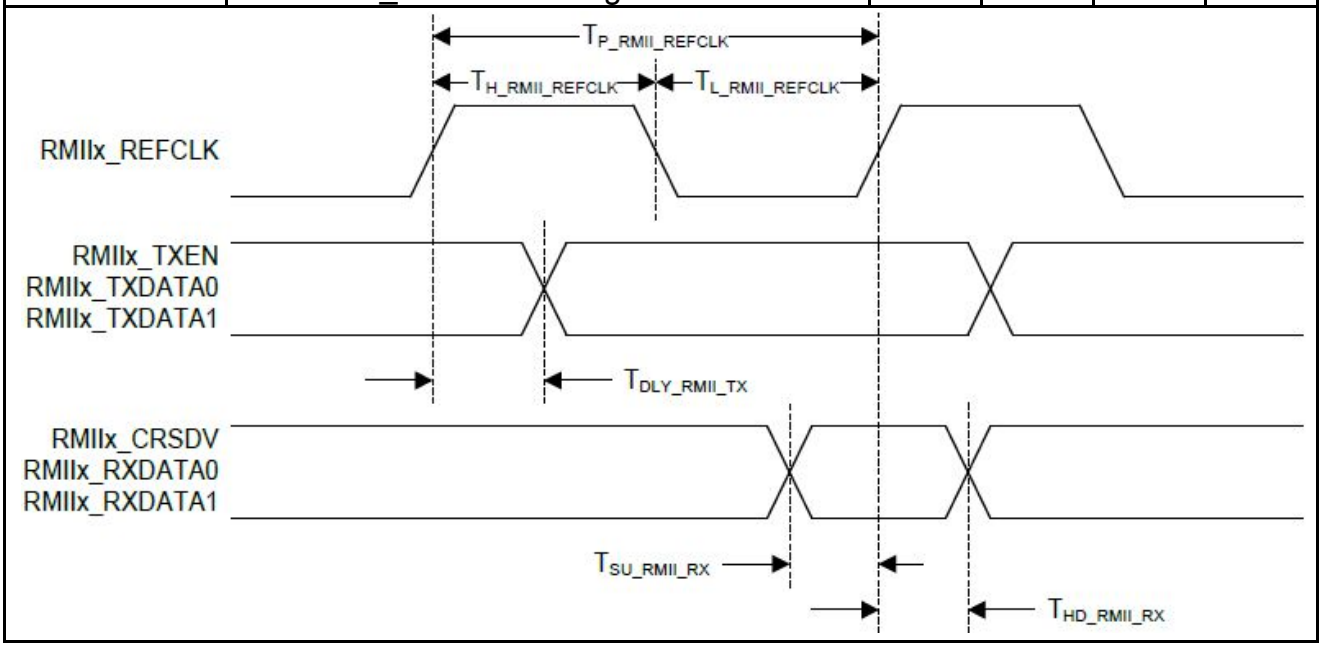
SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{CLKH}	Clock output High time			$T_{SPICLK}/2$	ns
t_{CLKL}	Clock output Low time			$T_{SPICLK}/2$	
T_{SS}	Slave select setup time	$T_{SPICLK}+2$			
T_{SH}	Slave select hold time	T_{SPICLK}			
T_{DS}	Data input setup time	0			
T_{DH}	Data input hold time	2			
T_V	Data output valid time			8	



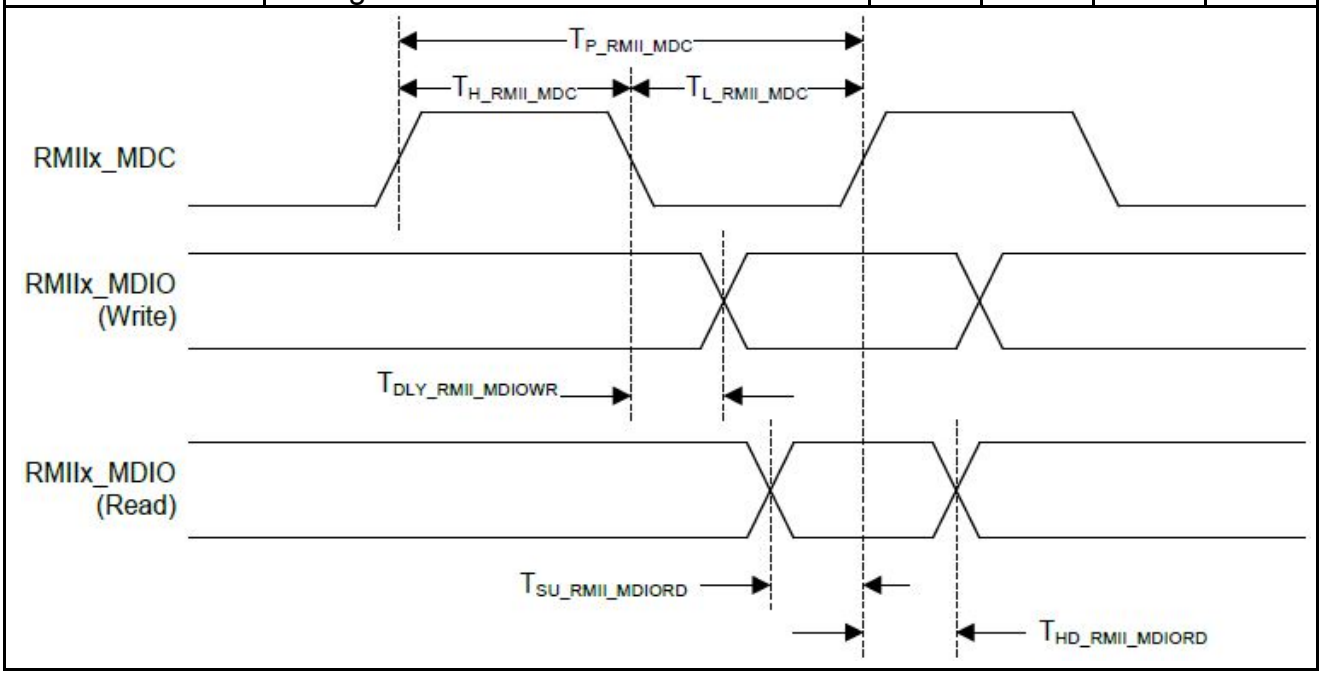
RMII Interface Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$T_{P\_RMII\_REFCLK}$	RMII_REFCLK Period		20.0 +/- 50 ppm		ns
$T_{H\_RMII\_REFCLK}$	RMII_REFCLK High Time	8.0	10.0	12.0	
$T_{L\_RMII\_REFCLK}$	RMII_REFCLK Low Time	8.0	10.0	12.0	
$T_{DLY\_RMII\_TX}$	RMII_REFCLK Rising to Valid RMII_TXEN, RMII_TXDATA0 and RMII_TXDATA1 Delay			10	
$T_{SU\_RMII\_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Setup Time to RMII_REFCLK Rising	5			
$T_{HD\_RMII\_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Hold Time from RMII_REFCLK Rising	2			

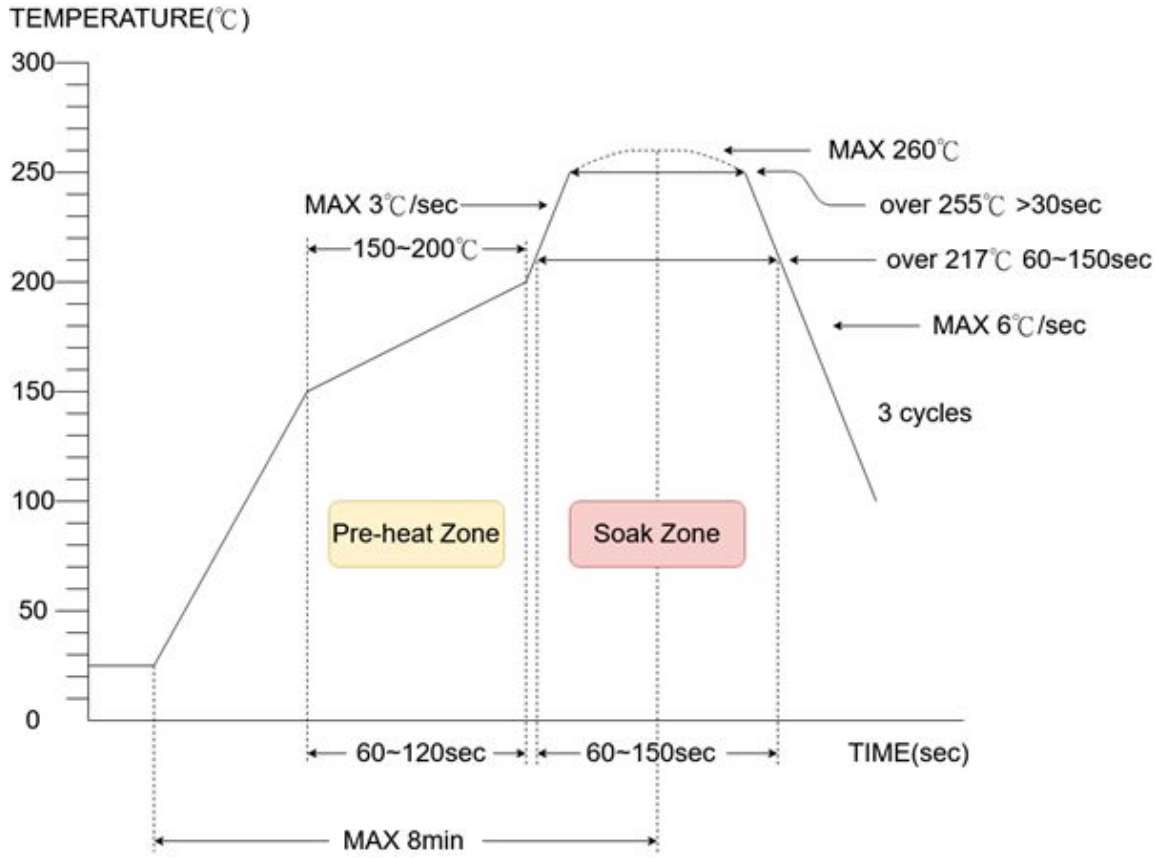


Ethernet PHY Management Interface Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$T_{P\_RMII\_MDC}$	RMII_MDC Period	400			ns
$T_{H\_RMII\_MDC}$	RMII_MDC High Time	200			
$T_{L\_RMII\_MDC}$	RMII_MDC Low Time	200			
$T_{DLY\_RMII\_MDIOWR}$	RMII_MDC Falling to Valid RMII_MDIO Delay			10	
$T_{SU\_RMII\_MDIORD}$	RMII_MDIO Setup Time to RMII_MDC Rising	10			
$T_{HD\_RMII\_MDIORD}$	RMII_MDIO Hold Time from RMII_MDC Rising	10			



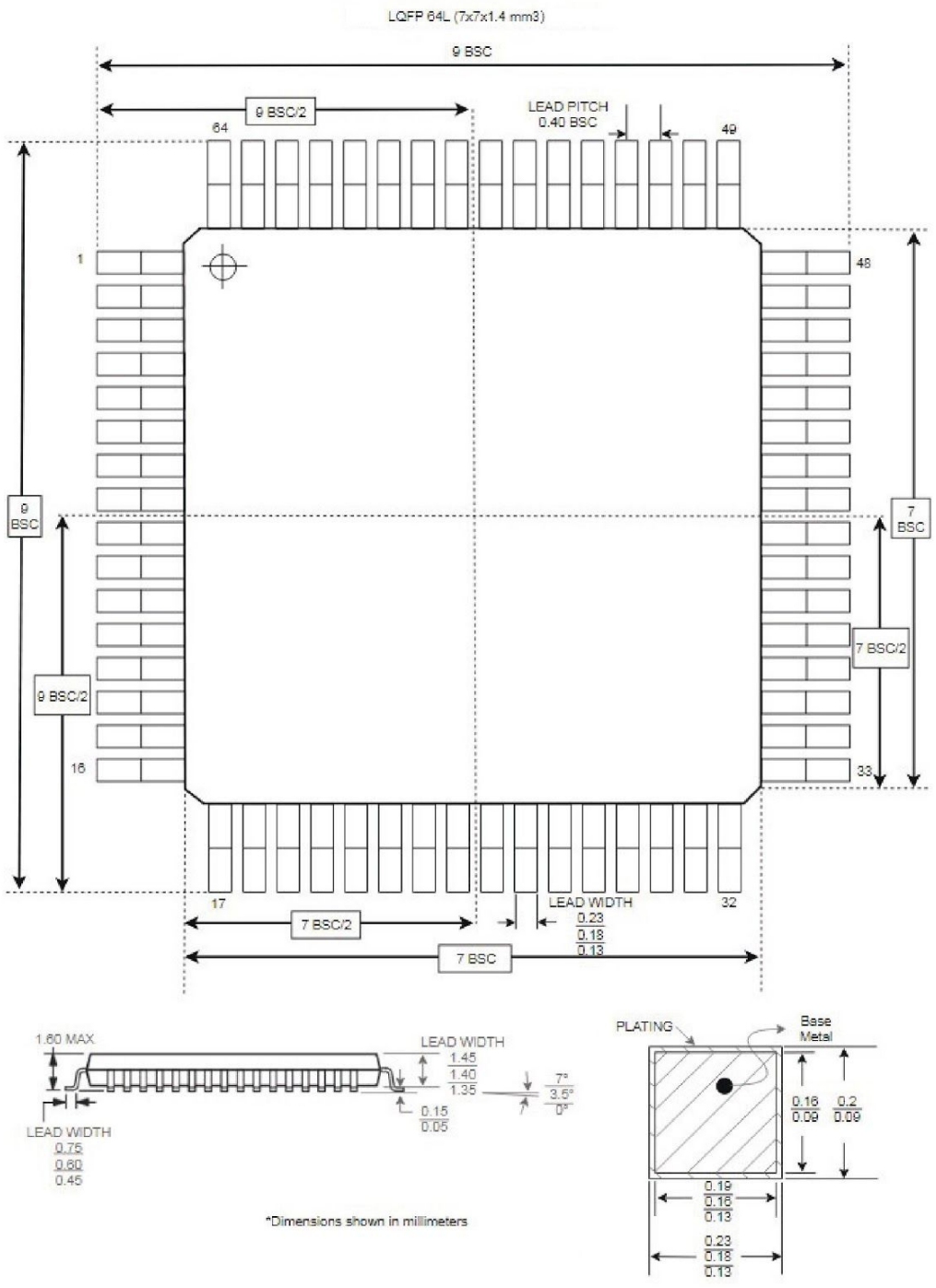
Recommendable Reflow Soldering Profile



Profile Feature	Pb Free Package
Average ramp-up rate(217℃ to peak)	3℃/sec. max
Preheat temperature 150℃~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec. max
Time 25℃ to peak temperature	8 min. max

* According to J-STD-020C

Package Dimensions



REVISION HISTORY

Date	Revision	Description
2020.03.24	0.9	Beta
2020.05.04	0.91	ADC_IN(Analog IN)
2020.05.21	0.92	APPLICATION CIRCUIT / BLOCK DIAGRAM
2020.05.25	0.93	SPI clock 96MHz / ADD GPIO16~GPIO19
2020.06.15	0.94	20 general purpose inputs/outputs
2020.07.27	0.95	Reference voltage
2020.11.25	0.96	Modify DAC description
2021.02.04	0.97	Modify ADC/DAC description
2021.02.20	0.98	USB RESERVE/LED description
2021.02.23	0.99	Modify APPLICATION CIRCUIT