SSN COLLEGE OF ENGINEERING ,SSN NAGAR603110
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
MULTICORE ARCHITECTURE(CP7103)
DATE:17-1-2018 VIII SEM B.E MAX:50 Time: 2Hrs

Unit Test -I Answer Key

PART A (10 Marks)

1)) The clock frequency is directly proportional to power. For every rise in 1% of clock frequency there will be 3% rise in the power requirement.
The clock frequency of a uniprocessor systems can not be increased beyond certain level because of the power limitation

2). A pipeline in which the stages of full-fledged instruction might be construed as MISD system. Multiple intr.s are applied to single stream of data item as it moves through the pipeline. Multiple intr.s operate on one data stream. Heterogeneous stytems operate on sam data stream. Eg. Space shuttle flight control computer, Systolic array

3) In a shared memory multi-processor environment, the processors have private caches and share a common memory. During the course of time, processors bring the data from shared memory to their private caches. It is possible that the same data item may be accessed by more than one processor. If one processor updates the data in its local cache and this updation may not be known to other processors. So there will be inconsistency among the copies of the same data present in different prcessors private caches. This inconsistency is called cache coherence.

4) Whenever a path is busy an alternate path is always exists. Therefore the processor interconnection path is never blocking for interconnections cross bar switch is a non blocking switch.

5) Speedup = 1/ ((1-F.E + F.E/S.E))
F.E=parallel mode
80= 1/(1- $F.E_{parallel}$+ $F.E_{parallel}$/100)
$F.E_{parallel} = 0.9975$
To achieve a speedup of 80 with 100 processors 0.25% of the computation be sequential.
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PART B (40 Marks)

6). Pl refer standard Text Book
(Or)
7). Pl refer standard Text Book

8).a) The most basic implementation of cache and virtual memory won't change either the number of instructions that can be executed at one time or the amount of data that can be operated on one time. However more sophisticated systems can provide some concurrency : where there is a cache miss or page fault, the CPU may attempt to execute instruction not involving unavailable data or instruction. Such systems may be described as having limited MIMD capabilities.

Pipeling: We can view pipelining as applying one complex instruction applied to multiple data items. Hence it is sometimes called SIMD

Multiple Issue and H/W Multithreading: Attempt to have multiple instructions to different data items. So they can be considered as MIMD.

b) 1) On a uniprocessor system,
120 iterations X 10,000 cycles = 12,00,000 cycles
2) on a 2 processor system, each one handles 60 iterations.
Base execution time = 60 X 10,000 cycles = 6,00,000 cycles
Synchronisation overhead = 50,000 cycles
Total Exce. Time = 6,00,000 + 50,000 = 6,50,000 cycles
Speed Up =Exec Time_old / Exec_Time_New
= 12,00,000 / 6,50,000 = 1.846
3) on a 4 processor system, each one handles 30 iterations.
Base execution time = 30 X 10,000 cycles = 3,00,000 cycles
Synchronisation overhead = 50,000 cycles
Total Exce. Time = 3,00,000 + 50,000 = 3,50,000 cycles
Speed Up =Exec Time_old / Exec_Time_New
= 12,00,000 / 3,50,000 = 3.43

(OR)

9). Pl refer standard Text Book. : SIMD variations : 1) Vector Processor, 2) GPU

10.
Multi-core is a design in which a single physical processor contains the core logic of more than one processor. It's a special kind of Multiprocessor.All processors are on the same chip. Multicore processors are MIMD. Different cores executes different threads (Multiple Instructions) ,operates on different parts of memory(Multiple Data) Multicore is a Shared Memory Multiprocessors. All cores share the same memory
Advantages:

1 Occupies less space on PCB
2 Higher throughput
3 Consume less power
4 Cache coherency can be greatly improved
5 Performs more operations/sec with less frequency

Disadvantages:

1.Maximizing the utilization of the computing resources provided by multi-core processors requires adjustments both to the operating system (OS) support and to existing application software

2. They are more difficult to manage thermally than lower-density single-chip designs

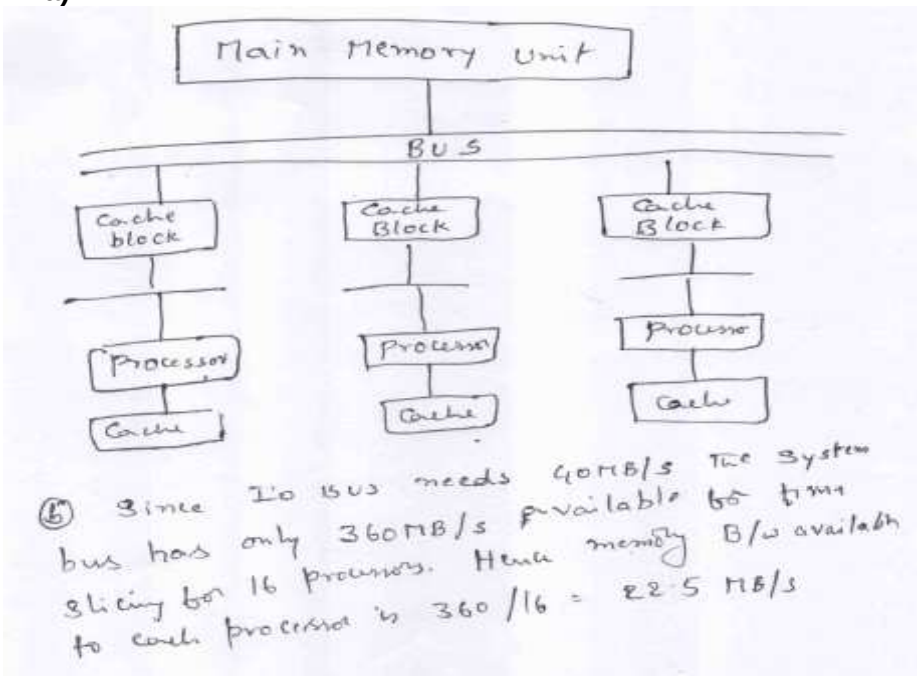
Applications:

1. Data base servers
2. Web servers
3. Compilers
4. Multimedia Applications
5. Scientific Applications

6. General applications with TLP as opposed to ILP
7. Downloading s/w while running Anti virus s/w. Editing photo while recording TV show
8. Climate modeling
9. Protein folding
10.Drug discovery
11.Energy Research
12. Data analysis

(Or)

11.a)



(b) Since I/O BUS needs 40MB/s the System bus has only 360MB/s available for time slicing for 16 processors. Hence memory B/w available to each processor is 360/16 = 22.5 MB/s