SSN COLLEGE OF ENGINEERING, KALAVAKKAM

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Compiler Design Lab – CS1356

PROGRAMMING ASSIGNMENT-11– Implementation of control and data flow analysis

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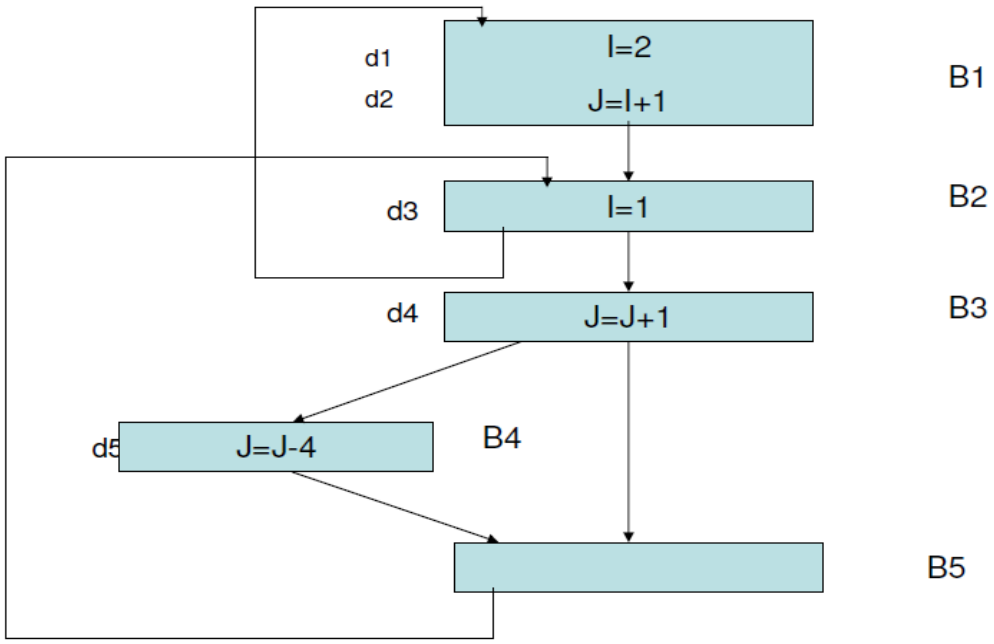
The idea of this assignment is to analyze the flow of data across alternative flows in the program to identify the reachable definitions. Further, these reachable definitions are removed. The following is the format of the code snippet that can be given as the input.



Utilize control and data flow analysis to generate and print the GEN, KILL set. Print the IN and OUT sets for the required number of iterations.

Block B	GEN[B]	Bit Vector	KILL[B]	Bit Vector
B1	{d1,d2}	11000	{d3,d4,d5}	00111
B2	{d3}	00100	{d1}	10000
B3	{d4}	00010	{d2,d5}	01001
B4	{d5}	00001	{d2,d4}	01010
B5	ø	00000	ø	00000

	INITIAL		PASS-I	
Block	IN[B]	OUT[B]	IN[B]	OUT[B]
B1	00000	11000	00100	11000
B2	00000	00100	11000	01100
B3	00000	00010	01100	00110
B4	00000	00001	00110	00101
B5	00000	00000	00111	00111

	PASS-II		PASS=III	
Block	IN[B]	OUT[B]	IN[B]	OUT[B]
B1	01100	11000	01111	11000
B2	11111	01111	11111	01111
B3	01111	00110	01111	00110
B4	00110	00101	00110	00101
B5	00111	00111	00111	00111

Try this example also