Distributed-memory interconnects

Indirect interconnects:

- Indirect interconnects provide an alternative to direct interconnects. In an indirectinterconnect, the switches may not be directly connected to a processor. They'reoften shown with unidirectional links and a collection of processors, each of whichhas an outgoing and an incoming link, and a switching network. See Figurebelow:

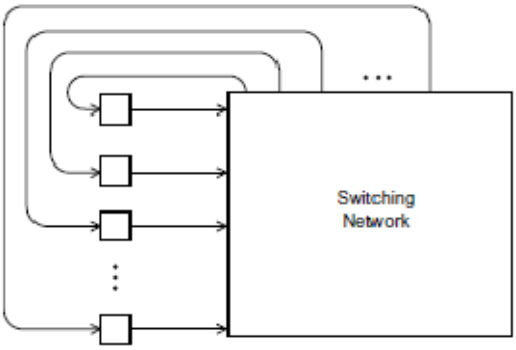


Fig: Generic indirect network

- The **crossbar** and the **omega network**are relatively simple examples of indirectnetworks. We saw a shared-memory crossbar with bidirectional links earlier
- The diagram of a distributed-memory crossbar in Figure below has unidirectional links. Notice that as long as two processors don't attempt to communicate with the same processor, all the processors can simultaneously communicate with another processor.

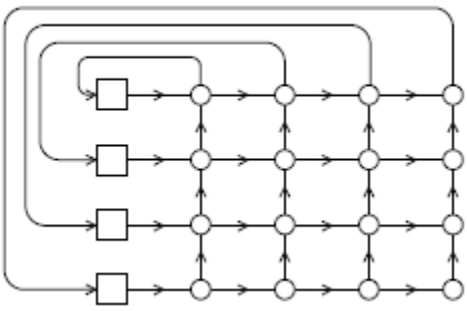
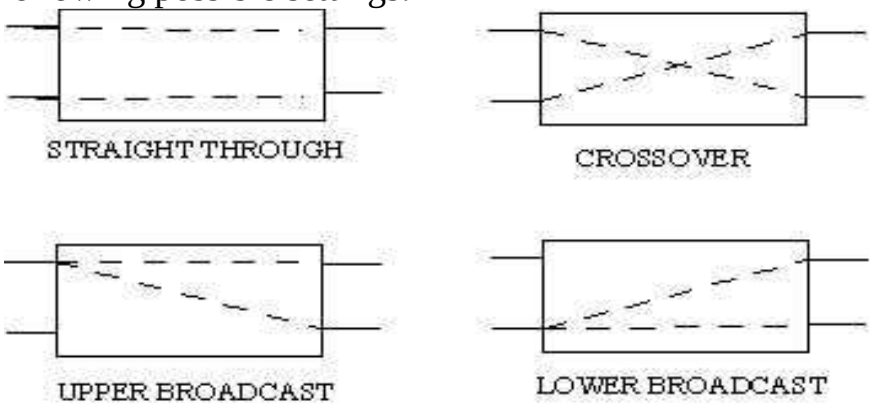


Fig: Crossbar interconnect for Distributed memory

The basic element of Omega network is 2x2 switch which has the following possible settings:



- An omega network is shown in Figure below. The switches are two-by-two crossbars (see Figure b). Observe that unlike the crossbar, there are communications

that cannot occur simultaneously.

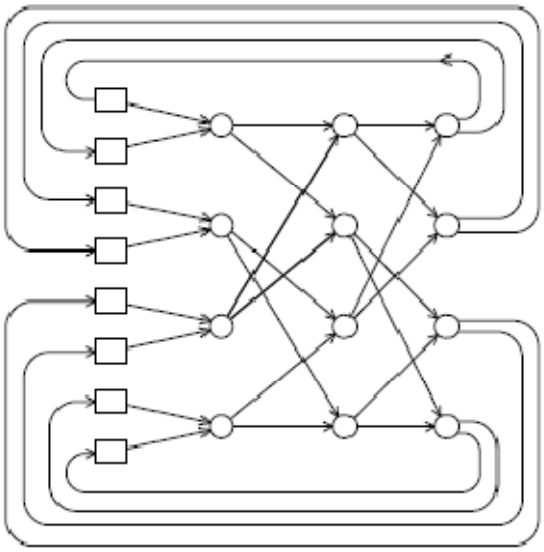


Fig: Omega network

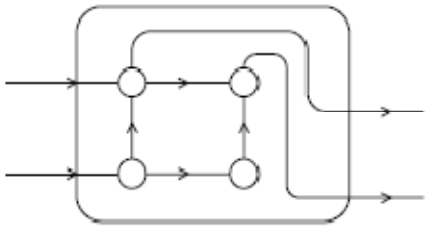


Fig: A switch in Omega netork

- For example, in Figure a above ,if processor 0 sends a message to processor 6, then processor 1 cannot simultaneously send a message to processor 7. On the other hand, the omega network is less expensive than the crossbar. The omega network uses ½ plog2 (p) of the 2x2 crossbar

switches, so it uses a total of 2plog2.(p) switches, while the crossbar uses p2.

- Indirect networks with multiple layers of switches between terminals
- complete connectivity for a set of inputs and outputs is the Omega Network.