Shared-memory interconnects

Currently the two most widely used interconnects on shared-memory systems are:

- Buses
- Crossbarswitch network .

Buses:

- Bus is a collection of parallel communication wires together with some hardware that controls access to the bus. The key characteristic of a bus is that the communication wires are shared by the devices that are connected to it.
- Buses have the virtue of low cost and flexibility; multiple devices can be connected to a bus with little additional cost. However, since the communication wires are shared, as the number of devices connected to the bus increases, the likelihood that there will be contention for use of the bus increases, and the expected performance of the bus decreases.
- If we connect a large number of processors to a bus, we would expect that the processors would frequently have to wait for access to main memory. Thus, as the size of shared-memory systems increases, buses are rapidly being replaced by switched interconnects

① Time-shared Common Bus:-

A common-bus multiprocessor system consists of a no of processors connected thru a common path to a memory unit. only one processor can communicate with the memory or another processor at any given time. Transfer operations are conducted by the processor that is in control of the bus at the time. Any other processor wishing to initiate a transfer must first det the availability status of the bus, and only after the bus becomes available can the processor address the destn unit to initiate transfer. A command is issued to the destn unit what op" is to be performed. The receiving unit recognizes its address in the bus and responds to the control signals from the sender after which the transfer is initiated. The system may exhibit transfer conflicts since one common bus is shared by all processors. These conflicts can be resolved by incorporating a bus controller that establishes the priority among the requesting units.

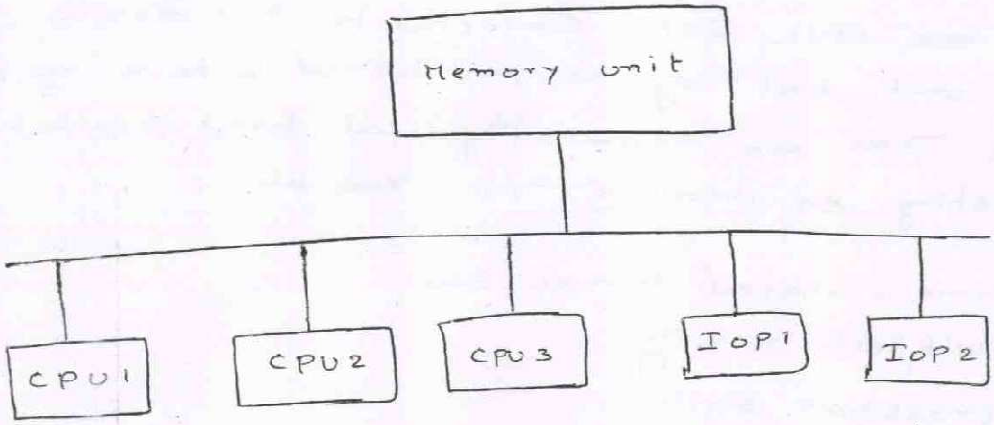

fig Time-shared Common Bus organization.

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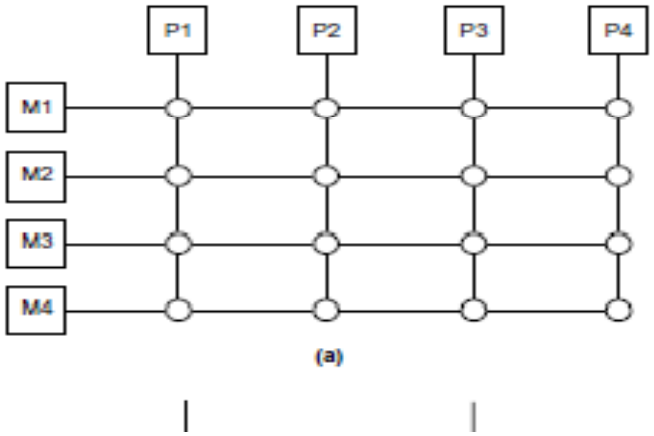
Crossbar Switch Network:

As the name suggests, switched interconnects use switches to control the routing
of data among the connected devices. A crossbar is illustrated in Figure below.The lines are bidirectional communication links, the squares are cores or memory
modules, and the circles are switches.



Crossbars allow simultaneous communication among different devices, so they are much faster than buses. However, the cost of the switches and links is relativelyhigh. A small bus-based system will be much less expensive than a crossbar-basedsystem of the same size.

- Every node connected to all others (non-blocking)
- Good for small number of nodes
- Low latency O(1)
- High throughput
- Expensive O(N square2) cost
- Difficult to arbitrate
- Ex:IBM POWER5 - Sun Niagara I/II

(3) Crossbar Switch:-

A crossbar switch organization consists of a no of cross points that are placed at intersec^{n} b/w processor buses and memory modules. The small □^{re} in each cross point is a switch that det^{s} the path from a processor to a memory module. Each switch pt has control logic to set up the transfer path b/w a processor and memory. It examines the address that is placed in the bus to det^{r} whether its particular module is being addressed. It also resolves multiple req^{s} for access to the same memory module on a predet^{d} priority basis.

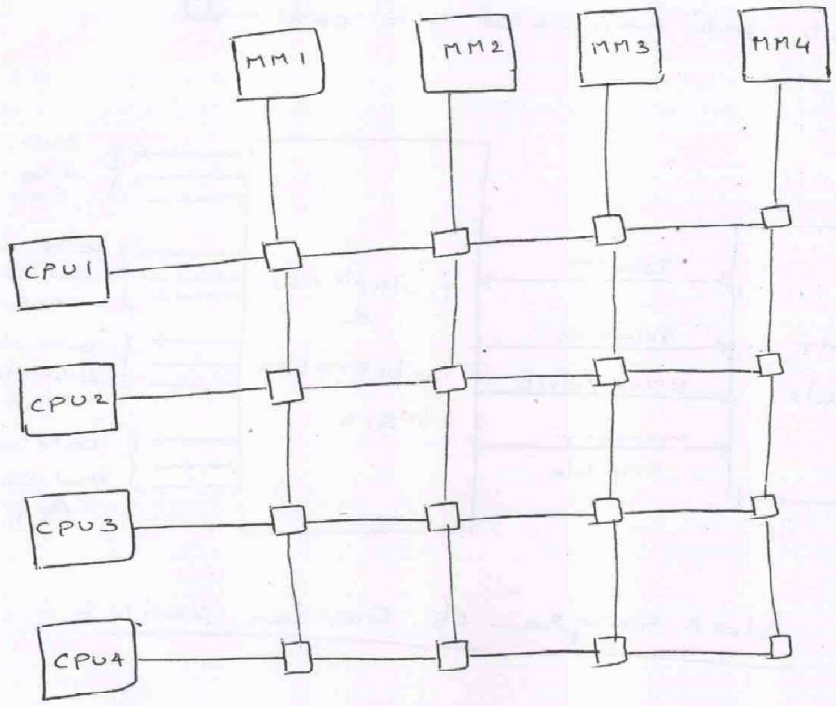


Fig Cross bar switch.

The following fig shows the block diag of a cross. Switch. Connected to one memory module. The circuit consist of multiplexers that select the data, address and cont from one CPU for Commu with memory module. priority levels are established by arbitration logic to select one CPU when two or more CPUs attempt to access the same memory. The mux are controlled with a binary code that is generated by the priority encoder. with in the arbitration logic.

A crossbar switch organization supports simultaneous transfers from all memory modules because there is a seperate path associated with each module.

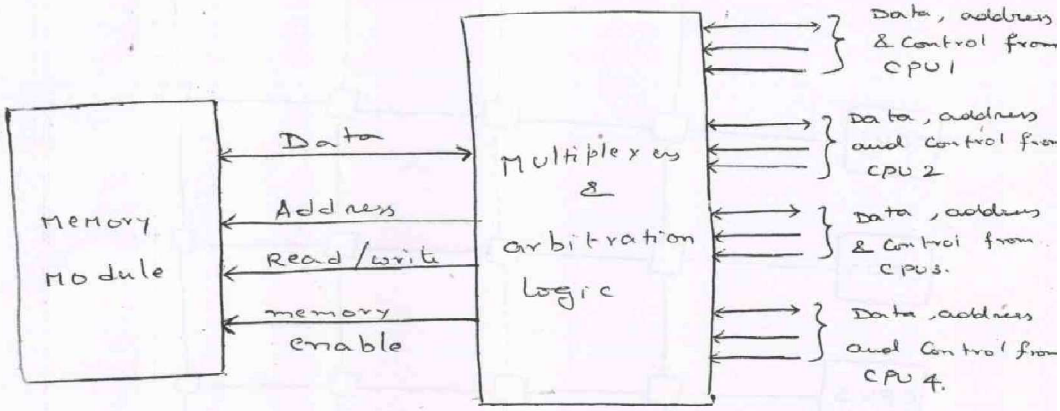


fig Block diagram of Crossbar switch.