

SSN COLLEGE OF ENGINEERING, KALAVAKKAM – 603110
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
VIII Sem B.E COMPUTER SCIENCE AND ENGINEERING
CS6801 MULTICORE ARCHITECTURES & PROGRAMMING

Internal Assessment Test - I

Class: VIII Sem B.E(A & B)
Time: 8.00AM TO 9.30AM

Date: 17-1-2018
Max Marks: 50

Part – A (5 x 2 = 10 marks)

1. What are the limitations of single core systems ?	[CO1, K1]
2. In our discussion of parallel hardware we used Flynn's taxonomy to identify 3 types of parallel systems: SISD, SIMD and MIMD. None of our systems were identified as Multiple Instruction and Single Data or MISD. How would a MISD system work. Give an example.	[CO1, K2]
3. What is Cache coherence.	[CO1, K1]
4. Why does a cross bar switch is a non blocking switch?	[CO1, K2]
5. Suppose you want to achieve a speedup of 80 with 100 processors. What fraction of original computation can be sequential.	[CO1, K3]

Part – B (40Marks)

6. Write a note on various interconnection networks.	[CO1, K1] (16)
(or)	
7. What is cache coherence. Explain briefly about the solutions for cache coherence.	[CO1, K1] (16)
8.a) Does the addition of cache and virtual memory to a Von Neumann system change its designation as SISD system? What about the addition of (a) pipelining (b) Multiple Issue (c) Hardware Multithreading ?	[CO1, K3] (8)
8 b) A program repeatedly executes a loop that has 120 iterations. Each iteration has 10,000 cycles. On a multiprocessor system 50,000 cycles are needed to synchronize the processors once all the iterations of the loop have completed. a) What is the execution time on a Uniprocessor system. b) What is the execution on a 2 processor system. What is the speedup over the uniprocessor system. c) What is the execution on a 4 processor system. What is the speedup over the uniprocessor system	[CO1, K3] (8)

(or)	
9.What are SIMD systems. Explain in detail the different types of SIMD systems [CO1, K2] (16)	
10. What are multi core architectures what are the Advantages and Disadvantages of Multicore Processors. Give their applications. [CO1, K2] (8)	
(or)	
11. Show a two level hierarchical bus assuming a Distributed memory Multiprocessor system with a processor with its local cache at it leaf (last node) and the main memory at the root and cache block at level1. b) Each processor connects a centralized memory unit. 16 processors connect the system bus at (level1) of 400MB/sec. What is the bandwidth available to each processor if all the processors connect the system bus to the memory unit and IO bus of (level2) of bandwidth 40MB/sec in a time sharing bus system. [CO1, K3] (8)	

*** ALL THE BEST ***

Prepared by	Reviewed by HOD-CSE

