RV1126 Linaro CE SDK Design

I2C MAP

Port	Pin Name	Domain	Bus Name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Slave Bus Capability	Note
I2C0	I2C0_SCL/GPIO0_B4_u I2C0_SDA/GPIO0_B5_u	PMUIO1	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC3V3_SYS	RK809-2	0x20		PMIC
I2C1	I2C1_SCL/UART4_CTSN_M2/GPIO1_D3_u I2C1_SDA/UART4_RTSN_M2/GPIO1_D2_u	VCCIO4	I2C1_SCL I2C1_SDA	VCC1V8_DOVDD				
I2C2	I2C2_SCL/PWM4_M0/GPIO0_C2_D I2C2_SDA/PMM5_M0/GPIO0_C3_D	PMUIO1_VDD	I2C2_SCL I2C2_SDA	VCC3V3_SYS				
I2C3	CIF_D0_M0/I2S0_SCLK_TX_M1/UART4_TX_M0/I2C3_SCL_M0/PWM8_M0/GPIO3_A4_D CIF_D1_M0/RGMII_CRS_M0/I2S0_LRCK_TX_M1/UART4_RX_M0/I2C3_SDA_M0/PWM9_M0/GPIO3_A5_D	VCCIO6	I2C3_SCL_M0 I2C3_SDA_M0	VCC_1V8				
I2C4	I2C4_SCL_M0/CAN_RXD_M0/UART3_TX_M2/PWM7_IR_M1/GPIO3_A0_U I2C4_SDA_M0/CAN_TXD_M0/UART3_RX_M2/PWM11_IR_M1/GPIO3_A1_U	VCCIO5	I2C4_SCL_M0 I2C4_SDA_M0	VCC_3V3				
I2C5	CIF_D4_M0/RGMII_RXD3_M0/I2S0_MCLK_M1/UART5_RTSN_M0/I2C5_SCL_M1/GPIO3_B0 CIF_D5_M0/RGMII_TXD2_M0/I2S0_SCLK_RX_M1/UART5_CTSN_M0/I2C5_SDA_M1/GPIO3_B1	VCCIO6	I2C5_SCL_M1 I2C5_SDA_M1	VCC_1V8				

Reference Design Main Functions Introduction	
Power	RK809-2 + 2DCDC
RAM	EMMC/SLC NAND FLASH/SPI FLASH
ROM	DDR3L/DDR3/LPDDR3/LPDDR4
Interface	SDMMC/SDIO/MAC/LCD/CIF/MIPI_DSI/MIPI_CSI0/ MIPI_CSI1/LVDS0/LVDS1/I2S/PDM/USB/ADC

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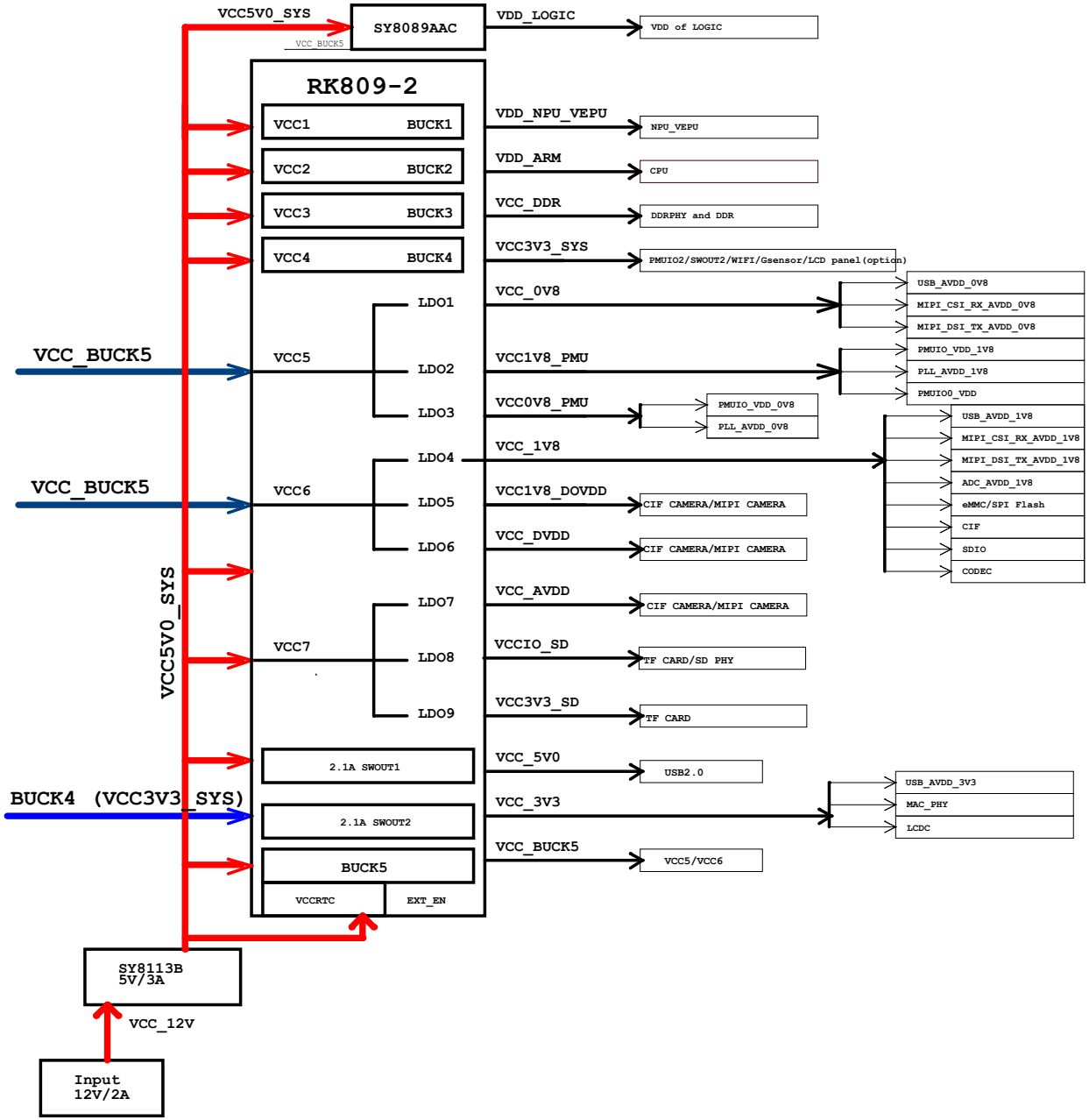
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	00.Cover Page		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	0 of 26

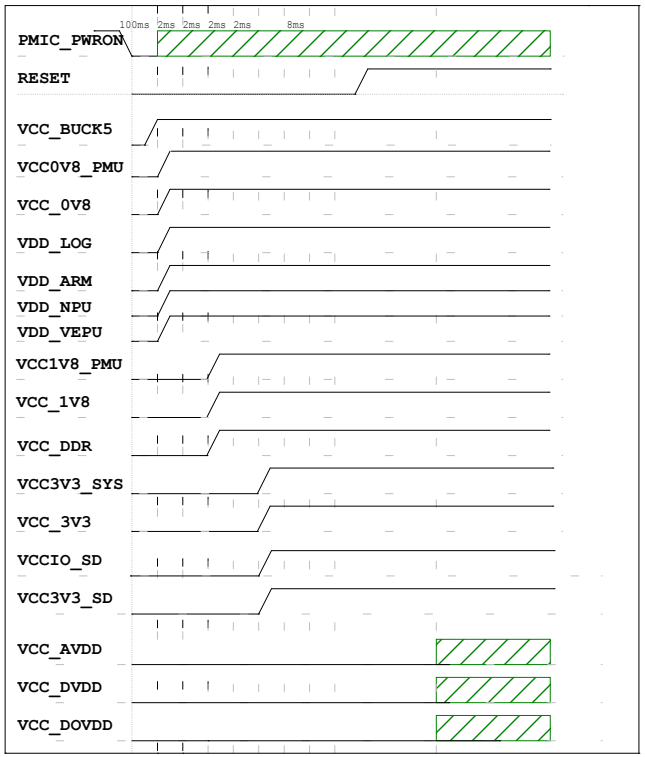
Power Diagram



RV1126_RV1109 Power-on Sequence

Power Name	PMIC Channel	Time Slot (step 2ms)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_BUCK5	RK809-2 BUCK5	Slot: 1	2.2V	2.5A	ON	ON		
VCC0V8_PMU	RK809-2 LDO3	Slot: 2	0.8V	0.1A	ON	ON		
VCC_0V8	RK809-2 LDO1	Slot: 2	0.8V	0.4A	ON	OFF		
VDD_LOGIC	Ext(SY8089AAC)	Slot: 2	0.8V	2.5A	ON	OFF		
VDD_ARM	RK809-2 BUCK2	Slot: 2	0.8V	2.5A	ON	OFF		
VCC1V8_PMU	RK809-2 LDO2	Slot: 3	1.8V	0.4A	ON	ON		
VCC_1V8	RK809-2 LDO4	Slot: 3	1.8V	0.4A	ON	OFF		
VDD_NPU	RK809-2 BUCK1	Slot: 2	0.8V	2.0A	ON	OFF		
VDD_VEPU	RK809-2 BUCK1	Slot: 2	0.8V	2.0A	ON	OFF		
VCC_DDR	RK809-2 BUCK3	Slot: 3	1.5V	1.5A	ON	ON		
VCC3V3_SYS	RK809-2 BUCK4	Slot: 4	3.3V	1.5A	ON	ON		
VCC_3V3	RK809-2 SWOUT2	Slot: 4	3.3V	1.5A	ON	OFF		
VCCIO_SD	RK809-2 LDO8	Slot: 4	3.3V	0.4A	ON	OFF		
VCC3V3_SD	RK809-2 LDO9	Slot: 4	3.3V	0.4A	ON	OFF		
VCC1V8_DOVDD	RK809-2 LDO5		1.8V	0.4A	OFF	OFF		
VCC_DVDD	RK809-2 LDO6		1.2V	0.4A	OFF	OFF		
VCC_AVDD	RK809-2 LDO7		2.8V	0.4A	OFF	OFF		
VCC5V0_HOST	RK809-2 SWOUT1		5V	2.1A	OFF	OFF		
RESET	RK809-2 sent out Reset signal for CPU(timing:10)							

NOTE:VCC_DVDD and VCC_AVDD according to camera sensor voltage



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项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	01.Power Diagram and Sequence		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	01 of 26

IO Power Domain Map

IO Domain	IO Group	Support of IO Voltage		Default Actual assigned IO Domain Voltage			Notes
		1.8V	3.3V	Net Name of Power Supply	Power Source	Voltage	
PMUIO0	GPIO0A	✓	✓	VCC1V8_PMU	RK809-2_LDO2	1.8V	
PMUIO1	GPIO0BC	✓	✓	VCC3V3_SYS	RK809-2_BUCK4	3.3V	
VCCIO1	GPIO0CD/GPIO1A	✓	✓	VCCIO_FLASH	RK809-2_LDO4	1.8V	GPIO0_B3/FLASH_VOL_SEL pin defined as a set pin for VCCIO1 voltage domain after power-on reset.It is pull-up for 1.8V
VCCIO2	GPIO1AB	✓	✓	VCCIO_SD	RK809-2_LDO8	3.3V	
VCCIO3	GPIO1BCD	✓	✓	VCCIO3_VDD	RK809-2_LDO4	1.8V	
VCCIO4	GPIO1D/GPIO2A	✓	✓	VCCIO4_VDD	RK809-2_LDO4	1.8V	
VCCIO5	GPIO2ABCD/GPIO3A	✓	✓	VCCIO5_VDD	RK809-2_SWOUT2	3.3V	
VCCIO6	GPIO3ABC	✓	✓	VCCIO6_VDD	RK809-2_LDO4	1.8V	
VCCIO7	GPIO3D/GPIO4A	✓	✓	VCCIO7_VDD	RK809-2_LDO4	1.8V	

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项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	02.IO Power Domain Map		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	02of 26

Power

U1000N
SOC_RV1126/RV1109
BGA409_14R00X14R00X0R90

NPU/LOGIC/VEPU/ARM Power

NPU_VDD_1	H11	VDD_NPU
NPU_VDD_2	H12	
NPU_VDD_3	J10	
NPU_VDD_4	J11	
NPU_VDD_5	K10	
NPU_VDD_6	K11	
LOGIC_VDD_1	H9	VDD_LOGIC
LOGIC_VDD_2	J9	
LOGIC_VDD_3	L10	
LOGIC_VDD_4	M11	
LOGIC_VDD_5	H13	
LOGIC_VDD_6	J13	
VEPU_VDD_1	L9	VDD_VEPU
VEPU_VDD_2	M9	
VEPU_VDD_3	N8	
VEPU_VDD_4	N9	
ARM_VDD_1	N12	VDD_ARM
ARM_VDD_2	P12	
ARM_VDD_3	P13	

Supply for VCCIO1~7 Power

VCCIO_VDD_1V8 — H14 — VCC_1V8

C1000 100nF X5R 6.3V C0402

VDD_NPU

C1006	C1005	C1004	C1003	C1002	C1001
10uF	1uF	1uF	100nF	100nF	100nF
X5R	X5R	X5R	X5R	X5R	X5R
4V	6.3V	6.3V	6.3V	6.3V	6.3V
C0402	C0402	C0402	C0201	C0201	C0201

For NPU Power

VDD_VEPU

C1019	C1018	C1017	C1016
10uF	1uF	100nF	100nF
X5R	X5R	X5R	X5R
4V	6.3V	6.3V	6.3V
C0402	C0402	C0201	C0201

For VEPU Power

VDD_ARM

C1015	C1014	C1013	C1012
10uF	1uF	100nF	100nF
X5R	X5R	X5R	X5R
4V	6.3V	6.3V	6.3V
C0402	C0402	C0201	C0201

VDD_LOGIC

C1011	C1009	C1010	C1007	C1008
10uF	1uF	1uF	100nF	100nF
X5R	X5R	X5R	X5R	X5R
4V	6.3V	6.3V	6.3V	6.3V
C0402	C0402	C0402	C0201	C0201

GND

U1000O
SOC_RV1126/RV1109
BGA409_14R00X14R00X0R90

VSS/AVSS

A1	VSS_1	VSS_53	K9
A21	AVSS_2	VSS_54	K12
B12	VSS_3	VSS_55	K13
C3	VSS_4	VSS_56	K14
C5	VSS_5	VSS_57	L2
C7	VSS_6	VSS_58	L5
C10	VSS_7	VSS_59	L6
C12	VSS_8	VSS_60	L11
D9	VSS_9	VSS_61	L12
D12	VSS_10	VSS_62	L13
D18	AVSS_11	VSS_63	L14
E4	VSS_12	VSS_64	L16
E6	VSS_13	VSS_65	M3
E8	VSS_14	VSS_66	M5
E9	VSS_15	VSS_67	M7
E10	VSS_16	VSS_68	M8
E11	VSS_17	VSS_69	M10
E12	VSS_18	VSS_70	M12
F3	VSS_19	VSS_71	M13
F5	VSS_20	VSS_72	M14
F7	VSS_21	VSS_73	M16
F8	VSS_22	VSS_74	N5
F9	VSS_23	VSS_75	N6
F10	VSS_24	VSS_76	N7
F11	VSS_25	VSS_77	N10
F12	VSS_26	VSS_78	N11
F13	VSS_27	VSS_79	N13
F14	AVSS_28	VSS_80	N14
F15	AVSS_29	VSS_81	N16
G2	VSS_30	VSS_82	P5
G5	VSS_31	VSS_83	P7
G6	VSS_32	VSS_84	P8
G10	VSS_33	VSS_85	P9
G11	VSS_34	VSS_86	P14
G12	VSS_35	VSS_87	P16
G13	VSS_36	VSS_88	R1
G16	AVSS_37	VSS_89	R5
G17	AVSS_38	VSS_90	R12
H4	VSS_39	VSS_91	R13
H5	VSS_40	VSS_92	R14
H6	VSS_41	VSS_93	T6
H7	VSS_42	VSS_94	T9
H10	VSS_43	VSS_95	T10
H15	VSS_44	VSS_96	T14
J5	VSS_45	VSS_97	T17
J6	VSS_46	VSS_98	V17
J12	VSS_47	VSS_99	W9
J14	VSS_48	VSS_100	W14
J16	VSS_49	VSS_101	AA1
K5	VSS_50	VSS_102	AA10
K6	VSS_51	VSS_103	AA21
K8	VSS_52		

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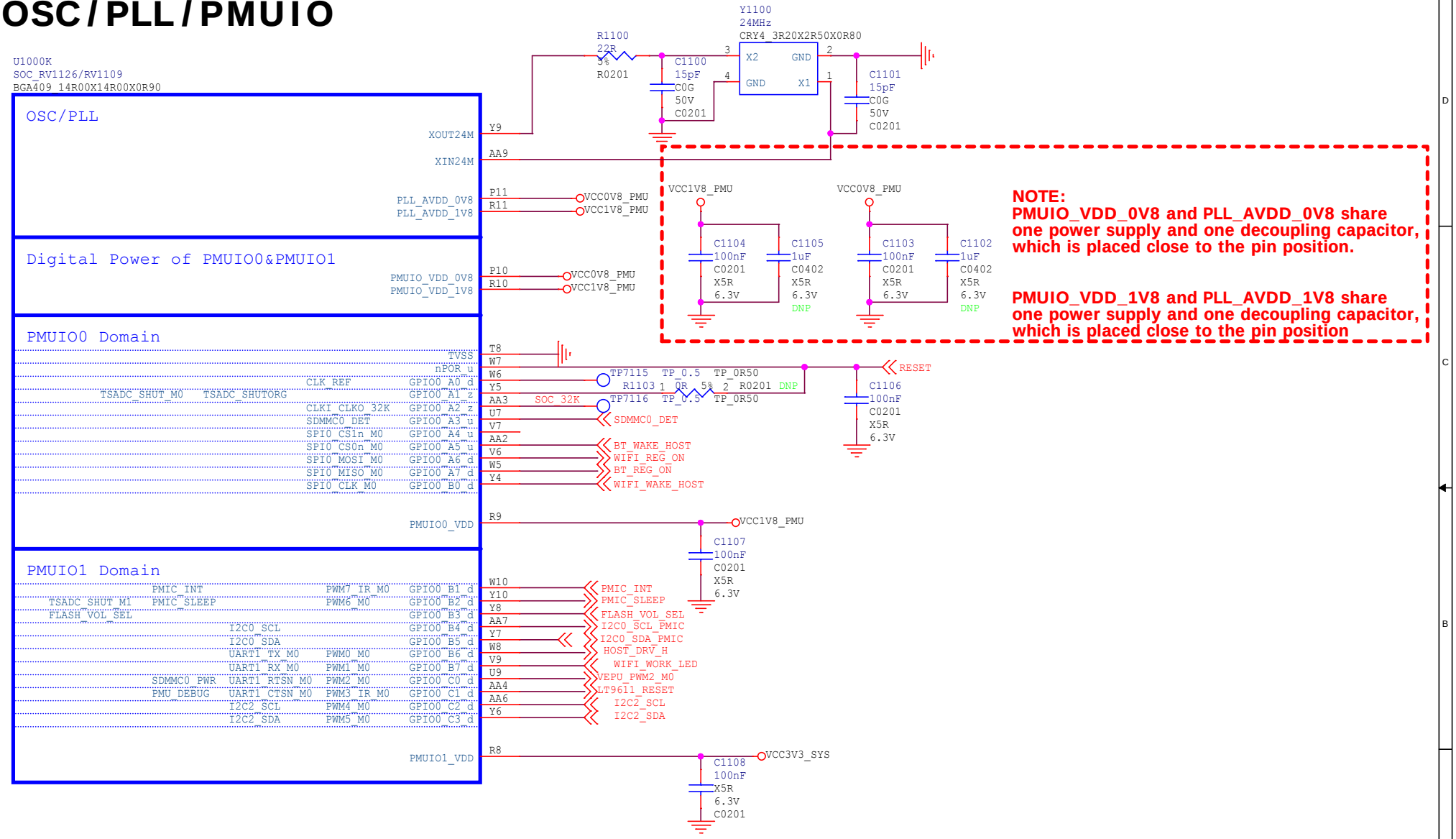
文件：	RV1126_CE_SCH		
图纸：	03.RV1126/1109_Power/GND		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	03of 26

OSC/PLL/PMUIO



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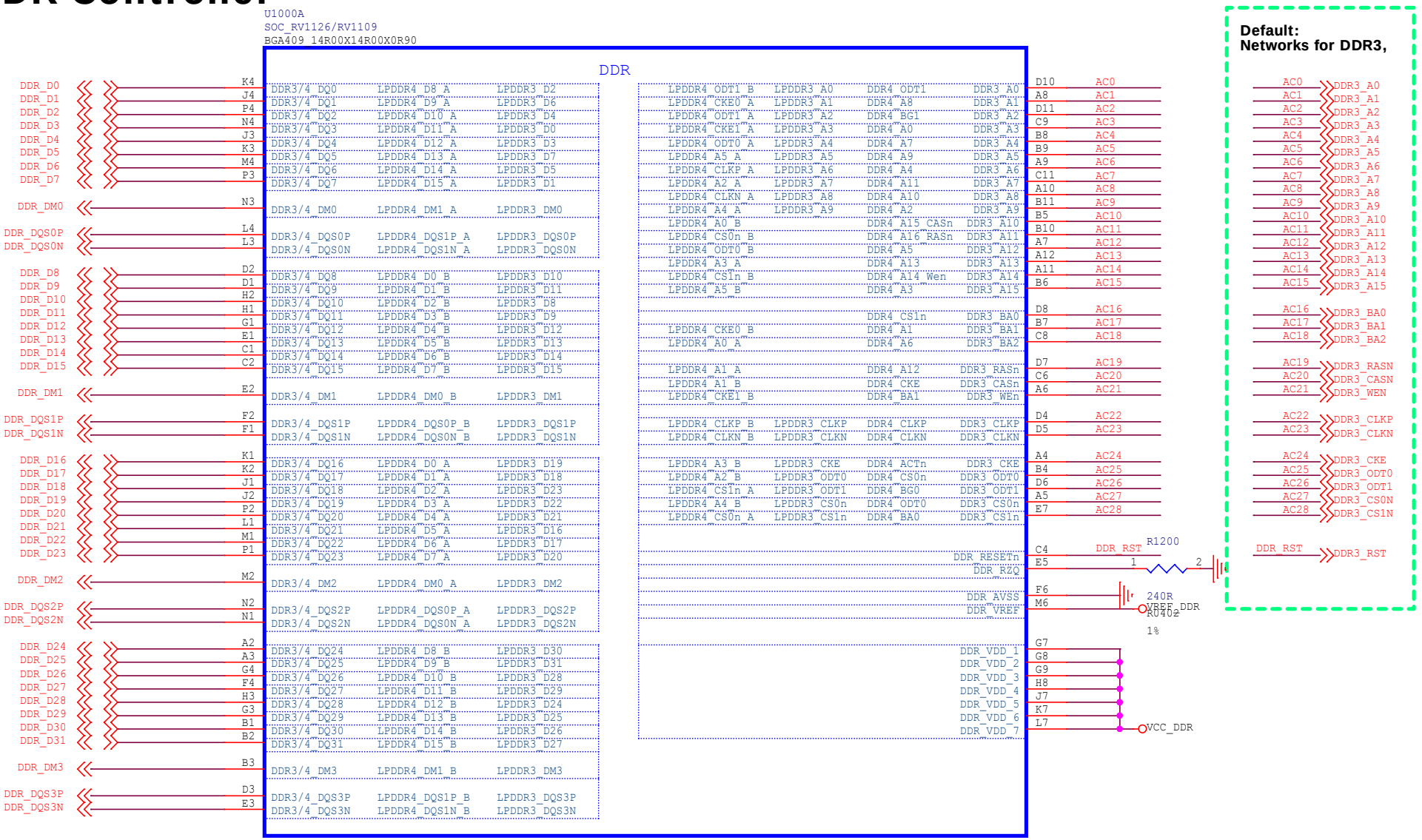
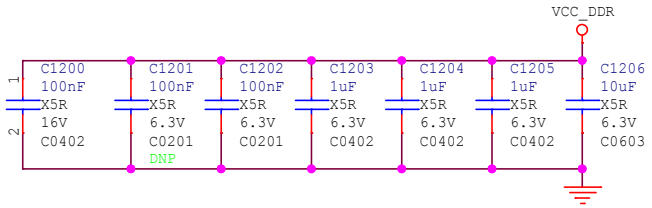
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	04.RV1126/1109_OSC/PLL/PMUIO		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	04 of 26

DDR Controller

U1000A
SOC_RV1126/RV1109
BGA409_14R00X14R00X0R90





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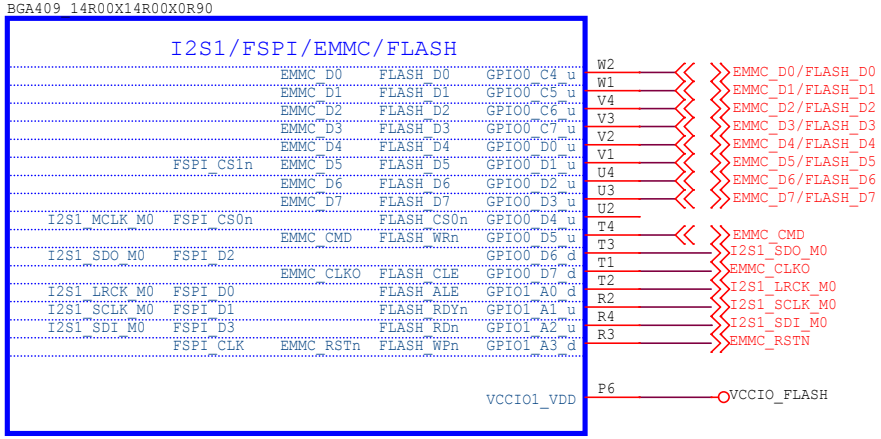
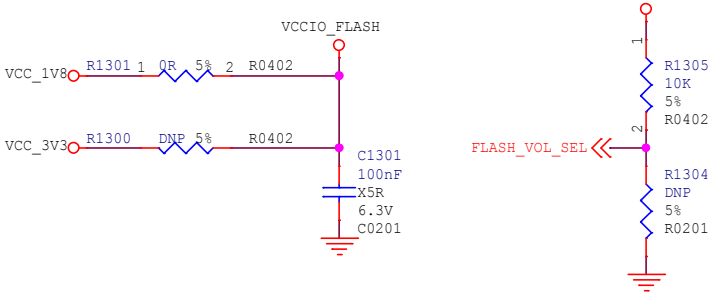
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	05.RV1126/1109_DRAM Controller		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	05of 26

EMMC/FLASH

U1000L
SOC_RV1126/RV1109
BGA409_14R00X14R00X0R90





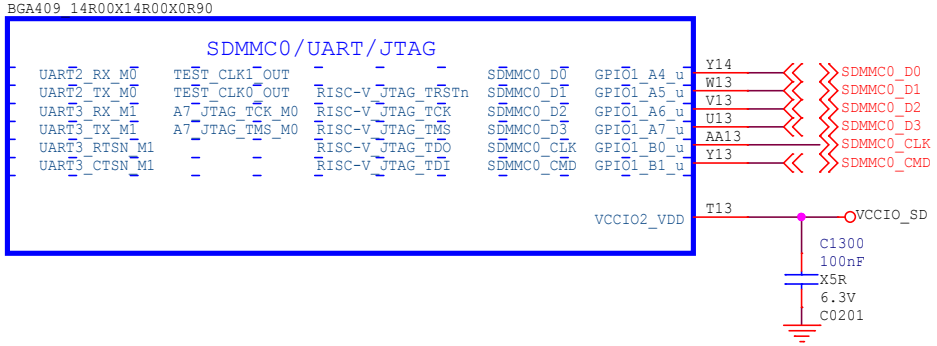
NOTE:
FLASH(VCCIO1) power domain IO supply configuration pin:

Condition	VCCIO1 (VCCIO_FLASH)
FLASH_VOL_SEL=0	3.3V
FLASH_VOL_SEL=1	1.8V Default

NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

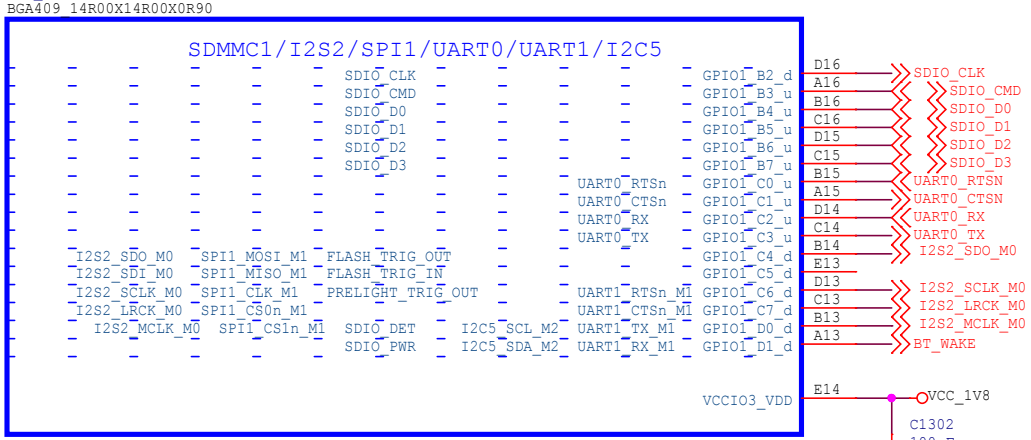
SDMMC0/JTAG

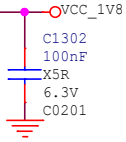
U1000I
SOC_RV1126/RV1109
BGA409_14R00X14R00X0R90



SDMMC1/UART/I2S2

U1000B
SOC_RV1126/RV1109
BGA409_14R00X14R00X0R90





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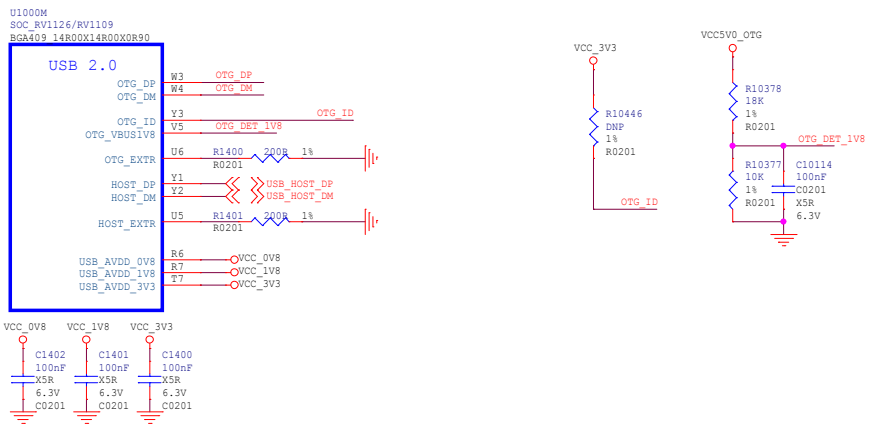
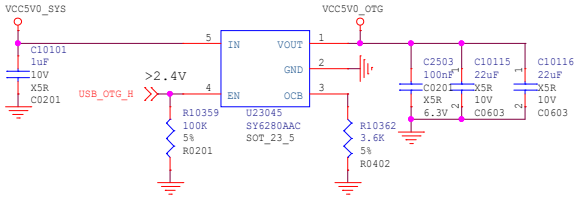
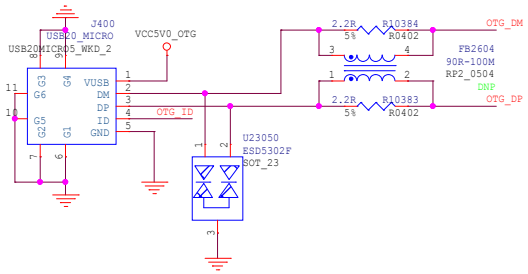
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	06.RV1126/1109_Flash/SD		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	06 of 26

USB Controller

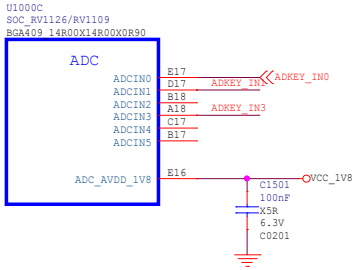


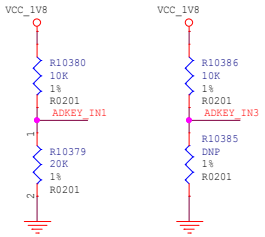


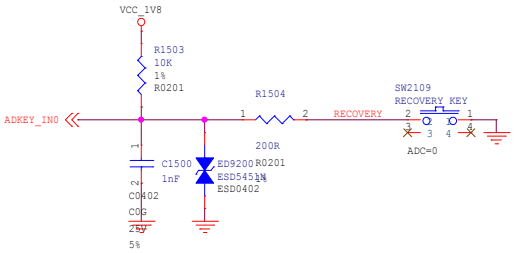


USB2.0 design rules:
1. Max intra-pair skew <4ps
2. Max trace length<6inchs
3. Max allowed via <6
4. Trace impedance 90ohm+/-10%
5. The distance between other signals follows the 3W rule.

SARADC







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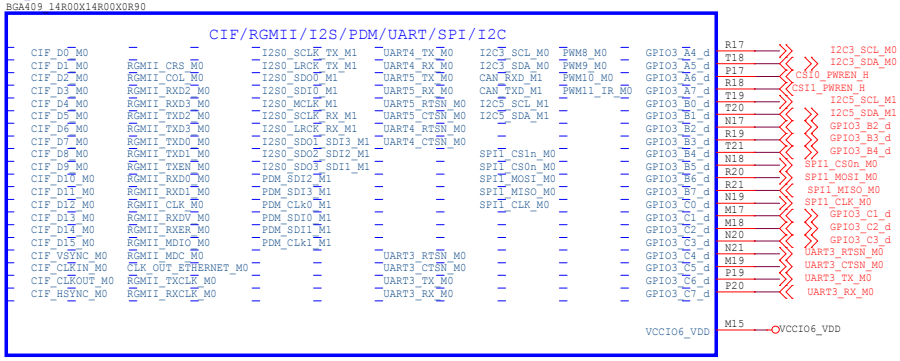
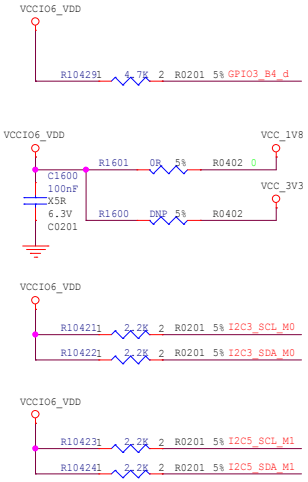
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	07.RV1126/1109_USB Controller		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	07 of 26

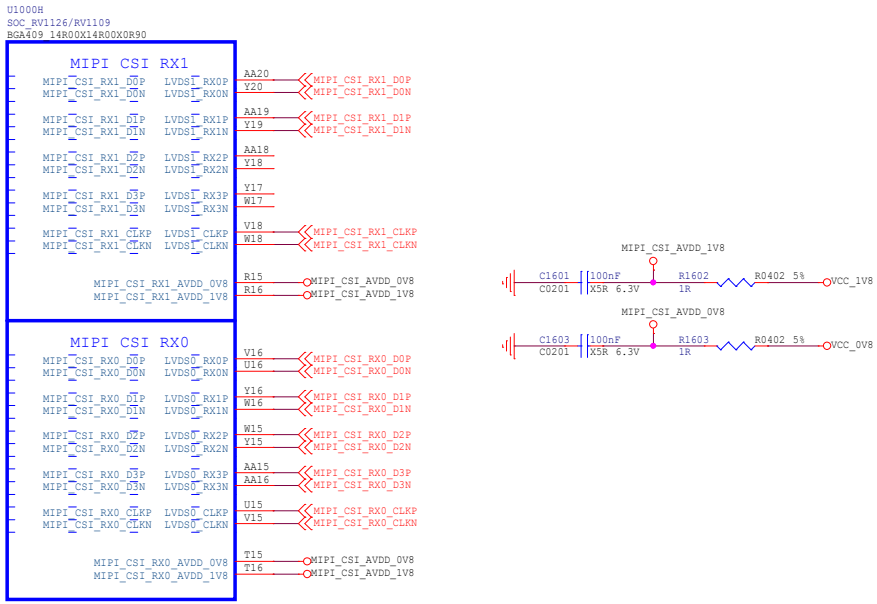
CIF Interface



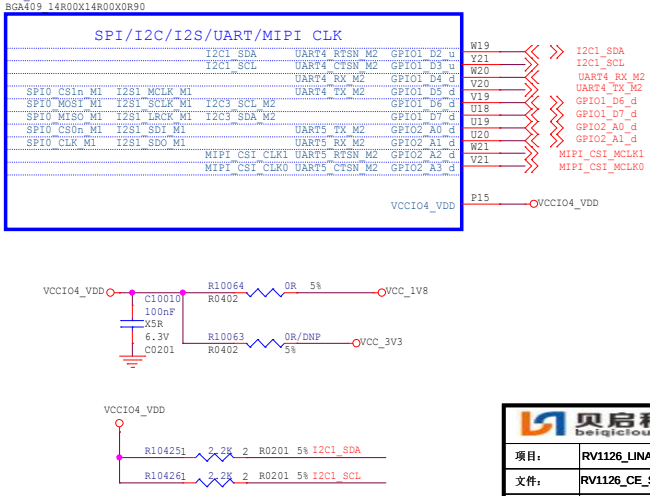


MIPI-CSI Interface

capacitors close to pin



I2C/SPI/MIPI-CLK



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项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	08.RV1126/1109_VideoInput		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	08 of 26

LCDC/RGMII/PWM

U1000E
SOC_RV1126/RV1109
BGA409_14R00X14R00X0R90

LCDC/RGMII/CIF/UART/JTAG/I2S/SPI/I2C

		UART4_RTSN_M1		RGMII_TXD3_M1	CIF_D0_M1	LCDC_D0	GPIO2_A4_d	J18 RGMII_TXD3
I2C5_SCL_M0		UART4_CTSN_M1		RGMII_CRS_M1	CIF_D1_M1	LCDC_D1	GPIO2_A5_d	L17 EPHY_RSTn
		UART4_TX_M1	PWM5_M1	RGMII_COL_M1	CIF_D2_M1	LCDC_D2	GPIO2_A6_d	M21 RGMII_INT
	I2S2_SDO_M1	UART4_RX_M1	PWM4_M1	SPI0_CSn_M2		LCDC_D3	GPIO2_A7_d	M20 FAN_CTRL
	I2S2_SDI_M1	UART5_TX_M1	PWM3_IR_M1	SPI0_MOSI_M2		LCDC_D4	GPIO2_B0_d	L19 GPIO2_B1
	I2S2_SCLK_M1	UART5_RX_M1	PWM2_M1	SPI0_MISO_M2		LCDC_D5	GPIO2_B1_d	L20 4G_DISABLE
	I2S2_LRCK_M1	UART5_RTSN_M1	PWM1_M1	SPI0_CLK_M2		LCDC_D6	GPIO2_B2_d	K16 LED3
I2C5_SDA_M0	I2S2_MCLK_M1	UART5_CTSN_M1	PWM0_M1	SPI0_CS1n_M2	CIF_D3_M1	LCDC_D7	GPIO2_B3_d	K17 LED0
				RGMII_RXDV_M1	CIF_D4_M1	LCDC_D8	GPIO2_B4_d	K18 RGMII_RXDV
				RGMII_RXD0_M1	CIF_D5_M1	LCDC_D9	GPIO2_B5_d	K19 RGMII_RXD0
				RGMII_RXD1_M1	CIF_D6_M1	LCDC_D10	GPIO2_B6_d	K20 RGMII_RXD1
				RGMII_CLK_M1	CIF_D7_M1	LCDC_D11	GPIO2_B7_d	K21 LED2
				RGMII_RXER_M1	CIF_D8_M1	LCDC_D12	GPIO2_C0_d	J19
				RGMII_MDIO_M1	CIF_D9_M1	LCDC_D13	GPIO2_C1_d	J21 RGMII_MDIO
				RGMII_MDC_M1	CIF_D10_M1	LCDC_D14	GPIO2_C2_d	J20 RGMII_MDC
				RGMII_TXD0_M1	CIF_D11_M1	LCDC_D15	GPIO2_C3_d	H20 RGMII_TXD0
				RGMII_TXD1_M1	CIF_D12_M1	LCDC_D16	GPIO2_C4_d	H19 RGMII_TXD1
				CIK_OUT_ETHERNET_M1	CIF_D13_M1	LCDC_D17	GPIO2_C5_d	G21 RGMII_CLKOUT
				RGMII_TXEN_M1	CIF_D14_M1	LCDC_D18	GPIO2_C6_d	G20 RGMII_TXEN
	I2S1_MCLK_M2			RGMII_RXD2_M1	CIF_D15_M1	LCDC_D19	GPIO2_C7_d	G19 RGMII_RXD2
	I2S1_SDO_M2			RGMII_RXD3_M1	CIF_VSYNC_M1	LCDC_D20	GPIO2_D0_d	H18 RGMII_RXD3
	I2S1_SCLK_M2			RGMII_TXD2_M1	CIF_CLKOUT_M1	LCDC_D21	GPIO2_D1_d	F21 RGMII_TXD2
	I2S1_LRCK_M2			RGMII_TXCLK_M1	CIF_CLKIN_M1	LCDC_D22	GPIO2_D2_d	E20 RGMII_TXCLK
	I2S1_SDI_M2			RGMII_RXCLK_M1	CIF_HSYNC_M1	LCDC_D23	GPIO2_D3_d	F19 RGMII_RXCLK
I2C3_SCL_M1			PWM6_M1	SPI1_CSn_M2		LCDC_DEN	GPIO2_D4_d	J17 BT_WORK_LED
I2C3_SDA_M1			PWM10_M1	SPI1_CLK_M2		LCDC_HSYNC	GPIO2_D5_d	H17 USB_OTG_H
		UART3_RTSN_M2	PWM9_M1	SPI1_MOSI_M2		LCDC_VSYNC	GPIO2_D6_d	C21 LT9611_INT
		UART3_CTSN_M2	PWM8_M1	SPI1_MISO_M2		LCDC_CLK	GPIO2_D7_d	D21 LT9611_PWR
I2C4_SCL_M0	CAN_RXD_M0	UART3_TX_M2	PWM7_IR_M1	SPI1_CS1n_M2			GPIO3_A0_u	E20 I2C4_SCL_M0
I2C4_SDA_M0	CAN_TXD_M0	UART3_RX_M2	PWM11_IR_M1				GPIO3_A1_u	E19 I2C4_SDA_M0
A7_JTAG_TCK_M1		UART2_TX_M1					GPIO3_A2_u	G18 UART2_TX
A7_JTAG_TMS_M1		UART2_RX_M1					GPIO3_A3_u	H16 UART2_RX

J15 K15 VCCIO5_VDD1 VCCIO5_VDD2 — VCC_3V3
C1700 100nF X5R 6.3V C0201

VCC_3V3
R10704 10K 5% R0201
R10448 2.2K 5% R0201
R10447 2.2K 5% R0201
I2C4_SCL_M0
I2C4_SDA_M0
RGMII_INT — RGMII_INT

MIPI-DSI Interface

U1000D
SOC_RV1126/RV1109
BGA409_14R00X14R00X0R90

MIPI_DSI_TX0

MIPI_DSI_TX0_D0P	A19	MIPI_TX0_D0P
MIPI_DSI_TX0_D0N	B19	MIPI_TX0_D0N
MIPI_DSI_TX0_D1P	A20	MIPI_TX0_D1P
MIPI_DSI_TX0_D1N	B20	MIPI_TX0_D1N
MIPI_DSI_TX0_D2P	B21	MIPI_TX0_D2P
MIPI_DSI_TX0_D2N	C20	MIPI_TX0_D2N
MIPI_DSI_TX0_D3P	D20	MIPI_TX0_D3P
MIPI_DSI_TX0_D3N	D19	MIPI_TX0_D3N
MIPI_DSI_TX0_CLKP	C19	MIPI_TX0_CLKP
MIPI_DSI_TX0_CLKN	C18	MIPI_TX0_CLKN
MIPI_DSI_TX0_AVDD_0V8	E18	MIPI_DSI_AVDD_0V8
MIPI_DSI_TX0_AVDD_1V8	G15	MIPI_DSI_AVDD_1V8

MIPI_DSI_AVDD_1V8 — R10061 1R 5% R0402 — VCC_1V8
C10008 100nF X5R 6.3V C0201

MIPI_DSI_AVDD_0V8 — R10062 1R 5% R0402 — VCC_0V8
C10009 100nF X5R 6.3V C0201

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项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	09.RV1126/1109_VideoOutput		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	09 of 26

Audio Interface

U1000J
SOC_RV1126/RV1109
BGA409_14R00X14R00X0R90

DEFAULT:
I2S0 connect to RK809-2
IO level is 1.8V

I2S/PDM/ACODEC/I2C

I2S0_SCLK_TX_M0		ACODEC_DAC_CLK			GPIO3_D0_d	W12
I2S0_SCLK_RX_M0	PDM_CLk1_M0	ACODEC_ADC_CLK			GPIO3_D1_d	V12
I2S0_MCLK_M0					GPIO3_D2_d	U12
I2S0_LRCK_TX_M0		ACODEC_DAC_SYNC	AUDPWM_L_M1	AUDDSM_LN	GPIO3_D3_d	W11
I2S0_LRCK_RX_M0	PDM_CLk0_M0	ACODEC_ADC_SYNC			GPIO3_D4_d	Y12
I2S0_SDO0_M0		ACODEC_DAC_DATAR	AUDPWM_R_M1	AUDDSM_LP	GPIO3_D5_d	Y11
I2S0_SDI0_M0	PDM_SDI0_M0	ACODEC_DAC_DATAL			GPIO3_D6_d	AA12
I2S0_SDO1_SDI3_M0	PDM_SDI3_M0	ACODEC_ADC_DATA			GPIO3_D7_d	T11
I2S0_SDO2_SDI2_M0	PDM_SDI2_M0	I2C4_SCL_M1	AUDPWM_L_M0	AUDDSM_RN	GPIO4_A0_d	U11
I2S0_SDO3_SDI1_M0	PDM_SDI1_M0	I2C4_SDA_M1	AUDPWM_R_M0	AUDDSM_RP	GPIO4_A1_d	V11

W12 I2S0_SCLK_TX_M0
V12 PDM_CLK1
U12 I2S0_MCLK_M0
W11 I2S0_LRCK_TX_M0
Y12 HP_DET_H
Y11 I2S0_SDO0_M0
AA12 LED1
T11 I2S0_SDI3_M0
U11 4G_RESET
V11

VCCIO7_VDD T12 VCC_1V8

C1800
100nF
X5R
6.3V
C0201

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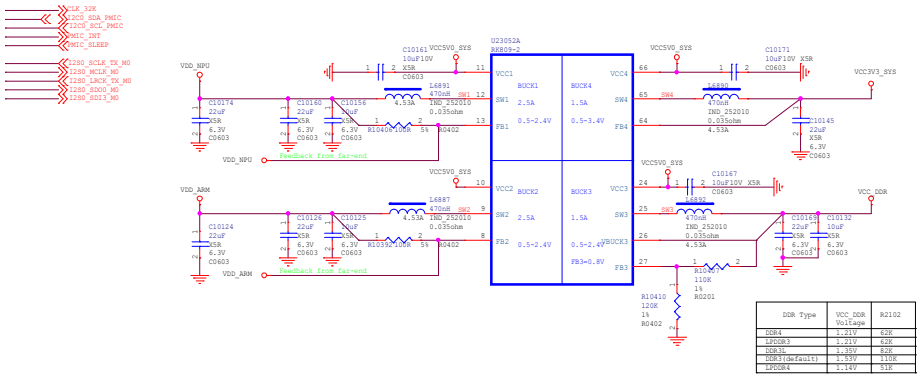
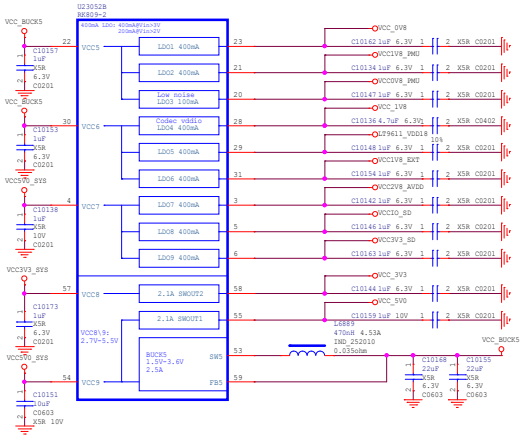
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	10.RV1126/1109_Audio		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	10of 26

PMIC RK809-2 DCDC

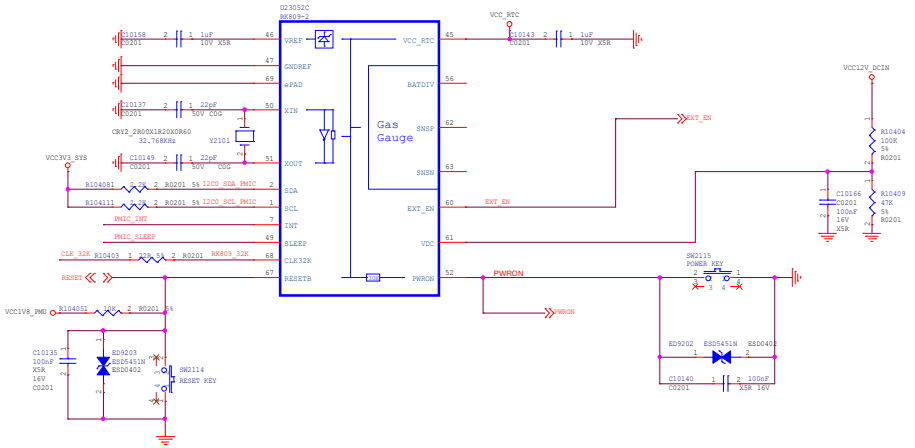


DDR Type	VCC_DDR Voltage	R2102
DDR4	1.21V	62K
LPDDR3	1.21V	62K
DDR3L	1.35V	82K
DDR3(default)	1.53V	110K
LPDDR4	1.14V	51K

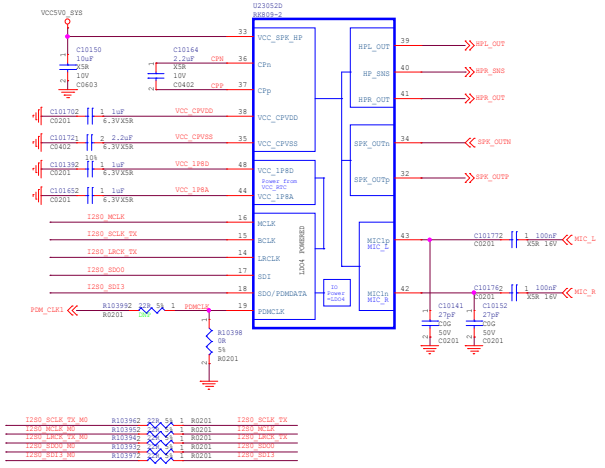
PMIC RK809-2 LDO



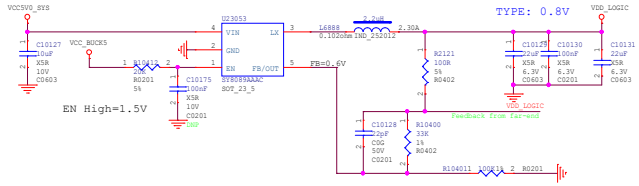
PMIC RK809-2 Managerment



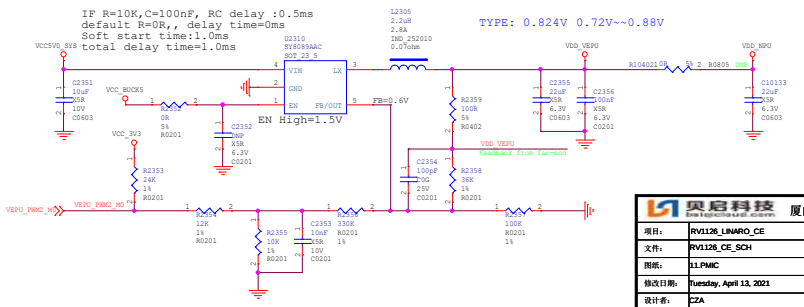
PMIC RK809-2 CODEC



VDD_LOGIC



Power Sequence: 2 VDD_VEPU



项目:	RV1126_LINARO_CE		
文件:	RV1126_CE_SCH		
图纸:	11.PMIC		
修改日期:	Tuesday, April 13, 2021	版本:	V0.1
设计者:	CZA	页码:	11 of 26

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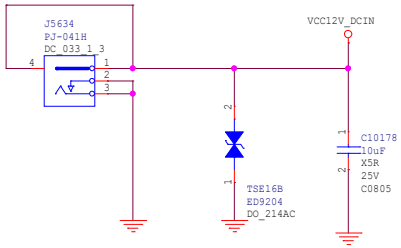
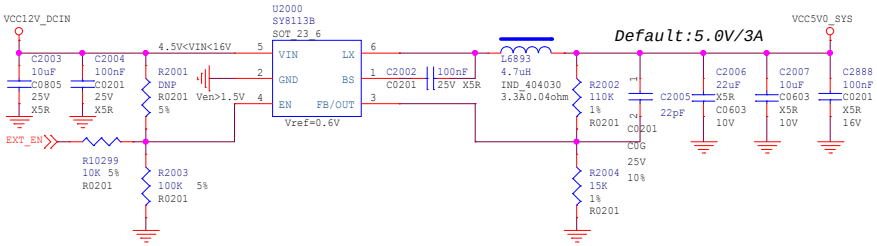
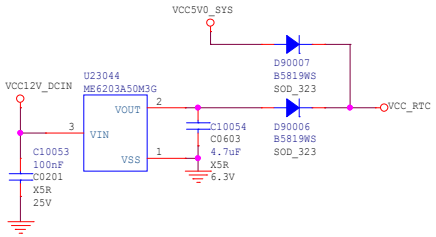
12V/2A DCIN

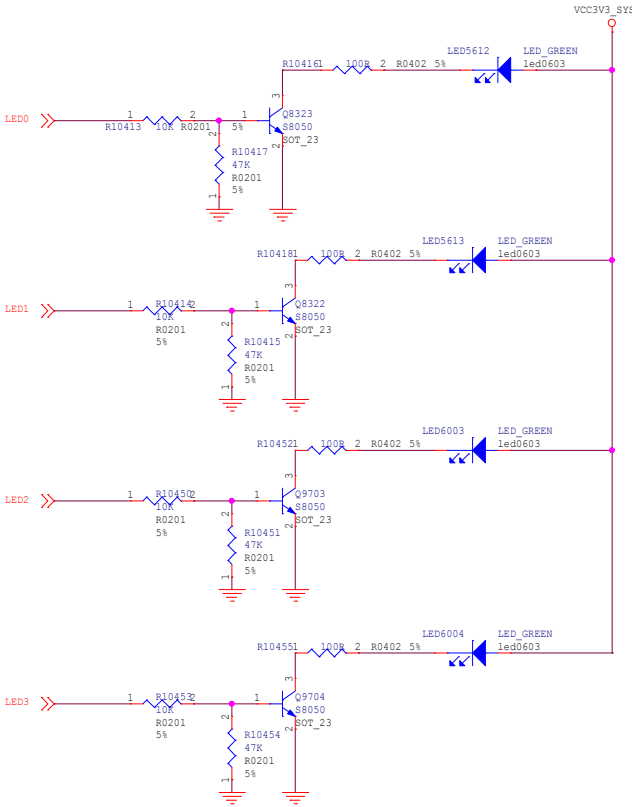


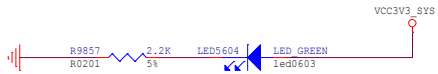
VCC5V0_SYS



VCC5V0_RTC







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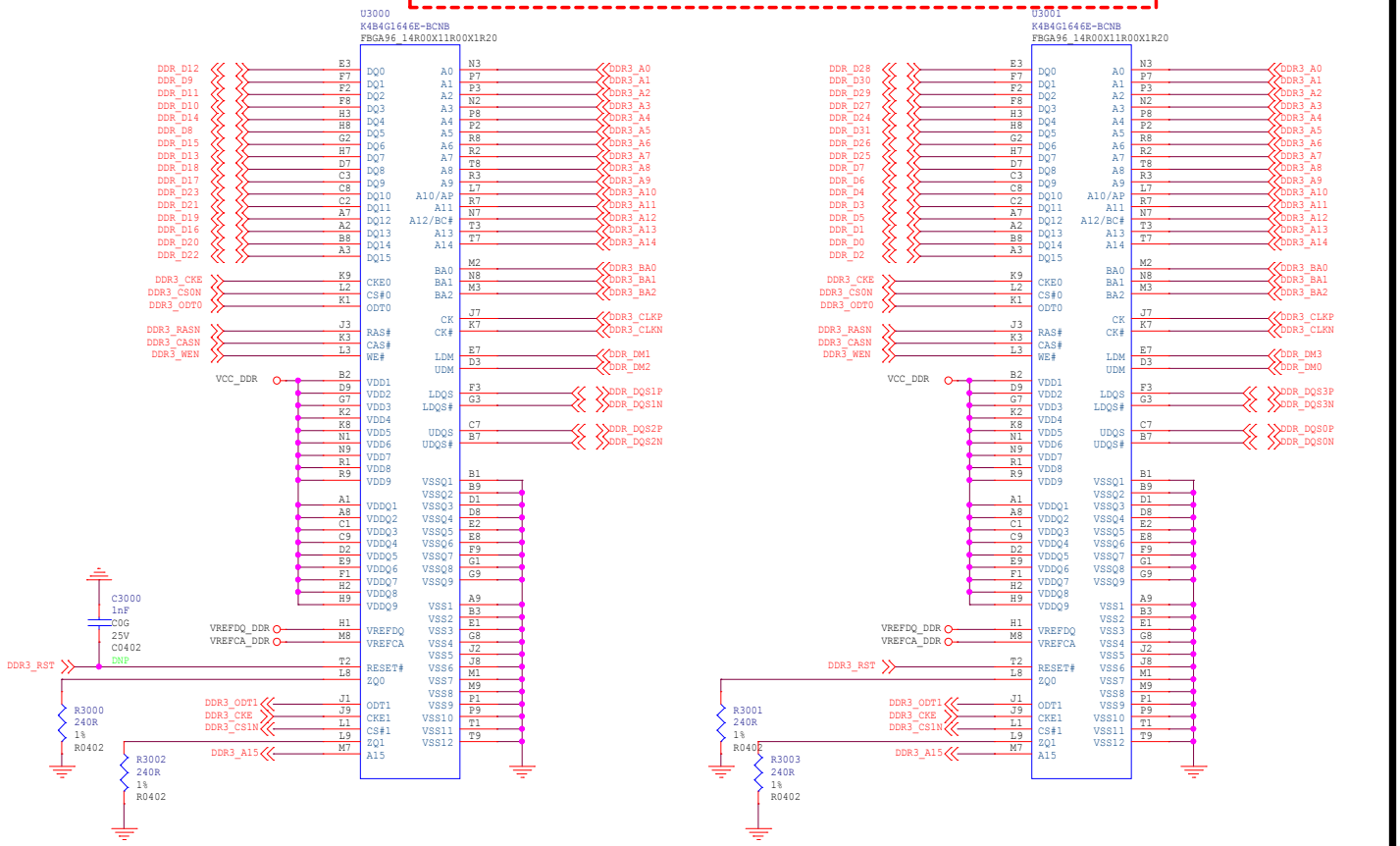
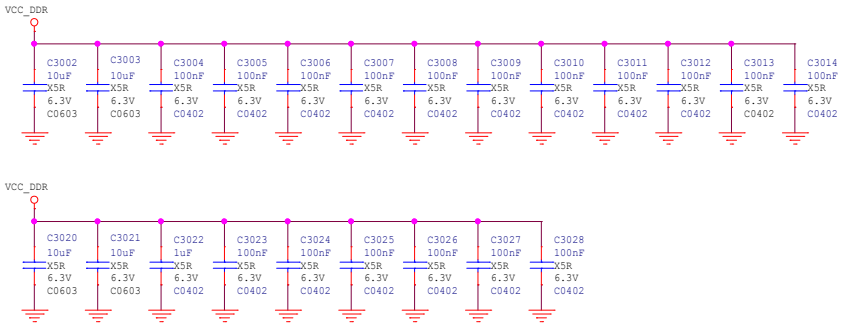
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	12.Power_DC IN		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	12 of 26

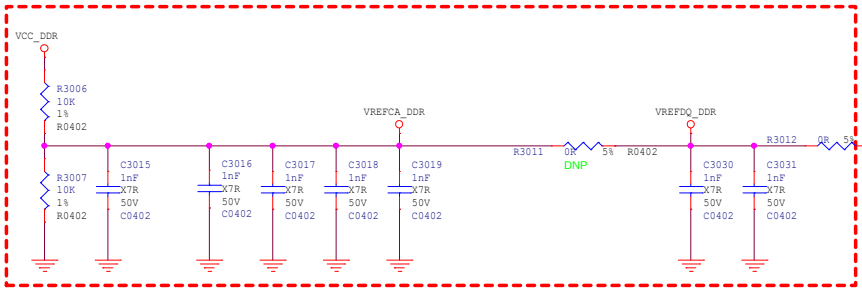
DDR3/DDR3L 2x16bit

NOTE:
This is a two DDR3 template. If only one DDR3 is used, please use DDR_DQ0 ~ DQ15
Refer to the latest AVL for parts selection.



Note:All the Power filter capacitors should be placed close to the power pins of DDR3





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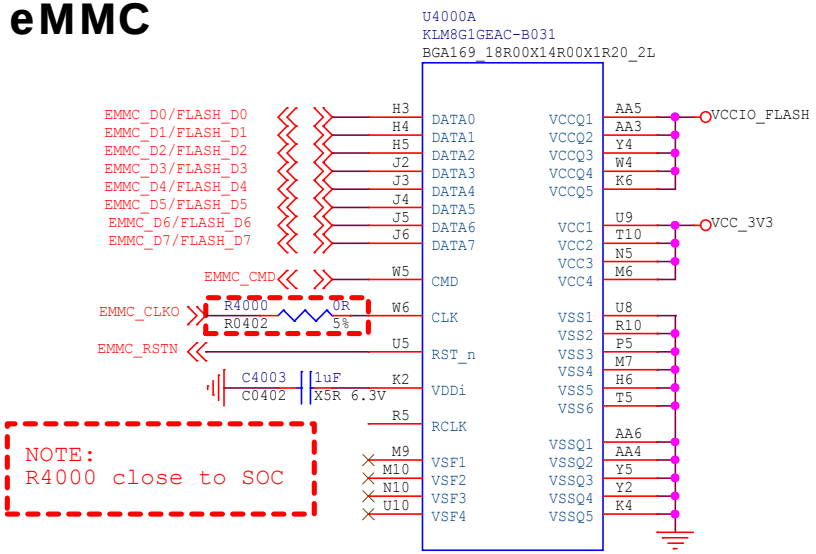
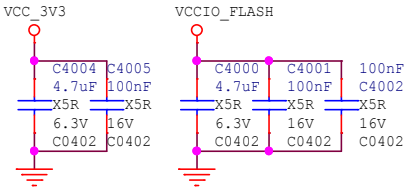
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	14.RAM_DDR3_96P_2X16bit		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	14 of 26

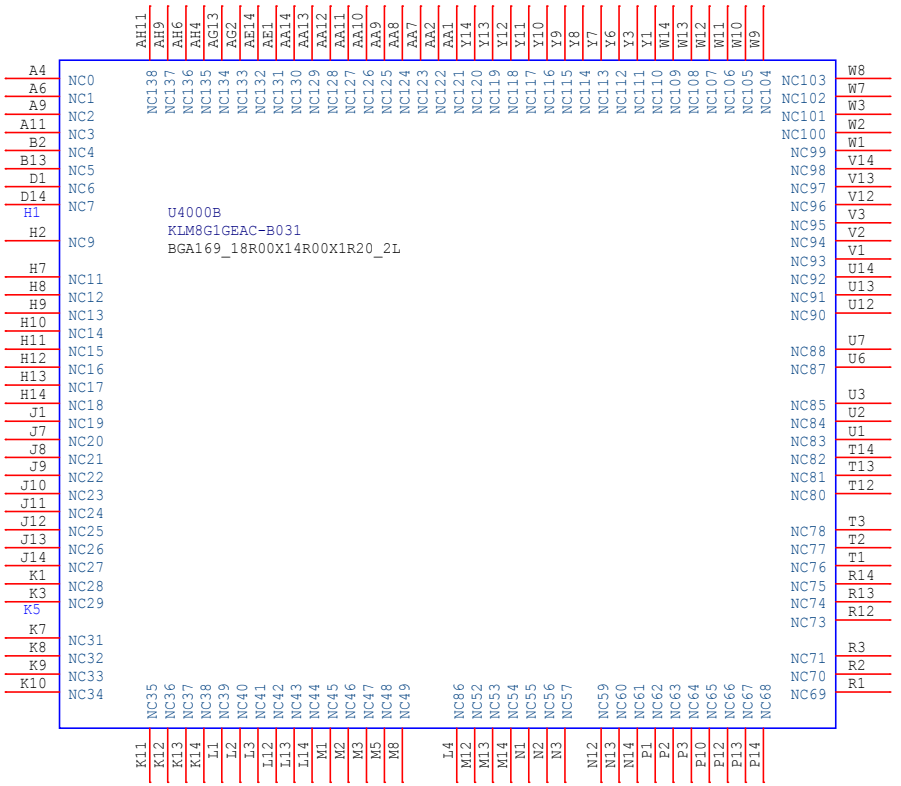
NOTE:
Refer to the latest AVL for parts selection.
NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

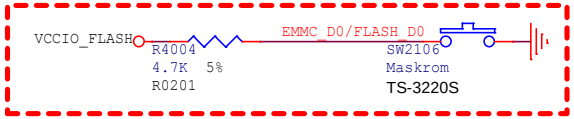
eMMC



NOTE:
R4000 close to SOC







NOTE:
Reserve testpoint for firmware update,
In the power on phase, if FLASH_D0= 0V,
the system will enter the maskROM mode

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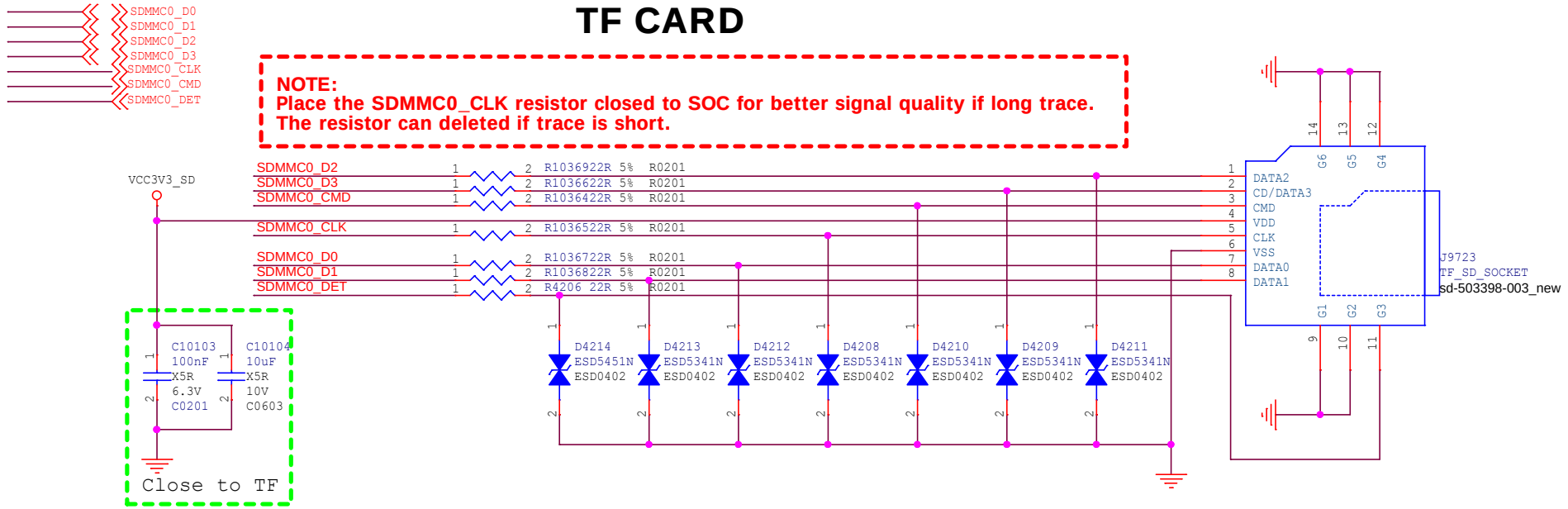
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	15.eMMC Flash		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	15of 26

TF CARD



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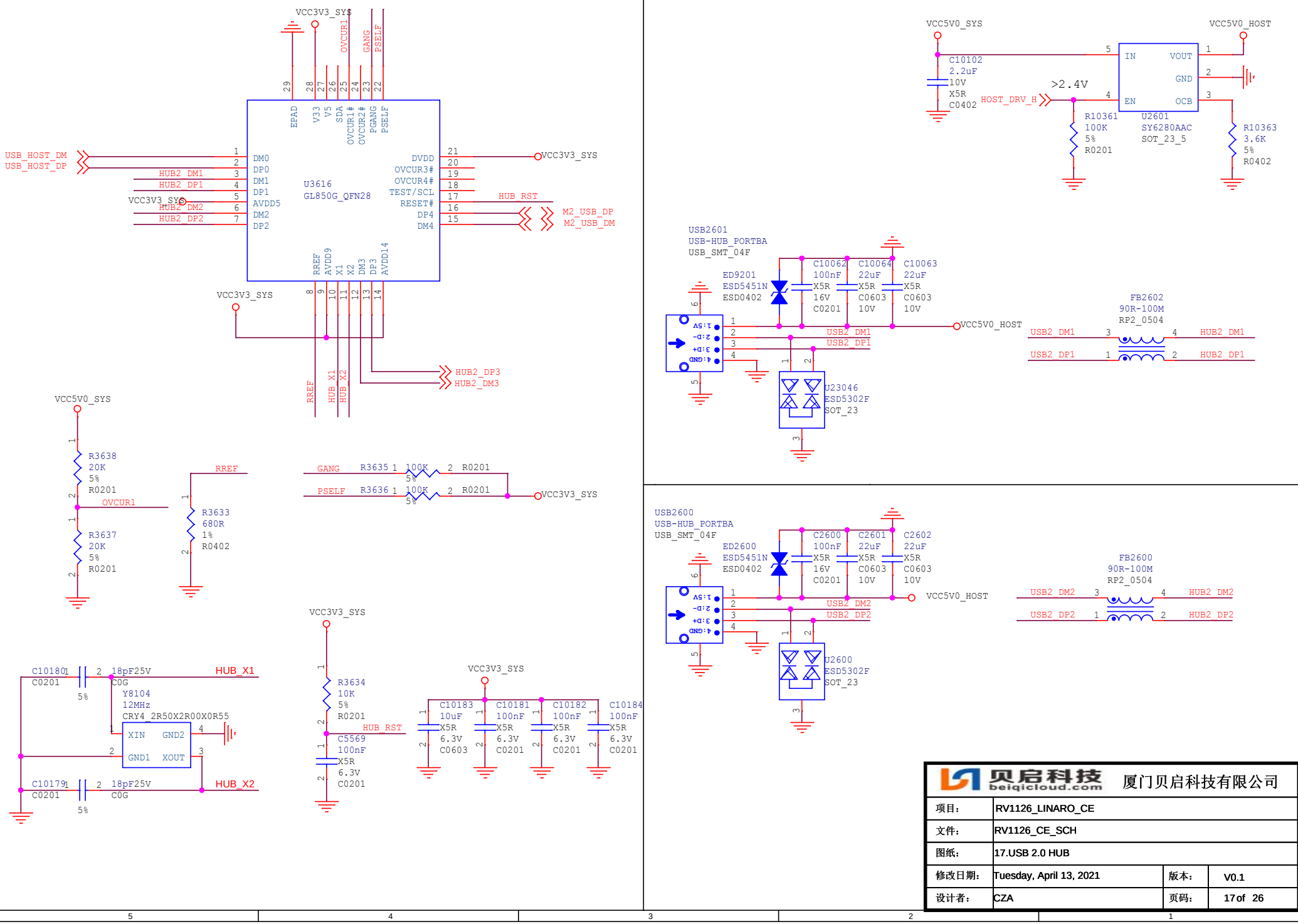
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	16.TF Card		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	16 of 26



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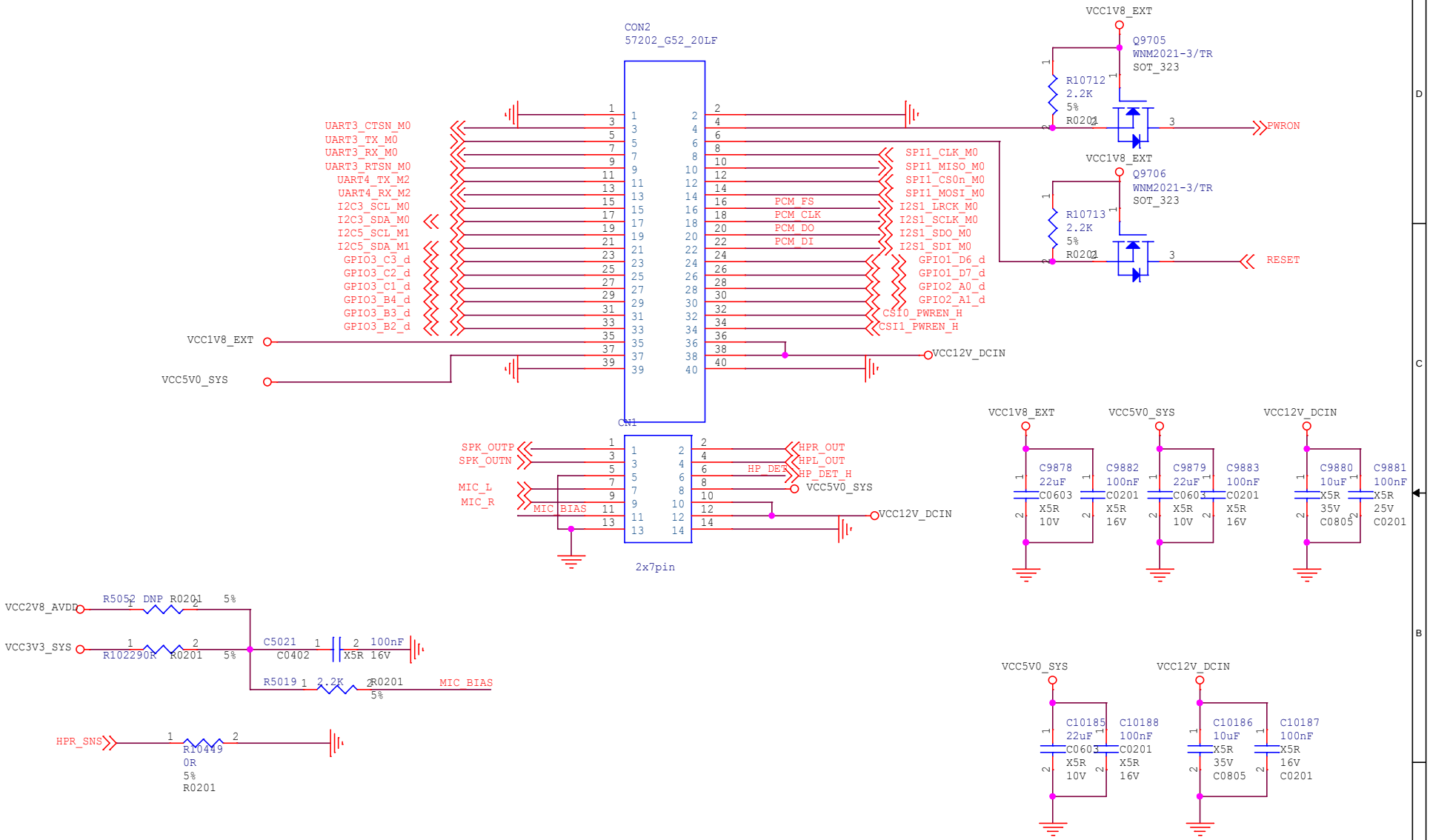
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	17.USB 2.0 HUB		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	17of 26



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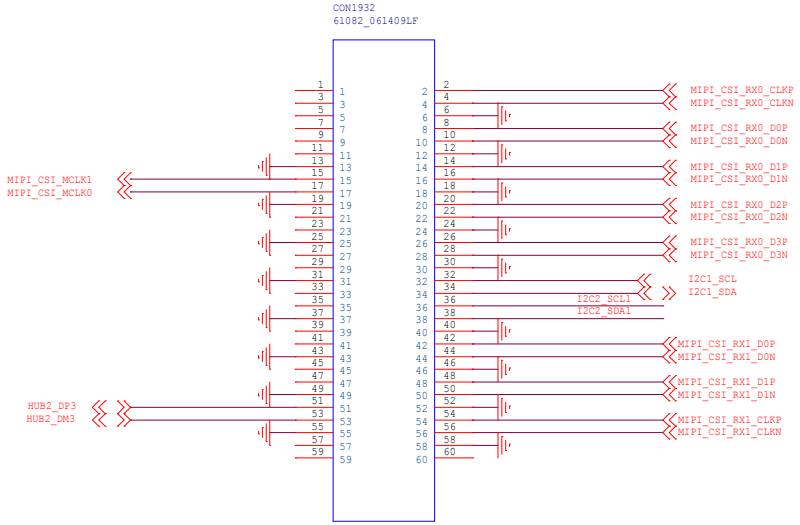
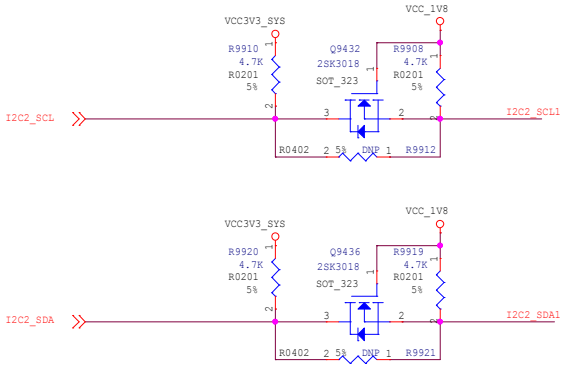
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	19.Low Speed IO EX		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	19 of 26





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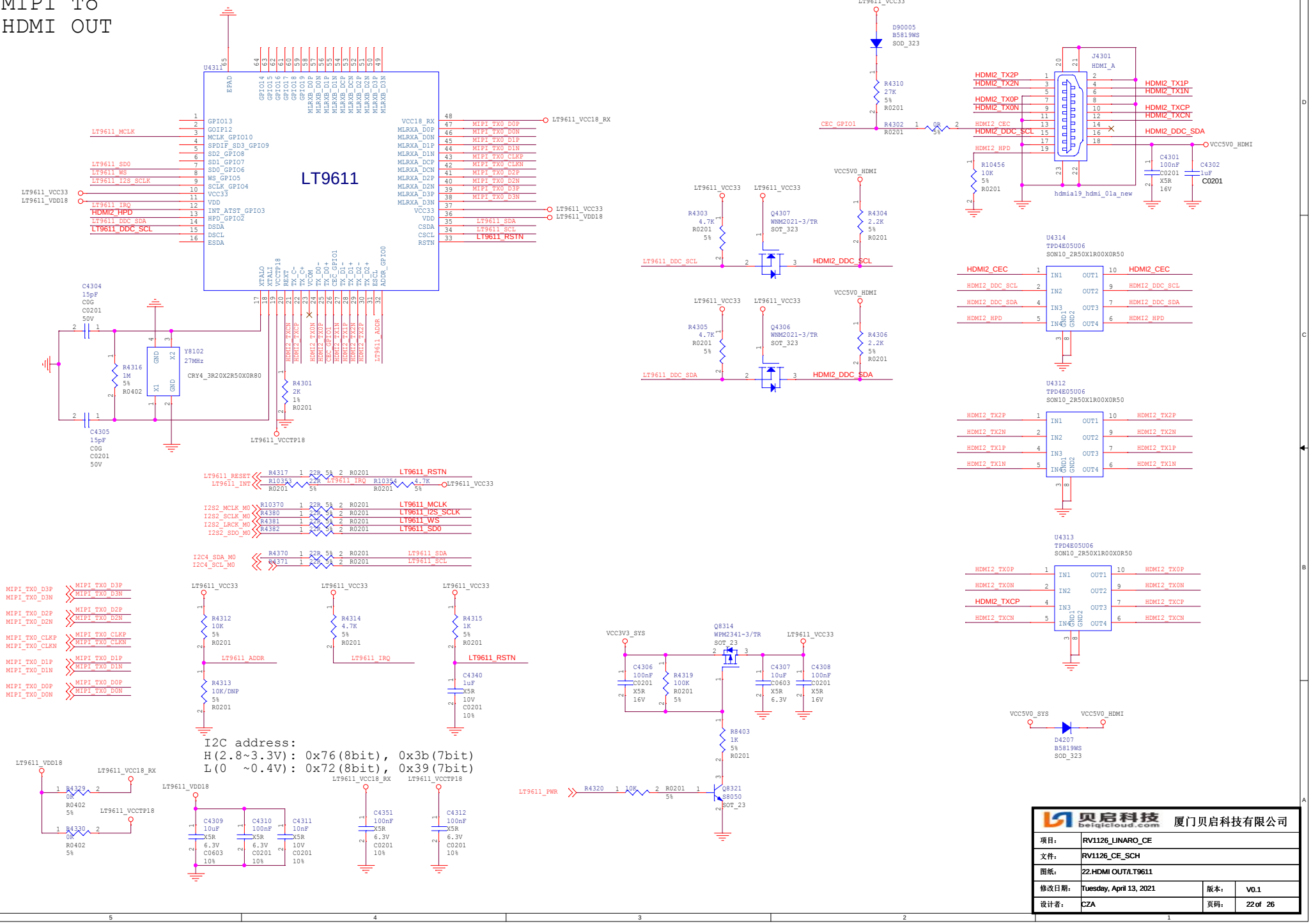
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	20.High speed Expansion_1		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	20 of 26

MIPI To HDMI OUT



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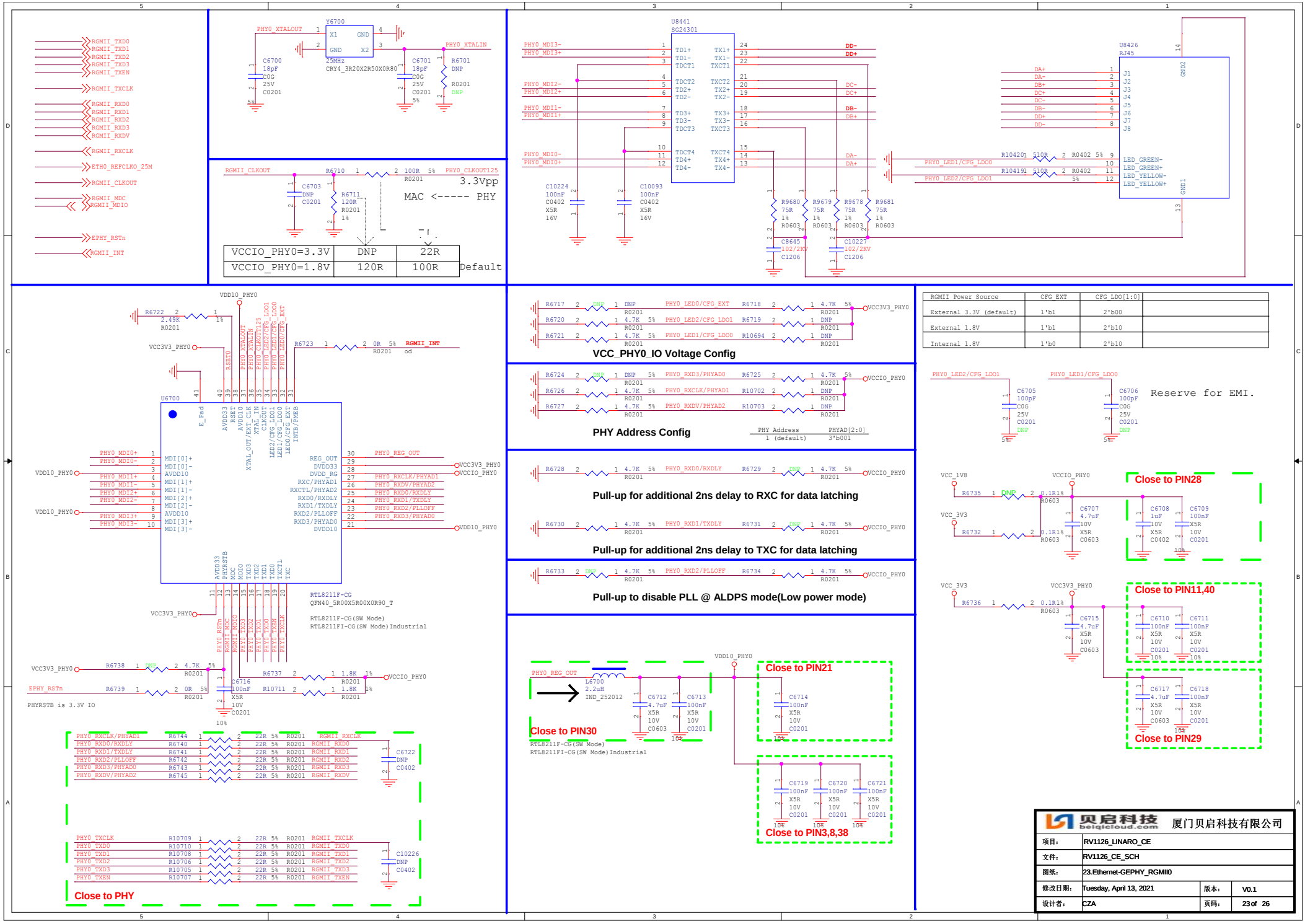
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	22.HDMI OUT/LT9611		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	22 of 26


RGMII_TXD0
RGMII_TXD1
RGMII_TXD2
RGMII_TXD3
RGMII_TXEN
RGMII_TXCLK
RGMII_RXD0
RGMII_RXD1
RGMII_RXD2
RGMII_RXD3
RGMII_RXDV
RGMII_RXCLK
ETH0_REFCLKO_25M
RGMII_CLKOUT
RGMII_MDC
RGMII_MDIO
EPHY_RSTn
RGMII_INT
Y6700
PHY0_XTALOUT
PHY0_XTALIN
25MHz
CRY4_3R20X2R50X0R80
C6700 18pF C0G 25V C0201
C6701 18pF C0G 25V C0201 5%
R6701 DNP
R0201 DNP
RGMII_CLKOUT
R6710 1 100R 5% R0201
PHY0_CLKOUT125
3.3Vpp
MAC <----- PHY
C6703 DNP C0201
R6711 120R R0201 1%
VCCIO_PHY0=3.3V | DNP | 22R
VCCIO_PHY0=1.8V | 120R | 100R Default
U8441
SG24301
PHY0_MDI3-
PHY0_MDI3+
PHY0_MDI2-
PHY0_MDI2+
PHY0_MDI1-
PHY0_MDI1+
PHY0_MDI0-
PHY0_MDI0+
TD1+ TD1- TDCT1 TX1+ TX1- TXCT1
TD2+ TD2- TDCT2 TX2+ TX2- TXCT2
TD3+ TD3- TDCT3 TX3+ TX3- TXCT3
TD4+ TD4- TDCT4 TX4+ TX4- TXCT4
DD- DD+ DC- DC+ DB- DB+ DA- DA+
C10224 100nF C0402 X5R 16V
C10093 100nF C0402 X5R 16V
R9680 R9679 R9678 R9681 75R 1% R0603
C8645 102/2KV C1206
C10223 102/2KV C1206
U8426
RJ45
J1 J2 J3 J4 J5 J6 J7 J8
GND2 GND1
R104201 510R R0402 5%
R104191 510R R0402 5%
LED_GREEN-
LED_GREEN+
LED_YELLOW-
LED_YELLOW+
PHY0_LED1/CFG_LDO0
PHY0_LED2/CFG_LDO1
VDD10_PHY0
R6722 2.49K R0201 1%
R6723 1 0R 5% R0201 RGMII_INT od
VCC3V3_PHY0
U6700
E_Pad
AVDD33 RSET AVDD10 XTAL_OUT/RXTL_CLK XTAL_IN/TXTL_CLK CLKOUT LED2/CFG_LDO1 LED1/CFG_LDO0 LED0/CFG_EXT INTB/PMEB
PHY0_MDI0+ PHY0_MDI0- PHY0_MDI1+ PHY0_MDI1- PHY0_MDI2+ PHY0_MDI2- PHY0_MDI3+ PHY0_MDI3-
MDI[0]+ MDI[0]- AVDD10 MDI[1]+ MDI[1]- MDI[2]+ MDI[2]- AVDD10 MDI[3]+ MDI[3]-
REG_OUT DVDD33 DVDD_RG RXC/PHYAD1 RXCTL/PHYAD2 RXD0/RXDLY RXD1/TXDLY RXD2/PLLOFF RXD3/PHYAD0 DVDD10
PHY0_REG_OUT
PHY0_RXCLK/PHYAD1
PHY0_RXDV/PHYAD2
PHY0_RXD0/RXDLY
PHY0_RXD1/TXDLY
PHY0_RXD2/PLLOFF
PHY0_RXD3/PHYAD0
AVDD33 PHYRSTB MDC MDIO TXD3 TXD2 TXD1 TXD0 TXCTL TXC
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
R6738 DNP 4.7K R0201
R6739 0R R0201
R6737 1.8K R0201
R10711 1.8K R0201
C6716 100nF X5R 10V C0201 10%
EPHY_RSTn
PHYRSTB is 3.3V IO
PHY0_RXCLK/PHYAD1 R6744 RGMII_RXCLK
PHY0_RXD0/RXDLY R6740 RGMII_RXD0
PHY0_RXD1/TXDLY R6741 RGMII_RXD1
PHY0_RXD2/PLLOFF R6742 RGMII_RXD2
PHY0_RXD3/PHYAD0 R6743 RGMII_RXD3
PHY0_RXDV/PHYAD2 R6745 RGMII_RXDV
22R 5% R0201
C6722 DNP C0402
PHY0_TXCLK R10709 RGMII_TXCLK
PHY0_TXD0 R10710 RGMII_TXD0
PHY0_TXD1 R10708 RGMII_TXD1
PHY0_TXD2 R10706 RGMII_TXD2
PHY0_TXD3 R10705 RGMII_TXD3
PHY0_TXEN R10707 RGMII_TXEN
C10226 DNP C0402
Close to PHY
R6717 R6720 R6721 DNP 4.7K R0201
PHY0_LED0/CFG_EXT R6718
PHY0_LED2/CFG_LDO1 R6719
PHY0_LED1/CFG_LDO0 R10694
VCC3V3_PHY0
VCC_PHY0_IO Voltage Config
R6724 R6726 R6727 DNP 4.7K R0201
PHY0_RXD3/PHYAD0 R6725
PHY0_RXCLK/PHYAD1 R10702
PHY0_RXDV/PHYAD2 R10703
VCCIO_PHY0
PHY Address Config
PHY_Address | PHYAD[2:0]
1 (default) | 3'b001
R6728 4.7K R0201
PHY0_RXD0/RXDLY R6729
Pull-up for additional 2ns delay to RXC for data latching
R6730 4.7K R0201
PHY0_RXD1/TXDLY R6731
Pull-up for additional 2ns delay to TXC for data latching
R6733 4.7K R0201
PHY0_RXD2/PLLOFF R6734
Pull-up to disable PLL @ ALDPS mode(Low power mode)
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V (default) | 1'b1 | 2'b00
External 1.8V | 1'b1 | 2'b10
Internal 1.8V | 1'b0 | 2'b10
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
C6705 100pF C0G 25V C0201 DNP
C6706 100pF C0G 25V C0201 DNP
Reserve for EMI.
VCC_1V8
VCCIO_PHY0
VCC_3V3
R6735 DNP 0.1R1% R0603
R6732 0.1R1% R0603
C6707 4.7uF 10V X5R C0603
C6708 1uF 10V X5R C0402
C6709 100nF 10V X5R C0201
Close to PIN28
VCC3V3_PHY0
R6736 0.1R1% R0603
C6715 4.7uF X5R 10V C0603
C6710 100nF X5R 10V C0201
C6711 100nF X5R 10V C0201
Close to PIN11,40
C6717 4.7uF X5R 10V C0603
C6718 100nF X5R 10V C0201
Close to PIN29
PHY0_REG_OUT
L6700 2.2uH IND_252012
C6712 4.7uF X5R 10V C0603
C6713 100nF X5R 10V C0201
Close to PIN30
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
C6714 100nF X5R 10V C0201
Close to PIN21
C6719 C6720 C6721 100nF X5R 10V C0201
Close to PIN3,8,38
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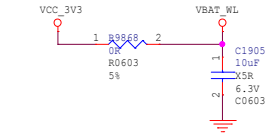
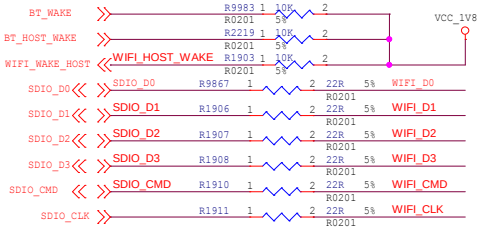
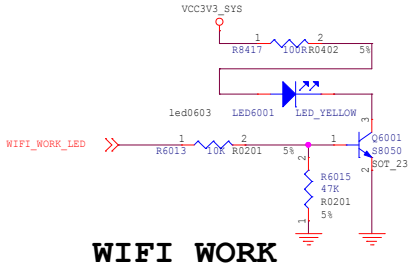
项目: RV1126_LINARO_CE
文件: RV1126_CE_SCH
图纸: 23.Ethernet-GEPHY_RGMII0
修改日期: Tuesday, April 13, 2021 版本: V0.1
设计者: CZA 页码: 23 of 26

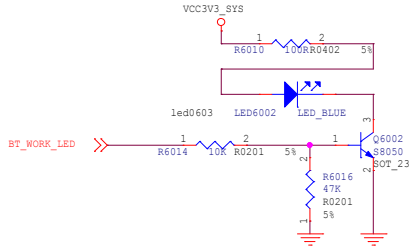
WIFI/BT MODULE



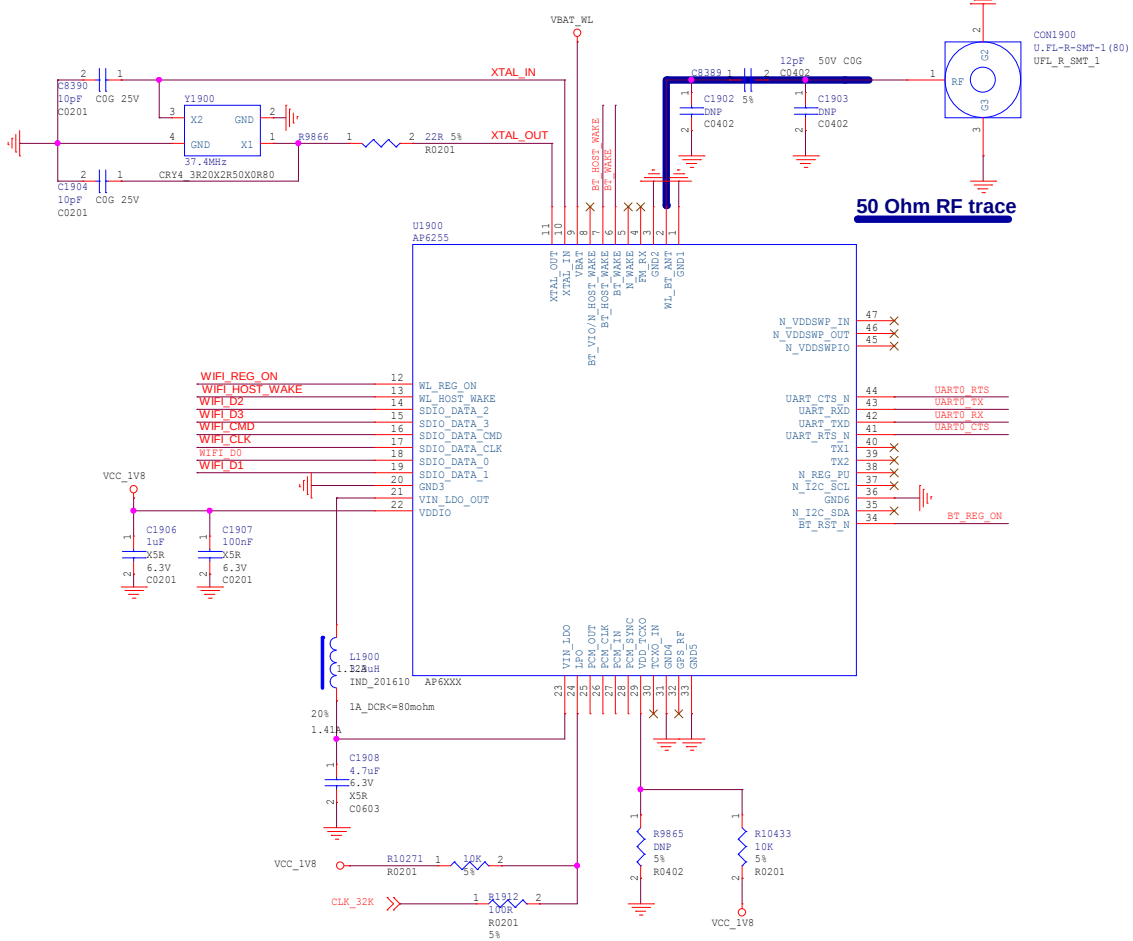




WIFI WORK



BT WORK



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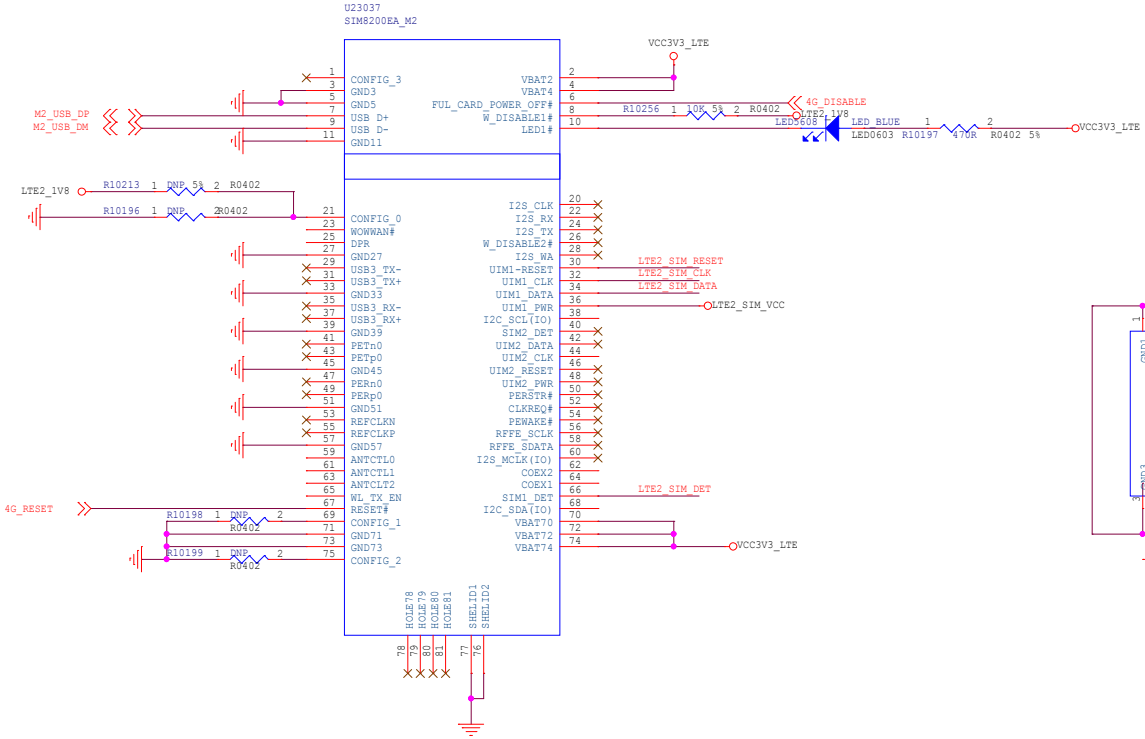
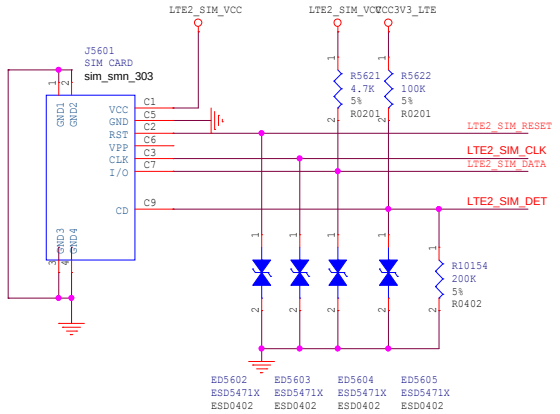
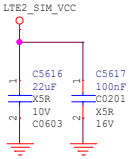
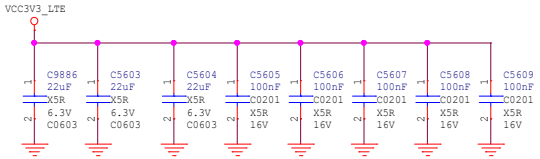
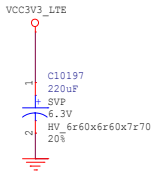
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	24.wifi6255		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	24 of 26



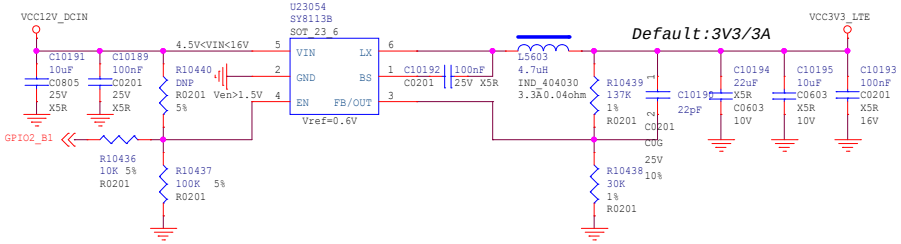








VCC5V0_SYS



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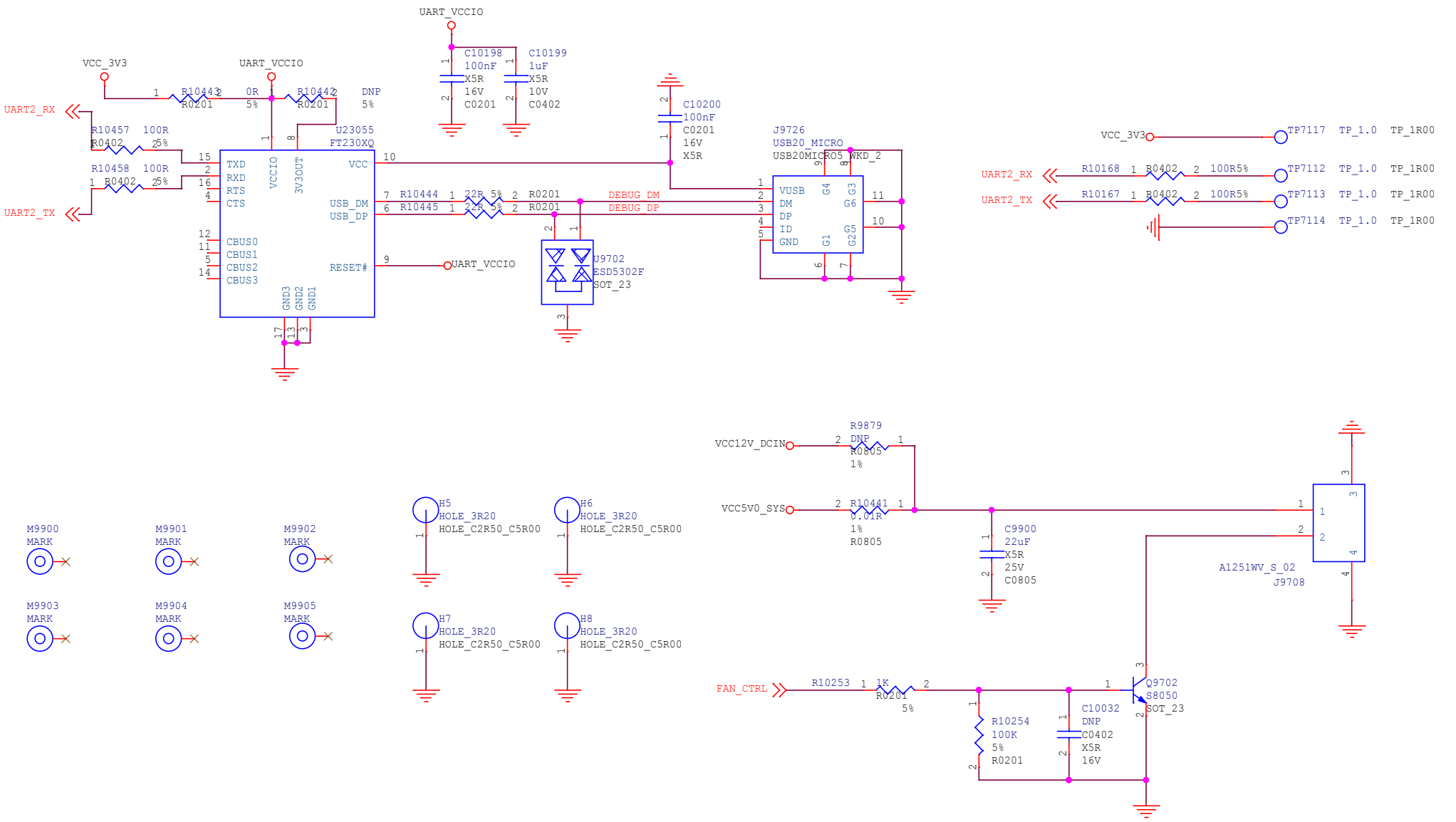
项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	25.M2		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	25 of 26



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项目：	RV1126_LINARO_CE		
文件：	RV1126_CE_SCH		
图纸：	26.DEBUG/FAN		
修改日期：	Tuesday, April 13, 2021	版本：	V0.1
设计者：	CZA	页码：	26 of 26