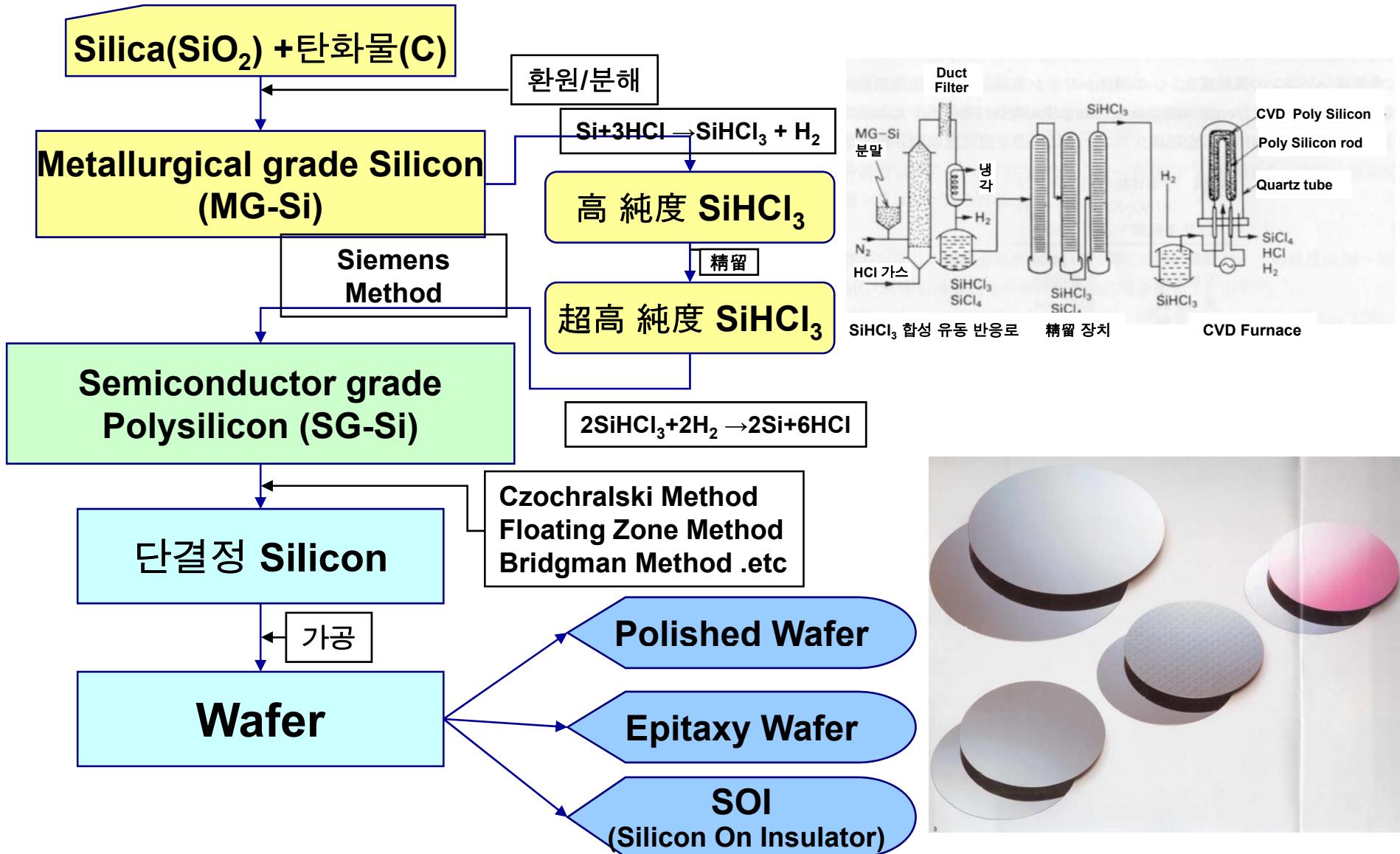


반도체 Process 기본

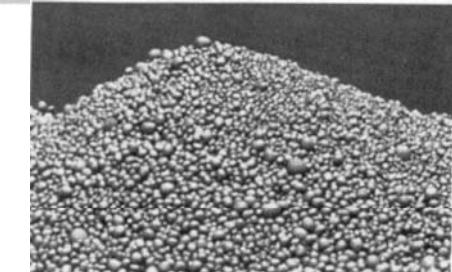
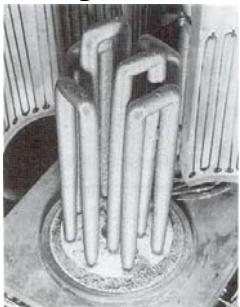
- Wafer 제조 과정
- Introduction
- 반도체 Process
 - Lithography
 - Etch
 - Diffusion
 - Thin Film
 - Capacitor
 - CMP & Cleaning
- 반도체 Integration Process
 - Isolation
 - Word Line
 - Landing Pad Contact
 - Bit Line
 - Storage Node Contact
 - Capacitor
 - MLM
- Failure analysis

Wafer 제조과정



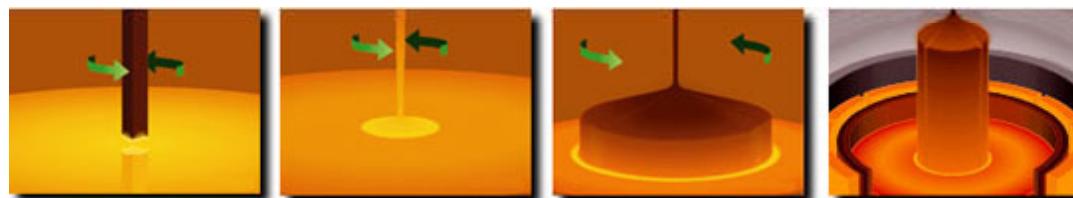
Wafer 제조과정

▶ Poly Silicon

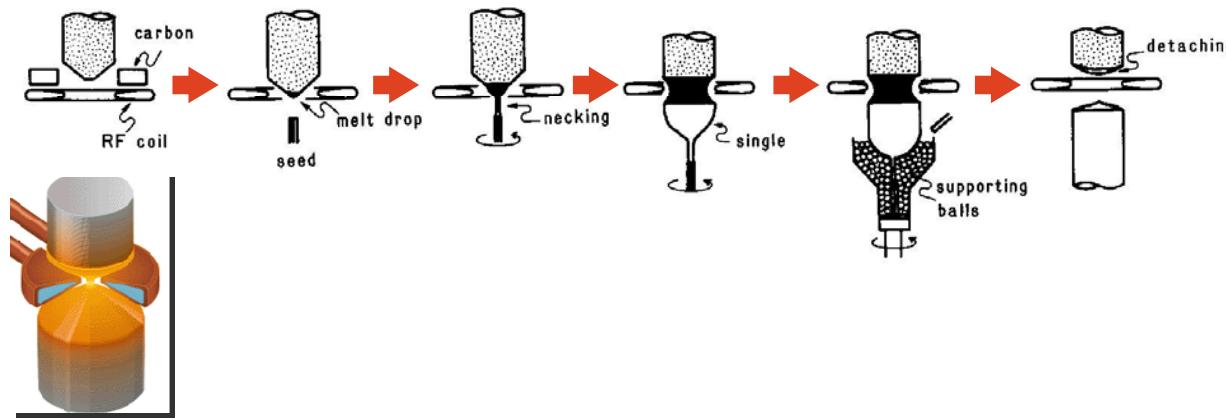


▶ 단결정 Silicon 제조방법

· Czochralski Method

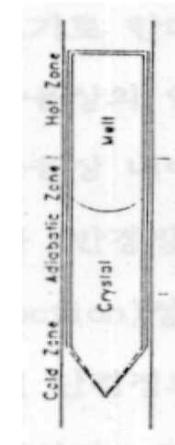


· Floating Zone method



Poly Silicon Granule

· Bridgman method

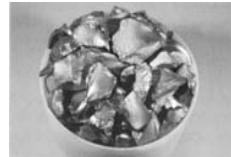


Wafer 제조과정

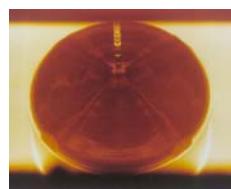
▶ 1916년 ‘Czochralski’에 의해 금속의 결정 성장 실험 방법으로 고안됨.
‘Teal’, ‘Little’, ‘Buhler’가 Si, Ge 결정 성장에 처음 적용함.

< Growing Process >

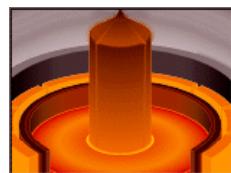
Poly Silicon Charge Preparation



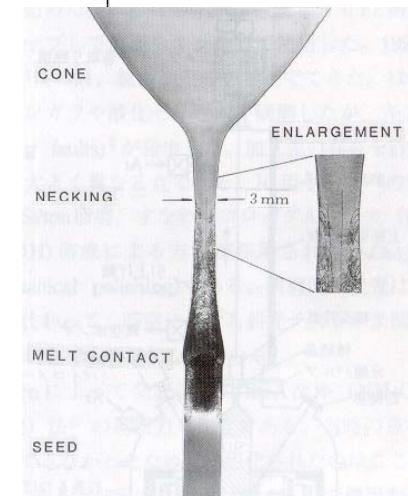
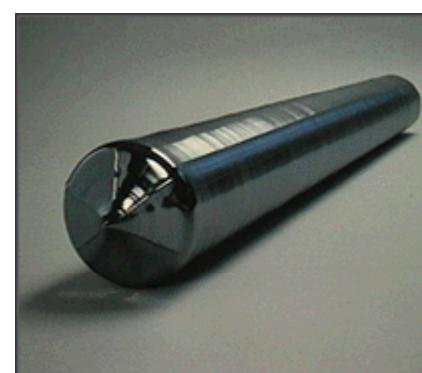
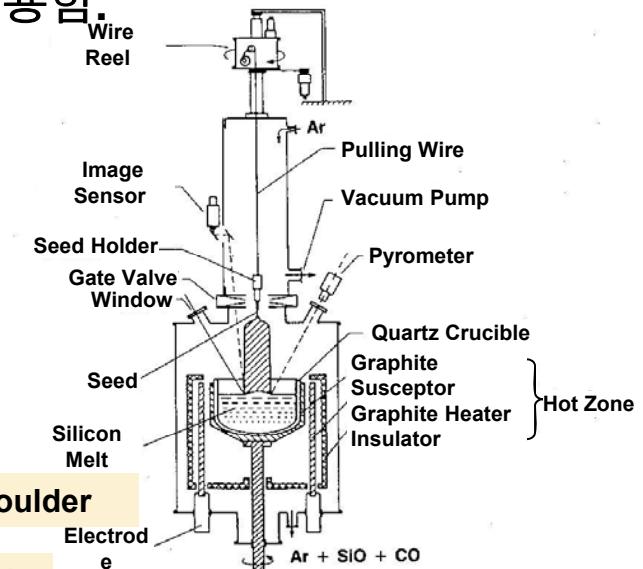
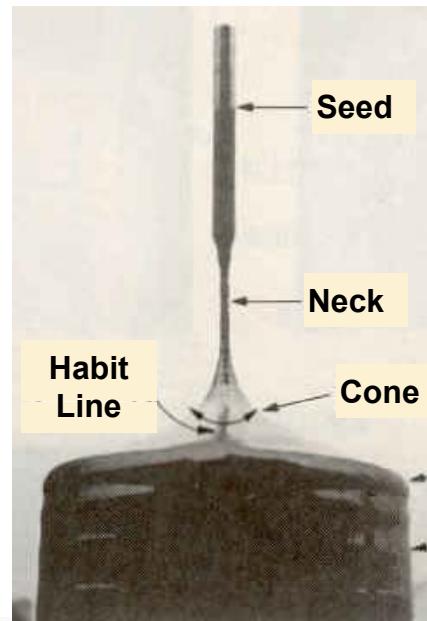
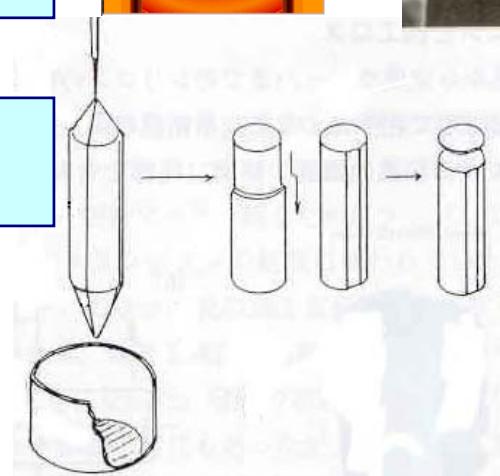
Growing



Cropping

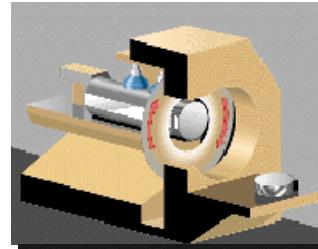
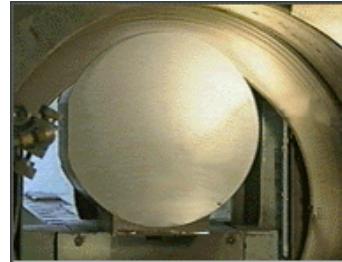
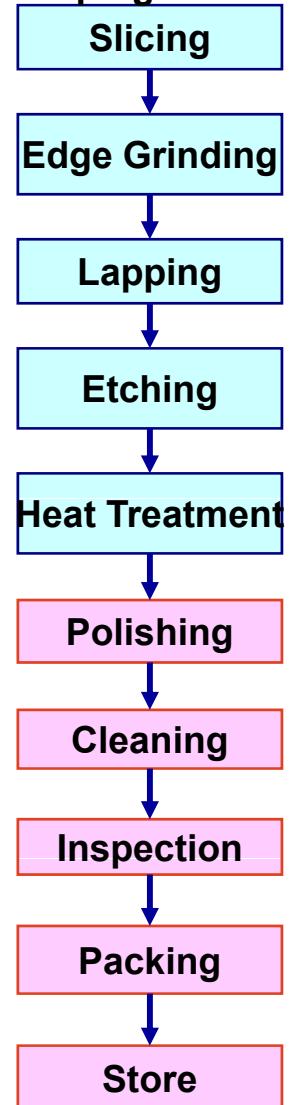


Ingot Store



Wafer 제조과정

< Shaping Process >



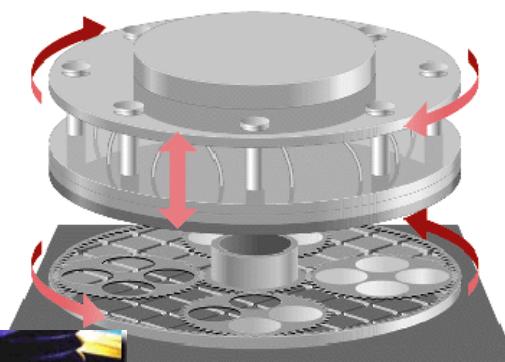
< ID Sawing >

< Heat Treatment >

- $600 \sim 800^{\circ}\text{C} \rightarrow 450^{\circ}\text{C}$ 급냉
- Thermal Donor (Oxygen) 제거 및 Stress 제거

< Lapping >

- 표면 흠 제거, 두께 / 면간 평행을 유지시킴.

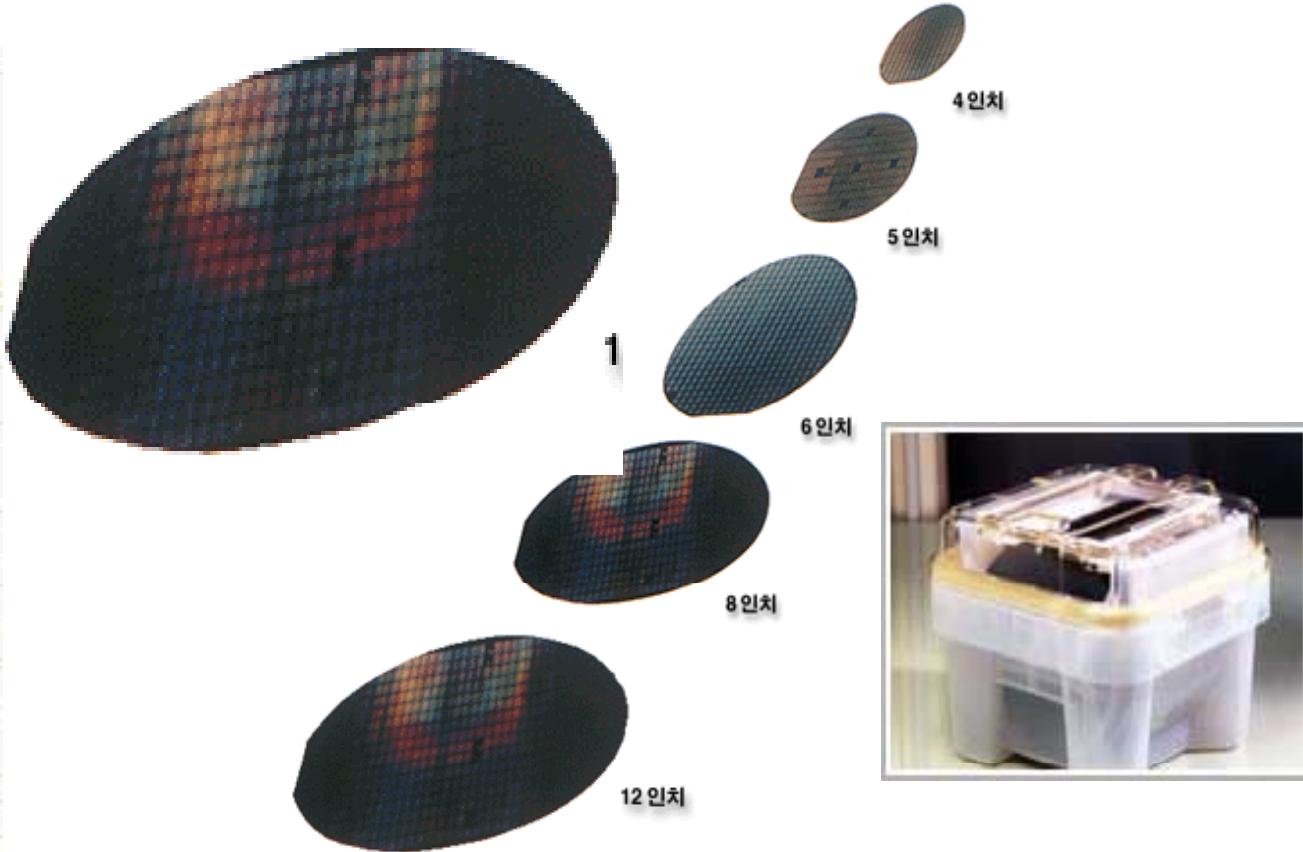
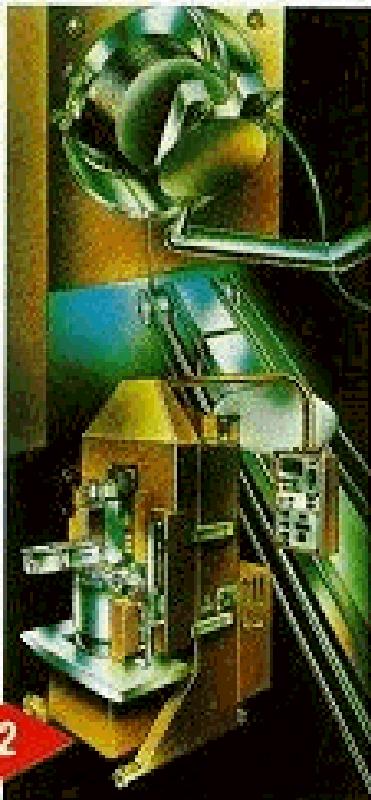


< Polishing >

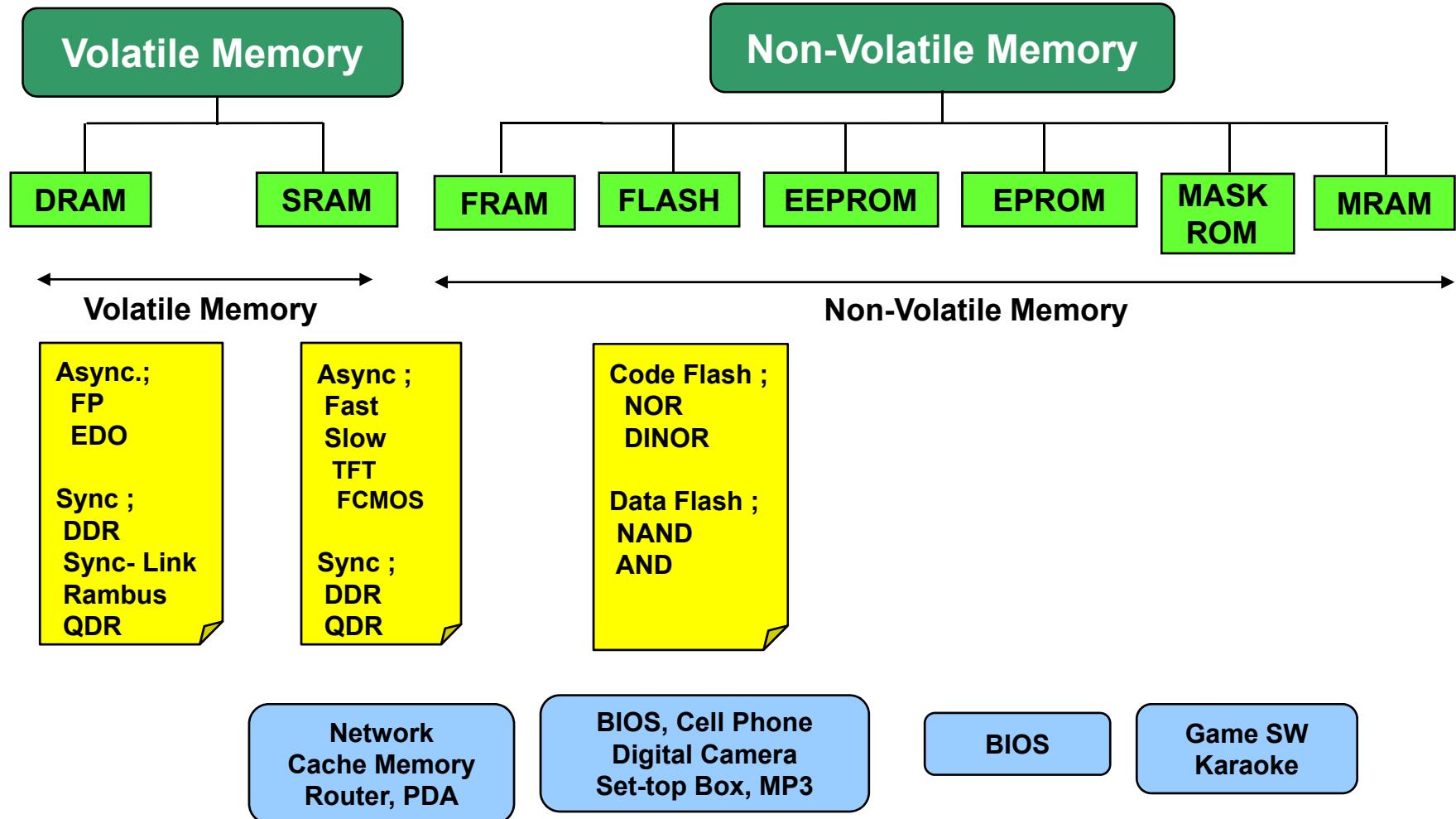
Wafer 제조과정

성장된 규소봉을 균일한 두께의 얇은 웨이퍼로 잘라낸다.

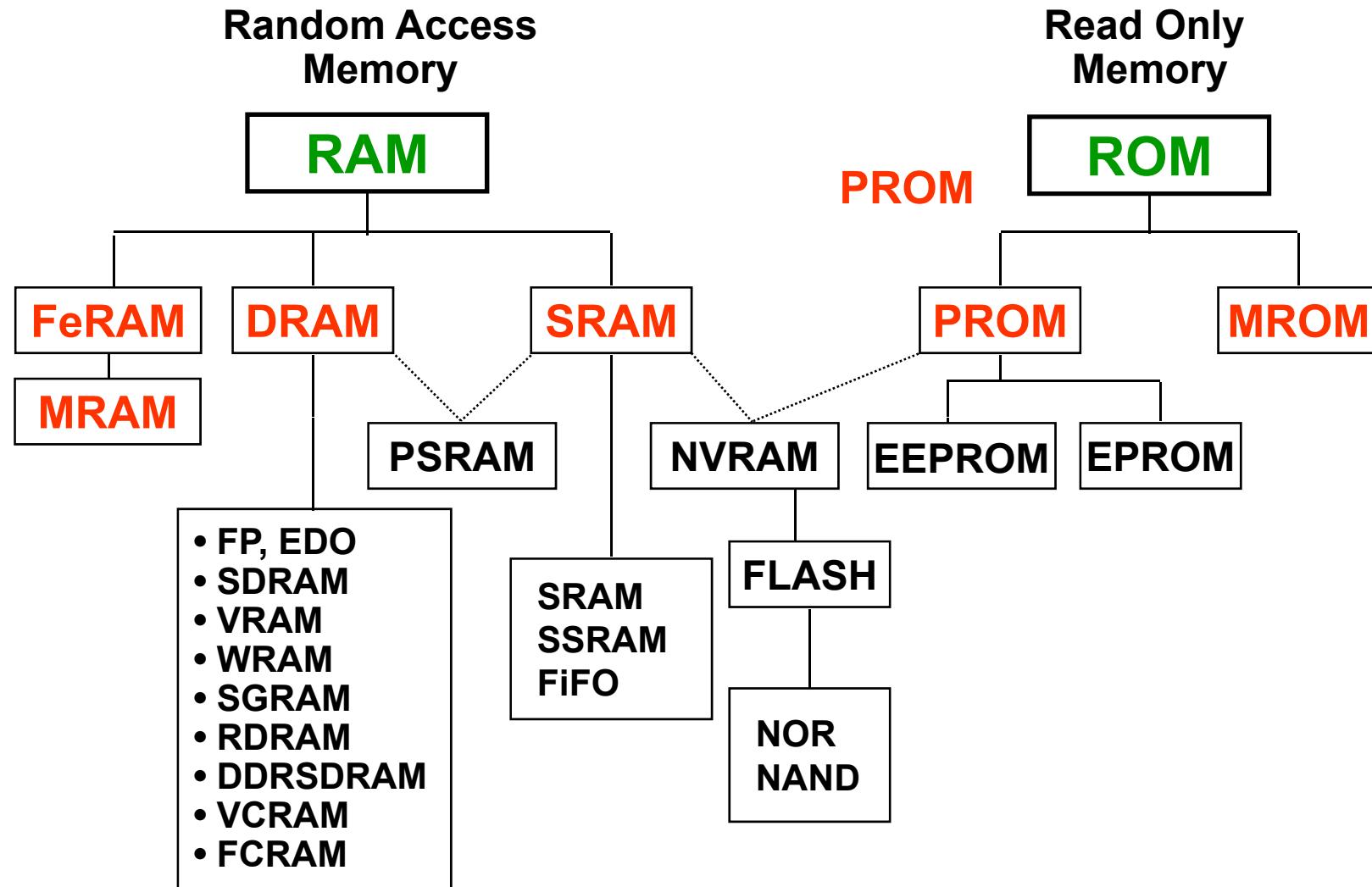
웨이퍼의 크기는 규소봉의 구경에 따라 3", 4", 6", 8", 12"로 만들어지며 생산성 향상을 위해 점점 대구경화 경향을 보이고 있음



Tree of MOS Memories



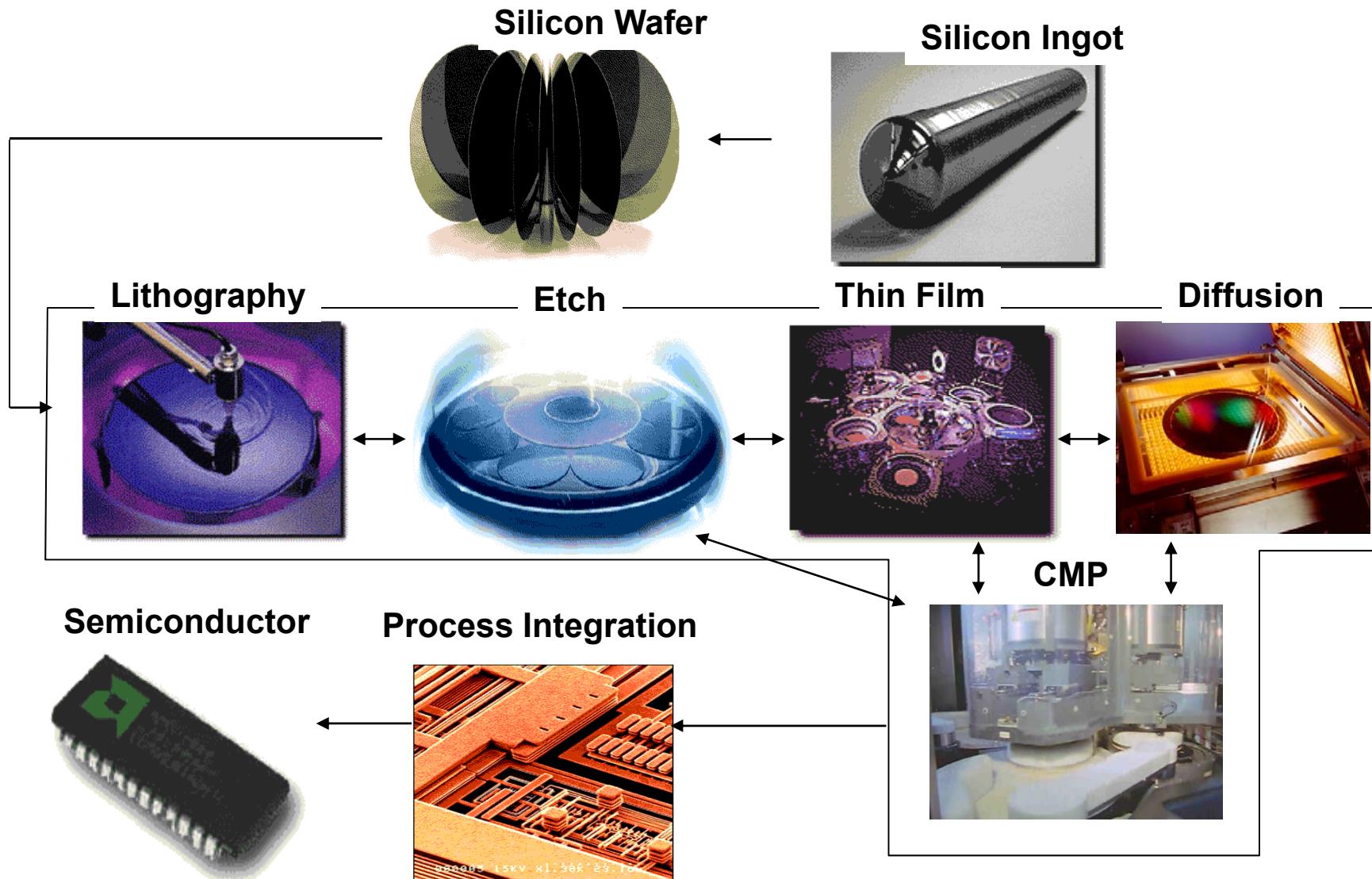
Tree of MOS Memories



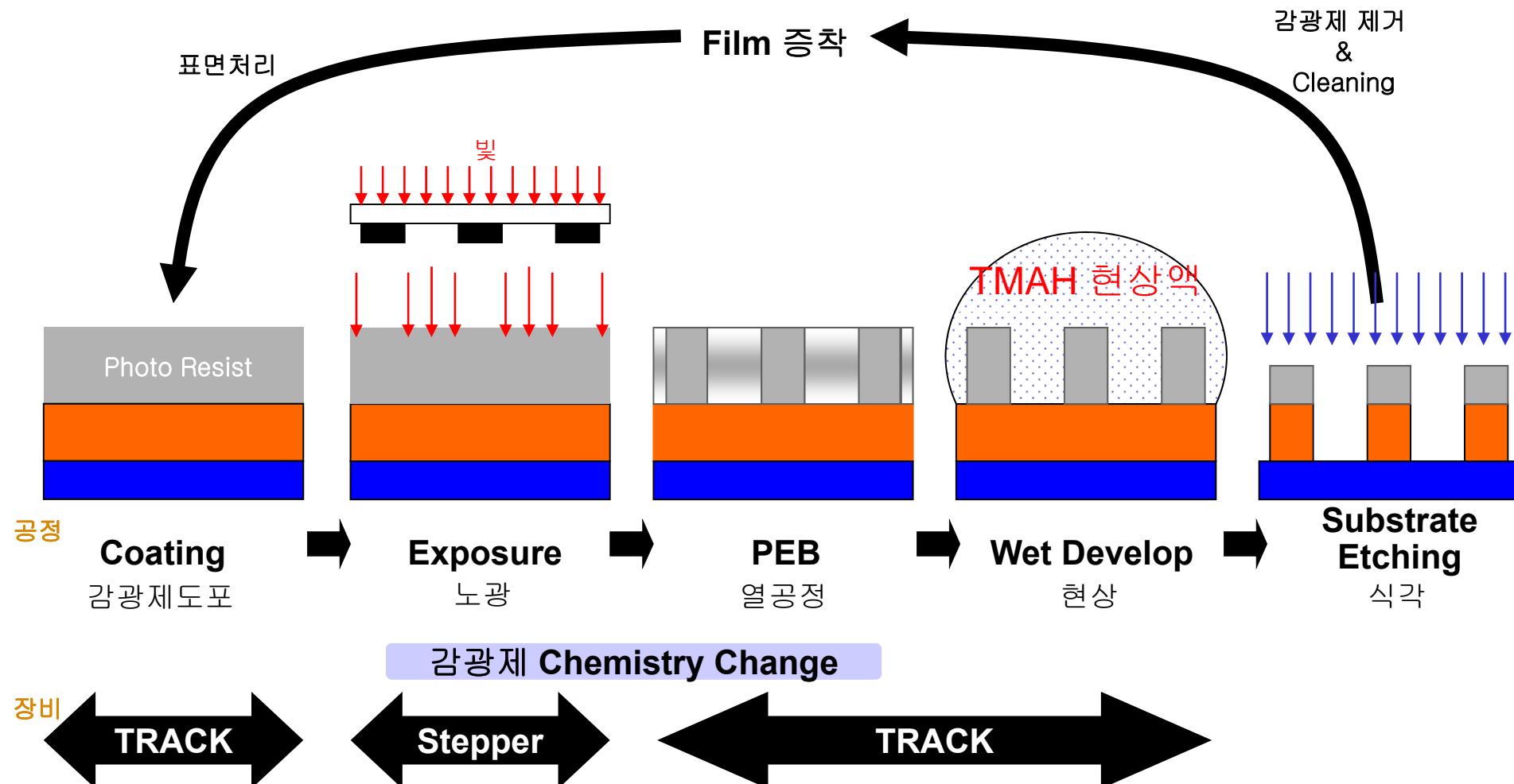
Comparison of MOS Memory Cells

DRAM	SRAM	Flash	FRAM	MRAM
<p>WL Capacitor BL</p>	<p>WL Vcc Load BL Vss BL</p>	<p>WL BL CG FG</p>	<p>WL BL F-Cap.</p>	<p>WL BL MTJ WL2</p>
<p>$Q = C(v)dv$</p>		<p>$\Delta V = \frac{I_{inj} dt}{C_{ox}}$</p>	<p>Pr</p>	<p>M_r</p>
1T + 1C	6Tr or 4Tr + 2Load	1T	1T + 1C (2T + 2C)	1T+1MTJ (1D+MTJ, 1MTJ)
Destructive Readout	Non-destructive Readout	Non-destructive Readout	Destructive Readout	Non-destructive Readout
Refresh	No refresh	No refresh	No refresh	No refresh
Volatile	Volatile	Non-volatile	Non-volatile	Non-volatile
Sub 8F2	60~120F2	4F2	12F2	4F2~8F2

반도체 제조 과정



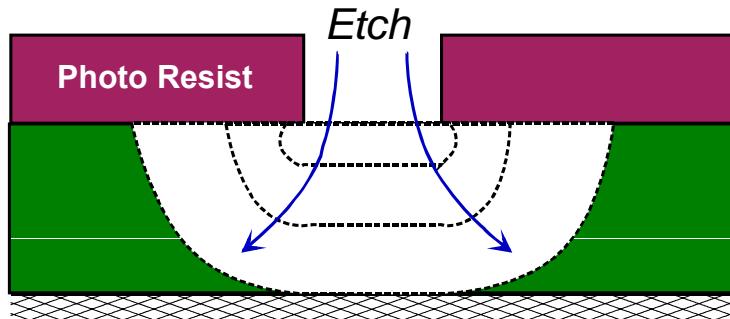
반도체 Process - *Lithography*



반도체 Process - Etch

Wet Etching

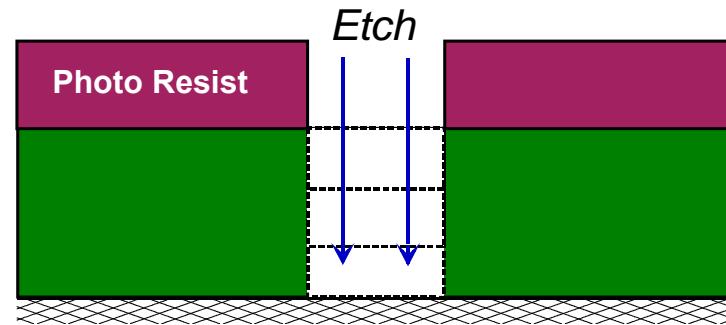
- by Wet chemical solution
- Isotropic etching



Vertical E/R = Horizontal E/R
Pure Chemical Reaction
High Selectivity
CD Loss or Gain
High Pressure
Batch Wafer Type
Less Electrical Damage

Dry Etching

- by Plasma
- Anisotropic etching

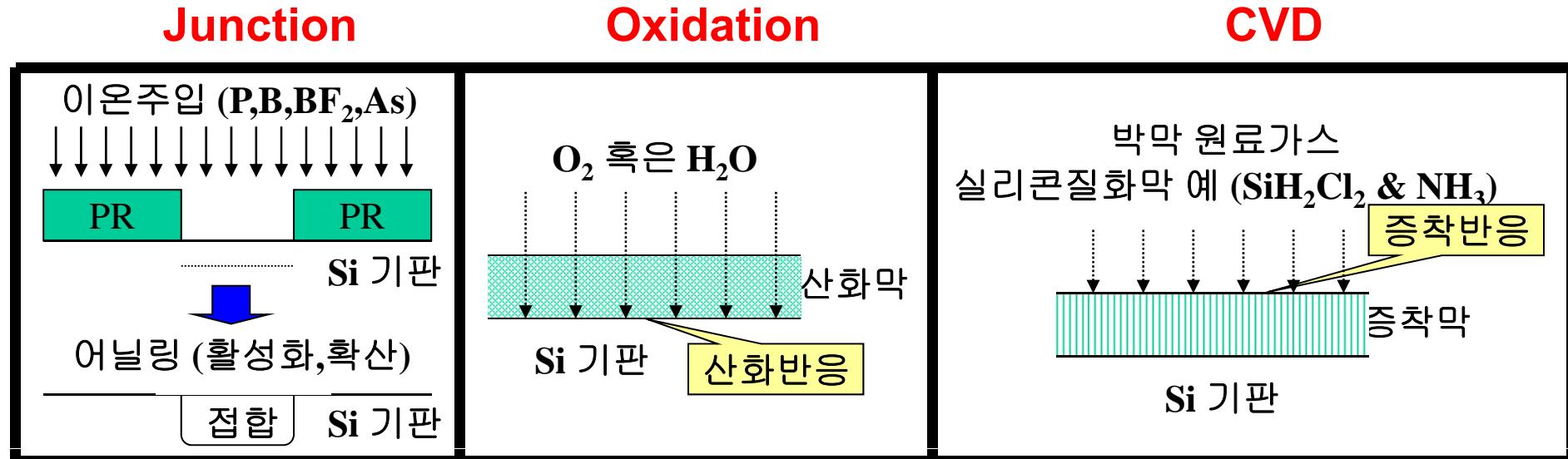


Vertical E/R >> Horizontal E/R
Ion assisted
Relatively low Selectivity
No CD bias
Low Pressure
High Directionality
Single Wafer Type
Low Etch rate
Purely Physical Process

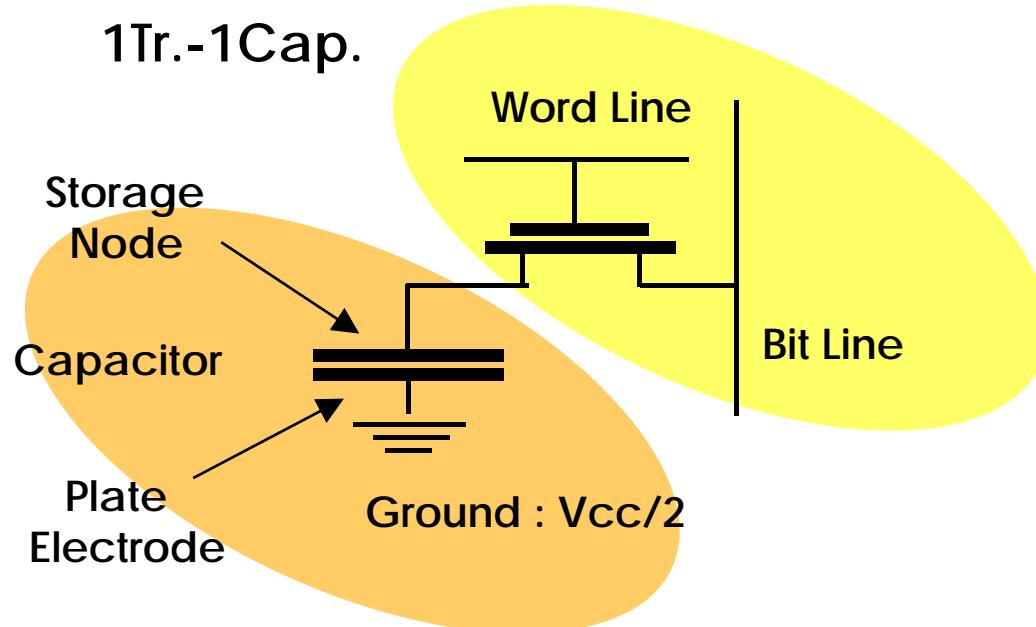
반도체 Process - Diffusion

Diffusion/Oxidation/Thermal CVD 공정을 통상 Diffusion 공정이라고 약칭함

- Diffusion : Si 기판 내 도펀트 주입 후 후속 열공정에 의한 도펀트의 Si 내 확산
- 산화반응 : O₂, H₂O의 확산에 의한 Si 기판 산화
- 화학기상증착 : 박막을 구성하는 원소를 함유한 가스분자를 일정 온도, 압력 하에서 기판 표면으로 공급하여 표면에서 화학증착 반응을 유도



반도체 Process – Capacitor



- Requirements
 - Capacitance $\geq 25fF/cell$
 - LKG $< 1fA/cell$

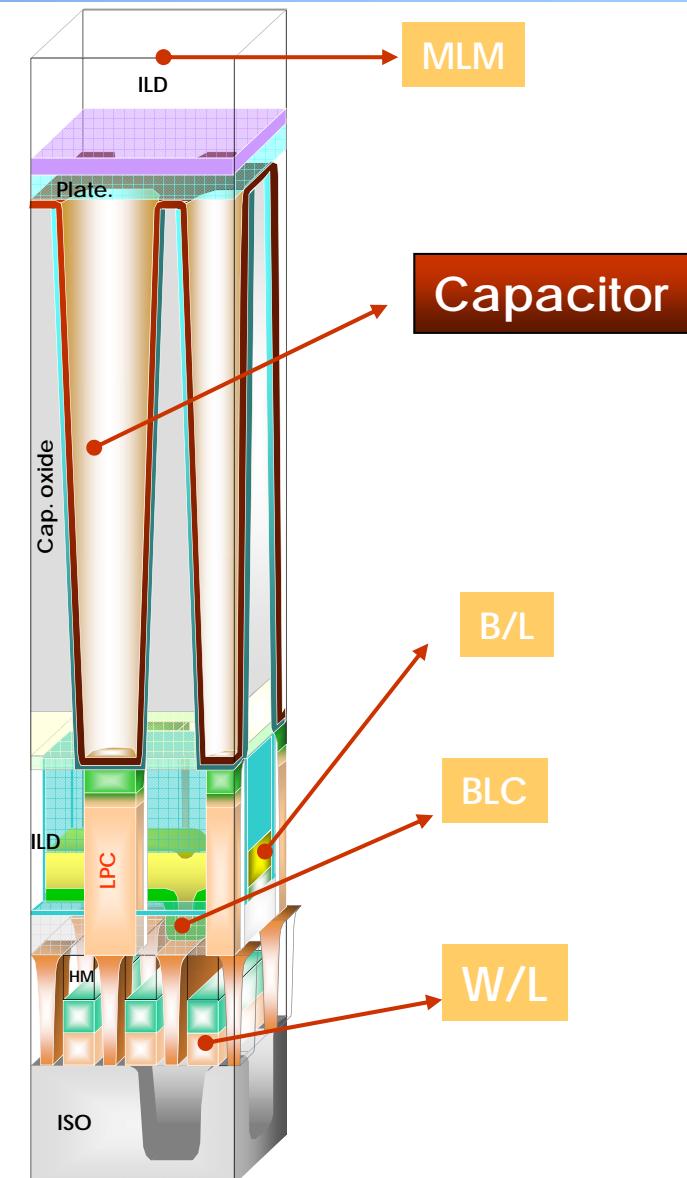
Capacitor - 전하를 저장하는 소자

모든 물질(진공 포함)은 전하를 저장하는 특성이 있다.

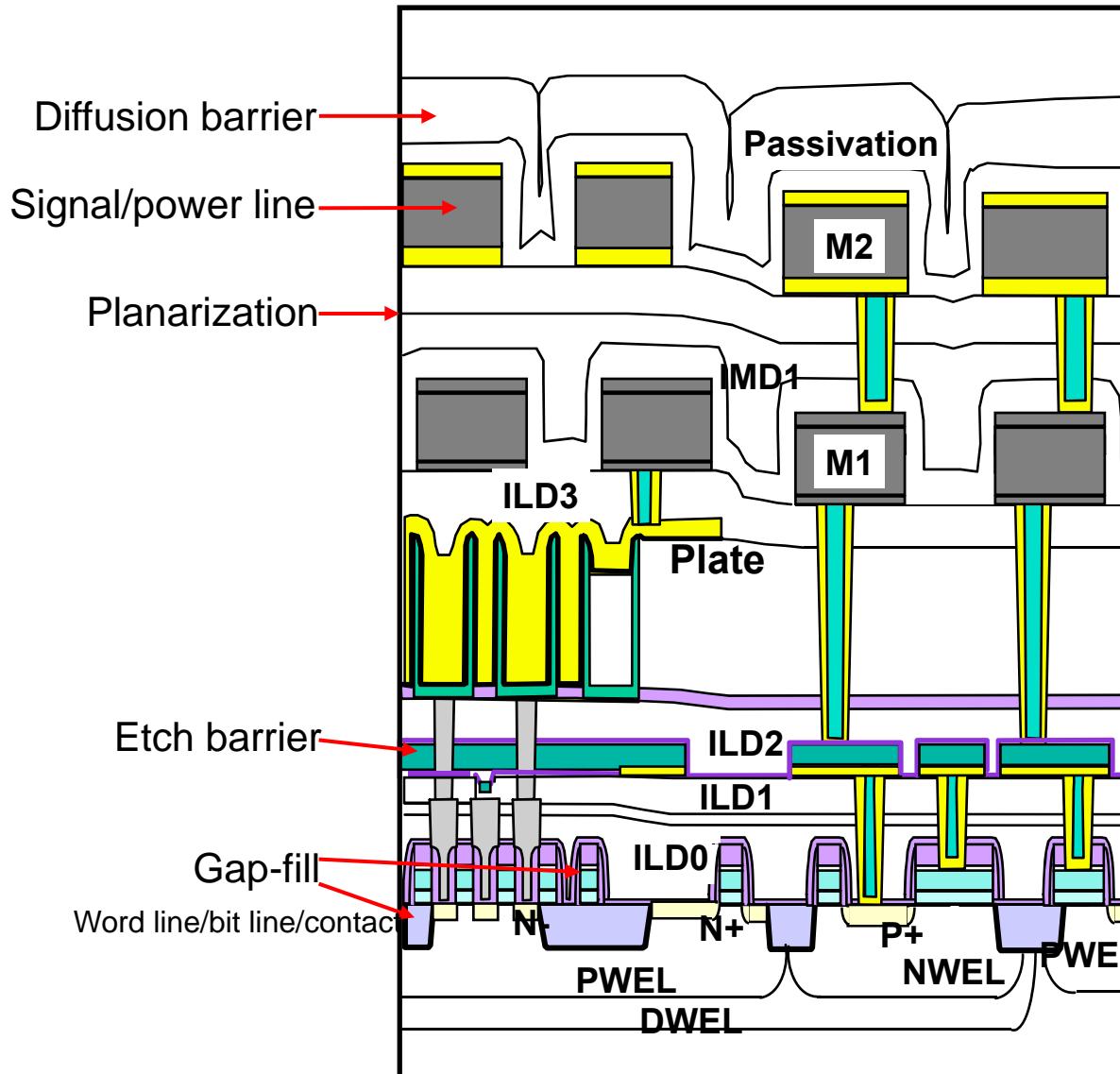
전하 저장 능력이 큰 물질들이 소자로서 개발된다.

유전물질, 양극, 음극으로 구성된다.

계량 척도는 정전용량(Capacitance)이다. 따라서 정전용량을 키우는 것이 Capacitor의 Key Issue이다.



반도체 Process – *Thin Film*



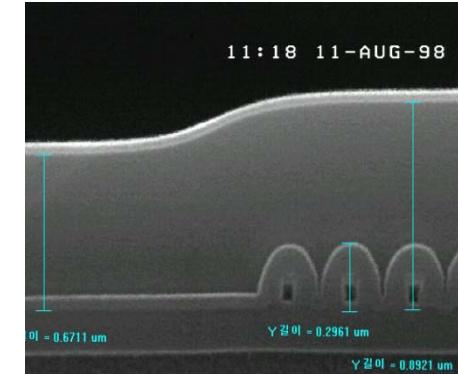
■ 배선물질의 요구 사항:

- 낮은 비저항
- 공정이 쉬워야 함.
- 패턴 형성이 쉬워야 함.
(smooth surface, high etch byproducts vapor pressure)
- 산화 분위기에서 안정
(not oxidize, stable oxide)
- 기계적으로 안정
(good adhesion, low stress)
- cleaning chemical과 반응하지 않아야
(HCl, NH₄OH, H₂O₂, HF)
- Device로의 오염원으로 작용하지 않아야 함.
- 높은 신뢰성 (resistant to high current density and high stress)
- 높은 열 안정성 (for gate, bit line)

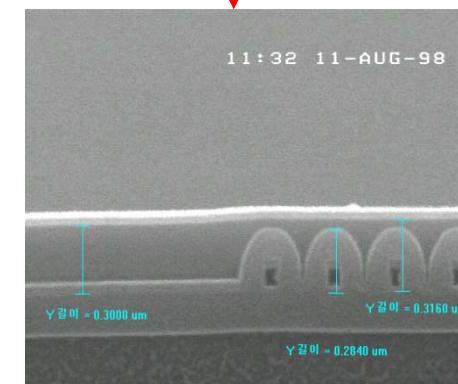
반도체 Process – CMP



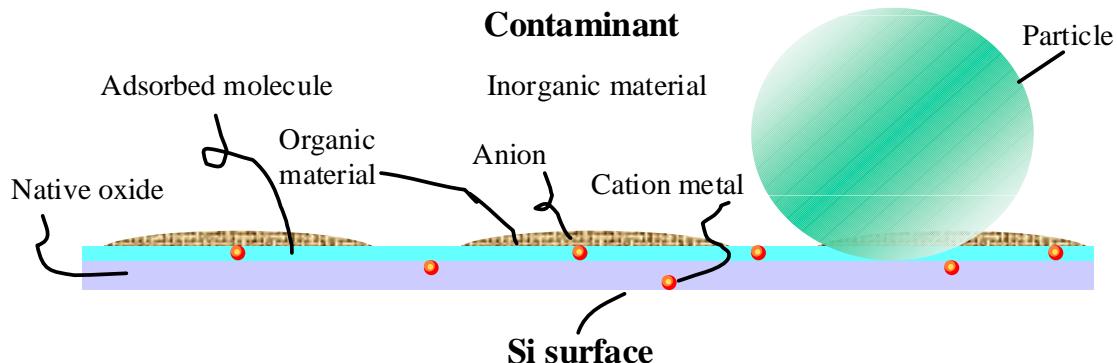
1. Shallow Trench Isolation CMP
2. Inter Level Dielectric CMP
3. Inter Metal Dielectric CMP
4. Plug poly CMP
5. Plug isolation (Modified SAC)
6. W plug/via formation
7. Al or Cu Damascene
8. X-tal silicon polishing (SOI)
9. Noble Metal (Pt/Ru/Ir/IrO₂/TiAl N/RTN/RTO 등)
10. Damascene Gate

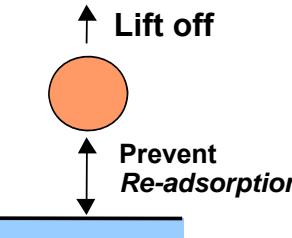


Planarization

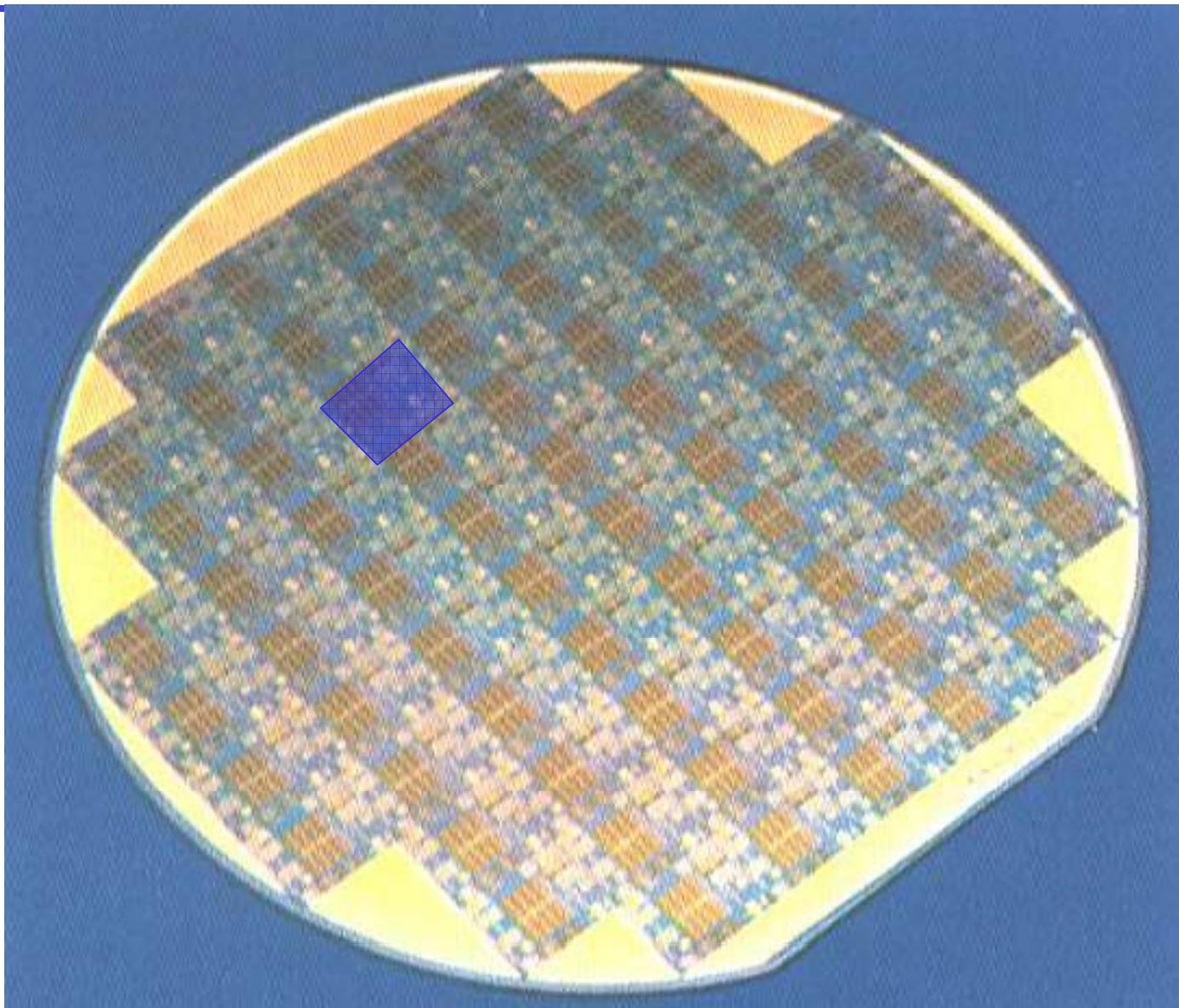


반도체 Process – Cleaning

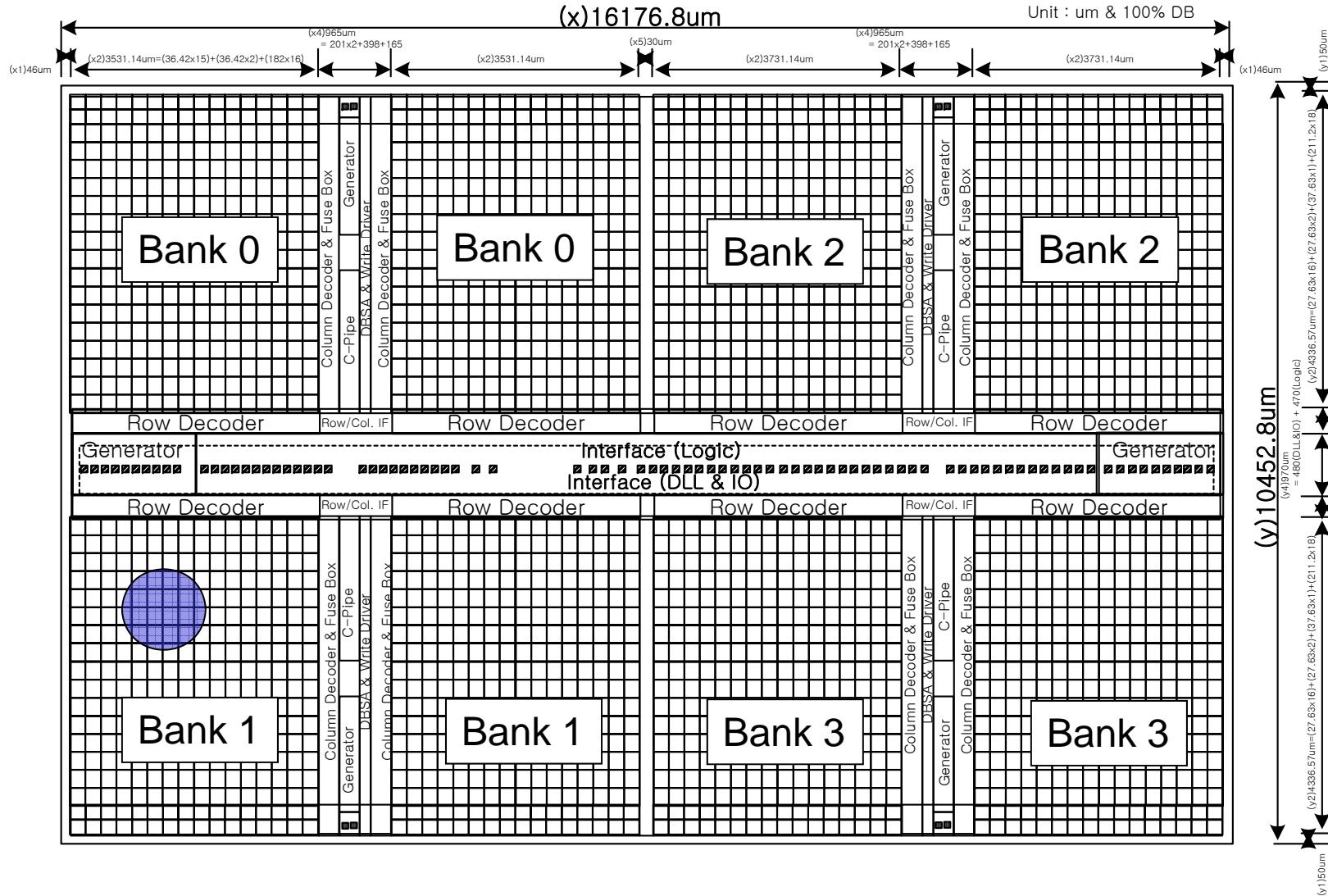


Particles: 	Lift-off Slight etch or Megasonic vibration	SC-1 ($\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O} = 1/4/20$ at 80°C) cleaning . $\text{Si} + 2\text{H}_2\text{O}_2 = \text{SiO}_2 + \text{H}_2\text{O}$ (on <i>Si surface</i>) . $\text{SiO}_2 + 2\text{NH}_4\text{OH} = (\text{NH}_4)_2\text{SiO}_3 + \text{H}_2\text{O}$
	Prevent re-adhesion Same polarity of zeta potential between particle and substrate	. Alkaline solutions like SC-1 or . Surfactant containing acidic solutions
Metals: Cleaning solution should take electrons away from adhering metals and dissolve them into solution as positive ions.		SC-2 ($\text{HCl}/\text{H}_2\text{O}_2/\text{H}_2\text{O} = 1/1/6$ at 85°C) cleaning M^0 (metallic state) in UPW $\text{M}^0 \rightarrow \text{M}^+ + e^-$ (ionic state in SC-2) cf: CLN_B, CLN_R, HF/ H_2O_2 , HNO_3 , HNO_3/HF , O_3 -UPW and etc
Organic impurities: Cleaning using high redox potential value to decompose them to smaller molecules such as CO_2 , H_2O and etc.		SPM ($\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2 = 3/1 \sim 4/1$ at $90^\circ\text{C} \sim 130^\circ\text{C}$) cleaning $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2 = \text{H}_2\text{SO}_5 + \text{H}_2\text{O}$ $\text{H}_2\text{SO}_5 + \text{Carbon compound} = \text{CO}_2 + \text{H}_2\text{SO}_4 + \text{H}_2\text{O}$ cf: O_3 -UPW and etc

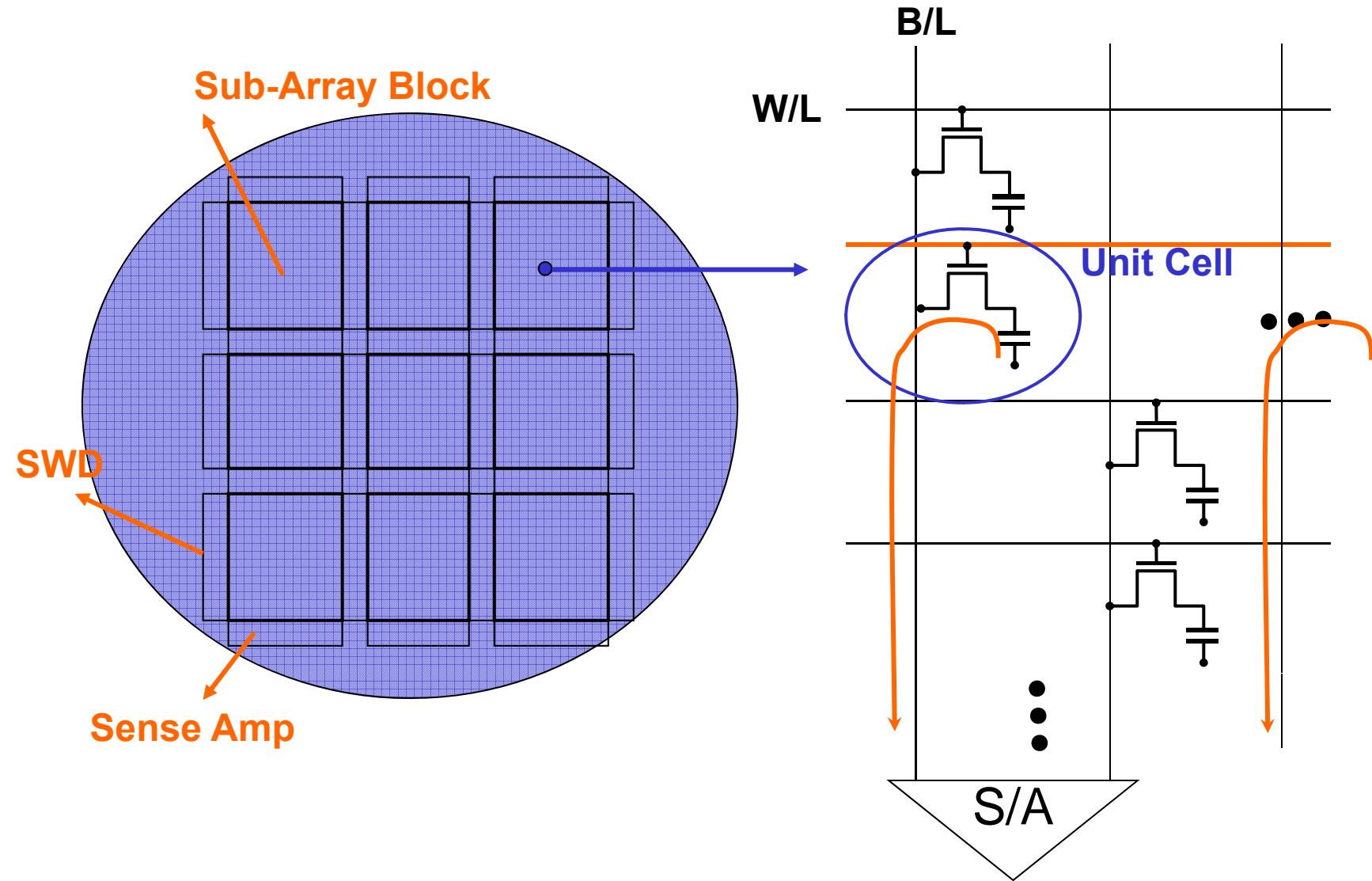
반도체 Introduction : Chip Architecture I



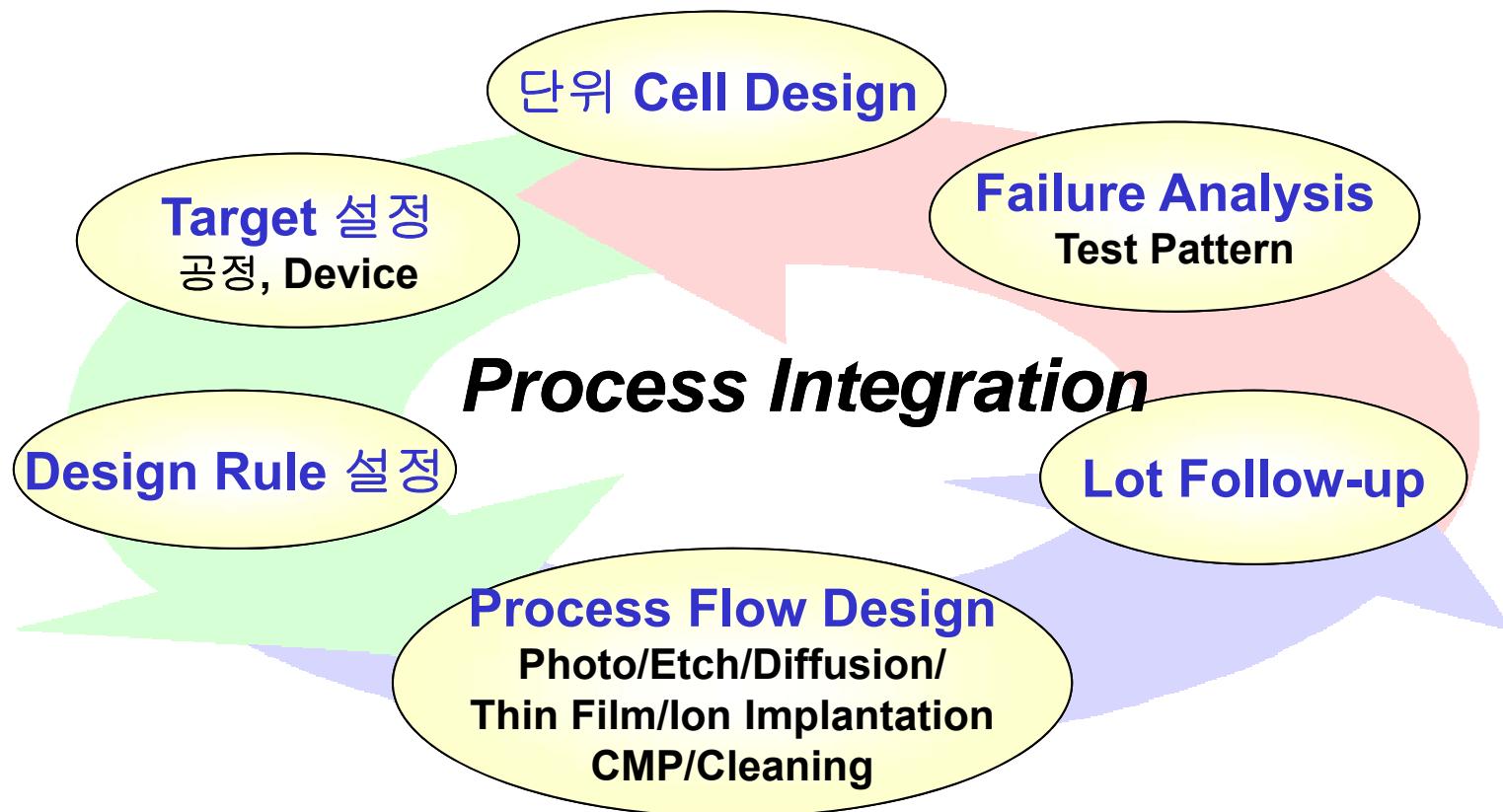
반도체 Introduction : Chip Architecture I



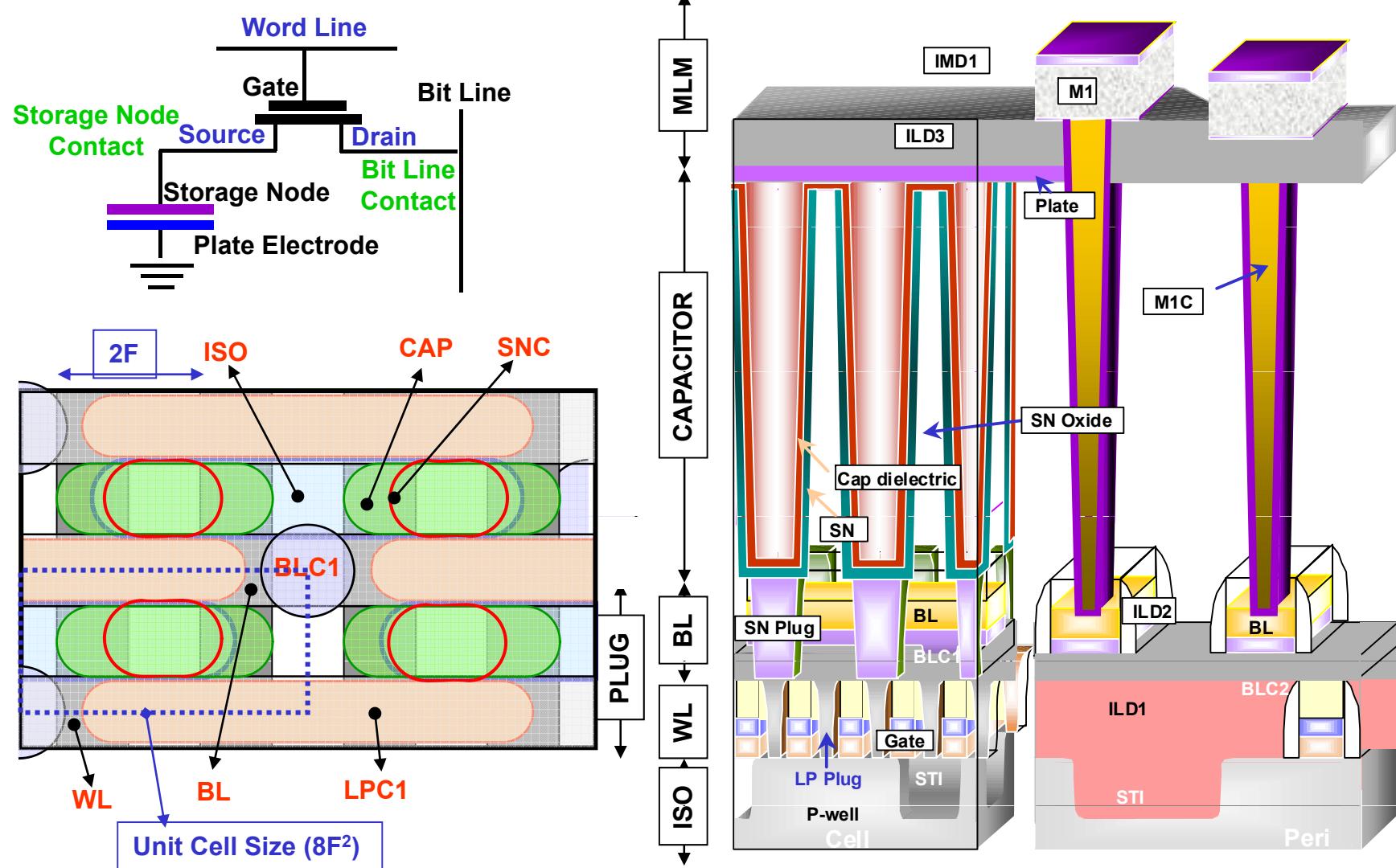
반도체 Introduction : Chip Architecture II



Process Integration



DRAM Integration Process Flow [Overview]

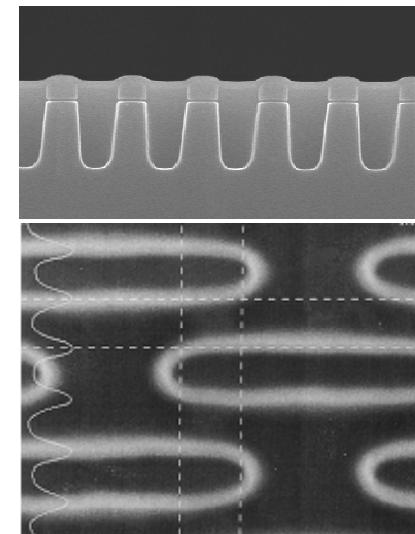
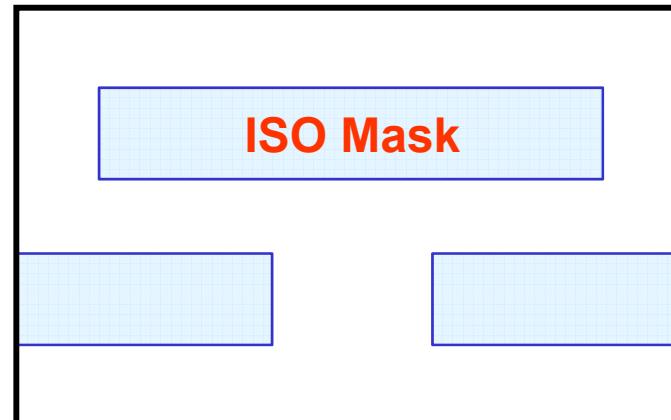
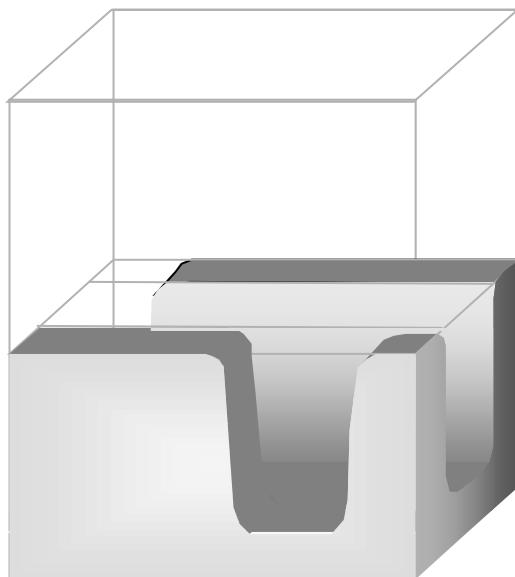


DRAM Integration Process Flow [Isolation]

- 목적 : Active와 Active를 분리시키기 위함.
- Isolation 종류
 - Conventional LOCOS (Local Oxidation of Silicon)
 - PBL (Poly Buffered LOCOS)
 - STI (Shallow Trench Isolation)

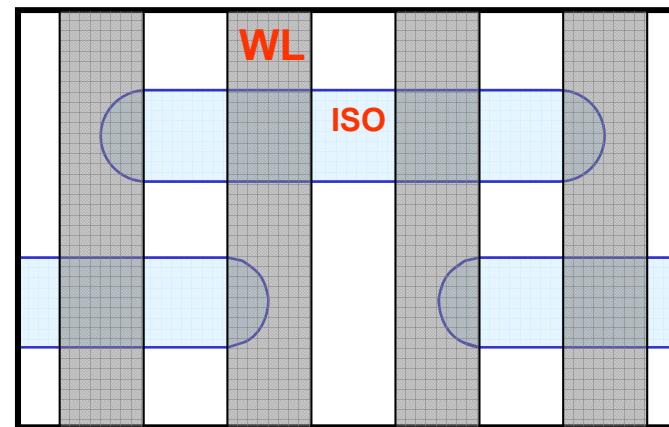
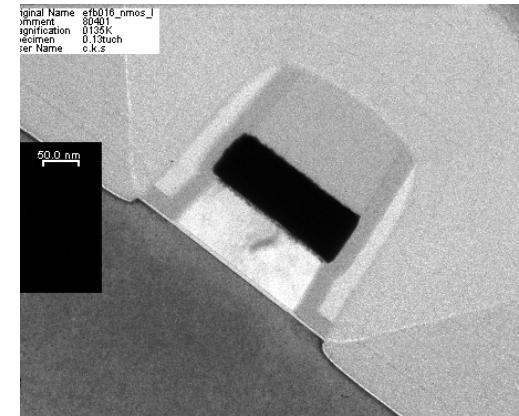
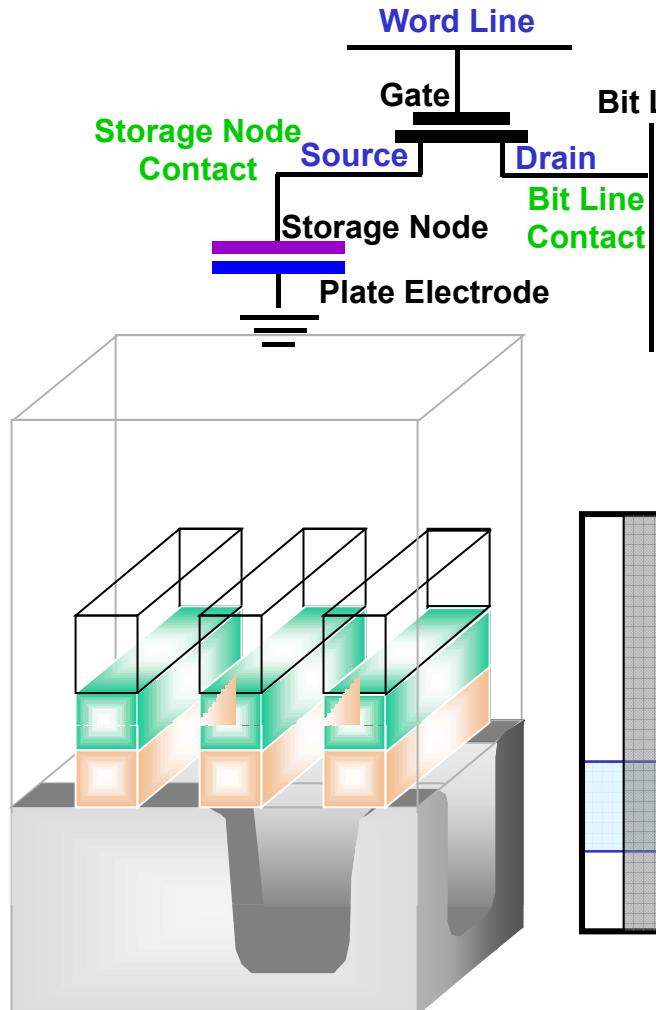
공정순서

- Pad Ox.
- Pad Nit DEP
- ISO Mask(1)
- ISO Etch
- ISO PR strip & PET
- Wall Ox.
- ISO HDP DEP
- STI CMP
- ISO Nit Strip
- Well Formation



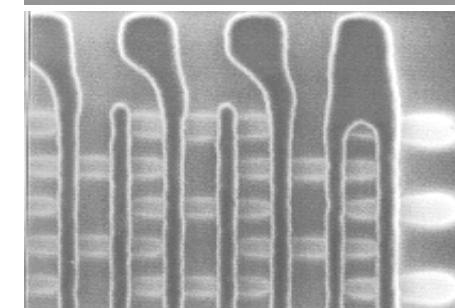
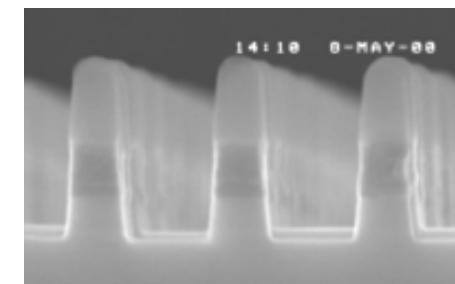
DRAM Integration Process Flow [Word Line]

- 목적 : Transistor 전극인 Gate 형성



공정순서

- Gate Oxidation
- Gate Poly DEP
- Gate Metal DEP
- Gate HM DEP
- Gate Mask
- Gate Etch
- LDD Formation
- Gate Spacer DEP

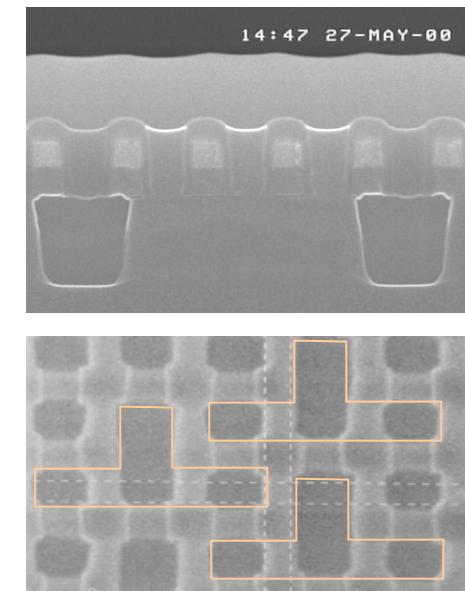
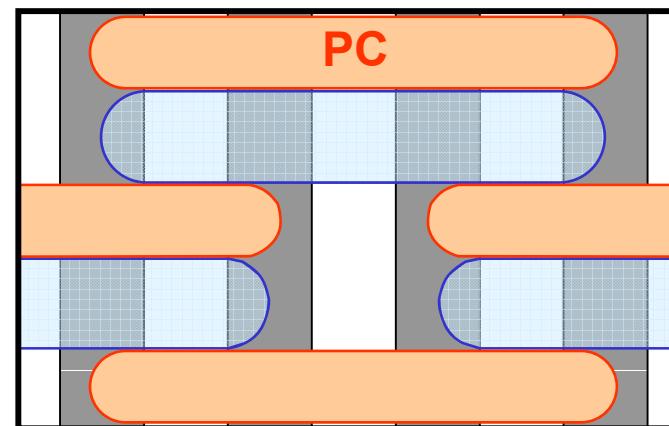
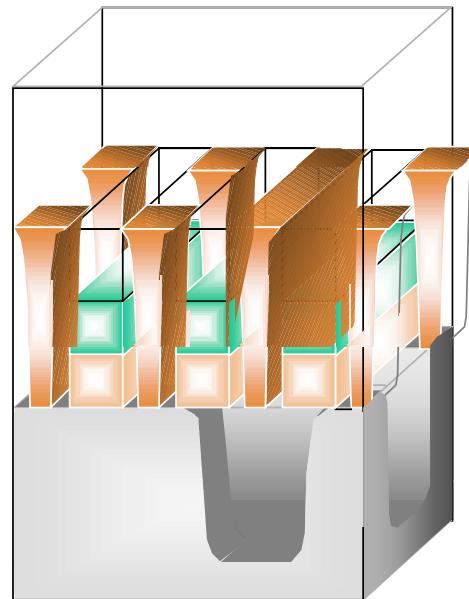


DRAM Integration Process Flow [Contact]

- 목적 : Cell Transistor의 S/D junction과 Bit Line 및 Storage Node Contact과 연결시켜 주기 위한 중간 공정.
- Self-Aligned Contact 사용

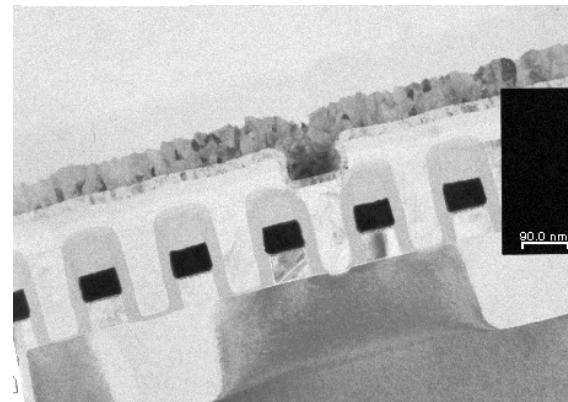
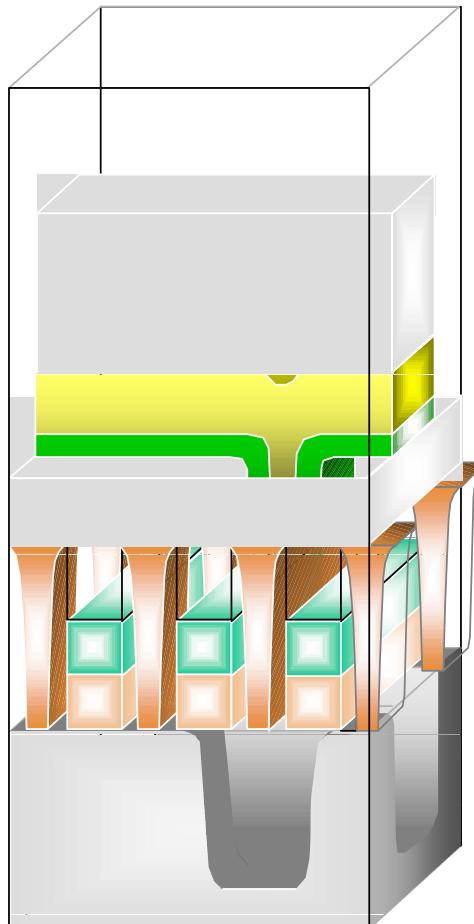
공정순서

- ILD DEP
- Gate Spacer etch
- Spacer SiN Dep
- ILD Dep
- ILD CMP
- LPC Mask
- LPC etch/PRST
- Poly Dep
- Poly CMP



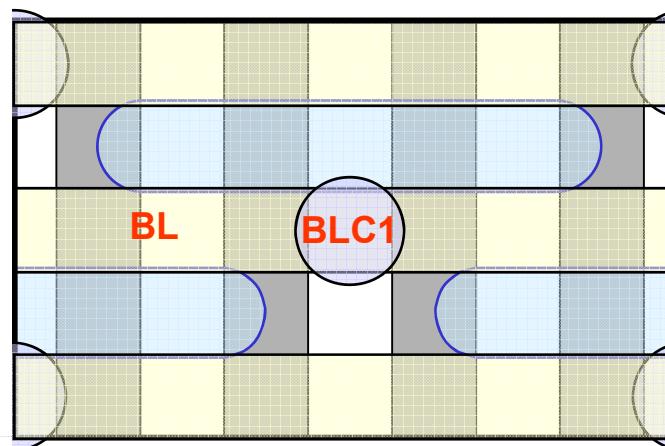
DRAM Integration Process Flow [Bit Line]

- 목적 : Transistor의 drain 영역과 외부 회로와의 Current path 형성을 위한 Bit line 공정



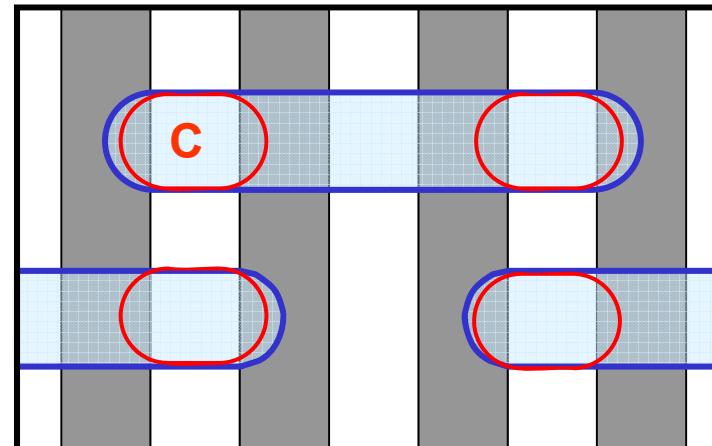
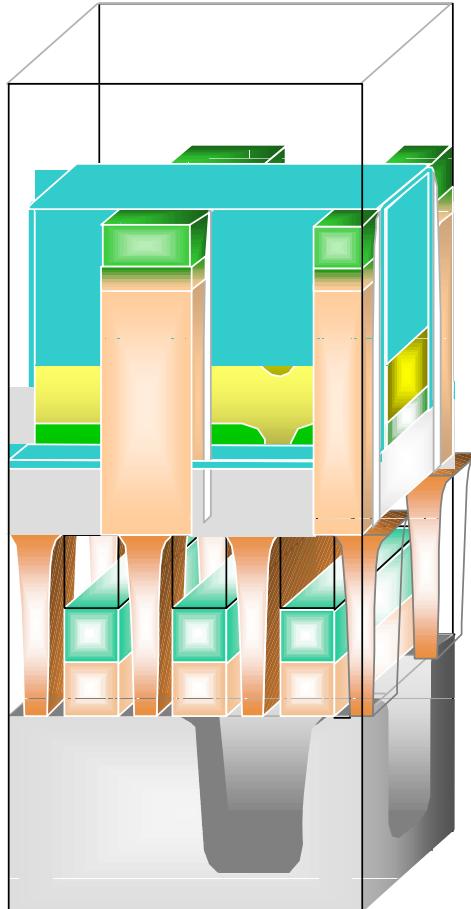
공정순서

- ILD DEP
- BLC Mask
- BLC etch
- BLC Mask
- BLC etch
- BL DEP
- BL HM DEP
- BL Mask
- BL Etch



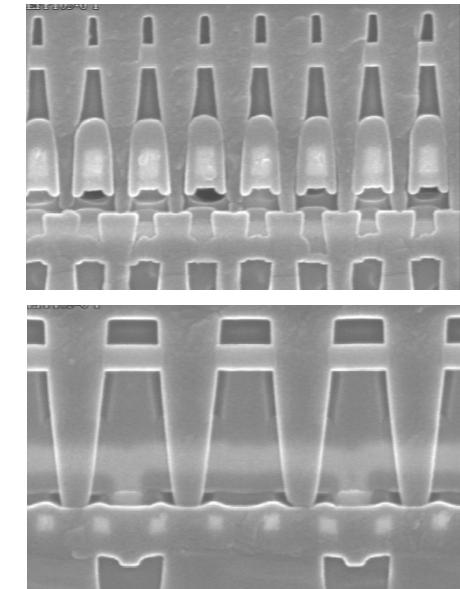
DRAM Integration Process Flow [Node Contact]

• 목적 : LPC1과 Storage node
를 연결시켜 주는
contact 형성 공정

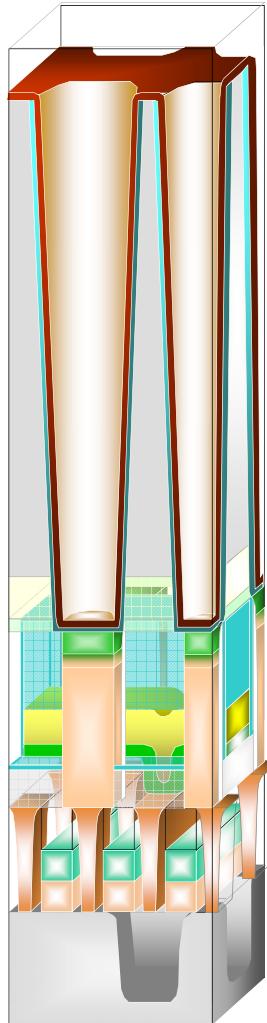


공정순서

- ILD HDP DEP
- ILD CMP
- C Mask
- C etch
- C Poly DEP
- C Poly EB (or CMP)

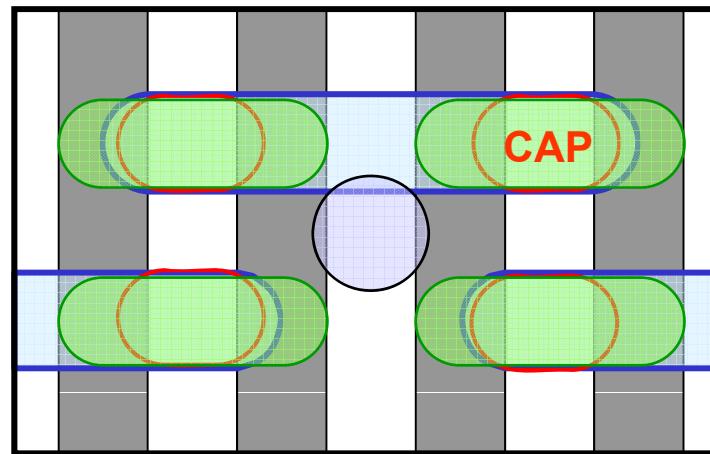


DRAM Integration Process Flow [Capacitor]

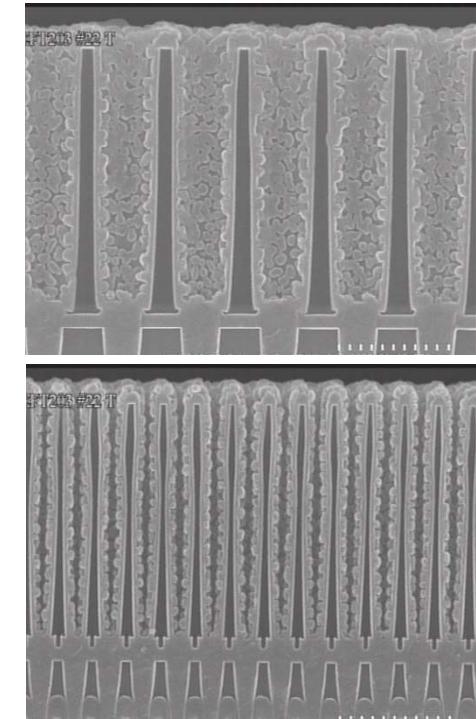


공정순서

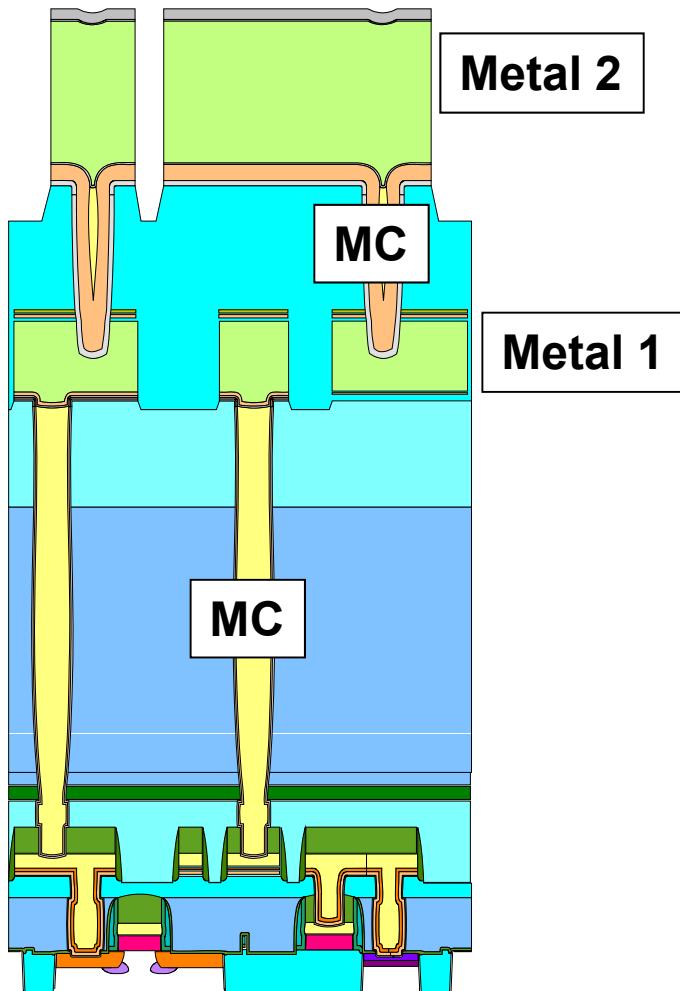
- Storage node oxide DEP
- CAP Mask
- SN oxide etch
- SN DEP
- SN PR coating
- SN EB (or CMP)
- SN PR Strip
- Capacitor dielectric film DEP
- Plate DEP
- Plate Mask
- Plate Etch



• 목적 : 정보 저장 역할을 하는 **cell capacitor**를 형성하는 공정.



DRAM Integration Process Flow [MLM]

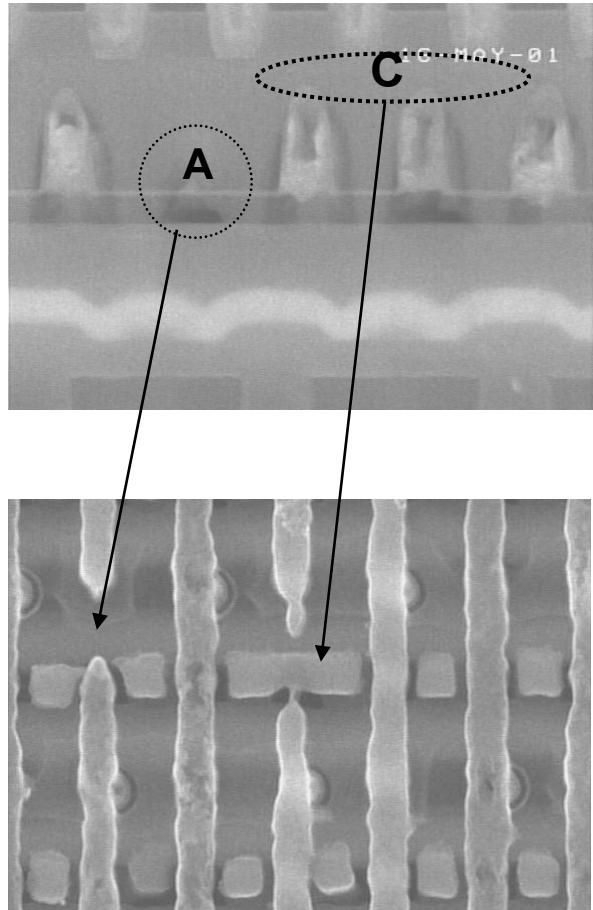


• 목적 : **Power** 공급 및 소자 상호 배선,
외부와의 연결에 사용되는 **metal Line** 형성 공정.

공정순서

- ILD DEP
- ILD CMP
- MC Mask
- MC etch
- MC DEP
- MC Etch back
(or W Plug CMP)
- M DEP
- M Mask
- M Etch
- IMD DEP
- IMD CMP
- MC Mask
- MC etch
- MC DEP
- MC Etch back
- M AI DEP
- M Mask
- M etch
- Passivation
- PAD Mask
- Repair-etch
- Anneal

Failure Analysis (F/A) -1



* **Broken SEM 및 Dimple Grinding**
방법 사용
* **BL line이 끊어지거나(A), BL의**
과다 Etch로 인해 BL-LP2(SNC)
간 Bridge 발생.(C)

Failure Analysis (F/A) -2

MC BL-BL Short (column fail / DC fail 분석)

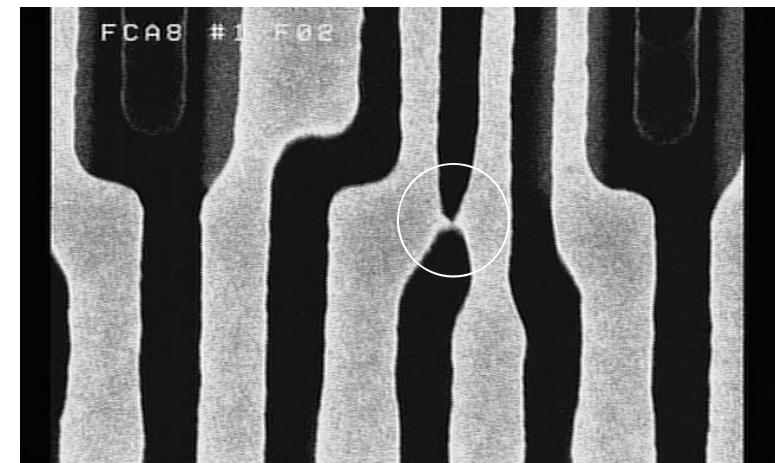
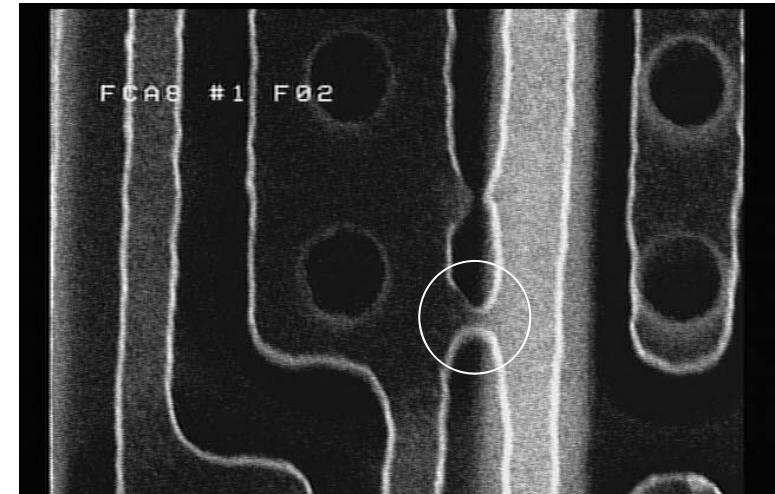
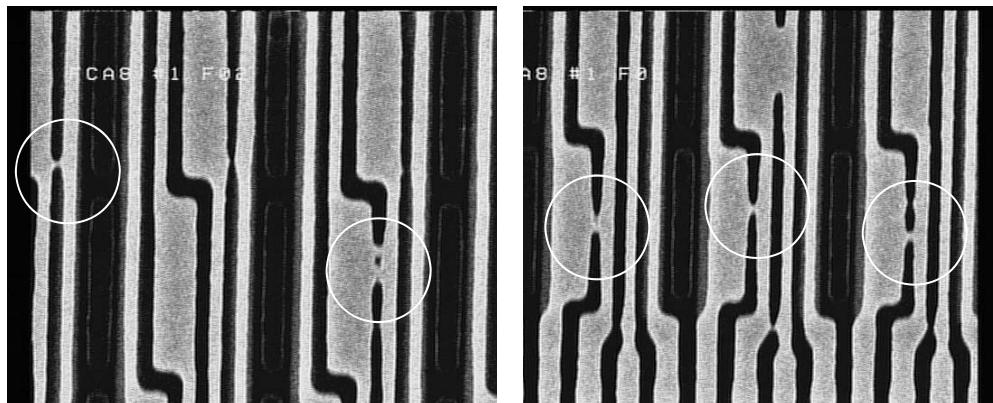
방법

Dimple Grinding / Wet Decoration

- Decoration : Hot H₂O₂ 30sec : W제거
1:4 HF 2Min. : Oxide 제거
- Dimple 정도에 따라 W이 남은 지역 존재

결과

Bit Line to Bit Line Short Monitoring - Sub WL Driver



결론

Word Line Selection시 Circuit 동작 Fail

∴ Vss , Vpp, Vdd Vbb 간 Short 유발

Bit Line CD Target Review 필요 , CD Inspection Point 재 추가 필요