

Enseignes et afficheurs à LED

Circuits logiques programmables : FPGA



Dr. Mamadou Lamine NDIAYE

Circuits logiques programmables : FPGA



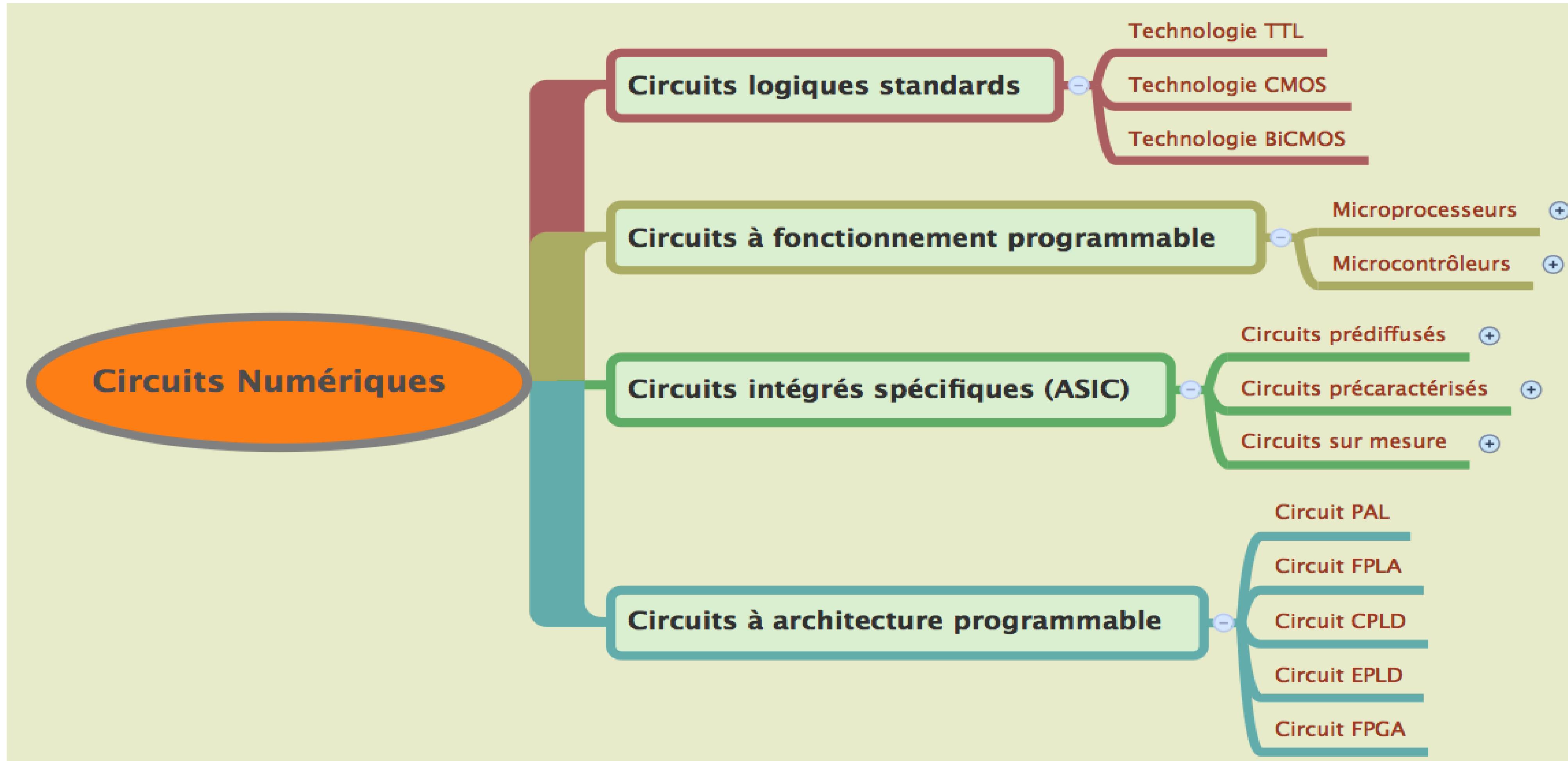
Mamadou Lamine NDIAYE

Circuits logiques programmables



- Les circuits logiques programmables
- Les circuits FPGA
- Méthodologie de conception des circuits FPGA
- Environnement de développement

Classification des circuits logiques

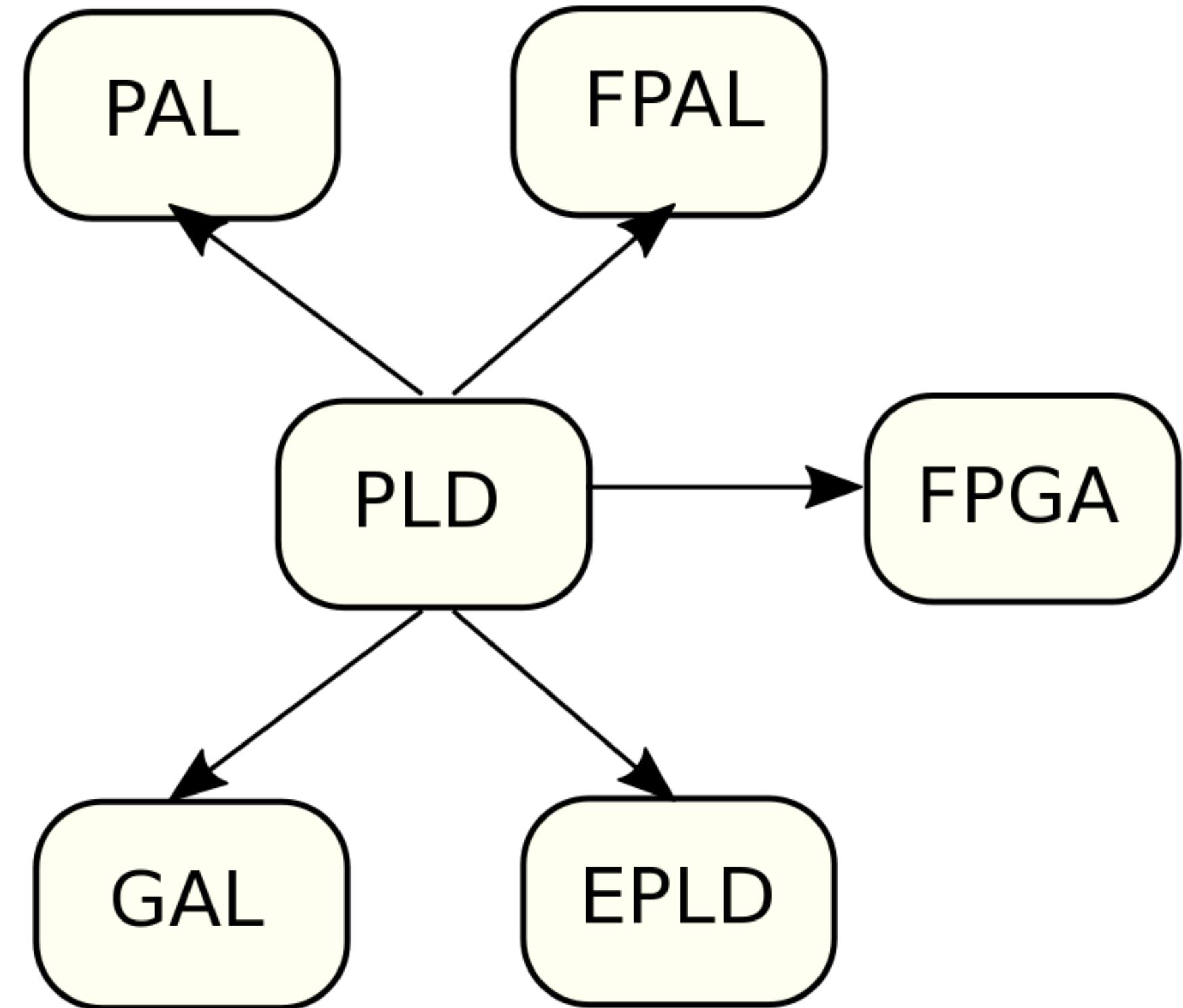


Circuits logiques programmables



Ensemble de portes logiques reconfigurables

- ET, OU
- Bascules, RAM, Multiplexeurs, registres

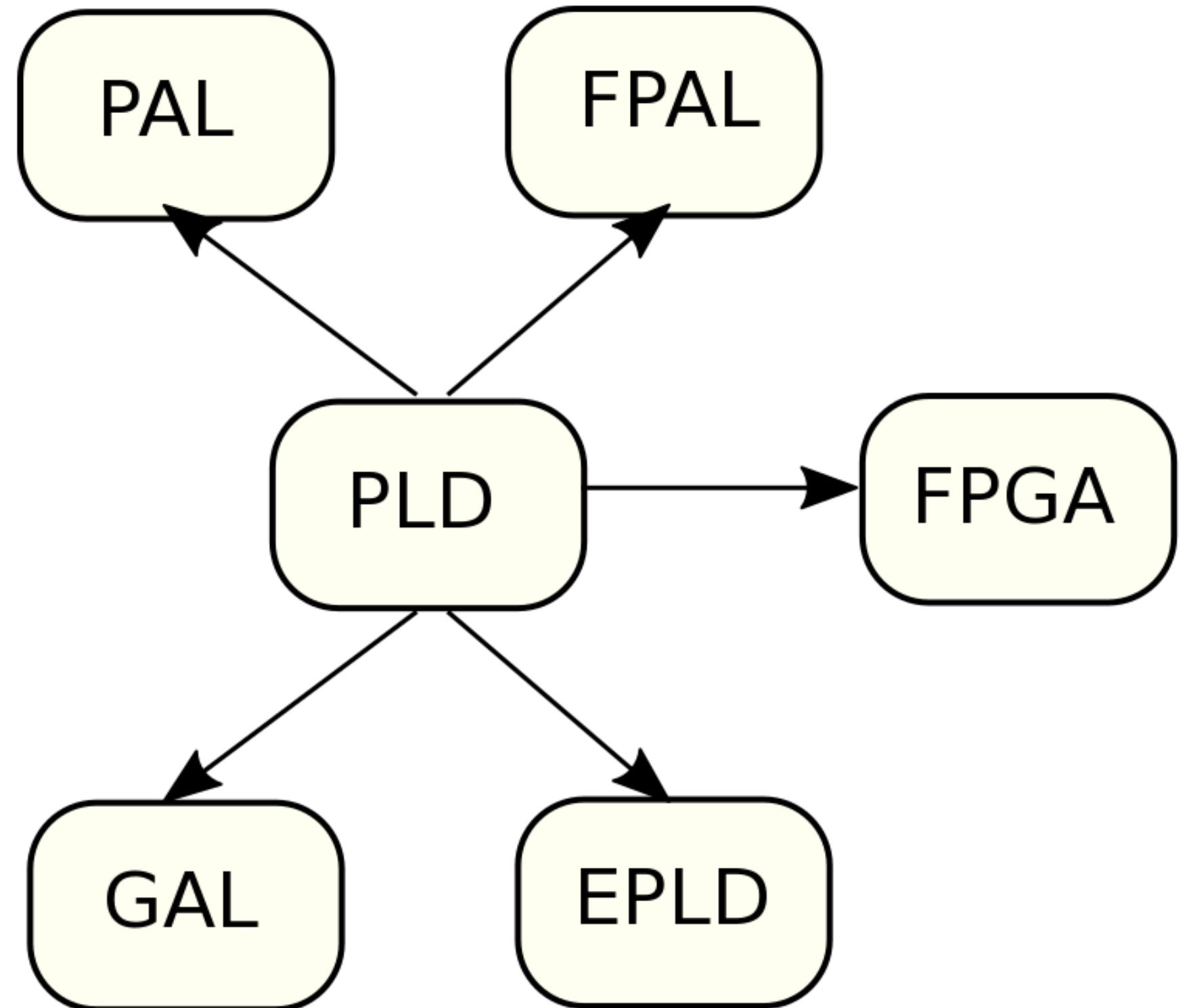


Circuits logiques programmables



Ensemble de portes logiques reconfigurables

- ET, OU
- Bascules, RAM, Multiplexeurs, registres
- Technologies fusible,
- Technologies Flash, EEPROM, SRAM



Circuits logiques programmables



- Circuit PAL (Programmable Array Logic) où seules les fonctions ET sont programmables
- Circuit PLA (Field Programmable Logic Array) est un circuit PAL dans lequel les fonctions ET et OU sont programmables
- Circuit CPLD (Complex Programmable Logic Device) est un circuit logique programmable complexe
- Circuit EPLD (Erasable Programmable Logic Device) est un circuit logique programmable et effaçable
- Circuit FPGA (Field Programmable Gate Array) est un réseau de circuits programmables à la demande

Les circuits FPGA



Les circuits FPGA



● Les circuits logiques programmables de type FPGA sont de plus en plus utilisés dans la conception des circuits numériques.

- Matrices de fonctions logiques (cellules logiques SRAM)
- Programmation des interconnexions (reconfiguration de l'architecture) in situ
- Reprogrammables à volonté
- Temps de développement très court.
- Grande souplesse pour des évolutions rapides à moindre coût

Les circuits FPGA



● Les circuits logiques programmables de type FPGA sont de plus en plus utilisés dans la conception des circuits numériques.

- Densités d'intégration pouvant atteindre plus de 10 millions de portes logiques.
- Possibilités de traitement parallèle des données (augmentation de la vitesse de calcul).
- Blocs logiques configurables constitués d'arbres de multiplexeurs connectés à des points mémoires.
- Capacité limitée par le nombre de blocs logiques configurables (non la complexité).

Méthodologie de conception des FPGA (CPLD)



Niveaux de description

● Comportemental ou fonctionnel

- Le modèle est décrit par, sa fonction, son algorithme. Il s'agit de décrire comment cela fonctionne.

● RTL (Register Transfert Logic)

- Le modèle est décrit sous forme d'éléments séquentiels
- Prend en compte la notion d'horloge, de cycle;

● Structurel (Porte logique)

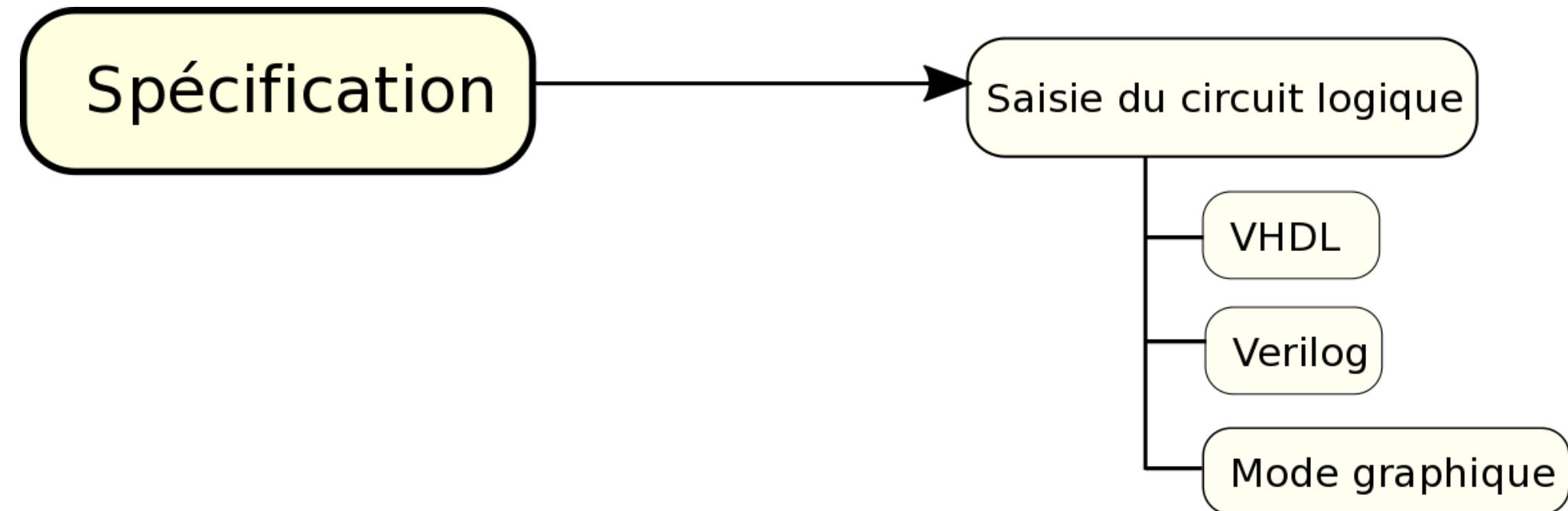
- Le modèle est décrit par sa topologie (netlist) de portes logiques, de registres, de composants

● Décomposition du cahier des charges en fonctions simples

- Fonctions combinatoires (**instructions concurrentes**)
- Fonctions séquentielles (**process**)

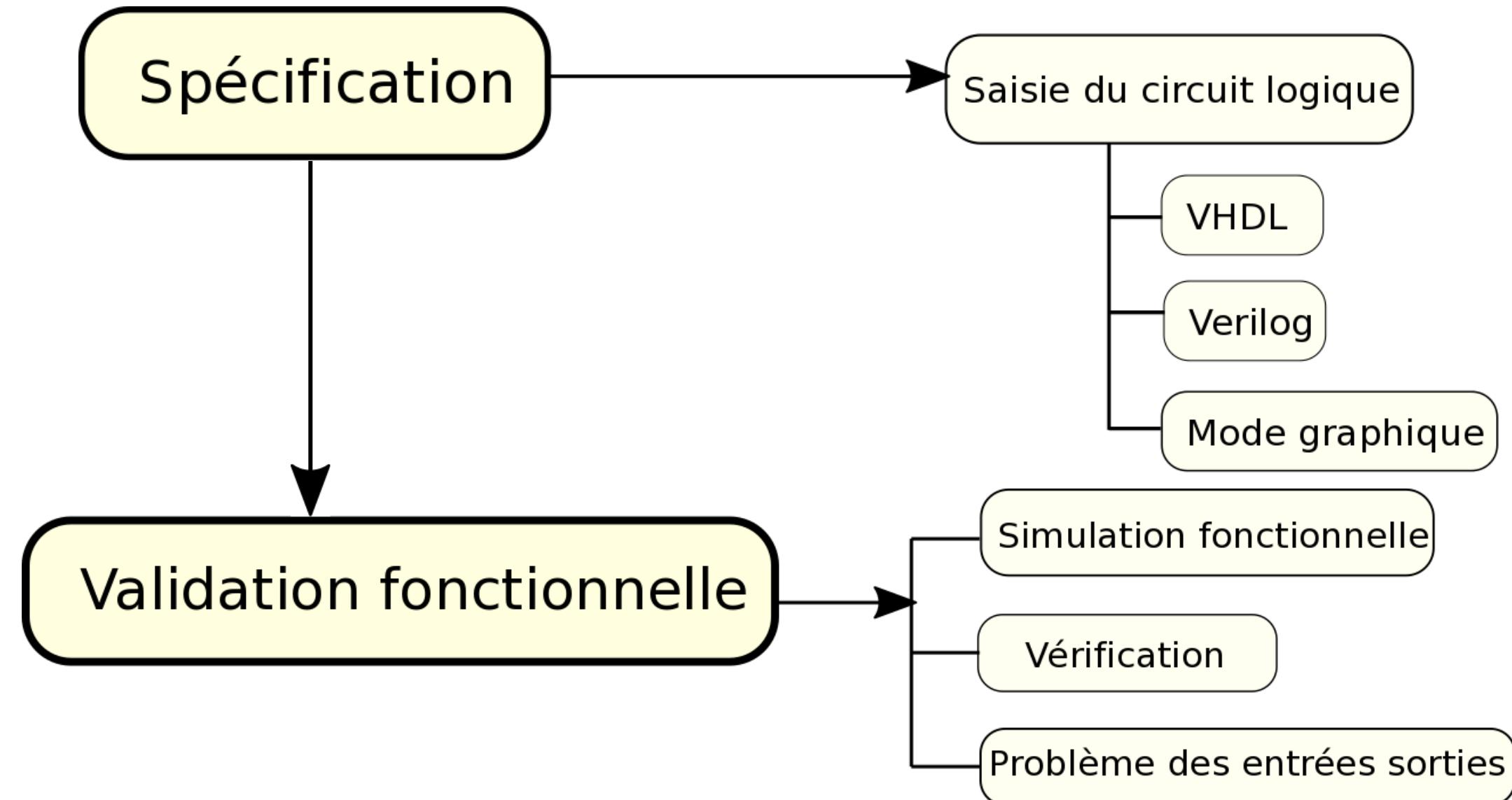


Méthodologie de conception des FPGA (CPLD)

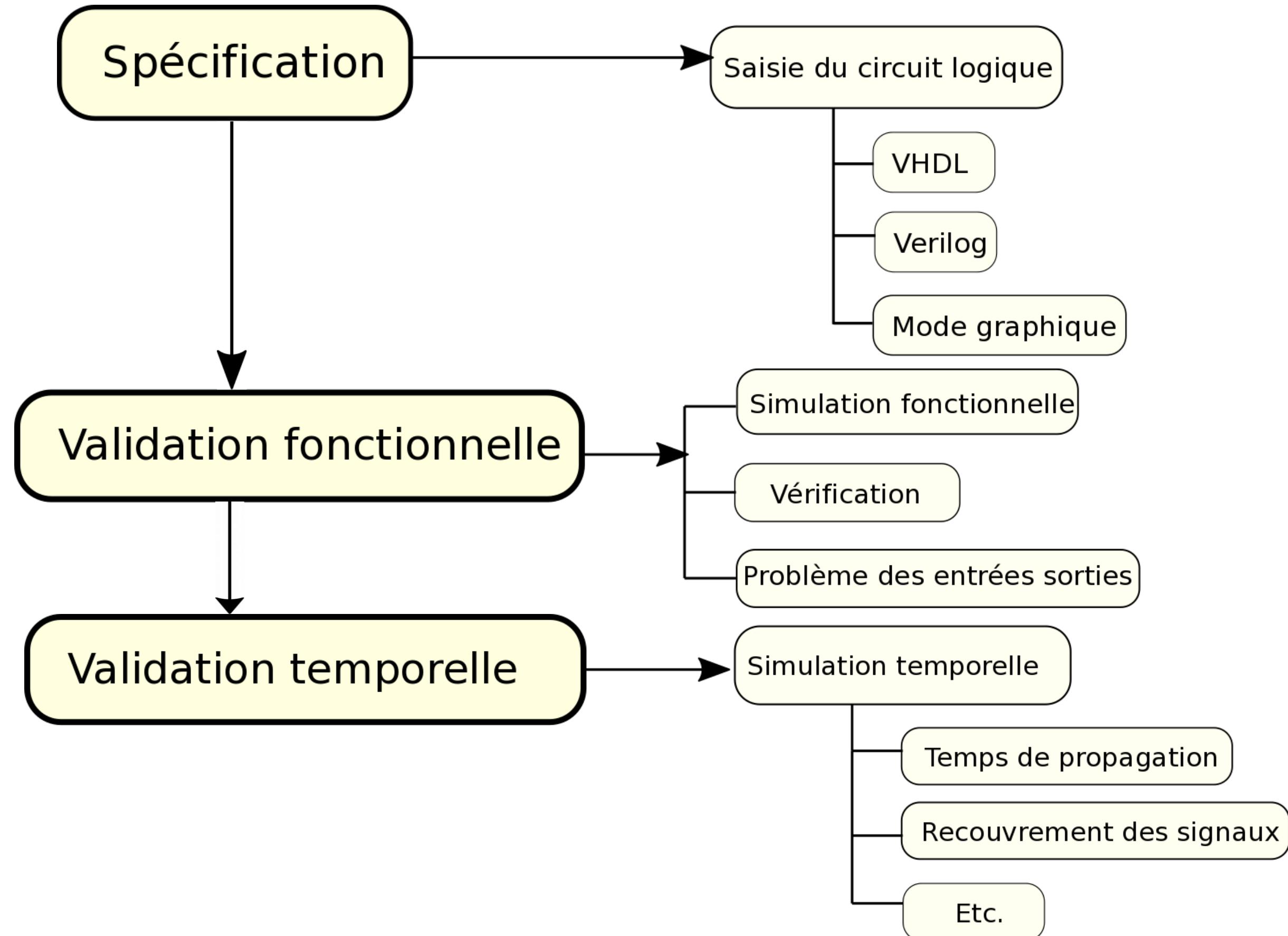




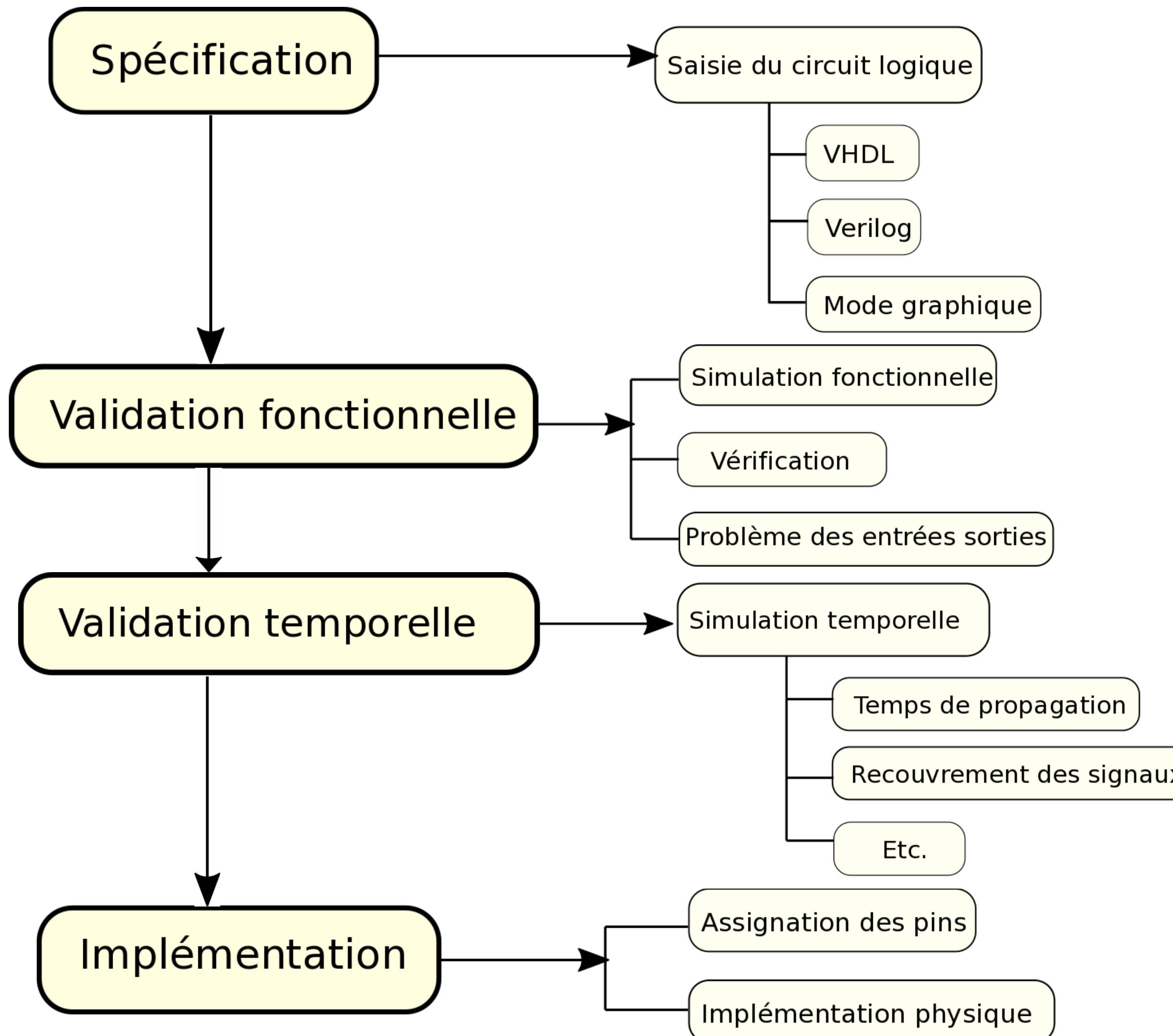
Méthodologie de conception des FPGA (CPLD)



Méthodologie de conception des FPGA (CPLD)



Méthodologie de conception des FPGA (CPLD)



Environnement de développement



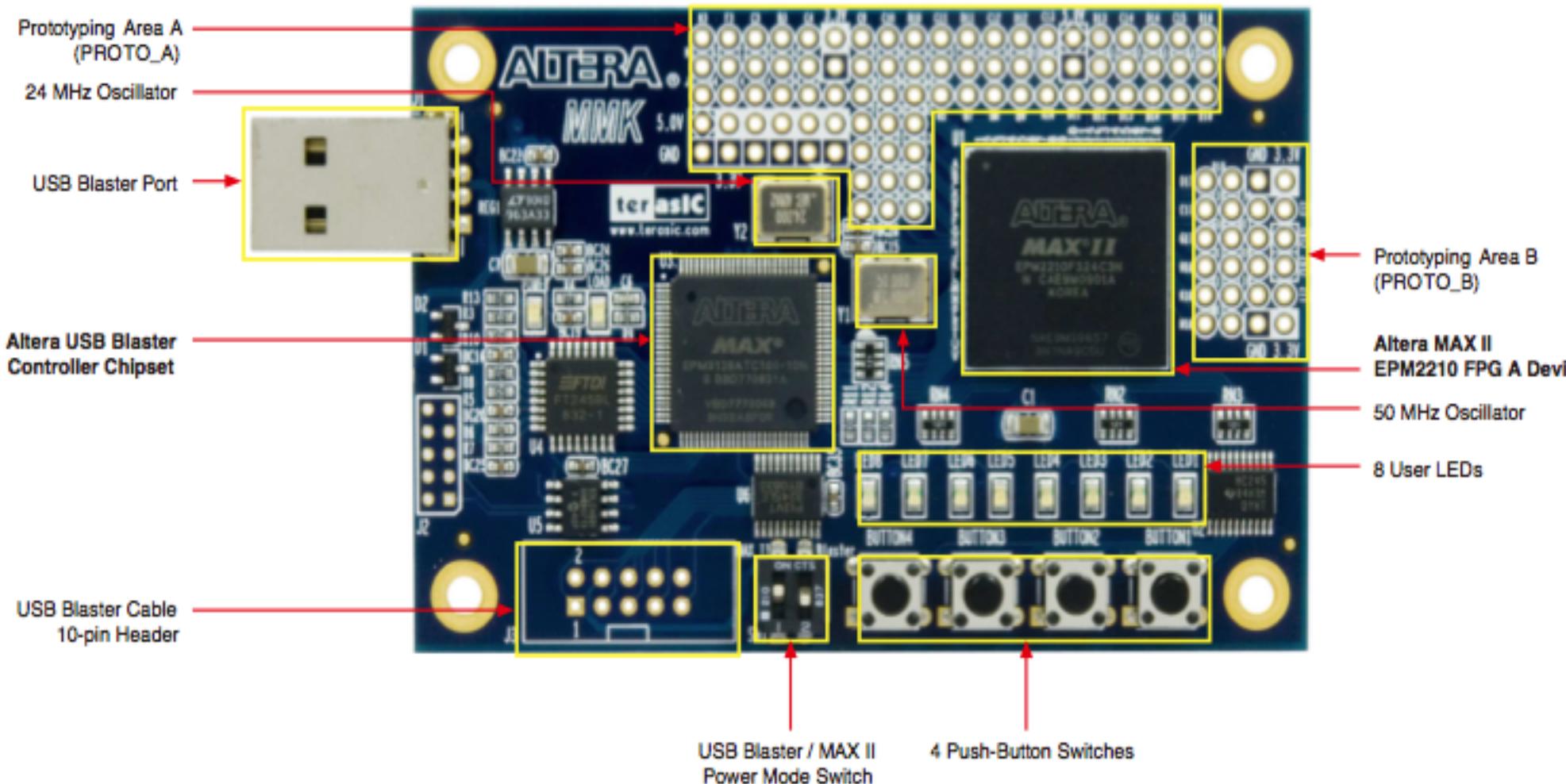
● Synthèse avec les deux principaux plateformes de développement

- Altera Quartus II
- Xilinx ISE

● Simulation.

- ModelSim

CARTE DEO (NANO) (ALTERA)



Specifications FPGA

- Altera MAX II EPM2210F324 FPGA device

I/O Devices

- Built-in USB Blaster for FPGA configuration

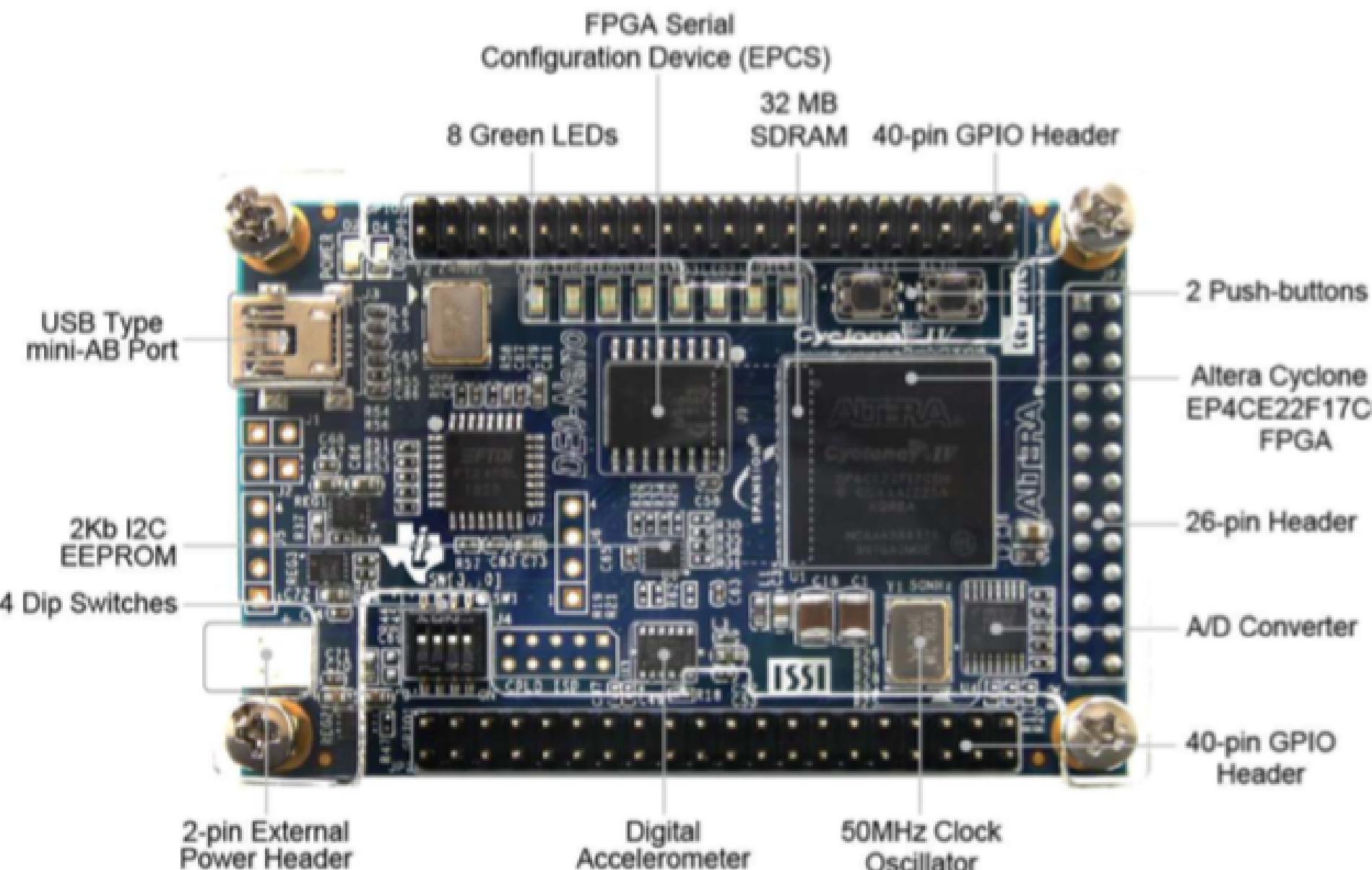
Switches, LEDs, and Clocks

- 1 DIP switch
- 4 pushbutton switches
- 2 red user LEDs,
- 2 yellow user LEDs,
- 2 blue user LEDs,
- 2 green user LEDs
- 50-MHz oscillator for clock sources
- Powered by USB

Prototyping Areas

- A 40-pin expansion port area compatible with Altera DE2/DE1 expansion ports.
- Prototyping Area A with **68 GPIO**, **6 3.3V**, **2 5V** and **8 GND** pins
- Prototyping Area B with **20 GPIO**, **2 3.3V**, and **2 GND** pins

CARTE DEO (NANO) (ALTERA)



Specifications FPGA

- Altera CYCLONE IV EP4CE22F17C6N FPGA device
 - 256 pins, 47 cellules

I/O Devices

- Built-in USB Blaster for FPGA configuration

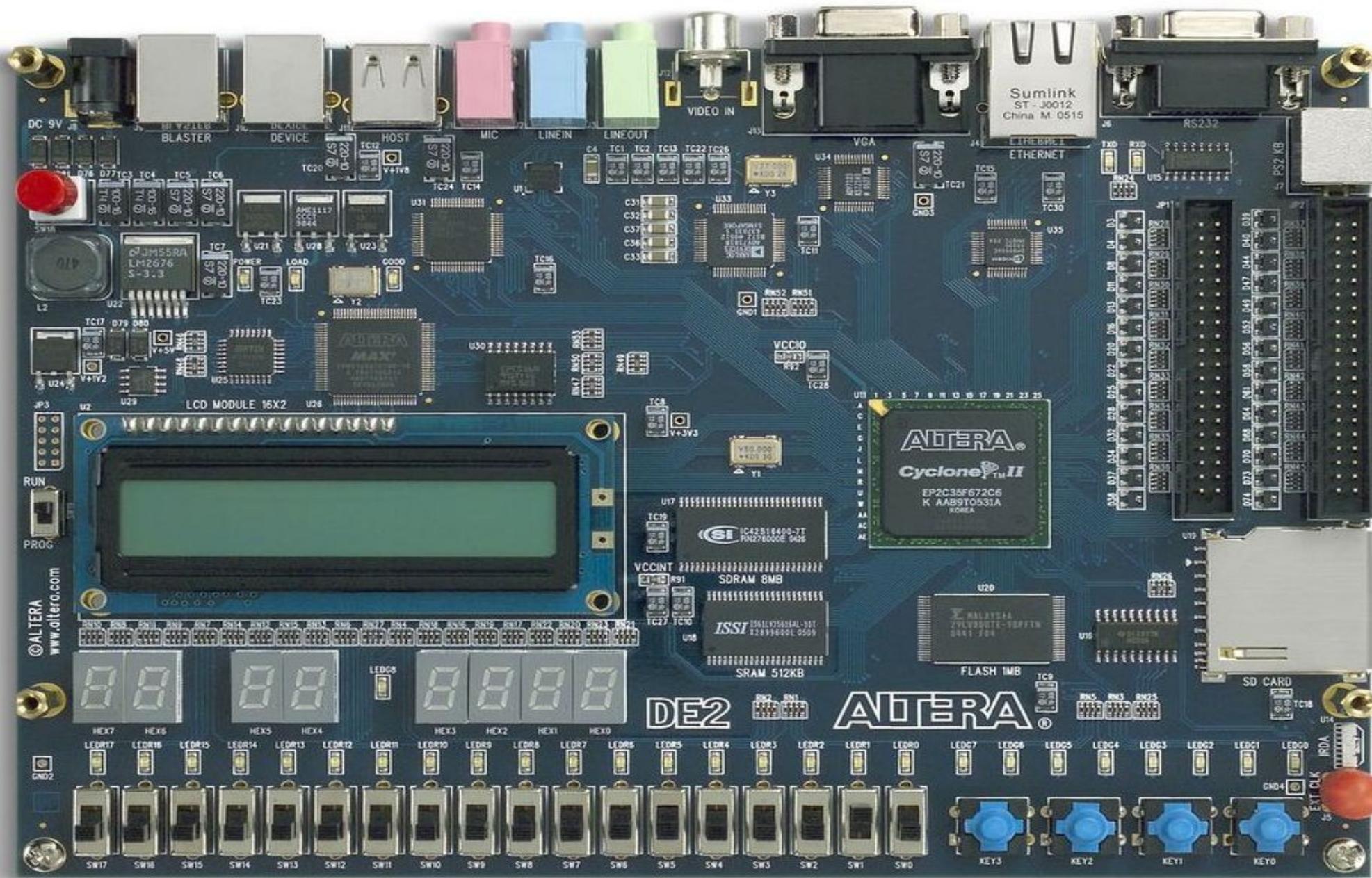
Switches, LEDs, Displays, and Clocks

- 4 DIP switch
- 2 pushbutton switches
- 2 red user LEDs,
- 2 yellow user LEDs,
- 2 blue user LEDs,
- 2 green user LEDs
- 50-MHz oscillator for clock sources
- Powered by USB
- A/D Converter, 8 channel – 12 bit A/D Converter

Prototyping Areas

- Two 40-pin Headers GPIO compatible provide 72 I/O pin, 5V Power pin, Two 3,3V and four ground pins .
- 32MB SDRAM, 2Kb I2C EEPROM

CARTE DE2 (ALTERA)



Specifications FPGA

- Cyclone II EP2C35F672C6 FPGA
- 672 pins, 4276 cellules

I/O Devices

- Built-in USB Blaster for FPGA configuration
- 10/100 Ethernet, RS-232, Infrared port
- Video Out (VGA 10-bit DAC)
- Video In (NTSC/PAL/Multi-format)
- USB 2.0 (type A and type B)
- PS/2 mouse or keyboard port
- Line-in, Line-out, microphone-in (24-bit audio CODEC)
- Expansion headers (76 signal pins)

Memory

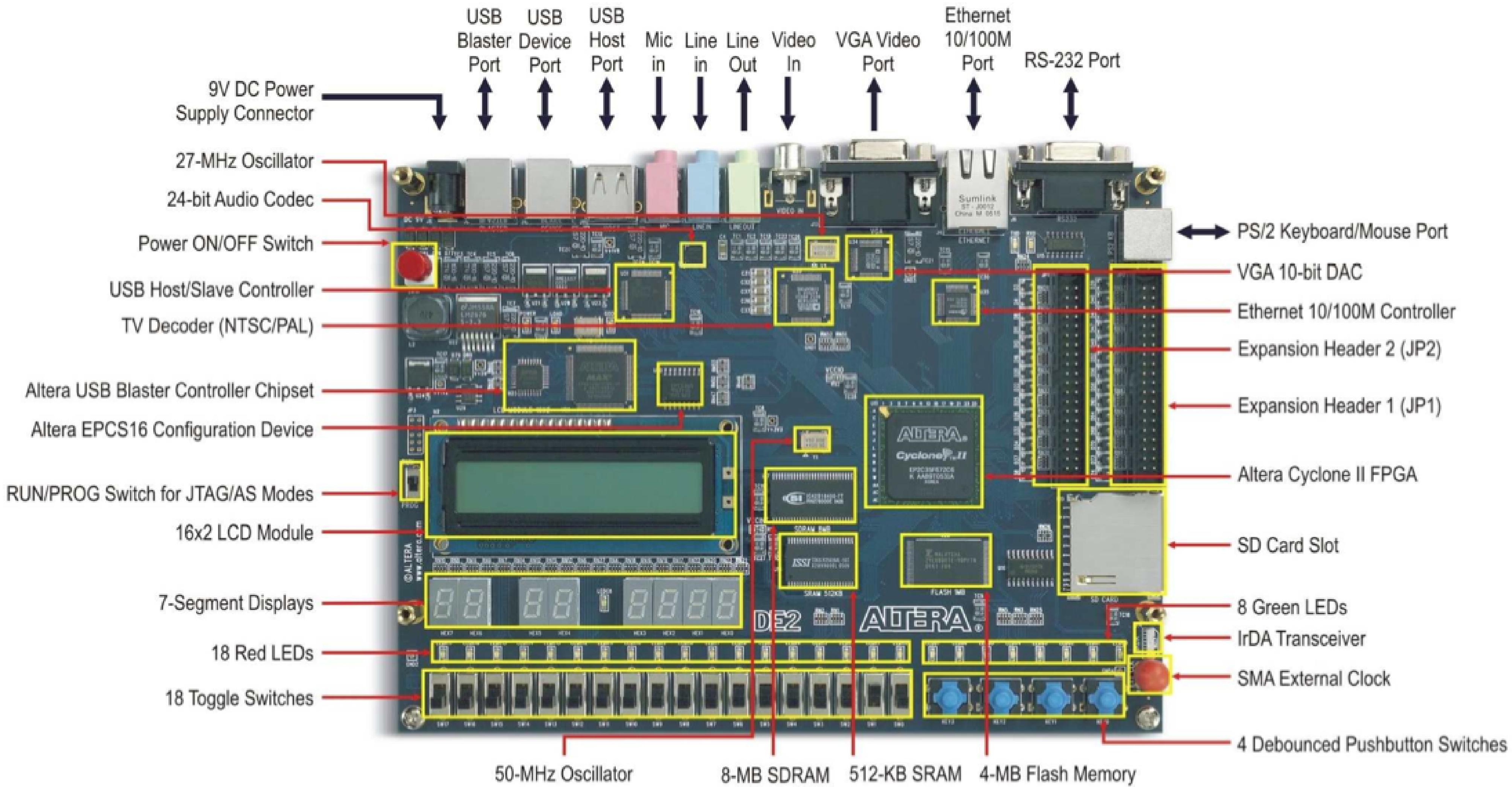
- 8-MB SDRAM, 512-KB SRAM, 4-MB Flash
- SD memory card slot

Switches, LEDs, Displays, and Clocks

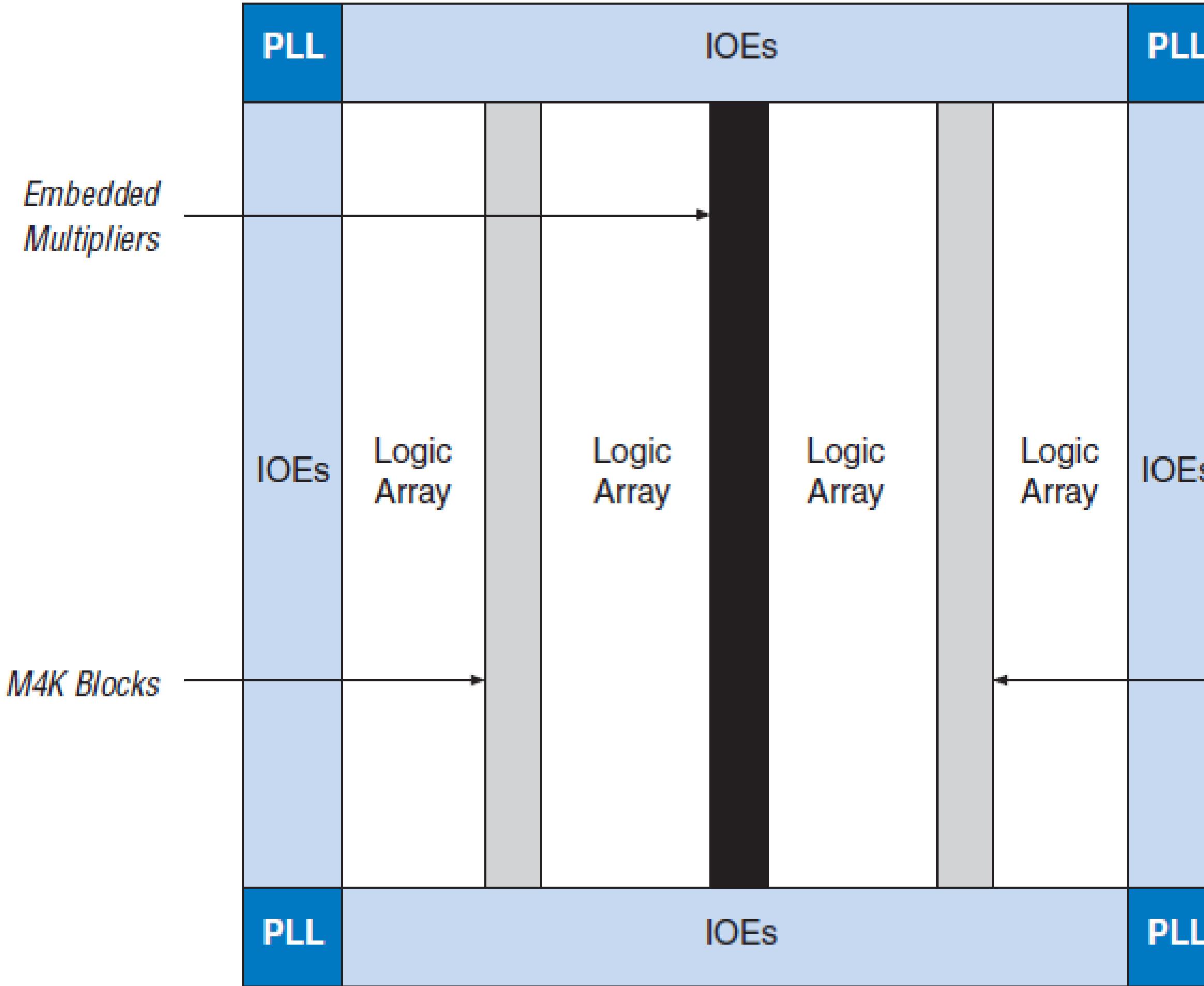
- 18 toggle switches
- 4 debounced pushbutton switches
- 18 red LEDs, 8 green LEDs
- Eight 7-segment displays
- 16 x 2 LCD display
- 27-MHz and 50-MHz oscillators, external SMA clock input



CARTE DE2 (ALTERA)

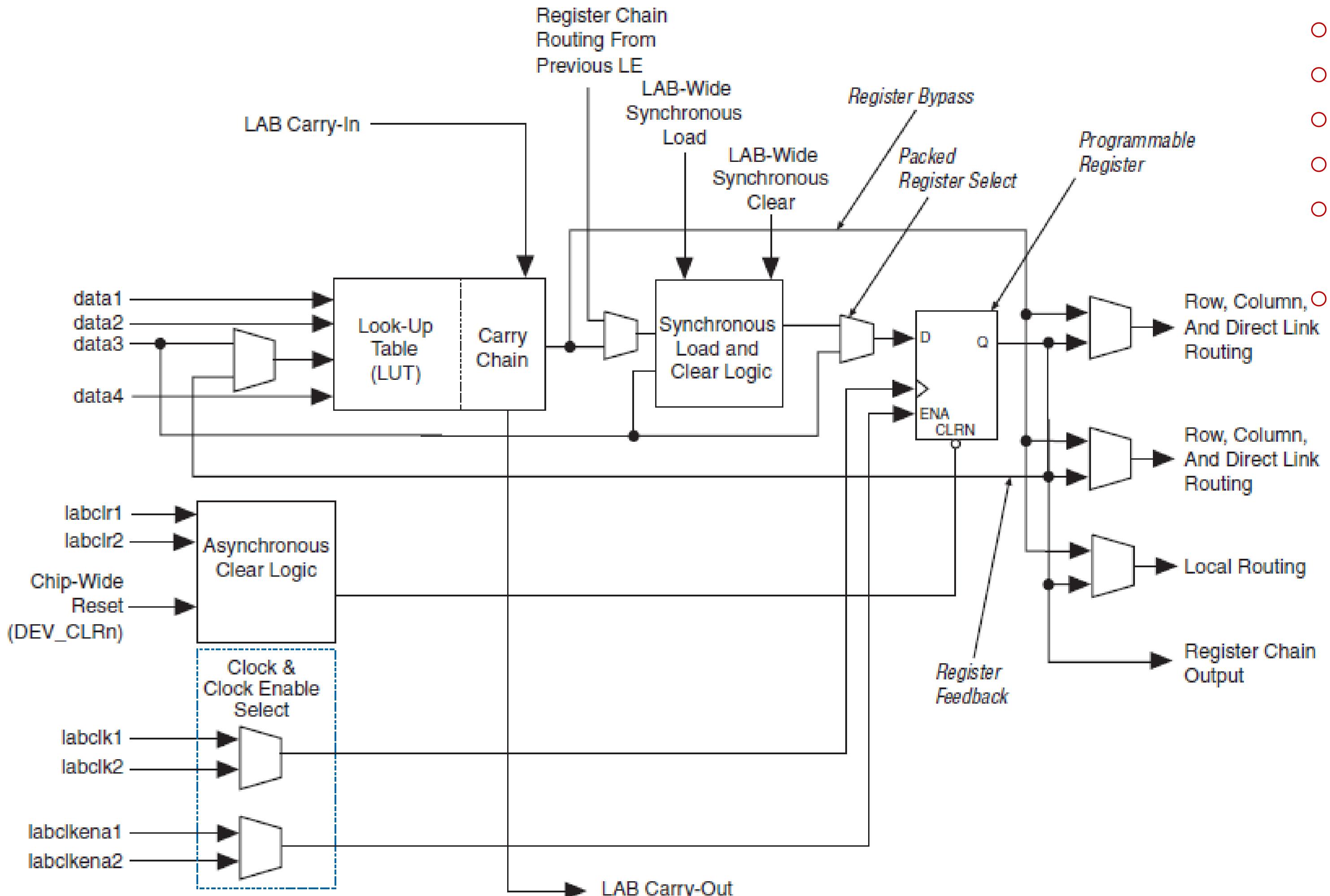


Exemple d'ALTERA : Le cyclone II



- Jusqu'à 68416 éléments logiques regroupés par blocs de 16
- Configuration rapide en moins de 100ms
- Mode de configuration série USB BLASTER ou JTAG
- <https://www.altera.com>

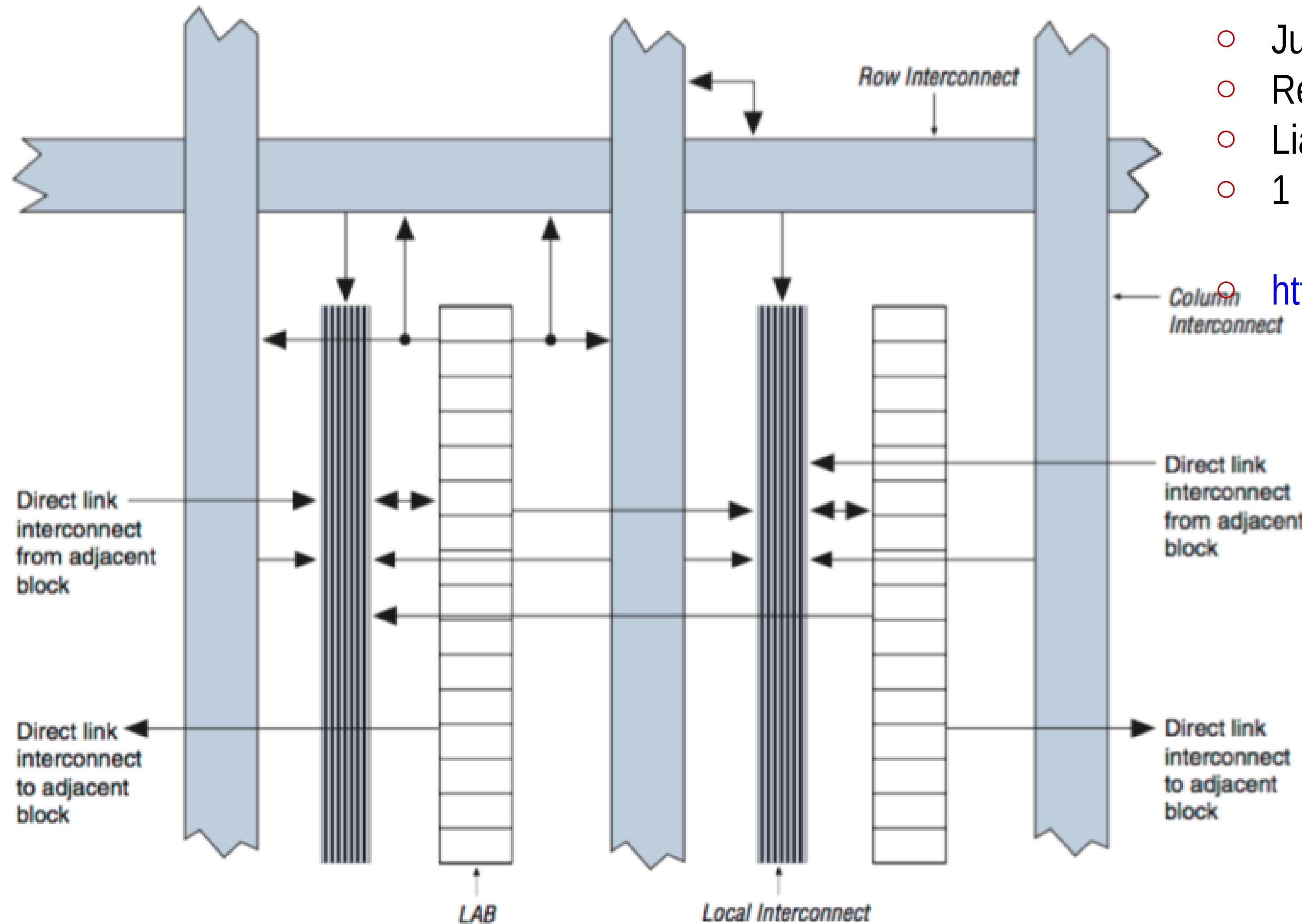
Cyclone II (architecture d'un élément logique)



- 4 entrées
- 1 registre de sortie programmable
- 1 entrée de retenue
- 1 sortie de retenue
- Interconnexion local

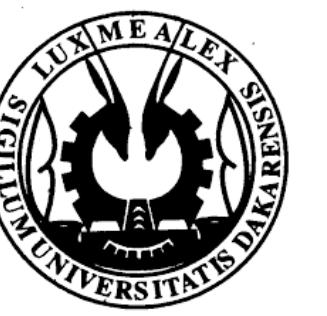
<https://www.altera.com>

Cyclone II (interconnexions des blocs logiques)



- Jusqu'à 68416 éléments logiques
- Réseau local d'interconnexion
- Liaisons directes avec BL adjacent
- 1 bloc mémoire, Ck, I/O entre BL adjacent

○ <https://www.altera.com>



Environnement de Travail

● QUARTUS II Web Edition

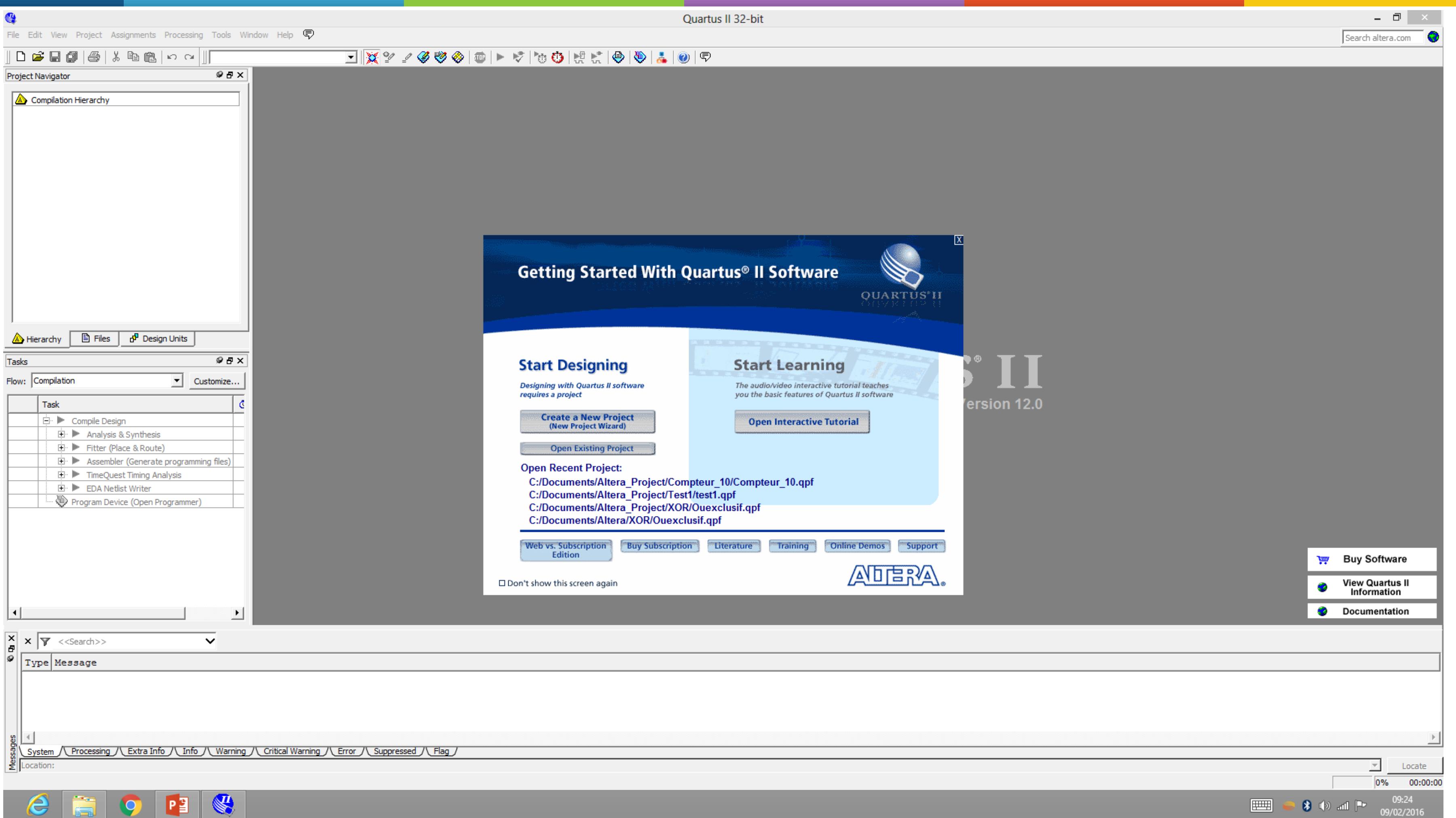
- Logiciel permettant le développement jusqu'à l'implémentation sur la carte FPGA
- Téléchargement gratuit sur www.altera.com

● Simulateur ModelSim-Altera Web Edition.

● Carte de développement DE0 et DE2



Prise en main de Quartus II





Prise en main de Quartus II

Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4

Primed to Perform
Go faster on next generation devices with the Spectra-Q™ engine.
Introducing the New Software → Quartus® Prime Design Software

ALTERA.

QUARTUS® II Version 12.0

Buy Software
Download New Software Release
Documentation

<> Search <>
Type Message

Messages
System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag

Location:
Starts the New Project Wizard

0% 00:00:00 09:25 09/02/2016

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Prise en main de Quartus II

The screenshot shows the Quartus II 32-bit software interface. The main window displays the "New Project Wizard" dialog box, which is currently on the "Introduction" page. The wizard explains its purpose: "The New Project Wizard helps you create a new project and preliminary project settings, including the following:" followed by a bulleted list of items. Below this, it states: "You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project." At the bottom of the dialog, there is a checkbox for "Don't show me this introduction again" and navigation buttons for "< Back", "Next >", "Finish", "Cancel", and "Help".

The interface also includes:

- Project Navigator:** Shows a "Compilation Hierarchy" tree.
- Tasks:** A panel showing a task flow: Compilation → Analysis & Synthesis → Fitter (Place & Route) → Assembler (Generate programming files) → TimeQuest Timing Analysis → EDA Netlist Writer → Program Device (Open Programmer).
- Message Center:** A search bar and a message input field labeled "Type Message".
- System Bar:** Includes icons for browser, file explorer, Google Chrome, Microsoft Word, and a network connection, along with system status indicators like battery level, signal strength, and date/time (09:25, 09/02/2016).



Prise en main de Quartus II

The screenshot shows the Quartus II 32-bit software interface. The main window displays the "New Project Wizard" with the first step, "Directory, Name, Top-Level Entity [page 1 of 5]". The working directory is set to "C:/Documents/Altera_Project/compteur_fpga", the project name to "compteur_10", and the top-level entity name to "compteur_10". The background features a promotional banner for Quartus Prime.

File Edit View Project Assignments Processing Tools Window Help

Quartus II 32-bit

Project Navigator

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New Project Wizard

Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?
C:/Documents/Altera_Project/compteur_fpga

What is the name of this project?
compteur_10

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
compteur_10

Use Existing Project Settings...

Tasks

Flow: Compilation Customize...

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming files)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

< Back Next > Finish Cancel Help

Buy Software

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Documentation

<> <<Search>>

Type Message

Messages

System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag

Location: Locate 0% 00:00:00

09:26 09/02/2016



Prise en main de Quartus II

The screenshot shows the Quartus II 32-bit software interface. The main window displays the "New Project Wizard" with the title "Add Files [page 2 of 5]". The wizard instructions state: "Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project." Below this, there is a table with columns: File Name, Type, Library, Design Entry/Synthesis Tool, and HDL Version. To the right of the table are buttons for Add, Add All, Remove, Up, Down, and Properties. At the bottom of the wizard window, there is a note: "Specify the path names of any non-default libraries. User Libraries...". Below the wizard, there are navigation buttons: < Back, Next >, Finish, Cancel, and Help.

Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

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New Project Wizard

Add Files [page 2 of 5]

Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.

Note: you can always add design files to the project later.

File Name	Type	Library	Design Entry/Synthesis Tool	HDL Version
-----------	------	---------	-----------------------------	-------------

Add

Add All

Remove

Up

Down

Properties

Specify the path names of any non-default libraries. User Libraries...

< Back Next > Finish Cancel Help

Buy Software

Download New Software Release

Documentation

Tasks

Flow: Compilation Customize...

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming files)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

Messages

Type Message

System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag

Location: Locate 0% 00:00:00

09:27 09/02/2016



Prise en main de Quartus II

Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

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New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family

Family: Cyclone IV E
Devices: All

Show in 'Available devices' list

Package: FBGA
Pin count: 256
Speed grade: 6
Name filter:

Target device

Auto device selected by the Filter
 Specific device selected in 'Available devices' list
 Other: n/a

Show advanced devices HardCopy compatible only

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	pal Clo
EP4CE6F17C6	1.2V	6272	180	276480	30	2	10
EP4CE10F17C6	1.2V	10320	180	423936	46	2	10
EP4CE15F17C6	1.2V	15408	166	516096	112	4	20
EP4CE22F17C6	1.2V	22320	154	608256	132	4	20

Companion device

HardCopy:

Limit DSP & RAM to HardCopy device resources

< Back | Next > | Finish | Cancel | Help

Buy Software

Download New Software Release

Documentation

<> <<Search>>

Type Message

Messages

System / Processing / Extra Info / Info / Warning / Critical Warning / Error / Suppressed / Flag

Location: 0% 00:00:00

Locate 09:27 09/02/2016

Internet Explorer Google Chrome Microsoft Word Microsoft Excel



Prise en main de Quartus II

The screenshot shows the Quartus II 32-bit software interface. A central window displays the "New Project Wizard" with the title "EDA Tool Settings [page 4 of 5]". The wizard is prompting the user to specify other EDA tools used with the Quartus II software to develop their project. The "EDA tools:" section contains a table with the following data:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	VHDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

Below the table, there are buttons for "< Back", "Next >", "Finish", "Cancel", and "Help". To the right of the wizard, a sidebar features links for "Buy Software", "Download New Software Release", and "Documentation". The main workspace of the Quartus II interface includes the Project Navigator, Tasks panel, and a central workspace area.



Prise en main de Quartus II

The screenshot shows the Quartus II 32-bit software interface. A central window displays the "New Project Wizard - Summary [page 5 of 5]" dialog. The dialog lists the following project settings:

Setting	Value
Project directory:	C:/Documents/Altera_Project/compteur_fpga
Project name:	compteur_10
Top-level design entity:	compteur_10
Number of files added:	0
Number of user libraries added:	0
Device assignments:	Cyclone IV E
Device:	EP4CE22F17C6
EDA tools:	<None> (<None>)
Design entry/synthesis:	<None>
Simulation:	ModelSim-Altera (VHDL)
Timing analysis:	0
Operating conditions:	
VCCINT voltage:	1.2V
Junction temperature range:	0-85 °C

Below the dialog, the main workspace shows the "Project Navigator" and "Tasks" panes. The "Project Navigator" pane is titled "Compilation Hierarchy" and contains a single entry: "compteur_10". The "Tasks" pane shows a tree view of compilation tasks: "Compile Design", "Analysis & Synthesis", "Fitter (Place & Route)", "Assembler (Generate programming files)", "TimeQuest Timing Analysis", "EDA Netlist Writer", and "Program Device (Open Programmer)".

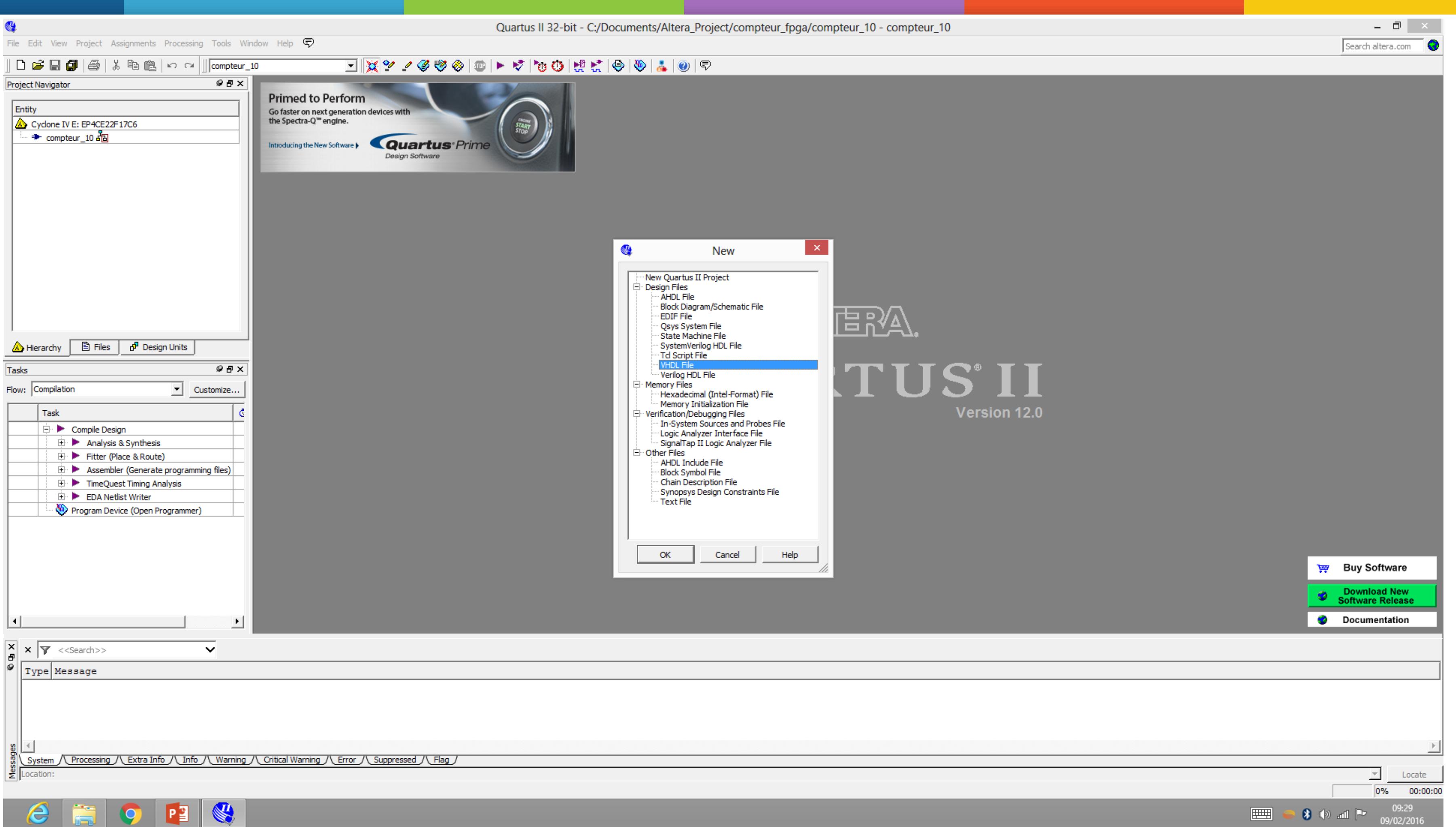


Prise en main de Quartus II

Enseignes et afficheurs à LED | FPGA



Prise en main de Quartus II





Prise en main de Quartus II

The screenshot shows the Quartus II 32-bit software interface. The main window displays a VHDL code for a 10-bit counter. The code defines an entity 'Compteur_10' with a single output port Q (STD_LOGIC_VECTOR(3 downto 0)) and two input ports Ck (IN STD_LOGIC) and R (IN STD_LOGIC). The architecture 'Structural' contains a process that updates Q based on Ck and R. If R is '0', Q remains at "0000". If Ck's edge and Ck = '1', Q is incremented by 1. A specific condition checks if Q equals "1010", in which case it is reset to "0000". The process ends with an IF statement and an END PROCESS block. The code concludes with an END Structural statement.

```
1 Library ieee;
2 Use ieee.std_logic_1164.all;
3 Use ieee.numeric_std.all;
4
5 ENTITY Compteur_10 IS
6 PORT (Ck, R : IN STD_LOGIC;
7 Q: OUT STD_LOGIC_VECTOR (3 downto 0));
8 END Compteur_10;
9
10 ARCHITECTURE Structural OF Compteur_10 IS
11 SIGNAL Qa: STD_LOGIC_VECTOR (3 downto 0);
12 BEGIN
13 PROCESS(Ck, R) -- liste de sensibilité
14 BEGIN
15 IF R = '0' then
16 Qa <= "0000";
17 ELSIF Ck'event and Ck = '1' then -- validation du front montant
18 Qa <= STD_LOGIC_VECTOR(UNSIGNED (Qa) + 1);
19 IF Qa="1010" THEN Qa <= "0000";
20 END IF;
21 END IF;
22 END PROCESS;
23 Q <= Qa;
24
25 END Structural;
```

The interface includes a Project Navigator on the left showing the entity 'compteur_10' for a Cyclone IV E: EP4CE22F17C6 device. Below it are tabs for Hierarchy, Files, and Design Units. A Tasks panel lists compilation steps like Compile Design, Analysis & Synthesis, and Fitter. At the bottom, a search bar and message logs are visible.



Prise en main de Quartus II

The screenshot shows the Quartus II 32-bit software interface. The main window displays a VHDL code for a 10-bit counter:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.NUMERIC_STD.all;

entity Compteur_10 is
    port (Q : OUT STD_LOGIC_VECTOR (3 downto 0));
end Compteur_10;

architecture Structural of Compteur_10 is
    signal Qa: STD_LOGIC_VECTOR (3 downto 0);
begin
    process(Ck, R) -- liste de sensibilité
    begin
        if R = '0' then
            Qa <= "0000";
        elsif Ck'event and Ck = '1' then -- validation du front montant
            Qa <= STD_LOGIC_VECTOR(UNSIGNED (Qa) + 1);
            if Qa="1010" then Qa <= "0000";
        end if;
    end process;
    Q <= Qa;
end Structural;
```

The interface includes a Project Navigator on the left showing an Entity named "compteur_10" for a Cyclone IV E: EP4CE22F17C6 device. The Tasks panel shows a list of compilation steps: Compile Design, Analysis & Synthesis, Fit (Place & Route), Assembler (Generate programming files), TimeQuest Timing Analysis, EDA Netlist Writer, and Program Device (Open Programmer). The bottom message window shows a search bar and a list of messages, with the status bar indicating a new compilation has started.



Prise en main de Quartus II

The screenshot shows the Quartus II 32-bit software interface with the following details:

- Project Navigator:** Shows the project structure with an entity named "Compteur_10" under "Cyclone IV E: EP4CE22F17C6".
- Flow Summary:** Displays the compilation results for "Compteur_10.vhd".

Category	Value
Flow Status	Successful - Tue Feb 09 09:32:30 2016
Quartus II Version	12.0 Build 263 08/02/2012 SP 2 SJ Web Edition
Revision Name	compteur_10
Top-level Entity Name	Compteur_10
Family	Cyclone IV E
Device	EP4CE22F17C6
Timing Models	Final
Total logic elements	4 / 22,320 (< 1 %)
Total combinational functions	4 / 22,320 (< 1 %)
Dedicated logic registers	4 / 22,320 (< 1 %)
Total registers	4
Total pins	6 / 154 (4 %)
Total virtual pins	0
Total memory bits	0 / 608,256 (0 %)
Embedded Multiplier 9-bit elements	0 / 132 (0 %)
Total PLLs	0 / 4 (0 %)
- Tasks:** Shows a list of completed tasks:
 - Compile Design
 - Analysis & Synthesis
 - Fitter (Place & Route)
 - Assembler (Generate programming files)
 - TimeQuest Timing Analysis
 - EDA Netlist Writer
 - Program Device (Open Programmer)
- Compilation Report:** A modal dialog box displays the message "Full Compilation was successful (11 warnings)".
- Messages:** A log window at the bottom shows the following output:

```
Info (204019): Generated file compteur_10_min_1200mv_0c_vhd.fast.sdo in folder "C:/Documents/Altera_Project/compteur_fpga/simulation/modelsim/" for EDA simulation tool
Info (204019): Generated file compteur_10_vhd.sdo in folder "C:/Documents/Altera_Project/compteur_fpga/simulation/modelsim/" for EDA simulation tool
Info: Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
Info (293026): Skipped module PowerPlay Power Analyzer due to the assignment FLOW_ENABLE_POWER_ANALYZER
Info (293000): Quartus II Full Compilation was successful. 0 errors, 11 warnings
```



Prise en main de Quartus II

● Validation du circuit



Prise en main de Quartus II

The screenshot shows the Quartus II 32-bit software interface. The title bar indicates the project is 'compteur_10'. The menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, Help, and a search bar for 'altera.com'. The Tools menu is open, showing options like Run Simulation Tool, RTL Simulation (which is selected), Launch Simulation Library Compiler, and Launch Design Space Explorer. The Project Navigator shows an Entity named 'Cyclone IV E: EP4CE22F17C6' with a sub-item 'vhdl Compteur_10'. The Tasks panel shows a list of tasks under 'Compilation' flow, all marked as completed with green checkmarks: Compile Design, Analysis & Synthesis, Fit (Place & Route), Assembler (Generate programming), TimeQuest Timing Analysis, EDA Netlist Writer, and Program Device (Open Programmer). The Messages panel at the bottom displays several informational messages in green, such as 'Info (204019): Generated file ...' and 'Info: Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings'. The status bar at the bottom right shows the date '09/02/2016' and time '09:33'.



Prise en main de Quartus II

The screenshot shows the Quartus II software interface with the following details:

- Title Bar:** Quartus II 12.0 SP2 - C:/Documents/Altera_Project/compteur_fpga/compteur_10 - compteur_10
- Menu Bar:** File, Edit, View, Compile, Simulate, Add, Process, Tools, Layout, Bookmarks, Window, Help
- Toolbars:** Standard, Project, File, Edit, View, Compile, Simulate, Tools, Layout, Bookmarks, Window.
- Libraries:** Library pane showing various Altera libraries like work, rtl_work, 220model, altera, etc.
- Objects:** Objects pane showing a large blue area representing the design.
- Processes (Active):** Processes pane showing a list of active processes.
- Transcript:** Transcript pane showing the command: # -- Compiling architecture Structural of Compteur_10.
- Messages:** Messages pane showing compilation logs:

```
Info (22036): Successfully launched NativeLink simulation (quartus_sh -t "c:/altera/12.0sp2/quartus/common/tcl/internal/nativelink/qnativesim.tcl" --rtl_sim "compteur_10" "compteur_10")
Info (22036): For messages from NativeLink execution see the NativeLink log file C:/Documents/Altera_Project/compteur_fpga/compteur_10_nativelink_simulation.rpt
```
- Bottom Bar:** Icons for Internet Explorer, File Explorer, Google Chrome, Microsoft Word, Microsoft Excel, and the Quartus II logo. Status bar showing 100% 00:00:16, 09:34, and 09/02/2016.



Prise en main de Quartus II

ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help

Library Objects Processes (Active)

Transcript

```
# -- Compiling architecture Structural of Compteur_10
#
ModelSim>
```

<No Design Loaded> compteur_10

09:34 09/02/2016



Prise en main de Quartus II

ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help

Library

Name	Type	Path
work	Library	rtl_work
+ E comp	Simulate	a_Project/compte...
+ rtl_work	Simulate without Optimization	a_Project/compte...
+ 220mod	Simulate with full Optimization	altera/vhdl/220model
+ 220mod	Simulate with Coverage	altera/verilog/220m...
+ altera	Edit	altera/vhdl/altera
+ altera_lr	Refresh	altera/vhdl/altera_l...
+ altera_lr	Recompile	altera/vhdl/altera_mf
+ altera_n	Optimize	altera/verilog/altera
+ altera_v	Update	altera/verilog/altera
+ altgxb	Create Wave	altera/vhdl/altgxb
+ altgxb_	Delete	teravhdl/altgxb
+ arriagx	Copy	teravhdl/arriagx
+ arriagx	New	teravhdl/arriagx...
+ arriagx	Properties...	teravhdl/arriagx
+ arraii	Library	\$MODEL_TECH/..altera/vhdl/arraii
+ arraii_hssi	Library	\$MODEL_TECH/..altera/vhdl/arraii_hssi
+ arraii_hssi_ver	Library	\$MODEL_TECH/..altera/verilog/arraii...
+ arraii_pcie_	Library	\$MODEL_TECH/..altera/vhdl/arraii_p...
+ arraii_pcie_	Library	\$MODEL_TECH/..altera/verilog/arraii...
+ arraii_ver	Library	\$MODEL_TECH/..altera/verilog/arraii
+ arraiigz	Library	\$MODEL_TECH/..altera/vhdl/arraigz
+ arraiigz_hssi	Library	\$MODEL_TECH/..altera/vhdl/arraigz...
+ arraiigz_hssi_ver	Library	\$MODEL_TECH/..altera/verilog/arraigz...
+ arraiigz_pcie_	Library	\$MODEL_TECH/..altera/vhdl/arraigz...
+ arraiigz_pcie_	Library	\$MODEL_TECH/..altera/verilog/arraigz...
+ arraiigz_ver	Library	\$MODEL_TECH/..altera/verilog/arraigz
+ arrav	Library	\$MODEL_TECH/..altera/vhdl/arrav
+ arrav_hssi_ver (e...)	Library	\$MODEL_TECH/..altera/verilog/arrav...
+ arrav_pcie_	Library	\$MODEL_TECH/..altera/verilog/arrav...
+ arrav_ver (empty)	Library	\$MODEL_TECH/..altera/verilog/arrav
+ arravgz	Library	\$MODEL_TECH/..altera/vhdl/arravgz
+ arravgz_hssi	Library	\$MODEL_TECH/..altera/vhdl/arravgz...
+ arravgz_hssi_ver (..)	Library	\$MODEL_TECH/..altera/verilog/arrav...
+ arravgz_pcie_	Library	\$MODEL_TECH/..altera/vhdl/arravgz...
+ arravgz_pcie_	Library	\$MODEL_TECH/..altera/verilog/arrav...
+ arravgz_ver (empty)	Library	\$MODEL_TECH/..altera/verilog/arravgz
+ cyclone	Library	\$MODEL_TECH/..altera/vhdl/cyclone
+ cyclone_ver	Library	\$MODEL_TECH/..altera/verilog/cyclone
+ cycloneii	Library	\$MODEL_TECH/..altera/vhdl/cycloneii
+ cycloneii_ver	Library	\$MODEL_TECH/..altera/verilog/cycloneii
+ cycloneiii	Library	\$MODEL_TECH/..altera/vhdl/cycloneiii

Objects

Name	Value	Kind	Mode
Ck	U	Signal	In
R	U	Signal	In
Q	UUUU	Signal	Out
QA	UUUU	Signal	Internal

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path
line_23	VHDL Process	Active	1	/compteur_10
line_13	VHDL Process	Ready	2	/compteur_10

Transcript

```
# Loading ieee.numeric_std(body)
# Loading work.compteur_10(structural)

VSIM 3>
```

Now: 0 ps Delta: 0 sim:/compteur_10

09:34 09/02/2016



Prise en main de Quartus II

ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help

Library Objects Wave - Default Transcript

Now: 0 ps Delta: 0 sim:/compteur_10

0 ps 200 ps 400 ps 600 ps 800 ps 1000 ps

0 ps Cursor 1

0 ps 0 ps

09:35 09/02/2016

Library

Name	Type	Path
work	Library	rtl_work
+ E compteur_10	Entity	C:/Documents/Altera_Project/compteur_10
+ rtl_work	Library	C:/Documents/Altera_Project/compteur_10/rtl_work
+ 220model	Library	\$MODEL_TECH../altera/vhdl/220model
+ 220model_ver	Library	\$MODEL_TECH../altera/verilog/220model
+ altera	Library	\$MODEL_TECH../altera/vhdl/altera
+ altera_lsim	Library	\$MODEL_TECH../altera/vhdl/altera_lsim
+ altera_lsim_ver	Library	\$MODEL_TECH../altera/verilog/altera_lsim
+ altera_mf	Library	\$MODEL_TECH../altera/vhdl/altera_mf
+ altera_mf_ver	Library	\$MODEL_TECH../altera/verilog/altera_mf
+ altera_ver	Library	\$MODEL_TECH../altera/verilog/altera
+ altgxb	Library	\$MODEL_TECH../altera/vhdl/altgxb
+ altgxb_ib	Library	\$MODEL_TECH../altera/vhdl/altgxb_ib
+ altgxb_ver	Library	\$MODEL_TECH../altera/verilog/altgxb
+ arriagx	Library	\$MODEL_TECH../altera/vhdl/arriagx
+ arriagx_hssi	Library	\$MODEL_TECH../altera/vhdl/arriagx_hssi
+ arriagx_hssi_ver	Library	\$MODEL_TECH../altera/verilog/arriagx_hssi
+ arriagx_ver	Library	\$MODEL_TECH../altera/vhdl/arriagx
+ arraii	Library	\$MODEL_TECH../altera/vhdl/arraii
+ arraii_hssi	Library	\$MODEL_TECH../altera/vhdl/arraii_hssi
+ arraii_hssi_ver	Library	\$MODEL_TECH../altera/verilog/arraii_hssi
+ arraii_pcie_1p1	Library	\$MODEL_TECH../altera/vhdl/arraii_pcie_1p1
+ arraii_ver	Library	\$MODEL_TECH../altera/verilog/arraii
+ arraiigz	Library	\$MODEL_TECH../altera/vhdl/arraigz
+ arraiigz_hssi	Library	\$MODEL_TECH../altera/vhdl/arraigz_hssi
+ arraiigz_hssi_ver	Library	\$MODEL_TECH../altera/verilog/arraigz_hssi
+ arraiigz_pcie_1p1	Library	\$MODEL_TECH../altera/vhdl/arraigz_pcie_1p1
+ arraiigz_pcie_1p1_v	Library	\$MODEL_TECH../altera/verilog/arraigz_pcie_1p1
+ arraiigz_ver	Library	\$MODEL_TECH../altera/verilog/arraigz
+ arriav	Library	\$MODEL_TECH../altera/vhdl/arraiv
+ arriav_hssi_ver (empty)	Library	\$MODEL_TECH../altera/verilog/arraiv
+ arriav_pcie_1p1	Library	\$MODEL_TECH../altera/vhdl/arraiv_pcie_1p1
+ arriav_ver (empty)	Library	\$MODEL_TECH../altera/verilog/arraiv
+ arriavgz	Library	\$MODEL_TECH../altera/vhdl/arraivgz
+ arriavgz_hssi	Library	\$MODEL_TECH../altera/vhdl/arraivgz_hssi
+ arriavgz_hssi_ver (empty)	Library	\$MODEL_TECH../altera/verilog/arraivgz_hssi
+ arriavgz_pcie_1p1	Library	\$MODEL_TECH../altera/vhdl/arraivgz_pcie_1p1
+ arriavgz_pcie_1p1_v	Library	\$MODEL_TECH../altera/verilog/arraivgz_pcie_1p1
+ arriavgz_ver (empty)	Library	\$MODEL_TECH../altera/verilog/arraivgz
+ cyclone	Library	\$MODEL_TECH../altera/vhdl/cyclone
+ cyclone_ver	Library	\$MODEL_TECH../altera/verilog/cyclone

Objects

Name	Value	Kind	Mode
Ck	U	Signal	In
R	U	Signal	In
Q	UUUU	Signal	Out
Qa	UUUU	Signal	Internal

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path
line_23	VHDL Process	Active	1	/compteur_10
line_13	VHDL Process	Ready	2	/compteur_10

Wave - Default

Msgs

0 ps 200 ps 400 ps 600 ps 800 ps 1000 ps

0 ps Now Cursor 1

0 ps 0 ps

09:35 09/02/2016



Prise en main de Quartus II

ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

Library Objects Wave - Default Processes (Active)

Objects (Selected): Ck, R, Q, Qa

Wave - Default (Empty)

Processes (Active): line_23, line_13

Transcript:

```
wave create -pattern none -portmode out -language vhdl -range 3 0 /compteur_10/Q
# compteur_10

VSIM 6>
```

Now: 0 ps Delta: 0 sim:/compteur_10 0 ps to 1 ns

09:35 09/02/2016



Prise en main de Quartus II

ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

Library Objects Wave - Default

Library Objects Wave - Default

Create Pattern Wizard

Select Pattern

Patterns

- Clock
- Constant
- Random
- Repeater
- Counter

Signal Name: Edit:/compteur_10/Ck

Start Time: 0 End Time: 100 Time Unit: us

Transcript

```
wave create -pattern none -portmode out -language vhdl -range 3 0 /compteur_10/Q
# compteur_10
```

VSIM 6>

Now: 0 ps Delta: 0 sim:/compteur_10 0 ps to 1 ns

09:36 09/02/2016



Prise en main de Quartus II

ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

Library Objects Wave - Default Transcript

Now: 0 ps Delta: 0 sim:/compteur_10 0 ps to 1 ns 09:37 09/02/2016

Library sim

Objects

Name	Type	Path
work	Library	rtl_work
+ E compteur_10	Entity	C:/Documents/Altera_Project/compte...
rtl_work	Library	C:/Documents/Altera_Project/compte...
220model	Library	\$MODEL_TECH../altera/vhdl/220model
220model_ver	Library	\$MODEL_TECH../altera/verilog/220m...
altera	Library	\$MODEL_TECH../altera/vhdl/altera
altera_lsim	Library	\$MODEL_TECH../altera/vhdl/altera_l...
altera_lsim_ver	Library	\$MODEL_TECH../altera/verilog/altera...
altera_mf	Library	\$MODEL_TECH../altera/vhdl/altera_mf
altera_mf_ver	Library	\$MODEL_TECH../altera/verilog/altera...
altera_ver	Library	\$MODEL_TECH../altera/verilog/altera
altgxb	Library	\$MODEL_TECH../altera/vhdl/altgxb
altgxb_ib	Library	\$MODEL_TECH../altera/vhdl/altgxb
altgxb_ver	Library	\$MODEL_TECH../altera/verilog/altgxb
arriagx	Library	\$MODEL_TECH../altera/vhdl/arriagx
arriagx_hssi	Library	\$MODEL_TECH../altera/vhdl/arriagx_...
arriagx_hssi_ver	Library	\$MODEL_TECH../altera/verilog/arriag...
arriagx_ver	Library	\$MODEL_TECH../altera/vhdl/arriagx
arriai	Library	\$MODEL_TECH../altera/vhdl/arriai
arriai_hssi	Library	\$MODEL_TECH../altera/vhdl/arriai_hssi
arriai_hssi_ver	Library	\$MODEL_TECH../altera/verilog/arriai...
arriai_pcie_1p	Library	\$MODEL_TECH../altera/vhdl/arriai_p...
arriai_pcie_1p_ver	Library	\$MODEL_TECH../altera/verilog/arriai...
arriai_ver	Library	\$MODEL_TECH../altera/verilog/arriai
arriaiigz	Library	\$MODEL_TECH../altera/vhdl/arriaiigz
arriaiigz_hssi	Library	\$MODEL_TECH../altera/vhdl/arriaiigz...
arriaiigz_hssi_ver	Library	\$MODEL_TECH../altera/verilog/arriai...
arriaiigz_pcie_1p	Library	\$MODEL_TECH../altera/vhdl/arriaiigz...
arriaiigz_pcie_1p_ver	Library	\$MODEL_TECH../altera/verilog/arriai...
arriaiigz_ver	Library	\$MODEL_TECH../altera/verilog/arriaiigz
arriav	Library	\$MODEL_TECH../altera/vhdl/arriav
arriav_hssi_ver (e...)	Library	\$MODEL_TECH../altera/verilog/arriav...
arriav_pcie_1p_ver	Library	\$MODEL_TECH../altera/verilog/arriav...
arriav_ver (empty)	Library	\$MODEL_TECH../altera/verilog/arriav
arriavgz	Library	\$MODEL_TECH../altera/vhdl/arriavgz
arriavgz_hssi	Library	\$MODEL_TECH../altera/vhdl/arriavgz...
arriavgz_hssi_ver (e...)	Library	\$MODEL_TECH../altera/verilog/arriav...
arriavgz_pcie_1p	Library	\$MODEL_TECH../altera/vhdl/arriavgz...
arriavgz_pcie_1p_ver	Library	\$MODEL_TECH../altera/verilog/arriav...
arriavgz_ver (empty)	Library	\$MODEL_TECH../altera/verilog/arriavgz
cyclone	Library	\$MODEL_TECH../altera/vhdl/cyclone
cyclone_ver	Library	\$MODEL_TECH../altera/verilog/cyclone

Objects

Name	Type	Value	Kind	Mode
Ck	Signal In	U	Signal	In
R	Signal In	U	Signal	In
Q	Signal Out	UUUU	Signal	Out
Qa	Internal	UUUU	Signal	Internal

Wave - Default

Edit:/compteur_10/Ck No Data

Edit:/compteur_10/R No Data

Edit:/compteur_10/Q No Data

Specify the Clock Pattern Attributes.

Processes

Initial Value: 0

Clock Period: 20 ns

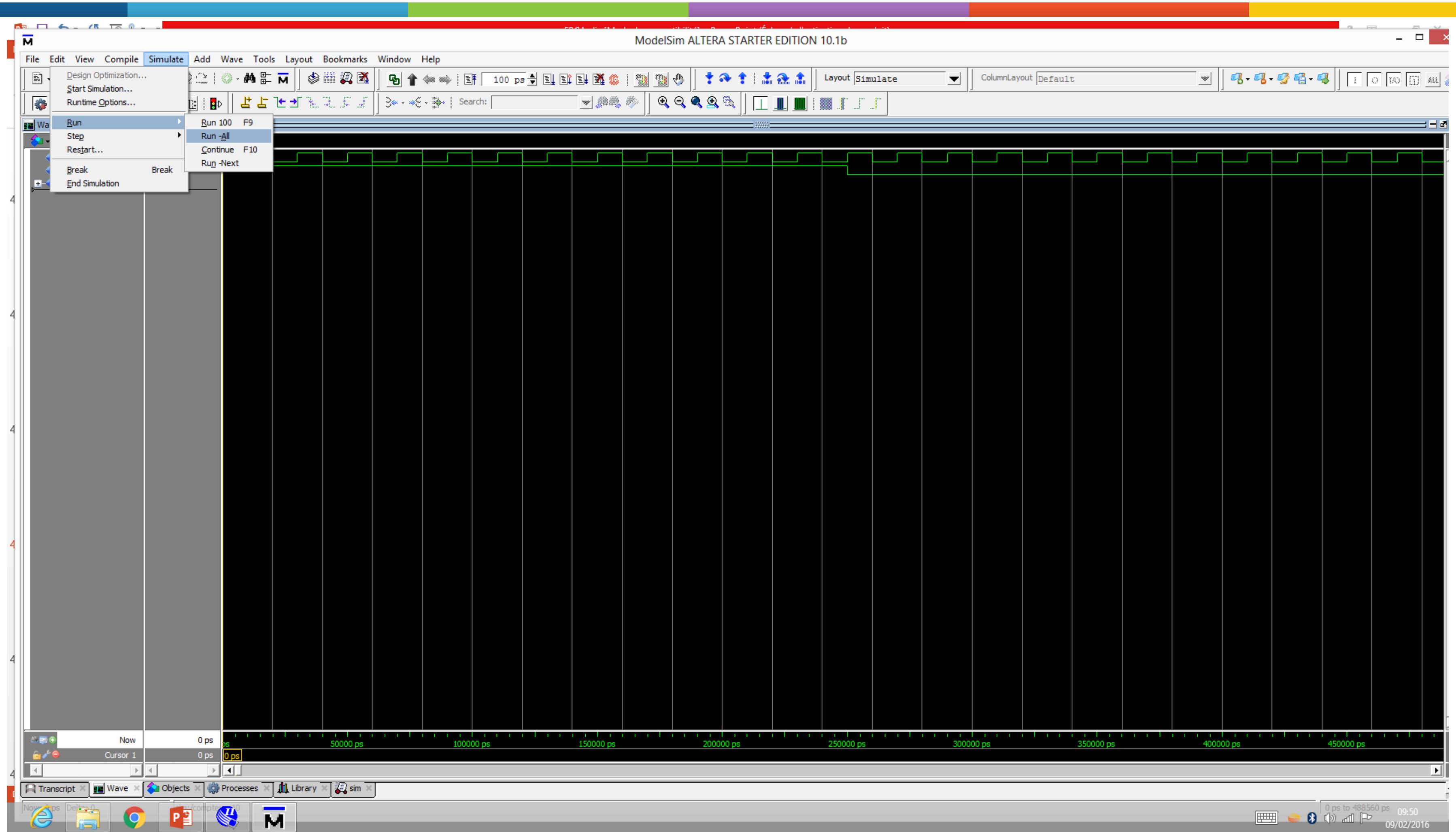
Duty Cycle: 50

Transcript

```
wave create -pattern none -portmode out -language vhdl -range 3 0 /compteur_10/Q
# compteur_10
VSIM 10>
```



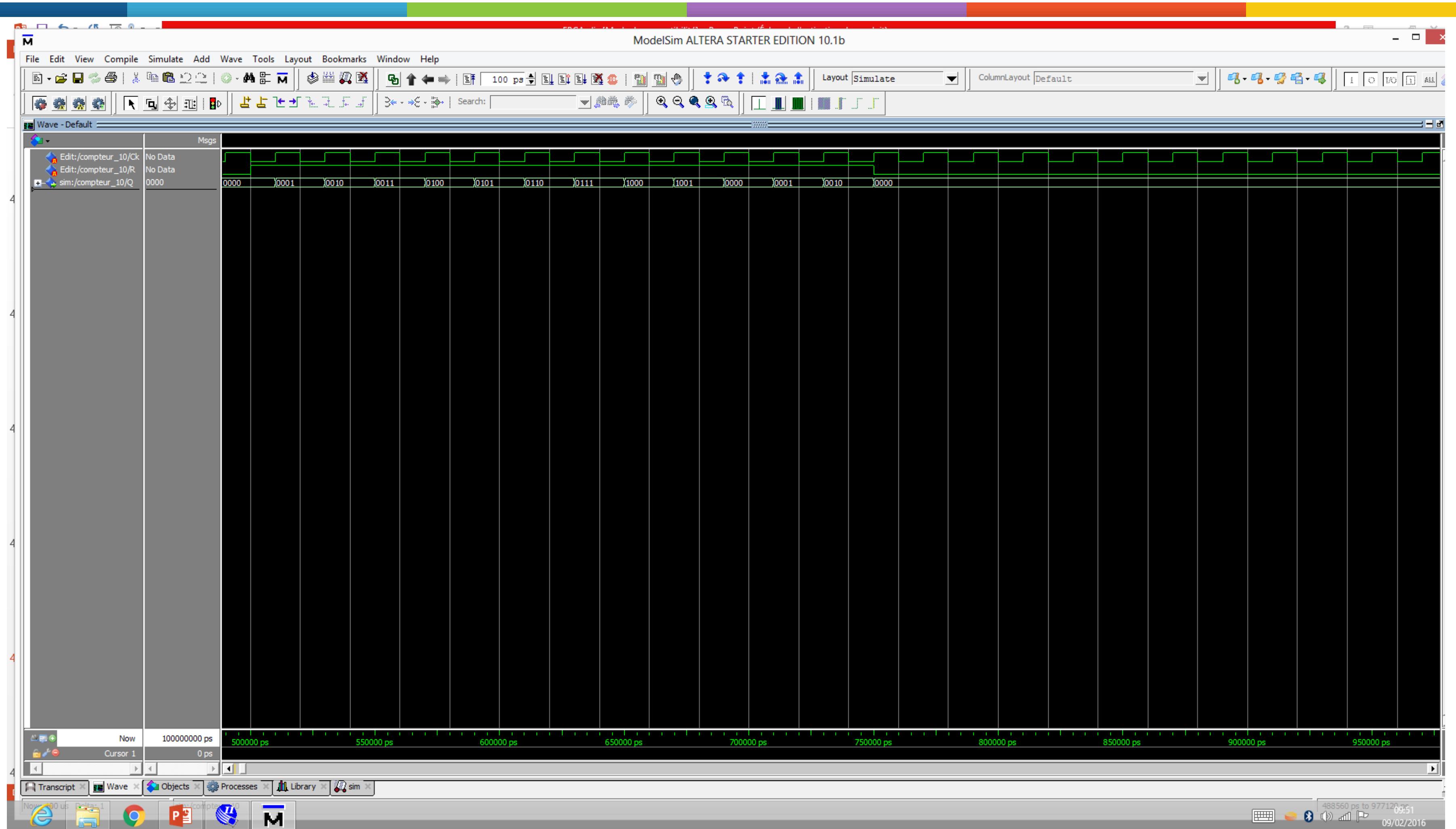
Prise en main de Quartus II



Enseignes et afficheurs à LED | FPGA



Prise en main de Quartus II



Enseignes et afficheurs à LED | FPGA



Prise en main de Quartus II

Implémentation sur FPGA DEII

- Assignation des PINs

Signaux	Nom	Pin
Ck	KEY[0]	PIN_G26
R	SW[0]	PIN_N25
Q(0)	LER[0]	PIN_AE23
Q(1)	LER[1]	PIN_AF23
Q(2)	LER[2]	PIN_AB21
Q(3)	LER[3]	PIN_AC22



Prise en main de Quartus II

Implémentation sur FPGA DE0

- Assignation des PINs

Signaux	Nom	Pin
Ck	KEY[0]	PIN_J15
R	KEY[1]	PIN_E1
Q(0)	LER[0]	PIN_A15
Q(1)	LER[1]	PIN_A13
Q(2)	LER[2]	PIN_B13
Q(3)	LER[3]	PIN_A11



Prise en main de Quartus II

Quartus II - D:/Altera_Project/Compteur_10/Compteur_10 - Compteur_10 - [Compteur_10.vhd]

File Edit View Project Assignments Processing Tools Window Help

Status

Module	Progress %	Time
Simulator	100 %	00:00:

Module: Compteur_10

Assignment Editor Ctrl+Shift+A

Pins

Timing Analysis Settings...

EDA Tool Settings...

Settings... Ctrl+Shift+E

Classic Timing Analyzer Wizard...

Assignment Editor Ctrl+Shift+A

Pin Planner Ctrl+Shift+N

Remove Assignments...

Demote Assignments...

Back-Annotate Assignments...

Import Assignments...

Export Assignments...

Assignment (Time) Groups...

Timing Closure Floorplan

LogicLock Regions Window Alt+L

Design Partitions Window Alt+D

Device...

ary ieee;

ieee.std_logic_1164.all;

ieee.numeric_std.all;

ENTITY Compteur_10 IS

(Ck, R : IN STD_LOGIC;

OUT STD_LOGIC_VECTOR (3 downto 0));

Compteur_10;

ARCHITECTURE Structural OF Compteur_10 IS

SIGNAL Qa: STD_LOGIC_VECTOR (3 downto 0);

BEGIN

PROCESS(Ck, R) -- liste de sensibilité

IN

IF R = '0' then

Qa <= "0000";

IF Ck'event and Ck = '1' then -- validation du front montant

Qa <= STD_LOGIC_VECTOR(UNSIGNED (Qa) + 1);

IF Qa="1010" THEN Qa <= "0000";

END IF;

END IF;

PROCESS;

Q <= Qa;

24

25 END Structural;

26

Info: Quartus II Simulator was successful. 0 errors, 0 warnings

Messages

\ System \ Processing \ Extra Info \ Info \ Warning \ Critical Warning \ Error \ Suppressed /

Message: 0 of 15

Edits assignments for the current focus entity

Ln 26, Col 1

Idle

démarrer Explorat... quartus Counter2.vhd... fpga-rgb-ma... DE2_UserMa... TP_CLM_1.d... Quartus II - ... Circuits sequ... FPGA-dia.p... FR 20:00

Prise en main de Quartus II



The screenshot shows the Quartus II software interface. The main window displays a VHDL code for a 10-bit counter. The code includes library declarations for IEEE, entity and architecture definitions, and a process block for updating the counter. An 'Ouvrir' (Open) dialog box is overlaid on the main window, showing a file selection tree and a list of files in the 'Compteur_10' project directory. The dialog includes fields for selecting a file type ('All Files (*.*)'), adding the file to the current project, and opening options ('Auto').

```
1 Library ieee;
2 Use ieee.std_logic_1164.all;
3 Use ieee.numeric_std.all;
4
5 ENTITY Compteur_10 IS
6 PORT (Ck, R : IN STD_LOGIC;
7 Q: OUT STD_LOGIC_VECTOR (3 downto 0));
8 END Compteur_10;
9
10 ARCHITECTURE Structural OF Compteur_10 IS
downto 0);

e sensibilité

en -- validation du front montant
GNED (Qa) + 1);
"0000";
```



Prise en main de Quartus II

Quartus II - D:/Altera_Project/Compteur_10/Compteur_10 - Compteur_10 - [Assignment Editor]

File Edit View Project Assignments Processing Tools Window Help

Compteur_10

Status

Module	Progress %	Time
Simulator	100 %	00:00:02

Information

This cell specifies the destination name for point-to-point assignments. For single-point assignments, this cell specifies the destination of the assignment. Altera recommends using the Node Finder to assign a destination name.

Edit: PIN_G26

To	Assignment Name	Value	Enabled
1 PIN_G26	Location	CK	Yes
2 PIN_N25	Location	R	Yes
3 PIN_AE23	Location	Q(0)	Yes
4 PIN_AF23	Location	Q(1)	Yes
5 PIN_AB21	Location	Q(2)	Yes
6 PIN_AC22	Location	Q(2)	Yes
7 <<new>>	<<new>>		

Messages

```
Info: set_instance_assignment -name PARTITION_HIERARCHY no_file_for_top_partition -to / -section_id Top -remove
```

System Processing Extra Info Info Warning Critical Warning Error Suppressed /

Message: 0 of 96 Locate

For Help, press F1

démarrer Explorat... quartus Counter2.vh... fpga-rgb-ma... DE2_UserMa... TP_CLM_1.d... Quartus II - ... Microsoft... Test.qsf - W... FR 20:13



Prise en main de Quartus II

Quartus II - D:/Altera_Project/Compteur_10/Compteur_10 - Compteur_10 - [Compteur_10.qsf]

File Edit View Project Assignments Processing Tools Window Help

Compteur_10

Status

Module	Progress %	Time
Simulator	100 %	00:00:02

Module Tree

27 set_global_assignment -name FAMILY "Cyclone II"
28 set_global_assignment -name TOP_LEVEL_ENTITY Compteur_10
29 set_global_assignment -name ORIGINAL_QUARTUS_VERSION 7.0
30 set_global_assignment -name PROJECT_CREATION_TIME_DATE "19:00:01 FEBRUARY 05, 2016"
31 set_global_assignment -name LAST_QUARTUS_VERSION 7.0
32 set_global_assignment -name EDA_DESIGN_ENTRY_SYNTHESIS_TOOL "FPGA Compiler II"
33 set_global_assignment -name EDA_INPUT_VCC_NAME VDD -section_id eda_design_synthesis
34 set_global_assignment -name EDA_LMF_FILE fpga_exp.lmf -section_id eda_design_synthesis
35 set_global_assignment -name EDA_INPUT_DATA_FORMAT EDIF -section_id eda_design_synthesis
36 set_global_assignment -name EDA_SIMULATION_TOOL "ModelSim-Altera (VHDL)"
37 set_global_assignment -name EDA_INCLUDE_VHDL_CONFIGURATION_DECLARATION ON -section_id eda_simulation
38 set_global_assignment -name EDA_OUTPUT_DATA_FORMAT VHDL -section_id eda_simulation
39 set_global_assignment -name EDA_TEST_BENCH_ENABLE_STATUS TEST_BENCH_MODE -section_id eda_simulation
40 set_global_assignment -name EDA_NATIVELINK_SIMULATION_TEST_BENCH TB_Test -section_id eda_simulation
41 set_global_assignment -name EDA_TEST_BENCH DESIGN_INSTANCE_NAME i1 -section_id eda_simulation
42 set_global_assignment -name EDA_TIMING_ANALYSIS_TOOL "PrimeTime (VHDL)"
43 set_global_assignment -name EDA_INCLUDE_VHDL_CONFIGURATION_DECLARATION ON -section_id eda_timing_analysis
44 set_global_assignment -name EDA_OUTPUT_DATA_FORMAT VHDL -section_id eda_timing_analysis
45 set_global_assignment -name USER_LIBRARIES "C:\Documents and Settings\Admin_2\Bureau\Matrice_LED_16x32\rgbmatrix:
46 set_global_assignment -name DEVICE_FILTER_PIN_COUNT 672
47 set_global_assignment -name VHDL_FILE Compteur_10.vhd
48 set_instance_assignment -name PARTITION_HIERARCHY no_file_for_top_partition -to | -section_id Top
49 set_global_assignment -name PARTITION_NETLIST_TYPE SOURCE -section_id Top
50 set_global_assignment -name VECTOR_WAVEFORM_FILE Compteur_10.vwf
51
52 set_location_assignment Ck -to PIN_G26
53 set_location_assignment R -to PIN_N25
54 set_location_assignment Q(0) -to PIN_AE23
55 set_location_assignment Q(1) -to PIN_AF23
56 set_location_assignment Q(2) -to PIN_AB21
57 set_location_assignment Q(2) -to PIN_AC22
58

Warning: Partition name "Top" is reserved -- specify a different name

System Processing Extra Info Info Warning Critical Warning Error Suppressed /

Message: 0 of 94

For Help, press F1

Ln 57, Col 37

démarrer Explorat... quartus Counter2.vhd... fpga-rgb-ma... DE2_UserMa... TP_CLM_1.d... Quartus II - ... Microsoft... Test.qsf - W... FR 20:13



Prise en main de Quartus II

Quartus II - D:/Altera_Project/Compteur_10/Compteur_10 - Compteur_10 - [Compilation Report - Flow Summary]

File Edit View Project Assignments Processing Tools Window Help

Status

Module	Progress %	Time
Full Compilation	100 %	00:00
Analysis & Synthesis	100 %	00:00
Partition Merge	100 %	00:00
Fitter	100 %	00:00
Assembler	100 %	00:00
Classic Timing Analyzer	100 %	00:00
EDA Netlist Writer	100 %	00:00

EDA Simulation Tool
Run EDA Timing Analysis Tool
Launch Design Space Explorer
TimeQuest Timing Analyzer
Advisors
Chip Planner (Floorplan & Chip Editor)
Netlist Viewers
SignalTap II Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
SignalProbe Pins...
Programmer
MegaWizard Plug-In Manager...
SOPC Builder...
Tcl Scripts...
Customize...
Options...
License Setup...
Customize Compilation Report...

Flow Status: Successful - Fri Feb 05 20:14:50 2016
Quartus II Version: 7.0 Build 33 02/05/2007 SJ Web Edition
Revision Name: Compteur_10
Top-level Entity Name: Compteur_10
Family: Cyclone II
Device: EP2C35F672C6
Timing Models: Final
Met timing requirements: Yes
Total logic elements: 4 / 33,216 (< 1 %)
Total combinational functions: 4 / 33,216 (< 1 %)
Dedicated logic registers: 4 / 33,216 (< 1 %)
Total registers: 4
Total pins: 6 / 475 (1 %)
Total virtual pins: 0
Total memory bits: 0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements: 0 / 70 (0 %)
Total PLLs: 0 / 4 (0 %)

Info: Quartus II EDA Netlist Writer was successful. 0 errors, 1 warning
Info: Quartus II Full Compilation was successful. 0 errors, 12 warnings

System Processing Extra Info Info Warning Critical Warning Error Suppressed /

Message: 0 of 183

Open a Programmer window

démarrer Explorat... quartus Counter2.vh... fpga-rgb-ma... DE2_UserMa... TP_CLM_1.d... Quartus II - ... Microsoft... Test.qsf - W... FR 20:23



Prise en main de Quartus II

Quartus II - D:/Altera_Project/Compteur_10/Compteur_10 - Compteur_10 - [Compteur_10.cdf*]

File Edit View Project Assignments Processing Tools Window Help

Compteur_10

Status

Module	Progress %	Time
Full Compilation	100 %	00:00
Analysis & Synthesis	100 %	00:00
Partition Merge	100 %	00:00
Fitter	100 %	00:00
Assembler	100 %	00:00
Classic Timing Analyzer	100 %	00:00
EDA Netlist Writer	100 %	00:00

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress: 0 %

Enable real-time ISP to allow background programming (for MAX II devices)

Start Stop Auto Detect Delete Add File... Change File... Save File... Add Device... Up Down

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
Compteur_10.sof	EP2C35F672	002F87EC	FFFFFFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>					

Info: Quartus II EDA Netlist Writer was successful. 0 errors, 1 warning
Info: Quartus II Full Compilation was successful. 0 errors, 12 warnings

System Processing Extra Info Info Warning Critical Warning Error Suppressed /

Message: 0 of 183 Locate

For Help, press F1

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Circuits logiques programmable : FPGA



- Les circuits logiques programmables
- Les circuits FPGA
- Méthodologie de conception des circuits FPGA
- Environnement de développement