WB:

RegWrite

MemtoReg

M:

Branch

MemRead

MemWrite

EX:

ALU_op

RegDst

ALUSrc

IF/ID:

32 pc+4

32 instr

ID/EX:

-----WB-----

1 RegWrite

1 MemtoReg

-----M-----

1 Branch

2 BranchInstr

1 MemRead

1 MemWrite

-----EX-----

3 ALU_op

1 RegDst

1 ALUSrc

---

32 Pc+4

5. RSAddr

5. RTAddr

32 RSData

32 RTData

32 Extended

5. instr[20-16]

5. instr[15-11]

EX/MEM:

-----WB-----

1 RegWrite

1 MemtoReg

-----M-----

1 Branch

2 BranchInstr

1 MemRead

1 MemWrite

---

32 pc_branch

1 . Zero

1 . Greater

32 ALUResult

32 RTData

5. WriteReg

MEM/WB:

-----WB-----

1 RegWrite

1 MemtoReg

---

32 MemData

32 ALUResult

5. WriteReg