2022 Digital IC Design Homework 3

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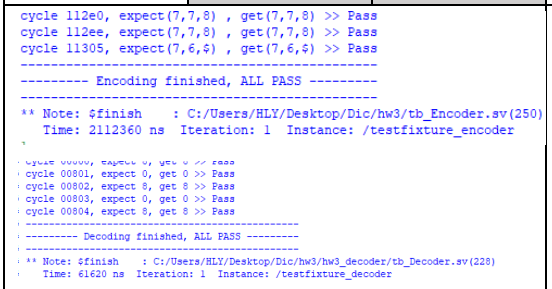
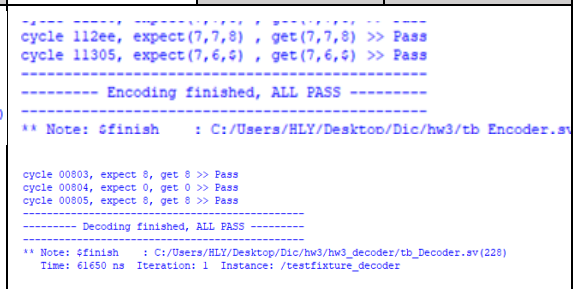
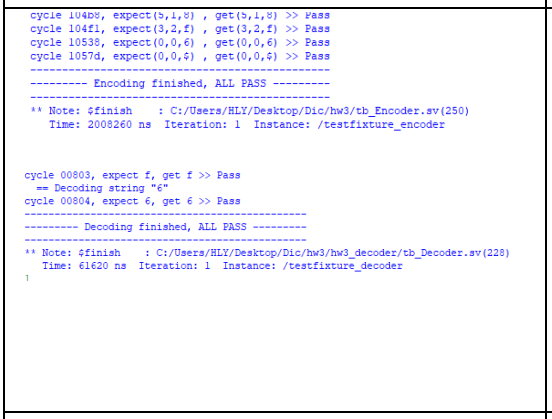
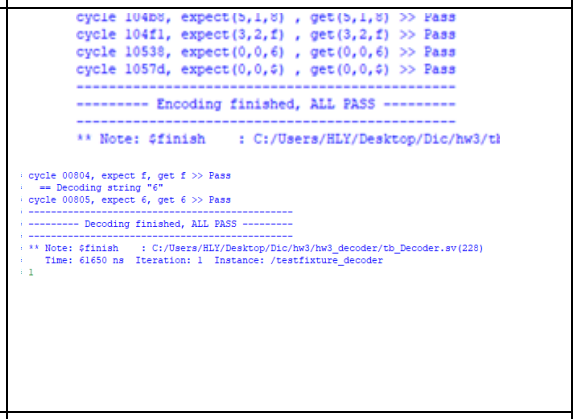
Simulation Result

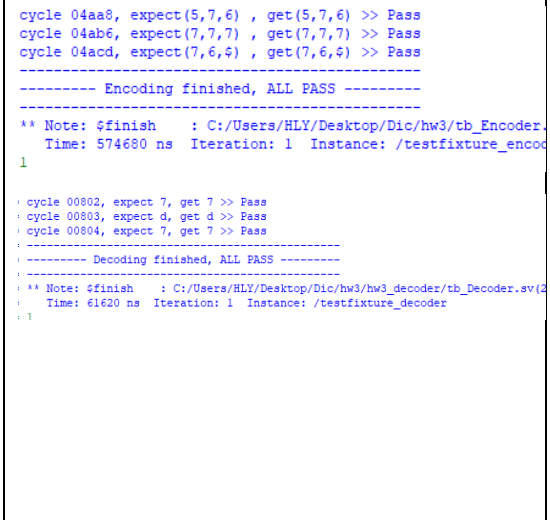
Functional simulation	Pass (encoder)	Pass (decoder)	Gate-level simulation	Pass (encoder)	Pass(decoder)



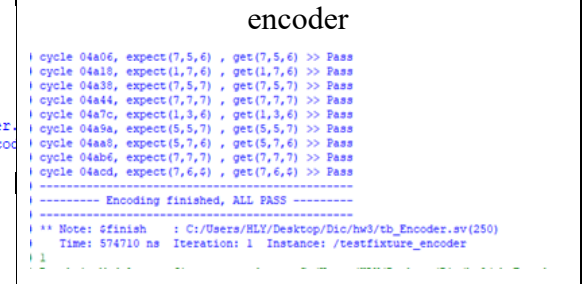




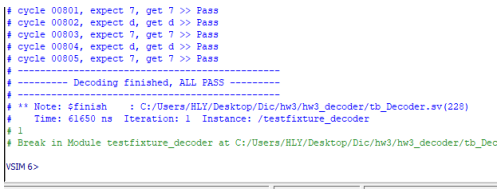




encoder



decoder



Synthesis Result	encoder	decoder
Total logic elements	21569/68416	96/68416
Total memory bit	0/1152000	0/1152000
Embedded multiplier 9-bit element	0/300	0/300

Simulation time img0	574710(ns)	61650(ns)
Simulation time img1	574710(ns)	61650(ns)
Simulation time img2	574710(ns)	61650(ns)

Flow Status	Successful - Fri Apr 29 01:40:09 2022
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	LZ77_Encoder
Top-level Entity Name	LZ77_Encoder
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	21,569 / 68,416 (32 %)
Total combinational functions	21,299 / 68,416 (31 %)
Dedicated logic registers	16,701 / 68,416 (24 %)
Total registers	16701
Total pins	28 / 622 (5 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Flow Summary	
Flow Status	Successful - Thu Apr 28 22:53:35 2022
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	LZ77_Decoder
Top-level Entity Name	LZ77_Decoder
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	96 / 68,416 (< 1 %)
Total combinational functions	66 / 68,416 (< 1 %)
Dedicated logic registers	81 / 68,416 (< 1 %)
Total registers	81
Total pins	27 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

簡介:

Encoder:

我的 state 狀態有 4 個，s0 用在 reset 的狀態，s1 是存 chardata，s2 是將 datamem 存入”sh”、”l_a”、”s_l”，s3 則是”l_a”和”s_l”的匹配。

1.儲存

Encoder 方面我用了 datamem 存 chardata 的資料後，使用三個暫存器儲存資料，分別是”sh”、”l_a”、”s_l”，其中”s_l”代表 search_buffer+look-ahead_buffer。儲存都是用 for 迴圈複製電路。

2.匹配

我取”l_a”和”s_l”的對應位元做比較，並根據對應位元匹配的結果輸出。”t[7]=s_l[16-k]===l_a[7]"、”if(t[7]&t[6]&t[5]&t[4]&t[3]&t[2]&t[1])”。

Decoder:

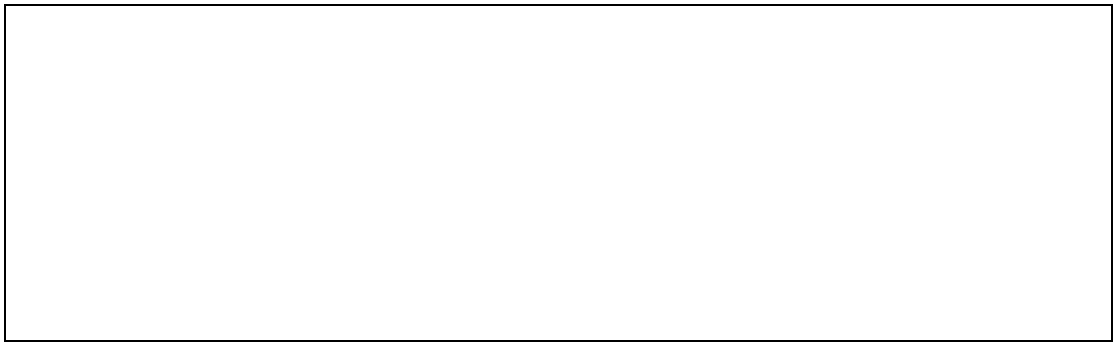
除了第一筆資料，我使用 code_len_count、code_pos_count 判斷，位元儲存的順序、次數、位置。

感想:

第三次作業難度比第二次高很多，雖然很有挑戰性，卻也很費力。如果時間充足，我覺得完成度應該會更高。但還是希望下次作業出簡單點，或給多點時間。尤其這次作業和期中考重疊，讓我這段時間每天都必須忙到晚上。

雖然我的說明很簡潔，但其實現在的做法是做過數次的改才成功的，我現在還記得我第一次把”l_a”和”s_l”的對應位元的所有結果寫出來，光這一步我就改了六次。而 Decoder 雖然和 Encoder 簡單不少，但兩者曾經因為我誤解說明，而讓我繞了不少路。

對這次作業的看法。我從這次作業學到很多東西，但也覺得不善，我目前會使用的語法不多，經驗也不足，面對複雜的作業很容易出錯。



*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element)*