Assignment: 01

Explain leach cycle with the corresponding Microprogramming. The face cycle is the initial stage of the instruction cycle, where the coverences the next instruction from memory utilizing the program country (Pc) and memory address register (MAR) and story it in the Instruction register (IR) For subsequent decoding and Execution. At the beginning of the fetch cycle 1 the address of the next instruction to be Executed in the program country (Pc) MAR MBR PC 000010110 IR AC Shept: The address is the program country is MAR PC 000010110 MBR PC 000010110 IR AC FOREDUCATIONALUSE		Ussignment , 01
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PC 0000100110 IR AC Step1: The address Pb the program (ounter t's Moved to the MAR MAR 0000100110 MBR PC 00000100110 IR AC FOR EDUCATIONAL USE	12.4	MAR
IR AC Step1: The address Pro the program (ounted 1/s) Moved to the MAR MAR 0000100110 MBR PC 00000100110 IR AC FOR EDUCATIONAL USE		MBR
AC Step1: The address Ph the program counter is Mare 0000100110 MBR PC 0000100110 IR AC FOR EDUCATIONAL USE	_	PC 0000100110
Step1: The address Pro the program counter Ps Moved to the MAR MAR 0000100110 MBR PC 00000100110 IR AC FOR EDUCATIONAL USE	7.	IR
Mared to the MAR MAR 0000100110 MBR PC 00000100110 IR AC FOR EDUCATIONAL USE		AC.
MAR 0000100110 MBR PC 00000100110 IR AC FOR EDUCATIONAL USE		Step1: The address to the program counter is
MAR 0000100110 MBR PC 00000100110 LR FOR EDUCATIONAL USE	4	The state of the s
PC 00000100110 IR FOR EDUCATIONAL USE	-)	all tell any ty is a first to
PC 00000100110 IR FOR EDUCATIONAL USE	:	MAR OUOOLOUIIO
IR FOR EDUCATIONAL USE		
TR AC FOR EDUCATIONAL USE		PC 00000100110
FOR EDUCATIONAL USE		
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ii		

	stupz: The address in the MAR Ps placed on the
-	address bus, now the control unit Pessus q
tion below to grant or the re-	READ command on the control bw. This result
	is copied to the MBR.
	MAR 0000010010
	MB6 000700007
	bc 0000001TO
-	7-
	Ac
HOTELT TO A WAY	Step 3: The Count of the MBR is moved to
	Instruction Registre (IR)
	MAR 0000010010
	MBR 0001000001
*******	bc 0000010010
Total Control of the	1R 0001000001
	Ac .)
emini Amerika (Art. Art. Art. Art. Art. Art. Art. Art.	Step4: PC Procement: Increment the pc to point
A CONTRACTOR OF THE PARTY OF TH	to the next institution's address.
STATE OF THE STATE	And the state of t
A THE REAL PROPERTY AND ADDRESS OF THE PERSON NAMED IN COLUMN TWO IN COLUMN TO THE PERSON NAMED	steps: Start Decode Eycle: Initiate the
	decoded cycle to interpet the fetched
)	d'usmutions.
,	
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67]	Explain with diagram functioning of the Micro-
	A convol unt whose benaus control values are saved as words in memory is comed Microprosgrammed control unt.
<u></u>	Mext-address (onto) Conto) Access Data
Exter	
73.3 4	
	° горы 2
	Step 1: It can Execute any Instruction - the CDU
17 14	divides Each instruction into sequential micro-
	step 2. Control signals stored for Rom Execute micro - operation by directing data flow.
	The state of the s
19.9	step3: The address of the next micro-instruction is generated for Execution.
	step 2 8 3 are repeated until all
	Mich Instructions for the instruction are Executed.
	The section of the second of t
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43]	what are the functions of the following registers?
1)	7
	Zastiag Status Registy; Indicates if the relat
	of an operation Ps 3ero, used for conditional
2]	Sp (stack point):
7	Points to the courent location in memory wed
	for the stack, which is used for temporary
len_	storage during functions (all and other operations.
3]	MAR (Memory address Register):
1 74	Hold the memory address of the data that
-	the counsed to access , acting as an pointer
	from where to read or write data.
)
4]	MDR (Memory Data Register).
	remporably sivres data being transferred to
2.1	or hum memory duing read and write
	operations.
5	y (accumulator) General purpose register)
	A genual purpose register used for storing
	data and performing calculations.
1.1	

[PD	Draw and Explain various pipe line hazards.
	when a cpu we pipelining to increase Institutions could pipeline hazards. Common types of pipe-line hazards. If smotural Hazards. It occurs when multiple immotions in the pipeline try to access the same hardware resource at the same hardware.
	For Example if both the instructions fetch stude of the memory access stage need to use the memory by simultaneously astroctured; hazard axises to the theorem of the transfer of the tran
	Resomic (lash.
	Reporting muniple instrument of the resource It the resource itself (an be pipelined)
to the second	The pipeline must stall one of the Jumilion

M Data Hazard It occurs when an ansmution depend on the result of a previous instruction that Ps SHP11 in the pipeline. Data Hazards. WAR WAW RAW write abter write. Read after write write abter read BUB, XY, X3, X6, X5 - IF ID IE ME RW. - - -BUB , XY , X3 , X5 -OR 1 x61 x31 x7 - - IF ID IC MENRO TE ID IC MEM XOR X12 1 X3, X11 - - -Data formaling morituros. The pipe-line must staw until the duta 29 available the compile can have recordy 1 nstruction to reduce data hazards. Discus various characturities of Memory. Q5] rocapion. This includes, con register & on thip code menon Inrunal. This gratudes memory that processor Sundaram

can directly acress. En RAM.
External: Thes is normally removable or virtual
Memory & access 15 510mel.
Capacity.
It is measured in turny of word size and
the no. of word a memory can store that
becomes the capacity of that memory.
unit of Hanster.
this refus to the data i.e Hangley in 1 clock
(ycle.
Access Method . [How the data of memory
(an be accensed)
L'ccess Method.
7
equential Direct Random Associative
ccecc Access access access
performance.
pulsomance of the memory depends upon its
speed of operation or data transfer rate.
physical characteristic.
The includes volatility, power consumption, erasable
& Klon Ercuable.
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Ф	e) Explain Mapping rechnique in cache.
	cuche mapping is a technique that defines how blocks hom main memory are mapped to cache lines, efficient data access by the
	1) Direct Mapping
	specified cache une.
	formula: cache line number = 1c mod n
1	K = MM Block nomber
	n = no. of Each lines
n	Suppose MM > 128 words cache > 16 words
2.45	Y T TYPE I TO THE TOTAL TO THE TOTAL TO THE TOTAL TO THE TOTAL TOTAL TO THE TOTAL TOTAL TO THE TOTAL TOTAL TO THE TOTAL TOTAL TO THE TOTAL
	TAGI LINE OFFICE WILL BO 828 LO
	3 2 2 = 130
2.07	331 831 3
7	Advantage: simple to implement.
	Disadvantage: High contlict missey.
[1]	Associative mapping.
	to any cache line.
	considering the same Example, here we don't
1	need 2-bit fox line number
laram	FOR EDUCATIONAL USE

	TAY Block
	5 2
	Advantage: Most flexible and can reduce conflict
	missey
	Disadiantage: Required complex haudwage.
	11) SET ASSOCIATIVE MAPPING.
Topa Control of the C	
	Combines the advantages of direct & so Associative
	mapping.
	The cache is divided to set and Each memory -
	Block maps to a specific set, but can -
	be placed in any line written that set.
-	TAY SET BIOUT
	3 2 2
	- + - + ~
	*