231456
SC-IT

Assignment : 01

Q1] Explain fetch cycle with the corresponding Microprogramming.

→ The fetch cycle is the initial stage of the instruction cycle, where the CPU retrieves the next instruction from memory utilizing the program counter (PC) and memory address Register (MAR) and stores it in the Instruction register (IR) for subsequent decoding and Execution.

At the beginning of the fetch cycle, the address of the next instruction to be Executed in the program counter (PC)

MAR
MBR
PC 0 0 0 0 1 0 0 1 1 0
IR
AC

Step 1: The address in the program counter is moved to the MAR

MAR 0 0 0 0 1 0 0 1 1 0
MBR
PC 0 0 0 0 0 1 0 0 1 1 0
IR
AC

Step2: The address in the MAR is placed on the address bus, now the control unit issues a READ command on the control bus. This result is copied to the MBR.

MAR	000000100010
MBR	0001000000001
PC	000000100010
IR	
AC	

Step3: The Count of the MBR is moved to Instruction Register (IR)

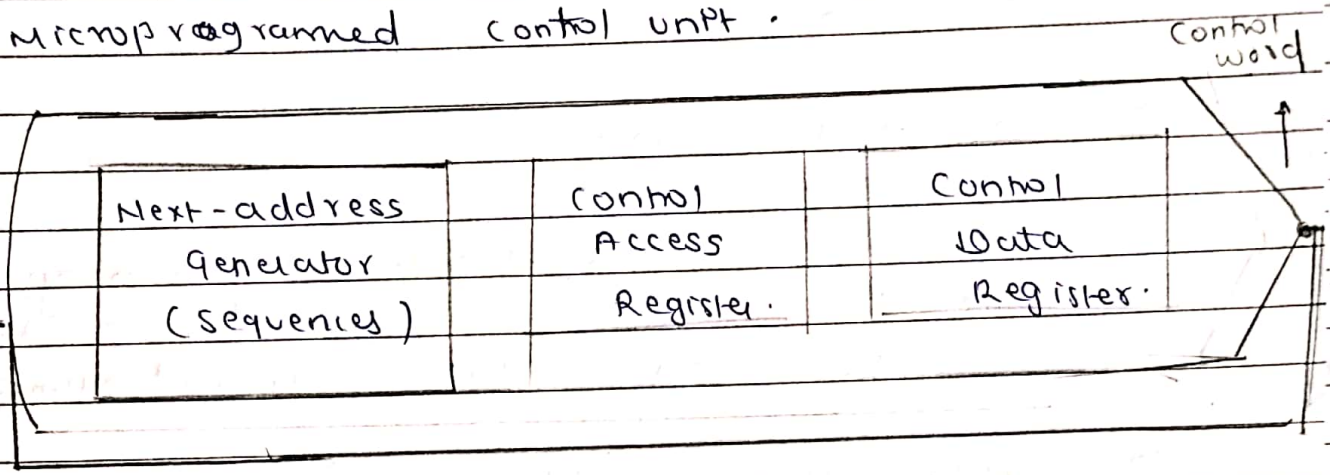
MAR	000000100010
MBR	0001000000001
PC	000000100010
IR	0001000000001
AC	

Step4: PC Increment: Increment the PC to point to the next instruction's address.

Step5: Start Decode Cycle: Initiate the decoder cycle to interpret the fetched instructions.

Q2] Explain with diagram functioning of the Micro-programmed control unit.

→ A control unit whose binary control values are saved as words in memory is called Microprogrammed control unit.



Steps:

Step 1: It can Execute any instruction. The CPU divides each instruction into sequential micro-operations called micro-instructions.

Step 2: Control signals stored in ROM Execute micro-operation by directing data flow.

Step 3: The address of the next micro-instruction is Generated for Execution.

Step 4: Step 2 & 3 are repeated until all Micro-Instructions for the instruction are Executed.

Q3] What are the functions of the following registers?

1] Z

Zero flag / Status Register : Indicates if the result of an operation is zero, used for conditional Execution.

2] SP (stack point):

Points to the current location in memory used for the stack, which is used for temporary storage during functions calls and other operations.

3] MAR (Memory address Register):

Hold the memory address of the data that the CPU need to access, acting as an pointer from where to read or write data.

4] MDR (Memory Data Register).

Temporarily stores data being transferred to or from memory during read and write operations.

5] Y (accumulator / General purpose Register)

A General purpose register used for storing data and peforming calculations.

Q4] Draw and Explain various pipeline hazards.

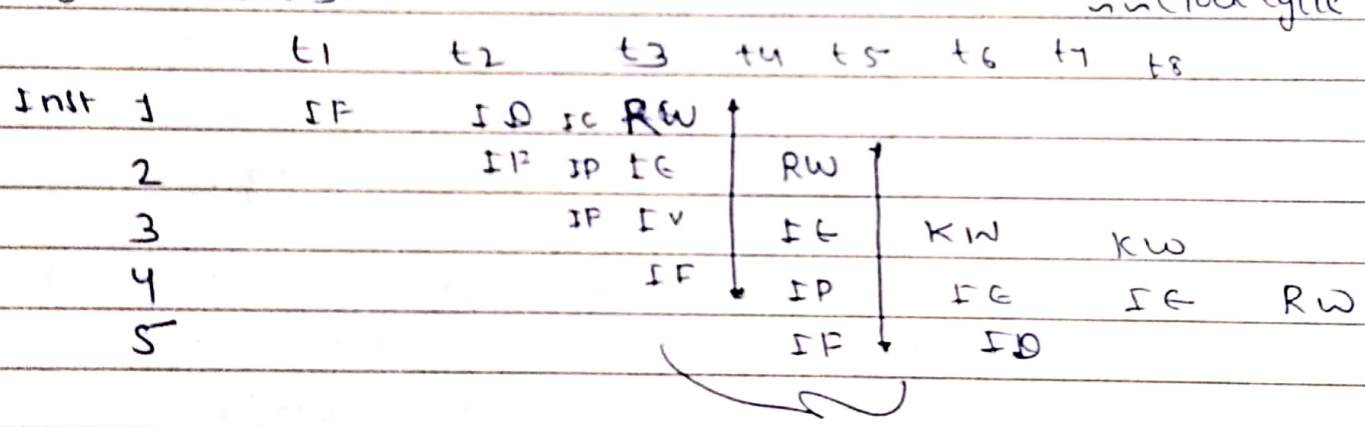
→ when a CPU uses pipelining to increase instruction throughout it can encounter situations called pipeline hazards.

common types of pipe-line hazards.

1] Structural Hazards.

It occurs when multiple instructions in the pipeline try to access the same hardware resource at the same time.

2] For Example if both the instructions fetch stage & the memory access stage need to use the memory bus. simultaneously a structural hazard arises



Solution:

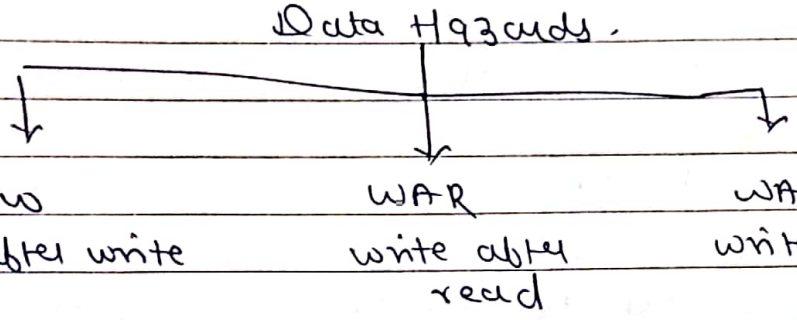
Providing multiple instances of the resource

If the resource itself can be pipelined

The pipeline must stall one of the instruction

iii] Data Hazards

It occurs when an instruction depend on the result of a previous instruction that is still in the pipeline.



ADD X3, X6, X5	IF	t1	t2	t3	t4	t5	t6	t7	t8	t9
SUB, X4, X3, X5	-	ID IF	IE ID	ME IE	RW ME	- RW	- -	- -	- -	- -
OR, X6, X3, X7	-	-	IF	ID	IE	ME	RW	-	-	-
AND X6, X3, X9	-	-	-	IF	ID	IE	ME	RW	-	-
XOR X12, X3, X11	-	-	-	-	IF	ID	IE	ME	RW	

Data forwarding.

Solution:

The pipe-line must stall until the data is available the compile can have recorded instruction to reduce data hazards.

Q5] Discuss various characteristics of memory.

i] Location.

This includes, CPU registers & on chip code memory Internal. This includes memory that processor

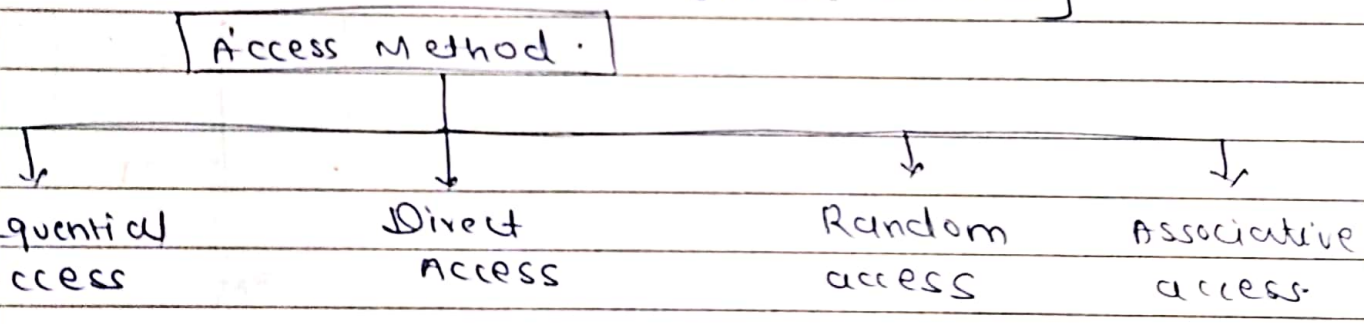
can directly access. Ex RAM.

External: This is normally removable or virtual Memory & access is slower.

2] Capacity.
It is measured in terms of word size and the no. of word a memory can store that becomes the capacity of that memory.

3] unit of transfer.
this refers to the data i.e transfer in 1 clock cycle.

4] Access Method. [How the data of memory can be accessed]



5] performance.
performance of the memory depends upon its speed of operation or data transfer rate.

6] physical characteristic:
This includes volatility, power consumption, erasable & Non Erasable.

Q6] Explain Mapping Technique in cache.

cache mapping is a technique that defines how blocks from main memory are mapped to cache lines, efficient data access by the CPU.

i] Direct Mapping

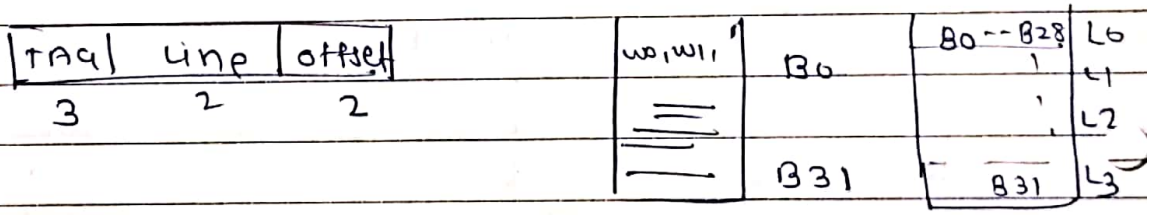
Each main memory block is mapped to a specified cache line.

formula: cache line number = k mod n

k = MM Block number

n = no. of Each lines

Suppose MM → 128 words cache → 16 words



Advantage: simple to implement.

Disadvantage: High Conflict misses.

ii] Associative mapping.

Any main memory block can be mapped to any cache line.

considering the same Example, here we do not need 2-bit for Line number

TAG	Block offset
5	2

Advantage: Most flexible and can reduce conflict misses

Disadvantage: Required complex hardware.

iii] SET ASSOCIATIVE MAPPING.

Combines the advantages of direct & Associative mapping.

The cache is divided to sets and Each memory Block maps to a specific set, but can be placed in any line written that set.

TAG	SET	Block
3	2	2