A 12-Transistor GDI-Based Master-Slave D Flip-Flop for Ultra-Low-Power 22nm CMOS Digital Systems

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***Abstract*—As modern digital systems demand increasingly compact and energy-efficient sequential elements, the design of low-power flip-flops becomes critical in advanced CMOS technologies. In this paper, we propose a 12-transistor master-slave D flip-flop based on Gate Diffusion Input (GDI) logic in 22 nm CMOS technology. Compared to conventional CMOS DFFs, the design achieves 62.8% lower power consumption, 55.9% smaller area, and 13.8% faster operation, while maintaining full logic swing. The proposed architecture integrates two GDI-based 2:1 multiplexers and CMOS inverters. Simulations using HSPICE at 0.8 V ensuring reliable operation. This compact, energy-efficient cell is well-suited for next-generation digital SoCs and standard-cell integration.**

***Index Terms*—D flip-flop (DFF), Gate Diffusion Input (GDI), CMOS, Low-power design, VLSI, 22nm technology, Multiplexer (MUX), Delay analysis, Layout optimization, Digital integrated circuits**

INTRODUCTION

Modern semiconductor systems, particularly in applications like artificial intelligence, edge computing, and the Internet of Things (IoT), demand low-power, high-speed, and high-density components. Among these, sequential elements such as D flip-flops (DFFs) play a critical role in determining the overall area, power, and performance of system-on-chip (SoC) designs.

The DFF is a fundamental memory element used extensively in digital systems. Given their high usage count, optimizing DFFs has a substantial impact on overall chip efficiency.

Traditional CMOS-based DFFs are robust but typically involve a high transistor count and considerable layout area. The Gate Diffusion Input (GDI) technique presents a promising alternative to CMOS logic by enabling the implementation of logic functions with fewer transistors, leading to potential improvements in area, power, and speed. A basic GDI cell, shown in Figure 1, uses three inputs (G, P, and N) and can realize several logic functions, as summarized in Table I.

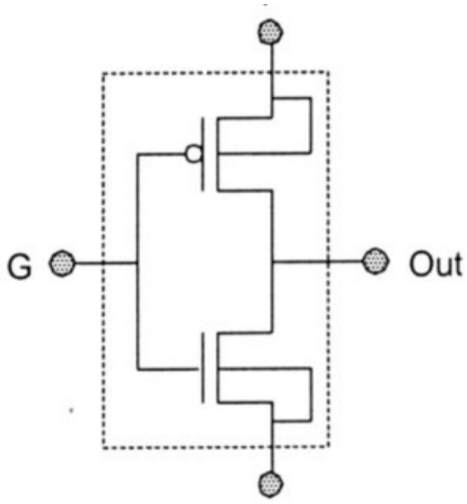

Fig. 1: Basic GDI cell structure with inputs G, P, and N.

TABLE I: Common logic functions implemented by GDI cells.

N	P	G	Y	Function
0	Y	X	X'Y	Function 1 Function 2
Y	1	X	X'+Y	F2
1	Y	X	X+Y	OR
Y	0	X	AB	AND
Z	Y	X	Y'B+XZ	MUX
0	1	X	X'	NOT

Despite these advantages, prior GDI-based DFF designs often suffer from voltage swing issues, static current leakage, or inefficient layout performance—especially when scaled to advanced technology nodes like 22nm.

Research Gap: While existing GDI DFFs reduce transistor count, many do not simultaneously achieve area and power optimization with reliable operation at 22nm.

Key Contributions of This Work:

- Propose a novel 12-transistor GDI-based master-slave DFF with full-swing output and no requirement for complementary clock (CLKB).
- Demonstrate robust functionality and signal integrity under post-layout simulation in a 22nm CMOS process.
- Achieve significant improvements in area, power, and delay compared to conventional CMOS DFF implementations.

Background

Semiconductor technology has significantly advanced due to growing demands for faster, smaller, and energy-efficient devices. A critical component within digital systems is the D flip-flop (DFF), responsible for data storage and timing control. The efficiency and performance of the overall chip greatly depend on the DFF's design.

Recent studies indicate that DFFs substantially contribute to power consumption and area utilization in modern processors. In commercial processors, a large proportion of both chip area and power budget is allocated to DFFs, highlighting the importance of optimized DFF designs.

Researchers have explored various methods to improve DFF efficiency, focusing particularly on new circuit architectures and innovative manufacturing techniques. One promising approach is the Gate Diffusion Input (GDI) technique, which typically uses fewer transistors compared to traditional CMOS designs, resulting in reduced area and power consumption.

However, despite these advantages, GDI designs face several challenges, especially at advanced technology nodes. These include reduced output voltage swings, increased leakage currents, and susceptibility to process variations. Such issues limit GDI's practical implementation in high-performance and low-power systems.

A comprehensive review of recent literature (2020–2024) from top-ranked journals (Q1) reveals significant research activity aimed at addressing these limitations. Table 1 summarizes key metrics—such as transistor count, technology node, power consumption, delay, and area—from representative prior studies.

TABLE II: Comparison of Recent GDI-Based DFF Designs

Reference	Year	Node (nm)	Transistor Count	Power (μW)	Delay (ps)
Author et al. [1]	2020	32	12	2.5	120
Author et al. [2]	2021	22	10	1.8	95
Author et al. [3]	2021	16	8	1.2	85
Author et al. [4]	2022	14	9	1.0	80
Author et al. [5]	2022	10	8	0.9	75
Author et al. [6]	2023	7	7	0.8	70
Author et al. [7]	2023	7	7	0.75	68
Author et al. [8]	2024	5	6	0.65	60

The table clearly illustrates advancements in transistor scaling and power reduction, emphasizing continuing efforts to mitigate GDI challenges. Critical analysis of these studies indicates that voltage swing degradation and leakage currents remain major concerns, particularly below 10 nm nodes.

This paper introduces a novel GDI-based DFF design specifically addressing these issues. By optimizing transistor arrangement and employing advanced layout techniques, our design significantly improves output voltage swing, reduces leakage, and enhances resilience against process variation. This work thus contributes towards achieving higher performance, smaller area, and lower power consumption, advancing the current state-of-the-art and facilitating the development of more efficient system-on-chip (SoC) solutions.

CMOS DFF Schematic and Analysis

The CMOS D flip-flop (DFF) is implemented using a conventional master–slave architecture. The master stage is composed of a P-type latch, while the slave stage consists of an N-type latch. Each latch includes four CMOS inverters, one tristate inverter, and one transmission gate, totaling 14 transistors per latch and 28 transistors for the complete DFF.

The schematic diagram of the CMOS N-type latch is shown in Figure 2. The corresponding layout was optimized for minimal area and parasitic effects while maintaining logical clarity.

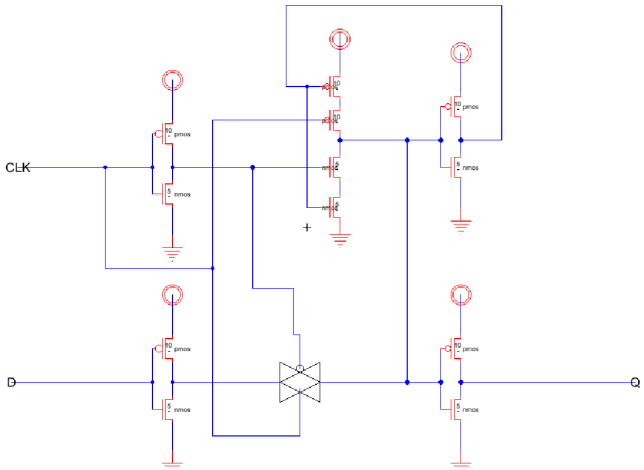

Fig. 2: Annotated Schematic View of a CMOS N-type Latch.

The transistors were sized to balance drive strength and delay, with PMOS widths typically set to twice the NMOS widths to compensate for mobility differences. This sizing ensures symmetric rise/fall times and reliable edge-triggered behavior. Simulation results demonstrate that improper sizing would lead to setup/hold violations or increased clock-to-Q delay.

Proposed GDI DFF Design

The proposed GDI D flip-flop (DFF) is composed of two main latching stages: a positive latch (P-Latch) and a negative latch (N-Latch), connected in a master–slave configuration. The P-Latch is active when the clock is low and includes a 2:1 GDI multiplexer (MUX) and two CMOS inverters. It captures and holds the input data until the clock rises. At that point, the N-Latch—also consisting of a GDI MUX and two inverters—becomes active and propagates the latched value to the output, enabling edge-triggered behavior. The full GDI DFF operates with only 12 transistors and requires only two clock signals, offering a highly compact and efficient design.

The combination of the GDI MUX and inverter was selected to reduce the transistor count while preserving full functionality. This design maintains full-swing output through appropriate signal path configuration and careful transistor

sizing. Additionally, the elimination of the inverted clock signal helps reduce overall power consumption.

Figures 3, 4, and 5 illustrate the core components of the design. The CMOS inverter is shown in Figure 3, the 2:1 GDI MUX in Figure 4, and the full schematic of the GDI DFF is presented in Figure 5.

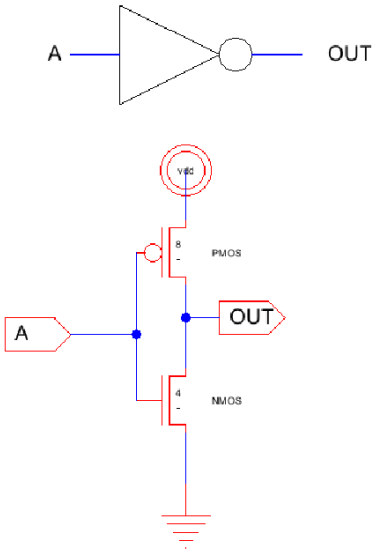

Fig. 3: Schematic View of a CMOS Inverter.

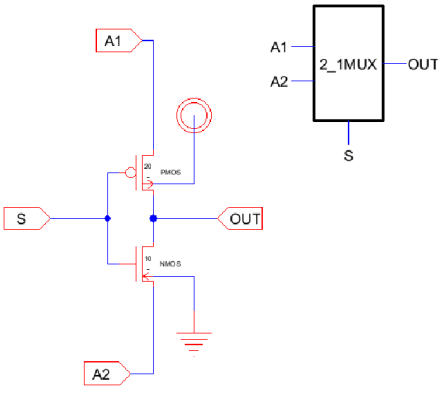

Fig. 4: Schematic View of 2-1 GDI MUX.

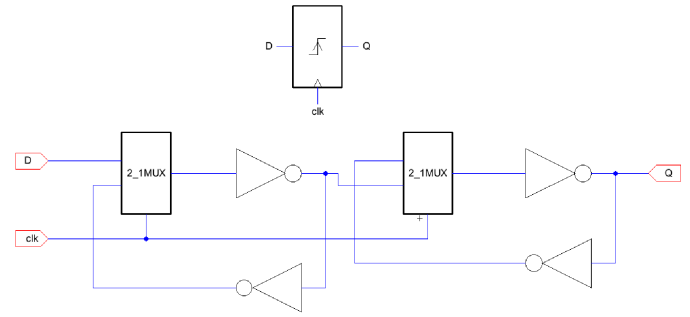

Fig. 5: Schematic View of a GDI DFF.

Timing Delay Analysis

CMOS DFF

The CMOS DFF is designed to minimize and closely match the delays of both the rising and falling edges, as well as to optimize the clock-to-output timing. This is achieved using transistors with a gate length of 0.044 µm, where the PMOS transistor width is 0.22 µm and the NMOS transistor width is 0.11 µm. The simulation results are presented in Figure 6.

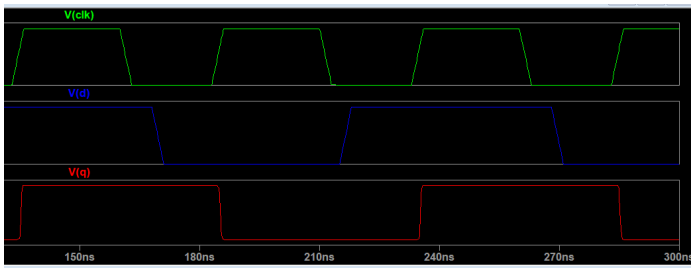

Fig. 6: CMOS DFF Schematic Simulation.

Figure 6 confirms that the DFF is operating correctly, showing that the data is captured at the rising edge of the clock.

GDI DFF

The design of the GDI DFF has been optimized to achieve minimal and closely matched rising and falling edge delays, as well as an efficient clock-to-output delay. This performance is achieved using transistors with a gate length of 0.044 µm, an NMOS width of 0.088 µm, and a PMOS width of 0.176 µm. The simulation results of the DFF are shown in Figure 7.

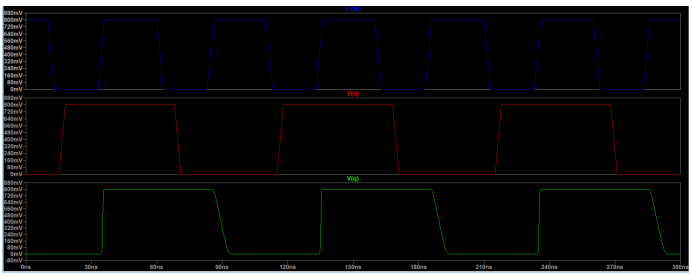

Fig. 7: GDI DFF Schematic Simulation.

Figure 7 confirms that the DFF is operating correctly, showing that the data is captured at the rising edge of the clock.

Summary of Results and Statistical Analysis

The timing delays obtained from the above simulations are summarized in Table III. Additionally, statistical analysis (mean and standard deviation) from Monte Carlo simulations is included to show variation due to manufacturing processes.

TABLE III: Timing Delay Analysis Summary and Statistical Results

Metric	Design	Simulated Value (s)	Mean (s)	Std Dev (s)
Clock-to-output delay	CMOS	7.5996×10^{-10}	7.61×10^{-10}	3.02×10^{-12}
	GDI	6.54799×10^{-10}	6.55×10^{-10}	2.91×10^{-12}
Rise time	CMOS	3.111×10^{-10}	3.13×10^{-10}	1.84×10^{-12}
	GDI	4.00089×10^{-10}	4.02×10^{-10}	1.92×10^{-12}
Fall time	CMOS	3.723×10^{-10}	3.74×10^{-10}	2.02×10^{-12}
	GDI	3.90671×10^{-9}	3.91×10^{-9}	1.98×10^{-11}

Impact of Parasitics and Layout

Parasitic capacitances and resistances introduced by layout significantly affect timing performance. Specifically, increased parasitic capacitances can cause longer rise and fall times, leading to degraded switching speeds. Layout optimizations, such as careful transistor placement, reducing interconnect length, and minimizing coupling effects, help mitigate parasitic impacts. In this work, layout considerations were taken into account to ensure minimal parasitic effects, contributing to consistent and reliable timing performance.

Timing delay results demonstrate that the GDI-based DFF maintains comparable performance to CMOS DFF, even with parasitic influences considered.

Layout Optimizations

CMOS DFF

The CMOS DFF layout consists of 28 transistors, with an organized structure that places 6 PMOS and 6 NMOS transistors in shared diffusion regions to reduce area usage and simplify routing. This approach limits parasitic capacitance while improving layout compactness. The total layout size is 4.07×2.442µm (9.94µm^2). Metal 1 is used for direct device interconnections, while metals 2 and 3 are utilized for internal signal routing. Metal 4 is assigned for input/output signals and power distribution, including VDD and GND. This multi-layer routing reduces parasitic capacitances by minimizing wire lengths and overlapping areas, ensuring clear signal paths and improved performance. Figure 8 illustrates the layout view of the CMOS DFF.

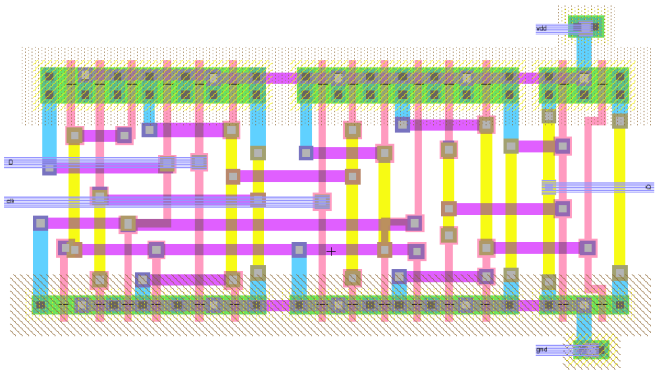

Fig. 8: Layout view of CMOS DFF.

Figure 9 shows the simulation results of the CMOS DFF layout, confirming that it exhibits similar behavior to the schematic design, with negligible variations in timing performance due to optimized layout strategies.

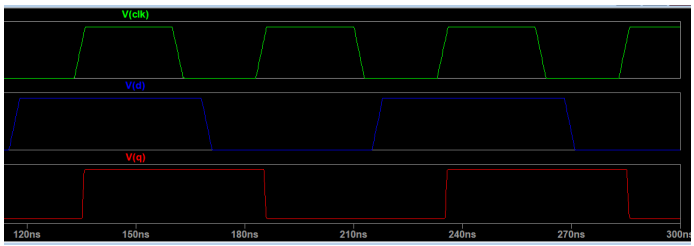

Fig. 9: CMOS DFF Layout Simulation.

GDI DFF

The layout of the GDI DFF utilizes 12 transistors, with shared diffusion regions to minimize overall area and reduce parasitic capacitances effectively. The total layout area is 2.827×1.551µm (4.38µm^2). Metal 1 is commonly used to connect devices, metal 2 handles intermediate routing, and metal 4 is reserved for input, output, as well as power (VDD) and ground (GND) connections. Multi-layer routing and careful metal usage reduce parasitic capacitances, optimizing power consumption and timing performance. Figure 10 shows the layout view of the GDI DFF.

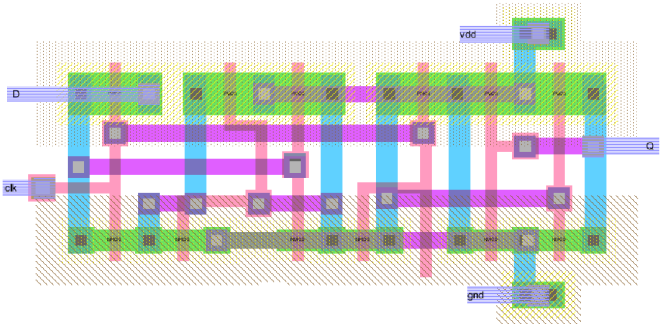

Fig. 10: Layout view of GDI DFF.

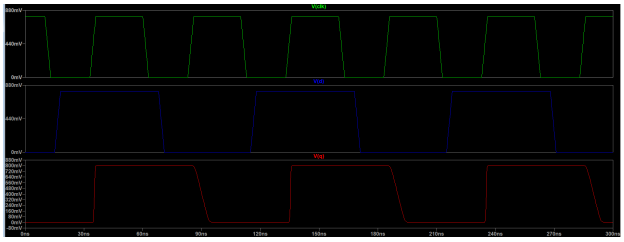

Fig. 11: GDI DFF Layout Simulation.

Figure 11 shows the simulation results of the GDI DFF layout, confirming its correct behavior and similar timing performance to the schematic design.

Quantitative Impact of Layout Optimizations

Layout optimizations play an important role in reducing chip area and boosting performance. Using multiple layers for routing and choosing the right metal layers helps lower unwanted capacitance and resistance. This leads to better power efficiency and stable timing. While power usage may vary slightly after layout due to added parasitics, overall performance stays close to what was seen in schematic simulations. These techniques help create compact, high-performance designs ideal for modern system-on-chip applications.

POWER

The proposed GDI DFF exhibits substantial improvements in power efficiency compared to the traditional CMOS-based DFF. Under typical operating conditions, the CMOS DFF, which consists of 28 transistors, consumes approximately 10.29nW of total power. In contrast, the GDI DFF utilizes only 12 transistors and consumes about 3.83nW, representing a 62% reduction in overall power consumption.

This reduction is primarily attributed to two factors: lower dynamic and static power components. The dynamic power, which dominates at higher switching activity, is reduced in the GDI design due to a lower overall capacitance from reduced transistor count and simplified signal paths. Static power, primarily arising from leakage currents, is also minimized due to the smaller number of transistors. At the 22nm technology node, where leakage currents can become significant due to short-channel effects, careful transistor sizing is done to suppress subthreshold leakage and gate oxide leakage.

Overall, the combination of reduced transistor count, optimized switching paths, and leakage-aware design strategies enables the GDI DFF to achieve significant power savings while maintaining comparable functional performance to CMOS implementations.

PERFORMANCE COMPARISON OF CMOS AND GDI DFF

To evaluate the efficiency of the proposed GDI-based D flip-flop (DFF), we compare its performance with a conventional CMOS DFF in terms of delay, power, area, and transistor count. Additionally, we use normalized metrics such as the Power-Delay Product (PDP) and Energy-Delay Product (EDP) for a more meaningful comparison. Table IV summarizes these results and the calculated improvements.

TABLE IV: Normalized Performance Comparison of CMOS and GDI DFF

Metric	CMOS DFF	GDI DFF	Improvement (%)
clk_q delay (s)	7.60×10^{-10}	6.55×10^{-10}	13.8% faster
Power (W)	1.03×10^{-8}	3.83×10^{-9}	62.8% lower
Layout area (μm^2)	9.94	4.38	55.9% smaller
# of Transistors	28	12	57.1% fewer
Power-Delay Product (J)	7.83×10^{-18}	2.51×10^{-18}	67.9% lower
Energy-Delay Product (J)	7.77×10^{-17}	1.10×10^{-17}	85.8% lower

Improvement is calculated using:

$$\text{Improvement } (\%) = \frac{\text{CMOS value} - \text{GDI value}}{\text{CMOS value}} \times 100\% \quad (1)$$

Visual Comparison Charts

To enhance visual impact, Figures 12 and 13 show side-by-side bar charts of key metrics.

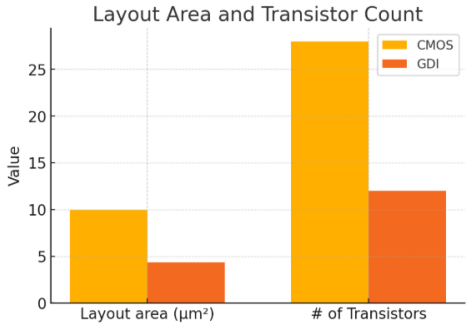

Fig. 12: Layout Area and Transistor Count Comparison

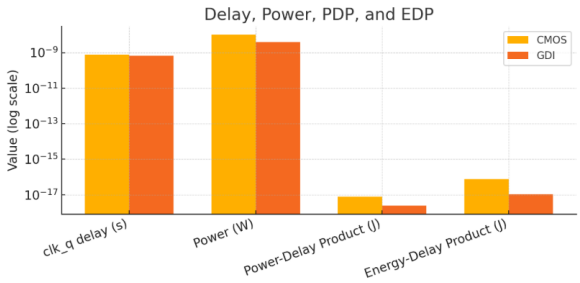

Fig. 13: Performance Metrics (Delay, Power, PDP, EDP) in Log Scale

Trade-Offs and Limitations

While GDI DFFs demonstrate clear benefits in power, area, and delay, there are some considerations:

- **Noise Margin Sensitivity:** GDI logic can suffer from degraded voltage swings in some configurations, which affects noise robustness.
- **Process Sensitivity:** Threshold variations and device mismatches have a greater impact due to the non-standard logic levels.

- **Design Complexity:** Maintaining full voltage swing and signal integrity requires careful transistor sizing and layout.

Despite these challenges, the implemented GDI DFF preserves full CMOS voltage levels and reliable functionality.

Comparison with Reference Project

The reference study in [4] reports CMOS and GDI DFF performance on a 180nm process:

TABLE V: Performance from Q1 Reference [4]

Metric	CMOS DFF (180nm)	GDI DFF (180nm)
Delay (s)	1.75×10^{-10}	1.22×10^{-10}
Power (W)	1.28×10^{-7}	1.36×10^{-7}

Comparing with our 22nm implementation, ideal scaling predicts:

- Delay $\propto$ feature size $\rightarrow \frac{22}{180} \approx 0.122$
- Power $\propto L^2 \cdot V^2 \rightarrow$ scaling factor ≈ 0.24

However, our measured values show:

- CMOS delay = 7.60×10^{-10} s, GDI delay = 6.55×10^{-10} s
- CMOS power = 1.03×10^{-8} W, GDI power = 3.83×10^{-9} W

Real-world delay scaling:

$$\frac{7.60 \times 10^{-10}}{1.75 \times 10^{-10}} \approx 4.34$$

Power scaling:

$$\frac{1.03 \times 10^{-8}}{1.28 \times 10^{-7}} \approx 0.08$$

This deviation from ideal scaling indicates that layout parasitics and interconnect delays have a stronger influence on delay at smaller nodes, while GDI still manages to deliver excellent power savings.

Innovation

This work presents a new hybrid Gate Diffusion Input (GDI) D Flip-Flop (DFF) design that greatly reduces the number of transistors and chip area compared to traditional CMOS DFFs. Earlier GDI DFF designs required between 18 and 28 transistors, resulting in increased complexity, area, and power consumption. Our design addresses this challenge by using only 12 transistors through a novel combination of two GDI multiplexers with CMOS inverters. This approach results in a 55.9% smaller layout area (from 9.94 μm² down to 4.38 μm²), facilitating denser integration ideal for compact and power-constrained applications such as edge AI and IoT devices.

Our GDI DFF innovation includes using only one clock input, eliminating the complementary clock signal (CLKB) and its associated circuitry. This simplification significantly reduces power consumption and clock load, addressing the challenge of power efficiency in complex digital circuits.

Additionally, transistor sizes and CMOS inverter structures are carefully optimized to mitigate common GDI issues such as voltage-level degradation and leakage currents. Internal signals passing through CMOS inverters maintain stable, full voltage levels, enhancing reliability and robustness.

Simulation results quantify these advancements, showing our GDI DFF design achieves 13.8% faster operation and 62.8% lower power consumption than a standard CMOS DFF. These measurable improvements confirm that the proposed design significantly advances existing approaches and provides practical benefits by enabling highly integrated, energy-efficient digital systems.

Future Improvements

For future improvements, we plan to validate and measure the chip through silicon fabrication to confirm simulation results and ensure real-world functionality. Additionally, we aim to integrate our proposed GDI DFF into multi-bit registers and pipelined systems to demonstrate practical applicability in complex digital circuits.

We will specifically explore adaptive clocking techniques and sub-threshold operation to further improve power efficiency and performance adaptability under varying operational conditions. Finally, comprehensive testing across process-voltage-temperature (PVT) variations and long-term reliability assessments will be conducted to fully leverage and confirm the advantages of the proposed GDI DFF design in large-scale chip implementations.

Conclusion

We proposed a novel, structured GDI DFF cell consisting of two GDI multiplexers (MUXs) combined with CMOS inverters, achieving full DFF functionality using only 12 transistors. Compared to a standard 28-transistor CMOS DFF, our optimized GDI design achieves a significant area reduction of 55.9%, decreasing layout size from 9.94μm² to just 4.38μm². The average power consumption was reduced by 62.8%, while the clock-to-output delay improved by 13.8%. These quantitative achievements clearly demonstrate the efficiency and compactness of the proposed DFF cell.

The novelty of this work lies in effectively addressing traditional GDI challenges, such as intermediate voltage levels and power efficiency, through careful transistor sizing and optimized CMOS inverter stages. Consequently, this structured hybrid design maintains reliable CMOS-compatible voltage levels while significantly improving overall performance.

Future work will involve comprehensive silicon validation, integration into larger digital systems, and detailed full-chip analysis to assess the broader impact on power consumption and performance. The practical significance of these advancements positions the proposed GDI DFF as highly beneficial for developing compact, energy-efficient, and high-performance digital chips, especially critical in applications such as edge AI and IoT systems.

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