**Ic Project Second semester 2024-2025**

This project aims to **design, simulate, and analyze a highly efficient, low-power master-slave D flip-flop using Gate Diffusion Input (GDI) logic, implemented in a 32nm (or smaller )CMOS** process. The design leverages the GDI technique to minimize transistor count, reduce power consumption, and decrease propagation delay compared to conventional CMOS flip-flops.

**Objectives:**

* Develop a transistor-level schematic of a GDI-based master-slave D flip-flop.
* Implement the design using Electric EDA -Electric tools and simulate its performance with LTspice.
* Compare the GDI design’s power, delay, and area with a standard CMOS flip-flop.
* Explore adaptive clock generation and body biasing for further power savings.
* Prepare a technical report and presentation summarizing the design process, simulation results, and comparative analysis.

**Expected Outcomes:**

* A validated schematic and layout of the GDI D flip-flop in Electric EDA.
* Simulation waveforms, power, and delay measurements.
* Comparative charts and tables highlighting improvements over CMOS.
* A final report and presentation suitable for IEEE journal submission or academic assessment.

**Project Timeline**

| **Week / Date** | **Task Description** |
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| **Week 1 (May 13–19)** | Literature review, finalize specifications, initial schematic entry in Electric. |
| **Week 2 (May 20–26)** | Complete transistor-level schematic for GDI latch and flip-flop. Start simulation setup in LTspice. |
| **Week 3 (May 27–Jun 2)** | Run functional and performance simulations (power, delay). Begin layout in Electric. |
| **Week 4 (Jun 3–8)** | Finalize layout, perform DRC/LVS checks, extract parasitics. Run post-layout simulations. |
| **June 9–10 (Mon–Tue)** | Prepare comparative analysis, charts, and tables. Draft report and presentation slides. |
| **June 11 (Wed)** | Final review of report and presentation. Peer feedback and revisions. |
| **June 12 (Thu)** | **Submit final report and deliver project presentation.** |

**Deliverables**

* **Transistor-level schematic and layout files** (Electric EDA)
* **Simulation files and results** (LTspice)
* **Comparative analysis** (charts/tables)
* **Final written report** (PDF/Word)
* **Presentation slides** (PowerPoint/PDF)

**Milestone Summary**

* **Schematic and simulation complete:** May 26
* **Layout and verification complete:** June 8
* **Draft report and slides:** June 10
* **Final submission and presentation:** **Thursday, June 12**