DSD Special Project Homework 03 Report

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1. Simulated timing (ns)
   Gate-level simulation clock cycle: 10
2. Area (um^2)
   Total cell area: 13584.292415
3. Cost (A*T)
   135842.92415
4. Screen shot

```
Number of ports:                         1772
Number of nets:                          2842
Number of cells:                         1100
Number of combinational cells:            933
Number of sequential cells:                44
Number of macros/black boxes:               0
Number of buf/inv:                        259
Number of references:                      19

Combinational area:              12455.521384
Buf/Inv area:                     2053.854044
Noncombinational area:            1128.771030
Macro/Black Box area:                0.000000
Net Interconnect area:          118813.925720

Total cell area:                 13584.292415
Total area:                     132398.218135
```

```
Inferred memory devices in process
        in routine PC line 158 in file
                '/home/raid7_2/userb09/b9502138/HW3/RISCV/verilog/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|     pc_out_reg      | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================
```