CS-505 Advanced Computer Architecture

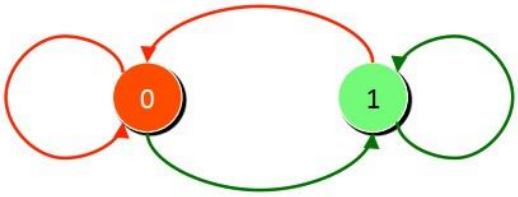
Quiz 3 (Solution) Total Time: 60 Mints

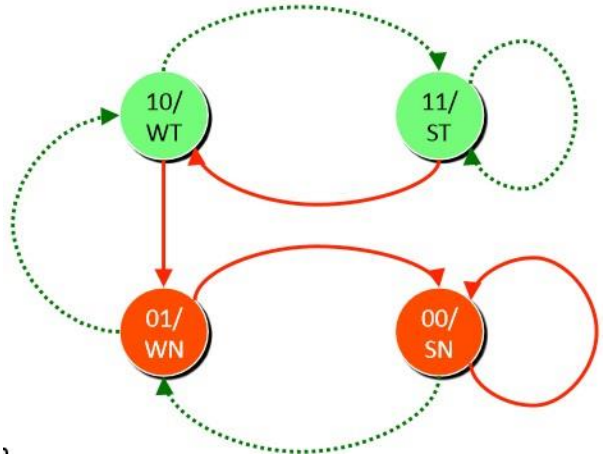
Name: _____ Registration#: _____

Question#/ Total Marks	Q1 (10)	Q2 (2+4+4=10)	Q3 (5+5=10)	Total (30)
Obtain Marks				

Question 1: (10 Marks)

We have a program core consisting of four conditional branches B1, B2, B3 & B4. Below are the actual outcomes of each branch for one execution of the program core (T for taken and NT for not taken). Write the predictions and calculate the accuracies for each of the following branch prediction schemes and fill the below table:





Branch Name		Predictions	CP	FP	PA	Predictor Type	Initial Condition
B1	T-T-T-NT-NT-NT-T-NT	T-T-T-T-NT-NT-NT-T	5	3	62.5%	1 bit	PT
B2	T-NT-T-NT-T-NT-T-NT	T-T-NT-T-NT-T-NT-T	1	7	12.5%	1 bit	PT
B3	NT-NT-T-T-NT-NT-T-T	NT-NT-NT-T-T-NT-NT-T	5	3	62.5%	1 bit	PN
B4	T-NT-T-NT-T-NT-T-NT	NT-T-NT-T-NT-T-NT-T	0	8	0%	1 bit	PN
B1	T-T-T-NT-NT-NT-T-NT	WT-ST-ST-ST-WT-WN-SN-WN	5	3	62.5%	2 bit	WT
B2	T-NT-T-NT-T-NT-T-NT	WT-ST-WT-ST-WT-ST-WT-ST	4	4	50%	2 bit	WT
B3	NT-NT-T-T-NT-NT-T-T	WN-SN-SN-WN-WT-WN-SN-WN	3	5	34.5%	2 bit	WN
B4	T-NT-T-NT-T-NT-T-NT	WN-WT-WN-WT-WN-WT-WN-WT	0	8	0%	2 bit	WN

* PT = Predict taken, PN = Predict not taken, WT = Weakly taken, WN = Weakly not taken

* CP = Correct prediction, FP = False prediction, PA = Prediction accuracy

Solution Registration#: _____

Question 2: (2+4+4=10 Marks)

a) Find the AMAT for a processor with a 1 ns clock cycle time, a miss penalty of 20 clock cycles, a miss rate of 0.05 misses per instruction, and a cache access time (including hit detection) of 1 clock cycle. Assume that the read and write miss penalties are the same and ignore write stalls

$$\text{Total Cycles} = \text{Cache Access Time} + \text{Miss Rate} \times \text{Miss Penelty}$$

$$\text{Total Cycles} = 1 + 0.05 \times 20$$

$$\text{Total Cycles} = 1 + 1$$

$$\text{Total Cycles} = 2 \text{ Cycles}$$

$$\text{AMAT} = 2 \times 1\text{ns} = 2\text{ns}$$

b) The average memory access time for a microprocessor with 1 level of cache in 2.4 clock cycles
(AMAT = Hit Time + Miss Rate × Miss Penalty)

− Hit time for L1 cache is 1 clock cycle

− Miss penalty for L1 is 80 Clock cycles if data is not present in L1

1. Calculate Miss Rate for L1?
2. Now if we want to improve the average memory access time to obtain a 65% speedup then what would be the new value of AMAT?

We must first determine the miss rate of the L1 cache to use in the revised AMAT formula:

AMAT = Hit Time + Miss Rate x Miss Penalty

2.4 = 1 + Miss Rate x 80 Miss Rate = 1.75%

Next, we can calculate the target AMAT … i.e. AMAT

Speedup = Time (old) / Time (new)

1+65 = 2.4 / Time (new)

Time (new) = 1.4545 clock cycles

c) How many bits are in the (1,2) branch predictor with 2K entries? How many entries are in a (3,3) predictor with the same number of bits?

$$Predictor\ Bits = 2^1 \times 2 \times 2K = 8K\ bits$$

$$2^3 \times 3 \times Number\ of\ prediction\ entries\ selected\ by\ the\ branch = 8K\ bits$$

$$Number\ of\ prediction\ entries\ selected\ by\ the\ branch = \frac{8K}{8 \times 3} = \frac{1}{3}K$$

Question 3: (5+5=10 Marks)

a) Assume there is a small two-way set-associative cache consisting of four one-word blocks. Find the number of HIT/MISS for cache organization given the following sequence of block addresses: 0, 8, 0, 6, and 8. **you can make assumptions if required!**

Sr #	Block Address	Hit/Miss	Cache block 0	Cache block 1	Cache block 2	Cache block 3
1	0	Miss	0			
2	8	Miss	0	8		
3	0	Hit	0	8		
4	6	Miss	0	6		
5	8	Miss	8	6		

b) Instruction:
Assume hardware forwarding for all parts.
Each stages of pipeline takes one cycle (IF, ID,EX,MEM,WB).

Fill the given table by rewriting/rescheduling the instructions to reduce stalls and delay slot (to finish in minimum cycles) without creating any additional data/control hazard.

1. ADDi V0, V0, 1 #add
2. ADDi T1, A0, 4 #add
3. LW T0, 0(T1) #load
4. ADDi A0, T0, A1 #add
5. ADDi A0, A0, 4 #add
6. BE T0, F0, Loop #branch
7. Delay Slot
8. JR FINISH #jump instruction to finish code

Sr	Instructions
1	2
2	3
3	1
4	4
5	6
6	5
7	8
8	
9	
10	