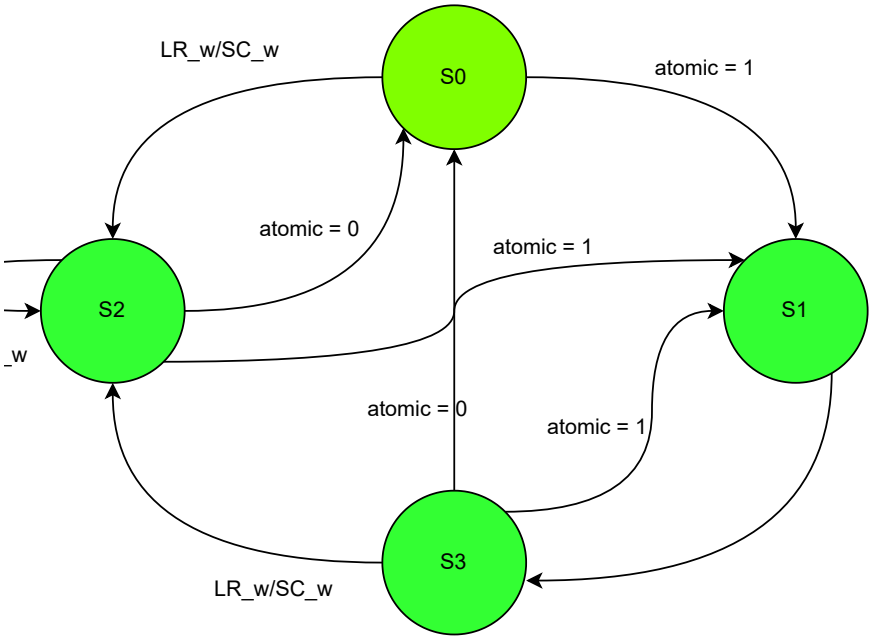
LR_w/SC_



In this FSM whenever atomic load/store instructions comes it will go to state 2
For remaining atomic instructions it will go to state 1 and stall will be generated then it will go to state 2 always without any conditions.

state01: In this state it will generate some of the signals like in this state it will read the memory

state02: In this state it will generate the remaining signals to complete the atomic instruction like it will calculate the result of the memory out and register value and write the results back to memory and register file according to instruction.