

Final project - Recurrent Unit Circuit Design

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1. 設計取捨

- 一開始花了一段時間考慮要把哪些權重主動儲存在 circuit 上面，而因為最後計算的結果是看 AT 值(面積 \times cycle 數 \times cycle time)，如果把所有權重資料都存在 circuit 上，雖然會使得總 cycle 數量變很低，但是會導致節省下來的 cycle 數量的倍率跑到面積上面，而這樣會導致 circuit 過大，很難壓 cycle time。因此最後是選擇所有資料都重新讀取。
- 雖然原本以為把 B_{ih} 及 B_{hh} 放在 Circuit 上可以用少量的 area 換取一些 cycle 數上的節省，但是實際上實作後發現為了存 B_{ih} 及 B_{hh} 會導致多用了大約一半面積，反而得不償失，而 cycle 數只少了 $\frac{1}{64}$ 左右。

2. Stage

- 一開始仔細思考之後，會發現基本上只要依照讀六種不同 memory 的位置來切狀態即可完成，並且會在其中的五個狀態中重複循環。

3. 乘法器

- 在寫之前就有預想到乘法部分會變成 critical path，而實際用 design compiler 跑下去結果也是如此。因此把一個大乘法拆成多段小的乘法，然後把加總的部分放到下個 cycle 處理，這樣就能壓低 cycle time。

4. activation function

- 把乘法壓低後，critical path 就變成了計算 activation function 到傳出結果到 mdata_w 的這段，因為這段只有半個 cycle 的時間可以運算(其它的運算都是在下次的 posedge 前能計算出結果就好，但是送出的資料則必須要在 negedge 前計算完成)，因此把 activation function 跟送出的部分拆開成兩個階段，雖然會讓總 cycle 數量多大約 1%，卻可以讓 cycle time 繼續往下壓，因此這也是個好的優化。

5. Pipeline

- 盡量把大步驟拆成多個小步驟，然後盡量把小步驟均勻的分散到每個 state 中，使得每個 state 的執行時間都差不多，就能達到 pipeline 的效果，並壓低 cycle time。

6. 讀寫優化

- 盡量讓每個 register 寫入之後都不要在同個 cycle 中去讀他，可以讓 compiler 更容易的優化這種東西。

7. 乘法和加法單元

- 因為乘法和加法的部份仍然容易成為 critical path，因此把乘法和加法的部分拉到外面變成單獨一塊，這樣計算乘法和加法前就不需要 stage 等等的判斷。

8. Transistor-level 合成

- Transistor-level 合成的時候，在 nano Route 這個階段的時候，如果 WNS 不夠大，innovus 會直接 crash，因此後來發現的解決方法是事先先執行 ECO Design，然後到 Mode 裡面把 Thresholds 裡的 Setup Slack 提高，這樣就能讓 WNS 變成正比較大的值，而不是 0.000 附近。這樣之後就能順利的讓 nano Route 不會 crash 了。

9. 合成 Cycle time

- Gate-Level: 3.8 ns
- Transistor-Level: 3.8 ns

10. 結果

- Gate-level results
 - Can you pass gate-level simulation?
 - yes
 - Cycle time that can pass your gate-level simulation:
 - 3.8 ns
 - Total simulation time:
 - 4848466.532 ns
 - Total cell area:
 - $169135.726395 \mu\text{m}^2$
 - Cell area \times Simulation time:
 - $820048908791.6665 \mu\text{m}^2 \cdot \text{ns}$
- Transistor-level results
 - Can you pass transistor-level simulation?
 - yes
 - Cycle time that can pass your transistor-level simulation:
 - 3.8 ns
 - Total simulation time:
 - 4848466.528 ns
 - Total cell area:
 - $188070.223 \mu\text{m}^2$
 - Cell area \times Simulation time:
 - $911852181128.9957 \mu\text{m}^2 \cdot \text{ns}$

11. 截圖

◦ RTL Pass

```
b5902086@cad30:~/project/RTL>
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
  Instances Unique
  Modules:       2       2
  Registers:    64      64
  Scalar wires: 6       -
  Vectorized wires: 5      -
  Always blocks: 4       4
  Initial blocks: 11     11
  Cont. assignments: 0       6
  Pseudo assignments: 4       4
  Simulation timescale: 10ps
Writing initial simulation snapshot: worklib.testfixture:v
Loading snapshot worklib.testfixture:v ..... Done
ncsim> source /usr/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
ncsim: #,DVE/XACCI: some objects excluded from $dumpvars due to access restrictions, use +access+r on command line for access to all objects.
File: ./testfixture.v, line = 74, pos = 9
Scope: testfixture
Time: 0 FS + 0

-----
START!!! Simulation Start .....

-----
reset==0
busy==1

-----
----- S U M M A R Y -----
Congratulations! All data have been generated successfully! The result is PASS!!

-----
Simulation complete via $finish(1) at time 4848465600 PS + 0
./testfixture.v:171      #(`CYCLE/2); $finish;
ncsim> exit

(7.35 s) Thu Jun 18 06:54:03
(19)#/~/project/RTL7
(CAD)b5902086@cad30:[0]$ ncverilog testfixture.v RNN.v
```

o Gate-level Area Report

```
b5902086@cad30:~/project/RTL7/syn
*****
Report : area
Design : RNN
Version: N-2017.09-SP2
Date : Thu Jun 18 06:16:03 2020
*****


Library(s) Used:
    slow (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/slow.db)

Number of ports:          98
Number of nets:           10638
Number of cells:          10367
Number of combinational cells: 7643
Number of sequential cells: 2724
Number of macros/black boxes: 0
Number of buf/inv:         1393
Number of references:      158

Combinational area:       96390.253355
Buf/Inv area:             12696.552081
Noncombinational area:    72745.473040
Macro/Black Box area:     0.000000
Net Interconnect area:   1111279.106781

Total cell area:          169135.726395
Total area:                12880414.833176

Hierarchical area distribution
-----


| Hierarchical cell | Global cell area |               | local cell area |                   |             |        |
|-------------------|------------------|---------------|-----------------|-------------------|-------------|--------|
|                   | Absolute Total   | Percent Total | Combi-national  | Noncombi-national | Black-boxes | Design |
| RNN               | 169135.7264      | 100.0         | 96390.2534      | 72745.4730        | 0.0000      | RNN    |
| Total             |                  |               | 96390.2534      | 72745.4730        | 0.0000      |        |


1

(11 ms) Thu Jun 18 07:24:52
(25)#/~/project/RTL7/syn
(CAD)b5902086@cad30:[0]$
```

o Gate-level Timing Report

```
b5902086@cad30:~/project/RTL7/syn
Endpoint: mul_02_reg[7]
(rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port      Wire Load Model      Library
-----              tsmc13_wl10      slow
RNN
Point                  Incr      Path
-----


clock clk (fall edge)        1.90      1.90
clock network delay (ideal)  0.50      2.40
input external delay         0.20      2.60 r
mdata_r[9] (in)              0.17      2.77 r
U3880/Y (BUF8X8)            0.18      2.95 r
U4280/Y (NAND2X2)           0.10      3.05 f
U3772/Y (NAND3X3)           0.13      3.18 r
U5082/Y (NAND2X6)           0.10      3.28 f
U5762/Y (ANOD2X8)           0.18      3.47 f
U3652/Y (NOINV4)             0.10      3.57 r
U3569/Y (NOINV4)             0.09      3.66 f
U3517/Y (NAND2X4)            0.09      3.75 r
U6015/Y (AOI21X4)            0.11      3.86 f
U8868/Y (OA121X2)            0.17      4.03 r
mul_02_reg[7]/D (DFFHQX2)    0.00      4.03 r
data arrival time            0.00

slack (MET)                  0.00

1

(10 ms) Thu Jun 18 07:25:25
(26)#/~/project/RTL7/syn
(CAD)b5902086@cad30:[0]$
```

- Gate-level Pass

```
b5902086@cad30:~/project/KIL7
-----
START!!! Simulation Start .....

-----
Warning! Timing violation
$setuphold$setup(< posedge CK && (flag == 1):5700 PS, negedge D:5532 PS, 0.284 : 284 PS, -0.131 : -131 PS );
File: ./syn/tsmc13_neg.v, line = 18114
Scope: testfixture.u_RNN.\t_offset_reg[3]
Time: 5700 PS

-----
Warning! Timing violation
$setuphold$setup(< posedge CK && (flag == 1):5700 PS, negedge D:5555 PS, 0.264 : 264 PS, -0.087 : -87 PS );
File: ./syn/tsmc13_neg.v, line = 18064
Scope: testfixture.u_RNN.\t_offset_reg[2]
Time: 5700 PS

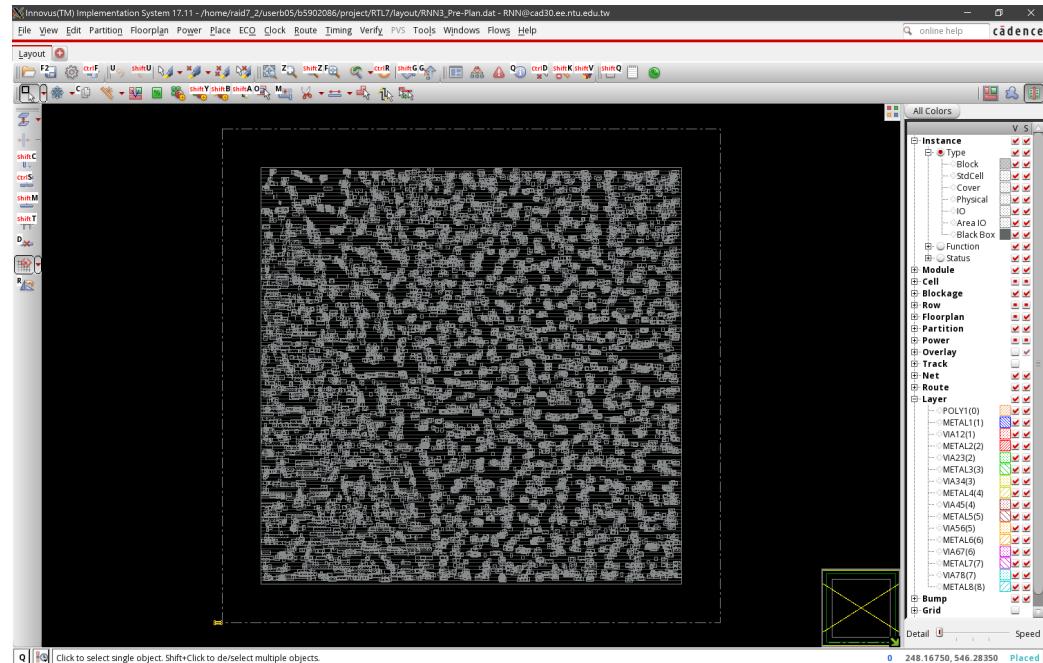
-----
Warning! Timing violation
$setuphold$setup(< posedge CK && (flag == 1):5700 PS, negedge D:5504 PS, 0.270 : 270 PS, -0.114 : -114 PS );
File: ./syn/tsmc13_neg.v, line = 18114
Scope: testfixture.u_RNN.\h_offset_reg[4]
Time: 5700 PS

reset==0
busy==1

-----
----- S U M M A R Y -----
Congratulations! All data have been generated successfully! The result is PASS!

-----
Simulation complete via $finish(1) at time 4848466532 PS + 0
./testfixture.v:171      #(`CYCLE/2); $finish;
ncsim> exit
(7 min 08 s) Thu Jun 18 07:01:30
(20)#/project/RTL7
(CAD)b5902086@cad30:[0]$ ncverilog testfixture.v RNN_syn.v -v syn/tsmc13_neg.v +define+SDF
```

- Transistor-level Floorplan



```

b5902086@cad30:~/project/RTL7/layout$ timeDesign
# Design Mode: 90nm
# Analysis Mode: MMNC Non-OCV
# Parasitics Mode: No SPEF/Rcdb
# Signoff Settings: SI OFF
#####
##### calculate delays in BcWC mode...
Start delay calculation (FullDC) (32 T). (MEM=3929.96)
AAE DR initialization (MEM=3058.71 CPU=0:00:00.1 REAL=0:00:00.0)
AAE_INFO: Cdb files are:
        /home/raid7_2/userb05/b5902086/project/RTL7/layout/RNN3_Pre-Plan.dat/libs/mmnc/slow.cdb
        /home/raid7_2/userb05/b5902086/project/RTL7/layout/RNN3_Pre-Plan.dat/libs/mmnc/fast.cdb

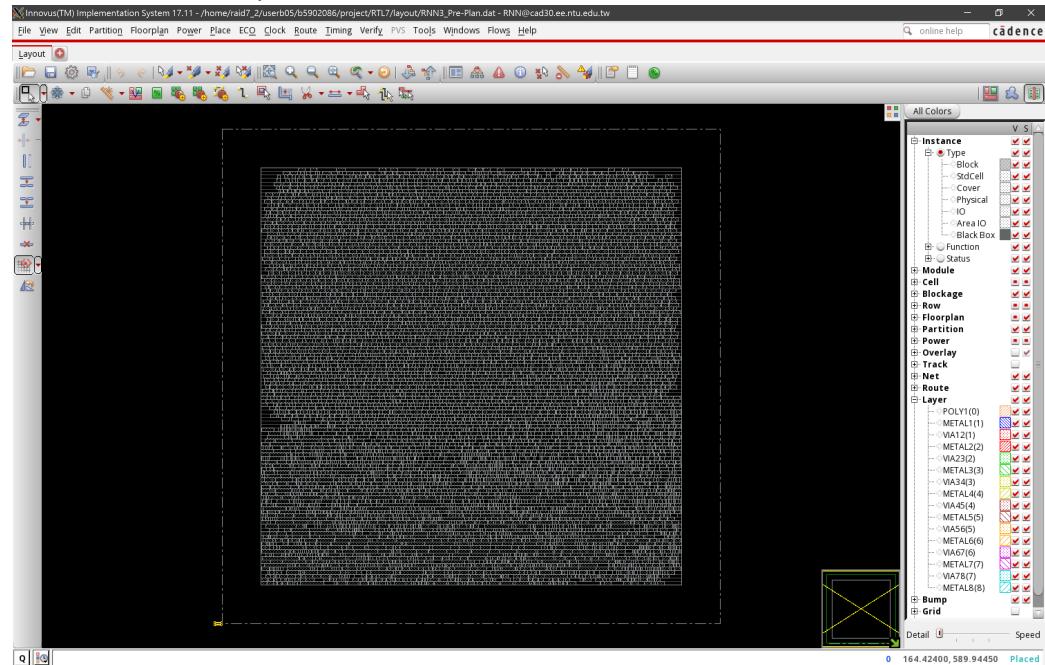
Total number of fetched objects 10641
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=5140.48 CPU=0:00:03.2 REAL=0:00:01.0)
End delay calculation (FullDC). (MEM=4981.11 CPU=0:00:04.9 REAL=0:00:02.0)
*** Done Building Timing Graph (cpu=0:00:06.8 real=0:00:02.0 totSession(cpu=0:05:54 mem=3385.6M)

timeDesign Summary
-----
Setup views included:
av_func_mode_max av_scan_mode_max

+-----+-----+-----+
| Setup mode | all | regZreg | default |
+-----+-----+-----+
| WNS (ns): | 0.475 | 0.783 | 0.475 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 2769 | 2726 | 2729 |
+-----+-----+-----+
Density: 89.932%
Set Using Default Delay Limit as 1000.
Resetting back High Fanout Nets as non-ideal
Set Default Net Delay as 1000 ps.
Set Default Net Load as 0.5 pF.
Reported timing to dlr timingReports
Total CPU time: 9.99 sec
Total Real time: 4.0 sec
Total Memory Usage: 3058.25 Mbytes
innovus 1>

```

○ Transistor-level Full placement



```

b5902086@cad30:~/project/RTL7/layout
misc timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
*WARN: (IMPEST-3014): The RC network is incomplete for net busy. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
*WARN: (IMPEST-3014): The RC network is incomplete for net mdata_w[0]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
total number of fetched objects: 10572
AAE INFO: total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=5796.49 CPU=0:00:02.7 REAL=0:00:00.0)
End delay calculation (FullDC). (MEM=5796.49 CPU=0:00:02.9 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:04.4 real=0:00:01.0 totSessionCpu=0:21:06 mem=3972.0M)

timeDesign Summary

Setup views included:
av_func_mode_max

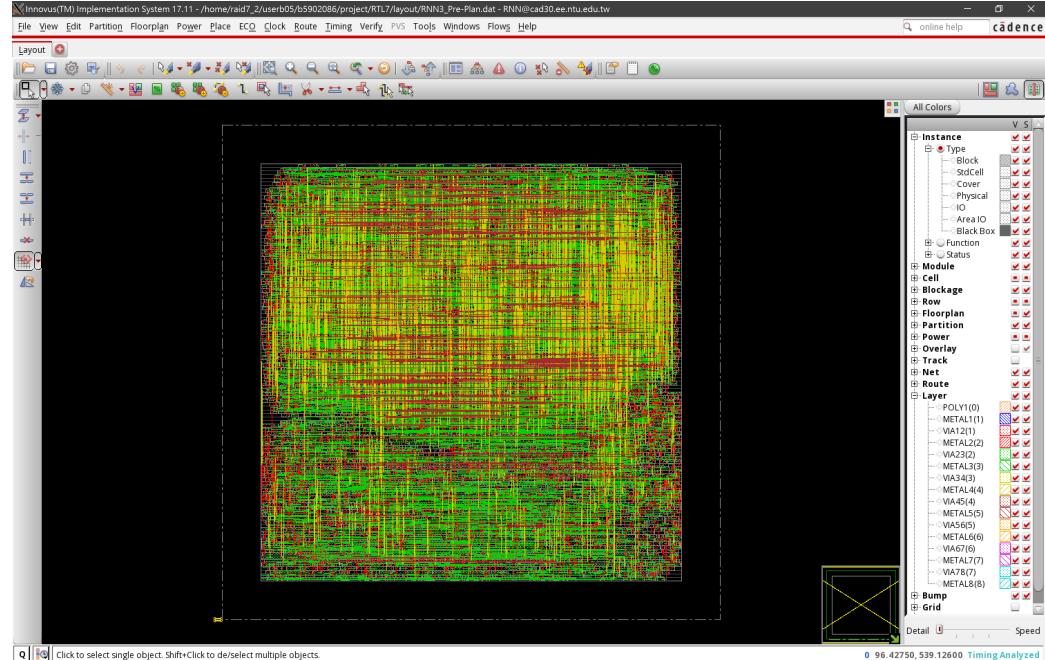
Setup mode | all | regReg | default |
WNS (ns): 0.346 0.346 0.346
TNS (ns): 0.000 0.000 0.000
Violating Paths: 0 0 0
All Paths: 2769 2726 2729

DRVs | Real | Total |
| Nr nets(terms) | Worst Vio | Nr nets(terms) |
max_cap | 0 (0) | 0.000 | 0 (0)
max_tran | 0 (0) | 0.000 | 0 (0)
max_fanout | 0 (0) | 0 | 0 (0)
max_length | 0 (0) | 0 | 0 (0)

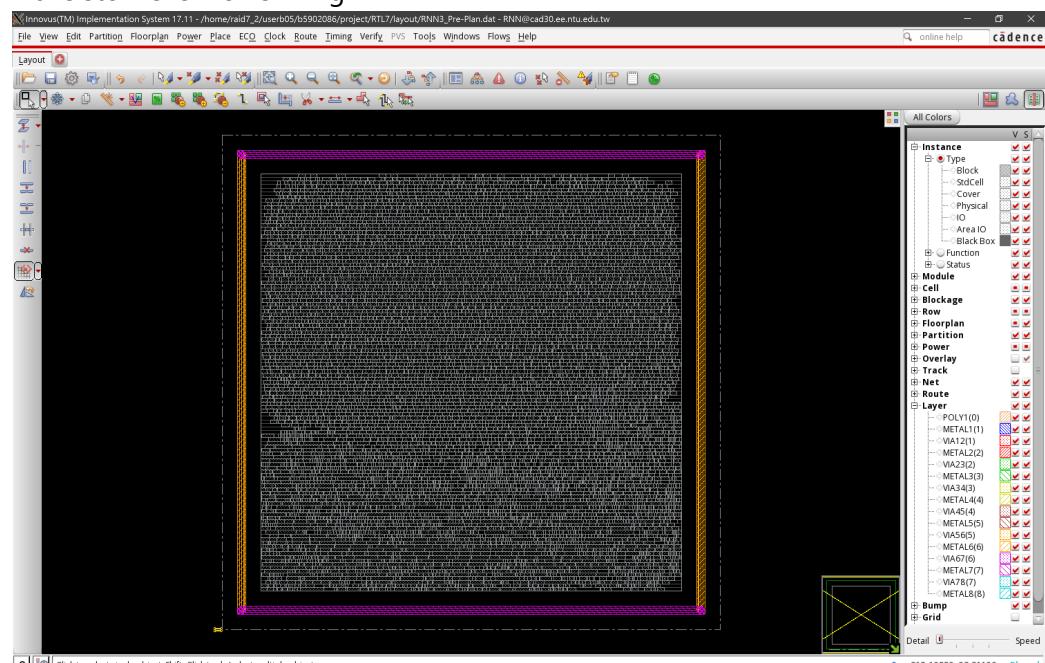
Density: 90.456%
Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports
Total CPU time: 8.87 sec
Total Real time: 2.0 sec
Total Memory Usage: 3978.984375 Mbytes
innovus 1>

```



- Transistor-level Power Ring



- Transistor-level Power Stripe

Innovus(TM) Implementation System 17.11 -/home/raid7_2/userb05/b5902086/project/RTL7/layout/RNN3_Plan.dat - RNN@cad30.ee.ntu.edu.tw

File View Edit Partition Floorplan Power Place FCO Clock Route Timing Verify PVS Tools Windows Flows Help

online help

cadence

Layout

Click to select single object. Shift+Click to de-select multiple objects.

Instance Type: Block, StdCell, Cover, Physical, IO, Input, Output, Black Box, Function, Status

Module: Cell, Blockage, Row, Floorplan, Partition, Power, Overlay, Track, Net, Route, Layer: POLY1(0), METAL1(1), VIA1(2), METAL2(2), VIA2(2), METAL3(3), VIA3(3), METAL4(4), VIA4(4), METAL5(5), VIA5(5), METAL6(6), VIA6(6), METAL7(7), VIA7(7), METAL8(8), VIA8(8), Burn, Grid

Detail Speed

192.33850, 103.94700 Placed

```

innovus 1> **WARN: (IMPTCM-125): Option "-checkPinLayerForAccess" for command getPlaceMode is obsolete and will be ignored. It no longer has any effect and should be removed from your script.
*** Starting refinePlace (0:21:38 mem=3988.9M) ***
Density distribution unevenness ratio = 3.385%
Move report: Detail placement moves 0 insts, mean move: 0.00 um, max move: 0.00 um
Runtime: CPU: 0:00:01.1 REAL: 0:00:01.0 MEM: 3988.9MB
Summary Report:
Instances move: 0 (out of 10398 movable)
Instances flipped: 0
Mean displacement: 0.00 um
Max displacement: 0.00 um
Runtime: CPU: 0:00:00.1 REAL: 0:00:01.0 MEM: 3988.9MB
*** Finished refinePlace (0:21:38 mem=3988.9M) ***
Density distribution unevenness ratio = 3.385%
innovus 1> *** Starting Verify Geometry (MEM: 4008.9) ***
**WARN: (IMPVG-257): verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future release. Please update your script to use the new command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
bin size: 8320
**WARN: (IMPVG-198): Area to be verified is small to see any runtime gain from multi-cpus. Use setMultiCpuUsage command to adjust the number of CPUs.
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
M: elapsed time: 4.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.
*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:04.2 MEM: 87.6M)
innovus 1> 

innovus 1> 
use timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
*WARN: (IMPESI-3014): The RC network is incomplete for net busy. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
*WARN: (IMPESI-3014): The RC network is incomplete for net mdata_w[0]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
Total number of fetched objects 10672
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=5814.16 CPU=0:00:02.8 REAL=0:00:01.0)
End delay calculation (fullDC). (MEM=5814.16 CPU=0:00:03.0 REAL=0:00:01.0)
*** Done Building Timing Graph (cpu=0:00:04.5 real=0:00:01.0 totSessionCpu=0:21:52 mem=3982.7M)

timeDesign Summary
-----
Setup views included:
av_func_mode_max



| Setup mode       | all   | reg2reg | default |
|------------------|-------|---------|---------|
| WNS (ns)         | 0.345 | 0.345   | 0.348   |
| TNS (ns)         | 0.000 | 0.000   | 0.000   |
| Violating Paths: | 0     | 0       | 0       |
| All Paths:       | 2769  | 2726    | 2729    |



| DRVs       | Real            | Total     |                 |
|------------|-----------------|-----------|-----------------|
|            | Nr nets(termss) | Worst Vio | Nr nets(termss) |
| max_cap    | 0 (0)           | 0.000     | 0 (0)           |
| max_tran   | 0 (0)           | 0.000     | 0 (0)           |
| max_fanout | 0 (0)           | 0         | 0 (0)           |
| max_length | 0 (0)           | 0         | 0 (0)           |


Density: 99.456%
Routing Overflow: 0.00% H and 0.00% V
Reported timing to dir timingReports
Total CPU time: 8.7 sec
Total Real time: 3.0 sec
Total Memory Usage: 3989.664062 Mbytes
innovus 1> 

```

- Transistor-level CTS

Innovus(TM) Implementation System 17.11 - /home/rajd7_2/userb05/b5902086/project/RTL7/layout/RNN3_Plan.dat - RNN@cad30.ee.ntu.edu.tw

File View Edit Partition Floorplan Power Place FCO Clock Route Timing Verify PVS Tools Windows Flows Help

cadence

Layout

Instance Type: Block, StdCell, Cover, Physical, IO, Input, ID, Black Box, Function, Status

Module: Cell, Blockage, Row, Floorplan, Partition, Power, Overlay, Track, Net, Route, Layer: POLY1(0), METAL1(1), VIA1(2), METAL2(2), VIA2(2), METAL3(3), VIA3(3), METAL4(4), VIA4(4), METAL5(5), VIA5(5), METAL6(6), VIA6(6), METAL7(7), VIA7(7), METAL8(8), Burn, Grid

All Colors

V S

Click to select single object. Shift+Click to de-select multiple objects.

575.98300, 508.34850 Timing Analyzed

```

b5902086@cad30:~/project/RTL7/layout
ise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPEST-3014): The RC network is incomplete for net busy. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPEST-3014): The RC network is incomplete for net mdata_w[0]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
total number of fetched objects 10672
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=5983.89 CPU=0:00:02.8 REAL=0:00:01.0)
End delay calculation (fullDC). (MEM=5983.89 CPU=0:00:03.0 REAL=0:00:01.0)
*** Done Building Timing Graph (cpu=0:00:04.4 real=0:00:01.0 totSessionCpu=0:23:36 mem=4170.4M)

timeDesign Summary

Setup views included:
av_func_mode_max



| Setup mode       | all   | reg2reg | default |
|------------------|-------|---------|---------|
| WNS (ns):        | 0.347 | 0.347   | 0.348   |
| TNS (ns):        | 0.000 | 0.000   | 0.000   |
| Violating Paths: | 0     | 0       | 0       |
| All Paths:       | 2769  | 2726    | 2729    |



| DRVs       | Real           |           | Total          |
|------------|----------------|-----------|----------------|
|            | Nr nets(terms) | Worst Vio | Nr nets(terms) |
| max_cap    | 0 (0)          | 0.000     | 0 (0)          |
| max_tran   | 0 (0)          | 0.000     | 0 (0)          |
| max_fanout | 0 (0)          | 0         | 0 (0)          |
| max_length | 0 (0)          | 0         | 0 (0)          |



Density: 90.456%
Routing Overflow: 0.00% H and 0.00% V
Reported timing to dir timingReports
Total CPU time: 7.45 sec
Total Real time: 2.0 sec
Total Memory Usage: 4179.398438 Mbytes
innovus 6> 
```



```

b5902086@cad30:~/project/RTL7/layout
**WARN: (IMPEST-3014): The RC network is incomplete for net mdata_r[1]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPEST-3014): The RC network is incomplete for net mdata_r[15]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPEST-3014): The RC network is incomplete for net mdata_r[9]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPEST-3014): The RC network is incomplete for net mdata_r[1]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPEST-3014): The RC network is incomplete for net mdata_r[15]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPEST-3014): The RC network is incomplete for net mdata_r[9]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPEST-3014): The RC network is incomplete for net mdata_w[0]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPEST-3014): The RC network is incomplete for net mdata_w[0]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
total number of fetched objects 10672
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=5937.33 CPU=0:00:03.4 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=5937.33 CPU=0:00:03.6 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:05.4 real=0:00:00.0 totSessionCpu=0:23:47 mem=4124.9M)

timeDesign Summary

Hold views included:
av_func_mode_min av_scan_mode_min

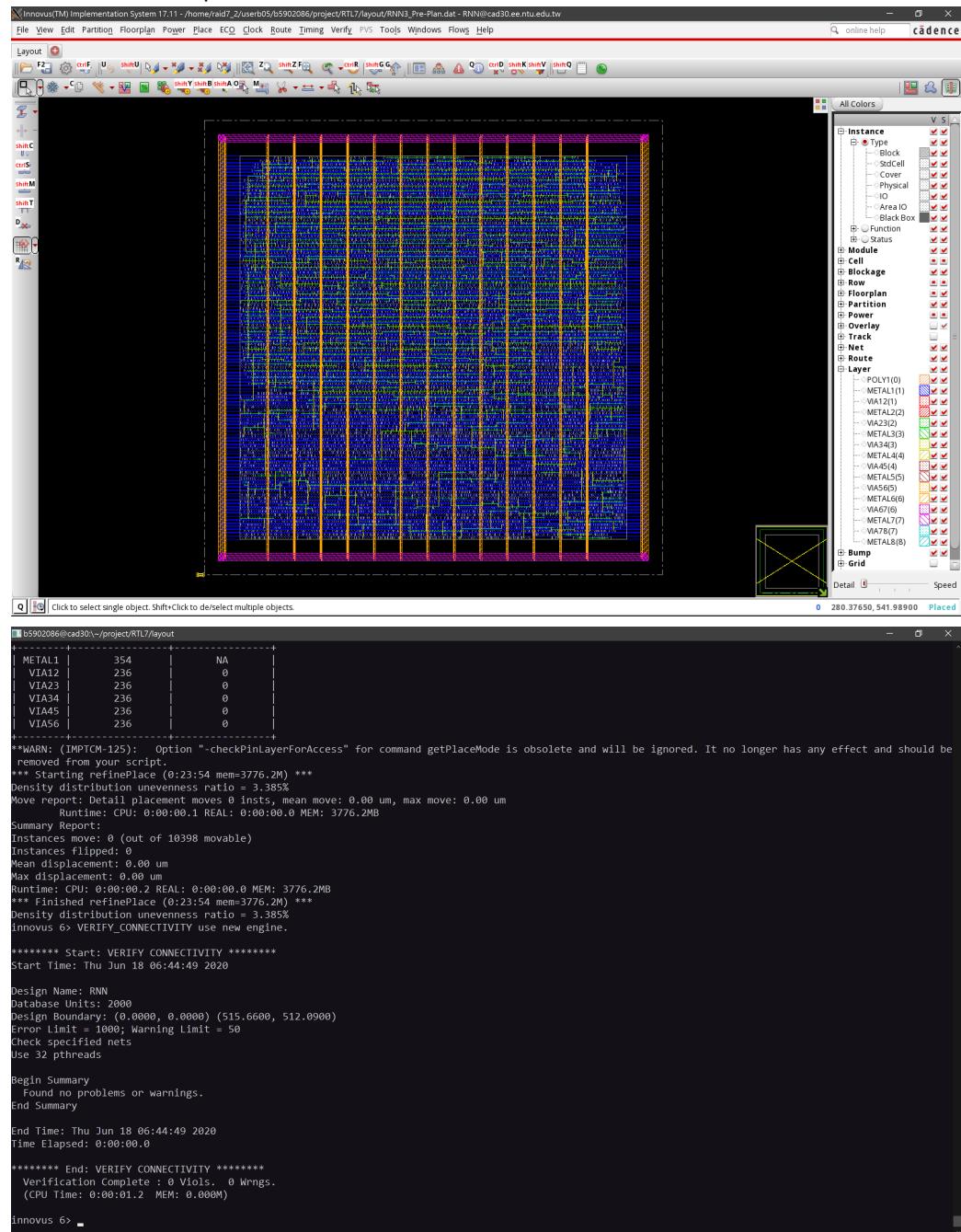


| Hold mode        | all   | reg2reg | default |
|------------------|-------|---------|---------|
| WNS (ns):        | 0.036 | 0.036   | 0.725   |
| TNS (ns):        | 0.000 | 0.000   | 0.000   |
| Violating Paths: | 0     | 0       | 0       |
| All Paths:       | 2769  | 2726    | 2729    |

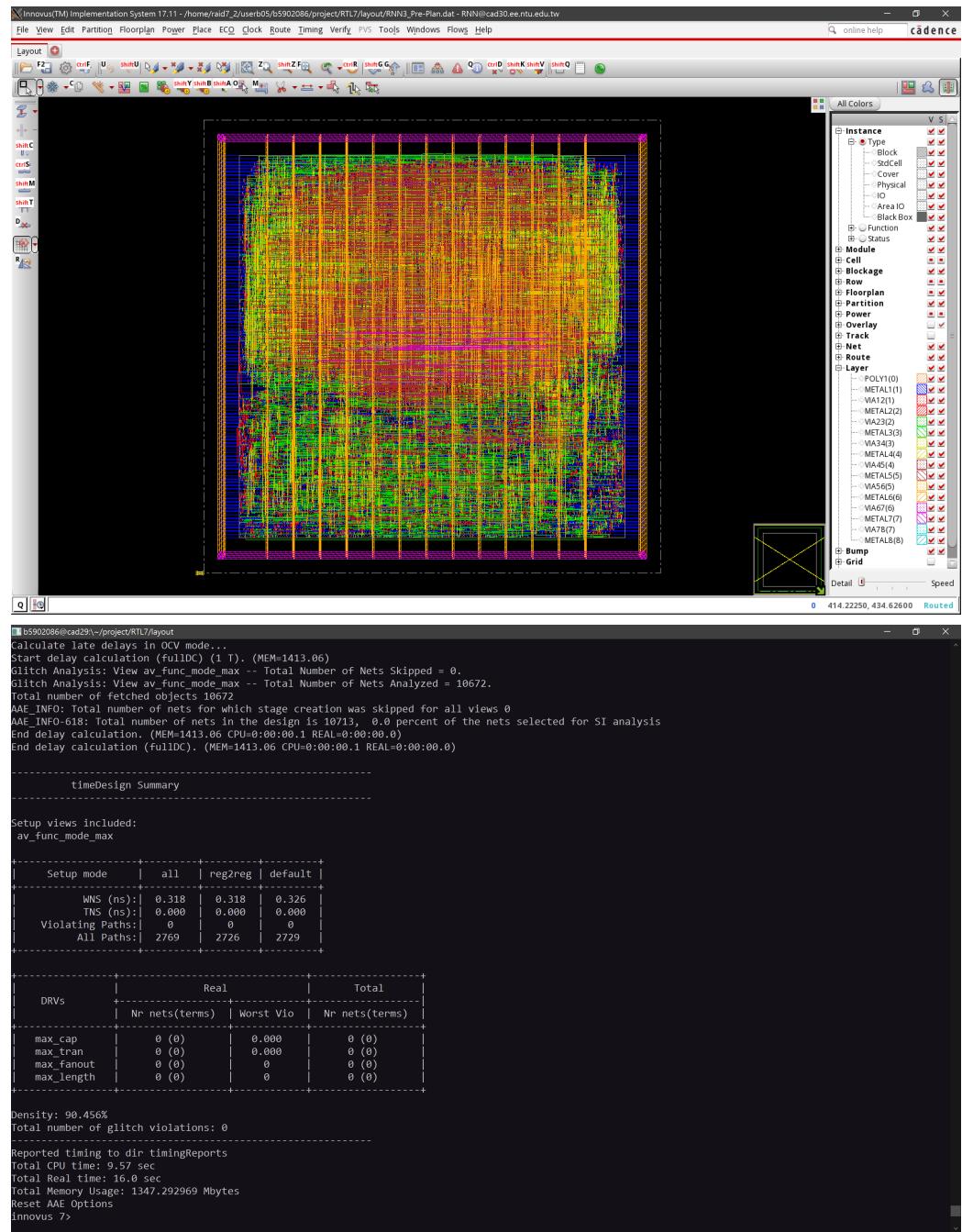


Density: 90.456%
Routing Overflow: 0.00% H and 0.00% V
Reported timing to dir timingReports
Total CPU time: 8.18 sec
Total Real time: 2.0 sec
Total Memory Usage: 3776.242188 Mbytes
innovus 6> 
```

- Transistor-level Special Route



- Transistor-level Nano Route



```

[1 b5902086@cad30:~/project/RTL7/layout]
End delay calculation. (MEM=5886.44 CPU=0:00:06.5 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=5886.44 CPU=0:00:07.4 REAL=0:00:01.0)
Loading CTE timing window with TwFlowType 0...(CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 4049.9M)
Add other locks and setup t0AAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.2, REAL = 0:00:01.0, MEM = 4049.9M)
Starting ST iteration 2
Calculate late delays in OCV mode...
Calculate early delays in OCV mode...
Calculate late delays in OCV mode...
Calculate early delays in OCV mode...
Start delay calculation (fullDC) (32 T). (MEM=4057.93)
Glitch Analysis: View av_func mode min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func mode min -- Total Number of Nets Analyzed = 98.
Glitch Analysis: View av_scan mode min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_scan mode min -- Total Number of Nets Analyzed = 98.
Total number of fetched objects: 10672
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 10713, 0.0 percent of the nets selected for ST analysis
End delay calculation. (MEM=5851.28 CPU=0:00:00.5 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=5851.28 CPU=0:00:00.5 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:13.0 real=0:00:02.0 tottSessionCpu=0:27:23 mem=5851.3M)

-----
timeDesign Summary
-----

Hold views included:
av_func_mode_min av_scan_mode_min

+-----+-----+-----+
| Hold mode | all | regRreg | default |
+-----+-----+-----+
| WNS (ns): | 0.035 | 0.035 | 0.764 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 2769 | 2726 | 2729 |
+-----+-----+-----+
Density: 90.456%
Reported timing to dir timingReports
Total CPU time: 17.86 sec
Total Real time: 4.0 sec
Total Memory Usage: 3689.445312 Mbytes
Reset AAE Options
innovus 7>

[1 b5902086@cad30:~/project/RTL7/layout]
+-----+-----+-----+
| WNS (ns): | 0.035 | 0.035 | 0.764 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 2769 | 2726 | 2729 |
+-----+-----+-----+
Density: 90.456%
Reported timing to dir timingReports
Total CPU time: 17.86 sec
Total Real time: 4.0 sec
Total Memory Usage: 3689.445312 Mbytes
Reset AAE Options
innovus 7> *** Starting Verify Geometry (MEM: 3689.4) ***
**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future release. Please update your script to use the new command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 8320
**WARN: (IMPVFG-198): Area to be verified is small to see any runtime gain from multi-cpus. Use setMultiCpuUsage command to adjust the number of CPUs.
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 7.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.
*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:07.0 MEM: 212.8M)
innovus 7>

```

○ Transistor-level Summary

```

[1 b5902086@cad30:~/project/RTL7/layout]
BUFX12 1.023840
BUFX12 1.023840
BUFX8 0.682560
BUFX8 0.682560
BUFX6 0.511920
BUFX6 0.511920
BUF4 0.341280
BUF4 0.341280
BUF3 0.259680
BUF3 0.259680
BUF2 0.170640
BUF2 0.170640 1054
# Cells in lib with max_fanout: 0
SDC max_cap: N/A
SDC max_tran: N/A
SDC max_fanout: N/A
Default Ext. Scale Factor: 1.000
Detail Ext. Scale Factor: 1.000

=====
Floorplan/Placement Information
=====
Total [redacted] of Standard cells: 179120.218 um^2
Total [redacted] of Standard cells(Subtracting Physical Cells): 170120.218 um^2
Total [redacted] of Macros: 0.000 um^2
Total [redacted] of Blockages: 0.000 um^2
Total [redacted] of Pad cells: 0.000 um^2
Total [redacted] of Core: 188070.223 um^2
Total [redacted] of Chip: 264064.329 um^2
Effective Utilization: 9.0456e-01
Number of Cell Rows: 117
% Pure Gate Density #1 (Subtracting BLOCKAGES): 90.456%
% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 90.456%
% Pure Gate Density #3 (Subtracting MACROS): 90.456%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 90.456%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 90.456%
% Pure Gate Density #6 ((Unplaced Standard Inst + Unplaced Block Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area)) for Insts where they are placed: 90.456%
% Core Density (Counting Std Cells and MACROs): 90.456%
% Core Density #2(Subtracting Physical Cells): 90.456%
% Chip Density (Counting Std Cells and MACROs and IOs): 64.424%
% Chip Density #2(Subtracting Physical Cells): 64.424%
# Macros within 5 sites of IO pad: No
Macro halo defined?: No

```

- Transistor-level Pass

```
b5902086@cad30:~/project/RTL
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
      Instances Unique
    Modules:          2      2
  Registers:        64     64
 Scalar wires:       6      -
Vectorized wires:   5      -
 Always blocks:    4      4
Initial blocks:    11     11
  Control assignments: 0      6
 Pseudo assignments: 4      4
 Simulation timescale: 10ps
Writing initial simulation snapshot: worklib.testfixture.v
Loading snapshot worklib.testfixture.v ..... Done
ncsim> source /usr/cad/cadence/INCISIV/curr/tools/inca/files/ncsimrc
ncsim> run
ncsim: #*,DVEXACC: some objects excluded from $dumpvars due to access restrictions, use +access+r on command line for access to all objects.
      File: ./testfixture.v, line = 74, pos = 9
      Scope: testfixture
      Time: 0 FS + 0
-----
----- START!!! Simulation Start .....
-----
reset==0
busy==1
-----
----- S U M M A R Y -----
Congratulations! All data have been generated successfully! The result is PASS!
-----
Simulation complete via $finish(1) at time 4848465600 PS + 0
./testfixture.v:171      #(`CYCLE/2); $finish;
ncsim> exit
(7.35 s) Thu Jun 18 06:54:03
(19)#/~/project/RTL
(CAD)b5902086@cad30:[0]$ ncverilog testfixture.v RNN.v
```