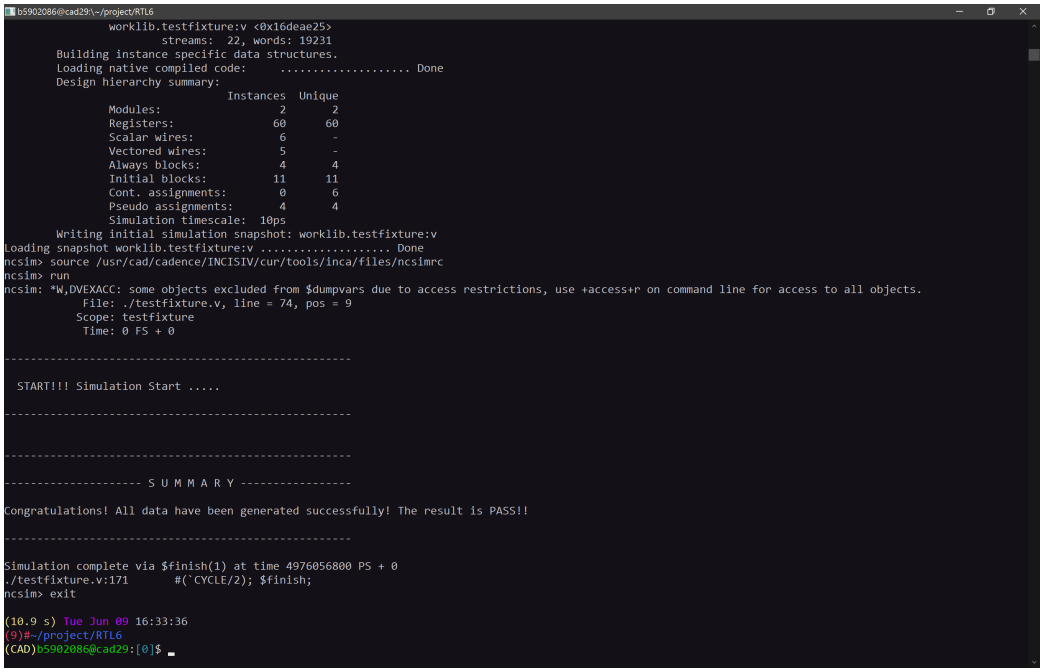
Final project - Recurrent Unit Circuit Design

b05902086 周逸

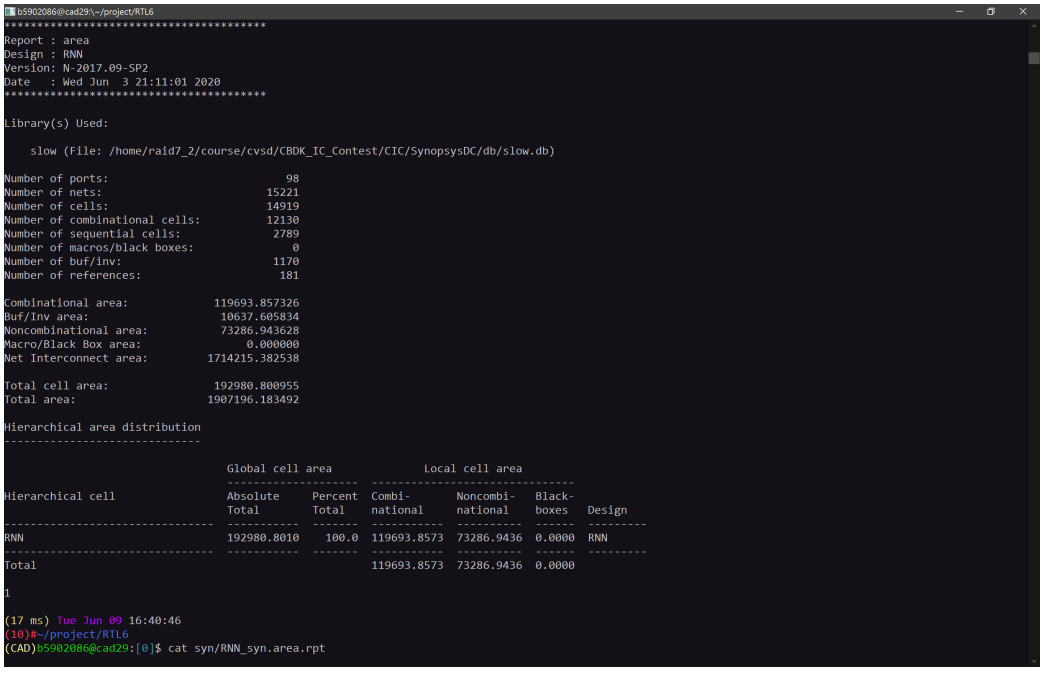
1. 設計取捨
    - 一開始花了一段時間考慮要把哪些權重主動儲存在 circuit 上面，而因為最後計算的結果是看 AT 值(面積×cycle數×cycle time)，如果把所有權重資料都存在 circuit 上，雖然會使得總 cycle 數量變很低，但是會導致節省下來的 cycle 數量的倍率跑到面積上面，而這樣會導致 circuit 過大，很難壓 cycle time。因此最後是選擇所有資料都重新讀取。
    - 雖然原本以為把 B_{ih} 及 B_{hh} 放在 Circuit 上可以用少量的 area 換取一些 cycle 數上的節省，但是實際上實作後發現為了存 B_{ih} 及 B_{hh} 會導致多用了大約一半面積，反而得不償失，而 cycle 數只少了$\frac{1}{64}$左右。
2. Stage
    - 一開始仔細思考之後，會發現基本上只要依照讀六種不同 memory 的位置來切狀態即可完成，並且會在其中的五個狀態中重複循環。
3. 乘法器
    - 在寫之前就有預想到乘法部分會變成 critical path，而實際用 design compiler 跑下去結果也是如此。因此把一個大乘法拆成多段小的乘法，然後把加總的部分放到下個 cycle 處理，這樣就能壓低 cycle time。
4. activation function
    - 把乘法壓低後，critical path 就變成了計算 activation function 到傳出結果到 mdata_w 的這段，因為這段只有半個 cycle 的時間可以運算(其它的運算都是在下次的 posedge 前能計算出結果就好，但是送出的資料則必須要在 negedge 前計算完成)，因此把 activation function 跟送出的部分拆開成兩個階段，雖然會讓總 cycle 數量多大約1%，卻可以讓 cycle time 繼續往下壓，因此這也是個好的優化。
5. 合成 Cycle time
    - Gate-Level: $4.5\ ns$
    - Transistor-Level: $4.5\ ns$
        - Ratio: 1.5
        - Density: 0.9
6. 結果
    - Gate-level results
        - Can you pass gate-level simulation?
            - yes
        - Cycle time that can pass your gate-level simulation:
            - $4.5\ ns$
        - Total simulation time:
            - $5741605.030\ ns$
        - Total cell area:
            - $192980.800955\ \mu m^2$
        - Cell area $\times$ Simulation time:
            - $1108019537456.657\ \mu m^2 \cdot ns$
    - Transistor-level results

- Can you pass transistor-level simulation?
  - yes
- Cycle time that can pass your transistor-level simulation:
  - $3.9\ ns$
- Total simulation time:
  - $4976057.763\ ns$
- Total cell area:
  - $214514.017\ \mu m^2$
- Cell area $\times$ Simulation time:
  - $1067434139565.164\ \mu m^2 \cdot ns$

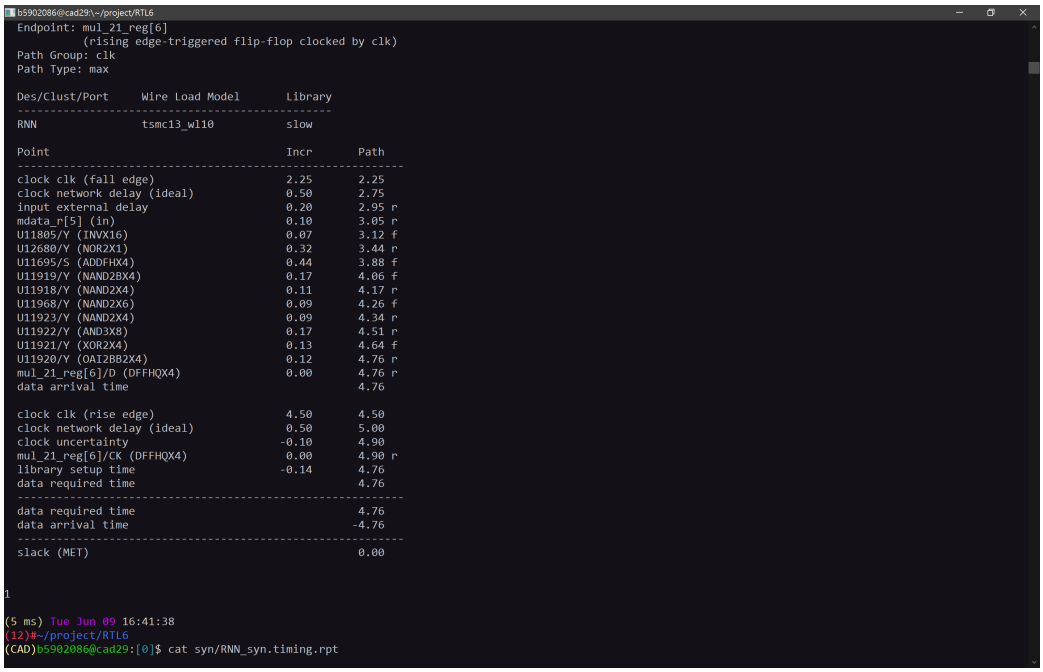
7. 截圖
   - RTL Pass



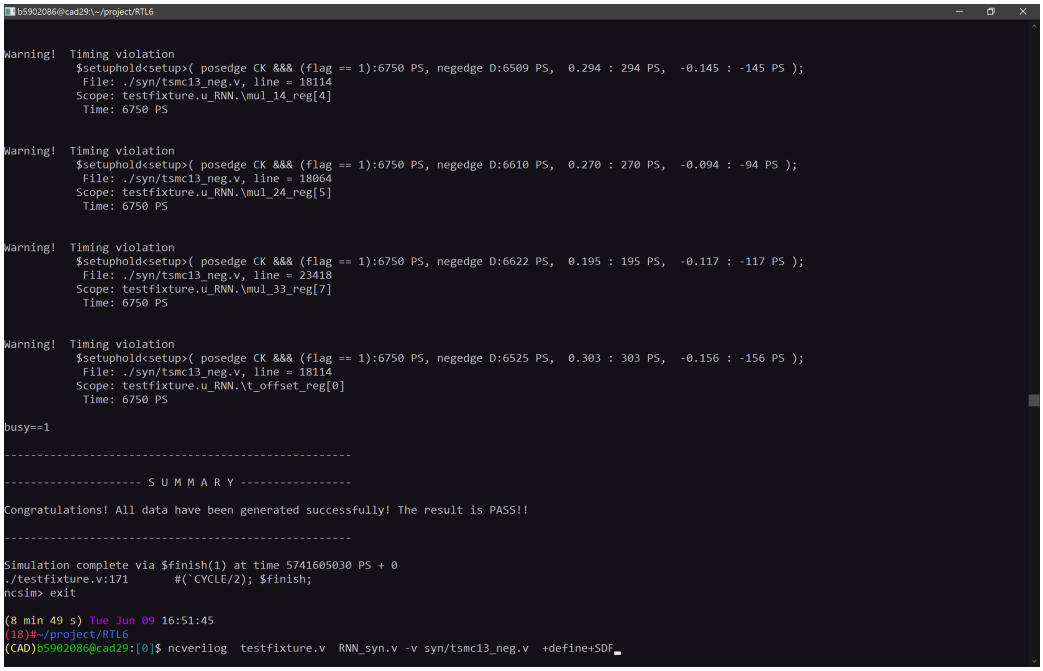
   - Gate-level Area Report



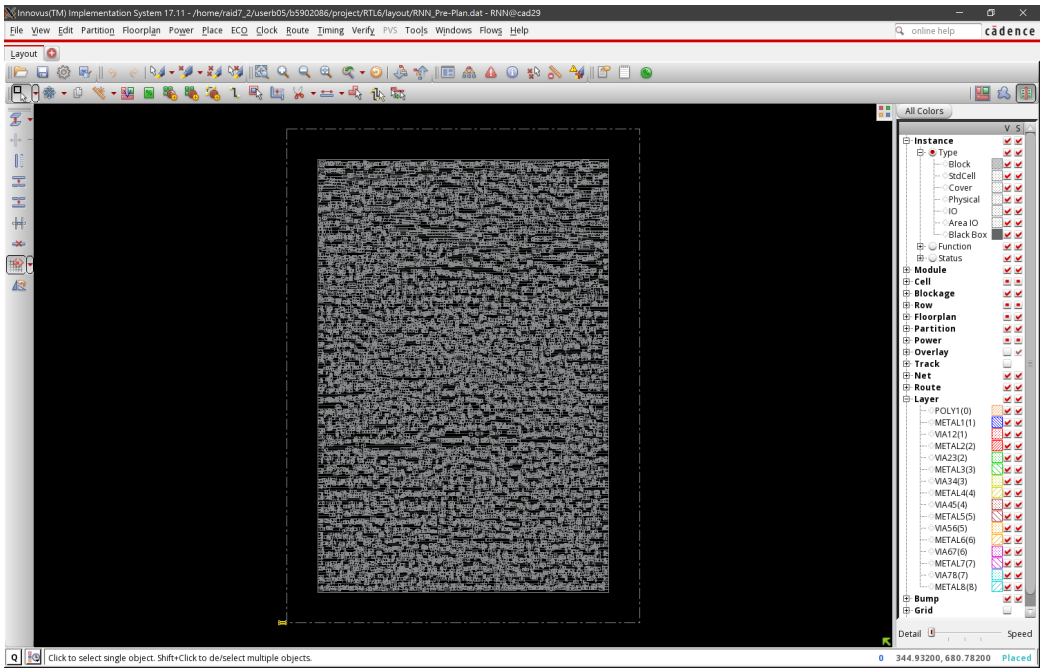
- Gate-level Timing Report



- Gate-level Pass

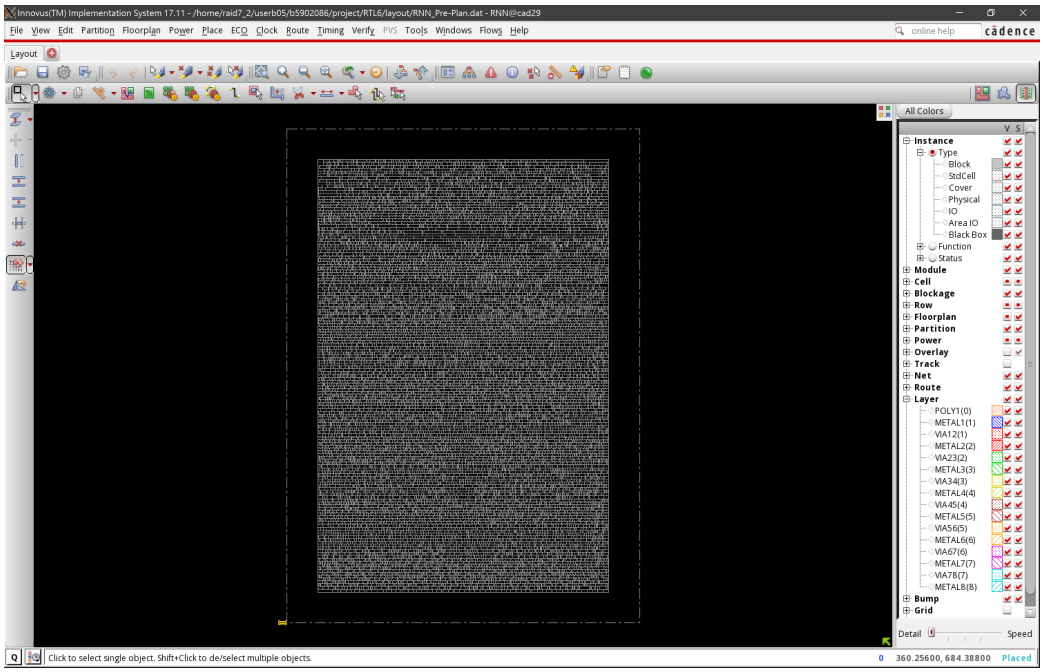


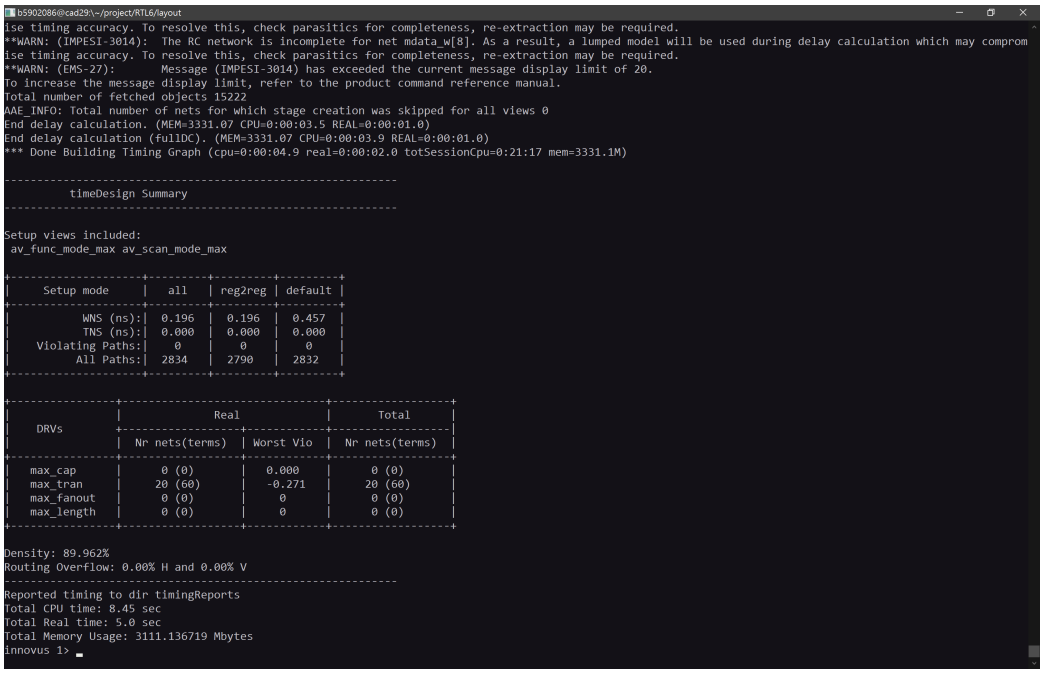
- Transistor-level Floorplan

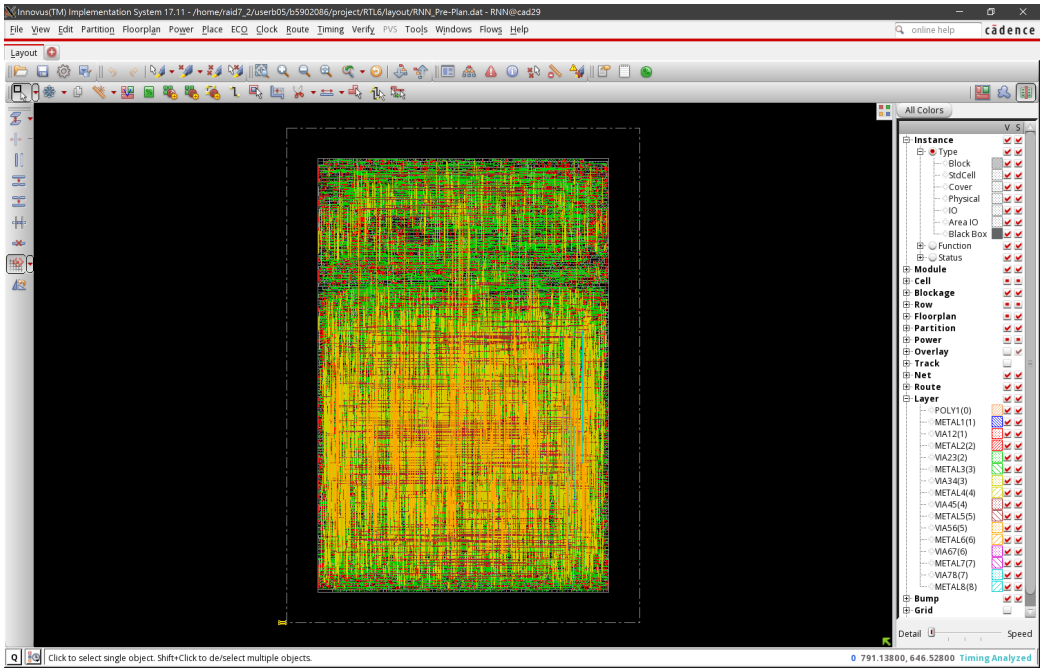



```
b5902086@cad29:\~/project/RTL6/layout
# Design Mode: 90nm
# Analysis Mode: MMMC Non-OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
################################################################################
Calculate delays in BcWc mode...
Calculate delays in BcWc mode...
Start delay calculation (fullDC) (4 T). (MEM=2902.43)
AAE DB initialization (MEM=2931.24 CPU=0:00:00.1 REAL=0:00:00.0)
AAE_INFO: Cdb files are:
        /home/raid7_2/userb05/b5902086/project/RTL6/layout/RNN_Pre-Plan.dat/libs/mmmc/slow.cdB
        /home/raid7_2/userb05/b5902086/project/RTL6/layout/RNN_Pre-Plan.dat/libs/mmmc/fast.cdB

Total number of fetched objects 15222
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=3411.68 CPU=0:00:02.8 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=3308.31 CPU=0:00:04.6 REAL=0:00:03.0)
*** Done Building Timing Graph (cpu=0:00:05.6 real=0:00:04.0 totSessionCpu=0:19:53 mem=3308.3M)

------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max av_scan_mode_max

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.596  |  0.960  |  0.596  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  2834   |  2790   |  2832   |
+--------------------+---------+---------+---------+

Density: 89.962%
------------------------------------------------------------
Set Using Default Delay Limit as 1000.
Resetting back High Fanout Nets as non-ideal
Set Default Net Delay as 1000 ps.
Set Default Net Load as 0.5 pF.
Reported timing to dir timingReports
Total CPU time: 7.52 sec
Total Real time: 5.0 sec
Total Memory Usage: 3062.171875 Mbytes
```

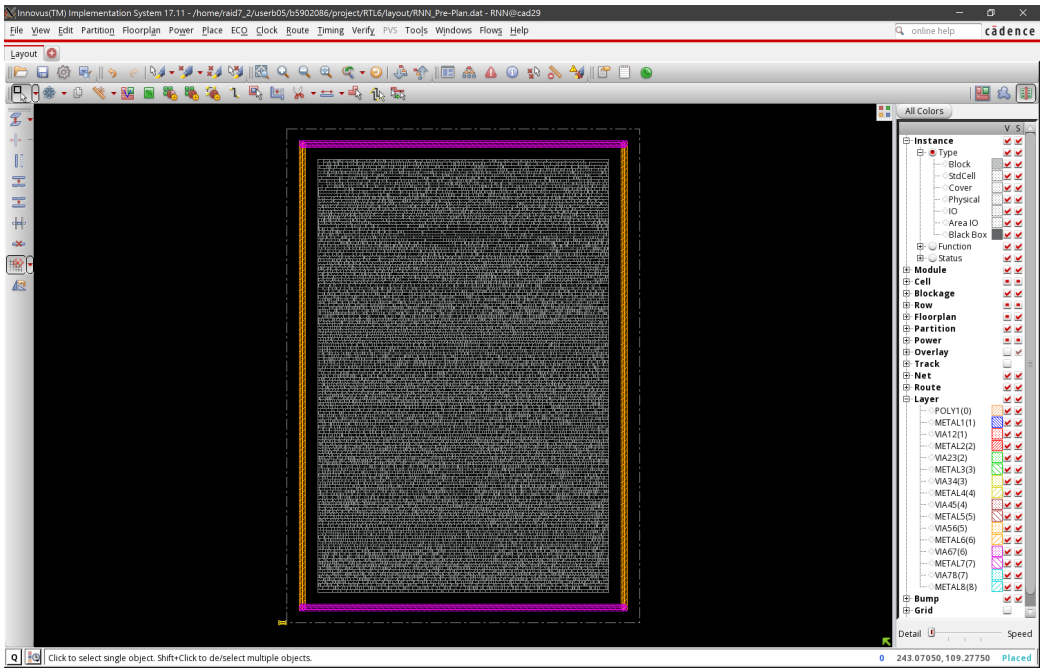
- Transistor-level Full placement



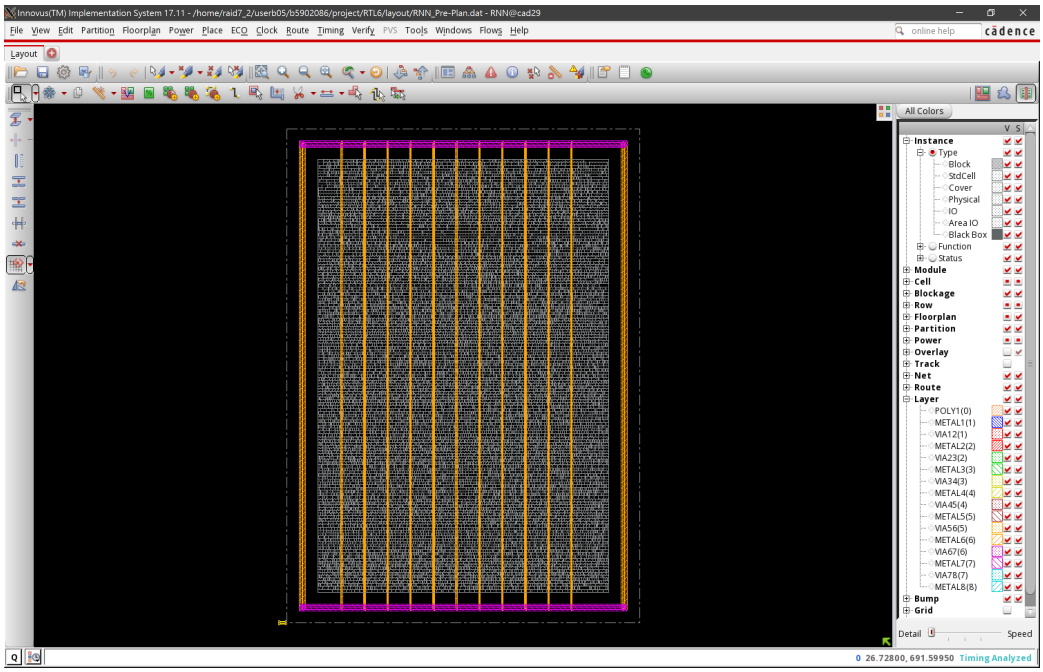




- Transistor-level Power Ring



- Transistor-level Power Stripe



```
b5902086@cad29:\~/project/RTL6/layout
ise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPESI-3014):  The RC network is incomplete for net mdata_w[8]. As a result, a lumped model will be used during delay calculation which may comprom
ise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (EMS-27):       Message (IMPESI-3014) has exceeded the current message display limit of 20.
To increase the message display limit, refer to the product command reference manual.
Total number of fetched objects 15223
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=3512.33 CPU=0:00:03.4 REAL=0:00:01.0)
End delay calculation (fullDC). (MEM=3512.33 CPU=0:00:03.7 REAL=0:00:01.0)
*** Done Building Timing Graph (cpu=0:00:04.7 real=0:00:02.0 totSessionCpu=0:23:05 mem=3512.3M)

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max av_scan_mode_max

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.195  |  0.195  |  0.455  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  2834   |  2790   |  2832   |
+--------------------+---------+---------+---------+


+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |     20 (60)      |   -0.321   |     20 (60)      |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 89.963%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 8.13 sec
Total Real time: 5.0 sec
Total Memory Usage: 3288.394531 Mbytes
innovus 5>
```

```
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**WARN: (IMPESI-3014):  The RC network is incomplete for net mdata_r[11]. As a result, a lumped model will be used during delay calculation which may compro
mise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPESI-3014):  The RC network is incomplete for net mdata_r[6]. As a result, a lumped model will be used during delay calculation which may comprom
ise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPESI-3014):  The RC network is incomplete for net mdata_r[5]. As a result, a lumped model will be used during delay calculation which may comprom
ise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPESI-3014):  The RC network is incomplete for net mdata_r[6]. As a result, a lumped model will be used during delay calculation which may comprom
ise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPESI-3014):  The RC network is incomplete for net mdata_r[4]. As a result, a lumped model will be used during delay calculation which may comprom
ise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPESI-3014):  The RC network is incomplete for net mdata_r[5]. As a result, a lumped model will be used during delay calculation which may comprom
ise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPESI-3014):  The RC network is incomplete for net mdata_r[2]. As a result, a lumped model will be used during delay calculation which may comprom
ise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (EMS-27):       Message (IMPESI-3014) has exceeded the current message display limit of 20.
To increase the message display limit, refer to the product command reference manual.
Total number of fetched objects 15223
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=3500.55 CPU=0:00:03.2 REAL=0:00:01.0)
End delay calculation (fullDC). (MEM=3500.55 CPU=0:00:03.4 REAL=0:00:01.0)
*** Done Building Timing Graph (cpu=0:00:04.3 real=0:00:01.0 totSessionCpu=0:23:22 mem=3500.5M)

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_min av_scan_mode_min

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.042  |  0.042  |  0.699  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  2834   |  2790   |  2832   |
+--------------------+---------+---------+---------+

Density: 89.963%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 6.16 sec
Total Real time: 3.0 sec
Total Memory Usage: 3260.210938 Mbytes
innovus 5>
```
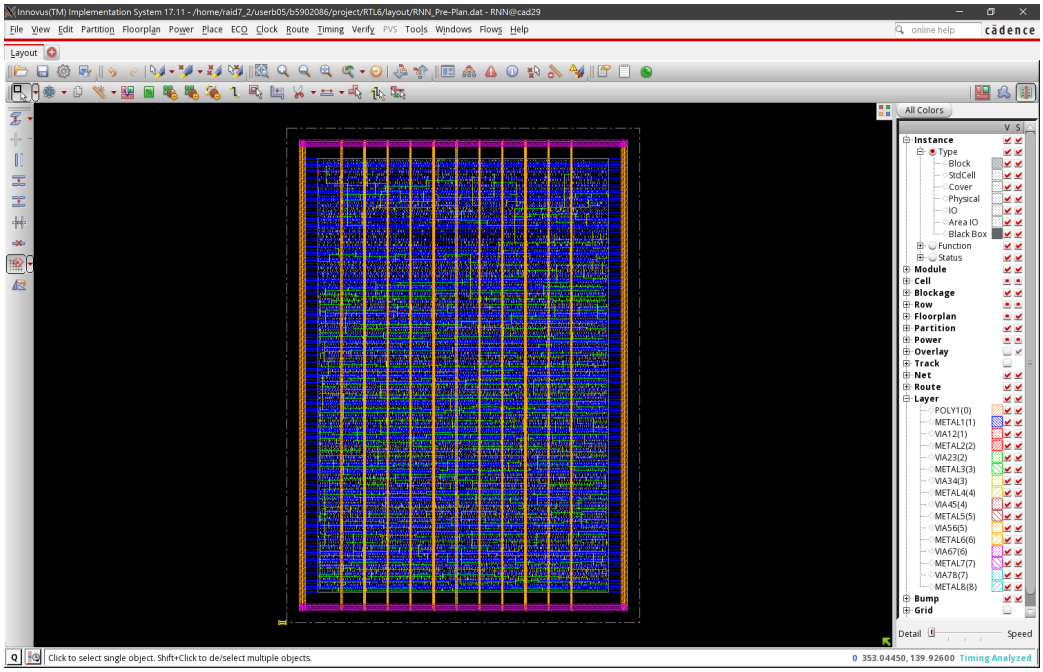
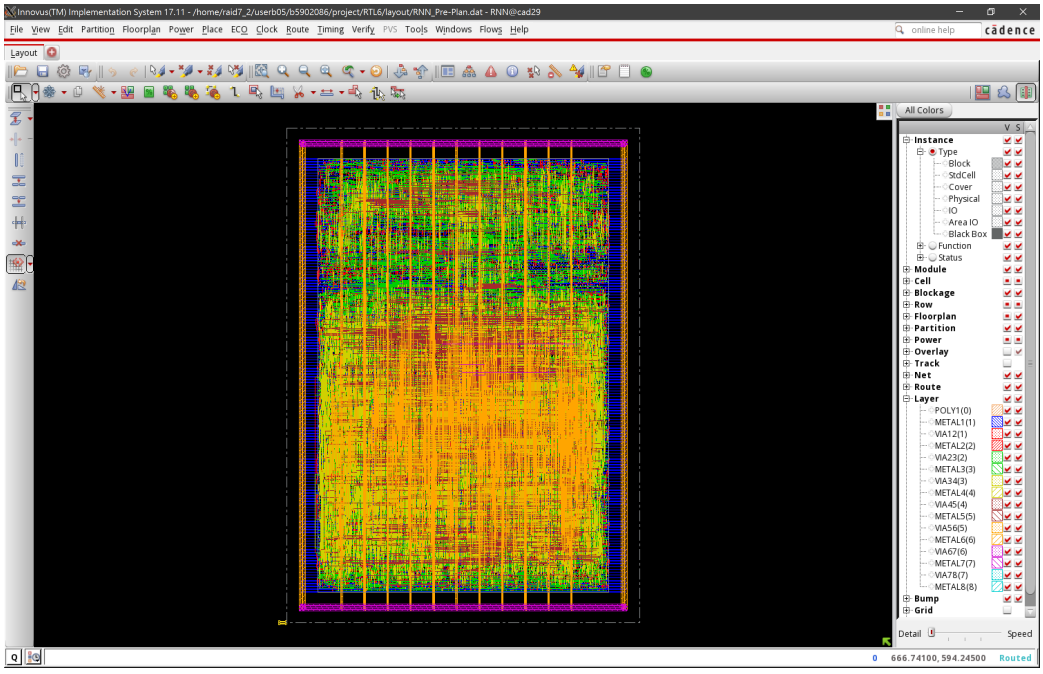

- Transistor-level Special Route



```
b5902086@cad29:\~/project/RTL6/layout

End Time: Tue Jun  9 22:42:34 2020
Time Elapsed: 0:00:01.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:01.3  MEM: 20.008M)

innovus 5> **WARN: (IMPTCM-125):        Option "-checkPinLayerForAccess" for command getPlaceMode is obsolete and will be ignored. It no longer has any effe
ct and should be removed from your script.
*** Starting refinePlace (0:23:29 mem=3336.5M) ***
Density distribution unevenness ratio = 1.980%
Move report: Detail placement moves 0 insts, mean move: 0.00 um, max move: 0.00 um
        Runtime: CPU: 0:00:00.4 REAL: 0:00:01.0 MEM: 3336.5MB
Summary Report:
Instances move: 0 (out of 14919 movable)
Instances flipped: 0
Mean displacement: 0.00 um
Max displacement: 0.00 um
Runtime: CPU: 0:00:00.6 REAL: 0:00:01.0 MEM: 3336.5MB
*** Finished refinePlace (0:23:30 mem=3336.5M) ***
Density distribution unevenness ratio = 1.980%
innovus 5> VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Tue Jun  9 22:42:54 2020

Design Name: RNN
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (460.0000, 644.9300)
Error Limit = 1000; Warning Limit = 50
Check specified nets
Use 4 pthreads

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Tue Jun  9 22:42:55 2020
Time Elapsed: 0:00:01.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:01.1  MEM: -2.000M)

innovus 5>
```

```
b5902086@cad29:\~/project/RTL6/layout
#Total wire length on LAYER METAL7 = 355 um.
#Total wire length on LAYER METAL8 = 0 um.
#Total number of vias = 103067
#Up-Via Summary (total 103067):
#
#-----------------------
# METAL1          50432
# METAL2          34708
# METAL3          13578
# METAL4           3127
# METAL5           1209
# METAL6             13
#-----------------------
#               103067
#
#detailRoute Statistics:
#Cpu time = 00:02:16
#Elapsed time = 00:00:38
#Increased memory = -7.03 (MB)
#Total memory = 1712.79 (MB)
#Peak memory = 1954.30 (MB)
#
#globalDetailRoute statistics:
#Cpu time = 00:02:53
#Elapsed time = 00:01:08
#Increased memory = -15.16 (MB)
#Total memory = 1688.33 (MB)
#Peak memory = 1954.30 (MB)
#Number of warnings = 22
#Total number of warnings = 114
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Tue Jun  9 22:45:23 2020
#
#routeDesign: cpu time = 00:02:53, elapsed time = 00:01:08, memory = 1688.34 (MB), peak = 1954.30 (MB)

*** Summary of all messages that are not suppressed in this session:
Severity  ID               Count  Summary
WARNING   IMPEXT-3493          1  The design extraction status has been re...
WARNING   IMPEXT-3530          1  The process node is not set. Use the com...
WARNING   IMPCK-8086           1  The command %s is obsolete and will be r...
WARNING   IMPESI-3014         64  The RC network is incomplete for net %s....
WARNING   TCLCMD-1403          1  '%s'
*** Message Summary: 68 warning(s), 0 error(s)

innovus 5>
```

- Transistor-level Nano Route



```
b5902086@cad29:\~/project/RTL6/layout
Calculate late delays in OCV mode...
Start delay calculation (fullDC) (4 T). (MEM=3729.42)
Glitch Analysis: View av_func_mode_max -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_max -- Total Number of Nets Analyzed = 15239.
Total number of fetched objects 15239
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 15276,  0.4 percent of the nets selected for SI analysis
End delay calculation. (MEM=3729.42 CPU=0:00:00.3 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=3729.42 CPU=0:00:00.3 REAL=0:00:00.0)

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.001  |  0.009  |  0.001  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  2834   |  2790   |  2832   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 90.176%
Total number of glitch violations: 0
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 18.25 sec
Total Real time: 11.0 sec
Total Memory Usage: 3463.394531 Mbytes
Reset AAE Options
innovus 6>
```

```
b5902086@cad29:\~/project/RTL6/layout
End delay calculation. (MEM=3695.37 CPU=0:00:08.0 REAL=0:00:02.0)
End delay calculation (fullDC). (MEM=3695.37 CPU=0:00:08.9 REAL=0:00:03.0)
Loading CTE timing window with TwFlowType 0...(CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 3695.4M)
Add other clocks and setupCteToAAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.2, REAL = 0:00:01.0, MEM = 3695.4M)
Starting SI iteration 2
Calculate late delays in OCV mode...
Calculate early delays in OCV mode...
Calculate late delays in OCV mode...
Calculate early delays in OCV mode...
Start delay calculation (fullDC) (4 T). (MEM=3703.44)
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 98.
Glitch Analysis: View av_scan_mode_min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_scan_mode_min -- Total Number of Nets Analyzed = 98.
Total number of fetched objects 15239
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 15276,  0.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=3703.44 CPU=0:00:00.2 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=3703.44 CPU=0:00:00.3 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:12.4 real=0:00:05.0 totSessionCpu=0:31:58 mem=3703.4M)

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_min av_scan_mode_min

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.541  |  0.541  |  0.704  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  2834   |  2790   |  2832   |
+--------------------+---------+---------+---------+

Density: 90.176%
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 17.77 sec
Total Real time: 10.0 sec
Total Memory Usage: 3414.867188 Mbytes
Reset AAE Options
innovus 6>
```

- Transistor-level Pass

```
b5902086@cad29:\~/project/RTL6


Warning!  Timing violation
          $setuphold<hold>( posedge CK &&& (flag == 1):5850 PS, negedge D:5777 PS,  0.255 : 255 PS,  -0.066 : -66 PS );
           File: ./syn/tsmc13_neg.v, line = 18064
          Scope: testfixture.u_RNN.\mul_00_reg[4]
           Time: 5862 PS


Warning!  Timing violation
          $setuphold<hold>( posedge CK &&& (flag == 1):5850 PS, negedge D:5776 PS,  0.255 : 255 PS,  -0.071 : -71 PS );
           File: ./syn/tsmc13_neg.v, line = 18064
          Scope: testfixture.u_RNN.\mul_00_reg[2]
           Time: 5863 PS


Warning!  Timing violation
          $setuphold<hold>( posedge CK &&& (flag == 1):5850 PS, negedge D:5771 PS,  0.258 : 258 PS,  -0.069 : -69 PS );
           File: ./syn/tsmc13_neg.v, line = 18064
          Scope: testfixture.u_RNN.\mul_31_reg[4]
           Time: 5863 PS


Warning!  Timing violation
          $setuphold<hold>( posedge CK &&& (flag == 1):5850 PS, negedge D:5767 PS,  0.259 : 259 PS,  -0.076 : -76 PS );
           File: ./syn/tsmc13_neg.v, line = 18064
          Scope: testfixture.u_RNN.\mul_22_reg[3]
           Time: 5869 PS

busy==1

-----------------------------------------------------

--------------------- S U M M A R Y -----------------

Congratulations! All data have been generated successfully! The result is PASS!!

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Simulation complete via $finish(1) at time 4976057763 PS + 0
./testfixture.v:171       #(`CYCLE/2); $finish;
ncsim> exit

(10 min 50 s) Tue Jun 09 23:51:23
(3)#~/project/RTL6
(CAD)b5902086@cad29:[0]$ ncverilog  testfixture.v  layout/RNN_APR.v -v syn/tsmc13_neg.v  +define+SDF +ncmaxdelays
```