

Final project - Recurrent Unit Circuit Design

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1. 設計取捨

- 一開始花了一段時間考慮要把哪些權重主動儲存在 circuit 上面，而因為最後計算的結果是看 AT 值(面積 \times cycle 數 \times cycle time)，如果把所有權重資料都存在 circuit 上，雖然會使得總 cycle 數量變很低，但是會導致節省下來的 cycle 數量的倍率跑到面積上面，而這樣會導致 circuit 過大，很難壓 cycle time。因此最後是選擇所有資料都重新讀取。
- 雖然原本以為把 B_{ih} 及 B_{hh} 放在 Circuit 上可以用少量的 area 換取一些 cycle 數上的節省，但是實際上實作後發現為了存 B_{ih} 及 B_{hh} 會導致多用了大約一半面積，反而得不償失，而 cycle 數只少了 $\frac{1}{64}$ 左右。

2. Stage

- ~~一開始仔細思考之後，會發現基本上只要依照讀六種不同 memory 的位置來切狀態即可完成，並且會在其中的五個狀態中重複循環。(後來為了 pipeline 和編號的方便，因此改成八個狀態)~~

3. 乘法器

- 在寫之前就有預想到乘法部分會變成 critical path，而實際用 design compiler 跑下去結果也是如此。因此使用 booth algorithm 把他變成幾個數字的加法，然後把加總的部分使用 pipeline 來處理，這樣就能壓低 cycle time。

4. Pipeline

- ~~盡量把大步驟拆成多個小步驟，然後盡量把小步驟均勻的分散到每個 state 中，使得每個 state 的執行時間都差不多，就能達到 pipeline 的效果，並壓低 cycle time。(盡量把所有的 delay 超過兩次 40bit 加法的運算都拆開變成多級的 pipeline，然後盡量讓資料輸入的當個 cycle 不要做額外的運算，只把資料存到 register 中，下個 cycle 才開始運算，並且在輸出前加入幾個 stall，讓運算有時間算完)~~

5. 讀寫優化

- ~~盡量讓每個 register 寫入之後都不要在同個 cycle 中去讀他，可以讓 compiler 更容易的優化這種東西。(後來直接把所有的 = 都換成 <=)~~

6. 乘法和加法單元

- ~~因為乘法和加法的部份仍然容易成為 critical path，因此把乘法和加法的部分拉到外面變成單獨一塊，這樣計算乘法和加法前就不需要 stage 等等的判斷。(後來的設計中，已經把幾乎所有的東西都從 stage 的判斷中拉出去了，這樣可以減少 stage 所造成的 delay)~~

7. Transistor-level 合成

- Transistor-level 合成的時候，在 nano Route 這個階段的時候，如果 WNS 不夠大，innovus 會直接 crash。後來發現的解決方法是事先先執行 ECO Design，然後到 Mode 裡面把 Thresholds 裡的 Setup Slack 提高，這樣就能讓 WNS 變成正比較大的值，而不是 0.000 附近。這樣之後就能順利的讓 nano Route 不會 crash 了。

8. Cycle time

- 這個 verilog 在 Gate-Level 合成的時候，用 2ns 當 cycle time 也能合成的出來 (timing 可以得到 MET)，但是拿去模擬的時候就會出現問題，而看起來主要都是

hold time violation，但是因為找不到解決的方式，最後只能把 cycle time 調整成 3.0 ns 才不會出錯。

9. 合成參數

- Gate-Level
 - Cycle time: 3.0 ns
 - Transistor-Level
 - Cycle time: 3.0 ns

10. 結果

- Gate-level results
 - Can you pass gate-level simulation?
 - yes
 - Cycle time that can pass your gate-level simulation:
 - 3.0 ns
 - Total simulation time:
 - 3904540.036 ns
 - Total cell area:
 - $146197.063362 \mu\text{m}^2$
 - Cell area \times Simulation time:
 - $570832287042.5577 \mu\text{m}^2 \cdot \text{ns}$
 - Transistor-level results
 - Can you pass transistor-level simulation?
 - yes
 - Cycle time that can pass your transistor-level simulation:
 - 3.0 ns
 - Total simulation time:
 - 3904539.831 ns
 - Total cell area:
 - $154015.286 \mu\text{m}^2$
 - Cell area \times Simulation time:
 - $601358818769.8566 \mu\text{m}^2 \cdot \text{ns}$

11. 截圖

- ## ◦ RTL Pass

```
(8 ms) Sun Jun 21 00:29:28
(16) #~/project/RTL7
(CAD)b5902086@cad30:[0]$ ncverilog testfixture.v RNN.v
ncverilog: 15.20-5039: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
Loading snapshot worklib.testfixture:v ..... Done
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
ncsim: "#DVEACC: some objects excluded from $dumpvars due to access restrictions, use +access+r on command line for access to all objects
      File: ./testfixture.v, line = 74, pos = 9
      Scope: testfixture
      Time: 0 FS + 0

-----
START!!! Simulation Start .....
-----
-----
-----
----- S U M M A R Y -----
Congratulations! All data have been generated successfully! The result is PASS!!

-----
Simulation complete via $finish(1) at time 3904539 NS + 0
./testfixture.v:171      #(`CYCLE/2); $finish;
ncsim> exit

(14.8 s) Sun Jun 21 00:29:45
(17) #~/project/RTL7
(CAD)b5902086@cad30:[0]$
```

o Gate-level Area Report

```
b5902086@cad30:~/project/RTL7
*****
Report : area
Design : RNN
Version: N-2017.09-SP2
Date : Sat Jun 20 16:03:11 2020
*****
Library(s) Used:
    slow (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/slow.db)

Number of ports:          98
Number of nets:           9408
Number of cells:          9329
Number of combinational cells: 6231
Number of sequential cells: 3108
Number of macros/black boxes: 0
Number of buf/inv:         965
Number of references:     156

Combinational area:      54238.719820
Buf/Inv area:            5866.214410
Noncombinational area:   91958.344341
Macro/Black Box area:    0.000000
Net Interconnect area:  1127052.545288

Total cell area:         146197.063362
Total area:              1273249.608650

Hierarchical area distribution
-----

```

Hierarchical cell	Global cell area	local cell area				
	Absolute Total	Percent Total	Combi-national	Noncombi-national	Black-boxes	Design
RNN	146197.0634	100.0	54238.7190	91958.3443	0.0000	RNN
Total			54238.7190	91958.3443	0.0000	

```
1
(20 ms) Sun Jun 21 00:31:37
(19)#/~/project/RTL7
(CAD)b5902086@cad30:[0]$ cat syn/RNN_syn.area.rpt
```

o Gate-level Timing Report

```
b5902086@cad30:~/project/RTL7
Startpoint: adder_d_reg[0][14]
(rising edge-triggered flip-flop clocked by clk)
Endpoint: adder_00_reg[17]
(rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port      Wire Load Model      Library
RNN                tsmc13_wl10        slow

Point                  Incr      Path
-----
```

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.50	0.50
adder_d_reg[0][14]/CK (DFFQX1)	0.00 #	0.50 r
adder_d_reg[0][14]/Q (DFFQX1)	0.52	1.02 r
U6685/Y (NAND2X1)	0.34	1.35 f
U6687/Y (OA12X2)	0.37	1.73 r
U4413/Y (NOTX1)	0.20	1.93 f
U4414/Y (OA12X1L)	0.44	2.37 r
U4411/Y (AO12X1L)	0.24	2.62 f
U6883/Y (OA12X1)	0.23	2.84 r
U6884/Y (XNOR2X1)	0.28	3.12 f
adder_00_reg[17]/D (DFFQX1)	0.00	3.12 f
data arrival time		
slack (MET)	0.00	

```
1
(56 ms) Sun Jun 21 00:32:33
(20)#/~/project/RTL7
(CAD)b5902086@cad30:[0]$
```

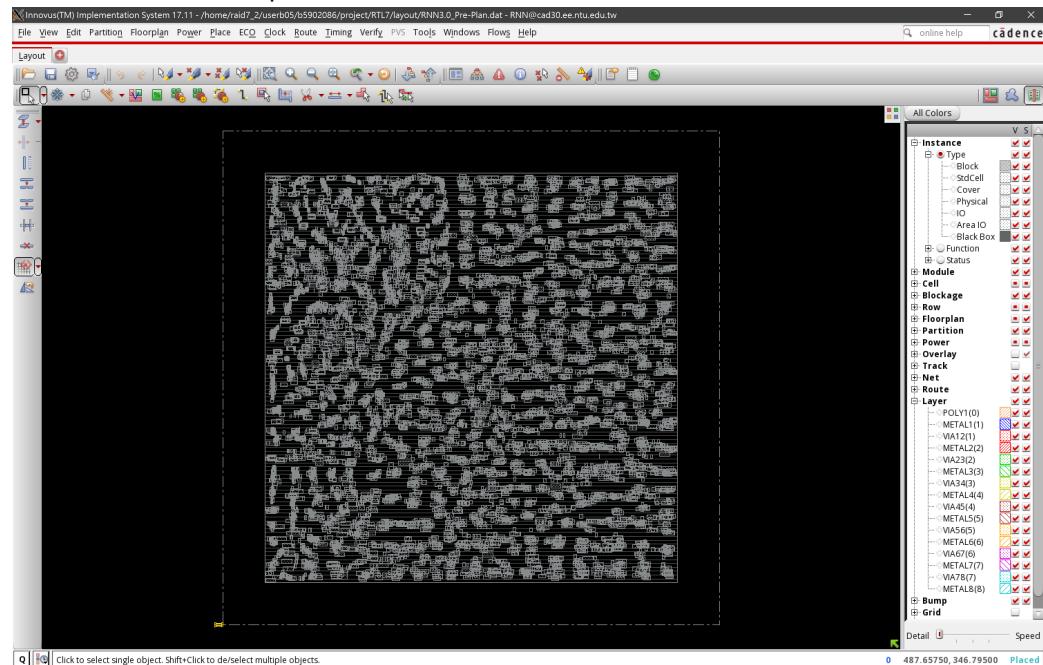
o Gate-level Pass

```
b5902086@cad30:~/project/RTL7
(5 ms) Sun Jun 21 00:33:47
(22) #~/project/RTL7
(CAD)b5902086@cad30:[0]$ ncverilog testfixture.v RNN_syn.v -v syn/tsmc13_neg.v +define+SDF
ncverilog: 15.20-s039; (c) Copyright 1995-2017 Cadence Design Systems, Inc.
Loading snapshot worklib.testfixture..... Done
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
ncsim: #,DVXACCI: some objects excluded from $dumpvars due to access restrictions, use +access+r on command line for access to all objects.
      File: ./testfixture.v, line = 74, pos = 9
      Scope: testfixture
      Time: 0 FS + 0

-----
START!!! Simulation Start .....
-----
-----
----- S U M M A R Y -----
Congratulations! All data have been generated successfully! The result is PASS!!

-----
Simulation complete via $finish(1) at time 3994540036 PS + 0
./testfixture.v:171      #(`CYCLE/2); $finish;
ncsim> exit
(7 min 22 s) Sun Jun 21 00:41:11
(23) #~/project/RTL7
(CAD)b5902086@cad30:[0]$
```

o Transistor-level Floorplan



```

b5902086@cad30:~/project/RTL7/layout$ timeDesignSummary
# Design Name: RNN
# Design Mode: 20nm
# Analysis Mode: MMIC Non-OCV
# Parasitic Mode: No SPEF/RCDB
# Signoff Settings: SI OFF
#####
Calculate delays in BcKc mode.
Start delay calculation (fullDC) (32 T). (MEM=3417.55)
AAE DB initialization (MEM=3446.3 CPU=0:00:00.1 REAL=0:00:00.0)
AAE_INFO: Cdb files are:
        /home/raid7_2/userb05/b5902086/project/RTL7/layout/RNN3.0_Pro-Plan.dat/libs/mmmc/slow.cdb
        /home/raid7_2/userb05/b5902086/project/RTL7/layout/RNN3.0_Pro-Plan.dat/libs/mmmc/fast.cdb

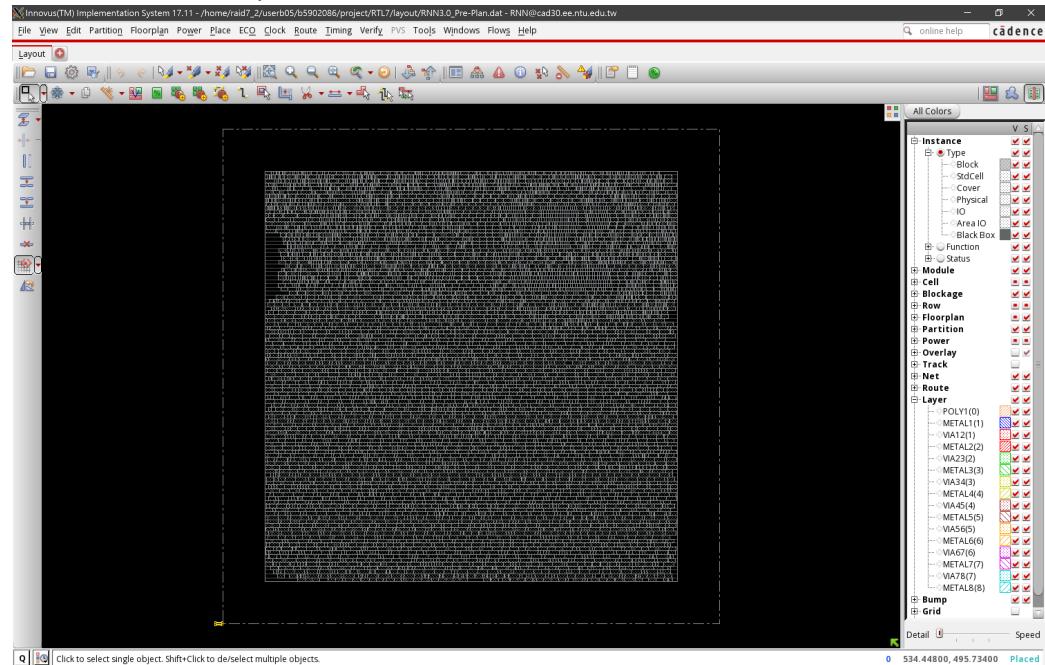
Total number of fetched objects 10550
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=5637.44 CPU=0:00:01.8 REAL=0:00:01.0)
End delay calculation (fullDC). (MEM=5480.07 CPU=0:00:04.0 REAL=0:00:03.0)
*** Done Building Timing Graph (cpu=0:00:05.2 real=0:00:04.0 totSession(cpu=0:55:26 mem=3782.1M)

timeDesign Summary
-----
Setup views included:
av_func_mode_max

Setup mode      +---+ +---+ +---+
|    all |    regZreg | default |
+---+ +---+ +---+
|      WNS (ns): 0.754 | 0.754 | 0.854 |
|      TNS (ns): 0.000 | 0.000 | 0.000 |
| Violating Paths: 0 | 0 | 0 |
| All Paths: 4285 | 4189 | 128 |
+---+ +---+ +---+ +---+ +---+ +---+ +---+
Density: 94.924%
-----
Set Using Default Delay Limit as 1000.
Resetting back High Fanout Nets as non-ideal
Set Default Net Delay as 1000 ps.
Set Default Net Load as 0.5 pF.
Reported timing to dlr timingReports
Total CPU time: 7.6 sec
Total Real time: 4.0 sec
Total Memory Usage: 3553.863281 Mbytes
innovus 7>

```

○ Transistor-level Full placement



```
b5902086@cad30:/project/RIL7/layout
timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPESSI-3014): The RC network is incomplete for net maddr[12]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPESSI-3014): The RC network is incomplete for net maddr[3]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
Total number of fetched objects 10566
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=5717.26 CPU=0:00:02.1 REAL=0:00:01.8)
End delay calculation (fullDC). (MEM=5561.89 CPU=0:00:04.2 REAL=0:00:03.0)
*** Done Building Timing Graph (cpu=0:00:05.3 real=0:00:03.0 totSessionCpu=0:57:57 mem=3906.0M)

----- timeDesign Summary -----
----- Setup views included: av_func_mode_max ----



| Setup mode       | all   | reg2reg | default |
|------------------|-------|---------|---------|
| WNS (ns):        | 0.323 | 0.323   | 0.644   |
| TNS (ns):        | 0.000 | 0.000   | 0.000   |
| Violating Paths: | 0     | 0       | 0       |
| All Paths:       | 4285  | 4189    | 128     |

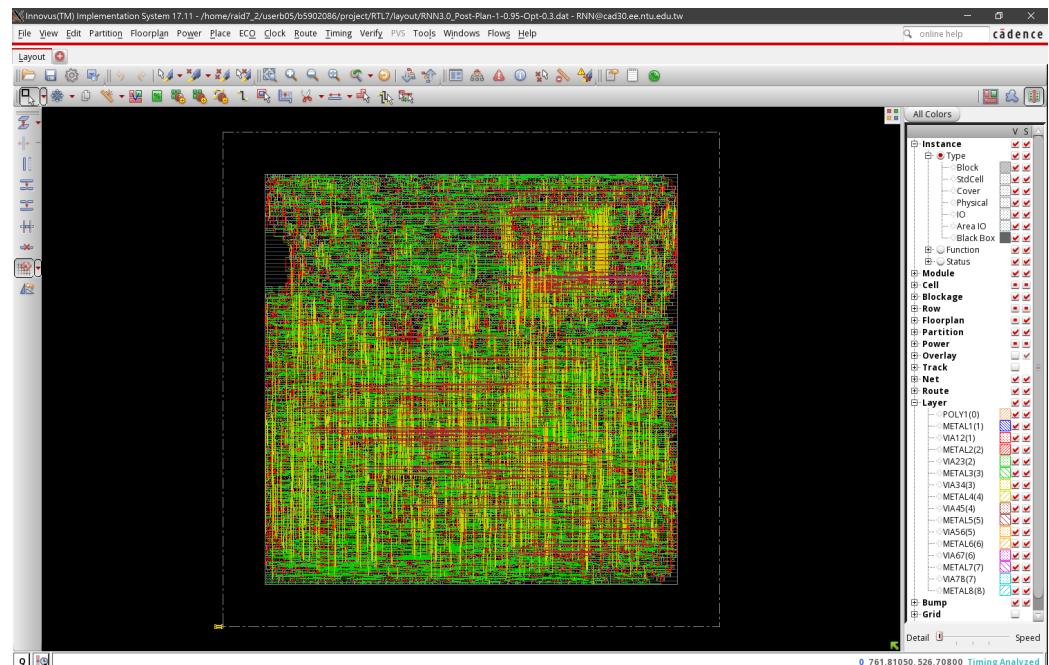


| DRVs       | Real           |           | Total          |
|------------|----------------|-----------|----------------|
|            | Nr nets(terms) | Worst Vto | Nr nets(terms) |
| max_cap    | 0 (0)          | 0.000     | 0 (0)          |
| max_tran   | 0 (0)          | 0.000     | 0 (0)          |
| max_fanout | 0 (0)          | 0         | 0 (0)          |
| max_length | 0 (0)          | 0         | 0 (0)          |

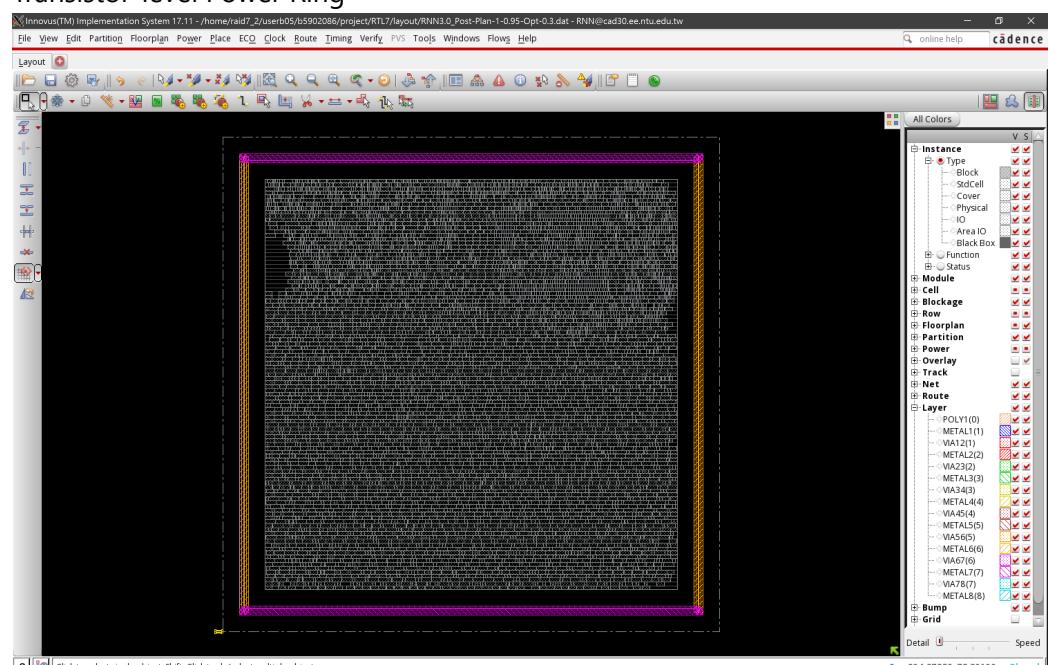


Density: 95.540%
Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports
Total CPU time: 8.24 sec
Total Real time: 6.6 sec
Total Memory Usage: 3914.996094 Mbytes
innovus >
```



◦ Transistor-level Power Ring



- Transistor-level Power Stripe

Innovus(TM) Implementation System 17.11 - /home/rajd7_2/userb05/b590286/project/RTL7/layout/RNN3_0_Post_Plan-1-0.95-Opt-0.3.dat - RNN@cad30.ee.ntu.edu.tw

File View Edit Partition Floorplan Power Place FCO Clock Route Timing Verify PVS Tools Windows Flows Help online help

cadence

Layout

Instance Type: Block, StdCell, Cover, Physical, IO, Bus, ID, Black Box, Function, Status

Module: Cell, Package, Row, Floorplan, Partition, Power, Overlay, Track, Net, Route, Layer: POLY1(0), METAL1(1), VIA1(2), VIA1L(2), VIA2(2), METAL2(3), VIA3(3), METAL3(3), VIA4(3), METAL4(4), VIA5(4), METAL5(5), VIA6(5), METAL6(6), VIA7(6), METAL7(7), VIA8(7), METAL8(8), Burn, Grid

All Colors

V S

Click to select single object. Shift+Click to select multiple objects.

0 396.05350, 253.87300 Placed

```
b590286@cad30:~/project/RTL7/layout
Non-Default Mode Option Settings :
  NONE
**WARN: (IMPPG-4055): The run time of addStripe will degrade with multiple cpu setting according to the number of stripe sets, ignore the setting of setMultiCpuUsage in addStripe.
Stripe generation is complete.
Vias are now being generated.
addStripe created 24 wires.
ViaGen created 96 vias, deleted 0 via to avoid violation.
+-----+
| Layer | Created | Deleted |
+-----+
| METAL6 |    24   |      0 |
| VIA67  |    96   |      0 |
+-----+
innovus 7> *** Starting Verify Geometry (MEM: 3935.0) ***
**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future release. Please update your script to use the new command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
bin size: 8320
**WARN: (IMPVFG-198): Area to be verified is small to see any runtime gain from multi-cpus. Use setMultiCpuUsage command to adjust the number of CPUs.
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
M: elapsed time: 6.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.
*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:05.4 MEM: 89.6M)
innovus 7> 

b590286@cad30:~/project/RTL7/layout
se timing analysis. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPESI-3014): The RC network is incomplete for net msel[0]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
**WARN: (IMPESI-3014): The RC network is incomplete for net maddr[12]. As a result, a lumped model will be used during delay calculation which may compromise timing accuracy. To resolve this, check parasitics for completeness, re-extraction may be required.
Total number of fetched objects 10566
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=5760.21 CPU=0:00:02.2 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=5760.21 CPU=0:00:02.4 REAL=0:00:01.0)
*** Done Building Timing Graph (cpu=0:00:03.3 real=0:00:01.0 totSessionCpu=0:58:23 mem=3928.7M)

timeDesign Summary
-----
Setup views included:
av_func_mode_max



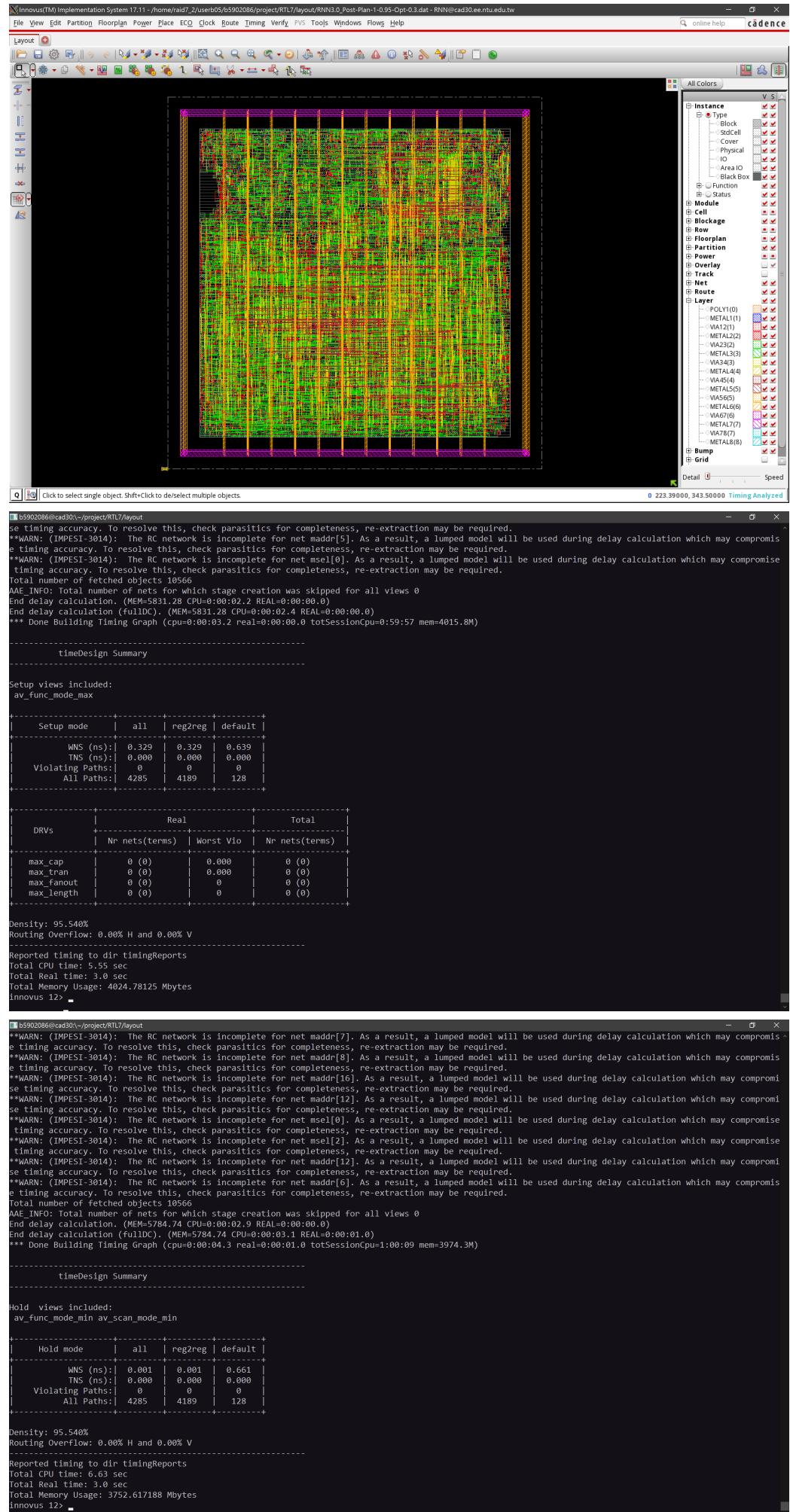
| Setup mode       | all   | reg2reg | default |
|------------------|-------|---------|---------|
| WNS (ns)         | 0.329 | 0.329   | 0.645   |
| TNS (ns)         | 0.000 | 0.000   | 0.000   |
| Violating Paths: | 0     | 0       | 0       |
| All Paths:       | 4285  | 4189    | 128     |



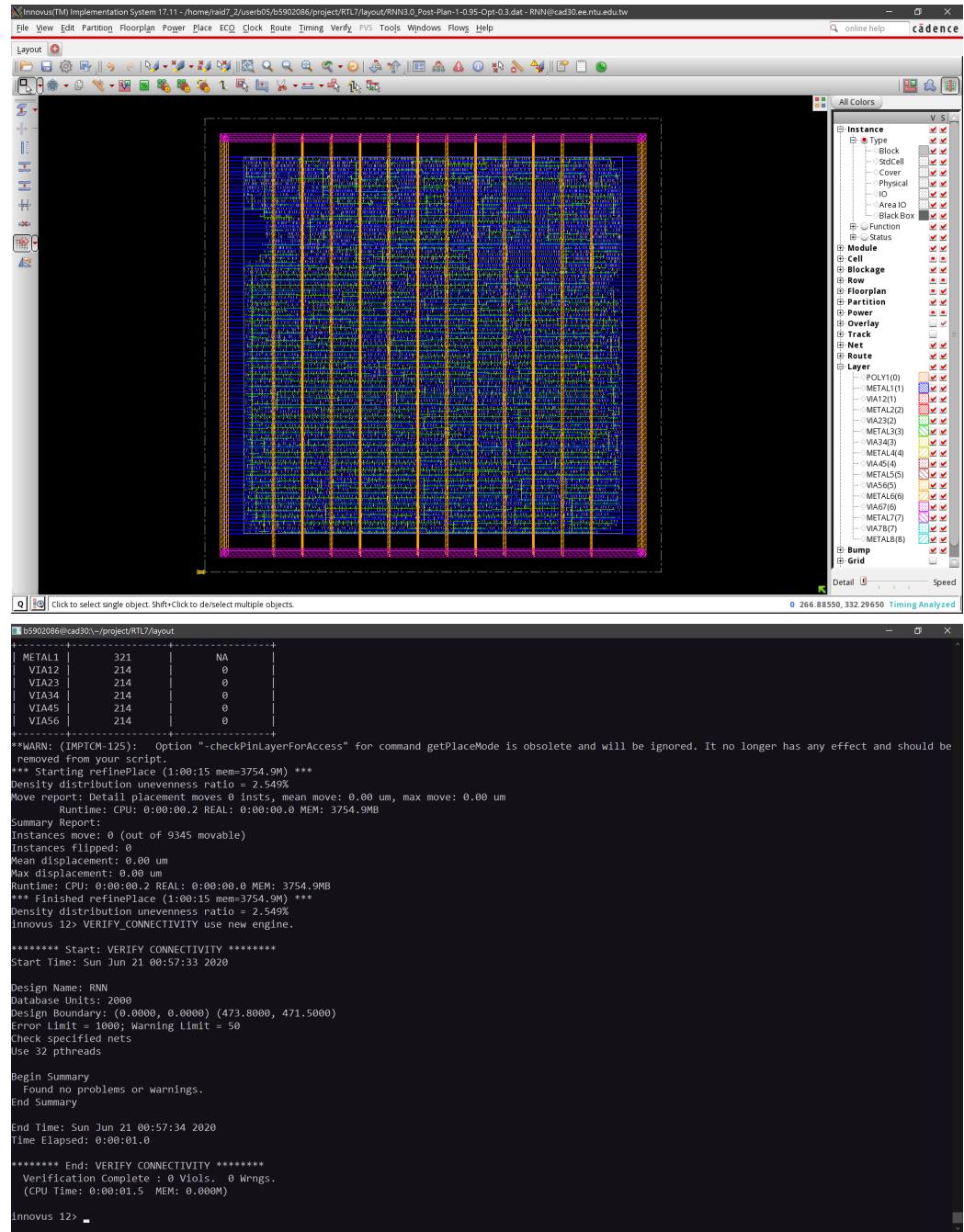
| DRVs       | Real            | Total     |                 |
|------------|-----------------|-----------|-----------------|
|            | Nr nets(termss) | Worst Vio | Nr nets(termss) |
| max_cap    | 0 (0)           | 0.000     | 0 (0)           |
| max_tran   | 0 (0)           | 0.000     | 0 (0)           |
| max_fanout | 0 (0)           | 0         | 0 (0)           |
| max_length | 0 (0)           | 0         | 0 (0)           |


Density: 95.540%
Routing Overflow: 0.00% H and 0.00% V
Reported timing to dir timingReports
Total CPU time: 6.45 sec
Total Real time: 3.0 sec
Total Memory Usage: 3927.714844 Mbytes
```

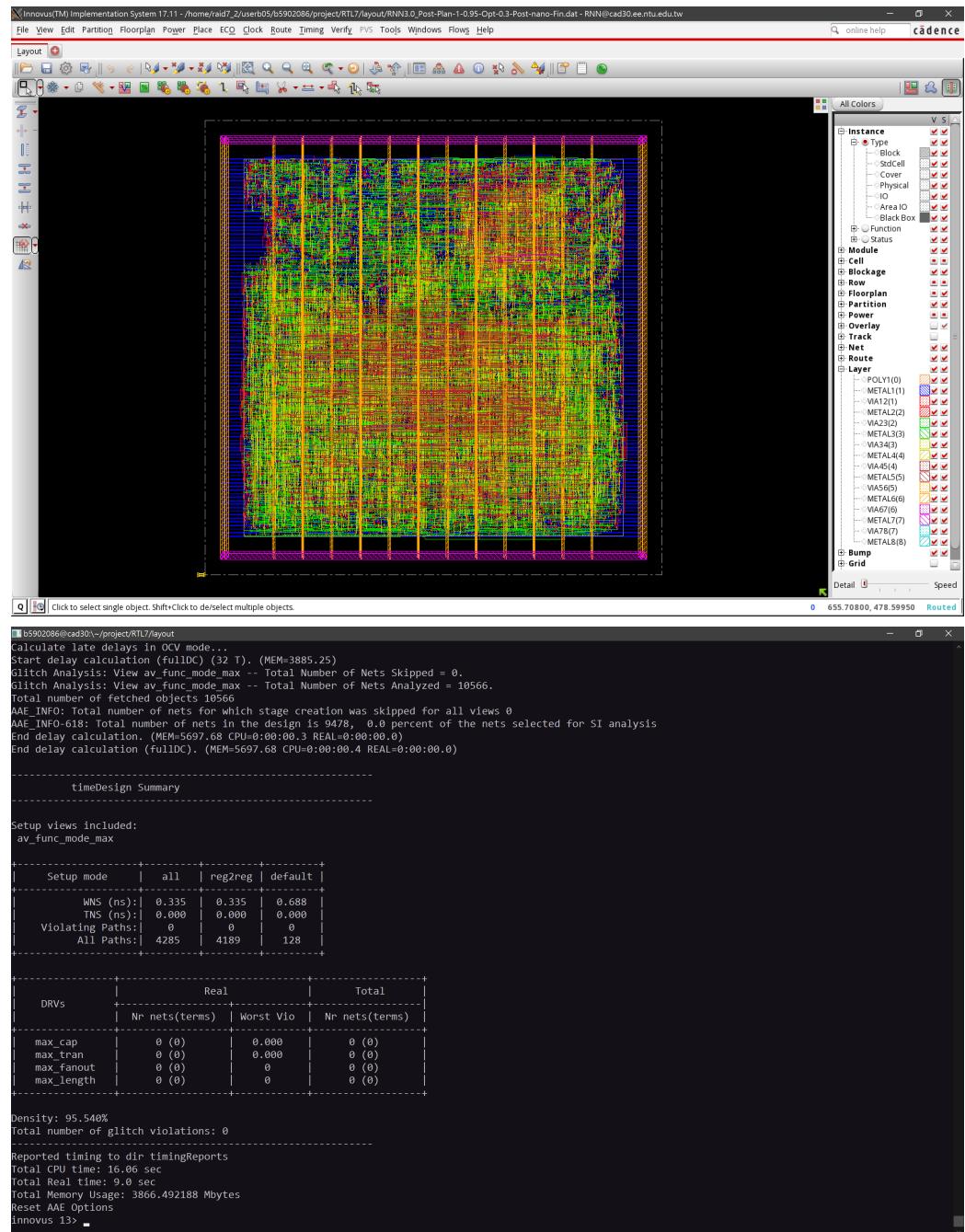
- Transistor-level CTS



- Transistor-level Special Route



- Transistor-level Nano Route



```

[1 b5902086@cad30:~/project/RTL7/layout]
End delay calculation. (MEM=5781.96 CPU=0:00:06.0 REAL=0:00:01.0)
End delay calculation (fullDC) (MEM=5781.96 CPU=0:00:06.0 REAL=0:00:01.0)
Loading CTE timing window with TwFlowType 0...(CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 3944.4M)
Add other locks and setup t0AAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.2, REAL = 0:00:00.0, MEM = 3944.4M)
Starting ST Iteration 2
Calculate late delays in OCV mode...
Calculate early delays in OCV mode...
Calculate late delays in OCV mode...
Calculate early delays in OCV mode...
Start delay calculation (fullDC) (32 T). (MEM=3953.47)
Glitch Analysis: View av_func mode min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func mode min -- Total Number of Nets Analyzed = 98.
Glitch Analysis: View av_scan mode min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_scan mode min -- Total Number of Nets Analyzed = 98.
Total number of fetched objects: 10566
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 9478. 0.0 percent of the nets selected for ST analysis
End delay calculation. (MEM=5765.89 CPU=0:00:00.2 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=5765.89 CPU=0:00:00.3 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:10.1 real=0:00:03.0 tottSessionCpu=1:01:10 mem=5765.9M)

-----
timeDesign Summary
-----

Hold views included:
av_func_mode_min av_scan_mode_min

+-----+-----+-----+
| Hold mode | all | regRreg | default |
+-----+-----+-----+
| WNS (ns): | 0.001 | 0.001 | 0.772 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 4285 | 4189 | 128 |
+-----+-----+-----+
Density: 95.540%
Reported timing to dir timingReports
Total CPU time: 14.02 sec
Total Real time: 5.0 sec
Total Memory Usage: 3741.460938 Mbytes
Reset AAE Options
innovus 13>

[1 b5902086@cad30:~/project/RTL7/layout]
+-----+-----+-----+
| WNS (ns): | 0.001 | 0.001 | 0.772 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 4285 | 4189 | 128 |
+-----+-----+-----+
Density: 95.540%
Reported timing to dir timingReports
Total CPU time: 14.02 sec
Total Real time: 5.0 sec
Total Memory Usage: 3741.460938 Mbytes
Reset AAE Options
innovus 13> *** Starting Verify Geometry (MEM: 3741.5) ***
**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future release. Please update your script to use the new command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 8320
**WARN: (IMPVFG-198): Area to be verified is small to see any runtime gain from multi-cpus. Use setMultiCpuUsage command to adjust the number of CPUs.
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 10.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.
*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:10.1 MEM: 208.6M)
innovus 13>

```

○ Transistor-level Summary

```

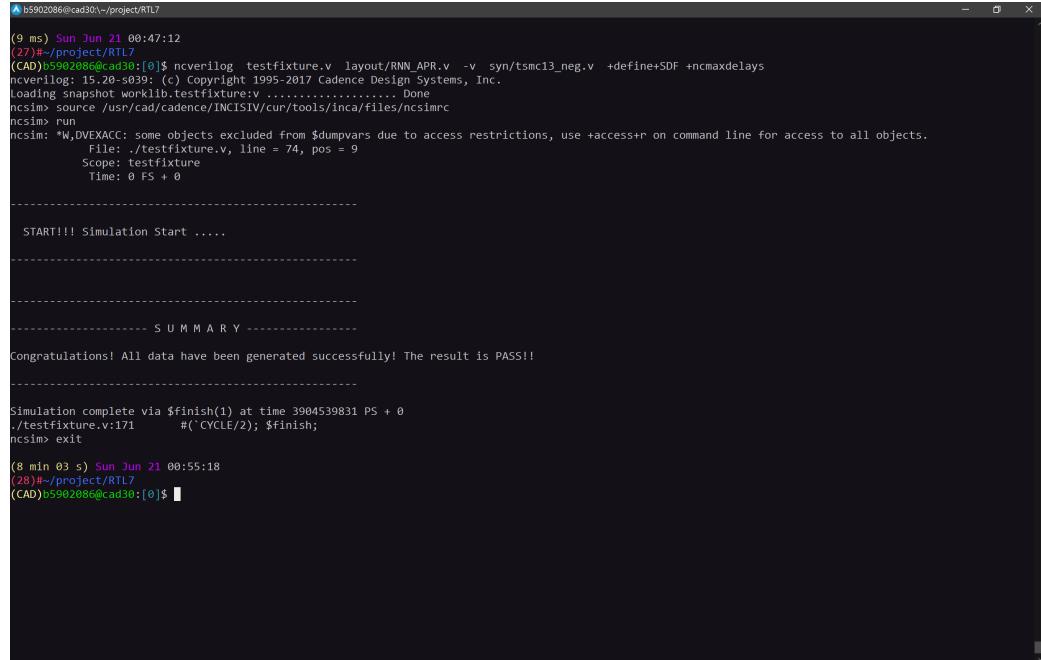
[1 b5902086@cad30:~/project/RTL7/layout]
BUFX12 1.023840
BUFX12 1.023840
BUFX8 0.682560
BUFX8 0.682560
BUFX6 0.511920
BUFX6 0.511920
BUF4 0.341280
BUF4 0.341280
BUF3 0.259680
BUF3 0.259680
BUF2 0.170640
BUF2 0.170640 1054
# Cells in lib with max_fanout: 0
SDC max_cap: N/A
SDC max_tran: N/A
SDC max_fanout: N/A
Default Ext. Scale Factor: 1.000
Detail Ext. Scale Factor: 1.000

=====
Floorplan/Placement Information
=====
Total area of Standard cells: 147145.909 um^2
Total area of Standard cells(Subtracting Physical Cells): 147145.909 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 154015.286 um^2
Total area of Chip: 223396.700 um^2
Effective Utilization: 9.5540e-01
Number of Cell Rows: 106
% Pure Gate Density #1 (Subtracting BLOCKAGES): 95.540%
% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 95.540%
% Pure Gate Density #3 (Subtracting MACROS): 95.540%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 95.540%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 95.540%
% Pure Gate Density #6 ((Unplaced Standard Inst + Unplaced Block Inst + Unplaced Black Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area)) for Insts where they are placed: 95.540%
% Core Density (Counting Std Cells and MACROs): 95.540%
% Core Density #2(Subtracting Physical Cells): 95.540%
% Chip Density (Counting Std Cells and MACROs and IOs): 65.868%
% Chip Density #2(Subtracting Physical Cells): 65.868%
# Macros within 5 sites of IO pad: No
Macro halo defined?: No

"summaryReport.rpt" 5432L, 230874C
5390,37 99%

```

- Transistor-level Pass



```
(9 ms) Sun Jun 21 00:47:12
(27)#/~/project/RTL7
(CAD)b5902086@cad30:[0]$ ncverilog testfixture.v layout/RNN_AP.RV -v syn/tsmc13_neg.v +define+SDF +ncmaxdelays
ncverilog: 15.20-s039; (c) Copyright 1995-2017 Cadence Design Systems, Inc.
Loading snapshot worklib.testfixture..... Done
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
ncsim: #,DVXACCI: some objects excluded from $dumpvars due to access restrictions, use +access+r on command line for access to all objects.
      File: ./testfixture.v, line = 74, pos = 9
      Scope: testfixture
      Time: 0 FS + 0

-----
----- START!!! Simulation Start -----
-----
-----
----- S U M M A R Y -----
Congratulations! All data have been generated successfully! The result is PASS!!

-----
Simulation complete via $finish(1) at time 3904539831 PS + 0
./testfixture.v:171      #(`CYCLE/2); $finish;
ncsim> exit

(8 min 03 s) Sun Jun 21 00:55:18
(28)#/~/project/RTL7
(CAD)b5902086@cad30:[0]$
```