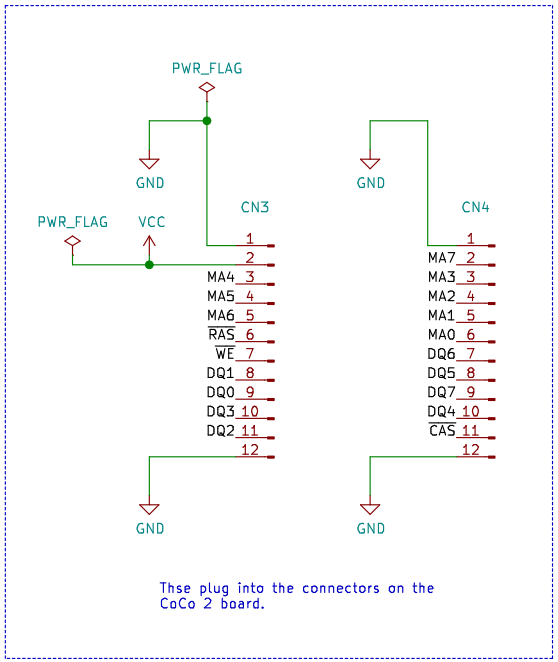
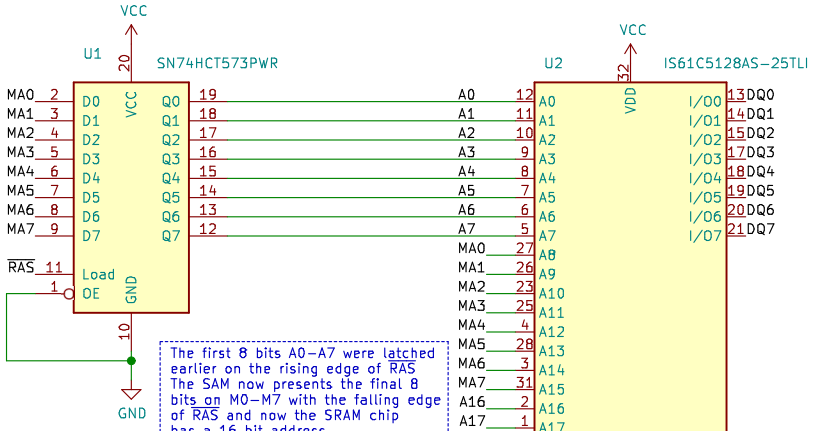
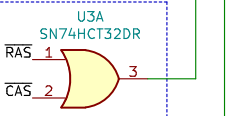
This design is inspired by several projects.
https://github.com/jamarju/c64-sram
which in turn was inspired by
https://postimg.cc/Ty3Ff6sb
And also Ciaran Ascomb's 512k
SRAM board for the CoCo 3.
https://gitlab.com/sixxie/cc3-512k



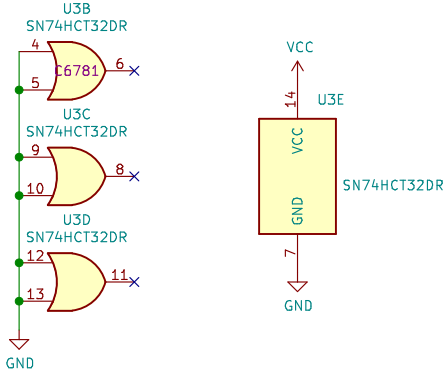
After the SAM presents the first 8 bits of the 16 bit address on MO-M7, the rising edge of RAS latches it on Q0-Q7.



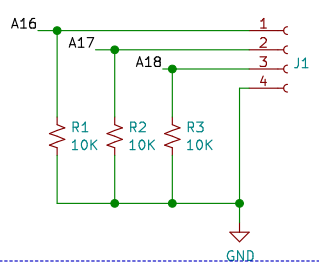
The first 8 bits A0-A7 were latched earlier on the rising edge of RAS The SAM now presents the final 8 bits on MO-M7 with the falling edge of RAS and now the SRAM chip has a 16 bit address.



The data sheet for the 4464 basically says that CAS is a chip enable and that the data is ready while RAS and CAS are low. I think this means that if you OR the two you can use them as an active low chip enable. The RAS refresh pulses will have no effect on CE when CAS is high.



A16-A18 are the extra address lines on this chip that are pulled low but also on a header so that people can use it for bank switching or whatever.



Rocky Hill		
Sheet: /		
File: coco2_3134_64k_static_ram_board.sch		
Title: D2S 64K Static RAM board for the 3134 CoCo 2		
Size: USLetter	Date: 2022-07-14	**Rev:**
KiCad E.D.A. kicad 5.1.5+dfsg1-2build2		Id: 1/1