Radstone PPC2A
Manual

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Trademarks

Document History

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Chapter 1 - Introduction

Radstone's PPC2A-603e, PPC2A-604e and PPC2A-740, with associated peripherals and software, are the latest products in Radstone's PowerFull family of VME-based PowerPC boards. They have the same architecture as the reference implementation of the PowerPC Reference Platform (PReP), ensuring compatibility with the abundance of PReP compliant software. Designed for users who require scaleable, high performance processors, sophisticated I/O subsystems and high levels of on-board integration, the PPC2A offers a cost-effective solution to a wide range of application requirements.

Like all Radstone's VME products, the PPC2A is available in a range of build styles, from Level 1 (Standard), suitable for a benign office-like environment, right through to Level 4 (Rugged Conduction Cooled), capable of withstanding the harshest of environments. All products are COTS/NDI, and make maximum use of low cost plastic packaged integrated circuits to ensure the most cost effective solution, whatever the market.

Local connection of SCSI-2, Ethernet and VME64 uses PCI, as does the IEEE P1386.1 PMC site. Twin PMC sites are available using a companion carrier card. PMCs available directly from Radstone include high performance graphics, FDDI, MIL-STD-1553, fast Ethernet and other communications. The PPC2A is the latest of Radstone's VME products to use 5-row connectors for P1 and P2, providing all I/O except PMC with direct connection to either P1 or P2.

Radstone is a key member of the VITA standards committee, setting the standards for rugged conduction cooled PMCs. In line with their recommendations, PMC I/O on Level 4 build standard product is connected to P0, allowing direct backplane connection to all I/O.

This flexibility, together with operating system support including VxWorks/Tornado, LynxOS, RTEMS, OS-9 and Spectra/VRTXSA are factors in making the PPC2A an ideal vehicle for applications such as communications, simulation, multi-media, real-time acquisition, terrain mapping, C^4, image processing and high performance graphics.

Documentation Objectives

This manual provides the user with sufficient information to understand the basic operation of the PPC2A hardware. The on-board firmware and other firmware (e.g. drivers and BSPs) are described in separate manuals.

Documentation Audience

This manual is written to cover, as far as possible, the range of people who will handle or use the PPC2A, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, systems, cabling, grounding, VME and communications. There is a glossary provided at the back of this manual that explains some of the terms used and expands all abbreviations.

Documentation Scope

This manual describes all build standards and variants of the PPC2A. It does not cover any PMC modules or the carrier card.

Documentation Structure

This manual is structured in a way that will reflect the sequence of operations from receipt of the PPC2A up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

Chapter 1 (this chapter) - gives a brief introduction, this manual's objectives, audience and scope, the documentation structure, some warnings, conventions and related documentation.

Chapter 2 - is a slightly more detailed, but still general product description.

Chapter 3 - contains unpacking and inspection instructions.

Chapter 4 - describes board configuration.

Chapter 5 - describes the PPC2A's connectors and signals used.

Chapter 6 - describes the PPC2A's front panel.

Chapter 7 - describes installation of the PPC2A in a system.

Chapter 8 - describes power-up and subsequent operation of the PPC2A.

Chapter 9 - is a functional description.

Chapter 10 - gives troubleshooting guidelines.

Appendix A - is a board specification.

There are also a glossary and an index provided.

Warnings

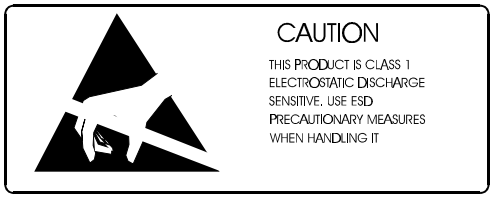
Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components.

Only use the PPC2A in backplanes that supply power on both the J1 and J2 connectors. Failure to observe this warning may result in damage to the board.

Do not remove the heatsink on the PPC2A-60x. Failure to observe this warning may result in *serious damage* to your PPC2A-60x during reattachment.

There are ***no*** PROMs or other user-alterable components underneath the heatsink, so users should have no reason to remove it.

Users should ***not*** attempt reattachment of the heatsink, as this requires precise torque on the screws attaching the heatsink to the PCB. Over-tightening the screws may cause the heatsink to damage components beneath it (e.g. the main PowerPC processor). **Removal and re-attachment of the heatsink should only be carried out by Radstone.**



Documentation Conventions

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a 'D' subscript and binary numbers have a 'B' subscript. The prefix '0x' shows a hexadecimal number, following the 'C' programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_B

Information of particular importance is highlighted by '**Note:** .

The multipliers 'k', 'M' and 'G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when 'K', 'M' and 'G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, k M and G mean $*10^3$, $*10^6$ and $*10^9$ not $*2^{10}$, $*2^{20}$ and $*2^{30}$**.**

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and VMEbus terminology follows the more familiar convention that bit 0 is the LSB and bit n is the MSB.

Signal names ending in with a tilde (~) denote active low signals; all other signals are active high.

The term PPC2A is used generically to refer to the PPC2A-603e (using the PowerPC 603e processor), the PPC2A-604e (using the PowerPC 604e processor) and the PPC2A-740 (using the PowerPC 740 processor). The devices are specifically referenced where necessary.

Related Documents

Due to the complexity of some of the parts used on the PPC2A, it is not possible to include all the detailed data on all such devices in this document. The following is a list of the specifications and data sheets that provide any additional information required:

VME64 Specification ANSI/VITA 1-1994 April 1995. *VMEbus International Trade Association AZ 85253 USA.*

VME64 Extensions Specification. Not Yet Published. *VMEbus International Trade Association AZ 85253 USA.*

PCI Local Bus Specification, Revision 2.1, June 1 1995. *PCI Special Interest Group OR 98214 USA.*

PCI System Design Guide.

IEEE P1386 Draft Standard for a Common Mezzanine Card Family.

IEEE P1386.1 Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards.

IEEE Std 802.3 Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) - (ETHERNET) (1985) *The Institute of Electronic and Electrical Engineers Inc., NY 10017 USA.*

ANSI X3.131-1986 - Small Computer System Interface (SCSI), *American National Standards Institute NY10036, USA.*

ANSI X3.131-1994 : Information Systems - Small Computer Systems Interface-2 (SCSI-2) *American National Standards Institute NY10036, USA.*

ANSI/EIA/TIA-232-E - Interface Between Data Terminal Equipment and Data Communications Equipment Employing Serial Binary Data Interchange (December 1991) *Electronic Industries Association, DC20006 USA.*

ANSI/EIA/TIA-422-B, Electrical Characteristics of Balanced Voltage Digital Interface Circuits (December 1978). *Electronic Industries Association, DC20006 USA.*

PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture, Version 1.0 (November 1995). *Morgan Kaufmann publishers Inc. San Francisco, California USA.*

PowerPC Microprocessor Family: The Programming Environments, 1994. *IBM VT 05452-4299 or Motorola AZ 85036 USA.*

The PowerPC Architecture: A Specification for a New Family of RISC Processors, Second Edition. *Morgan Kaufmann publishers Inc. San Francisco, California USA.*

PowerPC 603e RISC Microprocessor User's Manual, September 1995. *IBM VT 05452-4299 USA or Motorola AZ 85036 USA.*

PowerPC 604e RISC Microprocessor User's Manual. *IBM VT 05452-4299 USA or Motorola AZ 85036 USA.*

PowerPC 740/750 RISC Microprocessor User's Manual. *IBM VT 05452-4299 USA or Motorola AZ 85036 USA.*

MPC106 User Guide. *Motorola AZ 85036 USA.*

NCR53C860 PCI-SCSI I/O Processor Data Manual, Rev 2.1, May 1993. *NCR Microelectronic Products Division. CO 80916. USA.*

AM79C970 PCnet-PCI Single-Chip Ethernet Controller for PCI Local Bus. *Advanced Micro Devices Inc. CA 94088-3453 USA.*

82378 System I/O Data Book. August 1994. *Intel PCI Components Division CA 95052-8119 USA.*

UNIVERSE User Manual 1995. *Tundra Microsystems ON K2K 2M5 Canada.*

Flash Memory, Volume 1 1995. *Intel corporation IL 60056-7641 USA.*

Datacom ICs. 1991. *Zilog Inc. CA 95008-6600.*

Z8036 Z-CIO/Z8536 CIO Counter/timer and Parallel I/O Unit Technical Manual. *Zilog Inc. CA 95008-6600.*

Radstone X600 Modules Manual, publication number RT5060.

Radstone PPC Boot Firmware Manual, publication number RT5078.

Radstone PMC9100 Manual, publication number RT5062.

Radstone PMC2-9100 Manual, publication number RT30144.

Radstone BIT V3 User Manual, publication number HH681BITE3.

World Wide Web Sites

Manufacturers of many of the devices used on the PPC2A maintain FTP or world-wide-web sites. Some useful sites are:

http://www.mot.com
: Motorola PowerPC data is available through this site.

http://www.chips.ibm.com
: IBM PowerPC data is available through this site.

http://www.tundra.com
: Universe chip information, including the user manual for the Universe chip in Adobe Acrobat .pdf format, is available through this site.

Radstone on the world-wide-web is available at:

http://www.radstone.co.uk

or

http://www.radstone.com

Chapter 2 - General Description

This chapter contains a general description of the PPC2A. Chapter 9 describes the board in more detail.

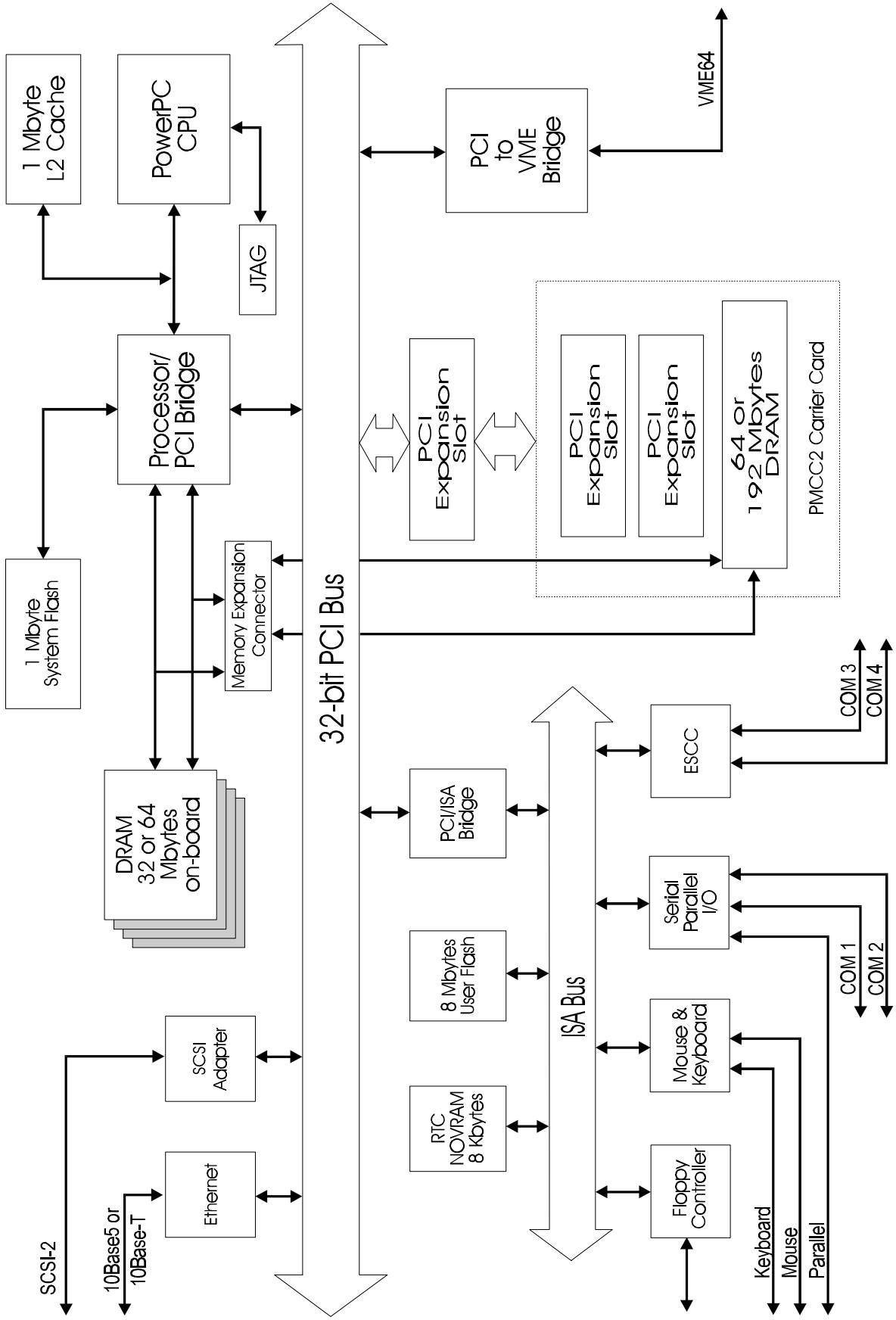
Introduction

The PPC2A-603e, PPC2A-604e and PPC2A-740 are highly integrated, PReP-based VMEbus processors using the PowerPC 603e, 604e and 740 RISC CPUs respectively. The products offer an extensive range of standard functions and expansion options including: processors clocked at 200, 266 and 300 MHz, user EDO DRAM up to 64 Mbytes with ECC, on-board serial, parallel and Ethernet channels, expansion for a wide range of communications controllers, 8 Mbytes of Flash memory, an Ultra SCSI-2 peripheral interface controller, high-resolution graphics (using a PMC module), a 64-bit VMEbus interface and direct connection for a keyboard and mouse.

On both products, expansion capabilities are provided by a PCI interface slot. PCI (PMC - IEEE P1386.1) provides an industry standard, high speed (132 Mbytes/second) local expansion bus, designed for graphics, high-speed communications (e.g. ATM, FDDI, ISDN, etc.), multi-media and user-defined custom functions. PCI has established itself as the leading local interconnect standard, and the wide availability of compatible devices, coupled with its adoption on an array of platforms, ensures that PCI-based modules are both high-performance and low cost.

The highly integrated nature of the PPC2A makes it a true single board computer. In many ways, the PPC2A resembles a high performance PC motherboard, although in a more rugged, lower profile and more compact form factor.

Figure 2-1. PPC2A Block Diagram



Features

- PowerPC 603e at 300 MHz, 604e at 200 or 300 MHz, or 740 at 266 MHz processor options (**contact your nearest Sales office for details of further speed grades**)
- Extensive operating system support, including VxWorks/Tornado, LynxOS, RTEMS Spectra/VRTXSA and OS-9
- Wide range of shrink-wrapped application software available
- PCI/PMC expansion slot on-board, with optional carrier for two PCI/PMC slots
- Up to 256 Mbytes of DRAM (up to 64 Mbytes on-board) with ECC
- 1 Mbyte Flash boot ROM
- Real Time Clock (TOD/calendar)
- *Standard* features include:
  - On-board PCnet-PCI Ethernet controller
  - Ultra SCSI-2 I/O processor
  - Two RS232 serial I/O channels up to 115.2 kbaud
  - Parallel/printer port
  - Keyboard/mouse interface
  - 1 Mbyte secondary cache
  - 8 Mbytes of user Flash
  - Floppy disk controller
  - VME64 interface using Tundra Universe VMEbus interface chip
- *Optional* features include:
  - Two additional fully featured RS232 or RS422/RS485 serial ports
  - High-resolution graphics (via a PMC slot)
- Single slot 6U VME board
- Range of 3U rear-mounting I/O modules
- PReP based design
- ANSI/VITA 1-1994 VME64 and VME64 extensions (5 row P1 and P2) compatible
- 4 build standards: 3 air cooled and one conduction cooled

Functional Overview

PowerPC Platform

The PowerPC Platform is an example implementation of a philosophy designed to allow software compatibility across different platforms based on the PowerPC processor. Aiming to achieve an open standard, the PowerPC Platform encourages the use of industry standard components and buses, and a wide range of operating systems.

As well as providing a detailed hardware design specification, the PowerPC Platform also embodies a software mechanism that allows the hardware to be isolated from the application by abstraction layers. It is these abstraction layers (in effect very low level system drivers) that are the key to differentiation, scalability and future-proofing. The operating systems, applications and drivers can 'sit' on these layers without needing to be aware of the underlying hardware (other than general functionality). This is fundamentally different from PCs, which use a BIOS that ultimately constrains operating systems and applications alike.

The major purpose of the PowerPC Platform architecture "... is to give direction to system designers, while still enabling differentiation in areas where real value can be added, thus allowing the PowerPC microprocessor industry to build a reusable body of OS and application software...". The knowledge that both OS and application programs will run on any host that complies with the PowerPC Platform architecture, provides security for today's valuable software investments, as well as expansion capabilities for the future.

Processor

The PowerPC has become the most widely used of the new generation of RISC processors. Its pedigree is unequalled - jointly developed by world-leading computer companies and backed by long-term commitments from major OEMs.

The PowerPC 603e, 604e and 740 are 32-bit superscalar RISC processors, featuring a 64-bit external data bus, on-chip instruction and data caches, MMU and integral FPU.

The PowerPC 604e is the highest performance device, clocked at 200, 266 or 300 MHz and employing a larger primary cache and enhanced branch prediction capabilities. The PowerPC 603e variant implements a fully static architecture and offers sophisticated power management capabilities. As a result, maximum power consumption is reduced to less than 6 Watts. The PowerPC 740 is a higher performance enhancement of the PowerPC 603e.

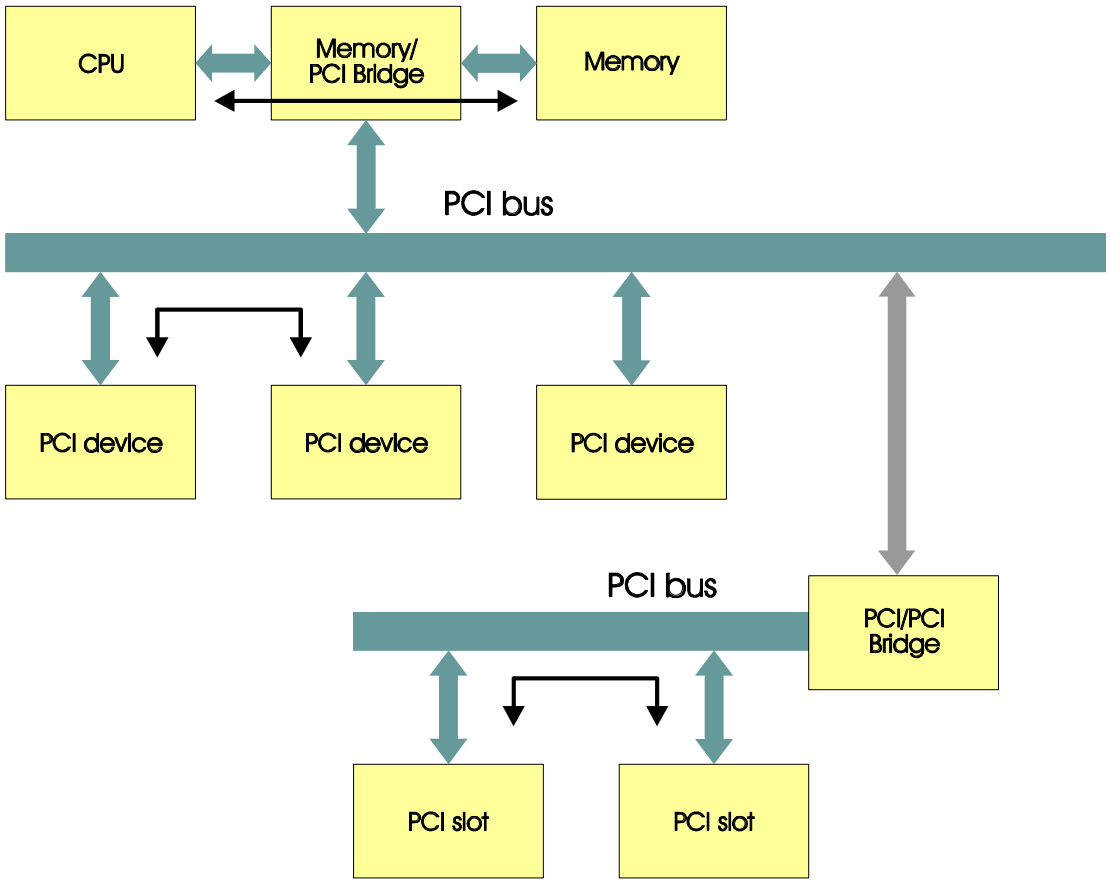
Processor	Clock (MHz)	Cache	Performance	Maximum Power (Watts)
603e	300	16 Kbytes data 16 Kbytes instruction	7.4 SPECint95 6.1 SPECfp95	6
604e	200	32 Kbytes data 32 Kbytes instruction	9.4 SPECint95 8.7 SPECfp95	16
	300		12.5 SPECint95 8.9 SPECfp95	13
740	266	32 Kbytes data 32 Kbytes instruction	11.5 SPECint95 6.9 SPECfp95	9

PCI

PCI has become a highly desirable local interface bus, due to its high bandwidth, glueless interface and low cost. The PPC2A uses PCI to provide a high-speed backbone, both for local interconnect of on-board devices (processor, Ethernet, SCSI-2, ISAbridge and VME64, all of which have direct PCI connectivity), and for communication with optional mezzanine expansion modules (PMCs). A range of PMCs are available from Radstone, including high-performance graphics, MIL-STD-1553, multi-channel communications, FDDI and ATM. These all fully comply with the IEEE P1386.1 standard. PCI provides a synchronous 32-bit multiplexed address and data bus (with future expansion capability to 64-bit), allowing burst data transfers to 132 Mbytes/second. The PCI mezzanine format also provides 64 I/O pins for user definition.

Using a PCI to PCI bridge device on the PCI carrier card, the PPC2A can maintain concurrent bus operation. This allows applications using PMCs for routing and communications to operate efficiently and in parallel without being blocked.

Figure 2-2. PCI Interconnectivity



PCI Bridge and Memory Controller

The MPC106 PCI bridge and memory controller interfaces the processor to the DRAM and the PCI bus.

PMC Carrier Card

One PMC slot is provided as standard on the PPC2A. For those configurations that require additional PCI functionality, Radstone has developed a PMC Carrier Card (PMCC2) that allows two PMC modules to be fitted in an adjacent VMEbus slot. Applications requiring up to two PCI slots can therefore easily be realised. The PMCC2 uses the PPC2A's on-board PMC slot for its direct coupling to the PCI bus.

The PMCC2 can also contain up to 192 Mbytes of DRAM, directly coupled to the main board's memory bus, allowing a total of 256 Mbytes of memory to be realised.

The following table shows the number of PCI slots and the amount of DRAM available with and without the PMCC2:

PMCC2	DRAM Memory	PCI Slots Available	VME Slots
Absent	32 or 64 Mbytes	1	1
Present	32 to 256 Mbytes	2	2

Memory

System RAM

Between 32 and 256 Mbytes of system memory is available. Up to 64 Mbytes of EDO DRAM can be fitted directly to the main board using 16 Mbit devices in two banks of 72-bit wide DRAM, controlled by the MPC106 PCI bridge. An additional 192 Mbytes can be added via the PMCC2. All system memory runs contiguously and is dual-ported between the processor and PCI.

The data is protected by Error Correction Coding capable of detecting all single bit, double bit and nibble errors, and correcting single bit errors.

System ROM

1 Mbyte of Flash is available to hold BIT, initialisation routines and operating system boot routines.

NOVRAM

For maintenance of general system parameters, such as boot options and the VME configuration, the 8 Kbytes of on-board NOVRAM provides a convenient storage area.

User Flash ROM

8 Mbytes of user Flash ROM is fitted as standard. The Flash resides in two sites and has support for on-board programming.

Level 2 Cache

For users who require extra performance, a 1 Mbyte secondary cache, directly connected to the processor bus, is fitted.

VMEbus Interface

The Tundra Universe II chip provides a full master/slave VMEbus interface. Features include full slot 1 (system controller) functionality, an interrupt handler, an interrupt generator, a DMA controller and support for VME64. VMEbus slave address decoding is software configurable.

Utility I/O and Auxiliary Function Bus

To take full advantage of low-cost, industry standard components, general purpose I/O and auxiliary functions are implemented via an ISA bus interface. Facilities provided include: a parallel/printer port, two PC-compatible serial interfaces, a floppy disk controller, a real-time clock, a keyboard/mouse interface, user Flash memory and two high speed RS232 or RS422 serial ports.

Input/Output

The PPC2A has a wide variety of possible I/O connectivity including fast SCSI-2, Ethernet, serial, mouse/keyboard and parallel/printer ports. To allow the greatest freedom and convenience of connecting to these ports, a range of I/O modules are available and are attached by a VME P2 transition module. Using P2 I/O minimises the effort needed to remove boards from a rack, so improving maintainability and reliability.

Operating System Support

PowerPC is one of the few platforms with a wide variety of operating systems ported to it, with more being added all the time. These include VxWorks/Tornado, LynxOS, RTEMs, OS-9 and Spectra/VRTXSA.

VxWorks/Tornado

Wind River System's VxWorks/Tornado distributed real-time operating system includes integrated networking facilities and a complete software development environment for Windows and UNIX hosts. It features a fast, multitasking kernel with pre-emptive scheduling, inter-task communications, multiprocessor support, symbolic and source-level debugging, performance monitoring and an I/O file system.

The full range of facilities are supported by BSPs for all Radstone CPU types, which have been validated by both Radstone and Wind River for the greatest confidence and ease of use. To complement the BSPs, many of Radstone's I/O and graphics products are also supported by libraries and drivers.

LynxOS

Created by Lynx Real Time Systems, LynxOS is compatible with UNIX V.3. It is POSIX compliant and supports X.11 (X-Windows), Motif, NFS and TCP/IP. Unlike conventional UNIX, it is fully pre-emptive to ensure that application tasks can be rescheduled if a higher priority task is ready.

OS-9

OS-9 is one of the most common real-time operating systems. Primarily used for industrial control, it is both modular and scaleable. This allows systems to be realised in a variety of configurations, from ROMable stand-alone kernels to full blown multi-user development systems. Recent additions to OS-9 now allow it to support sophisticated man-machine interfaces, and to target vertical applications such as multi-media telecommunications and video-on-demand.

OS-9/PowerPC is equipped with a full suite of resident, UNIX and Windows cross development tools, as well as a sophisticated feature set. This includes hierarchical file managers (for hard, floppy and optical disks, and RAM); network and file transfer protocols (TCP/IP, UDP/IP, FTP, NFS, RPC, Telnet and BOOTP); priority based, pre-emptive task scheduling; UNIX-like process model and I/O facilities, and extensive interprocess communications.

RTEMS

RTEMS is a high-performance, object-oriented, multiprocessing executive that provides a robust set of features for today's real-time software developer. It serves as the foundation for developing portable, reusable, efficient real-time software.

Developed by OAR for the US Army Missile Command to provide all the power and flexibility of the real-time executives available on the commercial market today, but without the high cost and royalties, RTEMS is freely available from the Internet with no royalties attached. RTEMS has been implemented in both C and Ada languages to meet the needs of both commercial and military embedded applications developers.

The RTEMS executive is a set of software components that consists of managers, an executive core, BSPs and device drivers. Together, these components provide a powerful run-time environment.

Developed in-house to provide the maximum correspondence with board hardware features, the RTEMS BSP for the Radstone PPCx board family is supported by, and available from, OAR. The BSP allows complete compatibility at the operating system level to be maintained across the whole PPCx range, meaning, for example, that there is complete portability of applications developed on commercial grade boards and deployed on extended temperature or ruggedised boards.

Spectra/VRTXsa

Microtec's Spectra development system represents the next generation in Integrated Development Environments for real-time and embedded software. Spectra addresses the full range of embedded applications, from austere, minimal resource systems with no real-time operating system requirements, up to complex resource-intensive systems. Designed specifically for real-world applications, Spectra radically reduces target memory consumption, allowing more room for innovation at the application level. Organisations standardising on Spectra can focus on a single software architecture - on both the host and target - so enjoying the full benefits of cross training, consolidated support and simplified maintenance. Spectra fully integrates the Microtec self-optimising C and C++ compilers, the XRAY Pro debug suite and the VRTX real-time operating system.

VRTX is designed for use with Spectra, and is the latest incarnation of the popular real-time operating system. It offers complete upward compatibility for applications based on the original VRTX and VRTX32, and features a state-of-the art, real-time kernel called VRTXsa, which is an upwardly compatible superset of the VRTX32 kernel. VRTXsa, reflecting the latest advances in operating system technology, is based on a revolutionary new real-time operating system architecture called Nanokernel. It can support multiple co-operating application programming interfaces on the same processor, so allowing code reusability across applications. VRTXsa also provides deterministic priority-inversion free operation, and can reduce system latency by accepting an interrupt for a new task without completing its current operation.

The full range of facilities for Spectra and VRTX are supported by BSPs for the Radstone PowerPC family.

Mechanical Overview

The PPC2A is available in four electrically compatible build styles. These have two basic mechanical configurations: convection-cooled in accordance with ANSI/VITA 1-1994 spec., and conduction-cooled in accordance with IEEE Std 1101.2-1992.

Convection-cooled boards include:

Level 1/Standard (S-style)
Level 2/Extended Temperature (X-style)
Level 3/Rugged Air-cooled (RA-style)

Conduction-cooled boards include:

Level 4/Rugged Conduction-cooled (RC-style)

A brief description of each build style follows:

Level 1/Standard (S-style)

Intended for use in benign environments, S-style also provides the ideal cost effective method of complete system development. The S-style assembly comprises a double-Eurocard size printed wiring board with high quality commercial (plastic encapsulated) components. As software compatibility throughout the build styles is absolute, a system intended for final implementation in a severe tactical environment can be developed and debugged at low cost, switching over to target style only in the final stages of system integration.

Level 2/Extended Temperature (X-style)

As S-style, but conformally coated and 100% tested in manufacture to provide an extended operating range.

Level 3/Rugged Air-cooled (RA-style)

RA-style boards are intended for applications that have extended temperature, shock and vibration requirements, but can be served by conventional, forced-air cooled, racking systems. These rugged boards comprise a double-Eurocard size printed wiring board fitted with wide temperature range, industrial grade components and are conformally coated as standard.

Level 4/Rugged Conduction-cooled (RC-style)

Designed primarily for use in sealed ATR chassis and other conduction-cooled environments, the RC-style board features wide temperature range, industrial grade devices, an integral thermal management layer, and incorporates a central stiffening bar for additional strength. Cooling is achieved through conduction of heat from the thermal management layer to the cold wall of the rack to which the boards are secured by screw driven wedgelocks. RC-style boards are 100% temperature characterised and conformally coated during manufacture. RC-style is mechanically compliant with IEEE Std. 1101.2-1992.

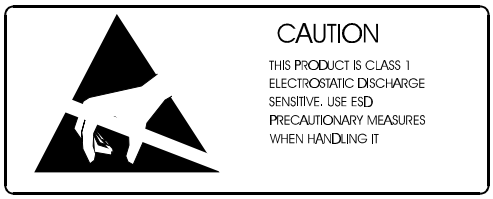
All five styles fully support the power and versatility of the VMEbus, so no matter how large or diversified your project, absolute compatibility is assured at all stages of development.

Chapter 3 - Unpacking and Inspection

This chapter gives guidelines on unpacking and inspecting the PPC2A.

Unpacking

Radstone boards are protected by an antistatic envelope. **Observe antistatic precautions and work at an approved antistatic work station when unpacking the board.**



The PPC2A is shipped in an individual, reusable shipping box. When you receive the shipping container, inspect it for any evidence of physical damage. If the container is damaged, request that the carrier's agent is present when the carton is opened. Keep the contents and packing materials for the agent's inspection and notify Radstone's customer service department of the incident. Retain the packing list for reference.

Assuming that there is no obvious damage, you may still want to keep the shipping carton in case you want to ship the PPC2A on elsewhere.

Board Identification

The PPC2A is identified by two labels fitted to the heatsink. The first label gives the board's part number, revision state and serial number, and the second label gives supplementary revision state data any modification (MIN) information. An example of each follows:

PPC2A-2BA-4726A	REV -2
9700321 MADE IN UK	

PPC2A-2BA-40		REV A3
9700321	MADE IN UK	MIN 1234

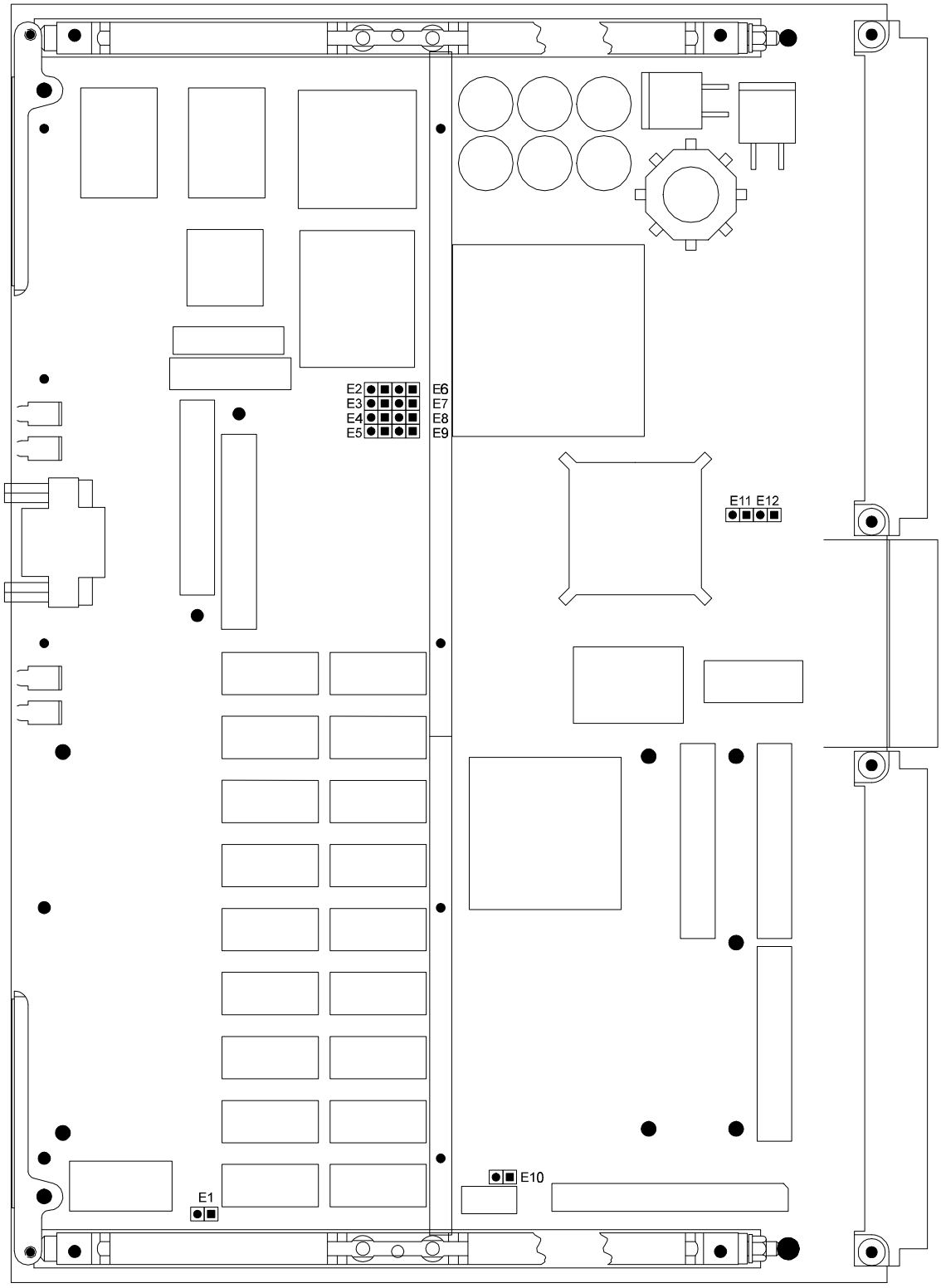
Inspection

Assuming that the PPC2A is not obviously damaged, you can now go on to inspect it. It is possible for components (connectors, links, socketed chips etc.) to work loose or be dislodged in transit or in the process of unpacking, although this is extremely unlikely. A quick visual inspection should reveal any obviously loose components. Report any defects you detect to Radstone.

Now inspect the board for any loose or missing links. The board is delivered with the following default link configuration:

Link	Setting	Action
E1	Out	Locked blocks of user Flash can be erased
E2	Out	Boot from System Flash
E3, E4, E5 and E9	Out	ID links (board ID = 15)
E6	Out	Machine Check routed to IRQ13
E7	Out	Machine Check ignored
E8	Out	Flash programming voltage not enabled
E10	Out	Factory option
E11	Out	5VSTNDBY needs 4.5 to 5.5 Volts
E12	Out	On-board SCSI terminators disabled

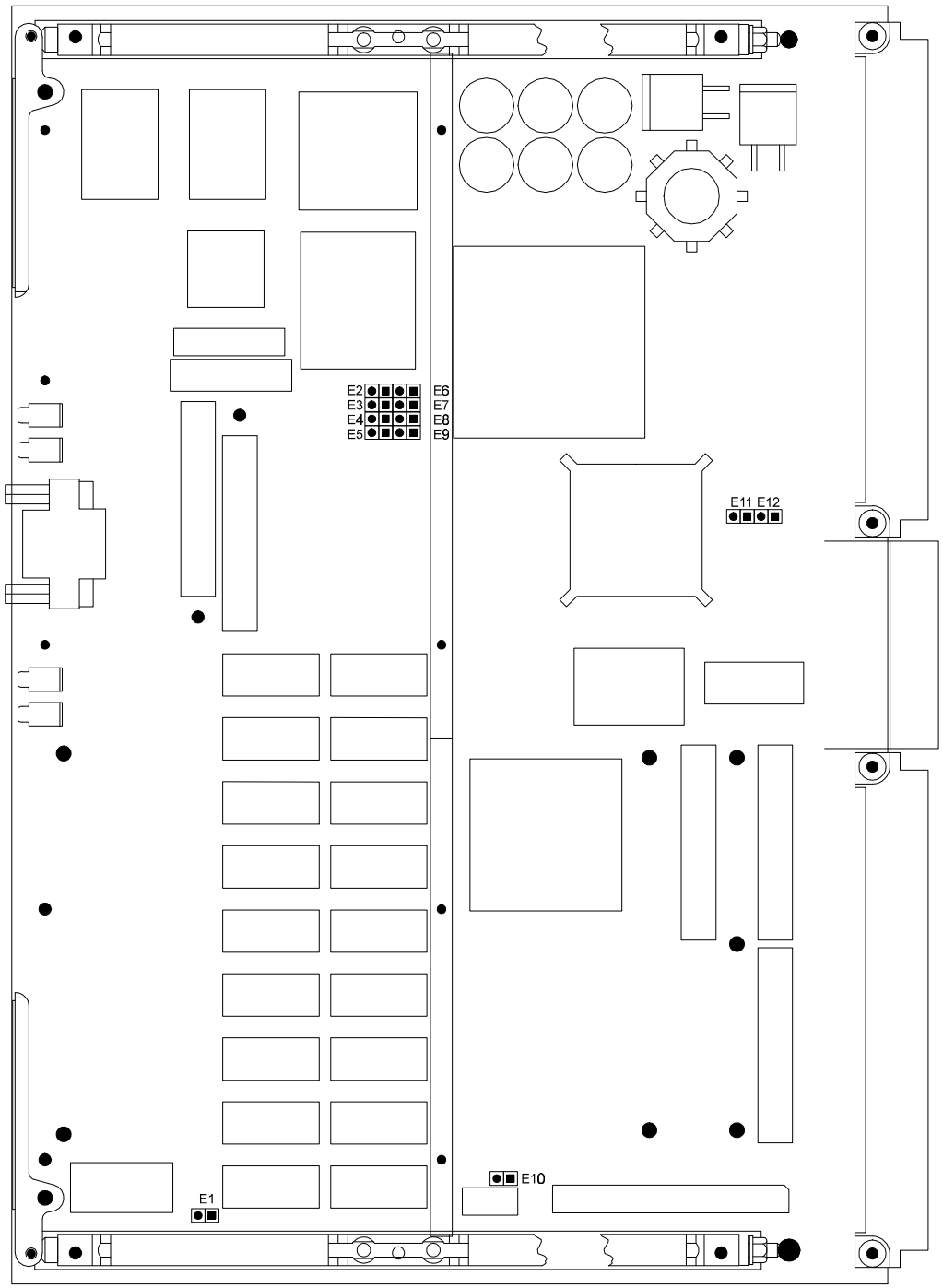
Figure 3-1. Link Positions and Default Configuration



Chapter 4 - Configuration

This chapter describes the configuration of links on the PPC2A. Push on jumper links are supplied with the board or the posts can be connected using wire wraps.

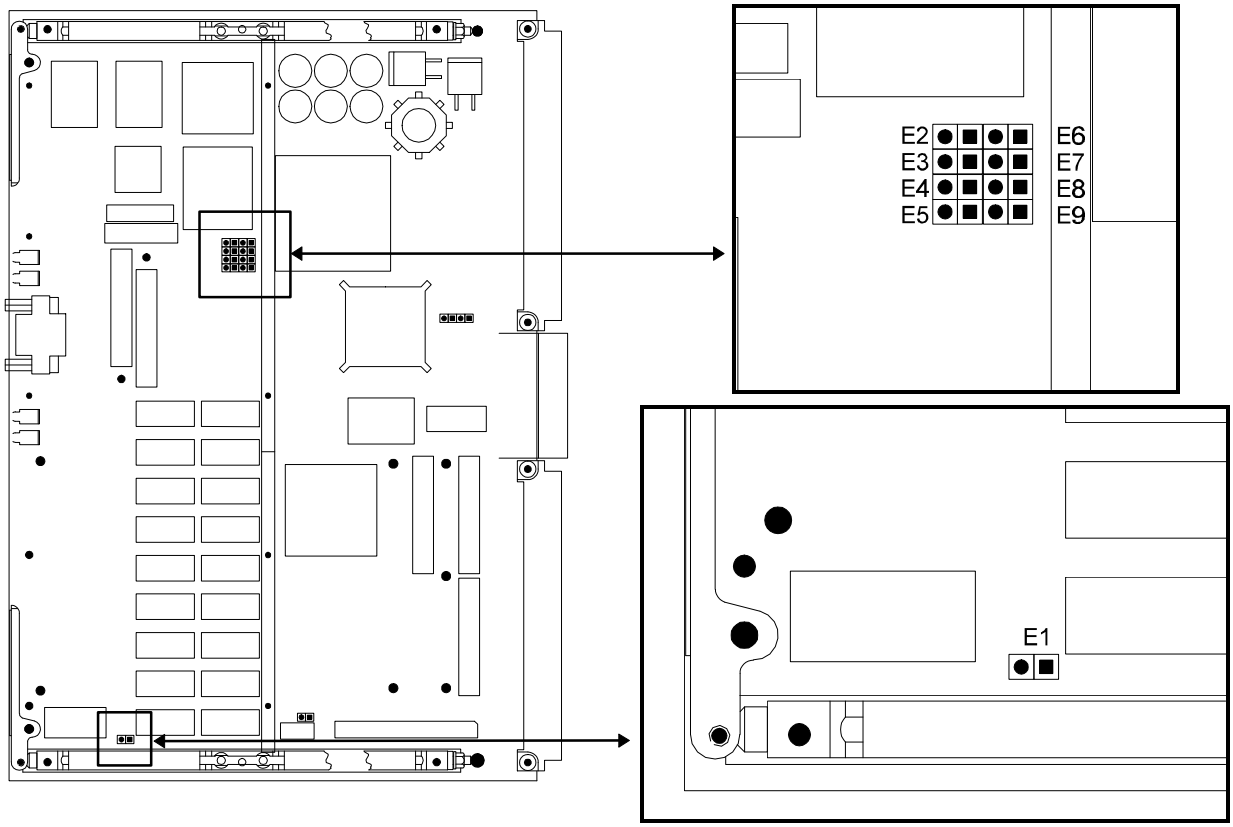
Figure 4-1. Link Positions



User Flash ROM Write Disable Link (E1)

This link enables or disables erasure of locked blocks of the user Flash ROM.
See Chapter 9 for details of user Flash operation.

Fitting	Meaning
In	Disable erasure of locked blocks of the user Flash ROM
Out (Default)	Locked blocks can be erased



VME Boot Link (E2)

This link enables or disables booting of firmware over the VMEbus as follows:

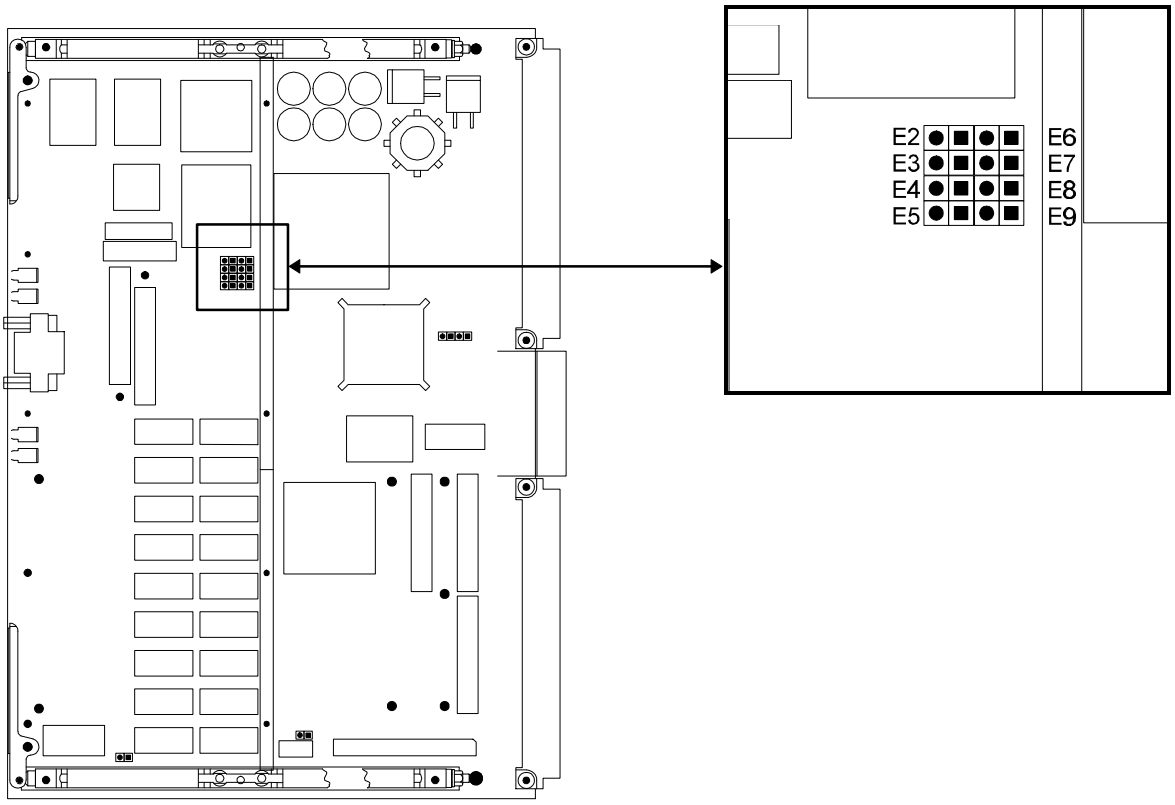
Fitting	Meaning
In	Firmware boot over VME enabled
Out (Default)	Firmware boot from System Flash enabled

Use of this link relies on the default Universe configuration (see the VMEbus Interface Configuration section).

ID Links (E3, E4, E5 and E9)

These links form a 4-bit board ID that may be read from the board ID register (see Chapter 9). The links are decoded as follows:

E9	E4	E3	E5	Board ID
Out	Out	Out	Out	15 (Default)
Out	Out	Out	In or P1 D10 GND	14
Out	Out	In or P1 D11 GND	Out	13
Out	Out	In or P1 D11 GND	In or P1 D10 GND	12
Out	In or P1 D13 GND	Out	Out	11
Out	In or P1 D13 GND	Out	In or P1 D10 GND	10
Out	In or P1 D13 GND	In or P1 D11 GND	Out	9
Out	In or P1 D13 GND	In or P1 D11 GND	In or P1 D10 GND	8
In or P1 D15 GND	Out	Out	Out	7
In or P1 D15 GND	Out	Out	In or P1 D10 GND	6
In or P1 D15 GND	Out	In or P1 D11 GND	Out	5
In or P1 D15 GND	Out	In or P1 D11 GND	In or P1 D10 GND	4
In or P1 D15 GND	In or P1 D13 GND	Out	Out	3
In or P1 D15 GND	In or P1 D13 GND	Out	In or P1 D10 GND	2
In or P1 D15 GND	In or P1 D13 GND	In or P1 D11 GND	Out	1
In or P1 D15 GND	In or P1 D13 GND	In or P1 D11 GND	In or P1 D10 GND	0



Machine Check Option Links (E6 and E7)

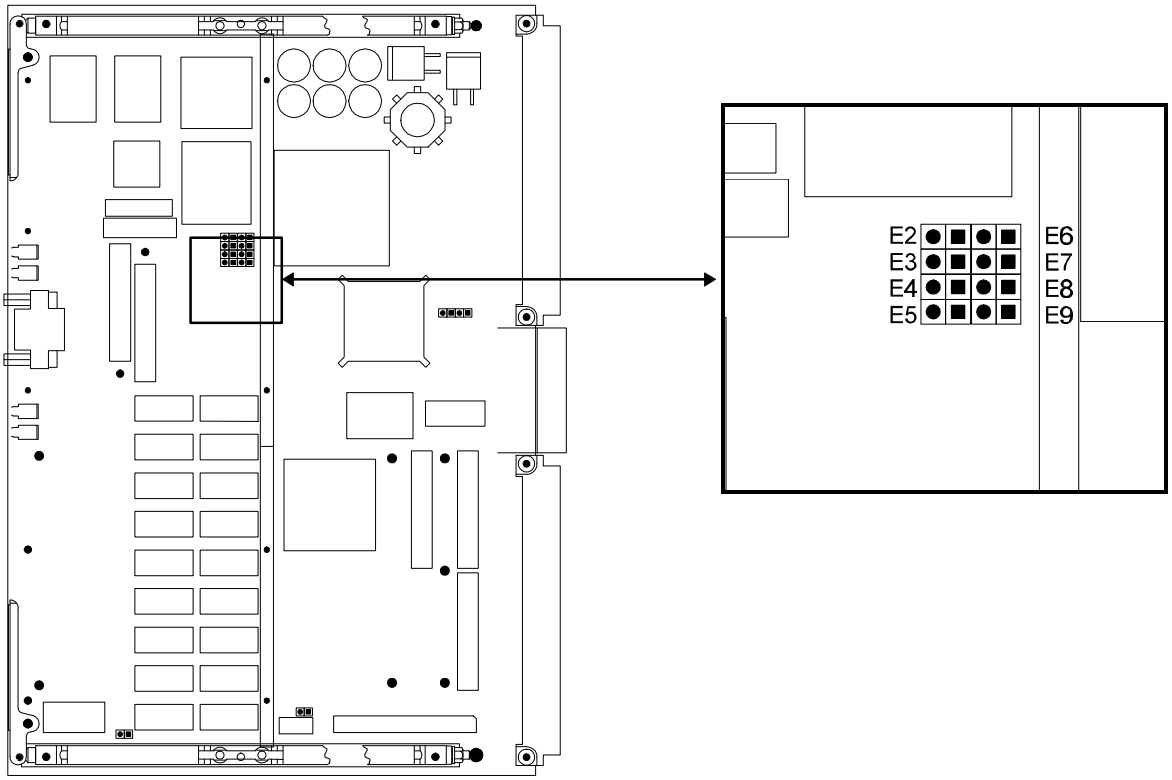
These links determine what action to take when the MPC106 PCI bridge signals a machine check due to a non-recoverable error. The options are to ignore the machine check, request an interrupt on IRQ13 or signal a machine check to the processor. For more details, see the Machine Check Exceptions section in Chapter 9.

These links are mutually exclusive; do not fit them both at the same time.

E6	E7	Meaning
Out	Out	Machine Check ignored (Default)
Out	In	Machine Check routed to IRQ13
In	Out	Machine Check exception enabled
In	In	***Do not fit this combination***

Flash Programming Enable Link (E8)

Link E8 must be fitted or P2 pin Z1 grounded before either the system or the user Flash can be programmed. With the link not fitted and P2 Z1 open circuit, the on-board programming voltage is disabled, ensuring that inadvertent writes to Flash do not occur.



Factory Test Option (E10)

Link E10 is for factory test purposes only. **Do *not* change the setting of this link from that fitted at the factory (out).**

+5VSTNDBY Option Link (E11)

During power-down, the RTC uses +5VSTNDBY from the backplane to continue its timekeeping. This link should be set according to the voltage (+5V or +3.3V) of the external battery/power supply powering the +5VSTNDBY signal.

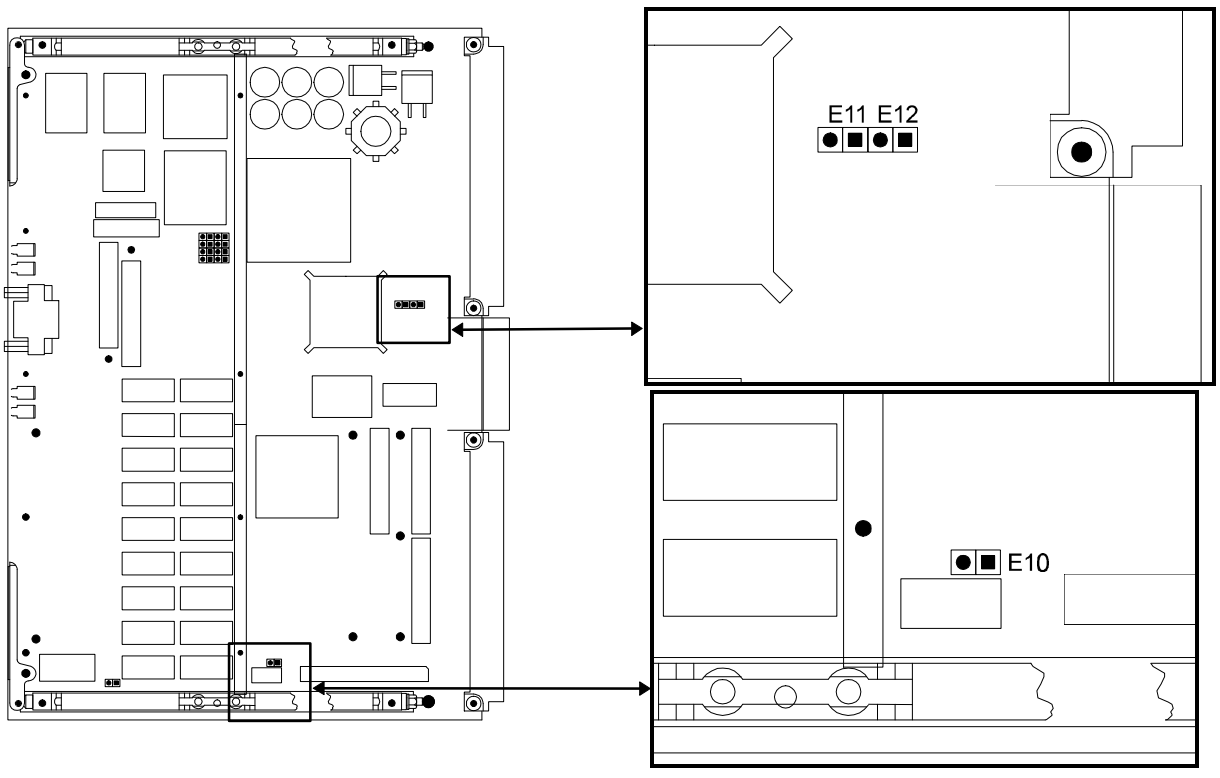
Note: If power is not supplied to the RTC via +5VSTNDBY, it will stop.

Setting	Meaning
Out (Default)	+5VSTNDBY is 4.5 to 5.5V
In	+5VSTNDBY is 3.0 to 3.6V

On-board SCSI Terminator Enable Link (E12)

This link enables or disables the on-board SCSI terminators.

Fitting	Meaning
In	Enable on-board SCSI terminators
Out (Default)	Disable on-board SCSI terminators



Default Link Settings

Link	Setting	Action
E1	Out	Locked blocks of user Flash can be erased
E2	Out	Boot from System Flash
E3, E4, E5 and E9	Out	ID links (board ID = 15)
E6	Out	Machine Check ignored
E7	Out	
E8	Out	Flash programming voltage not enabled
E10	Out	Factory option
E11	Out	+5VSTNDBY needs 4.5 to 5.5 Volts
E12	Out	On-board SCSI terminators disabled

Suggested Configuration

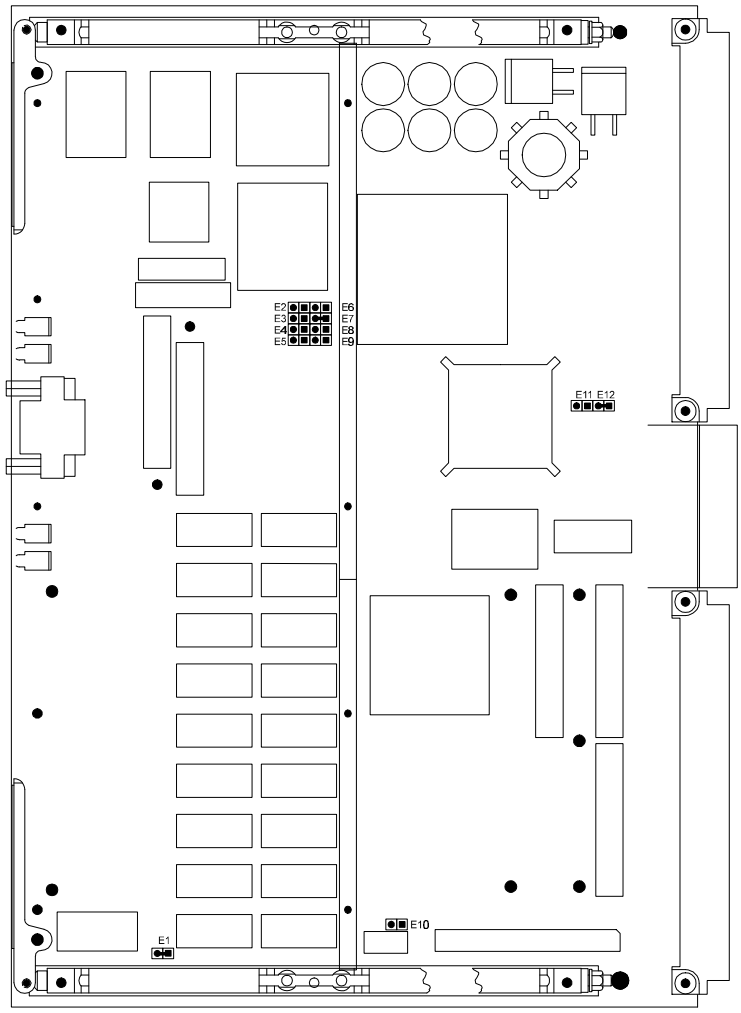
Although the default link configuration is for no links to be fitted, this may not suit your system, and you may need to fit links to configure your PPC2A before plugging it into your system. The following suggested link settings will be suitable in many cases (shown pictorially overleaf):

Link	Setting	Action
E1	In	Erasure of Locked Blocks of User Flash disabled
E2	Out	Boot from System Flash
E3, E4, E5 and E9	Out	ID links (board ID = 15)
E6	Out	Machine Check routed to IRQ13
E7	In	
E8	Out	Flash programming voltage not enabled
E10	Out	Factory option
E11	Out	+5VSTNDBY needs 4.5 to 5.5 Volts
E12	In	On-board SCSI terminators enabled

If you are using the SCSI bus, you are recommended to locate the PPC2A at one end and enable the terminator by fitting link E12. If you want to use the PPC2A somewhere other than at the end of the SCSI bus, ensure that E12 is not fitted. **Fitting E12 when the PPC2A is not located at the end of a SCSI bus may cause erroneous SCSI operation.**

The power supply to the RTC on the PPC2A is fed from the VSTANDBY pin on the VMEbus. VMEbus compliance requires this voltage to be 5V ± 5%. Fitting link E11 allows you to supply a voltage of 3V from a battery to this pin to maintain normal RTC operation. **Fitting E11 when VSTANDBY is connected to +5V may cause damage to the RTC.**

Figure 4-2. Suggested PPC2A Configuration



VMEbus Interface Configuration

Several operating features of the Universe VME interface are set at power-up or reset by surface mount jumper links. All of these, except local register access, may be overridden by software. The default settings are:

Register access slave image from VMEbus:	Enabled in A32 space at 0x80000000
VME CR/CSR slave image:	Disabled
PCI slave image 0:	Enabled in PCI memory space at 0xF0000000 to 0xFFFFFFFF
Local register access:	PCI I/O space
Auto-ID scheme:	Disabled

Changing the default power-up options requires surface-mount rework tools and would normally only be done at the factory. Further details are available from technical support at Radstone.

PMC Installation

One single width PMC module may be fitted to the PPC2A as shown in Figure 4-3. The PPC2A is keyed to accept only 5V PMC modules.

Each PMC module is supplied with a full kit of parts for mounting it, full fitting instructions and a manual (which also normally contains instructions on how to fit the module). The installation of driver software or other firmware configuration may be required to achieve full functionality of a PMC module (see the specific PMC manual for the exact procedure). PMC modules ordered with a PPC2A are supplied factory fitted by Radstone.

If the PMC is an air cooled module from Radstone's rugged PMC range, a half height central stiffening bar should be fitted to the PMC before installation. If this type of PMC module is ordered with a PPC2A, then this will be done by Radstone.

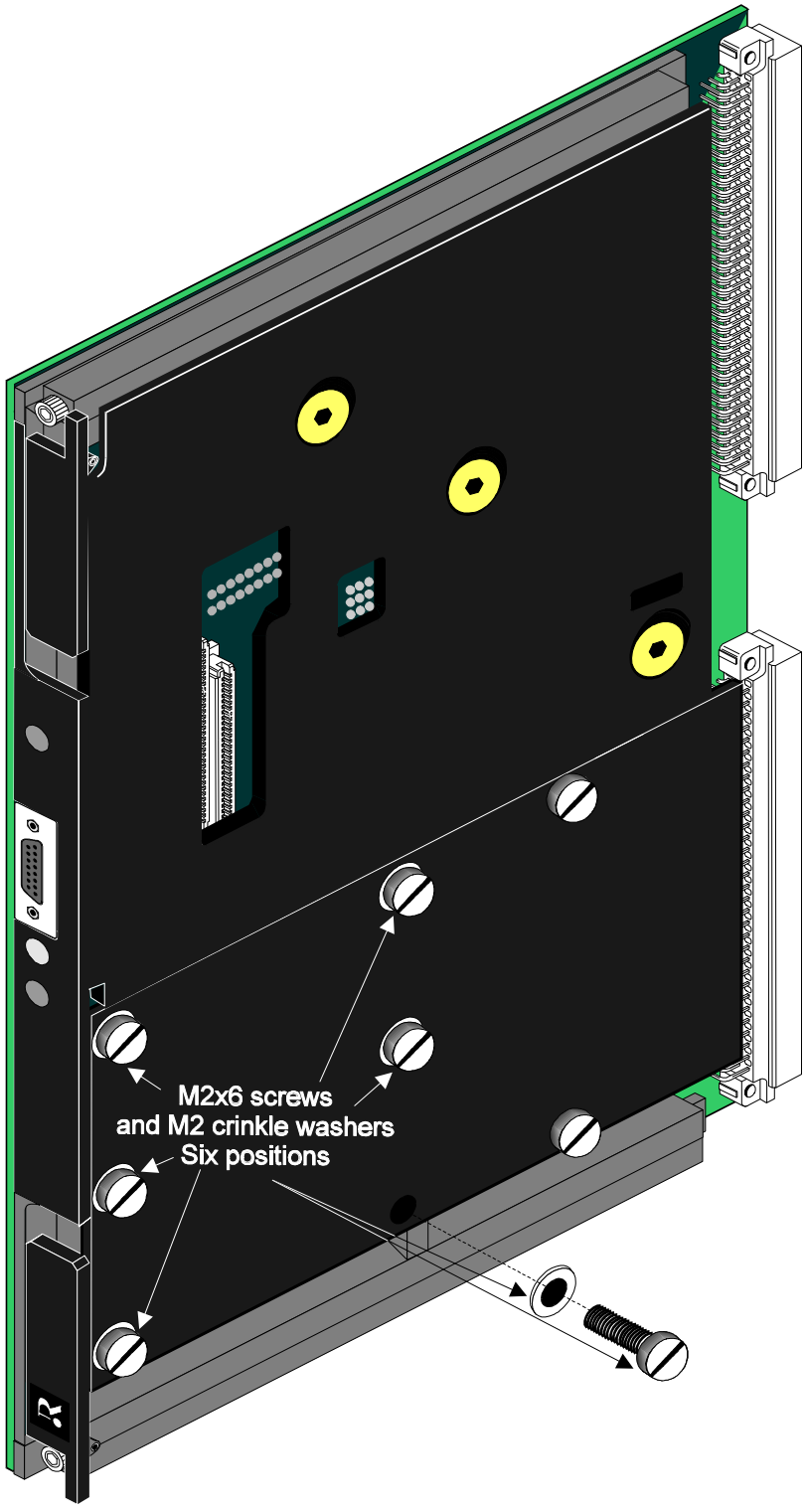
If you are fitting your own PMC module, then before fitting the module, remove the blanking plate from the PMC slot in the front panel. The PMC's bezel will fill the slot and will usually provide connection to the module.

Note: You are recommended not to route analogue signals through P0.

Carrier Card Installation

The PMCC2 may be installed in place of the PMC shown in Figure 4-3. If required, a PMCC2 ordered with a PPC2A can be factory fitted by Radstone (see the Ordering Information section in Appendix A for more details).

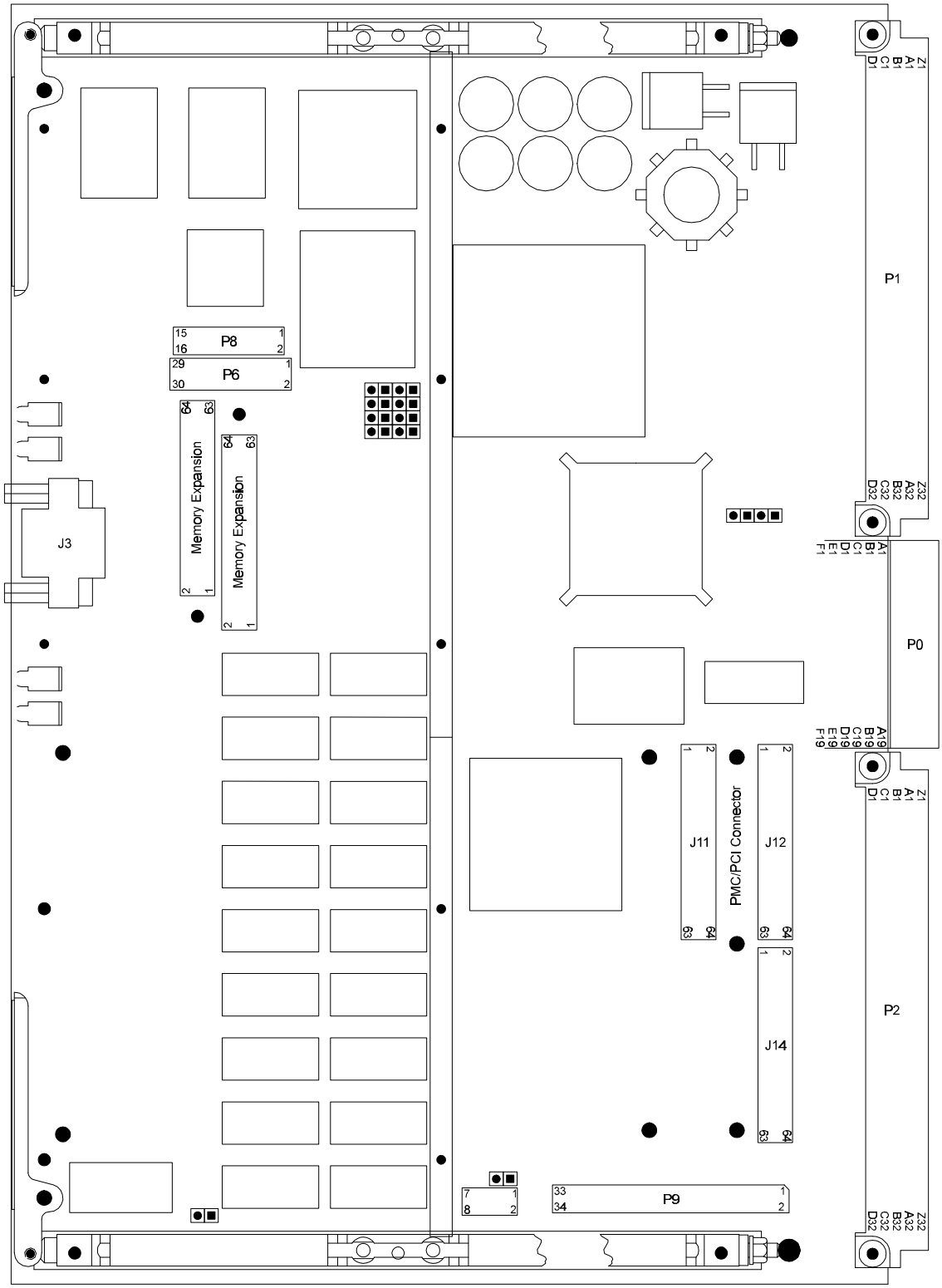
Figure 4-3. PMC Installation



Chapter 5 - Connectors

This chapter gives the pinouts and signal descriptions for the connectors on the PPC2A.

Figure 5-1. Connector Positions and Numbering



P1 (VMEbus) Connector

Pin Number	Row z	Row a	Row b	Row c	Row d
1	NC	D00	BBSY~	D08	+5V
2	GND	D01	BCLR~	D09	GND
3	NC	D02	ACFAIL~	D10	NC
4	GND	D03	BG0IN~	D11	NC
5	NC	D04	BG0OUT~	D12	NC
6	GND	D05	BG1IN~	D13	NC
7	NC	D06	BG1OUT~	D14	NC
8	GND	D07	BG2IN~	D15	NC
9	NC	GND	BG2OUT~	GND	NC
10	GND	SYSCLK	BG3IN~	SYSFAIL~	GA0~
11	NC	GND	BG3OUT~	BERR~	GA1~
12	GND	DS1~	BR0~	SYSRESET~	NC
13	NC	DS0~	BR1~	LWORD~	GA2~
14	GND	WRITE~	BR2~	AM5	NC
15	NC	GND	BR3~	A23	GA3~
16	GND	DTACK~	AM0	A22	NC
17	NC	GND	AM1	A21	NC
18	GND	AS~	AM2	A20	NC
19	NC	GND	AM3	A19	NC
20	GND	IACK~	GND	A18	NC
21	NC	IACKIN~	SERA	A17	NC
22	GND	IACKOUT~	SERB	A16	NC
23	NC	AM4	GND	A15	NC
24	GND	A07	IRQ7~	A14	NC
25	NC	A06	IRQ6~	A13	NC
26	GND	A05	IRQ5~	A12	NC
27	NC	A04	IRQ4~	A11	NC
28	GND	A03	IRQ3~	A10	NC
29	NC	A02	IRQ2~	A09	NC
30	GND	A01	IRQ1~	A08	NC
31	NC	-12V	+5VSTDBY	+12V	GND
32	GND	+5V	+5V	+5V	+5V

P2 Connector Pinout

Pin Number	Row z	Row a	Row b	Row c	Row d
1	FLPRGEN~	DB0~ (SCSI)	+5V	Collision-/RX+	COM3_TXD_A
2	GND	DB1~ (SCSI)	GND	Collision+/RX-	COM3_TXD_B
3	NC	DB2~ (SCSI)	Reserved	Transmit-/TX+	COM3_RXD_A
4	GND	DB3~ (SCSI)	A24	Transmit+/TX-	COM3_RXD_B
5	NC	DB4~ (SCSI)	A25	Receive-	COM3_RTS_A
6	GND	DB5~ (SCSI)	A26	Receive+	COM3_RTS_B
7	NC	DB6~ (SCSI)	A27	+12V Fused	COM3_CTS_A
8	GND	DB7~ (SCSI)	A28	nSTROBE	COM3_CTS_B
9	COM4_TXD_A	DBP~ (SCSI)	A29	D1	COM3_DSR_A
10	GND	ATN~ (SCSI)	A30	D2	COM3_DSR_B
11	COM4_TXD_B	BSY~ (SCSI)	A31	D3	COM3_DCD_A
12	GND	ACK~ (SCSI)	GND	D4	COM3_DCD_B
13	COM4_RXD_A	RST~ (SCSI)	+5V	D5	COM3_DTR_A
14	GND	MSG~ (SCSI)	D16	D6	COM3_DTR_B
15	COM4_RXD_B	SEL~ (SCSI)	D17	D7	COM3_TT_A
16	GND	C/D (SCSI)	D18	D8	COM3_TT_B
17	COM4_CTS_A	REQ~ (SCSI)	D19	nACK	COM3_ST_A
18	GND	I/O (SCSI)	D20	BUSY	COM3_ST_B
19	COM4_CTS_B	TERMPWR (SCSI)	D21	PERROR	COM3_RT_A
20	GND	MOUSE_CLK	D22	SELECT	COM3_RT_B
21	COM4_DCD_A	MOUSE_DATA	D23	nAUTOFD	COM4_RTS_A
22	GND	KBD_5V	GND	nFAULT	COM4_RTS_B
23	COM4_DCD_B	KBD_CLK	D24	nINIT	COM4_DSR_A
24	GND	KBD_DATA	D25	nSELECTIN	COM4_DSR_B
25	COM4_ST_A	COM2_TXD	D26	SPEAKER_OUT	COM4_DTR_A
26	GND	COM2_RXD	D27	KEYLOCK_IN	COM4_DTR_B
27	COM4_ST_B	COM2_RTS	D28	COM1_TXD	COM4_TT_A
28	GND	COM2_RI	D29	COM1_RXD	COM4_TT_B
29	COM4_RT_A	COM2_CTS	D30	COM1_RTS	COM1_DSR
30	GND	COM2_DTR	D31	COM1_CTS	COM1_RI
31	COM4_RT_B	COM2_DCD	GND	COM1_DTR	GND
32	GND	COM2_DSR	+5V	COM1_DCD	+5V

VMEbus Signal Descriptions

The VMEbus signals occupy rows a, b and c of the P1 connector and row b of the P2 connector.

Mnemonic	Signal Description
A01 to A15	**Address Bus (bits 1 to 15).** Address lines that are used to broadcast a short address
A16 to A23	**Address Bus (bits 16 to 23).** Address lines that are used with A01 to A15 and LWORD~ to broadcast a standard address
A24 to A31	**Address Bus (bits 24 to 31).** Address lines that are used with A01 to A23 and LWORD~ to broadcast an extended or 64-bit address
ACFAIL~	**AC Failure.** This shows that the AC input to the power supply is no longer being provided or that the required AC input voltage levels are not being met
AM0 to AM5	**Address Modifier (bits 0 to 5).** These are used to broadcast information such as the address size, cycle type, master identification or any combination of these
AS~	**Address Strobe.** This shows when a valid address has been placed on the address bus
BBSY~	**Bus Busy.** This is driven low by the requester associated with the current bus master to show that the master is using the bus
BCLR~	**Bus Clear.** This is generated by an arbiter to show that there is a higher priority request for the bus than the one being processed. This requests the current master to release the bus
BERR~	**Bus Error.** This is generated by a slave or bus timer to tell the master that the data transfer did not complete
BG0IN~ to BG3IN~	**Bus Grant (0 to 3) In.** These signals are generated by the arbiter to tell the board receiving it that if it is requesting the bus on that level, then it has been granted use of the bus. Otherwise the board should pass the signal down the daisy chain. The BGxIN~/BGxOUT~ signals form the bus grant daisy chain, i.e. the BGxOUT~ of one board forms the BGxIN~ of the next board in the daisy chain
BG0OUT~ to BG3OUT~	**Bus Grant (0 to 3) Out.** These signals are generated by requesters to tell the next board in the daisy chain that if it is requesting the bus on that level, then it can use the bus. Otherwise the board should pass the signal down the daisy chain
BR0~ to BR3~	**Bus Request (0 to 3).** A low level, generated by a requester, on one of these lines, shows that some master needs to use the bus.
D00 to D31	**Data Bus.** These are used to transfer data between masters and slaves, and status/ID information from interrupters to interrupt handlers
DS0~, DS1~	**Data Strobe 0, 1.** These are used with LWORD~ and A01 to show how many byte locations are being accessed (1, 2, 3 or 4). Also, during a write cycle, the falling edge of the first data strobe shows that valid data is available on the bus. On a read cycle, the rising edge of the first data strobe shows that data has been accepted from the data bus
DTACK~	**Data Transfer Acknowledge.** This signal is generated by a slave. The falling edge shows that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. The rising edge shows that the slave has released the data bus at the end of a read cycle
GND	The DC voltage reference for the system
IACK~	**Interrupt Acknowledge**. This is used by the interrupt handler to acknowledge an interrupt request. It is routed to the IACKIN~ pin of slot 1, where it is monitored by the IACK daisy chain driver

Mnemonic	Signal Description
IACKIN~	**Interrupt Acknowledge In.** This tells the board receiving it that that board can respond to the interrupt acknowledge cycle in process or pass it down the daisy chain. IACKIN~/IACKOUT~ form the interrupt acknowledge daisy chain
IACKOUT~	**Interrupt Acknowledge Out.** This is sent by a board to tell the next board in the daisy chain that it can respond to the interrupt acknowledge cycle in progress
IRQ1~ to IRQ7~	**Interrupt Request (1 to 7).** These are driven low by interrupters to request an interrupt on the corresponding level.
LWORD~	**Longword.** This is used with DS0~, DS1~ and A01 to select which byte location(s) within the 4-byte group are accessed during the data transfer.
Reserved	This signal is reserved for future enhancements of the VME specification.
SERA	The serial clock used to synchronise the data transmission on the serial bus.
SERB	This is used for serial data transmission.
SYSCLK	**System Clock.** This provides a constant 16 MHz clock signal that is independent of any other bus timing
SYSFAIL~	**System Fail.** This shows that a failure has occurred in the system. This signal can be generated by any board in the system
SYSRESET~	**System Reset.** When this is low, it causes the system to be reset.
WRITE~	**Write.** This is generated by a master to show whether the data transfer cycle is a read or a write
+5VSTDBY	**+5 Volts DC Standby.** This supplies +5V DC to devices requiring battery back-up.
+5V	+5 Volts DC power
+12V	+12 Volts DC power
-12V	-12 Volts DC power
GA0~ to GA3~	**Geographic Address**. These are used to set the slave VME address of the board.

P2 I/O Signal Descriptions

Mnemonic	Description
FLPRGEN~	Flash programming voltage enable
DB0~ to DB7~	SCSI bus data
DBP~	SCSI bus data parity
ATN~	SCSI bus Attention
BSY~	SCSI bus Busy
ACK~	SCSI bus Acknowledge
RST~	SCSI bus Reset
MSG~	SCSI bus Message phase
SEL~	SCSI bus Select
C/D	SCSI bus Command/Data phase
REQ~	SCSI bus Request
I/O	SCSI bus I/O phase
TERMPWR	**SCSI bus terminator power.** Supplies power for external SCSI bus terminators. Fused at 1 Amp
MOUSE_CLK	**Mouse Clock.** Clock drive for mouse
MOUSE_DATA	**Mouse Data.** Mouse data line
KBD_5V	**Keyboard 5V.** Supplies power for the keyboard and mouse. Fused at 1 Amp
KBD_CLK	**Keyboard Clock.** Clock drive for the keyboard
KBD_DATA	**Keyboard Data.** Keyboard data line
COM1/2_TXD	COM1/2 Transmit Data
COM1/2_RXD	COM1/2 Receive Data
COM1/2_RTS	COM1/2 Request-To-Send
COM1/2_RI	COM1/2 Ring Indicator
COM1/2_CTS	COM1/2 Clear-To-Send
COM1/2_DTR	COM1/2 Data Terminal Ready
COM1/2_DCD	COM1/2 Data Carrier Detect
COM1/2_DSR	COM1/2 Data Set Ready
KEYLOCK_IN	**Keylock input.** Used to detect the state of an external keyswitch. May be used to implement system password protection
SPEAKER_OUT	**Loudspeaker Output.** Outputs a mono mix of Business Audio line-out and Timer2 Audio. May be used to drive 4R or 8R loudspeaker
nSELECTIN	Parallel port Select In
nINIT	Parallel port INIT
nFAULT	Parallel port FAULT
nAUTOFD	Parallel port AUTOFD
SELECT	Parallel port SELECT
PERROR	Parallel port PERROR

Mnemonic	Description
BUSY	Parallel port BUSY
nACK	Parallel port ACK
D1 to D8	Parallel port data bits
nSTROBE	Parallel port STROBE
+12V	**12 Volts.** Fused at 1 Amp to power external Ethernet transceiver. Also used by P2 adapter
Receive+/-	10Base5 receive data
Transmit+/-	10Base5 transmit data
Collision+/-	10Base5 collision
TX+/-	10BaseT transmit data
RX+/-	10BaseT receive data
COM3/4_TXD_A	RS422 or RS232 Transmit Data
COM3/4_TXD_B	RS422 Transmit Data
COM3/4_RXD_A	RS422 or RS232 Receive Data
COM3/4_RXD_B	RS422 Receive Data
COM3/4_CTS_A	RS422 or RS232 Clear To Send
COM3/4_CTS_B	RS422 Clear To Send
COM3/4_DCD_A	RS422 or RS232 Data Carrier Detect
COM3/4_DCD_B	RS422 Data Carrier Detect
COM3/4_RTS_A	RS422 or RS232 Ready To Send
COM3/4_RTS_B	RS422 Ready To Send
COM3/4_DSR_A	RS422 or RS232 Data Set Ready
COM3/4_DSR_B	RS422 Data Set Ready
COM3/4_DTR_A	RS422 or RS232 Data Terminal Ready
COM3/4_DTR_B	RS422 Data Terminal Ready
COM3/4_ST_A/B	RS422 Send Timing
COM3/4_RT_A/B	RS422 Receive Timing
COM3/4_TT_A/B	RS422 Terminal Timing

PMC Connectors

J11 PMC Connector Pinout

Pin	Signal	Pin	Signal
1	NC	2	-12V
3	GND	4	INTA#
5	INTB#	6	INTC#
7	BUSMODE1#	8	+5V
9	INTD#	10	NC
11	GND	12	NC
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	+5V
19	+5V	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3#
27	AD22	28	AD21
29	AD19	30	+5V
31	+5V	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5V
39	GND	40	LOCK#
41	NC	42	NC
43	PAR	44	GND
45	+5V	46	AD15
47	AD12	48	AD11
49	AD09	50	+5V
51	GND	52	C/BE0#
53	AD06	54	AD05
55	AD04	56	GND
57	+5V	58	AD03
59	AD02	60	AD01
61	AD00	62	+5V
63	GND	64	REQ64#†

† REQ64# is only connected to a 4k7 pull-up.

J12 PMC Connector Pinout

Pin	Signal	Pin	Signal
1	+12V	2	NC
3	NC	4	NC
5	NC	6	GND
7	GND	8	NC
9	NC	10	NC
11	BUSMODE2#‡	12	3.3V†
13	RST#	14	BUSMODE3#¥
15	3.3V†	16	BUSMODE#4¥
17	NC	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	3.3V†
25	IDSEL	26	AD23
27	3.3V†	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2#
33	GND	34	NC
35	TRDY#	36	3.3V†
37	GND	38	STOP#
39	PERR#	40	GND
41	3.3V†	42	SERR#
43	C/BE1#	44	GND
45	AD14	46	AD13
47	GND	48	AD10
49	AD08	50	3.3V†
51	AD07	52	NC
53	3.3V†	54	NC
55	NC	56	GND
57	NC	58	NC
59	GND	60	NC
61	ACK64#‡	62	3.3V†
63	GND	64	NC

† The 3.3V pins are not connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on P0, and capacitively decoupled to ground.

‡ BUSMODE2# and ACK64# are only connected to 4k7 pullups.

¥ BUSMODE3# and BUSMODE4# are only connected to 1k pulldowns.

PMC Signal Descriptions

Mnemonic	Description
AD0 to AD31	**Address/Data bits.** Multiplexed address and data bus
C_BE0 to C_BE3	**Command/Byte Enables.** During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus
FRAME~	**FRAME.** Driven low by the current master to signal the start and duration of an access
DEVSEL~	**Device Select.** Driven low by a PCI agent to signal that it has decoded its address as the target of the current access
PAR	**Parity.** Parity protection bit for AD0 to AD31 and BE0 to BE3
IRDY~	**Initiator Ready.** Driven low by the initiator to signal its ability to complete the current data phase
LOCK~	**LOCK.** Driven low to indicate an atomic operation that may require multiple transactions to complete
BUSMODE1#	**Bus Mode 1.** Driven low by a PMC module if it supports the current bus mode
BUSMODE2#, BUSMODE3# and BUSMODE4#	**Bus mode.** Driven by the host to indicate the bus mode. On the PPC2A this is always PCI
RST~	**Reset.** Driven low to reset the PCI bus
TRDY~	**Target Ready.** Driven low by the current target to signal its ability to complete the current data phase
PERR~	**Parity Error.** Driven low by a PCI agent to signal a parity error
SERR~	**System Error.** Driven low by a PCI agent to signal a system error
STOP~	**STOP.** Driven low by a PCI target to signal a disconnect or target-abort
INTA~ to INTD~	**Interrupt lines.** Level-sensitive, active-low interrupt requests
CLK	**Clock.** All PCI bus signals except RST~ are synchronous to this 33 MHz clock
REQ~	**Request.** Driven low by a PCI agent to request ownership of the PCI bus
GNT~	**Grant.** Driven low by the arbiter to grant PCI bus ownership to a PCI agent
IDSEL	**Initialisation Device Select.** Device chip select during configuration cycles
NC	**No connection**

J14 PMC I/O Connector Pinout

J14 is routed to P0.

Pin Number	Signal	Pin Number	Signal
1	PMC_IO_1	2	PMC_IO_2
3	PMC_IO_3	4	PMC_IO_4
5	PMC_IO_5	6	PMC_IO_6
7	PMC_IO_7	8	PMC_IO_8
9	PMC_IO_9	10	PMC_IO_10
11	PMC_IO_11	12	PMC_IO_12
13	PMC_IO_13	14	PMC_IO_14
15	PMC_IO_15	16	PMC_IO_16
17	PMC_IO_17	18	PMC_IO_18
19	PMC_IO_19	20	PMC_IO_20
21	PMC_IO_21	22	PMC_IO_22
23	PMC_IO_23	24	PMC_IO_24
25	PMC_IO_25	26	PMC_IO_26
27	PMC_IO_27	28	PMC_IO_28
29	PMC_IO_29	30	PMC_IO_30
31	PMC_IO_31	32	PMC_IO_32
33	PMC_IO_33	34	PMC_IO_34
3	PMC_IO_35	36	PMC_IO_36
37	PMC_IO_37	38	PMC_IO_38
39	PMC_IO_39	40	PMC_IO_40
41	PMC_IO_41	42	PMC_IO_42
43	PMC_IO_43	44	PMC_IO_44
45	PMC_IO_45	46	PMC_IO_46
47	PMC_IO_47	48	PMC_IO_48
49	PMC_IO_49	50	PMC_IO_50
51	PMC_IO_51	52	PMC_IO_52
53	PMC_IO_53	54	PMC_IO_54
55	PMC_IO_55	56	PMC_IO_56
57	PMC_IO_57	58	PMC_IO_58
59	PMC_IO_59	60	PMC_IO_60
61	PMC_IO_61	62	PMC_IO_62
63	PMC_IO_63	64	PMC_IO_64

P0 Connector Pinout

P0 is routed to J14.

Pin Number	Row A	Row B	Row C	Row D	Row E	Row F
1	BITEMON~	SYSFAIL~	EXTRESET~			GND
2	INTER~	OFFLINE~	EXTABORT~			GND
3	3.3V†	3.3V†	3.3V†	+5V	+5V	GND
4	PMC_IO_5	PMC_IO_4	PMC_IO_3	PMC_IO_2	PMC_IO_1	GND
5	PMC_IO_10	PMC_IO_9	PMC_IO_8	PMC_IO_7	PMC_IO_6	GND
6	PMC_IO_15	PMC_IO_14	PMC_IO_13	PMC_IO_12	PMC_IO_11	GND
7	PMC_IO_20	PMC_IO_19	PMC_IO_18	PMC_IO_17	PMC_IO_16	GND
8	PMC_IO_25	PMC_IO_24	PMC_IO_23	PMC_IO_21	PMC_IO_21	GND
9						GND
10						GND
11						GND
12	PMC_IO_30	PMC_IO_29	PMC_IO_28	PMC_IO_27	PMC_IO_26	GND
13	PMC_IO_35	PMC_IO_34	PMC_IO_33	PMC_IO_32	PMC_IO_31	GND
14	PMC_IO_40	PMC_IO_39	PMC_IO_38	PMC_IO_37	PMC_IO_36	GND
15	PMC_IO_45	PMC_IO_44	PMC_IO_43	PMC_IO_42	PMC_IO_41	GND
16	PMC_IO_50	PMC_IO_49	PMC_IO_48	PMC_IO_47	PMC_IO_46	GND
17	PMC_IO_55	PMC_IO_54	PMC_IO_53	PMC_IO_52	PMC_IO_51	GND
18	PMC_IO_60	PMC_IO_59	PMC_IO_58	PMC_IO_57	PMC_IO_56	GND
19	+5V	PMC_IO_64	PMC_IO_63	PMC_IO_62	PMC_IO_61	GND

† The 3.3V pins are not connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on J12, and capacitively decoupled to ground.

The BITEMON~, SYSFAIL~, EXTRESET~, INTER~, OFFLINE~ and EXTABORT~ signals are used by the Debug Port Adapter Box. The SYSFAIL~ and OFFLINE~ signals can be used to drive LEDs directly.

Note: You are recommended not to route analogue signals through P0.

P9 Floppy Disk Drive Connector Pinout

Pin	Signal	Pin	Signal
1	GND	2	Density Select 0
3	GND	4	NC
5	GND	6	Density Select 1
7	GND	8	Index#
9	GND	10	Motor Select 0#
11	GND	12	Drive Select 1#
13	GND	14	Drive Select 0#
15	GND	16	Motor Select 1#
17	GND	18	Direction#
19	GND	20	Step#
21	GND	22	Write Data#
23	GND	24	Write Gate#
25	GND	26	Track 0#
27	GND	28	Write Protect#
29	GND	30	Read Data#
31	GND	32	Head Select#
33	NC	34	Disk Change#

P8 RISCWatch Connector Pinout

This connector allows the connection of software debugging tools that use the processor's JTAG port to control the operation of the processor.

Pin	Signal	Pin	Signal
16	GND	15	CKSTP~
14	Reserved	13	HRESET~
12	Reserved	11	SRESET~
10	Reserved	9	TMS
8	Reserved	7	TCK
6	+3.3V Pullup	5	Reserved
4	TRST~	3	TDI
2	Reserved	1	TDO

RISCWatch Connector Signal Descriptions

Signal	Description
GND	Signal ground
CKSTP~	Processor Checkstop input
HRESET~	Processor Hard Reset
SRESET~	Processor Soft Reset
TMS	Processor JTAG Test Mode Select
TCK	Processor JTAG Test Clock
+3.3V Pullup	Power-on status signal to RISCWatch hardware
TRST~	Processor JTAG Test Reset
TDI	Processor JTAG Test Data In
TDO	Processor JTAG Test Data Out

P6 JTAG Connector Pinout

The JTAG connector is for factory test purposes only. It has the following pinout:

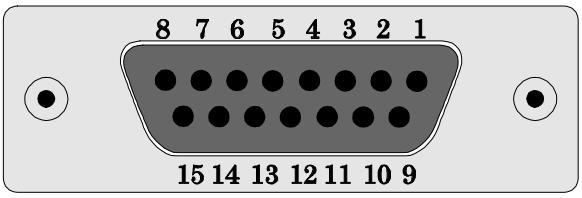
Pin	Signal	Pin	Signal
1	HRESET~	2	TDI_VME
3	TCK	4	TRST~
5	TMS_60X	6	TMS_106
7	TMS_VME	8	TDI_60X
9	TDO_60X	10	TDI_106
11	TDO_106	12	BGCPU~
13	TDO_VME	14	BRCPU~
15	GND	16	GND
17	TT(1)	18	TT(0)
19	TT(3)	20	TT(2)
21	TBRST~	22	TT(4)
23	GND	24	GND
25	TA~	26	AACK~
27	ARTRY~	28	TEA~
29	TS~	30	DBG~

J3 Connector Pinout

Pin	Signal
1	-
2	-
3	COM1_CTS
4	BITEMON~
5	5V_OUT_FUSED
6	-
7	COM2_RXD
8	INTER~
9	EXTRESET~
10	GND
11	COM2_TXD
12	COM1_RXD
13	EXTABORT~
14	COM1_RTS
15	COM1_TXD

See the P2 Signal Descriptions section for descriptions of the COM1 and COM2 signals. The BITEMON~, INTER~, EXTRESET~, EXTABORT~ and 5V_OUT_FUSED signals are used by the Debug Port Adapter Box.

Figure 5-1. J3 Pinout



Chapter 6 - Front Panel

This chapter describes the features found on the PPC2A front panel.

PMC Slot

Air Cooled Versions

There is one PMC slot in the front panel, however if you have not ordered a PMC module for the PMC site, or the slot is unavailable because the PMCC2 is fitted, then Radstone will fit a blanking plate in the slot for EMC protection.

If you are fitting your own PMC module, then before fitting the module, remove the blanking plate from the PMC slot. The PMC's bezel will fill the slot and will usually provide connection to the module. PMC modules are delivered with a full kit of parts for mounting them, and the manual for the module normally contains instructions on how to fit the module.

Conduction Cooled Version

There is a conduction cooled PMC slot in the front panel allowing limited front panel access to PCI signals.

If you are fitting your own PMC module, it must comply with the standard for rugged, conduction cooled PMC cards to ensure that it correctly mates with the PPC2A mechanics.

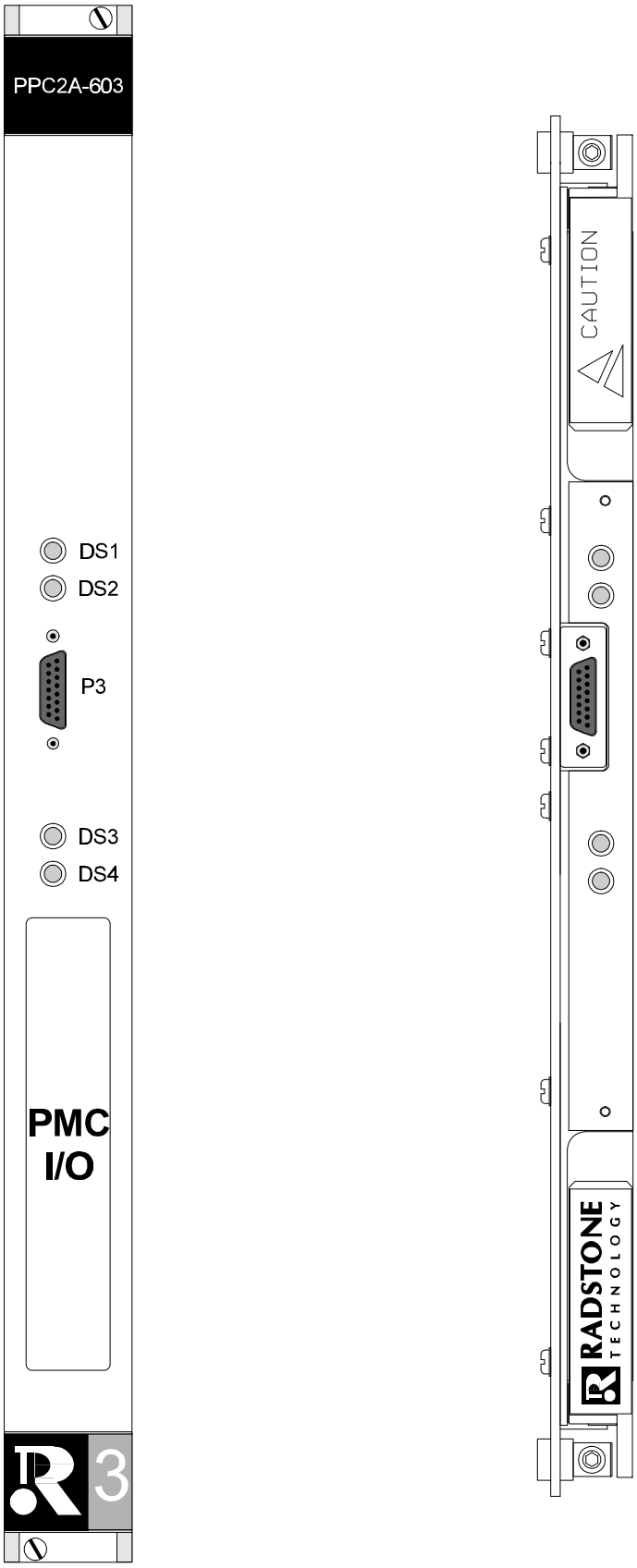
LEDs

Four software programmable LEDs (DS1 to DS4) are mounted on the front panel. DS4 is green, DS1 is red, and DS2 and DS3 are yellow. See the Software Programmable LEDs section in Chapter 9 for more details.

Connectors

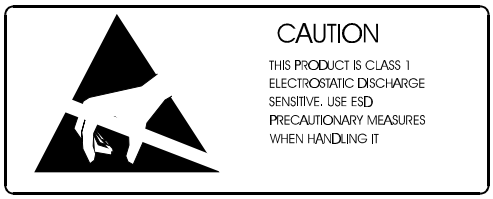
A 15-way micro-D type connector, J3, is fitted to allow debug communication to serial ports COM1 and COM2. See chapter 5 for details.

Figure 6-1. PPC2A Front Panels



Chapter 7 - Installation

This chapter describes the installation of the PPC2A board in a system.



System Backplane Configuration Links

Before plugging the PPC2A into a development rack, you should first check the rack's backplane configuration links.

Radstone enclosures usually have two sets of links in the J1 (VMEbus) half of the backplane. The upper set of four links configures the Bus Grant (BGx) daisy chain and the lower link configures the Interrupt Acknowledge (IACK) daisy chain. They are provided so that the appropriate 'In' signal (BGxIN~/IACKIN~) at a particular slot can be connected to the corresponding 'Out' signal (BGxOUT~/IACKOUT~) at the same slot. This is only necessary when a slot position is not occupied by a board and there are boards further down the daisy chain. Some backplanes have daisy chains that automatically link the signals across empty slots. See the manual appropriate to your enclosure for further details.

Note: Take extra care if you are using the PMCC2, as it occupies an extra system slot, but requires the daisy chains to be linked across the slot.

Chassis Ground

To ensure optimum operation of the air cooled PPC2A with regard to EMC, when taking I/O connections from the front panel connectors, there should always be a connection from the front panel to the chassis ground of the system. This also applies when the board is operating on a VME bus extender. When taking I/O connections from P2, use the Radstone P2 accessory kit (see Appendix A for more details), or some equivalent system.

System Configuration Suggestions

Check the J2 connections of the slot before powering up (see the Warnings in Chapter 1).

Use the suggested link configuration (see Chapter 4) for the first power-up attempt.

Use the PPC2A in a development rack on its own at first, and only plug it in with other cards later (if other cards are to be used). This enables you to prove basic operation before tackling any system configuration issues.

Chapter 4 defines the function of all the user configurable links and gives guidance on altering the PPC2A's link configuration to suit your requirements. It should be read before installing your PPC2A. Again, if possible, prove operation of the PPC2A on its own at first before integrating it into a system.

If you are using the SCSI bus, you are recommended to locate the PPC2A at one end and enable the terminator by fitting link E12. If you want to use the PPC2A somewhere other than at the end of the SCSI bus, ensure that E12 is not fitted. **Fitting E12 when the PPC2A is not located at the end of a SCSI bus may cause erroneous SCSI operation.**

The power supply to the RTC on the PPC2A is fed from the VSTANDBY pin on the VMEbus. VMEbus compliance requires this voltage to be 5V ± 5%. Fitting link E11 allows you to supply a voltage of 3V from a battery to this pin to maintain normal RTC operation. **Fitting E11 when VSTANDBY is connected to +5V may cause damage to the RTC.**

Ensure that air-cooled PPC2As receive sufficient air-flow. If you need to operate your PPC2A on an extender card, this requires an additional fan to supply the necessary air flow.

Ensure that conduction cooled PPC2As are fully installed in the conduction cooled box and that the wedgelocks are correctly tightened. If, for any reason, you need to operate the conduction cooled PPC2A on an extender card, you must maintain an airflow of 300 feet/minute over it.

To interact with the PPC2A's on-board firmware, you need to attach a serial terminal to the PPC2A. This terminal will use the serial signals on COM1 (the P3 connector gives front panel access to these signals. Alternatively, a PMC9100/PMC2-9100 graphics PMC module and a PS/2 compatible keyboard may be used. If these devices are used, the firmware detects their presence and uses them automatically.

Both the COM1 and COM2 interfaces are configured as DTE (9.6 kbaud, 8 bits/character, 1 stop bit, parity disabled). However, cables supplied by Radstone permit direct connection to a terminal without use of a null-modem.

Chapter 8 - Power-up & Operational Description

This chapter describes power-up and subsequent operation of the PPC2A.

Power-up

Having configured the backplane and taken note of the system configuration suggestions in chapter 7, with the PPC2A firmly secured in the rack, power-up the system.

The current on-board Boot firmware is described in the PPC Boot Firmware Manual, publication number RT5078.

On power-up, the PPC2A runs through a self-test routine called BIT. This is described in the accompanying release notes.

Operational Description

The on-board firmware for the PPC2A, which controls its operation after power-up, is described in separate manuals. This is because:

- The complexity of the firmware would lead to a chapter here that would be cumbersomely large and so possibly difficult to follow
- It allows changes to the firmware and corresponding manual to be made without needing to change this (hardware-oriented) manual
- It gives the possibility of offering more than one on-board firmware package
- Such documentation is often provided in an electronic on-line format, making its reproduction here unnecessary

Operating system support for the PPC2A is covered in Chapter 2.

Chapter 9 - Functional Description

This chapter gives a detailed description of the PPC2A's functional blocks.

Resetting the PPC2A

There are two types of reset that may be applied to the PPC2A: 'Hard' and 'Soft'.

Hard Reset

A hard reset resets all on-board resources and causes the processor immediately to branch to 0xFFF00100. A hard reset may be generated by:

- A power-on reset
- A reset via the front panel J3 or rear P0 connector
- A SYSRESET~ from VME
- A Watchdog timer reset
- A VME software-initiated reset
- RISCWatch and JTAG test port resets

As the hard reset signal is applied asynchronously to processor activity, it may cause a memory access to be aborted. A hard reset also disables the DRAM refresh function of the MPC106 PCI Bridge and Memory Controller. As a result, memory integrity cannot be guaranteed after a hard reset.

See the DRAM section for DRAM initialisation requirements following a hard reset.

Soft Reset

A soft reset causes the processor to reach a recoverable state and then branch to either 0x00000100 or 0xFFF00100, depending on the state of the IP bit in the processor's Machine State Register. A soft reset may generated by:

- A front panel EXTABORT~ reset via the front panel J3 or rear P0 connector
- A software controlled ALT_RST~ from the ISA bridge
- A RISCWatch test port soft reset

The standard boot firmware does not support the use of soft reset.

ISAbus Reset

The ISAbus may be reset under software control via the ISA Clock Divider register in the 82378ZB ISA bridge.

Memory Maps

The PPC2A supports both contiguous and non-contiguous PReP compliant memory maps. The following descriptions relate to the contiguous map unless otherwise stated. No fixed addresses are given for PCI connected resources (SCSI, Ethernet, VME bridge and PMC slots) since these addresses are configured by the boot process.

Memory Map Seen by the Processor

Processor Address Range		PCI Address Range	Cycle Type
00000000	7FFFFFFF	No PCI cycle	System memory space
80000000	8000FFFF	00000000 to 0000FFFF	ISA/PCI I/O space
80010000	807FFFFF	Reserved	Reserved
80800000	80FFFFFF	00800000 to 00FFFFFF	Alternate PCI configuration space
81000000	BF7FFFFF	01000000 to 3F7FFFFF	PCI I/O space
BF800000	BFFFFFEF	Reserved	Reserved
BFFFFFF0	BFFFFFFF	3FFFFFF0 to 3FFFFFFF	PCI/ISA interrupt acknowledge
C0000000	C07FFFFF	00000000 to 007FFFFF	User Flash ROM or PCI memory space
C0800000	C087FFFF	00800000 to 0087FFFF	NOVRAM
C0880000	FEFFFFFF	00880000 to 3EFFFFFF	PCI memory space
FF000000	FFEFFFFF	No PCI cycle	Reserved
FFF00000	FFFFFFFF	No PCI cycle	Flash boot ROM

PCI Memory Space Seen by the PCI Master

PCI Memory Address Range		Local Memory Cycle	Cycle Type
00000000	007FFFFF	No local memory cycle	User Flash ROM or PCI memory space
00800000	0087FFFF	No local memory cycle	NOVRAM
00880000	7EFFFFFF	No local memory cycle	PCI memory space
7F000000	7FFFFFFF	No local memory cycle	Reserved
80000000	FFFFFFFF	00000000 to 7FFFFFFF	System memory space

PCI I/O Space Seen by the PCI Master

PCI I/O Address Range		Local Memory Cycle	Cycle Type
00000000	0000FFFF	No local memory cycle	ISA/PCI I/O space
00010000	007FFFFF	No local memory cycle	Reserved
00800000	3F7FFFFF	No local memory cycle	PCI I/O space
3F800000	3FFFFFFF	No local memory cycle	Reserved
40000000	FFFFFFFF	No local memory cycle	Reserved

MPC106 PCI Bridge and Memory Controller

The Motorola MPC106 PCI Bridge and Memory Controller provides the host bridge between the processor bus and the PCI, a DRAM memory controller, the L2 cache controller, the Flash boot ROM interface and a central arbiter for the processor bus.

Second Level Cache

The size of the L2 cache (1 Mbyte) is reflected in the Equipment Present Register 1 (see the Control and Status Registers section). Operation of the L2 cache must be set up in the MPC106 PCI Bridge/Memory Controller. It may be configured for write-through or write-back operation, with or without parity.

Memory addresses in the range 0x00000000 to 0x40000000 (i.e. the lowest 1 Gbyte of the processor's memory map) are cacheable by the L2 cache.

Note: Accesses to this address range from the PCI bus are *not* cacheable.

Cache access times from the processor, referenced to the 66 MHz processor bus clock, for a 32-byte burst, are shown in the following table:

	66 MHz Clock	
Type	**Cycles**	**Transfer Rate (Mbytes/second)**
Burst read hit non-pipelined	3-1-1-1	356
Burst read hit pipelined	2-1-1-1	427

DRAM

The options available for DRAM on-board the PPC2A are shown in the following table:

DRAM Size (Mbytes)	Banks	Organisation
32	1	4M x 72
64	2	8M x 72

The DRAM is protected by eight ECC bits per 64 data bits. All single bit, double bit and nibble errors can be detected, and single bit errors can be corrected.

Following a hard reset, the MPC106 PCI Bridge/Memory Controller must be set up for the size and number of banks of DRAM (including any DRAM on a PMCC2) and the appropriate number of wait states to match the DRAM speed. This is done by the standard boot monitor firmware. The size and speed of motherboard DRAM may be checked by reading the Memory Size, Memory Presence and Memory Type Motherboard registers (see the Control and Status Registers section). At least 100µs must have elapsed from the negation of reset before enabling the DRAM. After being enabled, the DRAM must not be accessed until at least 8 refreshes have occurred. If ECC is to be enabled, it is then necessary to initialise the DRAM to set-up valid ECC bits.

DRAM access times from the processor, referenced to the 66 MHz processor clock, for a 32-byte burst assuming RAS~ has been precharged, are shown in the following table:

	Clock Cycles Initial Access/Subsequent	Equivalent Transfer Rate (Mbytes/second)
60ns DRAM sustainable burst at 66MHz bus clock without ECC	8-3-3-3	125
60ns DRAM sustainable burst at 66MHz bus clock with ECC	10-4-4-4	106
60ns DRAM sustainable burst at 33MHz bus clock without ECC	6-2-2-2	89
60ns DRAM sustainable burst at 33MHz bus clock with ECC	8-4-4-4	59

DRAM access times from the PCI, referenced to the 33 MHz PCI clock, for a 32-byte burst with no interference from L1 or L2 caches, are shown in the table:

	Clock Cycles Initial Access/Subsequent	Equivalent Transfer Rate (Mbytes/second)
Burst read	4-1-2-1-2-1-2-1	76
Burst write	2-1-1-1-1-1-1-1	118

Flash Boot ROM

The PPC2A is fitted with a 1 Mbyte Flash PROM, which holds the boot monitor firmware. This is a 12V programmable Flash component, supplied by an on-board 12V generator to allow on-board programming of the boot firmware. If boot code is lost or corrupted, the VME boot option allows the boot Flash to be rewritten.

Protection of the boot Flash against inadvertent store or erase cycles is provided by link E8 and P2 pin Z1. Either link E8 must be fitted or P2 pin Z1 must be grounded before the 12V programming voltage can be enabled.

VME Boot Option

Fitting link E2 (see Chapter 4) allows the PPC2A to boot using code held in memory located on the VMEbus. This operation relies on the factory default power-up configuration for the VMEbus interface (see page 4-6). The VME memory must be located in A32 space at address 0xFFF00000 and must be 32 bits wide (D32).

In this mode, you can map the Flash boot ROM to address 0xFF000000 by setting the Configuration bit CF_FF0_LOCAL in Grackle register 0xA8. You can now read from and write to the Flash boot ROM as the most significant byte of every 8-byte-aligned address.

Once you have programmed the Flash boot ROM, remove link E2 and carry out a hard reset. Normal booting now occurs from the Flash boot ROM at address 0xFFF00000.

Peripheral Component Interconnect

The PCI is a high performance synchronous bus running at 33 MHz. The PPC2A implements a 32-bit PCI bus with burst data rates up to 132 Mbytes/second between PCI agents. The PCI bus structure of the PPC2A is shown in the block diagram in Chapter 2.

PCnet-PCI Ethernet Controller

The AM79C970 PCnet-PCI supports ANSI 802.3 10Base5 and Ethernet standards, and has a direct interface to the PCI bus. It has 136-byte transmit and 128-byte receive FIFOs, and a 32-bit DMA controller for access to data and descriptors in system memory. The network address is factory configured and held in a serial E^2PROM. The PCnet-PCI requires 32 bytes of PCI I/O space. It cannot be accessed in PCI memory space.

Connection to the AUI is made through the P2 connector. Pinouts are given in Chapter 5. Three status LEDs (DS101 to DS103) are mounted on the back of the board behind the front panel (see the Software Programmable LEDs section). The default functions of these LEDs are receive status, link status and transmit status respectively. This may be overridden by the software.

As a build option, the Ethernet port can be configured for 10BaseT operation, instead of 10Base5. Pinouts are given in Chapter 5.

NCR53C860 SCSI Scripts Processor

The NCR53C860 SIOP executes commands, in the form of SCSI scripts. It has a PCI interface and DMA controller, which are used to access the scripts and data held in system memory. The SIOP can transfer data at 5 Mbytes/second asynchronously and, with an Ultra SCSI compliant target, 20 Mbytes/second synchronously (or 10 Mbytes/second with a non Ultra SCSI compliant target). The SIOP requires 256 bytes of either PCI memory or I/O space.

Connection to the SCSI bus is made through the P2 connector; the pinout is given in Chapter 5.

The PPC2A has an on-board active SCSI terminator, which may be enabled or disabled with a jumper (see the E12 description in Chapter 4). The SCSI specification allows a maximum cable stub length of 10 cm. If the SCSI bus connections are taken directly from the backplane J2 connector, then the PPC2A may be located anywhere on the SCSI bus and the terminator should only be enabled if the PPC2A is at the end of the SCSI bus. Otherwise, the PPC2A must be at the end of the SCSI bus and the terminator must be enabled.

A software programmable SCSI Activity LED (DS 104) is mounted on the back of the board behind the front panel. See the Software Programmable LEDs section and the SCSI LED Register description for more details.

Universe VMEbus Bridge

The CA91C142 Universe VMEbus interface chip provides all slot 1 (system controller) functions, interrupt control, a DMA controller, interprocessor communications and block transfer support. The Universe chip requires 64 Kbytes of PCI I/O space for control and status registers. Appendix A details the VMEbus compliance of the PPC2A.

VMEbus Master Access

Eight general purpose software programmable PCI slave images are available for access to the VMEbus. All of these can be configured to access VMEbus A32, A24 or A16 address space. An offset may be applied to translate the local address to a different address on the VMEbus, allowing any local address to access any VMEbus address. The start and end addresses of the A32, A24 and A16 PCI slave images may be set on any 64 Kbyte boundary in PCI memory or I/O space that is not allocated to other devices. One image may be set on 4 Kbyte boundaries to accommodate access to A16 space.

One further, special purpose, PCI slave image allows mapping of A16 and A24 space. This slave image uses a 64 Mbyte window, aligned to any 64 Mbyte address in PCI memory space. The window is divided into four 16 Mbyte quadrants. The top 64 Kbytes of each quadrant maps to A16 space, while the rest of each quadrant maps to A24 space. The Address Modifiers generated are software configurable for each quadrant.

VMEbus master cycles may be coupled or write posted. Coupled cycles are not terminated on the PCI until all data has been transferred over the VMEbus. Posted writes are queued in a FIFO until the VMEbus is available for the data to be transferred.

VMEbus Slave Access

Eight general purpose software programmable VMEbus slave images are available. All of these may be defined in VMEbus A32, A24 or A16 space. An offset may be applied to translate the VMEbus address to a different address on the local bus, allowing any VMEbus address to access any on-board address. The start and end addresses of the A32, A24 and A16 images may be set on any 64 Kbyte boundary. Two images may be set on 4 Kbyte boundaries to accommodate access to A16 space.

A further, special purpose, VMEbus slave image allows access to the Universe chip registers.

VMEbus slave accesses to the PPC2A may be coupled, write posted or prefetched block read. Coupled slave transfers can only proceed once the slave posted write FIFO is empty. Slave posted write cycles are queued in a FIFO until the PCI is available for the data to be transferred.

Typical single cycle access times, DS~ to DTACK~, are:

Slave DRAM read = 460 ns

Slave DRAM write = 360 ns

Slave posted write = 100 ns

Indivisible Cycles on VME

The Universe chip may be programmed to generate RMW cycles on the VMEbus. Data from the read portion is compared with a 32-bit compare value, qualified with a 32-bit mask. If the comparison is true, then those bits enabled by the mask are swapped with a 32-bit swap field. Alternatively, the Universe chip's VMEbus ownership bit may be set to cause it to acquire and hold ownership of the VMEbus. This method can be used in combination with PCI LOCK cycles to guarantee exclusive access to a VMEbus resource.

The VMEbus slave images may be programmed to generate locked cycles on the PCI to handle RMW cycles. The Universe chip also supports VMEbus lock commands using ADOH cycles.

VMEbus Arbitration

The Universe chip's VMEbus arbiter supports PRI and RRS arbitration with BCLR~ generation in priority mode.

The VMEbus requester may operate in fair or demand mode and may be configured as RWD or ROR.

1. When System Controller:

Period	Typical (ns)
BRx~(low) to BGxOUT~(low) when bus free	125
BBSY~(high) to BGxOUT~(low)	78

2. When non System Controller:

Period	Typical (ns)
BGxIN~(low) to BGxOUT~(low)	32

There is a limitation in the Tundra Universe VME Controller chip (CA91C042), specifically in its handling of VME bus request levels. This limitation and some suggested solutions are described below:

The Universe is designed to participate in VME bus arbitration handshaking. When it receives a VME bus grant, it either accepts bus ownership or passes the grant down the daisy chain to the next module. However, if the Universe receives an incoming bus grant and simultaneously makes a VME bus request on the same level, it may pass along the grant for a few nanoseconds and then retract it. The next board in the daisy chain could interpret this as a bus grant and assume VME bus mastership, leading to two boards trying to be VME bus Masters.

Radstone have installed a simple filter to prevent this problem on the BGOUT3 line, but is unable to do so on the BGOUT0, BGOUT1 or BGOUT2 lines.

Suggested solutions to cure the problem are:

1. Run the PPC2A at a different bus request level to other VME bus Masters.
2. Run the PPC2A at bus request level 3.
3. Fit 270pF capacitors to the backplane on the BGOUT0, BGOUT1 and BGOUT2 daisy chain lines.

VMEbus Master Block Transfers

The Universe chip's DMA controller may be used to transfer data between the PCI and the VMEbus using D32 or D64 transfers. DMA operations on the two buses are decoupled through a bi-directional FIFO.

The DMA controller may transfer multiple blocks of data using entries in a linked-list. It can also pack and unpack data to support differing data widths on the PCI and the VMEbus.

VMEbus Slave Block Transfers

The VMEbus slave interface can respond to D32:BLT and D64:MBLT block transfers. The Universe chip may be programmed to pre-fetch read data for VMEbus slave block transfers, which is queued in a FIFO.

VMEbus Interrupts

If the Universe chip is programmed accordingly, it responds to a VMEbus interrupt with a VMEbus interrupt acknowledge cycle. The Universe chip captures the status/ID and then raises an interrupt on the PCI when the VMEbus interrupt has been acknowledged. No further VMEbus interrupts are handled on that level until the processor reads the status/ID and re-arms the interrupt handler. The Universe chip can be programmed to generate any level of VMEbus interrupt.

Mailboxes and Location Monitor

The Universe II includes four 32-bit mailbox registers that can be initialised so that when data is written to them, an interrupt is generated on either the PCI or VME bus.

The Universe II's location monitor function allows events to be broadcast across the VMEbus backplane. Each Universe that shares the same enabled location monitor image responds to a read or write in that range by generating one of four internal Universe interrupts. Each of these can be individually enabled and mapped to specific PCI interrupts. If a Universe II initiates such a cycle, it should properly terminate it by asserting DTACK. Otherwise, another agent is responsible for doing so.

Semaphores

The Universe II has eight semaphores, accessible from two registers in the normal register space. Each of these registers has a status bit and an associated 7-bit tag field. Designers can use the semaphores to ensure exclusive access to system resources on either of the two busses (PCI or VME).

VMEbus Bus Errors

Assertion of VMEbus BERR~ during a coupled VMEbus master cycle causes a target-abort (bus error) on the PCI. A PCI target-abort during a coupled VMEbus slave cycle causes BERR~ on the VMEbus. See the Machine Check Exception section for further details of target abort.

A bus error during posted write transfers raises an interrupt to the processor (if enabled). Several options are available, including stopping the operation and purging the offending transaction.

A bus error during a DMA operation raises an interrupt and stops the operation on the bus where the error was detected.

VMEbus Retries

The Universe chip, as a PCI target, retries the PCI master under the following conditions:

- The PCI initiator requests a coupled cycle to the VMEbus while the Universe is not VMEbus master
- The PCI initiator requests a coupled cycle to the VMEbus while the posted write FIFO still contains data
- The PCI initiator requests a posted write cycle when the posted write FIFO cannot accept any more entries

VMEbus Reset Options

Several Universe chip operating features are set at power-up or reset by surface mount jumpers. See page 4-6 for the default options.

PMC Site

The PPC2A has a set of connectors (J11, J12 and J14) to allow a standard PMC to be connected to the PCI bus. Air-cooled PMCs are defined in IEEE 1386, and rugged conduction cooled PMCs are defined in the Draft Standard for Conduction Cooled PMCs. The PMC I/O connector, J14, is connected to P0 to allow backplane I/O on all styles. Front panel I/O is fully supported on levels 1 to 3 and, with reduced functionality, on level 4 product. While a level 4 card can only accept a conduction cooled PMC, levels 1, 2 and 3 boards can accept either air-cooled or conduction-cooled PMCs, as long as adequate cooling is provided.

82378ZB ISAbus Bridge

The Intel 82378ZB provides a bridge from the PCI to the ISAbus for connection of lower bandwidth I/O devices. This device also provides extra functionality, as shown in the following table:

Feature	Equivalent to Function of
7 channel DMA between ISA and PCI	Two 83C37s
Timer block	82C54
Interrupt controller	Two 8259s

The ISA bridge positively decodes some I/O cycles on the PCI for internal resources. It subtractively decodes and claims all PCI memory and I/O cycles not claimed by other PCI targets and forwards them to the ISAbus.

Apart from the ISA bridge, there are no other ISAbus masters in the PPC2A architecture.

ISA Bus Peripheral Components

Floppy Disk Controller

This is software compatible with the DP8473, 765A and 82077/82078, and has DMA capability. Connection to the FDC is through an on-board header (P9). Chapter 5 gives pinouts.

Serial I/O

COM1 and COM2

These two RS232-compatible serial channels contain FIFOs, and are software compatible with the INS8250N-B, PC16550A and PC16450. The baud rates are programmable from 50 baud up to 115.2 kbaud, and the signal set provided is [TXD, RXD, RTS, CTS, DCD, DTR, DSR and RI].

Connection to the serial ports is through the P2 connector or, with reduced functionality, through the front panel mounted 15-way micro-D connector P3. See Chapter 5 for pinouts.

COM3 and COM4

These two serial channels can be configured by build options to be either RS232 or RS422/RS485. The RS232 option only provides a limited signal set [TXD, RXD, RTS, CTS, DCD, DTR and DSR]. As there are no clocking options, synchronous operation is not possible. The RS422/485 option provides a RS530 compatible signal set with full clocking options, and is designed for synchronous operation. The signal set is [TXD, RXD, RTS, CTS, DCD, DTR, DSR, ST, RT and TT] or, in RS530 terminology, [BA, BB, CA, CB, CF, CD, CC, DB, DD and DA respectively].

Both channels are provided by an 85230 ESCC, which is software compatible with the AMD 8530. The 85230 provides:

- Synchronous or asynchronous operation
- Two baud rate generators covering a range of baud rates up to 230.4 kbaud for asynchronous operation and 3.6864 Mbaud for synchronous operation
- Two DPLLs to extract a clock from a serial data stream in typical low pin-count RS485 interfaces
- Receive and transmit FIFOs
- Four DMA channels to allow simultaneous reception and transmission on both interfaces
- Several facilities to enhance operation of frame based protocols such as HDLC, X.25 etc.

See Chapter 5 for pinouts.

Parallel I/O

The parallel port provides a Centronics style printer port, giving bi-directional connection with simple software driven protocols. Connection to the parallel port is through the P2 connector. The pinout is given in Chapter 5.

Keyboard and Mouse Controller

A PS/2 compatible Keyboard and Mouse interface is provided by an Intel 82C42PE with Phoenix Multikey/42G PS/2-compatible BIOS connected to the ISAbus. Connections to the mouse and keyboard are through the P2 connector.

User Flash ROM

The PPC2A has 8 Mbytes of user Flash ROM fitted as standard. You can check the actual size of ROM fitted by reading the Equipment Present Register 2 (see the Control and Status Registers section). The Flash resides in two sites and has support for on-board programming.

For improved performance, code contained in the Flash should be executed from DRAM, so the code should be constructed to copy itself into the DRAM before execution.

Protection of the boot Flash against inadvertent store or erase cycles is provided by link E8 and P2 pin Z1. Either link E8 must be fitted or P2 pin Z1 must be grounded before the 12V programming voltage can be enabled.

CIO

The 85C36 CIO provides three independent 16-bit counter/timers that each have a resolution of 333 ns. Two of the counter/timers may be linked to form a 32-bit counter/timer.

The functions of the I/O port bits are described in the Control and Status Registers section.

Software Programmable LEDs

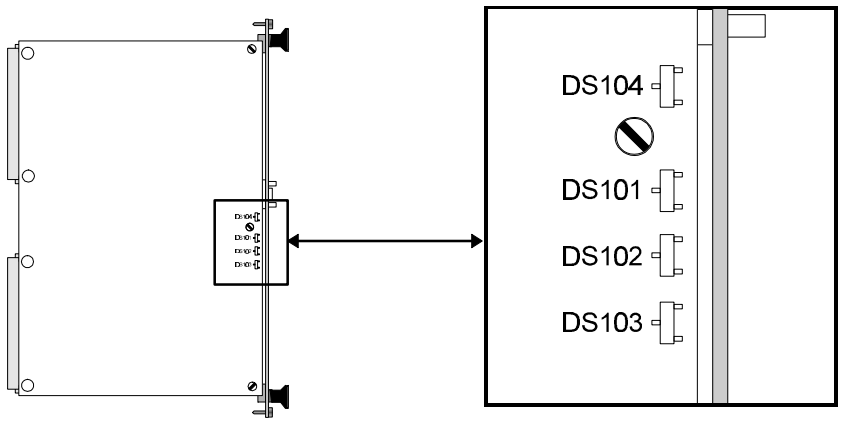
There are eight software programmable LEDs on the PPC2A.

Four of them, DS1 (red), DS2 (yellow), DS3 (yellow) and DS4 (green), are mounted through the front panel (see Figure 6-1 in Chapter 6 for the location of these LEDs). They are connected to port C of the CIO (see the CIO Port C Data Register description for more details). After power-up, DS1 is on by default.

The remaining four LEDs are all surface mounted on the reverse side of the PCB behind the front panel.

DS101, DS102 and DS103 are Ethernet status LEDs. The default functions of these LEDs are receive status, link status and transmit status respectively, but these may be overridden by the software.

DS104 is a SCSI Activity LED. See the SCSI LED Register description for more details.



RTC

A DS1285 provides the following RTC functions: year, month, date, hours, minutes and seconds. It also provides three interrupts, with separate masks: one for a time of day alarm (programmable from once per second to once per day), one for periodic rates from 122µsecs to 500msecs, and one to show that a clock update cycle is complete.

NOVRAM

A Simtek 11C68 provides 8 Kbytes of NOVRAM. This part provides read/write RAM shadowed by EEPROM with a capacity for 10,000 write cycles. The RAM is loaded from the EEPROM automatically at power up or under software control. It can also be written to as normal RAM by the ISA bus master. The RAM is stored to EEPROM under software control.

Watchdog Timer

The PPC2A contains a Maxim 706 microprocessor supervisory circuit with a watchdog timer. This timer, once enabled, must be retriggered every 1.6 seconds or a hard reset results.

Control and Status Registers

The PPC2A has a number of registers for controlling or reading the status of the hardware. The addresses shown in the following table are physical, as seen by the processor.

ISA I/O Port (Hex)	Contiguous I/O Mode Address	Description
0000 to 000F	8000 0000 to 000F	ISA Bridge DMA 1 Control
0020 & 0021	8000 0020 & 0021	ISA Bridge Interrupt 1 Control
0040 to 0043	8000 0040 to 0043	ISA Bridge Counter Control
0060	8000 0060	ISA Bridge Reset UBus IRQ12
0061	8000 0061	ISA Bridge NMI Status and Control
0064	8000 0064	Keyboard
0078 to 007B	8000 0078 to 007B	ISA Bridge BIOS Timer
0080 to 0090	8000 0080 to 0090	ISA Bridge DMA
0092	8000 0092	Port 92
0094 to 009F	8000 0094 to 009F	ISA Bridge DMA
00A0 & 00A1	8000 00A0 & 00A1	ISA Bridge Interrupt 2 Control
00C0 to 00DE	8000 00C0 to 00DE	ISA Bridge DMA 2 Control
03BC to 03BF	8000 03BC to 03BF	Parallel Port
03F8 to 03FF	8000 03F8 to 03FF	COM 1
040A to 043F	8000 040A to 043F	ISA Bridge DMA Scatter/Gather
0481 to 048B	8000 0481 to 048B	ISA Bridge DMA High Pg Registers
04D0 to 04D1	8000 04D0 to 04D1	ISA Bridge Edge/Level Control
02F8 to 02FF	8000 02F8 to 02FF	COM2
0398	8000 0398	ISA Bridge Index Register
0399	8000 0399	ISA Bridge Data Register
0803	8000 0803	DRAM Memory Bank Fitted
0804	8000 0804	DRAM Memory Bank Size
0808	8000 0808	SCSI LED
080C	8000 080C	Equipment Present #1
080E	8000 080E	Equipment Present #2
0814	8000 0814	L2 Invalidate
0818	8000 0818	Key Lock
0840	8000 0840	COM 4 Control
0841	8000 0841	COM 4 Data
0842	8000 0842	COM 3 Control
0843	8000 0843	COM 3 Data
0854	8000 0854	Board Revision

ISA I/O Port (Hex)	Contiguous I/O Mode Address	Description
0860	8000 0860	CIO Port C Data
0861	8000 0861	CIO Port B Data
0862	8000 0862	CIO Port A Data
0863	8000 0863	CIO Control
0864	8000 0864	Identity links and switches
0866	8000 0866	Memory Type Motherboard
0868	8000 0868	Memory Type Mezzanine

The ISA Bridge registers are described in more detail in the ISA Bridge documentation. The other registers are described in more detail in the following pages. The register bit significance is shown in big-endian mode (i.e. from the PowerPC603e/604e programmer's viewpoint).

Port 92 (Port 0x0092)

This register provides an alternate soft reset.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D5: Reserved

D6: Setting this bit causes the MPC106 PCI Bridge/Memory Controller to operate in little endian mode.
Clearing this bit causes the MPC106 to operate in big endian mode.
This bit may be used with D7 to ensure that both the MPC106 and the PowerPC processor switch between endian modes concurrently.

D7: Setting this bit causes a soft reset to occur. It must be cleared before another soft reset can be issued.

DRAM Memory Bank Size Register (Port 0x0803)

This register provides information on the size of each DRAM memory bank.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D3: Reserved

D4: Carrier Card banks populated MSB
0 = Less than 4 banks populated
1 = More than 3 banks populated

Note: Along with D4 and D5 of the DRAM Memory Bank Fitted register, this bit forms a 3-bit binary code indicating the number of memory banks fitted.

D5: PMCC2 memory bank size.
0 = 32 Mbytes
1 = 128 Mbytes

D6: Bank 1 size
0 = 8 Mbytes
1 = 32 Mbytes

D7: Bank 0 size
0 = 8 Mbytes
1 = 32 Mbytes

DRAM Memory Bank Fitted Register (Port 0x0804)

This register provides information on which of the eight possible DRAM memory banks are populated.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D3: Reserved

D4: PMCC2 banks populated
0 = 0, l, 4 or 5 banks populated
1 = 2 or 3 banks populated.

D5: PMCC2 banks populated LSB
0 = 0, 2, 4 or 6 banks populated
1 = 1, 3 or 5 banks populated

Note: D4 and D5, with D4 of the DRAM Memory Bank Size register, form a 3-bit binary code indicating the number of memory banks fitted.

D6: Bank 1 populated
0 = Bank populated
1 = Bank not populated

D7: Bank 0 populated
0 = Bank populated
1 = Bank not populated

SCSI LED Register (Port 0x0808)

This register allows control of the SCSI activity LED (DS104).

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D6: Reserved.

D7: SCSI activity LED
0 = LED off
1 = LED on

See the Software Programmable LEDs section for the location of this LED.

Equipment Present Register 1 (Port 0x080C)

This register provides information on hardware options and the state of the SCSI Terminator power fuse.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0: Hardware ID
This bit is clear for PPC2A

D1: SCSI_FUSE_GOOD
0 = SCSI fuse is bad
1 = SCSI fuse is good

Note: This is a resettable fuse that re-engages when the overcurrent condition is removed.

D2: Reserved.

D3: PRSNT1_1~
0 = Slot 1 PMC is present (on-board or on the PMCC2)
1 = Slot 1 is empty

D4: Reserved

D5: L2_256K
0 = L2 cache is 1 Mbyte
1 = L2 cache is 256 Kbyte

D6: Reserved

D7: L2_PRES~
0 = L2 cache is present
1 = L2 cache is not present

Equipment Present Register 2 (Port 0x080E)

This register provides information on hardware options.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0: VME_PRESENT
0 = VME not present
1 = VME present

D1: AUDIO_PRESENT
0 = Business Audio not present
1 = Business Audio present

D2: SFLSH2_PRESENT
0 = No Flash boot ROM
1 = 1 Mbyte Flash boot ROM

D3 to D5: Processor Bus Speed bits
000 = Reserved
001 = Reserved
010 = 66 MHz
011 = Reserved
100 = 75 MHz
101 = Reserved
110 = Reserved
111 = Reserved

D6 and D7: User Flash presence/size bits
00 = No user Flash
01 = 2 Mbyte user Flash
10 = 4 Mbyte user Flash
11 = 8 Mbyte user Flash

L2 Invalidate Register (Port 0x0814)

Writing any value to this register causes the L2 cache tag RAM to be reset. A read of this register has no effect.

Note: Disable the L2 cache before resetting the tag RAM.

Key Lock Register (Port 0x0818)

This register provides information on the state of the keylock signal. See the Keylock section for more details.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D6: Reserved

D7: Keylock
0 = Keylock signal low
1 = Keylock signal high

Board Revision Register (Port 0x0854)

This register provides information on the build state of the PPC2A.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D2: Number revision of hardware build state
1 = Revision 1
2 = Revision 2
3 = Revision 3
All other values are Reserved.

D3 to D7: Letter revision of hardware build state
0x0 = Revision A
0x1 = Revision B
...
0x18 = Revision Y
0x19 = Revision YA
...
0x1F = Revision YG

CIO Port C Data Register (Port 0x0860)

This register allows control of the four front-panel mounted, software programmable LEDs.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D3: Write protect mask for D4 to 7 respectively:
0 = Write enabled
1 = Write protected

D4: DS4, front panel green
0 = LED on
1 = LED off

D5: DS3, front panel yellow
0 = LED on
1 = LED off

D6: DS1, front panel red
0 = LED off
1 = LED on

D7: DS2 front panel yellow
0 = LED on
1 = LED off

See the Software Programmable LEDs section for the location of these LEDs.

Note: DS1 is on by default after power-up.

CIO Port B Data Register (Port 0x0861)

This register controls the DTR modem signals for the COM3 and COM4 serial ports and also the various transmit clocking options when RS422/485 transceivers are fitted.

For a description of how to set up this port for the operation described below, see the CIO Control Register section. Pull-up and pull-down resistors hold these bits to 10001000_B during reset of the CIO until the port is properly configured and enabled.

The data bits of this register are not changed by a reset.

MSB							**LSB**
D0	D1	D2	D3	D4	D5	D6	D7

D0: COM4_DTR (output)
0 = Assert DTR on COM4
1 = Negate DTR on COM4

D1 and D3: COM4_TX_CKSEL and COM4_TX_EN (output)
If RS422/485 transceivers are fitted, these bits configure the ESCC transmit clock options for the COM4 port, and assume that the ESCC has been programmed accordingly.

00 = Not a valid combination (ESCC transmit clock is neither transmitted on TT nor received on ST)
01 = ESCC supplies a transmit clock on TT
10 = ESCC transmit clock is received on ST
11 = ESCC transmit clock is received on ST and retransmitted on TT

If RS232 transceivers are fitted, D1 has no effect and D3 enables or disables the RS232 transceivers as follows:

0 = Disable all transceivers except the CTS receiver
1 = Enable all transceivers

D2: COM4_RX_EN (output)
0 = Disable receivers on RXD, CTS, DCD and DSR for COM4
1 = Enable receivers on RXD, CTS, DCD and DSR for COM4

Note: This bit has no effect if RS232 transceivers are fitted

D4: COM3_DTR (output)
0 = Assert DTR on COM3
1 = Negate DTR on COM3

D5 and D7: COM3_TX_CKSEL, COM3_TX_EN (output)
If RS422/485 transceivers are fitted, these bits configure the ESCC transmit clock options for the COM3 port, and assume that the ESCC has been programmed accordingly.

00 = Not a valid combination (ESCC transmit clock is neither transmitted on TT nor received on ST)
01 = ESCC supplies a transmit clock on TT
10 = ESCC transmit clock is received on ST
11 = ESCC transmit clock is received on ST and retransmitted on TT

If RS232 transceivers are fitted, D5 has no effect and D7 enables or disables the RS232 transceivers, as follows:

0 = Disable all transceivers except the CTS receiver
1 = Enable all transceivers

D6: COM3_RX_EN (output)
0 = Disable receivers on RXD, CTS, DCD and DSR for COM3
1 = Enable receivers on RXD, CTS, DCD and DSR for COM3

Note: This bit has no effect if the RS232 transceivers are fitted.

CIO Port A Data Register (Port 0x0862)

This register controls certain hardware features of the PPC2A.

For a description of how to set up this port for the operation described below, see the CIO Control Register section. Pull-up and pull-down resistors hold these bits to 00111X11B during reset of the CIO until the port is properly configured and enabled.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0: COM4_RX_CKSEL (output)
0 = Disable the RT receiver on the COM4 port.
1 = Enable the RT receiver on the COM4 port.

Note: This bit has no effect if the RS232 transceivers are fitted.

D1: COM3_RX_CKSEL (output)
0 = Disable the RT receiver on the COM3 port.
1 = Enable the RT receiver on the COM3 port.

Note: This bit has no effect if the RS232 transceivers are fitted.

D2: FLASH_VPP (output)
0 = Enable the +12V generator for Flash programming.
1 = Disable the +12V generator for Flash programming.

Note: It takes approximately 400µs for the +12V to stabilise after it is enabled. The generator only supplies enough current to program one Flash (System, User 0 or User 1) at a time.

D3: FLSH_RDY1 (input)
0 = User Flash 1 is busy doing a write/erase operation.
1 = User Flash 1 is ready.

D4: FLSH_RDY0 (input)
0 = User Flash 0 is busy doing a write/erase operation.
1 = User Flash 0 is ready.

D5: WATCHDOG
If this bit is configured as an input, the watchdog is disabled.
If this bit is configured as an output, writing to it (the value is not significant) triggers the watchdog timer. Once triggered, the timer must be retriggered at least once every 1.5 seconds, or a hard reset of the entire PPC2A occurs. Disabling the watchdog after triggering it clears the watchdog, and no reset is generated.

D6: COM4_DSR (input)
0 = DSR on the COM4 port is asserted.
1 = DSR on the COM4 port is negated.

D7: COM3_DSR (input)
0 = DSR on the COM3 port is asserted.
1 = DSR on the COM3 port is negated.

CIO Control Register (Port 0x0863)

This register is used to control the CIO ports. See the CIO datasheet for a full description of the control registers.

A reset of the CIO sets up ports A, B and C as follows:

- Disabled - external pins are tri-stated
- Non latching inputs
- Active high, TTL level outputs
- All bits configured as outputs
- No handshaking (simple parallel port)

Each port must be properly configured and set to its initial value before it can be enabled for use. The initial values are as follows:

Port A = 0x3B (non-latching inputs, active high TTL outputs, D0 to D2 outputs, D3 to D7 inputs).

Port B = 0x88 (non-latching inputs, active high TTL outputs, D0 to D7 outputs).

Port C = 0x02 (non-latching inputs, active high TTL outputs, D4 to D7 outputs).

ID Link Register (Port 0x0864)

This register allows you to read the Board ID links (E3, E4, E5 and E9), the state of the test connector signals BITEMON~ and INTER~, and the L2 cache type.

MSB							**LSB**
D0	D1	D2	D3	D4	D5	D6	D7

D0: L2_PIPE/BURST
0 = Flow through (burst) L2 cache fitted.
1 = Pipelined L2 cache fitted.

D1: Reserved

D2: INTER~ state (connected to J3 pin 8 for use during factory test).

D3: BITEMON~ state (connected to J3 pin 4 for use during factory test).

D4: E9
0 = Link fitted
1 = Link not fitted

D5: E4
0 = Link fitted
1 = Link not fitted

D6: E3
0 = Link fitted
1 = Link not fitted

D7: E5
0 = Link fitted
1 = Link not fitted

Memory Type Motherboard Register (Port 0x0866)

This register provides information on the type of DRAM fitted on the PPC2A. It should be used in conjunction with the DRAM Memory Bank Size and DRAM Memory Bank Fitted registers.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 and 1: DRAM Speed
00 = Reserved
01 = Reserved
10 = 60ns DRAM
11 = 70ns DRAM

D2: ECC_TYPE
0 = ECC
1 = Parity

D3: ECC
0 = ECC not fitted
1 = ECC fitted

D4: REFRESH_MODE
0 = Asymmetrical
1 = Symmetrical

D5: DRAM_TYPE
0 = Normal DRAM
1 = EDO DRAM

D6: Hardware ID
This bit is set to 1 for PPC2A

D7: Hardware ID
This bit is set to 0 for PPC2A

Memory Type Mezzanine Register (Port 0x0868)

This register provides information on the type of DRAM fitted on the PMCC2 (if used).

MSB							**LSB**
D0	D1	D2	D3	D4	D5	D6	D7

D0 and 1: DRAM Speed
00 = Reserved
01 = Reserved
10 = 60ns DRAM
11 = 70ns DRAM

D2: ECC_TYPE
0 = ECC
1 = Parity

D3: ECC
0 = ECC not fitted
1 = ECC fitted

D4: REFRESH_MODE
0 = Asymmetrical
1 = Symmetrical

D5: DRAM_TYPE
0 = Normal DRAM
1 = EDO DRAM

D6: Reserved

D7: Reserved

ESCC

COM3 Control Register (Port 0x842) and COM4 Control Register (Port 0x840)

A read of these registers accesses the Status register (RR0) and a write accesses the Command register (WR0). On reset, the Status register is set to x1xxx100B and the Command register is set to 0x00.

The Command register (WR0) provides indirect access to all registers in the ESCC by a pointer-plus-value mechanism. To use this, first write the address of the register to access into the Control register, then carry out a second read or write to access the addressed register. This second access also clears the address bits, restoring default access to WR0/RR0. If you ever lose track of where you are in this sequence, you can safely read the Control Register, which clears the address bits without any unwanted side effects.

For a full description of the ESCC registers and how to program them, see the ESCC User's Manual from Zilog.

Note: There is only one set of address bits, which are shared between COM3 and COM4.

Command Register (WR0)

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 and D1: 00 = Null code
01 = Reset Rx CRC checker
10 = Reset Tx CRC generator
11 = Reset Tx underrun/EOM latch

D2 to D4: 000 = Null code
001 = Point high
010 = Reset external/status interrupts
011 = Send abort
100 = Enable interrupt on next Rx character
101 = Reset Tx interrupt pending
110 = Error reset
111 = Reset highest IUS

D5 to D7: Address of register to access (WR0 to WR7 for writes, RR0 to RR7 for reads). If D2 to D4 = 001 (point high), then D5 to D7 address the upper registers (WR8 to WR15 for writes, RR8 to RR15 for reads).

Status Register (RR0)

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0: Break/abort

D1: Tx underrun/EOM

D2: CTS

D3: Synch/hunt

D4: DCD

D5: Tx buffer empty

D6: Zero count

D7: Rx character available

COM3 Data Register (Port 0x843) and COM4 Data Register (Port 0x841)

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

These registers provide direct access to the read and write FIFOs of COM3 and COM4, bypassing the two-stage pointer-plus-value mechanism of the Control registers. Any pointer value already set up in the Control registers is unaffected by accesses to these registers. A read of the register accesses the read FIFO (RR8), and a write accesses the write FIFO (WR8). The data bits of these registers are not changed by a reset.

Interrupts and Error Reporting

The various external interrupt sources to the processor and their relative priorities are shown in the table below. The table also shows whether the previous state of the processor is recoverable.

Priority	Interrupt	Cause	Recoverability
0	System Reset	Power on, Hard reset	Non-recoverable
1	Machine Check	TEA~ input, Address or Data Parity, Machine Check Input (MCP~), Non-maskable Interrupt (NMI~)	Non-recoverable in most cases
2	System Reset	Soft reset	Recoverable unless Machine Check occurs
3	System Management Interrupt	SMI~ input	Recoverable unless Machine Check or System Reset occurs
4	External Interrupt	INT~ input	Recoverable unless Machine Check or System Reset occurs

System Resets

See the Resetting the PPC2A section at the start of this chapter.

Machine Check Exception

The PCI bridge may be configured to assert TEA~ to the processor for a Flash write error or an unsupported local bus cycle. The processor may be configured to take a machine check exception or enter the checkstop state.

The processor address and data parity error inputs (APE~ and DPE~) are not used on the PPC2A. Address and data parity errors are reported via the machine check pin as described below.

The PCI bridge may be configured to assert the machine check input to the processor (MCP~) to signal a non-recoverable error. The processor may be configured to take a machine check exception or enter the checkstop state. Non-recoverable errors are:

- Flash write error
- Unsupported local bus cycle
- PCI PERR or SERR
- Memory read ECC multi-bit error
- Memory select error (address out of range)
- PCI target abort (e.g. VMEbus BERR~) or master abort
- Illegal L2 cache copyback
- L2 cache read parity error
- Refresh overflow error

In addition, the PCI bridge may be programmed to produce a machine check exception after a programmable number of correctable single bit errors.

Status bits in the PCI bridge allow the cause of the exception to be determined.

Links E6 and E7 allow the PPC2A hardware to be configured so that machine checks are signalled as an interrupt on IRQ13 rather than on the processor's MCP~ pin. These links are described in chapter 4.

Hint: If you know that a machine check may occur during a specific operation (e.g. a VMEbus BERR~ during a VMEbus memory sizing operation), it may be possible to ensure that the processor is in a recoverable state after the machine check exception by using the SYNC instruction before and after the instruction that potentially causes machine check.

Non-Maskable Interrupt (NMI~)

The NMI~ output of the ISA bridge is connected to the NMI~ input of the PCI bridge. It is not generally required, as the PCI bridge can be configured to detect SERR on the PCI bus.

System Management Interrupt (SMI~)

The System Management Interrupt pin of the PCI bridge is connected to the SMI~ output from the ISA bridge to support the power management features of the ISA bridge.

External Interrupt (INT~)

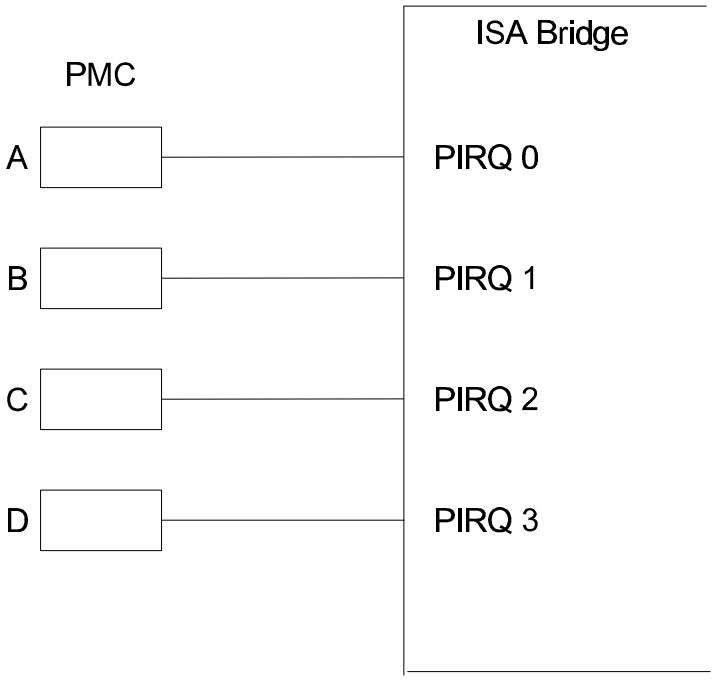
The processor external interrupt pin (INT~) is asserted for a pending interrupt from the interrupt controller in the ISA bridge.

Interrupt priorities and modes are assigned as shown in the table below. These assignments are set up by the standard boot firmware; if you are using alternate boot firmware, it must duplicate these settings. Edge sensitive interrupts are sensitive to the rising edge (except for IRQ8, which is sensitive to the *falling* edge); level sensitive interrupts are active low.

IRQ	Priority	Mode	Source
0	2	Edge	Timer 1 Counter 0 (internal to ISA bridge)
1	3	Edge	Keyboard
2			Cascade for IRQ8 to IRQ15
3	11	Edge	COM2 Serial Port
4	12	Edge	COM1 Serial Port
5	13	Level	CIO
6	14	Edge	Floppy Disk Controller
7	15	Level	Parallel Port
8	4	Edge	Real Time Clock
9	5	Level	Ethernet
10	6	Level	COM4/COM3 Serial Port
11	7	Level	VME
12	8	Edge	Mouse
13	1	Edge	Machine Check Interrupt
14	9	Level	SCSI
15	10	Level	PMC slot

PCI Interrupts

The four PCI interrupt lines (A, B, C and D) from the PMC slot are connected to the PIRQ0~ to PIRQ3~ inputs of the interrupt controller as shown in the following diagram:



PCI Configuration

The boot process must configure the base address and space type (memory or I/O) of all the PCI attached peripherals. The memory requirements of each PCI device are given in the appropriate device descriptions in this chapter.

Each PCI device also has several registers located in PCI configuration space, which is accessed by the processor through the MPC106 PCI bridge and memory controller using the CONFIG_ADDR and CONFIG_DATA registers. A full description of PCI configuration can be found in the PCI and MPC106 specifications.

The device number mapping for the PCI bus attached to the MPC106 follows:

Device Number	Function
0	MPC106 PCI bridge and memory controller
1 to 10	Not implemented
11	82378ZB ISA bridge
12	53C860 SCSI controller
13	79C970 PCnet to PCI
14	Universe VME controller
15	PMC
16 to 30	Not implemented

Keylock

The keylock input signal allows the software to interrogate an external keyswitch. For example, the boot firmware could request a password if the keyswitch is in the locked position and a password is set up in the NOVRAM.

The keylock signal defaults to high if no external connection is made.

Chapter 10 - Troubleshooting

Radstone does not anticipate that you will have any problems with your product. However, in the unlikely event that you do experience problems, for assistance please contact Radstone's Technical Help Line on:

+44 (0)1327 359804

When you phone for technical support, please be prepared to provide:

- Your contact details (name, work address, work telephone and fax numbers, and e-mail address if appropriate)
- A detailed description of the problem
- Any messages and error messages being generated
- What has been tried so far
- The software revision level, hardware platform, hardware revision and operating system level of all other boards that you are using in the system with the product
- If you are reporting a bug, give detailed instructions on how to reproduce the problem and sample code, if possible (if the bug occurs in an application)

Your query will be allocated a unique Call Reference Number (CRN) for use in future correspondence.

If you *are* experiencing a problem with your PPC2A and are awaiting a response from Radstone's technical support, there follow some rudimentary suggestions that you may also like to try to get your PPC2A operational:

- Ensure that the board is firmly seated and secured in the rack and that all male/female connectors mate together correctly
- Check the links on the board and the system backplane
- If you are unsure of which link configuration to use, try the configuration suggested in Chapter 4 initially
- Check that the VME rack has terminators, if these are not built in (the manual for your rack should tell you whether the terminators are built in)
- Check that the power supply is within VME limits on +5V, +12V and -12V with a digital volt meter

CAUTION
Any problems with the power supply should only be dealt with by qualified personnel.

- Check that there is only one board configured as system controller in a system and that this is in slot 1 of the rack
- Check that there are no vacant slots in the rack without jumpers (or that an automatic daisy chaining backplane is being used)
- **Take extra care if you are using the PMCC2, as this occupies an extra system slot, but requires the daisy chains to be linked across the slot**
- Prove the PPC2A's operation in isolation before adding it into a multi-board system
- If you are using the SCSI bus, then check that the cable stub length is less than 10 cm. You are also recommended to locate the PPC2A at one end and enable the bus terminator by fitting link E12. If you want to use the PPC2A somewhere other than at the end of the SCSI bus, ensure that E12 is not fitted. **Fitting E12 when the PPC2A is not located at the end of a SCSI bus may cause erroneous SCSI operation.**
- The power supply to the RTC on the PPC2A is fed from the VSTANDBY pin on the VMEbus. VMEbus compliance requires this voltage to be 5V ± 5%. Fitting link E11 allows you to supply a voltage of 3V from a battery to this pin to maintain normal RTC operation. **Fitting E11 when VSTANDBY is connected to +5V may cause damage to the RTC**
- If you have made your own cable for connection between J3 and a terminal, check that the pinout is correct
- Check that the terminal is set up for DTE (9.6 kbaud, 8 bits/character, 1 stop bit, parity disabled)
- Ensure that air-cooled PPC2As receive sufficient air-flow. If you need to operate your PPC2A on an extender card, this requires an additional fan to supply the necessary air flow
- Ensure that conduction cooled PPC2As are fully installed in the conduction cooled box and that the wedgelocks are correctly tightened. If, for any reason, you need to operate the conduction cooled PPC2A on an extender card, you must maintain an airflow of 300 feet/minute over it.

Appendix A - Specifications

This appendix gives a specification of the PPC2A. It also covers items such as the power requirements, the MTBF, the general measurements etc. and lists the available options.

VMEbus Compliance

The PPC2A conforms to the ANSI/VITA 1-1994 standard for VME64.

Master:	A16, A24 and A32 ADO, ADOH A16:LCK, A24:LCK, A32:LCK D08(EO), D08(EO):RMW, D08(EO):BLT D16, D16:RMW, D16:BLT D32, D32:RMW, D32:BLT, D32:UAT D64:MBLT
Slave:	A16, A24 and A32 ADO, ADOH A16:LCK, A24:LCK, A32:LCK D08(EO), D08(EO):RMW, D08(EO):BLT D16, D16:RMW, D16:BLT D32, D32:RMW, D32:BLT, D32:UAT D64:MBLT
Interrupt Handler:	D08(O), IH(1-7)
Interrupter:	I(1-7)
VMEbus Arbiter:	SGL, RRS, PRI, BCLR~ generation
VMEbus Requester:	ROR, RWD Early BBSY~ release Bus capture and hold
Bus Time-out Module:	16, 32, 64, 128, 256, 512, 1024 µS, disabled
Other Slot 1 Functions:	Slot 1 detector, IACK~ daisy chain driver, SYSCLK Driver
Auto Slot ID:	VME64 specified and SCV64 compatible modes

Local Resources

Processor	PowerPC 603e, PowerPC 604e or PowerPC 740, at speeds up to 300 MHz
DRAM	32 or 64 Mbytes with ECC on-board. Further expansion up to 256 Mbytes via PMCC2.
L2 Cache	1 Mbyte
Flash boot	1 Mbyte in byte wide, on board programmable Flash ROM.
User Flash	8 Mbytes of word-wide on-board programmable FlashFile program ROM
RTC	DS1285 RTC backed up by connection to VMEbus 5VSTDBY pin
NOVRAM	8 Kbyte SRAM device with shadow 8 Kbyte EEPROM providing automatic recall on power-up and software controlled store and recall cycles
PCI	32-bit
SCSI	8-bit ultra-fast SCSI via the P2 connector
Ethernet	Ethernet or IEEE 802.3 (10Base5 or 10BaseT) via P2 connector
PMC Slot	Air Cooled: 5V, 32-bit IEEE P1386.1 compliant slot with front panel or P0 I/O. Two 5V, 32-bit slots with front panel, P2 or P0 I/O on PMCC2
	Conduction Cooled: 5V, 32-bit rugged PMC compliant slot with P0 I/O and limited front panel I/O. Two 5V, 32-bit slots with limited front panel, P2 or P0 I/O on PMCC2
Serial I/O	Two PC-style COM ports via the P2 connector and a front panel mounted 15-way micro-D connector. Two further COM ports via P2 connector, configurable at build time as RS232 asynchronous or RS422 synchronous or asynchronous interfaces.
Keyboard and Mouse	PS/2 compatible Keyboard and Mouse interface via the P2 connector
Parallel I/O	Centronics style port via P2 connector
Floppy Disk Interface	MFM 1.44/2.88 Mbyte. On-board 34-way header
Counter/ Timers	Three independent 16-bit counter/timers with a resolution of 333ns. Two timers may be linked to form a 32-bit counter/timer
Front Panel I/O	P3 connector for COM1 and COM2 accessible on all build levels.
	PMC I/O for Levels 1 to 3.
	Level 4 has limited front panel I/O for PMCs with the appropriate layout, and connector size and location (e.g. PMC2-9100).
Status LEDs	4 software programmable LEDs (DS1 is red, DS2 and DS3 are yellow, and DS4 is green) front panel mounted. 3 Ethernet status LEDs (DS101 to DS103) on the back of the board behind the front panel. 1 SCSI Activity LED (DS104) on the back of the board behind the front panel.

Operating Systems	VxWorks/Tornado LynxOS RTEMS OS-9 Spectra/VRTX	
PCI Carrier	Compliance Occupies slots Provides slots I/O	PMC 1 VME Slot 2 PMC Slots Front panel, P0 or P2.
PCI Graphics	Compliance Graphics processor VRAM I/O Miscellaneous	PMC Weitek P9100 4 Mbytes Front panel VGA connector Shared frame buffer interface
I/O Modules	P2 (3U mounting)	SCSI Two serial Parallel, Mouse and keyboard Ethernet/10Base5/10BaseT 10Base2
	Miscellaneous	P2 transition module (including 50-way SCSI header)

Power Requirements

	PPC2A-603e 32 Mbyte DRAM	PPC2A-740 32 Mbyte DRAM	PPC2A-604e 64 Mbyte DRAM
+5V +5%, -2.5%	5A	5A	7A
+12V +5%, -2.5%	500 mA	500 mA	500 mA
-12V +5%, -2.5%	0 mA	0 mA	0 mA

Note: Take care when using PMC modules as to how much current they require, especially from the +5V supply. The VME specification allows a maximum of 7.5A to be drawn from the +5V supply in a single slot over the PPC2A's specified operating temperature range. It may not be possible to support all combinations of L2 cache, DRAM and PMC modules within this limit.

EMC Regulatory Compliance and Safety

Air-cooled versions of PPC2A are designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

Conduction cooled versions are designed for integration into EMC hardened cabinets/boxes.

All PCBs are manufactured by UL approved manufacturers and have a flammability rating of 94V-0.

Mean Time Between Failures

The calculated MTBFs for the PPC2A, for several example configurations, are shown in the table below. These failure rates are based only on the components and connectors fitted to the board at delivery and take no account of user fitted PMC modules. The failure rates used in this calculation are based on MIL-HDBK-217F Notice 1 with commercial or non-military quality level and Ground Benign environment (at 25°C). Where a component did not comply with the MIL-HDBK, the closest equivalent, compliant component was used.

Processor	Configuration	MTBF (Hours)
PPC2A-604e	32 Mbyte DRAM, 256 Kbyte L2 cache	30,000
PPC2A-604e	64 Mbyte DRAM, 256 Kbyte L2 cache	28,166

Environmental Specifications

Convection-cooled Boards

Build Style	Operating Temp (°C)	Storage Temp (°C)	Vibration	Shock	Humidity	Comments
Standard (Level 1)	0 to +55 with airflow of 300 feet/minute	-50 to +100	$0.002g^2$/Hz from 10 to 2000 Hz random, and 2g sinusoidal from 5 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH	Commercial grade cooled by forced air, for use in benign environments and software development applications.
Extended Temp (Level 2)	-20 to +65 with airflow of 300 feet/minute	-50 to +100	$0.002g^2$/Hz from 10 to 2000 Hz random, and 2g sinusoidal from 5 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	As Standard but conformally coated and temperature characterised.
Rugged Air Cooled (Level 3)	-40 to +75 with airflow of 600 feet/minute	-50 to +100	$0.04g^2$/Hz from 10 to 2000 Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	Wide temperature rugged, cooled by forced air. Conformally coated for additional protection.

Conduction-cooled Board

Build Style	Operating Temp (°C)	Storage Temp (°C)	Vibration	Shock	Humidity	Comments
Rugged Conduction Cooled (Level 4)	-40 to +75 at the thermal interface	-50 to +100	Random $0.1g^2$/Hz from 5 to 2000 Hz per MIL-STD-810E	40g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.

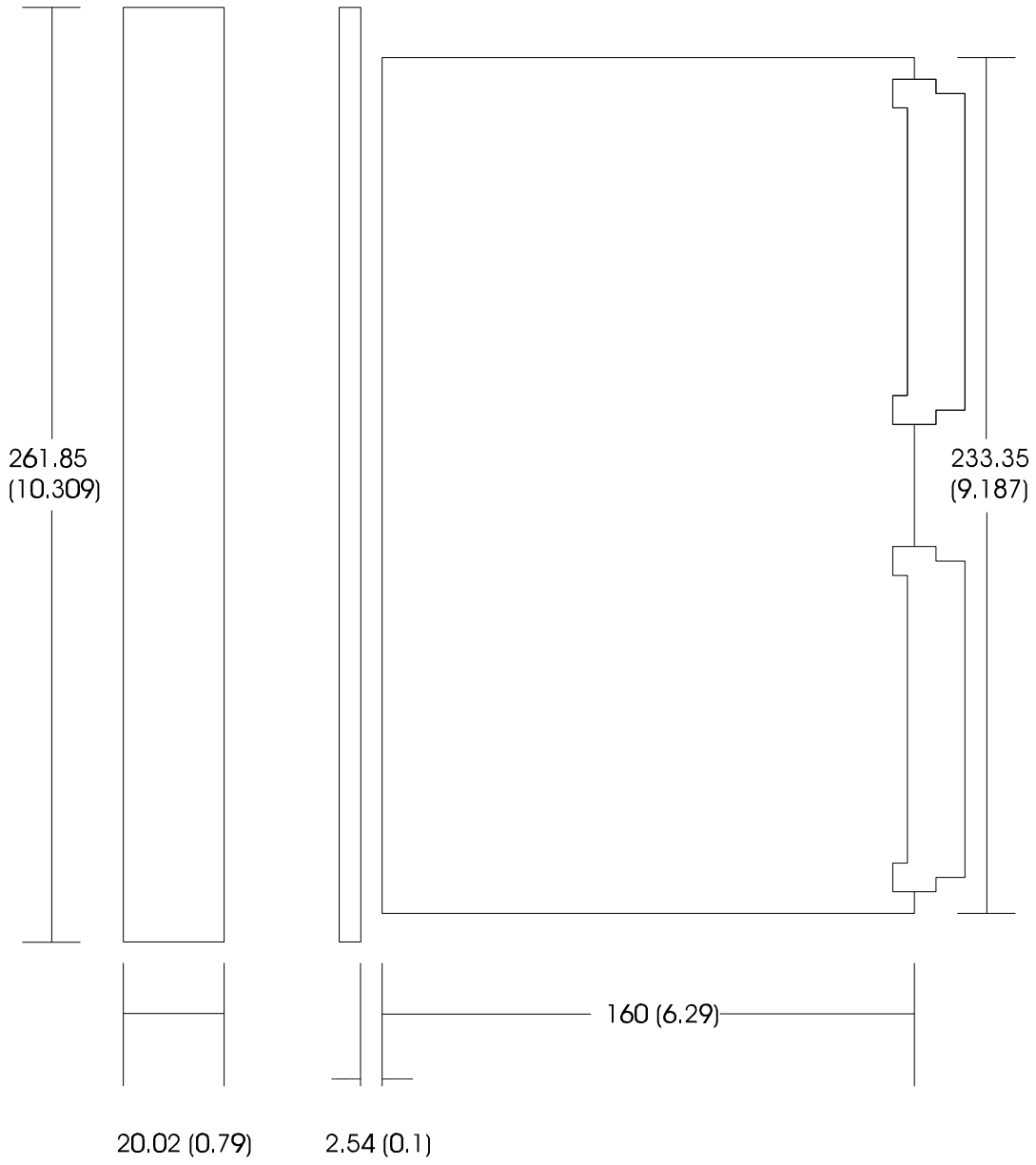
Mechanical Construction

Weight

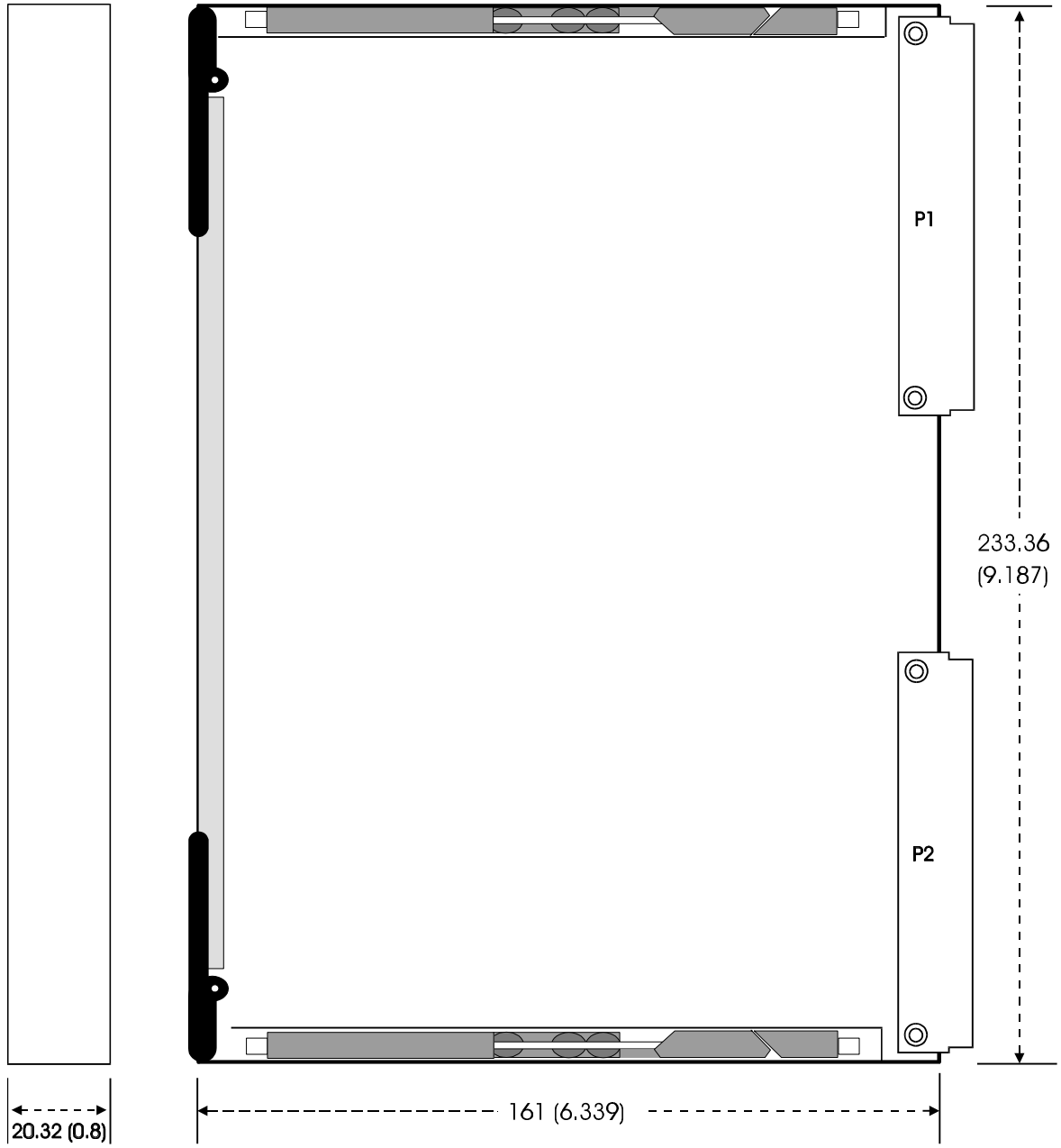
The approximate weight of the PPC2A is 710g. As most of this is due to the heatsink, the weight is more or less the same for all four styles.

Dimensions

The air-cooled PPC2A is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA 1-1994 specification. The dimensions shown below are in millimetres, with inches (in parentheses) for general guidance only.



The Conduction cooled PPC2A is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the IEEE 1101.2. The dimensions shown below are in millimetres, with inches (in parentheses) for general guidance only.



Ordering Information

The order code is specified as **PPC2A-603-vwxyz**, **PPC2A-604-vwxyz** or **PPC2A-740-vwxyz**, where **vwxyz** are explained in the following table:

v (Build Level)	w (Processor and Frequency)		x (DRAM)		y (L2 Cache and User Flash)			z (Ethernet and COM3/COM4 Configuration)		
1	2	603e @ 200 MHz	2	32 Mbytes	0	None	None	A	10Base5	RS422
2	4	603e @ 300 MHz	3	64 Mbytes	6	1 Mbyte	8 Mbytes	B	10BaseT	RS422
3	7	604e @ 200 MHz						C	10Base5	RS232
4	B	740 @ 266 MHz						D	10BaseT	RS232

Not all possible build variants are offered as standard production items. Standard production build variants are:

Code	Meaning
PPC2A-603-1236A	Level 1, 200 MHz PowerPC 603e, 64 Mbytes DRAM, 1 Mbyte L2 cache, 8 Mbytes User Flash, 10Base5 Ethernet, 2 x RS422 ports, no P0 connector
PPC2A-603-2236A	Level 2 build standard, otherwise as above
PPC2A-603-3236A	Level 3 build standard, otherwise as above
PPC2A-603-4236A	Level 4 build standard, Type A 80-way P0 connector fitted as standard, otherwise as above
PPC2A-603-1436A	Level 1, 300 MHz PowerPC 603e, 64 Mbytes DRAM, 1 Mbyte L2 cache, 8 Mbytes User Flash, 10Base5 Ethernet, 2 x RS422 ports, no P0 connector
PPC2A-603-2436A	Level 2 build standard, otherwise as above
PPC2A-603-3436A	Level 3 build standard, otherwise as above
PPC2A-603-4436A	Level 4 build standard, Type A 80-way P0 connector fitted as standard, otherwise as above
PPC2A-604-1736A	Level 1, 200 MHz PowerPC 604e, 64 Mbytes DRAM, 1 Mbyte L2 cache, 8 Mbytes User Flash, 10Base5 Ethernet, 2 x RS422 ports, no P0 connector
PPC2A-604-2736A	Level 2 build standard, otherwise as above
PPC2A-604-3736A	Level 3 build standard, otherwise as above
PPC2A-604-4736A	Level 4 build standard, Type A 80-way P0 connector fitted as standard, otherwise as above
PPC2A-740-1B36A	Level 1, 266 MHz PowerPC 740, 64 Mbytes DRAM, 1 Mbyte L2 cache, 8 Mbytes User Flash, 10Base5 Ethernet, 2 x RS422 ports, no P0 connector
PPC2A-740-2B36A	Level 2 build standard, otherwise as above
PPC2A-740-3B36A	Level 3 build standard, otherwise as above
PPC2A-740-4B36A	Level 4 build standard, Type A 80-way P0 connector fitted as standard, otherwise as above

All other items (such as 1 Mbyte System Flash, Ultra SCSI-2 interface, Mouse and PS/2 Keyboard interface, Floppy interface, Parallel interface, 2 x RS232 ports, 1 PMC slot, 5-row P1 and P2 connectors) are standard.

Other Build Options

Other permissible variants, apart from the standard ones listed previously, are as follows:

Code	Meaning	Standard
PPC2A-60*n*-vwxy**B**	10BaseT Ethernet	10Base5 Ethernet
PPC2A-60*n*-vwxy**C**	COM3/COM4 configured as RS232	COM3/COM4 configured as RS422
PPC2A-60*n*-vwxy**D**	10BaseT Ethernet *and* COM3/COM4 configured as RS232	10Base5 Ethernet *and* COM3/COM4 configured as RS422

Other options, which should be specified *in addition to* the order code, are as follows:

Code	Meaning
POPPPC2A-35	Type A 80-way P0 connector fitted to PPC2A Level 1, 2 or 3 build standard. This must be specified when the PPC2A is ordered
POPPPC2A-36	Type B 95-way P0 connector fitted to PPC2A Level 1, 2 or 3 build standard. This must be specified when the PPC2A is ordered
POPPPC2A-65	No P0 connector fitted to PPC2A Level 4 build standard. This must be specified when the Level 4 PPC2A is ordered

P3 Adapter Cable

The P3 adapter cable, ordered as PPC2CABL-4015a, is a 0.5m long, handy adapter cable with a 15-way micro D-type for connection to J3 fitted at one end, and the other end left unspecified for the user to fit their own connector.

PMCC2 Options

The PMCC2 provides two PMC slots and expansion DRAM. It is always supplied with a full mounting kit and instructions for fitting onto the PPC2A board.

The order code is specified as **PMCC2-xyz**, where **xyz** are explained in the following table:

x **(Build Level)**	**y** **(DRAM fitted)**	**z**
1	000 = No DRAM fitted	A = No P0 connector
2	064 = 64 Mbytes	B = P0 connector
3	192 = 192 Mbytes	
4		

The '**A**' version has 5-row P1 and P2 connectors, with no P0 connector fitted. PMC1 has 45 pins to rows Z and D of P2, and PMC2 has 64 pins to rows A and C of P2. On Level 1 to Level 3 build standards, I/O is via the front panel or P2. On Level 4, I/O is through P2 only.

The '**B**' version has 5-row P1 and P2 connectors, and a 5-row Type A P0 connector. PMC1 is routed to P0, and PMC2 is routed to P2 (64 pins each). On Level 1 to Level 3 build standards, I/O is via the front panel or P2 and P0. On Level 4, I/O is through P2 and P0 only.

PMC Modules

A range of PMCs is available both from Radstone and third parties. PMCs available from Radstone, in various build standards including Radstone's state-of-the-art rugged conduction-cooled PMCs, include:

- PMC2-9100 Graphics, Levels 1 to 4. Front panel/rear I/O, 4 Mbytes VRAM and analogue or digital video output options
- PMC9100 Graphics, Level 1 only. 4 Mbytes VRAM
- PMCFSAS/FDAS FDDI interface, Level 1 only. Single or Dual Attach options
- PMC1553 MIL-STD-1553B interface, Levels 1 to 4. Front panel or rear I/O, single or dual channel, and RT-only or RT/BC/MT options
- PMCEXT 100BaseTX Fast Ethernet interface, Level 1 only
- PMC-ATMF 155 Mbit ATM interface, Levels 1 to 4.

These products are backed-up by data sheets and manuals giving more information, and more details on the options. For more detail on any of these or forthcoming products, or for copies of the literature, please contact Radstone directly or your nearest Sales Office.

Note: Level 1 PMCs (both from Radstone and third parties) can be used on all air-cooled versions (Levels 1, 2 and 3) of the PPC2A, even if the PMC does not meet the extended temperature and environmental requirements of Levels 2 and 3. However, conduction cooled variants of the PPC2A can only accept conduction cooled PMCs.

Operating Systems

Availability includes:

- VxWorks/Tornado
- LynxOS
- RTEMS
- OS-9
- Spectra/VXRTSA

Please contact Radstone for more details.

P2 I/O Modules (3U)

Code	Meaning
P25X600-S	P2 transition module with 5-row VME connector. Provides headers for Ethernet, SCSI, COM1, COM2, COM3 and COM4 serial ports, parallel port and mouse/keyboard port. For use with PPC2A, but compatible with PPC1a for 3-row VME I/O
P25X600-X	Level 2 build standard, otherwise as above
SIOX600-S	Serial I/O panel with two 9-way D-type connectors and 0.5m internal ribbon cable
SIO2X600-S	Serial I/O panel with two 25-way D-type connectors and 0.5m internal ribbon cable. May be used with all four COM ports when RS232 is specified. Two units are required to access all 4 ports
SIO3X600-S	Serial I/O panel with one 25-way D-type connector and 0.5m internal ribbon cable. Complies with RS530 pinout and signal set. May be used with COM3 and COM4 ports when RS422 is specified. Two units are required to access both ports
PMKX600-S	Panel for parallel and mouse/keyboard ports with 0.5m internal ribbon cable
SCSIX600-S	Honda SCSI panel with 0.5m internal ribbon cable
CENTX600-S	Centronics SCSI panel (double width) with 0.5m internal ribbon cable
10B2X600-S	Cheapernet/10Base2 panel and module with 0.5m internal ribbon cable
10B5X600-S	10Base5 panel with 0.5m internal ribbon cable
ETHX600-S	Ethernet panel with 0.5m internal drop cable

Glossary

Note: The VMEbus signals are explained in chapter 5

A16
Providing or decoding addresses on VMEbus address lines A01 to A15.

A24
Providing or decoding addresses on VMEbus address lines A01 to A23.

A32
Providing or decoding addresses on VMEbus address lines A01 to A31.

A64
Providing or decoding addresses on VMEbus address lines A01 to A31.

AC
Alternating Current.

ADO
ADdress Only cycle on the VMEbus.

ADOH
ADdress Only Handshake cycle on the **VMEbus**.

AMD
Advanced Micro Devices. A chip manufacturer.

ANSI
American National Standards Institute.

Arbiter
An arbiter accepts requests and grants control to one requester at a time.

ARPA
The US Defence Advanced Research Projects Agency.

ASCII
American Standard Code for Information Interchange. A 7-bit code, established by ANSI, to achieve compatibility between data services. Equivalent to the international ISO 7-bit code.

ATM
Asynchronous Transfer Mode.

AUI

Attachment Unit Interface. The cable that connects the DTE to the **MAU**. Also called the **Drop Cable**.

Backplane (VMEbus)

A **PCB** with 96-pin connectors and signal paths that bus the connected pins. Some systems have a single PCB, called the J1 backplane. This provides the signal paths needed for basic operation. Other systems also have a second PCB, called the J2 backplane. This provides the additional 96-pin connectors and signal paths needed for wider data and address transfers. The J1 and J2 sections may be combined into a single J1/J2 backplane PCB.

Bandwidth

The bandwidth is the amount of a resource that is available (or the amount that is used). For a network or bus, the bandwidth is the maximum amount of data that could be transferred in 1 second.

BBSY

Bus Busy.

BCLR

Bus Clear.

BERR

Bus ERRor.

Big-endian

Refers to the way in which multi-byte data is stored in memory. Big-endian data is stored with the most significant byte at the lowest address (68XXX style). See also **Little-endian**.

BIOS

The Basic **I/O** System featured in most **PC**s.

BIT

Built In Test.

BLT

BLock Transfer.

BSP

Board Support Package.

BTO

The **VMEbus** Bus Time Out period. See **Timeout**.

Byte
An 8-bit data structure.

C^4
Control, Command, Configuration and Communications.

Cache
A small, fast access memory between the processor and the larger, slower main memory. Used to store the most recently used instructions/data to improve overall memory access time.

Chassis
See **enclosure**.

Chassis Ground
Most applications require the chassis to be connected to earth, normally via a mains cable or separate earthing strap.

CIO
Counter/timer and parallel I/O. The 85C36 device on the **PPC60x** is a CIO.

CMC
Common Mezzanine Card.

CN
Connector.

CODEC
Coder-Decoder.

COTS
Commercial Off-The-Shelf.

Coupling
A write cycle on the PCI bus can be 'locked' together with a write cycle on the VMEbus, so that the PCI bus cycle cannot continue until the VMEbus cycle has completed. This 'locking' is called coupling. The alternative is **write posting**.

CPU
Central Processing Unit.

CR/CSR
Configuration ROM/Control and Status Register.

CRC
Cyclic Redundancy Check.

CSMA/CD

Carrier Sense, Multiple Access with Collision Detect. The three basic steps for accessing **Ethernet**.

CTS

Clear To Send. A serial signal. See **RTS**.

D64

Sending and receiving data 64 bits at a time over D00 to D31 on the **VMEbus**.

D32

Sending and receiving data 32 bits at a time over D00 to D31 on the **VMEbus**.

D16

Sending and receiving data 16 bits at a time over D00 to D15 on the **VMEbus**.

D08(EO)

Sending and receiving data 8 bits at a time over D00 to D07 or D08 to D15 on the **VMEbus**.

D08(O)

Sending and receiving Status/**ID** 8 bits at a time over D00 to D07 on the **VMEbus**.

Daisy Chain

A signal line that propagates a signal from board to board (or chip to chip), starting with the first slot and ending at the last slot. There are 4 **VMEbus** grant daisy chains and one VMEbus interrupt acknowledge daisy chain.

DC

Direct Current.

DCD

Data Carrier Detect. A serial signal.

DEC

Digital Equipment Corporation. An **OEM**.

DIN

Deutsches Industrie Norm. A German standard.

DMA

Direct Memory Access. A direct, rapid link between a peripheral and main memory that avoids the use of the processor to transfer each item of data.

Double-word

A 64-bit structure.

DPLL
Digital Phase Locked Loop.

DRAM
Dynamic **RAM**. Memory that must be refreshed periodically to maintain the storage of information.

Drop Cable
The cable that connects the **DTE** to the **MAU**. See **AUI**.

DSR
Data Set Ready. A serial signal.

DTE
Data Terminal Equipment. The data terminal devices themselves. A category that includes the computer.

DTR
Data Terminal Ready. A serial signal.

D-type
A connector that has the approximate shape of a capital letter `D'.

E^2PROM (or EEPROM)
Electrically Erasable **PROM**. PROM whose contents can be erased electrically, so allowing the device to be re-used with new data.

ECC
Error Correction Coding.

ECP
Enhanced Capabilities Port.

EDO
Extended Data Out. EDO DRAM is similar to normal DRAM except that the data remains on the output pins longer, so giving the accessing device longer to read it.

EMC
Electro-Magnetic Compatibility.

EN
European Norm.

Enclosure

A rigid framework that provides mechanical support for boards inserted into the **backplane**, ensuring that the connectors mate properly and that adjacent boards do not touch each other. It also guides the cooling airflow through the system and ensures that inserted boards do not disengage themselves from the backplane due to vibration or shock.

EOM

End Of Message.

EPLD

Electrically Programmable Logic Device.

EPP

Enhanced Parallel Port.

EPROM

Erasable **PROM**. PROM whose contents can be erased through exposure to ultra-violet light, so allowing the device to be re-used with new data.

ESCC

Enhanced Serial Communications Controller.

ESD

Electrostatic Sensitive Device.

ESS

Environmental Stress Screening.

Ethernet

Ethernet is a baseband, thick-wire network based on an access method called **CSMA/CD**. It was originally developed by the Xerox Corporation in 1972.

FCC

Federal Communications Commission.

FDC

Floppy Disk Controller.

FDDI

Fiber Distributed Data Interface. A standard for fiber optic cable data transmission.

FIFO

First In First Out. A data queuing mechanism (or the implementation of it) in which the first item stored is the first item processed.

Flash Memory
A type of high-capacity **E^{2}PROM**.

FPU
Floating Point Unit.

FTP
File Transfer Protocol. See **TCP/IP**.

GND
The Ground (0V) signal or supply rail.

Half-word
In PowerPC terminology, a 16-bit structure. Cf **word, longword**.

Handler
See **Interrupt Handler.**

HDLC
High-level Data Link Control. A link-level protocol standard from **ISO**.

I(x-y)
The **interrupter** can generate interrupt requests on **VMEbus** lines IRQx~ to IRQy~.

IACK
Interrupt Acknowledge.

IBM
International Business Machines. An **OEM**.

ID
Identification.

IDE
Integrated Drive Electronics.

IEEE
Institute of Electrical and Electronic Engineers.

IH(x-y)
The **interrupt handler** can generate interrupt acknowledge cycles in response to interrupt requests on **VMEbus** lines IRQx~ to IRQy~.

Interrupter
An interrupter generates an interrupt request on the **VMEbus** and then provides status/**ID** information when requested by the **interrupt handler**.

Interrupt Handler

An interrupt handler detects interrupt requests on the **VMEbus**, generated by **interrupter**s. It acknowledges these requests with an IACK~ and responds to them by requesting Status/**ID** information.

I/O

Input/Output.

IRQ

Interrupt Request.

ISA

Industry Standard Architecture.

ISDN

Integrated Services Digital Network.

ISO

International Standards Organisation.

IUS

Interrupt Under Service.

JEDEC

Joint Electronic Devices Engineering Committee.

JTAG

Joint Test Action Group. A standard for board-level testing.

KBD

Keyboard.

L2 Cache

Second-level **cache**.

LCK

Lock.

LED

Light Emitting Diode. A semiconductor diode that radiates light. LEDs that emit in the visible region are used as indicators or warnings.

Little-endian

Refers to the way in which multi-byte data is stored in memory. Little-endian data is stored with the least significant byte at the lowest address. See also **Big-endian**.

Longword

A 32-bit data structure in **VME** systems. Cf **word, halfword**.

LSB

Least Significant Bit.

Master

A **VMEbus** master initiates bus cycles to transfer data between itself and a **slave** module.

MAU

Medium Access Unit or Media Attachment Unit. The transceiver unit which interfaces with the network medium.

MBLT

Multiplexed BLock Transfer.

Mezzanine

The American term for a daughter board.

MFM

Modified Frequency Modulation. A technique used by hard disk manufacturers.

MIDI

Musical Instrument Digital Interface.

MMU

Memory Management Unit.

MSB

Most Significant Bit.

MTBF

Mean Time Between Failures.

NC

No Connection or Not Connected.

NDI

Non-Developmental Item.

NFS

Network File Server.

Nibble

4 bits. So called because it's half a byte (honestly!).

NMI
Non-Maskable Interrupt.

NOVRAM
Non-Volatile **RAM**. Memory that does not lose its information when powered down.

Null Modem (Cable)
An RS232 cable that has pins 2 and 3 reversed so that the two connected computers are under the impression that they are linked using modems.

OAR
On-line Applications Research Corporation. The creators of **RTEMS**.

OEM
Original Equipment Manufacturer.

OS
Operating System.

PC
Personal Computer.

PCB
Printed Circuit Board.

PCC
PMC Carrier Card.

PCI
Peripheral Component Interconnect.

PCMCIA
PC Memory Card Interface Adapter (also People Can't Memorise Computer Industry Acronyms).

PLCC
Plastic Leadless Chip Carrier.

PLD
Programmable Logic Device.

PMC
PCI Mezzanine Card.

PMCC2
Radstone's **PMC** and Memory Carrier Card.

PMC9100
Radstone's high-performance graphics PMC.

POR
Power On Reset.

POSIX
Portable Operating System Environment. An **IEEE** standard.

PPC2A
Radstone's PowerPC-based processor card. The PPC2A-603e is based on the PowerPC 603e processor, the PPC2A-604e is based on the higher-specified PowerPC 604e processor and the PPC2A-740 is based on the PowerPC 740 processor, otherwise they are functionally equivalent.

Pre-emptive
A multi-tasking mechanism whereby tasks are (re)scheduled at regular intervals based on priority and external events, rather than the task being able to run to completion or some defined suspension point before the next task is scheduled (which is called co-operative). The unit of time between rescheduling is a fixed interval called a time slice.

PReP
PowerPC Reference Platform. An example implementation of a philosophy designed to allow 100% binary compatibility across different platforms, when based on the PowerPC processor.

PRI
Prioritised. A **VMEbus** **arbiter** that prioritises the four VMEbus request lines from BR0~ (the lowest) to BR3~ (the highest) and responds with BG0IN~ to BG3IN~. It also informs the VMEbus **master** when there is a higher level request than that being processed, by driving BCLR~ low.

PROM
Programmable **ROM**. A program in a PROM is electronically `hard-wired', and once the program is inserted into the PROM, it cannot be altered without using a new PROM.

PS/2
Programming System 2 from **IBM**.

RAM
Random Access Memory. Memory that can be read from or written to at any time.

RAS
Row Address Select.

Requester
A **VMEbus** requester requests use of the VMEbus when it is required by a **master**.

RH

Relative Humidity.

RI

Ring Indicator. A serial signal.

RISC

Reduced Instruction Set Computer. The basic principle is to have a small set of simple instructions that execute very quickly (i.e. in one cycle). This means that programs are longer, and sometimes more complicated, but run faster.

RMW

Read Modify Write. An indivisible **VMEbus** cycle that is used to both read from and write to a **slave** without permitting any other **master** to access that slave during the cycle. This is most useful in multiprocessing systems where certain memory locations are used to control access to certain resources (e.g. semaphores).

ROM

Read Only Memory. Semiconductor memory whose components are not alterable by computer instructions.

ROR

Release On Request. An access scheme in which the **VMEbus** **requester** only relinquishes control of the bus when it is required by another requester. This has an advantage over the **RWD** scheme in that if no other **master** uses the bus, the bus request phase of a transfer is avoided.

RPC

Remote Procedure Call.

RRS

Round Robin Select. Round robin is a **VMEbus** arbitration scheme for resources in which resource **bandwidth** is shared equally between competing requests. A requester that is granted a resource on one arbitration cycle has the lowest priority on the next arbitration cycle.

RS232(C)

The normal serial interface found in most **PC**s and terminals. It usually uses a 9 or 25 pin connector.

RS422

Allows higher transmission rates and has much less critical grounding requirements than the **RS232** standard. With the elimination of the ground potential problem, the transition region between mark and space states can be much narrower.

RS485

Electrically and functionally similar to **RS422**, but where RS422 only has one transmitter and one receiver, RS485 has one transmitter and many receivers. This requires a protocol to decide who has priority to transmit and the facility to stop transmitting.

RT/BC/MT

Remote Terminal/Bus Controller/Bus Monitor. The various modes in which a MIL-STD-1553B node can operate.

RTEMS

Real-Time Executive for Multiprocessor Systems. An operating system from **OAR**.

RTS

Ready To Send. A serial signal. See **CTS**.

RTC

Real Time Clock.

RWD

Release When Done. A **VMEbus** access scheme in which the **requester** relinquishes control of the bus as soon as it has finished a single data transfer cycle. This loses out to the **ROR** scheme during multiple accesses to an otherwise unused bus, as it has to request the bus each time.

Rx

Receive.

RXD

Receive Data. A serial signal.

SCSI

Small Computer Systems Interface. A standard and associated hardware for general purpose communication (usually) between a processor and large capacity storage devices.

SGL

Single Level. A **VMEbus** **arbiter** that only responds to bus requests on BR3~. This relies on the bus request **daisy chain** to arbitrate between requests.

SIO

System I/O.

SIOP

SCSI I/O Processor.

Slave

A slave detects **VMEbus** cycles initiated by a **master** and, when these cycles specify its participation, transfers data between itself and the master.

Slot

A position where a board can be inserted into a **backplane**. If the system has both a J1 and a J2 backplane (or a combination J1/J2 backplane), each slot provides a pair of 96-pin connectors.

SMI

System Management Interrupt.

SPECfp95

A benchmark package, produced in 1995, measuring the floating point performance of a processor.

SPECint95

A benchmark package, produced in 1995, measuring the integer performance of a processor.

SRAM

Static **RAM**. Memory that needs no refresh cycle once information has been stored (although it still needs power to retain its integrity).

Superscalar

A superscalar processor is a processor with multiple execution units that *may* operate in parallel.

System Controller

A board in **slot** 1 of the **VMEbus** **backplane**. It must have a SYSCLK driver, an **arbiter**, an IACK **daisy chain** driver and a bus timer.

TBA

To Be Announced.

TCP/IP

Transport Control Protocol/Internet Protocol. A collection of network protocols that together support host-to-host communication for hosts connected to any of a number of heterogeneous networks.

Network Layer Protocols (ISO Level 3)

IP	Provides internet transaction services for Layer 4 clients. Generally considered as providing Host-to-Host datagram delivery.

Transport Layer Protocols (ISO Layer 4)

TCP	A connection oriented reliable byte-stream protocol.
UDP	An unacknowledged transaction-oriented protocol parallel to TCP

Session, Presentation and Application Layer Protocols (ISO Layers 5 to 7)

FTP	Permits exchange of complete files between computers.
Telnet	Provides virtual terminal services for interactive access by terminal servers to hosts.

TEA

Transfer Error Acknowledge.

Telnet
The ARPA application level protocol. A bi-directional, **byte**-oriented communications protocol. See **TCP/IP**.

Timeout
The elapsing of a period of time within which an action should have happened.

TOD
Time-Of-Day.

TTL
Transistor/Transistor Logic.

Transceiver
A combination of a transmitter and a receiver.

Tx
Transmit.

TXD
Transmit Data. A serial signal.

U
The U is a standard unit of height measurement (e.g. 3U). One U is 4.445 centimetres (1.75 inches).

UAT
Unaligned Address Transfer. A **VMEbus** data transfer cycle that sends or receives data in an unaligned fashion.

UDP
User Datagram Protocol. See TCP/IP.

UL
Underwriter's Laboratory.

VCC
The five volt supply rail.

VDE
Verband Deutscher Elektrotechniker. The German Safety Regulations specification.

VGA
Video Graphics Array.

VITA

VFEA (VMEbus and Futurebus Extended Architecture) International Trade Association.

VME

Versa Module Europe. Often used as an abbreviation for **VMEbus**.

VME64

Extensions to the **VMEbus** standard that allow 64-bit data transfers.

VMEbus

An **ANSI/VITA** standard (1-1994) for a versatile backplane bus based on the Eurocard mechanical standard.

VRAM

Video **RAM**.

WABI

Windows Application Binary Interface

Watchdog

This is a type of timeout that ensures that a watchdog does not lock-up. If the software fails to access the watchdog at regular intervals (e.g. due to having hung-up somewhere), the watchdog brings the processor back to a known state by causing a reset.

Word

In PowerPC terminology, a 32-bit structure. Also often refers to a 16-bit data structure in **VME** systems. Cf **halfword**, **longword.**

Write Posting

This is a pipelining technique that can be used by the VME interface chip to increase system performance.

In *Master Write Posting*, when a local bus **master** writes to the **VMEbus**, instead of requesting and arbitrating for the bus, transferring data to the slave and waiting for the acknowledgement, the VME interface chip acknowledges the local bus master immediately and captures the address and data to write. The local bus master can then continue with its processing and the VME interface chip requests the VMEbus and transfers the data for the host.

Slave Write Posting works in a similar way. Write operations to the VME interface chip as a VME **slave** do not wait for the chip to become local bus master, write the data to the host memory and wait for its acknowledge. The VME interface chip acknowledges immediately and captures the address and data to write. Another transfer can then take place on the VMEbus while the VME interface chip writes the data from the previous one.

X11R5

Release 5 of version 11 of the X Windows System.

X.25

An interface between **DTE** and DCE for terminals operating in packet mode on public data networks.

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