FPGA-Based Software Defined Radio (SDR) – Project Report

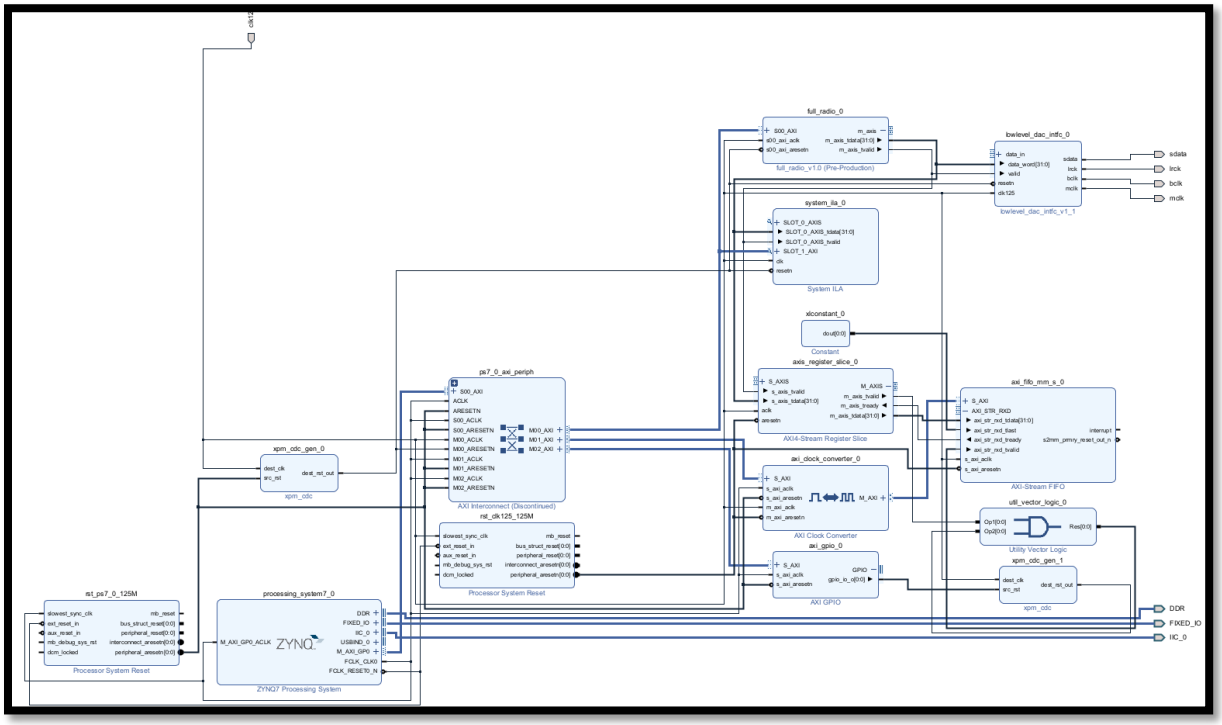
Project 1 – FPGA SDR Architecture (Zybo Z7 Block Design)

Objective: Implement a complete SDR datapath on Zynq SoC with FPGA fabric handling streaming, filtering, and DAC output.

Design Highlights:

• Built AXI-Stream chain: ADC simulation → FIR filter → AXI FIFO → DAC interface.
• Integrated clock domain crossing (XPM CDC, AXI clock converter) and async FIFOs for robust PS/PL data transfer.
• Used System ILA for live debugging of datapath signals, verifying correctness of AXI handshakes and sample flow.
• Enabled PS ↔ PL communication via AXI4-Lite for configuration and AXI-Stream for sample streaming.

Outcome: Achieved reliable SDR signal chain operation, with UDP streaming from PS to external host for visualization.



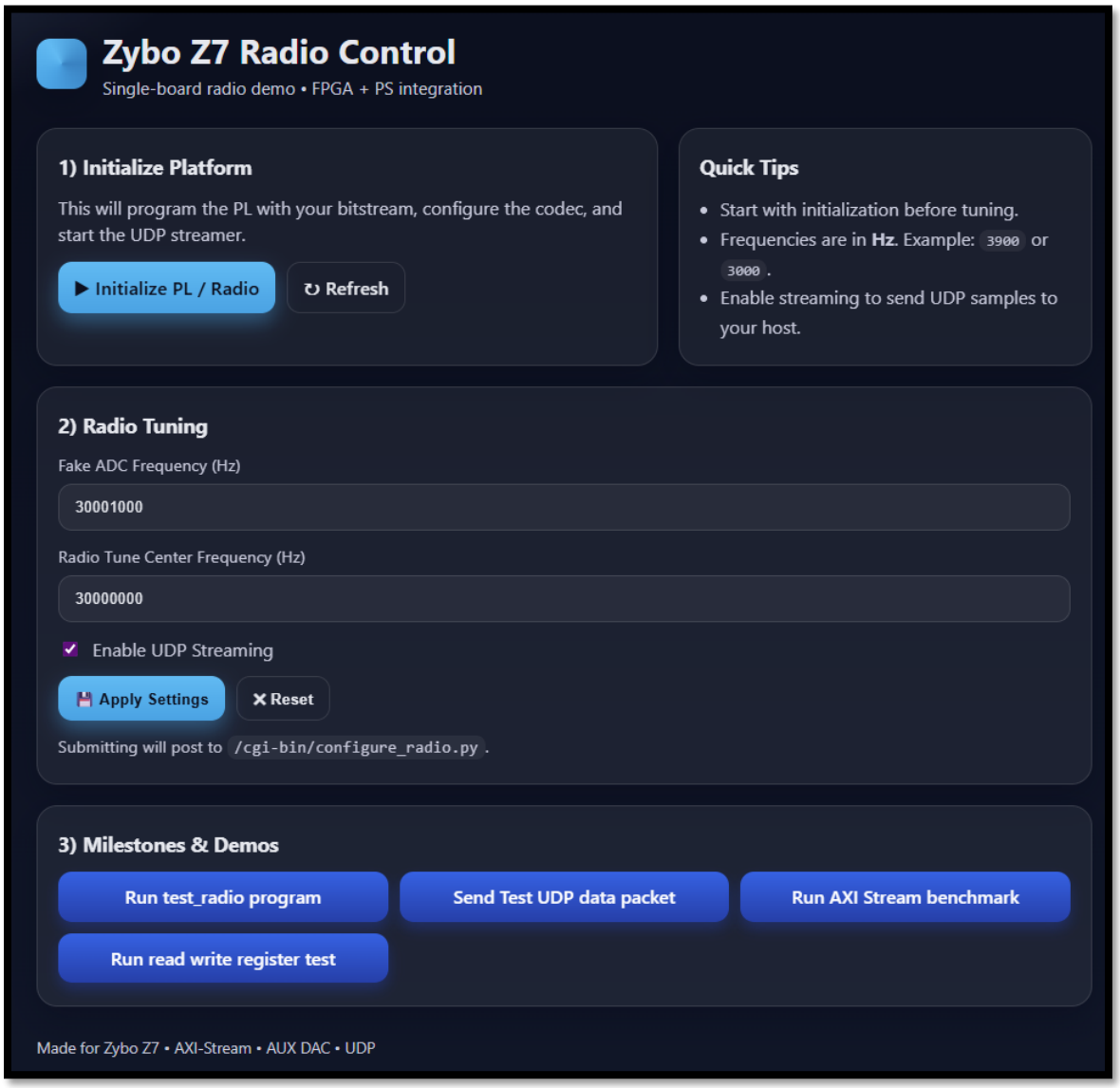
Project 2 – Web-Based SDR Control UI

Objective: Create a simple, user-friendly interface to configure and demonstrate SDR functionality.

Implementation:

• HTML-based control panel (no external dependencies) served by the PS.
• Functions: initialize FPGA bitstream + radio, set ADC/tuning frequencies, enable UDP streaming, run demos (FIFO test, register read/write, radio loopback).
• Redesigned UI with modern responsive styling for recruiters and engineers to interact with SDR quickly.

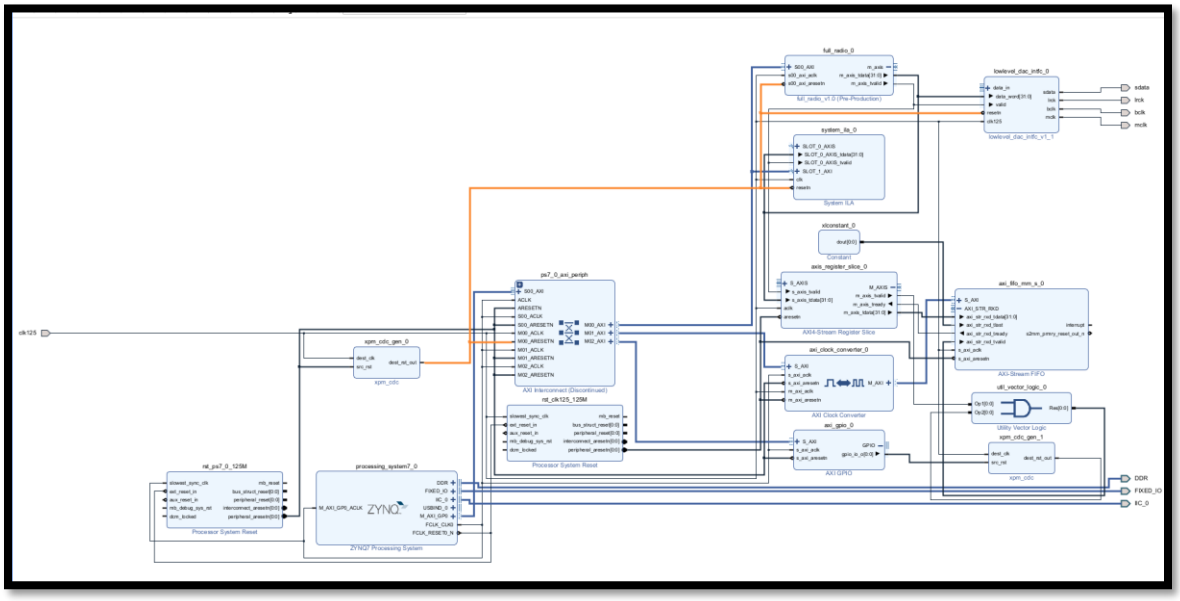
Outcome: Provided an intuitive “one-click” interface bridging low-level FPGA hardware with high-level user control.



Clock Domain Crossing (CDC) implementation

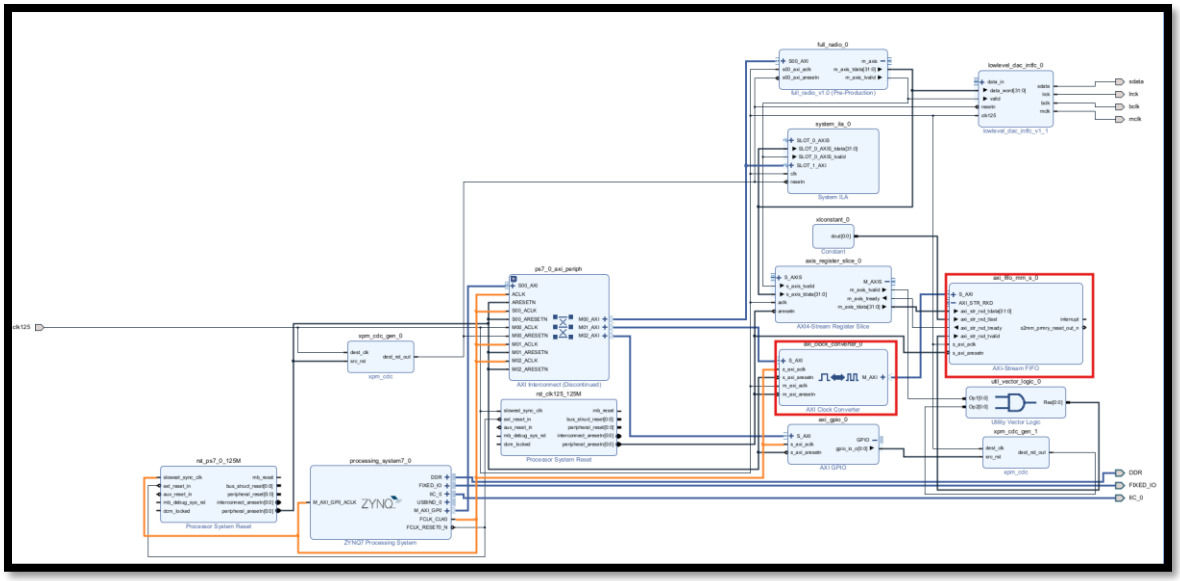
1) Reset signal from Processing System (PS) to Radio Periph and DAC interface

• Based on the requirements set by the Client, The ZynQ Processing System (PS) on the Zybo Z7 will drive a reset to the radio peripheral and the DAC interface. Since the PS has its own FCLK, a synchronizer IP has to be used to ensure proper CDC.



2) Full Radio Peripheral to Processing System (PS)

• The Processing System which is on its own clock (FCLK_CLK0) needs to read data from the AXI stream fifo which gets its data from the Full Radio Peripheral. The clock for Full Radio Peripheral is 125Mhz while the PS is running at 50Mhz. Therefore an AXI Clock Converter IP is used to ensure proper CDC.



As a result, all CDC are safe. See CDC report below.

Summary (by clock pair)

Severity	Source Clock	Destination Clock	CDC Type	Exceptions	Endpoints	Safe	Unsafe	Unknown	No ASYNC_REG
Info	sys_clk_pin	clk_fpga_0	No Common Primary Clock	Max Delay Datapath Only	10	10	0	0	0
Info	sys_clk_pin	dbg_hub/inst/B...bscan_inst/TCK	No Common Primary Clock	Max Delay Datapath Only	2	2	0	0	0
Info	clk_fpga_0	sys_clk_pin	No Common Primary Clock	Max Delay Datapath Only	12	12	0	0	0
Info	dbg_hub/inst/B...bscan_inst/TCK	sys_clk_pin	No Common Primary Clock	Max Delay Datapath Only	9	9	0	0	0

Design Timing Summary

All timing constraints are met after proper CDC handling. See Timing Summary below.

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.912 ns	Worst Hold Slack (WHS):	0.029 ns	Worst Pulse Width Slack (WPWS):	2.520 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	21685	Total Number of Endpoints:	21512	Total Number of Endpoints:	10194

All user specified timing constraints are met.

Resources Utilization

The SDR design fits comfortably on the Zybo Z7 (XC7Z020), using 5,711 LUTs (11%), 7,846 registers (7%), and 17 BRAM tiles (12%) out of available resources. DSP usage is 20 slices (9%), largely driven by the FIR filter and radio datapath. The design also uses 130 BUFG/IO resources efficiently for clocking and streaming. With timing met at 125 MHz, utilization leaves substantial headroom (<25% across major categories), showing the design is lightweight and scalable for future extensions (e.g., adding modulation schemes or more complex signal-processing blocks).

Key Skills Demonstrated

• Digital Design: RTL coding, AXI protocols, CDC, reset synchronization, hardware debugging with ILA.
• Embedded Systems: Zynq PS/PL integration, AXI4-Lite register mapping, software–hardware co-design.
• Full-Stack Engineering: Built a holistic SDR platform from RTL datapath → software control → web UI.