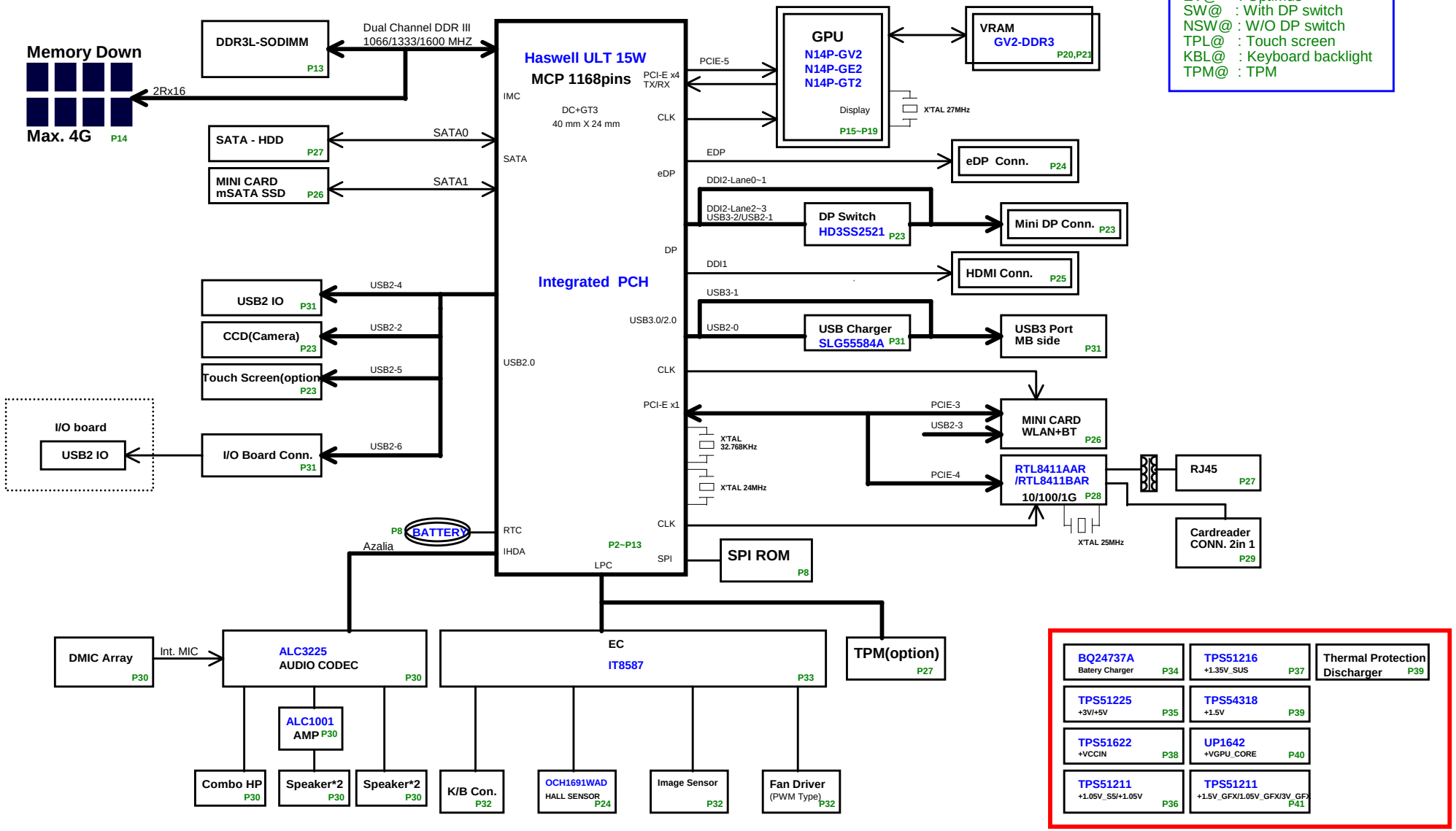
ZRQ GDDR3 SHB ULT SYSTEM BLOCK DIAGRAM

01

BOM

IV@ : iGPU
EV@ : Optimus
SW@ : With DP switch
NSW@ : W/O DP switch
TPL@ : Touch screen
KBL@ : Keyboard backlight
TPM@ : TPM



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PROJECT : ZRQ
Block Diagram
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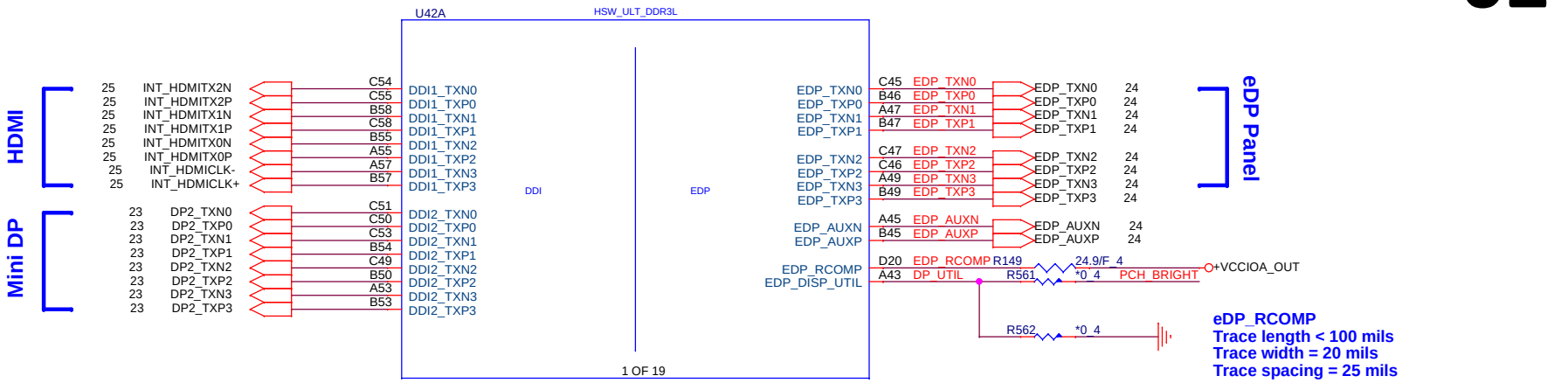
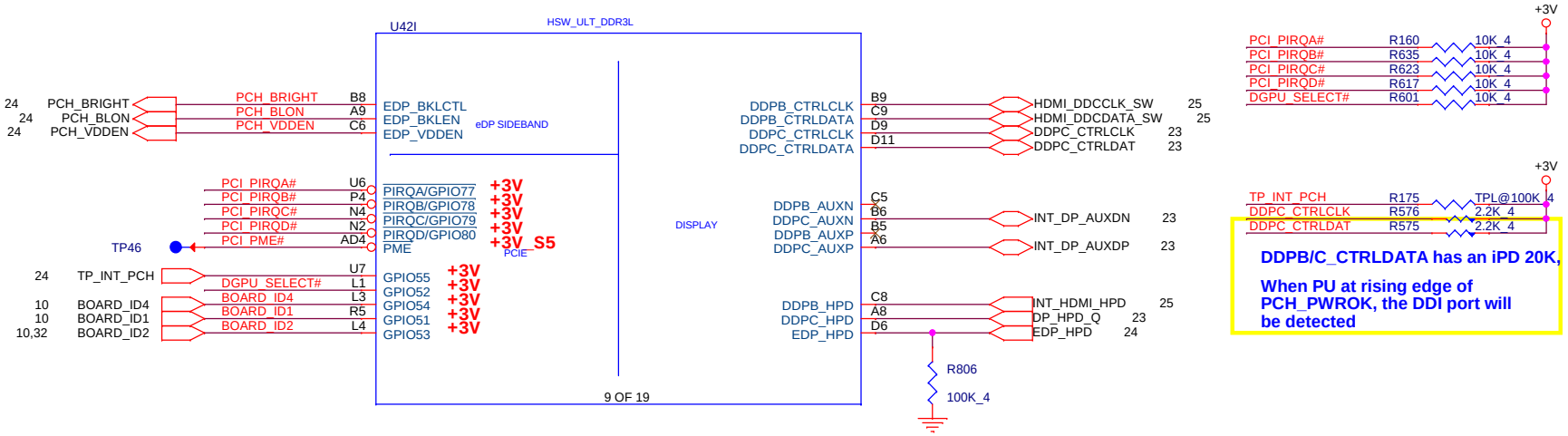
Haswell ULT (DISPLAY,eDP)

02





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Size	Document Number: Haswell 3/5 (DDI/eDP)	Rev 3A
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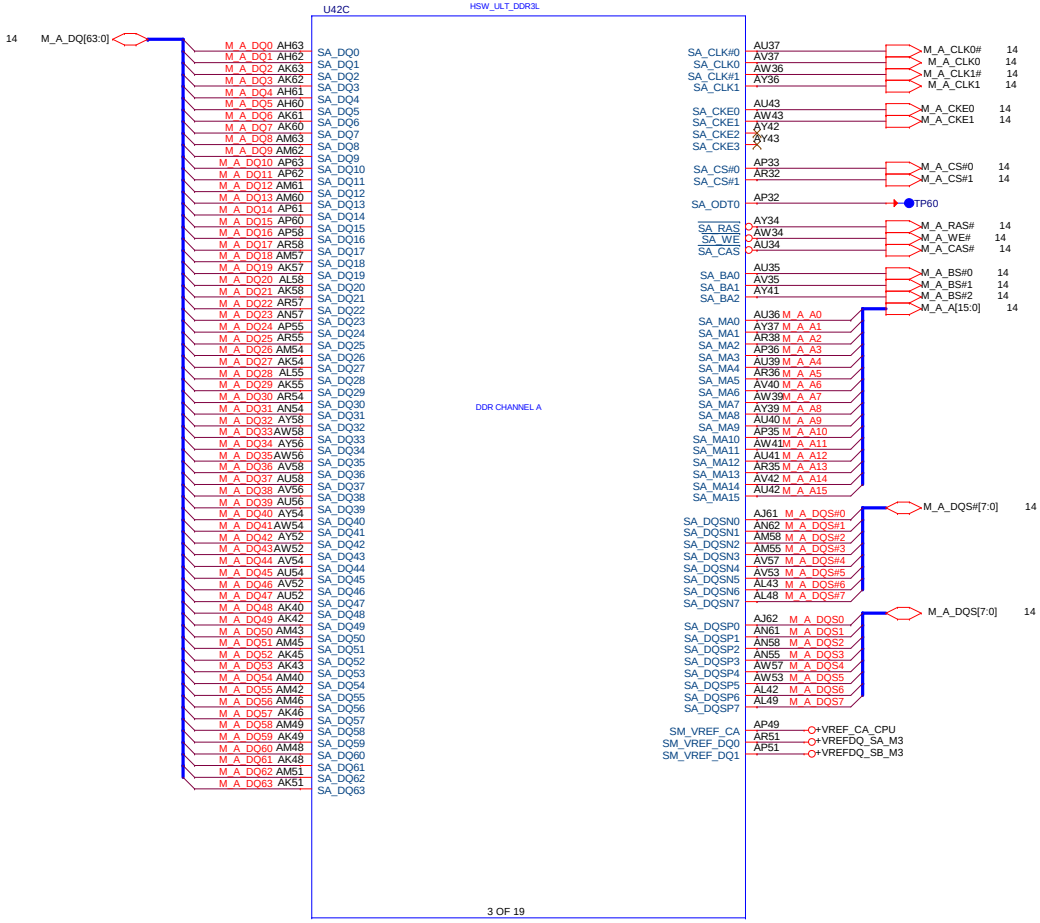
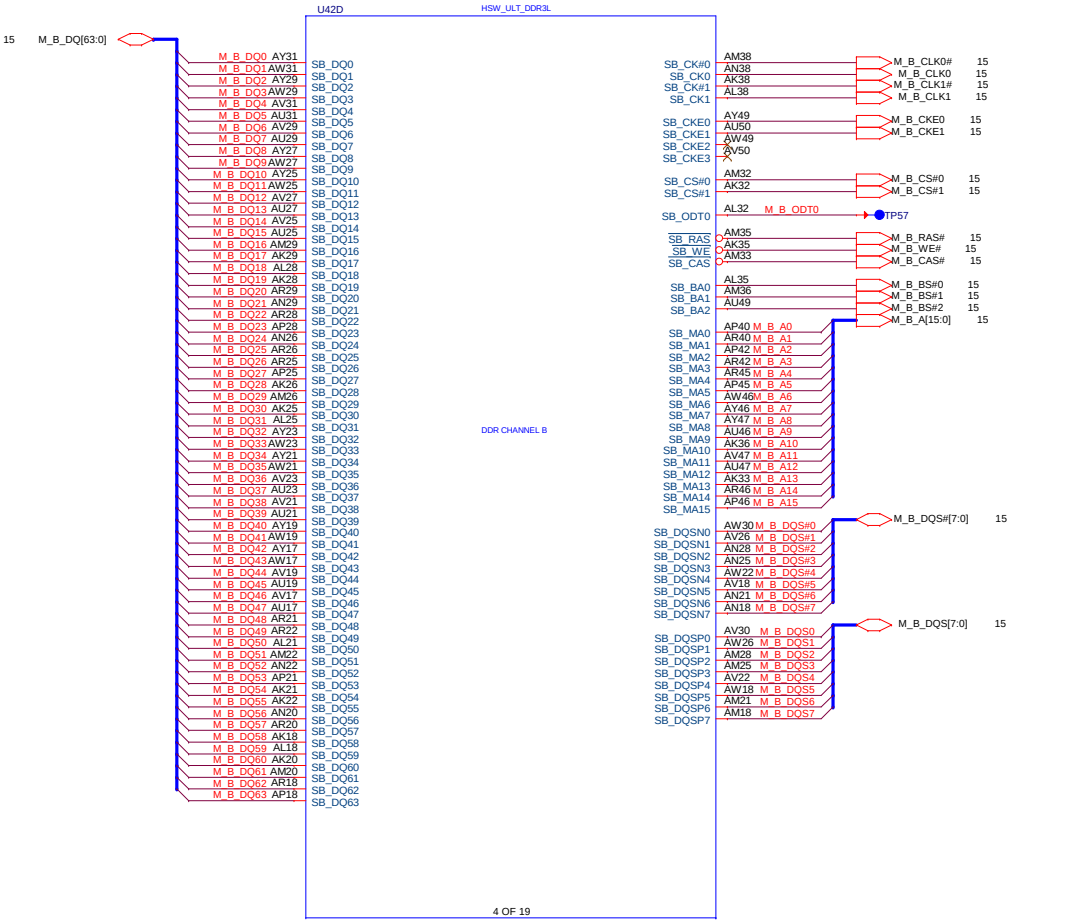
Haswell ULT (DDR3L)



Haswell Processor (DDR3)



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	Haswell 2/5 (DDR3 I/F)	3A
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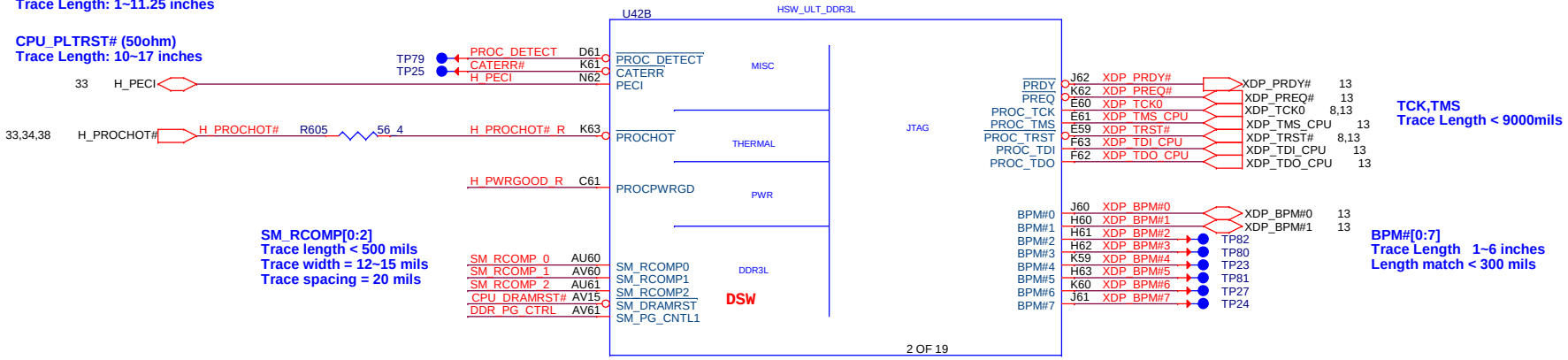
Haswell ULT (SIDEBAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

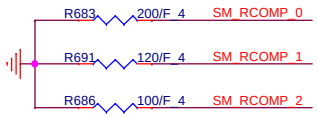


TCK,TMS
Trace Length < 9000mils

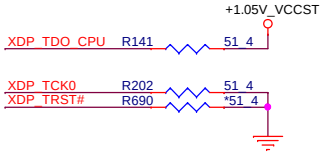
SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

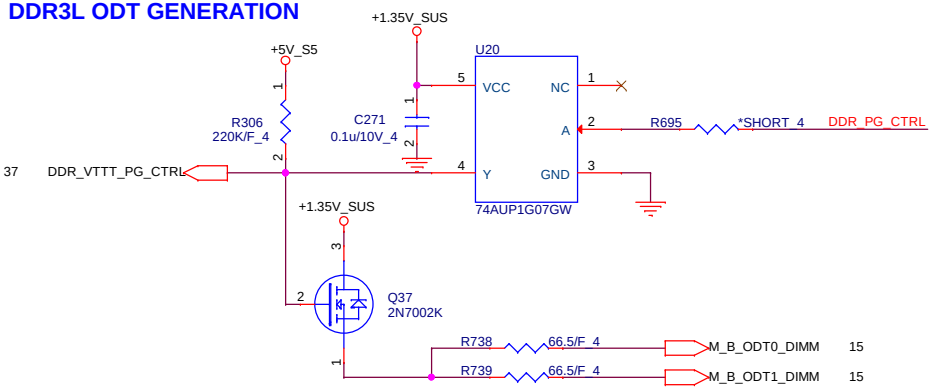
DRAM COMP



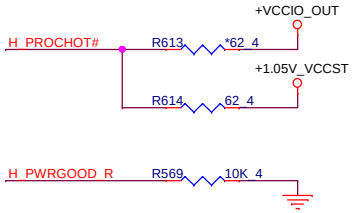
XDP PU/PD



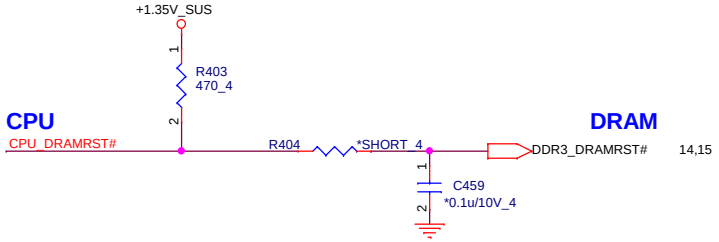
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST



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	Haswell 1/5 (PEG/DMI/FDI)	3A
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Haswell ULT (POWER)

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

VCCST PWRGD

CRB is via +1.05V PG

05

SVID

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to CPU

Place PU resistor close to CPU

HWPG_1.05V for DDR=1.5V

10/30 reserve
DDR=1.5V ,This block POP

Quanta Computer Inc.		
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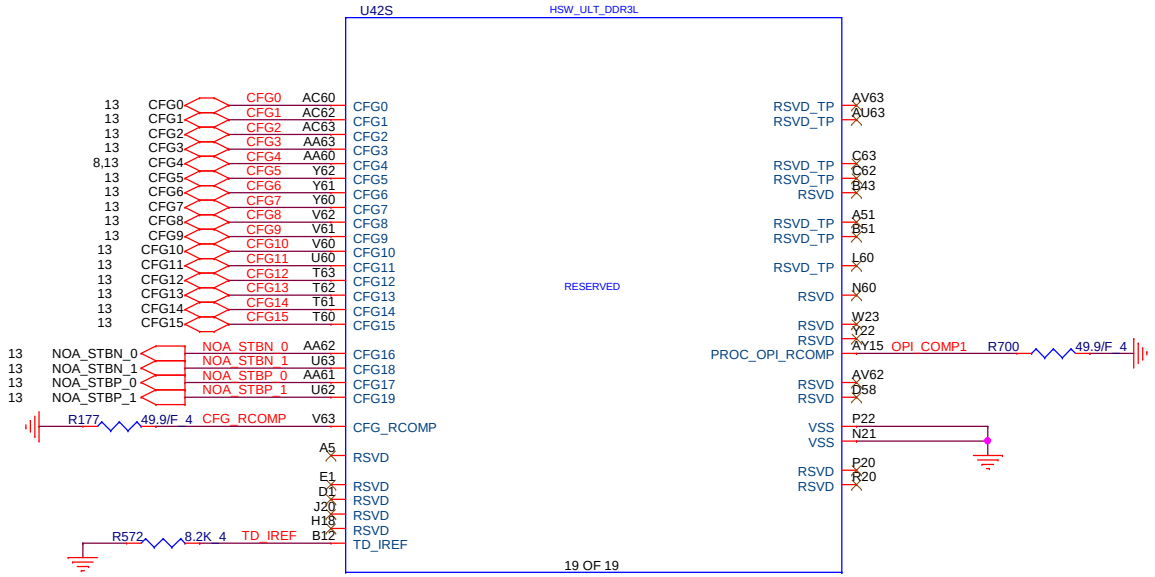
Haswell ULT (CFG,RSVD)

06



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R203 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R184 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R192 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R171 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R172 *1K_4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R183 *1K_4

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	Haswell 5/5 (CFG/GND)	3A

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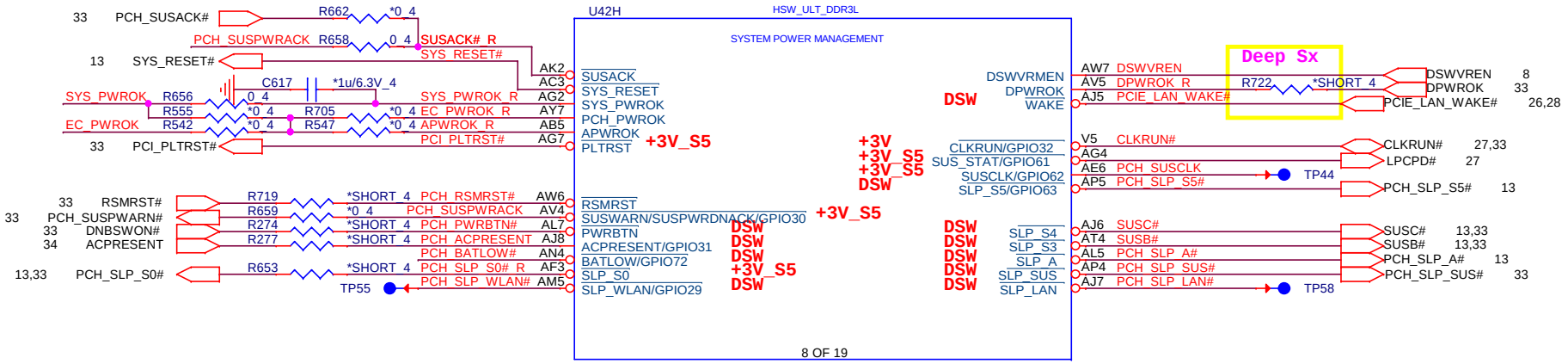
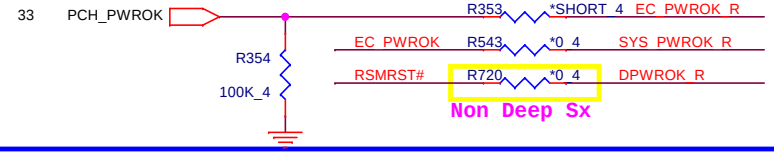
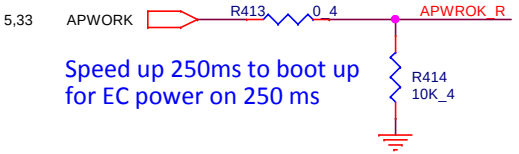
Haswell ULT PCH (PM)

07

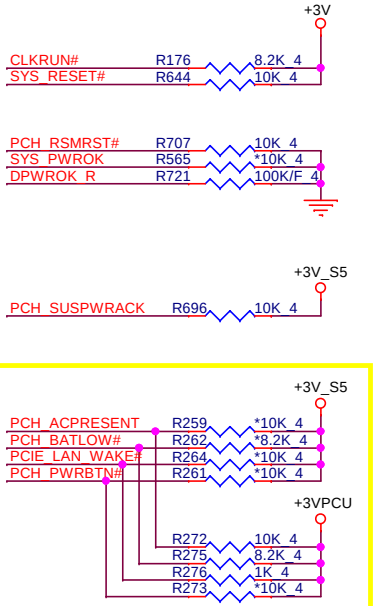


Power Sequence

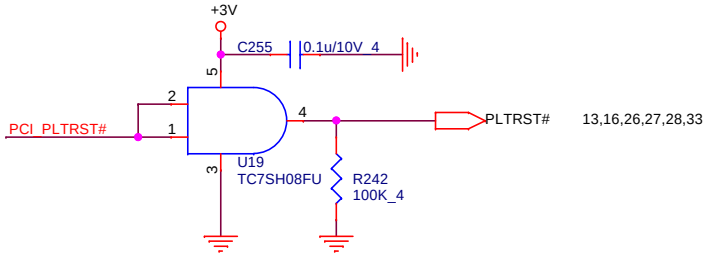




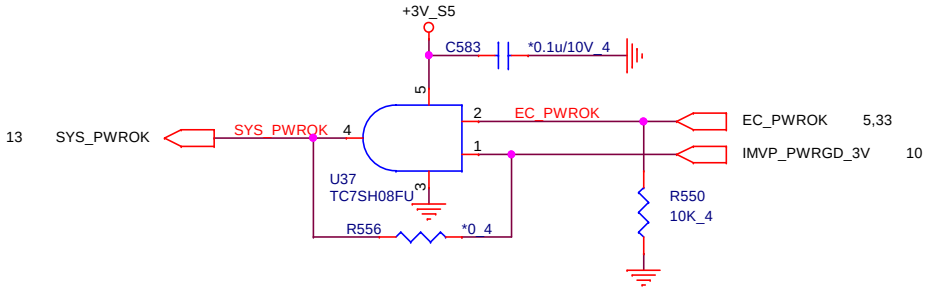
PCH PM PU/PD



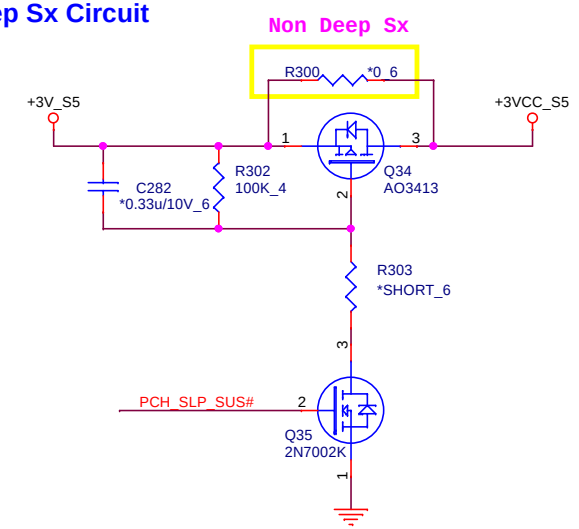
PLTRST# Buffer



SYSPWOK



Deep Sx Circuit



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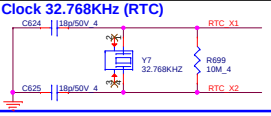
Haswell ULT PCH (RTC/HDA/SATA/SPI)

Haswell ULT PCH(LPC,SPI,SMBUS,C-LINK,THERMAL)

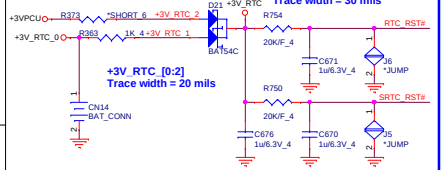
08

RTC Clock 32.768KHz (RTC)

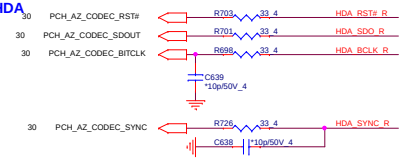


RTC Circuitry (RTC)

+3V_RTC
Trace width = 30 mils



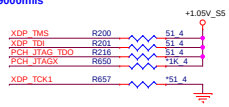
HDA

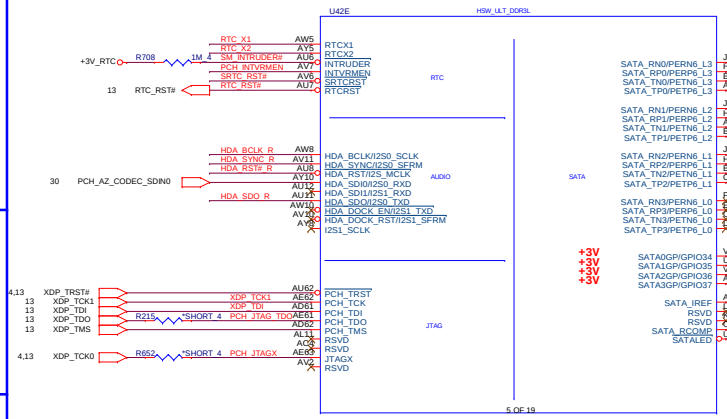


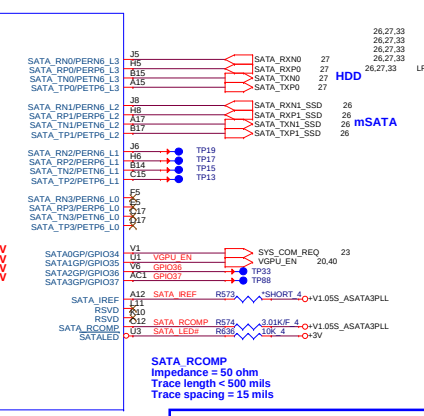
PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

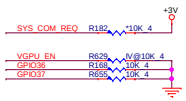
MP remove(Intel)



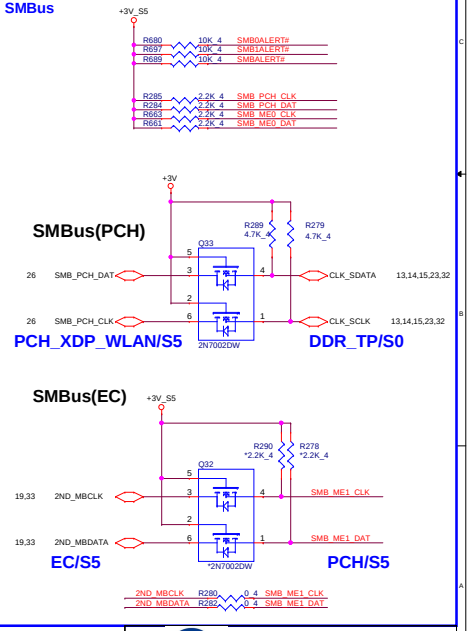




SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils



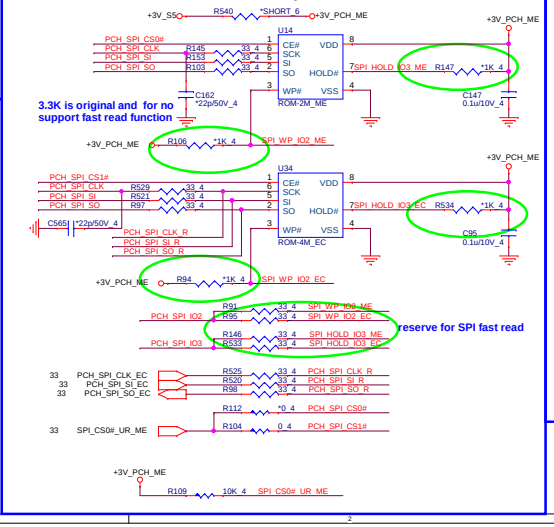
SMBus



PCH Quad SPI ROM

(Default for WIN8)

W25Q32BVSSIG / AKE391P0N00----->4MB
MX25L3206EM2I / AKE39FP0Z02----->4MB
MX25L1606EM2I / AKE38FP0Z01----->2MB
W25Q16BVSSIG / AKE38FP0N01----->2MB



ULT Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (iPD 20K) 1 =Disable No-Reboot mode	+3V R642 *1K_4 SPKR — SPKR 10,30
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (iPD 20K) 1 =can't program ME	HDA_SDO_R R702 *SHORT_4 ME_WR# 33
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	+3V_RTC R717 330K_4 PCH_INTVRMEN R704 *330K_4
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	10 GPIO66 +3V R578 *1K_4 GPIO66 R577 *1K_4
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (iPD 20K) 1 =LPC	10 GPIO86 +3V R136 *1K_4 GPIO86 R129 *1K_4
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	10 GPIO15 +3V_S5 R195 8.2K_4 GPIO15 R189 *1K_4
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 =disable	6,13 CFG4 CFG4 R193 1K_4
DSWVREN	Deep Sx well on die VR enable		1=Should be always pull-up	7 DSWVREN +3V_RTC R718 330K_4 DSWVREN R706 *330K_4

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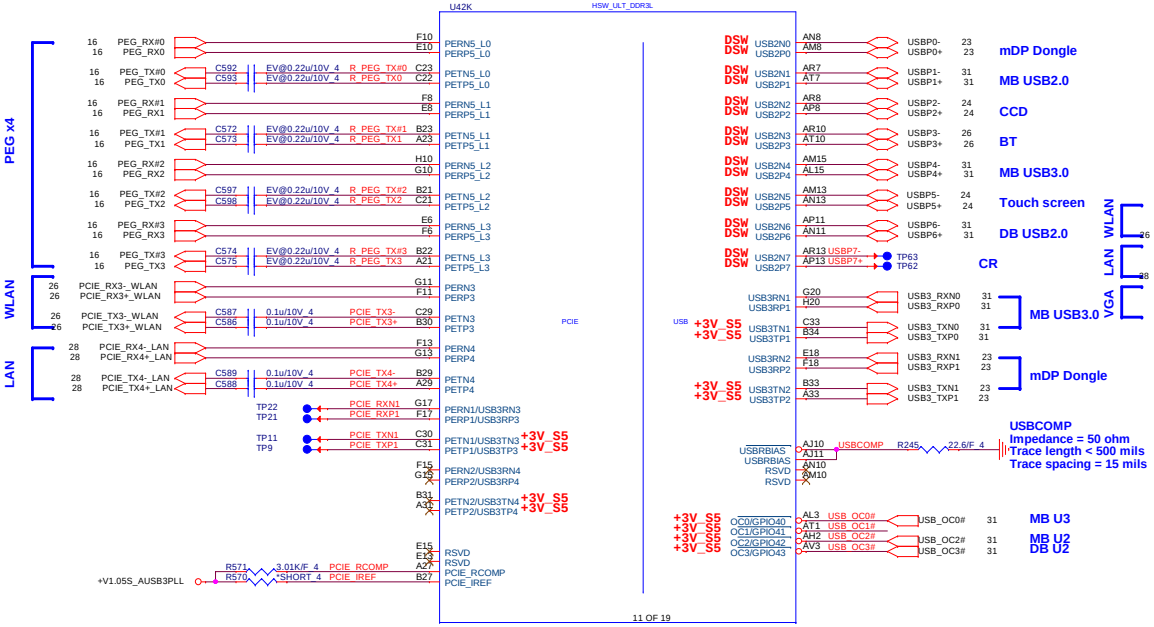
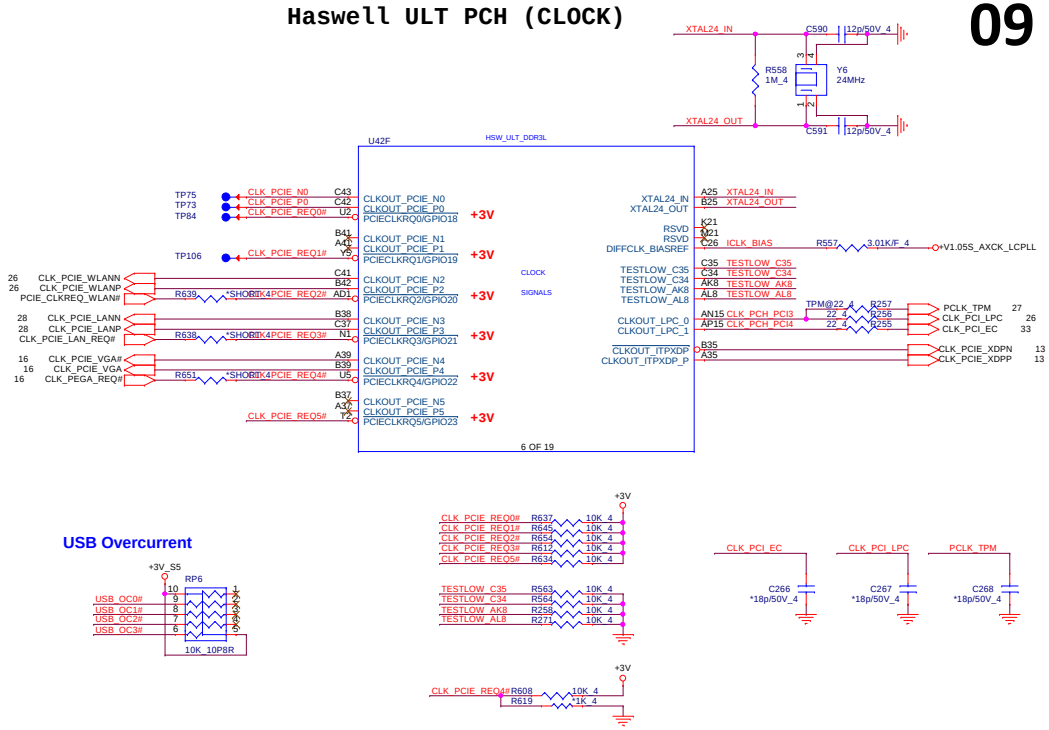
Haswell ULT PCH (PCIE,USB3.0,USB2.0)



Haswell ULT PCH (CLOCK)



09

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PROJECT : ZRQ		
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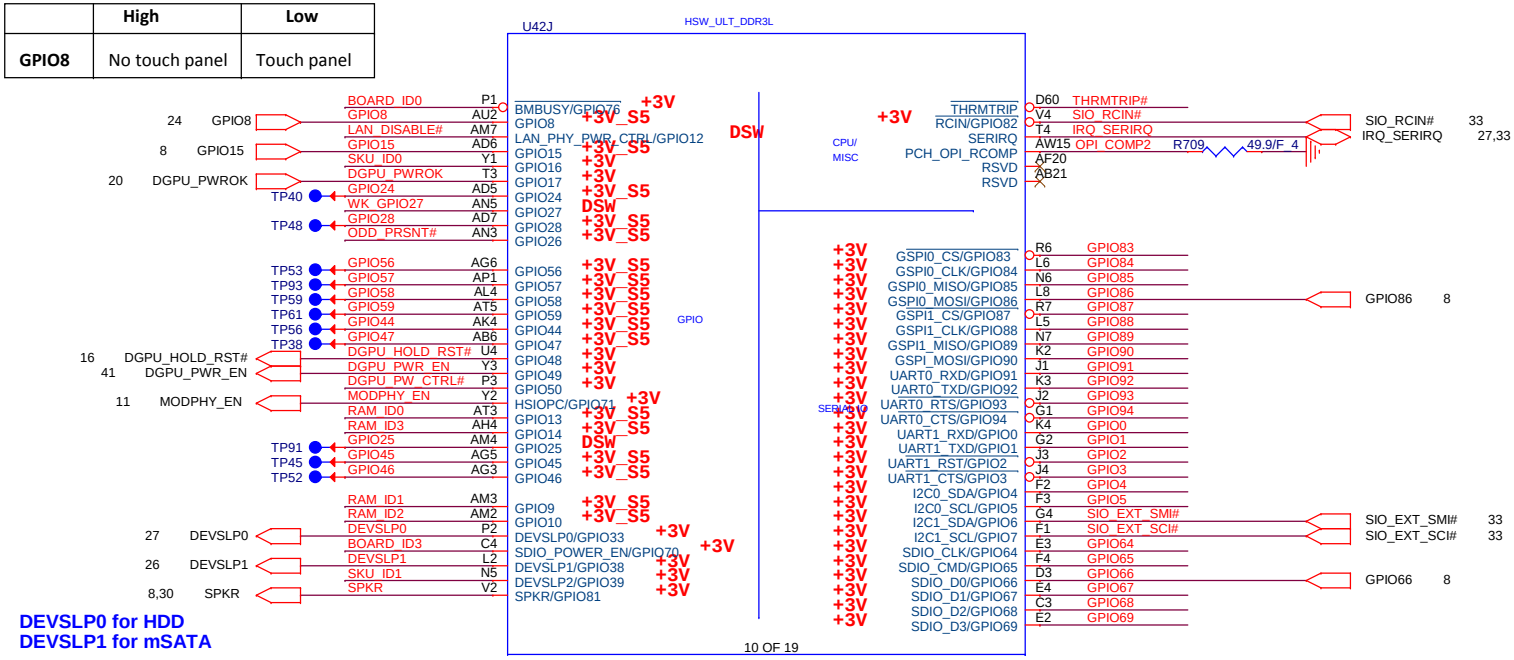
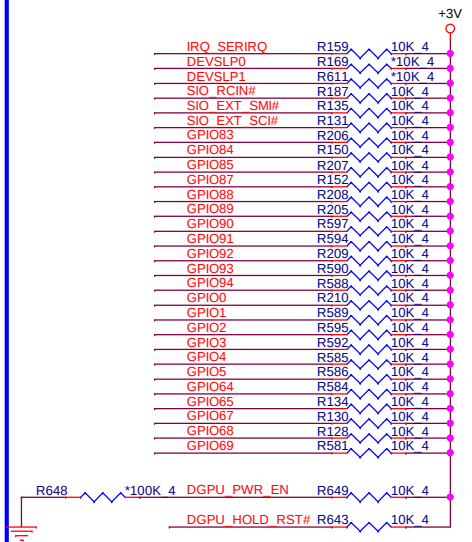
Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

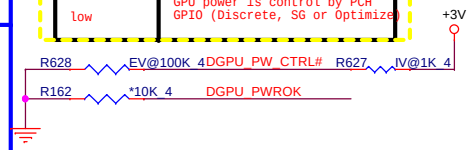
	High	Low
GPIO8	No touch panel	Touch panel

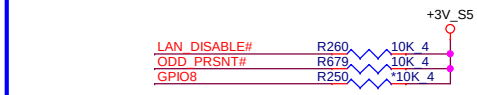


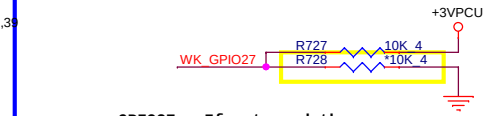
PCH GPIO PU/PD



high	UMA Only
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)

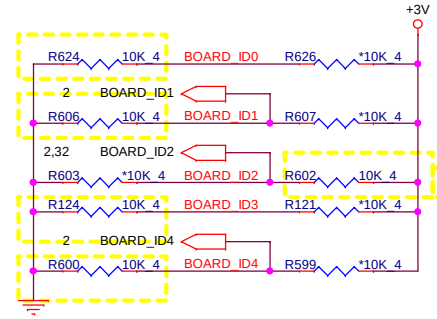






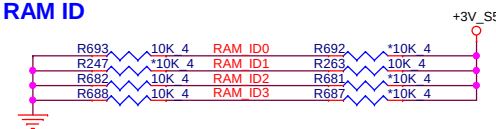
GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

Board ID



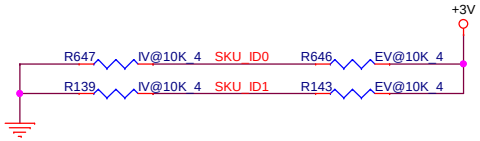
	Low	High
BOARD_ID0	DDR3	GDDR5
BOARD_ID1	Enable on board memory	Disable on board memory
BOARD_ID2	Pin8 of SYNAPTICS and ELAN are NC pin. BIOS maybe will use EEPROM detection. Default is pull high.	
BOARD_ID3	Reserved (Default)	Reserved
BOARD_ID4	Reserved (Default)	Reserved

RAM ID



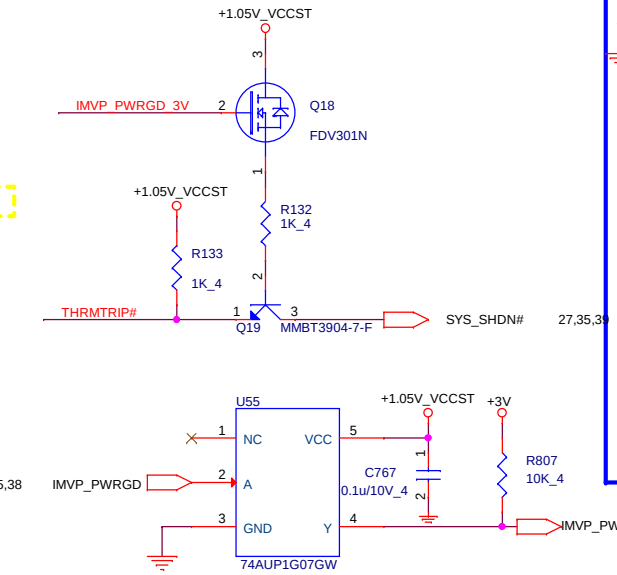
Vender	RAM_ID	Q PN	Mfr. PN	Freq.
Hynix	0000	AKD5JGETW04	H5TC4G63AFR-PRBA	1600MHz
Elpida	0001	AKD5JGST400	EDJ4216EBBG-DJ-F	1333MHz
Elpida	0010	AKD5JGST404	EDJ4216EFBG-GN-F	1600MHz

SKU ID



	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

CPU thermal trip



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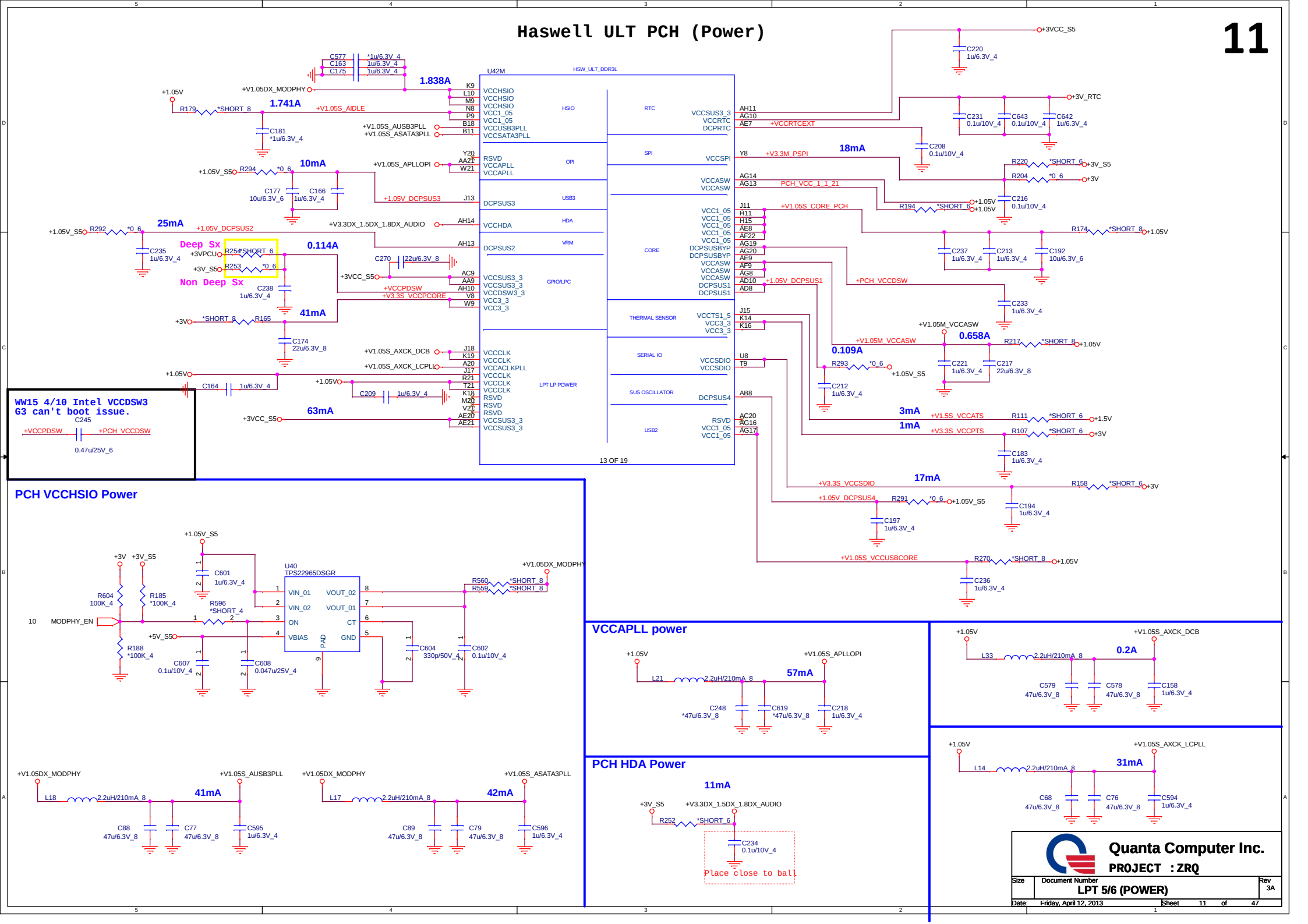
Haswell ULT PCH (Power)



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	LPT 5/6 (POWER)	3A

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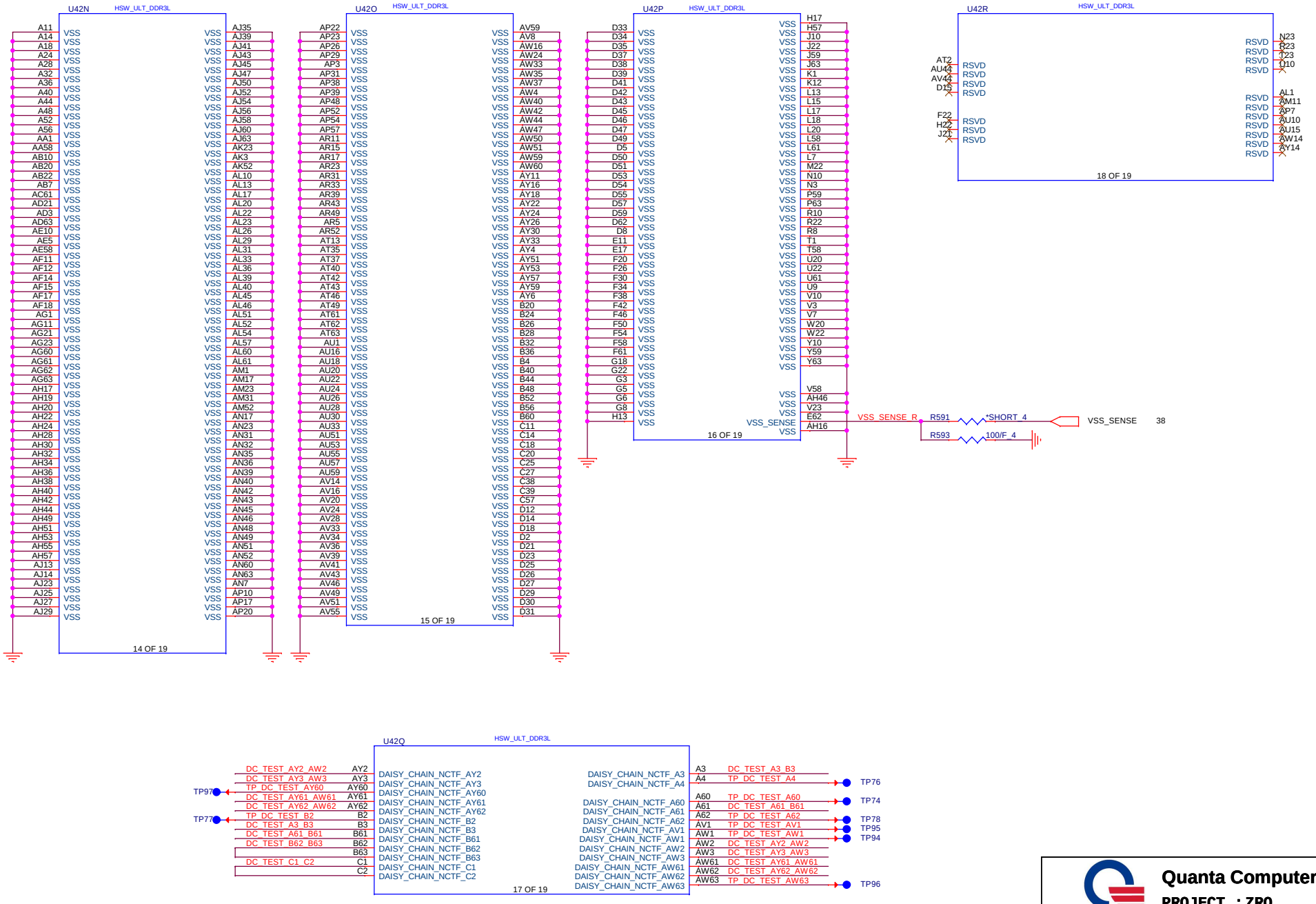
Haswell ULT (GND)



Quanta Computer Inc.		
PROJECT : ZRQ		
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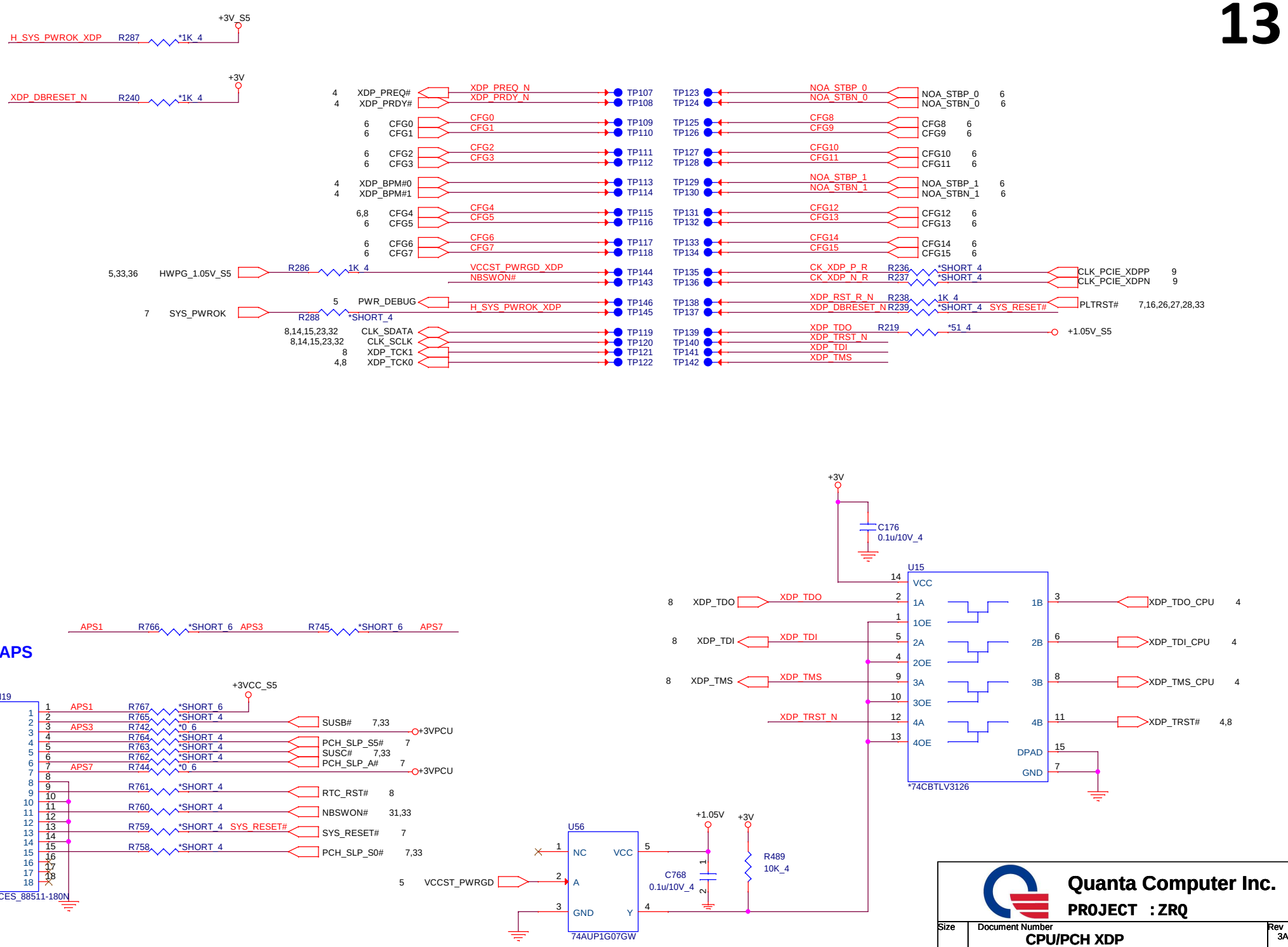
+3V_S5
H_SYS_PWROK_XDP R287 *1K_4
+3V
XDP_DBRESET_N R240 *1K_4
4 XDP_PREQ# XDP_PREQ_N TP107
4 XDP_PRDY# XDP_PRDY_N TP108
6 CFG0 CFG0 TP109
6 CFG1 CFG1 TP110
6 CFG2 CFG2 TP111
6 CFG3 CFG3 TP112
4 XDP_BPM#0 TP113
4 XDP_BPM#1 TP114
6,8 CFG4 CFG4 TP115
6 CFG5 CFG5 TP116
6 CFG6 CFG6 TP117
6 CFG7 CFG7 TP118
5,33,36 HWPG_1.05V_S5 R286 1K_4 VCCST_PWRGD_XDP TP144
NBSWON# TP143
5 PWR_DEBUG TP146
7 SYS_PWROK R288 *SHORT_4 H_SYS_PWROK_XDP TP145
8,14,15,23,32 CLK_SDATA TP119
8,14,15,23,32 CLK_SCLK TP120
8 XDP_TCK1 TP121
4,8 XDP_TCK0 TP122
TP123 NOA_STBP_0 NOA_STBP_0 6
TP124 NOA_STBN_0 NOA_STBN_0 6
TP125 CFG8 CFG8 6
TP126 CFG9 CFG9 6
TP127 CFG10 CFG10 6
TP128 CFG11 CFG11 6
TP129 NOA_STBP_1 NOA_STBP_1 6
TP130 NOA_STBN_1 NOA_STBN_1 6
TP131 CFG12 CFG12 6
TP132 CFG13 CFG13 6
TP133 CFG14 CFG14 6
TP134 CFG15 CFG15 6
TP135 CK_XDP_P_R R236 *SHORT_4 CLK_PCIE_XDPP 9
TP136 CK_XDP_N_R R237 *SHORT_4 CLK_PCIE_XDPN 9
TP138 XDP_RST_R_N R238 1K_4
TP137 XDP_DBRESET_N R239 *SHORT_4 SYS_RESET# PLTRST# 7,16,26,27,28,33
TP139 XDP_TDO R219 *51_4 +1.05V_S5
XDP_TRST_N TP140
XDP_TDI TP141
XDP_TMS TP142
APS1 R766 *SHORT_6 APS3 R745 *SHORT_6 APS7
APS
CN19
+3VCC_S5
APS1 R767 *SHORT_6
R765 *SHORT_4 SUSB# 7,33
APS3 R742 *0_6 +3VPCU
R764 *SHORT_4
R763 *SHORT_4 PCH_SLP_S5# 7
R762 *SHORT_4 SUSC# 7,33
APS7 R744 *0_6 PCH_SLP_A# 7 +3VPCU
R761 *SHORT_4 RTC_RST# 8
R760 *SHORT_4 NBSWON# 31,33
R759 *SHORT_4 SYS_RESET# SYS_RESET# 7
R758 *SHORT_4 PCH_SLP_S0# 7,33
*ACES_88511-180N
5 VCCST_PWRGD
U56
NC VCC
A
GND Y
74AUP1G07GW
+1.05V
+3V
C768 0.1u/10V_4
R489 10K_4
+3V
C176 0.1u/10V_4
U15
VCC
8 XDP_TDO XDP_TDO 1A 1B XDP_TDO_CPU 4
1OE
8 XDP_TDI XDP_TDI 2A 2B XDP_TDI_CPU 4
2OE
8 XDP_TMS XDP_TMS 3A 3B XDP_TMS_CPU 4
3OE
XDP_TRST_N 4A 4B XDP_TRST# 4,8
4OE
DPAD
GND
*74CBTLV3126
Quanta Computer Inc.
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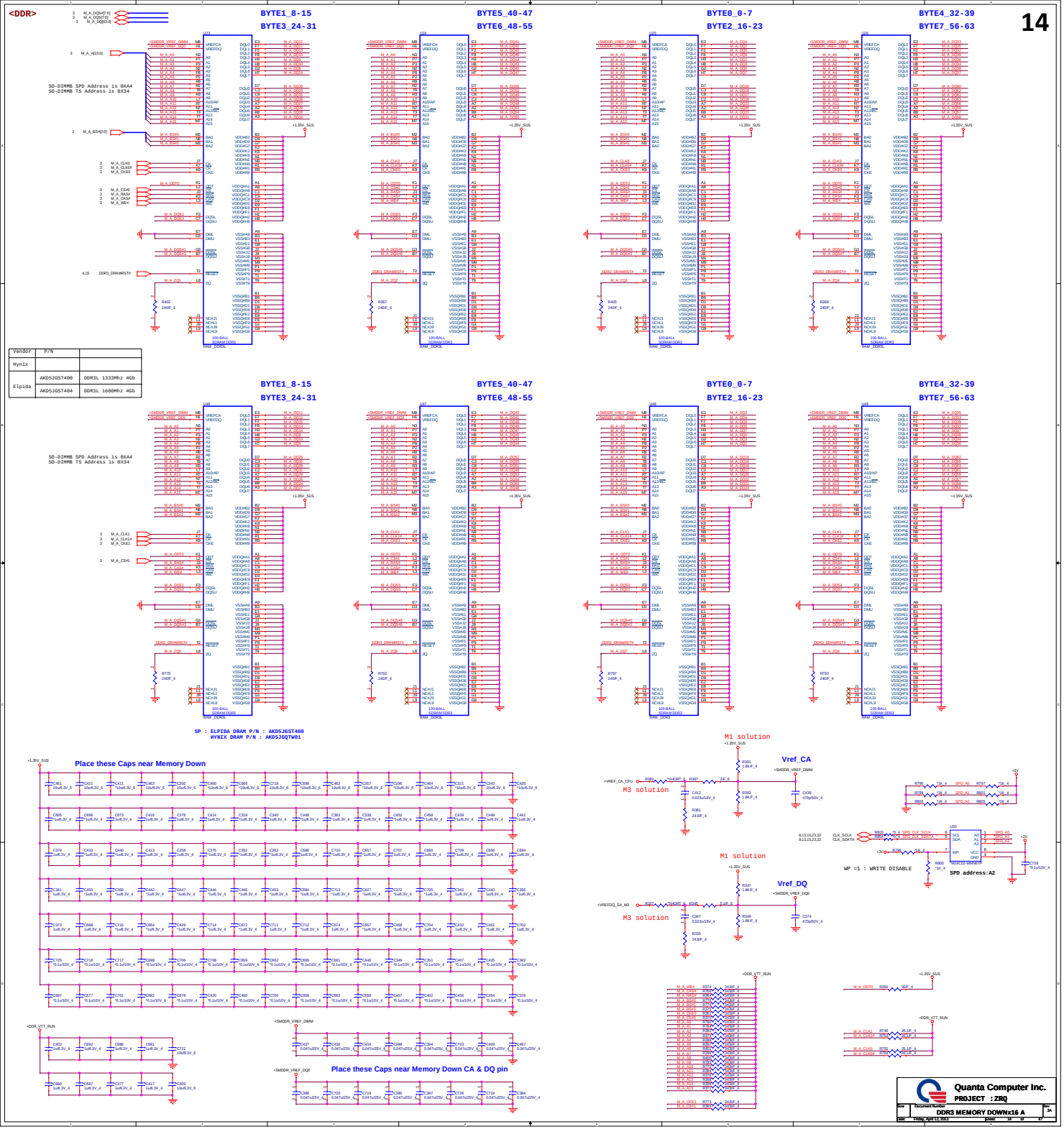
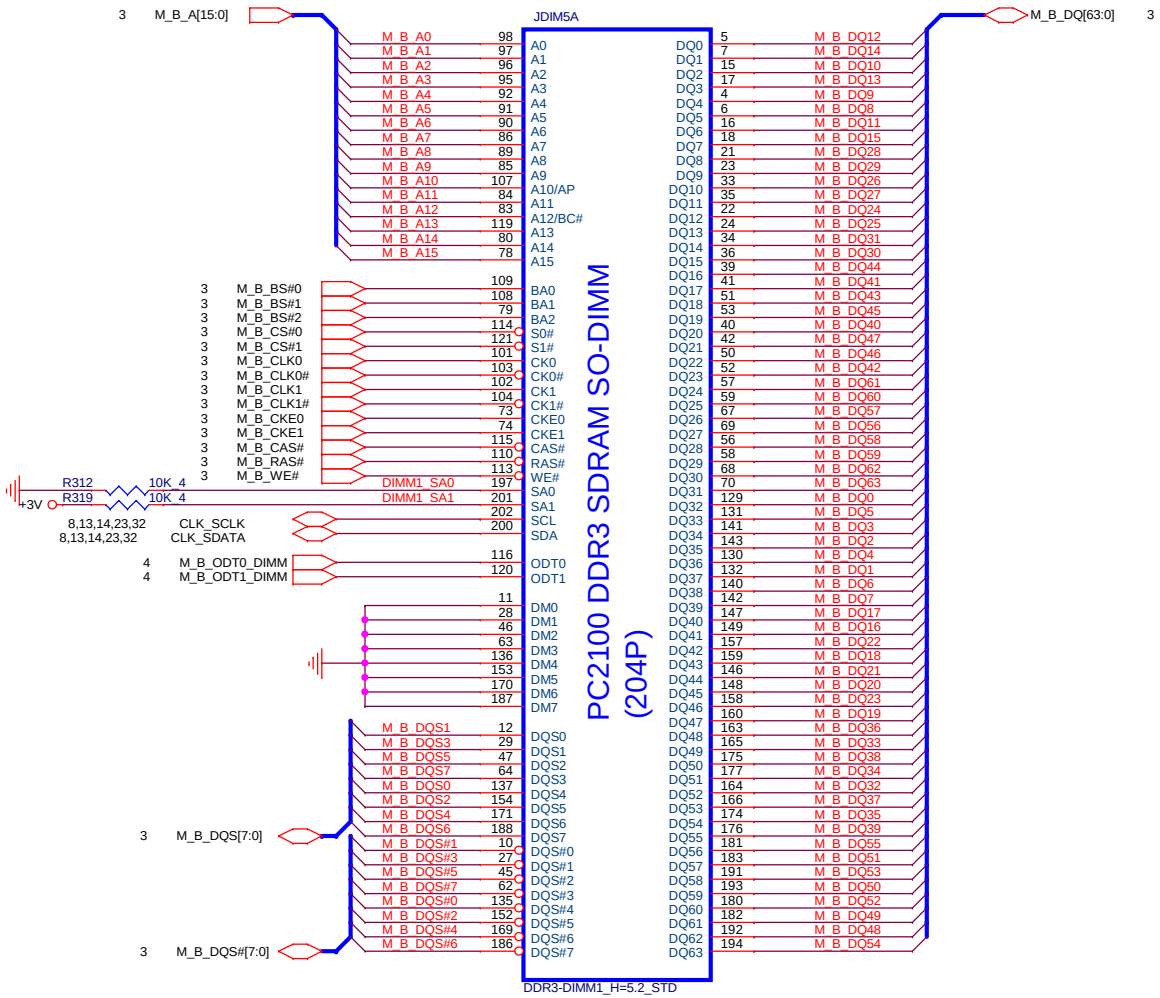
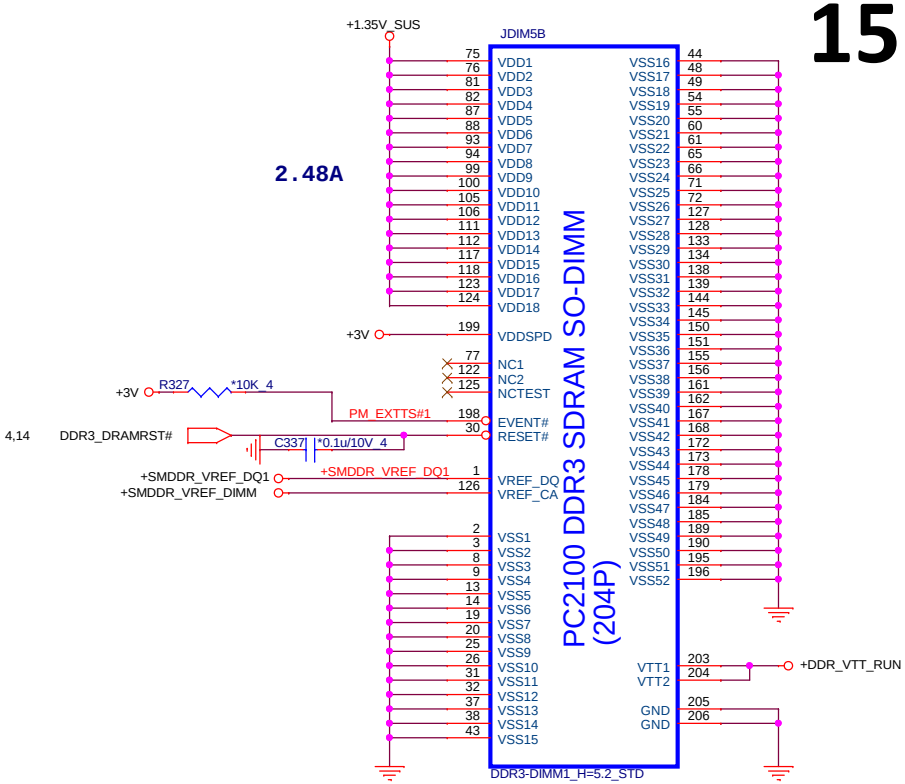
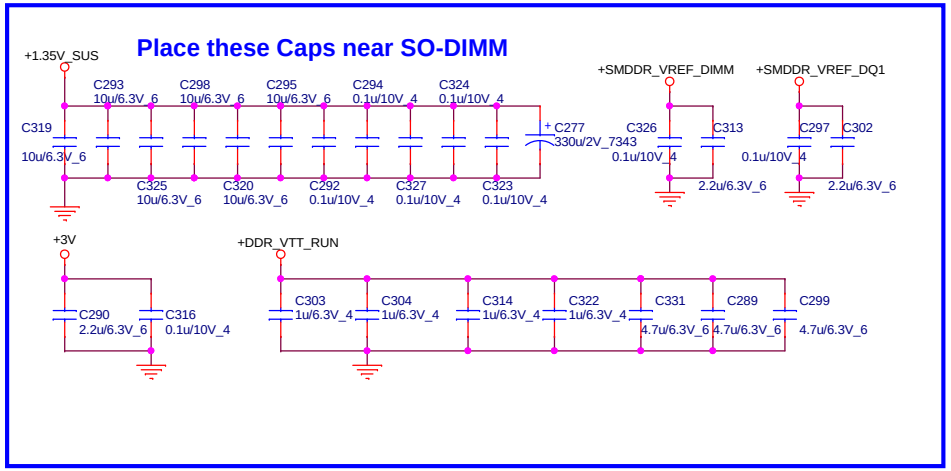
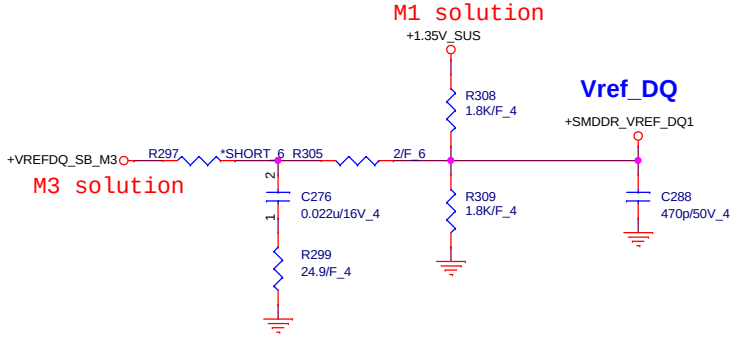


Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb









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N14P-GV2	
N14P-GT	

16

1000mA

+1.05V_GFX

To be placed no further from the GPU than bewteen BGA and Power supply
C564 EV@22u/6.3V_8
C563 EV@22u/6.3V_8
C153 EV@10u/6.3V_6
C109 EV@10u/6.3V_6
place near balls
C118 EV@4.7u/6.3V_6
C143 EV@1u/6.3V_4
place under BGA
C123 EV@1u/6.3V_4

+1.05V_GFX

To be placed no further from the GPU than bewteen BGA and Power supply
C570 EV@22u/6.3V_8
C569 EV@22u/6.3V_8
C98 EV@10u/6.3V_6
C70 EV@10u/6.3V_6
place near balls
C133 EV@4.7u/6.3V_6
C80 EV@1u/6.3V_4
place under BGA
C78 EV@1u/6.3V_4

2500mA

U39A

[PEG Interface]

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6

AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
AL27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

PEX_RX0 AN12 PEG_TX0 — PEG_TX0 9
PEX_RX0_N AM12 PEG_TX#0 — PEG_TX#0 9
PEX_RX1 AN14 PEG_TX1 — PEG_TX1 9
PEX_RX1_N AM14 PEG_TX#1 — PEG_TX#1 9
PEX_RX2 AP14 PEG_TX2 — PEG_TX2 9
PEX_RX2_N AP15 PEG_TX#2 — PEG_TX#2 9
PEX_RX3 AN15 PEG_TX3 — PEG_TX3 9
PEX_RX3_N AM15 PEG_TX#3 — PEG_TX#3 9
PEX_RX4 AN17
PEX_RX4_N AM17
PEX_RX5 AP17
PEX_RX5_N AP18
PEX_RX6 AN18
PEX_RX6_N AM18
PEX_RX7 AN20
PEX_RX7_N AM20
PEX_RX8 AP20
PEX_RX8_N AP21
PEX_RX9 AN21
PEX_RX9_N AM21
PEX_RX10 AN23
PEX_RX10_N AM23
PEX_RX11 AP23
PEX_RX11_N AP24
PEX_RX12 AN24
PEX_RX12_N AM24
PEX_RX13 AN26
PEX_RX13_N AM26
PEX_RX14 AP26
PEX_RX14_N AP27
PEX_RX15 AN27
PEX_RX15_N AM27

PEX_TX0 AK14 R_PEG_RX0 C142 EV@0.22u/10V_4 — PEG_RX0 9
PEX_TX0_N AJ14 R_PEG_RX#0 C135 EV@0.22u/10V_4 — PEG_RX#0 9
PEX_TX1 AH14 R_PEG_RX1 C131 EV@0.22u/10V_4 — PEG_RX1 9
PEX_TX1_N AG14 R_PEG_RX#1 C121 EV@0.22u/10V_4 — PEG_RX#1 9
PEX_TX2 AK15 R_PEG_RX2 C112 EV@0.22u/10V_4 — PEG_RX2 9
PEX_TX2_N AJ15 R_PEG_RX#2 C104 EV@0.22u/10V_4 — PEG_RX#2 9
PEX_TX3 AL16 R_PEG_RX3 C120 EV@0.22u/10V_4 — PEG_RX3 9
PEX_TX3_N AK16 R_PEG_RX#3 C115 EV@0.22u/10V_4 — PEG_RX#3 9
PEX_TX4 AK17
PEX_TX4_N AJ17
PEX_TX5 AH17
PEX_TX5_N AG17
PEX_TX6 AK18
PEX_TX6_N AJ18
PEX_TX7 AL19
PEX_TX7_N AK19
PEX_TX8 AK20
PEX_TX8_N AJ20
PEX_TX9 AH20
PEX_TX9_N AG20
PEX_TX10 AK21
PEX_TX10_N AJ21
PEX_TX11 AL22
PEX_TX11_N AK22
PEX_TX12 AK23
PEX_TX12_N AJ23
PEX_TX13 AH23
PEX_TX13_N AG23
PEX_TX14 AK24
PEX_TX14_N AJ24
PEX_TX15 AL25
PEX_TX15_N AK25

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13

PEX_REFCLK AL13 — CLK_PCIE_VGA 9
PEX_REFCLK_N AK13 — CLK_PCIE_VGA# 9

PEX_TSTCLK_OUT AJ26 PEX_TSTCLK R114 *EV@200/F_4
PEX_TSTCLK_OUT_N AK26 PEX_TSTCLK#

0815 change R53 to 1% tolerance

PEX_WAKE AJ11
PEX_RST_N AJ12 PEGX_RST#

PEX_CLKREQ_N AK12 PEX_CLKREQ#

PEX_TERMP AP29 PEX_TERMP R523 EV@2.49K/F_4
TESTMODE AK11 TESTMODE R157 EV@10K/F_4

PEX_PLLVDD AG26
PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
3.3V_AUX_NC P8
VDD_SENSE L4
GND_SENSE L5

J8/K8 0.4MM = 16mils

J8 VDD33_1
K8 VDD33_2
L8 VDD33_3
M8 VDD33_4

+3V_GFX

L8/M8 0.4MM = 16mils

PLACE CLOSE TO BGA L8/M8
+3V_GFX
C244 EV@4.7u/6.3V_6
C243 EV@1u/6.3V_4
C240 EV@0.1u/10V_4
C242 EV@0.1u/10V_4
C241 EV@0.1u/10V_4
PLACE CLOSE TO GPU BALLS L8/M8

PEX_PLLVDD R110 EV@0_6 — +1.05V_GFX

R1

C96 EV@4.7u/6.3V_6
C87 EV@1u/6.3V_4 — place near BGA
C84 EV@0.1u/10V_4 — place near ball

C1
C72 *EV@GV2@1u/6.3V_4

C182 EV@0.1u/10V_4
C185 EV@4.7u/6.3V_6
C184 EV@4.7u/6.3V_6 — +3V_GFX — PLACE NEAR BGA

AH12/AG12 need 210mA of +3V_GFX

RSVD R1 and C1 for GV2 co-layout sDDR3

PEX_PLLVDD : 0.3MM = 12mils (150mA)

GPU_VCCP_SENSE
GPU_VSSP_SENSE
40 40 8mils width (0.2MM)

EV@N14P

N14P

+3V_GFX +3V_GFX

R148 EV@10K/F_4

Follow Z09 to isolate CLK_REQ#

PEX_CLKREQ# — 1 — Q23 EV@2N7002K — 3 — CLK_PEGA_REQ# 9

PU at page 9

R154 *EV@0_4

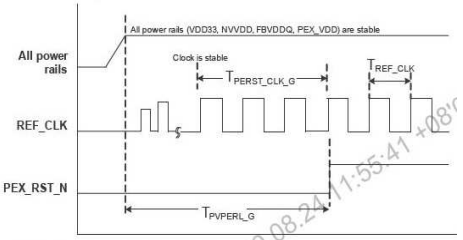


Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

+3V

C622 EV@0.1u/10V_4

7,13,26,27,28,33 PLTRST#
10 DGPU_HOLD_RST#

U45 EV@TC7SH08FU

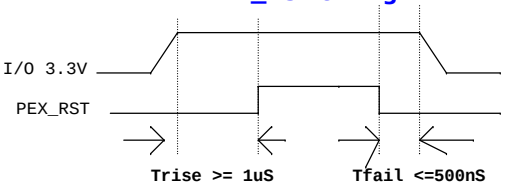
PEGX_RST# — PEGX_RST# 19

R694 EV@100K_4

R710 *EV@0_4

PCH control PEGX_RST#

PEX_RST timing



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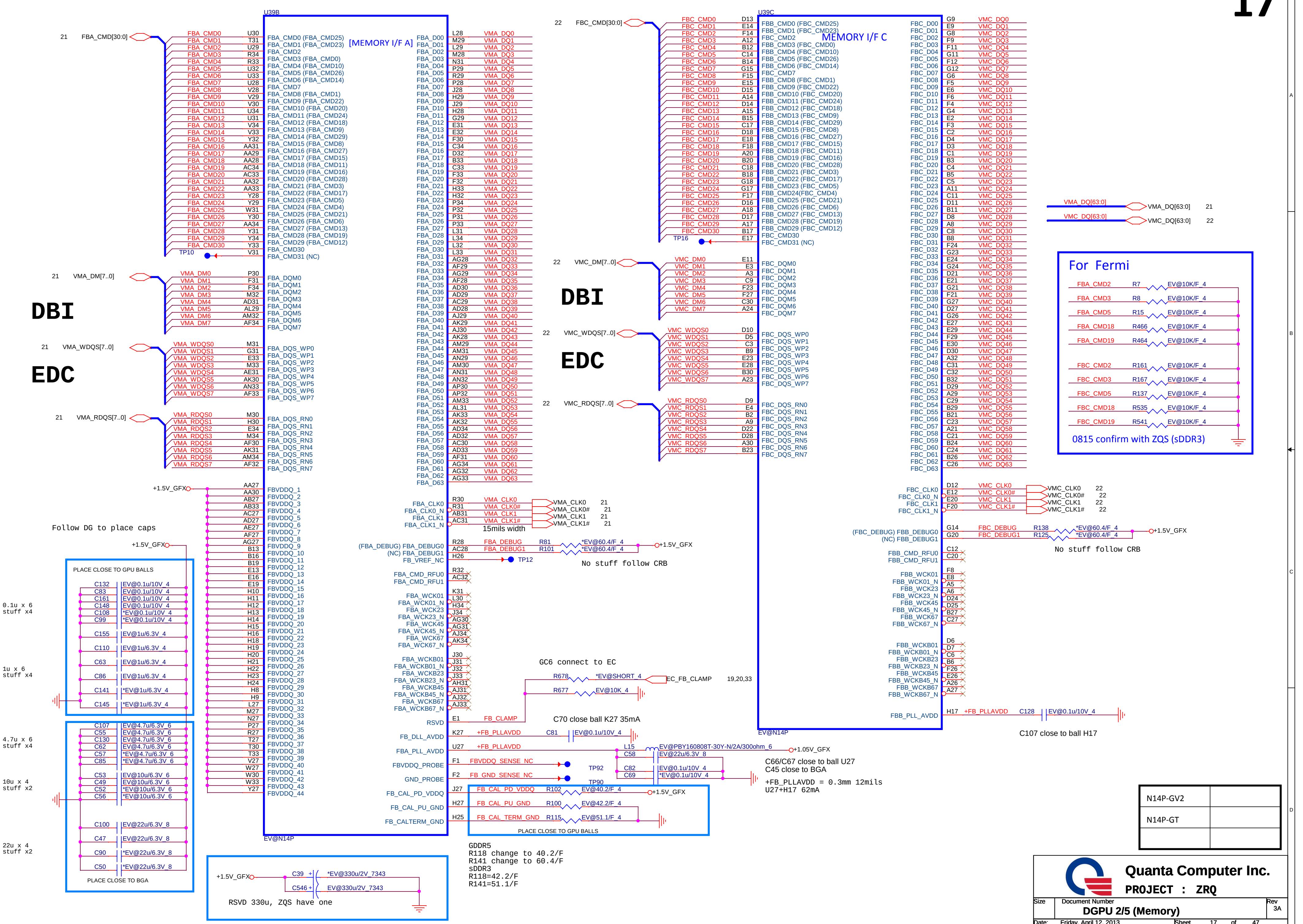

N14P-GV2	
N14P-GT	

Quanta Computer Inc.

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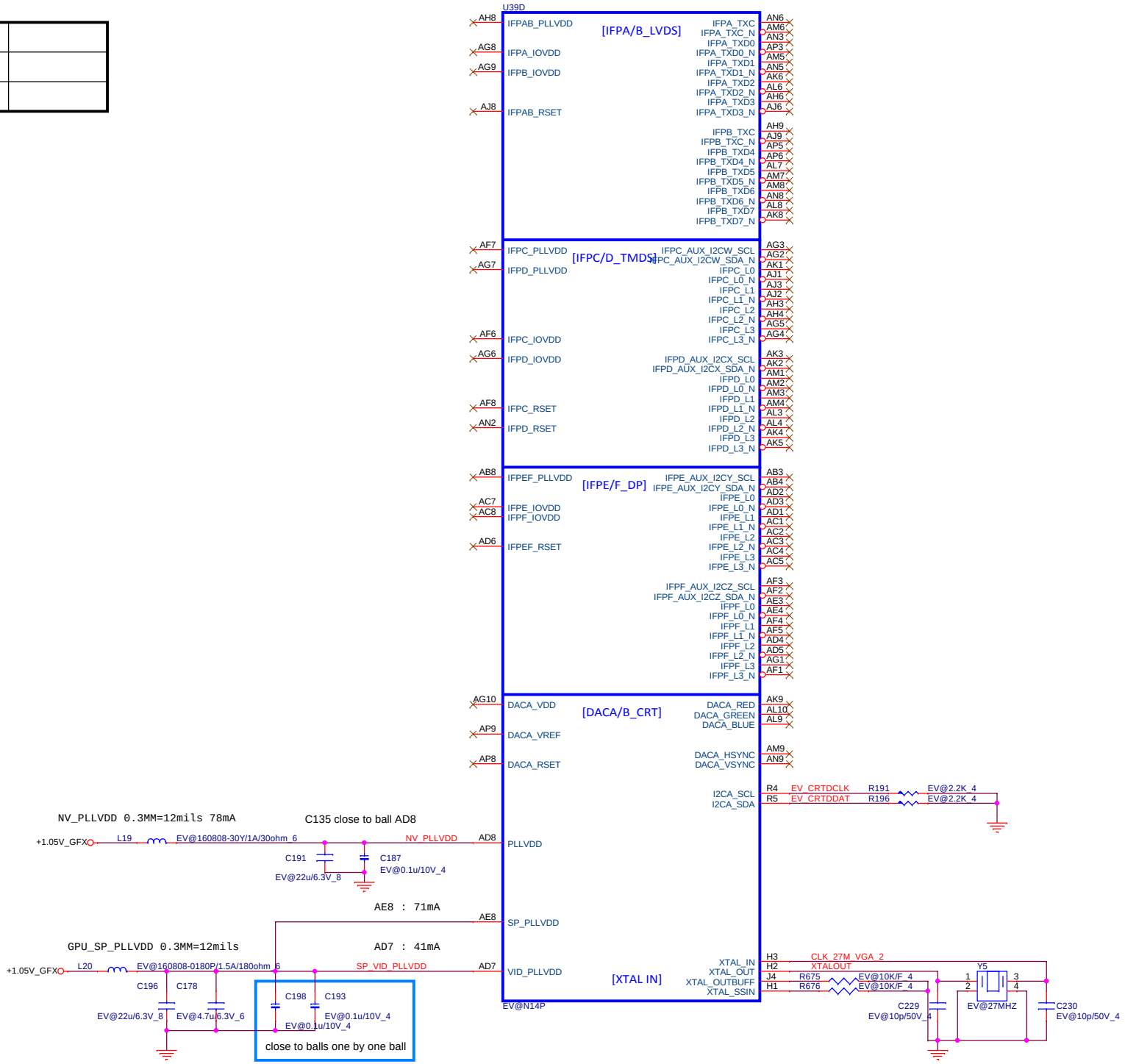
N14P-GV2	
N14P-GT	



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N14P-GV2	
N14P-GT	

A.ROM_SI - MEMORY STRAP
B.ROM_SO - 5K pull high

D.STRAP 0 - 45k pull high
E.STRAP 1 - 5K pull down
F.STRAP 3 - 5k pull down

C1.For N14P-GT sku
N14P-GT device ID=0x0FE4
1.ROM_SCLK =15K pull down
2.STRAP2 =25K pull down
3.STRAP4 = 45k pull down

C.For N14P-GV2 sku
N14P-GV2 QS device ID=0x1292
1.ROM_SCLK =5K pull high
2.STRAP2= 15k pull down
3.STRAP4=45 pull down
//For N14P-GV2 QS

N14P-GV2 ES device ID=0x12AD
1.ROM_SCLK =15K pull down
2.STRAP2= 30k pull high
3.STRAP4=10K pull down
//For N14P-GV2 ES

Logical Strap Bit Mapping

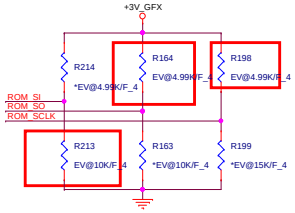
	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

STRAP3
Optimus ---> 4.99k PD
Discrete only ---> 15K PD

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K---> CS32492FB16
30.1K---> CS33012FB18
34.8K---> CS33482FB22
45.3K---> CS34532FB18

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0000
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0100
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX SPEED	DP_PLL_VDD33	0111

	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P_GV	L_10K	H_4.99K	H_4.99K	H_45.3K	L_45.3K	L_15K	L_4.99K	L_45.3K
N14P_GE	L_10K	L_10K	L_10K	H_10K	H_10K	L_10K	L_10K	L_10K
N14P_GT	L_10K	H_4.99K	L_15K	H_45.3K	L_4.99K	L_24.9K	L_4.99K	L_45.3K



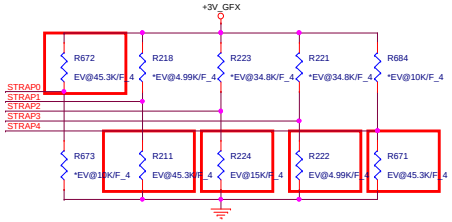
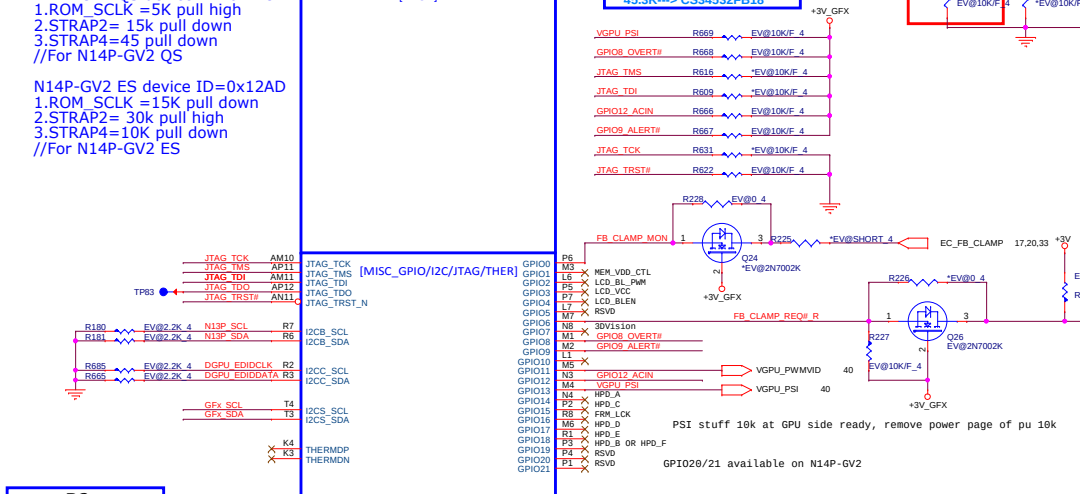


Table 9. N14P-GV/GT/GS/LP/GE GDDR5 Recommended Memories
128Mx16 Configuration

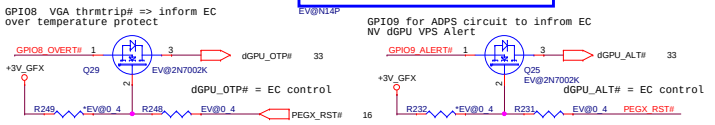
Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x4	1.5 V/ 1.5 V	H5GQ2H24AFR-T2C	2500	N/A	Production Candidate
		0x6	1.35V/ 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production Candidate
	Samsung	0x5	1.5 V/ 1.5 V	K4G20325FD-FC04	2500	1219	Production Candidate
		0x7	1.35V/ 1.35V	K4G20325FD-FC04	2000	1219	Production Candidate

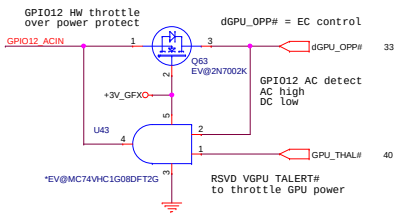
Vendor	P/N	Mfr. P/N	ROM_SI
Hynix	AKG5MWUTW13	H5GQ2H24AFR-T2C	0100
Samsung		K4G20325FD-FC04	0101

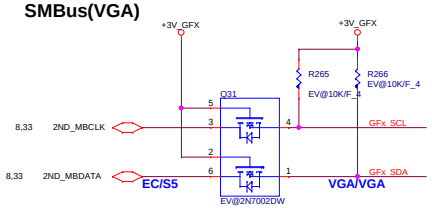


R3	
N14x others	40.2K
N14M-GE/GL	NC

R3
R674 EV@40.2K/F_4







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N14P-GV2	
N14P-GT	

LAYOUT NOTES:
UNDAER: WITHIN 150MILS
NEAR: WITHIN 1378MILS

+VGACORE

U39F [GPU VDD] EV@N14P

AA12	VDD_001	XVDD_001	U1
AA14	VDD_002	XVDD_002	U2
AA16	VDD_003	XVDD_003	U3
AA19	VDD_004	XVDD_004	U4
AA21	VDD_005	XVDD_005	U5
AA23	VDD_006	XVDD_006	U6
AB13	VDD_007	XVDD_007	U7
AB15	VDD_008	XVDD_008	U8
AB17	VDD_009	XVDD_009	V1
AB18	VDD_010	XVDD_010	V2
AB20	VDD_011	XVDD_011	V3
AB22	VDD_012	XVDD_012	V4
AC12	VDD_013	XVDD_013	V5
AC14	VDD_014	XVDD_014	V6
AC16	VDD_015	XVDD_015	V7
AC19	VDD_016	XVDD_016	V8
AC21	VDD_017	XVDD_017	W2
AC23	VDD_018	XVDD_018	W3
M12	VDD_019	XVDD_019	W4
M14	VDD_020	XVDD_020	W5
M16	VDD_021	XVDD_021	W7
M19	VDD_022	XVDD_022	W8
M21	VDD_023	XVDD_023	Y1
M23	VDD_024	XVDD_024	Y2
N13	VDD_025	XVDD_025	Y3
N15	VDD_026	XVDD_026	Y4
N17	VDD_027	XVDD_027	Y5
N18	VDD_028	XVDD_028	Y6
N20	VDD_029	XVDD_029	Y7
N22	VDD_030	XVDD_030	Y8
P12	VDD_031	XVDD_031	AA1
P14	VDD_032	XVDD_032	AA2
P16	VDD_033	XVDD_033	AA3
P19	VDD_034	XVDD_034	AA4
P21	VDD_035	XVDD_035	AA5
P23	VDD_036	XVDD_036	AA6
R13	VDD_037	XVDD_037	AA7
R15	VDD_038	XVDD_038	AA8
R17	VDD_039		
R18	VDD_040		
R20	VDD_041		
R22	VDD_042		
T12	VDD_043		
T14	VDD_044		
T16	VDD_045		
T19	VDD_046		
T21	VDD_047		
T23	VDD_048		
U13	VDD_049		
U15	VDD_050		
U17	VDD_051		
U18	VDD_052		
U20	VDD_053		
U22	VDD_054		
V13	VDD_055		
V15	VDD_056		
V17	VDD_057		
V18	VDD_058		
V20	VDD_059		
V22	VDD_060		
W12	VDD_061		
W14	VDD_062		
W16	VDD_063		
W19	VDD_064		
W21	VDD_065		
W23	VDD_066		
Y13	VDD_067		
Y15	VDD_068		
Y18	VDD_069		
Y17	VDD_070		
Y20	VDD_071		
Y22	VDD_072		

U39G [GPU GND] EV@N14P

A2	GND_1	GND_101	D2
AA17	GND_2	GND_102	D31
AA18	GND_3	GND_103	D33
AA20	GND_4	GND_104	E10
AA22	GND_5	GND_105	E22
AB12	GND_6	GND_106	E25
AB14	GND_7	GND_107	E5
AB16	GND_8	GND_108	E7
AB19	GND_9	GND_109	F28
AB2	GND_10	GND_110	F7
AB21	GND_11	GND_111	G10
A33	GND_12	GND_112	G13
AB23	GND_13	GND_113	G16
AB28	GND_14	GND_114	G19
AB30	GND_15	GND_115	G2
AB32	GND_16	GND_116	G22
AB5	GND_17	GND_117	G25
AB7	GND_18	GND_118	G28
AC13	GND_19	GND_119	G3
AC15	GND_20	GND_120	G30
AC17	GND_21	GND_121	G32
AC18	GND_22	GND_122	G33
AA13	GND_23	GND_123	G5
AC20	GND_24	GND_124	G7
AC22	GND_25	GND_125	K2
AE2	GND_26	GND_126	K28
AE28	GND_27	GND_127	K30
AE30	GND_28	GND_128	K32
AE32	GND_29	GND_129	K33
AE33	GND_30	GND_130	K5
AE5	GND_31	GND_131	K7
AE7	GND_32	GND_132	M13
AH10	GND_33	GND_133	M15
AA15	GND_34	GND_134	M17
AH13	GND_35	GND_135	M18
AH16	GND_36	GND_136	M20
AH19	GND_37	GND_137	M22
AH2	GND_38	GND_138	N12
AH22	GND_39	GND_139	N14
AH24	GND_40	GND_140	N16
AH28	GND_41	GND_141	N19
AH29	GND_42	GND_142	N2
AH30	GND_43	GND_143	N21
AH32	GND_44	GND_144	N23
AH33	GND_45	GND_145	N28
AH5	GND_46	GND_146	N30
AH7	GND_47	GND_147	N32
AJ7	GND_48	GND_148	N33
AK10	GND_49	GND_149	N5
AK7	GND_50	GND_150	N7
AL12	GND_51	GND_151	P13
AL14	GND_52	GND_152	P15
AL15	GND_53	GND_153	P17
AL17	GND_54	GND_154	P18
AL18	GND_55	GND_155	P20
AL2	GND_56	GND_156	P22
AL20	GND_57	GND_157	R12
AL21	GND_58	GND_158	R14
AL23	GND_59	GND_159	R16
AL24	GND_60	GND_160	R19
AL26	GND_61	GND_161	R21
AL28	GND_62	GND_162	R23
AL30	GND_63	GND_163	T13
AL32	GND_64	GND_164	T15
AL33	GND_65	GND_165	T17
AL5	GND_66	GND_166	T18
AM13	GND_67	GND_167	T2
AM16	GND_68	GND_168	T20
AM19	GND_69	GND_169	T22
AM22	GND_70	GND_170	AG11
AM25	GND_71	GND_171	T28
AN1	GND_72	GND_172	T32
AN10	GND_73	GND_173	T5
AN13	GND_74	GND_174	T7
AN16	GND_75	GND_175	U12
AN19	GND_76	GND_176	U14
AN22	GND_77	GND_177	U16
AN25	GND_78	GND_178	U19
AN30	GND_79	GND_179	U21
AN34	GND_80	GND_180	U23
AN4	GND_81	GND_181	V12
AN7	GND_82	GND_182	V14
AP2	GND_83	GND_183	V16
AP33	GND_84	GND_184	V19
B1	GND_85	GND_185	V21
B10	GND_86	GND_186	V23
B22	GND_87	GND_187	W13
B25	GND_88	GND_188	W15
B28	GND_89	GND_189	W17
B31	GND_90	GND_190	W18
B34	GND_91	GND_191	W20
B4	GND_92	GND_192	W22
B7	GND_93	GND_193	W28
C10	GND_94	GND_194	Y12
C13	GND_95	GND_195	Y14
C19	GND_96	GND_196	Y16
C22	GND_97	GND_197	Y19
C25	GND_98	GND_198	Y21
C28	GND_99	GND_199	Y23
C7	GND_100	GND_200	AH11
		GND_OPT_1	C16
		GND_OPT_2	W32

+VGACORE

0.1uF x 8 population x 4

C116 EV@0.1u/10V_4
C117 EV@0.1u/10V_4
C140 EV@0.1u/10V_4
C102 EV@0.1u/10V_4
C136 *EV@0.1u/10V_4
C137 *EV@0.1u/10V_4
C126 *EV@0.1u/10V_4
C114 *EV@0.1u/10V_4

PLACE UNDER GPU BALLS

+VGACORE

C127 EV@4.7u/6.3V_6
C150 EV@4.7u/6.3V_6
C122 EV@4.7u/6.3V_6
C105 EV@4.7u/6.3V_6
C151 EV@4.7u/6.3V_6
C152 EV@4.7u/6.3V_6
C93 EV@4.7u/6.3V_6
C111 EV@4.7u/6.3V_6

4.7uF x 15 population x10

C125 EV@4.7u/6.3V_6
C138 EV@4.7u/6.3V_6
C180 *EV@4.7u/6.3V_6
C200 *EV@4.7u/6.3V_6
C160 *EV@4.7u/6.3V_6
C101 *EV@4.7u/6.3V_6
C124 *EV@4.7u/6.3V_6

PLACE NEAR GPU

+VGACORE

47u x1 22u x7 stuff x 1 4.7u x6 stuff x 5 330u x1 RSVD by DG

C637 EV@330u/2V_7343
C154 EV@47u/6.3V_8
C139 EV@22u/6.3V_8
C156 EV@4.7u/25V_8
C97 EV@4.7u/25V_8
C144 EV@4.7u/25V_8
C106 EV@4.7u/25V_8
C92 EV@4.7u/25V_8

0817 RSVD more NVVDD caps by NV DG

C186 *EV@22u/6.3V_8
C219 *EV@22u/6.3V_8
C91 *EV@22u/6.3V_8
C179 *EV@22u/6.3V_8
C214 *EV@22u/6.3V_8
C199 *EV@22u/6.3V_8
C113 *EV@4.7u/25V_8

+1.05V_GFX R85 EV@4.7K_4 DGPU_POK4 2 C64 *EV@1000p/50V_4
+1.5V_GFX R86 EV@4.7K_4 DGPU_POK2 2 C65 *EV@1000p/50V_4

DGPU_PGOK-1
Q12 EV@MMBT3904-7-F
DGPU_POK_O
R72 *EV@0_4
Q13 EV@MMBT3904-7-F

+3V
R82 EV@4.7K_4
C51 EV@1000p/50V_4

+3V_GFX
R84 EV@4.7K_4
Q11 EV@DTC144EU
R83 EV@100K/F_4
DGPU_PWROK 10
PWRGD connect to PCH

for meet Power down sequence
for +3V_GFX

+VGACORE D14 EV@RB500V-40
+1.5V_GFX D13 *EV@RB500V-40
+3V_GFX

No stuff when GC6 support.

HWPG_1.5VGFX for DDR=1.5V

+3V_GFX
+3V
R156 EV@4.7K_4
R142 EV@10K_4
HWPG_1.5VGFX
DGPU_POK_O
R155 EV@100K/F_4
C157 EV@1000p/50V_4
Q22 EV@DTC144EUA
10/15 reserve
DDR=1.5V ,This block POP

+3V
C568 *EV@0.1u/10V_4
PU at VR
41 HWPG_1.5VGFX
VGPU_PWRGD
PU at VR
U36 EV@MC74VHC1G08DFT2G
+1.05V_GFX_enable, PD at VR
1.05V_GFX_EN 41
R548 *EV@0_4

GC6 need system 3V to control FBVDDQ

+3V
C559 EV@0.1u/10V_4
PD at GPU
41 FBVDDQ_EN
R527 EV@100K_4
U35 EV@SN74AHC1G32DCKR
EC_FB_CLAMP 17,19,33
VGPU_PWRGD_R
R552 EV@0_4
R554 *EV@0_4
C571 *EV@0.1u/10V_4
VGPU_PWRGD 40
VGPU_EN 8,40
PU at VR

Quanta Computer Inc.			
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Size	Document Number		Rev
	DGPU 5/5 (Power/Ground)		3A
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CHANNEL A: 1024MB DDR3X16

17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]

VRAM6 / VRAM10 / VRAM5 / VRAM9 — 96-BALL SDRAM DDR3, EV@VRAM _DDR3

Should be 240 Ohms +-1%

R67 EV@243/F_4 (VRAM6)
R469 EV@243/F_4 (VRAM10)
R465 EV@243/F_4 (VRAM5)
R505 EV@243/F_4 (VRAM9)

+1.5V_GFX

R468 EV@162/F_4 (VMA_CLK0 / VMA_CLK0#)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R5 EV@1.33K/F_4 — VREFC_VMA1 — R6 EV@1.33K/F_4 — C19 EV@0.1u/10V_4
R13 EV@1.33K/F_4 — VREFD_VMA1 — R14 EV@1.33K/F_4 — C9 EV@0.1u/10V_4

17 FBA_CMD17 — FBA_CMD17 — TP8
17 FBA_CMD1 — FBA_CMD1 — TP7
10/14 modify

R467 EV@162/F_4 (VMA_CLK1 / VMA_CLK1#)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R12 EV@1.33K/F_4 — VREFC_VMA3 — R11 EV@1.33K/F_4 — C8 EV@0.1u/10V_4
R10 EV@1.33K/F_4 — VREFD_VMA3 — R9 EV@1.33K/F_4 — C7 EV@0.1u/10V_4

+1.5V_GFX decoupling: C520 C513 C508 C512 EV@1u/10V_4; C16 C515 C516 C14 C23 C10 EV@1u/10V_4; C18 C11 C510 C505 C13 C504 C6 C22 EV@1u/10V_4; C503 C502 C15 C17 C511 C12 C506 EV@0.1u/10V_4; C5 C501 EV@10u/6.3V_6; C514 C509 C507 EV@0.1u/10V_4

Quanta Computer Inc.			
PROJECT : ZRQ			
Size	Document Number		Rev
	NN13P-LP DDR3 VRAM 1/2		3A
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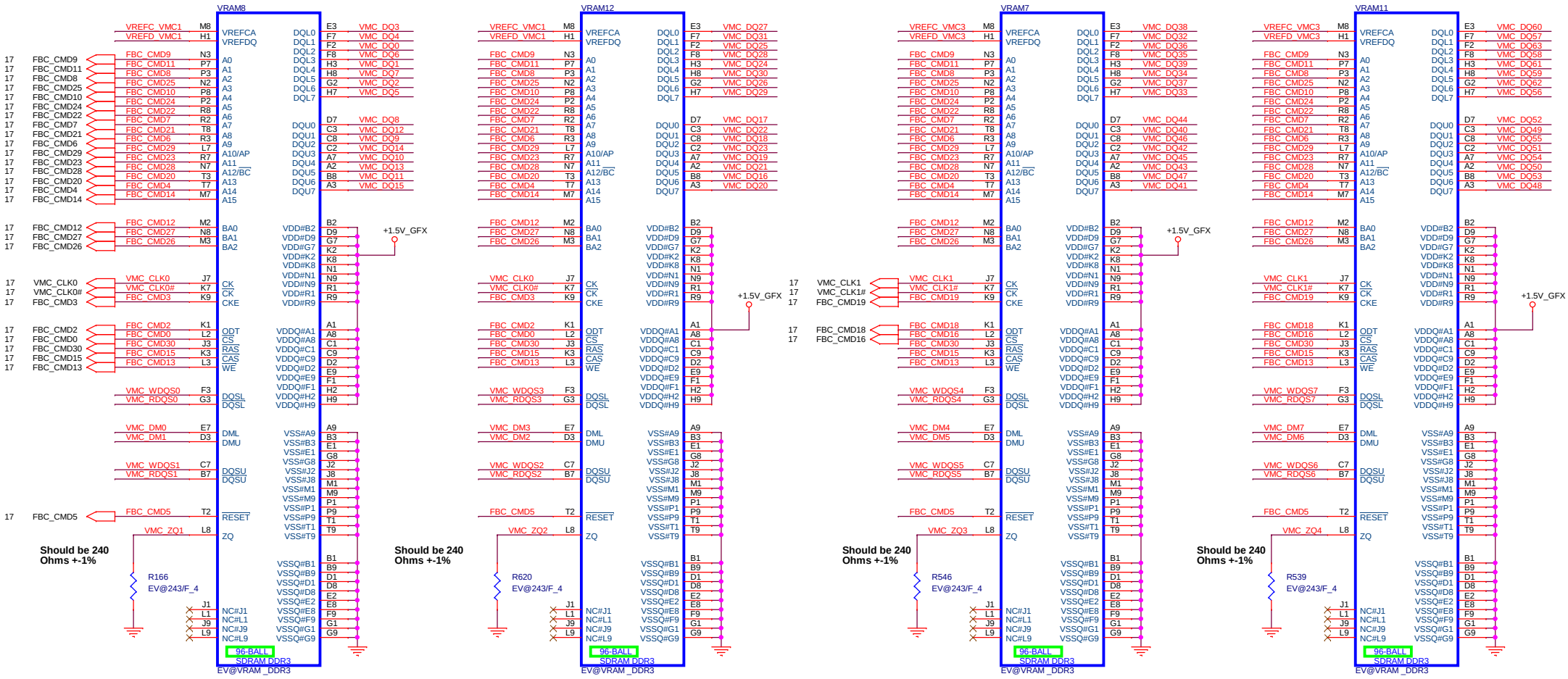
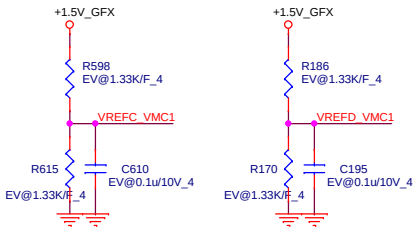
CHANNEL B: 1024MB DDR3X16

17 VMC_DQ[63..0]
17 VMC_DM[7..0]
17 VMC_WDQS[7..0]
17 VMC_RDQS[7..0]



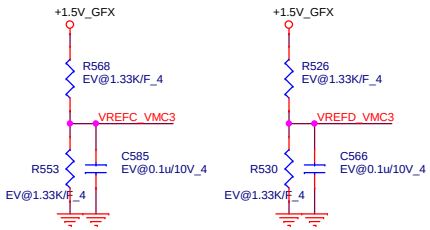
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

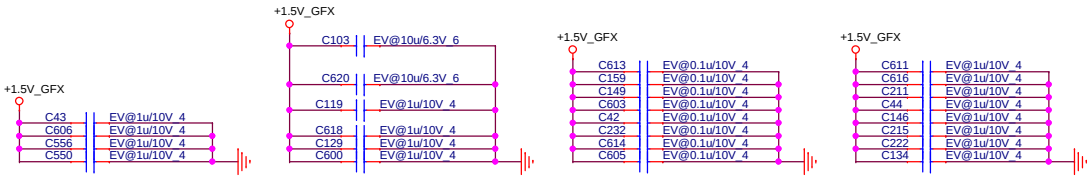
VMC_CLK0 — R632 EV@162/F_4 — VMC_CLK0#



Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

VMC_CLK1 — R96 EV@162/F_4 — VMC_CLK1#





17 FBC_CMD17 — FBC_CMD17 — TP14
17 FBC_CMD1 — FBC_CMD1 — TP18

Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	N13P-LP DDR3 VRAM 2/2	3A
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Mini DP ML (DPP)

Layout Notes:
Place near Pin13 and Pin14

SEL/OE# polarity Control

DP AUX

DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

Reserve by CRB

mDP connector

30mil
500mA (Max.)

For leakage from connector

Connect to HS_SEL_IN(pin12)
Connect to SS_SEL_IN(pin7)

Quanta Computer Inc.	
PROJECT : ZRQ	
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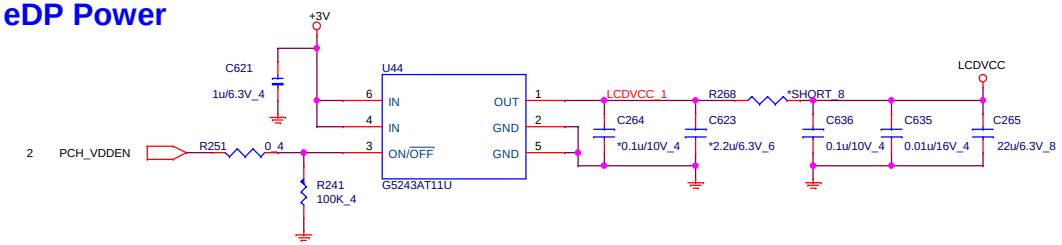
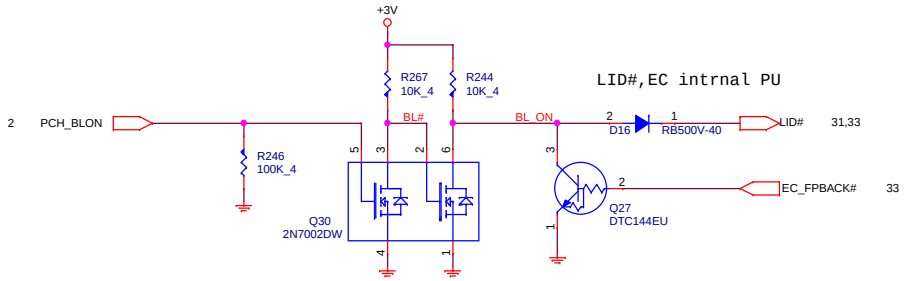
eDP Power

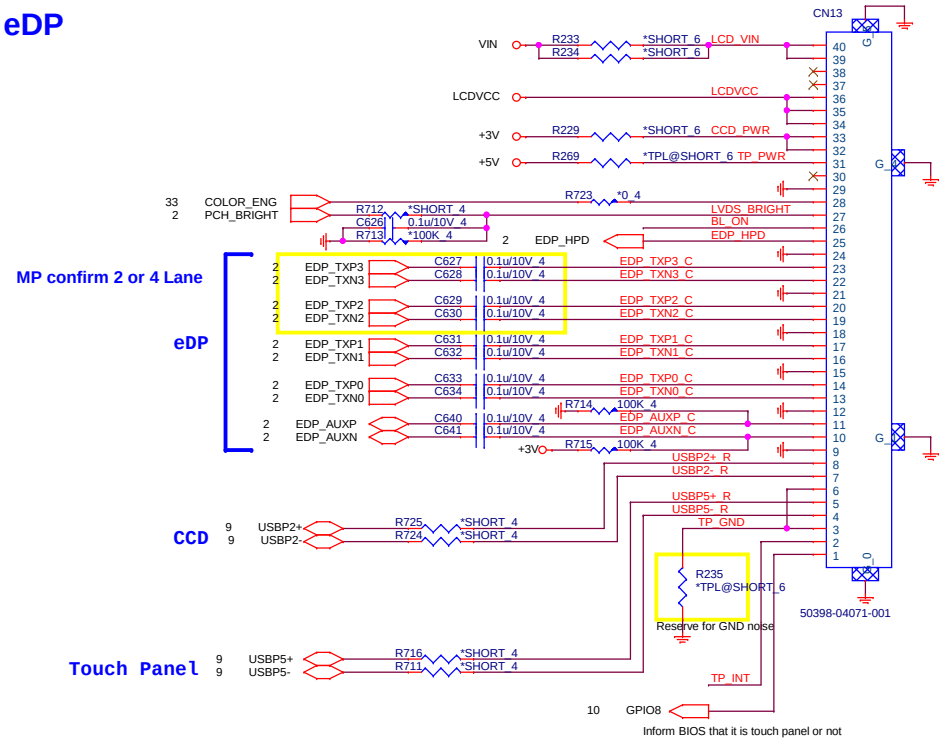


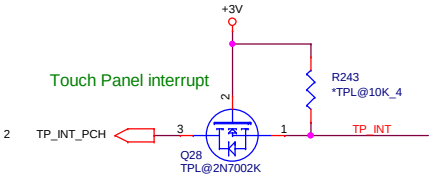
Backlight Control



Lid Switch (HSR)(move to USB/B)

eDP





Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	3A

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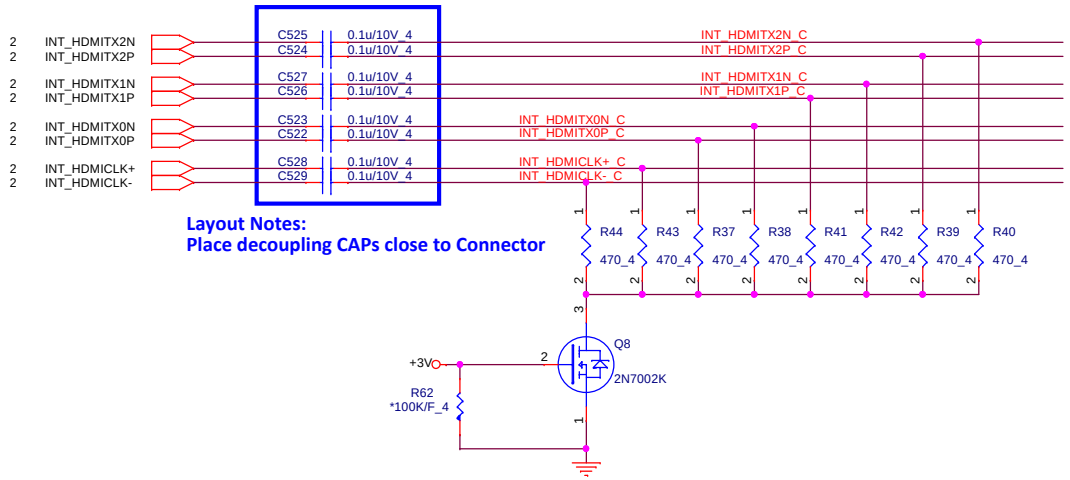
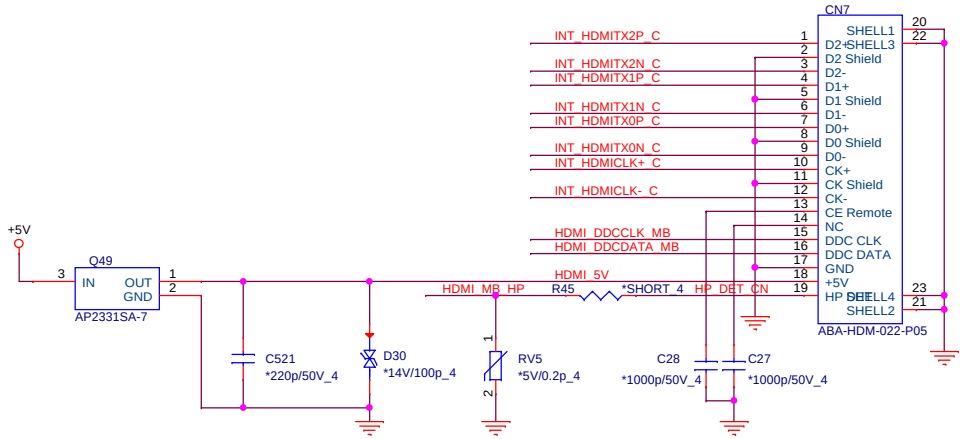
HDMI Cost Reduced level shift (HDM)

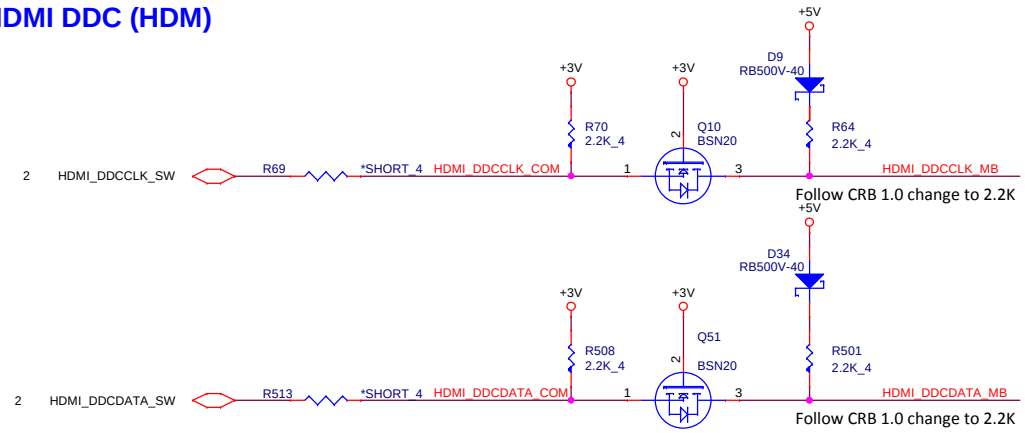


Layout Notes:
Place decoupling CAPs close to Connector

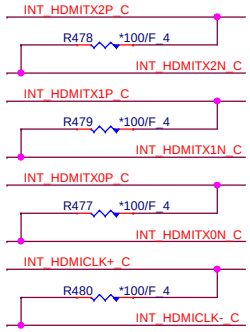
HDMI connector (HDM)



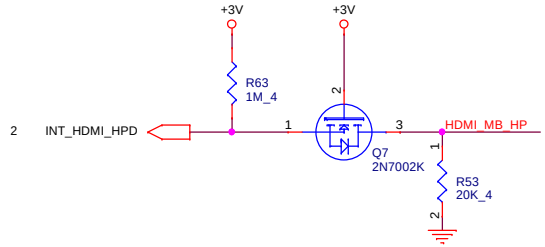
HDMI DDC (HDM)



EMI (EMC)



HDMI-detect (HDM)



Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	HDMI (PS8101)	3A

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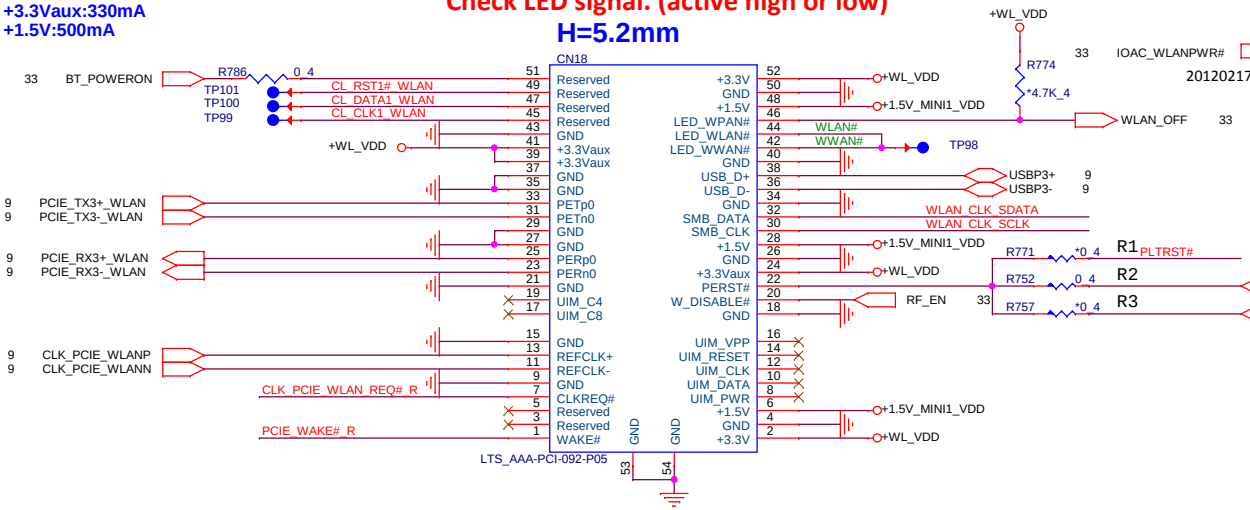
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)

H=5.2mm



+WL_VDD
R774 *4.7K_4
33 IOAC_WLANPWR#
WLAN_OFF 33

+3VPCU
Q65 AO3413
R740 *100K_4

20111122 change to PMOS

Low	Mini card +3V power enable
High	Mini card +3V power disable

20120217 reserve R648 PU 100k.

+3V_WLAN R749 *SHORT_8
+WL_VDD
C675 10u/6.3V_6
C665 0.1u/10V_4
C683 *0.1u/10V_4
C650 *0.1u/10V_4

R771 *0_4 R1 PLTRST#
R752 0_4 R2
R757 *0_4 R3
IOAC_RST# 28,33
PCIERST# 28,33

20120221 add R1 for PLTRST#.
20120216 add R2/R3 un-stuff for iRST reserve.

+1.5V_MINI1_VDD
+1.5V
500mA for +1.5V
R323 *0_8
C680 *1000p/50V_4
C668 *0.1u/10V_4
C653 *10u/6.3V_6

2011017 : stuff Q81 to enable wake function on WLAN for IOAC
check IOAC power rail can reduce Q81

LAYOUT NOTE:
CLOSE TO CONNECTOR

26

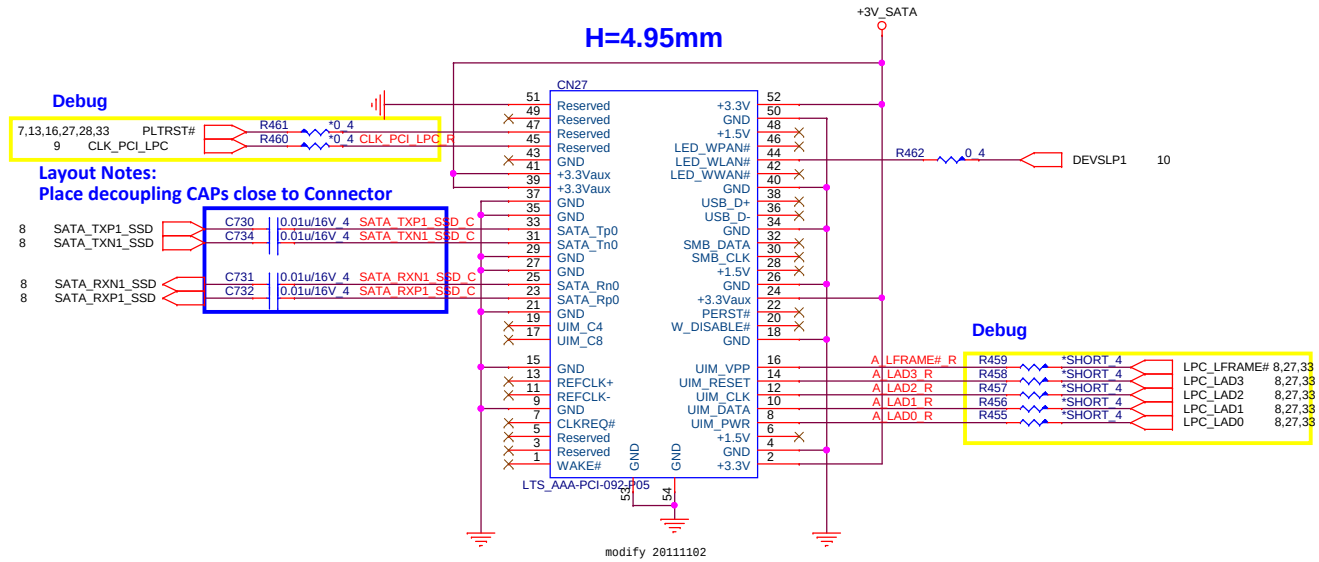
mSATA(MNC)

LAYOUT NOTE:
CLOSE TO CONNECTOR

rating = 1000mA @ 128G

+3V R452 *SHORT_8 +3V_SATA
C496 10u/6.3V_6
C500 0.1u/10V_4
C499 0.1u/10V_4

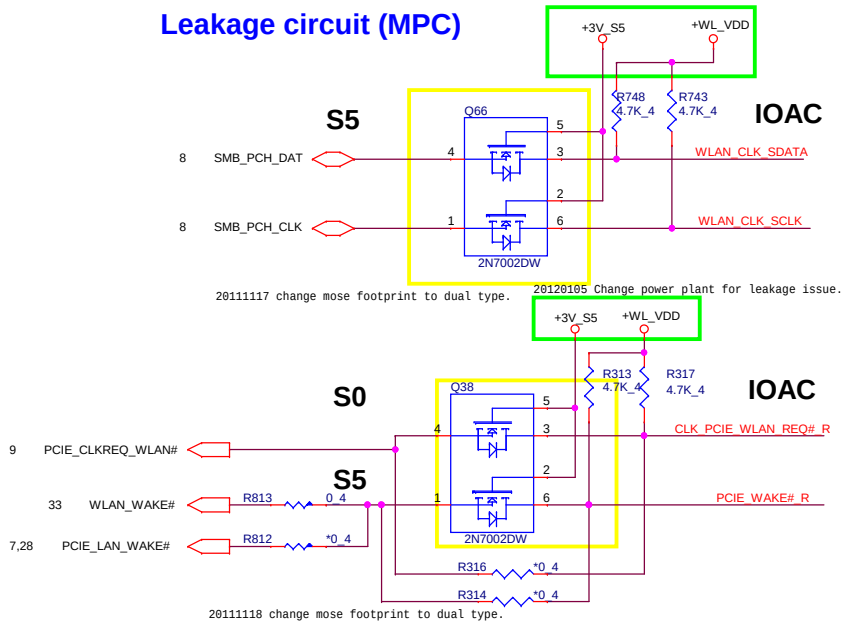
H=4.95mm



modify 20111102

20120105 Change power plant for leakage issue.

Leakage circuit (MPC)



Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	Mini Card/mSATA	3A

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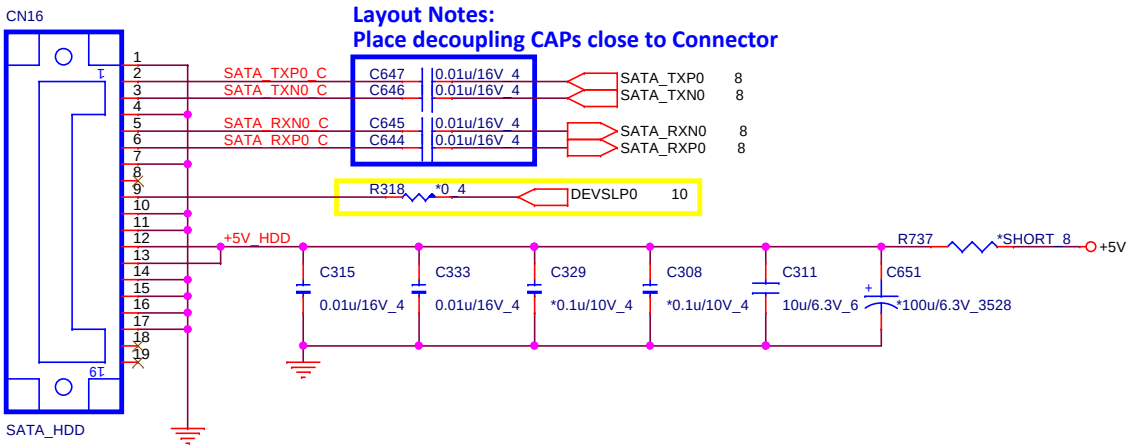
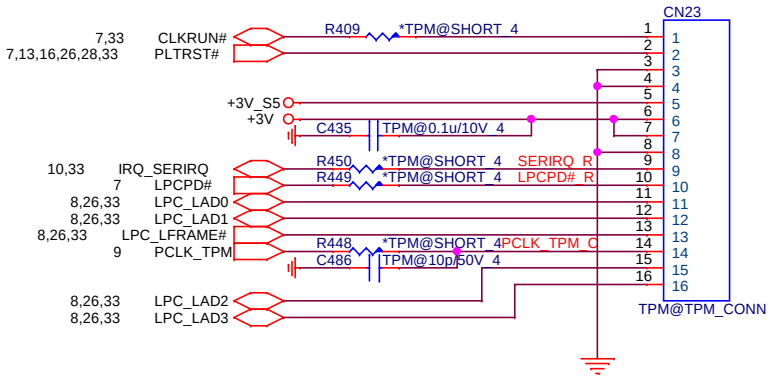
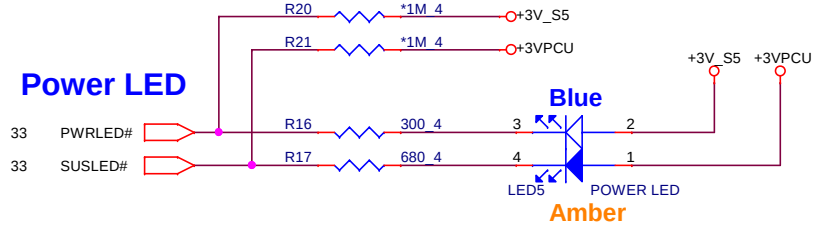
MAIN SATA HDD (HDD)

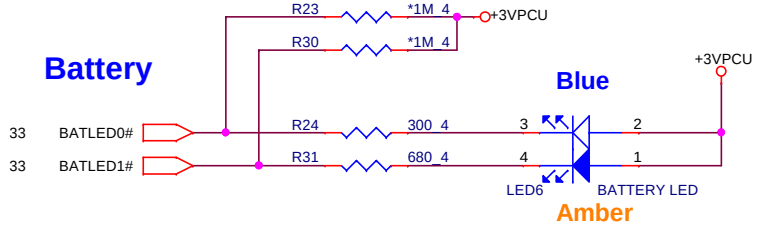


TPM (TPM)

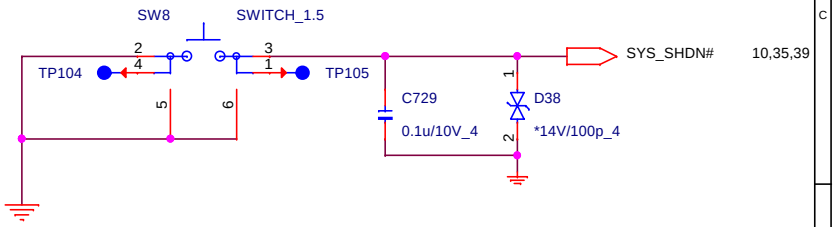


LED(UIF)





3/5VPCU reset switch (CLG)



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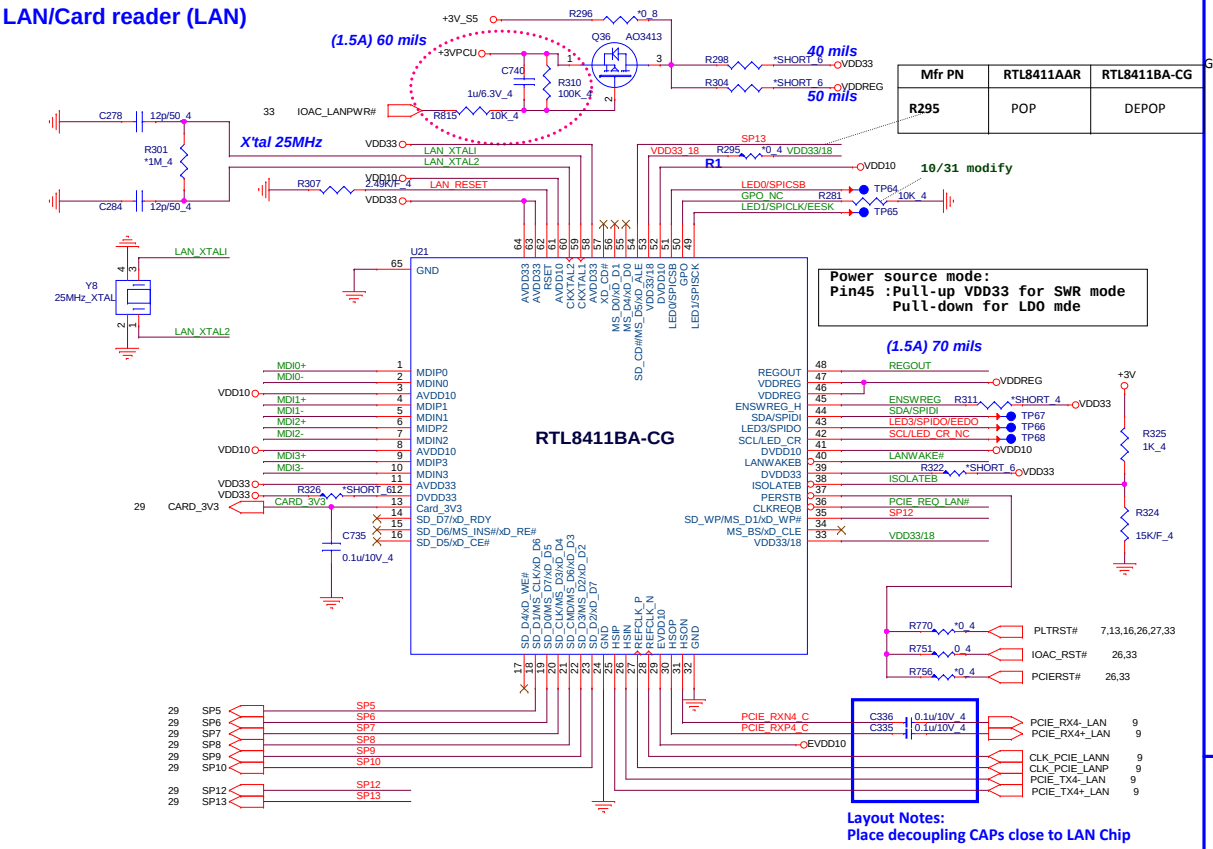
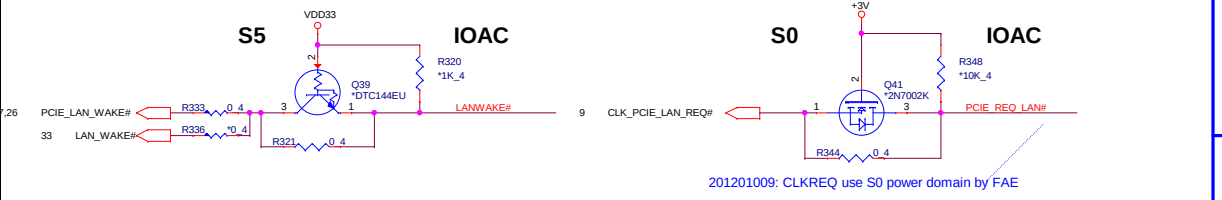
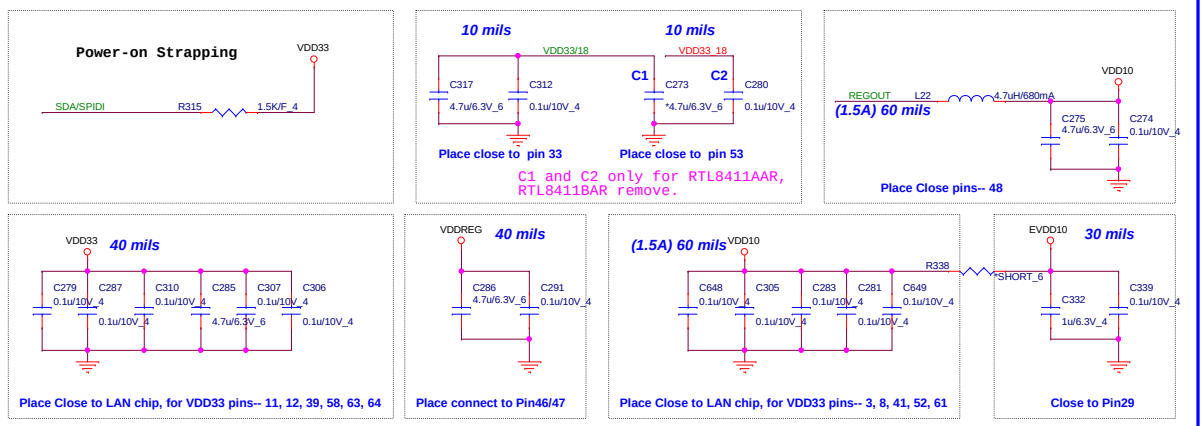
LAN/Card reader (LAN)



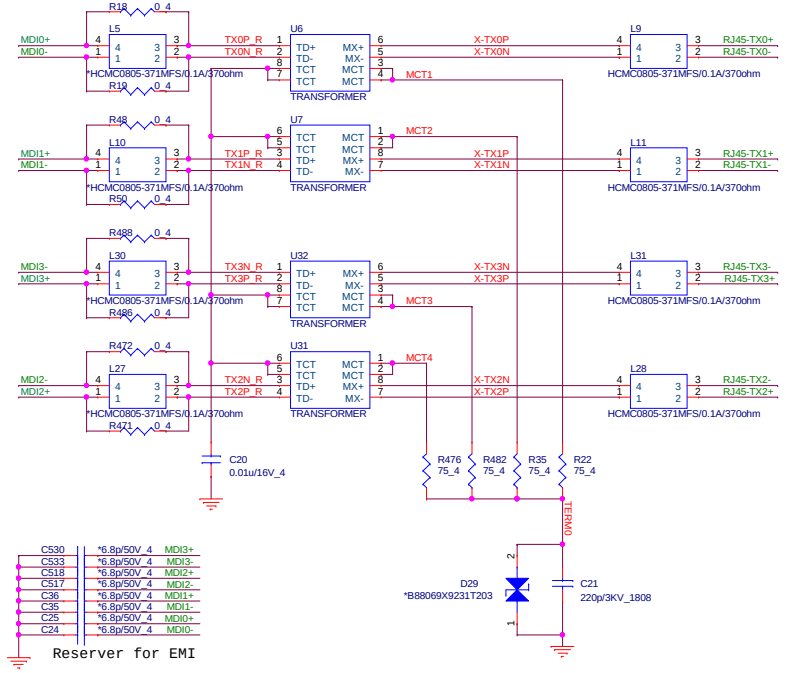
Mfr PN	RTL8411AAR	RTL8411BA-CG
R295	POP	DEPOP



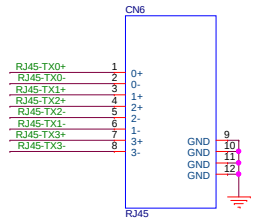


Transformer (LAN)

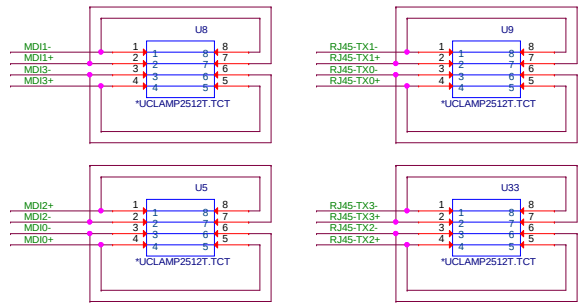
High GDDR5



RJ45 CONNECTOR (LAN)



SURGE (LAN)



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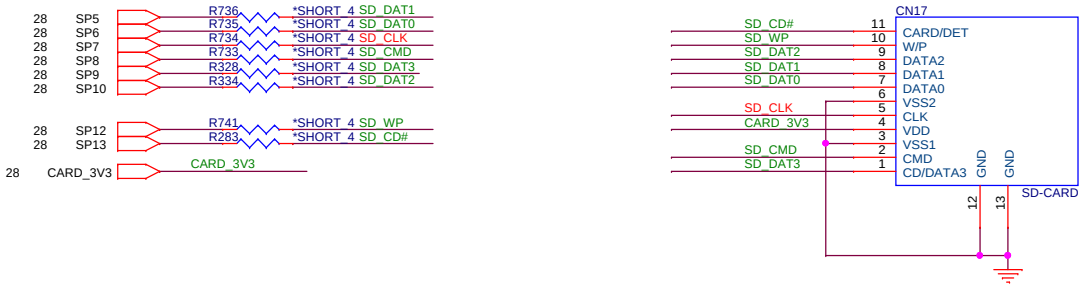
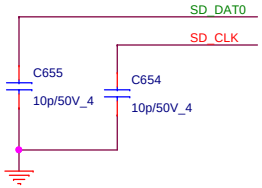
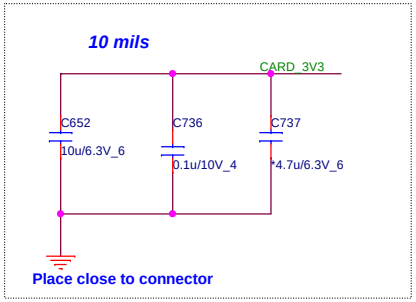
SD/MMC CARD READER CONNECTOR (MMC)



EMI

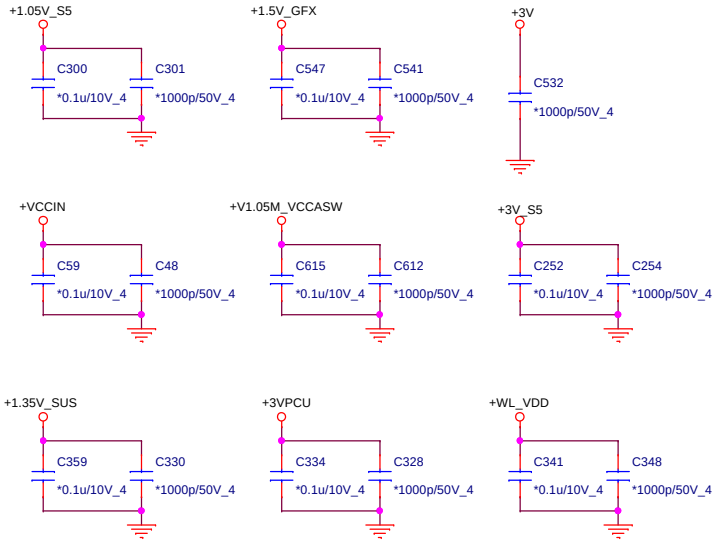




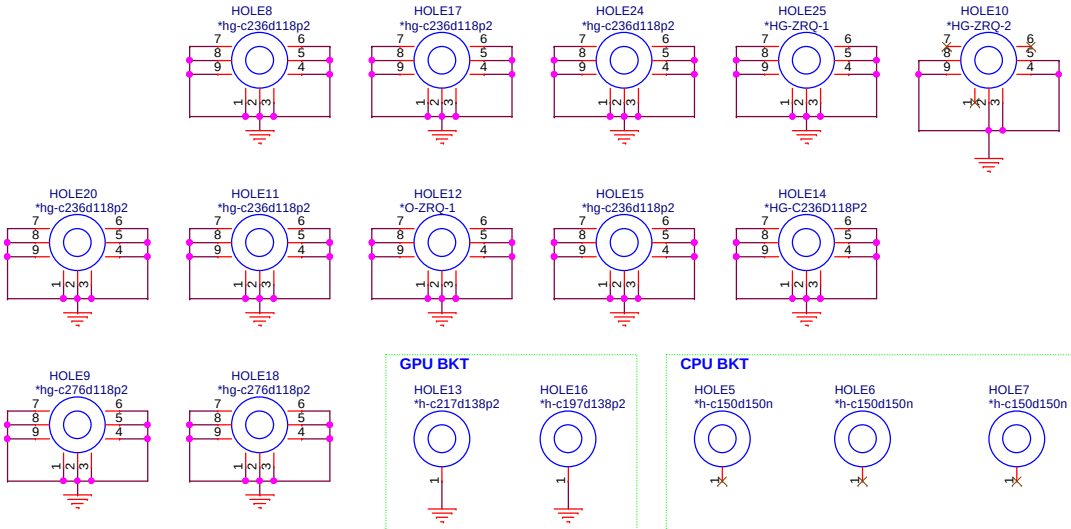
Share Pin

SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#

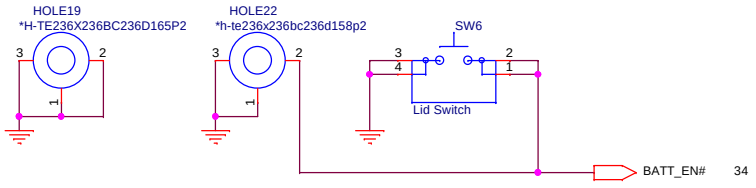
Stitching cap (EMC)

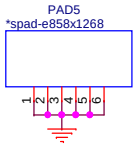


HOLE(OTH)



BATT Enable short pad





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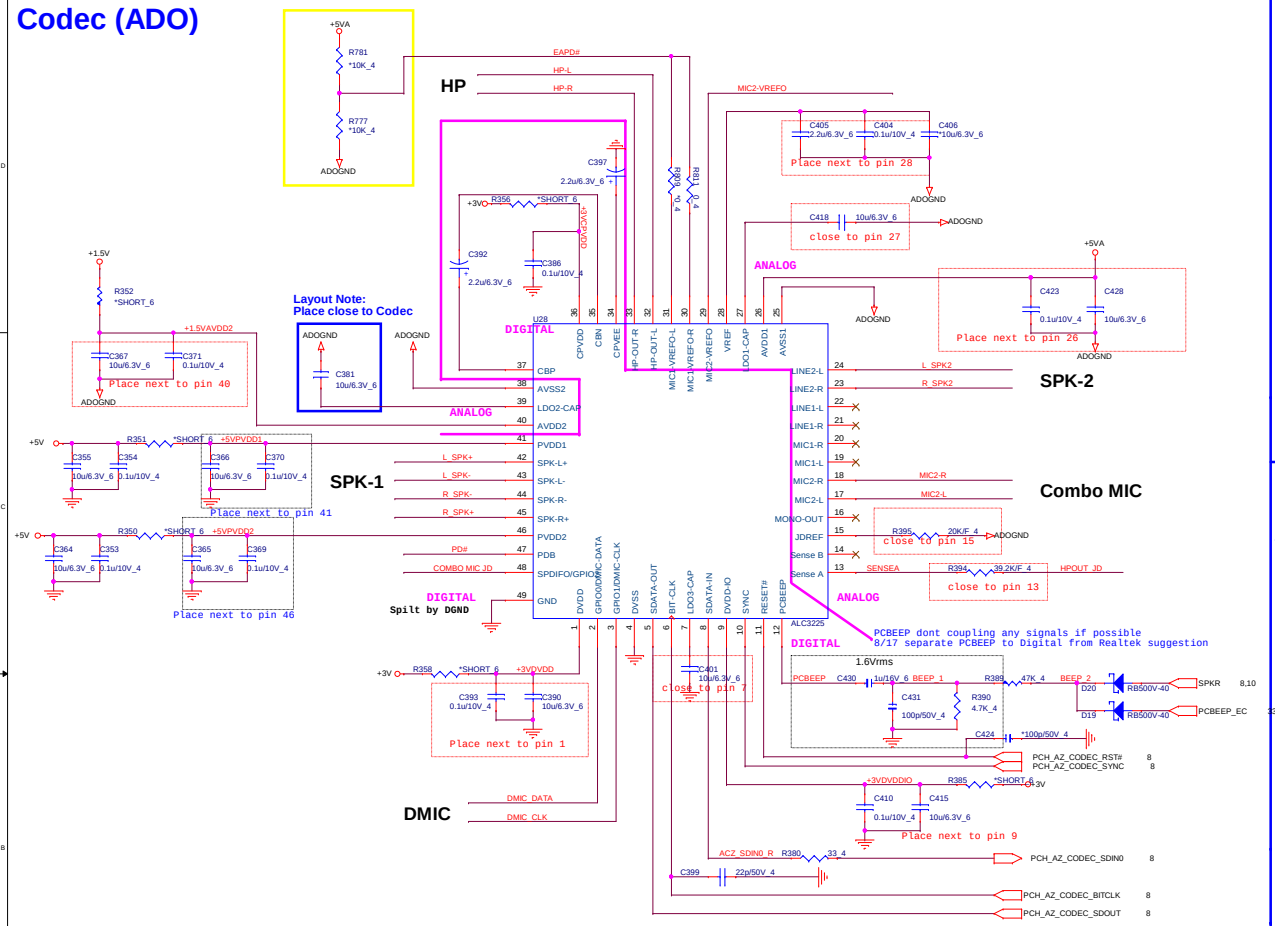
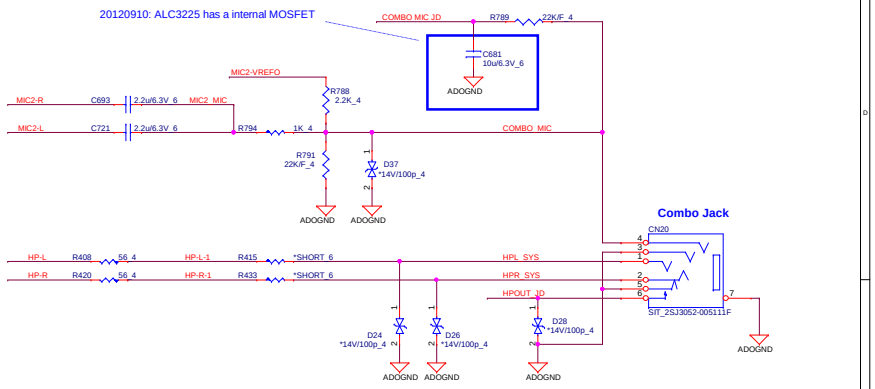
Codec (ADO)



HEADPHONE/Mic combo (AMP)

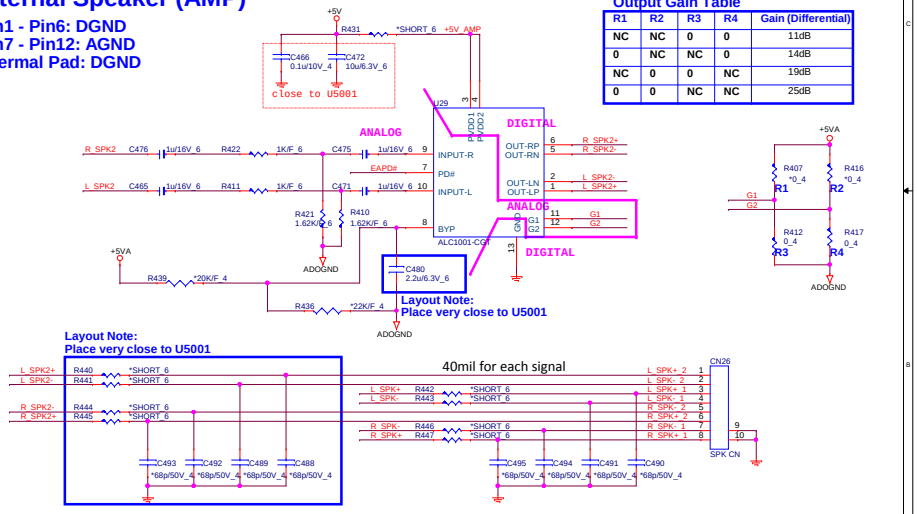


Internal Speaker (AMP)

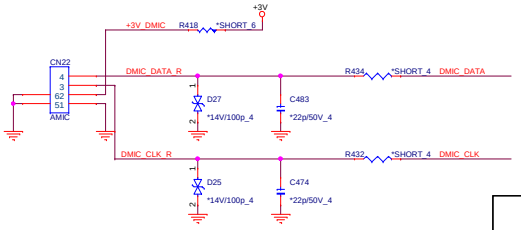
Pin1 - Pin6: DGND
Pin7 - Pin12: AGND
Thermal Pad: DGND

Output Gain Table

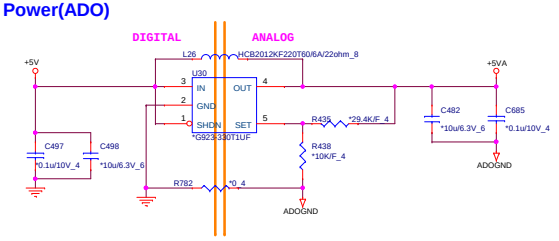
R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB



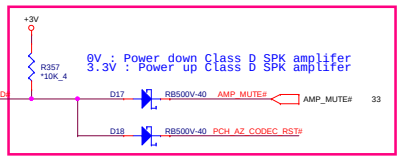
INT DMIC(AMP)



Power(ADO)



Mute(ADO)



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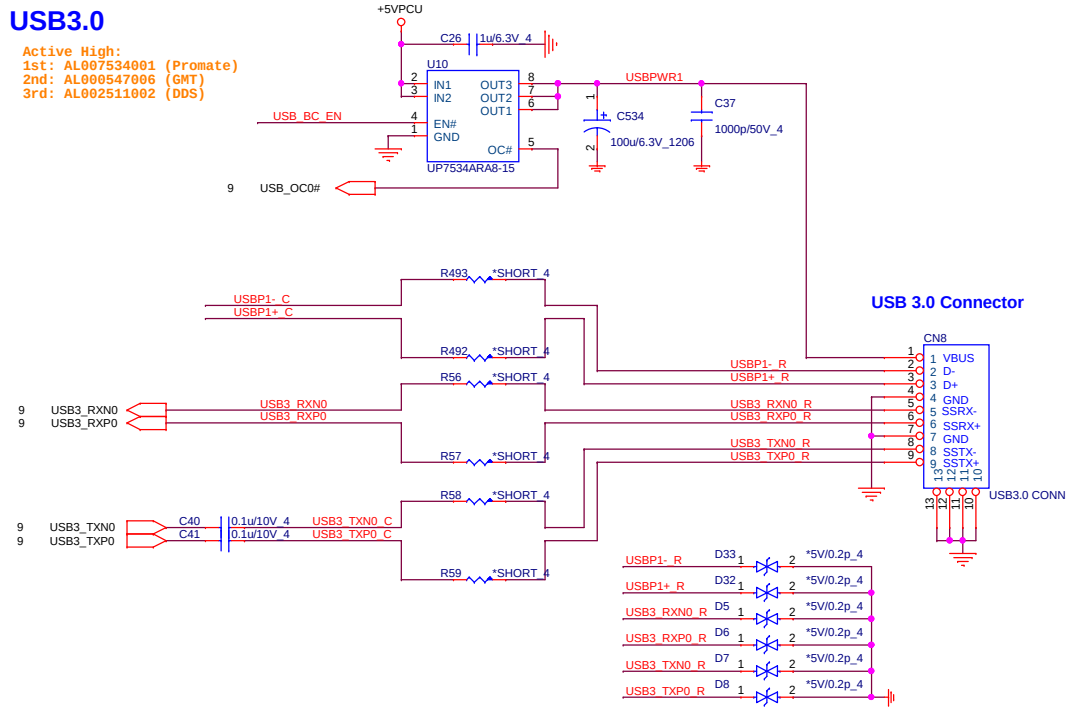
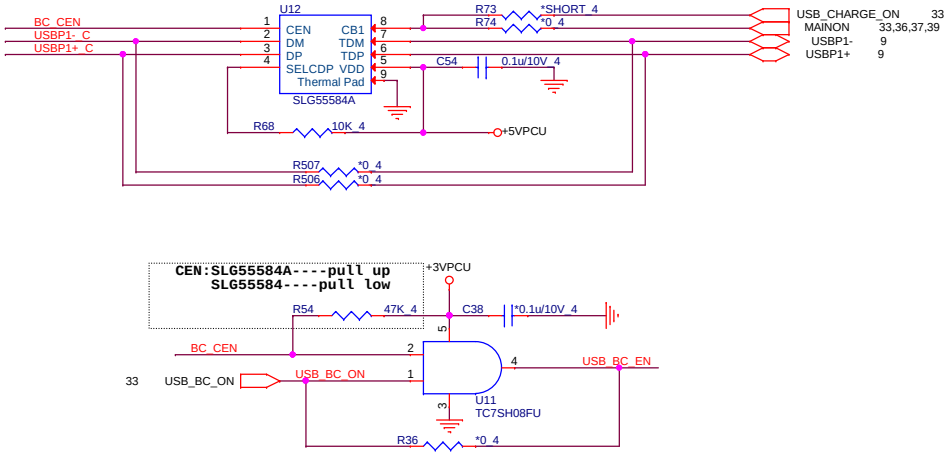
USB3.0

Active High:
1st: AL007534001 (Promate)
2nd: AL000547006 (GMT)
3rd: AL002511002 (DDS)

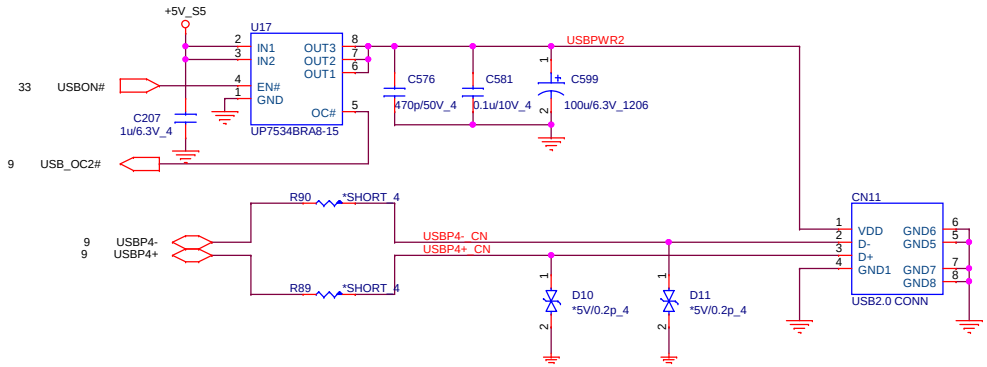


USB Charger to 3.0

CB	SELCDP	Funcion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

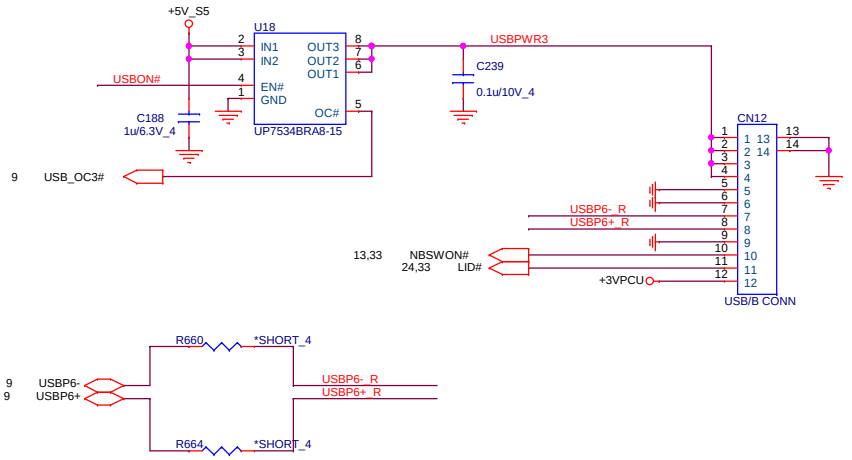


USB2.0



I/O board

1st source: AL007534000
2ns source: AL082025000



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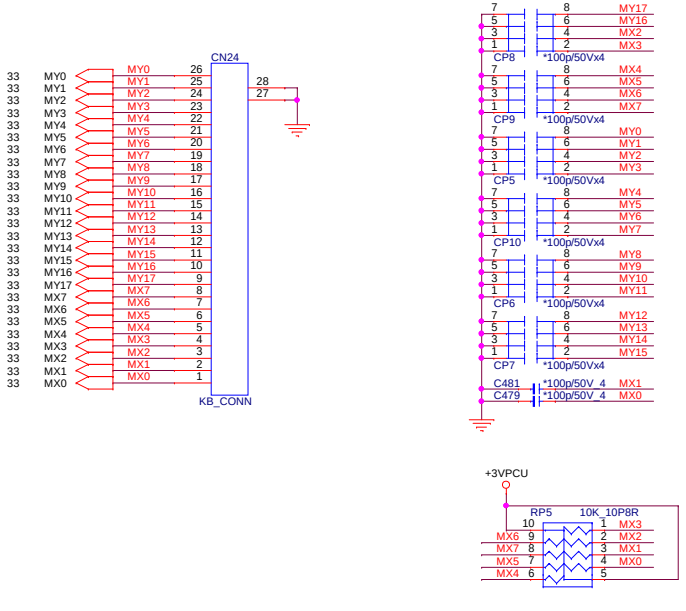
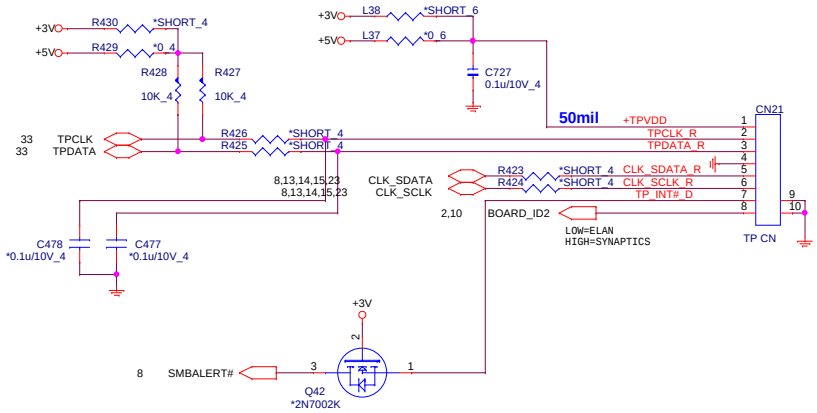
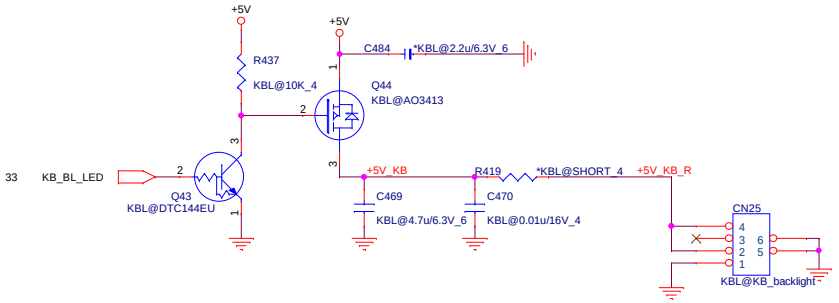
K/B (KBC)



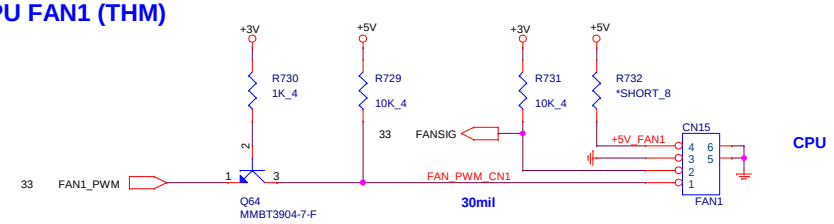
TOUCHPAD BOARD CONN (TPD)



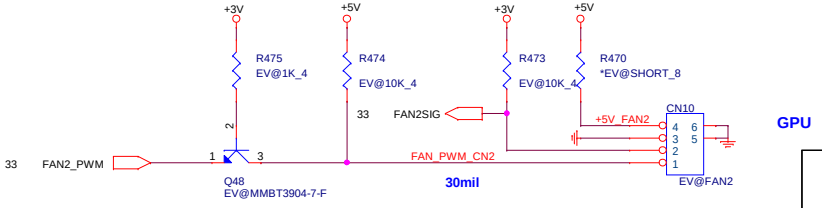
KB_BL LED (KBC)



CPU FAN1 (THM)



CPU FAN2 (THM)



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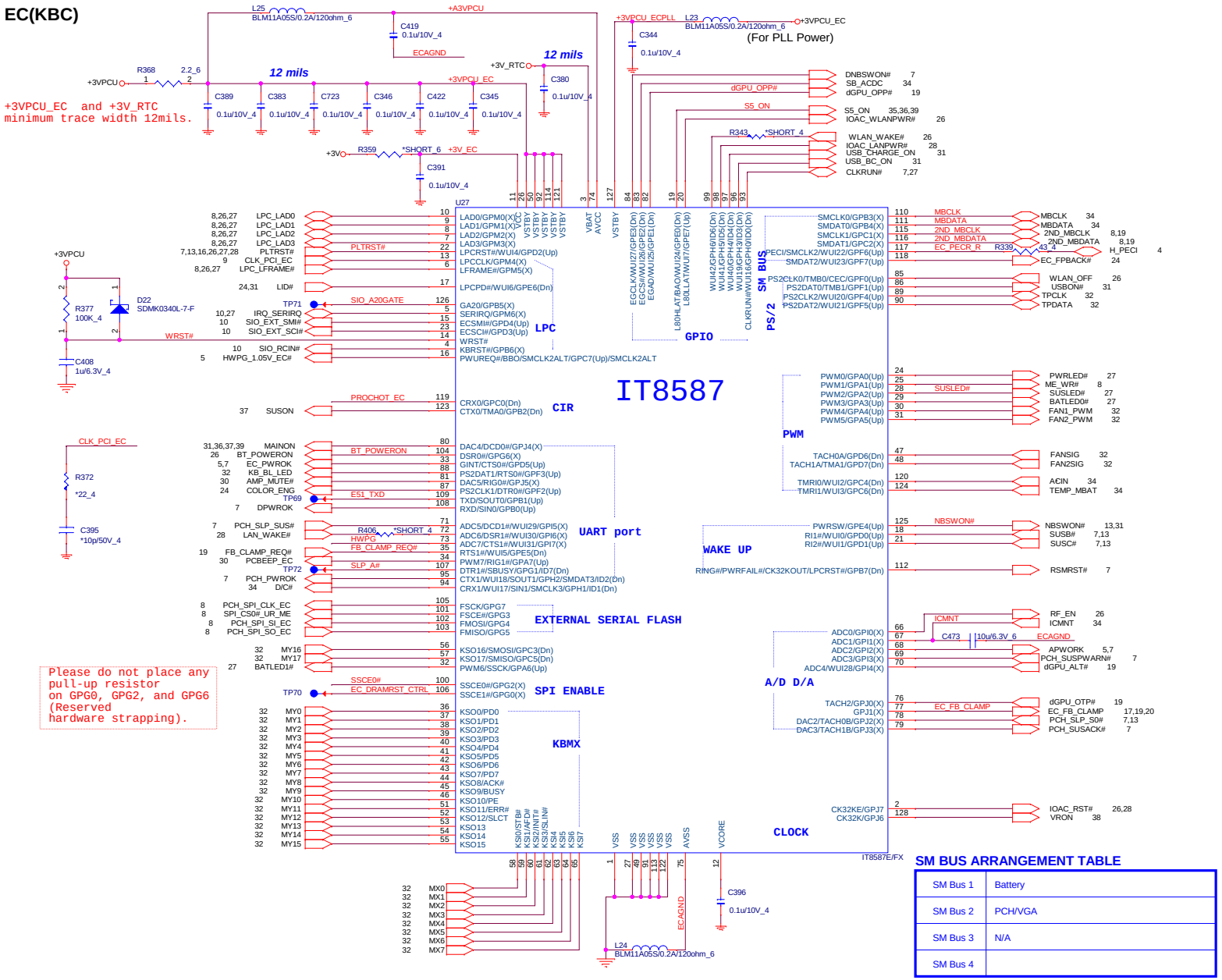
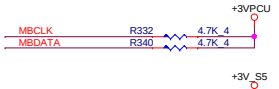
EC(KBC)



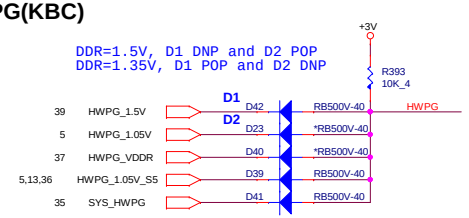
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	N/A
SM Bus 4	

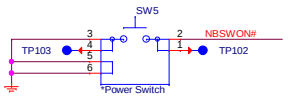
SM BUS PU(KBC)



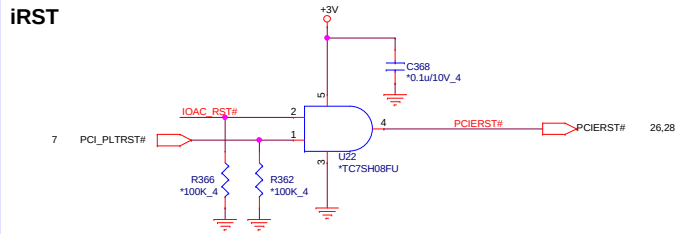
HWPG(KBC)



For test only



iRST



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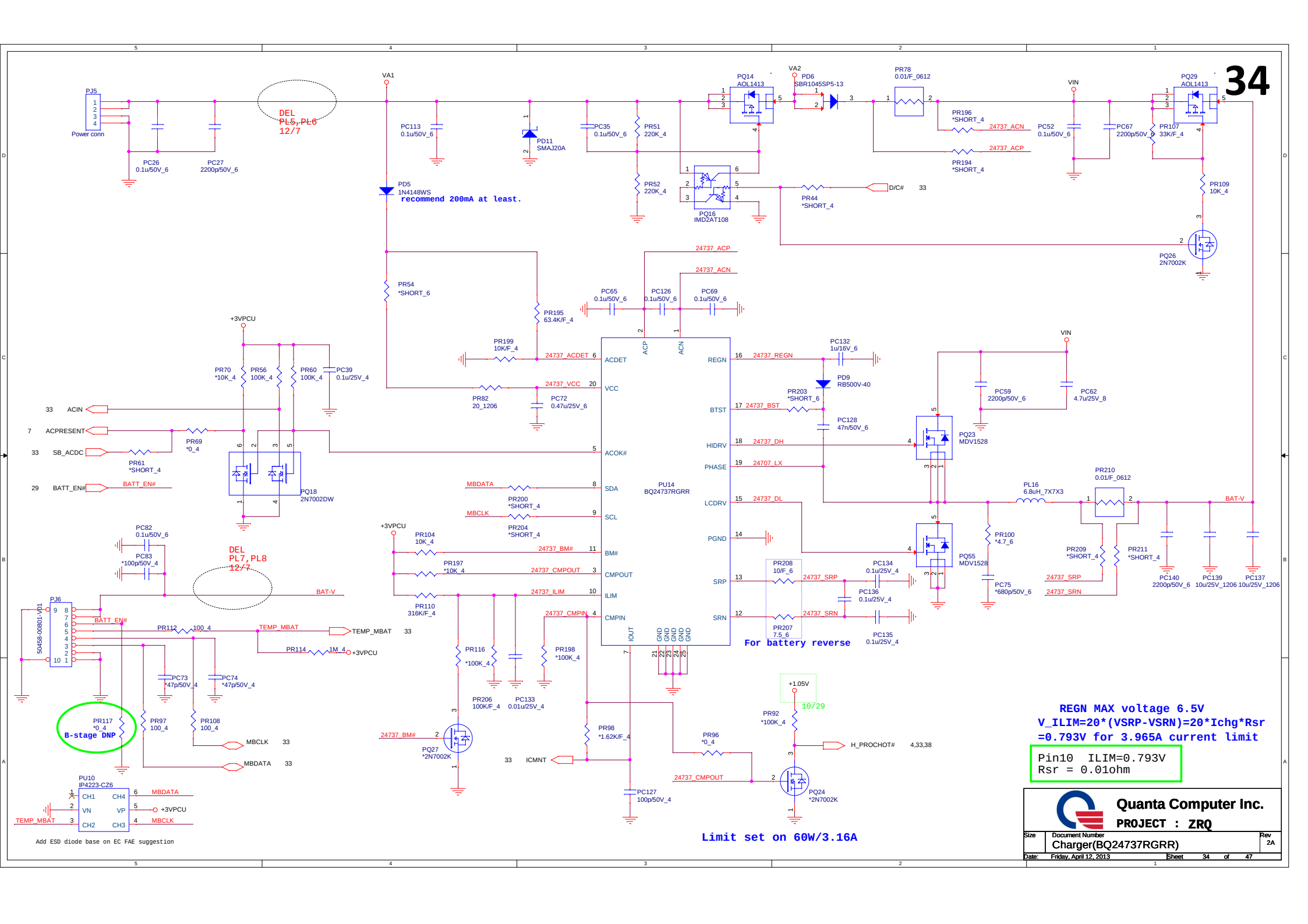
34
PJ5
Power conn
PC26 0.1u/50V_6
PC27 2200p/50V_6
DEL PL5,PL6 12/7
VA1
PC113 0.1u/50V_6
PD11 SMAJ20A
PD5 1N4148WS
recommend 200mA at least.
PC35 0.1u/50V_6
PR51 220K_4
PR52 220K_4
PQ14 AOL1413
PQ16 IMD2AT108
VA2
PD6 SBR1045SP5-13
PR78 0.01/F_0612
PR196 *SHORT_4
PR194 *SHORT_4
24737_ACN
24737_ACP
PR44 *SHORT_4
D/C# 33
VIN
PC52 0.1u/50V_6
PC67 2200p/50V_6
PQ29 AOL1413
PR107 33K/F_4
PR109 10K_4
PQ26 2N7002K
PR54 *SHORT_6
PR195 63.4K/F_4
PC65 0.1u/50V_6
PC126 0.1u/50V_6
PC69 0.1u/50V_6
+3VPCU
PR70 *10K_4
PR56 100K_4
PR60 100K_4
PC39 0.1u/25V_4
PR199 10K/F_4
PR82 20_1206
PC72 0.47u/25V_6
33 ACIN
7 ACPRESENT
33 SB_ACDC
29 BATT_EN#
PR69 *0_4
PR61 *SHORT_4
PQ18 2N7002DW
BATT_EN#
PU14 BQ24737RGRR
ACP
ACN
ACDET
VCC
ACOK#
SDA
SCL
BM#
CMPOUT
ILIM
CMPIN
IOUT
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
GND
24737_REGN
24737_BST
24737_DH
24707_LX
24737_DL
24737_SRP
24737_SRN
24737_VCC
24737_ACDET
24737_BM#
24737_CMPOUT
24737_ILIM
24737_CMPIN
MBDATA
MBCLK
PC132 1u/16V_6
PD9 RB500V-40
PR203 *SHORT_6
PC128 47n/50V_6
PQ23 MDV1528
PC59 2200p/50V_6
PC62 4.7u/25V_8
PR210 0.01/F_0612
PL16 6.8uH_7X7X3
BAT-V
PR100 *4.7_6
PQ55 MDV1528
PC75 *680p/50V_6
PR209 *SHORT_4
PR211 *SHORT_4
PC140 2200p/50V_6
PC139 10u/25V_1206
PC137 10u/25V_1206
PR200 *SHORT_4
PR204 *SHORT_4
PR104 10K_4
PR197 *10K_4
PR110 316K/F_4
PR208 10/F_6
PR207 7.5_6
PC134 0.1u/25V_4
PC136 0.1u/25V_4
PC135 0.1u/25V_4
For battery reverse
PC82 0.1u/50V_6
PC83 *100p/50V_4
DEL PL7,PL8 12/7
PJ6
50458-00801-V01
BATT_EN#
PR112 100_4
TEMP_MBAT
PR114 1M_4
+3VPCU
PC73 *47p/50V_4
PC74 *47p/50V_4
PR117 *0_4
B-stage DNP
PR97 100_4
PR108 100_4
MBCLK 33
MBDATA 33
PU10 IP4223-CZ6
CH1
CH4
VN
VP
CH2
CH3
Add ESD diode base on EC FAE suggestion
PR116 *100K_4
PR206 100K/F_4
PC133 0.01u/25V_4
PR198 *100K_4
PR98 *1.62K/F_4
PQ27 *2N7002K
33 ICMNT
PC127 100p/50V_4
PR96 *0_4
+1.05V
10/29
PR92 *100K_4
H_PROCHOT# 4,33,38
PQ24 *2N7002K
Limit set on 60W/3.16A
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Pin10 ILIM=0.793V
Rsr = 0.01ohm
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MAIND → MAIND 36,37,39

SYS_SHDN# → SYS_SHDN# 10,27,39

+5VPCU
5 Volt +/- 5%
TDC : 5.4A
PEAK : 7.2A
OCP : 9A
Width : 220mil

+3VPCU
3.3 Volt +/- 5%
TDC : 4.7A
PEAK : 6.2A
OCP : 7.5A
Width : 200mil

OCP:9A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=9-(3.367/2)=7.32A
Vth=7.32A*14mOhm+1mV=103.43mV
R(Ilim)=(103.43mV*8)/10uA
=82.774K

OCP:7.5A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=7.5-(2.676/2)=6.16A
Vth=6.16A*14mOhm+1mV=87.27mV
R(Ilim)=(87.27mV*8)/10uA
~69.81K

TDC : 1.5A
PEAK : 2A
Width : 80mil

TDC : 2.4A
PEAK : 3.2A
Width : 100mil

TDC : 1.4A
PEAK : 1.8A
Width : 110mil

TDC : 1.2A
PEAK : 1.6A
Width : 60mil

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Size	Document Number: SYSTEM 5V/3V (TPS51225) — Rev: 2A
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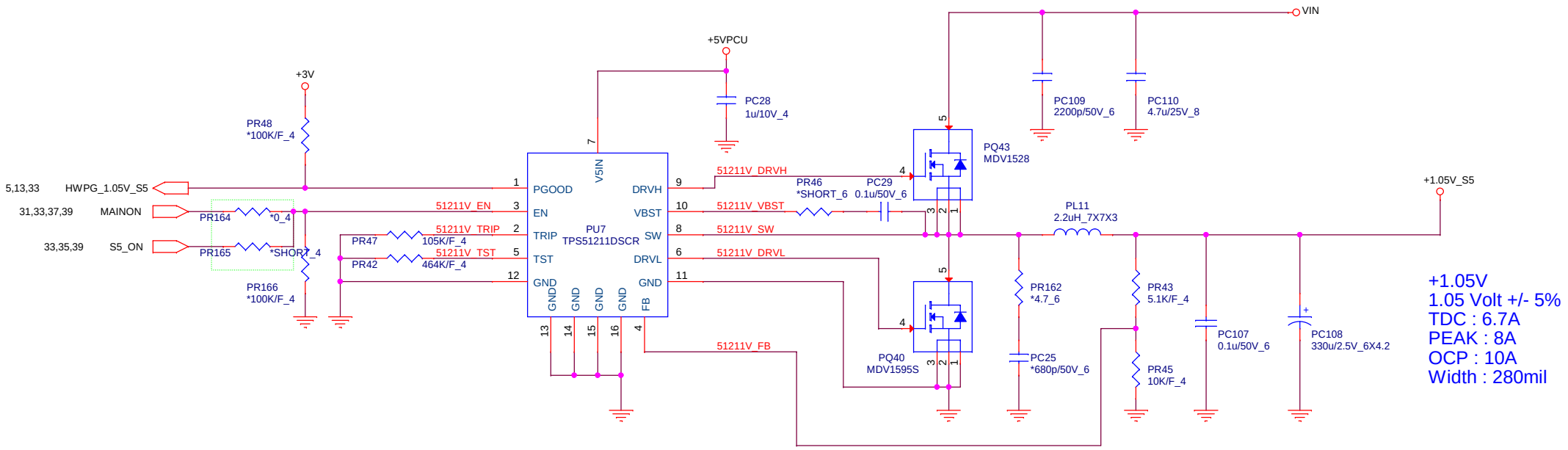
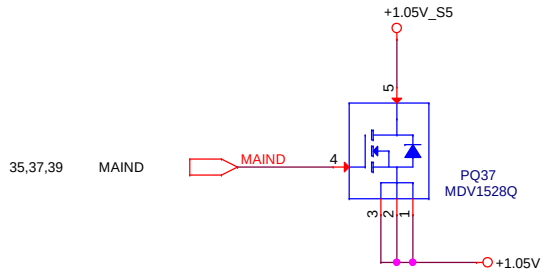


+1.05V
1.05 Volt +/- 5%
TDC : 6.7A
PEAK : 8A
OCP : 10A
Width : 280mil

OCP=10A
L ripple current
=(19-1.05)*1.05/(2.2u*290k*19)
=1.555A
Vtrip=10-(1.555/2)*14mohm
=0.129V
Rlimit=0.129/10uA*8=103.293Kohm



TDC : 2.4A
PEAK : 3.2A
Width : 100mil

Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	+1.05V(TPS51211)	2A
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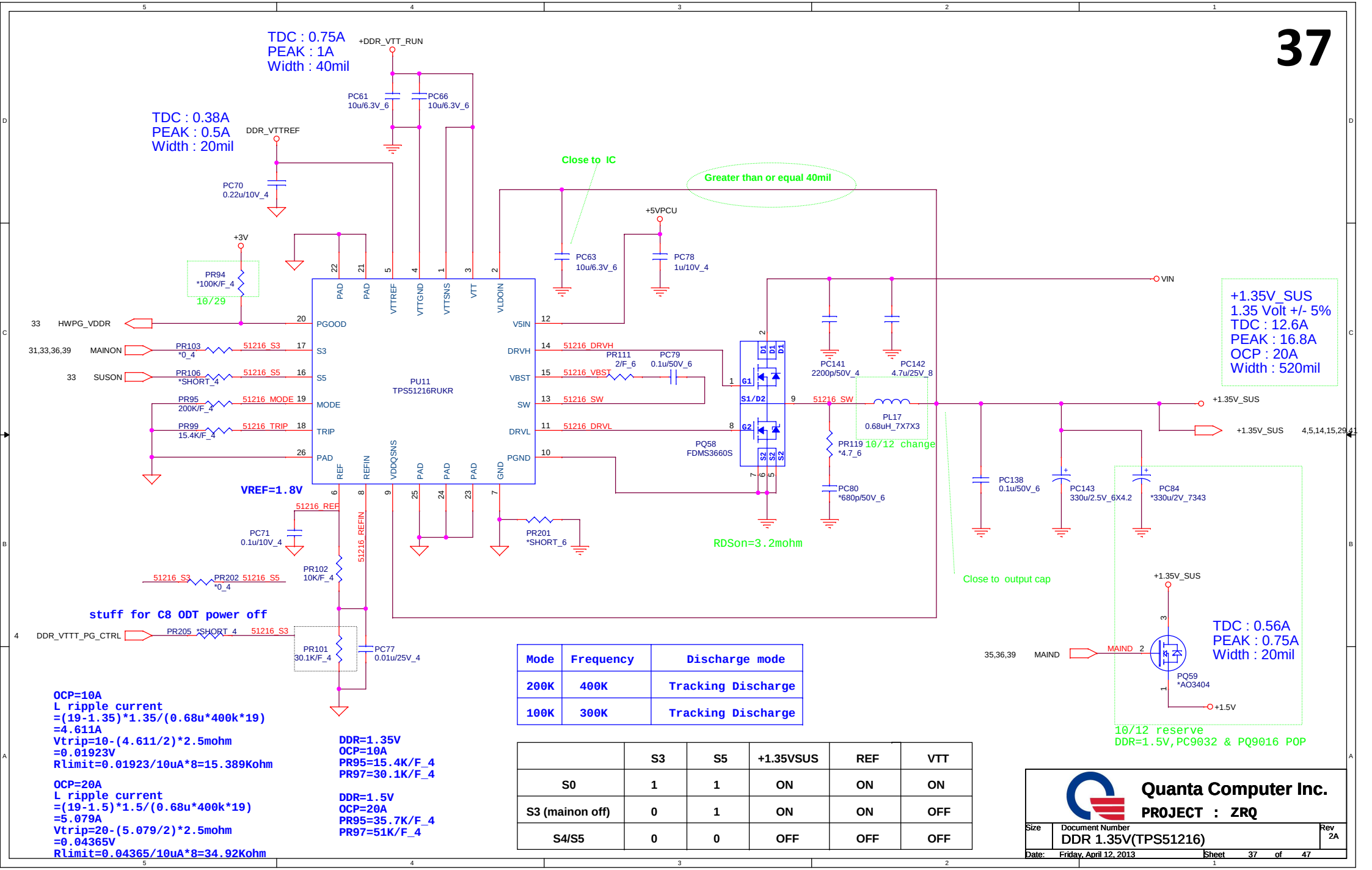

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=10A
L ripple current
=(19-1.35)*1.35/(0.68u*400k*19)
=4.611A
Vtrip=10-(4.611/2)*2.5mohm
=0.01923V
Rlimit=0.01923/10uA*8=15.389Kohm

OCP=20A
L ripple current
=(19-1.5)*1.5/(0.68u*400k*19)
=5.079A
Vtrip=20-(5.079/2)*2.5mohm
=0.04365V
Rlimit=0.04365/10uA*8=34.92Kohm

DDR=1.35V
OCP=10A
PR95=15.4K/F_4
PR97=30.1K/F_4

DDR=1.5V
OCP=20A
PR95=35.7K/F_4
PR97=51K/F_4

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Size	Document Number	Rev
	DDR 1.35V(TPS51216)	2A

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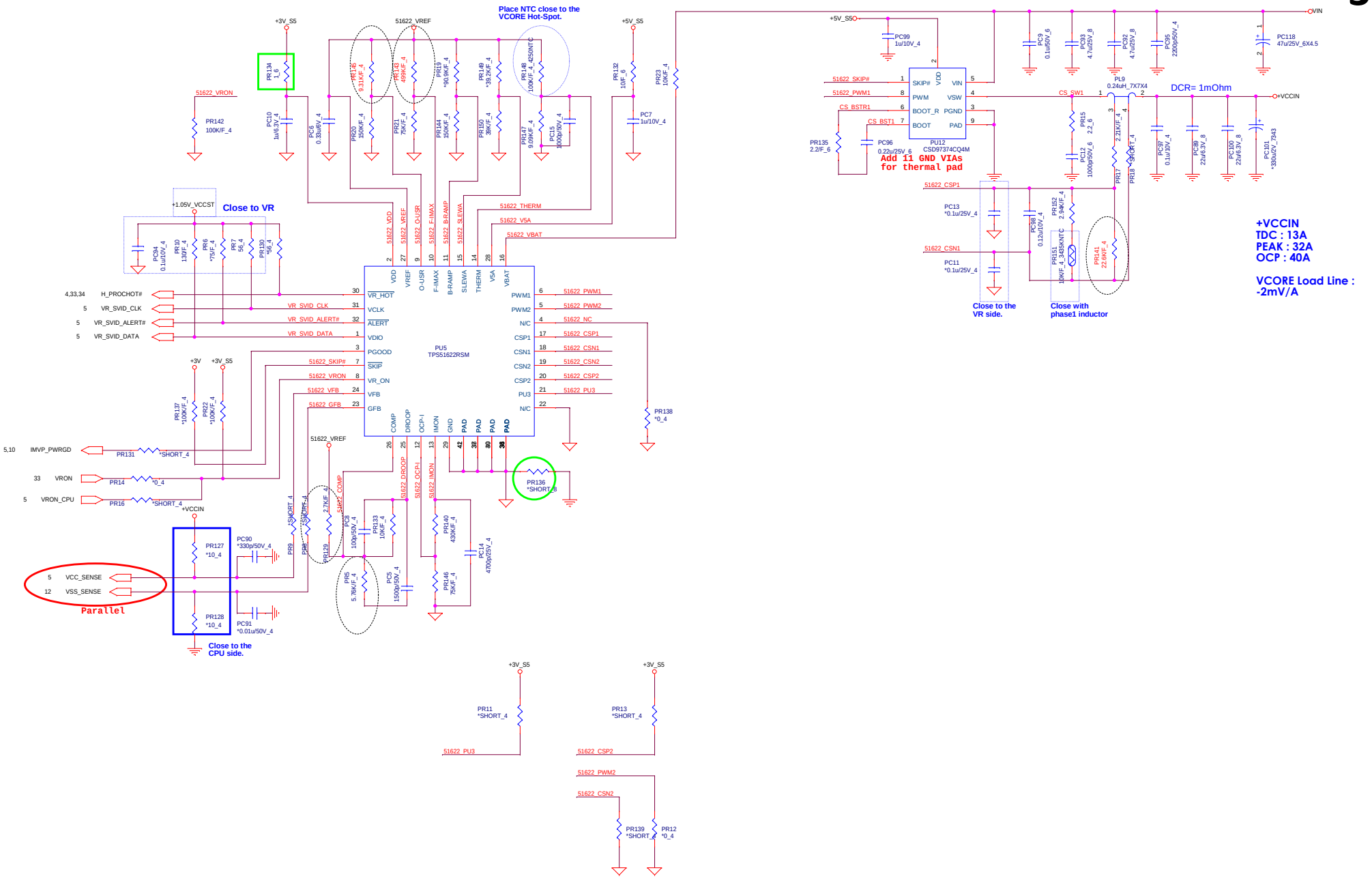

Quanta Computer Inc.		
PROJECT : ZRQ		
Size	Document Number: +VCCIN(TPS51622)	Rev: 2A
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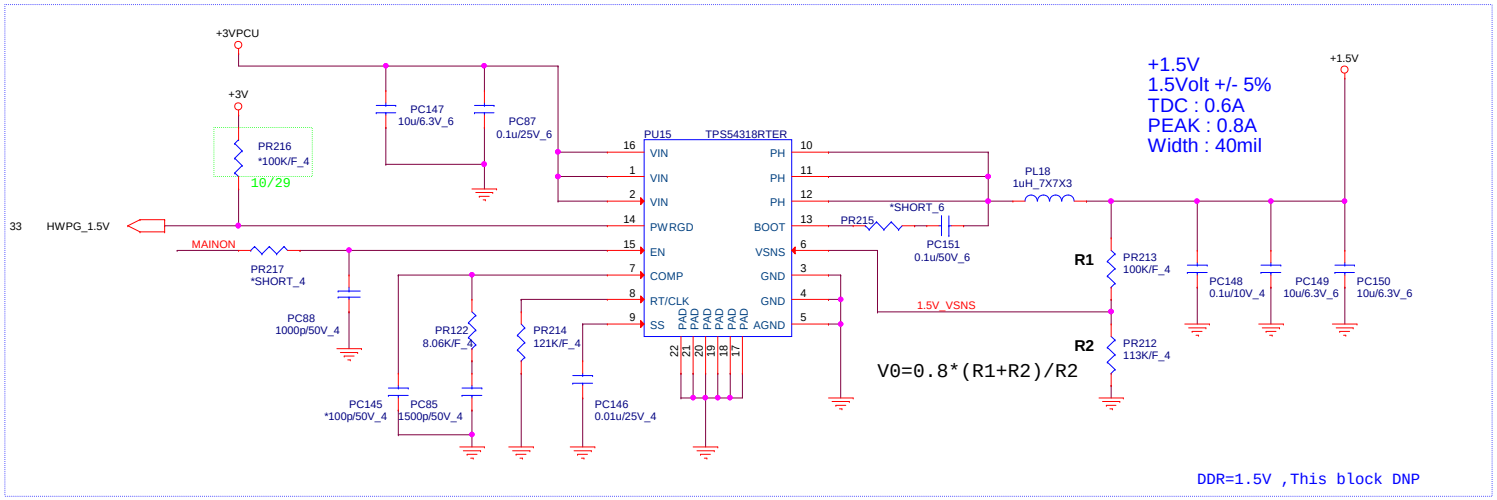
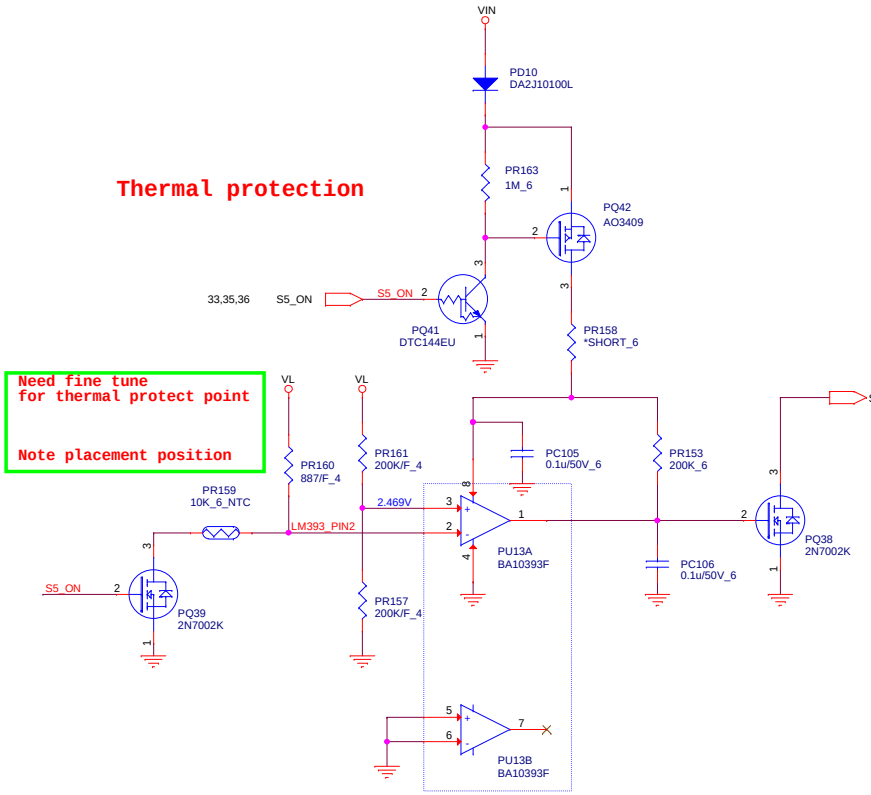
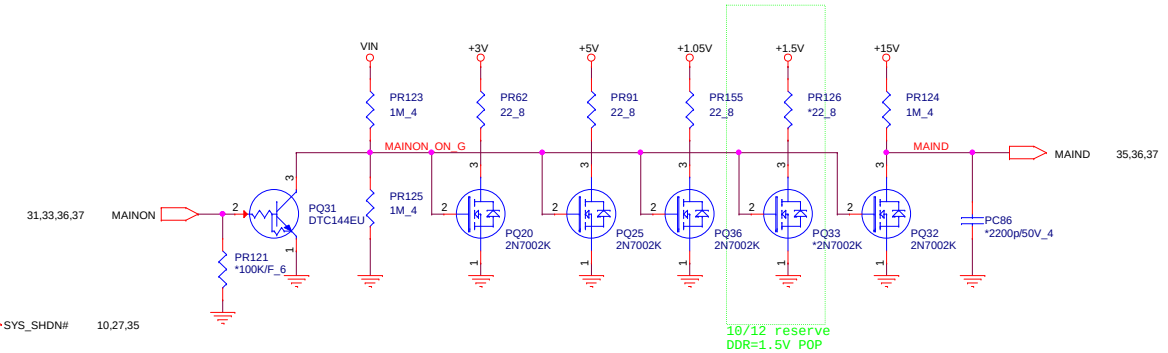


Thermal protection





For EC control thermal protection (output 3.3V)

Quanta Computer Inc.			
PROJECT : ZRQ			
Size	Document Number		Rev
	+1.5V/+1.8V/Thermal protect		2A
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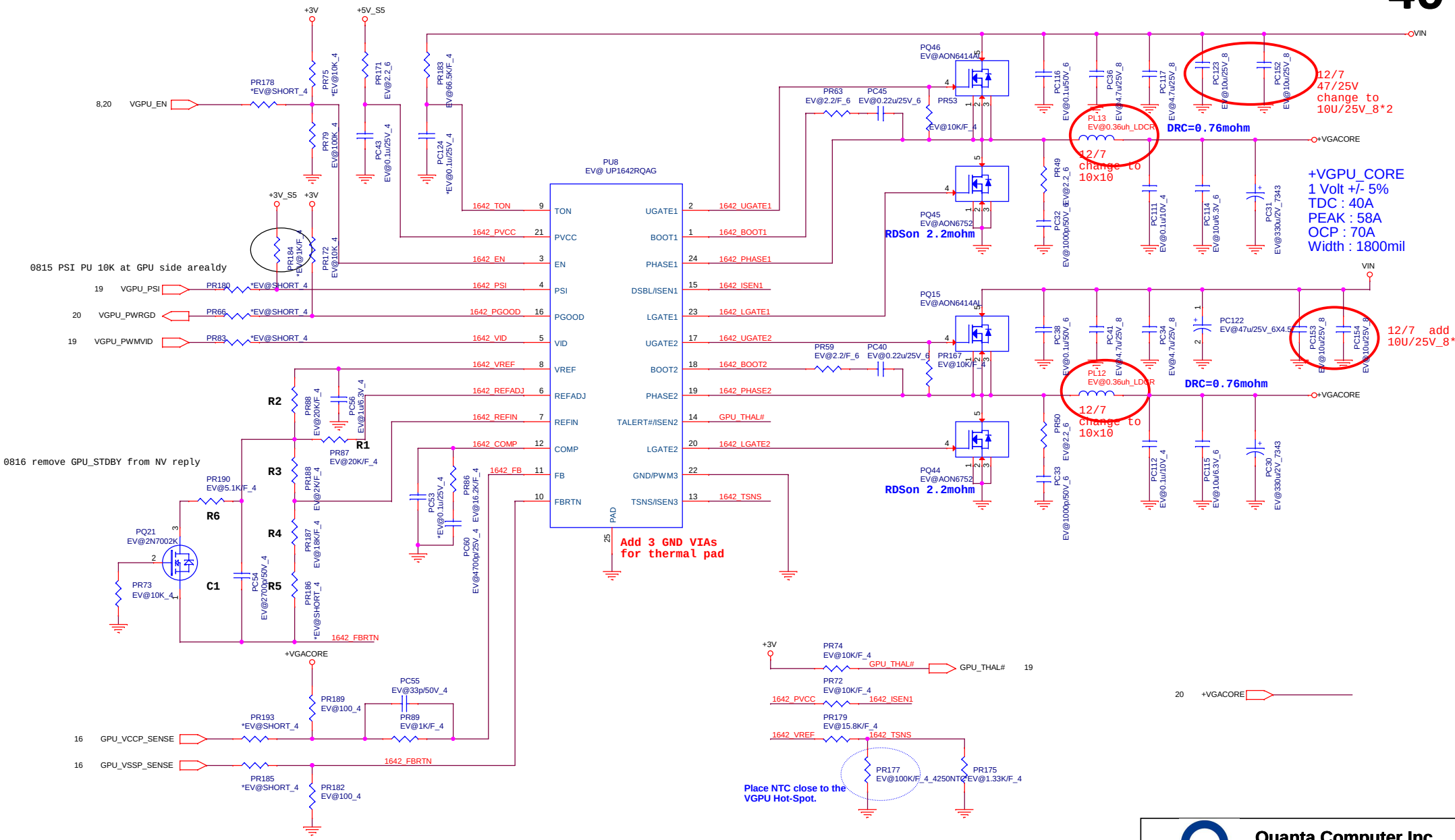
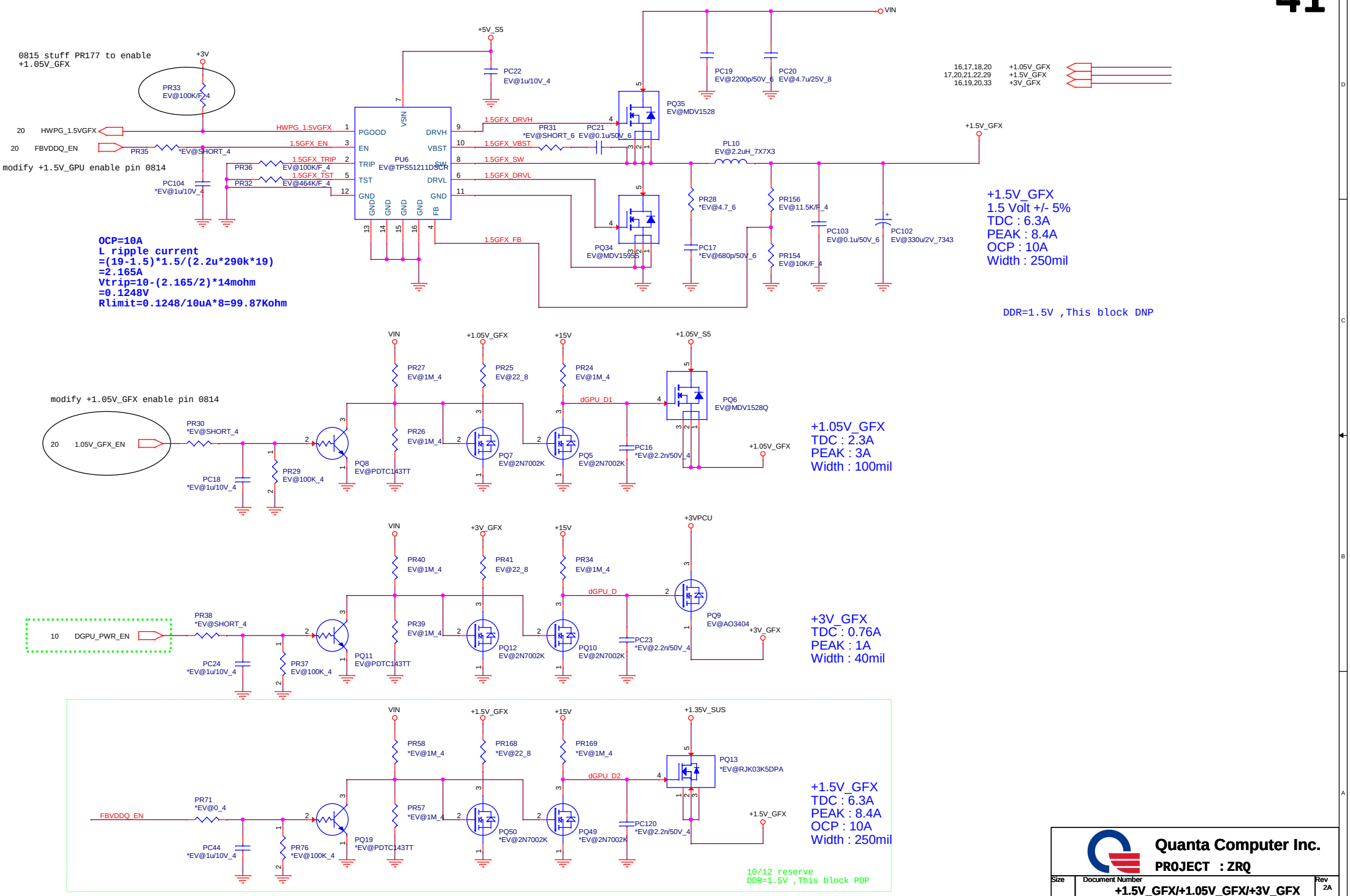


Quanta Computer Inc.		
PROJECT : ZRQ		
Size	Document Number: +VGPU_CORE(UP1642PQAG)	Rev: 2A
Date: Friday, April 12, 2013	Sheet 40 of 47	



Quanta Computer Inc. PROJECT : ZRQ			
Size	Document Number: +1.5V_GFX/+1.05V_GFX/+3V_GFX		Rev: 2A
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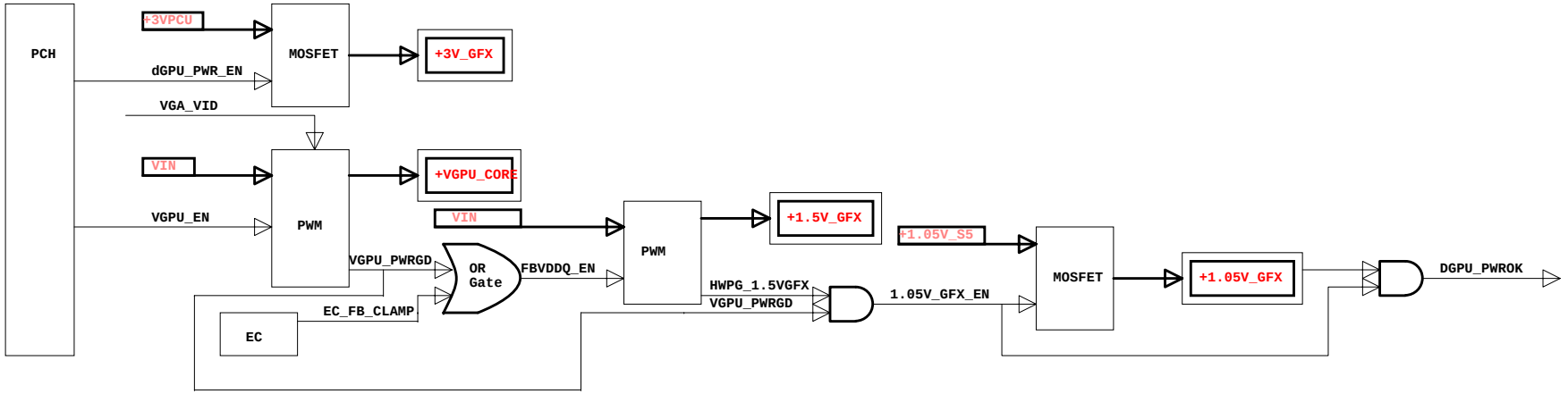
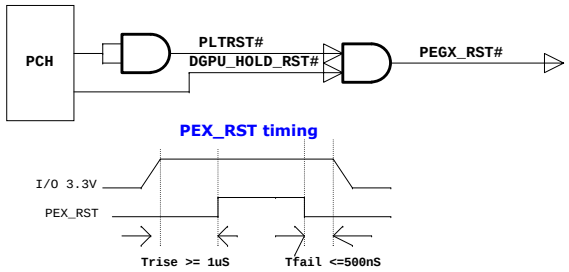
VGA power up sequence



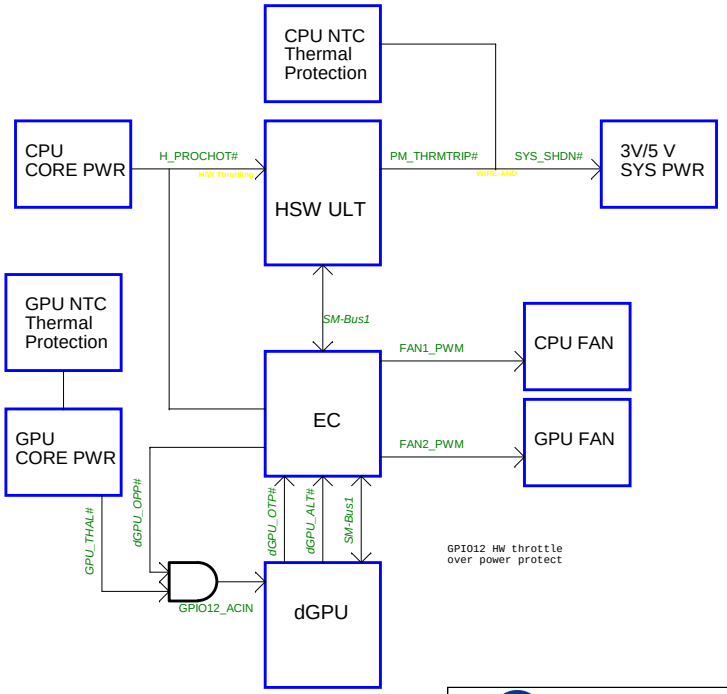
VGA Reset



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+VGPU_CORE	variation	External GPU POWER	VGPU_EN	S0
+3V_GFX	+3.3V	External GPU POWER	dGPU_PWR_EN	S0
+1.5V_GFX	+1.5V	External GPU POWER	FBVDDQ_EN	S0
+1.05V_GFX	+1.05V	External GPU POWER	1.05V_GFX_EN	S0

Thermal Follow Chart



dGPU_OPP# EC notify HW throttle over power protect
dGPU_ALT# for ADPS circuit to infrom EC NV dGPU VPS Alert
dGPU_OTP# VGA thrmtrip# => inform EC over temperature protect

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Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	3A

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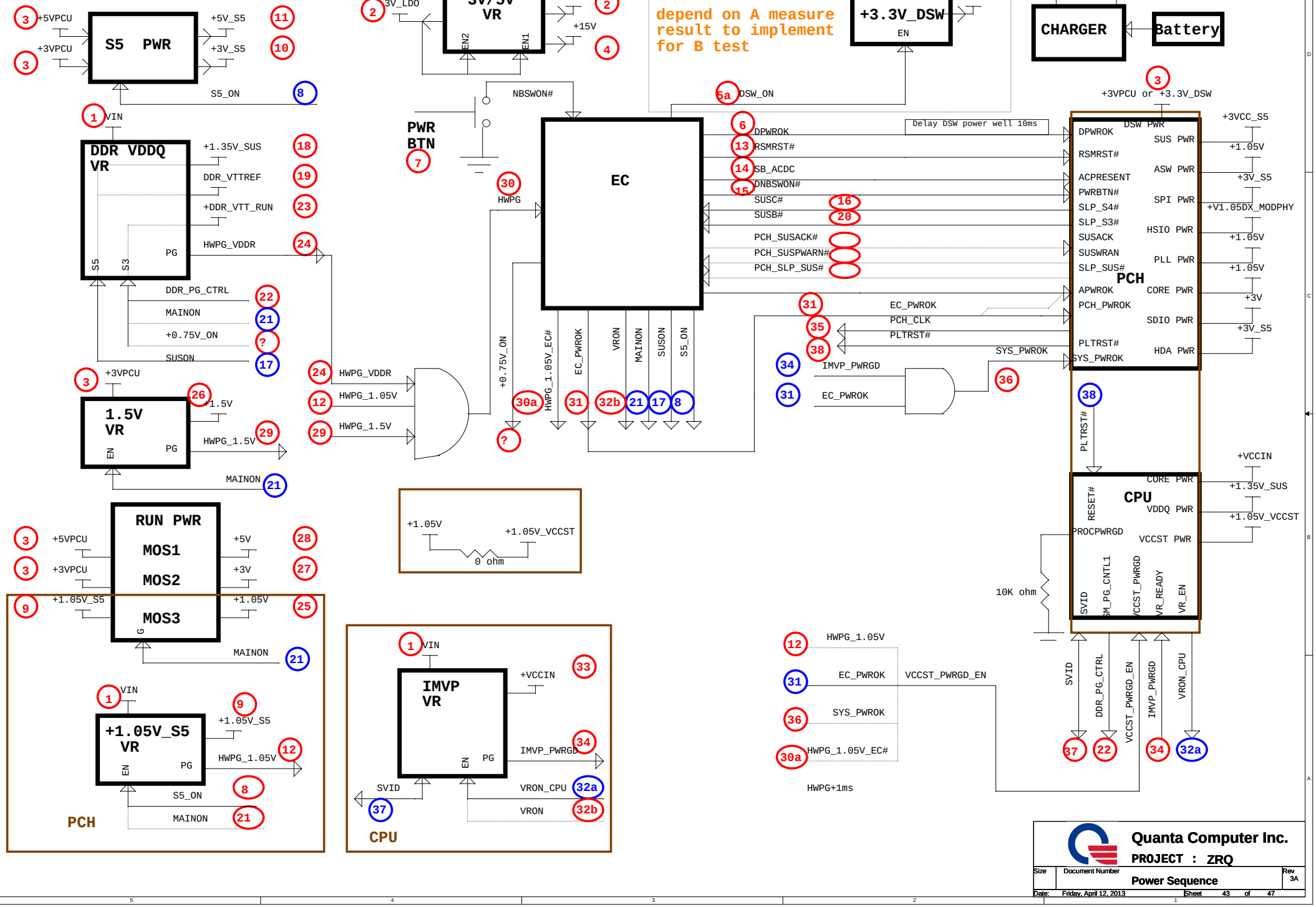
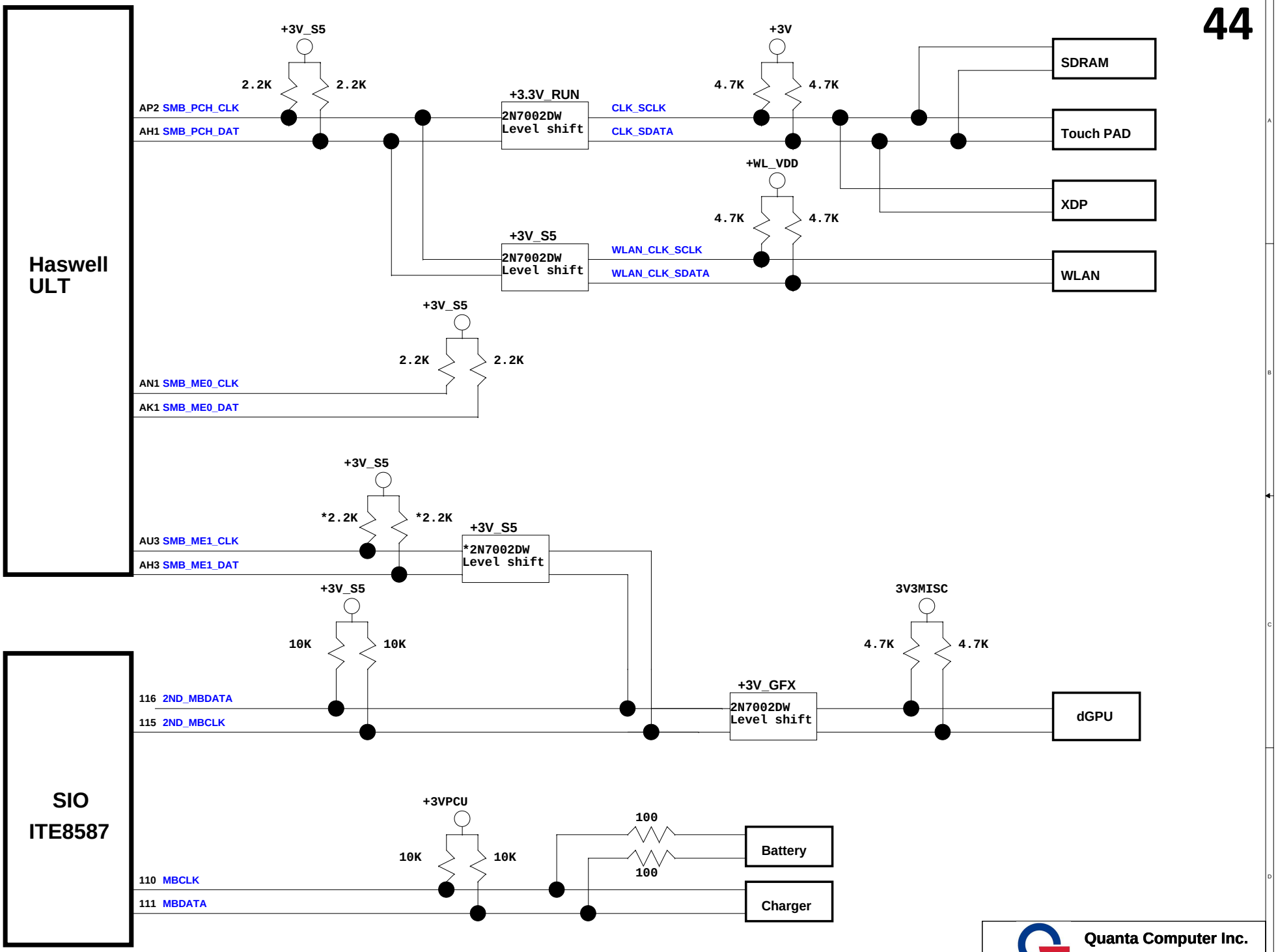
Battery Mode

Support Deep Sx

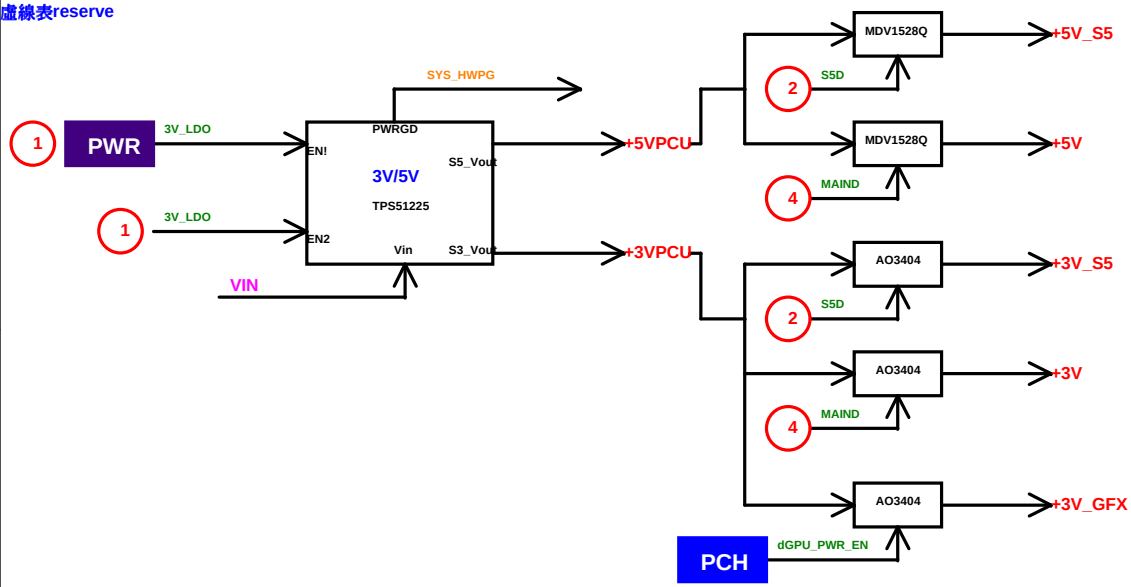


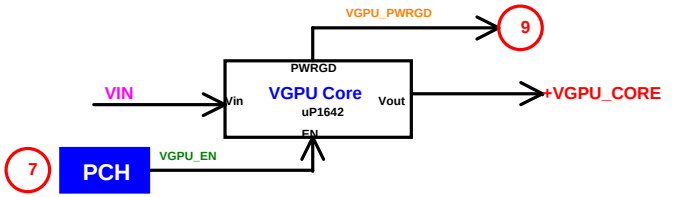
Quanta Computer Inc.	
PROJECT : ZRQ	
Size	Document Number: Power Sequence
Rev	3A
Date: Friday, April 12, 2013	Sheet 43 of 47

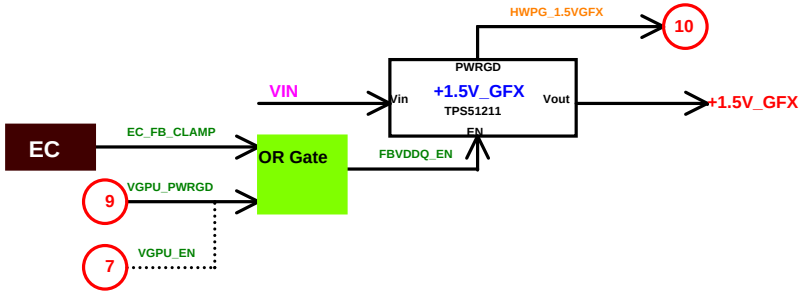


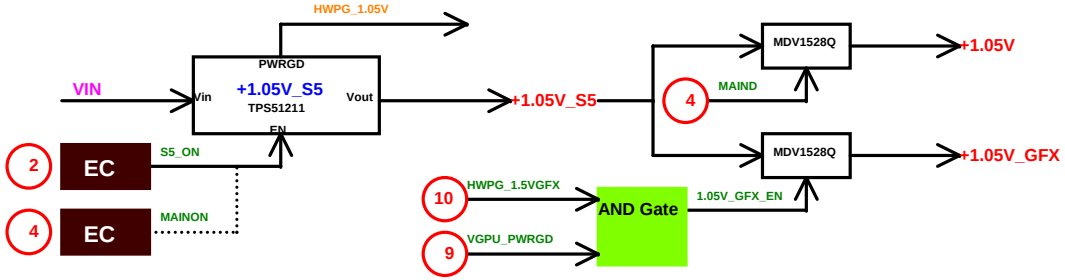
Quanta Computer Inc.		
PROJECT : ZRQ		
Size	Document Number	Rev 3A
	Block Diagram	
Date: Friday, April 12, 2013	Sheet 44 of 47	

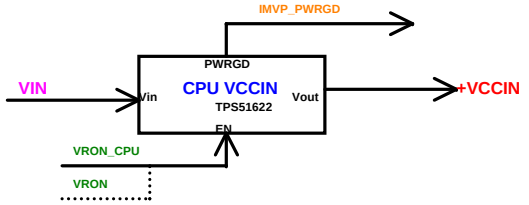
實線表defult
虛線表reserve

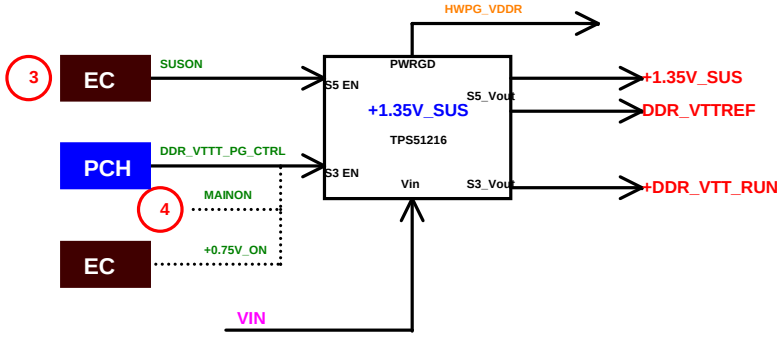


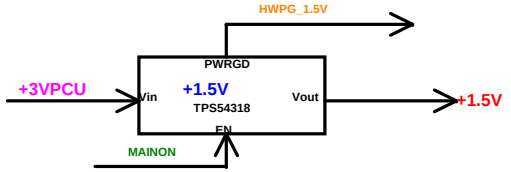












Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	ULT PWR CONTROL	3A

Date: Friday, April 12, 2013 Sheet 45 of 47

Model	Version		CHANGE LIST
ZRQ	1A		
	2A	1	Add R806 Pull down for EDP_HPD(Intel check List).(Page 02)
		2	Add R811 and reserve R809 for Codec Vendor request.(Page 30)
		3	Change R345 footprint from 0402 to 0603.(Page 14)
		4	Change U10 to correct PN AL007534001.(Page 31)
		5	Improve IMVP_PWRGD voltage to low , so del R66,Q9 , R61,Q50 ,R495 and add U55 , C767 , R807. (Page 10)
		6	Change CN12 to 12 PIN connect_DFFC12FR034 (Page 31)
		7	Change SW6 from DHP08TEPV00 to DHPATE2CK03.(Page 29)
		8	Move Hall sensor funtion to USB/B.(Page 24)
		9	Add R828 100K PD for MAINON. Upgrade U27 from AJ085870F02 to AJ085870F03. (Page33)
		10	Collect netname +V1.05S_VCCPCPU to +V3.3S_VCCSDIO. (Page11)
		11	Q7 change from PMF780SN to BAM70020002. (Page25)
		12	Correct U41 footprint to ssop5-p-a-toshiba-b. (Page23)
		13	Change LED5,LED6 P/N from BEB00024ZA0 to BEB00028ZA0. (Page27)
		14	Del Q5, Q47,R51,R25 , add U56,C768 . (Page13)
		15	DEL PL5,PL6,PL7,PL8 . (Page34_power)
		16	Change PR145 from CS28872FB08 to CS29312FB13 . (Page38_Power)
		17	Change PR143 from CS45362FB00 to CS44992FB11 . (Page38_Power)
		18	Change PR129 from CS22672FB12 to CS22702FB14 . (Page38_power)
		19	Change PR5 from CS31002FB26 to CS25762FB01 . (Page38_Power)
		20	Change PR141 from CS32432FB19 to CS32262FB15 . (Page38_Power)
		21	Change PC123 from CC64704MZ10 to CH6104KEA00 . (Page40_Power)
		22	Add PC152,PC153,PC154 to CH6104KEA00 . (Page40_Power)
		23	Change PL12,PL13 from CV+24P0MZ00 to CV+36T0MZ01 10X10 size . (Page40_Power)
		24	SWAP USB0 and USB1 . (Page09)
		25	Change CN27 to DFHS52FR044 ,same as CN18 (Page 26)
		26	add CN12 PIN4 for USBPWR3. (Page 31)
		27	CN9 change frootprint to dp-adis0022-p001a-20p-smt. (Page 23)
		28	Depop R728 and Pop R727 to sove Deep S3 can't wakep issue. (Page 10)
		29	Del C429. (Page20)
		30	Add R826(VRON) ,R827SON) 100k to Gnd. (Page33)
		31	Change CN9 PN to DFTD20FR001 . (Page23)
		32	Add C735_0.1u for Vendor request . (Page28)
		33	Add C736_0.1u and reserve C727_4.7u for Vendor request . (Page29)
		34	Change R348 Pu hign to +3V . (Page28)
		35	TEMP_MBAT from battery connect pin 5 to pin 6 (BATT_EN0) . (Page34)
		36	Change R354(PCH_PWROK) from 10 k to 100K . (Page07)
		37	Reserve R808 ,R810_0 Ohm . (Page30)
		38	Change JP18 Packing and PN same as JP19 . (Page37)
		39	Add R835 for Vendor request. (Page23)
		40	Change R491 from 1M to 5.1M . (Page23)
		41	Change R691 from 121 to 120ohm(Intel Check list) . (Page04)
		42	Change SUSLED# power from +3V_S5 to +3V_PCU . (Page27)
		43	Change CN13 to DFHS40FS047 (H=4) ,due to PE request. Footprint is "gs12401-1011-40p-r-nb-smt. (Page24)
		44	VGPU_PSI Pull high from +3V to +3V_S5. (Page40)
		45	B-SMT USE RTL8411BA-CG need Depop R295 and change U21 PN to AL008411004. (Page28)
		46	C590,C591 change from 18P to 12P(Y6). (Page09)
		47	C278,C284 change from 27P to 12P(Y8). (Page28)
		48	Depop R147,R106,R94,R534 and Pop R91,R95,R146,R533 to support Qual Mode. (Page10)
		~~49~~	~~Pop PR104. (Page40_Power)_內部行文~~
		50	Change PU8 from AL001642000 to AL001642001. (Page40_Power)_內部行文
		51	PC6 EOD Part change to CH4331K9B06. (Page38_Power)
		52	PC5,PC85 EOD Part change to CH21506KB14. (Page38,39_Power)
		53	Change U27 from AJ085870F03 to AJ085870F04. (Page33)_內部行文
		~~54~~	~~Add level Shift funtion. (Page25)~~
		55	Depop PR75. (Page40_Power)_內部行文
		56	Change PC15 to 1000p_50V(CH21006JB10). (Page38_Power)_內部行文
		57	Depop PR75. (Page40_Power)_內部行文
	3A	1	Depop R226, Pop Q26(BAM70020002) ,R795 (CS31002FB26) for CG6 funtion.(Page19)
		2	Swap Pin 25 and Pin 32.(Page33)
		3	Del D31,C519 , and Add Q69,C738,C822,C823,C824 for SDA request.(Page23)
		4	Add Test Pad on SW5 ,SW8 for SMT request.(Page27,33)
		5	Add C317_4.7u for Vendor request.(Page28)
		6	SWAP CLKOUT_PCIE.(Page09)
		7	Pop R477, R478, R479, R480 _100ohm(CS31002FB22)for HDMI EMI Issue.(Page25)
		8	Pop C655,C654_10p(CH01006JB08) for SD CLK EMI issue .(Page29)
		9	Pop Bitclk C399_22p(CH02206JB08) for EMI issue .(Page30)
		10	DePop PR117 .(Page34)
		11	C285 change from 0402 to 0603 size .(Page28)
		12	Del CN5,C272,C253 footprint .(Page13)
		13	Depop R336 ,Pop R333 for Lan can't link to exlorer .(Page28)
		14	Depop R348 .(Page28)
		15	Reserve R812 for PCIE_LAN_WAKE# .(Page26)
		16	Add R815,C740 and pop R310 for softstart of Lan VCC.(Page28)
		17	R608 connect to CLK_PCIE_REQ4# .(Page09)
		18	Depop SW5 .(Page33)
		19	Del JP Resistor 0.001/F_3720 (CS+0018FL00): JP5,JP6,JP10,JP11,JP12,JP13,JP14,JP15,JP17,JP18,JP19,JP20,JP21,JP16.
		20	Del 0_4 (CS00002JB38) to SHORT PAD_4 : PR8,PR9,PR11,PR13,PR16,PR18,PR30,PR35,PR38,PR44,PR61,PR66,PR83,PR106, PR131,PR139,PR165,PR170,PR178,PR180,PR185,PR191,PR193,PR194,PR196,PR200,PR204,PR205,PR209,PR211,PR217,PR186
		21	Del 0_6 (CS00003J951) to SHORT PAD_6 : PR31,PR46,PR54,PR77,PR90,PR181,PR201,PR203,PR215,PR158
		22	Del 0_8 (CS00004JA40) to SHORT PAD_8 : PR136
		23	Add R813_0 OHM.(Page26)
		24	Change C740 from 0603 ot 0402 size.(Page28)
		25	Depop Q39 , R276,Pop R321 and change R320 to 1K to meet Lanwake signal spec.(Page28)
			~~Depop L9,L11,L31,L28 , and Pop R34,R47,R49,R55,R490,R487,R485,R481.(Page28)~~
		26	Del JP7, JP8, JP9(CS+001AGM13).(Page05)
		27	Change to 0402 shortpad:R45,R69,R173,R215,R236,R237,R239,R274,R277,R283,R288,R311,R328,R334,R353,R404,R409,R419,R423,R424,R425,R426,R430,R432,R434,R448,R449,R450, R513,R570,R573,R587,R591,R596,R625,R641,R652,R653,R678,R695,R712,R719,R722,R733,R734,R735,R736,R741,R758,R759,R760,R761,R762,R763,R764,R765,
		28	Change to 0603 shortpad:R107,R111,R158,R194,R197,R212,R229,R233,R234,R252,R269,R298,R303,R304,R338,R350,R351,R352,R356,R358,RR411,415,R418,R422,R431,R433,R440,R441, R442,R443,R444,R445,R446,R447,R540,R745,R766,R767
		29	Change to 0805 shortpad:R165,R174,R179,R190,R217,R268,R270,R452,R470,R559,R560,R732,R737,R749
		30	Change R408,R420 from 47 ohm to 56 ohm.(Page30)
		31	Change R411, R422 from shortpad to 0603 footprint.(Page30)

DOC NO.	PROJECT MODEL :	ZRQ	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

Quanta Computer Inc.
PROJECT : ZRQ
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Date: Friday, April 16, 2010 | Sheet 36 of 47

Model	Version	CHANGE LIST
ZRQ	3B	1 R276 change fro m 10K to 1K , Depop R320. (PCIE_LAN_WAKE#)_內部行文 2 Change C24 KB Conn PN to DFFC26FR063 .(Page 32)_內部行文 3 Change U27 EC to E version AJ085870F05 .(Page 33)_內部行文. 4 Fine tune Amp Gain =>R422,R411 change from 0 ohm to 1k , and pop R421,R410 to 1.62K .(Page 30) 5 Change TEMP_MBAT from Pin 6 to Pin 5 of PJ1 .(Page 34) 6 Depop Q24 , and Add R228 to solve level abnormal issue for CG6 .(Page 19) 7 Add R816 and net "LB_PWR_CNN_Q" to stuff Q69 always for safety issue .(Page 19) 8 Reserve R855,R859 and add R854,R857 .(Page 23) 9 For WHQL Change USB Port1 and Port4 10 Add new on Board RAM HYNIX H5TC4G63AFR-PRBA RAM ID:0000 11 Del L35,L36,L6,L7,L8,L29,L12,L13,L32,L16,L34
	3C	1 Change to 0402 shortpad: R725,R724,R711,R716,R26,R27,R28,R29,R32,R33,R483,R484,R493,R492,R56,R57,R58,R59, R90,R89,R660,R664,R702,R638,R639,R651,R225,R346,R355,R778,R785,R790,R73 , R455,R456,R457,R458,R459,R343,R406,R596 2 For HDMI 7-2 issue change R37,R38,R39,R40,R41,R42,R43,R44 To 470 ohm and remove R478,R479,R477,R480 (Page 25) 3 For TI HD3SS2521 issue R77,R79,R502,R503 need mount 10K, change R528 from 100 ohm to 0 ohm and remove R854,R857 , add R855,R859. (Page 23) 4 Change to 0603 shortpad: R373,R337,R382,R297,R235,R326,R322,L38,R385,R220,R254,R359
	3F	1. Add C245 for intel request for G3 can't boot issue

DOC NO.	PROJECT MODEL :	ZRQ	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

Quanta Computer Inc.
PROJECT : ZRQ
Size: Document Number: Rev: 3A
Change list-2
Date: Friday, April 19, 2013 Sheet 37 of 47