Model Name : P5WE0
File Name : LA-6901P
BOM P/N:43

Compal Confidential

P5WE0 M/B Schematics Document

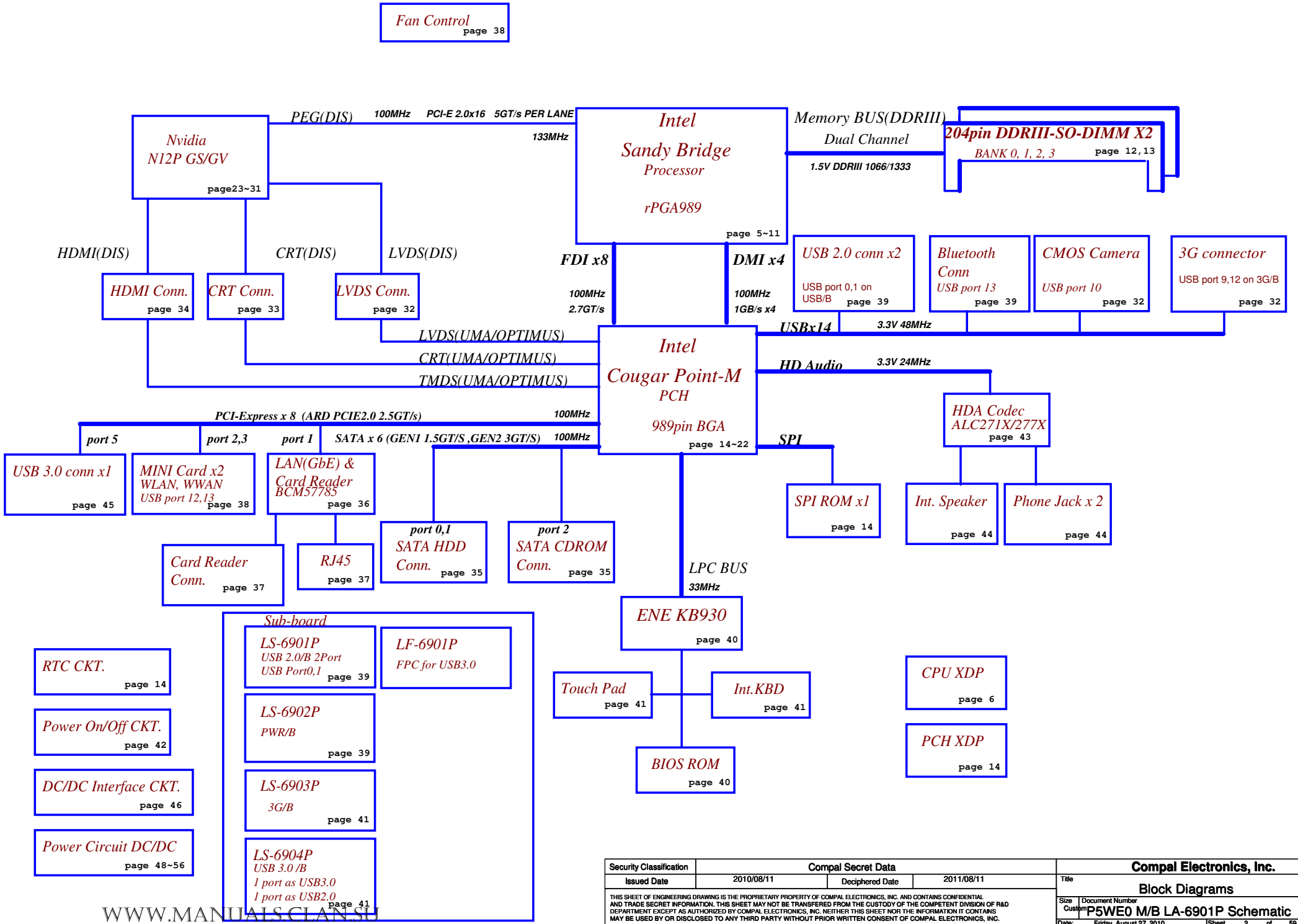
Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
Nvidia N12P GS/GV

2010-08-11

REV:0.1

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: P5WE0 M/B LA-6901P Schematic	Rev: 0A
Date: Friday, August 27, 2010	Sheet 1 of 59	



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	Block Diagrams		
Size	Document Number		Rev
Custom	P5WE0 M/B LA-6901P Schematic		0.1
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & BT & USB30 & USB20 Config

3G SKU: 3G@ USB30 SKU: USB30@ OPTMIUS SKU: OPT@

BT SKU: BT@ USB20 SKU: USB20@ Non-OPTMIUS SKU: NOPT@

LAN Chip A0 version: A0@

LAN chip B0 Version: B0@

BOM Config

UMA Only: BT@/3G@/USB30@/UMA@/UMAO@/NOPT@/A0@

OPTIMUS: BT@/3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@

DIS Only: BT@/3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@

VRAM BOM Config

X76***BOL01: Samsung

X76***BOL02: Hynix

VRAM P/N :

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)

Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EVT
DVT
PVT
Pre-MP

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
Dis with OPTIMUS	DIS@
DIS Only	DISO@
OPTIMUS	OPT@
Non-OPTIMUS	NOPT@
3G	3G@
Blue Tooth	BT@
USB2.0	USB20@
USB3.0	USB30@
VRAM	X76@
Connector	CONN@
Unpop	@
LAN Chip A0 version	A0@
LAN Chip B0 version	B0@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
	UHCI1	2	USB 2.0 & USB3.0 Conn.
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card 1(WLAN)
		9	3G/B(WWAN)
	UHCI5	10	Camera
		11	Mini Card 2(Reserved)
	UHCI6	12	SIM Card (3G/B)
		13	Blue Tooth

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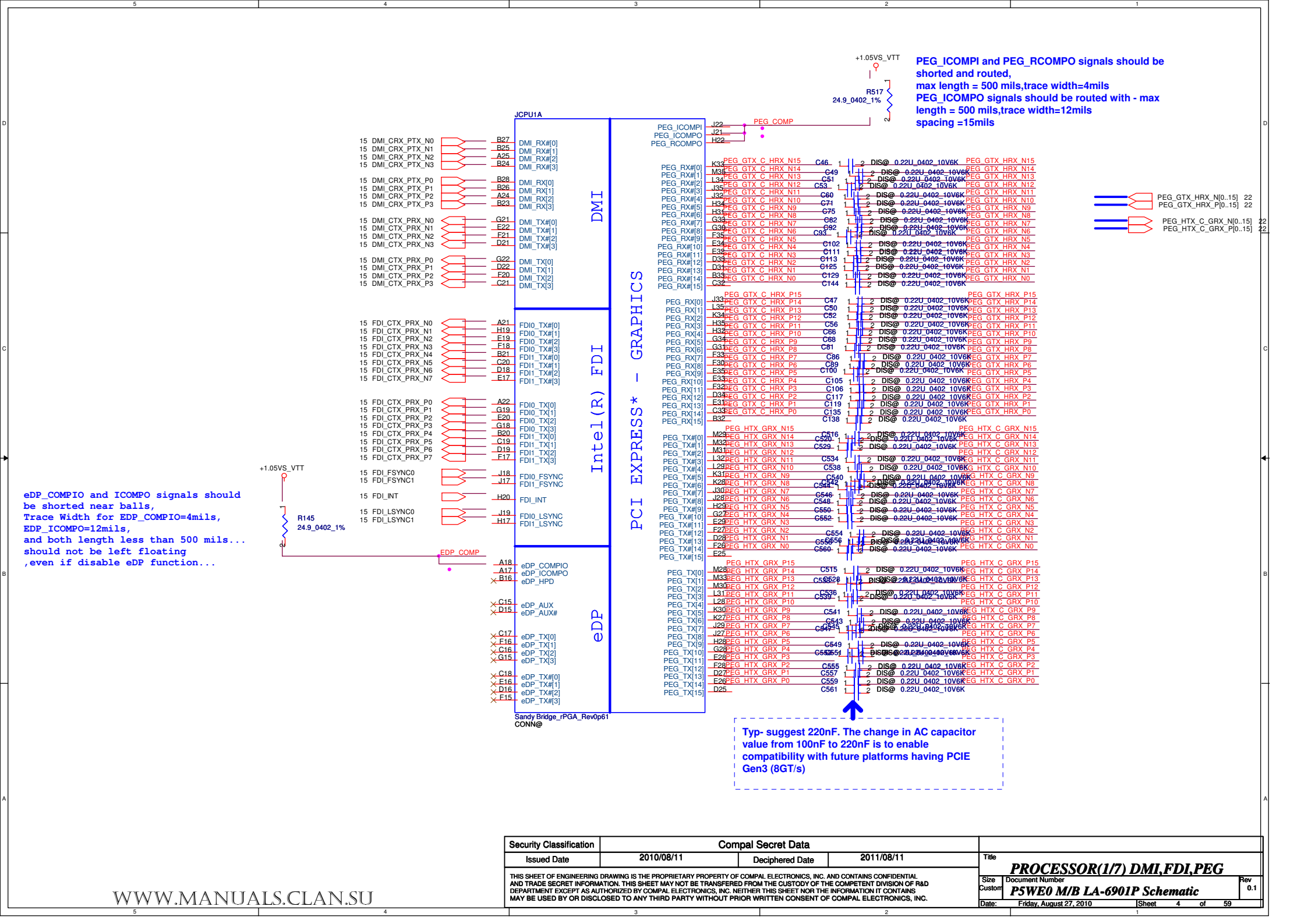
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.		
Title: Notes List		
Size: Custom	Document Number: P5WE0 M/B LA-6901P Schematic	Rev: 0.1
Date: Friday, August 27, 2010	Sheet 3 of 59	

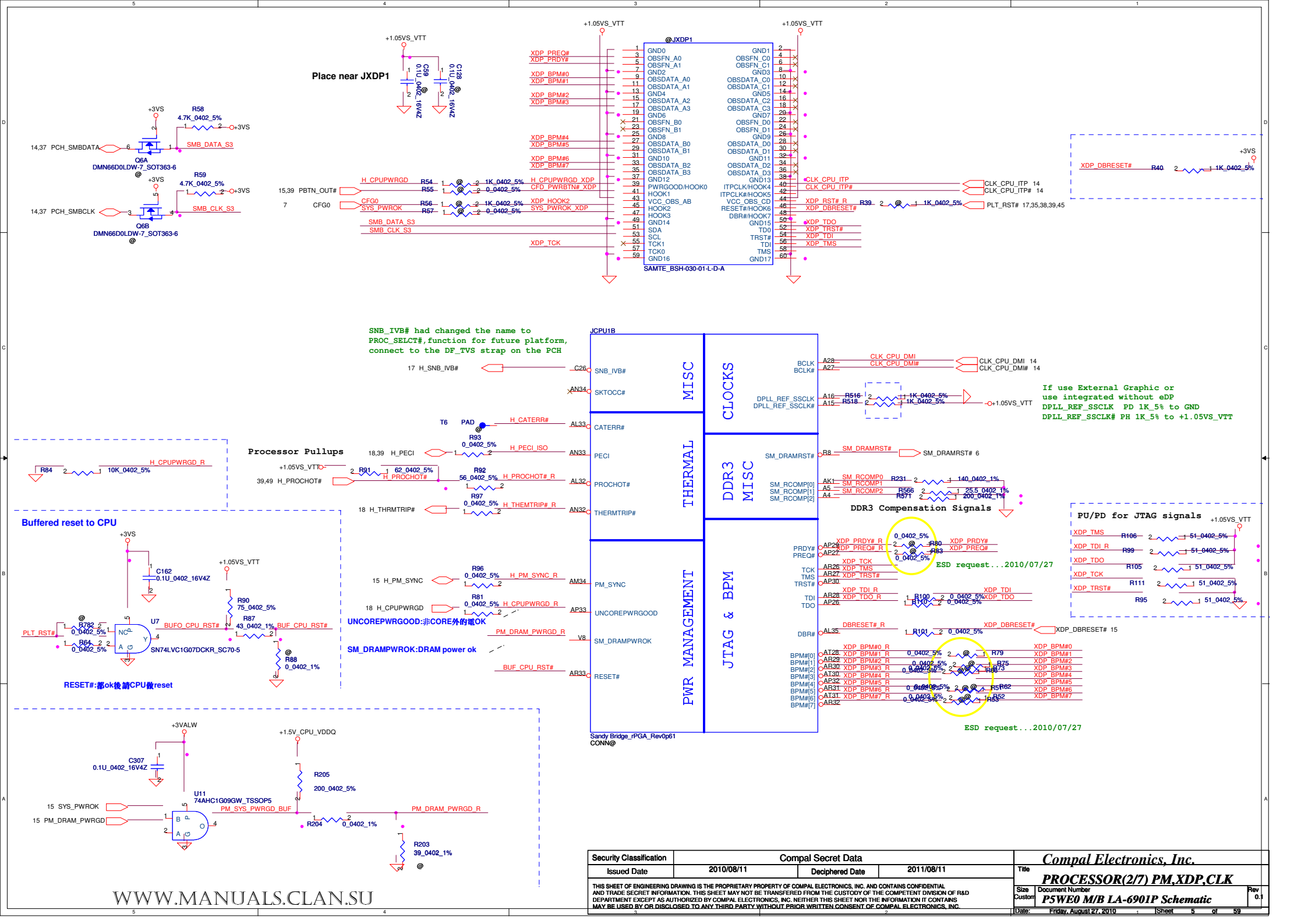


Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 Sheet 4 of 59



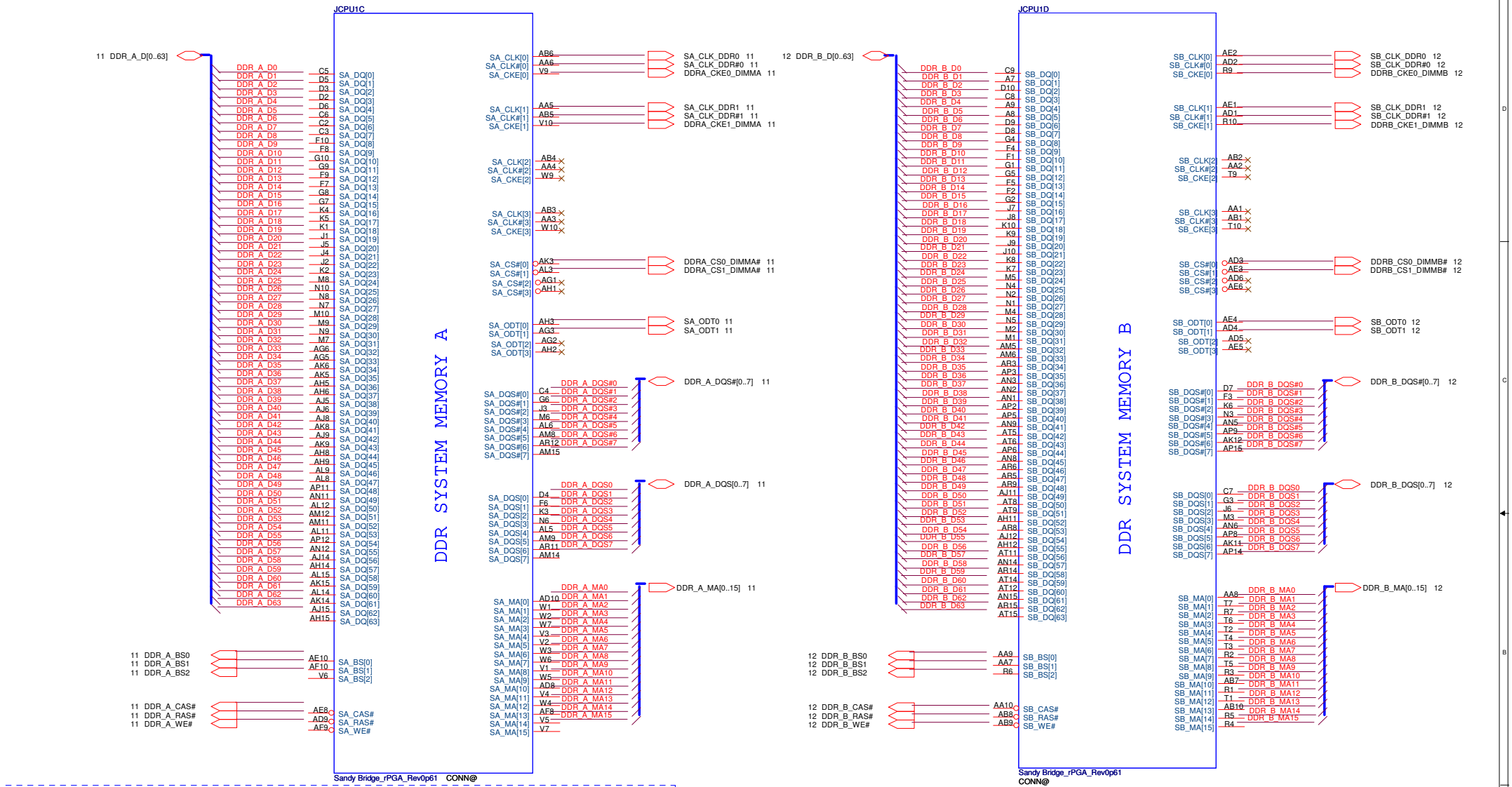
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

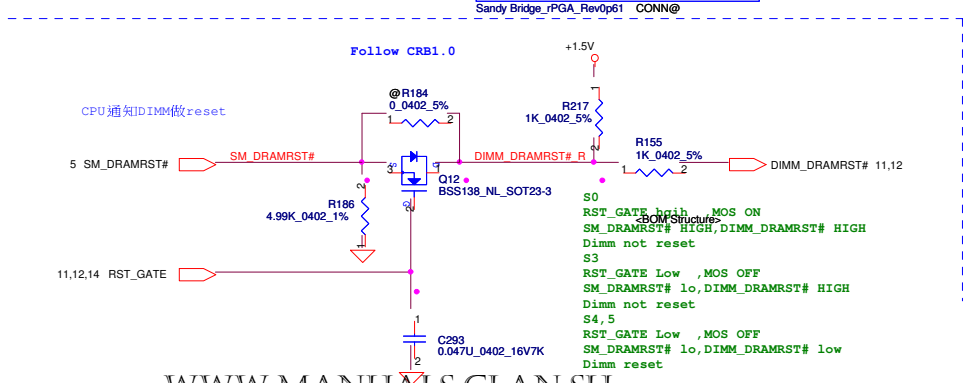
Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 | Sheet 5 of 59





Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

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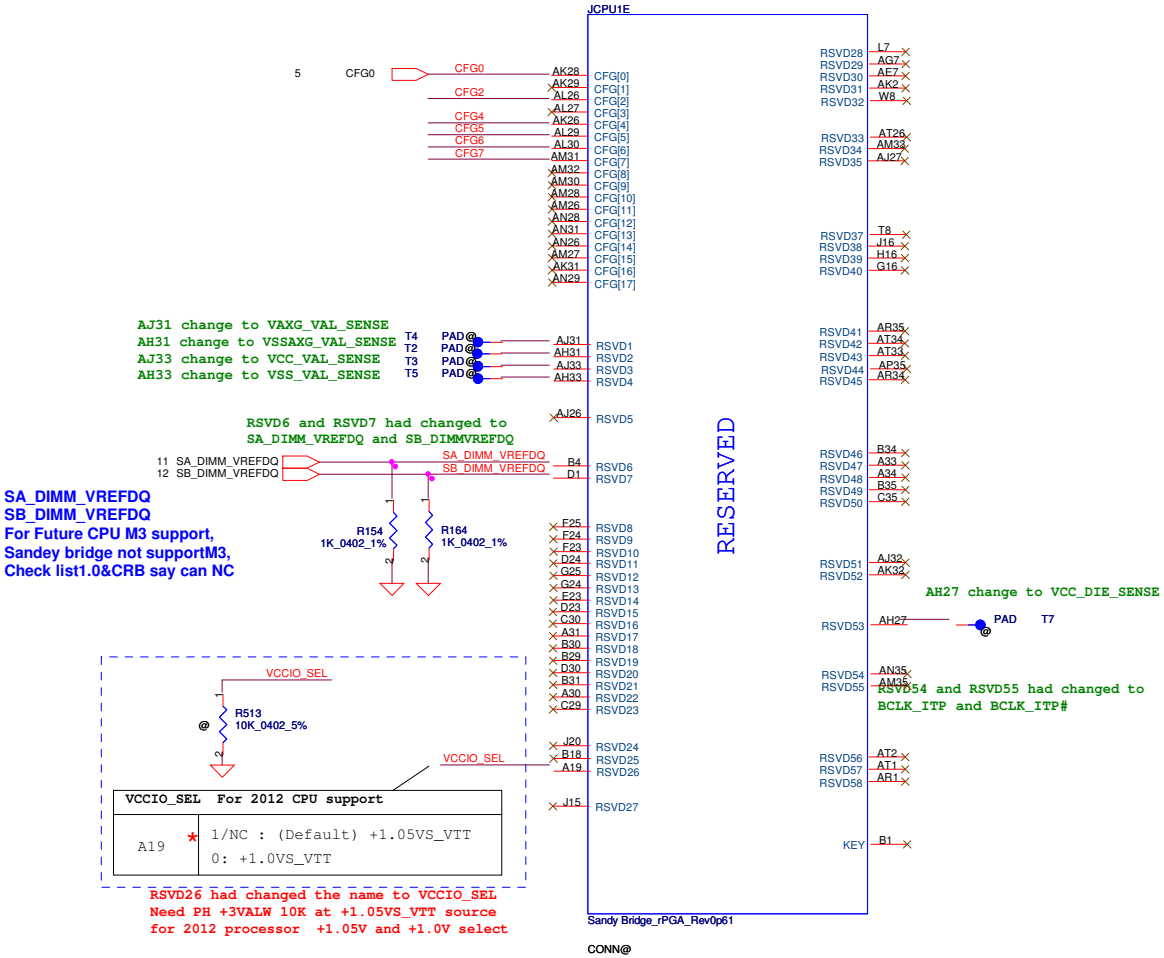
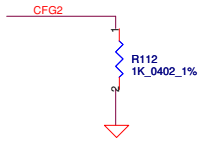
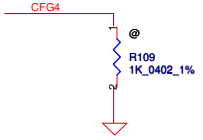
CFG Straps for Processor



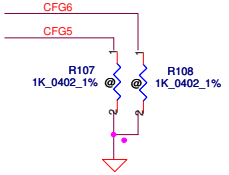
VCCIO_SEL For 2012 CPU support		
A19	*	1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT



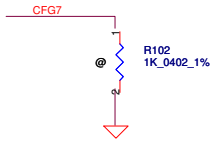
PEG Static Lane Reversal - CFG2 is for the 16x		
CFG2		1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap		
CFG4	*	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps		
CFG[6:5]	*	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING		
CFG7		1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 7 of 59

POWER

SV type CPU

QC 94A
DC 53A

JCPU1F

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

8.5A

INTEL Recommend
2*330uF,12*22uF
from PDDG 1.0

INTEL Recommend
4*470uF,16*22uF and 10*10uF
from PDDG 1.0

Follow Power Suggestion ,
place 3-pin Cap for CPU_CORE

PAW00
use 470uF*2
330uF*3

Place the PU
resistors close to VR

Place the PU
resistors close to CPU

change to
VSS_SENSE_VCCIO

Should change to connect form
power cirucit & layout differential
with VCCIO_SENSE.

Sandy Bridge rPGA_Rev0p61

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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POWER

INTEL Recommend
2*470uF,12*22uF
from PDDG 1.0

QC 33A
DC 26A

+VGFX_CORE

R151
0_0402_5%
DISO@

UMA@ 22U_0805_6.3V6M C611
UMA@ 22U_0805_6.3V6M C625
UMA@ 22U_0805_6.3V6M C212
UMA@ 22U_0805_6.3V6M C272
UMA@ 22U_0805_6.3V6M C211
UMA@ 22U_0805_6.3V6M C231
UMA@ 22U_0805_6.3V6M C210
UMA@ 22U_0805_6.3V6M C209
UMA@ 22U_0805_6.3V6M C274
UMA@ 22U_0805_6.3V6M C271
UMA@ 22U_0805_6.3V6M C242
UMA@ 22U_0805_6.3V6M C275
UMA@ 330U_D2_2V_Y C646
UMA@ 330U_D2_2V_Y C645
@ 22U_0805_6.3V6M C208
@ 22U_0805_6.3V6M C273
UMA@ 22U_0805_6.3V6M C600
@ 22U_0805_6.3V6M C599

Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

JCPU1G

GRAPHICS

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

SENSE LINES

VAXG_SENSE
VSSAXG_SENSE

AK35 VCC_AXG_SENSE 54
AK34 VSS_AXG_SENSE 54

VREF

SM_VREF AL1

+V_SM_VREF should have 20 mil trace width

+1.5V_CPU_VDDQ

R582 100_0402_1%
R575 100_0402_1%
+V_SM_VREF
C688 0.1U_0402_16V4Z
<BOM Structure>

DDR3 -1.5V RAILS

10A

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P2
VDDQ14 P4
VDDQ15 P1

+1.5V_CPU_VDDQ

10U_0805_6.3V6M C363
10U_0805_6.3V6M C384
10U_0805_6.3V6M C362
10U_0805_6.3V6M C341
10U_0805_6.3V6M C385
10U_0805_6.3V6M C361
330U_D2_2V_Y C355

+1.5V
J1 PAD-OPEN 4x4m @
+1.5VS
J2 PAD-OPEN 4x4m @

Short for +1.5VS to +1.5V_1

INTEL Recommend
1*330uF,6*10uF
from PDDG 1.0

INTEL Recommend
1*330uF,3*10uF
from PDDG 1.0

SA RAIL

6A

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

+VCCSA

10U_0805_6.3V6M C214
10U_0805_6.3V6M C605
10U_0805_6.3V6M C219
10U_0603_6.3V6M C213
330U_D2_2V_Y C221

R137 0_0402_5% VCCSA_SENSE
If possible,use os-con cap
if not,use the D2 size
R141 0_0402_5% VSSSA_SENSE 51

MISC

VCCSA_SENSE H23
VCCSA_SENSE 51

VCCSA_VID0
VCCSA_VID1
FC_C22 C22
VCCSA_VID1 C24
FC_C22
change to
VCCSA_VID0

VCCSA_VID1 51

R143 10K_0402_5%
R138 @0_0402_5%

VCCSA				
VID0	VID1	Vout	2011CPU	2012CPU
0	0	0.9V	V	V
0	1	0.8V	V	V
1	0	0.725V	X	V
1	1	0.675V	X	V

1.8V RAIL

1.2A

+1.8VS
R528 0_0805_5%
+1.8VS_VCCPLL

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

330U_D2_2V_Y C664
10U_0805_6.3V6M C655
1U_0402_6.3V6K C654
10U_0402_6.3V6K C653

INTEL Recommend
1*330uF,1*10uF and 2*1uF(0402)
from PDDG 1.0

Sandy Bridge_rPGA_Rev0p61

CONN@

Security Classification	Compal Secret Data		
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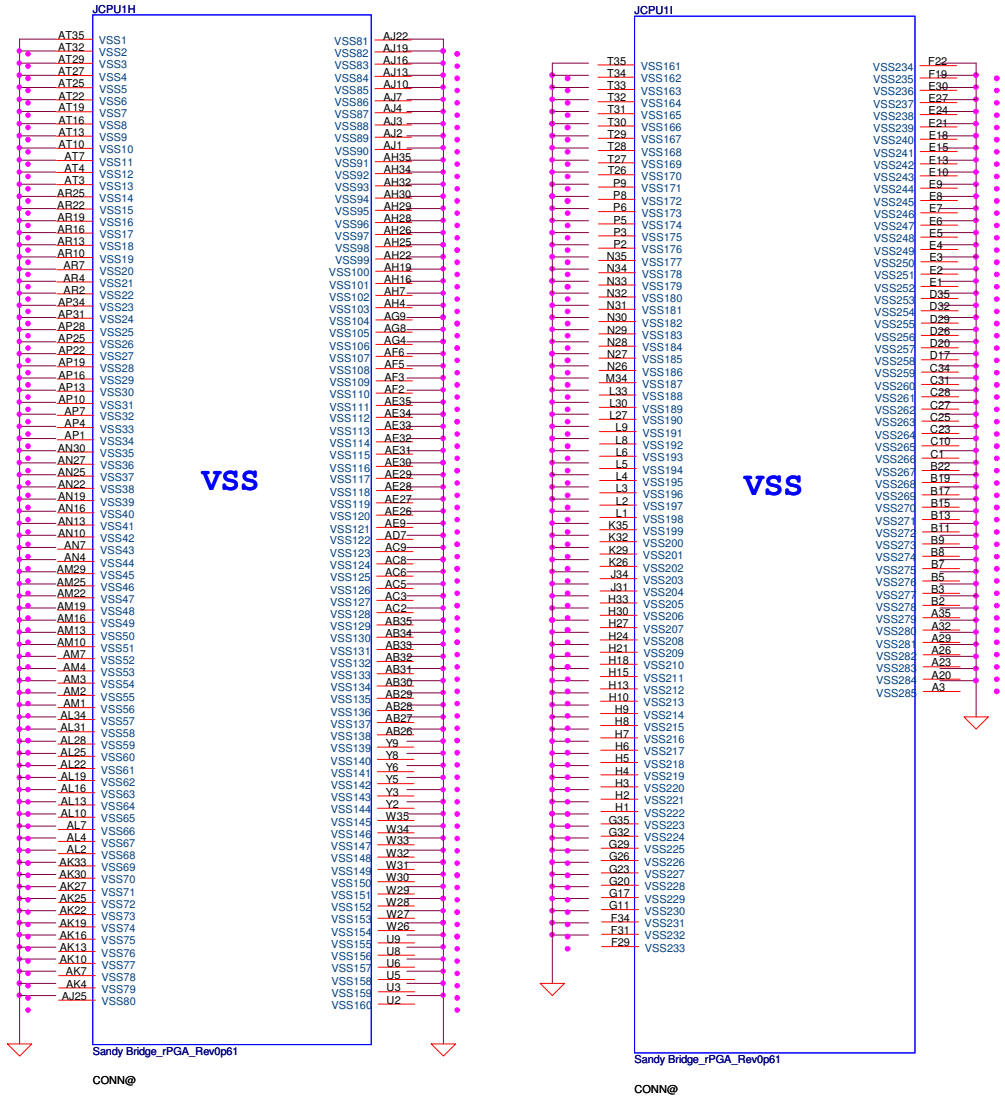
Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 9 of 59



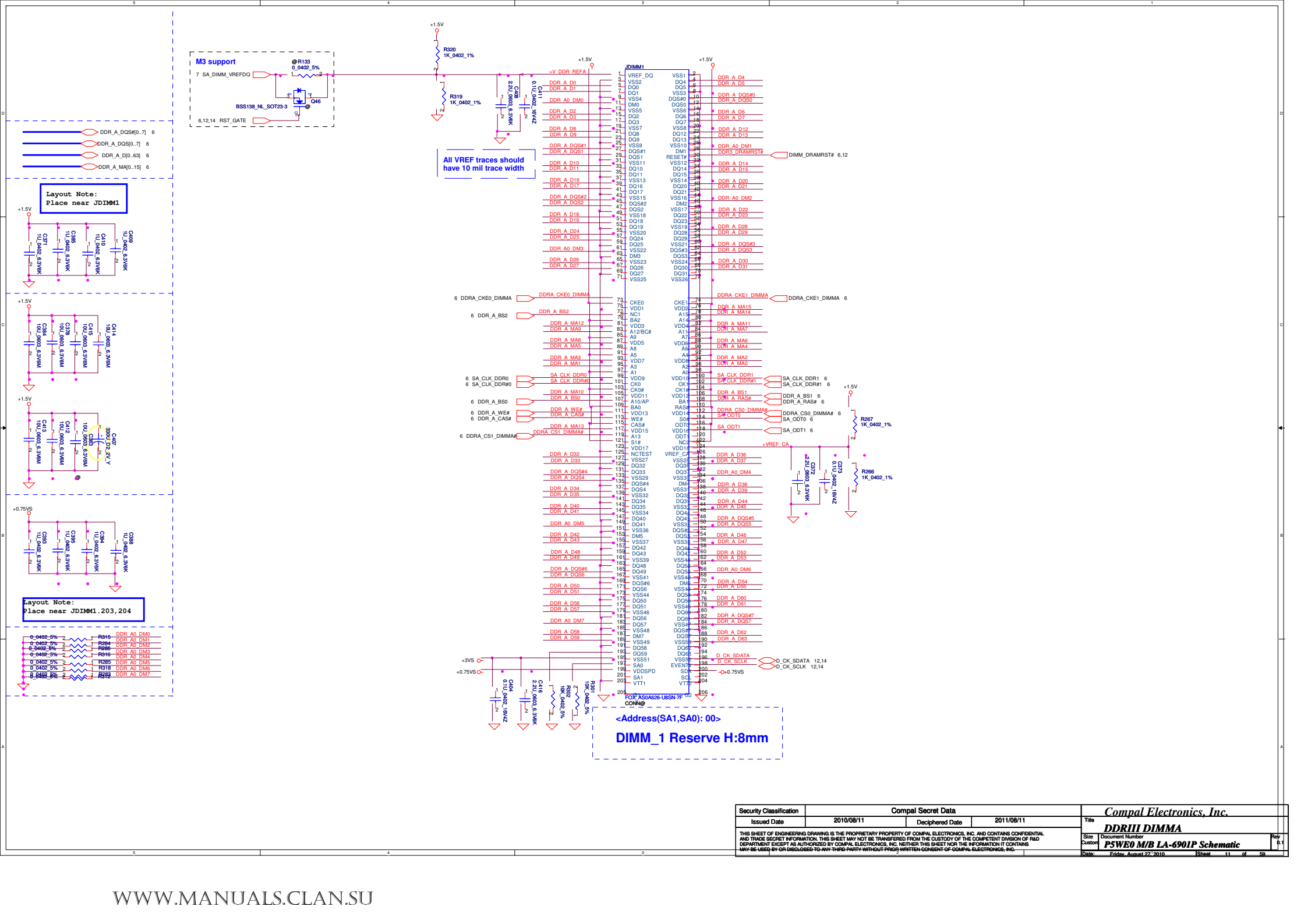
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 | Sheet 10 of 59



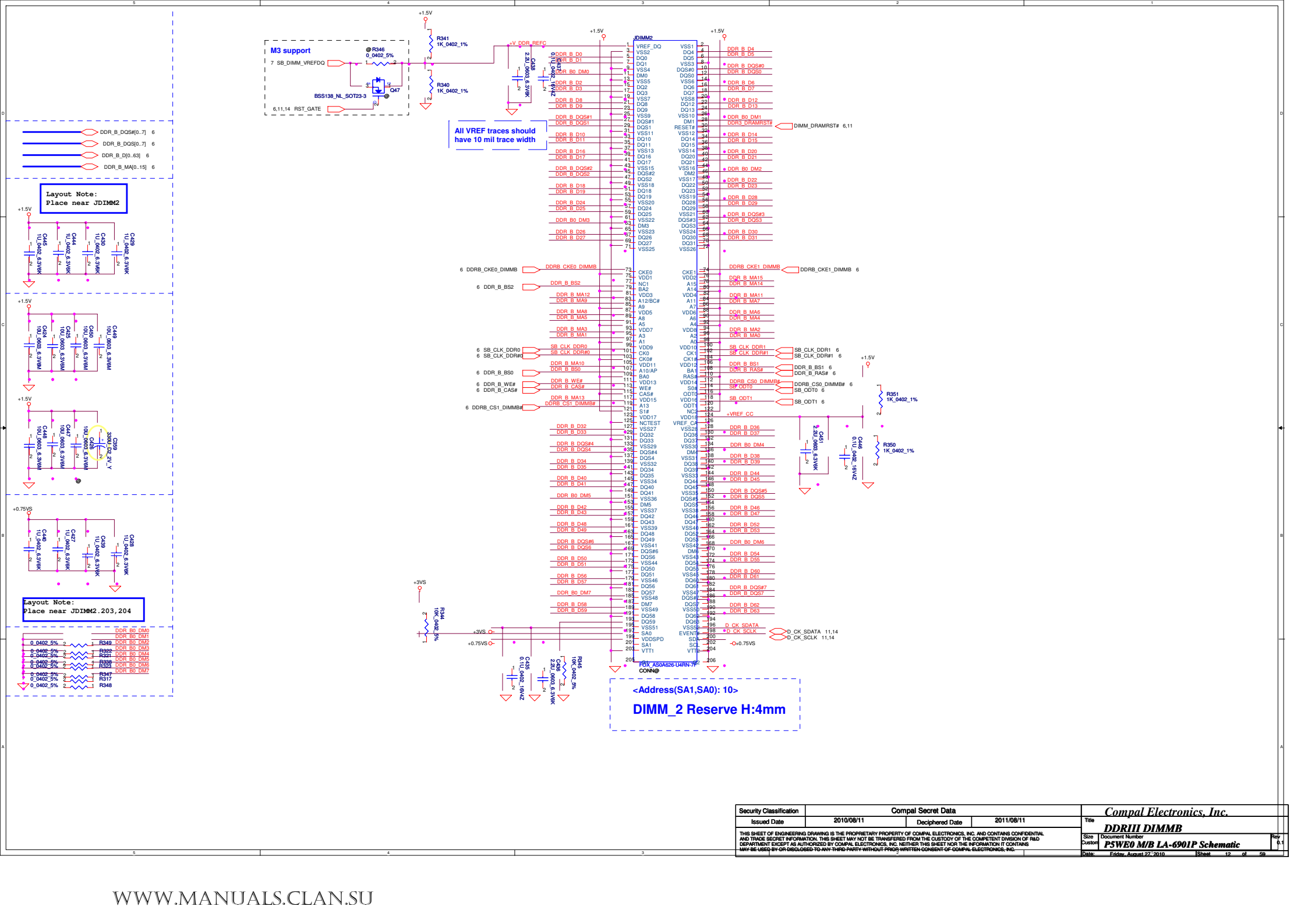
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: DDRIII DIMMA

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 11 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: DDRIII DIMMB

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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PCH_RTCX1
PCH_RTCX2
R568 10M_0402_5%
Y3 32.768KHZ_12.5PF_Q13MC14610002
C682 18P_0402_50V8J
C686 18P_0402_50V8J

+RTCVCC
R567 1M_0402_5% SM_INTRUDER#
R585 330K_0402_5% PCH_INTVRMEN

INTVRMEN

★ H : Integrated VRM enable
L : Integrated VRM disable

(INTVRMEN should always be pull high.)

+3VS
R294 @ 1K_0402_5% PCH_SPKR

HIGH= Enable (No Reboot)
★ LOW= Disable (Default)

+3VALW_PCH
R556 1K_0402_5%
R557 @ 0_0402_5%
39 HDA_SDO
HDA_SDOUT_PCH

HDA_SDO as Capella ME override (GPIO33)

ME debug mode,this signal has a weak internal PD
★ Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3VALW_PCH
R539 1K_0402_5% HDA_SYNC_PCH

This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
★ 1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

R544 33_0402_5%
41 HDA_BITCLK_AUDIO HDA_BITCLK_PCH
R542 33_0402_5%
41 HDA_SYNC_AUDIO HDA_SYNC_PCH_R
R545
41 HDA_RST_AUDIO# 33_0402_5% HDA_RST_PCH#
R555
41 HDA_SDOUT_AUDIO 33_0402_5% HDA_SDOUT_PCH

+3VALW_PCH
R666 200_0402_5% PCH_JTAG_TDO
R637 200_0402_5% PCH_JTAG_TMS
R646 200_0402_5% PCH_JTAG_TDI
R671 100_0402_1%
R636 100_0402_1%
R648 100_0402_1%

+RTCBATT
+CHGRTC
R375 1K_0402_5%
+RTCBATT_R
20mil
D13 DAN202UT106_SC70-3
+RTCVCC
20mil
C471 0.1U_0402_16V4Z

RTCRST close RAM door

+RTCVCC
C360 1U_0603_10V6K
R248 20K_0402_5%
R243 20K_0402_5%
C356 1U_0603_10V6K
J7 0_0603_5% @
J8 0_0603_5% @

SRTCRST close RAM door

Prevent back drive issue.

+3VS
Q36 BSS138_NL_SOT23-3
R540 @ 0_0402_5%

+RTCBATT
JBATT1
CONN@ SUYIN_060003HA002G202ZL

U33A

PCH_RTCX1	A20	RTCX1	RTC	FWH0 / LAD0	C38 LPC_AD0
PCH_RTCX2	C20	RTCX2		FWH1 / LAD1	A38 LPC_AD1
PCH_RTCRST#	D20	RTCRST#		FWH2 / LAD2	B37 LPC_AD2
PCH_SRTCRST#	G22	SRTCRST#		FWH3 / LAD3	C37 LPC_AD3
SM_INTRUDER#	K22	INTRUDER#		FWH4 / LFRAME#	D36 LPC_FRAME#
PCH_INTVRMEN	C17	INTVRMEN		LDRQ0#	E36
				LDRQ1# / GPIO23	K36
				SERIRQ	V5 SERIRQ
HDA_BITCLK_PCH	N34	HDA_BCLK	IHDA	SATA0RXN	AM3
HDA_SYNC_PCH	L34	HDA_SYNC		SATA0RXP	AM1
PCH_SPKR	T10	SPKR		SATA0TXN	AP7
HDA_RST_PCH#	K34	HDA_RST#		SATA0TXP	AP5
HDA_SDIN0	E34	HDA_SDIN0		SATA1RXN	AM10
	G34	HDA_SDIN1		SATA1RXP	AM8
	C34	HDA_SDIN2		SATA1TXN	AP11
	A34	HDA_SDIN3		SATA1TXP	AP10
HDA_SDOUT_PCH	A36	HDA_SDO	SATA	SATA2RXN	AD7
	C36	HDA_DOCK_EN# / GPIO33		SATA2RXP	AD5
	N32	HDA_DOCK_RST# / GPIO13		SATA2TXN	AH5
				SATA2TXP	AH4
				SATA3RXN	AB8
				SATA3RXP	AB10
				SATA3TXN	AF3
				SATA3TXP	AF1
				SATA4RXN	Y7
				SATA4RXP	Y5
				SATA4TXN	AD3
				SATA4TXP	AD1
				SATA5RXN	Y3
				SATA5RXP	Y1
				SATA5TXN	AB3
				SATA5TXP	AB1
PCH_JTAG_TCK	J3	JTAG_TCK	JTAG	SATAICOMPO	Y11 SATA_COMP
PCH_JTAG_TMS	H7	JTAG_TMS		SATAICOMPI	Y10
PCH_JTAG_TDI	K5	JTAG_TDI		SATA3RCOMPO	AB12 SATA3_COMP
PCH_JTAG_TDO	H1	JTAG_TDO		SATA3COMPI	AB13
PCH_SPI_CLK	T3	SPI_CLK	SPI	SATA3RBIAS	AH1 RBIAS_SATA3
PCH_SPI_CS0#	Y14	SPI_CS0#		SATALED#	P3 PCH_SATALED#
	T1	SPI_CS1#		SATA0GP / GPIO21	V14 SGEN#
PCH_SPI_MOSI	V4	SPI_MOSI		SATA1GP / GPIO19	P1 PCH_GPIO19
PCH_SPI_MISO	U3	SPI_MISO			

COUGARPOINT_FCBGA989-D

R674 51_0402_5% PCH_JTAG_TCK
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO

PCH_SPI_CLK_1 R681 0_0402_5% PCH_SPI_CLK
PCH_SPI_CS0#_1 R651 0_0402_5% PCH_SPI_CS0#
PCH_SPI_MOSI_1 PCH_SPI_MOSI
PCH_SPI_MISO_1 R684 0_0402_5% PCH_SPI_MISO
R652 0_0402_5%

+3VS R654 3.3K_0402_5% PCH_SPI_CS0#_1
R667 3.3K_0402_5% SPI_WP1#
SPI_HOLD1#

U36
1 CS# VCC 8 PCH_SPI_CLK_1
3 WP# SCLK 6 PCH_SPI_MOSI_1
7 HOLD# SI 5 PCH_SPI_MISO_1
4 GND SO 2
MX25L3205DM2I-12G SOP 8P

SPI ROM 4 OPTIONS (4MB)
Footprint 200mil

SERIRQ R275 10K_0402_5%
PCH_SATALED# R640 10K_0402_5%
PCH_GPIO19 R624 10K_0402_5%
+3VS

HDD: SATA_PRX_DTX_N0 34, SATA_PRX_DTX_P0 34, SATA_PTX_DRX_N0 34, SATA_PTX_DRX_P0 34
ODD: SATA_PRX_DTX_N2 34, SATA_PRX_DTX_P2 34, SATA_PTX_DRX_N2 34, SATA_PTX_DRX_P2 34

R260 37.4_0402_1% +1.05VS_PCH
R241 49.9_0402_1% +1.05VS_PCH
R625 750_0402_1%
R655 ?_0402_5% +3VALW_PCH
GPIO19 has internal ?? 0402_5%

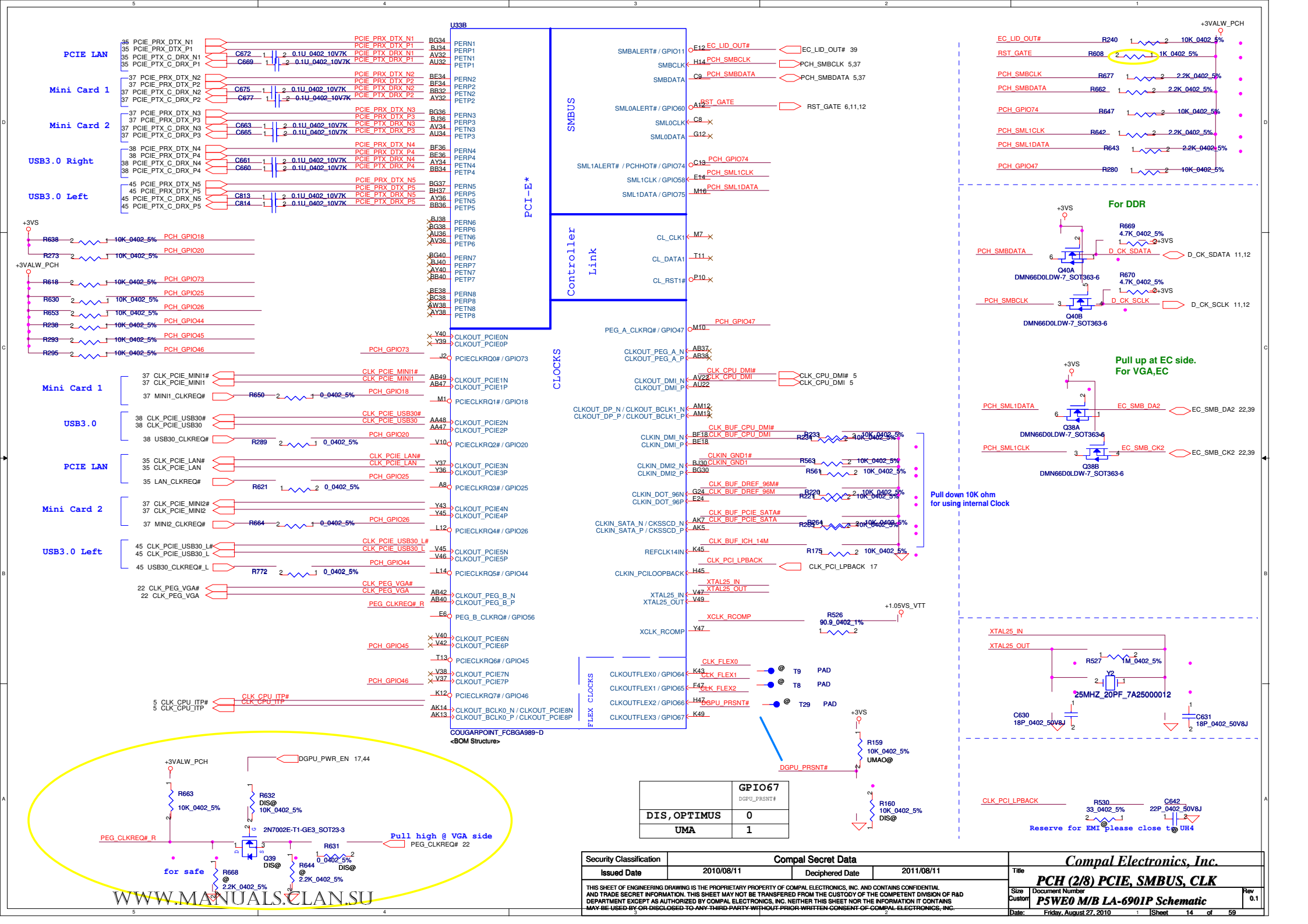
+3VS
SGEN# R259 10K_0402_5%
R258 10K_0402_5% @

	GPIO21 SGEN#
Switchable GPU	0
*Non-Switchable	1

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.
Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1
Date: Friday, August 27, 2010 | Sheet 13 of 59



	GPIO67 DGPU_PRSNT#
DIS,OPTIMUS	0
UMA	1

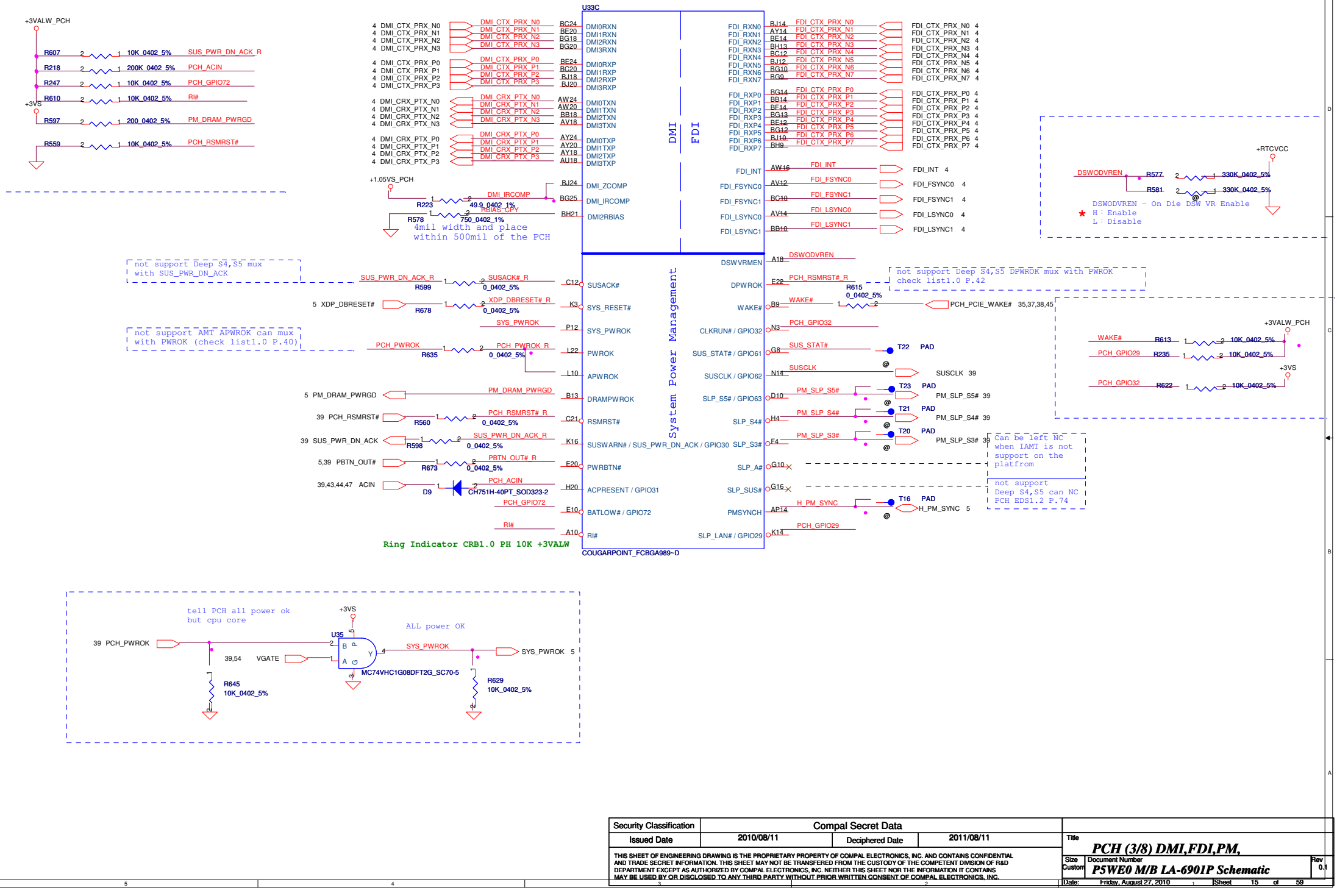
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

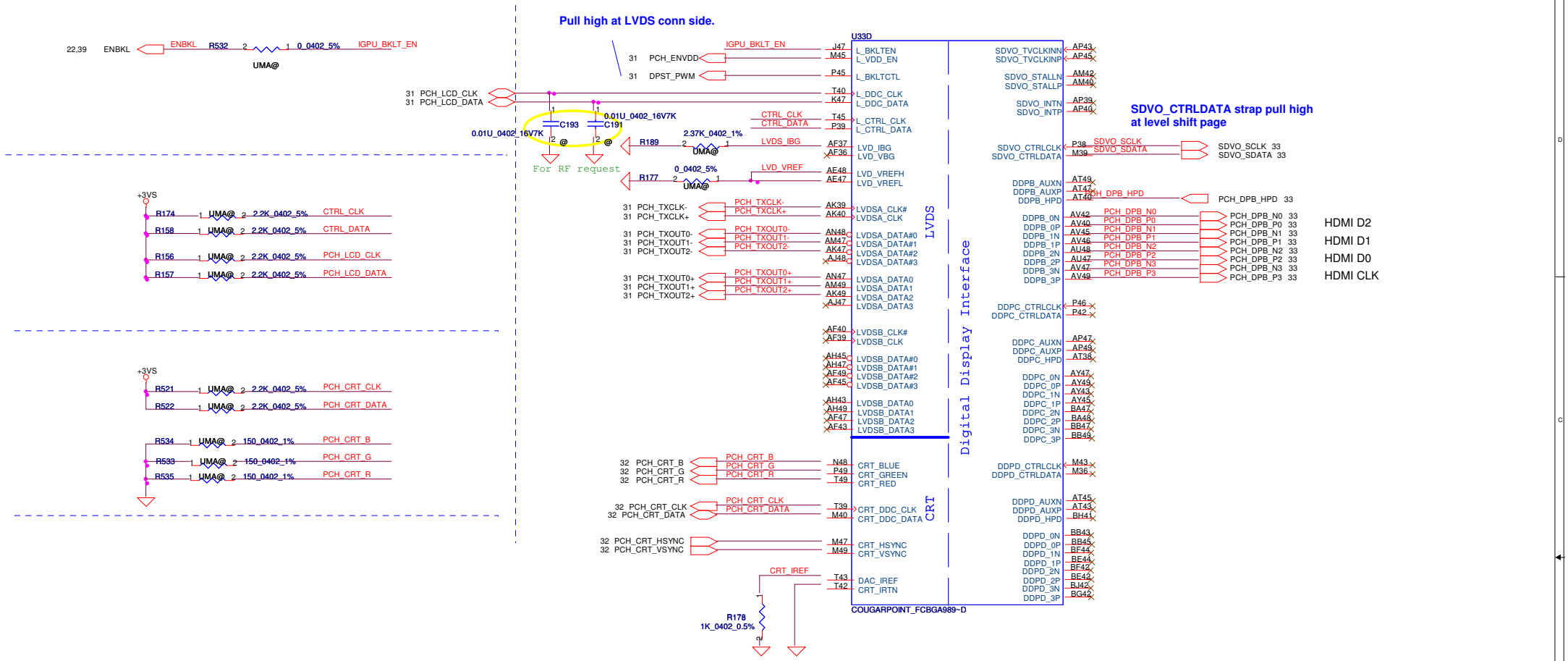
Date: Friday, August 27, 2010 | Sheet 14 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Title	PCH (3/8) DMI,FDI,PM,		
Size: Custom	Document Number: P5WE0 M/B LA-6901P Schematic		Rev: 0.1
Date: Friday, August 27, 2010		Sheet 15 of 59	

Compal Electronics, Inc.



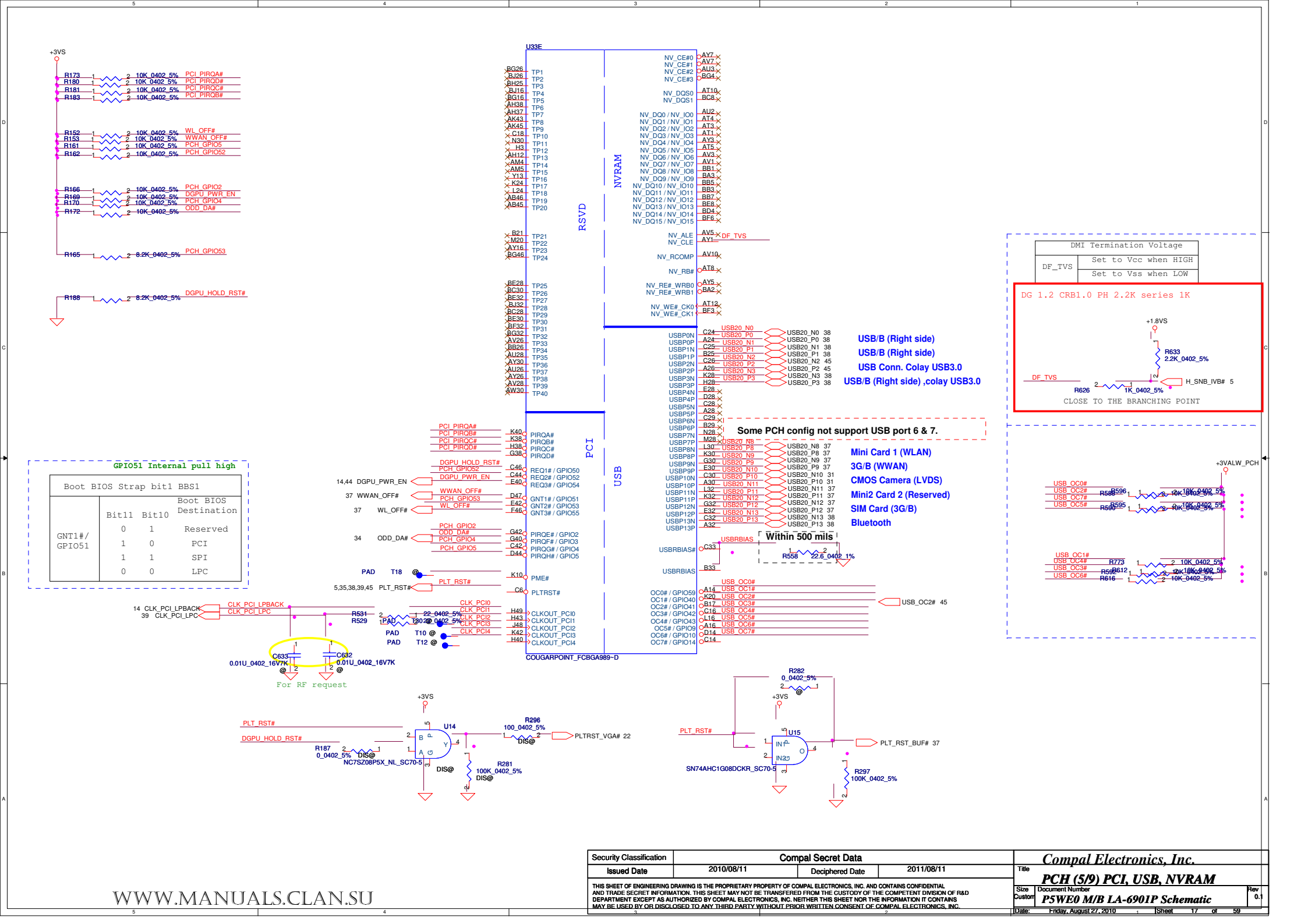
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 Sheet 16 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 17 of 59

HDA_SYNC PH(PLL =+1.5VS)

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R272 1 @ 2 1K_0402_5% PCH_GPIO28
+3VALW_PCH R768 1 2 4.7K_0402_5%

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

R661 1 2 10K_0402_5% PCH_GPIO27

+3VS
R623 2 1 1K_0402_5% OPTIMUS_EN#
NOPT@
R639 2 1 100K_0402_5%
OPT@

	GPIO38 OPTIMUS_EN#
* OPTIMUS	0
Non-OPTIMUS	1

+3VS
R277 1 2 100K_0402_5% PCH_GPIO37
R276 1 2 10K_0402_5% PCH_GPIO0
R546 1 2 10K_0402_5% PCH_GPIO1
R191 1 2 10K_0402_5% DGPU_HPD_INT#
R641 1 2 10K_0402_5% PCH_GPIO16
R194 1 2 10K_0402_5% DGPU_PWROK
R290 1 2 10K_0402_5% PCH_GPIO22
R649 1 2 10K_0402_5% PCH_GPIO39
R291 1 2 100K_0402_5% ODD_DETECT#
R619 1 2 10K_0402_5% BT_ON#
R292 1 2 10K_0402_5% PCH_GPIO48
R274 1 2 10K_0402_5% PCH_GPIO49

+3VALW_PCH
R262 1 2 10K_0402_5% PCH_GPIO24
R620 1 2 10K_0402_5% PCH_GPIO12
R672 1 2 1K_0402_5% SMIB
R263 1 2 10K_0402_5% PCH_GPIO57

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

CRB1.0 PH10K to +3VALW

U33F

PCH_GPIO0 T7 BMBUSY# / GPIO0
PCH_GPIO1 A42 TACH1 / GPIO1
33 DGPU_HPD_INT# DGPU_HPD_INT# H36 TACH2 / GPIO6
39 EC_SCI# EC_SCI# E38 TACH3 / GPIO7
39 EC_SMI# EC_SMI# C10 GPIO8
PCH_GPIO12 C4 LAN_PHY_PWR_CTRL / GPIO12
38,45 SMIB SMIB G2 GPIO15
PCH_GPIO16 U2 SATA4GP / GPIO16
53 VGA_PWROK R193 1 2 0_0402_5% DGPU_PWROK D40 TACH0 / GPIO17
PCH_GPIO22 T5 SCLOCK / GPIO22
PCH_GPIO24 E8 GPIO24 / MEM_LED
PCH_GPIO27 E16 GPIO27
PCH_GPIO28 P8 GPIO28
37,38 BT_ON# BT_ON# K1 STP_PCI# / GPIO34
K4 GPIO35
34 ODD_DETECT# ODD_DETECT# V8 SATA2GP / GPIO36
PCH_GPIO37 M5 SATA3GP / GPIO37
OPTIMUS_EN# N2 SLOAD / GPIO38
PCH_GPIO39 M3 SDATAOUT0 / GPIO39
PCH_GPIO48 V13 SDATAOUT1 / GPIO48
PCH_GPIO49 V3 SATA5GP / GPIO49
PCH_GPIO57 D6 GPIO57

GPIO

TACH4 / GPIO68 C40 ODD_EN# ODD_EN# 34
TACH5 / GPIO69 B41 PCH_GPIO69
TACH6 / GPIO70 C41 PCH_GPIO70
TACH7 / GPIO71 A40 PCH_GPIO71

CPU/MISC

A20GATE P4 GATEA20 39
PECI AU16 PCH_PECI_R 1 2 0_0402_5% R239 H_PECI 5,39
RCIN# P5 EC_KBRST# EC_KBRST# 39
PROCPWRGD AY11 H_CPUPWRGD 5
THRMTRIP# AY10 PCH_THRMTRIP#_R 1 R627 2 390_0402_5% H_THRMTRIP# H_THRMTRIP# 5
INIT3_3V# T14

NC_1 AH8
NC_2 AK11
NC_3 AH10
NC_4 AK10
NC_5 P37

NCTF

PAD T61 A4 VSS_NCTF_1
PAD T46 A44 VSS_NCTF_2
PAD T44 A45 VSS_NCTF_3
PAD T41 A46 VSS_NCTF_4
PAD T52 A5 VSS_NCTF_5
PAD T51 A6 VSS_NCTF_6
PAD T64 B3 VSS_NCTF_7
PAD T37 B47 VSS_NCTF_8
PAD T55 BD1 VSS_NCTF_9
PAD T34 BD49 VSS_NCTF_10
PAD T56 BE1 VSS_NCTF_11
PAD T35 BE49 VSS_NCTF_12
PAD T57 BF1 VSS_NCTF_13
PAD T36 BF49 VSS_NCTF_14

VSS_NCTF_15 BG2 T58 PAD
VSS_NCTF_16 BG48 T39 PAD
VSS_NCTF_17 BH3 T59 PAD
VSS_NCTF_18 BH47 T40 PAD
VSS_NCTF_19 BJ4 T60 PAD
VSS_NCTF_20 BJ44 T45 PAD
VSS_NCTF_21 BJ45 T43 PAD
VSS_NCTF_22 BJ46 T42 PAD
VSS_NCTF_23 BJ5 T50 PAD
VSS_NCTF_24 BJ6 T49 PAD
VSS_NCTF_25 C2 T65 PAD
VSS_NCTF_26 C48 T38 PAD
VSS_NCTF_27 D1 T63 PAD
VSS_NCTF_28 D49 T32 PAD
VSS_NCTF_29 E1 T54 PAD
VSS_NCTF_30 F49 T33 PAD
VSS_NCTF_31 F1 T53 PAD
VSS_NCTF_32 F49 T31 PAD

COUGARPOINT_FCBGA989~D
<BOM Structure>

+3VS
ODD_EN# R771 1 2 10K_0402_5%
EC_KBRST# R279 1 2 10K_0402_5%

+3VS
R278 2 1 10K_0402_5%

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130 degree shut sown

INIT3_3V Checklist1.0 P.59
This signal has weak internal PU, can't pull low,leave NC

TS_VSS1~4 PD to GND

+3VS
R554 10K_0402_5% PCH_GPIO69
R548 10K_0402_5% PCH_GPIO70
R550 10K_0402_5% PCH_GPIO71
R553 10K_0402_5%
R549 10K_0402_5%
R551 10K_0402_5%

Project ID	GPIO69	GPIO70	GPIO71
* P5WE0	0	0	0
P7YE0	0	0	0
x	0	1	0
x	0	1	1
x	1	0	0
x	0	0	1
x	0	1	0
x	0	1	1
x	1	0	0
x	1	0	1
x	1	1	0
x	1	1	1

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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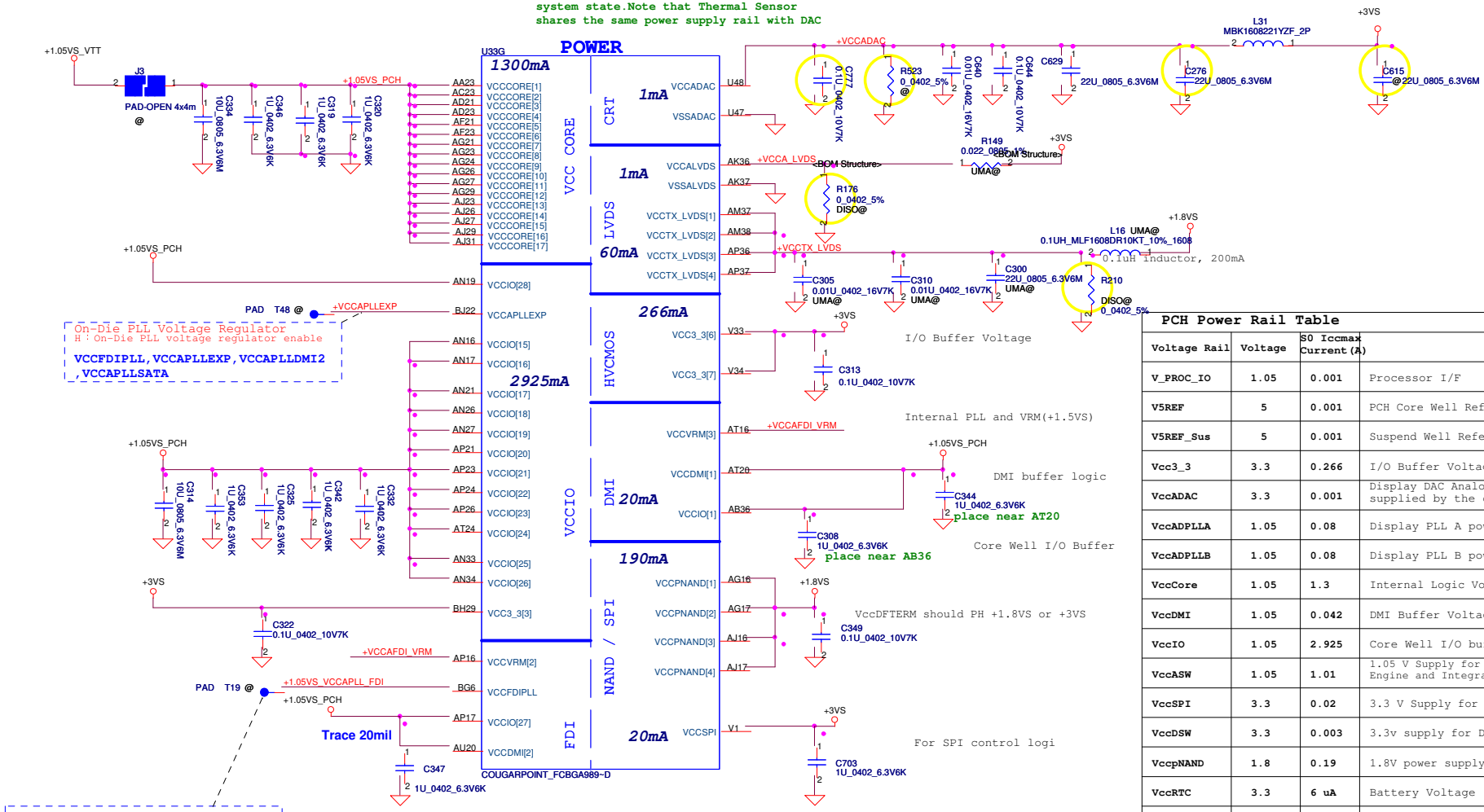
+VCCADAC should be powered up during S0 system state.Note that Thermal Sensor shares the same power supply rail with DAC



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 19 of 59

Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

POWER

U33J

+3VS
R150 0_0805_5%
L14 10UH_LB2012T100MR_20%
+3VS_VCC_CLKF33
C277 10U_0805_10V4Z
C304 1U_0402_6.3V6K

+1.05V analog internal clock PLL Can NC
+1.05VS_PCH
R167 0_0603_5%
+VCCACLK

Not support Deep S4,S5 connect to +3VALW
+3VALW_PCH
C340 0.1U_0402_10V7K

suppied by internal 1.05V VR must NC
PAD T17 @ +PCH_VCCDSW
+3VS_VCC_CLKF33
PAD T11 @ +VCCAPLL_CPY_PCH
+1.05VS_RCH
PAD T13 @ +VCCSUS1

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

+1.05VS_PCH
L12 10UH_LB2012T100MR_20%
+1.05VS_VCCA_A_DPL
C279 220U_B2_2.5VM_R35
C296 1U_0402_6.3V6K
L11 10UH_LB2012T100MR_20%
+1.05VS_VCCA_B_DPL
C278 220U_B2_2.5VM_R35
C295 1U_0402_6.3V6K
SGA00001700
220U 2.5V M B2
ESR 35mohm@100Khz

+1.05VS_PCH
C336 22U_0805_6.3V6M
C335 22U_0805_6.3V6M
C326 1U_0402_6.3V6K
C327 1U_0402_6.3V6K
C316 1U_0402_6.3V6K

C348 0.1U_0402_10V7K
+VCCRTCEXT
+VCCAFDI_VRM
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL

+1.05VS_PCH
C311 1U_0402_6.3V6K Place near AF17
C312 1U_0402_6.3V6K Place near AG33
C317 1U_0402_6.3V6K Place near AF33, AF34,AG34

C354 0.1U_0402_10V7K
+VCCSST
+1.05VM_VCCSUS
PAD T15 @
suppied by internal 1.05V VR Must NC

+1.05VS_PCH
C700 4.7U_0603_6.3V6K
C684 0.1U_0402_10V7K
C693 0.1U_0402_10V7K
Place near BJ8
+RTCVCC
C331 1U_0402_6.3V6K
C685 0.1U_0402_10V7K
C687 0.1U_0402_10V7K

AD49 VCCACLK
T16 VCCDSW3_3
V12 DCPSUSBYP
T38 VCC3_3[5]
BH23 VCCAPLLDMI2
AL29 VCCIO[14]
AL24 DCPSUS[3]

3mA
119mA
1010mA
1mA

AA19 VCCASW[1]
AA21 VCCASW[2]
AA24 VCCASW[3]
AA26 VCCASW[4]
AA27 VCCASW[5]
AA29 VCCASW[6]
AA31 VCCASW[7]
AC26 VCCASW[8]
AC27 VCCASW[9]
AC29 VCCASW[10]
AC31 VCCASW[11]
AD29 VCCASW[12]
AD31 VCCASW[13]
W21 VCCASW[14]
W23 VCCASW[15]
W24 VCCASW[16]
W26 VCCASW[17]
W29 VCCASW[18]
W31 VCCASW[19]
W33 VCCASW[20]

N16 DCPRTC
Y49 VCCVRM[4]
BD47 VCCADPLLA
BF47 VCCADPLLB

80mA
80mA

AF17 VCCIO[7]
AF33 VCCIO[8]
AF34 VCCIO[9]
AG34 VCCIO[11]
AG33 VCCIO[10]

55mA
95mA

V16 DCPSST
T17 DCPSUS[1]
V19 DCPSUS[2]
BJ8 V_PROC_IO
A22 VCCRTC

1mA
10mA

USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA

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N26 VCCIO[29]
P26 VCCIO[30]
P28 VCCIO[31]
T27 VCCIO[32]
T29 VCCIO[33]
+1.05VS_PCH
C321 1U_0402_6.3V6K

T23 VCCSUS3_3[7]
T24 VCCSUS3_3[8]
V23 VCCSUS3_3[9]
V24 VCCSUS3_3[10]
P24 VCCSUS3_3[6]
+3VALW_PCH
C330 0.1U_0402_10V7K Place near +24
C333 0.1U_0402_10V7K Place near +24

T26 VCCIO[34]
+1.05VS_PCH
M26 V5REF_SUS
+PCH_V5REF_SUS
AN23 DCPSUS[4]
+VCCA_USBSUS
AN24 VCCSUS3_3[1]
+3VALW_PCH
@ F14 PAD
Supplied by internal 1.05V VR Must NC

P34 V5REF
+PCH_V5REF_RUN
N20 VCCSUS3_3[2]
+3V_VCCPSUS
N22 VCCSUS3_3[3]
P20 VCCSUS3_3[4]
P22 VCCSUS3_3[5]
+3VALW_PCH
C352 1U_0402_6.3V6K

AA16 VCC3_3[1]
W16 VCC3_3[8]
T34 VCC3_3[4]
+3VS
C704 0.1U_0402_10V7K Place near J2
C343 0.1U_0402_10V7K Place near A16,W16
C309 0.1U_0402_10V7K Place near +24

AJ2 VCC3_3[2]
+1.05VS_PCH
AF13 VCCIO[5]
AH13 VCCIO[12]
AH14 VCCIO[13]
AF14 VCCIO[6]
C350 1U_0402_6.3V6K
<BOM Structure>
AK1 VCCAPLLSATA
+VCCSATAPLL
@ T62 PAD
+VCCAFDI_VRM
AF11 VCCVRM[1]
+VCCAFDI_VRM

AC16 VCCIO[2]
AC17 VCCIO[3]
AD17 VCCIO[4]
+1.05VS_PCH
C351 1U_0402_6.3V6K

T21 VCCASW[22]
+VCCME_22
R237 0_0603_5%
V21 VCCASW[23]
+VCCME_23
R224 0_0603_5%
T19 VCCASW[21]
+VCCME_21
R236 0_0603_5%
+1.05VS_PCH

P32 VCCSUSHDA
+VCCSUSHDA
R206 0_0603_5%
+3VALW_PCH
Need +3VALW and 0.1U close PCH
C315 0.1U_0402_16V4Z

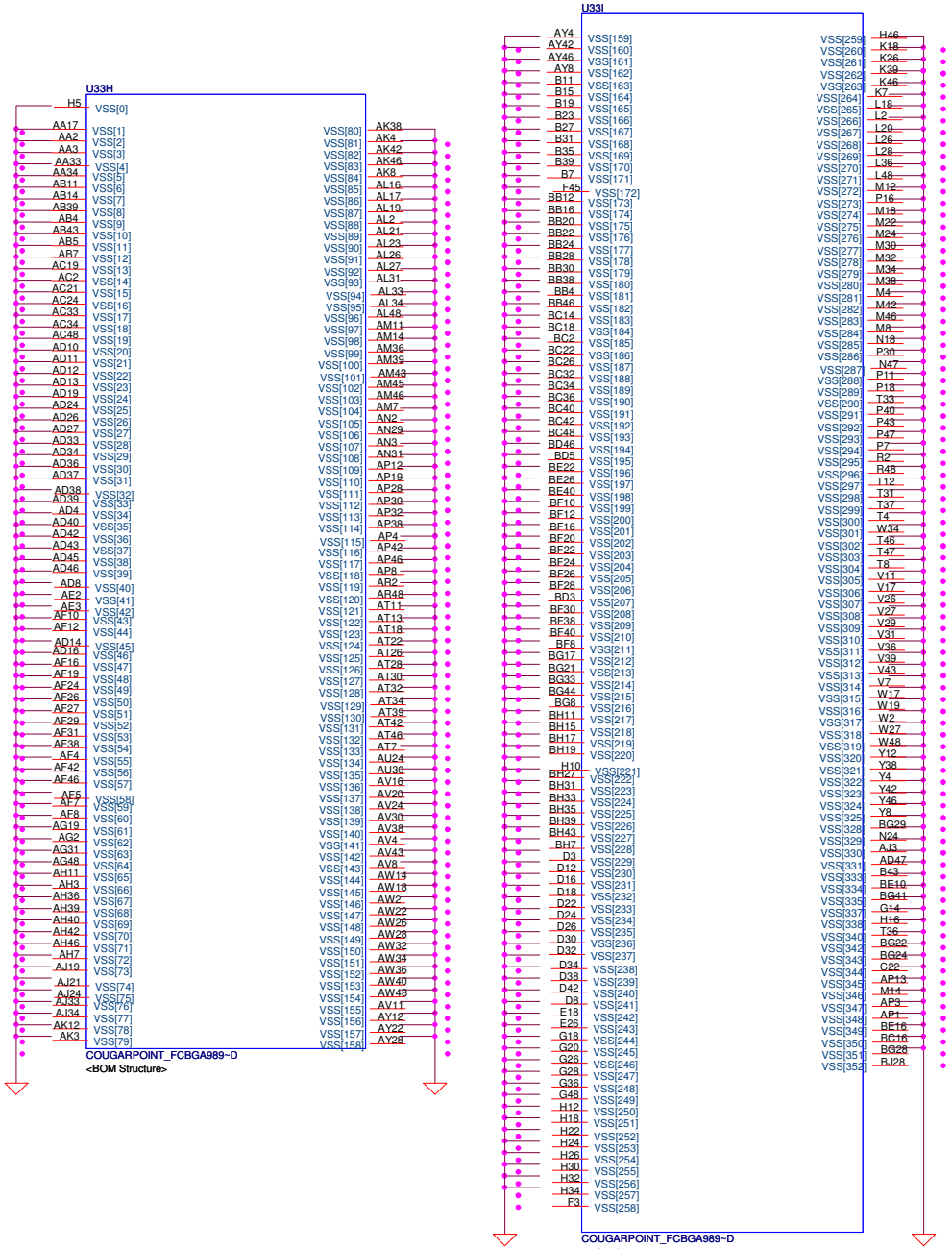
GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

+5VALW_PCH
+3VALW_PCH
R202 100_0402_5%
D8 CH751H-40PT_SOD323-2
+PCH_V5REF_SUS
C318 0.1U_0603_25V7K

+5VS
+3VS
R148 100_0402_5%
D7 CH751H-40PT_SOD323-2
+PCH_V5REF_RUN
C244 1U_0603_10V6K

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.
Title: PCH (8/9) PWR
Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1
Date: Friday, August 27, 2010 | Sheet 20 of 59



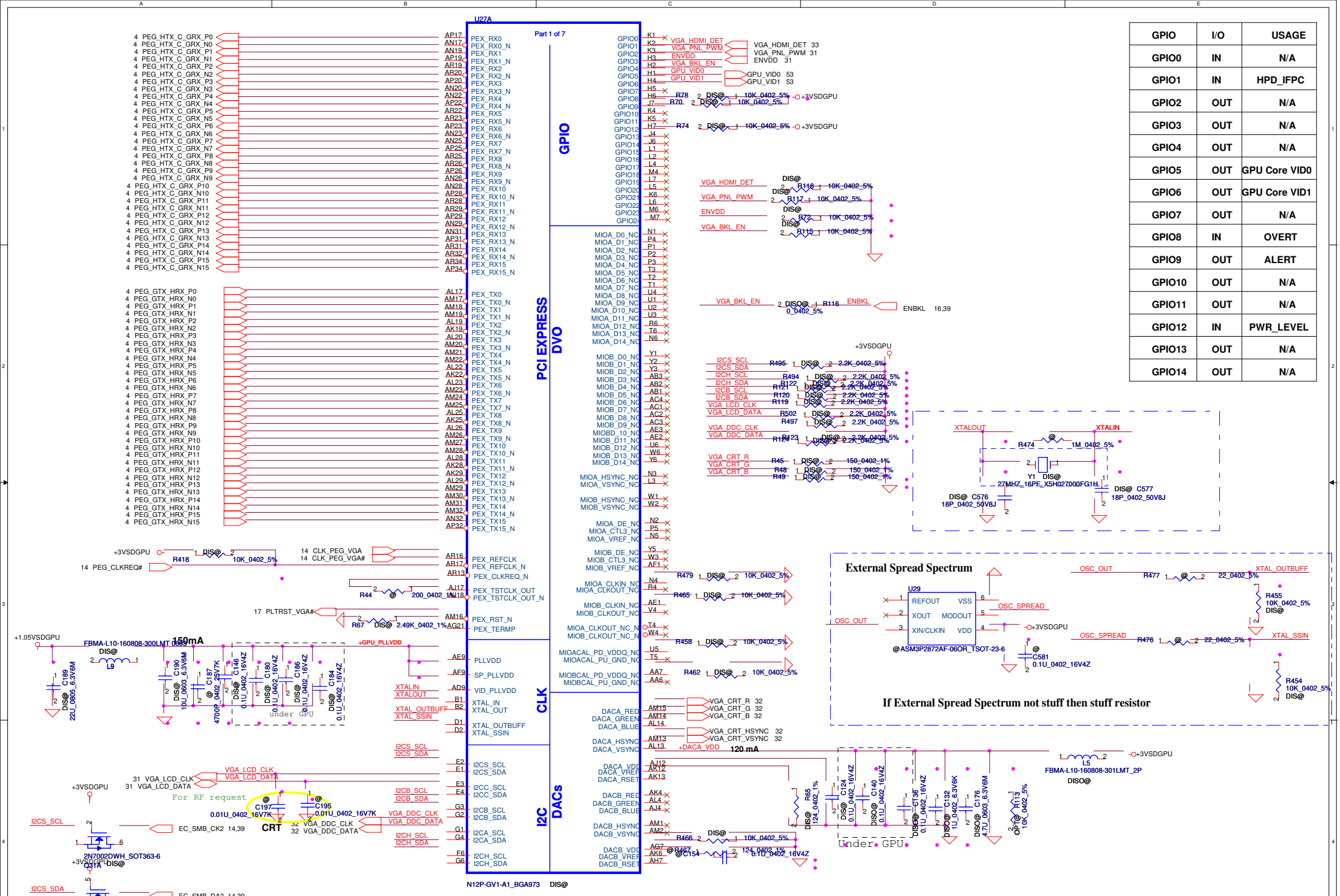
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 Sheet 21 of 59

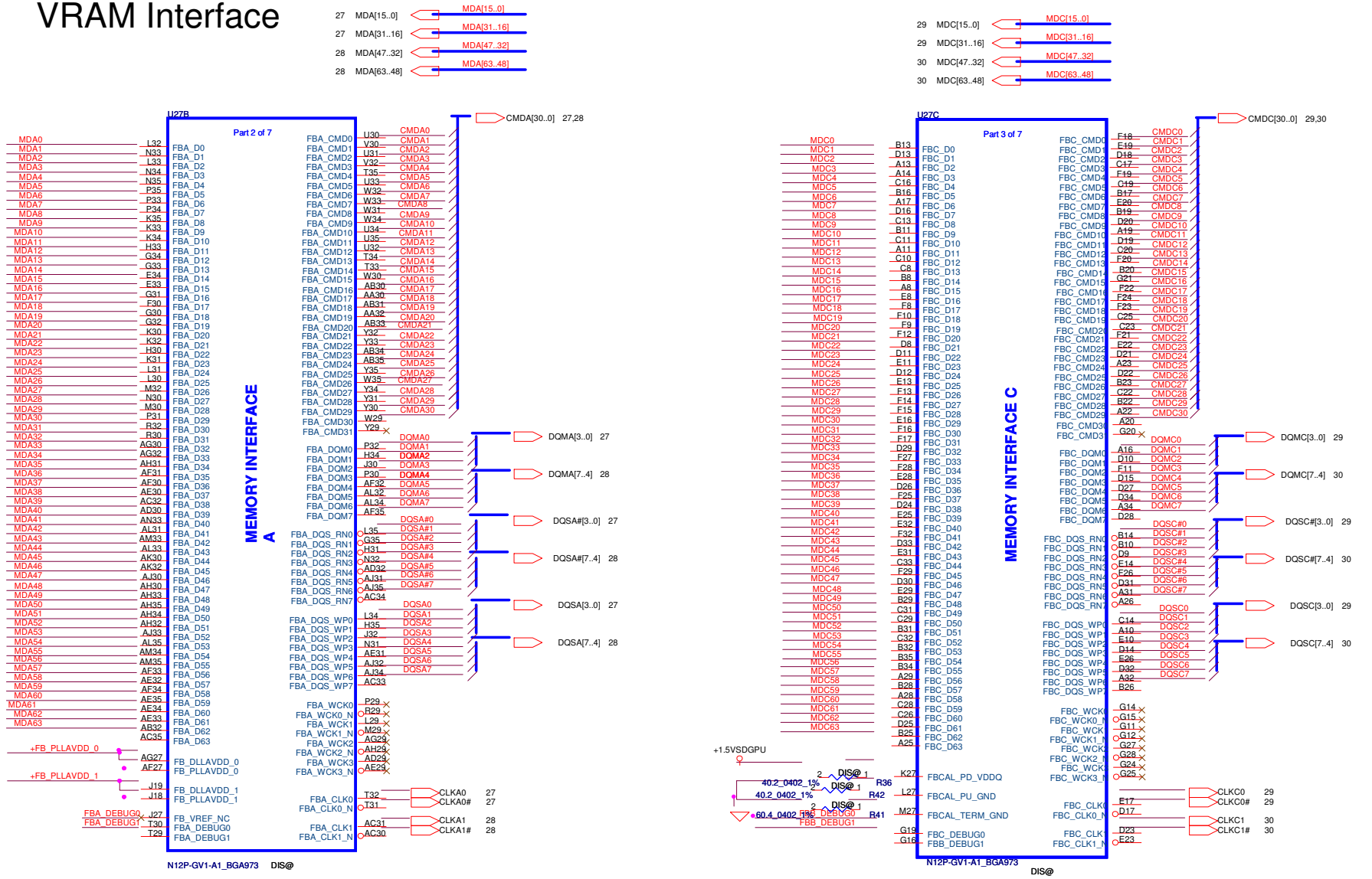


GPIO	I/O	USAGE
GPIO0	IN	N/A
GPIO1	IN	HPD_IFPC
GPIO2	OUT	N/A
GPIO3	OUT	N/A
GPIO4	OUT	N/A
GPIO5	OUT	GPU Core VID0
GPIO6	OUT	GPU Core VID1
GPIO7	OUT	N/A
GPIO8	IN	OVERT
GPIO9	OUT	ALERT
GPIO10	OUT	N/A
GPIO11	OUT	N/A
GPIO12	IN	PWR_LEVEL
GPIO13	OUT	N/A
GPIO14	OUT	N/A

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.			
Title	N12P PEG 1/9		
Size: Custom	Document Number: P5WE0 M/B LA-6901P Schematic		Rev: 0.1
Date: Friday, August 27, 2010		Sheet 22 of 59	

VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: **N12P VRAM 2/9**

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

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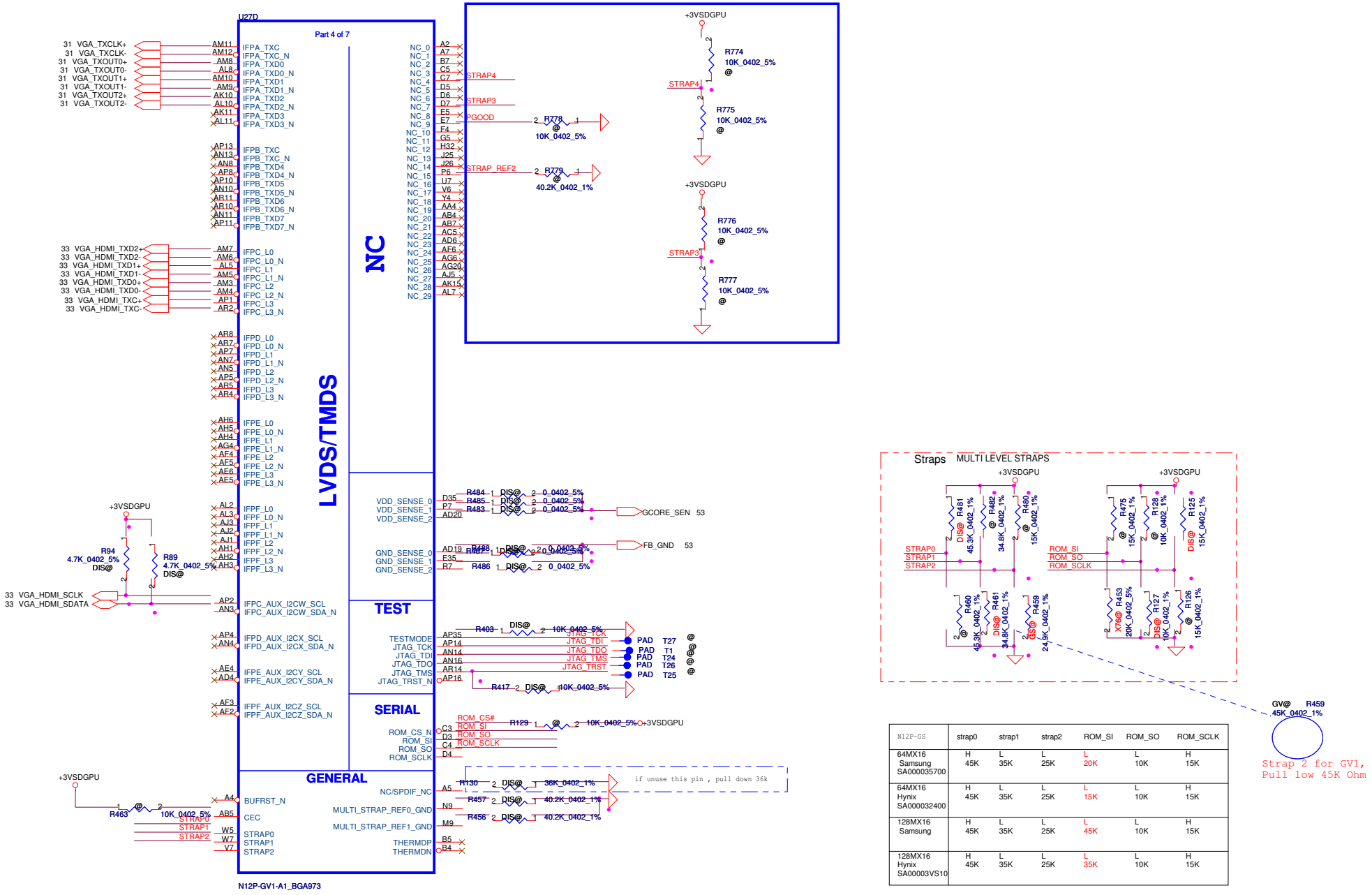
For GB2-128 & GB2b-128 colayout....



GV@ R459 45K_0402_1%

Strap 2 for GV1, Pull low 45K Ohm

N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	L 35K	L 25K	L 20K	L 10K	H 15K
64MX16 Hynix SA000032400	H 45K	L 35K	L 25K	L 15K	L 10K	H 15K
128MX16 Samsung	H 45K	L 35K	L 25K	L 45K	L 10K	H 15K
128MX16 Hynix SA00003VS10	H 45K	L 35K	L 25K	L 35K	L 10K	H 15K

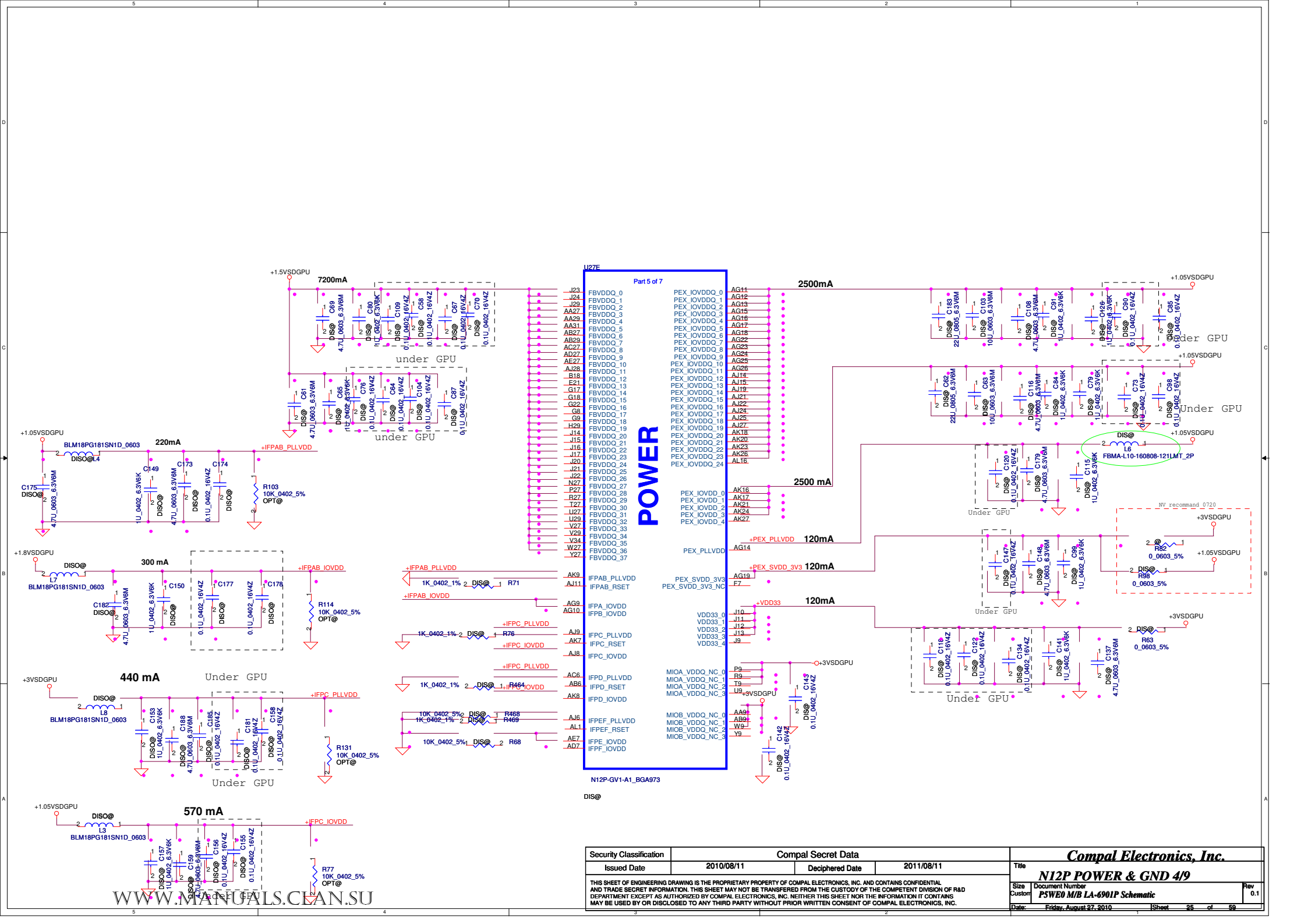
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: N12P LVDS 3/9

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 24 of 59



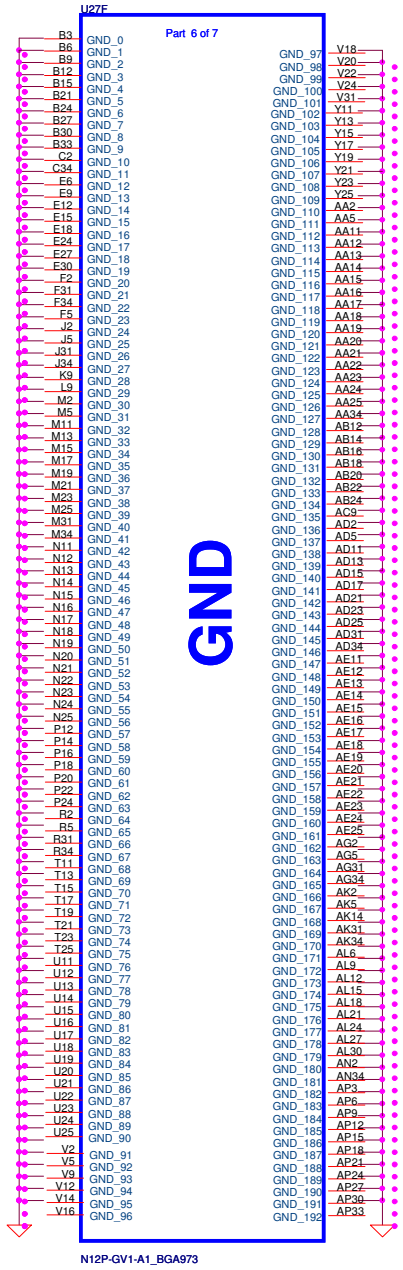
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

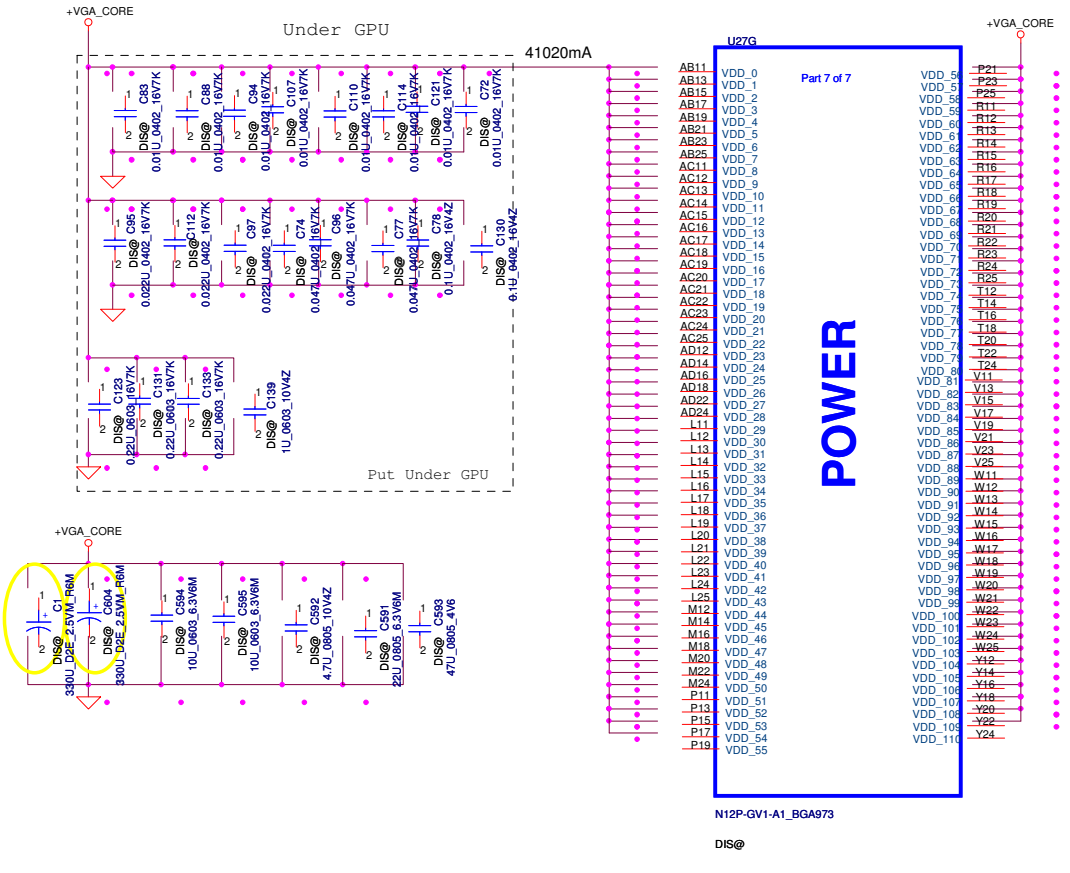
Compal Electronics, Inc.

Title: **N12P POWER & GND 4/9**

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 | Sheet 35 of 59





Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

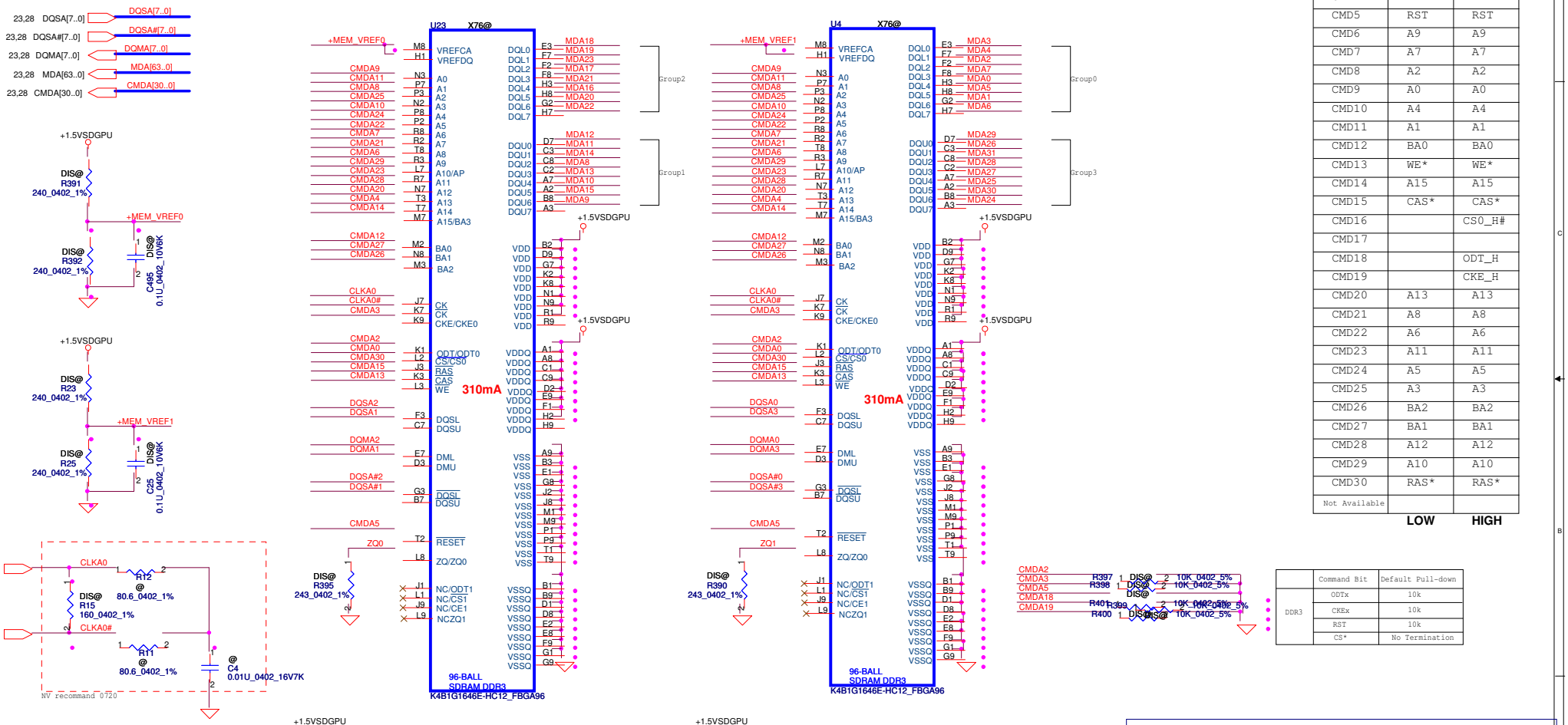
Title: N12P POWER & GND 5/9

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 Sheet 26 of 59

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

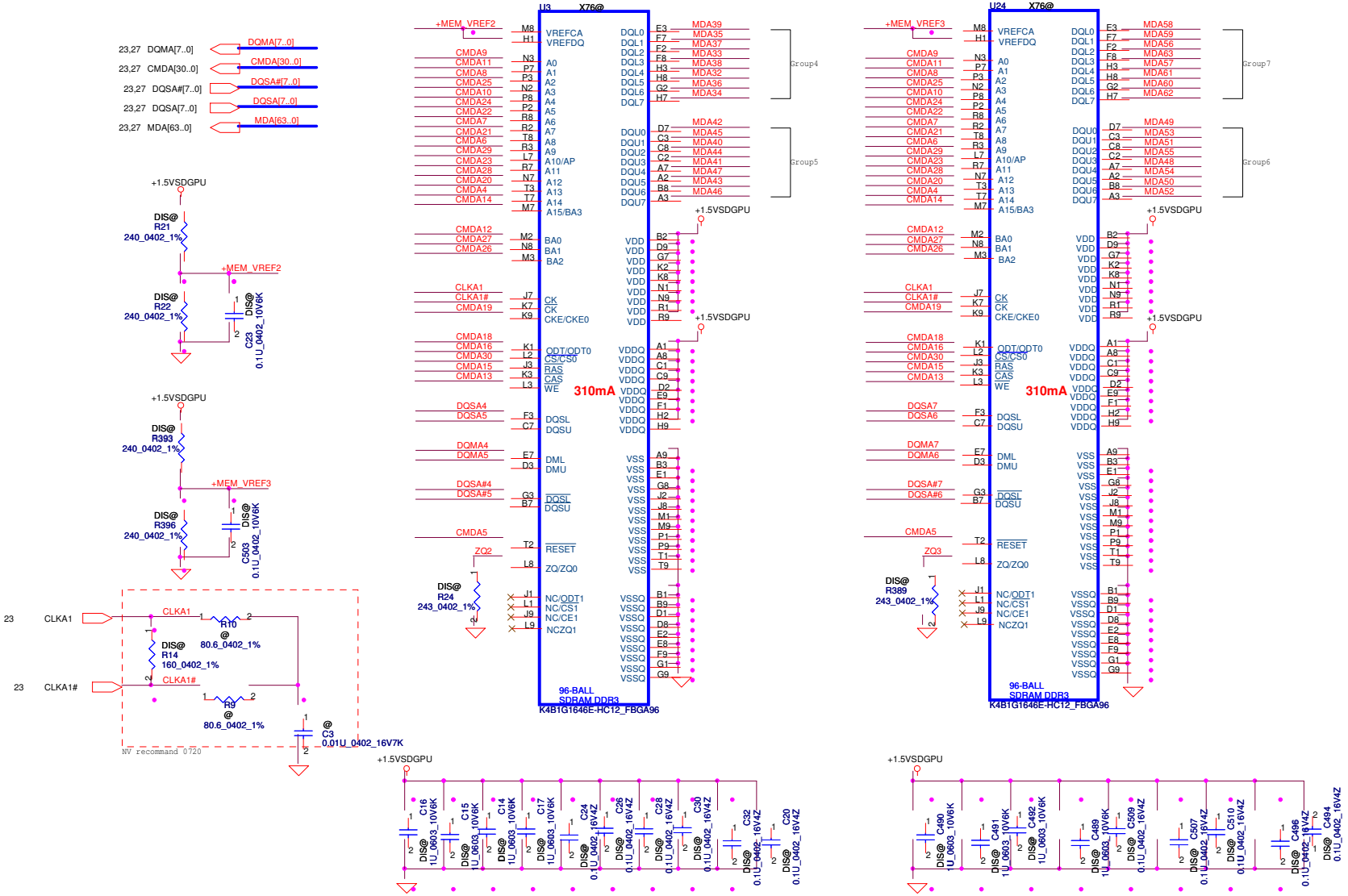
Title: N12P DDR3 6/9

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 27 of 59

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

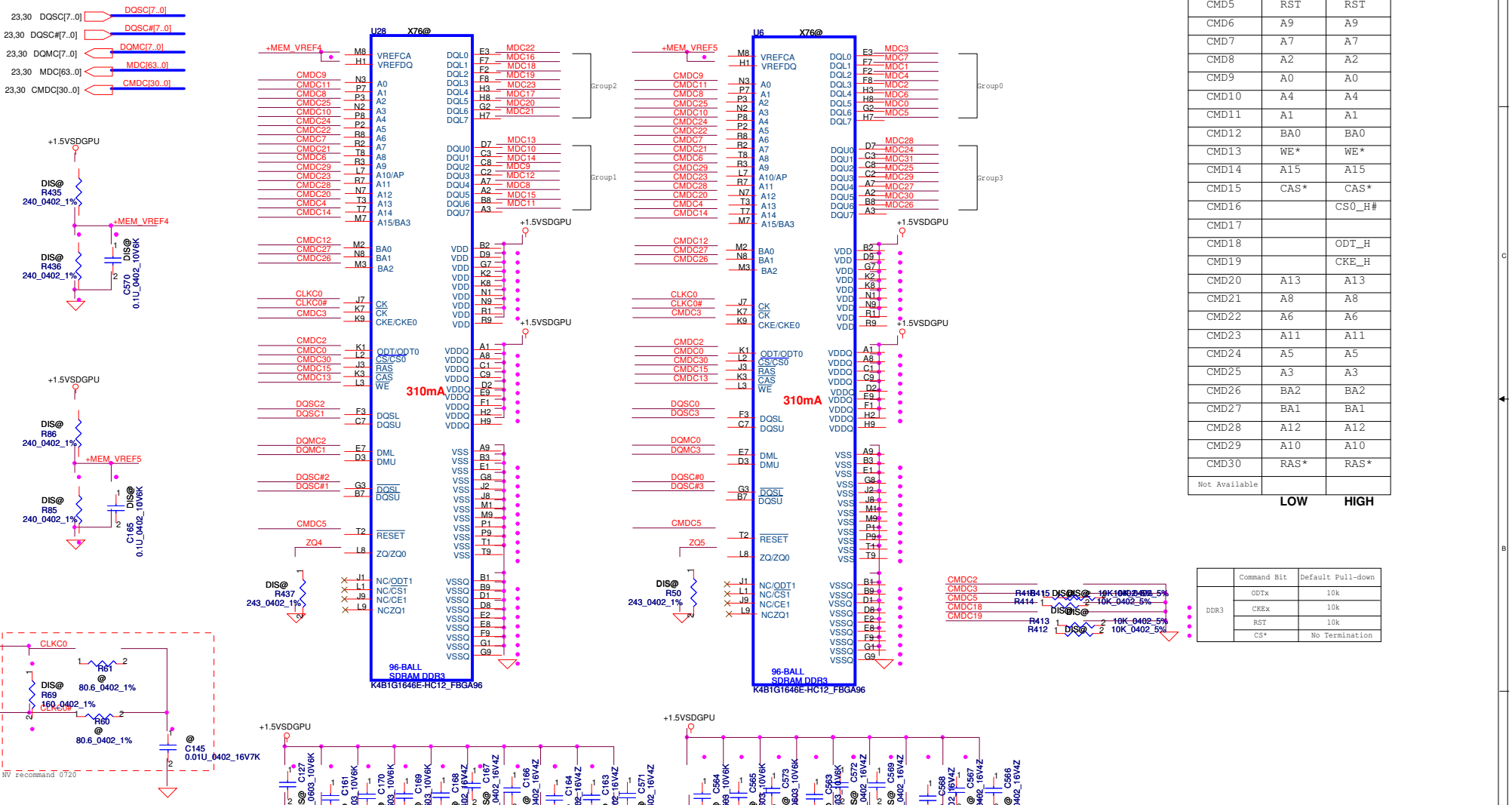
Title: N12P DDR3 7/9

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 28 of 59

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

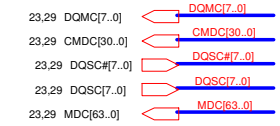
Title: N12P DDR3 8/9

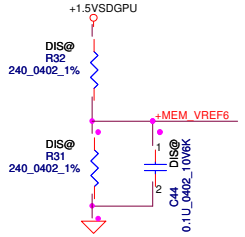
Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

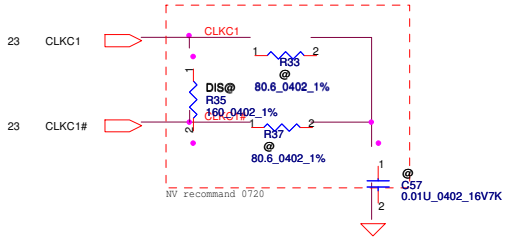
Date: Friday, August 27, 2010 | Sheet 29 of 59

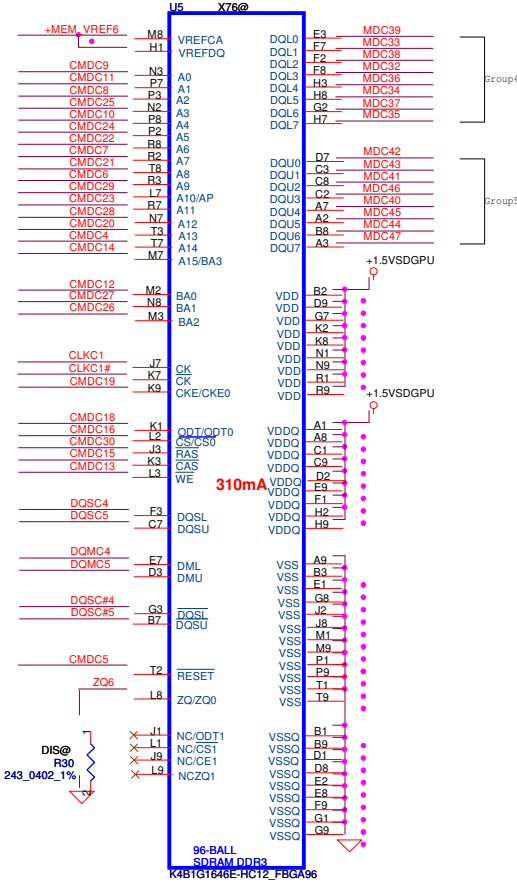
VRAM DDR3 chips (1GB)

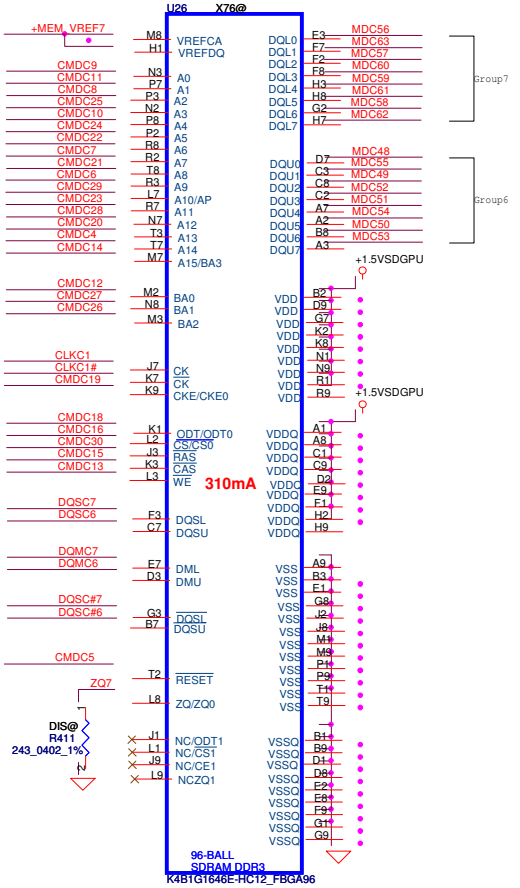
64Mx16 DDR3 *8==>1GB

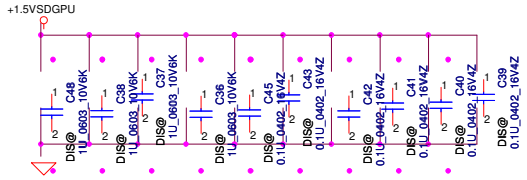


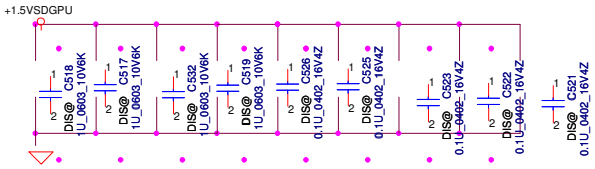












Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: N12P DDR3 9/9

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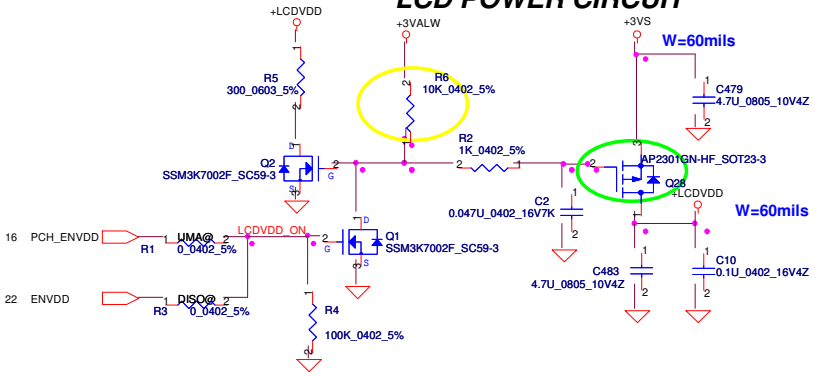
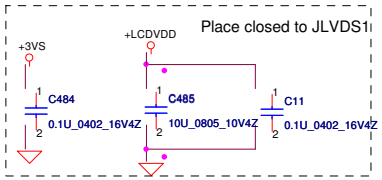
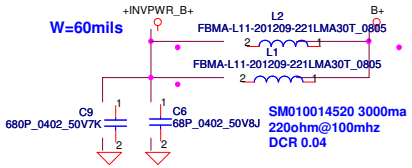
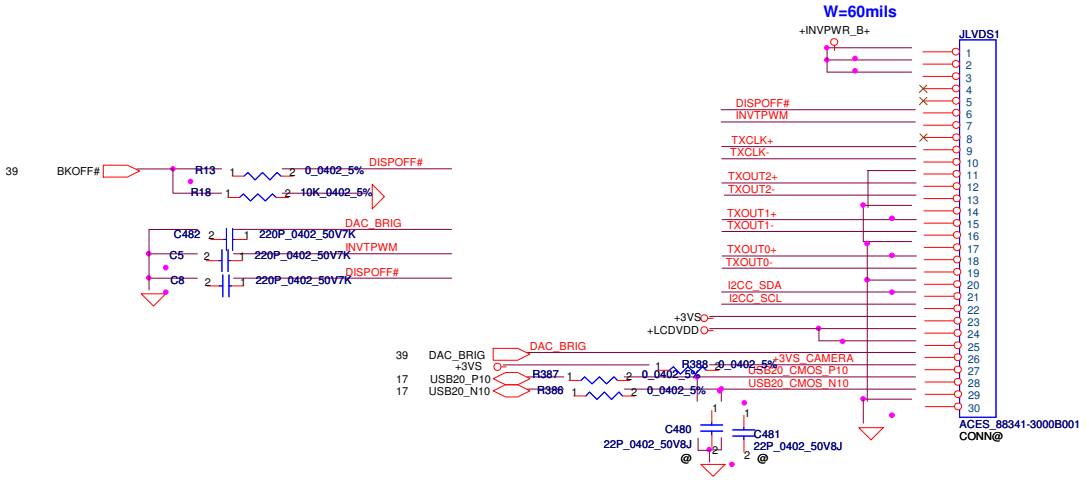
LCD POWER CIRCUIT



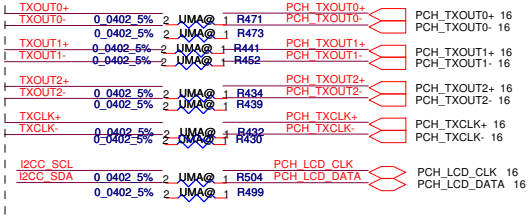




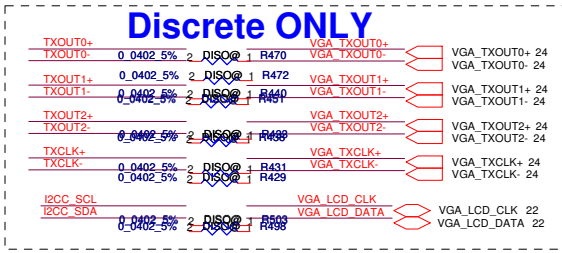
LCD/LED PANEL Conn.

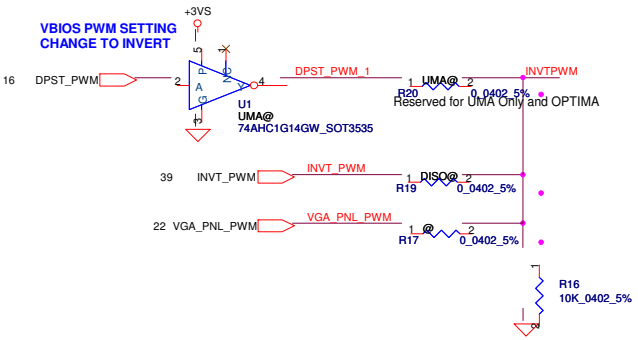


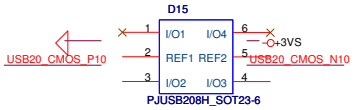
UMA Only / Optimus



Discrete ONLY







Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: LVDS Connector

Size	Document Number	Rev
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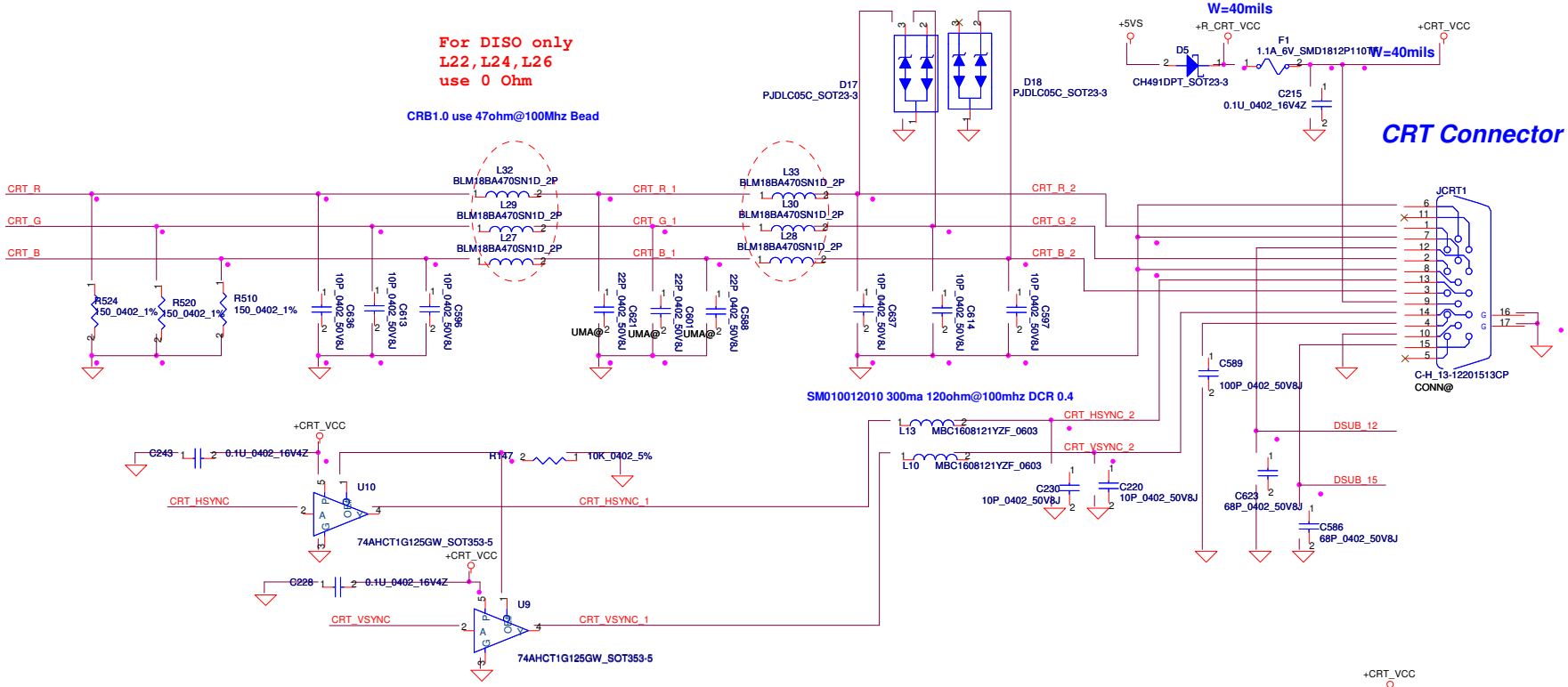

UMA Only / OPTIMUS

16	PCH_CRT_R	PCH_CRT_R	R420 2 UMA@ 1 0_0402_5%	CRT_R	
16	PCH_CRT_G	PCH_CRT_G	R424 2 UMA@ 1 0_0402_5%	CRT_G	
16	PCH_CRT_B	PCH_CRT_B	R422 2 UMA@ 1 0_0402_5%	CRT_B	
16	PCH_CRT_HSYNC	PCH_CRT_HSYNC	R428 2 UMA@ 1 33_0402_5%	CRT_HSYNC	
16	PCH_CRT_VSYNC	PCH_CRT_VSYNC	R426 2 UMA@ 1 33_0402_5%	CRT_VSYNC	
16	PCH_CRT_CLK	PCH_CRT_CLK	R506 2 UMA@ 1 0_0402_5%	CRT_DDC_CLK	
16	PCH_CRT_DATA	PCH_CRT_DATA	R501 2 UMA@ 1 0_0402_5%	CRT_DDC_DATA	

Discrete only

22	VGA_CRT_R	VGA_CRT_R	R419 2 DISO@ 1 0_0402_5%	CRT_R
22	VGA_CRT_G	VGA_CRT_G	R423 2 DISO@ 1 0_0402_5%	CRT_G
22	VGA_CRT_B	VGA_CRT_B	R421 2 DISO@ 1 0_0402_5%	CRT_B
22	VGA_CRT_HSYNC	VGA_CRT_HSYNC	R427 2 DISO@ 1 0_0402_5%	CRT_HSYNC
22	VGA_CRT_VSYNC	VGA_CRT_VSYNC	R425 2 DISO@ 1 0_0402_5%	CRT_VSYNC
22	VGA_DDC_CLK	VGA_DDC_CLK	R505 2 DISO@ 1 0_0402_5%	CRT_DDC_CLK
22	VGA_DDC_DATA	VGA_DDC_DATA	R500 2 DISO@ 1 0_0402_5%	CRT_DDC_DATA

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.			
Title	CRT Connector		
Size	Document Number		Rev
Custom	P5WE0 M/B LA-6901P Schematic		0.1
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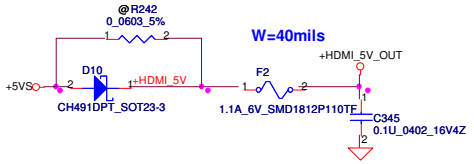
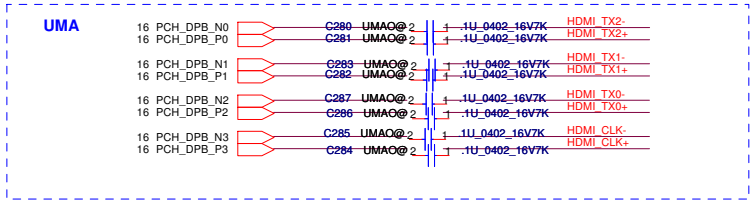
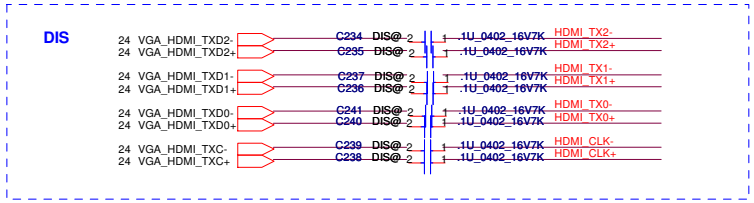
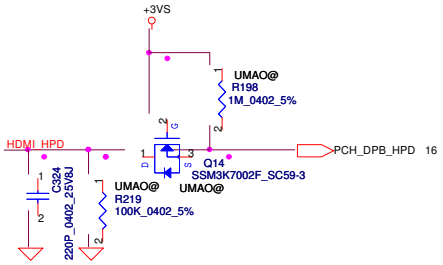
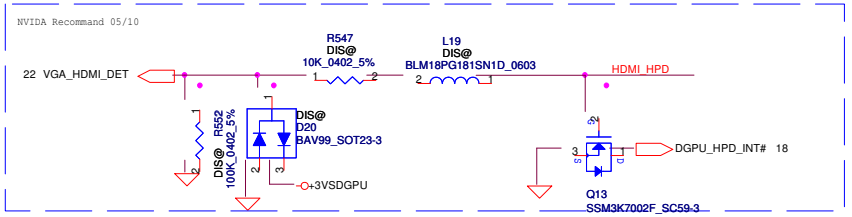


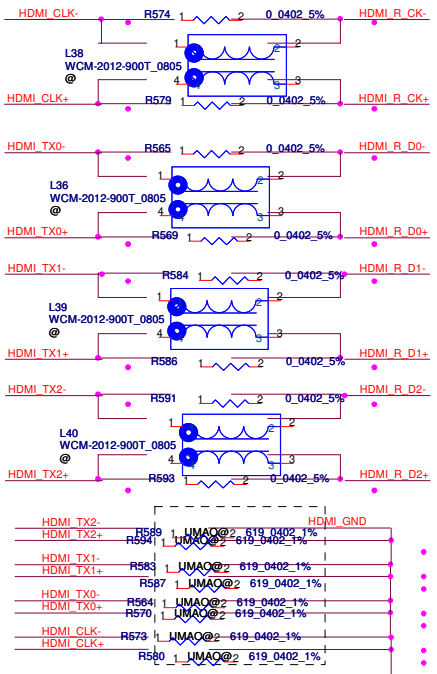






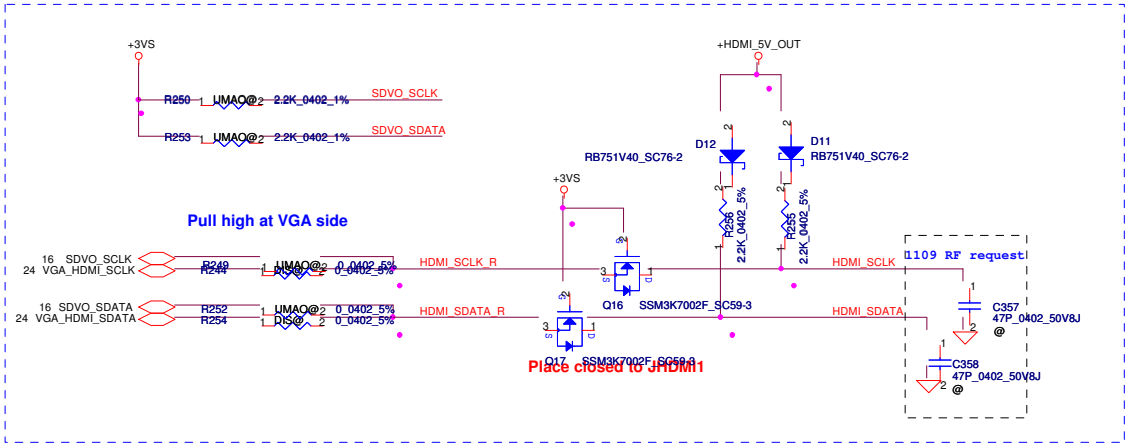


SM070001310 400ma 90ohm@100mhz DCR 0.3

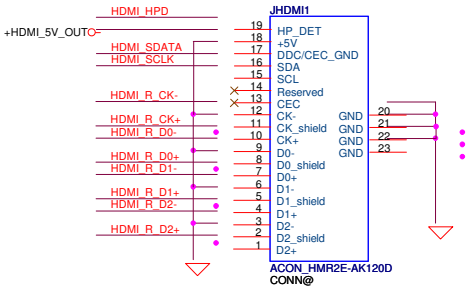


INTEL use 619 Ohm for terminationn

NV use 499 Ohm for terminationn



HDMI connector



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: HDMI Conn

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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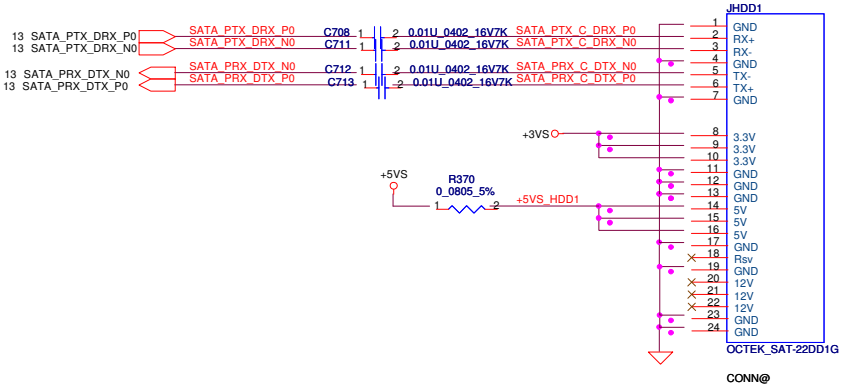
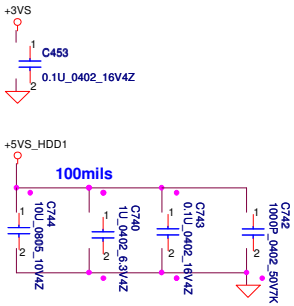
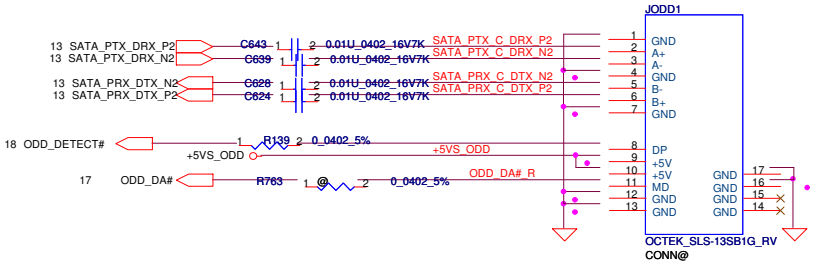
SATA HDD1 Conn.

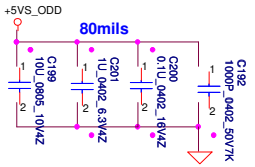
CL 4.0 mm

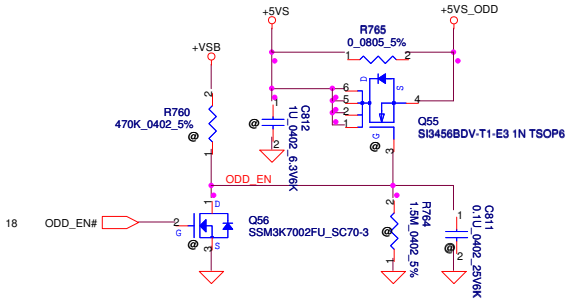




SATA ODD Conn.







Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size	Document Number	Rev
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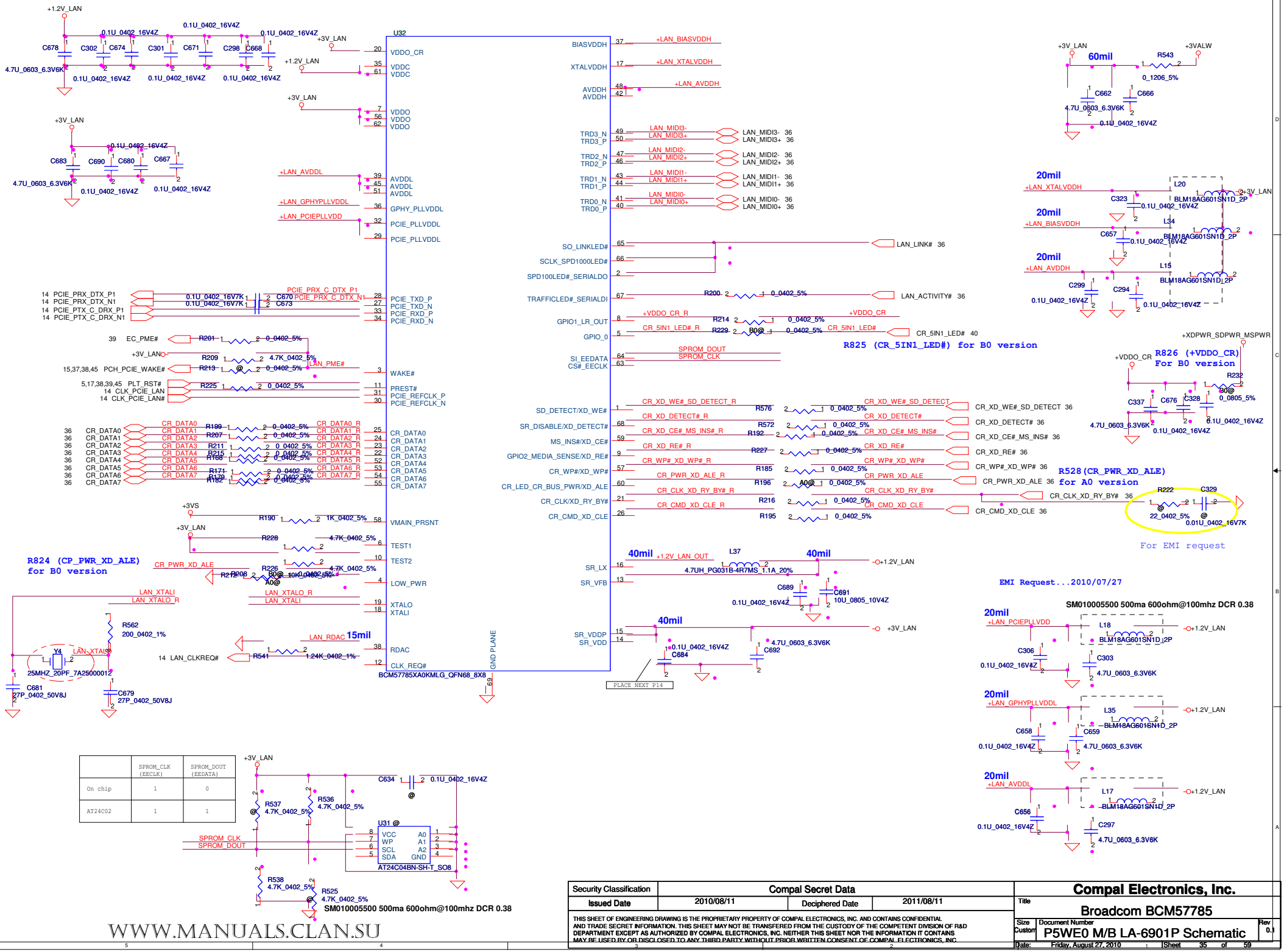

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: Broadcom BCM57785

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1
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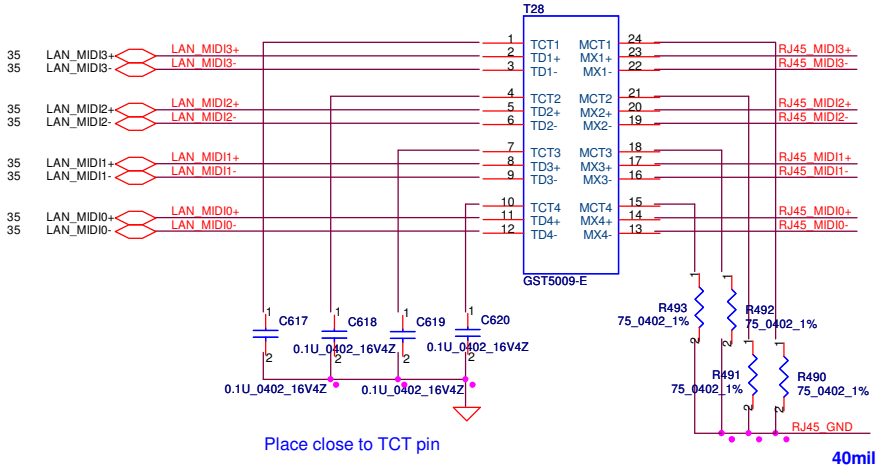
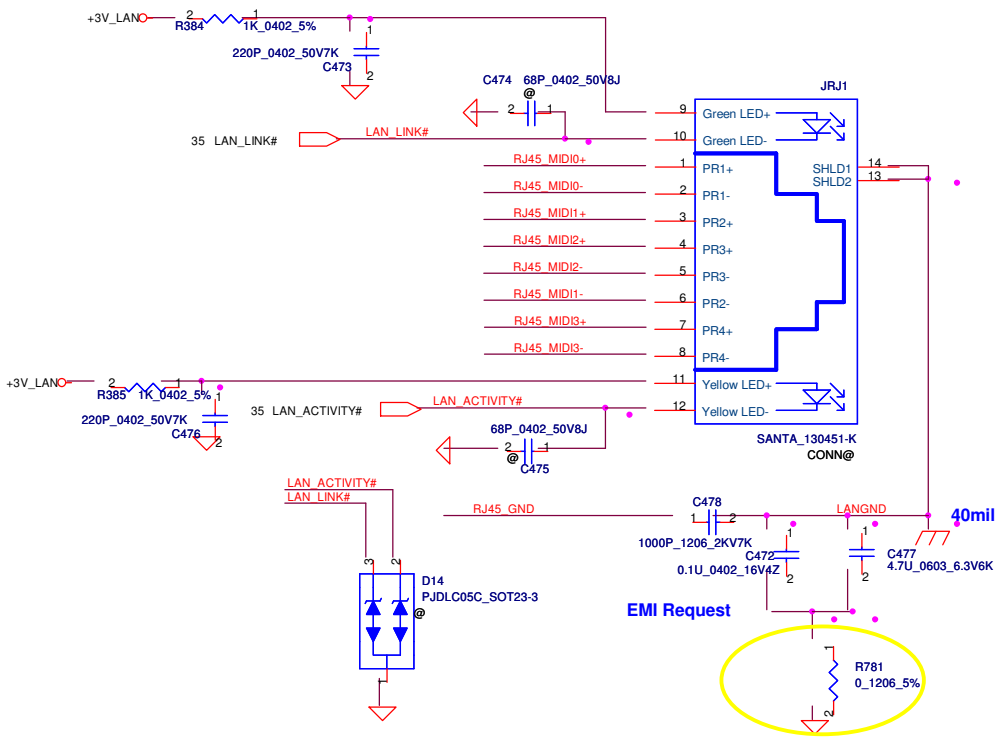
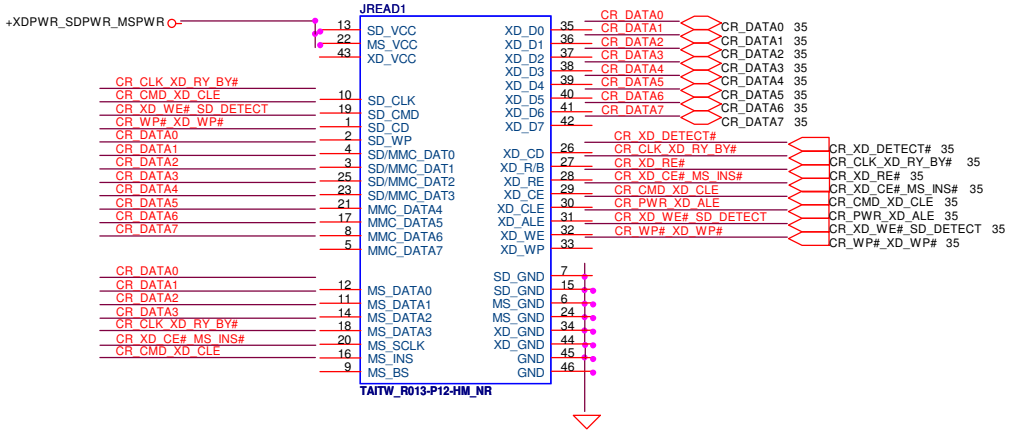
LAN Connector

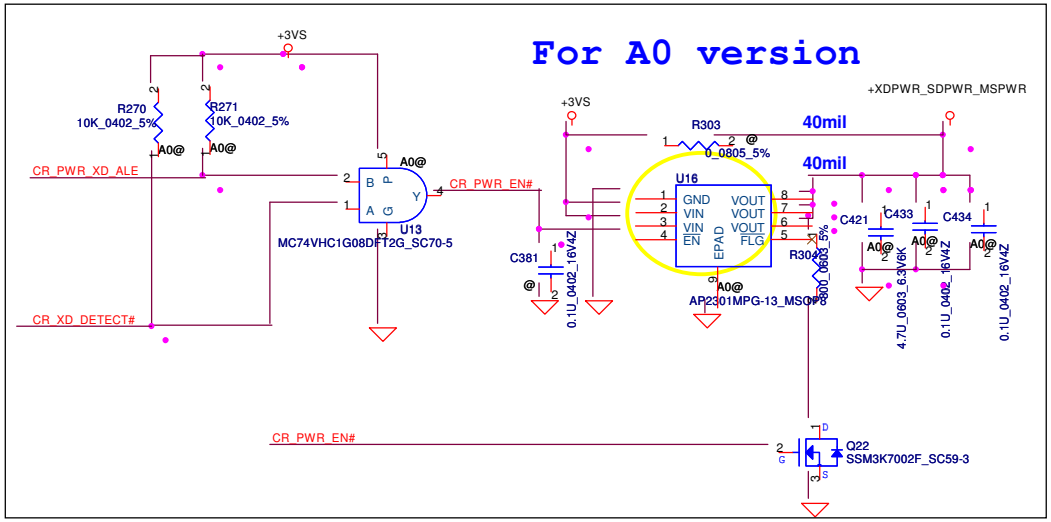


BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00



Card Reader Connector





Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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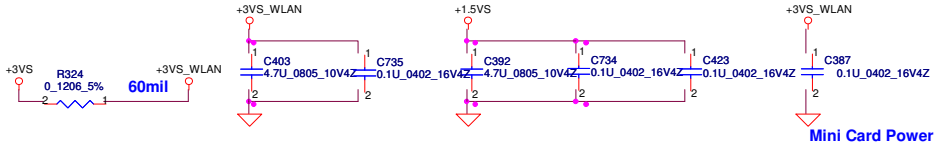
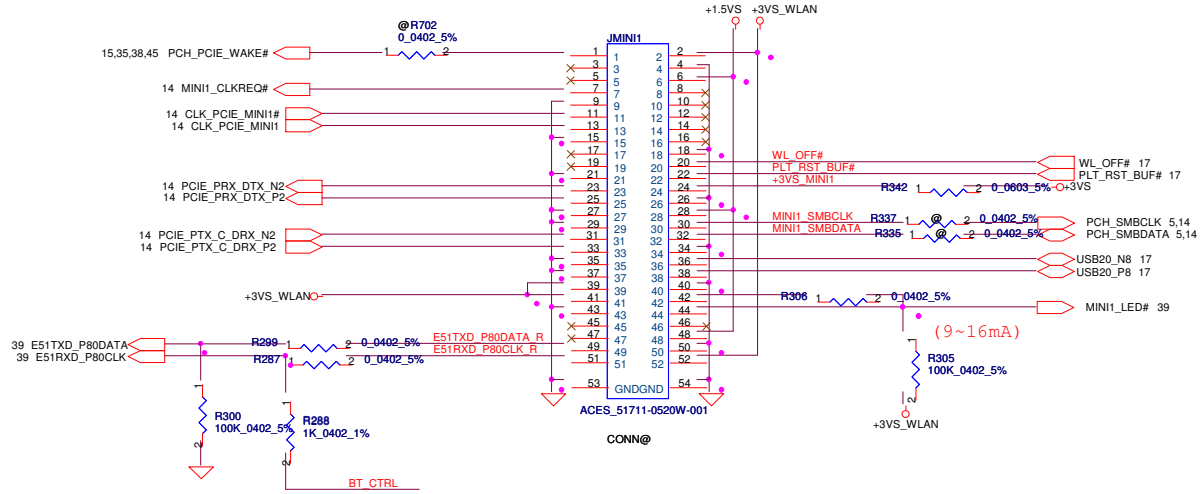
For Wireless LAN

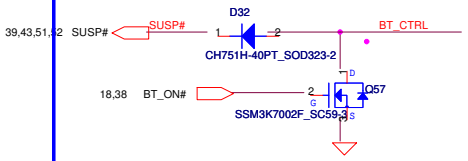


Mini Card Power Rating

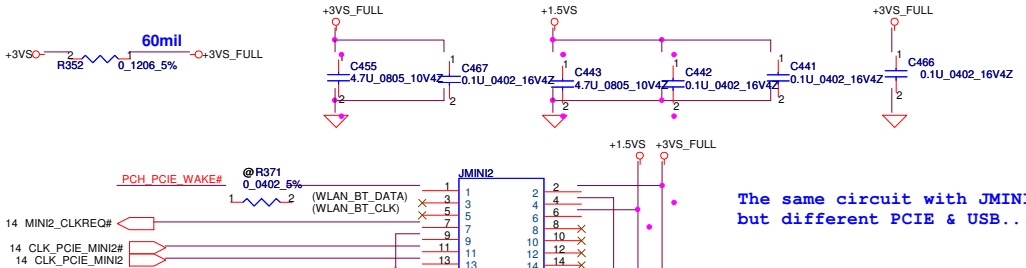


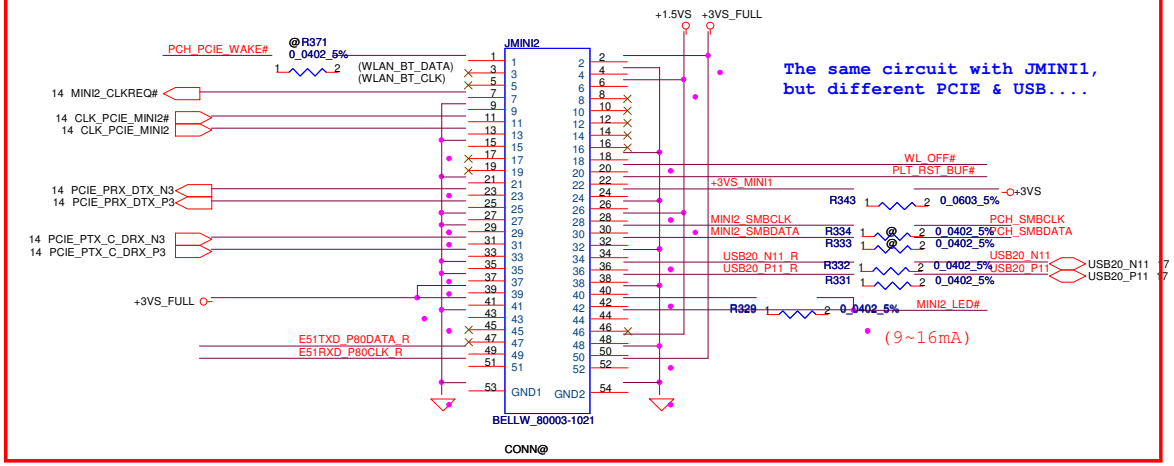
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H



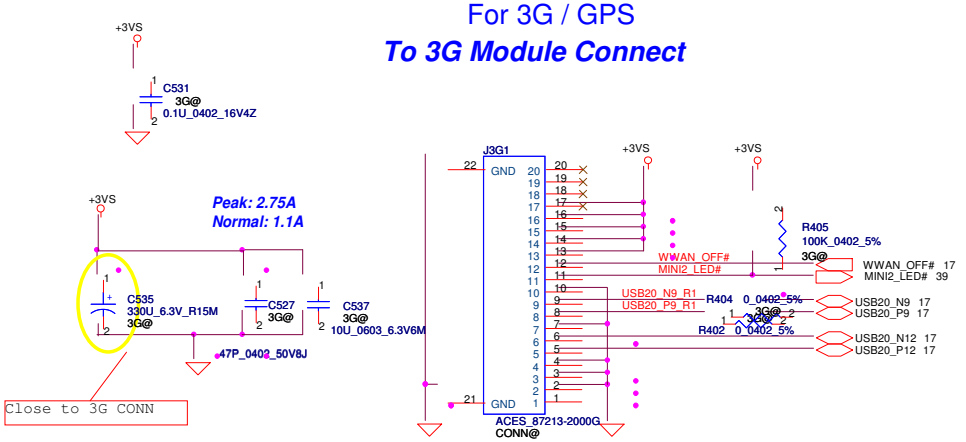
Reserve





For 3G / GPS

To 3G Module Connect



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)

Size	Document Number	Rev
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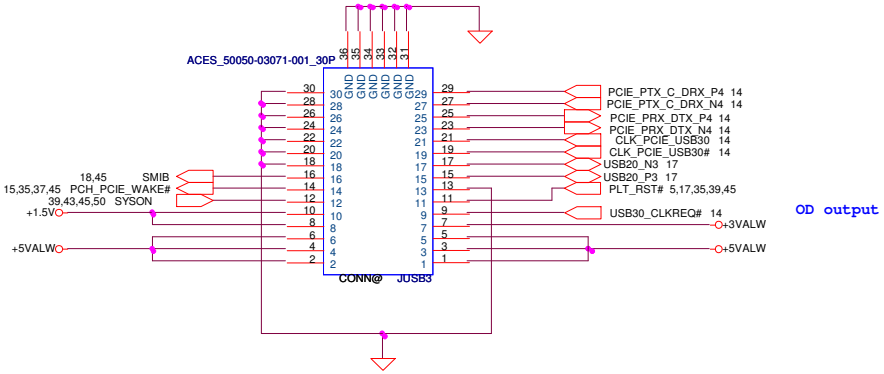
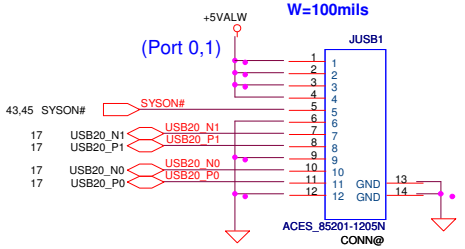
USB3.0 Conn.

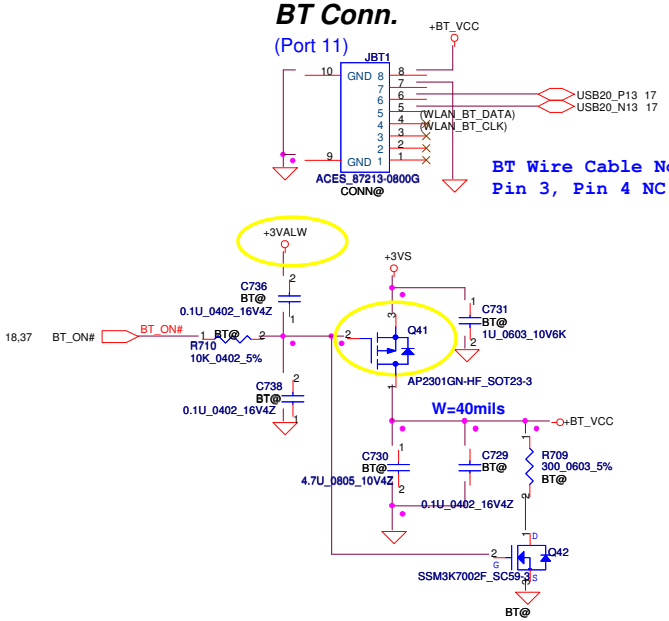


OD output

USB/B Conn.



BT Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: USB / BT / USBB

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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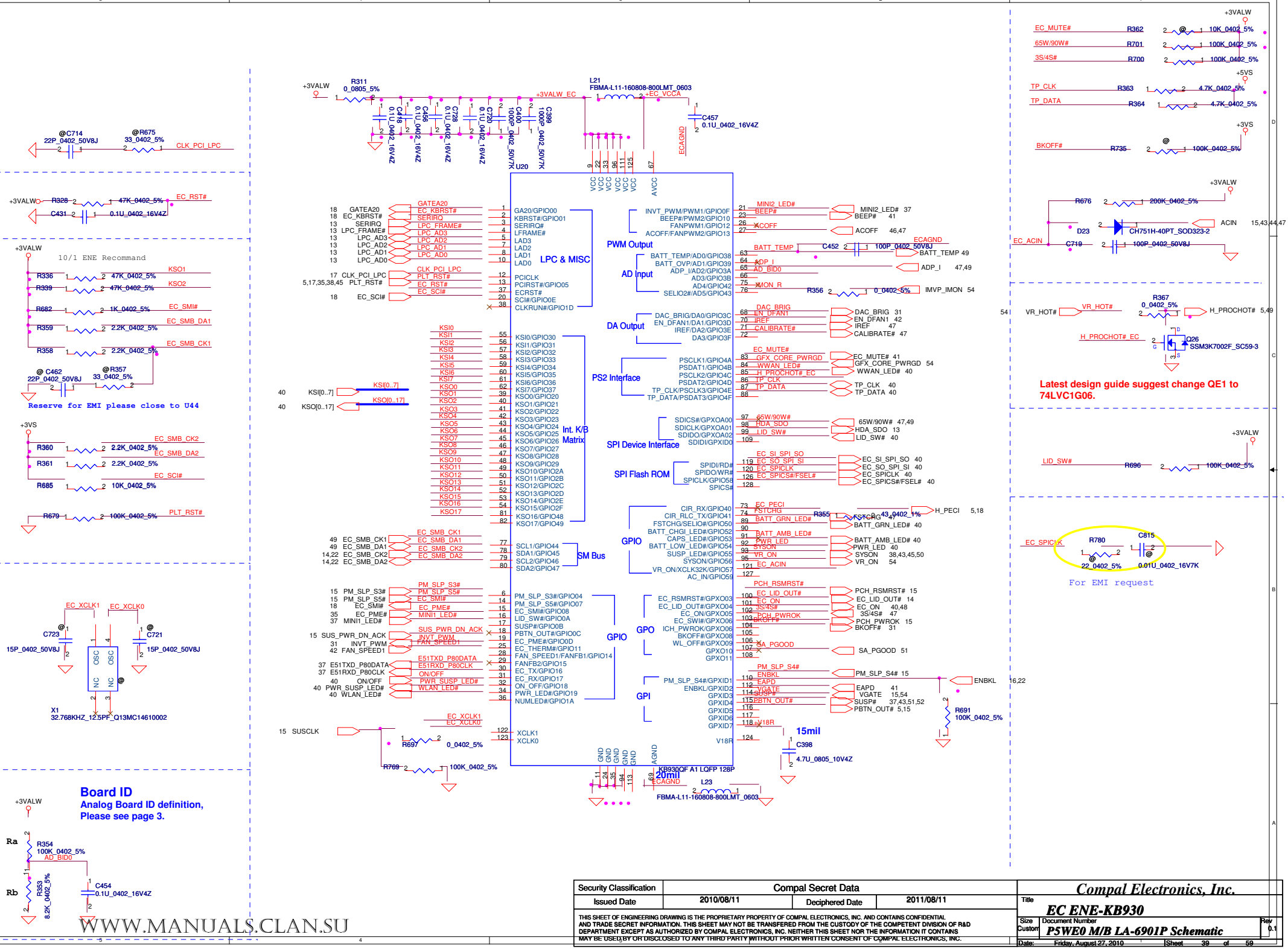

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: EC ENE-KB930

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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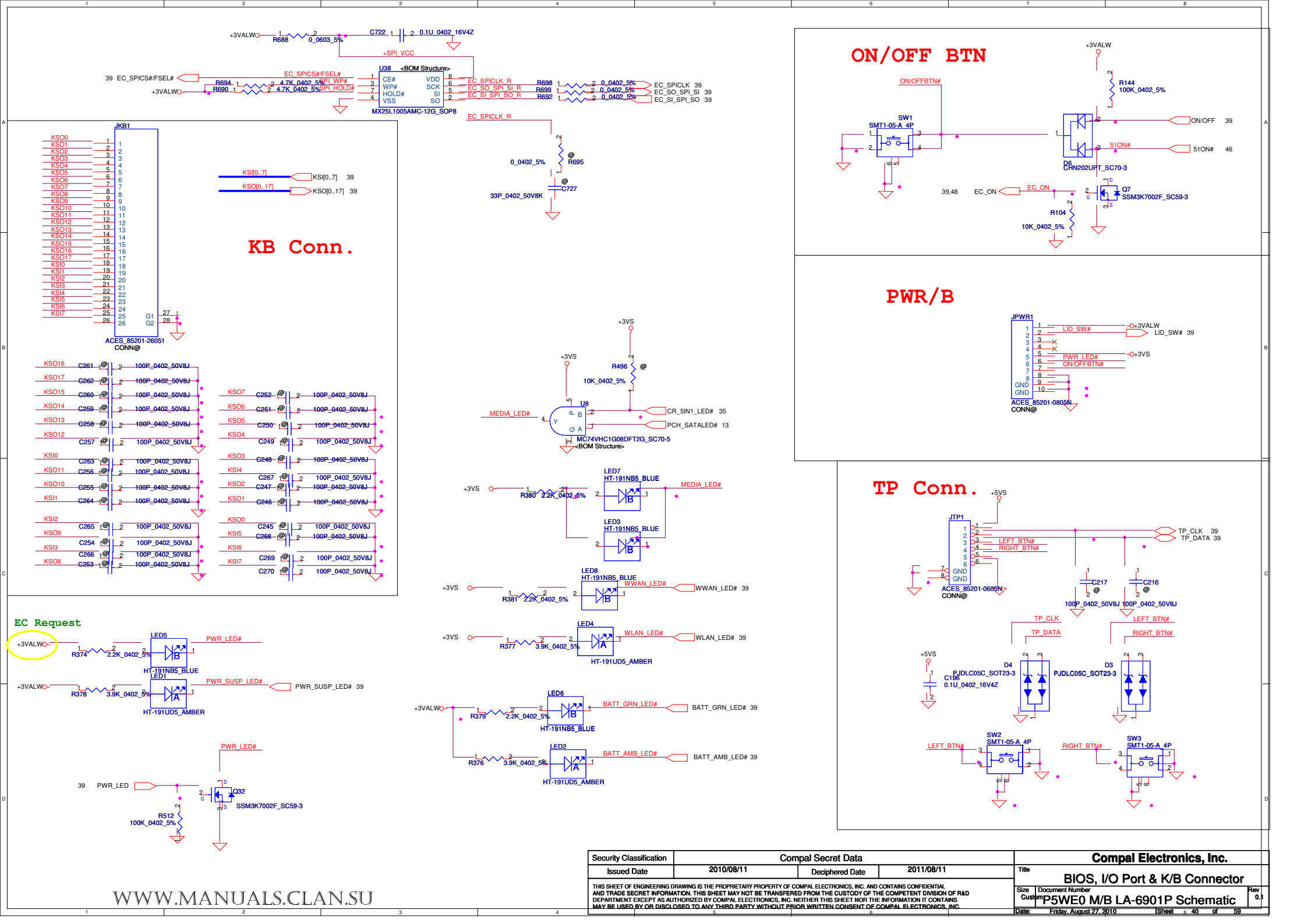

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

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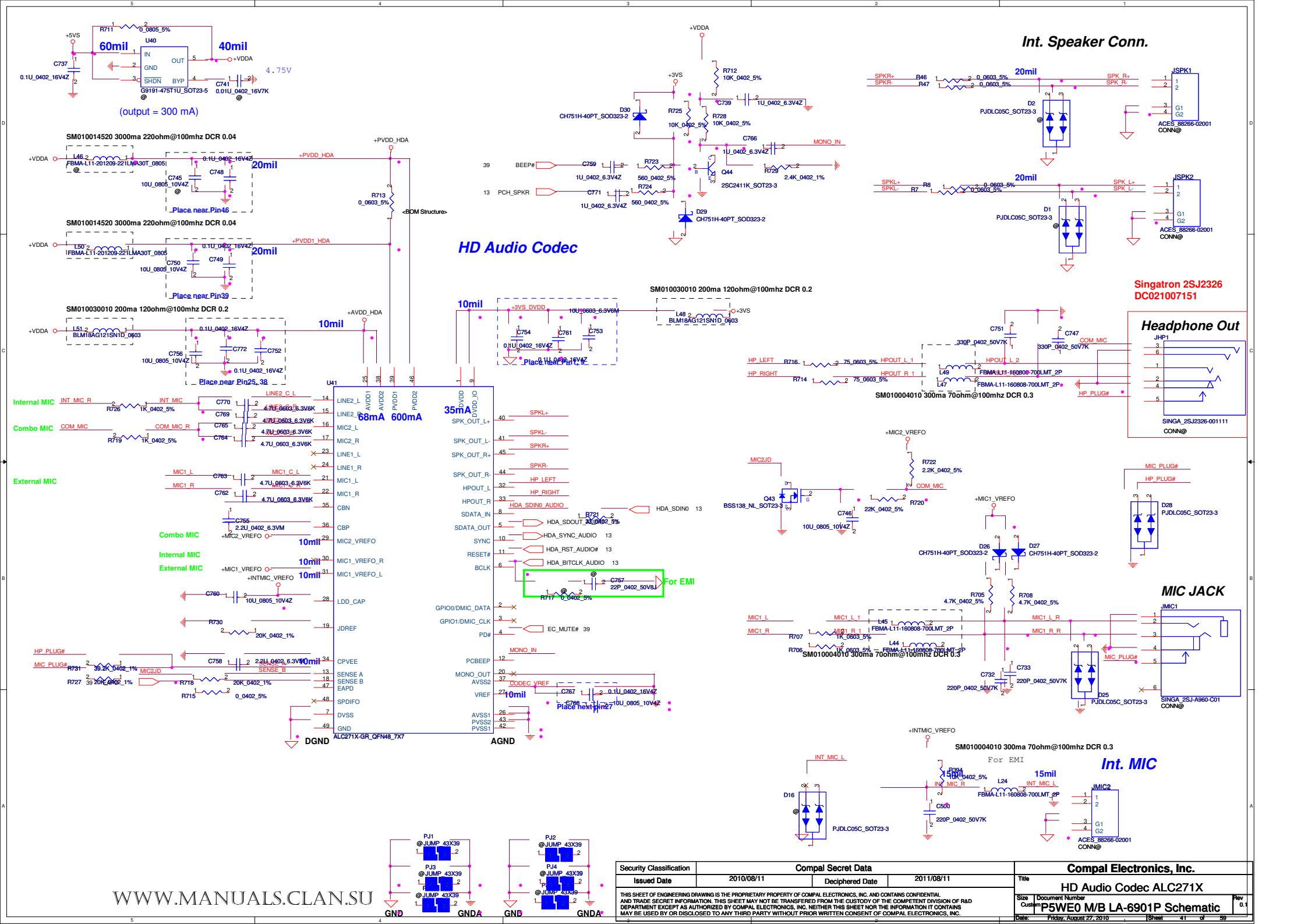
Int. Speaker Conn.
HD Audio Codec
Headphone Out
Singatron 2SJ2326
DC021007151
MIC JACK
Int. MIC
60mil
40mil
4.75V
(output = 300 mA)
SM010014520 3000ma 220ohm@100mhz DCR 0.04
SM010030010 200ma 120ohm@100mhz DCR 0.2
SM010004010 300ma 70ohm@100mhz DCR 0.3
20mil
10mil
Place near Pin46
Place near Pin39
Place near Pin25, 38
Place near Pin27
68mA
600mA
35mA
Internal MIC
Combo MIC
External MIC
For EMI
15mil
ALC271X-GR_QFN48_7X7
DGND
AGND
WWW.MANUALS.CLAN.SU
Security Classification
Compal Secret Data
Issued Date
2010/08/11
Deciphered Date
2011/08/11
Compal Electronics, Inc.
HD Audio Codec ALC271X
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FAN Stand-Off

JUSB3 Stand-Off

H1 H_3P4 H2 H_3P4 H3 H_3P4 H4 H_3P4 H5 H_3P4 H6 H_3P4 H7 H_3P4

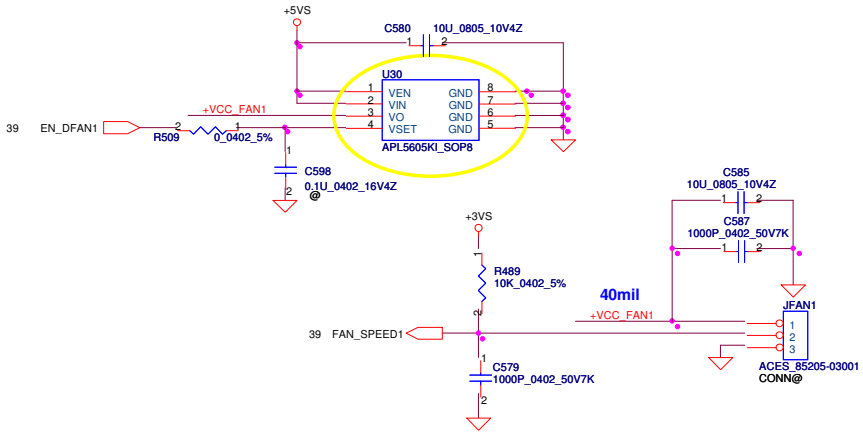
H8 H_3P0 H9 H_3P0 H10 H_3P0 H11 H_3P0 H12 H_3P0 H13 H_3P0 H14 H_3P0 H15 H_3P0 H16 H_3P0 H17 H_3P0 H18 H_3P0

H19 H_4P0 H20 H_4P0

H21 H_4P2 H22 H_4P2 H23 H_4P2 H24 H_4P2

H25 H_7P0N H26 H_3P0N H27 H_3P5X3P0N

FAN1 Conn



FD1 FIDUCIAL_C40M80 FD3 FIDUCIAL_C40M80 FD2 FIDUCIAL_C40M80 FD4 FIDUCIAL_C40M80

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: FAN & Screw Hole

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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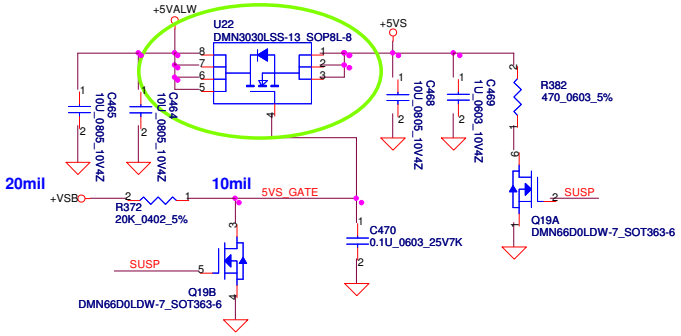
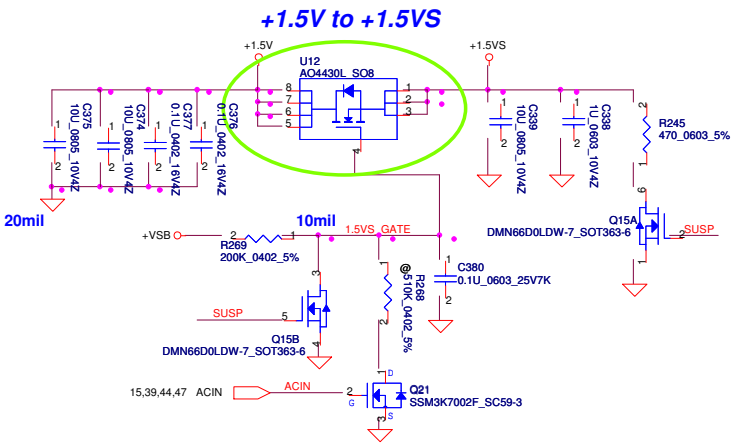
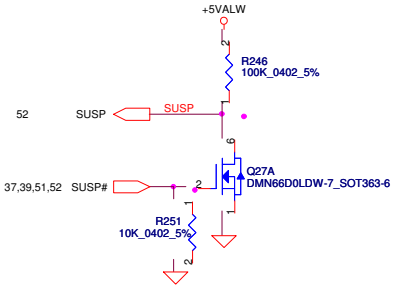
+5VALW TO +5VS

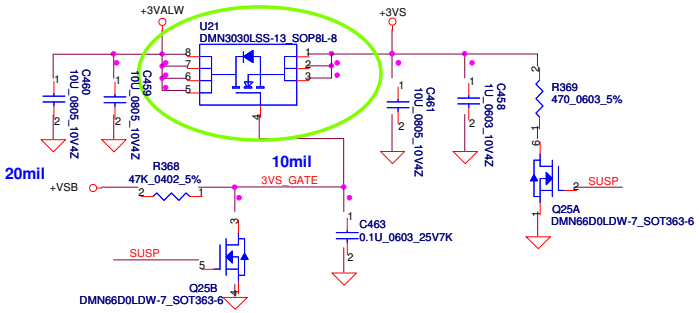


+1.5V to +1.5VS

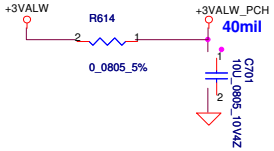


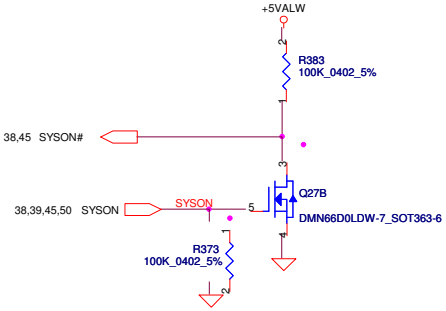


+3VALW TO +3VS

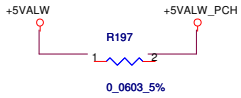


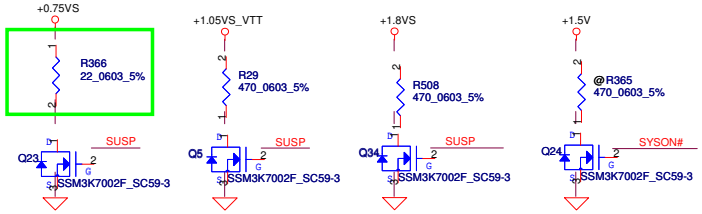
+3VALW TO +3VALW_PCH(PCH AUX Power)





+5VALW TO +5VALW_PCH(PCH AUX Power)





Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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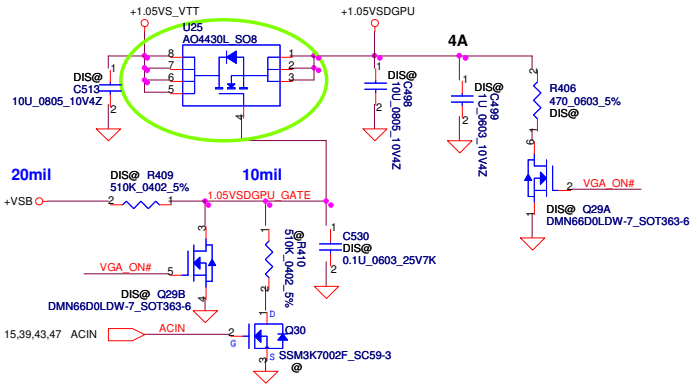
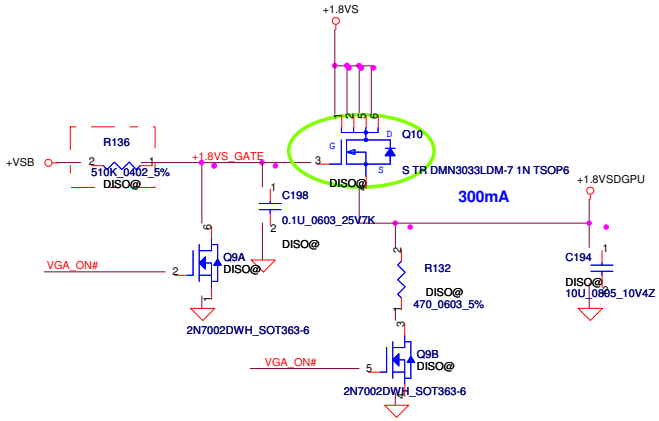
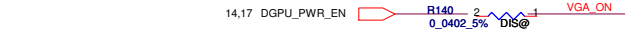
+1.05VS_VTT to +1.05VSDGPU for GPU

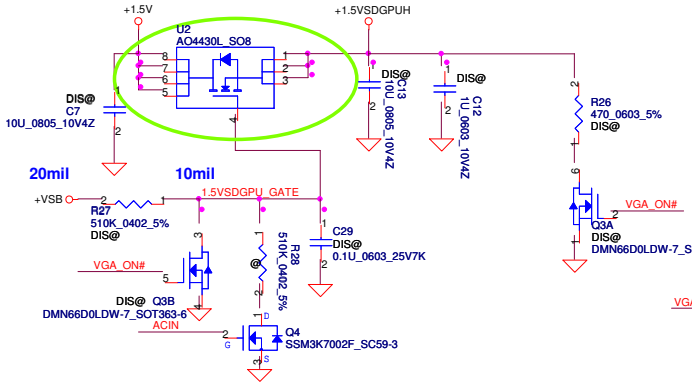


+1.8VS to +1.8VSDGPU for GPU

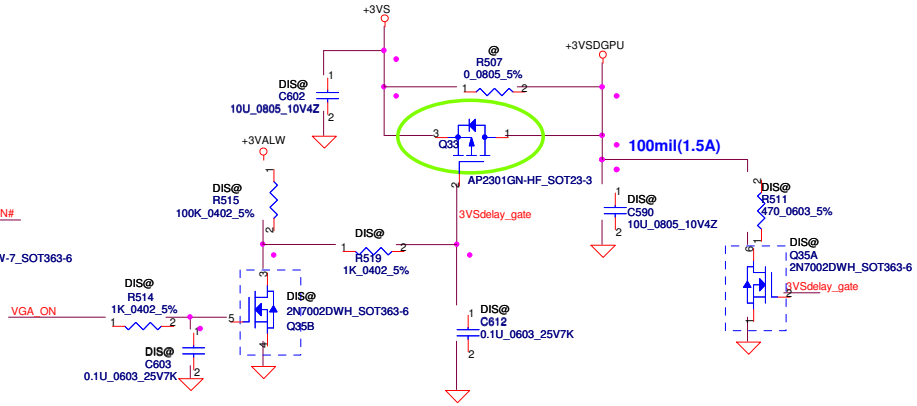


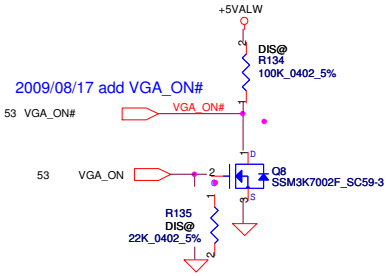


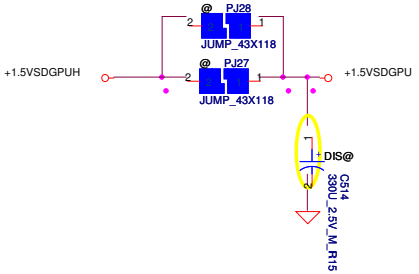
+1.5V to +1.5VSDGPUH for GPU



+3VS to +3VSDGPU for GPU







Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.			
Title: DC Interface			
Size: Custom	Document Number: P5WE0 M/B LA-6901P Schematic		Rev: 0.1
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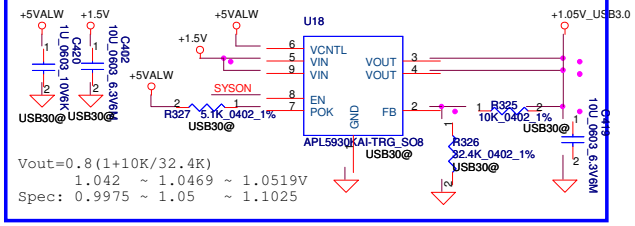
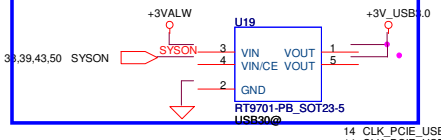
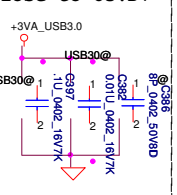
+1.5V to +1.05V Transfer



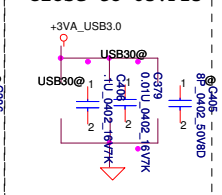
+3VALW to +3V Transfer

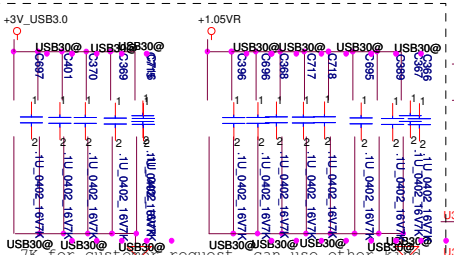


Close to U3.D7

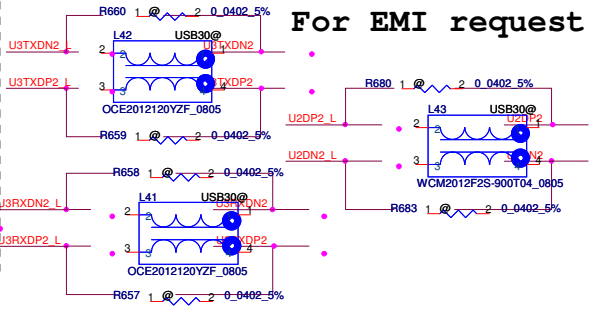


Close to U3.P13





For EMI request



SPEC Max:+3V---200mA;+1.05V---800mA
Idle mode:0.489W:
+3V---43mA;+1.05V---328mA
D3 mode:0.066W:
+3V---5.4mA;+1.05V---45mA

OD output

Can be attach to EC, either.

PCI Express/ExpressCard select signal
1:others
0:Express Card or Mini card

As short as possible

For ESD request

Resister option for L52

Place as close as possibile to U3.N14 and U3.M14

Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz when use 48MHz clock: mount R22,R25

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Title: USB3.0 PD720200

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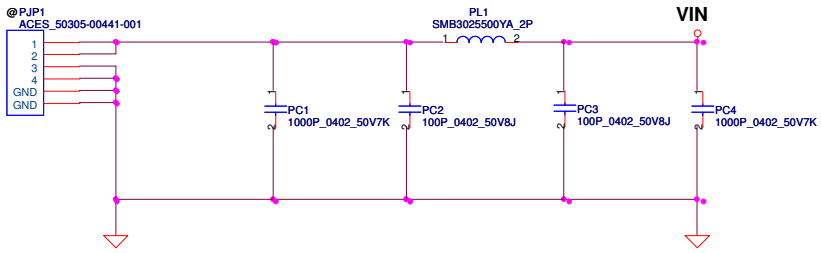

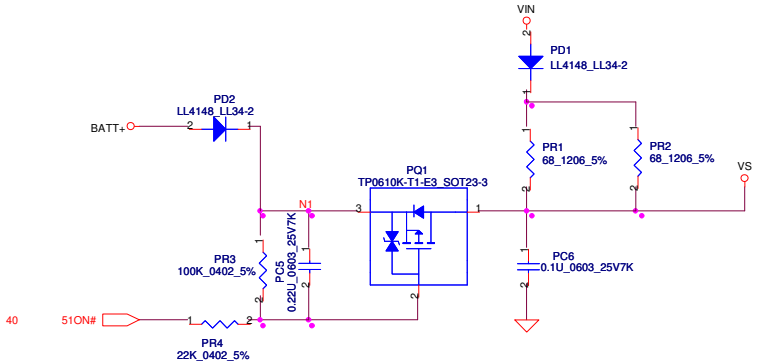

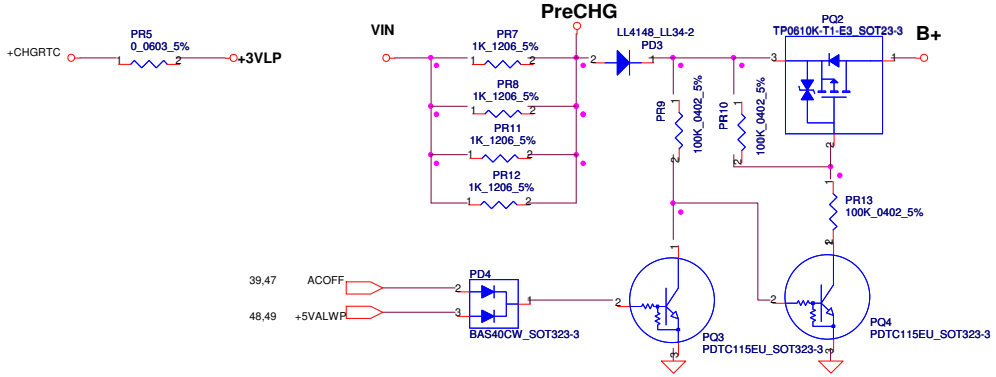

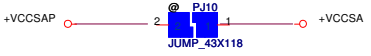

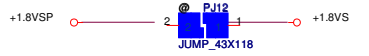

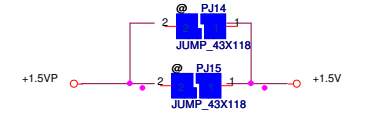

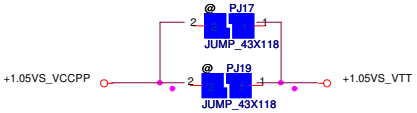

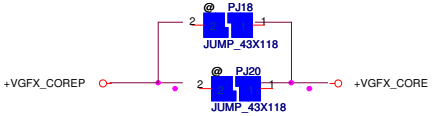

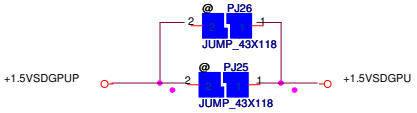

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

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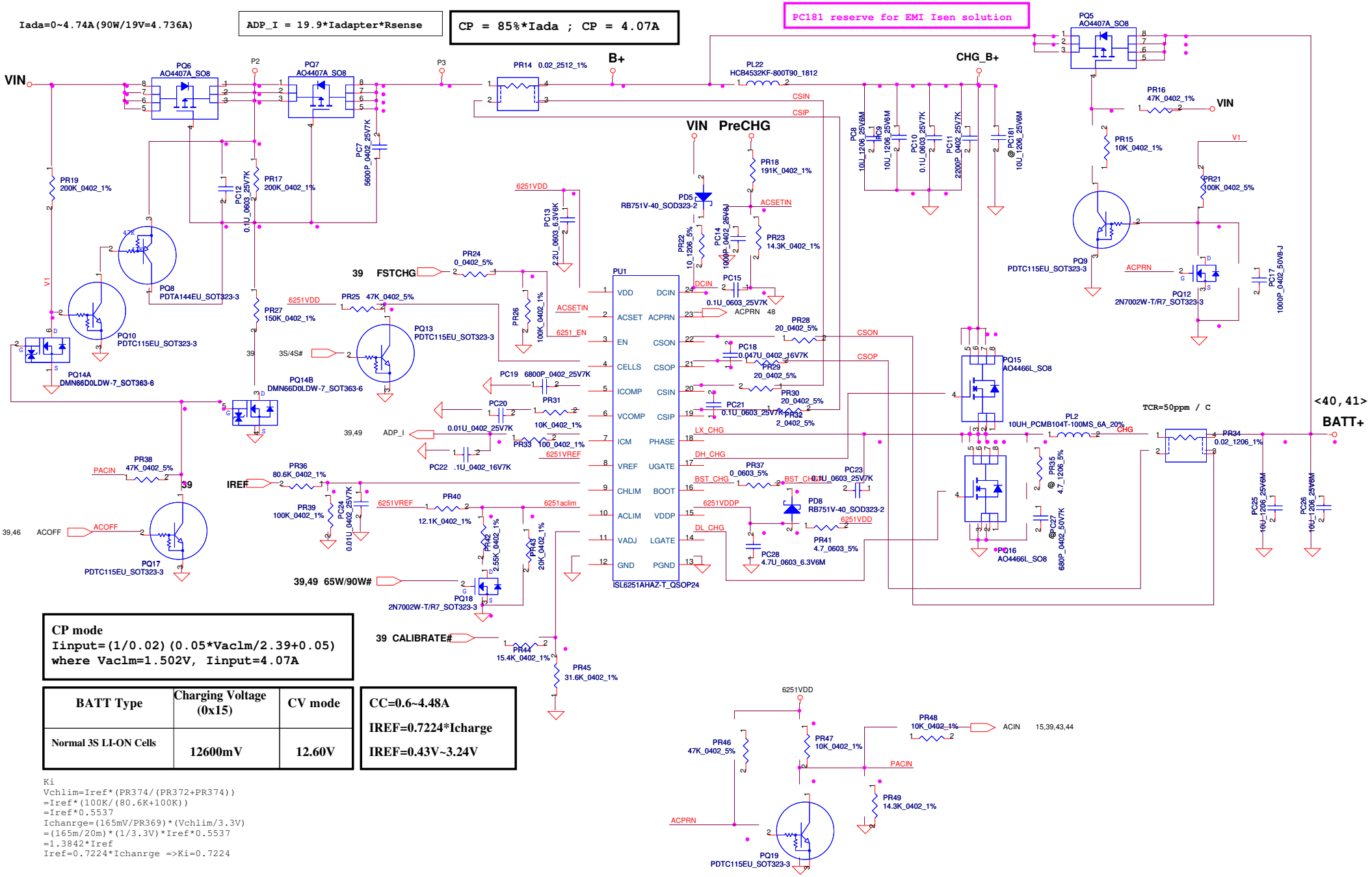
Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A

PC181 reserve for EMI Isen solution



CP mode

Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)

where Vaclm=1.502V, Iinput=4.07A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR-CHARGER

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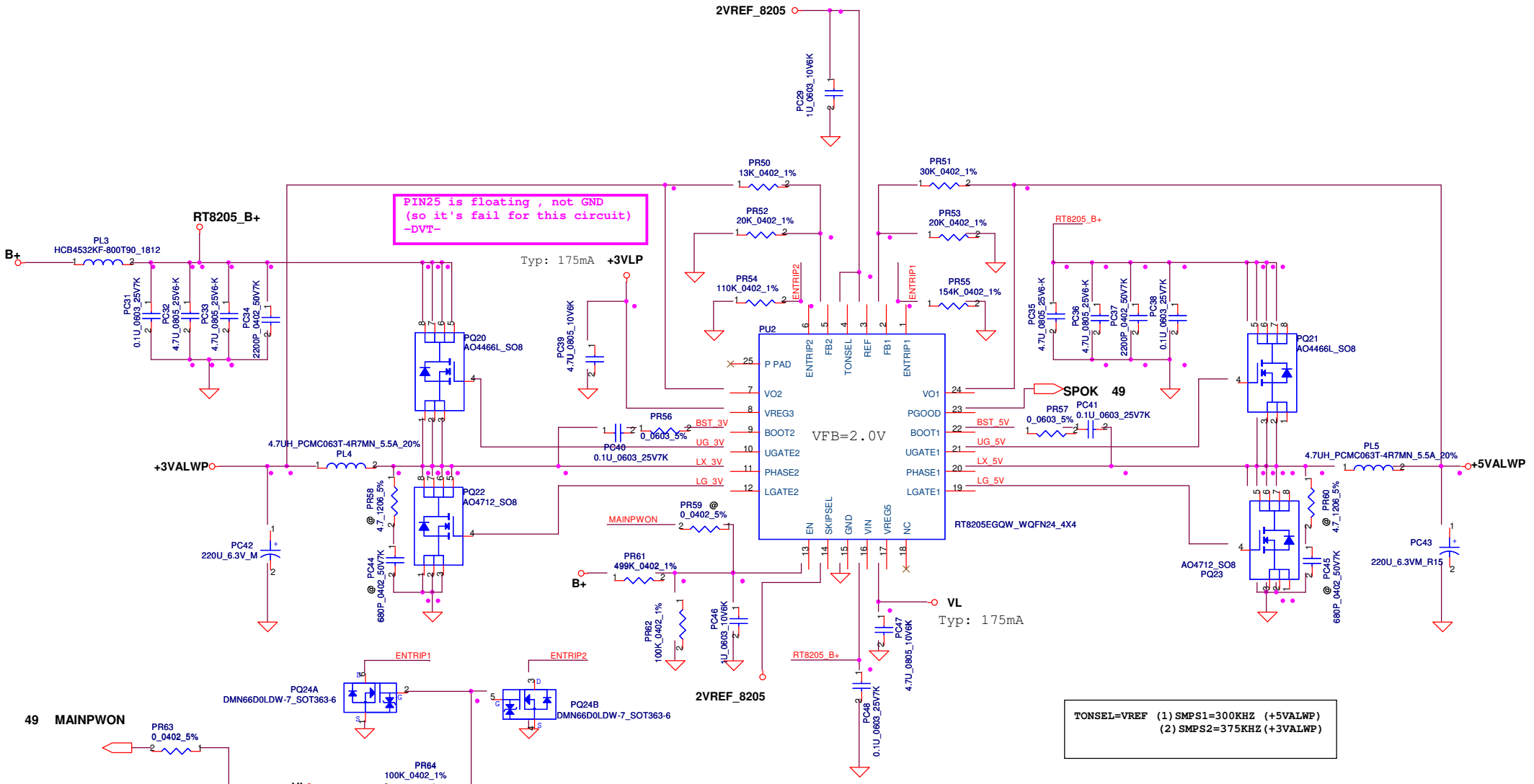

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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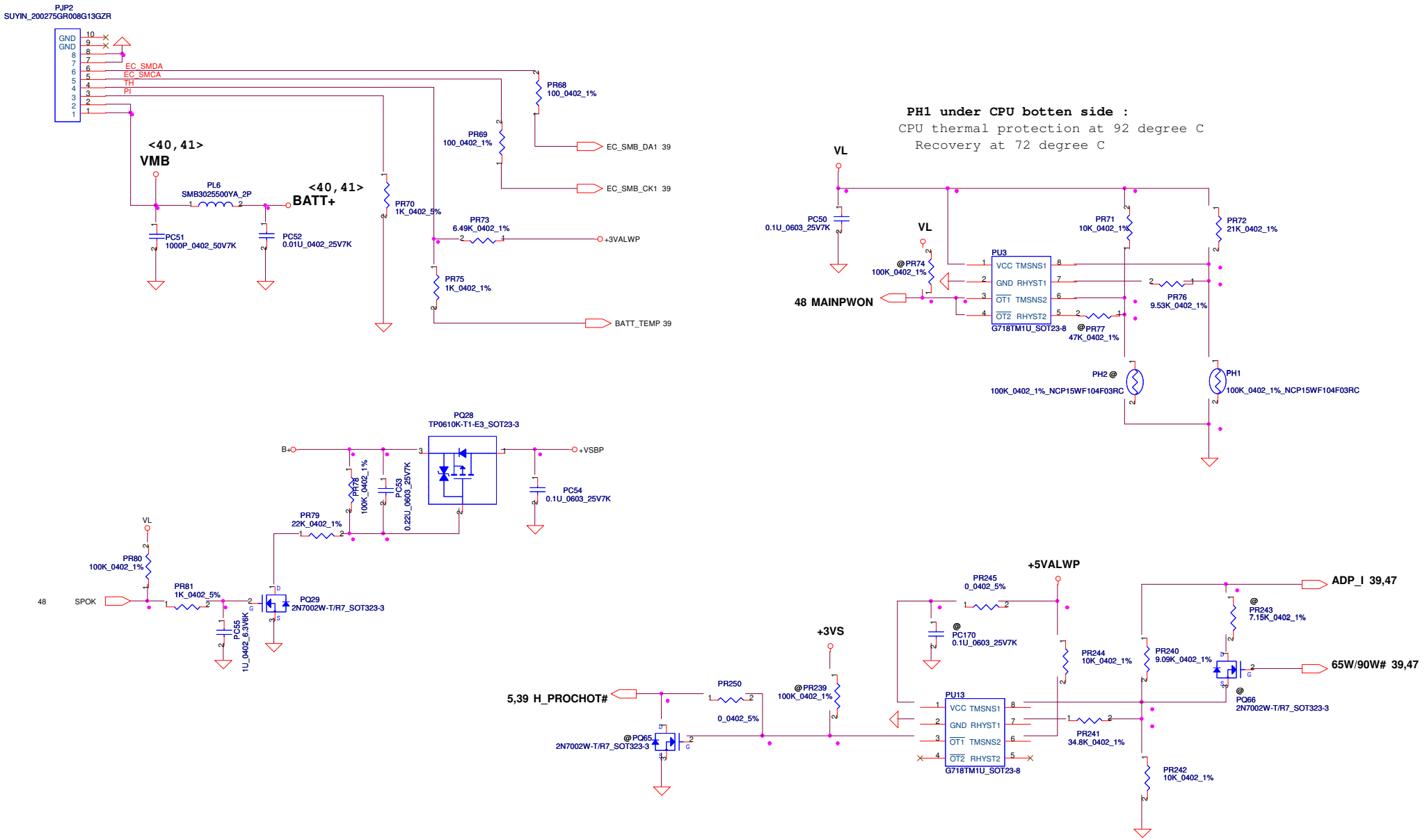


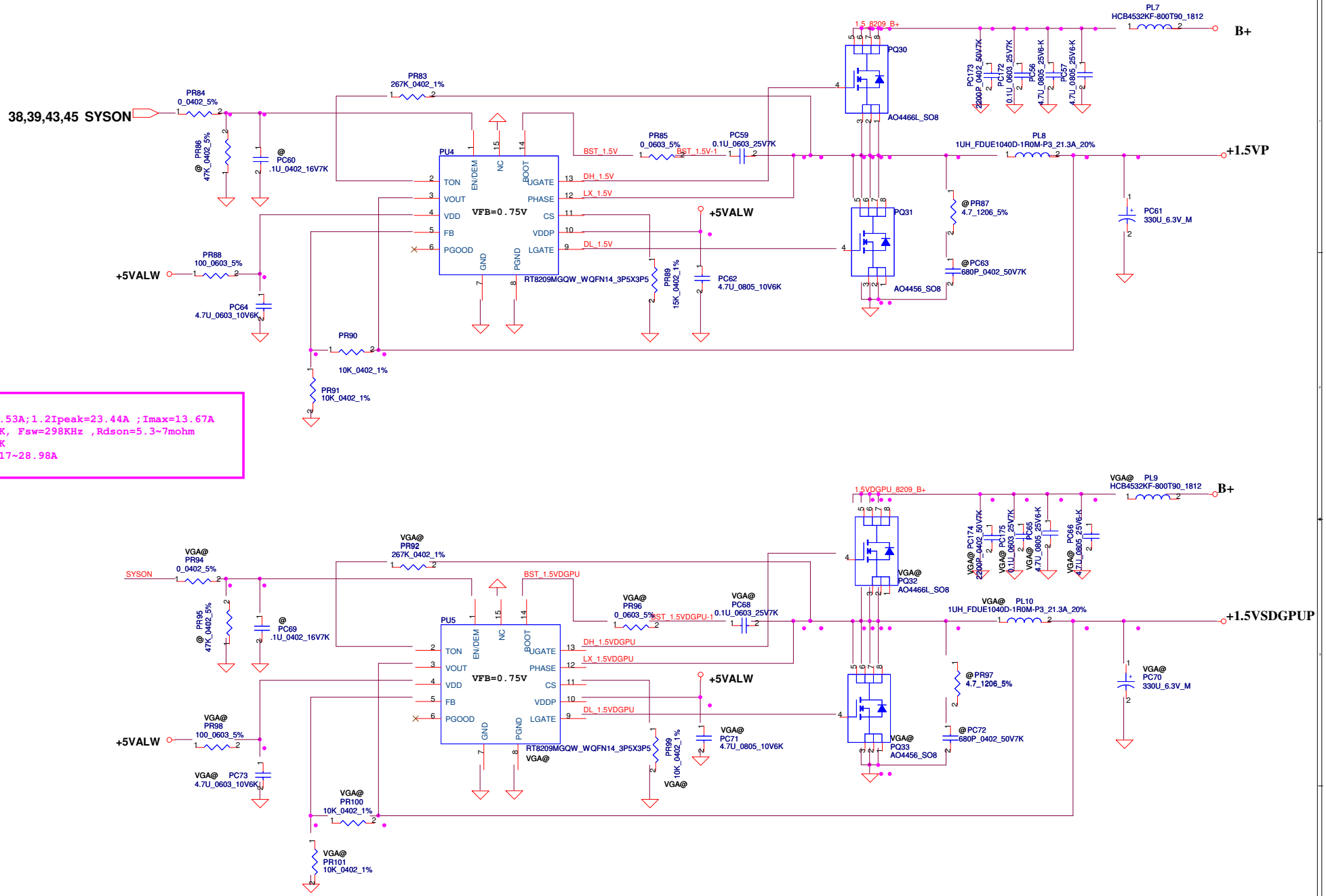
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 49 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.5VSDGPU

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

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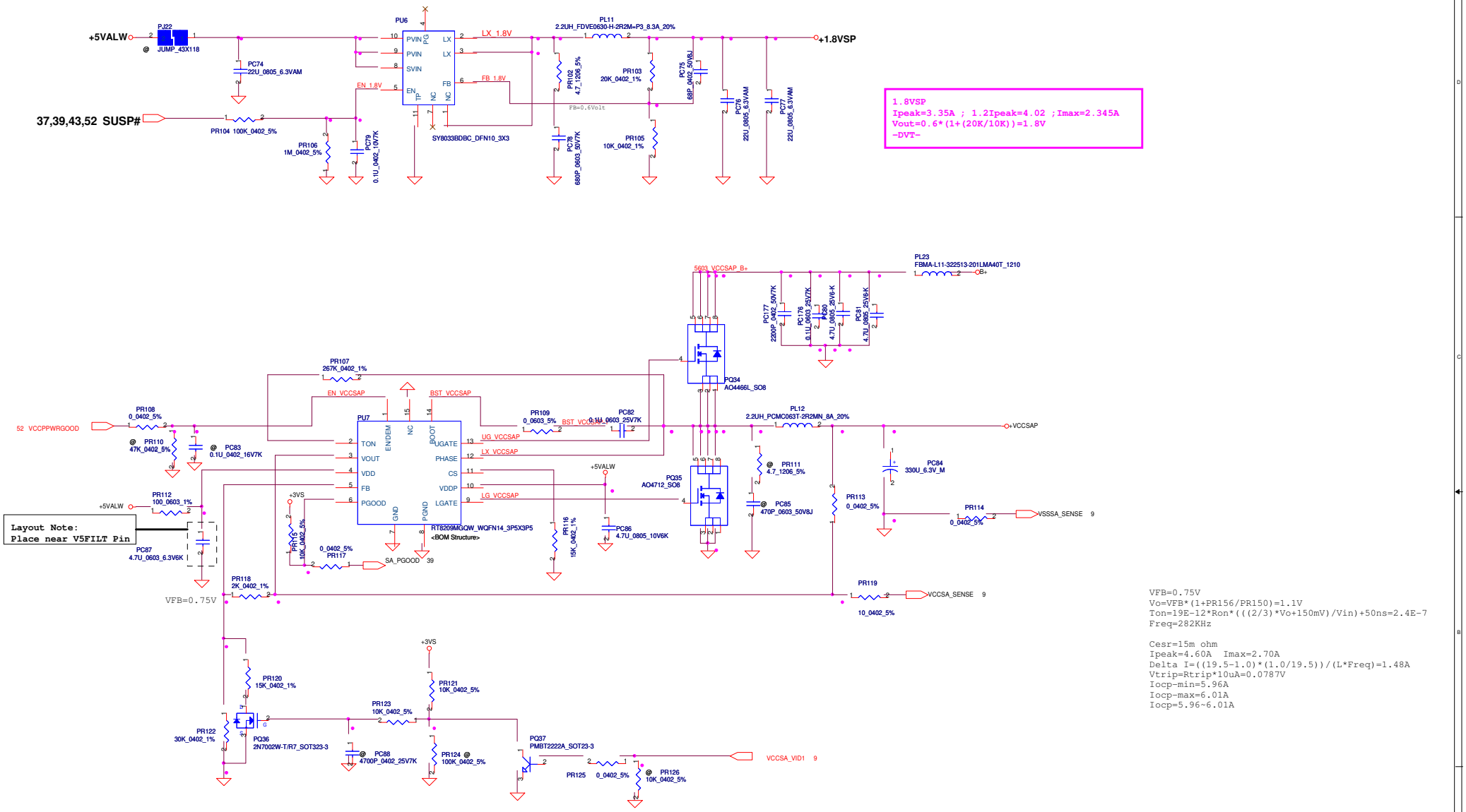

VFB=0.75V
Vo=VFB*(1+PR156/PR150)=1.1V
Ton=19E-12*Ron*(((2/3)*Vo+150mV)/Vin)+50ns=2.4E-7
Freq=282KHz

Cesr=15m ohm
Ipeak=4.60A Imax=2.70A
Delta I=((19.5-1.0)*(1.0/19.5))/(L*Freq)=1.48A
Vtrip=Rtrip*10uA=0.0787V
Iocp-min=5.96A
Iocp-max=6.01A
Iocp=5.96~6.01A

VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

+VCCSAP
Ipeak=6A , Imax=4.2A, 1.2Ipeak=7.2A
DCR= 9 m(typ)~10 m(max)
Rlimit=12K,Rdson=15~18mohm
Ilimit=10uA
Iocp=Rlimit/Rdson*10^(-5)= 7.59~10.654A

the resister change
from @ to pop component

Add two jumpers on the HW's output cap of the
+VCCSA's PIN(+) and PIN(-) to sense the
feedback voltage for VCCSA_SENSE & VSSSA_SENSE.

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size: C | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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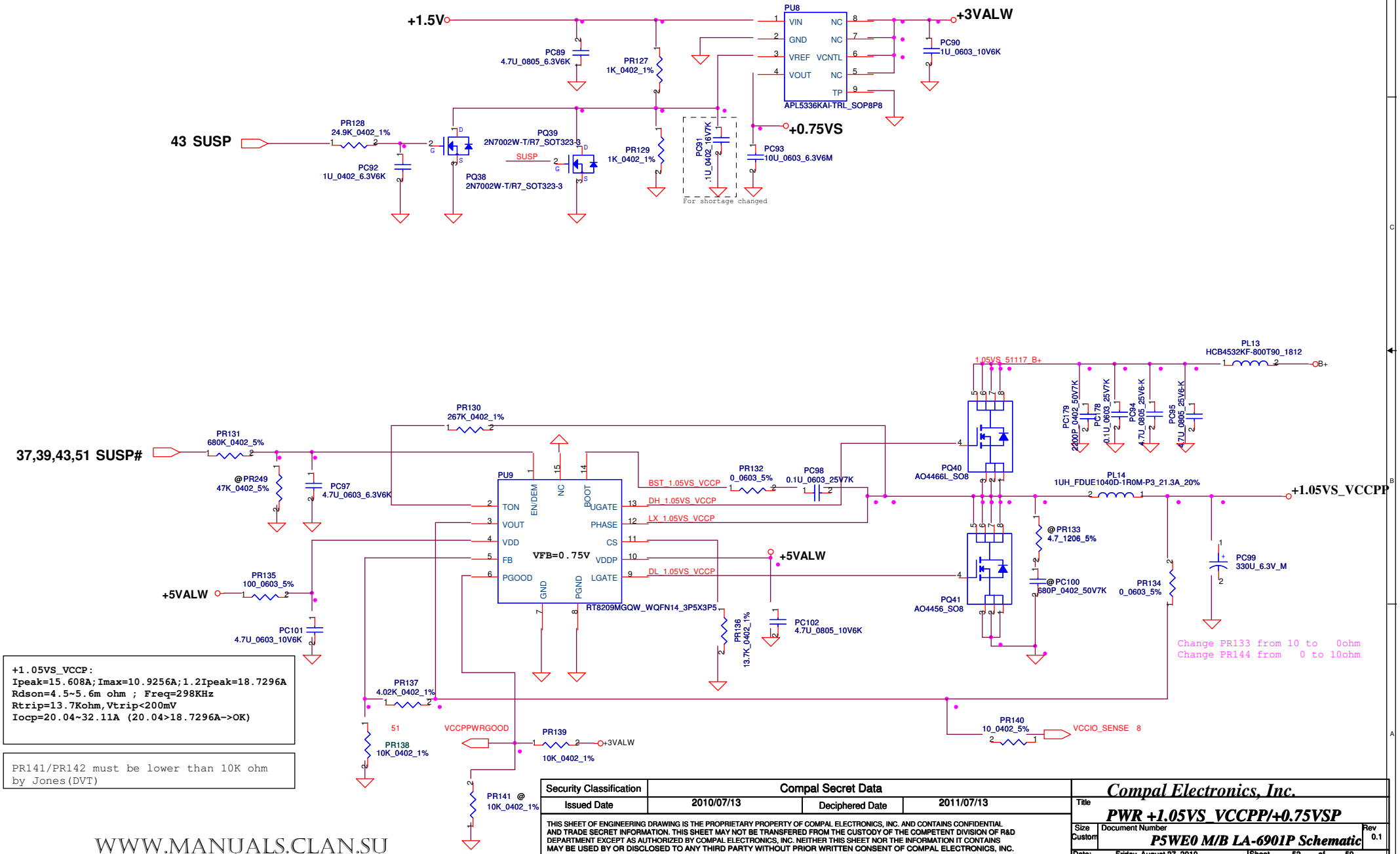


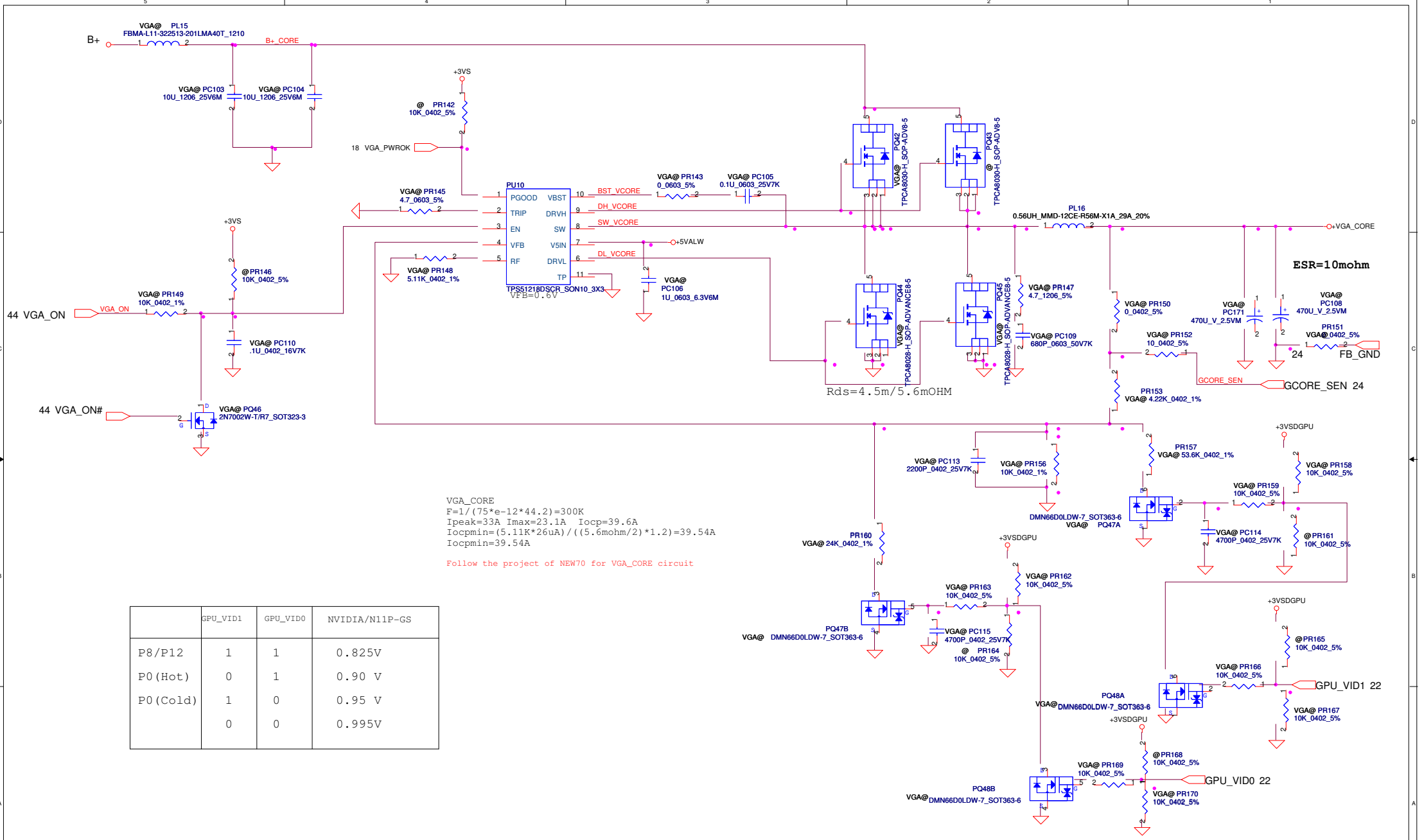
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 52 of 59



VGA_CORE
F=1/(75*e-12*44.2)=300K
Ipeak=33A Imax=23.1A Iocp=39.6A
Iocpmin=(5.11K*26uA)/((5.6mohm/2)*1.2)=39.54A
Iocpmin=39.54A

Follow the project of NEW70 for VGA_CORE circuit

	GPU_VID1	GPU_VID0	NVIDIA/N11P-GS
P8/P12	1	1	0.825V
P0(Hot)	0	1	0.90 V
P0(Cold)	1	0	0.95 V
	0	0	0.995V

Security Classification	Compal Secret Data		AP
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: +VGA_COREP

Size	Document Number	Rev
Custom	P5WE0	0.1

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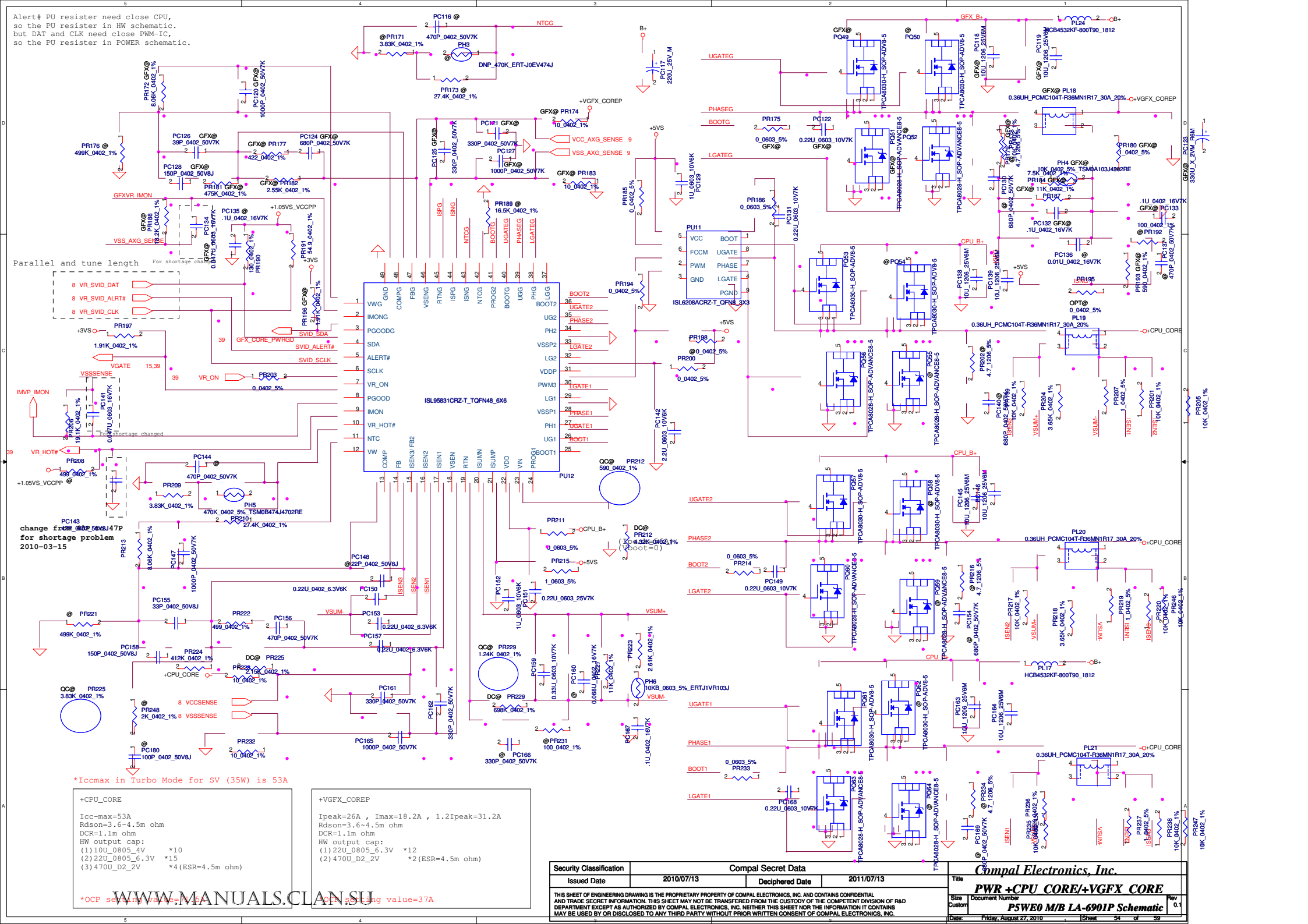

Version change list (P.I.R. List) for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Shut down for PWM3 pin floating	IF the PWM3 no used, please pull high it for +5VS and not floating	0.1	P.55	(1)Add PR638(0_0603_5%) between PWM3 and +5VS (2)connect the ISNG to +5VS	2010-03-29	DVT
2	OVP problem with PWR and HW side	If the HW side is 0V, through the jumper will cause the sense pin to over the votage setting and it may happen OVP problem.	0.1	P.55	Change the +VGFX_CORE to +VGFX_COREP	2010-03-29	DVT
3							

COMPAL ELECTRONICS

Title: <Title> PIR POWER1

Size: A | Document Number: PAW00(LA-6361P) | Rev: 0.1

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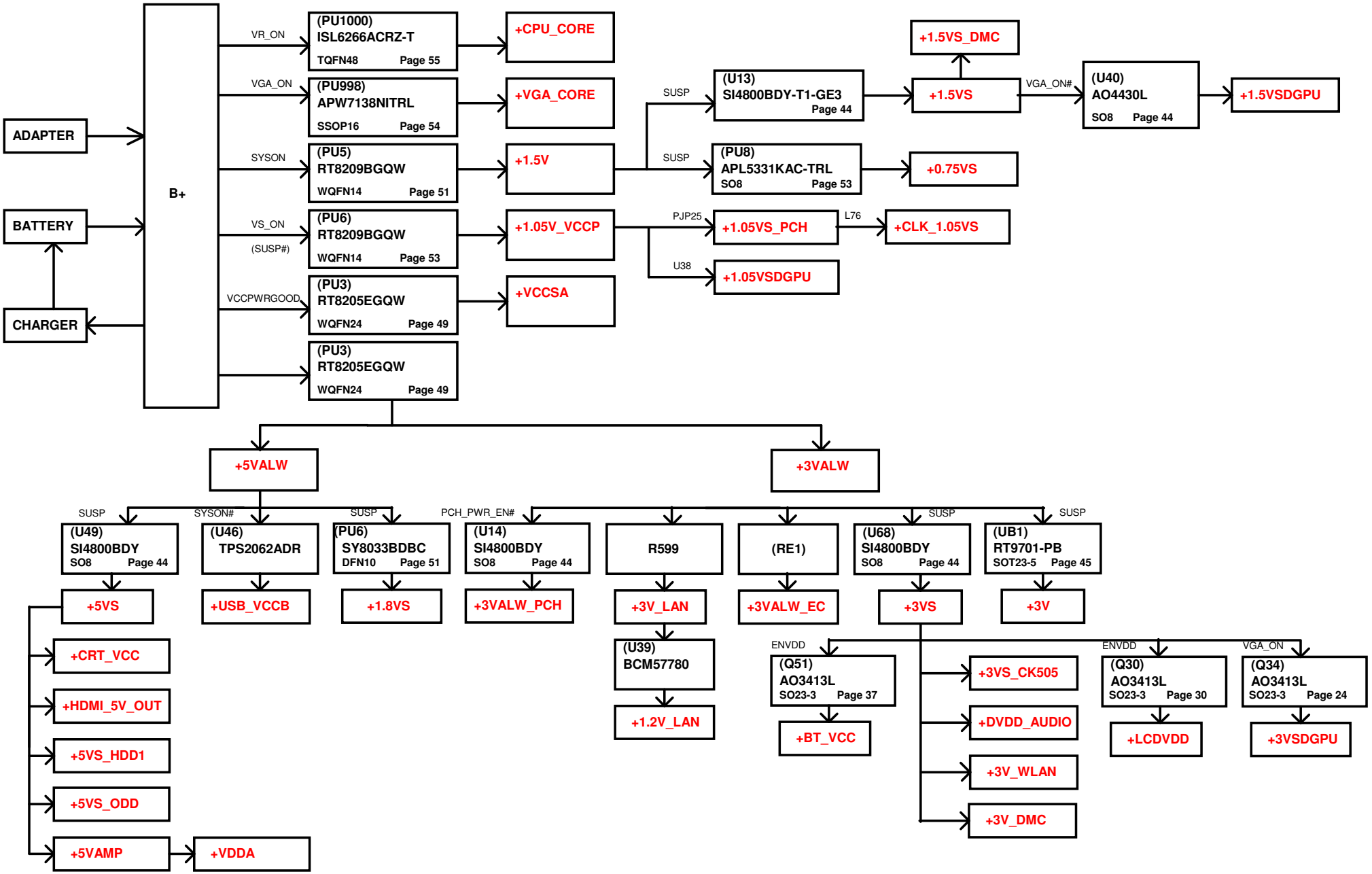

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: Power Rail

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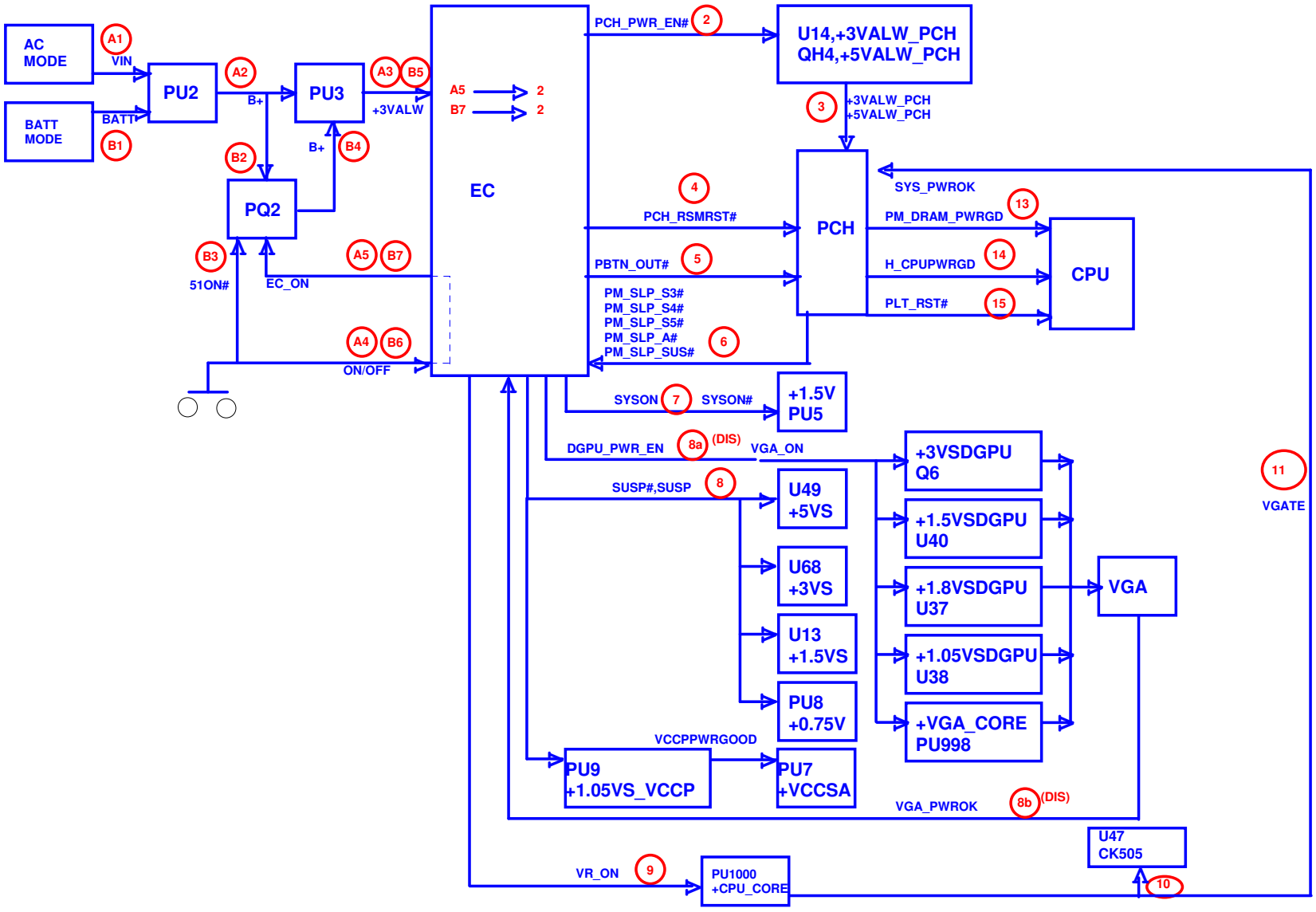

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

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Title: EE P.I.R (2)

Size	Document Number	Rev
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