Compal Confidential

Model Name : QILE1 & QILE2
File Name : LA-8131P, LA-8132P
BOM P/N:

QILE1:
4319GG39L01 : SMT MB A8131 QILE1 DIS-N13P
4319GG39L02 : SMT MB A8131 QILE1 DIS GPU-N13M
4319GG39L03 : SMT MB A8131 QILE1 UMA

QILE2:
4319GJ39L01 : SMT MB A8133 QILE2 DIS-N13P
4319GJ39L02 : SMT MB A8133 QILE2 DIS GPU-N13M
4319GJ39L03 : SMT MB A8133 QILE2 UMA

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M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

GPU nVIDIA N13M-GE1 / N13P-GL

2011-12-20

REV:0.6

Security Classification	Compal Secret Data		
Issued Date	**2011/07/12**	Deciphered Date	**2012/07/01**

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Title	**Cover Sheet**	
Size Custom	Document Number **LA-8131P**	Rev 0.6
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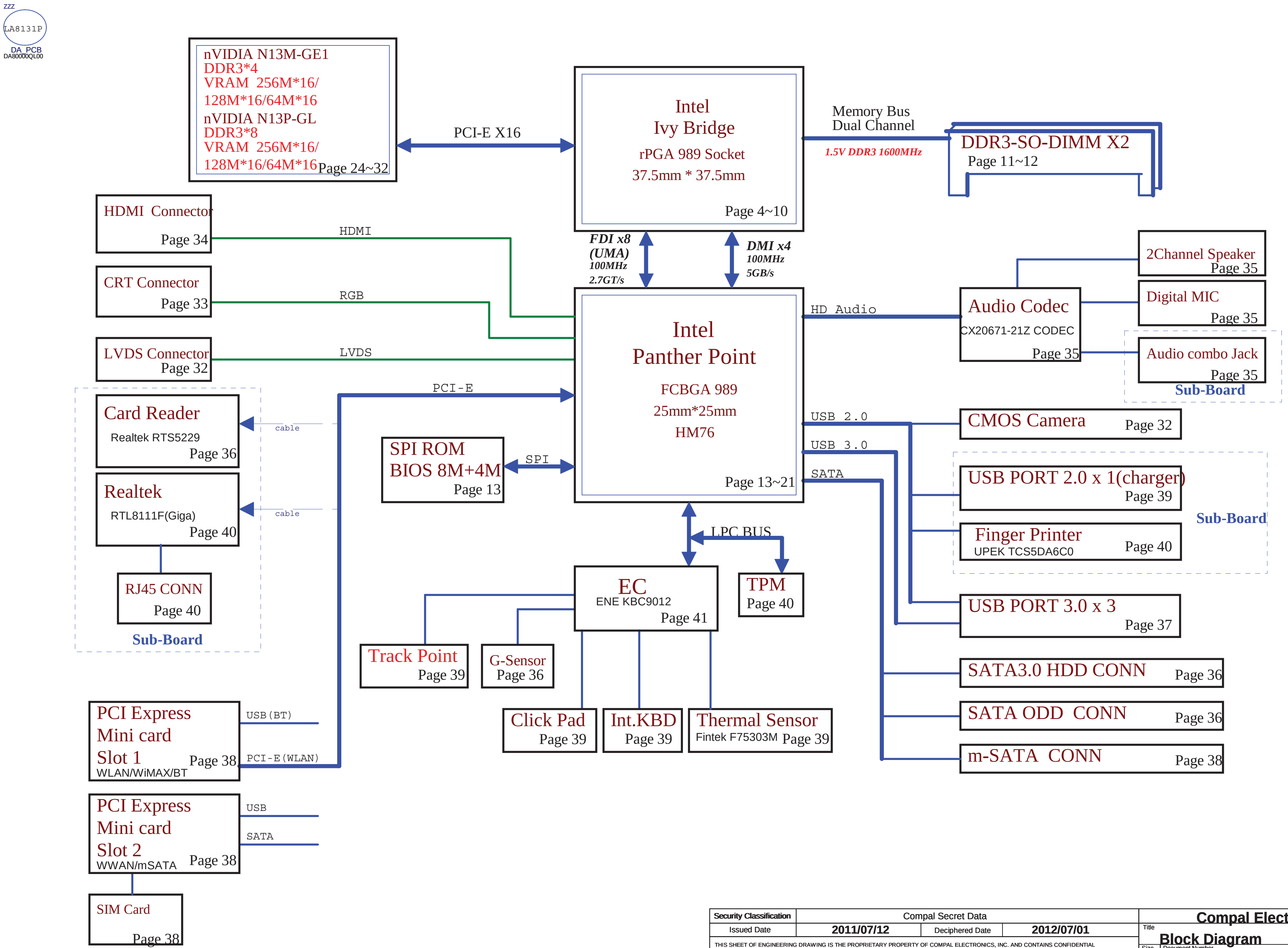

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Block Diagram

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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM
S0	O	O	O	O	O M3 Supported
S3	O	O	O	X	O M3 Supported
S5 S4/AC	O	O	X	X	O M3 Supported
S5 S4/ Battery only	X	X	X	X	
S5 S4/AC & Battery don't exist	X	X	X	X	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	
7	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB 3.0 Port (Left Side)
	UHCI1	2	USB 3.0 Port (Left Side)
		3	USB 3.0 Port (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB Port (Right Side)
	UHCI5	10	Mini Card(WLAN/BT)
		11	FPR
	UHCI6	12	Mini Card(WWAN)
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
Connector	CONN@
45 LEVEL	45@
Unpop	@
nVidia	DIS@
INTEL DD3 M3	M3@
SIM Card Slot	3G@
Intel UMA	UMA@
VRAM Option	X76@
Intel SBA	SBA@
Intel AOAC	AOAC@
TPM	TPM@
GPU N13M	N13M@
GPU N13P	N13MP

SMBUS Control Table

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

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Notes List

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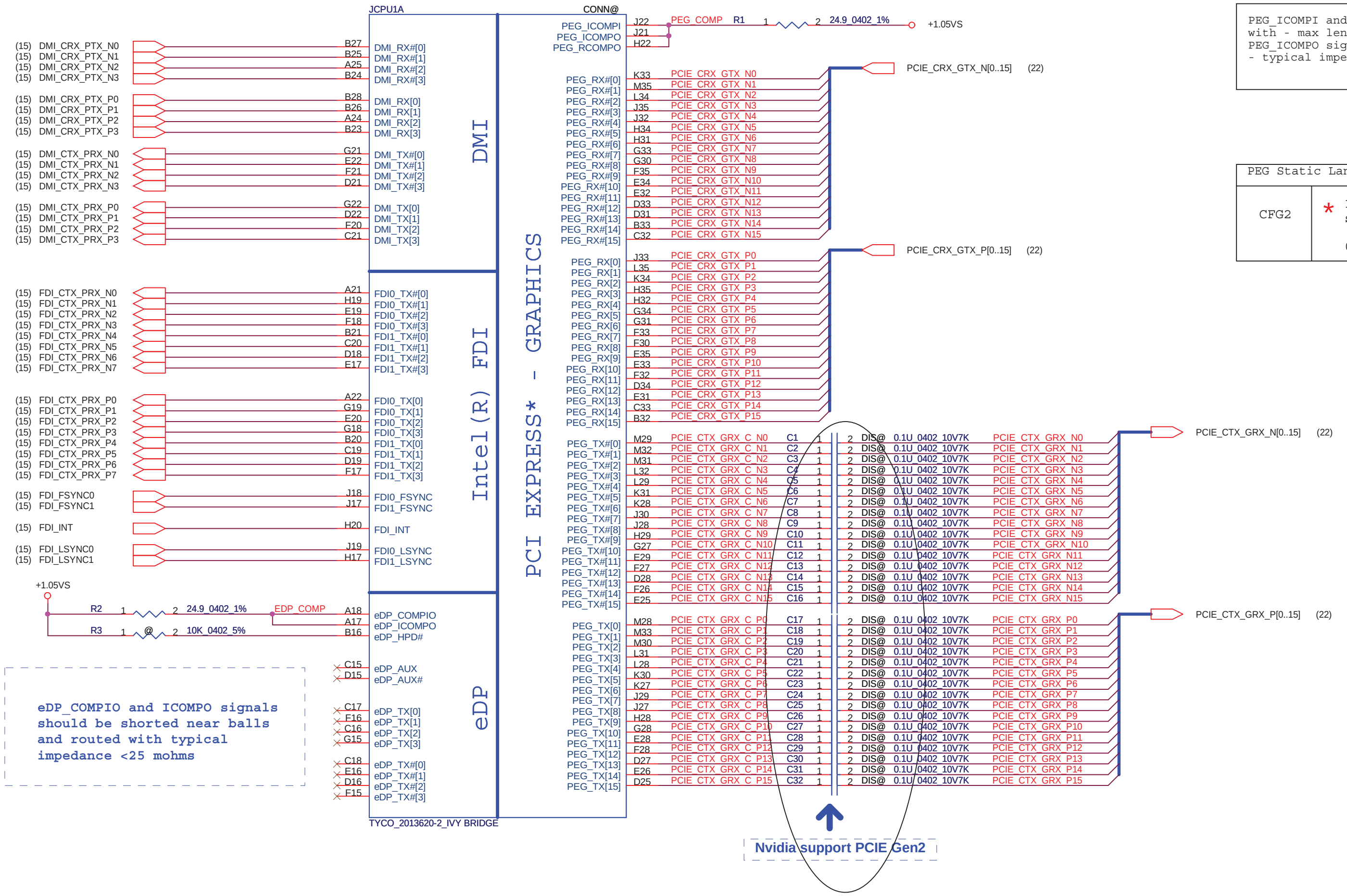
JCPU1A
CONN@
DMI
Intel(R) FDI
eDP
PCI EXPRESS* - GRAPHICS
TYCO_2013620-2_IVY BRIDGE
(15) DMI_CRX_PTX_N0
(15) DMI_CRX_PTX_N1
(15) DMI_CRX_PTX_N2
(15) DMI_CRX_PTX_N3
(15) DMI_CRX_PTX_P0
(15) DMI_CRX_PTX_P1
(15) DMI_CRX_PTX_P2
(15) DMI_CRX_PTX_P3
(15) DMI_CTX_PRX_N0
(15) DMI_CTX_PRX_N1
(15) DMI_CTX_PRX_N2
(15) DMI_CTX_PRX_N3
(15) DMI_CTX_PRX_P0
(15) DMI_CTX_PRX_P1
(15) DMI_CTX_PRX_P2
(15) DMI_CTX_PRX_P3
B27 DMI_RX#[0]
B25 DMI_RX#[1]
A25 DMI_RX#[2]
B24 DMI_RX#[3]
B28 DMI_RX[0]
B26 DMI_RX[1]
A24 DMI_RX[2]
B23 DMI_RX[3]
G21 DMI_TX#[0]
E22 DMI_TX#[1]
F21 DMI_TX#[2]
D21 DMI_TX#[3]
G22 DMI_TX[0]
D22 DMI_TX[1]
F20 DMI_TX[2]
C21 DMI_TX[3]
(15) FDI_CTX_PRX_N0
(15) FDI_CTX_PRX_N1
(15) FDI_CTX_PRX_N2
(15) FDI_CTX_PRX_N3
(15) FDI_CTX_PRX_N4
(15) FDI_CTX_PRX_N5
(15) FDI_CTX_PRX_N6
(15) FDI_CTX_PRX_N7
A21 FDI0_TX#[0]
H19 FDI0_TX#[1]
E19 FDI0_TX#[2]
F18 FDI0_TX#[3]
B21 FDI1_TX#[0]
C20 FDI1_TX#[1]
D18 FDI1_TX#[2]
E17 FDI1_TX#[3]
(15) FDI_CTX_PRX_P0
(15) FDI_CTX_PRX_P1
(15) FDI_CTX_PRX_P2
(15) FDI_CTX_PRX_P3
(15) FDI_CTX_PRX_P4
(15) FDI_CTX_PRX_P5
(15) FDI_CTX_PRX_P6
(15) FDI_CTX_PRX_P7
A22 FDI0_TX[0]
G19 FDI0_TX[1]
E20 FDI0_TX[2]
G18 FDI0_TX[3]
B20 FDI1_TX[0]
C19 FDI1_TX[1]
D19 FDI1_TX[2]
F17 FDI1_TX[3]
(15) FDI_FSYNC0
(15) FDI_FSYNC1
J18 FDI0_FSYNC
J17 FDI1_FSYNC
(15) FDI_INT
H20 FDI_INT
(15) FDI_LSYNC0
(15) FDI_LSYNC1
J19 FDI0_LSYNC
H17 FDI1_LSYNC
+1.05VS
R2 1 2 24.9_0402_1%
EDP_COMP
R3 1 @ 2 10K_0402_5%
A18 eDP_COMPIO
A17 eDP_ICOMPO
B16 eDP_HPD#
C15 eDP_AUX
D15 eDP_AUX#
C17 eDP_TX[0]
F16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
F15 eDP_TX#[3]
PEG_ICOMPI J22
PEG_ICOMPO J21
PEG_RCOMPO H22
PEG_COMP
R1 1 2 24.9_0402_1%
+1.05VS
PEG_RX#[0] K33 PCIE_CRX_GTX_N0
PEG_RX#[1] M35 PCIE_CRX_GTX_N1
PEG_RX#[2] L34 PCIE_CRX_GTX_N2
PEG_RX#[3] J35 PCIE_CRX_GTX_N3
PEG_RX#[4] J32 PCIE_CRX_GTX_N4
PEG_RX#[5] H34 PCIE_CRX_GTX_N5
PEG_RX#[6] H31 PCIE_CRX_GTX_N6
PEG_RX#[7] G33 PCIE_CRX_GTX_N7
PEG_RX#[8] G30 PCIE_CRX_GTX_N8
PEG_RX#[9] F35 PCIE_CRX_GTX_N9
PEG_RX#[10] E34 PCIE_CRX_GTX_N10
PEG_RX#[11] E32 PCIE_CRX_GTX_N11
PEG_RX#[12] D33 PCIE_CRX_GTX_N12
PEG_RX#[13] D31 PCIE_CRX_GTX_N13
PEG_RX#[14] B33 PCIE_CRX_GTX_N14
PEG_RX#[15] C32 PCIE_CRX_GTX_N15
PCIE_CRX_GTX_N[0..15] (22)
PEG_RX[0] J33 PCIE_CRX_GTX_P0
PEG_RX[1] L35 PCIE_CRX_GTX_P1
PEG_RX[2] K34 PCIE_CRX_GTX_P2
PEG_RX[3] H35 PCIE_CRX_GTX_P3
PEG_RX[4] H32 PCIE_CRX_GTX_P4
PEG_RX[5] G34 PCIE_CRX_GTX_P5
PEG_RX[6] G31 PCIE_CRX_GTX_P6
PEG_RX[7] F33 PCIE_CRX_GTX_P7
PEG_RX[8] F30 PCIE_CRX_GTX_P8
PEG_RX[9] E35 PCIE_CRX_GTX_P9
PEG_RX[10] E33 PCIE_CRX_GTX_P10
PEG_RX[11] F32 PCIE_CRX_GTX_P11
PEG_RX[12] D34 PCIE_CRX_GTX_P12
PEG_RX[13] E31 PCIE_CRX_GTX_P13
PEG_RX[14] C33 PCIE_CRX_GTX_P14
PEG_RX[15] B32 PCIE_CRX_GTX_P15
PCIE_CRX_GTX_P[0..15] (22)
PEG_TX#[0] M29 PCIE_CTX_GRX_C_N0 C1 1 2 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N0
PEG_TX#[1] M32 PCIE_CTX_GRX_C_N1 C2 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N1
PEG_TX#[2] M31 PCIE_CTX_GRX_C_N2 C3 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N2
PEG_TX#[3] L32 PCIE_CTX_GRX_C_N3 C4 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N3
PEG_TX#[4] L29 PCIE_CTX_GRX_C_N4 C5 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N4
PEG_TX#[5] K31 PCIE_CTX_GRX_C_N5 C6 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N5
PEG_TX#[6] K28 PCIE_CTX_GRX_C_N6 C7 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N6
PEG_TX#[7] J30 PCIE_CTX_GRX_C_N7 C8 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N7
PEG_TX#[8] J28 PCIE_CTX_GRX_C_N8 C9 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N8
PEG_TX#[9] H29 PCIE_CTX_GRX_C_N9 C10 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N9
PEG_TX#[10] G27 PCIE_CTX_GRX_C_N10 C11 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N10
PEG_TX#[11] E29 PCIE_CTX_GRX_C_N11 C12 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N11
PEG_TX#[12] F27 PCIE_CTX_GRX_C_N12 C13 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N12
PEG_TX#[13] D28 PCIE_CTX_GRX_C_N13 C14 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N13
PEG_TX#[14] F26 PCIE_CTX_GRX_C_N14 C15 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N14
PEG_TX#[15] E25 PCIE_CTX_GRX_C_N15 C16 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_N15
PCIE_CTX_GRX_N[0..15] (22)
PEG_TX[0] M28 PCIE_CTX_GRX_C_P0 C17 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P0
PEG_TX[1] M33 PCIE_CTX_GRX_C_P1 C18 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P1
PEG_TX[2] M30 PCIE_CTX_GRX_C_P2 C19 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P2
PEG_TX[3] L31 PCIE_CTX_GRX_C_P3 C20 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P3
PEG_TX[4] L28 PCIE_CTX_GRX_C_P4 C21 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P4
PEG_TX[5] K30 PCIE_CTX_GRX_C_P5 C22 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P5
PEG_TX[6] K27 PCIE_CTX_GRX_C_P6 C23 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P6
PEG_TX[7] J29 PCIE_CTX_GRX_C_P7 C24 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P7
PEG_TX[8] J27 PCIE_CTX_GRX_C_P8 C25 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P8
PEG_TX[9] H28 PCIE_CTX_GRX_C_P9 C26 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P9
PEG_TX[10] G28 PCIE_CTX_GRX_C_P10 C27 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P10
PEG_TX[11] E28 PCIE_CTX_GRX_C_P11 C28 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P11
PEG_TX[12] F28 PCIE_CTX_GRX_C_P12 C29 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P12
PEG_TX[13] D27 PCIE_CTX_GRX_C_P13 C30 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P13
PEG_TX[14] E26 PCIE_CTX_GRX_C_P14 C31 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P14
PEG_TX[15] D25 PCIE_CTX_GRX_C_P15 C32 DIS@ 0.1U_0402_10V7K PCIE_CTX_GRX_P15
PCIE_CTX_GRX_P[0..15] (22)

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Nvidia support PCIE Gen2

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

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Title
PROCESSOR(1/7) DMI,FDI,PEG

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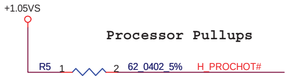

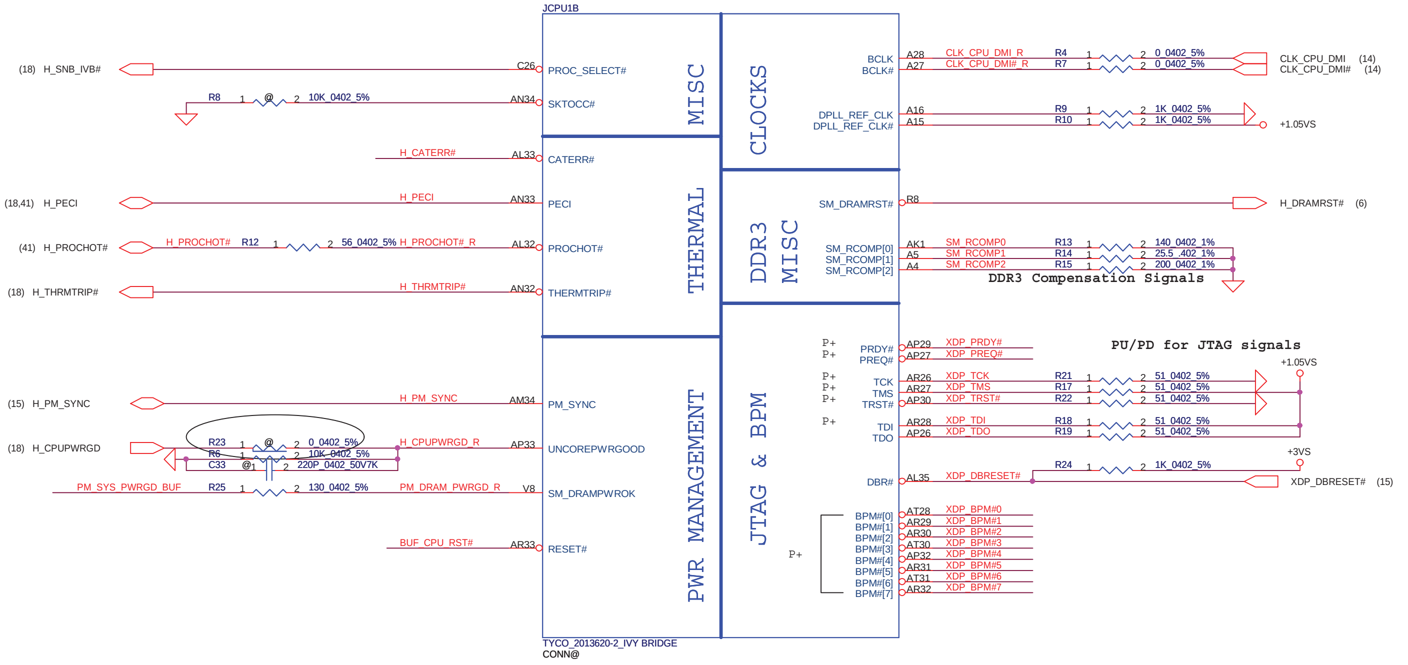

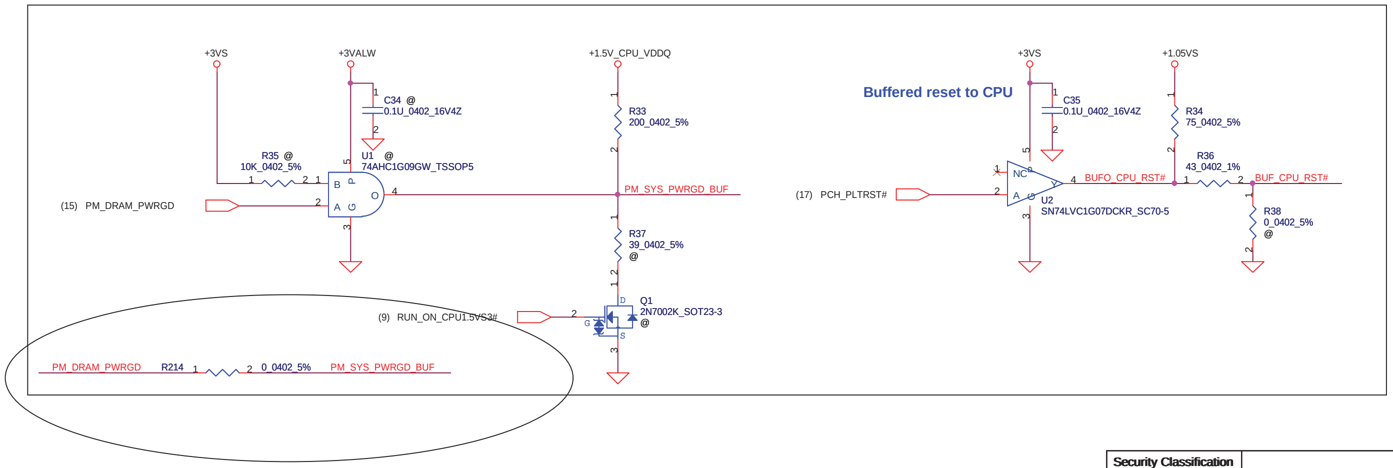

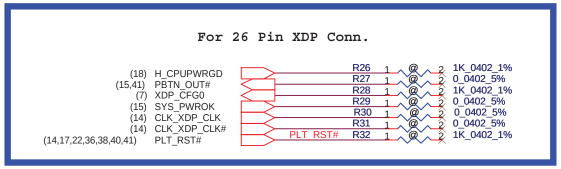
For 26 Pin XDP Conn.
(18) H_CPUPWRGD R26 1 @ 2 1K_0402_1%
(15,41) PBTN_OUT# R27 1 @ 2 0_0402_5%
(7) XDP_CFG0 R28 1 @ 2 1K_0402_1%
(15) SYS_PWROK R29 1 @ 2 0_0402_5%
(14) CLK_XDP_CLK R30 1 @ 2 0_0402_5%
(14) CLK_XDP_CLK# R31 1 @ 2 0_0402_5%
(14,17,22,36,38,40,41) PLT_RST# PLT_RST# R32 1 @ 2 1K_0402_1%

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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title PROCESSOR(2/7) PM,XDP,CLK
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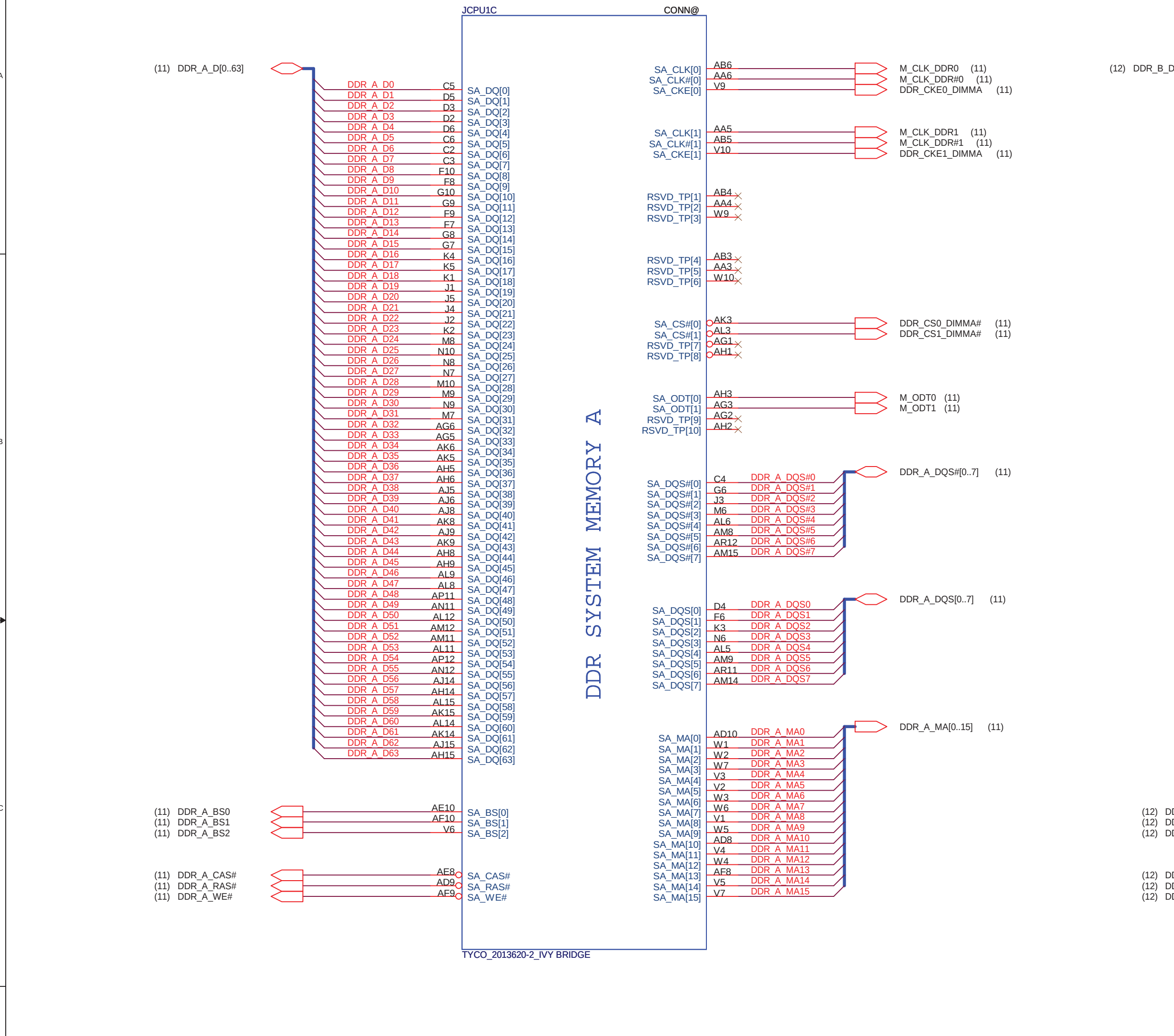
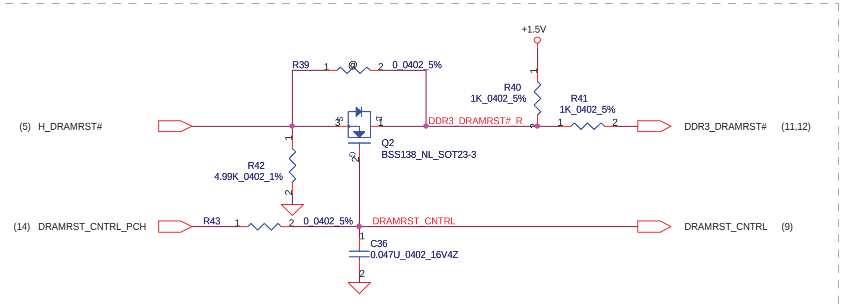
				Date: Friday, January 06, 2012 Sheet 5 of 58





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Title

PROCESSOR(3/7) DDRIII

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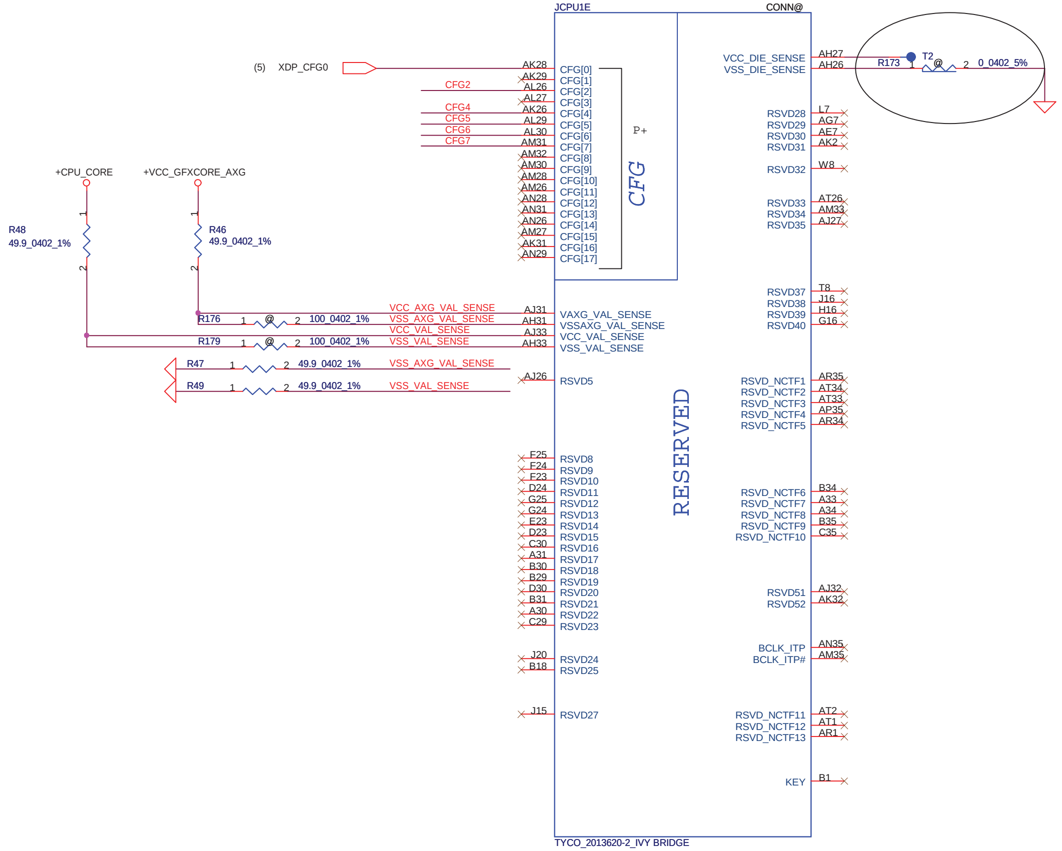
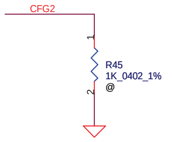
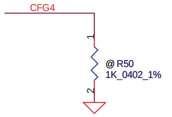


CFG Straps for Processor



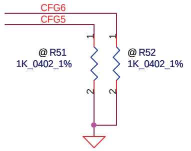
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



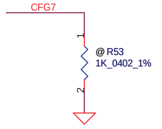
Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps

CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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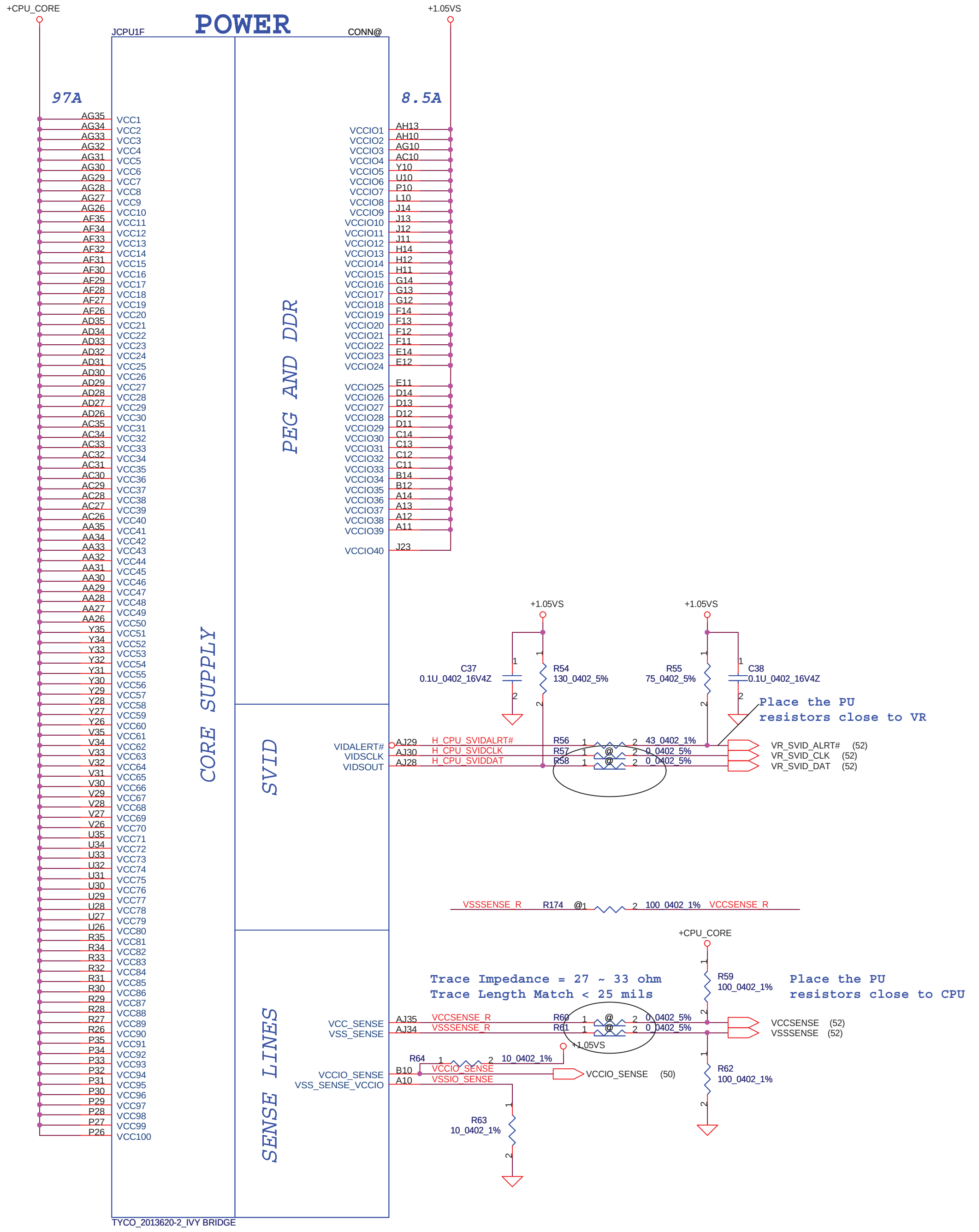
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title PROCESSOR(4/7) RSVD,CFG
				Size Custom Document Number LA-8131P Rev 0.6
				Date: Friday, January 06, 2012 Sheet 7 of 58



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Compal Electronics, Inc.

Title
PROCESSOR(5/7) PWR,BYPASS

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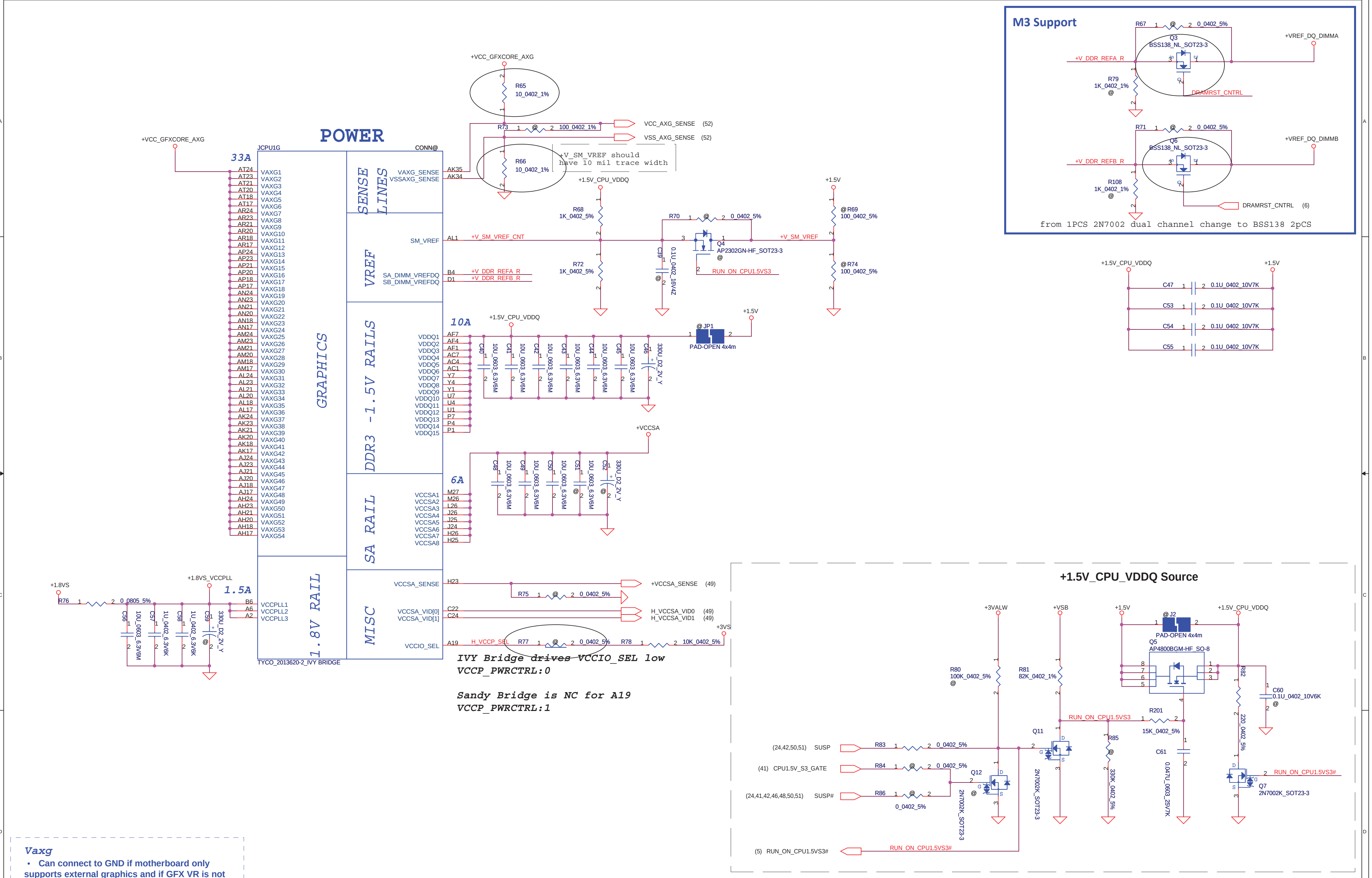


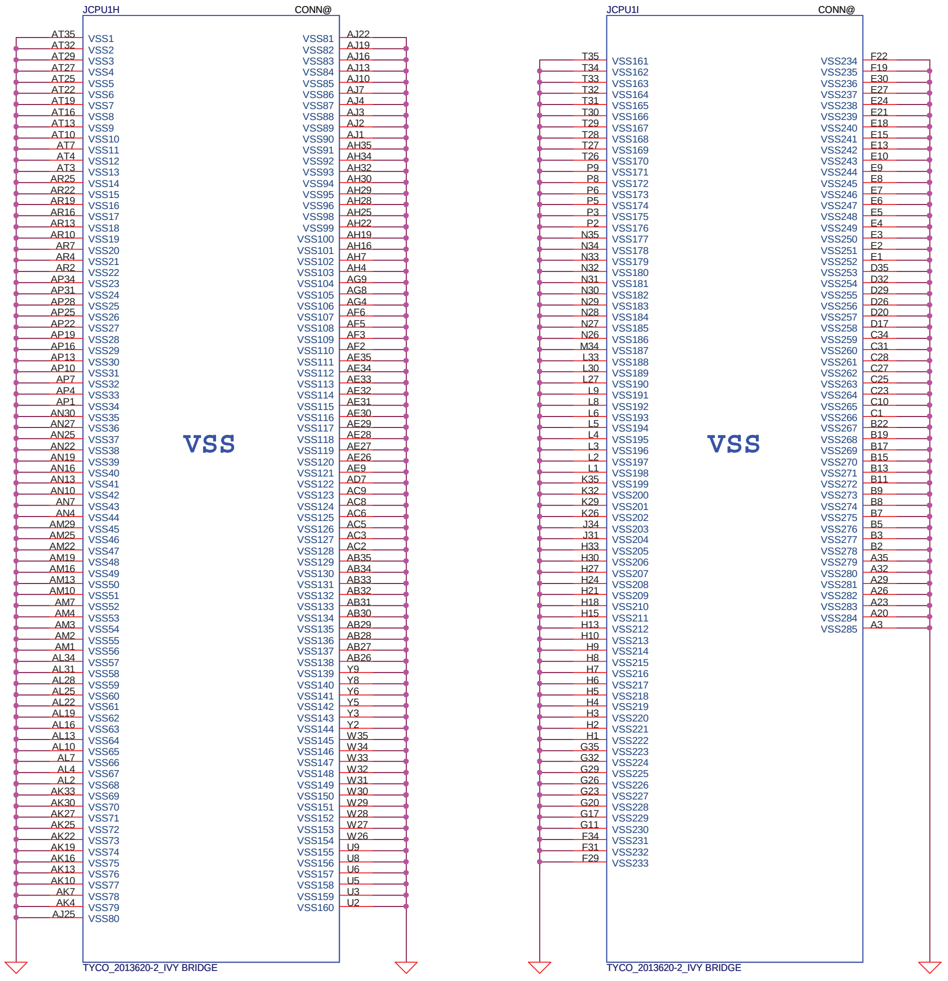
IVY Bridge drives VCCIO_SEL low
VCCP_PWRCTRL:0

Sandy Bridge is NC for A19
VCCP_PWRCTRL:1

Vaxg

- **Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,**
- **VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed**

Security Classification	Compal Secret Data			**Compal Electronics, Inc.**
Issued Date	**2011/07/12**	Deciphered Date	**2012/07/01**	Title **PROCESSOR(6/7) PWR**
				Size: Custom Document Number: **LA-8131P** Rev: 0.6
				Date: Friday, January 06, 2012 Sheet 9 of 58



Security Classification	Compal Secret Data		
Issued Date	**2011/07/12**	Deciphered Date	**2012/07/01**

Compal Electronics, Inc.

Title
PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	**LA-8131P**	0.6

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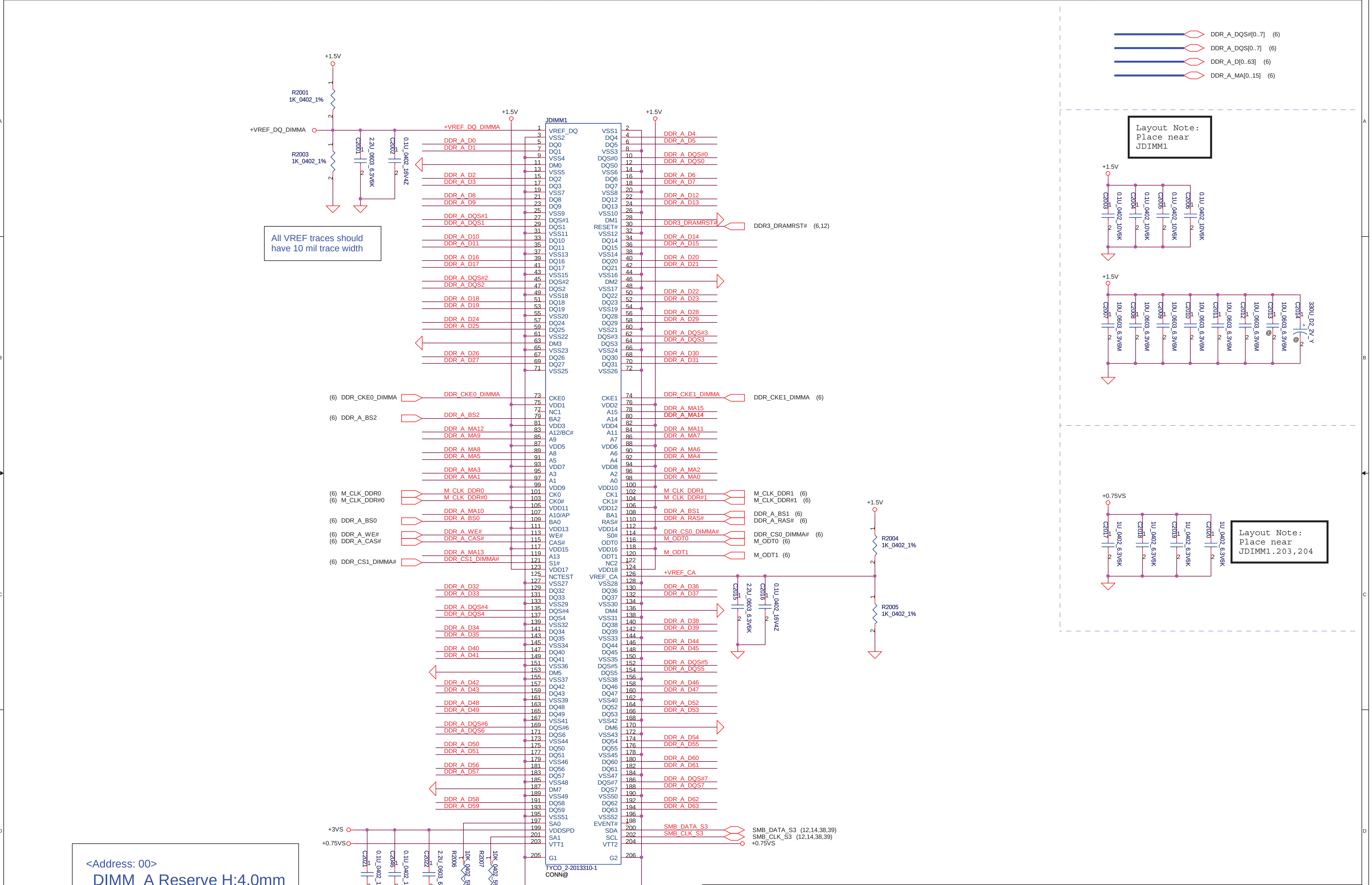
+1.5V
R2001
1K_0402_1%
R2003
1K_0402_1%
+VREF_DQ_DIMMA
C2001 2.2U_0603_6.3V6K
C2002 0.1U_0402_16V4Z
JDIMM1
+VREF_DQ_DIMMA
VREF_DQ VSS2 DQ0 DQ1 VSS4 DM0 VSS5 DQ2 DQ3 VSS7 DQ8 DQ9 VSS9 DQS#1 DQS1 VSS11 DQ10 DQ11 VSS13 DQ16 DQ17 VSS15 DQS#2 DQS2 VSS18 DQ18 DQ19 VSS20 DQ24 DQ25 VSS22 DM3 VSS23 DQ26 DQ27 VSS25
VSS1 DQ4 DQ5 VSS3 DQS#0 DQS0 VSS6 DQ6 DQ7 VSS8 DQ12 DQ13 VSS10 DM1 RESET# VSS12 DQ14 DQ15 VSS14 DQ20 DQ21 VSS16 DM2 VSS17 DQ22 DQ23 VSS19 DQ28 DQ29 VSS21 DQS#3 DQS3 VSS24 DQ30 DQ31 VSS26
DDR_A_D0 DDR_A_D1 DDR_A_D2 DDR_A_D3 DDR_A_D8 DDR_A_D9 DDR_A_DQS#1 DDR_A_DQS1 DDR_A_D10 DDR_A_D11 DDR_A_D16 DDR_A_D17 DDR_A_DQS#2 DDR_A_DQS2 DDR_A_D18 DDR_A_D19 DDR_A_D24 DDR_A_D25 DDR_A_D26 DDR_A_D27
DDR_A_D4 DDR_A_D5 DDR_A_DQS#0 DDR_A_DQS0 DDR_A_D6 DDR_A_D7 DDR_A_D12 DDR_A_D13 DDR3_DRAMRST# DDR_A_D14 DDR_A_D15 DDR_A_D20 DDR_A_D21 DDR_A_D22 DDR_A_D23 DDR_A_D28 DDR_A_D29 DDR_A_DQS#3 DDR_A_DQS3 DDR_A_D30 DDR_A_D31
DDR3_DRAMRST# (6,12)
(6) DDR_CKE0_DIMMA
(6) DDR_A_BS2
DDR_CKE0_DIMMA DDR_A_BS2 DDR_A_MA12 DDR_A_MA9 DDR_A_MA8 DDR_A_MA5 DDR_A_MA3 DDR_A_MA1 M_CLK_DDR0 M_CLK_DDR#0 DDR_A_MA10 DDR_A_BS0 DDR_A_WE# DDR_A_CAS# DDR_A_MA13 DDR_CS1_DIMMA#
CKE0 VDD1 NC1 BA2 VDD3 A12/BC# A9 VDD5 A8 A5 VDD7 A3 A1 VDD9 CK0 CK0# VDD11 A10/AP BA0 VDD13 WE# CAS# VDD15 A13 S1# VDD17 NCTEST
CKE1 VDD2 A15 A14 VDD4 A11 A7 VDD6 A6 A4 VDD8 A2 A0 VDD10 CK1 CK1# VDD12 BA1 RAS# VDD14 S0# ODT0 VDD16 ODT1 NC2 VDD18 VREF_CA
DDR_CKE1_DIMMA DDR_A_MA15 DDR_A_MA14 DDR_A_MA11 DDR_A_MA7 DDR_A_MA6 DDR_A_MA4 DDR_A_MA2 DDR_A_MA0 M_CLK_DDR1 M_CLK_DDR#1 DDR_A_BS1 DDR_A_RAS# DDR_CS0_DIMMA# M_ODT0 M_ODT1
DDR_CKE1_DIMMA (6)
(6) M_CLK_DDR0
(6) M_CLK_DDR#0
(6) DDR_A_BS0
(6) DDR_A_WE#
(6) DDR_A_CAS#
(6) DDR_CS1_DIMMA#
M_CLK_DDR1 (6)
M_CLK_DDR#1 (6)
DDR_A_BS1 (6)
DDR_A_RAS# (6)
DDR_CS0_DIMMA# (6)
M_ODT0 (6)
M_ODT1 (6)
+VREF_CA
C2015 2.2U_0603_6.3V6K
C2016 0.1U_0402_16V4Z
R2004 1K_0402_1%
R2005 1K_0402_1%
VSS27 DQ32 DQ33 VSS29 DQS#4 DQS4 VSS32 DQ34 DQ35 VSS34 DQ40 DQ41 VSS36 DM5 VSS37 DQ42 DQ43 VSS39 DQ48 DQ49 VSS41 DQS#6 DQS6 VSS44 DQ50 DQ51 VSS46 DQ56 DQ57 VSS48 DM7 VSS49 DQ58 DQ59 VSS51 SA0 VDDSPD SA1 VTT1 G1
VSS28 DQ36 DQ37 VSS30 DM4 VSS31 DQ38 DQ39 VSS33 DQ44 DQ45 VSS35 DQS#5 DQS5 VSS38 DQ46 DQ47 VSS40 DQ52 DQ53 VSS42 DM6 VSS43 DQ54 DQ55 VSS45 DQ60 DQ61 VSS47 DQS#7 DQS7 VSS50 DQ62 DQ63 VSS52 EVENT# SDA SCL VTT2 G2
DDR_A_D32 DDR_A_D33 DDR_A_DQS#4 DDR_A_DQS4 DDR_A_D34 DDR_A_D35 DDR_A_D40 DDR_A_D41 DDR_A_D42 DDR_A_D43 DDR_A_D48 DDR_A_D49 DDR_A_DQS#6 DDR_A_DQS6 DDR_A_D50 DDR_A_D51 DDR_A_D56 DDR_A_D57 DDR_A_D58 DDR_A_D59
DDR_A_D36 DDR_A_D37 DDR_A_D38 DDR_A_D39 DDR_A_D44 DDR_A_D45 DDR_A_DQS#5 DDR_A_DQS5 DDR_A_D46 DDR_A_D47 DDR_A_D52 DDR_A_D53 DDR_A_D54 DDR_A_D55 DDR_A_D60 DDR_A_D61 DDR_A_DQS#7 DDR_A_DQS7 DDR_A_D62 DDR_A_D63
SMB_DATA_S3 SMB_CLK_S3
SMB_DATA_S3 (12,14,38,39)
SMB_CLK_S3 (12,14,38,39)
+0.75VS
+3VS
+0.75VS
C2021 0.1U_0402_16V4Z
C2046 0.1U_0402_16V4Z
C2022 2.2U_0603_6.3V6K
R2006 10K_0402_5%
R2007 10K_0402_5%
@
TYCO_2-2013310-1
CONN@
DDR_A_DQS#[0..7] (6)
DDR_A_DQS[0..7] (6)
DDR_A_D[0..63] (6)
DDR_A_MA[0..15] (6)
C2003 0.1U_0402_10V6K
C2004 0.1U_0402_10V6K
C2005 0.1U_0402_10V6K
C2006 0.1U_0402_10V6K
C2007 10U_0603_6.3V6M
C2008 10U_0603_6.3V6M
C2009 10U_0603_6.3V6M
C2010 10U_0603_6.3V6M
C2011 10U_0603_6.3V6M
C2012 10U_0603_6.3V6M
C2013 10U_0603_6.3V6M
C2014 330U_D2_2V_Y
C2017 1U_0402_6.3V6K
C2018 1U_0402_6.3V6K
C2019 1U_0402_6.3V6K
C2020 1U_0402_6.3V6K

All VREF traces should have 10 mil trace width

Layout Note:
Place near
JDIMM1

Layout Note:
Place near
JDIMM1.203,204

<Address: 00>
DIMM_A Reserve H:4.0mm

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Title
DDRIII DIMMA

Size Custom
Document Number **LA-8131P**
Rev 0.6

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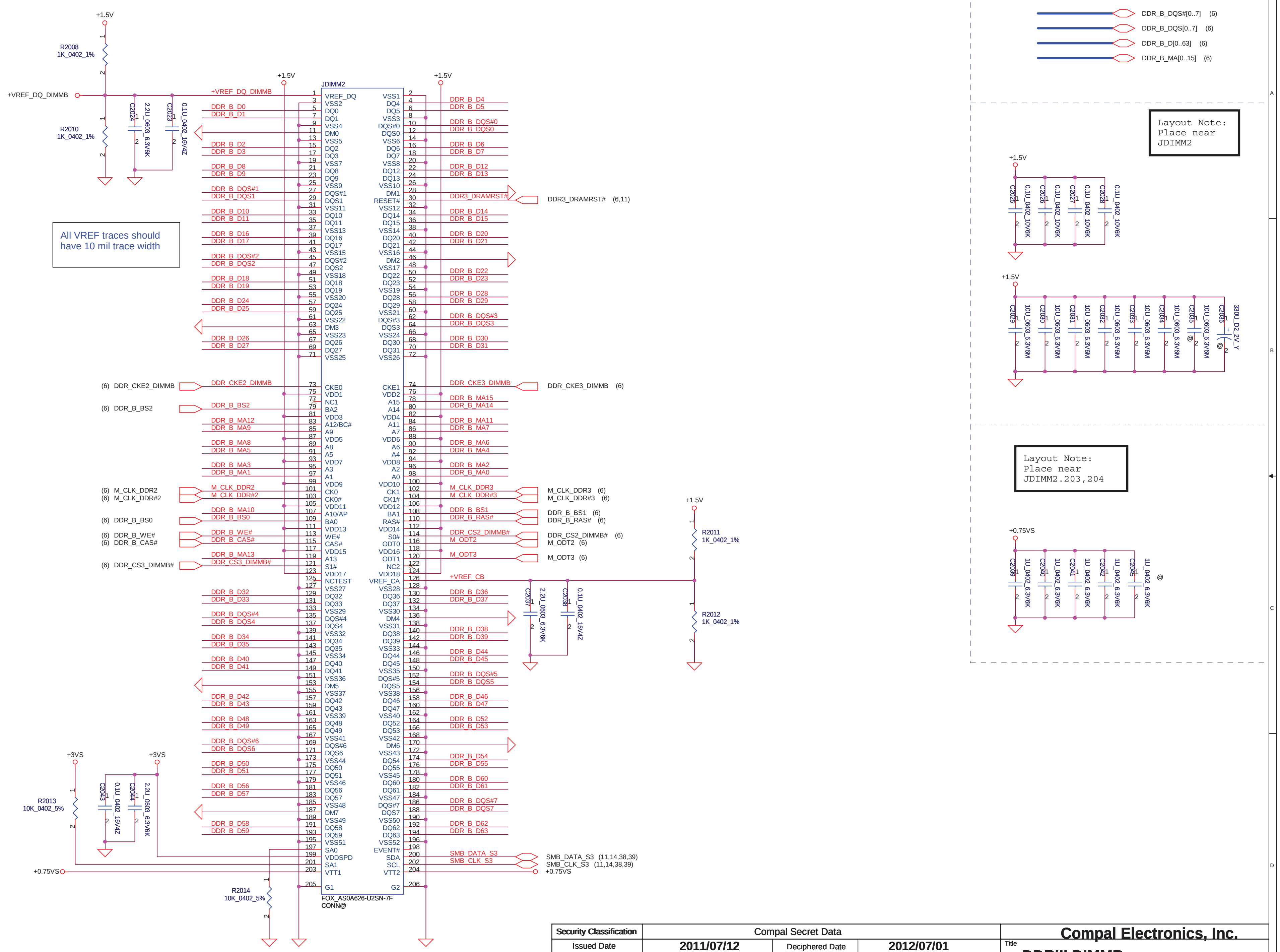

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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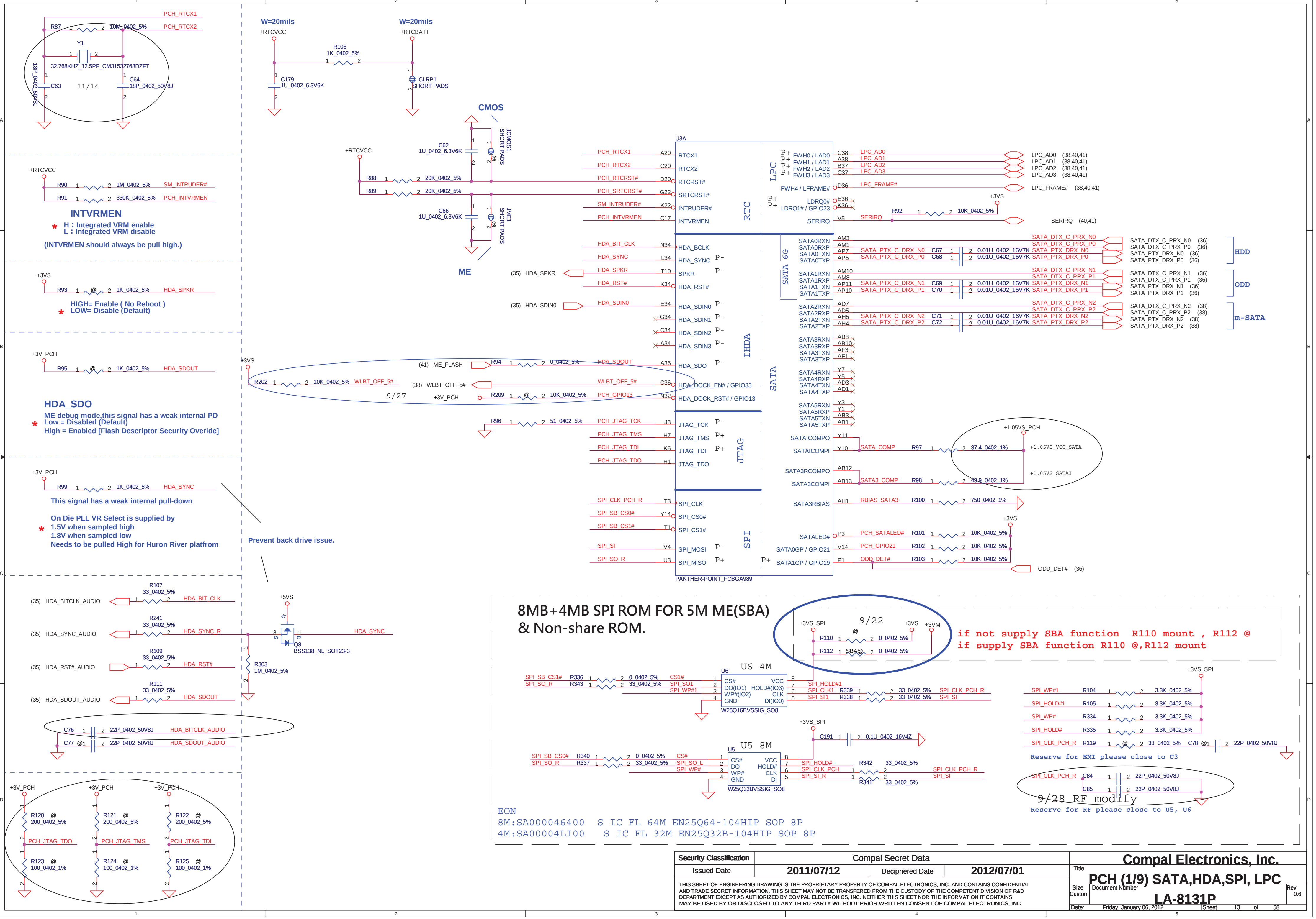
Compal Electronics, Inc.

Title
DDRIII DIMMB

Size	Document Number	Rev
Custom	LA-8131P	0.6

Date: Friday, January 06, 2012 Sheet 12 of 58


PCH_RTCX1
R87 1 2 10M_0402_5% PCH_RTCX2
Y1
32.768KHZ_12.5PF_CM31532768DZFT
18P_0402_50V8J C63
11/14
C64 18P_0402_50V8J
W=20mils
+RTCVCC
R106 1K_0402_5%
W=20mils
+RTCBATT
C179 1U_0402_6.3V6K
CLRP1 SHORT PADS
CMOS
JCMOS1 SHORT PADS
C62 1U_0402_6.3V6K
+RTCVCC
R88 1 2 20K_0402_5%
R89 1 2 20K_0402_5%
C66 1U_0402_6.3V6K
JME1 SHORT PADS
ME
+RTCVCC
R90 1M_0402_5% SM_INTRUDER#
R91 330K_0402_5% PCH_INTVRMEN
INTVRMEN
* H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)
+3VS
R93 @ 1K_0402_5% HDA_SPKR
* HIGH= Enable (No Reboot)
LOW= Disable (Default)
+3V_PCH
R95 @ 1K_0402_5% HDA_SDOUT
HDA_SDO
* ME debug mode,this signal has a weak internal PD
Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]
+3V_PCH
R99 1K_0402_5% HDA_SYNC
This signal has a weak internal pull-down
* On Die PLL VR Select is supplied by
1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom
Prevent back drive issue.
+3VS
(41) ME_FLASH R94 0_0402_5% HDA_SDOUT
R202 10K_0402_5% WLBT_OFF_5#
(38) WLBT_OFF_5# WLBT_OFF_5#
9/27
+3V_PCH R209 @ 10K_0402_5% PCH_GPIO13
R96 51_0402_5% PCH_JTAG_TCK
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
(35) HDA_SPKR
(35) HDA_SDIN0
U3A
PCH_RTCX1 A20 RTCX1
PCH_RTCX2 C20 RTCX2
PCH_RTCRST# D20 RTCRST#
PCH_SRTCRST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC
HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
A36 HDA_SDO
C36 HDA_DOCK_EN# / GPIO33
N32 HDA_DOCK_RST# / GPIO13
IHDA
J3 JTAG_TCK
H7 JTAG_TMS
K5 JTAG_TDI
H1 JTAG_TDO
JTAG
SPI_CLK_PCH_R T3 SPI_CLK
SPI_SB_CS0# Y14 SPI_CS0#
SPI_SB_CS1# T1 SPI_CS1#
SPI_SI V4 SPI_MOSI
SPI_SO_R U3 SPI_MISO
SPI
PANTHER-POINT_FCBGA989
LPC
FWH0 / LAD0 C38 LPC_AD0
FWH1 / LAD1 A38 LPC_AD1
FWH2 / LAD2 B37 LPC_AD2
FWH3 / LAD3 C37 LPC_AD3
FWH4 / LFRAME# D36 LPC_FRAME#
LDRQ0# E36
LDRQ1# / GPIO23 K36
SERIRQ V5 SERIRQ
LPC_AD0 (38,40,41)
LPC_AD1 (38,40,41)
LPC_AD2 (38,40,41)
LPC_AD3 (38,40,41)
LPC_FRAME# (38,40,41)
+3VS
R92 10K_0402_5%
SERIRQ (40,41)
SATA 6G
SATA0RXN AM3 SATA_DTX_C_PRX_N0
SATA0RXP AM1 SATA_DTX_C_PRX_P0
SATA0TXN AP7 SATA_PTX_C_DRX_N0 C67 0.01U_0402_16V7K SATA_PTX_DRX_N0
SATA0TXP AP5 SATA_PTX_C_DRX_P0 C68 0.01U_0402_16V7K SATA_PTX_DRX_P0
SATA_DTX_C_PRX_N0 (36)
SATA_DTX_C_PRX_P0 (36)
SATA_PTX_DRX_N0 (36)
SATA_PTX_DRX_P0 (36)
HDD
SATA1RXN AM10 SATA_DTX_C_PRX_N1
SATA1RXP AM8 SATA_DTX_C_PRX_P1
SATA1TXN AP11 SATA_PTX_C_DRX_N1 C69 0.01U_0402_16V7K SATA_PTX_DRX_N1
SATA1TXP AP10 SATA_PTX_C_DRX_P1 C70 0.01U_0402_16V7K SATA_PTX_DRX_P1
SATA_DTX_C_PRX_N1 (36)
SATA_DTX_C_PRX_P1 (36)
SATA_PTX_DRX_N1 (36)
SATA_PTX_DRX_P1 (36)
ODD
SATA2RXN AD7 SATA_DTX_C_PRX_N2
SATA2RXP AD5 SATA_DTX_C_PRX_P2
SATA2TXN AH5 SATA_PTX_C_DRX_N2 C71 0.01U_0402_16V7K SATA_PTX_DRX_N2
SATA2TXP AH4 SATA_PTX_C_DRX_P2 C72 0.01U_0402_16V7K SATA_PTX_DRX_P2
SATA_DTX_C_PRX_N2 (38)
SATA_DTX_C_PRX_P2 (38)
SATA_PTX_DRX_N2 (38)
SATA_PTX_DRX_P2 (38)
m-SATA
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATA
SATAICOMPO Y11
SATAICOMPI Y10 SATA_COMP R97 37.4_0402_1%
+1.05VS_PCH
+1.05VS_VCC_SATA
SATA3RCOMPO AB12
SATA3COMPI AB13 SATA3_COMP R98 49.9_0402_1%
+1.05VS_SATA3
SATA3RBIAS AH1 RBIAS_SATA3 R100 750_0402_1%
+3VS
SATALED# P3 PCH_SATALED# R101 10K_0402_5%
SATA0GP / GPIO21 V14 PCH_GPIO21 R102 10K_0402_5%
SATA1GP / GPIO19 P1 ODD_DET# R103 10K_0402_5%
ODD_DET# (36)
R107 33_0402_5%
(35) HDA_BITCLK_AUDIO HDA_BIT_CLK
R241 33_0402_5%
(35) HDA_SYNC_AUDIO HDA_SYNC_R
R109 33_0402_5%
(35) HDA_RST#_AUDIO HDA_RST#
R111 33_0402_5%
(35) HDA_SDOUT_AUDIO HDA_SDOUT
+5VS
Q8 BSS138_NL_SOT23-3
HDA_SYNC
R303 1M_0402_5%
C76 22P_0402_50V8J HDA_BITCLK_AUDIO
C77 @ 22P_0402_50V8J HDA_SDOUT_AUDIO
+3V_PCH +3V_PCH +3V_PCH
R120 @ 200_0402_5%
R121 @ 200_0402_5%
R122 @ 200_0402_5%
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_JTAG_TDI
R123 @ 100_0402_1%
R124 @ 100_0402_1%
R125 @ 100_0402_1%
8MB+4MB SPI ROM FOR 5M ME(SBA)
& Non-share ROM.
9/22
+3VS_SPI +3VS +3VM
R110 @ 0_0402_5%
R112 SBA@ 0_0402_5%
if not supply SBA function R110 mount , R112 @
if supply SBA function R110 @,R112 mount
U6 4M
SPI_SB_CS1# R336 0_0402_5% CS1#
SPI_SO_R R343 33_0402_5% SPI_SO1
SPI_WP#1
CS# VCC
DO(IO1) HOLD#(IO3)
WP#(IO2) CLK
GND DI(IO0)
SPI_HOLD#1
SPI_CLK1 R339 33_0402_5% SPI_CLK_PCH_R
SPI_SI1 R338 33_0402_5% SPI_SI
W25Q16BVSSIG_SO8
+3VS_SPI
C191 0.1U_0402_16V4Z
U5 8M
SPI_SB_CS0# R340 0_0402_5% CS#
SPI_SO_R R337 33_0402_5% SPI_SO_L
SPI_WP#
CS# VCC
DO HOLD#
WP# CLK
GND DI
SPI_HOLD#
SPI_CLK_PCH R342 33_0402_5% SPI_CLK_PCH_R
SPI_SI_R R341 33_0402_5% SPI_SI
W25Q32BVSSIG_SO8
+3VS_SPI
SPI_WP#1 R104 3.3K_0402_5%
SPI_HOLD#1 R105 3.3K_0402_5%
SPI_WP# R334 3.3K_0402_5%
SPI_HOLD# R335 3.3K_0402_5%
SPI_CLK_PCH_R R119 @ 33_0402_5% C78 @ 22P_0402_50V8J
Reserve for EMI please close to U3
SPI_CLK_PCH_R C84 22P_0402_50V8J
C85 22P_0402_50V8J
9/28 RF modify
Reserve for RF please close to U5, U6
EON
8M:SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P
4M:SA00004LI00 S IC FL 32M EN25Q32B-104HIP SOP 8P

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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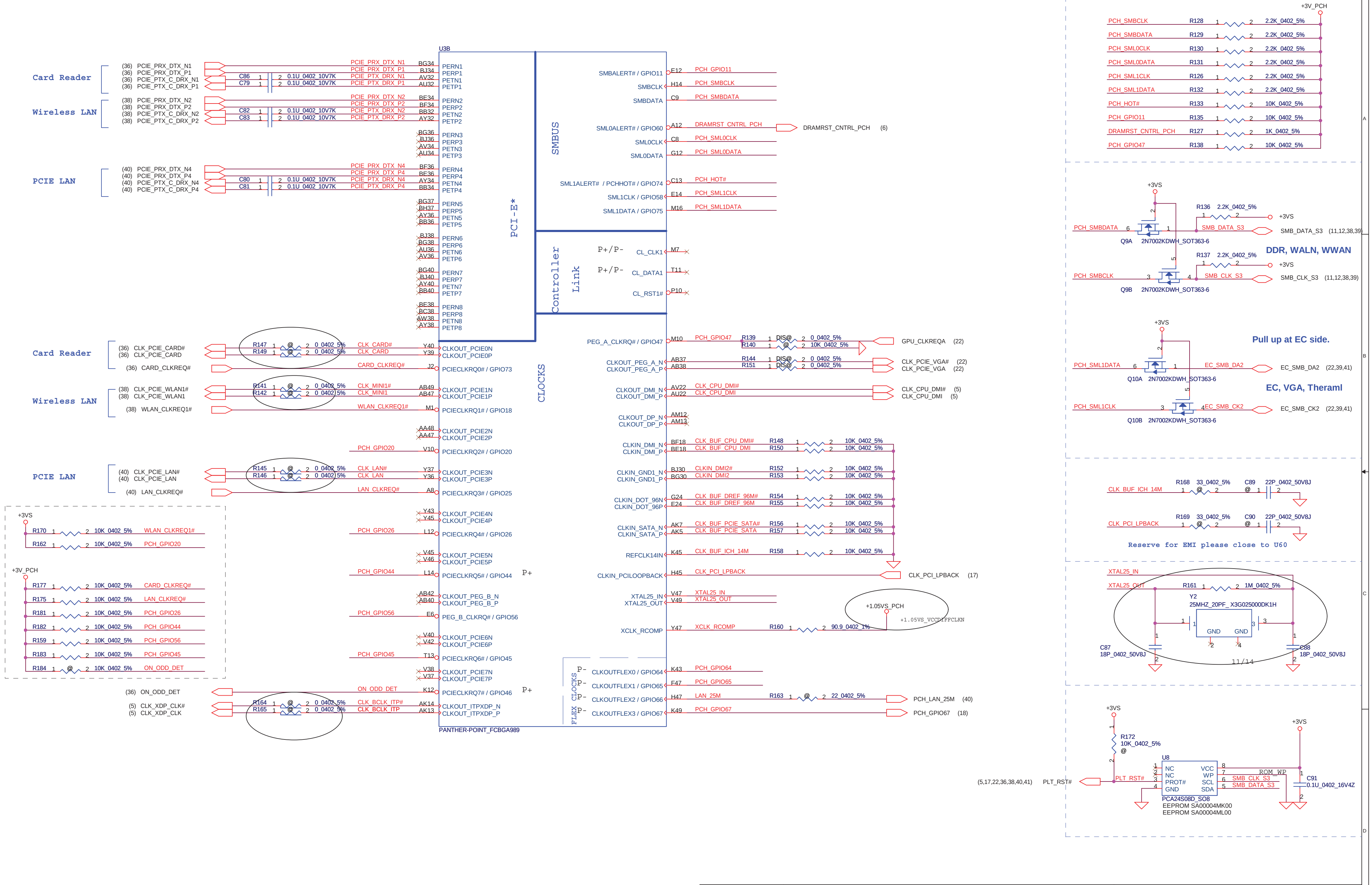
Compal Electronics, Inc.

Title
PCH (1/9) SATA,HDA,SPI, LPC

Size: Custom
Document Number: LA-8131P
Rev: 0.6
Date: Friday, January 06, 2012
Sheet 13 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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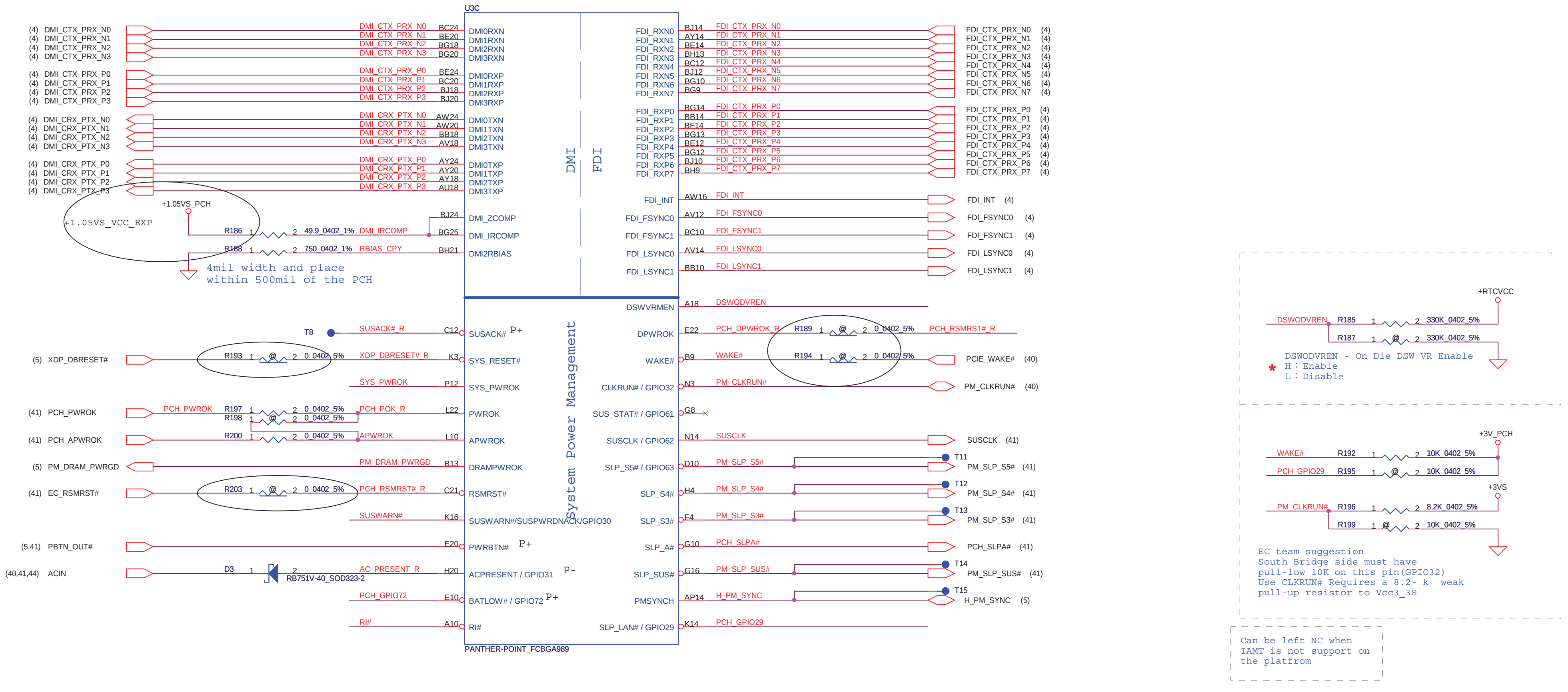
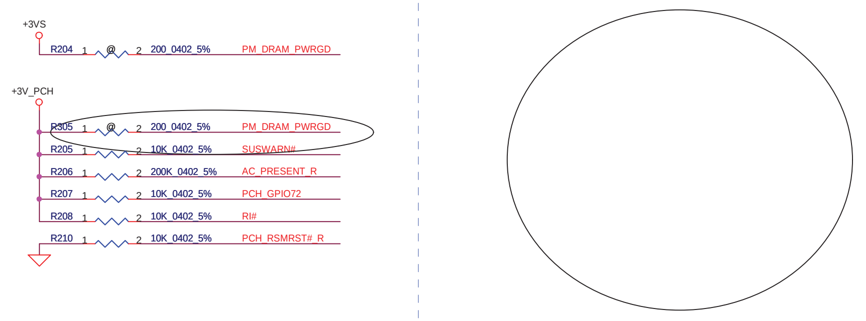
Compal Electronics, Inc.

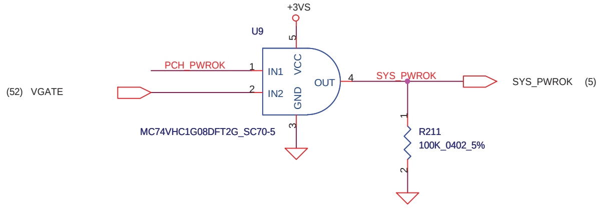
Title
PCH (2/8) PCIE, SMBUS, CLK

Size Custom
Document Number **LA-8131P**
Rev 0.6

Date: Friday, January 06, 2012 Sheet 14 of 58


U3C
(4) DMI_CTX_PRX_N0
(4) DMI_CTX_PRX_N1
(4) DMI_CTX_PRX_N2
(4) DMI_CTX_PRX_N3
(4) DMI_CTX_PRX_P0
(4) DMI_CTX_PRX_P1
(4) DMI_CTX_PRX_P2
(4) DMI_CTX_PRX_P3
(4) DMI_CRX_PTX_N0
(4) DMI_CRX_PTX_N1
(4) DMI_CRX_PTX_N2
(4) DMI_CRX_PTX_N3
(4) DMI_CRX_PTX_P0
(4) DMI_CRX_PTX_P1
(4) DMI_CRX_PTX_P2
(4) DMI_CRX_PTX_P3
BC24 DMI0RXN
BE20 DMI1RXN
BG18 DMI2RXN
BG20 DMI3RXN
BE24 DMI0RXP
BC20 DMI1RXP
BJ18 DMI2RXP
BJ20 DMI3RXP
AW24 DMI0TXN
AW20 DMI1TXN
BB18 DMI2TXN
AV18 DMI3TXN
AY24 DMI0TXP
AY20 DMI1TXP
AY18 DMI2TXP
AU18 DMI3TXP
+1.05VS_PCH
+1.05VS_VCC_EXP
BJ24 DMI_ZCOMP
R186 1 2 49.9_0402_1% DMI_IRCOMP BG25 DMI_IRCOMP
R188 1 2 750_0402_1% RBIAS_CPY BH21 DMI2RBIAS
4mil width and place within 500mil of the PCH
DMI
FDI
FDI_RXN0 BJ14 FDI_CTX_PRX_N0
FDI_RXN1 AY14 FDI_CTX_PRX_N1
FDI_RXN2 BE14 FDI_CTX_PRX_N2
FDI_RXN3 BH13 FDI_CTX_PRX_N3
FDI_RXN4 BC12 FDI_CTX_PRX_N4
FDI_RXN5 BJ12 FDI_CTX_PRX_N5
FDI_RXN6 BG10 FDI_CTX_PRX_N6
FDI_RXN7 BG9 FDI_CTX_PRX_N7
FDI_RXP0 BG14 FDI_CTX_PRX_P0
FDI_RXP1 BB14 FDI_CTX_PRX_P1
FDI_RXP2 BF14 FDI_CTX_PRX_P2
FDI_RXP3 BG13 FDI_CTX_PRX_P3
FDI_RXP4 BE12 FDI_CTX_PRX_P4
FDI_RXP5 BG12 FDI_CTX_PRX_P5
FDI_RXP6 BJ10 FDI_CTX_PRX_P6
FDI_RXP7 BH9 FDI_CTX_PRX_P7
FDI_CTX_PRX_N0 (4)
FDI_CTX_PRX_N1 (4)
FDI_CTX_PRX_N2 (4)
FDI_CTX_PRX_N3 (4)
FDI_CTX_PRX_N4 (4)
FDI_CTX_PRX_N5 (4)
FDI_CTX_PRX_N6 (4)
FDI_CTX_PRX_N7 (4)
FDI_CTX_PRX_P0 (4)
FDI_CTX_PRX_P1 (4)
FDI_CTX_PRX_P2 (4)
FDI_CTX_PRX_P3 (4)
FDI_CTX_PRX_P4 (4)
FDI_CTX_PRX_P5 (4)
FDI_CTX_PRX_P6 (4)
FDI_CTX_PRX_P7 (4)
FDI_INT AW16 FDI_INT — FDI_INT (4)
FDI_FSYNC0 AV12 FDI_FSYNC0 — FDI_FSYNC0 (4)
FDI_FSYNC1 BC10 FDI_FSYNC1 — FDI_FSYNC1 (4)
FDI_LSYNC0 AV14 FDI_LSYNC0 — FDI_LSYNC0 (4)
FDI_LSYNC1 BB10 FDI_LSYNC1 — FDI_LSYNC1 (4)
System Power Management
T8
SUSACK#_R C12 SUSACK# P+
(5) XDP_DBRESET# R193 1 @ 2 0_0402_5% XDP_DBRESET#_R K3 SYS_RESET#
SYS_PWROK P12 SYS_PWROK
(41) PCH_PWROK PCH_PWROK R197 1 2 0_0402_5% R198 1 @ 2 0_0402_5% PCH_POK_R L22 PWROK
(41) PCH_APWROK R200 1 2 0_0402_5% APWROK L10 APWROK
(5) PM_DRAM_PWRGD PM_DRAM_PWRGD B13 DRAMPWROK
(41) EC_RSMRST# R203 1 @ 2 0_0402_5% PCH_RSMRST#_R C21 RSMRST#
SUSWARN# K16 SUSWARN#/SUSPWRDNACK/GPIO30
(5,41) PBTN_OUT# E20 PWRBTN# P+
(40,41,44) ACIN D3 1 2 RB751V-40_SOD323-2 AC_PRESENT_R H20 ACPRESENT / GPIO31 P-
PCH_GPIO72 E10 BATLOW# / GPIO72 P+
RI# A10 RI#
PANTHER-POINT_FCBGA989
DSWVRMEN A18 DSWODVREN
DPWROK E22 PCH_DPWROK_R R189 1 @ 2 0_0402_5% PCH_RSMRST#_R
WAKE# B9 WAKE# R194 1 @ 2 0_0402_5% PCIE_WAKE# (40)
CLKRUN# / GPIO32 N3 PM_CLKRUN# — PM_CLKRUN# (40)
SUS_STAT# / GPIO61 G8
SUSCLK / GPIO62 N14 SUSCLK — SUSCLK (41)
SLP_S5# / GPIO63 D10 PM_SLP_S5# T11 PM_SLP_S5# (41)
SLP_S4# H4 PM_SLP_S4# T12 PM_SLP_S4# (41)
SLP_S3# F4 PM_SLP_S3# T13 PM_SLP_S3# (41)
SLP_A# G10 PCH_SLPA# — PCH_SLPA# (41)
SLP_SUS# G16 PM_SLP_SUS# T14 PM_SLP_SUS# (41)
PMSYNCH AP14 H_PM_SYNC T15 H_PM_SYNC (5)
SLP_LAN# / GPIO29 K14 PCH_GPIO29
+RTCVCC
DSWODVREN R185 1 2 330K_0402_5%
R187 1 @ 2 330K_0402_5%
DSWODVREN - On Die DSW VR Enable
* H : Enable
L : Disable
+3V_PCH
WAKE# R192 1 2 10K_0402_5%
PCH_GPIO29 R195 1 @ 2 10K_0402_5%
+3VS
PM_CLKRUN# R196 1 2 8.2K_0402_5%
R199 1 @ 2 10K_0402_5%
EC team suggestion
South Bridge side must have
pull-low 10K on this pin(GPIO32)
Use CLKRUN# Requires a 8.2- k weak
pull-up resistor to Vcc3_3S
Can be left NC when
IAMT is not support on
the platfrom


+3VS
R204 1 @ 2 200_0402_5% PM_DRAM_PWRGD
+3V_PCH
R305 1 @ 2 200_0402_5% PM_DRAM_PWRGD
R205 1 2 10K_0402_5% SUSWARN#
R206 1 2 200K_0402_5% AC_PRESENT_R
R207 1 2 10K_0402_5% PCH_GPIO72
R208 1 2 10K_0402_5% RI#
R210 1 2 10K_0402_5% PCH_RSMRST#_R



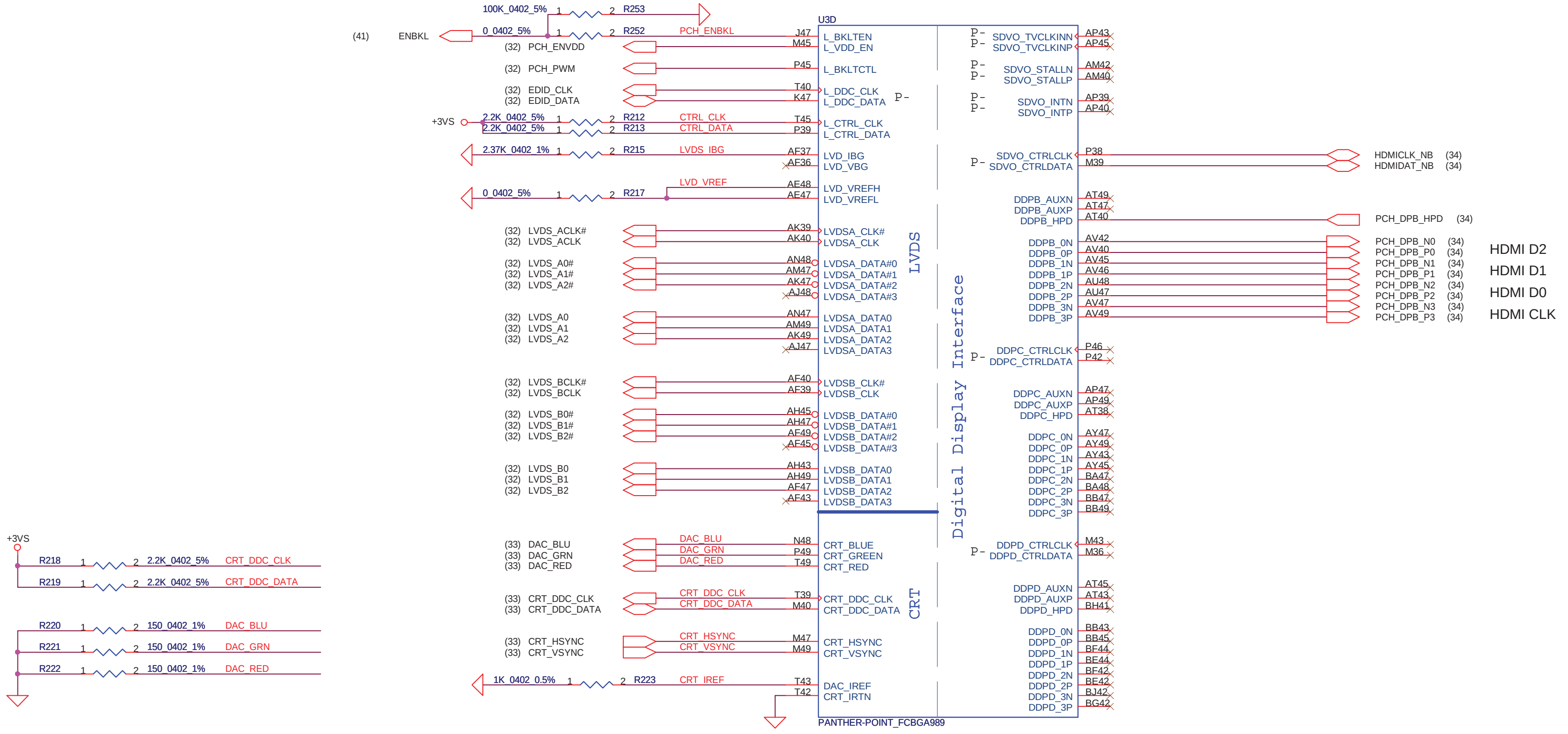
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
PCH (3/8) DMI,FDI,PM,

Size Custom
Document Number
LA-8131P
Rev 0.6

Date: Friday, January 06, 2012 Sheet 15 of 58



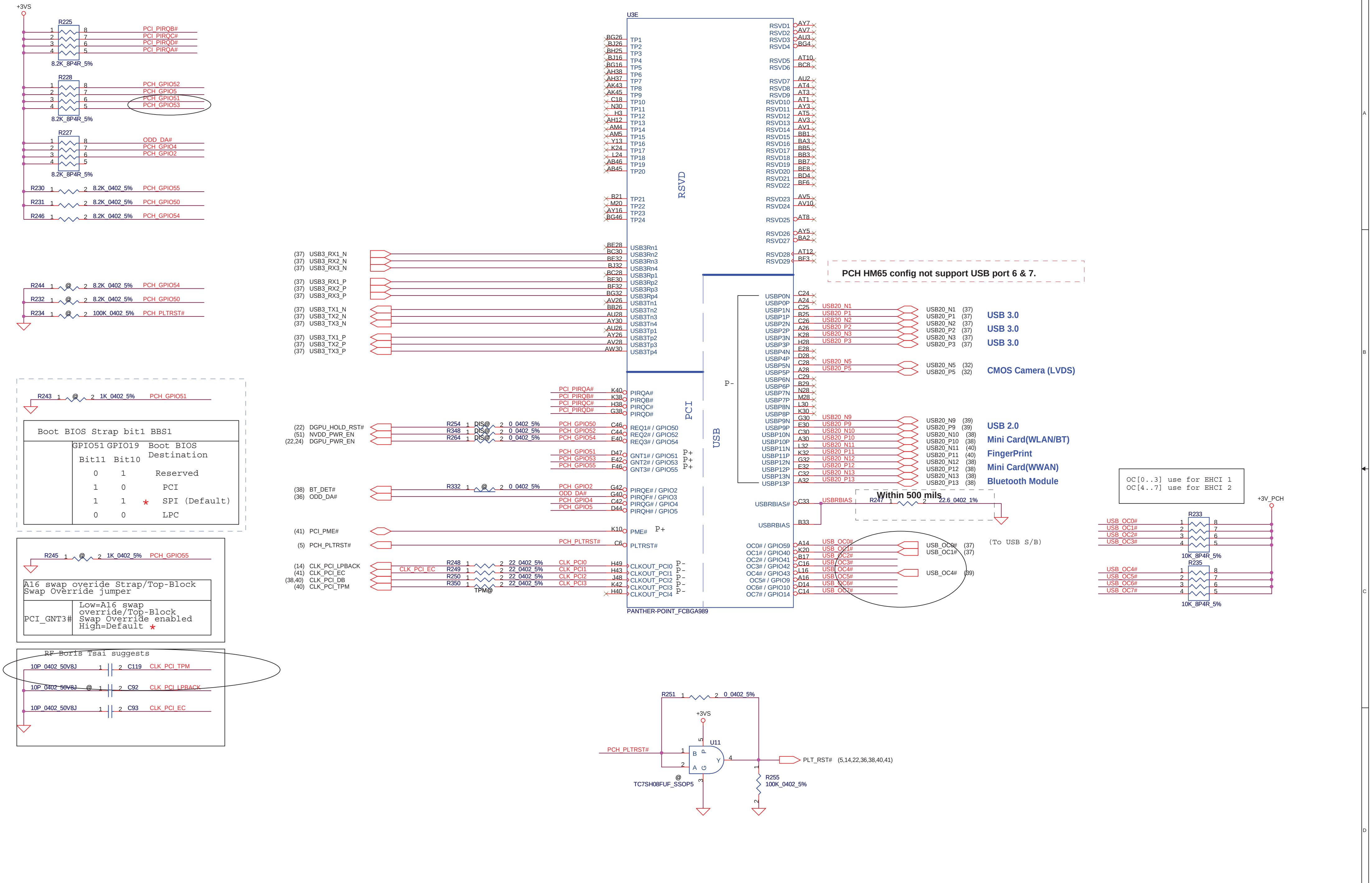
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
PCH (4/9) LVDS,CRT,DP,HDMI

Size
Custom
Document Number
LA-8131P
Rev
0.6

Date: Friday, January 06, 2012
Sheet 16 of 58



Boot BIOS Strap bit1 BBS1				
	GPIO51 Bit11	GPIO19 Bit10		Boot BIOS Destination
	0	1		Reserved
	1	0		PCI
	1	1	*	SPI (Default)
	0	0		LPC

A16 swap overide Strap/Top-Block Swap Override jumper	

PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled
	High=Default *

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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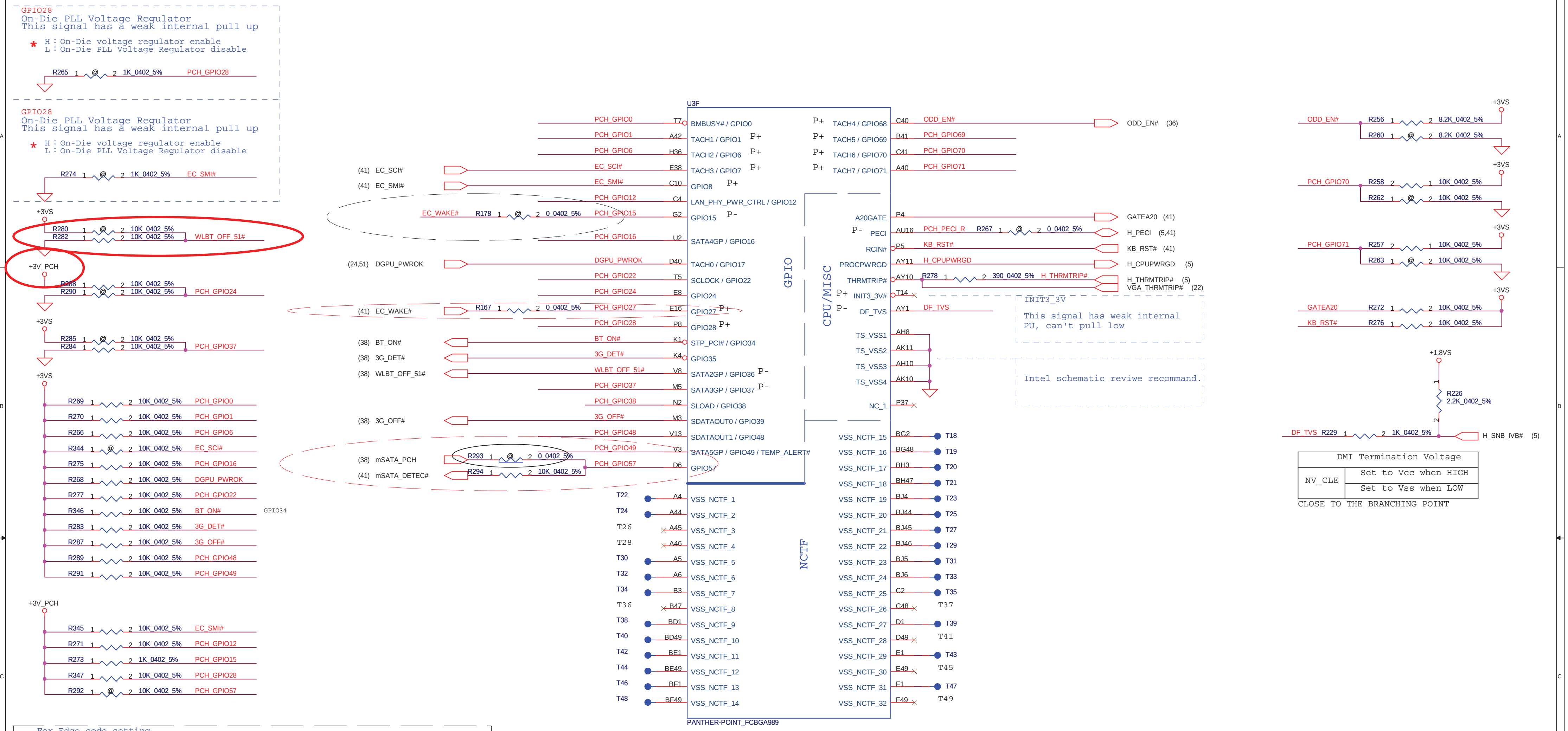
Compal Electronics, Inc.

Title
PCH (5/9) PCI, USB, NVRAM

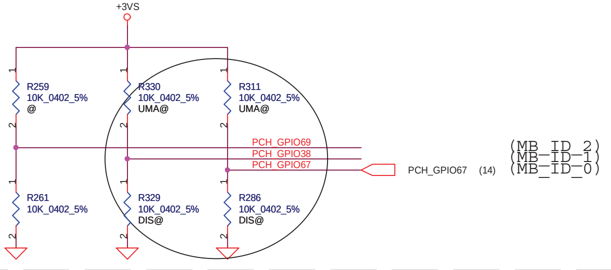
Size Custom
Document Number **LA-8131P**
Rev 0.6

Date: Tuesday, January 10, 2012
Sheet 17 of 58


GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R265 1 @ 2 1K_0402_5% PCH_GPIO28
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R274 1 @ 2 1K_0402_5% EC_SMI#
+3VS
R280 1 @ 2 10K_0402_5%
R282 1 2 10K_0402_5% WLBT_OFF_51#
+3V_PCH
R288 1 2 10K_0402_5%
R290 1 @ 2 10K_0402_5% PCH_GPIO24
+3VS
R285 1 @ 2 10K_0402_5%
R284 1 2 10K_0402_5% PCH_GPIO37
+3VS
R269 10K_0402_5% PCH_GPIO0
R270 10K_0402_5% PCH_GPIO1
R266 10K_0402_5% PCH_GPIO6
R344 @ 10K_0402_5% EC_SCI#
R275 10K_0402_5% PCH_GPIO16
R268 10K_0402_5% DGPU_PWROK
R277 10K_0402_5% PCH_GPIO22
R346 10K_0402_5% BT_ON# GPIO34
R283 10K_0402_5% 3G_DET#
R287 10K_0402_5% 3G_OFF#
R289 10K_0402_5% PCH_GPIO48
R291 10K_0402_5% PCH_GPIO49
+3V_PCH
R345 10K_0402_5% EC_SMI#
R271 10K_0402_5% PCH_GPIO12
R273 1K_0402_5% PCH_GPIO15
R347 10K_0402_5% PCH_GPIO28
R292 @ 10K_0402_5% PCH_GPIO57
(41) EC_SCI#
(41) EC_SMI#
EC_WAKE# R178 1 @ 2 0_0402_5%
(24,51) DGPU_PWROK
(41) EC_WAKE# R167 1 2 0_0402_5%
(38) BT_ON#
(38) 3G_DET#
(38) WLBT_OFF_51#
(38) 3G_OFF#
(38) mSATA_PCH R293 1 @ 2 0_0402_5%
(41) mSATA_DETEC# R294 1 2 10K_0402_5%
U3F
PCH_GPIO0 T7 BMBUSY# / GPIO0
PCH_GPIO1 A42 TACH1 / GPIO1
PCH_GPIO6 H36 TACH2 / GPIO6
EC_SCI# E38 TACH3 / GPIO7
EC_SMI# C10 GPIO8
PCH_GPIO12 C4 LAN_PHY_PWR_CTRL / GPIO12
PCH_GPIO15 G2 GPIO15
PCH_GPIO16 U2 SATA4GP / GPIO16
DGPU_PWROK D40 TACH0 / GPIO17
PCH_GPIO22 T5 SCLOCK / GPIO22
PCH_GPIO24 E8 GPIO24
PCH_GPIO27 E16 GPIO27
PCH_GPIO28 P8 GPIO28
BT_ON# K1 STP_PCI# / GPIO34
3G_DET# K4 GPIO35
WLBT_OFF_51# V8 SATA2GP / GPIO36
PCH_GPIO37 M5 SATA3GP / GPIO37
PCH_GPIO38 N2 SLOAD / GPIO38
3G_OFF# M3 SDATAOUT0 / GPIO39
PCH_GPIO48 V13 SDATAOUT1 / GPIO48
PCH_GPIO49 V3 SATA5GP / GPIO49 / TEMP_ALERT#
PCH_GPIO57 D6 GPIO57
P+ P-
GPIO
CPU/MISC
NCTF
TACH4 / GPIO68 C40 ODD_EN#
TACH5 / GPIO69 B41 PCH_GPIO69
TACH6 / GPIO70 C41 PCH_GPIO70
TACH7 / GPIO71 A40 PCH_GPIO71
A20GATE P4 GATEA20 (41)
PECI AU16 PCH_PECI_R R267 1 @ 2 0_0402_5% H_PECI (5,41)
RCIN# P5 KB_RST# KB_RST# (41)
PROCPWRGD AY11 H_CPUPWRGD H_CPUPWRGD (5)
THRMTRIP# AY10 R278 1 2 390_0402_5% H_THRMTRIP# H_THRMTRIP# (5) VGA_THRMTRIP# (22)
INIT3_3V# T14
DF_TVS AY1 DF_TVS
TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37
ODD_EN# (36)
INIT3_3V
This signal has weak internal PU, can't pull low
Intel schematic reviwe recommand.
T22 A4 VSS_NCTF_1
T24 A44 VSS_NCTF_2
T26 A45 VSS_NCTF_3
T28 A46 VSS_NCTF_4
T30 A5 VSS_NCTF_5
T32 A6 VSS_NCTF_6
T34 B3 VSS_NCTF_7
T36 B47 VSS_NCTF_8
T38 BD1 VSS_NCTF_9
T40 BD49 VSS_NCTF_10
T42 BE1 VSS_NCTF_11
T44 BE49 VSS_NCTF_12
T46 BF1 VSS_NCTF_13
T48 BF49 VSS_NCTF_14
VSS_NCTF_15 BG2 T18
VSS_NCTF_16 BG48 T19
VSS_NCTF_17 BH3 T20
VSS_NCTF_18 BH47 T21
VSS_NCTF_19 BJ4 T23
VSS_NCTF_20 BJ44 T25
VSS_NCTF_21 BJ45 T27
VSS_NCTF_22 BJ46 T29
VSS_NCTF_23 BJ5 T31
VSS_NCTF_24 BJ6 T33
VSS_NCTF_25 C2 T35
VSS_NCTF_26 C48 T37
VSS_NCTF_27 D1 T39
VSS_NCTF_28 D49 T41
VSS_NCTF_29 E1 T43
VSS_NCTF_30 E49 T45
VSS_NCTF_31 F1 T47
VSS_NCTF_32 F49 T49
PANTHER-POINT_FCBGA989
+3VS
ODD_EN# R256 1 2 8.2K_0402_5%
R260 1 @ 2 8.2K_0402_5%
+3VS
PCH_GPIO70 R258 2 1 10K_0402_5%
R262 1 @ 2 10K_0402_5%
+3VS
PCH_GPIO71 R257 2 1 10K_0402_5%
R263 1 @ 2 10K_0402_5%
+3VS
GATEA20 R272 1 2 10K_0402_5%
KB_RST# R276 1 2 10K_0402_5%
+1.8VS
R226 2.2K_0402_5%
DF_TVS R229 1 2 1K_0402_5% H_SNB_IVB# (5)
DMI Termination Voltage
NV_CLE Set to Vcc when HIGH
Set to Vss when LOW
CLOSE TO THE BRANCHING POINT

For Edge code setting

PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA



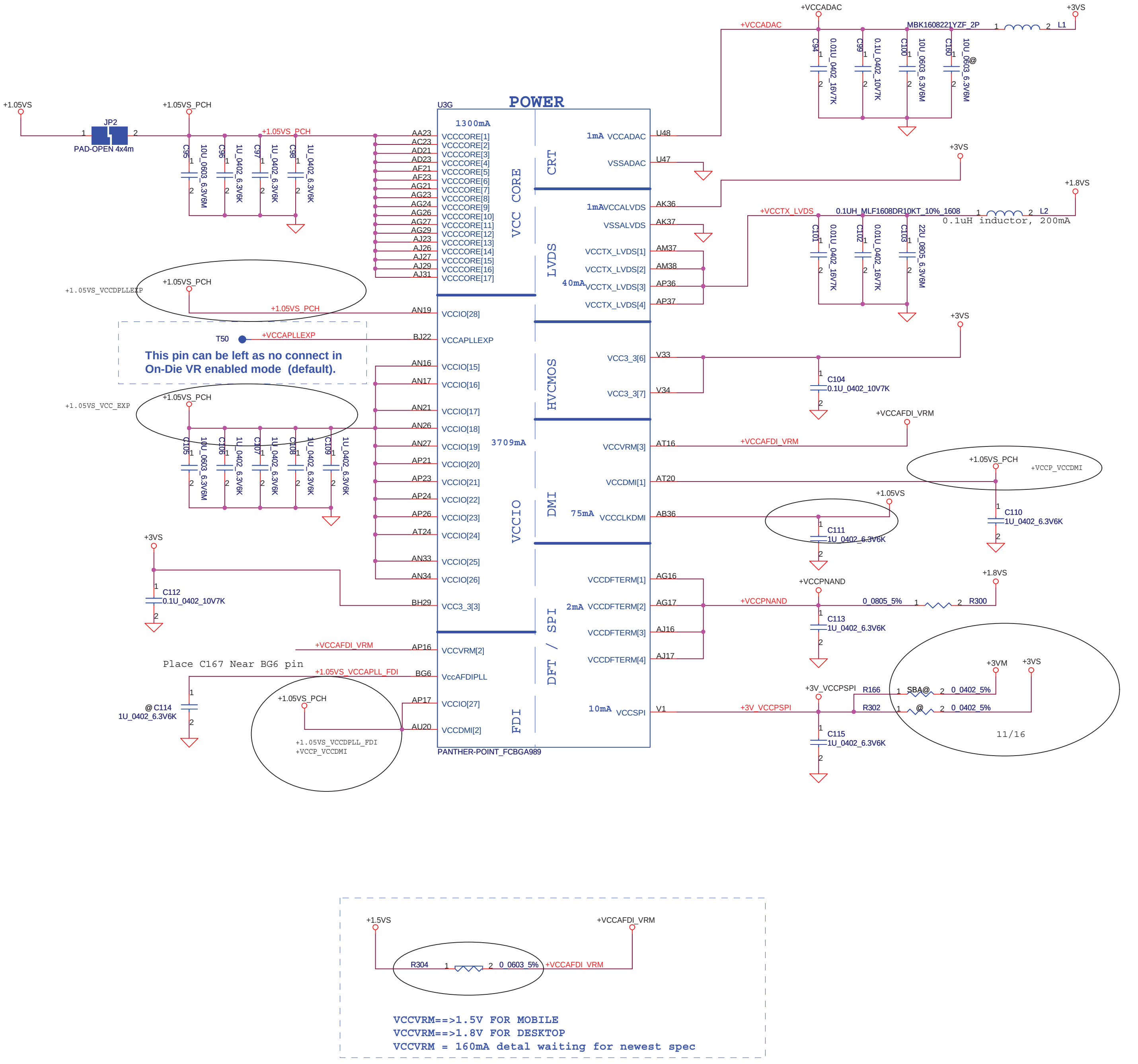
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
PCH (6/9) GPIO, CPU, MISC

Size Custom
Document Number
LA-8131P
Rev 0.6

Date: Tuesday, January 10, 2012



This pin can be left as no connect in On-Die VR enabled mode (default).

Place C167 Near BG6 pin

VCCVRM==>1.5V FOR MOBILE
VCCVRM==>1.8V FOR DESKTOP
VCCVRM = 160mA detal waiting for newest spec

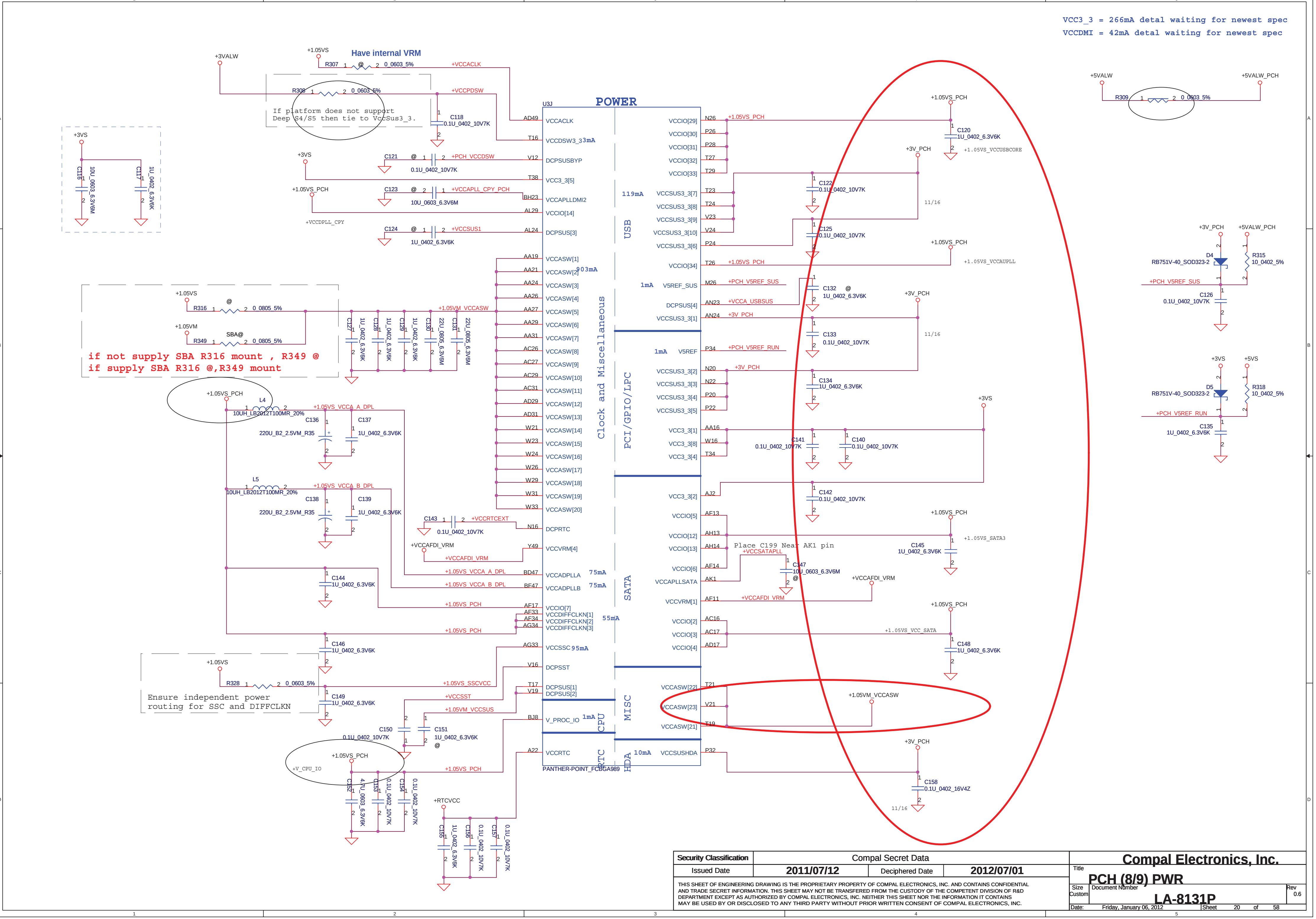
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
PCH (7/9) PWR

Size Custom
Document Number **LA-8131P**
Rev 0.6

Date: Tuesday, January 10, 2012 Sheet 19 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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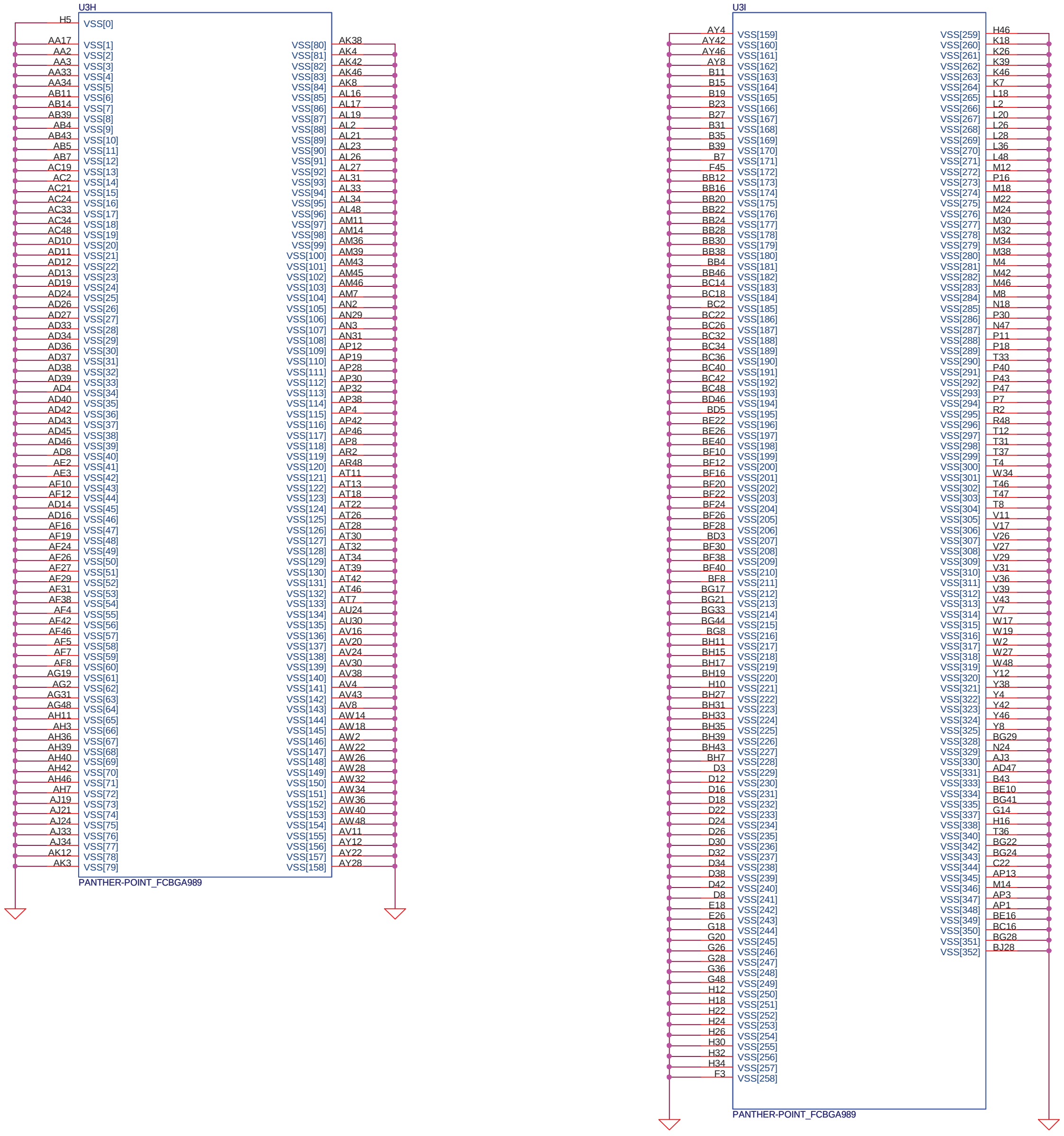
Compal Electronics, Inc.

Title
PCH (8/9) PWR

Size Custom
Document Number LA-8131P
Rev 0.6

Date: Friday, January 06, 2012
Sheet 20 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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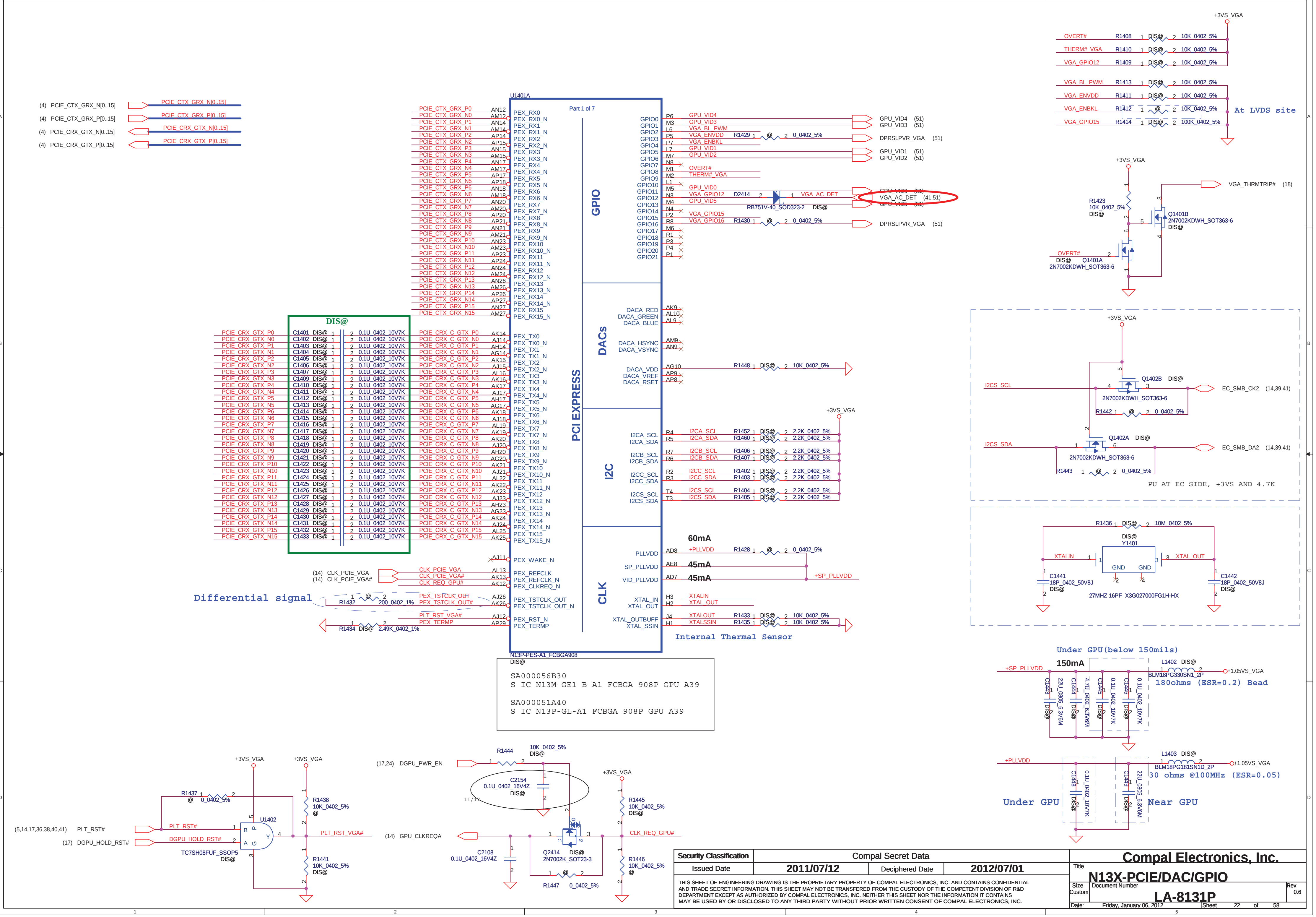
Compal Electronics, Inc.

Title
PCH (9/9) VSS

Size: Custom
Document Number: **LA-8131P**
Rev: 0.6

Date: Friday, January 06, 2012
Sheet 21 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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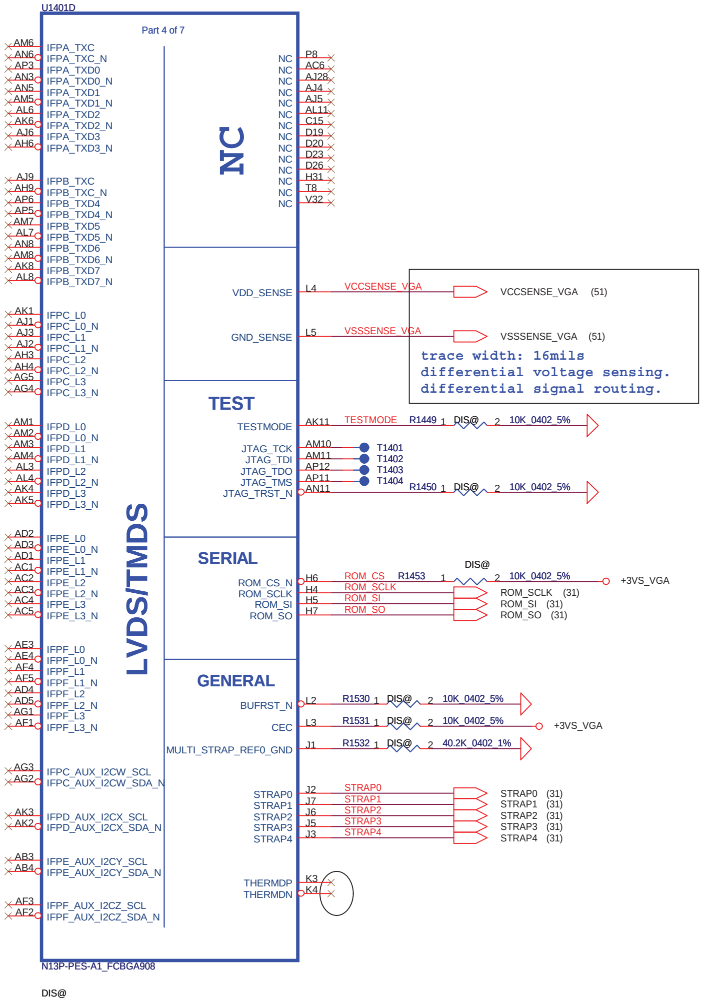
Compal Electronics, Inc.

Title
N13X-PCIE/DAC/GPIO

Size Custom
Document Number **LA-8131P**
Rev 0.6

Date: Friday, January 06, 2012 Sheet 22 of 58



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title N13X-LVDS/HDMI/DP/THM

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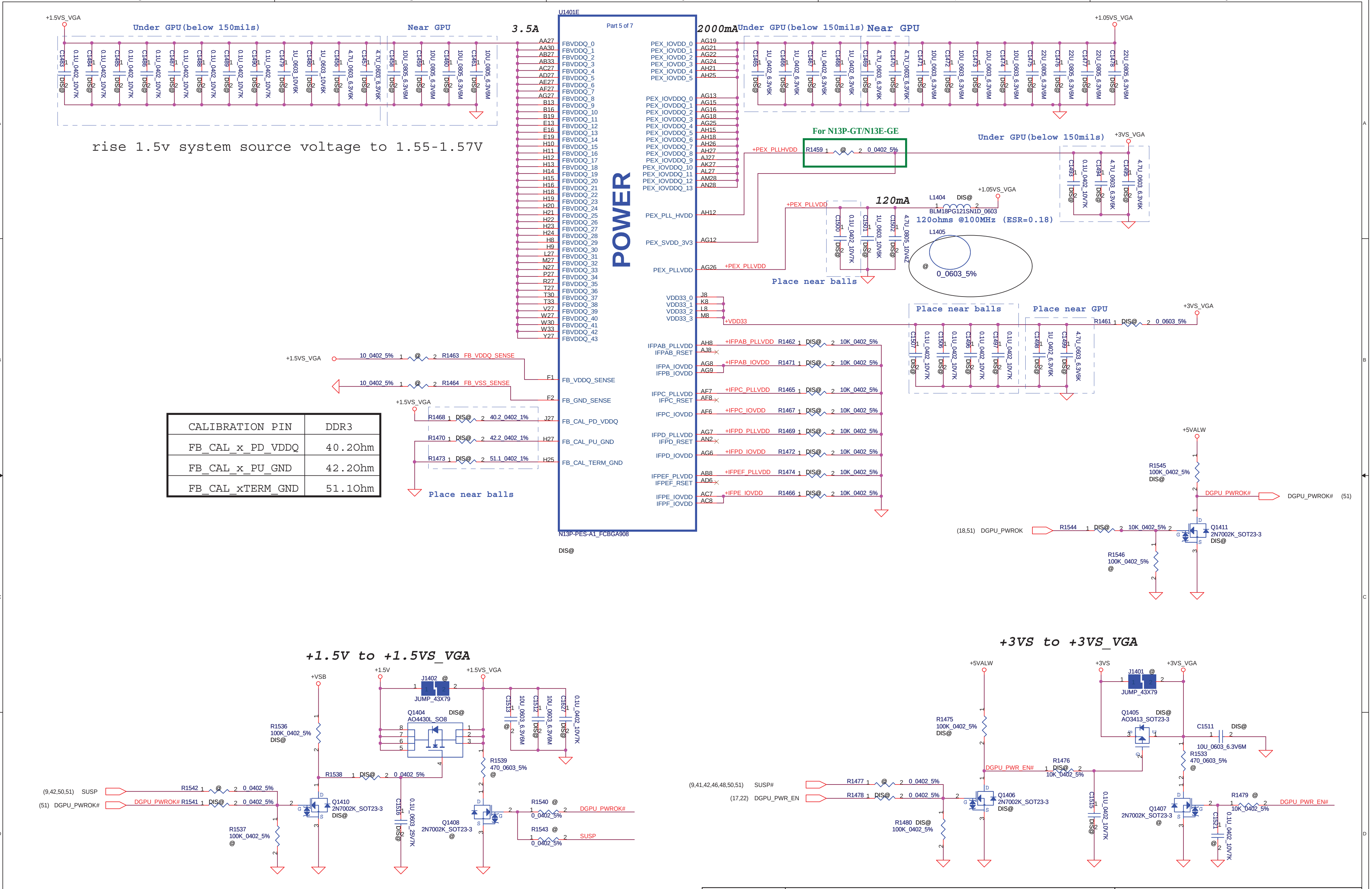
Size	Document Number	Rev
Custom	LA-8131P	0.6

Date: Friday, January 06, 2012 | Sheet 23 of 58



CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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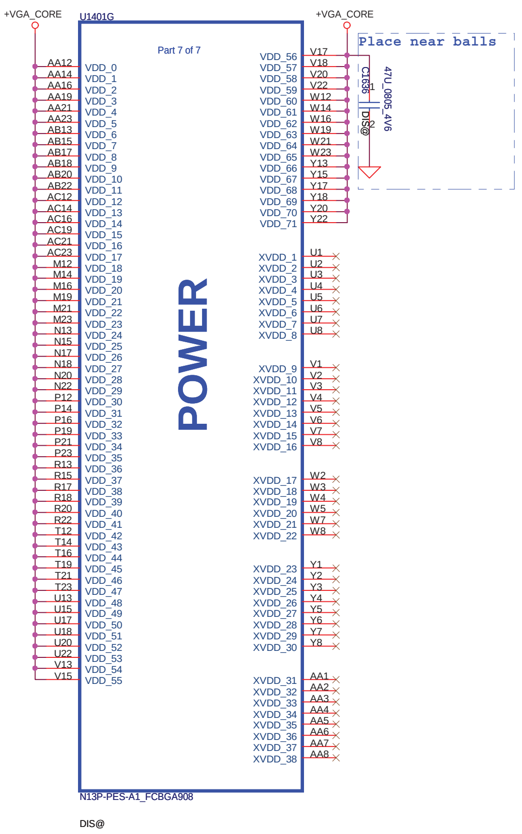
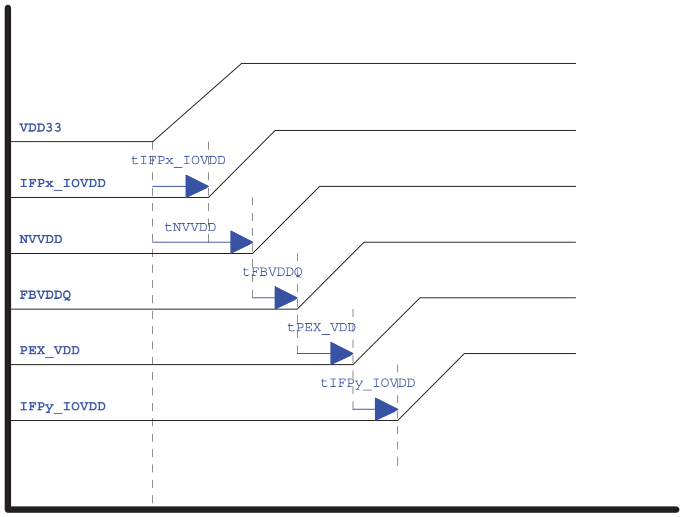
Compal Electronics, Inc.

Title
N13X-POWER

Size: Custom
Document Number: LA-8131P
Rev: 0.6

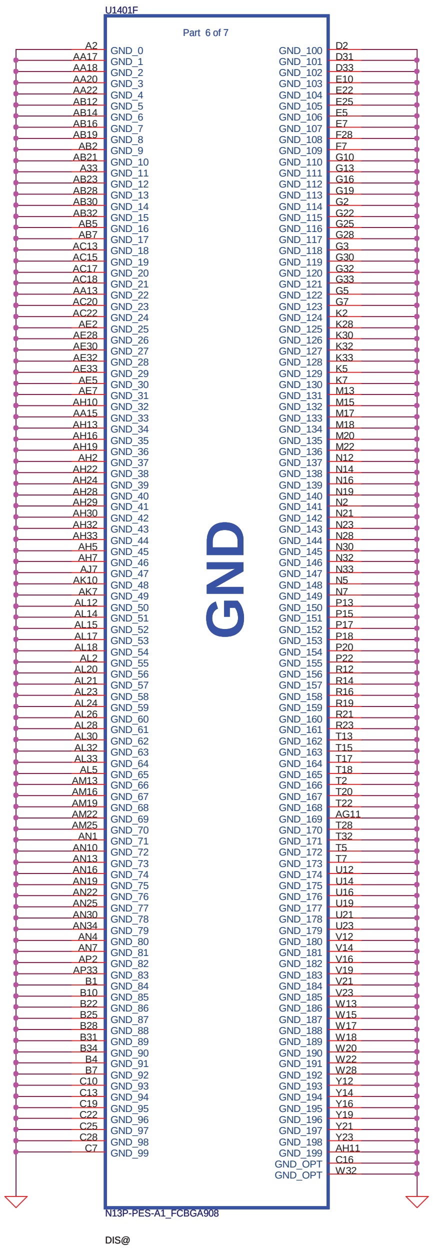
Date: Friday, January 06, 2012
Sheet 24 of 58





NV Recommended Power On Sequencing Order

X=A and B
Y=C,D,E and F



Security Classification	Compal Secret Data		
Issued Date	**2011/07/12**	Deciphered Date	**2012/07/01**

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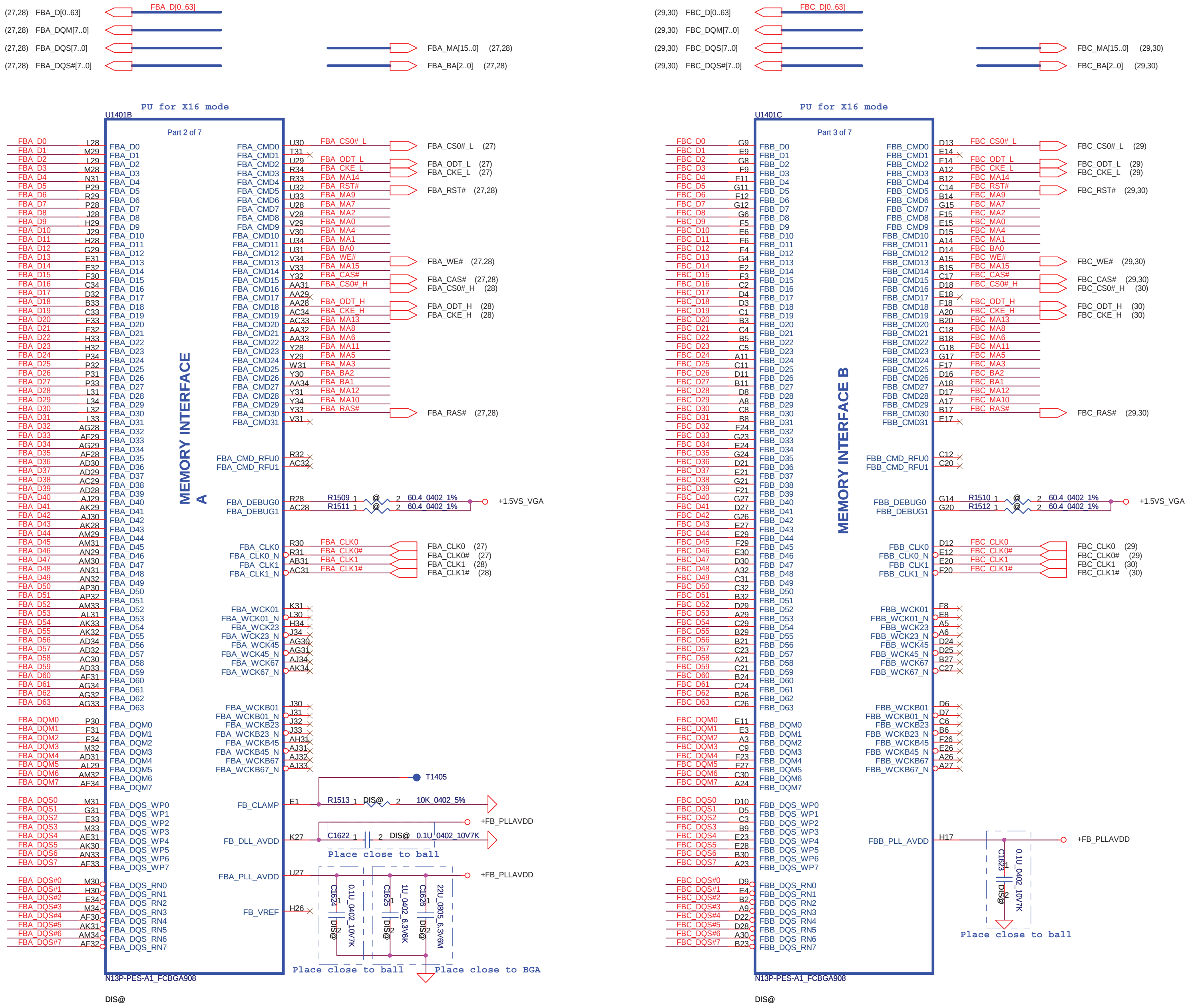
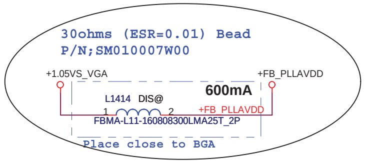
Compal Electronics, Inc.

Title
N13X-VGA CORE, GND

Size	Document Number	Rev
Custom	**LA-8131P**	0.6

Date: Friday, January 06, 2012 Sheet 25 of 58





Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

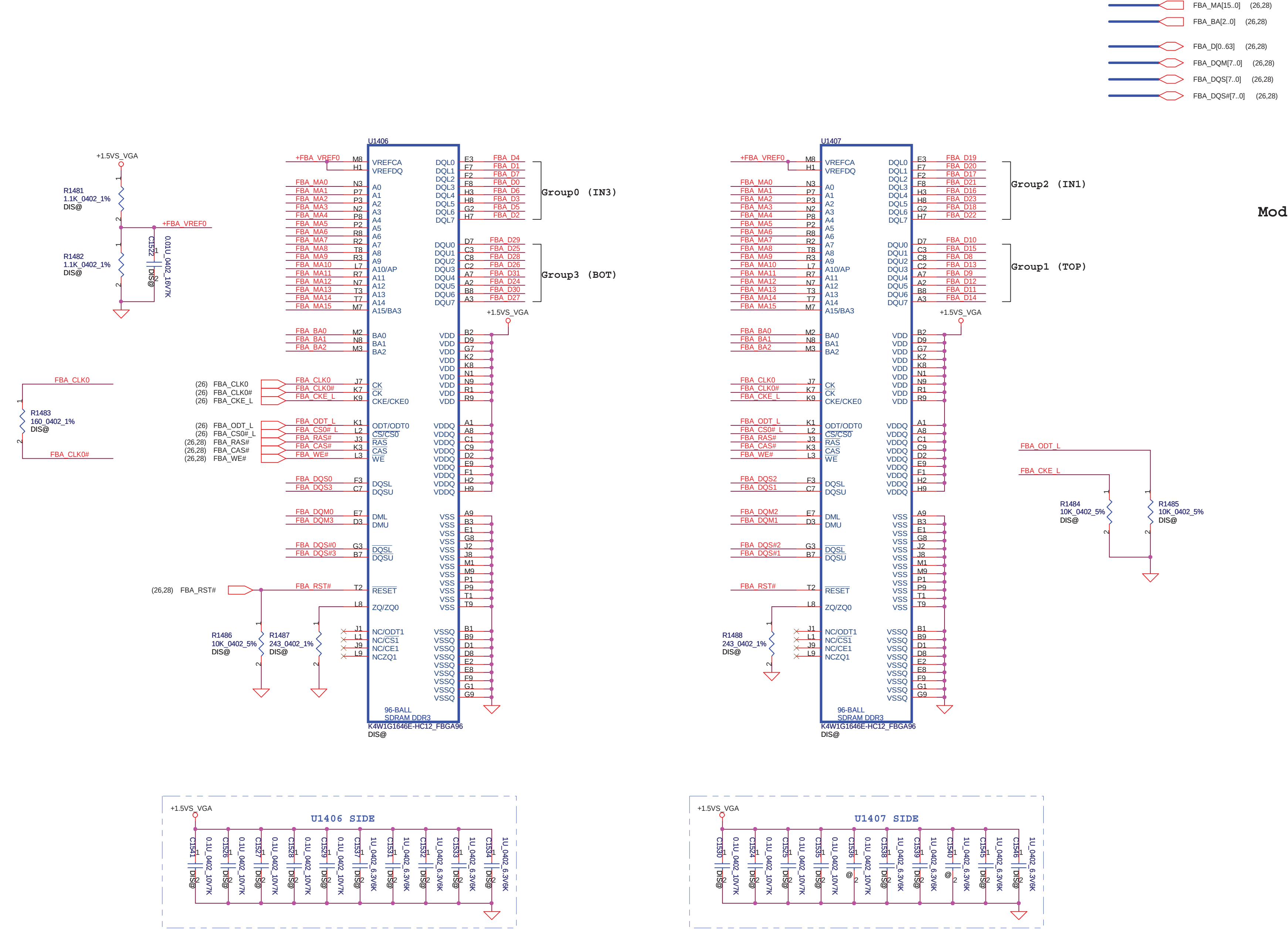
Compal Electronics, Inc.

Title
N13X-MEM Interface

Size: Custom
Document Number: LA-8131P
Rev: 0.6

Date: Friday, January 06, 2012
Sheet 26 of 58

Memory Partition A - Lower 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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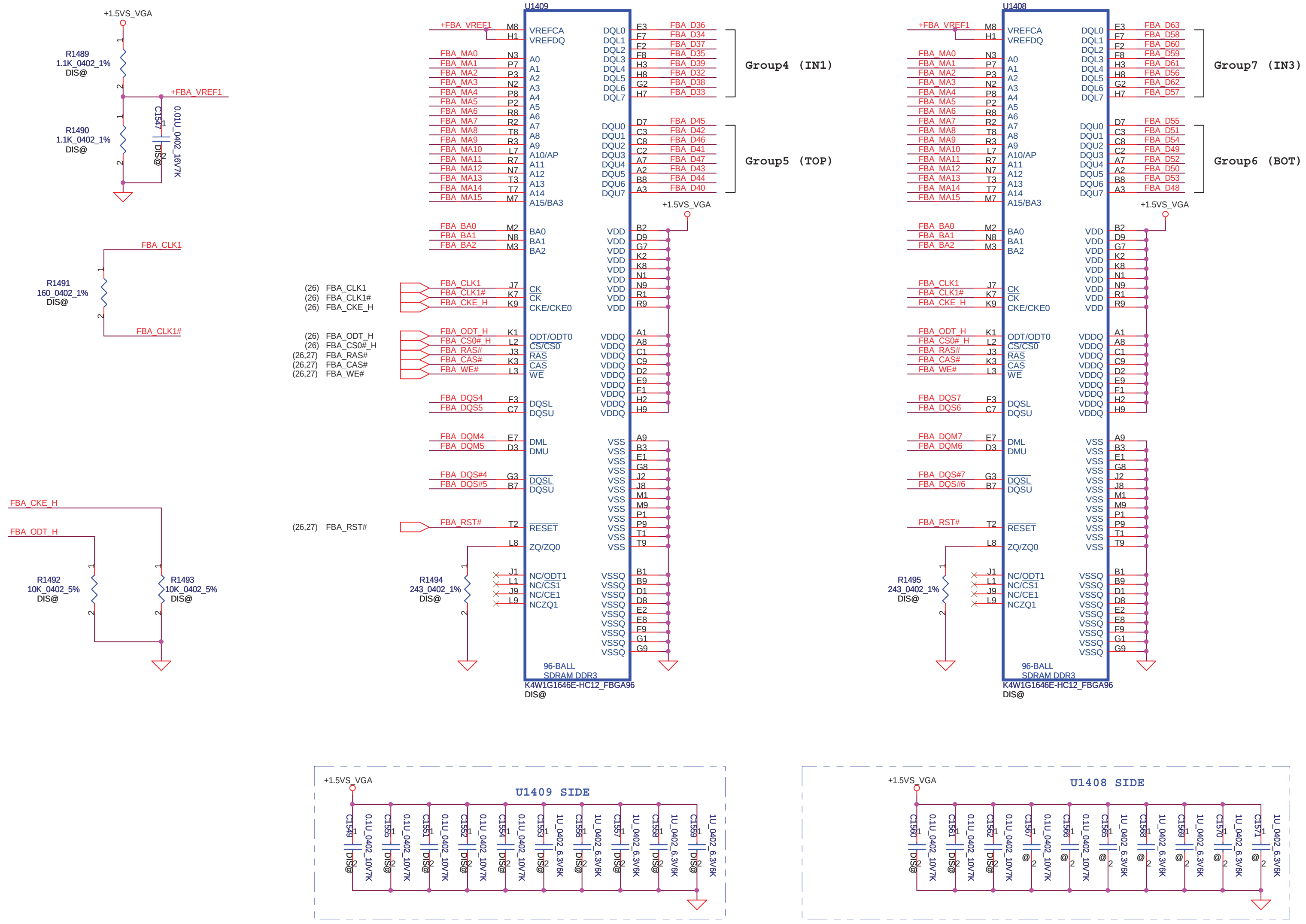
Compal Electronics, Inc.

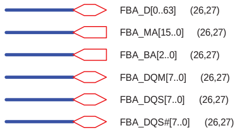
Title
N13X-VRAM A Lower

Size Custom | Document Number **LA-8131P** | Rev 0.6

Date: Friday, January 06, 2012 | Sheet 27 of 58

Memory Partition A - Upper 32 bits





Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
N13X-VRAM A Upper

Size Custom
Document Number LA-8131P
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Date: Friday, January 06, 2012
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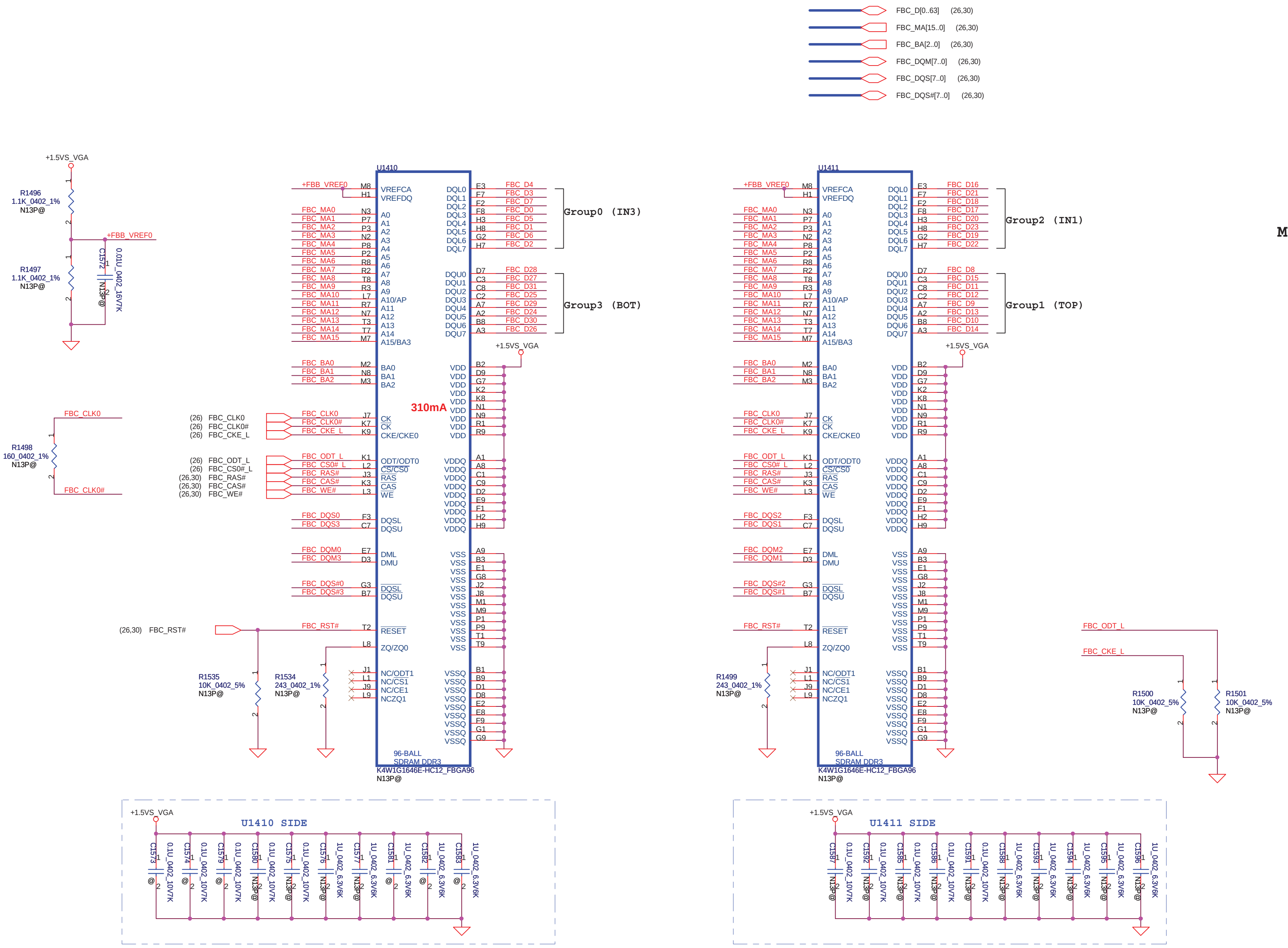
Memory Partition C - Lower 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

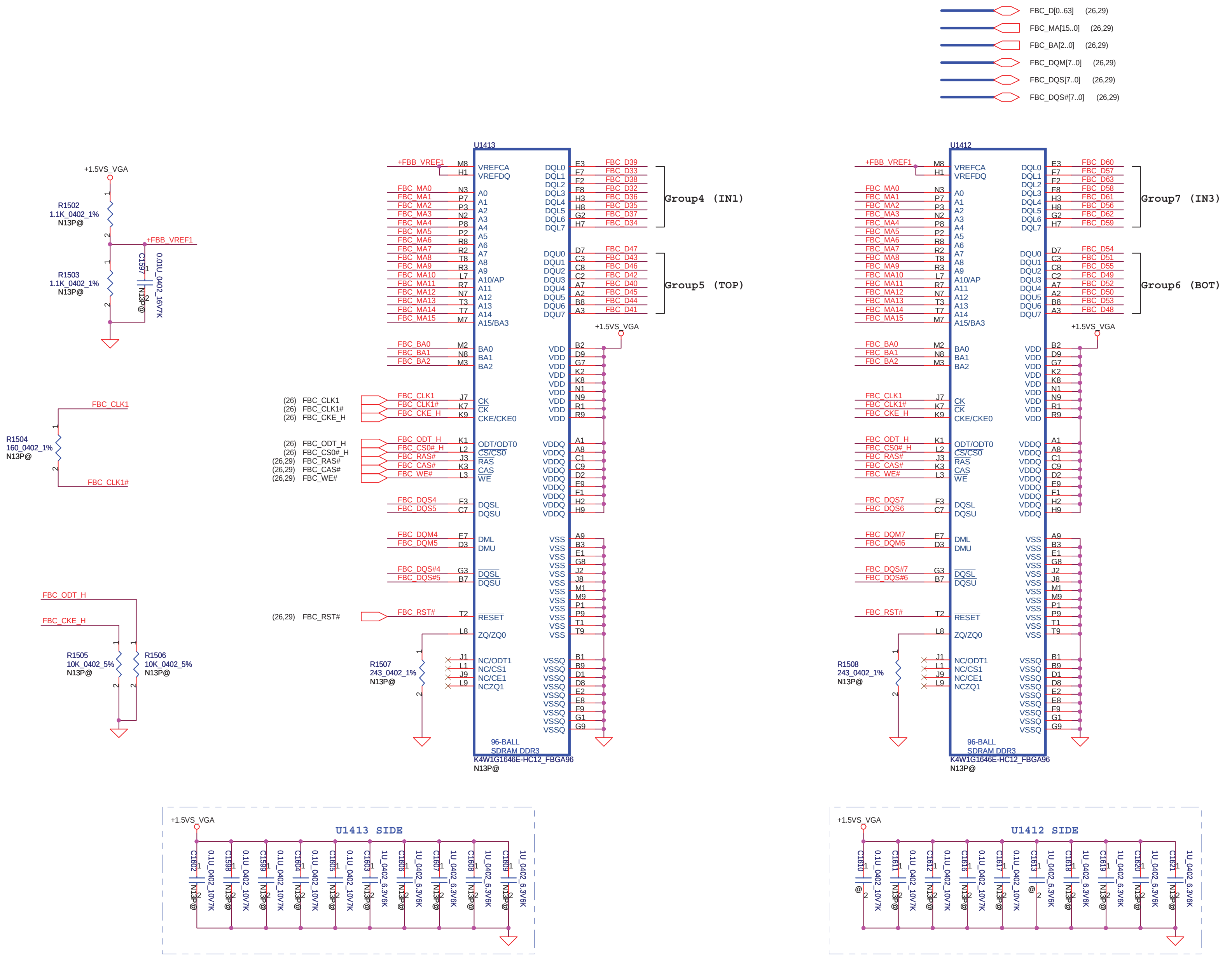
Compal Electronics, Inc.

Title
N13X-VRAM C Lower

Size Custom
Document Number LA-8131P
Rev 0.6

Date: Friday, January 06, 2012
Sheet 29 of 58

Memory Partition C - Upper 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
N13X-VRAM C Upper

Size Custom
Document Number LA-8131P
Rev 0.6

Date: Friday, January 06, 2012
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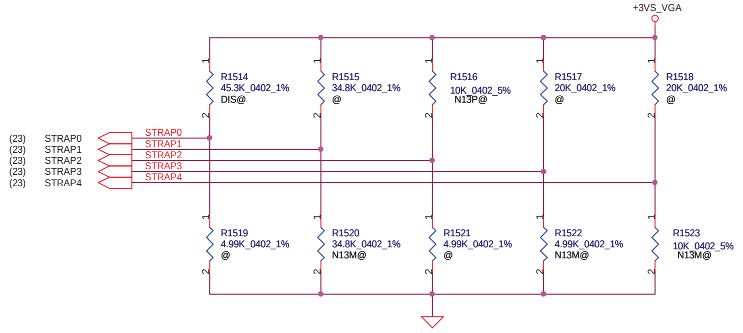

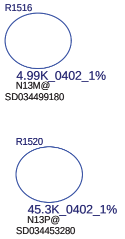

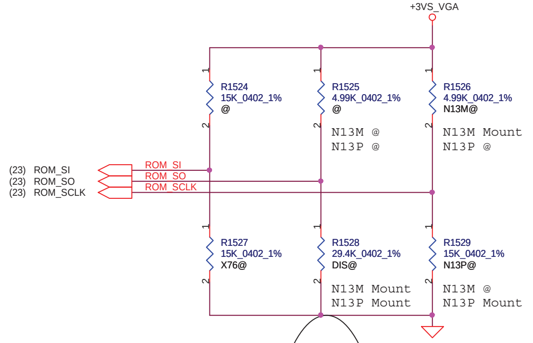

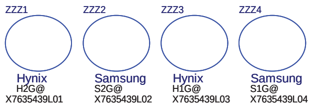

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GL	Samsung 900MHz	K4W1G1646G-BC11 64Mx16	PD 10K	PD 15K	PD 20K	PU 45K	PD 45K	PU 10K PU 45K(ES)	NC	NC
	Hynix 900MHz	H5TQ1G63DFR-11C 64Mx16	PD 10K	PD 15K	PD 15K	PU 45K	PD 45K	PU 10K PU 45K(ES)	NC	NC
	Samsung 900MHz	K4W2G1646C-HC11 128Mx16	PD 10K	PD 15K	PD 45K	PU 45K	PD 45K	PU 10K PU 45K(ES)	NC	NC
	Hynix 900MHz	H5TQ2G63BFR-11C 128Mx16	PD 10K	PD 15K	PD 35K	PU 45K	PD 45K	PU 10K PU 45K(ES)	NC	NC

X76

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1	Samsung 900MHz	K4W1G1646G-BC11 64Mx16	PD 30K	PU 5K	PD 20K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	Hynix 900MHz	H5TQ1G63DFR-11C 64Mx16	PD 30K	PU 5K	PD 15K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	Samsung 900MHz	K4W2G1646C-HC11 128Mx16	PD 30K	PU 5K	PD 45K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	Hynix 900MHz	H5TQ2G63BFR-11C 128Mx16	PD 30K	PU 5K	PD 35K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K

9/27
from 15K to 5K

X76

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
N13X-MISC

Size Custom
Document Number **LA-8131P**
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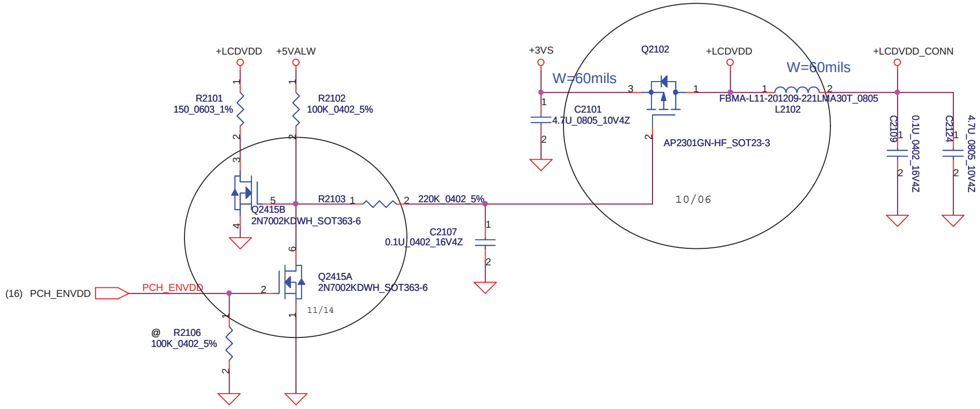
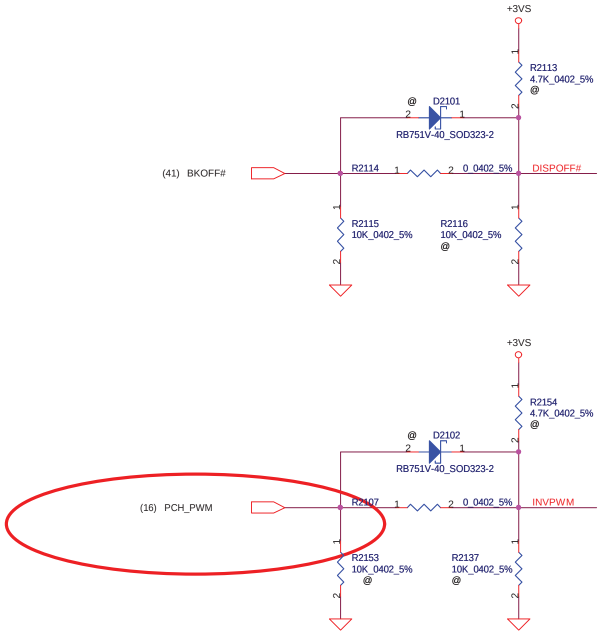
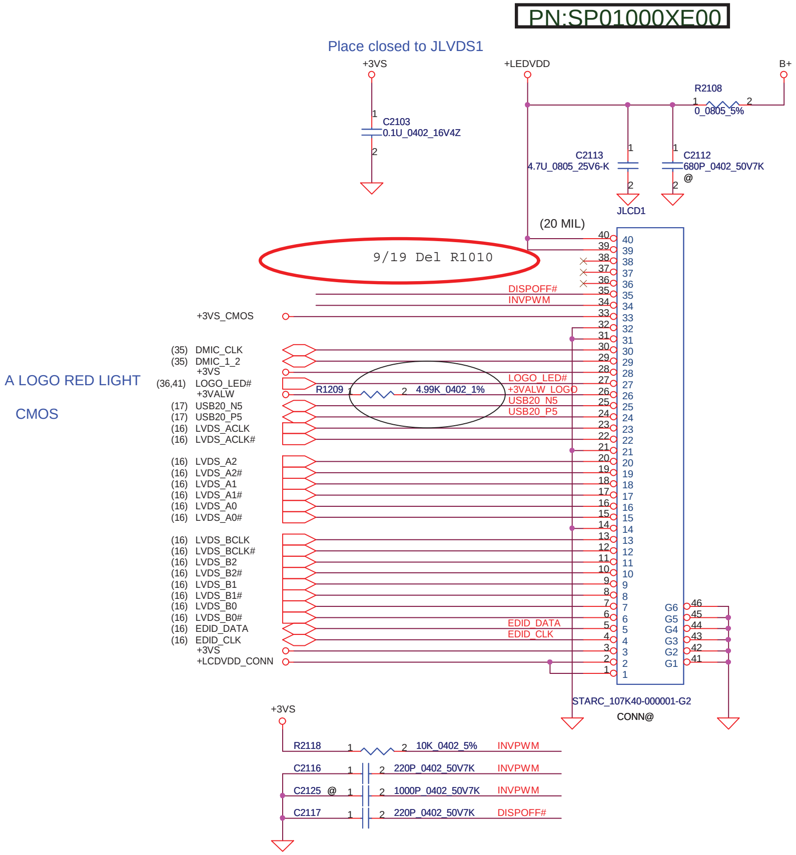
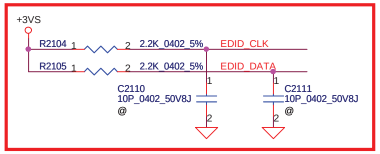
LCD POWER CIRCUIT



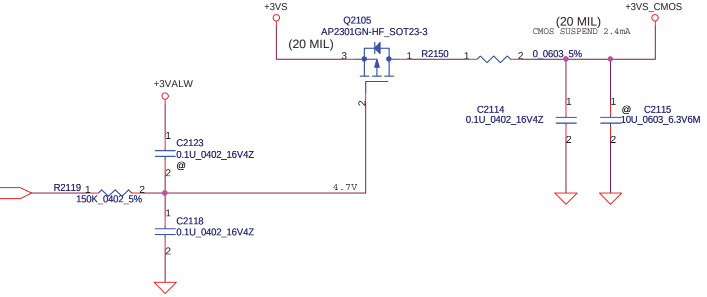


LCD/LED PANEL Conn.





CMOS Camera Conn



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title LVDS Connector
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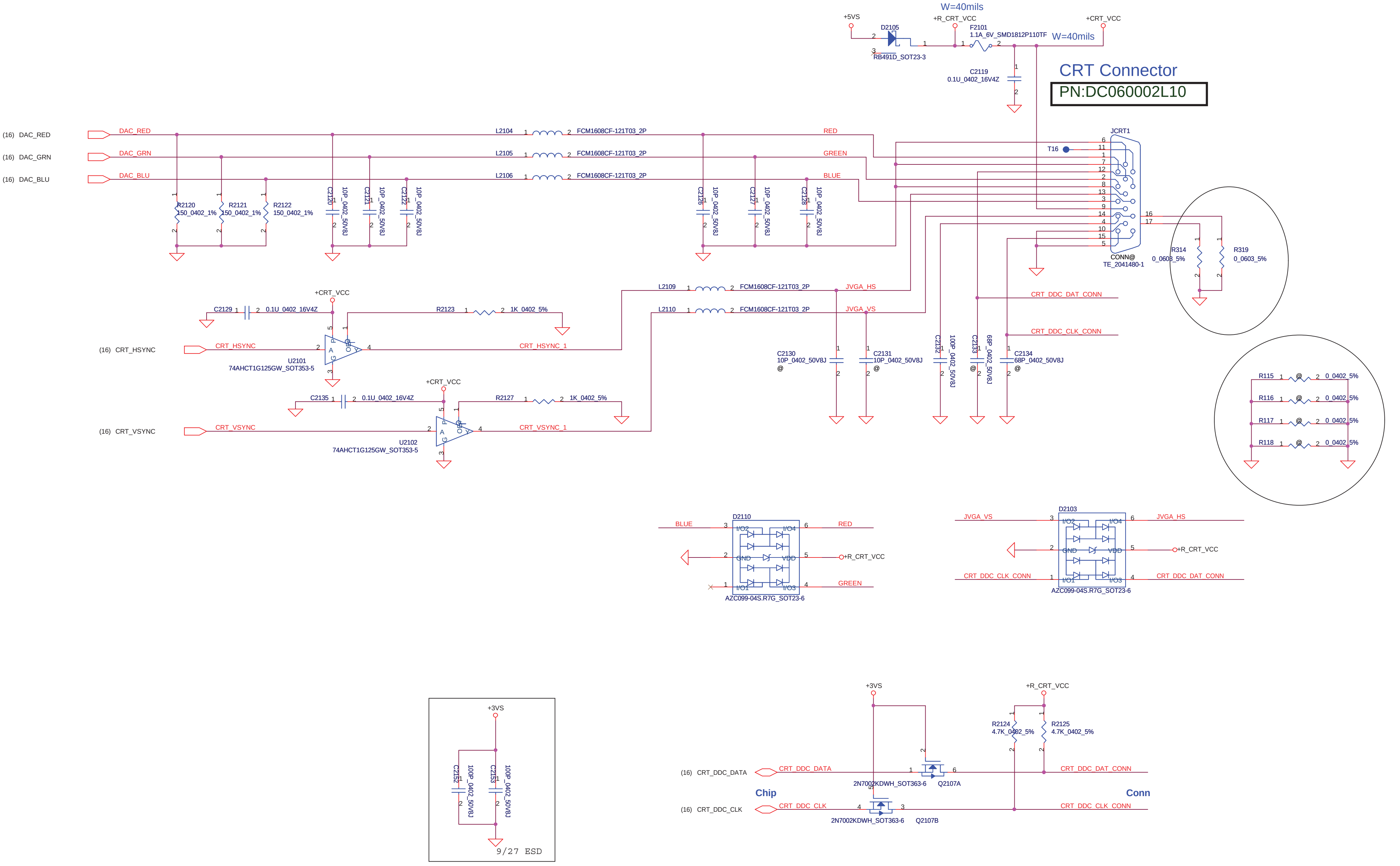


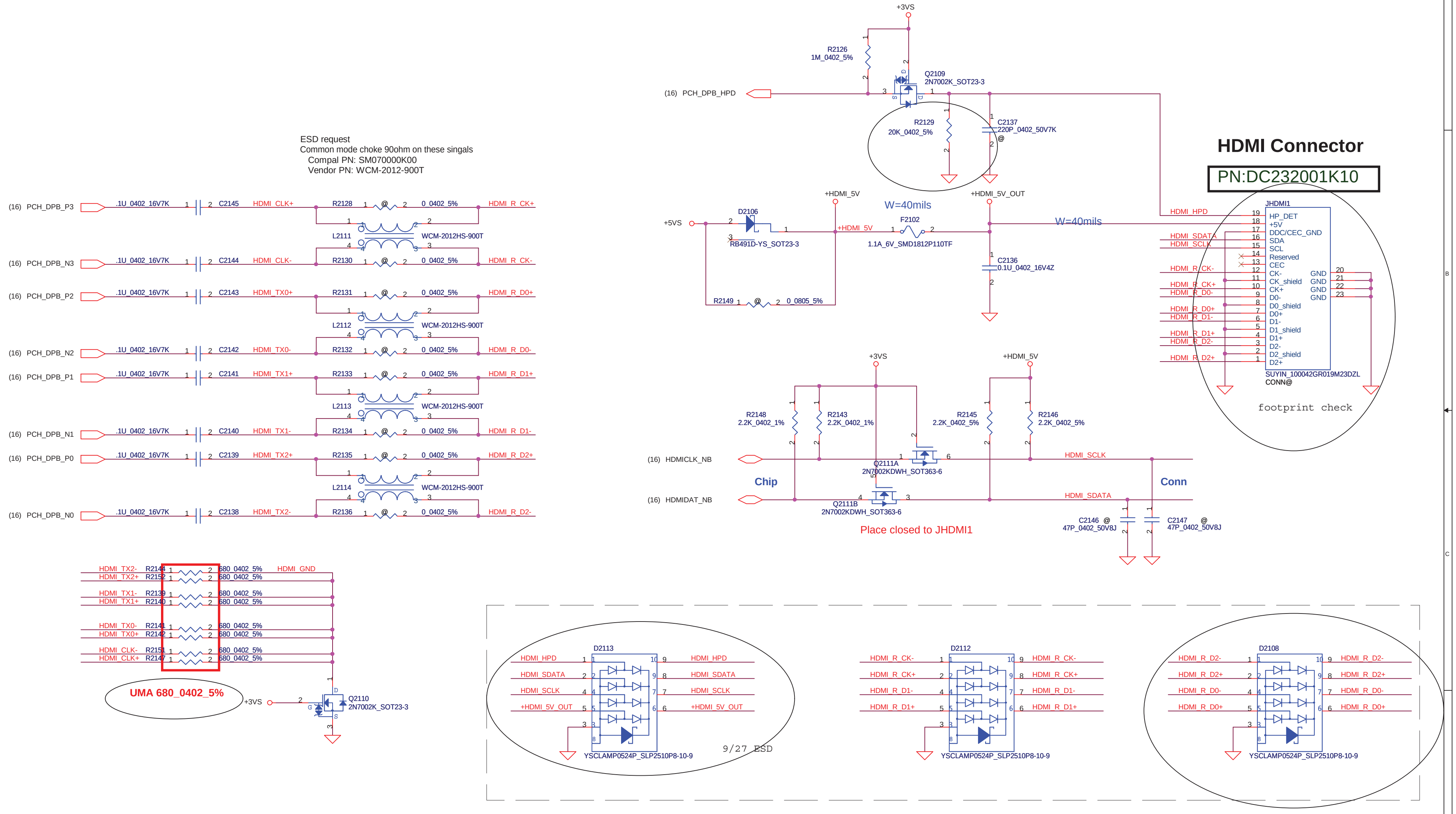
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
CRT Connector

Size Custom
Document Number **LA-8131P**
Rev 0.6

Date: Tuesday, January 10, 2012



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title
HDMI Connector

Size Custom
Document Number **LA-8131P**
Rev 0.6

Date: Tuesday, January 10, 2012 Sheet 34 of 58

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

Layout Note:Path from +5VS to Pin12,
Pin15 must be very low
resistance (<0.01 ohms)

To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 & VDD_IO pins must be powerd by a rail that is not removed unless AC power is removed.
*DSH page42 has more detail.

AVDD_3.3 pinis output of internal LDO. NOT connect to external supply.

10K only needed if supply to VAUX_3.3 is removed during system re-start.

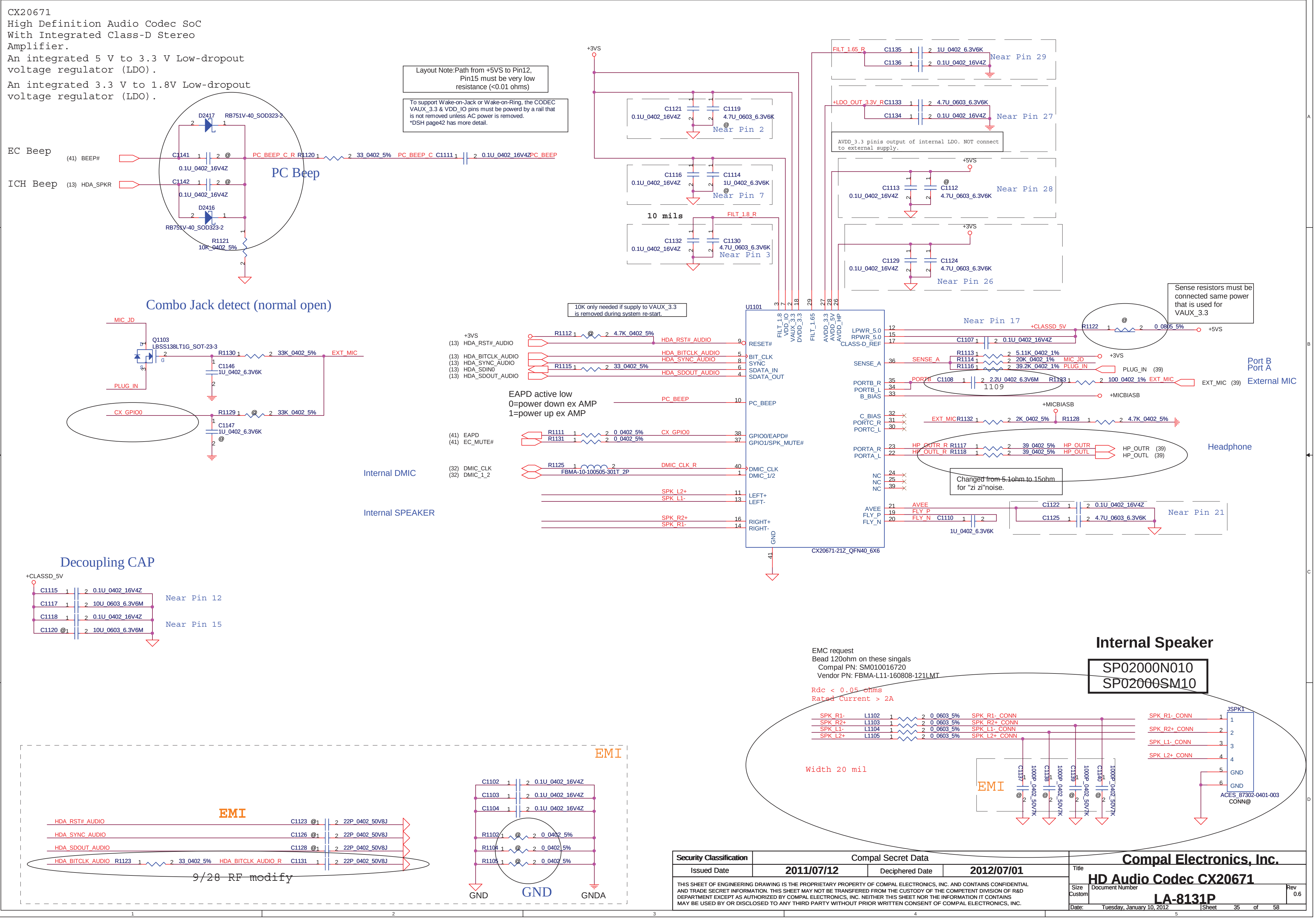
Sense resistors must be connected same power that is used for VAUX_3.3

EAPD active low
0=power down ex AMP
1=power up ex AMP

Changed from 5.1ohm to 15ohm for "zi zi"noise.

EMC request
Bead 120ohm on these singals
Compal PN: SM010016720
Vendor PN: FBMA-L11-160808-121LMT

Rdc < 0.05 ohms
Rated Current > 2A



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

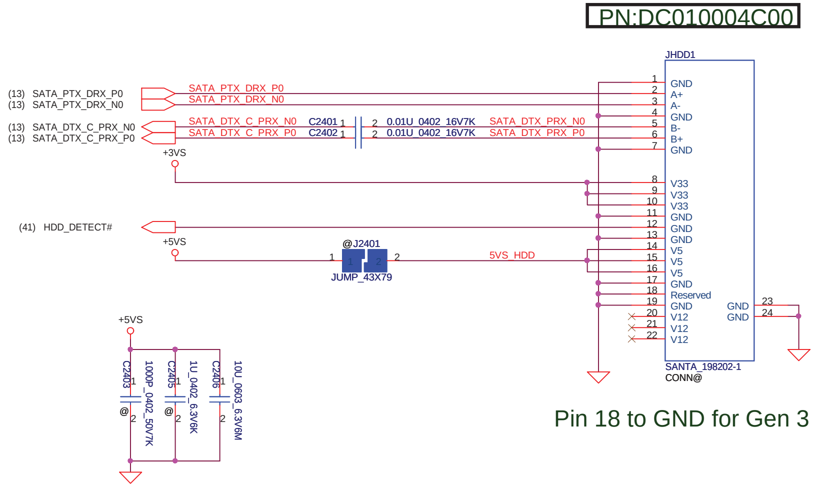
Compal Electronics, Inc.

Title
HD Audio Codec CX20671

Size Custom
Document Number **LA-8131P**
Rev 0.6

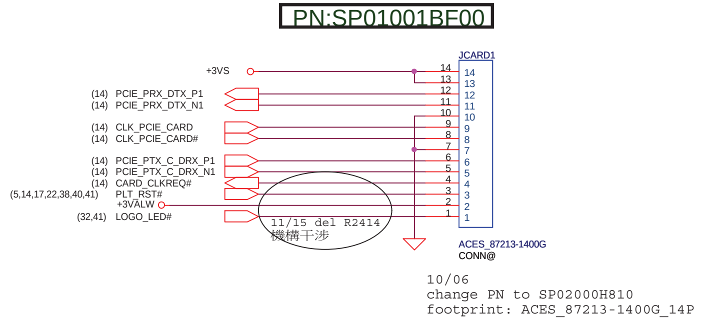
Date: Tuesday, January 10, 2012 Sheet 35 of 58

SATA HDD CONN.



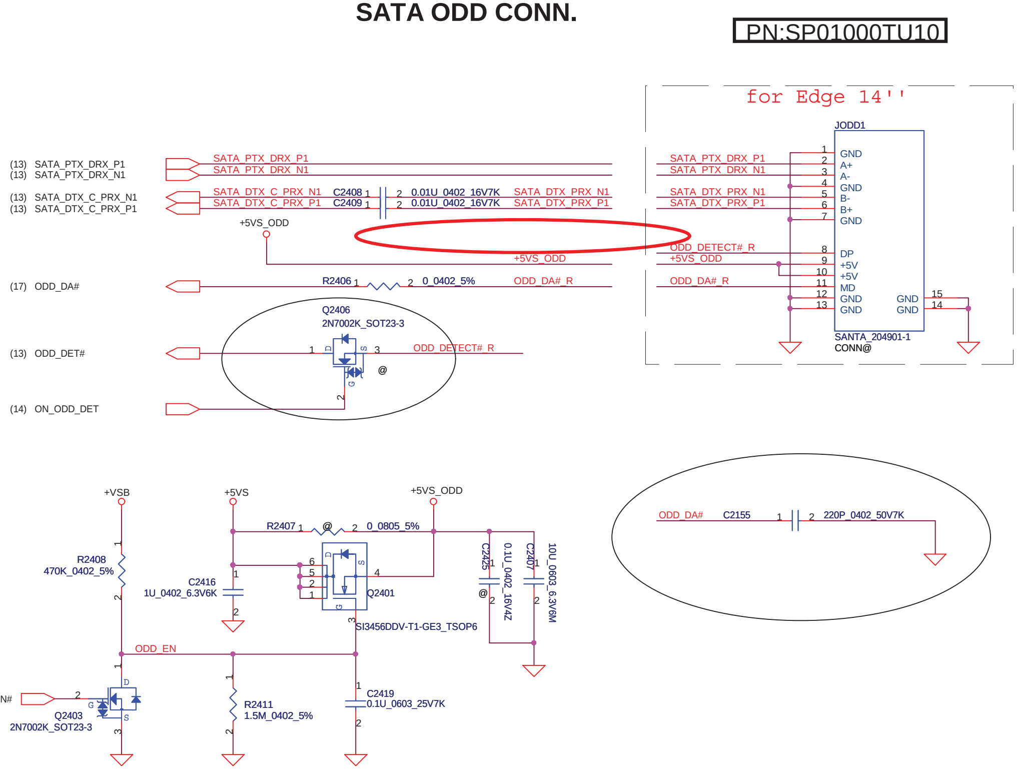
Pin 18 to GND for Gen 3

Card Reader CONN.

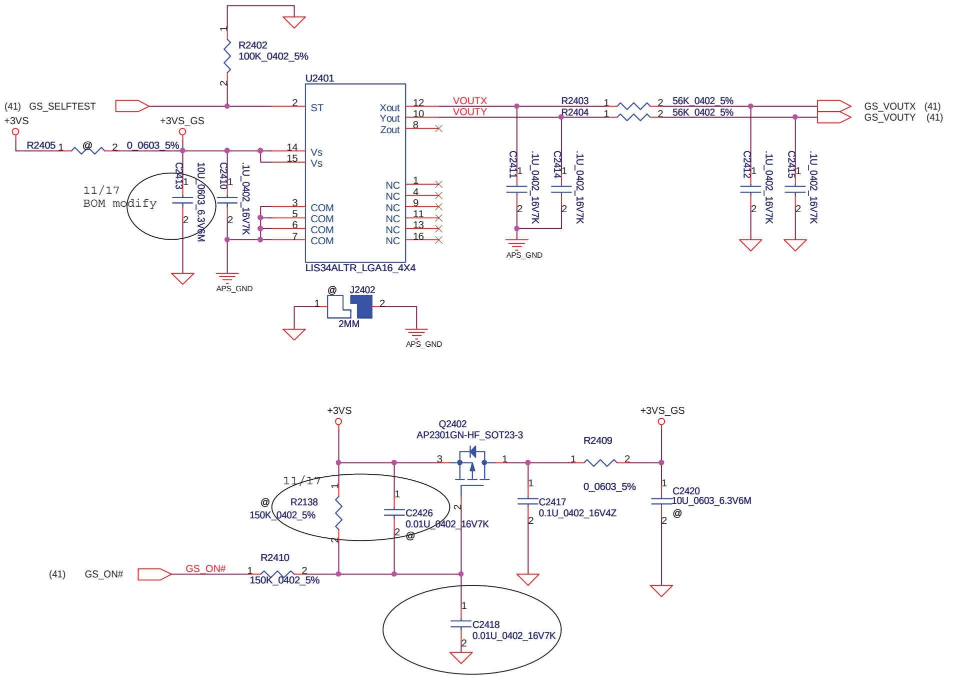


10/06
change PN to SP02000H810
footprint: ACES_87213-1400G_14P

SATA ODD CONN.



APS G-Sensor



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title
HDD/ODD/Card reader/G-Sensor

Size: Custom
Document Number: LA-8131P
Rev: 0.6

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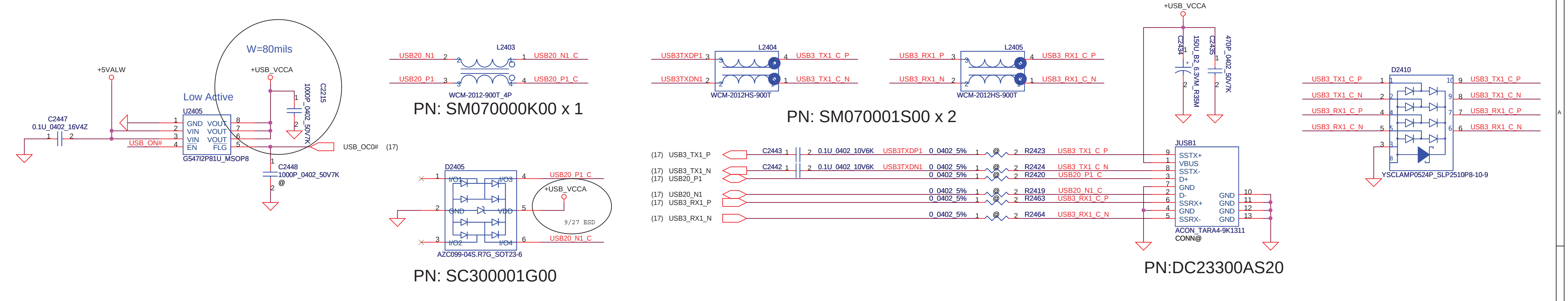
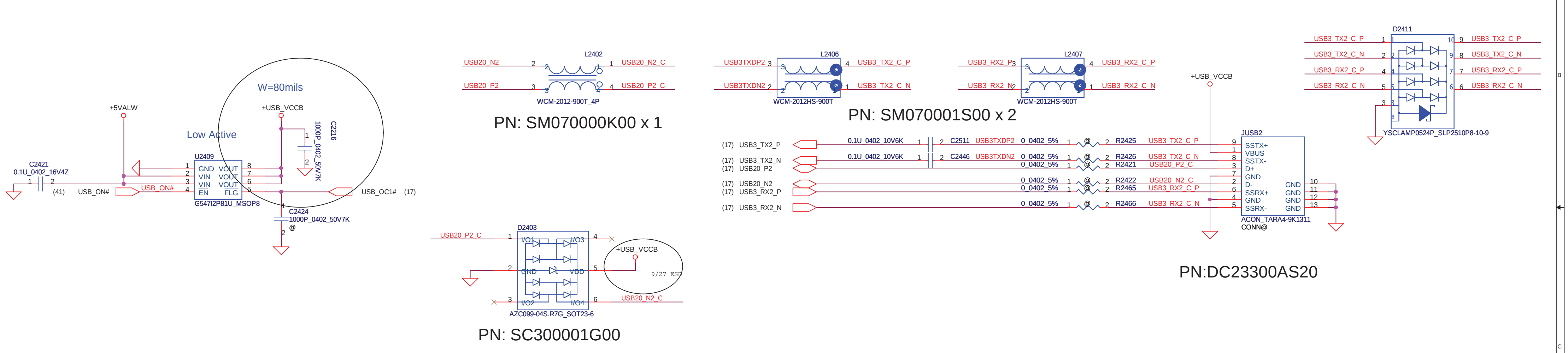
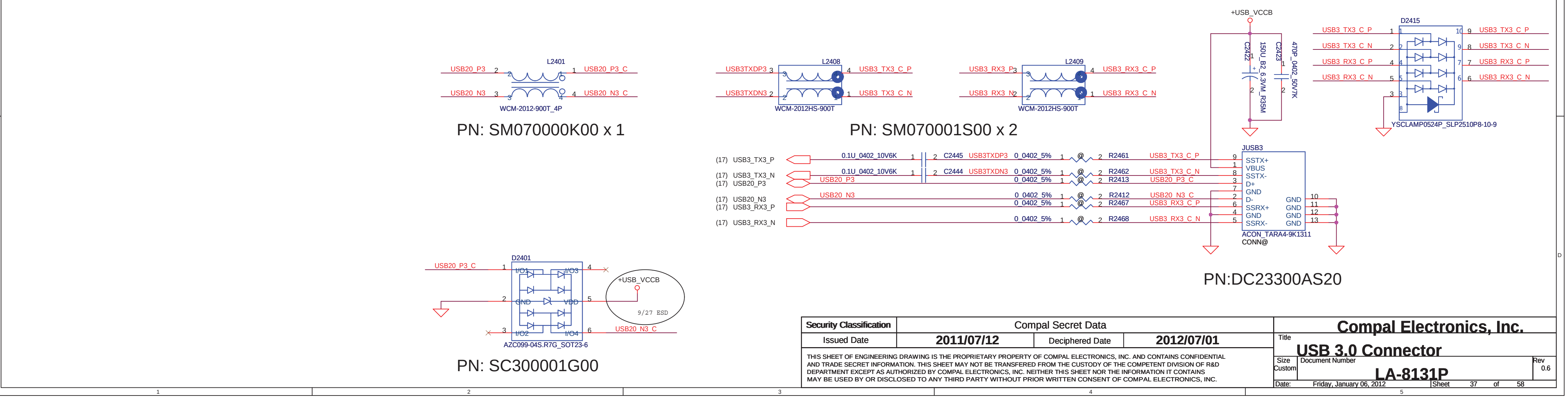
USB 3.0 Conn.







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Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title
USB 3.0 Connector

Size	Document Number	Rev
Custom	LA-8131P	0.6

Date: Friday, January 06, 2012 Sheet 37 of 58

Mini-Express Card for WLAN/WiMAX(Half)

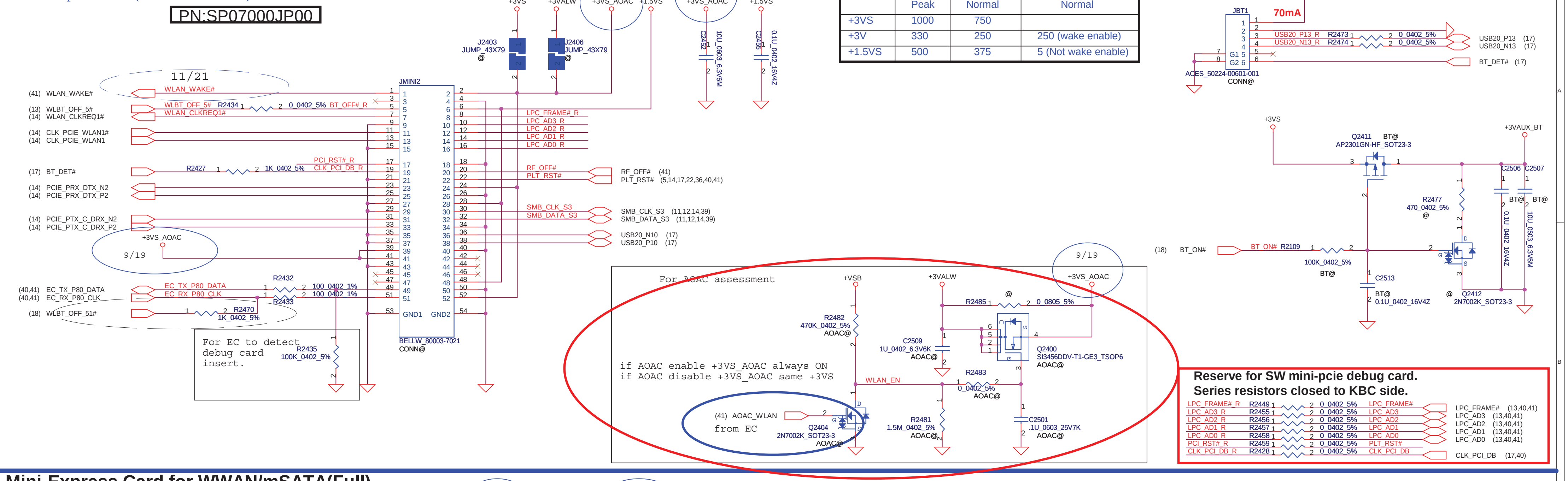
Mini-Express Card(WLAN/WiMAX)

PN:SP07000JP00

BT Connector

Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



For EC to detect debug card insert.

For AOAC assessment

if AOAC enable +3VS_AOAC always ON
if AOAC disable +3VS_AOAC same +3VS

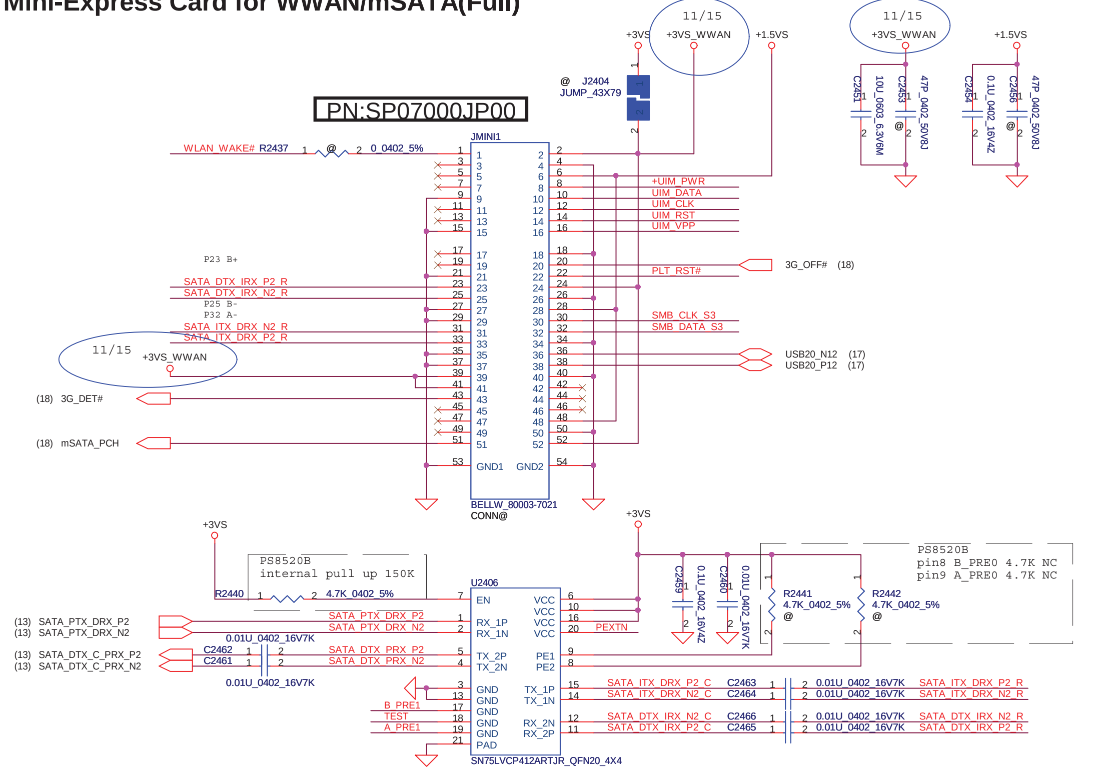
from EC

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

Mini-Express Card for WWAN/mSATA(Full)

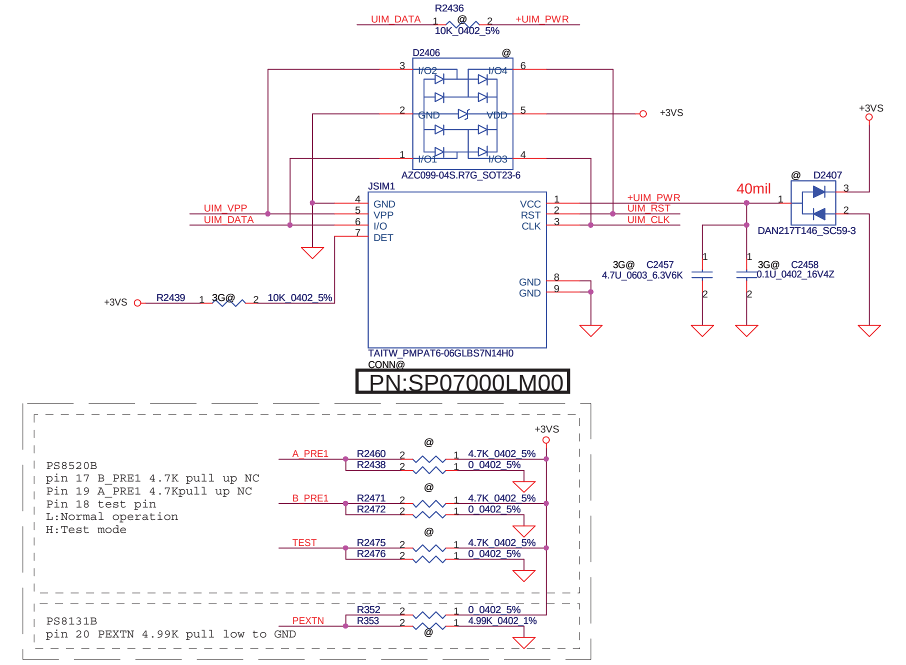
PN:SP07000JP00

PN:SP07000LM00



PS8520B
internal pull up 150K

PS8520B
pin8 B_PRE0 4.7K NC
pin9 A_PRE0 4.7K NC



PS8520B
pin 17 B_PRE1 4.7K pull up NC
Pin 19 A_PRE1 4.7Kpull up NC
Pin 18 test pin
L:Normal operation
H:Test mode

PS8131B
pin 20 PEXTN 4.99K pull low to GND

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
WLAN and WWAN/mSATA

Size Custom
Document Number **LA-8131P**
Rev 0.6

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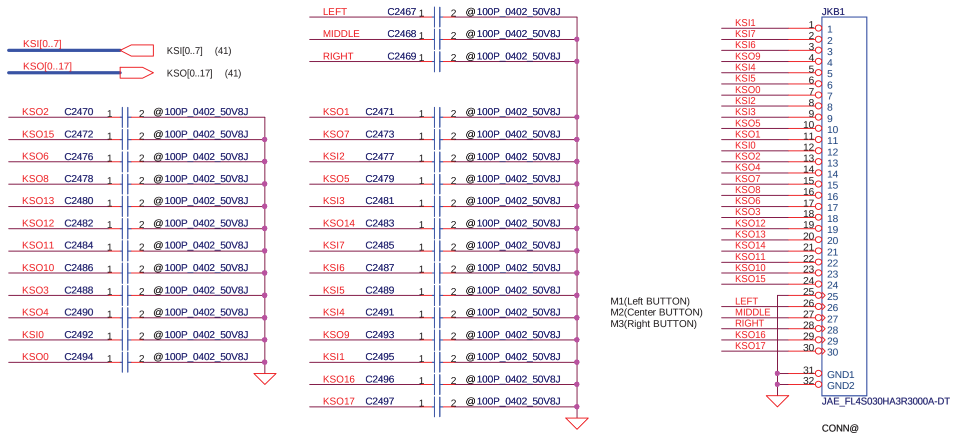
INT_KBD Conn.

PN:SP01000YH00

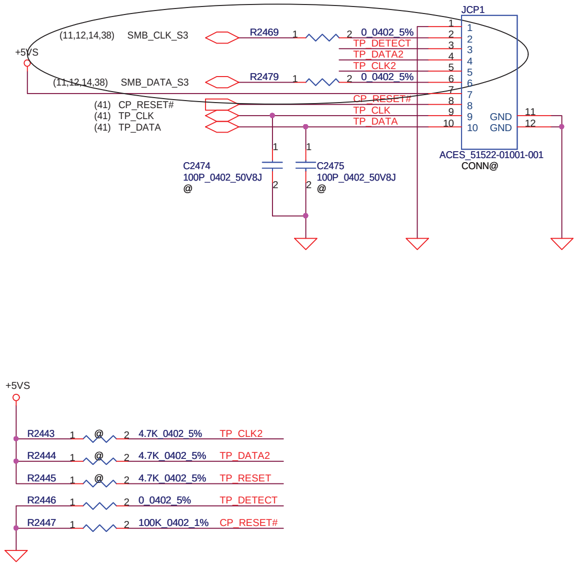

KSI[0..7]
KSI[0..7] (41)
KSO[0..17]
KSO[0..17] (41)
KSO2 C2470 @100P_0402_50V8J
KSO15 C2472 @100P_0402_50V8J
KSO6 C2476 @100P_0402_50V8J
KSO8 C2478 @100P_0402_50V8J
KSO13 C2480 @100P_0402_50V8J
KSO12 C2482 @100P_0402_50V8J
KSO11 C2484 @100P_0402_50V8J
KSO10 C2486 @100P_0402_50V8J
KSO3 C2488 @100P_0402_50V8J
KSO4 C2490 @100P_0402_50V8J
KSI0 C2492 @100P_0402_50V8J
KSO0 C2494 @100P_0402_50V8J
LEFT C2467 @100P_0402_50V8J
MIDDLE C2468 @100P_0402_50V8J
RIGHT C2469 @100P_0402_50V8J
KSO1 C2471 @100P_0402_50V8J
KSO7 C2473 @100P_0402_50V8J
KSI2 C2477 @100P_0402_50V8J
KSO5 C2479 @100P_0402_50V8J
KSI3 C2481 @100P_0402_50V8J
KSO14 C2483 @100P_0402_50V8J
KSI7 C2485 @100P_0402_50V8J
KSI6 C2487 @100P_0402_50V8J
KSI5 C2489 @100P_0402_50V8J
KSI4 C2491 @100P_0402_50V8J
KSO9 C2493 @100P_0402_50V8J
KSI1 C2495 @100P_0402_50V8J
KSO16 C2496 @100P_0402_50V8J
KSO17 C2497 @100P_0402_50V8J
M1(Left BUTTON)
M2(Center BUTTON)
M3(Right BUTTON)
JKB1
KSI1 KSI7 KSI6 KSO9 KSI4 KSI5 KSO0 KSI2 KSI3 KSO5 KSO1 KSI0 KSO2 KSO4 KSO7 KSO8 KSO6 KSO3 KSO12 KSO13 KSO14 KSO11 KSO10 KSO15
LEFT MIDDLE RIGHT KSO16 KSO17
GND1
GND2
JAE_FL4S030HA3R3000A-DT
CONN@

CONN PIN define need double check

Reserve for ESD.

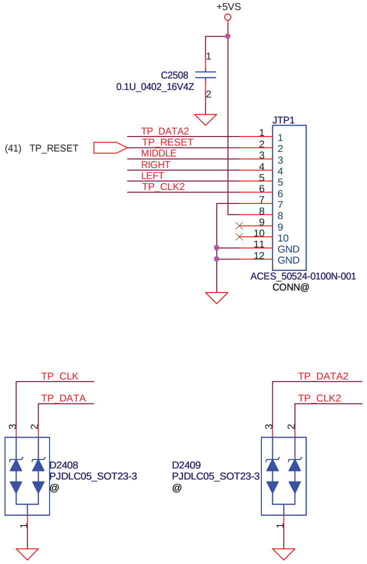
Click pad

PN:SP01001AL00



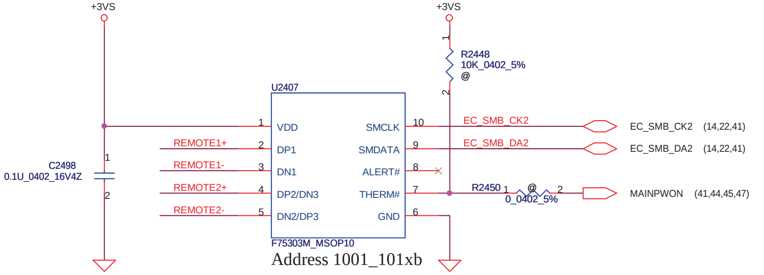
Track point

PN:SP01001CH00

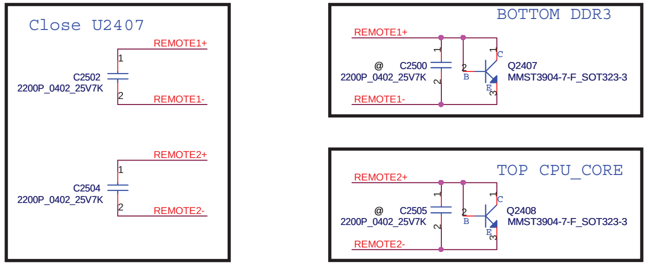


PN: SCA00000U10 X 2

Fintek thermal sensor placed near by TOP DDR3

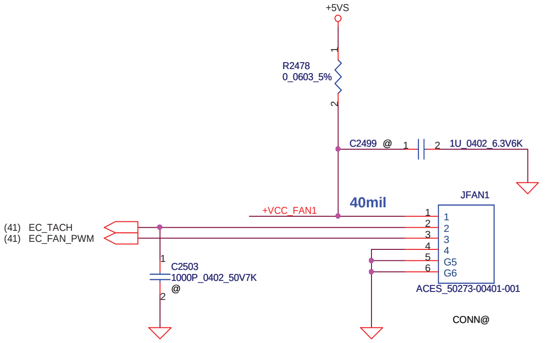


2nd source
SA000029210-->EMC1403-2-AIZL-TR



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

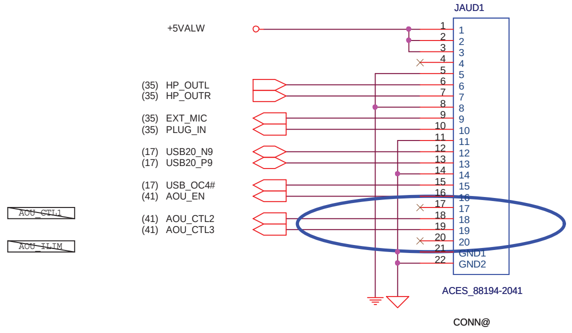
FAN CONN.



PN:SP02000U900

Audio Board

PN:SP011108040



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
KB/TP/Thermal Sensor/Audio

Size	Document Number	Rev
Custom	LA-8131P	0.6

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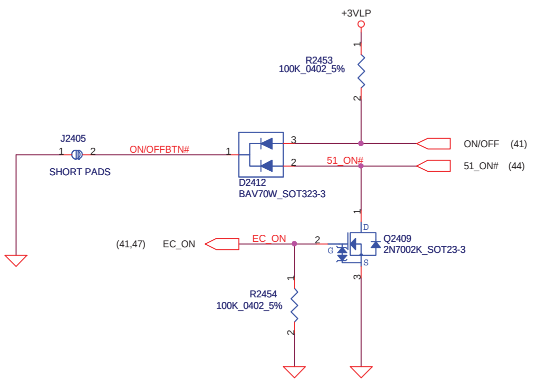
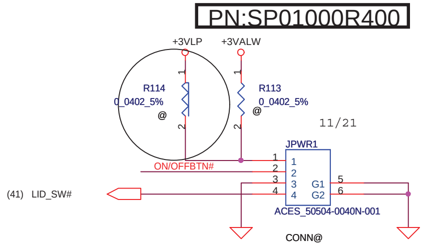
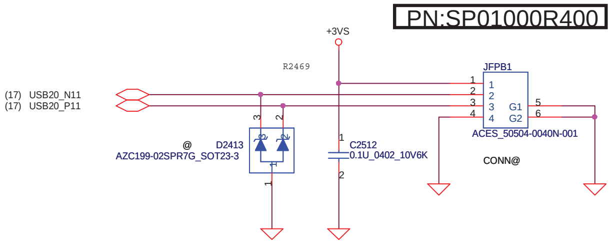
Power Button



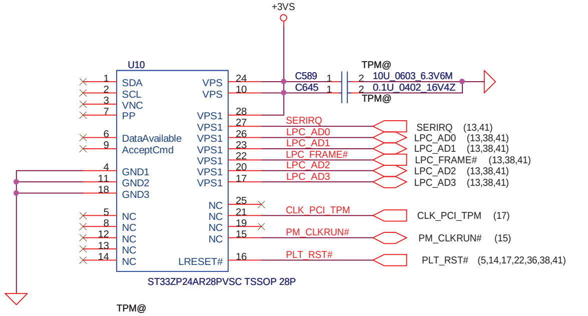
Power Button CONN.

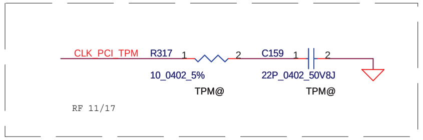


Finger Print Board

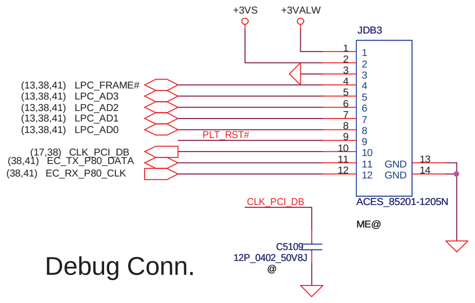


TPM

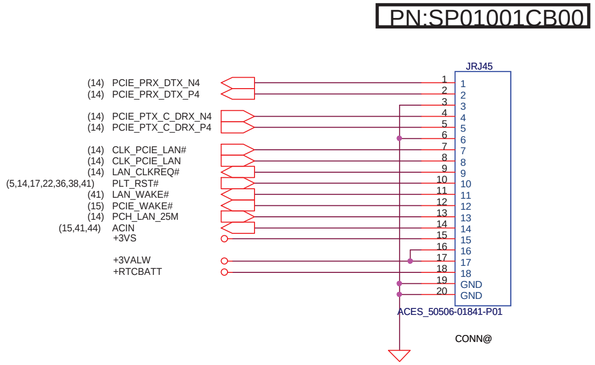




Debug Conn.



RJ45 Board



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title PWR Button/Power OK/RJ45
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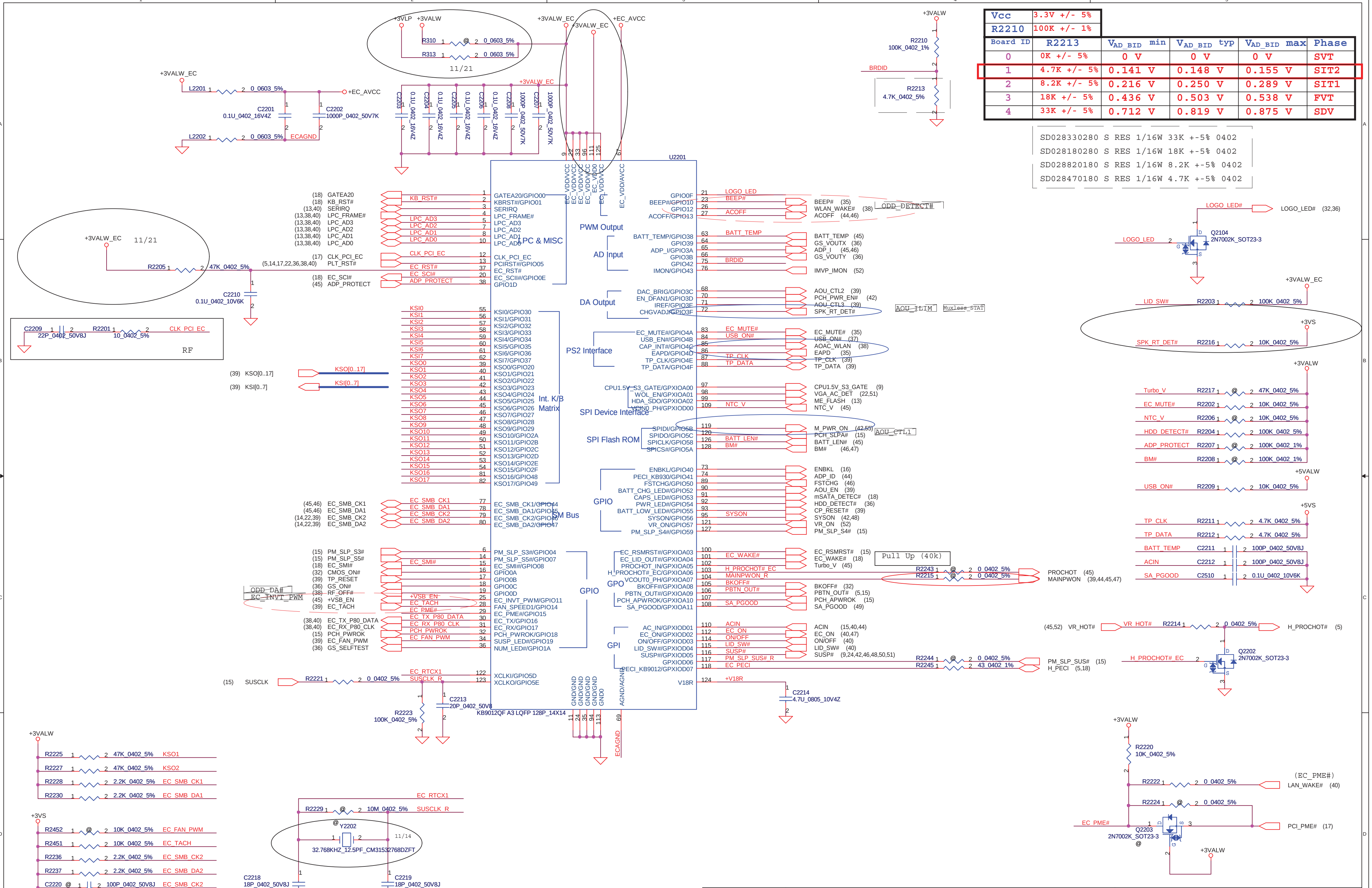
				Date: Tuesday, January 10, 2012 Sheet 40 of 58



Vcc	3.3V +/- 5%
R2210	100K +/- 1%

Board ID	R2213	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SVT
1	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	SIT2
2	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SIT1
3	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
4	33K +/- 5%	0.712 V	0.819 V	0.875 V	SDV

SD028330280 S RES 1/16W 33K +-5% 0402
SD028180280 S RES 1/16W 18K +-5% 0402
SD028820180 S RES 1/16W 8.2K +-5% 0402
SD028470180 S RES 1/16W 4.7K +-5% 0402

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
EC ENE-KB9012

Size Custom
Document Number **LA-8131P**
Rev 0.6

Date: Friday, January 06, 2012
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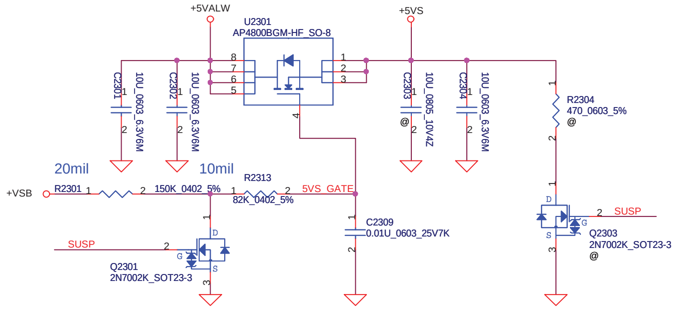
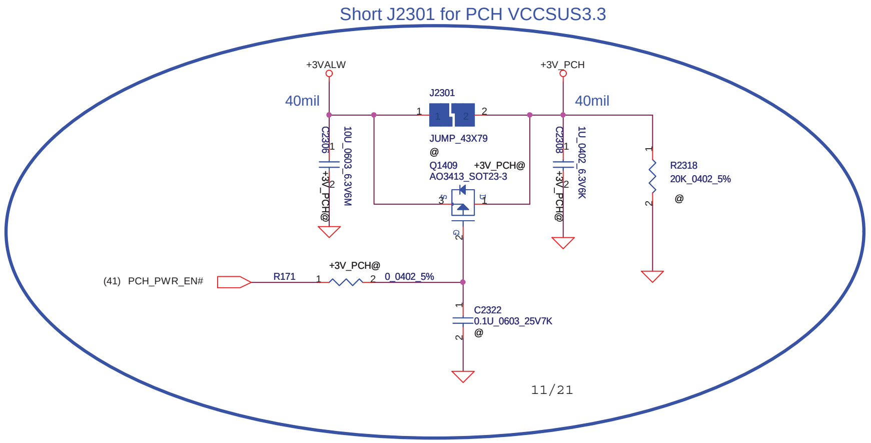
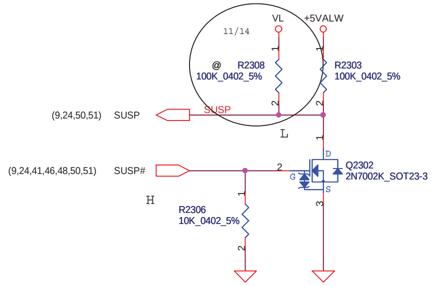
+5VALW TO +5VS

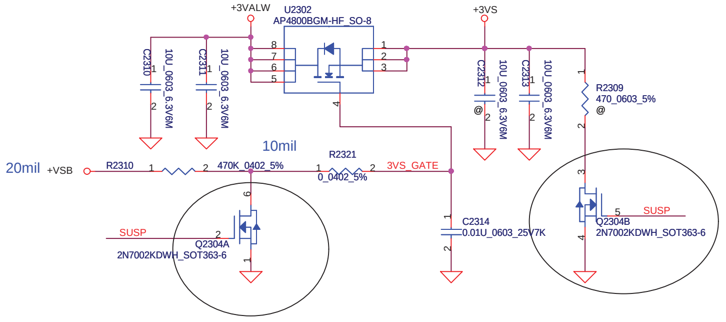


+3VALW TO +3VALW(PCH AUX Power)

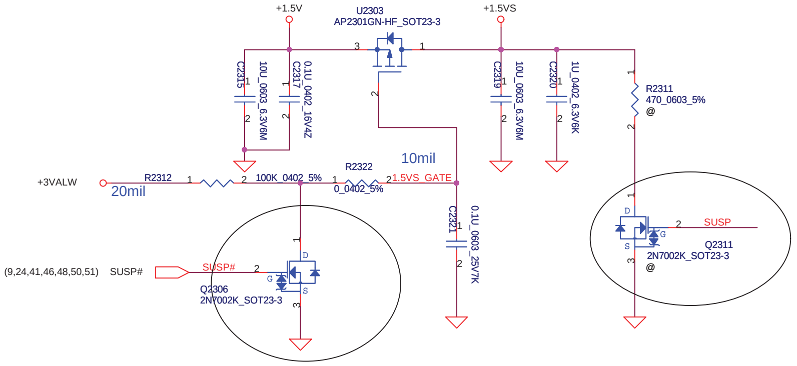




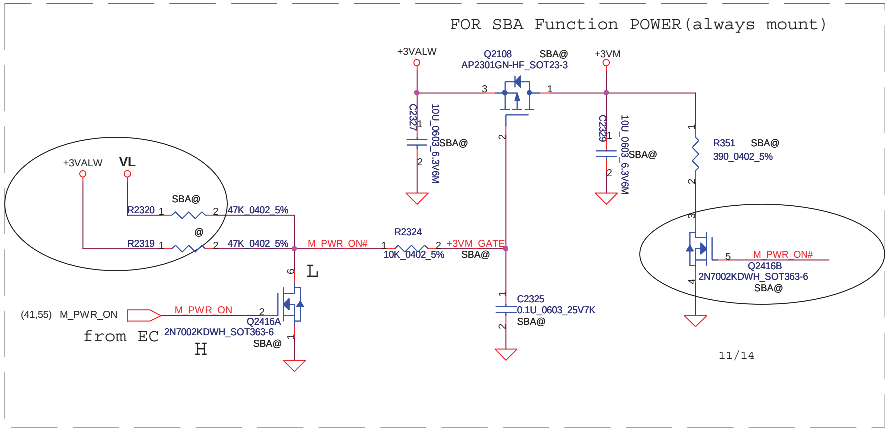
+3VALW TO +3VS

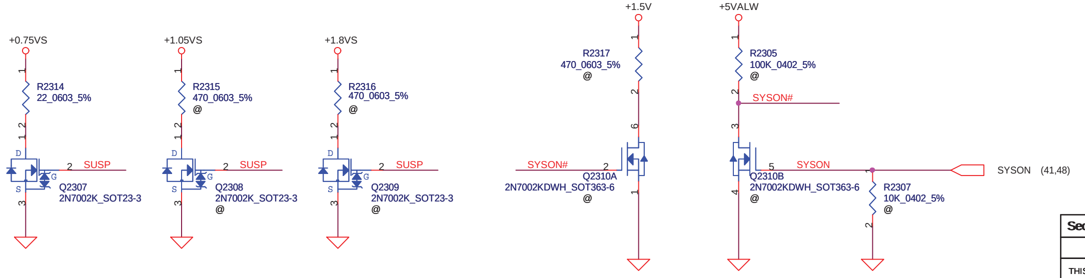


+1.5V to +1.5VS



FOR SBA Function POWER(always mount)





Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title	DC Interface		
Size Custom	Document Number LA-8131P		Rev 0.6
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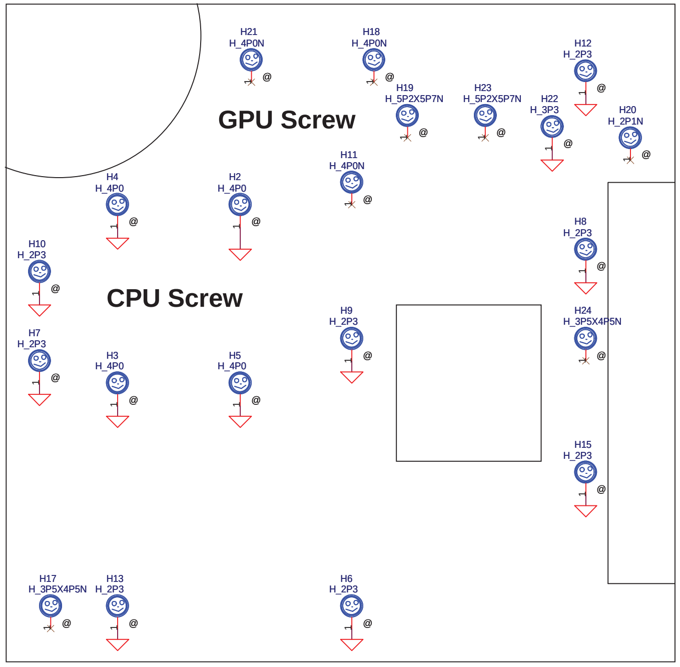
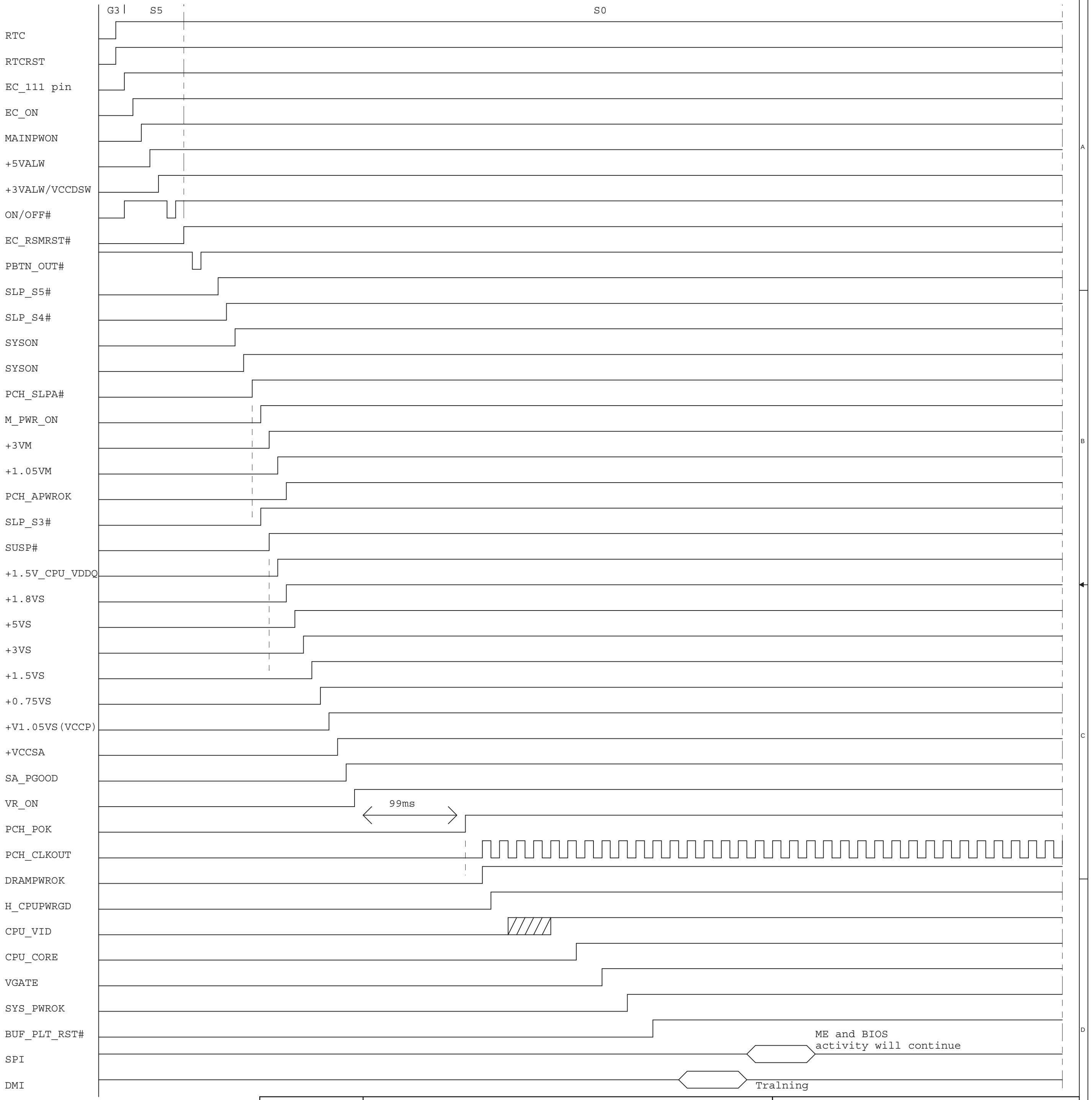




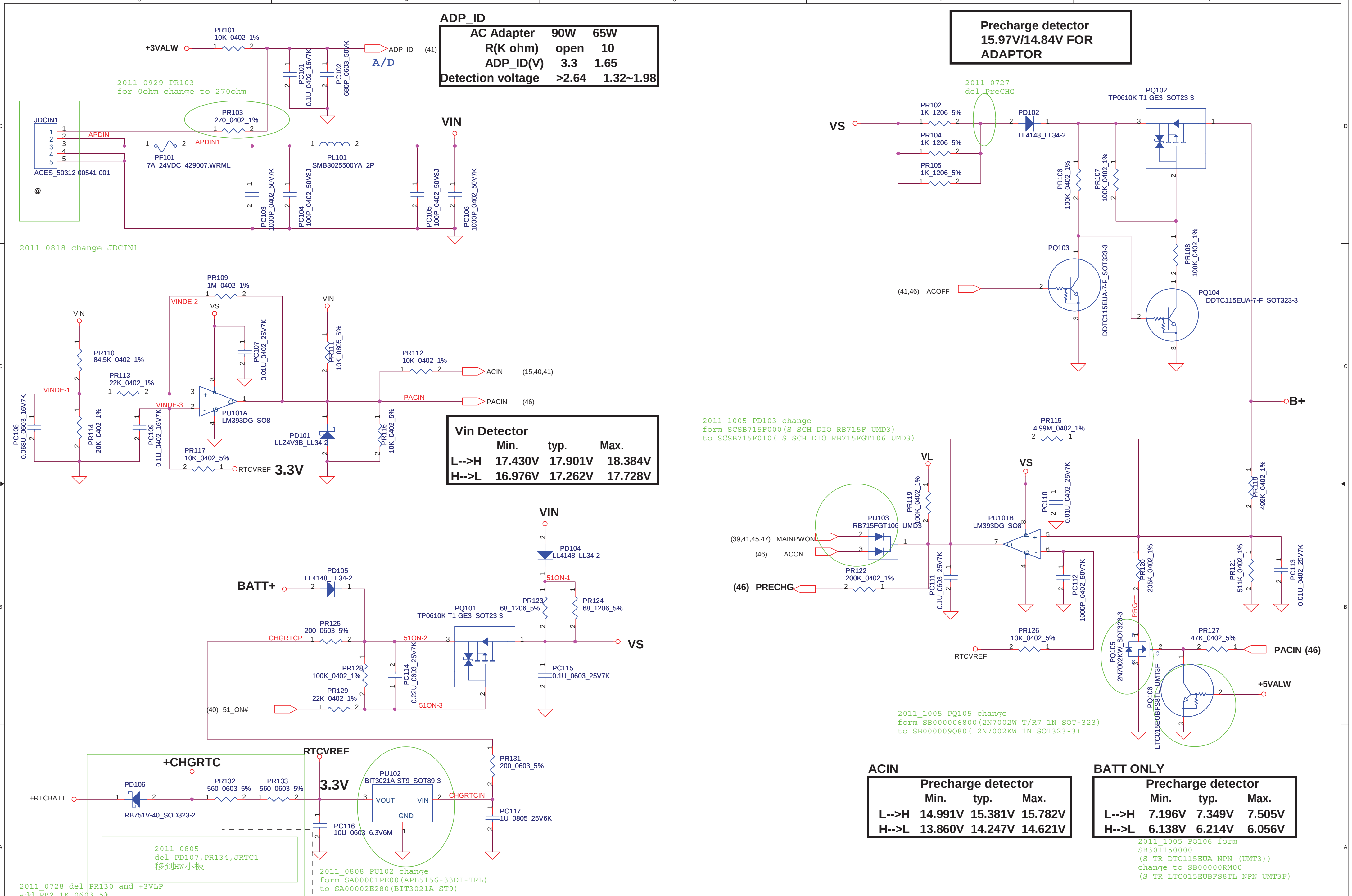
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
Screw Hole

Size Custom
Document Number **LA-8131P**
Rev 0.6

Date: Friday, January 06, 2012 Sheet 43 of 58



ADP_ID

AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

ACIN

Precharge detector

	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector

	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

2011_1005 PQ106 form
SB301150000
(S TR DTC115EUA NPN (UMT3))
change to SB00000RM00
(S TR LTC015EUBFS8TL NPN UMT3F)

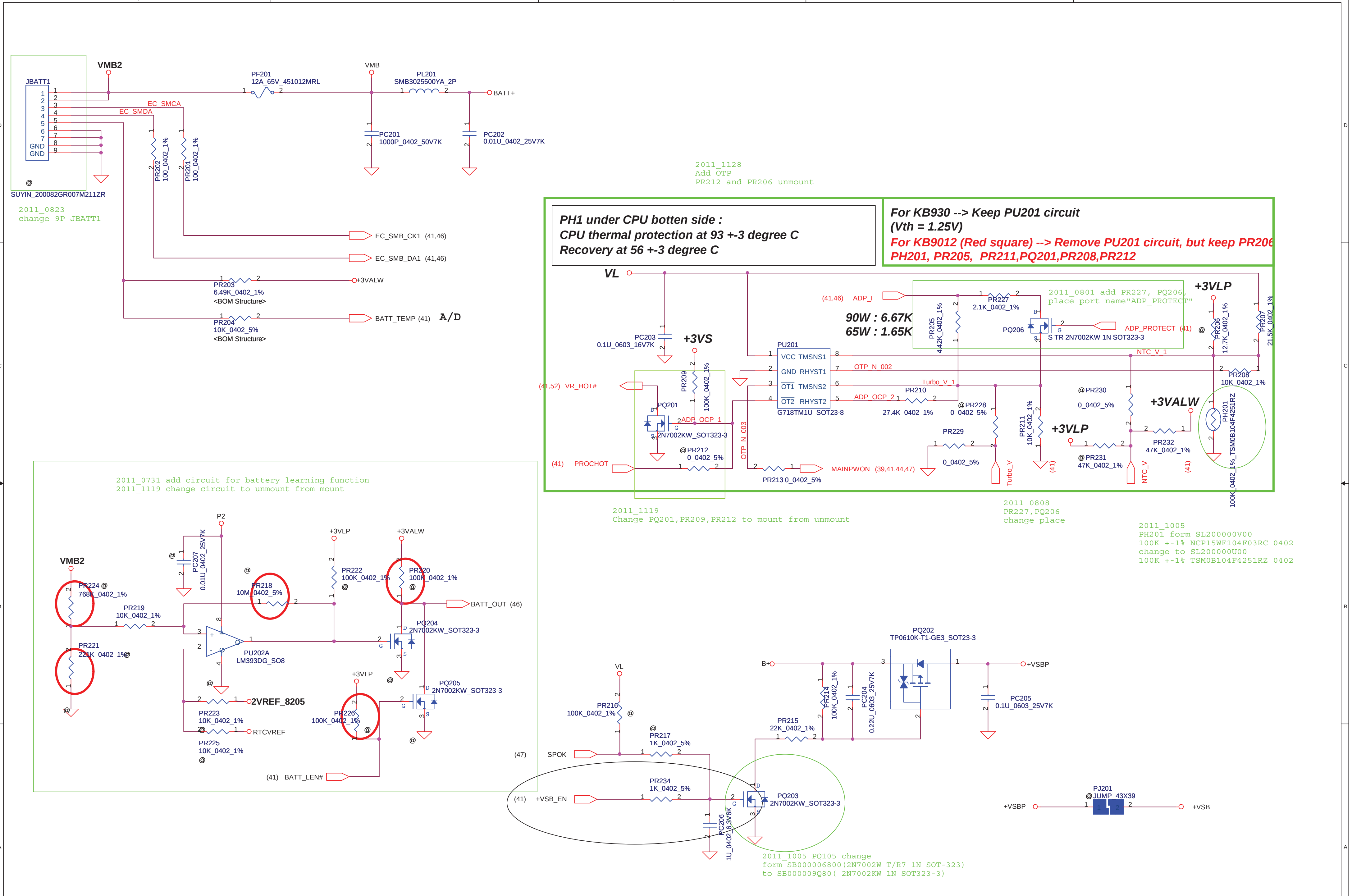
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title

PWR DCIN / Vin Detector /Pre-charge

Size Custom
Document Number
LA-8133P
Rev 0.6
Date: Friday, January 06, 2012



2011_0823
change 9P JBATT1

2011_1128
Add OTP
PR212 and PR206 unmount

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU201 circuit
(Vth = 1.25V)
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211,PQ201,PR208,PR212

2011_0801 add PR227, PQ206,
place port name"ADP_PROTECT"

2011_0731 add circuit for battery learning function
2011_1119 change circuit to unmount from mount

2011_1119
Change PQ201,PR209,PR212 to mount from unmount

2011_0808
PR227,PQ206
change place

2011_1005
PH201 form SL200000V00
100K +-1% NCP15WF104F03RC 0402
change to SL200000U00
100K +-1% TSM0B104F4251RZ 0402

2011_1005 PQ105 change
form SB000006800(2N7002W T/R7 1N SOT-323)
to SB000009Q80(2N7002KW 1N SOT323-3)

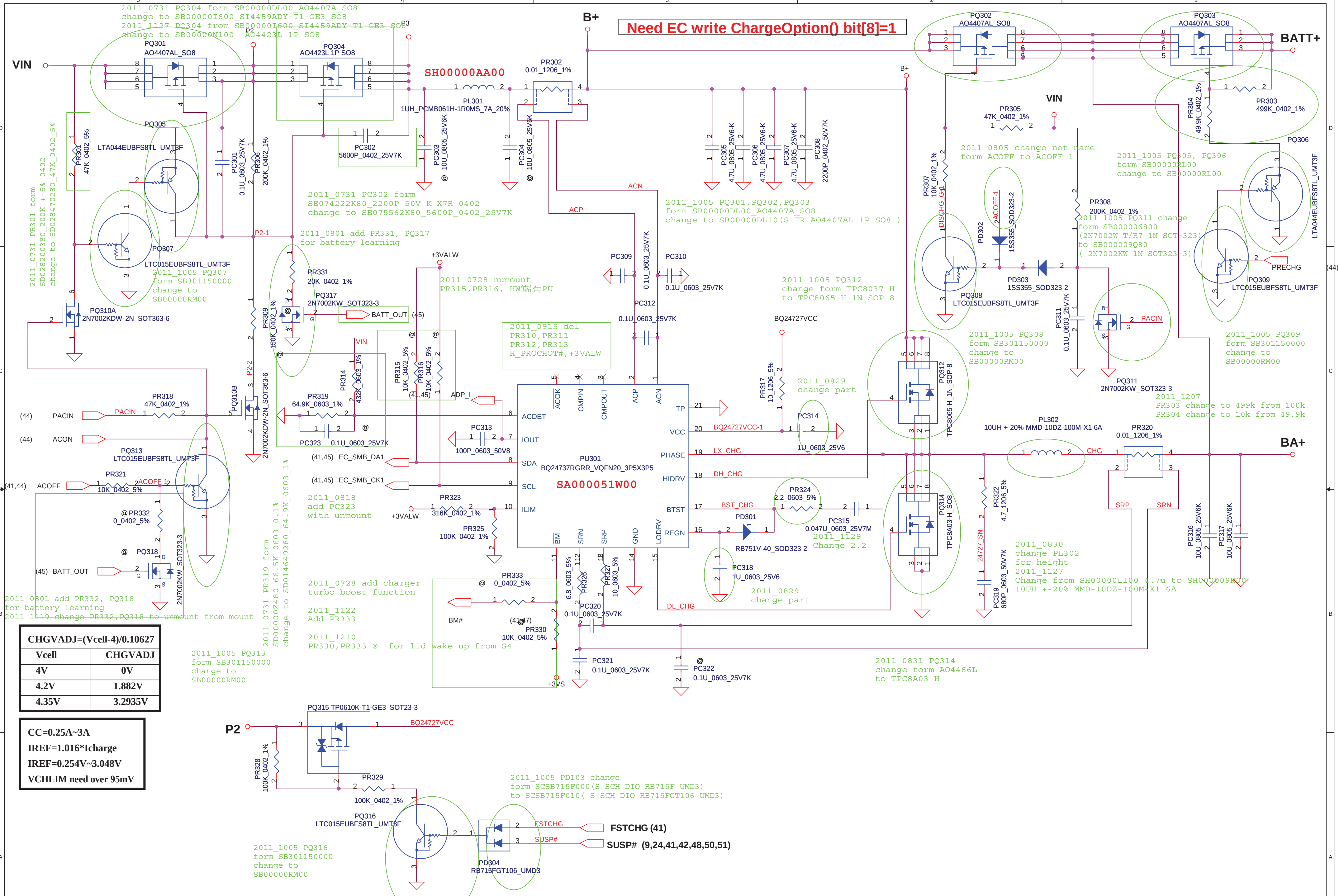
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
PWR-BATTERY CONN/OTP

Size Custom
Document Number LA-8133P
Rev 0.6

Date: Tuesday, January 10, 2012



Need EC write ChargeOption() bit[8]=1

2011_0731 PQ304 form SB00000DL00_AO4407A_SO8
change to SB00000I600_SI4459ADY-T1-GE3_SO8
2011_1127 PQ304 from SB00000I600_SI4459ADY-T1-GE3_SO8
change to SB00000N100 AO4423L 1P SO8

2011_0731 PR301 form
SD028200380_200K +-5% 0402
change to SD028470280_47K_0402_5%

2011_1005 PQ307
form SB301150000
change to
SB00000RM00

2011_0731 PC302 form
SE074222K80_2200P 50V K X7R 0402
change to SE075562K80_5600P_0402_25V7K

2011_0801 add PR331, PQ317
for battery learning

2011_0728 numount
PR315,PR316, HW端有PU

2011_0915 del
PR310,PR311
PR312,PR313
H_PROCHOT#,+3VALW

2011_1005 PQ301,PQ302,PQ303
form SB00000DL00_AO4407A_SO8
change to SB00000DL10(S TR AO4407AL 1P SO8)

2011_1005 PQ312
change form TPC8037-H
to TPC8065-H_1N_SOP-8

2011_0805 change net name
form ACOFF to ACOFF-1

2011_1005 PQ305, PQ306
form SB00000RL00
change to SB00000RL00

2011_1005 PQ311 change
form SB000006800
(2N7002W T/R7 1N SOT-323)
to SB000009Q80
(2N7002KW 1N SOT323-3)

2011_1005 PQ308
form SB301150000
change to
SB00000RM00

2011_1005 PQ309
form SB301150000
change to
SB00000RM00

2011_0829
change part

2011_1207
PR303 change to 499k from 100k
PR304 change to 10k from 49.9k

2011_0801 add PR332, PQ318
for battery learning
2011_1119 change PR332,PQ318 to unmount from mount

2011_0731 PR319 form
SD00000Z480_66.5K_0603_0.1%
change to SD014649280_64.9K_0603_1%

2011_0818
add PC323
with unmount

2011_0728 add charger
turbo boost function

2011_1122
Add PR333

2011_1210
PR330,PR333 @ for lid wake up from S4

2011_1005 PQ313
form SB301150000
change to
SB00000RM00

2011_1129
Change 2.2

2011_0829
change part

2011_0830
change PL302
for height
2011_1127
Change from SH00000LI00 4.7u to SH000009R00
10UH +-20% MMD-10DZ-100M-X1 6A

2011_0831 PQ314
change form AO4466L
to TPC8A03-H

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

2011_1005 PD103 change
form SCSB715F000(S SCH DIO RB715F UMD3)
to SCSB715F010(S SCH DIO RB715FGT106 UMD3)

2011_1005 PQ316
form SB301150000
change to
SB00000RM00

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title CHARGER
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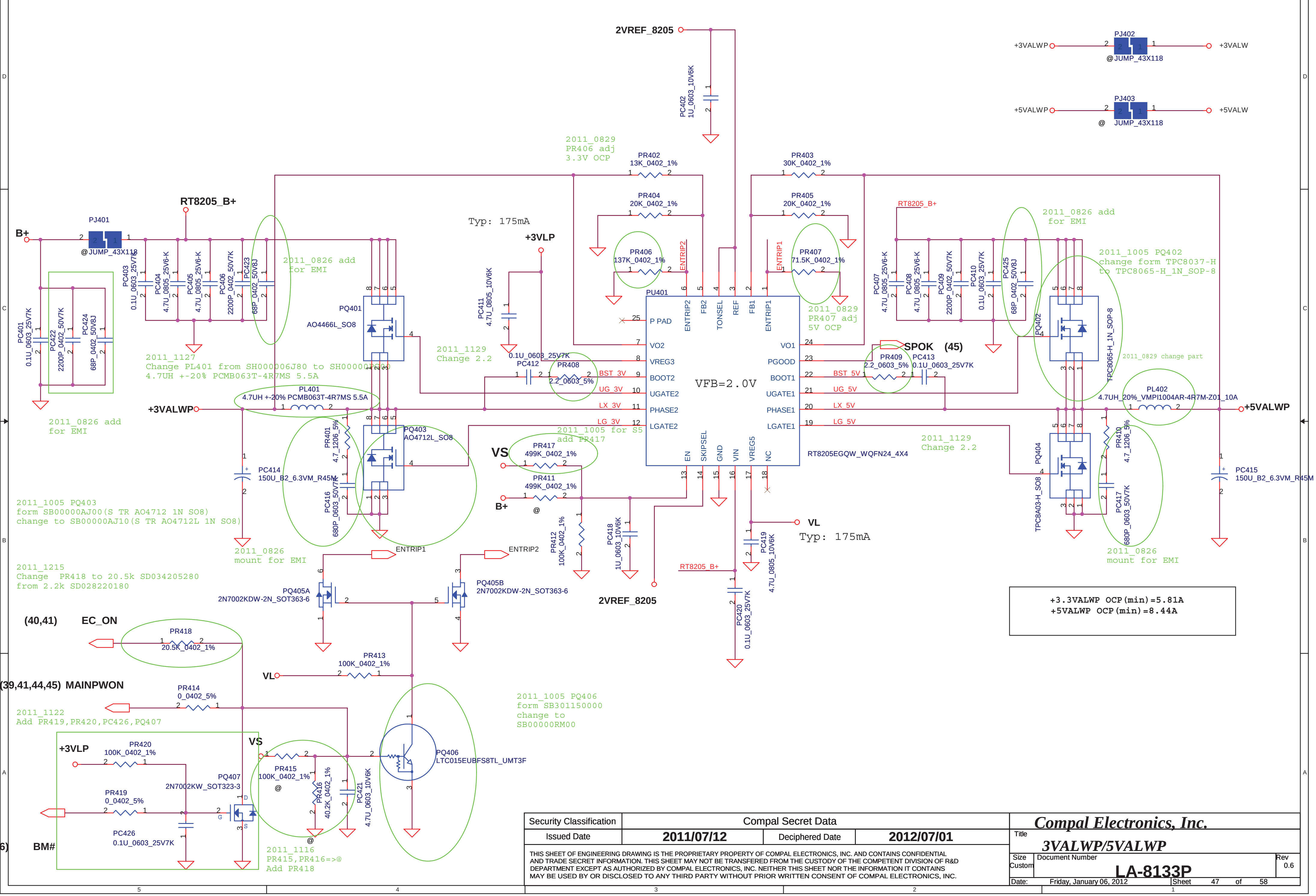
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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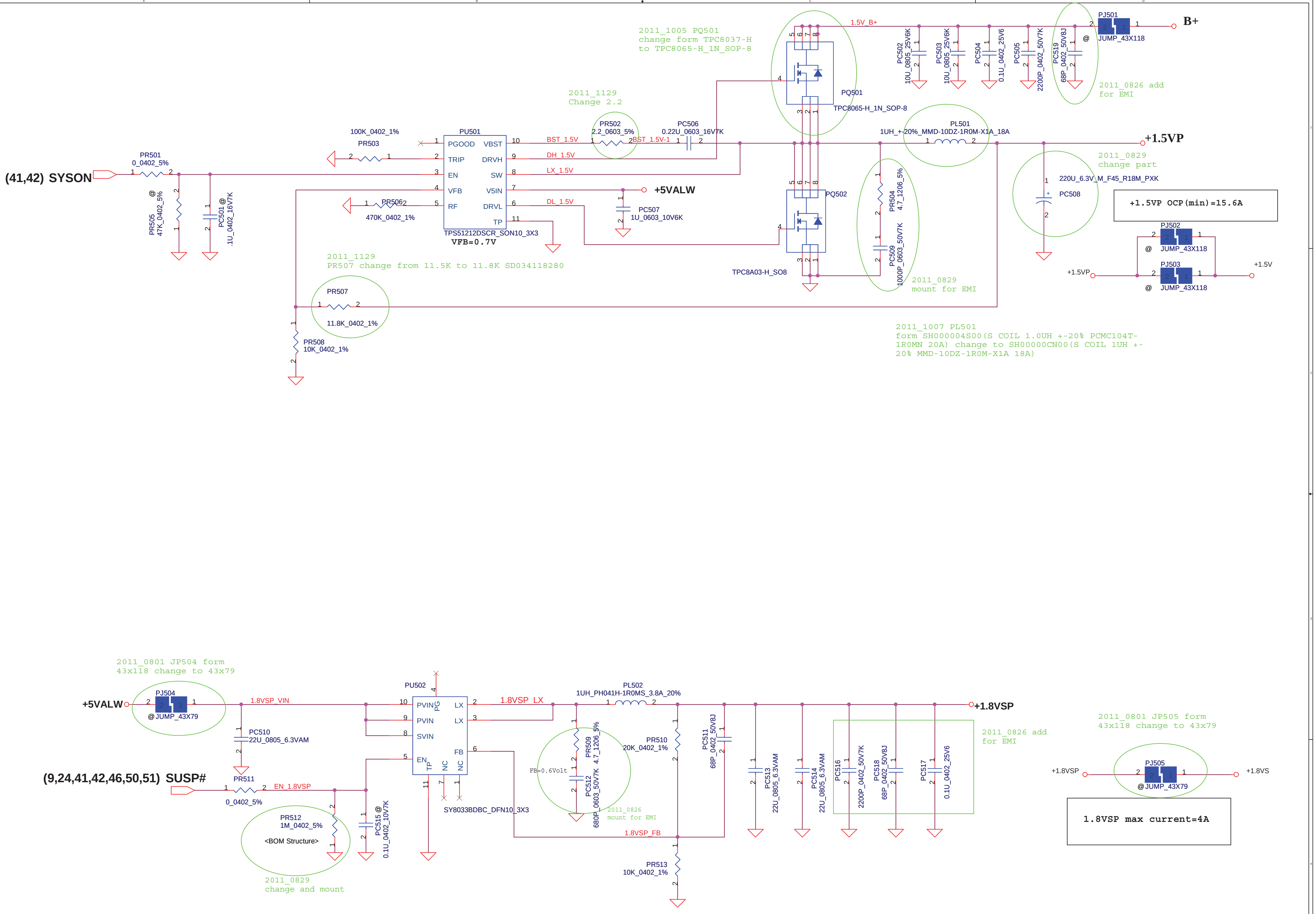
Compal Electronics, Inc.

Title
3VALWP/5VALWP

Size Custom
Document Number LA-8133P
Rev 0.6

Date: Friday, January 06, 2012



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title

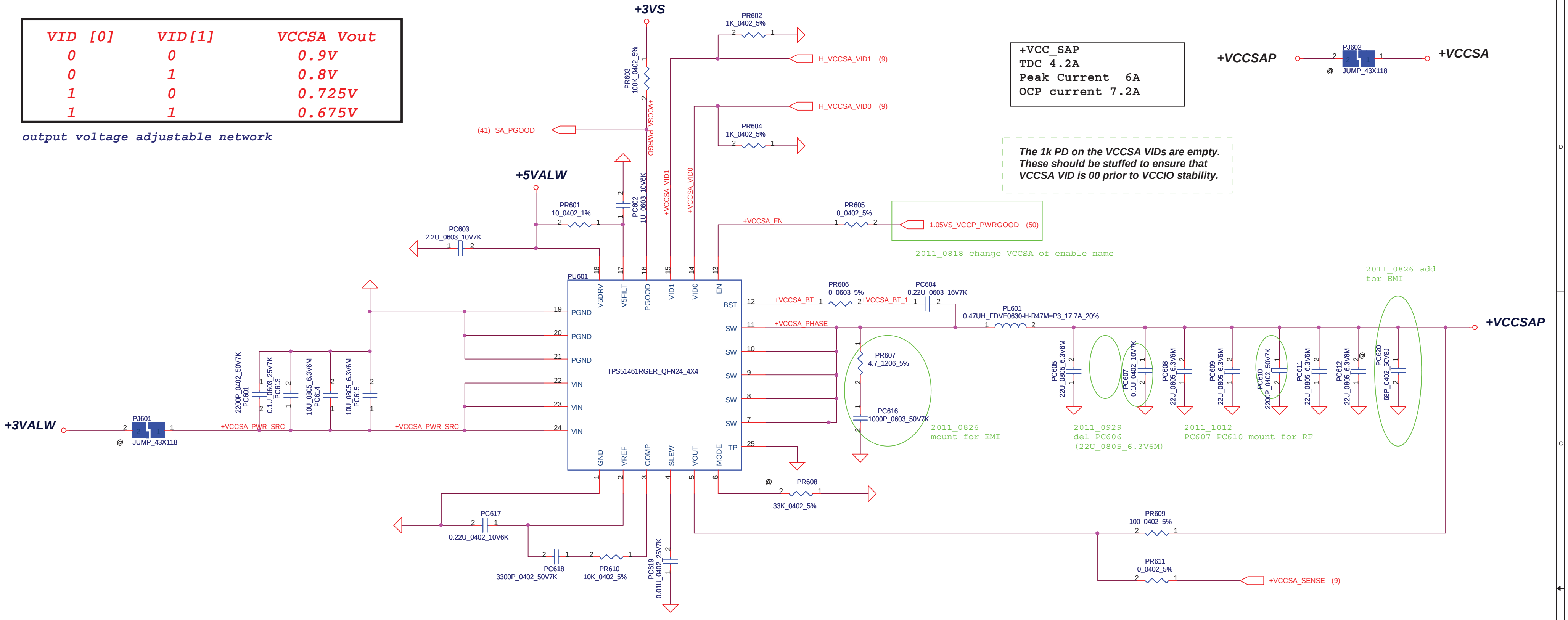
PWR-+1.5VP/+1.8VSP

Size	Document Number	Rev
Custom	LA-8133P	0.6

Date: Friday, January 06, 2012 Sheet 48 of 58

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

2011_0801 del +V1.05S_VCCPP circuit

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title
PWR +VCCSAP/1.0

Size C
Document Number LA-8133P
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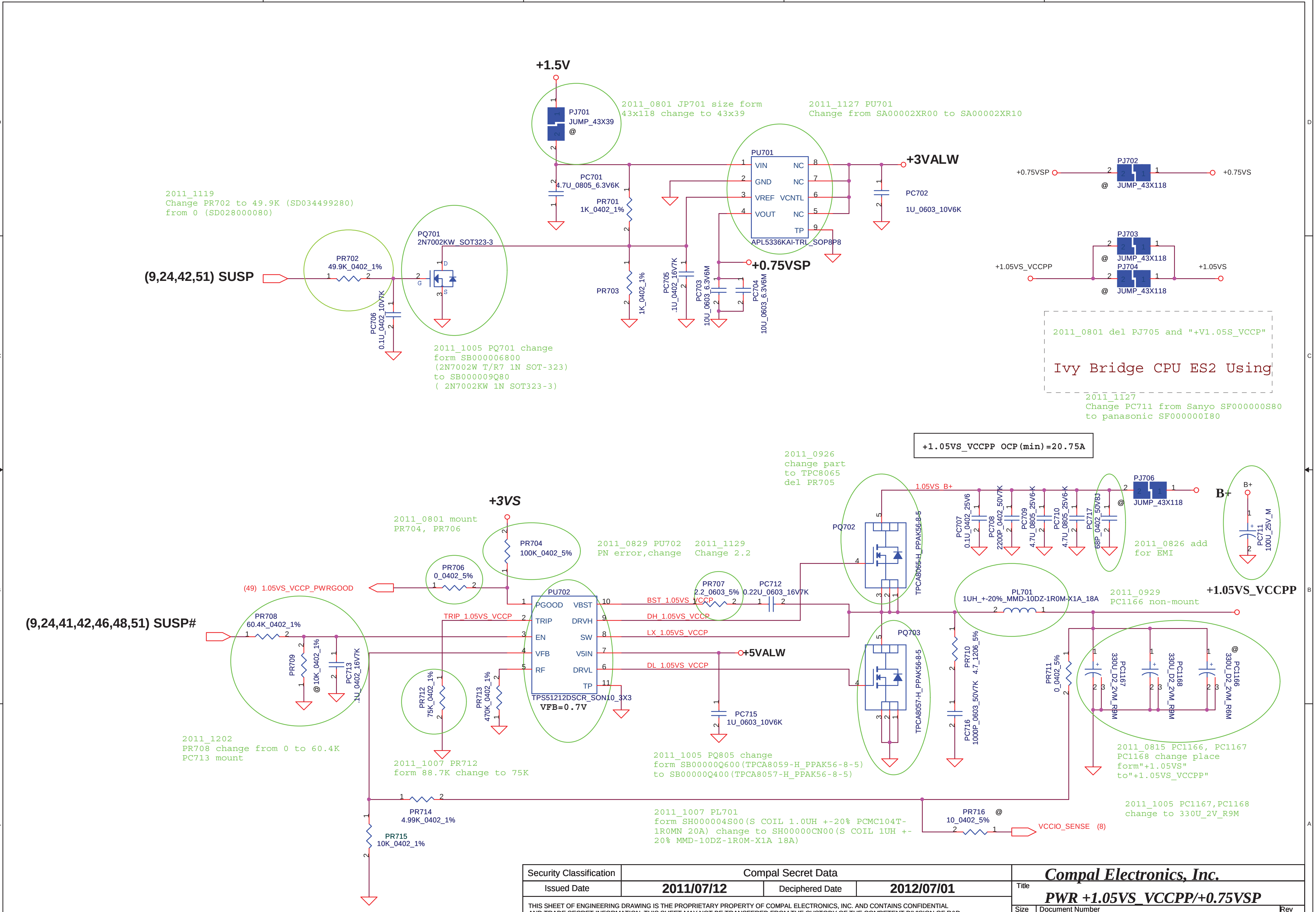

2011_0801 JP701 size form 43x118 change to 43x39

2011_1127 PU701 Change from SA00002XR00 to SA00002XR10

2011_1119 Change PR702 to 49.9K (SD034499280) from 0 (SD028000080)

2011_1005 PQ701 change form SB000006800 (2N7002W T/R7 1N SOT-323) to SB000009Q80 (2N7002KW 1N SOT323-3)

2011_0801 del PJ705 and "+V1.05S_VCCP"

Ivy Bridge CPU ES2 Using

2011_1127 Change PC711 from Sanyo SF000000S80 to panasonic SF000000I80

+1.05VS_VCCPP OCP(min)=20.75A

2011_0926 change part to TPC8065 del PR705

2011_0801 mount PR704, PR706

2011_0829 PU702 PN error,change

2011_1129 Change 2.2

2011_0826 add for EMI

2011_0929 PC1166 non-mount

2011_1202 PR708 change from 0 to 60.4K PC713 mount

2011_1007 PR712 form 88.7K change to 75K

2011_1005 PQ805 change form SB00000Q600(TPCA8059-H_PPAK56-8-5) to SB00000Q400(TPCA8057-H_PPAK56-8-5)

2011_0815 PC1166, PC1167 PC1168 change place form"+1.05VS" to"+1.05VS_VCCPP"

2011_1007 PL701 form SH000004S00(S COIL 1.0UH +-20% PCMC104T-1R0MN 20A) change to SH00000CN00(S COIL 1UH +-20% MMD-10DZ-1R0M-X1A 18A)

2011_1005 PC1167,PC1168 change to 330U_2V_R9M

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Title ***PWR +1.05VS_VCCPP/+0.75VSP***

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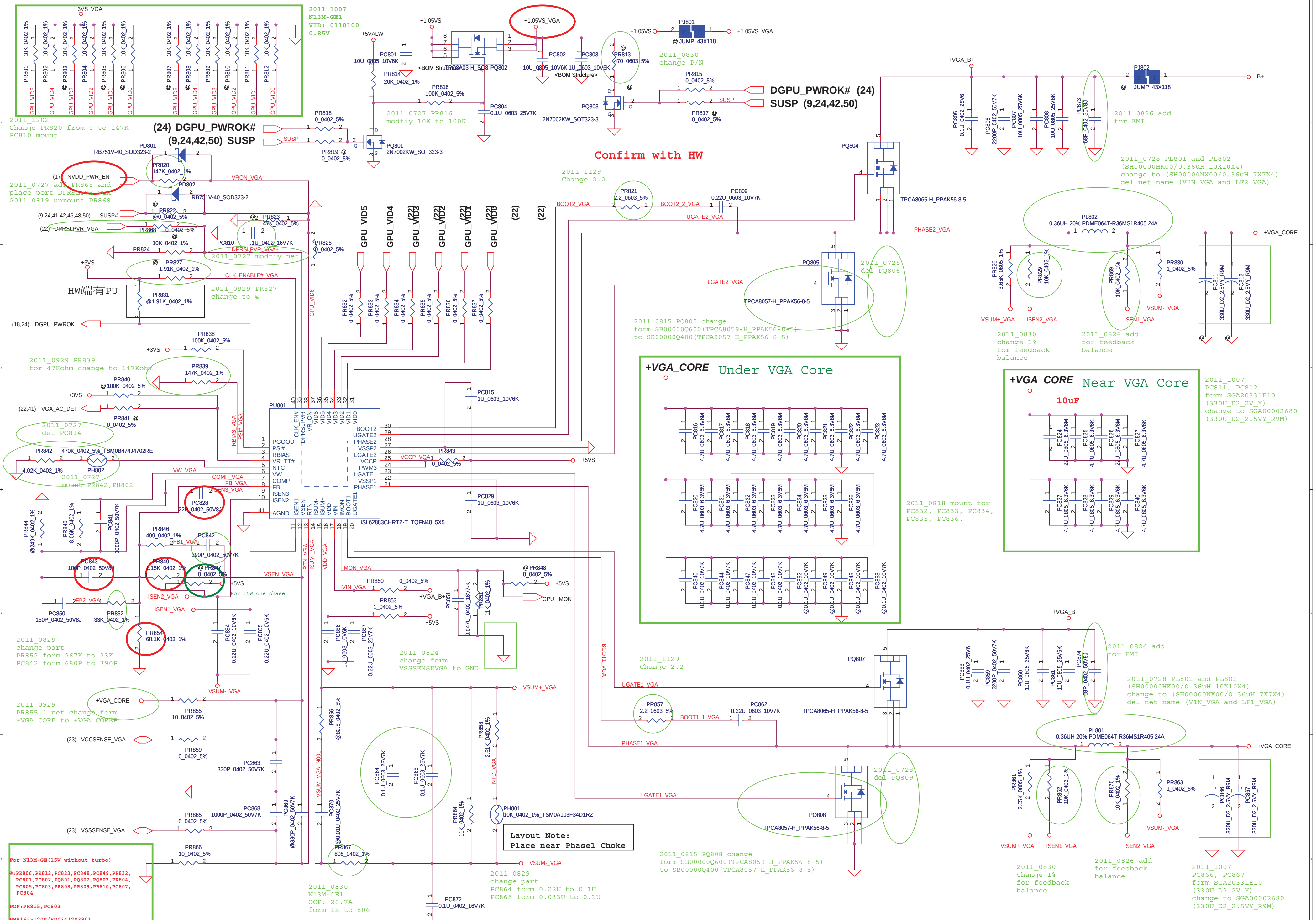

For N13M-GE(15W without turbo)

@:PR806,PR812,PC823,PC848,PC849,PR832,
PC801,PC802,PQ801,PQ802,PQ803,PR804,
PC805,PC803,PR808,PR809,PR810,PC807,
PC804

POP:PR815,PC803

PR816->120K(SD034120380)
PR820->1.69K(SD00000JB80)
PR822->22K(SD034220280)
PR837->866(SD034866080)
PC858->0.1uF(SE026104M80)
PC859->0.068uF(SE026683K80)
PR850->22.1K(SD034221280)

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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title PWR - VGA_COREP
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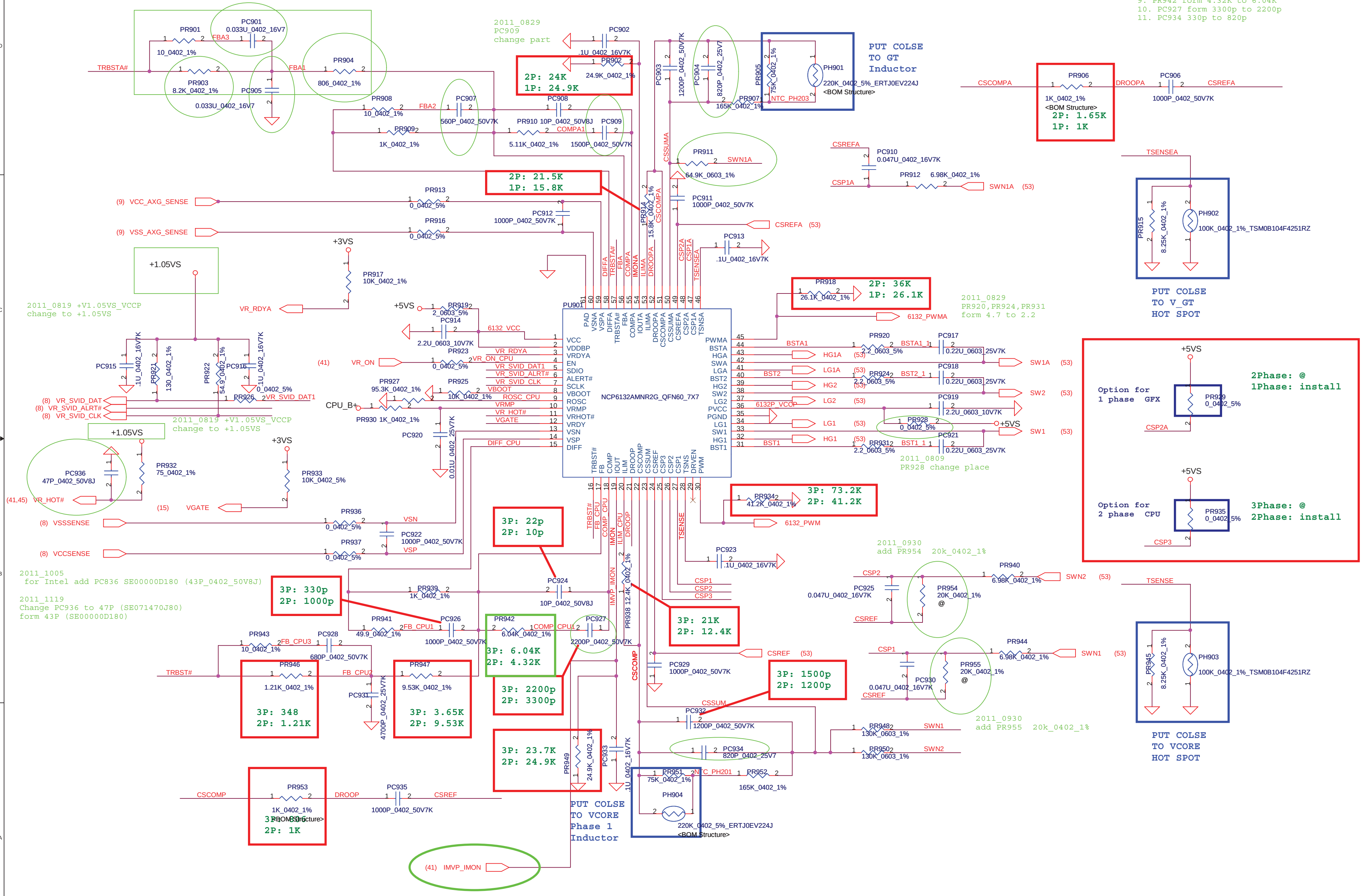
2011_0830
PC901,PC905,PR901,PR903,PR904 mount

2011_1119
Change PC901,PC905 to 0.033u (SE076333K80)
from 0.033u (SE076333KN0)

2011_1007 for function test
1. modify PR903 form 1.21K to 8.2K,
2. PC905 form 4700p to 33n,
3. PC901 form 680p to 33n,
4. PR904 form 10.7K to 806,
5. PC907 form 330p to 560p
6. PC909 form 3300p to 1500p
7. PC904 form 330p to 820p
8. PR911 form 63.4K to 66.5K
9. PR942 form 4.32K to 6.04K
10. PC927 form 3300p to 2200p
11. PC934 330p to 820p



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Title
PWR-CPU_CORE1

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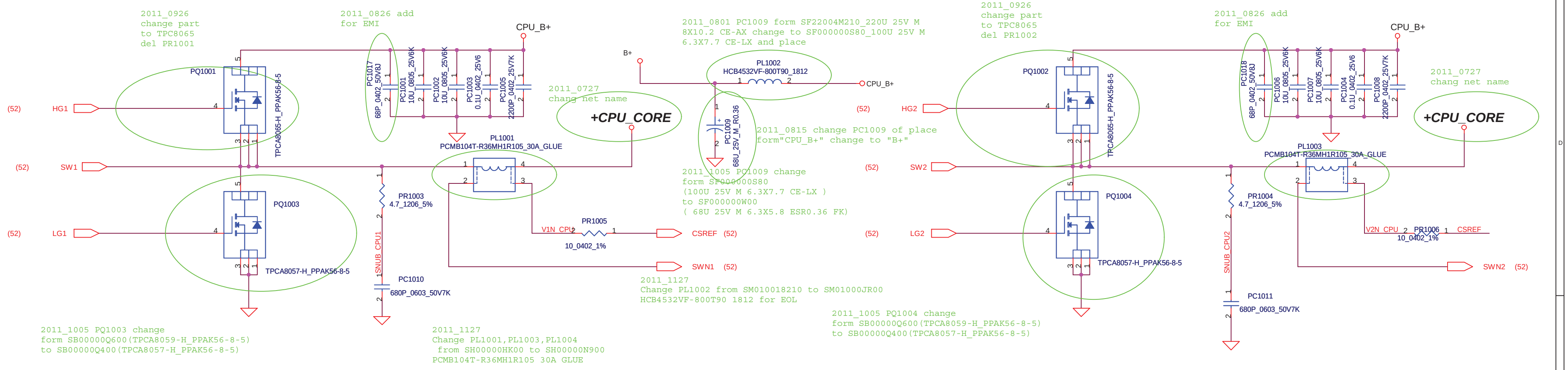
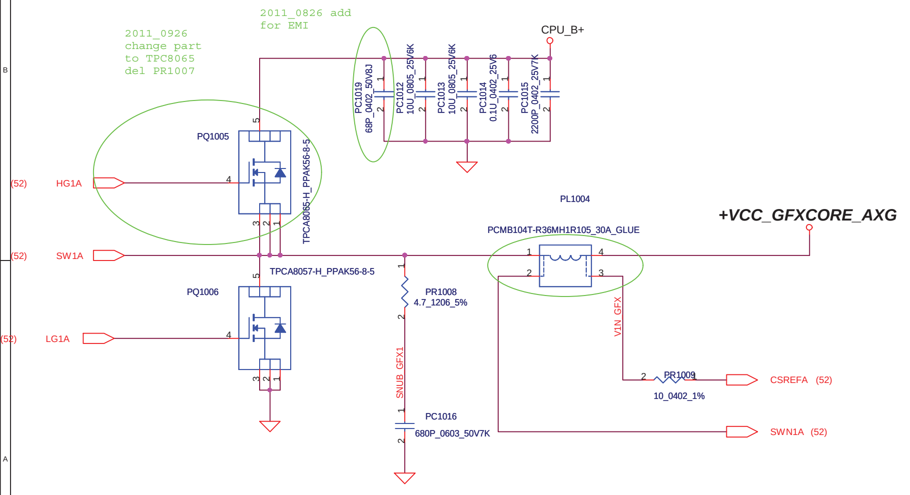


QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

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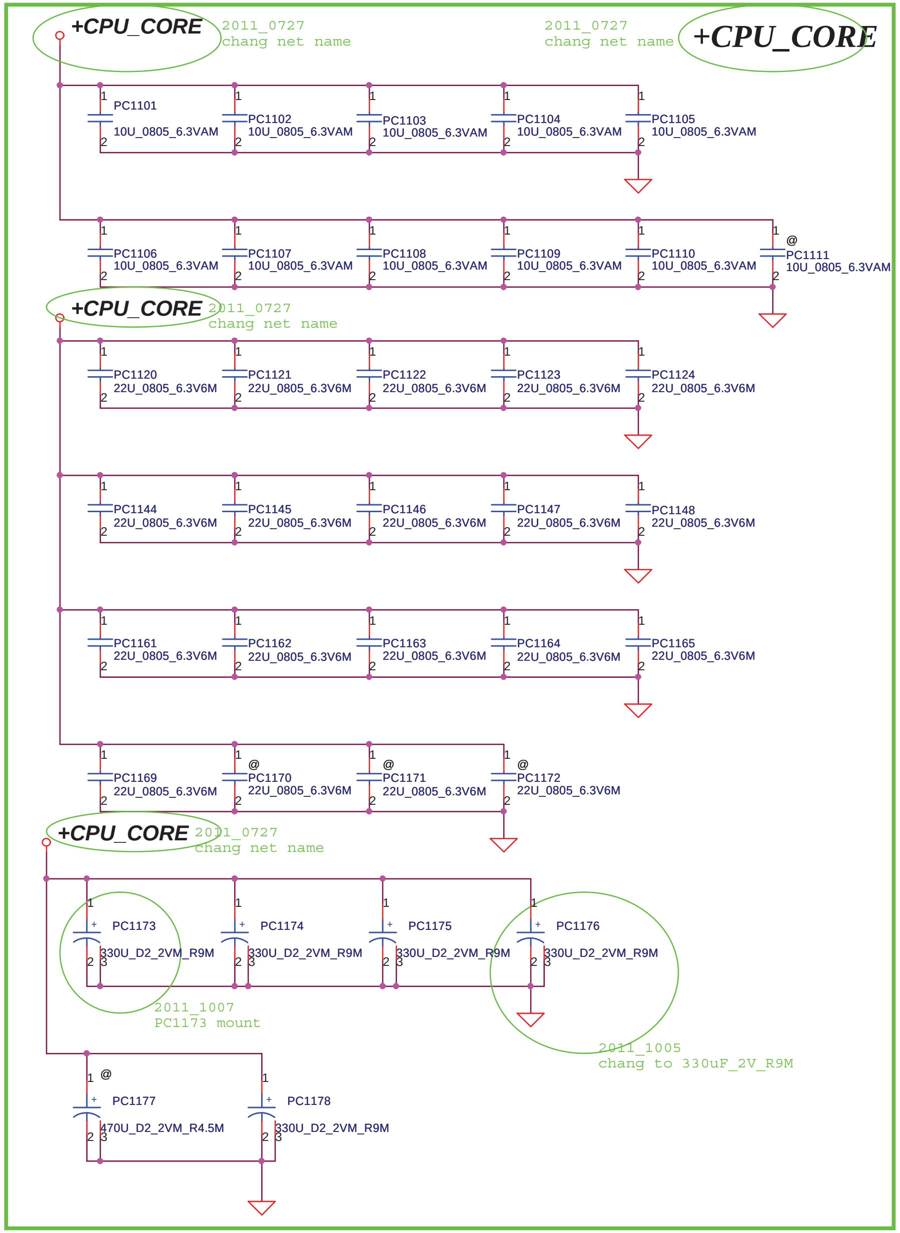
Issued Date	**2011/07/12**	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
PWR-CPU_CORE2

Size C
Document Number **LA-8133P**
Rev 0.6

Date: Friday, January 06, 2012



+CPU_CORE 2011_0727 chang net name

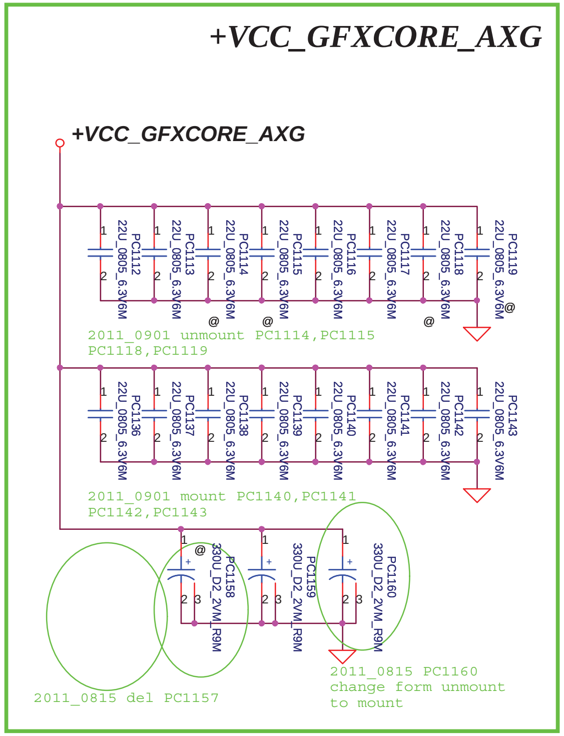
2011_0727 chang net name +CPU_CORE

2011_0727 chang net name

2011_0727 chang net name

2011_1007 PC1173 mount

2011_1005 chang to 330uF_2V_R9M



2011_0901 unmount PC1114,PC1115 PC1118,PC1119

2011_0901 mount PC1140,PC1141 PC1142,PC1143

2011_0815 del PC1157

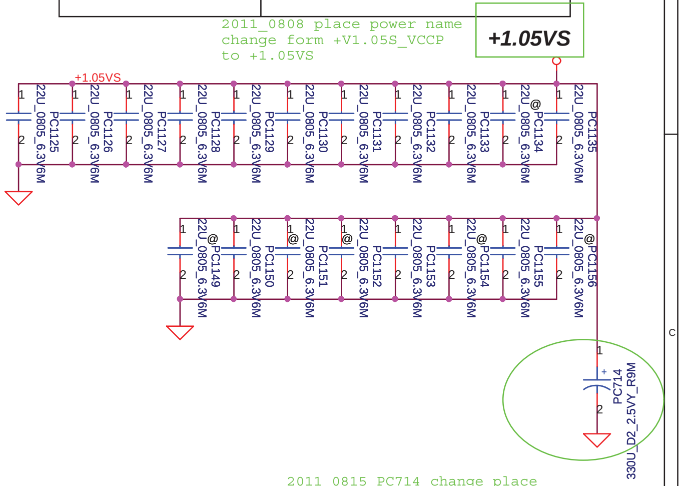
2011_0815 PC1160 change form unmount to mount

2011_07929 PC1158 non-mount

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

2011_0808 place power name change form +V1.05S_VCCP to +1.05VS



2011_0815 PC714 change place form "+1.05VS_VCCPP" to "+1.05VS"

2011_1005 PC714 change to 330uF_2V_R9M

2011_1007
PC714
form SGA00001Q802
(S POLY C 330U 2V M X LESR6M SX H1.9)
change to SGA00002680
(330U_D2_2.5VY_R9M)

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
PWR - PROCESSOR DECOUPLING

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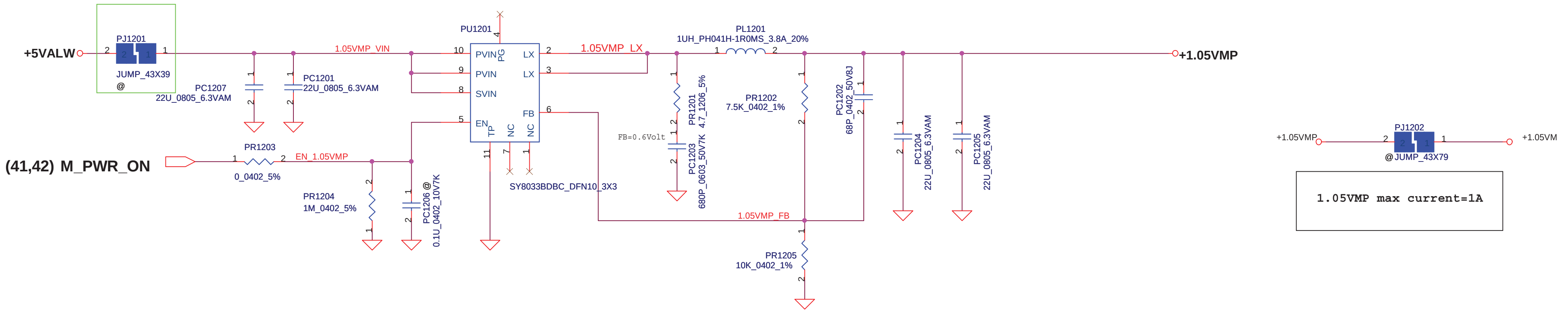

2011_0923 JUMP form 43X79 change to 43X79

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Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title

PWR-+1.05VMP

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Compal Electronics, Inc.

Title
PWR-Thermal Protect

Size
Document Number
LA-8131P
Rev
0.6

Date: Friday, January 06, 2012

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title
PIR (PWR)

Size: Custom
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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2011/09/13	No1		V	V	Add C2325,C2326,C2327,C2328,C2329,R2319,R2324,Q2312	Add SBA function (+3VM) power
	2011/09/15	No2		V		Del Q2305	Del SYSON#
	2011/09/15	No3		V		Add EC pin 119(M_PWR_ON) for SBA function	Add SBA function
	2011/09/15	No4		V		Add EC pin 120(PCH_SLPA#) from PCH to EC for SBA function	Add SBA function
	2011/09/15	No5		V		Add EC pin72 (Muxless_STAT) for GPU STAT	Add Muxless_STAT function
	2011/09/15	No6		V		Del PR310, PR311, PR312, PR313, net name:"H_PROCHOT#", +3VALW.	PWR-CHARGER-BQ24727
	2011/09/15	No7	V			mount PC832	
	2011/09/15	No8		V	V	Add R2482,Q2404,C2509,R2481,R2485,Q2400,R2483,C2501	AOAC Function
	2011/09/15	No9		V	V	change net name BT_OFF# to BT_ON# and change PCH EN GPIO from GPIO34 to GPIO36 R280 from @ to mount,R282 from mount to @	BT Function
	2011/09/15	No10		V	V	change net name(Mini-Express) from BT_OFF# to WLBT_OFF# PCH EN GPIO change to GPIO34	BT Function
	2011/09/19	No11		V	V	change +3VS_WLAN net name to +3VS_AOAC change +3VS_WWAN net name to +3VS_AOAC	AOAC Function
	2011/09/19	No12		V	V	Del R1010 for LVDS CONN plug high voltage	LVDS CONN
	2011/09/19	No13		V	V	R1102,R1104,R1105 from @ to mount fix MIC(ECR97236)issue	MIC function
	2011/09/19	No14		V	V	Add R2470 for 80 port function	80 port function
	2011/09/19	No15		V	V	Del R2476 Add Q2405	BT Function
	2011/09/20	No16		V	V	Add power schematic 9/15 again modify RF PC423, PC425, PC519, PC620, PC717, PC873, PC874, PC424, PC518 PC1017, PC1018, PC1019, PC422, PC516, PC517 modify POWER在VGA的PWM IC 加的零件PR869, PR870	
	2011/09/22	No17		V	V	Add U10,C589,C645 for TPM function	TPM function
	2011/09/22	No18		V	V	Add R110,R112 for SPI POWER choose(SBA function)	
	2011/09/23	No19		V	V	modify power page 44~57(PJ1201 JUMP form 43X79 change to 43X79)	
	2011/09/26	No20		V	V	change CPU footprint from TYCO_2013620-2_989P-T to TYCO_2013620-2_989P-T-A39 change PCH footprint from PANTHER-POINT_FCBGA_989P-T to PANTHER-POINT_FCBGA_989P-T-A39 change GPU footprint N13P-PES-A1_FCBGA_908P to N13P-PES-A1_FCBGA_908P-A39 change VRAM footprint K4W1G1646E-HC12_FBGA_96P to K4W1G1646E-HC12_FBGA_96P-A39	
	2011/09/26	No21		V	V	change PCH_GPIO24(R288) pull up to +3V_PCH	
	2011/09/26	No22		V		change P18 (R311,R330,R286,R329) for UMA and Optimus memon	
	2011/09/26	No23		V		change net name PCH_THRMTRIP#_R to VGA_THRMTRIP#	
	2011/09/26	No24		V	V	PQ702 change to TPC8065,Del PR705 PQ1001,PQ1002,PQ1005 change to TOC8065,Del PR1001,PR1002,PR1007	
	2011/09/26	No25		V	V	p43 change Q2304 dual channel 2n7002 to single channel Q2304,Q2305(Q2305 @) p43 change Q2306 dual channel 2n7002 to single channel Q2306,Q2311(Q2311 @)	
	2011/09/27	No27	V			modify EC Board ID R2213 to 18K	
	2011/09/27	No28		V	V	net name CX_GPIO0 connect to U1101 pin 38	
	2011/09/27	No29		V	V	Add C2152,C2153,D2113 for ESD	
	2011/09/27	No30		V	V	change NVIDIA N13M ROM_SCLK from 15K PU to 5K PU	
	2011/09/27	No31		V	V	change ESD part D2401,D2403,D2405 power from +5VALW to +USB VCCA	
	2011/09/27	No32		V	V	Add C2108 for GPU_CLKREQA	
	2011/09/27	No33				Add Q2406 , modify R2401,Change PCH_GPIO19 to ODD_DET#,for zero power ODD	
	2011/09/27	No34				change WLBT_OFF# to PCH_GPIO34	
	2011/09/27	No35				change PCH_GPIO34 to WLBT_OFF#(mini card pin5)	
	2011/09/27	No36				change BT_ON# connect to WLBT_OFF#(mini card pin51)	
	2011/09/28	No37				C76 , R1123 , c1131 , R2201,C2209 C84,C85 from @ to mount for RF team	
	2011/09/29	No38				R1529 change to 15K	
	2011/09/29	No39				Add CONN JDB3 fo debug	
	2011/09/29	No40				Add R2460,R2438,R2471,R2472,R2475,R2476 for PS8520B	
	2011/09/29	No41				change D2403 ,D2401 power to +USB_VCCB,and del D2403 ,D2401,D2405 Pin3 net	
	2011/09/29	No42				change power schematic del PC606 (22U_0805_6.3V6M) PR855.1 net change form +VGA_CORE to +VGA_COREP PR827 mount change to @(non-mount) PR839 for 47Kohm change to 147Kohm PR103 for 0ohm change to 270ohm PC1166 non-mount,PC1173 non-mount,PC1158 non-mount	
	2011/09/29	No43					
	2011/09/29	No44				Add Q2313,C2305,C2306,C2307,C2308,R2318,R2320,R2320,C2322 for +3V_PCH	
	2011/09/29	No45				change CRT CONN to DC061109231(footprint pin modify) Add PR954,PR955 Add H16,H27 change Q2304.Q2305 to Q2304 modify PTH H11,H18 ,H21 Del T10 for SUS_STAT(SLP_S3# 走不出來)	
	2011/10/04	No46				reserve R352,R353 for SATA re-drive PS-8131B change net name fron WLBT_OFF to WLBT_OFF_5# modify PCH_GPIO34 connect to BT_ON# for BT module modify PCH_GPIO36 from BT_ON# connect to WLBT_OFF_51# for mini card BT combo module changr Q2301 to 2N7002	
	2011/10/05	No47				Del R2469,T49,T45,T41,T37,T36,T28,T26 for ME 限高0 changer power net +3VS_FP to +3VS update power schematics P44~P57	
	2011/10/06	No48				change Q1202 part to SB000007H10. change JCARD1 PN to SP02000H810 footprint: ACES_87213-1400G_14P change some CONN part NO. for ME CONN list Add D2416	

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