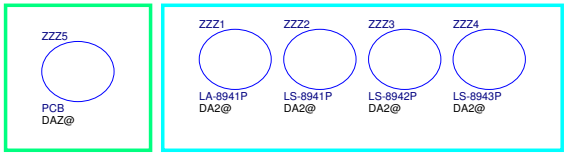
Compal Confidential

Model Name : Q1VZC
File Name :LA-8941P
BOM P/N:43



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Q1VZC M/B Schematics Document

Intel Sandy Bridge ULV Processor + Panther Point PCH

2012-04-19

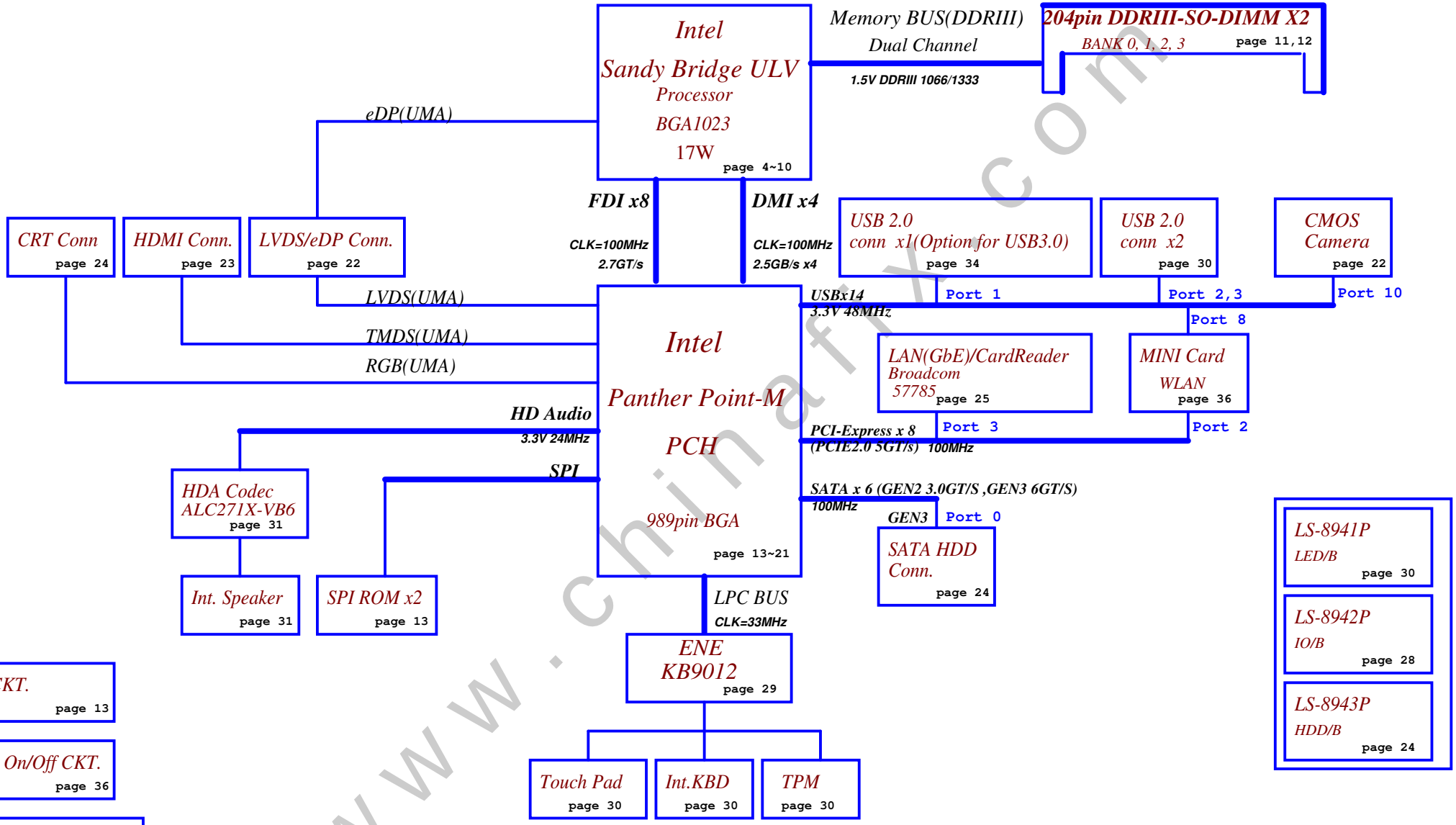
REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.		
Title: *Cover Page*		
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic	Rev: 1.0
Date: Friday, April 20, 2012	Sheet 1 of 45	

Compal Confidential

Model Name : Q1VZC
File Name :LA-8941P



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title: Block Diagrams			
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH (Short Jump)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VREF_SUS	+5VALW to +5VREF_SUS power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

PCH SM Bus address

Device			Address	
ChannelA	DIMM0	A0	1010 000X	JDIMM1(STD)
ChannelB	DIMM0	B0	1010 010X	JDIMM2(REV)

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Celeron 867	C867@
Pentium 977	P977@
Unpop	@
eDP Panel	EDP@
LVDS Panel	LVDS@
Connector	CONN@
USB3 Only	USB3@
Deep S3	DS3@
Normal S3	S3@
Intel i5/i7 CPU only	I57@
Celeron/Pentium/i3 CPU only	CP3@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	
		1	USB 2.0(Options for USB3.0)
	UHCI1	2	USB port(Left 2.0)
		3	USB Port(Left 2.0)
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	Camera
		11	
	UHCI6	12	
		13	

USB 3.0	Port	
XHCI	1	
	2	USB Port(Right 3.0)
	3	
	4	

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Issued Date	2011/11/22	Deciphered Date 2012/11/22	Title: Notes List

Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
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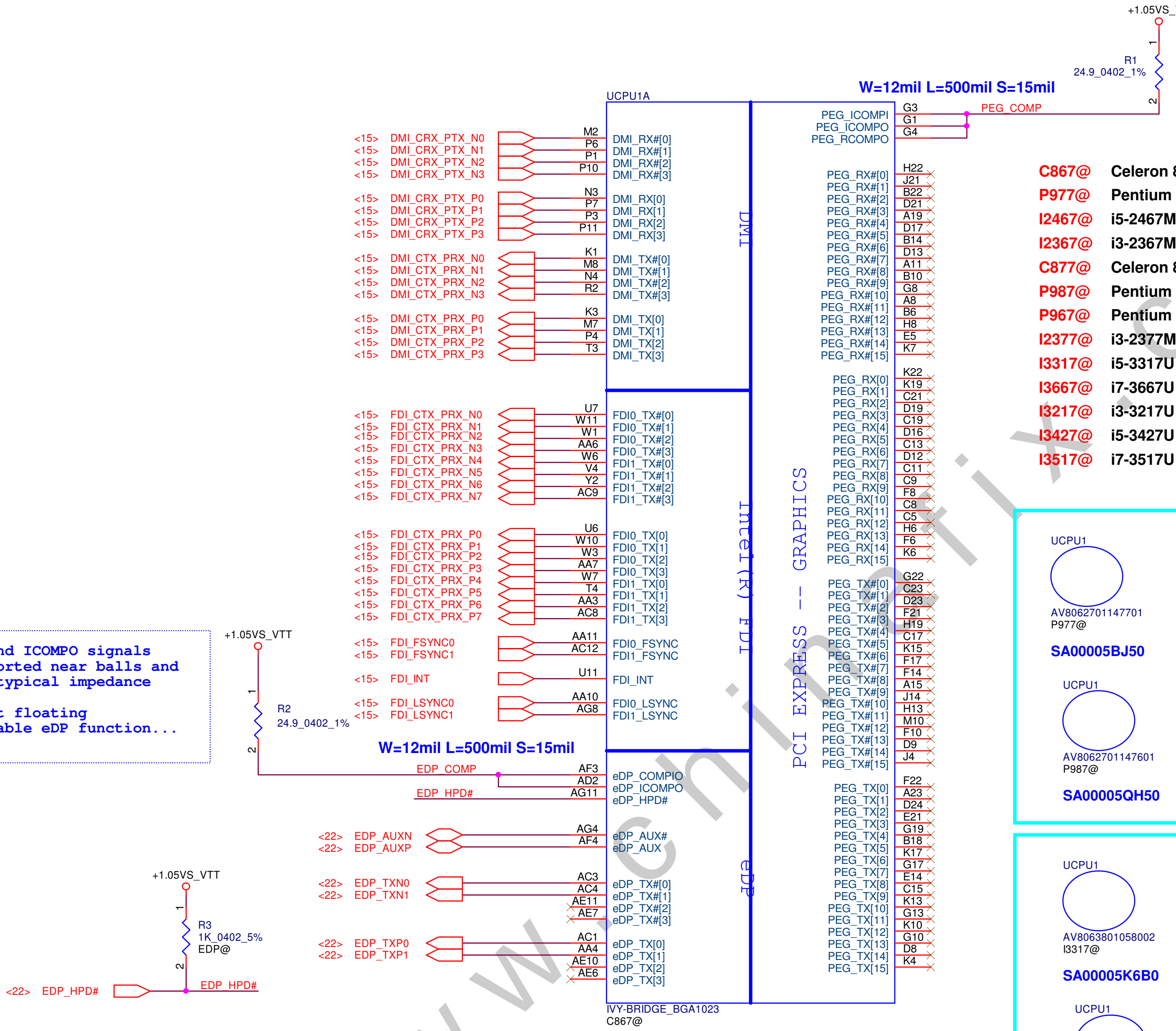
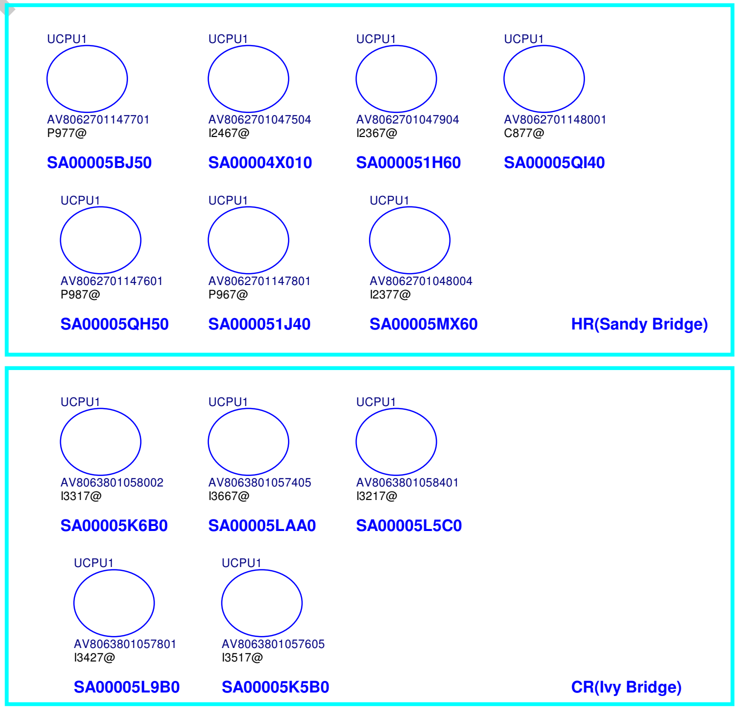
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms
can't be left floating
,even if disable eDP function...



+1.05VS_VTT
R1
24.9_0402_1%
W=12mil L=500mil S=15mil
PEG_COMP
UCPU1A
PEG_ICOMPI G3
PEG_ICOMPO G1
PEG_RCOMPO G4
<15> DMI_CRX_PTX_N0 M2 DMI_RX#[0]
<15> DMI_CRX_PTX_N1 P6 DMI_RX#[1]
<15> DMI_CRX_PTX_N2 P1 DMI_RX#[2]
<15> DMI_CRX_PTX_N3 P10 DMI_RX#[3]
<15> DMI_CRX_PTX_P0 N3 DMI_RX[0]
<15> DMI_CRX_PTX_P1 P7 DMI_RX[1]
<15> DMI_CRX_PTX_P2 P3 DMI_RX[2]
<15> DMI_CRX_PTX_P3 P11 DMI_RX[3]
<15> DMI_CTX_PRX_N0 K1 DMI_TX#[0]
<15> DMI_CTX_PRX_N1 M8 DMI_TX#[1]
<15> DMI_CTX_PRX_N2 N4 DMI_TX#[2]
<15> DMI_CTX_PRX_N3 R2 DMI_TX#[3]
<15> DMI_CTX_PRX_P0 K3 DMI_TX[0]
<15> DMI_CTX_PRX_P1 M7 DMI_TX[1]
<15> DMI_CTX_PRX_P2 P4 DMI_TX[2]
<15> DMI_CTX_PRX_P3 T3 DMI_TX[3]
DMI
<15> FDI_CTX_PRX_N0 U7 FDI0_TX#[0]
<15> FDI_CTX_PRX_N1 W11 FDI0_TX#[1]
<15> FDI_CTX_PRX_N2 W1 FDI0_TX#[2]
<15> FDI_CTX_PRX_N3 AA6 FDI0_TX#[3]
<15> FDI_CTX_PRX_N4 W6 FDI1_TX#[0]
<15> FDI_CTX_PRX_N5 V4 FDI1_TX#[1]
<15> FDI_CTX_PRX_N6 Y2 FDI1_TX#[2]
<15> FDI_CTX_PRX_N7 AC9 FDI1_TX#[3]
<15> FDI_CTX_PRX_P0 U6 FDI0_TX[0]
<15> FDI_CTX_PRX_P1 W10 FDI0_TX[1]
<15> FDI_CTX_PRX_P2 W3 FDI0_TX[2]
<15> FDI_CTX_PRX_P3 AA7 FDI0_TX[3]
<15> FDI_CTX_PRX_P4 W7 FDI1_TX[0]
<15> FDI_CTX_PRX_P5 T4 FDI1_TX[1]
<15> FDI_CTX_PRX_P6 AA3 FDI1_TX[2]
<15> FDI_CTX_PRX_P7 AC8 FDI1_TX[3]
<15> FDI_FSYNC0 AA11 FDI0_FSYNC
<15> FDI_FSYNC1 AC12 FDI1_FSYNC
<15> FDI_INT U11 FDI_INT
<15> FDI_LSYNC0 AA10 FDI0_LSYNC
<15> FDI_LSYNC1 AG8 FDI1_LSYNC
Intel(R) FDI
+1.05VS_VTT
R2
24.9_0402_1%
W=12mil L=500mil S=15mil
EDP_COMP AF3 eDP_COMPIO
AD2 eDP_ICOMPO
EDP_HPD# AG11 eDP_HPD#
<22> EDP_AUXN AG4 eDP_AUX#
<22> EDP_AUXP AF4 eDP_AUX
<22> EDP_TXN0 AC3 eDP_TX#[0]
<22> EDP_TXN1 AC4 eDP_TX#[1]
AE11 eDP_TX#[2]
AE7 eDP_TX#[3]
<22> EDP_TXP0 AC1 eDP_TX[0]
<22> EDP_TXP1 AA4 eDP_TX[1]
AE10 eDP_TX[2]
AE6 eDP_TX[3]
eDP
+1.05VS_VTT
R3
1K_0402_5%
EDP@
<22> EDP_HPD#
EDP_HPD#
PCI EXPRESS -- GRAPHICS
PEG_RX#[0] H22
PEG_RX#[1] J21
PEG_RX#[2] B22
PEG_RX#[3] D21
PEG_RX#[4] A19
PEG_RX#[5] D17
PEG_RX#[6] B14
PEG_RX#[7] D13
PEG_RX#[8] A11
PEG_RX#[9] B10
PEG_RX#[10] G8
PEG_RX#[11] A8
PEG_RX#[12] B6
PEG_RX#[13] H8
PEG_RX#[14] E5
PEG_RX#[15] K7
PEG_RX[0] K22
PEG_RX[1] K19
PEG_RX[2] C21
PEG_RX[3] D19
PEG_RX[4] C19
PEG_RX[5] D16
PEG_RX[6] C13
PEG_RX[7] D12
PEG_RX[8] C11
PEG_RX[9] C9
PEG_RX[10] F8
PEG_RX[11] C8
PEG_RX[12] C5
PEG_RX[13] H6
PEG_RX[14] F6
PEG_RX[15] K6
PEG_TX#[0] G22
PEG_TX#[1] C23
PEG_TX#[2] D23
PEG_TX#[3] F21
PEG_TX#[4] H19
PEG_TX#[5] C17
PEG_TX#[6] K15
PEG_TX#[7] F17
PEG_TX#[8] F14
PEG_TX#[9] A15
PEG_TX#[10] J14
PEG_TX#[11] H13
PEG_TX#[12] M10
PEG_TX#[13] F10
PEG_TX#[14] D9
PEG_TX#[15] J4
PEG_TX[0] F22
PEG_TX[1] A23
PEG_TX[2] D24
PEG_TX[3] E21
PEG_TX[4] G19
PEG_TX[5] B18
PEG_TX[6] K17
PEG_TX[7] G17
PEG_TX[8] E14
PEG_TX[9] C15
PEG_TX[10] K13
PEG_TX[11] G13
PEG_TX[12] K10
PEG_TX[13] G10
PEG_TX[14] D8
PEG_TX[15] K4
IVY-BRIDGE_BGA1023
C867@

C867@	Celeron 867	HR	1.3G	SA00005BH40(S IC AV8062701148901 SR0FK J1 1.3G ABO!)
P977@	Pentium 977	HR	1.4G	SA00005BJ50(S IC AV8062701147701 SR0FB J1 1.4G ABO!)
I2467@	i5-2467M	HR	1.6G	SA00004X010(S IC AV8062701047504 SR0D6 J1 1.6G ABO!)
I2367@	i3-2367M	HR	1.4G	SA000051H60(S IC AV8062701047904 SR0CV J1 1.4G ABO!)
C877@	Celeron 877	HR	1.4G	SA00005QI00(S IC AV8062701148001 QB35 J1 1.4G BGA)
P987@	Pentium 987	HR	1.5G	SA00005QH00(S IC AV8062701147601 QB31 J1 1.5G BGA)
P967@	Pentium 967	HR	1.3G	SA000051J40(S IC AV8062701147801 SR0FC J1 1.3G ABO!)
I2377@	i3-2377M	HR	1.5G	SA00005MX10(S IC AV8062701048004 QAXQ J1 1.5G BGA)
I3317@	i5-3317U	CR	1.7G	SA00005K650(S IC AV8063801058002 QC9E L1 1.7G BGA)
I3667@	i7-3667U	CR	2G	SA00005LA50(S IC AV8063801057405 QC9B L1 2G BGA 1023)
I3217@	i3-3217U	CR	1.8G	SA00005L530(S IC AV8063801058400 QC56 L0 1.8G ABO!)
I3427@	i5-3427U	CR	1.8G	SA00005L9A0(S IC AV8063801057801 SR0N7 L1 1.8G BGA)
I3517@	i7-3517U	CR	1.9G	SA00005K540(S IC AV8063801057605 QC9C L1 1.9G BGA)



UCPU1 AV8062701147701 P977@ SA00005BJ50
UCPU1 AV8062701047504 I2467@ SA00004X010
UCPU1 AV8062701047904 I2367@ SA000051H60
UCPU1 AV8062701148001 C877@ SA00005QI40
UCPU1 AV8062701147601 P987@ SA00005QH50
UCPU1 AV8062701147801 P967@ SA000051J40
UCPU1 AV8062701048004 I2377@ SA00005MX60
HR(Sandy Bridge)
UCPU1 AV8063801058002 I3317@ SA00005K6B0
UCPU1 AV8063801057405 I3667@ SA00005LAA0
UCPU1 AV8063801058401 I3217@ SA00005L5C0
UCPU1 AV8063801057801 I3427@ SA00005L9B0
UCPU1 AV8063801057605 I3517@ SA00005K5B0
CR(Ivy Bridge)

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Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: **PROCESSOR(1/7) DMI,FDI,PEG**

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev 1.0

Date: Friday, April 20, 2012 |

PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

Follow DG 1.5& Tacoma_Fall2 1.0
reserve
C65 2 @ 1 0.1U_0402_16V4Z H_CPUPWRGD
R6 2 1 10K_0402_5%

PROC_SELECT#
PH VCPLL and connect to PCH DF_TVS

偵測CPU有無安裝

XBOX 三紅功能

follow Checklist 1.5
+1.05VS_VTT R7 2 1 62_0402_5%
<29,35> H_PROCHOT# H_PROCHOT# R8 56_0402_5% H_PROCHOT_R

Follow DG 1.5 & Tacoma_Fall2 1.0
Buffered reset to CPU
+3VS C66 0.1U_0402_16V4Z
R14 0_0402_5% @
<17> PLT_RST# PLT_RST#
U1 NC A Y
BUFO_CPU_RST#
+1.05VS_VTT R12 75_0402_5% R15 43_0402_1%
BUF_CPU_RST#
SN74LVC1G07DCKR_SC70-5

Use open drain logic gate:
+1.05VS_VTT PU pop 75ohm
series resister pop 43ohm

RESET#:都ok後請CPU做reset

Follow DG 1.5 & Tacoma_Fall2 1.0
+3VALW C67 0.1U_0402_16V4Z
U2
<15> SYS_PWROK
<15> PM_DRAM_PWRGD
MC74VHC1G09DFT2G_SC70-5
PM_SYS_PWRGD_BUF
+1.5V_CPU_VDDQ R16 200_0402_5%
R18 130_0402_5% PM_DRAM_PWRGD_R

Use open drain logic gate:
+1.5V_CPU_VDDQ PU pop 200ohm
series resister pop 130ohm

C476 @ 180P_0402_50V8J H_CPUPWRGD_R
12/22 Add(ESD request)

UCPU1B
F49 PROC_SELECT#
C57 PROC_DETECT#
C49 CATERR#
A48 PECI
C45 PROCHOT#
D45 THERMTRIP#
C48 PM_SYNC
B46 UNCOREPWRGOOD
BE45 SM_DRAMPWROK
D44 RESET#
IVY-BRIDGE_BGA1023
C867@

MISC THERMAL PWR MANAGEMENT

<18> H_CPUPWRGD R13 0_0402_5% H_CPUPWRGD_R
UNCOREPWRGOOD:非CORE外的電OK
PM_DRAM_PWRGD_R
SM_DRAMPWROK:DRAM power ok
BUF_CPU_RST#

CLOCKS
BCLK J3 H2 CLK_CPU_DMI <14> CLK_CPU_DMI# <14>
DPLL_REF_CLK AG3 AG1 CLK_CPU_DPLL CLK_CPU_DPLL# <14>

SM_RCOMP0,SM_RCOMP1
W=20mil L=500mil S=13mil

SM_RCOMP2
W=15mil L=500mil S=13mil

DDR3 MISC
SM_DRAMRST# AT30 SM_DRAMRST# SM_DRAMRST# <6>
SM_RCOMP[0] BF44 SM_RCOMP0 R9 2 1 140_0402_1%
SM_RCOMP[1] BE43 SM_RCOMP1 R10 2 1 25.5_0402_1%
SM_RCOMP[2] BG43 SM_RCOMP2 R11 2 1 200_0402_1%
DDR3 Compensation Signals

JTAG & BPM
PRDY# N53
PREQ# N55
TCK L56 XDP_TCK @ PAD T2
TMS L55 XDP_TMS @ PAD T3
TRST# J58 XDP_TRST# @ PAD T4
TDI M60 XDP_TDI @ PAD T5
TDO L59 XDP_TDO @ PAD T6
DBR# K58 XDP_DBRESET# XDP_DBRESET# <15>
BPM#[0] G58
BPM#[1] E55
BPM#[2] E59
BPM#[3] G55
BPM#[4] G59
BPM#[5] H60
BPM#[6] J59
BPM#[7] J61

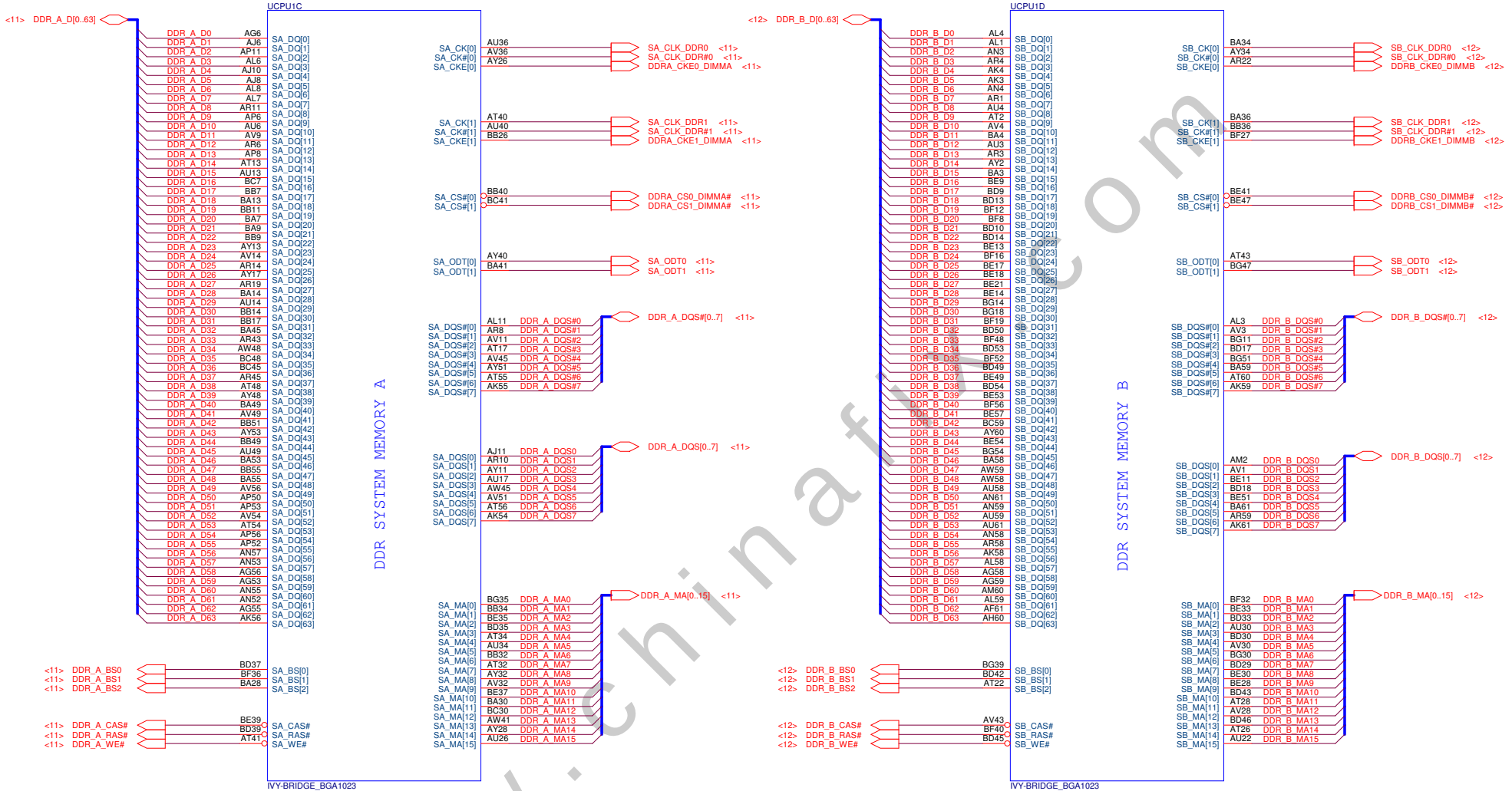
0921 LVDS@->@
+1.05VS_VTT
CLK_CPU_DPLL# R4 2 LVDS@ 1 1K_0402_5%
CLK_CPU_DPLL R5 2 LVDS@ 1 1K_0402_5%

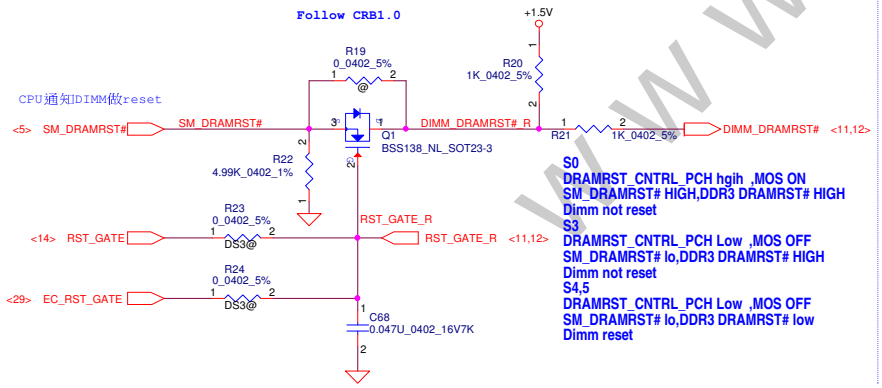
Checklist1.5 P.67 Graphis Disable Guide
eDP disable:
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PU 1K_5% to +1.05VS_VTT

+3VS
XDP_DBRESET# R17 2 1 1K_0402_5%
Tacoma_Fall2 1.0 PU 1K +3VS
Check list 1.5 PU 1K +3VS
Debug port DG1.1-1.3 50~5K ohm

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.
Title: PROCESSOR(3/7) DDRIII
Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0
Date: Friday, April 20, 2012 | Sheet 5 of 45

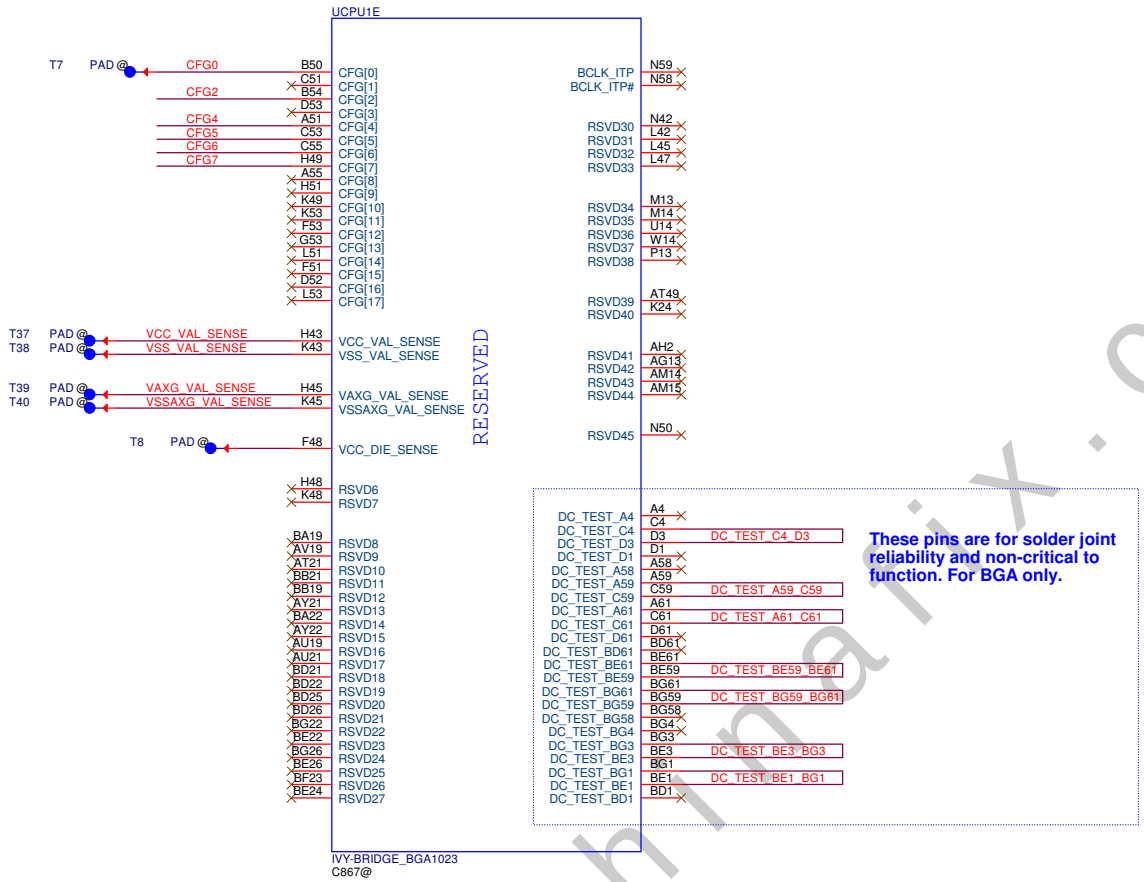




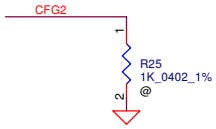
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title	PROCESSOR(3/7) DDRIII		
Size	Document Number		Rev
Custom	Q1VZC M/B LA-8941P Schematic		1.0
Date: Friday, April 20, 2012	Sheet 6 of 45		

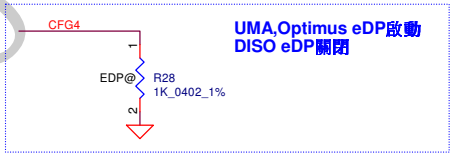
CFG Straps for Processor



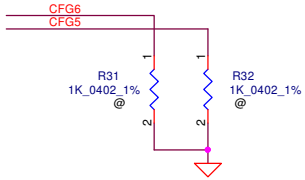
These pins are for solder joint reliability and non-critical to function. For BGA only.



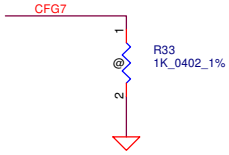
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



eDP enable	
CFG4	* 1:Disable 0:Enable



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) 1x16 PCI Express *10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	Tacoma_Fall2 1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title	PROCESSOR(4/7) RSVD,CFG		
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 7 of 45		

POWER

ULV type
DC 33A

8.5A

UCPU1F

+CPU_CORE

INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at P.51

CORE SUPPLY

VCC[1] A26
VCC[2] A29
VCC[3] A31
VCC[4] A34
VCC[5] A35
VCC[6] A38
VCC[7] A39
VCC[8] A42
VCC[9] C26
VCC[10] C27
VCC[11] C32
VCC[12] C34
VCC[13] C37
VCC[14] C39
VCC[15] C42
VCC[16] D27
VCC[17] D32
VCC[18] D34
VCC[19] D37
VCC[20] D39
VCC[21] D42
VCC[22] E26
VCC[23] E28
VCC[24] E32
VCC[25] E34
VCC[26] E37
VCC[27] E38
VCC[28] F25
VCC[29] F26
VCC[30] F28
VCC[31] F29
VCC[32] F32
VCC[33] F34
VCC[34] F37
VCC[35] F38
VCC[36] F42
VCC[37] G42
VCC[38] H25
VCC[39] H26
VCC[40] H28
VCC[41] H29
VCC[42] H32
VCC[43] H34
VCC[44] H35
VCC[45] H37
VCC[46] H38
VCC[47] H40
VCC[48] J25
VCC[49] J26
VCC[50] J28
VCC[51] J29
VCC[52] J32
VCC[53] J34
VCC[54] J35
VCC[55] J37
VCC[56] J38
VCC[57] J40
VCC[58] J42
VCC[59] K26
VCC[60] K27
VCC[61] K29
VCC[62] K32
VCC[63] K34
VCC[64] K35
VCC[66] K37
VCC[67] K39
VCC[68] K42
VCC[69] L25
VCC[70] L28
VCC[71] L33
VCC[72] L36
VCC[73] L40
VCC[74] N26
VCC[75] N30
VCC[76] N34
N38

PEG IO AND DDR IO

+1.05VS_VTT

For DDR

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at P.51

VCCIO[1] AF46
VCCIO[3] AG48
VCCIO[4] AG50
VCCIO[5] AG51
VCCIO[6] AJ17
VCCIO[7] AJ21
VCCIO[8] AJ25
VCCIO[9] AJ43
VCCIO[10] AJ47
VCCIO[11] AK50
VCCIO[12] AK51
VCCIO[13] AL14
VCCIO[14] AL15
VCCIO[15] AL16
VCCIO[16] AL20
VCCIO[17] AL22
VCCIO[18] AL26
VCCIO[19] AL45
VCCIO[20] AL48
VCCIO[21] AM16
VCCIO[22] AM17
VCCIO[23] AM21
VCCIO[24] AM43
VCCIO[25] AM47
VCCIO[26] AN20
VCCIO[27] AN42
VCCIO[28] AN45
VCCIO[29] AN48

For PEG

VCCIO[30] AA14
VCCIO[31] AA15
VCCIO[32] AB17
VCCIO[33] AB20
VCCIO[34] AC13
VCCIO[35] AD16
VCCIO[36] AD18
VCCIO[37] AD21
VCCIO[38] AE14
VCCIO[39] AE15
VCCIO[40] AF16
VCCIO[41] AF18
VCCIO[42] AF20
VCCIO[43] AG15
VCCIO[44] AG16
VCCIO[45] AG17
VCCIO[46] AG20
VCCIO[47] AG21
VCCIO[48] AJ14
VCCIO[49] AJ15

+1.05VS_VTT
VCCIO50 W16
VCCIO51 W17

+3VS
R34 10K_0402_5% @
VCCIO_SEL
R35 10K_0402_5% @

VCCIO_SEL after Ivy bridge ES2 Voltage support	
BC22 *	1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

VCCIO_SEL
BC22 VCCIO_SEL

QUIET RAILS

+1.05VS_VTT
VCCPQE[1] AM25
VCCPQE[2] AN22
C69 1U_0402_6.3V6K

+1.05VS_VTT
R36 130_0402_5%

+1.05VS_VTT
R37 75_0402_5%

Place the PU resistors close to CPU

SVID

VIDALERT# A44 H_CPU_SVIDALRT# R38 43_0402_1% SVID_ALERT# <41>
VIDSCLK B43 H_CPU_SVIDCLK R39 0_0402_5% SVID_CLK <41>
VIDSOUT C44 H_CPU_SVIDDAT R40 0_0402_5% SVID_DATA <41>

+CPU_CORE
R41 100_0402_1%

Place the PU resistors close to VR

SENSE LINES

VCC_SENSE F43 VCCSENSE_R R42 0_0402_5% VCCSENSE <41>
VSS_SENSE G43 VSSSENSE_R R43 0_0402_5% VSSSENSE <41>

R44 10_0402_5% +1.05VS_VTT
VCCIO_SENSE AN16 VCCIO_SENSE <40>
VSS_SENSE_VCCIO AN17 VSSIO_SENSE
R46 10_0402_5%

R45 100_0402_1%

Should change to connect form power cirucit & layout differential with VCCIO_SENSE.

Check list 1.5

IVY-BRIDGE_BGA1023
C867@

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

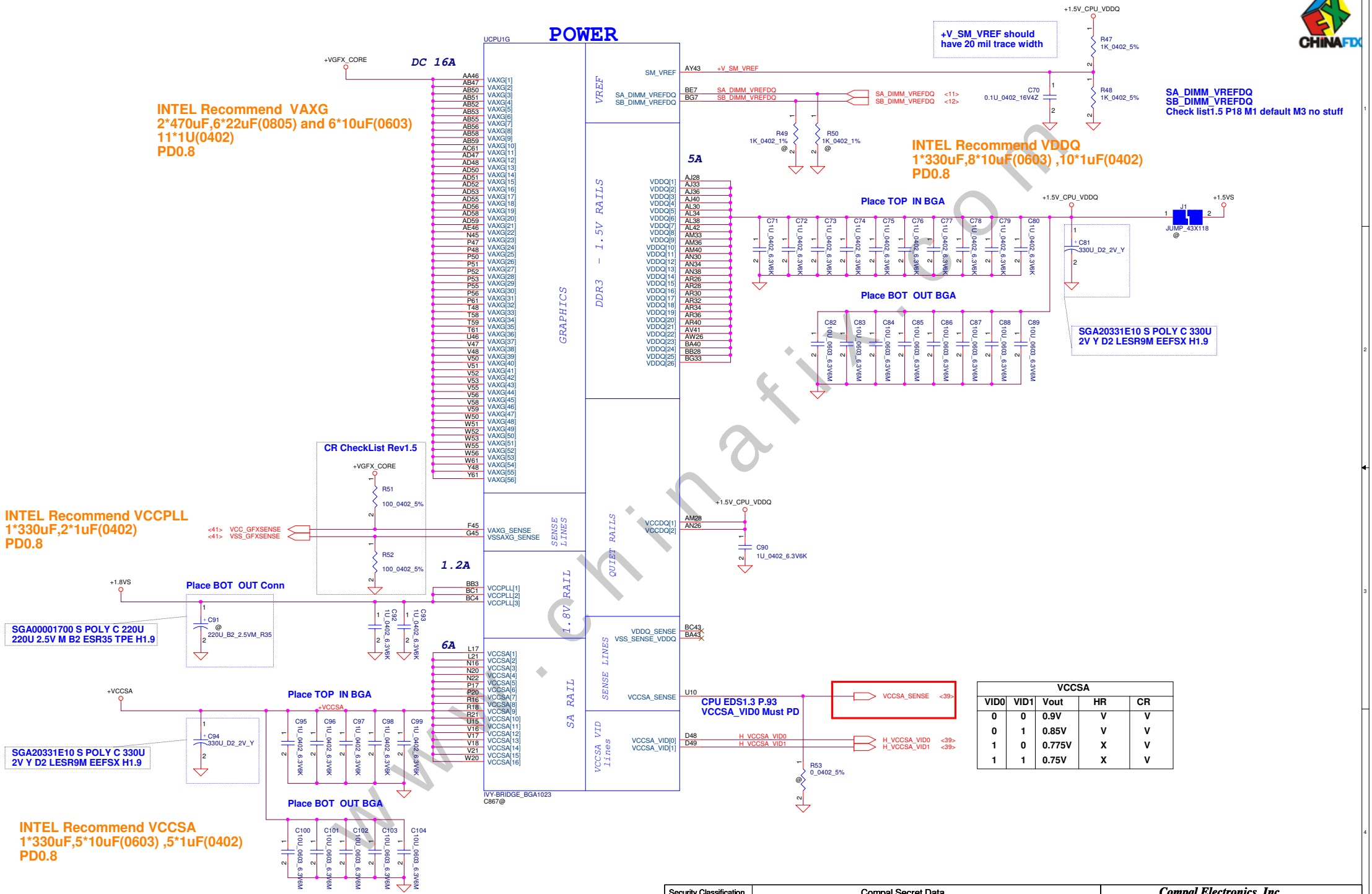
Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size	Document Number	Rev
Custom	Q1VZC M/B LA-8941P Schematic	1.0

Date: Friday, April 20, 2012 Sheet 8 of 45

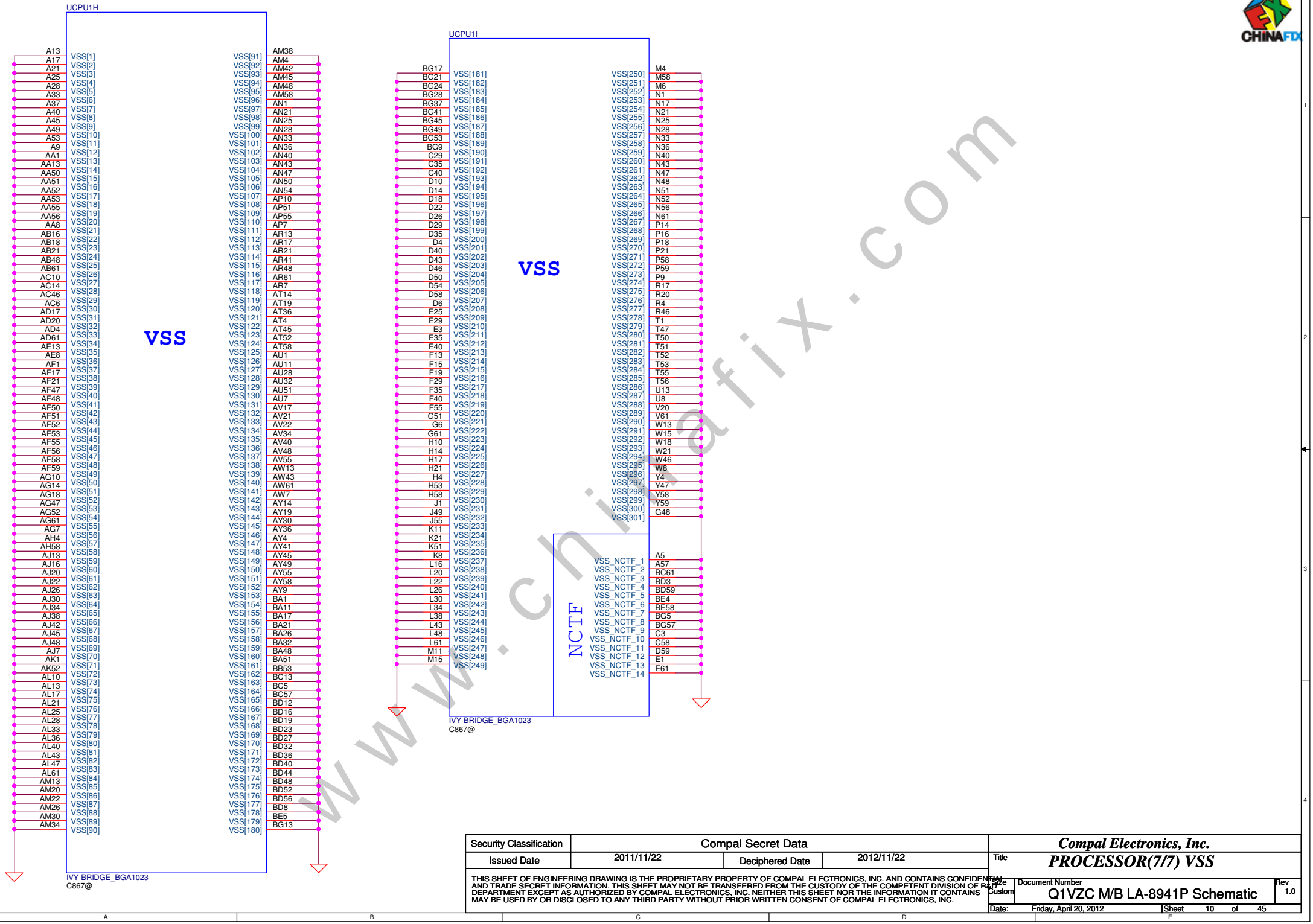
POWER



VCCSA				
VID0	VID1	Vout	HR	CR
0	0	0.9V	V	V
0	1	0.85V	V	V
1	0	0.775V	X	V
1	1	0.75V	X	V

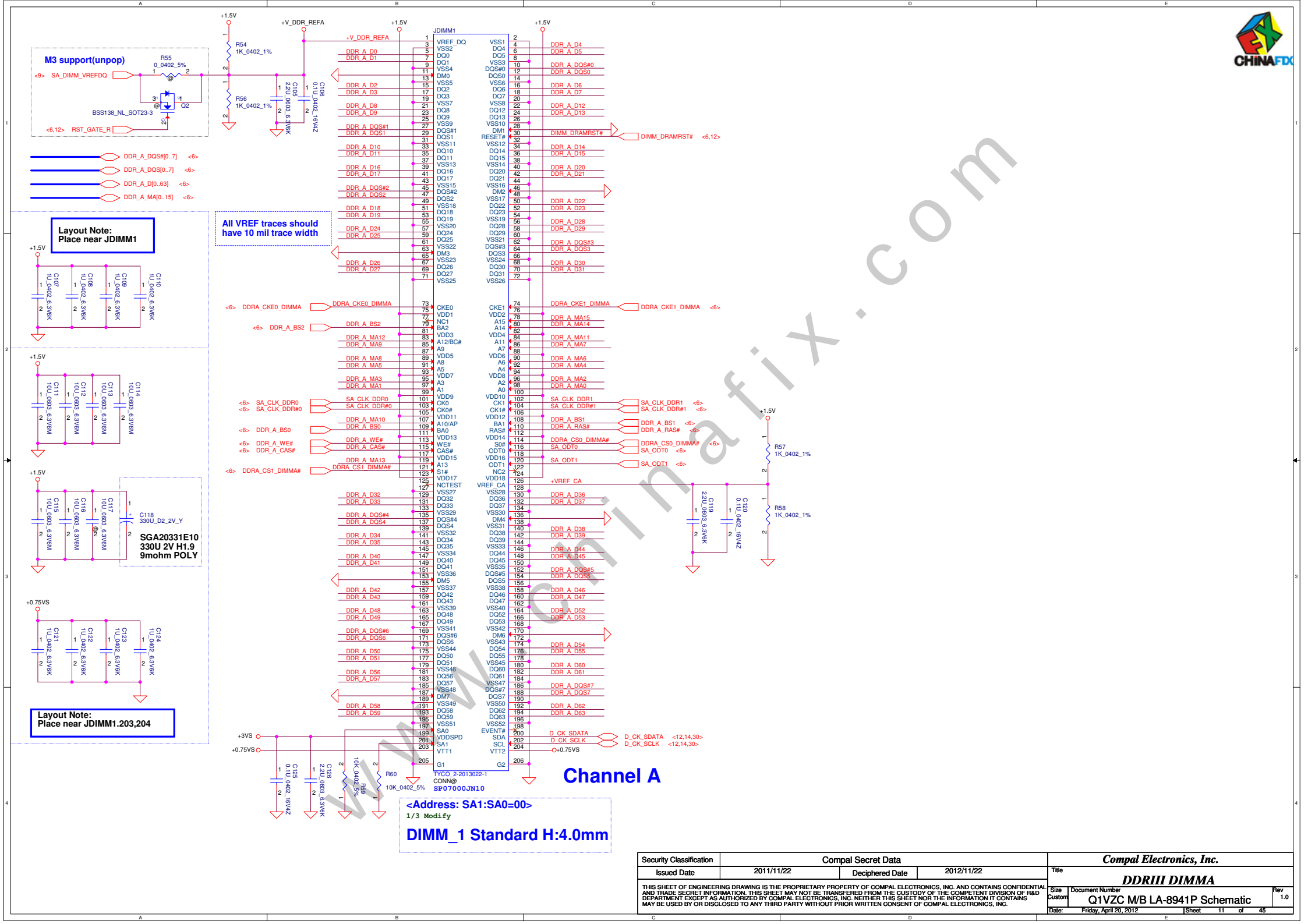
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title	PROCESSOR(6/7) PWR		
Size	Document Number		Rev
Custom	Q1VZC M/B LA-8941P Schematic		1.0
Date:	Friday, April 20, 2012	Sheet 9 of 45	



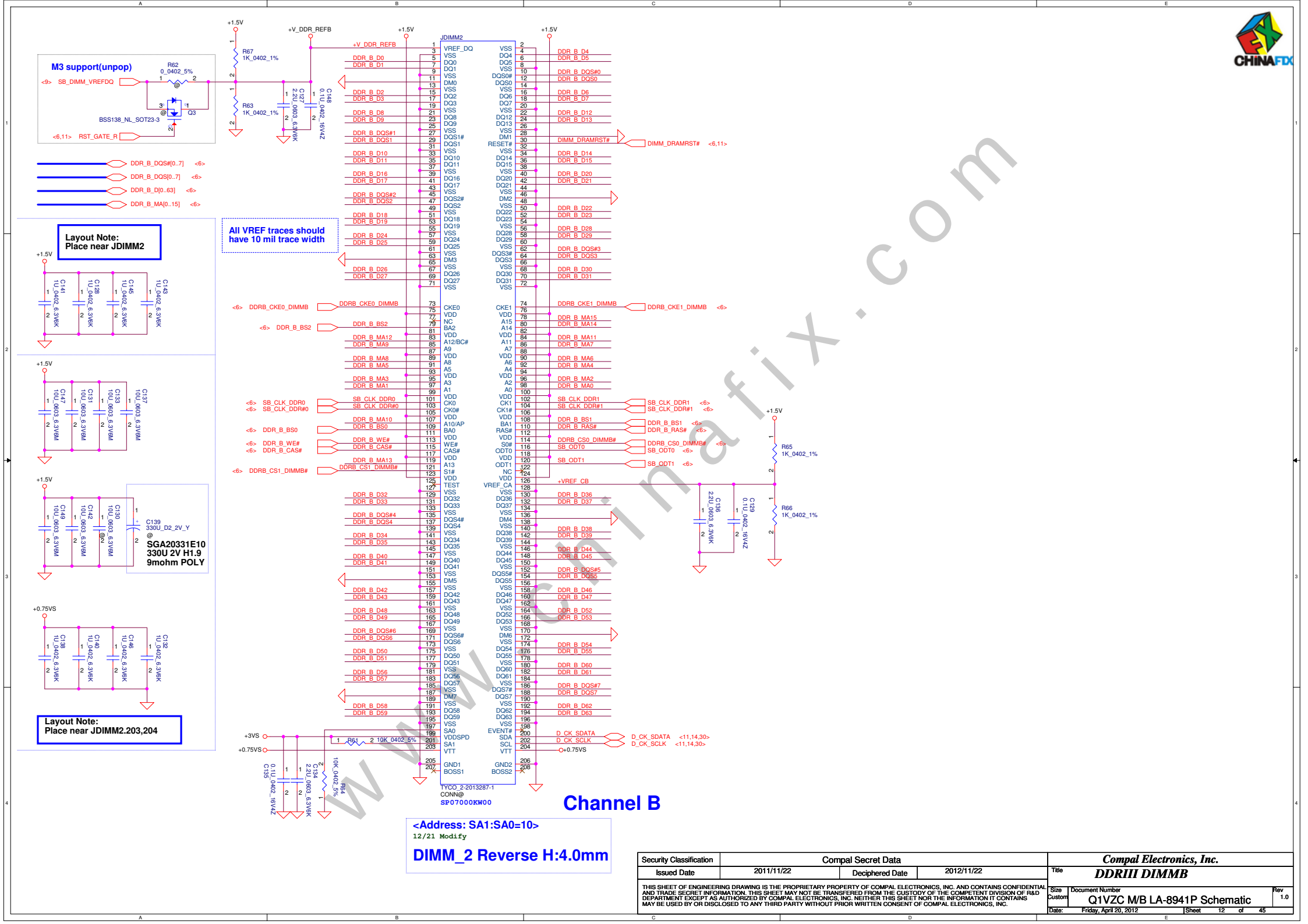
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title	PROCESSOR(7/7) VSS		
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 10 of 45		



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title	DDRIII DIMMA		
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 11 of 45		



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title	DDRIII DIMMB		
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 12 of 45		

RTCRST close RAM door J1

+RTCVCC
C163 1U_0603_10V6K
R74 0_0603_5%
R75 20K_0402_5%
R76 20K_0402_5%
PCH_RTCRST#
PCH_SRTCRST#
C164 1U_0603_10V6K
R77 0_0603_5%

+RTCVCC
R78 1M_0402_5% SM_INTRUDER#
R79 330K_0402_5% PCH_INTVRMEN

INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

+3VS
R82 1K_0402_5% PCH_SPKR
HIGH= Enable (No Reboot)Disable TCO timer system reboot feature
★ LOW= Disable (Default internal PD)

+VCCSUS3_3
R84 1K_0402_5%
R83 0_0402_5%
HDA_SDOUT_PCH
<29> HDA_SDO

HDA_SDO
ME debug mode,this signal has a weak internal PD
★ Low = Disable (Default)
High = Enabled [Flash Descriptor Security Overide]

+VCCSUS3_3
R87 1K_0402_5% HDA_SYNC_PCH
This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
★1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

<31> HDA_BITCLK_AUDIO R88 33_0402_5% HDA_BITCLK_PCH
<31> HDA_SYNC_AUDIO R89 33_0402_5% HDA_SYNC_PCH_R
<31> HDA_RST_AUDIO# R92 33_0402_5% HDA_RST_PCH#
<31> HDA_SDOUT_AUDIO R95 33_0402_5% HDA_SDOUT_PCH

PCH_RTCX1
PCH_RTCX2
R107 10M_0402_5%
Y1 32.768KHZ_12.5PF_1TJF125DP1A000D
18P_0402_50V8J C167
C168 18P_0402_50V8J

U16 3/7 Add
BD82HM70
HM70@
SA00005MQ60

11/30 Add (EMI request)
HDA_BITCLK_AUDIO
C467 22P_0402_50V8J @

Prevent back drive issue.
+5VS
Q4 BSS138_NL_SOT23-3
HDA_SYNC_PCH
R90 0_0402_5%
R93 1M_0402_5%

U16A

PCH_RTCX1	A20	RTCX1	RTC	FWH0 / LAD0	C38 LPC_AD0
PCH_RTCX2	C20	RTCX2		FWH1 / LAD1	A38 LPC_AD1
PCH_RTCRST#	D20	RTCRST#		FWH2 / LAD2	B37 LPC_AD2
PCH_SRTCRST#	G22	SRTCRST#		FWH3 / LAD3	C37 LPC_AD3
SM_INTRUDER#	K22	INTRUDER#		FWH4 / LFRAME#	D36 LPC_FRAME#
PCH_INTVRMEN	C17	INTVRMEN		LDRQ0#	E36
				LDRQ1# / GPIO23	K36 PCH_GPIO23
				SERIRQ	V5 SERIRQ
HDA_BITCLK_PCH	N34	HDA_BCLK	IHDA		
HDA_SYNC_PCH	L34	HDA_SYNC			
<31> PCH_SPKR	T10	SPKR			
HDA_RST_PCH#	K34	HDA_RST#			
<31> HDA_SDIN0	E34	HDA_SDIN0			
	G34	HDA_SDIN1			
	C34	HDA_SDIN2			
	A34	HDA_SDIN3			
HDA_SDOUT_PCH	A36	HDA_SDO			
	C36	HDA_DOCK_EN# / GPIO33			
	N32	HDA_DOCK_RST# / GPIO13			
PCH_JTAG_TCK	J3	JTAG_TCK	JTAG		
PCH_JTAG_TMS	H7	JTAG_TMS			
PCH_JTAG_TDI	K5	JTAG_TDI			
PCH_JTAG_TDO	H1	JTAG_TDO			
PCH_SPI_CLK	T3	SPI_CLK	SPI		
PCH_SPI_CS0#	Y14	SPI_CS0#			
PCH_SPI_CS1#	T1	SPI_CS1#			
PCH_SPI_MOSI	V4	SPI_MOSI			
PCH_SPI_MISO	U3	SPI_MISO			
			SATA	SATA0RXN / SATA0RXP / SATA0TXN / SATA0TXP	AM3 AM1 AP7 AP5
				SATA1RXN / SATA1RXP / SATA1TXN / SATA1TXP	AM10 AM8 AP11 AP10
				SATA2RXN / SATA2RXP / SATA2TXN / SATA2TXP	AD7 AD5 AH5 AH4
				SATA3RXN / SATA3RXP / SATA3TXN / SATA3TXP	AB8 AB10 AF3 AF1
				SATA4RXN / SATA4RXP / SATA4TXN / SATA4TXP	Y7 Y5 AD3 AD1
				SATA5RXN / SATA5RXP / SATA5TXN / SATA5TXP	Y3 Y1 AB3 AB1
				SATAICOMPO	Y11
				SATAICOMPI	Y10
				SATA3RCOMPO	AB12
				SATA3COMPI	AB13
				SATA3RBIAS	AH1
				SATALED#	P3 PCH_SATALED#
				SATA0GP / GPIO21	V14 PCH_GPIO21
				SATA1GP / GPIO19	P1 PCH_GPIO19

COUGARPOINT_FCBGA989
HM77@

HDD1
SATA_PRX_DTX_N0 <24>
SATA_PRX_DTX_P0 <24>
SATA_PTX_DRX_N0 <24>
SATA_PTX_DRX_P0 <24>

12/1 Del

HM70 not support
SATA for port1/port3

SATA_COMP R94 37.4_0402_1% +1.05VS_VTT
SATA3_COMP R97 49.9_0402_1% +1.05VS_VTT
RBIAS_SATA3 R99 750_0402_1%
L=500mil S=15mil
L=500mil S=15mil

No use PU 10K +3VS
GPIO19 has internal Pull up

+RTCBATT
20mil
D1 BAS40-04_SOT23-3
+RTCVCC
20mil
+CHGRTC
C165 0.1U_0402_16V4Z
20mil

SERIRQ R80 10K_0402_5%
PCH_SATALED# R81 10K_0402_5%

+3VS
R230 10K_0402_5%
PCH_GPIO23
R234 1K_0402_5% @
R85 10K_0402_5%
PCH_GPIO21
R86 10K_0402_5% @

R102 4.7K_0402_5%
PCH_GPIO19
Debug Port DG 1.2 PU 4.7K +3VS

PCH_SPI_CLK_2 R96 33_0402_5%
PCH_SPI_CLK_1 R98 33_0402_5%
PCH_SPI_CS0#_1 R100 33_0402_5%
PCH_SPI_CS1#_2 R101 33_0402_5%
PCH_SPI_MOSI_2 R103 33_0402_5%
PCH_SPI_MOSI_1 R104 33_0402_5%
PCH_SPI_MISO_1 R105 33_0402_5%
PCH_SPI_MISO_2 R106 33_0402_5%

+3VS
R109 3.3K_0402_5% SPI_WP1#
R108 3.3K_0402_5% SPI_HOLD1#
U17 MX25L3206EM2I-12G_SO8 SA000041P00
SPI ROM FOR ME (4MB)
Footprint 200mil

12/7 Change symbol of U18 from SA00000XT00 to SA000041O00
+3VS
R111 3.3K_0402_5% SPI_WP2#
U18 MX25L8006EM2I-12G_SO8 SA000041O00
R112 3.3K_0402_5%
SPI ROM FOR ME (1MB)
Footprint 200mil

Reserve for EMI
PCH_SPI_CLK R110 33_0402_5% C166 10P_0402_50V8J
11/30 Add
PCH_SPI_CLK_1 R466 33_0402_5% 22P_0402_50V8J C465
PCH_SPI_CLK_2 R467 33_0402_5% 22P_0402_50V8J C466

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

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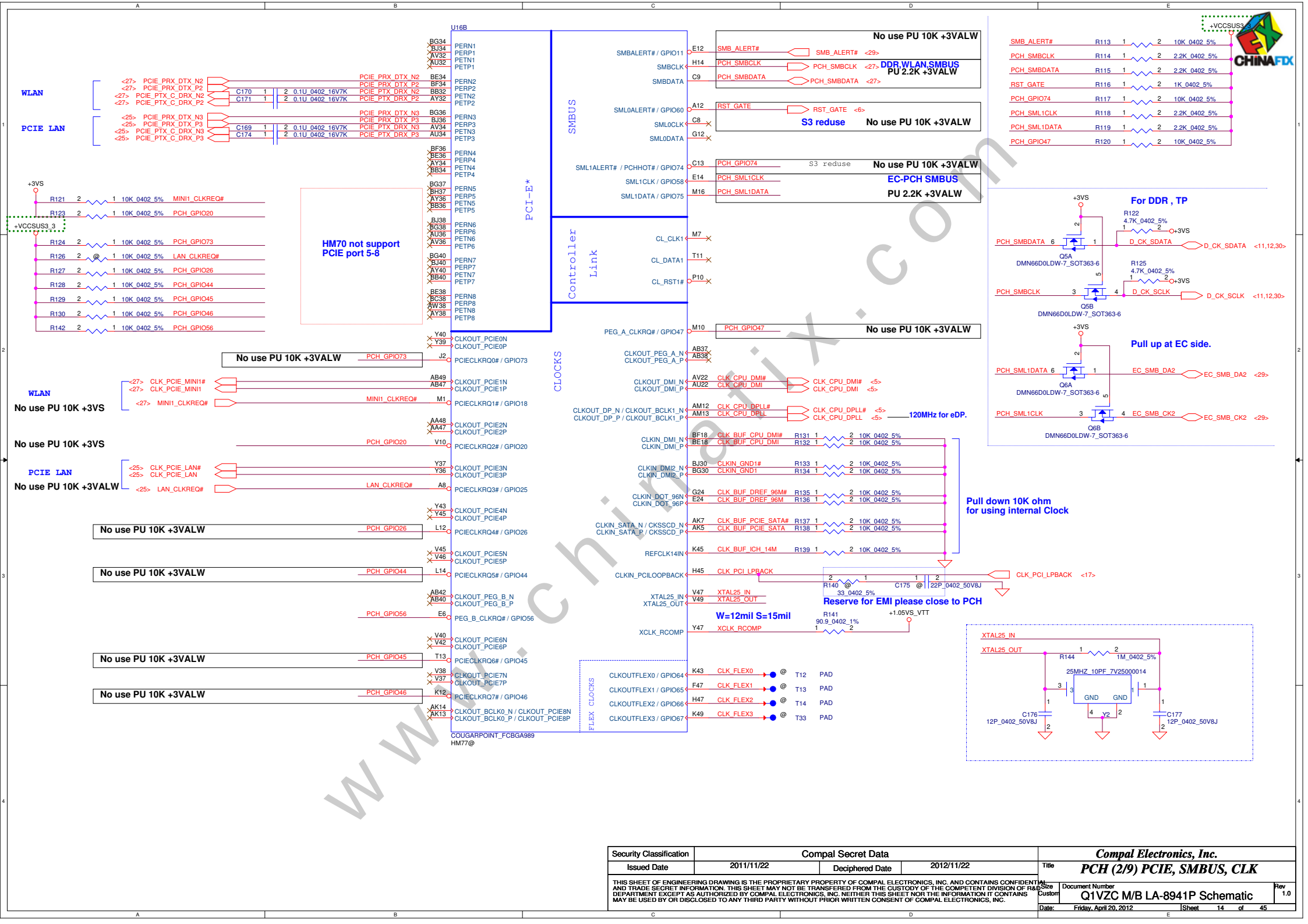
Compal Electronics, Inc.
Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0
Date: Friday, April 20, 2012 | Sheet 13 of 45



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Issued Date	2011/11/22	Deciphered Date	2012/11/22

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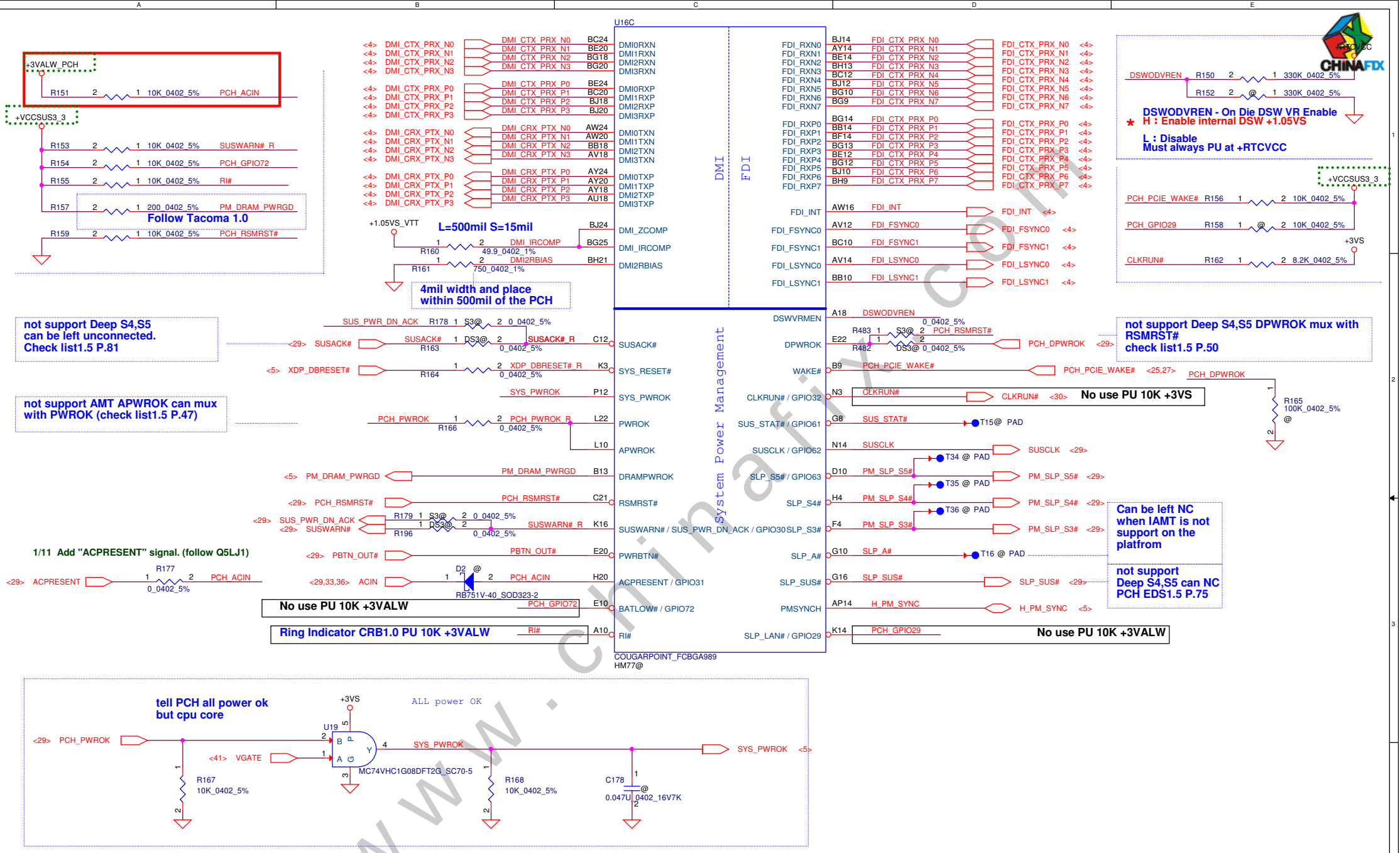
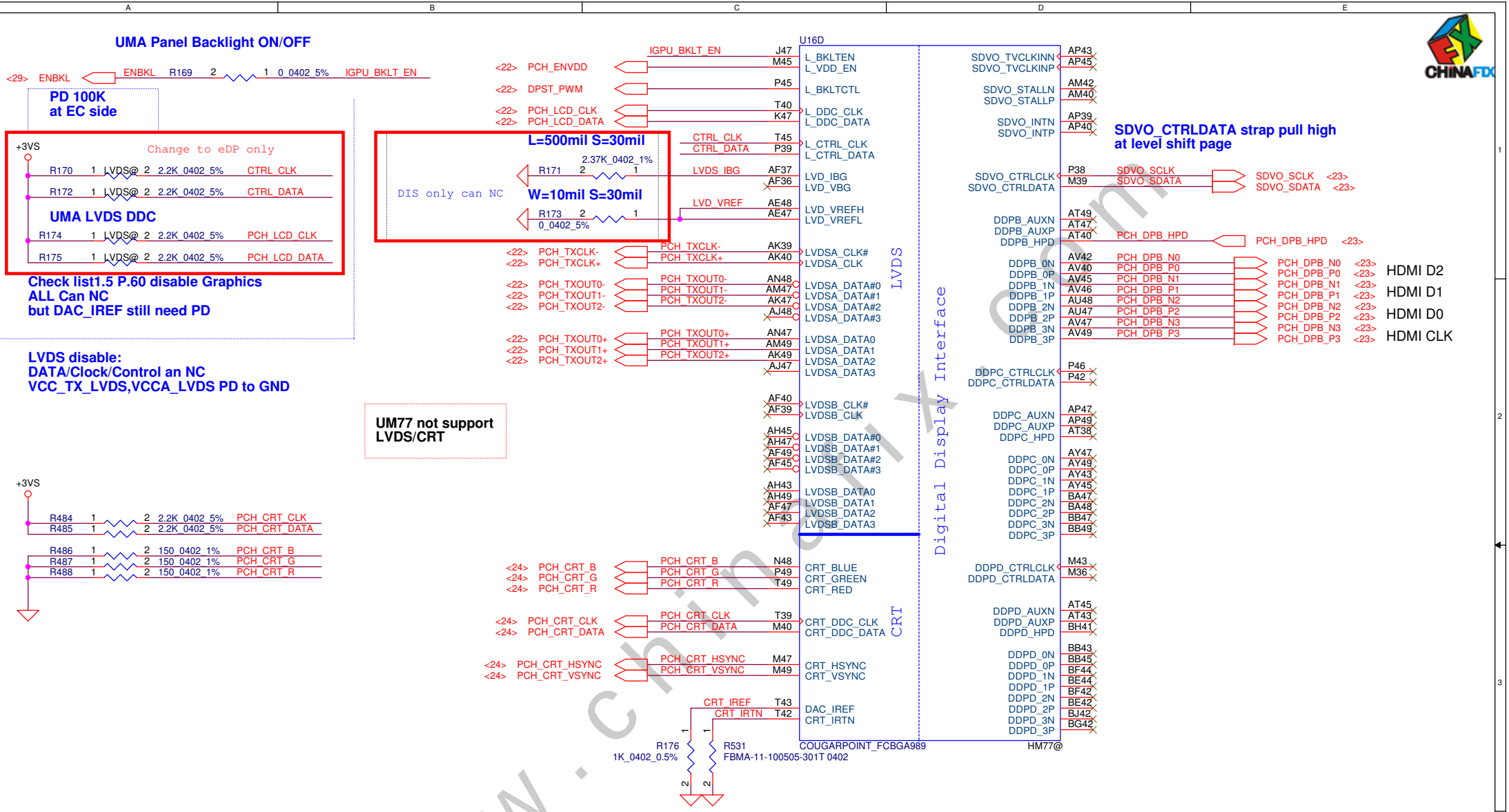
Compal Electronics, Inc.	
Title	PCH (2/9) PCIE, SMBUS, CLK
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic
Rev: 1.0	
Date: Friday, April 20, 2012	Sheet 14 of 45



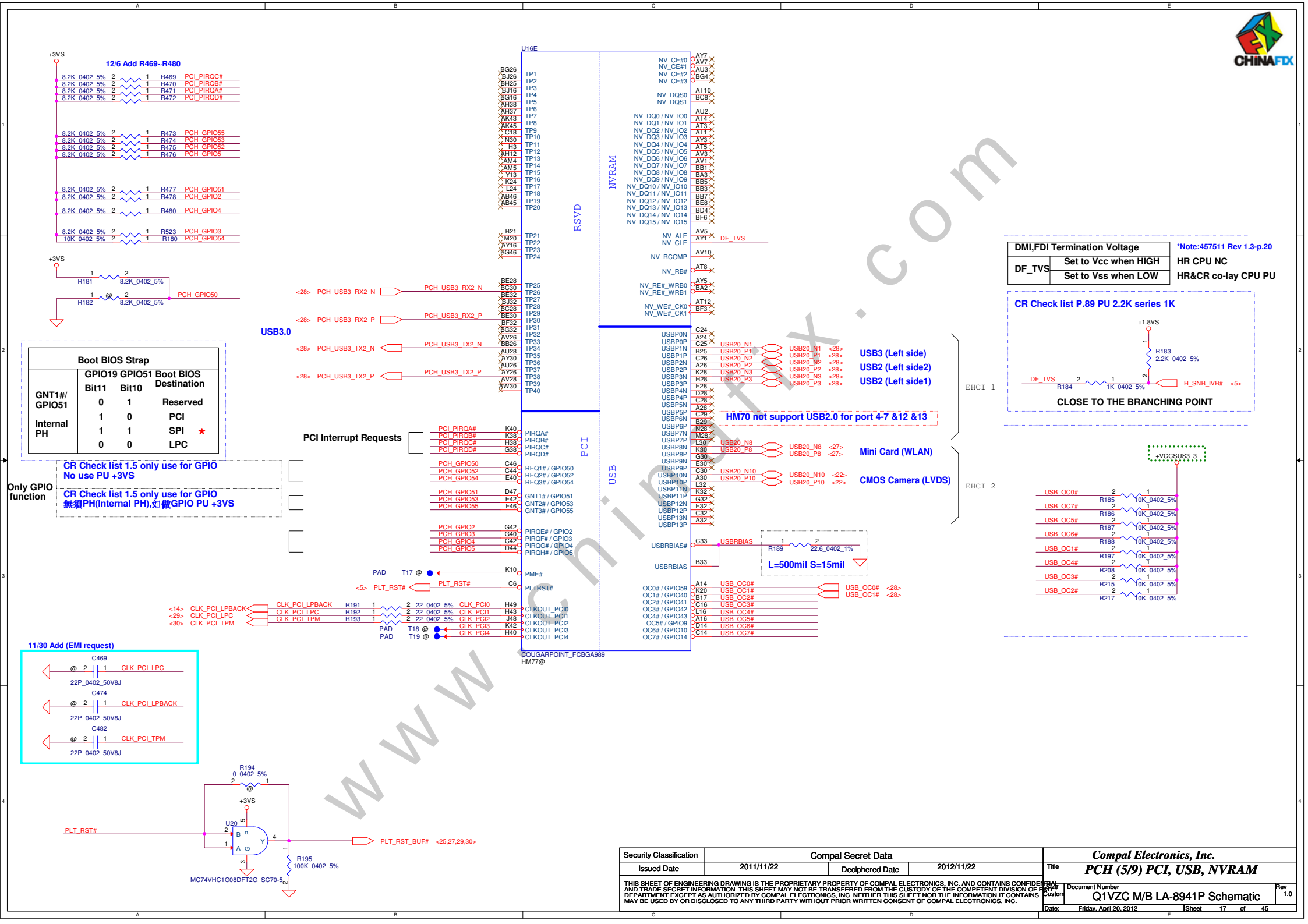
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title	PCH (3/9) DMI,FDI,PM		
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 15 of 45		



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title	PCH (4/9) LVDS,CRT,DP,HDMI		
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 16 of 45		



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 17 of 45

HDA_SYNC PH(PLL =+1.5VS)

GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up

★ H : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+VCCSUS3_3
R202 4.7K_0402_5%
PCH_GPIO28
R205 1K_0402_5%
Debug Port DG 1.2 PU 4.7K +3VALW_PCH

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal

R209 @ 10K_0402_5% PCH_GPIO27

+3VS
R211 200K_0402_5% PCH_GPIO36
+3VALW_PCH
R214 @ 1K_0402_5% EC_SMI#

SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down.
(weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

+3VS
R216 10K_0402_5% PCH_GPIO0
R218 10K_0402_5% PCH_GPIO1
R219 10K_0402_5% PCH_GPIO6
R220 10K_0402_5% PCH_GPIO16
R221 10K_0402_5% PCH_GPIO17
R522 10K_0402_5% PCH_GPIO38
12/13 Add
R222 10K_0402_5% PCH_GPIO34
R223 10K_0402_5% PCH_GPIO48
R225 10K_0402_5% PCH_GPIO49

+VCCSUS3_3
R227 10K_0402_5% PCH_GPIO12
R228 1K_0402_5% EC_LID_OUT#
R232 10K_0402_5% PCH_GPIO57

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.
CRB1.0 PU 10K to +3VALW

+VCCSUS3_3
R224 10K_0402_5% PCH_GPIO24
R226 @ 10K_0402_5%

Fan Tachometer Inputs
TACH1~7 only on server
can insted to GPIO

11/21 EDP@->POP

LVDS/eDP	GPIO71
LVDS	1
eDP	0

+3VS
R198 10K_0402_5% LVDS@ PCH_GPIO71
R201 10K_0402_5% EDP@
R199 10K_0402_5% @ PCH_GPIO69
R203 10K_0402_5%
R200 10K_0402_5%@ PCH_GPIO70
R204 10K_0402_5%

U16F

No use PU 10K +3VS	PCH_GPIO0	T7	BMBUSY# / GPIO0
No use PU 10K +3VS	PCH_GPIO1	A42	TACH1 / GPIO1
No use PU 10K +3VS	PCH_GPIO6	H36	TACH2 / GPIO6
No use PU 10K +3VS <29> EC_SCI#	EC_SCI#	E38	TACH3 / GPIO7
No use PU 10K +3VALW <29> EC_SMI#	EC_SMI#	C10	GPIO8
No use PU +3VALW	PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12
No use PU +3VALW <29> EC_LID_OUT#	EC_LID_OUT#	G2	GPIO15
No use PU +3VS	PCH_GPIO16	U2	SATA4GP / GPIO16
No use PU +3VS	PCH_GPIO17	D40	TACH0 / GPIO17
No use PU 10K +3VS RAM flag	PCH_GPIO22	T5	SCLOCK / GPIO22
No use PU +3VALW DDR3/DDR3L	PCH_GPIO24	E8	GPIO24 / MEM_LED
No use PD 10K to GND	PCH_GPIO27	E16	GPIO27
No use PU 10K +3VALW	PCH_GPIO28	P8	GPIO28
No use PU 10K +3VS BT ON/OFF	PCH_GPIO34	K1	STP_PCI# / GPIO34
No use can NC PAD T20 @	PCH_GPIO35	K4	GPIO35
Can't PU	PCH_GPIO36	V8	SATA2GP / GPIO36
Can't PU PAD T21 @	PCH_GPIO37	M5	SATA3GP / GPIO37
No use PU 10K +3VS	PCH_GPIO38	N2	SLOAD / GPIO38
No use PU 10K +3VS RAM flag	PCH_GPIO39	M3	SDATAOUT0 / GPIO39
No use PU 10K +3VS	PCH_GPIO48	V13	SDATAOUT1 / GPIO48
SATA5GP&TEMP_ALERT# CRB PU 10K +3VS	PCH_GPIO49	V3	SATA5GP / GPIO49
No use PU +3VALW	PCH_GPIO57	D6	GPIO57

GPIO

TACH4 / GPIO68	C40	PCH_GPIO68	
TACH5 / GPIO69	B41	PCH_GPIO69	
TACH6 / GPIO70	C41	PCH_GPIO70	
TACH7 / GPIO71	A40	PCH_GPIO71	

CPU/MISC

A20GATE	P4	GATEA20 <29>	
PECI	AU16	PCH_PECI_R 0_0402_5% R207	H_PECI <5,29>
RCIN#	P5	EC_KBRST#	EC_KBRST# <29>
PROCPWRGD	AY11		H_CPUPWRGD <5>
THRMTRIP#	AY10	PCH_THRMTRIP#_R R210 390_0402_5%	H_THRMTRIP# <5>
INIT3_3V#	T14		

+3VS
R206 10K_0402_5%

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130c shut down

INIT3_3V Checklist1.5 P.69
This signal has weak internal PU, can't pull low,leave NC

NC_1	AH8	
NC_2	AK11	
NC_3	AH10	
NC_4	AK10	
NC_5	P37	

TS_VSS1~4
PD to GND

+3VS
EC_KBRST# R212 10K_0402_5%
PCH_GPIO68 R213 10K_0402_5%

NCTF

VSS_NCTF_1	A4	VSS_NCTF_15	BG2
VSS_NCTF_2	A44	VSS_NCTF_16	BG48
VSS_NCTF_3	A45	VSS_NCTF_17	BH3
VSS_NCTF_4	A46	VSS_NCTF_18	BH47
VSS_NCTF_5	A5	VSS_NCTF_19	BJ4
VSS_NCTF_6	A6	VSS_NCTF_20	BJ44
VSS_NCTF_7	B3	VSS_NCTF_21	BJ45
VSS_NCTF_8	B47	VSS_NCTF_22	BJ46
VSS_NCTF_9	BD1	VSS_NCTF_23	BJ5
VSS_NCTF_10	BD49	VSS_NCTF_24	BJ6
VSS_NCTF_11	BE1	VSS_NCTF_25	C2
VSS_NCTF_12	BE49	VSS_NCTF_26	C48
VSS_NCTF_13	BF1	VSS_NCTF_27	D1
VSS_NCTF_14	BF49	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

COUGARPOINT_FCBGA989
HM77@

9/15 Layout request remove Test point They will route by itself

9/15 Layout request remove Test point They will route by itself

+3VS
R229 10K_0402_5% PCH_GPIO39
R233 10K_0402_5% @
R231 10K_0402_5% PCH_GPIO22
R235 10K_0402_5% @

GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When uses as SATA2GP/SATA3GP for mechanical presence detect
-use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check list page 47

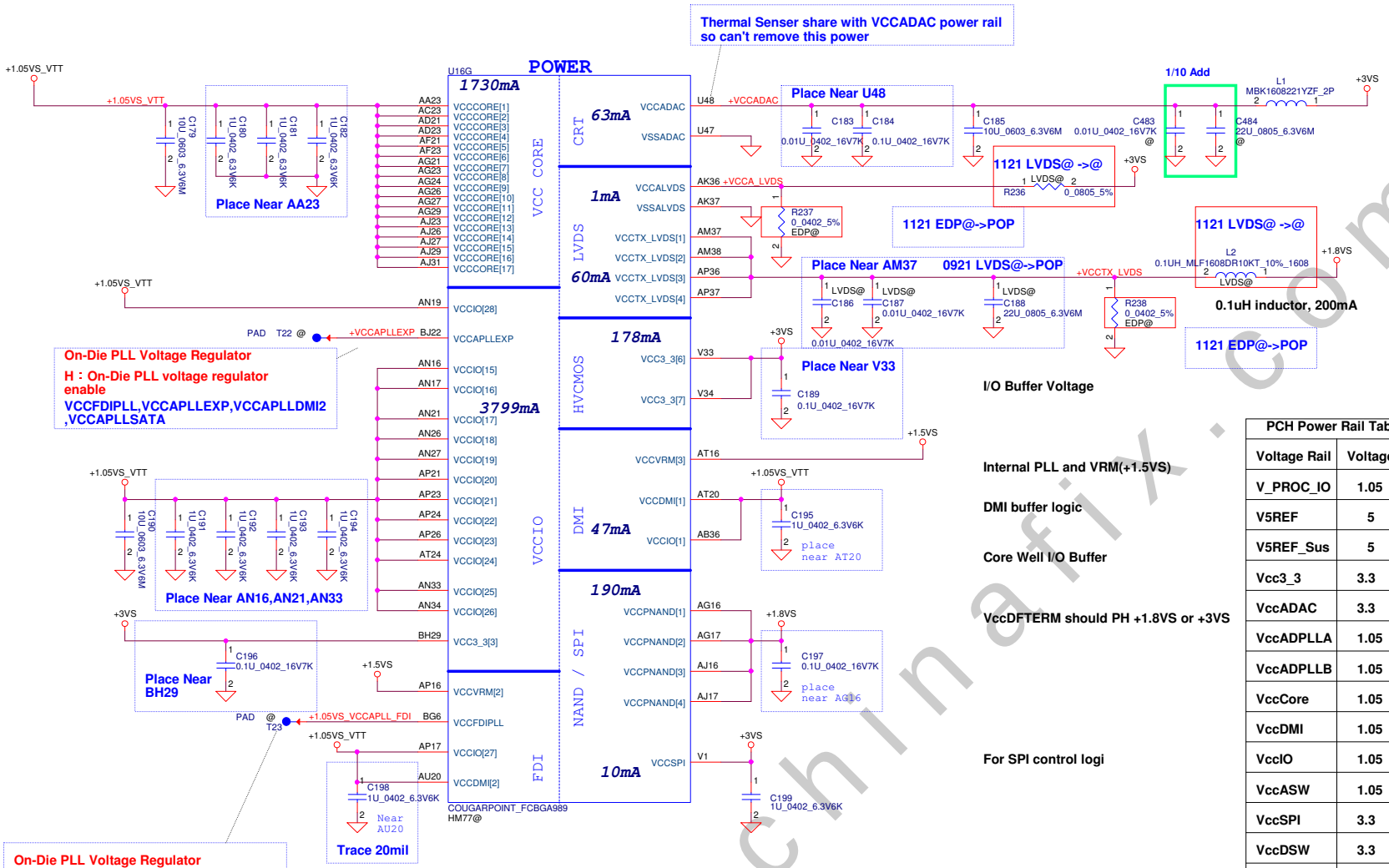
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

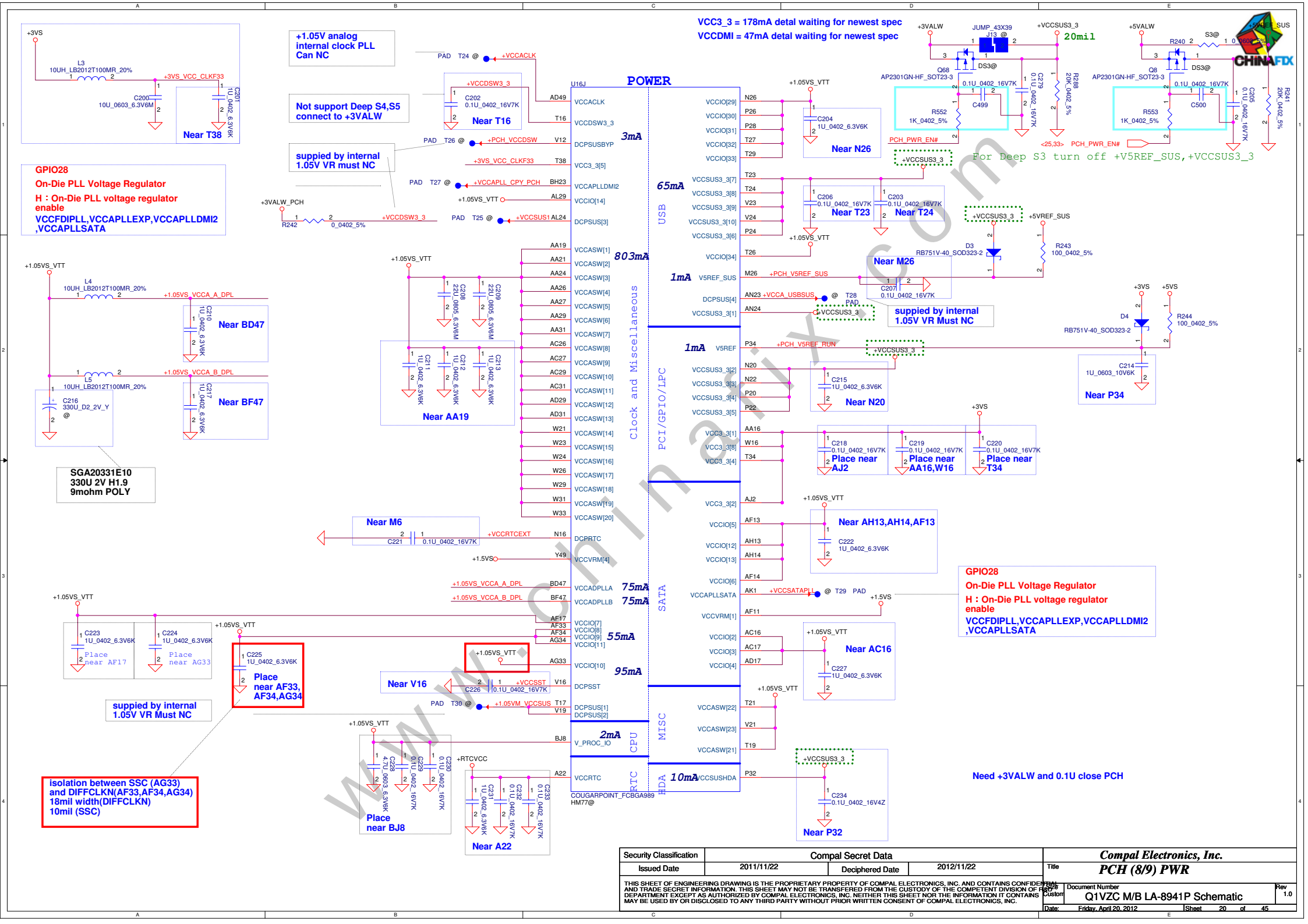
Date: Friday, April 20, 2012 | Sheet 18 of 45

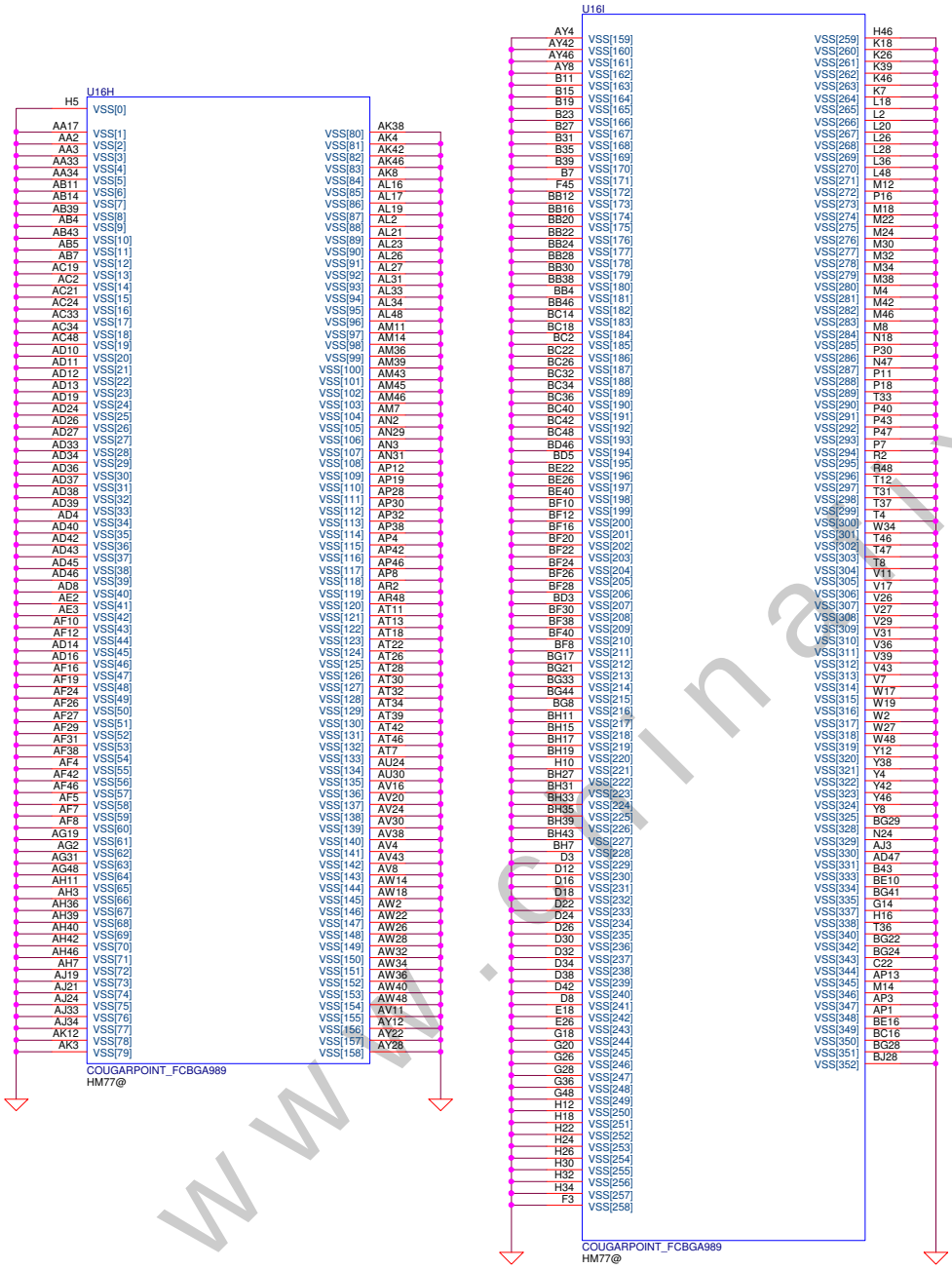


PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.002	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.178	I/O Buffer Voltage
VccADAC	3.3	0.063	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.075	Display PLL A power
VccADPLLB	1.05	0.075	Display PLL B power
VccCore	1.05	1.73	Internal Logic Voltage
VccDMI	1.05	0.047	DMI Buffer Voltage
VccIO	1.05	3.799	Core Well I/O buffers
VccASW	1.05	0.803	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.01	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.065	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title	PCH (7/9) PWR		
Size	Document Number		Rev
Custom	Q1VZC M/B LA-8941P Schematic		1.0
Date:	Friday, April 20, 2012	Sheet	19 of 45

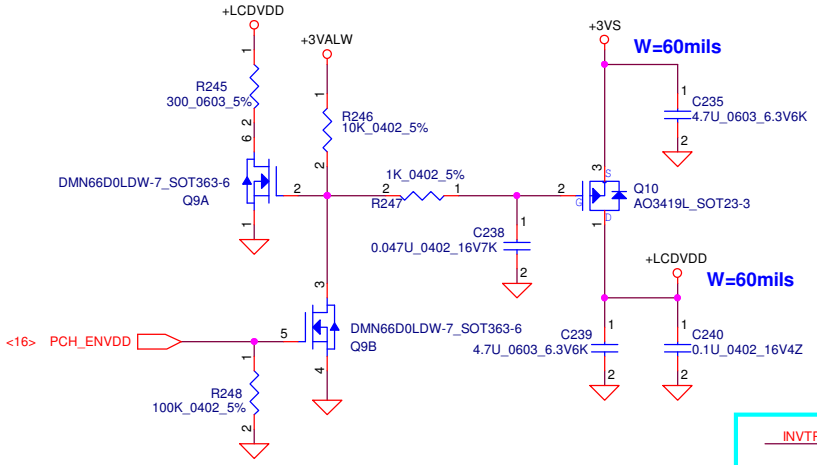


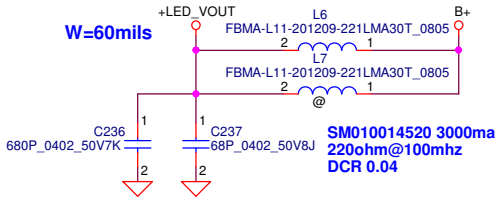


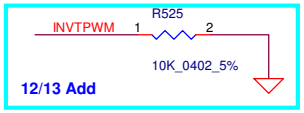
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

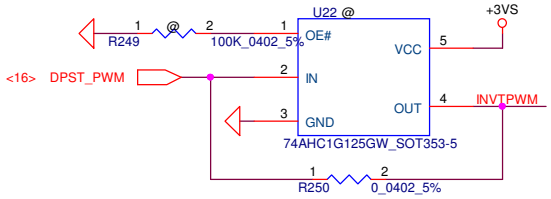
Compal Electronics, Inc.			
Title: PCH (9/9) VSS			
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 21 of 45		

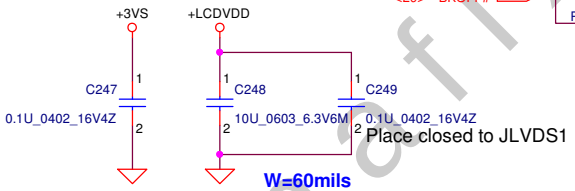
LCD POWER CIRCUIT



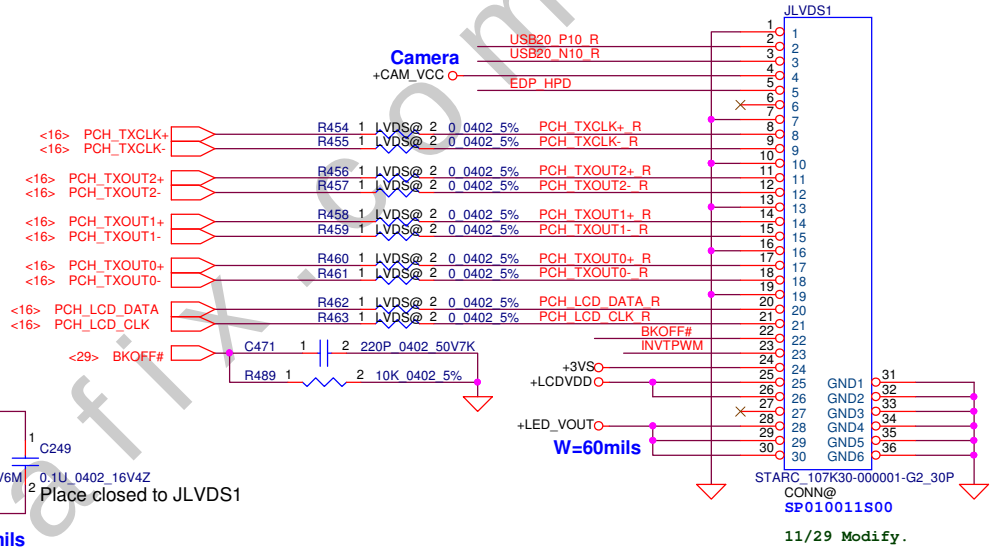


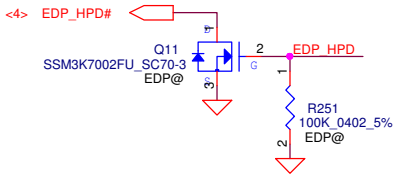




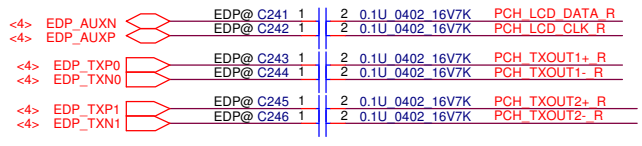


LCD/LED PANEL Conn.

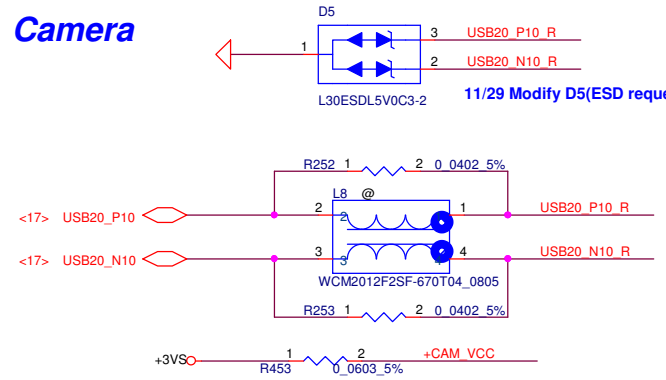




eDP



Camera



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Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: LVDS&eDP

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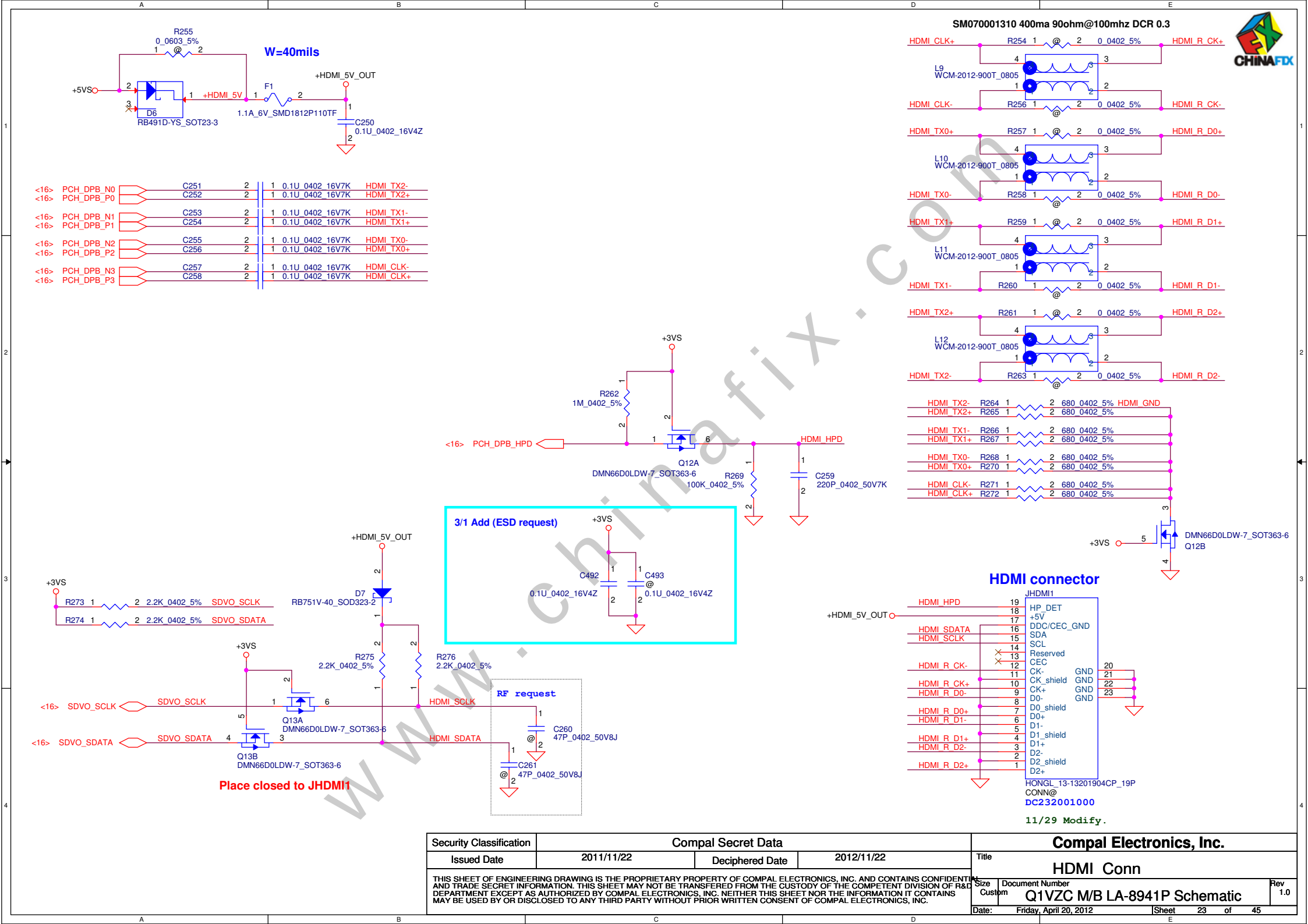
Date: Friday, April 20, 2012 | Sheet 22 of 45



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Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: HDMI Conn

Size	Document Number	Rev
Custom	Q1VZC M/B LA-8941P Schematic	1.0

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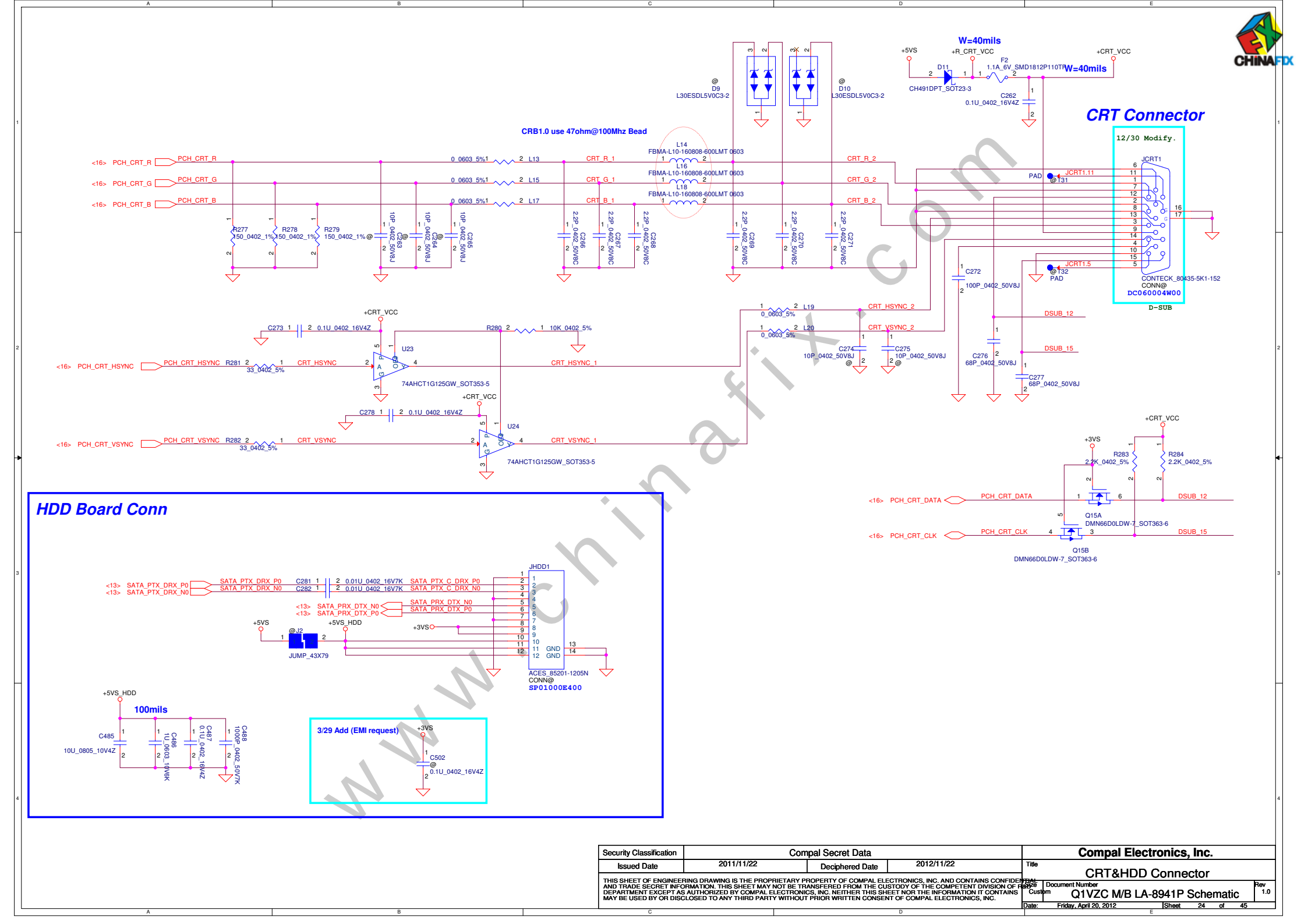

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/22	Deciphered Date 2012/11/22	Title: CRT&HDD Connector
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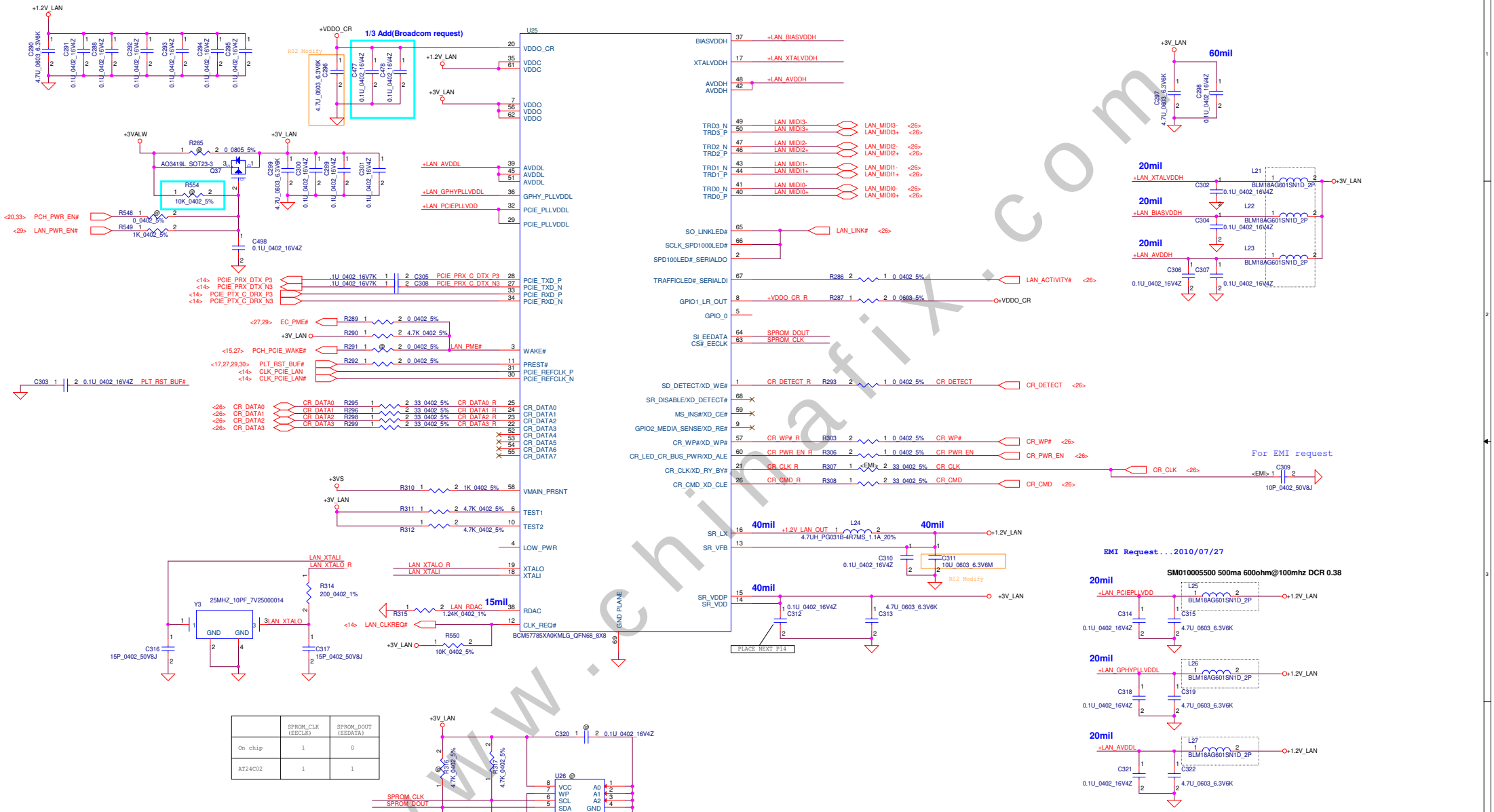
			Date: Friday, April 20, 2012; Sheet 24 of 45



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Issued Date	2011/11/22
Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: LAN Boardcom 57785

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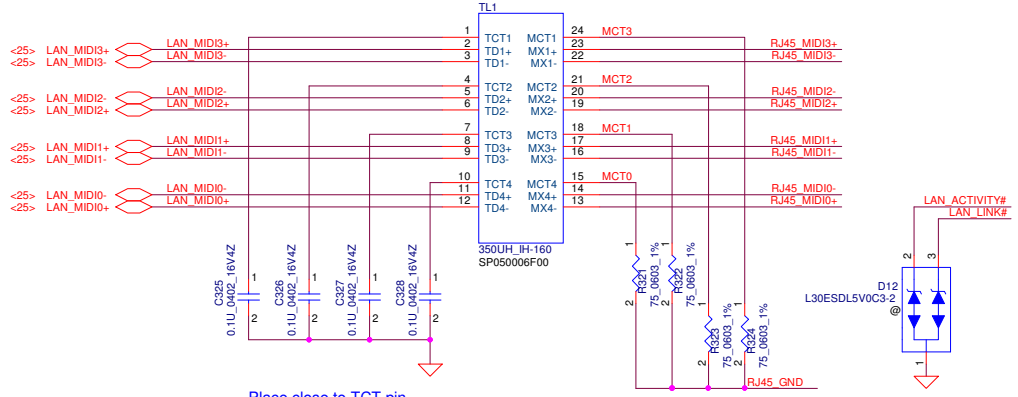
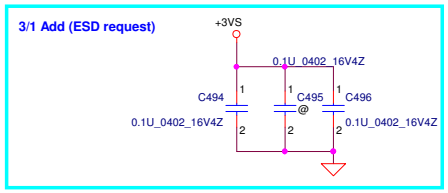
BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00

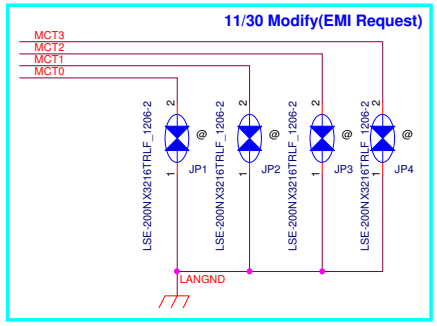
LAN Connector

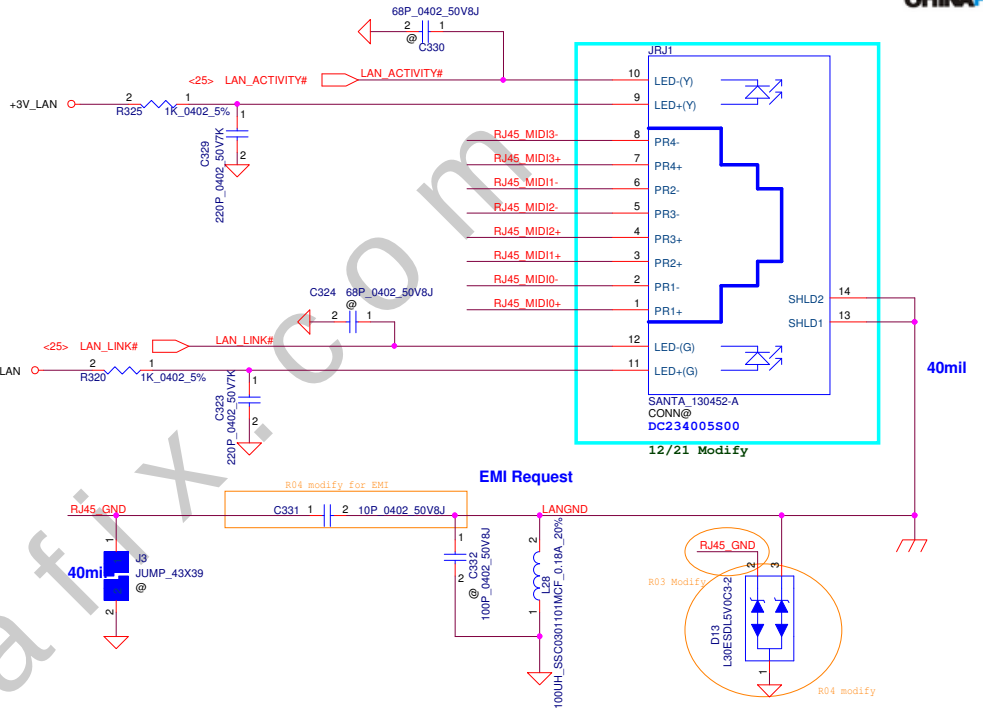
C474,C475 and D14
ME interefer,do not pop!!



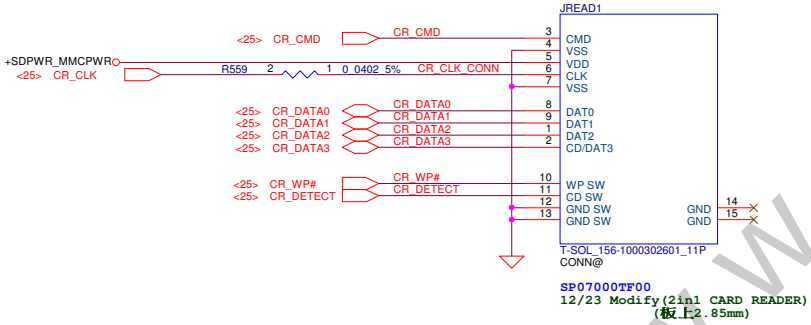
Place close to TCT pin

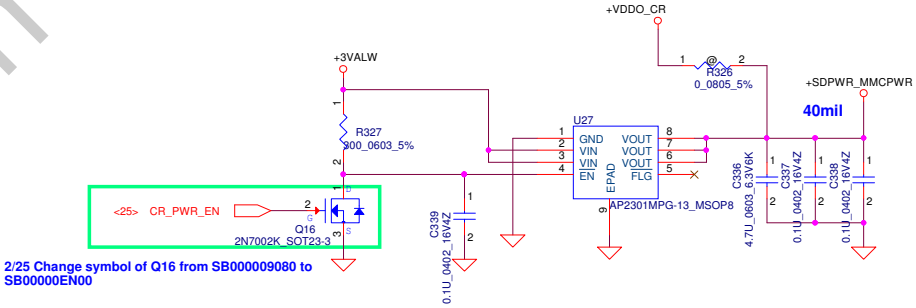


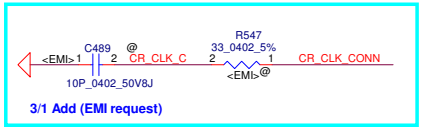


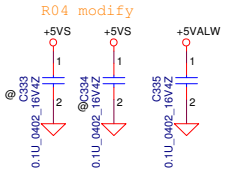


Card Reader Connector









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Compal Electronics, Inc.

Title: Card Reader

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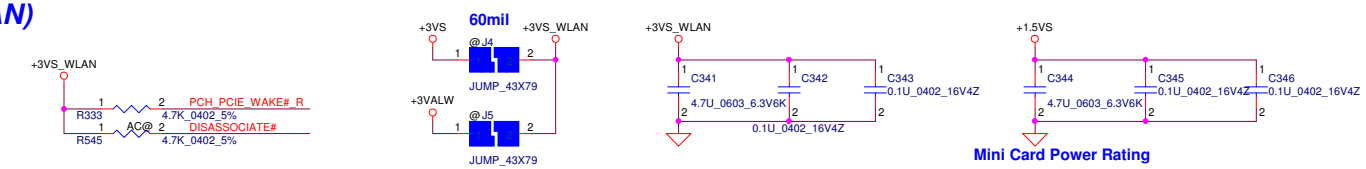
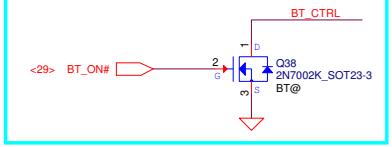
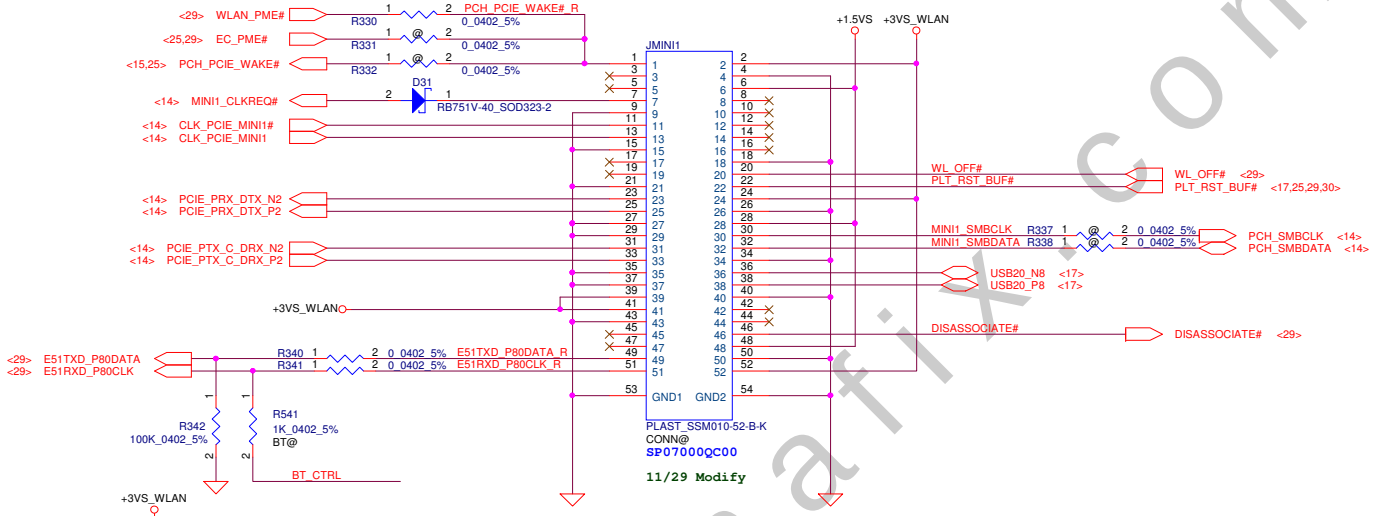
MINI CARD(Wireless LAN)

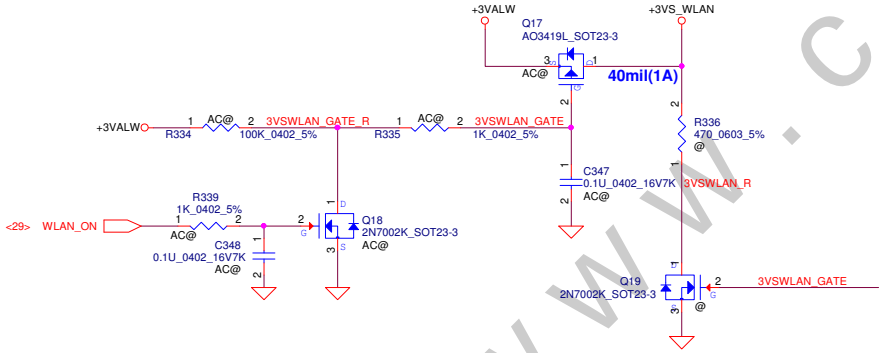


WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H







Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: MINI CARD (WLAN)

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

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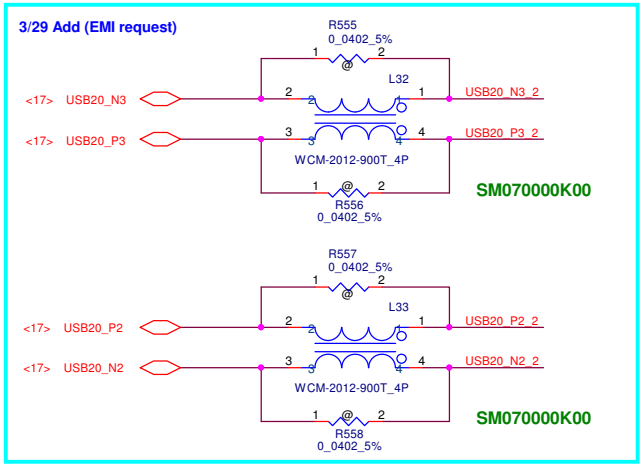
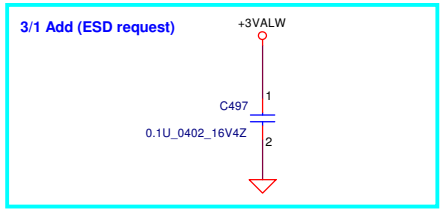
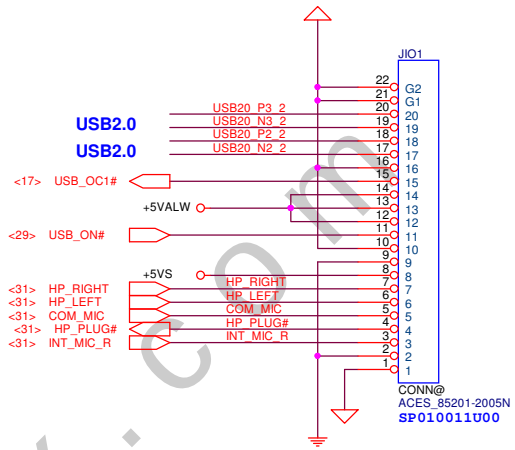
IO Board

3/29 Add (EMI request)



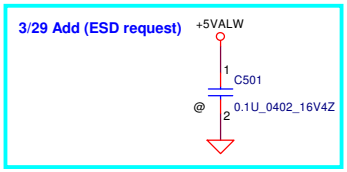
3/1 Add (ESD request)



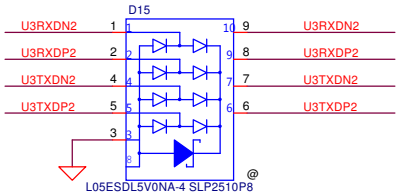


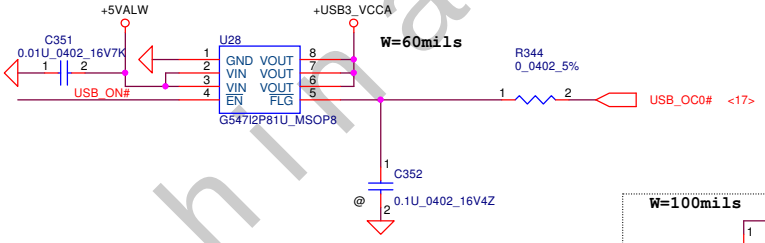
USB3.0

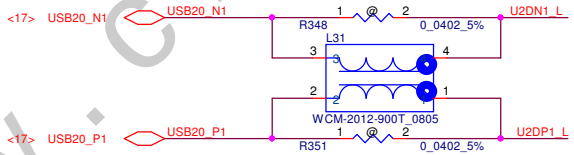
3/29 Add (ESD request)



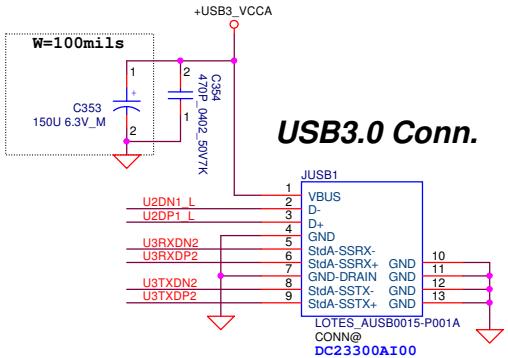
For ESD request







SM070001310 WCM2012F2SF-900T04 90ohm



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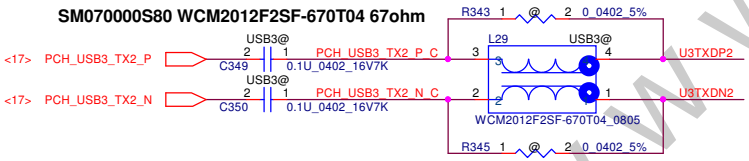

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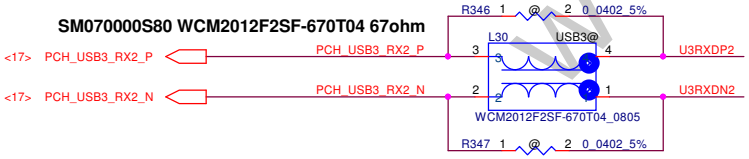
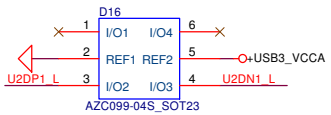


For USB2.0 ESD request



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Title	IO Board & USB3.0		
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
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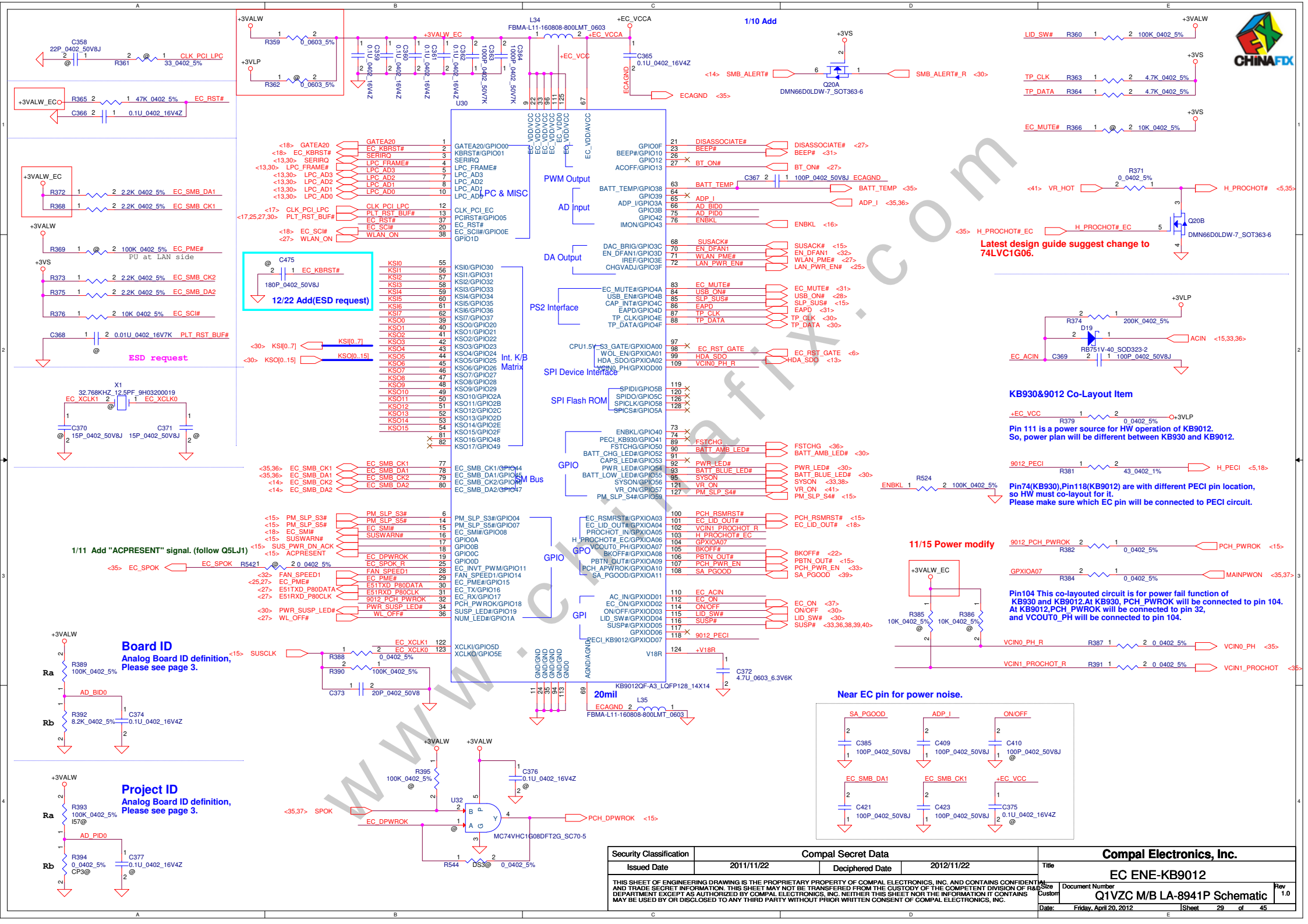

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: EC ENE-KB9012

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

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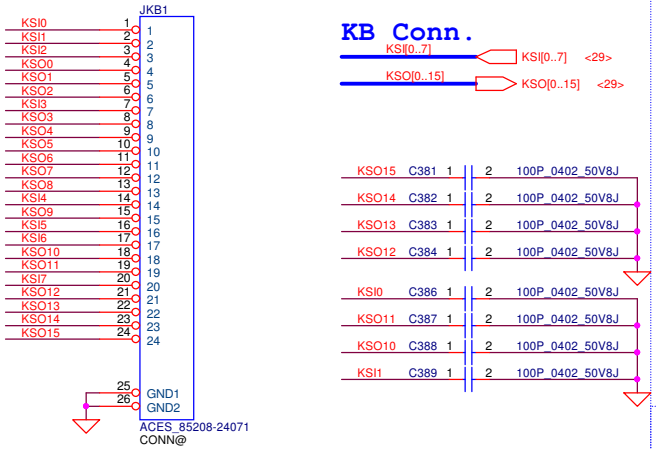
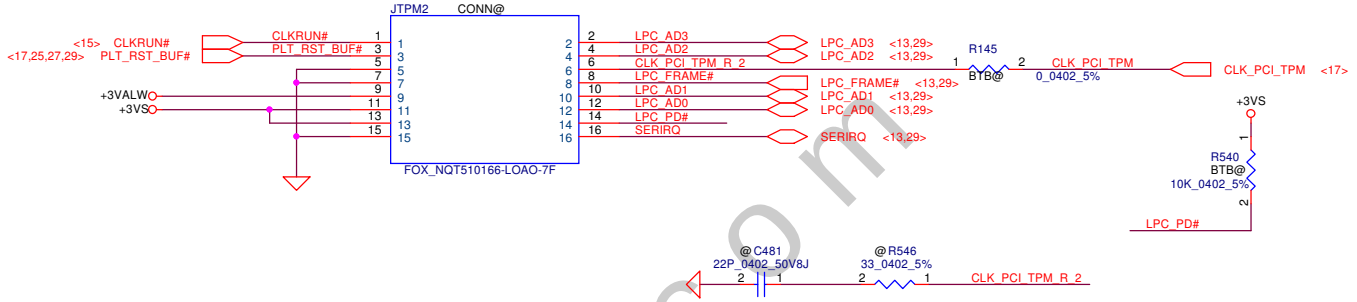
KB Conn.

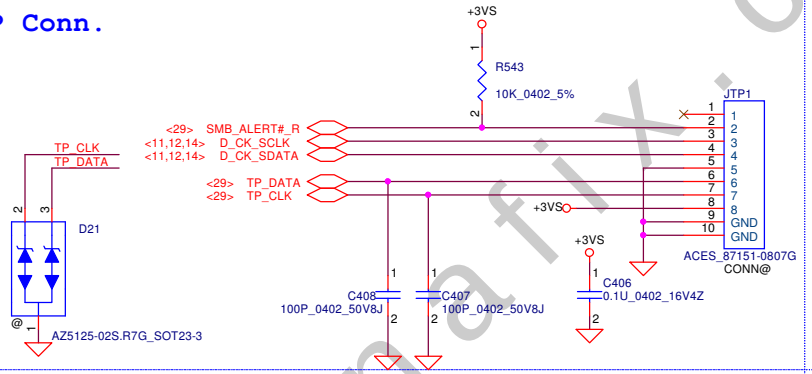


12/30 Modify.

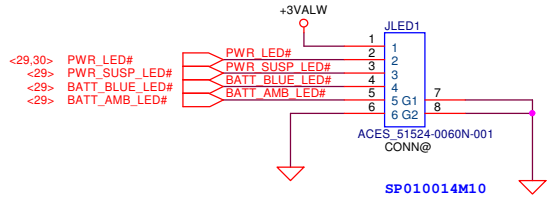
TPM



TP Conn.

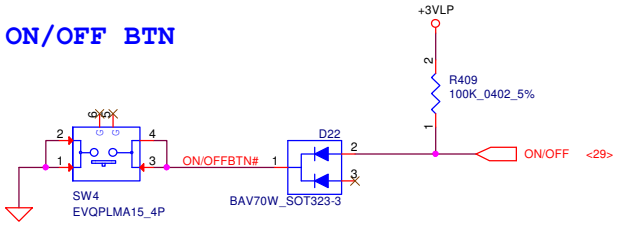


LED Board

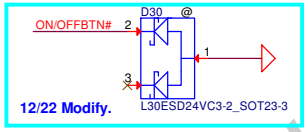


01/12 Change to ACES_51524-0060N-001 .

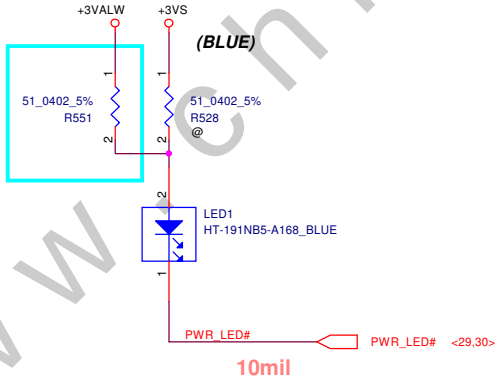
ON/OFF BTN



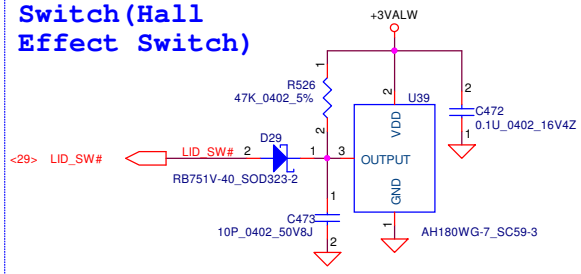
For power button ESD request



Power LED



Lid Switch(Hall Effect Switch)



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title	TP/IO Port/ KB CONN/TPM
Size	Custom
Document Number	Q1VZC M/B LA-8941P Schematic
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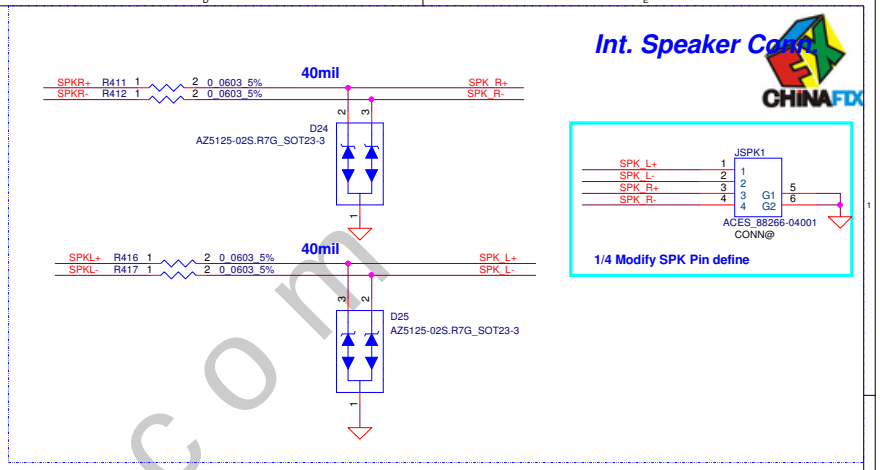
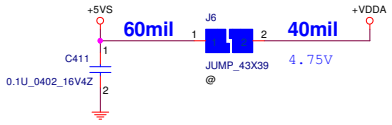
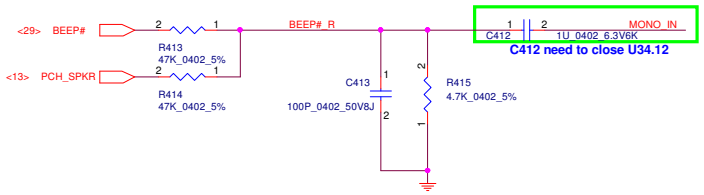
HD Audio Codec

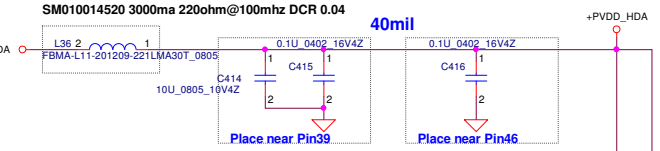
Int. Speaker Conn

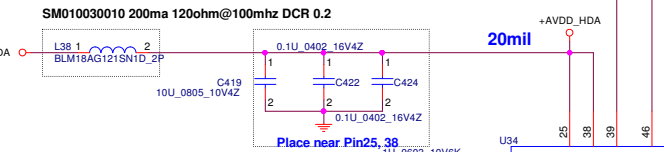


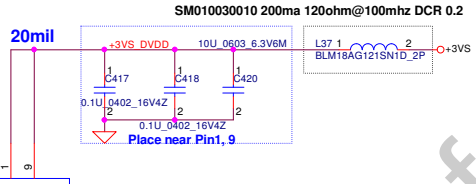


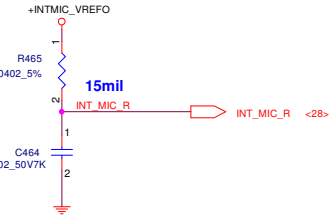
(output = 300 mA)

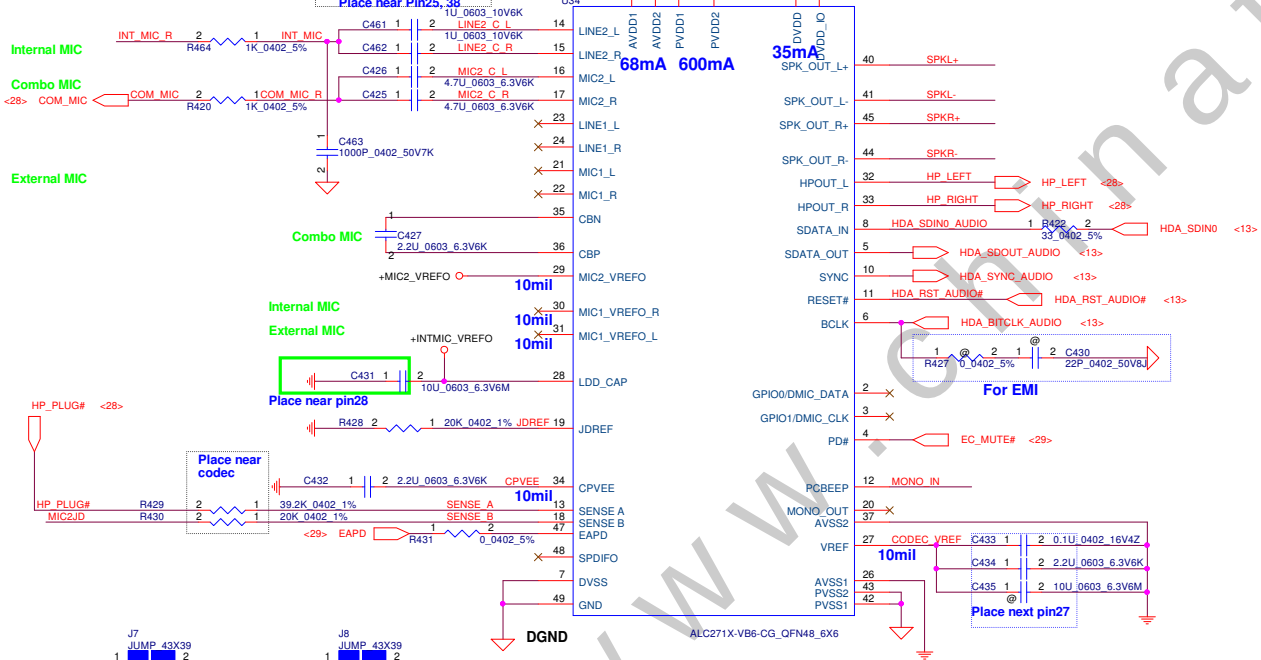


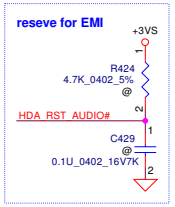


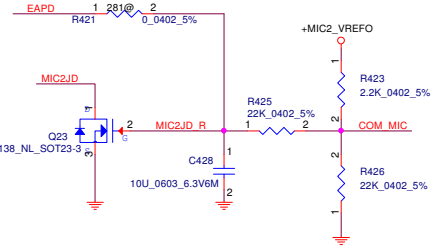


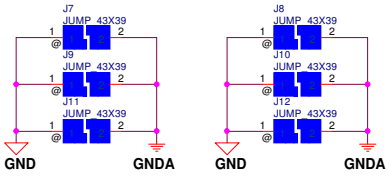












Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: HD Audio Codec ALC271X

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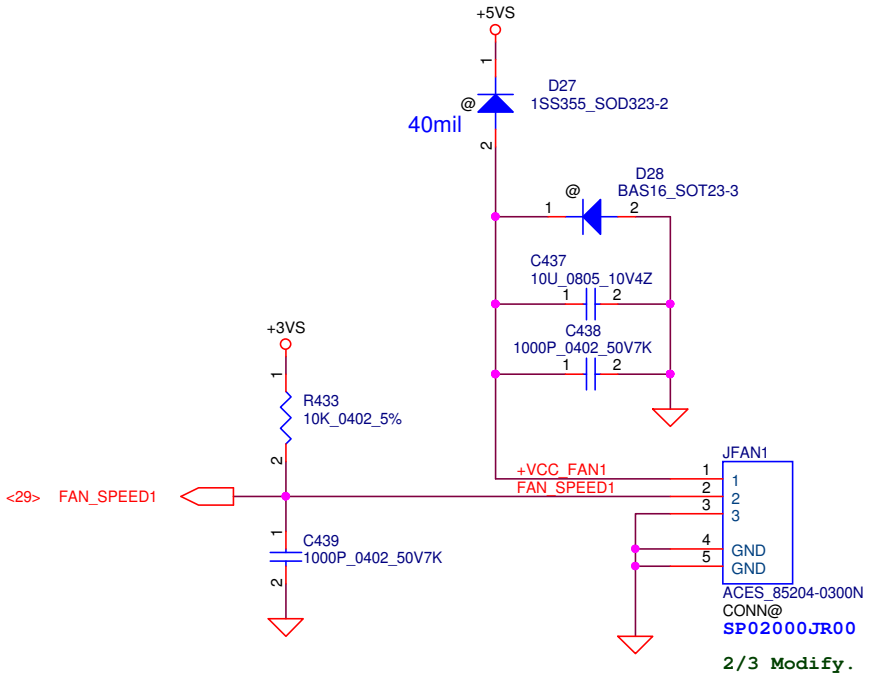
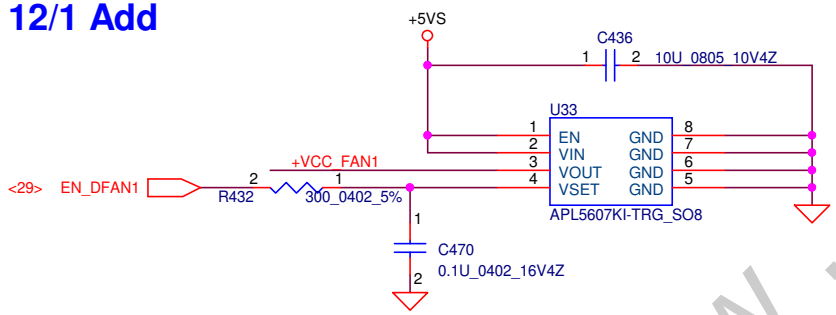
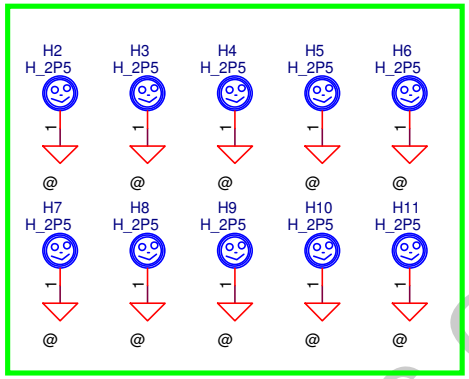
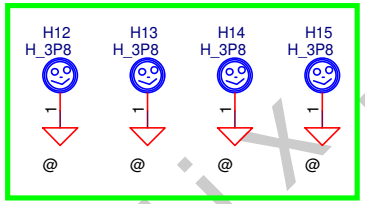
FAN1 Conn

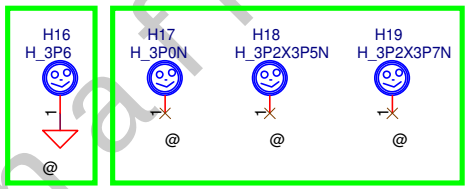


12/1 Add

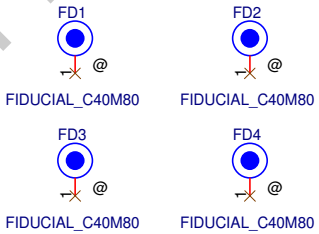








CPU support plate



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: FAN & Screw Hole

Size	Document Number	Rev
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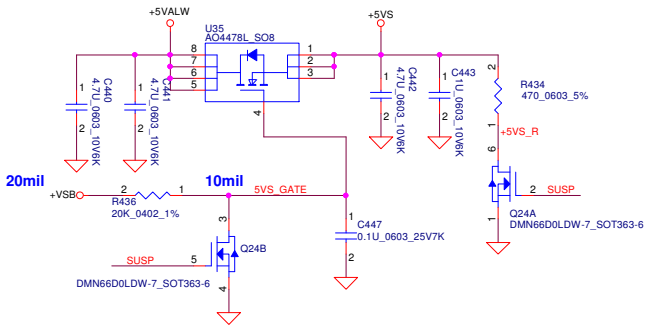
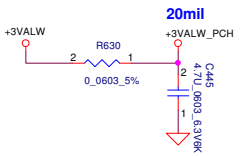
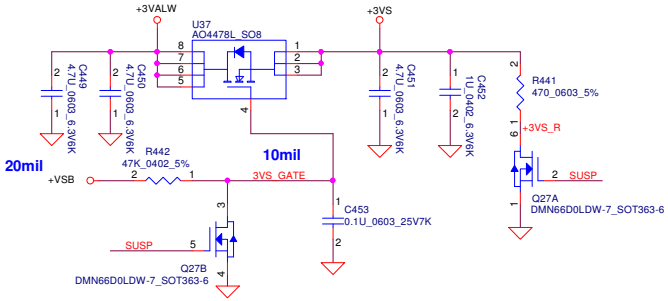
+5VALW TO +5VS



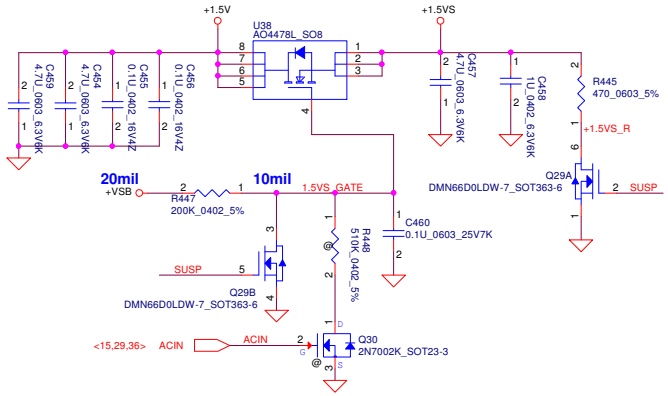
+3VALW to +3VALW_PCH(PCH AUX Power)

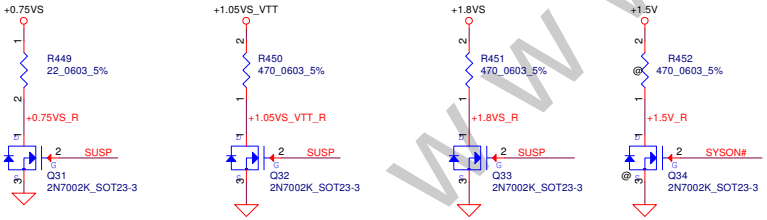


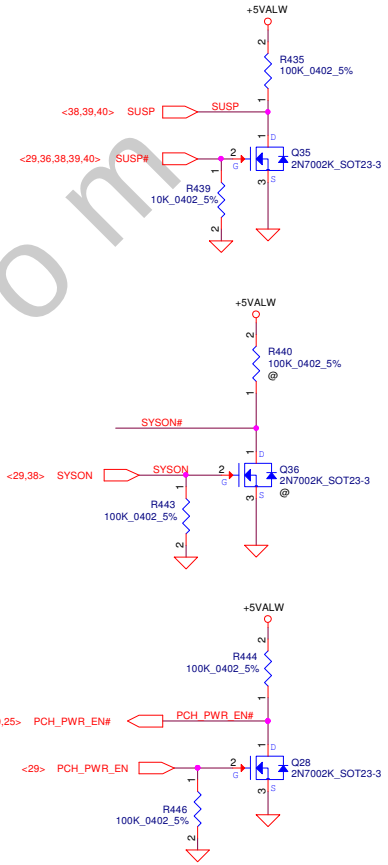
+3VALW TO +3VS



+1.5V to +1.5VS







Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

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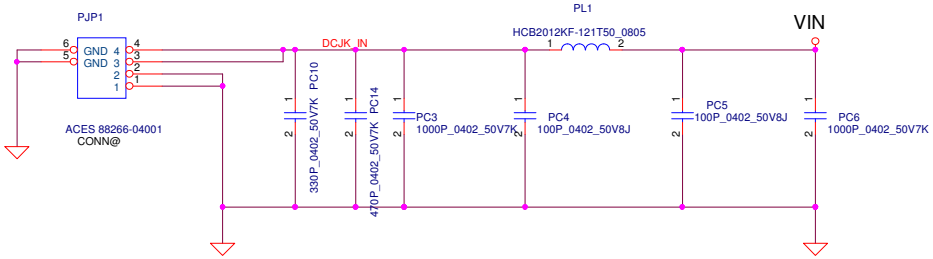

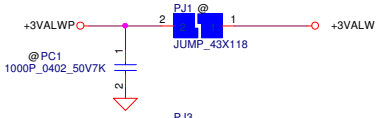

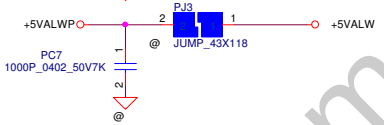

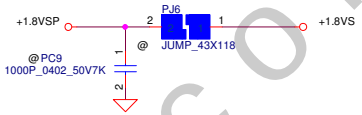

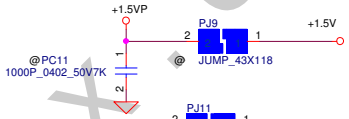

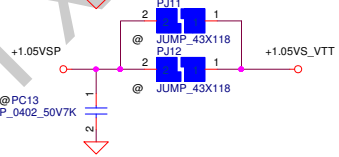

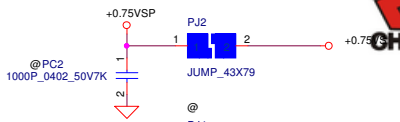

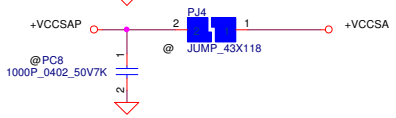

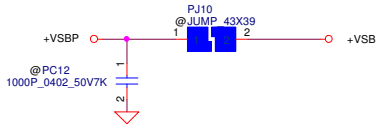

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size	Document Number	Rev
Custom	Q1VZC M/B LA-8941P Schematic	1.0

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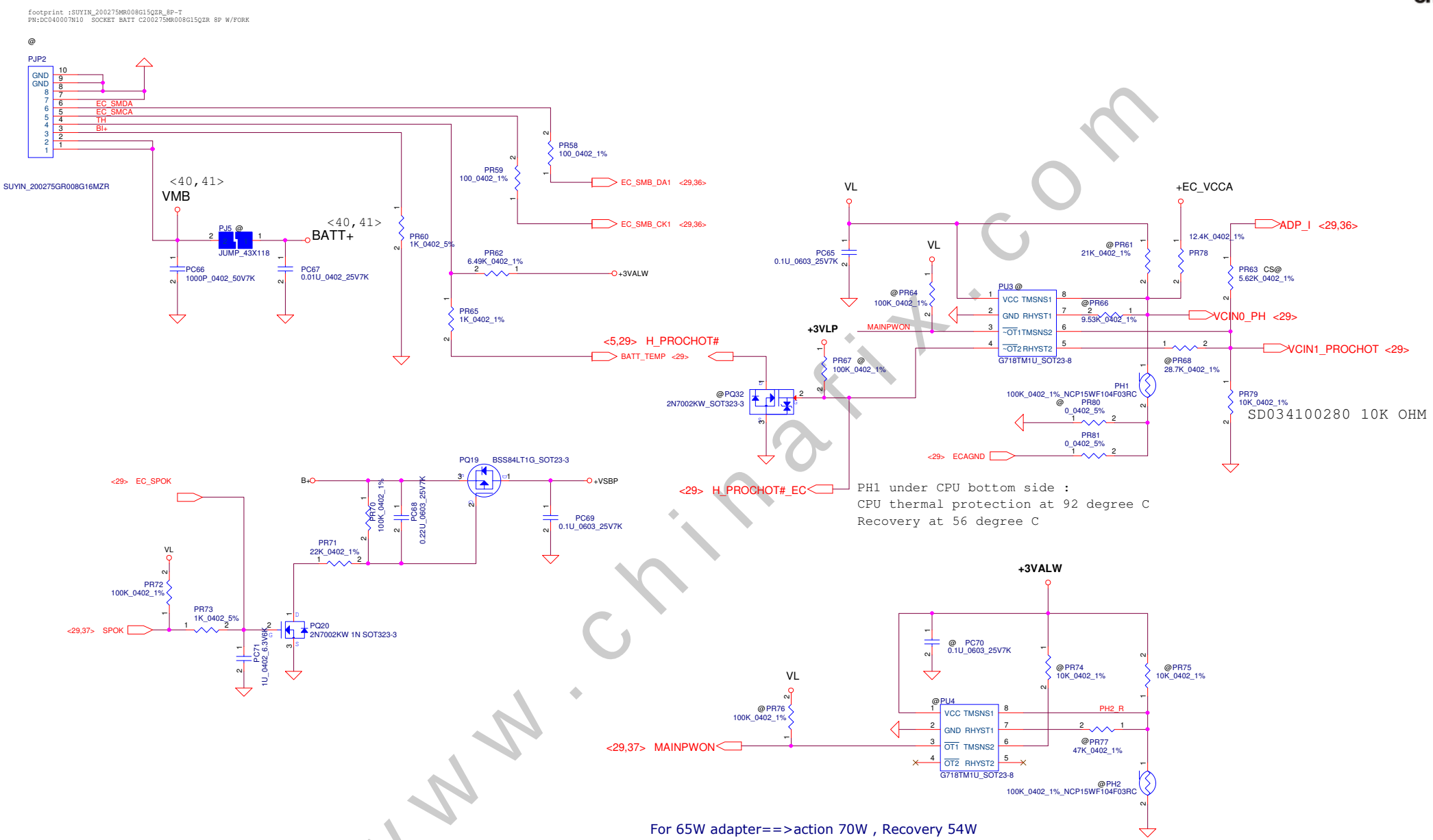

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

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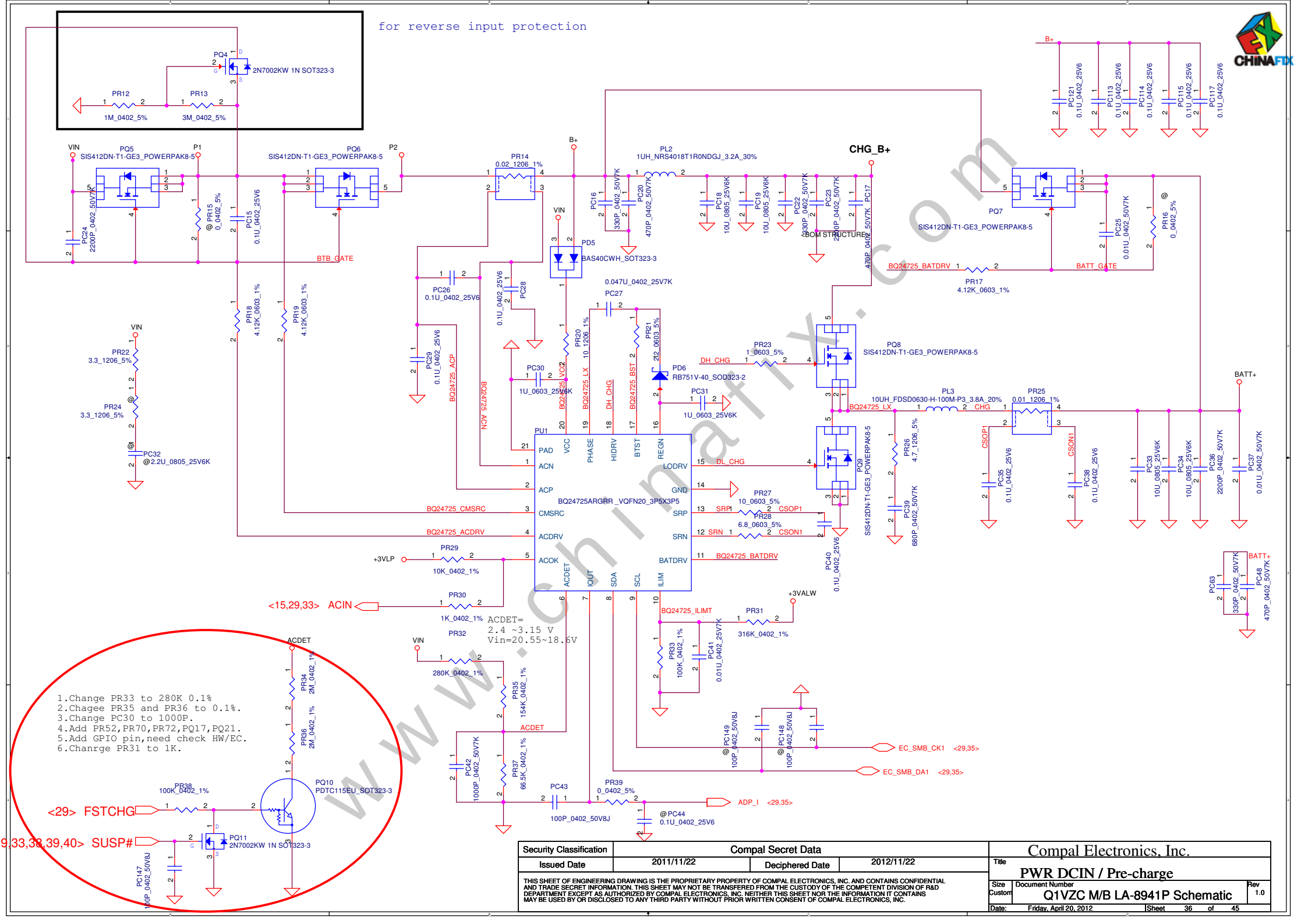

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

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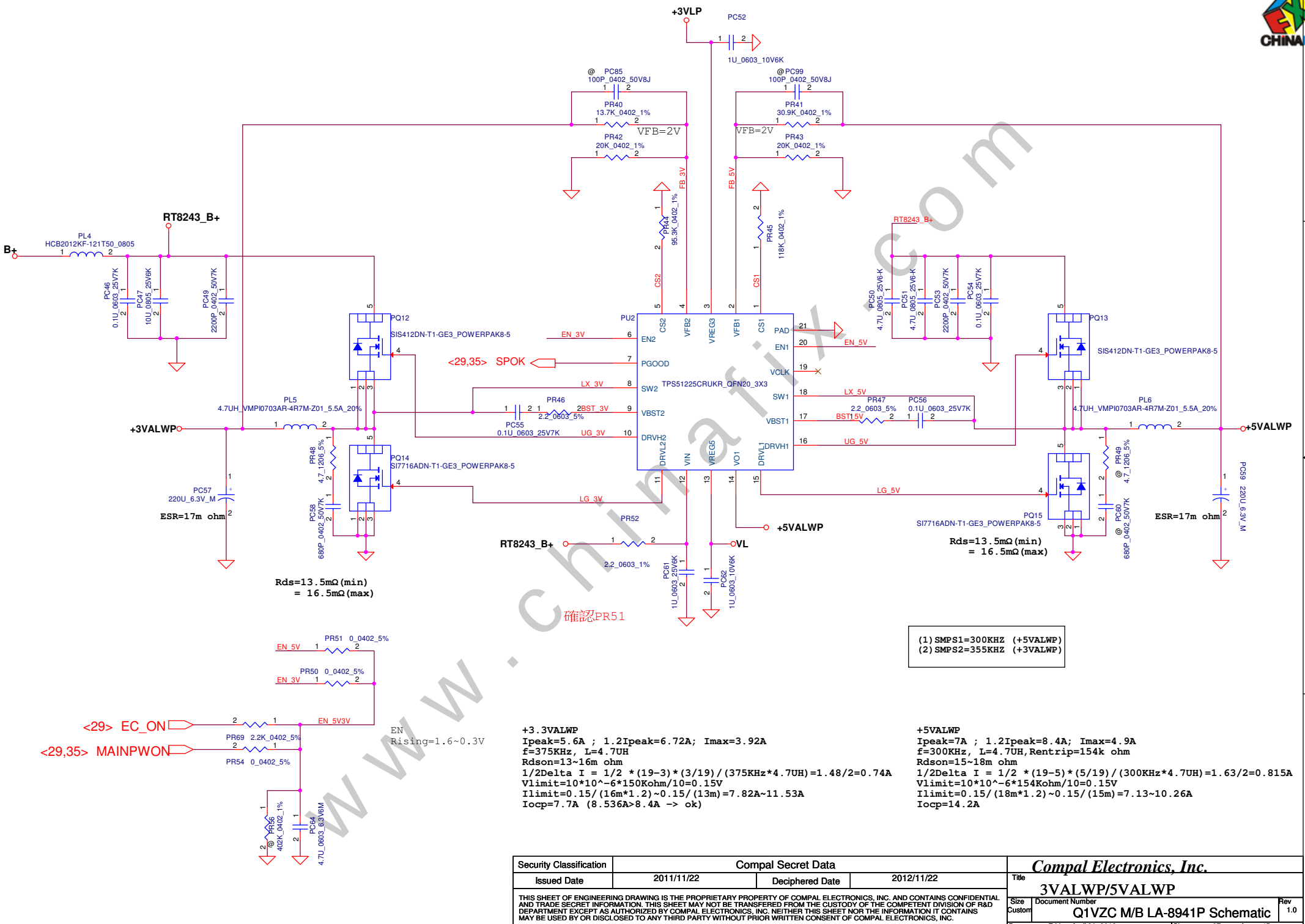

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	Q1VZC M/B LA-8941P Schematic	1.0

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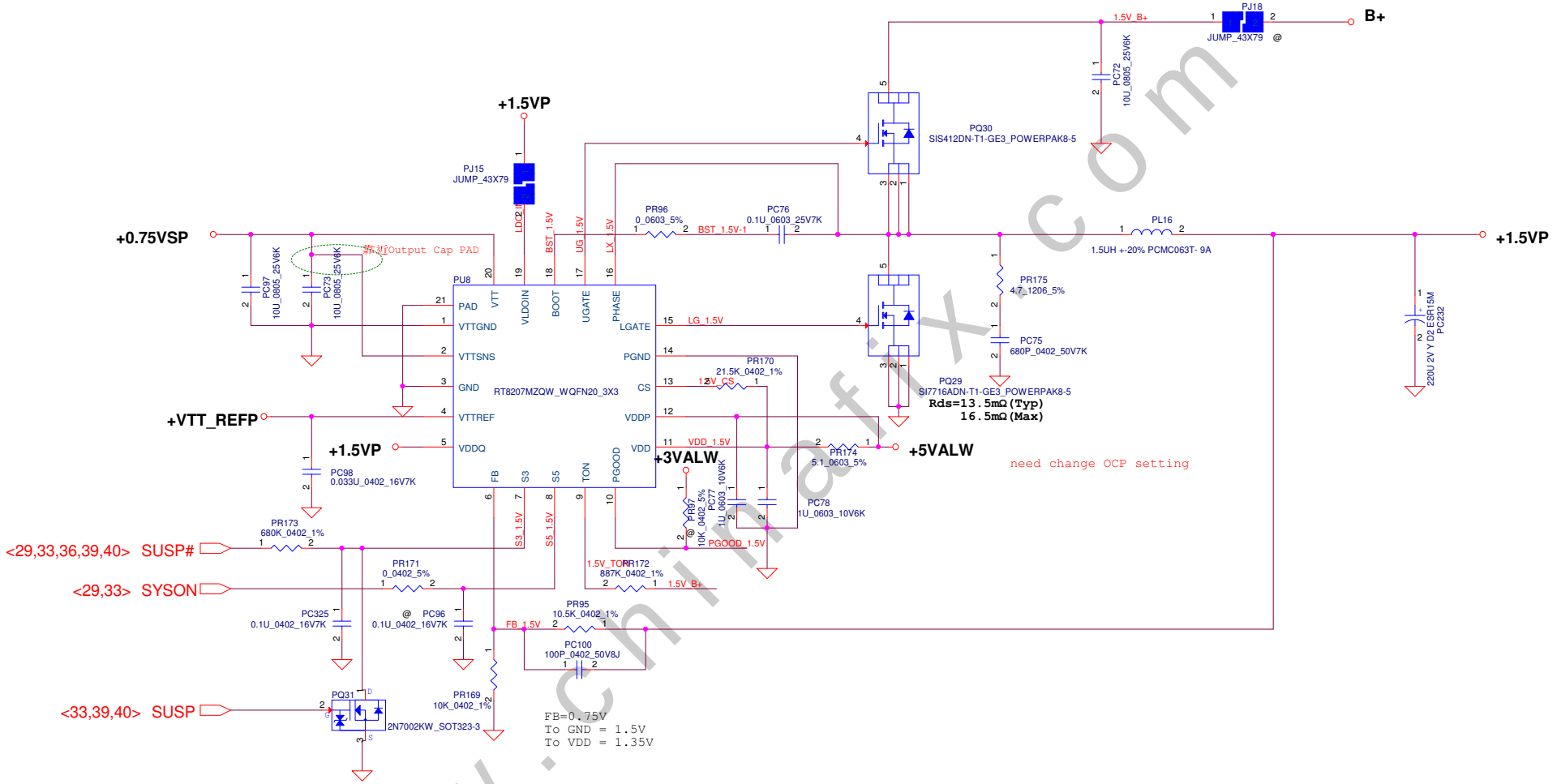

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off					

<Vo=1.5V> VFB=0.75V
V=0.75*(1+10K/10.5K)=1.52V
Fsw=286K to 200KHz

Cout ESR=17m ohm Rdson(max)=16.5 mohm Rdson(typ)=13.5 mohm.
Ipeak=12 A, Imax=8.4A, Iocp=14.4A

Delta I=((Vin-Vo)*(Vo/Vin))/(L*Fsw)=2.195A
=>1/2Delta I=1.099A

Iocpmax=((21.5K*11uA)/0.0135)+0.5 delta I= A
Iocpmin=((21.5K*9uA)/(0.0165))+0.5 delta I=15.6A

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Issued Date	2011/11/22	Deciphered Date	2012/11/22

Title	PWR-+1.5VP		
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
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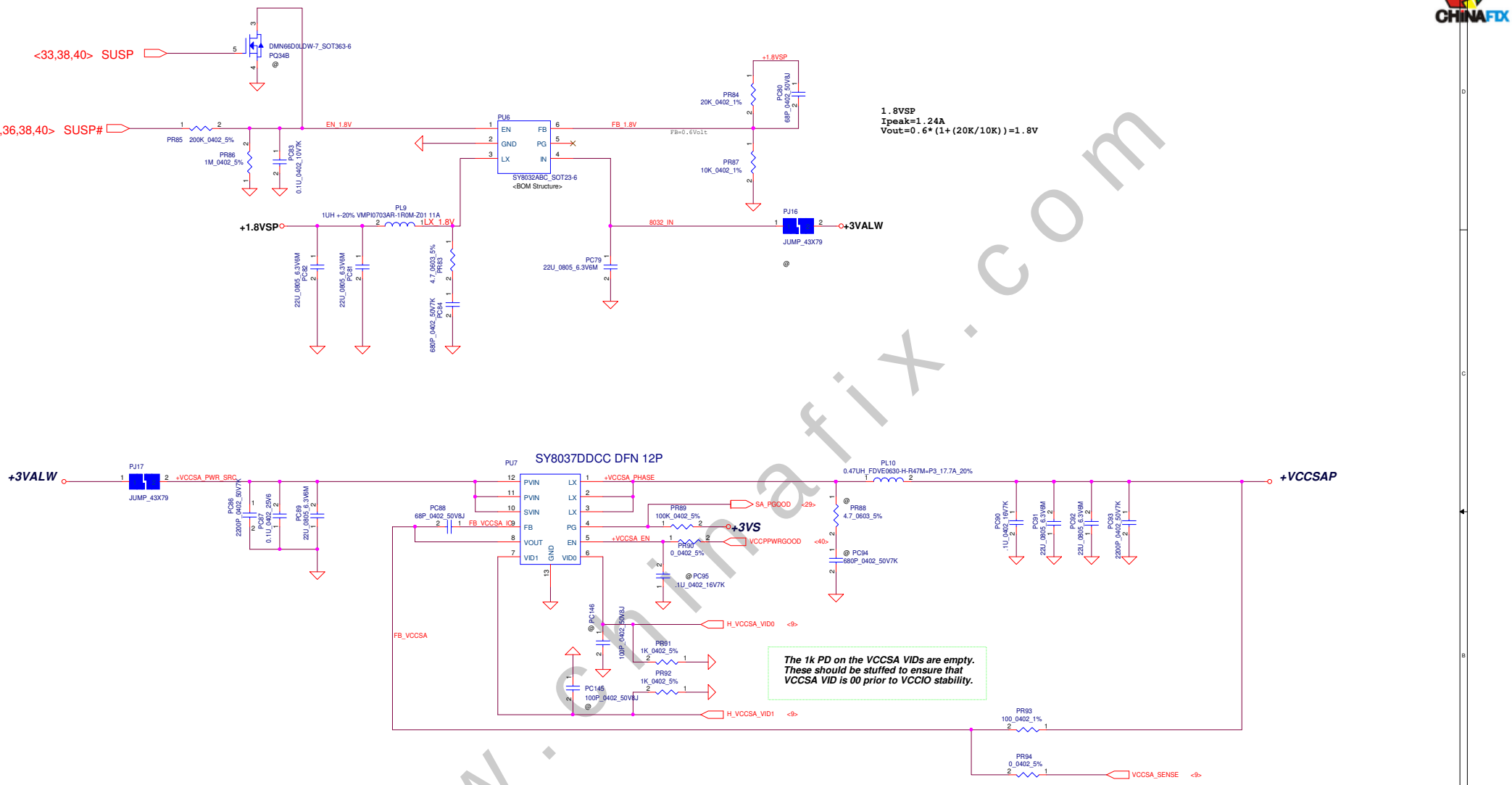

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

VID [0]	VID[1]	VCCSA Vout(ULV only)
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PWR +VCCSAP

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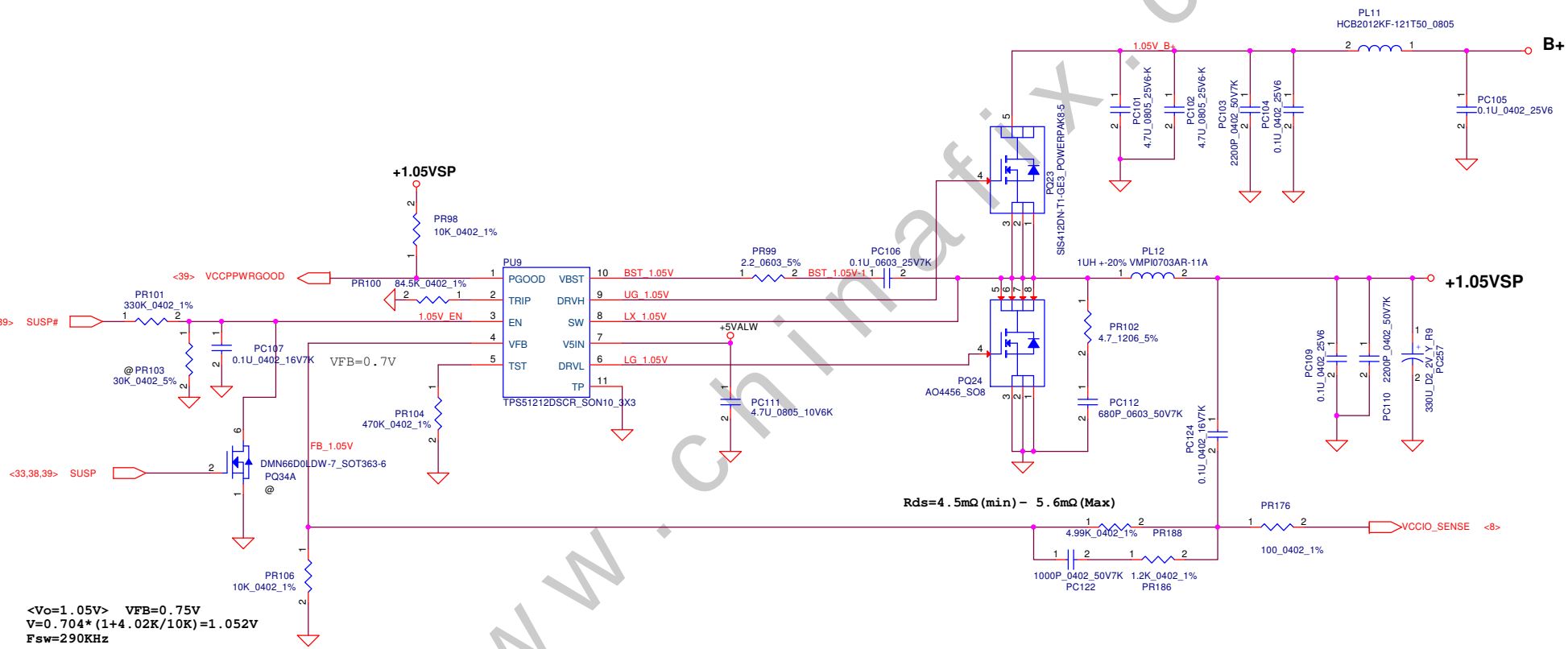

<Vo=1.05V> VFB=0.75V
V=0.704*(1+4.02K/10K)=1.052V
Fsw=290KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=15.6A, Imax=10.92A, Iocp=18.72A

Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=2.06A

Iocpmax=((15K*11uA)/0.0045)+1.665A=23.54A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=19A
Iocp=A

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size	Document Number	Rev
Custom	Q1VZC M/B LA-8941P Schematic	1.0

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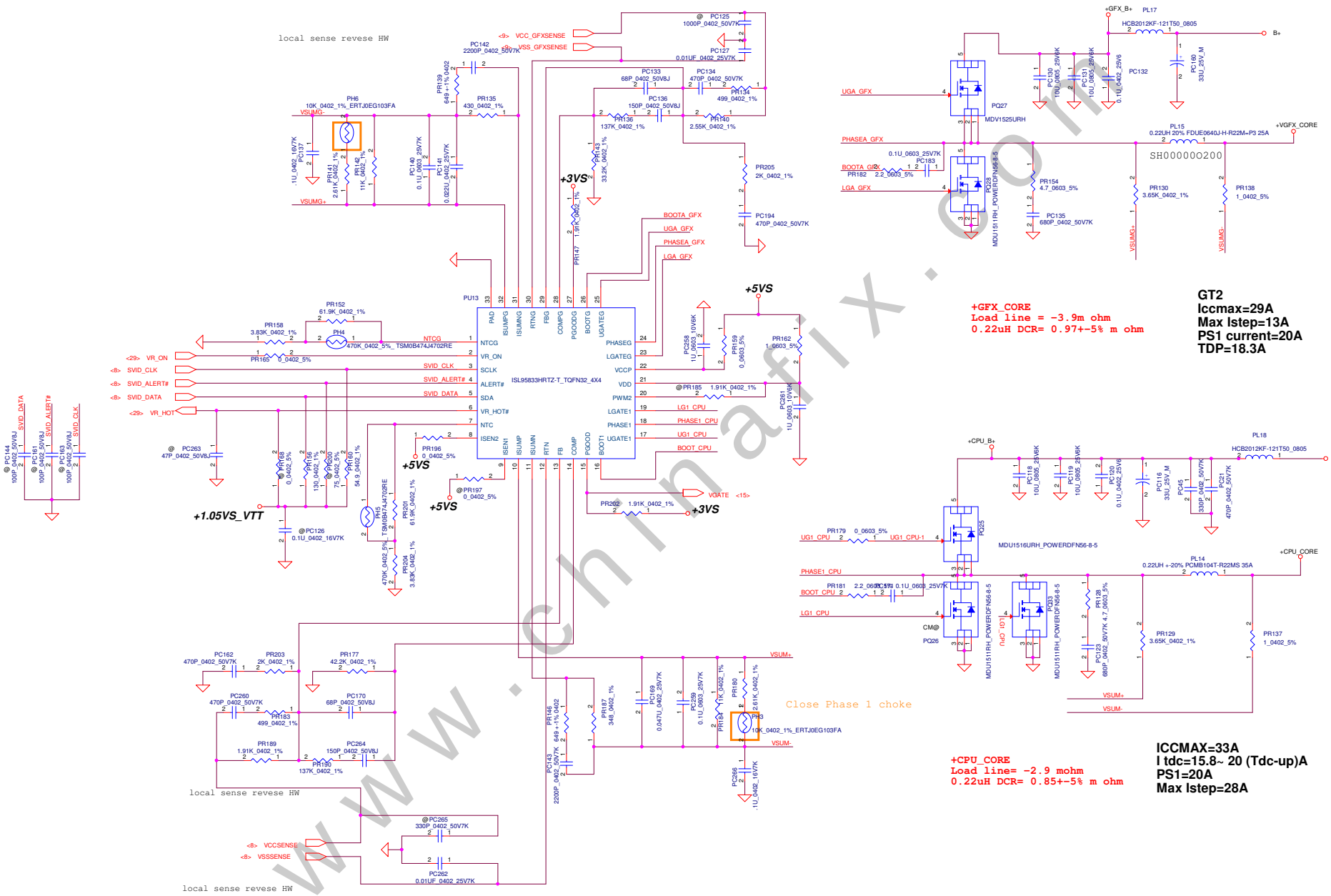

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/22	Deciphered Date 2012/11/22	Title CPU/GFX_CORE

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CR PDDG Rev 0.95

+CPU_CORE

Mid-Frequency Decoupling
12x22µF

PC150 22U_0805_6.3V6M
PC151 22U_0805_6.3V6M
PC152 22U_0805_6.3V6M
PC153 22U_0805_6.3V6M
PC154 22U_0805_6.3V6M
PC155 22U_0805_6.3V6M
PC156 22U_0805_6.3V6M
PC157 22U_0805_6.3V6M
PC234 22U_0805_6.3V6M
PC233 22U_0805_6.3V6M
PC158 22U_0805_6.3V6M
PC159 22U_0805_6.3V6M

Low-Frequency
Decoupling 3x330 µF 9m

PC179 330U_D2_2V_Y
PC180 330U_D2_2V_Y
@ PC181 330U_D2_2V_Y
PC182 330U_D2_2V_Y

+CPU_CORE

PC186 2.2U_0402_6.3V6M
PC187 2.2U_0402_6.3V6M
PC188 2.2U_0402_6.3V6M
PC189 2.2U_0402_6.3V6M
PC190 2.2U_0402_6.3V6M
PC191 2.2U_0402_6.3V6M
PC192 2.2U_0402_6.3V6M
PC193 2.2U_0402_6.3V6M
PC174 330P_0402_50V7K
PC108 470P_0402_50V7K
PC195 2.2U_0402_6.3V6M
PC196 2.2U_0402_6.3V6M
PC197 2.2U_0402_6.3V6M
PC198 2.2U_0402_6.3V6M
PC199 2.2U_0402_6.3V6M
PC200 2.2U_0402_6.3V6M
PC201 2.2U_0402_6.3V6M
PC202 2.2U_0402_6.3V6M

High-Frequency Decoupling
16x2.2µF

+VGFX_CORE

Mid-Frequency Decoupling
6x22µF

+VGFX_CORE

PC164 22U_0805_6.3V6M
PC165 22U_0805_6.3V6M
PC166 22U_0805_6.3V6M
PC167 22U_0805_6.3V6M
PC168 22U_0805_6.3V6M
PC172 22U_0805_6.3V6M

Mid-Frequency Decoupling
6x10µF 0603

PC173 10U_0603_6.3V6M
PC174 10U_0603_6.3V6M
PC175 10U_0603_6.3V6M
PC176 10U_0603_6.3V6M
PC177 10U_0603_6.3V6M
PC178 10U_0603_6.3V6M

Low-Frequency
Decoupling 2x330 µF 9m

PC184 330U_D2_2V_Y
PC185 330U_D2_2V_Y

High-Frequency Decoupling
11x1µF

PC204 1U_0402_6.3V6K
PC205 1U_0402_6.3V6K
PC206 1U_0402_6.3V6K
PC207 1U_0402_6.3V6K
PC208 1U_0402_6.3V6K
PC209 1U_0402_6.3V6K
PC219 1U_0402_6.3V6K
PC220 1U_0402_6.3V6K
PC221 1U_0402_6.3V6K
PC222 1U_0402_6.3V6K
PC223 1U_0402_6.3V6K

+1.05VS_VTT

High-Frequency Decoupling
27x1µF

PC254 1U_0402_6.3V6K
PC239 1U_0402_6.3V6K
PC240 1U_0402_6.3V6K
PC238 1U_0402_6.3V6K
PC237 1U_0402_6.3V6K
PC236 1U_0402_6.3V6K
PC231 1U_0402_6.3V6K
PC230 1U_0402_6.3V6K
PC235 1U_0402_6.3V6K
PC229 1U_0402_6.3V6K
PC228 1U_0402_6.3V6K
PC226 1U_0402_6.3V6K
PC225 1U_0402_6.3V6K
PC227 1U_0402_6.3V6K
PC253 1U_0402_6.3V6K
PC252 1U_0402_6.3V6K
PC251 1U_0402_6.3V6K
PC249 1U_0402_6.3V6K
PC250 1U_0402_6.3V6K
PC248 1U_0402_6.3V6K
PC246 1U_0402_6.3V6K
PC247 1U_0402_6.3V6K
PC245 1U_0402_6.3V6K
PC243 1U_0402_6.3V6K
PC241 1U_0402_6.3V6K
PC242 1U_0402_6.3V6K
PC244 1U_0402_6.3V6K

+1.05VS_VTT

Mid-Frequency Decoupling
10x10µF

PC224 10U_0603_6.3V6M
PC218 10U_0603_6.3V6M
PC217 10U_0603_6.3V6M
PC216 10U_0603_6.3V6M
PC215 10U_0603_6.3V6M
PC214 10U_0603_6.3V6M
PC213 10U_0603_6.3V6M
PC212 10U_0603_6.3V6M
PC211 10U_0603_6.3V6M
PC210 10U_0603_6.3V6M

Low-Frequency
Decoupling 1x330 µF 9m

PC203 330U_D2_2V_Y

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1			0.1			2010/12/29	
2			0.1	---		2010/12/29	
3						2011/02/08	
4						2011/02/08	
5						2011/02/08	
6				---		2011/02/08	
7				---		2011/02/16	
8				---		2011/05/13	PVT2
9				---		2011/05/13	PVT2
10				---		2011/05/13	PVT2
11				---		2011/05/13	PVT2
12						2011/05/13	PVT2
13							
14							
15							

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

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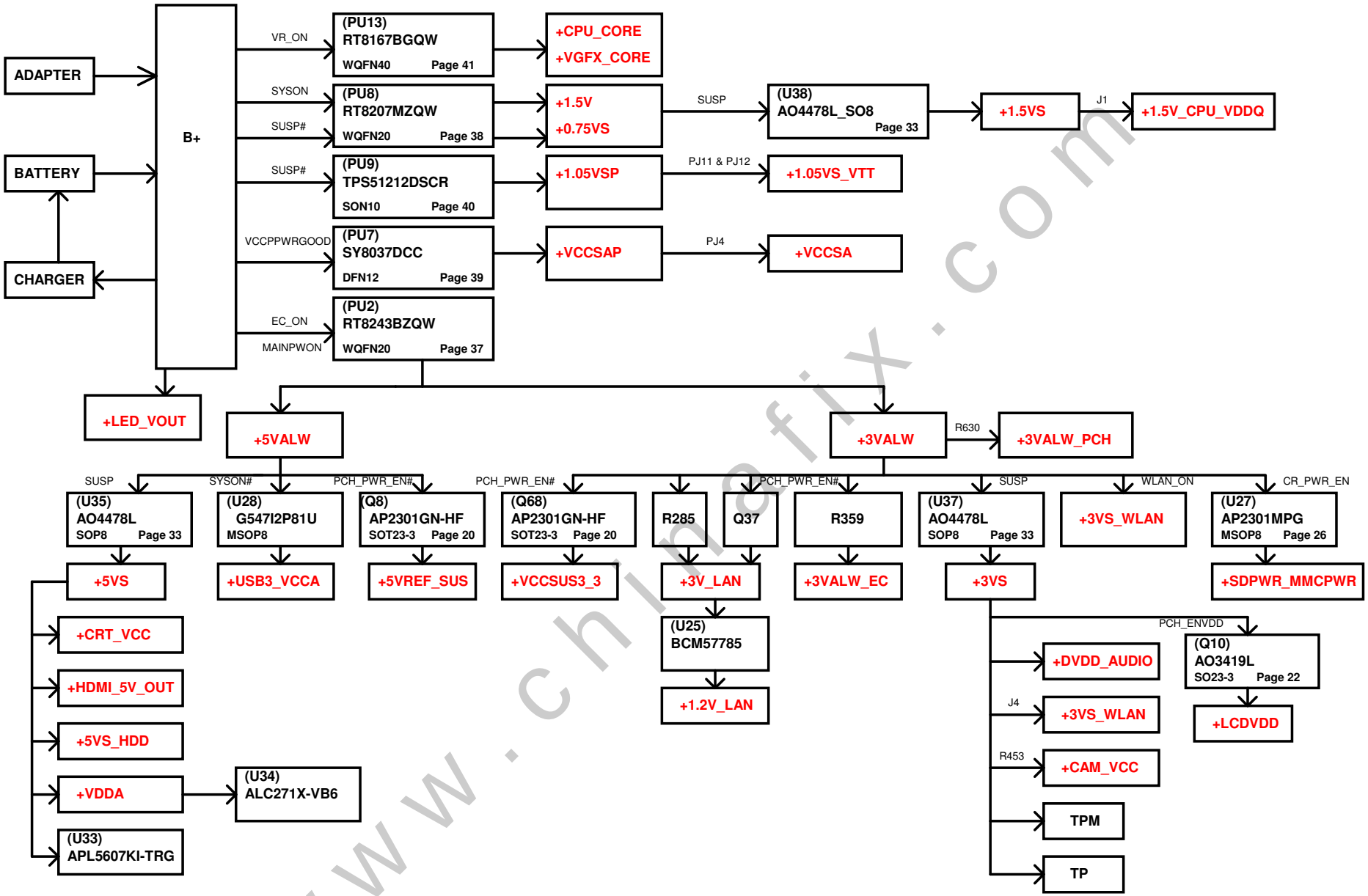

Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2012/06/13

Compal Electronics, Inc.

Title: Power Rail

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

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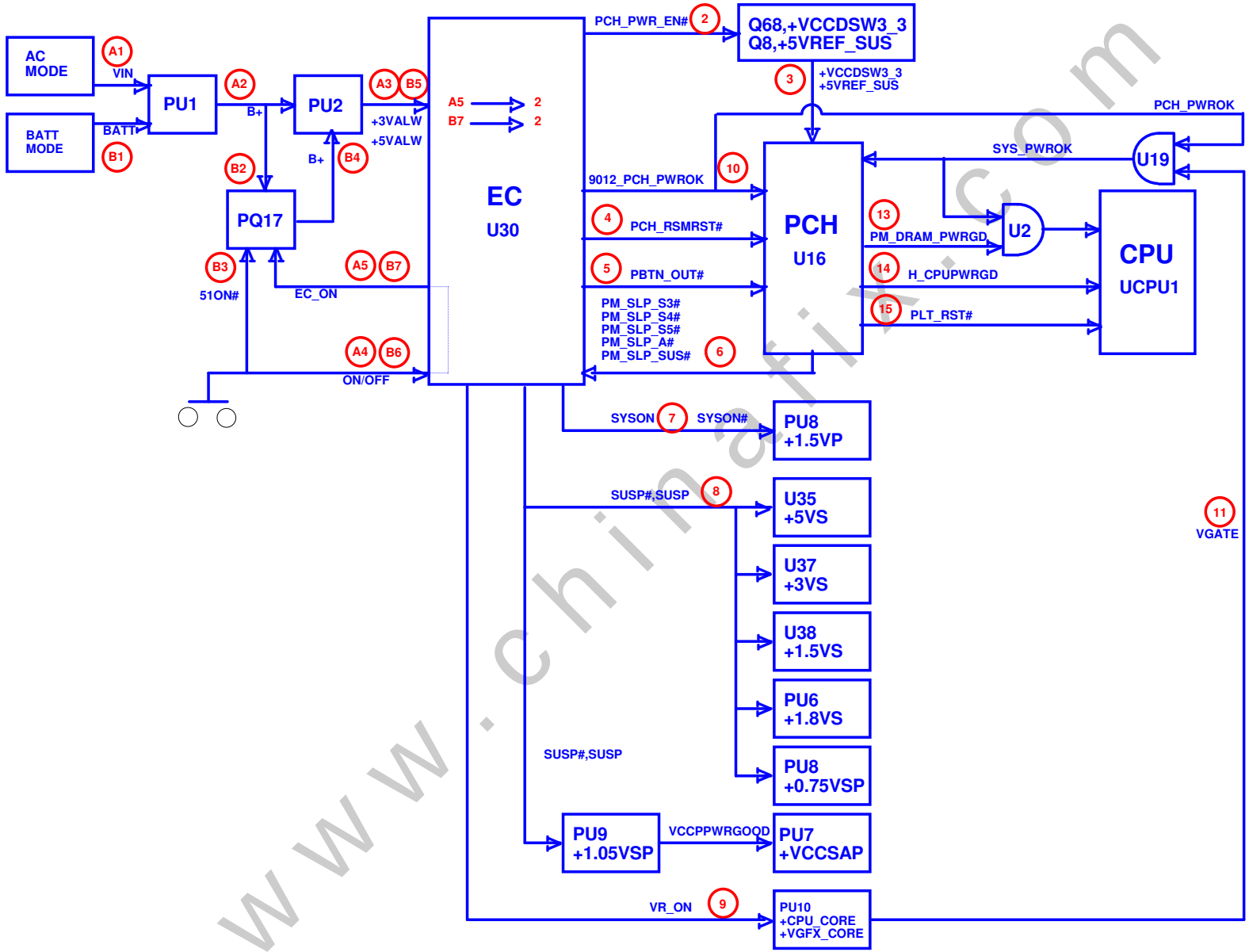

Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2012/06/13

Compal Electronics, Inc.

Title: Power sequence

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

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