3-Phase Synchronous-Rectified Buck Controller for Mobile GPU Power

General Description

The uP1642P is a 3/2/1-phase synchronous-rectified buck controller specifically designed to work with 4.5V ~ 26V input voltage and deliver high quality output voltage for high-performance graphic processor power.

The uP1642P adopts proprietary RCOT™ technology, providing flexible selection of output LC filter and excellent transient response to load and line change.

The uP1642P supports NVIDIA Open Voltage Regulator-2 and 2+1 with PWMVID feature. The PWMVID input is buffered and filtered to generate accurate reference voltage, and the output voltage is precisely regulated to the reference input.

The uP1642P integrates two bootstrapped MOSFET gate drivers and one PWM output achieving optimal balance between cost and flexibility. The uP1642P uses MOSFET $R_{DS(ON)}$ current sensing for channel current balance.

Other features include accurate and reliable short-circuit protection, adjustable on-time setting, power saving control input, and a delayed power good output. This part is available in VQFN4x4 - 24L package.

Ordering Information

Order Number	Package Type	Top Marking
uP1642PQAG	VQFN4x4-24L	uP1642P

Note: uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

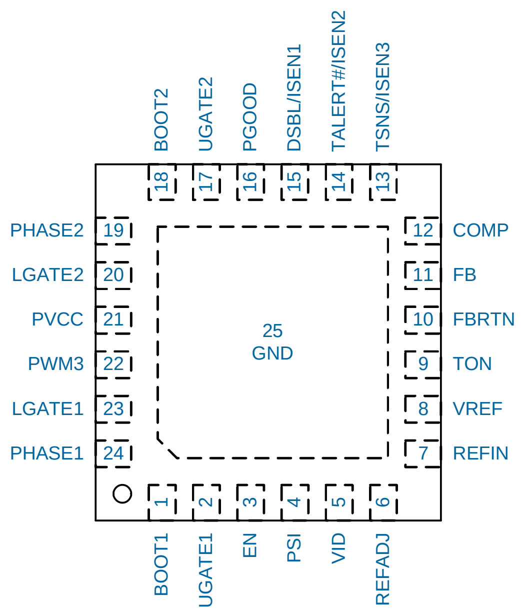
Applications

- Middle-High End GPU Core Power
- High End Desktop PC Memory Core Power
- Low Output Voltage, High Power Density DC-DC Converters
- Voltage Regulator Modules

Features

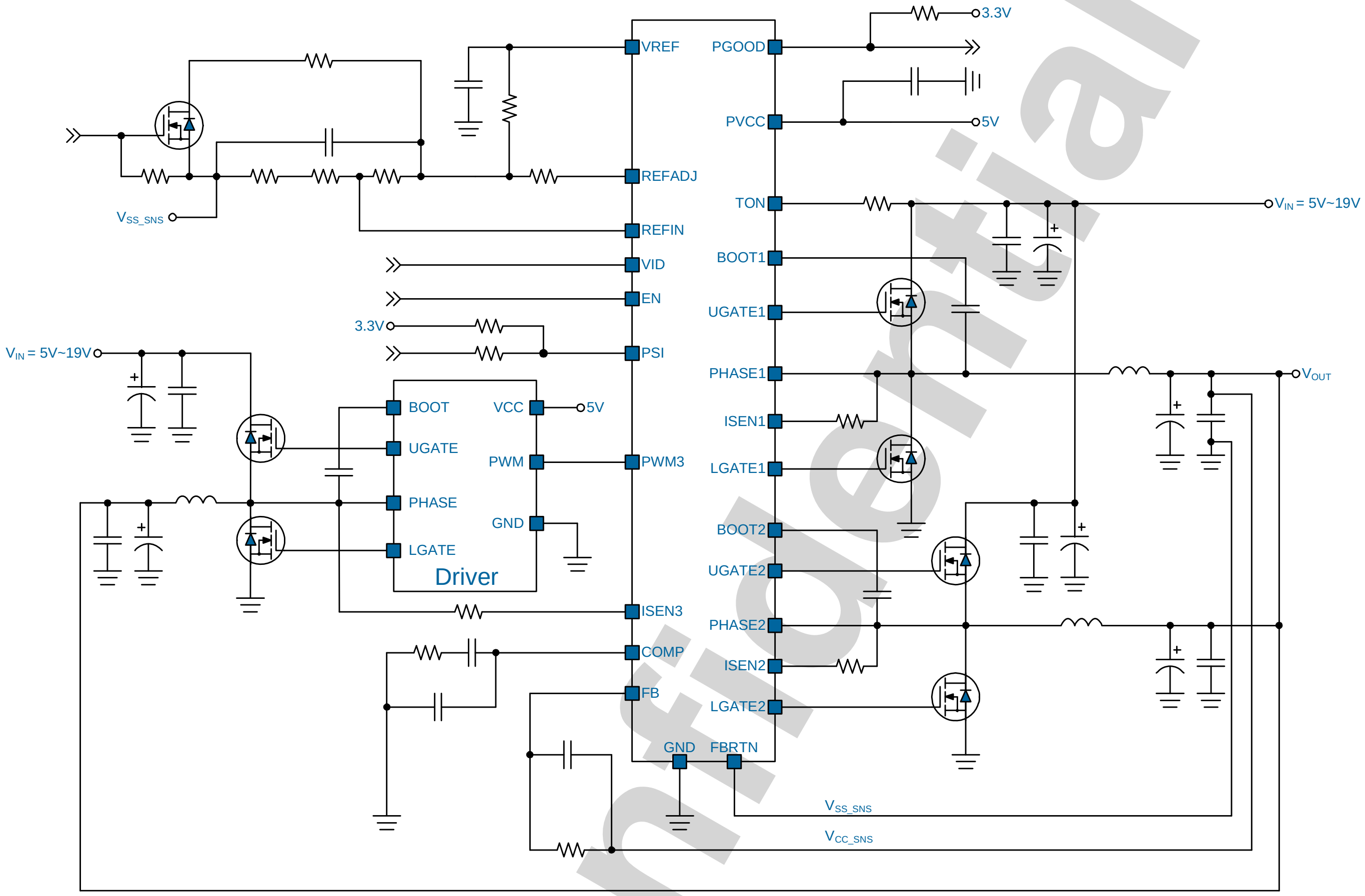
- Support NVIDIA's Open VReg Type-2 and 2+1 PWMVID Technology
- Wide Input Voltage Range 4.5V ~ 26V
- Robust Constant On-Time Control
- 3/2/1 Phase Operation
- Two Integrated MOSFET Drivers with Shoot-Through Protection and Internal Bootstrap Switch
- Adjustable Current Balancing by $R_{DS(ON)}$ Current Sensing
- Adjustable Operation Frequency from 200kHz to 1MHz
- External Compensation
- Support NVIDIA's PWMVID Function
- Dynamic Output Voltage Adjustment
- Temperature Sensing and Thermal Alert
- Power Good Indication
- Over Voltage Protection
- Under Voltage Protection
- Short Circuit Protection
- Over Temperature Protection
- RoHS Compliant and Halogen Free

Pin Configuration



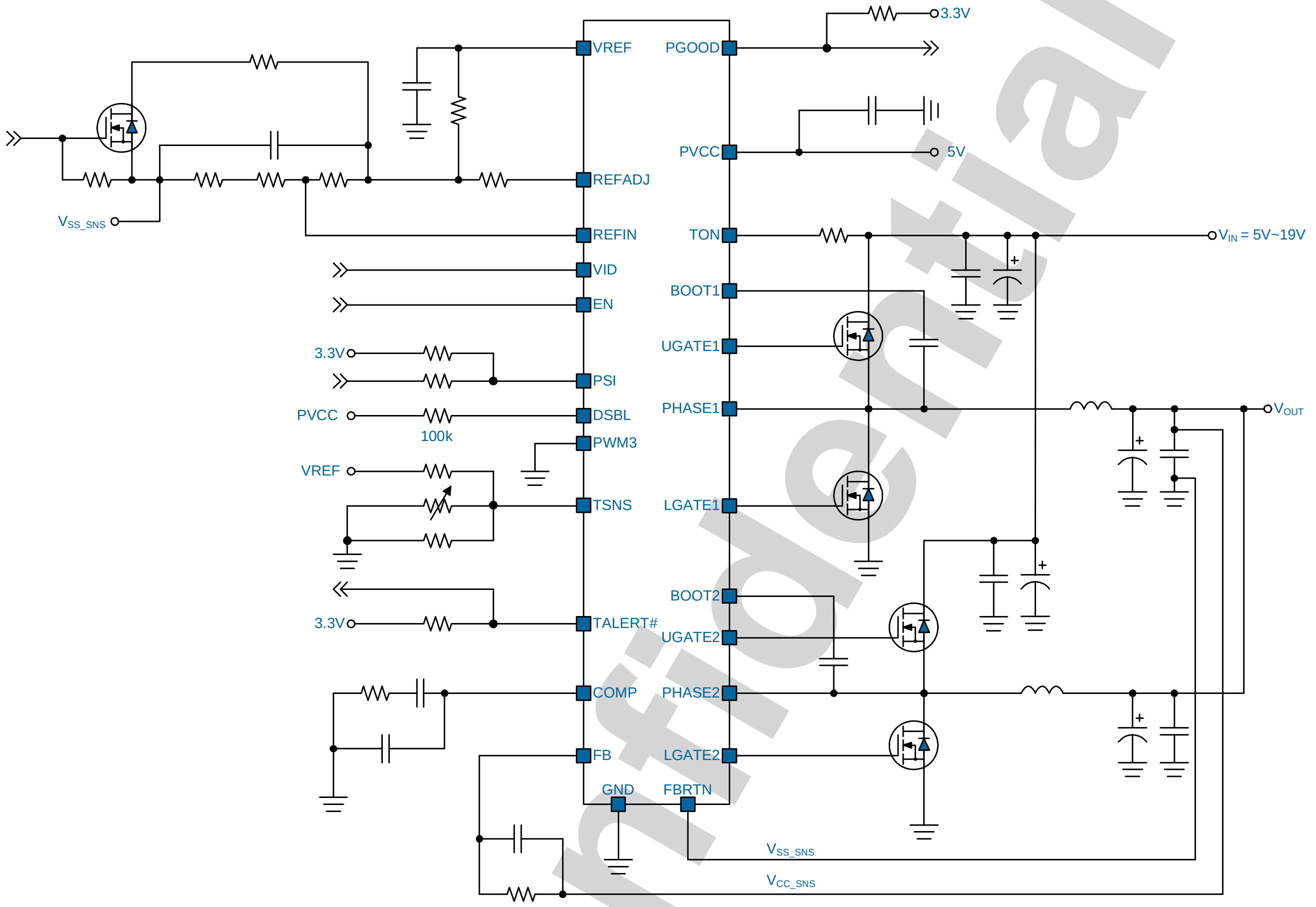
Typical Application Circuit

3-Phase Mode



Typical Application Circuit

2-Phase Mode



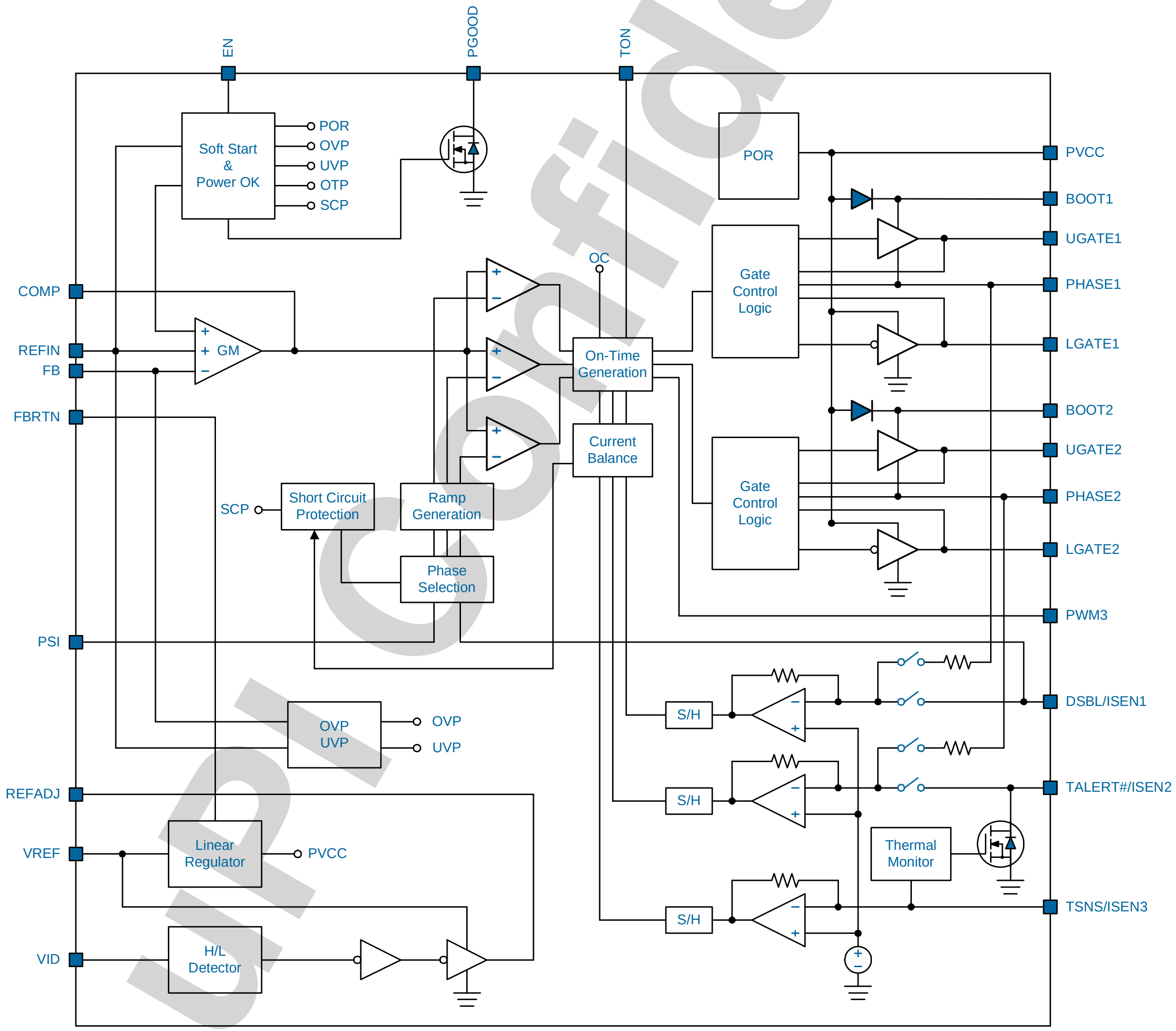
Functional Pin Description

No.	Name	Pin Function
1	BOOT1	**BOOT for Phase 1.** Connect a capacitor form this pin to PHASE1 to form a bootstrap circuit for upper gate driver of the phase 1.
2	UGATE1	**Upper Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 upper MOSFET.
3	EN	**Enable.** Chip enable.
4	PSI	**Power Saving Input.** An input pin receiving power saving control signal from GPU.
5	VID	**VID.** PWMVID input pin.
6	REFADJ	**Reference Adjustment.** PWMVID output pin. Connect this pin with an RC integrator to generate REFIN voltage.
7	REFIN	**Reference Input.** Connect this pin to an external reference voltage through a resistor or connect to the output of the REFADJ circuit. Pulling low this pin down to 0.15V shuts down the uP1642P.
8	VREF	**Reference Voltage.** 2V LDO voltage output pin. Connect an at least 1uF decoupling capacitor between this pin and GND.
9	TON	**On-time Setting Pin.** Connect a resistor from this pin to VIN to set the on-time of the upper MOSFET.
10	FBRTN	**Return for the Reference Circuit.** Connect this pin to the ground point where output voltage is to be regulated.
11	FB	**Feedback Pin.** This pin is the inverting input of the error amplifier.
12	COMP	**Compensation Output.** This pin is the output of the error amplifier.
13	TSNS/ISEN3	**Thermal monitor (2-phase mode) or ISEN3 (3-phase mode).** As thermal monitor pin, connect this pin to an NTC network near power stage to monitor thermal condition of the system. As ISEN3 pin, connect this pin to the phase node of phase 3 with a resistor to sense phase 3 output current.
14	TALERT#/IS-EN2	**TALERT# (2-phase mode) or ISEN2 (3-phase mode).** As TALERT# pin, connect this pin to a voltage source with a pull-up resistor. TALERT# is an active low, open-drain output to indicate high temperature condition. As ISEN2 pin, connect this pin to the PHASE2 pin with a resistor to sense phase 3 output current.
15	DSBL/ISEN1	**DSBL (2-phase mode) or ISEN1 (3-phase mode). If** in 2-phase mode, this pin should be connected to PVCC. If in 3-phase mode, connect this pin to the PHASE1 pin with a resistor to sense phase 1 output current.
16	PGOOD	**Power Good Indication.** Connect this pin to a voltage source with a pull-up resistor. Open-drain structure.
17	UGATE2	**Upper Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 upper MOSFET.
18	BOOT2	**BOOT for Phase 2.** Connect a capacitor form this pin to PHASE2 to form a bootstrap circuit for upper gate driver of the phase 2.
19	PHASE2	**Phase Pin for Phase 2.** This pin is the return path of upper gate driver for phase 2. Connect a capacitor from this pin to BOOT2 to form a bootstrap circuit for upper gate driver of the phase2.
20	LGATE2	**Lower Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 lower MOSFET.

Functional Pin Description

No.	Name	Pin Function
21	PVCC	**Supply Input for the IC.** Voltage power supply of the IC. Connect this pin to a 5V supply and decouple using at least a 0.1uF ceramic capacitor.
22	PWM3	**PWM Output of Phase 3**. Connect this pin to the PWM input pin of the companion gate driver. Connect this pin to GND when maximum 2 phase operation.
23	LGATE1	**Lower Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 lower MOSFET.
24	PHASE1	**Phase Pin for Phase 1.** This pin is the return path of upper gate driver for phase 1. Connect a capacitor from this pin to BOOT1 to form a bootstrap circuit for upper gate driver of the phase 1.
25	Exposed Pad	**Ground.** Tie this pin to ground island/plane through the lowest impedance connection available.

Functional Block Diagram



Functional Description

The uP1642P is a 3/2/1-phase synchronous-rectified buck controller specifically designed to work with 4.5V ~ 26V input voltage and deliver high quality output voltage for high-performance graphic processor power.

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Other features include accurate and reliable short-circuit protection, adjustable on-time setting, power saving control input, and a power good output. This part is available in VQFN4x4 - 24L package.

Supply Input and Power On Reset

The uP1642P receives supply input from PVCC pin to provide current to gate drivers and internal control circuit. PVCC is continuously monitored for power on reset. The POR level is typical 4.1V at rising. The TON pin voltage is used for on-time calculation and should be connected to the supply input of power stage.

The uP1642P integrates floating MOSFET gate driver that are powered from the PVCC pin. A bootstrap switch is embedded to facilitates PCB design and reduce the total BOM cost. No external Schottky diode is required in real applications. An external Schottky diode with lower voltage drop can improve the power conversion efficiency.

Phase Number of Operation (Hard-wire Programming)

The uP1642P supports 3/2/1 phase operation. The maximum phase number of operation is determined by checking the DSBL/ISEN1 status when POR. If DSBL/ISEN1 is connected to a voltage source higher than (PVCC-1V) during POR, the uP1642P enters 2-phase operation. Tie DSBL/ISEN1 by a 100kΩ resistor to PVCC for maximum 2-phase configuration where phase3 is disabled. In 2-phase operation, pin 13 is auto-switched to TSNS pin, and pin 14 is auto-switched to TALERT# pin. Once selected, the maximum phase number of operation is latched and can only be changed at the next POR.

Constant On-Time Setting

The uP1642P adopts a compensated constant-on-time control scheme. A resistor R_{TON} connected to TON pin programs the constant on time according to the equation:

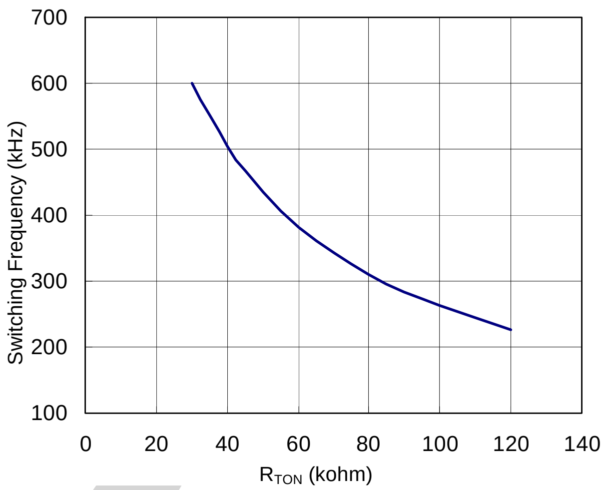


Figure 1. Switching Frequency vs. R_{TON}

$$T_{ON} = 300 \times \frac{R_{TON} + 18k\Omega}{9k\Omega} \times \frac{V_{REFIN}}{V_{IN}} \text{ (ns)}$$

where R_{TON} is in kΩ, V_{IN} is the supply input voltage and V_{REFIN} is the input voltage at the REFIN pin.

Voltage Control Loop and PWMVID Function

Figure 2 illustrates the voltage control loop of the uP1642P. FB and REFIN are negative and positive inputs of the Error Amplifier respectively. The Error Amplifier modulates the COMP voltage V_{COMP} of buck converter to force FB voltage V_{FB} follows V_{REFIN}.

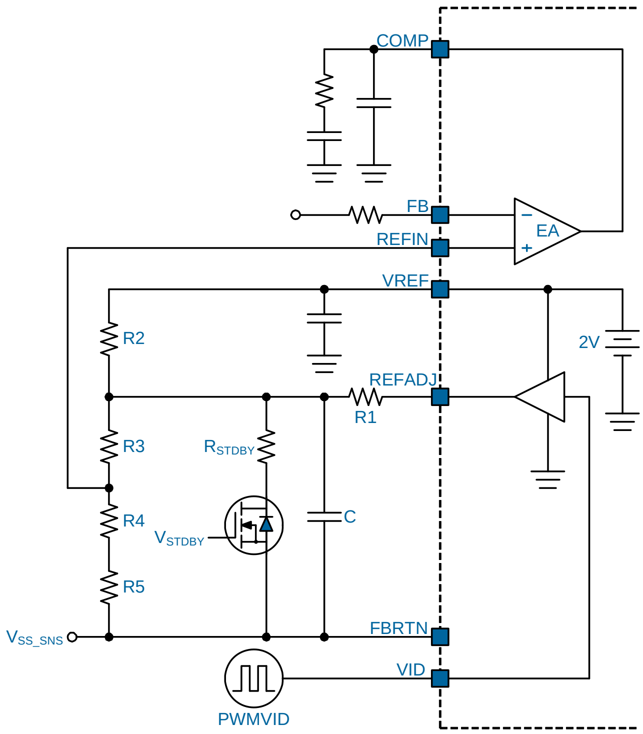


Figure 2. Voltage Control Loop

The PWMVID signal from GPU is applied to the VID pin, which is the input pin of the internal buffer. This buffer plays the role of level shifting, and the output of this buffer is injected into the external RC integrator to generate REFIN voltage, which can be calculated as:

$$V_{REFIN} =$$

$$V_{VREF} \times D \times \frac{R2//(R3+R4+R5)}{R1+R2//(R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5} +$$

$$V_{VREF} \times \frac{R1//(R3+R4+R5)}{R2+R1//(R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5}$$

where $V_{REFIN,DC}$ is the DC voltage of REFIN, V_{VREF} is the voltage of VREF (typically 2V), and D is the duty cycle of PWMVID input.

Boot Voltage and Standby Mode

The new generation PWMVID structure includes two operation modes other than normal operation: boot mode and standby mode. During boot mode, the GPU stops sending PWMVID signal and the input of the PWMVID buffer is floating. The REFADJ pin enters high impedance state after the VID pin enters tri-state region, and the REFIN voltage can then be calculated as:

$$V_{REFIN,BOOT} = V_{VREF} \times \frac{R4+R5}{R2+R3+R4+R5}$$

During standby mode, other than GPU stopping the PWMVID transaction, an external system standby signal additionally controls the entry of standby mode. An additional external switch should be connected in parallel with the original PWMVID resistors as shown in Figure 3 to generate the standby mode voltage:

$$V_{REFIN,STDBY} =$$

$$V_{VREF} \times \frac{(R3+R4+R5)//R_{STDBY}}{R2+(R3+R4+R5)//R_{STDBY}} \times \frac{R4+R5}{R3+R4+R5}$$

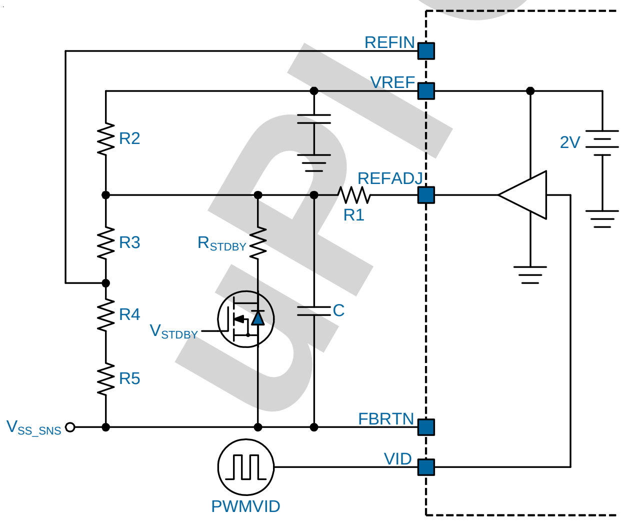


Figure 3. Standby Mode Configuration

Channel Current Balance

The uP1642P senses phase currents for current balance by the means of on-resistance of power stage low-side MOSFET as shown in Figure 4.

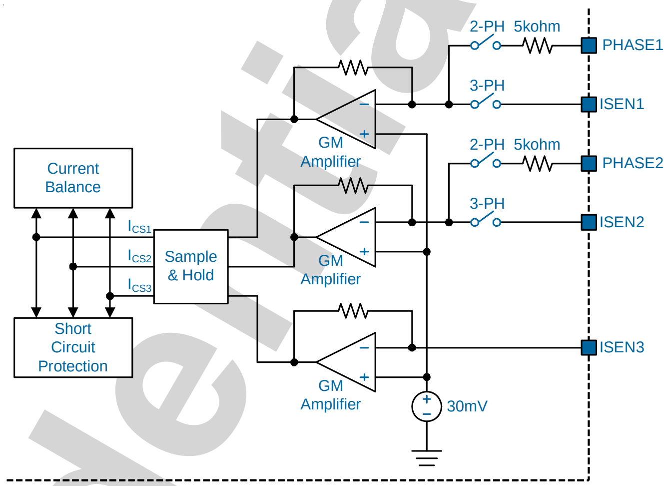


Figure 4. $R_{DS(ON)}$ Current Sensing Scheme

The GM amplifier senses the voltage drop across the low-side MOSFET and converts it into current signal each time it turns on. The sampled and held current is expressed as:

$$I_{CSX} = \frac{(I_{LX} \times R_{DS(ON)} + V_{DC})}{R_{ISENX}}$$

where I_{LX} is the phase X current in Ampere, $R_{DS(ON)}$ is the on-resistance of low-side MOSFET of the power stage in mΩ, V_{DC} is an internal 30mV voltage source, and R_{ISENX} is the external sensing resistor connected at ISENx pins. In maximum 3-phase operation, the R_{ISENX} is determined by external ISEN resistors. In maximum 2-phase operation, the ISEN pins are auto-switched into multi-function pins (TSNS and TALERT#), and the current sense resistors are also auto-switched into the internal R_{ISEN} resistors. The resistance of the internal R_{ISEN} resistors during maximum 2-phase operation is 5kΩ. In this current sense mechanism, the valley of the inductor current is sampled and held. Therefore, the equivalent sensed current can be described by the following equation:

$$I_{LX\_SH} = I_{LX\_AVG} - \frac{1}{2} \times \Delta I_{LX}$$

The sensed current I_{LX_SH} is mirrored to the current balance circuit, comparing between each other, and generating current adjusting signals for each phase. These current adjusting signals are fed to the on-time circuit of the uP1642P to separately adjust each phase on-time for the purpose of adjusting current balance.

Soft-Start and Power Good

A built-in soft-start is used to prevent surge current from power supply input during turn on. The error amplifier is a three-input device. Reference voltage V_{REFIN} or the internal soft-start voltage SS whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. SS internally ramps up to PVCC with a slew rate determined by V_{REFIN} after the soft start cycle is initiated. Accordingly, the output voltage will follow the SS signal and ramp up smoothly to its target level. The output voltage ramp-up time is typically 1.4ms.

Power Saving Mode

The uP1642P provides power saving features for platform designers to program platform specific power saving configuration. There are four operation modes: multi-phase CCM, single-phase USM, single-phase FCCM, and single-phase PSM. The uP1642P switches between these four operation modes according to the input voltage level of the PSI pin. Figure 5 shows typical PSI application circuit, and table 1 shows recommended PSI setting voltage level of four operation modes. In single-phase operation, the uP1642P auto-selects phase 1 to be the operating phase. In PSM, the uP1642P automatically reduces switching frequency at light load to maintain high efficiency. As the load current decreases, the rectifying MOSFET is turned off when zero inductor current is detected, and the converter runs in discontinuous conduction mode. In USM, the operation of the converter is also a discontinuous conduction mode similar to PSM, and additionally the USM control circuit monitors both high-side and low-side MOSFETs and force to change into the ON state to avoid the switching frequency falling within audible region.

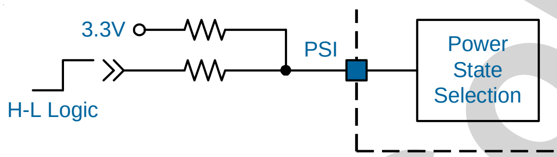


Figure 5. PSI application circuit

Operation Mode	Recommended Voltage Setting at PSI
Multi-Phase CCM	3.3V
Single-Phase USM	2V
Single-Phase FCCM	1.2V
Single-Phase PSM	GND

Table 1. Recommended PSI Setting

Thermal Alert Function

By pulling pin 15 to PVCC, the uP1642P operates in 2-phase mode and the thermal alert function is enabled on pin 14 (TALERT#) and pin 13 (TSNS). Figure 6 shows typical settings of the thermal alert function. A resistive voltage divider with NTC linearization network forms a typical TSNS setting. The pull-up voltage of the TSNS pin must be the VREF (2V) voltage generated by the uP1642P to guarantee the accuracy of the thermal alert function. When the sensed temperature rises, the TSNS voltage falls along with the resistance change of the NTC. When the TSNS voltage falls below 35% of VREF, the TALERT# is asserted (low active). There is a 7.5% hysteresis of TSNS voltage to prevent false trigger of TALERT#.

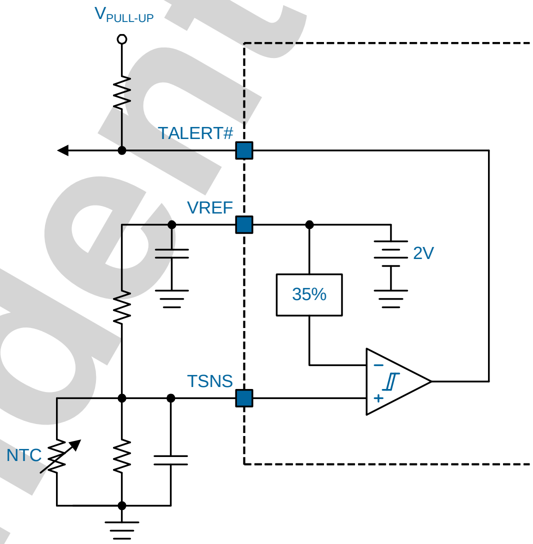


Figure 6. Thermal Alert Function

Short Circuit Protection (SCP)

The uP1642P adopts per-phase current short circuit protection function to avoid catastrophic damage to power stage components. The uP1642P monitors the sensed current at ISENx pins and if the sensed I_{CSX} of any phase exceeds 37.5uA, the short circuit protection activates. According the mentioned current sense equation, the short circuit protection equation can be written as:

$$I_{MAX,per-phase} = \frac{37.5uA \times R_{ISENX} - V_{DC}}{R_{DS(ON)}}$$

Where 37.5uA is the internal SCP threshold current, R_{ISENX} is the external sensing resistor connected at ISENx pins, V_{DC} is an internal 30mV voltage source, and $R_{DS(ON)}$ is the on-resistance of the low-side MOSFET of the power stage in mΩ. Since the SCP mechanism detects per-phase current for SCP triggering, the total SCP threshold can be calculated as:

$$I_{MAX,total} = P \times \frac{(37.5uA \times R_{ISENX} - V_{DC})}{R_{DS(ON)}}$$

where P denotes operating phase number.

In maximum 3-phase operation, the R_{ISENX} is determined by external ISEN resistors. In maximum 2-phase operation, the ISEN pins are auto-switched into multi-function pins (TSNS and TALERT#), and the current sense resistors are also auto-switched into the internal R_{ISEN} resistors. The resistance of the internal R_{ISEN} resistors during maximum 2-phase operation is 5kΩ.

After per-phase current exceeds SCP threshold and sustained 6us, the short circuit protection is triggered and shuts down the uP1642P and turns off all high-side and low-side MOSFETs if any phase's current exceeds I_{MAX}, and this latched-off protection can only be reset by PVCC re-POR or EN restart.

Over Voltage Protection (OVP)

The OVP is triggered if $V_{FB} > 1.4xV_{REFIN}$ sustained 6us. When OVP is activated, the uP1642P turns on all low-side MOSFET and turns off all high-side MOSFET. The over voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Under Voltage Protection (UVP)

The under voltage protection is triggered if $V_{FB} < 0.5xV_{REFIN}$ sustained 10us. When UVP is activated, the uP1642P turns off all high-side and low-side MOSFET. The under voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Over Temperature Protection (OTP)

The uP1642P monitors the temperature of itself. If the temperature exceeds typical 150^{O}C, the uP1642P is forced into shutdown mode. The over temperature protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, PVCC ---------- -0.3V to +6.5V

BOOTx to PHASEx

DC ---------- -0.3V to +6V

PHASEx to GND

DC ---------- -0.7V to +28V

<200ns ---------- -8V to +36V

BOOTx to GND

DC ---------- -0.3V to (V_{PVCC}+36V)

<200ns ---------- -0.3V to +42V

UGATEx to PHASEx

DC ---------- -0.3V to (BOOTx-PHASEx+0.3V)

<200ns ---------- -5V to (BOOTx-PHASEx+0.3V)

LGATEx to GND

DC ---------- -0.3V to (V_{PVCC}+0.3V)

<200ns ---------- -5V to (V_{PVCC}+0.3V)

Other Pins ---------- -5V to (V_{PVCC} + 0.3V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

HBM (Human Body Mode) ---------- 2kV

MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

VQFN4x4 - 24L θ_{JA} ---------- 40°C/W

VQFN4x4 - 24L θ_{JC} ---------- 4°C/W

Power Dissipation, P_D @ T_A = 25°C

VQFN4x4 - 24L θ_{JC} ---------- 2.5W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Input Voltage, V_{IN} ---------- 3V to 26V

Electrical Characteristics

(PVCC = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Current	I_{PVCC}	V_{REFIN} = 0.9V, EN = 3.3V, V_{FB} = 1V, no switching	--	2	--	mA
Shutdown Current	I_{SHDN}	EN = 0V	--	2	--	uA
PVCC POR Threshold	$V_{PVCCRTH}$	V_{PVCC} rising, T_A = 0°C to 85°C	3.9	4.1	4.3	V
PVCC POR Hysteresis	$V_{PVCCHYS}$		--	0.3	--	V
VREF Voltage Accuracy		T_A = 0°C to 85°C	1.98	2	2.02	V
VREF Maximum Output Current			10	--	--	mA
Control Input: EN						
Logic Low Threshold		T_A = 0°C to 85°C	--	--	0.8	V
Logic High Threshold		T_A = 0°C to 85°C	2.4	--	--	V
Internal Pull-down Current			--	10	--	uA
Reference Voltage						
REFIN Disable Threshold		T_A = 0°C to 85°C	--	--	0.13	V
External Rererence Voltage Range	V_{REFIN}		0.27	--	2	V
On Time						
One Shot Width	T_{ON}	V_{OUT} = 1.1V, R_{TON} = 75kΩ, V_{IN} = 12V	--	280	--	ns
Minimum Off Time	T_{OFF_MIN}		--	350	--	ns
USM Frequency						
USM Frequency	f_{USM}	USM	25	--	--	kHz
PWM3 Output						
Output Low Voltage	V_{OL}	I_{SINK} = 4mA, T_A = 0°C to 85°C	--	--	0.5	V
Output High Voltage	V_{OH}	I_{SRC} = 4mA, T_A = 0°C to 85°C	4.5	--	--	V
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	30	--	--	MHz
Slew Rate	SR	Guaranteed by Design	3	6	--	V/us
Trans-conductance	GM	R_{LOAD} = 20kΩ	--	1800	--	uA/V
Maximum Current (Source & Sink)	I_{COMP}	V_{COMP} = 1.6V	250	300	--	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Current Sense Amplifier						
Input Offset Voltage	V_{OS}		-1	--	1	mV
Max Sourcing Current			100	--	--	uA
ISENx Voltage		R_{ISENx} = 5kΩ for internal appliction, T_A = 0°C to 85°C	25	30	35	mV
FBRTN						
FBRTN Current	I_{FBRTN}	EN = 3.3V, no switching	--	--	500	uA
Soft Start						
Soft Start Period	T_{SS}	From EN = high to PGOOD = high	--	1.4	--	ms
PWMVID Buffer						
VID Input Low Level	V_{OL}		--	1	--	V
VID Input High Level	V_{OH}		--	2	--	V
VID Tri-state Delay			--	100	--	ns
REFADJ Output Low Voltage	V_{IL}	I_{SINK} = 1mA, T_A = 0°C to 85°C	0	--	0.05	V
REFADJ Output High Voltage	V_{IH}	I_{SRC} = 1mA, T_A = 0°C to 85°C	1.95	--	2	V
VREFADJ Source Resistance	R_{BF_SRC}	I_{SRC} = 1mA, T_A = 0°C to 85°C	10	20	30	Ω
VREFADJ Sink Resistance	R_{BF_SNK}	I_{SNK} = 1mA, T_A = 0°C to 85°C	10	20	30	Ω
PSI						
Power Saving Input Threshold	V_{PSI}	Multi-phase CCM, T_A = 0°C to 85°C	52	--	--	% of PVCC
		USM, T_A = 0°C to 85°C	36	--	44	% of PVCC
		Single-phase FCCM, T_A = 0°C to 85°C	20	--	28	% of PVCC
		PSM, T_A = 0°C to 85°C	--	--	12	% of PVCC
Gate Drivers						
Upper Gate Source	R_{UG_SRC}	I_{UG} = -80mA	--	1	2	Ω
Upper Gate Sink	R_{UG_SNK}	I_{UG} = 80mA	--	0.5	1	Ω
Lower Gate Source	R_{LG_SRC}	I_{LG} = -80mA	--	1	2	Ω
Lower Gate Sink	R_{LG_SNK}	I_{LG} = 80mA	--	0.4	0.8	Ω
Dead Time	T_{DT}		--	30	--	ns
Internal Bootstrap Switch						
On Resistance	R_{ST}	I_F = 10mA	--	80	--	Ω
Reverse Leakage Current	I_{ST}	V_{BOOTX} = 26V	--	0.01	1.5	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Zero Current Detection Threshold						
Zero Current Threshold	V_{ZC}	GND-PHASE	--	2	--	mV
Protection						
Short Circuit Protection Threshold Level	I_{ISENx}	R_{ISENx} = 5kΩ, T_A = 0°C to 85°C	--	37.5	--	uA
OVP Threshold	V_{OVP}	V_{FB}/V_{REFIN}, T_A = 0°C to 85°C	130	--	150	%
UVP Threshold	V_{UVP}	V_{FB}/V_{REFIN}, T_A = 0°C to 85°C	45	--	55	%
OTP Threshold		T_A = 0°C to 85°C	150	--	170	°C
Temperature Monitor						
TALERT# Threshold Level	V_{TSNS}	TALERT# high to low	33	35	37	% of VREF
TALERT# Hysteresis	V_{TSNS_HYS}	TALERT# low to high hysteresis	--	7.5	--	% of VREF
Power Good Indicator						
Power Good Indicator		I_{SINK} = 4mA	--	--	0.3	V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

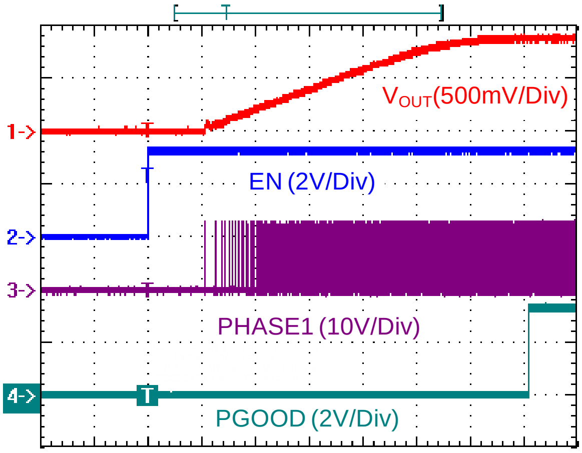
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

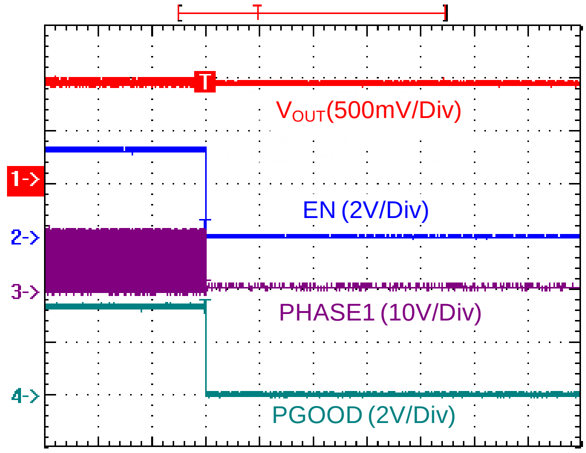
Typical Operation Characteristics

Power On



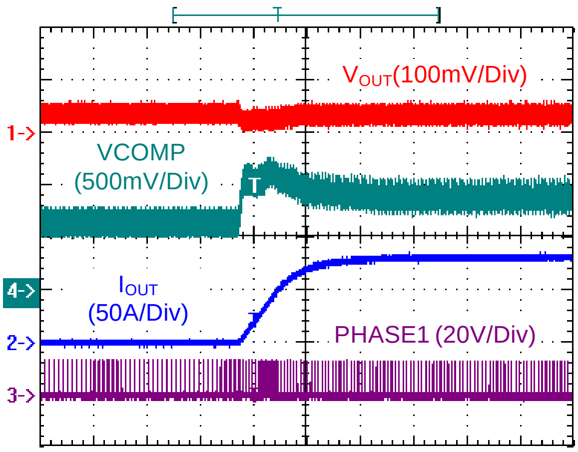
200us/Div
V_{IN} = 12V, no load

Power Off



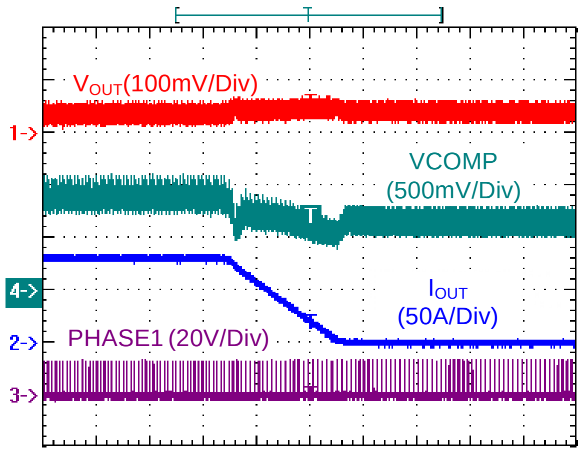
200us/Div
V_{IN} = 12V, no load

Load Transient: Undershoot



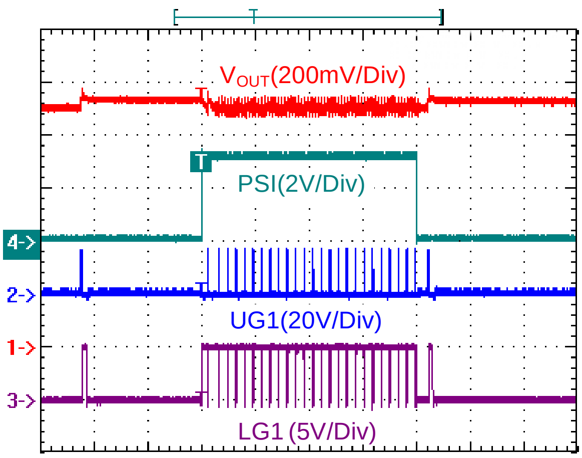
40us/Div
V_{IN} = 12V, V_{CC} = 5V

Load Transient: Overshoot



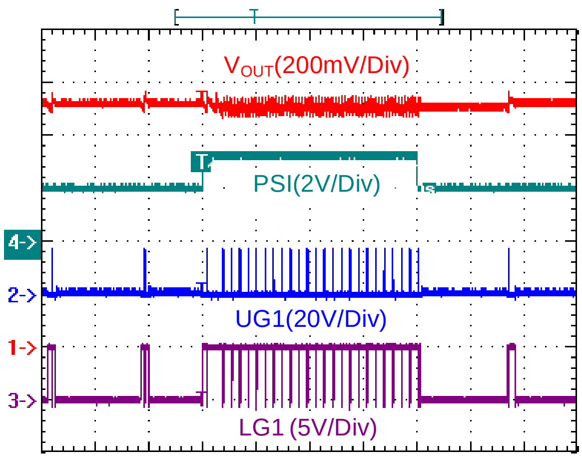
40us/Div
V_{IN} = 12V, V_{CC} = 5V

PSI Toggle: PSM & Multi-Phase



20us/Div
V_{IN} = 12V, no load

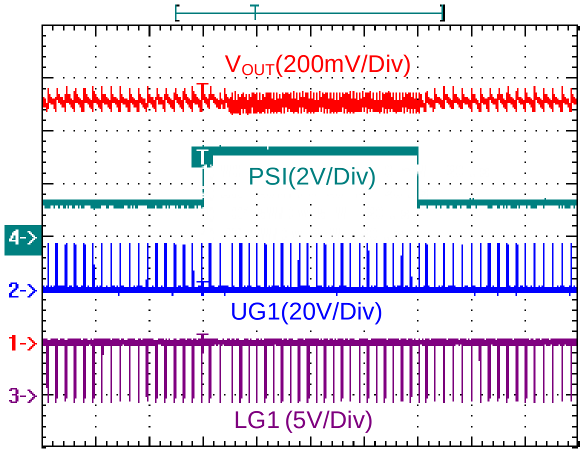
PSI Toggle: USM & Multi-Phase



20us/Div
V_{IN} = 12V, no load

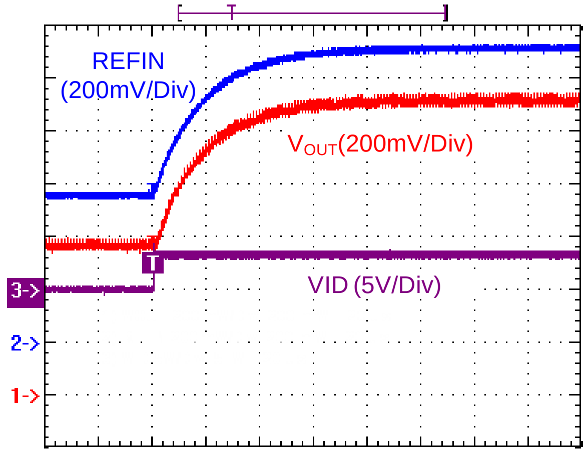
Typical Operation Characteristics

PSI Toggle: CCM & Multi-Phase



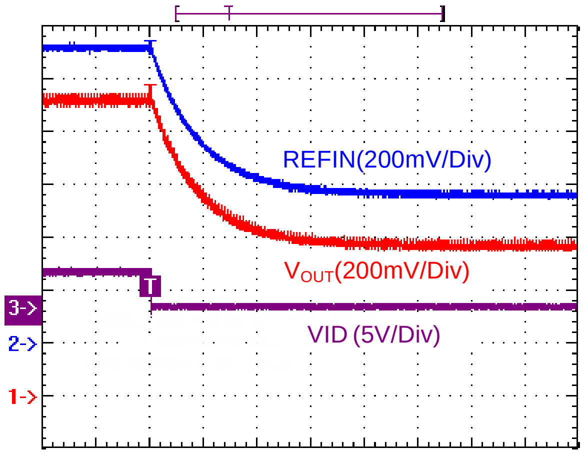
20us/Div
V_{IN} = 12V, no load

VID: PWM 100% to 0%



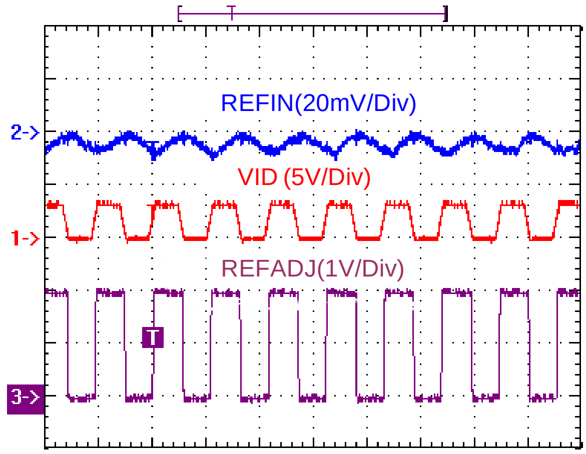
20us/Div
V_{IN} = 12V, no load

VID: PWM 100% to 0%



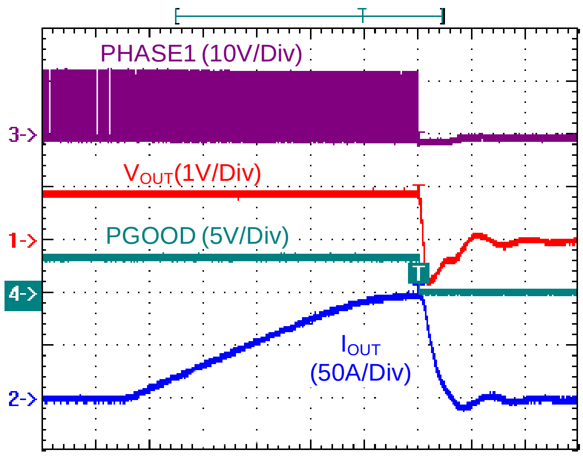
20us/Div
V_{IN} = 12V, no load

PWMVID: 50%, 931KHz



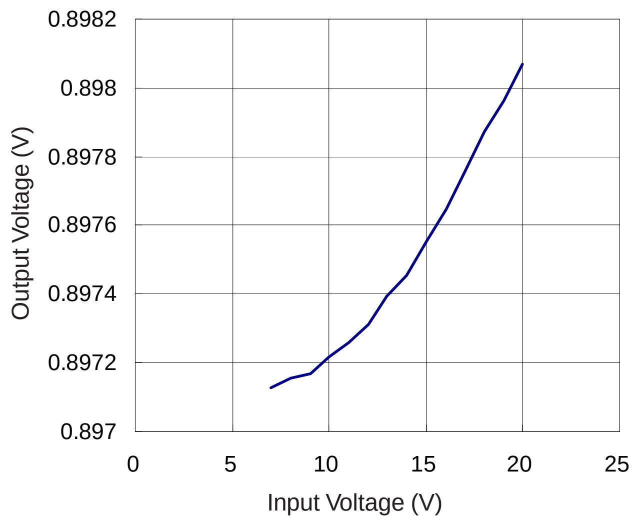
1us/Div
V_{IN} = 12V, V_{CC} = 5V

SCP



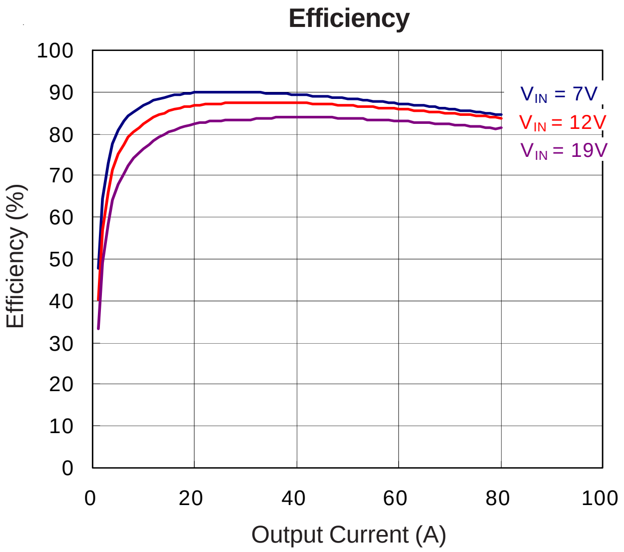
100us/Div
R_{ISEN1} = R_{ISEN2} = R_{ISEN3} = 1.65kΩ

Line Regulation



V_{CC} = 5V

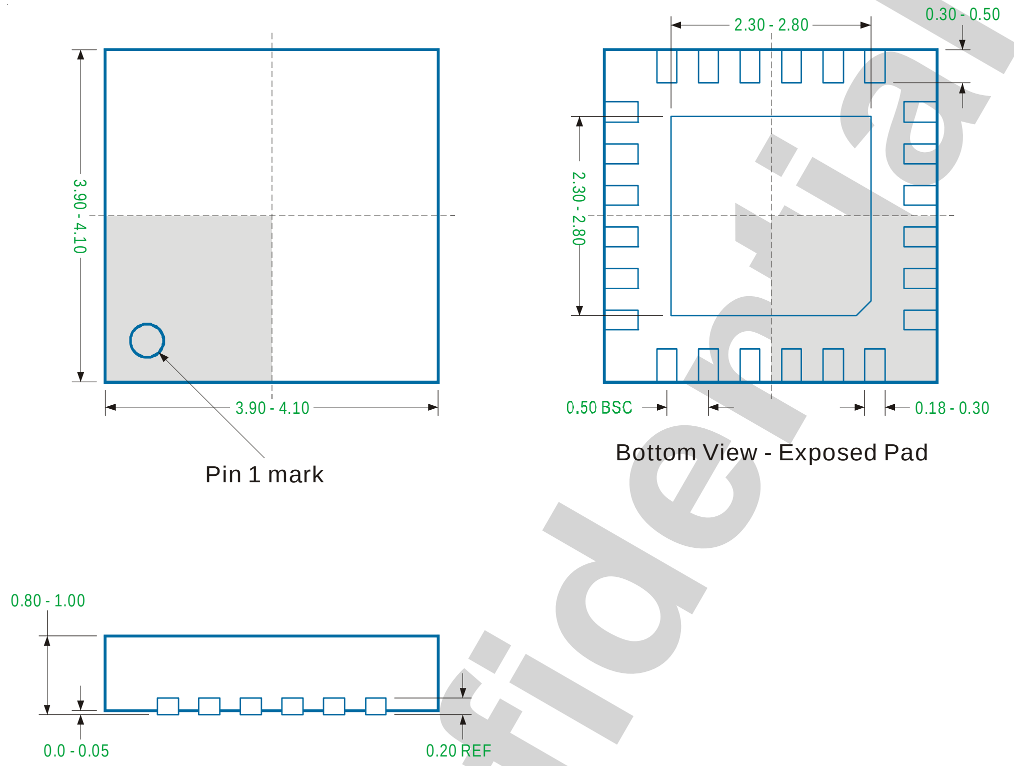
Typical Operation Characteristics



V_{CC} = 5V, MOSFETs: CSD87350*2 per phase
R_{TON}: 91kΩ

Package Information

VQFN4x4 - 24L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

uPI Semiconductor Corp.

Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666   FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062   FAX : 886.2.8751.5064