

Change List

HK5_MB_SCH_PVT_001
P21--Add LQ2[CHT2301PT],LR18[47K],LC27[0.01UF],LC26[1U].
P21--No mount LR15[0 ohm].
P21--LR16 pin1 connect to "+3V_S5".

Reason : Modify circuit for LAN power Rise time.
Possible Risk: No.

HK5_MB_SCH_PVT_002
P22--Delete R409[3.01K].
P22--U29 value change to "G5240/TPS2051".
Reason : Modify circuit for K/B Backlight protect.
Possible Risk: No.

HK5_MB_SCH_PVT_003
P4--Delete R332[0 ohm].
P5--Delete R171[0 ohm].
P6--Delete R189,R186,R197[0 ohm].
P8--Delete R438,R38,R37,R439[0 ohm].
P9--Delete R121,R67,R65,R122[0 ohm].
P10--Delete R73[0 ohm].
P12--Delete R102,R126,R299,R302[0 ohm]
P14--Delete R312[0 ohm]
P15--Delete R309[0 ohm]
P16--Delete KR39,KR60,KR6,KR30[0 ohm]
P18--Delete ML1,MR5[0 ohm]
P21--Delete LR12[0 ohm]
P22--Delete R96[0 ohm]
P23--Delete R461 ,R462
P24--Delete AL1,AR21,AR8,AR23,AR24,AR25,AR22,AR15,AR16,AR17,AL3,AL4,R418,AR20[0 ohm]
P27--Delete PR490,PR502[0 ohm]
P31--Delete PR504[0 ohm]
Reason : Cancel 0 ohm.
Possible Risk: No.

HK5_MB_SCH_PVT_004
P27--Delete PR513.
Reason : Cancel 0 ohm.
Possible Risk: No.

HK5_MB_SCH_PVT_005
P26--PR100,PR108,PR109 change to short PAD.
P27--PR325,PR318,PR324,PR326 change to short PAD.
P28--PR352,PR356,PR360,PR357,PR358 change to short PAD.
P30--PR388,PR390,PR392 change to short PAD.
P31--PR413,PR429,PR430,PR440,PR441 change to short PAD.
P33--PR271 change to short PAD.

Reason : Cancel 0 ohm.
Possible Risk: No.

HK5_MB_SCH_PVT_006
P23--reserve D9 and D10
Reason : reserve ESD diode
Possible Risk: No.

HK5_MB_SCH_PVT_007
P25--change CON1 form 12Pin to 10pin
Reason : delete samll board LID fuction
Possible Risk: No.

HK5_MB_SCH_PVT_008
P42-- Del J5,J6,J7,J8,J9,J10 for EMI request
Reason : For EMI
Possible Risk:
No.

HK5_MB_SCH_PVT_009
P23-- Delete reserve ESD diode D23 ,D24
Reason : ESD test PASS , we don't need to reserve
Possible Risk: No.

HK5_MB_SCH_PVT_010
P23-- change ODD ESD diode form Rclamp0502n to SR05
Reason : for SMT issue , Rclamp0502n easy to short , we change to SR05 and still reserve it
Possible Risk: No.

HK5_MB_SCH_PVT_011
P25-- change R225 form 150ohm to 40.2ohm
Reason : for W/L LED dark issue
Possible Risk: No.

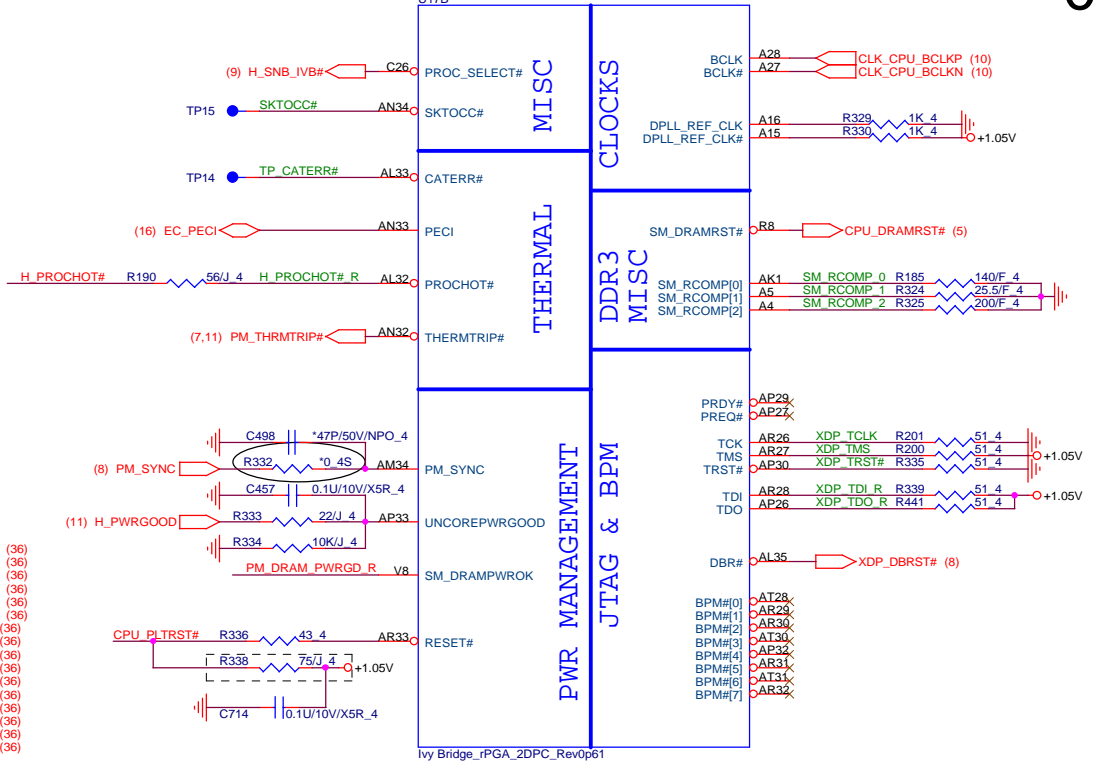
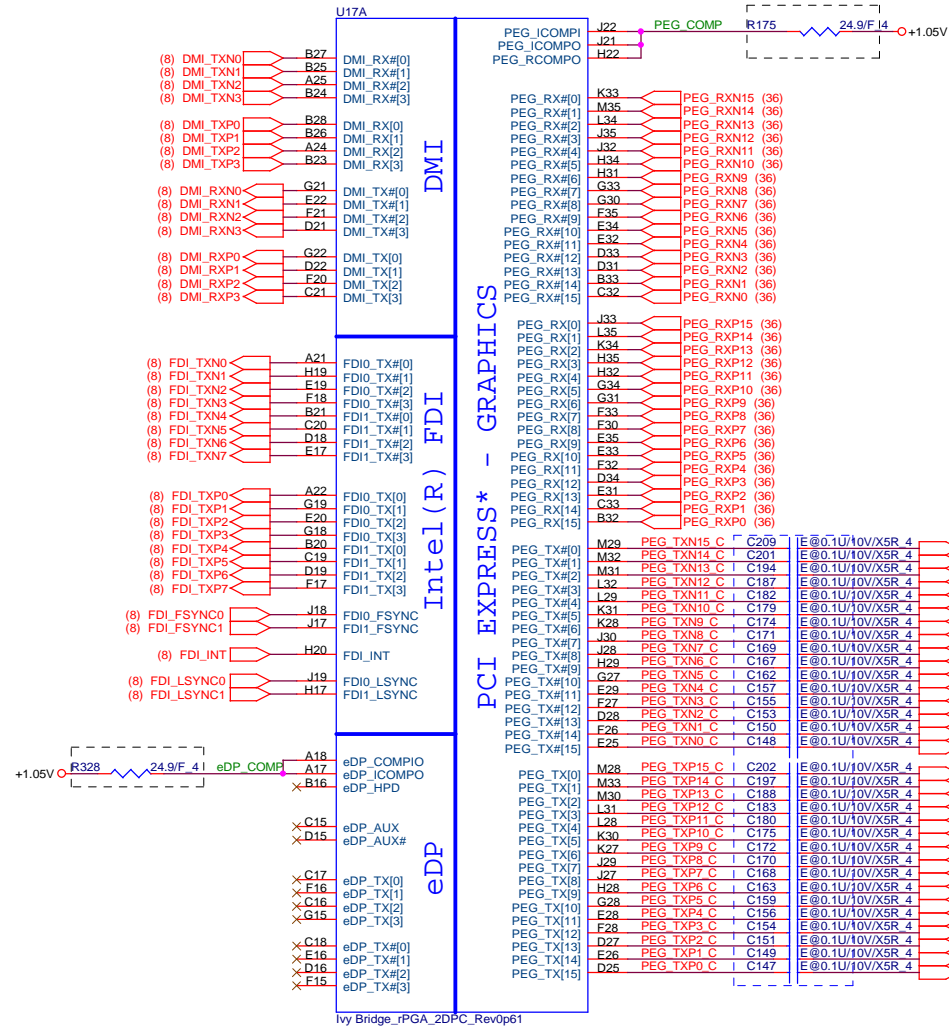
HK5_MB_SCH_PVT_012
P25-- change R224 R226 R349 form 150ohm to 75ohm
Reason : for HDD ,Battery and card reader LED dark issue
Possible Risk: No.

HK5_MB_SCH_PVT_013
P23-- add R461 ,R462 [0ohm]
Reason : customer requirement for TP SMBUS signal
Possible Risk: No.

Ivy Bridge Processor (DMI,PEG,FDI)

Ivy Bridge Processor (CLK,MISC,JTAG)

04



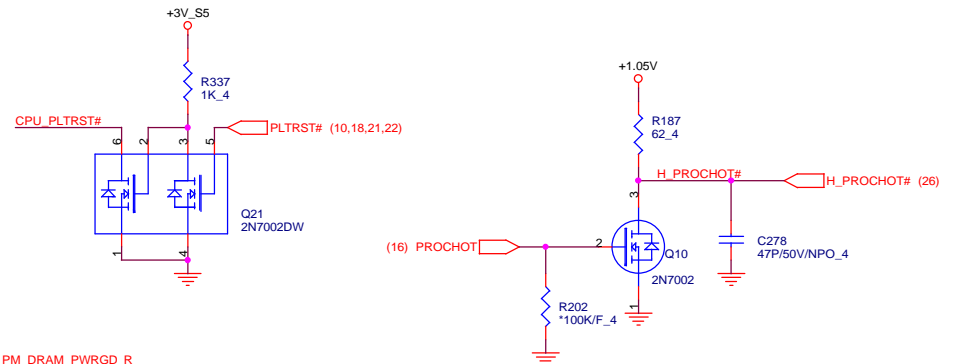
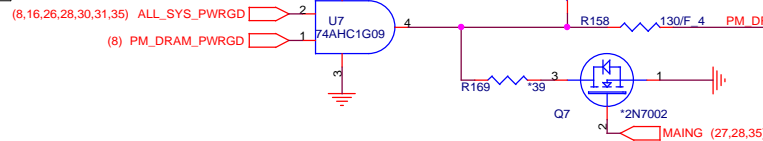
SNB_IVB#:

- It is NC when using Sandy Bridge.(1.05V)
- For next generation processor it will be grounded.(1.0V)

FDI Disabling (Discrete Only)

FDI_FSYNC (J18/J17/J19/H17) can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

FDI_INT connect to GND with 1K ohm.

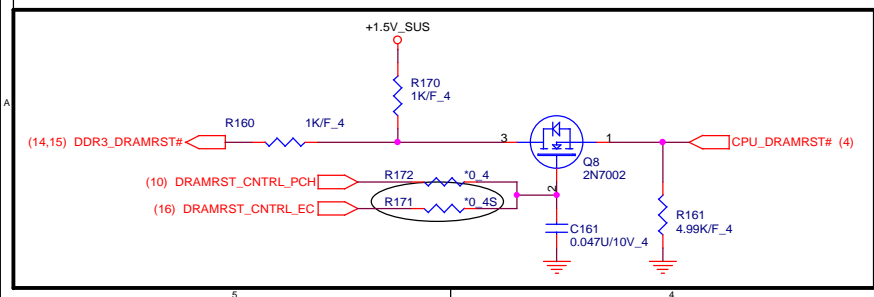
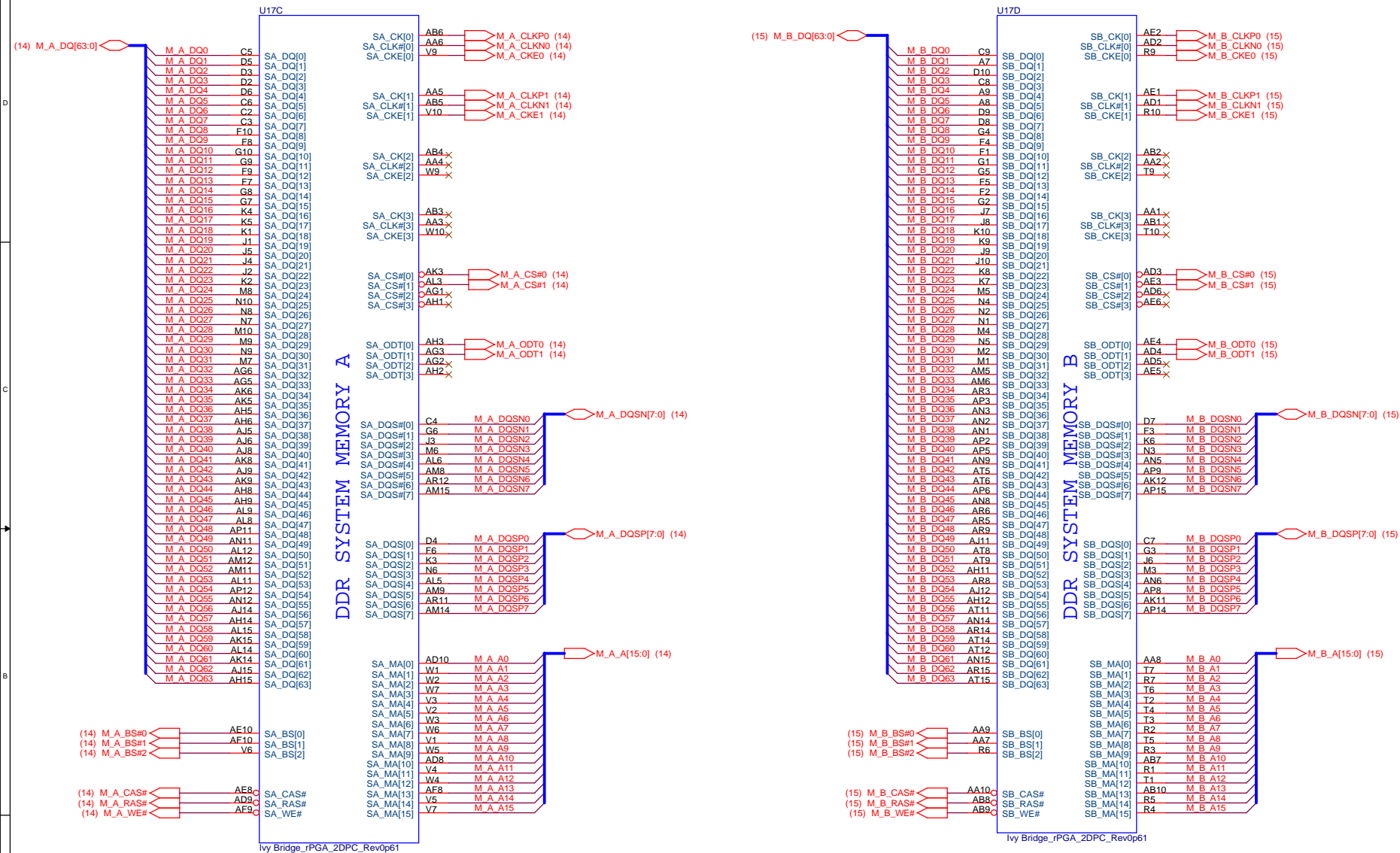


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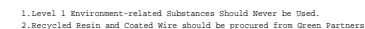
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SNB/IVB 1/4
Date: Wednesday, February 01, 2012 Sheet 4 of 43
Rev 1A

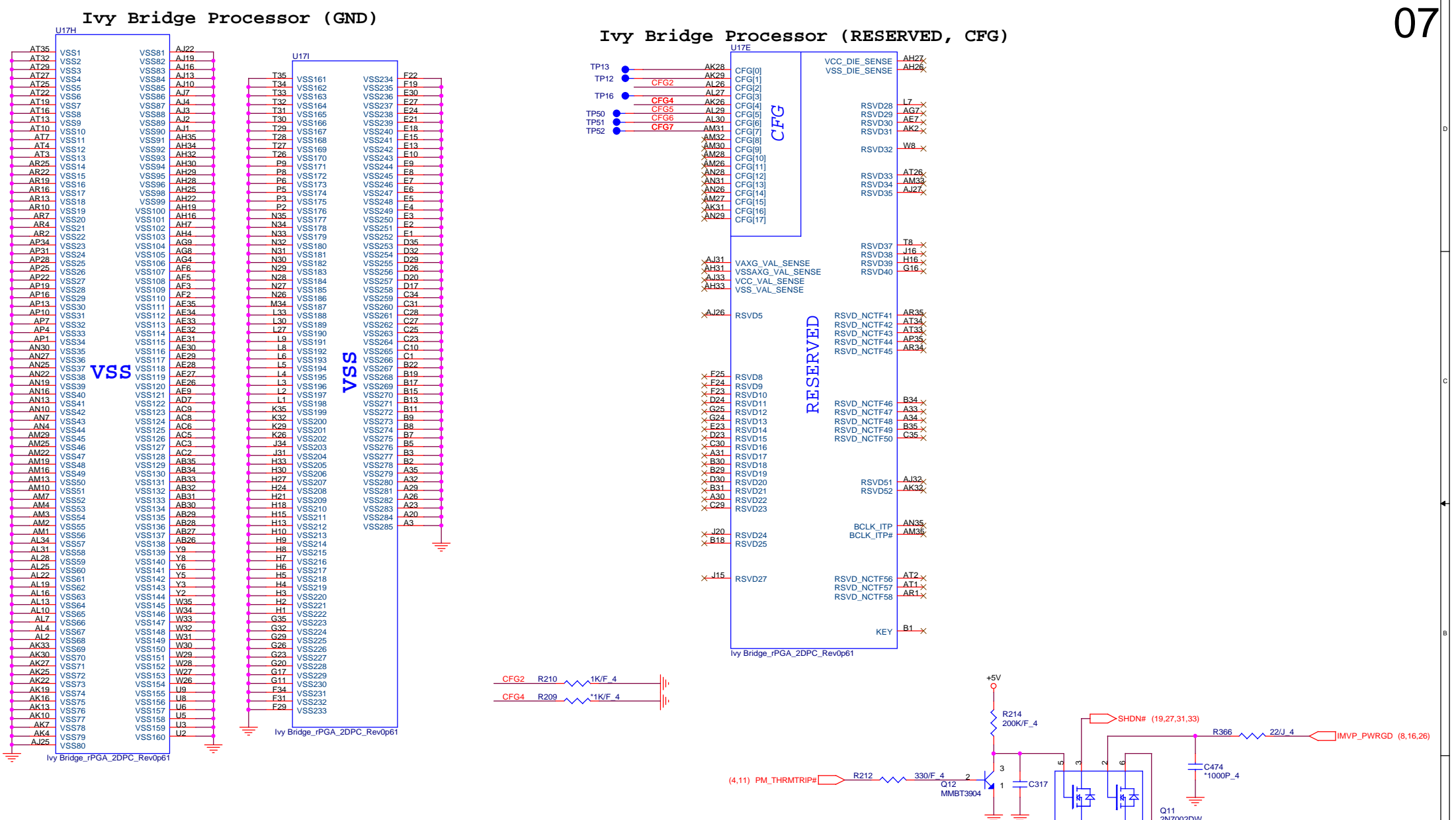
1.Level 1 Environment-related Substances Should Never be Used.

2.Recycled Resin and Coated Wire should be procured from Green Partners.



POWER






Processor Strapping			The CFG signals have a default value of '1' if not terminated on the board.		
			1	0	
CFG2 (PEG Static Lane Reversal)	Normal Operation		Lane Reversed		
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP		Enable; An ext DP device is connected to eDP		
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion		PEG wait for BIOS training		

CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - X16 PEG interface
10: PEG x8 x8 bifurcation enabled/disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



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Size

Document Number

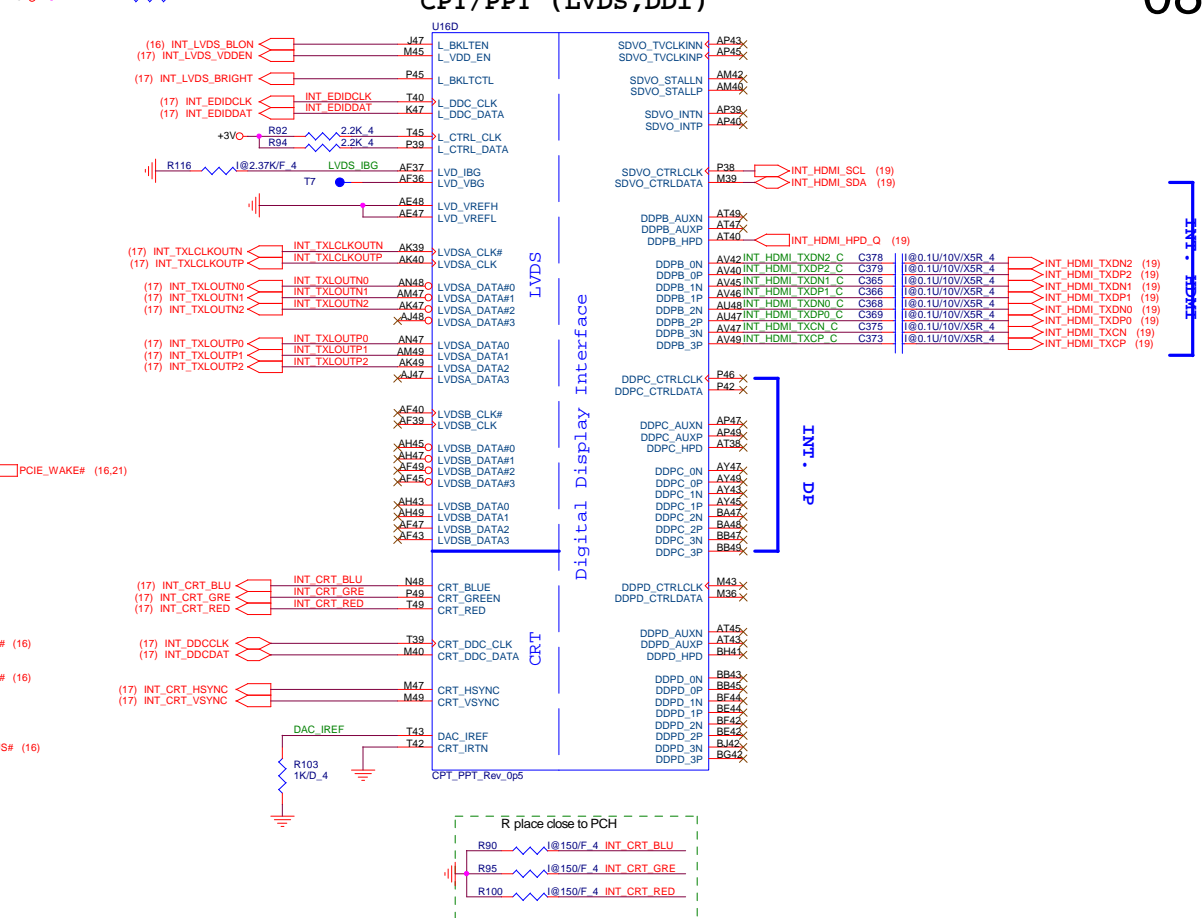
SNB/IVB 4/4

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CPT/PPT (LVDS,DDI)



(7,16,26) IMVP_PWRGD

(16) PCH_PWROK_EC

U25 TC7SH08FU

+3V_SS

C475

0.1U/10V/X5R 4

R367

22k 4

1

4

SYS_PWROK

FDI_INT R132 E@1K 4

FDI_FSYNC0 R139 E@1K 4

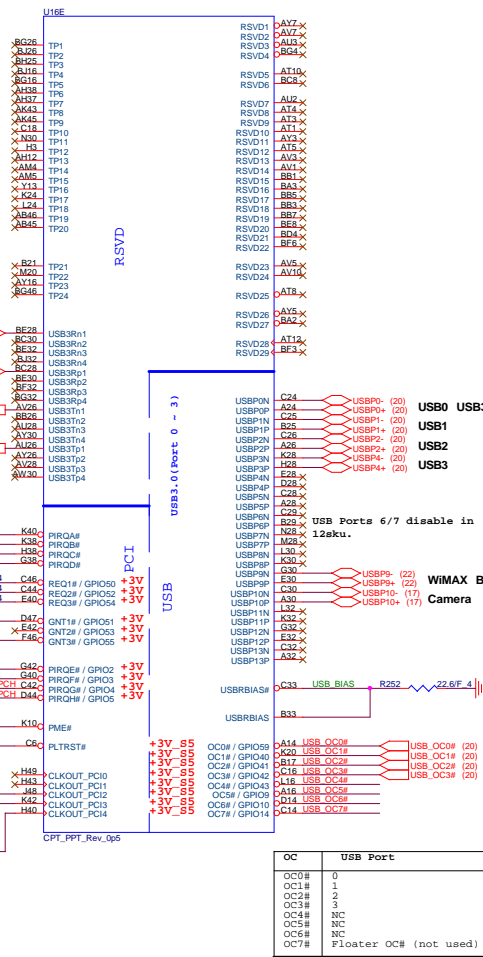
FDI_FSYNC1 R144 E@1K 4

FDI_LSYNC0 R131 E@1K 4

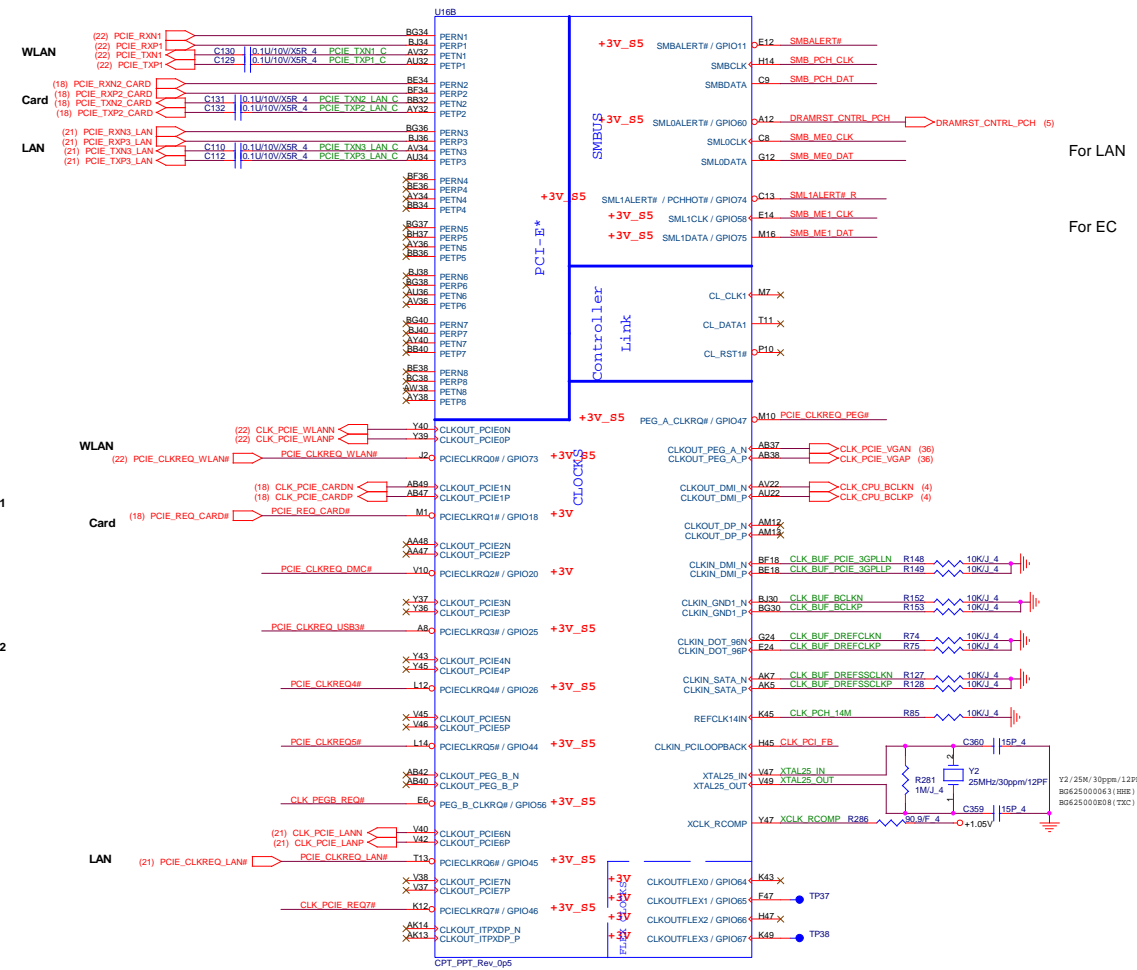
FDI_LSYNC1 R138 E@1K 4

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

CPT/PPT (PCI,USB,NVRAM)



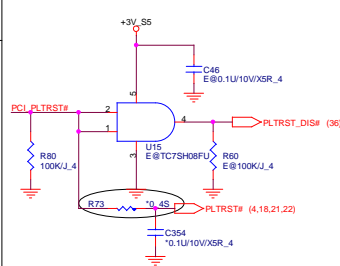
CPT/PPT (PCI-E, SMBUS, CLK)



For LAN

For EC

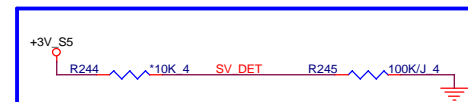
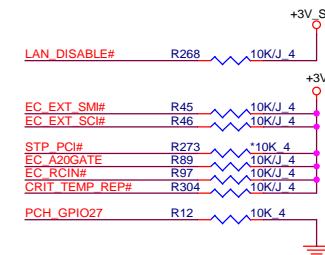
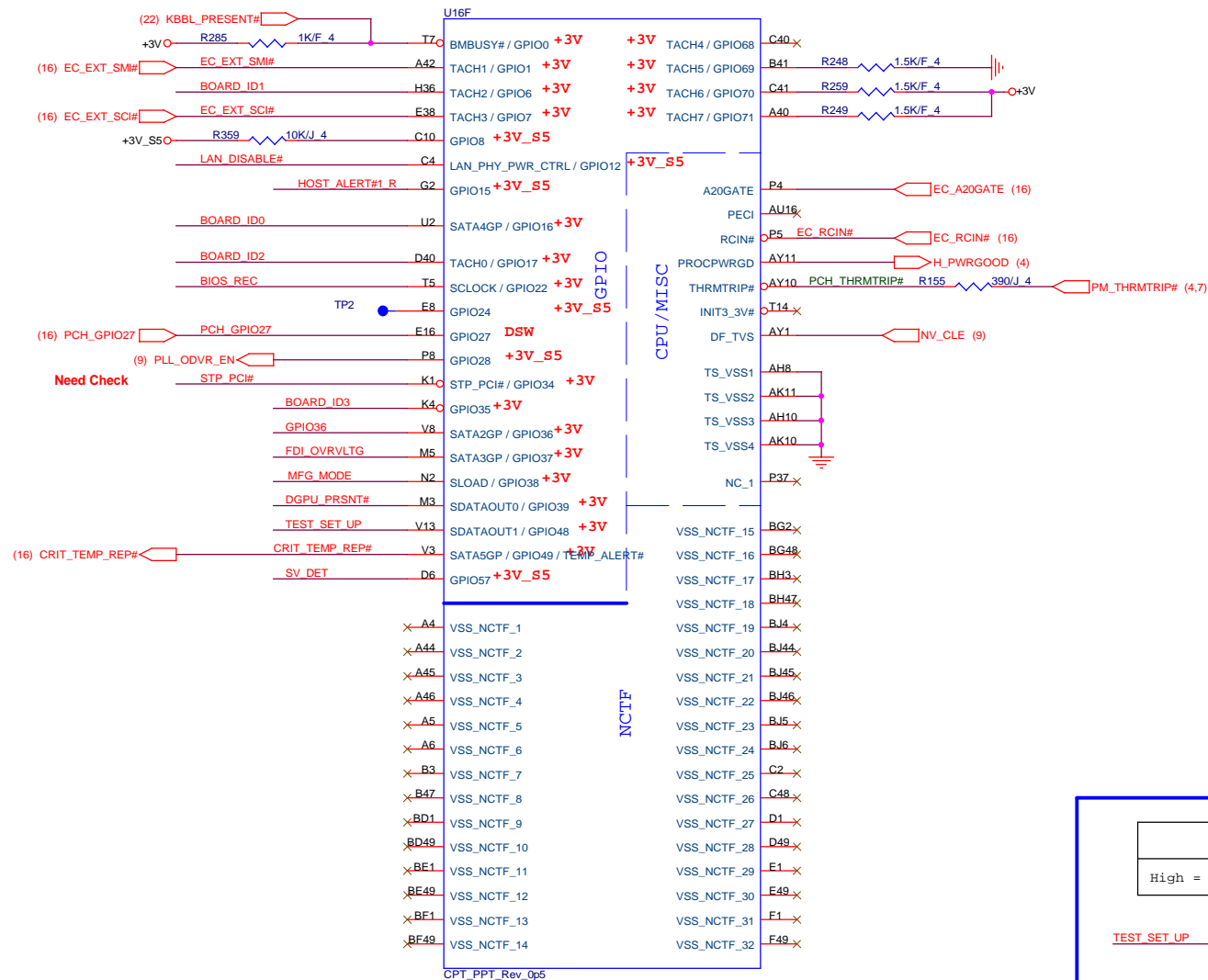
PLTRST#(CLG)



CPT/PPT (GPIO,VSS_NCTF,RSVD)

GPIO Pull-up/Pull-down(CLG)

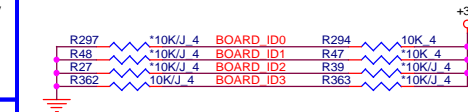
11



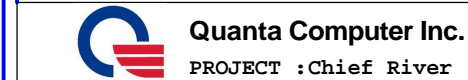
	R363(High) R362(Low)	R294(High) R297(Low)
Board ID3	0	0
Board ID0	0	0
14"/HK6/HK76	1	0
14"/HK6/HK70	1	0
15"/HK5/HM76	0	1
15"/HK5/HM70	1	1

Board ID1 (VRAM Vendor)	Samaung(1)	Hynix(0)
R47(High)	Stuff	No Stuff
R48(Low)	No Stuff	Stuff

Board ID2		
14" 4PCS	1G	512M
15" 8PCS	1G	2G
R39(High)	Stuff	No Stuff
R27(Low)	No Stuff	Stuff



PCBA SKU	Discrete	UMA
R277(Pull High)	Stuff	No Stuff
R275(Pull Low)	No Stuff	Stuff



Size	Document Number	Rev
	CPT/PPT 4/6	1A

1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.

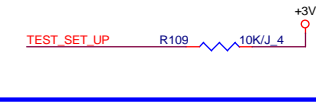
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FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage
--	--

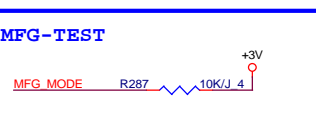
DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)
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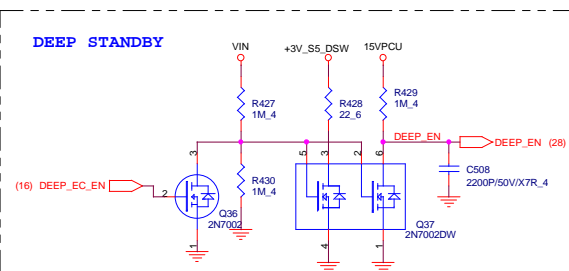
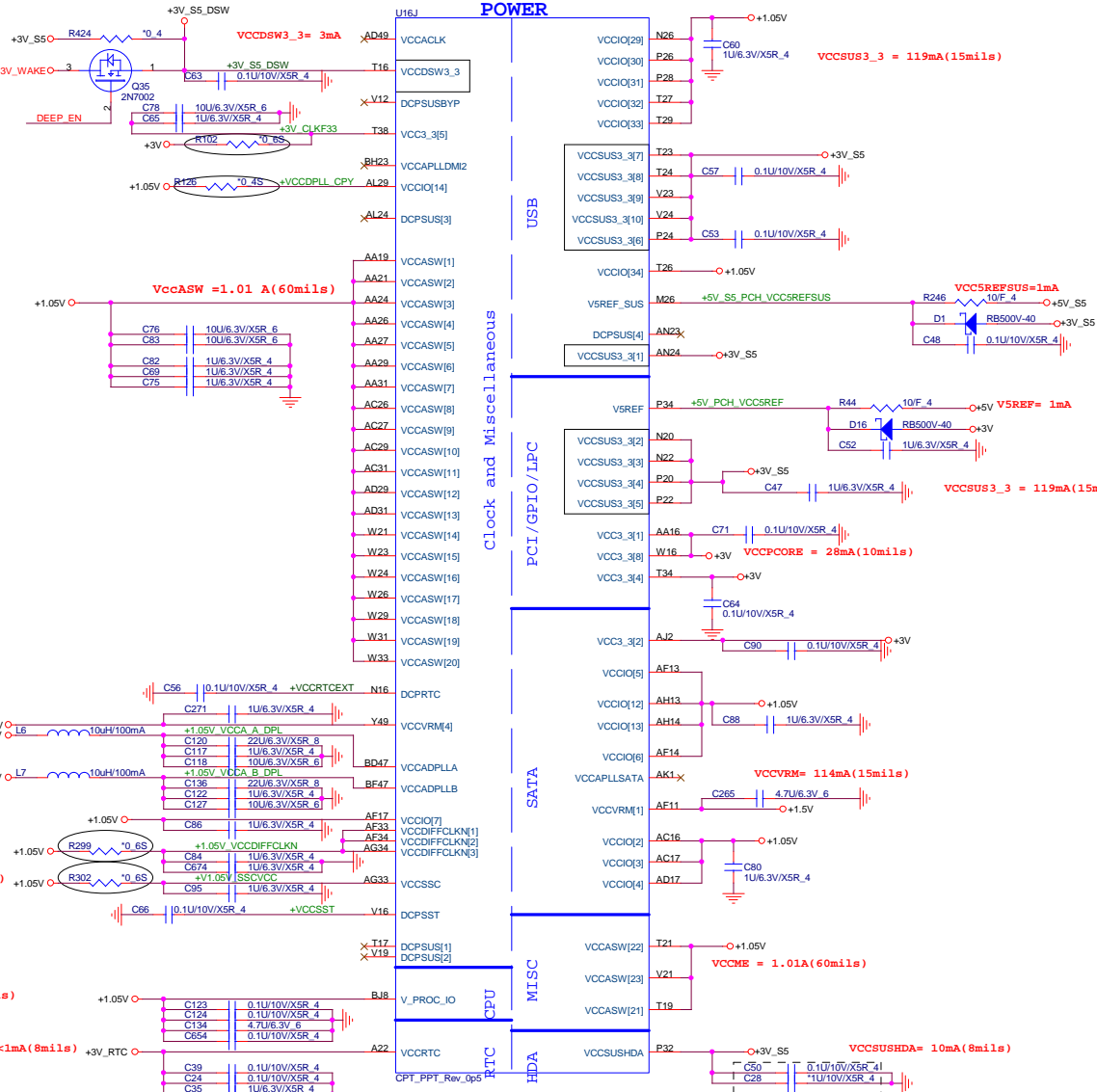
BIOS RECOVERY	High = Disable (Default) Low = Enable
---------------	--

SV_SET_UP
High = Strong (Default)



HOST_ALERT#1_R
Intel ME Crypto Transport Layer Security (TLS) cipher suite Low = Disable (Default) High = Enable





2. Recycled Resin and Coated Wire should be procured from Green Partner

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CPT/PPT (GND)

U16H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80]
AA2	VSS[2]	AK38
AA3	VSS[3]	AK4
AA33	VSS[4]	AK42
AA34	VSS[5]	AK46
AB11	VSS[6]	AK8
AB14	VSS[7]	AL16
AB38	VSS[8]	AL17
AB4	VSS[9]	AL19
AB43	VSS[10]	AL2
AB5	VSS[11]	VSS[88]
AB7	VSS[12]	VSS[89]
AC19	VSS[13]	VSS[90]
AC2	VSS[14]	VSS[91]
AC21	VSS[15]	VSS[92]
AC24	VSS[16]	VSS[93]
AC33	VSS[17]	VSS[94]
AC34	VSS[18]	VSS[95]
AC48	VSS[19]	VSS[96]
AD10	VSS[20]	VSS[97]
AD11	VSS[21]	VSS[98]
AD12	VSS[22]	VSS[99]
AD13	VSS[23]	VSS[100]
AD19	VSS[24]	VSS[101]
AD24	VSS[25]	VSS[102]
AD26	VSS[26]	VSS[103]
AD27	VSS[27]	VSS[104]
AD33	VSS[28]	VSS[105]
AD34	VSS[29]	VSS[106]
AD36	VSS[30]	VSS[107]
AD37	VSS[31]	VSS[108]
AD38	VSS[32]	VSS[109]
AD39	VSS[33]	VSS[110]
AD4	VSS[34]	VSS[111]
AD40	VSS[35]	VSS[112]
AD42	VSS[36]	VSS[113]
AD43	VSS[37]	VSS[114]
AD45	VSS[38]	VSS[115]
AD46	VSS[39]	VSS[116]
AD8	VSS[40]	VSS[117]
AE2	VSS[41]	VSS[118]
AE3	VSS[42]	VSS[119]
AF10	VSS[43]	VSS[120]
AF12	VSS[44]	VSS[121]
AD14	VSS[45]	VSS[122]
AD16	VSS[46]	VSS[123]
AF16	VSS[47]	VSS[124]
AF19	VSS[48]	VSS[125]
AF24	VSS[49]	VSS[126]
AF26	VSS[50]	VSS[127]
AF27	VSS[51]	VSS[128]
AF29	VSS[52]	VSS[129]
AF31	VSS[53]	VSS[130]
AF38	VSS[54]	VSS[131]
AF4	VSS[55]	VSS[132]
AF42	VSS[56]	VSS[133]
AF46	VSS[57]	VSS[134]
AF5	VSS[58]	VSS[135]
AF7	VSS[59]	VSS[136]
AF8	VSS[60]	VSS[137]
AG19	VSS[61]	VSS[138]
AG2	VSS[62]	VSS[139]
AG31	VSS[63]	VSS[140]
AG48	VSS[64]	VSS[141]
AH11	VSS[65]	VSS[142]
AH3	VSS[66]	VSS[143]
AH36	VSS[67]	VSS[144]
AH39	VSS[68]	VSS[145]
AH40	VSS[69]	VSS[146]
AH42	VSS[70]	VSS[147]
AH46	VSS[71]	VSS[148]
AH7	VSS[72]	VSS[149]
AJ19	VSS[73]	VSS[150]
AJ21	VSS[74]	VSS[151]
AJ24	VSS[75]	VSS[152]
AJ33	VSS[76]	VSS[153]
AJ34	VSS[77]	VSS[154]
AK12	VSS[78]	VSS[155]
AK3	VSS[79]	VSS[156]
		VSS[157]
		VSS[158]


CPT_PPT_Rev_0p5

U16I		
AY4	VSS[159]	
AY42	VSS[160]	
AY46	VSS[161]	
AY8	VSS[162]	
B11	VSS[163]	
B15	VSS[164]	
B19	VSS[165]	
B23	VSS[166]	
B27	VSS[167]	
B31	VSS[168]	
B35	VSS[169]	
B39	VSS[170]	
B7	VSS[171]	
F45	VSS[172]	
BB12	VSS[173]	
BB16	VSS[174]	
BB20	VSS[175]	
BB22	VSS[176]	
BB24	VSS[177]	
BB28	VSS[178]	
BB30	VSS[179]	
BB38	VSS[180]	
BB4	VSS[181]	
BB46	VSS[182]	
BC14	VSS[183]	
BC18	VSS[184]	
BC2	VSS[185]	
BC22	VSS[186]	
BC26	VSS[187]	
BC32	VSS[188]	
BC34	VSS[189]	
BC36	VSS[190]	
BC40	VSS[191]	
BC42	VSS[192]	
BC48	VSS[193]	
BD46	VSS[194]	
BD5	VSS[195]	
BE22	VSS[196]	
BE26	VSS[197]	
BE40	VSS[198]	
BE10	VSS[199]	
BE12	VSS[200]	
BF16	VSS[201]	
BF20	VSS[202]	
BF22	VSS[203]	
BF24	VSS[204]	
BF26	VSS[205]	
BF28	VSS[206]	
BD3	VSS[207]	
BF30	VSS[208]	
BF38	VSS[209]	
BF40	VSS[210]	
BF8	VSS[211]	
BG17	VSS[212]	
BG21	VSS[213]	
BG33	VSS[214]	
BG44	VSS[215]	
BG8	VSS[216]	
BH11	VSS[217]	
AU30	VSS[218]	
BH17	VSS[219]	
BH19	VSS[220]	
H10	VSS[221]	
BH27	VSS[222]	
BH31	VSS[223]	
BH33	VSS[224]	
BH35	VSS[225]	
BH39	VSS[226]	
BH43	VSS[227]	
BH7	VSS[228]	
D3	VSS[229]	
AW22	VSS[230]	
D16	VSS[231]	
D18	VSS[232]	
D22	VSS[233]	
D24	VSS[234]	
D26	VSS[235]	
D30	VSS[236]	
D32	VSS[237]	
D34	VSS[238]	
D38	VSS[239]	
D42	VSS[240]	
D8	VSS[241]	
E18	VSS[242]	
E26	VSS[243]	
G18	VSS[244]	
G20	VSS[245]	
G26	VSS[246]	
G28	VSS[247]	
G36	VSS[248]	
G48	VSS[249]	
H12	VSS[250]	
H18	VSS[251]	
H22	VSS[252]	
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

CPT_PPT_Rev_0p5

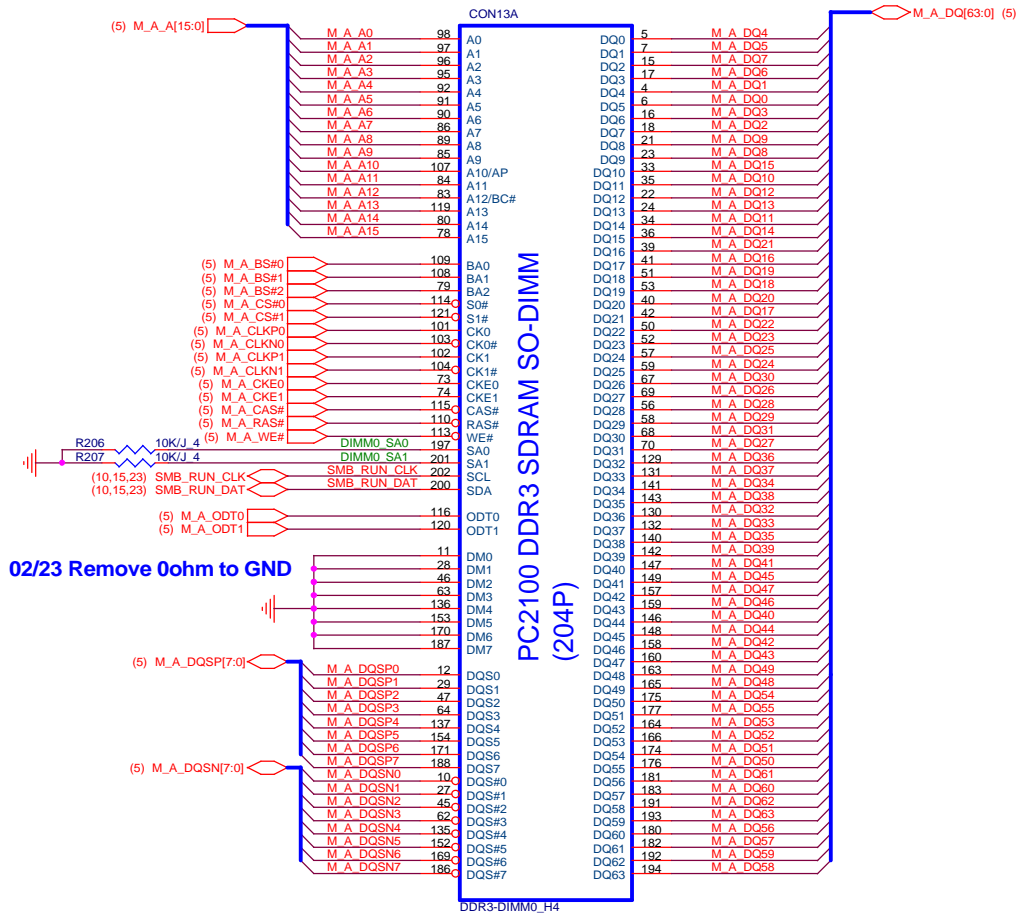
VSS[259]	H46
VSS[260]	K18
VSS[261]	K26
VSS[262]	K38
VSS[263]	K46
VSS[264]	K7
VSS[265]	L18
VSS[266]	L2
VSS[267]	L20
VSS[268]	L26
VSS[269]	L28
VSS[270]	L36
VSS[271]	L48
VSS[272]	M12
VSS[273]	P16
VSS[274]	M18
VSS[275]	M22
VSS[276]	M24
VSS[277]	M30
VSS[278]	M32
VSS[279]	M34
VSS[280]	M38
VSS[281]	M4
VSS[282]	M42
VSS[283]	M46
VSS[284]	M8
VSS[285]	N18
VSS[286]	P30
VSS[287]	N47
VSS[288]	P11
VSS[289]	P18
VSS[290]	T33
VSS[291]	P40
VSS[292]	P43
VSS[293]	P47
VSS[294]	R2
VSS[295]	R48
VSS[296]	T12
VSS[297]	T31
VSS[298]	T37
VSS[299]	T4
VSS[300]	V34
VSS[301]	T46
VSS[302]	T47
VSS[303]	T8
VSS[304]	V11
VSS[305]	V17
VSS[306]	V26
VSS[307]	V27
VSS[308]	V29
VSS[309]	V31
VSS[310]	V36
VSS[311]	V39
VSS[312]	V43
VSS[313]	V7
VSS[314]	W17
VSS[315]	W19
VSS[316]	W2
VSS[317]	W27
VSS[318]	W48
VSS[319]	Y12
VSS[320]	Y38
VSS[321]	Y4
VSS[322]	Y42
VSS[323]	Y46
VSS[324]	Y8
VSS[325]	BG29
VSS[326]	N24
VSS[327]	AJ3
VSS[328]	AD47
VSS[329]	B43
VSS[330]	BE10
VSS[331]	BG41
VSS[332]	G14
VSS[333]	H16
VSS[334]	T36
VSS[335]	BG22
VSS[336]	BG24
VSS[337]	C22
VSS[338]	AP13
VSS[339]	M14
VSS[340]	AP3
VSS[341]	AP1
VSS[342]	BE16
VSS[343]	BC16
VSS[344]	BG28
VSS[345]	BJ28
VSS[346]	
VSS[347]	
VSS[348]	
VSS[349]	
VSS[350]	
VSS[351]	
VSS[352]	

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

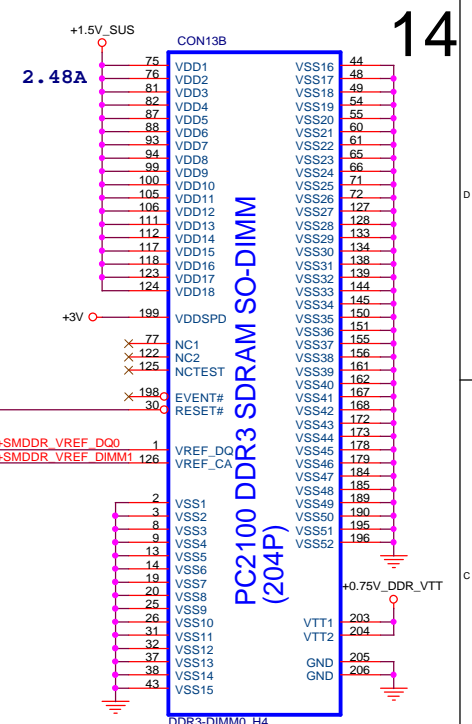
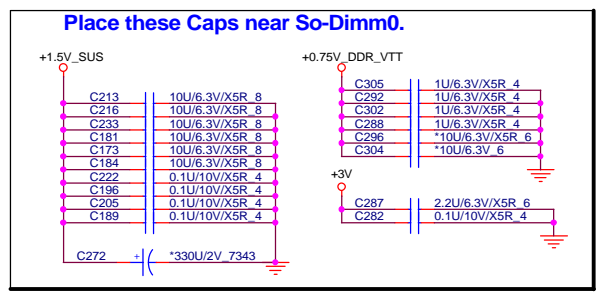


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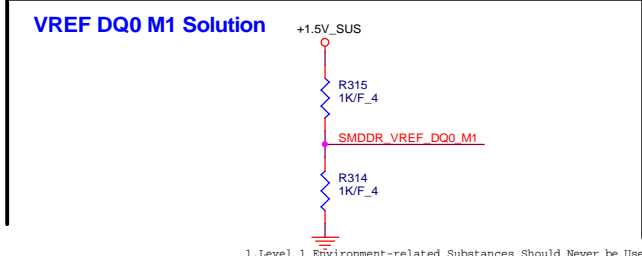
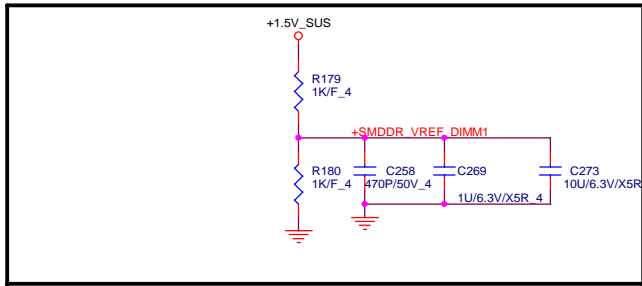
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	CPT/PPT 6/6	1A
Date:	Wednesday, February 01, 2012	Sheet 13 of 43




RUV Type



RUV Type



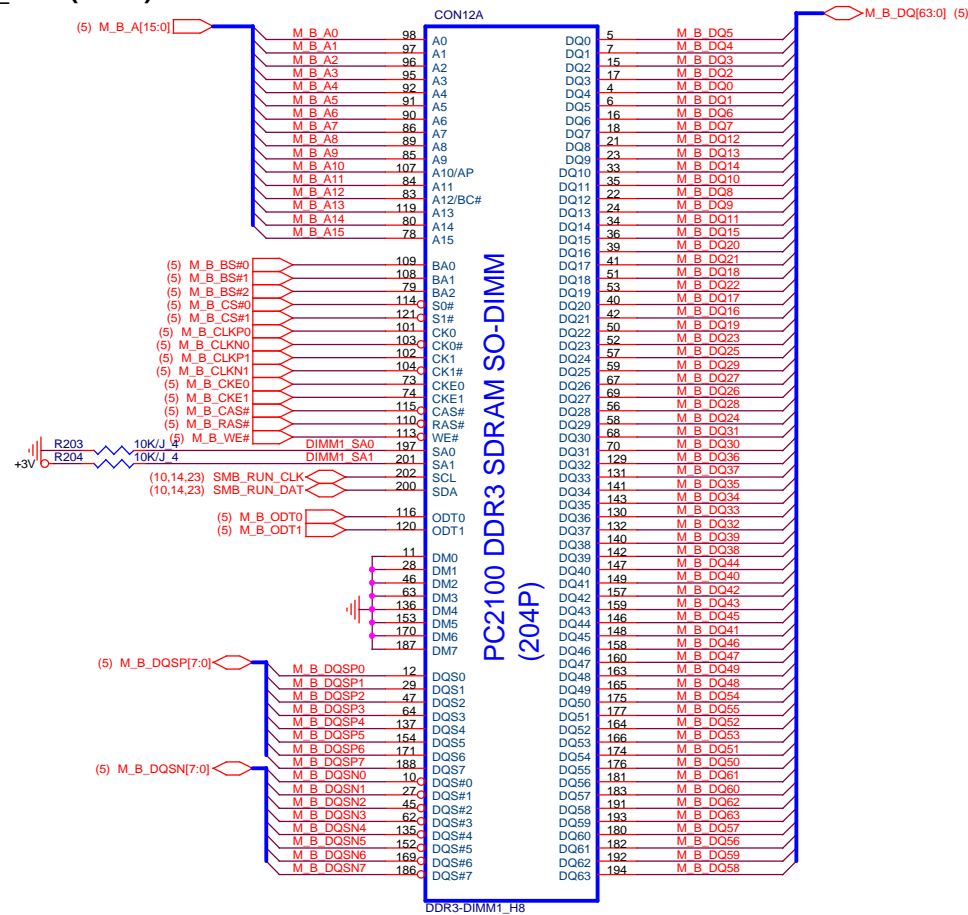


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Size	Document Number	Date	Rev
	DDRIII SO-DIMM-0	Wednesday, February 01, 2012	1A
		Sheet 14 of 43	

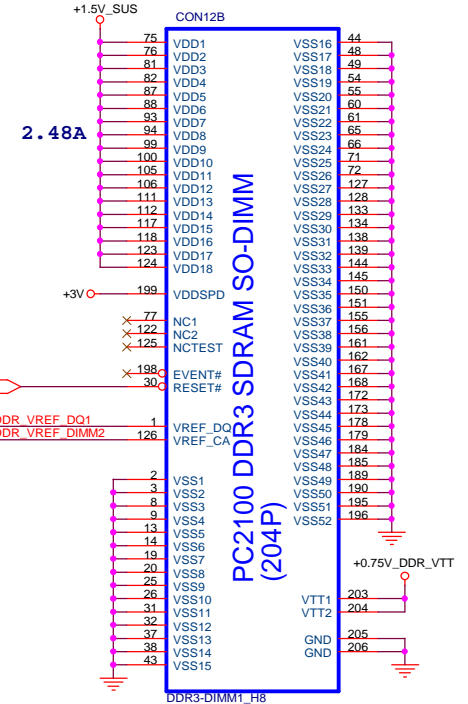
1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.

DDR_RVS (DDR)



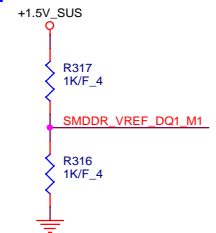
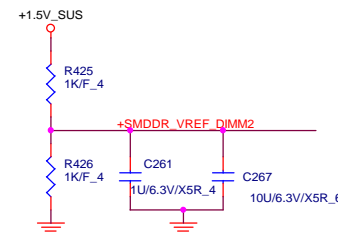
PC2100 DDR3 SDRAM SO-DIMM (204P)

RUV Type

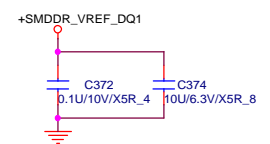
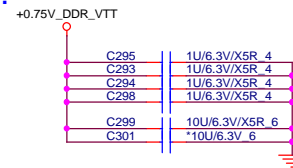
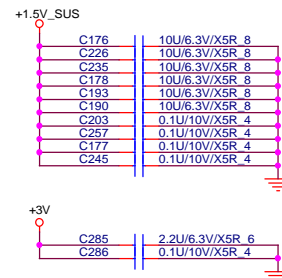


RUV Type

VREF DQ1 M1 Solution



Place these Caps near So-Dimm1.



Quanta Computer Inc.

PROJECT :Chief River

Size	Document Number	Rev
	DDR3 SO-DIMM-1	1A

1.Level 1 Environment-related Substances Should Never be Used.

2.Recycled Resin and Coated Wire should be procured from Green Partners.

Date: Wednesday, February 01, 2012 Sheet 15 of 43

Note the input leakage current to the strap pins must be less than 10uA.

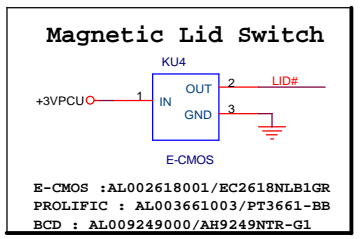
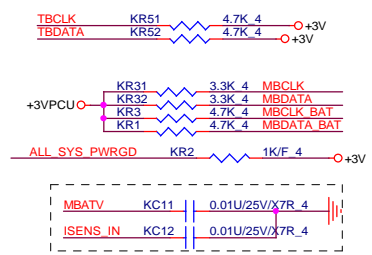
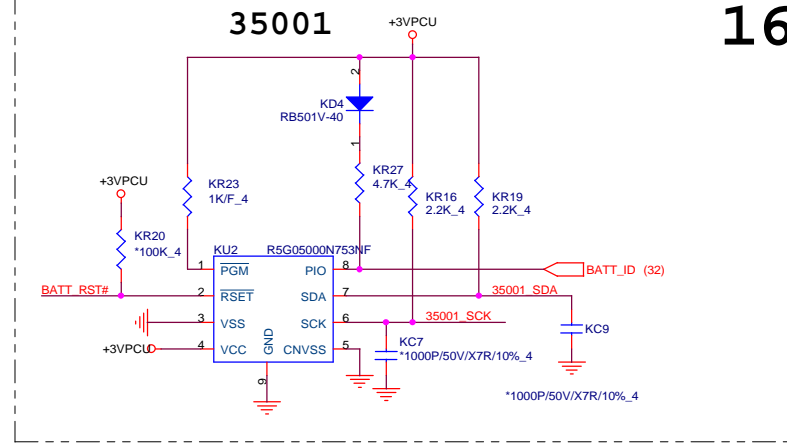
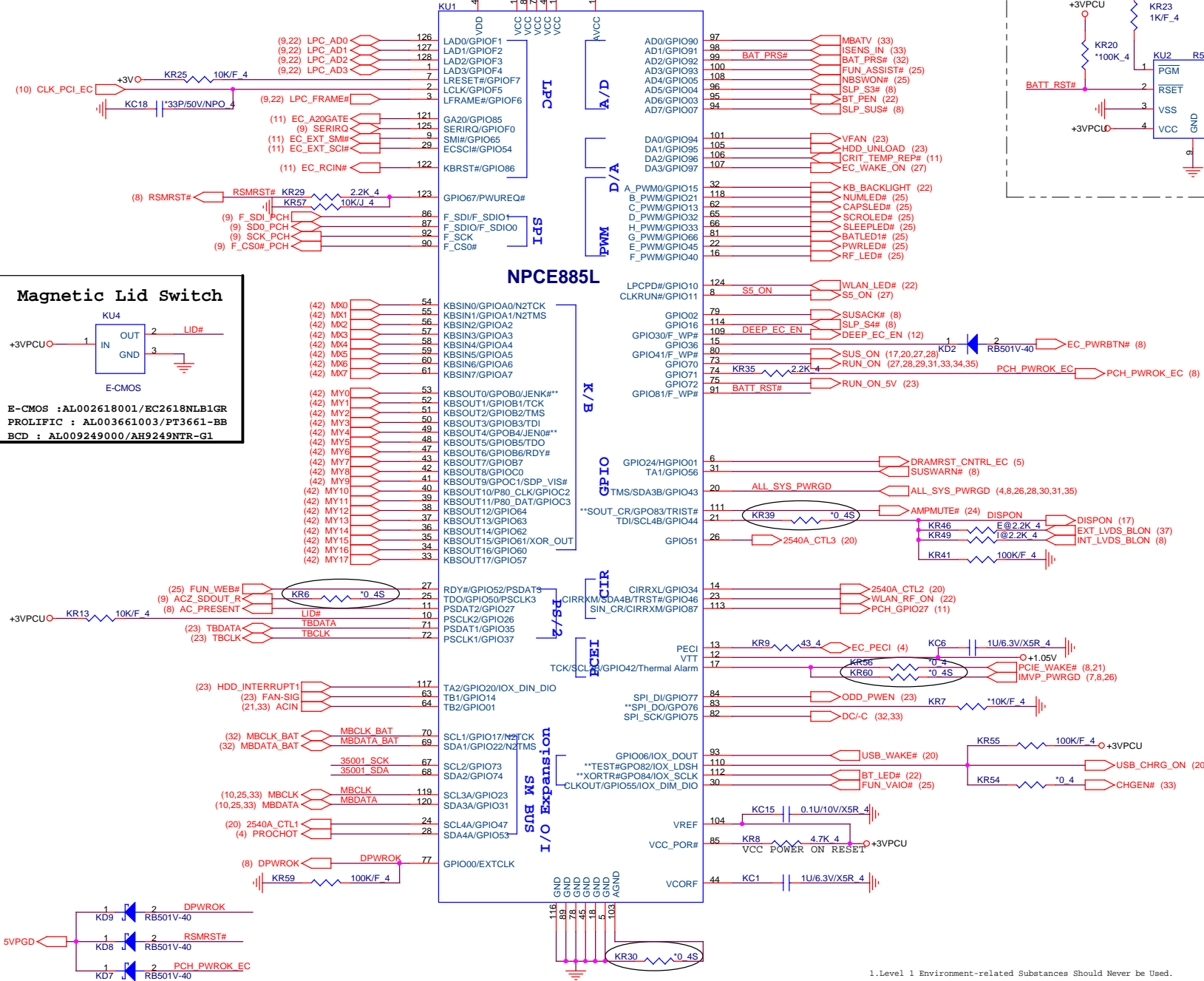
3VPCU

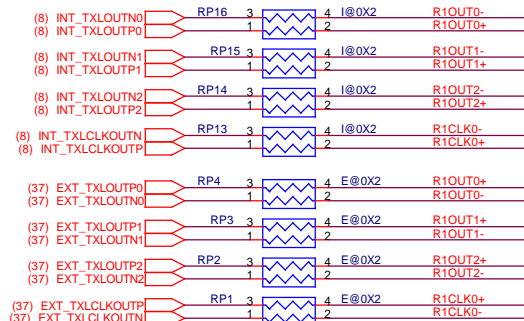
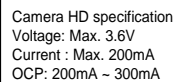
KC17	*10U/6.3V/X5R_8
KC5	0.1U/10V/X5R_4
KC2	0.1U/10V/X5R_4
KC14	0.1U/10V/X5R_4
KC8	0.1U/10V/X5R_4
KC3	0.1U/10V/X5R_4
KC10	0.1U/10V/X5R_4

KC16 *10U/6.3V/X5R_8

KC13 0.1U/10V/X5R_4

02

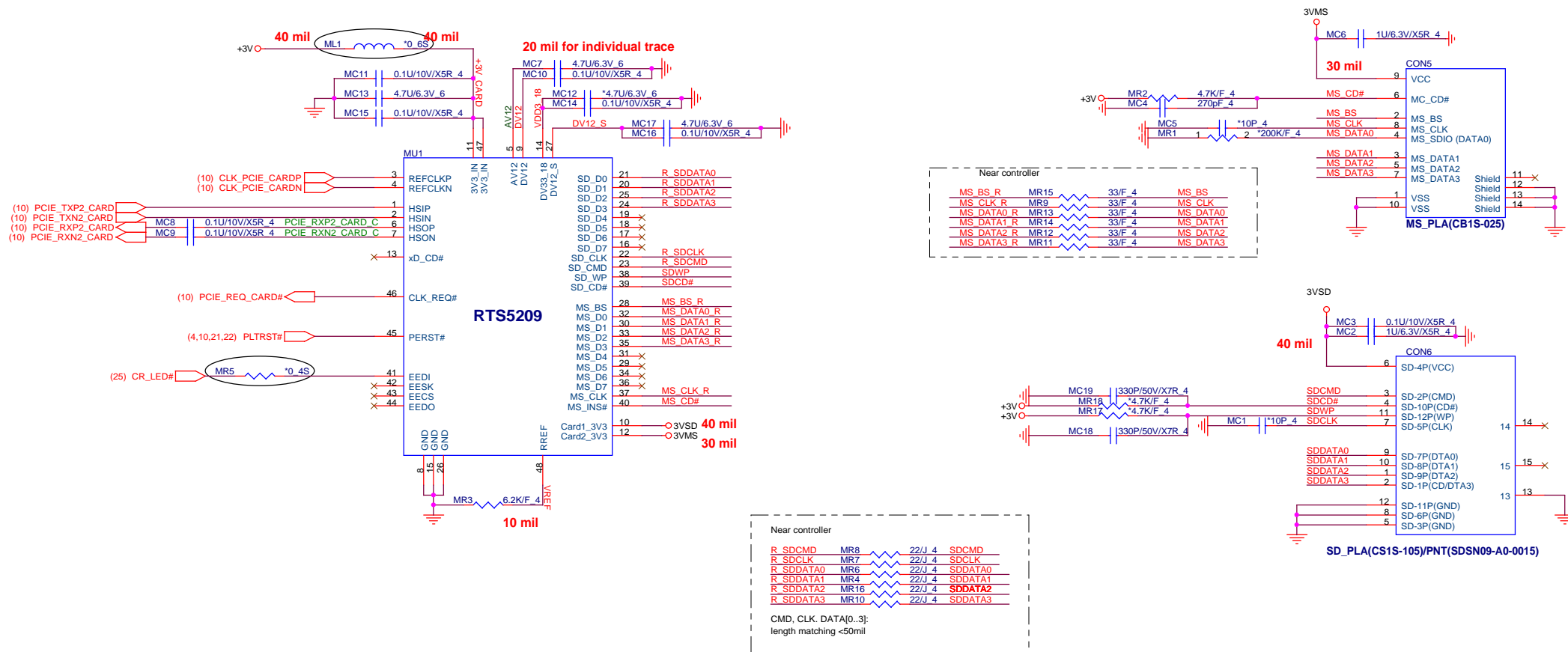




PROJECT :Chief River

CRT/LVDS

Rev	1A
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Quanta Computer Inc.

PROJECT : Chief River

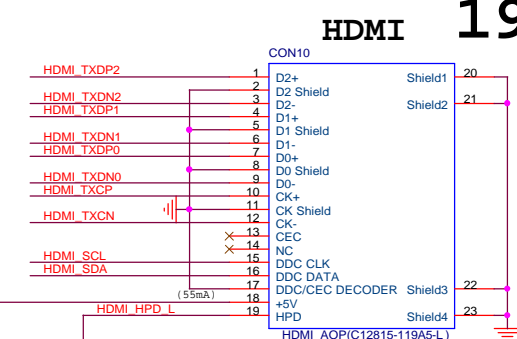
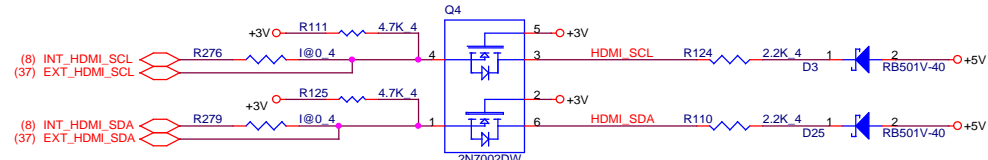
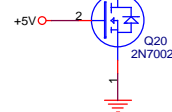
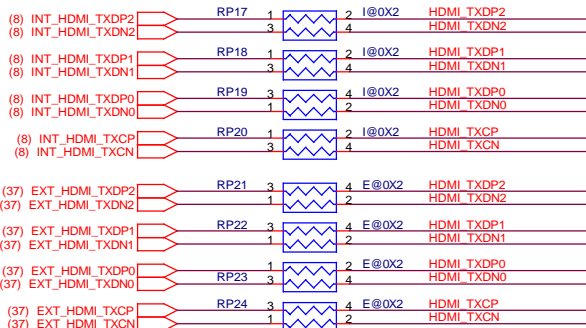
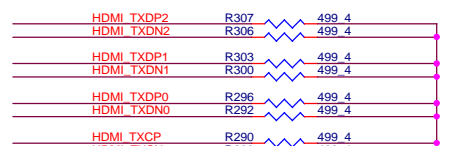
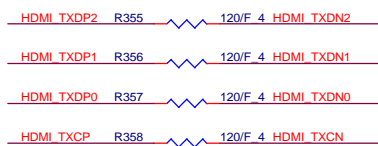
CARD

Size	Document Number	Rev
		1A

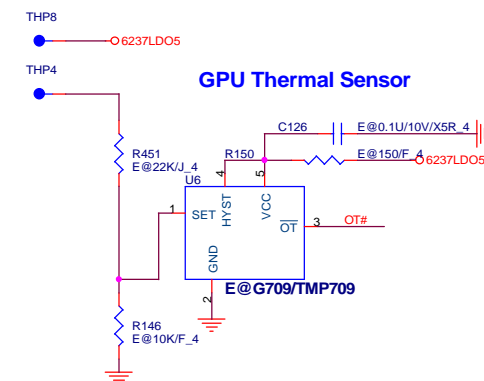
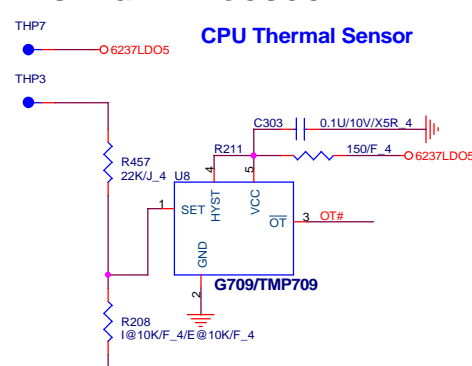
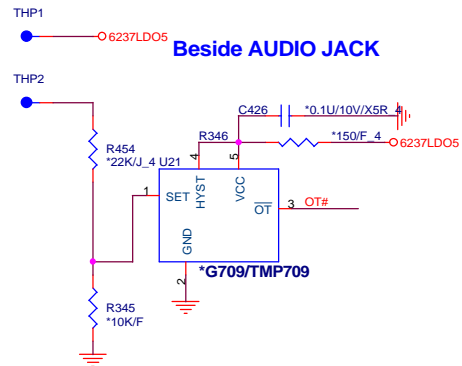
1. Level 1 Environment-related Substances Should Never be Used.

2. Recycled Resin and Coated Wire should be procured from Green Partners.

Date: Wednesday, February 01, 2012 Sheet 18 of 43



H/W Thermal Protect

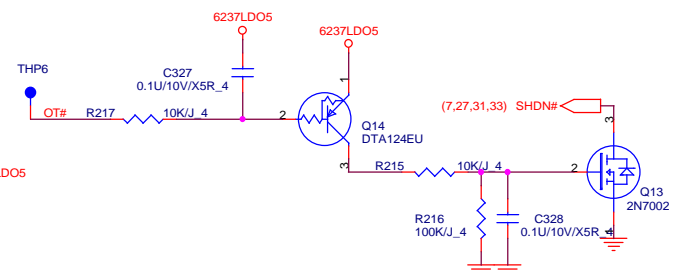
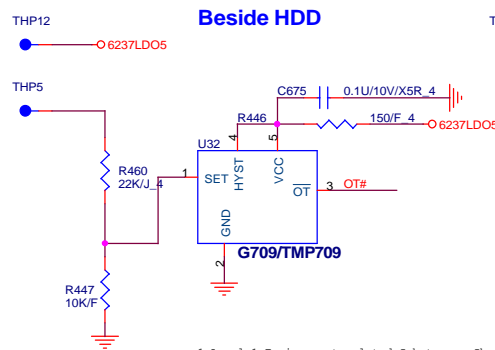


$$RSET(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$$

95	18.5K
100	15K
107	10.3K
110	8.2K

DIS SKU					
Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	73	R208=34.59K	34.8K	73.2	72.2
Near GFX sensor temp	73	R146=34.59K	34.8K	73.2	72.2
Near AUDIO sensor temp	55	R345=48.58K	48.7K	55.5	54.2

UMA SKU					
Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	82	R208=27.89K	27.4K	83.1	82.2
Near AUDIO sensor temp	55	R345=48.58K	48.7K	55.5	54.2

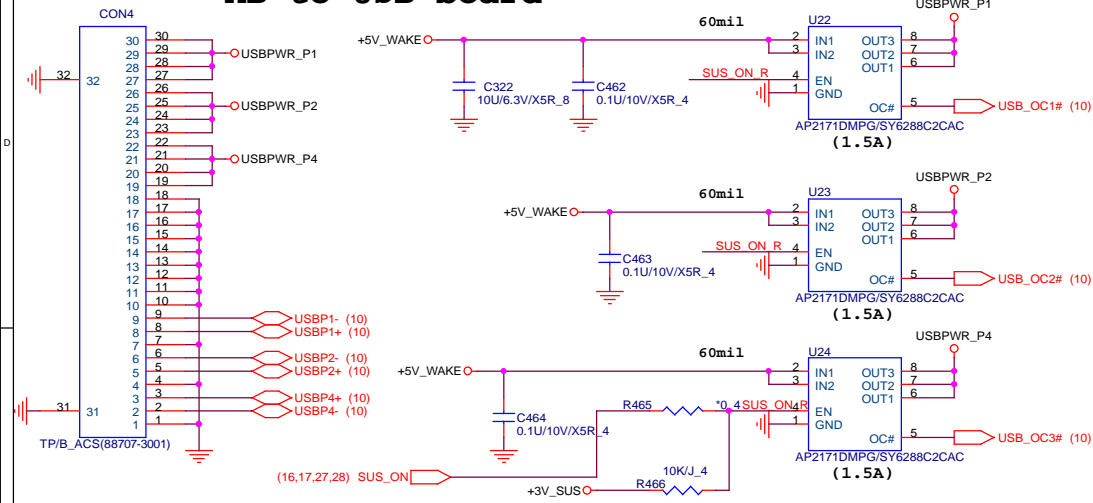


Quanta Computer Inc.
PROJECT :Chief River

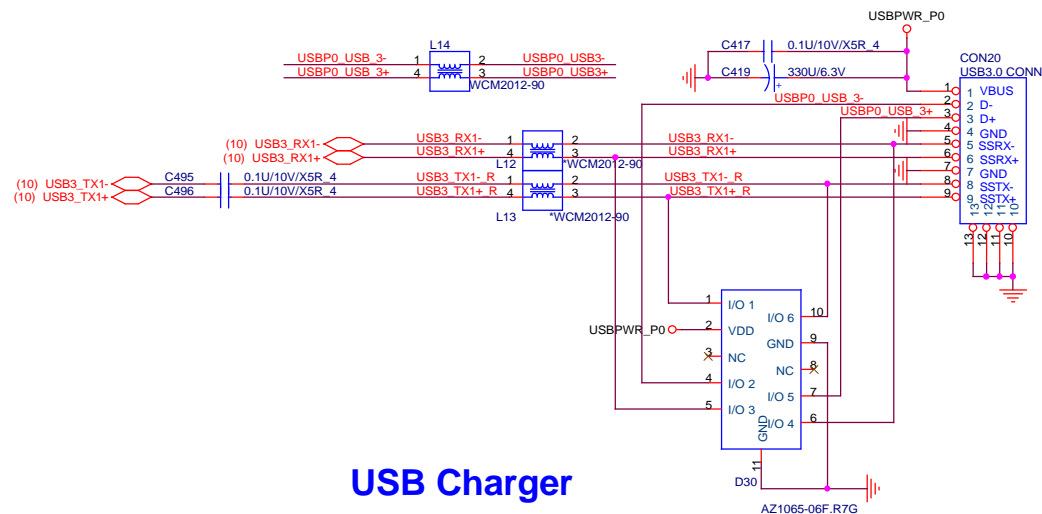
Size	Document Number	Date	Sheet	Rev
	HDMI/Thermal IC	Friday, February 03, 2012	19 of 43	1A

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners

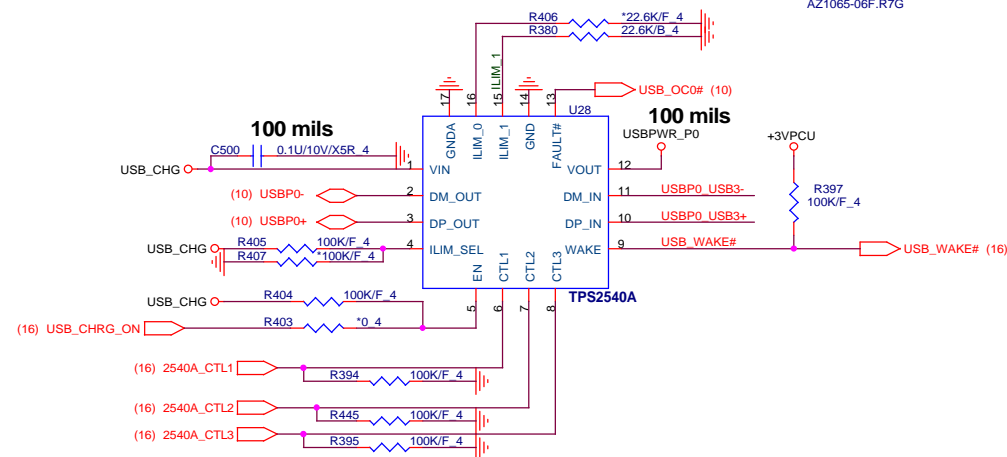
MB to USB board



USB 3.0 PORT0



USB Charger



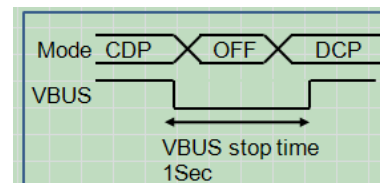
System State	USB Battery Charging Setting	
	Disable	Enable
S0	SDP	CDP
S3	SDP	DCP
Deep Standby	SDP (VBUS OFF)	DCP
S4	SDP (VBUS OFF)	DCP
S5	SDP (VBUS OFF)	DCP

SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS

CTL_1	CTL_2	CTL_3	TPS 2540A/2543 Truth Table
0	0	0	OUT discharge, power switch OFF
0	X	1	DCP, Auto-detect (S3/S4/S5, 1.5A)
X	1	0	SDP, USB2.0 mode (S0, 0.5A)
1	0	0	DCP, BC SPEC1.2 only (S3/Deep standby/S4/S5, 1.5A)
1	0	1	DCP, Divider mode only (S3/S4/S5, 1.5A)
1	1	1	CDP (S0, 1.5A)

TPS-2540A	TPS-2543	MODE	AC/DC Mode			
			C1	C2	C3	ILIM_SEL
S0	S0	SDP	X(1)	1	0	X
S0	S0	CDP	1	1	1	1
S3(Wake Enable)	X	SDP	1	1	0	1
S3(Charger Mode)	S3	DCP	1	X(0)	0	1
S4	S4	DCP	1	X(0)	0	1
S5	S5	DCP	1	X(0)	0	1
Discharge	Discharge	DIS	0	0	0	X

DCP: BC 1.2 only.

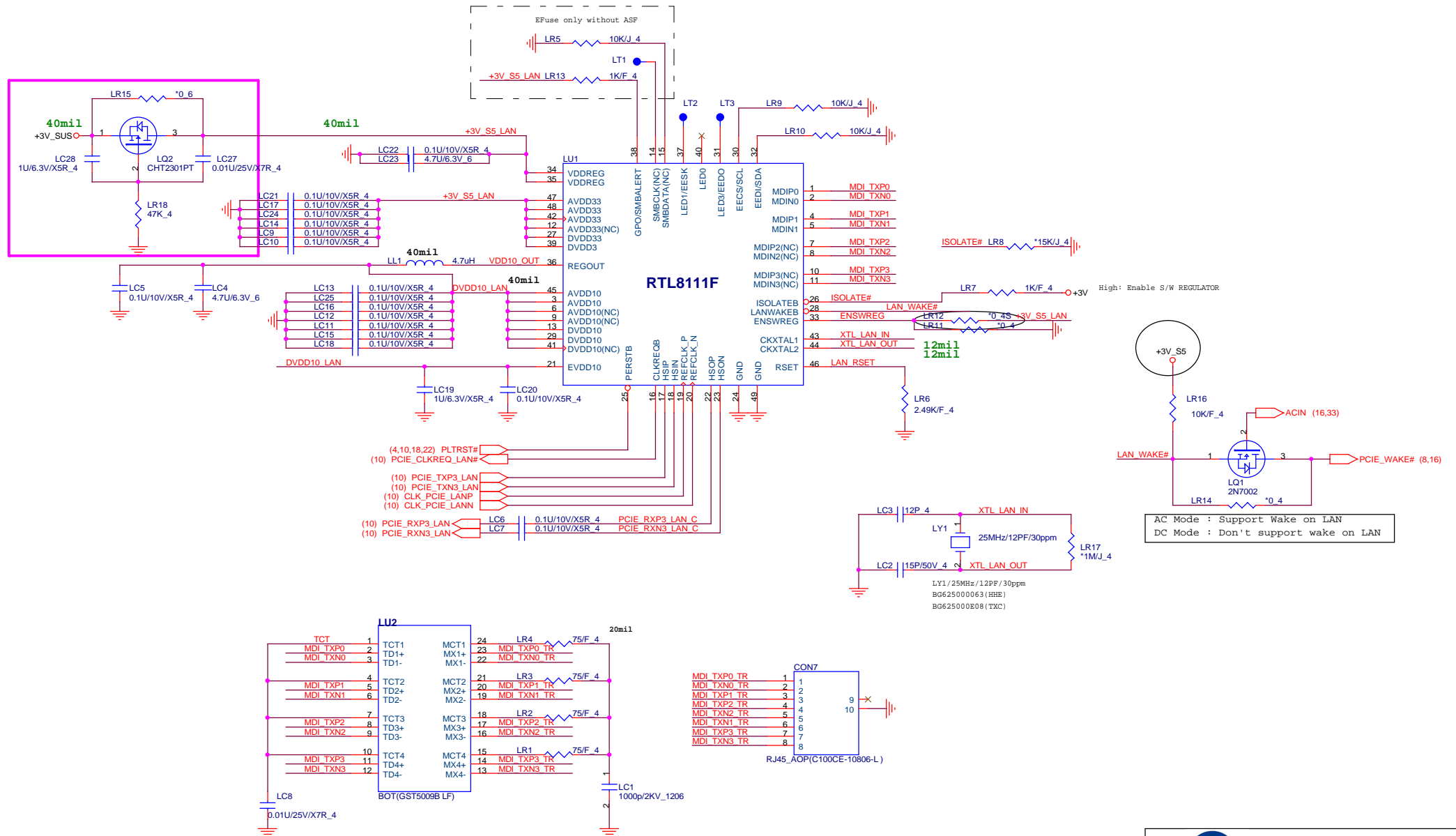


USB WAKE	
1	No device plug(LDO)
0	Device plug(Switch Power)

ILIM_SEL (I LIMIT(A)= 48000/R)	
HI	I_LIM_1
LO	I_LIM_0
48000/22.6K=2.123A	

Quanta Computer Inc.
PROJECT :Chief River
USB/USB Charger

Size Document Number
Date: Thursday, February 02, 2012 Sheet 20 of 43

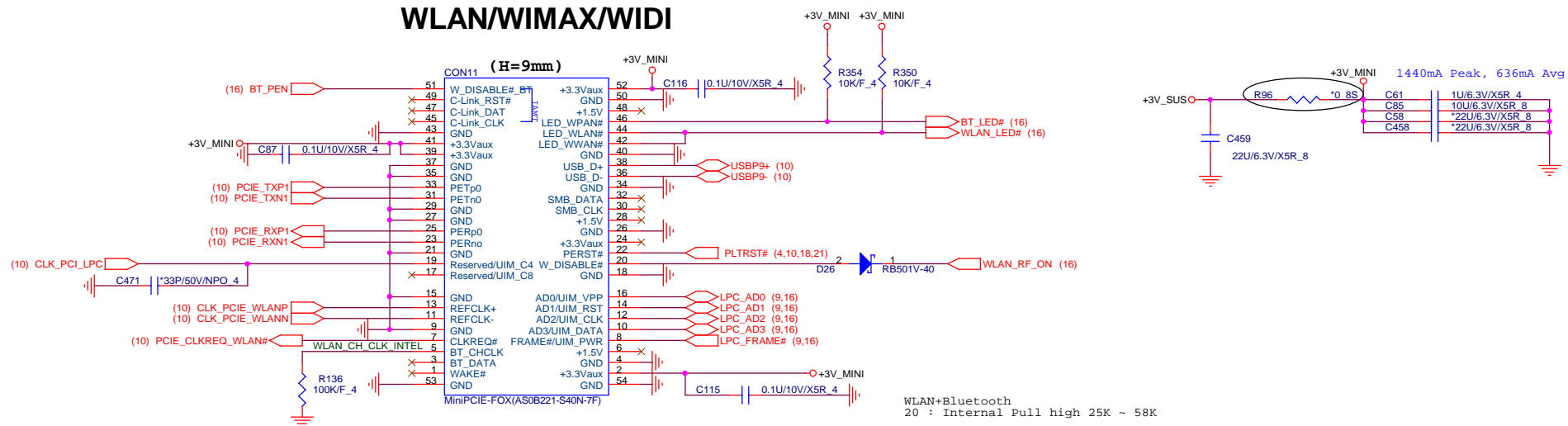


Quanta Computer Inc.
PROJECT : Chief River

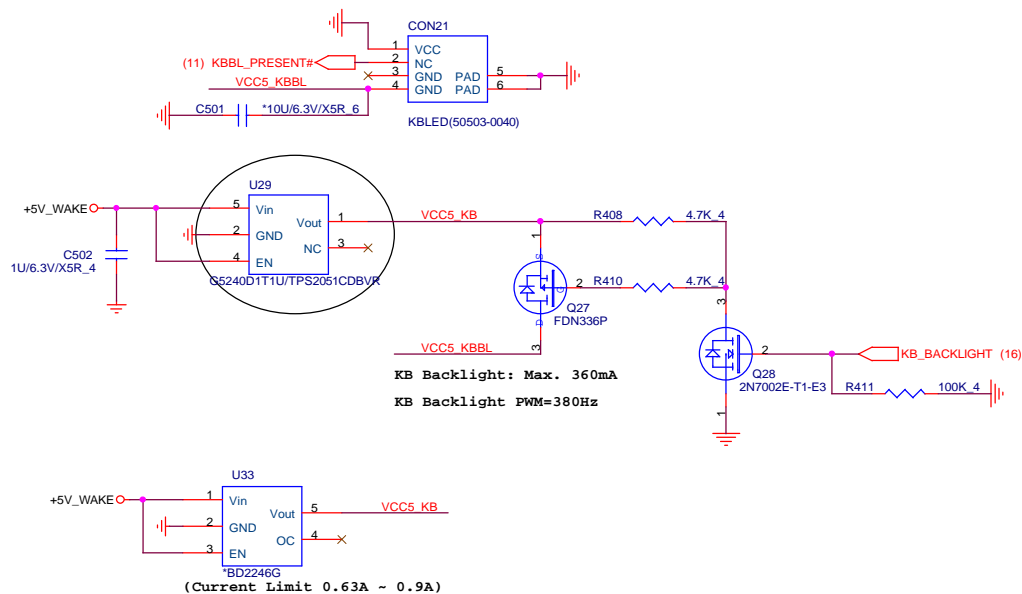
Size	Document Number	Date	Wednesday, February 01, 2012	Sheet	21 of 43	Rev	1A
LAN RTL8111E							

1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.

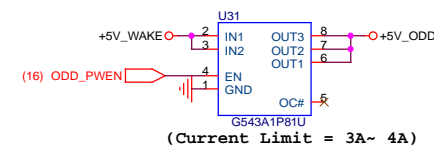
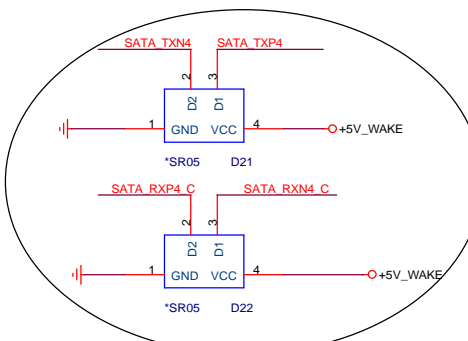
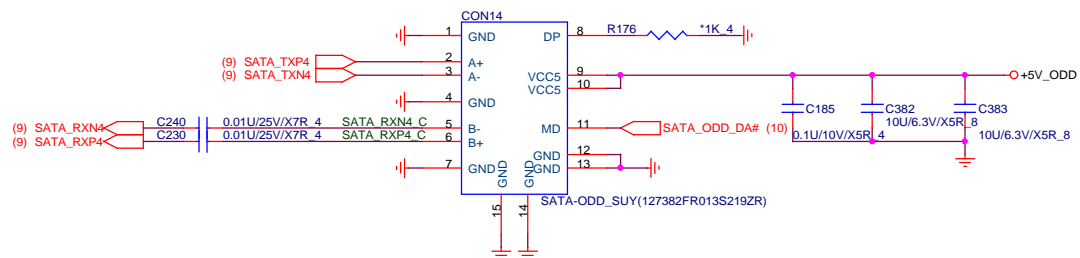
WLAN/WIMAX/WIDI



KB BACKLIGHT

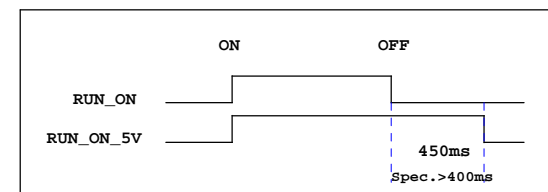
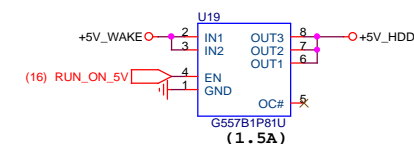
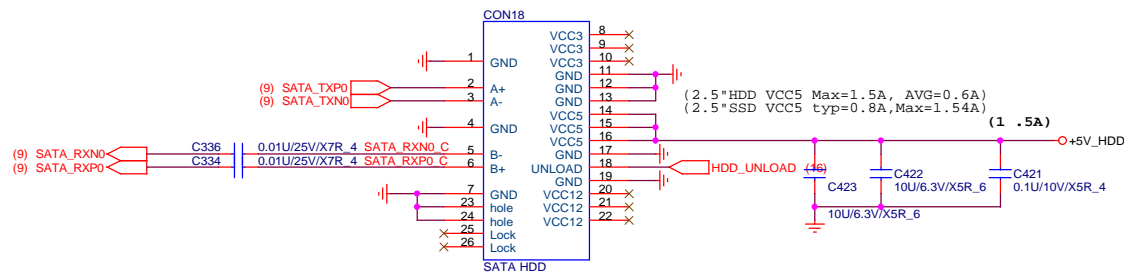


ODD CONNECTOR

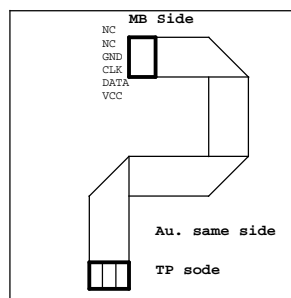


0130-- change ODD ESD diode form Rclamp0502n to SR05

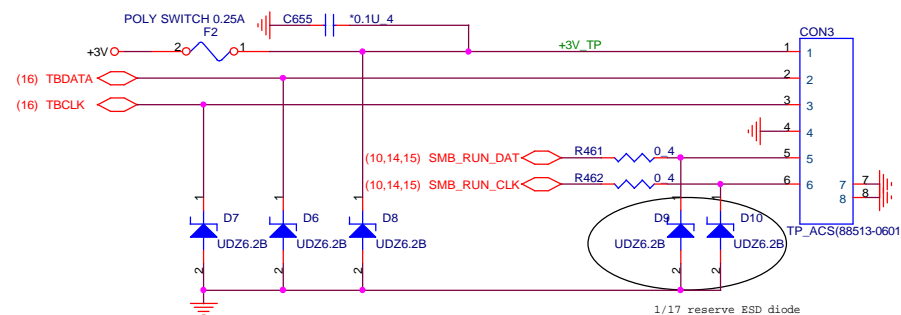
HDD CONNECTOR



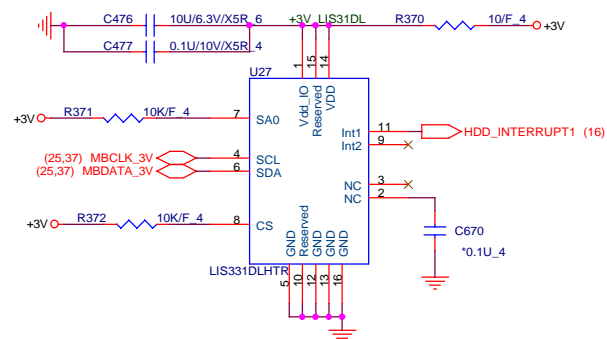
01/30 del D23 , D24 ESD diode



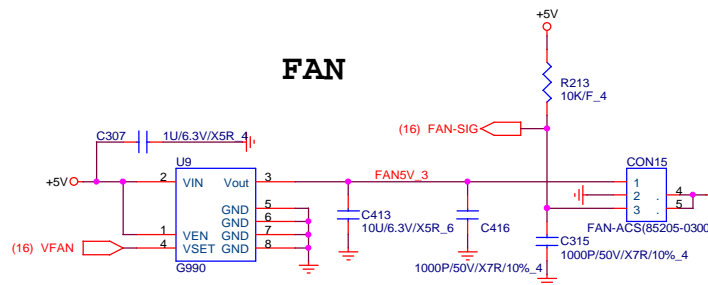
T/P Board to T/P

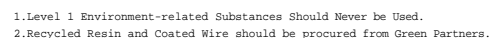


HDD PROTECT

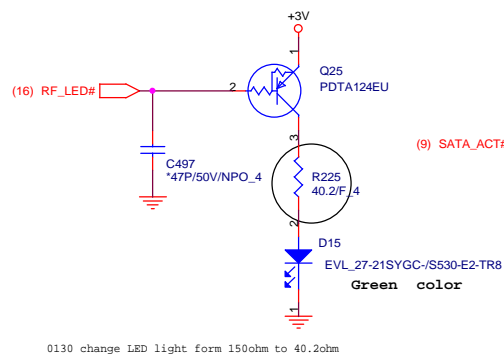


FAN

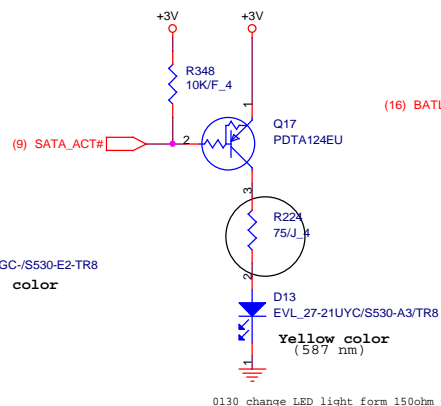




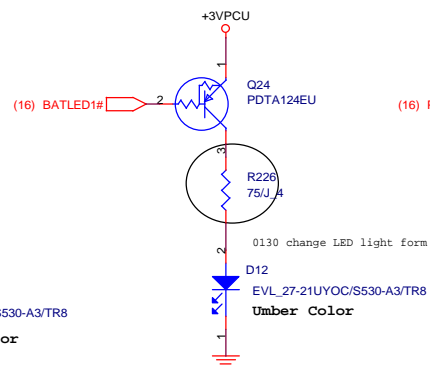
RF LED



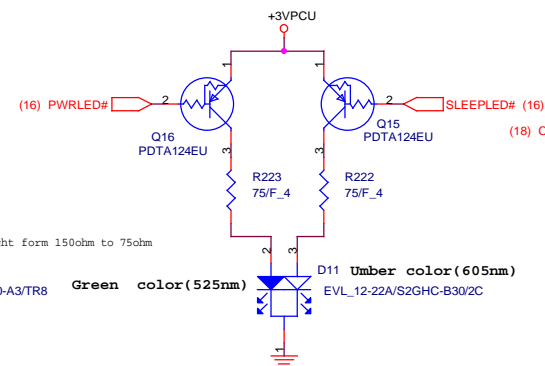
SATA LED



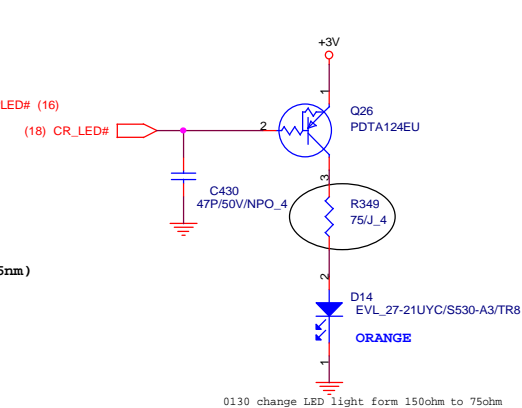
BATTERY LED



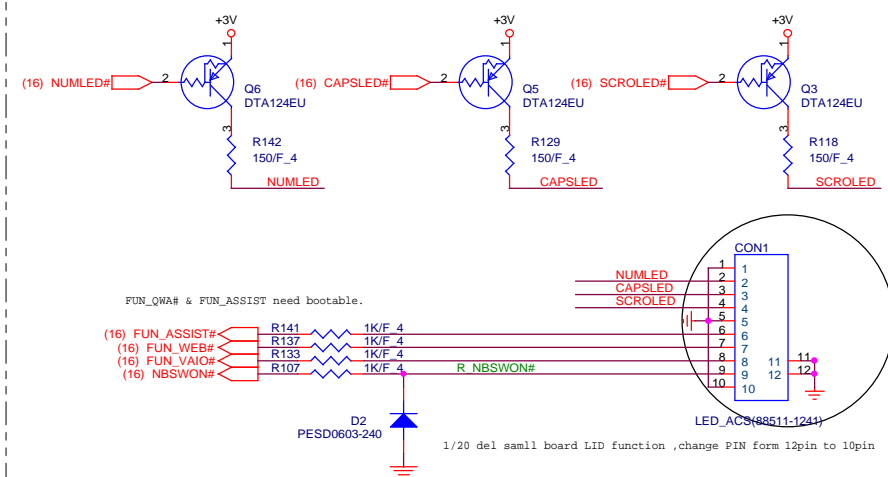
Power/Sleep LED



CARD LED

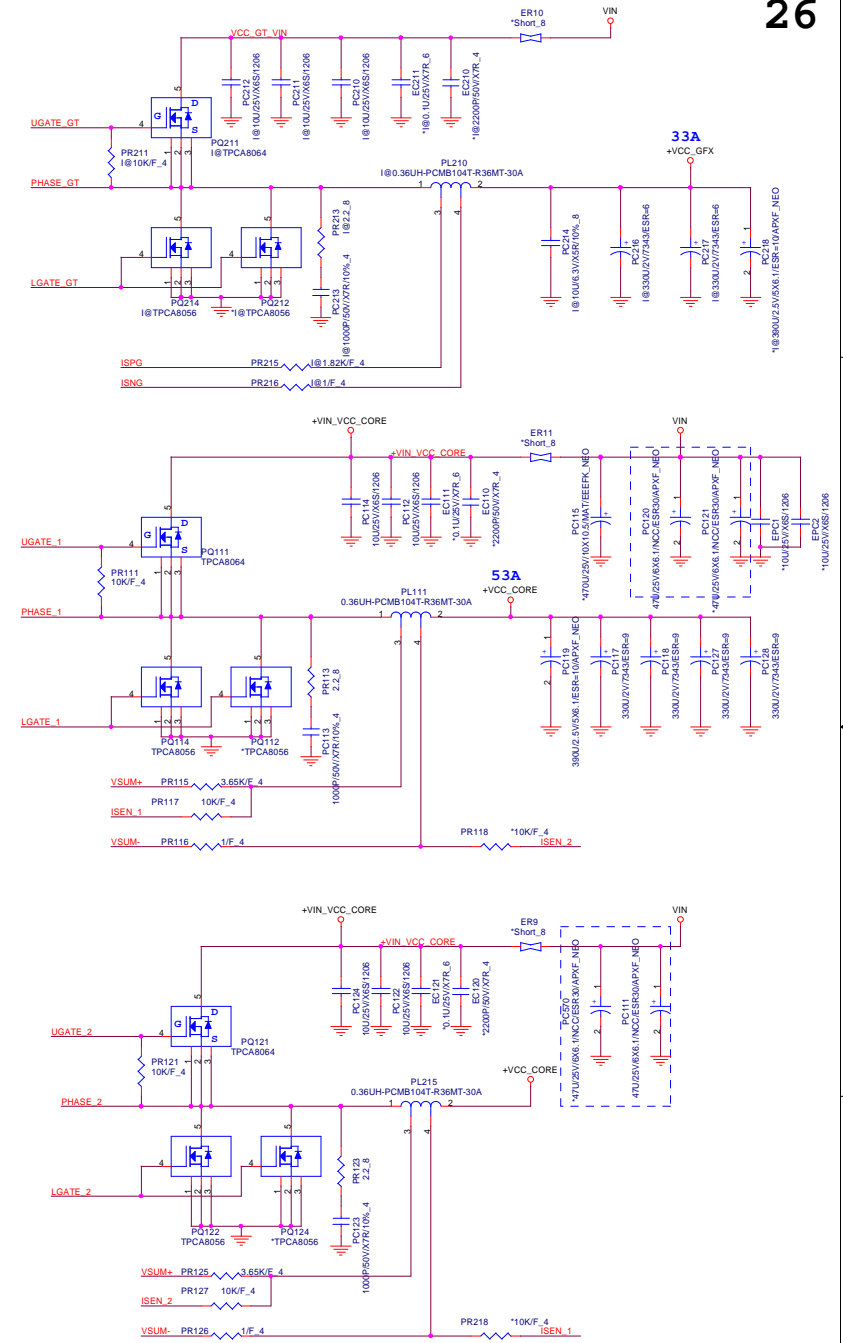


Power SW Board Connector

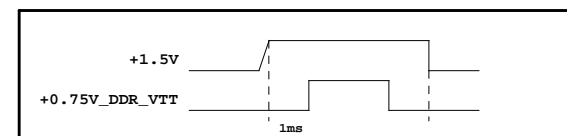
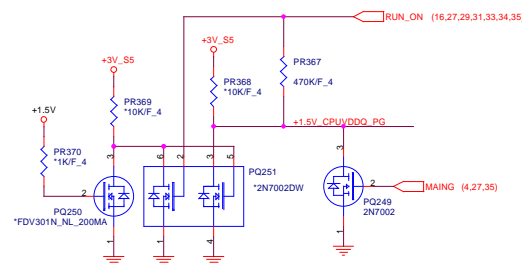
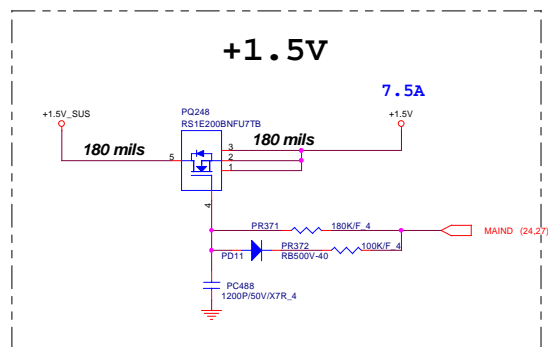
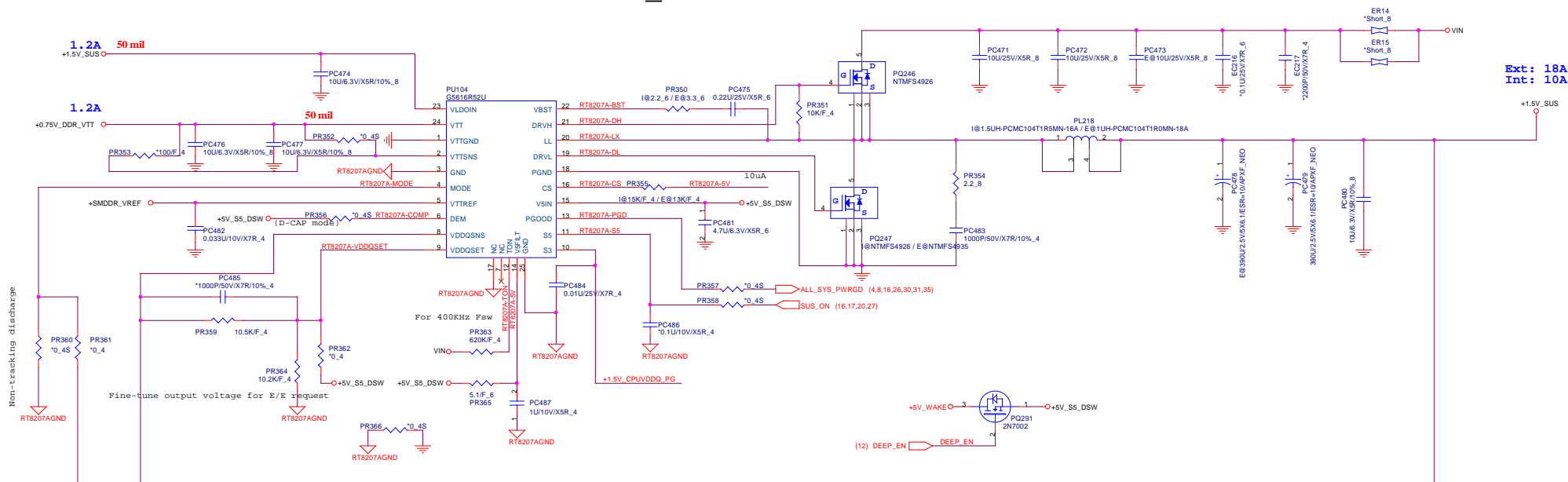


Quanta Computer Inc.
PROJECT :Chief River

Size	Document Number	Rev
	LED/RF/KB/PS	1A
Date:	Wednesday, February 01, 2012	Sheet 25 of 43



1.5VSUS & VTT_MEM

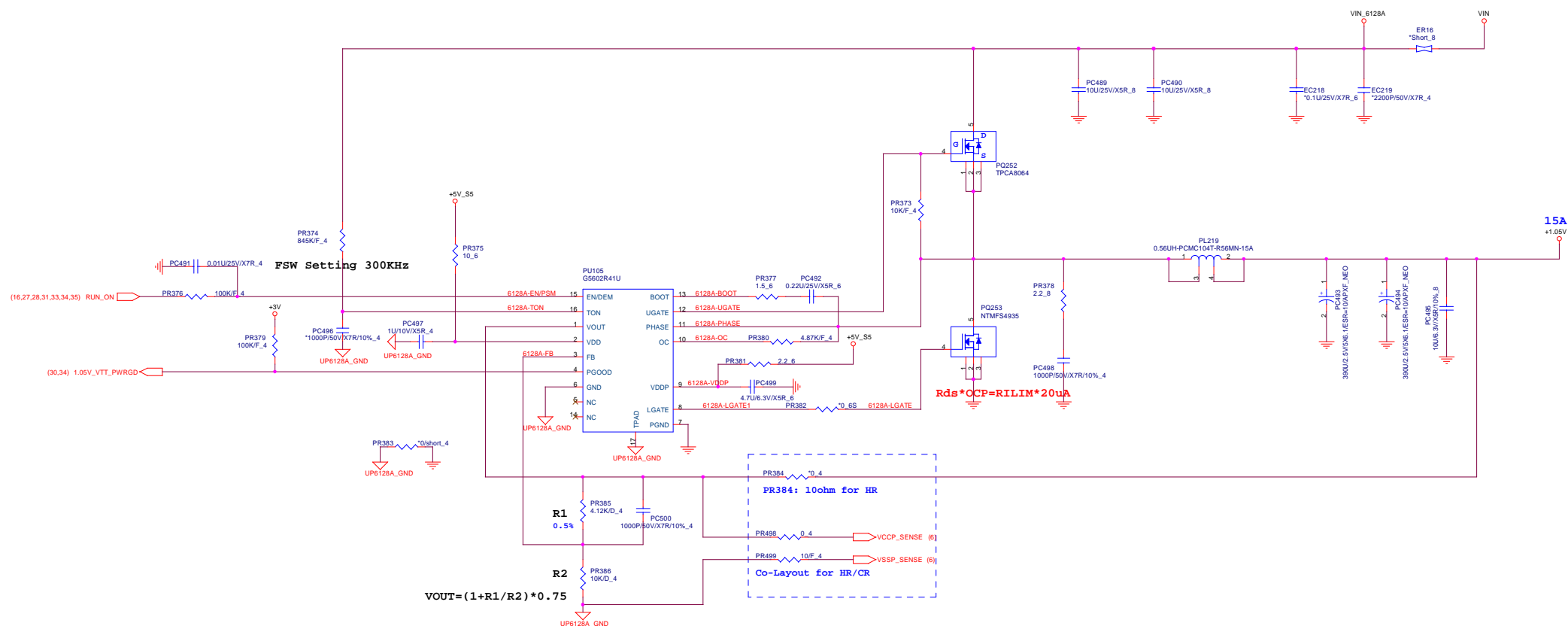


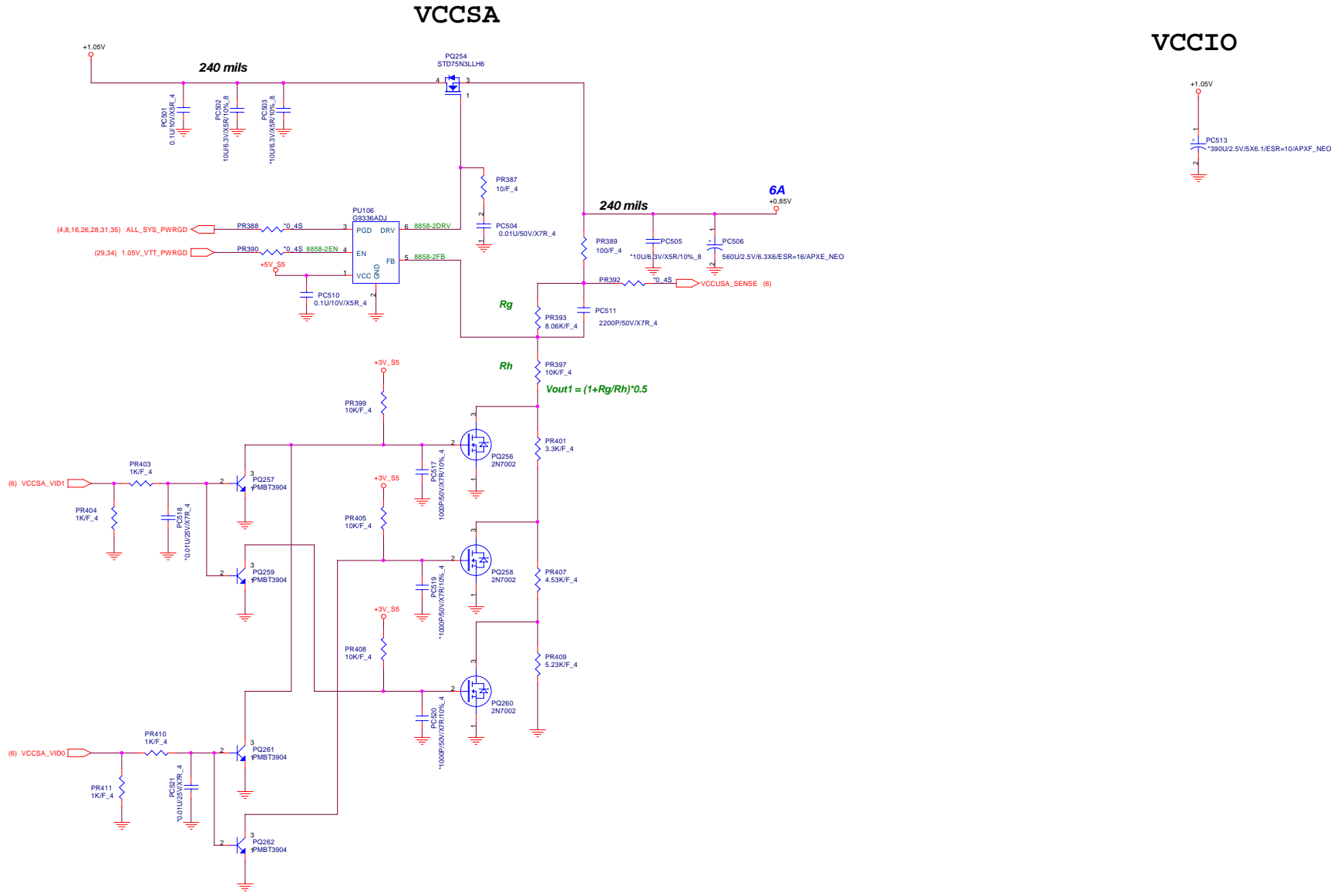
MODE	DISCHARGE MODE
+5V	No discharge
+1.5V	Tracking discharge
GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VITREF & VTT	NOTE
GND	1.5 fixed	VDDQSNS/2	DDR3
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

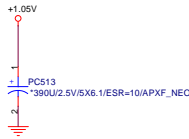
$$V_{TT} = V_{TTREF} = V_{DDQSNS}/2 = 0.75V$$

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off



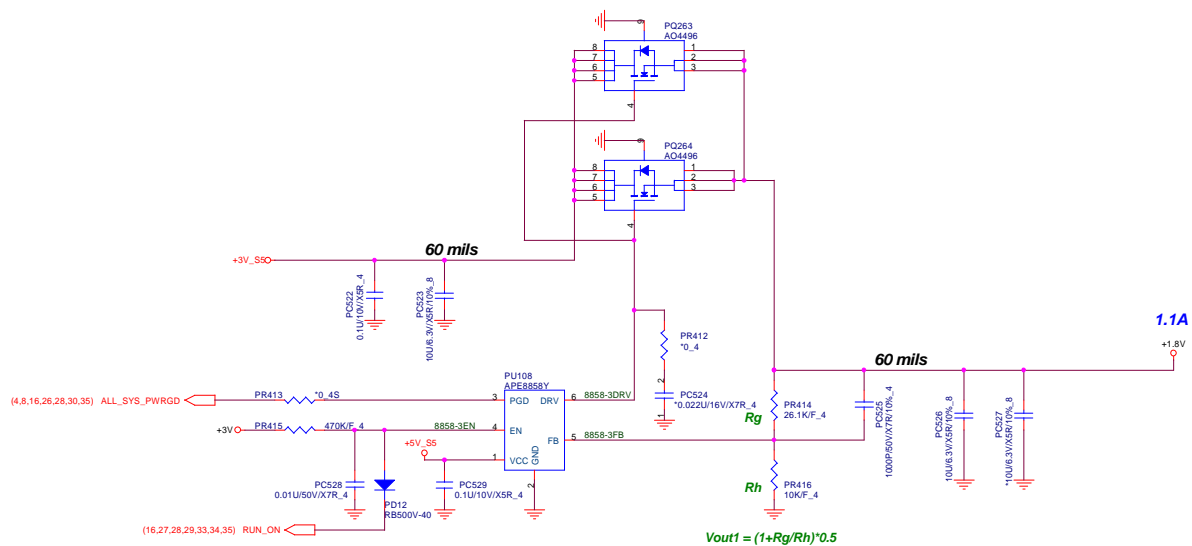


VCCIO



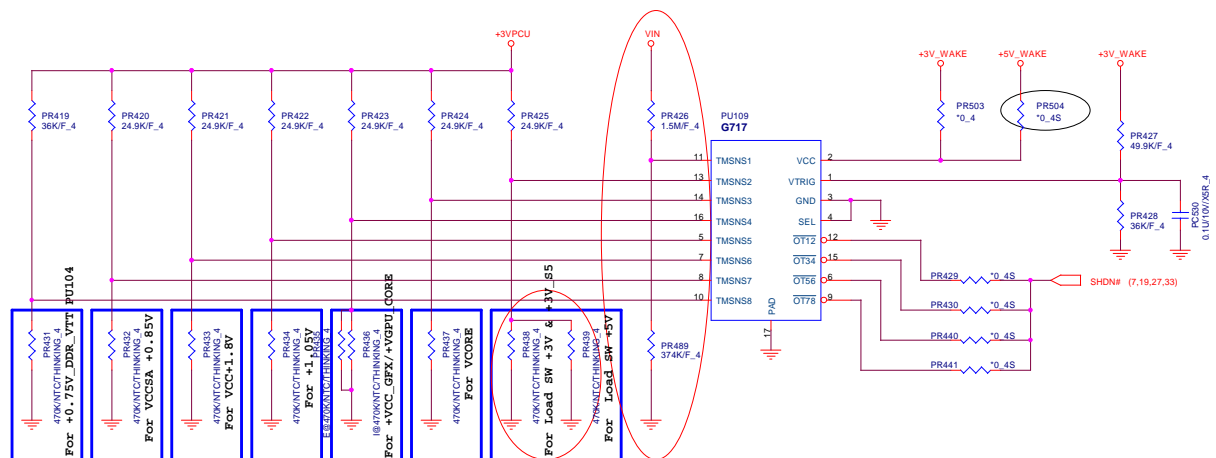
VID 0	VID 1	+0.85V
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCC1.8



Thermal Protection and Battery UVP for VEDS

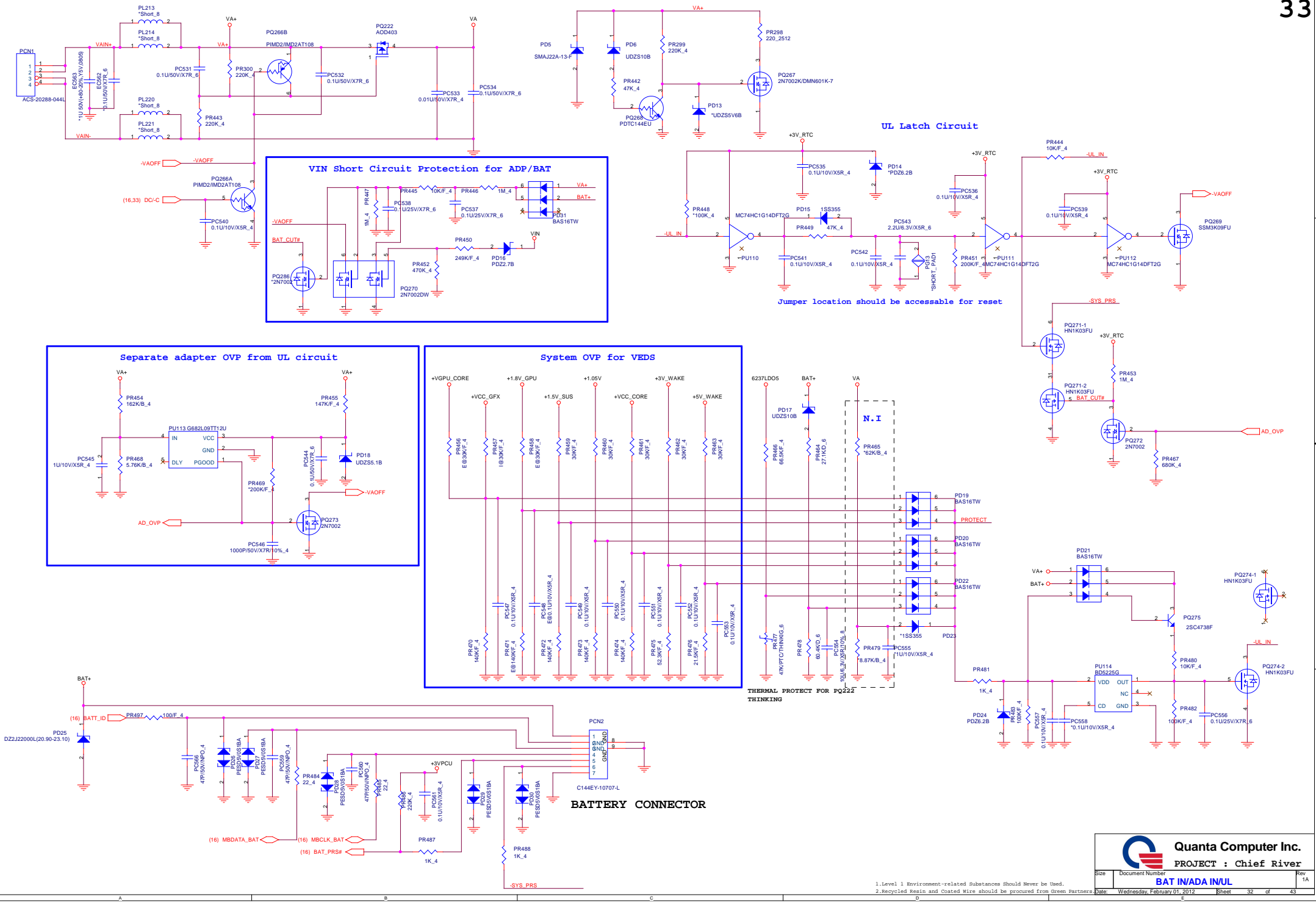
For DVT 111115

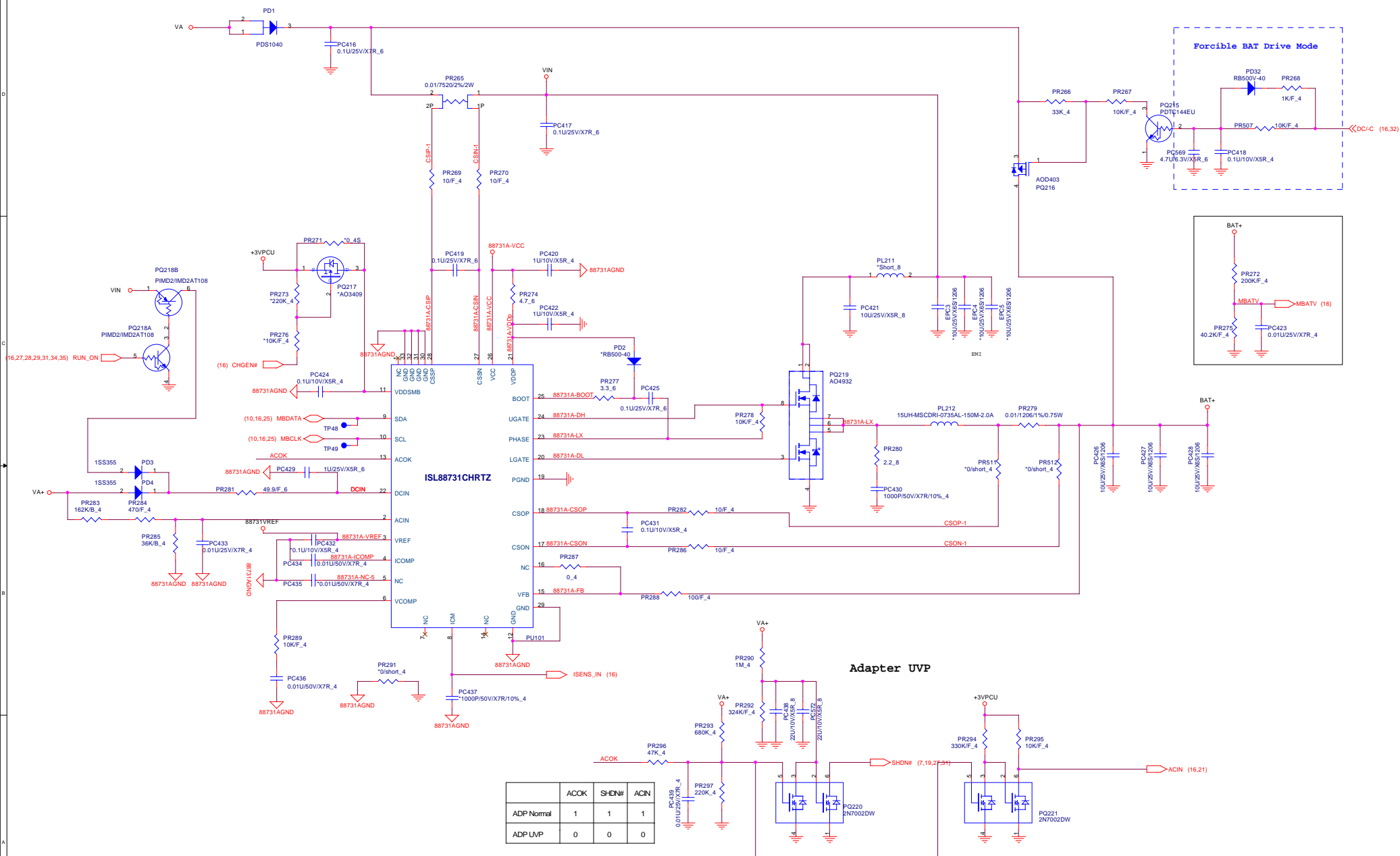


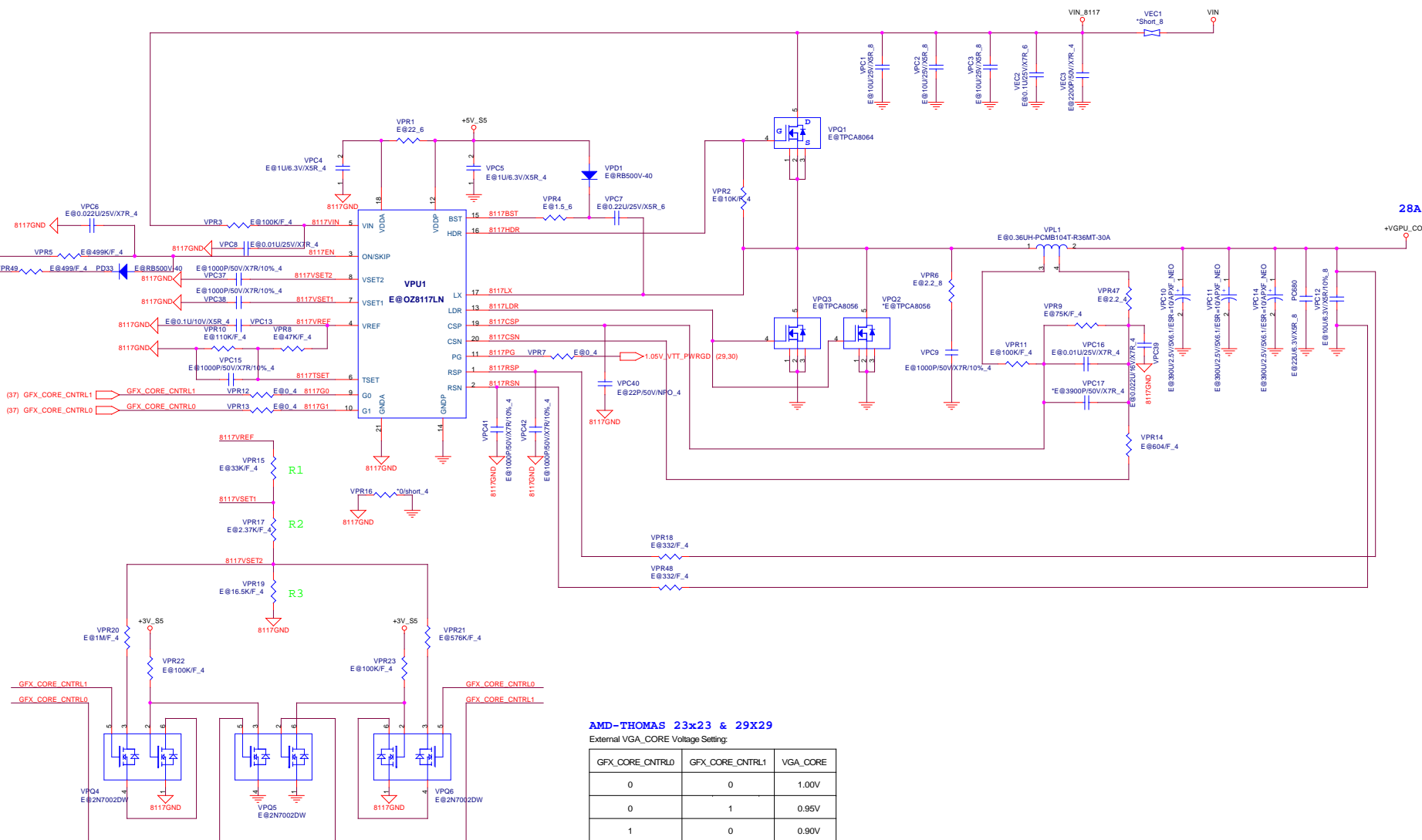
Quanta Computer Inc.
PROJECT : Chief River

Number
VCC1.8

Re







AMD-THOMAS 23x23 & 29x29

External VGA_CORE Voltage Setting:

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	VGA_CORE
0	0	1.00V
0	1	0.95V
1	0	0.90V
1	1	0.875V



Quanta Computer Inc.
PROJECT : Chief River

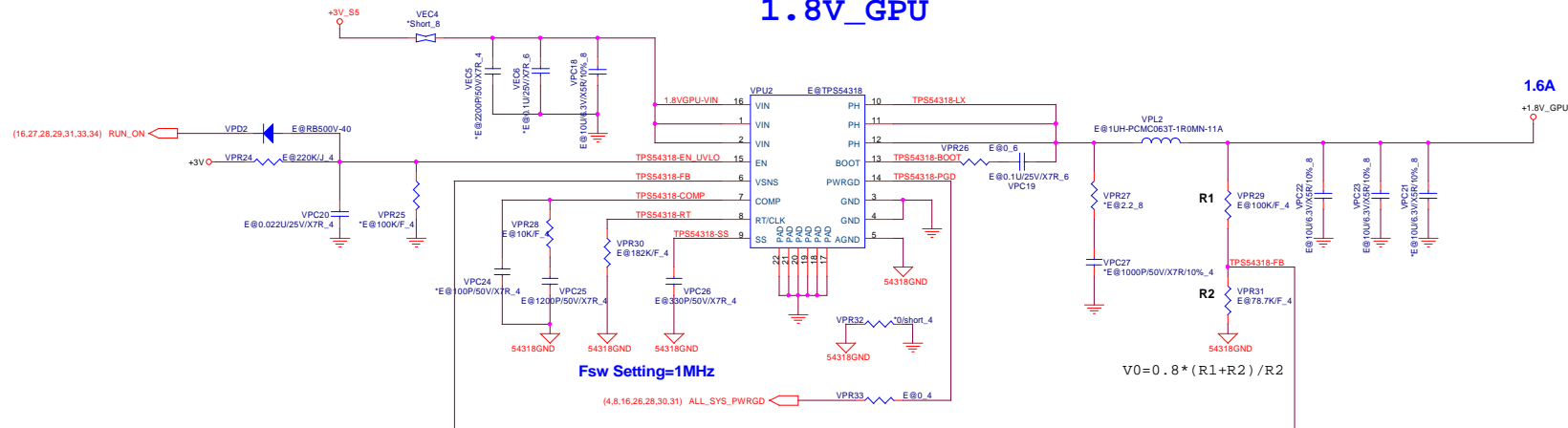
Size Document Number
VGA_CORE (OZ8117) Rev 1A

1. Level 1 Environment-related Substances Should Never be Used.

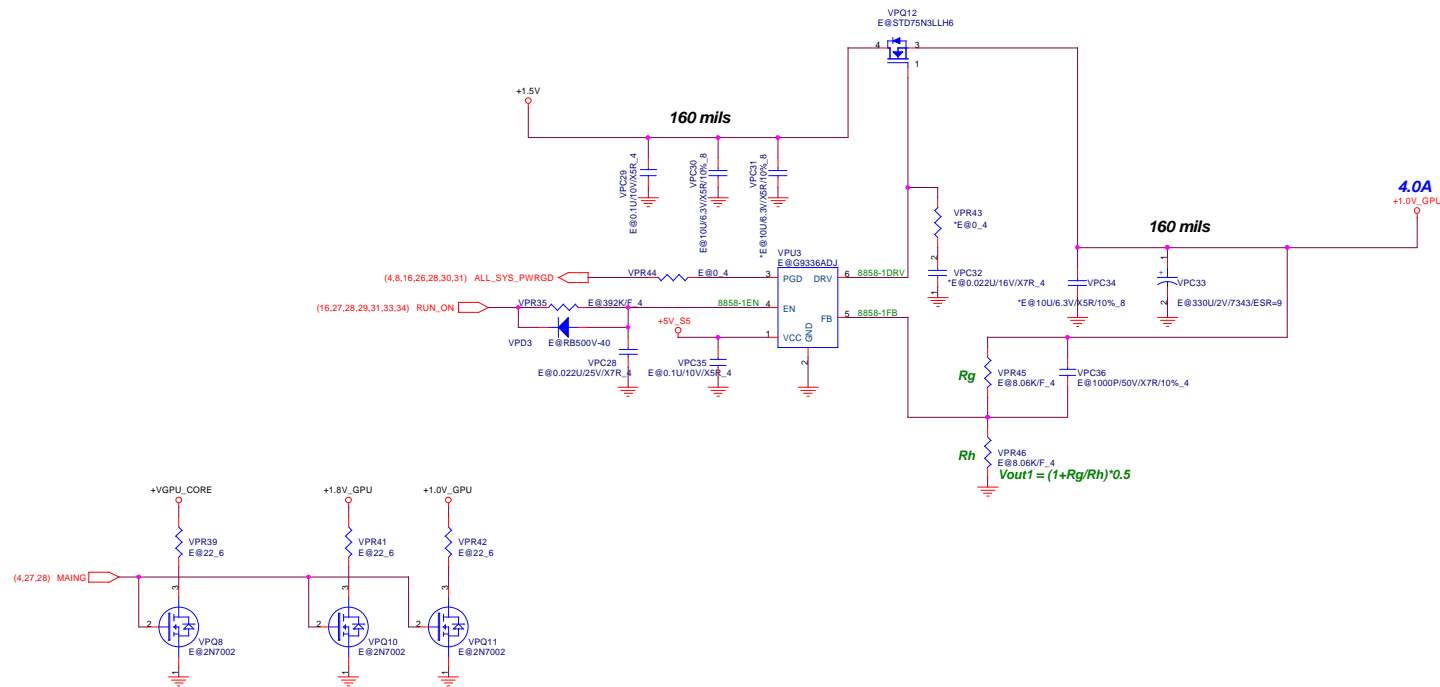
2. Recycled Resin and Coated Wire should be procured from Green Partners.

Date: Wednesday, February 01, 2012 Sheet 34 of 43

1.8V_GPU



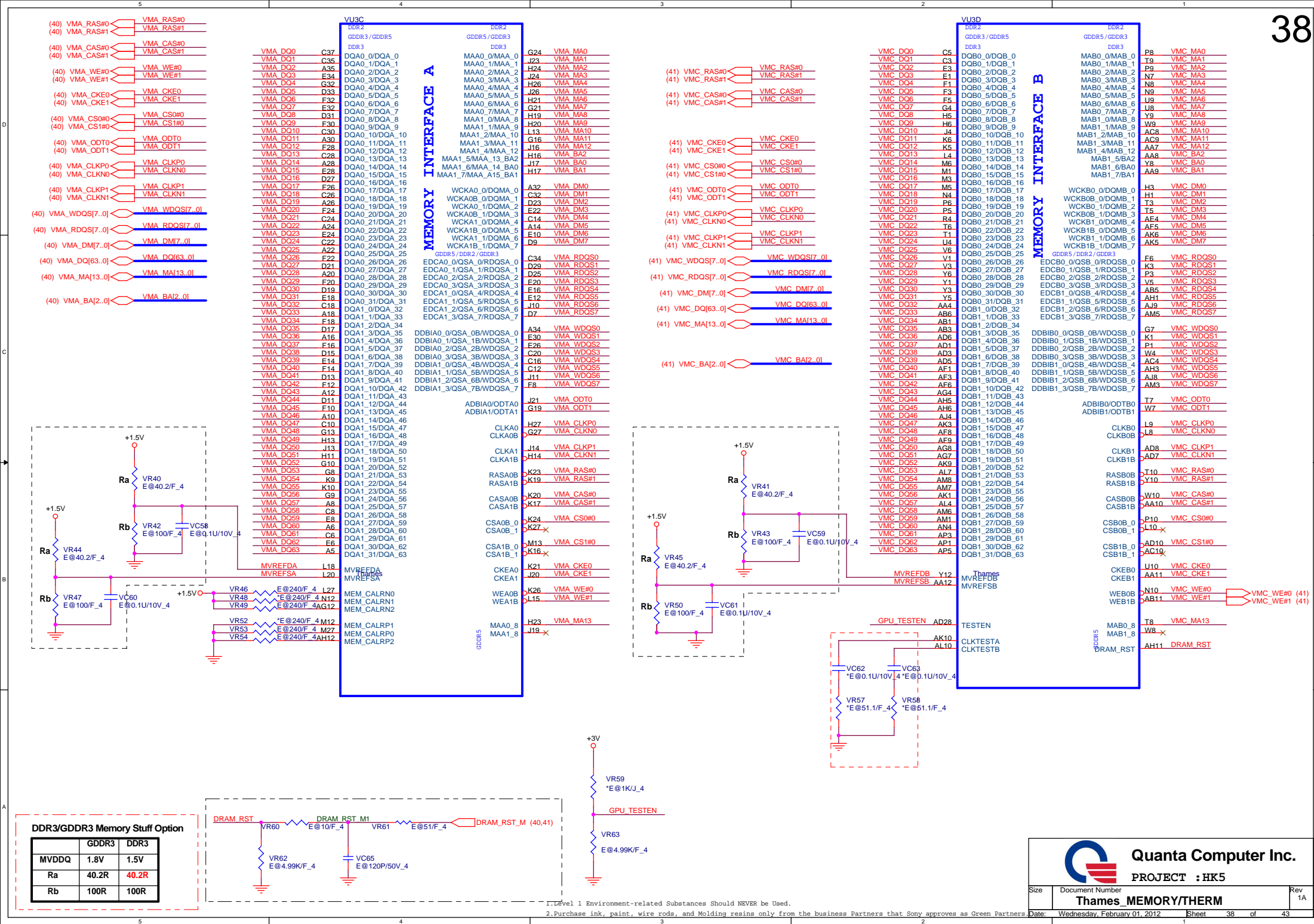
+1.0V_GPU (Support VRAM 900MHz)



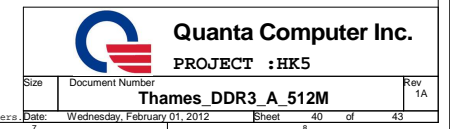


All power rails reach nominal within 20ms

```
1 => +3V_GPU
2 => +VDDC_CORE
3 => +1.0V_GPU
3 => +1.8V_GPU
```

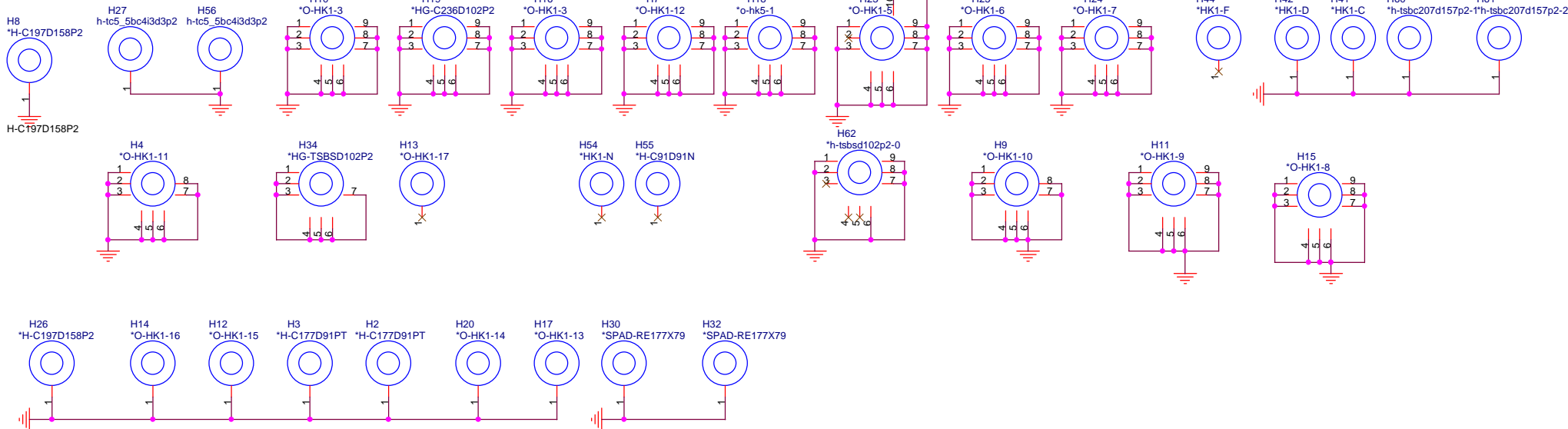




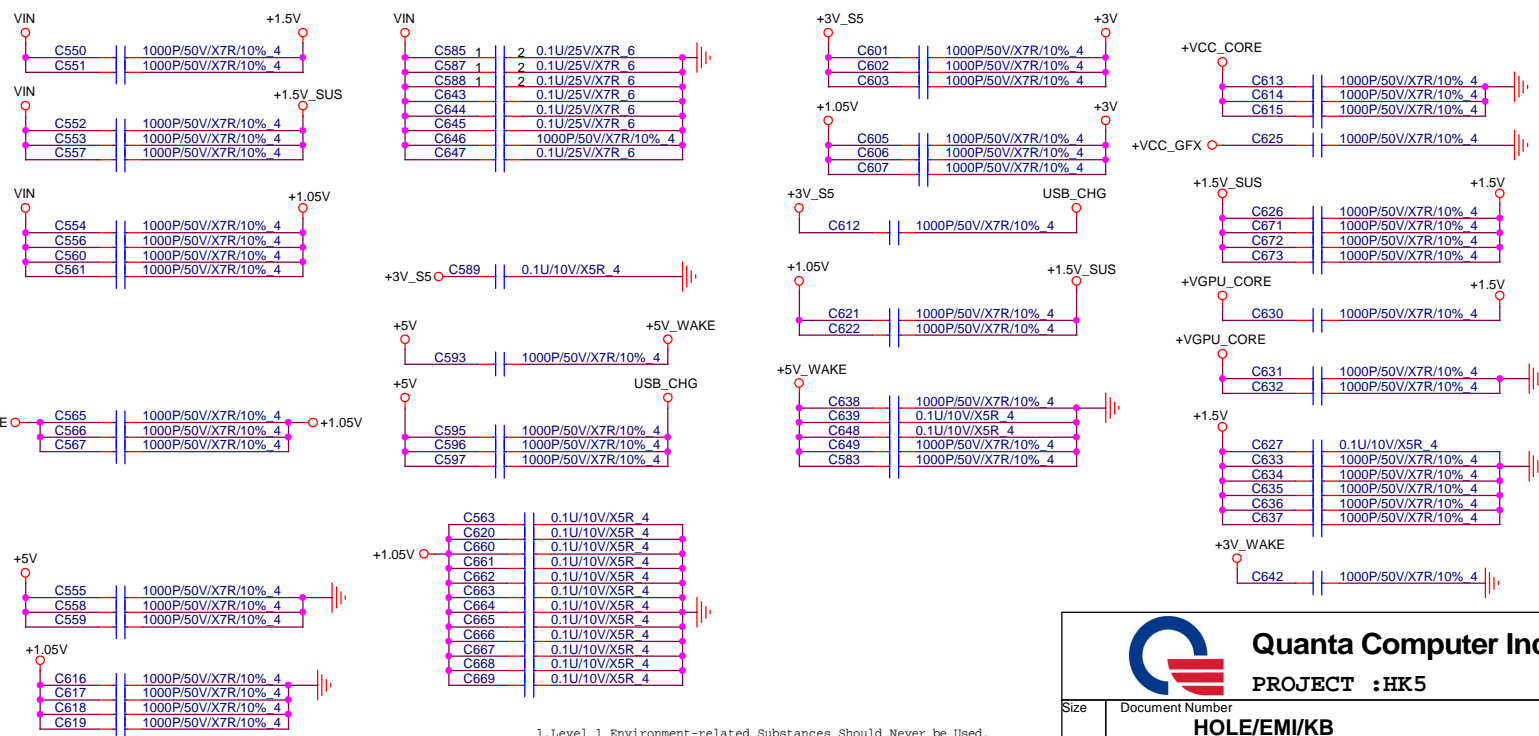
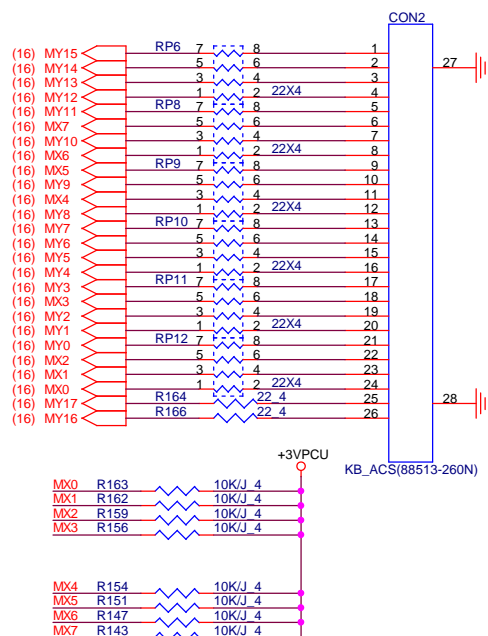


WLAN

PCH



KEY BOARD Connector



1.Level 1 Environment-related Substances Should Never be Used.

2. Recycled Resin and Coated Wire should be procured from Green Partners.

Size	Document Number	Rev
	HOLE/EMI/KB	1A
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rs. Date: Wednesday, February 01, 2012 Sheet 42 of 43

	1
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USB PORT Architecture	
PORT 0	USB3.0
PORT 1	USN2.0
PORT 2	USN2.0
PORT 3	USB2.0
PORT 4	N/A
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A
PORT 9	WiMax/BT
PORT 10	Camera
PORT 11	N/A
PORT 12	N/A
PORT 13	N/A

PCIE BUS	
PORT 1	WLAN Port
PORT 2	CARD READER
PORT 3	GLAN(RTL8111E)
PORT 4	N/A
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A

SATA BUS	
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	N/A
PORT 4	ODD
PORT 5	N/A

SM BUS	MBCLK/MBDATA	WRITE	READ	Function
ISL88731CHRTZ	0001 001X	0001 0010	0001 0011	Charger
AMD Thames	0100 0001	-	0100 0001	Graphice
LIS331DL	0011 101X	0011 1010	0011 1011	G Sensor

SM BUS	MBCLK_BAT/MBDATA_BAT	WRITE	READ	Function
VGP-BPS26	0001 011X	0001 0110	0001 0111	Battery

SM BUS	SMB_PCH_CLK/SMB_PCH_DAT	WRITE	READ	Function
DIMM Module0	1010 000X	1010 0000	1010 0001	DDRIII
DIMM Module 1	1010 010X	1010 0100	1010 0101	DDRIII
Synaptics	0010 110X	0010 1100	0010 1101	Click PAD

	R363(High) R362(Low)	R294(High) R297(low)
	Board ID3	Board ID0
14"/HK6	0	0
15"/HK5	0	1
17"/HK7	1	0

Board ID1 (VRAM Vendor)	Samaung(1)	Hynix(0)
R47(High)	Stuff	No Stuff
R48(Low)	No Stuff	Stuff

Board ID2		
14" 4PCS	1G	512M
15" 8PCS	1G	2G
R39(High)	Stuff	No Stuff
R27(Low)	No Stuff	Stuff

PCBA SKU	Discrete	UMA
R277(Pull High)	Stuff	No Stuff
R275(Pull Low)	No Stuff	Stuff

	S0	S3	DS3	S4	S5 (Charger Enable)	S5 (Charger Disable)
RUN_ON	H	L	L	L	L	L
+3V	H	L	L	L	L	L
+5V	H	L	L	L	L	L
+0.75V_DDR_VTT	H	L	L	L	L	L
+1.05V	H	L	L	L	L	L
+0.85V	H	L	L	L	L	L
+1.5V	H	L	L	L	L	L
+1.8V	H	L	L	L	L	L
+1.8V_GPU	H	L	L	L	L	L
+1.0V_GPU	H	L	L	L	L	L
+VGPU_CORE	H	L	L	L	L	L
+VCC_GFX	H	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L
SUS_ON	H	H	H	L	L	L
+1.5V_SUS	H	H	H	L	L	L
S5_ON	H	H	L	H	L	L
+5V_S5	H	H	L	H	L	L
+3V_S5	H	H	L	H	L	L
EC_WAKE_ON	H	H	H	H	H	L
+3V_WAKE	H	H	H	H	H	L
+5V_WAKE	H	H	H	H	H	L
DEEP_EC_EN	H	H	H	H	L	L
+3V_S5_DSW	H	H	H	H	L	L
+3V_SUS	H	H	L	L	L	L