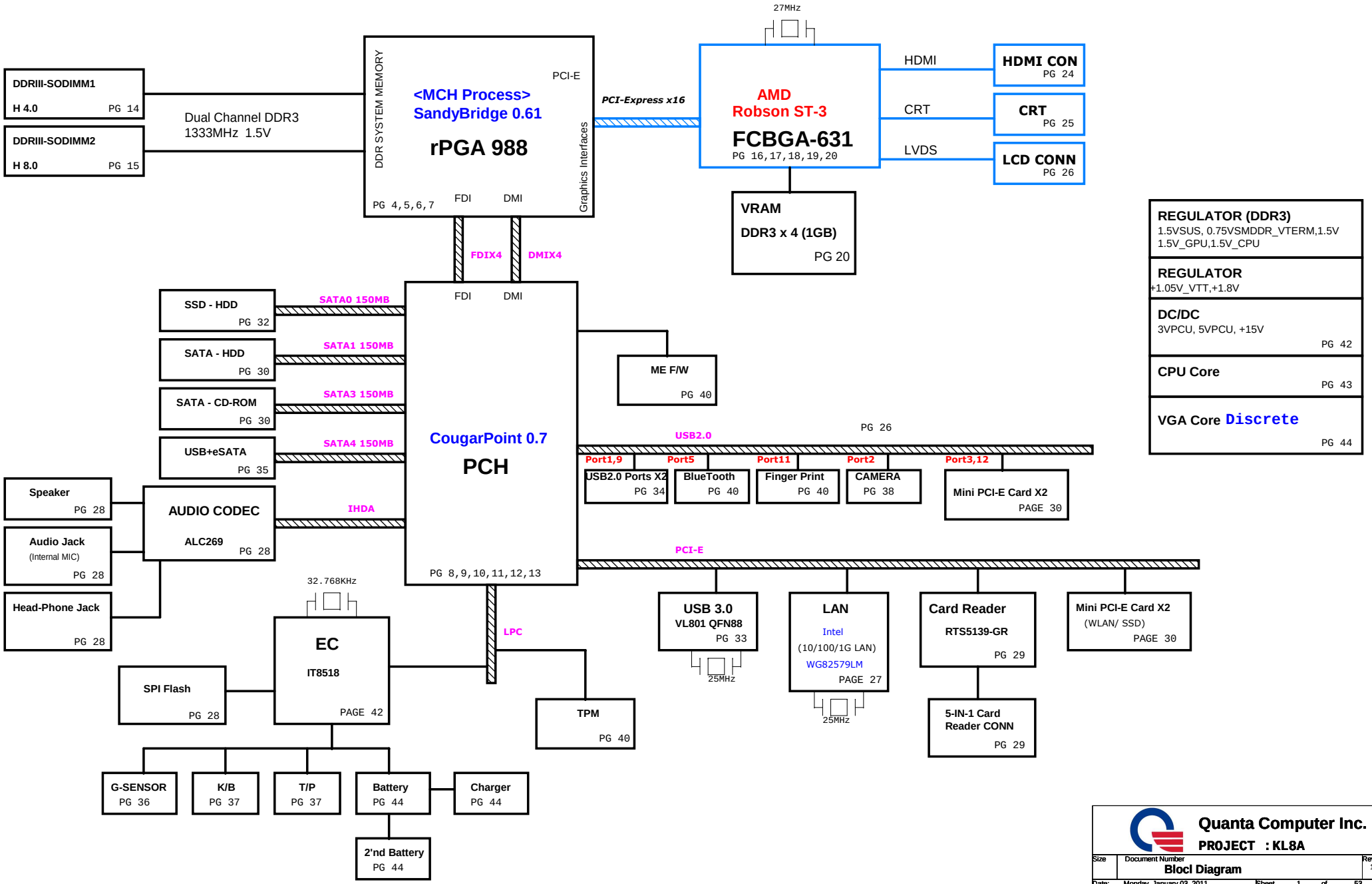
KL8A Intel Huron River Platform with Discrete GFX

FAN / THERMAL
EMC2103-2

01



Quanta Computer Inc.
PROJECT : KL8A

Size	Document Number	Rev
	Blocl Diagram	1A

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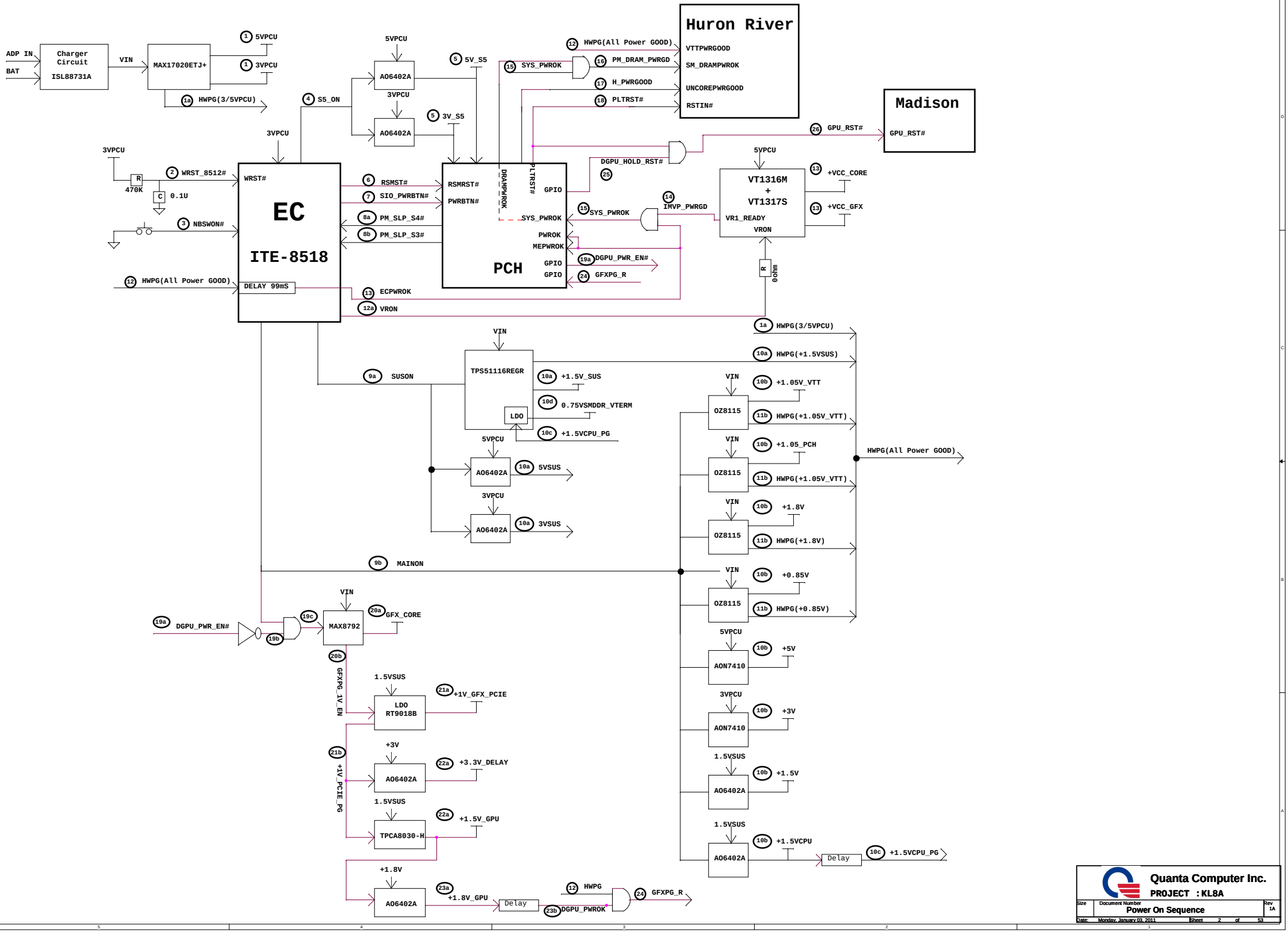
Huron River
VTTPWRGOOD
SM_DRAMPWROK
UNCOREPWRGOOD
RSTIN#
Madison
GPU_RST#
ADP IN
BAT
Charger Circuit
ISL88731A
VIN
MAX17020ETJ+
5VPCU
3VPCU
HWPG(3/5VPCU)
S5_ON
AO6402A
5V_S5
3V_S5
SYS_PWROK
PM_DRAM_PWRGD
H_PWRGOOD
PLTRST#
HWPG(All Power GOOD)
GPU_RST#
DGPU_HOLD_RST#
VT1316M + VT1317S
VR1_READY
VRON
IMVP_PWRGD
+VCC_CORE
+VCC_GFX
R 470K
C 0.1U
WRST_8512#
NBSWON#
EC
ITE-8518
WRST#
RSMRST#
PWRBTN#
DELAY 99mS
RSMST#
SIO_PWRBTN#
PM_SLP_S4#
PM_SLP_S3#
ECPWROK
VRON
PCH
DRAMPWROK
PLTRST#
GPIO
SYS_PWROK
PWROK
MEPWROK
DGPU_PWR_EN#
GFXPG_R
R 0ohm
SUSON
TPS51116REGR
LDO
+1.5V_SUS
0.75VSMDDR_VTERM
+1.5VCPU_PG
5VSUS
3VSUS
OZ8115
+1.05V_VTT
HWPG(+1.05V_VTT)
+1.05_PCH
+1.8V
HWPG(+1.8V)
+0.85V
HWPG(+0.85V)
AON7410
+5V
+3V
+1.5V
+1.5VCPU
Delay
+1.5VCPU_PG
MAINON
MAX8792
GFX_CORE
DGPU_PWR_EN#
GFXPG_1V_EN
LDO RT9018B
+1V_GFX_PCIE
+1V_PCIE_PG
+3.3V_DELAY
TPCA8030-H
+1.5V_GPU
+1.8V_GPU
HWPG
DGPU_PWROK
Quanta Computer Inc.
PROJECT : KL8A
Power On Sequence
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CLK Gen(CLK)

03

02/20 DEL for Pre-ES1

CPU_CLK select(CLK)

02/20 DEL for Pre-ES1

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

Quanta Computer Inc.

PROJECT : KL8A

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	CLKGEN N.A	1A

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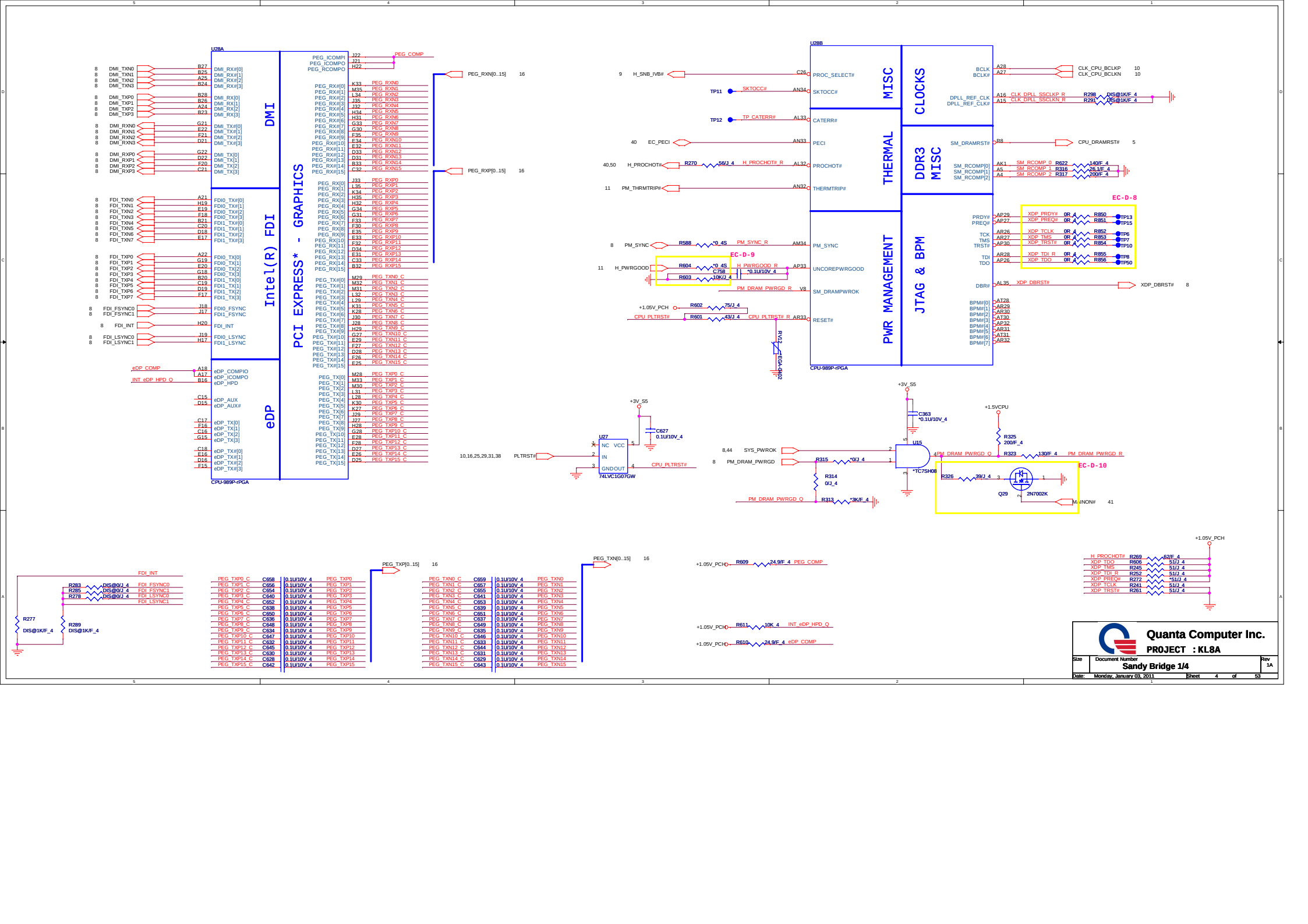
U28A
DMI
Intel(R) FDI
eDP
PCI EXPRESS* - GRAPHICS
CPU-989P-rPGA
U28B
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
CPU-989P-rPGA
EC-D-8
EC-D-9
EC-D-10
U27
74LVC1G07GW
U15
*TC7SH08
Q29
2N7002K
Quanta Computer Inc.
PROJECT : KL8A
Sandy Bridge 1/4
Rev 1A
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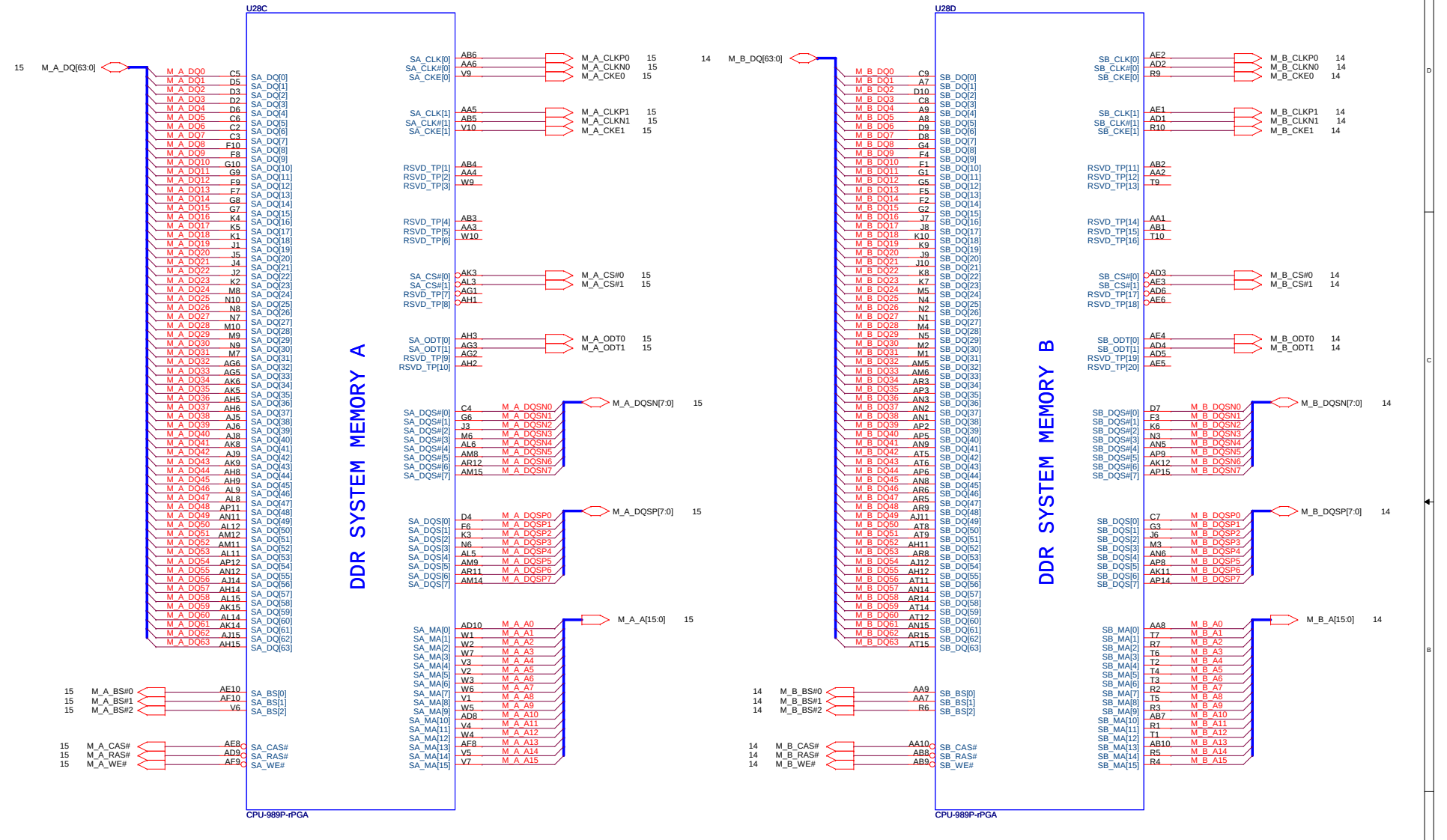
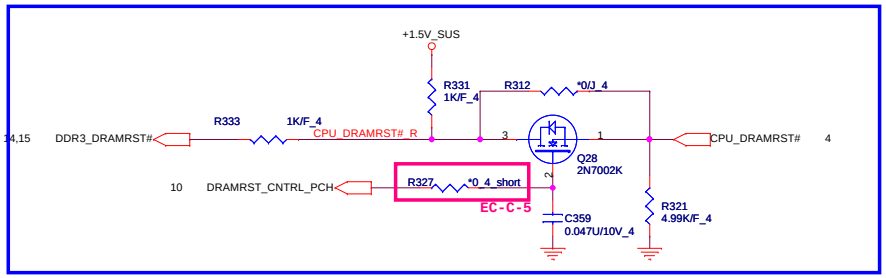
Sandy Bridge Processor (DDR3)

05





Quanta Computer Inc.			
PROJECT : KL8A			
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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

06

CPU Core Power
SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)

CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)

CPU VGT
SNB 45W:22A
22uF x 12
22uF x 4 (Reserved)

CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

POWER
CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES
GRAPHICS
DDR3 -1.5V RAILS
SA RAIL
1.8V RAIL
MISC
SENSE LINES
VREF

Reserved

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
SVID DATA
SVID ALERT
Close to VR
Place PU resistor close to CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

Quanta Computer Inc.
PROJECT : KL8A
Size | Document Number: Sandy Bridge 3/4 | Rev: 1A
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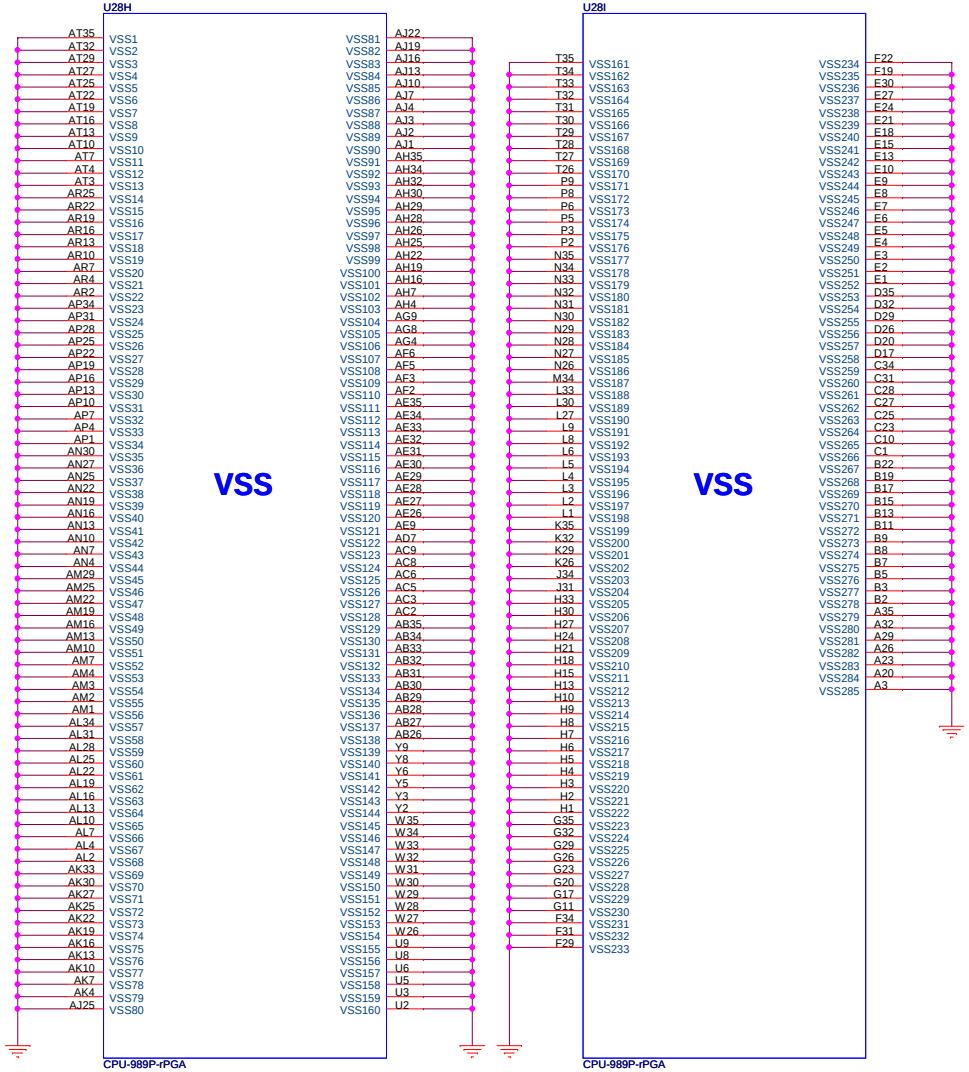
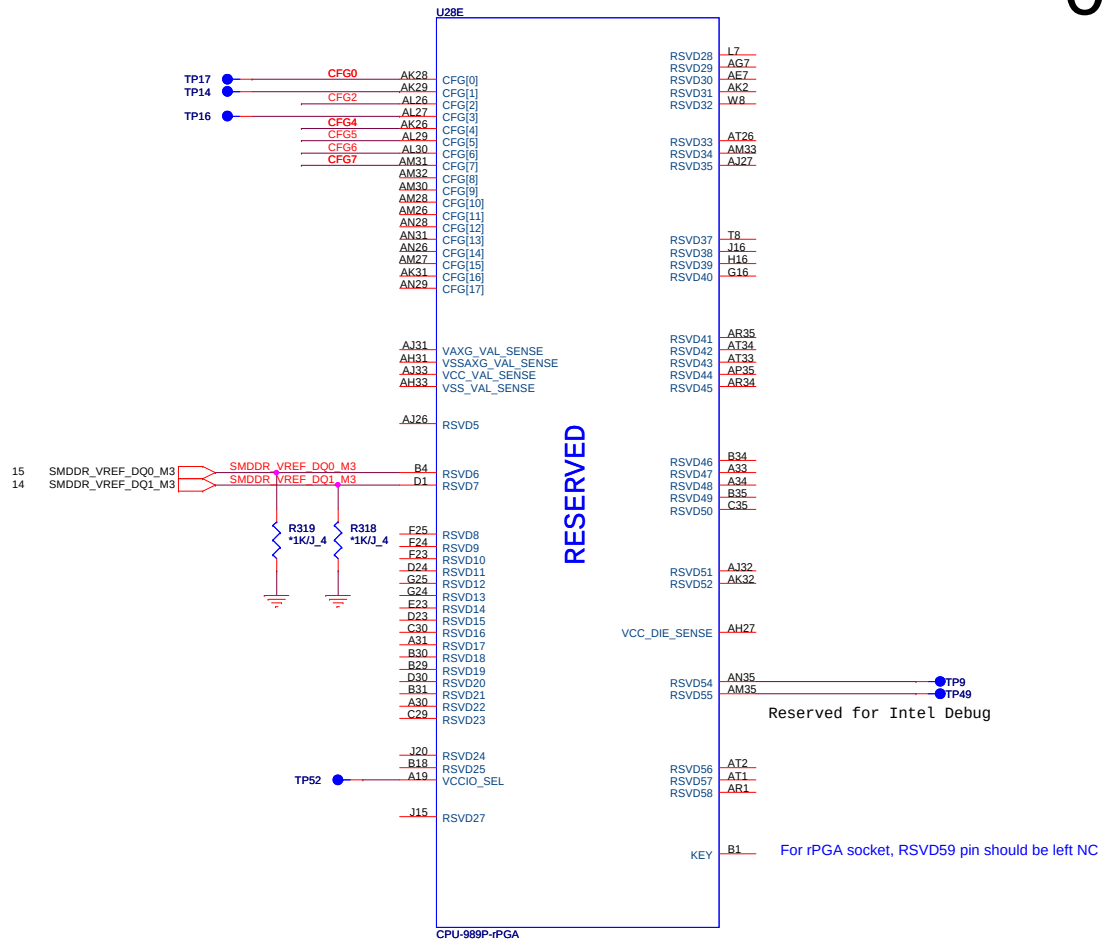
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

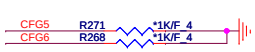


07

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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PROJECT : KL8A

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	Sandy Bridge 4/4	1A
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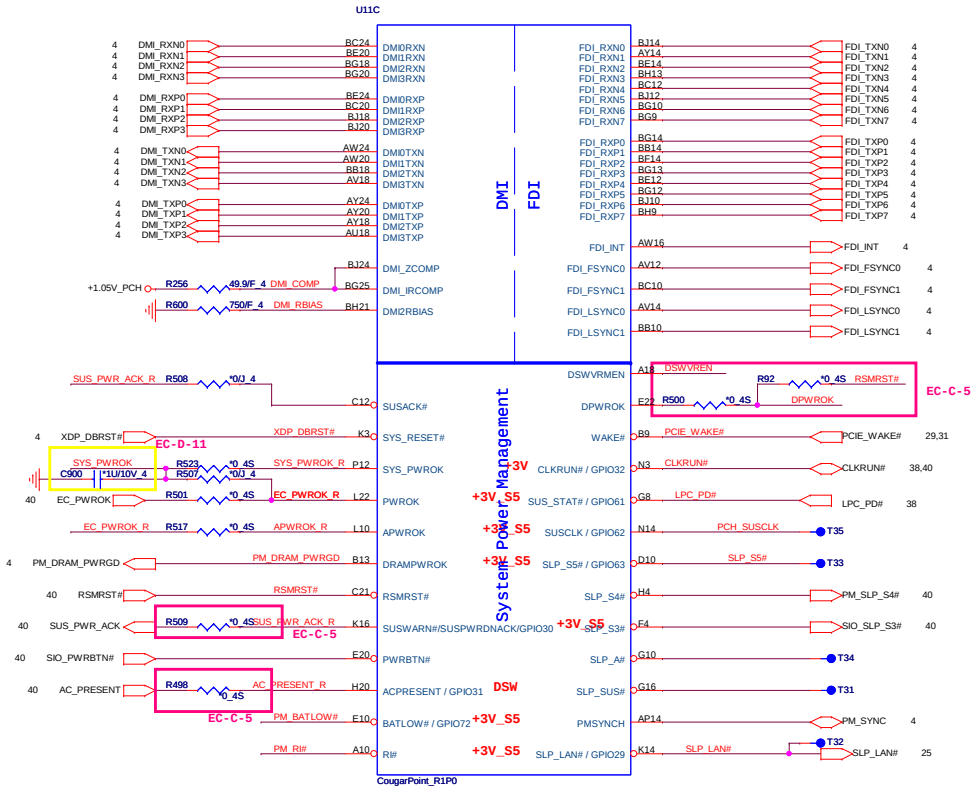
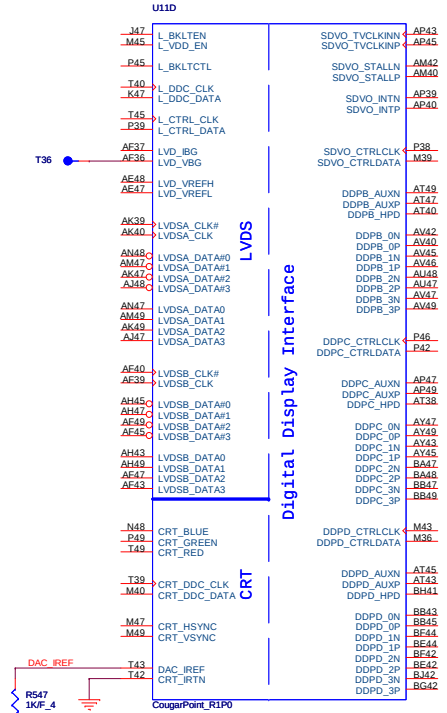
Cougar Point (DMI,FDI,PM)



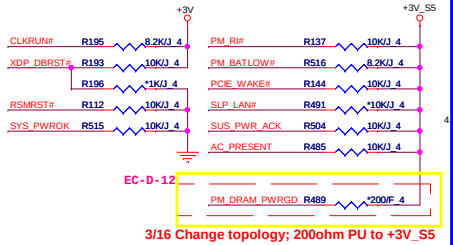
Cougar Point (LVDS,DDI)



20ohm for SW;
33ohm for UMA

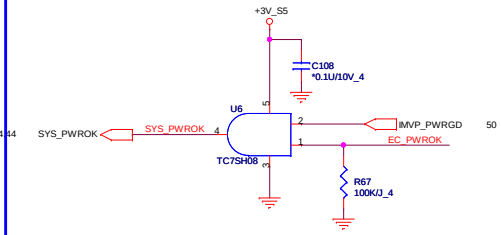
Deep sleep option	Support	Not support
SUS_PWR_ACK	To PCH SUSACK# (Pop R597)	EC or NC (Non-pop R597)
DPWROK	DSWPWRGD (Pop Q54, R663, Q55, R677)	RSMRST (Pop R639)
SLP_SUS	EC	NC

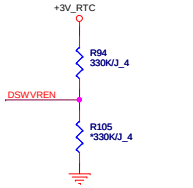
PCH Pull-high/low(CLG)



3/16 Change topology; 200ohm PU to +3V_S5

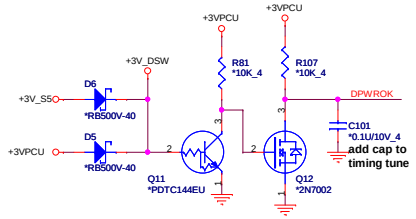
System PWR_OK(CLG)





On Die DSW VR Enable
High = Enable (Default)
Low = Disable

DPWROK FOR DSW



Quanta Computer Inc.
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	Cougar Point 1/6	1A
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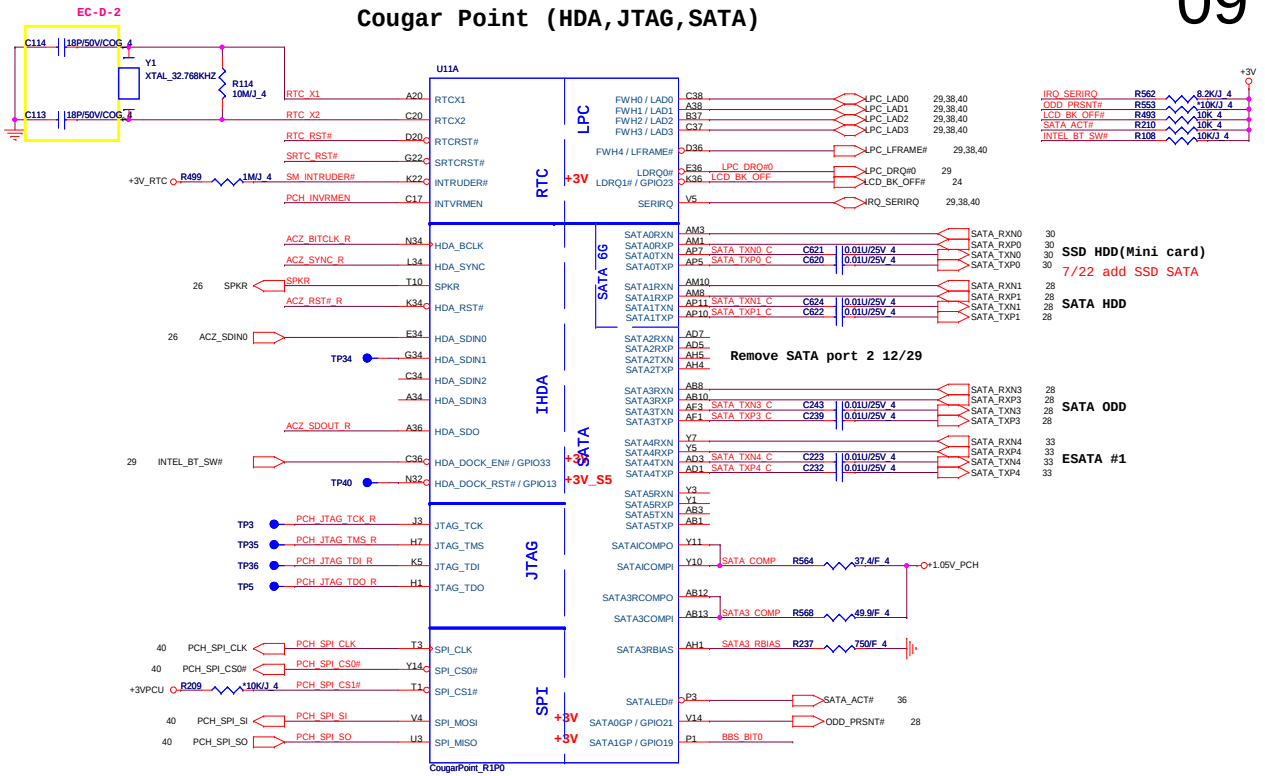
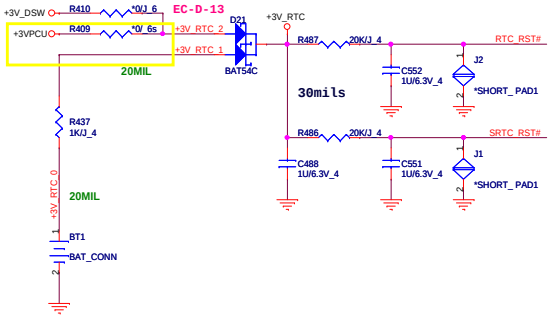
PCH2(CLG)

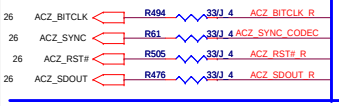
Cougar Point (HDA,JTAG,SATA)



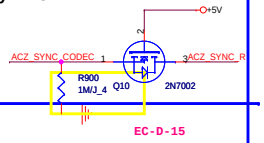
RTC Circuitry(RTC)



HDA Bus(CLG)

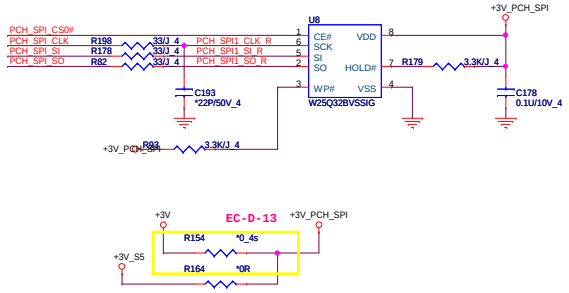


To Separate Codec Sync by PD3



PCH JTAG Debug (CLG)

PCH Dual SPI (CLG)

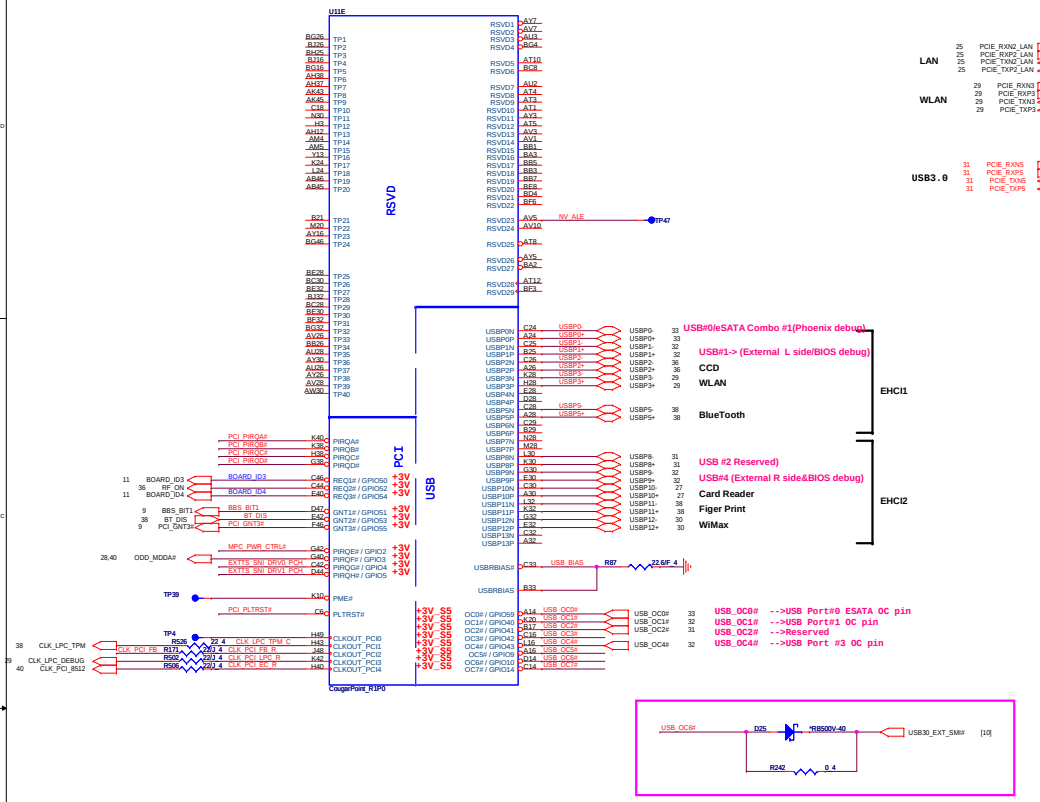


PCH Strap Table

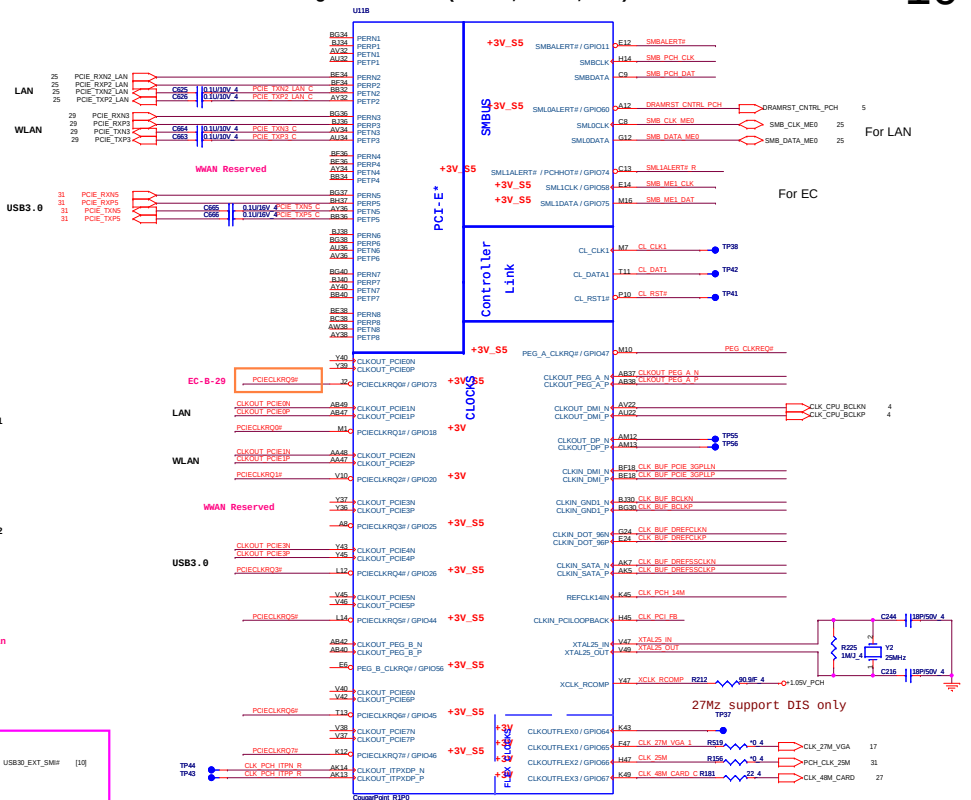
Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

Cougar Point-M (PCI,USB,NVRAM)



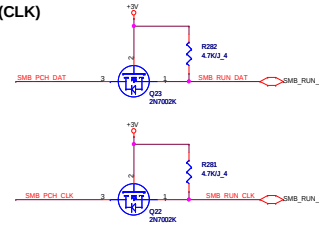
Cougar Point-M (PCI-E,SMBUS,CLK)



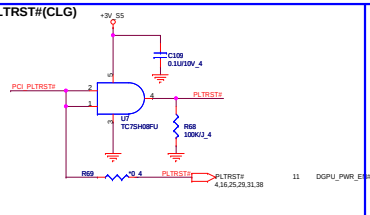
DGPU Power ON

PEG CLK detect

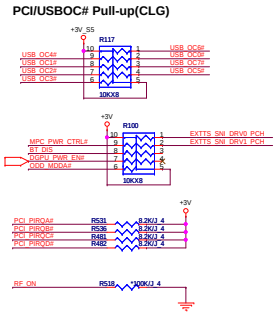
SMBus(CLK)

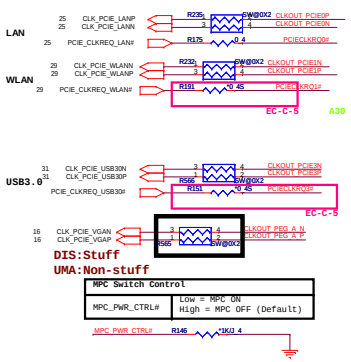


PLTRST#(CLG)

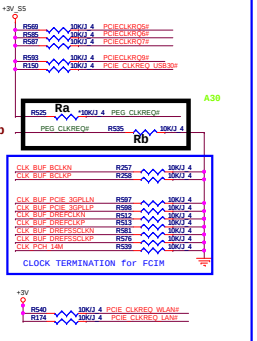


PCI/USBOC# Pull-up(CLG)

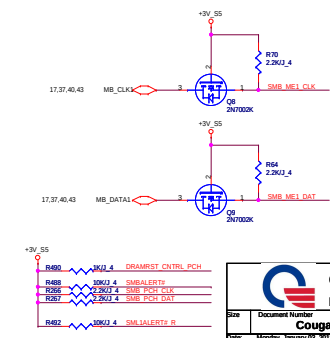


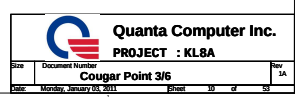


CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)





Cougar Point (GPIO,VSS_NCTF,RSVD)

U11F

S_GPIO R549 100_4 — T7 BMBUSY# / GPIO0 +3V
31,40 EC_EXT_SMI# — A42 TACH1 / GPIO1 +3V
BOARD_ID0 — H36 TACH2 / GPIO6 +3V
40 EC_EXT_SCI# — E38 TACH3 / GPIO7 +3V
SYSTEM_ID — C10 GPIO8 +3V_S5
25 LAN_DISABLE# — C4 LAN_PHY_PWR_CTRL / GPIO12 +3V_S5
HOST_ALERT#1_R — G2 GPIO15 +3V_S5
29 WLAN_OFF# — U2 SATA4GP / GPIO16 +3V
DGPU_PWROK — D40 TACH0 / GPIO17 +3V
BIOS_REC — T5 SCLOCK / GPIO22 +3V
30 SDD_DA_DSS — E8 GPIO24 / MEM_LED +3V_S5
GPIO27 — E16 GPIO27 DSW
9,40 PLL_ODVR_EN — R542 *0_4S — P8 GPIO28 +3V_S5
EC-C-5
STP_PCI# — K1 STP_PCI# / GPIO34 +3V
38 BT_ON# — K4 GPIO35 +3V
10 DGPU_PWR_EN# — V8 SATA2GP / GPIO36 +3V
TP60 — M5 SATA3GP / GPIO37 +3V
MFG_MODE — N2 SLOAD / GPIO38 +3V
FDI_OVRVLTG — M3 SDATAOUT0 / GPIO39 +3V
TEST_SET_UP — V13 SDATAOUT1 / GPIO48 +3V
37,40 TEMP_ALERT# — V3 SATA5GP / GPIO49 +3V
SV_DET — D6 GPIO57 +3V_S5

GPIO

C40 BOARD_ID1 — TACH4 / GPIO68 +3V
B41 T30 — TACH5 / GPIO69 +3V
C41 SSD_DETECT# 30 — TACH6 / GPIO70 +3V
A40 BOARD_ID2 — TACH7 / GPIO71 +3V

CPU/MISC

A20GATE — P4 — EC_A20GATE 40
PECI — AU16 — TP46
RCIN# — P5 EC_RCIN# — EC_RCIN# 40
PROCPWRGD — AY11 — H_PWRGOOD 4
THRMTRIP# — AY10 PCH_THRMTRIP# R591 390/J_4 — PM_THRMTRIP# 4
INIT3_3V# — T14
DF_TVS — AY1 — DF_TVS 9

TS_VSS1 — AH8
TS_VSS2 — AK11
TS_VSS3 — AH10
TS_VSS4 — AK10
NC_1 — P37

3/16 Connected to GND
DG rev0.9

NCTF

VSS_NCTF_1 A4
VSS_NCTF_2 A44
VSS_NCTF_3 A45
VSS_NCTF_4 A46
VSS_NCTF_5 A5
VSS_NCTF_6 A6
VSS_NCTF_7 B3
VSS_NCTF_8 B47
VSS_NCTF_9 BD1
VSS_NCTF_10 BD49
VSS_NCTF_11 BE1
VSS_NCTF_12 BE49
VSS_NCTF_13 BF1
VSS_NCTF_14 BF49
VSS_NCTF_15 BG2
VSS_NCTF_16 BG48
VSS_NCTF_17 BH3
VSS_NCTF_18 BH47
VSS_NCTF_19 BJ4
VSS_NCTF_20 BJ44
VSS_NCTF_21 BJ45
VSS_NCTF_22 BJ46
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ6
VSS_NCTF_25 C2
VSS_NCTF_26 C48
VSS_NCTF_27 D1
VSS_NCTF_28 D49
VSS_NCTF_29 E1
VSS_NCTF_30 E49
VSS_NCTF_31 F1
VSS_NCTF_32 F49

CougarPoint_R1P0

GPIO Pull-up/Pull-down(CLG)

+3V_S5
LAN_DISABLE# R158 10K/J_4
+3V
EC_EXT_SMI# R90 10K/J_4
EC_EXT_SCI# R483 10K/J_4
SSD_DETECT# R111 10K/J_4
STP_PCI# R194 10K/J_4
EC_A20GATE R546 10K/J_4
EC_RCIN# R545 10K/J_4
TEMP_ALERT# R218 10K/J_4
BT_ON# R533 10K/J_4
DGPU_PWROK R496 10K/J_4
WLAN_OFF# R558 10K/J_4
GPIO27 R511 10K/J_4

EC-B-16

Board ID	ID2 GPIO71	ID1 GPIO68	ID0 GPIO6
KL7	0	0	0
KL8	0	1	0
KL9	1	0	0
KL8A	0	1	1
KL9A	1	0	1

+3V
R109 *10K/J_4 BOARD_ID0 R88 10K/J_4
R484 *10K/J_4 BOARD_ID1 R475 10K/J_4
R110 10K/J_4 BOARD_ID2 R89 *10K/J_4
R503 10K/J_4 BOARD_ID3 R497 *10K/J_4
R479 10K/J_4 BOARD_ID4 R480 *10K/J_4
R143 10K/J_4 SYSTEM_ID R145 *10K/J_4
10 BOARD_ID3 — BOARD_ID3
10 BOARD_ID4 — BOARD_ID4

SV_SET_UP
High = Strong (Default)
TEST_SET_UP R555 10K/J_4 R561 *0/J_4

EC-D-1
+3V_S5
R522 *10K/J_4 SV_DET R520 100K/J_4

SGPIO
S_GPIO R556 10K/J_4 R557 *0/J_4

HOST_ALERT#1_R R521 1K/J_4
Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

R544 100K/J_4 FDI_OVRVLTG R541 *1K/F_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

SDD_DA_DSS R677 200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS_REC R560 10K/J_4 R554 *0/J_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST
MFG_MODE R203 10K/J_4 R201 *0/J_4

Quanta Computer Inc.
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	Cougar Point 6/6	1A
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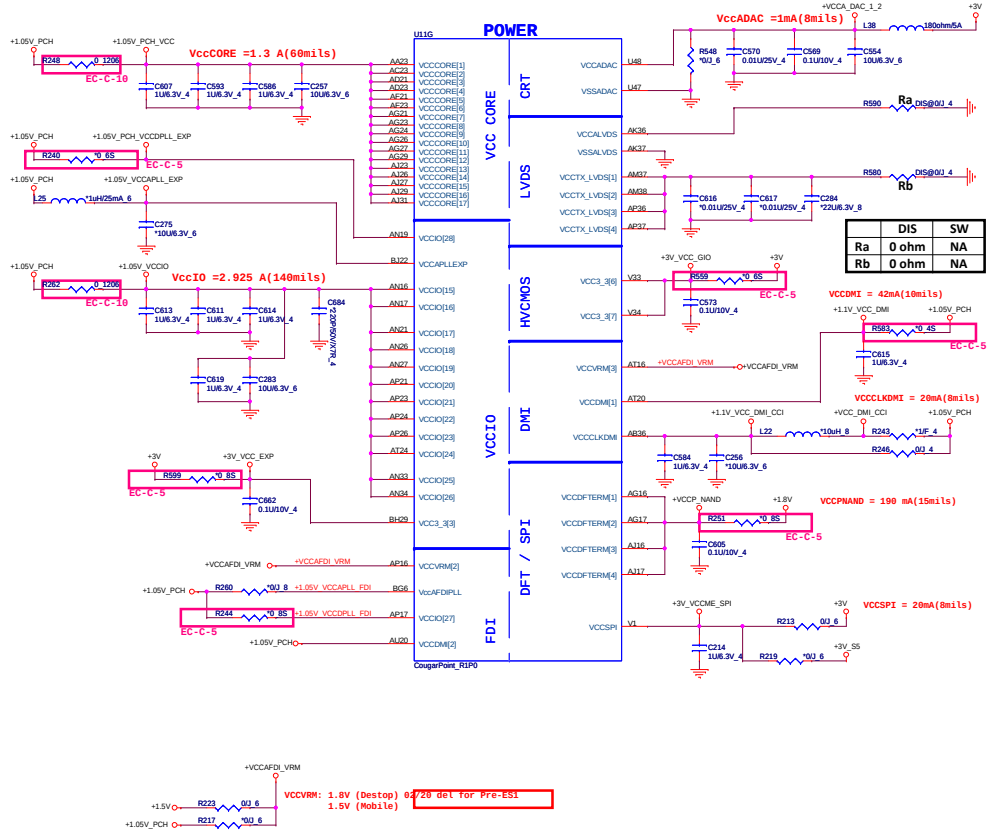
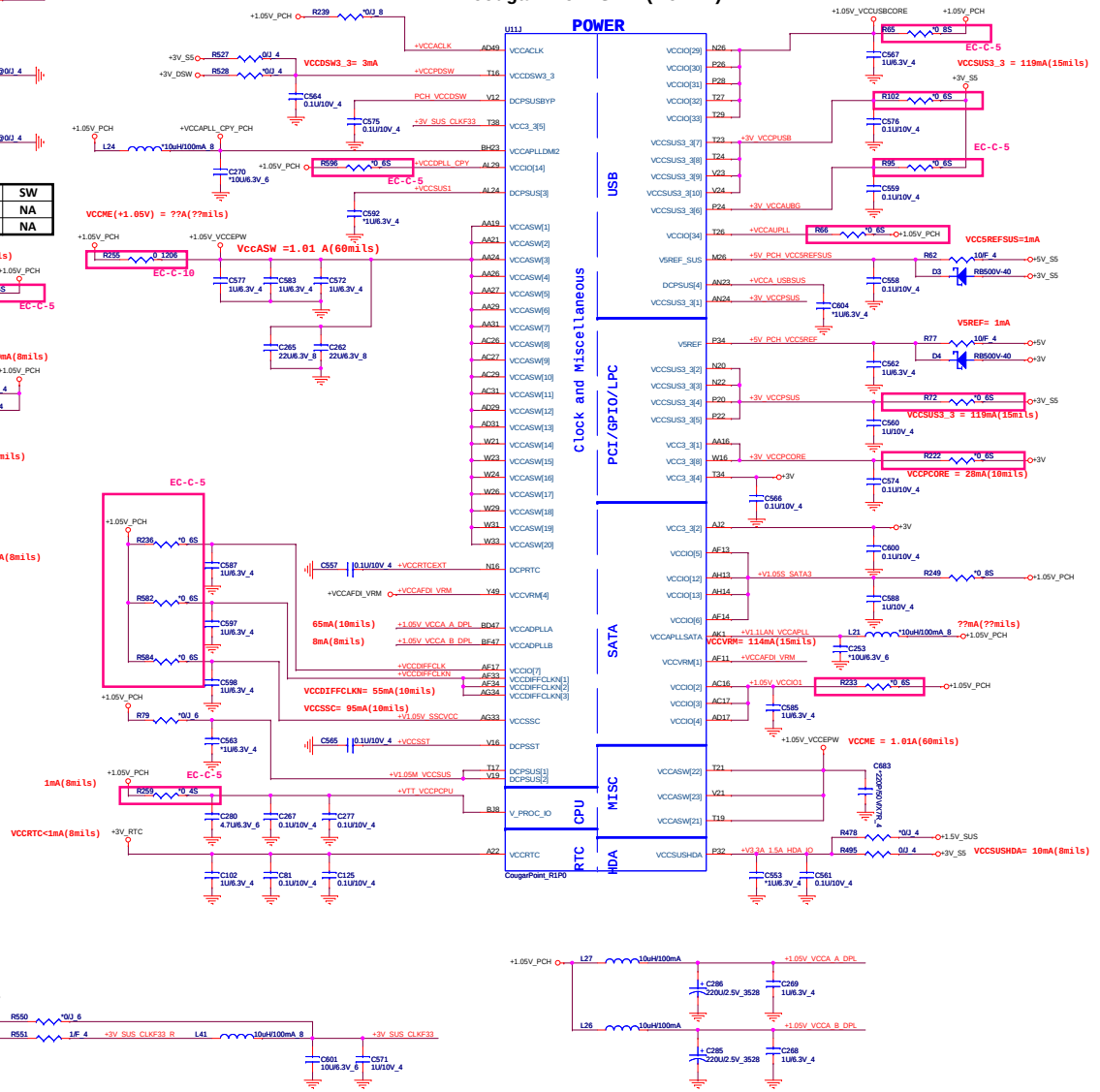
COUGAR POINT (POWER)



Cougar Point-M (POWER)



Quanta Computer Inc.		
PROJECT : KL8A		
Size	Document Number: Cougar Point 5/6	Rev: 1A
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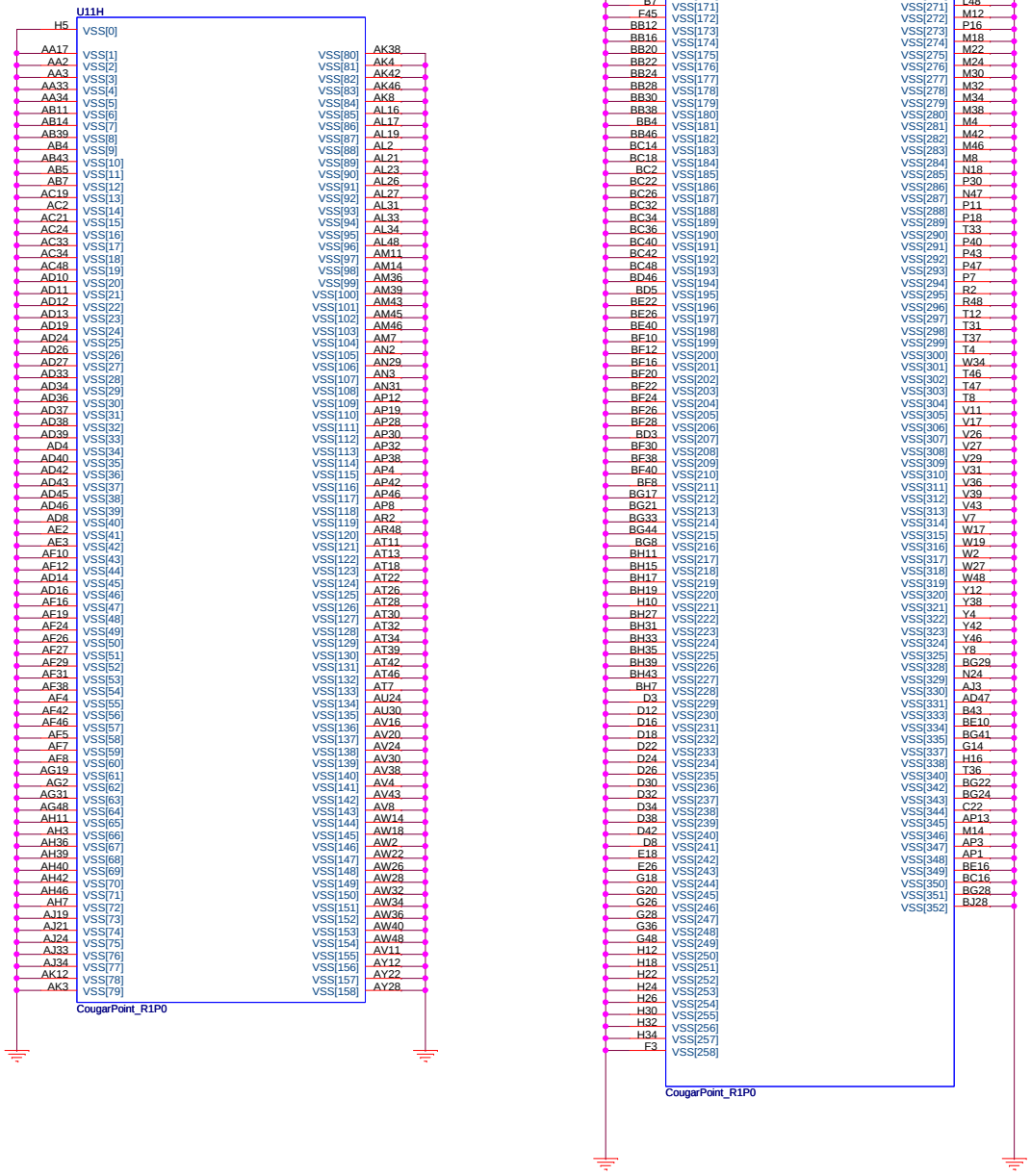
IBEX PEAK-M (GND)



Quanta Computer Inc.

PROJECT : KL8A

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	Cougar Point 6/6	1A
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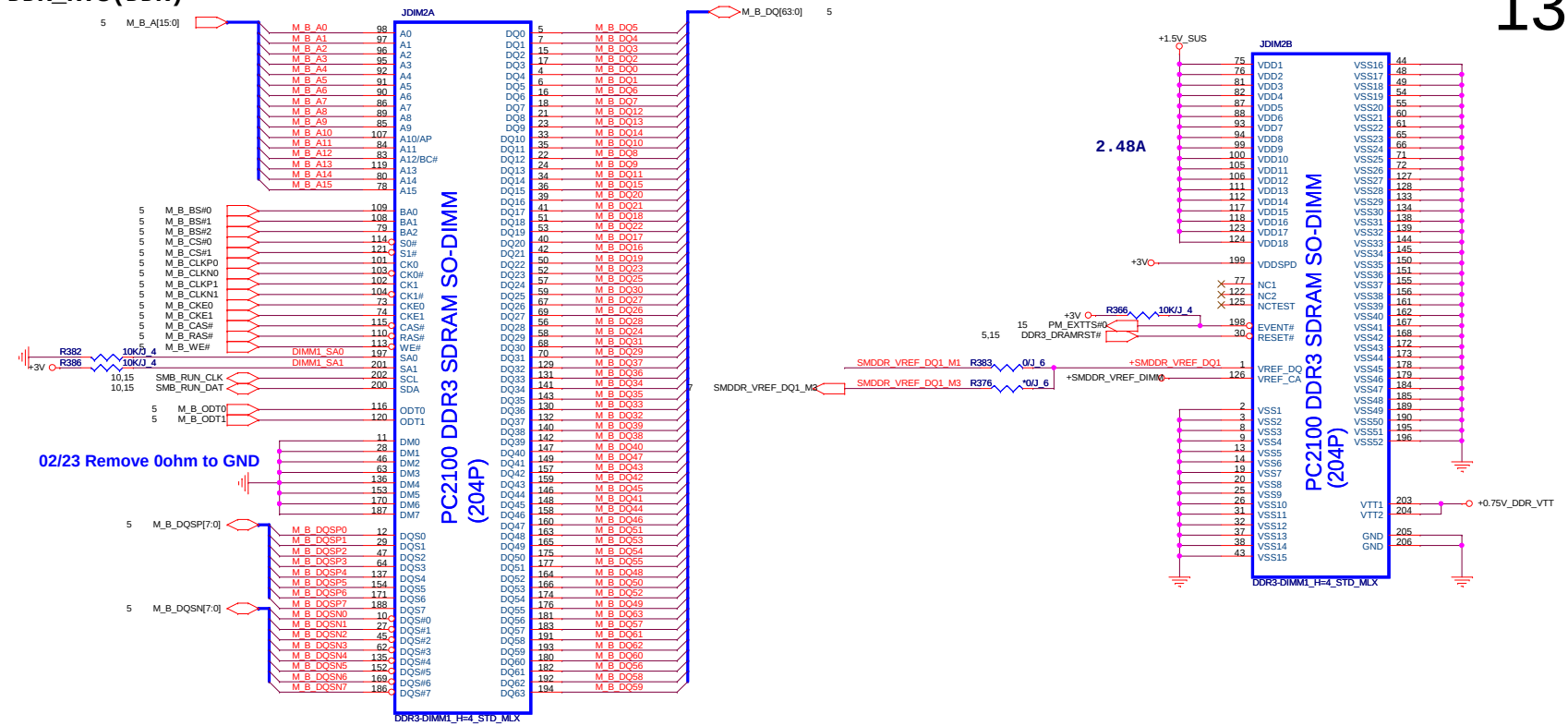
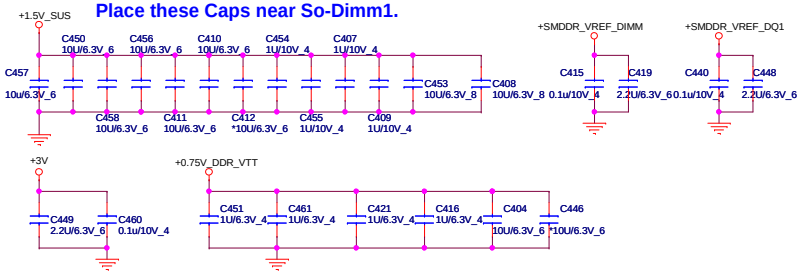
DDR_RVS(DDR)



Place these Caps near So-Dimm1.

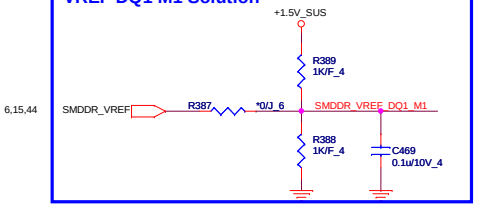


VREF DQ1 M2 Solution

6/22 Remove M2 Solution by MOW26

A16

VREF DQ1 M1 Solution



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRIII SO-DIMM-0	1A

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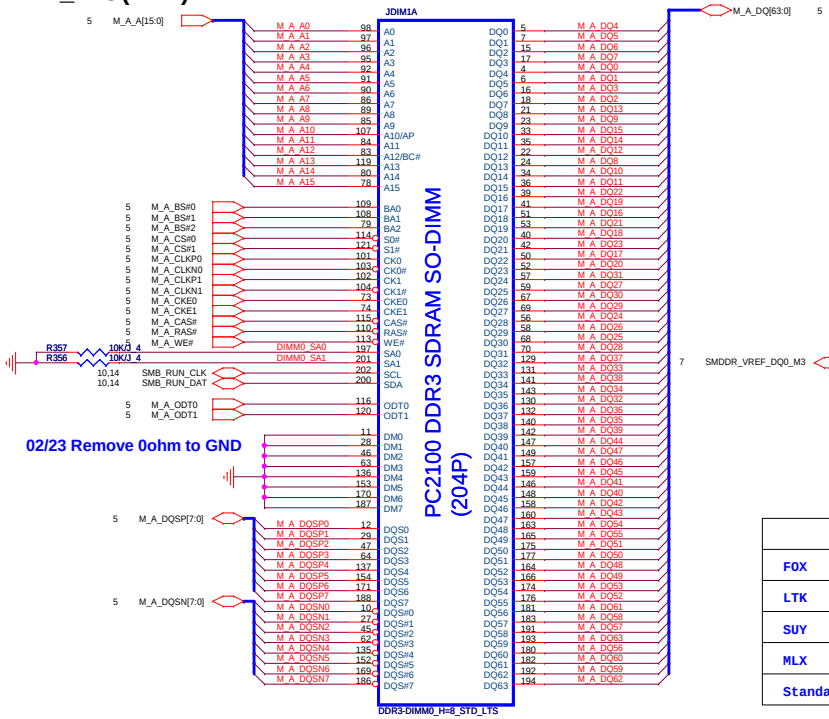
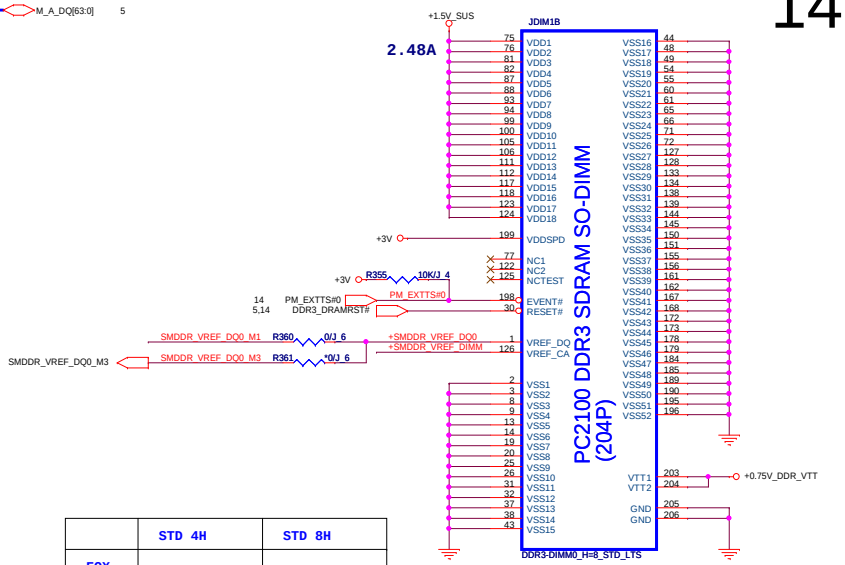
DDR_RVS(DDR)



02/23 Remove 0ohm to GND



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

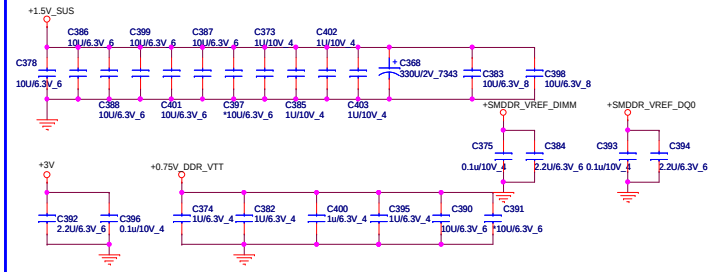
Standard 4H type:DDR-C-2013289-204p

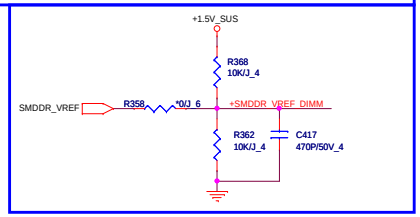
VREF DQ0 M2 Solution

6/22 Remove M2 Solution by MOW26

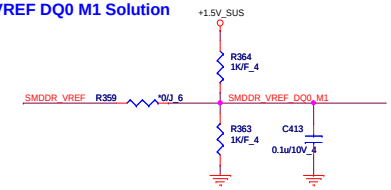
A16

Place these Caps near So-Dimm0.





VREF DQ0 M1 Solution



POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=0.9~1.2V

2.5GT/s bit rate

U26A

PCI EXPRESS INTERFACE

4	PEG_TXP15	PEG_TXP15	AF30	PCIE_RX0P	PCIE_TX0P	AH30	C_PEG_RXP15	C213	0.1U/10V_4	PEG_RXP15	4
4	PEG_TXN15	PEG_TXN15	AE31	PCIE_RX0N	PCIE_TX0N	AG31	C_PEG_RXN15	C203	0.1U/10V_4	PEG_RXN15	4
4	PEG_TXP14	PEG_TXP14	AE29	PCIE_RX1P	PCIE_TX1P	AG29	C_PEG_RXP14	C200	0.1U/10V_4	PEG_RXP14	4
4	PEG_TXN14	PEG_TXN14	AD28	PCIE_RX1N	PCIE_TX1N	AF28	C_PEG_RXN14	C198	0.1U/10V_4	PEG_RXN14	4
4	PEG_TXP13	PEG_TXP13	AD30	PCIE_RX2P	PCIE_TX2P	AF27	C_PEG_RXP13	C226	0.1U/10V_4	PEG_RXP13	4
4	PEG_TXN13	PEG_TXN13	AC31	PCIE_RX2N	PCIE_TX2N	AF26	C_PEG_RXN13	C225	0.1U/10V_4	PEG_RXN13	4
4	PEG_TXP12	PEG_TXP12	AC29	PCIE_RX3P	PCIE_TX3P	AD27	C_PEG_RXP12	C190	0.1U/10V_4	PEG_RXP12	4
4	PEG_TXN12	PEG_TXN12	AB28	PCIE_RX3N	PCIE_TX3N	AD26	C_PEG_RXN12	C196	0.1U/10V_4	PEG_RXN12	4
4	PEG_TXP11	PEG_TXP11	AB30	PCIE_RX4P	PCIE_TX4P	AC25	C_PEG_RXP11	C189	0.1U/10V_4	PEG_RXP11	4
4	PEG_TXN11	PEG_TXN11	AA31	PCIE_RX4N	PCIE_TX4N	AC24	C_PEG_RXN11	C183	0.1U/10V_4	PEG_RXN11	4
4	PEG_TXP10	PEG_TXP10	AA29	PCIE_RX5P	PCIE_TX5P	Y23	C_PEG_RXP10	C164	0.1U/10V_4	PEG_RXP10	4
4	PEG_TXN10	PEG_TXN10	Y28	PCIE_RX5N	PCIE_TX5N	Y24	C_PEG_RXN10	C176	0.1U/10V_4	PEG_RXN10	4
4	PEG_TXP9	PEG_TXP9	Y30	PCIE_RX6P	PCIE_TX6P	AB27	C_PEG_RXP9	C179	0.1U/10V_4	PEG_RXP9	4
4	PEG_TXN9	PEG_TXN9	W31	PCIE_RX6N	PCIE_TX6N	AB26	C_PEG_RXN9	C181	0.1U/10V_4	PEG_RXN9	4
4	PEG_TXP8	PEG_TXP8	W29	PCIE_RX7P	PCIE_TX7P	W27	C_PEG_RXP8	C158	0.1U/10V_4	PEG_RXP8	4
4	PEG_TXN8	PEG_TXN8	V28	PCIE_RX7N	PCIE_TX7N	W26	C_PEG_RXN8	C163	0.1U/10V_4	PEG_RXN8	4
4	PEG_TXP7	PEG_TXP7	V30	PCIE_RX8P	PCIE_TX8P	V25	C_PEG_RXP7	C157	0.1U/10V_4	PEG_RXP7	4
4	PEG_TXN7	PEG_TXN7	U31	PCIE_RX8N	PCIE_TX8N	V24	C_PEG_RXN7	C148	0.1U/10V_4	PEG_RXN7	4
4	PEG_TXP6	PEG_TXP6	U29	PCIE_RX9P	PCIE_TX9P	V27	C_PEG_RXP6	C143	0.1U/10V_4	PEG_RXP6	4
4	PEG_TXN6	PEG_TXN6	T28	PCIE_RX9N	PCIE_TX9N	U26	C_PEG_RXN6	C146	0.1U/10V_4	PEG_RXN6	4
4	PEG_TXP5	PEG_TXP5	T30	PCIE_RX10P	PCIE_TX10P	U25	C_PEG_RXP5	C140	0.1U/10V_4	PEG_RXP5	4
4	PEG_TXN5	PEG_TXN5	R31	PCIE_RX10N	PCIE_TX10N	U24	C_PEG_RXN5	C133	0.1U/10V_4	PEG_RXN5	4
4	PEG_TXP4	PEG_TXP4	R29	PCIE_RX11P	PCIE_TX11P	T25	C_PEG_RXP4	C132	0.1U/10V_4	PEG_RXP4	4
4	PEG_TXN4	PEG_TXN4	P28	PCIE_RX11N	PCIE_TX11N	T27	C_PEG_RXN4	C122	0.1U/10V_4	PEG_RXN4	4
4	PEG_TXP3	PEG_TXP3	P30	PCIE_RX12P	PCIE_TX12P	T29	C_PEG_RXP3	C110	0.1U/10V_4	PEG_RXP3	4
4	PEG_TXN3	PEG_TXN3	N31	PCIE_RX12N	PCIE_TX12N	T28	C_PEG_RXN3	C120	0.1U/10V_4	PEG_RXN3	4
4	PEG_TXP2	PEG_TXP2	N29	PCIE_RX13P	PCIE_TX13P	P27	C_PEG_RXP2	C106	0.1U/10V_4	PEG_RXP2	4
4	PEG_TXN2	PEG_TXN2	M28	PCIE_RX13N	PCIE_TX13N	P26	C_PEG_RXN2	C100	0.1U/10V_4	PEG_RXN2	4
4	PEG_TXP1	PEG_TXP1	M30	PCIE_RX14P	PCIE_TX14P	P24	C_PEG_RXP1	C96	0.1U/10V_4	PEG_RXP1	4
4	PEG_TXN1	PEG_TXN1	L31	PCIE_RX14N	PCIE_TX14N	P23	C_PEG_RXN1	C90	0.1U/10V_4	PEG_RXN1	4
4	PEG_TXP0	PEG_TXP0	L29	PCIE_RX15P	PCIE_TX15P	M27	C_PEG_RXP0	C83	0.1U/10V_4	PEG_RXP0	4
4	PEG_TXN0	PEG_TXN0	K30	PCIE_RX15N	PCIE_TX15N	N26	C_PEG_RXN0	C78	0.1U/10V_4	PEG_RXN0	4

CLOCK

10	CLK_PCIE_VGAP	AK30	PCIE_REFCLKP	
10	CLK_PCIE_VGAN	AK32	PCIE_REFCLKN	

M93-S3--NC
PARK-S3--install
10K/F_4 R120 N10 NC_PWRGOOD

25,29,31,38 PLTRST# AL27 PERSTB

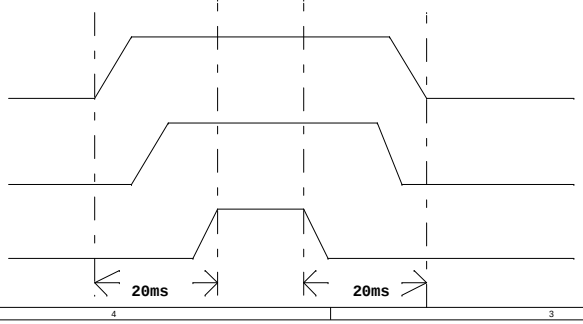
CALIBRATION

PCIE_CALRP Y22 M72_PCIE_CALRP R135 1.27K/F_4
PCIE_CALRN AA22 M72_PCIE_CALRN R220 2K/F_4 +1.1V_GPU

PARK

100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

VGA Core BPP
VGA Core VDDC
+1.8V PCIE_VDDR
+1.8V PCIE_PVDD
+1.8V VDDR1
+3V_VGA VDDR3



U26G

DP E/F POWER

+1.8V_DPE_VDD18	AG15 AG16	DPE_VDD18#1 DPE_VDD18#2
+1.1V_DPE_VDD10	AG20 AG21	DPE_VDD10#1 DPE_VDD10#2
	AG14 AH14 AM14 AM16 AM18	DPE_VSSR#1 DPE_VSSR#2 DPE_VSSR#3 DPE_VSSR#4 DPE_VSSR#5
+1.8V_DPE_VDD18	AF16 AG17	DPF_VDD18#1 DPF_VDD18#2
+1.1V_DPE_VDD10	AF22 AG22	DPF_VDD10#1 DPF_VDD10#2
	AF23 AG23 AM20 AM22 AM24	DPF_VSSR#1 DPF_VSSR#2 DPF_VSSR#3 DPF_VSSR#4 DPF_VSSR#5
R187 150/F_4 DPEF_CALR	AF17	DPEF_CALR
+1.8V_DPE_PVDD	AG18 AF19	DPE_PVDD DPE_PVSS
+1.8V_DPF_PVDD	AG19 AF20	NC_DPF_PVDD NC_DPF_PVSS

M93-S3--NC
PARK-S3--install

DP PLL POWER

DP A/B POWER

	AE11 AF11	NC_DPA_VDD18#1 NC_DPA_VDD18#2
+1.1V_DPB_VDD10	AF6 AF7	DPA_VDD10#1 DPA_VDD10#2
	AE1 AE3 AG1 AG6 AH5	DPA_VSSR#1 DPA_VSSR#2 DPA_VSSR#3 DPA_VSSR#4 DPA_VSSR#5
	AE13 AF13	NC_DPB_VDD18#1 NC_DPB_VDD18#2
	AF8 AF9	DPB_VDD10#1 DPB_VDD10#2
	AF10 AG9 AH8 AM6 AM8	DPB_VSSR#1 DPB_VSSR#2 DPB_VSSR#3 DPB_VSSR#4 DPB_VSSR#5
DPAB_CALR R571 150/F_4	AE10	DPAB_CALR
	AG8 AG7	DPA_PVDD DPA_PVSS
	AG10 AG11	DPB_PVDD DPB_PVSS

PARK

+1.8V_DPA_VDD18 +1.8V_DPA_PVDD +1.8V_DPB_VDD10 +1.8V_DPE_VDD18 +1.8V_DPE_PVDD +1.8V_DPF_PVDD +1.1V_DPE_VDD10

+1.1V_DPB_VDD10 L14 BLM18PG181SN1D(180,1.5A)_6 +1.1V_GPU
1.1V(S100,D200mA)
C199 0.1U/10V_4 C211 10U/6.3V_6S C201 1U/10V_4

(Park-S3:110mA@1.0V)
(M9X-S2/S3:200mA@1.1V)
+1.1V_DPE_VDD10 +1.1V_DPE_VDD10 L45 BLM18PG181SN1D(180,1.5A)_6 +1.1V_GPU
C236 0.1U/10V_4 C209 1U/10V_4 C248 10U/6.3V_6S

+1.8V_DPA_VDD18 +1.8V_DPA_VDD18 L15 BLM18PG181SN1D(180,1.5A)_6 +1.8V_GPU
1.8V(130mA)
C194 0.1U/10V_4 C218 1U/10V_4 C228 10U/6.3V_6S
M93-S3--NC
PARK-S3--install

1.8V -(440mA)
+1.8V_DPE_VDD18 L42 BLM18PG181SN1D(180,1.5A)_6 +1.8V_GPU
C197 0.1U/10V_4 C595 1U/10V_4 C609 10U/6.3V_6S

+1.8V_DPA_PVDD +1.8V_DPA_PVDD L13 BLM18PG181SN1D(180,1.5A)_6 +1.8V_GPU
1.8V(20mA)
C212 0.1U/10V_4 C210 1U/10V_4 C217 10U/6.3V_6S

+1.8V_DPF_PVDD +1.8V_DPF_PVDD L18 BLM18PG181SN1D(180,1.5A)_6 +1.8V_GPU
1.8V(20mA)
C207 0.1U/10V_4 C234 1U/10V_4 C249 10U/6.3V_6S
M93-S3--NC
PARK-S3--install

+1.8V_DPE_PVDD +1.8V_DPE_PVDD L19 BLM18PG181SN1D(180,1.5A)_6 +1.8V_GPU
1.8V(20mA)
C208 0.1U/10V_4 C227 1U/10V_4 C250 10U/6.3V_6S

Quanta Computer Inc.
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Size	Document Number	Rev
	Robson_PCIE_Interface	1A

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MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung	128MB*16-800MHZ	K4W2G1646C-HC12
0001	Hynix	128MB*16 -800MHZ	H5TQ2G63BFR-12C

KL8A

KL8A

Table : VDDC_OPT VID

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	VDDC
1	1	1.15V
1	0	1.00V
0	1	1.1V
0	0	0.9V

10/8 :Reserve GFX_CORE_CNTRL0/GFX_CORE_CNTRL1 VID pull down Res for AMD FAE suggest

M93 MV Added
AMD Suggestion

GPIO22(ROMCS#)
PD without external VBIOS ROM

0916: AMD modify

R576 add for Robson co-layout
PARK, M93----->Install
Robson-------->Uninstall

1.8V@75mA

1.8V@125mA 1.1V(300mA DPLL_VDDC)

Reserved

For Int Clk 27Mhz

CL=20PF

Memory ID

For M93-S3: Use 150 Ohms Pull Down
For M92-S2: Use 0R to VDDR4
For Park-S3: NC

EC-B-14

FAE ask R/G/B2B connect to GND

EC-B-06-07

EC-B-37

PARK-- Install
M93-- NC

	Robson	Seymour
R229	ASM	No ASM
R162	ASM	No ASM
R572	ASM	No ASM
R206	ASM	No ASM
R9221	ASM	No ASM
R9223	ASM	No ASM
R9224	ASM	No ASM

Thermal Sensor

I2C ADDRESS: 98H

W/S 10 / 10

Quanta Computer Inc.
PROJECT : KL8A

Size	Document Number	Rev
	Robson_MAIN	1A

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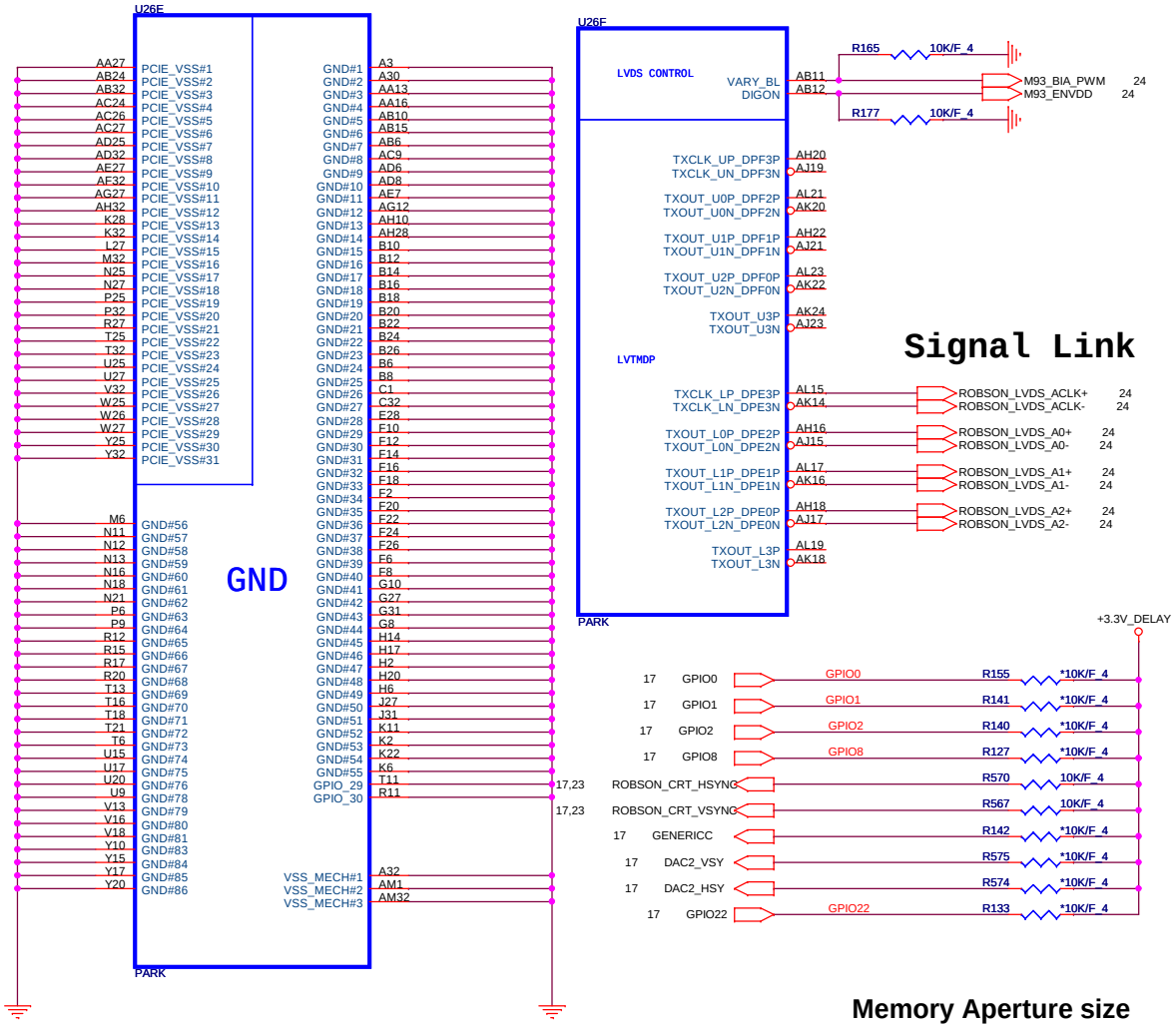


Signal Link

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN ROMIDCFG(2:0) VIP_DEVICE_STRAP_ENA	GPIO_22_ROMCSB GPIO[13:11] V2SYNC	ENABLE EXTERNAL BIOS ROM SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT IGNORE VIP DEVICE STRAPS	0 0 0 1 0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

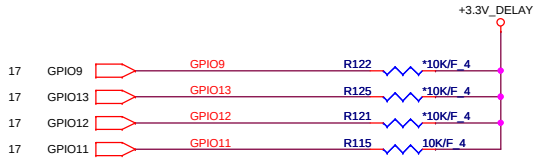
H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1



Due to memory management constraints, the aperture size should be the same size as the frame buffer for 64 MB, 128 MB
and 256 MB. For frame buffers larger than 256 MB (e.g. 512 MB, 1 GB) the aperture size should be 256 MB.

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Quanta Computer Inc.
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	Robson_GND / LVDS /Straps	1A
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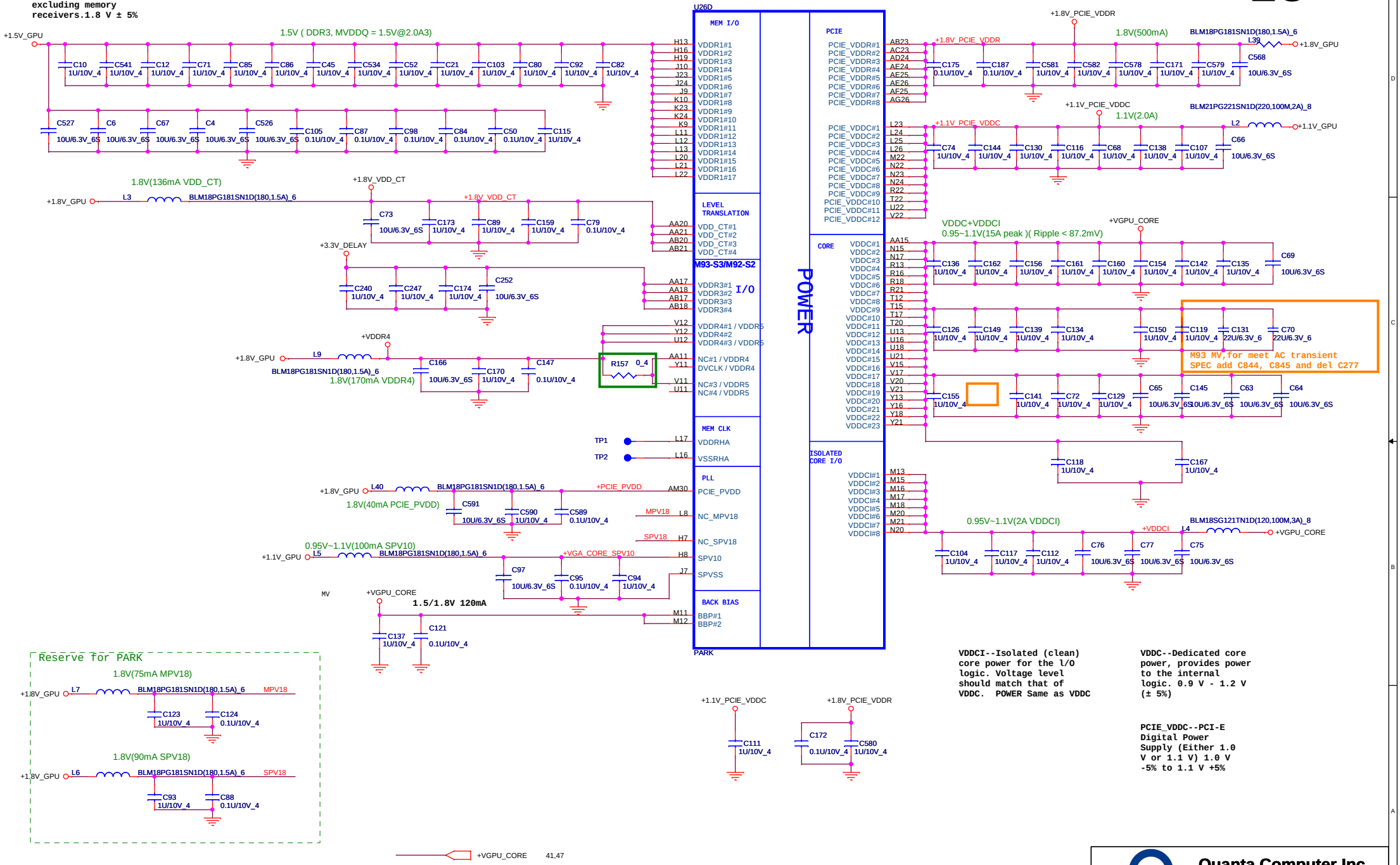
VDD_CT -- Level translation between core and I/O, excluding memory receivers.1.8 V ± 5%

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

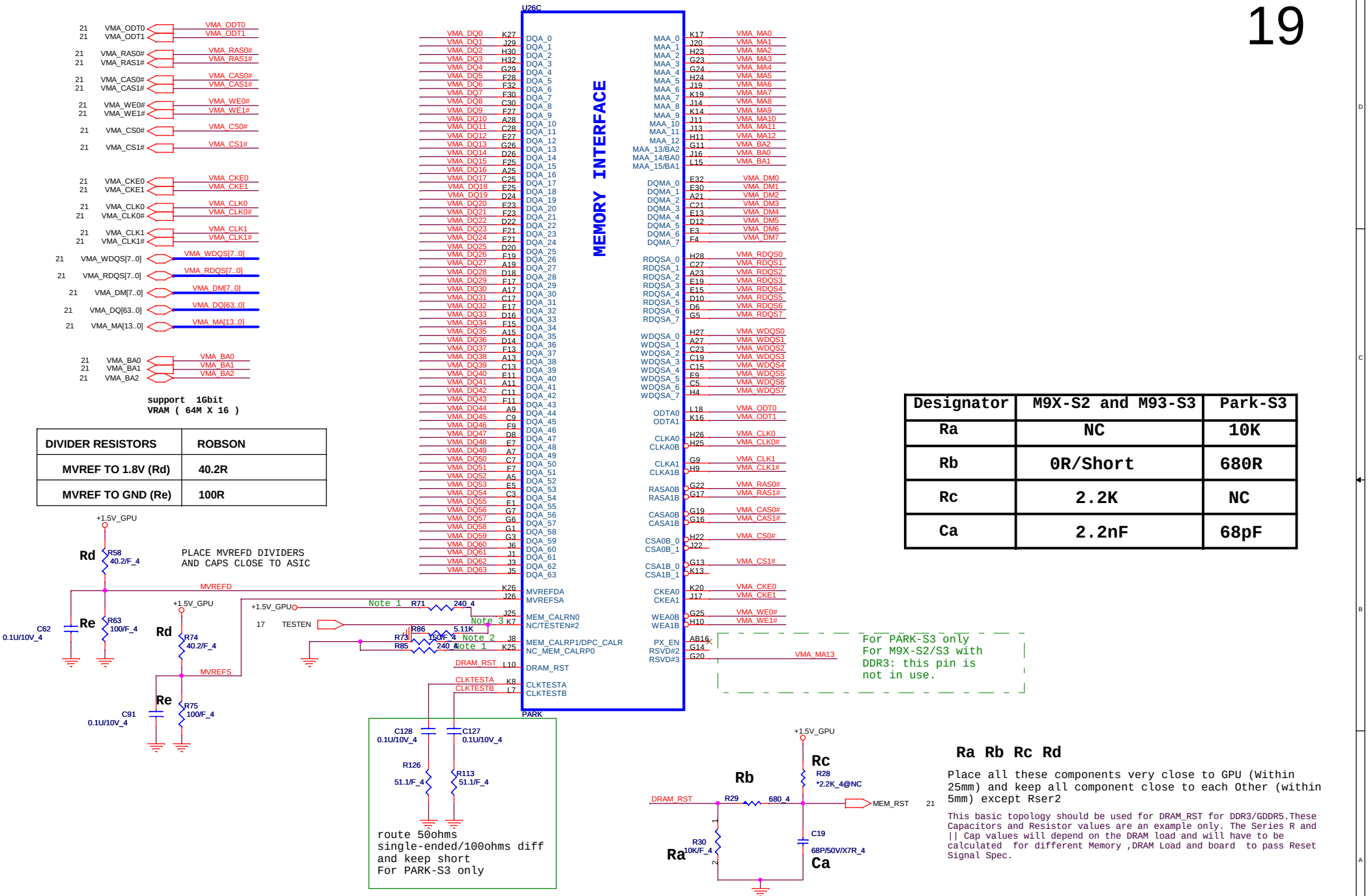
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

Quanta Computer Inc.

PROJECT : KL8A

Size	Document Number	Rev
	Robson_Power_and_NC	1A
Date: Monday, January 03, 2011	Sheet 19 of 53	



Designator	M9X-S2 and M93-S3	Park-S3
Ra	NC	10K
Rb	0R/Short	680R
Rc	2.2K	NC
Ca	2.2nF	68pF

Ra Rb Rc Rd

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

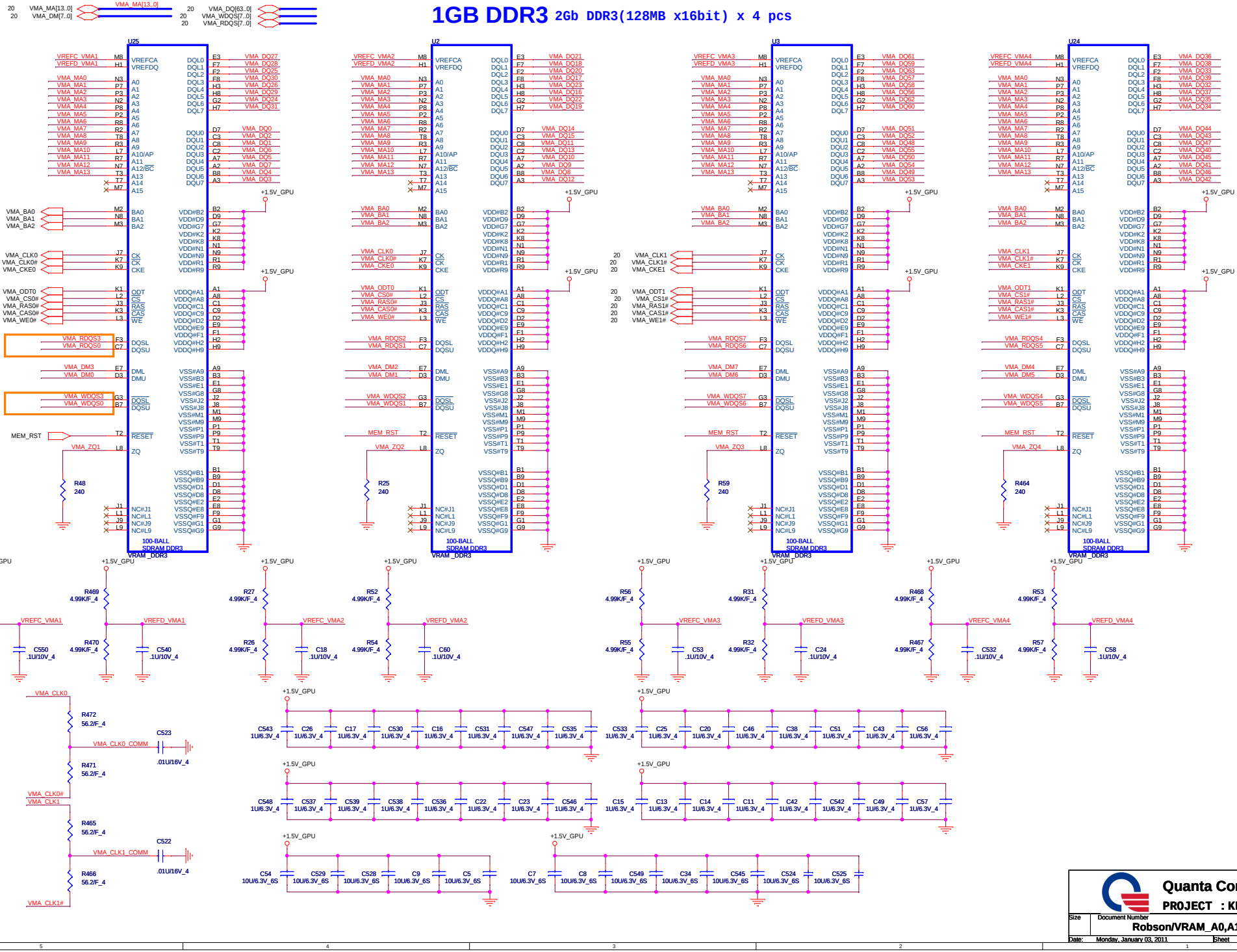
This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24
R575 for Robson only

Quanta Computer Inc.
PROJECT : KL8A

Size	Document Number	Rev
	Robson_MEM_Interface	1A
Date: Monday, January 03, 2011	Sheet 20 of 53	

1GB DDR3 2Gb DDR3(128MB x16bit) x 4 pcs



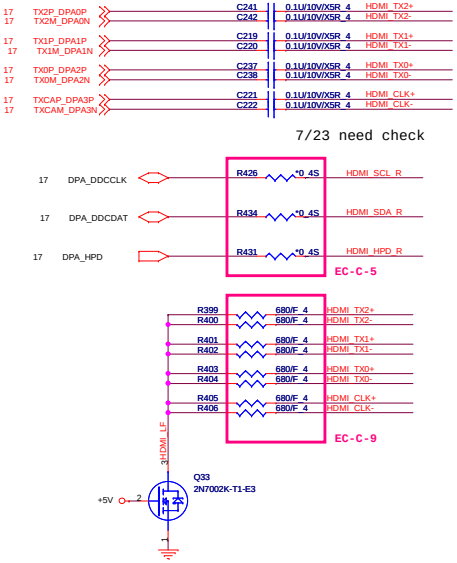
Quanta Computer Inc.

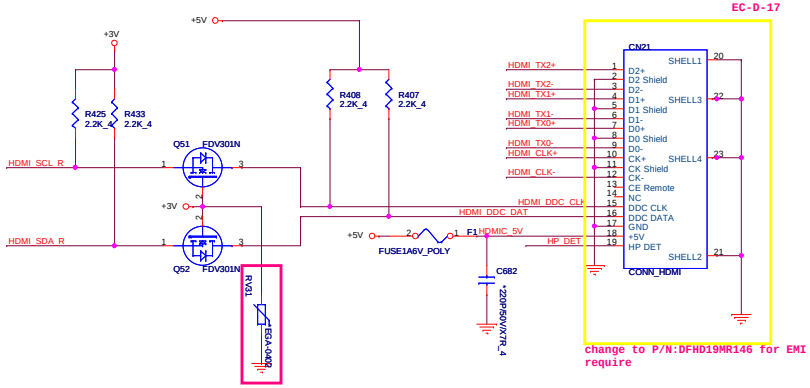
PROJECT : KL8A

Size	Document Number	Rev
	Robson/VRAM_A0,A1	1A

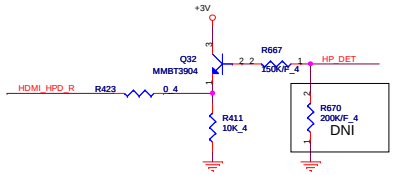
Date: Monday, January 03, 2011 Sheet 21 of 53

DIS HDMI

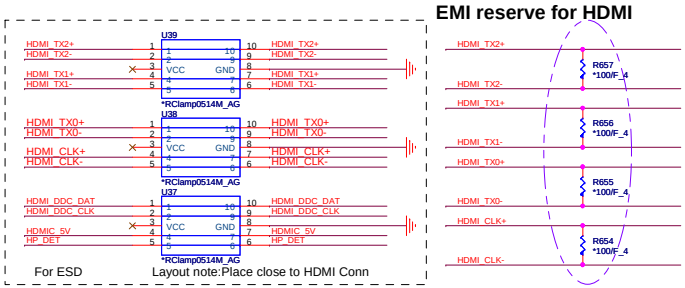




HDMI Hot-PLUG to EC and GPU



Copy from GC9A



9,12,23,26,28,34,35,36,37,38,40,41,43,50 +5V
4,8,9,10,11,12,14,15,17,23,24,26,27,28,29,30,31,33,36,37,38,40,41,43,47,48,49,50 +3V

Quanta Computer Inc.
PROJECT : KL8A

Size	Document Number	Rev
	Madison_LVDS/HDMI/CRT switchable	1A
Date: Monday, January 03, 2011	Sheet 22 of 53	

9,12,22,26,28,34,35,36,37,38,40,41,43,50 +5V
4,8,9,10,11,12,14,15,17,22,24,26,27,28,29,30,31,33,36,37,38,40,41,43,47,48,49,50 +3V

ESD PROTECTION

U46 *CM1293A-04SO
U47 *TVLST2304AD0
ESD

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

ROBSON_CRT_RED / ROBSON_CRT_GRN / ROBSON_CRT_BLU
L33 / L32 / L31 BK1608LL680
CRT_R1 / CRT_G1 / CRT_B1
R299 / R290 / R279 150/F_4
C331 / C318 / C309 / C308 / C317 / C330 5.6P/50V/COG_4
TP51

CRT_VCC
D24 RB500V-40
C674 0.1U/10V/X5R_4
F2 FUSE1A6V_POLY
C678 *VARISTOR_4
CRT_VCC_R

CN16 CRT_CONN

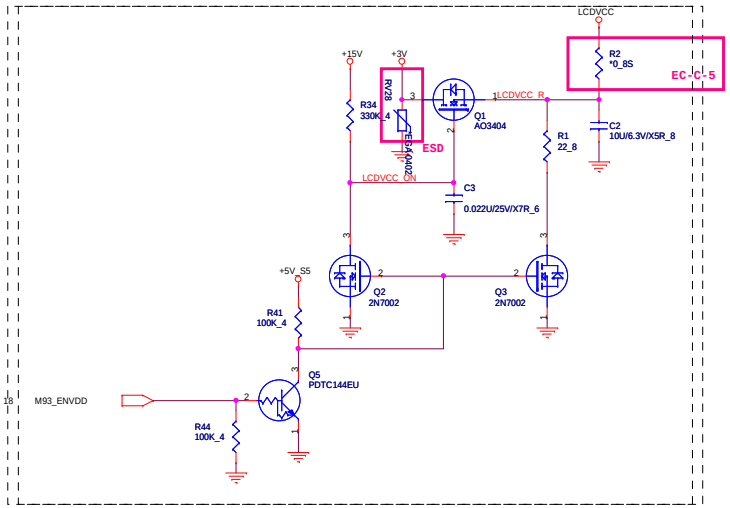
U12 / U13 AHCT1G125DCH
ROBSON_CRT_VSYNC / ROBSON_CRT_HSYNC
VGAVSYNC_R / VGAHSYNC_R
C282 0.1U/10V/X5R_4
R263 / R264 10_4
Place near U37,U38 < 200 mil
CRTVSYNC1 / CRTHSYNC1
C288 / C287 *10P/50V/COG_4
L29 / L30 HB-1T1608-121JT
CRTVSYNC / CRTHSYNC
C298 / C297 10P/50V/COG_4
Place near CN5002 connector < 200 mil

17,18 ROBSON_CRT_VSYNC → ROBSON_CRT_VSYNC
17,18 ROBSON_CRT_HSYNC → ROBSON_CRT_HSYNC
17 ROBSON_CRT_DDCCLK → ROBSON_CRT_DDCCLK
17 ROBSON_CRT_DDCDAT → ROBSON_CRT_DDCDAT
17 ROBSON_CRT_RED → ROBSON_CRT_RED
17 ROBSON_CRT_GRN → ROBSON_CRT_GRN_R
17 ROBSON_CRT_BLU → ROBSON_CRT_BLU_R

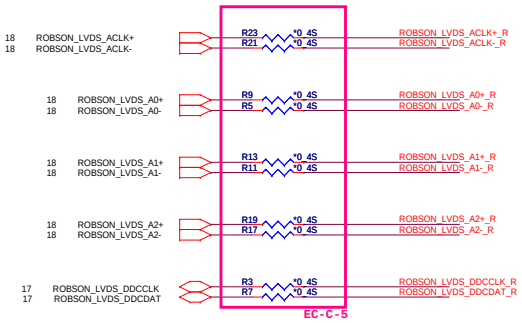
+3V
R615 / R605 2.2K_4
R612 4.7K_4
R607 4.7K_4
Q42 / Q44 2N7002K-T1-E3
DDCCLK / DDCDAT
C685 / C670 *10P/50V/COG_4
RV33 EGA0402

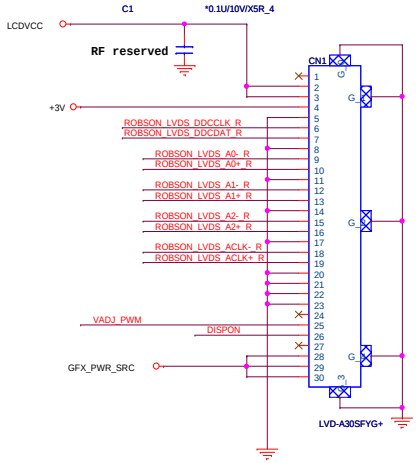
Quanta Computer Inc. PROJECT : KL8A			
Size	Document Number: CRT CONN		Rev: 1A
Date: Monday, January 03, 2011	Sheet 23 of 53		

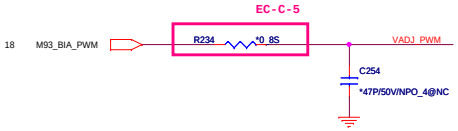
LCDVCC

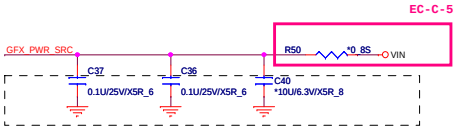


Layout note: Those resister place colse LVDS connector

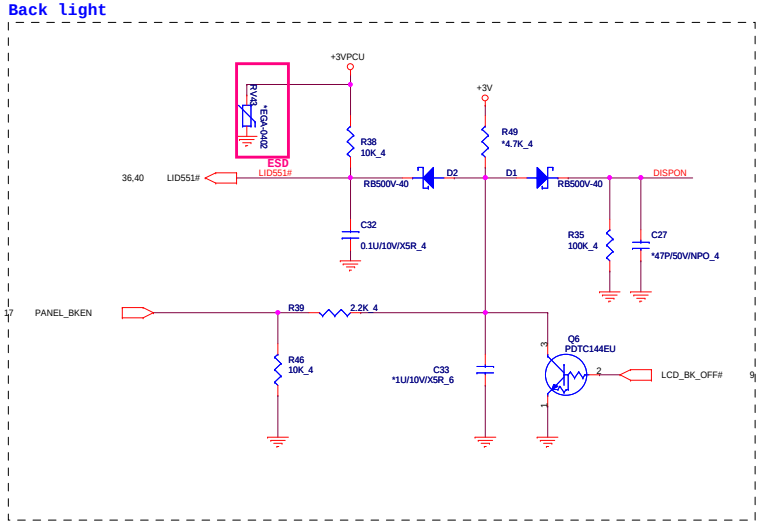








Back light



Quanta Computer Inc. PROJECT : KL8A			
Size	Document Number: LCD CONN		Rev: 1A
Date: Monday, January 03, 2011	Sheet 24 of 53		

LANVCC

+3VPCU
Q49 AO6402A
RV42 *EGA-0402 ESD
8 SLP_LAN# R662 *0_4
41 LAN_ON R659 *0_4_short
+3.3V_LAN_R R648 *0_8_short
+3.3V_LAN
C729 0.1U/10V/X5R_4

VDDIO Power Decoupling

+3.3V_LAN
C724 10U/10V/X5R_8
C726 0.1U/10V/X5R_4
C738 10U/10V/X5R_8
EC-C-7 C728 *0.1U/10V/X5R_4
CAP : 10U*2 , 0.1U*1 - 07/20
Rev1.2 - Intel 431786

U34 82579

10 PCIE_CLKREQ_LAN# 4,10,16,29,31,38 PLTRST#
10 CLK_PCIE_LAN
10 CLK_PCIE_LANN
10 PCIE_RXP2_LAN
10 PCIE_RXN2_LAN
10 PCIE_TXP2_LAN
10 PCIE_TXN2_LAN
C732 0.1U/10V/X5R_4 LAN_PCIETXDP
C733 0.1U/10V/X5R_4 LAN_PCIETXDN
CLK_REQ_N
PE_RST_N
PE_CLKP
PE_CLKN
PETp
PETn
PERp
PERn
PCIE

MDI_PLUS0 MDI_MINUS0 TRD0+ TRD0-
MDI_PLUS1 MDI_MINUS1 TRD1+ TRD1-
MDI_PLUS2 MDI_MINUS2 TRD2+ TRD2-
MDI_PLUS3 MDI_MINUS3 TRD3+ TRD3-
MDI

SMB_CLK_ME0_R
SMB_DAT_ME0_R
SMB_CLK
SMB_DATA
SMBUS

VCT
RSVD_VCC3P3_1 R649 4.7K_4
RSVD_VCC3P3_2 R646 4.7K_4 +3.3V_LAN
VDD3P3_IN
VDD3P3_OUT +V3.3M_LAN_OUT
VDD3P3_15 VDD3P3_19 VDD3P3_29 C721 1U/10V/X5R_4
VDD1P0_47 VDD1P0_46 VDD1P0_37
+1.0V_LOM
VDD1P0_43
VDD1P0_11
VDD1P0_40 VDD1P0_22 VDD1P0_16 VDD1P0_8
C715 0.01U/16V/X7R_4
C713 10U/10V/X5R_8
C714 *10U/10V/X5R_8
CTRL_1P0 L37 4.7uH/510mA_12
VSS_EPAD
Close to CTRL_1P0 (PIN7)

Added CAP,Total = 20uF - 07/23
Rev1.2 - Intel 431786

LAN_DISABLE# is active low.
11 LAN_DISABLE# R644 0_4
+3.3V_LAN R643 *10K_4
R641 *10K_4
RV45 *EGA-0402
LAN_DISABLE_N

ACTLED#
LINKLED
LED0 LED1 LED2
LED

+3.3V_LAN R640 10K_4 R642 10K_4
JTAG_TDI JTAG_TDO JTAG_TMS JTAG_TCK
JTAG

LAN_XTALO
LAN_XTALI
XTAL_OUT XTAL_IN
TEST_EN
RBIAS
R636 1K_4 R631 3.01K/F_4

U32 / U31 CM1293A-04SO

U32: TRD0+ TRD1- TRD0- TRD1+
U31: TRD2+ TRD3- TRD2- TRD3+
IO1 IO4 GND REF IO2 IO3
+3.3V_LAN
ESD

LAN_XTALO_R R635 0_4 LAN_XTALO

Y7 25MHZ
LAN_XTALI
C720 33P/50V/NPO_4
C719 33P/50V/NPO_4

Reserved

Tramsformer

U29 NS892405
TD4- TD4+ TCT4 TD3- TD3+ TCT3 TD2- TD2+ TCT2 TD1- TD1+ TCT1
MX4- MX4+ MCT4 MX3- MX3+ MCT3 MX2- MX2+ MCT2 MX1- MX1+ MCT1
TRD0- TRD0+ TRD1- TRD1+ TRD2- TRD2+ TRD3- TRD3+
LAN_MX0- LAN_MX0+ LAN_MCT0 LAN_MX1- LAN_MX1+ LAN_MCT1 LAN_MX2- LAN_MX2+ LAN_MCT2 LAN_MX3- LAN_MX3+ LAN_MCT3
C376 C377 C381 C379 0.1U/10V/X5R_4
C380 1U/10V/X5R_6
Place near to Transformer
R308 R309 R310 R311 75/F_4
LANCT3
EC-C-7 (Place close to RJ45)
R307 1M_6
C702 1000P/3KV/NPO_18

RJ45 Connector

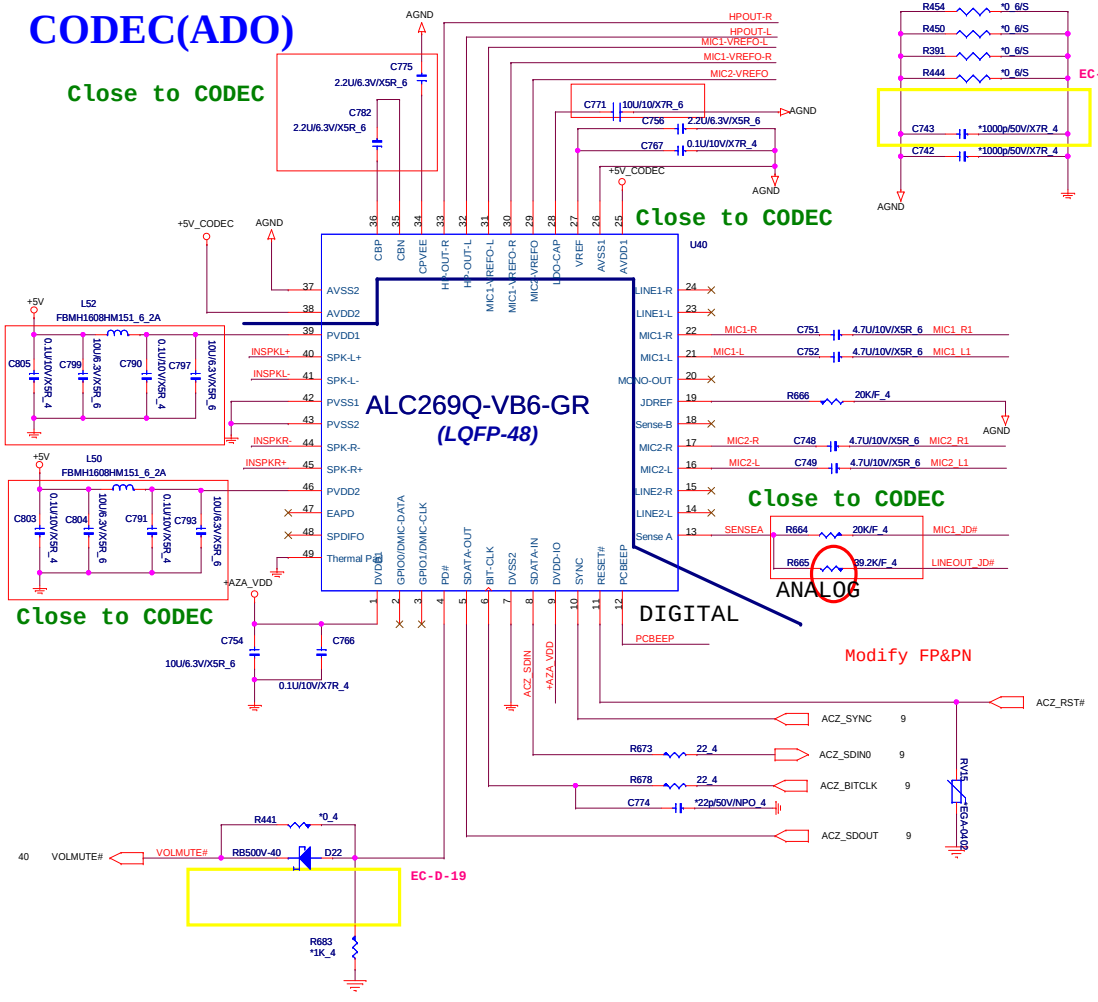
EMI:close RJ45
C710 *0.1U/10V/X5R_4@NC
CN18 100073FR012S176ZL
+3.3V_LAN R626 150/F_4 LAN_YLED
ACTLED#
C712 *0.1U/10V/X5R_4@NC
LAN_MX0+ LAN_MX0- LAN_MX1+ LAN_MX2+ LAN_MX2- LAN_MX1- LAN_MX3+ LAN_MX3-
+3.3V_LAN R624 150/F_4 LAN_GLED LINKLED
G3 G2 G1 G0 Lan_Gnd1 Lan_Gnd2
EMI:close RJ45
C700 *0.1U/10V/X5R_4@NC

SMBUS address 0XC8

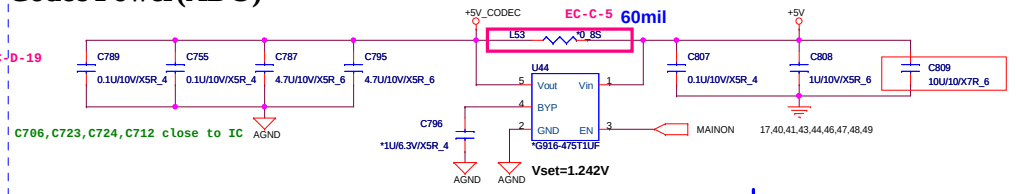
+3V_S5
RV34 *EGA-0402 ESD
+3.3V_LAN
R639 2.2K_4 R634 2.2K_4
10 SMB_DATA_ME0 Q48 2N7002 SMB_DAT_ME0_R
10 SMB_CLK_ME0 Q47 2N7002 SMB_CLK_ME0_R

Quanta Computer Inc.		
PROJECT : KL8A		
Size	Document Number: Giga LAN 82579	Rev 1A
Date: Monday, January 03, 2011	Sheet 25 of 53	

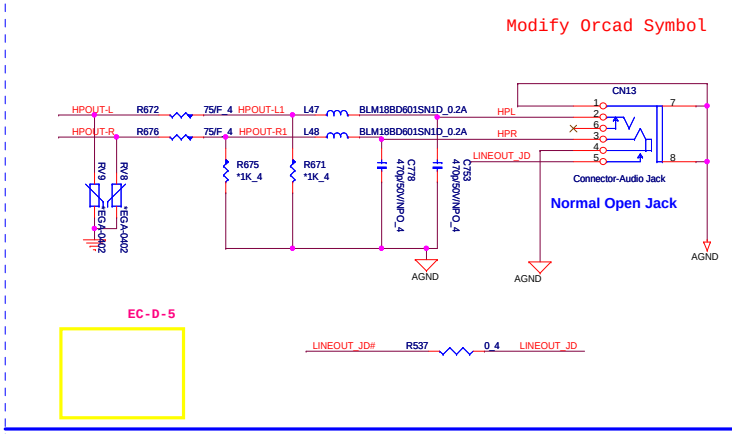
CODEC(ADO)



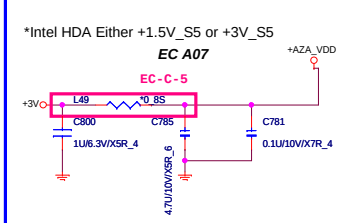
Codec Power(ADO)



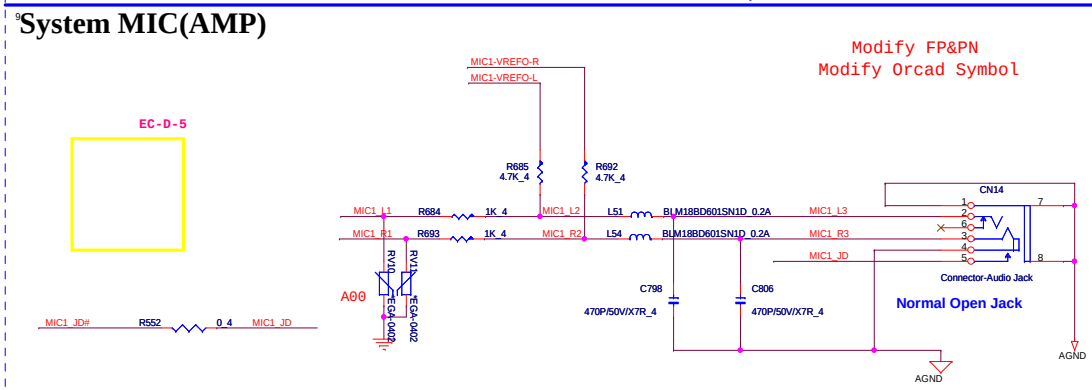
Earphone(AMP)



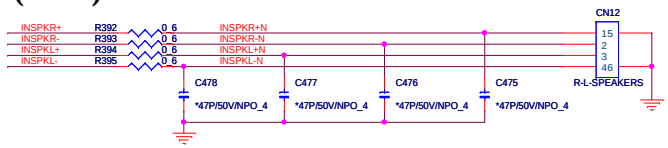
HDA Power(ADO)



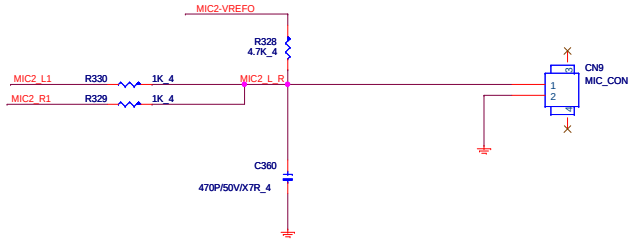
System MIC(AMP)



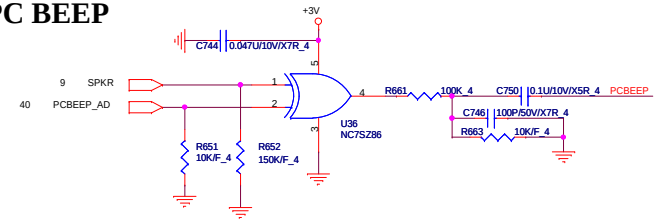
Speaker(AMP)



INTERNAL MIC

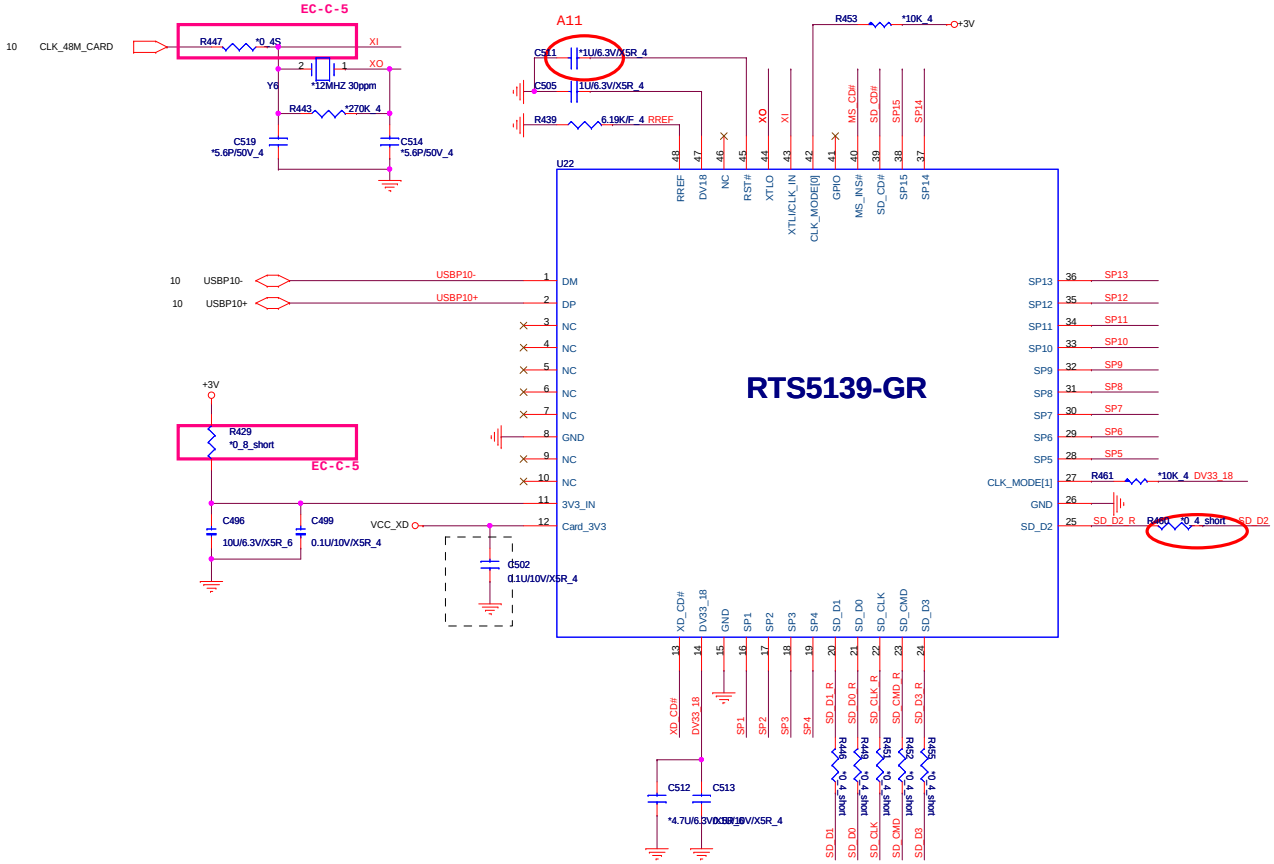


PC BEEP



Quanta Computer Inc.
PROJECT : KL8A

Size	Document Number	Rev
	ALC269/MIC/Line-Out	1A
Date: Tuesday, January 04, 2011	Sheet 26 of 53	

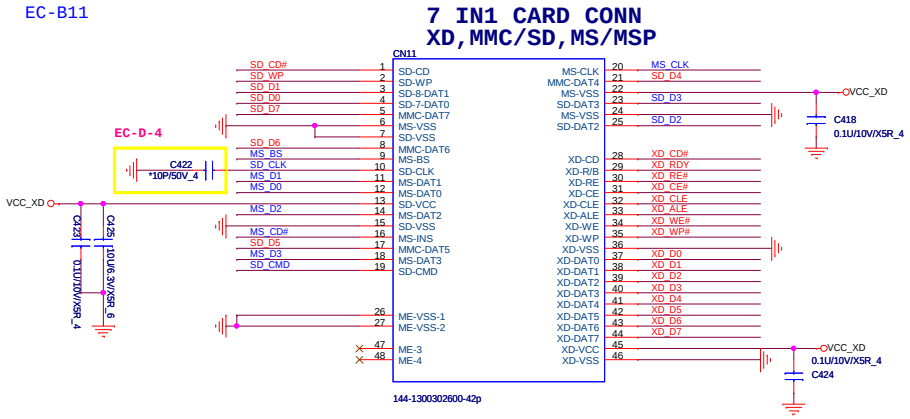


Clock Mode strap	R9287	R9307
48MHz	×	×
24MHz	×	○
12MHz	○	×
12MHz (Crystal)	○	○

Note:

For RTS5139

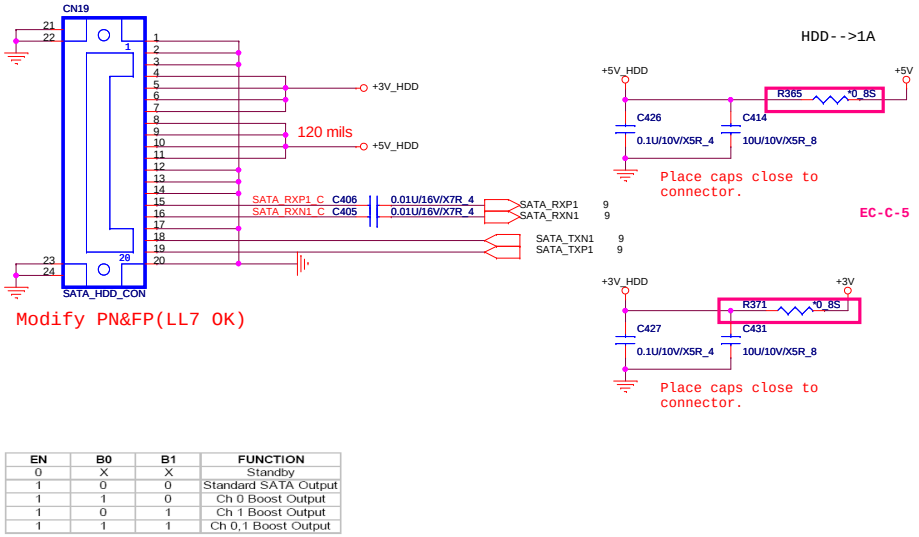
	SD/MMC	MS	XD
SP1	SD_D7		XD_RDY
SP2	SD_D6		XD_RE#
SP3	SD_D5		XD_CE#
SP4	SD_D4		XD_WE#
SP5		MS_BS	XD_CLE
SP6		MS_D5	XD_ALE
SP7		MS_D1	XD_WP#
SP8		MS_D4	XD_D0
SP9		MS_D0	XD_D1
SP10		MS_D2	XD_D2
SP11		MS_D6	XD_D3
SP12		MS_D3	XD_D4
SP13		MS_D7	XD_D5
SP14		MS_CLK	XD_D6
SP15	SD_WP		XD_D7



Quanta Computer Inc.
PROJECT : KL8A

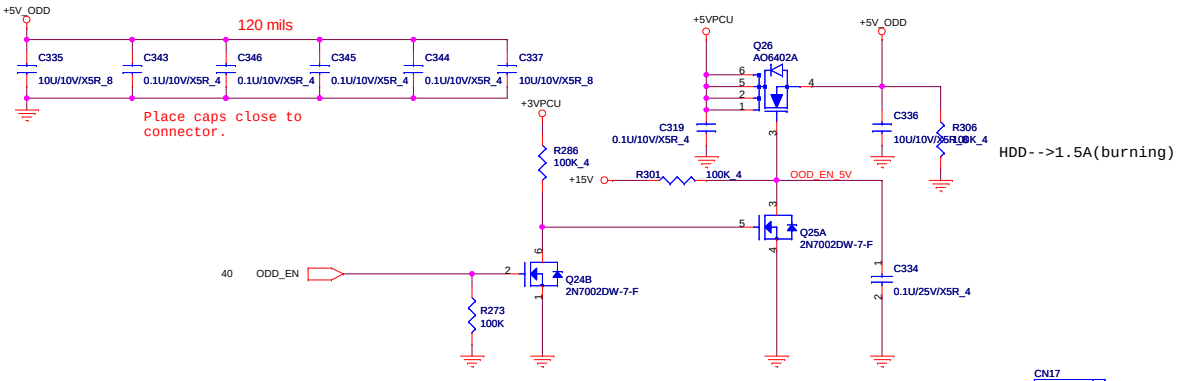
Size	Document Number	Rev
	Card Reader (RTS5139)	1A
Date: Monday, January 03, 2011	Sheet 27 of 53	

SATA HDD Connector.

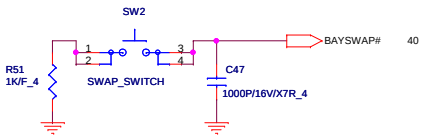


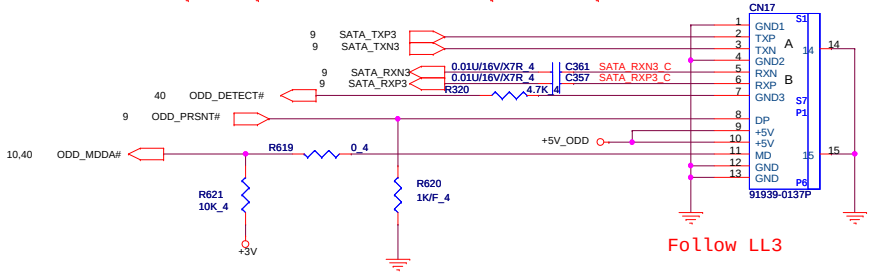
EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

SATA ODD Connector.



SATA ODD SW



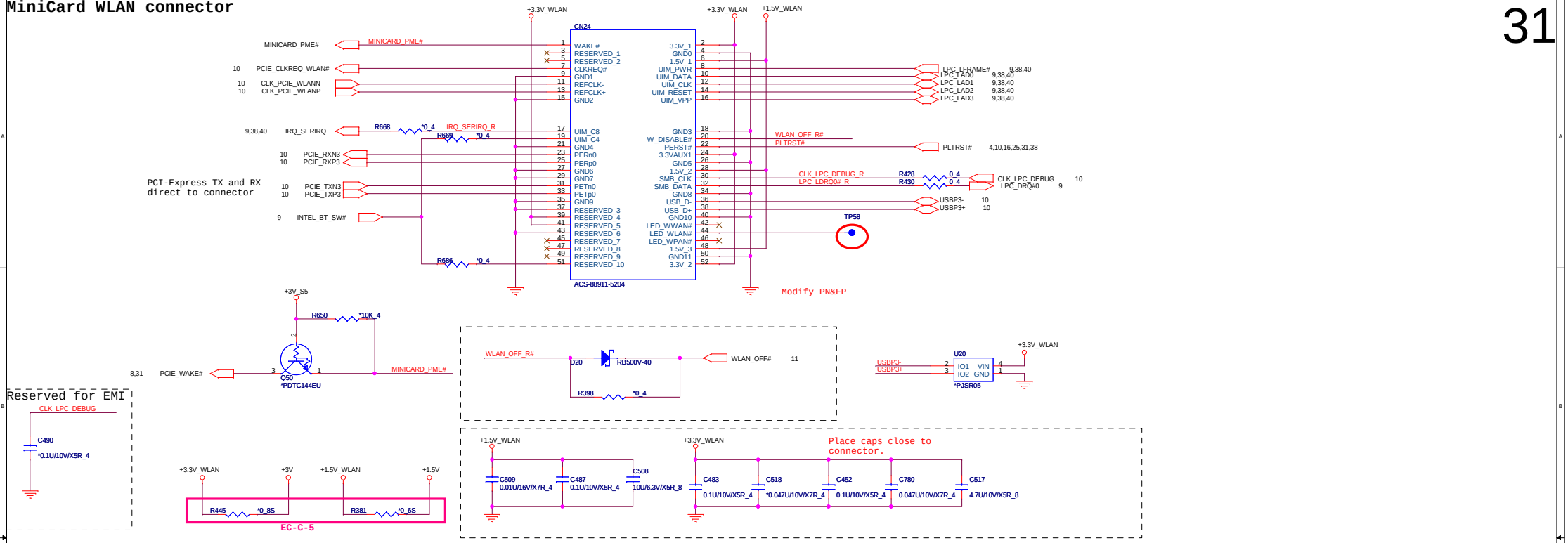


Quanta Computer Inc.
PROJECT : KL8A

Size	Document Number	Rev
	SATA HDD/ESATA/CD-ROM	1A

Date: Monday, January 03, 2011 Sheet 28 of 53

MiniCard WLAN connector



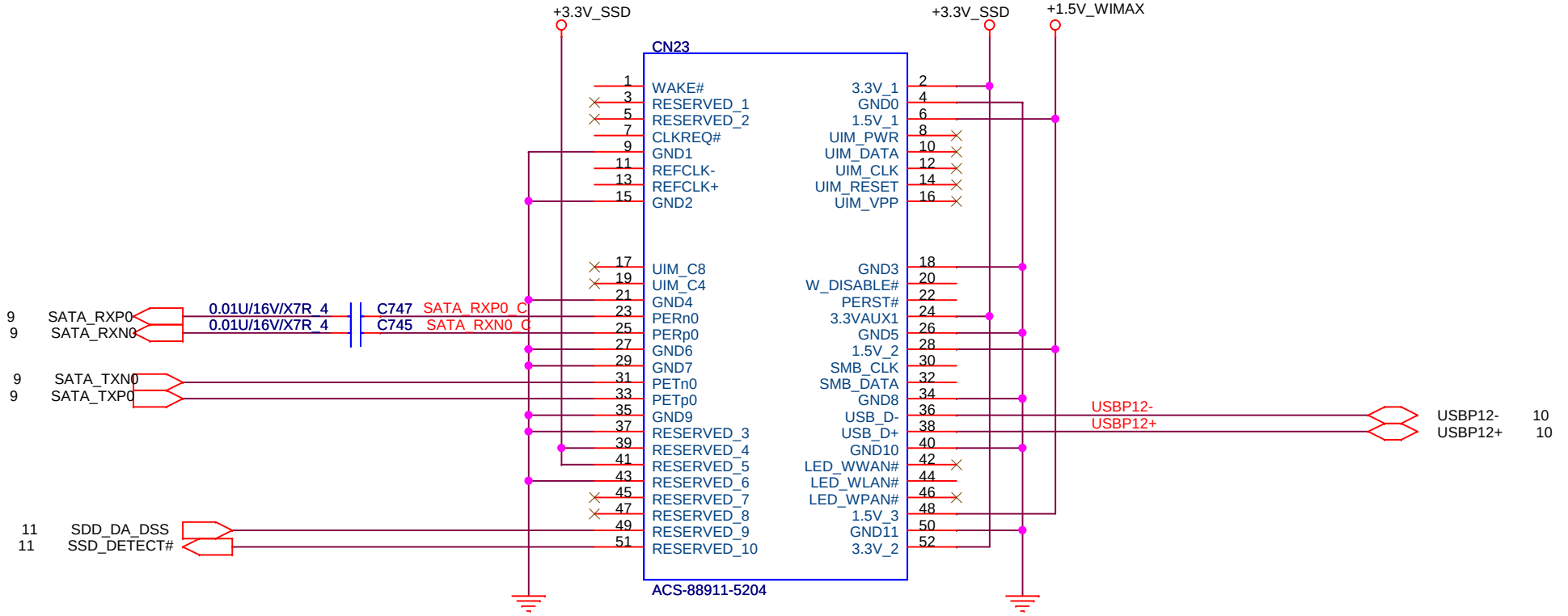
Quanta Computer Inc.	
PROJECT : KL8A	
Size	Document Number: MINI-Card (WLAN/WWAN) — Rev: 1A
Date: Monday, January 03, 2011	Sheet 29 of 53

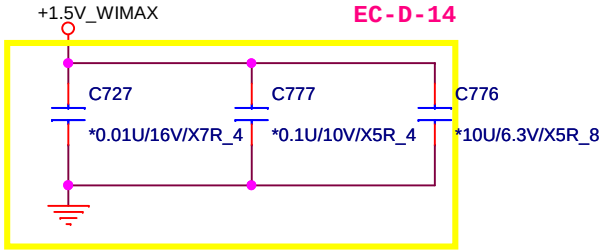
Mini PCI-E Card 3 SSD

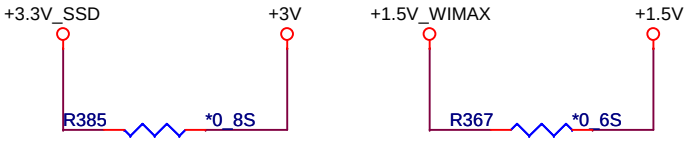
12,19,20,21,29,33,41,44
4,8,9,10,11,12,14,15,17,22,23,24,26,27,28,29,31,33,36,37,38,40,41,43,47,48,49,50

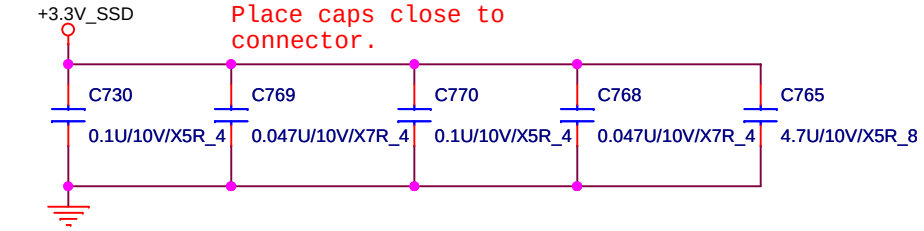
+1.5V
+3V

32









Quanta Computer Inc.

PROJECT : KL8A

Size	Document Number	Rev
	MINI Card (SSD)	1A
Date: Monday, January 03, 2011	Sheet 30 of 53	

Co-layout USB PORT for 2.0&3.0

USB 3.0 function reserved

prevent from leakage

For debug only.
Don't connect to system SMBus

U18

VL800 / VL801 QFN88
VL800 4PORT
VL801 2PORT

Near PCIEx Slot

EC-B-19

Don't need this power with VL801

X'tal 25MHz

Crystal foot print must be reserved in case 25MHz clock from clock generator is not stable enough.

For USB3.0

Remove SUSD turn on switch
(From PCU to SUS)
(Used +3V_S5 power plane)

Remove LDO and connector
+1.05V_PCH to P1V05_SUS

0.6A

SPI Flash ROM

10/08 P/N: AKE34FN0800

USB3.0 : Install
USB2.0 : Remove

USB3.0 : Remove
USB2.0 : Install

ESD

Mount R638 with USB3.0

Mount R637 with USB2.0

Power sequence for Host.

Quanta Computer Inc.
PROJECT : KL8A

Size	Document Number	Rev
	USB3.0	1A
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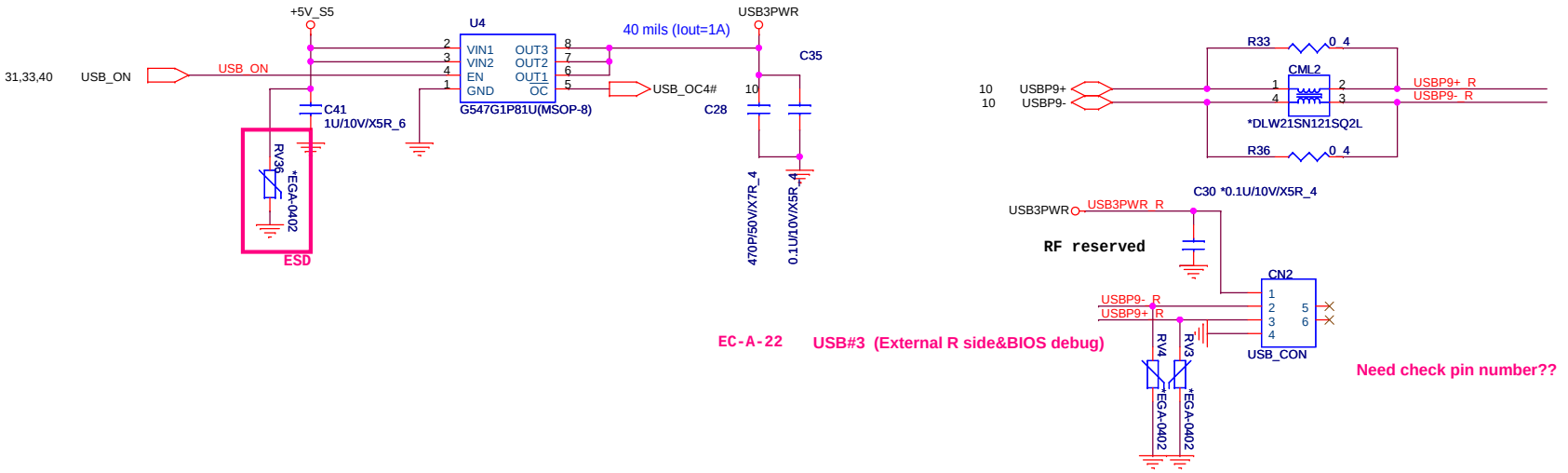
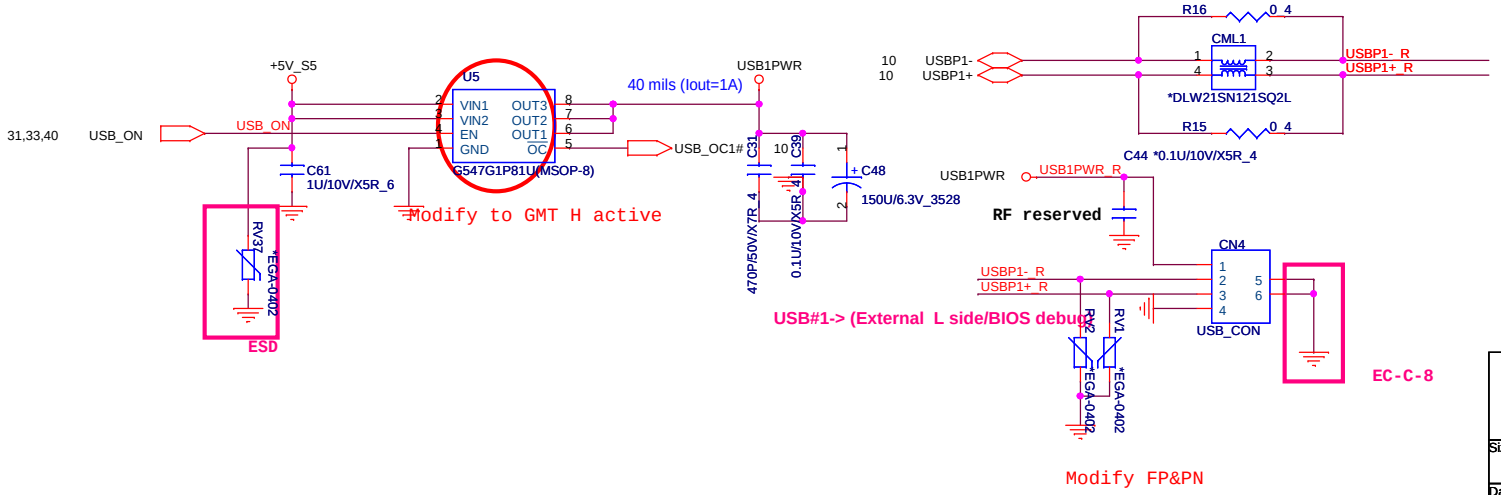
USB2.0*2

External (R side) USB*1



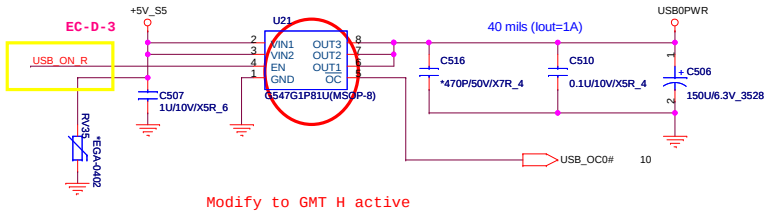
EC-A-22 USB#3 (External R side&BIOS debug)

External (L side) USB*1

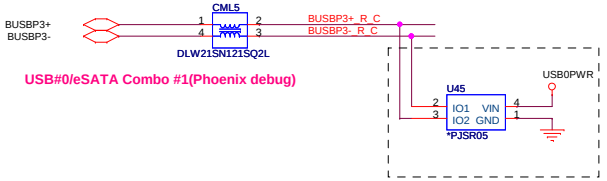


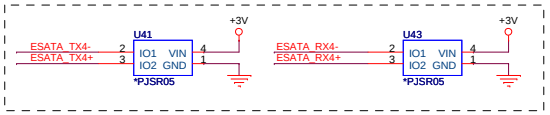
Quanta Computer Inc. PROJECT : KL8A		
Size	Document Number: USB2.0 x 2	Rev: 1A
Date: Monday, January 03, 2011	Sheet 32 of 53	

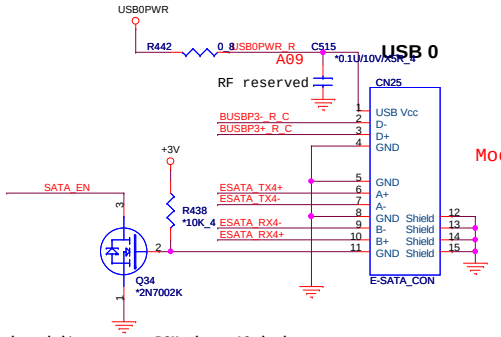
USB + E-SATA



Modify to GMT H active

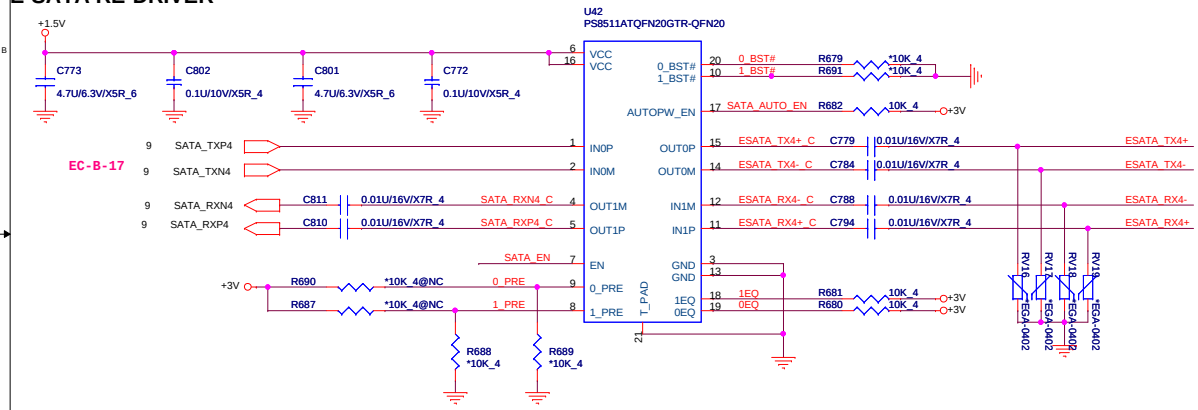






Modify FP&PN

E-SATA RE-DRIVER



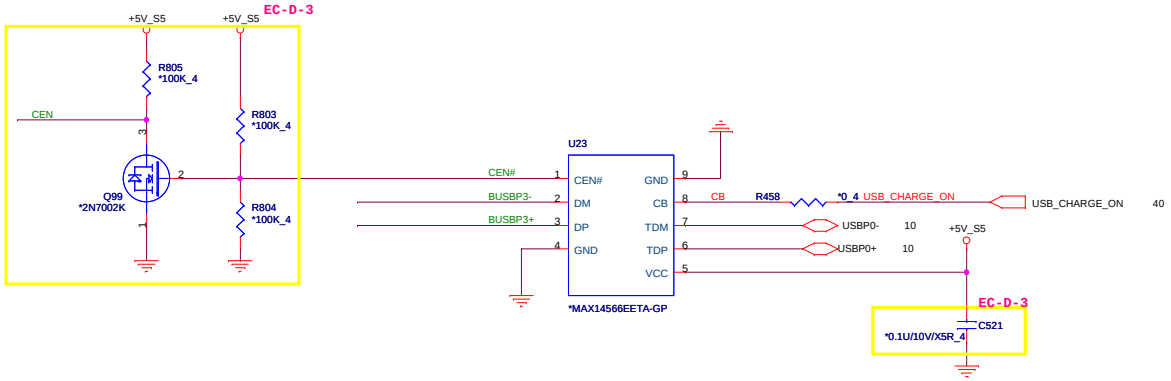
Layout: Locate this IC near to conn 2~3 inch,and it can away PCH above 10 inch.

Straps notice:
1. SATA 3G-->600mV ; 0/1 BST#-->H
2. If input length is over 7 inch ; 0/1EQ-->H

Int.PH(150Kohm) : EN,0/1_BST#
Int.PL(150Kohm) : AUTO_EN,0/1EQ,0/1_PRE

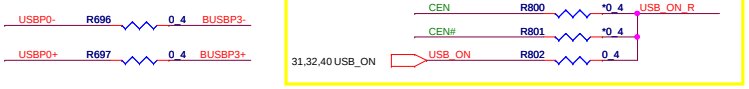
EN	AUTO_EN	0/1EQ	0/1EQ	0/1_BST#	0/1_BST#	0/1_PRE	0/1_PRE	Function
0	X	X	X	X	X	X	X	Standby
1	0	X	X	X	X	X	X	disable auto power saving
1	1	X	X	X	X	X	X	enable auto power saving
1	X	0	X	X	X	X	X	Short and medium length
1	X	X	1	X	X	X	X	Long length
1	X	X	X	0	X	X	X	Output :800~1200 mVpp
1	X	X	X	X	1	X	X	Output :400~700 mVpp
1	X	X	X	X	X	0	X	Pre-emphasis disabled
1	X	X	X	X	X	X	1	Pre-emphasis enabled

USB charger



EC-A-08

Stuff for bypass USB charger



USB Charge Function					
	R696	R697	R800	R802	State
Enable	X	X	V	X	
Disable	V	V	X	V	Default

Quanta Computer Inc.
PROJECT : KL8A

Size	Document Number	Rev
	USB Discharge	1A
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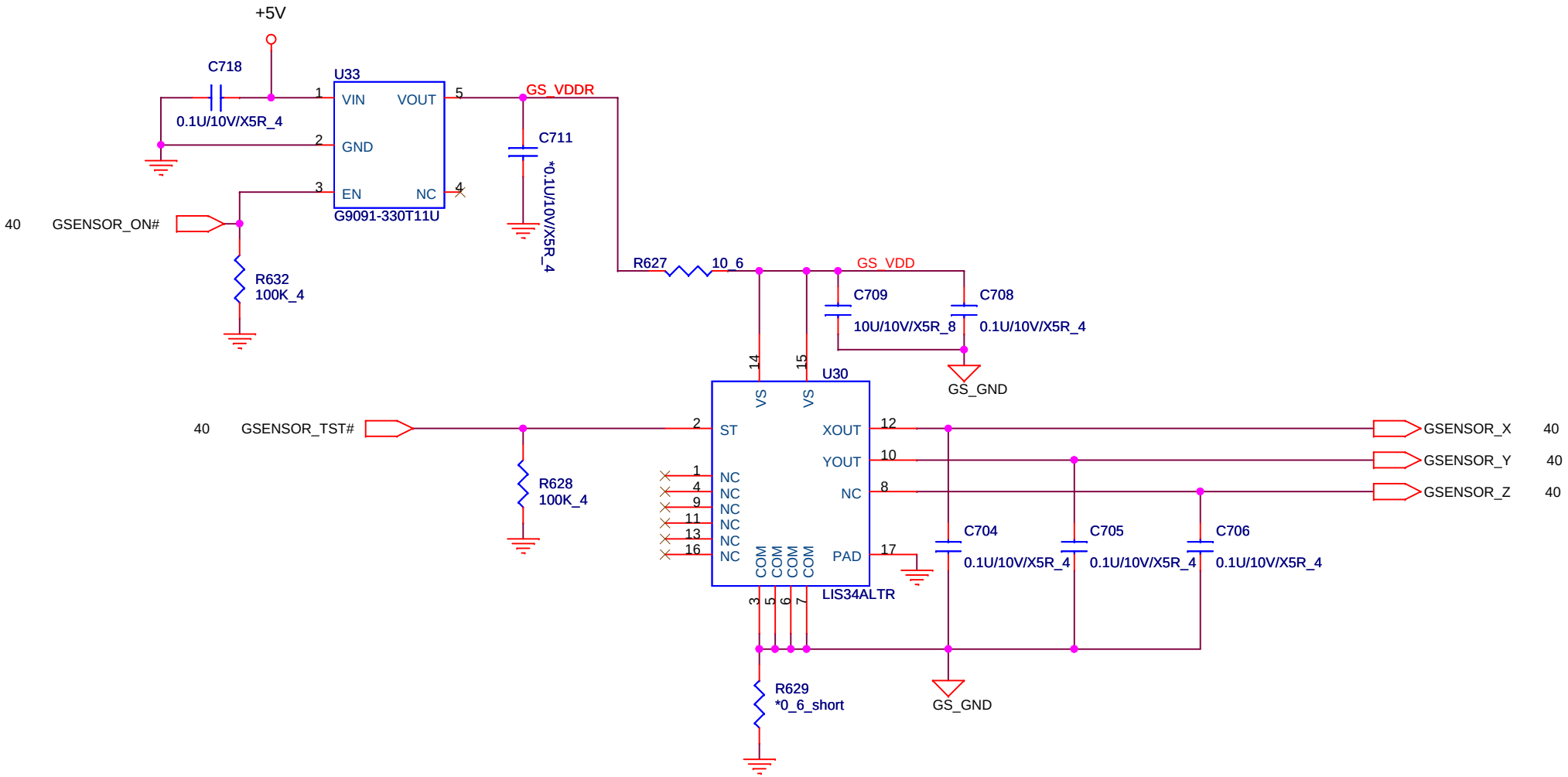
G-SENSOR (3-Axial)

4,8,9,10,11,12,14,15,17,22,23,24,26,27,28,29,30,31,33,36,37,38,40,41,43,47,48,49,50 +3V
24,28,36,38,41,44,45 +15V

38



Quanta Computer Inc.

PROJECT : KL8A

Size	Document Number	Rev
	G-SENSOR	1A
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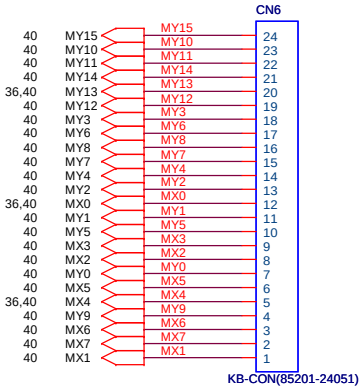
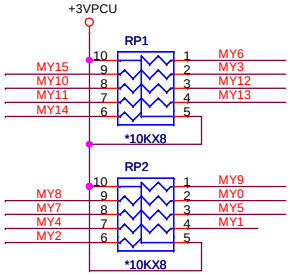
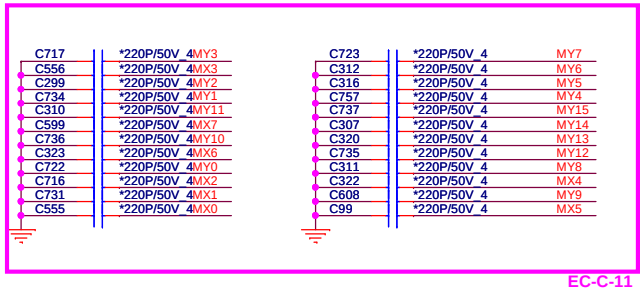
KEYBOARD

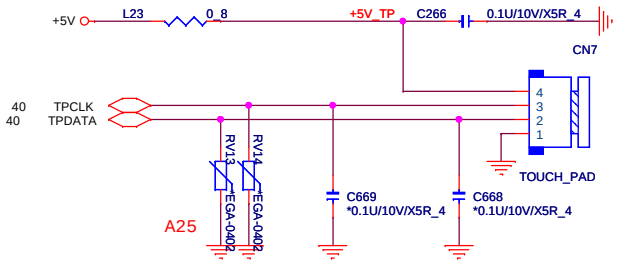






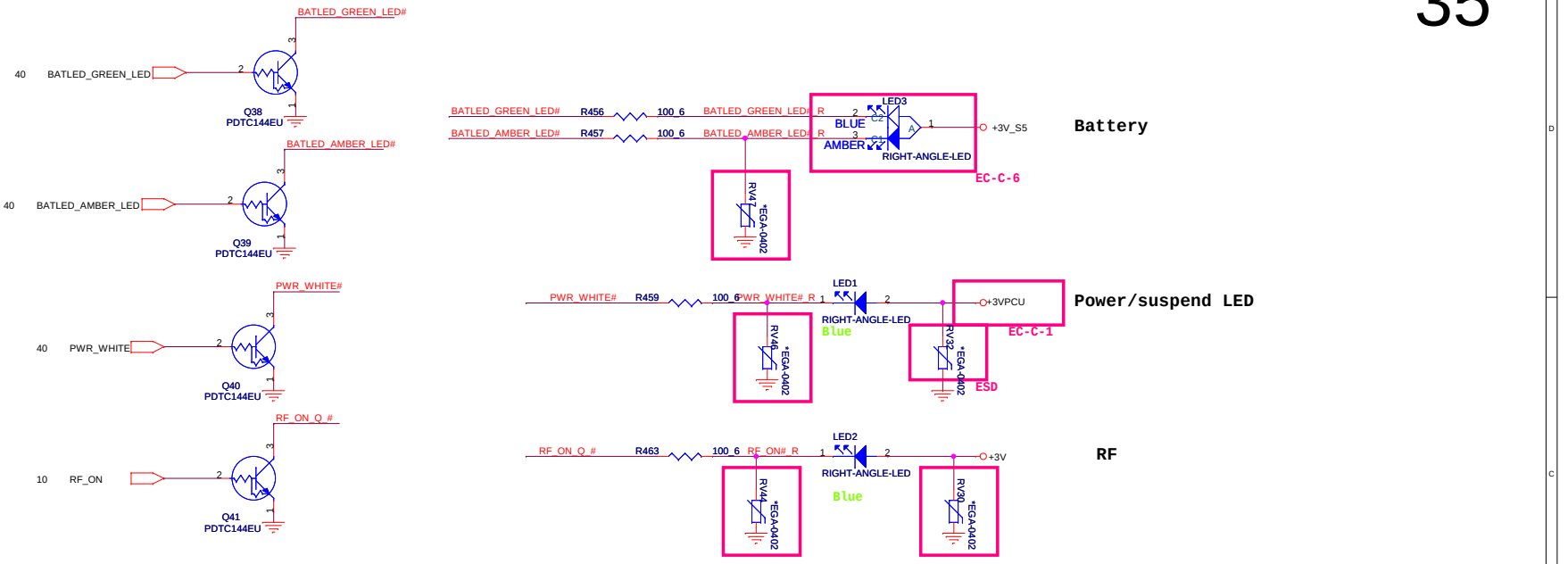
Follow LL3 KB

Touch pad

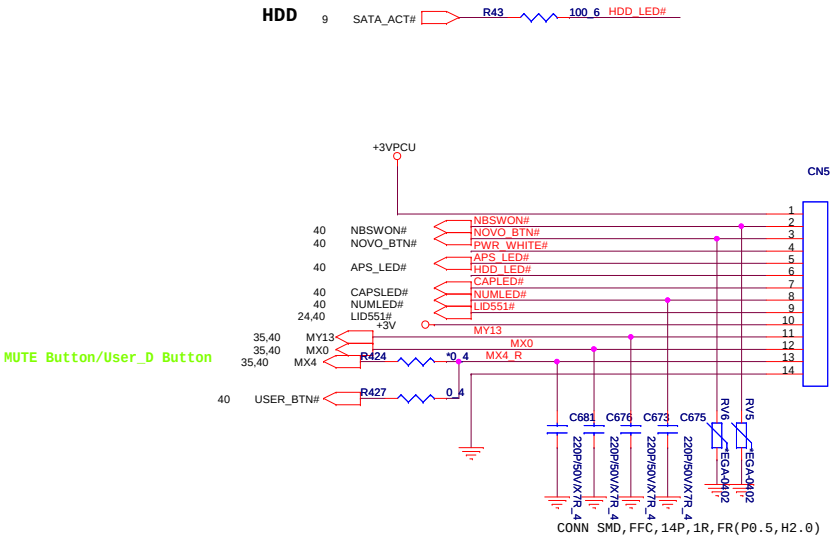


Quanta Computer Inc.		
PROJECT : KL8A		
Size	Document Number: K/B, T/P	Rev: 1A
Date: Monday, January 03, 2011	Sheet 35 of 53	

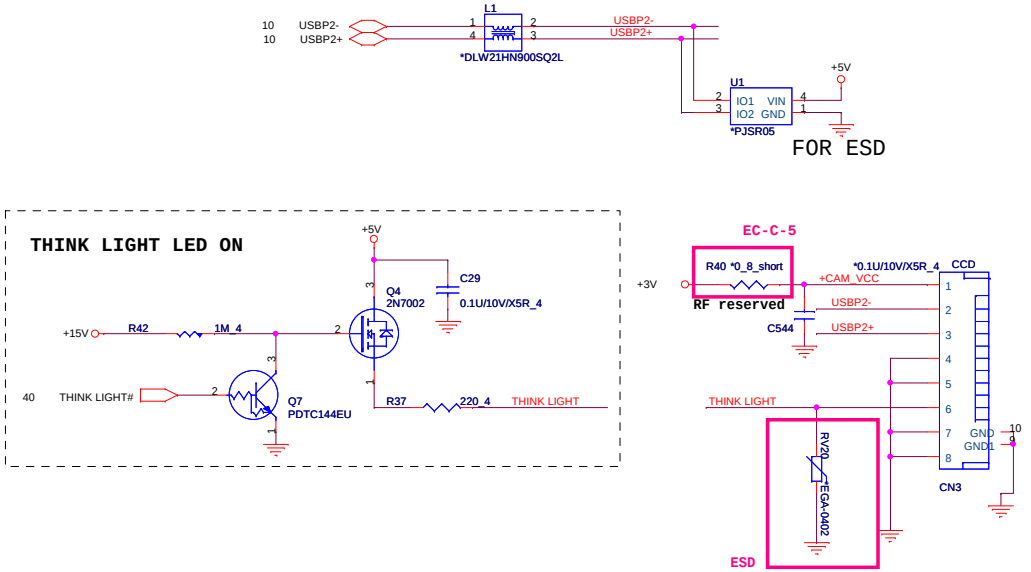
POWER / Battery /RF LED



B to B connector



CAMERA & Keyboard light



Quanta Computer Inc.			
PROJECT : KL8A			
Size	Document Number		Rev
	B TO B CON/LED/CCD		1A
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FAN CONTROL

28

NOTE:
Place C625 near Q37

NOTE:
Place C623 near Q38

NOTE:
Place C624 near U48

NOTE:
Place C627 near Q39

NOTE:
Place C626 near U48

Q46
*SST3904

C707
*100P/50V/X7R_4

DDR3

Q53
*SST3904

C783
*100P/50V/X7R_4

WLAN-ONFI

C206
*2200P/50V/X7R_4

R215
2.05K_4

+5V
R60
*0_8_short
+5V_FAN
C59
1U/10V/X5R_6
C55
0.1U/10V/X5R_4

EC-C-12

R192
*0_4
R190
*0_4
R227
6.8K/F_4

U10
EMC2103-2

+3V

R197 10K_4
R211 10K_4
R207 10K_4
R208 10K_4
R231 10K_4
R230 10K_4

+5V
R238
10K_4

D8
RB500V-40

FAN_PWM
FANSIG
+5V_FAN

CN15
FAN_CON

EC-B-28

ESD

C677
*100P/50V/X7R_4

SST3904
Q43

CPU

C192
2200P/50V/X7R_4

+3V
R180
22_4

3V_FAN

C191
0.1U/10V/X5R_4

DN
DP
VDD
GPIO1
DP2/DN3
DN2/DP3
TRIP_SET
SHDN_SEL
GND
GND
PWM
TACH
SMCLK
GPIO2
ALERT#
SYS_SHDN#
SMDATA

RV29
*EGA-0402

Q16
2N7002

MB_CLK1 10,17,40,43

Q17
2N7002

MB_DATA1 10,17,40,43

SYS_SHDN-1#

Q19
2N7002

SYS_SHDN# 17,45,50

D7
*RB500V-40

VGA_OVT# 40

MB_ALRET#

R184
*0_4

TEMP_ALERT# 11,40

RV21 *EGA-0402
RV22 *EGA-0402
RV23 *EGA-0402

ESD

RV25 *EGA-0402
RV52 *EGA-0402
RV7 *EGA-0402
RV24 *EGA-0402
RV26 *EGA-0402
RV27 *EGA-0402

ESD

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN /THERMAL	1A
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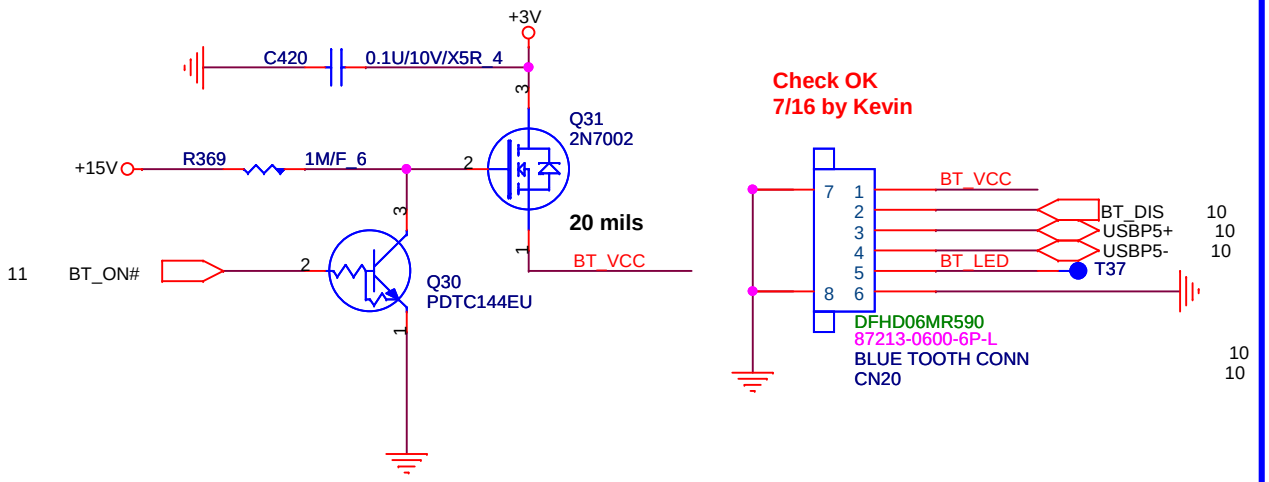
BLUETOOTH

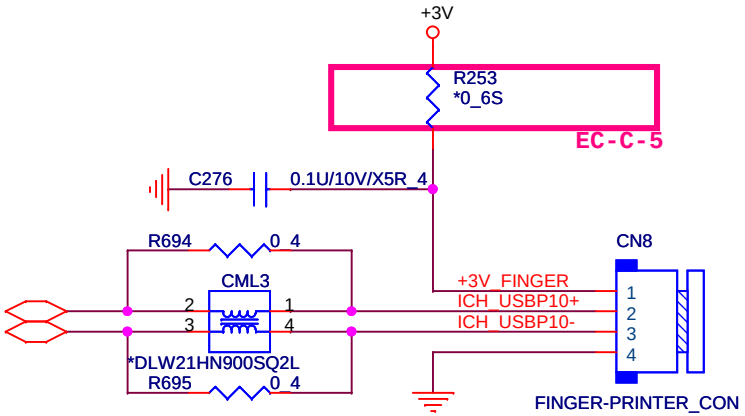


Check OK
7/16 by Kevin

4,8,9,10,11,12,14,15,17,22,23,24,26,27,28,29,30,31,33,36,37,40,41,43,47,48,49,50 +3V
9,12,22,23,26,28,34,35,36,37,40,41,43,50 +5V

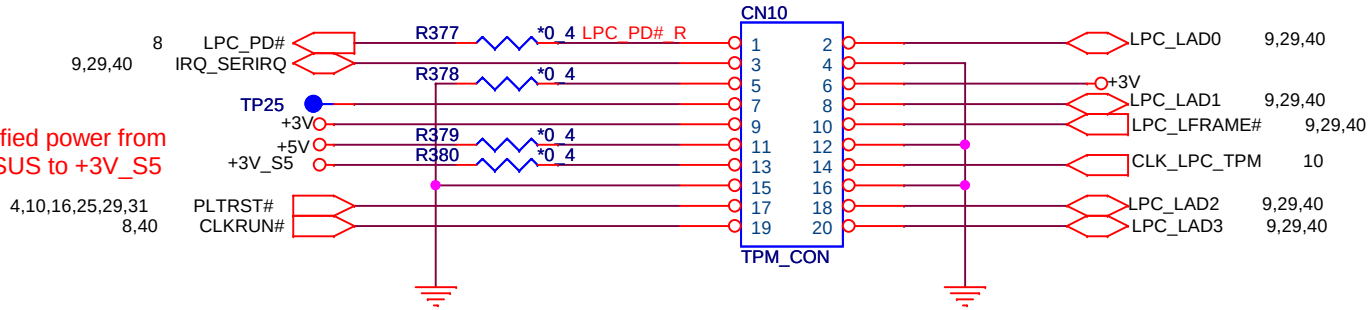
FINGER PRINTER

34



TPM

Modified power from
+3VSUS to +3V_S5



Quanta Computer Inc.
PROJECT : KL8A

Size	Document Number	Rev
	BT/FP/TPM	1A
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WLAN/WWAN/Mini-SSD Nuts

39

HOLE20 *hg-c315d110p2

HOLE3 *h-tc6bc3_76i3d3p2

HOLE5 *H-TC315BC110D110P2

HOLE22 H-TC217BC142D102P2

HOLE23 H-TC217BC142D102P2

HOLE6 *hg-c315d110p2

HOLE2 *hg-c315d110p2

HOLE19 *hg-c315d110p2

HOLE16 *hg-c315d110p2

HOLE14 *hg-c315d110p2

HOLE17 *hg-c315d110p2

HOLE1 *hg-c315d110p2

HOLE25 H-TC217BC75I75D35P2

HOLE24 H-TC217BC75I75D35P2

VGA Nuts

HOLE21 H-TC217BC142D118P2

TPM

HOLE13 h-tc217bc98d59p2

HOLE10 h-tc217bc98d59p2

HOLE8 *H-C394D315X335PBD10

HOLE7 *h-o276x866d276x866n

EC-D-7

CPU BKT

HOLE15 *h-c118d118n

HOLE18 *h-c118d118n

HOLE9 *HG-E315X268D110P2

FAN

HOLE4 *h-c1260d1260na1300

BKT1

cpu-bracket

Screw Hole

HOLE26 H-TC217BC142D102P2

ESD

+0.85V SC28 *220P/50V/X7R_4

+3V SC8 SC9 SC7 *0.1U/25V/X5R_4 SC24 *0.1U/25V/X5R_4

+1.05V_PCH +0.85V SC20 *0.1U/25V/X5R_4

+VCC_CORE SC40 *0.1U/25V/X5R_4

+VGPU_CORE +3V SC41 SC42 *0.1U/25V/X5R_4

+3V SC29 SC31 SC32 *220P/50V/X7R_4

+1.5V_SUS SC34 SC33 SC27 *0.1U/25V/X5R_4

+1.05V_PCH +3V SC14 SC13 *0.1U/25V/X5R_4

+VGPU_CORE SC25 *0.1U/25V/X5R_4

+1.05V_PCH SC16 SC15 *0.1U/25V/X5R_4

+0.85V +3V SC17 SC18 SC4 *0.1U/25V/X5R_4

+5V RV39 RV40 RV41 *EGA-0402

EC-D16-Add ESD/EMI sulotion

+VCC_CORE SC46 SC47 SC48 SC49 SC50 SC51 SC52 SC53 0.1U/25V/X5R_4

+VCC_CORE SC58 SC59 SC60 SC61 SC54 SC55 SC56 SC57 0.1U/25V/X5R_4

+1.05V_PCH SC62 SC63 SC64 SC65 0.1U/25V/X5R_4

+0.85V SC66 SC67 SC68 SC69 0.1U/25V/X5R_4

+1.8V SC78 SC79 SC80 0.1U/25V/X5R_4

+1.5V_SUS SC81 330U/2V/ESR9_7343

+1.5VCPU SC74 SC75 SC76 SC77 0.1U/25V/X5R_4

EMI

+5V_S5 SC30 *220P/50V/X7R_4

+1.05V_VCCEPW SC44 *220P/50V/X7R_4

+5V SC43 *220P/50V/X7R_4

VBATT_A SC82 0.1U/25V/X5R_4

VIN SC90 SC88 SC85 SC86 SC87 SC83 SC84 SC89 0.1U/25V/X5R_4

Quanta Computer Inc.

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	HOLD & SKEW	1A

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EC pins are modified on 7/29

IT8518 IT8519

RF ON/OFF SWITCH

POWER SWITCH/ NOVO BUTTON

16Mbit (2M Byte), SPI

Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13

10/8 P/N: AKE37FN0N01 4M-bit

Borad ID

Width = 6mils Spacing = 10 mils

P/N: AJ085180F01

Quanta Computer Inc.	
PROJECT : KL8A	
Size	Document Number: KBC IT8512E
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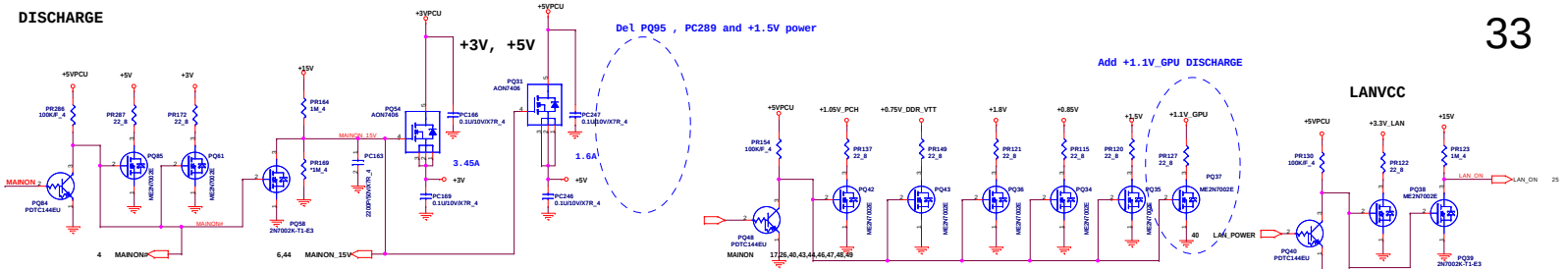
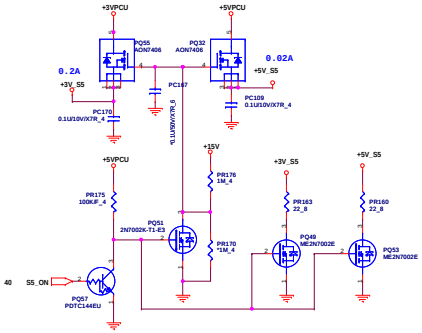
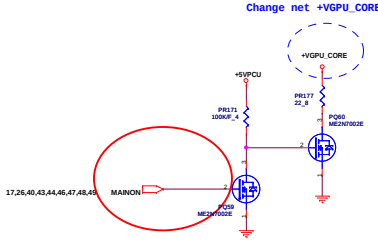
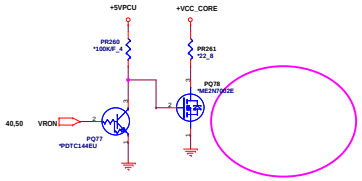
DISCHARGE

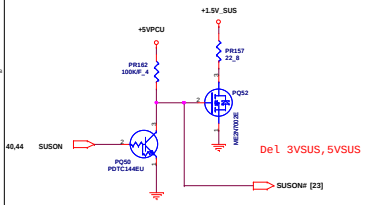


3V_S5, 5V_S5









PROJECT KL5A Quanta Computer Inc.		
Size: D	Document Number: Discharge	Rev: 1A
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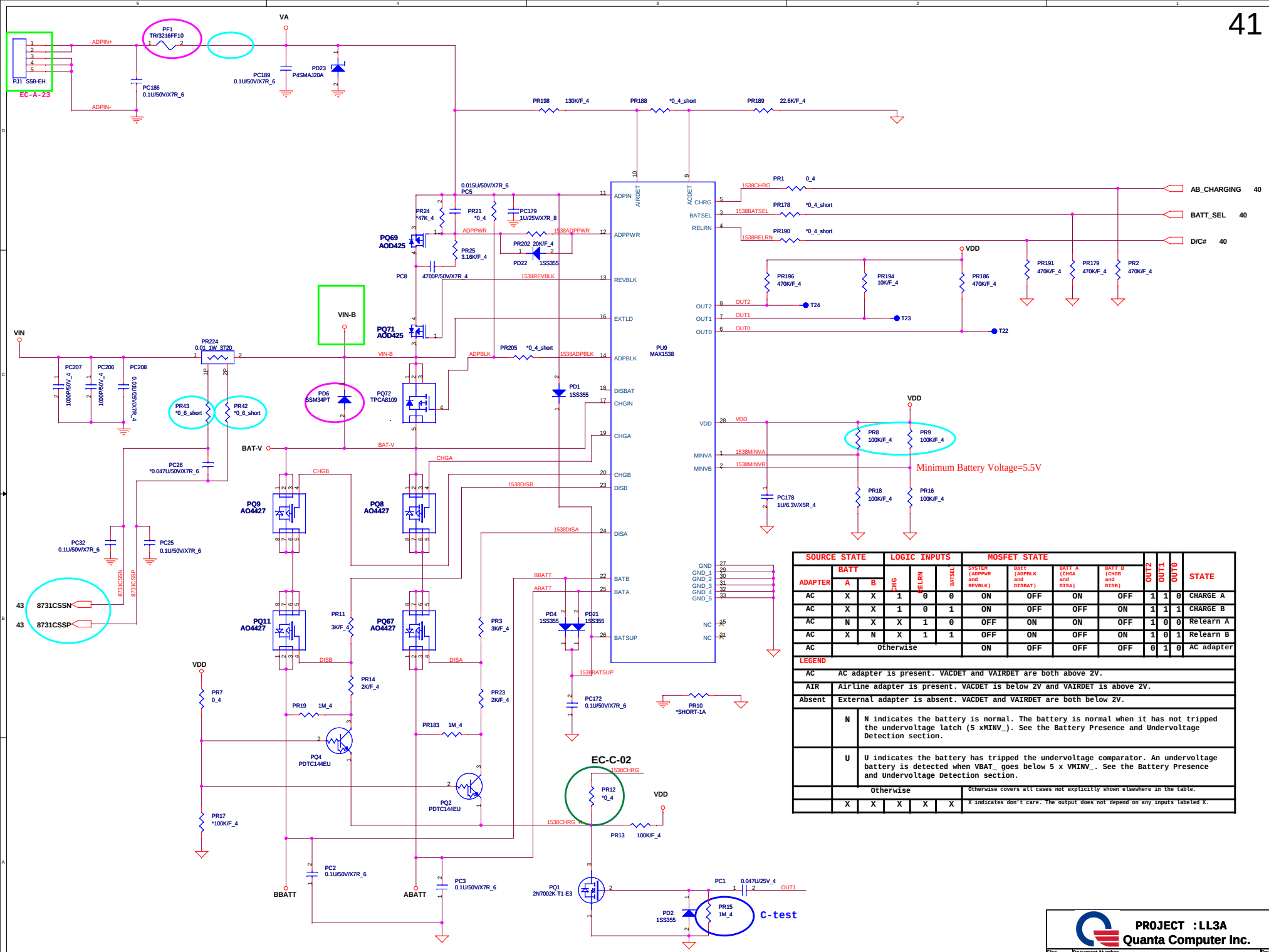


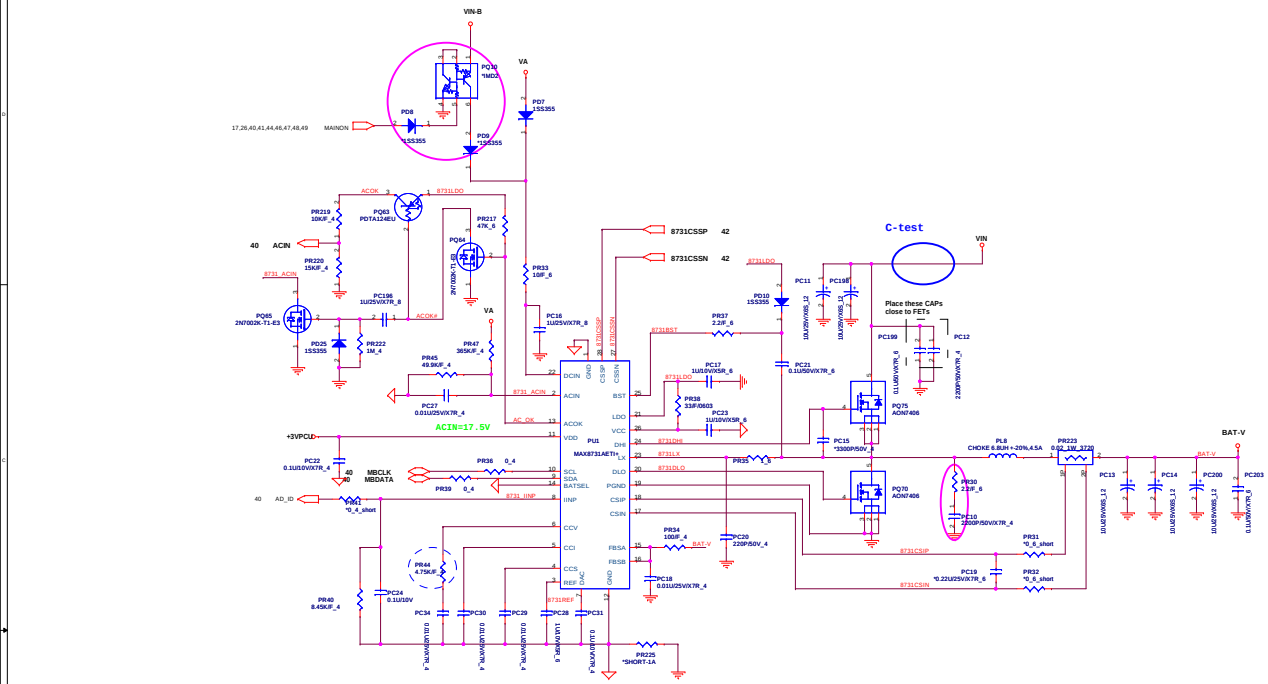
SOURCE STATE			LOGIC INPUTS			MOSFET STATE							
	BATT												
ADAPTER	A	B	CHG	RELRN	BATSEL	SYSTEM (ADPPWR and REVBLK)	Batt (ADPBLK and DISBAT)	BATT A (CHGA and DISA)	BATT B (CHGB and DISB)	OUT2	OUT1	OUT0	STATE
AC	X	X	1	0	0	ON	OFF	ON	OFF	1	1	0	CHARGE A
AC	X	X	1	0	1	ON	OFF	OFF	ON	1	1	1	CHARGE B
AC	N	X	X	1	0	OFF	ON	ON	OFF	1	0	0	Relearn A
AC	X	N	X	1	1	OFF	ON	OFF	ON	1	0	1	Relearn B
AC	Otherwise					ON	OFF	OFF	OFF	0	1	0	AC adapter

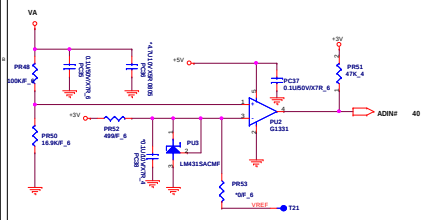
LEGEND

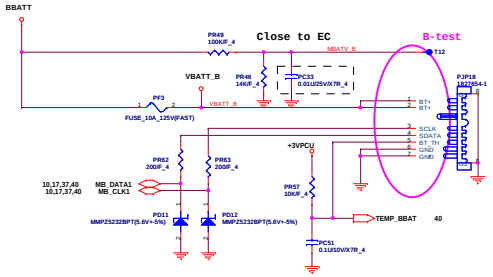
AC	AC adapter is present. VACDET and VAIRDET are both above 2V.
AIR	Airline adapter is present. VACDET is below 2V and VAIRDET is above 2V.
Absent	External adapter is absent. VACDET and VAIRDET are both below 2V.
N	N indicates the battery is normal. The battery is normal when it has not tripped the undervoltage latch (5 xMINV_). See the Battery Presence and Undervoltage Detection section.
U	U indicates the battery has tripped the undervoltage comparator. An undervoltage battery is detected when VBAT_ goes below 5 x VMINV_. See the Battery Presence and Undervoltage Detection section.
Otherwise	Otherwise covers all cases not explicitly shown elsewhere in the table.
X	X indicates don't care. The output does not depend on any inputs labeled X.

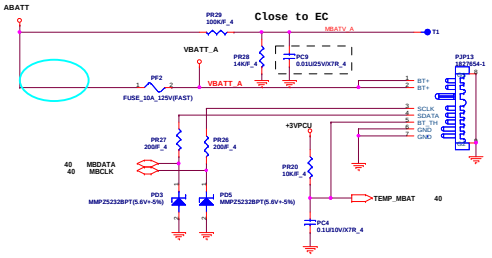
PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
C	Battery Selector (MAX1538)	1C
Date: Monday, January 03, 2011	Sheet 42 of 53	

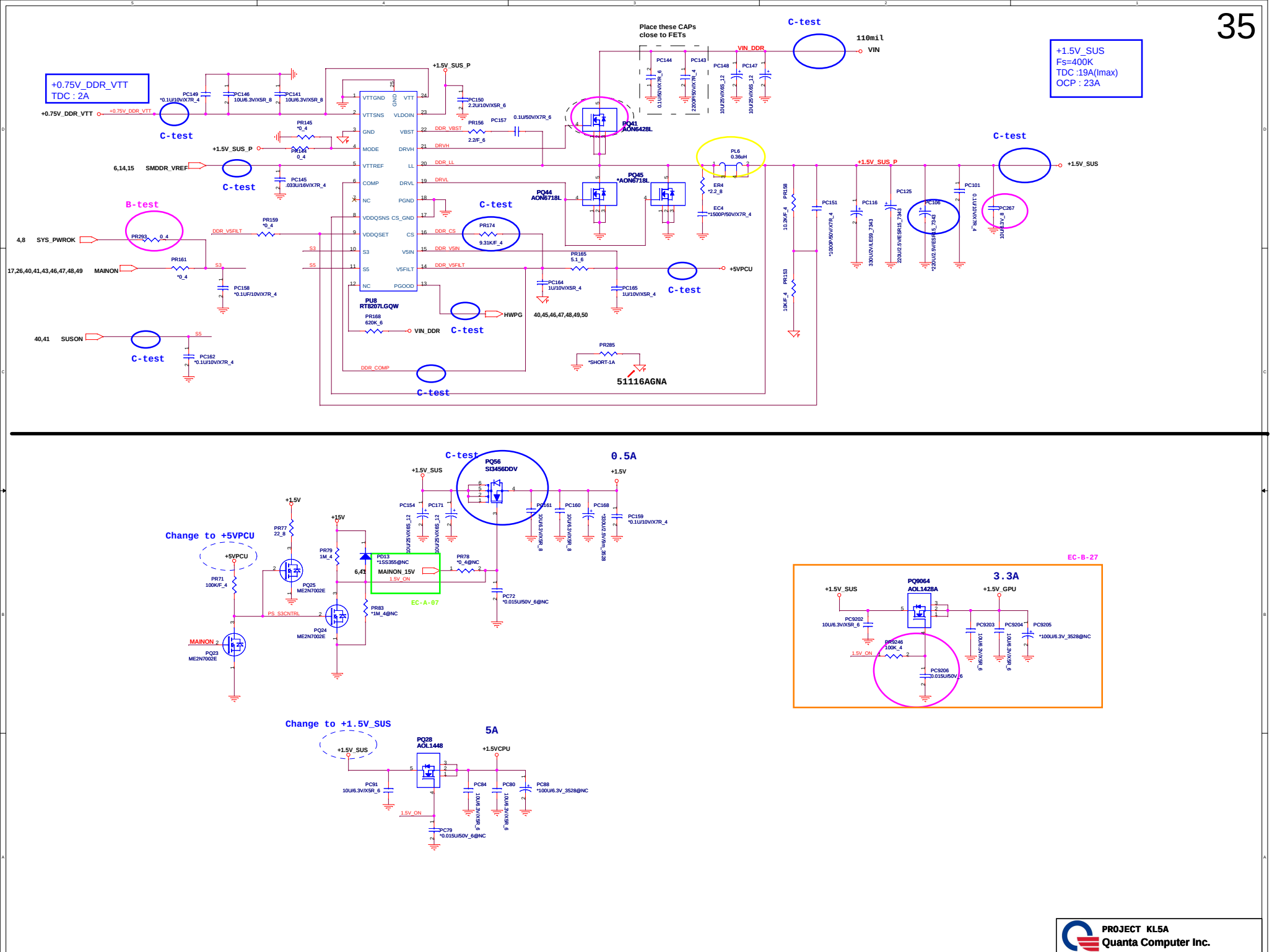








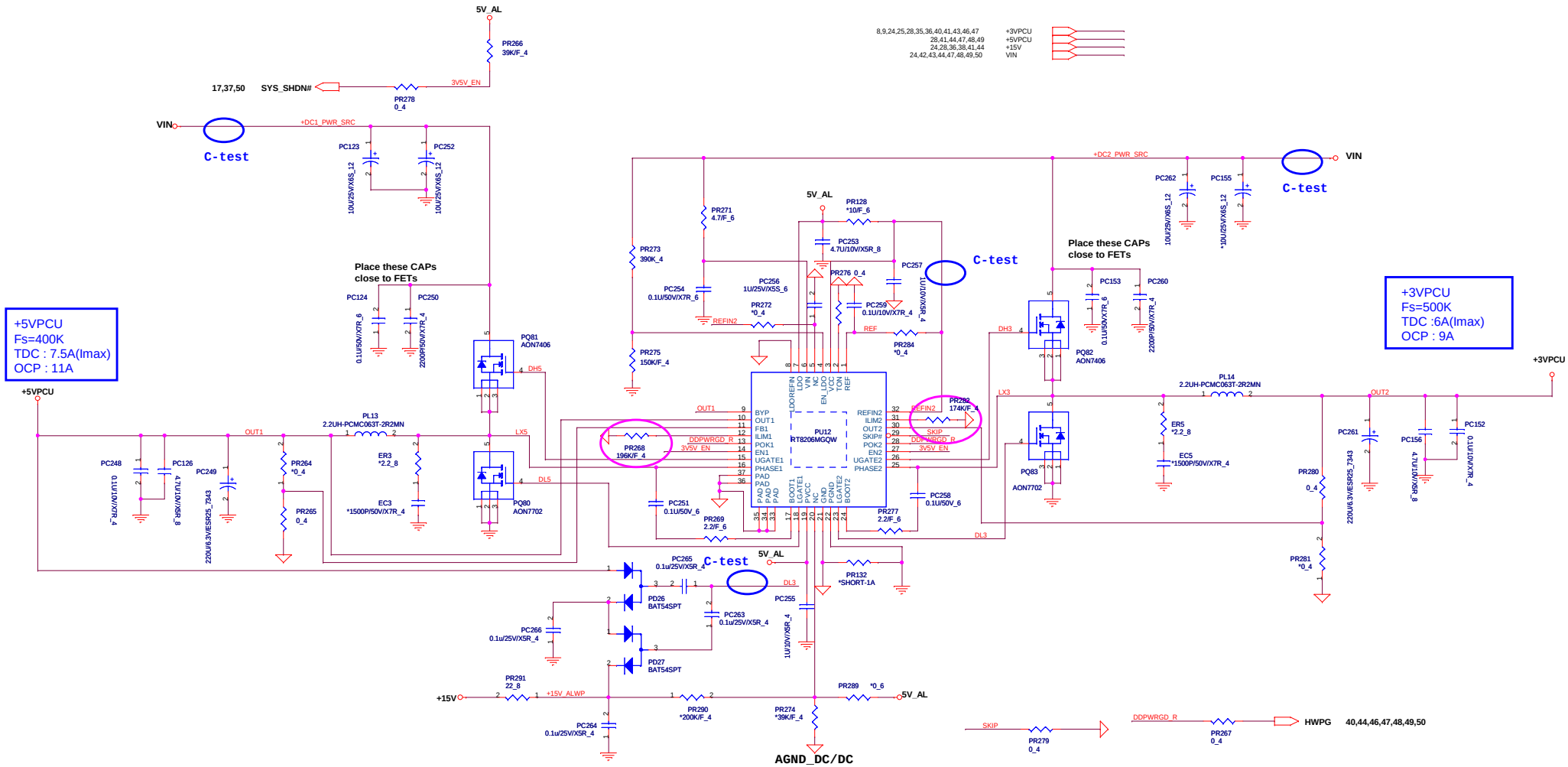
PROJECT : LL3A Quanta Computer Inc.			
Size D	Document Number Charger(MAX8731)		Rev 1C
Date: Monday, January 03, 2011		Sheet 43 of 53	

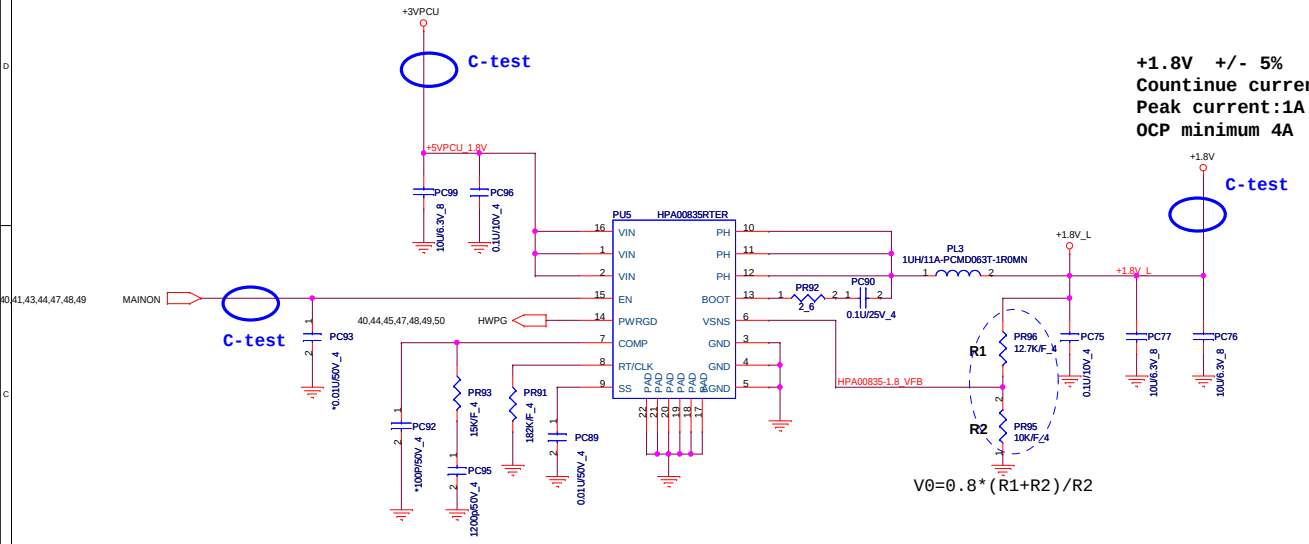


PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3/0.75V(RT8207AGQW)	1A

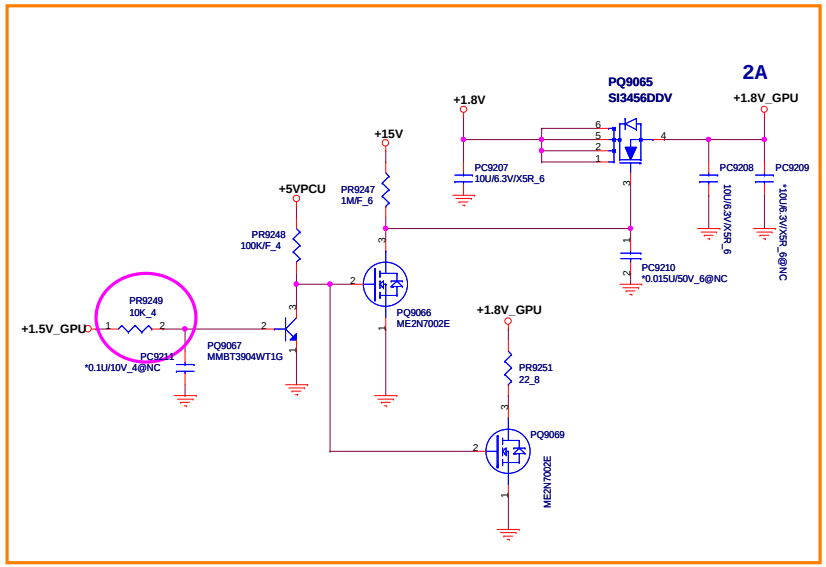
Date: Monday, January 03, 2011 Sheet 44 of 53


+5VPCU
Fs=400K
TDC : 7.5A(Imax)
OCP : 11A
+3VPCU
Fs=500K
TDC :6A(Imax)
OCP : 9A
Place these CAPs close to FETs
Place these CAPs close to FETs
C-test
C-test
C-test
C-test
5V_AL
VIN
+DC1_PWR_SRC
+DC2_PWR_SRC
SYS_SHDN#
3V5V_EN
+15V
+15V_ALWP
PU12 RT8206MGQW
PQ80 AON7702
PQ81 AON7406
PQ82 AON7406
PQ83 AON7702
PL13 2.2UH-PCMC063T-2R2MN
PL14 2.2UH-PCMC063T-2R2MN
PD26 BAT54SPT
PD27 BAT54SPT
AGND_DC/DC
HWPG
40,44,46,47,48,49,50
PROJECT KL5A
Quanta Computer Inc.
3V/5V (RT8206BGQW)
Monday, January 03, 2011
Sheet 45 of 53



+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A
OCP minimum 4A

EC-B-27



PROJECT KL5A Quanta Computer Inc.		
Size: Custom	Document Number: +1.8V (HPA00835RTER)	Rev: 1A
Date: Monday, January 03, 2011	Sheet 46 of 53	

Place these CAPs close to FETs

+VGPU_CORE
Fs=300K
TDC : 16.8A(Imax)
OCP : 33.6A

Close To VGPU Discrete Power Rail Side

Change to +VGPU_CORE

Del 3VSUS , PR9034

Change to +1.5V_SUS

Change to +5VPCU

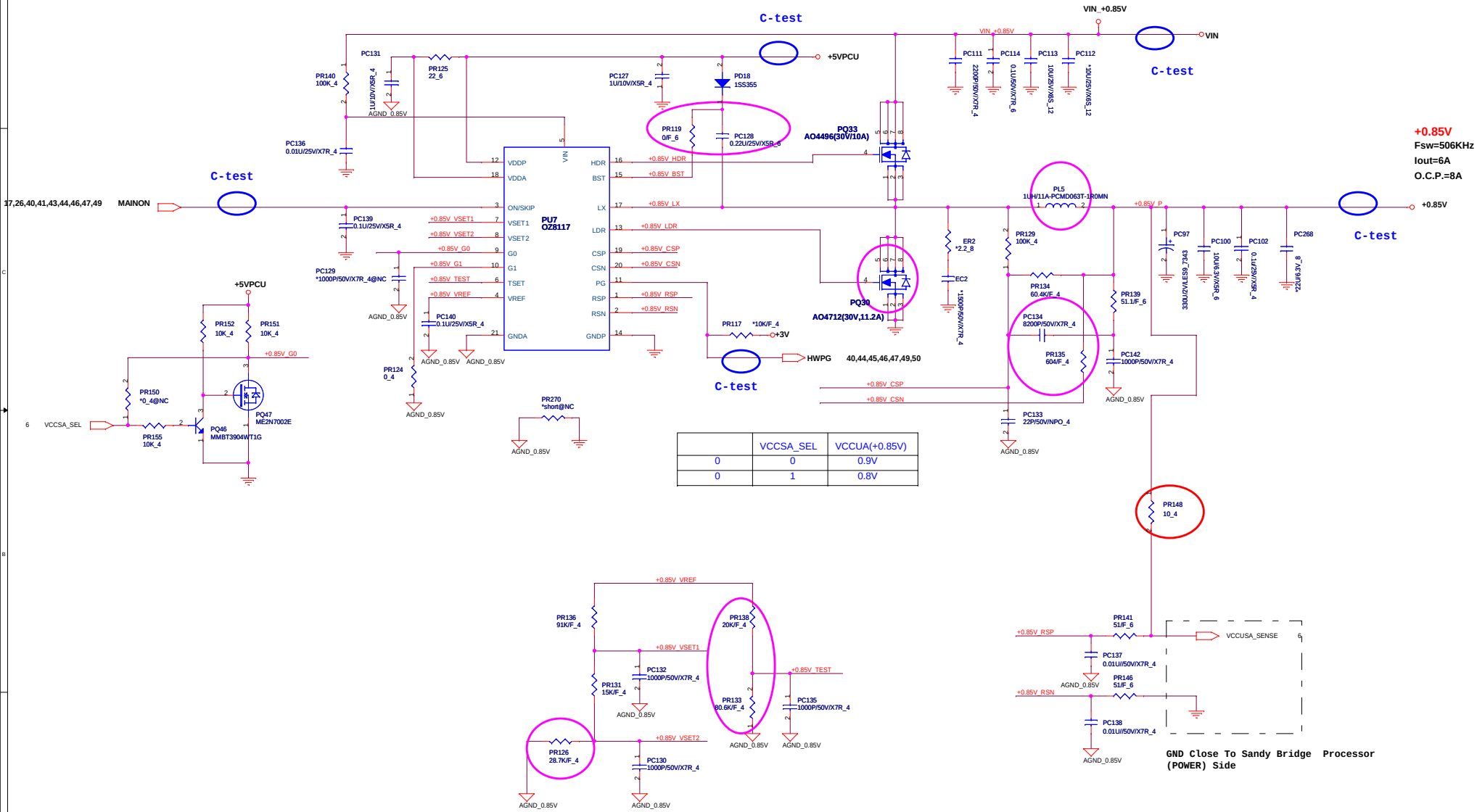
+1.1V_GPU
Iout=2A

VO=(0.8(R1+R2)/R2)
R2<120Kohm

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VCC_GFX_CORE
1	1	1.15V
1	0	1.0V
0	1	1.1V
0	0	0.9V

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGPU_CORE (OZ8117)	1A
Date: Monday, January 03, 2011	Sheet 47 of 53	



	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V

PROJECT KL5A			
Quanta Computer Inc.			
Size C	Document Number +0.85V (OZ8117)		Rev 1A
Date: Monday, January 03, 2011	Sheet 48 of 53		

The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:

- NVVDD <= VDD33+0.5 V
- FBVDDQ <= VDD33+0.5 V

+1.05V_PCH

VIN=20V, FSW(KHZ)=226K
VIN=9V, FSW(KHZ)=210K
Iout=17.5A
O.C.P.=20A

17,26,40,41,43,44,46,47,48 MAINON

PU6 OZ8117

PQ26 AON6718L
PQ27 *AON6718L
PQ29 AON6428L

PL4 0.36uH

C-test

HWPG 40,44,45,46,47,48,50

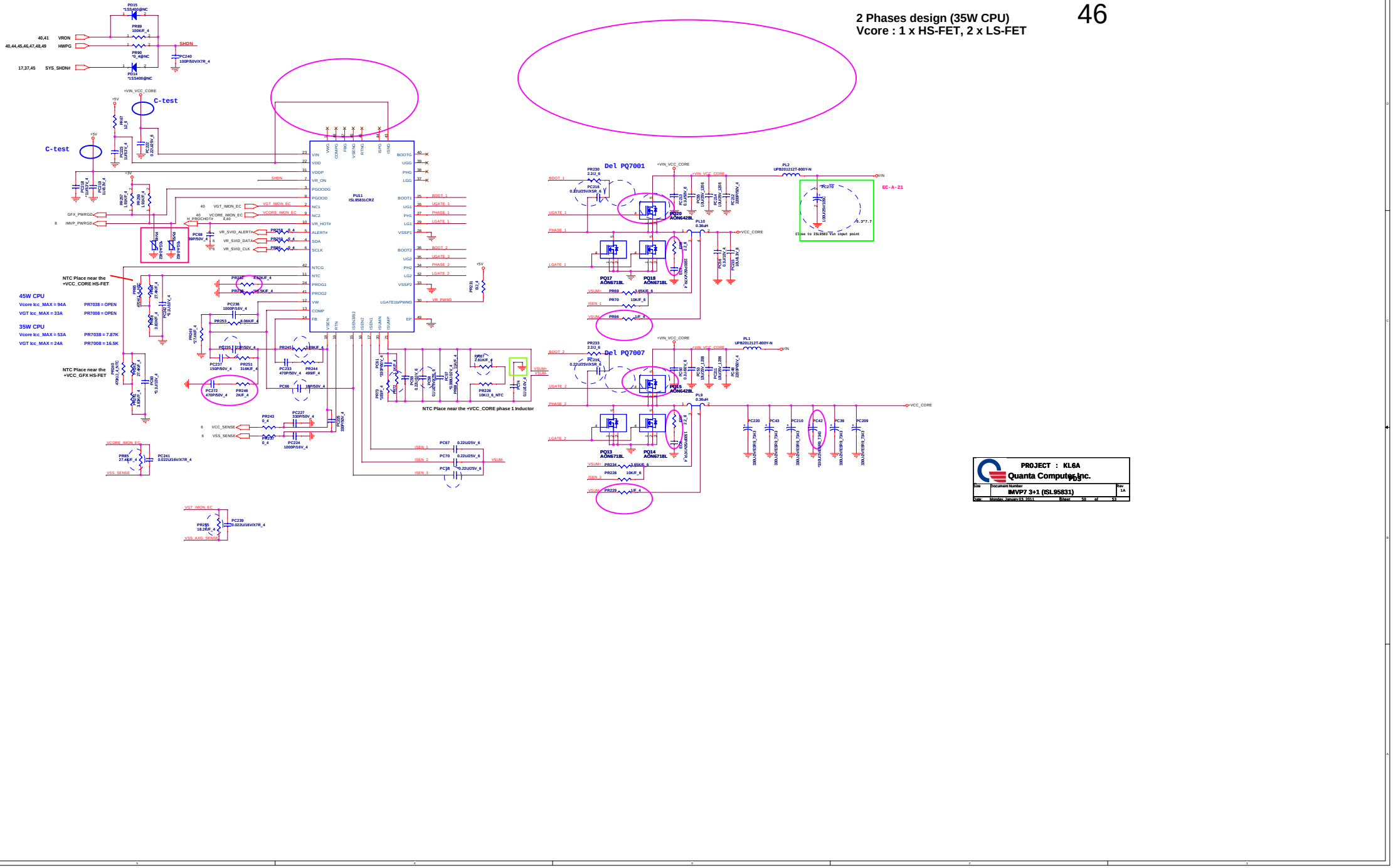
Change to AGND_1.05V_PCH

GND Close To Sandy Bridge Processor (POWER) Side

Del +1.5V SW

PROJECT KL5A		
Quanta Computer Inc.		
Size C	Document Number +1.05_PCH (OZ8117)	Rev 1A
Date: Monday, January 03, 2011	Sheet 49 of 53	

2 Phases design (35W CPU)
Vcore : 1 x HS-FET, 2 x LS-FET



EC #	Page	Description	Part Affected
EC-B-02	8	Del Int HDMI to Keep VGA schematic to Dis only	C608/C599/Q21/R595/R242/R585/R254
EC-B-03	22	Del Int HDMI to Keep VGA schematic to Dis only	U14
EC-B-04	8	Del Int LVDS/ Int CRT net and relate parts	
EC-B-05	12	Del Int LVDS power to Keep VGA schematic to Dis only	change C616/C617/C284 to ASM and change R580/R590 to stuff
EC-B-06	17	change GPU form Robson to Seymour, follow AMD refer schematic	change R229,R162,R572,R206,R9221,R9223,R9224 No ASM
EC-B-07	17	change GPU form Robson to Seymour, follow AMD refer schematic	change R9221,R9223,R9224 No ASM
EC-B-08	23	Del INT_CRT net in CRT connrctor side,Del Int CRT net to Keep VGA schematic to Dis only	
EC-B-09	24	Del Int LVDS net to Keep VGA schematic to Dis only	
EC-B-10	24	Del Int LVDS to Keep VGA schematic to Dis only,Del R45/R47 location	Del R45/R47 location
EC-B-11	33	change U21 pin.4 from USB_ON to USB_CHARGE_ON for S5 power save	
EC-B-12	27	add Card reader SD 3.0 net	U12,CN11
EC-B-13	4	change U15 P/N	CN15
EC-B-14	9	Fineture GPU 3.3V Power timming	Add L8034,C9476,C9390,C9475 ASM
EC-B-15	10,31,25	change PCH GPIO66 form CLK_26M_LAN to PCH_CLK_25M	
EC-B-16	11	change Board ID GPIO pin	
EC-B-17	26	connector LINEOUT_JD# and LINEOUT_JD derect for normal open Phone jack reserve	add R537/R552
EC-B-18	29	swap CN 24 pin.8,10,12,14,16 for correct LPC pin	CN24
EC-B-19	31	Correct the pin connection of CN8.	U18
EC-B-20	33	swap U42 pin.4,5 SATA_RXN4/SATA_RXP4	U42
EC-B-21	35	swap CN7 pin.1~4	CN7
EC-B-22	36,40	change THINK LIGHT# connect to U14 pin.86 , Add R532	Q7/U14/R532
EC-B-23	36	add R427 connect CN5 pin.13 to U14 pin.20 , add R435	ASM C673/C675/C676/681 , CML4/CML2/CA1~CA6 ASM
EC-B-24	31,32,36	EMI solution	
EC-B-25	4,10	change to DIS only schematic,del CLK_DPLL_SSCLKP/N net and R294	R294
EC-B-26	46,48	del Int LVDS power	L28,R589 No ASM
EC-B-27	16~21, 44,46	for GPU power isolate,add +1.5VGPU and +1.8VGPU	
EC-B-28	37	change FAN connector pin define for standar parts rule	CN15
EC-B-29	10	Add connect PCIECLKREQ 0,5,6,7,PEG_B_CLKRQ to pull high 10K	U11B,R569,R585,R587,R589,R593,R630

KL8A Schematic EC Tracking Record B (for A2 --> B)Oct. 26, 2010

EC #	Page	Description	Part Affected
EC-B-30	**4**	Del XDP_DBRST# pull high Res	
EC-B-31	**4,8**	Add VCCSA_SEL pull low	**ASM R45**
EC-B-32	**40**	del SLP_A# connect to EC pin.88	**U14 pin.88**
EC-B-33	**11,40**	Change EC GPIO	**U17**
EC-B-34	**9**	change to 6pF for fineturn X'tal Freq	**C114,C113**
EC-B-35	**9**	Change EC P/N and X'tal no ASM	**Y4,C372,C366**
EC-B-36	**40**	Reserve GFX_CORE_CNTRL0/GFX_CORE_CNTRL1 VID pull down Res for AMD FAE suggest	**R130,R131**
EC-B-37	**17**	Follow AMD FAE suggest for Syemour	**R573 No ASM**
EC-B-38	**17**	Fineture VRAM RST timming,change R/C vaule	**R28 No ASM, R29,R30,C19 ASM**
EC-B-39	**17**	Reserve GFX_CORE_CNTRL0/GFX_CORE_CNTRL1 VID pull down Res for AMD FAE suggest	**R130,R131**
EC-B-40	**17**	Reserve GFX_CORE_CNTRL0/GFX_CORE_CNTRL1 VID pull down Res for AMD FAE suggest	**R130,R131**
EC-C-1	**36**	Change Power LED1 power plan from +3V_S5 to +3VPCU	
EC-C-2	**40**	PWR_WHITE change from pin.24 to pin.47	
EC-C-3	**40**	Add EAPD and reserved D23	**D23 No ASM**
EC-C-4	**4**	change PM_DRAM_PWRGD_Q to PM_DRAM_PWRGD_R,	**R315,U15 , C363 , No ASM**
EC-C-5	**All**	change Res 0 ohm to short pad	
EC-C-6	**22**	LED Symbol update for SMT require,SWAP Bettery LED pin.1 and Pin.3	**LED3**
EC-C-7	**25**	Add C728,C712 location 0.1u cap for EMI require	**C728 ,C712 No ASM**
EC-C-8	**12**	connect CN4 pin.5,6 to GND for EMI require	**CN4**
EC-C-9	**22**	change Res vaule	**R399,R400,R401,R402,R403,R404,R405,R406 change from 499 to 680 ohm**
EC-C-10	**12**	change Res value from 0.002 to 0 ohm	**R248,R262,R255**
EC-C-11	**35**	Del CA1~6, change to 0402 cap **ADD And ASM :C99,C608C,322,C311,C735,C320,C307,C737,C757,C316,C312,C723,C555,C731,C716,C722,C323,C736,C599,C310,C734,C299,C556,C717**	
EC-C-12	**37**	add Res R190,R192	No ASM R190,R192
EC-D-1	**11**	modify schematic the SV_DET(GPIO57) signal of PCH that pull high from +3V to +3V_S5	
EC-D-2	**09**	change Cap vaule for RTC time issue	change C113,C114 from 6pF to 18pF
EC-D-3	**33**	modify USB charger circuit	Add Q99, R800,R801,R803,R804,R805 location and No ASM. Add R802 location and ASM. change C521 from ASM to No ASM
EC-D-4	**27**	unmount EMI solution in cardreader SD_CLK net	C422 change to No ASM
EC-D-5	**26**	cencel Audio jack normal close reserve circuit	Del Q35,R412,Q37,Q440 location
EC-D-6	**09**	Del JTAG debug reserved circuit for un-used	change R183,R182,R524,R530,R529,R534,R169 from No ASM to Del location

KL8A Schematic EC Tracking Record B (for A2 --> B)Oct. 26, 2010

EC #	Page	Description	Part Affected
EC-D-7	**39**	change Hole 8 to NPTH	Hole8 change from PTH to NPTH
EC-D-8	**39**	reserved Res for ESD require	Add R850,R851,R852,R853,R854,R856 location and ASM
EC-D-9	**04**	Add C758 location for reserved	Add C758 location but No ASM
EC-D-10	**04**	modify Mainon# timing	R326,Q29 change from No ASM to ASM
EC-D-11	**08**	reserved SYS_PWROK	Add C900 location and No ASM
EC-D-12	**08**	Del PM_DRAM_PWRGD pull high Res	change R489 from ASM to No ASM
EC-D-13	**09**	change 0 ohm to short pad for cost down	change R409 and R154 from Res 0603 to short pad (No ASM)
EC-D-14	**30**	+1.5V_WIMAX	change C727,C777,C776 from ASM to No ASM
EC-D-15	**30**	ACZ_SYNC_CODEC add pull down resister	Add R900 location and ASM
EC-D-16	**39**	ESD solution EMI solution	Del SC1,SC22,SC23,SC26,SC35,SC36,SC37,SC38,SC39,SC45 locatoion Add SC46 ~ SC80 location and ASM Add SC82 location and ASM
EC-D-17	**22**	change HDMI connector for EMI require	CN21 change to P/N:DFHD19MR146
EC-D-18	**31**	Modify USB3.0 for power save	Del Q36 , R413,R414, location, R420 change from 0 ohm to 10K
			Add D100 ,R906 location and ASM,
			Add D100 l,R902 ,Q100,C901 ,C902 ,Q101,R903,C903 ,Q102,R904,R905,C904 ,C905 Location and NO ASM,
EC-D-19	**26**	Layout issue, so Del D23, R436 location	Del D23 , R436 location,
EC-D-6	**09**	Del JTAG debug reserved circuit for un-used	change R183,R182,R524,R530,R529,R534,R169 from No ASM to Del location

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC RECORD B	1A
Date: Tuesday, January 04, 2011	Sheet 53 of 53	