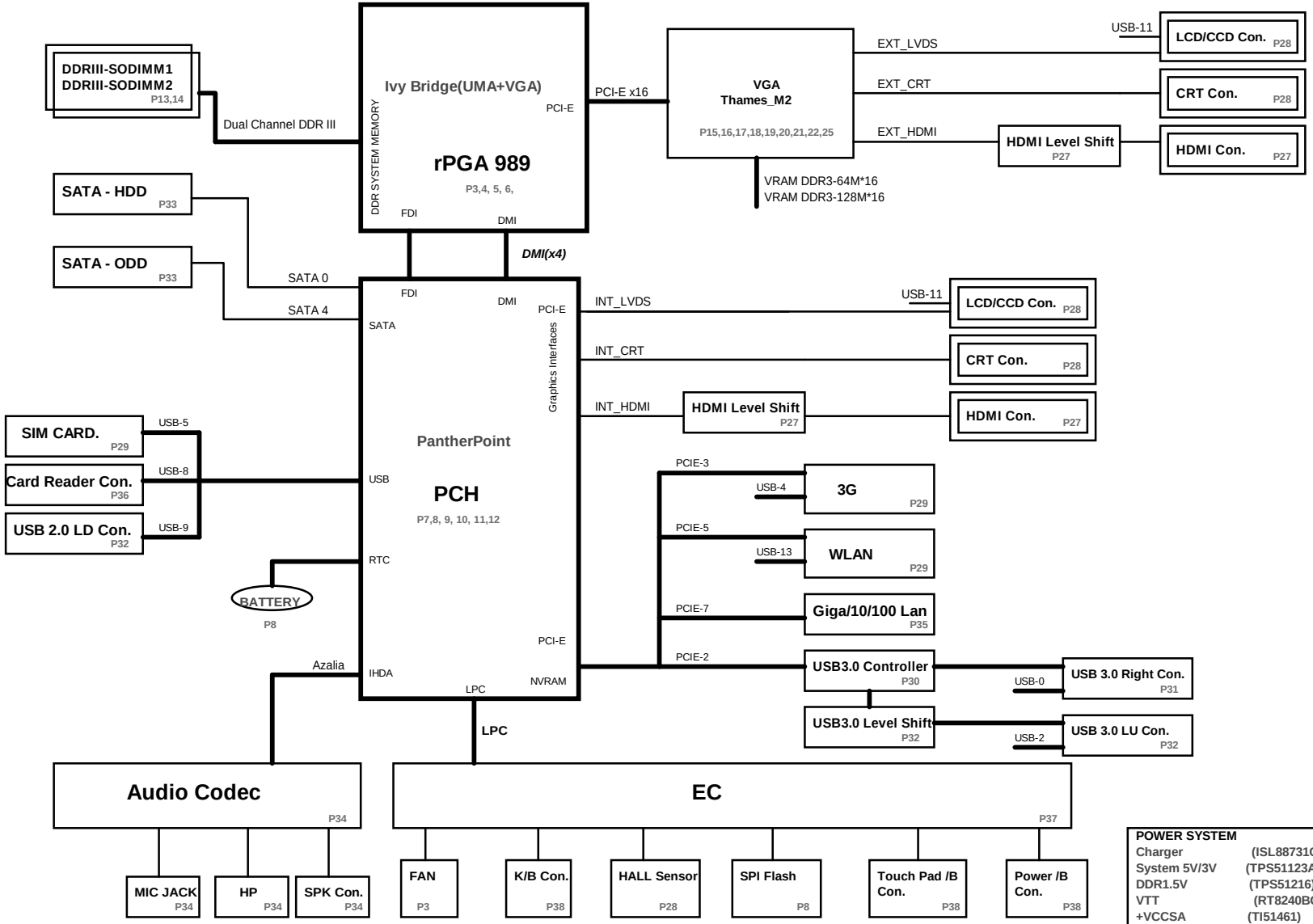
Chief River Block Diagram



POWER SYSTEM		
Charger	(ISL88731C)	P40
System 5V/3V	(TPS51123A)	P41
DDR1.5V	(TPS51216)	P42
VTT	(RT8240BGQW)	P43
+VCCSA	(TI51461)	P44
+VCORE+VGFX	(ISL95836)	P45
+1.8V	(G966A)	P46
AMD_GPU	(ISL95870A)	P47

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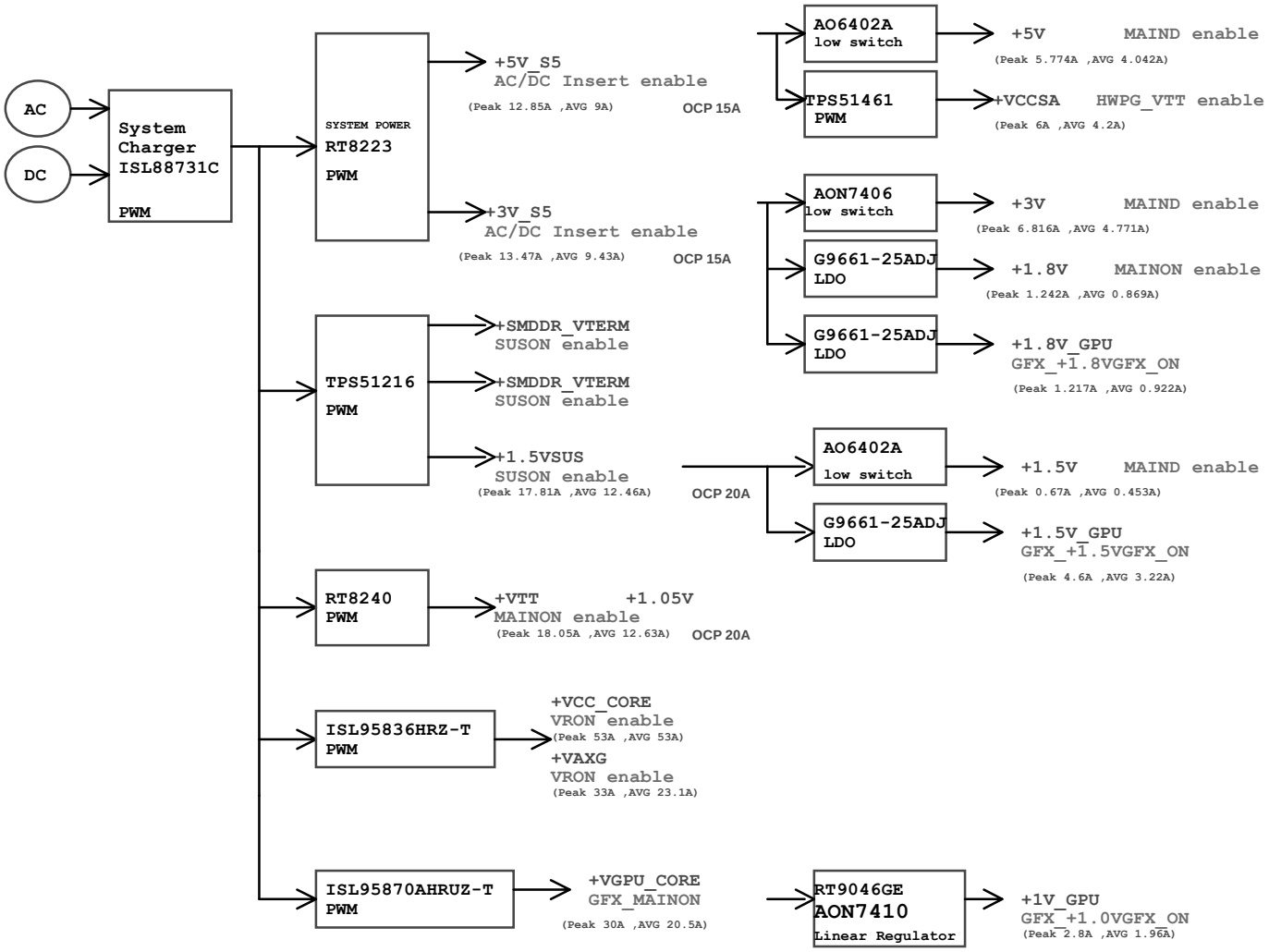
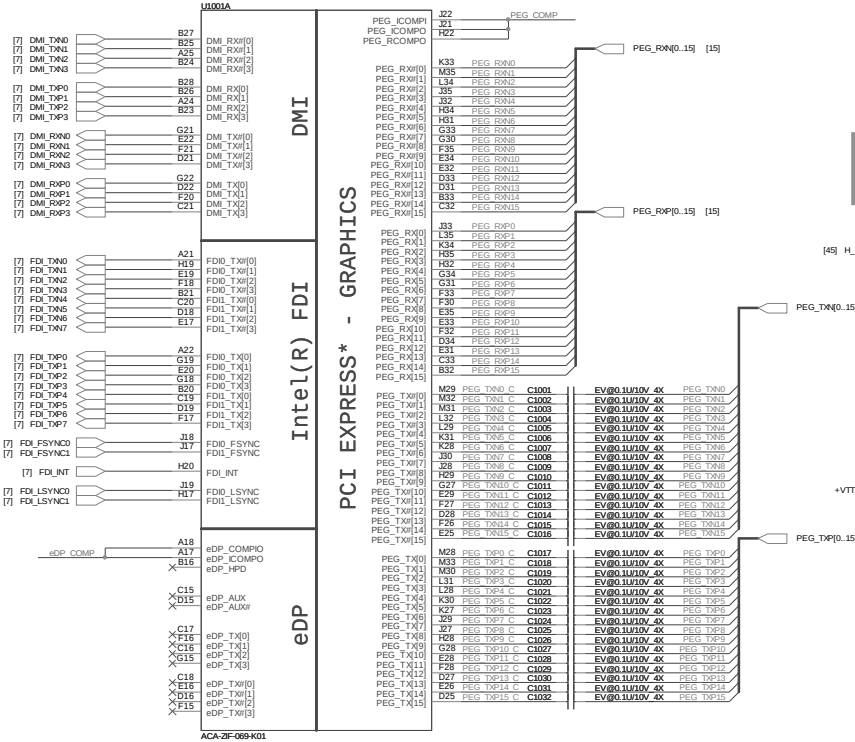
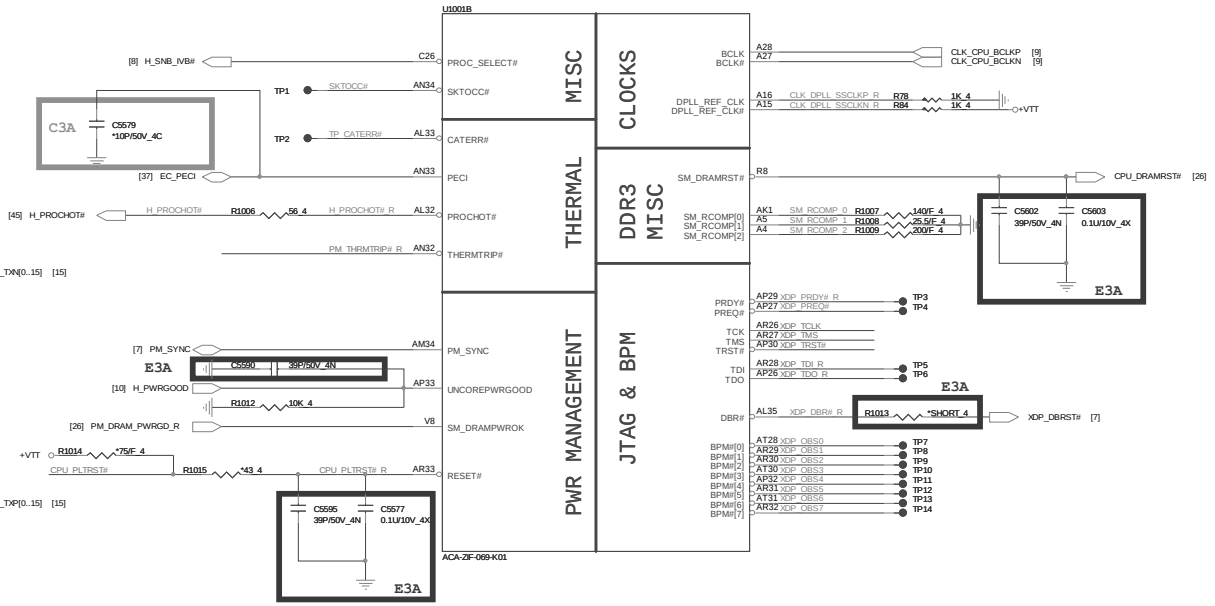


POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

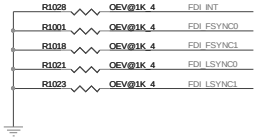
Ivy Bridge Processor (DMI,PEG,FDI) CPU/VGA



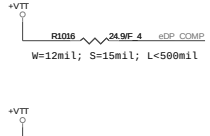
Ivy Bridge Processor (CLK,MISC,JTAG) CPU



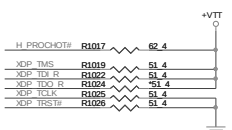
FDI Disabling (Discrete Only) OEV



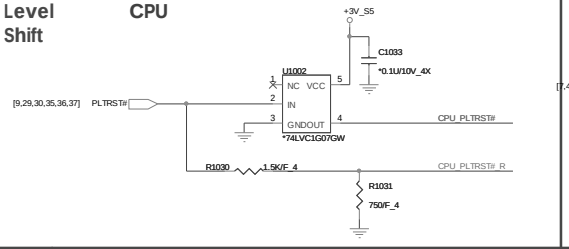
DP & PEG Compensation CPU



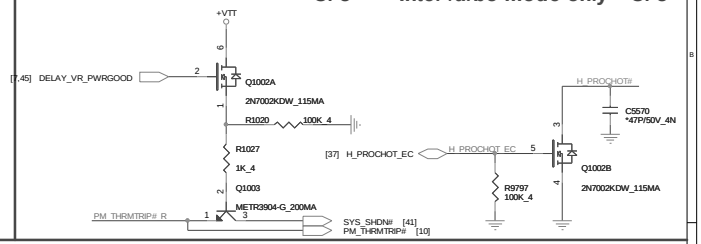
Processor pull-up CPU



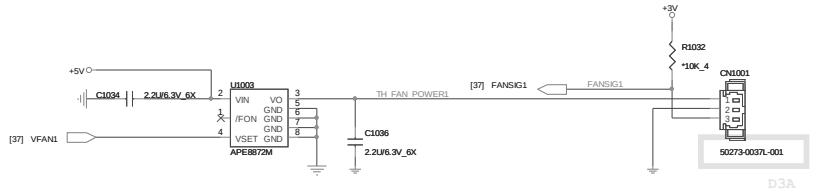
Level Shift CPU



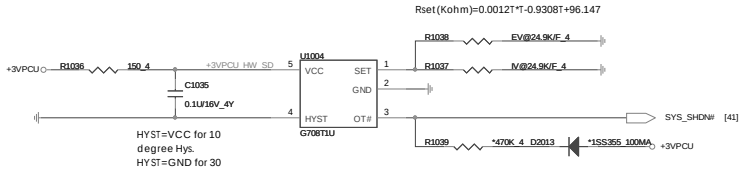
Thermal Trip & Process HOT CPU Intel Turbo mode only CPU



FAN Control-->For one FAN solution THC



CPU Thermal sensor / MB Local TEMP THP/UGA/VGA



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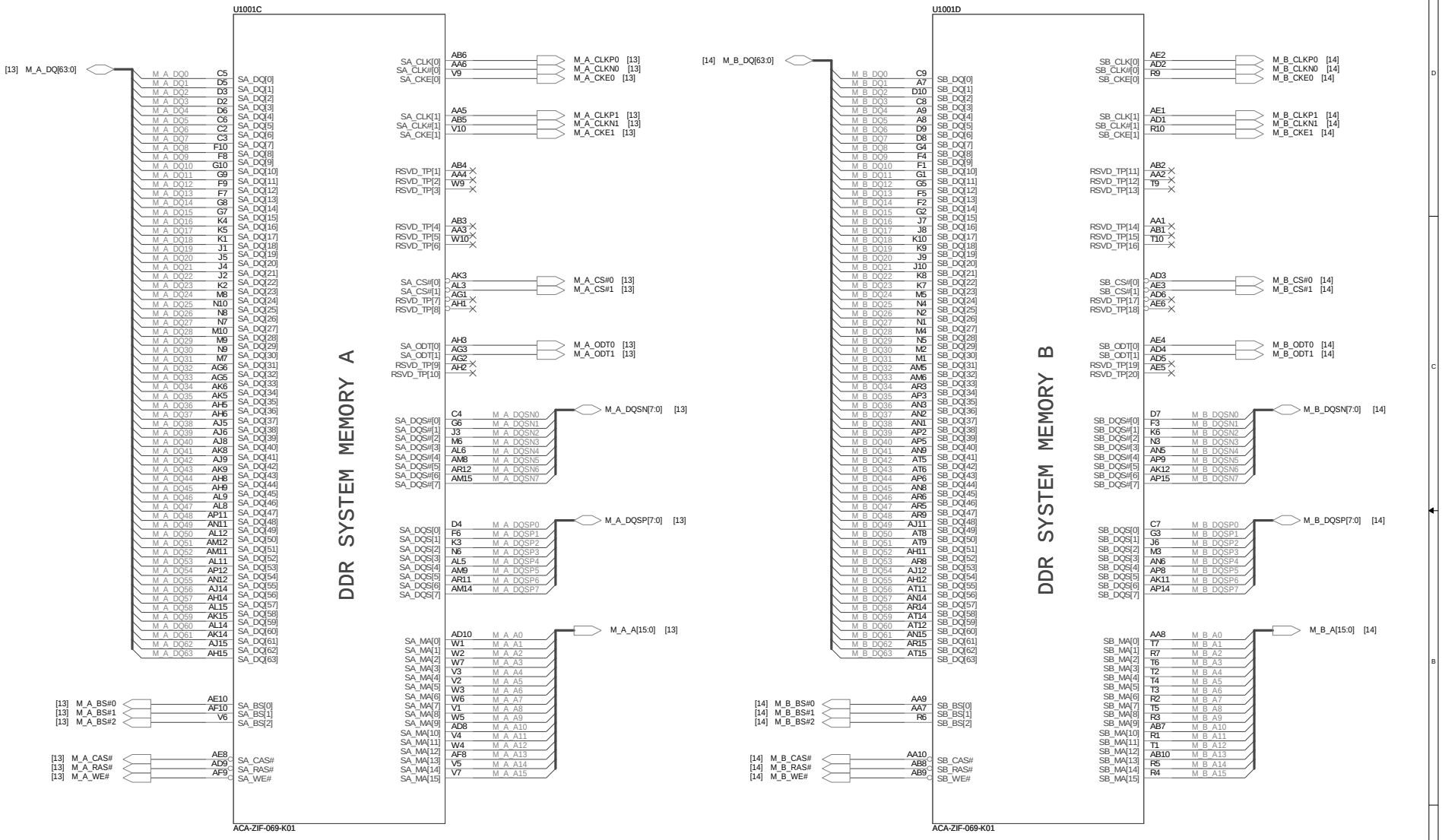
Ivy Bridge Processor (DDR3)CPU

04



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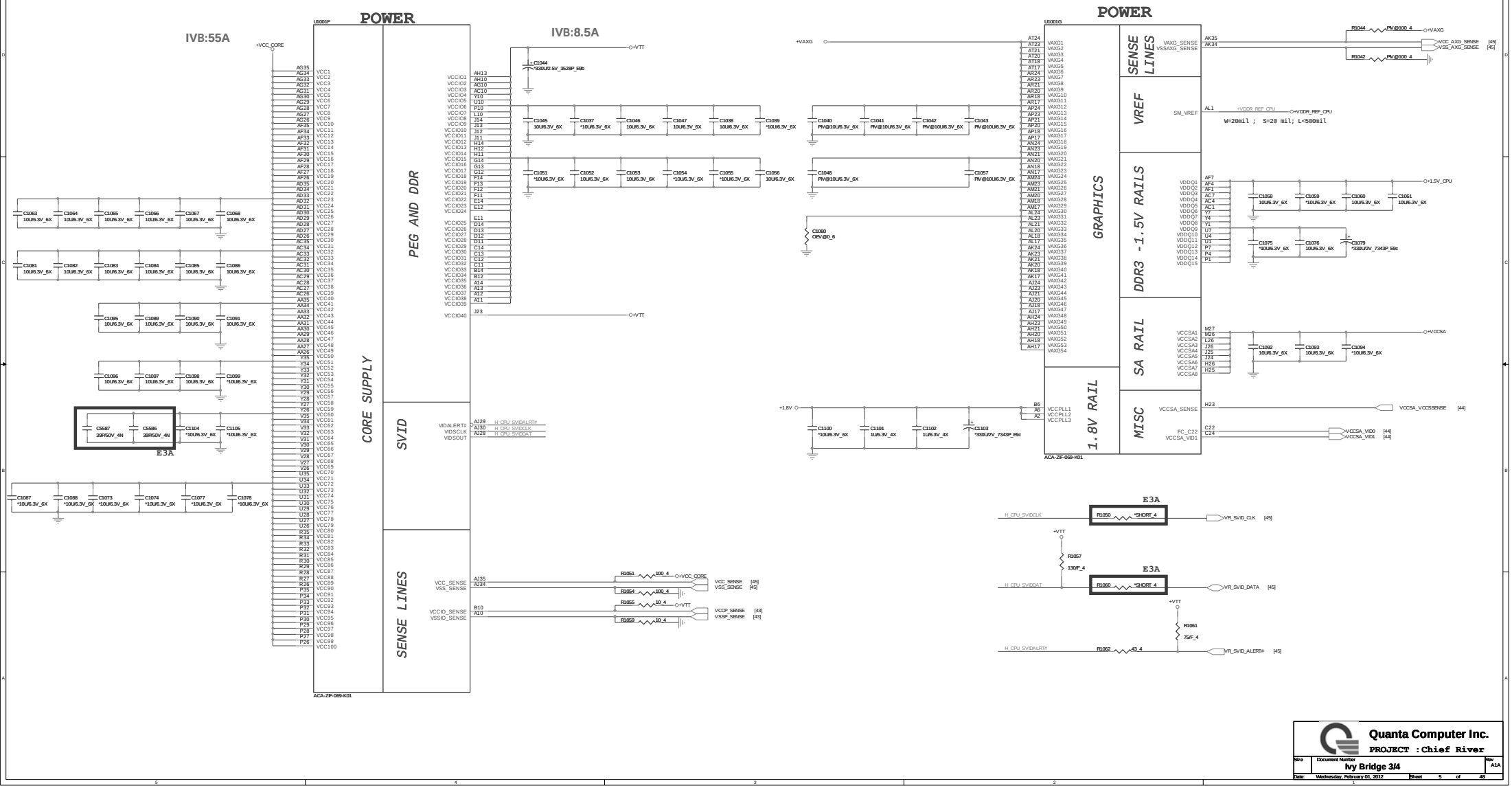
Ivy Bridge Processor (POWER) CPU

Ivy Bridge Processor (GRAPHIC POWER) CPU/OEV/PIV



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	Ivy Bridge 3/4	A1A
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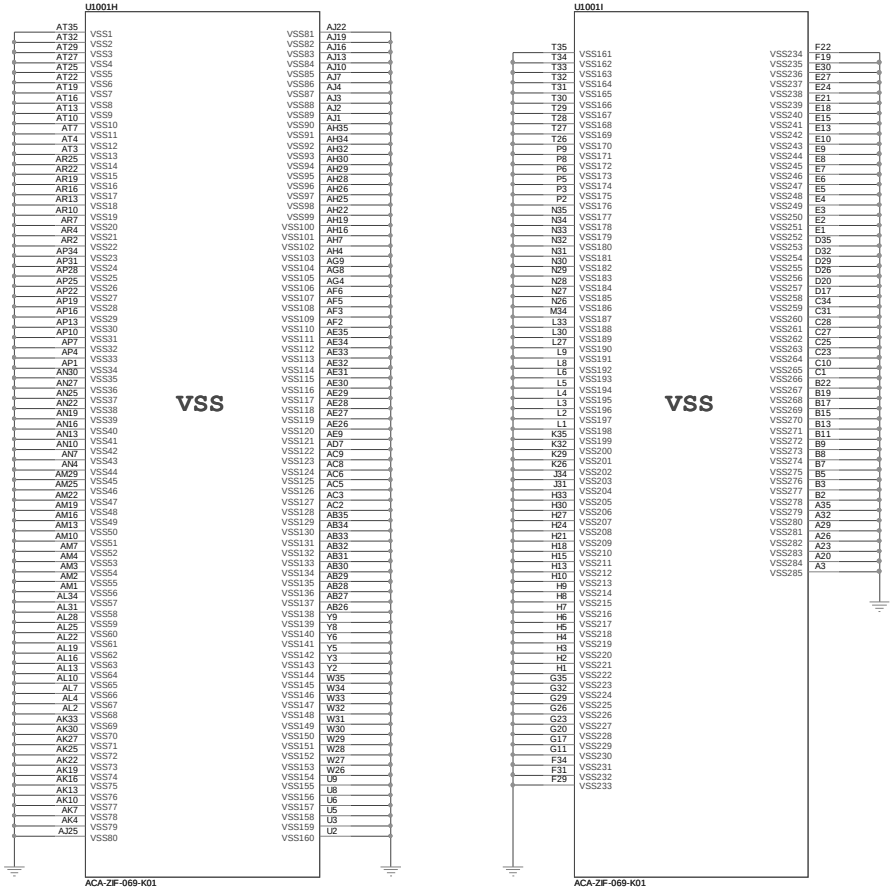
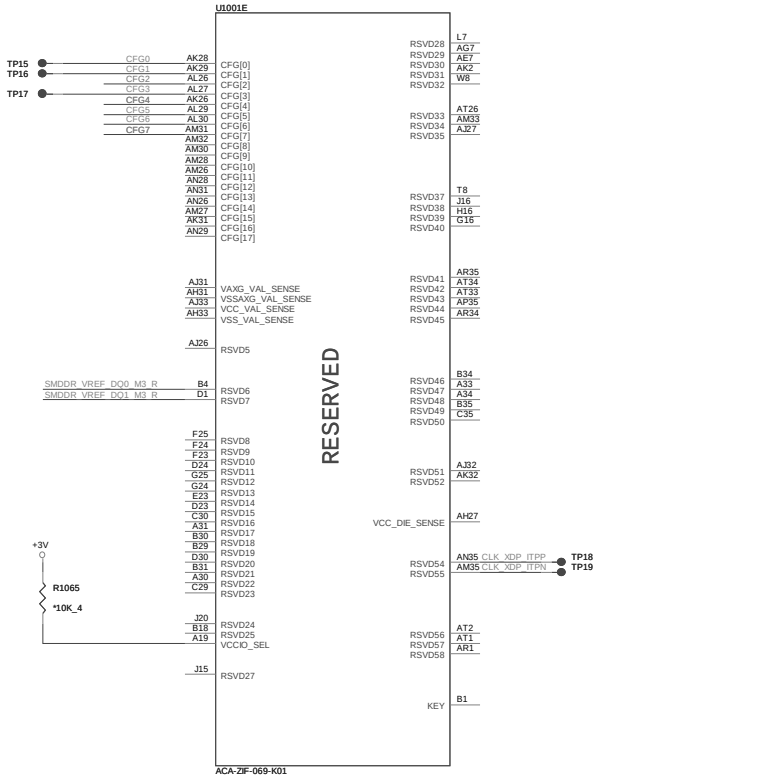
Ivy Bridge Processor (GND) CPU



Ivy Bridge Processor (RESERVED, CFG) CPU

06

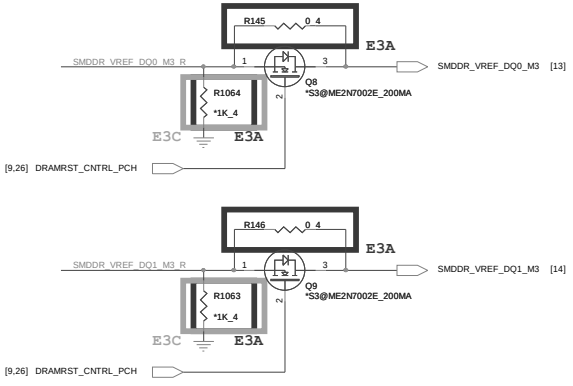


Processor Strapping CPU/VGA

The CFG signals have a default value of '1' if not terminated on the board.

Pin Name	Configuration	
CFG2 (PEG Static Lane Reversal --> 16 Lane)	1=Normal Operation 0=Lane Reversed	CFG2 R118 EV@1K_4
CFG3 (Reserved)		
CFG4 (DP Presence Strap)	1=Disable; No physical DP attached to eDP 0=Enable; An ext DP device is connected to eDP	CFG4 R117 *1K_4
CFG5 CFG6 (PCIE Bifurction)	00=x8,x4,x4 - Device 1 function 1 and 2 enable 01=Reserved - (Device 1 function 1 disable ; function 2 enable) 10=x8,x8 -Device 1 function 1 enable ; function 2 enable 11=(Default) x16 -Device 1 function 1 and 2 disable	CFG5 R104 *1K_4 CFG6 R116 *1K_4
CFG7 (PEG Defer Training)	1=PEG train immediately following xxRESETB de assertion 0=PEG wait for BIOS training	CFG7 R115 *1K_4

DDR3 VREF DQ (M3) S3P



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	Ivy Bridge 4/4	A1A

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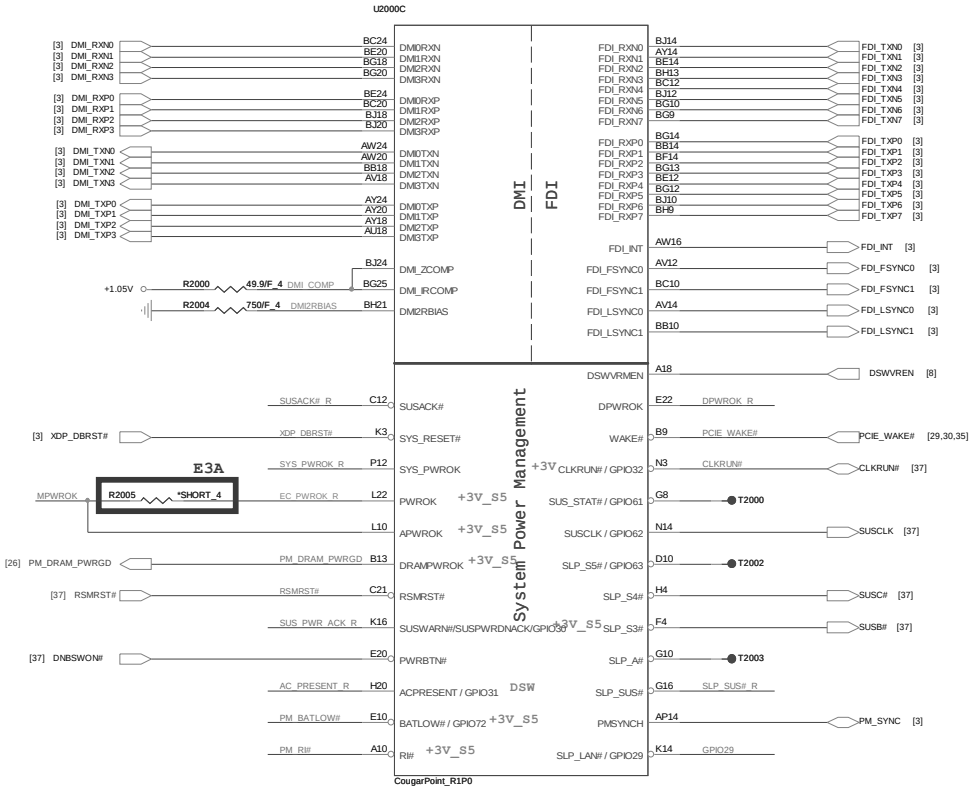
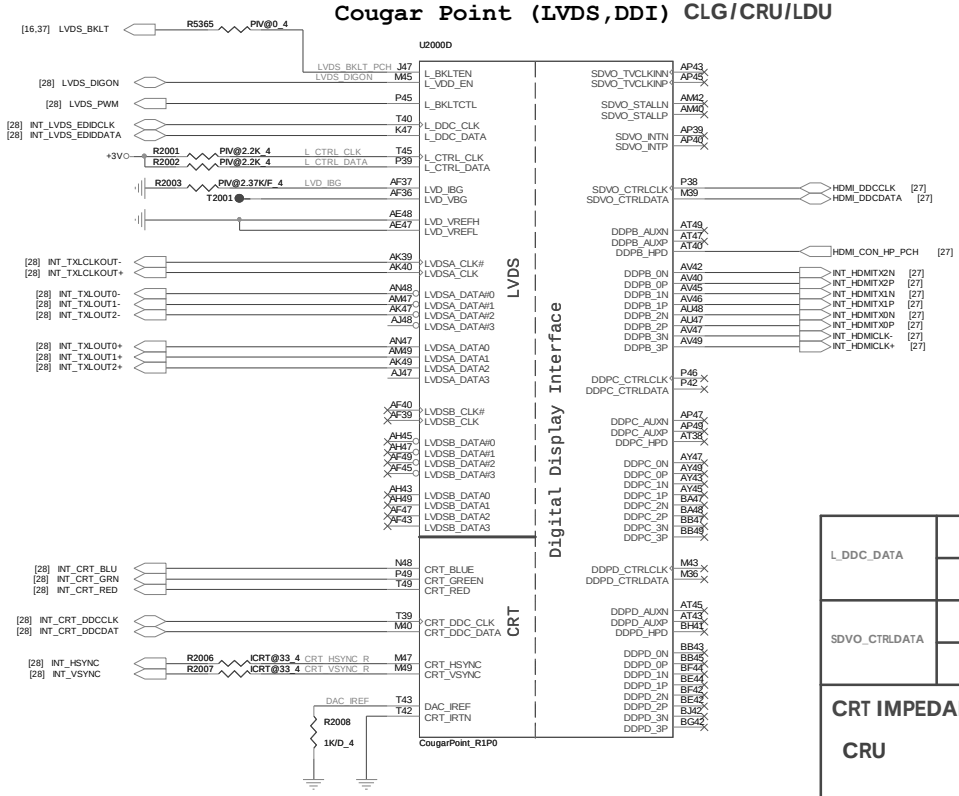
Cougar Point (DMI,FDI,PM) CLG



Cougar Point (LVDS,DDI) CLG/CRU/LDU

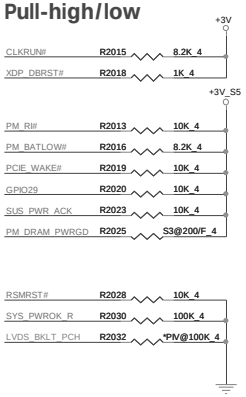


L_DDC_DATA	1 -- LVDS ENABLE
	0 -- LVDS DISABLE
SDVO_CTRLDATA	1 -- PORT B Detected
	0 -- PORT B Disable

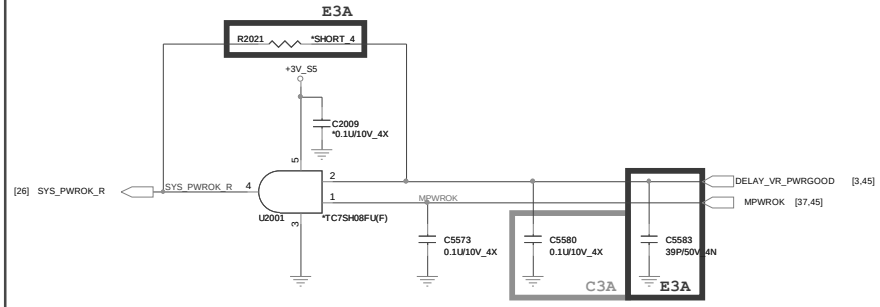
CRT IMPEDANCE MATCHING

CRU

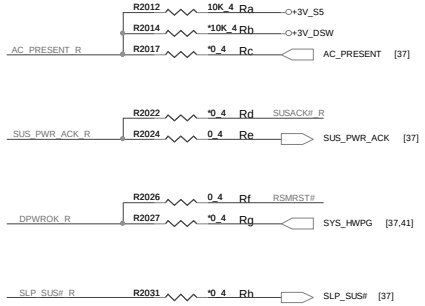
PCH Pull-high/low CLG/PIV/S3P



System PWR_OK CLG



Deep Sx CLG



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

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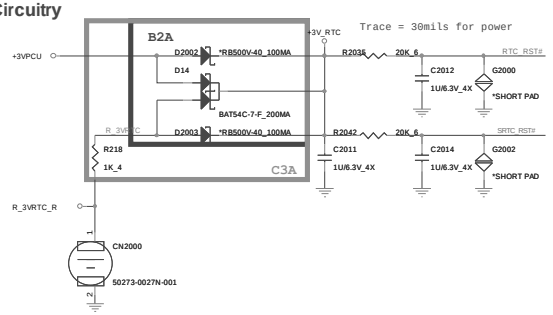
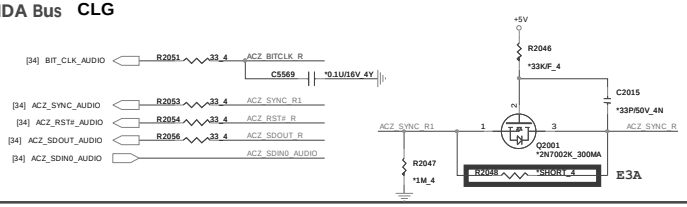
RTC Circuitry

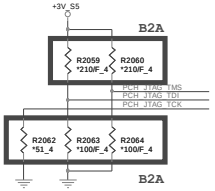


PU & Password Clear CLG

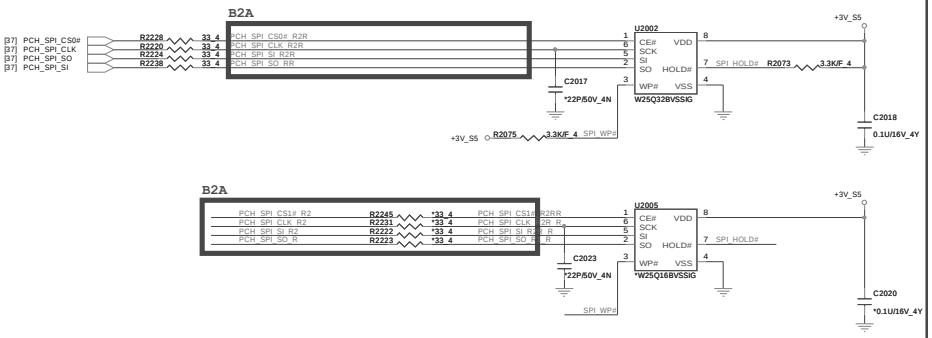
HDA Bus CLG



PCH JTAG Debug DEG

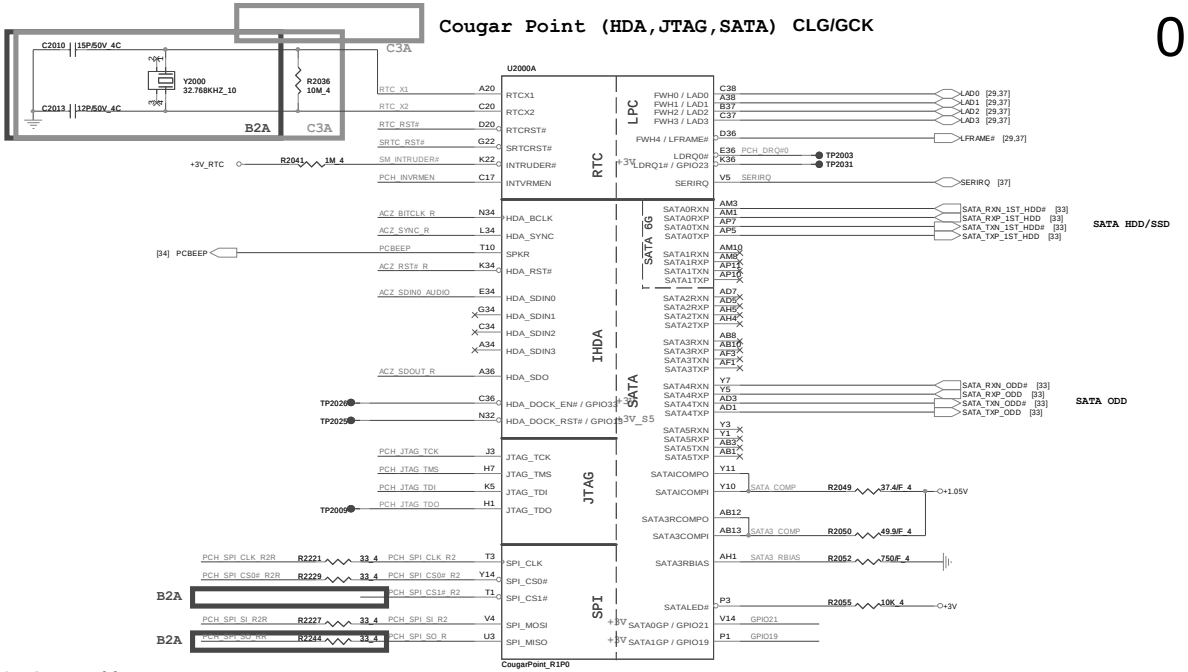


PCH Dual SPI CLG



Cougar Point (HDA,JTAG,SATA) CLG/GCK

08



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	**RSMRST**	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	**DMI/FDI Termination voltage**	**PWROK**	**0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	**On-Die PLL VR Voltage Select**	**RSMRST**	**0 = Support by 1.8V (weak pull-down)** **1= Support by 1.5V**
INIT3_3V#	**Reserved**	PWROK	1 = Default (weak pull-up 20K)
GNT2#/ GPIO53	**ESI Strap (Server Only)**	PWROK	1 = Default. Should not be pulled low for desktop and mobile
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected
SATA3GP/ GPIO37	**Reserved**	PWROK	0 = Default
SATA2GP/ GPIO36	**Reserved**	PWROK	0 = Default
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable

Pin Name	Configuration
SPKR	+3VO R2057 *1K_4 PCBEEP
GNT3# / GPIO55	R2058 *1K_4 PCI_GNT3# [9]
INTVRMEN	+3V_RTC R2061 330K_4 PCH_INVRMEN
GNT1# / GPIO51	R2065 *1K_4 GNT1# [9]
GPIO19	R2066 *1K_4 GPIO19
HDA_SDO	+3V_S5 R2067 *1K_4 ACZ_SDOUT_R ACZ_SDOUT_R [37]
DF_TVS	R2068 2.2K_4 +1.8V R2069 1K_4 DF_TVS [10] H_SNB_IVB# [3]
GPIO28	+3V_S5 R2070 *10K_4 R2071 *1K_4 PLL_ODVR_EN [10]
HDA_SYNC	+3V_S5 R2072 1K_4 ACZ_SYNC_R
INIT3_3V#	**Should not pull low. leave as No Connect**
GNT2#/ GPIO53	**Should not pull low for desktop and mobile**
GPIO15	+3V_S5 R2074 1K_4 GPIO15 [10]
L_DDC_DATA	1= PU to 3V
SDVO_CTRLDATA	1= PU to 3V
DDPC_CTRLDATA	0=NC
DDPD_CTRLDATA	0=NC
SATA3GP/ GPIO37	**Should not be pulled high when strap is sampled**
SATA2GP/ GPIO36	**Should not be pulled high when strap is sampled**
DSWVRMEN	DSWVREN [7] +3V_RTC R2076 330K_4 R2077 *330K_4

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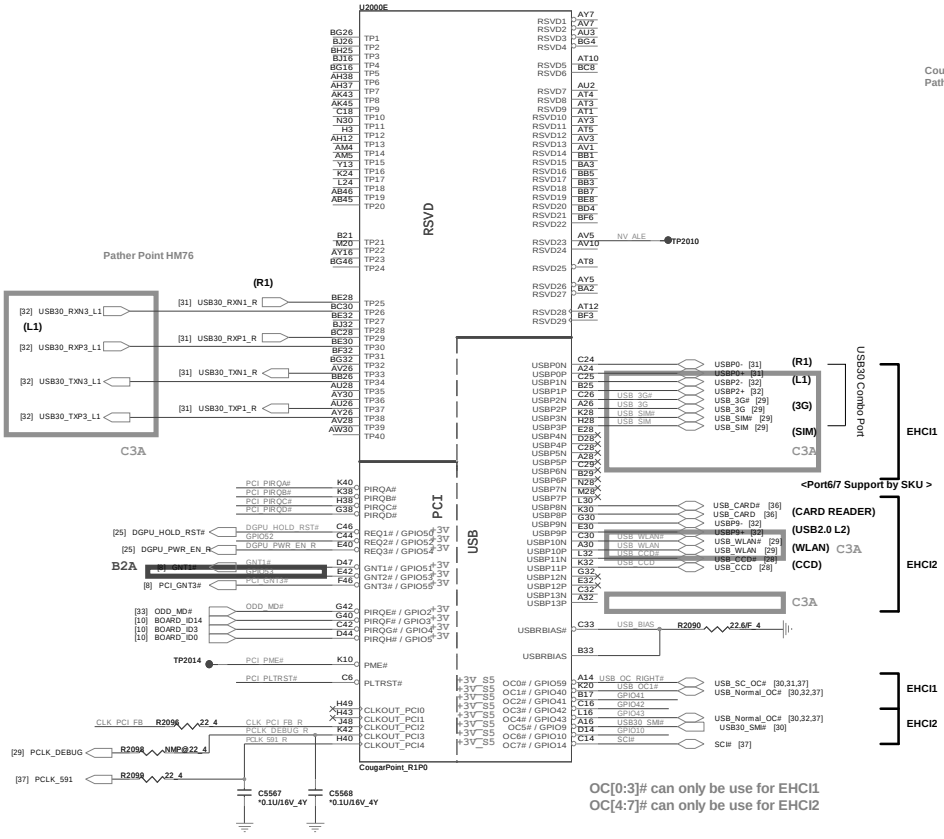
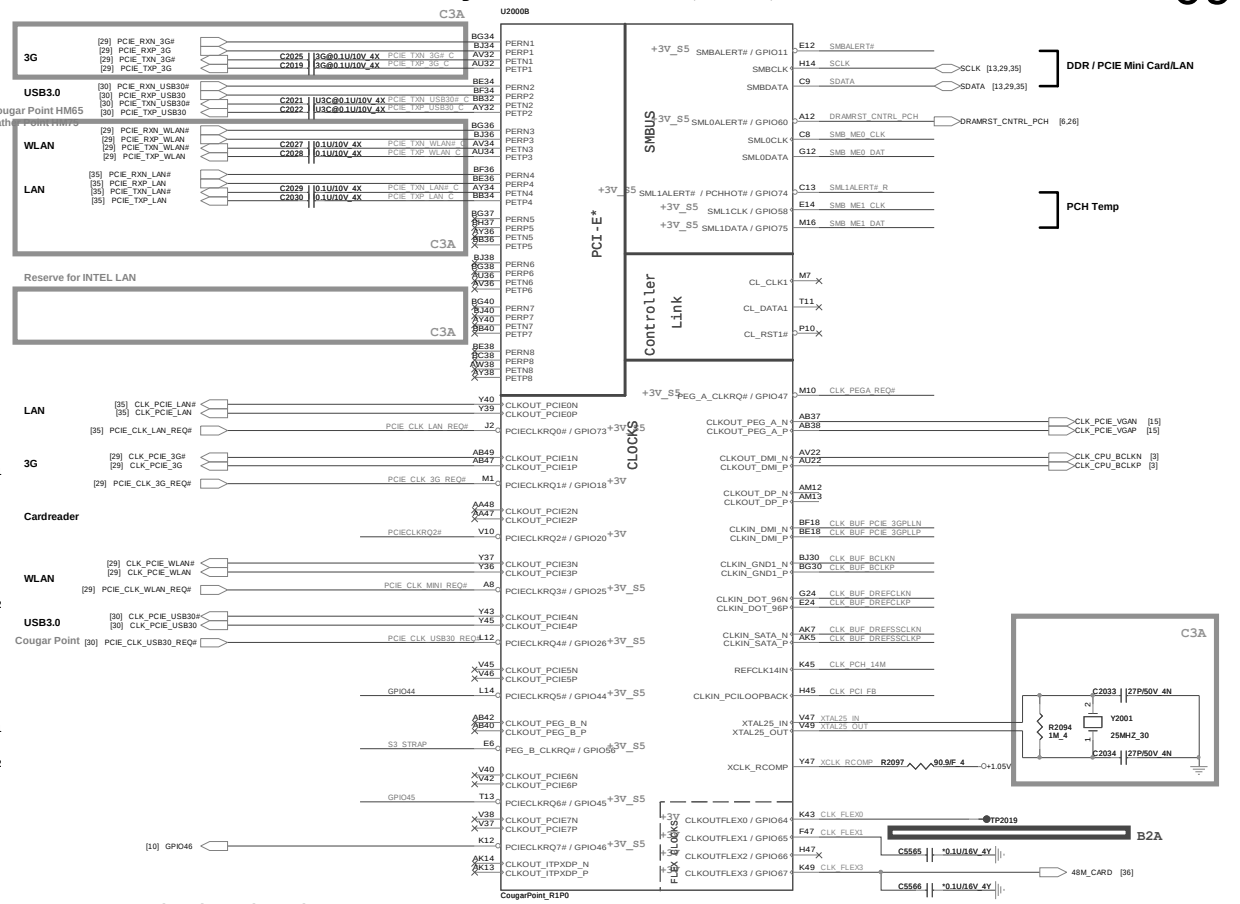
Cougar Point-M (PCI,USB,NVRAM) CLG/DEG

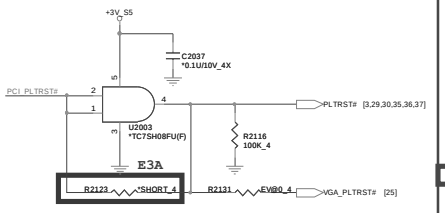


Cougar Point-M (PCI-E,SMBUS,CLK)CLG/GCK/MNG/U3C

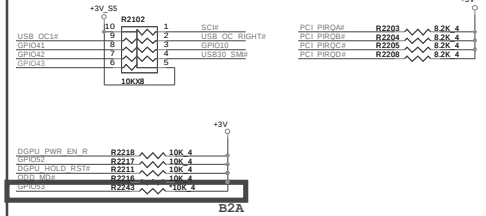


CLG/S3P/NS3P/VGA/UGA

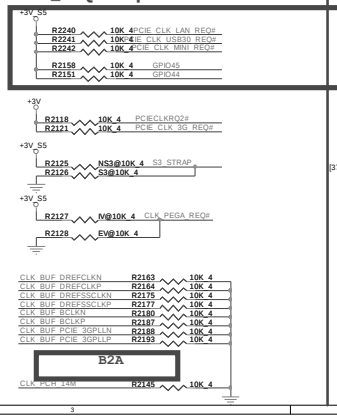
PLTRST# CLG



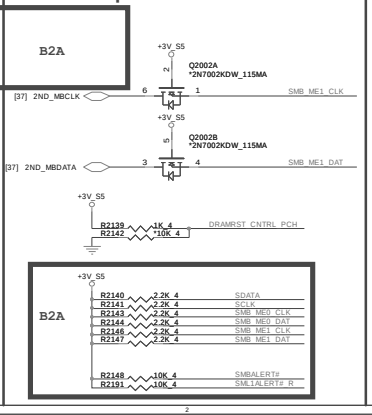
PCI/USBOC# Pull-up CLG



CLK_REQ/Strap Pin



SMBus/Pull-up CLG



	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0	●	●	●	●	
CLK_FLEX1		●	●	●	
CLK_FLEX2	●	●	●	●	●
CLK_FLEX3		●	●	●	

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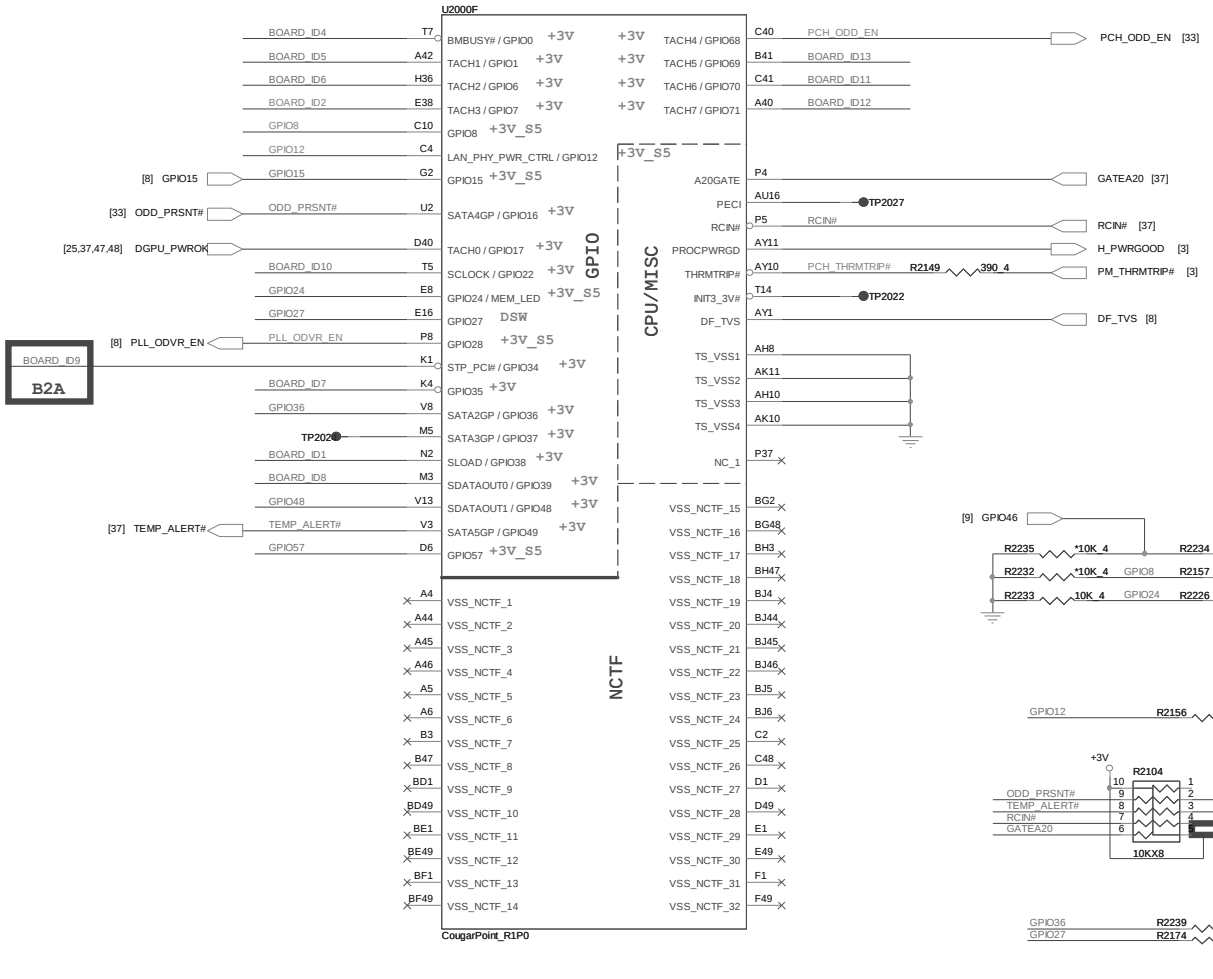
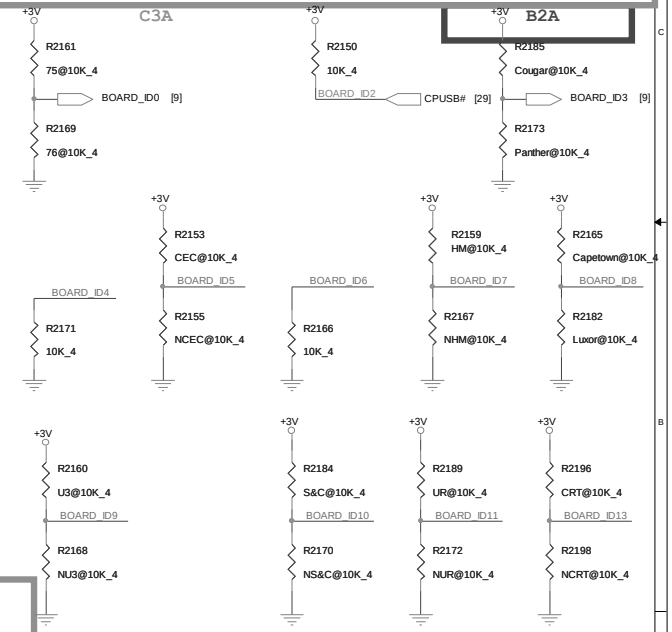
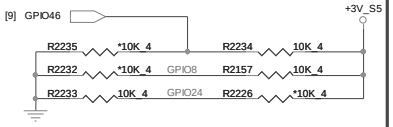
Cougar Point (GPIO,VSS_NCTF,RSVD) CLG

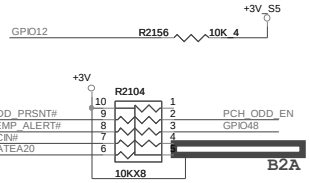


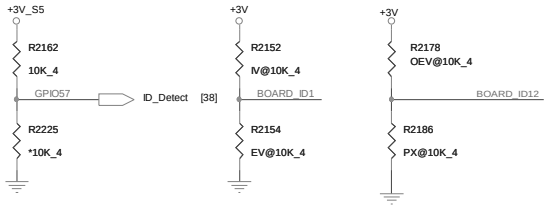
BOARD ID SETTING CLG/PX/OEV/UGA/CLG-Strap

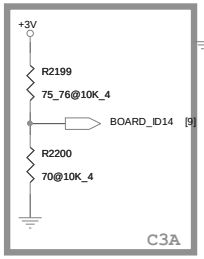
Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID12	ID13	ID14
HM75 HM76	H L											
UMA SKU VGA SKU		H L										
W/O 3G W/ 3G			H L									
HuronRiver ChiefRiver				H L								
13" 14"					H L							
W/ CEC W/O CEC						H L						
W/ G-sensor W/O G-sensor							H L					
W/ HDMI W/O HDMI								H L				
Capetown Luxor									H L			
Only VGA PX mode										H L		
W/ CRT W/O CRT											H L	
HM75_76 HM70												H L











ID_Detect	default
Metal/IMR	H
TEXTURE	L

	Description	ID9	ID10	ID11
NU3@/NSC@/NUR@	ULU-2 and W/O R-USB Port	L	L	L
NU3@/NSC@/UR@	ULU-2 and W/O S&C UR-2	L	L	H
U3@/NSC@/UR@	ULU-2 and W/O S&C UR-3	H	L	H
NU3@/SC@/UR@	ULU-2 and W/S&C UR-2	L	H	H
U3@/SC@/UR@	ULU-3 and W/S&C UR-3	H	H	H

U3@ S&C@ UR@
NU3@ NS&C@ NUR@

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	Cougar Point 4/6	A1A
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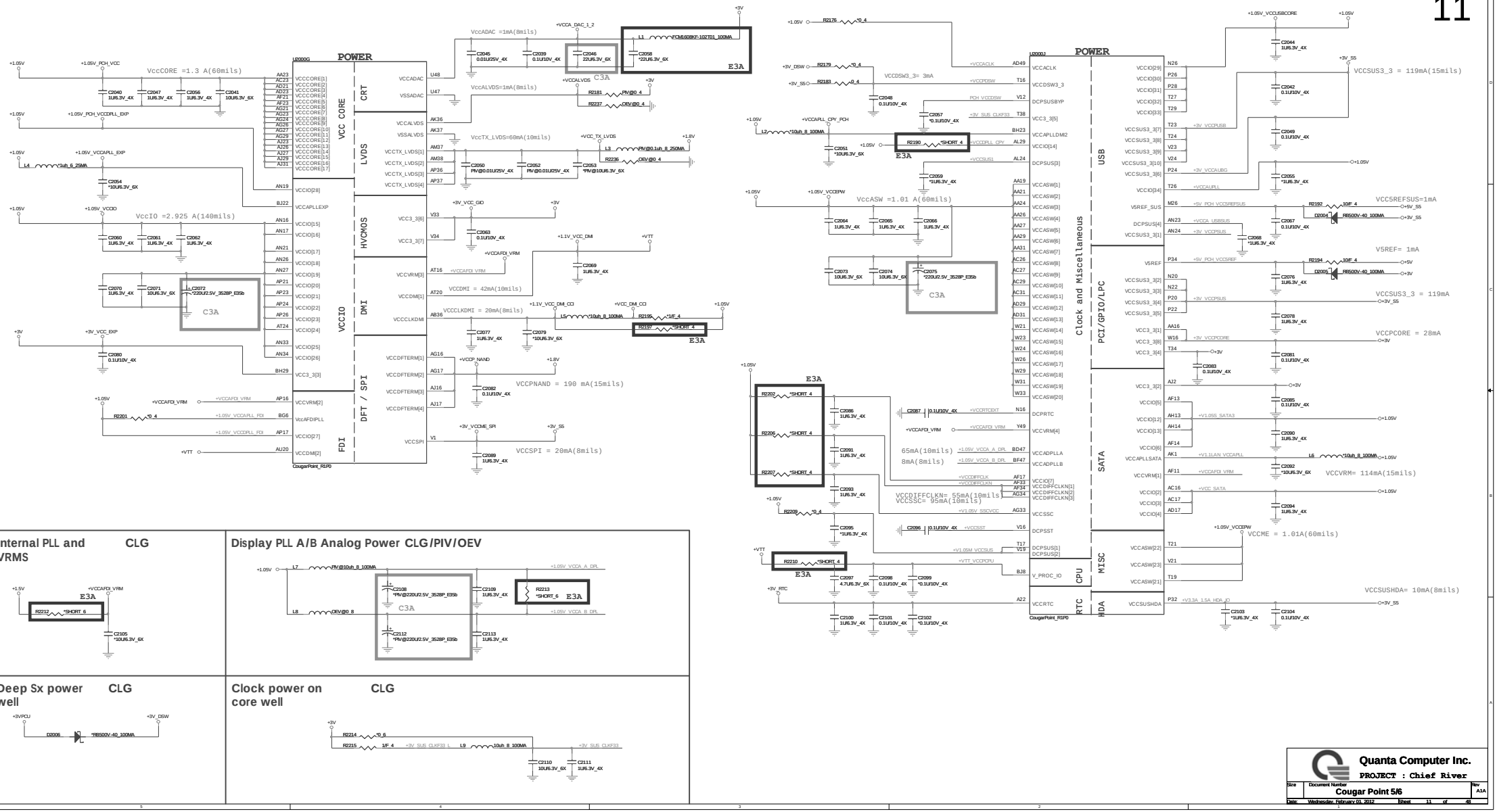

Internal PLL and VRMS CLG

Display PLL A/B Analog Power CLG/PIV/OEV

Deep Sx power well CLG

Clock power on core well CLG

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	Cougar Point 5/6	A1A

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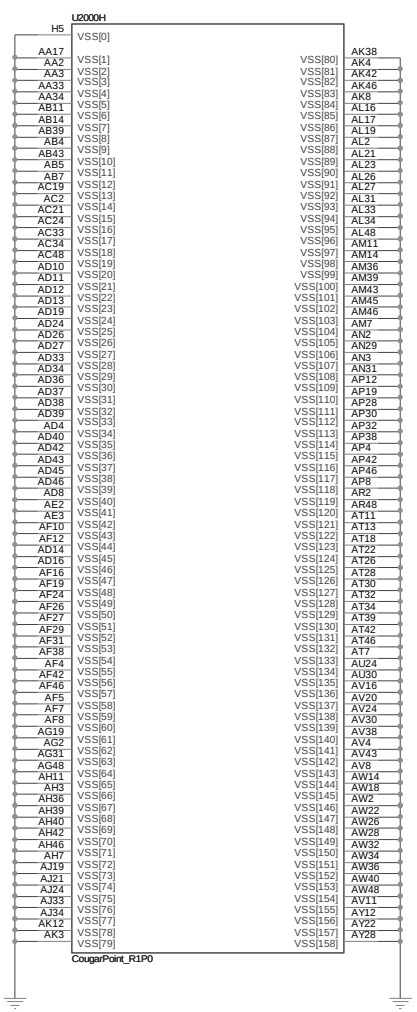

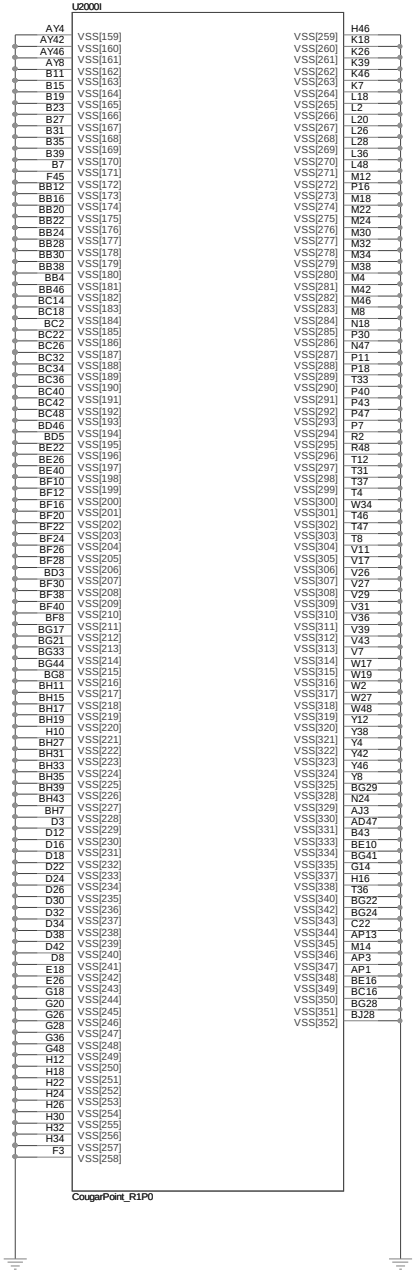

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PROJECT : Chief River

Size	Document Number	Rev
	Cougar Point 6/6	A1A
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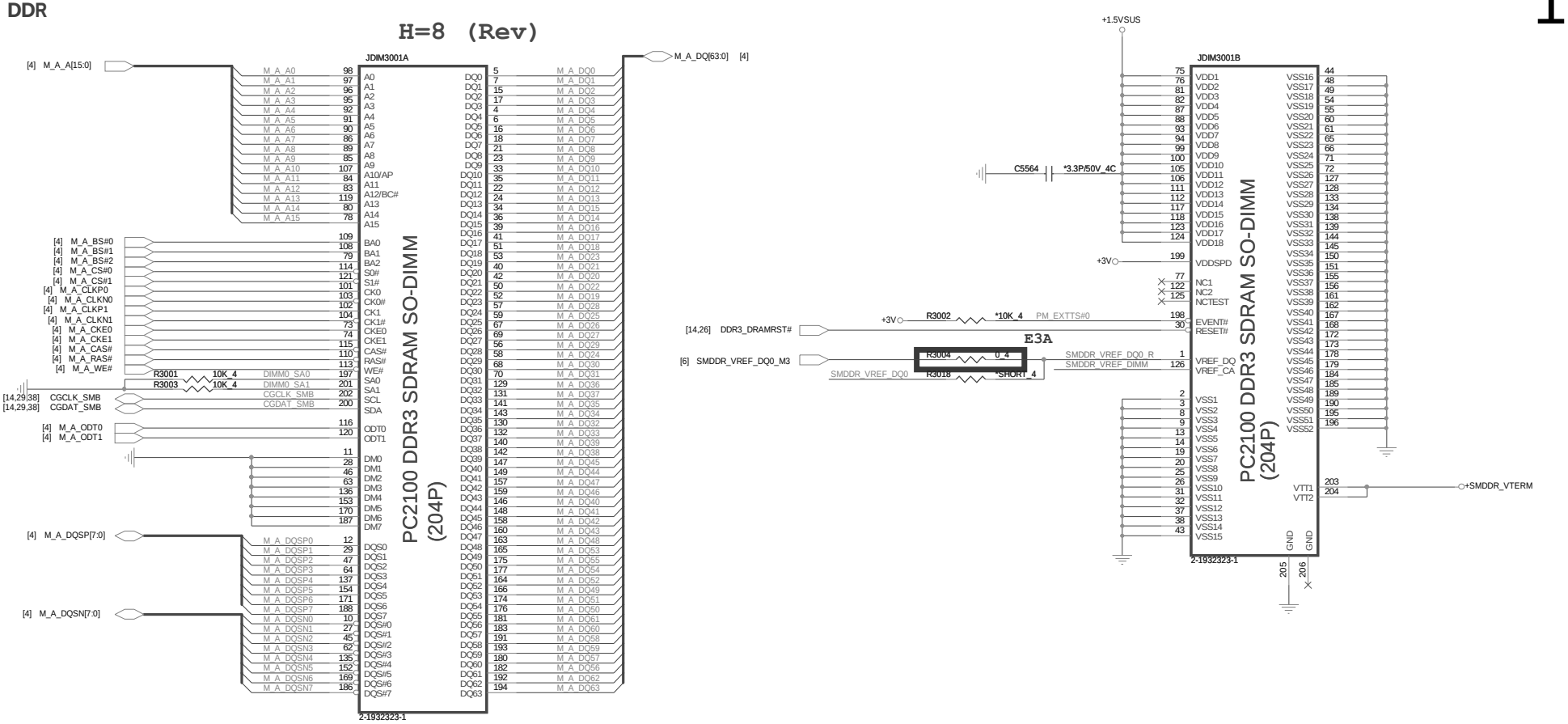
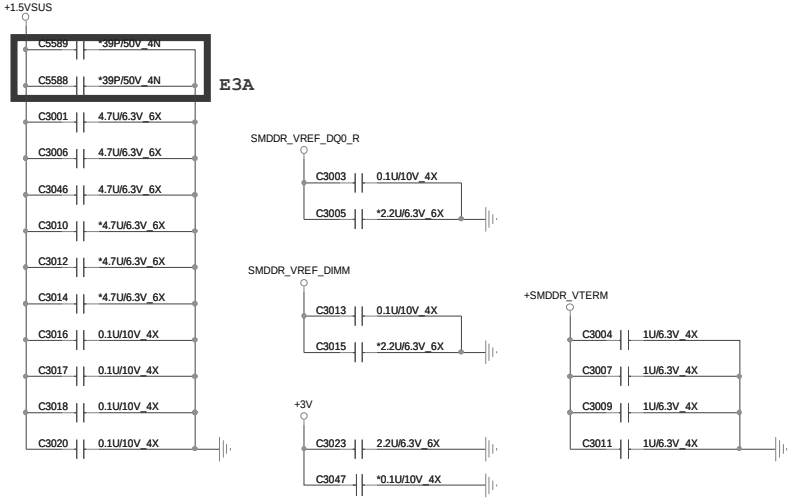
DDR

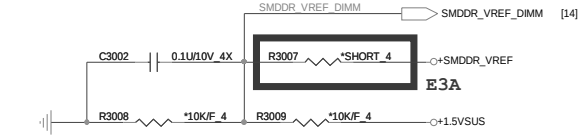
H=8 (Rev)



DDR Power Decoupling DDR

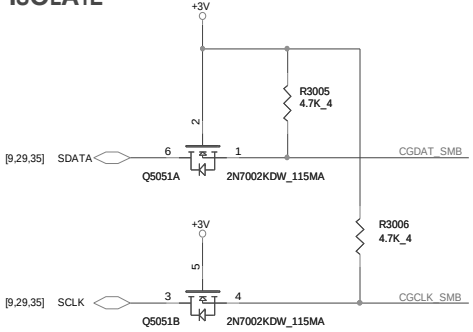


DDR3 VREF CA DDR



DDR3 VREF DQ (M1) DDR

SMBUS ISOLATE DDR



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Size	Document Number	Rev
	DDR3 DIMM-0	A1A

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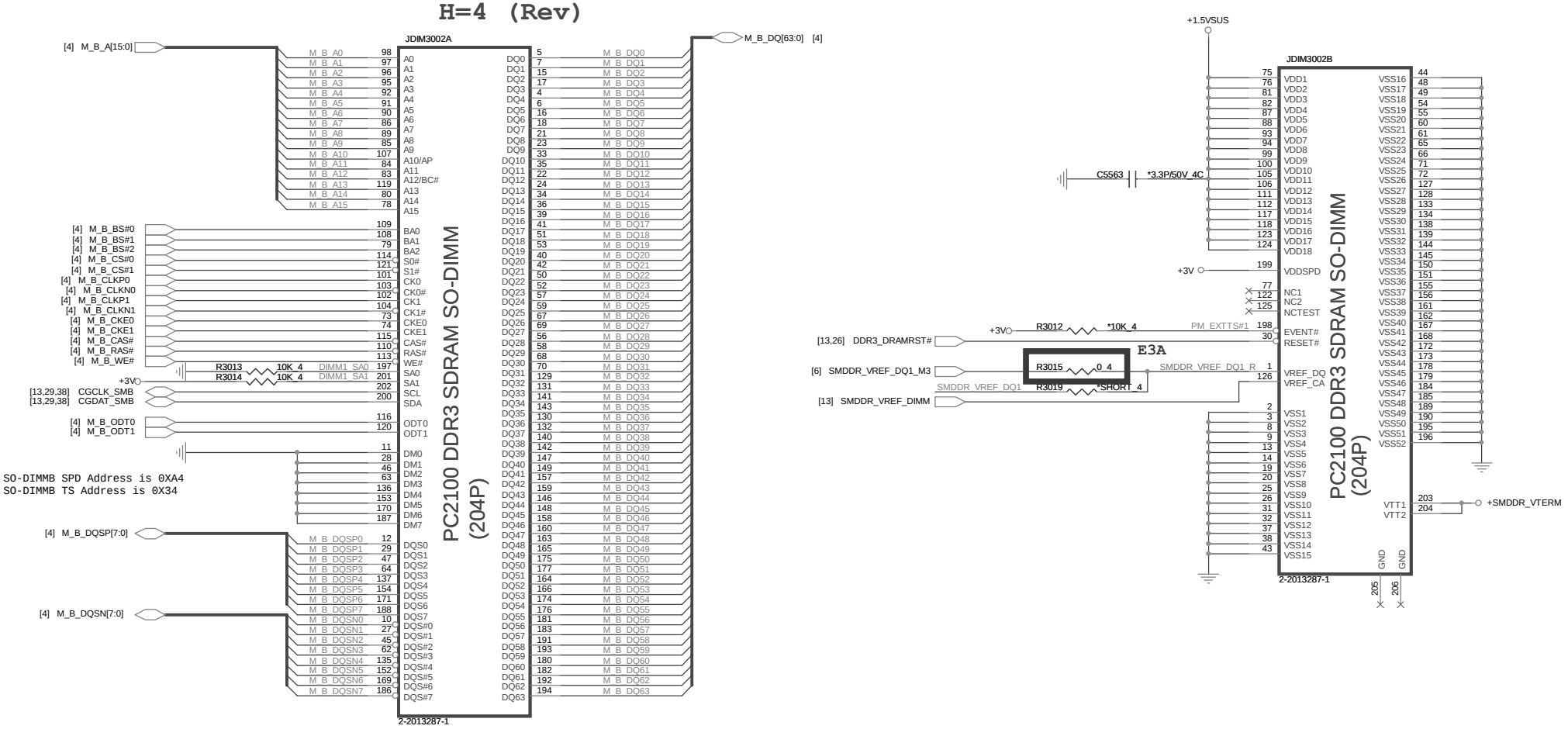
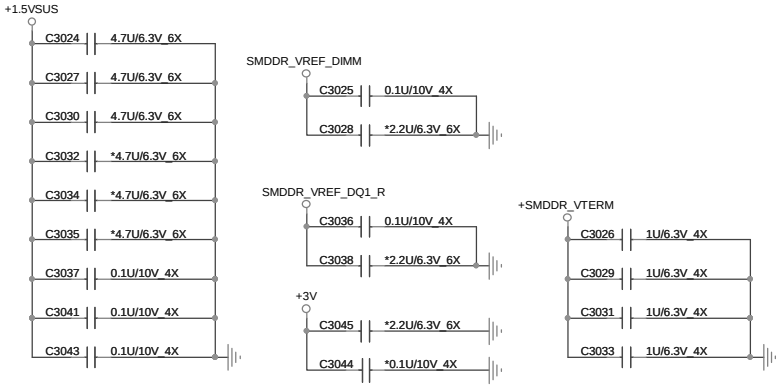
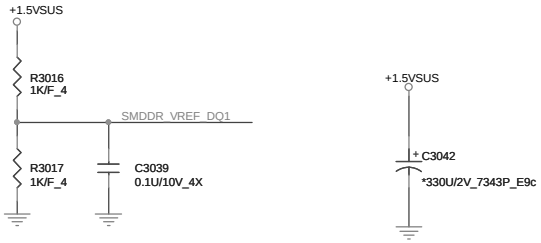
H=4 (Rev)



DDR Power Decoupling DDR



DDR3 VREF DQ (M1) DDR



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	DDR3 DIMM-1	A1A

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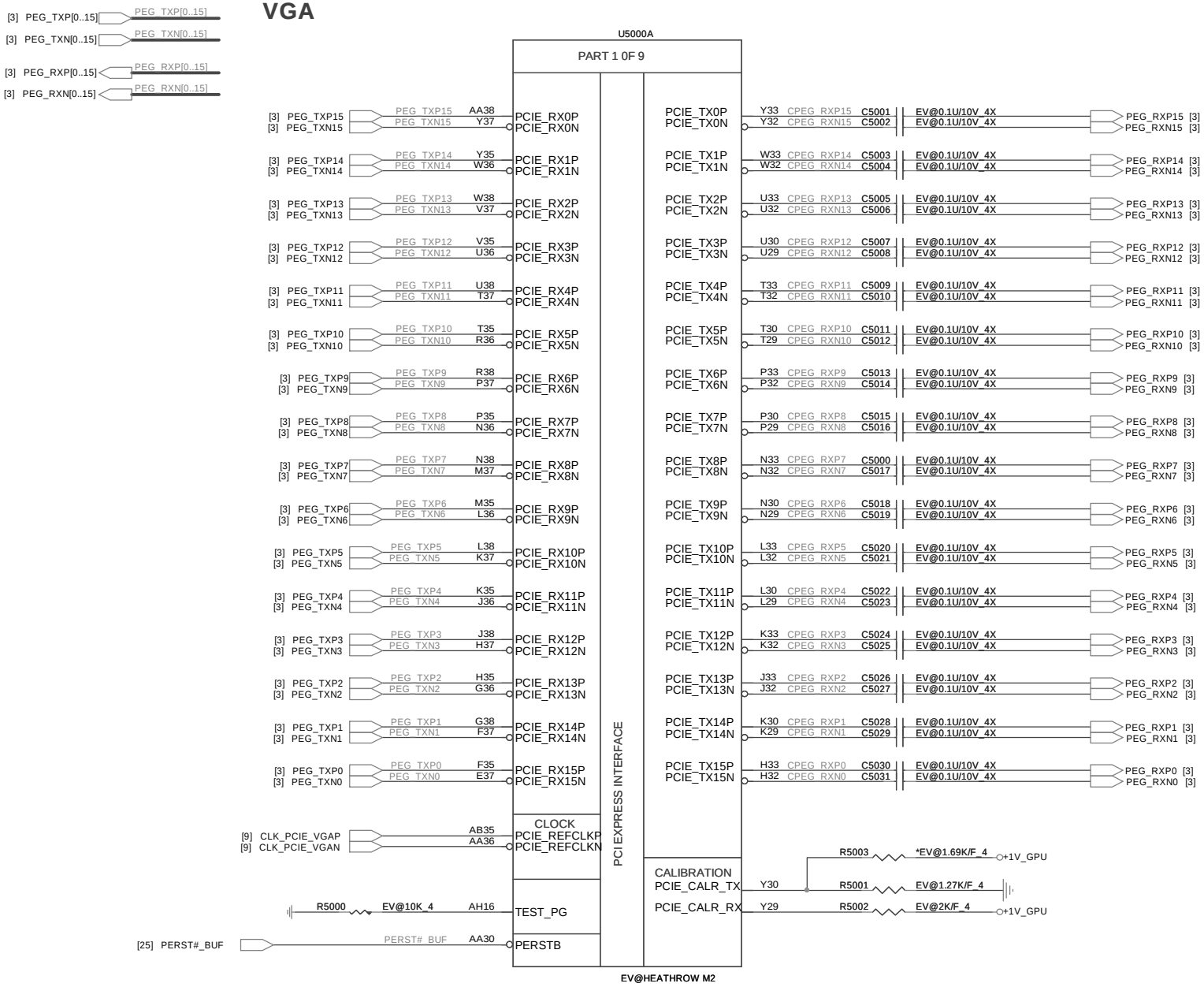
VGA

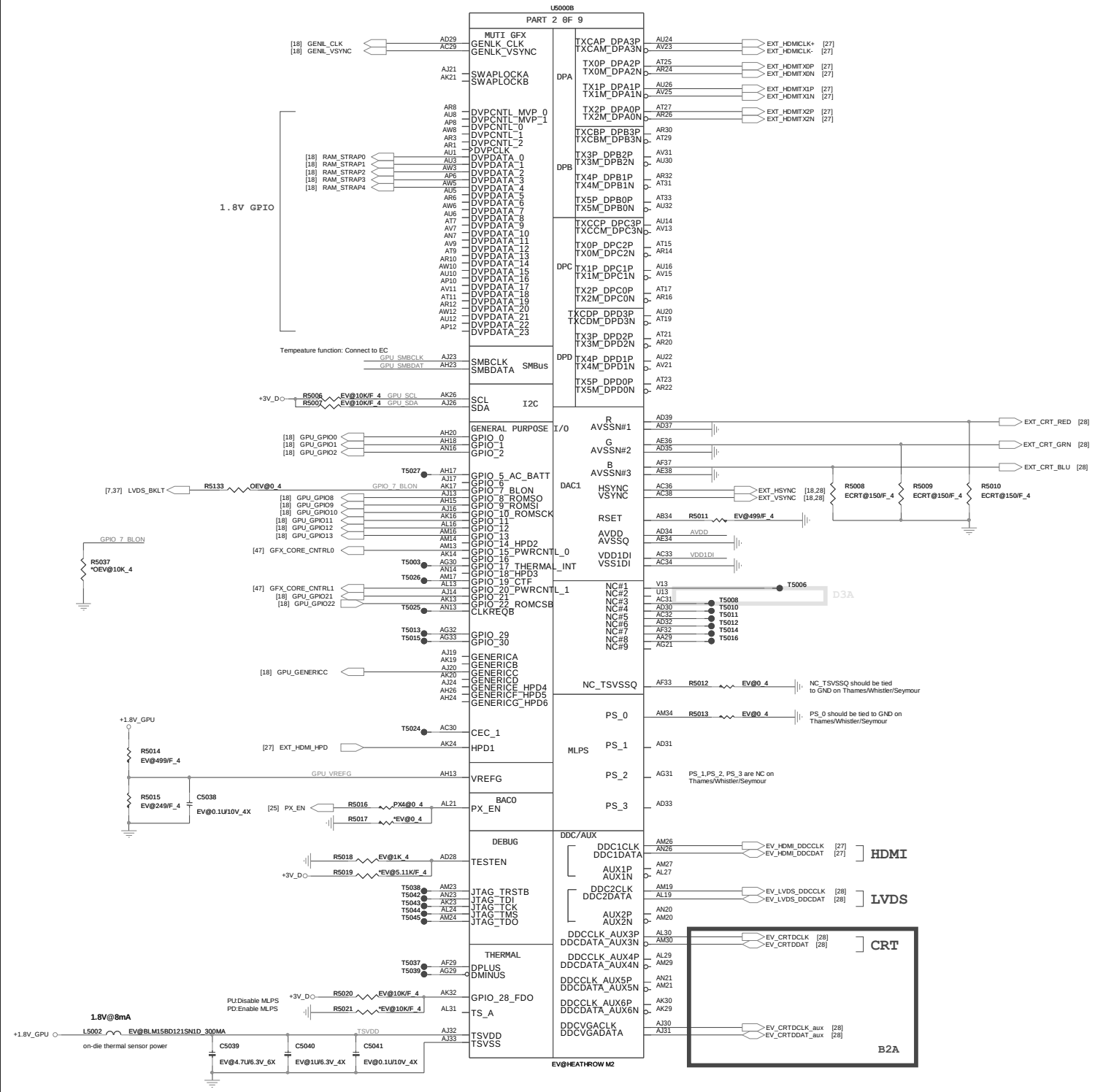


Thames and Seymour Power-on sequence

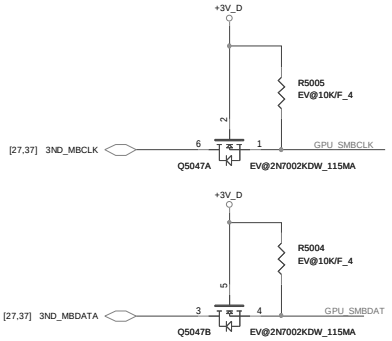
1 => +1V_GPU
2 => +3V_D
3 => +VGPU_CORE,+1.5V_GPU
4 => +1.8V_GPU

PEG

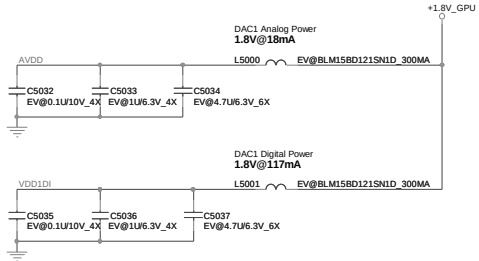
Intel platform: Lane0 ~ Lane15
Brazos platform: Lane12 ~ Lane15
Comal and Sabine platform: Lane8 ~Lane15



SMBUS power plane isolate



DAC Power



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Size	Document Number	Rev
	02_Thames_M2/ GPIO_DP_CRT_I2C	A1A
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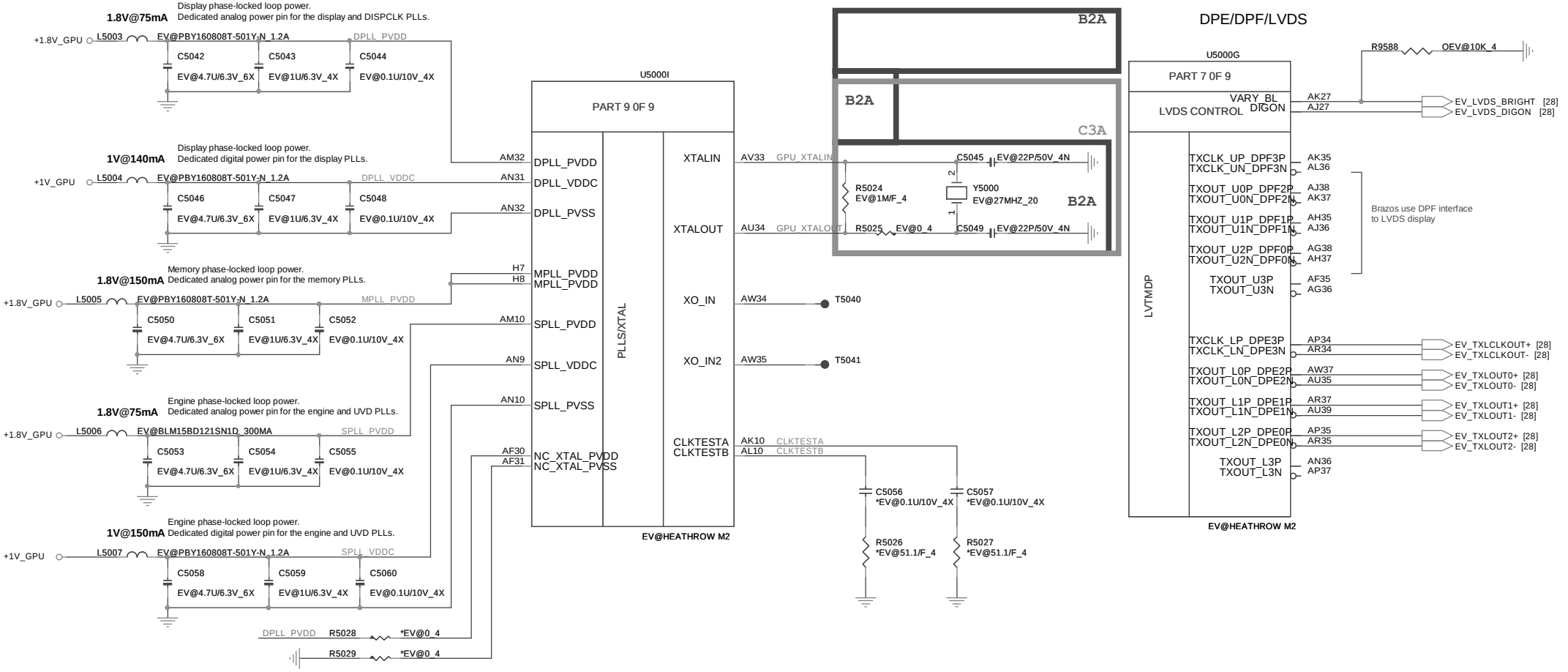

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Size	Document Number	Rev
	Thames_M2/ XTAL_LVDS	A1A

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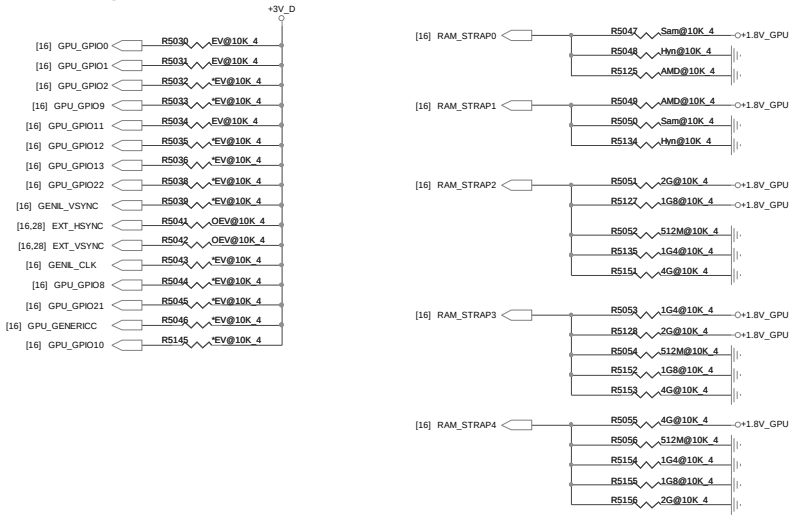
VGA/VGA-Strap



CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	MB Default Setting(IC internal PD)
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	1
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	0
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	0
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	0
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

DDR3 Memory TYPE				Size			Vendor		
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP4 DVPDATA_4	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	
Hynix	H5TQ1G63DFR-11C (64M*16)	AKD5LZWTW02 * 4	512MB	0	0	0	0	0	512@ & Hyn@
		AKD5LZWTW02 * 8	1GB	0	0	1	0	0	1G8@ & Hyn@
	H5TQ2G63BFR-11C (128M*16)	AKD5MGWTW00 * 4	1GB	0	1	0	0	0	1G4@ & Hyn@
		AKD5MGWTW00 * 8	2GB	0	1	1	0	0	2G@ & Hyn@
	H5TQ4G****** (256M*16)	AK********** * 8	4GB	1	0	0	0	0	4G@ & Hyn@
Samsung	K4W1G1646G-BC11 (64M*16)	AKD5EGGT500 * 4	512MB	0	0	0	0	1	512@ & Sam@
		AKD5EGGT500 * 8	1GB	0	0	1	0	1	1G8@ & Sam@
	K4W2G1646C-HC11 (128M*16)	AKD5MGWT500 * 4	1GB	0	1	0	0	1	1G4@ & Sam@
		AKD5MGWT500 * 8	2GB	0	1	1	0	1	2G@ & Sam@
	K4W4G****** (256M*16)	AK********** * 8	4GB	1	0	0	0	1	4G@ & Sam@
AMD	23EY2387MC11 (64M*16)	AKD5EZWT700 * 4	512MB	0	0	0	1	0	512@ & AMD@
		AKD5EZWT700 * 8	1GB	0	0	1	1	0	1G8@ & AMD@
	23EY4187MC11 (128M*16)	AKD5DZWT700 * 4	1GB	0	1	0	1	0	1G4@ & AMD@
		AKD5DZWT700 * 8	2GB	0	1	1	1	0	2G@ & AMD@
	23EY********** (256M*16)	AK********** * 8	4GB	1	0	0	1	0	4G@ & AMD@

System Memory Aperture size

GPIO22 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1

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	Thames_M2/ STRAPS_Thermal	A1A

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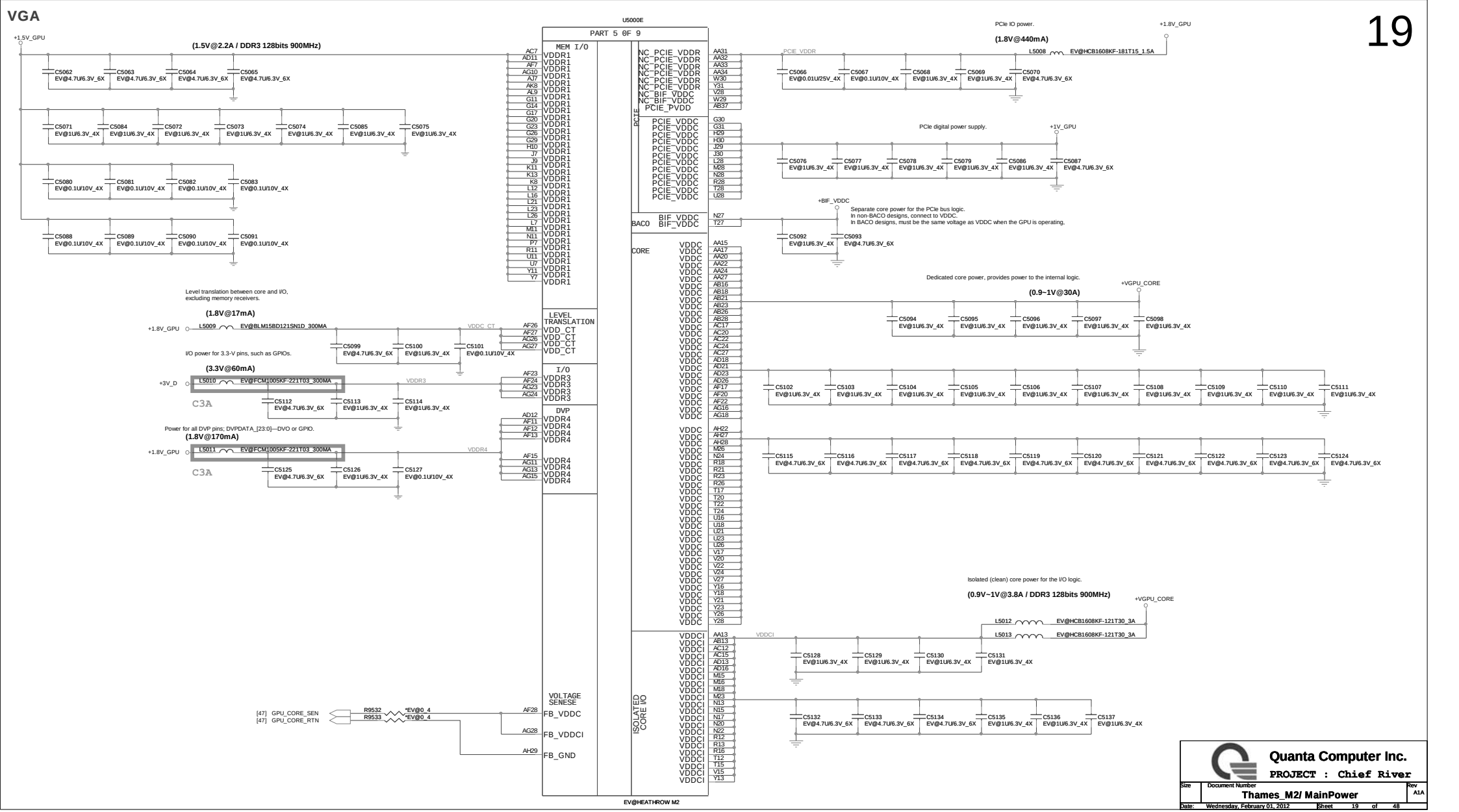
U5000E
PART 5 0F 9
+1.5V_GPU
(1.5V@2.2A / DDR3 128bits 900MHz)
MEM I/O
LEVEL TRANSLATION
I/O
DVP
VOLTAGE SENESE
PCIE
BACO
CORE
ISOLATED CORE I/O
Level translation between core and I/O, excluding memory receivers.
(1.8V@17mA)
I/O power for 3.3-V pins, such as GPIOs.
(3.3V@60mA)
Power for all DVP pins; DVPDATA_[23:0]—DVO or GPIO.
(1.8V@170mA)
PCIe IO power.
(1.8V@440mA)
PCIe digital power supply.
Separate core power for the PCIe bus logic.
In non-BACO designs, connect to VDDC.
In BACO designs, must be the same voltage as VDDC when the GPU is operating,
Dedicated core power, provides power to the internal logic.
(0.9~1V@30A)
Isolated (clean) core power for the I/O logic.
(0.9V~1V@3.8A / DDR3 128bits 900MHz)
EV@HEATHROW M2

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Document Number
Thames_M2/ MainPower
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A1A
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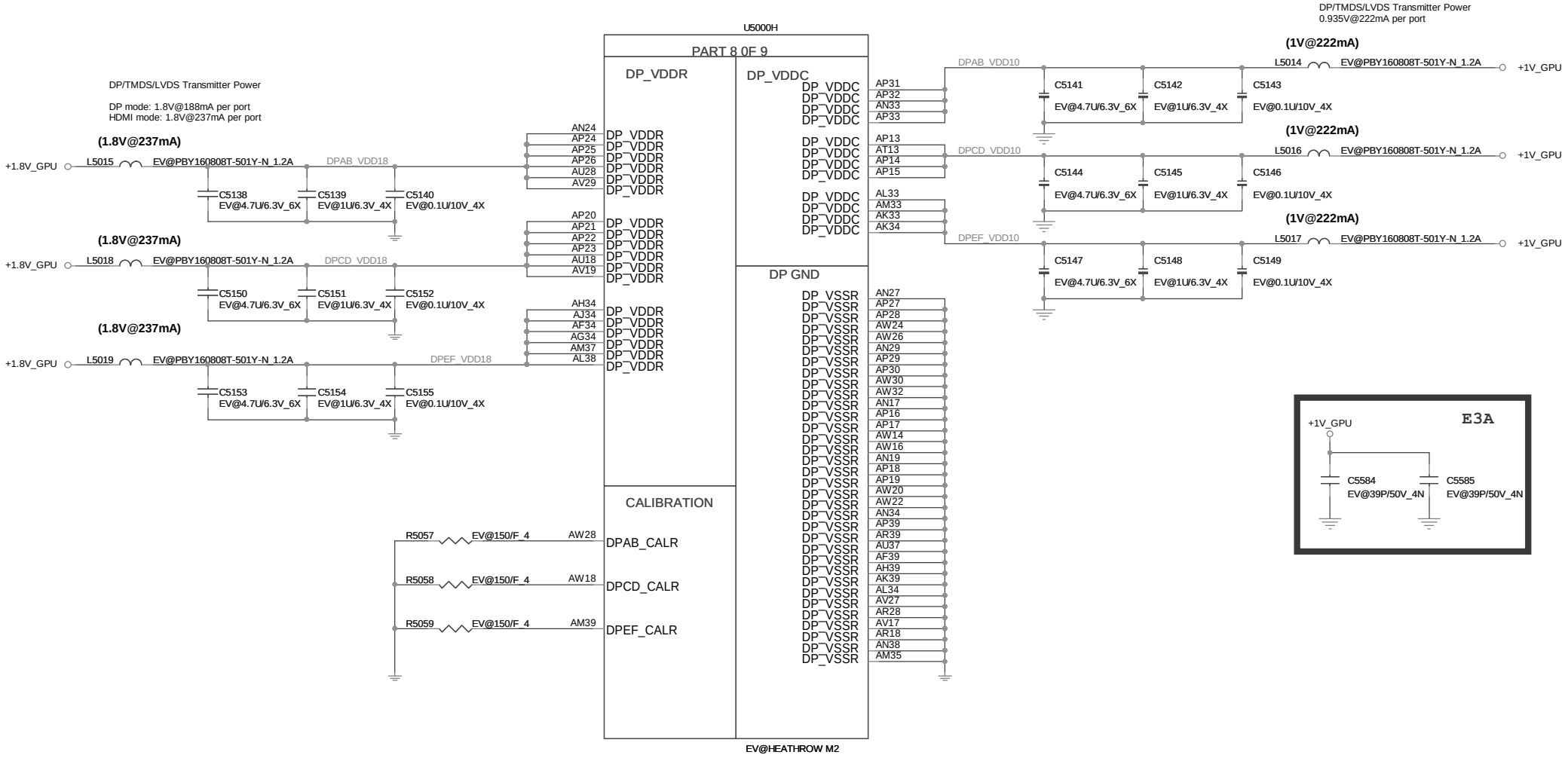

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Size	Document Number: Thames_M2/ DP_Powers	Rev: A1A
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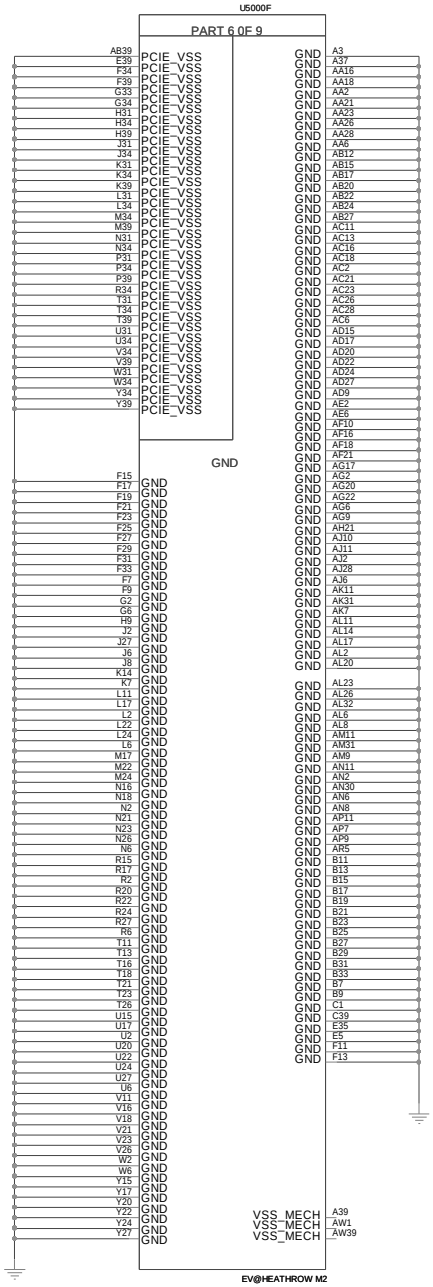

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Size	Document Number: Thames_M2/ GND	Rev: A1A
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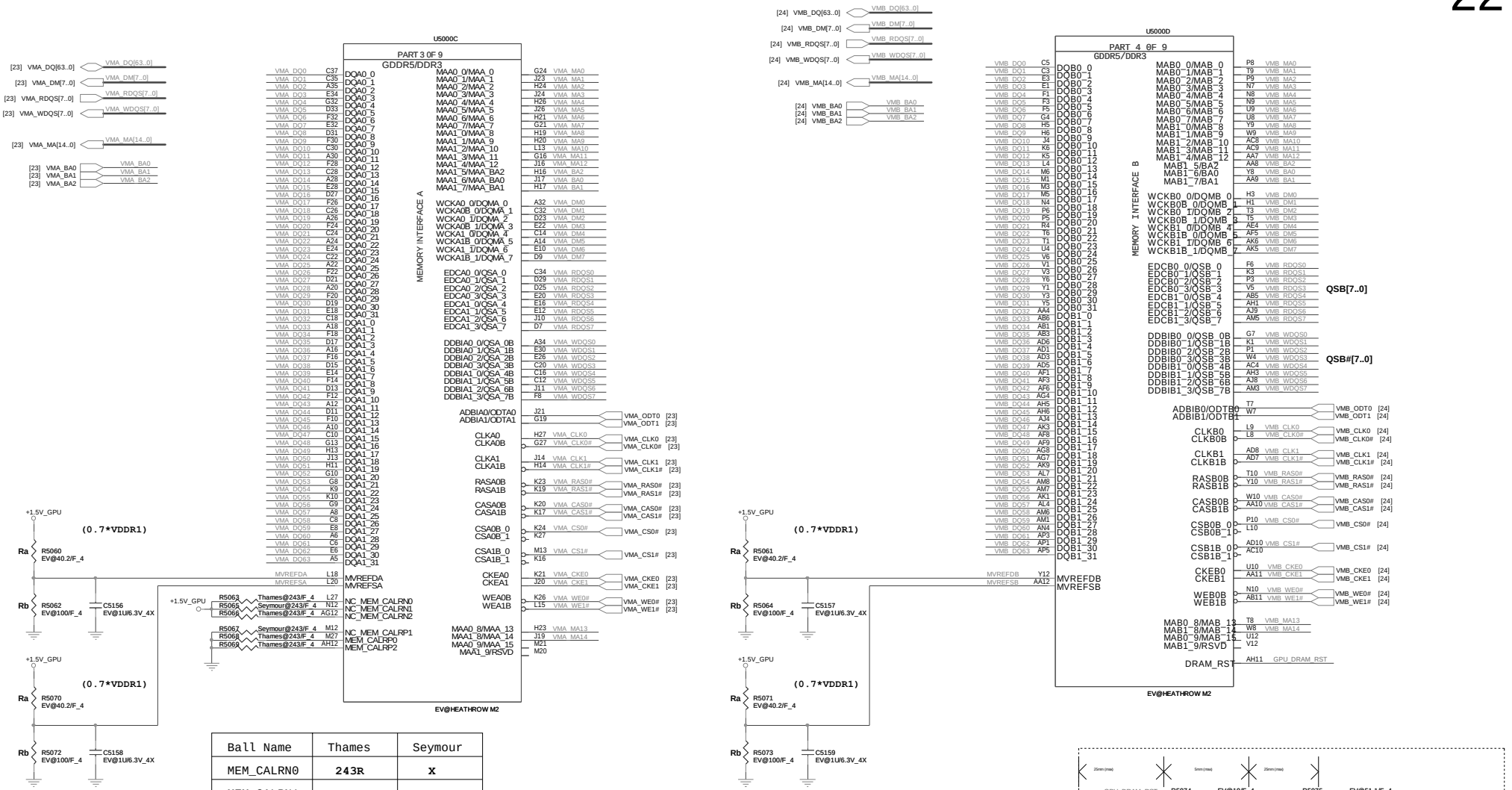
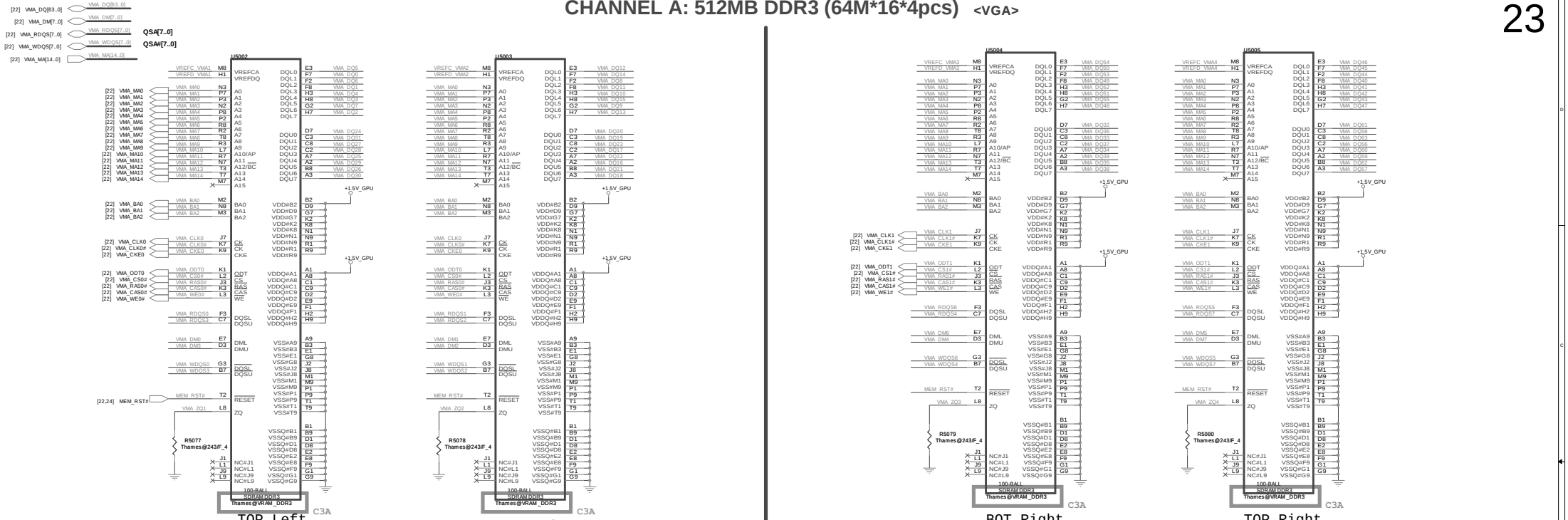


Ball Name	Thames	Seymour
MEM_CALRN0	243R	X
MEM_CALRN1	X	243R
MEM_CALRN2	243R	X
MEM_CALRP0	243R	X
MEM_CALRP1	X	243R
MEM_CALRP2	243R	X

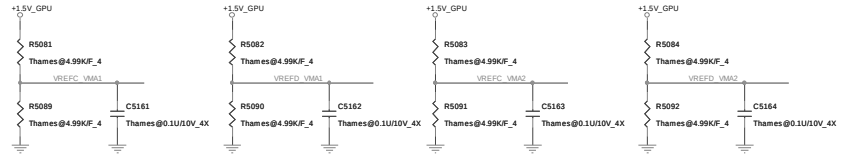
Place all these componets very close to GPU (within 25mm)
and keep all components close to each other
** This basic topology should be used for DRAM_RAT for DDR3/GDDR5

These Capacitors and Resistor values arre an example only
The series R and || cap values will depend on the DRAM loads
and will have to be calculated for differrent Memory, DRAM loads and board
to pass Reset Signal Spec

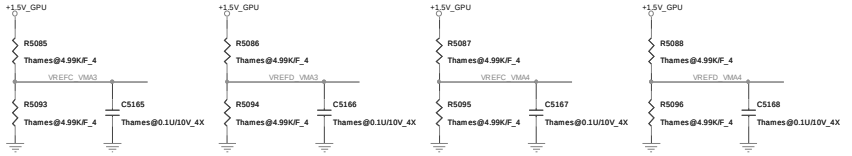
CHANNEL A: 512MB DDR3 (64M*16*4pcs) <VGA>



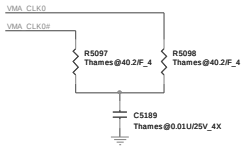
Group-A0 VREF



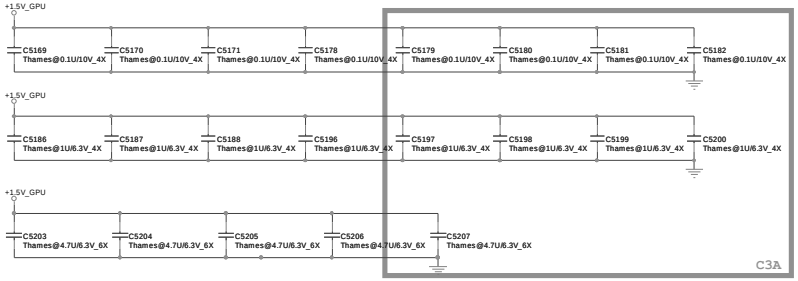
Group-A1 VREF



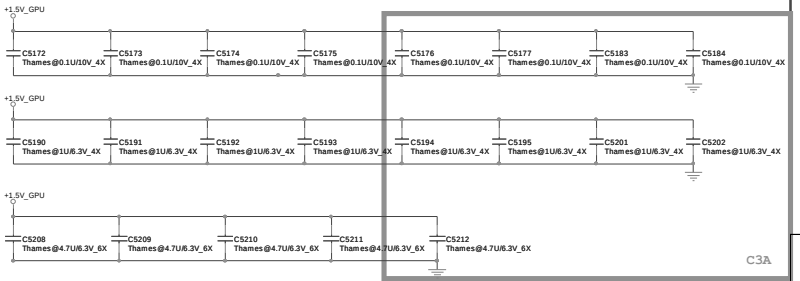
MEM_A0 CLK



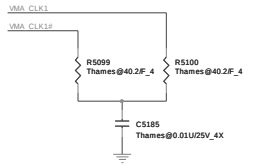
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



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	VRAM_A: DDR3*4PCS	A1A

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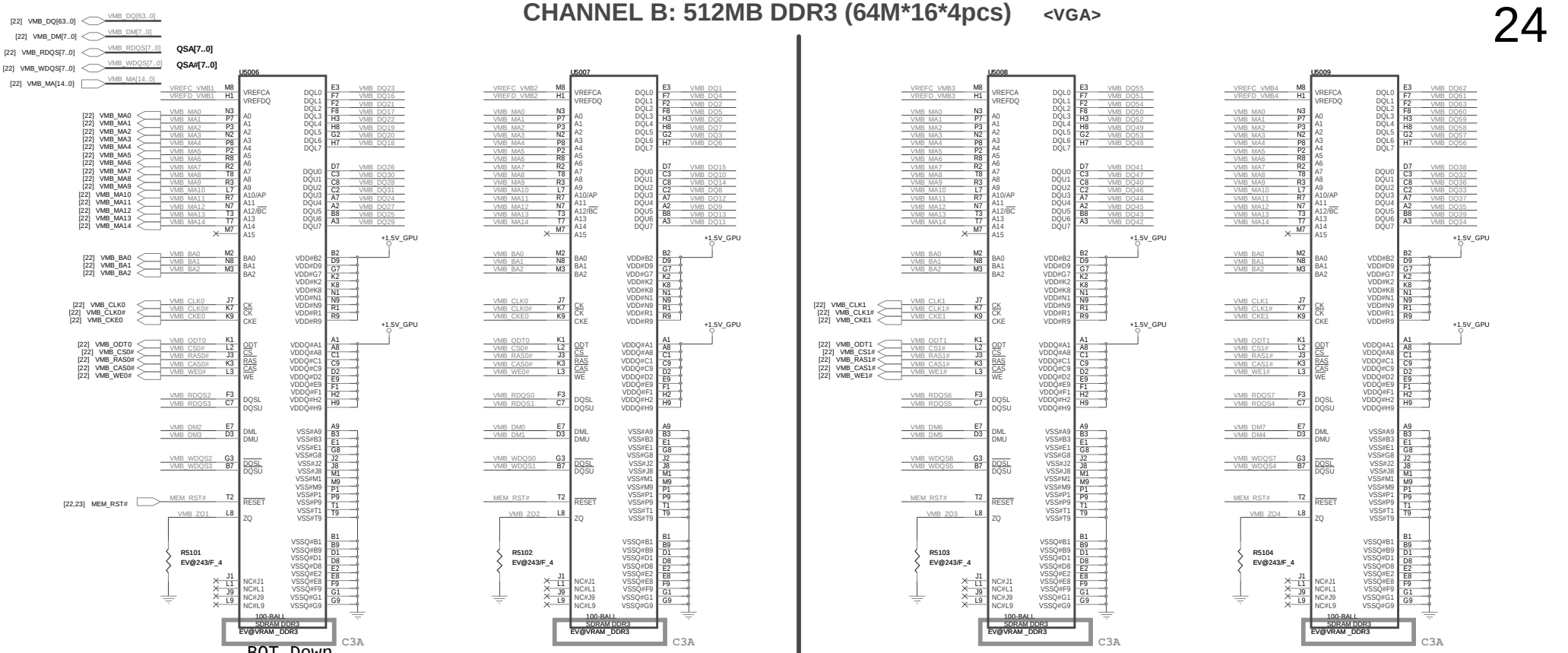
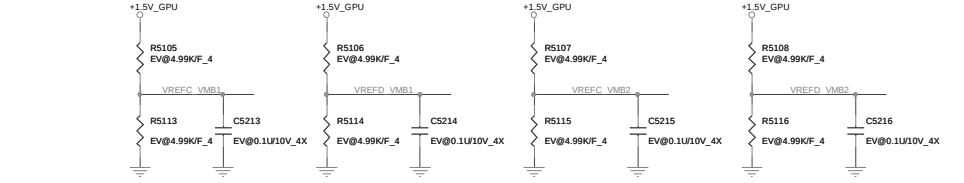
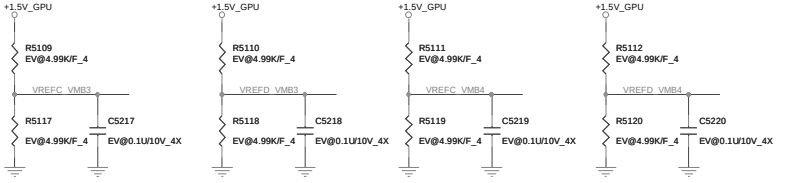
CHANNEL B: 512MB DDR3 (64M*16*4pcs) <VGA>



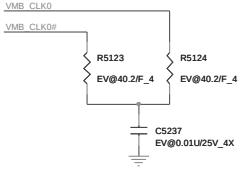
Group-B0 VREF



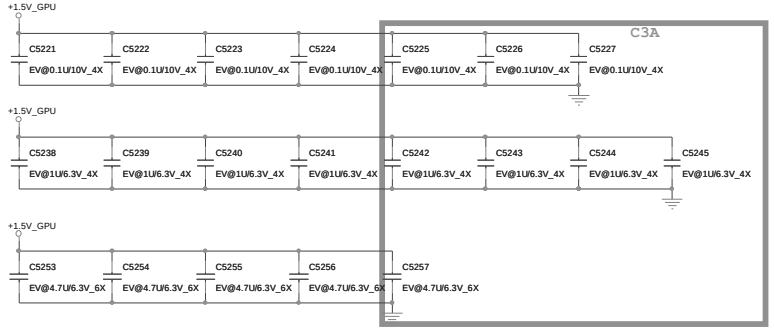
Group-B1 VREF



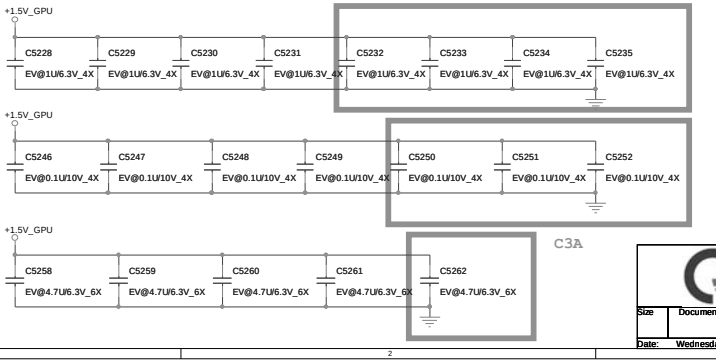
MEM_B0 CLK



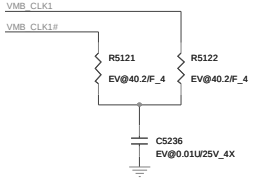
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



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PROJECT : Chief River

Size	Document Number	Rev
	VRAM_B: DDR3*4PCS	A1A
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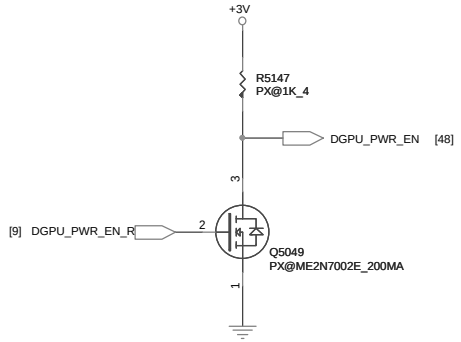
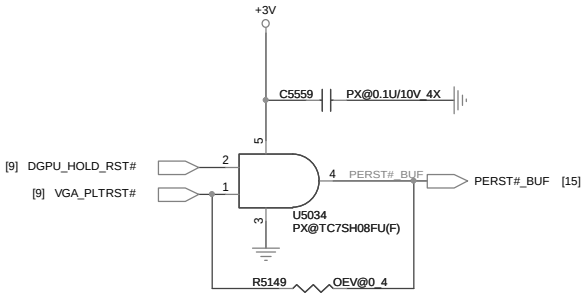
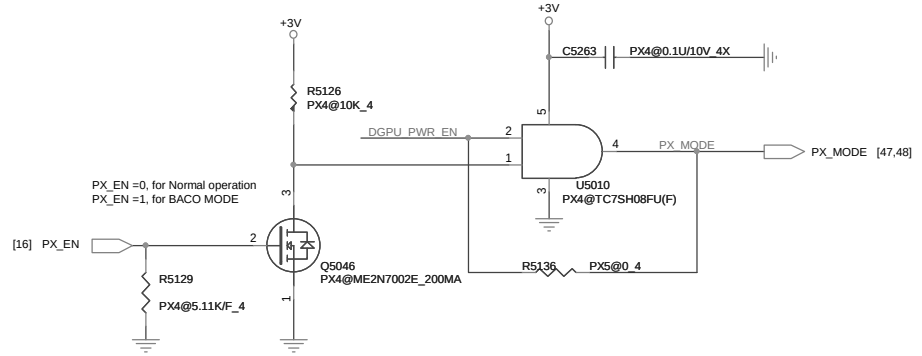
VGA Power Enable Reverse (Intel --> Low Active) PX



Platform Reset PX/OEV

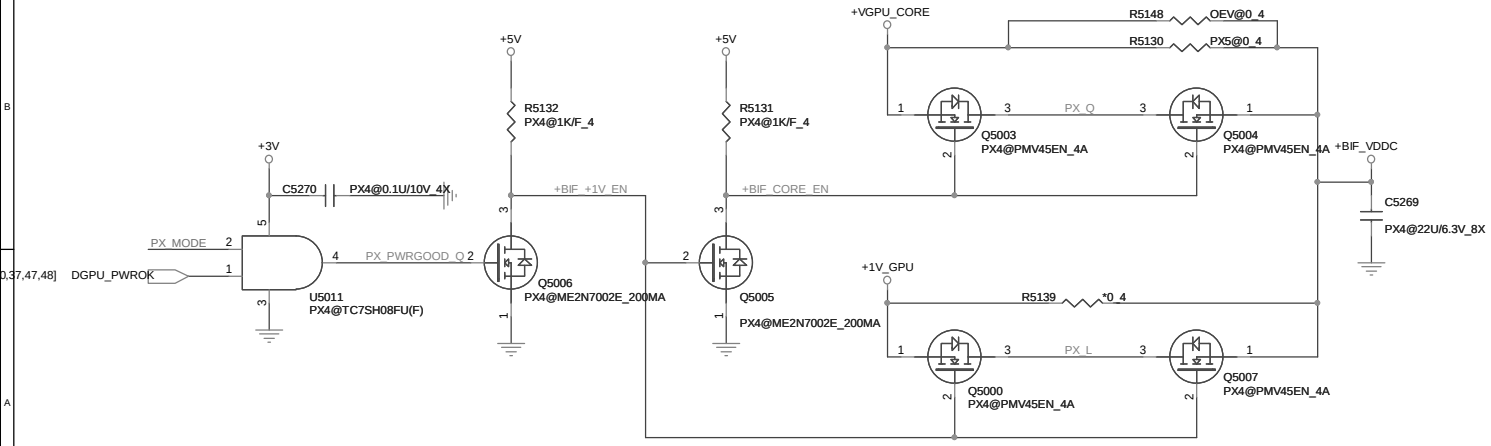


PX Mode control signal PX4/PX5

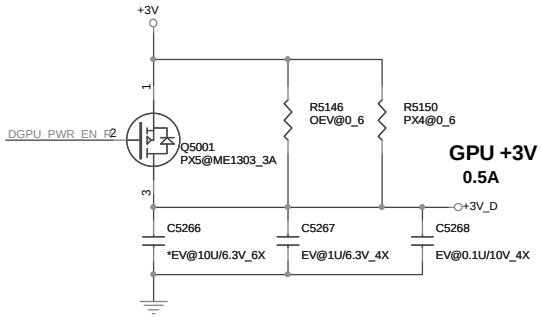


Core power for PCIE Logic PX4/PX5/OEV

Designs that do not support the BACO option must connect the BIF_VDDC to VDDC



3.3V VGA/PX4/PX5/OEV



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Size	Document Number: Thames_M2/ Baco	Rev: A1A
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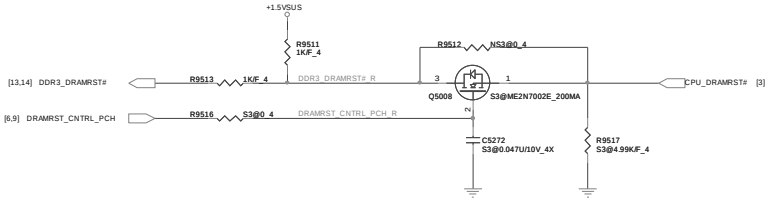
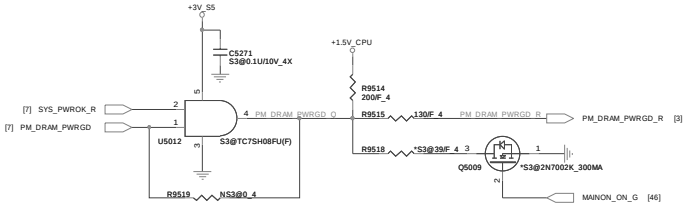
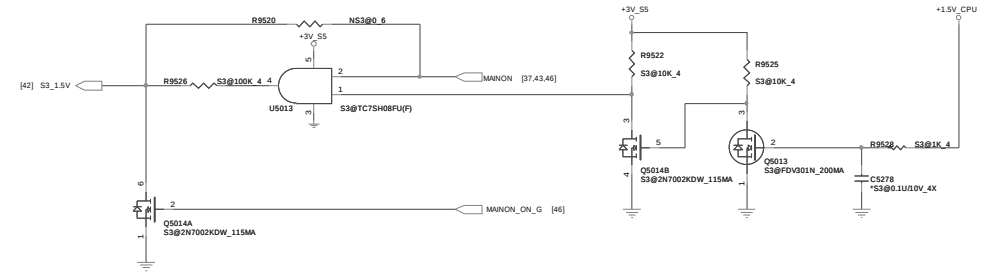
S3 power Reduction (SM_DRAMRST#) S3P/NS3P/CPU



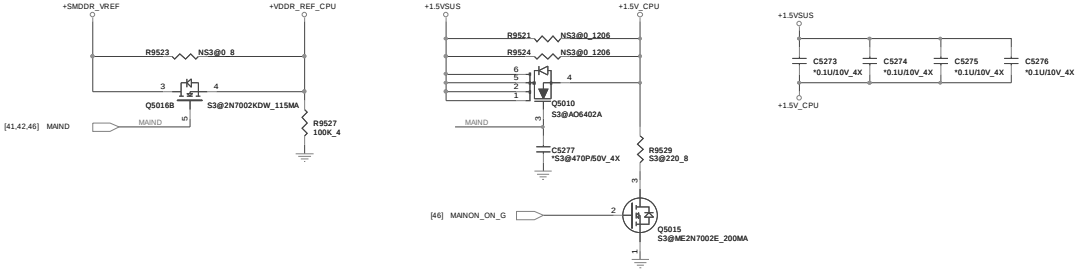
S3 power Reduction (SM_DRAMPWROK) S3P/NS3P/CPU



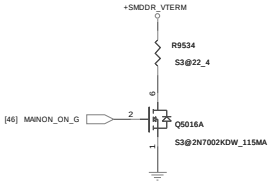
For S3 power Reduction Sequence S3P/NS3P/CPU



S3 power Reduction (CPU Power) S3P/NS3P/CPU



For S3 power Reduction VTT discharge S3P/NS3P/CPU



Quanta Computer Inc.

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Size	Document Number	Rev
	S3 power Reduction	A1A
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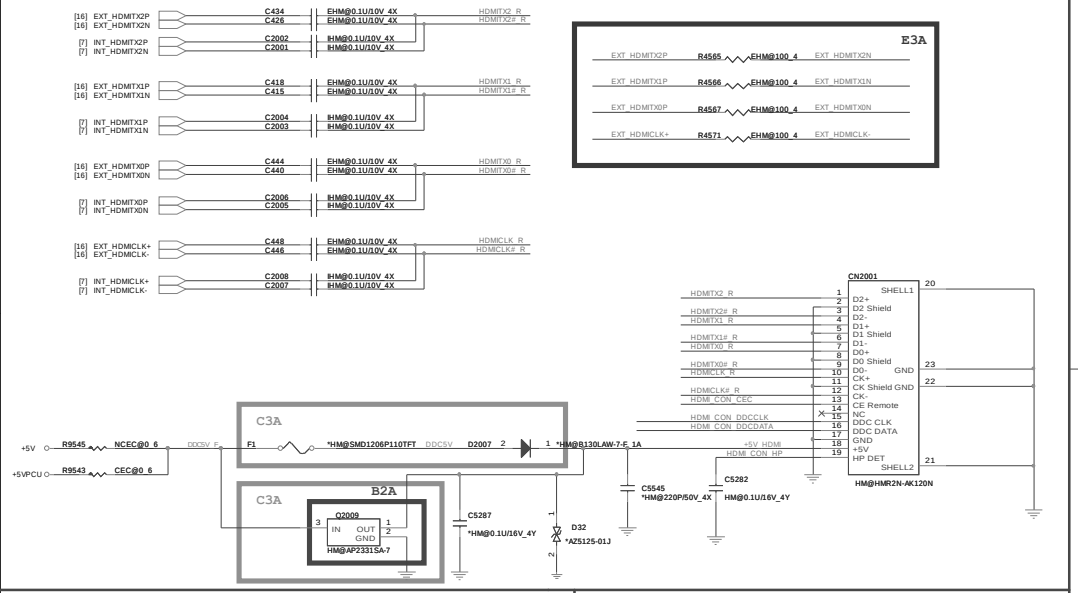
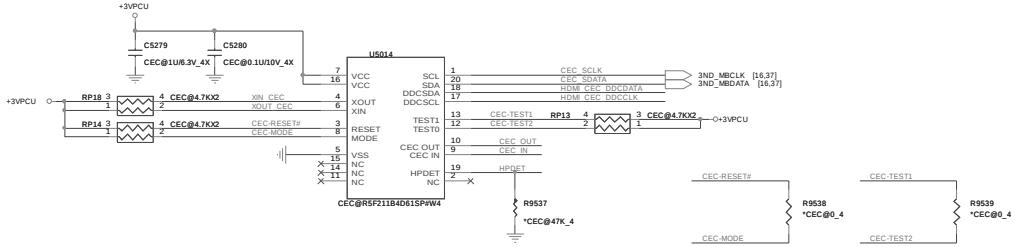
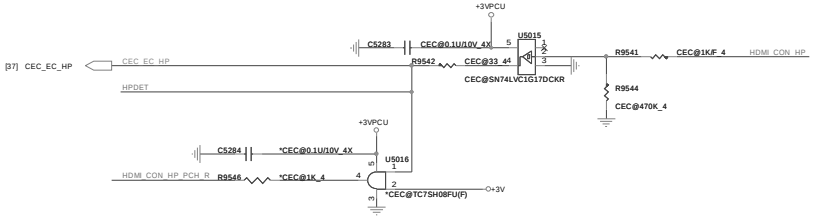
HDMI Conn HDM/HMU/HMV



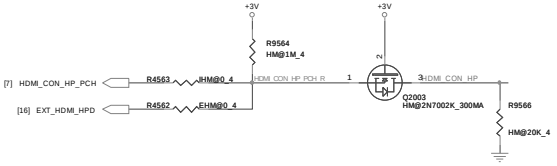
HDMI CEC CEC



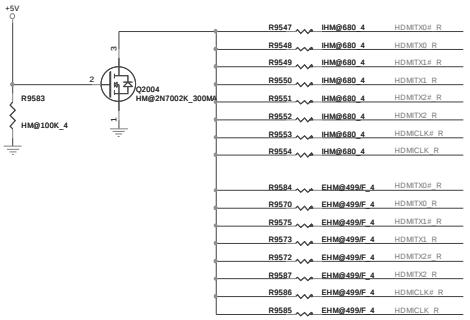
CEC HotPlug CEC



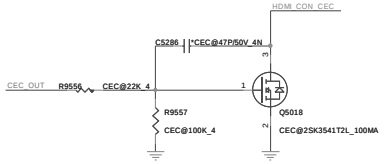
HDMI-HPD HDM/HMU/HMV



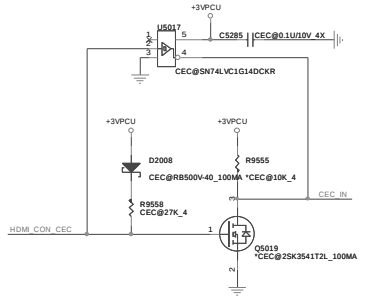
HDMI LEVEL SHIFT HDM/HMU/HMV



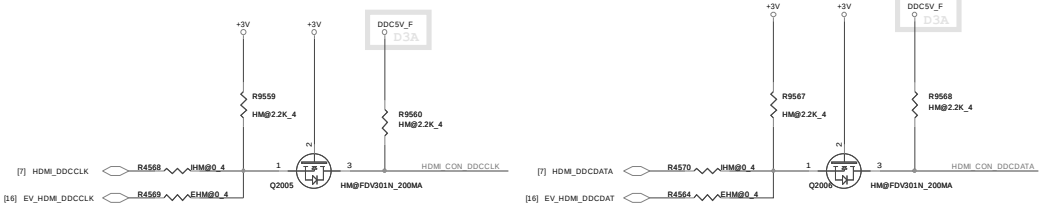
CEC Output CEC



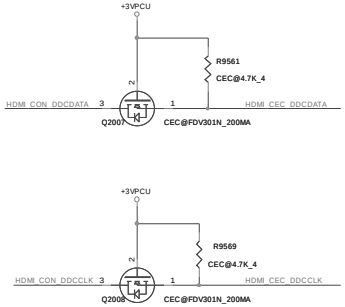
CEC Input CEC



HDMI-SMBus HDM/HMU/HMV



CEC SMBus Level Shift CEC



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	HDMI CONN	A1A

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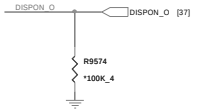
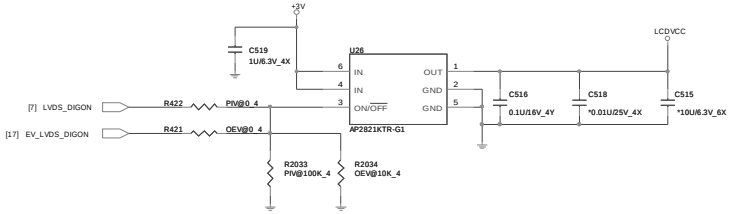
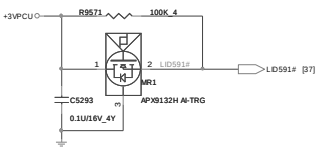
Panel backlight control LDS



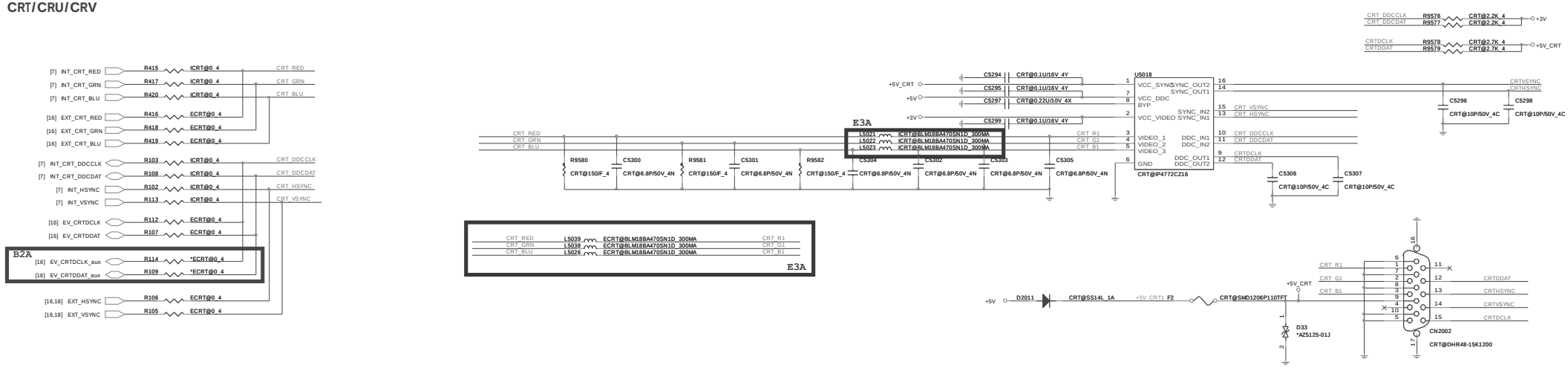
LCD POWER SWITCH LDS/LDU/LDV



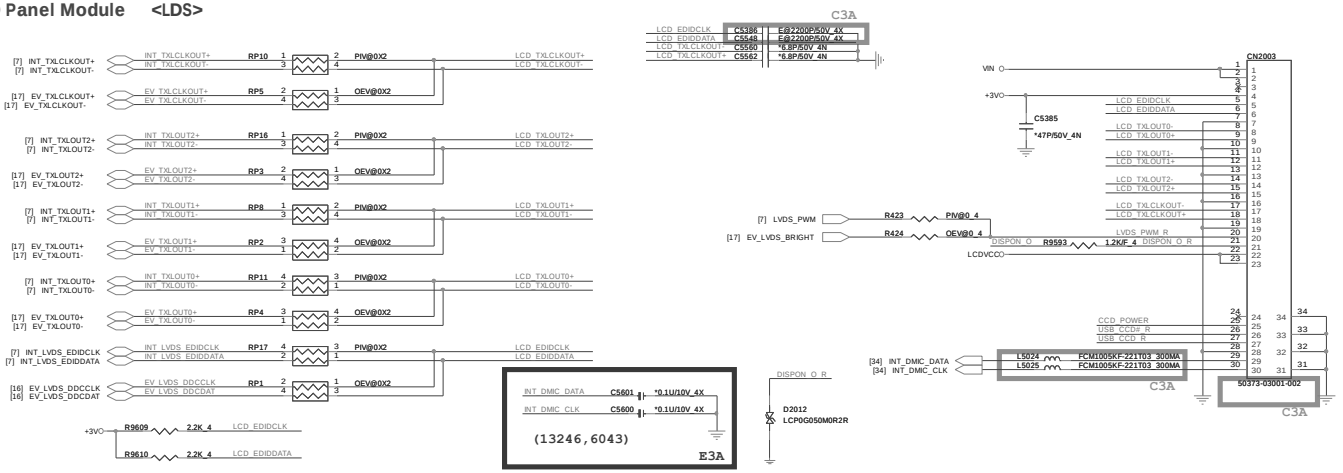
HALL Sensor HSR



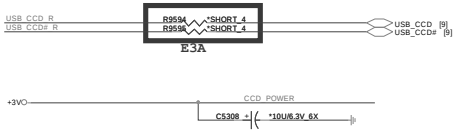
CRT CRT/CRU/CRV



LCD Panel Module <LDS>



CCD CCD



Quanta Computer Inc.
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Size	Document Number	Rev
	LCD/LED Panel/CCD	A1A

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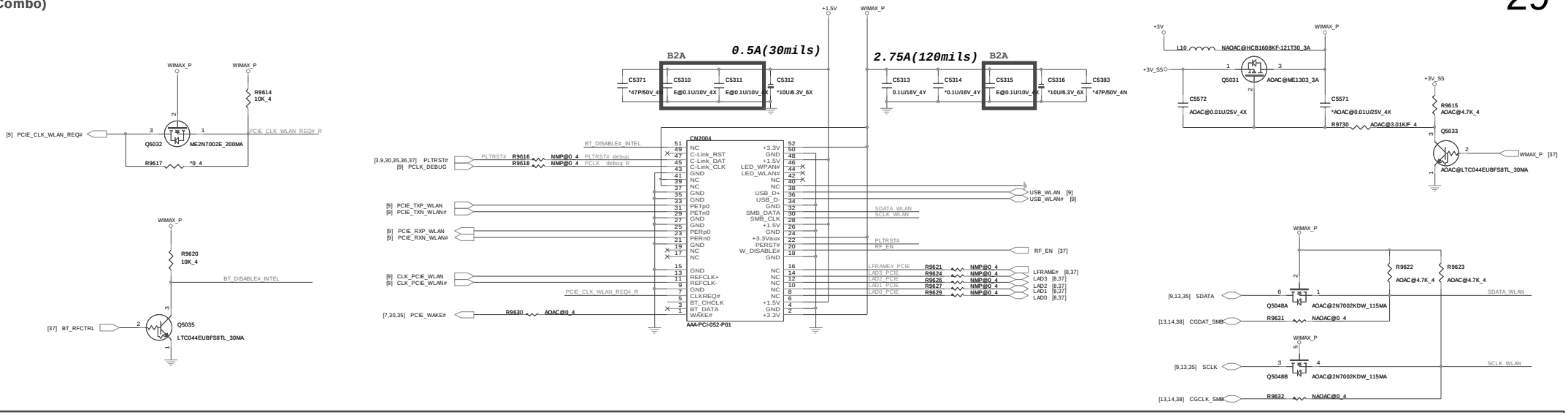
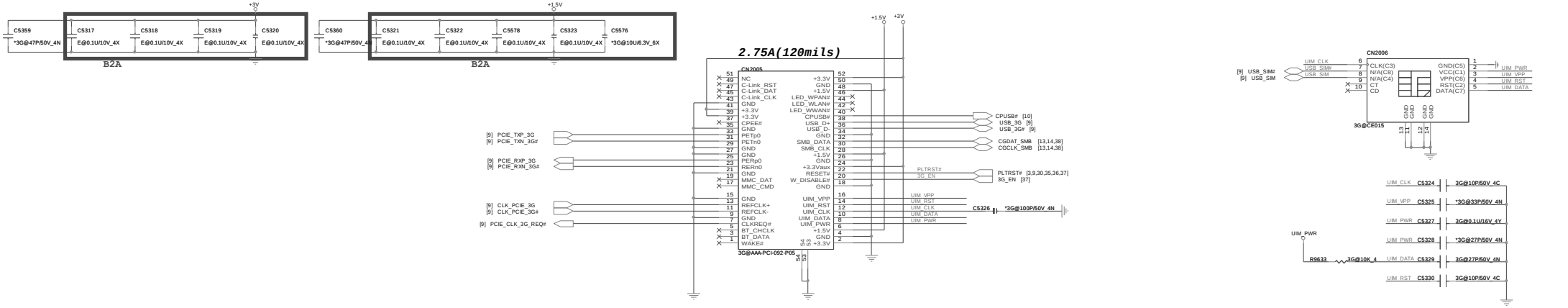
MINI Card Slot#1(WiFi / Wimax / Combo)

MNW/DEG



MINI Card Slot#2-3G

MNG



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Size	Document Number: MINI CARD(WLAN/3G/SIM Card) — Rev: A1A
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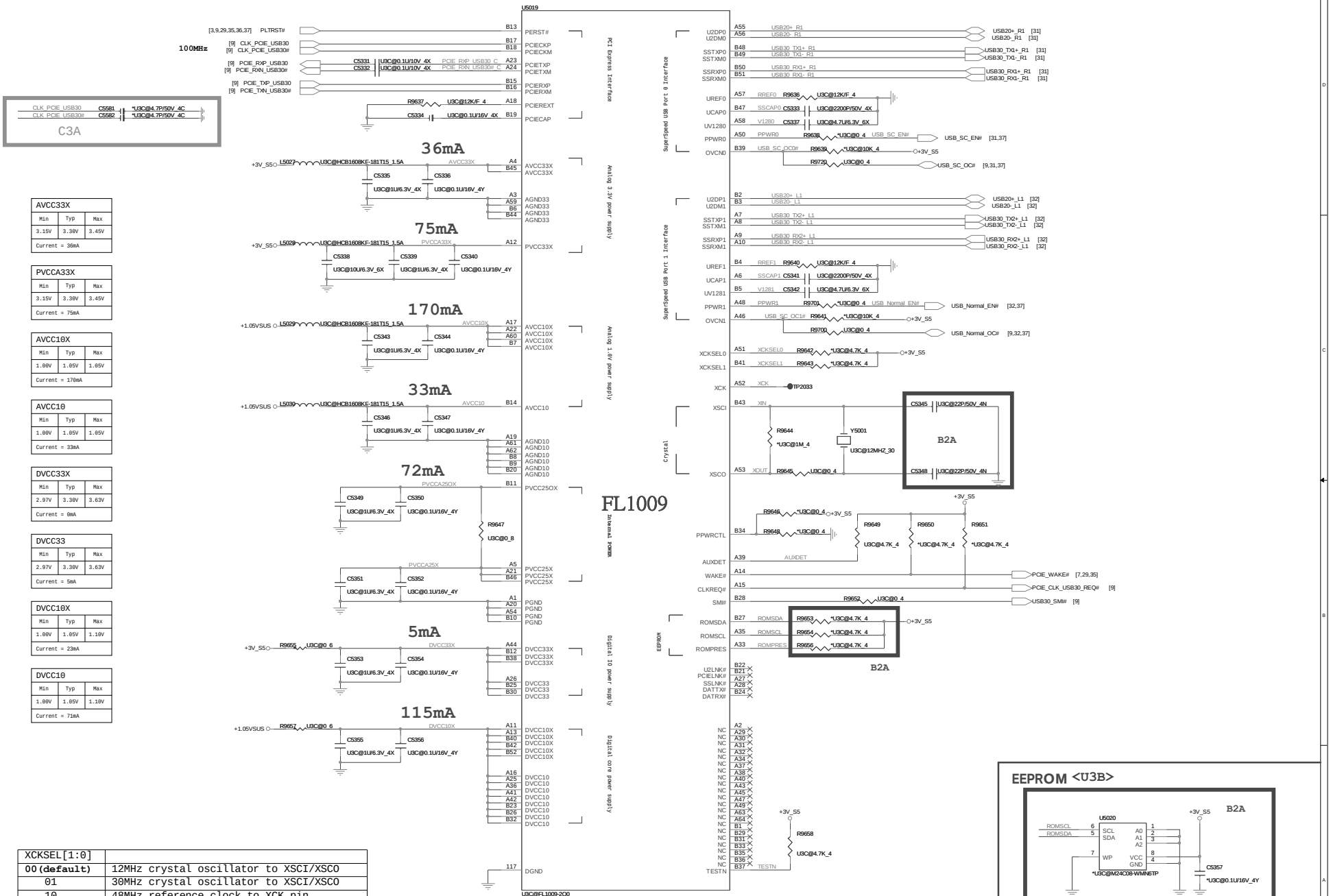


AVCC33X		
Min	Typ	Max
3.15V	3.30V	3.45V
Current = 36mA		

PVCCA33X		
Min	Typ	Max
3.15V	3.30V	3.45V
Current = 75mA		

AVCC10X		
Min	Typ	Max
1.00V	1.05V	1.05V
Current = 170mA		

AVCC10		
Min	Typ	Max
1.00V	1.05V	1.05V
Current = 33mA		

DVCC33X		
Min	Typ	Max
2.97V	3.30V	3.63V
Current = 0mA		

DVCC33		
Min	Typ	Max
2.97V	3.30V	3.63V
Current = 5mA		

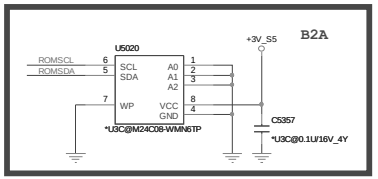
DVCC10X		
Min	Typ	Max
1.00V	1.05V	1.10V
Current = 23mA		

DVCC10		
Min	Typ	Max
1.00V	1.05V	1.10V
Current = 71mA		

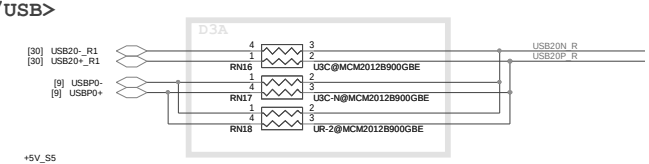
XCKSEL[1:0]	
00(default)	12MHz crystal oscillator to XSCI/XSCO
01	30MHz crystal oscillator to XSCI/XSCO
10	48MHz reference clock to XCK pin
11	24MHz reference clock to XCK pin

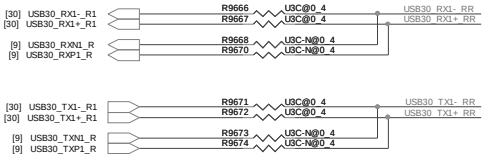
PPWRCTL	VBus controllable, internal pull down
0	VBus is not controlled by FL1009
1	VBus is controlled by FL1009

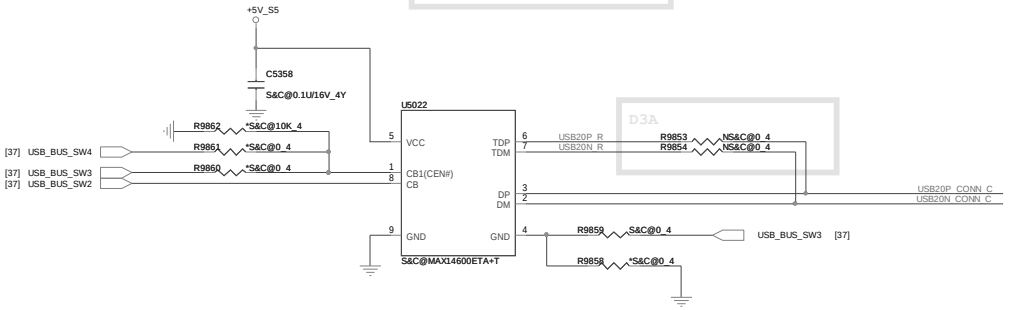
EEPROM <U3B>



USB CONNECT RIGHT(UR) <U3B/USB>



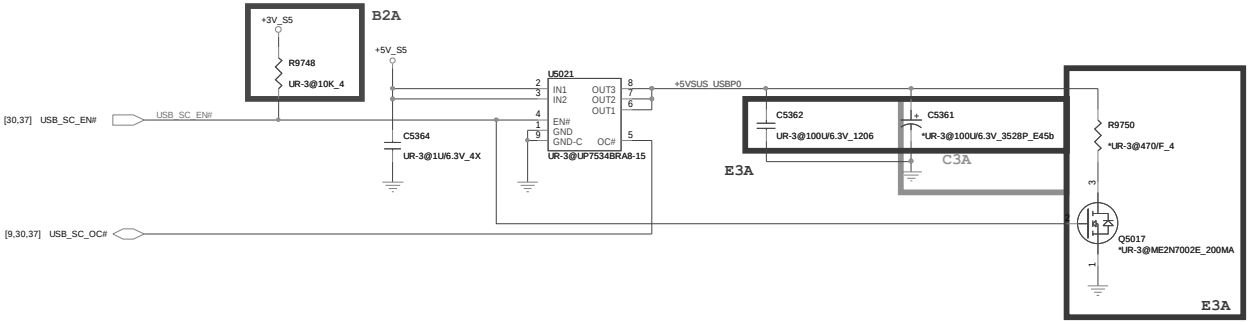


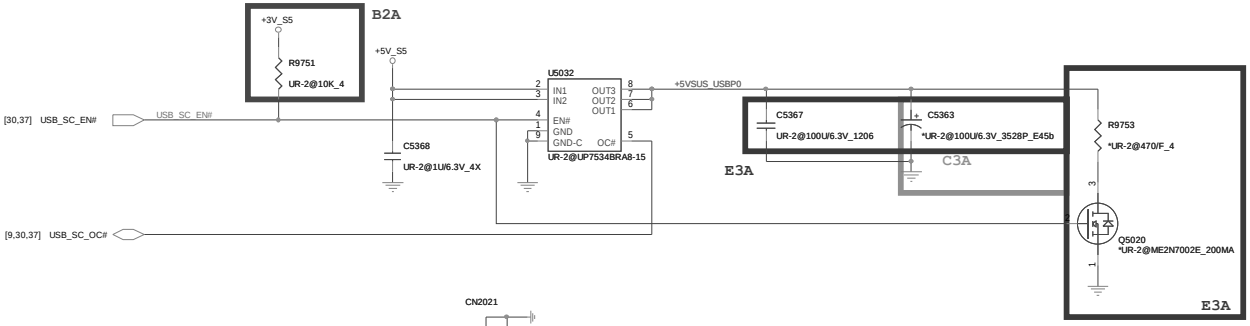


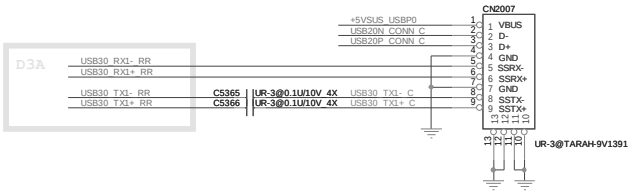
	R9861	R9860	R9859	R9858	R9862
14566		V		V	
14600			V		
14617(with CB2)	V		V		
14617(no CB2)			V		V

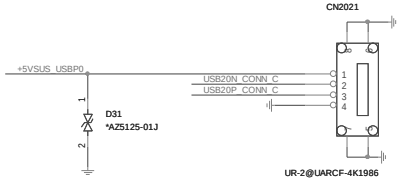
14566/14600		
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM for 14566
1	0	Pass-Through(USB) mode for 14600
1	1	pass-through(USB) with CDP Emulation for 14600

14617			
CB0	CB1	CB2	Status
X	X	1	Force Apple 2A Charger Mode
0	0	0	Autodetection charger mode
0	1	0	Force-Dedicated Charger Mode
1	0	0	USB Pass-Through Mode(USB) Connect DP/DM to TDP/TDM
1	1	0	USB Pass-Through Mode with CDP Emulation.Auto connect DP/DM to TDP/TDM depending on CDP status









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	USB3 Redriver/S&C/USB2	A1A
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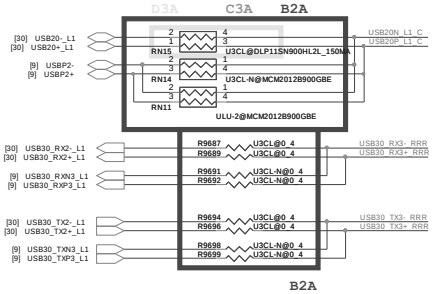
USB CONNECT LEFT1(ULU)

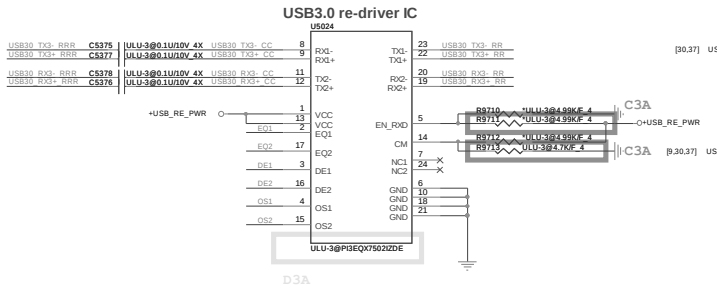
<U3B/USB>

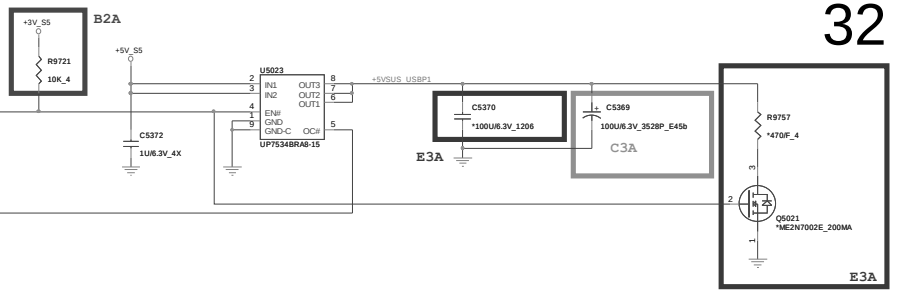


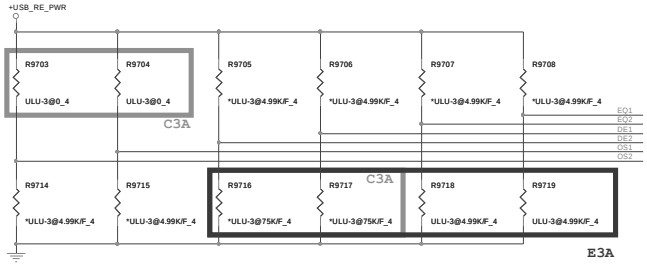
USB 3.0 Rrdriver IC

<U3B>

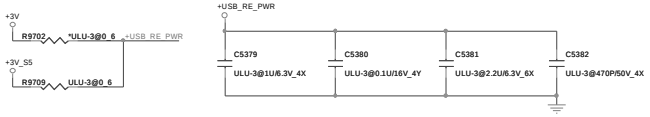
USB3.0 re-driver IC

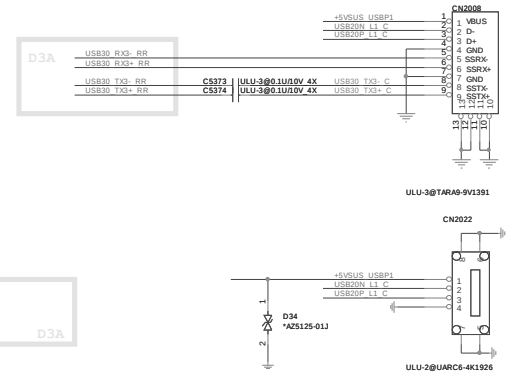






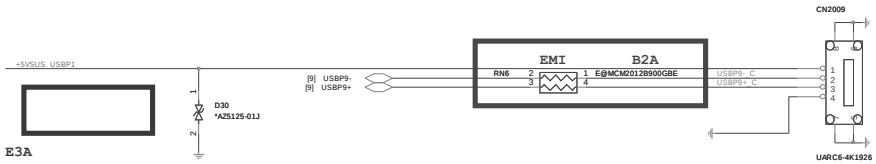
Control pins setting			
EN_RXD	Device function	CM	Device function
1(default)	Normal Operation	0(default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode





USB CONNECT LEFT2(ULD)

ULD



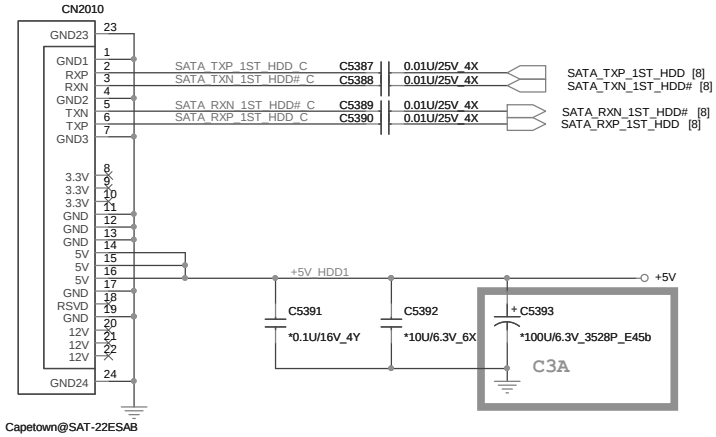
D3A

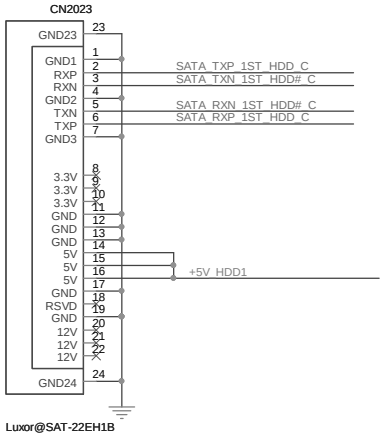
Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	USB3 Redriver/USB2_Left	ALA
Date: Wednesday, February 01, 2012	Sheet 32 of 48	

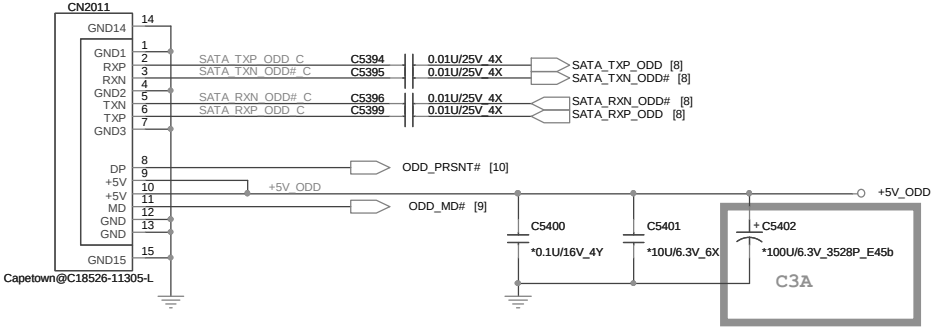
SATA HDD

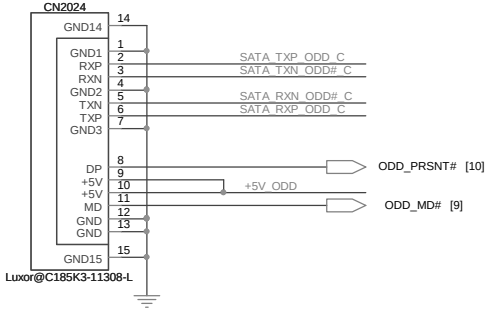
HDD



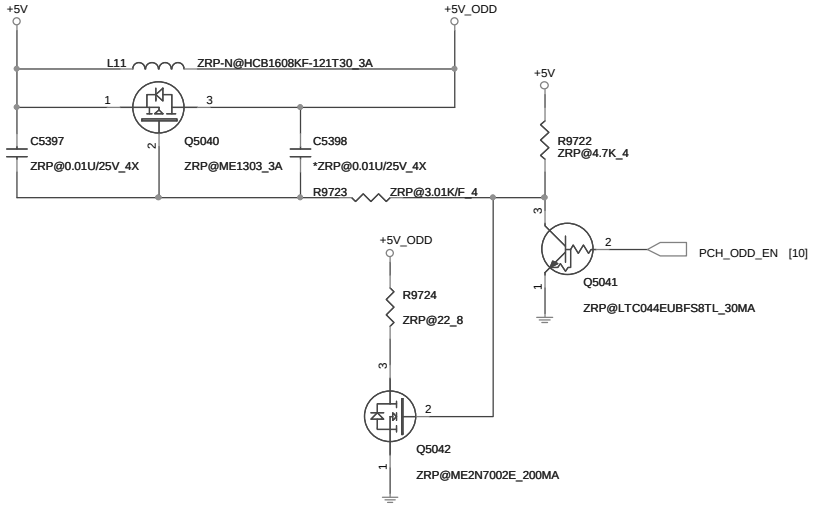


SATA ODD <ODD>



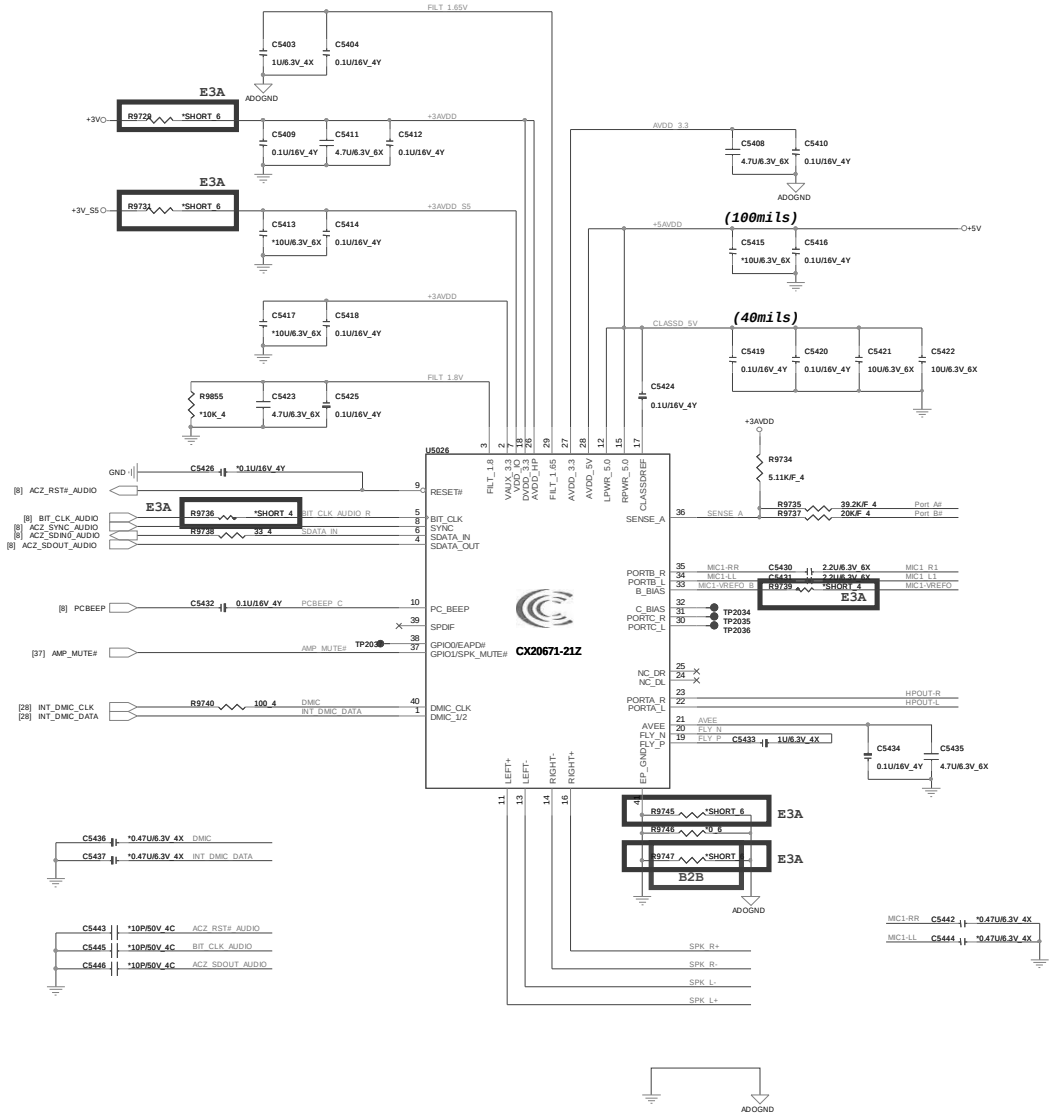


ODD Zero power . (Only for Intel) <OZP>

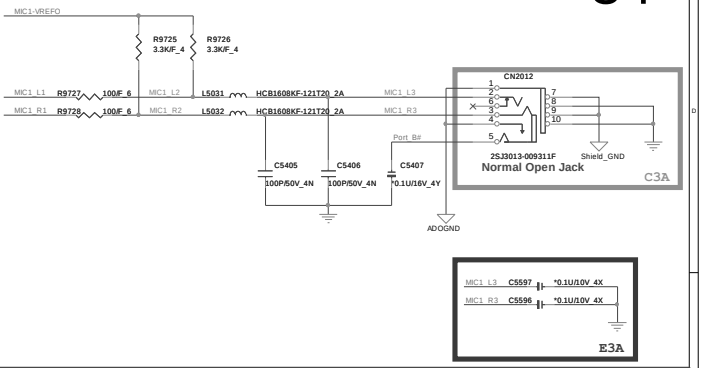


Quanta Computer Inc.		
PROJECT : Chief River		
Size	Document Number: HDD/ODD	Rev: A1A
Date: Wednesday, February 01, 2012	Sheet 33 of 48	

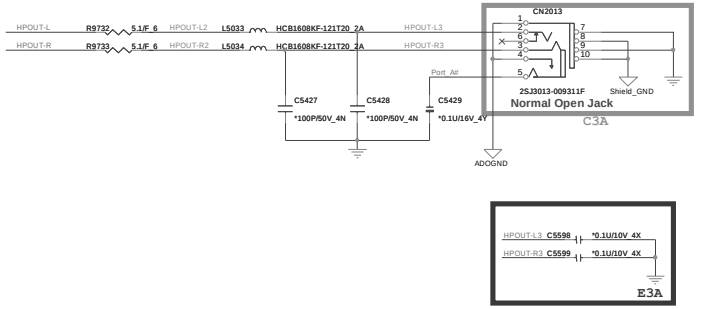
Codec (CX20671-21Z) <ADO>



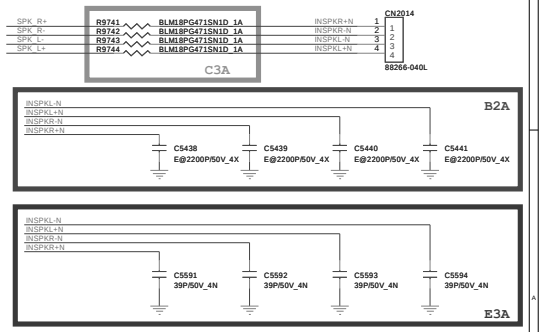
External MIC <ADO>



Headphone <ADO>



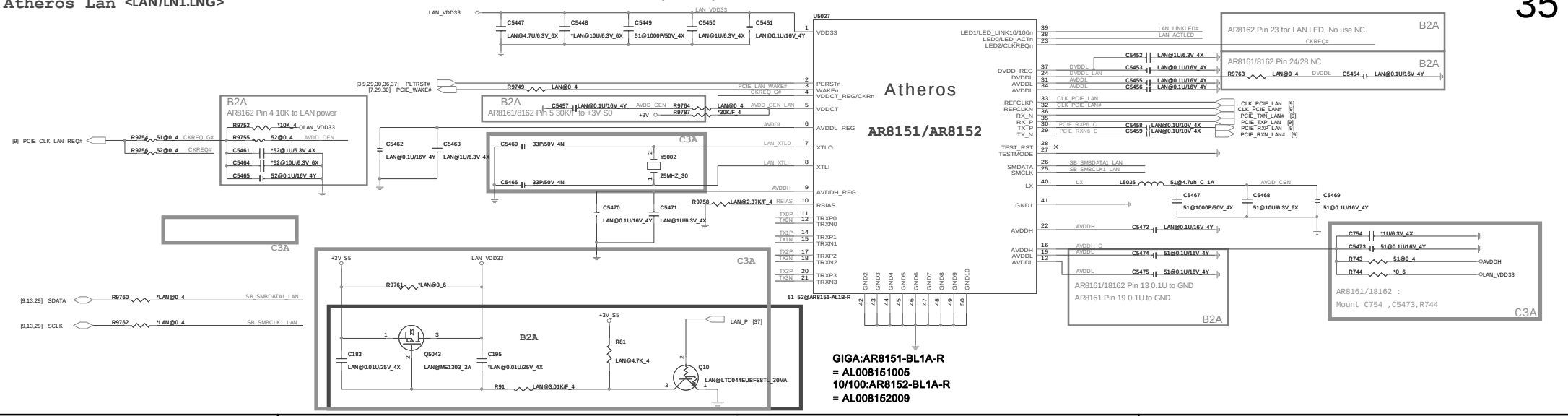
Internal Speaker <ADO>



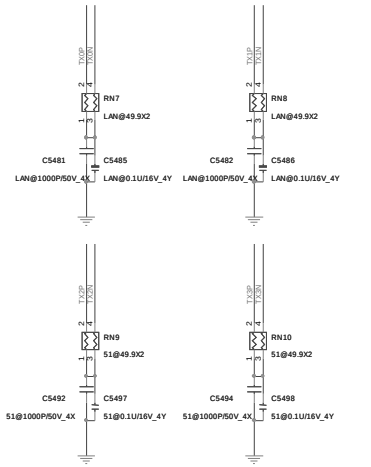
Quanta Computer Inc.	
PROJECT : Chief River	
Size	Document Number: Audio Codec (CX20671) — Rev: A1A
Date: Wednesday, February 01, 2012	Sheet 34 of 48

Atheros Lan <LAN/LN1.LNG>

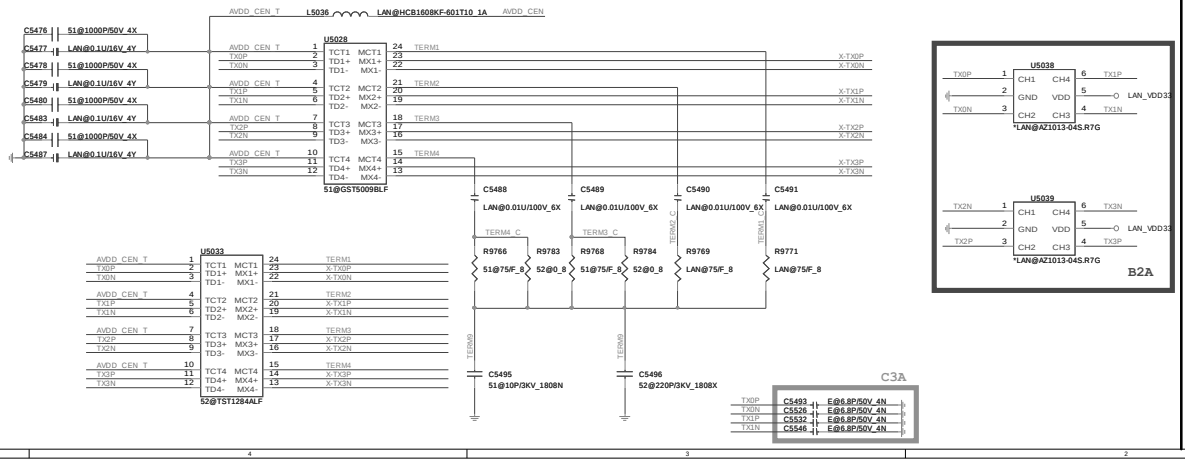
0.163A(20mils)



PLACE NEAR LAN IC SIDE <LAN/LN1.LNG>



TRANSFORMER <LAN/LN1.LNG>



LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

Power on Strapping pin

Quanta Computer Inc.
PROJECT : BLG
Size: Document Number: Atheros Lan
Rev: A1A
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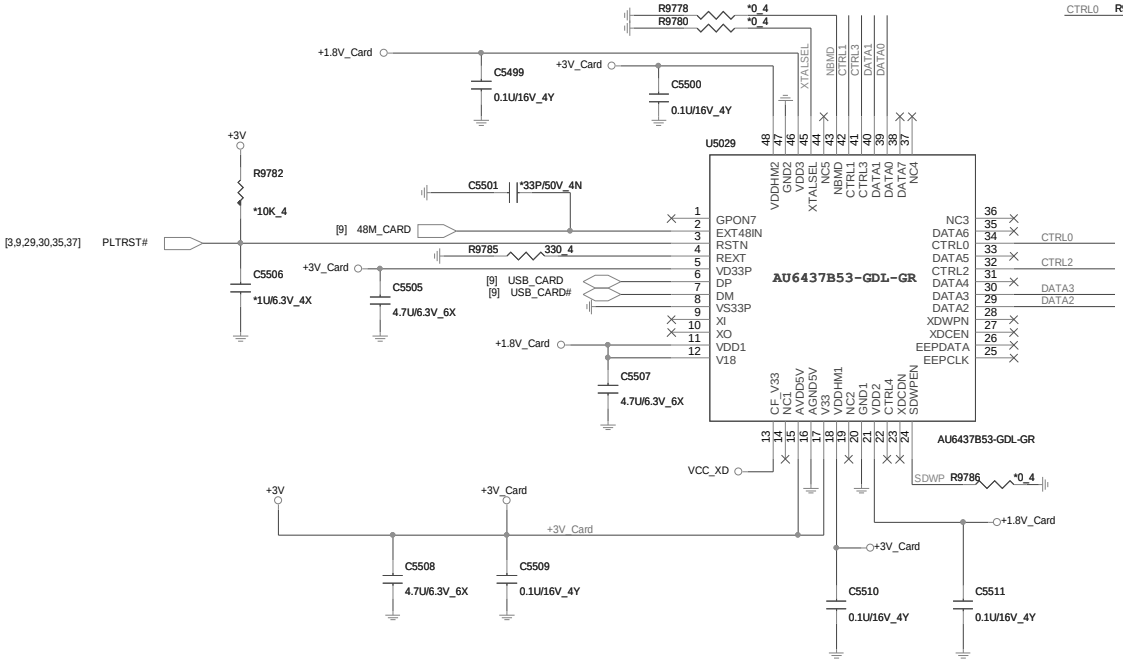
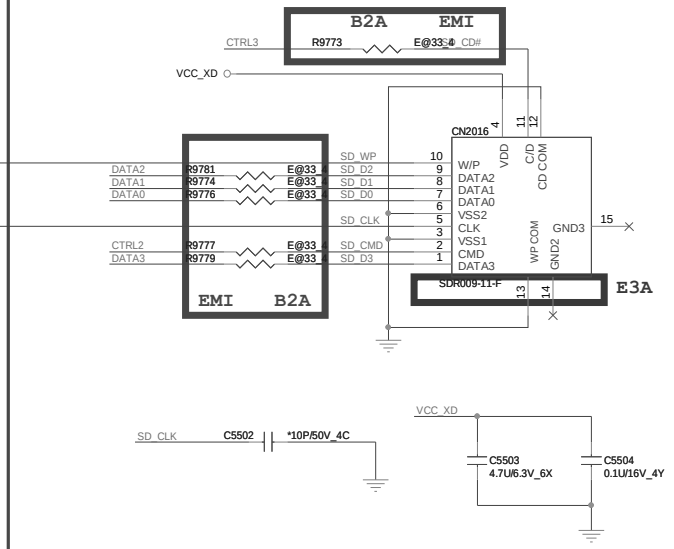
Card Reader (AU6437B53-GDL-GR) <MMC>



CTRL1 R9772 BLM15BD121SN1D_300MA

CTRL0 R9775 BLM15BD121SN1D_300MA

2 IN 1 Card Reader <MMC>



SDWPEN (SD write protect enable) 1 : decided by SDWP(default) 0 : SD always write-able
NBMD (Power saving mode enable) 1 : enable (default) 0 : disable
XTALSEL (Clock input selection) 1 : 48MHz input (default) 0 : 12MHz input

Quanta Computer Inc.

PROJECT : Chief River

Size	Document Number	Rev
	Card Reader(AU6437)	A1A

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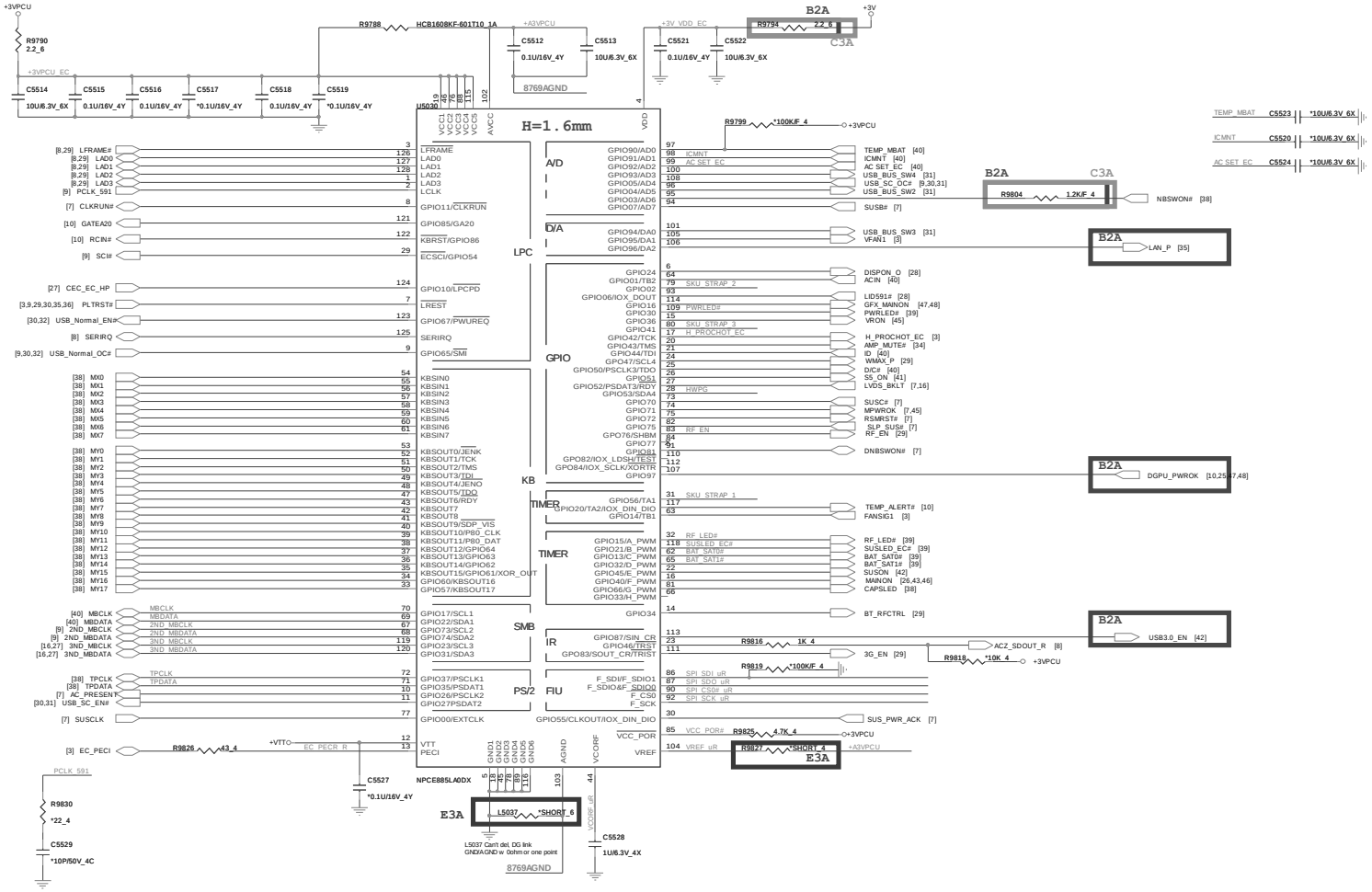
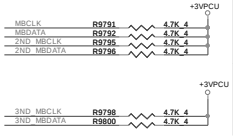
EC<KBC>

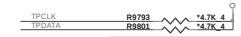


SM BUS <KBC> PU/Address

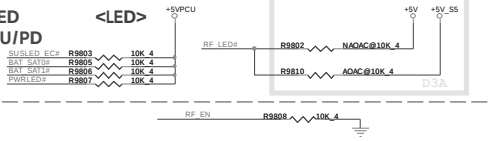


SMBUS	Devices	Address
1	Battery(A)	
2	PCH(S5)	
	G-sensor(S0)	
	CPU Thermal(A)	98H
	IDROM(A)	
3	VGA Thermal(A or S0)	98H
	CEC(A)	
	MMB(A)	

TP <KBC>

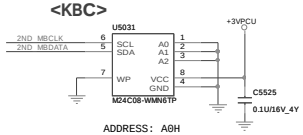


LED PU/PD <LED>



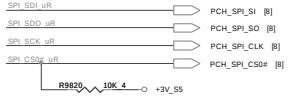
INTERNAL KEYBOARD STRIP SET <KBC>

ID EEPROM <KBC>

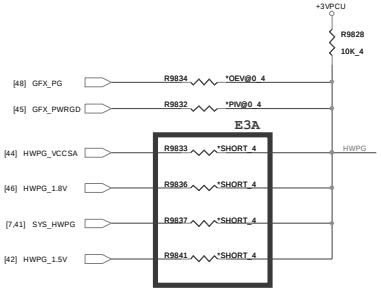


ADDRESS: A0H

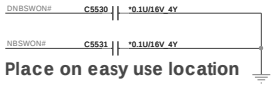
SPI FLASH <KBC>



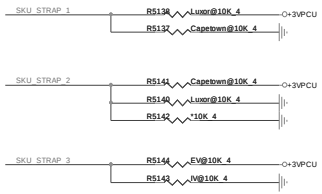
HWPG circuit <KBC>



Power Button <KBC>



Place on easy use location



MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3
	Capetown@/Luxor@	EV@ / IV@	
13'' UMA	0	0	0
13'' DIS	0	0	1
14'' Capetown UMA	0	1	0
14'' Capetown DIS	0	1	1
14'' Luxor UMA	1	0	0
14'' Luxor DIS	1	0	1

Quanta Computer Inc.

PROJECT : Chief River

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	EC-NPCE885L	A1A

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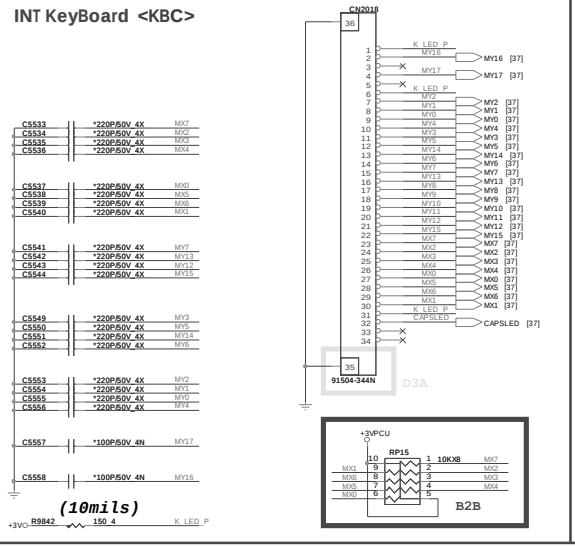
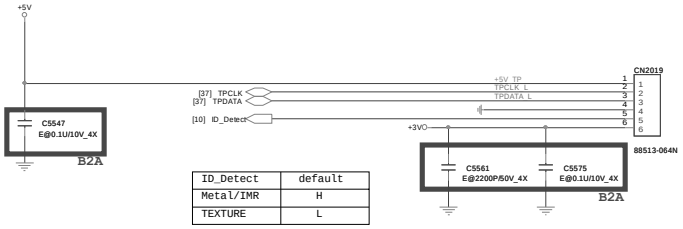
INT KeyBoard <KBC>

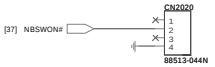


TP board <TPD>

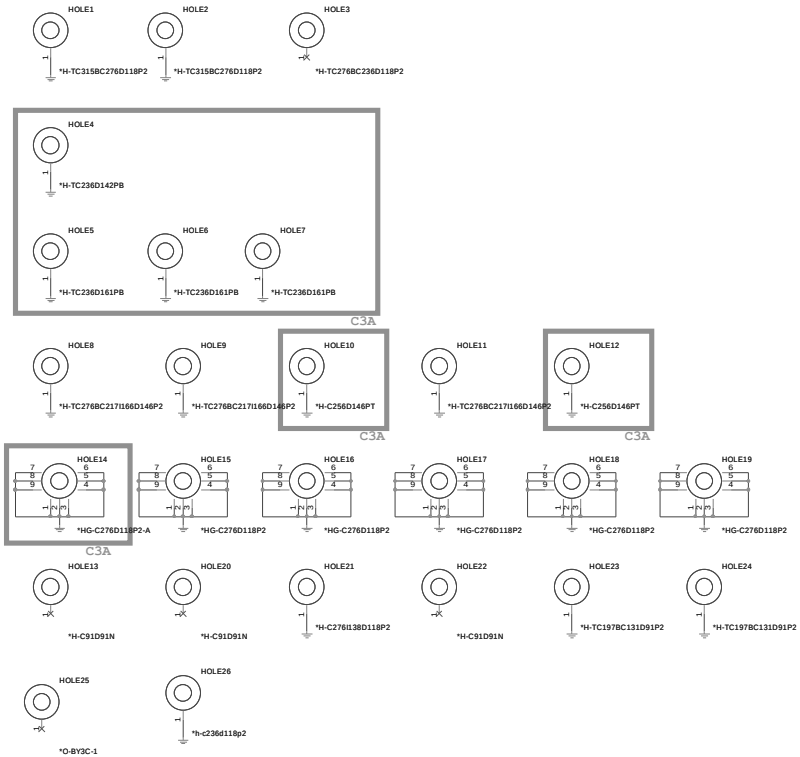


ID_Detect	default
Metal/IMR	H
TEXTURE	L

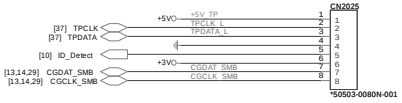
Power board w LED <PSW>



HOLE



TP board <TPD>



Quanta Computer Inc.

PROJECT : Chief River

Size	Document Number	Rev
	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	A1A

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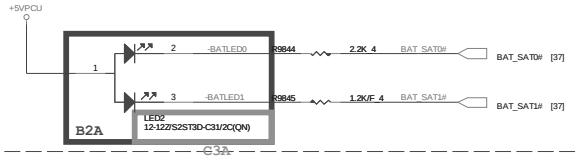
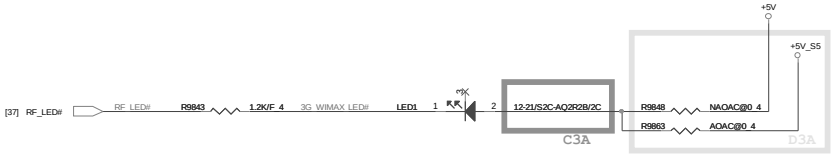
LED LED

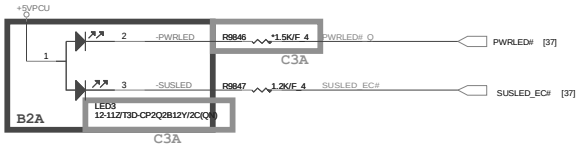
BATERRY



RF LED LED

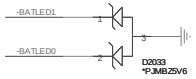


POWER LED

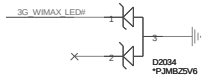


ESD Protect LED

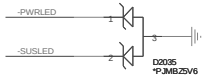
FOR BATTERY LED



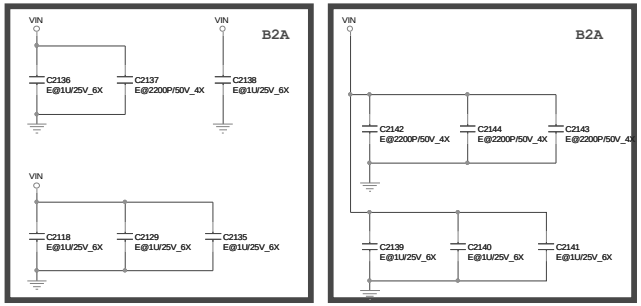
FOR W-LAN LED

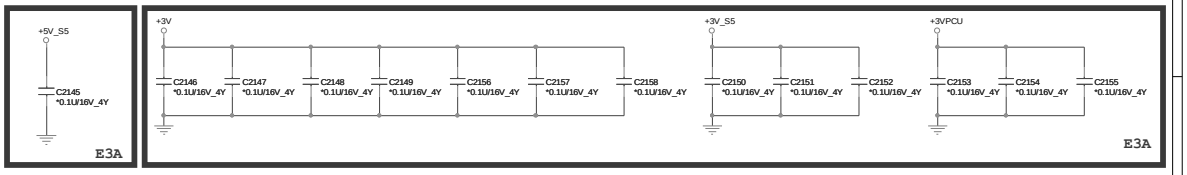


FOR Power LED



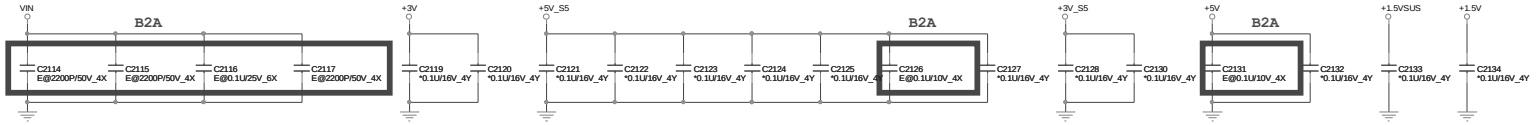
EMI EMI





(13644,1700) (2776,6392) (3884,6592) (13254,5454) (13054,1828) (4664,6694) (5201,6650) (13333,5677)

(2702,5916) (3534,5878) (6949,6677) (7361,6182) (7047,5660) (7807,5563)



Quanta Computer Inc.

PROJECT : Chief River

Size	Document Number	Rev
	LED/EMI/Green CLK	A1A

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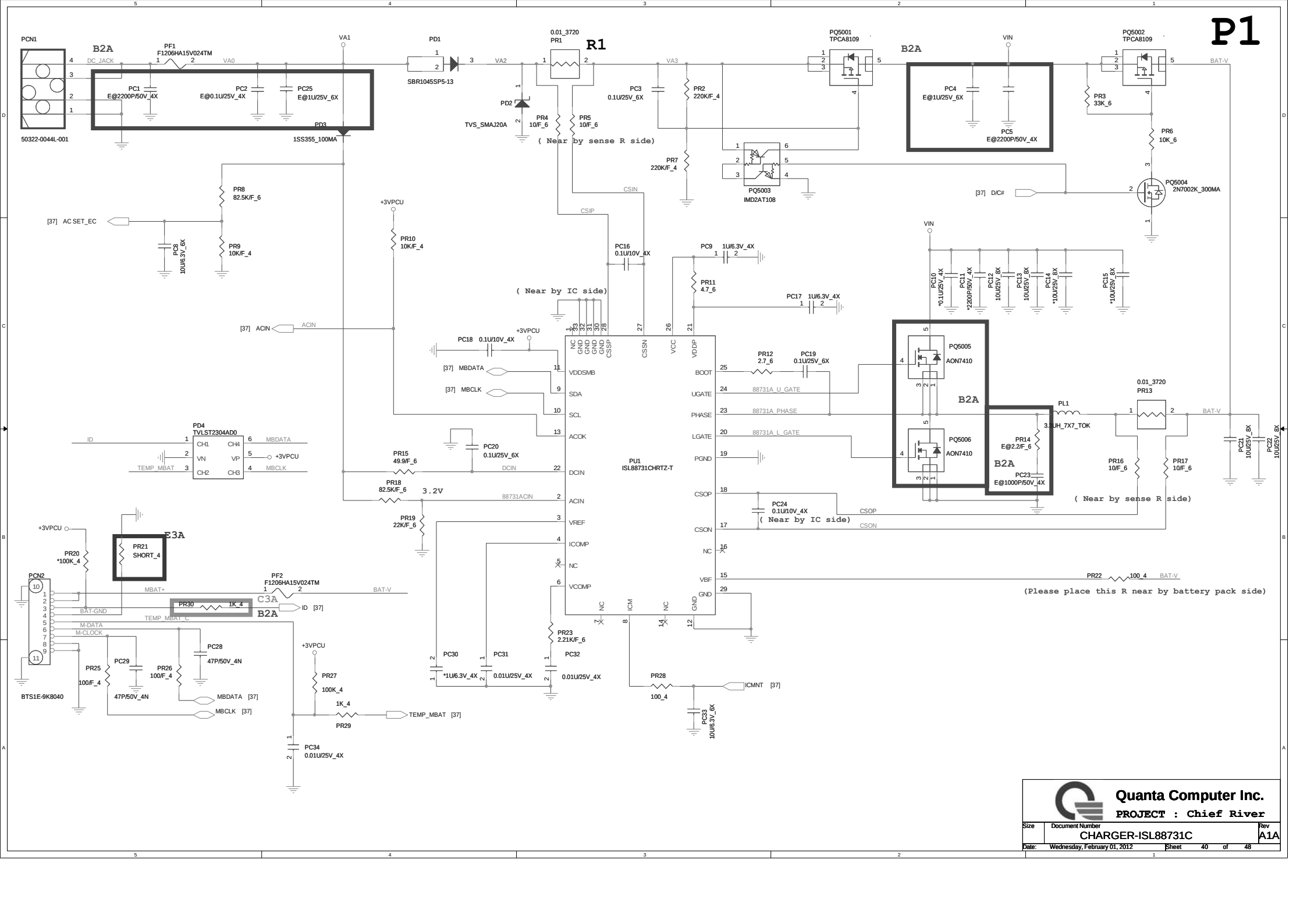
P1
PU1
ISL88731CHRTZ-T
R1
PCN1
50322-0044L-001
PF1
F1206HA15V024TM
PD1
SBR1045SP5-13
PD2
TVS_SMAJ20A
PD3
1SS355_100MA
PQ5001
TPCA8109
PQ5002
TPCA8109
PQ5003
IMD2AT108
PQ5004
2N7002K_300MA
PQ5005
AON7410
PQ5006
AON7410
PL1
3.3UH_7X7_TOK
PD4
TVLST2304AD0
PCN2
BTS1E-9K8040
PF2
F1206HA15V024TM
(Near by sense R side)
(Near by IC side)
(Please place this R near by battery pack side)
B2A
C3A
E3A
Quanta Computer Inc.
PROJECT : Chief River
CHARGER-ISL88731C
Wednesday, February 01, 2012
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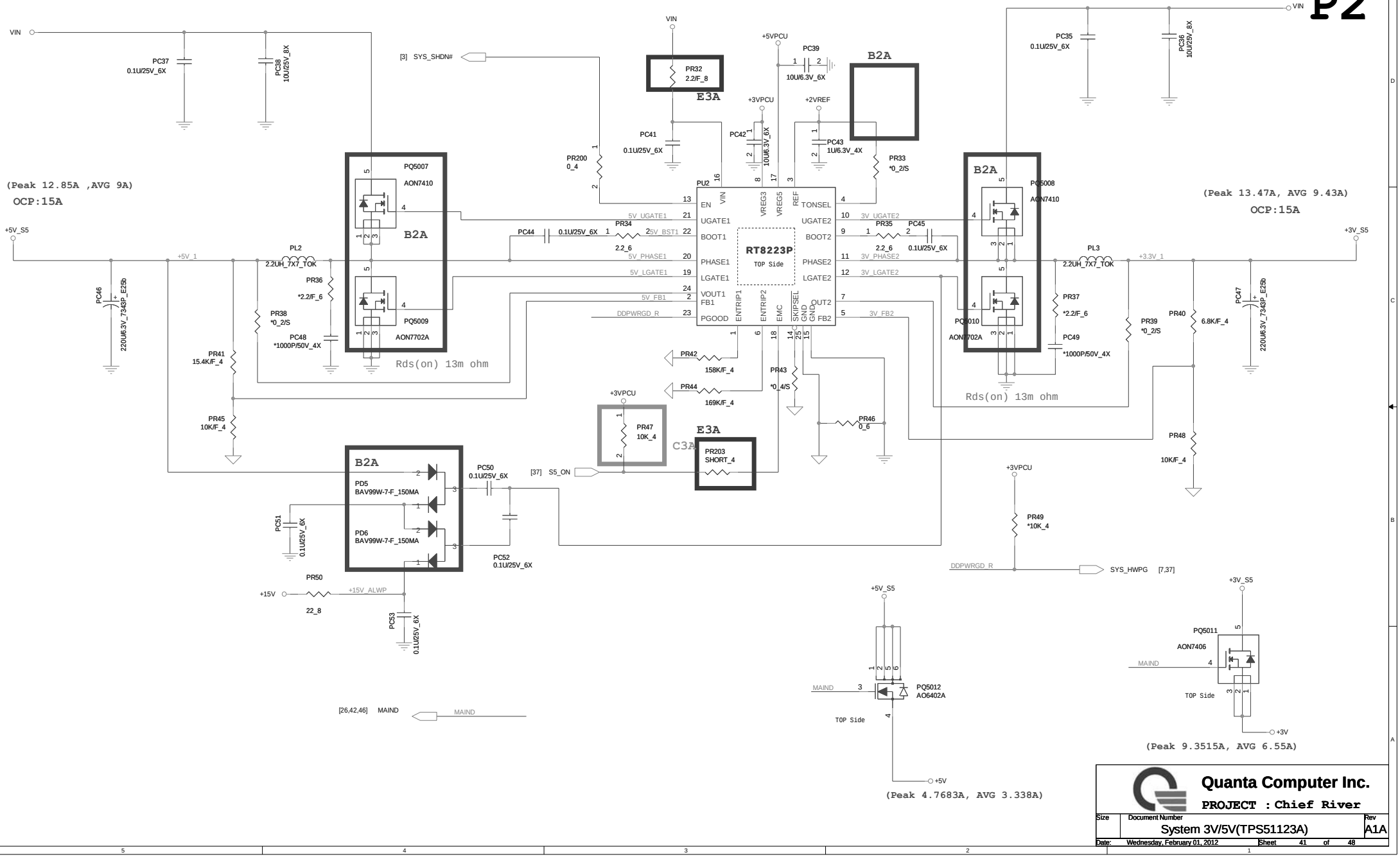
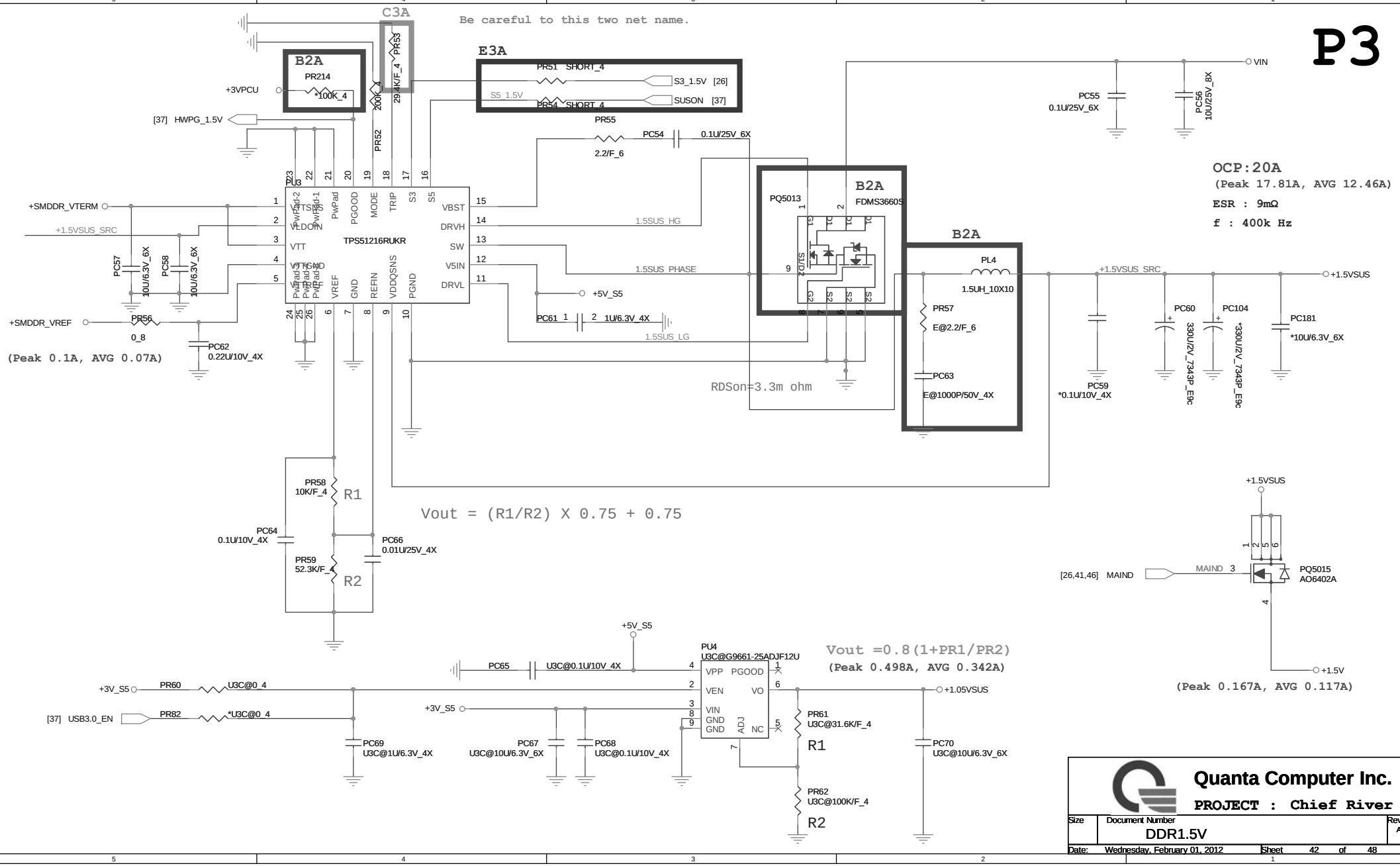
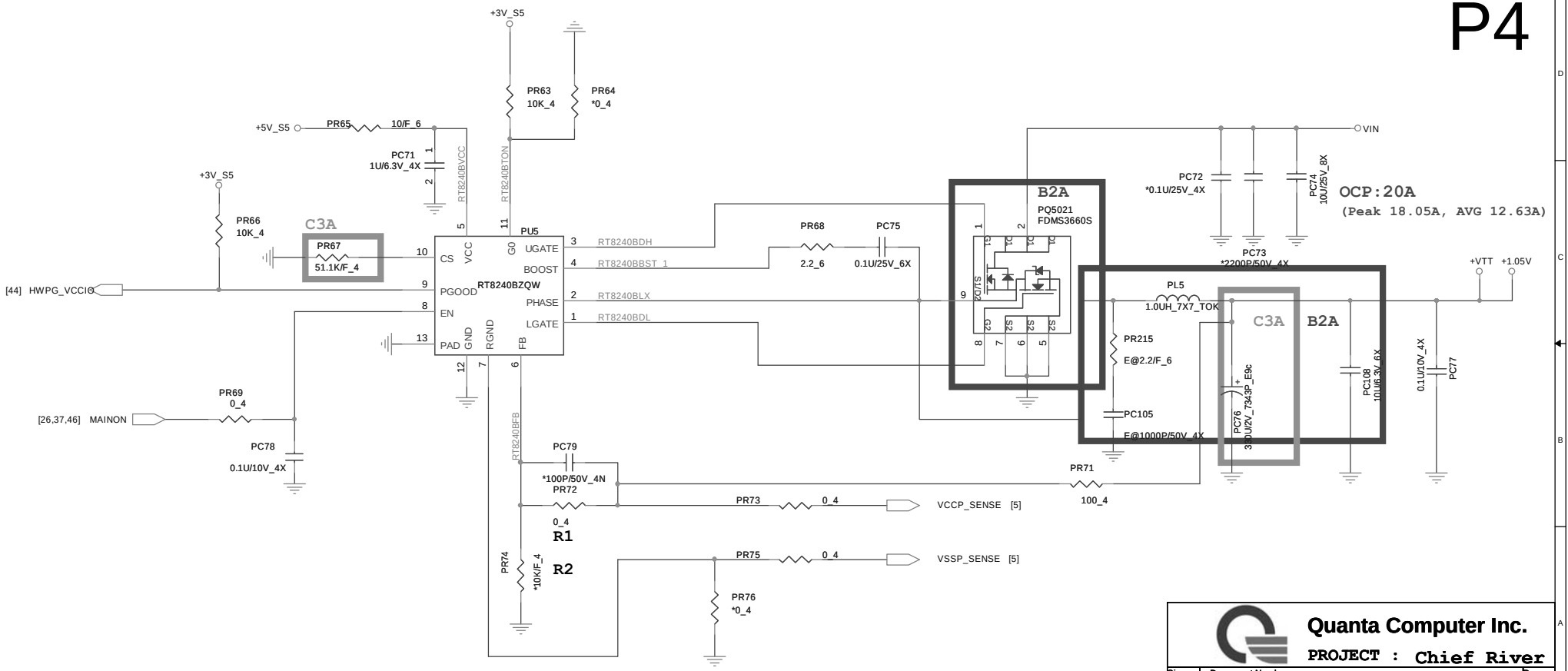
A1A


P2
VIN
PC37 0.1U/25V_6X
PC38 10U/25V_8X
[3] SYS_SHDN#
PR32 2.2/F_8
E3A
PC41 0.1U/25V_6X
PR200 0_4
+5VPCU
PC39 10U/6.3V_6X
B2A
+3VPCU
PC42 10U/6.3V_6X
+2VREF
PC43 1U/6.3V_4X
PR33 *0_2/S
PC35 0.1U/25V_6X
PC36 10U/25V_8X
(Peak 12.85A ,AVG 9A)
OCP:15A
PQ5007
AON7410
B2A
PU2
RT8223P
TOP Side
EN
VIN
VREG3
VREG5
REF
TONSEL
UGATE1
BOOT1
PHASE1
LGATE1
VOUT1
FB1
PGOOD
ENTRIP1
ENTRIP2
EMC
SKIPSEL
GND
GND
UGATE2
BOOT2
PHASE2
LGATE2
OUT2
FB2
5V_UGATE1
5V_BST1
5V_PHASE1
5V_LGATE1
5V_FB1
DDPWRGD_R
3V_UGATE2
3V_PHASE2
3V_LGATE2
3V_FB2
PC44 0.1U/25V_6X
PR34 2.2_6
PR35 2.2_6
PC45 0.1U/25V_6X
PQ5008
AON7410
B2A
(Peak 13.47A, AVG 9.43A)
OCP:15A
+5V_S5
+5V_1
PL2 2.2UH_7X7_TOK
PR36 *2.2/F_6
PR38 *0_2/S
PC48 *1000P/50V_4X
PC46 220U/6.3V_7343P_E25b
PR41 15.4K/F_4
PR45 10K/F_4
PQ5009
AON7702A
Rds(on) 13m ohm
PR42 158K/F_4
PR44 169K/F_4
PR43 *0_4/S
PR46 0_6
PQ5010
AON7702A
Rds(on) 13m ohm
PL3 2.2UH_7X7_TOK
+3.3V_1
PR37 *2.2/F_6
PC49 *1000P/50V_4X
PR39 *0_2/S
PR40 6.8K/F_4
PC47 220U/6.3V_7343P_E25b
+3V_S5
+3VPCU
PR47 10K_4
E3A
C3A
PR203 SHORT_4
PR48 10K/F_4
B2A
PD5 BAV99W-7-F_150MA
PD6 BAV99W-7-F_150MA
PC50 0.1U/25V_6X
[37] S5_ON
PC51 0.1U/25V_6X
PC52 0.1U/25V_6X
PR50 22_8
+15V
+15V_ALWP
PC53 0.1U/25V_6X
+3VPCU
PR49 *10K_4
DDPWRGD_R
SYS_HWPG [7,37]
+5V_S5
MAIND
PQ5012
AO6402A
TOP Side
+5V
(Peak 4.7683A, AVG 3.338A)
+3V_S5
PQ5011
AON7406
MAIND
TOP Side
+3V
(Peak 9.3515A, AVG 6.55A)
[26,42,46] MAIND
MAIND
Quanta Computer Inc.
PROJECT : Chief River
Size
Document Number
System 3V/5V(TPS51123A)
Rev
A1A
Date: Wednesday, February 01, 2012
Sheet 41 of 48


P3
C3A
Be careful to this two net name.
B2A
PR214
*100K_4
+3VPCU
[37] HWPG_1.5V
PR53
29.4K/F_4
200K_4
PR52
E3A
PR51 SHORT_4
S5_1.5V
PR54 SHORT_4
S3_1.5V [26]
SUSON [37]
PR55
2.2/F_6
PC54 0.1U/25V_6X
VIN
PC55 0.1U/25V_6X
PC56 10U/25V_8X
OCP:20A
(Peak 17.81A, AVG 12.46A)
ESR : 9mΩ
f : 400k Hz
PU3
TPS51216RUKR
+SMDDR_VTERM
+1.5VSUS_SRC
+SMDDR_VREF
PC57 10U/6.3V_6X
PC58 10U/6.3V_6X
PR56 0_8
PC62 0.22U/10V_4X
(Peak 0.1A, AVG 0.07A)
1.5SUS_HG
1.5SUS_PHASE
1.5SUS_LG
+5V_S5
PC61 1U/6.3V_4X
B2A
PQ5013
FDMS3660S
B2A
PL4
1.5UH_10X10
PR57
E@2.2/F_6
PC63
E@1000P/50V_4X
RDSon=3.3m ohm
+1.5VSUS_SRC
+1.5VSUS
PC59
*0.1U/10V_4X
PC60
330U/2V_7343P_E9c
PC104
*330U/2V_7343P_E9c
PC181
*10U/6.3V_6X
PR58
10K/F_4
R1
PC64
0.1U/10V_4X
PC66
0.01U/25V_4X
PR59
52.3K/F_4
R2
Vout = (R1/R2) X 0.75 + 0.75
+1.5VSUS
[26,41,46] MAIND
MAIND
PQ5015
AO6402A
+1.5V
(Peak 0.167A, AVG 0.117A)
+5V_S5
PU4
U3C@G9661-25ADJF12U
PC65 U3C@0.1U/10V_4X
+3V_S5
PR60 U3C@0_4
[37] USB3.0_EN
PR82 *U3C@0_4
PC69 U3C@1U/6.3V_4X
PC67 U3C@10U/6.3V_6X
PC68 U3C@0.1U/10V_4X
Vout =0.8(1+PR1/PR2)
(Peak 0.498A, AVG 0.342A)
+1.05VSUS
PR61 U3C@31.6K/F_4
R1
PR62 U3C@100K/F_4
R2
PC70 U3C@10U/6.3V_6X
Quanta Computer Inc.
PROJECT : Chief River
Size
Document Number
DDR1.5V
Rev
A1A
Date: Wednesday, February 01, 2012
Sheet 42 of 48

P4



VOUT=(1+R1/R2)*0.5

Quanta Computer Inc.		
PROJECT : Chief River		
Size	Document Number: +VCCIO(RT8240BGQW)	Rev: A1A
Date: Wednesday, February 01, 2012	Sheet 43 of 48	

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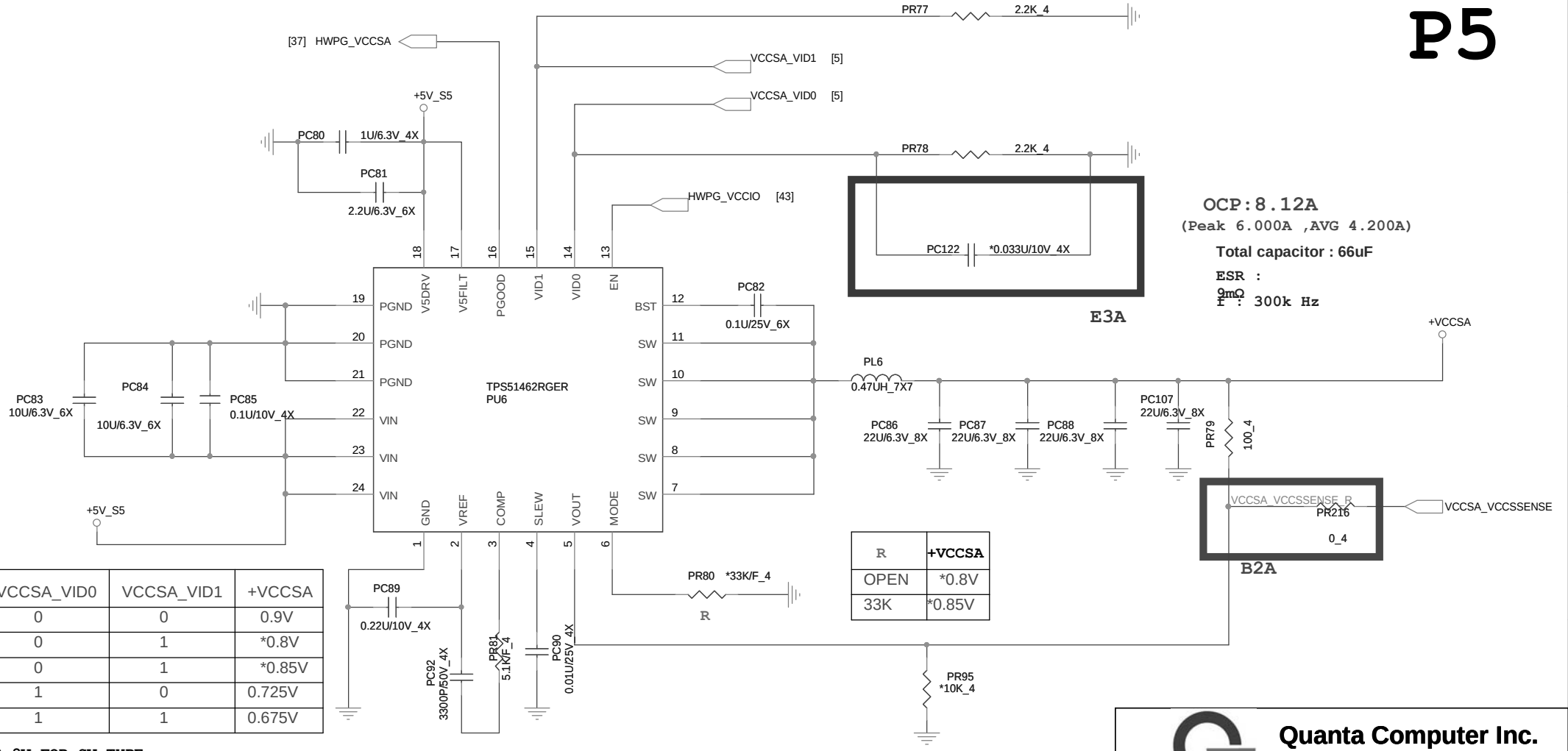


R	+VCCSA
OPEN	*0.8V
33K	*0.85V

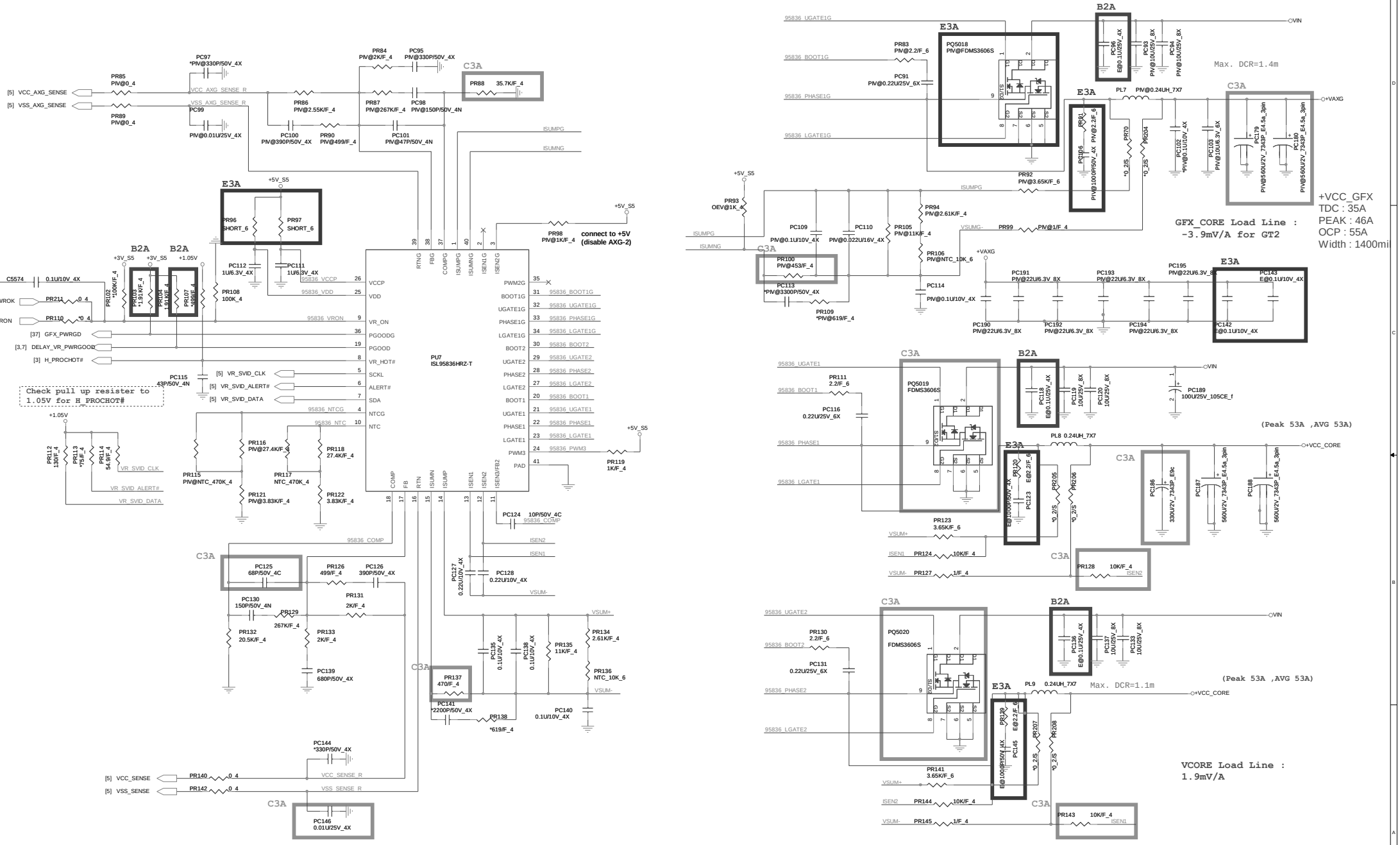
VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.9V
0	1	*0.8V
0	1	*0.85V
1	0	0.725V
1	1	0.675V

*0.8V FOR SV TYPE
*0.85V FOR LV/ULV TYPE

Quanta Computer Inc.

PROJECT : Chief River

Size	Document Number	Rev
	+VCCSA(TI51461)	A1A
Date: Wednesday, February 01, 2012	Sheet 44 of 48	



Quanta Computer Inc.		
PROJECT : Chief River		
Size	Document Number: +VCC_CORE+VGFX (ISL95836) 35W	Rev: A1A
Date: Wednesday, February 01, 2012	Sheet 45 of 48	

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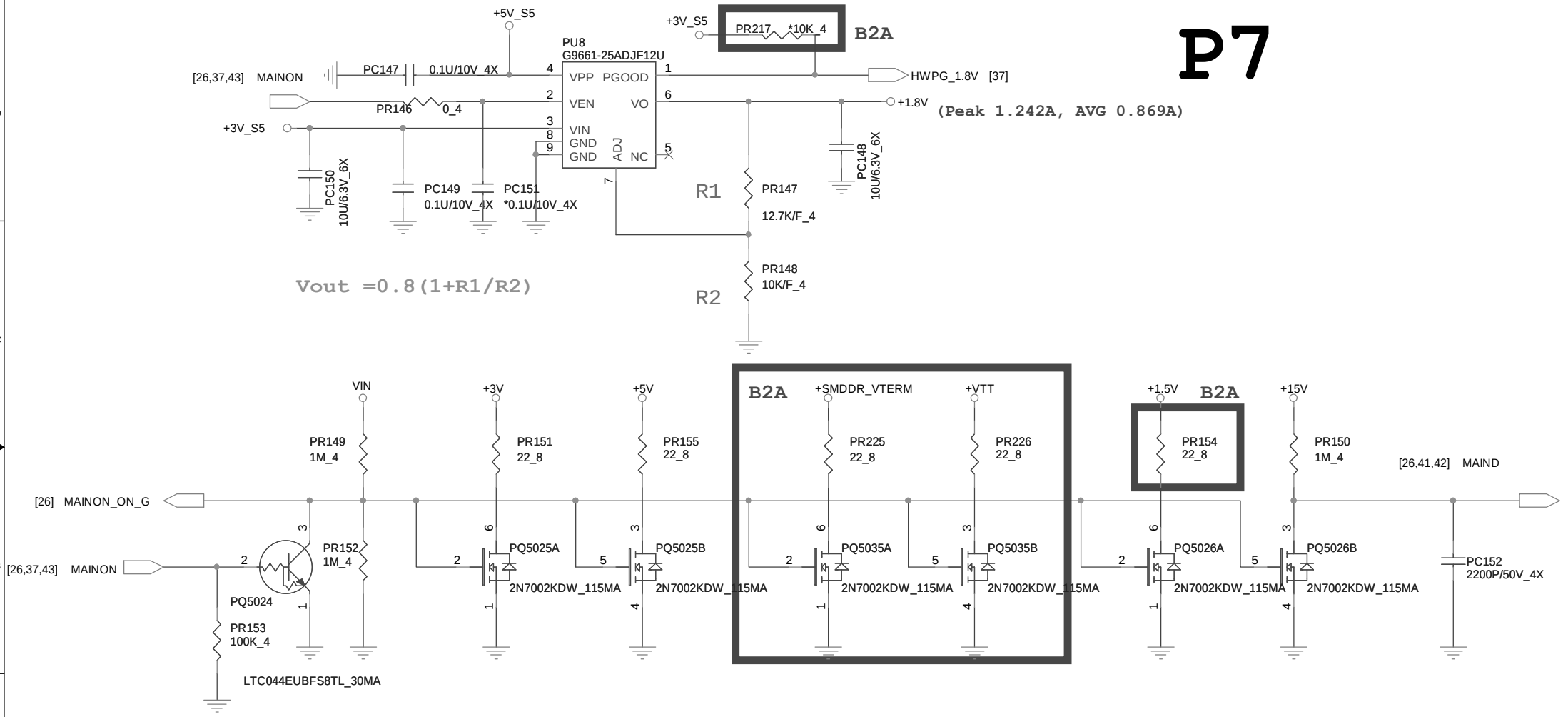

Quanta Computer Inc.

PROJECT :Chief River

Size	Document Number	Rev
	+1.8V/Discharge	A1A

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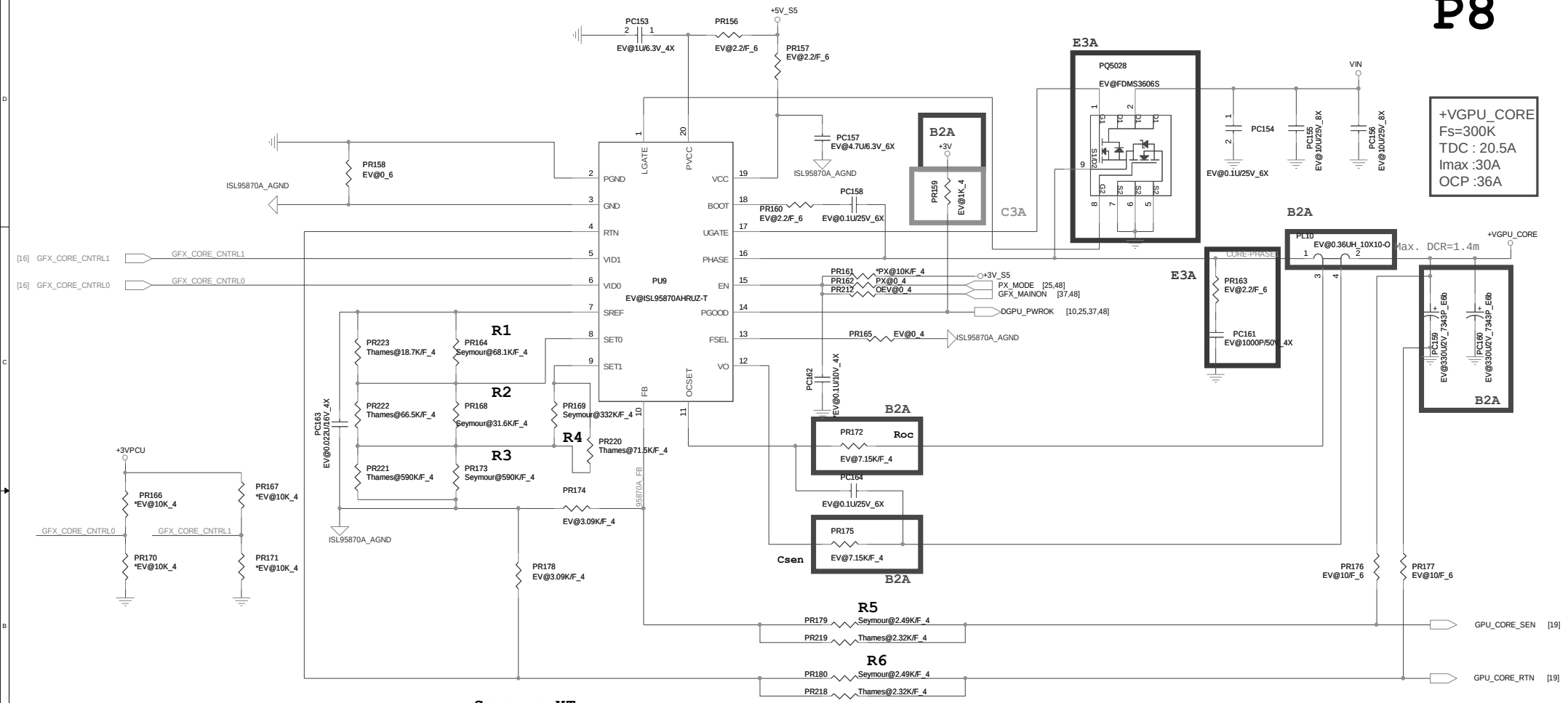

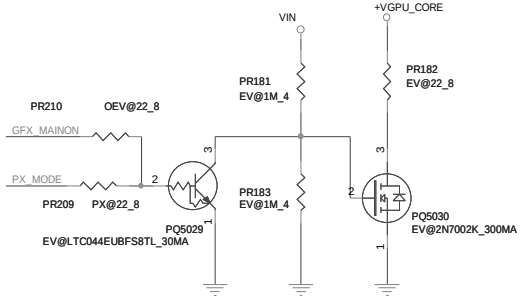

Seymous XT

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	1V
0	1	1.05V
0	0	1.15V

Thames XT

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.875V
1	0	0.9V
0	1	1V
0	0	1V

	Seymous XT	Thames XT
R1	68.1K	18.7K
R2	31.6K	66.5K
R3	590K	590K
R4	332K	71.5K
R5	2.49K	2.32K
R6	2.49K	2.32K

Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	GPU Core (ISL62881C)	A1A

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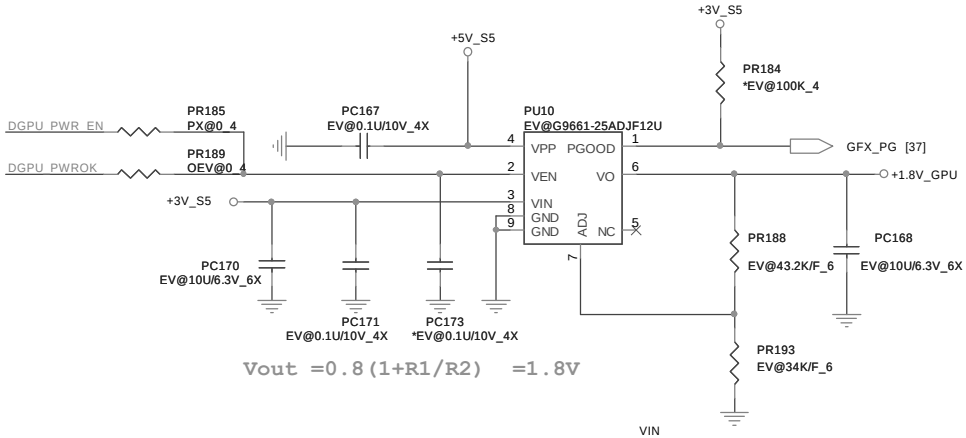
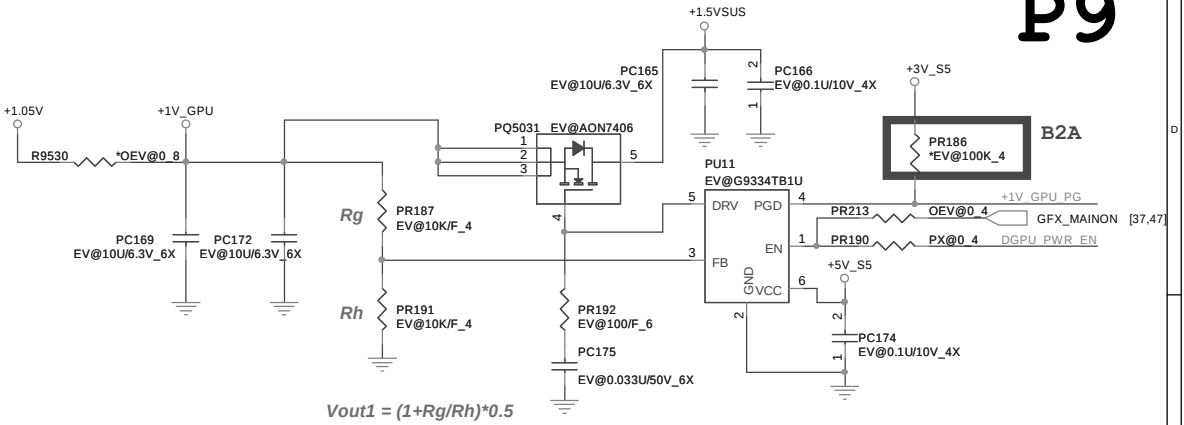
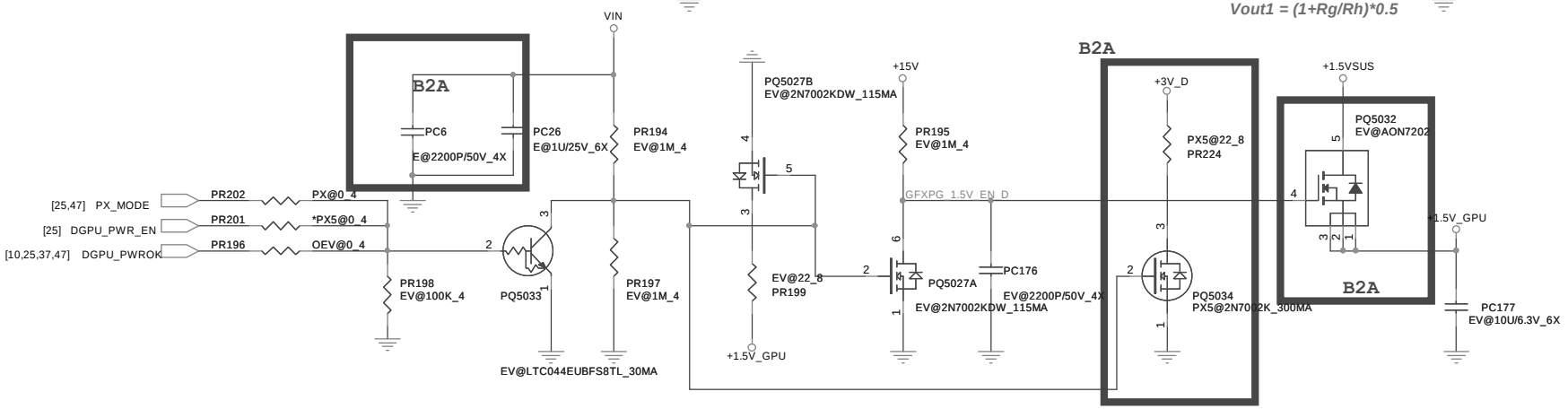




(Peak 6.000A ,AVG 4.200A)

Total capacitor : 22uF



Power On Sequence
1. +3V_GPU connect +3V
2.PX_PWRGOOD Enable +VGPU_CORE
3.DGPU_PWROK Enable(Delay) +1.8V_GFX
4. DGPU_PWR_EN Enable(Delay) +1.5V_GFX
5.DGPU_PWR_EN Enable(Delay) +1V_GFX

Quanta Computer Inc.

PROJECT : Chief River

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	+VGACORE	A1A
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CHANGE LIST

Model	REV	
BY3/BY4	1A	PAGE 8: Dual SPI ROM circuit modify for Win8.
		PAGE 8: C2010 change value to 15P/C2013 change value to 12P.
		PAGE 9: SMBUS/CLK REQ pin PU/PD resister pallerel resister to single resister.
		PAGE 10: R2185 change power to +3V.
		PAGE 10: R2160 MB_ID9 change to GPIO34.
		PAGE 16/28: d-GPU CRT Port change from Port6 to Port3.
		PAGE 17: C5045/C5049 change to 22P.
		PAGE 25: Del PX Mode PERST#_BUF double drawing.
		PAGE 30: C5345/C5348 change value to 22P.
		PAGE 31: Add RN12/RN13 CHOCK for EMI test..
		PAGE 32: Add RN11/RN6 CHOCK for EMI test..
		PAGE 34: Stuff C5438/C5439/C5440/C5441 for EMI test.
		PAGE 35: Reserve LAN power circuit.
		PAGE 36: r9781/r9774/r9776/r9777/r9779/r9733 to 33ohm for EMI test.
		PAGE 37: Reserve GPIO for USB3.0 Power enable/LAN power/Inform VGA power status.
		PAGE 39: LED3 change to single white color for PRD1.0
		PAGE 39: Add C2136/C2137/C2138/C2118/C2129/C2135/C2142/C2144/C2143/C2139/C2140/C2141 for EMI test.

MODEL TE5

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 204

PROJECT MODEL :	BY3,BY4	APPROVED BY:		DATE:	
PART NUMBER:		DRAWING BY:		REVISON:	

Quanta Computer Inc.

PROJECT : BY3,BY4

Size | Document Number: Change list | Rev: 1A

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