KL3A Intel Calpella Platform with Discrete GFX(4 core)

01

POWER

- BATT CHARGER — PG 40
- AC/BATT CONNECTOR — PG 40
- RUN POWER SW — 3VSUS, 5VSUS, 3V_S5, 5V_S5, +3V, +5V — PG 43
- Discharge — PG 39

FAN / THERMAL
FAN G993P1U
THERMAL EMC2103-2 PG 34

14.318MHz

CLOCK GEN
ICS9LPRS365BGLFT
PG 3

POWER

- REGULATOR +1.1V_VTT — PG 42
- REGULATOR (DDR3) 1.5VSUS, SMDDR_VREF,1.5V — PG 41
- REGULATOR +1.8V — PG 46
- REGULATOR +1.05V_PCH — PG 49
- CPU Core — PG 44,45
- DC/DC 3VPCU, 5VPCU, +15V — PG 43
- VGA Core Discrete — PG 47,48

DDRIII-SODIMM1 PG 14
DDRIII-SODIMM2 PG 15

Dual Channel DDR3
800/1067 1.5V

DDR SYSTEM MEMORY

Auburndale (UMA+VGA) / Clarksfield (VGA)

rPGA 989

Graphics Interfaces

PCI-E

PG 4,5,6,7

FDI DMI

PCI-Express *16X*

AMD (40nm)
Medison XT 128 Bit
969p
PG 16,17,18,19,20,21,22

27MHz

HDMI CON PG 23

EXT_HDMI EXT_CRT

LVDS_CRT_HDMI Switch Grapgics PG 23

CRT PG 25

LCD CONN PG 24

INT_CRT
INT_LVDS

DMIX4

32.768KHz

FDI DMI

Ibex Peak-M
PCH
PG 8,9,10,11,12,13

- SATA - HDD — PG 28 — SATA0 150MB
- SATA - CD-ROM — PG 28 — SATA1 150MB
- USB+eSATA — PG 28 — SATA4 150MB / USB2.0 0
- SPI BIOS ME — PG 9 — SPI

USB2.0

- 1,8,9 — USB2.0 Ports X3 — PG 29
- 13 — BlueTooth — PG 29
- 4,5,11 — Mini PCI-E Card X 3 Express Card — PG 31,32
- 2 — Express Card (NEW CARD) — PG 33

PCI-E

- X1 — LAN — Broadcom (10/100/1G LAN) BCM57780 — PAGE 26
- X2 — Mini PCI-E Card (WLAN/ WWAN) — PAGE 31
- X1 — Express Card (NEW CARD) — PAGE 33
- X1 — Card Reader JMB387 — PAGE 30
- X1 — Mini PCI-E Card (TV) — PAGE 32

25MHz

24.576MHz

RJ45 CONN PG 26

5-IN-1 Card Reader CONN PG 30

- Speaker — PG 27
- Audio Jack (External MIC) — PG 27
- Head-Phone Jack + SPDIF — PG 27

AUDIO CODEC ALC272 — PG 27 — IHDA

Camera + D-MIC PG 24 — USB2.0 3

LPC

32.768KHz

- Touch Pad — PG 35 — PS/2
- Keyboard — PG 35

EC
IT8512E
PAGE 37

SPI

SPI BIOS EC — PG 37

PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Wednesday, December 23, 2009 Sheet 1 of 53

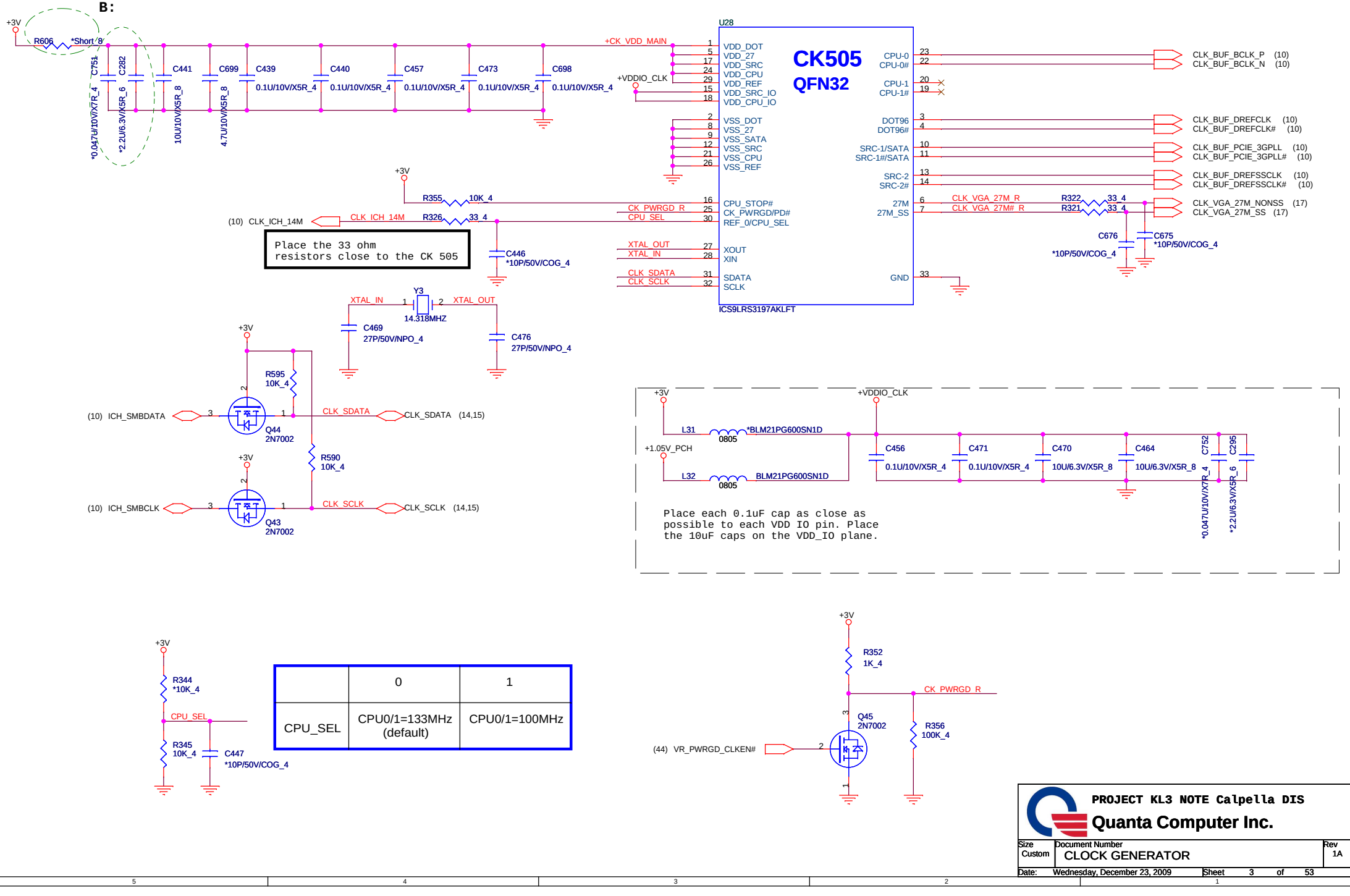
Table of Contents

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	23,32,43,44,45,46,47,48,49,50	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	9,12,41	RTC		S0~S5
3VPCU	+3.3V	9,23,27,30,32,35,39,41,43,44,47	ITE8052 POWER	3V5V_EN	S0~S5
5VPCU	+5V	14,43,44,45,46,47,49,50	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	23,38,43,45,46,47	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	27,43	LAN POWER	LAN_ON	
5V_S5	+5V	12,29,30,43	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	8,9,10,11,12,43,52	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	23,39,43,48	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	14,15,30,34,41,43,49	SLP_S4# CTRLD POWER	SUSON	S0~S3
1.5VSUS	+1.5V	4,6,14,15,43,45,46,49,50	SODIMM POWER	SUSON	S0~S3
0.75VSMDDR_VTERM	+0.75V	14,15,43,45	DDR3 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,18,23,24,25,26,28,35,37,41,43,44	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,8,9,10,11,12,14,15,17,23,25,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41,43,44,45,46,47,48,50,52	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,12,17,18,21,22,33,43,50	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	12,18,19,20,31,32,34,45,46	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V_VTT	+1.05V	4,6,11,12,43,46,48,52	AuBurndale VTT POWER	MAIN_ON	S0
+1.05V_PCH	+1.05V	3,10,12,43,46,52	PCH CORE POWER	1.05V_RUN_ON	S0
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,43,49	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		6,43,48	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	23	LCD Power	ENVDD	S0
+5V_ODD	+5V	28	ODD Power	MAIN_ON	S0
+5V_HDD	+5V	28	HDD Power	MAIN_ON	S0
BAT-V	+10V~+17V	44	MAIN BATTERY	CHG_PBATT	S0~S5

(4,8,9,10,11,12,14,15,18,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,44,47) +3V
(8,9,10,12,39,49) +1.05V_PCH

B:



Place the 33 ohm resistors close to the CK 505

Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

Date: Wednesday, December 23, 2009 Sheet 3 of 53

AUBURNDALE PROCESSOR (DMI,PEG,FDI)

(3,8,9,10,11,12,14,15,18,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,44,47) +3V
(6,11,12,39,42,44,48) +1.05V_VTT
(14,15,39,41,47) 1.5VSUS

	Auburndale	Clarksfield
RP5	POP	DE-POP
R484	DE-POP	POP
R485	DE-POP	POP

U51A

DMI_RX#[0]
DMI_RX#[1]
DMI_RX#[2]
DMI_RX#[3]
DMI_TX#[0]
DMI_TX#[1]
DMI_TX#[2]
DMI_TX#[3]

DMI

2.7GT/s data rate

FDI_TX#[0]
FDI_TX#[1]
FDI_TX#[2]
FDI_TX#[3]
FDI_TX#[4]
FDI_TX#[5]
FDI_TX#[6]
FDI_TX#[7]
FDI_FSYNC[0]
FDI_FSYNC[1]
FDI_INT
FDI_LSYNC[0]
FDI_LSYNC[1]

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

IC,AUB_CFD_rPGA,R0P9

PEG_RXN[0..15] (16)
PEG_RXP[0..15] (16)
PEG_TXN[0..15] (16)
PEG_TXP[0..15] (16)

U51B

MISC THERMAL
CLOCKS
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM

CLK_CPU_BCLK (11)
CLK_CPU_BCLK# (11)
CLK_PCIE_3GPLL (10)
CLK_PCIE_3GPLL# (10)
DREFSSCLK (10)
DREFSSCLK# (10)

For S3 Power Saving

+1.05V_VTT

PM_EXTTS#0 (14)
PM_EXTTS#1 (15)

XDP_DBRESET# (8)

IC,AUB_CFD_rPGA,R0P9

	Auburndale	Clarksfield
R479	DE-POP	POP
R480	DE-POP	POP
R481	DE-POP	POP
R482	DE-POP	POP
R483	DE-POP	POP

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

For S3 Power Saving

EC GPIO

EC B01

For S3 Power Saving

For S3 Power Saving

JTAG MAPPING

Scan Chain (Default)	STUFF -> R421, R411, R422 NO STUFF -> R430, R429
CPU Only	STUFF -> R421, R430 NO STUFF -> R411, R429, R422
GMCH Only	STUFF -> R429, R422 NO STUFF -> R421, R430, R411

Processor Pullups

Processor Compensation Signals

DDR3 Compensation Signals

Layout Note: Place these resistors near Processor

PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PCI)	1A

Date: Wednesday, December 23, 2009 Sheet 4 of 53

AUBURNDALE PROCESSOR (DDR3)

05

U51C

DDR SYSTEM MEMORY A

IC,AUB_CFD_rPGA,R0P9

U51D

DDR SYSTEM MEMORY - B

IC,AUB_CFD_rPGA,R0P9

(14) M_A_DQ[63:0]

(15) M_B_DQ[63:0]

M_A_DQ0	A10	SA_DQ[0]	M_B_DQ0 B5 SB_DQ[0]
M_A_DQ1	C10	SA_DQ[1]	M_B_DQ1 A5 SB_DQ[1]
M_A_DQ2	C7	SA_DQ[2]	M_B_DQ2 C3 SB_DQ[2]
M_A_DQ3	A7	SA_DQ[3]	M_B_DQ3 B3 SB_DQ[3]
M_A_DQ4	B10	SA_DQ[4]	M_B_DQ4 E4 SB_DQ[4]
M_A_DQ5	D10	SA_DQ[5]	M_B_DQ5 A6 SB_DQ[5]
M_A_DQ6	E10	SA_DQ[6]	M_B_DQ6 A4 SB_DQ[6]
M_A_DQ7	A8	SA_DQ[7]	M_B_DQ7 C4 SB_DQ[7]
M_A_DQ8	D8	SA_DQ[8]	M_B_DQ8 D1 SB_DQ[8]
M_A_DQ9	F10	SA_DQ[9]	M_B_DQ9 D2 SB_DQ[9]
M_A_DQ10	E6	SA_DQ[10]	M_B_DQ10 F2 SB_DQ[10]
M_A_DQ11	F7	SA_DQ[11]	M_B_DQ11 F1 SB_DQ[11]
M_A_DQ12	E9	SA_DQ[12]	M_B_DQ12 C2 SB_DQ[12]
M_A_DQ13	B7	SA_DQ[13]	M_B_DQ13 F5 SB_DQ[13]
M_A_DQ14	E7	SA_DQ[14]	M_B_DQ14 F3 SB_DQ[14]
M_A_DQ15	C6	SA_DQ[15]	M_B_DQ15 G4 SB_DQ[15]
M_A_DQ16	H10	SA_DQ[16]	M_B_DQ16 H6 SB_DQ[16]
M_A_DQ17	G8	SA_DQ[17]	M_B_DQ17 G2 SB_DQ[17]
M_A_DQ18	K7	SA_DQ[18]	M_B_DQ18 J6 SB_DQ[18]
M_A_DQ19	J8	SA_DQ[19]	M_B_DQ19 J3 SB_DQ[19]
M_A_DQ20	G7	SA_DQ[20]	M_B_DQ20 G1 SB_DQ[20]
M_A_DQ21	G10	SA_DQ[21]	M_B_DQ21 G5 SB_DQ[21]
M_A_DQ22	J7	SA_DQ[22]	M_B_DQ22 J2 SB_DQ[22]
M_A_DQ23	J10	SA_DQ[23]	M_B_DQ23 J1 SB_DQ[23]
M_A_DQ24	L7	SA_DQ[24]	M_B_DQ24 J5 SB_DQ[24]
M_A_DQ25	M6	SA_DQ[25]	M_B_DQ25 K2 SB_DQ[25]
M_A_DQ26	M8	SA_DQ[26]	M_B_DQ26 L3 SB_DQ[26]
M_A_DQ27	L9	SA_DQ[27]	M_B_DQ27 M1 SB_DQ[27]
M_A_DQ28	L6	SA_DQ[28]	M_B_DQ28 K5 SB_DQ[28]
M_A_DQ29	K8	SA_DQ[29]	M_B_DQ29 K4 SB_DQ[29]
M_A_DQ30	N8	SA_DQ[30]	M_B_DQ30 M4 SB_DQ[30]
M_A_DQ31	P9	SA_DQ[31]	M_B_DQ31 N5 SB_DQ[31]
M_A_DQ32	AH5	SA_DQ[32]	M_B_DQ32 AE3 SB_DQ[32]
M_A_DQ33	AE5	SA_DQ[33]	M_B_DQ33 AG1 SB_DQ[33]
M_A_DQ34	AK6	SA_DQ[34]	M_B_DQ34 AJ3 SB_DQ[34]
M_A_DQ35	AK7	SA_DQ[35]	M_B_DQ35 AK1 SB_DQ[35]
M_A_DQ36	AF6	SA_DQ[36]	M_B_DQ36 AG4 SB_DQ[36]
M_A_DQ37	AG5	SA_DQ[37]	M_B_DQ37 AG3 SB_DQ[37]
M_A_DQ38	AJ7	SA_DQ[38]	M_B_DQ38 AJ4 SB_DQ[38]
M_A_DQ39	AJ6	SA_DQ[39]	M_B_DQ39 AH4 SB_DQ[39]
M_A_DQ40	AJ10	SA_DQ[40]	M_B_DQ40 AK3 SB_DQ[40]
M_A_DQ41	AJ9	SA_DQ[41]	M_B_DQ41 AK4 SB_DQ[41]
M_A_DQ42	AL10	SA_DQ[42]	M_B_DQ42 AM6 SB_DQ[42]
M_A_DQ43	AK12	SA_DQ[43]	M_B_DQ43 AN2 SB_DQ[43]
M_A_DQ44	AK8	SA_DQ[44]	M_B_DQ44 AK5 SB_DQ[44]
M_A_DQ45	AL7	SA_DQ[45]	M_B_DQ45 AK2 SB_DQ[45]
M_A_DQ46	AK11	SA_DQ[46]	M_B_DQ46 AM4 SB_DQ[46]
M_A_DQ47	AL8	SA_DQ[47]	M_B_DQ47 AM3 SB_DQ[47]
M_A_DQ48	AN8	SA_DQ[48]	M_B_DQ48 AP3 SB_DQ[48]
M_A_DQ49	AM10	SA_DQ[49]	M_B_DQ49 AN5 SB_DQ[49]
M_A_DQ50	AR11	SA_DQ[50]	M_B_DQ50 AT4 SB_DQ[50]
M_A_DQ51	AL11	SA_DQ[51]	M_B_DQ51 AN6 SB_DQ[51]
M_A_DQ52	AM9	SA_DQ[52]	M_B_DQ52 AN4 SB_DQ[52]
M_A_DQ53	AN9	SA_DQ[53]	M_B_DQ53 AN3 SB_DQ[53]
M_A_DQ54	AT11	SA_DQ[54]	M_B_DQ54 AT5 SB_DQ[54]
M_A_DQ55	AP12	SA_DQ[55]	M_B_DQ55 AT6 SB_DQ[55]
M_A_DQ56	AM12	SA_DQ[56]	M_B_DQ56 AN7 SB_DQ[56]
M_A_DQ57	AN12	SA_DQ[57]	M_B_DQ57 AP6 SB_DQ[57]
M_A_DQ58	AM13	SA_DQ[58]	M_B_DQ58 AP8 SB_DQ[58]
M_A_DQ59	AT14	SA_DQ[59]	M_B_DQ59 AT9 SB_DQ[59]
M_A_DQ60	AT12	SA_DQ[60]	M_B_DQ60 AT7 SB_DQ[60]
M_A_DQ61	AL13	SA_DQ[61]	M_B_DQ61 AP9 SB_DQ[61]
M_A_DQ62	AR14	SA_DQ[62]	M_B_DQ62 AR10 SB_DQ[62]
M_A_DQ63	AP14	SA_DQ[63]	M_B_DQ63 AT10 SB_DQ[63]

(14) M_A_BS#0 AC3 SA_BS[0]
(14) M_A_BS#1 AB2 SA_BS[1]
(14) M_A_BS#2 U7 SA_BS[2]

(15) M_B_BS#0 AB1 SB_BS[0]
(15) M_B_BS#1 W5 SB_BS[1]
(15) M_B_BS#2 R7 SB_BS[2]

(14) M_A_CAS# AE1 SA_CAS#
(14) M_A_RAS# AB3 SA_RAS#
(14) M_A_WE# AE9 SA_WE#

(15) M_B_CAS# AC5 SB_CAS#
(15) M_B_RAS# Y7 SB_RAS#
(15) M_B_WE# AC6 SB_WE#

SA_CK[0]	AA6	M_A_CLK0 (14)	SB_CK[0] W8 M_B_CLK0 (15)
SA_CK#[0]	AA7	M_A_CLK0# (14)	SB_CK#[0] W9 M_B_CLK0# (15)
SA_CKE[0]	P7	M_A_CKE0 (14)	SB_CKE[0] M3 M_B_CKE0 (15)
SA_CK[1]	Y6	M_A_CLK1 (14)	SB_CK[1] V7 M_B_CLK1 (15)
SA_CK#[1]	Y5	M_A_CLK1# (14)	SB_CK#[1] V6 M_B_CLK1# (15)
SA_CKE[1]	P6	M_A_CKE1 (14)	SB_CKE[1] M2 M_B_CKE1 (15)
SA_CS#[0]	AE2	M_A_CS#0 (14)	SB_CS#[0] AB8 M_B_CS#0 (15)
SA_CS#[1]	AE8	M_A_CS#1 (14)	SB_CS#[1] AD6 M_B_CS#1 (15)
SA_ODT[0]	AD8	M_A_ODT0 (14)	SB_ODT[0] AC7 M_B_ODT0 (15)
SA_ODT[1]	AF9	M_A_ODT1 (14)	SB_ODT[1] AD1 M_B_ODT1 (15)

SA_DM[0]	B9	M_A_DM0	SB_DM[0] D4 M_B_DM0
SA_DM[1]	D7	M_A_DM1	SB_DM[1] E1 M_B_DM1
SA_DM[2]	H7	M_A_DM2	SB_DM[2] H3 M_B_DM2
SA_DM[3]	M7	M_A_DM3	SB_DM[3] K1 M_B_DM3
SA_DM[4]	AG6	M_A_DM4	SB_DM[4] AH1 M_B_DM4
SA_DM[5]	AM7	M_A_DM5	SB_DM[5] AL2 M_B_DM5
SA_DM[6]	AN10	M_A_DM6	SB_DM[6] AR4 M_B_DM6
SA_DM[7]	AN13	M_A_DM7	SB_DM[7] AT8 M_B_DM7

M_A_DM[7:0] (14) — M_B_DM[7:0] (15)

SA_DQS[0]	C9	M_A_DQS#0	SB_DQS#[0] D5 M_B_DQS#0
SA_DQS#[1]	F8	M_A_DQS#1	SB_DQS#[1] F4 M_B_DQS#1
SA_DQS#[2]	J9	M_A_DQS#2	SB_DQS#[2] J4 M_B_DQS#2
SA_DQS#[3]	N9	M_A_DQS#3	SB_DQS#[3] L4 M_B_DQS#3
SA_DQS#[4]	AH7	M_A_DQS#4	SB_DQS#[4] AH2 M_B_DQS#4
SA_DQS#[5]	AK9	M_A_DQS#5	SB_DQS#[5] AL4 M_B_DQS#5
SA_DQS#[6]	AP11	M_A_DQS#6	SB_DQS#[6] AR5 M_B_DQS#6
SA_DQS#[7]	AT13	M_A_DQS#7	SB_DQS#[7] AR8 M_B_DQS#7

M_A_DQS#[7:0] (14) — M_B_DQS#[7:0] (15)

SA_DQS[0]	C8	M_A_DQS0	SB_DQS[0] C5 M_B_DQS0
SA_DQS[1]	F9	M_A_DQS1	SB_DQS[1] E3 M_B_DQS1
SA_DQS[2]	H9	M_A_DQS2	SB_DQS[2] H4 M_B_DQS2
SA_DQS[3]	M9	M_A_DQS3	SB_DQS[3] M5 M_B_DQS3
SA_DQS[4]	AH8	M_A_DQS4	SB_DQS[4] AG2 M_B_DQS4
SA_DQS[5]	AK10	M_A_DQS5	SB_DQS[5] AL5 M_B_DQS5
SA_DQS[6]	AN11	M_A_DQS6	SB_DQS[6] AP5 M_B_DQS6
SA_DQS[7]	AR13	M_A_DQS7	SB_DQS[7] AR7 M_B_DQS7

M_A_DQS[7:0] (14) — M_B_DQS[7:0] (15)

SA_MA[0]	Y3	M_A_A0	SB_MA[0] U5 M_B_A0
SA_MA[1]	W1	M_A_A1	SB_MA[1] V2 M_B_A1
SA_MA[2]	AA8	M_A_A2	SB_MA[2] T5 M_B_A2
SA_MA[3]	AA3	M_A_A3	SB_MA[3] V3 M_B_A3
SA_MA[4]	V1	M_A_A4	SB_MA[4] R1 M_B_A4
SA_MA[5]	AA9	M_A_A5	SB_MA[5] T8 M_B_A5
SA_MA[6]	V8	M_A_A6	SB_MA[6] R2 M_B_A6
SA_MA[7]	T1	M_A_A7	SB_MA[7] R6 M_B_A7
SA_MA[8]	Y9	M_A_A8	SB_MA[8] R4 M_B_A8
SA_MA[9]	U6	M_A_A9	SB_MA[9] R5 M_B_A9
SA_MA[10]	AD4	M_A_A10	SB_MA[10] AB5 M_B_A10
SA_MA[11]	T2	M_A_A11	SB_MA[11] P3 M_B_A11
SA_MA[12]	U3	M_A_A12	SB_MA[12] R3 M_B_A12
SA_MA[13]	AG8	M_A_A13	SB_MA[13] AF7 M_B_A13
SA_MA[14]	T3	M_A_A14	SB_MA[14] P5 M_B_A14
SA_MA[15]	V9	M_A_A15	SB_MA[15] N1 M_B_A15

M_A_A[15:0] (14) — M_B_A[15:0] (15)

PROJECT KL3 NOTE Calpella DIS

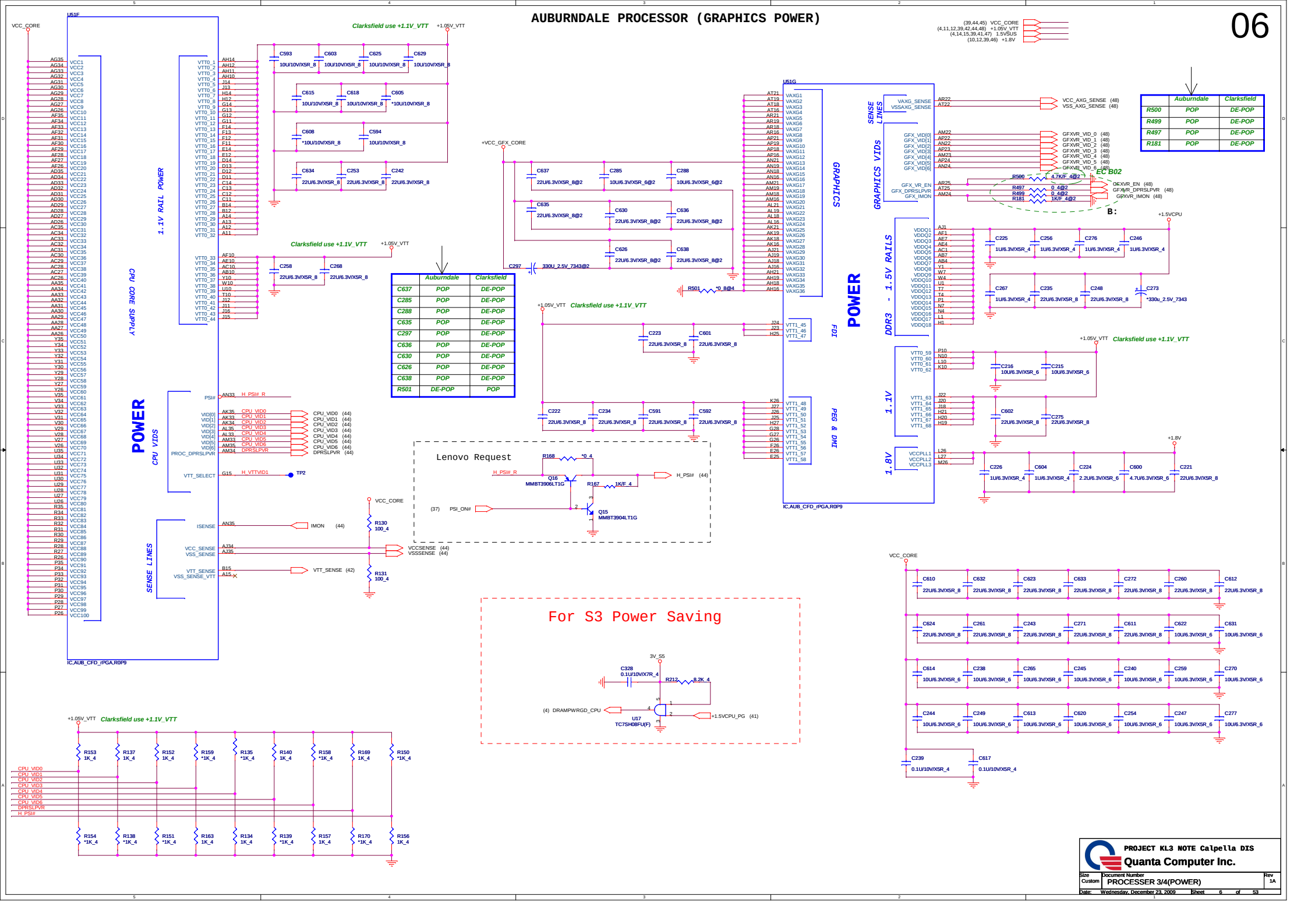
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 2/4(DDR)	1A

Date: Wednesday, December 23, 2009 Sheet 5 of 53

AUBURNDALE PROCESSOR (GRAPHICS POWER)

06



	Auburndale	Clarksfield
R500	POP	DE-POP
R499	POP	DE-POP
R497	POP	DE-POP
R181	POP	DE-POP

	Auburndale	Clarksfield
C637	POP	DE-POP
C285	POP	DE-POP
C288	POP	DE-POP
C635	POP	DE-POP
C297	POP	DE-POP
C636	POP	DE-POP
C630	POP	DE-POP
C626	POP	DE-POP
C638	POP	DE-POP
R501	DE-POP	POP

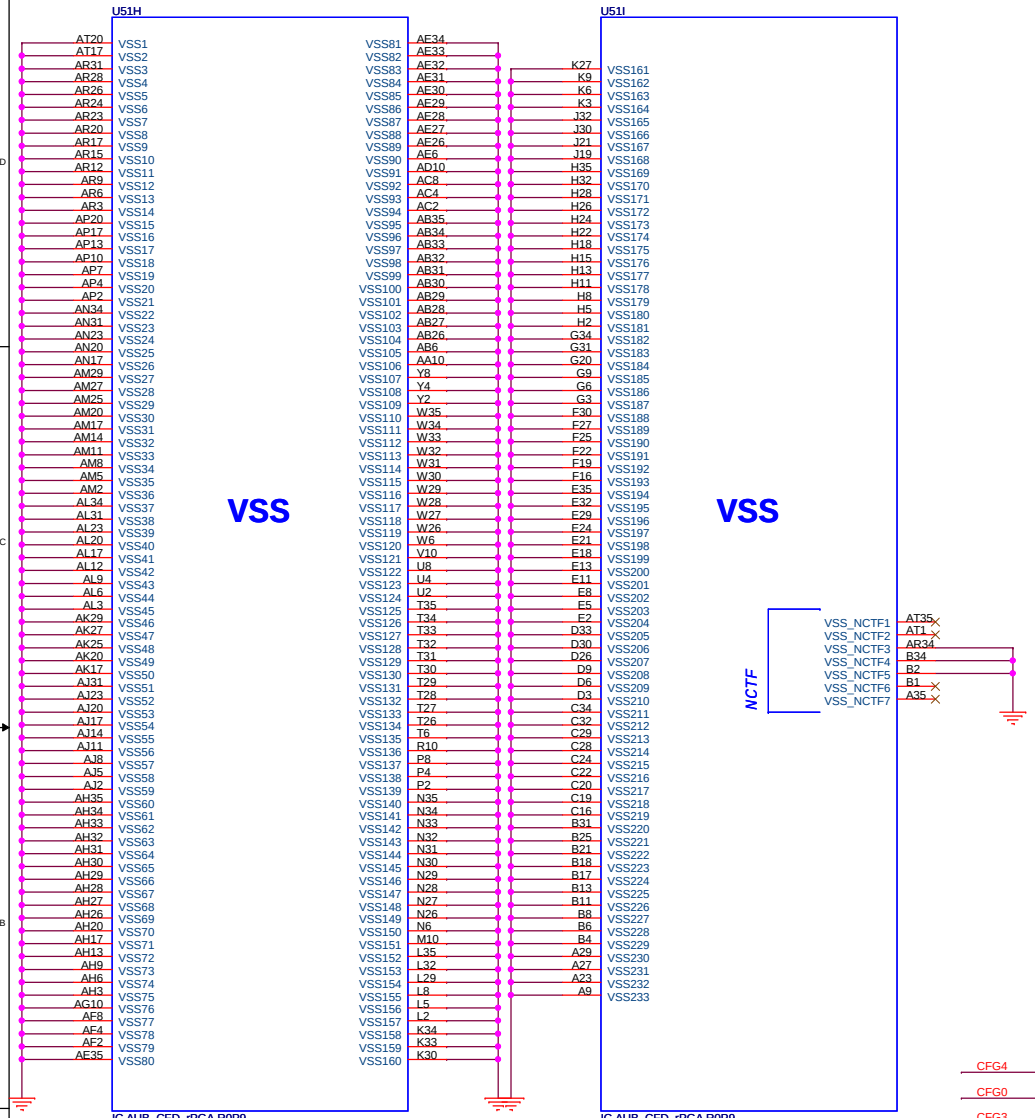
PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

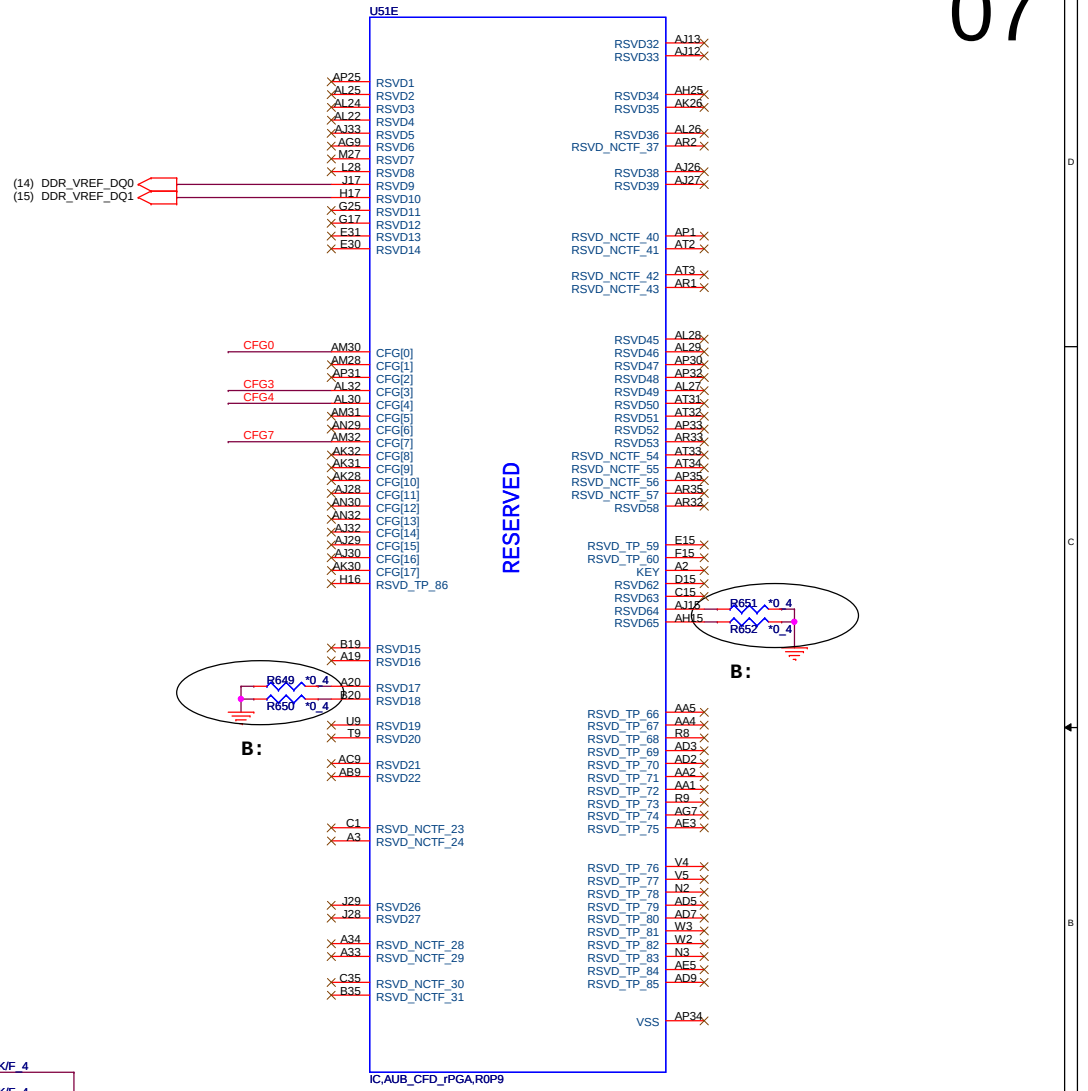
Size	Document Number	Rev
Custom	PROCESSER 3/4(POWER)	1A

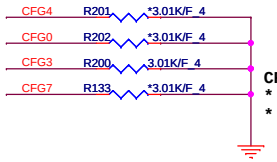
Date: Wednesday, December 23, 2009 Sheet 6 of 53

AUBURNDALE PROCESSOR (GND)



AUBURNDALE PROCESSOR(RESERVED, CFG)





CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

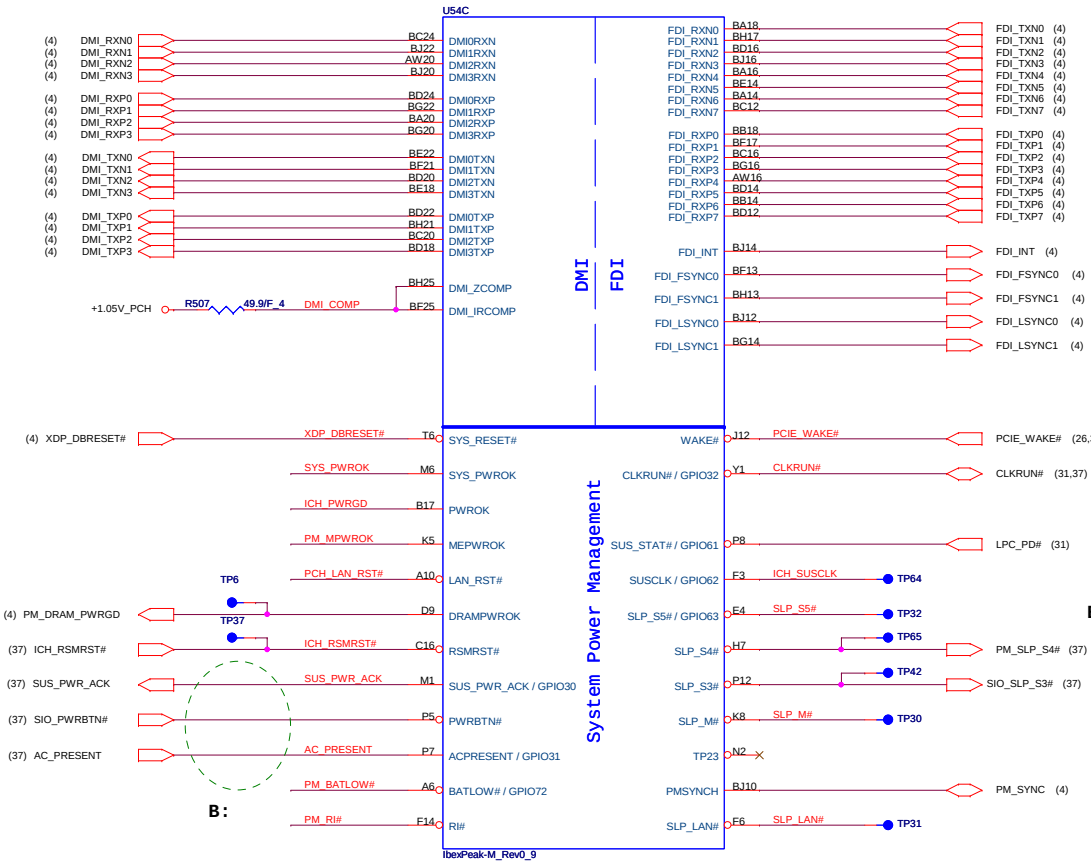
PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

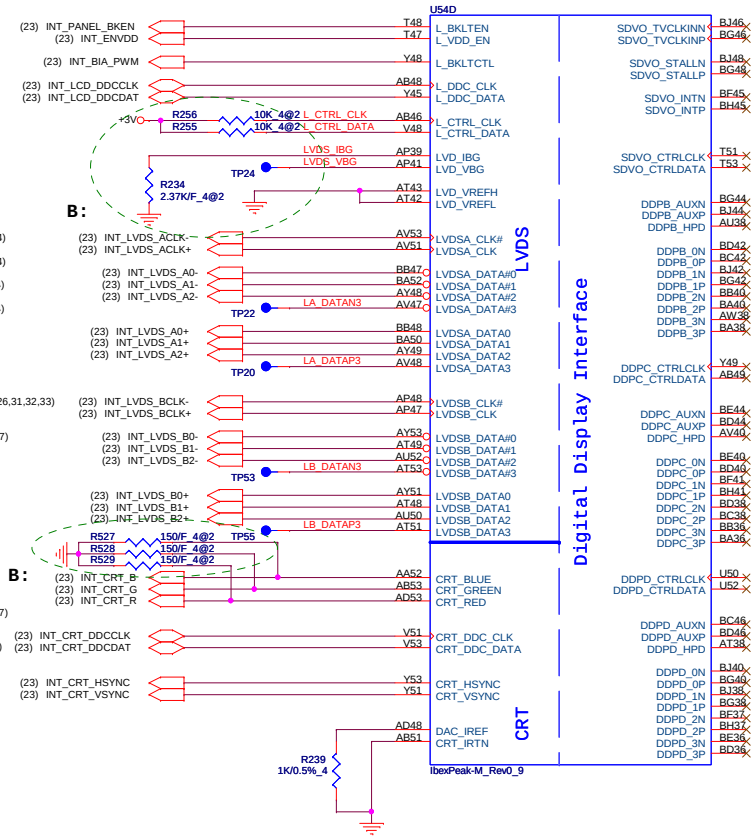
Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	1A

Date: Wednesday, December 23, 2009 Sheet 7 of 53

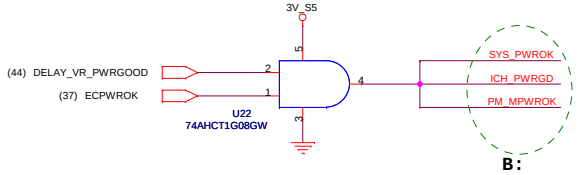
IBEX PEAK-M (DMI,FDI,GPIO)

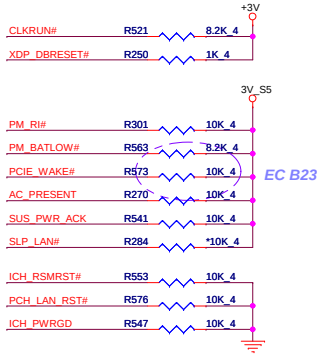


IBEX PEAK-M (LVDS,DDI)



SDVO
Display port B
Display port C
Display port D





	Auburndale	Clarksfield
R256	POP	DE-POP
R255	POP	DE-POP
R234	POP	DE-POP
R527	POP	DE-POP
R528	POP	DE-POP
R529	POP	DE-POP

PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI&VIDEO)	1A

Date: Wednesday, December 23, 2009 Sheet 8 of 53

(12,37) +3VRTC
(24,26,35,36,37,39,40,43,47) 3VPCU
(3,4,8,10,11,12,14,15,18,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,44,47) +3V
(6,8,10,11,12,31,39,41) 3V_S5
(3,8,10,12,39,49) +1.05V_PCH

RTC Circuitry

CMOS Settings	J3
Clear CMOS	1-2
Save CMOS	1-X (Default)

TPM Settings	J2
Clear ME RTC registers	1-2
Save ME RTC registers	1-X (Default)

B:

Cap values depend on Xtal

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

B:

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

EC B11

No Reboot Strap

Place near connector

iTPM ENABLE/DISABLE

TPM Function	R9386
Enable	Stuff
Disable	NC (Default)

For PCH

16Mbit (2M Byte), SPI

IBEX PEAK-M (HDA,JTAG,SATA)

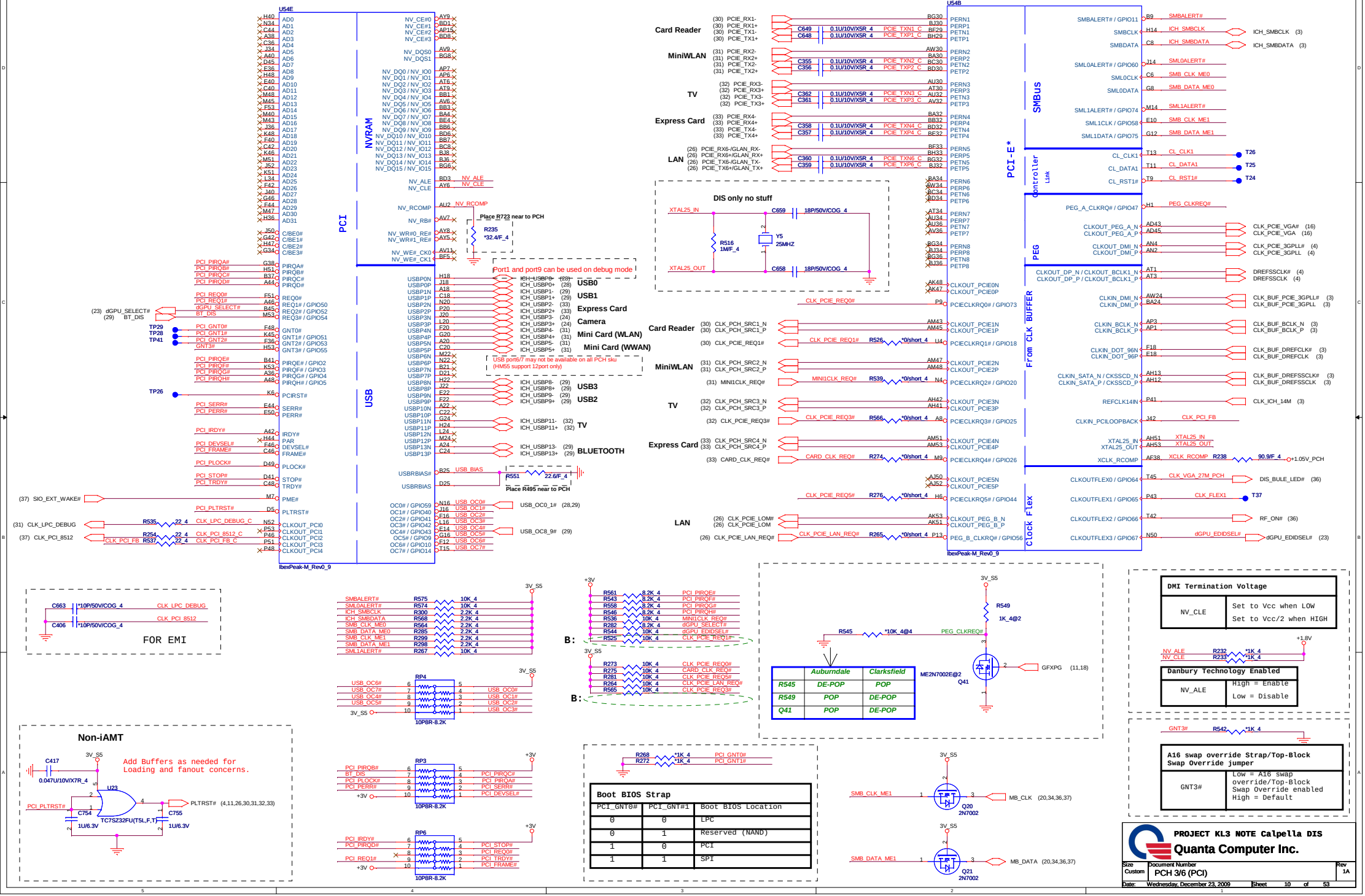
IbexPeak-M_Rev0_9

PROJECT	KL3 NOTE Calpella DIS
Quanta Computer Inc.	
Size	Custom
Document Number	PCH 2/6 (SATA&HDA&JTA)
Rev	1A
Date:	Wednesday, December 23, 2009
Sheet	9 of 53

IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

(3,4,8,9,11,12,14,15,18,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,44,47) +3V
(6,8,9,11,12,31,39,41) 3V_S5
(3,8,9,12,39,49) +1.05V_PCH
(6,12,39,46) +1.8V



FOR EMI

Non-iAMT

	Auburndale	Clarksfield
R545	DE-POP	POP
R549	POP	DE-POP
Q41	POP	DE-POP

Boot BIOS Strap

PCI_GNT0#	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/6 (PCI)	1A

Date: Wednesday, December 23, 2009 Sheet 10 of 53

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

(3,4,8,9,10,12,14,15,18,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,44,47) +3V
(6,8,9,10,12,31,39,41) 3V_S5
(3,8,9,10,12,39,49) +1.05V_PCH

U54F

MISC

(30) JMB387_INT#	JMB387_INT#	Y3	BMBUSY# / GPIO0	
(37) SIO_EXT_SMI#	SIO_EXT_SMI#	C38	TACH1 / GPIO1	
(37) SIO_EXT_SCI#	SIO_EXT_SCI#	D37	TACH2 / GPIO6	
(33) EXPRCRD_PWREN#	EXPRCRD_PWREN#	J32	TACH3 / GPIO7	
	PCH_GPIO8	F10	GPIO8	
	PCH_GPIO12	K9	LAN_PHY_PWR_CTRL / GPIO12	
	PCH_GPIO15	T7	GPIO15	

GPIO

	DGPU_HOLD_RST#	AA2	SATA4GP / GPIO16	
	GFXPG_R	F38	TACH0 / GPIO17	
	MODEL_ID0	Y7	SCLOCK / GPIO22	
(31) WLAN_OFF#	WLAN_OFF#	H10	MEM_LED / GPIO24	
TP25	PCH_GPIO27	AB12	GPIO27	
	TP_PCH_GPIO28	V13	GPIO28	
(31) SSD_DETECT#	SSD_DETECT#	M11	STP_PCI# / GPIO34	
(29) BT_ON#	BT_ON#	V6	SATACLKREQ# / GPIO35	
	DGPU_PWR_EN#	AB7	SATA2GP / GPIO36	
	BOARD_ID1	AB13	SATA3GP / GPIO37	
	BOARD_ID2	V3	SLOAD / GPIO38	
	BOARD_ID3	P3	SDATAOUT0 / GPIO39	
	CLK_PCIE_REQ6#	H3	PCIECLKRQ6# / GPIO45	
(4,14,15) DRAMRST_PCH	DRAMRST_PCH	F1	PCIECLKRQ7# / GPIO46	
(31) WWAN_OFF#	R249 *0_4/SV_SET_UP	AB6	SDATAOUT1 / GPIO48	
(34,37) TEMP_ALERT#	TEMP_ALERT#	AA4	SATA5GP / GPIO49	
	BOARD_ID0	F8	GPIO57	

CPU

CLKOUT_PCIE6N	CLKOUT_PCIE6N	AH45	
CLKOUT_PCIE6P	CLKOUT_PCIE6P	AH46	
CLKOUT_PCIE7N	CLKOUT_PCIE7N	AF48	
CLKOUT_PCIE7P	CLKOUT_PCIE7P	AF47	
A20GATE	A20GATE	U2	SIO_A20GATE (37)
CLKOUT_BCLK0_N / CLKOUT_PCIE8N	CLKOUT_BCLK0_N / CLKOUT_PCIE8N	AM3	CLK_CPU_BCLK# (4)
CLKOUT_BCLK0_P / CLKOUT_PCIE8P	CLKOUT_BCLK0_P / CLKOUT_PCIE8P	AM1	CLK_CPU_BCLK (4)
PECI	PECI	BG10	H_PECI (4)
RCIN#	SIO_RCIN# T1 RCIN#		SIO_RCIN# (37)
PROCPWRGD	PROCPWRGD	BE10	H_PWRGOOD (4)
THRMTRIP#	PCH_THRMTRIP# R231 56_4 BD10 THRMTRIP#		PM_THRMTRIP# (4)

R230 56_4 → +1.05V_VTT

TP1	TP1_PCH	BA22	TP19
TP2	TP2_PCH	AW22	TP21
TP3		BB22	
TP4		AY45	
TP5		AY46	
TP6		AV43	
TP7		AV45	
TP8		AF13	
TP9		M18	
TP10		N18	
TP11		AJ24	
TP12		AK41	
TP13		AK42	
TP14		M32	
TP15		N32	
TP16		M30	
TP17		N30	
TP18		H12	
TP19		AA23	
NC_1		AB45	
NC_2		AB38	
NC_3		AB42	
NC_4		AB41	
NC_5		T39	
INIT3_3V#	TP_INT3_3V	P6	TP27
TP24		C10	

NCTF / RSVD

VSS_NCTF_1 … VSS_NCTF_31 (A4, A49, A5, A50, A52, A53, B2, B4, B52, B53, BE1, BE53, BF1, BF53, BH1, BH2, BH52, BH53, BJ1, BJ2, BJ4, BJ49, BJ5, BJ50, BJ52, BJ53, D1, D2, D53, E1, E53)

IbexPeak-M_Rev0_9

B:

PCH_GPIO8	R297	10K_4	3V_S5
PCH_GPIO12	R569	10K_4	
PCH_GPIO15	R253	1K_4	
TP_PCH_GPIO28	R571	10K_4	
CLK_PCIE_REQ6#	R548	10K_4	
DRAMRST_PCH	R562	10K_4	
WLAN_OFF#	R572	10K_4	

B:

JMB387_INT#	R522	10K_4	+3V
SIO_RCIN#	R530	10K_4	
SIO_A20GATE	R531	10K_4	
SSD_DETECT#	R570	10K_4	
EXPRCRD_PWREN#	R288	10K_4	
BT_ON#	R252	10K_4	
SIO_EXT_SCI#	R559	10K_4	
SIO_EXT_SMI#	R560	10K_4	
TEMP_ALERT#	R518	10K_4	
DGPU_HOLD_RST#	R519	*10K_4	
DGPU_PWR_EN#	R517	10K_4	

R513 *0_4@4 — +3V — (18,47) GFXON — U53 TC7SH08FU(F)@2 — MAINON (27,37,39,41,42,46,47,49)

R514 1K_4@2 — +3V

ME2N7002E@2 Q40 — DGPU_PWR_EN#

R294 *0_4@4 — +3V — GFXPG_R — R293 10K_4 — U24 TC7SH08FU(F)@2 — HWPG (4,37,41,42,43,44,46,48,49) — GFXPG (10,18)

C383 0.047U/10V/X7R_4 — 3V_S5

B: R520 *0_4@4 — (4,10,26,30,31,32,33) PLTRST# — DGPU_HOLD_RST# — U55 TC7SH08FU(F)@2 — EXT_RST# (16)

R660 100K_4

Add Buffers as needed for Loading and fanout concerns.

	Auburndale	Clarksfield
U53	POP	DE-POP
R514	POP	DE-POP
Q40	POP	DE-POP
U24	POP	DE-POP
U55	POP	DE-POP
R513	DE-POP	POP
R294	DE-POP	POP
R520	DE-POP	POP

Board ID

Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO57
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	1	0	0
SOVP	1	0	0	0

B: DIS 1

B:

R286	*10K_4	BOARD_ID0	R287	10K_4	+3V
R515	*10K_4	BOARD_ID1	R512	10K_4	
R523	10K_4	BOARD_ID2	R524	*10K_4	
R534	*10K_4@DIS	BOARD_ID3	R538	10K_4@OTHERS	

Model ID

Model ID	MODEL_ID0	MODEL_ID1
14"	0	1
15"	1	0
Default	1	1

+3V — R247 10K_4 — MODEL_ID0 — R248 *10K_4

+3V — R240 *10K_4 — (9) MODEL_ID1 — R243 10K_4

+3V — SV_SET_UP — R251 10K_4

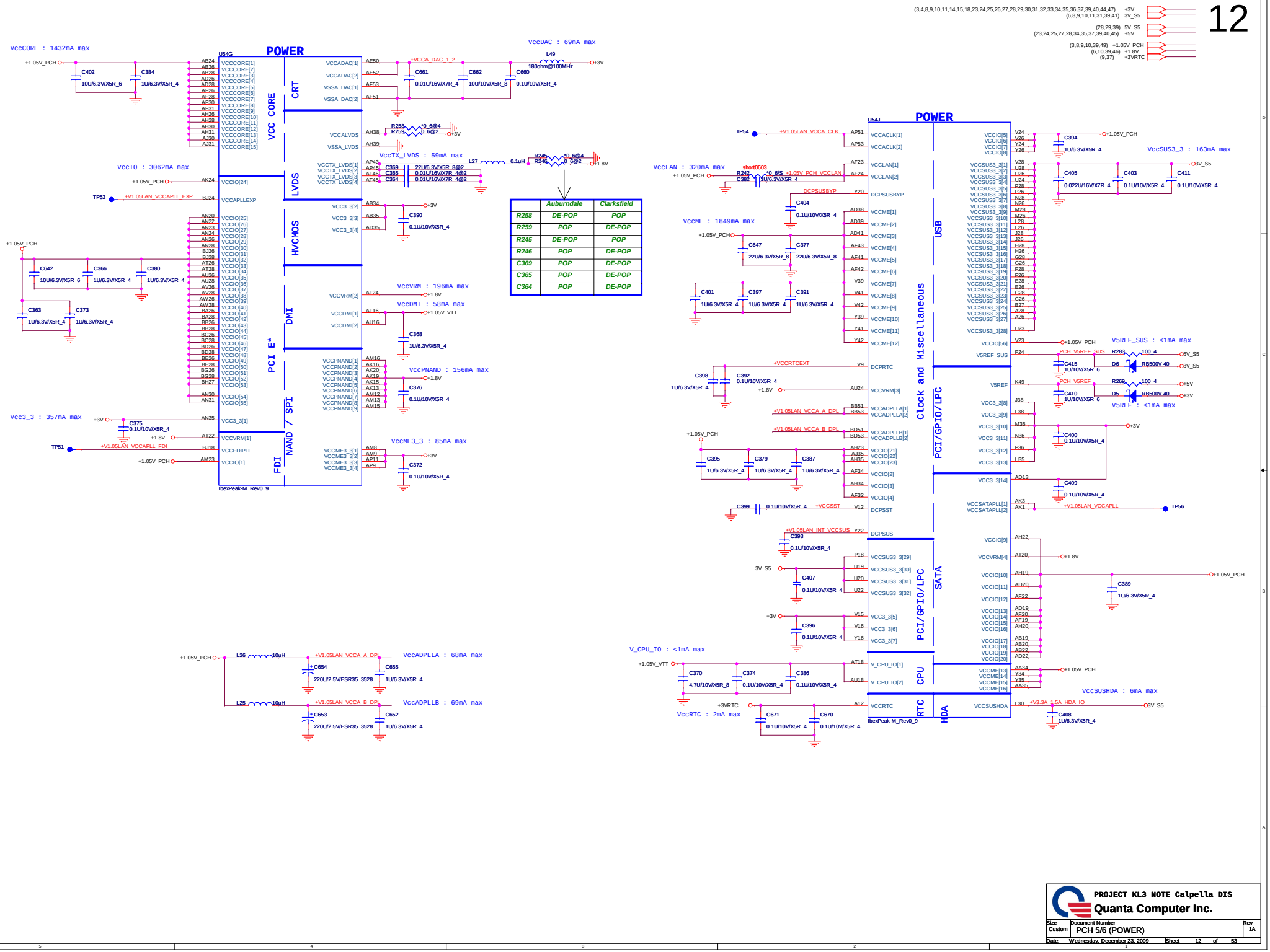
SV_SET_UP	1-X High = Strong (Default)

PROJECT KL3 NOTE Calpella DIS

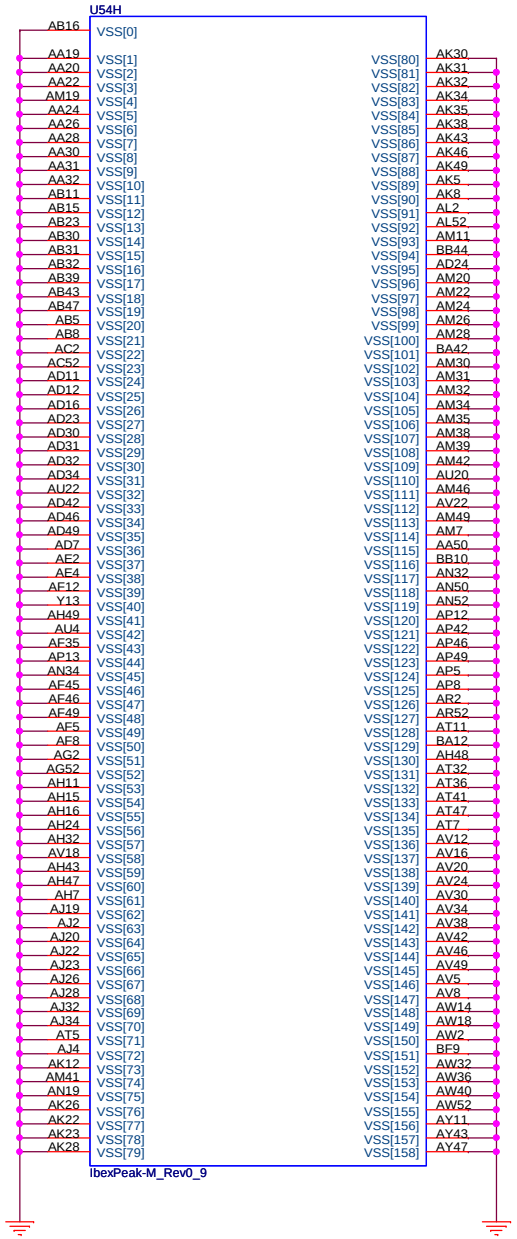
Quanta Computer Inc.

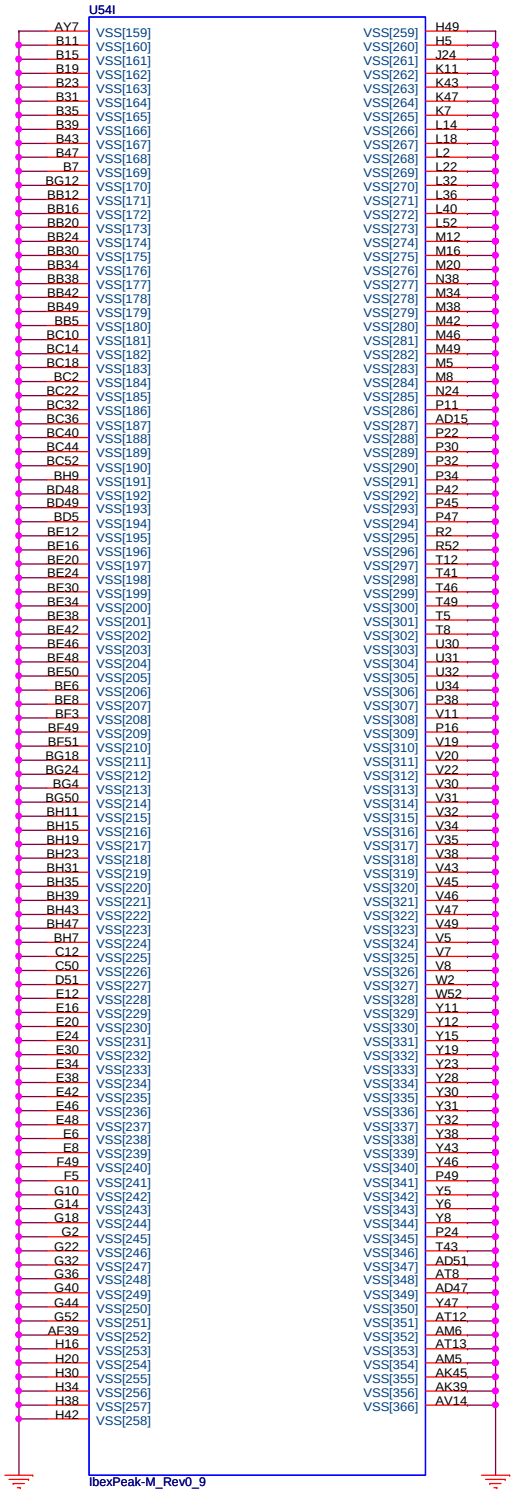
Size	Document Number	Rev
Custom	PCH 4/6 (GPIO)	1A

Date: Wednesday, December 23, 2009 Sheet 11 of 53


POWER
VccCORE : 1432mA max
VccDAC : 69mA max
VccIO : 3062mA max
VccTX_LVDS : 59mA max
VccVRM : 196mA max
VccDMI : 58mA max
VccPNAND : 156mA max
Vcc3_3 : 357mA max
VccME3_3 : 85mA max
VccADPLLA : 68mA max
VccADPLLB : 69mA max
VccLAN : 320mA max
VccME : 1849mA max
V_CPU_IO : <1mA max
VccRTC : 2mA max
VccSUS3_3 : 163mA max
V5REF_SUS : <1mA max
V5REF : <1mA max
VccSUSHDA : 6mA max
U54G
U54J
CRT
VCC CORE
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IbexPeak-M_Rev0_9
Auburndale
Clarksfield
R258 DE-POP POP
R259 POP DE-POP
R245 DE-POP POP
R246 POP DE-POP
C369 POP DE-POP
C365 POP DE-POP
C364 POP DE-POP
PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.
PCH 5/6 (POWER)
Wednesday, December 23, 2009

IBEX PEAK-M (GND)



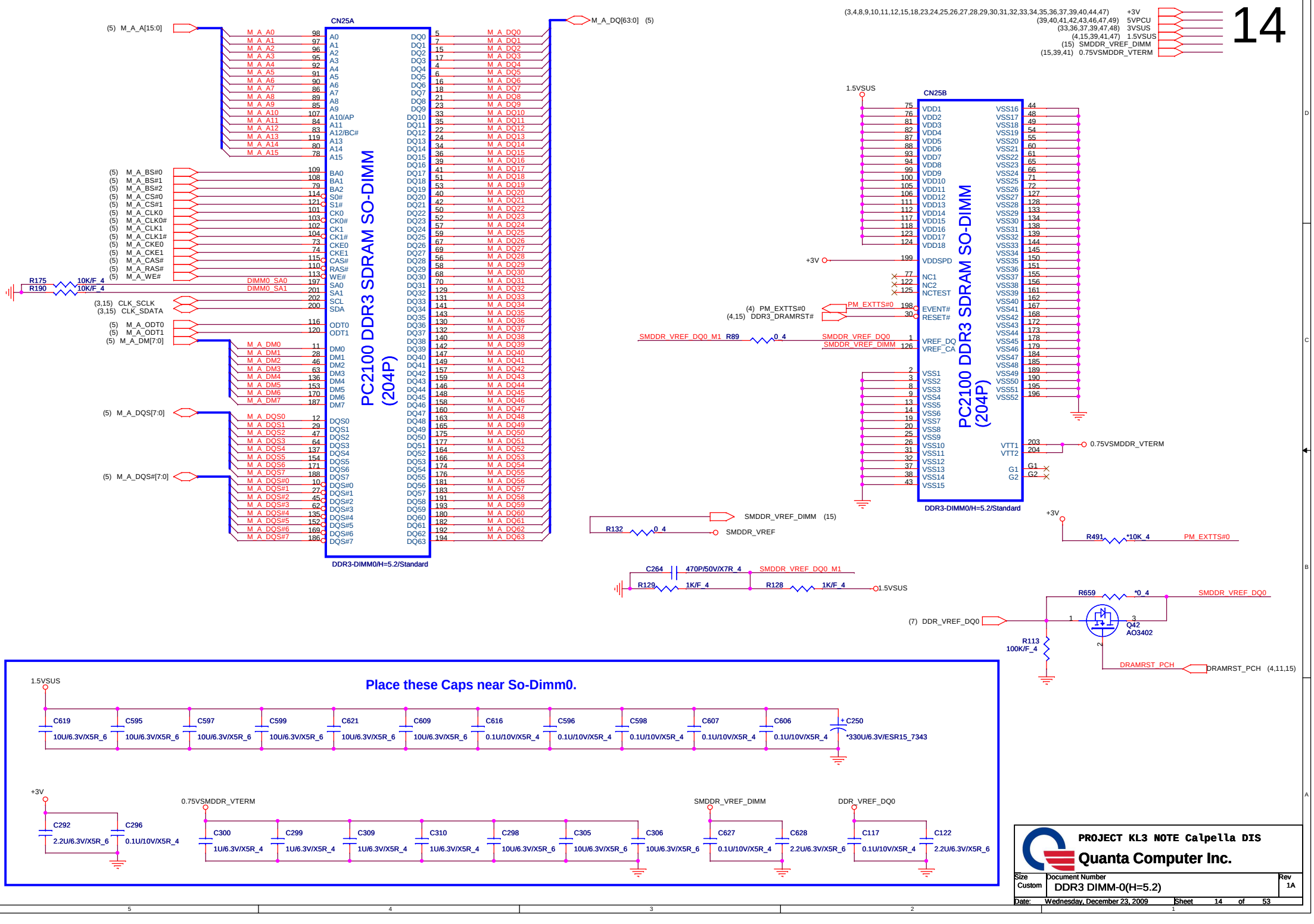


PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

Date: Wednesday, December 23, 2009 Sheet 13 of 53



PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0(H=5.2)	1A

Date: Wednesday, December 23, 2009 Sheet 14 of 53

(3,4,8,9,10,11,12,14,18,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,44,47) +3V
(33,36,37,39,47,48) 3VSUS
(4,14,39,41,47) 1.5VSUS
(14) SMDDR_VREF_DIMM
(14,39,41) 0.75VSMDDR_VTERM

CN26A

(5) M_B_A[15:0]
M_B_A0 98 A0
M_B_A1 97 A1
M_B_A2 96 A2
M_B_A3 95 A3
M_B_A4 92 A4
M_B_A5 91 A5
M_B_A6 90 A6
M_B_A7 86 A7
M_B_A8 89 A8
M_B_A9 85 A9
M_B_A10 107 A10/AP
M_B_A11 84 A11
M_B_A12 83 A12/BC#
M_B_A13 119 A13
M_B_A14 80 A14
M_B_A15 78 A15

(5) M_B_BS#0 109 BA0
(5) M_B_BS#1 108 BA1
(5) M_B_BS#2 79 BA2
(5) M_B_CS#0 114 S0#
(5) M_B_CS#1 121 S1#
(5) M_B_CLK0 101 CK0
(5) M_B_CLK0# 103 CK0#
(5) M_B_CLK1 102 CK1
(5) M_B_CLK1# 104 CK1#
(5) M_B_CKE0 73 CKE0
(5) M_B_CKE1 74 CKE1
(5) M_B_CAS# 115 CAS#
(5) M_B_RAS# 110 RAS#
(5) M_B_WE# 113 WE#

R486 10K/F_4 DIMM1_SA0 197 SA0
+3V R498 10K/F_4 DIMM1_SA1 201 SA1

(3,14) CLK_SCLK 202 SCL
(3,14) CLK_SDATA 200 SDA

(5) M_B_ODT0 116 ODT0
(5) M_B_ODT1 120 ODT1
(5) M_B_DM[7:0]
M_B_DM0 11 DM0
M_B_DM1 28 DM1
M_B_DM2 46 DM2
M_B_DM3 63 DM3
M_B_DM4 136 DM4
M_B_DM5 153 DM5
M_B_DM6 170 DM6
M_B_DM7 187 DM7

(5) M_B_DQS[7:0]
M_B_DQS0 12 DQS0
M_B_DQS1 29 DQS1
M_B_DQS2 47 DQS2
M_B_DQS3 64 DQS3
M_B_DQS4 137 DQS4
M_B_DQS5 154 DQS5
M_B_DQS6 171 DQS6
M_B_DQS7 188 DQS7

(5) M_B_DQS#[7:0]
M_B_DQS#0 10 DQS#0
M_B_DQS#1 27 DQS#1
M_B_DQS#2 45 DQS#2
M_B_DQS#3 62 DQS#3
M_B_DQS#4 135 DQS#4
M_B_DQS#5 152 DQS#5
M_B_DQS#6 169 DQS#6
M_B_DQS#7 186 DQS#7

PC2100 DDR3 SDRAM SO-DIMM (204P)

M_B_DQ[63:0] (5)
M_B_DQ0 5 DQ0
M_B_DQ1 7 DQ1
M_B_DQ2 15 DQ2
M_B_DQ3 17 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 6 DQ5
M_B_DQ6 16 DQ6
M_B_DQ7 18 DQ7
M_B_DQ8 21 DQ8
M_B_DQ9 23 DQ9
M_B_DQ10 33 DQ10
M_B_DQ11 35 DQ11
M_B_DQ12 22 DQ12
M_B_DQ13 24 DQ13
M_B_DQ14 34 DQ14
M_B_DQ15 36 DQ15
M_B_DQ16 39 DQ16
M_B_DQ17 41 DQ17
M_B_DQ18 51 DQ18
M_B_DQ19 53 DQ19
M_B_DQ20 40 DQ20
M_B_DQ21 42 DQ21
M_B_DQ22 50 DQ22
M_B_DQ23 52 DQ23
M_B_DQ24 57 DQ24
M_B_DQ25 59 DQ25
M_B_DQ26 67 DQ26
M_B_DQ27 69 DQ27
M_B_DQ28 56 DQ28
M_B_DQ29 58 DQ29
M_B_DQ30 68 DQ30
M_B_DQ31 70 DQ31
M_B_DQ32 129 DQ32
M_B_DQ33 131 DQ33
M_B_DQ34 141 DQ34
M_B_DQ35 143 DQ35
M_B_DQ36 130 DQ36
M_B_DQ37 132 DQ37
M_B_DQ38 140 DQ38
M_B_DQ39 142 DQ39
M_B_DQ40 147 DQ40
M_B_DQ41 149 DQ41
M_B_DQ42 157 DQ42
M_B_DQ43 159 DQ43
M_B_DQ44 146 DQ44
M_B_DQ45 148 DQ45
M_B_DQ46 158 DQ46
M_B_DQ47 160 DQ47
M_B_DQ48 163 DQ48
M_B_DQ49 165 DQ49
M_B_DQ50 175 DQ50
M_B_DQ51 177 DQ51
M_B_DQ52 164 DQ52
M_B_DQ53 166 DQ53
M_B_DQ54 174 DQ54
M_B_DQ55 176 DQ55
M_B_DQ56 181 DQ56
M_B_DQ57 183 DQ57
M_B_DQ58 191 DQ58
M_B_DQ59 193 DQ59
M_B_DQ60 180 DQ60
M_B_DQ61 182 DQ61
M_B_DQ62 192 DQ62
M_B_DQ63 194 DQ63

DDR3-DIMM1/H=5.2/Standard

+3V R188 *10K_4 PM_EXTTS#1

CN26B

1.5VSUS
VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3V VDDSPD 199

NC1 77
NC2 122
NCTEST 125

(4) PM_EXTTS#1 PM_EXTTS#1 EVENT# 198
(4,14) DDR3_DRAMRST# RESET# 30

SMDDR_VREF_DQ1 VREF_DQ 1
(14) SMDDR_VREF_DIMM VREF_CA 126

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

VTT1 203 0.75VSMDDR_VTERM
VTT2 204

G1
G2

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1/H=5.2/Standard

R329 1K/F_4
C784 470P/50V_4
R339 1K/F_4 1.5VSUS
SMDDR_VREF_DQ1_M1 R488 0_4 SMDDR_VREF_DQ1

R487 *0_4
(7) DDR_VREF_DQ1 1 Q49 AO3402 3 2
R328 100K/F_4
DRAMRST_PCH (4,11,14)

Place these Caps near So-Dimm1.

1.5VSUS
C252 10U/6.3V/X5R_6
C278 10U/6.3V/X5R_6
C198 10U/6.3V/X5R_6
C266 10U/6.3V/X5R_6
C211 10U/6.3V/X5R_6
C257 10U/6.3V/X5R_6
C241 0.1U/10V/X5R_4
C212 0.1U/10V/X5R_4
C217 0.1U/10V/X5R_4
C218 0.1U/10V/X5R_4
C236 0.1U/10V/X5R_4
C220 *330U/6.3V/ESR15_7343

+3V
C294 2.2U/6.3V/X5R_6
C308 0.1U/10V/X5R_4

0.75VSMDDR_VTERM
C307 1U/6.3V/X5R_4
C312 1U/6.3V/X5R_4
C304 1U/6.3V/X5R_4
C313 1U/6.3V/X5R_4
C293 10U/6.3V/X5R_6
C315 10U/6.3V/X5R_6
C314 10U/6.3V/X5R_6

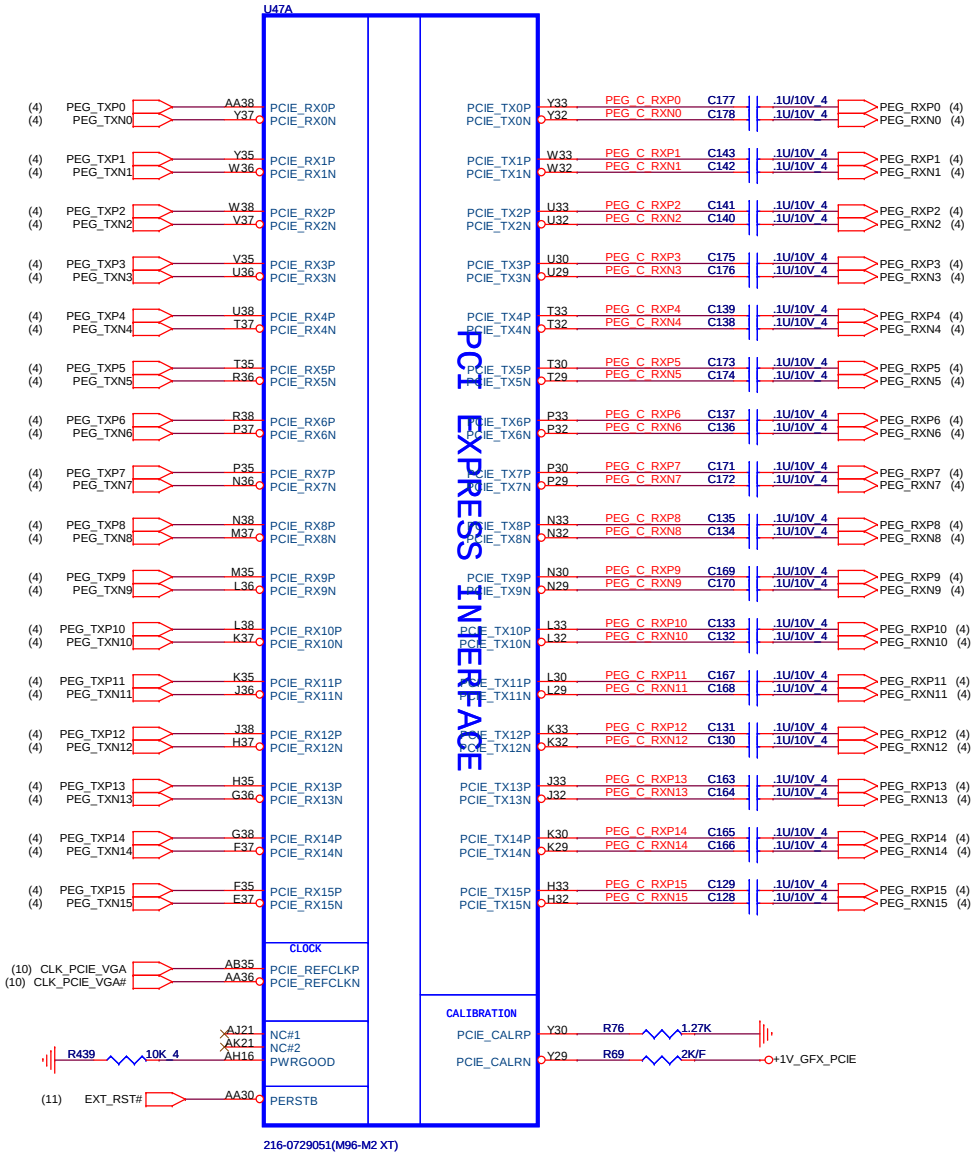
SMDDR_VREF_DIMM
C262 0.1U/10V/X5R_4
C269 2.2U/6.3V/X5R_6

DDR_VREF_DQ1
C147 0.1U/10V/X5R_4
C156 2.2U/6.3V/X5R_6

PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1(H=9.2)	1A

Date: Wednesday, December 23, 2009 Sheet 15 of 53



PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	M96XT_PCIE	1A

Date: Wednesday, December 23, 2009 Sheet 16 of 53

Memory Straps		RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0
800 MHz 1GB(64M*16) Hynix_Orion die	H5TQ1G63BFR-12C	0	0	0	0
800 MHz 1GB(64M*16) Samsung_E die	K4W1G1646E-HC12	0	0	0	1
		0	0	1	0
		0	0	1	1
		0	1	0	0
		0	1	0	1

Note : Required Frequency = 800 MHz

VRAM TYPE

APERTURE SIZE

MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

B:

Power PWM config

GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK

CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	1
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

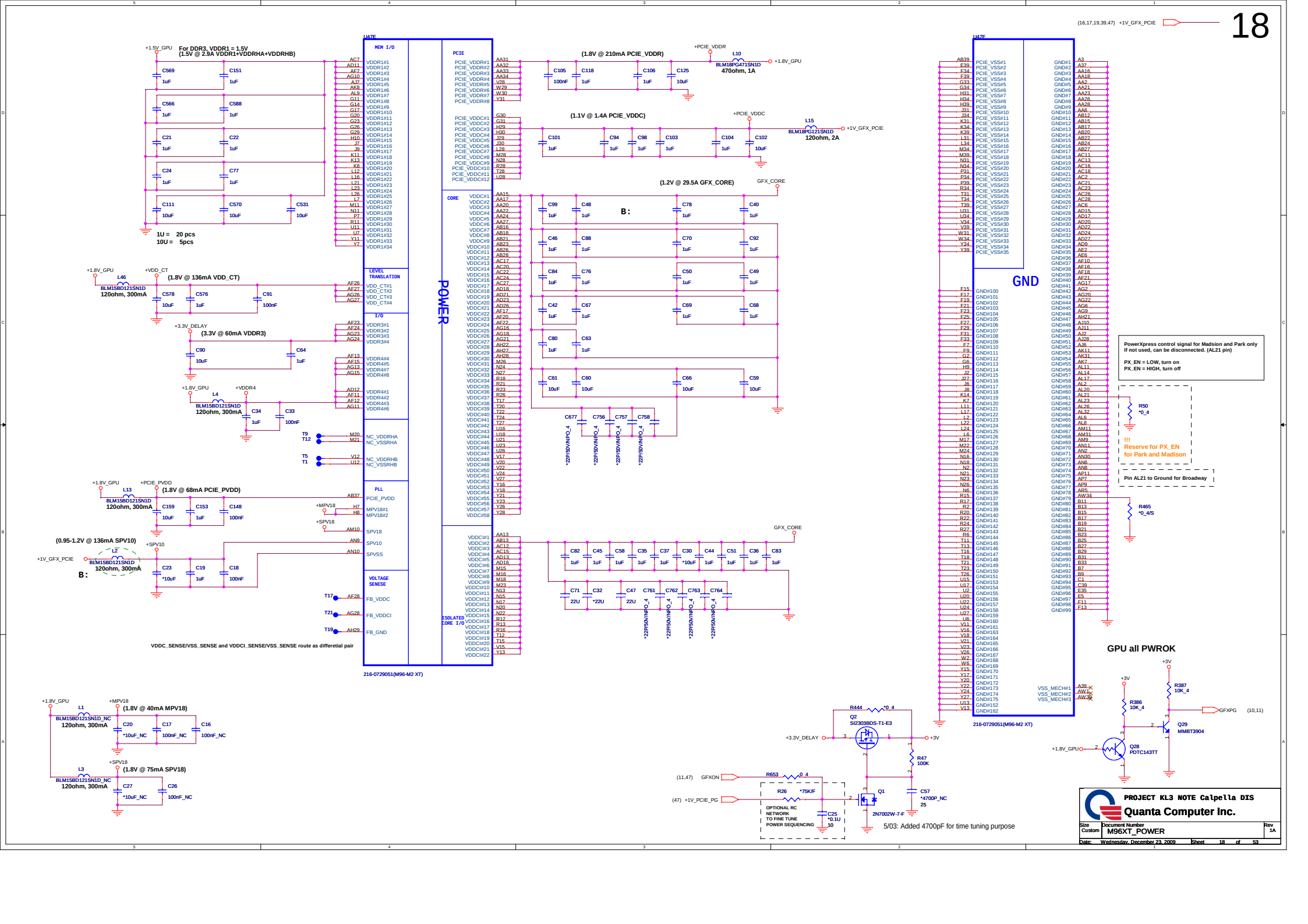
!!! NC when M92-M2

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

!!! NC when M92-M2

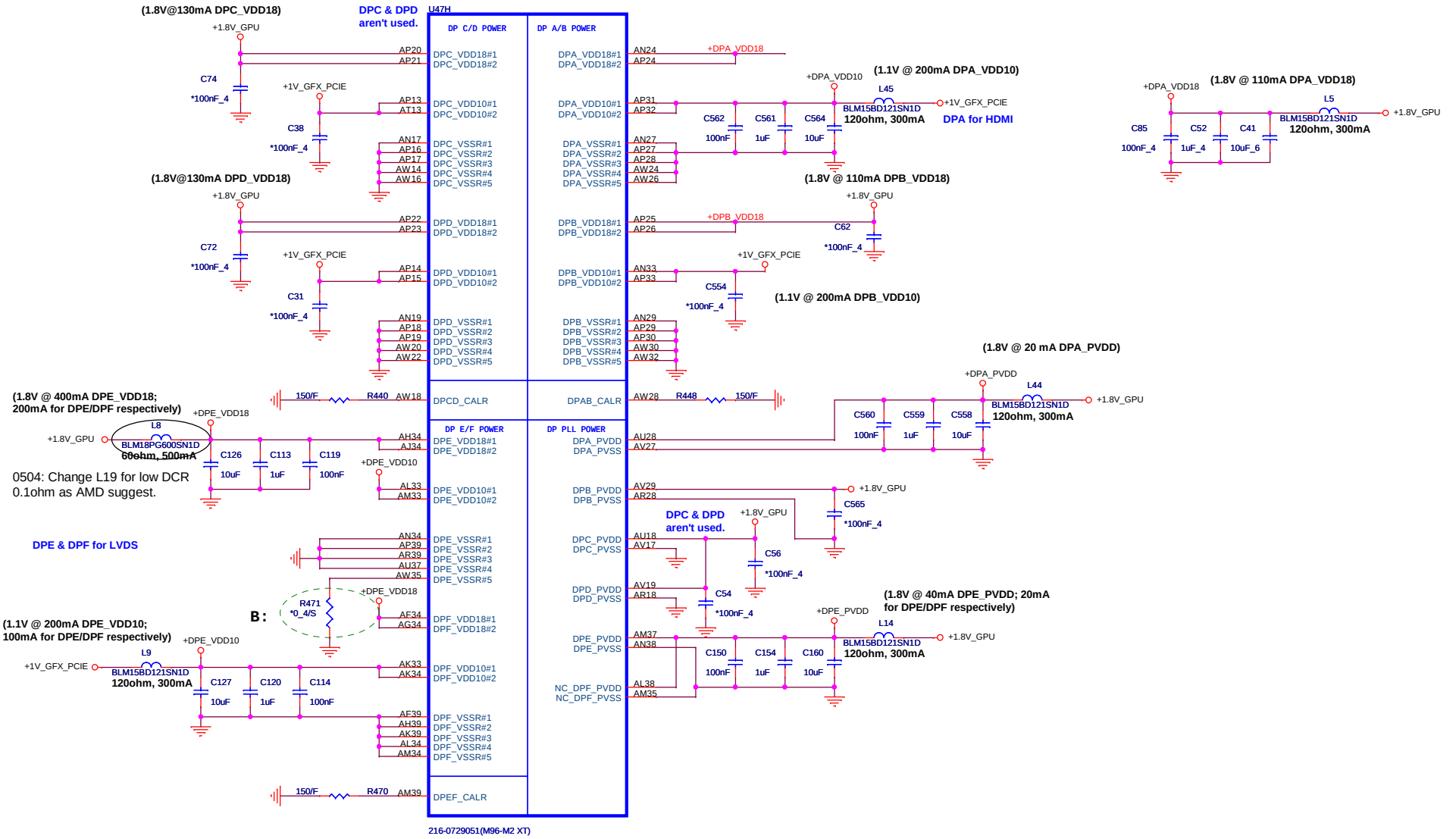
DDC6CLK/DDC6DATA support internal HDCP(High-bandwidth Digital Content Protection) function.

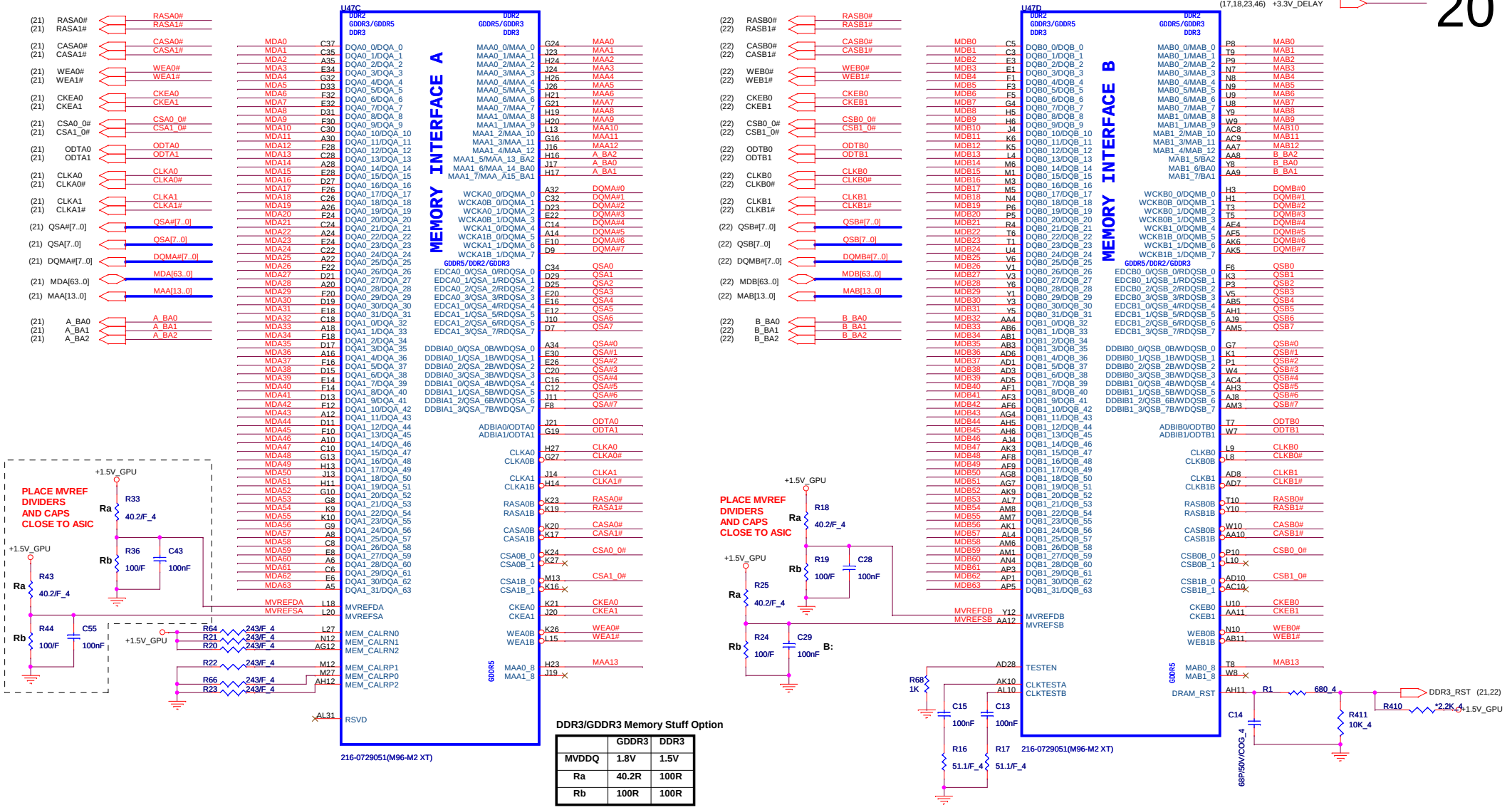
216-0729051(M96-M2 XT)


U47E
MEM I/O
POWER
PCIE
CORE
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
ISOLATED CORE I/O
GND
+1.5V_GPU
For DDR3, VDDR1 = 1.5V
(1.5V @ 2.9A VDDR1+VDDRHA+VDDRHB)
1U = 20 pcs
10U = 5pcs
(1.8V @ 210mA PCIE_VDDR)
BLM18PG471SN1D
470ohm, 1A
(1.1V @ 1.4A PCIE_VDDC)
BLM18PG121SN1D
120ohm, 2A
(1.2V @ 29.5A GFX_CORE)
(1.8V @ 136mA VDD_CT)
(3.3V @ 60mA VDDR3)
(1.8V @ 68mA PCIE_PVDD)
(0.95-1.2V @ 136mA SPV10)
(1.8V @ 40mA MPV18)
(1.8V @ 75mA SPV18)
VDDC_SENSE/VSS_SENSE and VDDCI_SENSE/VSS_SENSE route as differetial pair
216-0729051(M96-M2 XT)
PowerXpress control signal for Madsion and Park only
If not used, can be disconnected. (AL21 pin)
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
!!! Reserve for PX_EN for Park and Madison
Pin AL21 to Ground for Broadway
GPU all PWROK
OPTIONAL RC NETWORK TO FINE TUNE POWER SEQUENCING
5/03: Added 4700pF for time tuning purpose
PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.
M96XT_POWER
Wednesday, December 23, 2009

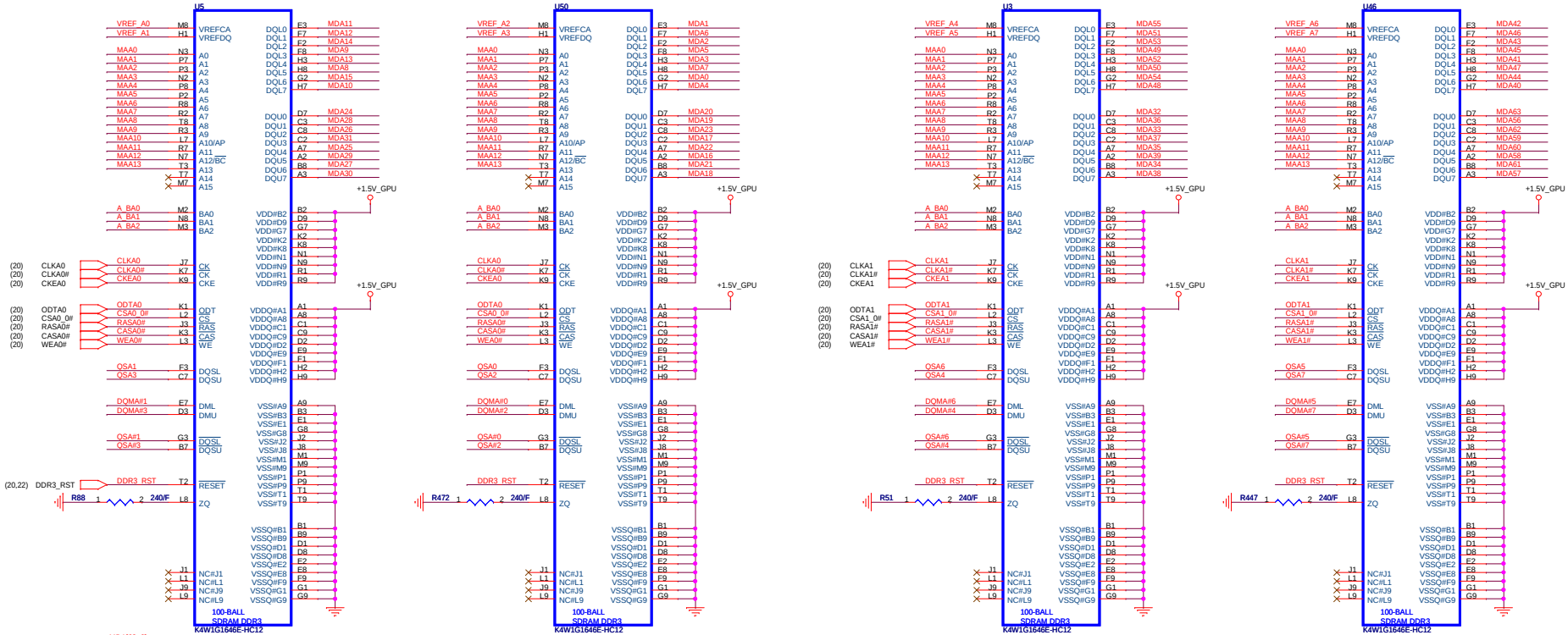
(16,17,18,39,47) +1V_GFX_PCIE

!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V

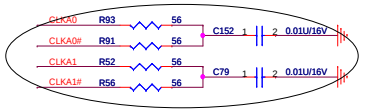


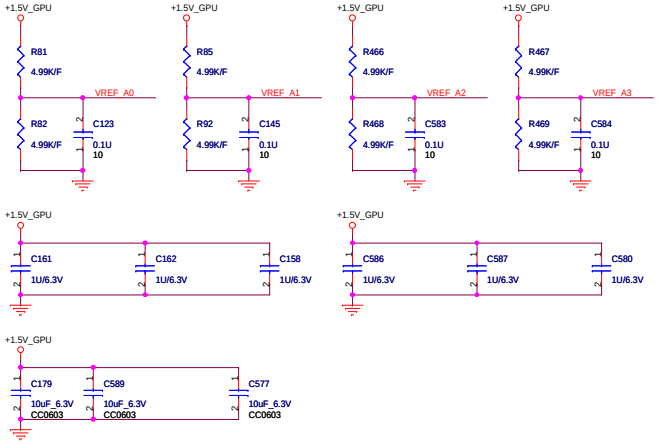

U47C
MEMORY INTERFACE A
DDR2
GDDR3/GDDR5
DDR3
GDDR5/DDR2/GDDR3
216-0729051(M96-M2 XT)
U47D
MEMORY INTERFACE B
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC
+1.5V_GPU
+3.3V_DELAY
(18,21,22,46,47) +1.5V_GPU
(17,18,23,46) +3.3V_DELAY
DDR3/GDDR3 Memory Stuff Option
MVDDQ 1.8V 1.5V
Ra 40.2R 100R
Rb 100R 100R
THERMAL MONITOR
*ADM1032ARMZ-1RL
*2N7002W-7-F
*2N7002
PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.
Size Custom
Document Number M96XT_MEMORY/THERM
Rev 1A
Date: Wednesday, December 23, 2009
Sheet 20 of 53

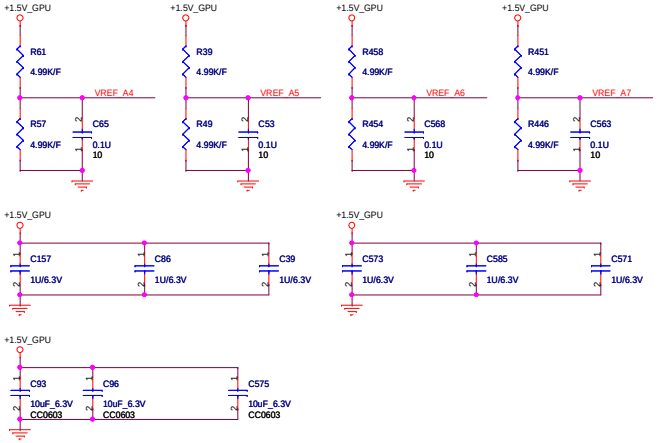
DDR3 64MX16, CH A : 512MB



Placement has to be close to VRAM







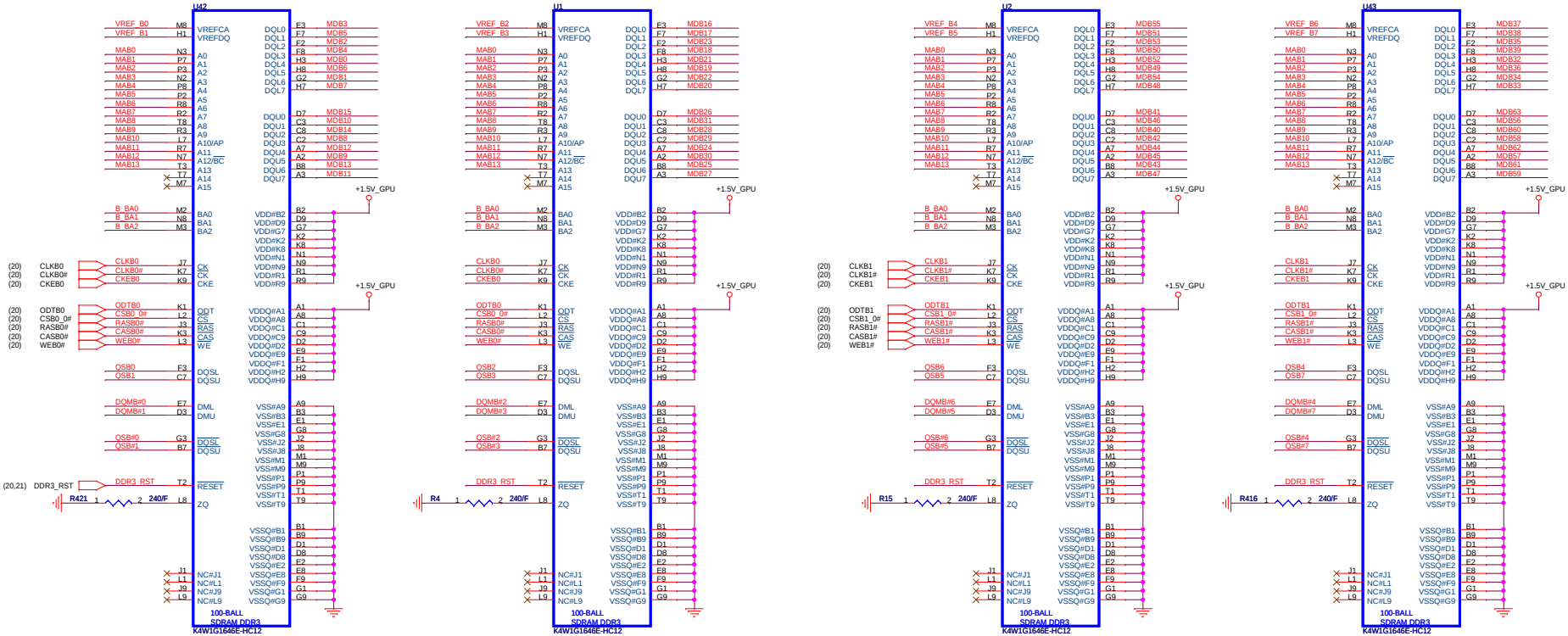
PROJECT KL3 NOTE Calpella DIS

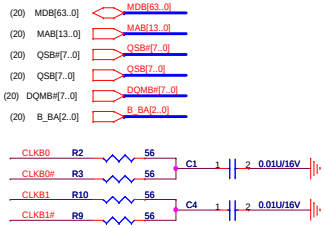
Quanta Computer Inc.

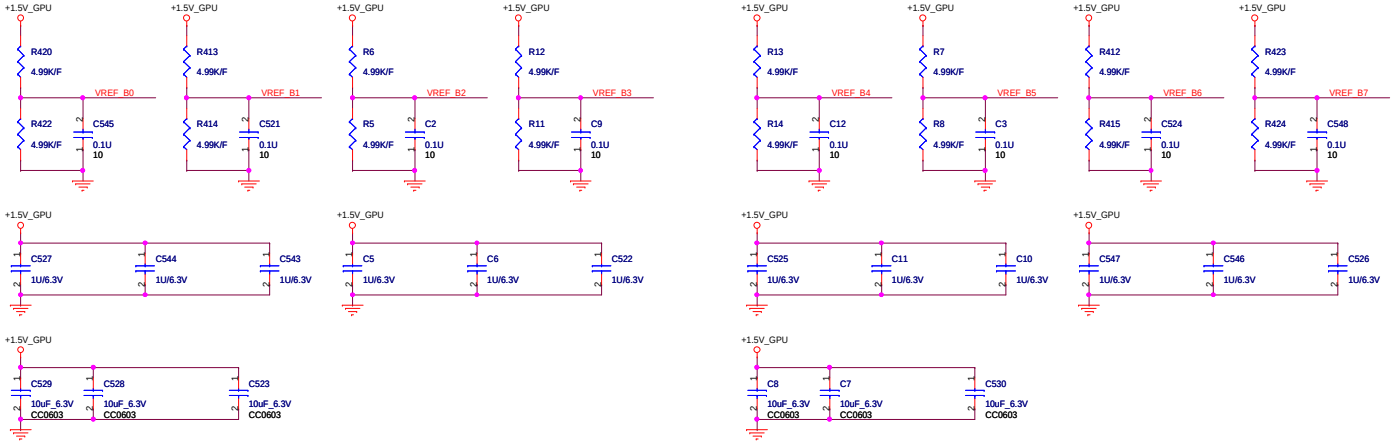
Size	Document Number	Rev
C	M96XT_DDR3_A_512M	1A

Date: Wednesday, December 23, 2009 Sheet 21 of 53

DDR3 64MX16, CH B : 512MB







PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
C	M96XT_DDR3_B_512M	1A

Date: Wednesday, December 23, 2009 Sheet 22 of 53

CRT

S	Yn
0	EV
1	IV

dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

	Auburndale	Clarksfield
R100	DE-POP	POP
R101	DE-POP	POP
R102	DE-POP	POP
R104	DE-POP	POP
R105	DE-POP	POP
R107	DE-POP	POP
R118	DE-POP	POP
Other	POP	DE-POP

HDMI

HDMI Hot-PLUG to EC and GPU

EMI reserve for HDMI

Close CN24

For ESD

Layout note:Place close to HDMI Conn

	Auburndale	Clarksfield
RN2	DE-POP	POP
RN3	DE-POP	POP
RN4	DE-POP	POP
RN5	DE-POP	POP
RN6	DE-POP	POP
RN7	DE-POP	POP
RN8	DE-POP	POP
RN9	DE-POP	POP
RN10	DE-POP	POP
RN1	DE-POP	POP
Other	POP	DE-POP

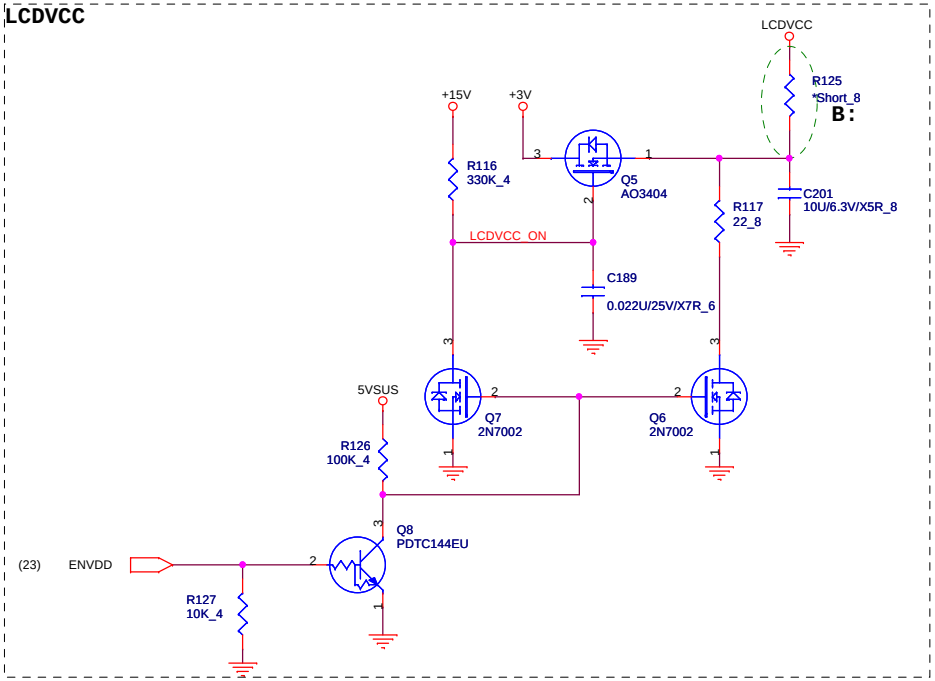
PROJECT KL3 NOTE Calpella DIS

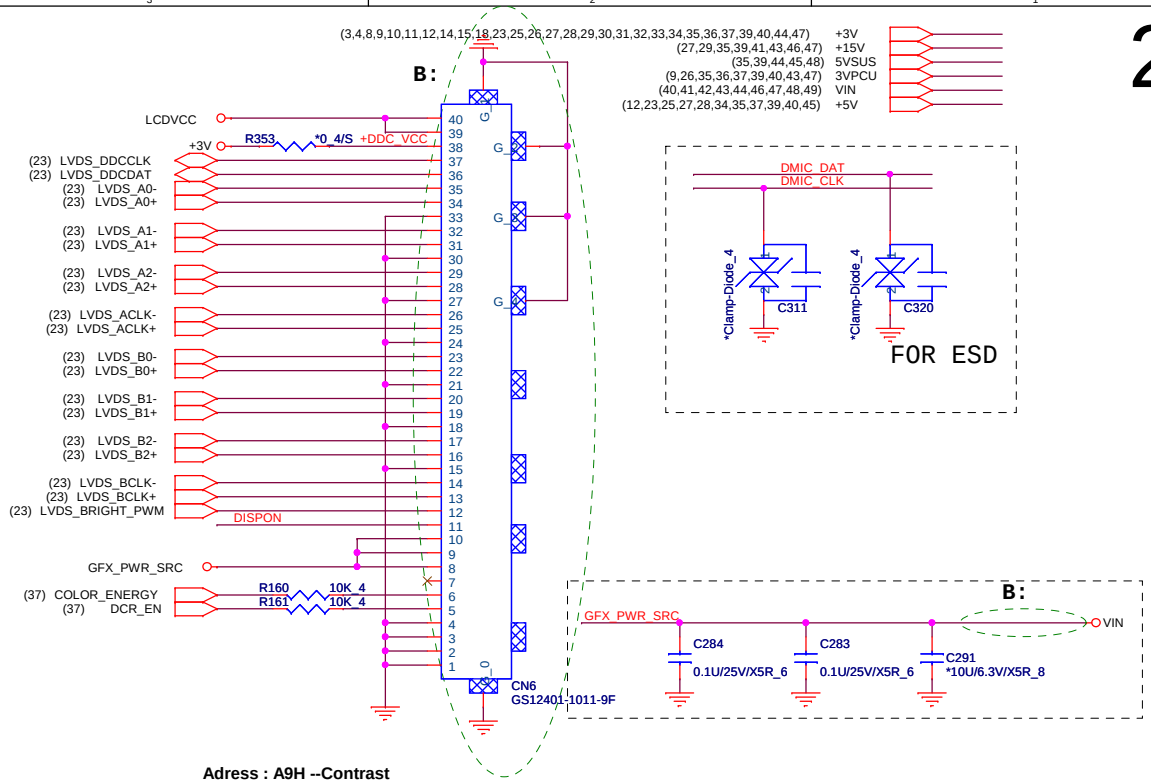
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD/HDMI/CRT switchable	1A

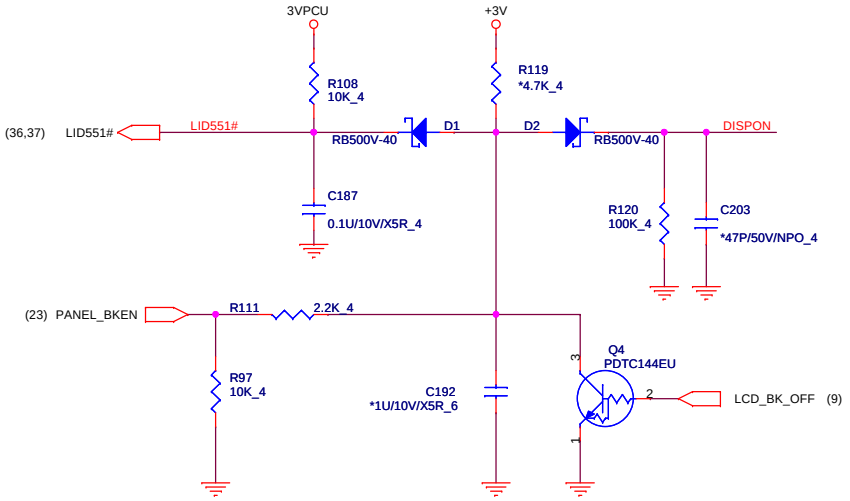
Date: Wednesday, December 23, 2009 Sheet 23 of 53

LCDVCC

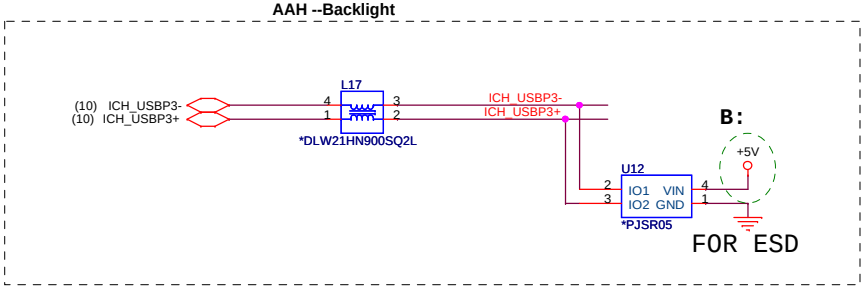




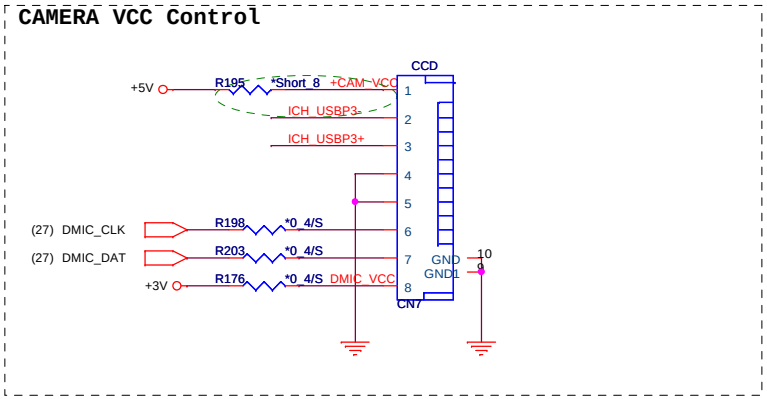
back light



Adress : A9H --Contrast
AAH --Backlight



CAMERA VCC Control

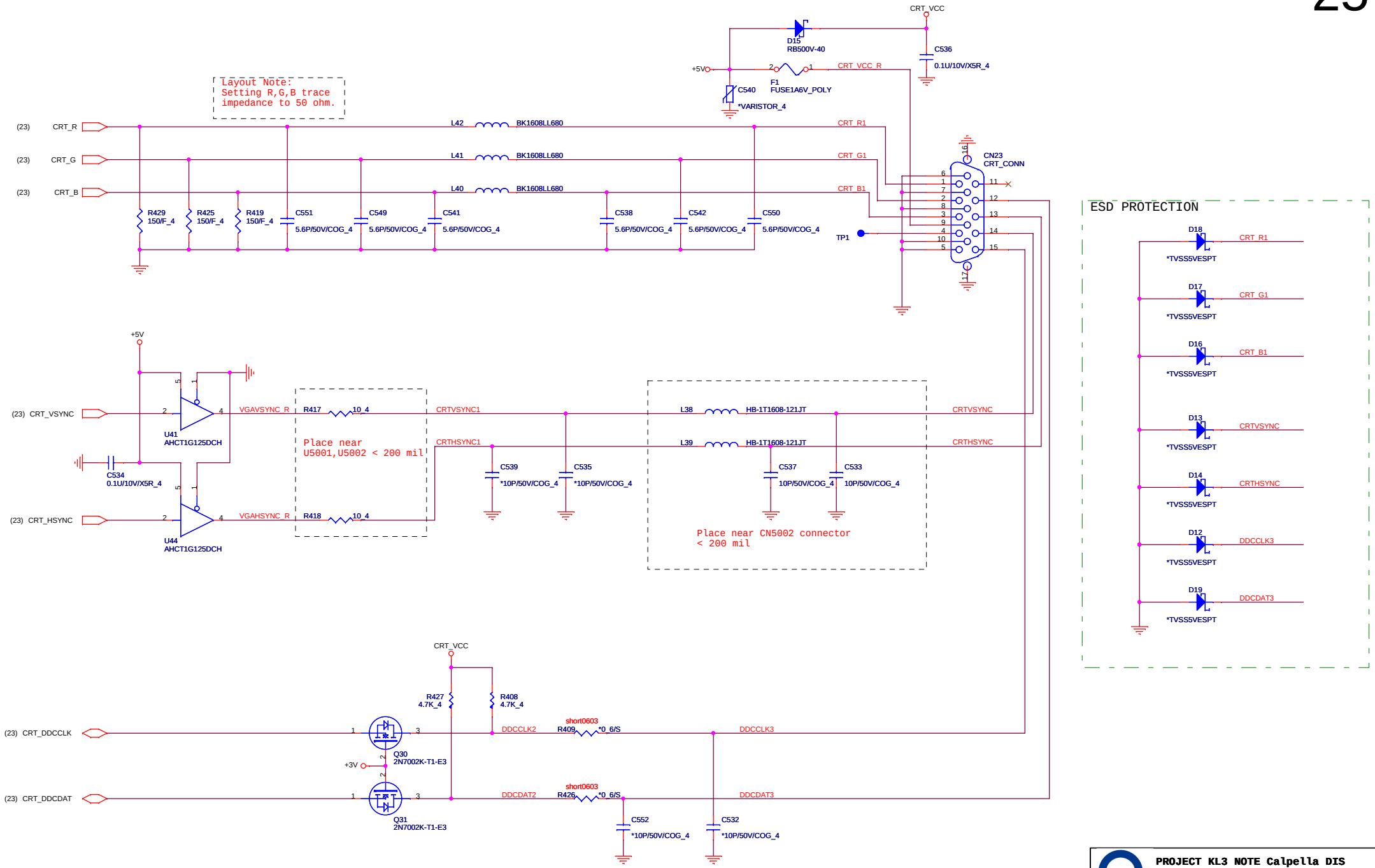


PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	1A

Date: Wednesday, December 23, 2009 Sheet 24 of 53



PROJECT KL3 NOTE Calpella DIS		
Quanta Computer Inc.		
Size: Custom	Document Number: CRT CONN	Rev: 1A
Date: Wednesday, December 23, 2009	Sheet 25 of 53	

Core Power Decoupling

VDDIO Power Decoupling

U19

BCM57780

7mm x 7mm

48-Pin QFN

Package Body

Transformer

U15

NA0069R LF

RJ45 Connector

CN10

RJ45_CONN

Change Footprint For Ver.C

3.3V Device ONLY

U20

M24C02-WMN6TP

U18

*CM1293A-04SO

U14

*CM1293A-04SO

U67

*74AHCT1G08GW

B:

3.3V LANVCC

Q17

AO6402

Q18

PDTC144EU

Q19

PDTC144EU

0213 LC reserved

PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size: Custom

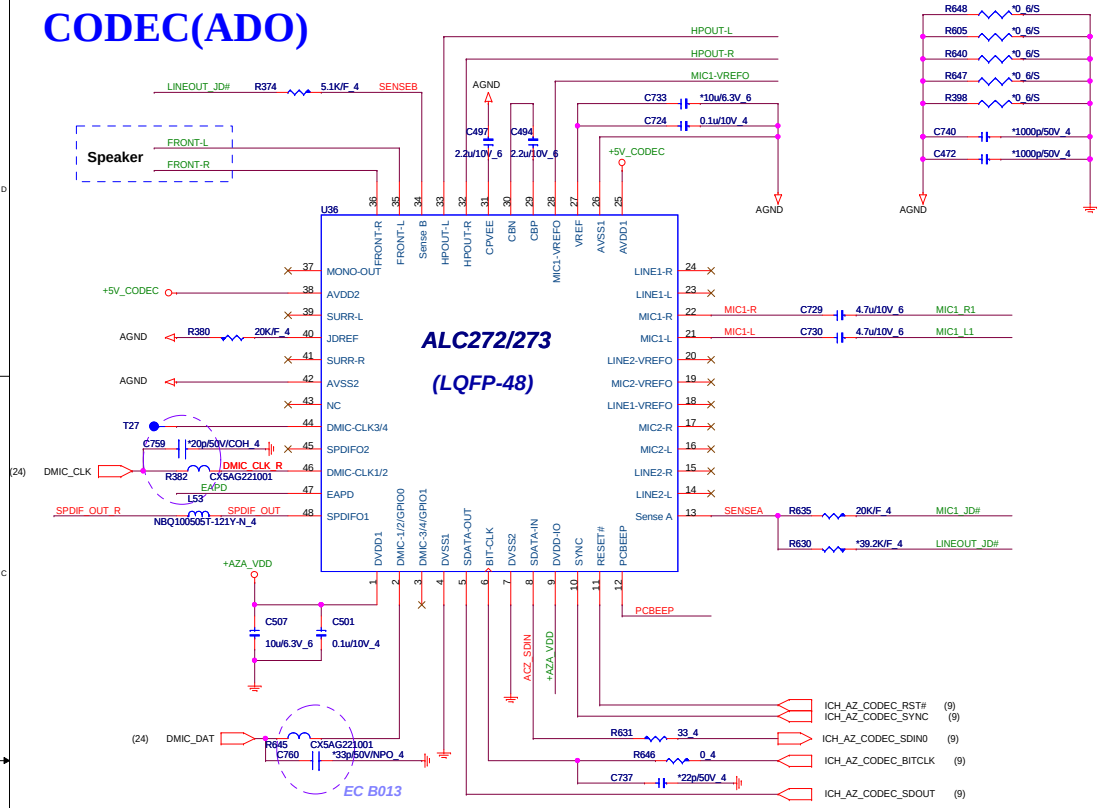
Document Number: LAN (BCM57780, RJ45)

Rev: 1A

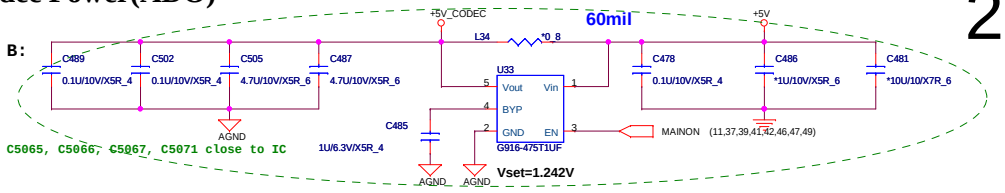
Date: Wednesday, December 23, 2009

Sheet 26 of 53

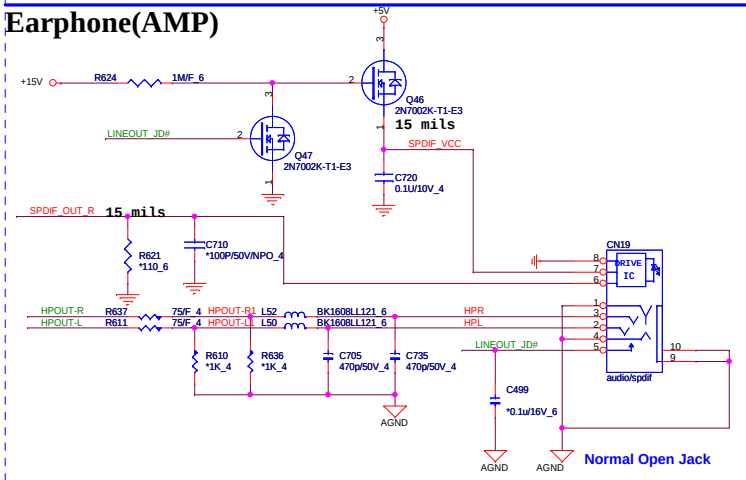
CODEC(ADO)



Codec Power(ADO)

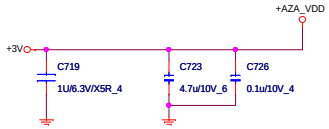


Earphone(AMP)

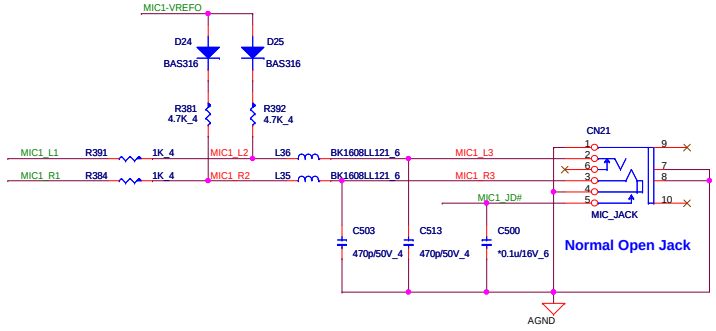


HDA Power(ADO)

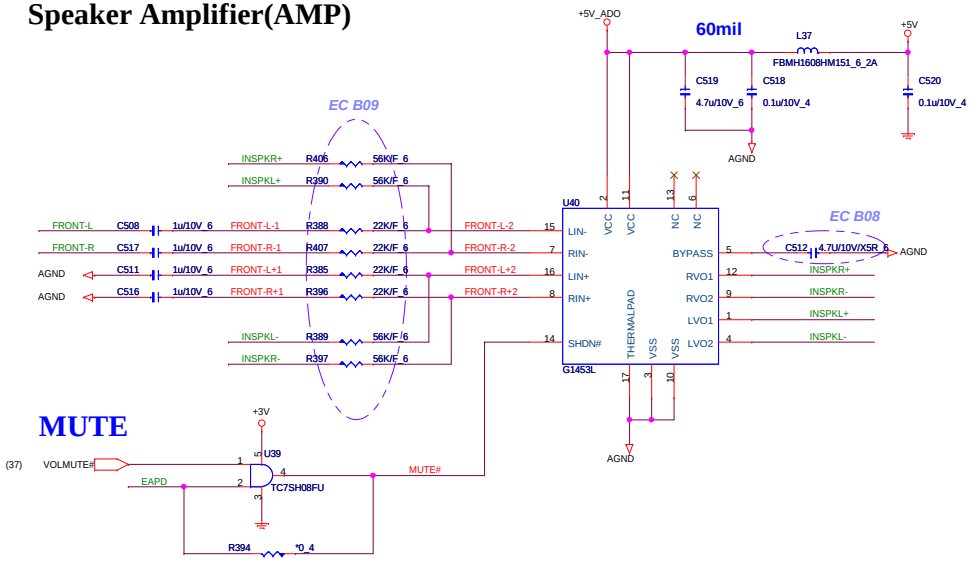
*Intel HDA Either +1.5V_S5 or +3V_S5



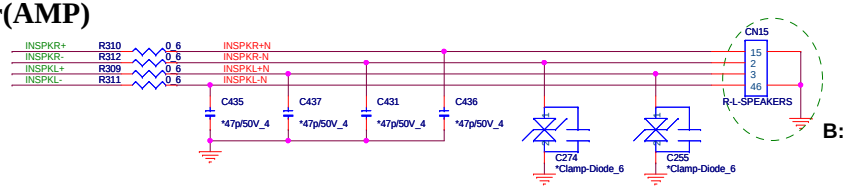
System MIC(AMP)



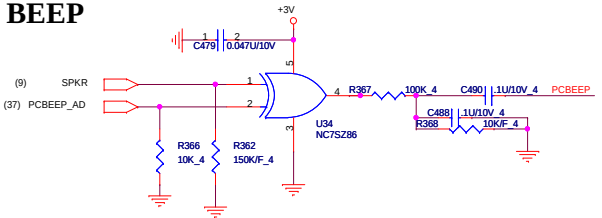
Speaker Amplifier(AMP)



Speaker(AMP)



PC BEEP



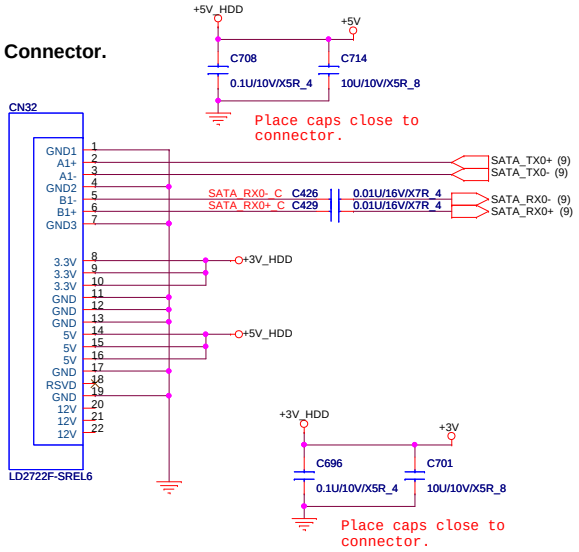
PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

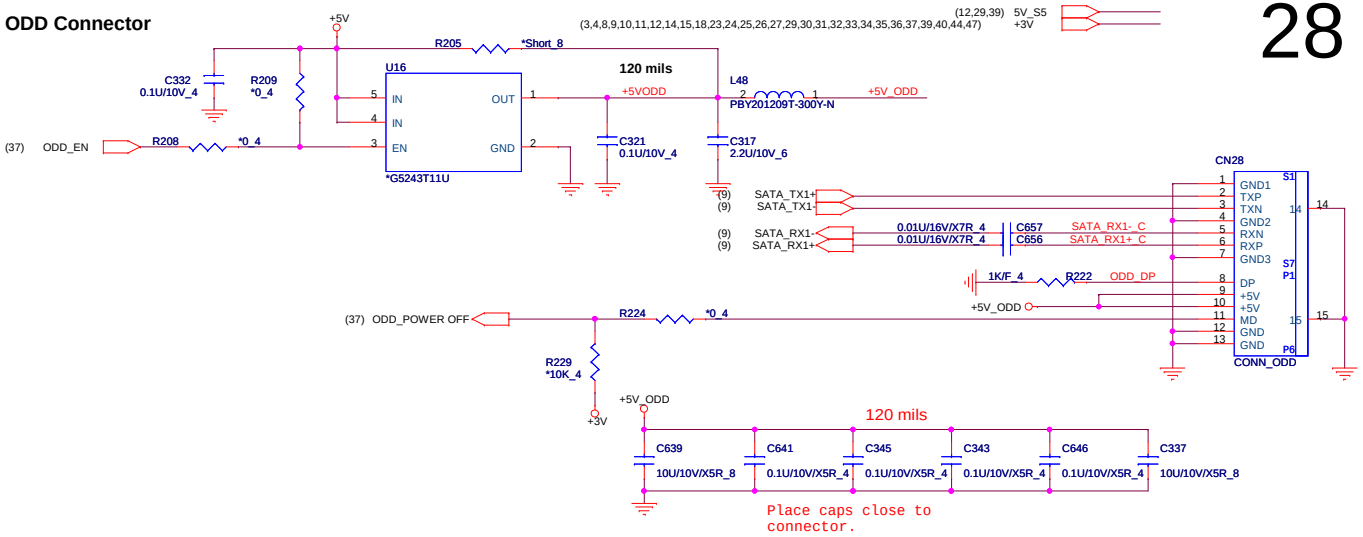
Size	Document Number	Rev
Custom	AL272/AMP/MIC/LINE-OUT	1A

Date: Wednesday, December 23, 2009 Sheet 27 of 53

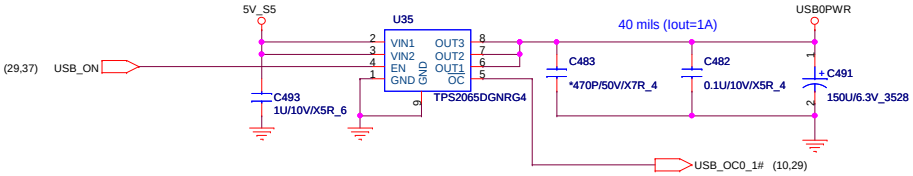
SATA Connector.

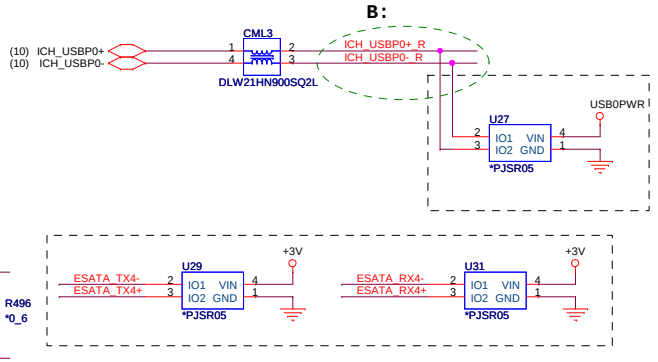


ODD Connector

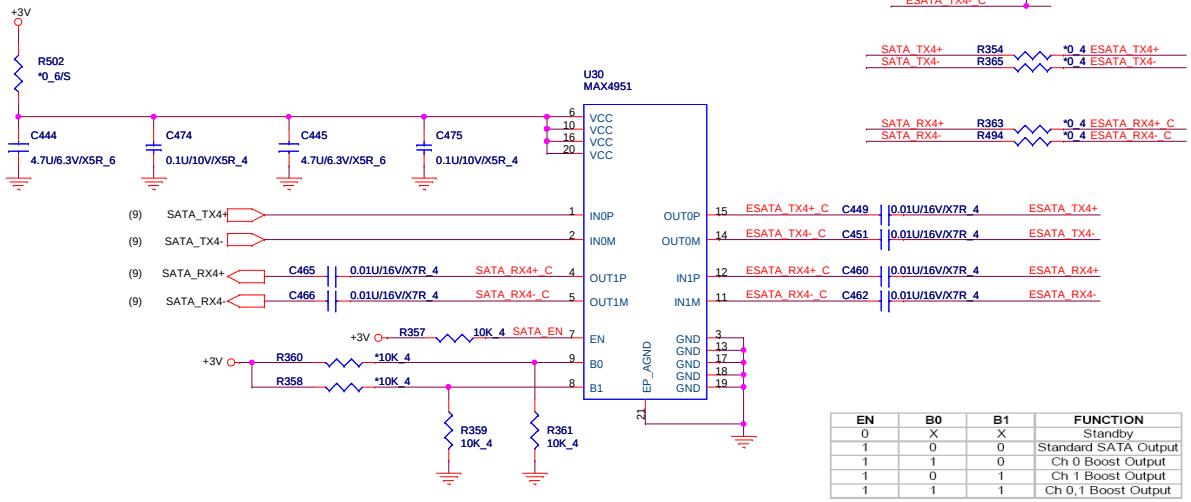


USB + E-SATA

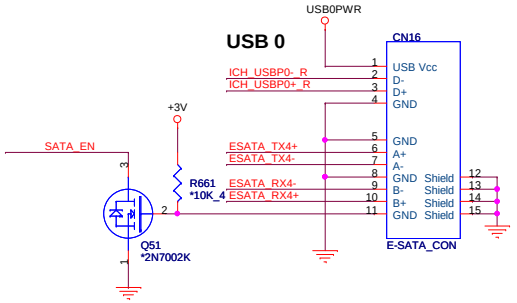




E-SATA RE-DRIVER



EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output



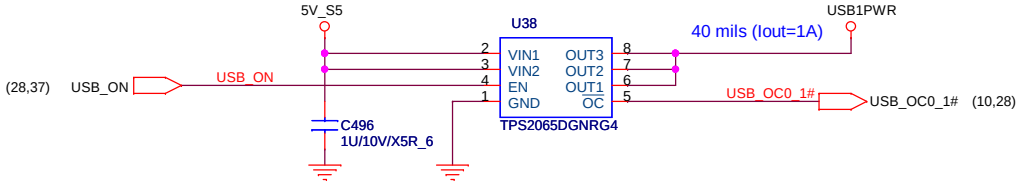
PROJECT KL3 NOTE Calpella DIS

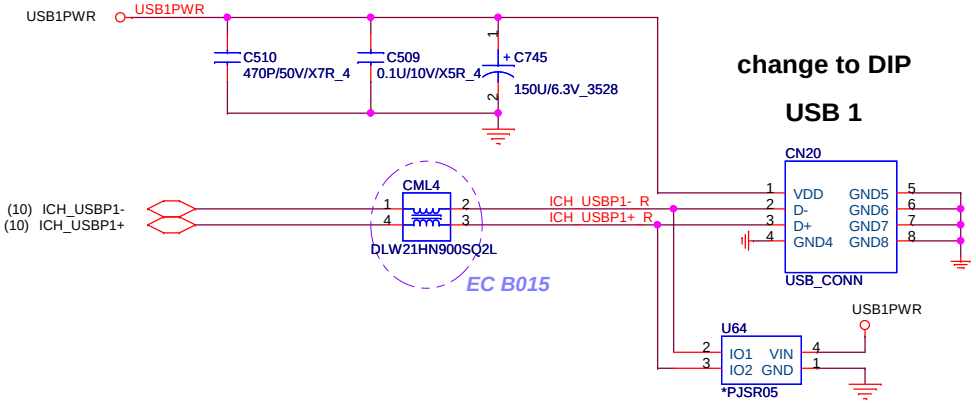
Quanta Computer Inc.

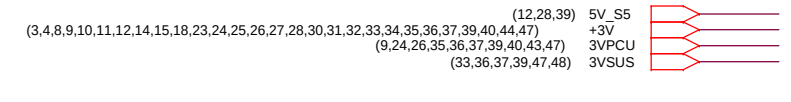
Size	Document Number	Rev
Custom	SATA HDD/ESATA/CD-ROM	1A

Date: Wednesday, December 23, 2009 Sheet 28 of 53

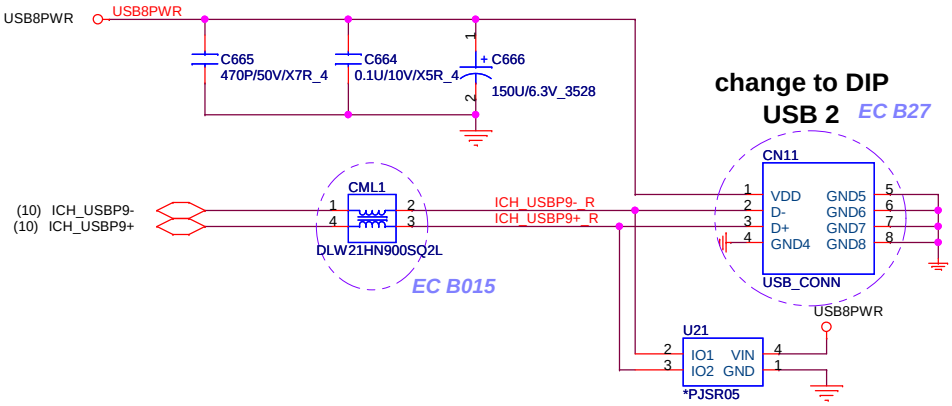
USBX3

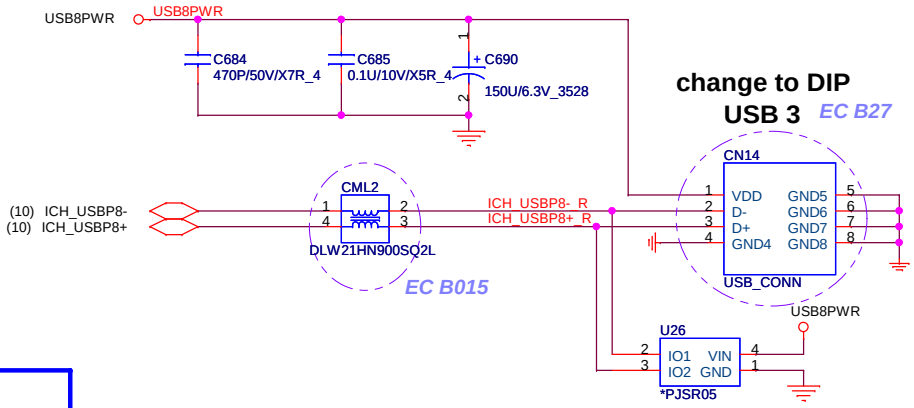




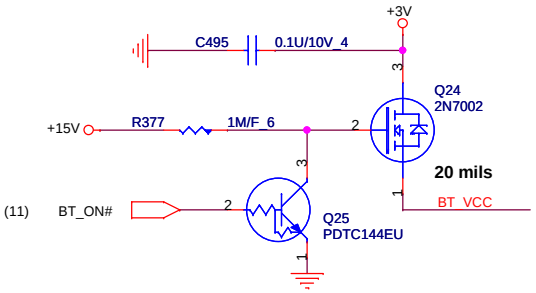


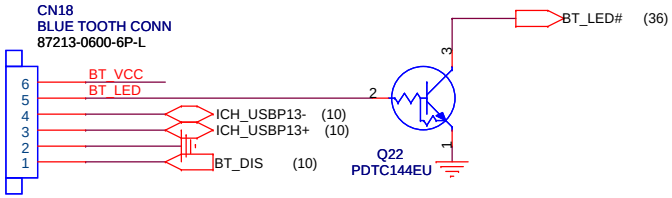
29

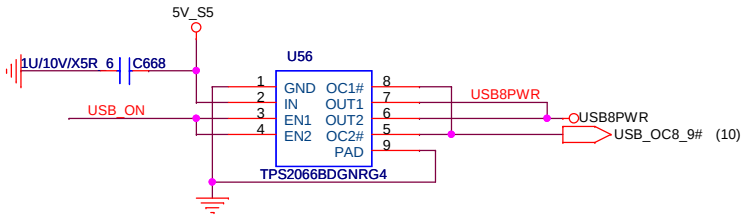




BLUETOOTH







PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB X3/BT	1A

Date: Wednesday, December 23, 2009 Sheet 29 of 53

C640 & C639 close to APVDD(pin5)
(length must under 120mil) and
trace width = 30mil, after C640,
pls put one more 0.1uF for it.

+1.8V_VDD
C694 10U/6.3V/X5R_6
C681 0.1U/10V/X5R_4
C680 0.1U/10V/X5R_4
C706 0.1U/10V/X5R_4
C695 1000P/50V/X7R_4

+3V
R625 *Short_8
C703 10U/6.3V/X5R_6
C700 0.1U/10V/X5R_4
C717 0.1U/10V/X5R_4
C693 0.1U/10V/X5R_4
C713 0.1U/10V/X5R_4
+3V_CARD

JMB385 C Only
R618 *0_4

5 IN 1 CARD READER

U57
JMB385 C
JMB387 A

JMB387 A Only
R609 0_4

+1.8V_VDD
+3V_CARD

XD_D4/MS_D4
XD_D5/MS_D5
XD_D6/MS_D6
XD_D7/MS_D7
XD_RE#
XD_R/B#
XD_ALE
XD_CLE
XD_WP#/SD_WP/MMC_WP#
XD_CE#/MS_SCLK/SD_CLK_L
XD_WE#/MS_BS/SD_CMD
XD_D3/MS_D3/SD_D3
XD_D2/MS_D2/SD_D2
XD_D1/MS_D1/SD_D1
XD_D0/MS_D0/SD_D0

D26 *RB501V-40@NC
JMB387_INT# (11)
PWR_CTRL
SD_MMC_CD#
MS_CD#
xD_CD#
CR_CPPE#
R582 *0_4/S
CLK_PCIE_REQ1# (10)

JMICRON
(4,10,11,26,31,32,33) PLTRST#
PCIE_RX1+_C C679 0.1U/10V/X5R_4
PCIE_RX1-_C C678 0.1U/10V/X5R_4
PCIE_RX1+ (10)
PCIE_RX1- (10)
(10) CLK_PCH_SRC1_N
(10) CLK_PCH_SRC1_P
R586 9.1K_4
PREXT
Trace width = 12mil" at PREXT
PCIE_TX1- (10)
PCIE_TX1+ (10)

CN22
R015-212-LM
VCC_XD

Memory Card Power Supply

250mA
PWR_CTRL
VCC_XD

Use 0805 type and
Trace width = 30 mil"
at MC_PWR_CTRL#,
C686 0.1U/10V/X5R_4
C688 10U/6.3V/X5R_6

XD_CE#/MS_SCLK/SD_CLK_L R599 22_4 XD_CE#/MS_SCLK/SD_CLK

+3V_CARD
R583 4.7K_4 xD_CD#
R584 4.7K_4 MS_CD#
R585 4.7K_4 SD_MMC_CD#
R604 10K_4 XD_CLE

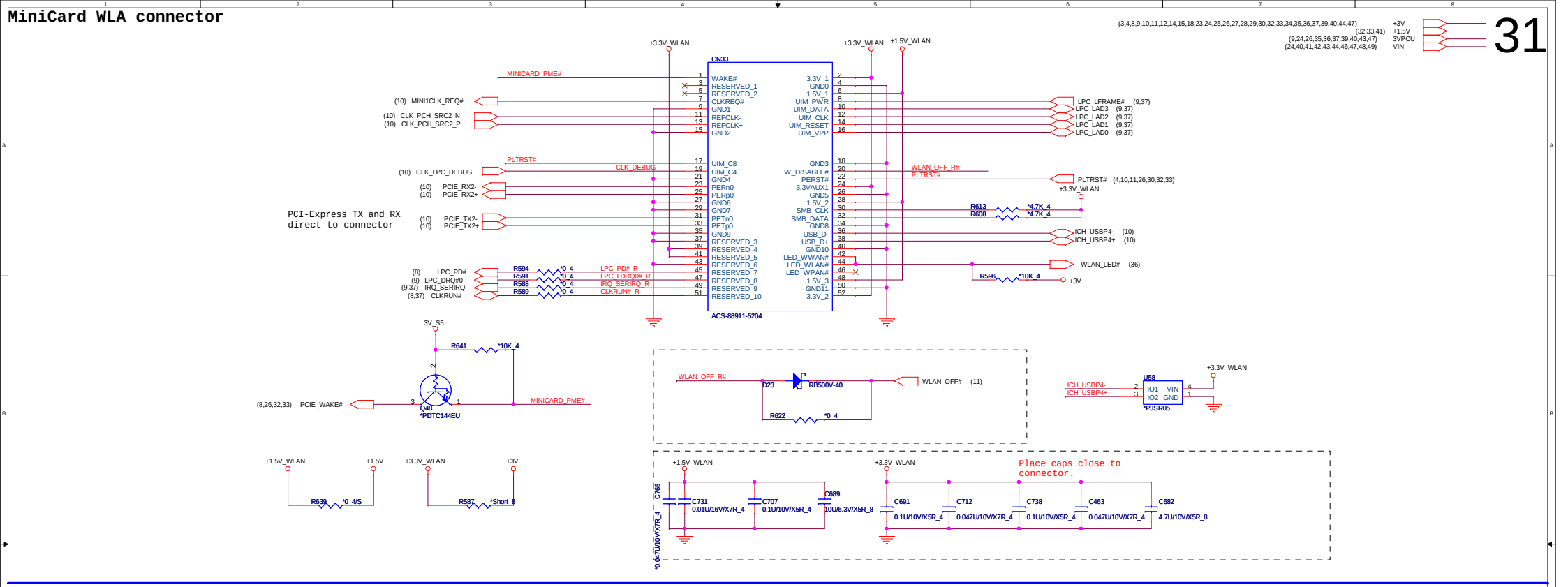
VCC_XD
R597 10K_4 XD_WE#/MS_BS/SD_CMD
R615 1K_4 XD_R/B#
R602 10K_4 XD_WP#/SD_WP/MMC_WP#
XD_RE# R620 200K_4
XD_ALE R616 200K_4

PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.

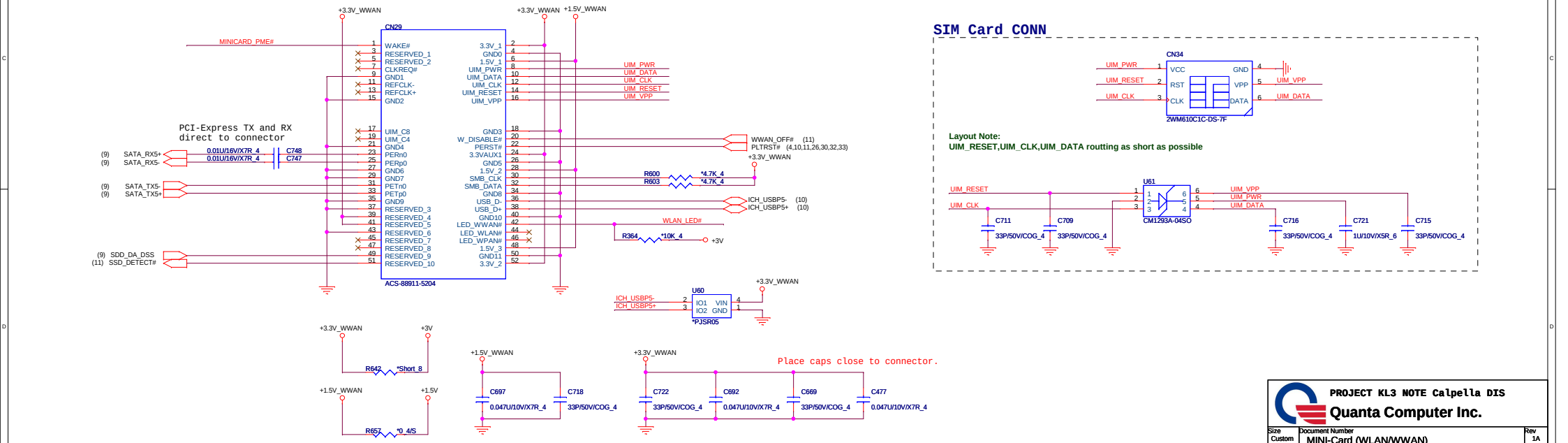
Size	Document Number	Rev
Custom	JMB385/387 Card Reader	1A

Date: Wednesday, December 23, 2009 Sheet 30 of 53

MiniCard WLA connector



MiniCard WWAN/SATA SSD connector



PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

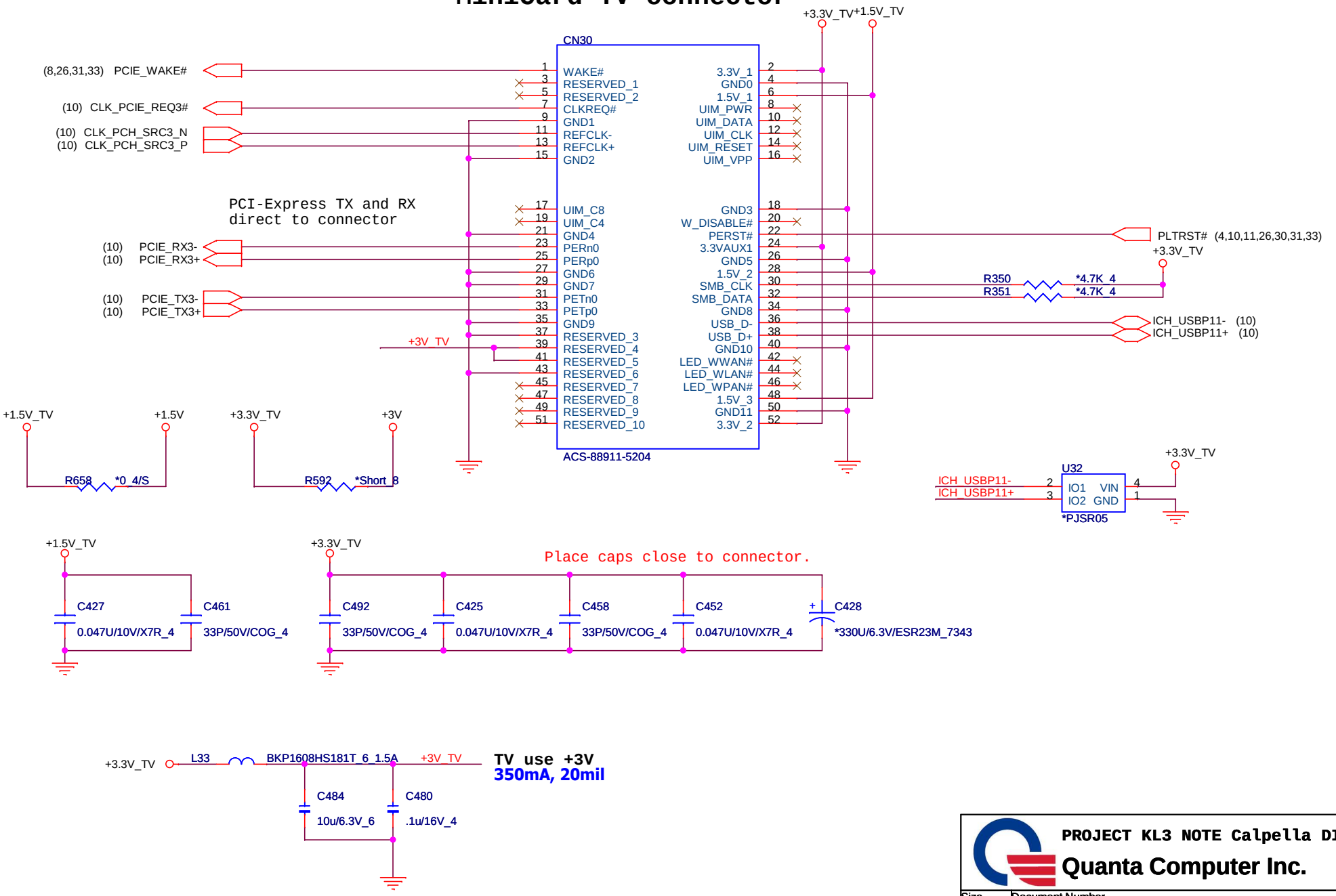
Size	Document Number	Rev
Custom	MINI-Card (WLAN/WWAN)	1A

Date: Wednesday, December 23, 2009 Sheet 31 of 53

(3,4,8,9,10,11,12,14,15,18,23,24,25,26,27,28,29,30,31,33,34,35,36,37,39,40,44,47) +3V
(31,33,41) +1.5V

32

MiniCard TV connector



PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-Card (TV)	1A
Date: Wednesday, December 23, 2009	Sheet 32 of 53	

Express Card

33

(3,4,8,9,10,11,12,14,15,18,23,24,25,26,27,28,29,30,31,32,34,35,36,37,39,40,44,47) +3V
(31,32,41) +1.5V
(36,37,39,47,48) 3VSUS

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA.

(10) ICH_USBP2+
(10) ICH_USBP2-
L51
*DLW21HN900SQ2L
ICH_USBP2+
ICH_USBP2-
+3.3V_CARD
U62
IO1 VIN
IO2 GND
*PJSR05
FOR ESD

+1.5V +3V 3VSUS
U63
AUXIN 3.3VIN_0 3.3VIN_1 1.5VIN_0 1.5VIN_1
AUXOUT 3.3VOUT_0 3.3VOUT_1 1.5VOUT_0 1.5VOUT_1
+3.3V_CARDAUX +3.3V_CARD +1.5V_CARD
ExpressSwitch
SHDN# STBY# SYSRST# NC GND0
PERST# CPPE# CPUSB# OC# RCLKEN
3VSUS
R643 *100K_4 2231_SHDN#
R644 *100K_4 2231_STBY#
(4,10,11,26,30,31,32) PLTRST#
CARD_RESET#
EXPRCRD_PWREN#
CPUSB#
R634 *100K_4
R633 *100K_4
T34
T33
G577BSR91U/ RT9716AGQW

CN31
GND4 USB_D- USB_D+ CPUSB# RESERVED2 RESERVED1 SMB_CLK SMB_DATA +1.5V2 +1.5V1 WAKE# +3.3VAUX PERST# +3.3V2 +3.3V1 CLKREQ# CPPE# REFCLK- REFCLK+ GND3 PERn0 PERp0 GND2 PETn0 PETp0 GND1
SHIELD5 SHIELD4 SHIELD3 SHIELD2 SHIELD1
ICH_USBP2-
ICH_USBP2+
CPUSB#
+3.3V_CARDAUX
R619 10K_4
R614 10K_4
+1.5V_CARD
(8,26,31,32) PCIE_WAKE#
+3.3V_CARDAUX
CARD_RESET#
+3.3V_CARD
(10) CARD_CLK_REQ#
(11) EXPRCRD_PWREN#
(10) CLK_PCH_SRC4_N
(10) CLK_PCH_SRC4_P
EXPRCRD_PWREN#
(10) PCIE_RX4-
(10) PCIE_RX4+
(10) PCIE_TX4-
(10) PCIE_TX4+
NEW_CARD_CON

PCI-Express TX and RX direct to connector.

JAE PX10FS16PH-26P

+3V C743 0.1U/10V/X5R_4 10
Please the cap near pin 2 & 4 (3.3VIN).

3VSUS C732 0.1U/10V/X5R_4 10
Please the cap near pin 17 (AUXIN).

+3.3V_CARDAUX C727 0.1U/10V/X5R_4
Please the cap near pin 15 (AUXOUT).

+3.3V_CARD C742 0.1U/10V/X5R_4
Please the cap near pin 3 & 5 (3.3VOUT).

+1.5V_CARD C725 0.1U/10V/X5R_4
Please the cap near pin 11 & 13(1.5VOUT).

+1.5V_CARD C704 0.1U/10V/X5R_4 C702 0.1U/10V/X5R_4
Please the cap near connector.

+3.3V_CARD C453 0.1U/10V/X5R_4 C459 0.1U/10V/X5R_4 C448 10U/6.3V/X5R_6
Please the cap near connector.

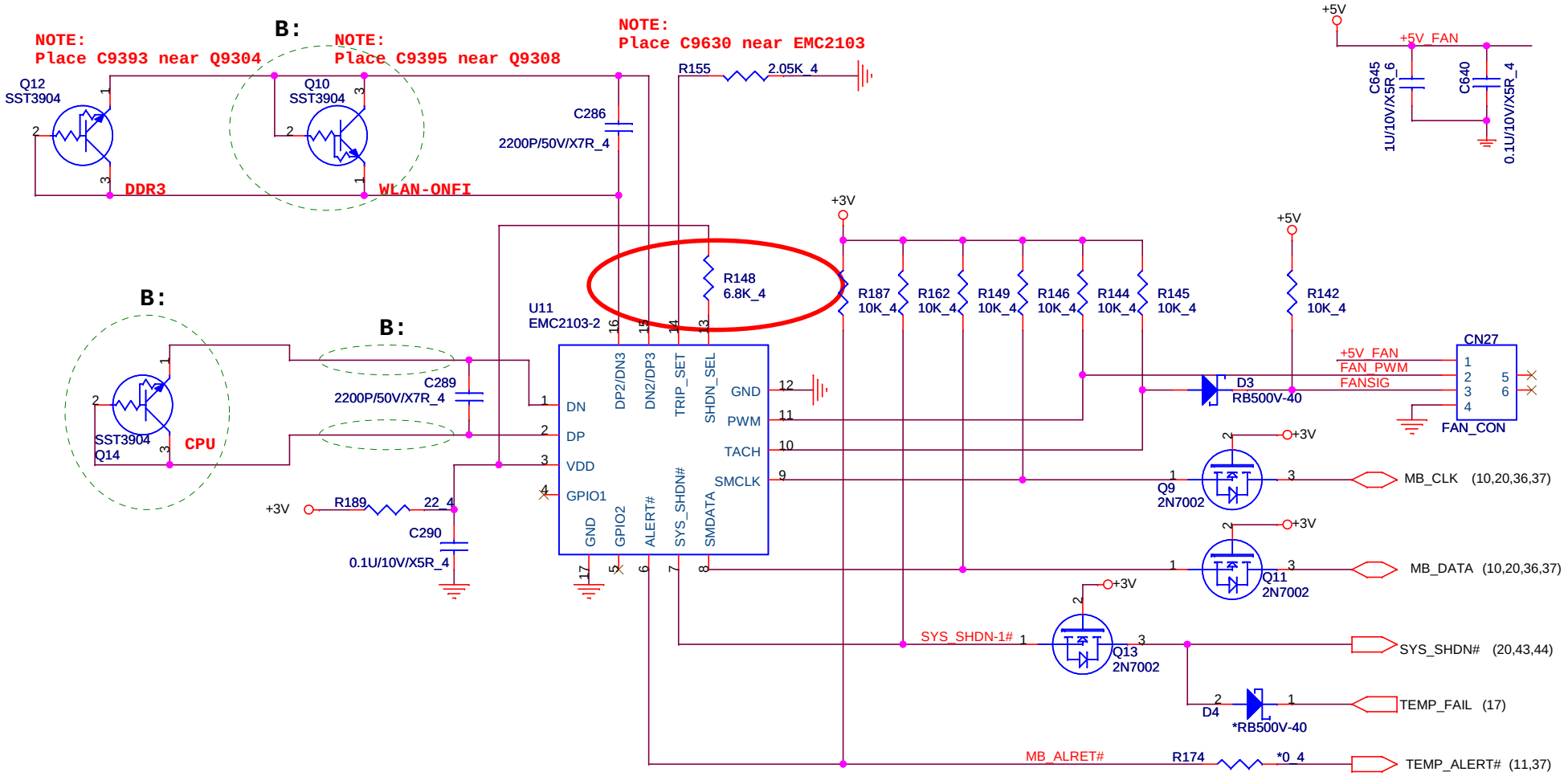
+1.5V C728 0.1U/10V/X5R_4 10
Please the cap near pin 12 & 14(1.5VIN).

PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Express Card	1A
Date: Wednesday, December 23, 2009	Sheet 33 of 53	

FAN CONTROL

(3,4,8,9,10,11,12,14,15,18,23,24,25,26,27,28,29,30,31,32,33,35,36,37,39,40,44,47) +3V
(12,23,24,25,27,28,35,37,39,40,45) +5V



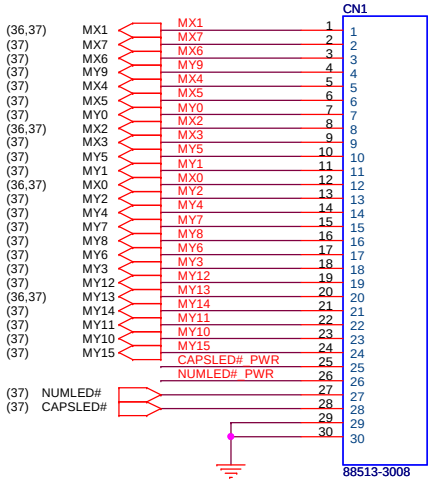
PROJECT KL3 NOTE Calpella DIS

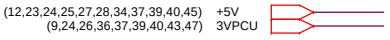
Quanta Computer Inc.

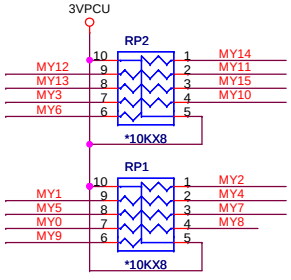
Size	Document Number	Rev
Custom	FAN /THERMAL	1A

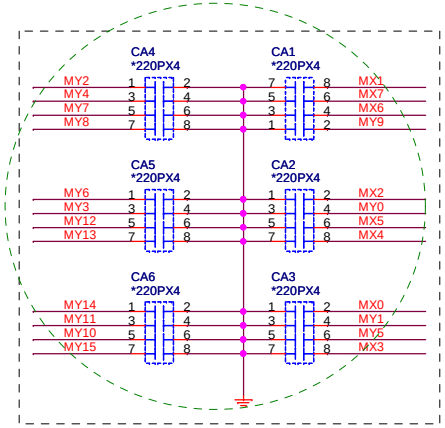
Date: Wednesday, December 23, 2009 Sheet 34 of 53

KEYBOARD



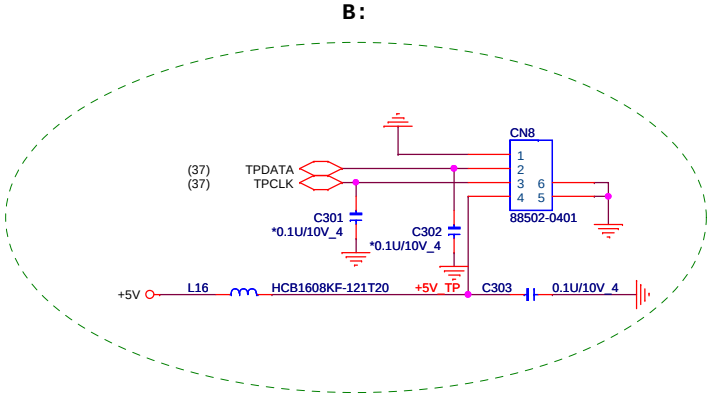




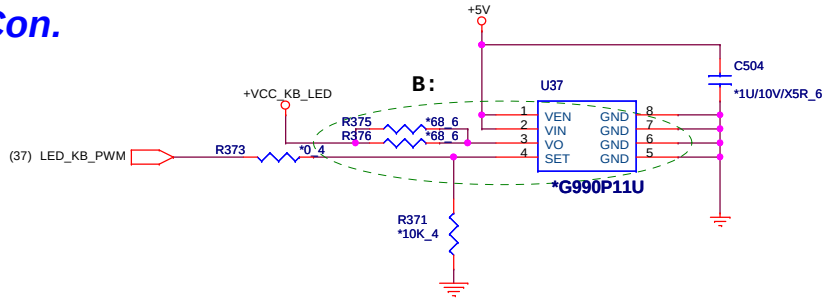


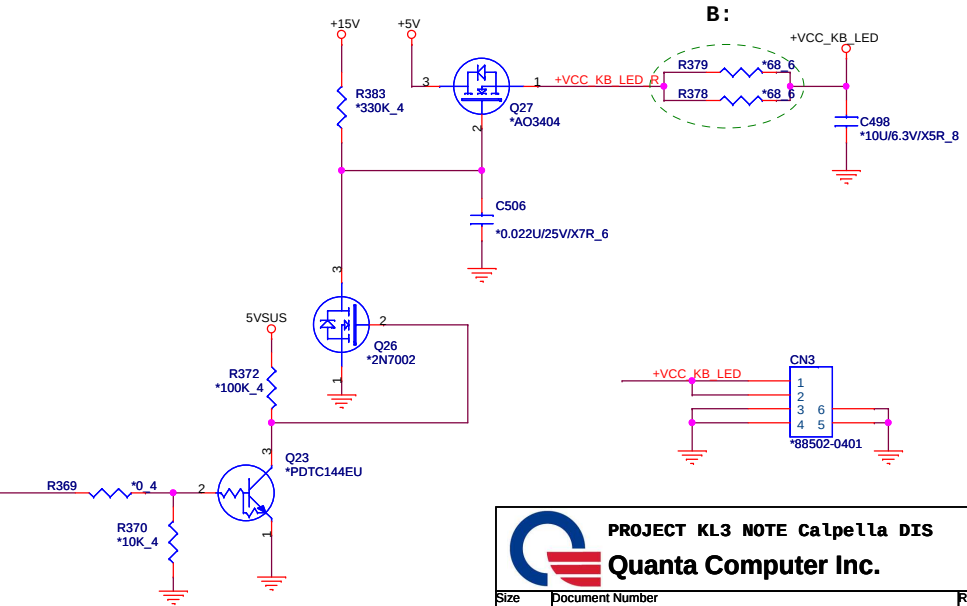
For EMI request

Touch pad



Backlight Keyboard Con.





PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

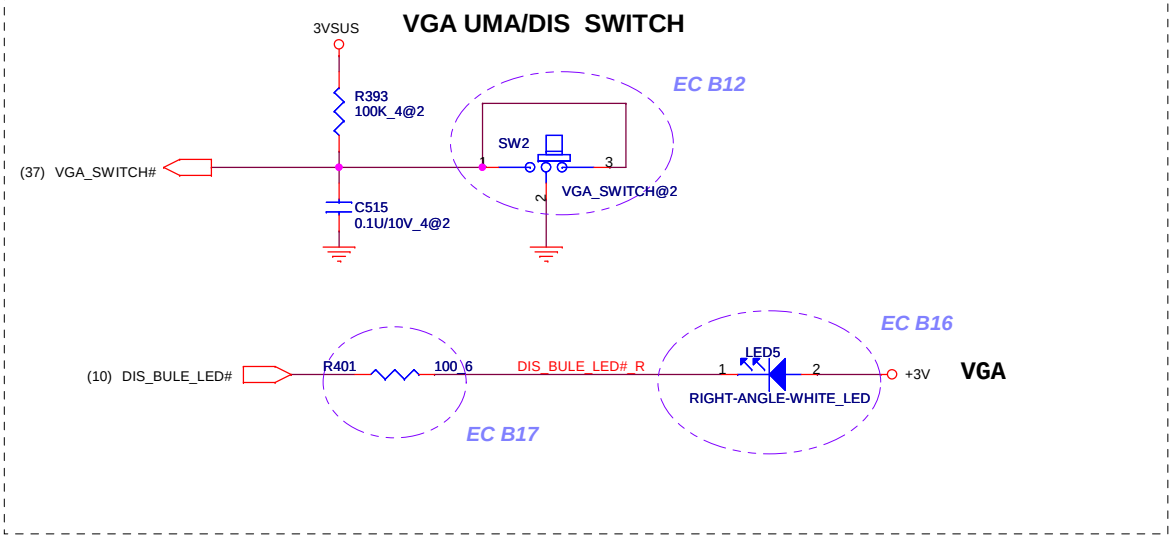
Size	Document Number	Rev
Custom	K/B, T/P	1A

Date: Wednesday, December 23, 2009 Sheet 35 of 53

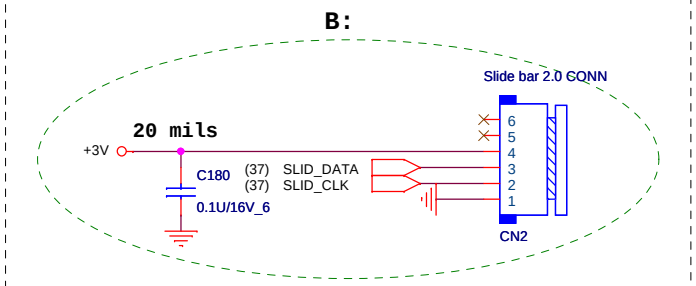
(9,24,26,35,37,39,40,43,47) 3VPCU

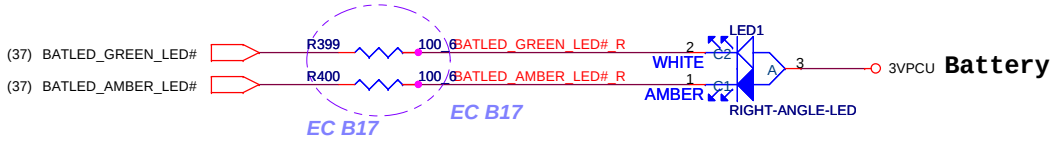
(3,4,8,9,10,11,12,14,15,18,23,24,25,26,27,28,29,30,31,32,33,34,35,37,39,40,44,47) +3V

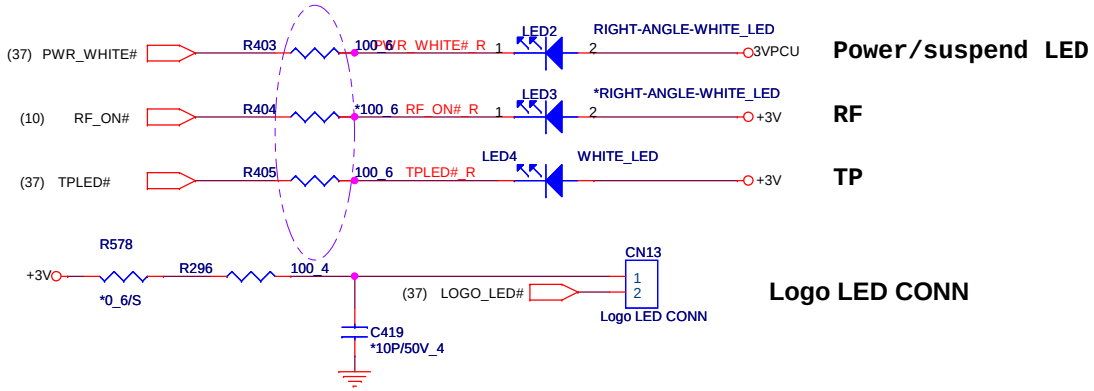
VGA UMA/DIS SWITCH



Slide bar 2.0







UP LED BOARD

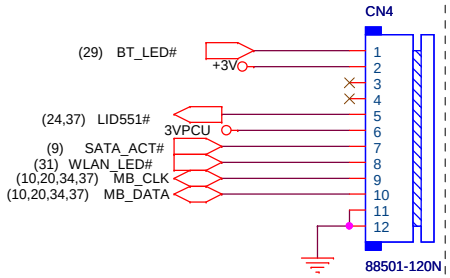
BT

LID SWITCH

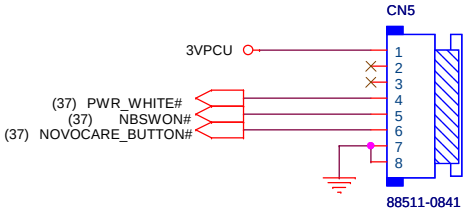
HDD

WLAN

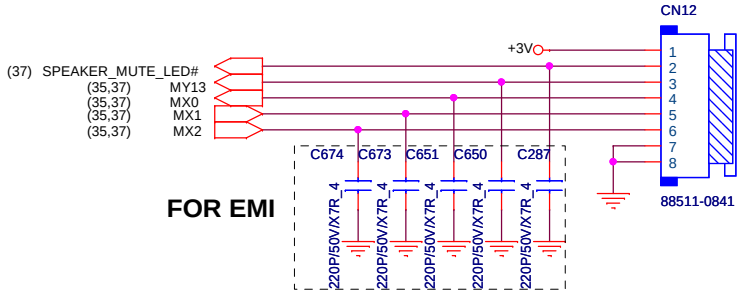
LIGHT SENSOR



LEFT POWER BOARD



RIGHT VOLUME BOARD



FOR EMI

PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	B TO B CON/LED	1A

Date: Wednesday, December 23, 2009 Sheet 36 of 53

(3,4,8,9,10,11,12,14,15,18,23,24,25,26,27,28,29,30,31,32,33,34,35,36,39,40,44,47) +3V
(9,24,26,35,36,39,40,43,47) 3VPCU
(9,12) +3VRTC
(12,23,24,25,27,28,34,35,39,40,45) +5V

IT8512

RF ON/OFF SWITCH

POWER SWITCH/ NOVO BUTTON

16Mbit (2M Byte), SPI

Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13

FLASH TYPE SELECT

R609	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

(For PLL Power)

DIS =>R278
UMA=>R279

38

MiniCard WLAN

HOLE30 H-TC205I4BC146D146P2
HOLE33 H-TC205I4BC146D146P2

MiniCard WWAN

HOLE28 H-TC205I119BC79D79P2
HOLE31 H-TC205I119BC79D79P2

Hole for PCH support

HOLE27 H-TC205I99BC59D59P2
HOLE26 H-TC205I99BC59D59P2

Drink Hole

ESD for ESATA

Hole for CPU support

HOLE5 *h-tc236i157bc157d157pt
HOLE10 *h-tc236i157bc157d157pt
HOLE11 *h-tc236i157bc157d157pt
HOLE6 *h-tc236i157bc157d157pt

VGA nut

HOLE24 H-TC205I99BC59D59P2
HOLE25 H-TC205I99BC59D59P2

MiniCard TV

HOLE32 H-TC205I119BC79D79P2
HOLE29 H-TC205I119BC79D79P2

Boundary Hole

HOLE12 *H-C315D106P2
HOLE20 *H-C315D106P2
HOLE4 *H-TC197BC315D106P2
HOLE17 *H-C315D106P2
HOLE22 *H-C315D106P2
HOLE1 *H-C315D106P2
HOLE8 *H-C315D106P2
HOLE23 *H-C315I126D106P2
HOLE21 *H-C315D106P2
HOLE2 *H-C315D106P2

Boundary Hole

HOLE3 *H-TC197BC315D106P2
HOLE14 *H-TC197BC315D106P2
HOLE9 *H-O157X375D157X375N
HOLE19 *H-C118D118N
HOLE18 *H-C118D118N
HOLE7 *H-C1811D1811NA1851
HOLE15 *O-KL3A-1
HOLE13 O-KL3-2
HOLE16 O-KL3-3

Card reader board nut

Break Hole

Boundary Hole (ODD)

HDD PAD

ESD PAD

GP1 *spad-KL3A-1
GP2 spad-KL3A-1
GP3 spad-KL3A-2
GP4 spad-KL3A-3
GP5 spad-KL3A-4
GP6 spad-KL3A-5
GP7 spad-KL3A-6
GP8 spad-KL3A-7
GP9 spad-KL3A-8
GP10 spad-KL3A-9
GP11 spad-KL3A-10
GP12 spad-KL3A-11
GP13 *spad-KL3A-12
GP14 SPAD-KL3A-13

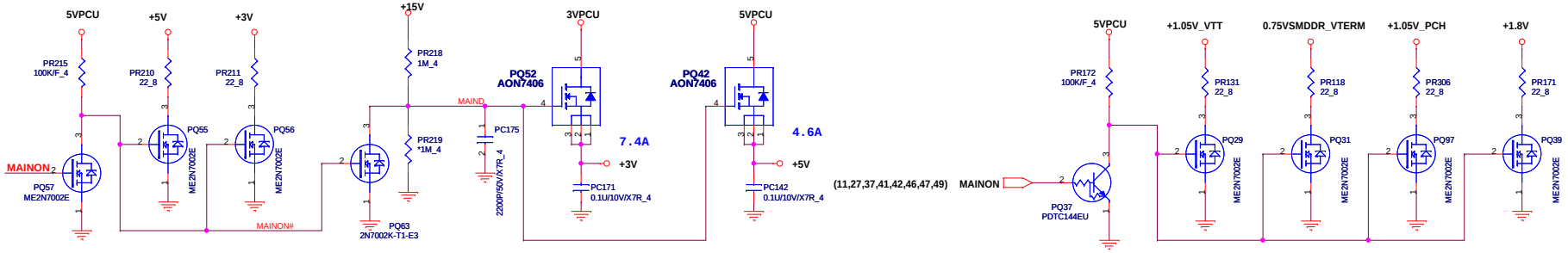
PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

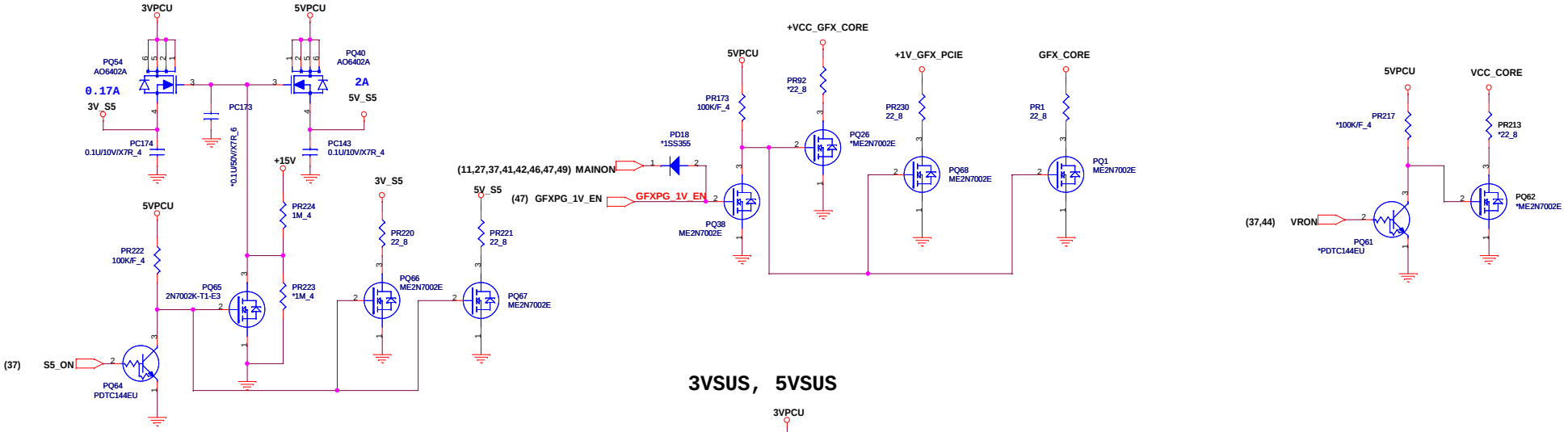
Size	Document Number	Rev
Custom	HOLD & SKEW	1A

Date: Wednesday, December 23, 2009 Sheet 38 of 53

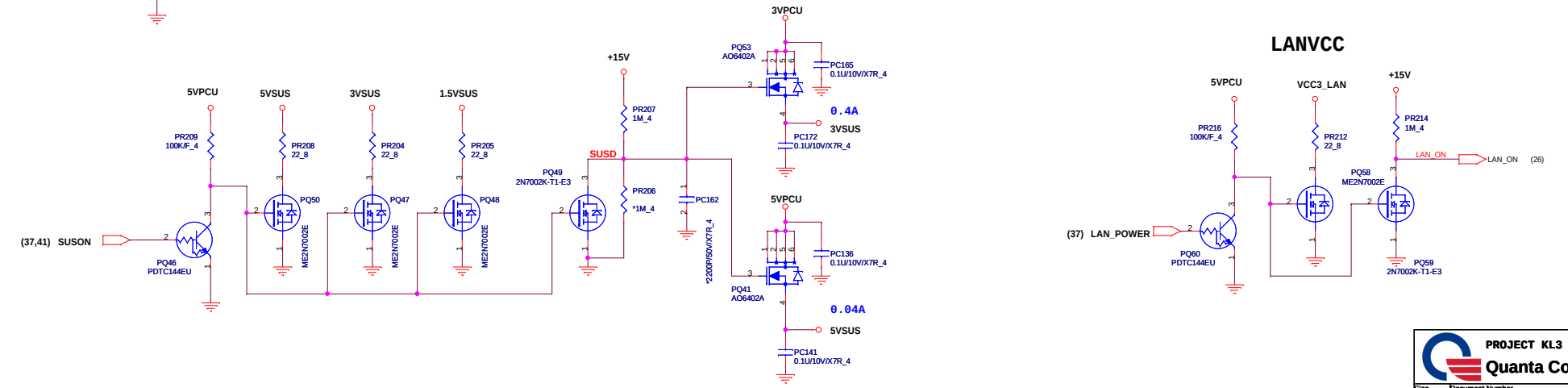
+3V, +5V



3V_S5, 5V_S5



3VSUS, 5VSUS



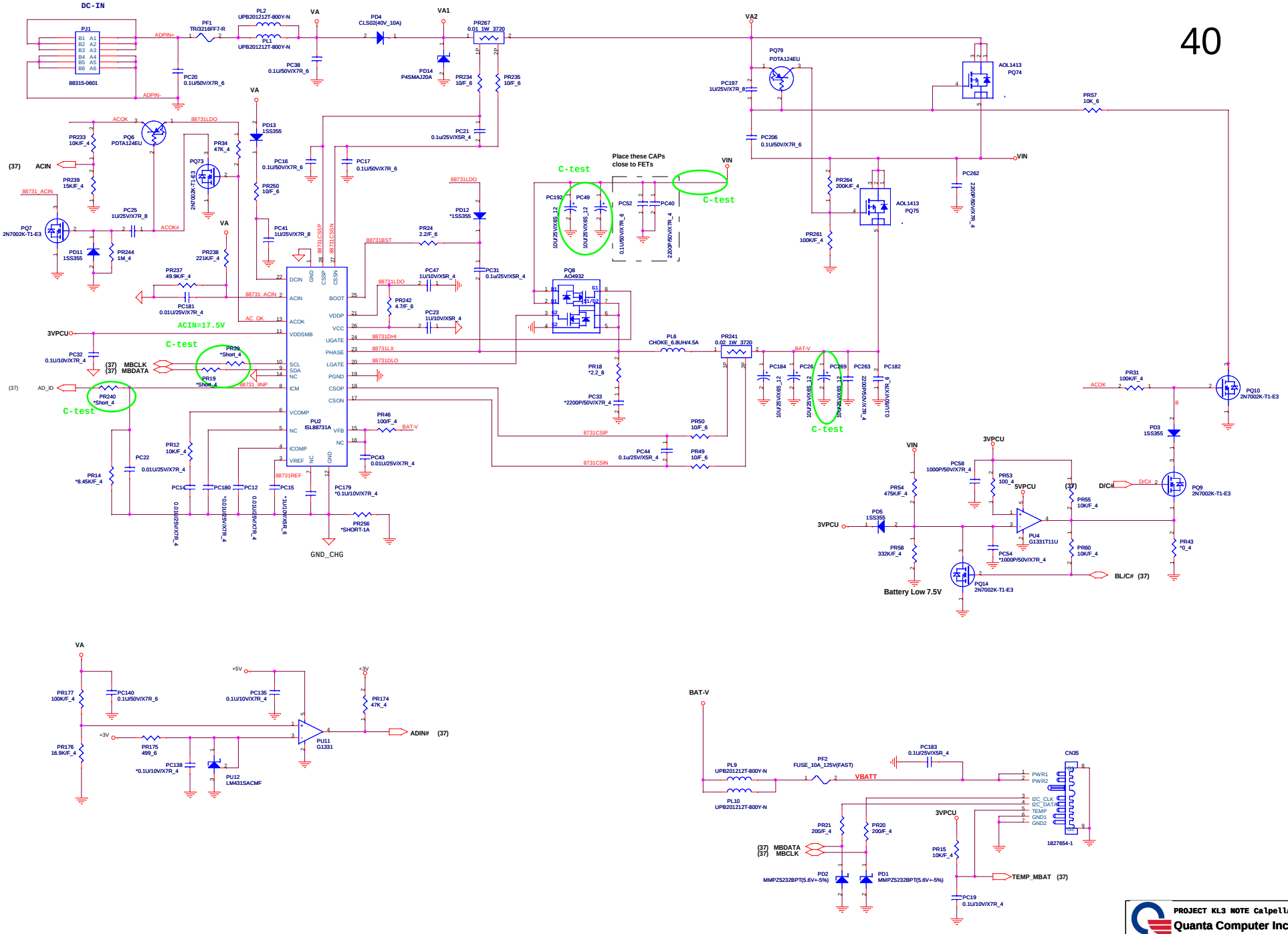
LANVCC

PROJECT KL3 NOTE Calpella DIS

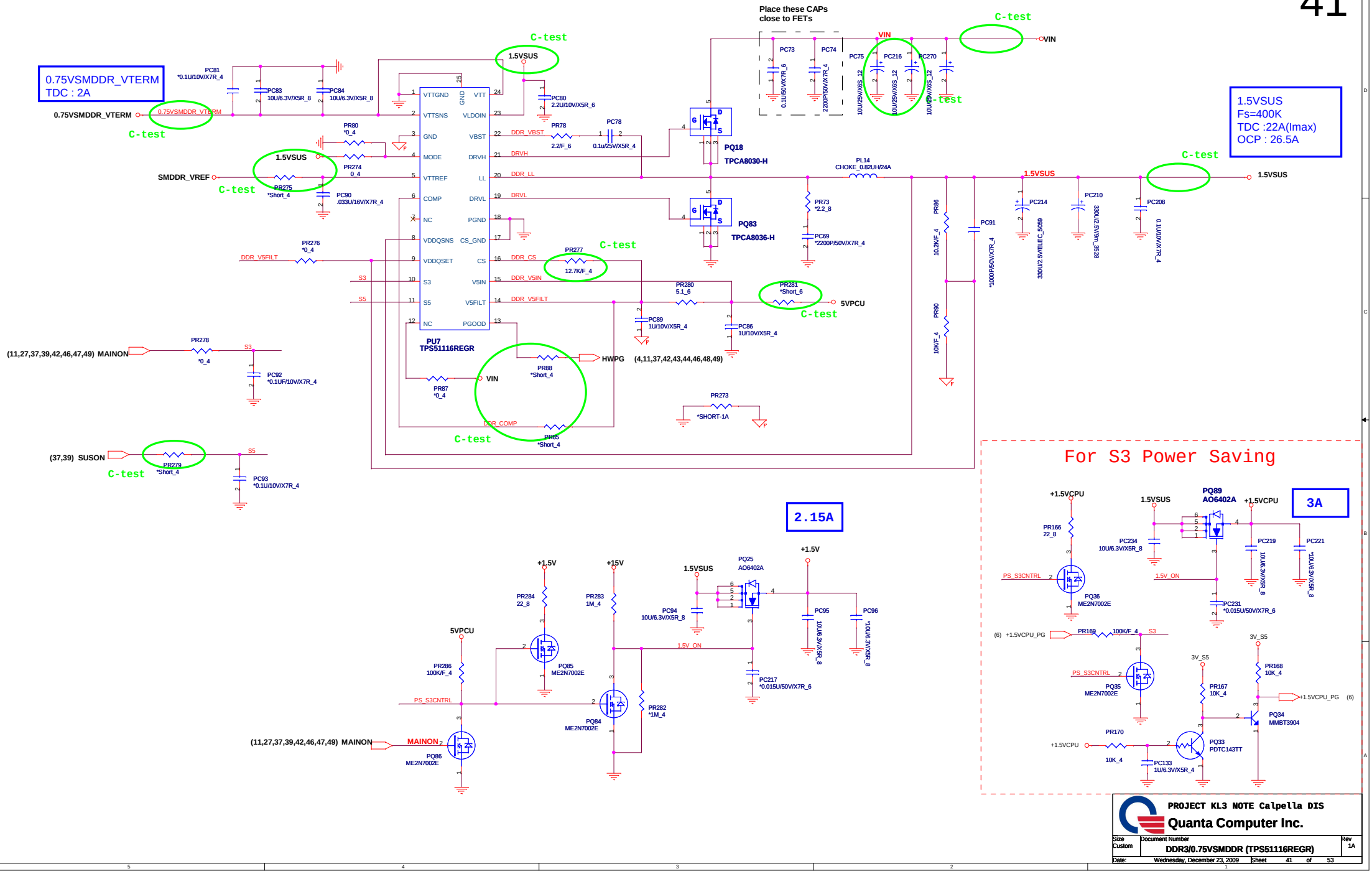
Quanta Computer Inc.

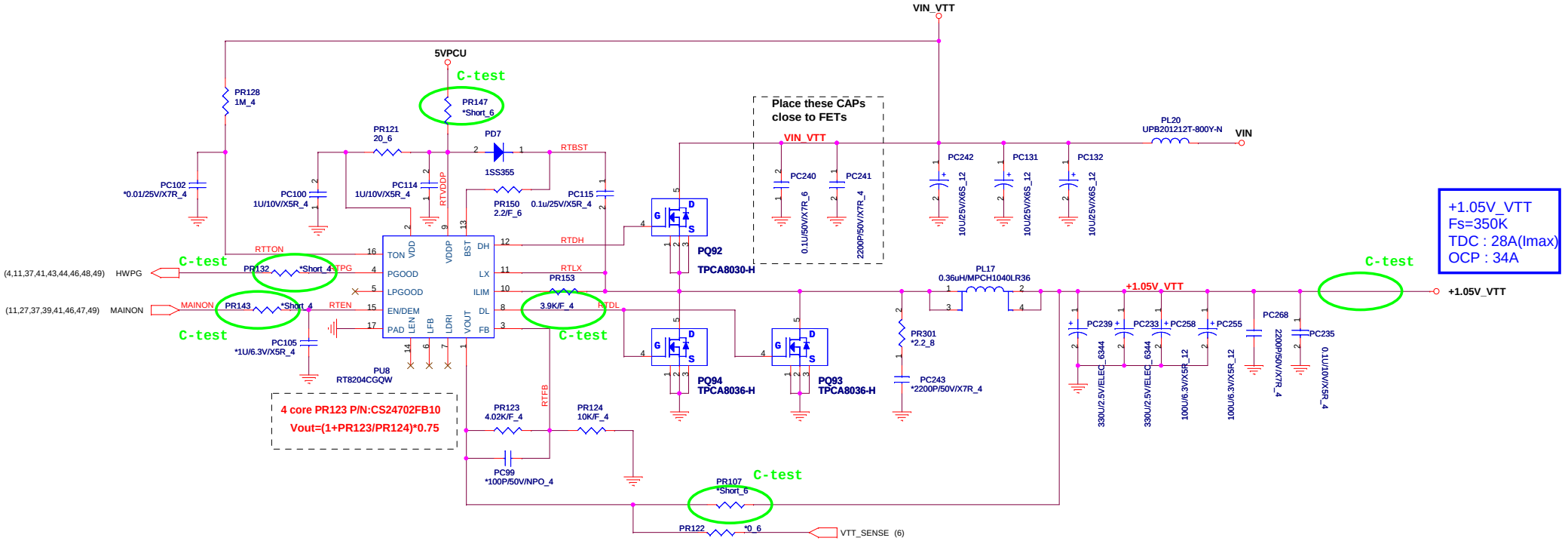
Size	Document Number	Rev
Custom	Discharge	1A
Date: Wednesday, December 23, 2009	Sheet 39 of 53	

R138=0.02m ohm for 65W adapter-->current limit is 3A;

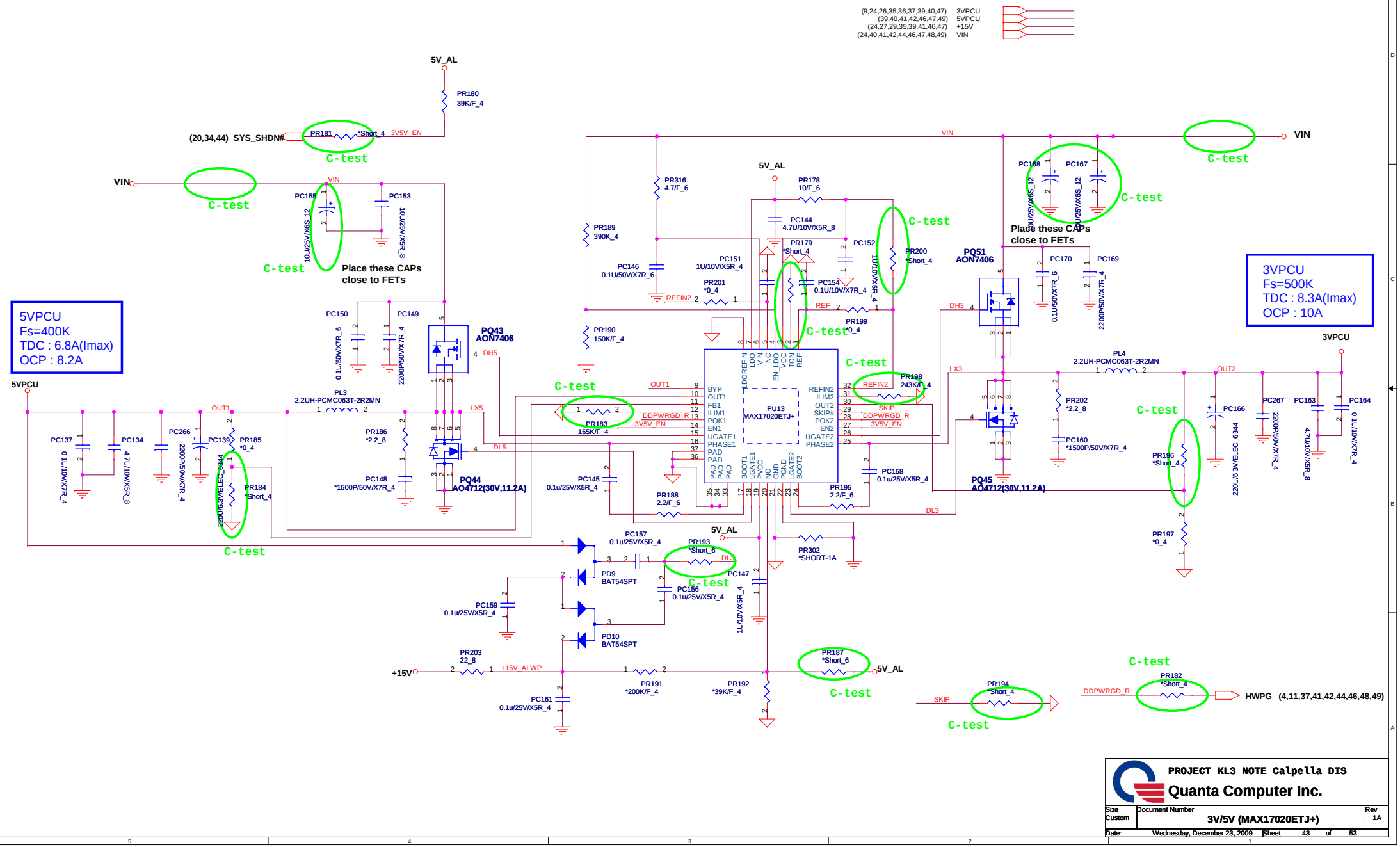


PROJECT KL3 NOTE Calpella DIS			
Quanta Computer Inc.			
Size: Custom	Document Number: Charger(MAX8731)		Rev: 1A
Date: Wednesday, December 23, 2009	Sheet 40 of 53		


0.75VSMDDR_VTERM
TDC : 2A
1.5VSUS
Fs=400K
TDC :22A(Imax)
OCP : 26.5A
Place these CAPs
close to FETs
C-test
PU7
TPS51116REGR
PQ18
TPCA8030-H
PQ83
TPCA8036-H
PL14
CHOKE_0.82UH/24A
5VPCU
HWPG
VIN
SMDDR_VREF
DDR_V5FILT
(11,27,37,39,42,46,47,49) MAINON
(37,39) SUSON
(4,11,37,42,43,44,46,48,49)
2.15A
3A
For S3 Power Saving
PQ89
AO6402A
PQ36
ME2N7002E
PQ35
ME2N7002E
PQ34
MMBT3904
PQ33
PDTC143TT
PQ25
AO6402A
PQ85
ME2N7002E
PQ84
ME2N7002E
PQ86
ME2N7002E
PS_S3CNTRL
1.5V_ON
3V_S5
+1.5VCPU_PG
PROJECT KL3 NOTE Calpella DIS
Quanta Computer Inc.
DDR3/0.75VSMDDR (TPS51116REGR)
Wednesday, December 23, 2009
Sheet 41 of 53



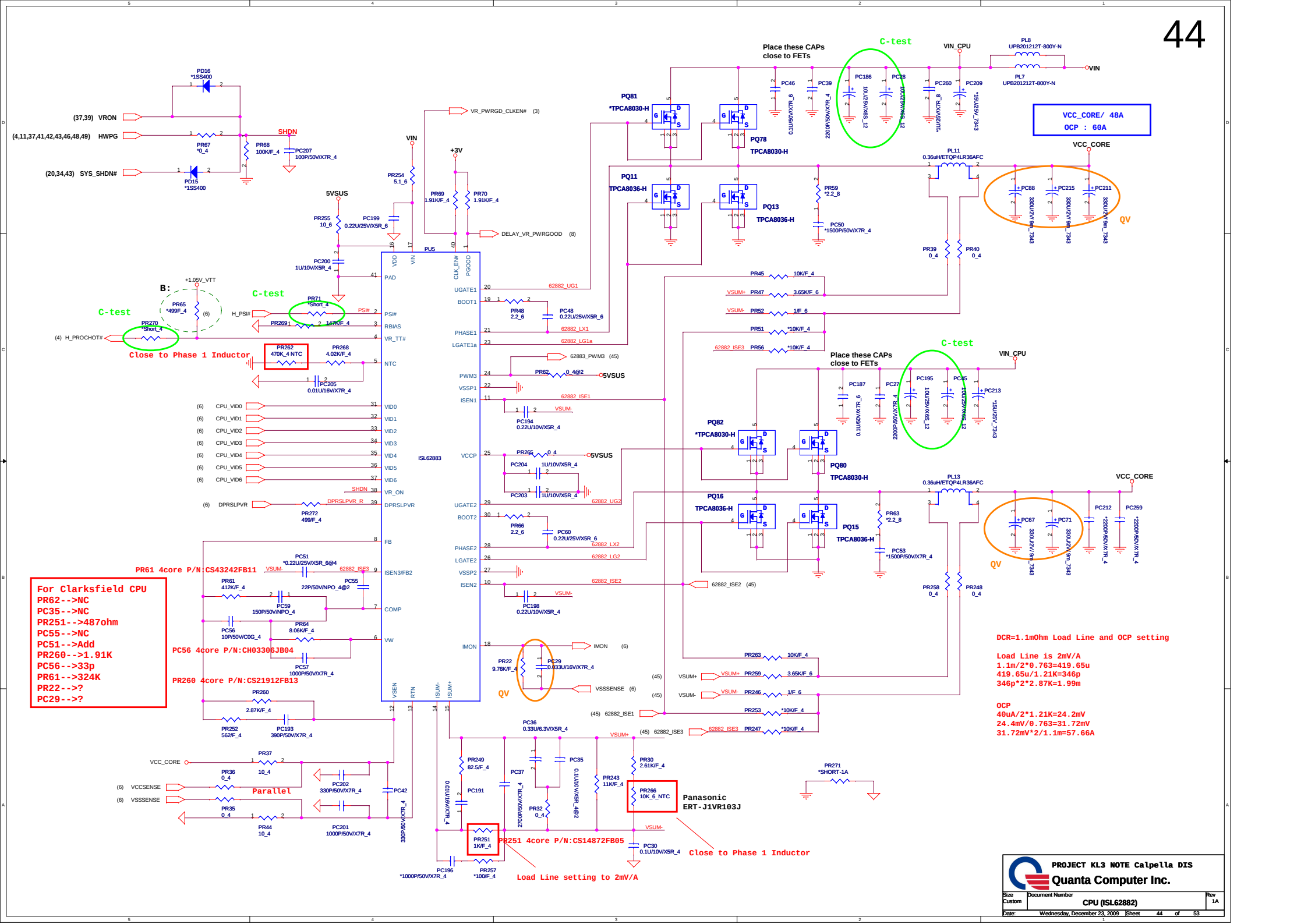
PROJECT KL3 NOTE Calpella DIS			
Quanta Computer Inc.			
Size: Custom	Document Number: 1.1V_VTT(RT8204)		Rev: 1A
Date: Wednesday, December 23, 2009	Sheet 42 of 53		



PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	3V/5V (MAX17020ETJ+)	1A
Date: Wednesday, December 23, 2009	Sheet 43 of 53	

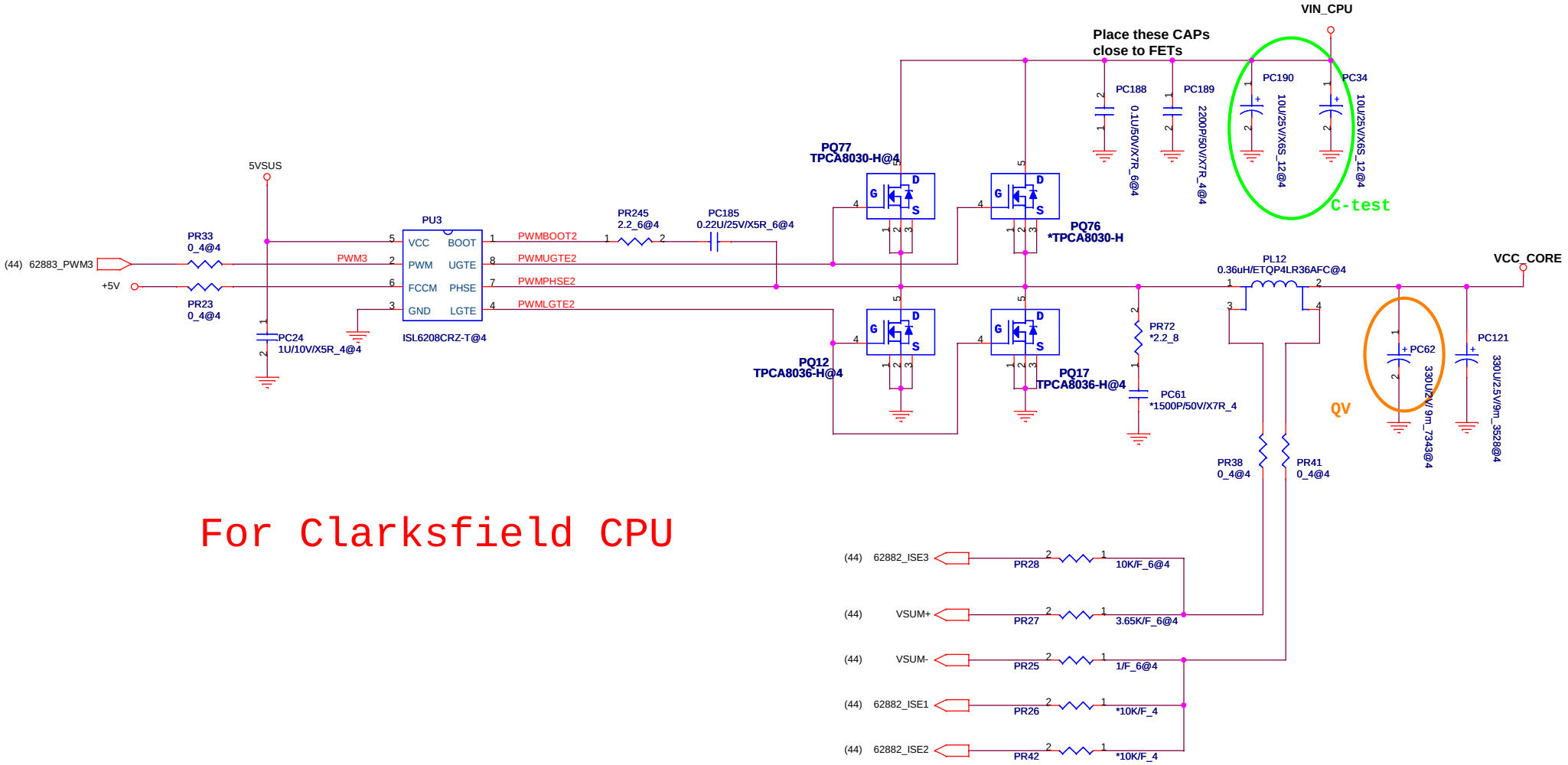


PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU (ISL62882)	1A

Date: Wednesday, December 23, 2009 Sheet 44 of 53



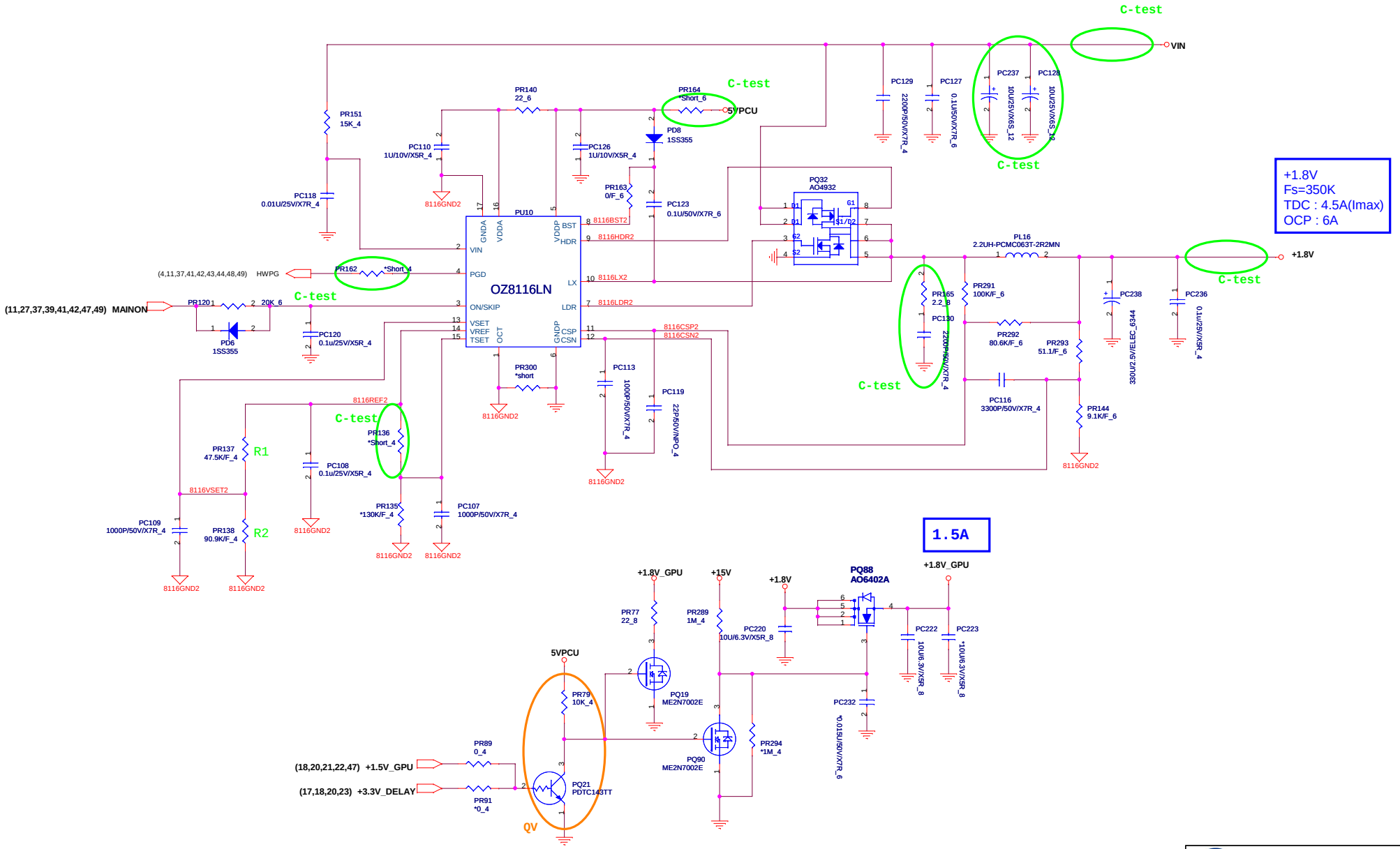
For Clarksfield CPU

PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU (ISL6208)	1A

Date: Wednesday, December 23, 2009 Sheet 45 of 53

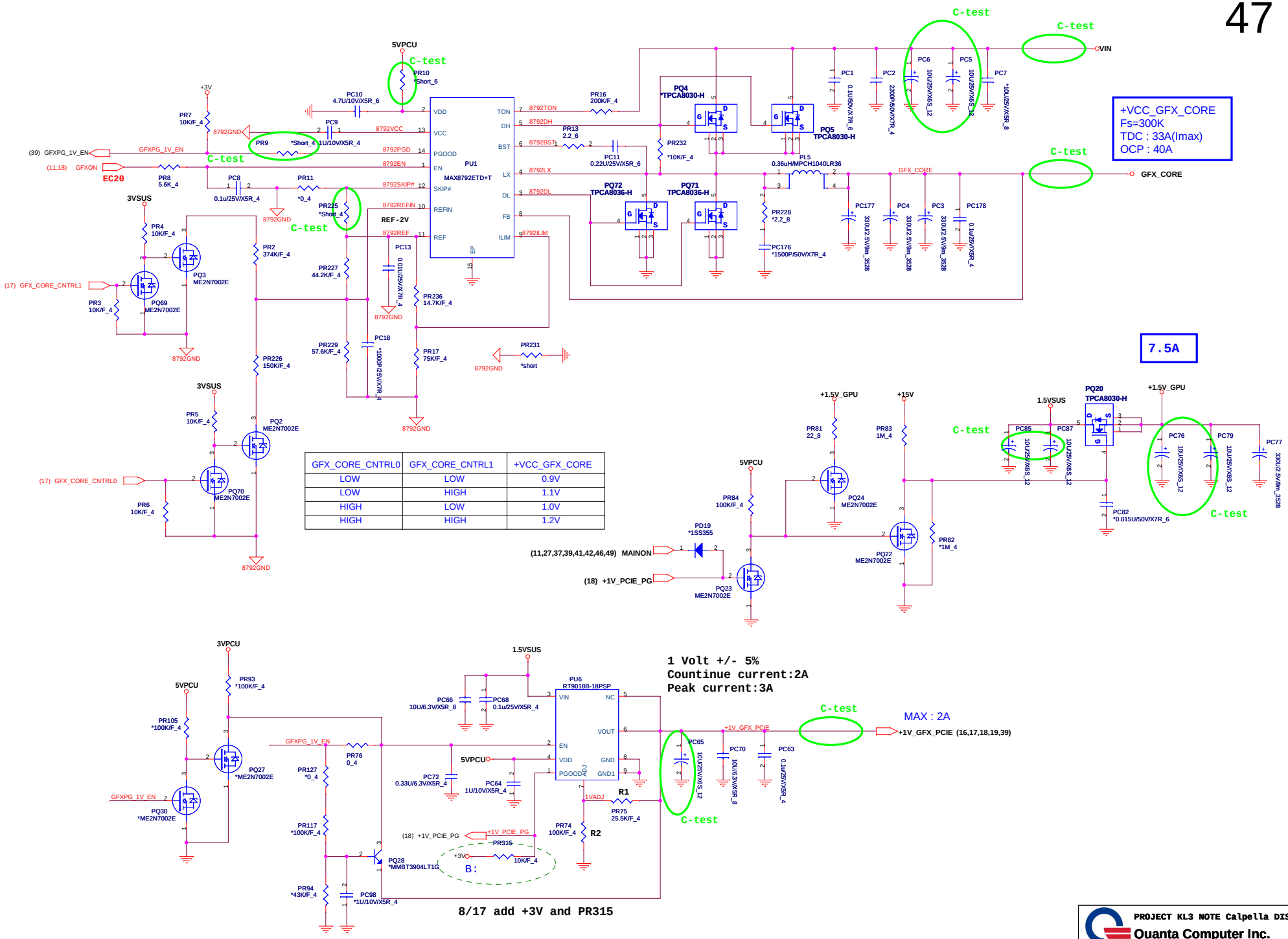


PROJECT KL3 NOTE Calpella DIS

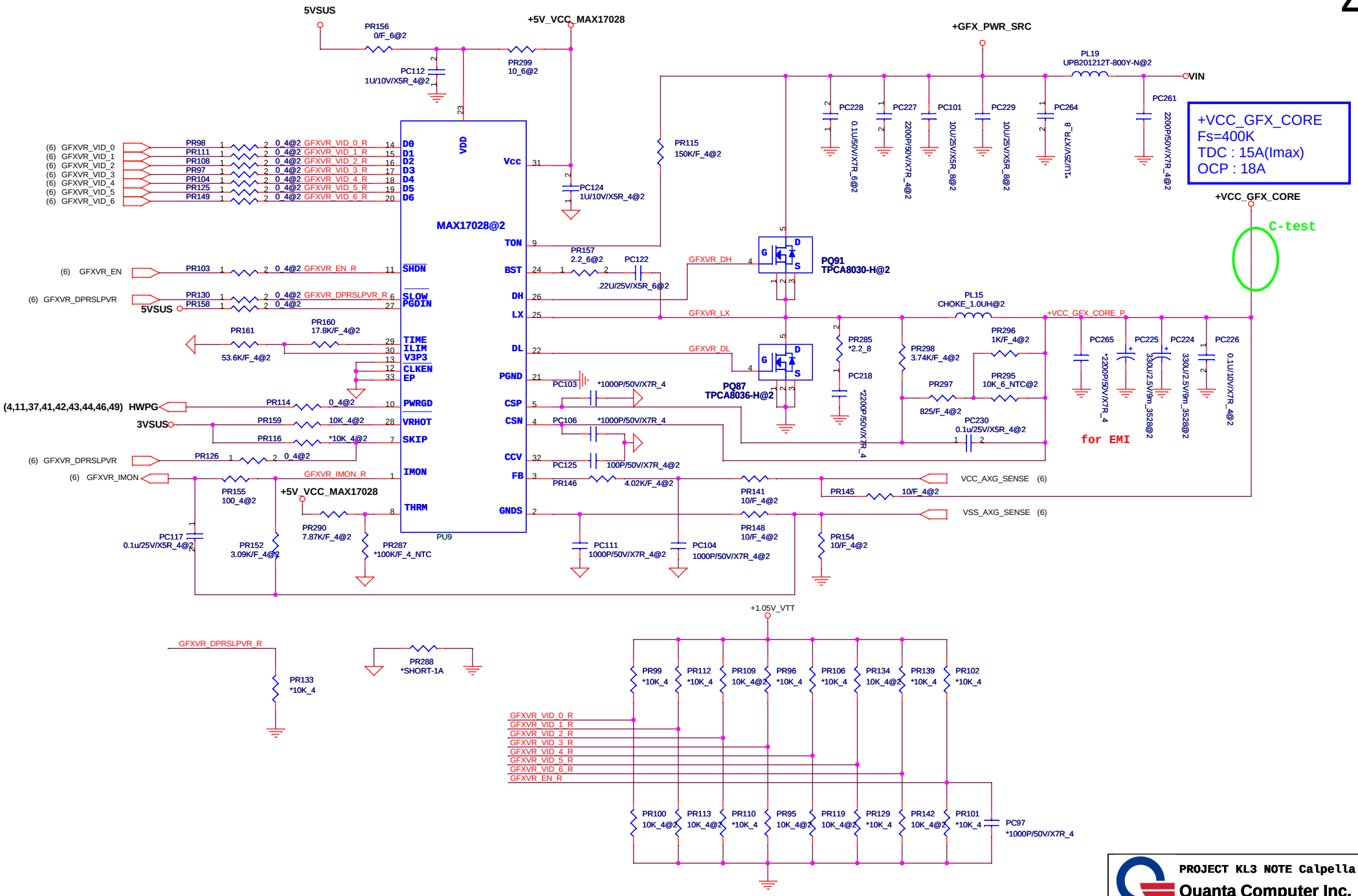
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DIS_1.8V_RUN (OZ8116LN)	1A

Date: Wednesday, December 23, 2009 Sheet 46 of 53



GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
LOW	HIGH	1.1V
HIGH	LOW	1.0V
HIGH	HIGH	1.2V

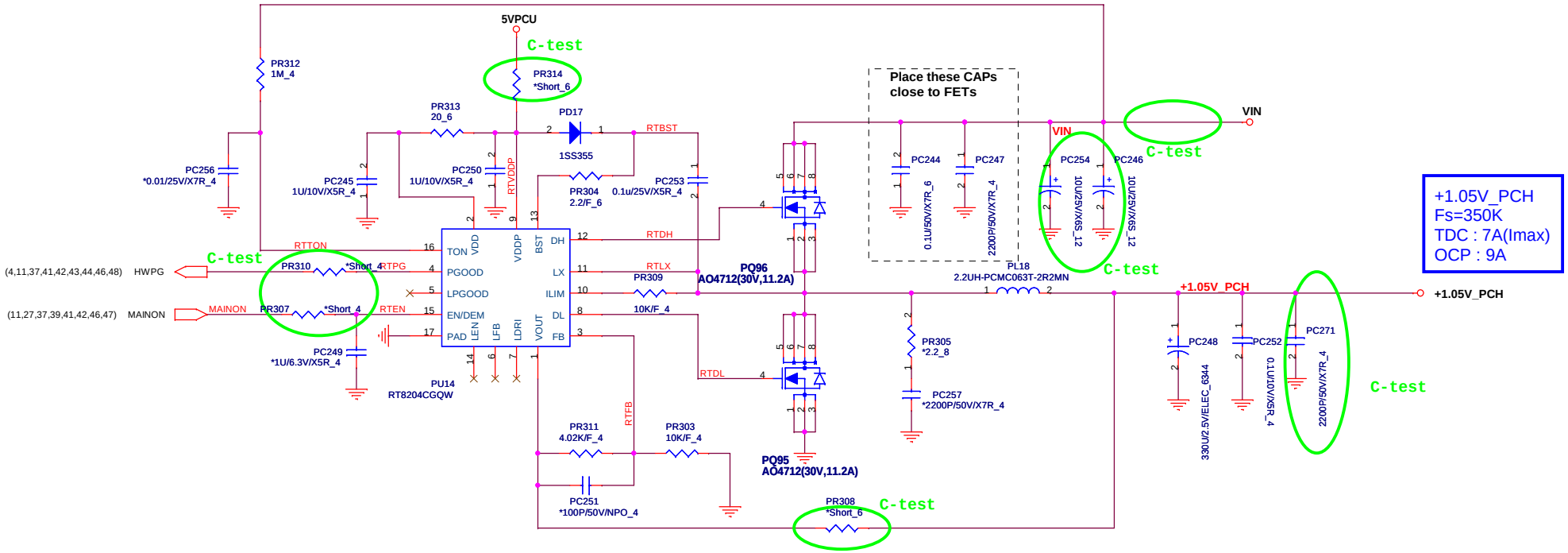


PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	GFX_VCC (MAX17028)	1A

Date: Wednesday, December 23, 2009 Sheet 48 of 53



PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.05V_PCH(RT8204)	1A

Date: Wednesday, December 23, 2009 Sheet 49 of 53

Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
1A		DV	Initial release		

Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP

CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

G NOTE SKU TABLE

Location					

G NOTE SKU TABLE

Location					Page

PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BOM Matrix Table	1A

Date: Wednesday, December 23, 2009 Sheet 51 of 53

PROJECT KL3 NOTE Calpella DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	POWER BLOCK	1A

Date: Wednesday, December 23, 2009 Sheet 52 of 53

EC #	Page	Description	Part Affected
EC-A-01	12	0 ohm change to DEL for reduce 1.05V drop	R261
EC-A-02	35	Change footprint and schematic for design request	CN5
EC-A-03	35	DEL R126 and connect CN5.25 to GND directly	R126
EC-A-04	38	Add 10 ohm for reduce noise	R577
EC-A-05	39	DEL CN2 for combine with GC4/GC5	CN2
EC-A-06	10	25MHz X'tal ICG support removed from POR	Y6,R478,C671,C670
EC-A-07	12	Based on Intel DG V1.5 page320, remove external LC filter for VCCACIk, VccapllEXP, VCCFDIPLL, VCCSATAPLL.	L45,C692,L46,C697,L47,C712, C715,L21,C329,C331
EC-A-08	14	Based on Intel DG V1.5 page100 ,remove DDR3 Vref control circuit M2 option.	U1 etc...
EC-A-09	15	Based on Intel DG V1.5 page100 ,remove DDR3 Vref control circuit M2 option.	U46 etc...
EC-A-10	23	Change from 0 ohm to bead for EMI request	R150
EC-A-11	26	Change from 0 ohm to bead for EMI request	R237,R238,R239,R240
EC-A-12	43	Del +1.05V_PCH discharge	PR219,PQ11
EC-A-13	43	Add charger PTC	PR263
EC-A-14	43	Change Footprint	PQ66
EC-A-15	43	Modify OTP circuit	PD34
EC-A-16	44	Del NO ASM circuit	PU16 etc...
EC-A-17	46	Del +1.05V_PCH circuit	PQ133 etc...
EC-A-18	46	Reduce +1.05V power rail impedance	PJP13,PJP4
EC-A-19	46	Reserve for current derating	PL23
EC-A-20	46	Reduce transient regulation	PL20
EC-A-21	47	Reduce ripple voltage	PC216
EC-A-22	49	Add to separate enable from protect circuit	PR264
EC-A-23	49	Reserve for sequence	PR265
EC-A-24	29	ESD suggestion because ESATA don't CDE test so we DEL U7,U8 and add a GND shielding in board file	U7,U8