KL9A Intel Huron River Platform with AMD Discrete GFX

DDRIII-SODIMM1
H 4.0 PG 14

DDRIII-SODIMM2
H 8.0 PG 15

Dual Channel DDR3
1067/1333 1.5V

DDR SYSTEM MEMORY

<MCH Process>
SandyBridge 0.61

rPGA 988

PCI-E

Graphics Interfaces

PG 4,5,6,7

FDI DMI

PCI-Express

27MHz

AMD
Robson ST-3
PG 16,17,18,19,20,21

HDMI CON PG 22

CRT PG 23

LCD CONN PG 24

FAN / THERMAL
EMC2103-2
PG 37

REGULATOR (DDR3)
1.5VSUS, 0.75VSMDDR_VTERM,1.5V
1.5V_GPU,1.5V_CPU PG 43

REGULATOR
+1.05V_VTT,+1.8V PG 45

DC/DC
3VPCU, 5VPCU, +15V PG 44

CPU Core PG 49

VGA Core Discrete PG 46

FDIX4 DMIX4

FDI DMI

SATA-SDD PG 30 — SATA0 150MB

SATA - HDD PG 28 — SATA1 150MB

SATA - CD-ROM PG 28 — SATA3 150MB

CougarPoint 0.7
PCH

PG 8,9,10,11,12,13

USB2.0

Port1,9 USB2.0 Ports X2 PG 32

Port 5 BlueTooth PG 38

Port 11 Finger Print PG 38

Port 2 Canera PG 36

Port3 Mini PCI-E WLAN PG 29

Port4 Mini PCI-E WWAN PG 29

PCI-E

Speaker PG 26

Audio Jack (External MIC) PG 26

Audio Jack (Headphone) PG 26

AUDIO CODEC
ALC269 PG 26

IHDA

32.768KHz

25MHz

LAN
Intel
(10/100/1G LAN)
WG82579LM
PAGE 25

25MHz

Card Reader
RTS5139-GR PG 27

5-IN-1 Card Reader CONN PG 27

USB 3.0
VIA VL801
PAGE 31

USB 2.0/3.0 CONN PAGE 31

Option

ME FW PG 9 — SPI

32.768KHz

LPC

EC
IT8518
PAGE 40

SPI Flash PG 40

K/B PG 35

T/P PG 35

Battery PG 44

Charger PG 42

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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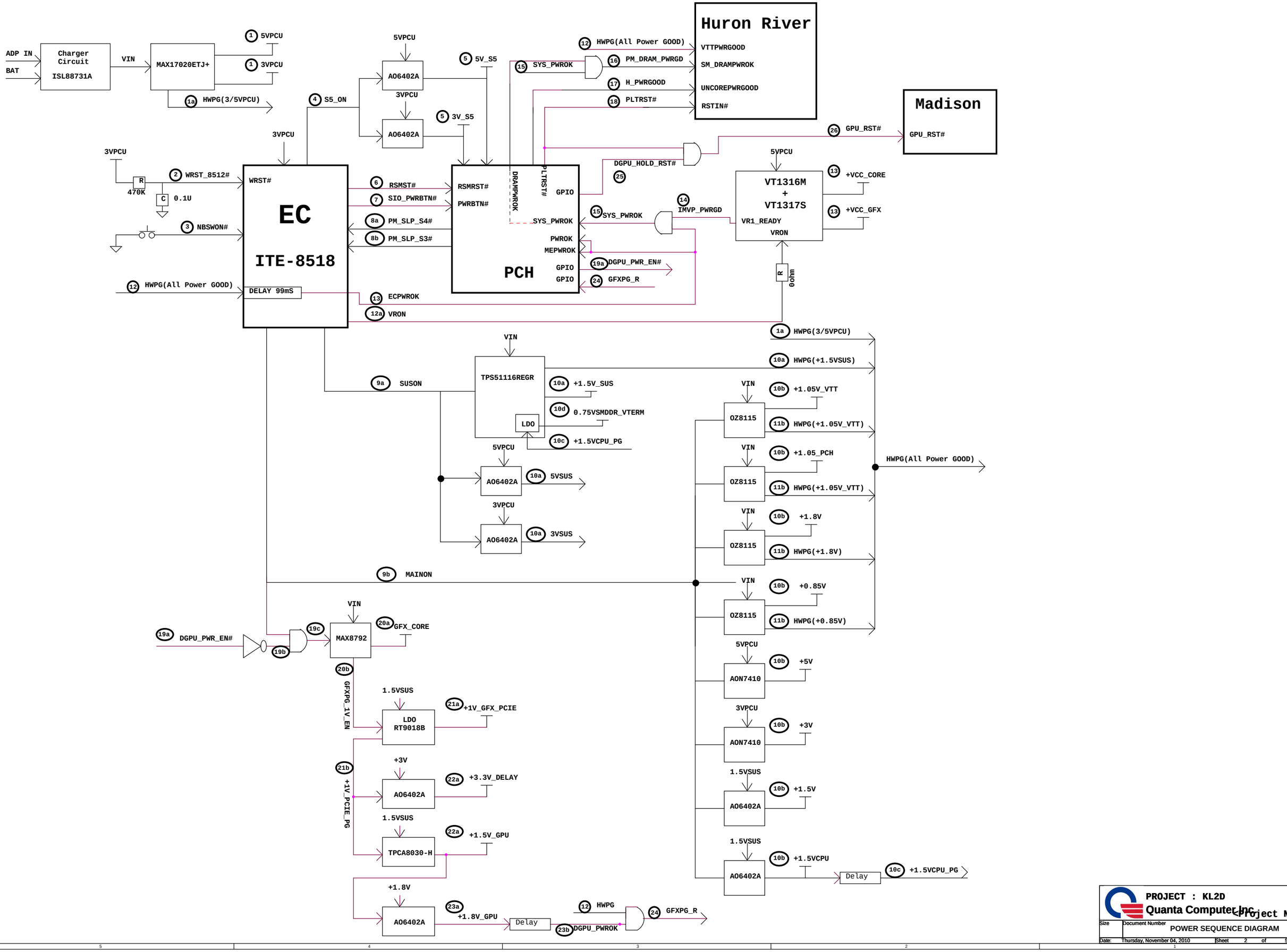

PROJECT : KL2D
Quanta Computer Inc.
<Project Name>

Size	Document Number	Rev
	POWER SEQUENCE DIAGRAM	1A
Date: Thursday, November 04, 2010	Sheet 2 of 53	

CLK Gen(CLK)

02/20 DEL for Pre-ES1

CPU_CLK select(CLK)

02/20 DEL for Pre-ES1

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
	Clock Generator	1A

Date: Thursday, November 04, 2010 Sheet 3 of 53

Sandy Bridge Processor (DMI,PEG,FDI)

U32A

DMI
(8) DMI_TXN0 B27 DMI_RX#[0]
(8) DMI_TXN1 B25 DMI_RX#[1]
(8) DMI_TXN2 A25 DMI_RX#[2]
(8) DMI_TXN3 B24 DMI_RX#[3]
(8) DMI_TXP0 B28 DMI_RX[0]
(8) DMI_TXP1 B26 DMI_RX[1]
(8) DMI_TXP2 A24 DMI_RX[2]
(8) DMI_TXP3 B23 DMI_RX[3]
(8) DMI_RXN0 G21 DMI_TX#[0]
(8) DMI_RXN1 E22 DMI_TX#[1]
(8) DMI_RXN2 F21 DMI_TX#[2]
(8) DMI_RXN3 D21 DMI_TX#[3]
(8) DMI_RXP0 G22 DMI_TX[0]
(8) DMI_RXP1 D22 DMI_TX[1]
(8) DMI_RXP2 F20 DMI_TX[2]
(8) DMI_RXP3 C21 DMI_TX[3]

Intel(R) FDI
(8) FDI_TXN0 A21 FDI0_TX#[0]
(8) FDI_TXN1 H19 FDI0_TX#[1]
(8) FDI_TXN2 E19 FDI0_TX#[2]
(8) FDI_TXN3 F18 FDI0_TX#[3]
(8) FDI_TXN4 B21 FDI1_TX#[0]
(8) FDI_TXN5 C20 FDI1_TX#[1]
(8) FDI_TXN6 D18 FDI1_TX#[2]
(8) FDI_TXN7 E17 FDI1_TX#[3]
(8) FDI_TXP0 A22 FDI0_TX[0]
(8) FDI_TXP1 G19 FDI0_TX[1]
(8) FDI_TXP2 E20 FDI0_TX[2]
(8) FDI_TXP3 G18 FDI0_TX[3]
(8) FDI_TXP4 B20 FDI1_TX[0]
(8) FDI_TXP5 C19 FDI1_TX[1]
(8) FDI_TXP6 D19 FDI1_TX[2]
(8) FDI_TXP7 F17 FDI1_TX[3]
(8) FDI_FSYNC0 J18 FDI0_FSYNC
(8) FDI_FSYNC1 J17 FDI1_FSYNC
(8) FDI_INT H20 FDI_INT
(8) FDI_LSYNC0 J19 FDI0_LSYNC
(8) FDI_LSYNC1 H17 FDI1_LSYNC

eDP
eDP_COMP A18 eDP_COMPIO
INT_eDP_HPD_Q A17 eDP_ICOMPO
B16 eDP_HPD
C15 eDP_AUX
D15 eDP_AUX#
C17 eDP_TX[0]
F16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
F15 eDP_TX#[3]

CPU-989P-rPGA

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

PCI EXPRESS* - GRAPHICS
PEG_ICOMPI J22 PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

PEG_RXN[0..15] (16)
PEG_RX#[0] K33 PEG_RXN0
PEG_RX#[1] M35 PEG_RXN1
PEG_RX#[2] L34 PEG_RXN2
PEG_RX#[3] J35 PEG_RXN3
PEG_RX#[4] J32 PEG_RXN4
PEG_RX#[5] H34 PEG_RXN5
PEG_RX#[6] H31 PEG_RXN6
PEG_RX#[7] G33 PEG_RXN7
PEG_RX#[8] G30 PEG_RXN8
PEG_RX#[9] E35 PEG_RXN9
PEG_RX#[10] E34 PEG_RXN10
PEG_RX#[11] E32 PEG_RXN11
PEG_RX#[12] D33 PEG_RXN12
PEG_RX#[13] D31 PEG_RXN13
PEG_RX#[14] B33 PEG_RXN14
PEG_RX#[15] C32 PEG_RXN15

PEG_RXP[0..15] (16)
PEG_RX[0] J33 PEG_RXP0
PEG_RX[1] L35 PEG_RXP1
PEG_RX[2] K34 PEG_RXP2
PEG_RX[3] H35 PEG_RXP3
PEG_RX[4] H32 PEG_RXP4
PEG_RX[5] G34 PEG_RXP5
PEG_RX[6] G31 PEG_RXP6
PEG_RX[7] F33 PEG_RXP7
PEG_RX[8] F30 PEG_RXP8
PEG_RX[9] E35 PEG_RXP9
PEG_RX[10] E33 PEG_RXP10
PEG_RX[11] F32 PEG_RXP11
PEG_RX[12] D34 PEG_RXP12
PEG_RX[13] E31 PEG_RXP13
PEG_RX[14] C33 PEG_RXP14
PEG_RX[15] B32 PEG_RXP15

PEG_TXN[0..15] (16)
PEG_TX#[0] M29 PEG_TXN0_C
PEG_TX#[1] M32 PEG_TXN1_C
PEG_TX#[2] M31 PEG_TXN2_C
PEG_TX#[3] L32 PEG_TXN3_C
PEG_TX#[4] L29 PEG_TXN4_C
PEG_TX#[5] K31 PEG_TXN5_C
PEG_TX#[6] K28 PEG_TXN6_C
PEG_TX#[7] J30 PEG_TXN7_C
PEG_TX#[8] J28 PEG_TXN8_C
PEG_TX#[9] H29 PEG_TXN9_C
PEG_TX#[10] G27 PEG_TXN10_C
PEG_TX#[11] E29 PEG_TXN11_C
PEG_TX#[12] F27 PEG_TXN12_C
PEG_TX#[13] D28 PEG_TXN13_C
PEG_TX#[14] F26 PEG_TXN14_C
PEG_TX#[15] E25 PEG_TXN15_C

PEG_TXP[0..15] (16)
PEG_TX[0] M28 PEG_TXP0_C
PEG_TX[1] M33 PEG_TXP1_C
PEG_TX[2] M30 PEG_TXP2_C
PEG_TX[3] L31 PEG_TXP3_C
PEG_TX[4] L28 PEG_TXP4_C
PEG_TX[5] K30 PEG_TXP5_C
PEG_TX[6] K27 PEG_TXP6_C
PEG_TX[7] J29 PEG_TXP7_C
PEG_TX[8] J27 PEG_TXP8_C
PEG_TX[9] H28 PEG_TXP9_C
PEG_TX[10] G28 PEG_TXP10_C
PEG_TX[11] E28 PEG_TXP11_C
PEG_TX[12] F28 PEG_TXP12_C
PEG_TX[13] D27 PEG_TXP13_C
PEG_TX[14] E26 PEG_TXP14_C
PEG_TX[15] D25 PEG_TXP15_C

CPU-989P-rPGA

Sandy Bridge Processor (CLK,MISC,JTAG)

04

U32B

MISC
SNB_IVB# N.A at SNB EDS #27637 0.7v1
(9) H_SNB_IVB# C26 PROC_SELECT#
TP11 SKTOCC# AN34 SKTOCC#

THERMAL
TP12 TP_CATERR# AL33 CATERR#
(40) EC_PECI AN33 PECI
(40,49) H_PROCHOT# R269 56/J_4 H_PROCHOT#_R AL32 PROCHOT#
(11) PM_THRMTRIP# AN32 THERMTRIP#

PWR MANAGEMENT
EC-C-15
(8) PM_SYNC R592 *SHORT_4 PM_SYNC_R AM34 PM_SYNC
(11) H_PWRGOOD R608 *SHORT_4 H_PWRGOOD_R AP33 UNCOREPWRGOOD
EC-QV-07
C900 *0.1U/10V_4
R607 10K/J_4
PM_DRAM_PWRGD_R V8 SM_DRAMPWROK
+1.05V_PCH R606 75/J_4
CPU_PLTRST# R605 43/J_4 CPU_PLTRST#_R AR33 RESET#
RV12 *EGA-0002

CPU-989P-rPGA

CLOCKS
BCLK A28 CLK_CPU_BCLKP_R R632 0/J_4 CLK_CPU_BCLKP (10)
BCLK# A27 CLK_CPU_BCLKN_R R633 0/J_4 CLK_CPU_BCLKN (10)
EC-B-31
DPLL_REF_CLK A16 CLK_DPLL_SSCLKP_R R293 Ra 0X2 CLK_DPLL_SSCLKP (10)
DPLL_REF_CLK# A15 CLK_DPLL_SSCLKN_R CLK_DPLL_SSCLKN (10)
R297 Rb 1K/F_4
R290 1K/F_4
Rc

	DIS	UMA
Ra	NA	0 ohm
Rb	1K ohm	NA
Rc	1K ohm	NA

DDR3 MISC
SM_DRAMRST# R8 CPU_DRAMRST# (5)
SM_RCOMP[0] AK1 SM_RCOMP_0 R626 140/F_4
SM_RCOMP[1] A5 SM_RCOMP_1 R315 25.5/F_4
SM_RCOMP[2] A4 SM_RCOMP_2 R316 200/F_4
EC-C-21
SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

JTAG & BPM
PRDY# AP29 XDP_PRDY# TP13
PREQ# AP27 XDP_PREQ# TP15
TCK AR26 XDP_TCLK TP6
TMS AR27 XDP_TMS TP7
TRST# AP30 XDP_TRST# TP10
TDI AR28 XDP_TDI_R TP8
TDO AP26 XDP_TDO TP50
DBR# AL35 XDP_DBRST# (8)
EC-B-34
BPM#[0] AT28
BPM#[1] AR29
BPM#[2] AR30
BPM#[3] AT30
BPM#[4] AP32
BPM#[5] AR31
BPM#[6] AT31
BPM#[7] AR32
EC-B-31
CLK_CPU_BCLKN C705 *22P/50V_4
CLK_CPU_BCLKP C704 *22P/50V_4
CLK_DPLL_SSCLKN_R C706 *22P/50V_4
CLK_DPLL_SSCLKP_R C713 *22P/50V_4
RF reserved

+3V_S5
U31 74LVC1G07GW
C636 0.1U/10V_4
(10,16,25,29,31) PLTRST# CPU_PLTRST#

EC-C-08
+3V_S5
C366 *0.1U/10V_4
U18 *74AHC1G09
(8,43) SYS_PWROK
(8) PM_DRAM_PWRGD R314 *0/J_4
R313 0/J_4
PM_DRAM_PWRGD_Q R312 *3K/F_4
PM_DRAM_PWRGD_Q R324 200/F_4
+1.5VCPU
R322 130/F_4 PM_DRAM_PWRGD_R
R325 39/J_4
Q29 2N7002K
EC-QV-08
MAINON# (41)

FDI Enable

FDI_INT
R282 DIS@0/J_4 FDI_FSYNC0
R284 DIS@0/J_4 FDI_FSYNC1
R277 DIS@0/J_4 FDI_LSYNC0
FDI_LSYNC1
R276 DIS@1K/F_4
R288 *DIS@1K/F_4

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 (UMA Non-stuff)

PEG_TXP0_C	C667	0.1U/10V_4	PEG_TXP0	PEG_TXN0_C	C668	0.1U/10V_4	PEG_TXN0
PEG_TXP1_C	C665	0.1U/10V_4	PEG_TXP1	PEG_TXN1_C	C666	0.1U/10V_4	PEG_TXN1
PEG_TXP2_C	C663	0.1U/10V_4	PEG_TXP2	PEG_TXN2_C	C664	0.1U/10V_4	PEG_TXN2
PEG_TXP3_C	C649	0.1U/10V_4	PEG_TXP3	PEG_TXN3_C	C650	0.1U/10V_4	PEG_TXN3
PEG_TXP4_C	C661	0.1U/10V_4	PEG_TXP4	PEG_TXN4_C	C662	0.1U/10V_4	PEG_TXN4
PEG_TXP5_C	C647	0.1U/10V_4	PEG_TXP5	PEG_TXN5_C	C648	0.1U/10V_4	PEG_TXN5
PEG_TXP6_C	C659	0.1U/10V_4	PEG_TXP6	PEG_TXN6_C	C660	0.1U/10V_4	PEG_TXN6
PEG_TXP7_C	C645	0.1U/10V_4	PEG_TXP7	PEG_TXN7_C	C646	0.1U/10V_4	PEG_TXN7
PEG_TXP8_C	C657	0.1U/10V_4	PEG_TXP8	PEG_TXN8_C	C658	0.1U/10V_4	PEG_TXN8
PEG_TXP9_C	C643	0.1U/10V_4	PEG_TXP9	PEG_TXN9_C	C644	0.1U/10V_4	PEG_TXN9
PEG_TXP10_C	C656	0.1U/10V_4	PEG_TXP10	PEG_TXN10_C	C655	0.1U/10V_4	PEG_TXN10
PEG_TXP11_C	C641	0.1U/10V_4	PEG_TXP11	PEG_TXN11_C	C642	0.1U/10V_4	PEG_TXN11
PEG_TXP12_C	C654	0.1U/10V_4	PEG_TXP12	PEG_TXN12_C	C653	0.1U/10V_4	PEG_TXN12
PEG_TXP13_C	C639	0.1U/10V_4	PEG_TXP13	PEG_TXN13_C	C640	0.1U/10V_4	PEG_TXN13
PEG_TXP14_C	C637	0.1U/10V_4	PEG_TXP14	PEG_TXN14_C	C638	0.1U/10V_4	PEG_TXN14
PEG_TXP15_C	C651	0.1U/10V_4	PEG_TXP15	PEG_TXN15_C	C652	0.1U/10V_4	PEG_TXN15

DP & PEG Compensation

+1.05V_PCH R613 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

+1.05V_PCH R615 10K_4 INT_eDP_HPD_Q
+1.05V_PCH R614 24.9/F_4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)

+1.05V_PCH
H_PROCHOT# R268 62/F_4
XDP_TDO R610 51/J_4
XDP_TMS R243 51/J_4
XDP_TDI_R R251 51/J_4
XDP_PREQ# R271 *51/J_4
XDP_TCLK R240 51/J_4
XDP_TRST# R260 51/J_4

PROJECT : KL2D
Quanta Computer Inc.

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Sandy Bridge Processor (DDR3)

05

U32C

(15) M_A_DQ[63:0]

M_A_DQ0	C5	SA_DQ[0]
M_A_DQ1	D5	SA_DQ[1]
M_A_DQ2	D3	SA_DQ[2]
M_A_DQ3	D2	SA_DQ[3]
M_A_DQ4	D6	SA_DQ[4]
M_A_DQ5	C6	SA_DQ[5]
M_A_DQ6	C2	SA_DQ[6]
M_A_DQ7	C3	SA_DQ[7]
M_A_DQ8	F10	SA_DQ[8]
M_A_DQ9	F8	SA_DQ[9]
M_A_DQ10	G10	SA_DQ[10]
M_A_DQ11	G9	SA_DQ[11]
M_A_DQ12	F9	SA_DQ[12]
M_A_DQ13	F7	SA_DQ[13]
M_A_DQ14	G8	SA_DQ[14]
M_A_DQ15	G7	SA_DQ[15]
M_A_DQ16	K4	SA_DQ[16]
M_A_DQ17	K5	SA_DQ[17]
M_A_DQ18	K1	SA_DQ[18]
M_A_DQ19	J1	SA_DQ[19]
M_A_DQ20	J5	SA_DQ[20]
M_A_DQ21	J4	SA_DQ[21]
M_A_DQ22	J2	SA_DQ[22]
M_A_DQ23	K2	SA_DQ[23]
M_A_DQ24	M8	SA_DQ[24]
M_A_DQ25	N10	SA_DQ[25]
M_A_DQ26	N8	SA_DQ[26]
M_A_DQ27	N7	SA_DQ[27]
M_A_DQ28	M10	SA_DQ[28]
M_A_DQ29	M9	SA_DQ[29]
M_A_DQ30	N9	SA_DQ[30]
M_A_DQ31	M7	SA_DQ[31]
M_A_DQ32	AG6	SA_DQ[32]
M_A_DQ33	AG5	SA_DQ[33]
M_A_DQ34	AK6	SA_DQ[34]
M_A_DQ35	AK5	SA_DQ[35]
M_A_DQ36	AH5	SA_DQ[36]
M_A_DQ37	AH6	SA_DQ[37]
M_A_DQ38	AJ5	SA_DQ[38]
M_A_DQ39	AJ6	SA_DQ[39]
M_A_DQ40	AJ8	SA_DQ[40]
M_A_DQ41	AK8	SA_DQ[41]
M_A_DQ42	AJ9	SA_DQ[42]
M_A_DQ43	AK9	SA_DQ[43]
M_A_DQ44	AH8	SA_DQ[44]
M_A_DQ45	AH9	SA_DQ[45]
M_A_DQ46	AL9	SA_DQ[46]
M_A_DQ47	AL8	SA_DQ[47]
M_A_DQ48	AP11	SA_DQ[48]
M_A_DQ49	AN11	SA_DQ[49]
M_A_DQ50	AL12	SA_DQ[50]
M_A_DQ51	AM12	SA_DQ[51]
M_A_DQ52	AM11	SA_DQ[52]
M_A_DQ53	AL11	SA_DQ[53]
M_A_DQ54	AP12	SA_DQ[54]
M_A_DQ55	AN12	SA_DQ[55]
M_A_DQ56	AJ14	SA_DQ[56]
M_A_DQ57	AH14	SA_DQ[57]
M_A_DQ58	AL15	SA_DQ[58]
M_A_DQ59	AK15	SA_DQ[59]
M_A_DQ60	AL14	SA_DQ[60]
M_A_DQ61	AK14	SA_DQ[61]
M_A_DQ62	AJ15	SA_DQ[62]
M_A_DQ63	AH15	SA_DQ[63]

DDR SYSTEM MEMORY A

SA_CLK[0]	AB6	M_A_CLKP0 (15)
SA_CLK#[0]	AA6	M_A_CLKN0 (15)
SA_CKE[0]	V9	M_A_CKE0 (15)
SA_CLK[1]	AA5	M_A_CLKP1 (15)
SA_CLK#[1]	AB5	M_A_CLKN1 (15)
SA_CKE[1]	V10	M_A_CKE1 (15)
RSVD_TP[1]	AB4	
RSVD_TP[2]	AA4	
RSVD_TP[3]	W9	
RSVD_TP[4]	AB3	
RSVD_TP[5]	AA3	
RSVD_TP[6]	W10	
SA_CS#[0]	AK3	M_A_CS#0 (15)
SA_CS#[1]	AL3	M_A_CS#1 (15)
RSVD_TP[7]	AG1	
RSVD_TP[8]	AH1	
SA_ODT[0]	AH3	M_A_ODT0 (15)
SA_ODT[1]	AG3	M_A_ODT1 (15)
RSVD_TP[9]	AG2	
RSVD_TP[10]	AH2	

SA_DQS#[0]	C4	M_A_DQSN0	M_A_DQSN[7:0] (15)
SA_DQS#[1]	G6	M_A_DQSN1	
SA_DQS#[2]	J3	M_A_DQSN2	
SA_DQS#[3]	M6	M_A_DQSN3	
SA_DQS#[4]	AL6	M_A_DQSN4	
SA_DQS#[5]	AM8	M_A_DQSN5	
SA_DQS#[6]	AR12	M_A_DQSN6	
SA_DQS#[7]	AM15	M_A_DQSN7	
SA_DQS[0]	D4	M_A_DQSP0	M_A_DQSP[7:0] (15)
SA_DQS[1]	F6	M_A_DQSP1	
SA_DQS[2]	K3	M_A_DQSP2	
SA_DQS[3]	N6	M_A_DQSP3	
SA_DQS[4]	AL5	M_A_DQSP4	
SA_DQS[5]	AM9	M_A_DQSP5	
SA_DQS[6]	AR11	M_A_DQSP6	
SA_DQS[7]	AM14	M_A_DQSP7	

SA_MA[0]	AD10	M_A_A0	M_A_A[15:0] (15)
SA_MA[1]	W1	M_A_A1	
SA_MA[2]	W2	M_A_A2	
SA_MA[3]	W7	M_A_A3	
SA_MA[4]	V3	M_A_A4	
SA_MA[5]	V2	M_A_A5	
SA_MA[6]	W3	M_A_A6	
SA_MA[7]	W6	M_A_A7	
SA_MA[8]	V1	M_A_A8	
SA_MA[9]	W5	M_A_A9	
SA_MA[10]	AD8	M_A_A10	
SA_MA[11]	V4	M_A_A11	
SA_MA[12]	W4	M_A_A12	
SA_MA[13]	AF8	M_A_A13	
SA_MA[14]	V5	M_A_A14	
SA_MA[15]	V7	M_A_A15	

(15) M_A_BS#0	AE10	SA_BS[0]
(15) M_A_BS#1	AE10	SA_BS[1]
(15) M_A_BS#2	V6	SA_BS[2]
(15) M_A_CAS#	AE8	SA_CAS#
(15) M_A_RAS#	AD9	SA_RAS#
(15) M_A_WE#	AF9	SA_WE#

CPU-989P-rPGA

U32D

(14) M_B_DQ[63:0]

M_B_DQ0	C9	SB_DQ[0]
M_B_DQ1	A7	SB_DQ[1]
M_B_DQ2	D10	SB_DQ[2]
M_B_DQ3	C8	SB_DQ[3]
M_B_DQ4	A9	SB_DQ[4]
M_B_DQ5	A8	SB_DQ[5]
M_B_DQ6	D9	SB_DQ[6]
M_B_DQ7	D8	SB_DQ[7]
M_B_DQ8	G4	SB_DQ[8]
M_B_DQ9	F4	SB_DQ[9]
M_B_DQ10	F1	SB_DQ[10]
M_B_DQ11	G1	SB_DQ[11]
M_B_DQ12	G5	SB_DQ[12]
M_B_DQ13	F5	SB_DQ[13]
M_B_DQ14	F2	SB_DQ[14]
M_B_DQ15	G2	SB_DQ[15]
M_B_DQ16	J7	SB_DQ[16]
M_B_DQ17	J8	SB_DQ[17]
M_B_DQ18	K10	SB_DQ[18]
M_B_DQ19	K9	SB_DQ[19]
M_B_DQ20	J9	SB_DQ[20]
M_B_DQ21	J10	SB_DQ[21]
M_B_DQ22	K8	SB_DQ[22]
M_B_DQ23	K7	SB_DQ[23]
M_B_DQ24	M5	SB_DQ[24]
M_B_DQ25	N4	SB_DQ[25]
M_B_DQ26	N2	SB_DQ[26]
M_B_DQ27	N1	SB_DQ[27]
M_B_DQ28	M4	SB_DQ[28]
M_B_DQ29	N5	SB_DQ[29]
M_B_DQ30	M2	SB_DQ[30]
M_B_DQ31	M1	SB_DQ[31]
M_B_DQ32	AM5	SB_DQ[32]
M_B_DQ33	AM6	SB_DQ[33]
M_B_DQ34	AR3	SB_DQ[34]
M_B_DQ35	AP3	SB_DQ[35]
M_B_DQ36	AN3	SB_DQ[36]
M_B_DQ37	AN2	SB_DQ[37]
M_B_DQ38	AN1	SB_DQ[38]
M_B_DQ39	AP2	SB_DQ[39]
M_B_DQ40	AP5	SB_DQ[40]
M_B_DQ41	AN9	SB_DQ[41]
M_B_DQ42	AT5	SB_DQ[42]
M_B_DQ43	AT6	SB_DQ[43]
M_B_DQ44	AP6	SB_DQ[44]
M_B_DQ45	AN8	SB_DQ[45]
M_B_DQ46	AR6	SB_DQ[46]
M_B_DQ47	AR5	SB_DQ[47]
M_B_DQ48	AR9	SB_DQ[48]
M_B_DQ49	AJ11	SB_DQ[49]
M_B_DQ50	AT8	SB_DQ[50]
M_B_DQ51	AT9	SB_DQ[51]
M_B_DQ52	AH11	SB_DQ[52]
M_B_DQ53	AR8	SB_DQ[53]
M_B_DQ54	AJ12	SB_DQ[54]
M_B_DQ55	AH12	SB_DQ[55]
M_B_DQ56	AT11	SB_DQ[56]
M_B_DQ57	AN14	SB_DQ[57]
M_B_DQ58	AR14	SB_DQ[58]
M_B_DQ59	AT14	SB_DQ[59]
M_B_DQ60	AT12	SB_DQ[60]
M_B_DQ61	AN15	SB_DQ[61]
M_B_DQ62	AR15	SB_DQ[62]
M_B_DQ63	AT15	SB_DQ[63]

DDR SYSTEM MEMORY B

SB_CLK[0]	AE2	M_B_CLKP0 (14)
SB_CLK#[0]	AD2	M_B_CLKN0 (14)
SB_CKE[0]	R9	M_B_CKE0 (14)
SB_CLK[1]	AE1	M_B_CLKP1 (14)
SB_CLK#[1]	AD1	M_B_CLKN1 (14)
SB_CKE[1]	R10	M_B_CKE1 (14)
RSVD_TP[11]	AB2	
RSVD_TP[12]	AA2	
RSVD_TP[13]	T9	
RSVD_TP[14]	AA1	
RSVD_TP[15]	AB1	
RSVD_TP[16]	T10	
SB_CS#[0]	AD3	M_B_CS#0 (14)
SB_CS#[1]	AE3	M_B_CS#1 (14)
RSVD_TP[17]	AD6	
RSVD_TP[18]	AE6	
SB_ODT[0]	AE4	M_B_ODT0 (14)
SB_ODT[1]	AD4	M_B_ODT1 (14)
RSVD_TP[19]	AD5	
RSVD_TP[20]	AE5	

SB_DQS#[0]	D7	M_B_DQSN0	M_B_DQSN[7:0] (14)
SB_DQS#[1]	F3	M_B_DQSN1	
SB_DQS#[2]	K6	M_B_DQSN2	
SB_DQS#[3]	N3	M_B_DQSN3	
SB_DQS#[4]	AN5	M_B_DQSN4	
SB_DQS#[5]	AP9	M_B_DQSN5	
SB_DQS#[6]	AK12	M_B_DQSN6	
SB_DQS#[7]	AP15	M_B_DQSN7	
SB_DQS[0]	C7	M_B_DQSP0	M_B_DQSP[7:0] (14)
SB_DQS[1]	G3	M_B_DQSP1	
SB_DQS[2]	J6	M_B_DQSP2	
SB_DQS[3]	M3	M_B_DQSP3	
SB_DQS[4]	AN6	M_B_DQSP4	
SB_DQS[5]	AP8	M_B_DQSP5	
SB_DQS[6]	AK11	M_B_DQSP6	
SB_DQS[7]	AP14	M_B_DQSP7	

SB_MA[0]	AA8	M_B_A0	M_B_A[15:0] (14)
SB_MA[1]	T7	M_B_A1	
SB_MA[2]	R7	M_B_A2	
SB_MA[3]	T6	M_B_A3	
SB_MA[4]	T2	M_B_A4	
SB_MA[5]	T4	M_B_A5	
SB_MA[6]	T3	M_B_A6	
SB_MA[7]	R2	M_B_A7	
SB_MA[8]	T5	M_B_A8	
SB_MA[9]	R3	M_B_A9	
SB_MA[10]	AB7	M_B_A10	
SB_MA[11]	R1	M_B_A11	
SB_MA[12]	T1	M_B_A12	
SB_MA[13]	AB10	M_B_A13	
SB_MA[14]	R5	M_B_A14	
SB_MA[15]	R4	M_B_A15	

(14) M_B_BS#0	AA9	SB_BS[0]
(14) M_B_BS#1	AA7	SB_BS[1]
(14) M_B_BS#2	R6	SB_BS[2]
(14) M_B_CAS#	AA10	SB_CAS#
(14) M_B_RAS#	AB8	SB_RAS#
(14) M_B_WE#	AB9	SB_WE#

CPU-989P-rPGA

+1.5V_SUS

R330 1K/F_4

R311 *0/J_4

R332 1K/F_4

(14,15) DDR3_DRAMRST#

CPU_DRAMRST# R

Q28 2N7002K

CPU_DRAMRST# (4)

(10) DRAMRST_CNTRL_PCH

R326 *SHORT_4

EC-C-15

C362 0.047U/10V_4

R320 4.99K/F_4

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Quanta Computer Inc.

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Sandy Bridge Processor (POWER)

CPU Core Power
SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)

+VCC_CORE

C309 22U/6.3V_8 C308 22U/6.3V_8 C307 22U/6.3V_8 C297 22U/6.3V_8
C306 22U/6.3V_8 C296 22U/6.3V_8 C316 22U/6.3V_8 C264 22U/6.3V_8
C295 22U/6.3V_8 C294 22U/6.3V_8 C293 22U/6.3V_8 C669 22U/6.3V_8
C317 22U/6.3V_8 C318 22U/6.3V_8 C284 22U/6.3V_8 C282 22U/6.3V_8
C305 22U/6.3V_8 C688 22U/6.3V_8 C689 22U/6.3V_8 C261 22U/6.3V_8
C298 22U/6.3V_8 C276 22U/6.3V_8 C299 22U/6.3V_8 C292 22U/6.3V_8
C676 22U/6.3V_8 C281 22U/6.3V_8 C277 22U/6.3V_8 C670 22U/6.3V_8
C275 22U/6.3V_8 C266 22U/6.3V_8 C263 22U/6.3V_8 C267 22U/6.3V_8

Reserved
C262 *22U/6.3V_8 C274 *22U/6.3V_8 C258 *22U/6.3V_8

U32F

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CPU-989P-rPGA

POWER

CORE SUPPLY

SVID

SENSE LINES

PEG AND DDR

CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)

+1.05V_PCH

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

C330 22U/6.3V_8 C336 10U/6.3V_6 C331 22U/6.3V_8 C329 22U/6.3V_8 C328 22U/6.3V_8 C327 22U/6.3V_8
C699 *22U/6.3V_8 C700 *22U/6.3V_8 C701 22U/6.3V_8 C335 10U/6.3V_6 C324 10U/6.3V_6 C332 22U/6.3V_8

22uF (Reserved)
C695 *22U/6.3V_8 C696 *22U/6.3V_8 C697 *22U/6.3V_8 C698 *22U/6.3V_8

+1.05V_VTT_40 R612 *0/short_4 +1.05V_PCH

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

VCC_SENSE AJ35 R590 100/J_4 +VCC_CORE
VSS_SENSE AJ34 R596 100/J_4
VCC_SENSE (49) VSS_SENSE (49)

VCCIO_SENSE B10
VSSIO_SENSE A10
VTT_SENSE (48) TP53

+VDDR_REF_CPU
(14,15,43) SMDDR_VREF R629 *0/J_8
Q44 2N7002K
(41,43) MAINON_15V R627 100K/J_4

Sandy Bridge Processor (GRAPHIC POWER)

CPU VGT
SNB 45W:22A
22uF x 12
22uF x 4 (Reserved)

EC-B-44

+VCC_GFX

C684 *22U/6.3V_8 C685 *22U/6.3V_8 C690 *22U/6.3V_8 C682 *22U/6.3V_8
C302 *22U/6.3V_8 C310 *22U/6.3V_8 C313 *22U/6.3V_8 C319 *22U/6.3V_8
C314 *22U/6.3V_8 C693 *22U/6.3V_8 C323 *22U/6.3V_8 C315 *22U/6.3V_8
C325 *22U/6.3V_8 C326 *22U/6.3V_8 C692 *22U/6.3V_8 C691 *22U/6.3V_8

R294 Ra 0/J_4

Ra	DIS	SW
	0 ohm	NA

U32G

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

CPU-989P-rPGA

POWER

GRAPHICS

1.8V RAIL

CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

+1.8V

C710 10U/6.3V_6 C708 1U/6.3V_4 C707 1U/6.3V_4 +C712 *330U/2V_7343

B6 VCCPLL1
A6 VCCPLL2
A2 VCCPLL3

SENSE LINES

VAXG_SENSE
VSSAXG_SENSE
AK35 AK34
TP48 TP45
R597 *100/J_4 +VCC_GFX
R591 *100/J_4
VCC_AXG_SENSE (49)
VSS_AXG_SENSE (49)

EC-B-44

VREF

SM_VREF AL1 +VDDR_REF_CPU +VDDR_REF_CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

DDR3 -1.5V RAILS

CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

+1.5VCPU
C353 10U/6.3V_6 C361 10U/6.3V_6 C352 10U/6.3V_6 C354 10U/6.3V_6
C351 10U/6.3V_6 C358 10U/6.3V_6 +C359 *330U/2V_7343 C368 22U/6.3V_8 C367 22U/6.3V_8

22uF (Reserved)

SA RAIL

CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

+0.85V
C303 10U/6.3V_6 C304 10U/6.3V_6 C680 10U/6.3V_6 C681 *10U/6.3V_6

MISC

VCCSA_SENSE H23 VCCUSA_SENSE (47)
FC_C22 C22 H_FC_C22 R273 10K/J_4
VCCSA_VID1 C24 VCCSA_SEL (47)
R598 10K/J_4

EC-B-35

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
+1.05V_PCH
Close to VR
R291 54.9/F_4
EC-C-15
H_CPU_SVIDCLK R292 *SHORT_4 VR_SVID_CLK (49)

SVID DATA
Place PU resistor close to CPU
+1.05V_PCH R283 130/F_4
EC-C-15
+1.05V_PCH Close to VR R286 130/F_4
EC-C-22
H_CPU_SVIDDAT R287 *SHORT_4 VR_SVID_DATA (49)

SVID ALERT
Place PU resistor close to CPU
+1.05V_PCH R275 75/J_4
EC-C-15
H_CPU_SVIDALRT# R279 43/J_4 R274 *SHORT_4 VR_SVID_ALERT# (49)

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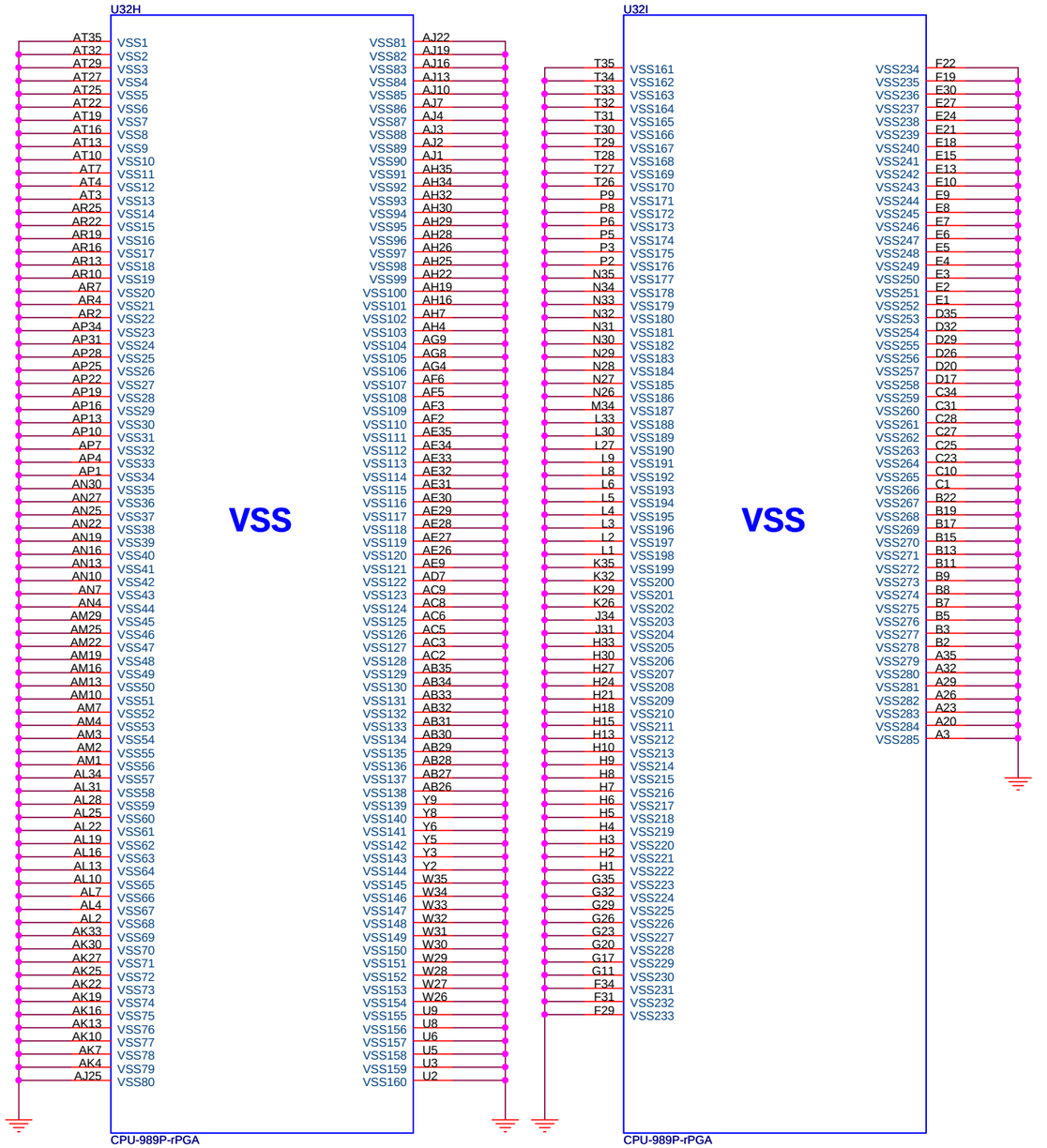
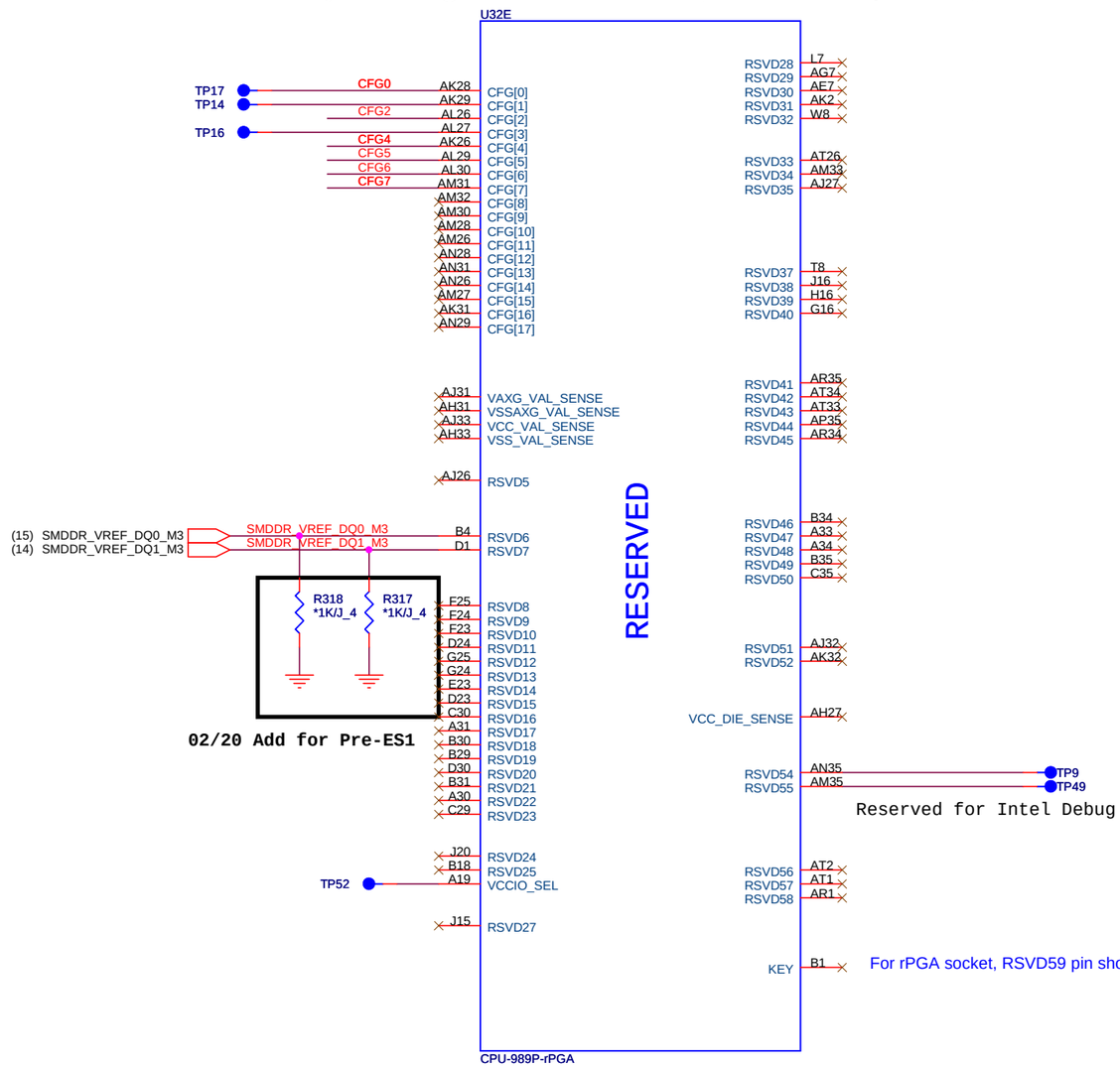
Sandy Bridge Processor (GND)



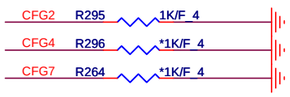
Sandy Bridge Processor (RESERVED, CFG)

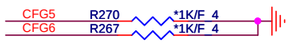


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training





CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Cougar Point (DMI,FDI,PM)

U14C

DMI0RXN / DMI1RXN / DMI2RXN / DMI3RXN
DMI0RXP / DMI1RXP / DMI2RXP / DMI3RXP
DMI0TXN / DMI1TXN / DMI2TXN / DMI3TXN
DMI0TXP / DMI1TXP / DMI2TXP / DMI3TXP
DMI_ZCOMP
DMI_IRCOMP
DMI2RBIAS

+1.05V_PCH R255 49.9/F_4 DMI_COMP
R604 750/F_4 DMI_RBIAS

FDI_RXN0 FDI_RXN1 FDI_RXN2 FDI_RXN3 FDI_RXN4 FDI_RXN5 FDI_RXN6 FDI_RXN7
FDI_RXP0 FDI_RXP1 FDI_RXP2 FDI_RXP3 FDI_RXP4 FDI_RXP5 FDI_RXP6 FDI_RXP7
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

EC-C-15

SUS_PWR_ACK_R R512 *0_4
XDP_DBRST# R527 *SHORT_4 SYS_PWROK_R
SYS_PWROK R511 *0/J_4
C901 *1U/10V_4
EC_PWROK R505 *SHORT_4 EC_PWROK_R
EC_PWROK_R R521 *SHORT_4 APWROK_R
PM_DRAM_PWRGD
RSMRST# R513 *SHORT_4 SUS_PWR_ACK_R
SUS_PWR_ACK
SIO_PWRBTN#
AC_PRESENT R502 *SHORT_4 PM_PRESENT_R
PM_BATLOW# R520 8.2K/J_4
PM_RI# R136 10K/J_4

EC-QV-09
EC-B-40
RV16 *EGA-0402

SUSACK# / SYS_RESET# / SYS_PWROK / PWROK / APWROK / DRAMPWROK / RSMRST# / SUSWARN#/SUSPWRDNACK/GPIO30 / PWRBTN# / ACPRESENT / GPIO31 / BATLOW# / GPIO72 / RI#

DSW

DSWVRMEN / DPWROK / WAKE# / CLKRUN# / GPIO32 / SUS_STAT# / GPIO61 / SUSCLK / GPIO62 / SLP_S5# / GPIO63 / SLP_S4# / SLP_S3# / SLP_A# / SLP_SUS# / PMSYNCH / SLP_LAN# / GPIO29

+3V_S5

EC-C-15
R91 *SHORT_4 RSMRST#
R504 *SHORT_4 DPWROK

PCIE_WAKE# (19,31)
CLKRUN# (40)
LPC_PD# T33
PCH_SUSCLK T29
SLP_S5# T27
PM_SLP_S4# (40)
SIO_SLP_S3# (40)
SLP_A# T28
SLP_SUS# T25
PM_SYNC (4)
SLP_LAN# T26
SLP_LAN# (25)

EC-B-36

CougarPoint_R1P0

R place close to PCH
R189 150/F_4 INT_CRT_BLU
R198 150/F_4 INT_CRT_GRE
R203 150/F_4 INT_CRT_RED

Cougar Point (LVDS,DDI)

U14D

EC-B-31
R662 0/J_4
R664 0/J_4
C564 *0.1U/10V_4
C563 *0.1U/10V_4
RF reserved close to PCH

L_BKLTEN L_VDD_EN L_BKLTCTL L_DDC_CLK L_DDC_DATA L_CTRL_CLK L_CTRL_DATA LVD_IBG LVD_VBG LVD_VREFH LVD_VREFL LVDSA_CLK# LVDSA_CLK LVDSA_DATA#0 LVDSA_DATA#1 LVDSA_DATA#2 LVDSA_DATA#3 LVDSA_DATA0 LVDSA_DATA1 LVDSA_DATA2 LVDSA_DATA3 LVDSB_CLK# LVDSB_CLK LVDSB_DATA#0 LVDSB_DATA#1 LVDSB_DATA#2 LVDSB_DATA#3 LVDSB_DATA0 LVDSB_DATA1 LVDSB_DATA2 LVDSB_DATA3

LVDS

(24) INT_LVDS_BLON
(24) INT_LVDS_VDDEN
(24) LVDS_BRIGHT_PWM
INT_EDIDCLK_R INT_EDIDDAT_R
+3V R556 2.2K/J_4 R562 2.2K/J_4
R573 2.37K/F_4 LVD_IBG
T30
INT_TXLCLKOUTN_R INT_TXLCLKOUTP_R
(24) INT_TXLOUTN0 (24) INT_TXLOUTN1 (24) INT_TXLOUTN2
(24) INT_TXLOUTP0 (24) INT_TXLOUTP1 (24) INT_TXLOUTP2

EC-B-31
(24) INT_EDIDCLK (24) INT_EDIDDAT
R678 0/J_4 INT_EDIDCLK_R
R699 0/J_4 INT_EDIDDAT_R
C717 *22P/50V_4
C718 *22P/50V_4
(24) INT_TXLCLKOUTN (24) INT_TXLCLKOUTP
R700 0/J_4 INT_TXLCLKOUTN_R
R701 0/J_4 INT_TXLCLKOUTP_R
C715 *22P/50V_4
C714 *22P/50V_4
RF reserved

CRT_BLUE CRT_GREEN CRT_RED CRT_DDC_CLK CRT_DDC_DATA CRT_HSYNC CRT_VSYNC DAC_IREF CRT_IRTN

CRT

(23) INT_CRT_BLU (23) INT_CRT_GRE (23) INT_CRT_RED
(23) INT_DDCCLK (23) INT_DDCDAT
(23) INT_CRT_HSYNC (23) INT_CRT_VSYNC
R536 33/J_4 INT_CRT_HSYNC_R
R541 33/J_4 INT_CRT_VSYNC_R

20ohm for SW;
33ohm for UMA

R551 1K/F_4

CougarPoint_R1P0

Digital Display Interface

SDVO_TVCLKINN SDVO_TVCLKINP SDVO_STALLN SDVO_STALLP SDVO_INTN SDVO_INTP SDVO_CTRLCLK SDVO_CTRLDATA DDPB_AUXN DDPB_AUXP DDPB_HPD DDPB_0N DDPB_0P DDPB_1N DDPB_1P DDPB_2N DDPB_2P DDPB_3N DDPB_3P DDPC_CTRLCLK DDPC_CTRLDATA DDPC_AUXN DDPC_AUXP DDPC_HPD DDPC_0N DDPC_0P DDPC_1N DDPC_1P DDPC_2N DDPC_2P DDPC_3N DDPC_3P DDPD_CTRLCLK DDPD_CTRLDATA DDPD_AUXN DDPD_AUXP DDPD_HPD DDPD_0N DDPD_0P DDPD_1N DDPD_1P DDPD_2N DDPD_2P DDPD_3N DDPD_3P

INT_HDMI_HPD_Q
DDPC_HPD_PU
DDPD_HPD_PU

EC-B-31 RF reserved close to PCH
R702 0/J_4
R703 0/J_4
C617 *0.1U/10V_4
C608 *0.1U/10V_4
INT_HDMI_SCL (22)
INT_HDMI_SDA (22)

INT_HDMI_TXDN2 (22)
INT_HDMI_TXDP2 (22)
INT_HDMI_TXDN1 (22)
INT_HDMI_TXDP1 (22)
INT_HDMI_TXDN0 (22)
INT_HDMI_TXDP0 (22)
INT_HDMI_TXCN (22)
INT_HDMI_TXCP (22)

INT. HDMI

+5V
INT_HDMI_HPD_Q
Q21 2N7002K
R599 *100K/J_4
R244 100K/J_4
INT_HDMI_HPD (22)

Deep sleep option	Support	Not support
SUS_PWR_ACK	To PCH SUSACK# (Pop R597)	EC or NC (Non-pop R597)
DPWROK	DSWPWRGD (Pop Q54, R663, Q55, R677)	RSMRST (Pop R639)
SLP_SUS	EC	NC

PCH Pull-high/low(CLG)

+3V
CLKRUN# R194 8.2K/J_4
XDP_DBRST# R192 10K/J_4
R195 *1K/J_4
RSMRST# R111 10K/J_4
SYS_PWROK R519 10K/J_4

+3V_S5
PM_RI# R136 10K/J_4
PM_BATLOW# R520 8.2K/J_4
PCIE_WAKE# R143 10K/J_4
SLP_LAN# R495 *10K/J_4
SUS_PWR_ACK R508 10K/J_4
AC_PRESENT R489 10K/J_4

EC-QV-10
PM_DRAM_PWRGD R493 *200/F_4

3/16 Change topology; 200ohm PU to +3V_S5

System PWR_OK(CLG)

+3V_S5
C113 *0.1U/10V_4
U9 TC7SH08
(4,43) SYS_PWROK
IMVP_PWRGD (49)
EC_PWROK
R478 100K/J_4

+3V_RTC

R93 330K/J_4
DSWVREN
R104 *330K/J_4

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

DPWROK FOR DSW

+3VPCU
+3V_DSW
+3V_S5
D6 *RB500V-40
D5 *RB500V-40
R80 *10K_4
R106 *10K_4
DPWROK
C106 *0.1U/10V_4
add cap to timing tune
Q11 *PDTC144EU
Q12 *2N7002

+3V

DDPC_HPD_PU R589 10K/J_4
DDPD_HPD_PU R253 10K/J_4
INT_EDIDCLK R199 2.2K/J_4
INT_EDIDDAT R191 2.2K/J_4
Follow PDG eDP disable guide

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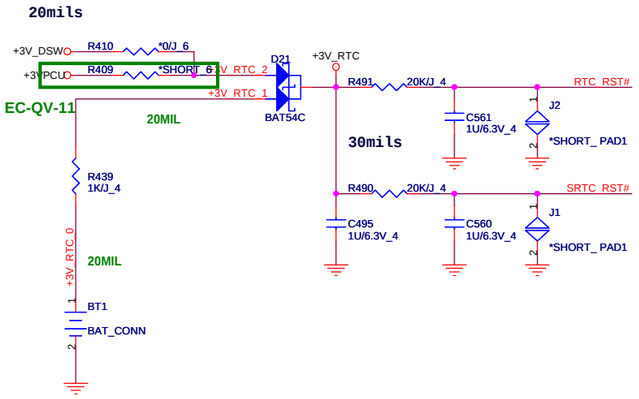
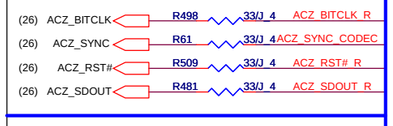
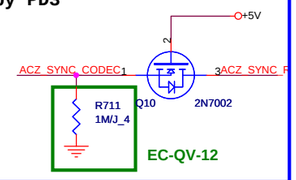
RTC Circuitry(RTC)



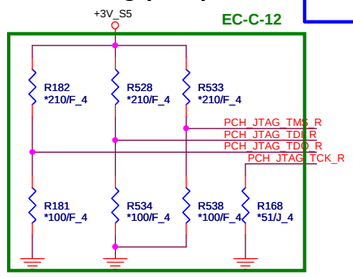
HDA Bus(CLG)



To Separate Codec Sync by PD3

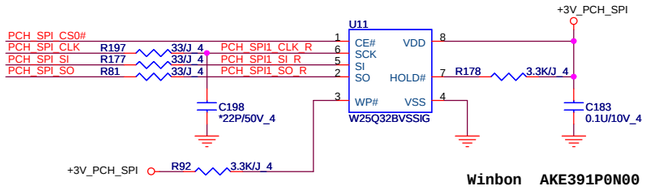


PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

32Mbit (4M Byte), SPI

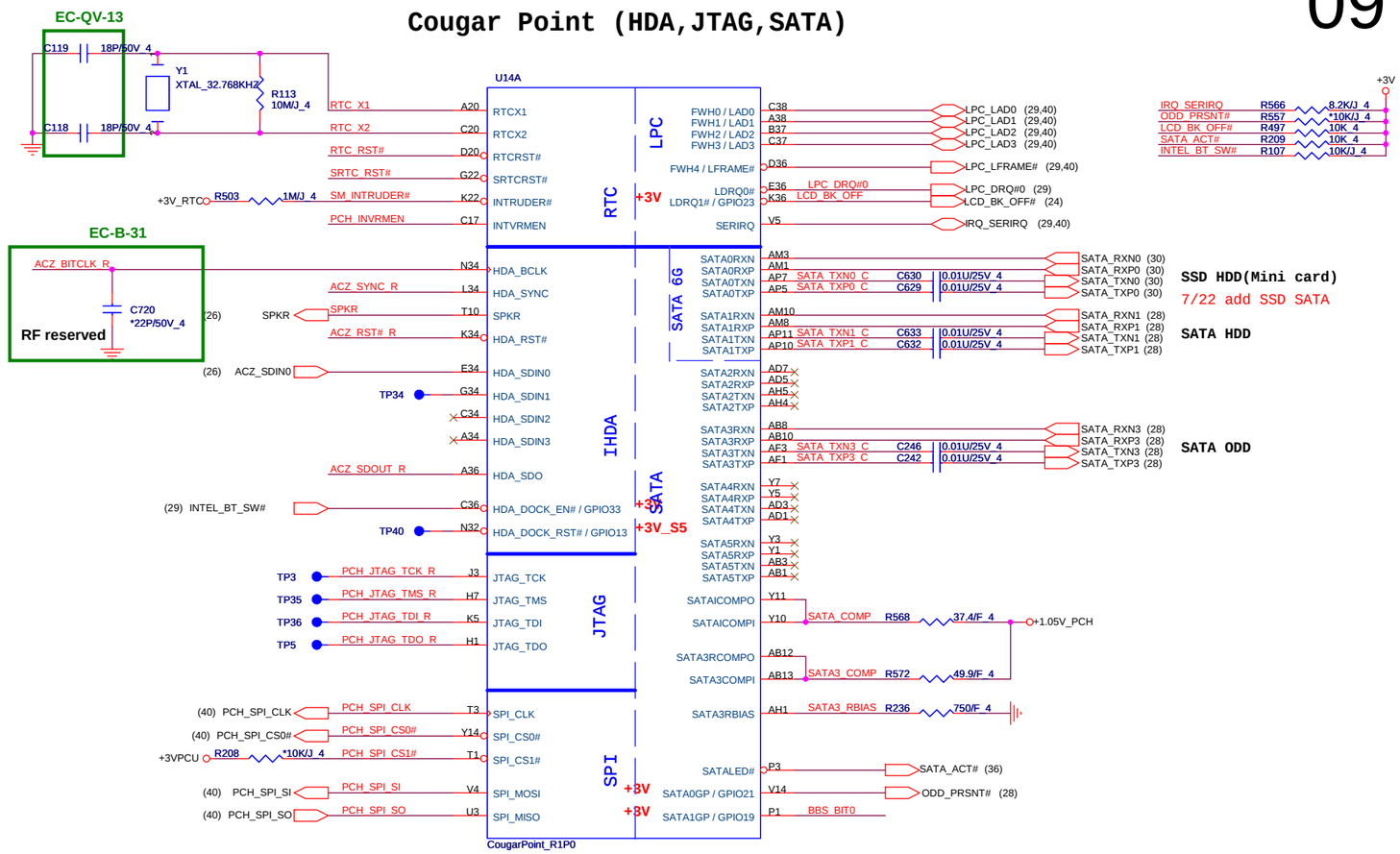


Winbon AKE391P0N00

PCH2(CLG)

Cougar Point (HDA,JTAG,SATA)

09



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R567 *1K/J_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R518 *1K/J_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R105 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / **SPI** * ; 0 / 0 / LPC	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]**
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R514 *1K/J_4 BBS_BIT1 (10) R201 *1K/J_4 BBS_BIT0
HDA_SDO	Flash Descriptor Security	**RSMRST**	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 R479 *1K/J_4 ACZ_SDOUT_R
DF_TVS	**DMI/FDI Termination voltage**	**PWROK**	**0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**	R249 2.2K/J_4 +1.8V R246 4.7K/J_4 DF_TVS (11) H_SNB_IVB# (41)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R547 *1K/J_4 PLL_ODVR_EN (11,40)
HDA_SYNC	**On-Die PLL VR Voltage Select**	**RSMRST**	**0 = Support by 1.8V (weak pull-down)** **1 = Support by 1.5V**	+3V_S5 R75 1K/J_4 ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R188 *1K/J_4 PCH_SPI_SI
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

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Cougar Point-M (PCI,USB,NVRAM)

U14E

RSVD

TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24 TP25 TP26 TP27 TP28 TP29 TP30 TP31 TP32 TP33 TP34 TP35 TP36 TP37 TP38 TP39 TP40

RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14 RSVD15 RSVD16 RSVD17 RSVD18 RSVD19 RSVD20 RSVD21 RSVD22 RSVD23 RSVD24 RSVD25 RSVD26 RSVD27 RSVD28 RSVD29

NV_ALE → TP47

PCI

PIRQA# PIRQB# PIRQC# PIRQD#

PCI_PIRQA# PCI_PIRQB# PCI_PIRQC# PCI_PIRQD#

REQ1# / GPIO50 +3V
REQ2# / GPIO52 +3V
REQ3# / GPIO54 +3V

(11) BOARD_ID3 — BOARD_ID3
(36) RF_ON
(11) BOARD_ID4 — BOARD_ID4

GNT1# / GPIO51 +3V
GNT2# / GPIO53 +3V
GNT3# / GPIO55 +3V

(9) BBS_BIT1 — BBS_BIT1
(38) BT_DIS — BT_DIS
(9) PCI_GNT3# — PCI_GNT3#

PIRQE# / GPIO2 +3V
PIRQF# / GPIO3 +3V
PIRQG# / GPIO4 +3V
PIRQH# / GPIO5 +3V

(28,40) ODD_MDDA# — EXTTS_SNI_DRV0_PCH — EXTTS_SNI_DRV1_PCH

MPC_PWR_CTRL# → TP39

PME#

PCI_PLTRST# → PLTRST#

TP49 TP50 CLK_LPC_TPM_C

CLK_PCI_FB — R510 22/J_4 — CLK_PCI_FB_R — J48

(29) CLK_LPC_DEBUG — R508 22/J_4 — CLK_PCI_LPC_R — K42
(40) CLK_PCI_8512 — R510 22/J_4 — CLK_PCI_EC_R — H40

CLKOUT_PCI0 H49
CLKOUT_PCI1 H43
CLKOUT_PCI2 J48
CLKOUT_PCI3 K42
CLKOUT_PCI4 H40

EC-B-27

EC11 10P/50V/C0G_4
EC12 10P/50V/C0G_4

EC-B-31

CLK_PCI_FB — C811 *22P/50V_4 — RF reserved

CougarPoint_R1P0

USB

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P

USBP0- (33) USBP0+ (33) USBP1- (32) USBP1+ (32) USBP2- (36) USBP2+ (36) USBP3- (29) USBP3+ (29) USBP4- (29) USBP4+ (29) USBP5- (38) USBP5+ (38)

USB#0/eSATA Combo #1(Phoenix debug)
USB#1-> (External L side/BIOS debug)
CCD
WLAN
WWAN
BlueTooth

EHCI1

USBP8- (31) USBP8+ (31) USBP9- (32) USBP9+ (32) USBP10- (27) USBP10+ (27) USBP11- (38) USBP11+ (38) USBP12- (30) USBP12+ (30) USBP13- (29) USBP13+ (29)

USB #2 Reserved)
USB#4 (External R side&BIOS debug)
Card Reader
Figer Print
WiMax
USIM

EHCI2

USBRBIAS# C33 — USB_BIAS — R86 22.6/F_4
USBRBIAS B33

OC0# / GPIO59 OC1# / GPIO40 OC2# / GPIO41 OC3# / GPIO42 OC4# / GPIO43 OC5# / GPIO9 OC6# / GPIO10 OC7# / GPIO14

+3V_S5 on all

USB_OC0# A14 — USB_OC0# (33)
USB_OC1# K20 — USB_OC1# (32)
USB_OC2# B17 — USB_OC2# (31)
USB_OC3# C16
USB_OC4# L16
USB_OC5# A16
USB_OC6# D14
USB_OC7# C14

USB_OC4# (32)
USB30_EXT_SMI# (31)

USB_OC0# -->USB Port#0 ESATA OC pin
USB_OC1# -->USB Port#1 OC pin
USB_OC2# -->Reserved
USB_OC4# -->USB Port #3 OC pin

EC-C-13

Cougar Point-M (PCI-E,SMBUS,CLK)

U14B

PCI-E*

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

LAN

(25) PCIE_RXN2_LAN — C634 0.1U/10V_4 — PCIE_TXN2_LAN_C
(25) PCIE_RXP2_LAN — C635 0.1U/10V_4 — PCIE_TXP2_LAN_C
(25) PCIE_TXN2_LAN
(25) PCIE_TXP2_LAN

WLAN

(29) PCIE_RXN3 — C673 0.1U/10V_4 — PCIE_TXN3_C
(29) PCIE_RXP3 — C672 0.1U/10V_4 — PCIE_TXP3_C
(29) PCIE_TXN3
(29) PCIE_TXP3

WWAN only use USB interface.

USB3.0

(31) PCIE_RXN5 — C674 0.1U/16V_4 — PCIE_TXN5_C
(31) PCIE_RXP5 — C675 0.1U/16V_4 — PCIE_TXP5_C
(31) PCIE_TXN5
(31) PCIE_TXP5

SMBUS

+3V_S5

SMBALERT# / GPIO11 E12 — SMBALERT# — SMB_PCH_CLK
SMBCLK H14
SMBDATA C9 — SMB_PCH_DAT

+3V_S5

SML0ALERT# / GPIO60 A12 — DRAMRST_CNTRL_PCH — DRAMRST_CNTRL_PCH (5)
SML0CLK C8 — SMB_CLK_ME0 — SMB_CLK_ME0 (30)
SML0DATA G12 — SMB_DATA_ME0 — SMB_DATA_ME0 (30)

For LAN

EC-B-31

SMB_PCH_CLK — C727 *22P/50V_4
SMB_CLK_ME0 — C809 *22P/50V_4
SMB_ME1_CLK — C810 *22P/50V_4
RF reserved

+3V_S5

SML1ALERT# / PCHHOT# / GPIO74 C13 — SML1ALERT#_R
SML1CLK / GPIO58 E14 — SMB_ME1_CLK
SML1DATA / GPIO75 M16 — SMB_ME1_DAT

For EC

Controller Link

CL_CLK1 M7 — CL_CLK1 — TP38
CL_DATA1 T11 — CL_DATA1 — TP42
CL_RST1# P10 — CL_RST# — TP41

+3V_S5

PEG_A_CLKRQ# / GPIO47 M10 — PEG_CLKREQ#

CLOCKS

CLKOUT_PCIE0N Y40
CLKOUT_PCIE0P Y39

EC-B-30 — PCIECLKRQ0# — J2 — PCIECLKRQ0# / GPIO73 +3V_S5

LAN

CLKOUT_PCIE1N AB49
CLKOUT_PCIE1P AB47

PCIECLKRQ0# — M1 — PCIECLKRQ1# / GPIO18 +3V

WLAN

CLKOUT_PCIE2N AA48
CLKOUT_PCIE2P AA47

PCIECLKRQ1# — V10 — PCIECLKRQ2# / GPIO20 +3V

WWAN only use USB interface.

CLKOUT_PCIE3N Y37
CLKOUT_PCIE3P Y36

PCIECLKRQ3# / GPIO25 +3V_S5

USB3.0

CLKOUT_PCIE4N Y43
CLKOUT_PCIE4P Y45

PCIECLKRQ4# — L12 — PCIECLKRQ4# / GPIO26 +3V_S5

EC-B-30 — PCIECLKRQ5# — L14 — PCIECLKRQ5# / GPIO44 +3V_S5

CLKOUT_PEG_B_N AB42
CLKOUT_PEG_B_P AB40

EC-B-30 — PCIECLKRQ6# — E6 — PEG_B_CLKRQ# / GPIO56 +3V_S5

CLKOUT_PCIE6N Y40
CLKOUT_PCIE6P Y42

EC-B-30 — PCIECLKRQ6# — T13 — PCIECLKRQ6# / GPIO45 +3V_S5

CLKOUT_PCIE7N V38
CLKOUT_PCIE7P V37

EC-B-02 EC-B-30 — PCIECLKRQ7# — K12 — PCIECLKRQ7# / GPIO46 +3V_S5

TP44 TP43 CLK_PCH_ITPN_R CLK_PCH_ITPP_R — AK14 AK13 — CLKOUT_ITPXDP_N CLKOUT_ITPXDP_P

CougarPoint_R1P0

FWH/LPC/SPI

+3V CLKOUTFLEX0 / GPIO64 K43 — TP27 — Reserve to cost down crystal.
+3V CLKOUTFLEX1 / GPIO65 F47 — CLK_27M_VGA_1 — R523 *0.4 — CLK_27M_VGA (17)
+3V CLKOUTFLEX2 / GPIO66 H47 — CLK_25M — TP84
+3V CLKOUTFLEX3 / GPIO67 K49 — CLK_48M_CARD_C — R180 22.4 — CLK_48M_CARD (27)

27Mz support DIS only

EC-B-33
EC-C-13

XCLK_RCOMP Y47 — XCLK_RCOMP — R211 90.9/F_4 — +1.05V_PCH

CLKIN_PCILOOPBACK H45 — CLK_PCI_FB — C247 18P/50V_4

XTAL25_IN V47 — XTAL25_IN — R224 1M/J_4 — Y2 25MHz — C221 18P/50V_4
XTAL25_OUT V49 — XTAL25_OUT

REFCLK14IN K45 — CLK_PCH_14M

CLKIN_DOT_96N G24 — CLK_BUF_DREFCLKN
CLKIN_DOT_96P E24 — CLK_BUF_DREFCLKP

CLKIN_SATA_N AK7 — CLK_BUF_DREFSSCLKN
CLKIN_SATA_P AK5 — CLK_BUF_DREFSSCLKP

CLKIN_DMI_N BF18 — CLK_BUF_PCIE_3GPLLN
CLKIN_DMI_P BE18 — CLK_BUF_PCIE_3GPLLP

CLKIN_GND1_N BJ30 — CLK_BUF_BCLKN
CLKIN_GND1_P BG30 — CLK_BUF_BCLKP

CLKOUT_DMI_N AV22 — CLK_CPU_BCLKN (4)
CLKOUT_DMI_P AU22 — CLK_CPU_BCLKP (4)

CLKOUT_DP_N AM12 — CLK_DPLL_SSCLKN (4)
CLKOUT_DP_P AM13 — CLK_DPLL_SSCLKP (4)

CLKOUT_PEG_A_N AB37 — CLKOUT_PEG_A_N
CLKOUT_PEG_A_P AB38 — CLKOUT_PEG_A_P

SMBus(CLK)

+3V — R281 4.7K/J_4 — SMB_PCH_DAT — Q23 2N7002K — SMB_RUN_DAT — SMB_RUN_DAT (14,15)

+3V — R280 4.7K/J_4 — SMB_PCH_CLK — Q22 2N7002K — SMB_RUN_CLK — SMB_RUN_CLK (14,15)

PLTRST#(CLG)

+3V_S5 — C114 0.1U/10V_4 — U10 TC7SH08FU — PCI_PLTRST# — PLTRST# — R67 100K/J_4

R68 *0.4 — PLTRST# — PLTRST# (4,16,25,29,31)

(11) DGPU_PWR_EN#

PCI/USBOC# Pull-up(CLG)

+3V_S5 — R116 10KX8

USB_OC4# USB_OC1# USB_OC2# USB_OC3# — USB_OC6# USB_OC0# USB_OC7# USB_OC5#

+3V — R99 10KX8

MPC_PWR_CTRL# BT_DIS DGPU_PWR_EN# ODD_MDDA# — EXTTS_SNI_DRV0_PCH EXTTS_SNI_DRV1_PCH

+3V

PCI_PIRQA# — R535 8.2K/J_4
PCI_PIRQB# — R540 8.2K/J_4
PCI_PIRQC# — R485 8.2K/J_4
PCI_PIRQD# — R486 8.2K/J_4

EC-C-18

CLK_REQ/Strap Pin(CLG)

+3V_S5

EC-B-30

R531 10K/J_4 PCIECLKRQ0#
R379 10K/J_4 PCIECLKRQ5#
R620 10K/J_4 PCIECLKRQ6#
R621 10K/J_4 PCIECLKRQ7#
R622 10K/J_4 PCIECLKRQ3#
R149 10K/J_4 PCIE_CLKREQ_USB30#

UMA:Ra
DIS:Rb

R529 Ra *10K/J_4 PEG_CLKREQ#
PEG_CLKREQ# R539 10K/J_4 Rb

CLK_BUF_BCLKN R256 10K/J_4
CLK_BUF_BCLKP R257 10K/J_4

CLK_BUF_PCIE_3GPLLN R601 10K/J_4
CLK_BUF_PCIE_3GPLLP R602 10K/J_4
CLK_BUF_DREFCLKN R516 10K/J_4
CLK_BUF_DREFCLKP R517 10K/J_4
CLK_BUF_DREFSSCLKN R585 10K/J_4
CLK_BUF_DREFSSCLKP R580 10K/J_4
CLK_PCH_14M R543 10K/J_4

CLOCK TERMINATION for FCIM

+3V — R544 10K/J_4 PCIE_CLKREQ_WLAN# — R173 10K/J_4 PCIE_CLKREQ_LAN#

SMBus/Pull-up(CLG)

+3V_S5

(17,37,40) MB_CLK1 — Q8 2N7002K — R69 2.2K/J_4 — SMB_ME1_CLK

(17,37,40) MB_DATA1 — Q9 2N7002K — R64 2.2K/J_4 — SMB_ME1_DAT

+3V_S5

R494 1K/J_4 DRAMRST_CNTRL_PCH
R492 10K/J_4 SMBALERT#
R285 2.2K/J_4 SMB_PCH_CLK
R266 2.2K/J_4 SMB_PCH_DAT
R496 10K/J_4 SML1ALERT#_R

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# — R145 *1K/J_4

R234 SW@0X2

LAN
(25) CLK_PCIE_LANP — CLKOUT_PCIE0P
(25) CLK_PCIE_LANN — CLKOUT_PCIE0N
(25) PCIE_CLKREQ_LAN# — R174 0.4 — PCIECLKRQ0#

R231 SW@0X2

WLAN
(29) CLK_PCIE_WLANN — CLKOUT_PCIE1N
(29) CLK_PCIE_WLANP — CLKOUT_PCIE1P
(29) PCIE_CLKREQ_WLAN# — R190 0.4 — PCIECLKRQ1#

R570 SW@0X2

USB3.0
(31) CLK_PCIE_USB30N — CLKOUT_PCIE3N
(31) CLK_PCIE_USB30P — CLKOUT_PCIE3P
PCIE_CLKREQ_USB30# — R150 0.4 — PCIECLKRQ3#

R569 SW@0X2

(16) CLK_PCIE_VGAN — CLKOUT_PEG_A_N
(16) CLK_PCIE_VGAP — CLKOUT_PEG_A_P

DIS:Stuff
UMA:Non-stuff

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Cougar Point (GPIO,VSS_NCTF,RSVD)

11

U14F

S_GPIO R553 100_4 T7 BMBUSY# / GPIO0 +3V
(40) EC_EXT_SMI# EC_EXT_SMI# A42 TACH1 / GPIO1 +3V
BOARD_ID0 EC-B-03 H36 TACH2 / GPIO6 +3V
(40) EC_EXT_SCI# EC_EXT_SCI# E38 TACH3 / GPIO7 +3V
SYSTEM_ID C10 GPIO8 +3V_S5
(25) LAN_DISABLE# LAN_DISABLE# C4 LAN_PHY_PWR_CTRL / GPIO12 +3V_S5
HOST_ALERT#1_R G2 GPIO15 +3V_S5
EC-B-04 (29) WLAN_OFF# U2 SATA4GP / GPIO16 +3V
DGPU_PWROK DGPU_PWROK D40 TACH0 / GPIO17 +3V
+3V Follow DMRB4, need check BIOS_REC T5 SCLOCK / GPIO22 +3V
R542 *10K (30) SDD_DA_DSS SDD_DA_DSS E8 GPIO24 / MEM_LED +3V_S5
GPIO27 E16 GPIO27 DSW
(9,40) PLL_ODVR_EN R546 *0/J_4 PLL_ODVR_EN_R P8 GPIO28 +3V_S5
STP_PCI# K1 STP_PCI# / GPIO34 +3V
(38) BT_ON# BT_ON# K4 GPIO35 +3V
(10) DGPU_PWR_EN# V8 SATA2GP / GPIO36 +3V
Need check EC-B-04 (29) WWAN_OFF# M5 SATA3GP / GPIO37 +3V
EC-C-19 MFG_MODE N2 SLOAD / GPIO38 +3V
FDI_OVRVLTG M3 SDATAOUT0 / GPIO39 +3V
TEST_SET_UP V13 SDATAOUT1 / GPIO48 +3V
(37,40) TEMP_ALERT# V3 SATA5GP / GPIO49 +3V
SV_DET D6 GPIO57 +3V_S5

GPIO

TACH4 / GPIO68 C40 BOARD_ID1 EC-B-03
TACH5 / GPIO69 B41 T24
TACH6 / GPIO70 C41 SSD_DETECT# (30)
TACH7 / GPIO71 A40 BOARD_ID2

CPU/MISC

A20GATE P4 EC_A20GATE (40)
PECI AU16 TP46
RCIN# P5 EC_RCIN# EC_RCIN# (40)
PROCPWRGD AY11 H_PWRGOOD (4)
THRMTRIP# AY10 PCH_THRMTRIP# R595 390/J_4 PM_THRMTRIP# (4)
INIT3_3V# T14
DF_TVS AY1 DF_TVS (9)

TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37

3/16 Connected to GND
DG rev0.9

NCTF

VSS_NCTF_1 A4
VSS_NCTF_2 A44
VSS_NCTF_3 A45
VSS_NCTF_4 A46
VSS_NCTF_5 A5
VSS_NCTF_6 A6
VSS_NCTF_7 B3
VSS_NCTF_8 B47
VSS_NCTF_9 BD1
VSS_NCTF_10 BD49
VSS_NCTF_11 BE1
VSS_NCTF_12 BE49
VSS_NCTF_13 BF1
VSS_NCTF_14 BF49

VSS_NCTF_15 BG2
VSS_NCTF_16 BG48
VSS_NCTF_17 BH3
VSS_NCTF_18 BH47
VSS_NCTF_19 BJ4
VSS_NCTF_20 BJ44
VSS_NCTF_21 BJ45
VSS_NCTF_22 BJ46
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ6
VSS_NCTF_25 C2
VSS_NCTF_26 C48
VSS_NCTF_27 D1
VSS_NCTF_28 D49
VSS_NCTF_29 E1
VSS_NCTF_30 E49
VSS_NCTF_31 F1
VSS_NCTF_32 F49

CougarPoint_R1P0

GPIO Pull-up/Pull-down(CLG)

+3V_S5
LAN_DISABLE# R157 10K/J_4

+3V
EC_EXT_SMI# R89 10K/J_4
EC_EXT_SCI# R487 10K/J_4
SSD_DETECT# R110 10K/J_4
STP_PCI# R193 10K/J_4
EC_A20GATE R550 10K/J_4
EC_RCIN# R549 10K/J_4
TEMP_ALERT# R217 10K/J_4
BT_ON# R537 10K/J_4
DGPU_PWROK R500 10K/J_4
EC-B-04 WLAN_OFF# R530 10K/J_4

GPIO27 R515 10K/J_4

	GPIO71	GPIO68	GPIO6
	BOARD_ID2	BOARD_ID1	BOARD_ID0
KL7	0	0	0
KL8	0	1	0
KL9	1	0	0
KL8A	0	1	1
KL9A	1	0	1

EC-B-05

+3V
R108 *10K/J_4 BOARD_ID0 R87 10K/J_4
R488 10K/J_4 BOARD_ID1 R480 *10K/J_4
R109 *10K/J_4 BOARD_ID2 R88 10K/J_4
R507 10K/J_4 BOARD_ID3 R501 *10K/J_4
R483 10K/J_4 BOARD_ID4 R484 *10K/J_4
R142 10K/J_4 SYSTEM_ID R144 *10K/J_4

(10) BOARD_ID3 BOARD_ID3
(10) BOARD_ID4 BOARD_ID4

SV_SET_UP
High = Strong (Default)

+3V
TEST_SET_UP R559 10K/J_4
R565 *0/J_4

+3V_S5 EC-QV-03
R526 *10K/J_4 SV_DET R524 100K/J_4

+3V_S5
HOST_ALERT#1_R R525 1K/J_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

SGPIO

+3V
S_GPIO R560 10K/J_4
R561 *0/J_4

+3V
R548 100K/J_4 FDI_OVRVLTG R545 *1K/F_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

+3V
SDD_DA_DSS R681 *200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

+3V
BIOS_REC R564 10K/J_4
R558 *0/J_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST

+3V
MFG_MODE R202 10K/J_4
R200 *0/J_4

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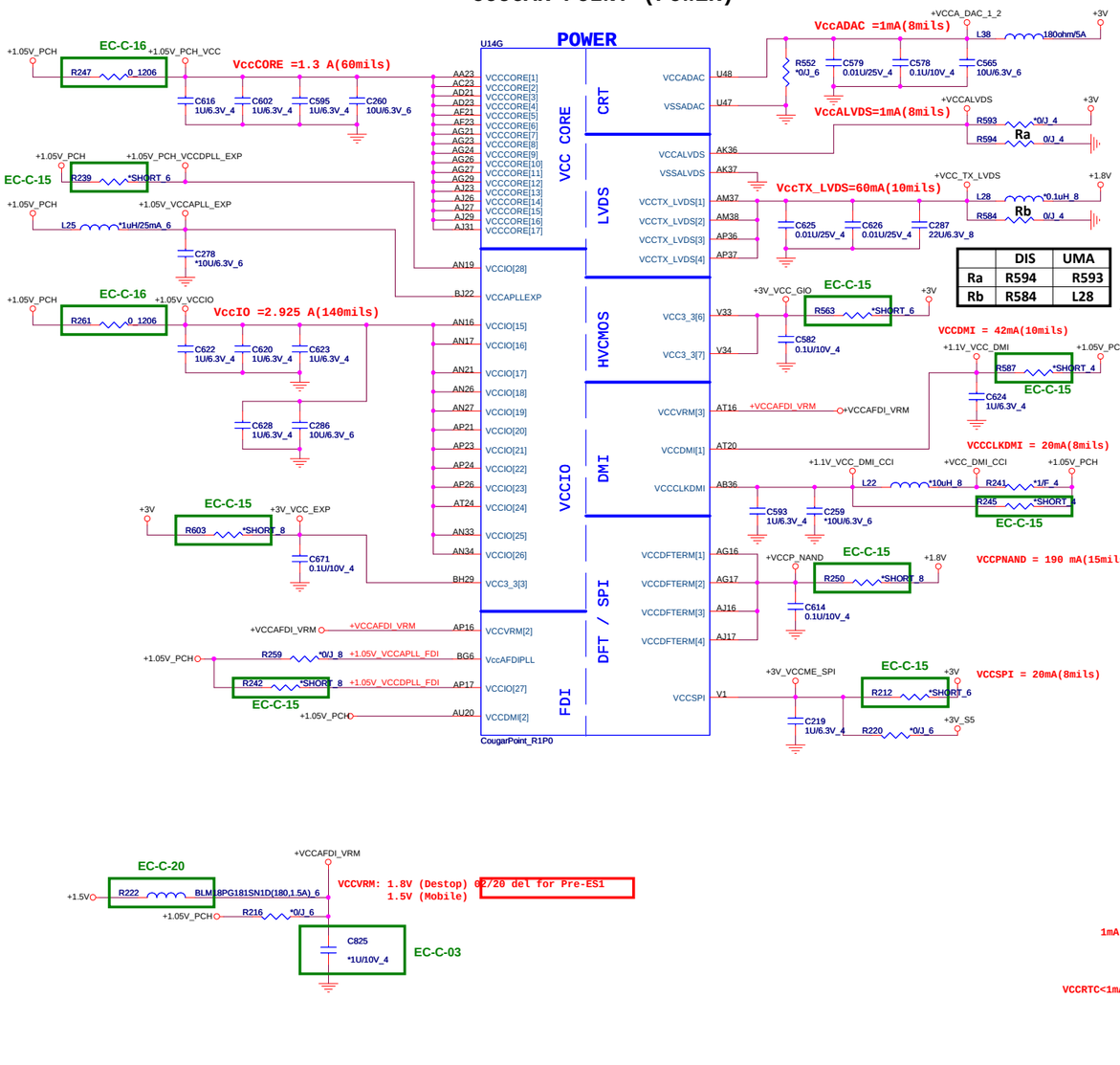
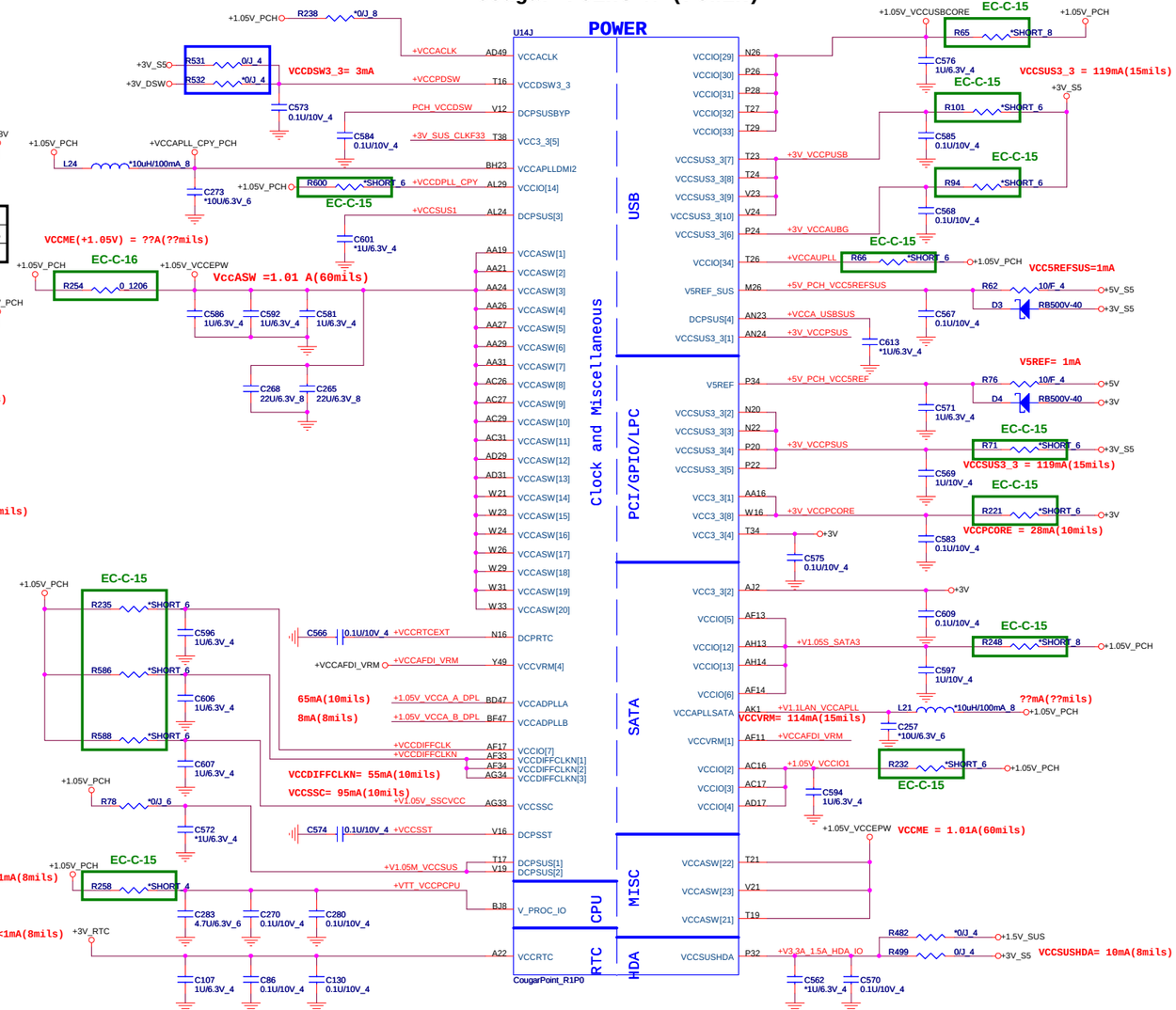
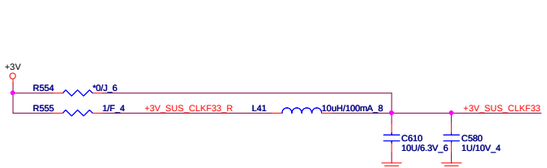
COUGAR POINT (POWER)

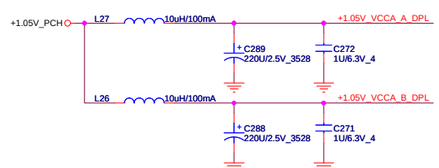


	DIS	UMA
Ra	R594	R593
Rb	R584	L28

Cougar Point-M (POWER)







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IBEX PEAK-M (GND)

U14H

H5	VSS[0]		
AA17	VSS[1]	VSS[80]	AK38
AA2	VSS[2]	VSS[81]	AK4
AA3	VSS[3]	VSS[82]	AK42
AA33	VSS[4]	VSS[83]	AK46
AA34	VSS[5]	VSS[84]	AK8
AB11	VSS[6]	VSS[85]	AL16
AB14	VSS[7]	VSS[86]	AL17
AB39	VSS[8]	VSS[87]	AL19
AB4	VSS[9]	VSS[88]	AL2
AB43	VSS[10]	VSS[89]	AL21
AB5	VSS[11]	VSS[90]	AL23
AB7	VSS[12]	VSS[91]	AL26
AC19	VSS[13]	VSS[92]	AL27
AC2	VSS[14]	VSS[93]	AL31
AC21	VSS[15]	VSS[94]	AL33
AC24	VSS[16]	VSS[95]	AL34
AC33	VSS[17]	VSS[96]	AL48
AC34	VSS[18]	VSS[97]	AM11
AC48	VSS[19]	VSS[98]	AM14
AD10	VSS[20]	VSS[99]	AM36
AD11	VSS[21]	VSS[100]	AM39
AD12	VSS[22]	VSS[101]	AM43
AD13	VSS[23]	VSS[102]	AM45
AD19	VSS[24]	VSS[103]	AM46
AD24	VSS[25]	VSS[104]	AM7
AD26	VSS[26]	VSS[105]	AN2
AD27	VSS[27]	VSS[106]	AN29
AD33	VSS[28]	VSS[107]	AN3
AD34	VSS[29]	VSS[108]	AN31
AD36	VSS[30]	VSS[109]	AP12
AD37	VSS[31]	VSS[110]	AP19
AD38	VSS[32]	VSS[111]	AP28
AD39	VSS[33]	VSS[112]	AP30
AD4	VSS[34]	VSS[113]	AP32
AD40	VSS[35]	VSS[114]	AP38
AD42	VSS[36]	VSS[115]	AP4
AD43	VSS[37]	VSS[116]	AP42
AD45	VSS[38]	VSS[117]	AP46
AD46	VSS[39]	VSS[118]	AP8
AD8	VSS[40]	VSS[119]	AR2
AE2	VSS[41]	VSS[120]	AR48
AE3	VSS[42]	VSS[121]	AT11
AF10	VSS[43]	VSS[122]	AT13
AF12	VSS[44]	VSS[123]	AT18
AD14	VSS[45]	VSS[124]	AT22
AD16	VSS[46]	VSS[125]	AT26
AF16	VSS[47]	VSS[126]	AT28
AF19	VSS[48]	VSS[127]	AT30
AF24	VSS[49]	VSS[128]	AT32
AF26	VSS[50]	VSS[129]	AT34
AF27	VSS[51]	VSS[130]	AT39
AF29	VSS[52]	VSS[131]	AT42
AF31	VSS[53]	VSS[132]	AT46
AF38	VSS[54]	VSS[133]	AT7
AF4	VSS[55]	VSS[134]	AU24
AF42	VSS[56]	VSS[135]	AU30
AF46	VSS[57]	VSS[136]	AV16
AF5	VSS[58]	VSS[137]	AV20
AF7	VSS[59]	VSS[138]	AV24
AF8	VSS[60]	VSS[139]	AV30
AG19	VSS[61]	VSS[140]	AV38
AG2	VSS[62]	VSS[141]	AV4
AG31	VSS[63]	VSS[142]	AV43
AG48	VSS[64]	VSS[143]	AV8
AH11	VSS[65]	VSS[144]	AW14
AH3	VSS[66]	VSS[145]	AW18
AH36	VSS[67]	VSS[146]	AW2
AH39	VSS[68]	VSS[147]	AW22
AH40	VSS[69]	VSS[148]	AW26
AH42	VSS[70]	VSS[149]	AW28
AH46	VSS[71]	VSS[150]	AW32
AH7	VSS[72]	VSS[151]	AW34
AJ19	VSS[73]	VSS[152]	AW36
AJ21	VSS[74]	VSS[153]	AW40
AJ24	VSS[75]	VSS[154]	AW48
AJ33	VSS[76]	VSS[155]	AV11
AJ34	VSS[77]	VSS[156]	AY12
AK12	VSS[78]	VSS[157]	AY22
AK3	VSS[79]	VSS[158]	AY28

CougarPoint_R1P0

U14I

AY4	VSS[159]	VSS[259]	H46
AY42	VSS[160]	VSS[260]	K18
AY46	VSS[161]	VSS[261]	K26
AY8	VSS[162]	VSS[262]	K39
B11	VSS[163]	VSS[263]	K46
B15	VSS[164]	VSS[264]	K7
B19	VSS[165]	VSS[265]	L18
B23	VSS[166]	VSS[266]	L2
B27	VSS[167]	VSS[267]	L20
B31	VSS[168]	VSS[268]	L26
B35	VSS[169]	VSS[269]	L28
B39	VSS[170]	VSS[270]	L36
B7	VSS[171]	VSS[271]	L48
F45	VSS[172]	VSS[272]	M12
BB12	VSS[173]	VSS[273]	P16
BB16	VSS[174]	VSS[274]	M18
BB20	VSS[175]	VSS[275]	M22
BB22	VSS[176]	VSS[276]	M24
BB24	VSS[177]	VSS[277]	M30
BB28	VSS[178]	VSS[278]	M32
BB30	VSS[179]	VSS[279]	M34
BB38	VSS[180]	VSS[280]	M38
BB4	VSS[181]	VSS[281]	M4
BB46	VSS[182]	VSS[282]	M42
BC14	VSS[183]	VSS[283]	M46
BC18	VSS[184]	VSS[284]	M8
BC2	VSS[185]	VSS[285]	N18
BC22	VSS[186]	VSS[286]	P30
BC26	VSS[187]	VSS[287]	N47
BC32	VSS[188]	VSS[288]	P11
BC34	VSS[189]	VSS[289]	P18
BC36	VSS[190]	VSS[290]	T33
BC40	VSS[191]	VSS[291]	P40
BC42	VSS[192]	VSS[292]	P43
BC48	VSS[193]	VSS[293]	P47
BD46	VSS[194]	VSS[294]	P7
BD5	VSS[195]	VSS[295]	R2
BE22	VSS[196]	VSS[296]	R48
BE26	VSS[197]	VSS[297]	T12
BE40	VSS[198]	VSS[298]	T31
BF10	VSS[199]	VSS[299]	T37
BF12	VSS[200]	VSS[300]	T4
BF16	VSS[201]	VSS[301]	W34
BF20	VSS[202]	VSS[302]	T46
BF22	VSS[203]	VSS[303]	T47
BF24	VSS[204]	VSS[304]	T8
BF26	VSS[205]	VSS[305]	V11
BF28	VSS[206]	VSS[306]	V17
BD3	VSS[207]	VSS[307]	V26
BF30	VSS[208]	VSS[308]	V27
BF38	VSS[209]	VSS[309]	V29
BF40	VSS[210]	VSS[310]	V31
BF8	VSS[211]	VSS[311]	V36
BG17	VSS[212]	VSS[312]	V39
BG21	VSS[213]	VSS[313]	V43
BG33	VSS[214]	VSS[314]	V7
BG44	VSS[215]	VSS[315]	W17
BG8	VSS[216]	VSS[316]	W19
BH11	VSS[217]	VSS[317]	W2
BH15	VSS[218]	VSS[318]	W27
BH17	VSS[219]	VSS[319]	W48
BH19	VSS[220]	VSS[320]	Y12
H10	VSS[221]	VSS[321]	Y38
BH27	VSS[222]	VSS[322]	Y4
BH31	VSS[223]	VSS[323]	Y42
BH33	VSS[224]	VSS[324]	Y46
BH35	VSS[225]	VSS[325]	Y8
BH39	VSS[226]	VSS[328]	BG29
BH43	VSS[227]	VSS[329]	N24
BH7	VSS[228]	VSS[330]	AJ3
D3	VSS[229]	VSS[331]	AD47
D12	VSS[230]	VSS[333]	B43
D16	VSS[231]	VSS[334]	BE10
D18	VSS[232]	VSS[335]	BG41
D22	VSS[233]	VSS[337]	G14
D24	VSS[234]	VSS[338]	H16
D26	VSS[235]	VSS[340]	T36
D30	VSS[236]	VSS[342]	BG22
D32	VSS[237]	VSS[343]	BG24
D34	VSS[238]	VSS[344]	C22
D38	VSS[239]	VSS[345]	AP13
D42	VSS[240]	VSS[346]	M14
D8	VSS[241]	VSS[347]	AP3
E18	VSS[242]	VSS[348]	AP1
E26	VSS[243]	VSS[349]	BE16
G18	VSS[244]	VSS[350]	BC16
G20	VSS[245]	VSS[351]	BG28
G26	VSS[246]	VSS[352]	BJ28
G28	VSS[247]		
G36	VSS[248]		
G48	VSS[249]		
H12	VSS[250]		
H18	VSS[251]		
H22	VSS[252]		
H24	VSS[253]		
H26	VSS[254]		
H30	VSS[255]		
H32	VSS[256]		
H34	VSS[257]		
F3	VSS[258]		

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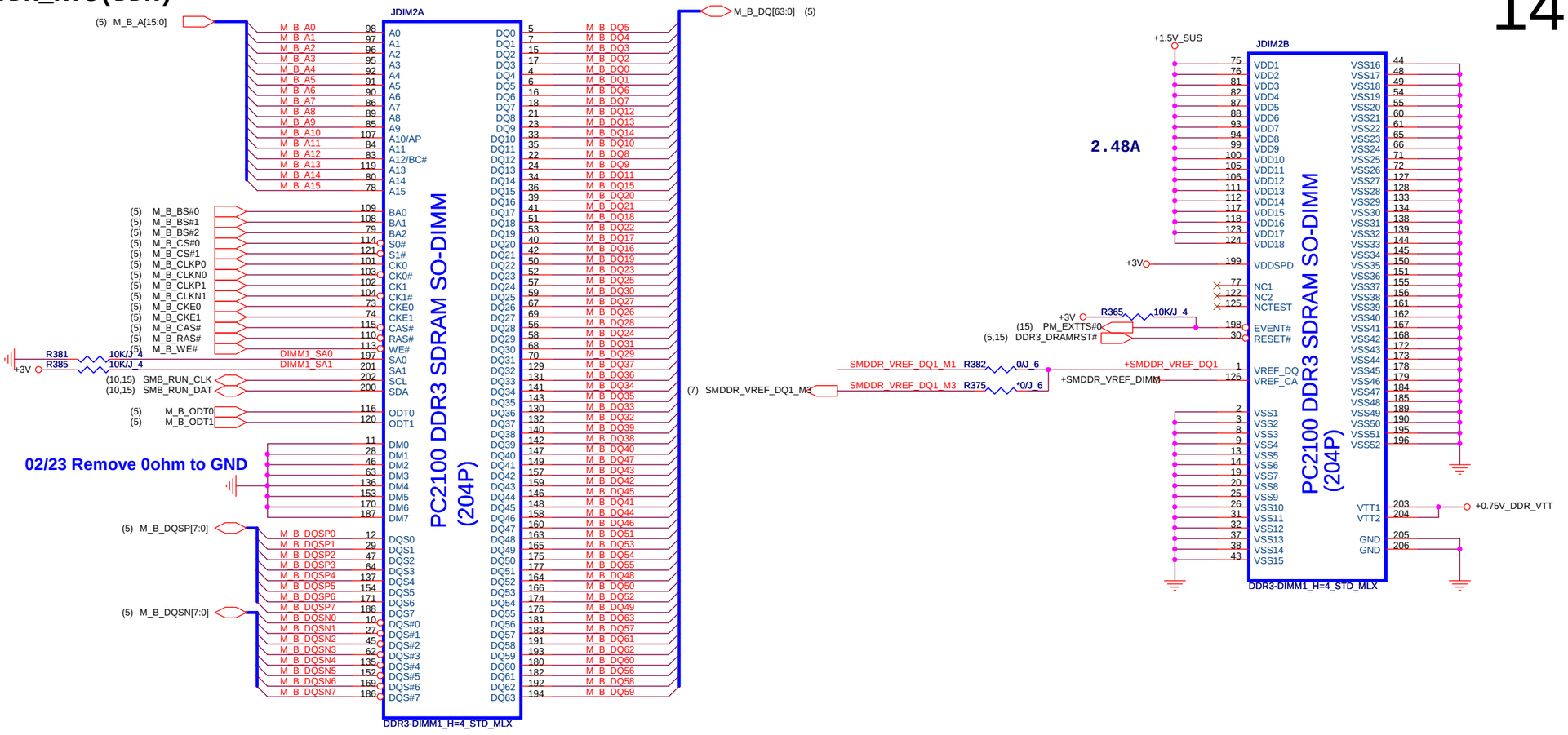
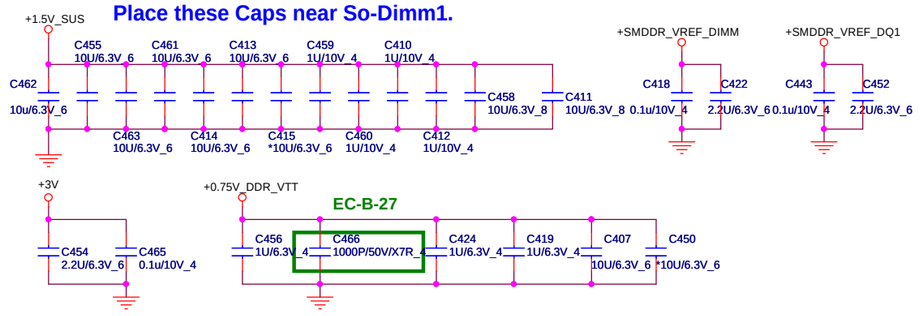
DDR_RVS(DDR)



02/23 Remove 0ohm to GND

Place these Caps near So-Dimm1.

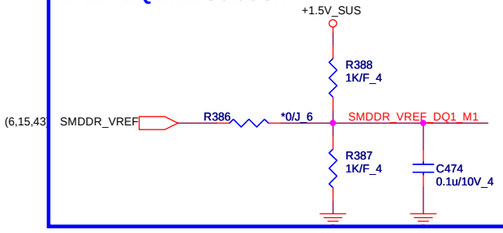


VREF DQ1 M2 Solution

6/22 Remove M2 Solution by MOW26

A16

VREF DQ1 M1 Solution



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8H type:DDR-C-2013310-204p-1		

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Custom	DDRIII SO-DIMM-0	1A
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DDR_RVS(DDR)

(5) M_A_A[15:0]

JDIM1A

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12/BC#
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15

(5) M_A_BS#0 109 BA0
(5) M_A_BS#1 108 BA1
(5) M_A_BS#2 79 BA2
(5) M_A_CS#0 114 S0#
(5) M_A_CS#1 121 S1#
(5) M_A_CLKP0 101 CK0
(5) M_A_CLKN0 103 CK0#
(5) M_A_CLKP1 102 CK1
(5) M_A_CLKN1 104 CK1#
(5) M_A_CKE0 73 CKE0
(5) M_A_CKE1 74 CKE1
(5) M_A_CAS# 115 CAS#
(5) M_A_RAS# 110 RAS#
(5) M_A_WE# 113 WE#

R356 10K/J_4 DIMM0_SA0 197 SA0
R355 10K/J_4 DIMM0_SA1 201 SA1

(10,14) SMB_RUN_CLK 202 SCL
(10,14) SMB_RUN_DAT 200 SDA

(5) M_A_ODT0 116 ODT0
(5) M_A_ODT1 120 ODT1

02/23 Remove 0ohm to GND

11 DM0
28 DM1
46 DM2
63 DM3
136 DM4
153 DM5
170 DM6
187 DM7

(5) M_A_DQSP[7:0]

M_A_DQSP0 12 DQS0
M_A_DQSP1 29 DQS1
M_A_DQSP2 47 DQS2
M_A_DQSP3 64 DQS3
M_A_DQSP4 137 DQS4
M_A_DQSP5 154 DQS5
M_A_DQSP6 171 DQS6
M_A_DQSP7 188 DQS7

(5) M_A_DQSN[7:0]

M_A_DQSN0 10 DQS#0
M_A_DQSN1 27 DQS#1
M_A_DQSN2 45 DQS#2
M_A_DQSN3 62 DQS#3
M_A_DQSN4 135 DQS#4
M_A_DQSN5 152 DQS#5
M_A_DQSN6 169 DQS#6
M_A_DQSN7 186 DQS#7

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=8_STD_LTS

M_A_DQ[63:0] (5)

DQ0 5 M_A_DQ4
DQ1 7 M_A_DQ5
DQ2 15 M_A_DQ6
DQ3 17 M_A_DQ7
DQ4 4 M_A_DQ0
DQ5 6 M_A_DQ1
DQ6 16 M_A_DQ3
DQ7 18 M_A_DQ2
DQ8 21 M_A_DQ13
DQ9 23 M_A_DQ9
DQ10 33 M_A_DQ15
DQ11 35 M_A_DQ14
DQ12 22 M_A_DQ12
DQ13 24 M_A_DQ8
DQ14 34 M_A_DQ10
DQ15 36 M_A_DQ11
DQ16 39 M_A_DQ22
DQ17 41 M_A_DQ19
DQ18 51 M_A_DQ16
DQ19 53 M_A_DQ21
DQ20 40 M_A_DQ18
DQ21 42 M_A_DQ23
DQ22 50 M_A_DQ17
DQ23 52 M_A_DQ20
DQ24 57 M_A_DQ31
DQ25 59 M_A_DQ27
DQ26 67 M_A_DQ30
DQ27 69 M_A_DQ29
DQ28 56 M_A_DQ24
DQ29 58 M_A_DQ26
DQ30 68 M_A_DQ25
DQ31 70 M_A_DQ28
DQ32 129 M_A_DQ37
DQ33 131 M_A_DQ33
DQ34 141 M_A_DQ38
DQ35 143 M_A_DQ34
DQ36 130 M_A_DQ32
DQ37 132 M_A_DQ36
DQ38 140 M_A_DQ35
DQ39 142 M_A_DQ39
DQ40 147 M_A_DQ44
DQ41 149 M_A_DQ47
DQ42 157 M_A_DQ46
DQ43 159 M_A_DQ45
DQ44 146 M_A_DQ41
DQ45 148 M_A_DQ40
DQ46 158 M_A_DQ42
DQ47 160 M_A_DQ43
DQ48 163 M_A_DQ54
DQ49 165 M_A_DQ55
DQ50 175 M_A_DQ51
DQ51 177 M_A_DQ50
DQ52 164 M_A_DQ48
DQ53 166 M_A_DQ49
DQ54 174 M_A_DQ53
DQ55 176 M_A_DQ52
DQ56 181 M_A_DQ61
DQ57 183 M_A_DQ58
DQ58 191 M_A_DQ57
DQ59 193 M_A_DQ63
DQ60 180 M_A_DQ56
DQ61 182 M_A_DQ60
DQ62 192 M_A_DQ59
DQ63 194 M_A_DQ62

	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		

+1.5V_SUS

2.48A

JDIM1B

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3V VDDSPD 199

NC1 77
NC2 122
NCTEST 125

+3V R354 10K/J_4

(14) PM_EXTTS#0 PM_EXTTS#0 EVENT# 198
(5,14) DDR3_DRAMRST# RESET# 30

SMDDR_VREF_DQ0_M1 R359 0/J_6 +SMDDR_VREF_DQ0
(7) SMDDR_VREF_DQ0_M3 SMDDR_VREF_DQ0_M3 R360 *0/J_6 +SMDDR_VREF_DIMM

VREF_DQ 1
VREF_CA 126

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

VTT1 203
VTT2 204

+0.75V_DDR_VTT

GND 205
GND 206

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=8_STD_LTS

Place these Caps near So-Dimm0.

+1.5V_SUS

C381 10U/6.3V_6
C389 10U/6.3V_6
C391 10U/6.3V_6
C402 10U/6.3V_6
C404 10U/6.3V_6
C390 10U/6.3V_6
C400 *10U/6.3V_6
C376 1U/10V_4
C388 1U/10V_4
C405 1U/10V_4
C406 1U/10V_4
C371 330U/2V_7343
C386 10U/6.3V_8
C401 10U/6.3V_8

+SMDDR_VREF_DIMM
C378 0.1u/10V_4
C387 2.2U/6.3V_6

+3V
C395 2.2U/6.3V_6
C399 0.1u/10V_4

+0.75V_DDR_VTT
C377 1U/6.3V_4
C385 1U/6.3V_4
C403 1u/6.3V_4
C398 1U/6.3V_4
C393 10U/6.3V_6
C394 *10U/6.3V_6

+SMDDR_VREF_DQ0
C396 0.1u/10V_4
C397 2.2U/6.3V_6

VREF DQ0 M1 Solution

+1.5V_SUS
R363 1K/F_4
SMDDR_VREF R358 *0/J_6 SMDDR_VREF_DQ0_M1
R362 1K/F_4
C416 0.1u/10V_4

+1.5V_SUS
R367 10K/J_4
(6,14,43) SMDDR_VREF R357 *0/J_6 +SMDDR_VREF_DIMM
R361 10K/J_4
C420 470P/50V_4

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
B	DDRIII SO-DIMM-1	1A

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POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=0.9~1.2V

2.5GT/s bit rate

U30A

PCI EXPRESS INTERFACE

(4) PEG_TXP15	PEG_TXP15	AE30	PCIE_RX0P	PCIE_TX0P	AH30	C_PEG_RXP15	C218	0.1U/10V_4	PEG_RXP15 (4)
(4) PEG_TXN15	PEG_TXN15	AE31	PCIE_RX0N	PCIE_TX0N	AG31	C_PEG_RXN15	C208	0.1U/10V_4	PEG_RXN15 (4)
(4) PEG_TXP14	PEG_TXP14	AE29	PCIE_RX1P	PCIE_TX1P	AG29	C_PEG_RXP14	C205	0.1U/10V_4	PEG_RXP14 (4)
(4) PEG_TXN14	PEG_TXN14	AD28	PCIE_RX1N	PCIE_TX1N	AF28	C_PEG_RXN14	C203	0.1U/10V_4	PEG_RXN14 (4)
(4) PEG_TXP13	PEG_TXP13	AD30	PCIE_RX2P	PCIE_TX2P	AF27	C_PEG_RXP13	C230	0.1U/10V_4	PEG_RXP13 (4)
(4) PEG_TXN13	PEG_TXN13	AC31	PCIE_RX2N	PCIE_TX2N	AF26	C_PEG_RXN13	C229	0.1U/10V_4	PEG_RXN13 (4)
(4) PEG_TXP12	PEG_TXP12	AC29	PCIE_RX3P	PCIE_TX3P	AD27	C_PEG_RXP12	C195	0.1U/10V_4	PEG_RXP12 (4)
(4) PEG_TXN12	PEG_TXN12	AB28	PCIE_RX3N	PCIE_TX3N	AD26	C_PEG_RXN12	C201	0.1U/10V_4	PEG_RXN12 (4)
(4) PEG_TXP11	PEG_TXP11	AB30	PCIE_RX4P	PCIE_TX4P	AC25	C_PEG_RXP11	C194	0.1U/10V_4	PEG_RXP11 (4)
(4) PEG_TXN11	PEG_TXN11	AA31	PCIE_RX4N	PCIE_TX4N	AB25	C_PEG_RXN11	C188	0.1U/10V_4	PEG_RXN11 (4)
(4) PEG_TXP10	PEG_TXP10	AA29	PCIE_RX5P	PCIE_TX5P	Y23	C_PEG_RXP10	C169	0.1U/10V_4	PEG_RXP10 (4)
(4) PEG_TXN10	PEG_TXN10	Y28	PCIE_RX5N	PCIE_TX5N	Y24	C_PEG_RXN10	C181	0.1U/10V_4	PEG_RXN10 (4)
(4) PEG_TXP9	PEG_TXP9	Y30	PCIE_RX6P	PCIE_TX6P	AB27	C_PEG_RXP9	C184	0.1U/10V_4	PEG_RXP9 (4)
(4) PEG_TXN9	PEG_TXN9	W31	PCIE_RX6N	PCIE_TX6N	AB26	C_PEG_RXN9	C186	0.1U/10V_4	PEG_RXN9 (4)
(4) PEG_TXP8	PEG_TXP8	W29	PCIE_RX7P	PCIE_TX7P	V27	C_PEG_RXP8	C163	0.1U/10V_4	PEG_RXP8 (4)
(4) PEG_TXN8	PEG_TXN8	V28	PCIE_RX7N	PCIE_TX7N	V26	C_PEG_RXN8	C168	0.1U/10V_4	PEG_RXN8 (4)
(4) PEG_TXP7	PEG_TXP7	V30	PCIE_RX8P	PCIE_TX8P	V24	C_PEG_RXP7	C162	0.1U/10V_4	PEG_RXP7 (4)
(4) PEG_TXN7	PEG_TXN7	U31	PCIE_RX8N	PCIE_TX8N	V23	C_PEG_RXN7	C153	0.1U/10V_4	PEG_RXN7 (4)
(4) PEG_TXP6	PEG_TXP6	U29	PCIE_RX9P	PCIE_TX9P	U27	C_PEG_RXP6	C148	0.1U/10V_4	PEG_RXP6 (4)
(4) PEG_TXN6	PEG_TXN6	T28	PCIE_RX9N	PCIE_TX9N	U26	C_PEG_RXN6	C151	0.1U/10V_4	PEG_RXN6 (4)
(4) PEG_TXP5	PEG_TXP5	T30	PCIE_RX10P	PCIE_TX10P	U24	C_PEG_RXP5	C145	0.1U/10V_4	PEG_RXP5 (4)
(4) PEG_TXN5	PEG_TXN5	R31	PCIE_RX10N	PCIE_TX10N	U23	C_PEG_RXN5	C138	0.1U/10V_4	PEG_RXN5 (4)
(4) PEG_TXP4	PEG_TXP4	R29	PCIE_RX11P	PCIE_TX11P	T26	C_PEG_RXP4	C137	0.1U/10V_4	PEG_RXP4 (4)
(4) PEG_TXN4	PEG_TXN4	P28	PCIE_RX11N	PCIE_TX11N	T27	C_PEG_RXN4	C127	0.1U/10V_4	PEG_RXN4 (4)
(4) PEG_TXP3	PEG_TXP3	P30	PCIE_RX12P	PCIE_TX12P	T24	C_PEG_RXP3	C115	0.1U/10V_4	PEG_RXP3 (4)
(4) PEG_TXN3	PEG_TXN3	N31	PCIE_RX12N	PCIE_TX12N	T23	C_PEG_RXN3	C125	0.1U/10V_4	PEG_RXN3 (4)
(4) PEG_TXP2	PEG_TXP2	N29	PCIE_RX13P	PCIE_TX13P	P27	C_PEG_RXP2	C111	0.1U/10V_4	PEG_RXP2 (4)
(4) PEG_TXN2	PEG_TXN2	M28	PCIE_RX13N	PCIE_TX13N	P26	C_PEG_RXN2	C105	0.1U/10V_4	PEG_RXN2 (4)
(4) PEG_TXP1	PEG_TXP1	M30	PCIE_RX14P	PCIE_TX14P	P24	C_PEG_RXP1	C101	0.1U/10V_4	PEG_RXP1 (4)
(4) PEG_TXN1	PEG_TXN1	L31	PCIE_RX14N	PCIE_TX14N	P23	C_PEG_RXN1	C95	0.1U/10V_4	PEG_RXN1 (4)
(4) PEG_TXP0	PEG_TXP0	L29	PCIE_RX15P	PCIE_TX15P	M27	C_PEG_RXP0	C88	0.1U/10V_4	PEG_RXP0 (4)
(4) PEG_TXN0	PEG_TXN0	K30	PCIE_RX15N	PCIE_TX15N	N26	C_PEG_RXN0	C83	0.1U/10V_4	PEG_RXN0 (4)

CLOCK

(10) CLK_PCIE_VGAP	AK30	PCIE_REFCLKP	
(10) CLK_PCIE_VGAN	AK32	PCIE_REFCLKN	

M93-S3--NC
PARK-S3--install
10K/F_4 1 2 R119 N10 NC_PWRGOOD

(4,10,25,29,31) PLTRST# AL27 PERSTB

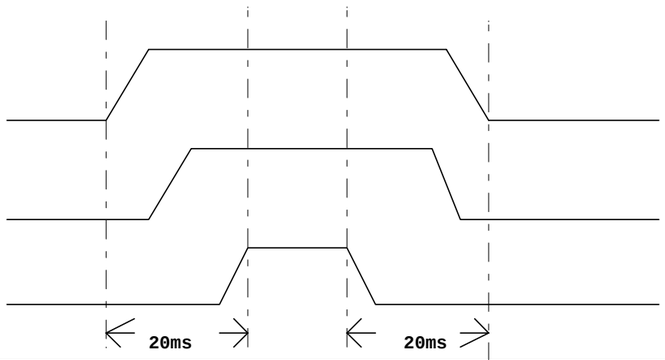
PARK

CALIBRATION

PCIE_CALRP	Y22	M72_PCIE_CALRP	R134	1.27K/F_4	
PCIE_CALRN	AA22	M72_PCIE_CALRN	R218	2K/F_4	+1.1V_GPU

100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

VGA Core	BPP
VGA Core	VDDC
+1.8V	PCIE_VDDR
+1.8V	PCIE_PVDD
+1.8V	VDDR1
+3V_VGA	VDDR3



U30G

DP E/F POWER

+1.8V_DPE_VDD18	AG15 AG16	DPE_VDD18#1 DPE_VDD18#2
+1.1V_DPE_VDD10	AG20 AG21	DPE_VDD10#1 DPE_VDD10#2
	AG14 AH14 AM14 AM16 AM18	DPE_VSSR#1 DPE_VSSR#2 DPE_VSSR#3 DPE_VSSR#4 DPE_VSSR#5
+1.8V_DPE_VDD18	AF16 AG17	DPF_VDD18#1 DPF_VDD18#2
+1.1V_DPE_VDD10	AF22 AG22	DPF_VDD10#1 DPF_VDD10#2
	AF23 AG23 AM20 AM22 AM24	DPF_VSSR#1 DPF_VSSR#2 DPF_VSSR#3 DPF_VSSR#4 DPF_VSSR#5
R186 150/F_4 DPEF_CALR	AF17	DPEF_CALR
+1.8V_DPE_PVDD +1.8V_DPE_PVDD	AG18 AF19	DPE_PVDD DPE_PVSS
+1.8V_DPF_PVDD R185 0_4	AG19 AF20	NC_DPF_PVDD NC_DPF_PVSS

M93-S3--NC
PARK-S3--install

DP A/B POWER

	AE11 AF11	NC_DPA_VDD18#1 NC_DPA_VDD18#2
	AF6 AF7	DPA_VDD10#1 DPA_VDD10#2
	AE1 AE3 AG1 AG6 AH5	DPA_VSSR#1 DPA_VSSR#2 DPA_VSSR#3 DPA_VSSR#4 DPA_VSSR#5
	AE13 AF13	NC_DPB_VDD18#1 NC_DPB_VDD18#2
	AE8 AF9	DPB_VDD10#1 DPB_VDD10#2
	AE10 AG9 AH8 AM6 AM8	DPB_VSSR#1 DPB_VSSR#2 DPB_VSSR#3 DPB_VSSR#4 DPB_VSSR#5
DPAB_CALR R575 150/F_4	AE10	DPAB_CALR
	AG8 AG7	DPA_PVDD DPA_PVSS
	AG10 AG11	DPB_PVDD DPB_PVSS

DP PLL POWER

PARK

+1.8V_DPA_VDD18 → AE11 AF11 → NC_DPA_VDD18#1 NC_DPA_VDD18#2
+1.1V_DPB_VDD10 → AF6 AF7 → DPA_VDD10#1 DPA_VDD10#2
+1.8V_DPA_VDD18 → AE13 AF13 → NC_DPB_VDD18#1 NC_DPB_VDD18#2
+1.1V_DPB_VDD10 → AF8 AF9 → DPB_VDD10#1 DPB_VDD10#2
+1.8V_DPA_PVDD → AG8 AG7 → DPA_PVDD DPA_PVSS
+1.8V_DPA_PVDD → AG10 AG11 → DPB_PVDD DPB_PVSS

BLM18PG181SN1D(180,1.5A)_6
L14 +1.1V_DPB_VDD10 → +1.1V_GPU
1.1V(S100,D200mA)
C204 0.1U/10V_4 C216 10U/6.3V_6S C206 1U/10V_4

(Park-S3:110mA@1.0V)
(M9X-S2/S3:200mA@1.1V)

+1.1V_DPE_VDD10 → +1.1V_GPU
L45 BLM18PG181SN1D(180,1.5A)_6
C239 0.1U/10V_4 C214 1U/10V_4 C251 10U/6.3V_6S

1.8V -(440mA)

+1.8V_DPE_VDD18 → +1.8V_GPU
C202 0.1U/10V_4 C604 1U/10V_4 C618 10U/6.3V_6S
L42 BLM18PG181SN1D(180,1.5A)_6

+1.8V_DPF_PVDD → +1.8V_GPU
1.8V(20mA)
C212 0.1U/10V_4 C237 1U/10V_4 C252 10U/6.3V_6S
L18 BLM18PG181SN1D(180,1.5A)_6
M93-S3--NC
PARK-S3--install

+1.8V_DPA_VDD18 → +1.8V_GPU
1.8V(130mA)
C199 0.1U/10V_4 C223 1U/10V_4 C232 10U/6.3V_6S
L15 BLM18PG181SN1D(180,1.5A)_6
M93-S3--NC
PARK-S3--install

+1.8V_DPA_PVDD → +1.8V_GPU
1.8V(20mA)
C217 0.1U/10V_4 C215 1U/10V_4 C222 10U/6.3V_6S
L13 BLM18PG181SN1D(180,1.5A)_6

+1.8V_DPE_PVDD → +1.8V_GPU
1.8V(20mA)
C213 0.1U/10V_4 C231 1U/10V_4 C253 10U/6.3V_6S
L19 BLM18PG181SN1D(180,1.5A)_6

Quanta Computer Inc.
PROJECT : DM4/RB4

Size	Document Number	Rev
	Robson_PCIE_Interface	1A
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MEM_ID[3:0]				Vendor	Type	Vendor P/N	Project
R160	R152	R146	R151				
0	0	0	0	Samsung	128MB*16-800MHZ	K4W2G1646C-HC12	KL8A/KL9A
0	0	0	1	Hynix	128MB*16 -800MHZ	H5TQ2G63BFR-12C	KL8A/KL9A
0	0	1	0	Samsung	64x16 800MHz	K4W1G1646E-HC12	KL9A only
0	0	1	1	Hynix	64x16 800MHz	H5TQ1G63DFR-12C	KL9A only

Table : VDDC_OPT VID

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VCC_GFX_CORE
1	1	1.12V
1	0	0.95V
0	1	1.05V
0	0	0.9V

U30B

M93-S3/M92-S2

DVCNTL_0/ DVPDATA_18
DVCNTL_1 / NC
DVCNTL_2 / NC
DVDATA_12 / DVPDATA_16
DVDATA_11 / DVPDATA_20
DVDATA_10 / DVPDATA_22
DVDATA_9 / DVPDATA_12
DVDATA_8 / DVPDATA_14
DVDATA_7 / DVPCNTL_0
DVDATA_6 / DVPDATA_8
DVDATA_5 / DVPDATA_6
DVDATA_4 DVPDATA_4

DVO

DVDATA_3 / DVPDATA_19
DVDATA_2 / DVPDATA_21
DVDATA_1 / DVPDATA_2
DVDATA_0 / DVPDATA_0

M93-S3/M92-S2

DPC_PVDD / DVPDATA_11
GND#82

DPC_VDD18#1/DVPDAT10
DPC_VDD18#2/DVPDAT23

DPC_VDD10#1/DVPDAT15
DPC_VDD10#2/DVPDAT17

DPC_VSSR#1 / DVPCLK
DPC_VSSR#2 / DVPDAT5
GND#77
GND#87
DPC_VSSR#5/ DVPCNTL_MV0

LVDS

(24) ROBSON_LVDS_DDCCLK
(24) ROBSON_LVDS_DDCDAT

I2C

SCL
SDA

GENERAL PURPOSE I/O

GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB

JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
TESTEN

GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4

HPD1

VREFG

PLL/CLOCK

DPLL_PVDD
DPLL_PVSS

DPLL_VDDC

XTALIN
XTALOUT
NC#2
NC#1

DPLUS
DMINUS

THERMAL

TS_FDO
TSVDD
TSVSS

PARK

DPA

TXCAP_DPA3P
TXCAM_DPA3N
TX0P_DPA2P
TX0M_DPA2N
TX1P_DPA1P
TX1M_DPA1N
TX2P_DPA0P
TX2M_DPA0N

DPB

TXCBP_DPB3P
TXCBM_DPB3N
TX3P_DPB2P
TX3M_DPB2N
TX4P_DPB1P
TX4M_DPB1N
TX5P_DPB0P
TX5M_DPB0N

M92-S2/M93-S3

DVPDATA_3/TXCCP_DPC3P
DVPCNTL_2/TXCCM_DPC3N
DVPDATA_7 / TX0P_DPC2P
DVPDATA_1 / TX0M_DPC2N
DVPCNTL_MV1 / TX1P_DPC1P
DVPDATA_9 / TX1M_DPC1N
DVPDATA_13 / TX2P_DPC0P
DVPCNTL_1 / TX2M_DPC0N
VDDR4 / DPCD_CALR

DPC

DAC1

R
RB
G
GB
B
BB
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1DI
VSS1DI

M92-S2/M93-S3

R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC
H2SYNC
V2SYNC
VDD2DI / NC
VSS2DI / NC
A2VDD / NC
A2VDDQ / NC
A2VSSQ
R2SET / NC

DAC2

DDC/AUX

DDC1CLK
DDC1DATA
AUX1P
AUX1N
DDC2CLK
DDC2DATA
AUX2P
AUX2N
DDCCLK_AUX5P
DDCDATA_AUX5N
DDC6CLK
DDC6DATA
DDCCLK_AUX3P
DDCDATA_AUX3N

HDMI

CRT

EC-B

EC-A-30

For M93-S3: Use 150 Ohms Pull Down
For M92-S2: Use 0R to VDDR4
For Park-S3: NC

R576 add for Robson EC layout
PARK, M93---->Install
Robson---------->Uninstall

0916: AMD modify

Reserved

M93 MV Added
AMD Suggestion

GPIO22(ROMCS#)
PD without external VBIOS ROM

For Int Clk 27Mhz

CL=20PF

PARK-- Install
M93-- NC

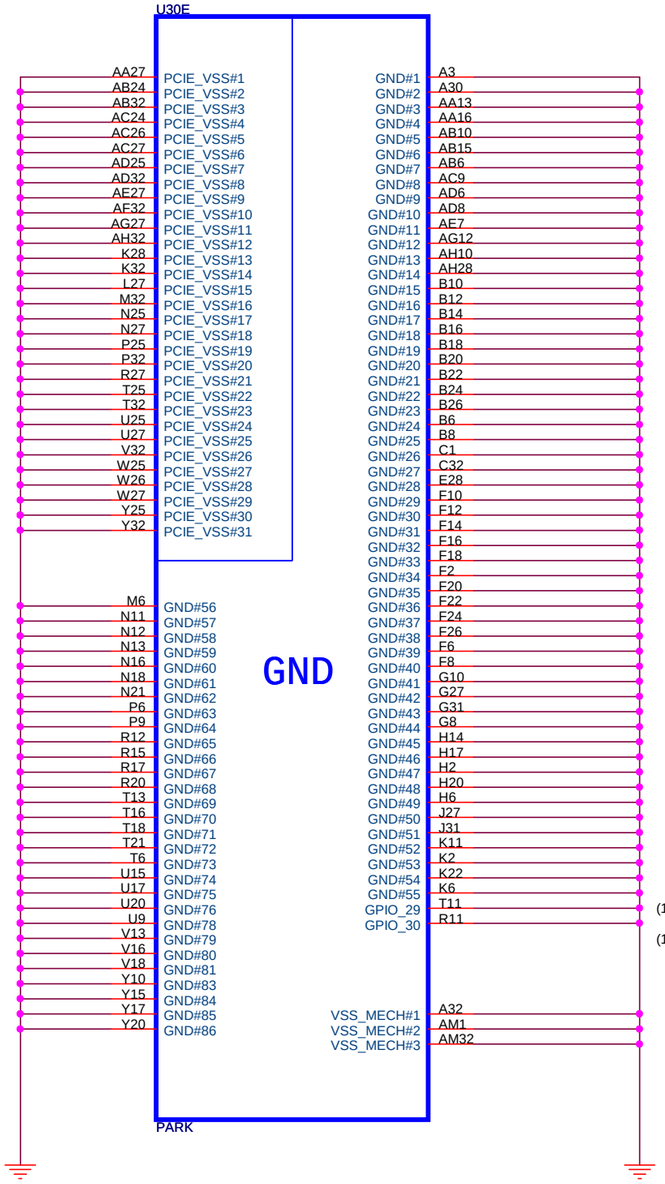
M93-S3--NC
PARK-S3--install

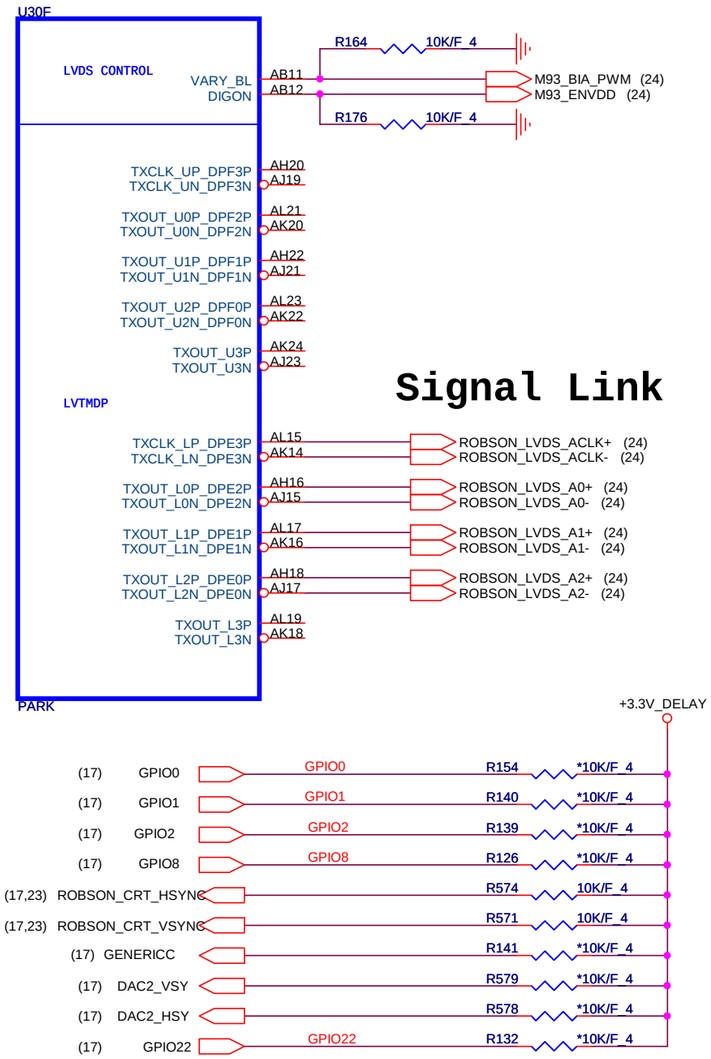
1.8V(70mA)
1.8V(45mA VDD1DI)
3.3V(65mA)
1.8V(200mA DPC_PVDD)
1.8V(130mA DPC_VDD18)
1.1V(200mA DPC_VDD10)
1.8V(120mADPLL_PVDD)
1.8V(300mA DPLL_VDDC)
1.8V(20mA TSVDD)
1.8V@75mA
1.8V@125mA

	Robson	Seymour
R694	ASM	No ASM
R695	ASM	No ASM
R696	ASM	No ASM
R228	ASM	No ASM
R161	ASM	No ASM
R576	ASM	No ASM
R205	ASM	No ASM

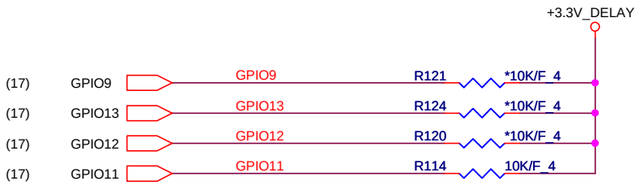
I2C ADDRESS: 9AH

W/S 10 / 10





Signal Link



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN ROMIDCFG(2:0) VIP_DEVICE_STRAP_ENA	GPIO_22_ROMCSB GPIO[13:11] V2SYNC	ENABLE EXTERNAL BIOS ROM SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT IGNORE VIP DEVICE STRAPS	0 0 0 1 0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

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	Robson_GND / LVDS /Straps	1A
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VDD_CT -- Level translation between core and I/O, excluding memory receivers.1.8 V ± 5%

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

+1.5V_GPU

1.5V (DDR3, MVDDQ = 1.5V@2.0A3)

C10 1U/10V_4, C550 1U/10V_4, C12 1U/10V_4, C76 1U/10V_4, C90 1U/10V_4, C91 1U/10V_4, C45 1U/10V_4, C543 1U/10V_4, C52 1U/10V_4, C21 1U/10V_4, C108 1U/10V_4, C85 1U/10V_4, C97 1U/10V_4, C87 1U/10V_4

C536 10U/6.3V_6S, C6 10U/6.3V_6S, C71 10U/6.3V_6S, C4 10U/6.3V_6S, C535 10U/6.3V_6S, C110 0.1U/10V_4, C92 0.1U/10V_4, C103 0.1U/10V_4, C89 0.1U/10V_4, C50 0.1U/10V_4, C120 0.1U/10V_4

U30D

MEM I/O

VDDR1#1 H13
VDDR1#2 H16
VDDR1#3 H19
VDDR1#4 J10
VDDR1#5 J23
VDDR1#6 J24
VDDR1#7 J9
VDDR1#8 K10
VDDR1#9 K23
VDDR1#10 K24
VDDR1#11 K9
VDDR1#12 L11
VDDR1#13 L12
VDDR1#14 L13
VDDR1#15 L20
VDDR1#16 L21
VDDR1#17 L22

1.8V(136mA VDD_CT)

+1.8V_GPU — L3 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_VDD_CT

C78 10U/6.3V_6S, C178 1U/10V_4, C94 1U/10V_4, C164 1U/10V_4, C84 0.1U/10V_4

+1.8V_VDD_CT

LEVEL TRANSLATION

VDD_CT#1 AA20
VDD_CT#2 AA21
VDD_CT#3 AB20
VDD_CT#4 AB21

+3.3V_DELAY

C243 1U/10V_4, C250 1U/10V_4, C179 1U/10V_4, C255 10U/6.3V_6S

M93-S3/M92-S2 I/O

VDDR3#1 AA17
VDDR3#2 AA18
VDDR3#3 AB17
VDDR3#4 AB18

+VDDR4

+1.8V_GPU — L9 BLM18PG181SN1D(180,1.5A)_6

1.8V(170mA VDDR4)

C171 10U/6.3V_6S, C175 1U/10V_4, C152 0.1U/10V_4

R156 0_4

VDDR4#1 / VDDR5 V12
VDDR4#2 Y12
VDDR4#3 / VDDR5 U12

NC#1 / VDDR4 AA11
DVCLK / VDDR4 Y11

NC#3 / VDDR5 V11
NC#4 / VDDR5 U11

MEM CLK

TP1 — L17 VDDRHA
TP2 — L16 VSSRHA

PLL

+1.8V_GPU — L40 BLM18PG181SN1D(180,1.5A)_6 — +PCIE_PVDD — AM30 PCIE_PVDD

1.8V(40mA PCIE_PVDD)

C600 10U/6.3V_6S, C599 1U/10V_4, C598 0.1U/10V_4

MPV18 L8 NC_MPV18

SPV18 H7 NC_SPV18

0.95V~1.1V(100mA SPV10)

+1.1V_GPU — L5 BLM18PG181SN1D(180,1.5A)_6 — +VGA_CORE_SPV10 — H8 SPV10

C102 10U/6.3V_6S, C100 0.1U/10V_4, C99 0.1U/10V_4

J7 SPVSS

BACK BIAS

MV +VGPU_CORE

1.5/1.8V 120mA

C142 1U/10V_4, C126 0.1U/10V_4

BBP#1 M11
BBP#2 M12

PARK

POWER

PCIE

PCIE_VDDR#1 AB23
PCIE_VDDR#2 AC23
PCIE_VDDR#3 AD24
PCIE_VDDR#4 AE24
PCIE_VDDR#5 AE25
PCIE_VDDR#6 AE26
PCIE_VDDR#7 AE25
PCIE_VDDR#8 AG26

+1.8V_PCIE_VDDR

1.8V(500mA)

+1.8V_PCIE_VDDR — BLM18PG181SN1D(180,1.5A)_6 — L39 — +1.8V_GPU

C180 0.1U/10V_4, C192 0.1U/10V_4, C590 1U/10V_4, C591 1U/10V_4, C587 1U/10V_4, C176 1U/10V_4, C588 1U/10V_4, C577 10U/6.3V_6S

+1.1V_PCIE_VDDC

1.1V(2.0A)

+1.1V_PCIE_VDDC — BLM21PG221SN1D(220,100M,2A)_8 — L2 — +1.1V_GPU

C79 1U/10V_4, C149 1U/10V_4, C135 1U/10V_4, C121 1U/10V_4, C72 1U/10V_4, C143 1U/10V_4, C112 1U/10V_4, C69 10U/6.3V_6S

PCIE_VDDC#1 L23
PCIE_VDDC#2 L24
PCIE_VDDC#3 L25
PCIE_VDDC#4 L26
PCIE_VDDC#5 M22
PCIE_VDDC#6 N22
PCIE_VDDC#7 N23
PCIE_VDDC#8 N24
PCIE_VDDC#9 R22
PCIE_VDDC#10 T22
PCIE_VDDC#11 U22
PCIE_VDDC#12 V22

CORE

VDDC+VDDCI

0.95~1.1V(15A peak)(Ripple < 87.2mV)

+VGPU_CORE

VDDC#1 AA15
VDDC#2 N15
VDDC#3 N17
VDDC#4 R13
VDDC#5 R16
VDDC#6 R18
VDDC#7 R21
VDDC#8 T12
VDDC#9 T15
VDDC#10 T17
VDDC#11 T20
VDDC#12 U13
VDDC#13 U16
VDDC#14 U18
VDDC#15 U21
VDDC#16 V15
VDDC#17 V17
VDDC#18 V20
VDDC#19 V21
VDDC#20 Y13
VDDC#21 Y16
VDDC#22 Y18
VDDC#23 Y21

C141 1U/10V_4, C167 1U/10V_4, C161 1U/10V_4, C166 1U/10V_4, C165 1U/10V_4, C159 1U/10V_4, C147 1U/10V_4, C140 1U/10V_4, C73 10U/6.3V_6S

C131 1U/10V_4, C154 1U/10V_4, C144 1U/10V_4, C139 1U/10V_4, C155 1U/10V_4, C124 1U/10V_4, C136 22U/6.3V_6, C74 22U/6.3V_6

M93 MV,for meet AC transient SPEC add C844, C845 and del C277

C160 1U/10V_4, C146 1U/10V_4, C77 1U/10V_4, C134 1U/10V_4, C68 10U/6.3V_6S, C150 10U/6.3V_6S, C66 10U/6.3V_6S, C67 10U/6.3V_6S

C123 1U/10V_4, C172 1U/10V_4

ISOLATED CORE I/O

VDDCI#1 M13
VDDCI#2 M15
VDDCI#3 M16
VDDCI#4 M17
VDDCI#5 M18
VDDCI#6 M20
VDDCI#7 M21
VDDCI#8 N20

0.95V~1.1V(2A VDDCI)

+VDDCI — BLM18SG121TN1D(120,100M,3A)_8 — L4 — +VGPU_CORE

C109 1U/10V_4, C122 1U/10V_4, C117 1U/10V_4, C81 10U/6.3V_6S, C82 10U/6.3V_6S, C80 10U/6.3V_6S

VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

+1.1V_PCIE_VDDC — C116 1U/10V_4

+1.8V_PCIE_VDDR — C177 0.1U/10V_4, C589 1U/10V_4

Reserve for PARK

1.8V(75mA MPV18)

+1.8V_GPU — L7 BLM18PG181SN1D(180,1.5A)_6 — MPV18

C128 1U/10V_4, C129 0.1U/10V_4

1.8V(90mA SPV18)

+1.8V_GPU — L6 BLM18PG181SN1D(180,1.5A)_6 — SPV18

C98 1U/10V_4, C93 0.1U/10V_4

+VGPU_CORE (38,41,46)

Quanta Computer Inc.

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	Robson_Power_and_NC	1A
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(21) VMA_ODT0 — VMA_ODT0
(21) VMA_ODT1 — VMA_ODT1

(21) VMA_RAS0# — VMA_RAS0#
(21) VMA_RAS1# — VMA_RAS1#

(21) VMA_CAS0# — VMA_CAS0#
(21) VMA_CAS1# — VMA_CAS1#

(21) VMA_WE0# — VMA_WE0#
(21) VMA_WE1# — VMA_WE1#

(21) VMA_CS0# — VMA_CS0#

(21) VMA_CS1# — VMA_CS1#

(21) VMA_CKE0 — VMA_CKE0
(21) VMA_CKE1 — VMA_CKE1

(21) VMA_CLK0 — VMA_CLK0
(21) VMA_CLK0# — VMA_CLK0#

(21) VMA_CLK1 — VMA_CLK1
(21) VMA_CLK1# — VMA_CLK1#

(21) VMA_WDQS[7..0] — VMA_WDQS[7..0]

(21) VMA_RDQS[7..0] — VMA_RDQS[7..0]

(21) VMA_DM[7..0] — VMA_DM[7..0]

(21) VMA_DQ[63..0] — VMA_DQ[63..0]

(21) VMA_MA[13..0] — VMA_MA[13..0]

(21) VMA_BA0 — VMA_BA0
(21) VMA_BA1 — VMA_BA1
(21) VMA_BA2 — VMA_BA2

support 1Gbit VRAM (64M X 16)

DIVIDER RESISTORS	ROBSON
MVREF TO 1.8V (Rd)	40.2R
MVREF TO GND (Re)	100R

U30C

MEMORY INTERFACE

VMA_DQ0	K27	DQA_0	
VMA_DQ1	J29	DQA_1	
VMA_DQ2	H30	DQA_2	
VMA_DQ3	H32	DQA_3	
VMA_DQ4	G29	DQA_4	
VMA_DQ5	F28	DQA_5	
VMA_DQ6	F32	DQA_6	
VMA_DQ7	F30	DQA_7	
VMA_DQ8	C30	DQA_8	
VMA_DQ9	F27	DQA_9	
VMA_DQ10	A28	DQA_10	
VMA_DQ11	C28	DQA_11	
VMA_DQ12	E27	DQA_12	
VMA_DQ13	G26	DQA_13	
VMA_DQ14	D26	DQA_14	
VMA_DQ15	F25	DQA_15	
VMA_DQ16	A25	DQA_16	
VMA_DQ17	C25	DQA_17	
VMA_DQ18	E25	DQA_18	
VMA_DQ19	D24	DQA_19	
VMA_DQ20	E23	DQA_20	
VMA_DQ21	F23	DQA_21	
VMA_DQ22	D22	DQA_22	
VMA_DQ23	F21	DQA_23	
VMA_DQ24	E21	DQA_24	
VMA_DQ25	D20	DQA_25	
VMA_DQ26	F19	DQA_26	
VMA_DQ27	A19	DQA_27	
VMA_DQ28	D18	DQA_28	
VMA_DQ29	F17	DQA_29	
VMA_DQ30	A17	DQA_30	
VMA_DQ31	C17	DQA_31	
VMA_DQ32	E17	DQA_32	
VMA_DQ33	D16	DQA_33	
VMA_DQ34	F15	DQA_34	
VMA_DQ35	A15	DQA_35	
VMA_DQ36	D14	DQA_36	
VMA_DQ37	F13	DQA_37	
VMA_DQ38	A13	DQA_38	
VMA_DQ39	C13	DQA_39	
VMA_DQ40	E11	DQA_40	
VMA_DQ41	A11	DQA_41	
VMA_DQ42	C11	DQA_42	
VMA_DQ43	F11	DQA_43	
VMA_DQ44	A9	DQA_44	
VMA_DQ45	C9	DQA_45	
VMA_DQ46	F9	DQA_46	
VMA_DQ47	D8	DQA_47	
VMA_DQ48	E7	DQA_48	
VMA_DQ49	A7	DQA_49	
VMA_DQ50	C7	DQA_50	
VMA_DQ51	F7	DQA_51	
VMA_DQ52	A5	DQA_52	
VMA_DQ53	E5	DQA_53	
VMA_DQ54	C3	DQA_54	
VMA_DQ55	E1	DQA_55	
VMA_DQ56	G7	DQA_56	
VMA_DQ57	G6	DQA_57	
VMA_DQ58	G1	DQA_58	
VMA_DQ59	G3	DQA_59	
VMA_DQ60	J6	DQA_60	
VMA_DQ61	J1	DQA_61	
VMA_DQ62	J3	DQA_62	
VMA_DQ63	J5	DQA_63	
	K26	MVREFDA	
	J26	MVREFSA	
	J25	MEM_CALRN0	
	K7	NC/TESTEN#2	
	J8	MEM_CALRP1/DPC_CALR	
	K25	NC_MEM_CALRP0	
DRAM_RST	L10	DRAM_RST	
CLKTESTA	K8	CLKTESTA	
CLKTESTB	L7	CLKTESTB	

PARK

MAA_0	K17	VMA_MA0
MAA_1	J20	VMA_MA1
MAA_2	H23	VMA_MA2
MAA_3	G23	VMA_MA3
MAA_4	G24	VMA_MA4
MAA_5	H24	VMA_MA5
MAA_6	J19	VMA_MA6
MAA_7	K19	VMA_MA7
MAA_8	J14	VMA_MA8
MAA_9	K14	VMA_MA9
MAA_10	J11	VMA_MA10
MAA_11	J13	VMA_MA11
MAA_12	H11	VMA_MA12
MAA_13/BA2	G11	VMA_BA2
MAA_14/BA0	J16	VMA_BA0
MAA_15/BA1	L15	VMA_BA1
DQMA_0	E32	VMA_DM0
DQMA_1	E30	VMA_DM1
DQMA_2	A21	VMA_DM2
DQMA_3	C21	VMA_DM3
DQMA_4	E13	VMA_DM4
DQMA_5	D12	VMA_DM5
DQMA_6	E3	VMA_DM6
DQMA_7	F4	VMA_DM7
RDQSA_0	H28	VMA_RDQS0
RDQSA_1	C27	VMA_RDQS1
RDQSA_2	A23	VMA_RDQS2
RDQSA_3	E19	VMA_RDQS3
RDQSA_4	E15	VMA_RDQS4
RDQSA_5	D10	VMA_RDQS5
RDQSA_6	D6	VMA_RDQS6
RDQSA_7	G5	VMA_RDQS7
WDQSA_0	H27	VMA_WDQS0
WDQSA_1	A27	VMA_WDQS1
WDQSA_2	C23	VMA_WDQS2
WDQSA_3	C19	VMA_WDQS3
WDQSA_4	C15	VMA_WDQS4
WDQSA_5	E9	VMA_WDQS5
WDQSA_6	C5	VMA_WDQS6
WDQSA_7	H4	VMA_WDQS7
ODTA0	L18	VMA_ODT0
ODTA1	K16	VMA_ODT1
CLKA0	H26	VMA_CLK0
CLKA0B	H25	VMA_CLK0#
CLKA1	G9	VMA_CLK1
CLKA1B	H9	VMA_CLK1#
RASA0B	G22	VMA_RAS0#
RASA1B	G17	VMA_RAS1#
CASA0B	G19	VMA_CAS0#
CASA1B	G16	VMA_CAS1#
CSA0B_0	H22	VMA_CS0#
CSA0B_1	J22	
CSA1B_0	G13	VMA_CS1#
CSA1B_1	K13	
CKEA0	K20	VMA_CKE0
CKEA1	J17	VMA_CKE1
WEA0B	G25	VMA_WE0#
WEA1B	H10	VMA_WE1#
PX_EN	AB16	
RSVD#2	G14	
RSVD#3	G20	VMA_MA13

For PARK-S3 only
For M9X-S2/S3 with DDR3: this pin is not in use.

+1.5V_GPU
Rd R58 40.2/F_4
Re R63 100/F_4
C64 0.1U/10V_4

PLACE MVREFD DIVIDERS AND CAPS CLOSE TO ASIC

MVREFD
+1.5V_GPU
Rd R73 40.2/F_4
Re R74 100/F_4
C96 0.1U/10V_4
MVREFS

+1.5V_GPU — Note 1 — R70 240_4 — J25
(17) TESTEN — Note 3 — K7
R85 5.11K
R72 150/F_4 — Note 2 — J8
R84 240_4 — Note 1 — K25

C133 0.1U/10V_4
C132 0.1U/10V_4
R125 51.1/F_4
R112 51.1/F_4

route 50ohms single-ended/100ohms diff and keep short For PARK-S3 only

+1.5V_GPU
Rc R28 2.2K_4
Rb
DRAM_RST — R29 0_4 — MEM_RST (21)
Ra R30 *10K/F_4
Ca C19 2200P/50V_4

Ra Rb Rc Rd

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24
R575 for Robson only

Quanta Computer Inc.
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	Robson_MEM_Interface	1A
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1GB DDR3 2Gb DDR3(128MB x16bit) x 4 pcs

(20) VMA_MA[13..0]
(20) VMA_DM[7..0]
VMA_MA[13..0]
(20) VMA_DQ[63..0]
(20) VMA_WDQS[7..0]
(20) VMA_RDQS[7..0]

EC-C-07

U29

VREFC_VMA1
VREFD_VMA1
VMA_MA0
VMA_MA1
VMA_MA2
VMA_MA3
VMA_MA4
VMA_MA5
VMA_MA6
VMA_MA7
VMA_MA8
VMA_MA9
VMA_MA10
VMA_MA11
VMA_MA12
VMA_MA13
(20) VMA_BA0
(20) VMA_BA1
(20) VMA_BA2
(20) VMA_CLK0
(20) VMA_CLK0#
(20) VMA_CKE0
(20) VMA_ODT0
(20) VMA_CS0#
(20) VMA_RAS0#
(20) VMA_CAS0#
(20) VMA_WE0#
VMA_RDQS3
VMA_RDQS0
VMA_DM3
VMA_DM0
VMA_WDQS3
VMA_WDQS0
(20) MEM_RST
VMA_ZQ1
R48 240
VMA_DQ27 VMA_DQ28 VMA_DQ25 VMA_DQ30 VMA_DQ26 VMA_DQ29 VMA_DQ24 VMA_DQ31
VMA_DQ0 VMA_DQ2 VMA_DQ1 VMA_DQ6 VMA_DQ5 VMA_DQ7 VMA_DQ4 VMA_DQ3
+1.5V_GPU
100-BALL SDRAM DDR3 VRAM _DDR3

U4

VREFC_VMA2
VREFD_VMA2
VMA_MA0
VMA_MA1
VMA_MA2
VMA_MA3
VMA_MA4
VMA_MA5
VMA_MA6
VMA_MA7
VMA_MA8
VMA_MA9
VMA_MA10
VMA_MA11
VMA_MA12
VMA_MA13
VMA_BA0
VMA_BA1
VMA_BA2
VMA_CLK0
VMA_CLK0#
VMA_CKE0
VMA_ODT0
VMA_CS0#
VMA_RAS0#
VMA_CAS0#
VMA_WE0#
VMA_RDQS2
VMA_RDQS1
VMA_DM2
VMA_DM1
VMA_WDQS2
VMA_WDQS1
MEM_RST
VMA_ZQ2
R25 240
VMA_DQ21 VMA_DQ18 VMA_DQ20 VMA_DQ17 VMA_DQ23 VMA_DQ16 VMA_DQ22 VMA_DQ19
VMA_DQ14 VMA_DQ15 VMA_DQ11 VMA_DQ13 VMA_DQ10 VMA_DQ9 VMA_DQ8 VMA_DQ12
+1.5V_GPU
100-BALL SDRAM DDR3 VRAM _DDR3

U5

VREFC_VMA3
VREFD_VMA3
VMA_MA0
VMA_MA1
VMA_MA2
VMA_MA3
VMA_MA4
VMA_MA5
VMA_MA6
VMA_MA7
VMA_MA8
VMA_MA9
VMA_MA10
VMA_MA11
VMA_MA12
VMA_MA13
VMA_BA0
VMA_BA1
VMA_BA2
(20) VMA_CLK1
(20) VMA_CLK1#
(20) VMA_CKE1
(20) VMA_ODT1
(20) VMA_CS1#
(20) VMA_RAS1#
(20) VMA_CAS1#
(20) VMA_WE1#
VMA_RDQS7
VMA_RDQS6
VMA_DM7
VMA_DM6
VMA_WDQS7
VMA_WDQS6
MEM_RST
VMA_ZQ3
R59 240
VMA_DQ61 VMA_DQ59 VMA_DQ63 VMA_DQ57 VMA_DQ58 VMA_DQ56 VMA_DQ62 VMA_DQ60
VMA_DQ51 VMA_DQ52 VMA_DQ48 VMA_DQ55 VMA_DQ50 VMA_DQ54 VMA_DQ49 VMA_DQ53
+1.5V_GPU
100-BALL SDRAM DDR3 VRAM _DDR3

U28

VREFC_VMA4
VREFD_VMA4
VMA_MA0
VMA_MA1
VMA_MA2
VMA_MA3
VMA_MA4
VMA_MA5
VMA_MA6
VMA_MA7
VMA_MA8
VMA_MA9
VMA_MA10
VMA_MA11
VMA_MA12
VMA_MA13
VMA_BA0
VMA_BA1
VMA_BA2
VMA_CLK1
VMA_CLK1#
VMA_CKE1
VMA_ODT1
VMA_CS1#
VMA_RAS1#
VMA_CAS1#
VMA_WE1#
VMA_RDQS4
VMA_RDQS5
VMA_DM4
VMA_DM5
VMA_WDQS4
VMA_WDQS5
MEM_RST
VMA_ZQ4
R467 240
VMA_DQ36 VMA_DQ38 VMA_DQ33 VMA_DQ39 VMA_DQ32 VMA_DQ37 VMA_DQ35 VMA_DQ34
VMA_DQ44 VMA_DQ43 VMA_DQ47 VMA_DQ40 VMA_DQ45 VMA_DQ41 VMA_DQ46 VMA_DQ42
+1.5V_GPU
100-BALL SDRAM DDR3 VRAM _DDR3

+1.5V_GPU
R476 4.99K/F_4
R477 4.99K/F_4
VREFC_VMA1
C559 .1U/10V_4
R472 4.99K/F_4
R473 4.99K/F_4
VREFD_VMA1
C549 .1U/10V_4
R27 4.99K/F_4
R26 4.99K/F_4
VREFC_VMA2
C18 .1U/10V_4
R52 4.99K/F_4
R54 4.99K/F_4
VREFD_VMA2
C60 .1U/10V_4
R56 4.99K/F_4
R55 4.99K/F_4
VREFC_VMA3
C53 .1U/10V_4
R31 4.99K/F_4
R32 4.99K/F_4
VREFD_VMA3
C24 .1U/10V_4
R471 4.99K/F_4
R470 4.99K/F_4
VREFC_VMA4
C541 .1U/10V_4
R53 4.99K/F_4
R57 4.99K/F_4
VREFD_VMA4
C58 .1U/10V_4

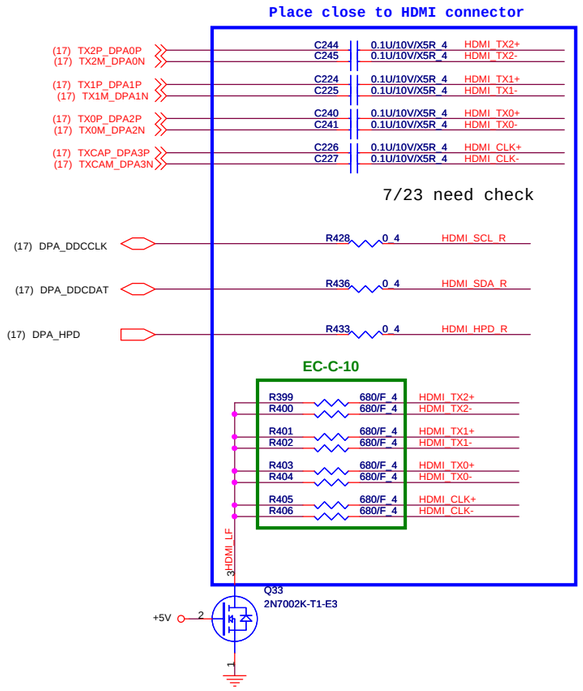
VMA_CLK0
R475 56.2/F_4
VMA_CLK0_COMM
C532 .01U/16V_4
R474 56.2/F_4
VMA_CLK0#
VMA_CLK1
R468 56.2/F_4
VMA_CLK1_COMM
C531 .01U/16V_4
R469 56.2/F_4
VMA_CLK1#

+1.5V_GPU
C552 1U/6.3V_4
C26 1U/6.3V_4
C17 1U/6.3V_4
C539 1U/6.3V_4
C16 1U/6.3V_4
C540 1U/6.3V_4
C556 1U/6.3V_4
C544 1U/6.3V_4
C542 1U/6.3V_4
C25 1U/6.3V_4
C20 1U/6.3V_4
C46 1U/6.3V_4
C38 1U/6.3V_4
C51 1U/6.3V_4
C42 1U/6.3V_4
C56 1U/6.3V_4
C557 1U/6.3V_4
C546 1U/6.3V_4
C548 1U/6.3V_4
C547 1U/6.3V_4
C545 1U/6.3V_4
C22 1U/6.3V_4
C23 1U/6.3V_4
C555 1U/6.3V_4
C15 1U/6.3V_4
C13 1U/6.3V_4
C14 1U/6.3V_4
C11 1U/6.3V_4
C41 1U/6.3V_4
C551 1U/6.3V_4
C48 1U/6.3V_4
C57 1U/6.3V_4
C54 10U/6.3V_6S
C538 10U/6.3V_6S
C537 10U/6.3V_6S
C9 10U/6.3V_6S
C5 10U/6.3V_6S
C7 10U/6.3V_6S
C8 10U/6.3V_6S
C558 10U/6.3V_6S
C34 10U/6.3V_6S
C554 10U/6.3V_6S
C533 10U/6.3V_6S
C534 10U/6.3V_6S

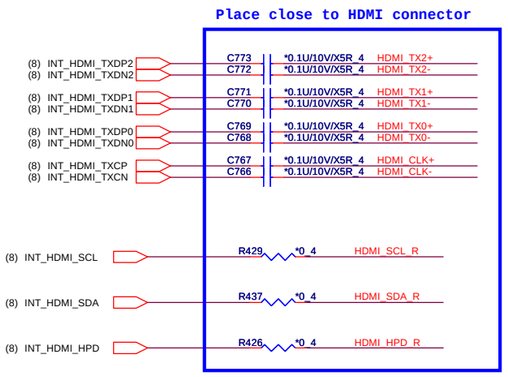
Quanta Computer Inc.
PROJECT : DM4/RB4

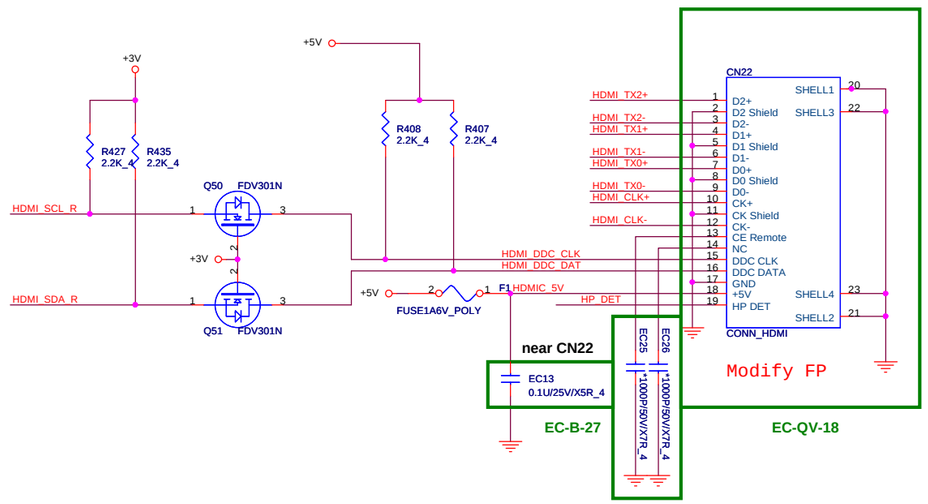
Size	Document Number	Rev
	Robson/VRAM_A0,A1	1A
Date: Friday, November 19, 2010	Sheet 21 of 53	

DIS HDMI

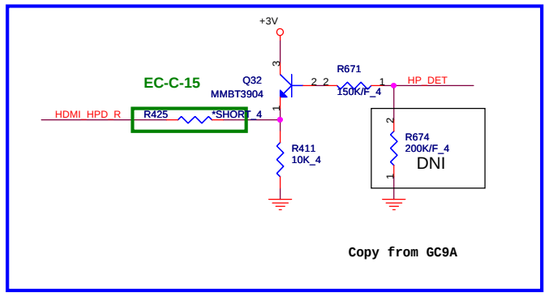


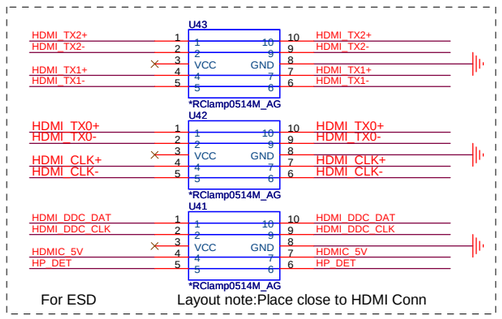
UMA Only



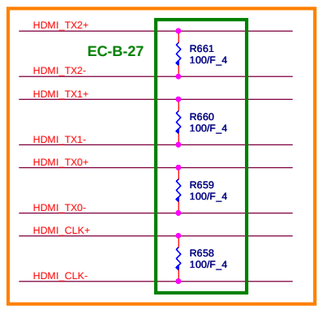


HDMI Hot-PLUG to EC and GPU





EMI reserve for HDMI



(8,9,12,23,26,28,35,36,37,38,40,41,42,49) +5V
(8,9,10,11,12,14,15,17,23,24,26,27,28,29,30,31,36,37,38,40,41,42,46,47,48,49) +3V

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

Date: Tuesday, January 04, 2011 Sheet 22 of 53

(8,9,12,22,26,28,35,36,37,38,40,41,42,49) +5V
(8,9,10,11,12,14,15,17,22,24,26,27,28,29,30,31,36,37,38,40,41,42,46,47,48,49) +3V

EC-B-06

ESD PROTECTION

U47
CRT_R1 — IO1 IO4 — CRT_G1
DDCDAT — GND REF
IO2 IO3 — CRT_B1
TVLST2304AD0

U48
CRT_VCC_R — IO1 IO4 — DDCCLK
CRTHSYNC — GND REF
IO2 IO3 — CRTVSYNC
TVLST2304AD0

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

CRT_VCC
D24 RB500V-40
+5V — F2 FUSE1A6V_POLY — CRT_VCC_R
C687 *VARISTOR_4
C683 0.1U/10V/X5R_4

ROBSON_CRT_RED_R — L33 BK1608LL680 — CRT_R1
ROBSON_CRT_GRN_R — L32 BK1608LL680 — CRT_G1
ROBSON_CRT_BLU_R — L31 BK1608LL680 — CRT_B1
R298 150/F_4
R289 150/F_4
R278 150/F_4
C334 5.6P/50V/COG_4
C321 5.6P/50V/COG_4
C312 5.6P/50V/COG_4
C311 5.6P/50V/COG_4
C320 5.6P/50V/COG_4
C333 5.6P/50V/COG_4
TP51

CN17 CRT_CONN

+5V
U15 AHCT1G125DCH
ROBSON_CRT_VSYNC_R — VGAVSYNC_R — R262 10_4 — CRTVSYNC1
C285 0.1U/10V/X5R_4
U16 AHCT1G125DCH
ROBSON_CRT_HSYNC_R — VGAHSYNC_R — R263 10_4 — CRTHSYNC1
Place near U37,U38 < 200 mil
C291 *10P/50V/COG_4
C290 *10P/50V/COG_4
L29 HB-1T1608-121JT — CRTVSYNC
L30 HB-1T1608-121JT — CRTHSYNC
C301 10P/50V/COG_4
C300 10P/50V/COG_4
Place near CN5002 connector < 200 mil

DIS

(8) INT_CRT_VSYNC	R103 / R102	*0_4 / 0_4	ROBSON_CRT_VSYNC_R
(17,18) ROBSON_CRT_VSYNC			
(8) INT_CRT_HSYNC	R118 / R117	*0_4 / 0_4	ROBSON_CRT_HSYNC_R
(17,18) ROBSON_CRT_HSYNC			
(8) INT_DDCCLK	R166 / R165	*0_4 / 0_4	ROBSON_CRT_DDCCLK_R
(17) ROBSON_CRT_DDCCLK			
(8) INT_DDCDAT	R159 / R158	*0_4 / 0_4	ROBSON_CRT_DDCDAT_R
(17) ROBSON_CRT_DDCDAT			
(8) INT_CRT_RED	R148 / R147	*0_4 / 0_4	ROBSON_CRT_RED_R
(17) ROBSON_CRT_RED			
(8) INT_CRT_GRE	R138 / R137	*0_4 / 0_4	ROBSON_CRT_GRN_R
(17) ROBSON_CRT_GRN			
(8) INT_CRT_BLU	R130 / R129	*0_4 / 0_4	ROBSON_CRT_BLU_R
(17) ROBSON_CRT_BLU			

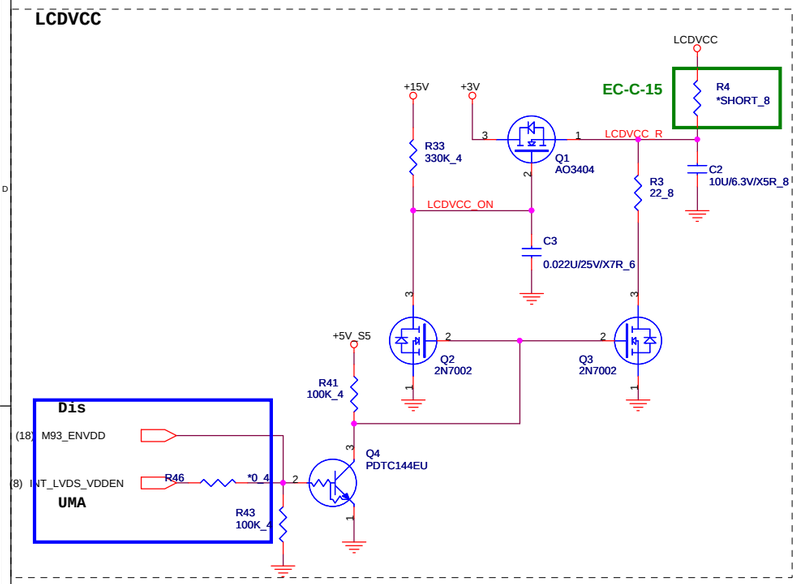
+3V
R619 2.2K_4
R609 2.2K_4
CRT_VCC
R616 4.7K_4
R611 4.7K_4
ROBSON_CRT_DDCCLK_R — Q41 2N7002K-T1-E3 — DDCCLK
+3V
ROBSON_CRT_DDCDAT_R — Q43 2N7002K-T1-E3 — DDCDAT
C694 *10P/50V/COG_4
C679 *10P/50V/COG_4

PROJECT : KL2D
Quanta Computer Inc.

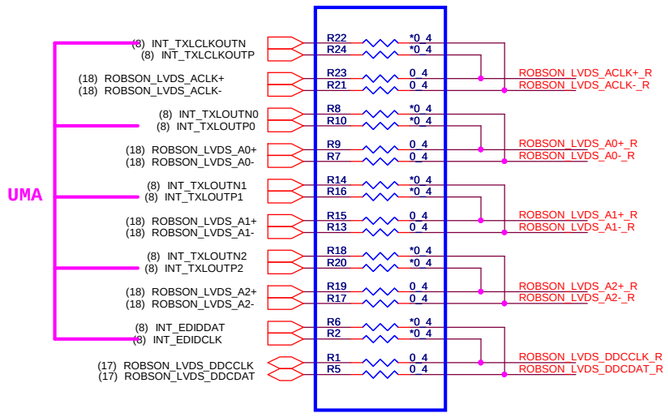
Size	Document Number	Rev
C	CRT CONN	1A

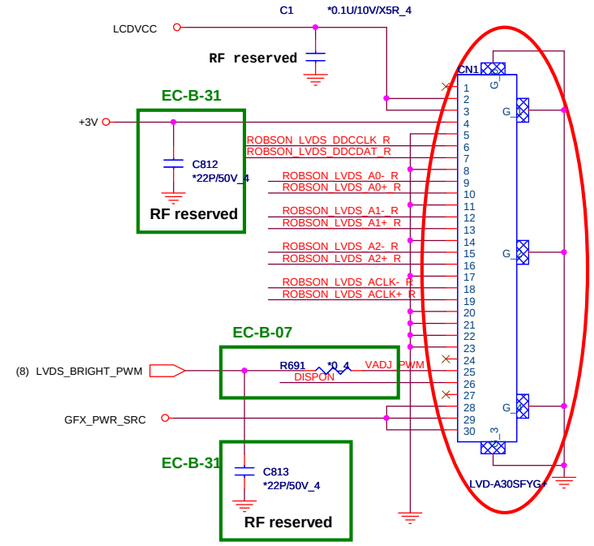
Date: Tuesday, January 04, 2011 Sheet 23 of 53

LCDVCC

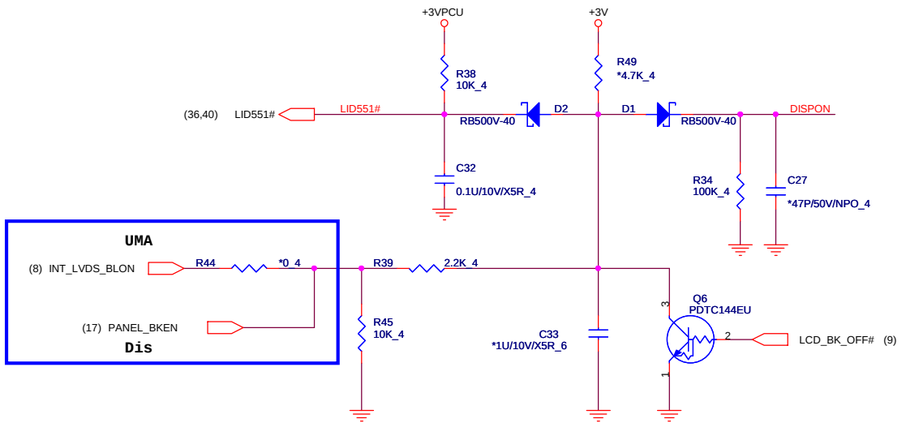


Layout note: Those resister place colse LVDS connector

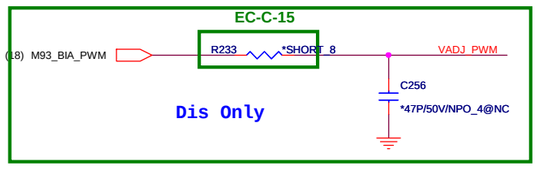


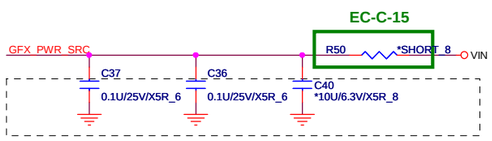


Back light



EC-B-07





PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
C	LCD CONN	1A
Date: Tuesday, January 04, 2011	Sheet 24 of 53	

(4,8,9,10,11,12,29,31,36,40,41) +3V_S5
(4,6,8,9,10,12,31,38,41,48) +1.05V_PCH
(8,9,24,28,35,36,38,40,41,42,44,45,46) +3VPCU

LANVCC

+3VPCU
Q48 AO6402A
(8) SLP_LAN# — R666 *0_4 — Q48.3
(41) LAN_ON — R663 *0_4_short — Q48.4
Q48.1 Q48.2 Q48.5 Q48.6
EC-C-15
+3.3V_LAN — R652 *SHORT_8 — +3.3V_LAN_R
C738 0.1U/10V/X5R_4

Core Power Decoupling

+1.0V_LOM
C721 4.7U/6.3V/X5R_6
C746 C731 C726 C725 C740 C743 C744 0.1U/10V/X5R_4
C745 0.1U/10V/X5R_4

VDDIO Power Decoupling

+3.3V_LAN
C737 4.7U/6.3V/X5R_6
C732 C733 C735 0.1U/10V/X5R_4
C747 10U/10V/X5R_8

U38

(10) PCIE_CLKREQ_LAN# (4,10,16,29,31) PLTRST# — CLK_REQ_N, PE_RST_N
(10) CLK_PCIE_LANP / (10) CLK_PCIE_LANN — PE_CLKP, PE_CLKN
(10) PCIE_RXP2_LAN / (10) PCIE_RXN2_LAN — C741 0.1U/10V/X5R_4 LAN_PCIETXDP; C742 0.1U/10V/X5R_4 LAN_PCIETXDN — PETp, PETn
(10) PCIE_TXP2_LAN / (10) PCIE_TXN2_LAN — PERp, PERn
PCIE

MDI_PLUS0 / MDI_MINUS0 — TRD0+ / TRD0-
MDI_PLUS1 / MDI_MINUS1 — TRD1+ / TRD1-
MDI_PLUS2 / MDI_MINUS2 — TRD2+ / TRD2-
MDI_PLUS3 / MDI_MINUS3 — TRD3+ / TRD3-
MDI

+3.3V_LAN
R647 *10K_4
EC-C-15
(11) LAN_DISABLE# — R648 *SHORT_4 — LAN_DISABLE_N
R645 *10K_4
SMB_CLK_ME0_R — SMB_CLK
SMB_DAT_ME0_R — SMB_DATA
SMBUS

ACTLED# — LED0
LINKLED — LED1
LED2
LED

+3.3V_LAN
R644 10K_4
R646 10K_4
JTAG_TDI, JTAG_TDO, JTAG_TMS, JTAG_TCK
JTAG

LAN_XTALO — XTAL_OUT
LAN_XTALI — XTAL_IN
TEST_EN
RBIAS
R640 1K_4
R635 3.01K/F_4
82579LM/LC

VCT — 6
RSVD_VCC3P3_1, RSVD_VCC3P3_2 — R653 4.7K_4, R650 4.7K_4 — +3.3V_LAN
VDD3P3_IN — 5
VDD3P3_OUT — 4 — +V3.3M_LAN_OUT
VDD3P3_15, VDD3P3_19, VDD3P3_29 — C730 0.1U/10V/X5R_4
VDD1P0_47, VDD1P0_46, VDD1P0_37 — +1.0V_LOM
VDD1P0_43
VDD1P0_11
VDD1P0_40, VDD1P0_22, VDD1P0_16, VDD1P0_8 — C724 0.01U/16V/X7R_4; C722 10U/10V/X5R_8; C723 *10U/10V/X5R_8
CTRL_1P0 — L37 4.7uH/510mA_12 — EC-QV-04
Close to CTRL_1P0 (PIN7)
VSS_EPAD — 49

Added CAP,Total = 20uF - 07/23
Rev1.2 - Intel 431786

+1.0V_LOM — R634 *0_6 — +1.05V_PCH

U36 / U35

U36: TRD0+ 1, TRD1- 3, GND 2, IO1, IO2, IO3, IO4, REF, 6 TRD0-, 5, 4 TRD1+ — CM1293A-04SO
U35: TRD2+ 1, TRD3- 3, GND 2, IO1, IO2, IO3, IO4, REF, 6 TRD2-, 5, 4 TRD3+ — CM1293A-04SO

LAN_DISABLE# is active low.

LAN_XTALO_R / LAN_XTALO

LAN_XTALO_R — R639 0_4 — LAN_XTALO
Y7 25MHZ: 1, 2 — LAN_XTALI
C729 33P/50V/NPO_4
C728 33P/50V/NPO_4

EC-B-33

SMBUS address 0XC8

+3.3V_LAN
R643 2.2K_4
R638 2.2K_4
+3V_S5
(10) SMB_DATA_ME0 — Q47 2N7002 — SMB_DAT_ME0_R
(10) SMB_CLK_ME0 — Q46 2N7002 — SMB_CLK_ME0_R

Tramsformer

U33 NS892405
TRD0- 12, TRD0+ 11 — TD4-, TD4+ — MX4-, MX4+ — LAN_MX0-, LAN_MX0+
C379 0.1U/10V/X5R_4
TCT4 — MCT4 — LAN_MCT0 — R307 75/F_4 — LANCT3
TRD1- 9, TRD1+ 8 — TD3-, TD3+ — MX3-, MX3+ — LAN_MX1-, LAN_MX1+
C380 0.1U/10V/X5R_4
TCT3 — MCT3 — LAN_MCT1 — R308 75/F_4
TRD2- 6, TRD2+ 5 — TD2-, TD2+ — MX2-, MX2+ — LAN_MX2-, LAN_MX2+
C384 0.1U/10V/X5R_4
TCT2 — MCT2 — LAN_MCT2 — R309 75/F_4
TRD3- 3, TRD3+ 2 — TD1-, TD1+ — MX1-, MX1+ — LAN_MX3-, LAN_MX3+
C382 0.1U/10V/X5R_4
TCT1 — MCT1 — LAN_MCT3 — R310 75/F_4
C383 1U/10V/X5R_6
Place near to Transformer

R306 1M_6
C711 10P/3KV/NPO_18

EC-B-27

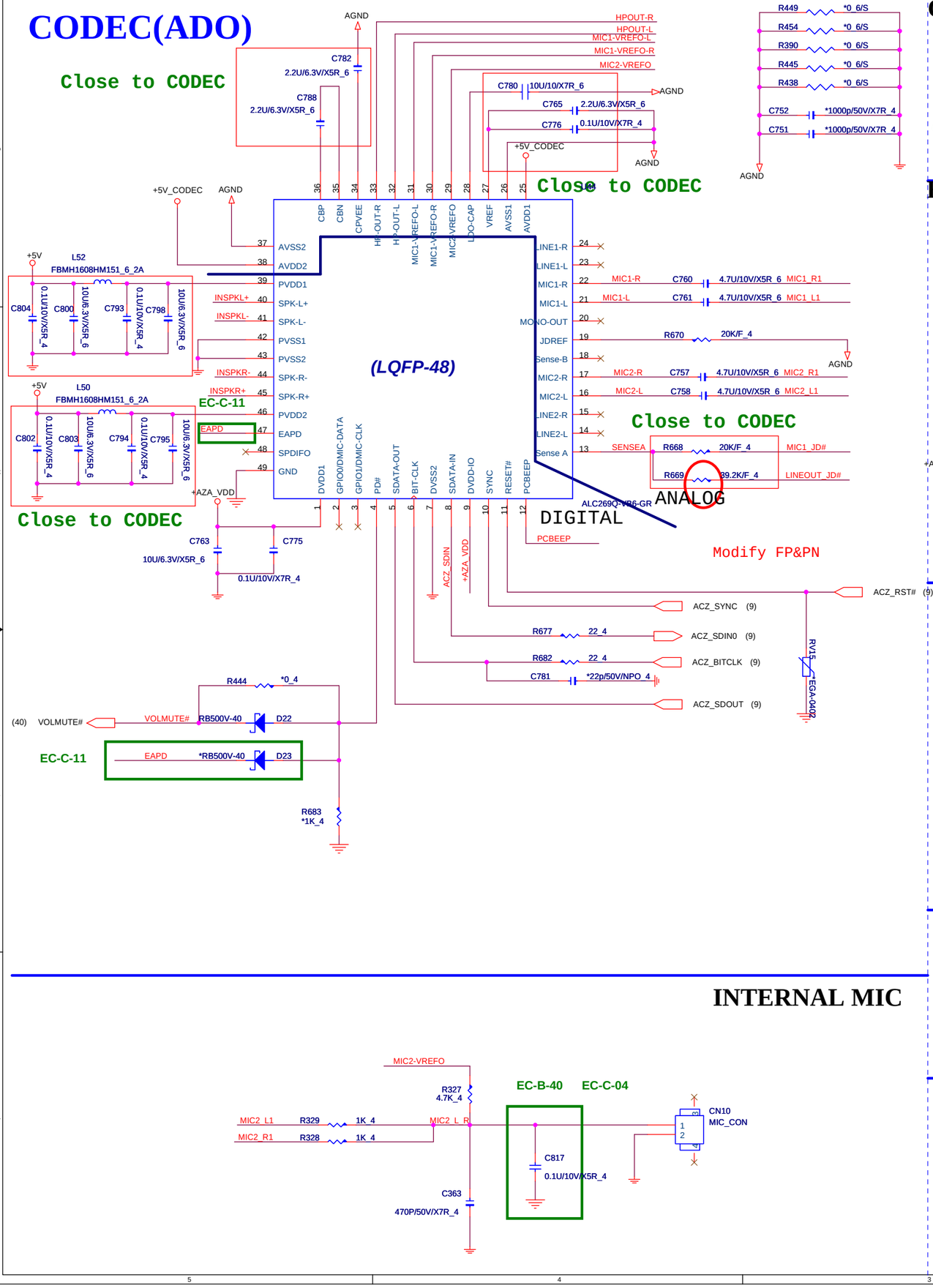
RJ45 Connector

EMI:close RJ45
C719 *0.1U/10V/X5R_4@NC
CN19 100073FR012S176ZL
+3.3V_LAN — R630 150/F_4 — LAN_YLED
ACTLED#
LAN_MX0+, LAN_MX0-, LAN_MX1+, LAN_MX2+, LAN_MX2-, LAN_MX1-, LAN_MX3+, LAN_MX3-
+3.3V_LAN — R628 150/F_4 — LAN_GLED, LINKLED
C816 *0.1U/10V/X5R_4
C815 *0.1U/10V/X5R_4
C709 *0.1U/10V/X5R_4@NC
EMI:close RJ45

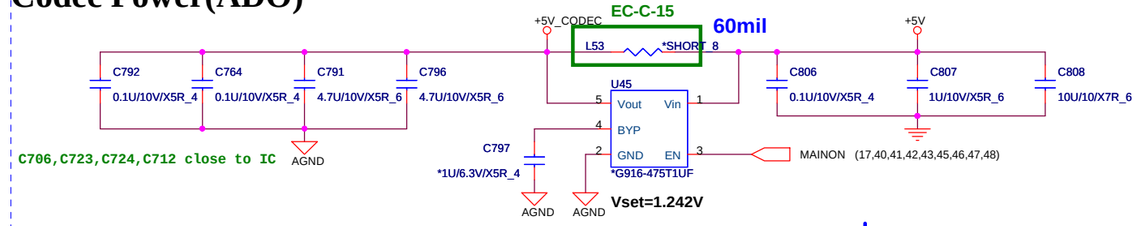
EC-B-40

PROJECT : LL3A		
Quanta Computer Inc.		
Size: Custom	Document Number: LAN(82577LM)	Rev: 1E
Date: Tuesday, January 04, 2011	Sheet 25 of 53	

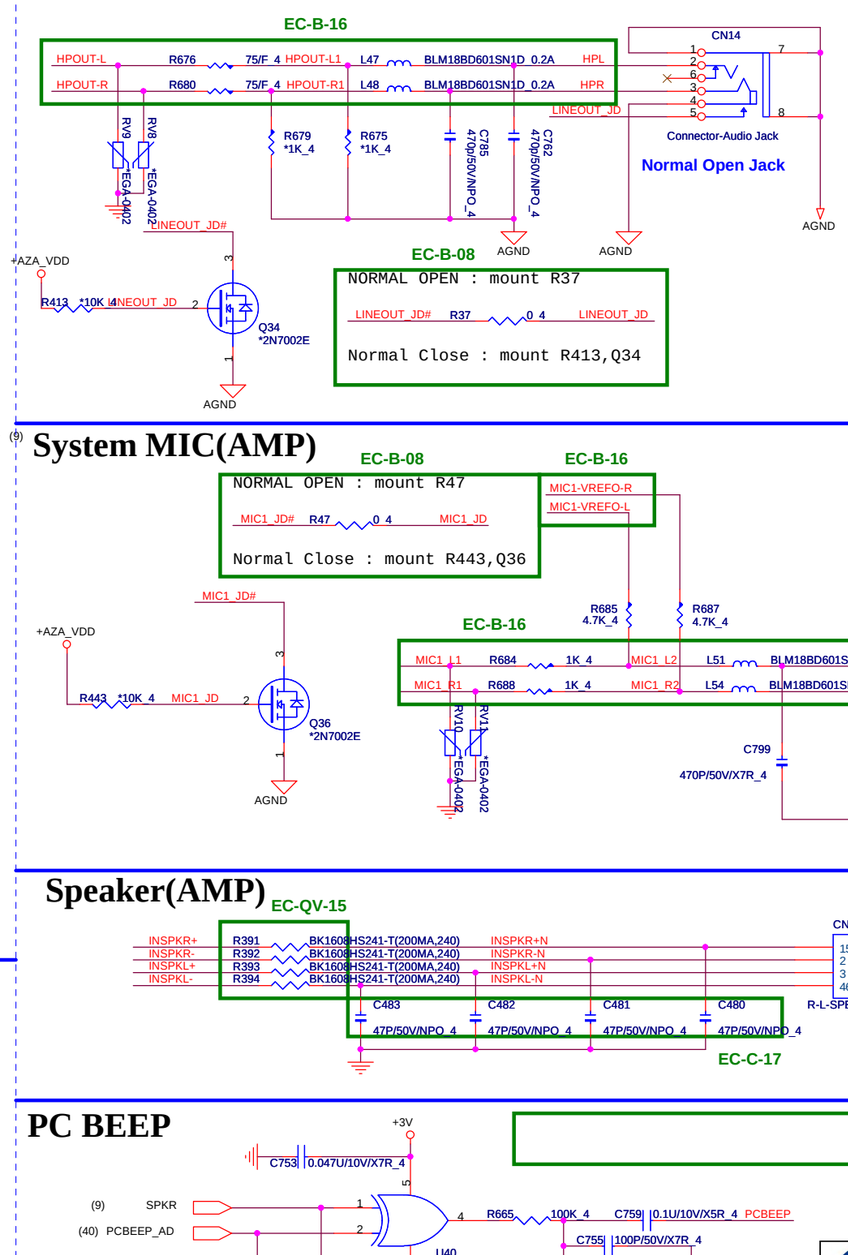
CODEC(ADO)



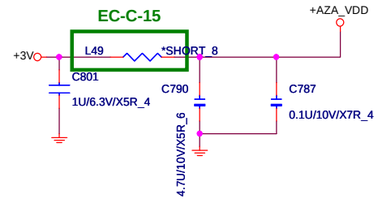
Codec Power(ADO)



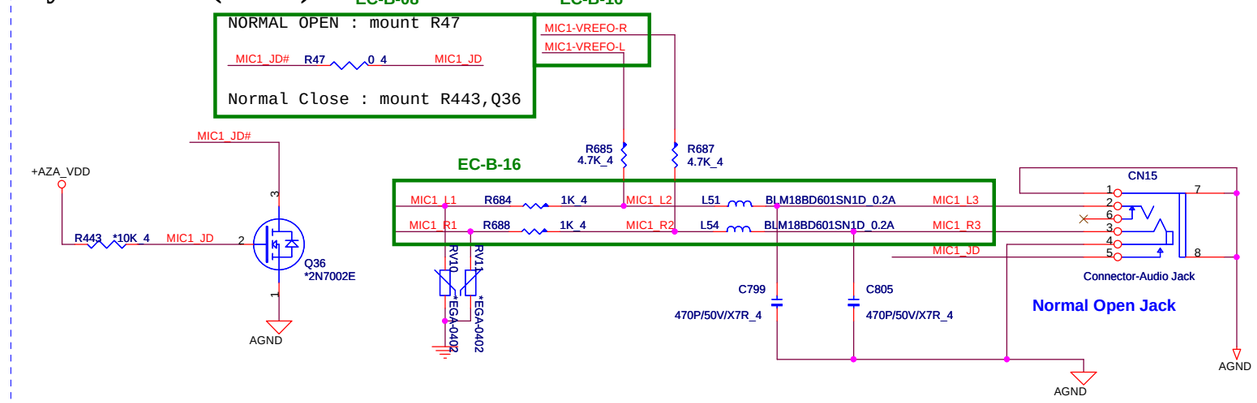
Earphone(AMP)



HDA Power(ADO)



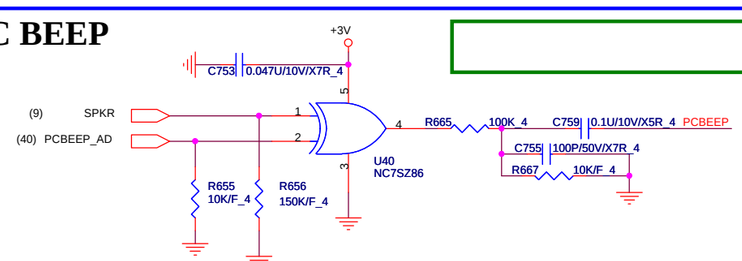
System MIC(AMP)



Speaker(AMP)

INTERNAL MIC

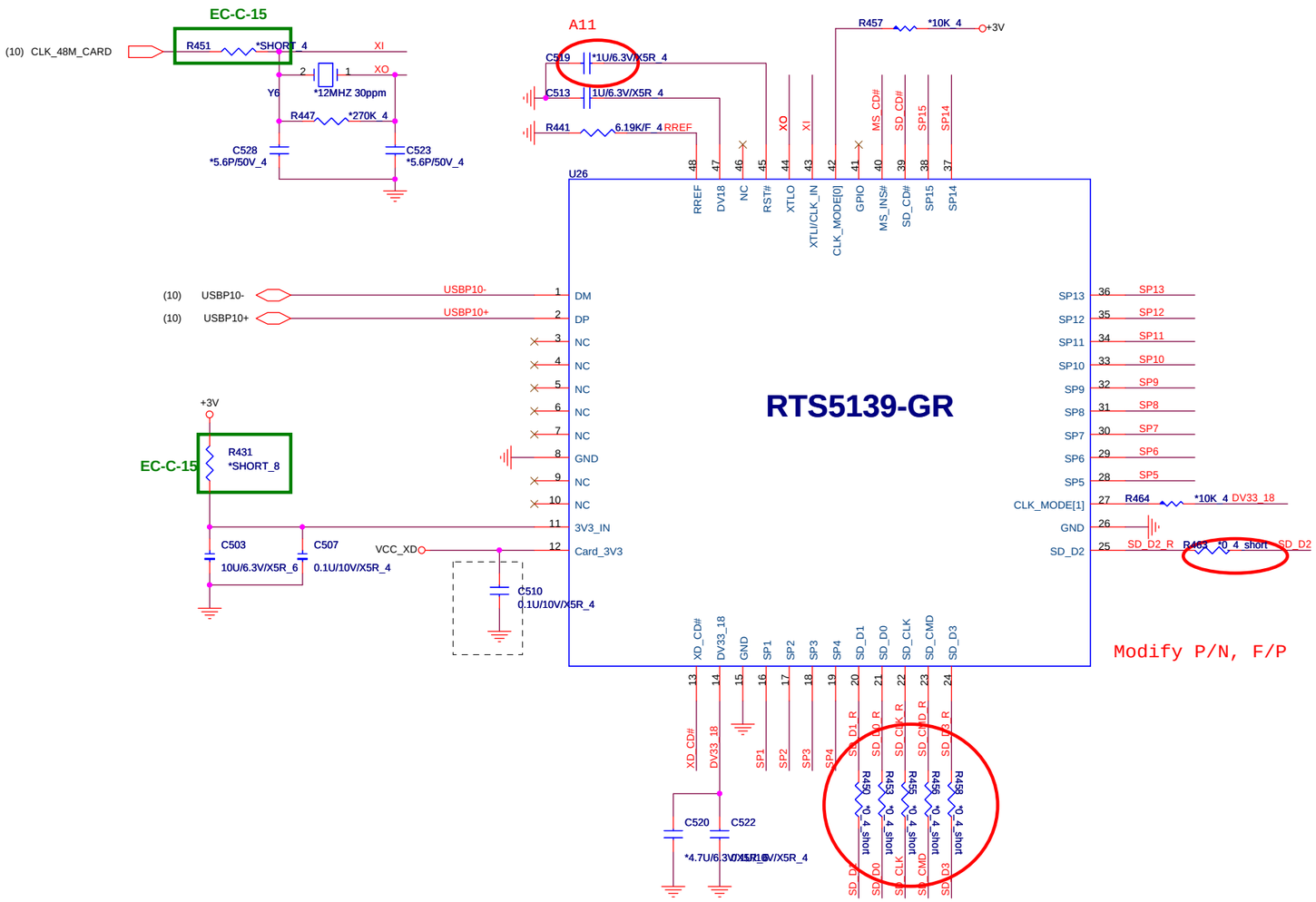
PC BEEP



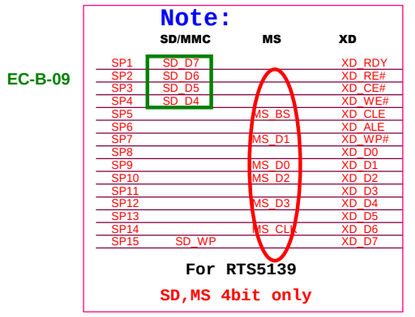
PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AL269/MIC/Line out	1A
Date: Tuesday, January 04, 2011	Sheet 26 of 53	

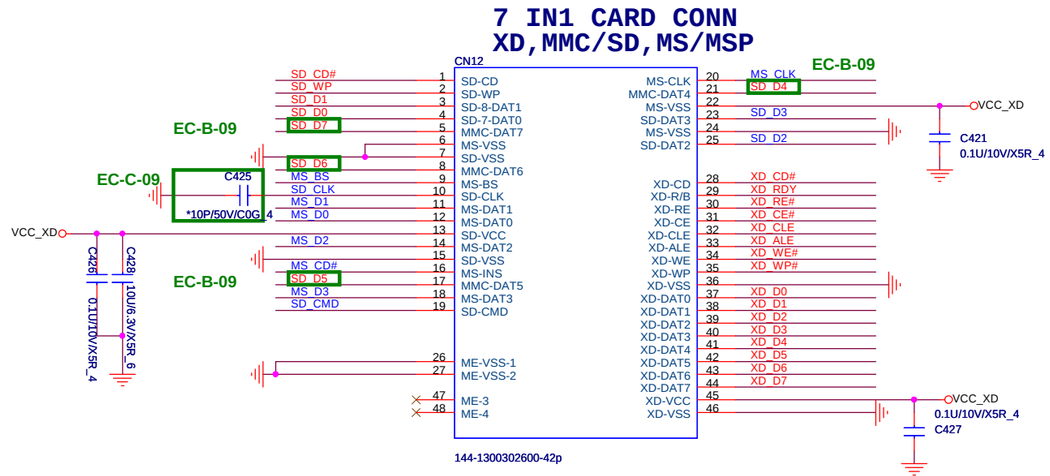
Clock Mode strap	R9287	R9307
48MHz	X	X
24MHz	X	O
12MHz	O	X
12MHz (Crystal)	O	O



Modify P/N, F/P

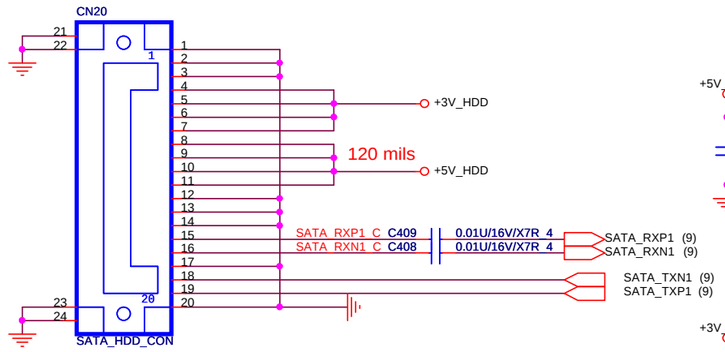


EC-B-09

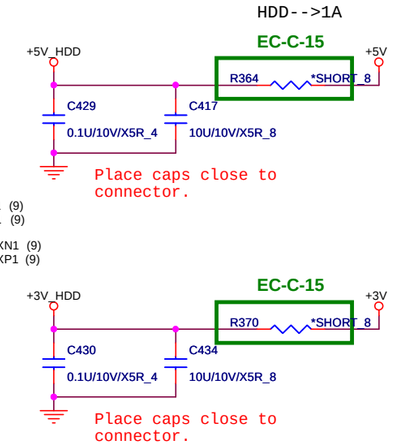


PROJECT KL5A			
Quanta Computer Inc.			
Size: Custom	Document Number: Card Reader (RTS5159)		Rev: 1A
Date: Friday, November 19, 2010	Sheet 27 of 53		

SATA HDD Connector.

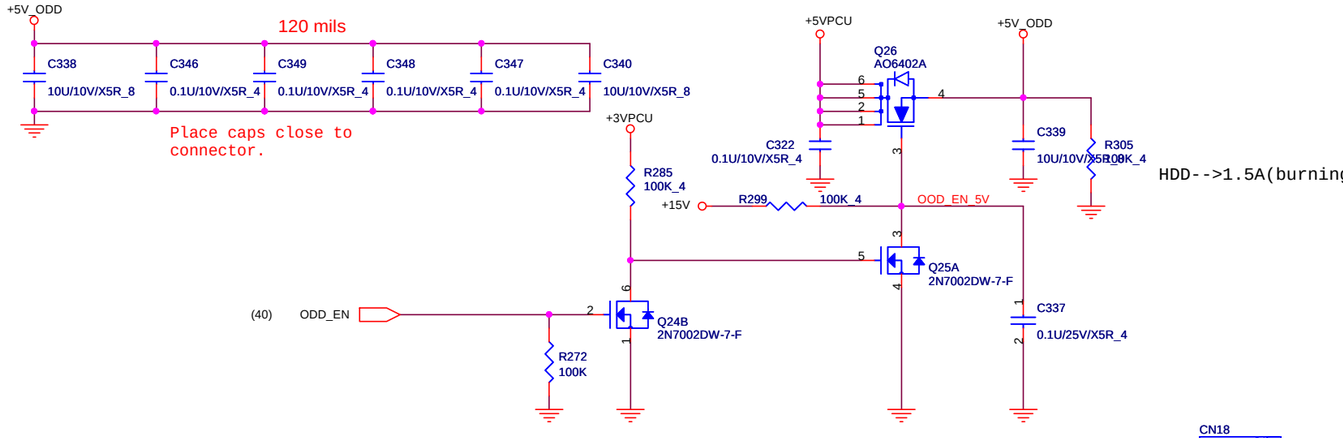


Modify PN&FP(LL7 OK)

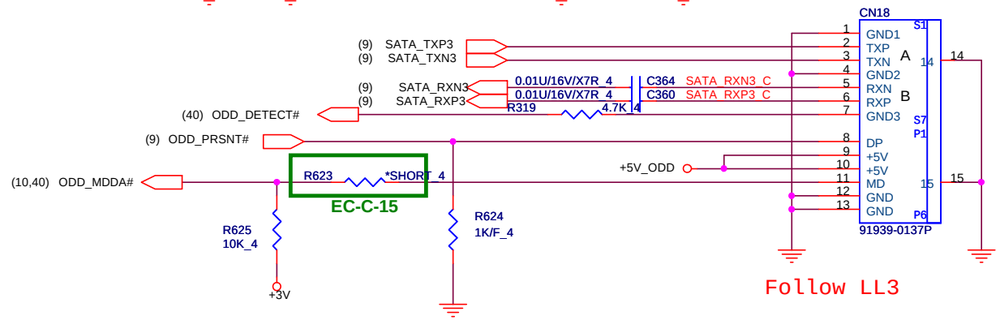


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

SATA ODD Connector.



EC-B-10

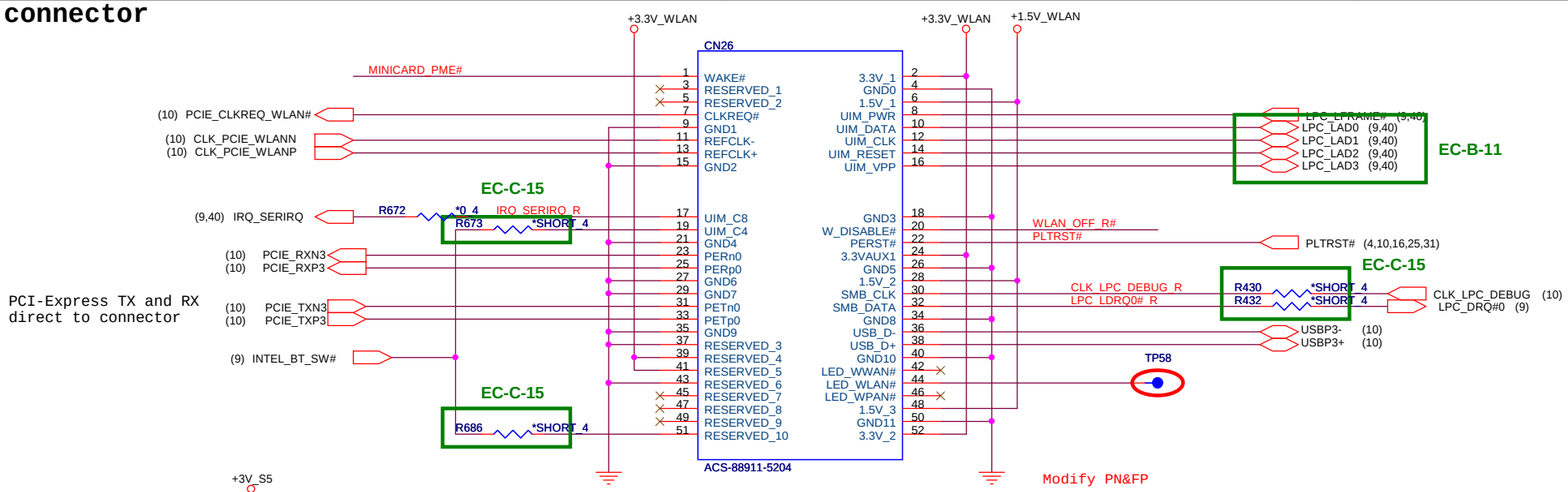


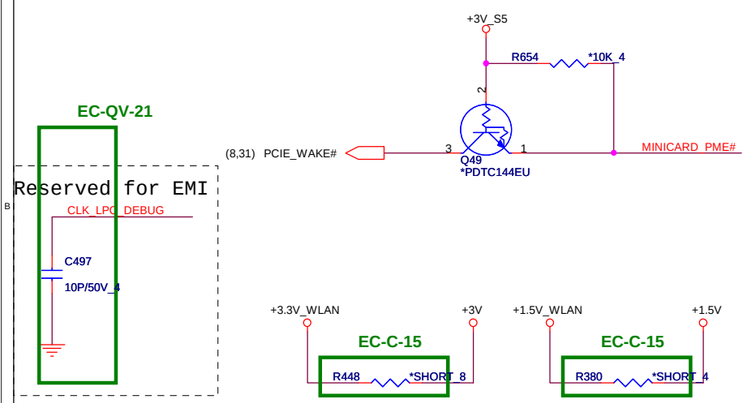
Follow LL3

PROJECT KL5A
Quanta Computer Inc.

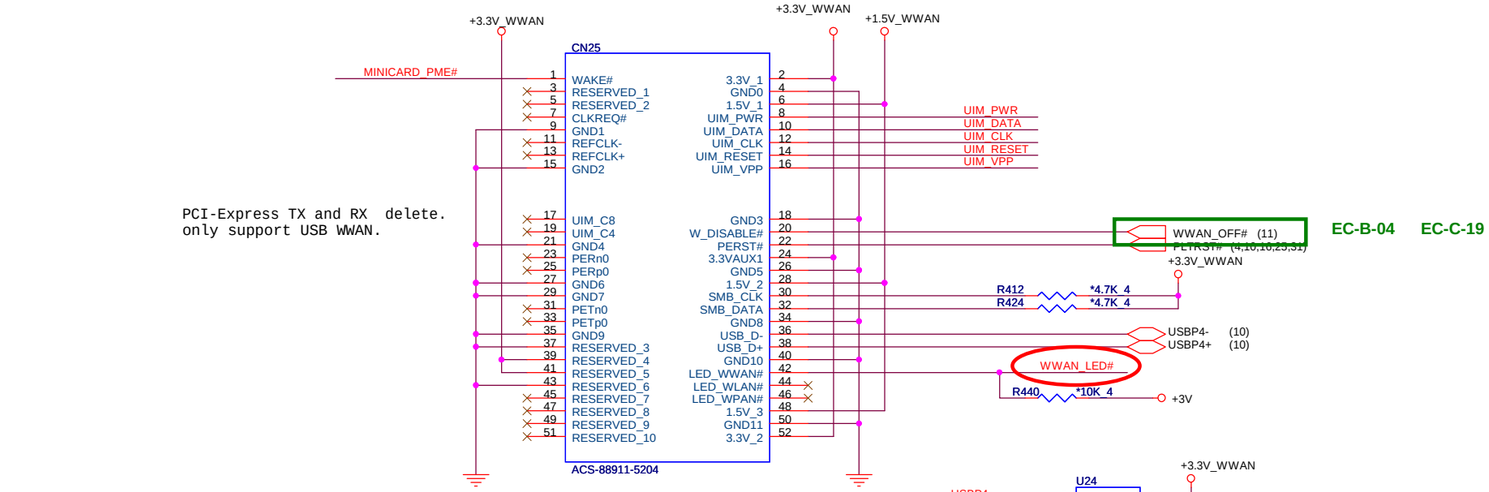
Size	Document Number	Rev
Custom	SATA HDD/ESATA/CD-ROM	1A
Date: Tuesday, January 04, 2011	Sheet 28 of 53	

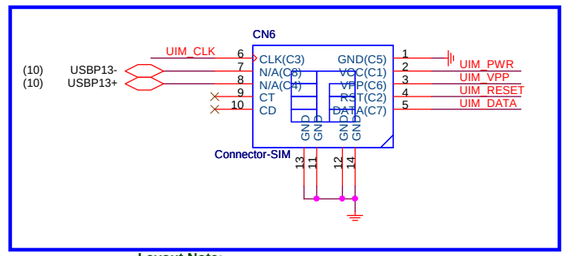
MiniCard WLAN connector

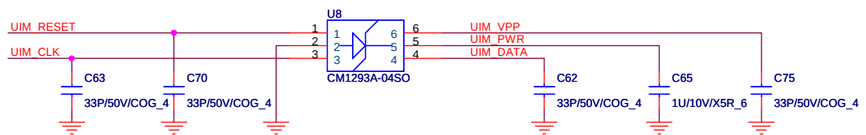


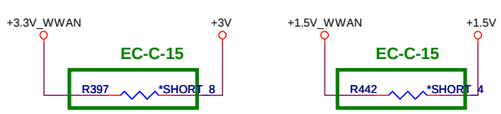


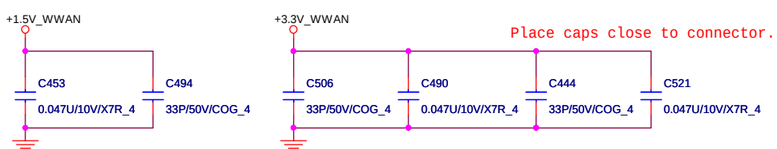
MiniCard WWAN (Reserved for KL9)











PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-Card (WLAN/WWAN)	1A
Date: Wednesday, January 05, 2011	Sheet 29 of 53	

Mini PCI-E Card 3 SSD

(12,29,38,41,43) +1.5V
(8,9,10,11,12,14,15,17,22,23,24,26,27,28,29,31,36,37,38,40,41,42,46,47,48,49) +3V

32

EC-B-13

+3.3V_SSD

+3.3V_SSD

+1.5V_WIMAX

CN24

1	WAKE#		3.3V_1	2	
3	RESERVED_1		GND0	4	
5	RESERVED_2		1.5V_1	6	
7	CLKREQ#		UIM_PWR	8	
9	GND1		UIM_DATA	10	
11	REFCLK-		UIM_CLK	12	
13	REFCLK+		UIM_RESET	14	
15	GND2		UIM_VPP	16	
17	UIM_C8		GND3	18	
19	UIM_C4		W_DISABLE#	20	
21	GND4		PERST#	22	
23	PERn0		3.3VAUX1	24	
25	PERp0		GND5	26	
27	GND6		1.5V_2	28	
29	GND7		SMB_CLK	30	
31	PETn0		SMB_DATA	32	
33	PETp0		GND8	34	
35	GND9		USB_D-	36	
37	RESERVED_3		USB_D+	38	
39	RESERVED_4		GND10	40	
41	RESERVED_5		LED_WWAN#	42	
43	RESERVED_6		LED_WLAN#	44	
45	RESERVED_7		LED_WPAN#	46	
47	RESERVED_8		1.5V_3	48	
49	RESERVED_9		GND11	50	
51	RESERVED_10		3.3V_2	52	

ACS-88911-5204

(9) SATA_RXP0
(9) SATA_RXN0

0.01U/16V/X7R_4 C756 SATA_RXP0_C
0.01U/16V/X7R_4 C754 SATA_RXN0_C

(9) SATA_TXN0
(9) SATA_TXP0

USBP12- USBP12- (10)
USBP12+ USBP12+ (10)

(11) SDD_DA_DSS
(11) SSD_DETECT#

EC-B-12

+1.5V_WIMAX

Place caps close to connector.

C736 *0.01U/16V/X7R_4
C784 *0.1U/10V/X5R_4
C783 *10U/6.3V/X5R_8

EC-B-12

+3.3V_SSD

Place caps close to connector.

C739 0.1U/10V/X5R_4
C778 0.047U/10V/X7R_4
C779 0.1U/10V/X5R_4
C777 0.047U/10V/X7R_4
C774 4.7U/10V/X5R_8

+3.3V_SSD +3V

EC-C-15

R384 *SHORT_8

+1.5V_WIMAX +1.5V

EC-C-15

R366 *SHORT_4

PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI Card (SSD)	1E
Date: Tuesday, January 04, 2011	Sheet 30 of 53	

USB30_SMI#
R712 *0/J_4
D28 RB500V-40
(10) USB30_EXT_SMI#
EC-QV-17

+3.3VAUX
EC-C-13
R420 10K/F_4
R419 10K/F_4
R418 10K/F_4
R637 10K/F_4
R657 10K/F_4
R704 10K/F_4
R705 *10K/F_4
PCIE_WAKE#
USB30_SMI#
JTAGCK
GPIO3
LOPWREN#
RMTWKEN#
EC-C-13

+3.3VAUX
R423 10K/F_4
R422 10K/F_4
TP30
TP29
SMDAT
SMCLK
For debug only.
Don't connect to
system SMBus

+3.3VAUX
OVCUR1#
OVCUR3#
OVCUR4#
OVCUR2#
R417 10K_4
R416 10K_4
EC-QV-17

SPI Flash ROM
P3V3_USB30
R396 10K/F_4
U22
SPICS# SPISCLK SPISI SPISO
CE# SCK SI SO WP# HOLD# VDD VSS
MX25L512MC-12G
8/13 P/N: AKE34ZN0501

ESD
U20
USB30_RX1- USB30_RX1+ USB30_TX1- USB30_TX1+
Z1 Z2 GND Z3 Z4 NC NC VCC NC NC
USB30_RX1- USB30_RX1+ USB2PWR USB30_TX1- USB30_TX1+
*RClamp0544.TBT
msop10-4_9-5

Co-layout USB
PORT for 2.0&3.0
USB 3.0 function reserved

EC-C-13
USB3.0 : Install
USB2.0 : Remove
USB20_DM1 USB20_DP1
R371 0R_4
R365 0R_4
USB0_FB- USB0_FB+

USB30_RX1- USB30_RX1+ USB30_TX1- USB30_TX1+
TP20 TP21 TP22 TP23
EC-C-14

	USB3.0	USB2.0
R651	No-ASM	No-ASM
R649	No-ASM	No-ASM
CML4	No-ASM	ASM

EC-B-27
R651 *0_4
CML4
*DLW21SN121SQ2L
R649 *0_4
(10) USBP8-
(10) USBP8+
USB0_FB-
USB0_FB+
D27 D26
BC5V0U1BZ01 BC5V0U1BZ01

EC-C-13
USB2PWR
CN23
USB0_FB- USB0_FB+ USB30_RX1- USB30_RX1+ USB30_TX1- USB30_TX1+
VBUS D- D+ GND RX- RX+ GND TX- TX+
USB2.0/3.0 CONN

U21
VL800 / VL801 QFN88
VL800 4PORT
VL801 2PORT
VDD VSTX1+ VSTX1- VCCA10SSRX1 SSRX1+ SSRX1- VCCA33SS1 USBHP1+ USBHP1- VCCA33SS1 SSTX2+ SSTX2- VCCA10SSRX2 SSRX2+ SSRX2- VCCA33SS2 USBHP2+ USBHP2- VCCA33SS2 VCCA10SSM SSXI SSXO
VSUSUSB SSREXT VCCA10SSM SSTX2+ SSTX2- VCCA10SRX3 SSRX3+ SSRX3- VCCA33SS3 USBHP3+ USBHP3- VCCA33SS3 GND SSTX4+ SSTX4- VCCA10SRX4 SSRX4+ SSRX4- VCCA33SS4 USBHP4+ USBHP4- VCCA33SS4 GND_PAD
1.0VL 1.0VE +3.3VAUX
USB30_TX1+ USB30_TX1- C486 C484 0.1U/16V_4
USB30_RX1+ USB30_RX1- R395 R389 0R_4
U3TXDP1 U3TXDN1 U3RXDP1 U3RXDN1
USB20_DP1 USB20_DM1
SSXI SSXO SSREXT

Near PCIEx Slot
VSUS33 USBHPE2# USBHPE3# USBHPE4# SPISO SPISI SPISCLK SPICS# VDD VCCA33PEXTX PEXTX0- PEXTX0+ VCCA33PEXM PEXRX0- PEXRX0+ VCCA33PEXRX PEXCLK- PEXCLK+ VCCA33REG12 PEXREXT VCCA33REG25 VDD
PWREN2 PWREN3 PWREN4 SPISO SPISI SPISCLK SPICS#
TP28 TP27 TP26
PCIE_RXN5_C PCIE_RXP5_C 0.1U/16V_4 C479 C477
PCIE_RXN5 (10) PCIE_RXP5 (10)
PCIE_TXN5 (10) PCIE_TXP5 (10)
CLK_PCIE_USB30N (10) CLK_PCIE_USB30P (10)
EC-B-14

PLTRST_PCIE_N_USB 10K_4 R421
PLTRST# (4,10,16,25,29)
C828 *0.1U/10V/X5R_4
EC-QV-17
EC-C-13

EC-C-13 C830 *0.1U/10V/X5R_4

+5V_S5
(32,40) USB_ON
U39
VIN1 VIN2 EN GND OUT3 OUT2 OUT1 OC
C734 1U/10V/X5R_6
G547G1P81U(MSOP-8)
80 mils (Iout=2A)
R642 0_4
USB3.0 : Install
USB2.0 : Remove
OVCUR2#
To USB3.0 IC
R641 *0_4
USB3.0 : Remove
USB2.0 : Install
USB_OC2# (10)
To PCH
C750 470P/50V/X7R_4
C749 0.1U/10V/X5R_4
C748 150U/6.3V_3528
USB2PWR

Mount R9969 with VL801
Mount R9970 without VL801

EC-QV-17
PLTRST_PCIE_N_USB R713 0_4
C952 *0.1U/10V/X5R_4
+3.3VAUX
R707 100K/F_4
Q58 ME2303T1
C829 1U/6.3V_4
+3.3VAUX
R714 *100K/F_4
Q61 *ME2303T1
R719 100K/F_4
COREPWRDN
C953 *0.1U/10V_4

Remove LDO and connector
+1.05V_PCH to P1V05_SUS
+1.05V_PCH
P1V05_SUS
R374 0_8 0.6A

X'tal 25MHz EC-B-33 EC-C-13
27P/50V_4 C433 R372 0R_6 SSXI
Y5 25MHz/20pF/30ppm
27P/50V_4 C432 SSXO
BG625000486
XTL-5_3X3_2-3_8-1_2H
Crystal foot print must be reserved
in case 25MHz clock from clock
generator is not stable enough.

EC-C-13
From M/B
+3V_SUS +3.3VAUX
FB5 BLM18PG300SN1D
C509 4.7uF/6.3V_6
C512 0.1U/16V_4
C511 4.7uF/6.3V_6
C508 0.1U/16V_4

From M/B
+3V
FB4 BLM18PG300SN1D
C467 4.7uF/6.3V_6
C471 0.1U/16V_4
COREPWRDN
R716 *0_4
*ME2303T1
Q62
C950 *1U/6.3V_4
P3V3_USB30
C468 4.7uF/6.3V_6
C469 0.1U/16V_4
EC-QV-17

P1V05_SUS
From M/B
C447 4.7uF/6.3V_6
C440 0.1U/16V_4
FB3 BLM18PG300SN1D
P/N:CX11P300000
*ME2303T1
Q63
COREPWRDN R717 *0_4
C951 *1U/6.3V_4
1.0V
FB1 BLM18PG300SN1D
FB2 BLM18PG300SN1D
1.0VE
1.0VL
C435 0.1U/16V_4
C431 4.7uF/6.3V_6
C441 0.1U/16V_4
C448 4.7uF/6.3V_6
EC-QV-17

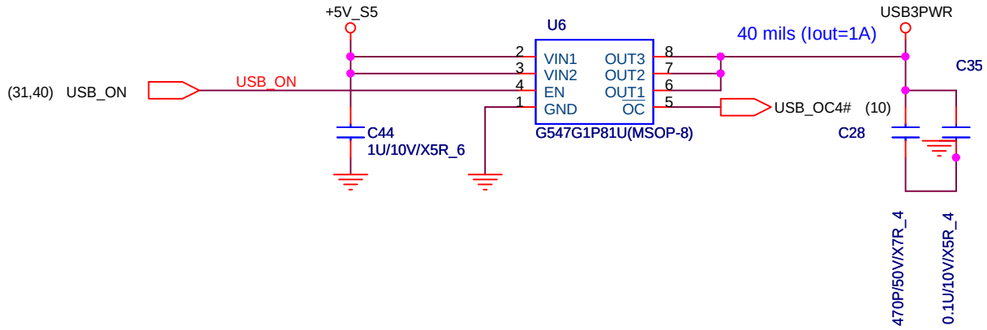
+3.3VAUX
C492 C502 C500 C501 C491 C489 C470 C445 C436 C439
1.0VL
C449 C498 C487 C499 C504 C505
P3V3_USB30
C451 C472 C475 C485 C476
+3.3VAUX
C446 C437 C473
1.0VE
C442 C438 C464 C478 C496
0.1U/16V_4

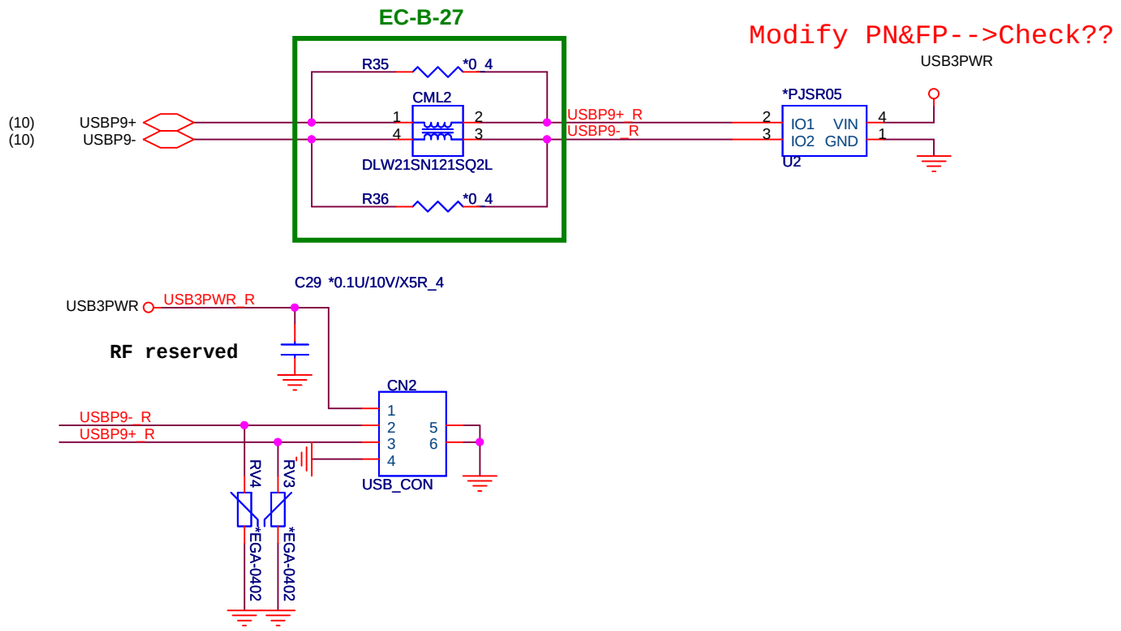
EC-C-13
+15V
R706 1M_4
Q54 2N7002K
(41) SUSON#
C826 *0.1U/50V/X7R_6
+3V_S5
Q53 AO6402A
+3V_SUS
C827 0.1U/10V/X7R_4

Power sequence for Host.
+3.3VSUS +3.3V Reset
+1.0VSUS +1.0V

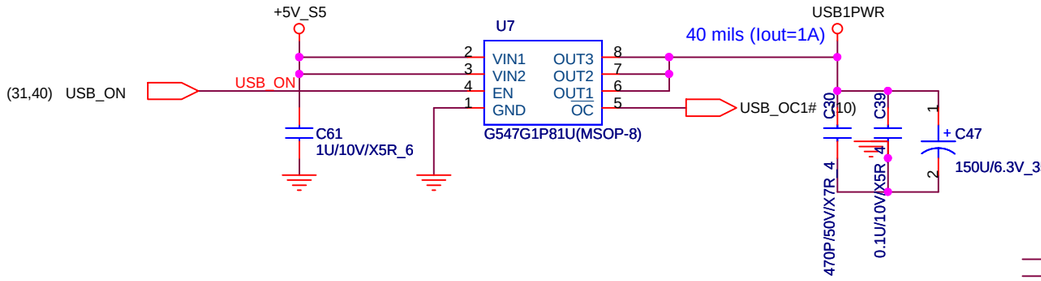
USB2.0*2

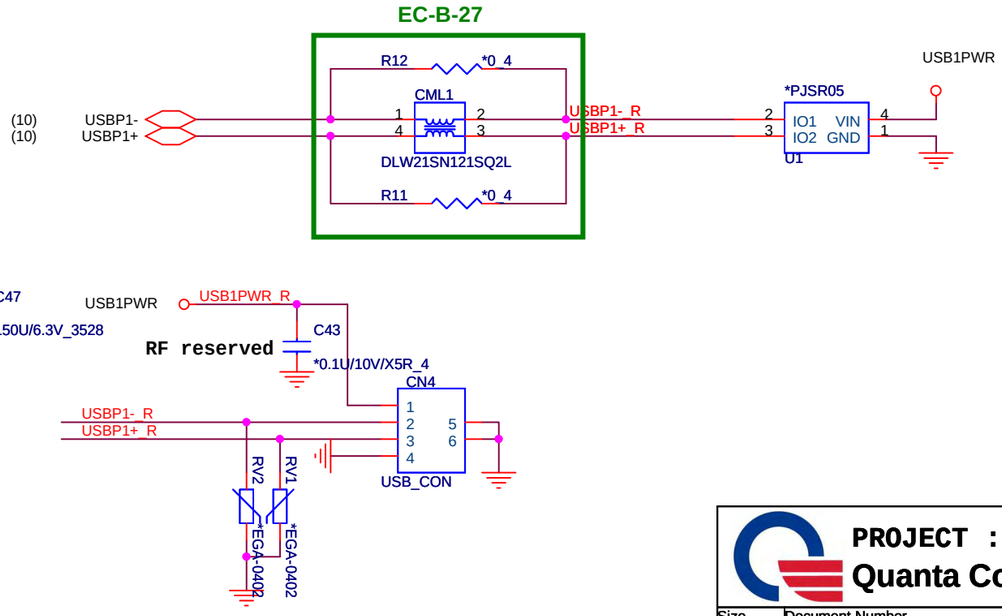
External (R side) USB*1





External (L side) USB*1





PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
B	MINI-Card (WLAN/WWAN)	1A

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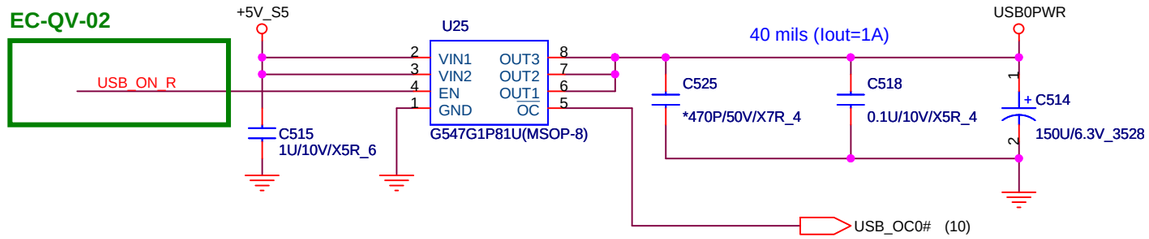
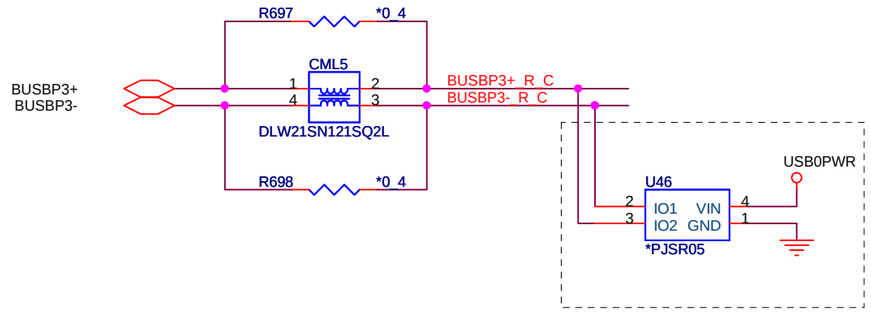
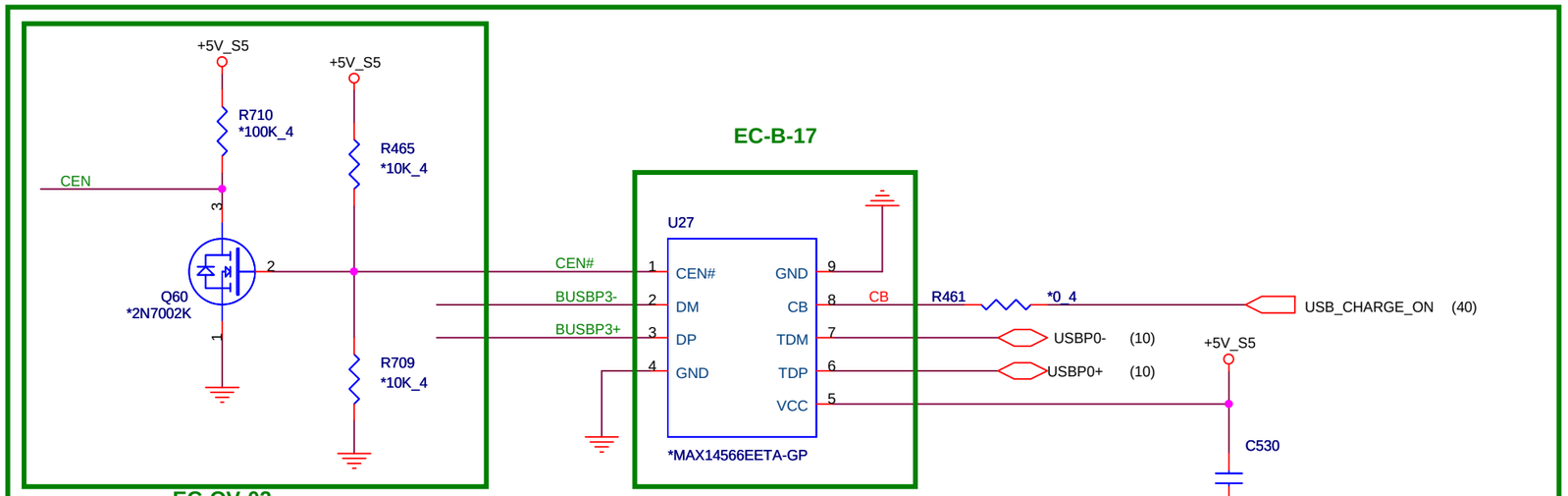
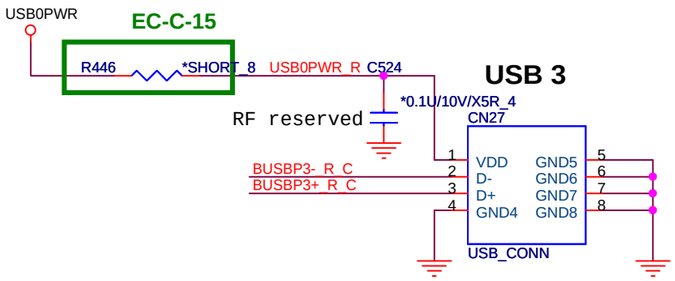
USB

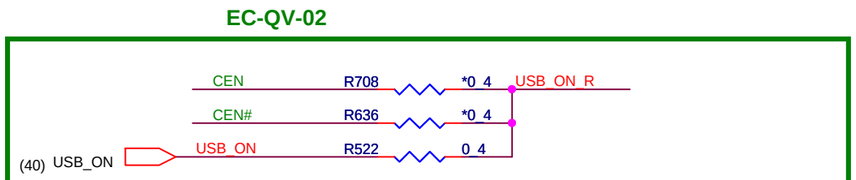




USB charger







Stuff for bypass USB charger

USBP0-	R689	0_4	BUSBP3-
USBP0+	R690	0_4	BUSBP3+

USB Charge Function

	R689	R690	R708	R522	State
Enable	X	X	V	X	
Disable	V	V	X	V	Default

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
B	USB Discharge	1A

Date: Tuesday, January 04, 2011 Sheet 33 of 53

G-SENSOR (3-Axial)

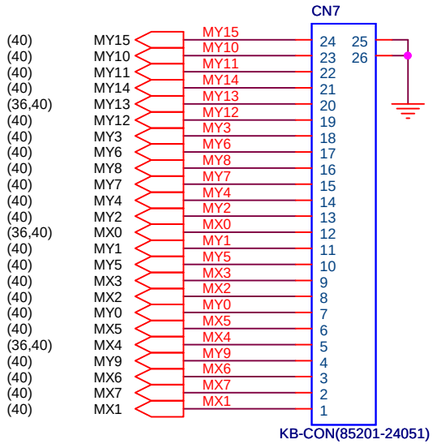
(8,9,10,11,12,14,15,17,22,23,24,26,27,28,29,30,31,36,37,38,40,41,42,46,47,48,49) +3V
(24,28,31,38,41,43,44,45) +15V

36

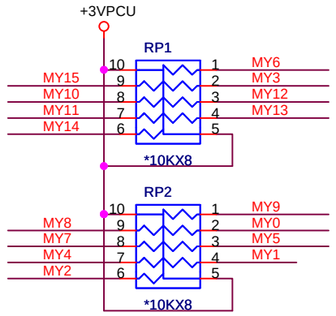
EC-B-18

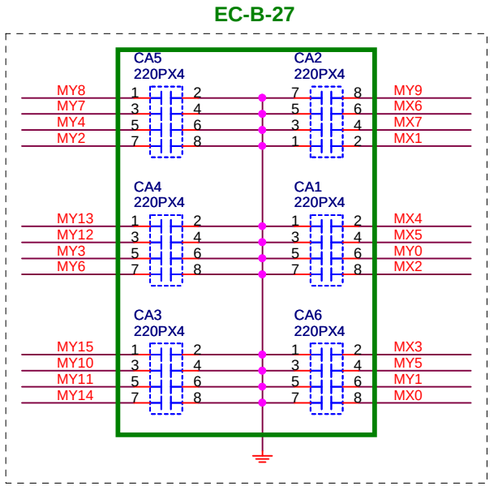
PROJECT : LL3A Quanta Computer Inc.		
Size Custom	Document Number G-SENSOR	Rev 1E
Date: Tuesday, January 04, 2011	Sheet 34 of 53	

KEYBOARD



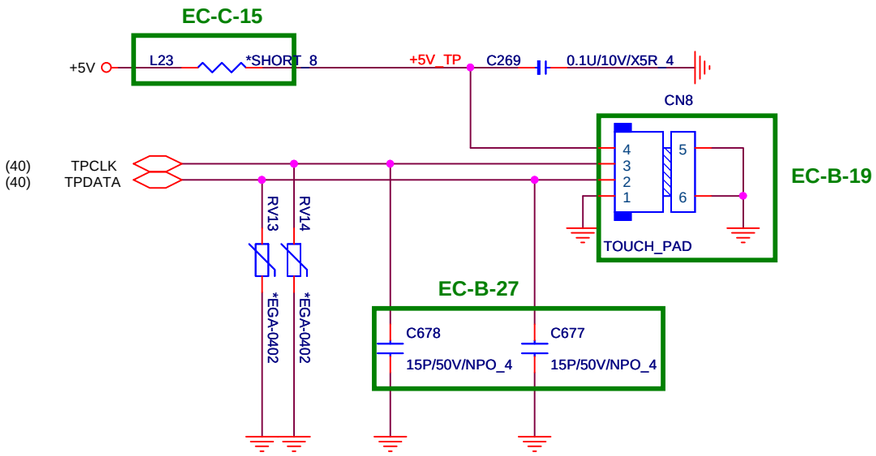
Follow LL3 KB





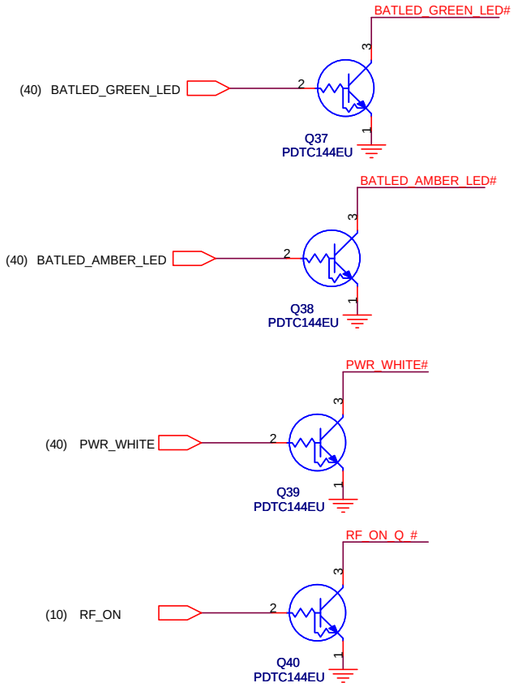
For EMI request

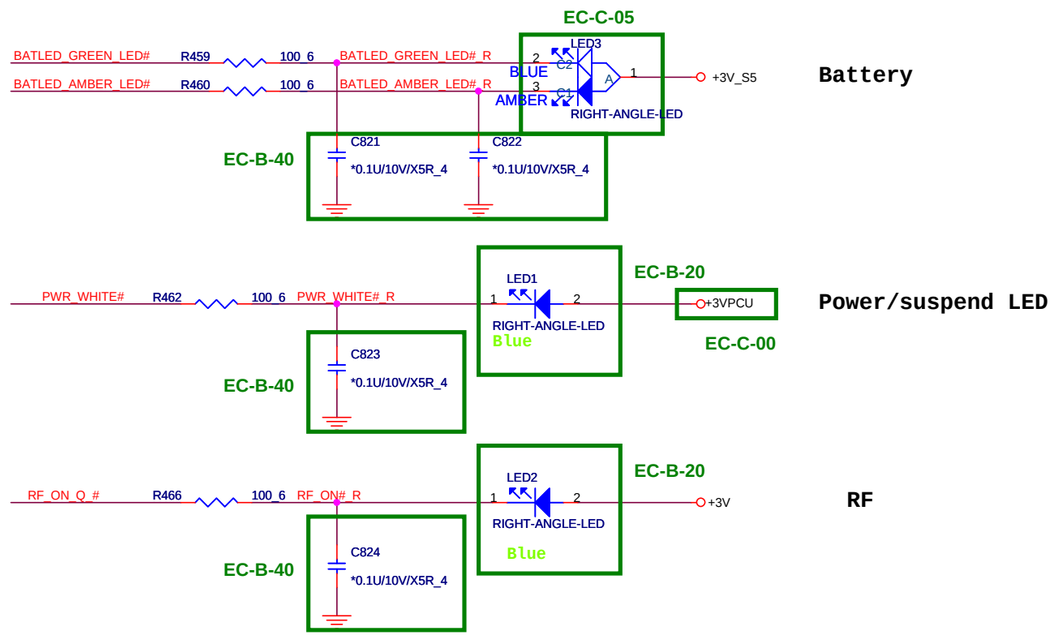
Touch pad



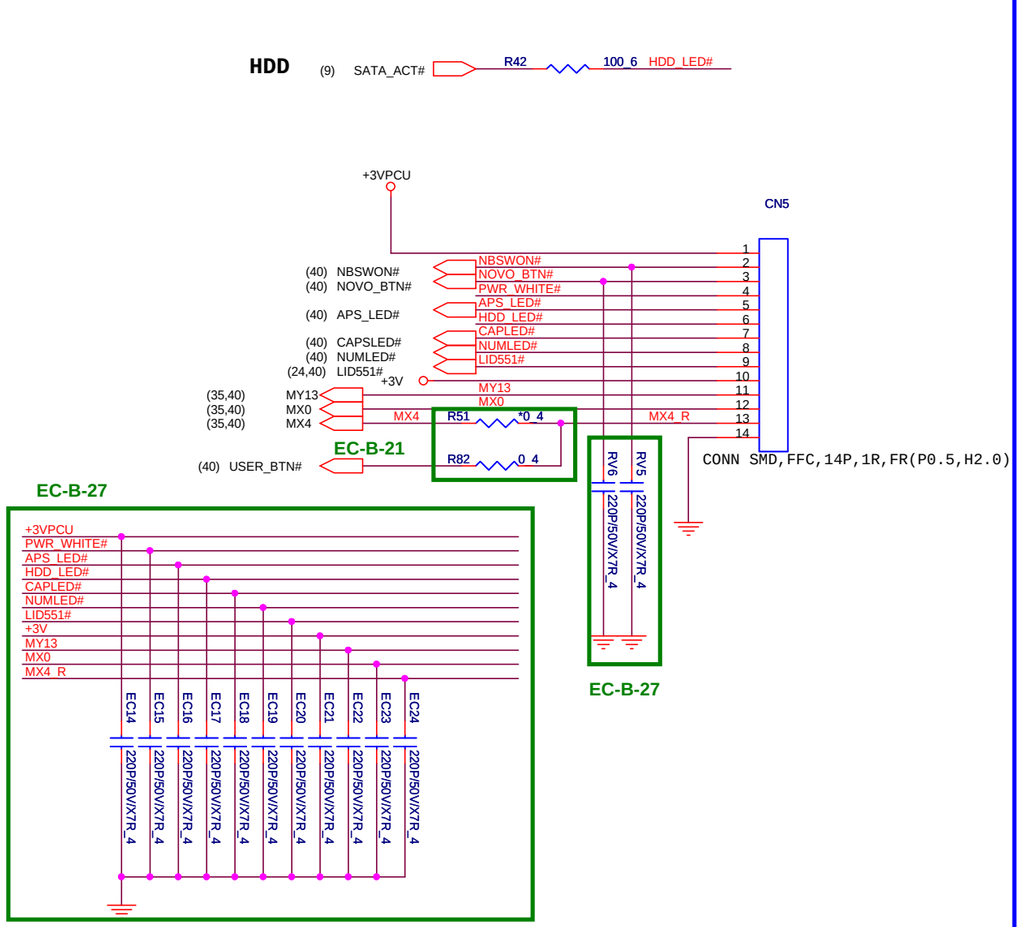
PROJECT KL5A Quanta Computer Inc.		
Size: Custom	Document Number: K/B, T/P	Rev: 1A
Date: Tuesday, January 04, 2011	Sheet 35 of 53	

POWER / Battery /RF LED

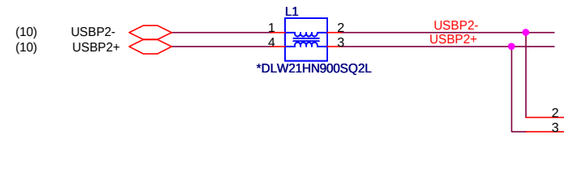


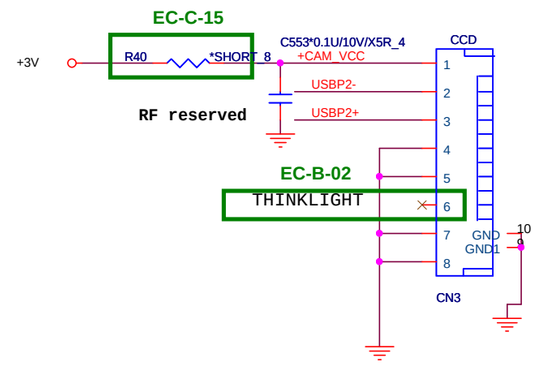


B to B connector



CAMERA & Keyboard light





PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	B TO B CON/LED/CCD	1A
Date: Tuesday, January 04, 2011	Sheet 36 of 53	

FAN CONTROL

NOTE:
Place C625 near Q37

NOTE:
Place C623 near Q38

NOTE:
Place C624 near U48

NOTE:
Place C627 near Q39

NOTE:
Place C626 near U48

Q45
SST3904

C716
*100P/50V/X7R_4

DDR3

Q52
SST3904

C789
*100P/50V/X7R_4

C211
2200P/50V/X7R_4

WLAN-ONFI

R214
2.05K_4

R133
*0_4

R155
*0_4

R226
6.8K/F_4

EC-C-15

+5V

R60
*SHORT_8

+5V_FAN

C59
1U/10V/X5R_6

C55
0.1U/10V/X5R_4

+3V

R196
10K_4

R210
10K_4

R206
10K_4

R207
10K_4

R230
10K_4

R229
10K_4

+5V

R237
10K_4

EC-B-29

CN16

FAN_PWM
FANSIG
+5V_FAN
FAN_CON

D8
RB500V-40

Q16
2N7002

MB_CLK1 (10,17,40)

Q17
2N7002

MB_DATA1 (10,17,40)

Q19
2N7002

SYS_SHDN-1#

SYS_SHDN# (17,44,49)

D7
*RB500V-40

VGA_OVT# (40)

MB_ALRET#

R183
*0_4

TEMP_ALERT# (11,40)

U13

GND
DP2/DN3
DN2/DP3
TRIP_SET
SHDN_SEL
GND
PWM
TACH
SMCLK
SMDATA
SYS_SHDN#
ALERT#
GPIO2
GPIO1
VDD
DP
DN

EMC2103-2

C686
*100P/50V/X7R_4

SST3904
Q42

CPU

C197
2200P/50V/X7R_4

R179
22_4

+3V_FAN

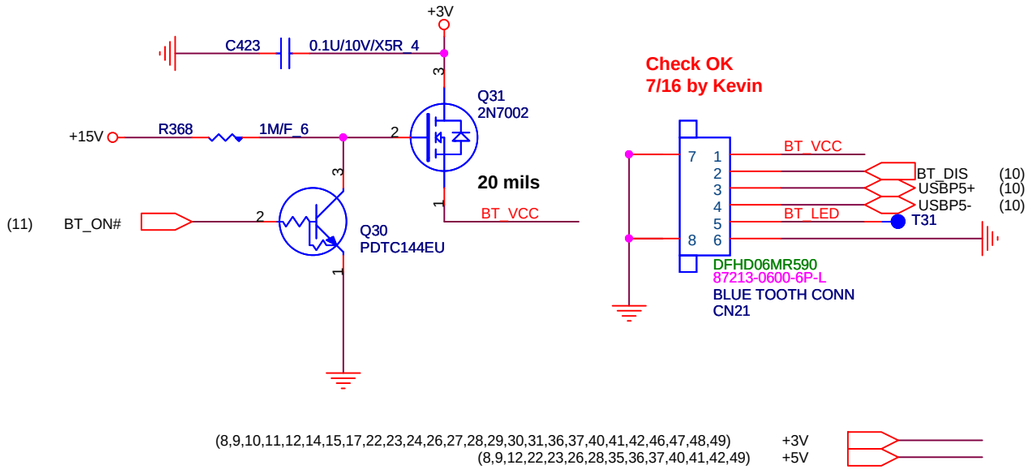
C196
0.1U/10V/X5R_4

RV7
*EGA-0402

Size B	Document Number FAN /THERMAL		Rev 1A
Date: Tuesday, January 04, 2011		Sheet 37 of 53	

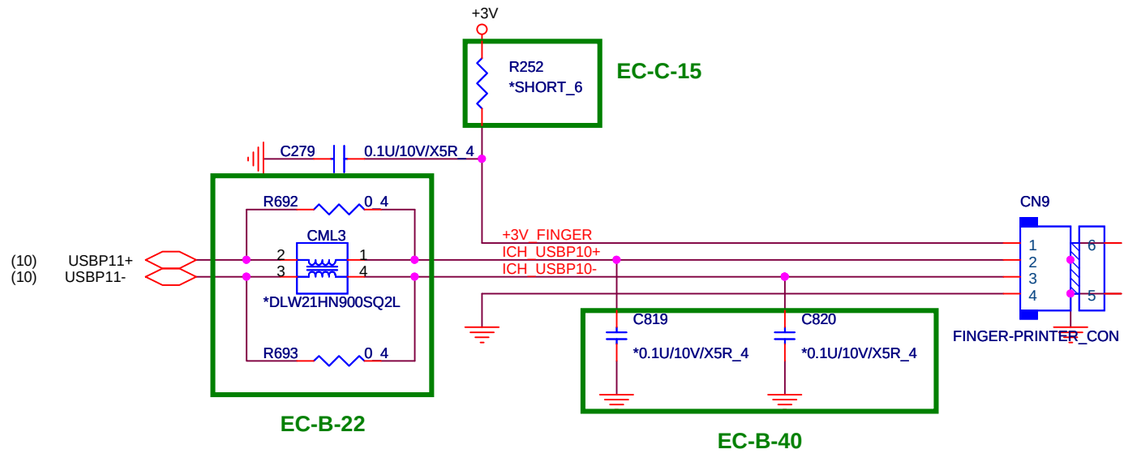
PROJECT KL5A
Quanta Computer Inc.

BLUETOOTH



FINGER PRINTER

34

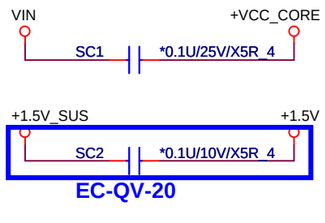


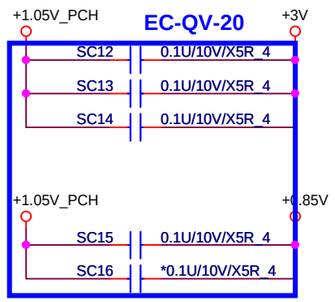
TPM

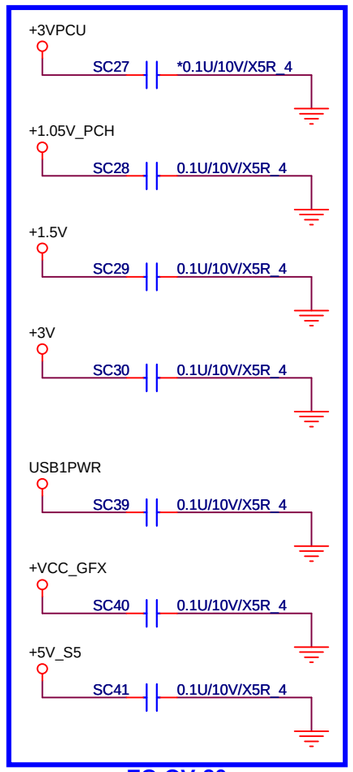
EC-B-23

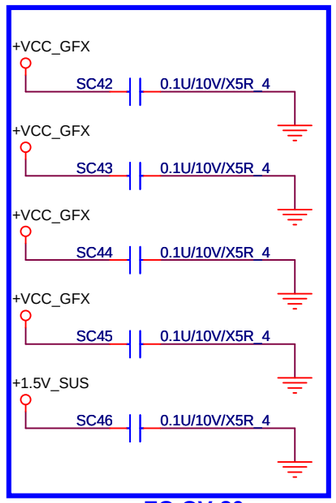
ESD suggestions

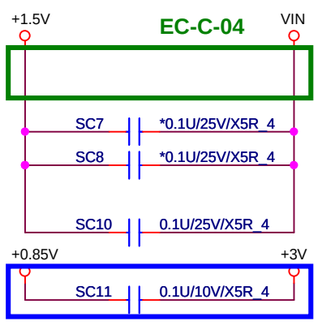
EC-B-28

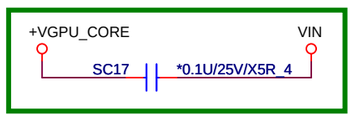


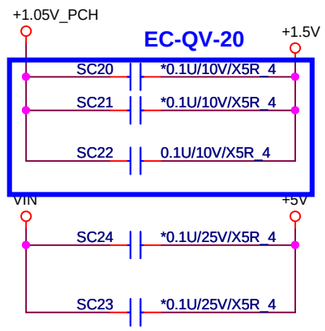






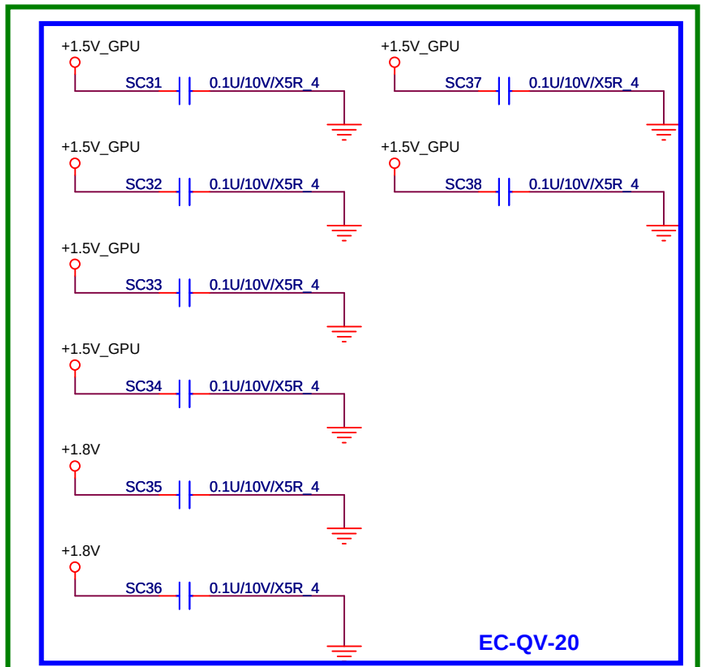






EMI suggestions

EC-C-01



PROJECT : LL3A
Quanta Computer Inc.

Size	Document Number	Rev
B	BT/FP/TPM	1E
Date: Wednesday, January 05, 2011	Sheet 38 of 53	

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WLAN/WWAN/Mini-SSD Nuts

EC-B-37

HOLE3
*h-tc315bc118d118p2

HOLE5
*H-TC315BC110D110P2

EC-C-02

HOLE9
*hg-e315x268d110p2

PAD1
*spad-spe236x766np

HOLE22
H-TC217BC142D102P2

HOLE23
H-TC217BC142D102P2

HOLE24
H-TC217BC142D102P2

HOLE26
H-TC217BC75I75D35P2

HOLE27
H-TC217BC75I75D35P2

HOLE25
H-TC217BC75I75D35P2

EC-QV-16

HOLE8
*h-o315x334d315x334n

HOLE7
*h-o276x866d276x866n

EC-B-40

CPU BKT

BKT1
(PTH)
cpu-bracket

EC-B-37

VGA Nuts

HOLE21
h-tc142bc217d102p2

HOLE15
*h-c118d118n

HOLE18
*h-c118d118n

FAN Hole

HOLE4
*h-c1260d1260na1300

EC-C-02

HOLE1
*hg-c315d110p2

HOLE2
*hg-c315d110p2

HOLE6
*hg-c315d110p2

HOLE14
*hg-c315d110p2

HOLE16
*hg-c315d110p2

HOLE17
*hg-c315d110p2

HOLE20
*hg-c315d110p2

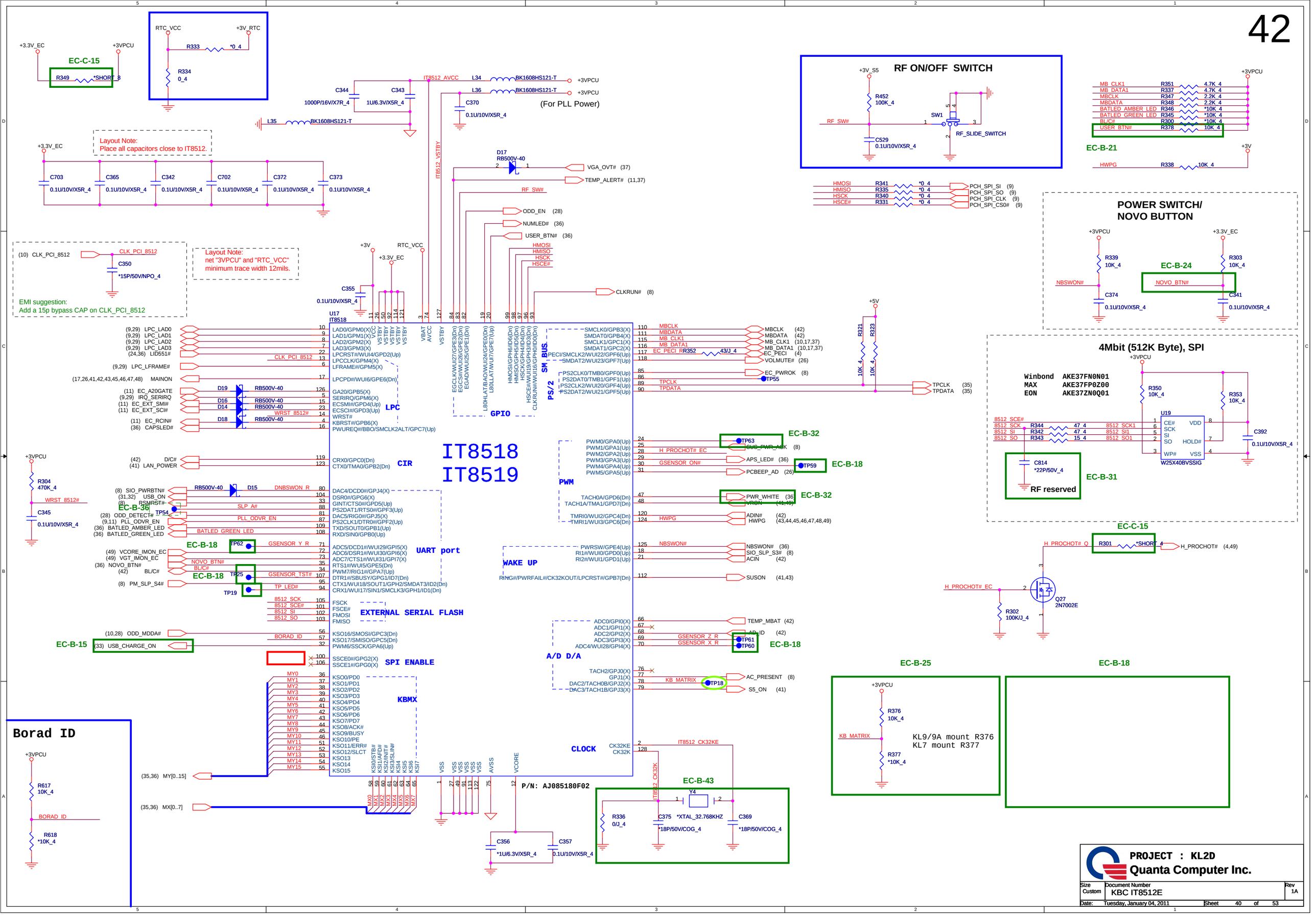
EC-B-40 EC-C-02

HOLE19
*hg-c315d110p2
AGND

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
A	HOLD & SKEW	1A
Date: Tuesday, January 04, 2011	Sheet 39 of 53	

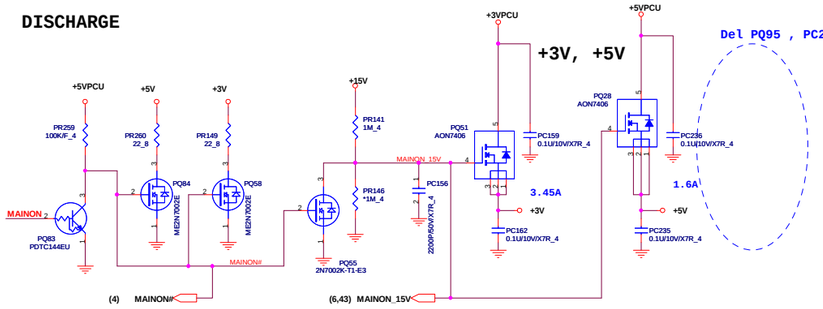


PROJECT : KL2D
Quanta Computer Inc.

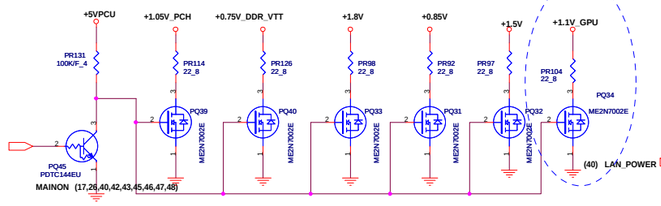
Size	Document Number	Rev
Custom	KBC IT8512E	1A

Date: Tuesday, January 04, 2011 Sheet 40 of 53

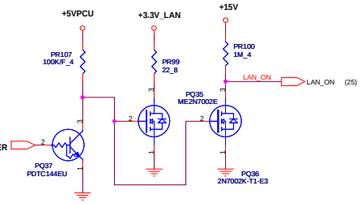
DISCHARGE



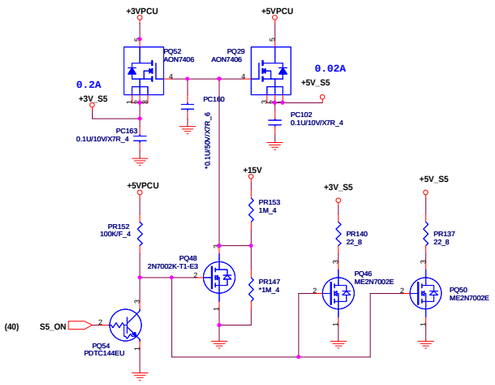
Add +1.1V_GPU DISCHARGE



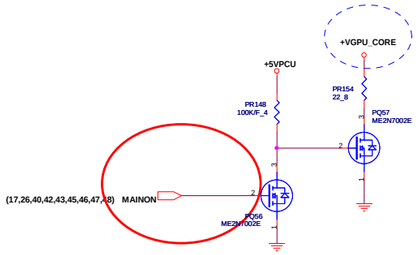
LANVCC

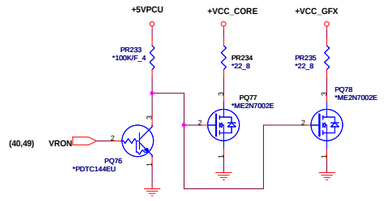


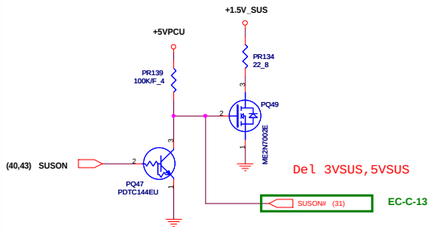
3V_S5, 5V_S5



Change net +VGPU_CORE







PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
D	Discharge	1A
Date: Tuesday, January 04, 2011	Sheet 41 of 53	

Modify FP&PN as LL7

DC-IN

PJ1 SSB-BH

ADPIN+ / ADPIN-

PF1 TR/3216FF10

EL1 UPB201212T-800Y-N

EL2 UPB201212T-800Y-N

PC181 0.1U/50V/X7R_6

PC182 0.1U/50V/X7R_6

VA

PQ63 SI4825DDY-T1

PR155 220K/F_4

PR170 1K/J_6

PR171 1M/J_4

PR159 1M_4

PR166 220K/F_4

PD17 P4SMAJ20A

PQ61 UMT1NTN

VA1

PR162 *1K_4

PQ59 *MMBT3904LT1G

PC170 1U/25V/X7R_8

PQ62 PDTA124EU

PQ66 AOD425

PR9252 1.5K_6

PR164 10K_6

AD_D

PC175 0.1U/50V/X7R_6

EC-C-28

ADPIN+ SC26 *0.1U/25V/X5R_4

ESD suggestions

PQ5 *IMD2

PD5 *1SS355

(17,26,40,41,43,45,46,47,48) MAINON

PD4 *1SS355

PD3 1SS355

ACOK

PQ72 PDTA124EU

88731LDO

PR196 10K/F_4

PR10 47K_4

(40) ACIN

PR197 15K/F_4

PQ73 2N7002K-T1-E3

88731_ACIN

PQ74 2N7002K-T1-E3

PD19 1SS355

PR198 1M_4

PC197 1U/25V/X7R_8

ACOK#

PR22 221K/F_4

PR20 49.9K/F_4

PC21 0.01U/25V/X7R_4

PC8 1U/25V/X7R_8

PR8 10/F_6

PC18 0.1U/50V/X7R_6

88731CSSP

88731CSSN

PC17 0.1U/50V/X7R_6

Place these CAPs close to FETs

C-test

VIN

PC7 10U/25V/X6S_12

PC192 10U/25V/X6S_12

PC191 0.1U/50V/X7R_6

PC6 2200P/50V/X7R_4

PD6 *1SS355

88731BST

PR14 2.2/F_6

PC13 0.1U/50V/X7R_6

PC9 1U/10V/X5R_4

88731LDO

PR13 4.7/F_6

PC16 1U/10V/X5R_4

88731DHI

88731LX

88731DLO

PQ71 MDV1660URH

PQ67 MDV1660URH

PL10 CHOKE_6.8UH/4.5A(7*7*3)

PR193 0.02_1W_3720

BAT-V

PC188 10U/25V/X6S_12

PC190 10U/25V/X6S_12

PC5 10U/25V/X6S_12

PC4 0.1U/50V/X7R_6

ER1 2.2_8

EC1 1500P/50V/X7R_4

PR178 200K/F_4

AOL1413 PQ70

PR180 100K/F_4

EC-C-41

PD22 SSM34PT

PR194 0.01_1W_3720

PR19 10/F_6

PR18 10/F_6

88731CSSP

88731CSSN

PC20 0.1U/50V/X7R_6

PR11 100K/F_4

ACOK

PQ6 2N7002K-T1-E3

ACIN=17.5V

AC_OK

+3VPCU

PC12 0.1U/10V/X7R_4

PR16 0_4

(40) AD_ID

MBCLK

MBDATA

PR12 0_4

PR15 0_4

88731_IINP

PR21 4.75K_4

PC19 0.01U/25V/X7R_4

PR17 *8.45K/F_4

PC25 0.01U/25V/X7R_4

PC24 *0.01U/25V/X7R_4

PC23 0.01U/25V/X7R_4

PC22 *1U/10V/X5R_6

PC26 *0.1U/10V/X7R_4

PR195 *SHORT-1A

GND_CHG

PR9 100/F_4

PC10 0.01U/25V/X7R_4

88731REF

PC11 0.1U/50V/X7R_6

PR6 10/F_6

PR7 10/F_6

88731CSOP

88731CSON

PU1 ISL88731A

DCIN GND CSSP CSSN BOOT VDDP VCC UGATE PHASE LGATE PGND CSOP CSON VFB NC ICOMP VREF NC GND SCL SDA NC ICM VCOMP NC ICOMP

PD7 1SS355

PQ7 2N7002K-T1-E3

D/C#

PR26 *0_4

PR24 10K/F_4

PR25 10K/F_4

PC29 *1000P/50V/X7R_4

PU2 G1331T11U

PD8 1SS355

PR27 332K/F_4

PR28 475K/F_4

PC28 1000P/50V/X7R_4

PR23 100_4

+5VPCU

(40) D/C#

BL/C# (40)

PQ8 2N7002K-T1-E3

Battery Low 7.5V

BAT-V

PL8 UPB201212T-800Y-N

PL9 UPB201212T-800Y-N

PF2 FUSE_10A_125V(FAST)

VBATT

PC3 0.1U/25V/X5R_4

PJP13 1827654-1

BT+ BT+ SCLK SDATA BT_TH GND GND

(40) MBDATA

(40) MBCLK

PR5 200/F_4

PR4 200/F_4

PD1 MMBZ5232BPT(5.6V+5%)

PD2 MMBZ5232BPT(5.6V+5%)

PC15 100P/50V/NPO_4

PC14 100P/50V/NPO_4

PR67 10K/F_4

PC68 0.1U/10V/X7R_4

TEMP_MBAT (40)

Modify FP&PN as LL7

VA

PR29 100K/F_4

PC27 0.1U/50V/X7R_6

PR30 16.9K/F_4

+5V

PC30 0.1U/10V/X7R_4

+3V

PR32 499_6

PC38 *0.1U/10V/X7R_4

PU4 LM431SACMF

PU3 G1331

PR31 47K_4

ADIN# (40)

VIN

PC9212

PR9253 475K/F_4

PR9254 100_4

PR9255 10K/F_4

PD23 1SS355VM

PR9256 300K/F_4

PC9213 *1000P/50V/X7R_4

PU13 G1331T11U

PQ9070 2N7002K

+0.75V_DDR_VTT
TDC : 2A

+1.5V_SUS
Fs=400K
TDC :19A(Imax)
OCP : 23A

Place these CAPs close to FETs

C-test

110mil

VIN

VIN_DDR

PC137 0.1U/50V/X7R_6
PC136 2200P/50V/X7R_4
PC141 10U/25V/X6S_12
PC140 10U/25V/X6S_12

+0.75V_DDR_VTT
PC142 *0.1U/10V/X7R_4
PC139 10U/6.3V/X5R_8
PC134 10U/6.3V/X5R_8

+1.5V_SUS_P
PC143 2.2U/10V/X5R_6
PR122 *0_4
PR121 0_4
PC150 0.1U/50V/X7R_6
PR133 2.2/F_6

(6,14,15) SMDDR_VREF
PC138 .033U/16V/X7R_4

PU9
RT8207LGQW

1	VTTGND	GND	25
2	VTTSNS	VTT	24
3	GND	VLDOIN	23
4	MODE	VBST	22
5	VTTREF	DRVH	21
6	COMP	LL	20
7	NC	DRVL	19
8	VDDQSNS	PGND	18
9	VDDQSET	CS_GND	17
10	S3	CS	16
11	S5	VSIN	15
12	NC	V5FILT	14
		PGOOD	13

DDR_VBST
DRVH
DDR_LL
DRVL
DDR_CS
DDR_VSIN
DDR_V5FILT

PQ38 AON6428L
PQ41 AON6718L
PQ42 *AON6718L

EC-QV-05
PL6 0.36uH
ER5 *2.2_8
EC5 *1500P/50V/X7R_4

C-test
+1.5V_SUS

+1.5V_SUS_P
PR135 10.2K/F_4
PR130 10K/F_4
PC144 *1000P/50V/X7R_4
PC109 330U/2VLESG_7343
PC111 220U/2.5V/ESR15_7343
PC99 *220U/2.5V/ESR15_7343
PC94 0.1U/10V/X7R_4
PC256 10U/6.3V_8

EC-C-39

(4,8) SYS_PWROK
PR266 0_4
(17,26,40,41,42,45,46,47,48) MAINON
PR138 *0_4
PC151 *0.1UF/10V/X7R_4

DDR_V5FILT
PR136 *0_4
S3
S5
PR151 7.15K/F_4
PR142 5.1_6
PC157 1U/10V/X5R_4
PC158 1U/10V/X5R_4
+5VPCU
HWPG
(40,44,45,46,47,48,49)

PR145 620K_6
VIN_DDR
DDR_COMP

(40,41) SUSON
PR150 0_4
PC155 *0.1U/10V/X7R_4

PR258 *SHORT-1A

51116AGNA

C-test

+1.5V_SUS
PQ53 SI3456DDV
0.5A
+1.5V
PC147 10U/25V/X6S_12
PC164 10U/25V/X6S_12
PC154 10U/6.3V/X5R_8
PC153 10U/6.3V/X5R_8
PC161 *330U/2.5V/9m_3528
PC152 *0.1U/10V/X7R_4

+1.5V
PR53 22_8
PQ22 ME2N7002E
PR55 1M_4
PD9 *1SS355@NC
(6,41) MAINON_15V
1.5V_ON
PR54 *0_4@NC
PC65 *0.015U/50V_6@NC
EC-A-07
PR59 *1M_4@NC
PQ21 ME2N7002E
PS_S3CNTRL
+5VPCU
PR47 100K/F_4
MAINON
PQ20 ME2N7002E

Change to +5VPCU

EC-C-26

PQ9064 AOL1428A
6.8A
+1.5V_SUS
+1.5V_GPU
PC9202 10U/6.3V/X5R_6
PR9246 100K_4
1.5V_ON
PC9206 0.015U/50V_6
PC9203 10U/6.3V/X5R_6
PC9204 10U/6.3V/X5R_6
PC9205 *100U/6.3V_3528@NC

Change to +1.5V_SUS

PQ25 AOL1448
5A
+1.5V_SUS
+1.5VCPU
PC84 10U/6.3V/X5R_6
1.5V_ON
PC73 *0.015U/50V_6@NC
PC77 10U/6.3V/X5R_6
PC74 10U/6.3V/X5R_6
PC81 *100U/6.3V_3528@NC

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3/0.75V(RT8207AGQW)	1A

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+5VPCU
Fs=400K
TDC : 7.5A(Imax)
OCP : 11A

+3VPCU
Fs=500K
TDC :6A(Imax)
OCP : 9A

(8,9,24,25,28,35,36,38,40,41,42,45,46) +3VPCU
(28,41,42,43,45,46,47,48) +5VPCU
(24,28,31,38,41,43,45) +15V
(24,38,42,43,46,47,48,49) VIN

5V_AL
PR239 39K/F_4
(17,37,49) SYS_SHDN#
3V5V_EN
PR251 0_4
VIN
C-test
+DC1_PWR_SRC
PC116 10U/25V/X6S_12
PC241 10U/25V/X6S_12
Place these CAPs close to FETs
PC117 0.1U/50V/X7R_6
PC239 2200P/50V/X7R_4
PQ80 AON7406
DH5
EC-QV-05
PL15 2.2UH-PCMC063T-2R2MN
OUT1
LX5
PC237 0.1U/10V/X7R_4
PC119 4.7U/10V/X5R_8
PC238 220U/6.3V/ESR25_7343
PR237 *0_4
PR238 0_4
ER4 *2.2_8
EC4 *1500P/50V/X7R_4
PQ79 AON7702
DL5
PR241 196K/F_4
DDPWRGD_R
3V5V_EN
PC240 0.1U/50V_6
PR242 2.2/F_6
PU12 RT8206MGQW
BYP OUT1 FB1 ILIM1 POK1 EN1 UGATE1 PHASE1 PAD PAD PAD
LDOREFIN LDO VIN NC EN_LDO VCC TON REF
BOOT1 LGATE1 PVCC NC GND PGND LGATE2 BOOT2
REFIN2 ILIM2 OUT2 SKIP# POK2 EN2 UGATE2 PHASE2
PR255 174K/F_4
SKIP
PC247 0.1U/50V_6
PR250 2.2/F_6
DL3
PR244 4.7/F_6
PR246 390K_4
PC243 0.1U/50V/X7R_6
PC245 1U/25V/X5S_6
PR245 *0_4
REFIN2
PR248 150K/F_4
5V_AL
PR105 *10/F_6
PC242 4.7U/10V/X5R_8
PC246 1U/10V/X5R_4
PR249 0_4
PC248 0.1U/10V/X7R_4
PR256 0_4
REF
PR257 *0_4
+DC2_PWR_SRC
VIN
C-test
PC251 10U/25V/X6S_12
PC148 *10U/25V/X6S_12
Place these CAPs close to FETs
PC146 0.1U/50V/X7R_6
PC249 2200P/50V/X7R_4
DH3
PQ81 AON7406
LX3
PL16 2.2UH-PCMC063T-2R2MN
OUT2
ER6 *2.2_8
EC6 *1500P/50V/X7R_4
PQ82 AON7702
PR253 0_4
PR254 *0_4
PC250 220U/6.3V/ESR25_7343
PC149 4.7U/10V/X5R_8
PC145 0.1U/10V/X7R_4
+3VPCU
PC254 0.1u/25V/X5R_4
PR261 0_6
DL3
PD20 BAT54SPT
PD21 BAT54SPT
PC252 0.1u/25V/X5R_4
PC255 0.1u/25V/X5R_4
PC244 1U/10V/X5R_4
PR109 *SHORT-1A
PR264 22_8
+15V
+15V_ALWP
PR263 *200K/F_4
PR247 *39K/F_4
PR262 *0_6
5V_AL
PC253 0.1u/25V/X5R_4
AGND_DC/DC
SKIP
PR252 0_4
DDPWRGD_R
PR240 0_4
HWPG (40,43,45,46,47,48,49)

PROJECT KL5A
Quanta Computer Inc.
Size C
Document Number 3V/5V (RT8206MGQW)
Rev 1A
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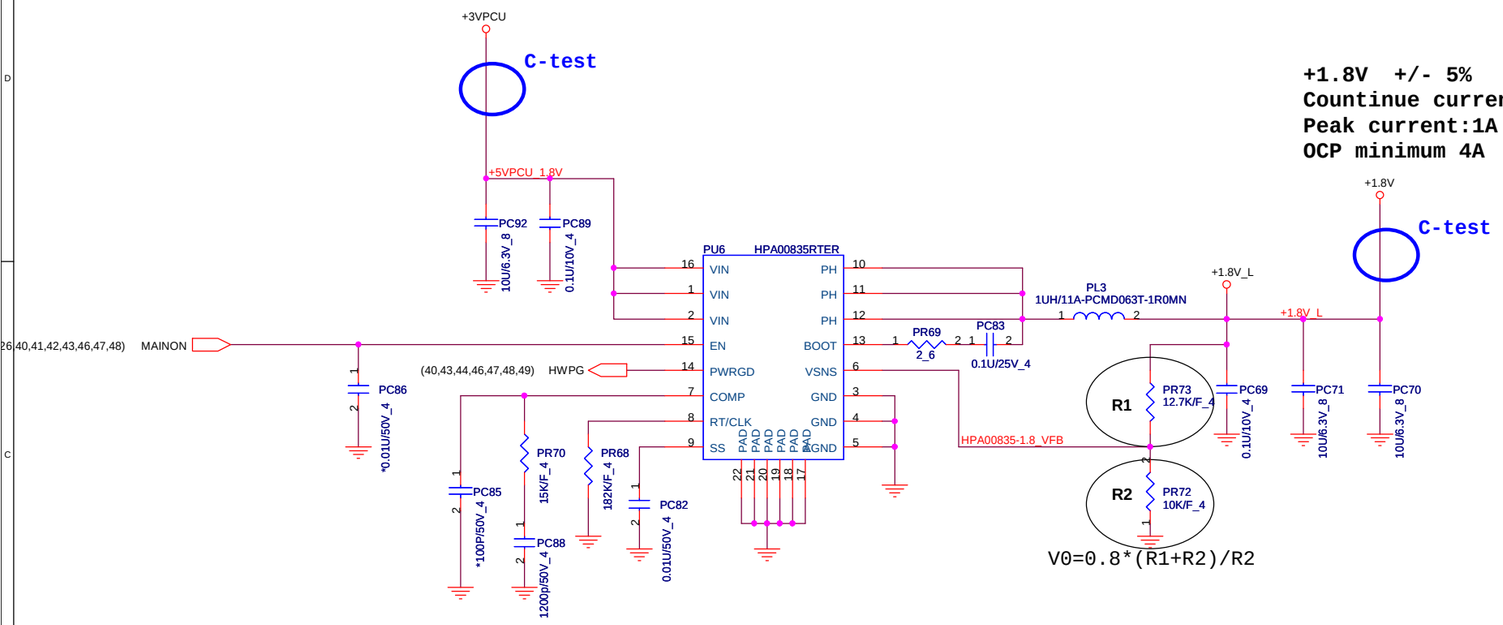
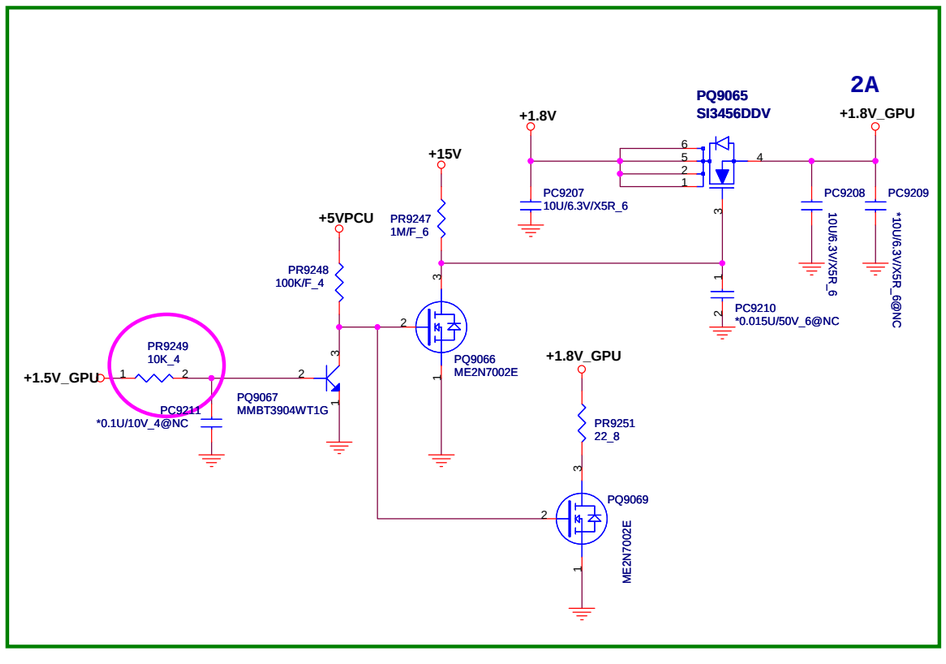
+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A
OCP minimum 4A



EC-C-26



PROJECT KL5A Quanta Computer Inc.		
Size: Custom	Document Number: +1.8V (HPA00835RTER)	Rev: 1A
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+VGPU_CORE
Fs=300K
TDC : 16.8A(Imax)
OCP : 33.6A

Place these CAPs close to FETs

VIN_GFX_CORE
PC195 2200P/50V/X7R_4
PC196 0.1U/50V/X7R_6
PC189 10U/25V/X6S_12
PC193 10U/25V/X6S_12
PC194 10U/25V/X6S_12
C-test VIN

+5VPCU
PC178 1U/10V/X5R_4
PR157 100K_4
PR183 22_6
AGND_VGPU
PC165 0.01U/25V/X7R_4
PC186 1U/10V/X5R_4
PD18 1SS355
C-test
PR190 2.2/F_6
PC180 0.1U/50V/X7R_6
GFX_CORE_HDR
GFX_CORE_BST
GFX_CORE_LX
GFX_CORE_LDR
GFX_CORE_CSP
GFX_CORE_CSN
GFX_CORE_RSP
GFX_CORE_RSN

PU10 OZ8117
VIN
VDDP
VDDA
ON/SKIP
VSET1
VSET2
G0
G1
TSET
VREF
GNDA
HDR
BST
LX
LDR
CSP
CSN
PG
RSP
RSN
GNDP

PQ65 AON6428L
PQ68 AON6718L
PQ69 AON6718L
ER7 *2.2_8
EC7 *1500P/50V/X7R_4

EC-QV-05
PL7 0.36uH
GFX_CORE_P
PR173 20K/F_4
PR174 20K/F_4
PR176 10K/J_6_NTC
PC171 0.033U/50V/X7R_6
PC2 330U/2V/ESR9_7343
PC187 330U/2V/ESR9_7343
PR165 51.1/F_6
PC173 1000P/50V/X7R_4
PR163 432/F_4
PC176 22P/50V/NPO_4
AGND_VGPU

PC184 10U/6.3V_8
PC1 10U/6.3V_8
PC185 0.1U/25V/X5R_4
+VGPU_CORE
C-test

Close To VGPU Discrete Power Rail Side
Change to +VGPU_CORE

(17) GFX_RUN_ON
PR158 68K_4
PD16 1SS355
PC167 0.1U/25V/X5R_4
Change to 3VPCU next stage
+3VPCU
PR181 10K_4
PR184 10K/F_4
PR182 0_4
PC166 0.1U/25V/X5R_4
PC179 *1000P/50V/X7R_4@NC
AGND_VGPU
PR179 10K_4
(17) GFX_CORE_CNTRL0
PR177 10K_4
PQ4 MMBT3904WT1G
PQ3 ME2N7002E
Change to 3VPCU next stage
PR175 *SHORT-1A
PR186 10K/F_4
+3V
HWPG
(40,43,44,45,47,48,49)
C-test

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VCC_GFX_CORE
1	1	1.12V
1	0	0.95V
0	1	1.05V
0	0	0.9V

PR167 51/F_6
PC169 0.01U//50V/X7R_4
PR156 51/F_6
PC168 0.01U//50V/X7R_4
+VGPU_CORE

Change to +5VPCU
+3VPCU
PR189 10K_4
PR185 10K_4
PR188 10K_4
GFX_CORE_G1 #
PC183 *1000P/50V/X7R_4@NC
GFX_CORE_ACT
(17) GFX_CORE_CNTRL1
PR192 10K_4
PQ2 ME2N7002E
PQ64 MMBT3904WT1G

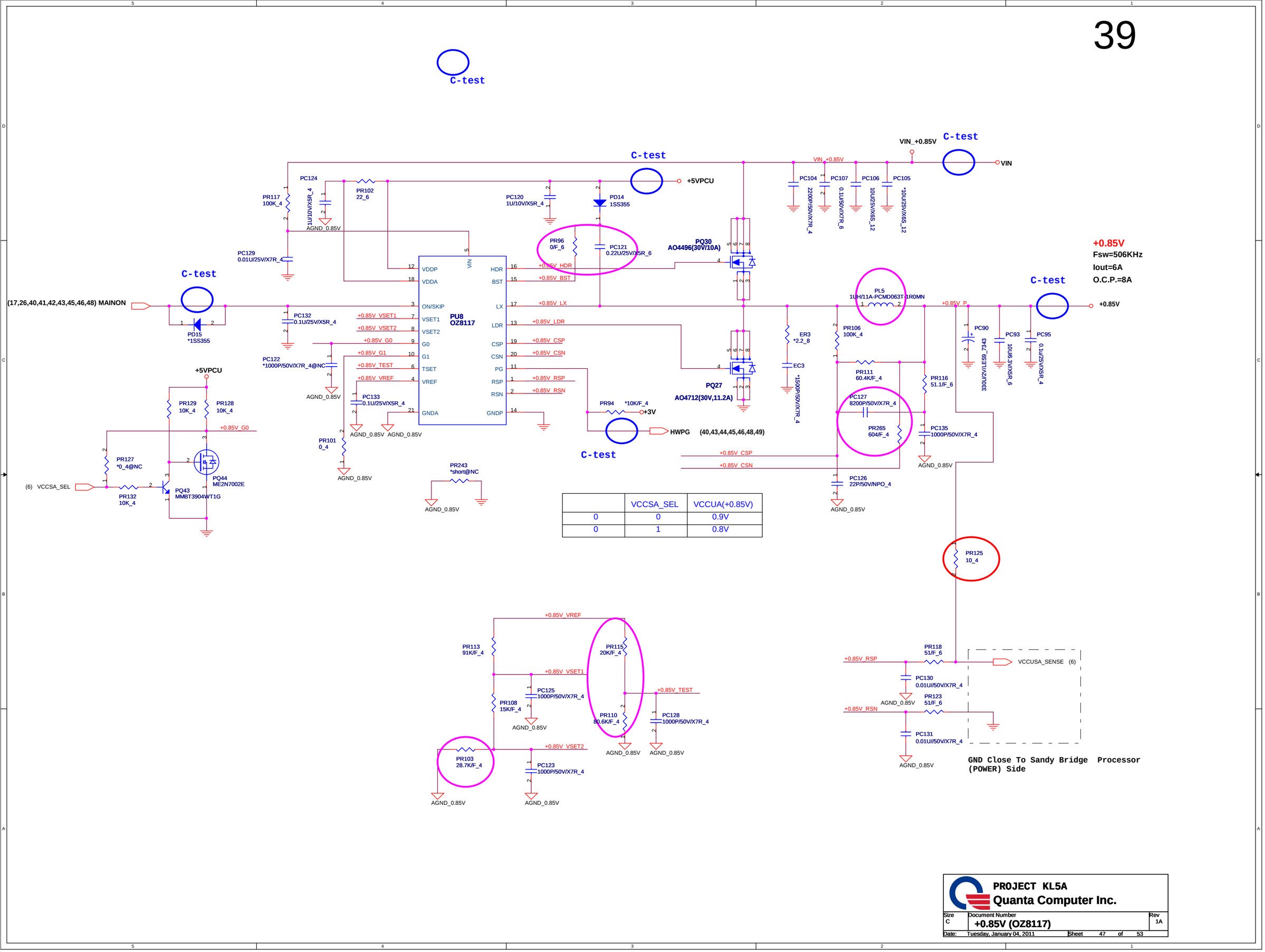
Del 3VSUS , PR9034
+5VPCU
PR39 100K/F_4
PR40 100K/F_4
PQ13 ME2N7002E
PQ16 ME2N7002E
(17,26,40,41,42,43,45,47,48) MAINON
PR35 *0_4@NC
PR36 0_4
PR37 100K/1_4
PR38 43K/F_4
PQ9 MMBT3904WT1G
PC46 1U/10V/X5R_4

Change to +1.5V_SUS
C-test
+1.5V_SUS
PC42 10U/6.3V/X5R_8
PC40 0.1U/25V/X5R_4
Change to +5VPCU
PC44 0.33U/6.3V/X5R_4
+5VPCU
PC39 1U/10V/X5R_4
PU5 UP0104PSU8
VIN
NC
EN
VDD
GND
PGOOD
VOUT
ADJ
GND1
(40,43,44,45,47,48,49) HWPG
HWPG
R1
1VADJ
PR33 2.7K/F_4
PR34 10K/F_4
R2
VO=(0.8(R1+R2)/R2)
R2<120Kohm

+1.1V_GPU
Iout=2A
+1.1V_GPU
PC33 10U/6.3V/X5R_6
PC32 10U/6.3V/X5R_6
PC36 0.1uF/25V/X5R_4
PC37 *10U/6.3V/X5R_8@NC

PR179、PR188、PR184、PR189 will connect to 3VPCU and change to 10k at B stage layout(Same as KL8A),

PR1 82K/F_4
PR2 25.5K/F_4
PR3 294K/F_4
PR161 20K/F_4
PR160 80.6K/F_4
PR168 30.1K/F_4
PR172 4.87K/F_4
GFX_CORE_VREF
GFX_CORE_VSET2
GFX_CORE_VSET1
GFX_CORE_TEST
PC177 1000P/50V/X7R_4
PC172 1000P/50V/X7R_4
PC174 1000P/50V/X7R_4
PQ1 ME2N7002E
PQ60 ME2N7002E
GFX_CORE_ACT
GFX_CORE_G1 #
AGND_VGPU



	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
C	+0.85V (OZ8117)	1A

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The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:

- NVVDD <= VDD33+0.5 V
- FBVDDQ <= VDD33+0.5 V

+1.05V_PCH

VIN=20V, FSW(KHZ)=226K
VIN=9V, FSW(KHZ)=210K
Iout=17.5A
O.C.P.=20A

(17,26,40,41,42,43,45,46,47) MAINON

+5VPCU

VIN

+1.05V_PCH

+3V

HWPG (40,43,44,45,46,47,49)

VTT_SENSE (6)

PU7 OZ8117

PQ23 AON6718L

PQ24 *AON6718L

PQ26 AON6428L

PC100 1U/10V/X5R_4

PR78 22_6

PR81 100K_4

PC114 0.01U/25V/X7R_4

PC96 1U/10V/X5R_4

PD12 1SS355

PR77 0/F_6

PC97 0.22U/25V/X5R_6

PC79 2200P/50V/X7R_4

PC78 0.1U/50V/X7R_6

PC76 10U/25V/X6S_12

PC75 10U/25V/X6S_12

PD13 *1SS355

PC112 0.1U/25V/X5R_4

PC113 0.1U/25V/X5R_4

PR75 *10K/F_4

PR236 *short@NC

PL4 0.36uH

ER2 *2.2_8

EC2 *150P/50V/X7R_4

PR82 20K/F_4

PR85 20K/F_4

PR267 10K/J_6_NTC

PR88 51.1/F_6

PC108 0.033U/50V/X7R_6

PR86 402/F_4

PC115 1000P/50V/X7R_4

PC103 22P/50V/NPO_4

PC80 330U/2V/LESG_7343

PC87 *330U/2V/LESG_7343

PC91 10U/6.3V/X5R_6

PC72 0.1U/25V/X5R_4

PC257 330U/2V/LESG_7343

PR90 10_4

1.05VPCH_HDR
1.05VPCH_BST
1.05VPCH_LX
1.05VPCH_LDR
1.05VPCH_CSP
1.05VPCH_CSN
1.05VPCH_RSP
1.05VPCH_RSN
1.05VPCH_VSET1
1.05VPCH_TEST
1.05VPCH_VREF
1.05VPCH_P

AGND_1.05V_PCH

C-test

Change to AGND_1.05V_PCH

PR80 84.5K/F_4
PR79 52.3K/F_4
PC98 1000P/50V/X7R_4
PR84 20K/F_4
PR83 80.6K/F_4
PC101 1000P/50V/X7R_4

PR89 51/F_6
PR87 51/F_6
PC110 0.01U/50V/X7R_4
PC111 0.01U/50V/X7R_4

GND Close To Sandy Bridge Processor (POWER) Side

Del +1.5V SW

PROJECT KL5A Quanta Computer Inc.		
Size: C	Document Number: +1.05_PCH (OZ8117)	Rev: 1A
Date: Tuesday, January 04, 2011	Sheet 48 of 53	

3+1 Phases design (45W CPU)
Vcore : 1 x HS-FET, 2 x LS-FET
VGT : 1 x HS-FET, 2 x LS-FET

	DIS	UMA
PR269	0 ohm	NA

45W CPU
Vcore Icc_MAX = 94A — PR7038 = OPEN
VGT Icc_MAX = 33A — PR7008 = OPEN

35W CPU
Vcore Icc_MAX = 53A — PR7038 = 7.87K
VGT Icc_MAX = 24A — PR7008 = 16.5K

NTC Place near the +VCC_GFX O/P Inductor
NTC Place near the +VCC_CORE phase 1 Inductor
NTC Place near the +VCC_CORE HS-FET
NTC Place near the +VCC_GFX HS-FET

KL9A Schematic EC Tracking Record B (for A2 --> B)Sep. 27, 2010

EC #	Page	Description	Part Affected
EC-B-00	**4**	Change U18 output type from coms to open-drain.	**U18**
EC-B-01	**10**	Remove TPM funtion. (LPC interface)	**U14**
EC-B-02	**10,38**	Remove keyboard light funtion.	**U14,CN3**
EC-B-03	**11**	Switch pins between BOARD_ID0 and BOARD_ID1.	**U14**
EC-B-04	**11,31**	Change net name from WIMAX_OFF# TO WLAN_OFF#, also add pull high 10K with GPIO16	**U14,R530**
EC-B-05	**11**	Add board id table.	
EC-B-06	**25**	Change ESD protection components.	**U47,U48**
EC-B-07	**26**	Modify the DIS backlight pin connecting to LVDS connector.	**CN1**
EC-B-08	**28**	Add R37 and R47 for normal-open audio jack.	**R37,R47**
EC-B-09	**29**	Add SD_4~SD_7 to support SD 3.0	**CN12**
EC-B-10	**30**	Remove 2nd battery switch.It is only for KL8/8A.	
EC-B-11	**31**	Correct the LPC connection for debug card.	**CN26**
EC-C-12	**32**	change capacitors connection from +3V to +3.3V_SSD,+1.5V to +1.5V_WIMAX	
EC-B-13	**32**	Remove unused nets in SSD connector.	**CN24**
EC-B-14	**33**	Switch the PCIE_TXN5 , PCIE_TXP5 for the right connection.	**U21**
EC-B-15	**35**	Change control signal of U25 enable pin from USB_ON to USB_CHARGE_ON for usb charge function.	**U25**
EC-B-16	**28**	Modify left & right sound reverse issue	
EC-B-17	**35**	Correct USB charge IC footprint.	**U27**
EC-B-18	**36,42**	Remove G-sensor circuits.	**U17**
EC-B-19	**37**	Correct the pin connection of CN8.	**CN8**
EC-B-20	**38**	Correct LED footprint.	**LED1,LED2**
EC-B-21	**38**	Add R51,R82 for user button defined as a power button function.	**R51,R82,R378**
EC-B-22	**40**	Add R692,R693 and disable EMI solution "CML3".	**R692,R693,CML3**
EC-B-23	**40**	Remove TPM circuits.	
EC-B-24	**42**	Correct connection and net name of NOVO_BTN#	
EC-B-25	**42**	Add KB_MATRIX signal for different keyboard matrix selection between KL7 and KL9.	**R376,R377**
EC-B-26	**46,48**	Add a +1.5V_GPU and +1.8V_GPU circuits for GPU power sequence tuning.	**PQ9064,PC9202,PC9203,P9204,PC9205,PC9206,PR9246**
EC-B-27	**10,24,27 33,34,14 37,38**	Add EMI solution	**EC11,EC12,R658,R659,R660,R661,EC13,C711,CML1,R11,R12,CML2,R35,R36,CML4,R649,R651,C677,C678 CA1,CA2,CA3,CA4,CA5,CA6,EC14~EC26,C466**
EC-B-28	**40**	Add ESD solution	**SC1~SC30**
EC-B-29	**39**	Follow PDC standard parts pin definition	**CN16**

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC RECORD B	1A

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EC #	Page	Description	Part Affected
EC-B-30	**4,8**	Add net PCIECLKRQ5~9#	**U14**
EC-B-31	**4,8,9 10,26 42**	Add RF solutions	**R632,R633,C704,C705,C706,C713,R662,R664,R678,R699,R700,R701,R702,R703,C714,C715 C717,C718,C720,C727,C809,C810,C811,C812,C813,C814**
EC-B-32	**42**	Change EC GPIO	**U17**
EC-B-33	**10,33**	Change PCH GPIO66 net name to PCH_CLK_25M and connect to USB3.0 XTAL	**R636,R637**
EC-B-34	**4**	Delete XDP_DBRST# pull high RES	**U32,R598**
EC-B-35	**4**	Add VCCSA_SEL pulll down RES	**R598**
EC-B-36	**4**	Disconnect SLP_A# from PCH to EC	
EC-B-37	**41**	Modify hole footprint	**Hole21,Hole3**
EC-B-38	**35**	Un-stuff USB charger schematic	**R461,R465,C530,U27,R689,R690**
EC-B-39	**46**	Modify power sequence to fix S3 issue	**PR266**
EC-B-40	**8,27 28,53 40,38**	Reserve ESD solution	**RV16,C815,C816,C817,C818,C819,C820,C821,C822,C823,C824**
EC-B-41	**45**	Power add discharge current solution	**PD22**
EC-B-42	**9**	Follow vendor XTAL CAP suggestion	**C118,C119**
EC-B-43	**42**	Change EC PN & un-stuff XTAL	**Y4,C369,C375,R336,U17**
EC-B-44	**6 53**	Del +VCC_GFX power	**C684,C685,C690,C682,C302,C310,C313,C319,C314,C693,C323,C315,R597,R591 PL13,PC221,PC218,PC58,PC215,PQ75,PC232,PC62,PL14,PR56,PR58,ER10,EC10,PQ1,PQ19,PR209,PC210 PC64,PR52,PR212,PR51,PC57,PC56,PR229,PC220,PC217,PC219,PR221,PR220,PC223,PR112, PC258,PC233,PR225,PC234,PC227,PR227**

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KL9A Schematic EC Tracking Record C (for B --> C)Nov. 4, 2010

EC #	Page	Description	Part Affected
EC-C-00	**36**	Change power LED pull high power plane to +3VPCU to fix system enter S3 can't flicker issue	**LED1**
EC-C-01	**38**	Add EMI solution	**SC31,SC32,SC33,SC34,SC35,SC36,SC37,SC38**
EC-C-02	**39**	Modify Hole footprint	**Hole1,Hole2,Hole6,Hole14,Hole16,Hole17,Hole20,Hole19,Hole9,Hole8**
EC-C-03	**12**	Reserve CAP for +VCCAFDI_VRM	**C825**
EC-C-04	**38**	Delete ESD solution SC9 due to +1.5V power plane was deleted & change SC17 power plane bridge, add some component	**SC9,SC17,SC25,SC39,SC40,SC41,SC42,SC43,SC44,SC45,SC14,SC18,SC19,SC28,SC29,SC30,SC10,SC11 SC12,SC13,SC15,SC22,SC46**
EC-C-05	**36**	Modify LED footprint to fix SMT issue	**LED3**
EC-C-06	**25**	Modify bead footprint to fix SMT issue	**L37**
EC-C-07	**21**	Modify VRAM footprint to fix SMT issue	**U4,U5,U28,U29**
EC-C-08	**4**	Un-stuff AND gate component	**U18,C366,R314,R313**
EC-C-09	**27**	Change SD_CLK CAP from 33p to 10p	**C425**
EC-C-10	**22**	Change RES value to fix HDMI test fail item	**R399,R400,R401,R402,R403,R404,R405,R406**
EC-C-11	**26**	Reserve diode for EAPD pin	**D23**
EC-C-12	**9**	Un-stuff JTAG RES	**R181,R182,R528,R534,R533,R538,R168**
EC-C-13	**31**	Add USB3.0 schematic	**CN23,R369,R371,CML4,R637,R657,R704,R705,Q53,Q54,C706,C826,C827,C828,R636,R155,R707,C829,Q55,C830**
EC-C-14	**31**	Modify TP footprint to 3050	**TP20,TP21,TP22,TP23**
EC-C-15		Modify 0 ohm RES to short pad	**R592,R608,R326,R274,R287,R292,R502,R504,R505,R512,R513,R521,R527,R91,R245,R258,R587,R301 R648,R451,R380,R442,R366,R425,R623,R673,R686,R77,R430,R432,R101,R212,R221,R232,R235,R239 R563,R586,R588,R600,R66,R71,R94,R391,R392,R393,R394,R252,R242,R248,R250,R603,R65,R233 R4,R50,R652,L49,L53,R431,R364,R370,R397,R448,R384,R446,L23,R40,R60,R349**
EC-C-16	**12**	Change 0.002 ohm RES to 0 ohm	**R247,R261,R254**
EC-C-17	**26**	Stuff ESD solution	**C480,C481,C482,C483**
EC-C-18	**10**	Remove RF_ON pull down RES	**R522**
EC-C-19	**29**	Add net WWAN_OFF# to disable WWAN function	
EC-C-20	**12**	Change 0 ohm RES to bead	**R222**
EC-C-21	**4**	For INTEL design guide definition and material shortage, will change to 25.5ohm	**R315**
EC-C-22	**6**	Stuff SVID DATA pull high RES	**R286**

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KL9A Schematic EC Tracking Record QV (for C --> QV)DEC. 20, 2010

EC #	Page	Description	Part Affected
EC-QV-00	**42**	Add power circuit for charge issue.	**PR9252,PR9253,PR9254,PR9255,PR9256,PC9212,PC9213,PD23,PU13,PQ9070**
EC-QV-01	**37**	Add 0 Ohm for thermal sensor of DDR & WWAN	**R133,R155**
EC-QV-02	**33**	Modify the USB charge circuit(Add option and reverse circuit, change the USB switch EN to USB_ON_R)	**R522,R636,R708,R709,R710,Q60**
EC-QV-03	**11**	Change the SV_DET pull high to +3V_S5 from +3V	
EC-QV-04	**25**	Change footprint of L37 for SMT request	**L37**
EC-QV-05	**43**	Change footprint of PL4, PL6, PL7, PL15, PL16	**PL4, PL6, PL7, PL15, PL16**
EC-QV-06	**49**	Add capacitor in +VCC_GFX	**PC260**
EC-QV-07	**4**	Add un-stuff capacitor on H_PWRGOOD_R	**C900**
EC-QV-08	**4**	Change to component stuff	**R325,Q29**
EC-QV-09	**8**	Add un-stuff capacitor on SYS_PWROK	**C901**
EC-QV-10	**8**	Change R493 to un-stuff	**R493**
EC-QV-11	**9**	Change footprint to shortpad	**R409,R153**
EC-QV-12	**9**	Add 1M ohm on ACZ_SYNC_CODEC	**R711**
EC-QV-13	**9**	Change C119,C118 to 18p from 6p for RTC issue	**C118,C119**
EC-QV-14	**30**	Change component to un-stuff.	**C783,C784,C736**
EC-QV-15	**26**	Change the footprint for EMI solution stuff BEAD	**R391,R392,R393,R394**
EC-QV-16	**39**	Change HOLE8 to NTPH	
EC-QV-17	**31**	Modify USB3.0 circuit for power saving.	**Q35,R414,R415, D28,R712,Q62,R716,C950,Q63,R717,C951,C952,R713,R714,Q61,C953,R715,R421**
EC-QV-18	**22**	Change the footprint to 4 GND PIN for HDMI	**CN22**
EC-QV-19	**49**	Change PC47 to stuff	**PC47**
EC-QV-20	**38**	Change the P/N for cost saving	**SC2,SC11,SC12,SC13,SC14,SC15,SC16,SC20,SC21,SC22,SC27,SC28,SC29,SC30,SC39,SC40,SC41,SC42 ,SC43,SC44,SC45,SC46,SC31,SC32,SC33,SC34,SC35,SC36,SC37,SC38**
EC-QV-21	**29**	Change C497 to stuff	**C497**

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