Compal Confidential

Schematics Document

NIWE1

Arrandale

with Intel IBEX PEAK-M core logic

REV:0.3

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: **Cover Sheet**

Size	Document Number	Rev
Custom	LA-5751	0.3

Date: Thursday, October 29, 2009 | Sheet 1 of 51

Compal confidential
File Name :

ZZZ1
14W_PCB_LA5751P
ZZZ
HYN@
X76_H512

POWER BD:
POWER BTN
NOVO BTN
POWER MANAGE BTN

CAP SENSOR BD:
VOLUME UP
VOLUME DOWN
MUTE
AUDIO ENHANCE
BUTTON & LED

CARD READER BD:
ENE UB6250/52
HP JACK
MIC JACK

VRAM 64*16
DDR3*4
page23

NVidia N11M-GE1
page19~23

PCI-E X16

Intel
Arrandale
(UMA/DIS)
Socket-rPGA989
37.5mm*37.5mm
page5~9

Clock Generator
RTM890N
page12

DDR3-SO-DIMM X2
BANK 0, 1, 2, 3
page 10,11
UP TO 8G

Dual Channel
DDR3-800(1.5V)
DDR3-1066(1.5V)

HDMI
CONN
page24

level shift IC
ASM1442
page25

100MHz
2.7GT/s
FDI *8
DMI *4

CRT Connector
page26

LVDS
Connector
page27

Intel Ibex Peak M
FCBGA 951
25mm*25mm
page 13~18

AZALIA

Audio Codec
CONEXTAN
CX20671
page33

2Channel Speaker
page33

Analog MIC_Int
page33

PCI Express
Mini card Slot 1
page28

6*PCI-E BUS

PCI Express
Mini card Slot 2
page28

14*USB2.0

CMOS Camera
page27

BlueTooth CONN
page37

6*SATA serial

USB CONN X1(Right)
page37

USB PORT X1(Left)
page37

New Card X1
page28

WWAN
page28

SPI ROM
BIOS
page13

LPC BUS

SIM Card
page28

USB (WWAN)

RTL8103EL/8111DL
10/100/1G LAN
page29

EC
ENE KB926D
page34

Card Reader/Audio Jack SB CONN
ENE UB6250/52 HP X 1+
MS/MS MIC_Ext X1
pro/SD/SD
pro/mmc/XD
page38

ESATA HDD AND USB CONN
page37

RJ45 CONN
page30

Int.KBD
page35

EMC1403
Thermal Sensor
page31

SPI ROM
EC
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SATA HDD CONN
page32

Touch Pad
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SATA ODD CONN
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Title: MB Block Diagram

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DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1 SMB_EC_DA1	KB926 +3VALW	X	V +3VALW	X	X	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926 +3VALW	X	X	X	X	X	X	X	X	X	X	V +3VALW
SMBCLK SMBDATA	PCH +3VALW	V +3VALW	X	X	V +3VS	V +3VS	X	X	X	X	V +3VS	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	X	X	V +3VALW	X	X	X	V +3VS	X	V +3VS	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

@ FUNCTION

Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
3G@	3G function (WWAN)	
CAP@	CAP Sensor function	
CMOS@	CMOS CAMERA function	
ESATA@	E-SATA function	
HDMI@	HDMI function (UMA or DIS)	
UMA_HDMI@	HDMI function (UMA only)	
X76@	X76 BOM	
100@	10/100 LAN function	
GIGA@	GIGA LAN function	
UMA@	UMA only (Arrandale)	
DIS@	DIS only (Arrandale)	

SKU

Arrandale(dGPU) DIS only	DIS@
Arrandale(iGPU) UMA only	UMA@

PCIE PORT LIST

PORT	DEVICE
1	
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	
7	
8	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

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Title: MB Notes List

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VGA and DDR3 Voltage Rails (N11x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	N/A	
GPIO8	I/O	N/A	
GPIO9	OUT	N/A	
GPIO10	OUT	N/A	
GPIO11	I/O	-	Reserve 10K pull low.
GPIO12	IN	N/A	
GPIO13	OUT	N/A	
GPIO14	OUT	-	Reserve 10K pull low.
GPIO15	IN	N/A	
GPIO16	OUT	N/A	
GPIO17	IN	-	PAD
GPIO18	IN	N/A	
GPIO19	IN	N/A	

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.5V) (A)	FBVDD (1.5V) (W)	FBVDDQ (GPU+Mem) (1.5V) (A)	FBVDDQ (GPU+Mem) (1.5V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N11M-GE1 64bit 512MB DDR3	14.02	2.16	TBD	TBD	12.9	12.26	0.66	0.99	1.3	1.95	530	0.56	84	0.15	140	0.15	38	0.13

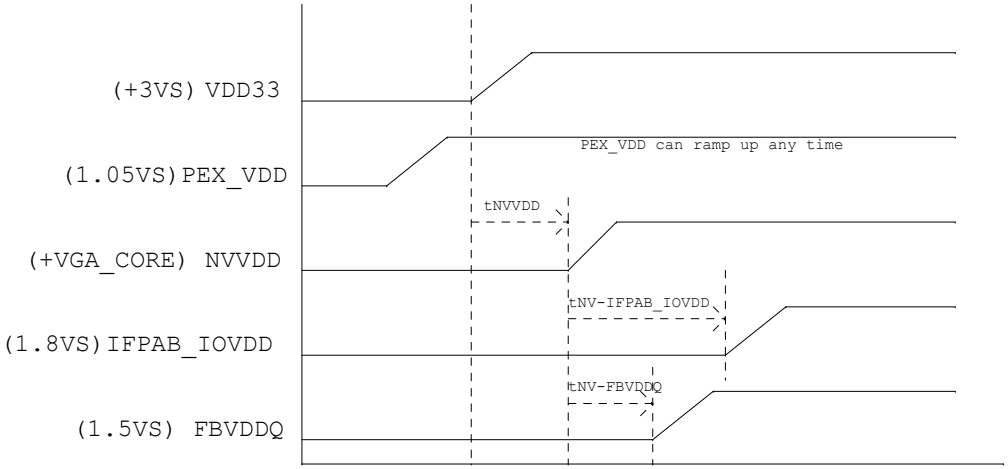
GPIO5 GPIO6

	Device ID
N11M-GE1/LP1 (40nm)	0x0A7D

GPU_VID0	GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	1.03V	P0

Power Sequence

The ramp time for any rail must be more than 40us



Security Classification	Compal Secret Data		
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Title: VGA Notes List

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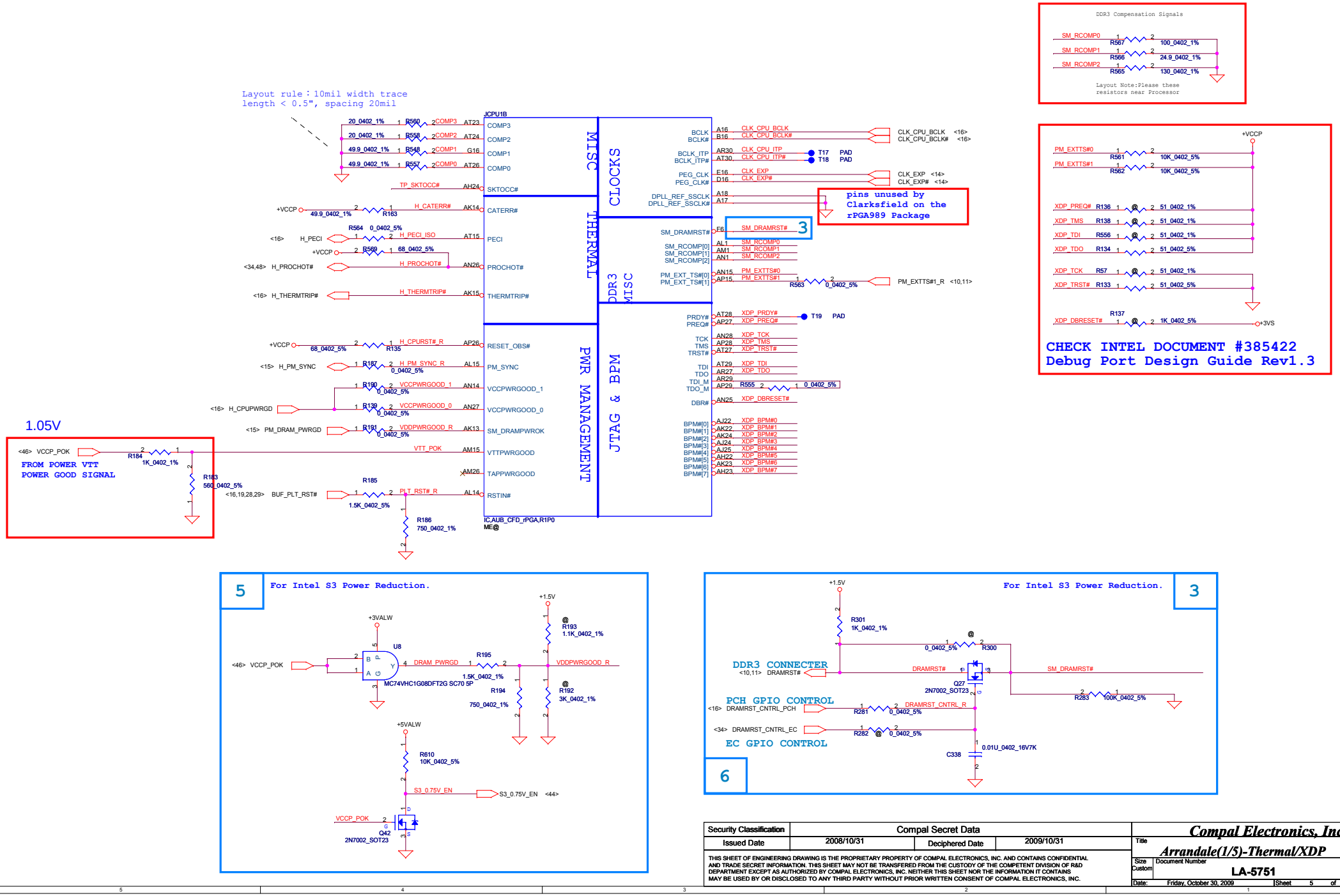

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Title: *Arrandale(1/5)-Thermal/XDP*

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Layout rule : trace length < 0.5"

JCPU1A

DMI

PCI EXPRESS -- GRAPHICS

Intel(R) FDI

IC,AUB_CFD_rPGA,R1P0
ME@

PCIE Lane Numbers Reversed
CFG3-PCI Express Static Lane Reversal

DIS@

FOR ES1 SAMPLE ONLY

JCPU1E

RESERVED

IC,AUB_CFD_rPGA,R1P0
ME@

CFG Straps for PROCESSOR

CFG0 — R58 3.01K_0402_1%

PCI-Express Configuration Select	
CFG0	1: Single PEG 0: Bifurcation enabled

Not applicable for Clarksfield Processor

CFG[1:0] 11=1*16 PEG
10=2*8 PEG

CFG3 — R61 3.01K_0402_1%

CFG3-PCI Express Static Lane Reversal	
CFG3	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 ->1, ...

CFG4 — R60 3.01K_0402_1%

CFG4-Display Port Presence	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
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Title: Arrandale(2/5)-DMI/PEG/FDI

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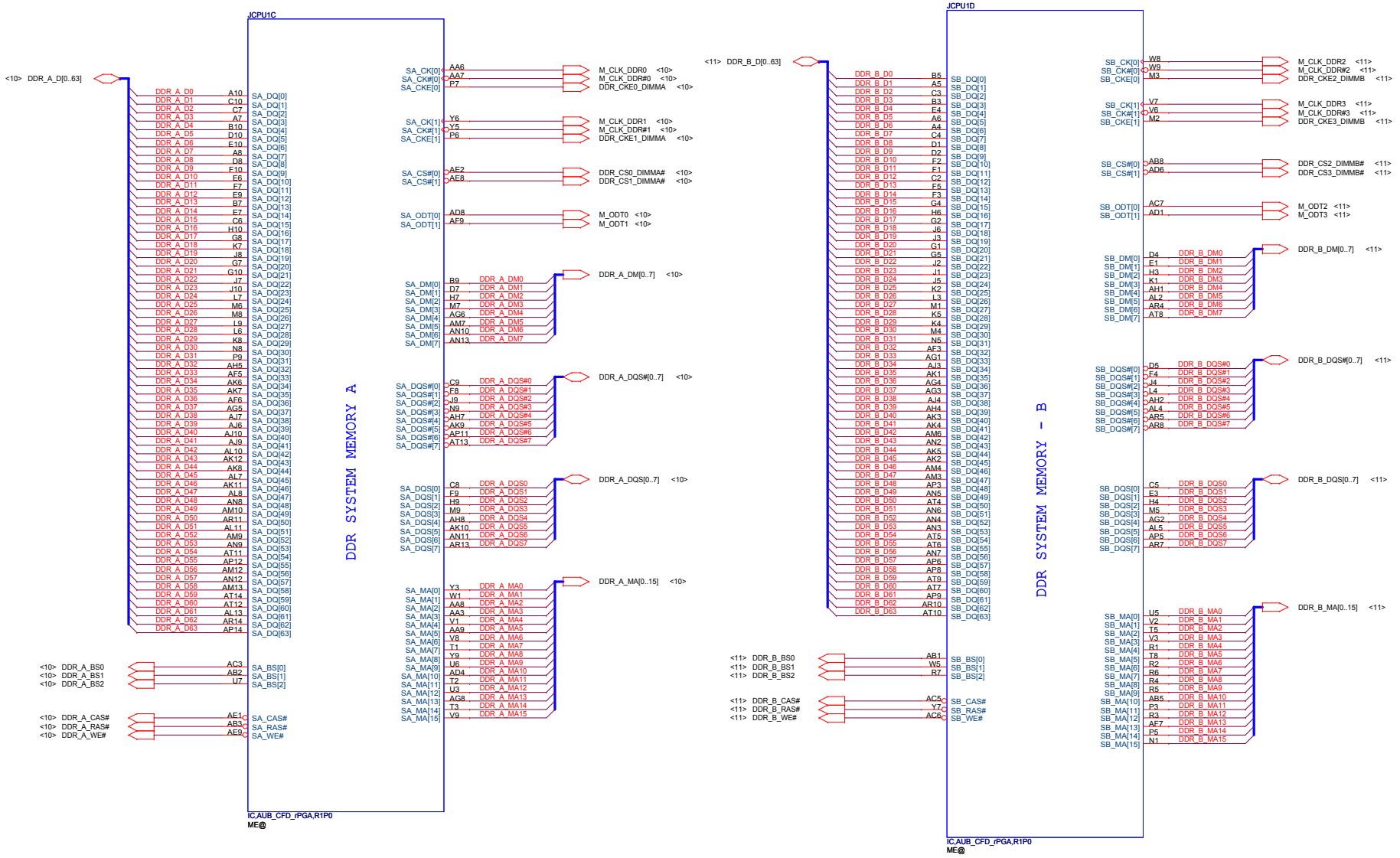

Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

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Title: Arrandale(3/5)-DDR III

Size: Custom | Document Number: LA-5751 | Rev: 0.3

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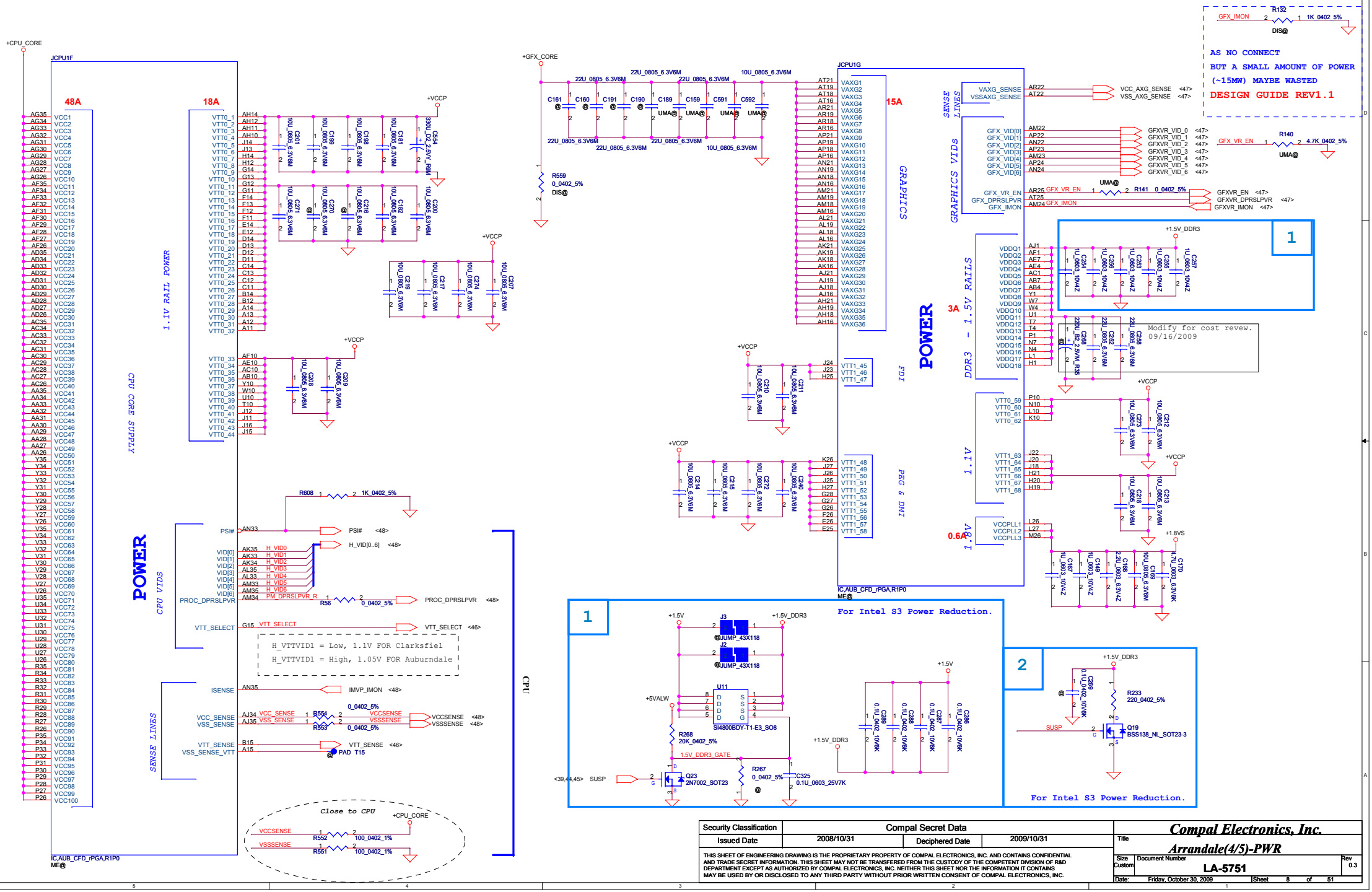

Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

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Title: **Arrandale(4/5)-PWR**

Size	Document Number	Rev
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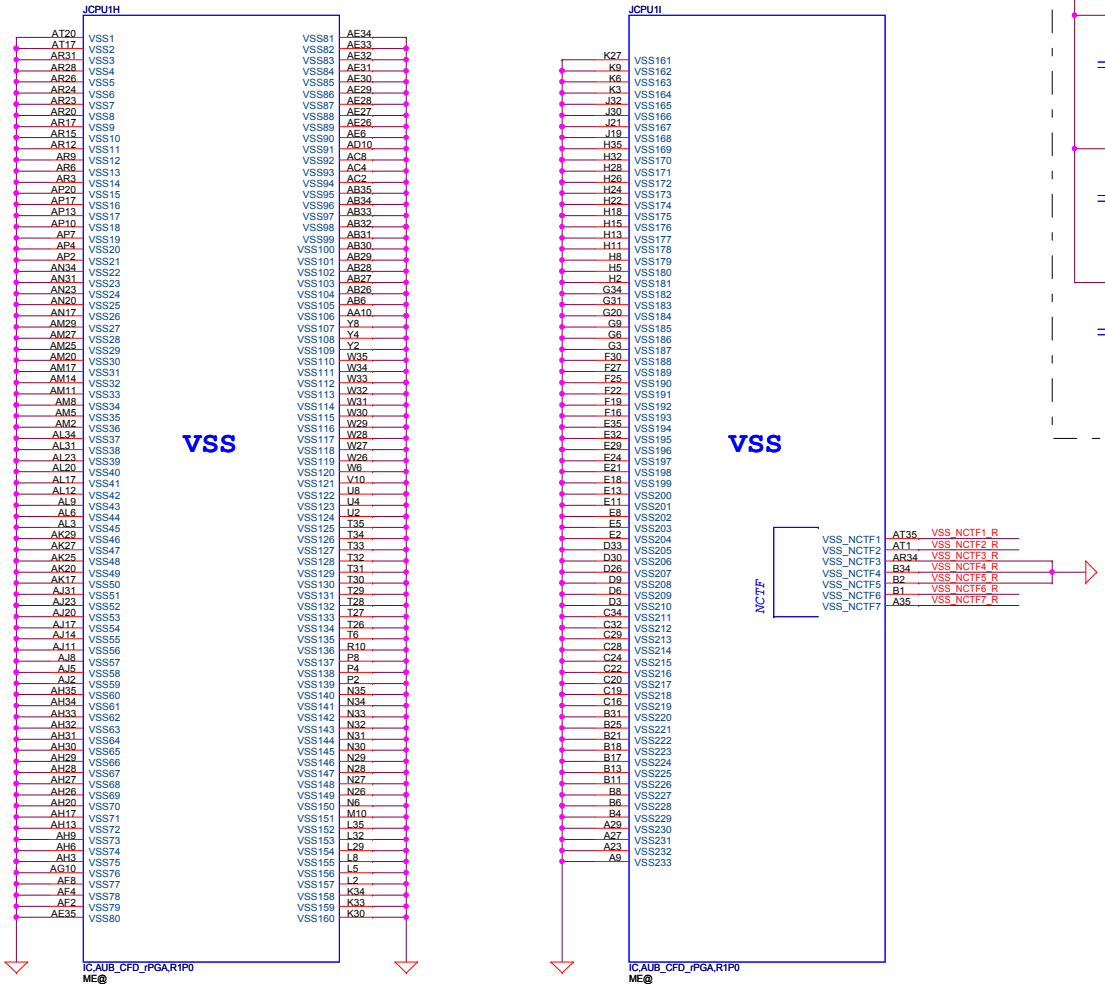

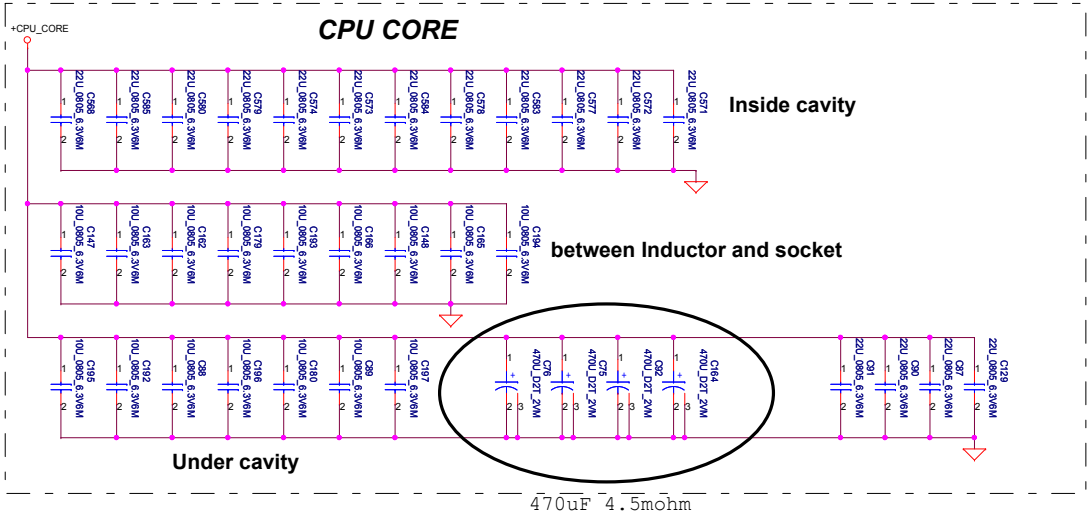

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: *Arrandale(5/5)-GND/Bypass*

Size	Document Number	Rev
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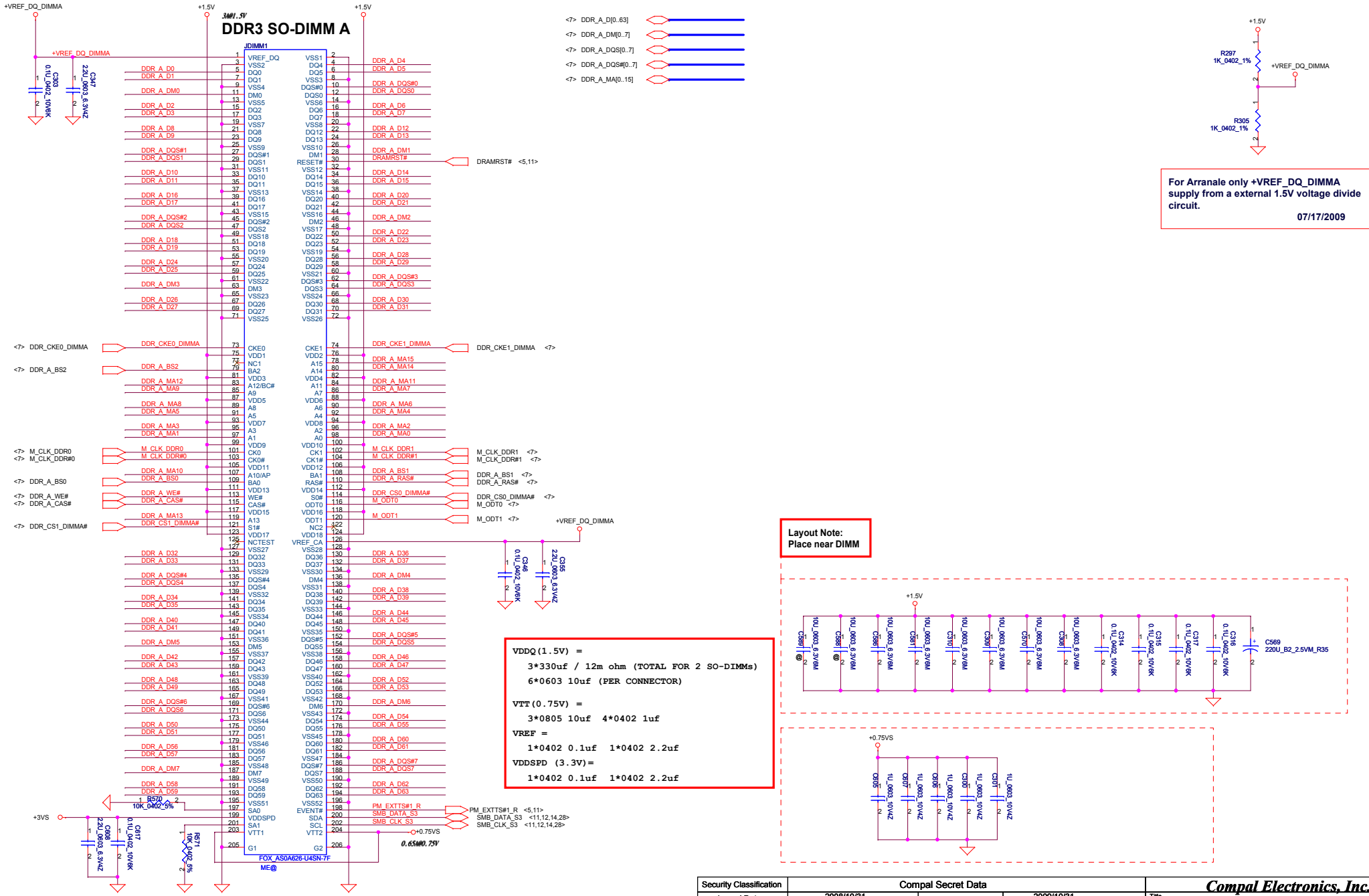

Security Classification	Compal Secret Data		
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Title: DDRIII-SODIMM SLOT1

Size	Document Number	Rev
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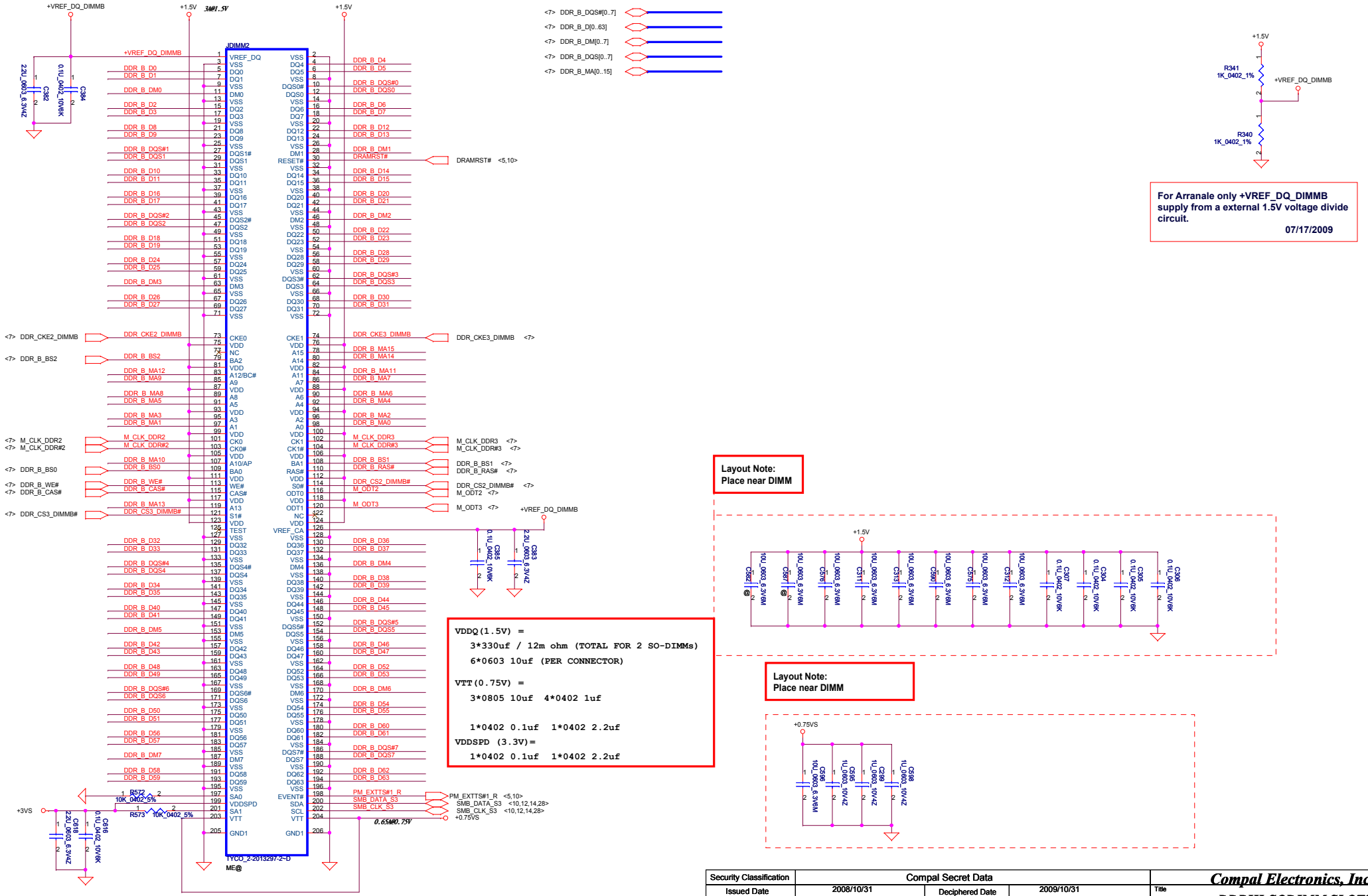

For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.

07/17/2009

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

```
VDDQ(1.5V) =
  3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
  6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
  3*0805 10uf  4*0402 1uf

  1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
  1*0402 0.1uf  1*0402 2.2uf
```

Security Classification	Compal Secret Data		
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Title: **DDRIII-SODIMM SLOT2**

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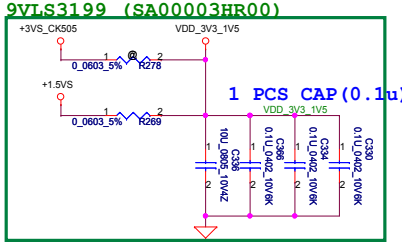
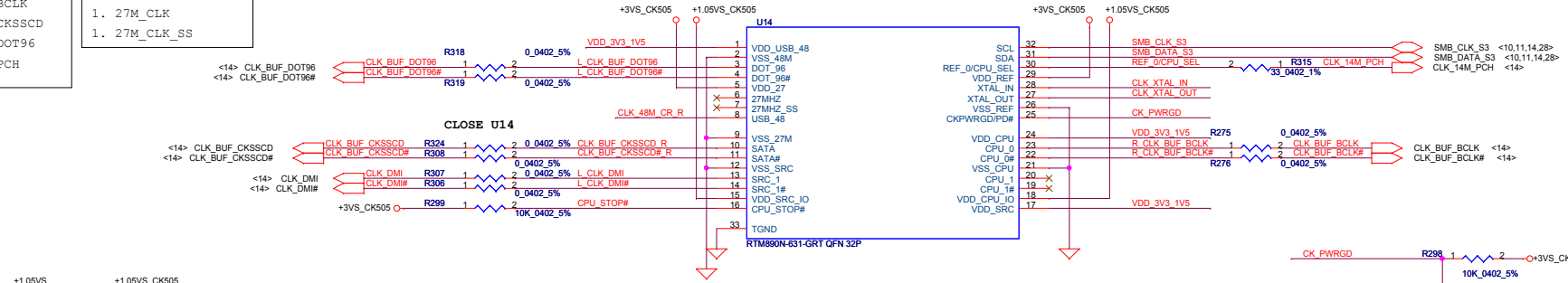
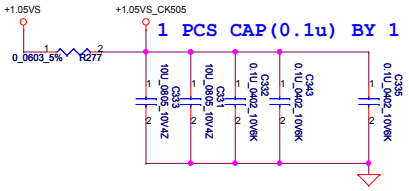
Reserve for Low Power CLK GEN.
RTM890N-631(SA00003HQ00)
SLG8LV597VTR
9VLS3199 (SA00003HR00)



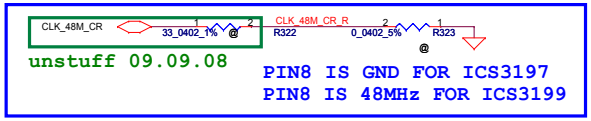
CLK GEN TO PCH
1. CLK_DMI
2. CLK_BUF_BCLK
3. CLK_BUF_CKSSCD
4. CLK_BUF_DOT96
5. CLK_14M_PCH

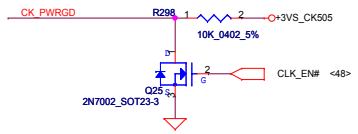
CLK GEN TO VGA
Unused
1. 27M_CLK
1. 27M_CLK_SS

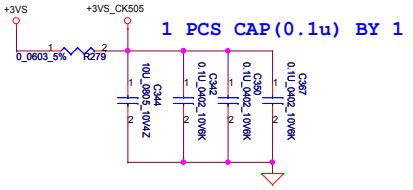


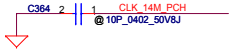


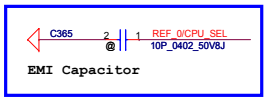
S IC SLG8SP587VTR QFN 32P CLK GEN (SA00002XY00)
S IC ICS9LRS3199AKLFT MLF 32P CLK GEN (SA000030P00)

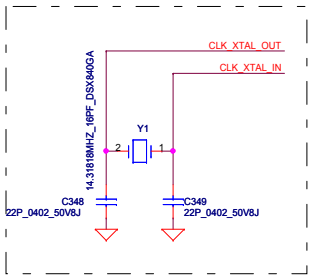




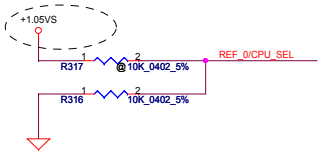








PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: CLOCK GENERATOR

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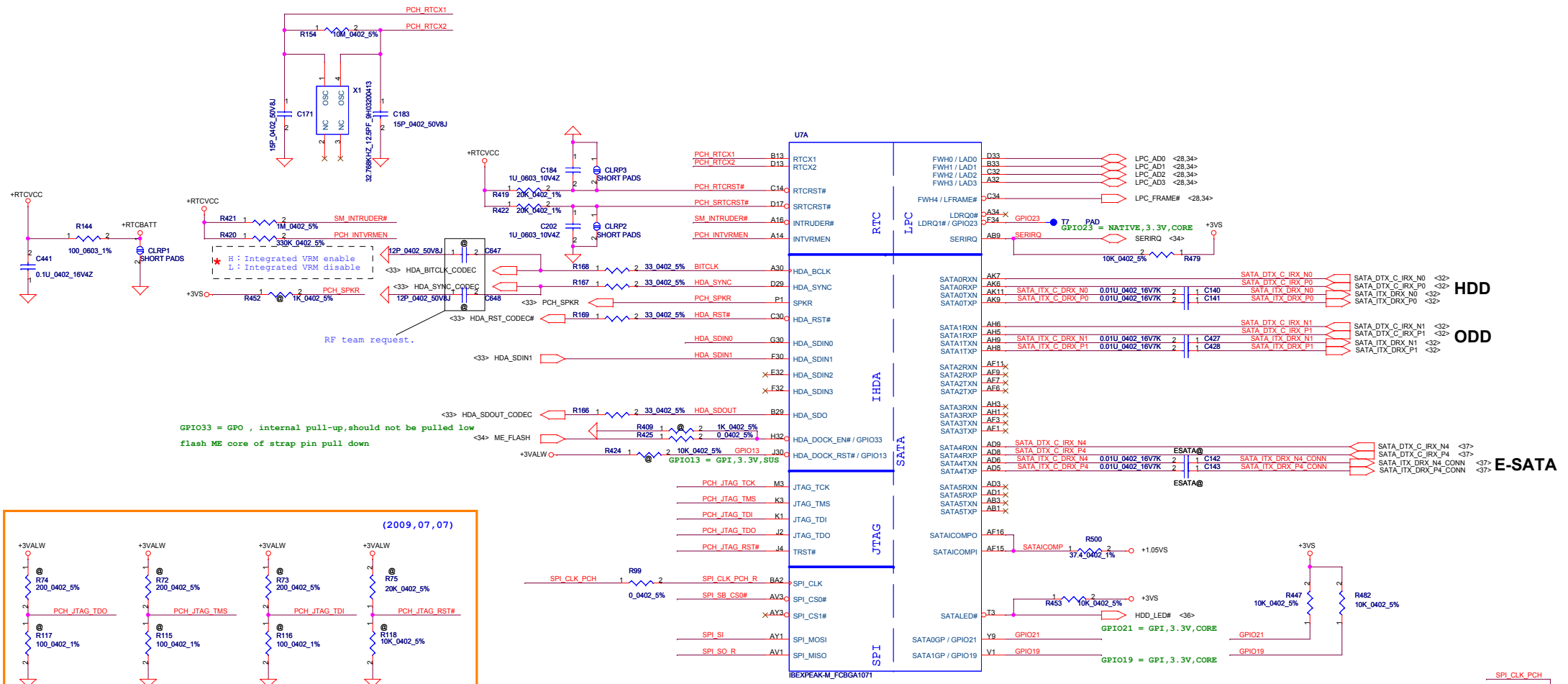

PCH Pin	RefDes	PCH JTAG Pre-Production ES1	PCH JTAG Pre-Production ES2	PCH JTAG Production * MP
PCH_JTAG_TDO	R591	No Install	200ohm	No Install
	R590	No Install	100ohm	No Install
PCH_JTAG_TMS	R584	200ohm	200ohm	No Install
	R583	100ohm	100ohm	No Install
PCH_JTAG_TDI	R587	200ohm	200ohm	No Install
	R586	100ohm	100ohm	No Install
PCH_JTAG_TCK	R580	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R595	20Kohm	20Kohm	No Install
	R594	10Kohm	10Kohm	No Install

PCH_JTAG_TCK R114 51_0402_5% (2009,05,04)

FOR INTEL DPDG REV1.6 (MAY 2009)

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: IBEX-M(1/6)-HDA/JTAG/SATA

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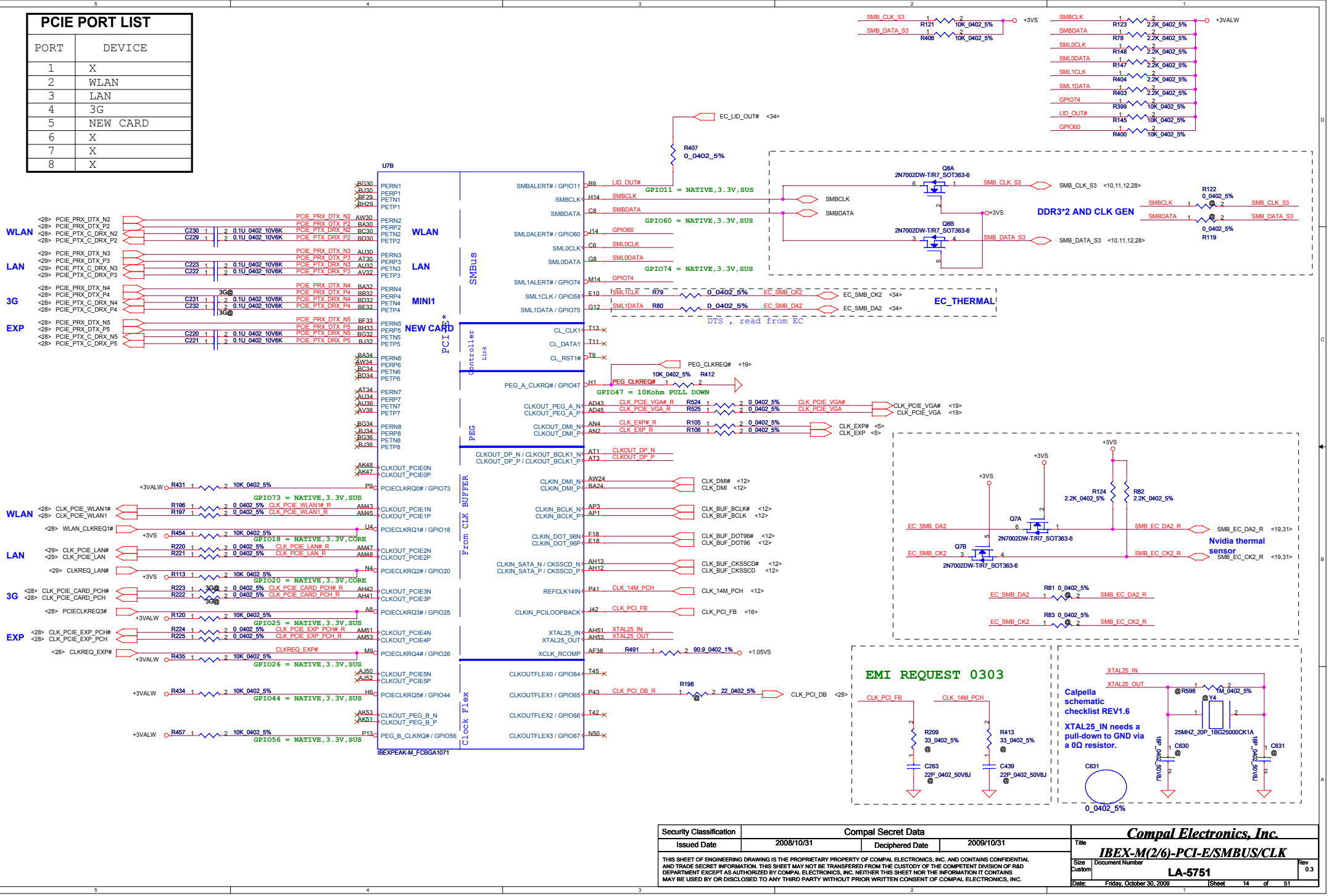
PCIE PORT LIST

PORT	DEVICE
1	X
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	X
7	X
8	X



Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: IBEX-M(2/6)-PCI-E/SMBUS/CLK

Size: Custom | Document Number: LA-5751 | Rev: 0.3

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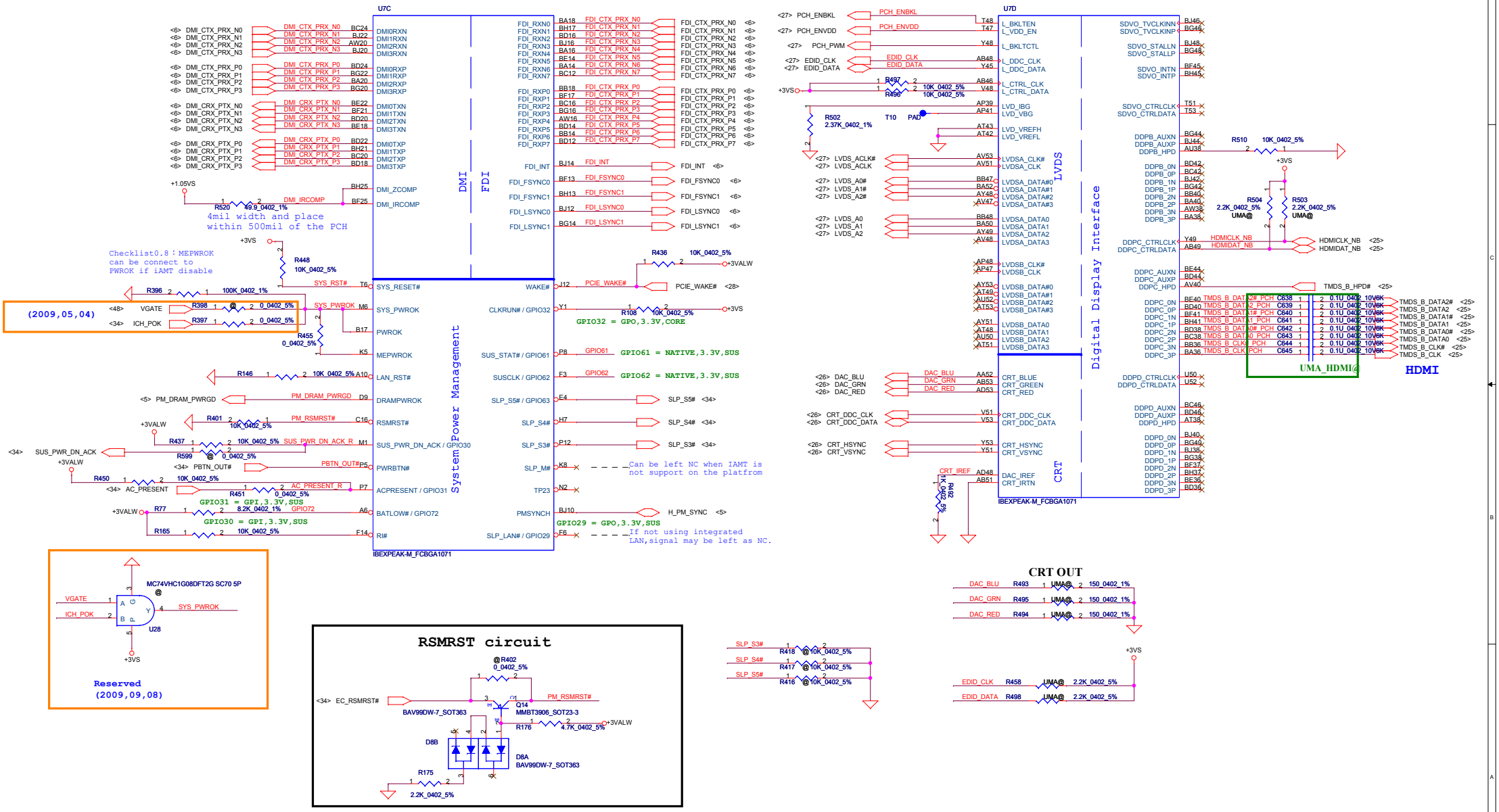

Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: IBEX-M(3/6)-DMI/GPIO/LVDS

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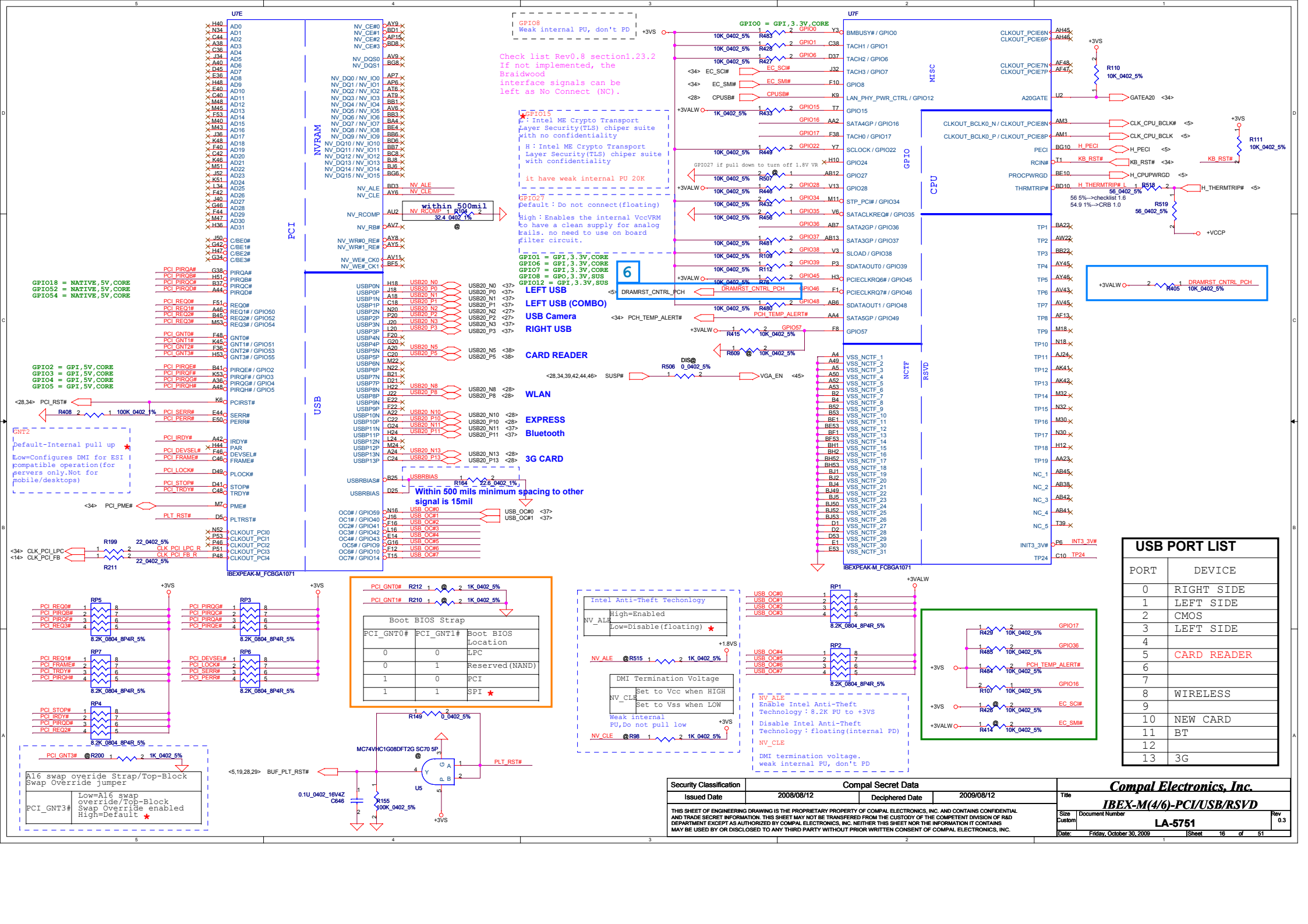
U7E
U7F
PCI
NVRAM
USB
GPIO
MISC
CPU
NCTF
RSVD
IBEXPEAK-M_FCBGA1071
LEFT USB
LEFT USB (COMBO)
USB Camera
RIGHT USB
CARD READER
WLAN
EXPRESS
Bluetooth
3G CARD
Within 500 mils minimum spacing to other signal is 15mil
Check list Rev0.8 section1.23.2
If not implemented, the Braidwood interface signals can be left as No Connect (NC).
GPIO0 = GPI,3.3V,CORE
GPIO1 = GPI,3.3V,CORE
GPIO6 = GPI,3.3V,CORE
GPIO7 = GPI,3.3V,CORE
GPIO8 = GPO,3.3V,SUS
GPIO12 = GPI,3.3V,SUS
GPIO18 = NATIVE,5V,CORE
GPIO52 = NATIVE,5V,CORE
GPIO54 = NATIVE,5V,CORE
GPIO2 = GPI,5V,CORE
GPIO3 = GPI,5V,CORE
GPIO4 = GPI,5V,CORE
GPIO5 = GPI,5V,CORE
Boot BIOS Strap
PCI_GNT0# | PCI_GNT1# | Boot BIOS Location
0 | 0 | LPC
0 | 1 | Reserved(NAND)
1 | 0 | PCI
1 | 1 | SPI
Intel Anti-Theft Techonlogy
NV_ALE: High=Enabled; Low=Disable(floating)
DMI Termination Voltage
NV_CLE: Set to Vcc when HIGH; Set to Vss when LOW
A16 swap overide Strap/Top-Block Swap Override jumper
PCI_GNT3#: Low=A16 swap override/Top-Block Swap Override enabled; High=Default
USB PORT LIST
PORT | DEVICE
0 | RIGHT SIDE
1 | LEFT SIDE
2 | CMOS
3 | LEFT SIDE
4 |
5 | CARD READER
6 |
7 |
8 | WIRELESS
9 |
10 | NEW CARD
11 | BT
12 |
13 | 3G
Security Classification: Compal Secret Data
Issued Date: 2008/08/12
Deciphered Date: 2009/08/12
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Compal Electronics, Inc.
Title: IBEX-M(4/6)-PCI/USB/RSVD
Size: Custom
Document Number: LA-5751
Rev: 0.3
Date: Friday, October 30, 2009
Sheet 16 of 51

DG1.1 no M3 support and not Intel LAN, VCCLAN Source=>GND

POWER

U7J

IBEXPEAK-M_FCBGA1071

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

CPU

RTC

HDA

UPDATE 0210

lsolate AF32,AF34,AH34 from AH35,AJ35 for Intel request 09.09.08

POWER

U7G

IBEXPEAK-M_FCBGA1071

VCC CORE

CRT

LVDS

HVCMOS

DMI

PCI E*

NAND / SPI

FDI

0.1uH inductor, 200mA

10uH inductor, 120mA

C447 changed to 1u 09/04/2009 check list Rev2.0 update.

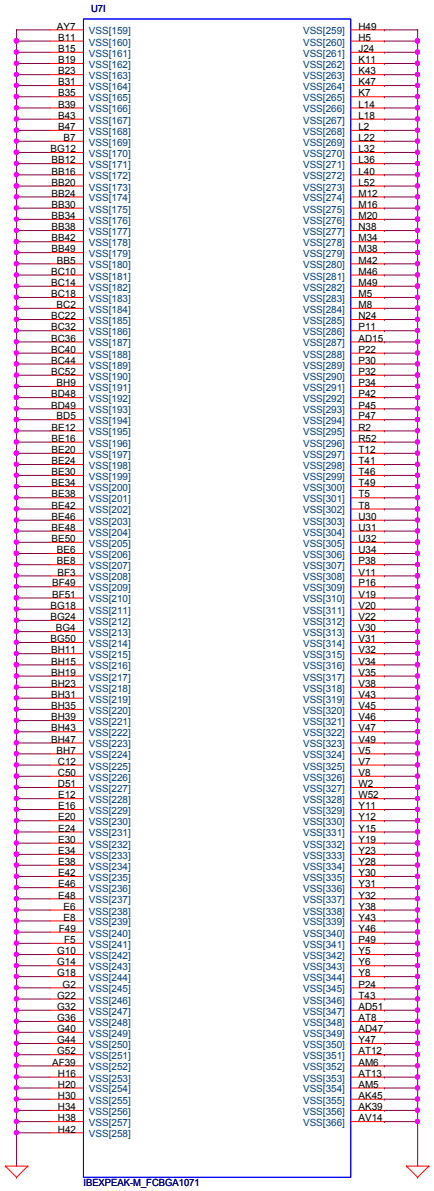
Security Classification	Compal Secret Data		
Issued Date	2008/08/12	Deciphered Date	2009/08/12

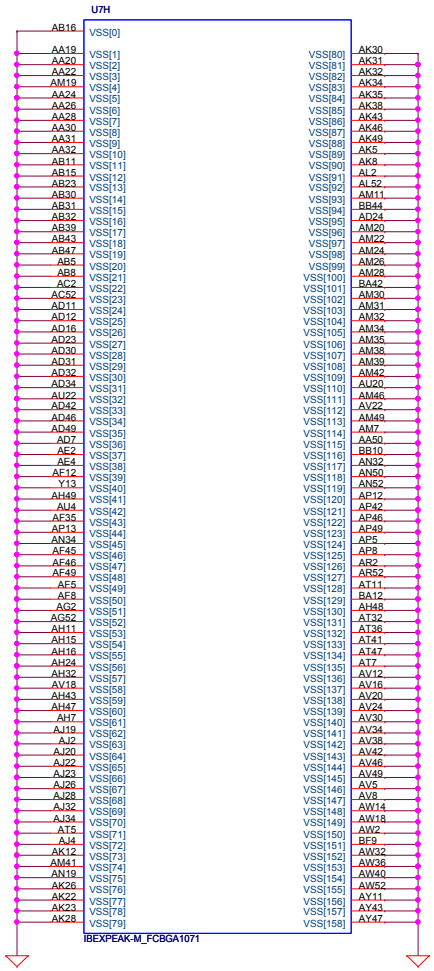
Compal Electronics, Inc.

Title: IBEX-M(5/6)-PWR

Size: Custom | Document Number: LA-5751 | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 17 of 51





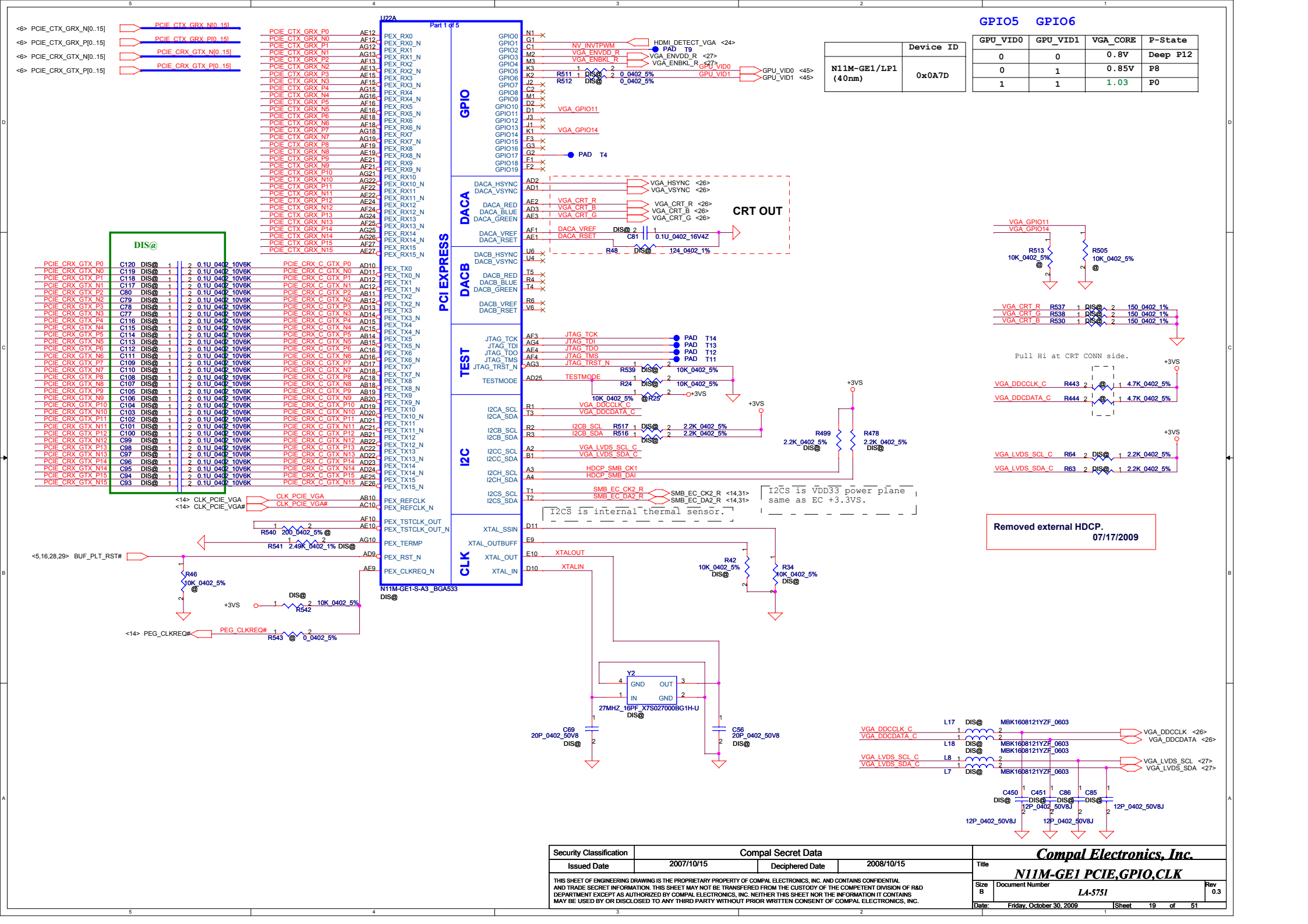
Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: **IBEX-M(6/6)-GND**

Size	Document Number	Rev
Custom	LA-5751	0.3

Date: Thursday, October 29, 2009 | Sheet 18 of 51


GPIO5 GPIO6
Device ID
N11M-GE1/LP1 (40nm)
0x0A7D
GPU_VID0 | GPU_VID1 | VGA_CORE | P-State
0 | 0 | 0.8V | Deep P12
0 | 1 | 0.85V | P8
1 | 1 | 1.03 | P0
U22A
Part 1 of 5
PCI EXPRESS
GPIO
DACA
DACB
TEST
I2C
CLK
CRT OUT
DIS@
N11M-GE1-S-A3 _BGA533
I2CS is internal thermal sensor.
I2CS is VDD33 power plane same as EC +3.3VS.
Removed external HDCP.
07/17/2009
Pull Hi at CRT CONN side.
Y2
27MHZ_16PF_X7S027000BG1H-U
Security Classification
Compal Secret Data
Issued Date
2007/10/15
Deciphered Date
2008/10/15
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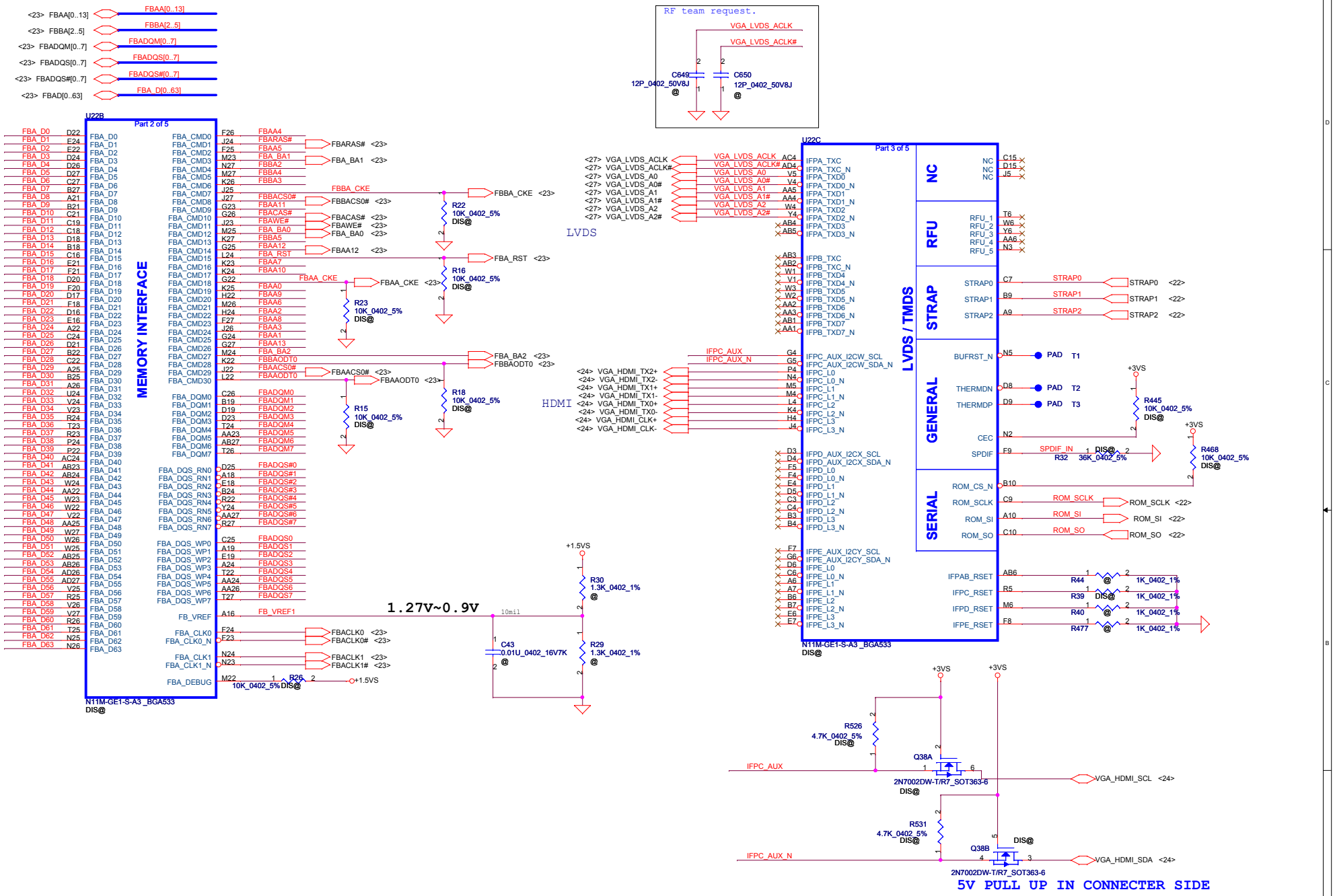
Compal Electronics, Inc.
Title
N11M-GE1 PCIE,GPIO,CLK
Size B
Document Number
LA-5751
Rev 0.3
Date: Friday, October 30, 2009
Sheet 19 of 51



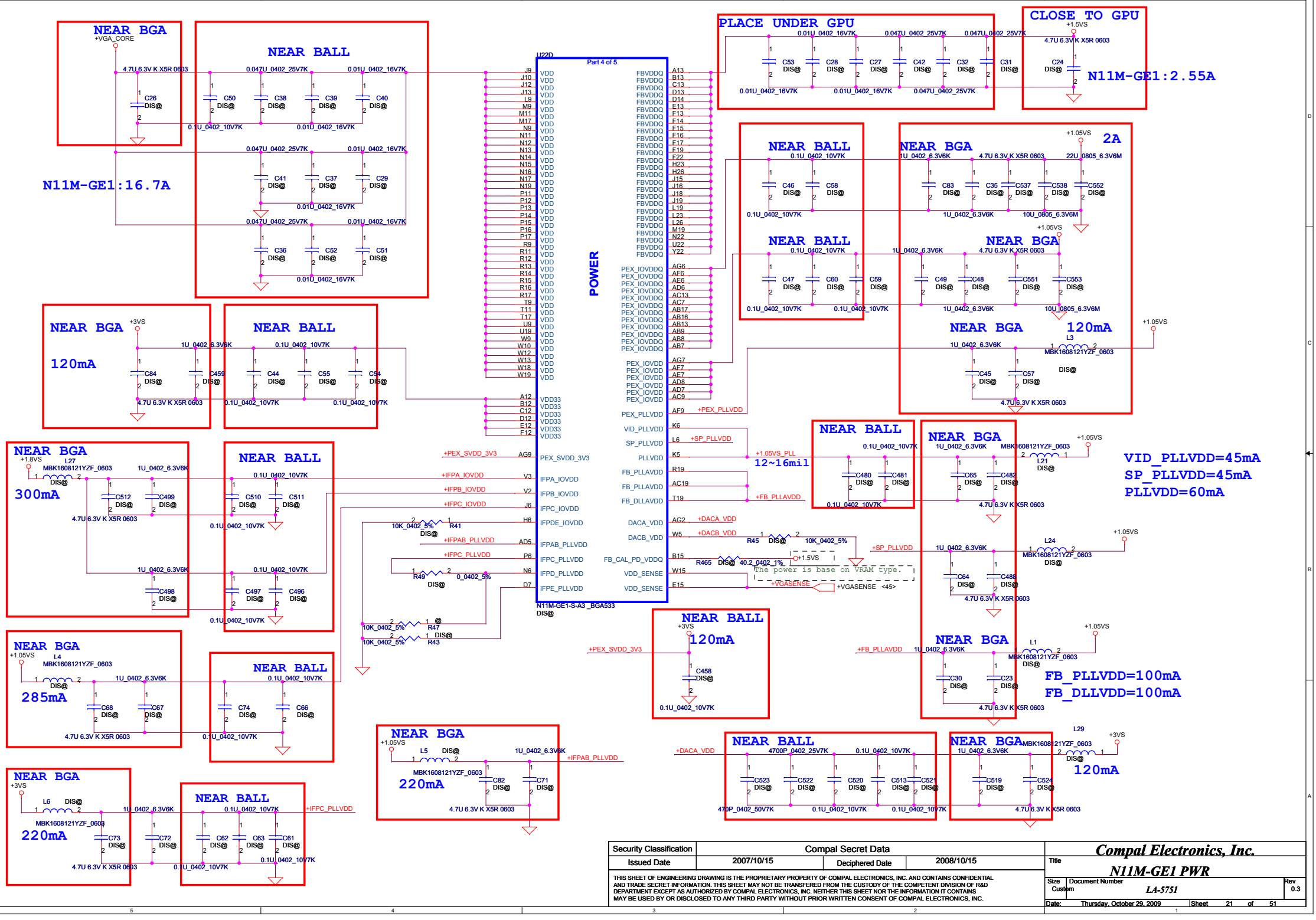
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: N11M-GE1 LVDS,Memory Bus

Size	Document Number	Rev
B	LA-5751	0.3

Date: Friday, October 30, 2009 Sheet 20 of 51



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

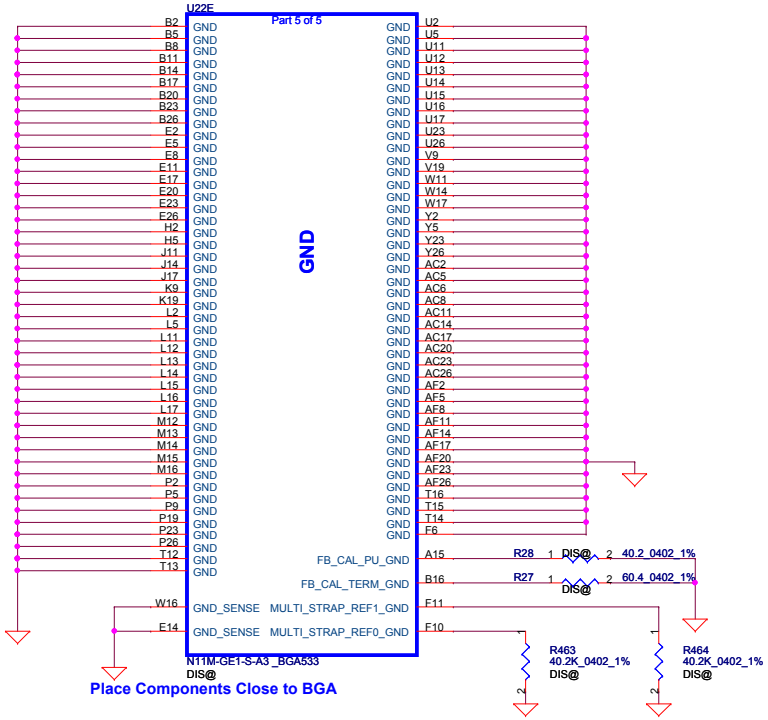
Compal Electronics, Inc.

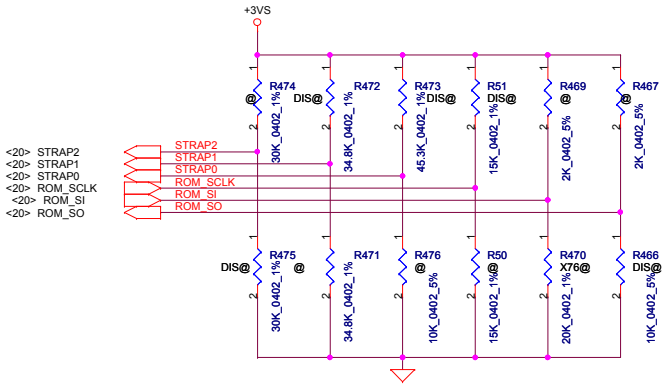
Title: *N11M-GE1 PWR*

Size	Document Number	Rev
Custom	*LA-5751*	0.3

Date: Thursday, October 29, 2009 | Sheet 21 of 51

A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available





STRAP1 use for 3GIO_PADCFG to set 35K pull up.
(PUN-04335-001_V10 HW9 update)

N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

Must be used 1% resister for driver calibration

DG-04642-001-V01(May 22, 2009)

GPU	FB Memory (DDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (defaul)	K4W1G1646E-HC12						
		64Mx16	PD 10K		PU 15K	PD 20K	PD 30K	PU 35K	PU 45K
	Hynix 800MHz	H5TQ1G63BFR-12C						
		64Mx16	PD 10K		PU 15K	PD 15K	PD 30K	PU 35K	PU 45K
						X76		

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

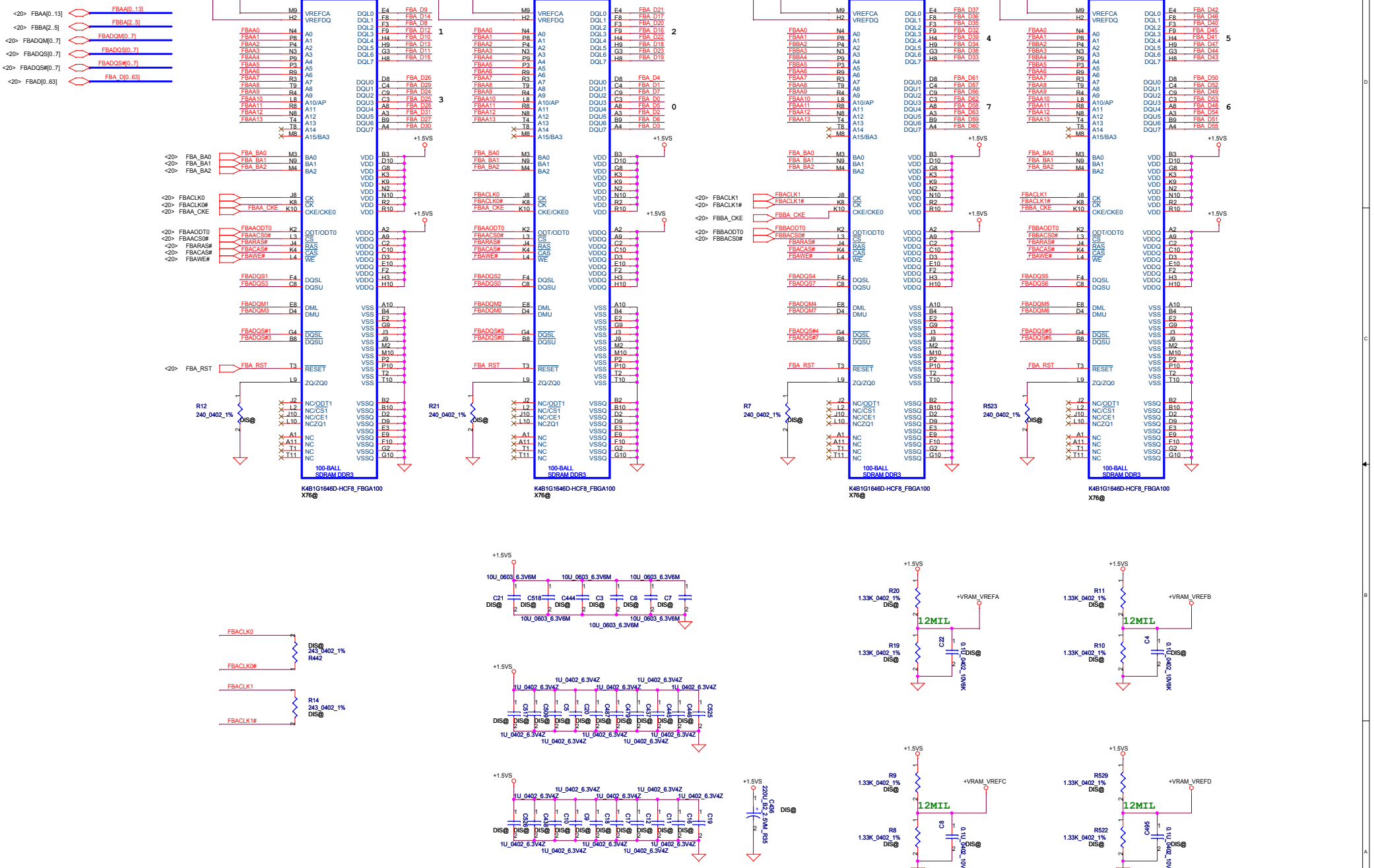
Compal Electronics, Inc.

Title: N11M-GE1 GND & STRAP

Size: B | Document Number: LA-5751 | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 22 of 51

N11x 40nm DDR3 MAPPING
NVIDIA COCUMENT FOR DA-3978-001



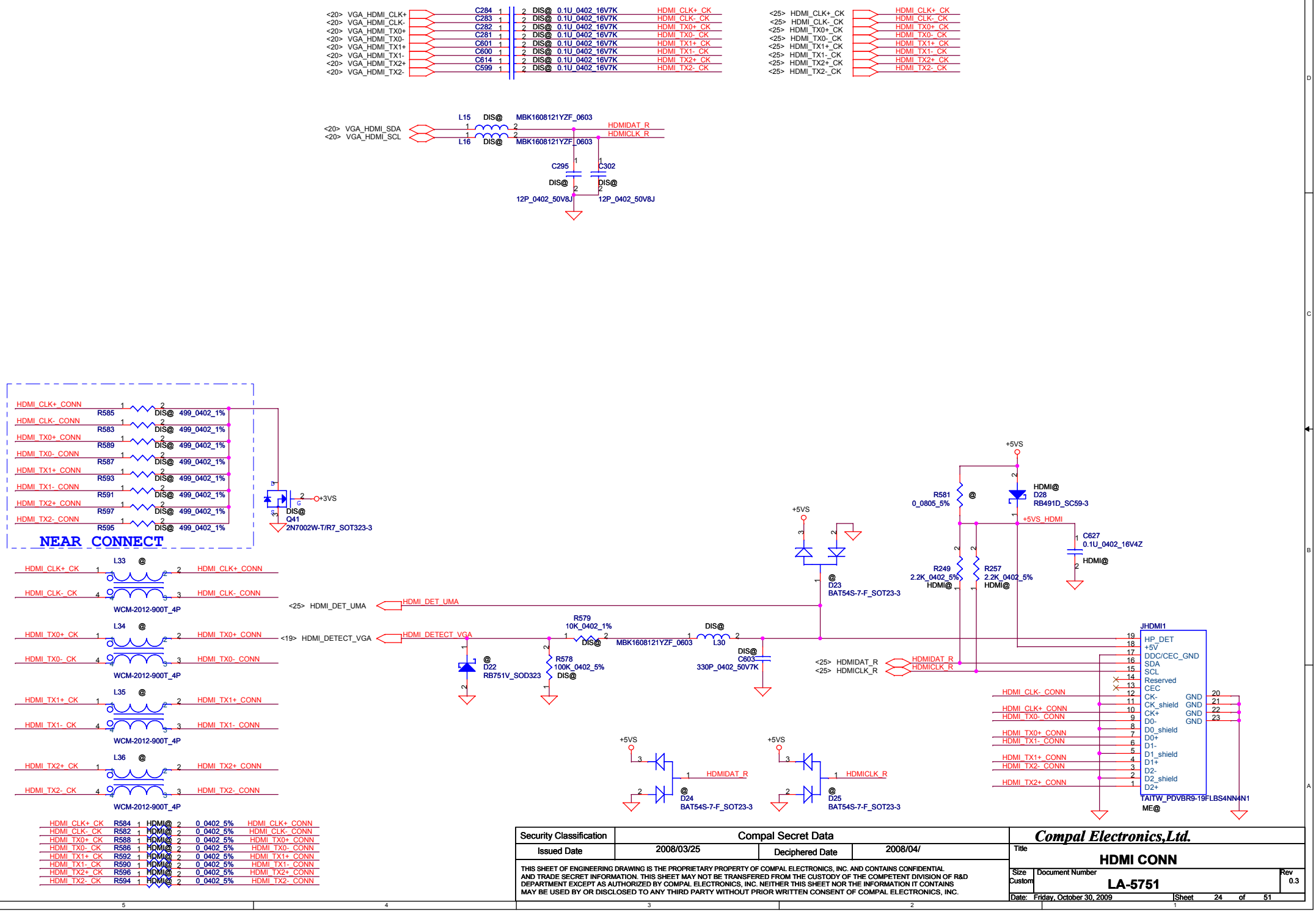
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **VRAM DDR3**

Size	Document Number	Rev
C	LA-5751	0.3

Date: Thursday, October 29, 2009 | Sheet 23 of 51



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

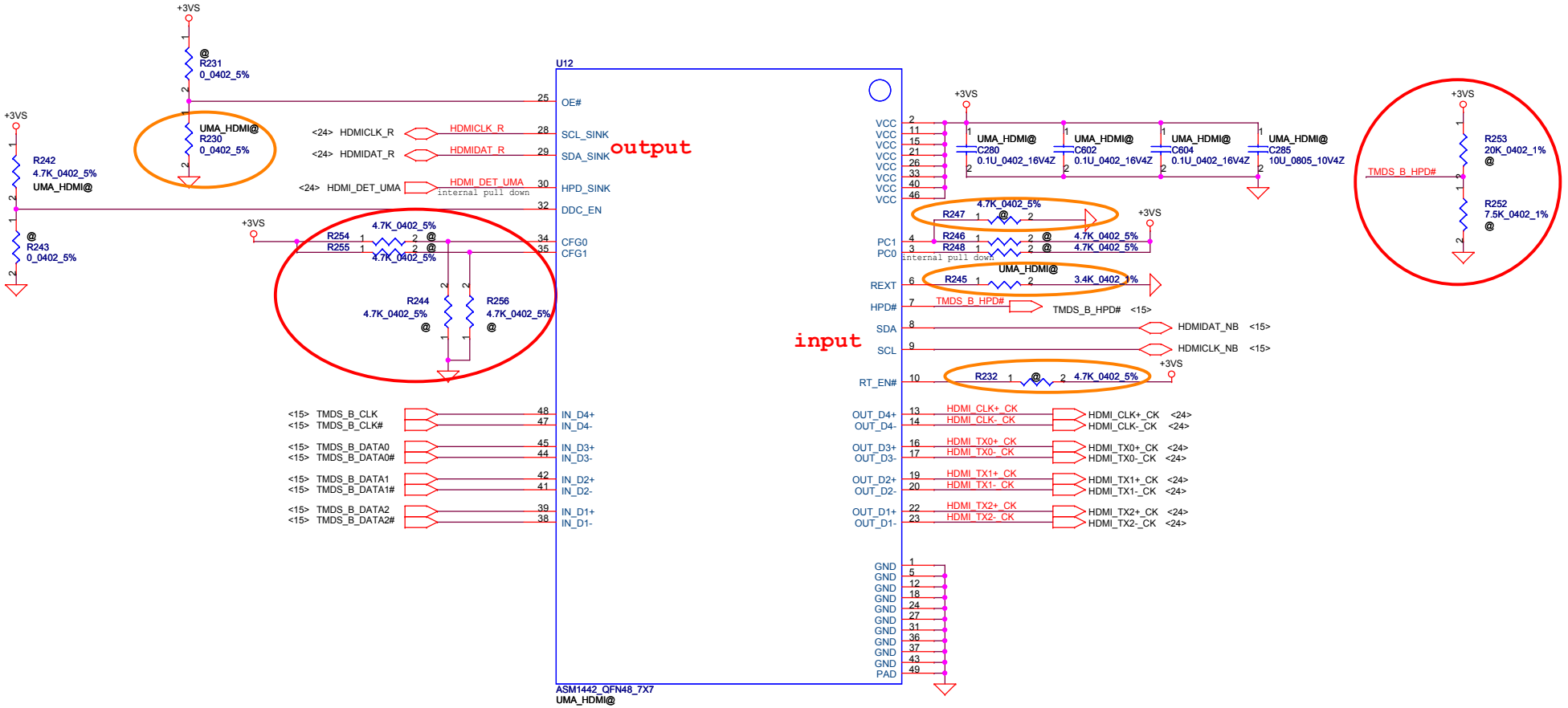
Compal Electronics,Ltd.
Title: HDMI CONN
Size: Custom
Document Number: LA-5751
Rev: 0.3
Date: Friday, October 30, 2009
Sheet 24 of 51

P/N:SA00003GT00 (ASM1442)

FOR asmedia R230 STUFF
RESERVE THE R232 PULL UP TO 3VS
RESERVE THE R247 PULL DOWN TO GND
CHANGE R245 FROM 499 TO 3.4K OHM

P/N:SA00002D700 (8101T)
P/N:SA00001U900 (CH7318A)

FOR 7318C PIN6 PULL DOWN 1.2Kohm
PIN7 PULL DOWN 7.5Kohm
PIN7 PULL UP 20Kohm



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

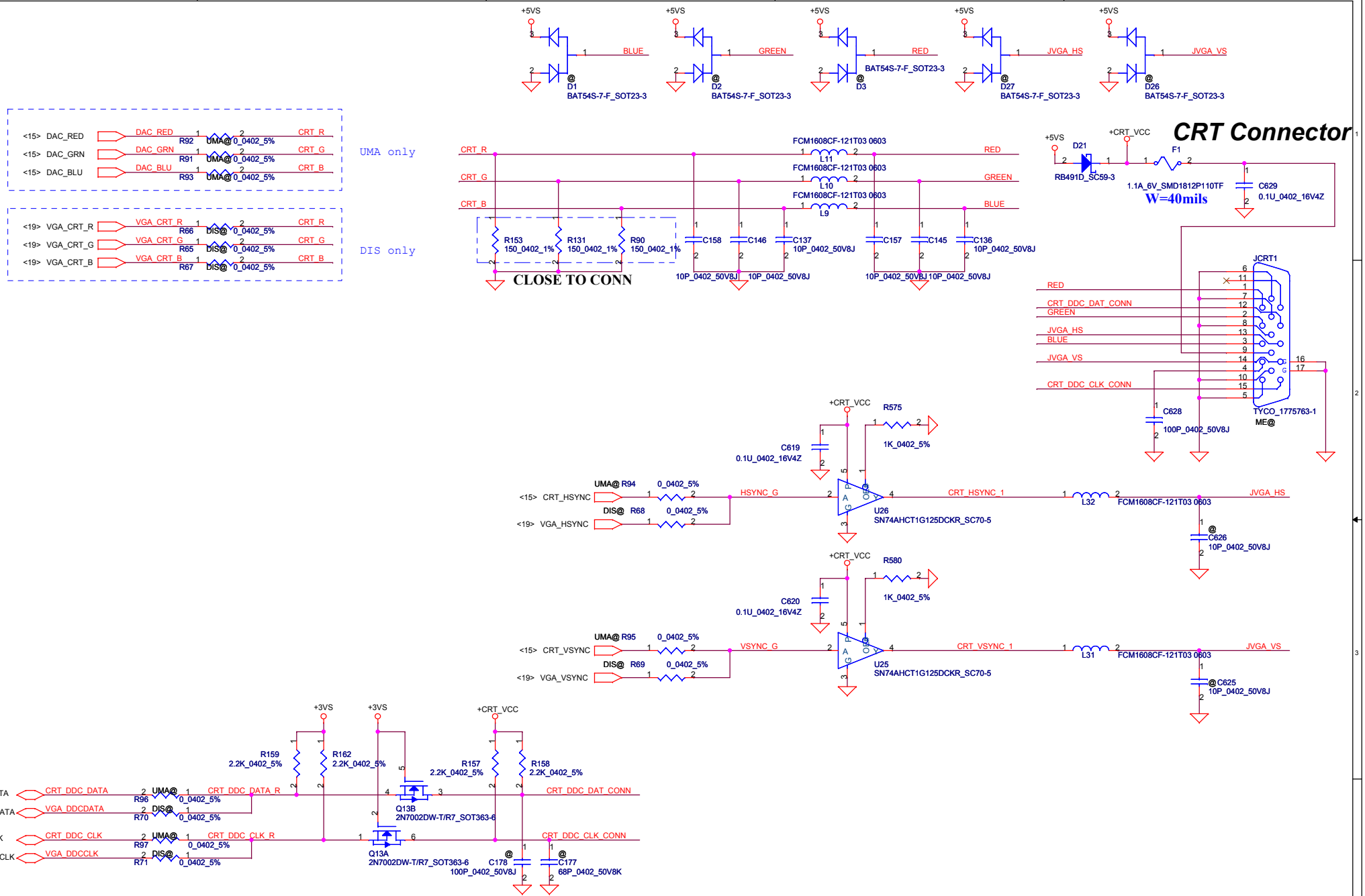
Compal Electronics,Ltd.

Title: Level Shiftter_ASM1442

Size: Custom | Document Number: LA-5751 | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 25 of 51

CRT Connector



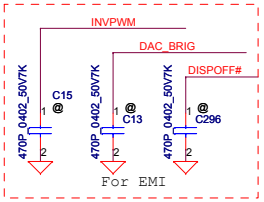
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

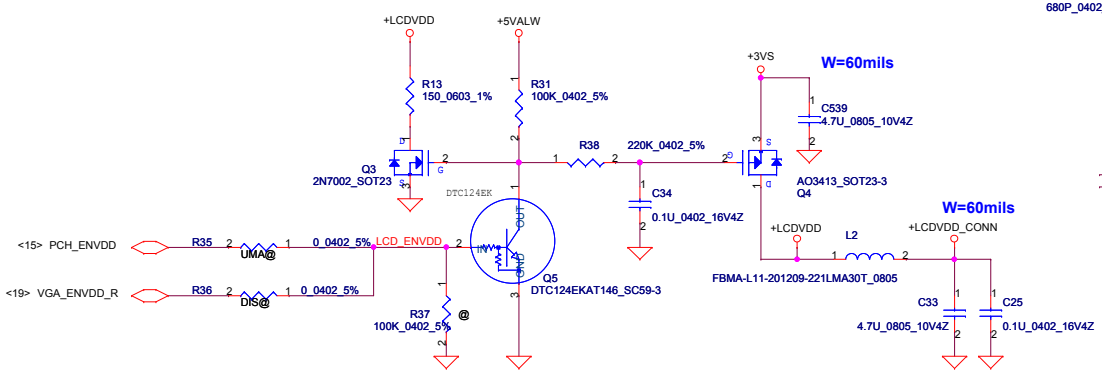
Title: CRT Connector

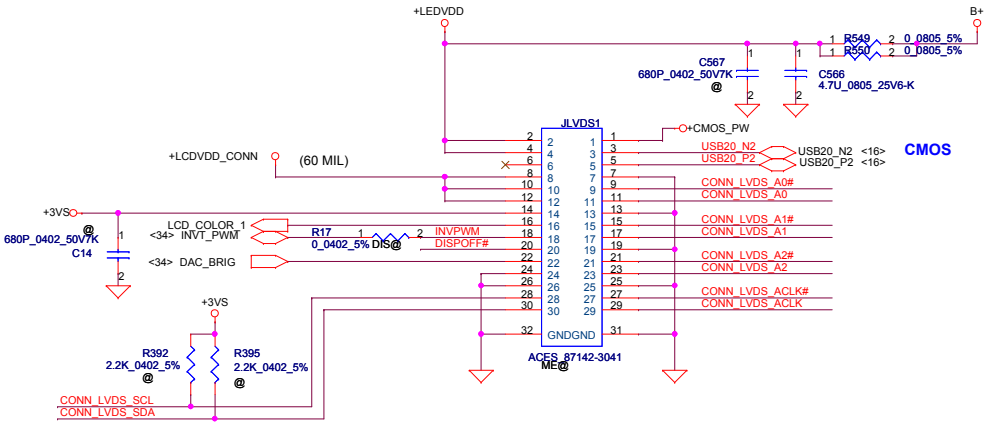
Size	Document Number	Rev
Custom	LA-5751	0.3

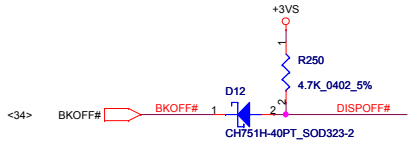
Date: Thursday, October 29, 2009 Sheet 26 of 51

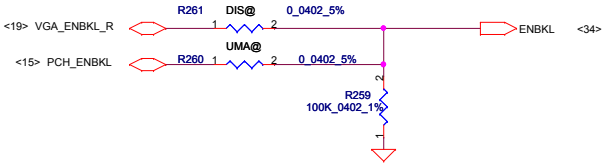


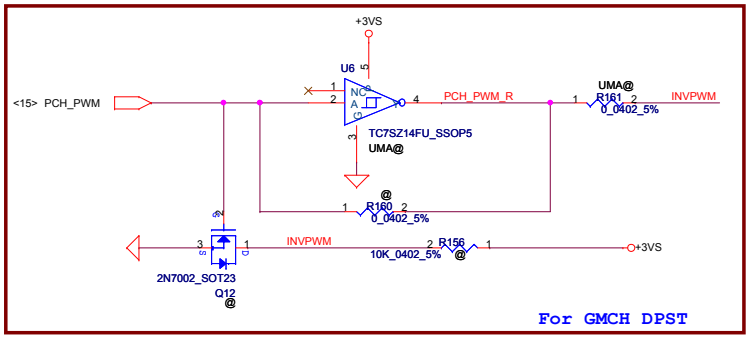
LCD POWER CIRCUIT



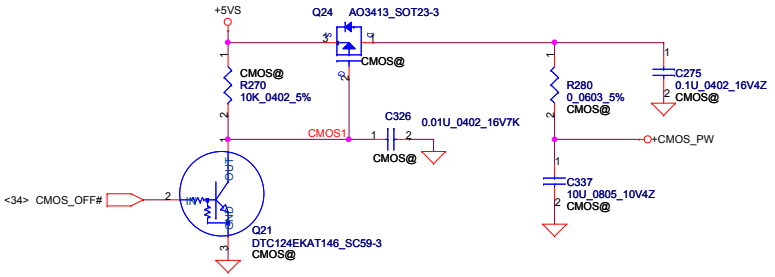


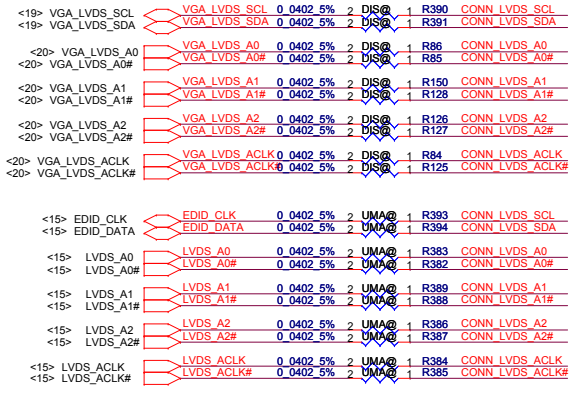






CMOS Camera



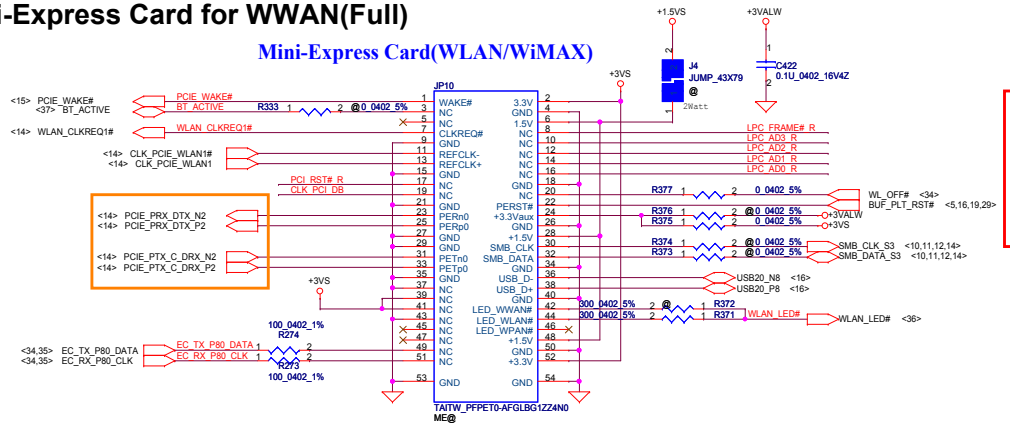


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

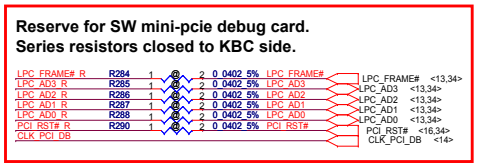
Compal Electronics, Inc.			
Title: LVDS/CAMERA			
Size: B	Document Number: LA-5751		Rev: 0.3
Date: Friday, October 30, 2009	Sheet 27 of 51		

Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for WWAN(Full)

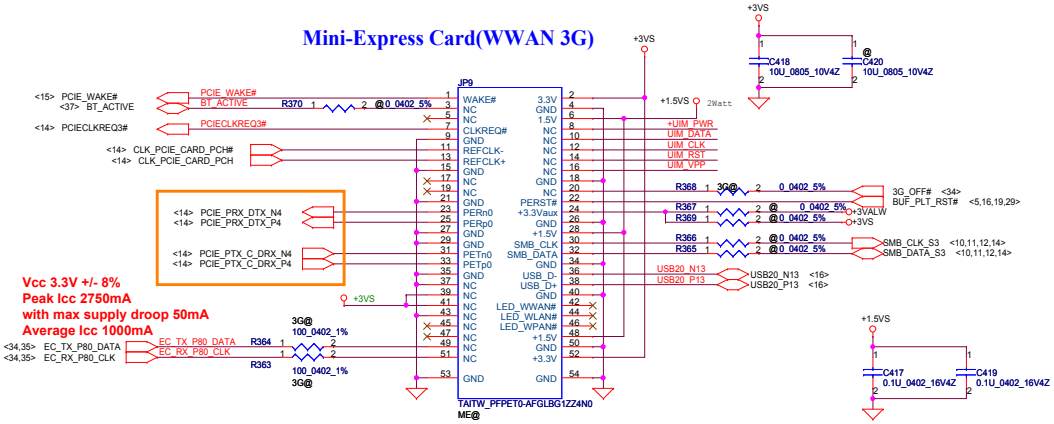
Mini-Express Card(WLAN/WiMAX)



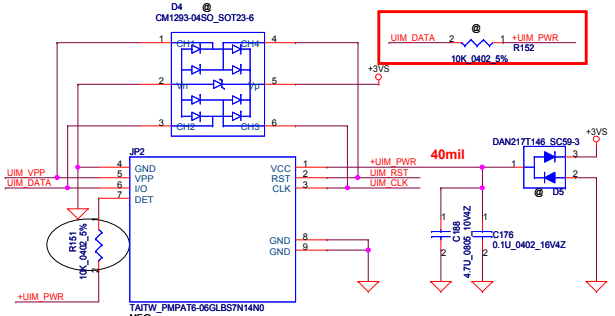
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



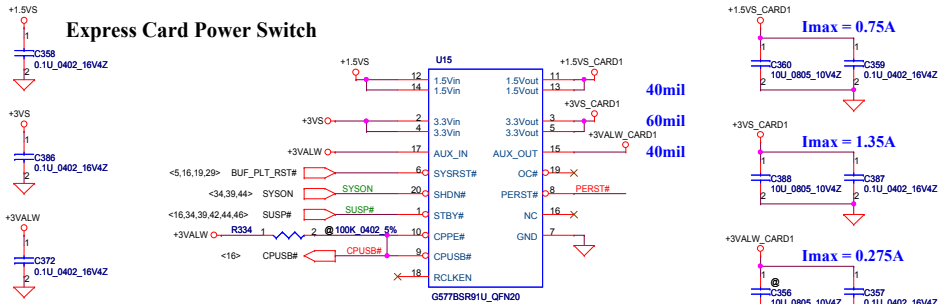
Mini-Express Card(WWAN 3G)



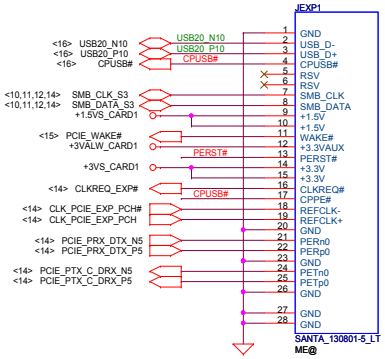
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA



Express Card Power Switch



New Card 34mm Socket (Left/TOP)



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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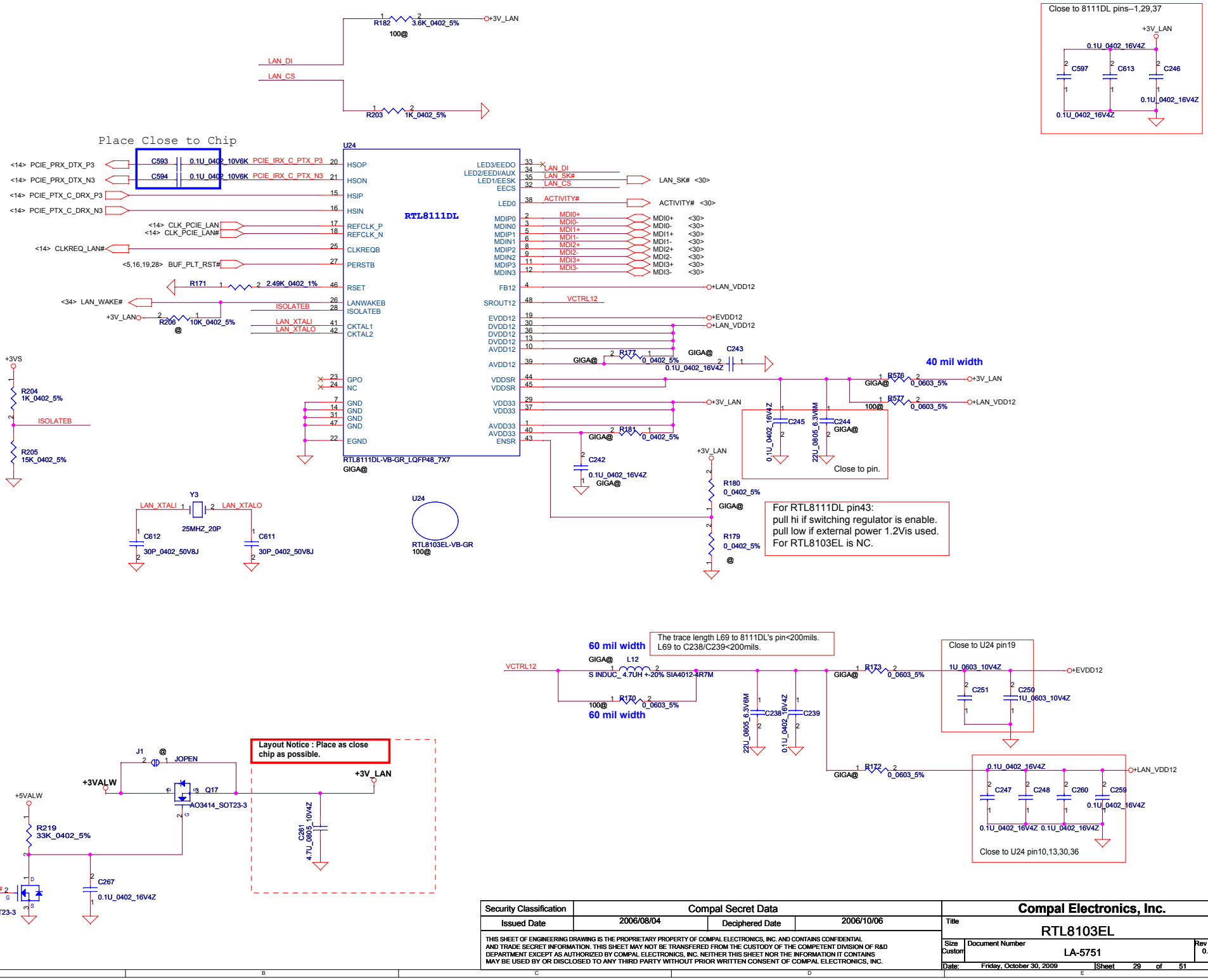
Compal Electronics, Inc.			
Title: Mini-Card/Nwe Card/SIM			
Size	Document Number: LA-5751		Rev: 0.3
Date: Friday, October 30, 2009		Sheet 28 of 51	



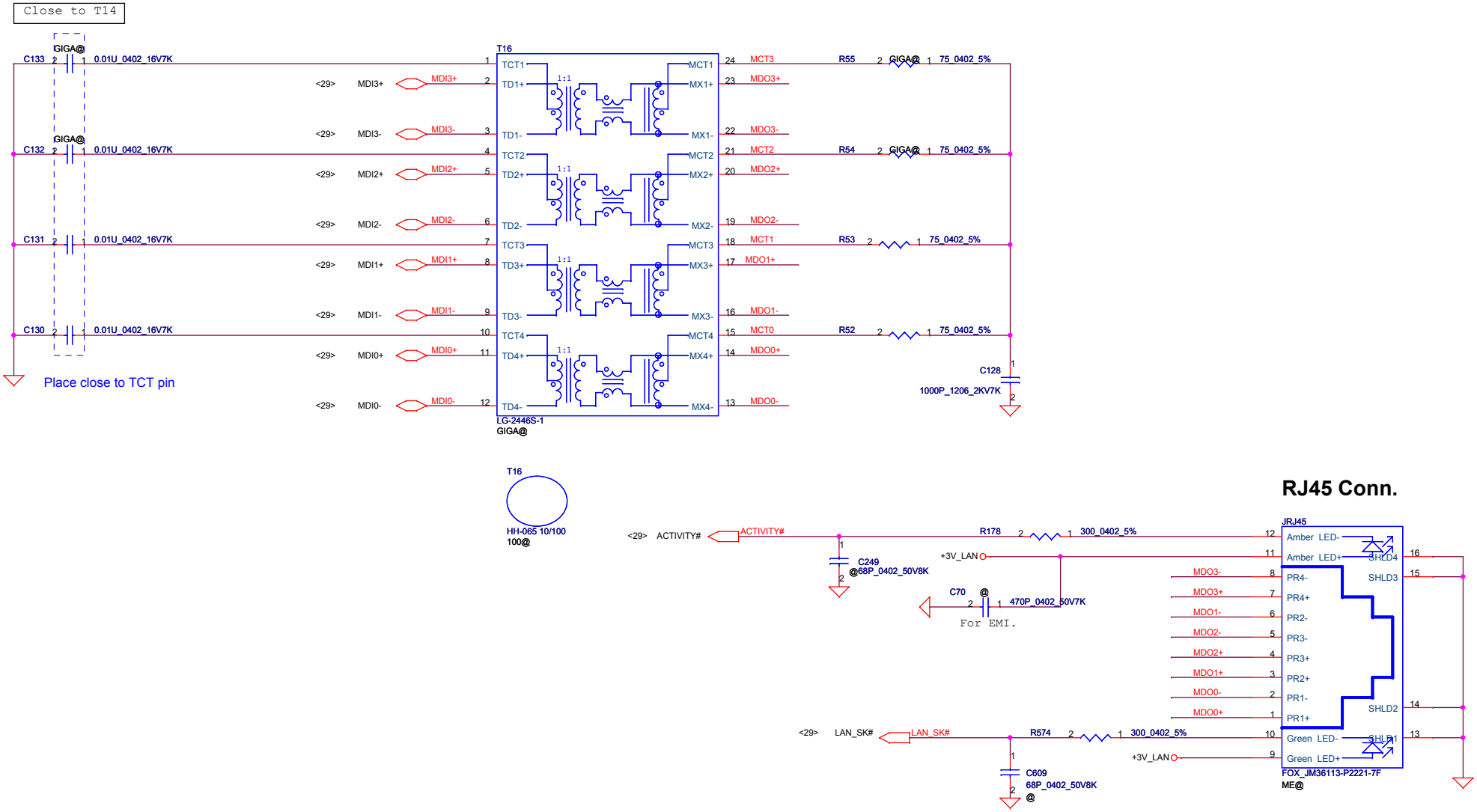
Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

Compal Electronics, Inc.

Title: RTL8103EL

Size	Document Number	Rev
Custom	LA-5751	0.3

Date: Friday, October 30, 2009 Sheet 29 of 51



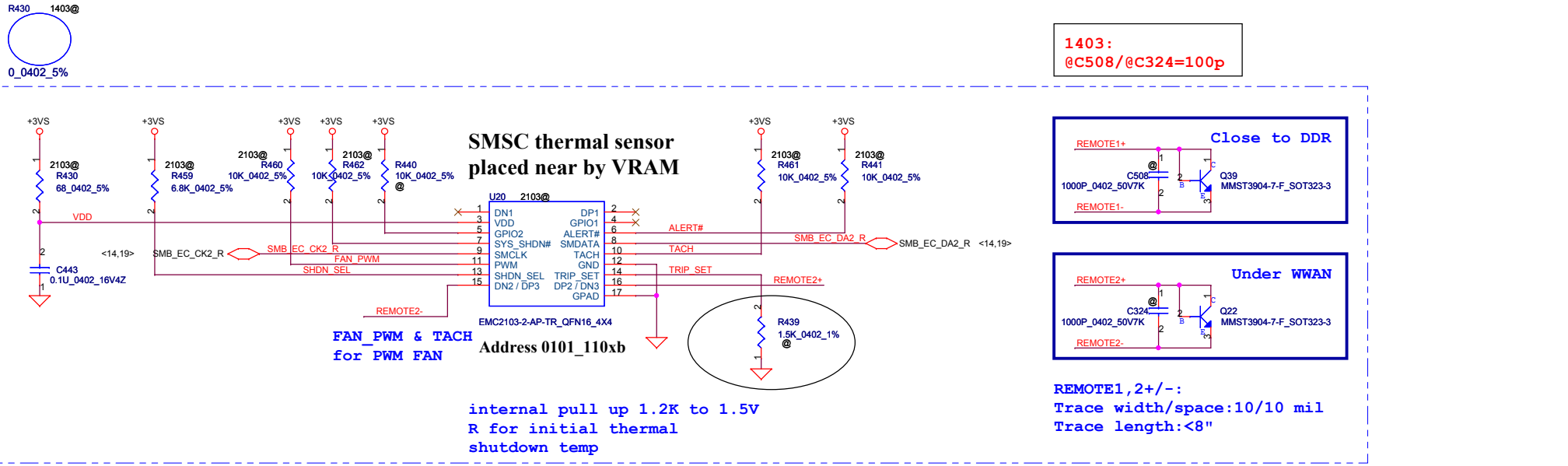
Security Classification	Compal Secret Data		
Issued Date	2009/03/20	Deciphered Date	2010/03/20

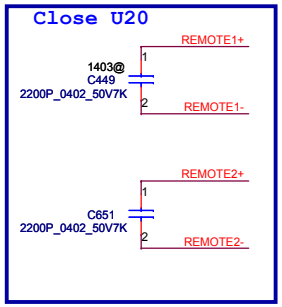
Compal Electronics, Inc.

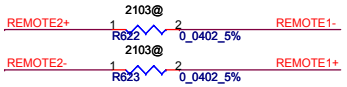
Title: **LAN_Transformer**

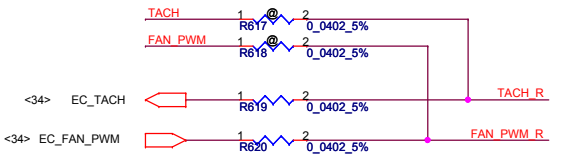
Size	Document Number	Rev
Custom	LA-5751	0.3

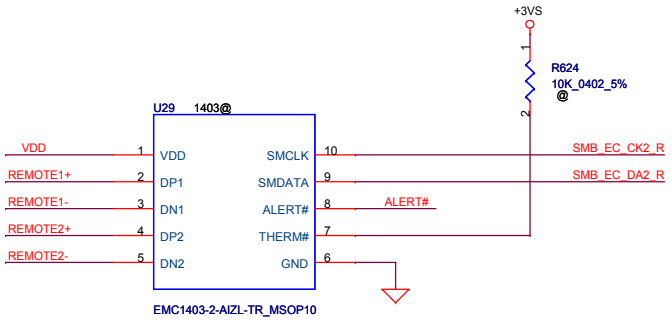
Date: Friday, October 30, 2009 Sheet 30 of 51

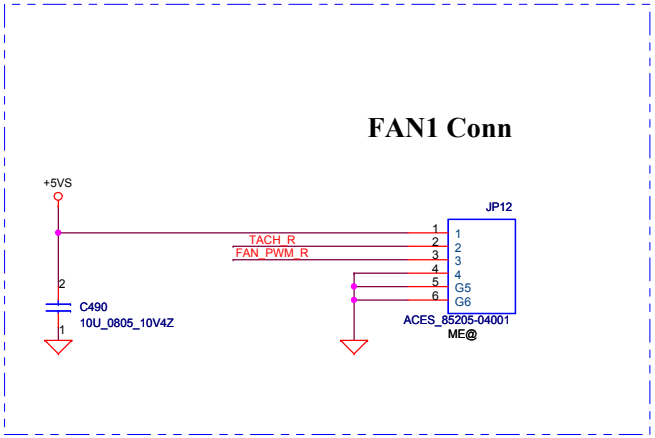












Shutdown Temp	TRIP_SET R439 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

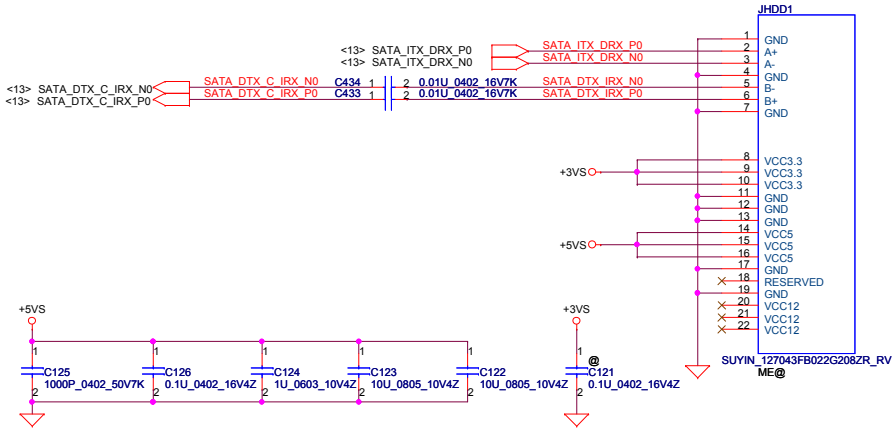
Compal Electronics,Ltd.

Title: EMC2103/1403_Thermal sensor/FAN

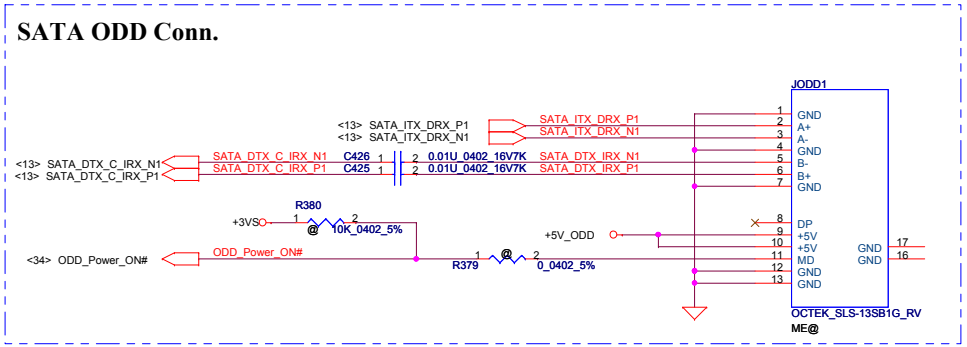
Size	Document Number	Rev
Custom	LA-5751	0.3

Date: Friday, October 30, 2009 Sheet 31 of 51

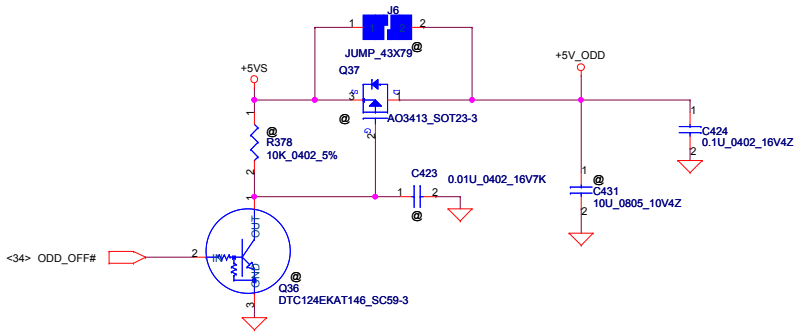
SATA HDD Conn.



SATA ODD Conn.



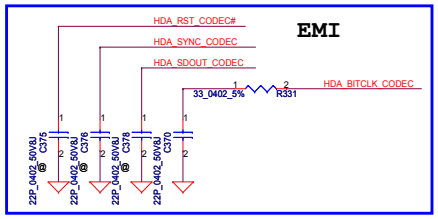
ODD Power Control

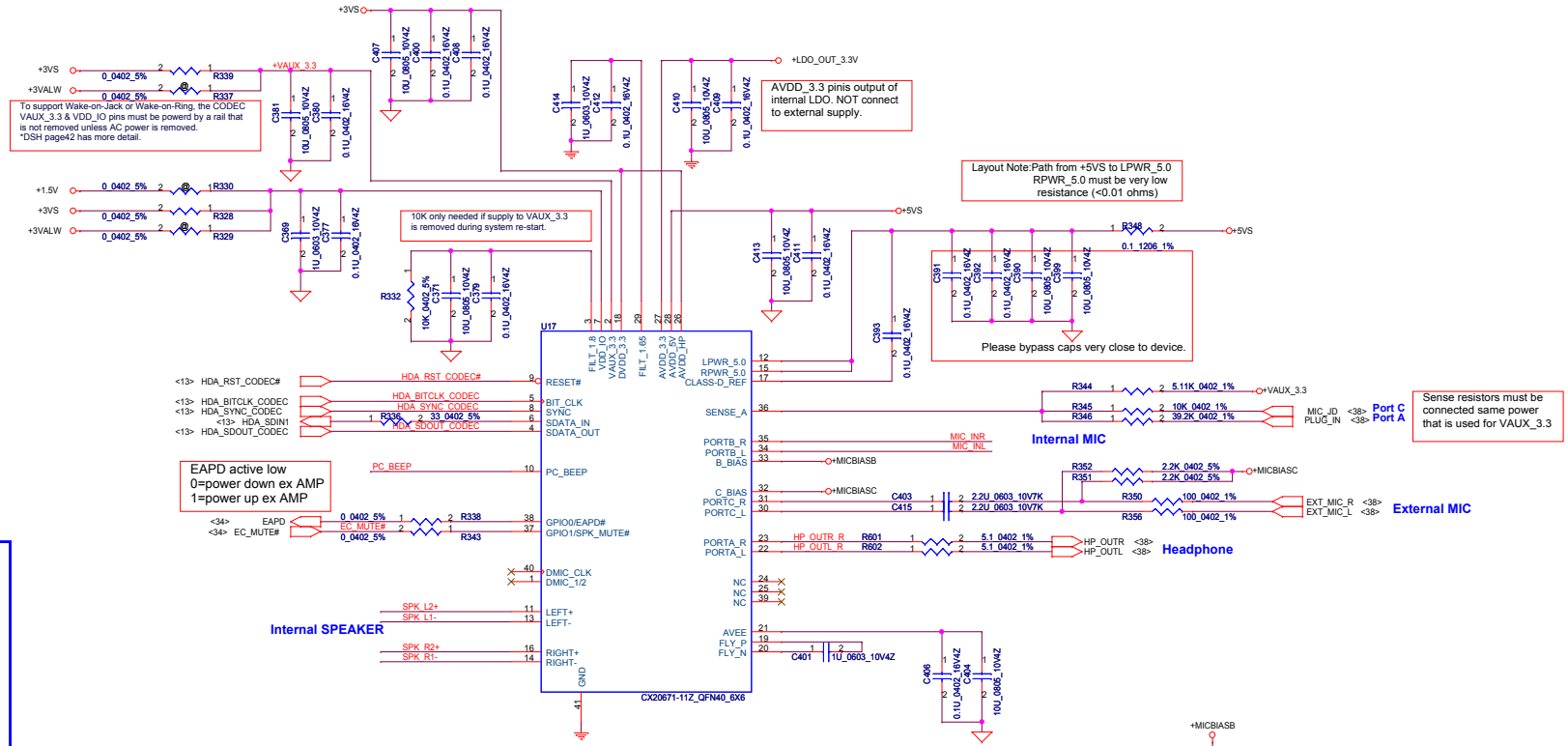


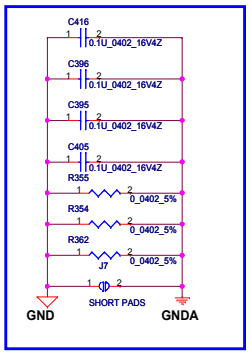
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

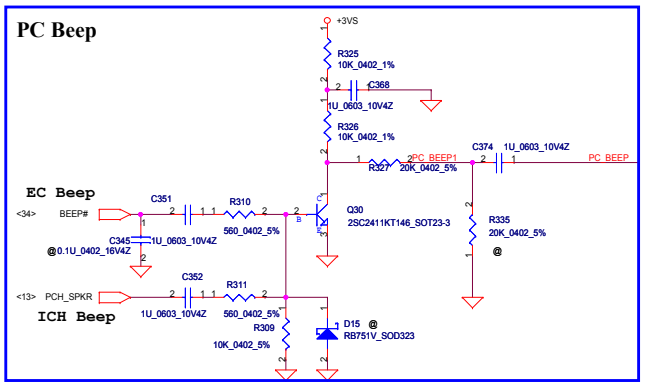
Compal Electronics, Inc.			
Title: HDD/ODD Connector			
Size: B	Document Number: LA-5751		Rev: 0.3
Date: Friday, October 30, 2009	Sheet 32 of 51		

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

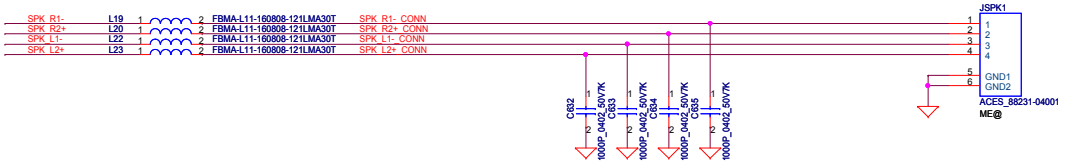








wide 20MIL



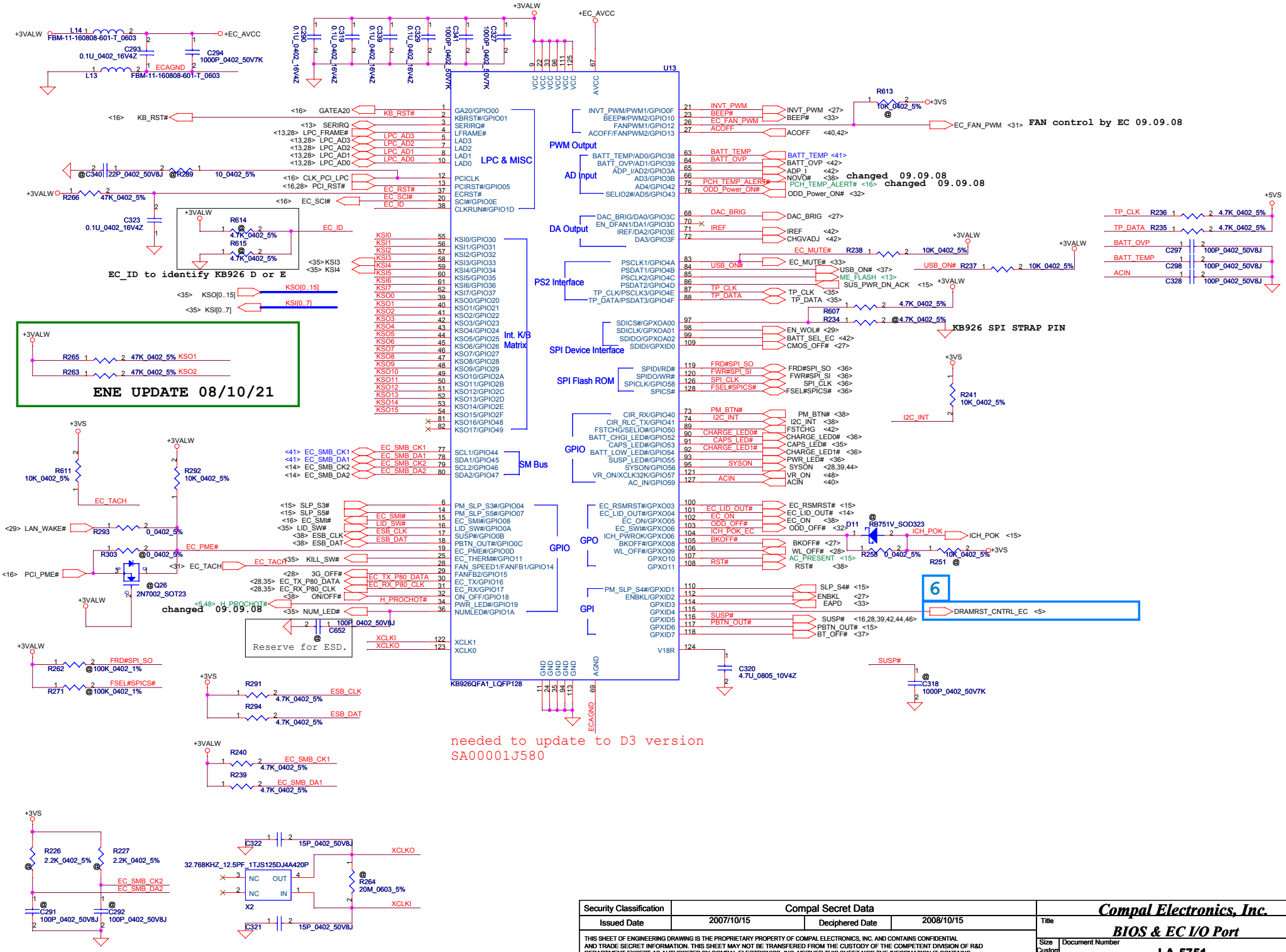
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: CX20671 Codec

Size: C | Document Number: LA-5751 | Rev: 0.3

Date: Friday, October 30, 2009 | Sheet 33 of 51



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

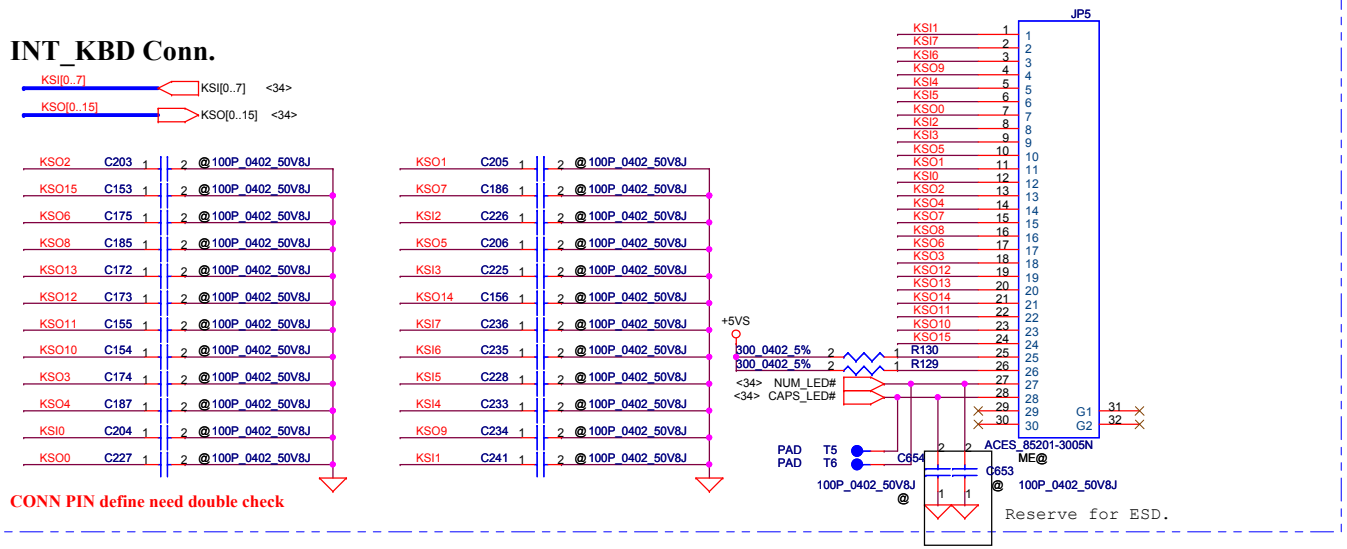
Compal Electronics, Inc.

Title: BIOS & EC I/O Port

Size	Document Number	Rev
Custom	LA-5751	0.3

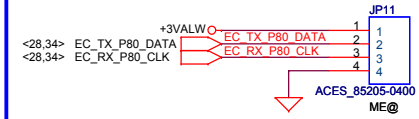
Date: Friday, October 30, 2009 Sheet 34 of 51

INT_KBD Conn.

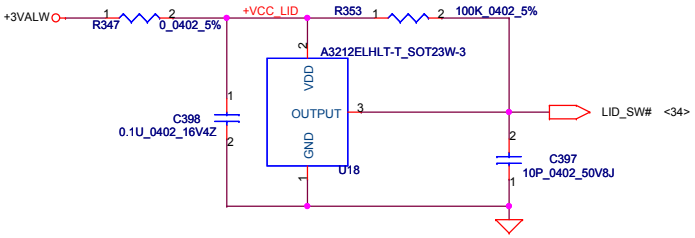


CONN PIN define need double check

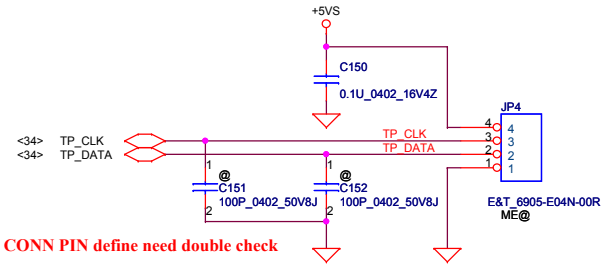
EC DEBUG PORT



Lid Switch

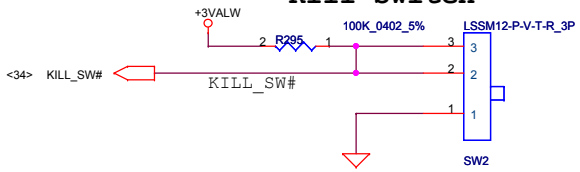


To TP/B Conn.



CONN PIN define need double check

Kill Switch



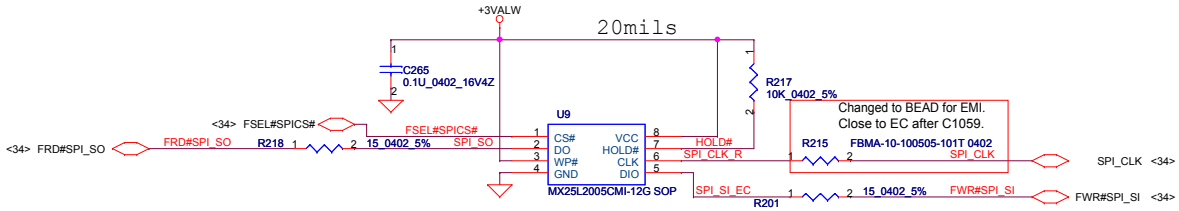
Kill

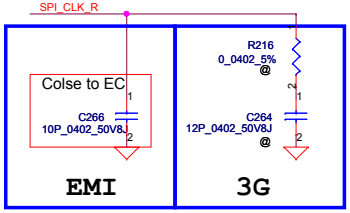
STATUS	
1,2(LOW)	OFF
2,3(HI)	ON

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

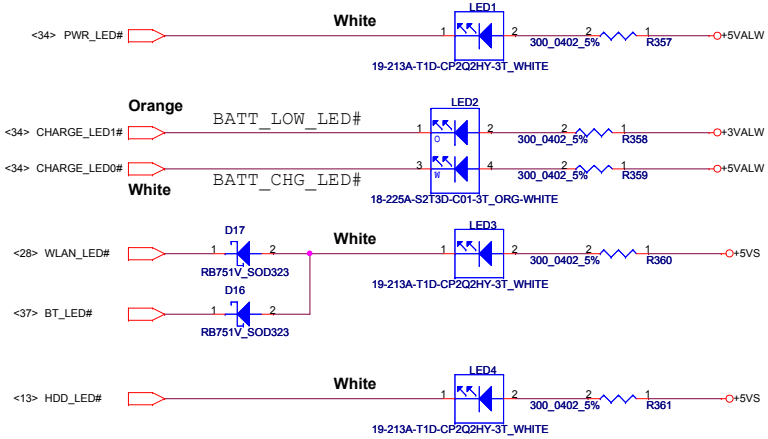
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: LA-5751		Rev: 0.3
Date: Friday, October 30, 2009	Sheet 35 of 51		

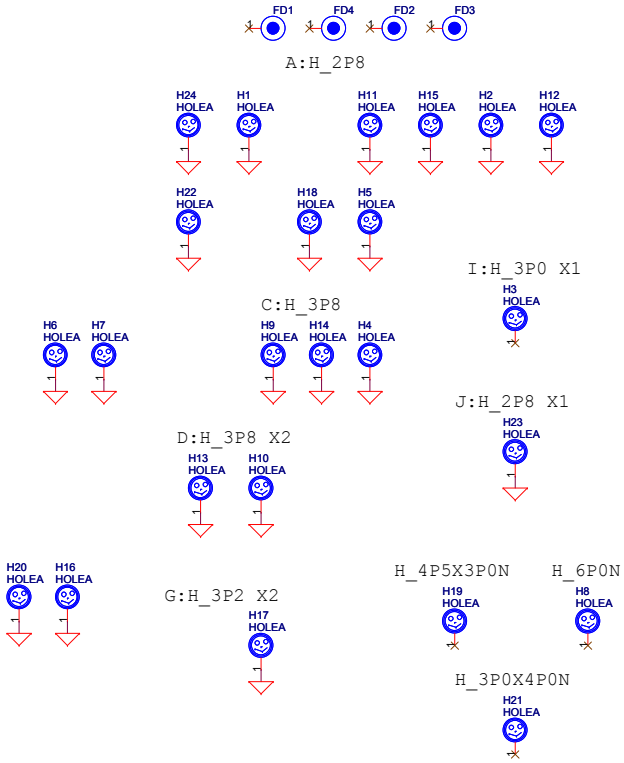
FOR EC 256KB SPI ROM
(150mil PACKAGE)





LED





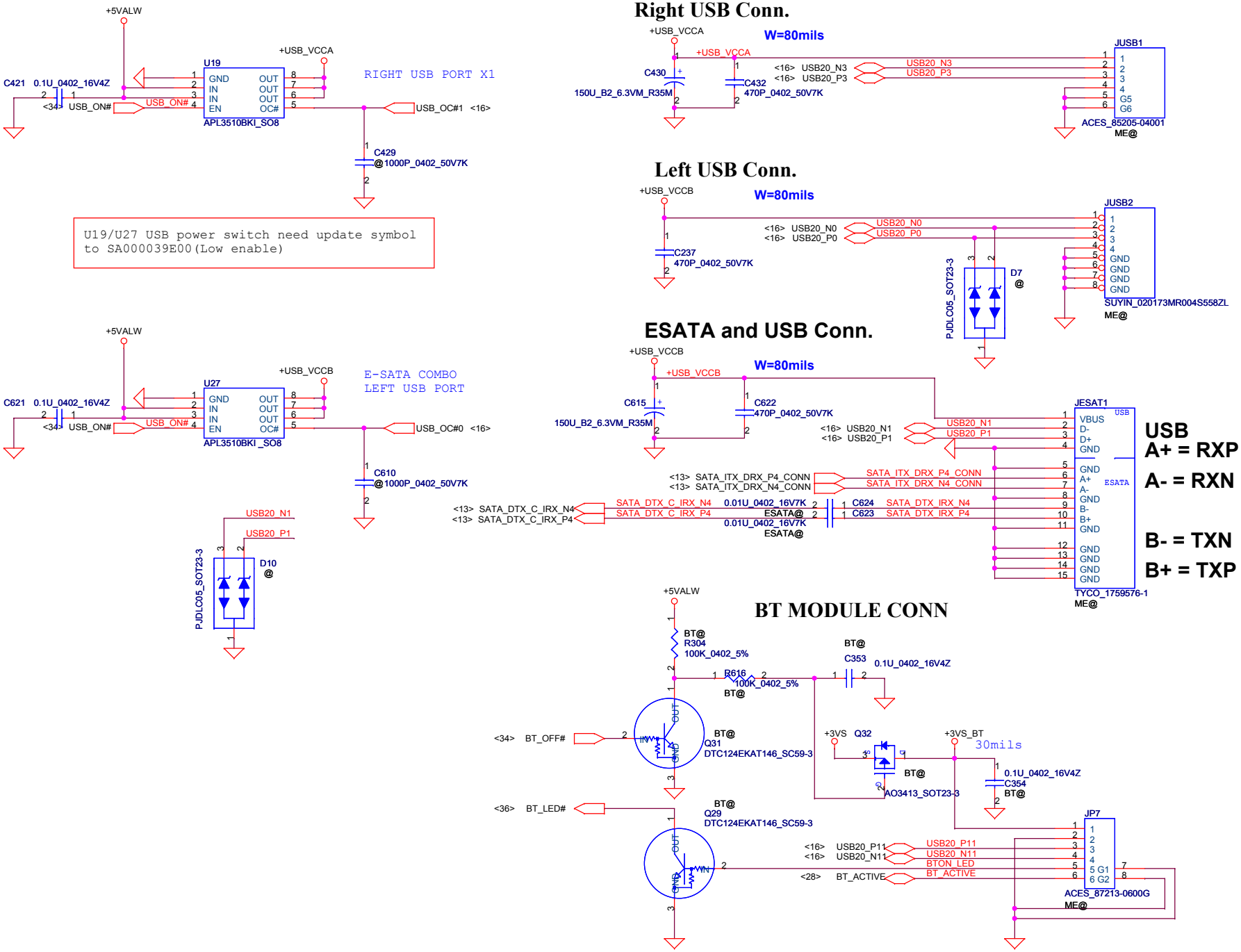
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: LED/EC SPI ROM

Size	Document Number	Rev
B	LA-5751	0.3

Date: Friday, October 30, 2009 Sheet 36 of 51



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

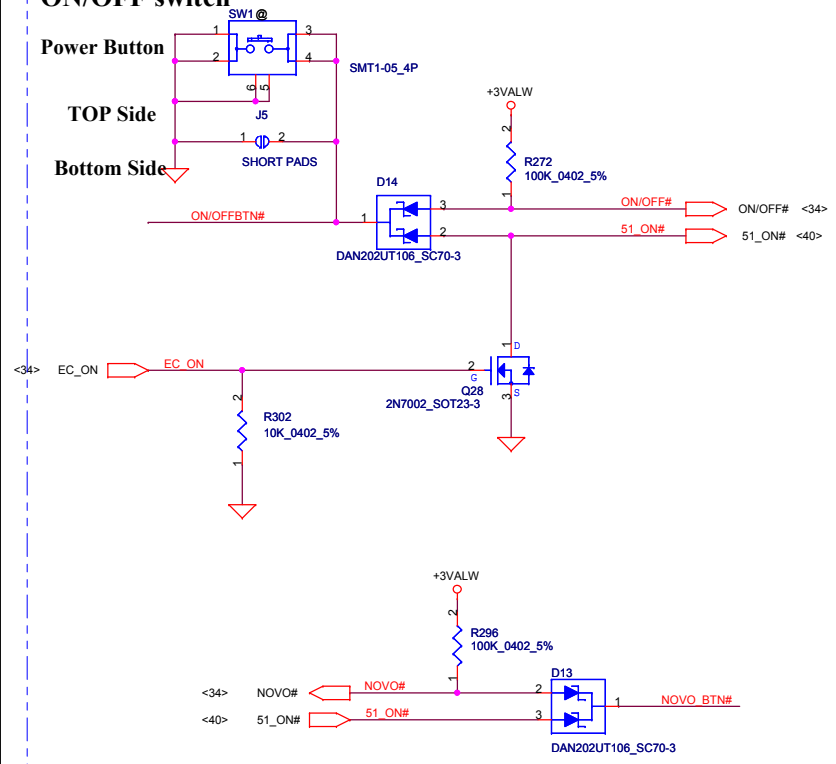
Compal Electronics, Inc.

Title: USB ports/BT/E-SATA

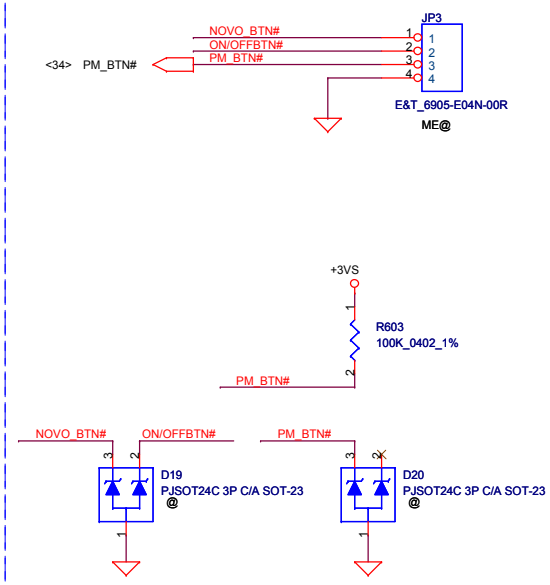
Size	Document Number	Rev
Custom	LA-5751	0.3

Date: Thursday, October 29, 2009 | Sheet 37 of 51

ON/OFF switch

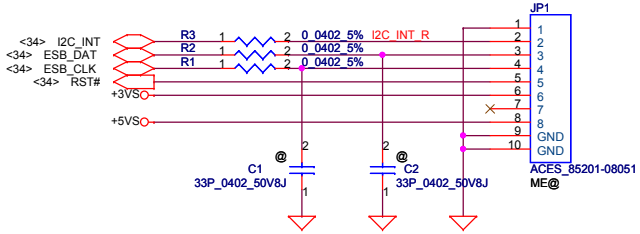


Power Bottom Board Conn. 4pin

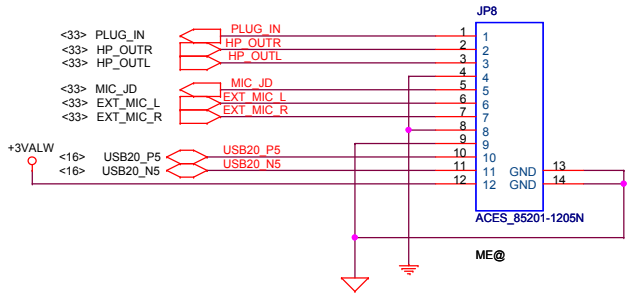


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Cap Sensor Board Conn. 6pin
ENE SB3534



Card Reader/Audio Jack SB CONN



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

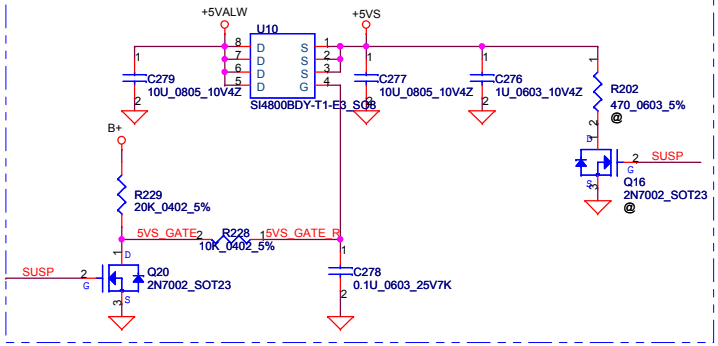
Compal Electronics,Ltd.

Title: **Audio Jack & SW connector**

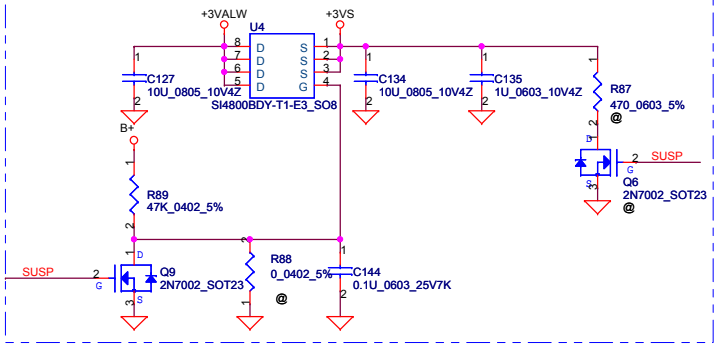
Size	Document Number	Rev
Custom	LA-5751	0.3

Date: Friday, October 30, 2009 | Sheet 38 of 51

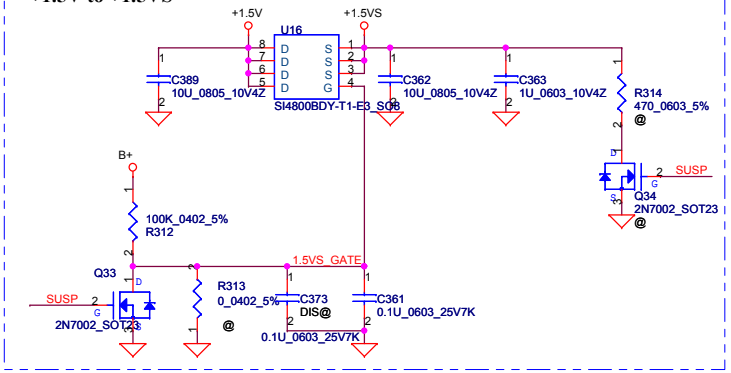
+5VALW TO +5VS

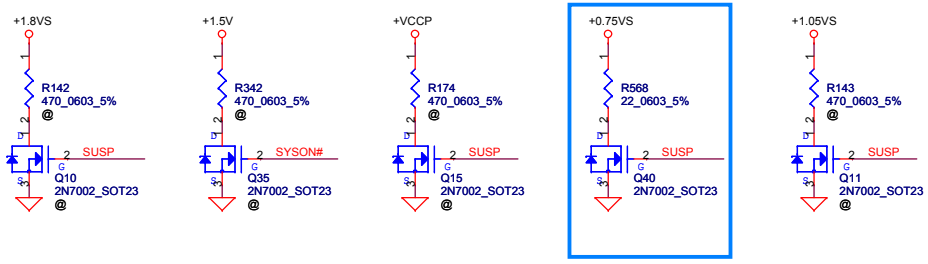


+3VALW TO +3VS

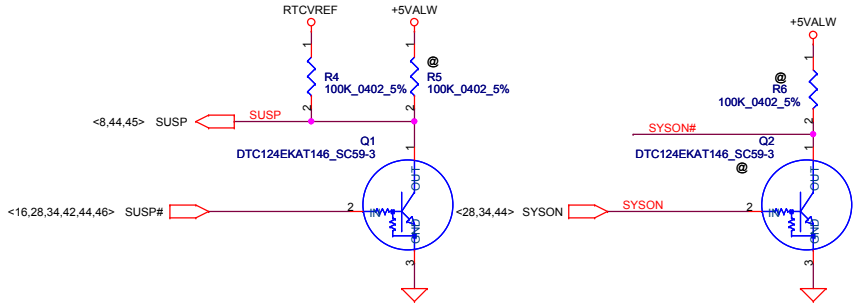


+1.5V to +1.5VS





For Intel S3 Power Reduction.



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-5751	0.3

Date: Thursday, October 29, 2009 Sheet 39 of 51

DC030006J00

VIN

PF1 7A_24VDC_429007.WRML

PL2 SMB3025500YA_2P

APDIN APDIN1

@4602-Q04C-09R 4P P2.5 JDCIN

PC8 0.1U_0603_25V7K
PC9 1000P_0402_50V7K
PC10 100P_0402_50V8J
PC7 0.1U_0603_25V7K
PC6 100P_0402_50V8J
PC5 1000P_0402_50V7K

ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Vin Detector	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

PR26 1M_0402_1%
VINDE-2
VS
PC97 0.01U_0402_25V7K
PR21 10K_0805_5%
PR18 10K_0402_1%
ACIN <34>
PACIN <42>
PR134 84.5K_0402_1%
PR27 22K_0402_1%
VINDE-1
VINDE-3
PU10A LM393DG_SO8
PD9 LLZ4V3B_LL34-2
PR19 10K_0402_5%
PC14 1000P_0603_50V7K
PR135 20K_0402_1%
PC13 0.1U_0402_16V7K
PR20 10K_0402_5%
RTCVREF 3.3V

PR142 1K_1206_5%
PR38 1K_1206_5%
PR31 1K_1206_5%
PD13 RLS4148_LL34-2
PQ26 TP0610K-T1-E3_SOT23-3
PR143 100K_0402_1%
PR138 100K_0402_1%
PR39 100K_0402_1%
<34,42> ACOFF
PQ11 DTC115EUA_SC70-3
PQ12 DTC115EUA_SC70-3
B+

VL
PR25 2.2M_0402_5%
PR137 100K_0402_1%
PD10 RB715F_SOT323-3
<41,43> MAINPWON
<42> ACON
PU10B LM393DG_SO8
PC99 0.01U_0402_25V7K
PC98 0.1U_0603_25V7K
PC11 1000P_0402_50V7K
PR17 10K_0402_5%
RTCVREF
PR22 499K_0402_1%
PR24 499K_0402_1%
PC12 0.01U_0402_25V7K
PR23 205K_0402_1%
PRG++
PQ3 SSM3K7002F_SC59-3
PR136 47K_0402_5%
PACIN <42>
+5VALW
PQ25 DTC115EUA_SC70-3

VIN
PD2 LL4148_LL34-2
BATT+
PD12 LL4148_LL34-2
51ON-1
PR141 68_1206_5%
PR140 68_1206_5%
PQ4 TP0610K-T1-E3_SOT23-3
PR122 200_0603_5%
CHGRTCP
51ON-2
VS
PR15 100K_0402_1%
PC4 0.22U_0603_25V7K
PC16 0.1U_0603_25V7K
PR16 22K_0402_1%
<38> 51_ON#
51ON-3

RTCVREF
+CHGRTC
PR125 560_0603_5%
PR124 560_0603_5%
3.3V
PU8 G920AT24U_SOT89-3
OUT IN GND
PR123 200_0603_5%
CHGRTCIN
PC91 10U_0603_6.3V6M
PC90 1U_0805_25V6K

JRTC
@MAXEL_ML1220T10
+RTCBATT
PD8 RB751V-40_SOD323-2
+CHGRTC
RTC Battery

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

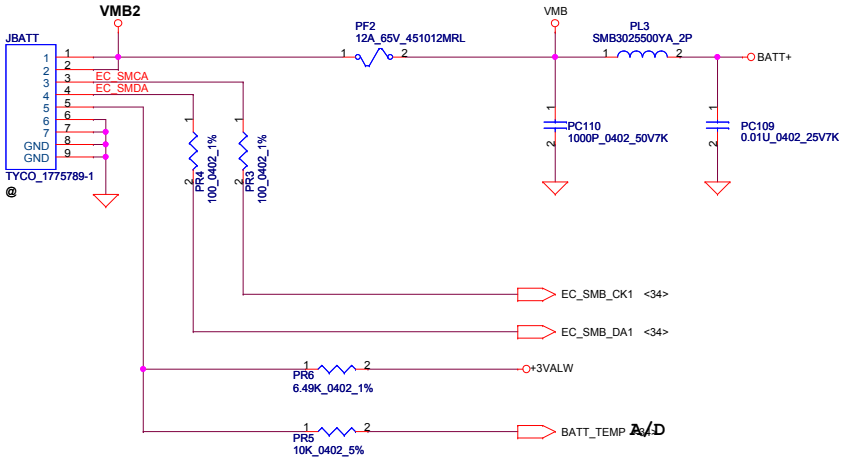
Compal Electronics, Inc.

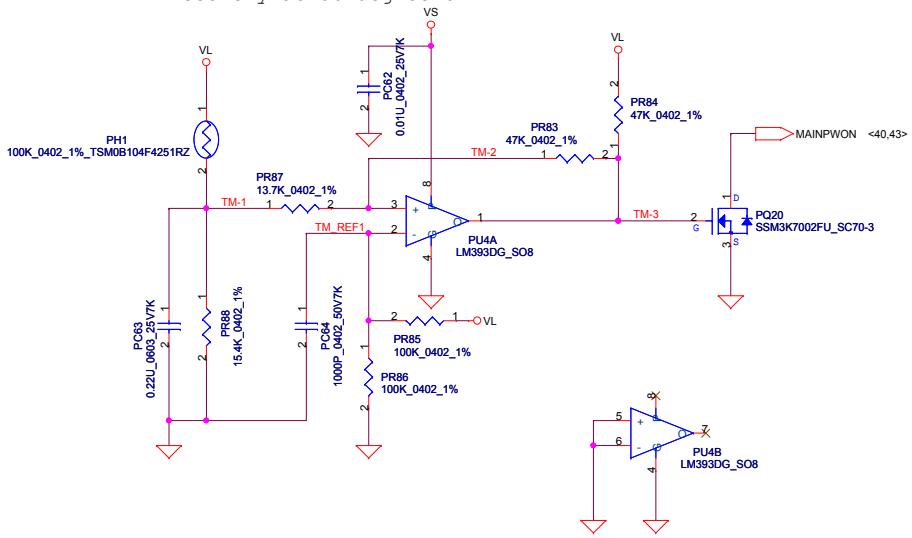
Title: DCIN & DETECTOR

Size: Custom | Document Number | Rev: 0.1

Date: Friday, October 30, 2009 | Sheet 40 of 51

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





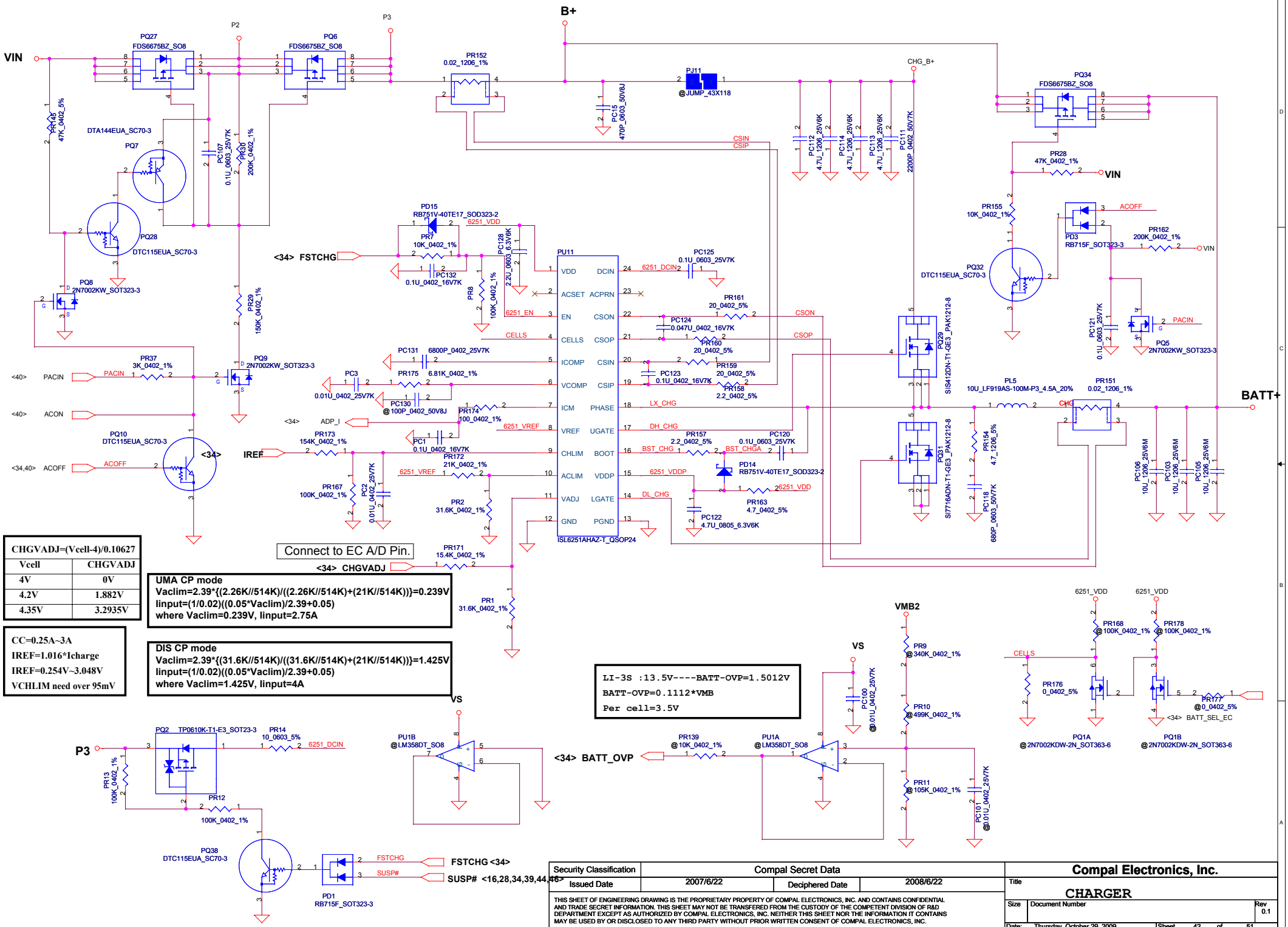
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.1

Date: Thursday, October 29, 2009 | Sheet 41 of 51



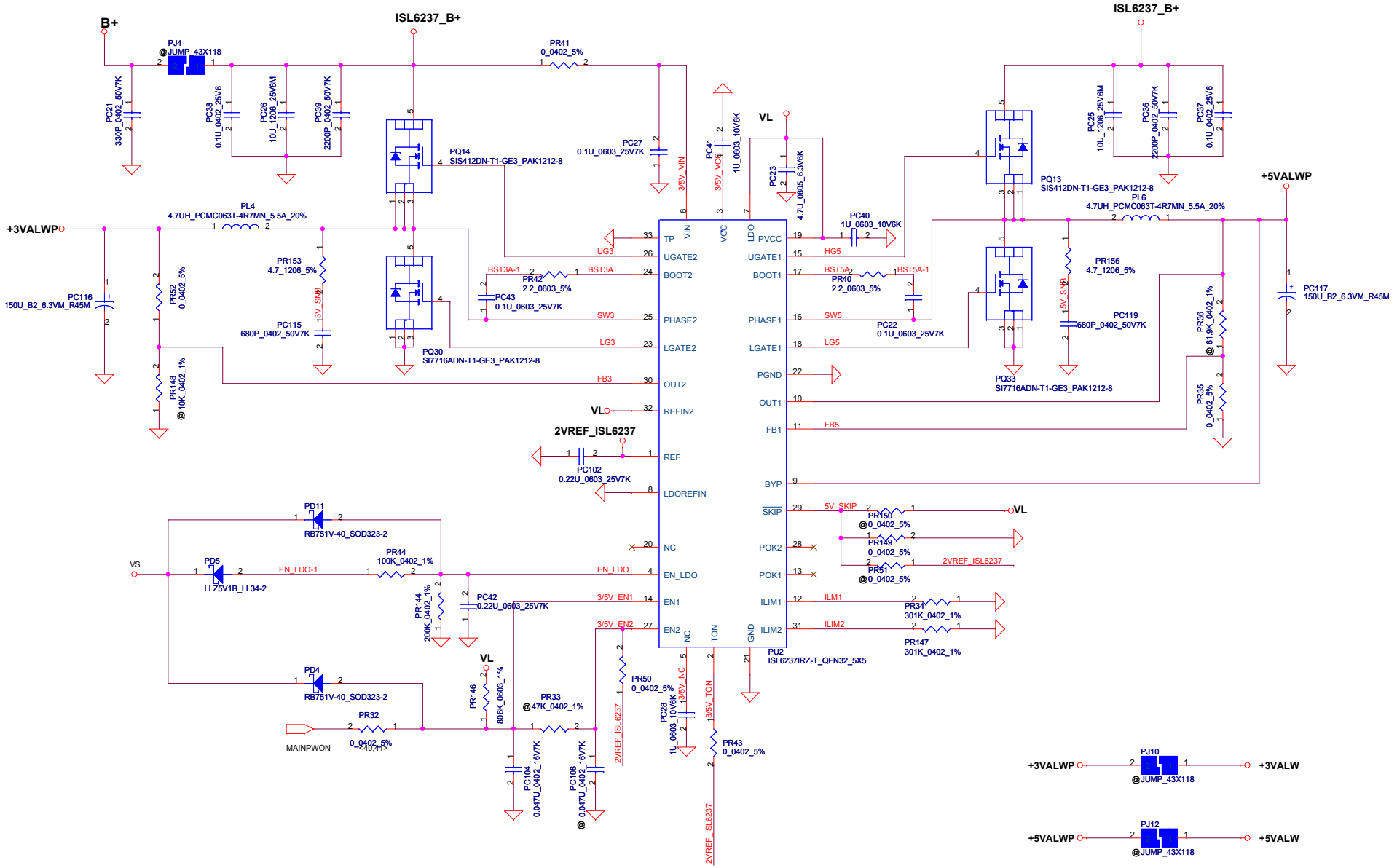
Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
		0.1

Date: Thursday, October 29, 2009 | Sheet 42 of 51



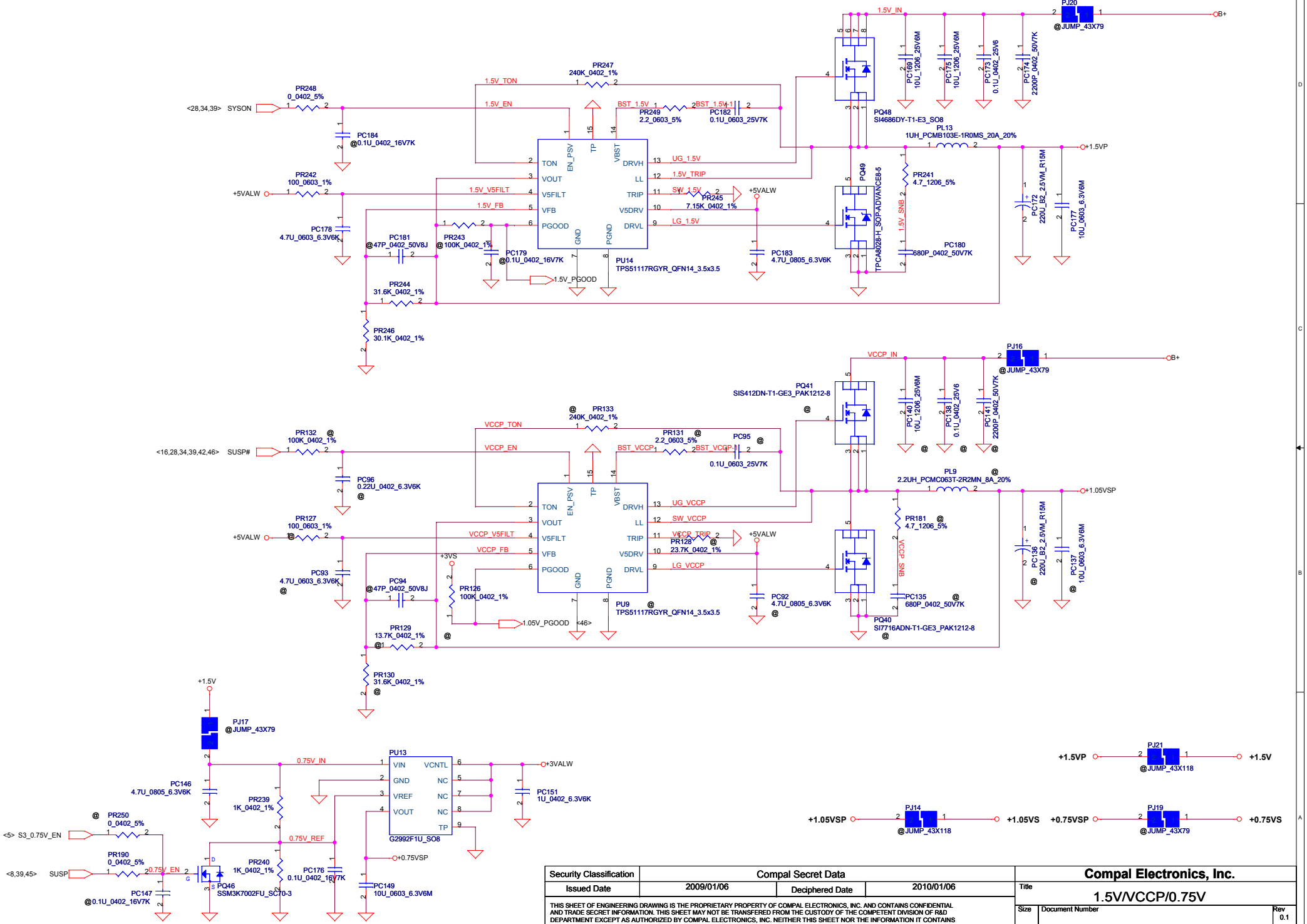
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom		0.1

Date: Thursday, October 29, 2009 | Sheet 43 of 51



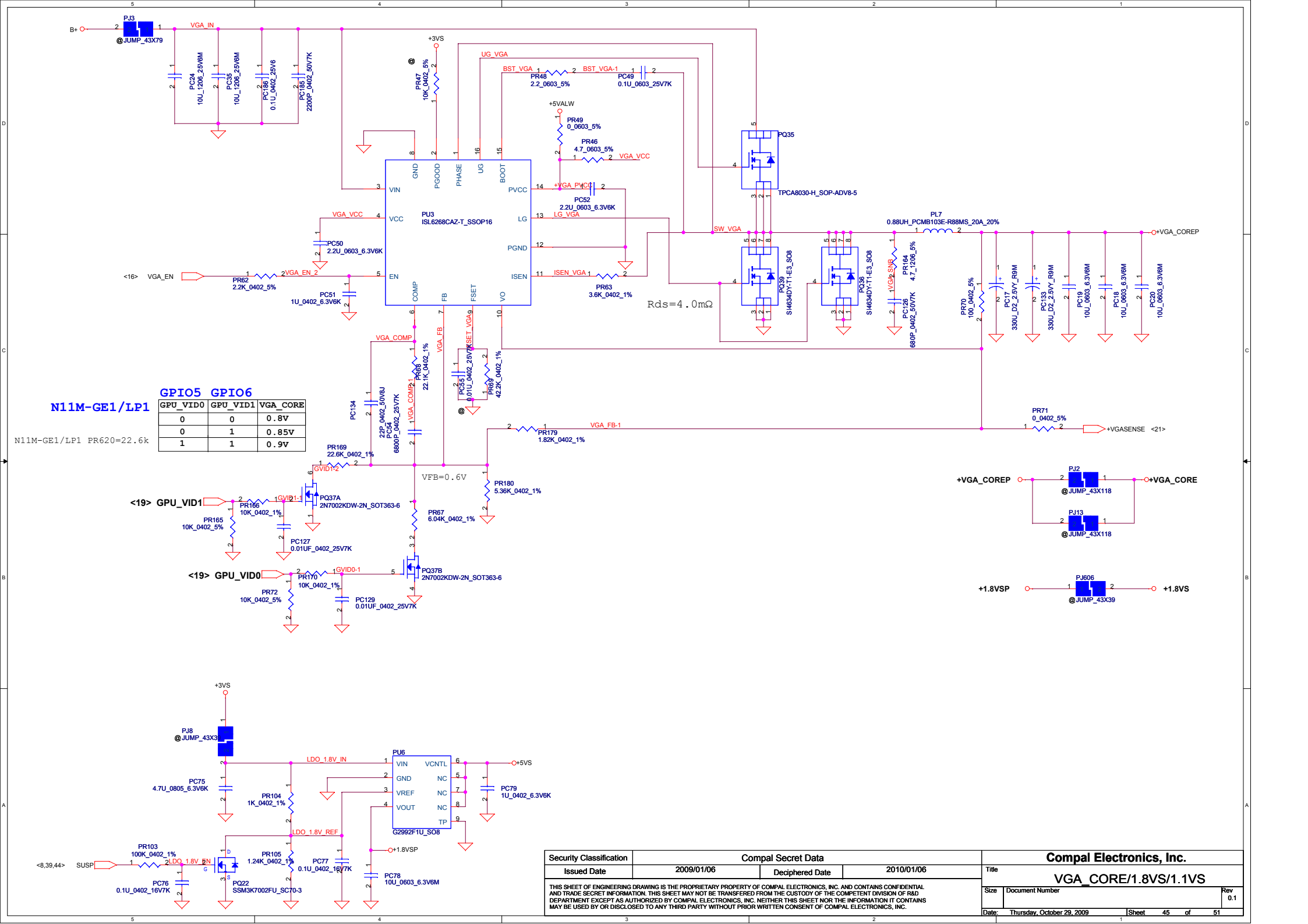
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 1.5V/VCCP/0.75V

Size	Document Number	Rev
		0.1

Date: Friday, October 30, 2009 | Sheet 44 of 51



N11M-GE1/LP1

N11M-GE1/LP1 PR620=22.6k

GPIO5	GPIO6	
GPU_VID0	GPU_VID1	VGA_CORE
0	0	0.8V
0	1	0.85V
1	1	0.9V

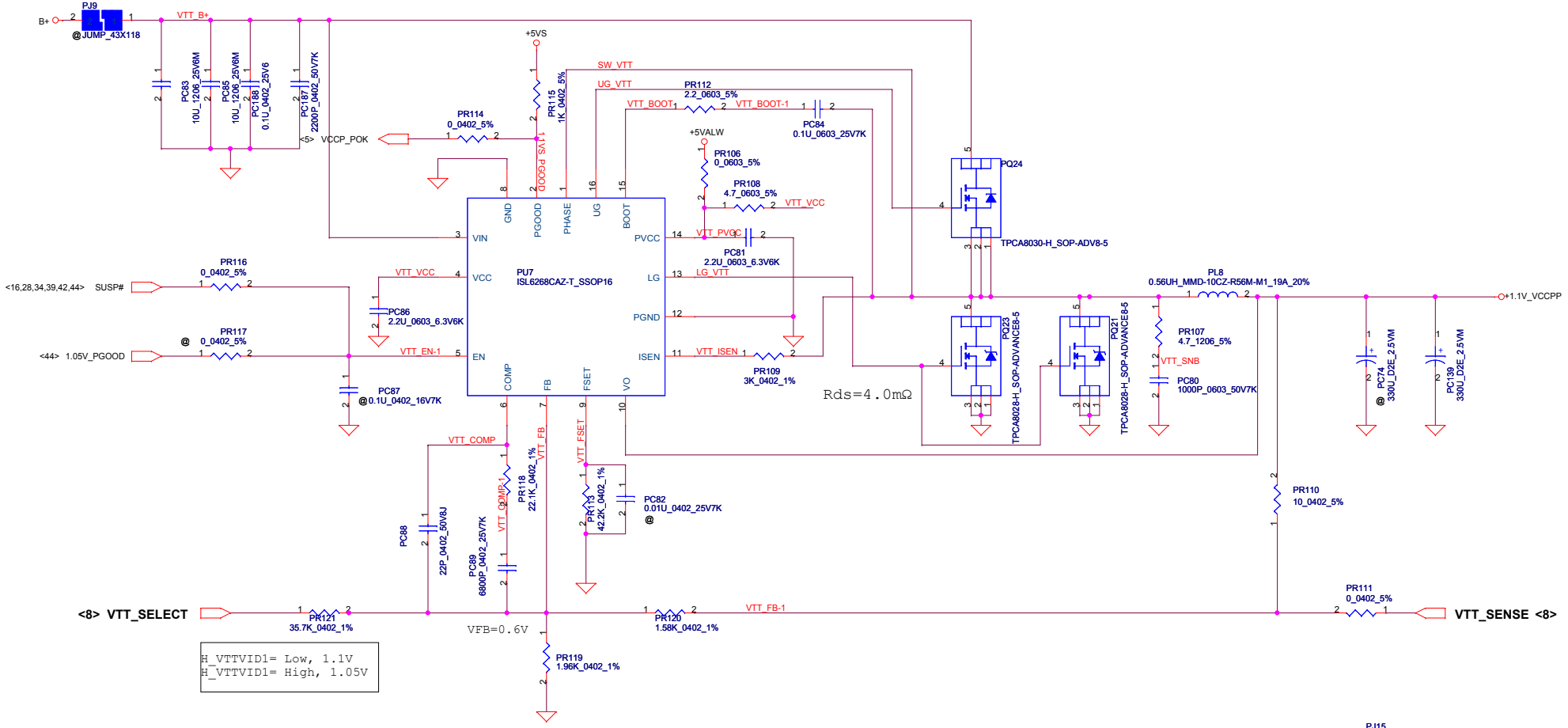
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: VGA_CORE/1.8VS/1.1VS

Size	Document Number	Rev
		0.1

Date: Thursday, October 29, 2009 | Sheet 45 of 51



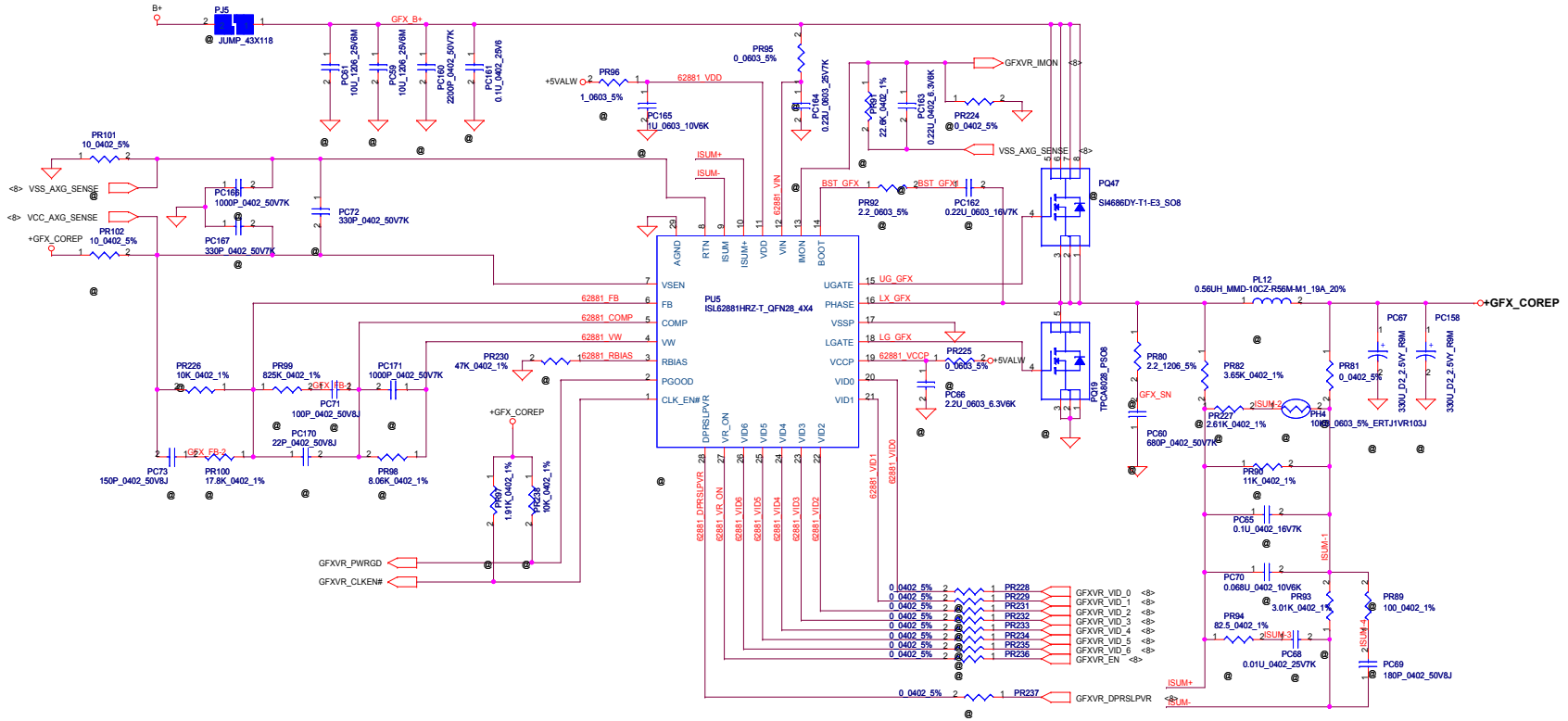
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: +1.1VS_VTT

Size	Document Number	Rev
Custom		0.1

Date: Thursday, October 29, 2009 | Sheet 46 of 51



(15A,600mils ,Via NO.= 30)

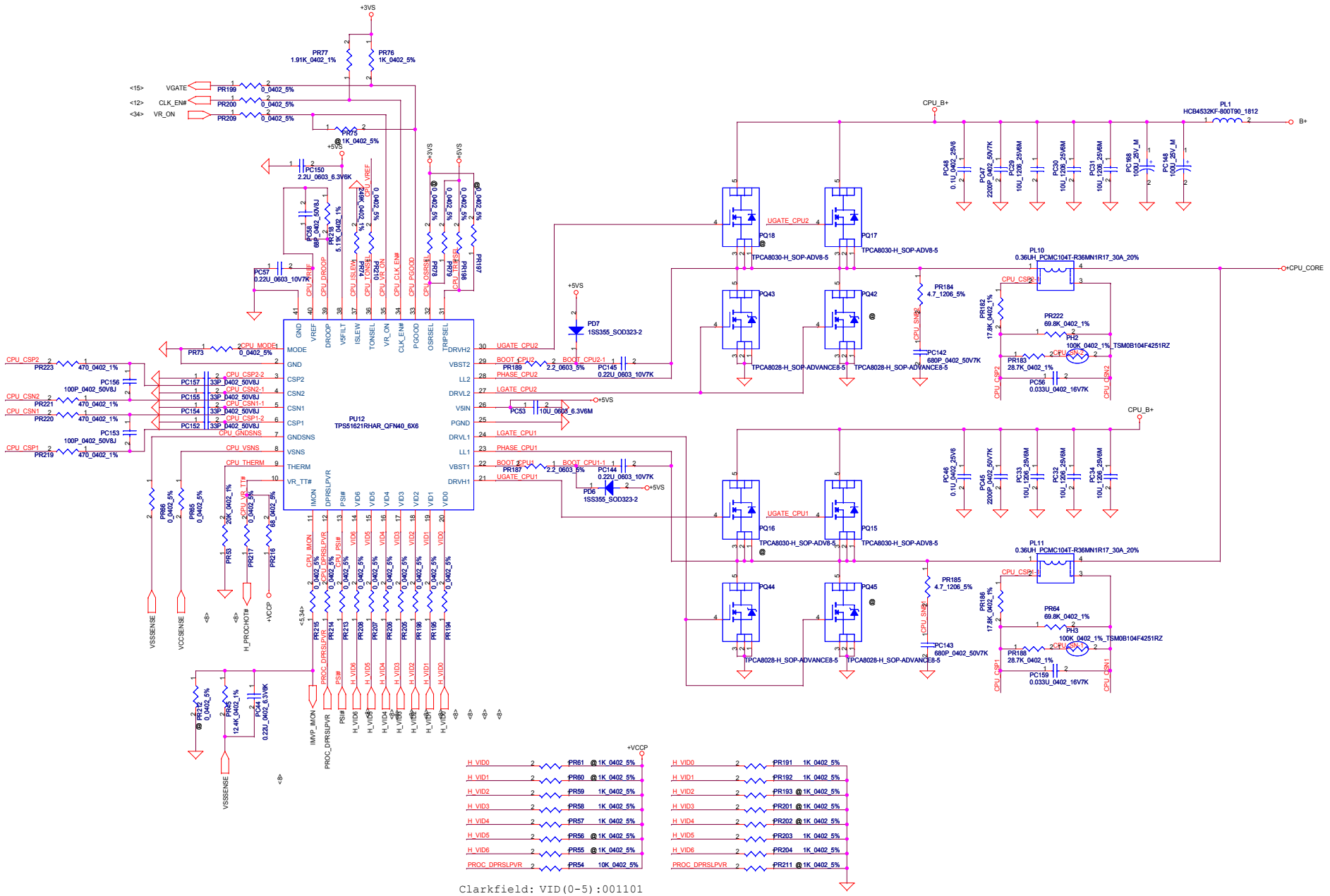
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: GFX_CORE

Size	Document Number	Rev
		0.1

Date: Friday, October 30, 2009 | Sheet 47 of 51



Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.			
Title	CPU_CORE		
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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
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Compal Electronics, Inc.

Title: PIR (PWR)

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				EVT TO DVT
1		P15	Add C638~C645	For UMA HDMI
2		P05	Add test point for BCLK_ITP,BCLK_ITP#,PRDY#	For XDP connector
3		P32,P28	Change J6 size & unstuff ODD power control components Change J4 size	Disable ODD power control circuit
4		P17	Stuff C262	For UMA CRT
5		P34	Change R291,R294 from +3VALW to +3VS	
6		P38	Add R603 pull high to +3VS	For PM_BTN#
7		P38	Change JP1 from 6 pin to 8 pin , Change JP8 from 14 pin to 12 pin , unstuff R322	For LED color changed Remove CLK_48M_CR
8		P29,P34	Change EN_WOL to EN_WOL#	For identify clearly
9		P34	EC pin26-> EC_FAN_PWM , pin75->PCH_TEMP_ALERT , pin34->PROCHOT# , pin66->NOVO#	EC GPIO arrangement
10		P31	Change JP12 pin define	For EC FAN control
11		P16	Change U5 pin3,pin5	POWER , GND reversed
12		P15	Add U28 for ICH_POK & VGATE	Reserved
13		P12	Unstuff R278,stuff R269 and change U14 to SA00003HQ00	For low power CLK GEN
14		P13	Change U3 from 2MBytes to 4MBytes	For 4MBytes SPI ROM for PCH
15		P29	Correct Q17 to P/N:SB000007600	For +3V_LAN power
16		P16	Add C646 for BUF_PLT_RST#	Reserved for BUF_PLT_RST# overshoot problem
17		P36	Change U9 from 2MBytes to 256KBytes	For 256KBytes SPI ROM for EC
18		P03	UMA_HDMI@ , HDMI@ , BT@ , 3G@ , ESATA@ , CMOS@	New BOM structure
19		P08	Add R608	For PSI# pull down
20		P37	Delete D18	
21		P16	Unstuff R210,R212	Set Boot BIOS Strap to SPI
22		P22	Change & stuff R475 to 30K,R51 to 15K Unstuff R474,R50	For N11M-GE1 QS sample
23		P25	Unstuff R246	Level shift default setting
24		P39	Change C373 to DIS@	for DIS power sequence
25		P15,P16,P17	Change R436 from 1K to 10K Change C447 from 0.1u to 1u Delete R514 Unstuff C493,C494 Reserve R609	Check list Rev2.0 update
27		P34	Add R607	Reserved for KB926 SPI STRAP PIN
28		P36	Change LED1,LED3,LED4 to white color LED2 to orang\white color and orage connect to +3VALW	
29		P14	Change exp-card from PCIE port 1 to port 5	SW BIOS request
30		P38	Unstuff SW1	
31		P13,P34	Change X1,X2 footprint	
32		P12	Change C348 to 22p,C349 to 22p	For Crystal matching
33		P13,P20	Add C647~C650 12p, stuff C370->22p, R331->33	Reserved for RF team
34		P36	Delete JP6	SPI ROM socket
35		P37	Change C430,C615 footprint to B2 type	
36		P27,P32,P37	Change Q4,Q24,Q32,Q37 footprint to AO3413	

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				EVT TO DVT
37		P34	Change C320 to 0805 type	
38		P08	Unstuff C268 Change C252,C258 from 10u to 22u	For CPU VDDQ (DDR3 1.5V rails)
39		P34	Change ODD_power_on# from U13 pin28 to pin 76 Add EC_TACH on U13 pin28 to JP12	EC GPIO arrangement
40		P31	Change U20 to EMC1403, add C651	Change thermal sensor solution to EMC1403
41		P05	Add Q42,R610	Reserve for +0.75V enable option
42		P34,P35	Add C652,C653,C654	Reserve for NUM_LED#,CAPS_LED# ESD request
43		P34	Add R611,R612,R613	For EC_FAN_PWM, EC_TACH

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				DVT TO PVT
1		P34	Reseve R614,R615.	EC_ID to identify KB926 D or E
2		P34	Stuff R607	KB926 SPI STRAP PIN
3		P33	Stuff C632~C635	EMI request
4		P16	Stuff C646	For PLT_RST# singnal quality
5		P37	Add R616 100K, change R304 to 100K, C353 to 0.1u	For +3VS_BT power on rising time
6		P37	Changed R304 pin1 from +5VS to +5VALW	For +3VS_BT power on leakage
7		P5	Stuff R283, C338 0.01u	For S3 power reduction
8		P31	Add U29	Colay EMC2103/EMC1403 thermal sensor

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