ZZZ
PCB

ZZZ1
LA-5081P
DAZ@

ZZZ2
LS-5081P
DAZ@

ZZZ3
LS-5082P
DAZ@

KIWA5/A6

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM/PM+ICH9-M core logic

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

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Title: **Cover Sheet**

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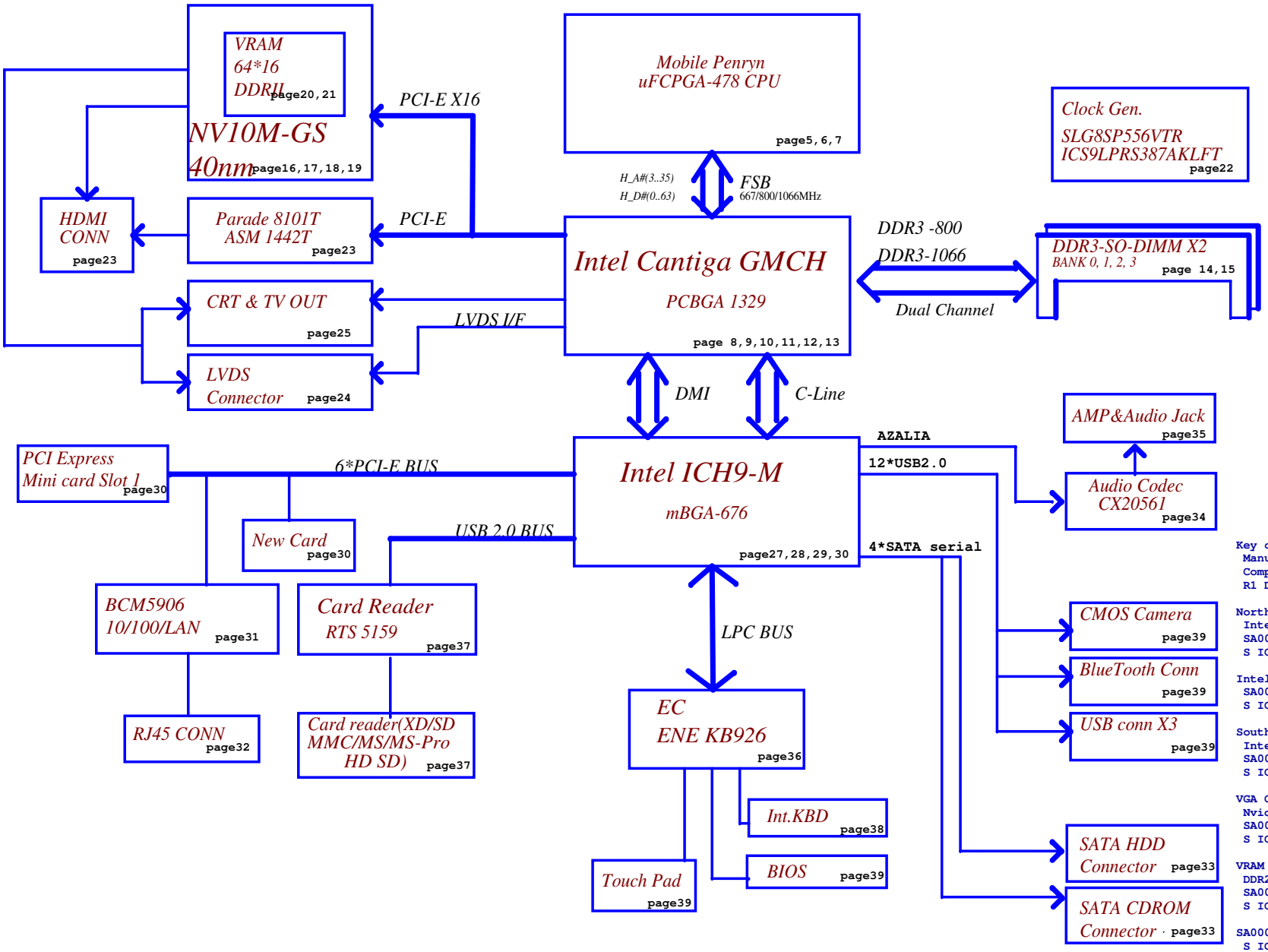
Compal confidential
File Name :

ZZZ
PCB KIWA5 LA-5081P LS-5081P/5082P

POWER Board

CAP SENSE LEDs Board



Key component
Manufacturer
Compal P/N
R1 Desc

Northbridge
Intel / Cantiga PM45
SA00002JJM0
S IC AC82PM45 QV11 A1 FCBGA 1329 PM C38

Intel / Cantiga GM 45
SA00002JTD0
S IC AC82GM45 SLB94 B3 FCBGA1329 GM C38!

SouthBridge
Intel / ICH9M
SA00002JH90
S IC AF82801IBM SLB8Q A3 676P ICH9M C38! (MP)

VGA Chip
Nvidia / N10M
SA00002V810
S IC N10M-GE1-S-U2(H) BGA 533P C38

VRAM
DDR2/512MB
SA00002MF00 (14")
S IC D2 64M16/500 HYB18T1G161C2F-20

SA00002UH00 (15.6")
S IC D2 64M16/500 H5PS1G63EFR-20L FBGA84

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

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Title: **MB Block Diagram**

Size	Document Number	Rev
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DDR3 Voltage Rails

power plane / State	B+	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	o	o	o	o
S1	o	o	o	o
S3	o	o	o	x
S5 S4/AC	o	o	x	x
S5 S4/ Battery only	o	x	x	x
S5 S4/AC & Battery don't exist	x	x	x	x

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	X	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	N10M	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	N10M	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT (55nm)	N10M	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	N10M	X	X	X	V	X	X	X	X	X	X	X	X	X
IFPC_AUX IFPC_AUX_N (40nm)	N10M	V	X	X	X	X	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

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Issued Date	2009/04/23	Deciphered Date	2010/05

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Title: MB Notes List

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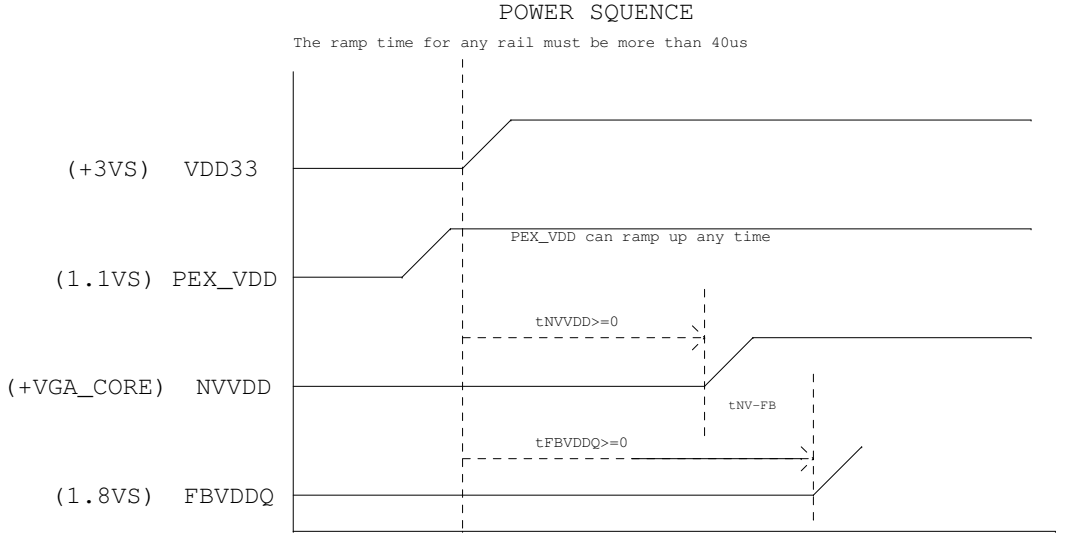
VGA and DDR2 Voltage Rails (N10M)

power plane / State	+3VS +VGA_CORE +1.1VS +1.8VS
S0	O
S1	O
S3	X
S5 S4/AC	X
S5 S4/ Battery only	X
S5 S4/AC & Battery don't exist	X

EDP at Tj = 97C*

Power Supply Rail	(V)	NB10M-GS		N10M-GE1-S	
		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	13.56A	13.47A
FB_DLLAVDD	1.1	25mA		25mA	
FB_PLLAVDD	1.1	10mA		10mA	
IFPC_IOVDD	1.1	385mA		180mA	
IFPD_IOVDD	1.1	385mA		180mA	
IFPE_IOVDD	1.1	385mA		180mA	
IFPF_IOVDD	1.1	385mA		180mA	
PEX_IOVDD/Q	1.1	1550mA		1550mA	
PEX_PLLVDD	1.1	165mA		65mA	
PLLVDD	1.1	55mA		30mA	
SP_PLLVDD	1.1	25mA		10mA	
VID_PLLVDD	1.1	50mA		25mA	
TOTAL	1.1	3.425A		2.435A	
FBVDD/Q	1.8	2.24A	1.65A	2.24A	1.75A
IFPA_IOVDD	1.8	50mA		50mA	
IFPB_IOVDD	1.8	50mA		50mA	
IFPAB_PLLVDD	1.8	100mA		75mA	
IFPCD_PLLVDD	1.8	160mA		80mA	
IFPEF_PLLVDD	1.8	160mA		80mA	
TOTAL	1.8	2.76A	2.17A	2.575A	2.085A
DACA_VDD	3.3	110mA		110mA	
DACB_VDD	3.3	125mA		125mA	
DACC_VDD	3.3	110mA		110mA	
MIOA_VDDQ	3.3	10mA		10mA	
MIOB_VDDQ	3.3	10mA		10mA	
VDD33	3.3	80mA		80mA	
TOTAL	3.3	0.445A		0.445A	

POWER SQUENCE



Compal Electronics, Inc.

Title: VGA Notes List

Size: B | Document Number: KIWA5/6 LA-5081P | Rev: 1.0

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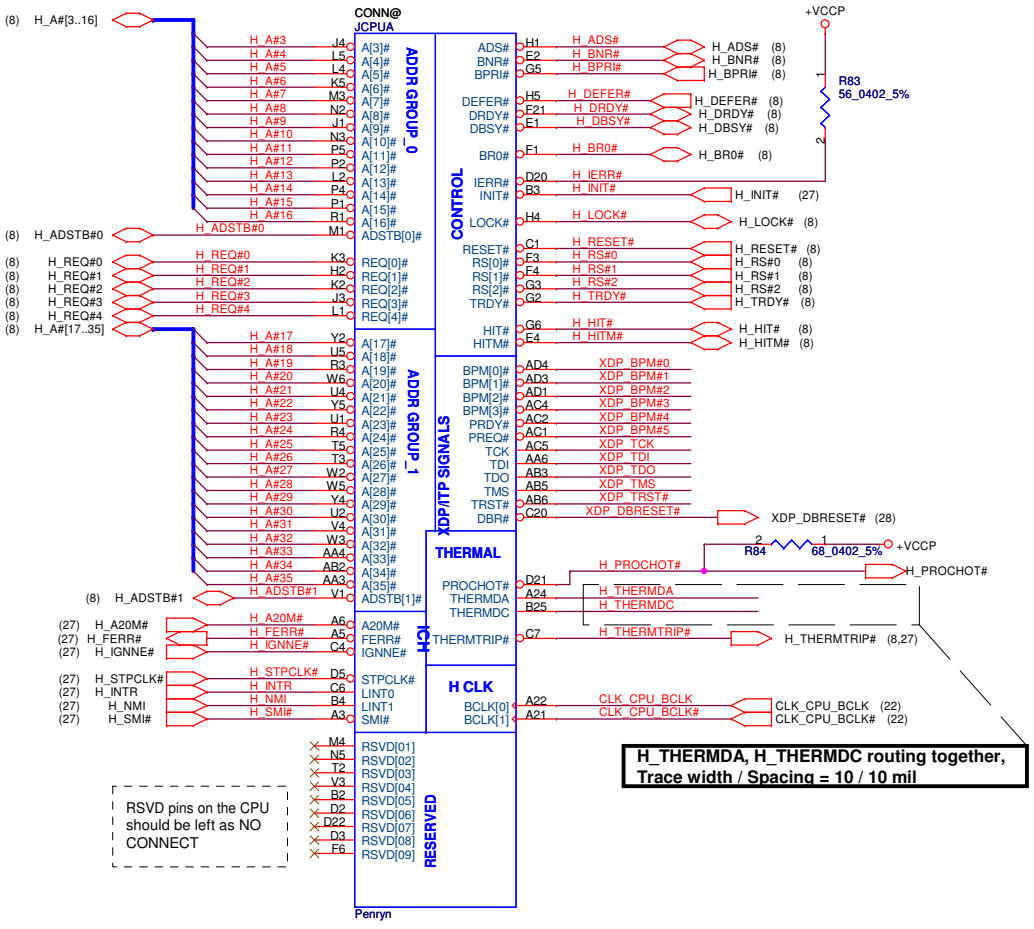
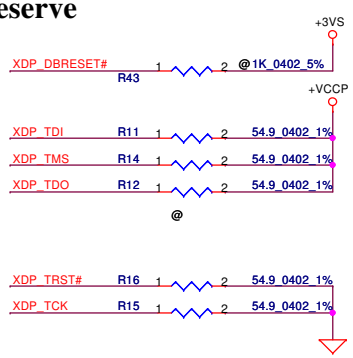
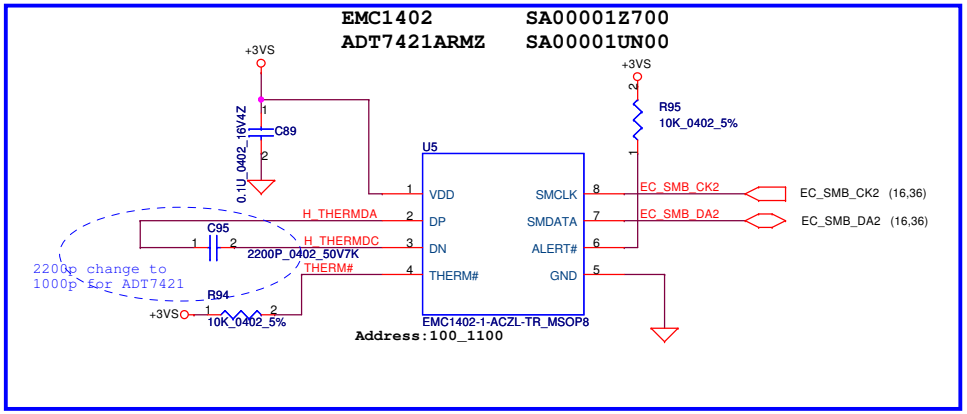
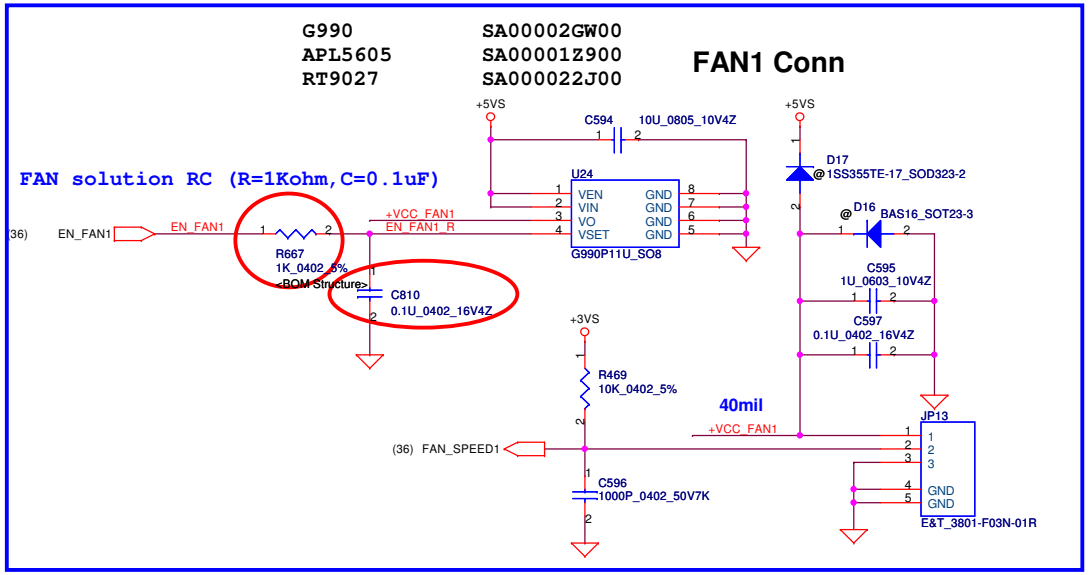


XDP Reserve







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Compal Electronics, Inc.			
Title: Penryn (1/3)			
Size: B	Document Number: KIWAX_LA-5081P		Rev: 1.0
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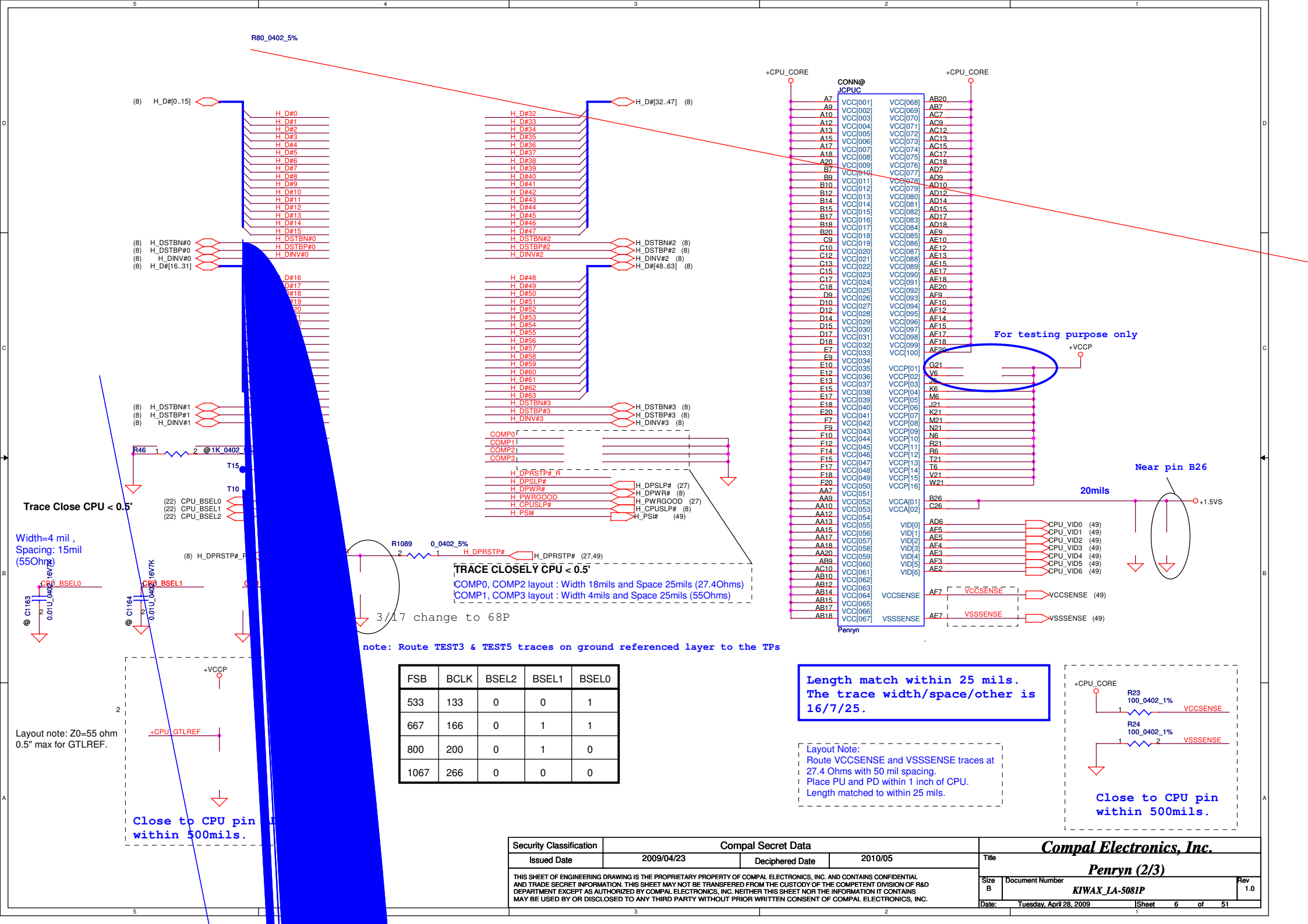

note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

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Title: Penryn (2/3)

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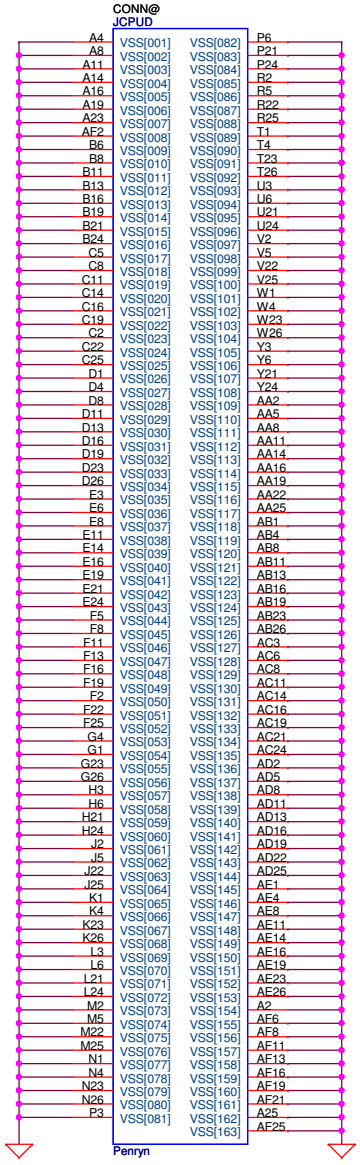
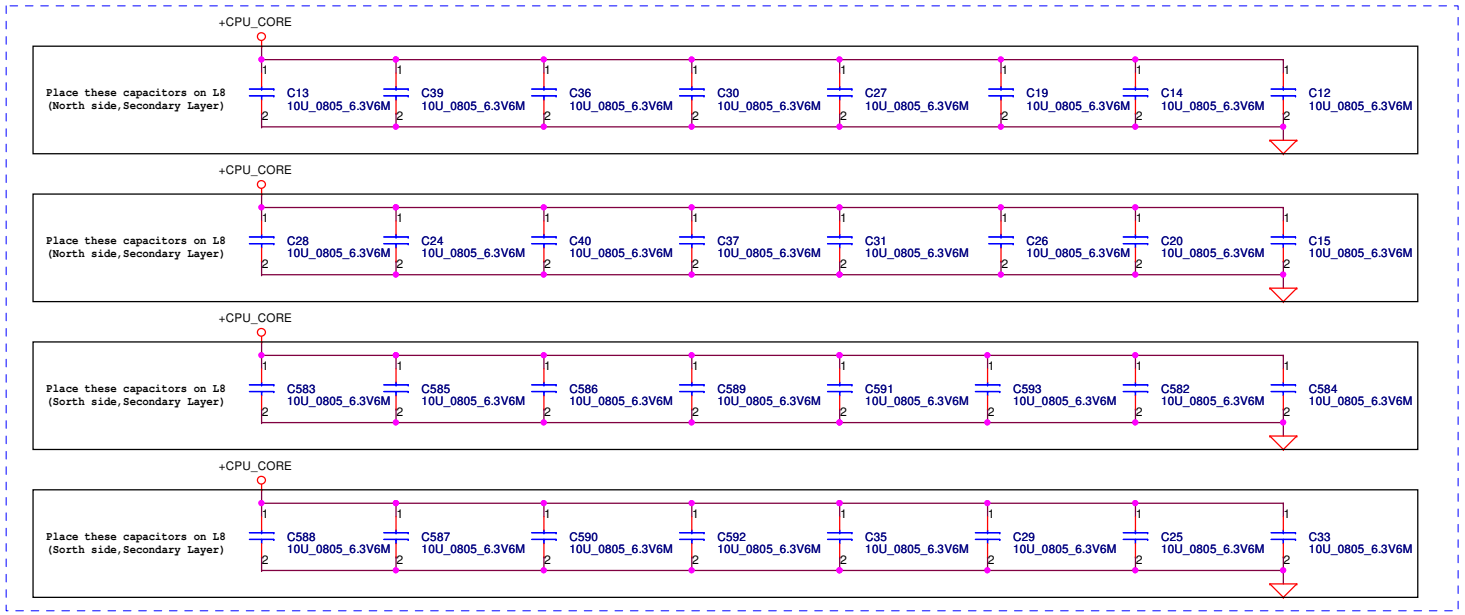
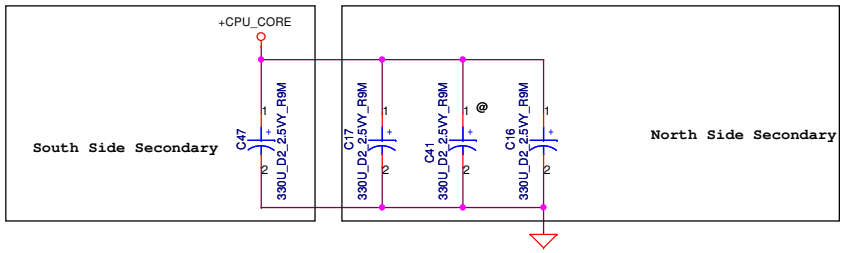


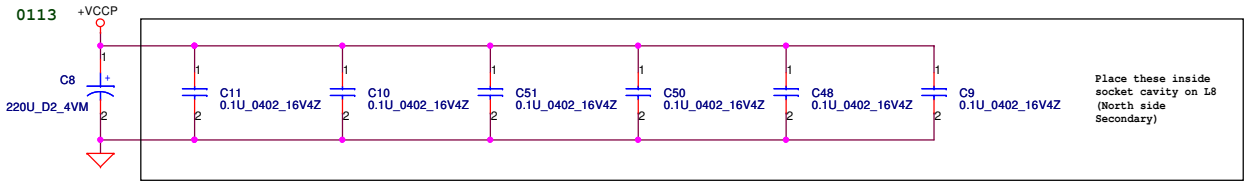


Mid Frequence Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF

Delete "REMOVE?" 0113



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Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.

Title: **Penryn (3/3)**

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H_D#0

H_D#2
H_D#3
H_D#4

H_D#6
H_D#7
H_D#8
H_D#9
H_D#10
H_D#11

H_D#13
H_D#14
H_D#15
H_D#16

H_D#18
H_D#19
H_D#20
H_D#21
H_D#22

H_D#25
H_D#26
H_D#27
H_D#28
H_D#29
H_D#30
H_D#31
H_D#32
H_D#33

H_D#36

H_D#39

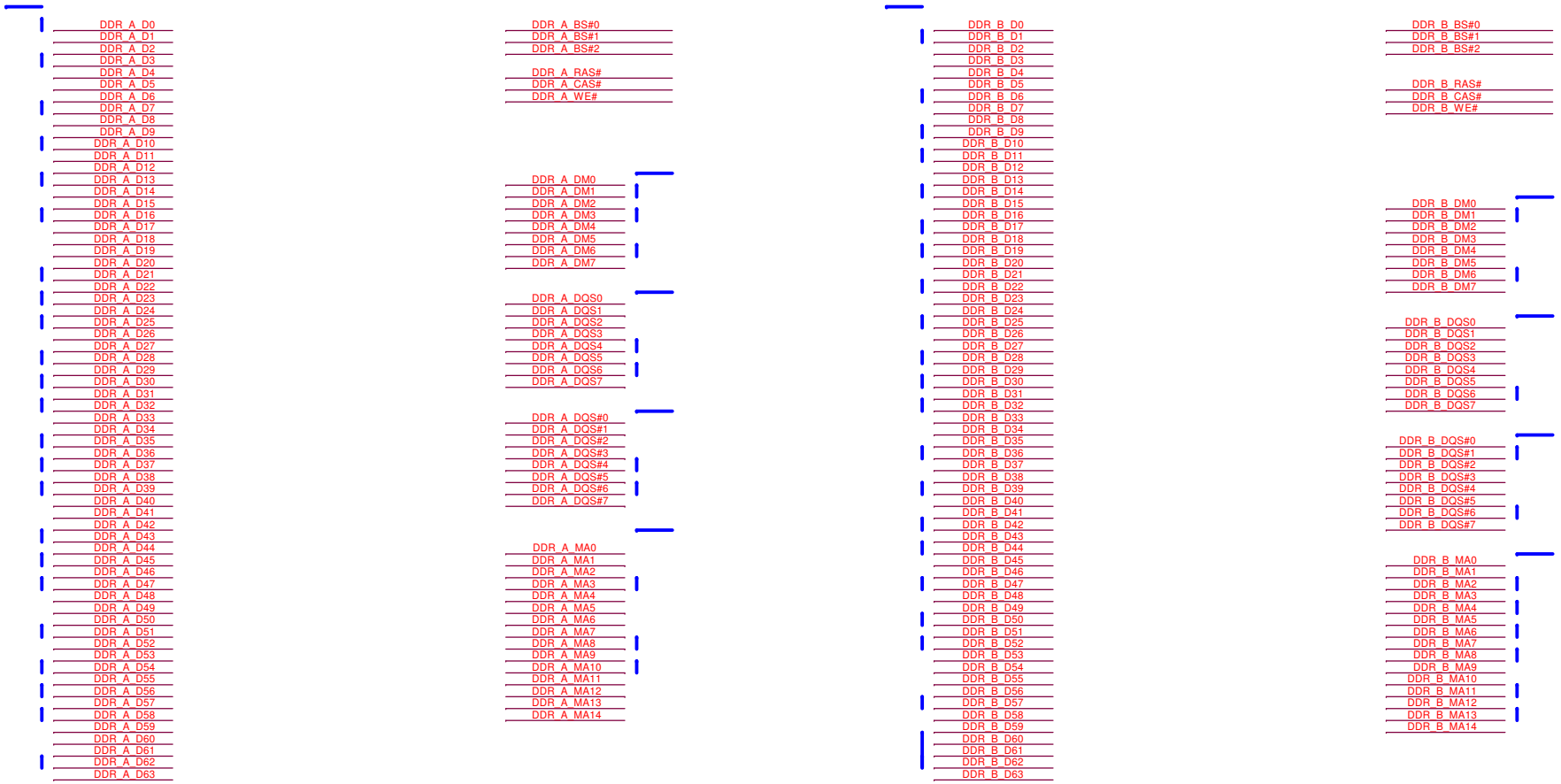
H_D#41
H_D#42
H_D#43
H_D#44
H_D#45
H_D#46
H_D#47
H_D#48

H_D#52
H_D#53
H_D#54

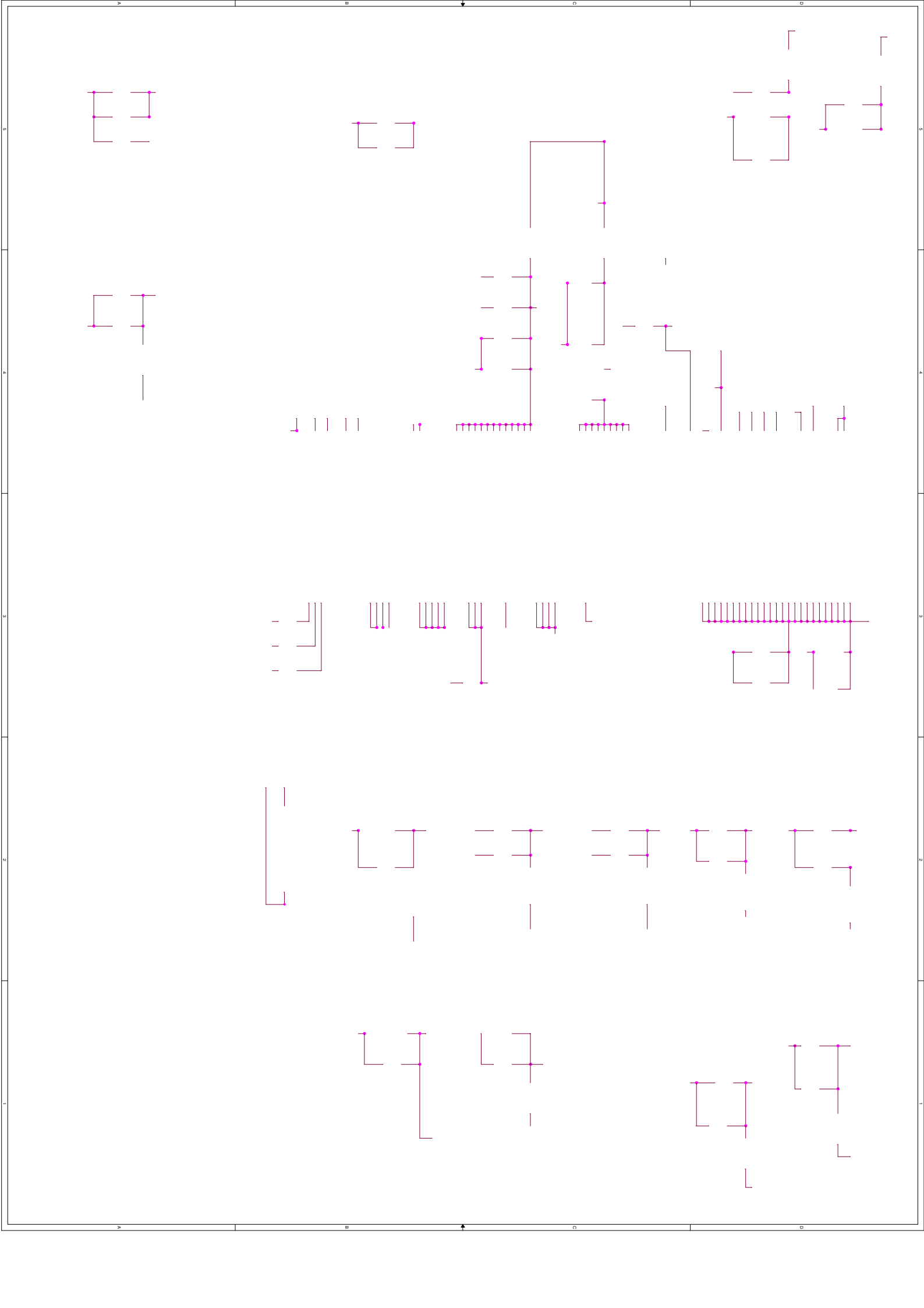
H_D#57
H_D#58
H_D#59
H_D#60
H_D#61
H_D#62

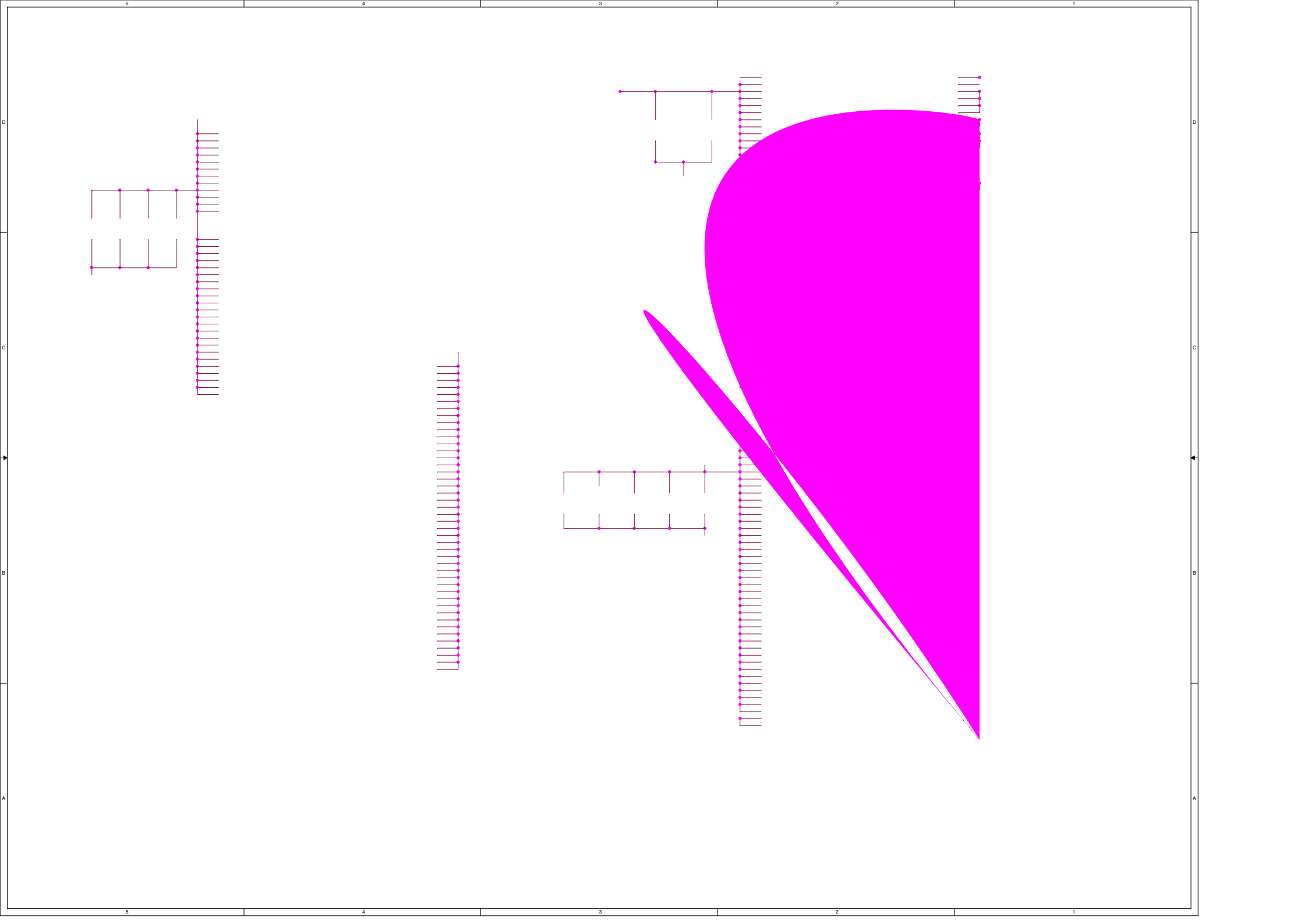
H_RESET#
H_CPUSLP#

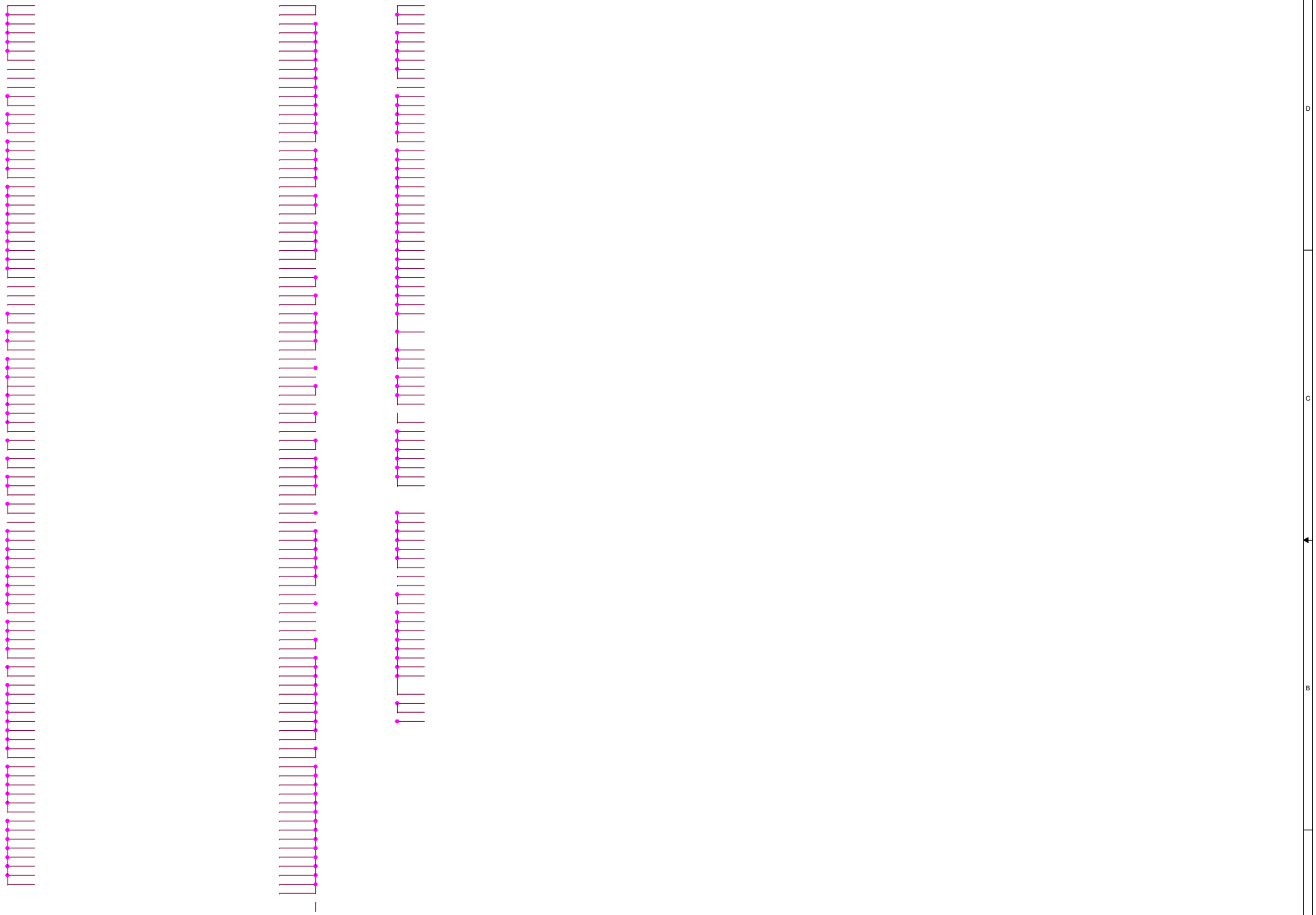
SM_REXT
TP_SM_DRAMRST#

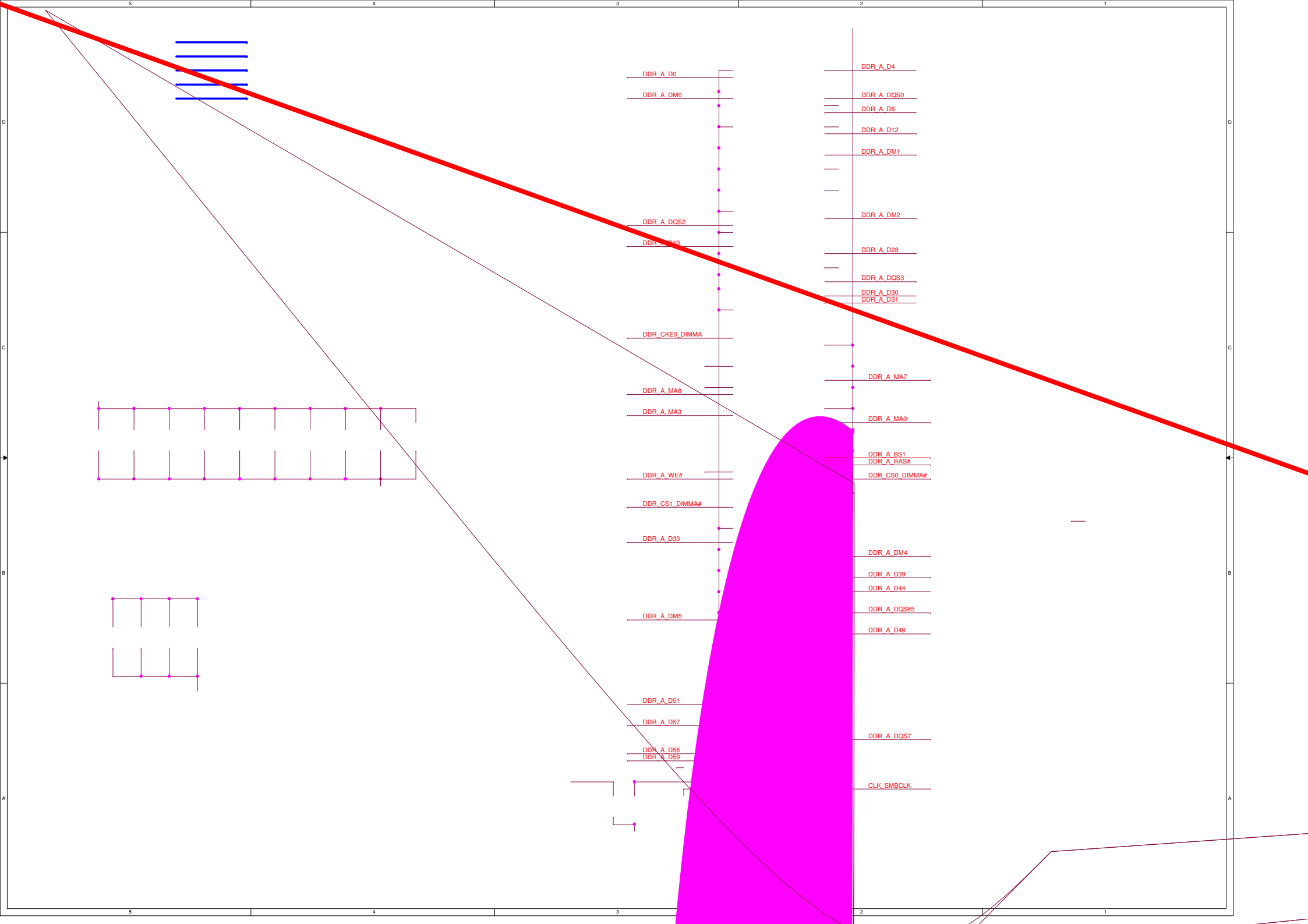

DDR_A_D0
DDR_A_D1
DDR_A_D2
DDR_A_D3
DDR_A_D4
DDR_A_D5
DDR_A_D6
DDR_A_D7
DDR_A_D8
DDR_A_D9
DDR_A_D10
DDR_A_D11
DDR_A_D12
DDR_A_D13
DDR_A_D14
DDR_A_D15
DDR_A_D16
DDR_A_D17
DDR_A_D18
DDR_A_D19
DDR_A_D20
DDR_A_D21
DDR_A_D22
DDR_A_D23
DDR_A_D24
DDR_A_D25
DDR_A_D26
DDR_A_D27
DDR_A_D28
DDR_A_D29
DDR_A_D30
DDR_A_D31
DDR_A_D32
DDR_A_D33
DDR_A_D34
DDR_A_D35
DDR_A_D36
DDR_A_D37
DDR_A_D38
DDR_A_D39
DDR_A_D40
DDR_A_D41
DDR_A_D42
DDR_A_D43
DDR_A_D44
DDR_A_D45
DDR_A_D46
DDR_A_D47
DDR_A_D48
DDR_A_D49
DDR_A_D50
DDR_A_D51
DDR_A_D52
DDR_A_D53
DDR_A_D54
DDR_A_D55
DDR_A_D56
DDR_A_D57
DDR_A_D58
DDR_A_D59
DDR_A_D60
DDR_A_D61
DDR_A_D62
DDR_A_D63
DDR_A_BS#0
DDR_A_BS#1
DDR_A_BS#2
DDR_A_RAS#
DDR_A_CAS#
DDR_A_WE#
DDR_A_DM0
DDR_A_DM1
DDR_A_DM2
DDR_A_DM3
DDR_A_DM4
DDR_A_DM5
DDR_A_DM6
DDR_A_DM7
DDR_A_DQS0
DDR_A_DQS1
DDR_A_DQS2
DDR_A_DQS3
DDR_A_DQS4
DDR_A_DQS5
DDR_A_DQS6
DDR_A_DQS7
DDR_A_DQS#0
DDR_A_DQS#1
DDR_A_DQS#2
DDR_A_DQS#3
DDR_A_DQS#4
DDR_A_DQS#5
DDR_A_DQS#6
DDR_A_DQS#7
DDR_A_MA0
DDR_A_MA1
DDR_A_MA2
DDR_A_MA3
DDR_A_MA4
DDR_A_MA5
DDR_A_MA6
DDR_A_MA7
DDR_A_MA8
DDR_A_MA9
DDR_A_MA10
DDR_A_MA11
DDR_A_MA12
DDR_A_MA13
DDR_A_MA14
DDR_B_D0
DDR_B_D1
DDR_B_D2
DDR_B_D3
DDR_B_D4
DDR_B_D5
DDR_B_D6
DDR_B_D7
DDR_B_D8
DDR_B_D9
DDR_B_D10
DDR_B_D11
DDR_B_D12
DDR_B_D13
DDR_B_D14
DDR_B_D15
DDR_B_D16
DDR_B_D17
DDR_B_D18
DDR_B_D19
DDR_B_D20
DDR_B_D21
DDR_B_D22
DDR_B_D23
DDR_B_D24
DDR_B_D25
DDR_B_D26
DDR_B_D27
DDR_B_D28
DDR_B_D29
DDR_B_D30
DDR_B_D31
DDR_B_D32
DDR_B_D33
DDR_B_D34
DDR_B_D35
DDR_B_D36
DDR_B_D37
DDR_B_D38
DDR_B_D39
DDR_B_D40
DDR_B_D41
DDR_B_D42
DDR_B_D43
DDR_B_D44
DDR_B_D45
DDR_B_D46
DDR_B_D47
DDR_B_D48
DDR_B_D49
DDR_B_D50
DDR_B_D51
DDR_B_D52
DDR_B_D53
DDR_B_D54
DDR_B_D55
DDR_B_D56
DDR_B_D57
DDR_B_D58
DDR_B_D59
DDR_B_D60
DDR_B_D61
DDR_B_D62
DDR_B_D63
DDR_B_BS#0
DDR_B_BS#1
DDR_B_BS#2
DDR_B_RAS#
DDR_B_CAS#
DDR_B_WE#
DDR_B_DM0
DDR_B_DM1
DDR_B_DM2
DDR_B_DM3
DDR_B_DM4
DDR_B_DM5
DDR_B_DM6
DDR_B_DM7
DDR_B_DQS0
DDR_B_DQS1
DDR_B_DQS2
DDR_B_DQS3
DDR_B_DQS4
DDR_B_DQS5
DDR_B_DQS6
DDR_B_DQS7
DDR_B_DQS#0
DDR_B_DQS#1
DDR_B_DQS#2
DDR_B_DQS#3
DDR_B_DQS#4
DDR_B_DQS#5
DDR_B_DQS#6
DDR_B_DQS#7
DDR_B_MA0
DDR_B_MA1
DDR_B_MA2
DDR_B_MA3
DDR_B_MA4
DDR_B_MA5
DDR_B_MA6
DDR_B_MA7
DDR_B_MA8
DDR_B_MA9
DDR_B_MA10
DDR_B_MA11
DDR_B_MA12
DDR_B_MA13
DDR_B_MA14


GMCH_ENBKL
GM_ENVDD
GMCH_CRT_R
GMCH_CRT_G
GMCH_CRT_B
GMCH_CRT_B
GMCH_CRT_G
GMCH_CRT_R





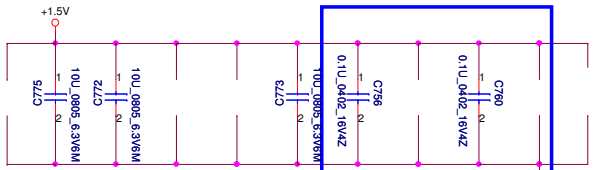



DDR_A_D0
DDR_A_DM0
DDR_A_DQS2
DDR_A_D19
DDR_CKE0_DIMMA
DDR_A_MA8
DDR_A_MA3
DDR_A_WE#
DDR_CS1_DIMMA#
DDR_A_D33
DDR_A_DM5
DDR_A_D51
DDR_A_D57
DDR_A_D58
DDR_A_D59
DDR_A_D4
DDR_A_DQS0
DDR_A_D6
DDR_A_D12
DDR_A_DM1
DDR_A_DM2
DDR_A_D28
DDR_A_DQS3
DDR_A_D30
DDR_A_D31
DDR_A_MA7
DDR_A_MA0
DDR_A_BS1
DDR_A_RAS#
DDR_CS0_DIMMA#
DDR_A_DM4
DDR_A_D39
DDR_A_D44
DDR_A_DQS#5
DDR_A_D46
DDR_A_DQS7
CLK_SMBCLK

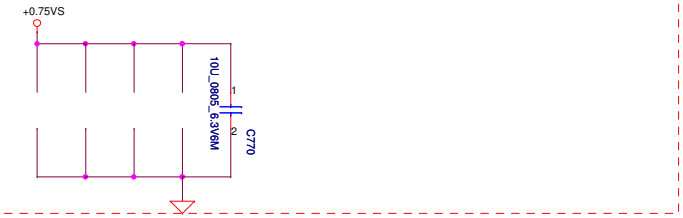
(9) DDR_B_DQS#[0..7]
(9) DDR_B_D[0..63]
(9) DDR_B_DM[0..7]
(9) DDR_B_DQS[0..7]
(9) DDR_B_MA[0..14]

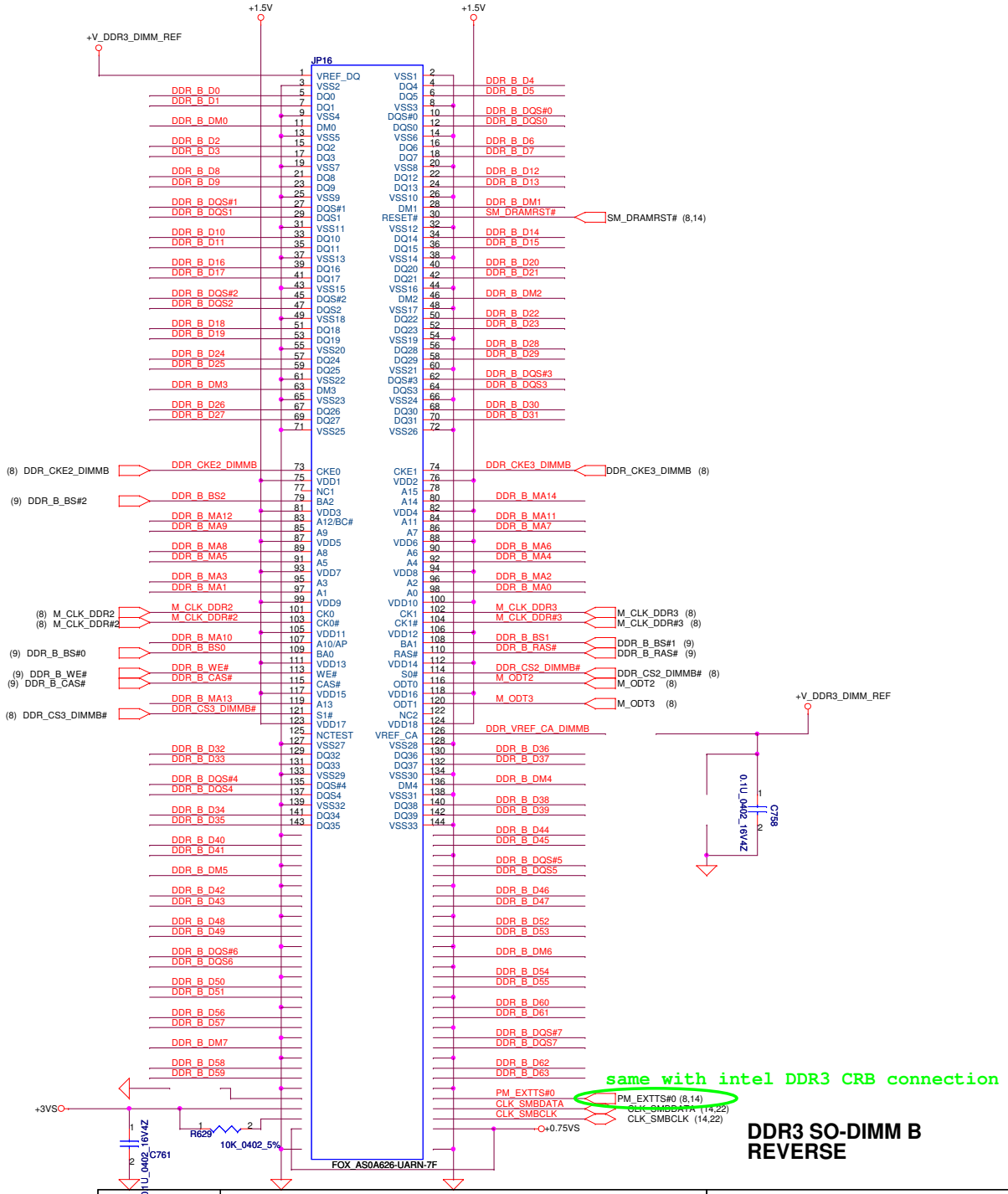
Layout Note:
Place near JP5

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JP5.203 & JP5.204



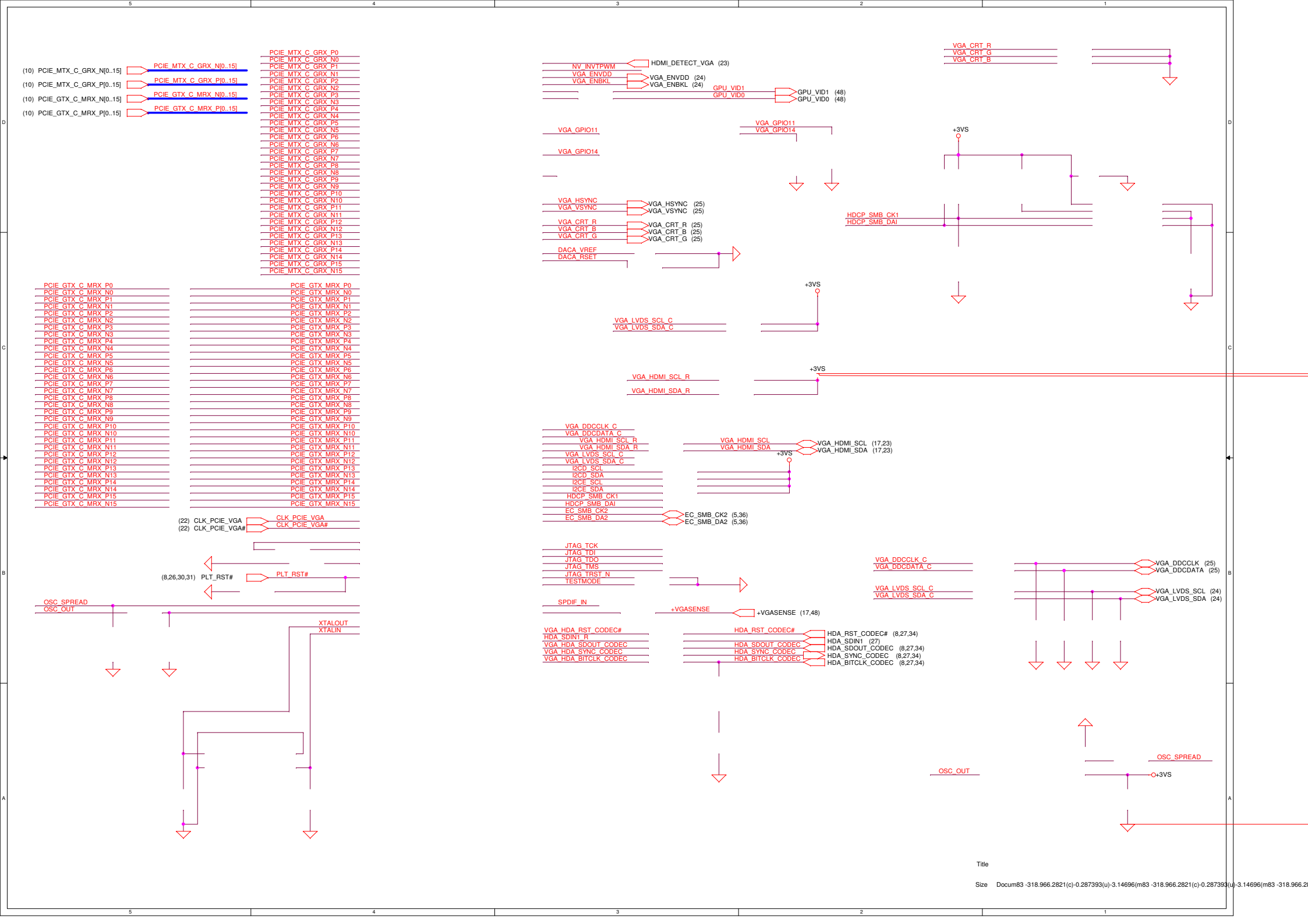


same with intel DDR3 CRB connection

DDR3 SO-DIMM B
REVERSE

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.			
Title: DDRIII-SODIMM SLOT2			
Size	Document Number: KIWAX_LA-5081P		Rev: 1.0
Date: Tuesday, April 28, 2009	Sheet 15 of 51		


(10) PCIE_MTX_C_GRX_N[0..15]
PCIE_MTX_C_GRX_N[0..15]
(10) PCIE_MTX_C_GRX_P[0..15]
PCIE_MTX_C_GRX_P[0..15]
(10) PCIE_GTX_C_MRX_N[0..15]
PCIE_GTX_C_MRX_N[0..15]
(10) PCIE_GTX_C_MRX_P[0..15]
PCIE_GTX_C_MRX_P[0..15]
PCIE_MTX_C_GRX_P0
PCIE_MTX_C_GRX_N0
PCIE_MTX_C_GRX_P1
PCIE_MTX_C_GRX_N1
PCIE_MTX_C_GRX_P2
PCIE_MTX_C_GRX_N2
PCIE_MTX_C_GRX_P3
PCIE_MTX_C_GRX_N3
PCIE_MTX_C_GRX_P4
PCIE_MTX_C_GRX_N4
PCIE_MTX_C_GRX_P5
PCIE_MTX_C_GRX_N5
PCIE_MTX_C_GRX_P6
PCIE_MTX_C_GRX_N6
PCIE_MTX_C_GRX_P7
PCIE_MTX_C_GRX_N7
PCIE_MTX_C_GRX_P8
PCIE_MTX_C_GRX_N8
PCIE_MTX_C_GRX_P9
PCIE_MTX_C_GRX_N9
PCIE_MTX_C_GRX_P10
PCIE_MTX_C_GRX_N10
PCIE_MTX_C_GRX_P11
PCIE_MTX_C_GRX_N11
PCIE_MTX_C_GRX_P12
PCIE_MTX_C_GRX_N12
PCIE_MTX_C_GRX_P13
PCIE_MTX_C_GRX_N13
PCIE_MTX_C_GRX_P14
PCIE_MTX_C_GRX_N14
PCIE_MTX_C_GRX_P15
PCIE_MTX_C_GRX_N15
PCIE_GTX_C_MRX_P0
PCIE_GTX_C_MRX_N0
PCIE_GTX_C_MRX_P1
PCIE_GTX_C_MRX_N1
PCIE_GTX_C_MRX_P2
PCIE_GTX_C_MRX_N2
PCIE_GTX_C_MRX_P3
PCIE_GTX_C_MRX_N3
PCIE_GTX_C_MRX_P4
PCIE_GTX_C_MRX_N4
PCIE_GTX_C_MRX_P5
PCIE_GTX_C_MRX_N5
PCIE_GTX_C_MRX_P6
PCIE_GTX_C_MRX_N6
PCIE_GTX_C_MRX_P7
PCIE_GTX_C_MRX_N7
PCIE_GTX_C_MRX_P8
PCIE_GTX_C_MRX_N8
PCIE_GTX_C_MRX_P9
PCIE_GTX_C_MRX_N9
PCIE_GTX_C_MRX_P10
PCIE_GTX_C_MRX_N10
PCIE_GTX_C_MRX_P11
PCIE_GTX_C_MRX_N11
PCIE_GTX_C_MRX_P12
PCIE_GTX_C_MRX_N12
PCIE_GTX_C_MRX_P13
PCIE_GTX_C_MRX_N13
PCIE_GTX_C_MRX_P14
PCIE_GTX_C_MRX_N14
PCIE_GTX_C_MRX_P15
PCIE_GTX_C_MRX_N15
PCIE_GTX_MRX_P0
PCIE_GTX_MRX_N0
PCIE_GTX_MRX_P1
PCIE_GTX_MRX_N1
PCIE_GTX_MRX_P2
PCIE_GTX_MRX_N2
PCIE_GTX_MRX_P3
PCIE_GTX_MRX_N3
PCIE_GTX_MRX_P4
PCIE_GTX_MRX_N4
PCIE_GTX_MRX_P5
PCIE_GTX_MRX_N5
PCIE_GTX_MRX_P6
PCIE_GTX_MRX_N6
PCIE_GTX_MRX_P7
PCIE_GTX_MRX_N7
PCIE_GTX_MRX_P8
PCIE_GTX_MRX_N8
PCIE_GTX_MRX_P9
PCIE_GTX_MRX_N9
PCIE_GTX_MRX_P10
PCIE_GTX_MRX_N10
PCIE_GTX_MRX_P11
PCIE_GTX_MRX_N11
PCIE_GTX_MRX_P12
PCIE_GTX_MRX_N12
PCIE_GTX_MRX_P13
PCIE_GTX_MRX_N13
PCIE_GTX_MRX_P14
PCIE_GTX_MRX_N14
PCIE_GTX_MRX_P15
PCIE_GTX_MRX_N15
(22) CLK_PCIE_VGA
(22) CLK_PCIE_VGA#
CLK_PCIE_VGA
CLK_PCIE_VGA#
(8,26,30,31) PLT_RST#
PLT_RST#
OSC_SPREAD
OSC_OUT
XTALOUT
XTALIN
NV_INVTPWM
HDMI_DETECT_VGA (23)
VGA_ENVDD
VGA_ENBKL
VGA_ENVDD (24)
VGA_ENBKL (24)
GPU_VID1
GPU_VID0
GPU_VID1 (48)
GPU_VID0 (48)
VGA_GPIO11
VGA_GPIO14
VGA_HSYNC
VGA_VSYNC
VGA_HSYNC (25)
VGA_VSYNC (25)
VGA_CRT_R
VGA_CRT_B
VGA_CRT_G
VGA_CRT_R (25)
VGA_CRT_B (25)
VGA_CRT_G (25)
DACA_VREF
DACA_RSET
VGA_LVDS_SCL_C
VGA_LVDS_SDA_C
VGA_HDMI_SCL_R
VGA_HDMI_SDA_R
VGA_DDCCLK_C
VGA_DDCDATA_C
VGA_HDMI_SCL_R
VGA_HDMI_SDA_R
VGA_LVDS_SCL_C
VGA_LVDS_SDA_C
I2CD_SCL
I2CD_SDA
I2CE_SCL
I2CE_SDA
HDCP_SMB_CK1
HDCP_SMB_DAI
EC_SMB_CK2
EC_SMB_DA2
EC_SMB_CK2 (5,36)
EC_SMB_DA2 (5,36)
VGA_HDMI_SCL
VGA_HDMI_SDA
VGA_HDMI_SCL (17,23)
VGA_HDMI_SDA (17,23)
+3VS
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST_N
TESTMODE
SPDIF_IN
+VGASENSE
+VGASENSE (17,48)
VGA_HDA_RST_CODEC#
HDA_SDIN1_R
VGA_HDA_SDOUT_CODEC
VGA_HDA_SYNC_CODEC
VGA_HDA_BITCLK_CODEC
HDA_RST_CODEC#
HDA_SDOUT_CODEC
HDA_SYNC_CODEC
HDA_BITCLK_CODEC
HDA_RST_CODEC# (8,27,34)
HDA_SDIN1 (27)
HDA_SDOUT_CODEC (8,27,34)
HDA_SYNC_CODEC (8,27,34)
HDA_BITCLK_CODEC (8,27,34)
VGA_CRT_R
VGA_CRT_G
VGA_CRT_B
VGA_GPIO11
VGA_GPIO14
+3VS
HDCP_SMB_CK1
HDCP_SMB_DAI
VGA_DDCCLK (25)
VGA_DDCDATA (25)
VGA_LVDS_SCL (24)
VGA_LVDS_SDA (24)
OSC_SPREAD
OSC_OUT
+3VS
Title
Size
Docum83 -318.966.2821(c)-0.287393(u)-3.14696(m83 -318.966.2821(c)-0.287393(u)-3.14696(m83 -318.966.2

FBAD0
FBAD1
FBAD2
FBAD3
FBAD4
FBAD5
FBAD6
FBAD7
FBAD8
FBAD9
FBAD10
FBAD11
FBAD12
FBAD13
FBAD14
FBAD15
FBAD16
FBAD17
FBAD18
FBAD19
FBAD20
FBAD21
FBAD22
FBAD23
FBAD24
FBAD25
FBAD26
FBAD27
FBAD28
FBAD29
FBAD30
FBAD31
FBAD32
FBAD33
FBAD34
FBAD35

FBAD62
FBAD63

FOR N10M 40NM , 1.1VS needs to be changed to 1.05VS

+VGA_CORE
13.56A
NEAR BALL
220U_25V_M
C1177
PM@
C1001
PM@
4.7U 6.3V K X5R 0603
NEAR BGA

PLACE NEAR BGA
+1.8VS
4.7U 6.3V K X5R 0603
C976
PM@

PLACE BELOW GPU
FBAVDDQ=2.24A
+1.8VS
4700P_0402_25V7K
C986
PM@
C997
PM@
4700P_0402_25V7K

NEAR BGA
80mA
+3VS
NEAR BALL

NEAR BALL
PEX_IOVDDQ=1.6A
PEX_IOVDD=500mA
PEX_PLLVDD=100mA
+1.1VS

+PEX_PLLVDD
+1.1VS_PLL
12~16mil
+FB_PLLAVDD
+FB_DLLAVDD
+DACA_VDD
+DACB_VDD
+DACC_VDD
MBK1608121YZF_0603
1U_0402_5260.91 c 2457 5260.91 2457 5260.91 v S 2456K
L27
PM@
C1017
PM@
NEAR BALL
PLLVDD=65mA
SP_PLLVDD=25mA
VID_PLLVDD=50mA

+1.8VS
+IFPA_IOVDD
+IFPB_IOVDD
+IFPC_IOVDD
12~16mil
10K_0402_5% R994
PM@
+IFPAB_PLLVDD
+IFPC_PLLVDD
110mA
NEAR BGA
NEAR BALL

+FB_PLLAVDD
+FB_PLLAVDD
C1024
PM@
4.7U 6.3V K X5R 0603
+FB_DLLAVDD
+1.1VS

+PEX_PLLVDD
C1028
PM@
0.01U_0402_16V7K
NEAR BALL
+1.1VS
NEAR BGA

IFPC_PLLVDD: please add option to support
both 1.8V (for G9X) and 3.3V(for GT21X)
+1.8VS
+3VS
+1.1VS
+IFPC_PLLVDD
+IFPC_IOVDD
NEAR BGA
NEAR BALL

260mA NEAR BGA
+1.8VS
+1.1VS
+IFPAB_PLLVDD
NEAR BALL
IFPAB_PLLVDD: please add option to support
both 1.8V(for G9X) and 1.05V(for GT21X)

+DACA_VDD
110mA
+3VS

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

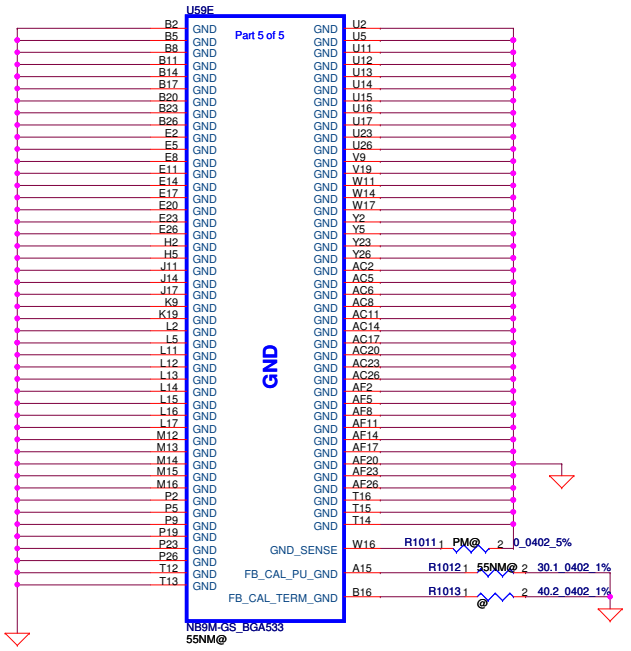
Compal Electronics, Inc.

Title: NB10M Power

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	1.0

Date: Tuesday, April 28, 2009 Sheet 18 of 51

A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available

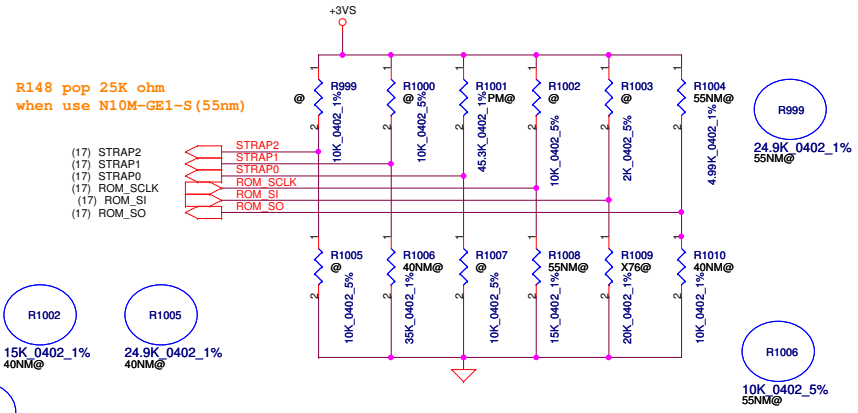


Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

To update for NV PUN-03304-001_V06 (2008/4/01)

U59
NB10M-GS-S
40NM@

R148 pop 25K ohm
when use N10M-GE1-S(55nm)



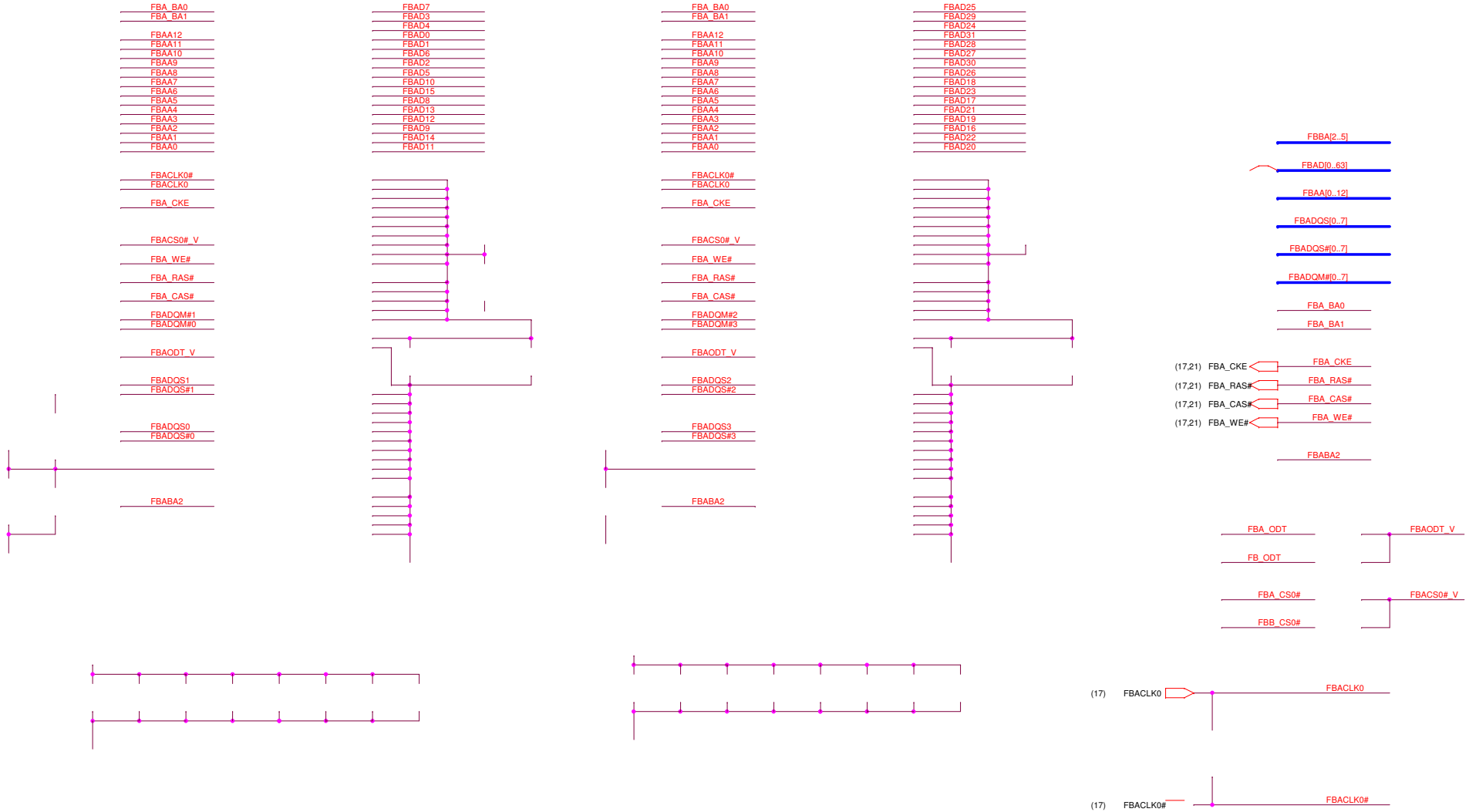
GB1 Family GPU Strap Options X76

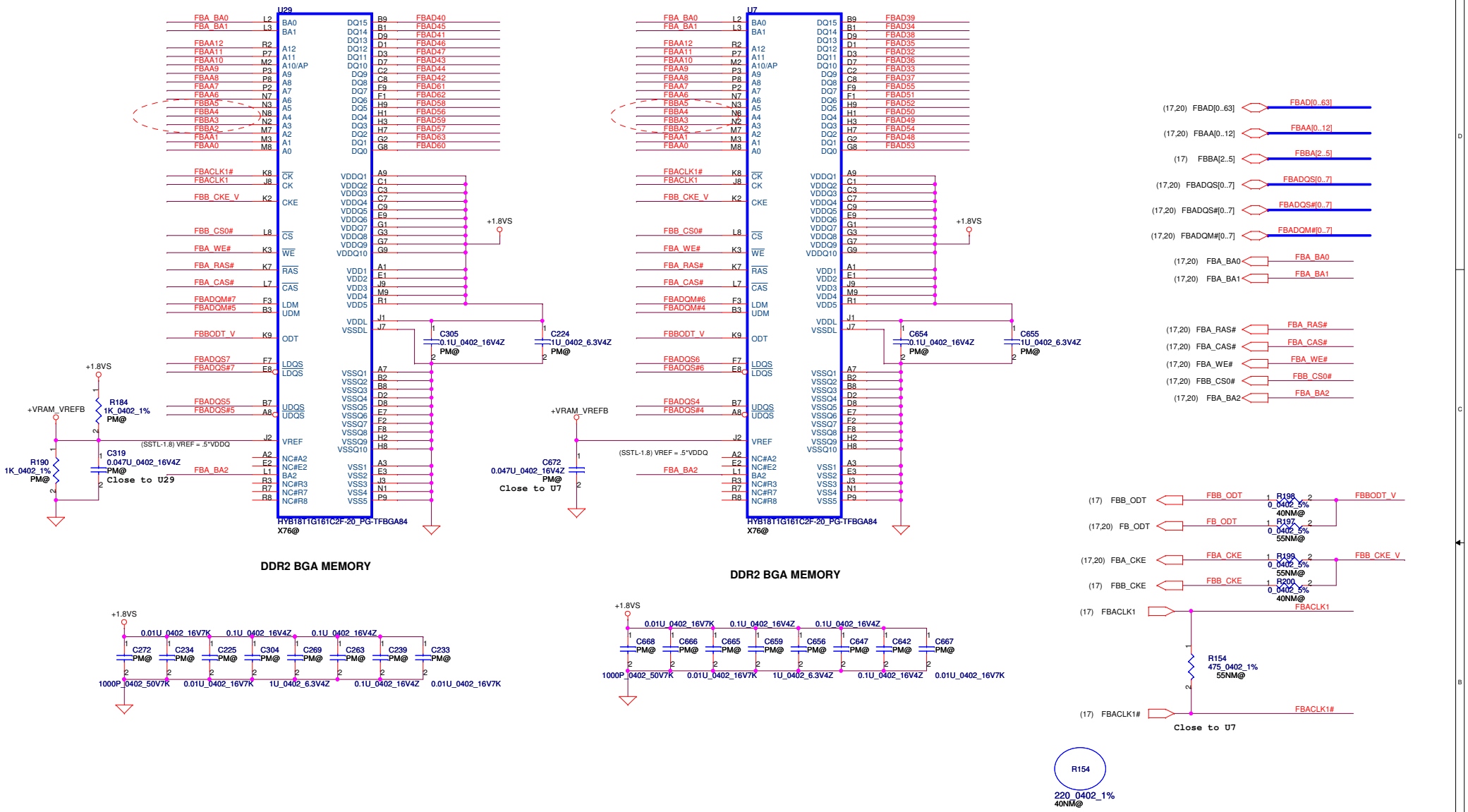
GPU	FB Memory (DDR2)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GE1-S (0x6EC) 55nm	Samsung	64Mx16	PU 5K	PD 15K	PD 20K	PU 25K	PD 10K	PU 45K
	Hynix	64Mx16	PU 5K	PD 15K	PD 5K	PU 25K	PD 10K	PU 45K
	Qimonda	64Mx16	PU 5K	PD 15K	PD 15K	PU 25K	PD 10K	PU 45K

4/23 update strap1 10K to 35K
according to N10M latest PUN

GPU	FB Memory (DDR2)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GS (0x6EC) 40nm	Samsung	64Mx16	PD 10K	PD 15K	PD 10K	PU 10K	PD 35K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 5K	PU 10K	PD 35K	PU 45K
	Qimonda	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 35K	PU 45K

Compal Electronics, Inc.
Title: N10M GND & STRAP
Size: B | Document Number: KIWA5/6 LA-5081P | Rev: 1.0
Date: Tuesday, April 28, 2009 | Sheet 19 of 51


FBA_BA0
FBA_BA1
FBAA12
FBAA11
FBAA10
FBAA9
FBAA8
FBAA7
FBAA6
FBAA5
FBAA4
FBAA3
FBAA2
FBAA1
FBAA0
FBACLK0#
FBACLK0
FBA_CKE
FBACS0#_V
FBA_WE#
FBA_RAS#
FBA_CAS#
FBADQM#1
FBADQM#0
FBAODT_V
FBADQS1
FBADQS#1
FBADQS0
FBADQS#0
FBABA2
FBAD7
FBAD3
FBAD4
FBAD0
FBAD1
FBAD6
FBAD2
FBAD5
FBAD10
FBAD15
FBAD8
FBAD13
FBAD12
FBAD9
FBAD14
FBAD11
FBA_BA0
FBA_BA1
FBAA12
FBAA11
FBAA10
FBAA9
FBAA8
FBAA7
FBAA6
FBAA5
FBAA4
FBAA3
FBAA2
FBAA1
FBAA0
FBACLK0#
FBACLK0
FBA_CKE
FBACS0#_V
FBA_WE#
FBA_RAS#
FBA_CAS#
FBADQM#2
FBADQM#3
FBAODT_V
FBADQS2
FBADQS#2
FBADQS3
FBADQS#3
FBABA2
FBAD25
FBAD29
FBAD24
FBAD31
FBAD28
FBAD27
FBAD30
FBAD26
FBAD18
FBAD23
FBAD17
FBAD21
FBAD19
FBAD16
FBAD22
FBAD20
FBBA[2..5]
FBAD[0..63]
FBAA[0..12]
FBADQS[0..7]
FBADQS#[0..7]
FBADQM#[0..7]
FBA_BA0
FBA_BA1
(17,21) FBA_CKE
FBA_CKE
(17,21) FBA_RAS#
FBA_RAS#
(17,21) FBA_CAS#
FBA_CAS#
(17,21) FBA_WE#
FBA_WE#
FBABA2
FBA_ODT
FBAODT_V
FB_ODT
FBA_CS0#
FBACS0#_V
FBB_CS0#
(17) FBACLK0
FBACLK0
(17) FBACLK0#
FBACLK0#



Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.			
Title: VRAM DDRB			
Size: Custom	Document Number: KIWA5/6 LA-5081P		Rev: 1.0
Date: Tuesday, April 28, 2009	Sheet 21 of 51		

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

SA000020K00 (Silego : SLG8SP556VTR)

SA000020H00 (ICS : ICS9LPRS387AKLFT)

BOM Structure

BOM Structure

+3VSM_CK505

+3VS R668 1 2 0_0805_5%

C812 0.1U_0402_16V4Z

C814 0.1U_0402_16V4Z

C815 0.1U_0402_16V4Z

C817 0.1U_0402_16V4Z

+1.5VS R672 1 2 @0_0805_5%

+VCCP R673 1 2 0_0805_5%

+VDD_CK505

C818 10U_0805_10V4Z

C819 0.1U_0402_16V4Z

C820 0.1U_0402_16V4Z

C821 0.1U_0402_16V4Z

C822 0.1U_0402_16V4Z

C824 0.1U_0402_16V4Z

+3VS

R669 1 2 0_0402_5%

R670 2.2K_0402_5%

R671 2.2K_0402_5%

2N7002DW-T/R7_SOT363-6 Q1A

(28,30) ICH_SMBDATA

CLK_SMBDATA

Q1B

(28,30) ICH_SMBCLK

CLK_SMBCLK

R674 1 2 0_0402_5%

+VCCP

R675 56_0402_5%

(6) CPU_BSEL0 R678 1 2 0_0402_5%

R679 1K_0402_5%

MCH_CLKSEL0 (8)

R686 1K_0402_5%

FSB R688 1 2 1K_0402_5%

(6) CPU_BSEL1 R690 1 2 0_0402_5%

R691 0_0402_5%

MCH_CLKSEL1 (8)

R692 1K_0402_5%

FSC R696 1 2 10K_0402_5%

R697 1 2 1K_0402_5%

(6) CPU_BSEL2 R699 1 2 0_0402_5%

R704 0_0402_5%

MCH_CLKSEL2 (8)

+3VSM_CK505

U30

VDD_SRC	55		
VDD_REF	6		
VDD_PCI	12		
VDD_CPU	72		
VDD_48	19		
VDD_PLL3	27		
VDD_CPU_IO	66		
VDD_PLL3_IO	31		
VDD_SRC_IO	62		
VDD_SRC_IO	52		
VDD_IO	23		
VDD_SRC_IO	38		
USB_0/FS_A	20	FSA	
FS_B/TEST_MODE	2	FSB	
REF_0/FS_C/TEST_	7	FSC	
REF_1	8		
CKPWRGD/PD#	1	CK_PWRGD	(28) CK_PWRGD
NC	11		
CPU_STOP#	53	PM_STP_CPU#	(28) H_STP_CPU#
PCI_STOP#	54	PM_STP_PCI#	(28) H_STP_PCI#
XTAL_IN	5	CLK_XTAL_IN	
XTAL_OUT	4	CLK_XTAL_OUT	
PCI_1	13		
PCI_2	14	PCI2_TME	(38) CLK_PCI_DB
PCI_3	15		
PCI_4/SEL_LCDCL	16	PCI4_SEL	(36) CLK_PCI_LPC
PCIF_5/ITP_EN	17	ITP_EN	(26) CLK_PCI_ICH
VSS_PCI	18		
VSS_REF	3		
VSS_48	22		
VSS_IO	26		
VSS_CPU	69		
VSS_PLL3	30		
VSS_SRC	34		
VSS_SRC	59		
VSS_SRC	42		
VSS	73		

SLG8SP556VTR_QFN72_10X10

SDA	9	CLK_SMBDATA → CLK_SMBDATA (14,15)
SCL	10	CLK_SMBCLK → CLK_SMBCLK (14,15)
CPU_0	71	CLK_CPU_BCLK → CLK_CPU_BCLK (5)
CPU_0#	70	CLK_CPU_BCLK# → CLK_CPU_BCLK# (5)
CPU_1	68	CLK_MCH_BCLK → CLK_MCH_BCLK (8)
CPU_1#	67	CLK_MCH_BCLK# → CLK_MCH_BCLK# (8)
SRC_0/DOT_96	24	R_CLK_DOT R677 GM@ 0_0402_5% → CLK_MCH_DREFCLK (8)
SRC_0#/DOT_96#	25	R_CLK_DOT# R681 PM@ 0_0402_5% → CLK_PCIE_VGA (16); R683 PM@ 0_0402_5% → CLK_MCH_DREFCLK# (8), CLK_PCIE_VGA# (16)
LCDCLK/27M	28	MCH_SSCDREFCLK (8)
LCDCLK#/27M_SS	29	MCH_SSCDREFCLK# (8)
SRC_2	32	CLK_MCH_3GPLL → CLK_MCH_3GPLL (8)
SRC_2#	33	CLK_MCH_3GPLL# → CLK_MCH_3GPLL# (8)
SRC_3	35	CLK_PCIE_EXP → CLK_PCIE_EXP (30)
SRC_3#	36	CLK_PCIE_EXP# → CLK_PCIE_EXP# (30)
SRC_4	39	CLK_PCIE_WLAN2 → T153
SRC_4#	40	CLK_PCIE_WLAN2# → T154
SRC_6	57	CLK_PCIE_WLAN → T155
SRC_6#	56	CLK_PCIE_WLAN#
SRC_7	61	CLK_PCIE_WLAN1 → CLK_PCIE_WLAN1 (30)
SRC_7#	60	CLK_PCIE_WLAN1# → CLK_PCIE_WLAN1# (30)
SRC_8/CPU_ITP	64	
SRC_8#/CPU_ITP#	63	
SRC_9	44	CLK_PCIE_LAN → CLK_PCIE_LAN (31)
SRC_9#	45	CLK_PCIE_LAN# → CLK_PCIE_LAN# (31)
SRC_10	50	CLK_PCIE_ICH → CLK_PCIE_ICH (28)
SRC_10#	51	CLK_PCIE_ICH# → CLK_PCIE_ICH# (28)
SRC_11	48	CLK_PCIE_SATA → CLK_PCIE_SATA (27)
SRC_11#	47	CLK_PCIE_SATA# → CLK_PCIE_SATA# (27)
CLKREQ_3#	37	EXP_CLKREQ# → EXP_CLKREQ# (30)
CLKREQ_4#	41	WLAN_CLKREQ2# → WLAN_CLKREQ2#
CLKREQ_6#	58	WLAN_CLKREQ# → WLAN_CLKREQ#
CLKREQ_7#	65	WLAN_CLKREQ1# → WLAN_CLKREQ1# (30)
CLKREQ_9#	43	CLKREQ_LAN# → CLKREQ_LAN# (31)
SLKREQ_10#	49	
CLKREQ_11#	46	SATA_CLKREQ#_R → SATA_CLKREQ# (28)
USB_1/CLKREQ_A#	21	MCH_CLKREQ#_R → MCH_CLKREQ# (8)

CARD@

(37) CLK_48M_CR R684 1 2 12_0402_5%

(28) CLK_48M_ICH R685 1 2 12_0402_5%

(28) CLK_14M_ICH R687 1 2 33_0402_5%

(38) CLK_14M_SIO R689 1 2 @33_0402_5%

SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

+3VS

SATA_CLKREQ#_R R693 10K_0402_5%

EXP_CLKREQ# R694 10K_0402_5%

WLAN_CLKREQ1# R695 10K_0402_5%

MCH_CLKREQ#_R R698 10K_0402_5%

CLKREQ_LAN# R701 10K_0402_5%

WLAN_CLKREQ# R702 10K_0402_5%

WLAN_CLKREQ2# @

REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

+3VS

@ R707 10K_0402_5% ITP_EN

PM@ R708 10K_0402_5% PCI4_SEL

R709 10K_0402_5% PCI2_TME

GM@ R711 10K_0402_5%

R710 10K_0402_5%

@ R712 10K_0402_5%

C825 22P_0402_50V8J CLK_XTAL_IN

Y4 14.31818MHZ_16PF_DSX840GA

C828 22P_0402_50V8J CLK_XTAL_OUT

Routing the trace at least 10mil

CLK_48M_CR

CLK_48M_ICH

CLK_14M_ICH

CLK_14M_SIO

C829 @ 22P_0402_50V8J

C827 @ 22P_0402_50V8J

C830 @ 22P_0402_50V8J

place CAPs near Resistors of U10
For 3G RF noise .

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#

1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.

Title: Clock Generator CK505

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 1.0

Date: Tuesday, April 28, 2009 | Sheet 22 of 51

10/30 update PS8171 co-lay circuit
4/14 update 1442T co-lay circuit

P/N:SA00002D700 (8101T)
P/N:SA00001U920 (CH7318C)

For 8171

PIN NUM	8101T	8171
PIN1	GND	ASQ0
PIN3	PC0	PEQ
PIN4	PC1	PIO
PIN7	HPD#	HPDX
PIN10	RE_EN#	CEXT
PIN11	VCC	APD
PIN12	GND	ASQ1
PIN27	GND	EMI0
PIN33	VCC	EMI1
PIN34	DDCBUF_EN	DDCBUF
PIN35	CFG	PRE

For 8171 net name:
EMI0, EMI1
ASQ0, ASQ1
APD

TMDS pull down (500ohm) resistors for ATI M92-S2 XT

NEAR CONNECTOR

Reserved for CH7318C

place those component near JP? for NV request 0515

KIWB3/B4_LA4551P

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

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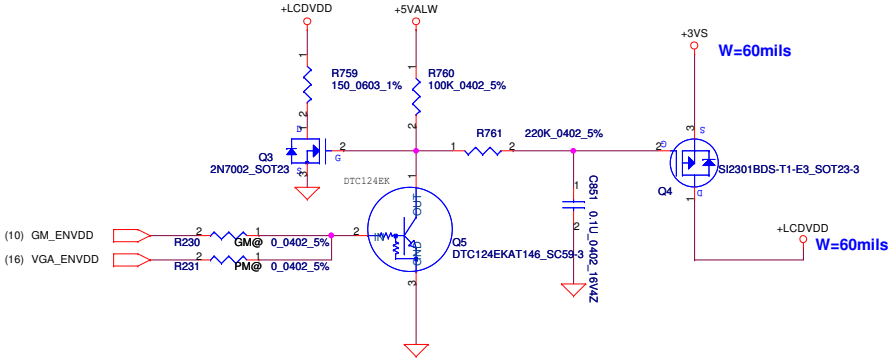
Compal Electronics, Inc.

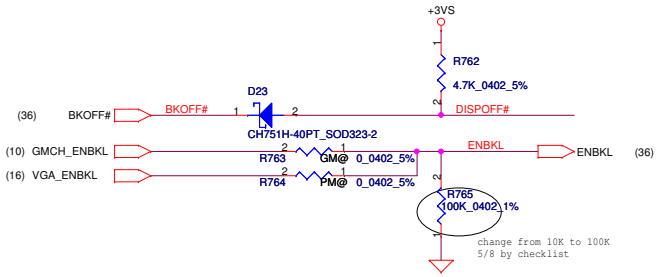
Title: Level Shiftter_PS8101T

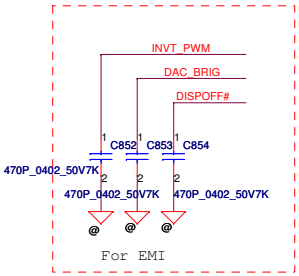
Size	Document Number	Rev
Custom	KIWAX_LA-5081P	1.0

Date: Tuesday, April 28, 2009 | Sheet 23 of 51

LCD POWER CIRCUIT

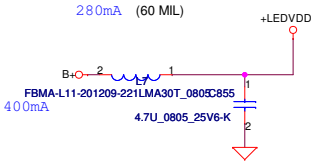


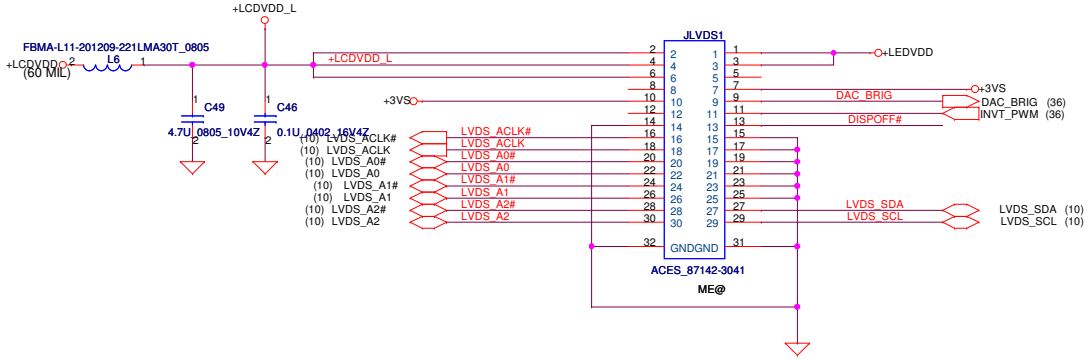


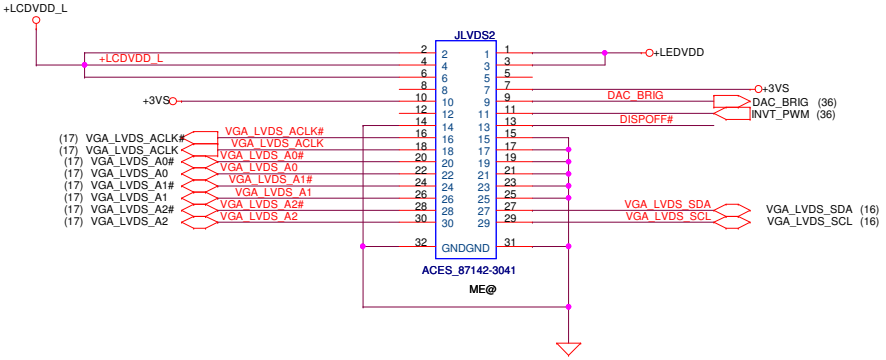


LCD/PANEL BD. Conn. FOR UMA

LCD/PANEL BD. Conn. FOR DIS

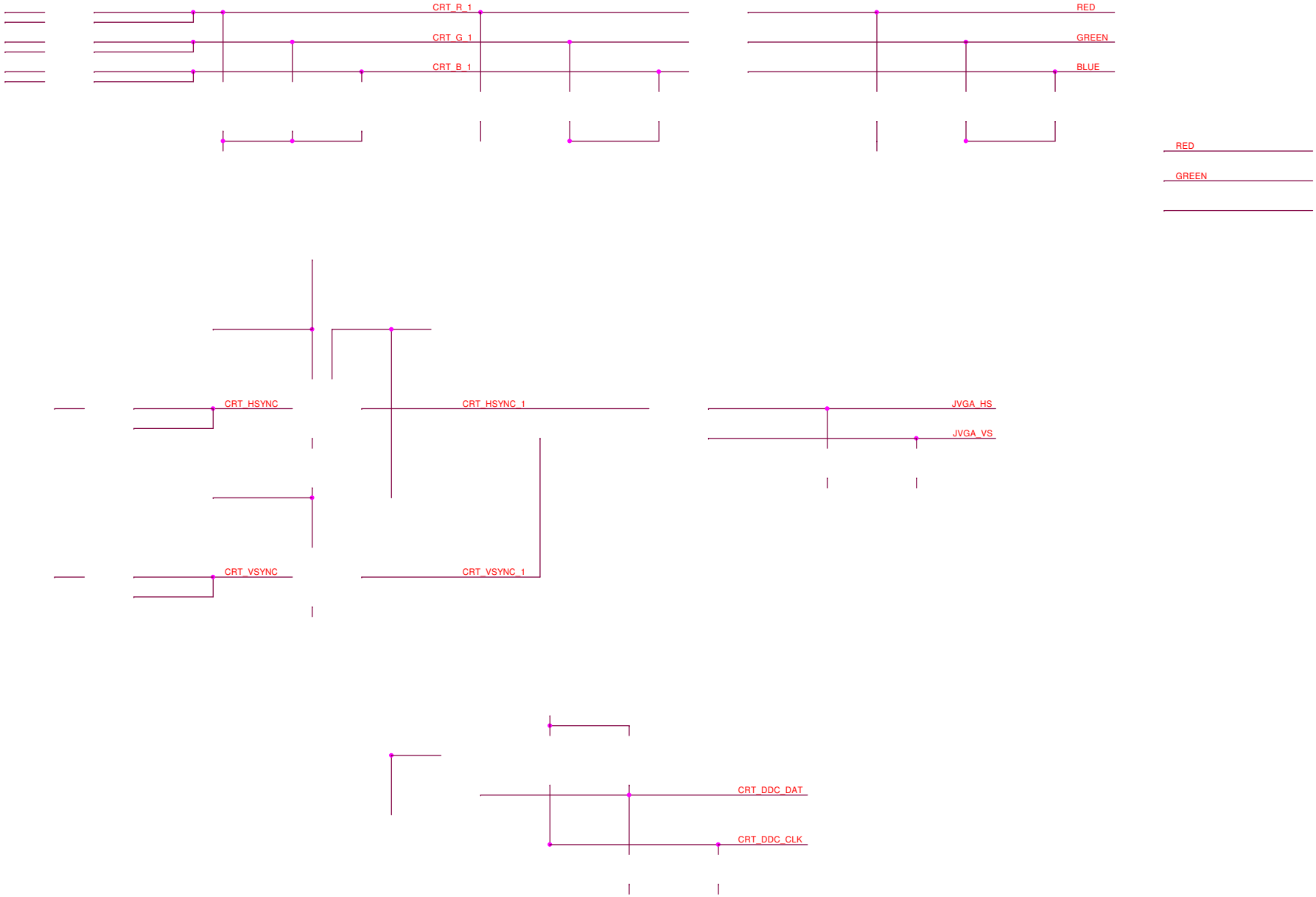


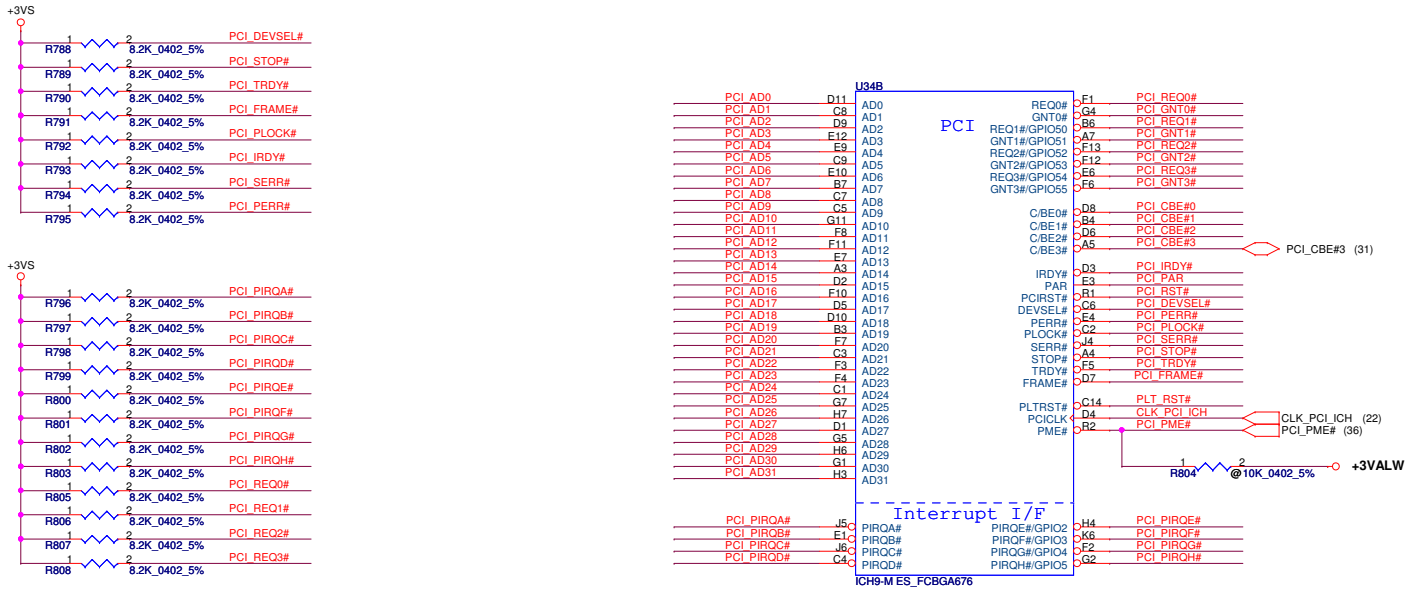




Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.			
Title: LVDS & DVI Connector			
Size: B	Document Number: KIWA5/6 LA-5081P		Rev: 1.0
Date: Tuesday, April 28, 2009	Sheet 24 of 51		


CRT_R_1
CRT_G_1
CRT_B_1
RED
GREEN
BLUE
RED
GREEN
CRT_HSYNC
CRT_HSYNC_1
JVGA_HS
JVGA_VS
CRT_VSYNC
CRT_VSYNC_1
CRT_DDC_DAT
CRT_DDC_CLK

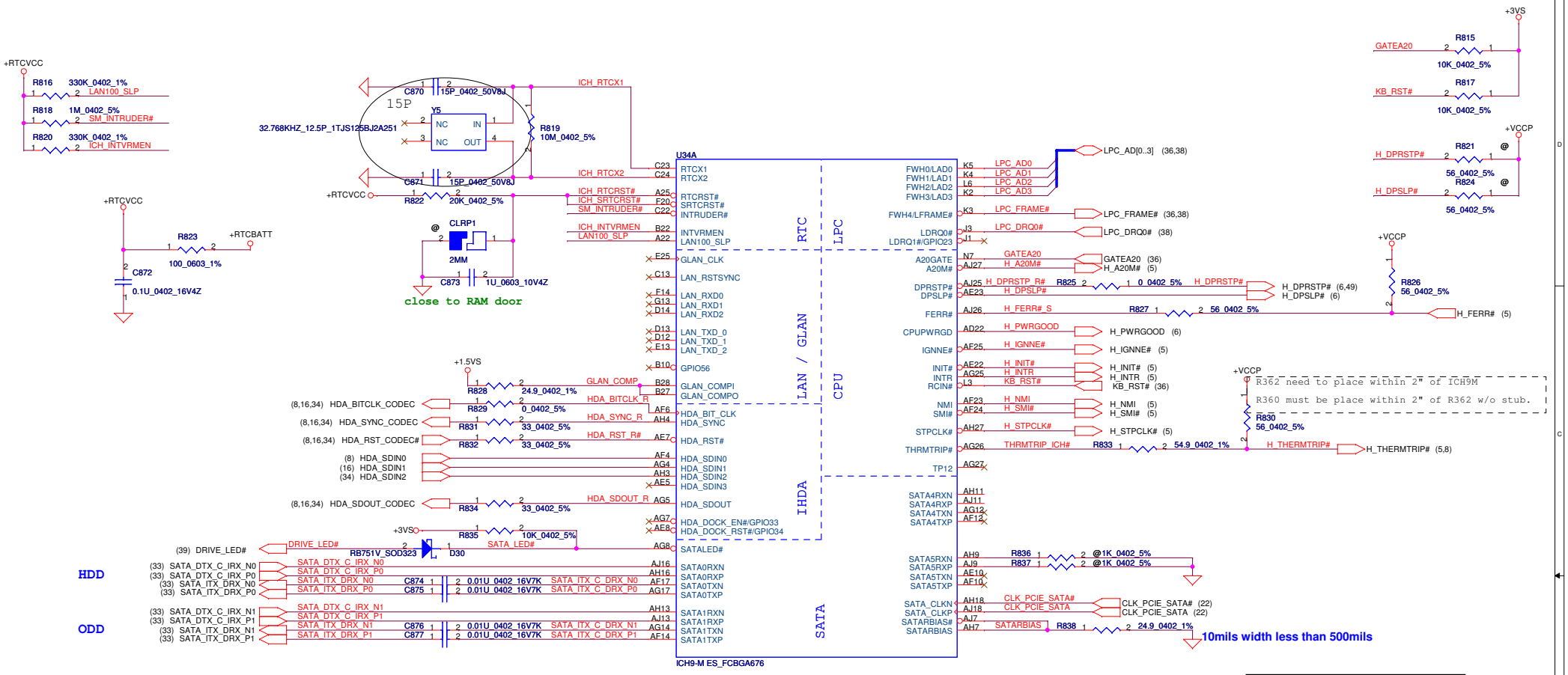


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.	
Title	ICH9M(1/4)-PCI
Size	Document Number: KIWA5/6 LA-5081P
Rev	1.0
Date: Tuesday, April 28, 2009	Sheet 26 of 51



SATA PORT LIST

PORT	DEVICE
0	HDD
1	ODD
4	E-SATA
5	

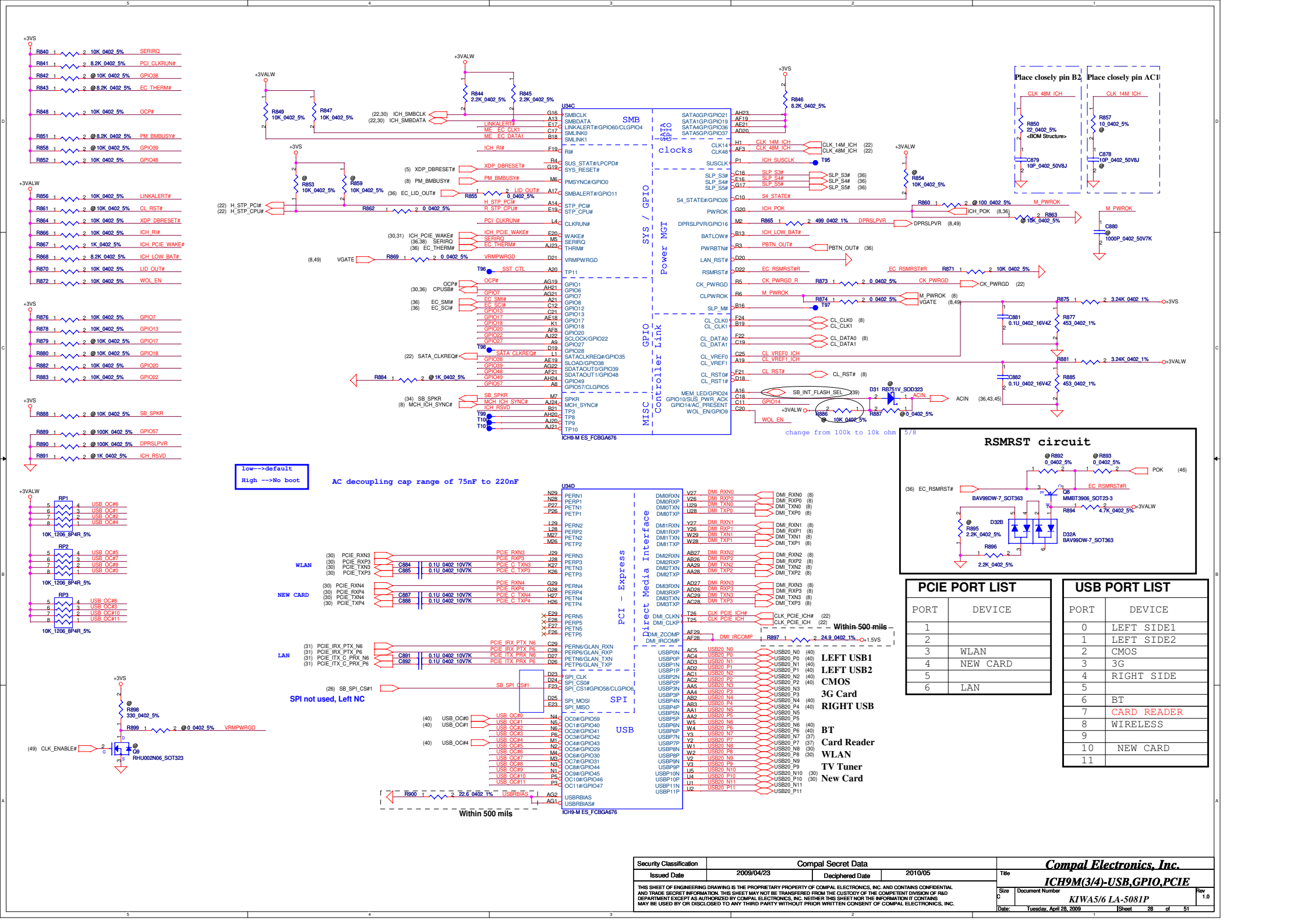
XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 1.0

Date: Tuesday, April 28, 2009 | Sheet 27 of 51



PCIE PORT LIST

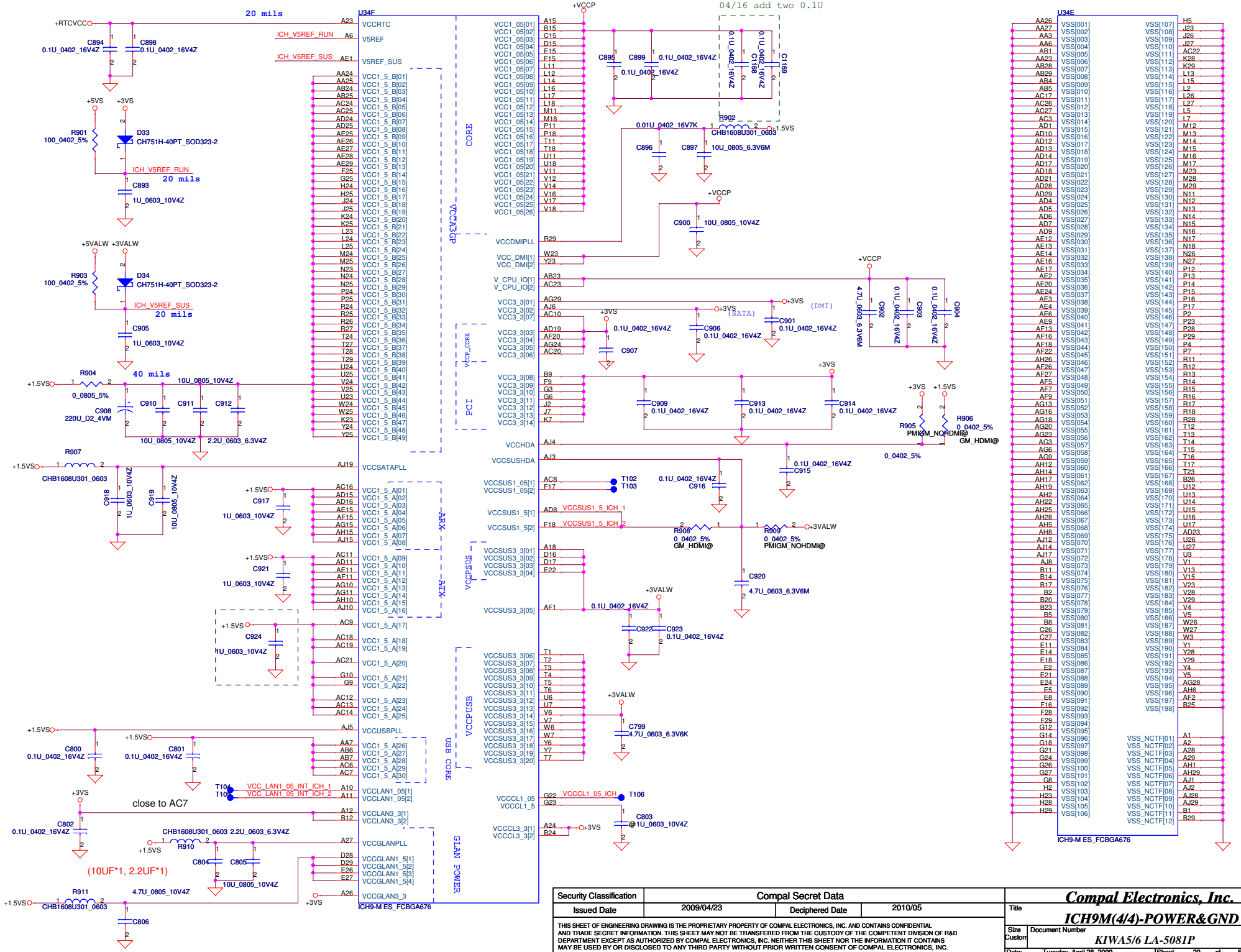
PORT	DEVICE
1	
2	
3	WLAN
4	NEW CARD
5	
6	LAN

USB PORT LIST

PORT	DEVICE
0	LEFT SIDE1
1	LEFT SIDE2
2	CMOS
3	3G
4	RIGHT SIDE
5	
6	BT
7	CARD READER
8	WIRELESS
9	
10	NEW CARD
11	

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

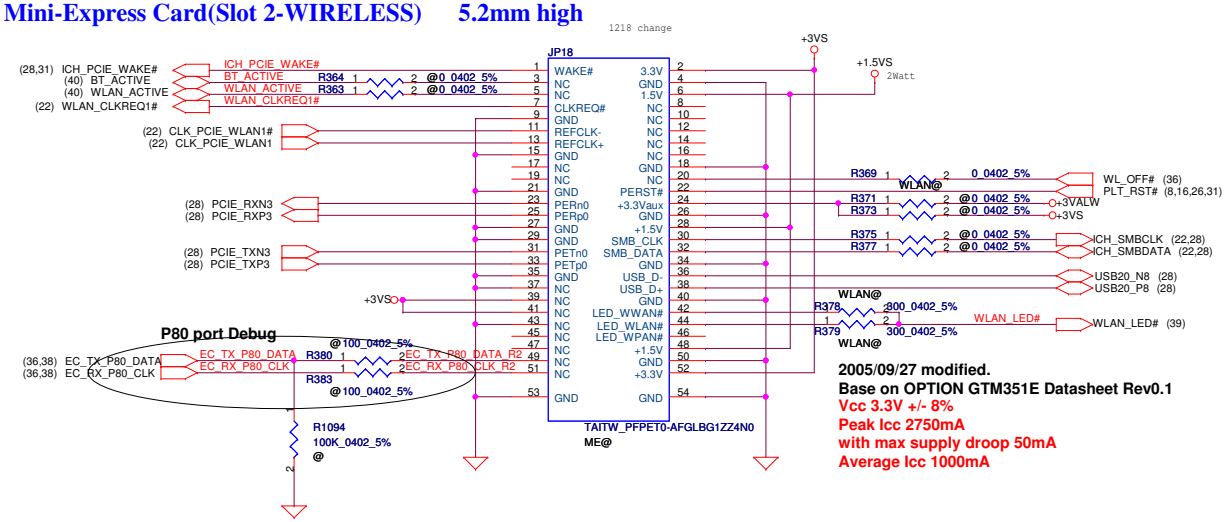
Title	Compal Electronics, Inc.		
	ICH9M(3/4)-USB,GPIO,PCIE		
Size	Document Number		Rev
C	KIWA5/6 LA-5081P		1.0
Date:	Tuesday, April 28, 2009	Sheet	28 of 51

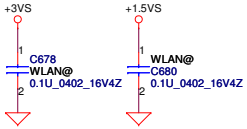


Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

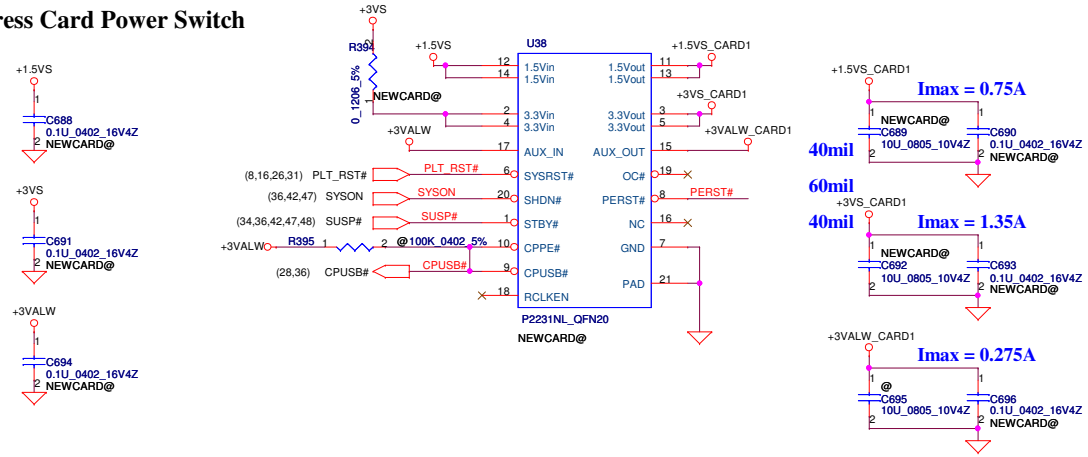
Compal Electronics, Inc.			
Title: ICH9M(4/4)-POWER&GND			
Size: Custom	Document Number: KIWA5/6 LA-5081P		Rev: 1.0
Date: Tuesday, April 28, 2009	Sheet 29 of 51		

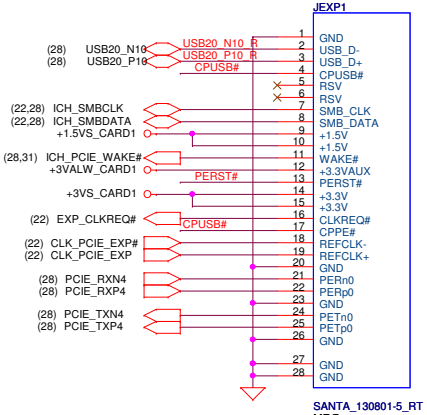
Mini-Express Card(Slot 2-WIRELESS) 5.2mm high





Express Card Power Switch





Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.			
Title: Mini-Card/3G/TV /BT			
Size	Document Number: KIWAX_LA-5081P		Rev: 1.0
Date: Tuesday, April 28, 2009	Sheet 30 of 51		

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

Layout Notice : 1.2V filter. Place as close chip as possible.

(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

Notice : 4.7u 6.3V capactor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

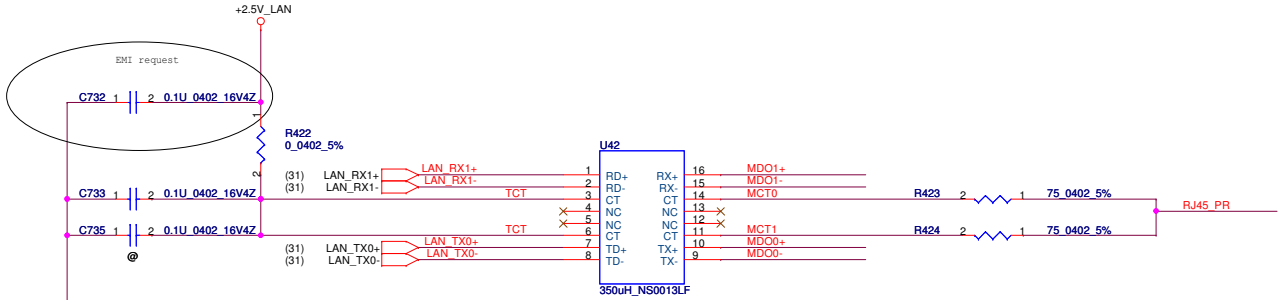
Compal Electronics, Inc.

Title: BCM5906

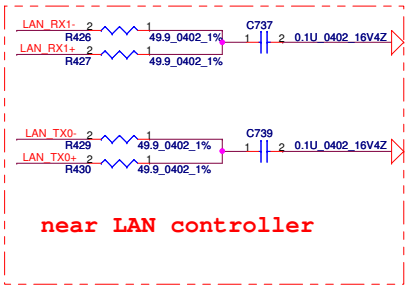
Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 1.0

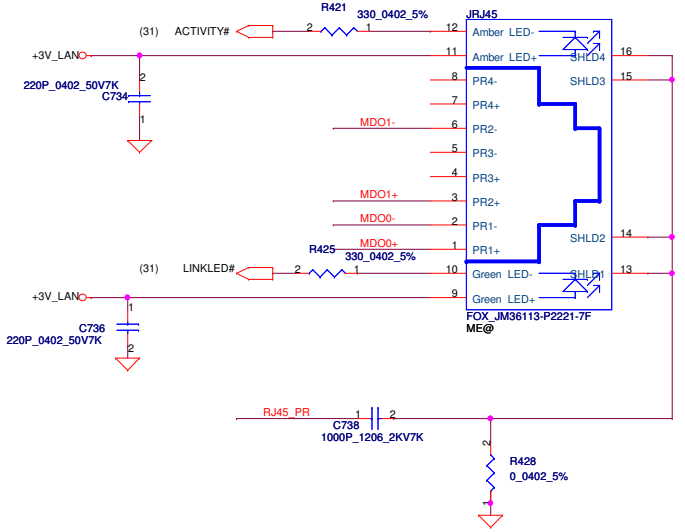
Date: Tuesday, April 28, 2009 | Sheet 31 of 51

RJ45 CONN



Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF





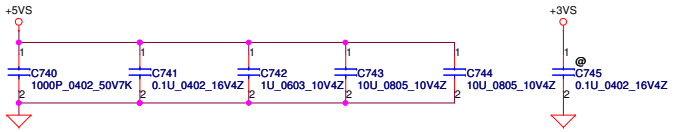
Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.

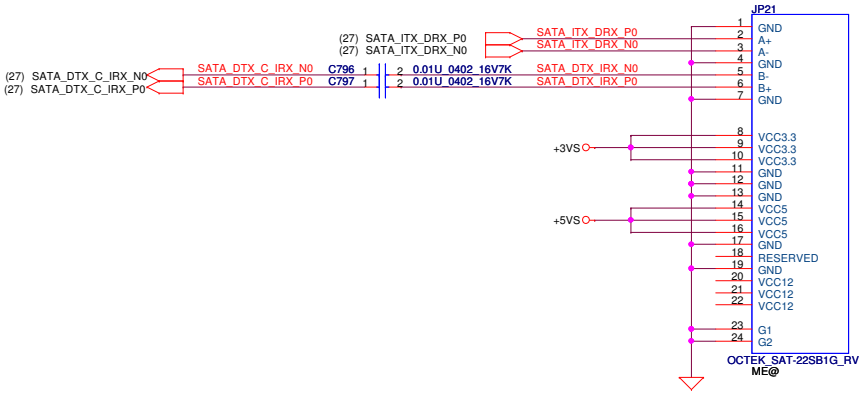
Title: LAN CONTROLLER

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 1.0

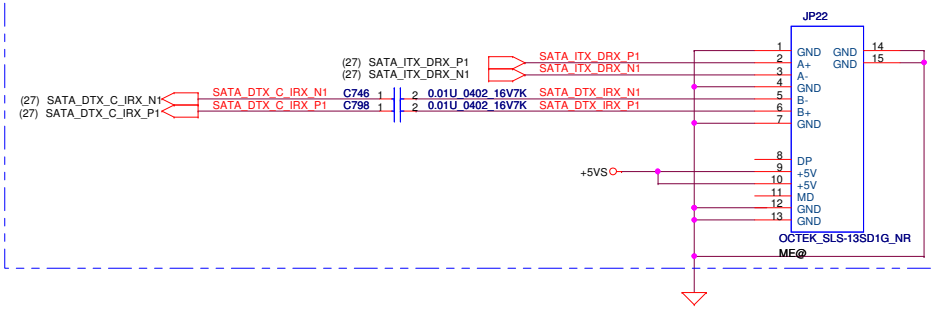
Date: Tuesday, April 28, 2009 | Sheet 32 of 51



SATA HDD Conn.



SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.			
Title: HDD & ODD Connector			
Size: B	Document Number: KIWA5/6 LA-5081P		Rev: 1.0
Date: Tuesday, April 28, 2009	Sheet 33 of 51		

AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

CX20548
AMOM DAA

11/20 update
PC_BEEP dB control

0216_Change value.

DIGITAL **ANALOG**

Place these C and R around AGND and DGND, then choose the one which is close to Codec to populate

CODEC POWER

(3.33V)
250mW

W=40Mil

2.2kohm for MICL + MICR
4.7kohm for MICL or MICR

external MIC
Internal MIC / Array MIC
Internal WOOFER
Internal SPKR.

11/20 update

port A : 5.11K ohm
port B : 10.0K ohm
port C : 20.0K ohm
port D : 39.2K ohm

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

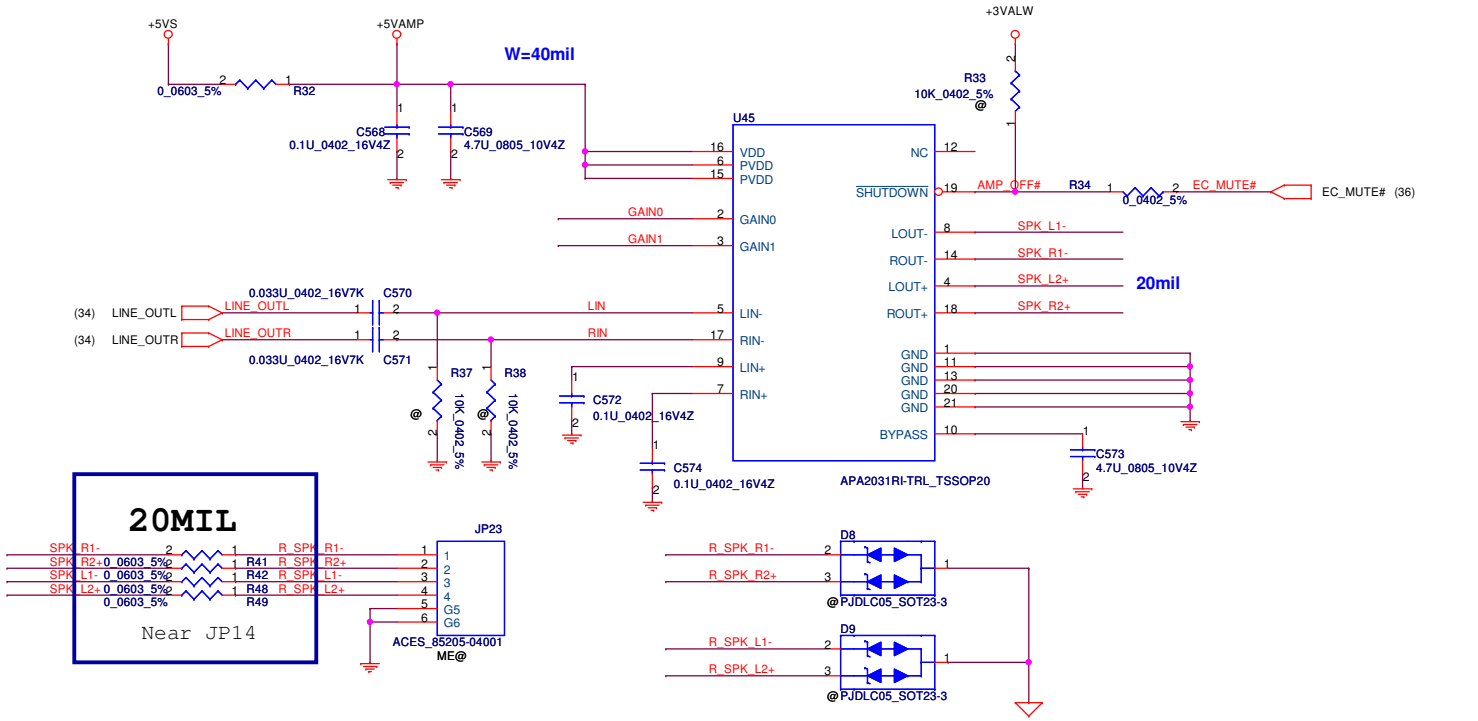
Compal Electronics, Inc.

Title: CX20561-AMOM Codec

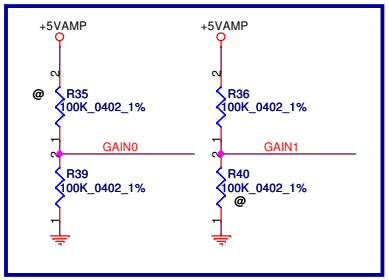
Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	1.0

Date: Tuesday, April 28, 2009 Sheet 34 of 51

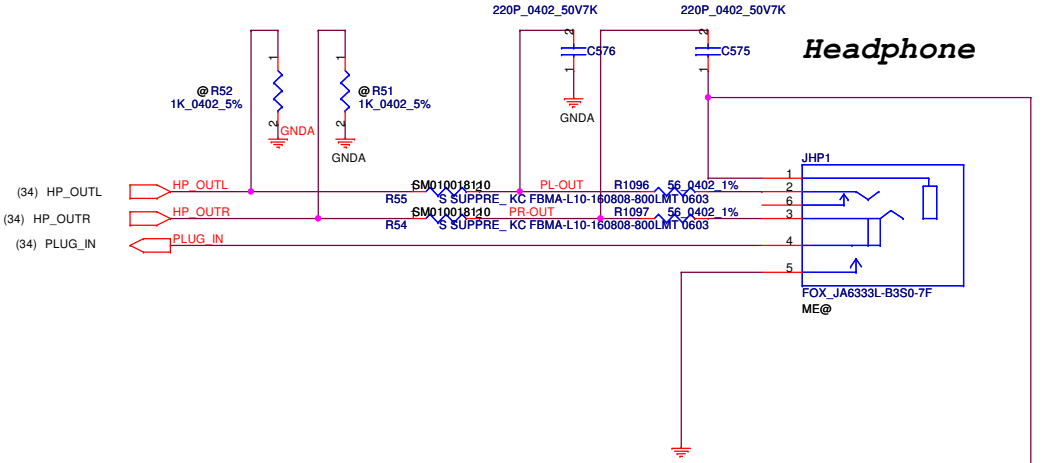
Speaker Connector



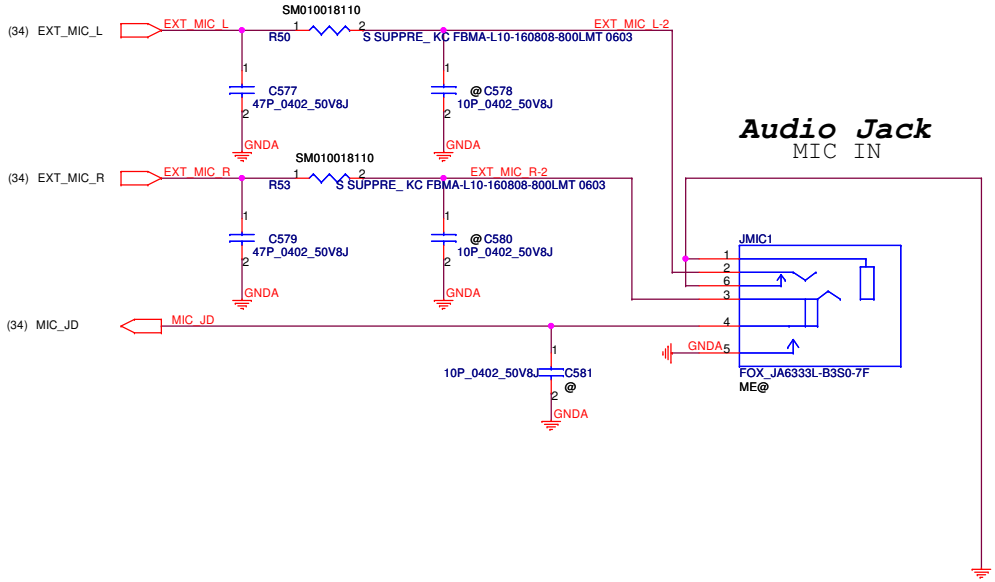
GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



Headphone



Audio Jack



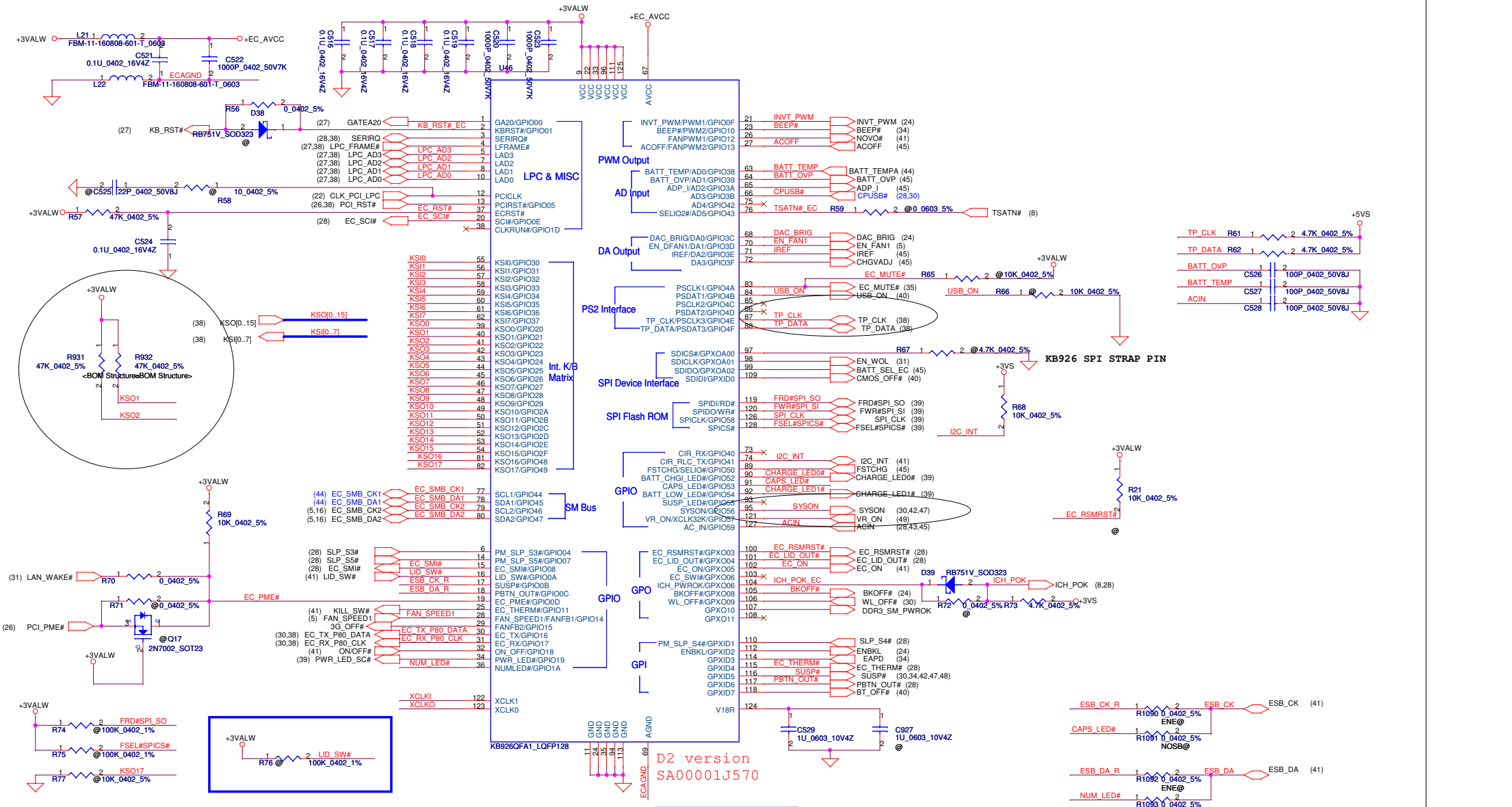
Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.

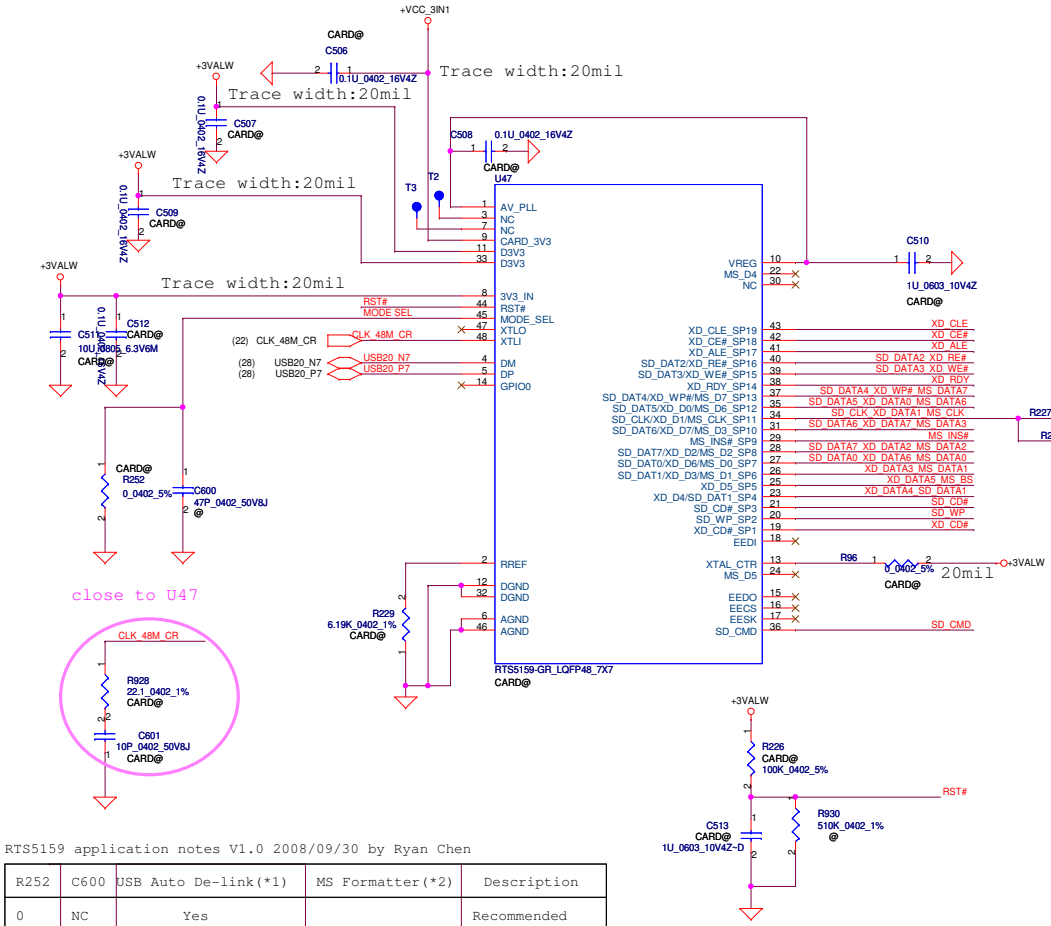
Title: AMP,Audio speaker CONN

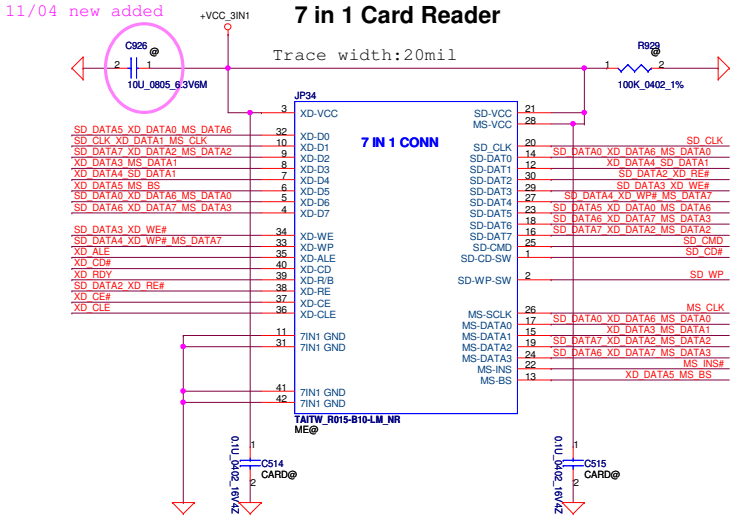
Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 1.0

Date: Tuesday, April 28, 2009 | Sheet 35 of 51


KB926QFA1_LQFP128
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
KB926 SPI STRAP PIN
D2 version
SA00001J570
For SED Team
32.768KHZ_12.5PF_1TJS125BJ4A421P
<BOM Structure>
Compal Electronics, Inc.
BIOS & EC I/O Port
KIWA5/6 LA-5081P
Compal Secret Data
2009/04/23
2010/05
Tuesday, April 28, 2009

Card reader(XD/SD/MMC/MS/MS-Pro HD SD)





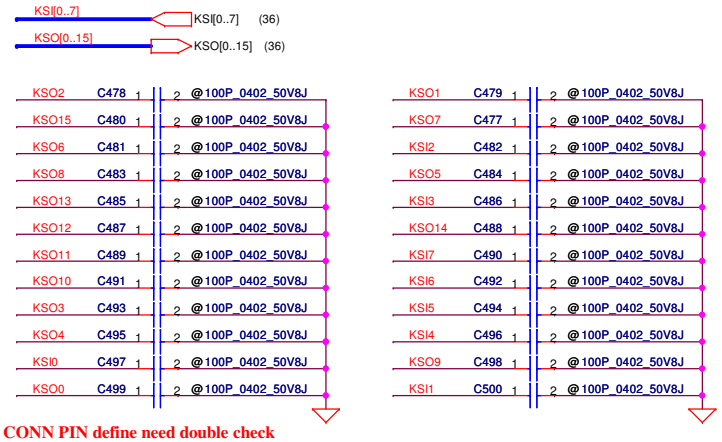
RTS5159 application notes V1.0 2008/09/30 by Ryan Chen

R252	C600	USB Auto De-link(*1)	MS Formatter(*2)	Description
0	NC	Yes		Recommended
NC	47pF	Yes	Yes	
NC	NC			Compatible with RTS5158E
NC	680pF	Yes		LED ON (*3)
10K	180pF			LED ON (*3)
10K	680pF		Yes	

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

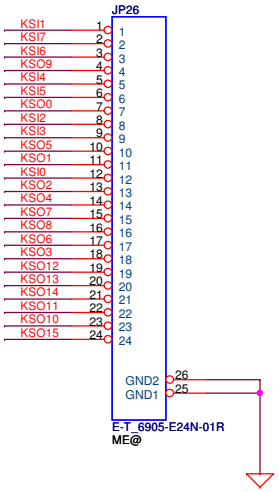
Compal Electronics, Inc.			
Title: USB_CR board			
Size: Custom	Document Number: KIWAX_LA-5081P		Rev: 1.0
Date: Tuesday, April 28, 2009	Sheet 37 of 51		

INT_KBD Conn.

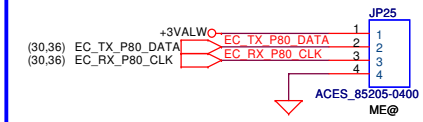


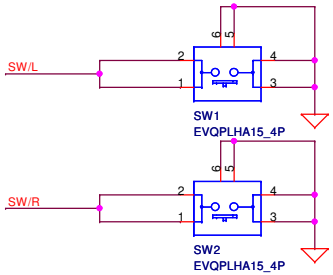
CONN PIN define need double check

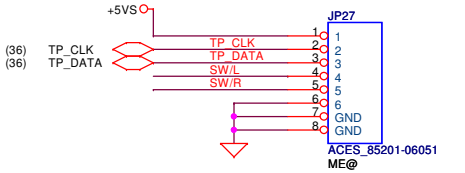
Source:SP01000IE00
2nd source:SP01000IF00
30 pin

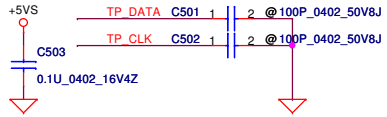


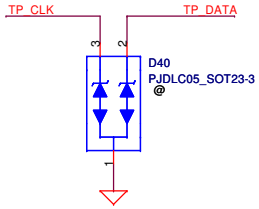
EC DEBUG PORT



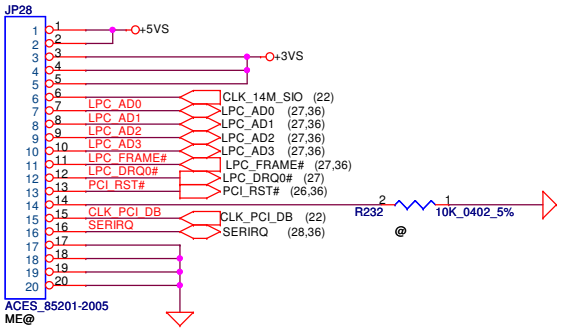








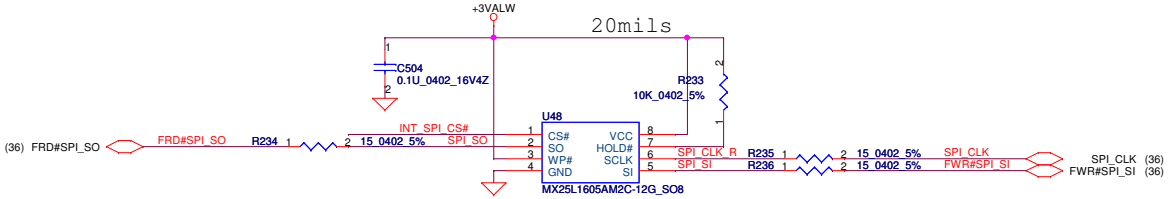
FOR LPC SIO DEBUG PORT

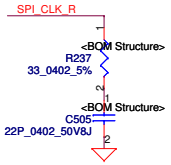


Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: KIWA5/6 LA-5081P		Rev: 1.0
Date: Tuesday, April 28, 2009	Sheet 38 of 51		

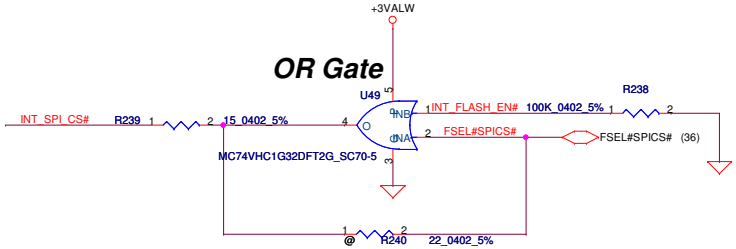
FOR EC 16M SPI ROM

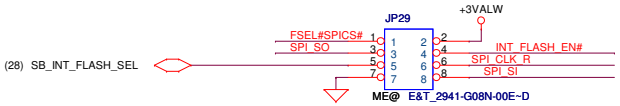




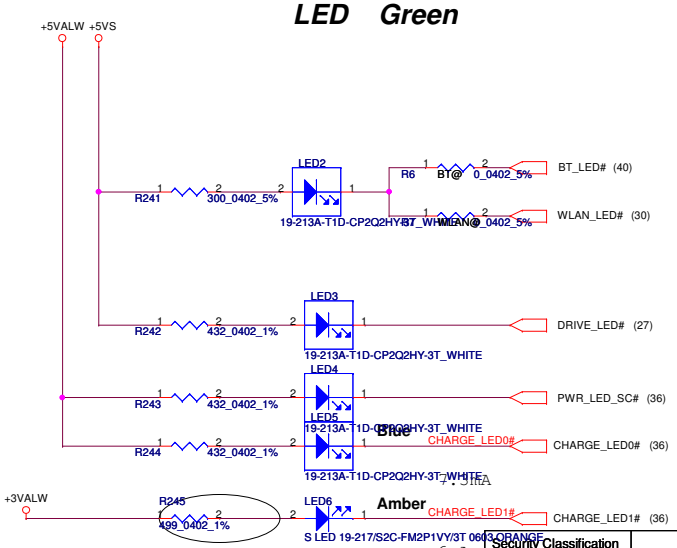
INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

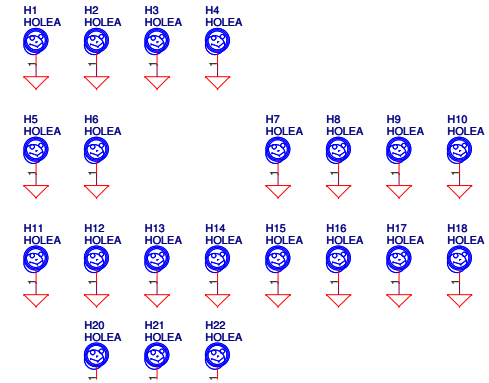
OR Gate





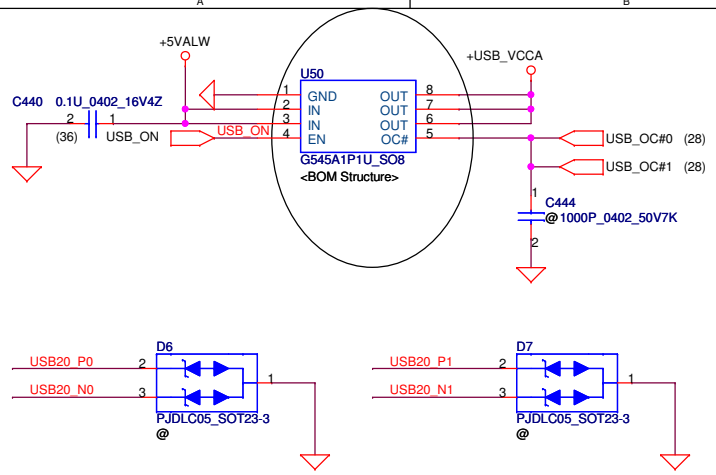
LED Green

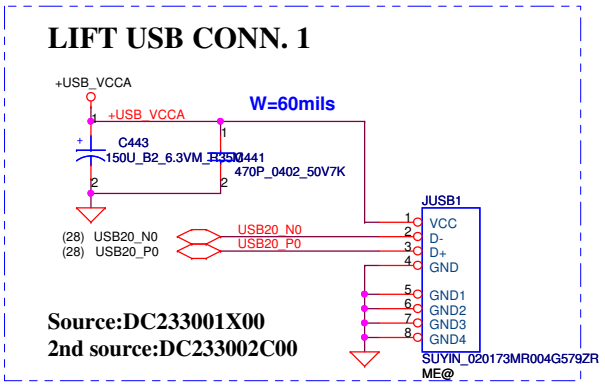


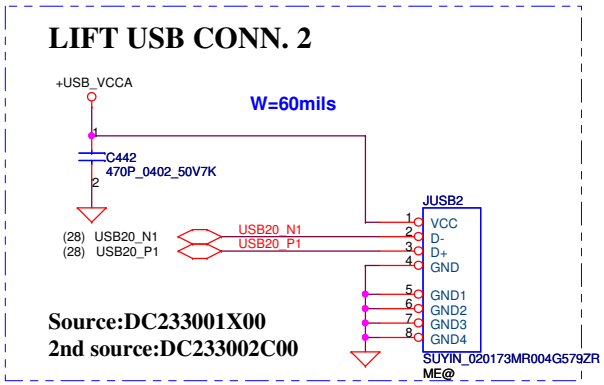


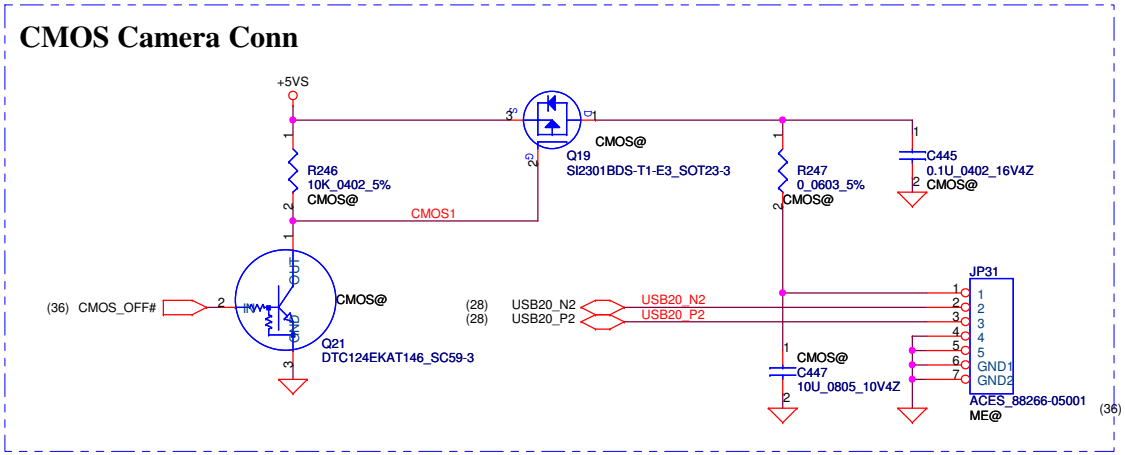
Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

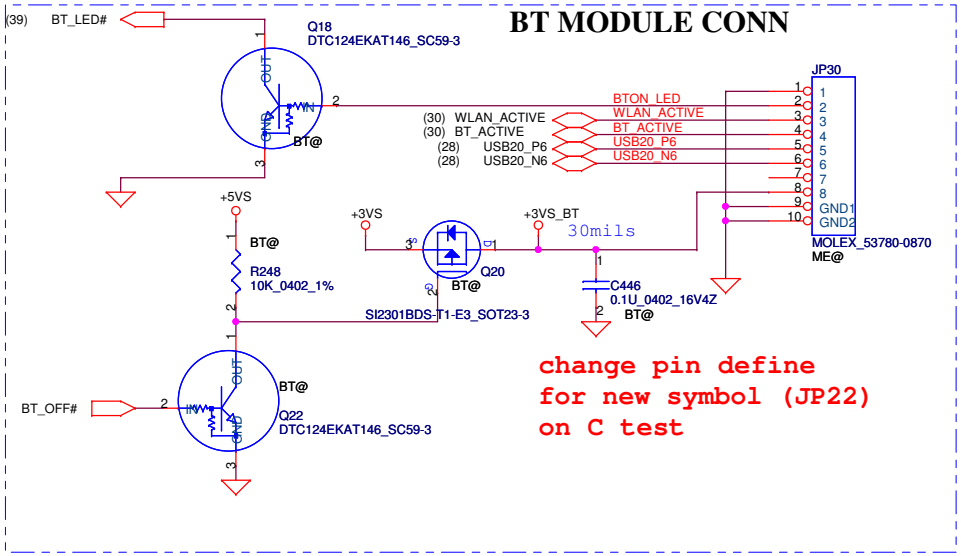
Compal Electronics, Inc.			
Title	LED/EC SPI ROM		
Size B	Document Number KIWA5/6 LA-5081P		Rev 1.0
Date: Tuesday, April 28, 2009	Sheet 39 of 51		

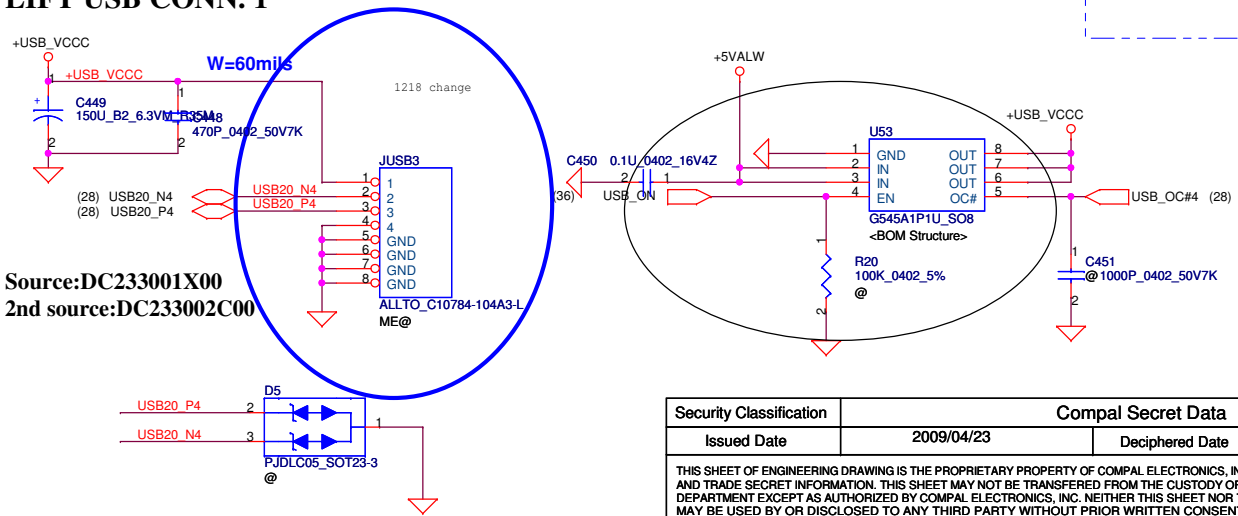












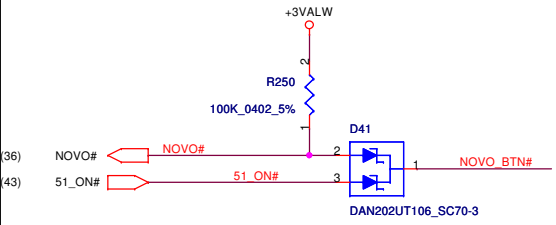
Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

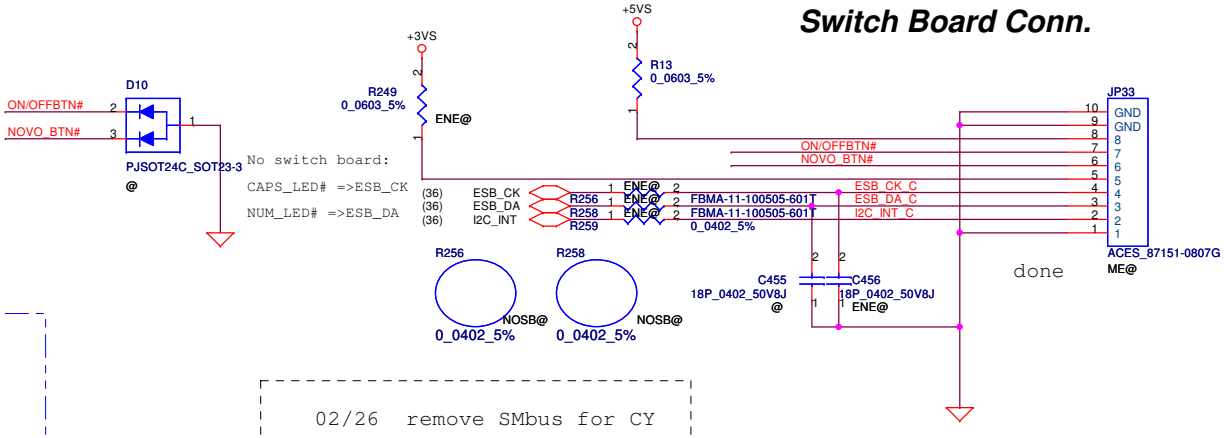
Compal Electronics, Inc.

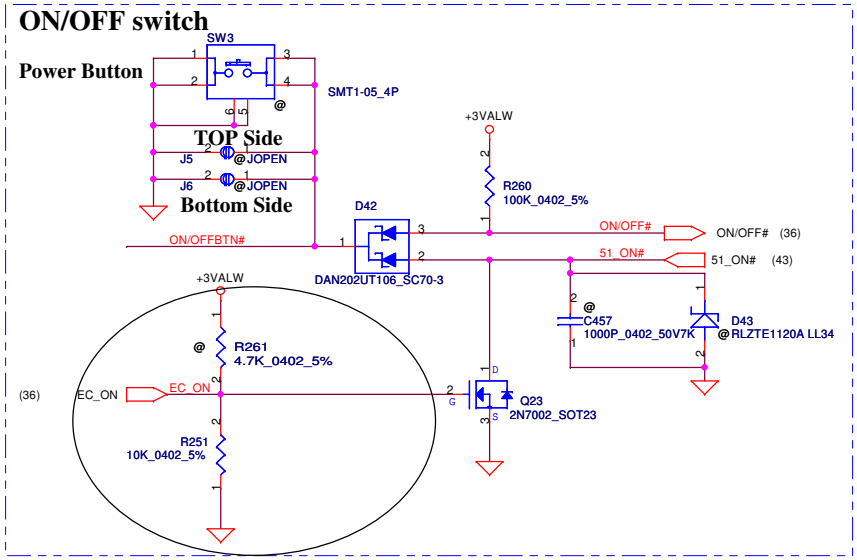
Title: Power OK, Reset and RTC Circuit, TP

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	1.0

Date: Tuesday, April 28, 2009 | Sheet 40 of 51

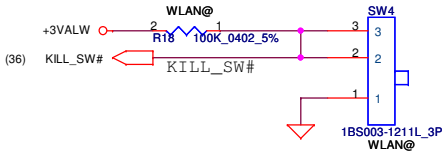


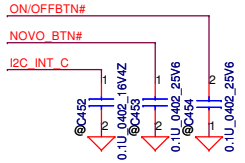




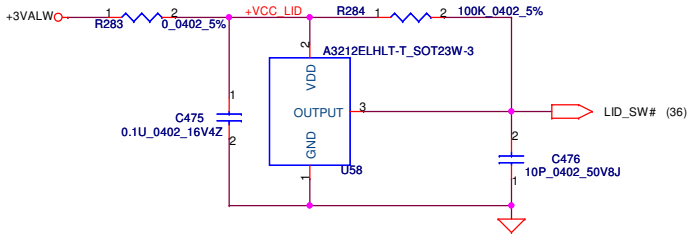
02/26 remove SMbus for CY

Kill Switch





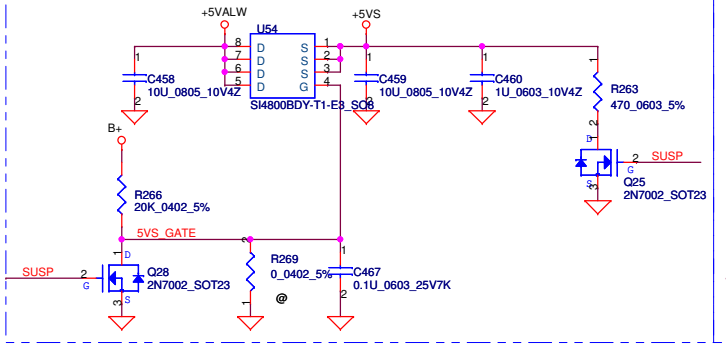
Lid Switch



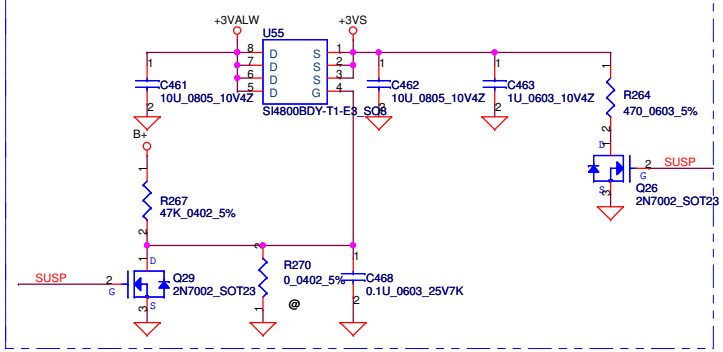
Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

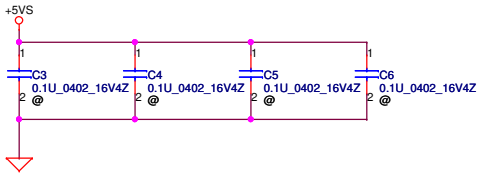
Compal Electronics, Inc.			
Title: Audio Jack & SW connector			
Size: Custom	Document Number: KIWA5/6 LA-5081P		Rev: 1.0
Date: Tuesday, April 28, 2009	Sheet 41 of 51		

+5VALW TO +5VS

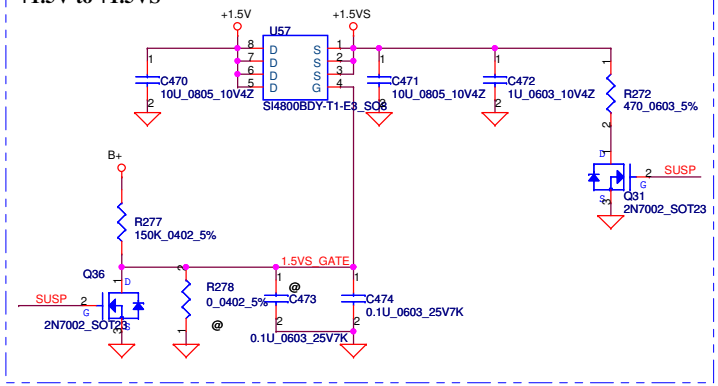


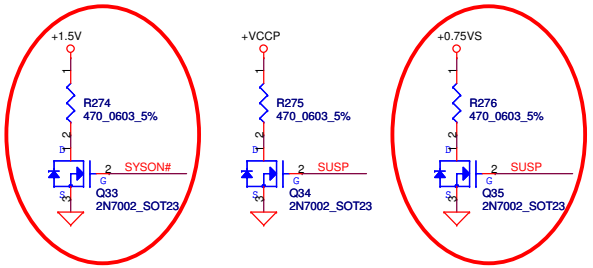
+3VALW TO +3VS

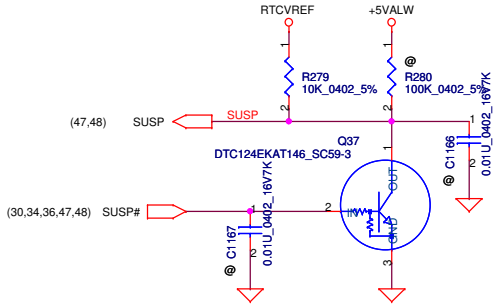


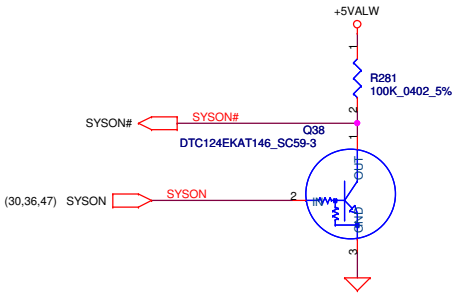


+1.5V to +1.5VS









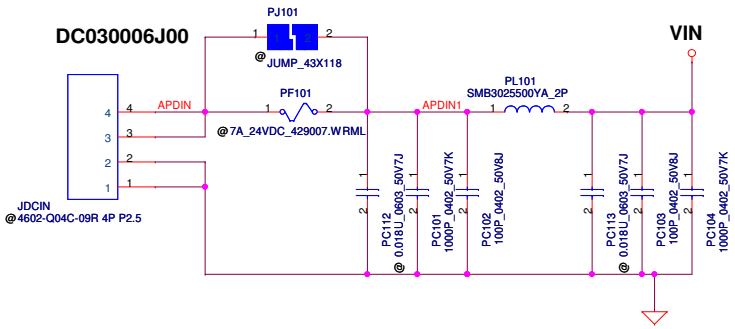
Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.

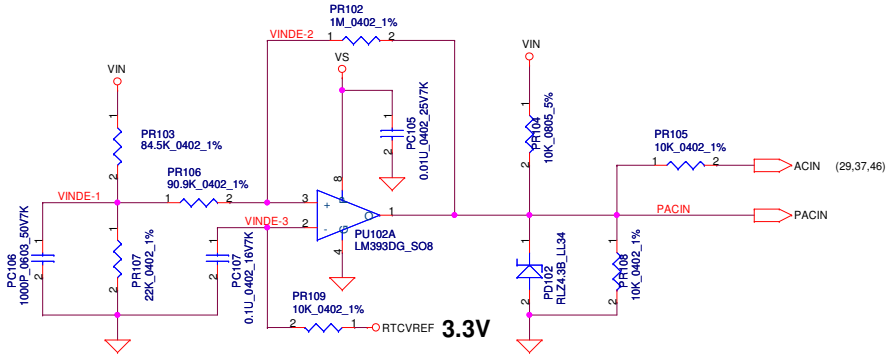
Title: DC Interface

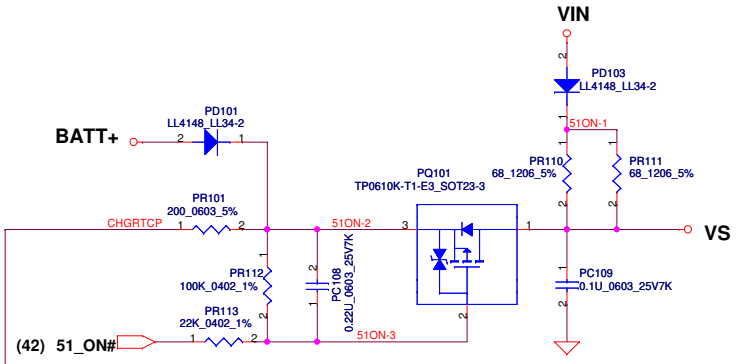
Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	1.0

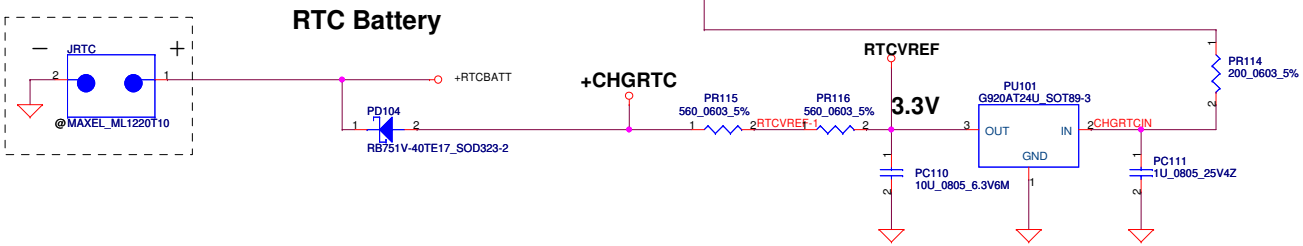
Date: Tuesday, April 28, 2009 Sheet 42 of 51



Vin Detector			
High	17.944	17.706	17.470
Low	16.242	16.027	15.808







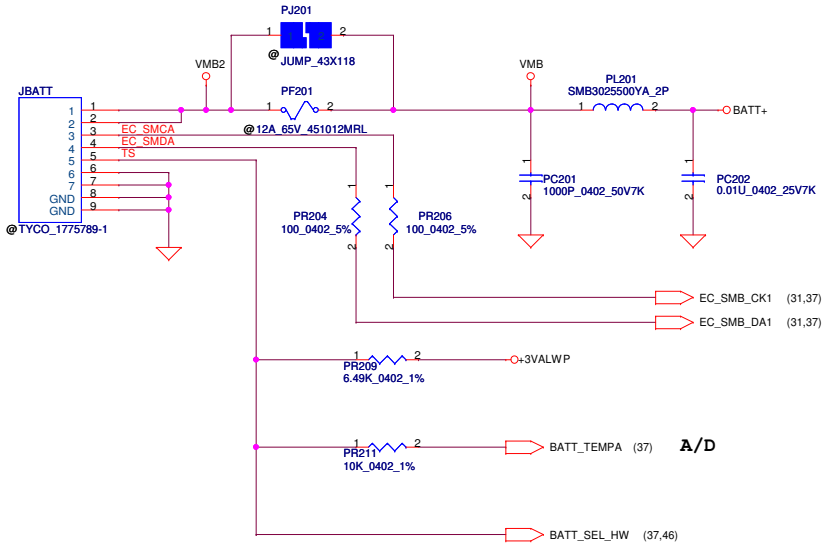
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom		0.1

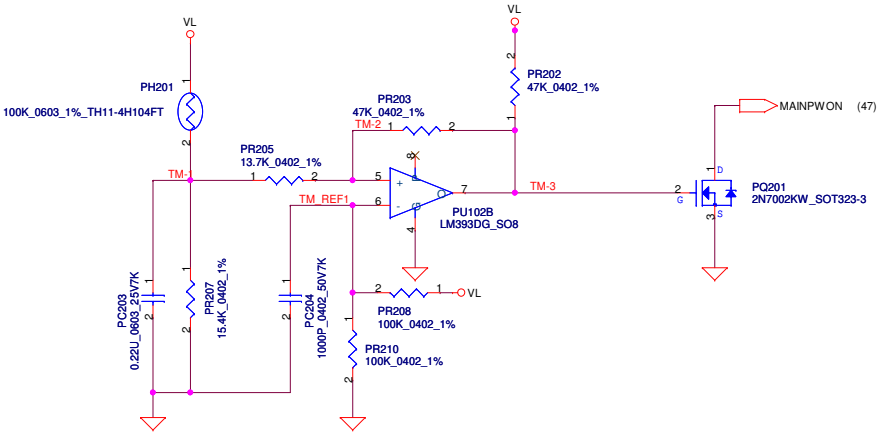
Date: Tuesday, April 28, 2009 | Sheet 44 of 53



PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 56 degree C



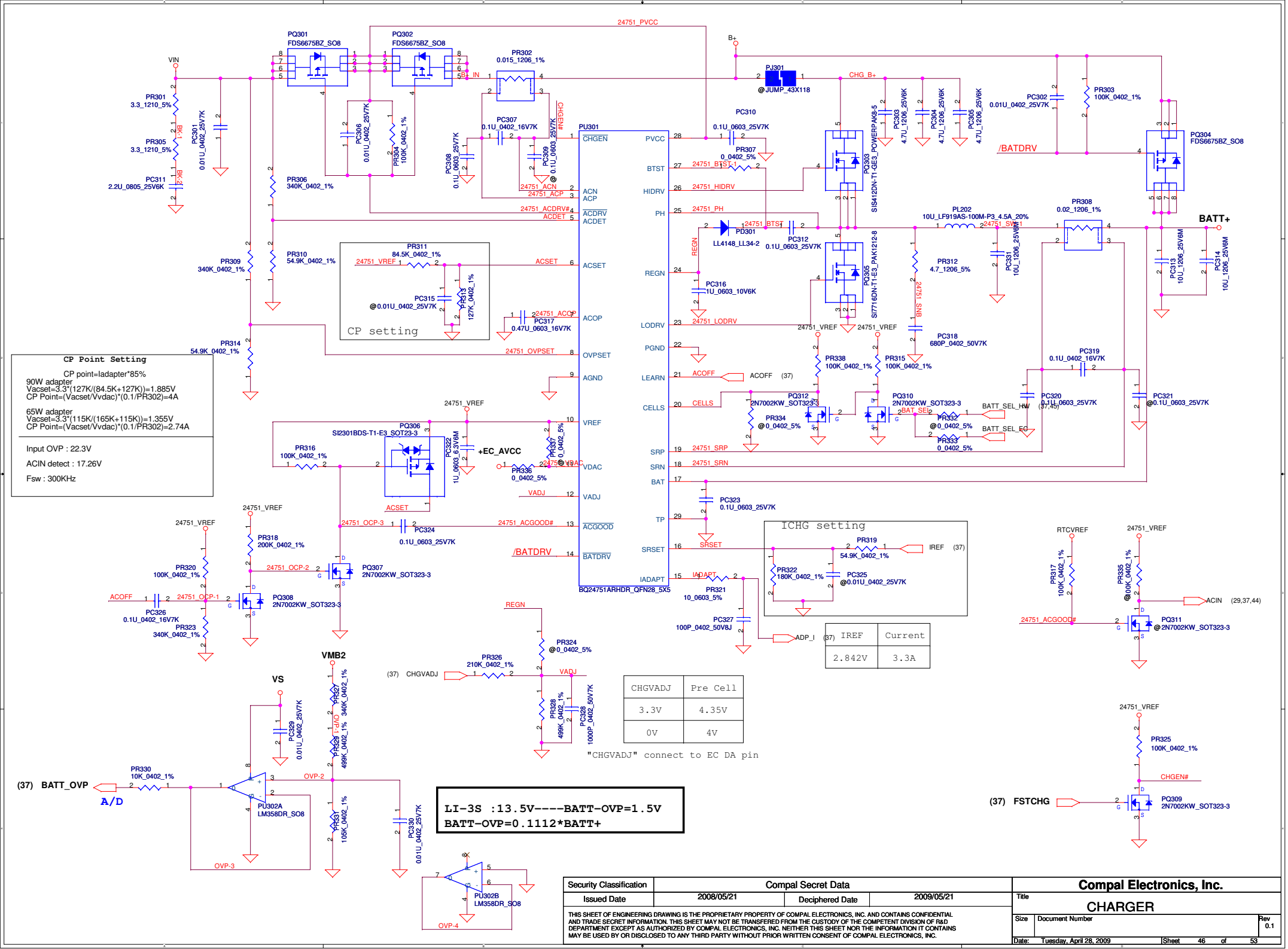
Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.1

Date: Tuesday, April 28, 2009 | Sheet 45 of 53



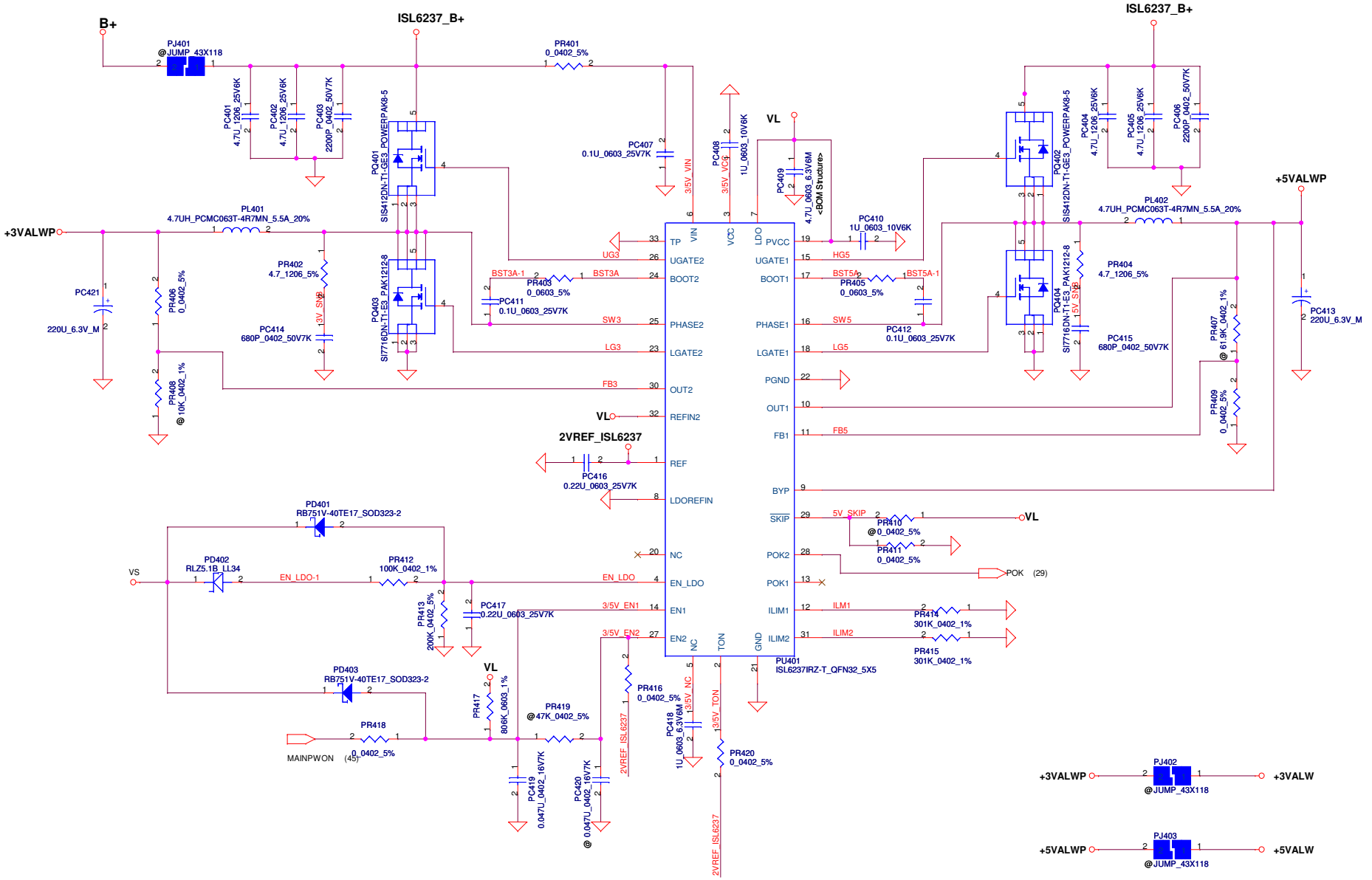
Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
		0.1

Date: Tuesday, April 28, 2009 | Sheet 46 of 53



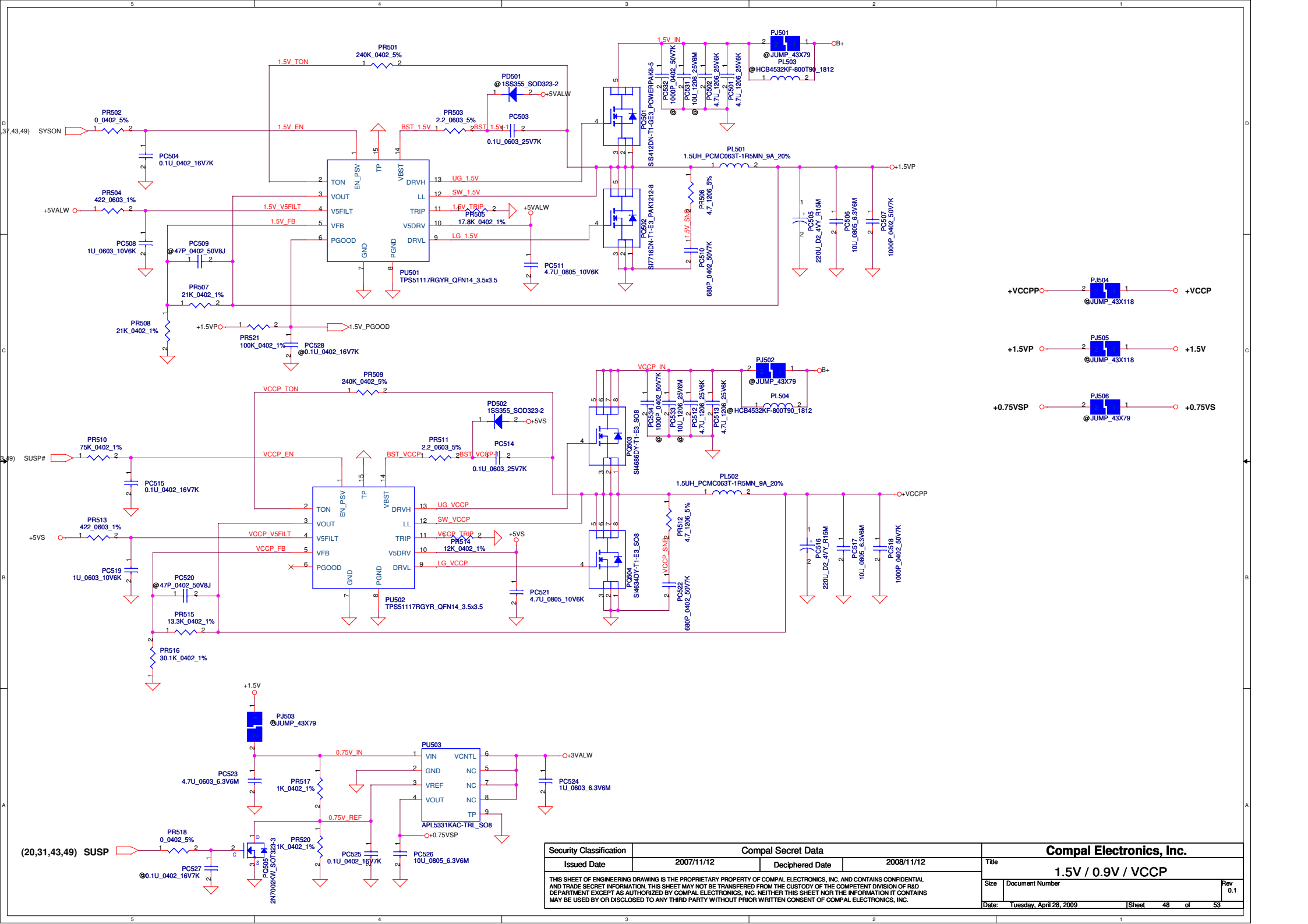
Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom		0.1

Date: Tuesday, April 28, 2009 | Sheet 47 of 53



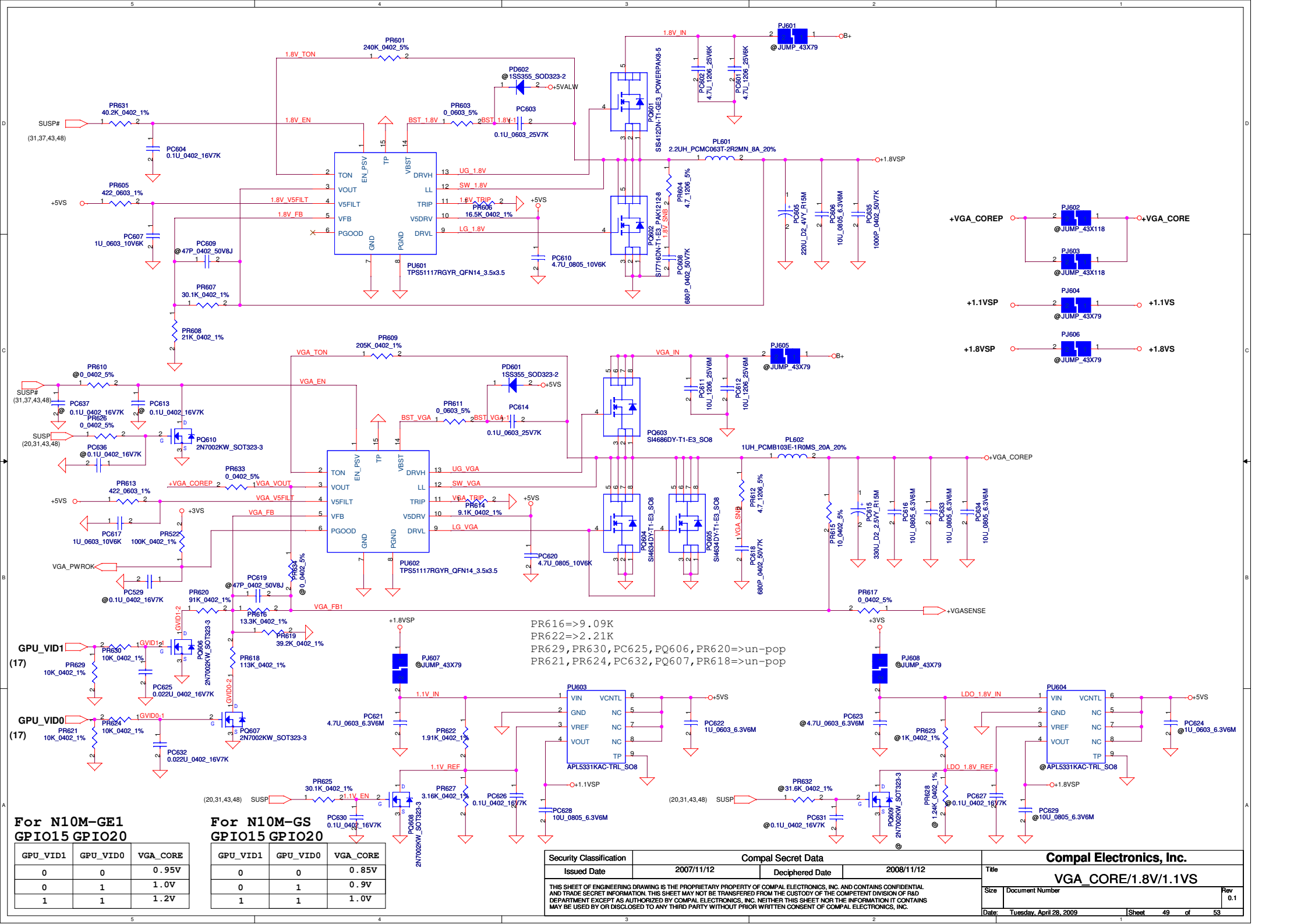
Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: 1.5V / 0.9V / VCCP

Size	Document Number	Rev
		0.1

Date: Tuesday, April 28, 2009 | Sheet 48 of 53



For N10M-GE1
GPIO15 GPIO20

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.95V
0	1	1.0V
1	1	1.2V

For N10M-GS
GPIO15 GPIO20

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.85V
0	1	0.9V
1	1	1.0V

Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: VGA_CORE/1.8V/1.1VS

Size	Document Number	Rev
		0.1

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CPU VPL-1

CPU_TONSEL

CPU_VR_ON

CPU_DPRSLPVR

Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		modify battery select circuit			add PQ312 and PR338	2009.01.14	
2		change +1.1VS voltage to +1.05V			change P622 to 2.21K only for N10M-GS(40nm)	2009.01.14	
3							
4							
5							
6							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							

Compal Electronics, Inc.

Title: PIR (PWR)

Size	Document Number	Rev
Custom	KIWAX_LA-5081P	0.1

Date: Tuesday, April 28, 2009 | Sheet 51 of 53

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/10	39	Remove D11, and add R6, R7	
	12/10	36	change PWR_LED_SC# from U46.38 to U46.34	
2	1/15	39	modify H18 hold size, and change the H5、H6 and H18 hold type.	
		42	add 4 CAPs C3, C4, C5 and C6 for EMI.	
		35	change C572 and C574 footprint from 0603 to 0402.	
		34	add R25 for BEEP# test	
3	3/16	06	add R1089, C1162 and H_DPRSTP#_R	
			add C1163, C1164,and C1165 for EMC request.	
		08	change H_DPRSTP# to H_DPRSTP#_R	
		19	P19 add Bom structure 40nm@ GPU and 55nm@ GPU	
			R999 change to 24.9K	
		23	add R1095 pull high	
		35	swap HP_OUTL and HP_OUTR	
		36	add R1090, R1091, R1092, R1093	
			CAPS_LED#, NUJM_LED#, ESB_CK_R, and ESB_DA_R	
		41	add R256, R258 Bom configuration	
			Remove CY SMBus	
		42	add C1166, C1167 for EMC request.	
4	4/20	27	R829 changed to 0ohm.	
		08	R80 changed to 33ohm	
		34	R1044 changed to 33ohm	
			R1056 changed to 33ohm	
			C1089 changed to 10P	

Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2010/05

Compal Electronics, Inc.

Title: **HW PIR**

Size	Document Number	Rev
B	KIWAX_LA-5081P	1.0

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