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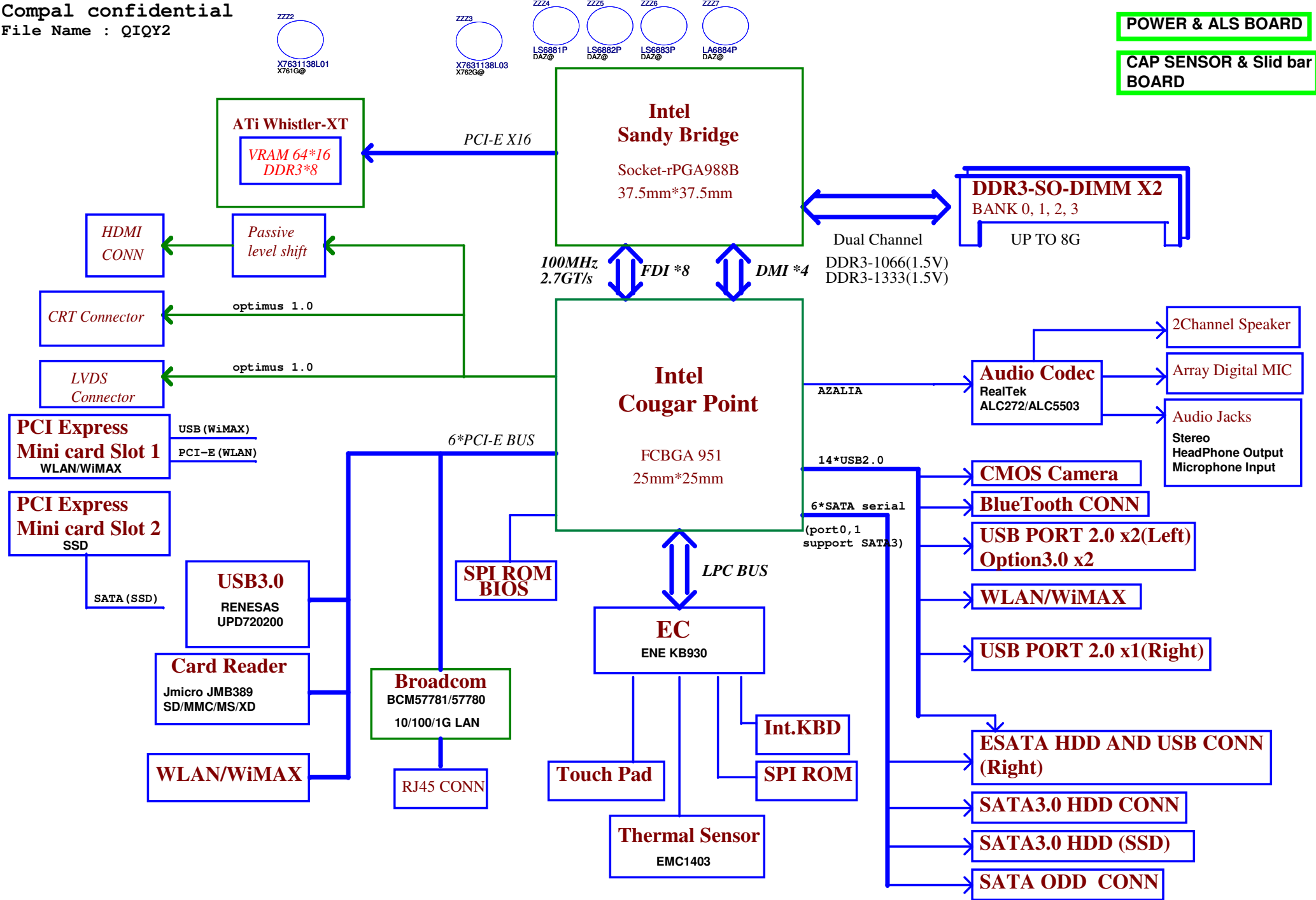
QIQY2 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATi Whistler XT+DDR3

2011-05-11

REV: 1.0

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Voltage Rails

power plane	State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0		○	○	○	○
S3		○	○	○	✗
S5 S4/AC		○	○	✗	✗
S5 S4/ Battery only		○	✗	✗	✗
S5 S4/AC & Battery don't exist		✗	✗	✗	✗

SMBUS Control Table

	SOURCE	VGA	BATT	KB930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	✗	✓ +3VALW	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	✗	✗	✗	✗	✗	✗	✓ +3VS
SMBCLK SMBDATA	PCH +3VALW	✗	✗	✗	✓ +3VS	✓ +3VS	✗	✗
SML0CLK SML0DATA	PCH +3VALW	✗	✗	✗	✗	✗	✗	✗
SML1CLK SML1DATA	PCH +3VALW	✓ +3VS	✗	✓ +3VS	✗	✗	✓ +3VS	✗

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403-2	1001_101xb

EC SM Bus2 address

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BOM Structure Table

BTO Item	BOM Structure
UMA	
UMA Only	UMA_ONLY@
Optimus	OPTI@
VRAM	X76@
HDMI	HDMI@
Blue Tooth	BT@
USB3.0	USB30@
ESATA	ESATA@
USB Charger	USB_CHG@
No USB Charger	NO_CHG@
Unpop	@
Codec ALC272	272@
Codec ALC5503	5503@
LAN 57781	57781@
LAN 57780	57780@
Ventura Feature	
Camera	CMOS@

VRAM BOM Config

X761G@: X7625738L01	Samsung 1GB
Sub: X7625738L02	Hynix 1GB
X762G@: X7625738L03	Samsung 2GB
Sub: X7625738L04	Hynix 2GB

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/Cable (Right Side)
		1	USB Port (Right Side COMBO)
	UHCI1	2	USB/B (Left Side)
		3	USB/B (Left Side)
	UHCI2	4	
		5	Camera
EHCI2	UHCI3	6	
		7	
	UHCI4	8	
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
	UHCI6	12	
		13	Blue Tooth

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Power-Up/Down Sequence

1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5. VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)

VDDR3(3.3VGS)

PCIE_VDDC(1.0V)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset

Note: Do not drive any IOs before VDDR3 is ramped up.

T4+16clock

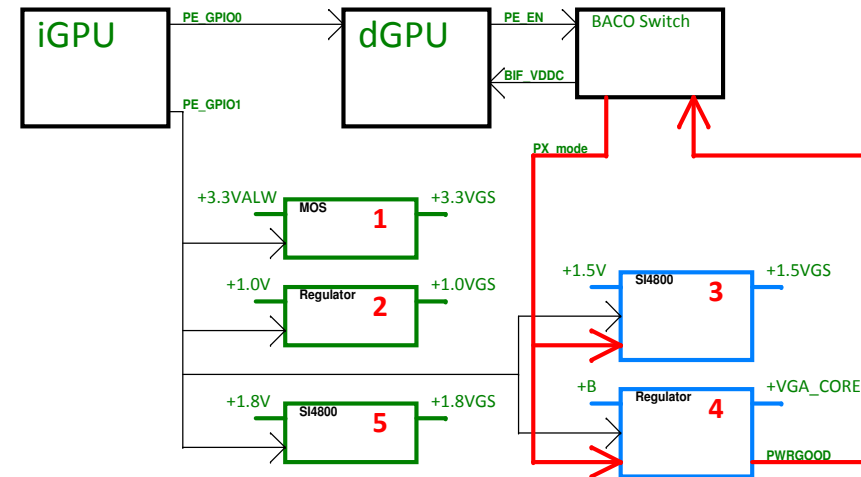
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High -> Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

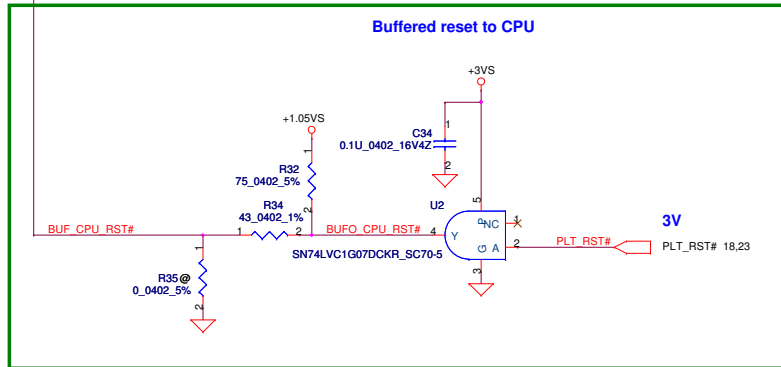
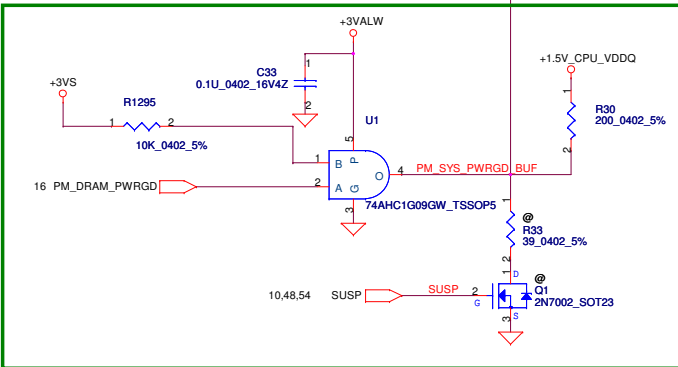
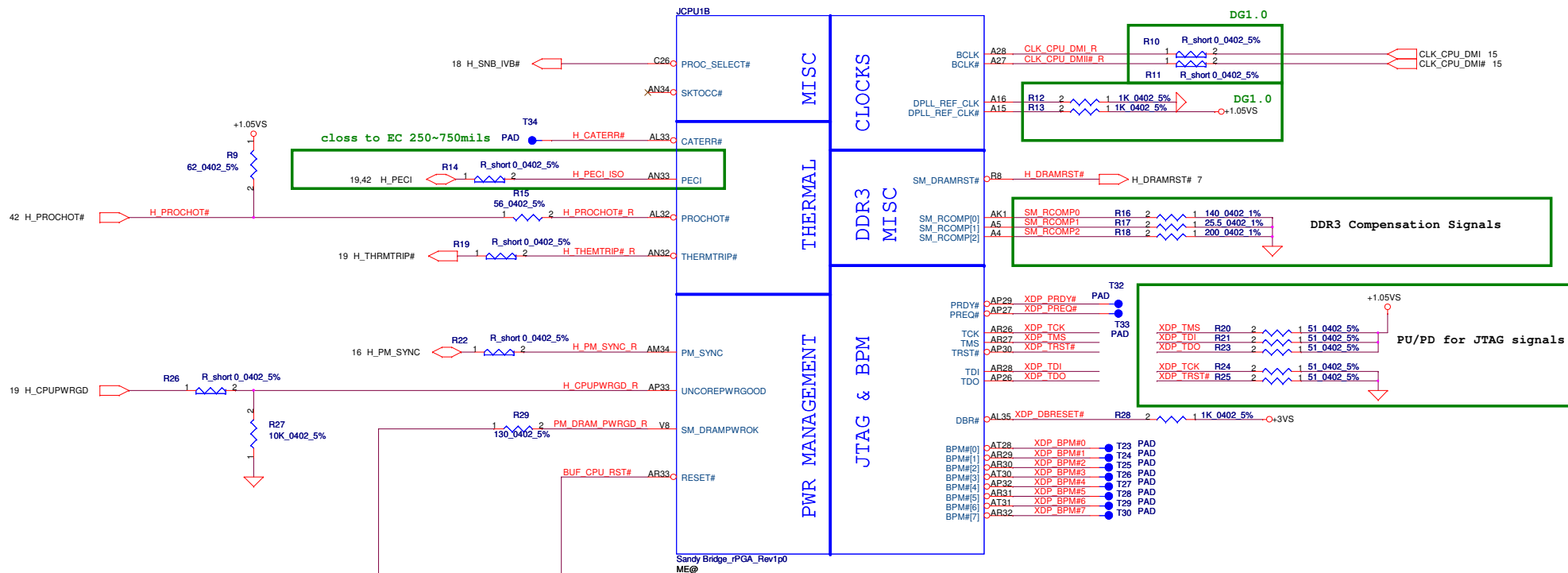
BACO option :

PE_GPIO0 : High -> Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

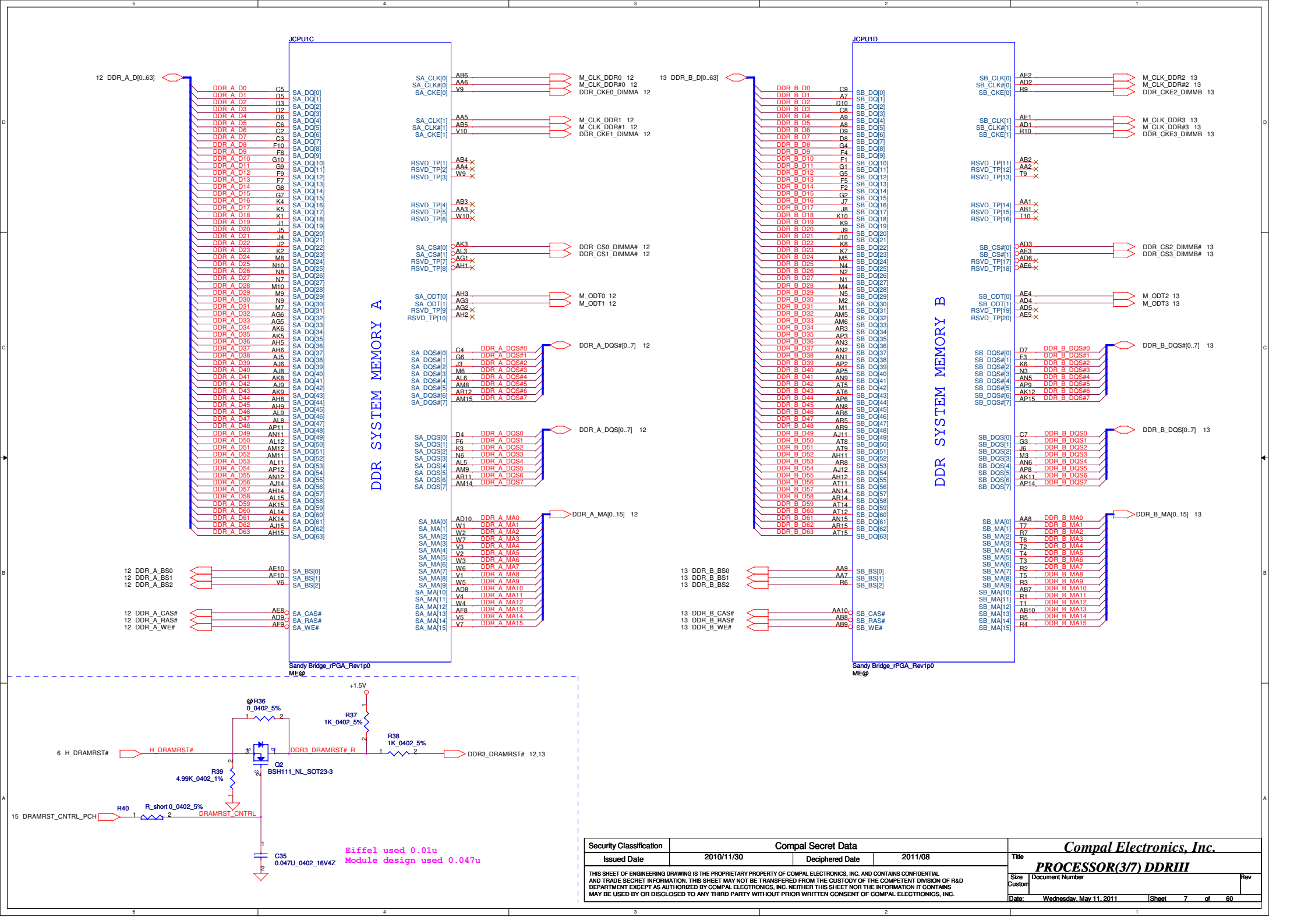
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



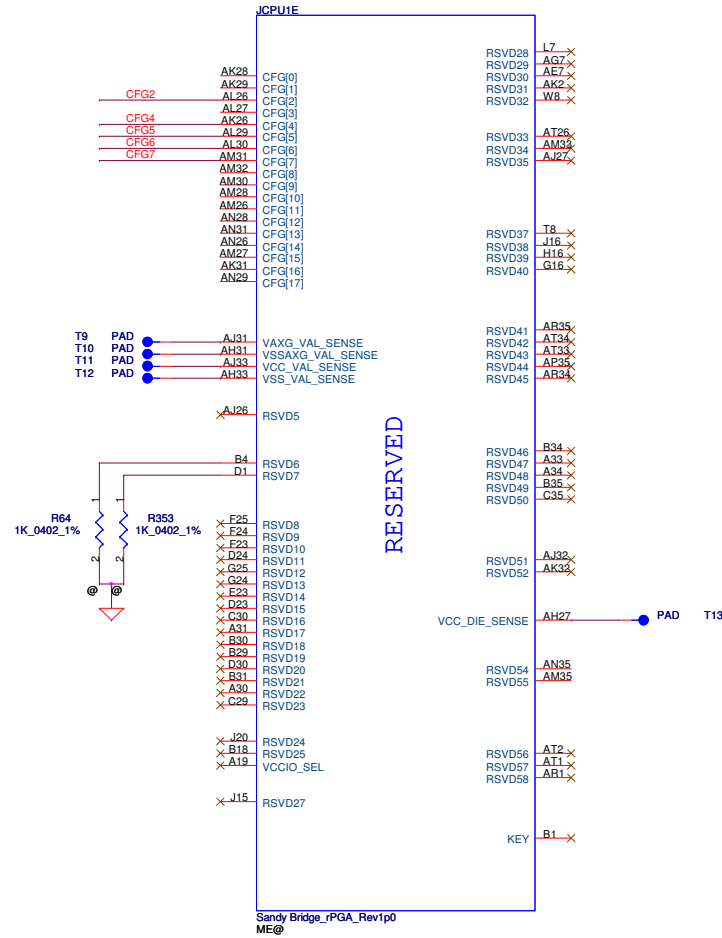
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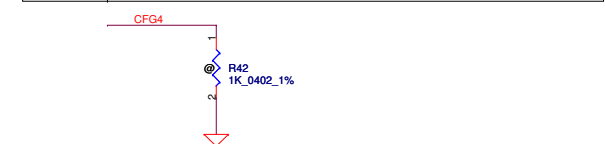
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Title				PROCESSOR(2/7) PM,XDP,CLK				Rev			
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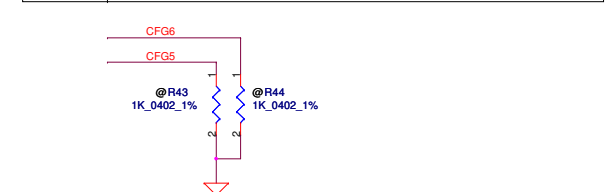
CFG Straps for Processor



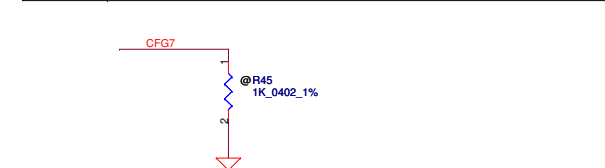
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



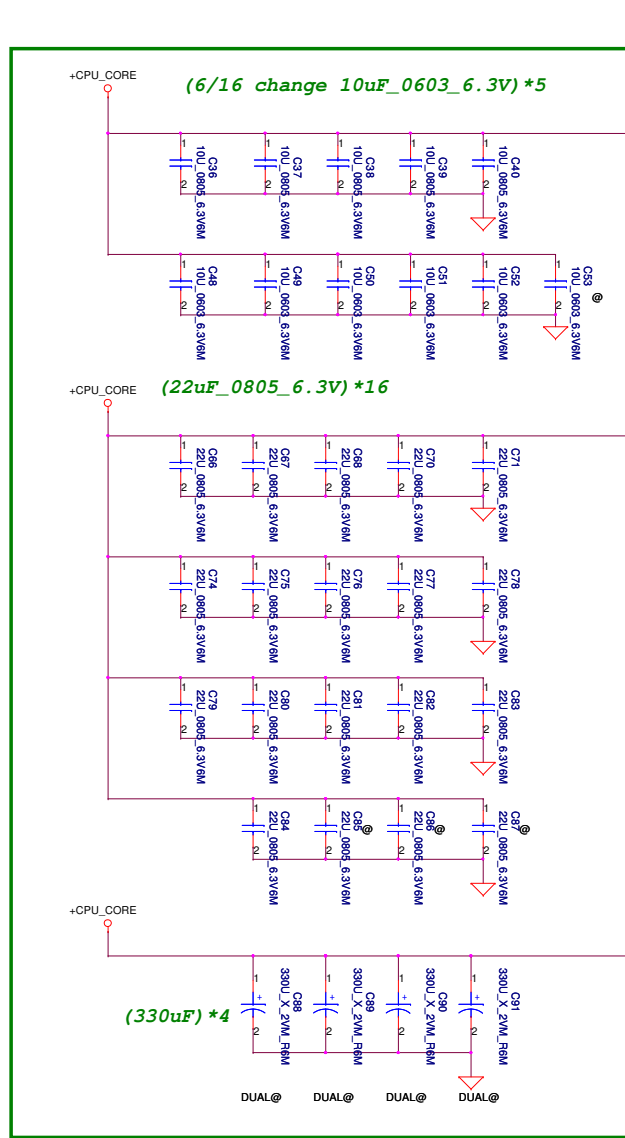
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



QC=94A
DC=53A

JCPU1F

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
Y25	VCC61
Y24	VCC62
Y23	VCC63
Y22	VCC64
Y21	VCC65
Y20	VCC66
Y19	VCC67
Y18	VCC68
Y17	VCC69
Y16	VCC70
Y15	VCC71
Y14	VCC72
Y13	VCC73
Y12	VCC74
Y11	VCC75
Y10	VCC76
Y09	VCC77
Y08	VCC78
Y07	VCC79
Y06	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

POWER

PEG AND DDR

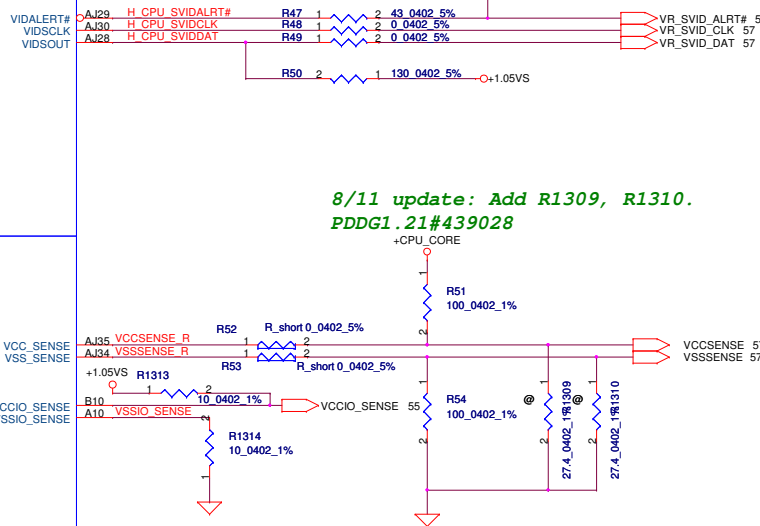
CORE SUPPLY

SVID

SENSE LINES

VIDALERT#
VIDSCLK
VIDSOUT

VCC_SENSE
VSS_SENSE
VCCIO_SENSE
VSSIO_SENSE



Sandy Bridge_rPGA Rev1.0
ME@

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PROCESSOR(5/7) PWR,BYPASS			
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JCPU1H

AT35	VSS1	VSS81	AJ22
AT32	VSS2	VSS82	AJ19
AT29	VSS3	VSS83	AJ16
AT27	VSS4	VSS84	AJ13
AT25	VSS5	VSS85	AJ10
AT22	VSS6	VSS86	AJ7
AT19	VSS7	VSS87	AJ4
AT16	VSS8	VSS88	AJ3
AT13	VSS9	VSS89	AJ2
AT10	VSS10	VSS90	AJ1
AT7	VSS11	VSS91	AH35
AT4	VSS12	VSS92	AH34
AT3	VSS13	VSS93	AH32
AR25	VSS14	VSS94	AH30
AR22	VSS15	VSS95	AH29
AR19	VSS16	VSS96	AH28
AR16	VSS17	VSS97	AH26
AR13	VSS18	VSS98	AH25
AR10	VSS19	VSS99	AH22
AR7	VSS20	VSS100	AH19
AR4	VSS21	VSS101	AH16
AR2	VSS22	VSS102	AH7
AP34	VSS23	VSS103	AH4
AP31	VSS24	VSS104	AG9
AP28	VSS25	VSS105	AG8
AP25	VSS26	VSS106	AG4
AP22	VSS27	VSS107	AF6
AP19	VSS28	VSS108	AF5
AP16	VSS29	VSS109	AF3
AP13	VSS30	VSS110	AF2
AP10	VSS31	VSS111	AE35
AP7	VSS32	VSS112	AE34
AP4	VSS33	VSS113	AE33
AP1	VSS34	VSS114	AE32
AN30	VSS35	VSS115	AE31
AN27	VSS36	VSS116	AE30
AN25	VSS37	VSS117	AE29
AN22	VSS38	VSS118	AE28
AN19	VSS39	VSS119	AE27
AN16	VSS40	VSS120	AE26
AN13	VSS41	VSS121	AE9
AN10	VSS42	VSS122	AD7
AN7	VSS43	VSS123	AC9
AN4	VSS44	VSS124	AC8
AM29	VSS45	VSS125	AC6
AM25	VSS46	VSS126	AC5
AM22	VSS47	VSS127	AC3
AM19	VSS48	VSS128	AC2
AM16	VSS49	VSS129	AB35
AM13	VSS50	VSS130	AB34
AM10	VSS51	VSS131	AB33
AM7	VSS52	VSS132	AB32
AM4	VSS53	VSS133	AB31
AM3	VSS54	VSS134	AB30
AM2	VSS55	VSS135	AB29
AM1	VSS56	VSS136	AB28
AL34	VSS57	VSS137	AB27
AL31	VSS58	VSS138	AB26
AL28	VSS59	VSS139	Y9
AL25	VSS60	VSS140	Y8
AL22	VSS61	VSS141	Y6
AL19	VSS62	VSS142	Y5
AL16	VSS63	VSS143	Y3
AL13	VSS64	VSS144	Y2
AL10	VSS65	VSS145	W35
AL7	VSS66	VSS146	W34
AL4	VSS67	VSS147	W33
AL2	VSS68	VSS148	W32
AK33	VSS69	VSS149	W31
AK30	VSS70	VSS150	W30
AK27	VSS71	VSS151	W29
AK25	VSS72	VSS152	W28
AK22	VSS73	VSS153	W27
AK19	VSS74	VSS154	W26
AK16	VSS75	VSS155	U9
AK13	VSS76	VSS156	U8
AK10	VSS77	VSS157	U6
AK7	VSS78	VSS158	U5
AK4	VSS79	VSS159	U3
AJ25	VSS80	VSS160	U2

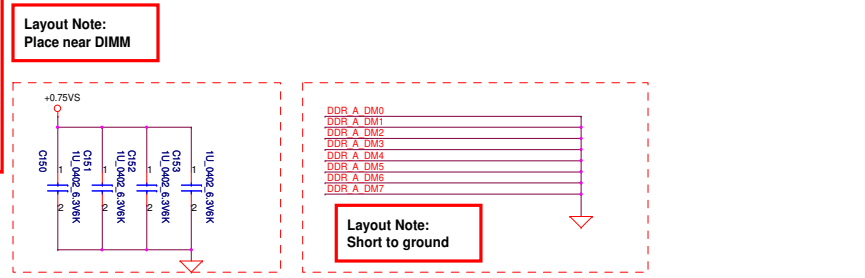
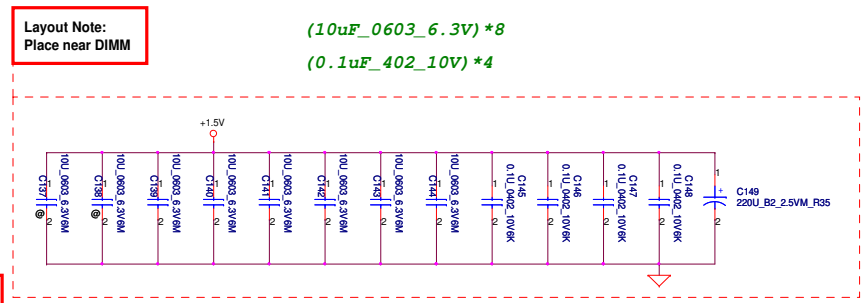
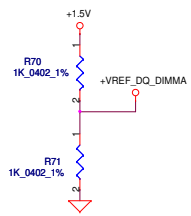
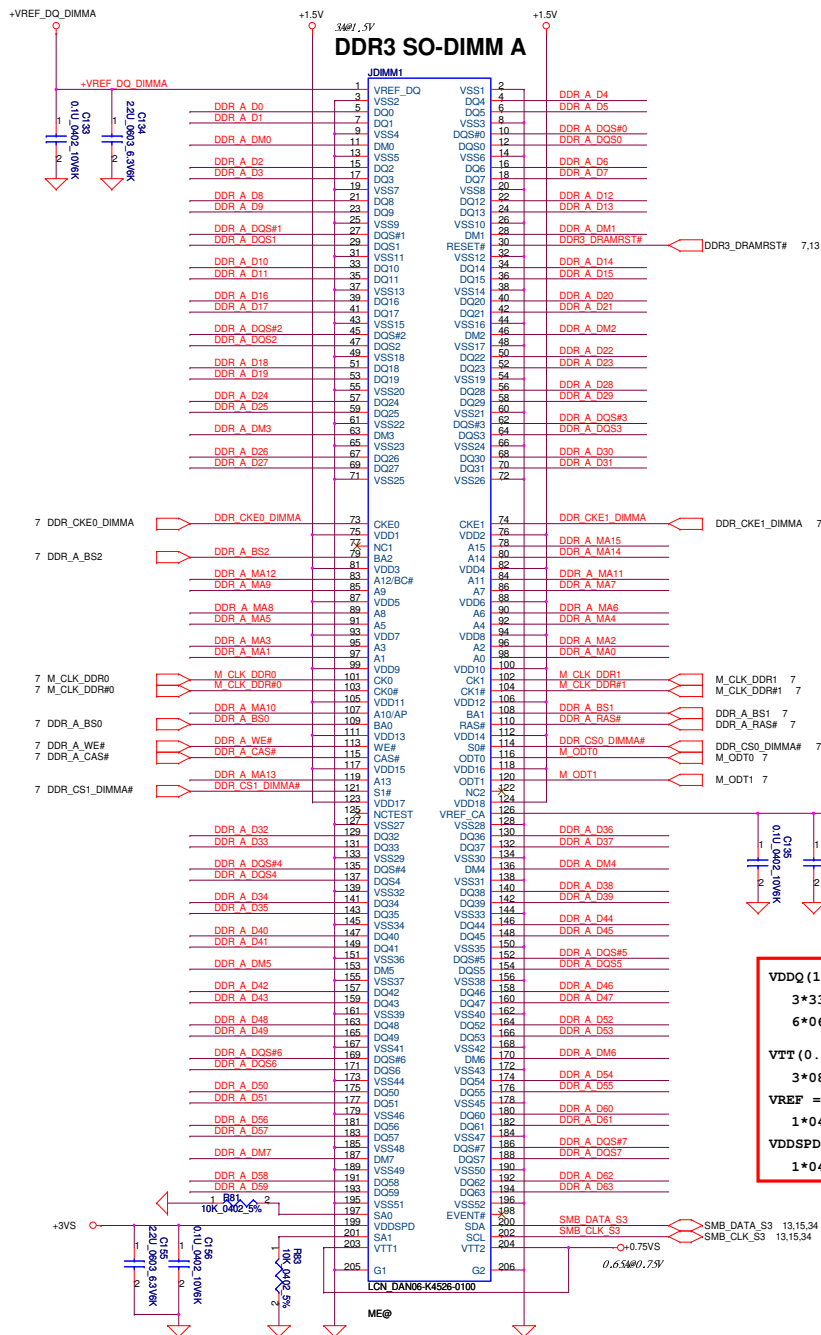
Sandy Bridge_rPGA_Rev1p0
ME@

JCPU1I

T35	VSS161	VSS234	F22
T34	VSS162	VSS235	F19
T33	VSS163	VSS236	E30
T32	VSS164	VSS237	E27
T31	VSS165	VSS238	E24
T29	VSS166	VSS239	E18
T28	VSS167	VSS240	E15
T27	VSS168	VSS241	E13
T26	VSS169	VSS242	E10
P9	VSS170	VSS243	E9
P8	VSS171	VSS244	E8
P6	VSS172	VSS245	E7
P5	VSS173	VSS246	E6
P3	VSS174	VSS247	E5
P2	VSS175	VSS248	E4
N35	VSS176	VSS249	E3
N34	VSS177	VSS250	E2
N33	VSS178	VSS251	E1
N32	VSS179	VSS252	D35
N31	VSS180	VSS253	D32
N30	VSS181	VSS254	D29
N29	VSS182	VSS255	D26
N28	VSS183	VSS256	D20
N27	VSS184	VSS257	D17
N26	VSS185	VSS258	C34
N34	VSS186	VSS259	C31
L33	VSS187	VSS260	C28
L32	VSS188	VSS261	C27
L30	VSS189	VSS262	C23
L27	VSS190	VSS263	C10
L19	VSS191	VSS264	C1
L18	VSS192	VSS265	B22
L16	VSS193	VSS266	B19
L15	VSS194	VSS267	B17
L14	VSS195	VSS268	B15
L13	VSS196	VSS269	B13
L12	VSS197	VSS270	B11
L11	VSS198	VSS271	B9
K35	VSS199	VSS272	B8
K32	VSS200	VSS273	B7
K29	VSS201	VSS274	B5
K26	VSS202	VSS275	B3
K34	VSS203	VSS276	A35
J31	VSS204	VSS277	A32
H33	VSS205	VSS278	A29
H30	VSS206	VSS279	A26
H27	VSS207	VSS280	A23
H24	VSS208	VSS281	A20
H21	VSS209	VSS282	A3
H18	VSS210	VSS283	
H15	VSS211	VSS284	
H13	VSS212	VSS285	
H10	VSS213		
H9	VSS214		
H8	VSS215		
H7	VSS216		
H6	VSS217		
H5	VSS218		
H4	VSS219		
H3	VSS220		
H2	VSS221		
H1	VSS222		
G35	VSS223		
G32	VSS224		
G29	VSS225		
G26	VSS226		
G23	VSS227		
G20	VSS228		
G17	VSS229		
G11	VSS230		
F34	VSS231		
F31	VSS232		
F29	VSS233		

Sandy Bridge_rPGA_Rev1p0
ME@

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	PROCESSOR(7/7) VSS
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MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Customer	QIQY2 LA6884P
				Date:	Wednesday, May 11, 2011
				Sheet	11 of 60



VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

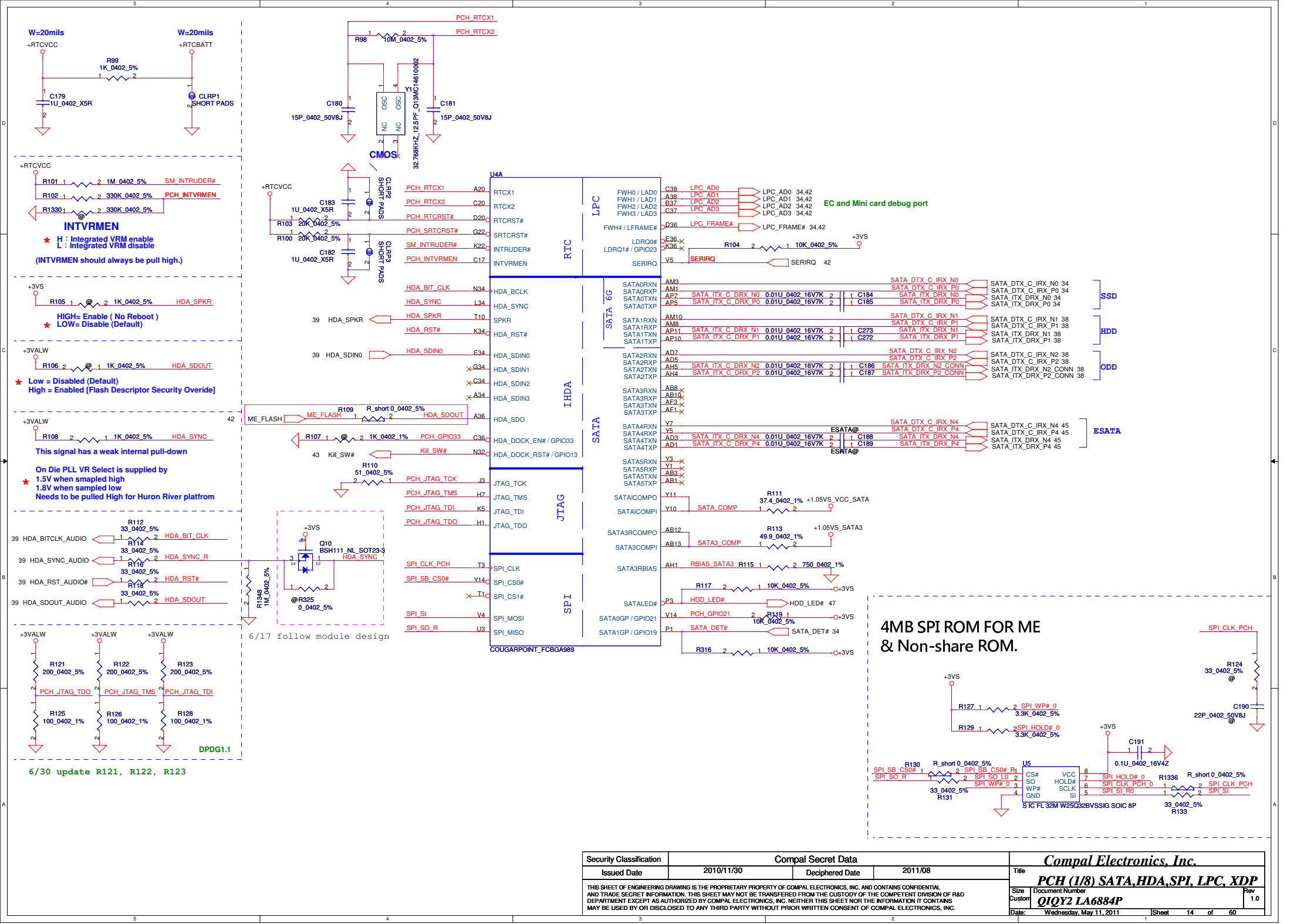
VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf

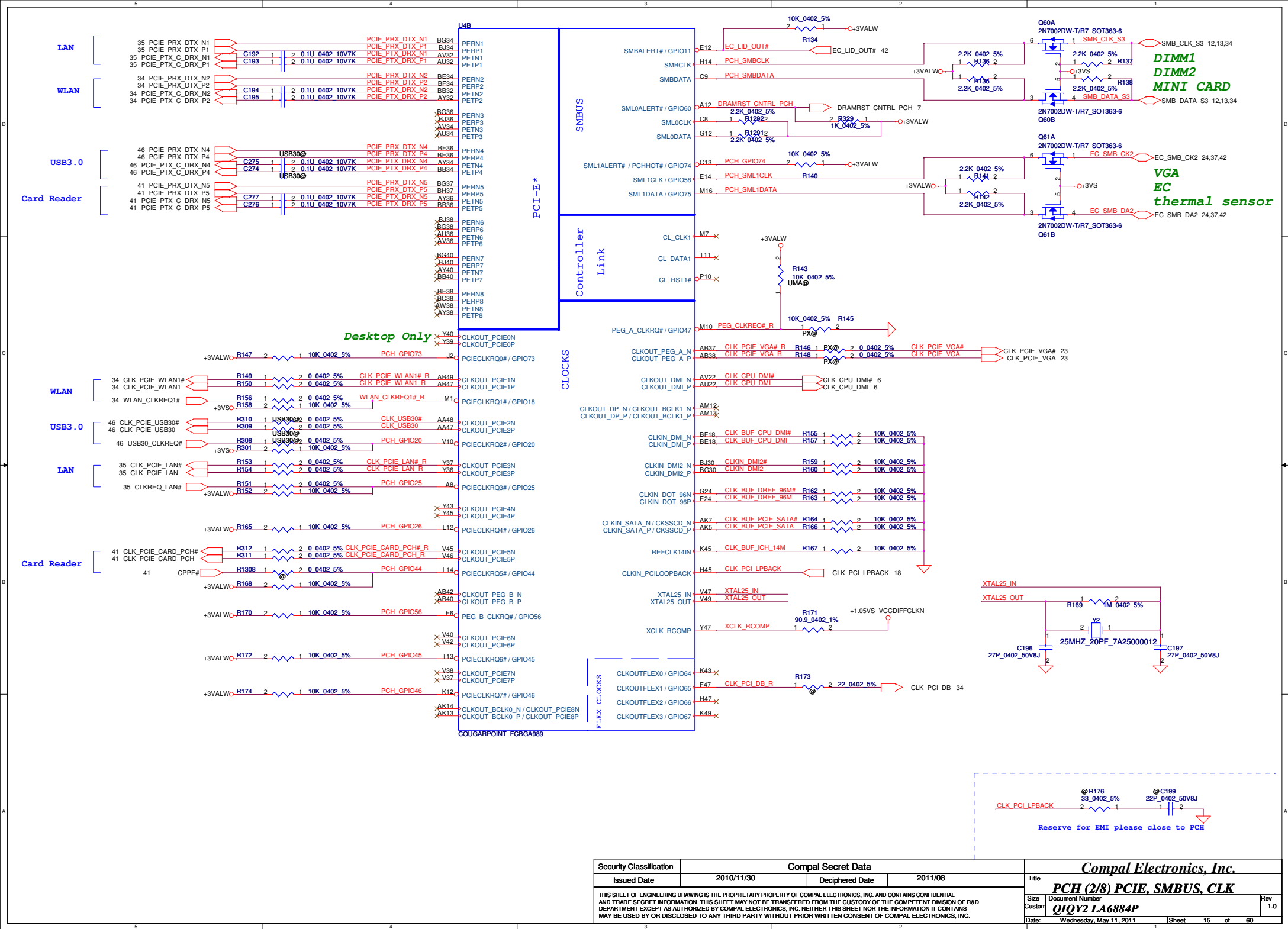
Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

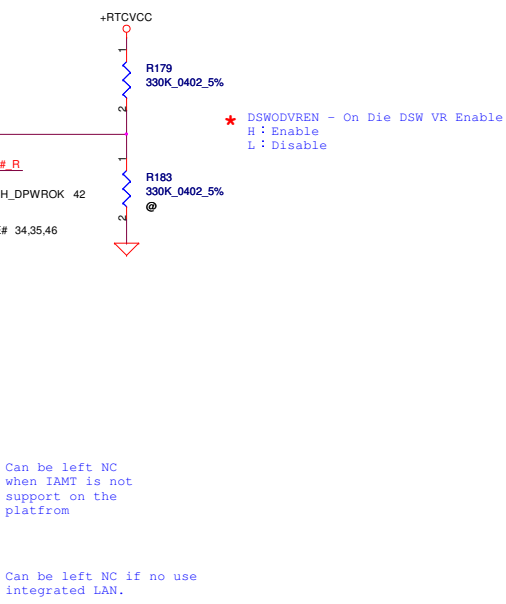
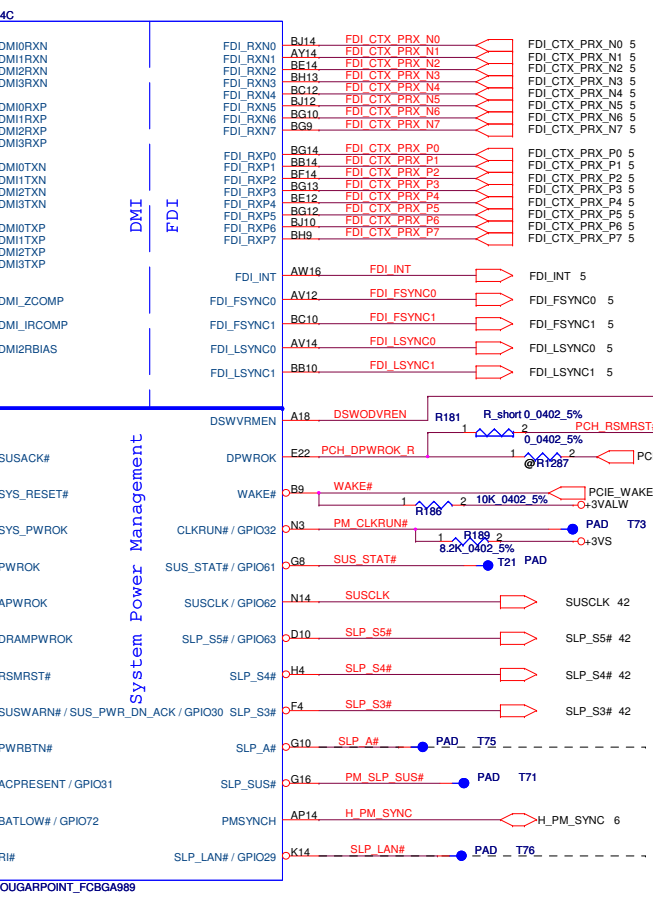
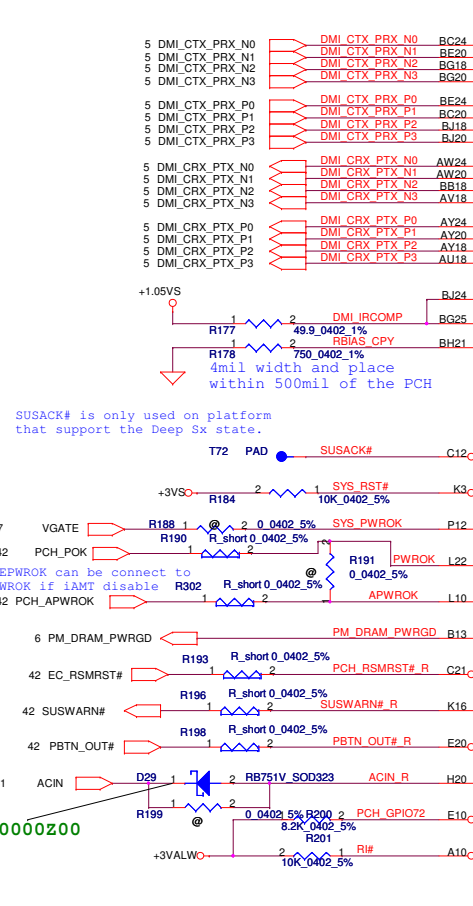
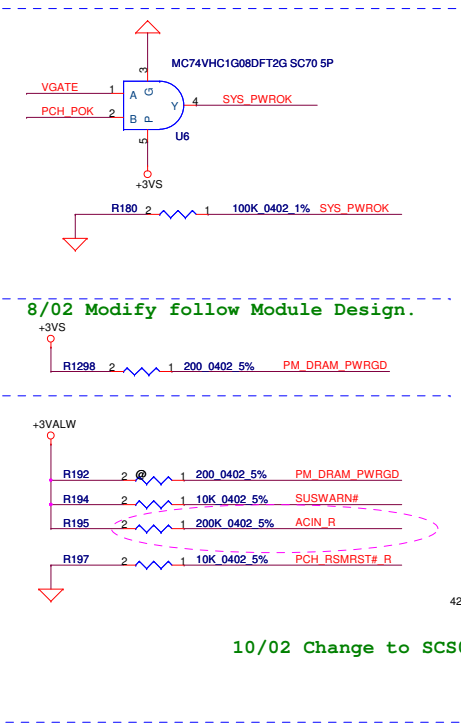
Layout Note:
Short to ground

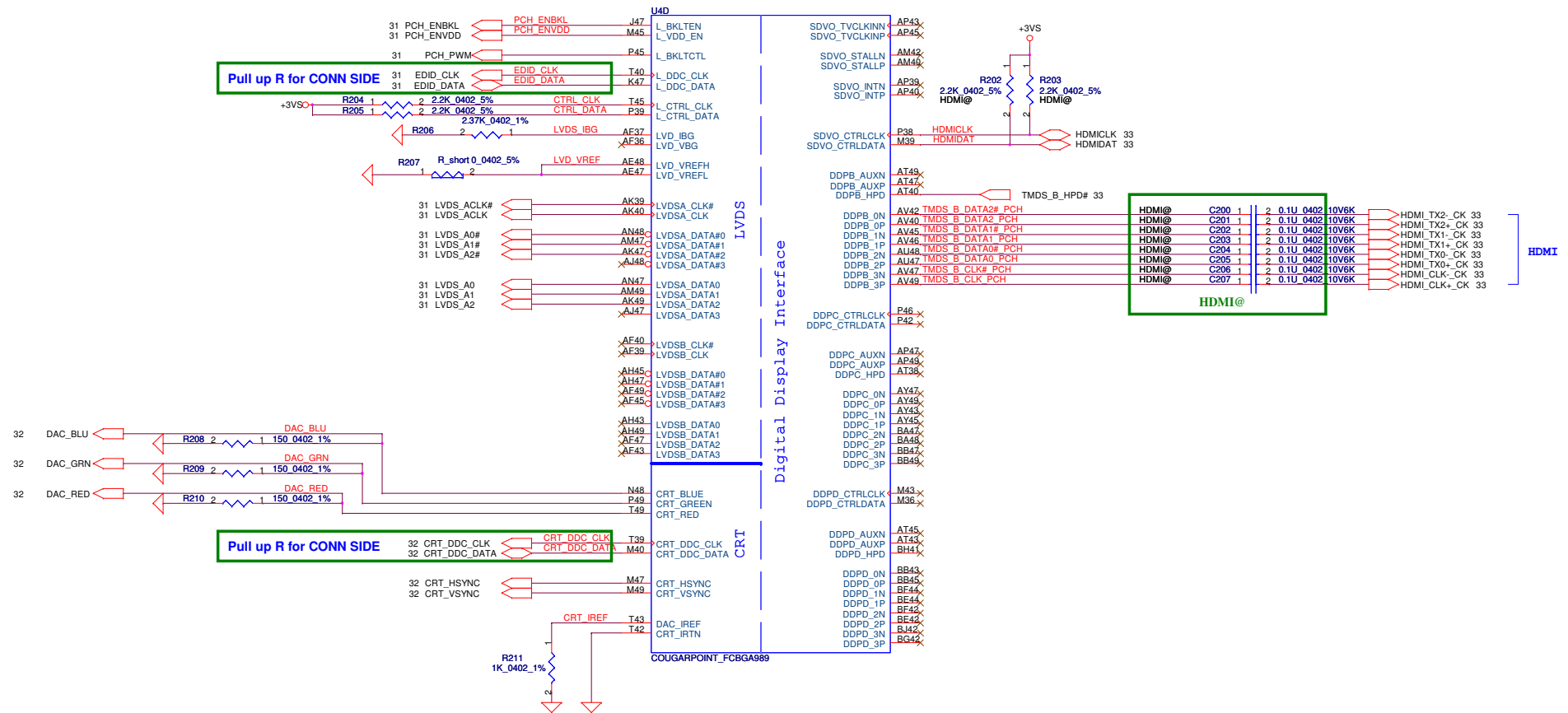
Security Classification		Compal Secret Data		Title	
Issued Date	2010/11/30	Deciphered Date	2011/08	DDRIII-SODIMM SLOT1	
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				QIQY2 LA6884P	
				Date: Wednesday, May 11, 2011	Sheet 12 of 60

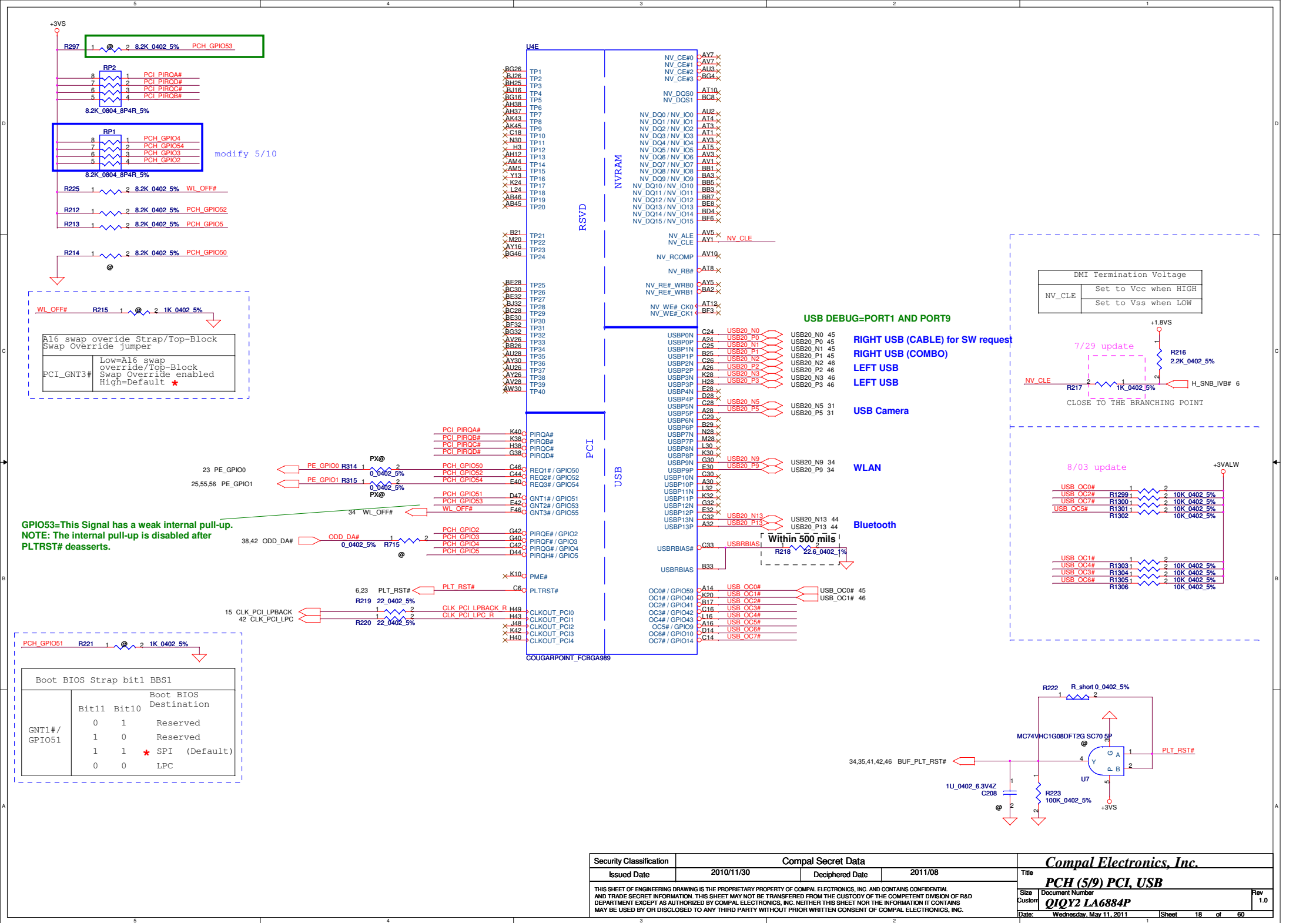




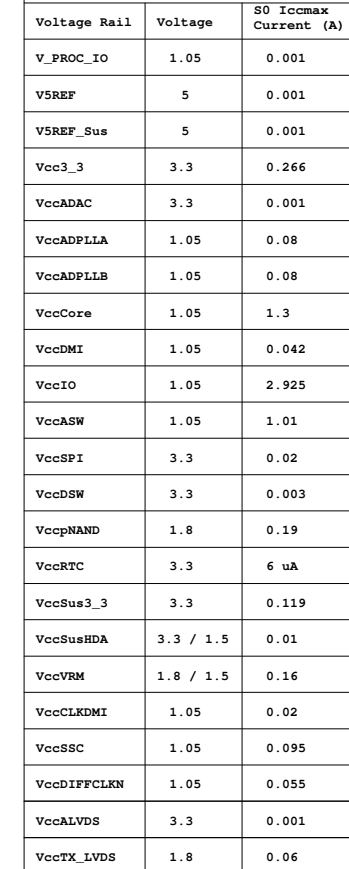
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	PCH (2/8) PCIE, SMBUS, CLK	
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					QI0Y2 LA6884P	1.0
				Date:	Wednesday, May 11, 2011	Sheet





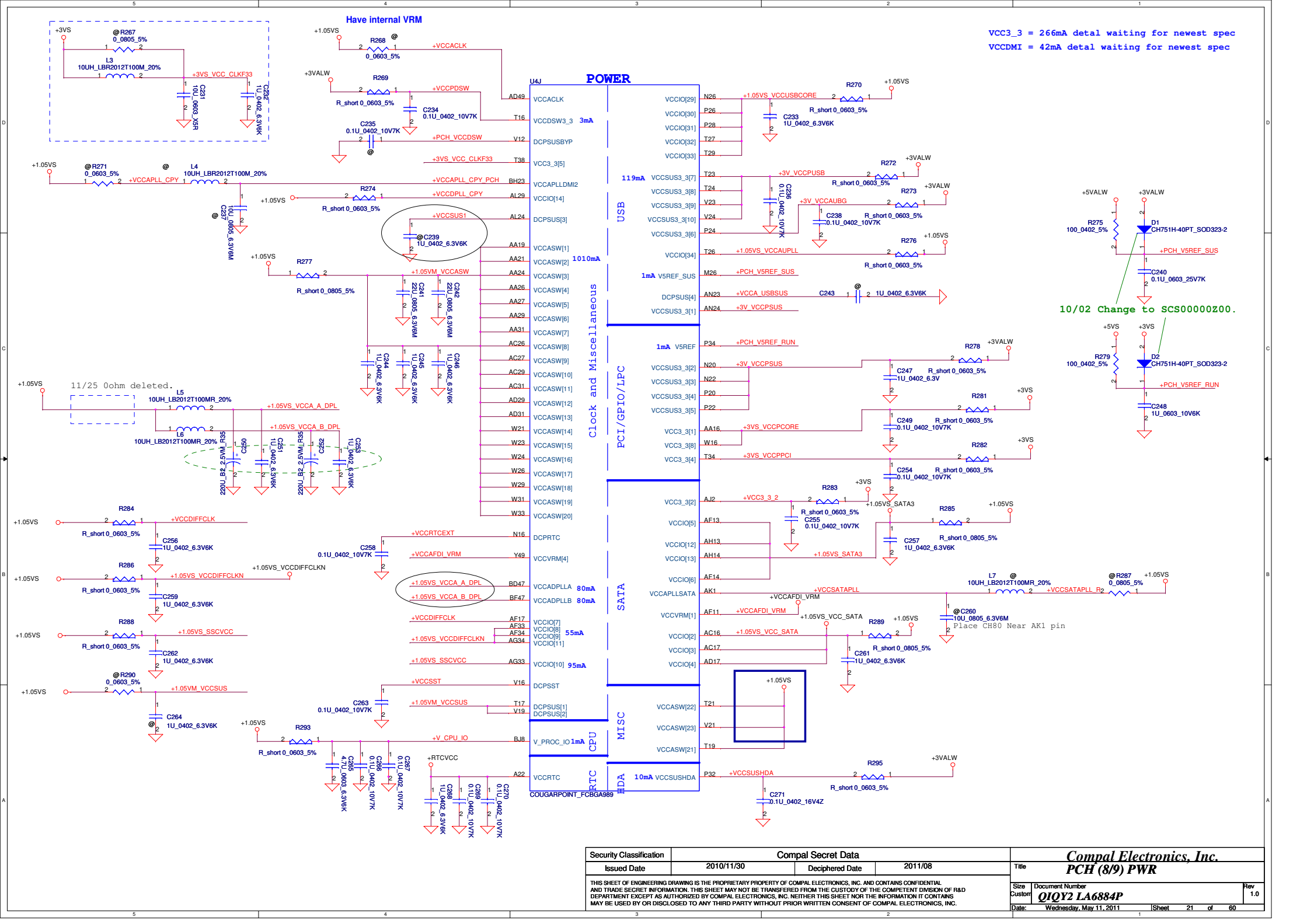


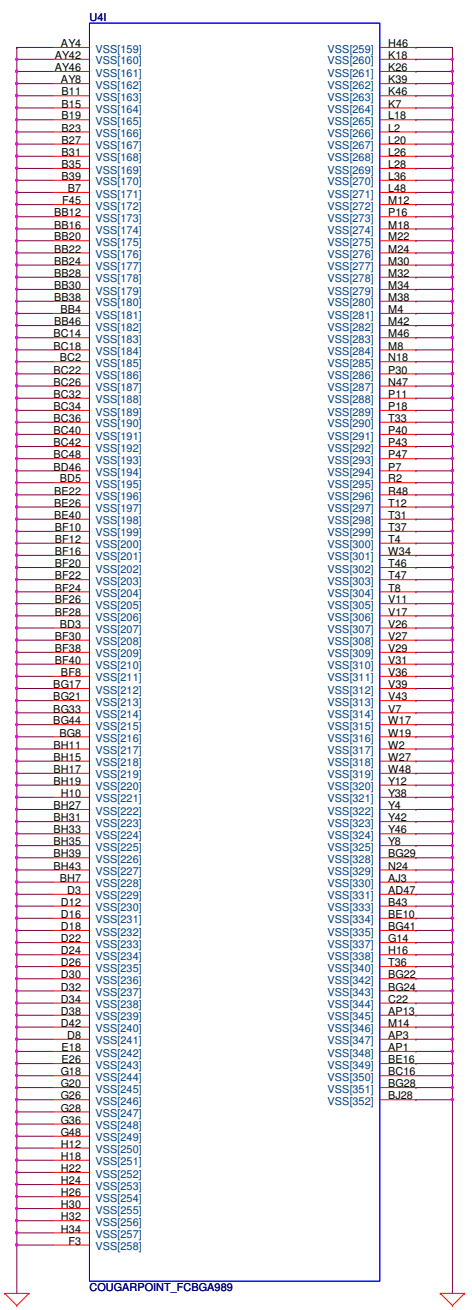
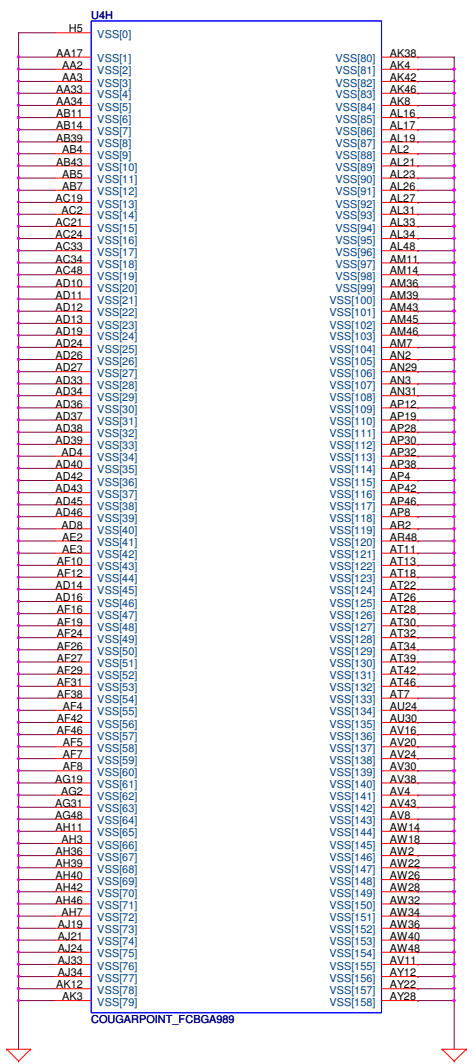
PCH Power Rail Table



VCCVRM = 160mA detal waiting for newest spec

Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> PCH (7/9) PWR	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	Rev 1.0 QIQY2 LA6884P
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				Date:	Wednesday, May 11, 2011 Sheet 20 of 60





5 PCIE_CTX_GRX_P[15..0]
5 PCIE_CTX_GRX_N[15..0]

PCIE_CTX_GRX_P[15..0]
PCIE_CTX_GRX_N[15..0]

U8A PX@

PCIE_CRX_GTX_P[15..0]
PCIE_CRX_GTX_N[15..0]

PCIE_CRX_GTX_P[15..0] 5
PCIE_CRX_GTX_N[15..0] 5

LVDS Interface

PCIE_CTX_GRX_P0 AA38
PCIE_CTX_GRX_N0 Y37
PCIE_CTX_GRX_P1 Y35
PCIE_CTX_GRX_N1 W36
PCIE_CTX_GRX_P2 W38
PCIE_CTX_GRX_N2 V37
PCIE_CTX_GRX_P3 Y35
PCIE_CTX_GRX_N3 U36
PCIE_CTX_GRX_P4 U38
PCIE_CTX_GRX_N4 T37
PCIE_CTX_GRX_P5 T35
PCIE_CTX_GRX_N5 R36
PCIE_CTX_GRX_P6 R38
PCIE_CTX_GRX_N6 P37
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PCIE_CTX_GRX_N9 L36
PCIE_CTX_GRX_P10 L38
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PCIE_CTX_GRX_P11 K35
PCIE_CTX_GRX_N11 J36
PCIE_CTX_GRX_P12 J38
PCIE_CTX_GRX_N12 H37
PCIE_CTX_GRX_P13 H35
PCIE_CTX_GRX_N13 G36
PCIE_CTX_GRX_P14 G38
PCIE_CTX_GRX_N14 F37
PCIE_CTX_GRX_P15 F35
PCIE_CTX_GRX_N15 E37

CLOCK
PCIE_REFCLKP
PCIE_REFCLKN

15 CLK_PCIE_VGA
15 CLK_PCIE_VGA#

PX@
R1355
10K_0402_5%
VGA_RST#
AA30

WHESTLERM2

PCI EXPRESS INTERFACE

CALIBRATION

PCIE_CALRP
PCIE_CALRN

PWRGOOD
PERSTB

PCIE_TX0P Y33
PCIE_TX0N Y32
PCIE_TX1P W33
PCIE_TX1N W32
PCIE_TX2P U33
PCIE_TX2N U32
PCIE_TX3P U30
PCIE_TX3N U29
PCIE_TX4P T33
PCIE_TX4N T32
PCIE_TX5P T30
PCIE_TX5N T29
PCIE_TX6P P33
PCIE_TX6N P32
PCIE_TX7P P30
PCIE_TX7N P29
PCIE_TX8P N33
PCIE_TX8N N32
PCIE_TX9P N30
PCIE_TX9N N29
PCIE_TX10P L33
PCIE_TX10N L32
PCIE_TX11P K30
PCIE_TX11N K29
PCIE_TX12P J33
PCIE_TX12N J32
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PCIE_TX14P G30
PCIE_TX14N K29
PCIE_TX15P H33
PCIE_TX15N H32

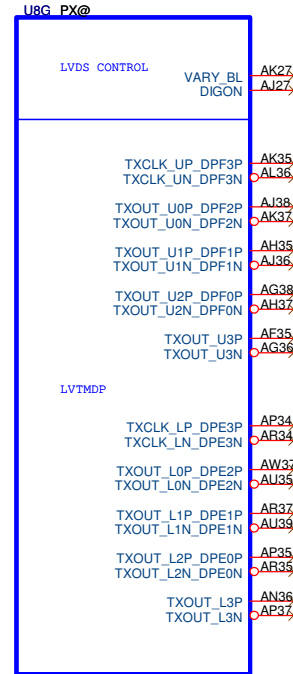
Y30 1.27K 0402 1% PX@ 2 R1354
Y29 2K 0402 5% 1 PX@ 2 R1356

PCIE LANE

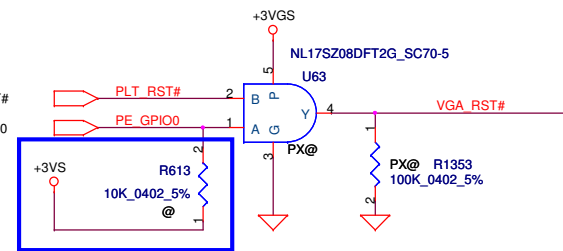
modify 3/17

+1.0VGS

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Issued Date	2010/07/12	Deciphered Date	2012/07/11
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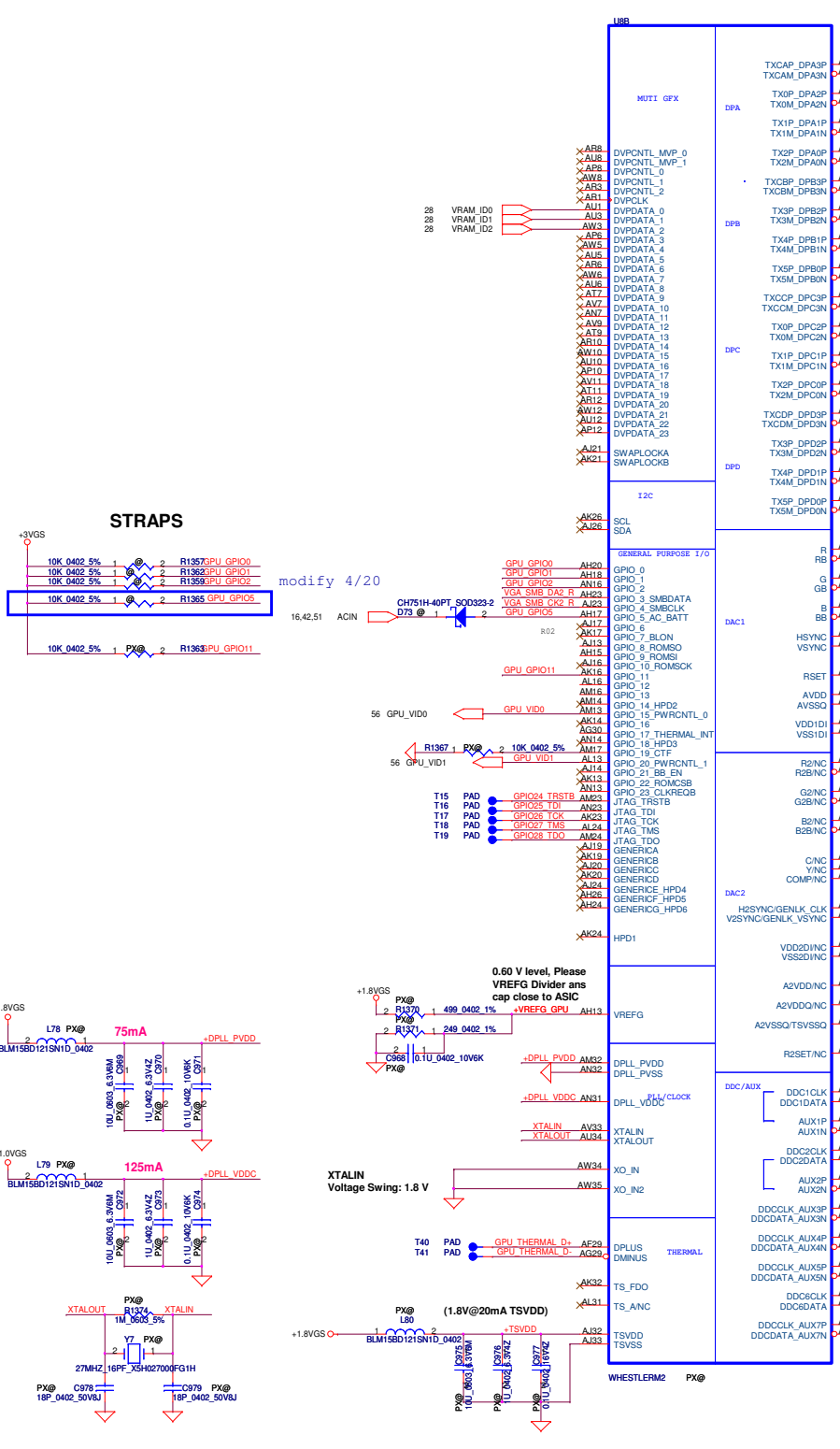
WHESTLERM2

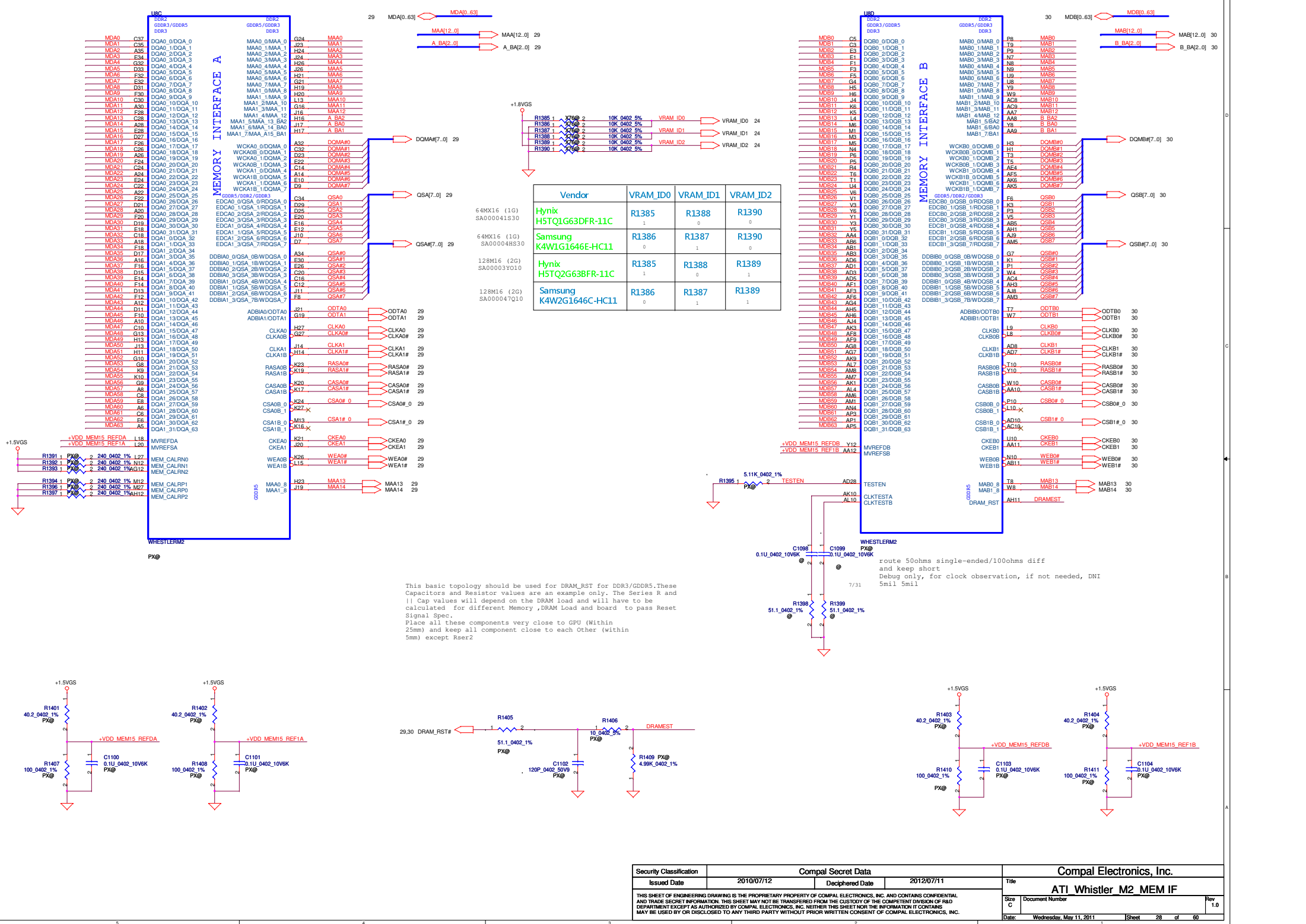


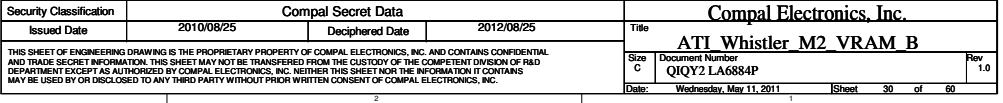
Compal Electronics, Inc.

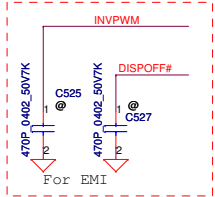
ATI Whistler_M2_PEG & LVDS

Size B	Document Number	Rev 1.0
Date: Wednesday, May 11, 2011	Sheet 23 of 60	

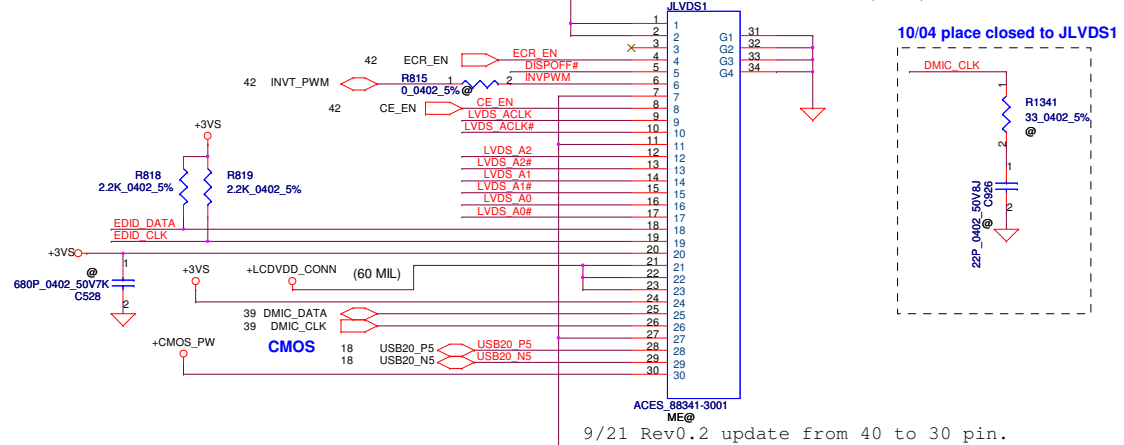
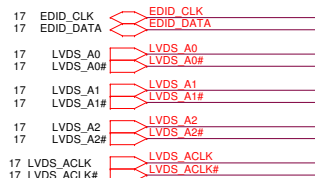
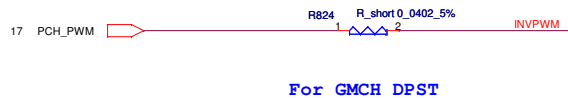
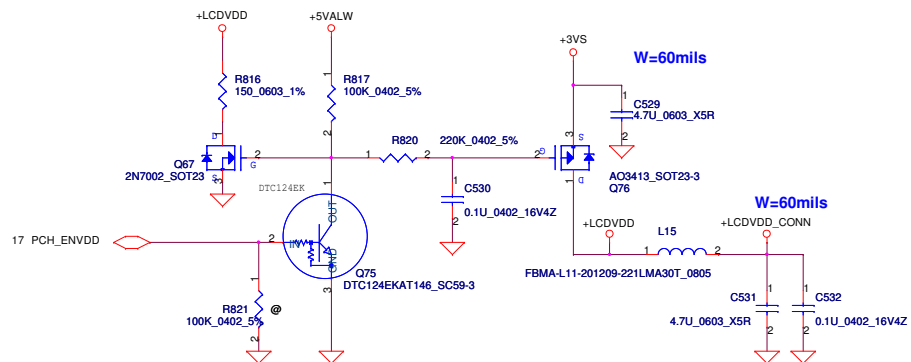




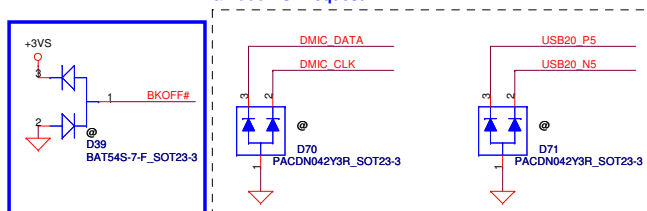




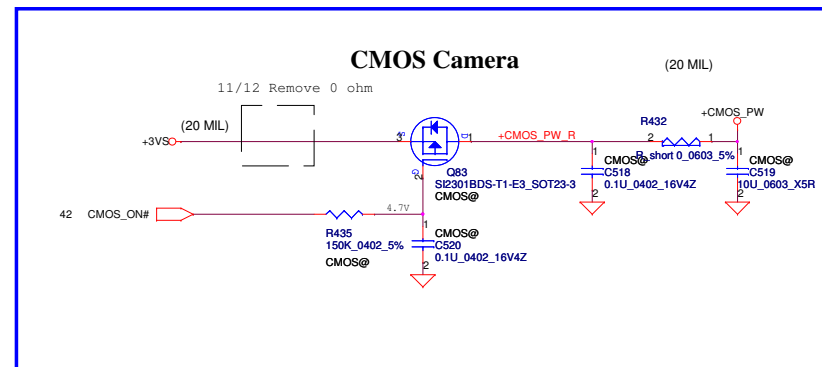
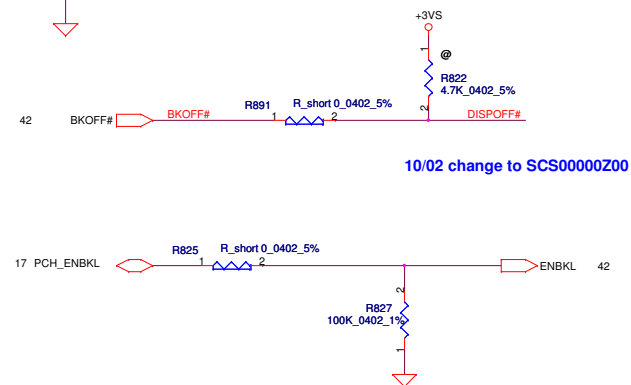
LCD POWER CIRCUIT



8/4 add ESD request



modify 4/20



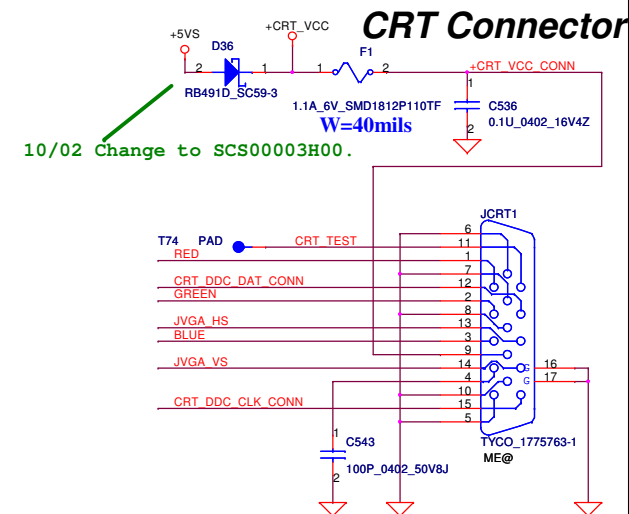
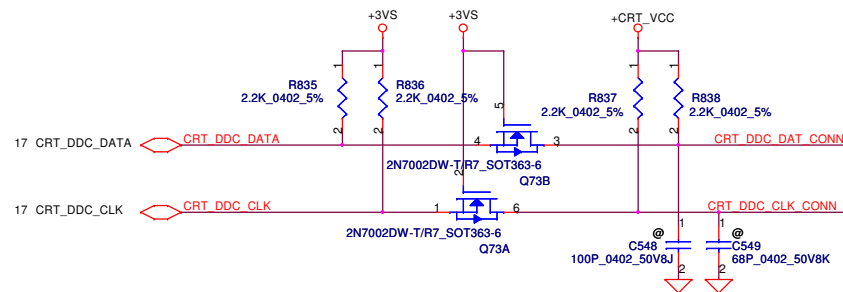
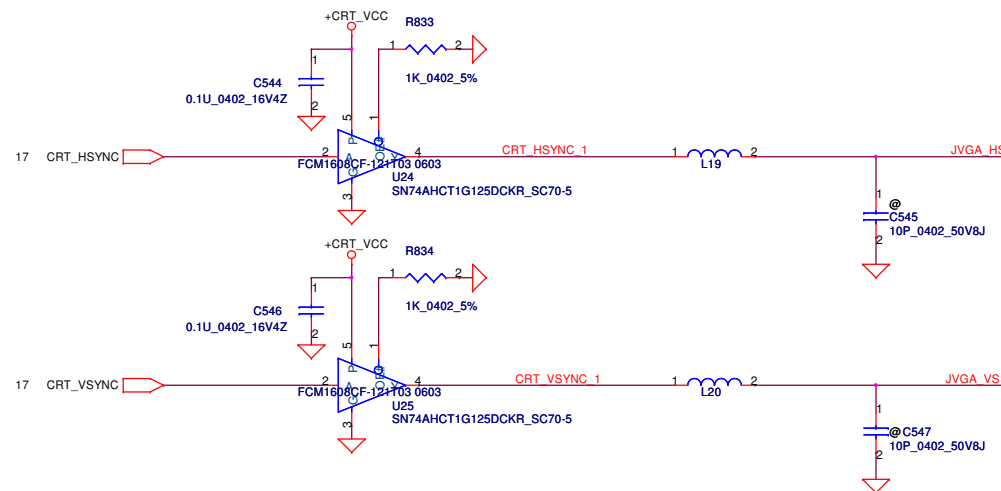
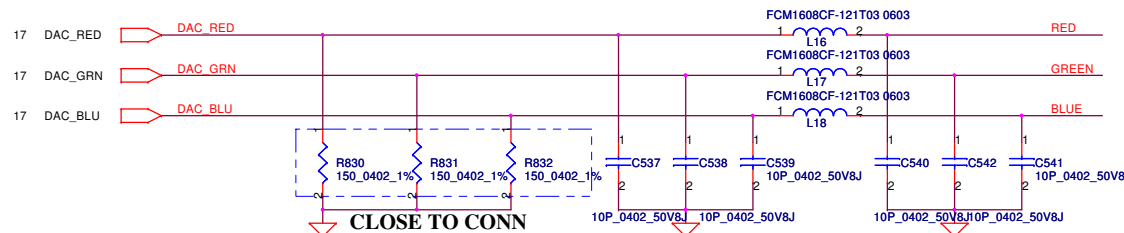
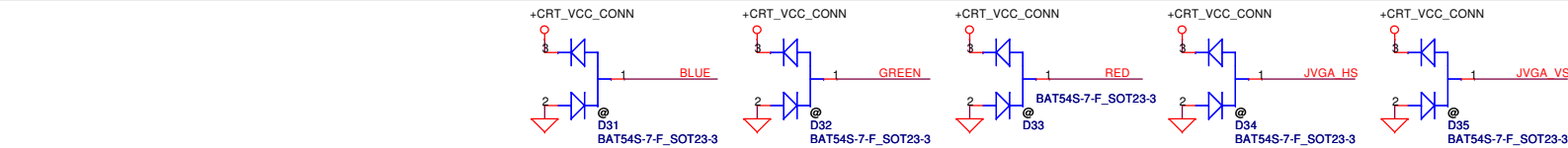
Security Classification		Compal Secret Data		Title	
Issued Date	2010/11/30	Deciphered Date	2011/08	Size	Document Number
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				Sheet	31 of 60

Compal Electronics, Inc.

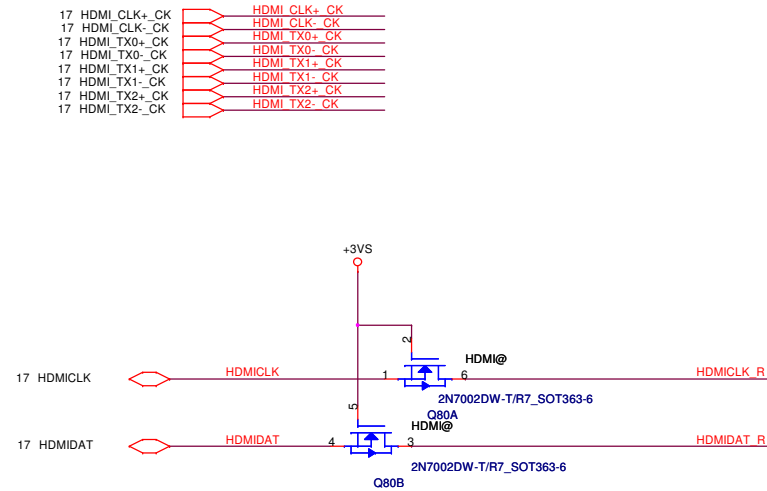
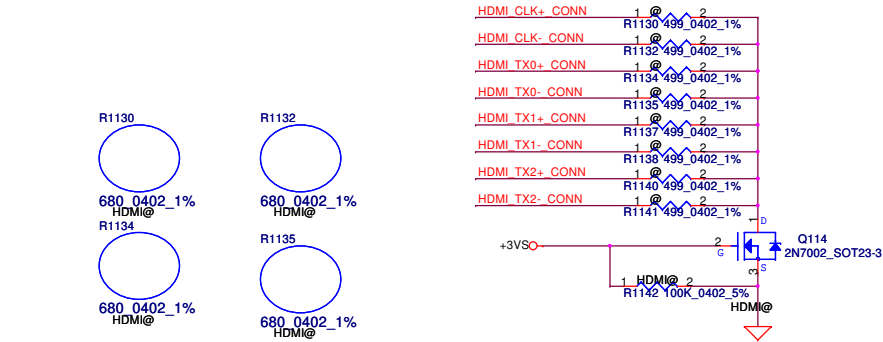
LVDS/CAMERA

QIQY2 LA6884P

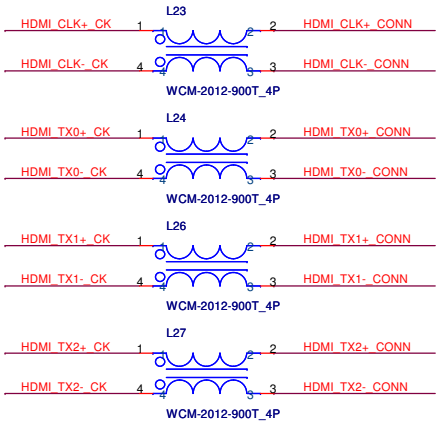
Rev 1.0



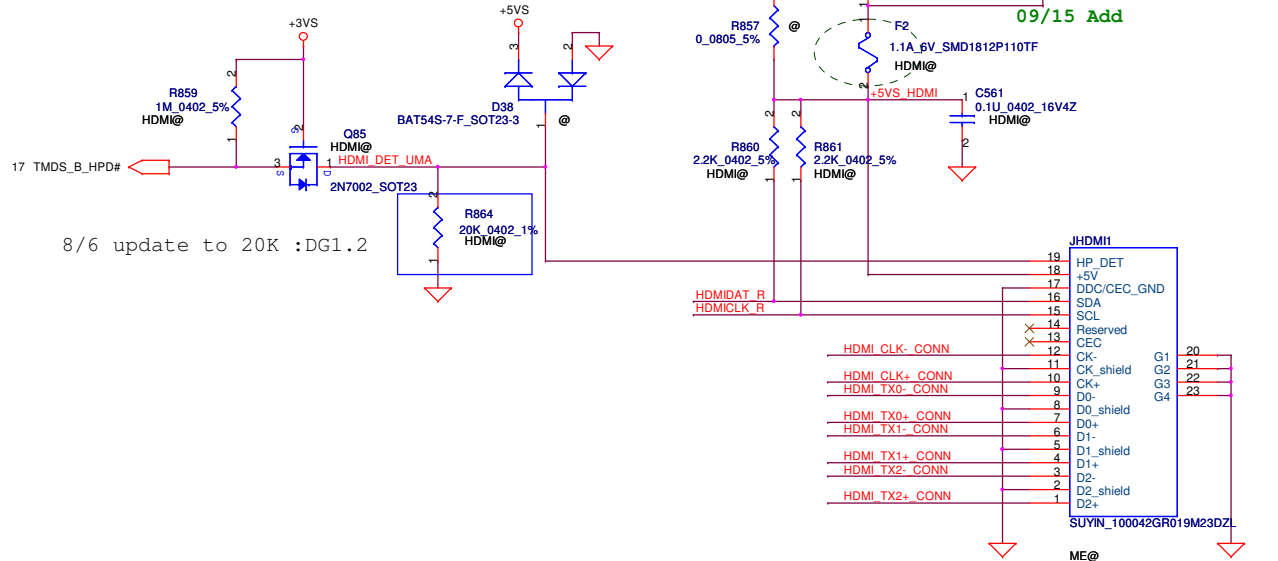
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	
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				Custom	QIQY2 LA6884P
				Date	Wednesday, May 11, 2011
				Sheet	32 of 60
				Rev	1.0



DVT, Change to SM070000I00 for EMI request.



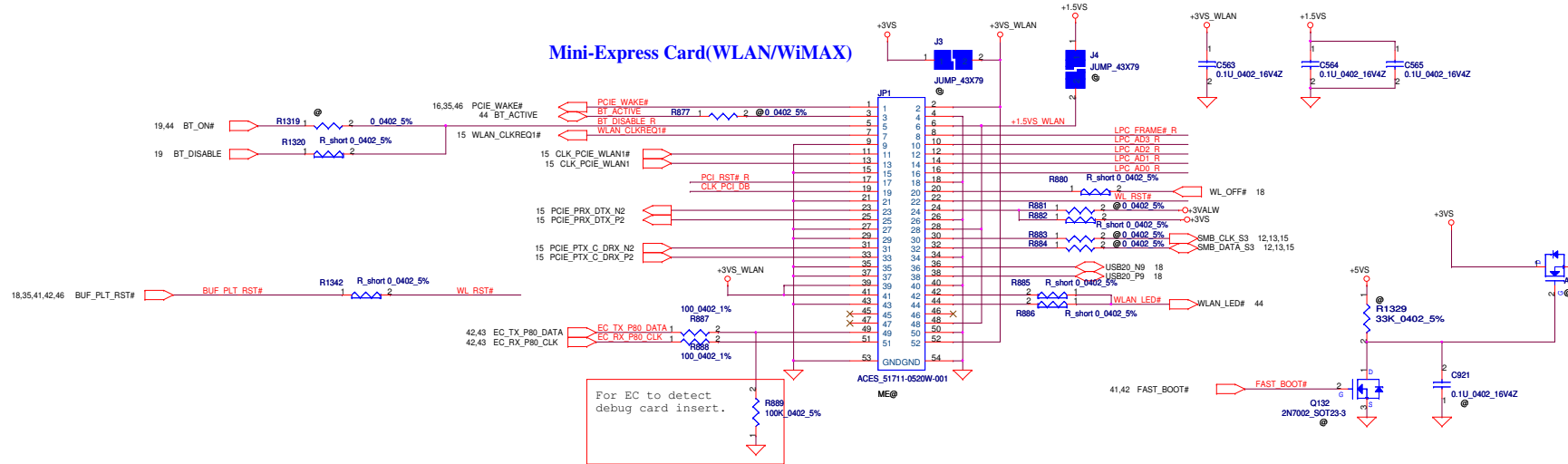
HDMI CLK+ CK	R885	1	0	0402_5%	HDMI CLK+ CONN
HDMI CLK- CK	R886	1	0	0402_5%	HDMI CLK- CONN
HDMI TX0+ CK	R887	1	0	0402_5%	HDMI TX0+ CONN
HDMI TX0- CK	R888	1	0	0402_5%	HDMI TX0- CONN
HDMI TX1+ CK	R889	1	0	0402_5%	HDMI TX1+ CONN
HDMI TX1- CK	R890	1	0	0402_5%	HDMI TX1- CONN
HDMI TX2+ CK	R891	1	0	0402_5%	HDMI TX2+ CONN
HDMI TX2- CK	R892	1	0	0402_5%	HDMI TX2- CONN



Security Classification				Compal Secret Data				Compal Electronics, Ltd.			
Issued Date				2010/11/30				Title			
Deciphered Date				2011/08				HDMI CONN			
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				Custom				QIQY2 LA6884P			
				Date: Wednesday, May 11, 2011				Rev 1.0			
				Sheet 33 of 60							

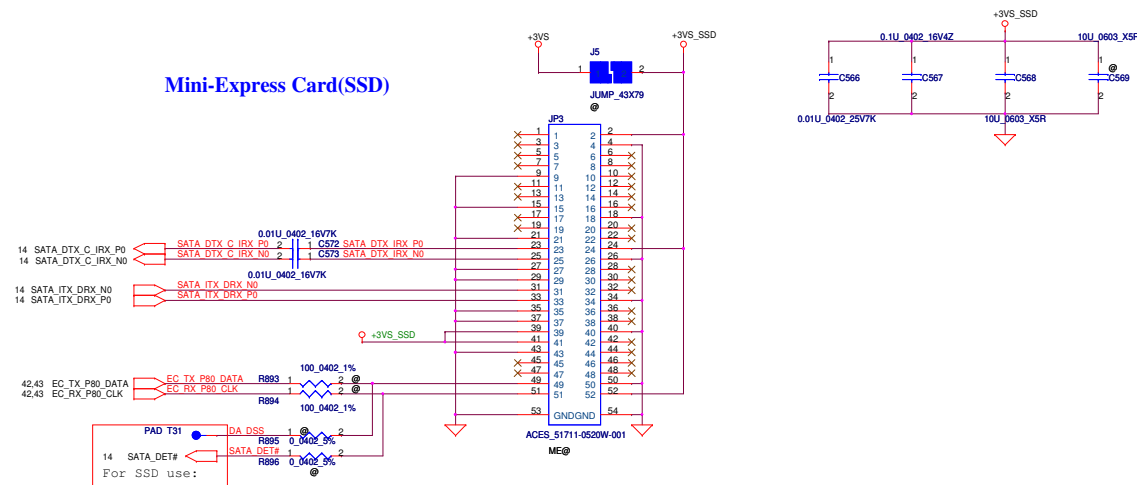
Mini-Express Card for WLAN/WiMAX(Half) Mini-Express Card for SSD(Full)

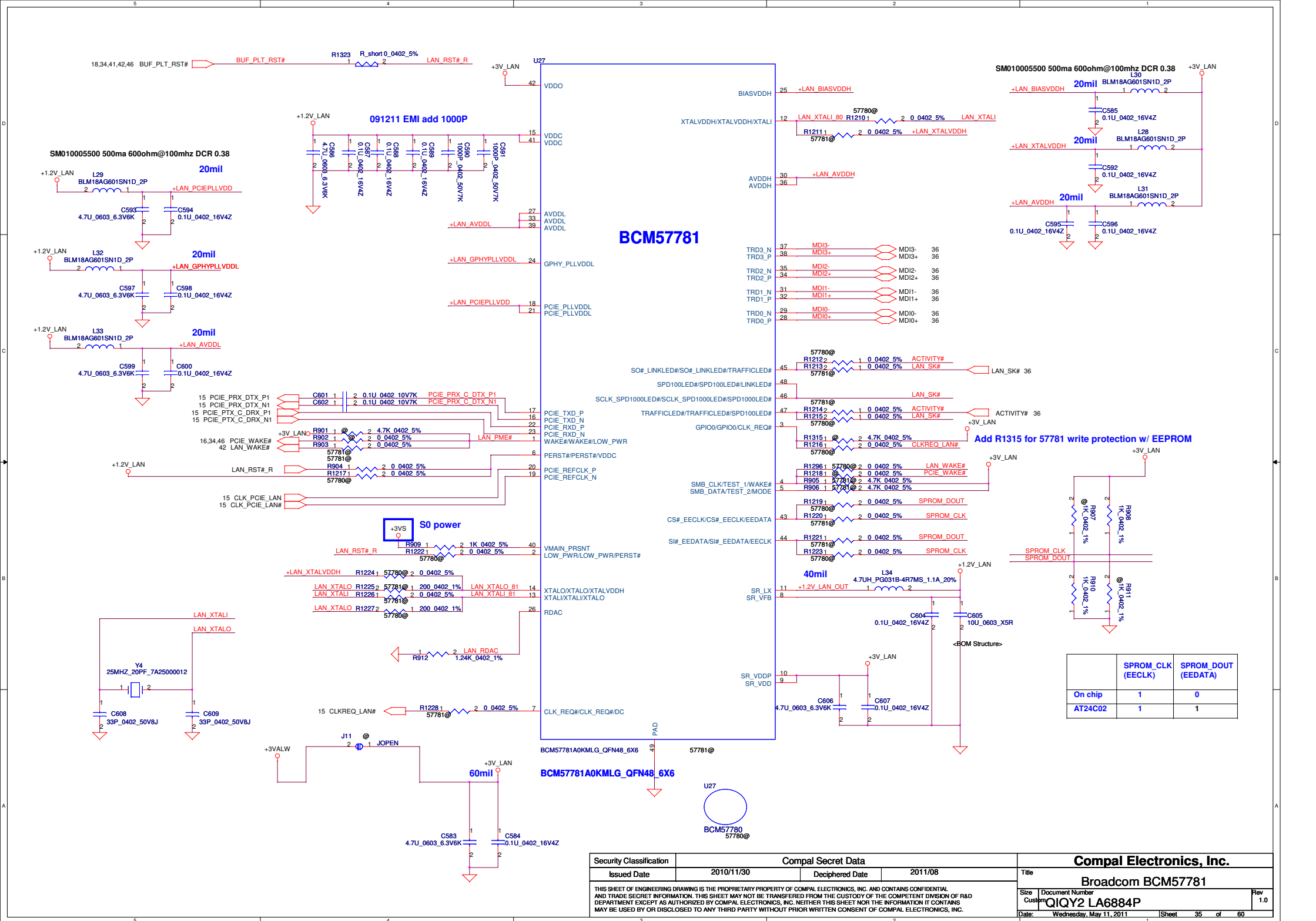
Mini-Express Card(WLAN/WiMAX)

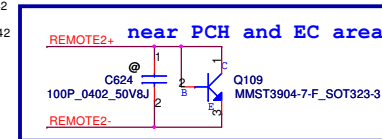
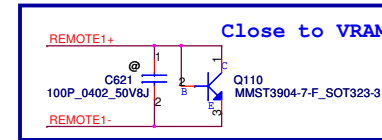
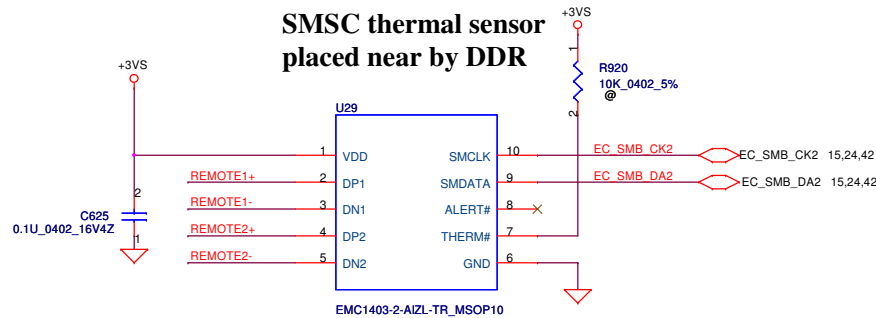
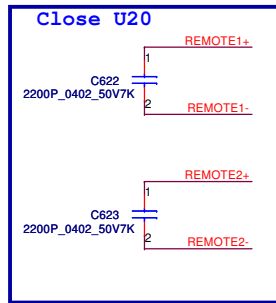


SSD Active:0.22W(0.06A)

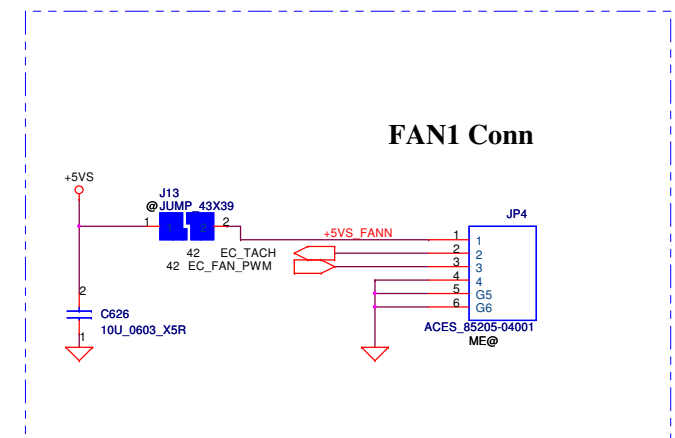
Mini-Express Card(SSD)





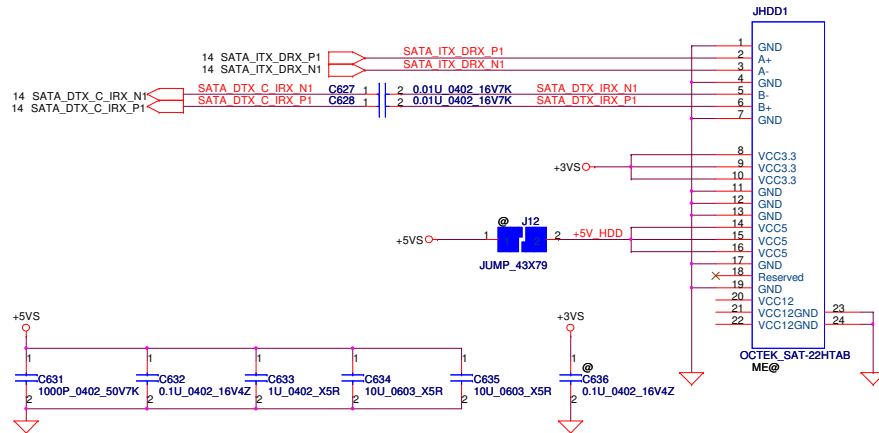


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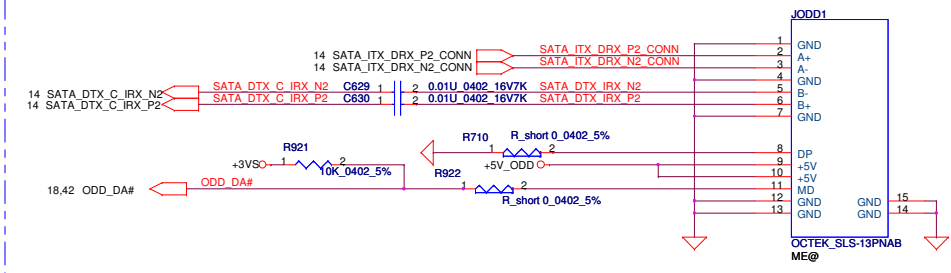


Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	EMC1403_ Thermal sensor/FAN
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				Date: Wednesday, May 11, 2011	Rev 1.0
				Sheet 37 of 60	

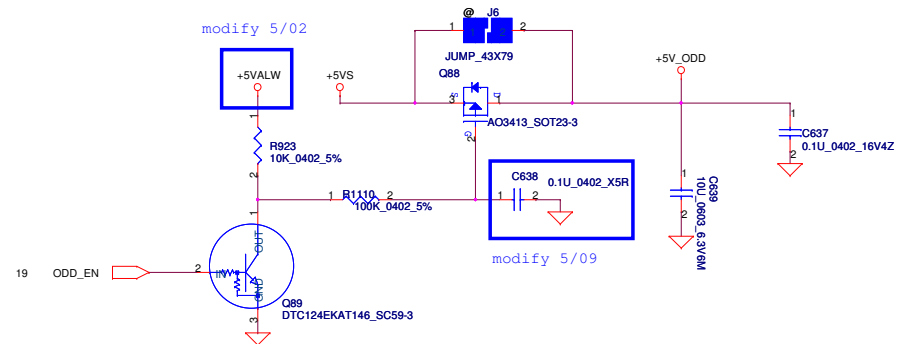
SATA HDD Conn.



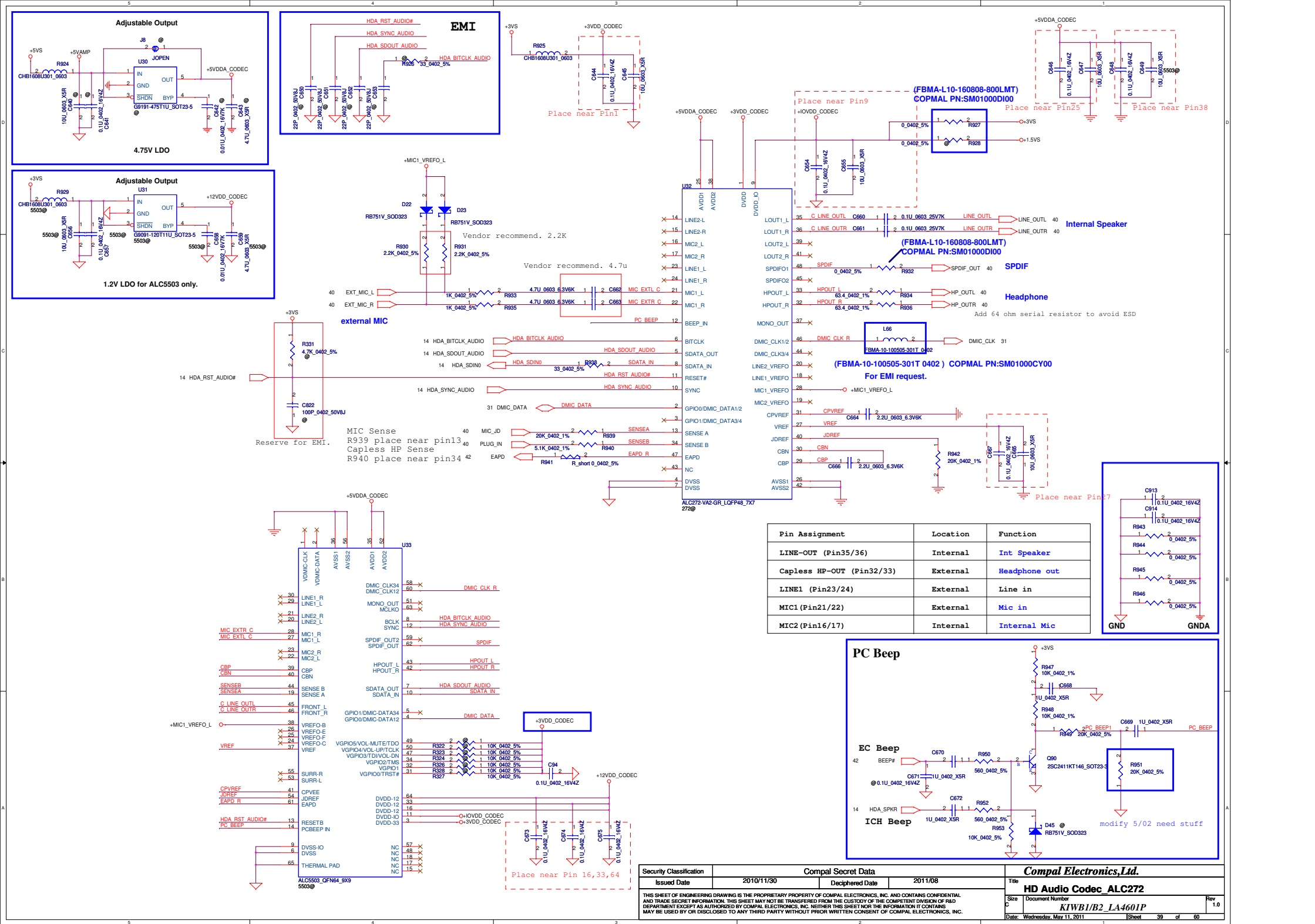
SATA ODD Conn.



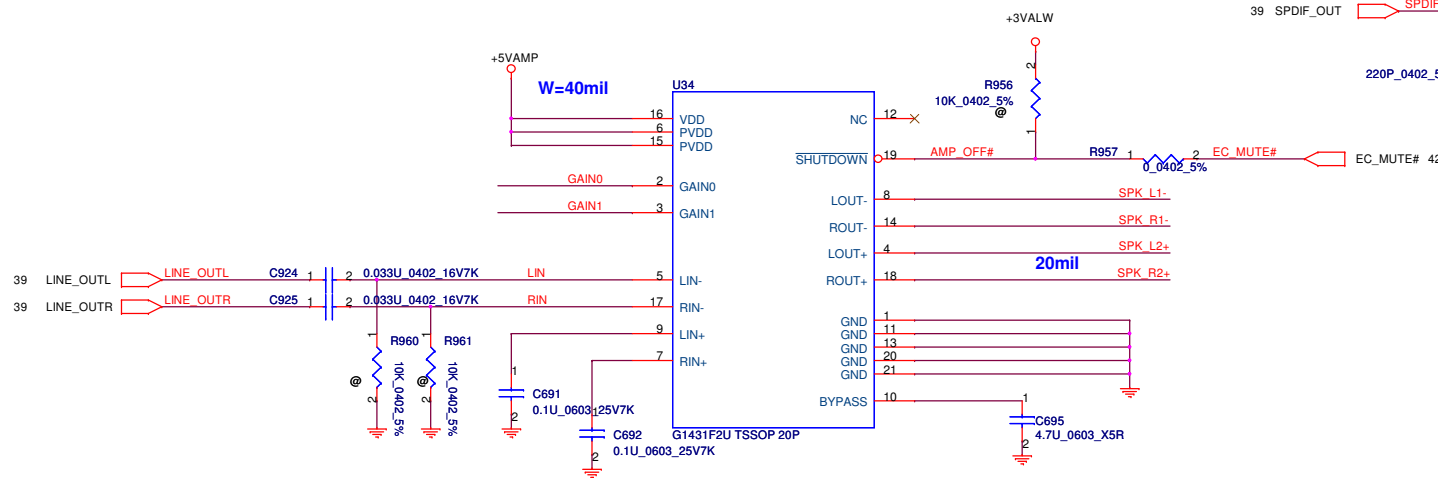
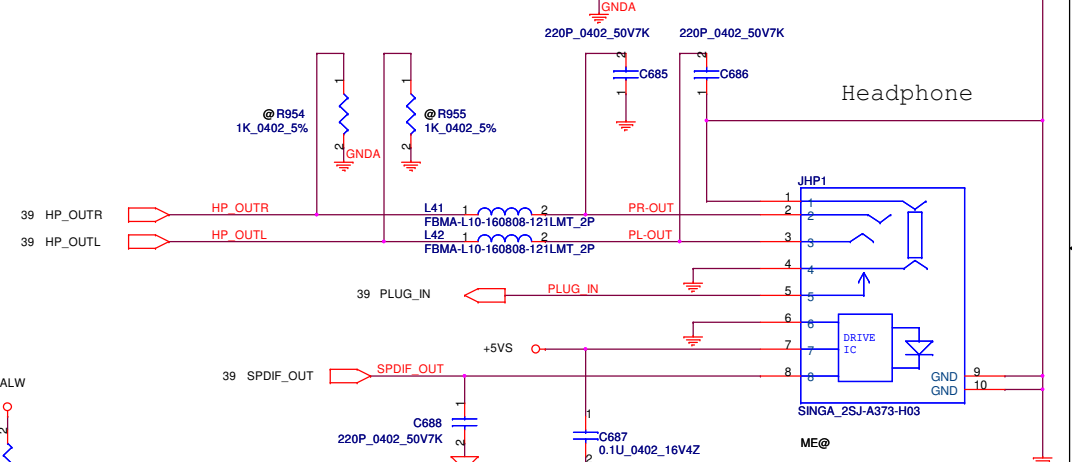
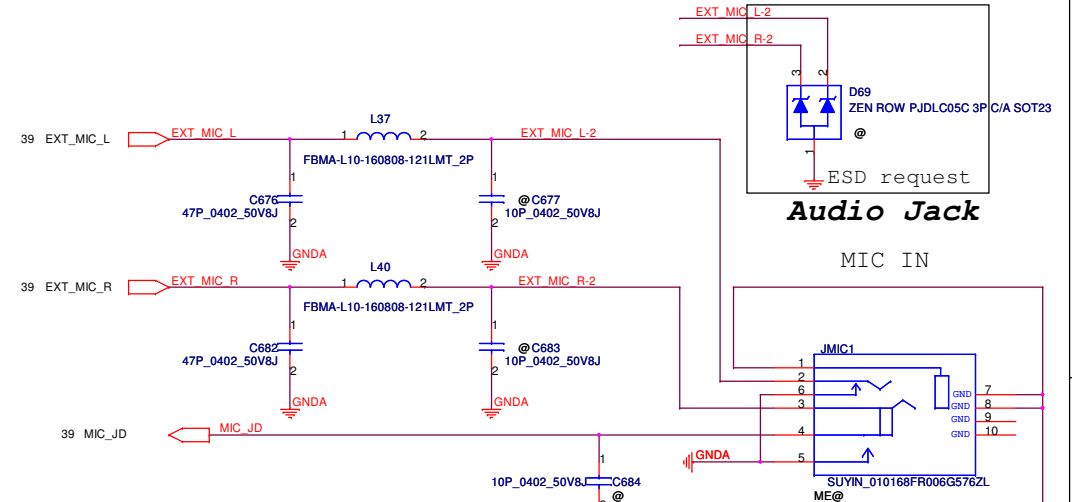
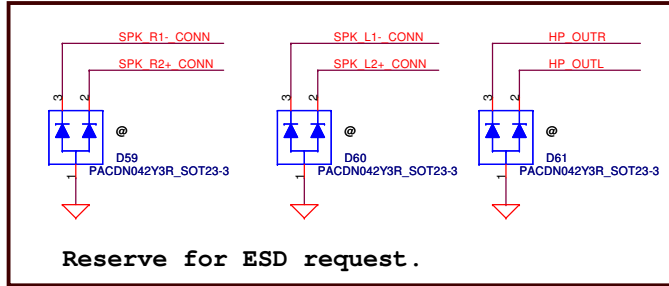
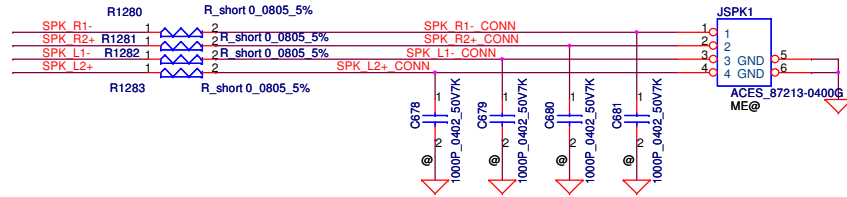
ODD Power Control



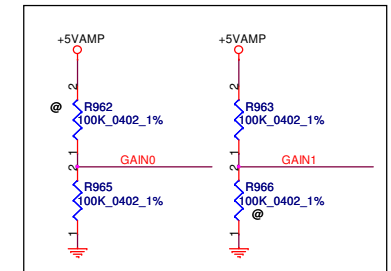
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/11/30	Deciphered Date	2011/08	Title		
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				Size B	Document Number	Rev 1.0
				Date: Wednesday, May 11, 2011		
				Sheet 38	of 60	



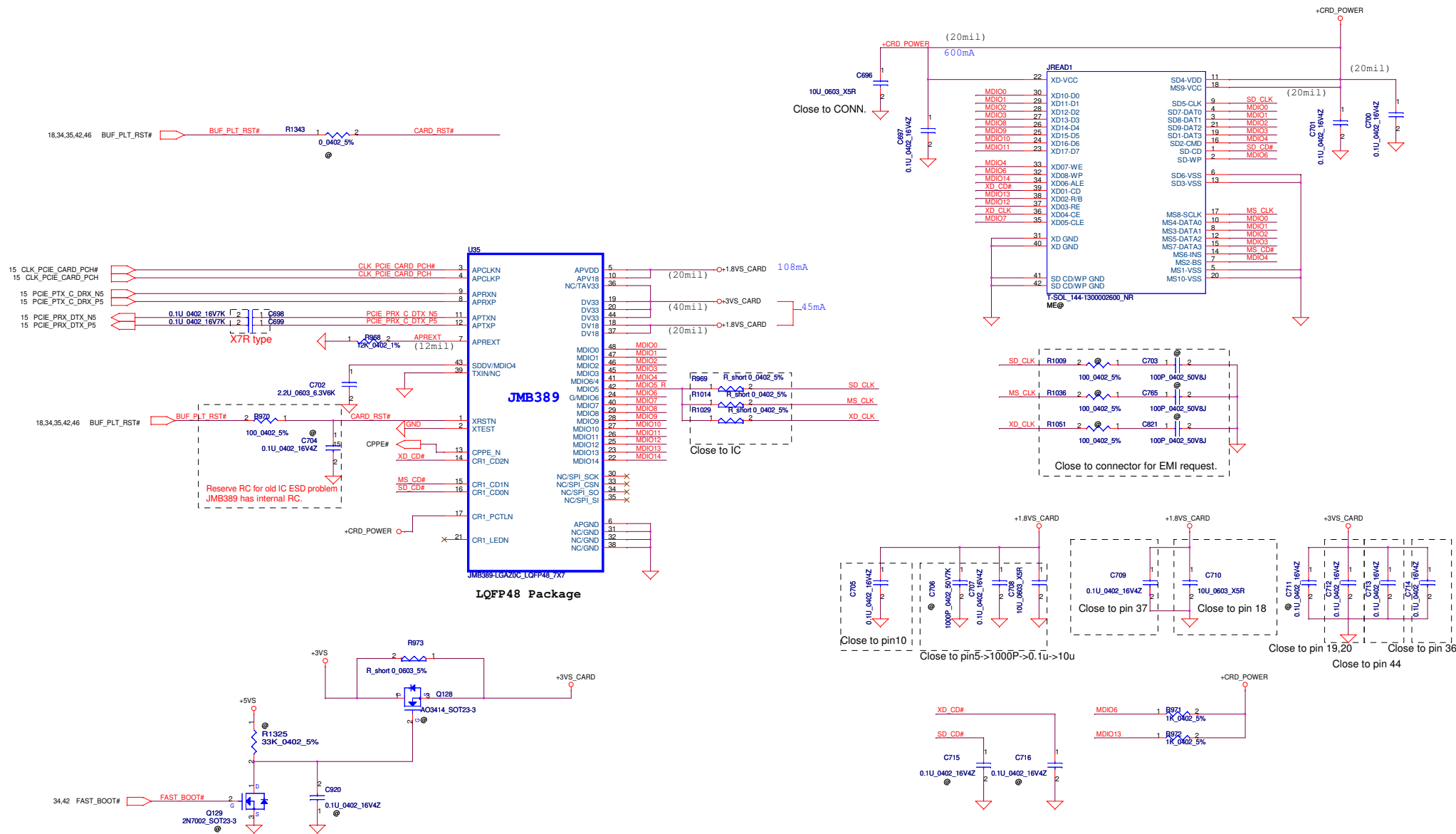
wide 20MIL



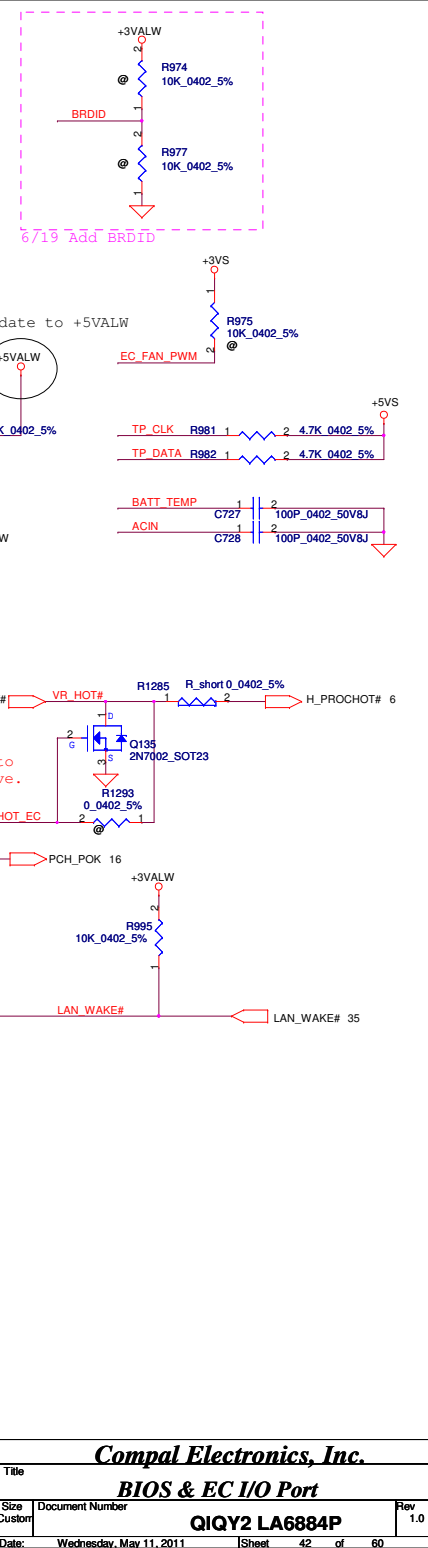
GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



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Issued Date	2010/11/30	Deciphered Date	2011/08	Title	AMP, Audio speaker CONN
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				KIWB1/B2_LA4601P	
				Date: Wednesday, May 11, 2011	Sheet 40 of 60

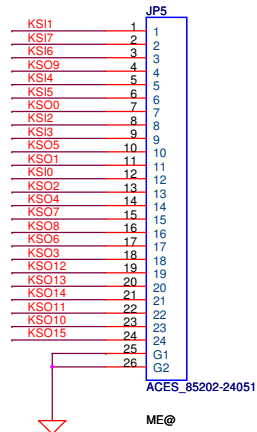
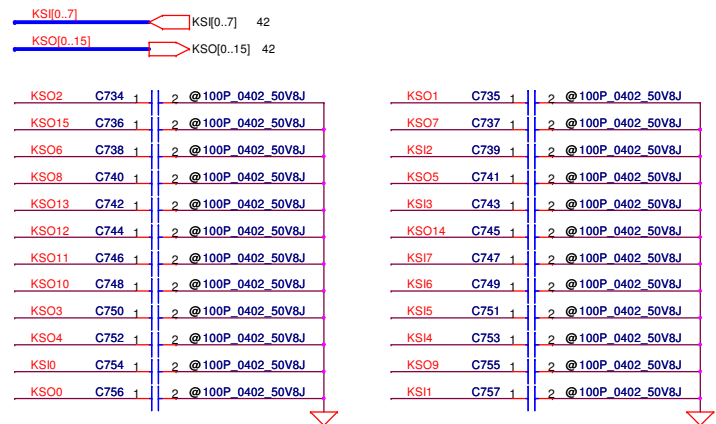


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	
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Size		Document Number		Rev	
Custom		QIYQ2 LA6884P		1.0	
Date		Wednesday, May 11, 2011		Sheet 41 of 60	

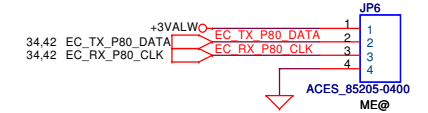


Security Classification		Compal Secret Data		Compal Electronics, Inc. BIOS & EC I/O Port					
Issued Date		2010/11/30	Deciphered Date				2011/08		
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						Size	Document Number		Rev
						Custom	QIQY2 LA6884P		1.0
Date:		Wednesday, May 11, 2011		Sheet	42 of 60				

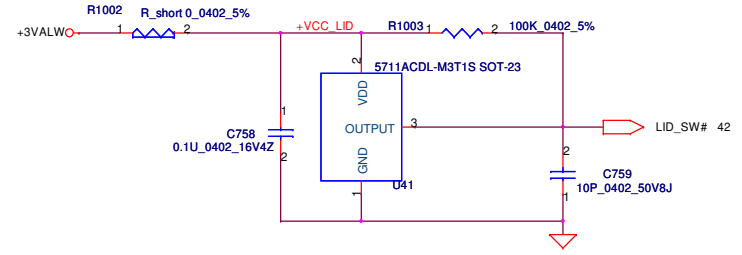
INT_KBD Conn.



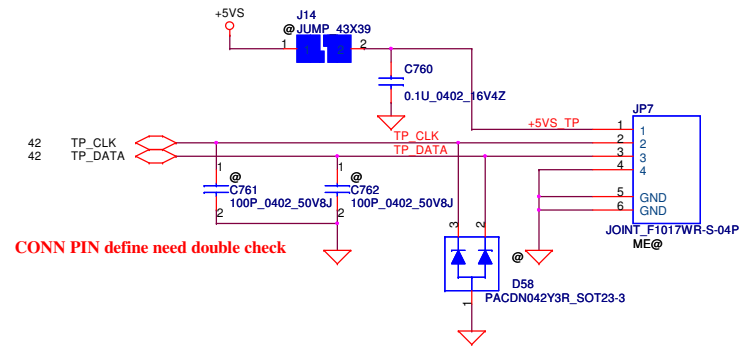
EC DEBUG PORT



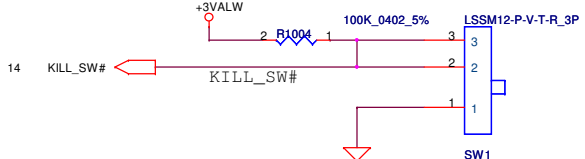
Lid Switch



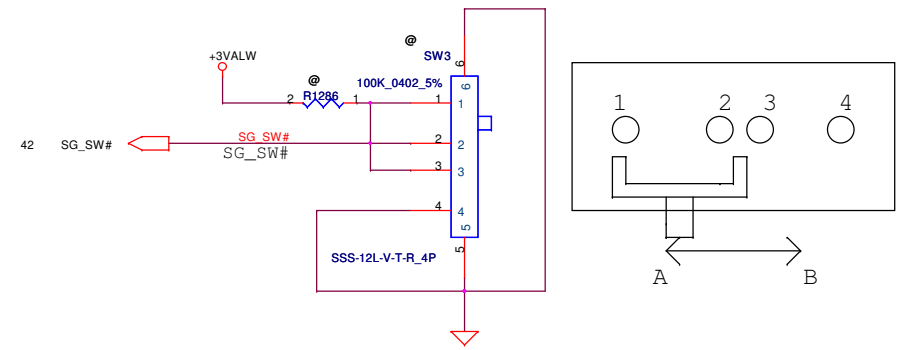
To TP/B Conn.



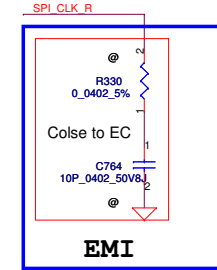
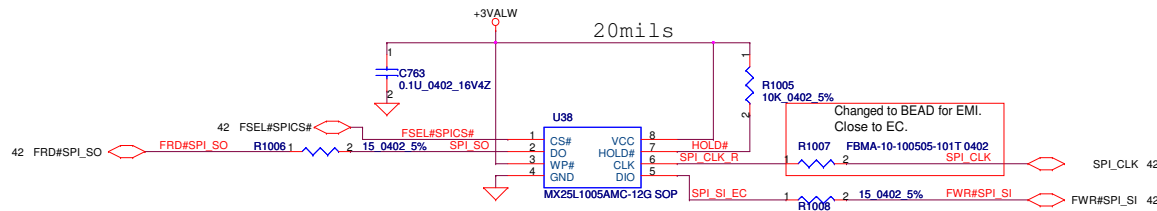
Kill Switch



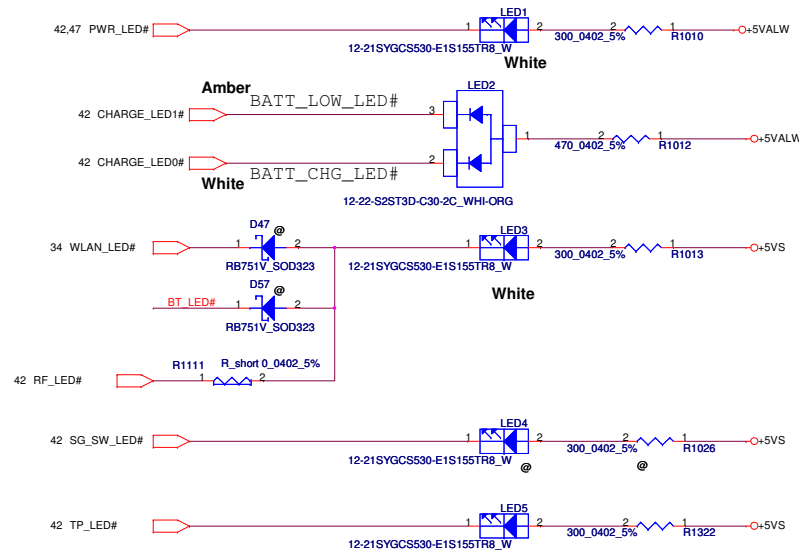
Kill	
STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON



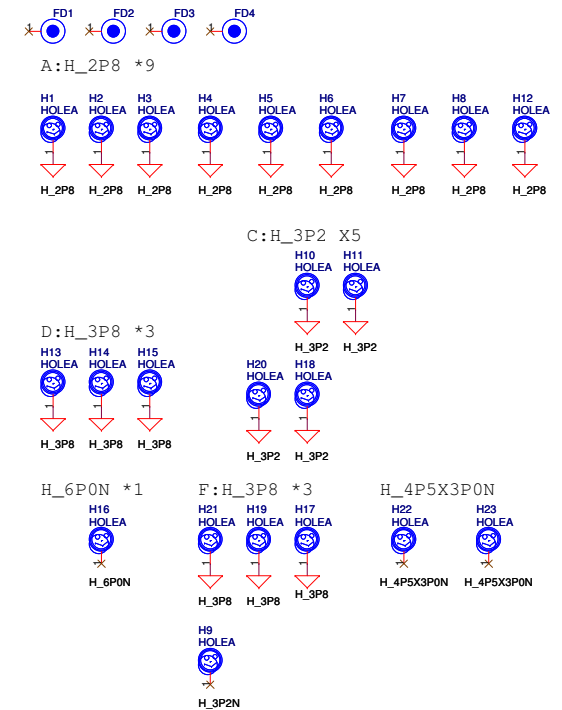
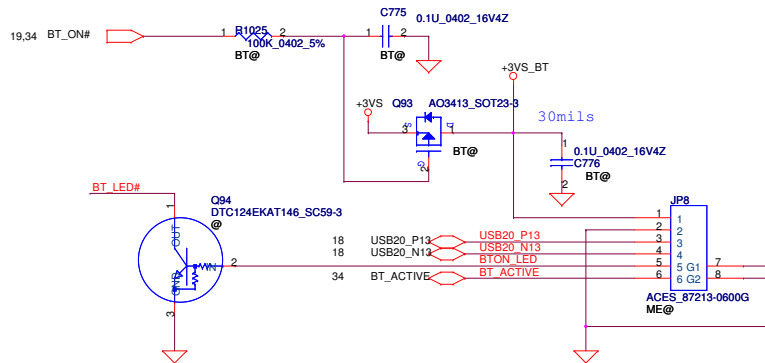
FOR EC 128KB SPI ROM
(150mil PACKAGE)
P/N : SA00002C100



LED

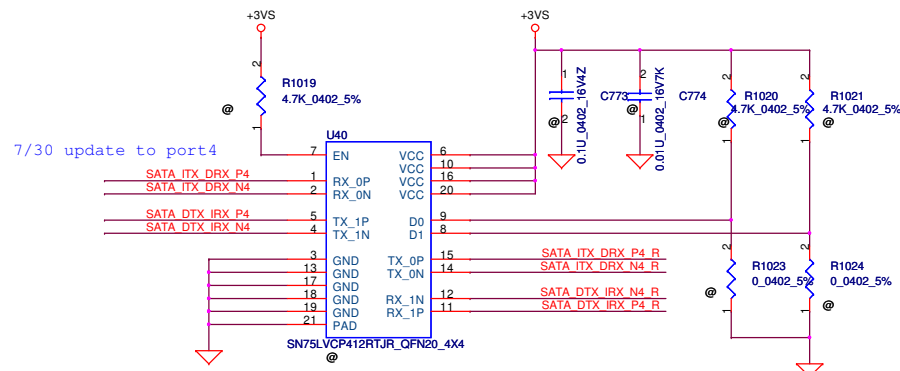
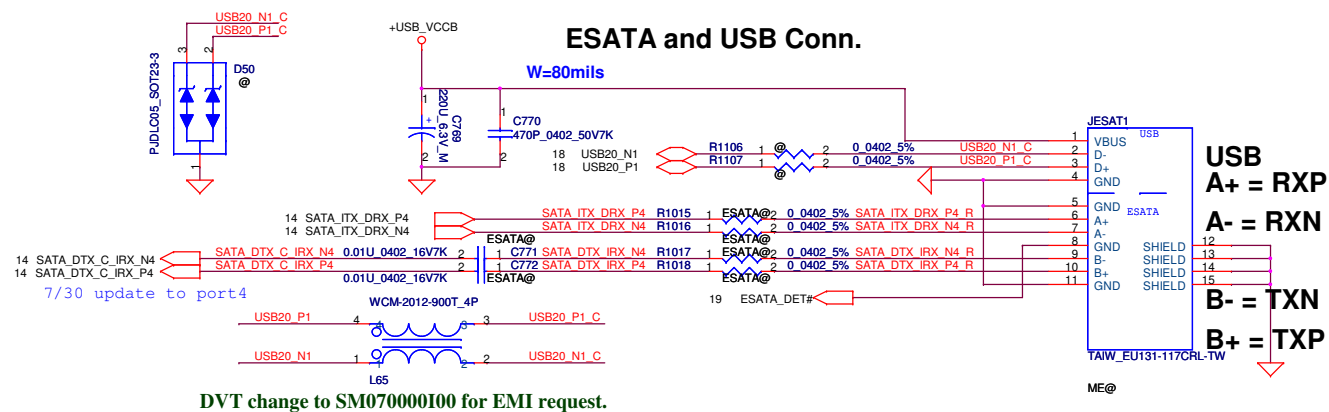
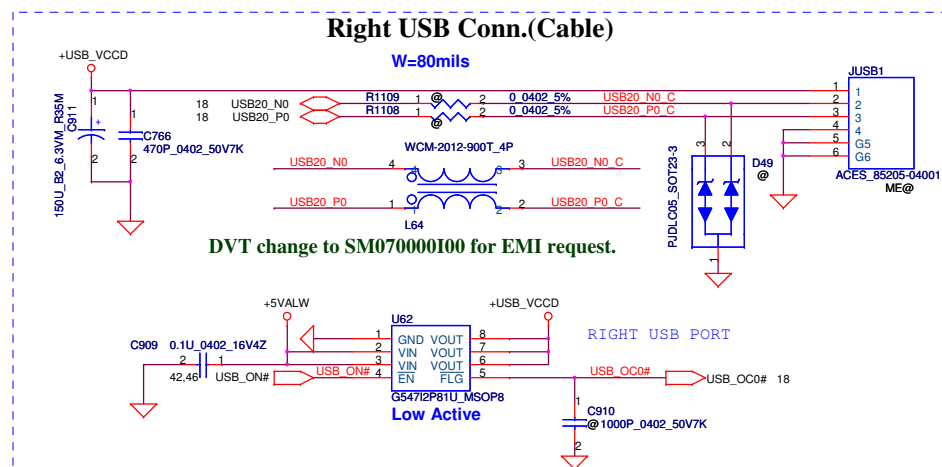


BT MODULE CONN



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/11/30		Deciphered Date		2011/08		Title	
										LED/EC SPI ROM/BT	
										Size B Document Number	
										QIQY2 LA6884P	
										Rev 1.0	
										Date: Wednesday, May 11, 2011	
										Sheet 44 of 60	

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Issued Date	2010/11/30	Deciphered Date	2011/08	Title USB ports/E-SATA		
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				Date:	Wednesday, May 11, 2011	Sheet 45 of 60

Power Button

TOP Side

Bottom Side

ON/OFFBTN#

ON/OFF# 42

51_ON# 49

DAN202UT106_SC70-3

10/02 Change to SC600000B00.

42,52 EC_ON

EC_ON

R1112 10K_0402_5%

2N7002_SOT23-3

Q95

3V3VALW

R1118 100K_0402_5%

NOVO# 42

51_ON# 49

NOVO_BTN#

DAN202UT106_SC70-3

10/02 Change to SC600000B00.

Diagram illustrating the connection of the D54 P/SOT24C 3P C/A SOT-23 component to the ACES_87151-1207G component.

The diagram shows the following connections:

- Power Supply:** +5VALW and +5VS are connected to the board.
- LEDs:** CAPS_LED#, NUM_LED#, and HDD_LED# are connected to the board.
- Buttons:** NOVO_BTN# and ON/OFFBTN# are connected to the board.
- LEDs:** PWR_LED# is connected to the board.
- Connector JP13:** The connector is connected to the board.
- Component D54:** The component is connected to the NOVO_BTN# and ON/OFFBTN# signals.
- Component ACES_87151-1207G:** The component is connected to the ME@ signal.

The diagram is labeled with "9/30 remove EC_SMB".

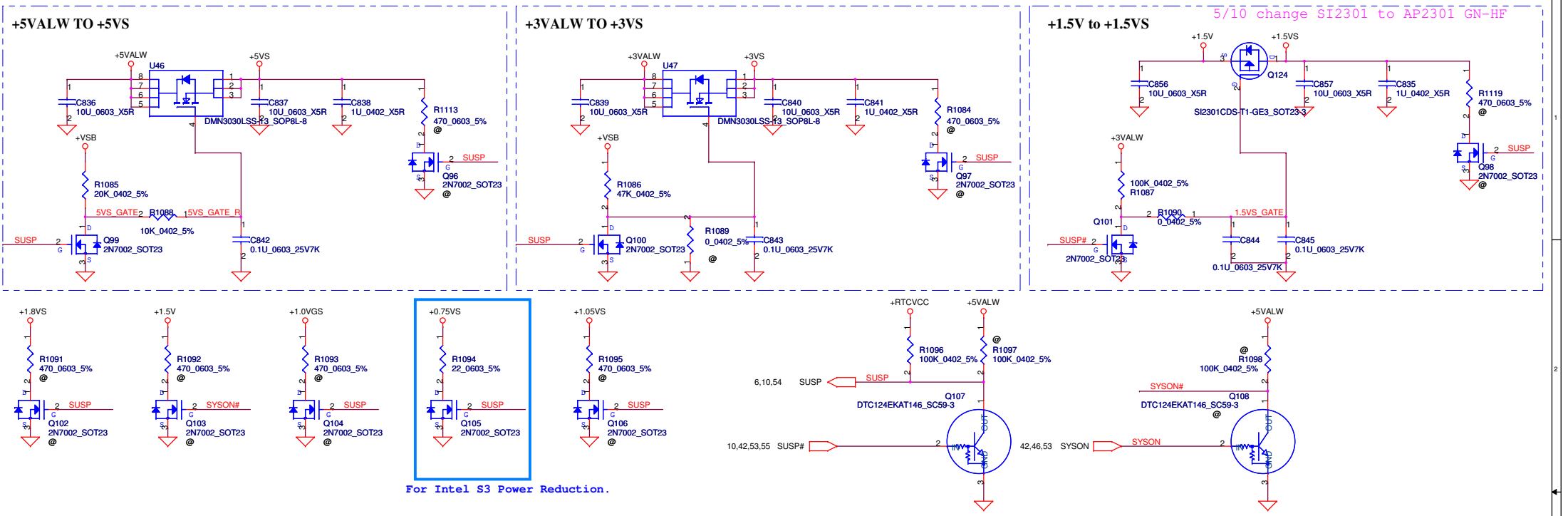
DVT, R1117 change to SM01000CY00 for EMI request.

The diagram shows a portion of the ACES_85201-08051 ME@ board. Key components and connections include:

- ESB_INT** (pin 42) connected to **ESB_INT R** (pin 1).
- ESB_CLK** (pin 42) connected to **ESB CLK R** (pin 3).
- ESB_DAT** (pin 42) connected to **ESB DAT R** (pin 4).
- ESB_RST#** (pin 42) connected to **ESB_RST#** (pin 7).
- R1114** (R_short 0_0402_5%) connected to **ESB_INT R** (pin 1).
- R1117** (R_short 0_0402_5%) connected to **ESB_CLK R** (pin 3).
- R1116** (R_short 0_0402_5%) connected to **ESB_RST#** (pin 7).
- C929** (0.1u_0402_10V6K) connected to **ESB_INT R** (pin 1).
- C958** (33P_0402_50V8J) connected to **ESB_RST#** (pin 7).
- JP9** (pin 1) connected to **ESB_INT R** (pin 1).
- JP9** (pin 2) connected to **ESB_CLK R** (pin 3).
- JP9** (pin 3) connected to **ESB_DAT R** (pin 4).
- JP9** (pin 4) connected to **ESB_RST#** (pin 7).
- JP9** (pin 5) connected to **ESB_RST#** (pin 7).
- JP9** (pin 6) connected to **ESB_RST#** (pin 7).
- JP9** (pin 7) connected to **ESB_RST#** (pin 7).
- JP9** (pin 8) connected to **ESB_RST#** (pin 7).
- JP9** (pin 9) connected to **ESB_RST#** (pin 7).
- JP9** (pin 10) connected to **ESB_RST#** (pin 7).

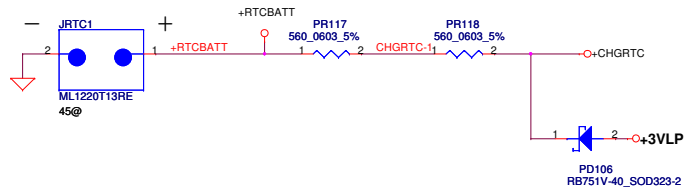
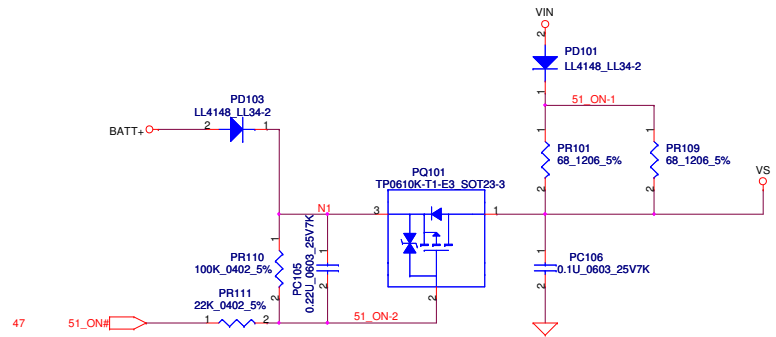
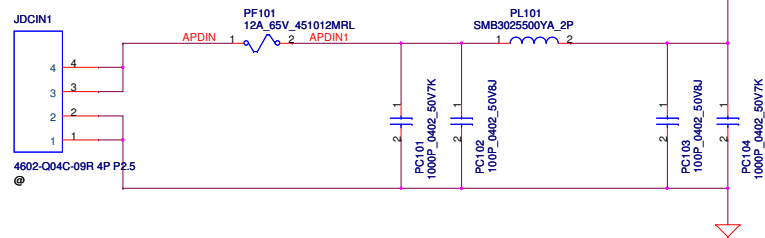
[illegible]

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								Size	Document Number						Rev
								Custom	QIQY2 LA6884P						1.0
								Date:	Wednesday, May 11, 2011			Sheet	47	of	60

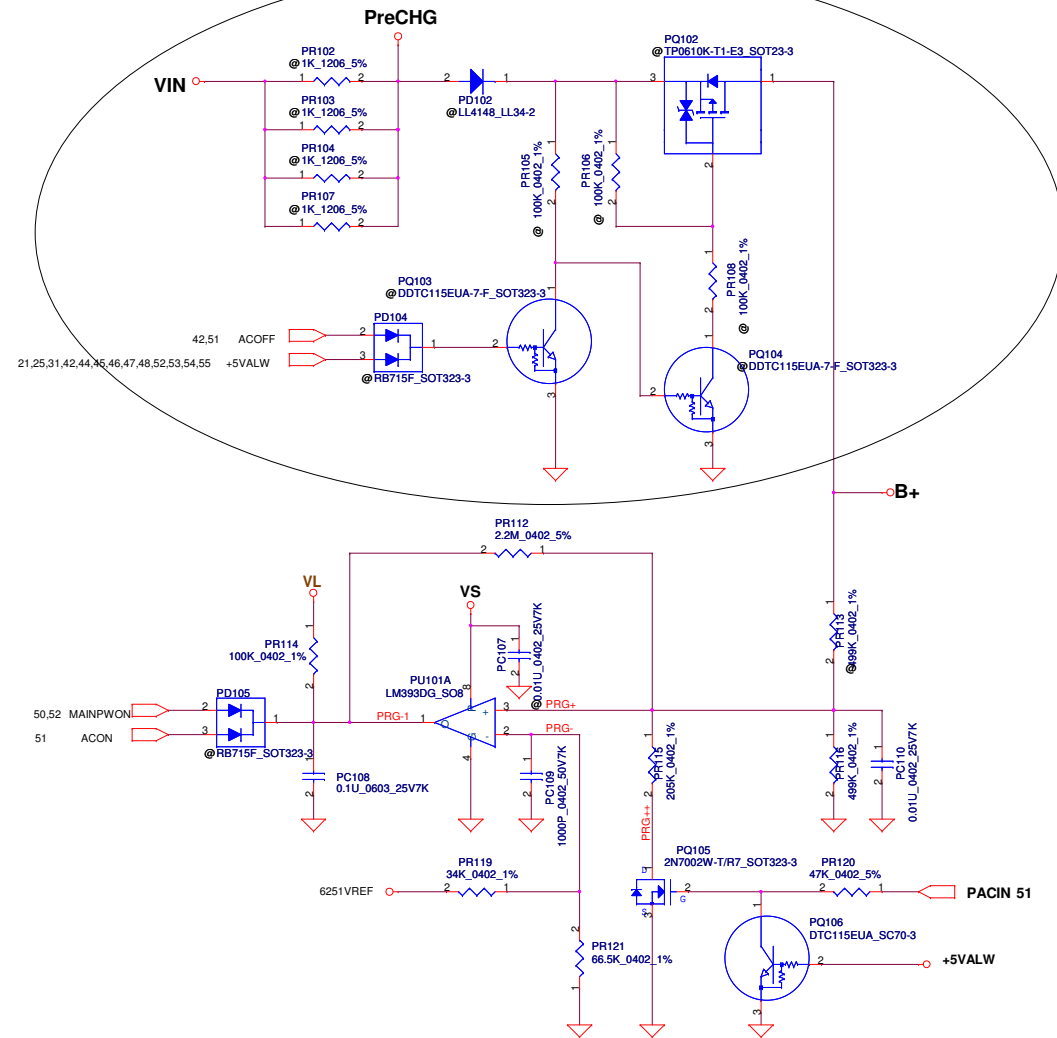


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Issued Date		2010/11/30	Deciphered Date	2011/08	Title
					DC Interface
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					Document Number QIQY2 LA6884P
					Rev 1.0
					Date: Wednesday, May 11, 2011
					Sheet 48 of 60

DC030006J00



Precharge detector 15.97V/14.84V FOR ADAPTOR



ACIN

Precharge detector

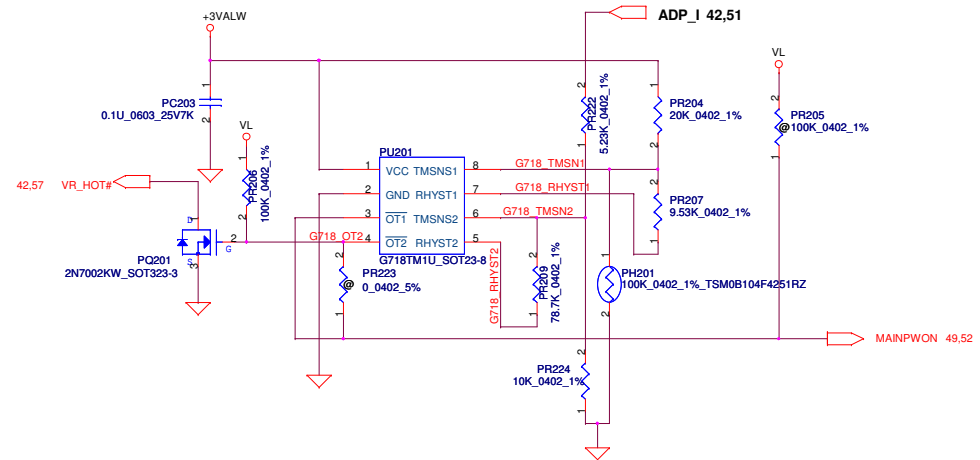
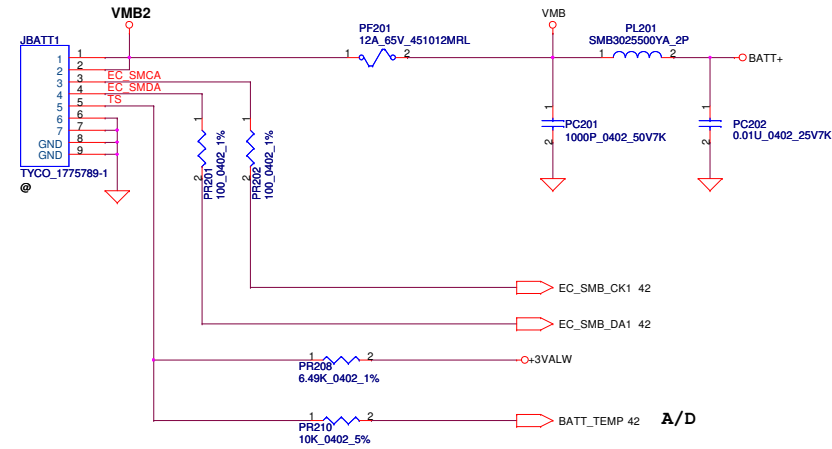
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

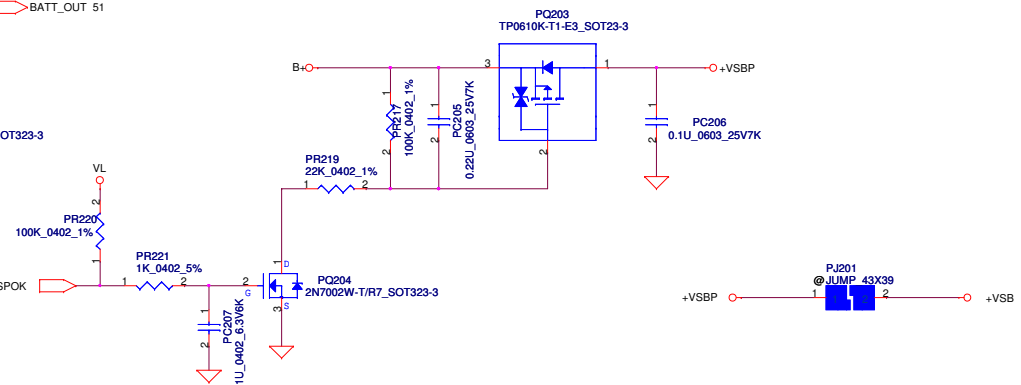
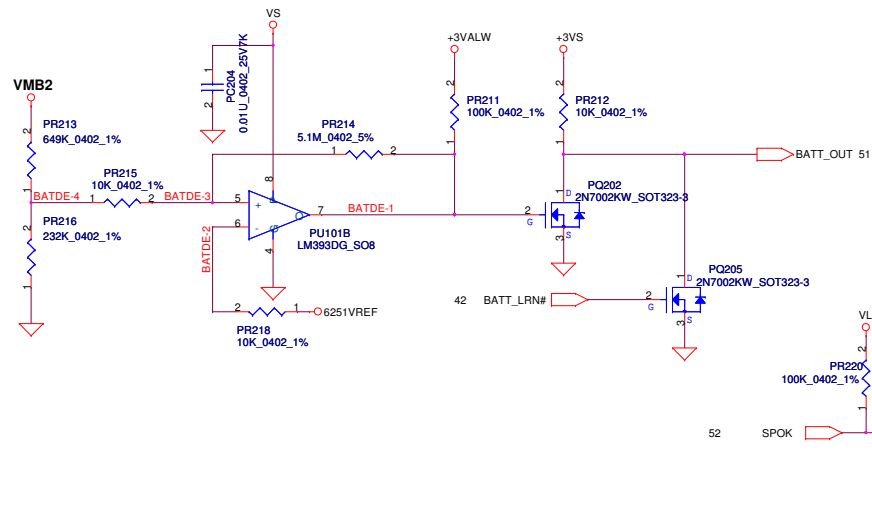
Precharge detector

	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

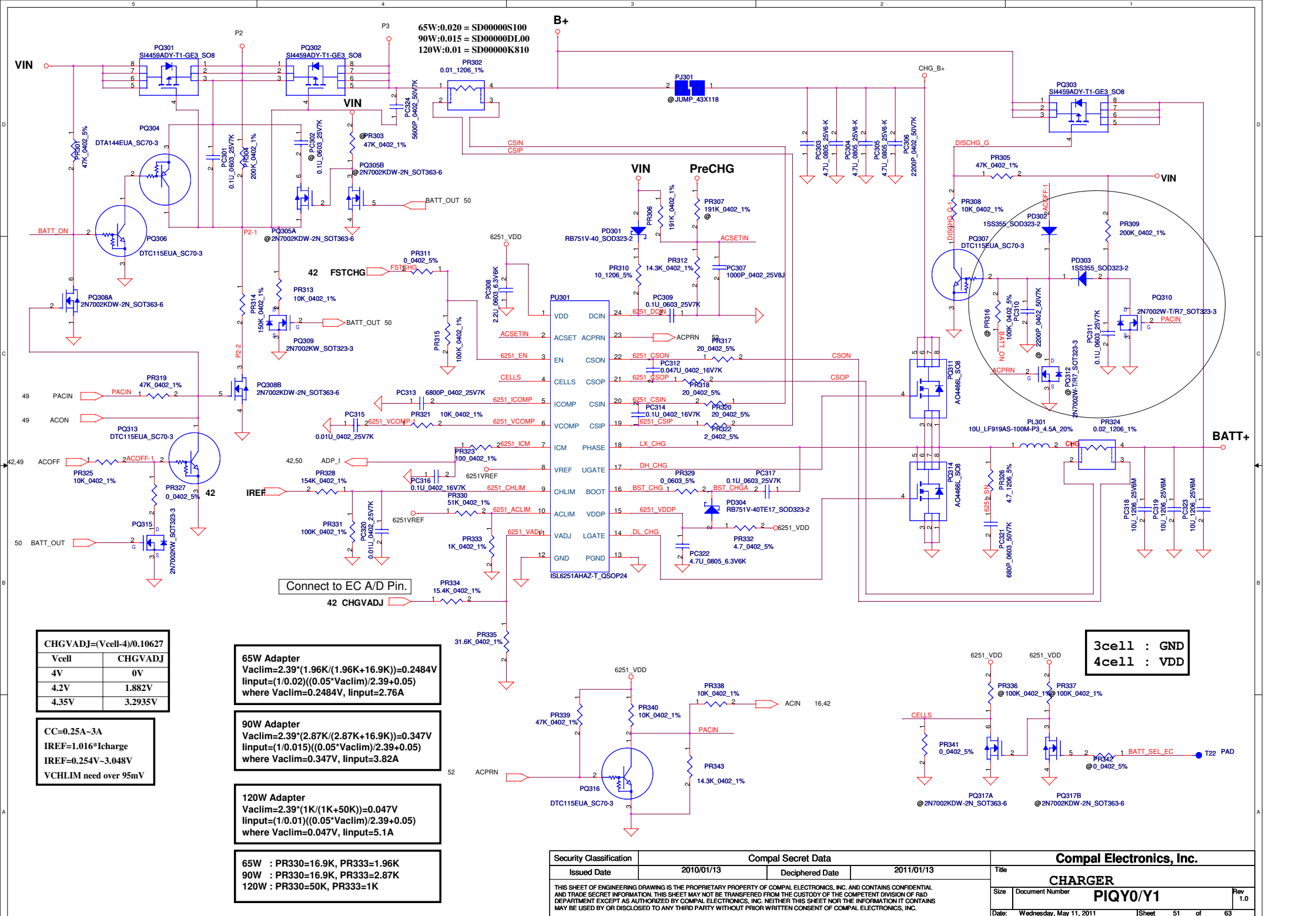
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title PWR DCIN / Vin Detector /Pre-charge	
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				Date Wednesday, May 11, 2011	Rev 1.0
				Sheet 49	of 63



PR222
90W : 6.65K ohm
120W : 5.23K ohm



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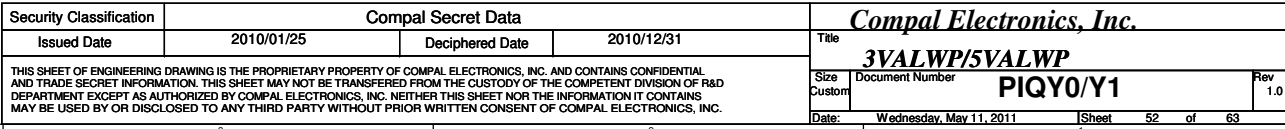
EC_ON

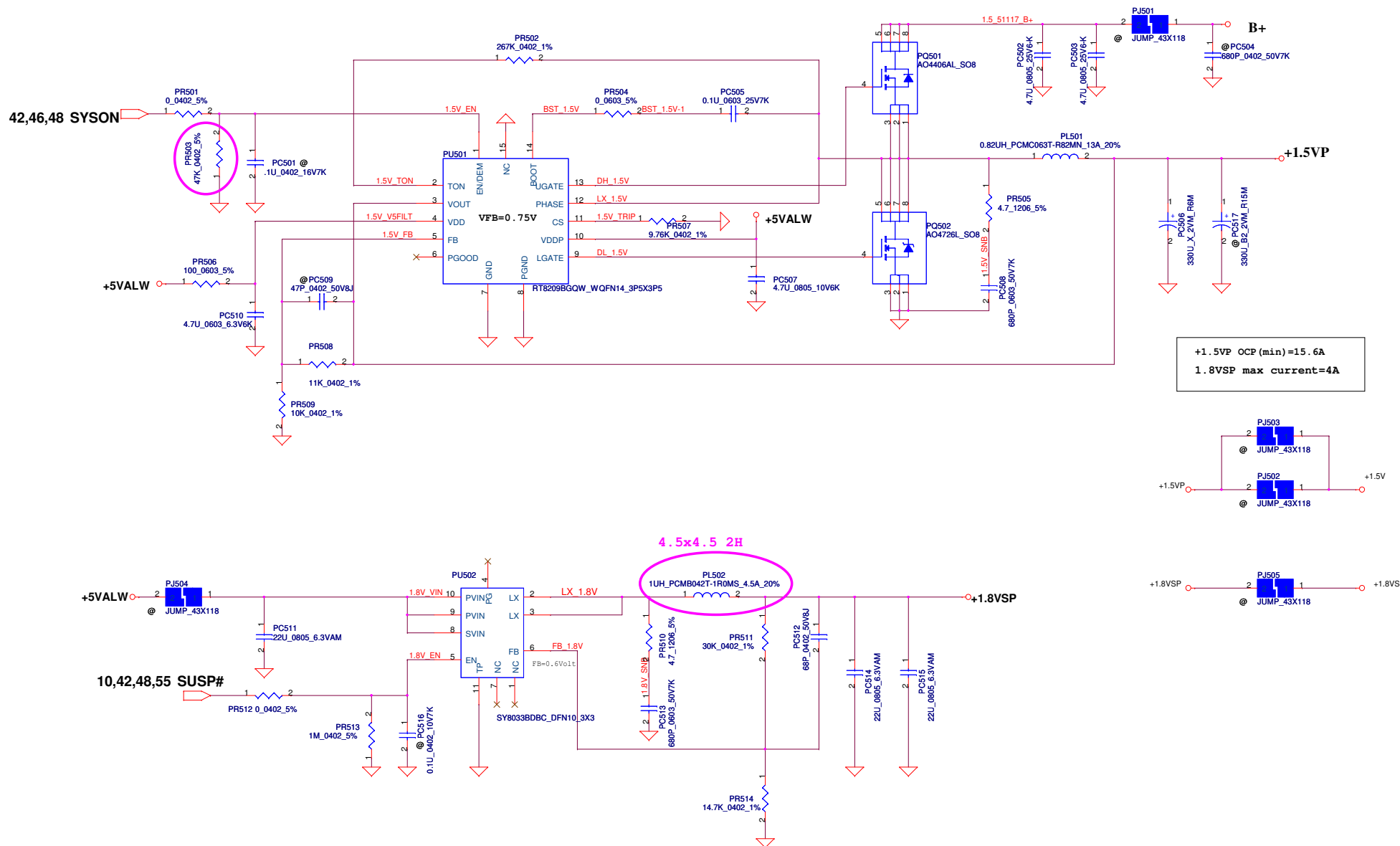
402nF

402nF

220uF

DTC115EUA_SC70-3





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				Customer	Rev 1.0
				Date:	Wednesday, May 11, 2011
				Sheet	53 of 63

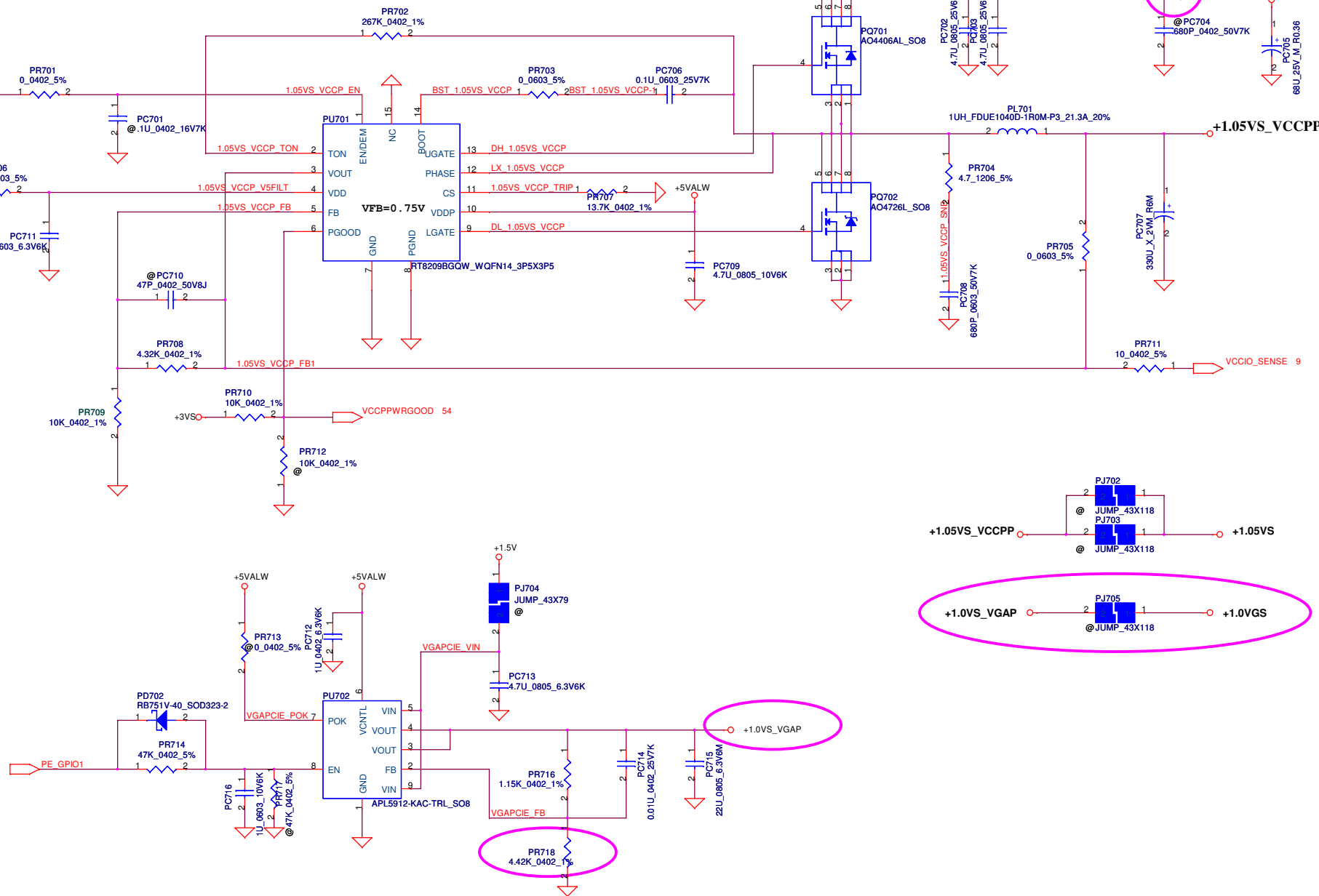


Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> PWR +VCCSAP+0.75VSP		
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PQI90/Y1	
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					PQI90/Y1	1.0
				Date:	Wednesday, May 11, 2011	Sheet 54 of 63

10,42,48,53 SUSP#

+5VALW

18,25,56 PE_GPIO1

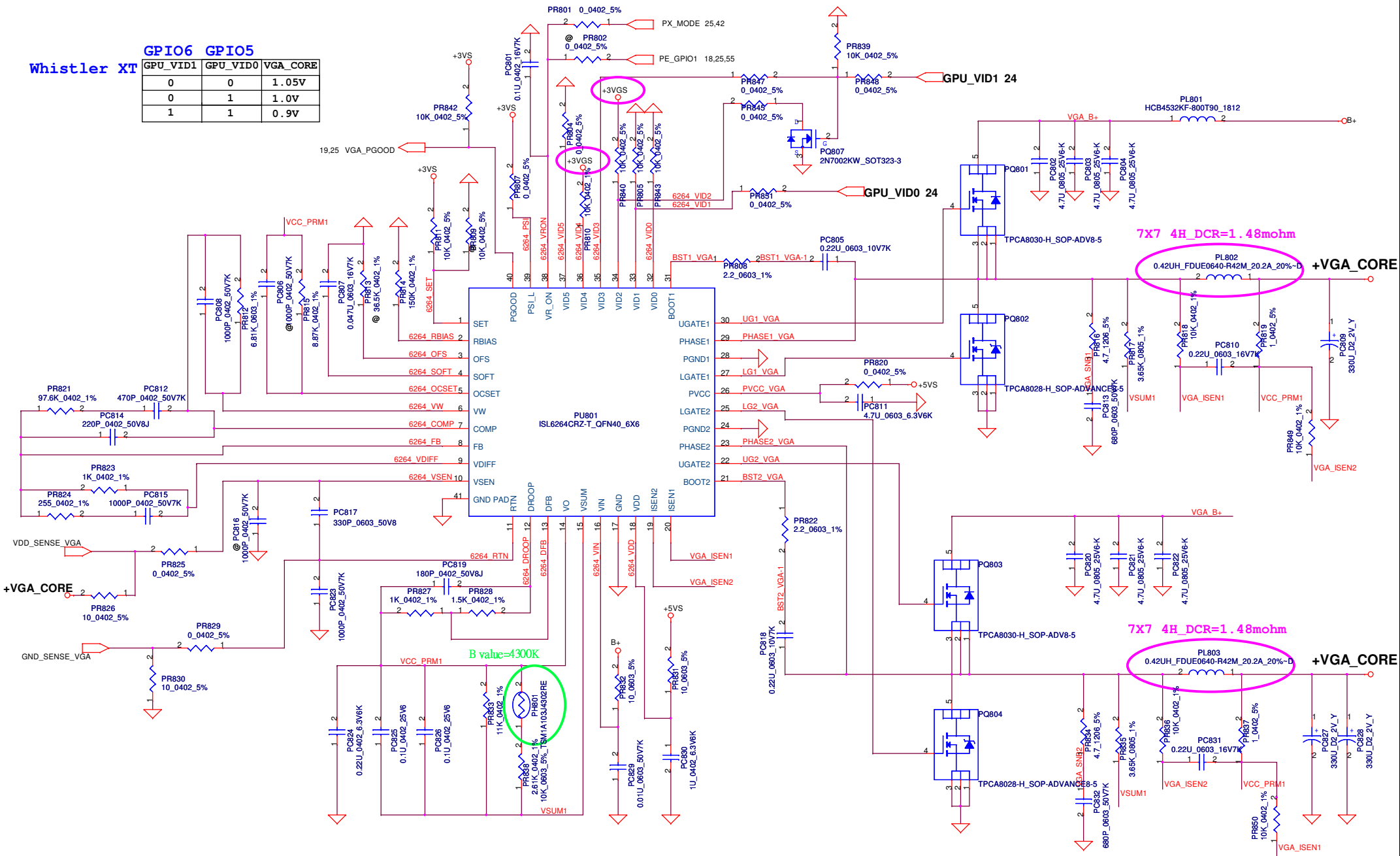


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR +1.05VS VCCPP/1.0VS VGA
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				Date: Wednesday, May 11, 2011	Rev 1.0
				Sheet 55 of 63	

Whistler XT

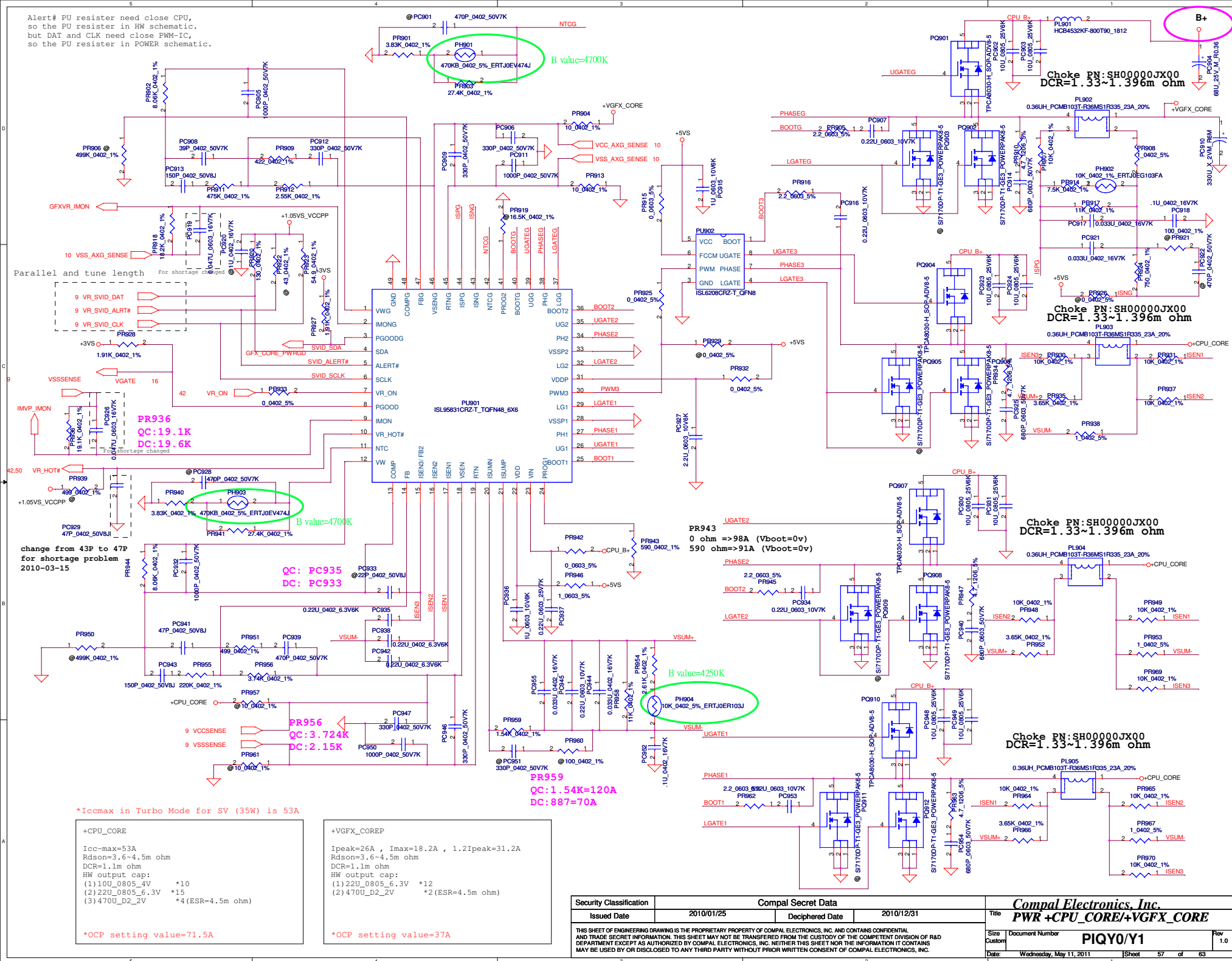
GPIO6 GPIO5

GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.05V
0	1	1.0V
1	1	0.9V



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/12/12	Deciphered Date	2007/12/12	Title	Power-VGA_CORE
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				Custom	PIQY0/Y1
				Rev	1.0
Date:		Wednesday, May 11, 2011		Sheet	56 of 63

Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.



Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> PWR +CPU_CORE/+VGFY_CORE		
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title		
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				Custom	PIQY0/Y1	1.0
				Date:	Wednesday, May 11, 2011	Sheet 57 of 63

Item	Reason for change	PG#	Modify List	Date	Phase
1	Disable Pre-charge		PR102, PR103, PR104, PR107, PD102, PD104, PQ102, PQ103, PQ104		
2	Back to Back MOS change		PQ301, PQ302, PQ303		
3	Battery Learning function		PQ205		
4					
5					
6					
7					
8					
9					
10					
11					
12					
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 QIQY2 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	
					SDV
1		P23	Change U8 to SA00004R500	Customer need to change	
2		P23	Del C998/ C1067/ C343/ C339/ C382/ C376/ C377/ R692	For VGA function	
3		P23	Change Q69 to Q75, Q68 to Q76, U56 to U62, U60 to U64, Q87 to Q109, Q86 to Q110, C732 to C777, U59 to U66, R872 to R890, U37 to U41	For VGA function	
4		P42	Del R994/ R999/ D46/ Q91	For EC function	
5		P15	Del PJP2/ R67/ R257/ R261	For PCH function	
6		P23	Del C386/ C732/ R1400/ R1360	For VGA function	
7		P33	Del R354/ R3461/ R1372/ R1373 Del R185/ R434/ Q84/ R1022/ Q92/ CV253-CV260/ Q115/R1144/ R1143/ L67/ R997/ R1321	For HDMI function	
8		P44	BT_OFF# change to BT_ON#	For BT function	
9		P35	EC_PME# change to LAN_WAKE#	For LAN wake funcion	
10		P32	CMOS_OFF# change to CMOS_ON#	For CMOS function	
11		P45	U11 from SB000007010 change to SB548000210	For +1.5VGS function	
12		P32	D31~D35 from +5VS change to +CRT_VCC_CONN	For CRT function	
13		P15	U4 from SA00004EEJ0 change to SA00004EEV0	PCH from rev.B2 change to rev.B3	
14		P14	R133 from 0 ohm change to 33 ohm	For BIOS ROM function	SIT
1		P23	Add C69 22Uf_0805 cap for +BIF_VDDC.	For vendor feedback	
2		P23	Reserve R613 & R614 to pull up +3VS.	For VGA function	
3		P23	Change 0 ohm to R_short --- R10/R1002/R1014/R1029/R109/ R11/R1111/R1114/R1116/R1280/R1281/R1282/R1283/R1285/ R130/R1320/R1336/R1342/R1323/R14/R181R19/R190/R193/R196/ R198/R207/R22/R222/R254R256/R258/R26/R260/R263/R265/R269 /R270/R272R273/R274/R276/R277/R278/R281/R282/R283/R284/ R285/R286/R288/R289/R293/R295/R302/R303/R313/R40/R432/ R52/R53/R668/R710/R824/R825/R880/R882/R885/R886/R891/ R922/R941/R969/R973/R993/R996.	For IO/ PCH/ VGA function	
4		P45	U39/ U62 /U44 from SA000039E00 change to SA00003TV00.	For USB function	
5		P18	Del net name PCH_GPI051 connect to RP1 pin2.	For VGA function	
6		P25	C351 from 0.1uF_0603 change to 0.047uF_0402.	For VGA function	
7		P10	ADD PJP2 jump.	For PCH function	
8		P43	U41 from SA000031C00 change to SA00001TC00.	For LID function	
9		P25	R352 from 0 ohm change to 330K ohm.	For VGA function	
10		P25	Add C343 & C346 for reserve.	For VGA function	
11		P25	Q121 from SBX01240010 change to SB000008J10.	For VGA function	

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