LCFC Confidential

ACLUA M/B Schematics Document

Intel Haswell/Broadwell U-Processor with DDRIIIL + NV (N15V-GM/N15S-GT) GPU

2013-12-26

REV:0.3

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title *Cover Page*		LCFC
Size Custom	Document Number *ACLUA*	Rev 1.0
Date: Thursday, December 26, 2013	Sheet 1 of 59	

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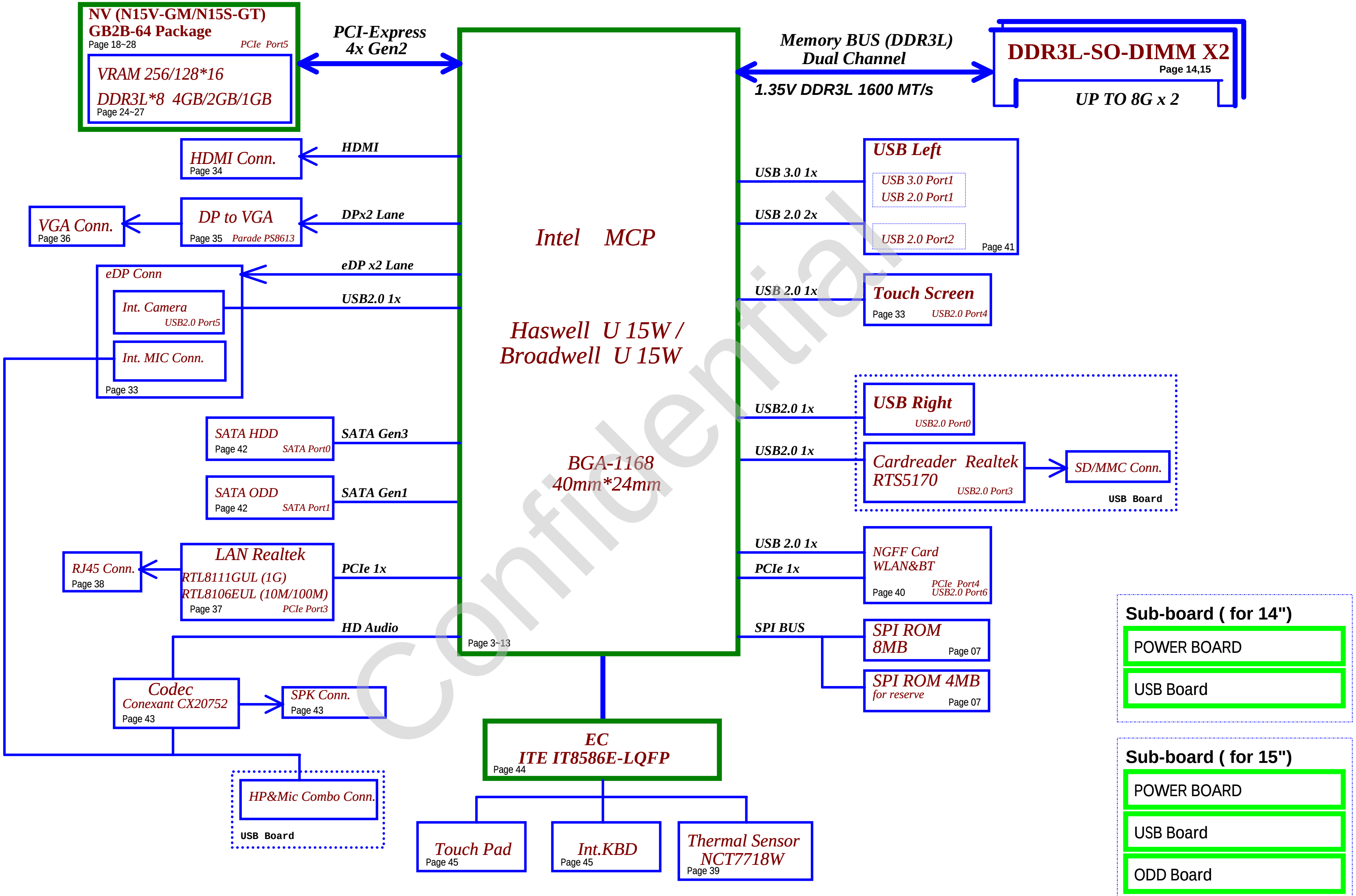

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Title
Block Diagram

Size: Custom
Document Number: ACLUA
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 2 of 59

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.35VS +1.05VS +0.675VS CPU_CORE +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0 EHCI1		USB 3.0 XHCI	
0	USB Port (Right Side)		
1	USB Port1 (Left Side)	1	USB Port1 (Left Side)
2	USB Port2 (Left Side)	2	
3	Cardreader	3	
4	TOUCH PANEL	4	
5	Camera		
6	NGFF(WLAN)		
7			

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
100M@	100M LAN Part
GIGA@	GIGA LAN Part
OPT@	Discrete GPU SKU part
N15SGT@	For N15S-GT GPU part
N15VGM@	For N15V-GM part
GC6@	GC62.0 support part
RANKA@	For VRAM RankA part
RANKB@	For VRAM RankB part
UMA@	UMA SKU part
TS@	For support touch panel sku part
AOAC@	AOAC support part
ME@	ME part(connector, hole)

PCIE PORT LIST

Port	Device
1	
2	
3	LAN
4	WLAN
5	Discrete GPU
6	

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

EC SM Bus1 address

Device	
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor NCT7718W	1001_100xb
VGA	0x41(default)
PCH	need to update

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

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Title
Notes List

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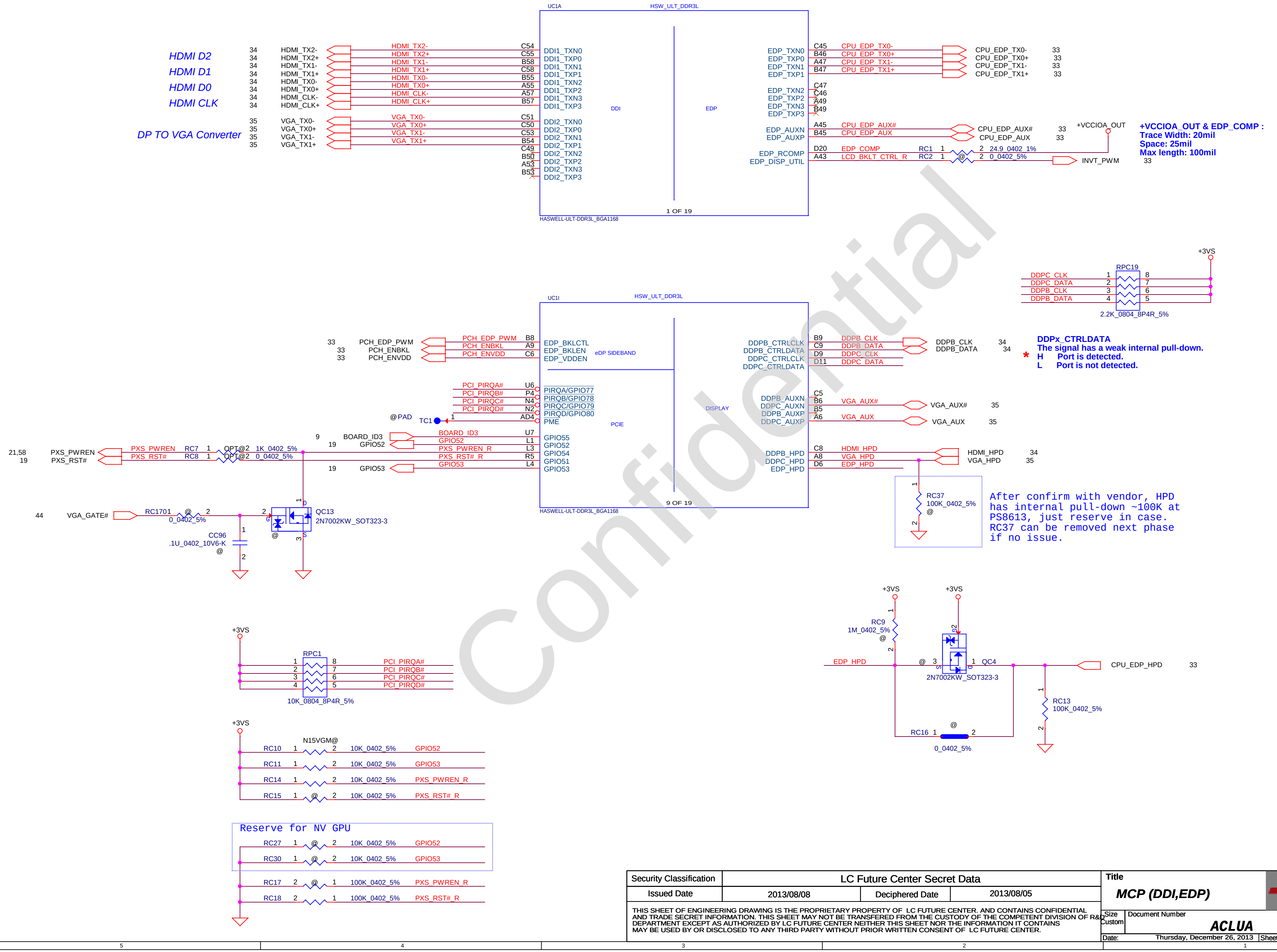
Document Number: ACLUA
Rev: 1.0
Date: Thursday, December 26, 2013



+VCCIOA_OUT & EDP_COMP :
Trace Width: 20mil
Space: 25mil
Max length: 100mil

DDPx_CTRLDATA
The signal has a weak internal pull-down.
*** H Port is detected.**
L Port is not detected.

After confirm with vendor, HPD has internal pull-down ~100K at PS8613, just reserve in case. RC37 can be removed next phase if no issue.

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Title
MCP (DDI,EDP)

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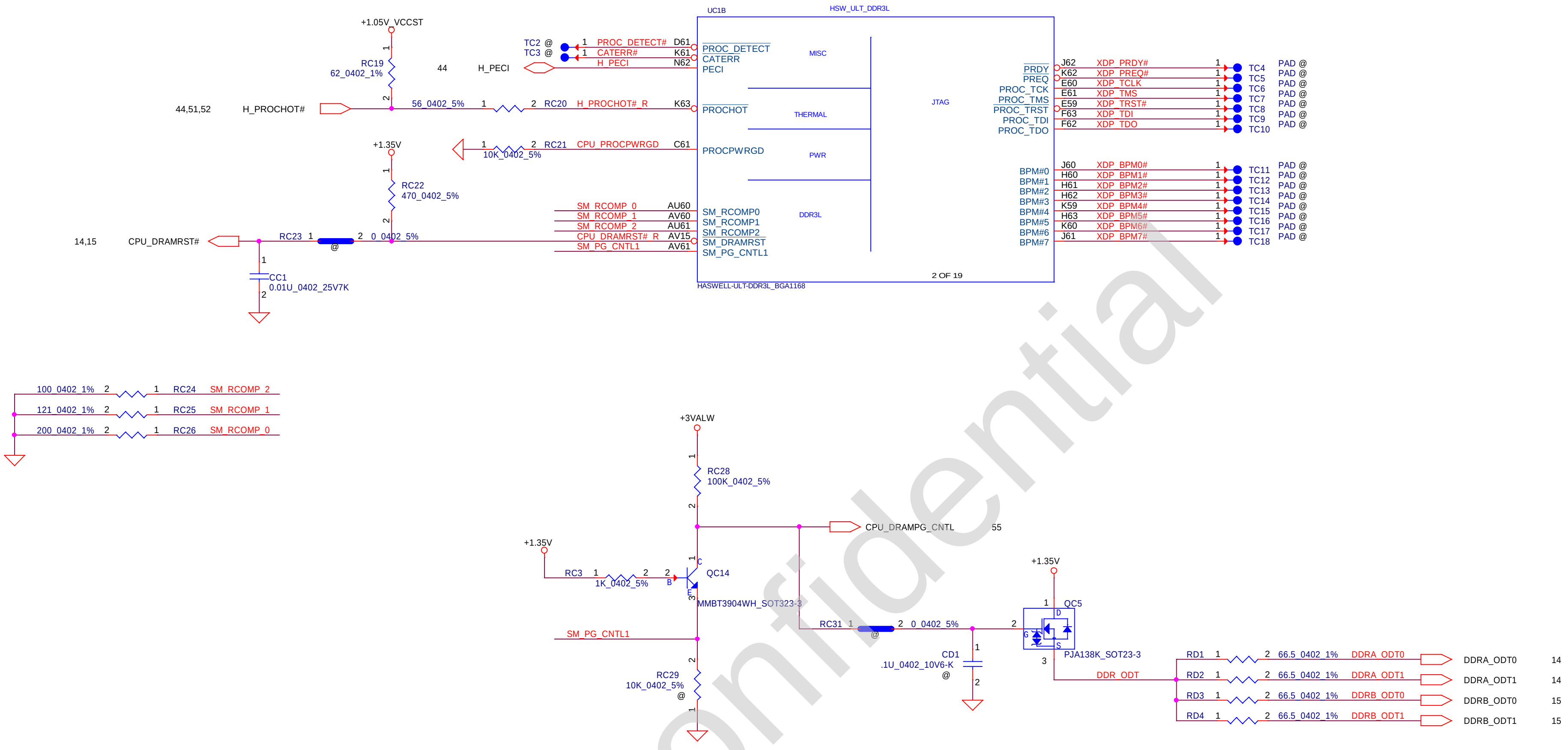
Size Custom
Document Number **ACLUA**
Rev 1.0
Date: Thursday, December 26, 2013 Sheet 4 of 59



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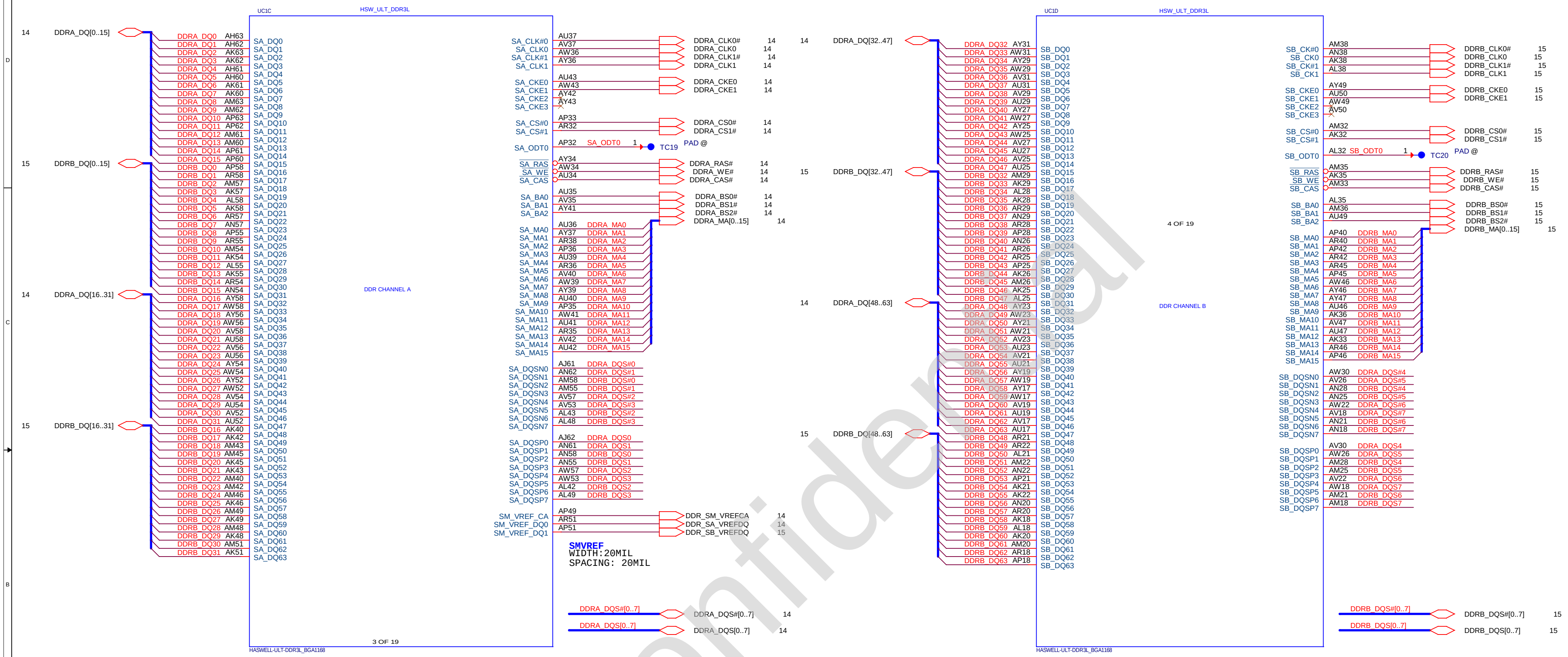
Title
MCP (MISC,THERMAL,JATG)

Size	Document Number	Rev
Custom	ACLUA	1.0

Date: Thursday, December 26, 2013 Sheet 5 of 59



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Title
MCP (DDR3L)

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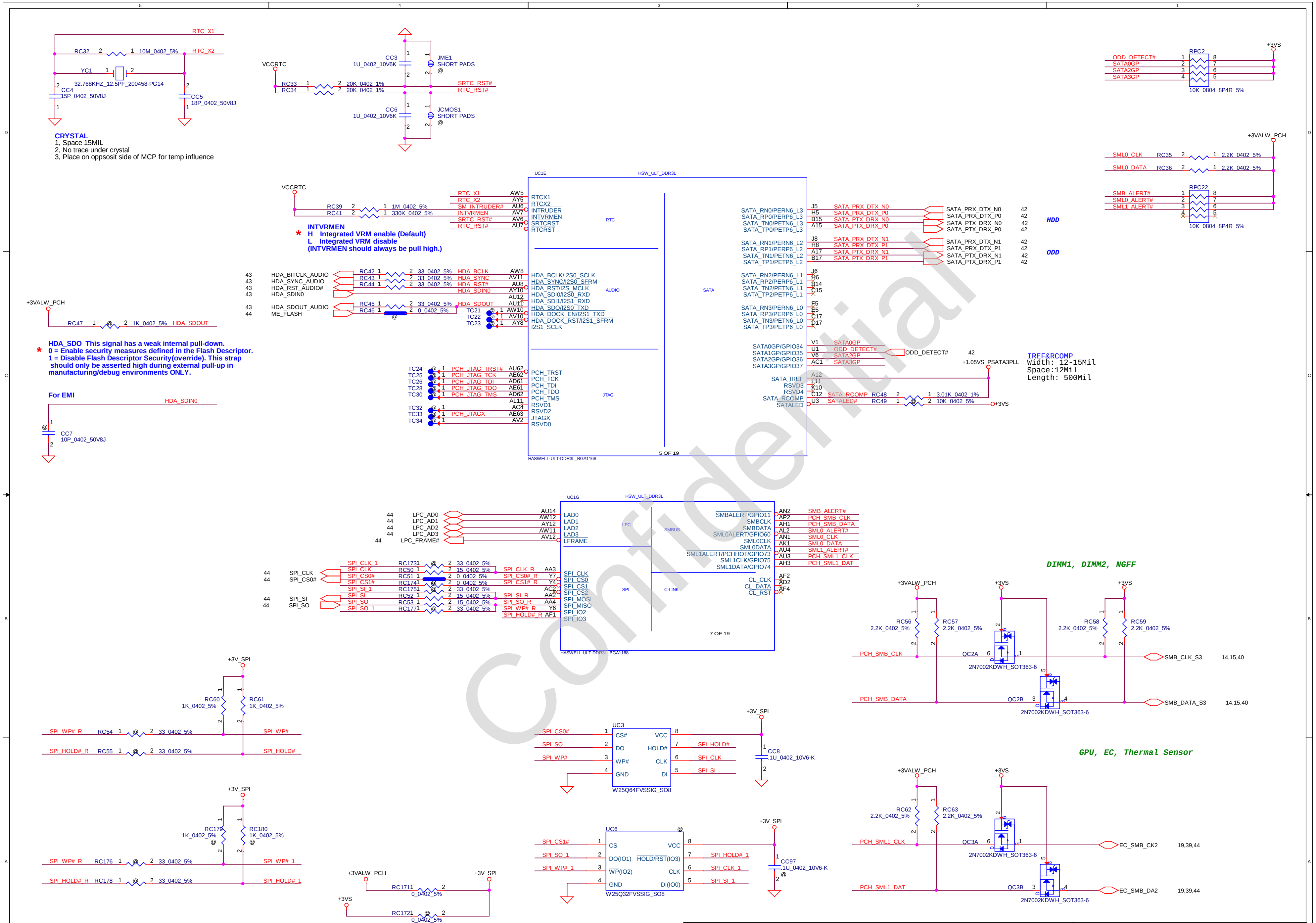
Document Number: **ACLUA**
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 6 of 59



RTC_X1
RC32 2 1 10M_0402_5% RTC_X2
YC1 1 2
32.768KHZ_12.5PF_200458-PG14
CC4 15P_0402_50V8J
CC5 18P_0402_50V8J
CC3 1U_0402_10V6K
JME1 SHORT PADS
VCCRTC
RC33 1 2 20K_0402_1% SRTC_RST#
RC34 1 2 20K_0402_1% RTC_RST#
CC6 1U_0402_10V6K
JCMOS1 SHORT PADS
UC1E
HSW_ULT_DDR3L
RC39 2 1 1M_0402_5%
RC41 2 1 330K_0402_5%
RTC_X1 AW5 RTCX1
RTC_X2 AY5 RTCX2
SM_INTRUDER# AU6 INTRUDER
INTVRMEN AV7 INTVRMEN
SRTC_RST# AV6 SRTCRST
RTC_RST# AU7 RTCRST
RTC
43 HDA_BITCLK_AUDIO
43 HDA_SYNC_AUDIO
43 HDA_RST_AUDIO#
43 HDA_SDIN0
43 HDA_SDOUT_AUDIO
44 ME_FLASH
RC42 33_0402_5% HDA_BCLK AW8 HDA_BCLK/I2S0_SCLK
RC43 33_0402_5% HDA_SYNC AV11 HDA_SYNC/I2S0_SFRM
RC44 33_0402_5% HDA_RST# AU8 HDA_RST/I2S_MCLK
HDA_SDIN0 AY10 HDA_SDI0/I2S0_RXD
AU12 HDA_SDI1/I2S1_RXD
RC45 33_0402_5% HDA_SDOUT AU11 HDA_SDO/I2S0_TXD
RC46 0_0402_5%
TC21 AW10 HDA_DOCK_EN/I2S1_TXD
TC22 AV10 HDA_DOCK_RST/I2S1_SFRM
TC23 AY8 I2S1_SCLK
AUDIO
+3VALW_PCH
RC47 1 @ 2 1K_0402_5% HDA_SDOUT
TC24 PCH_JTAG_TRST# AU62 PCH_TRST
TC25 PCH_JTAG_TCK AE62 PCH_TCK
TC26 PCH_JTAG_TDI AD61 PCH_TDI
TC28 PCH_JTAG_TDO AE61 PCH_TDO
TC30 PCH_JTAG_TMS AD62 PCH_TMS
AL11 RSVD1
TC32 AC4 RSVD2
TC33 PCH_JTAGX AE63 JTAGX
TC34 AV2 RSVD0
JTAG
5 OF 19
HASWELL-ULT-DDR3L_BGA1168
HDA_SDIN0
CC7 10P_0402_50V8J
SATA
SATA_RN0/PERN6_L3 J5 SATA_PRX_DTX_N0
SATA_RP0/PERN6_L3 H5 SATA_PRX_DTX_P0
SATA_TN0/PETN6_L3 B15 SATA_PTX_DRX_N0
SATA_TP0/PETP6_L3 A15 SATA_PTX_DRX_P0
SATA_RN1/PERN6_L2 J8 SATA_PRX_DTX_N1
SATA_RP1/PERN6_L2 H8 SATA_PRX_DTX_P1
SATA_TN1/PETN6_L2 A17 SATA_PTX_DRX_N1
SATA_TP1/PETP6_L2 B17 SATA_PTX_DRX_P1
SATA_RN2/PERN6_L1 J6
SATA_RP2/PERN6_L1 H6
SATA_TN2/PETN6_L1 B14
SATA_TP2/PETP6_L1 C15
SATA_RN3/PERN6_L0 F5
SATA_RP3/PERN6_L0 E5
SATA_TN3/PETN6_L0 C17
SATA_TP3/PETP6_L0 D17
SATA_PRX_DTX_N0 42
SATA_PRX_DTX_P0 42
SATA_PTX_DRX_N0 42
SATA_PTX_DRX_P0 42
HDD
SATA_PRX_DTX_N1 42
SATA_PRX_DTX_P1 42
SATA_PTX_DRX_N1 42
SATA_PTX_DRX_P1 42
ODD
SATA0GP/GPIO34 V1 SATA0GP
SATA1GP/GPIO35 U1 ODD_DETECT# ODD_DETECT# 42
SATA2GP/GPIO36 V6 SATA2GP
SATA3GP/GPIO37 AC1 SATA3GP
+1.05VS_PSATA3PLL
SATA_IREF A12
RSVD3 L11
RSVD4 K10
SATA_RCOMP C12 SATA_RCOMP RC48 1 3.01K_0402_1%
SATALED U3 SATALED# RC49 1 @ 2 10K_0402_5% +3VS
ODD_DETECT# SATA0GP SATA2GP SATA3GP RPC2 10K_0804_8P4R_5%
+3VS
+3VALW_PCH
SML0_CLK RC35 2.2K_0402_5%
SML0_DATA RC36 2.2K_0402_5%
SMB_ALERT# SML0_ALERT# SML1_ALERT# RPC22 10K_0804_8P4R_5%
UC1G HSW_ULT_DDR3L
44 LPC_AD0 AU14 LAD0
44 LPC_AD1 AW12 LAD1
44 LPC_AD2 AY12 LAD2
44 LPC_AD3 AW11 LAD3
44 LPC_FRAME# AV12 LFRAME
LPC
SMBUS
SMBALERT/GPIO11 AN2 SMB_ALERT#
SMBCLK AP2 PCH_SMB_CLK
SMBDATA AH1 PCH_SMB_DATA
SML0ALERT/GPIO60 AL2 SML0_ALERT#
SML0CLK AN1 SML0_CLK
SML0DATA AK1 SML0_DATA
SML1ALERT/PCHHOT/GPIO73 AU4 SML1_ALERT#
SML1CLK/GPIO75 AU3 PCH_SML1_CLK
SML1DATA/GPIO74 AH3 PCH_SML1_DAT
CL_CLK AF2
CL_DATA AD2
CL_RST AF4
C-LINK
44 SPI_CLK
44 SPI_CS0#
44 SPI_SI
44 SPI_SO
SPI_CLK_1 RC1731 @ 33_0402_5%
SPI_CLK RC50 15_0402_5% SPI_CLK_R AA3 SPI_CLK
SPI_CS0# RC51 0_0402_5% SPI_CS0#_R Y7 SPI_CS0
SPI_CS1# RC1741 @ 0_0402_5% SPI_CS1#_R Y4 SPI_CS1
SPI_SI_1 RC1751 @ 33_0402_5% AC2 SPI_CS2
SPI_SI RC52 15_0402_5% SPI_SI_R AA2 SPI_MOSI
SPI_SO RC53 15_0402_5% SPI_SO_R AA4 SPI_MISO
SPI_SO_1 RC1771 @ 33_0402_5% SPI_WP#_R Y6 SPI_IO2
SPI_HOLD#_R AF1 SPI_IO3
SPI
7 OF 19
HASWELL-ULT-DDR3L_BGA1168
DIMM1, DIMM2, NGFF
+3VALW_PCH +3VS +3VS
RC56 2.2K_0402_5%
RC57 2.2K_0402_5%
RC58 2.2K_0402_5%
RC59 2.2K_0402_5%
PCH_SMB_CLK QC2A 2N7002KDWH_SOT363-6 SMB_CLK_S3 14,15,40
PCH_SMB_DATA QC2B 2N7002KDWH_SOT363-6 SMB_DATA_S3 14,15,40
+3V_SPI
RC60 1K_0402_5%
RC61 1K_0402_5%
SPI_WP#_R RC54 @ 33_0402_5% SPI_WP#
SPI_HOLD#_R RC55 @ 33_0402_5% SPI_HOLD#
UC3
SPI_CS0# 1 CS# VCC 8
SPI_SO 2 DO HOLD# 7 SPI_HOLD#
SPI_WP# 3 WP# CLK 6 SPI_CLK
4 GND DI 5 SPI_SI
W25Q64FVSSIG_SO8
+3V_SPI
CC8 1U_0402_10V6-K
GPU, EC, Thermal Sensor
+3VALW_PCH +3VS
RC62 2.2K_0402_5%
RC63 2.2K_0402_5%
PCH_SML1_CLK QC3A 2N7002KDWH_SOT363-6 EC_SMB_CK2 19,39,44
PCH_SML1_DAT QC3B 2N7002KDWH_SOT363-6 EC_SMB_DA2 19,39,44
+3V_SPI
RC179 1K_0402_5% @
RC180 1K_0402_5% @
SPI_WP#_R RC176 @ 33_0402_5% SPI_WP#_1
SPI_HOLD#_R RC178 @ 33_0402_5% SPI_HOLD#_1
UC6 @
SPI_CS1# 1 CS VCC 8
SPI_SO_1 2 DO(IO1) HOLD/RST(IO3) 7 SPI_HOLD#_1
SPI_WP#_1 3 WP(IO2) CLK 6 SPI_CLK_1
4 GND DI(IO0) 5 SPI_SI_1
W25Q32FVSSIG_SO8
+3V_SPI
CC97 1U_0402_10V6-K @
+3VALW_PCH +3V_SPI
RC1711 0_0402_5%
+3VS
RC1721 @ 0_0402_5%

CRYSTAL
1, Space 15MIL
2, No trace under crystal
3, Place on oppsosit side of MCP for temp influence

INTVRMEN
* H Integrated VRM enable (Default)
L Integrated VRM disable
(INTVRMEN should always be pull high.)

HDA_SDO This signal has a weak internal pull-down.
* **0 = Enable security measures defined in the Flash Descriptor.**
1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.

For EMI

IREF&RCOMP
Width: 12-15Mil
Space:12Mil
Length: 500Mil

+3V_SPI
* 1. If support DS3, connect to +3VS and don't support EC mirror code;
2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.

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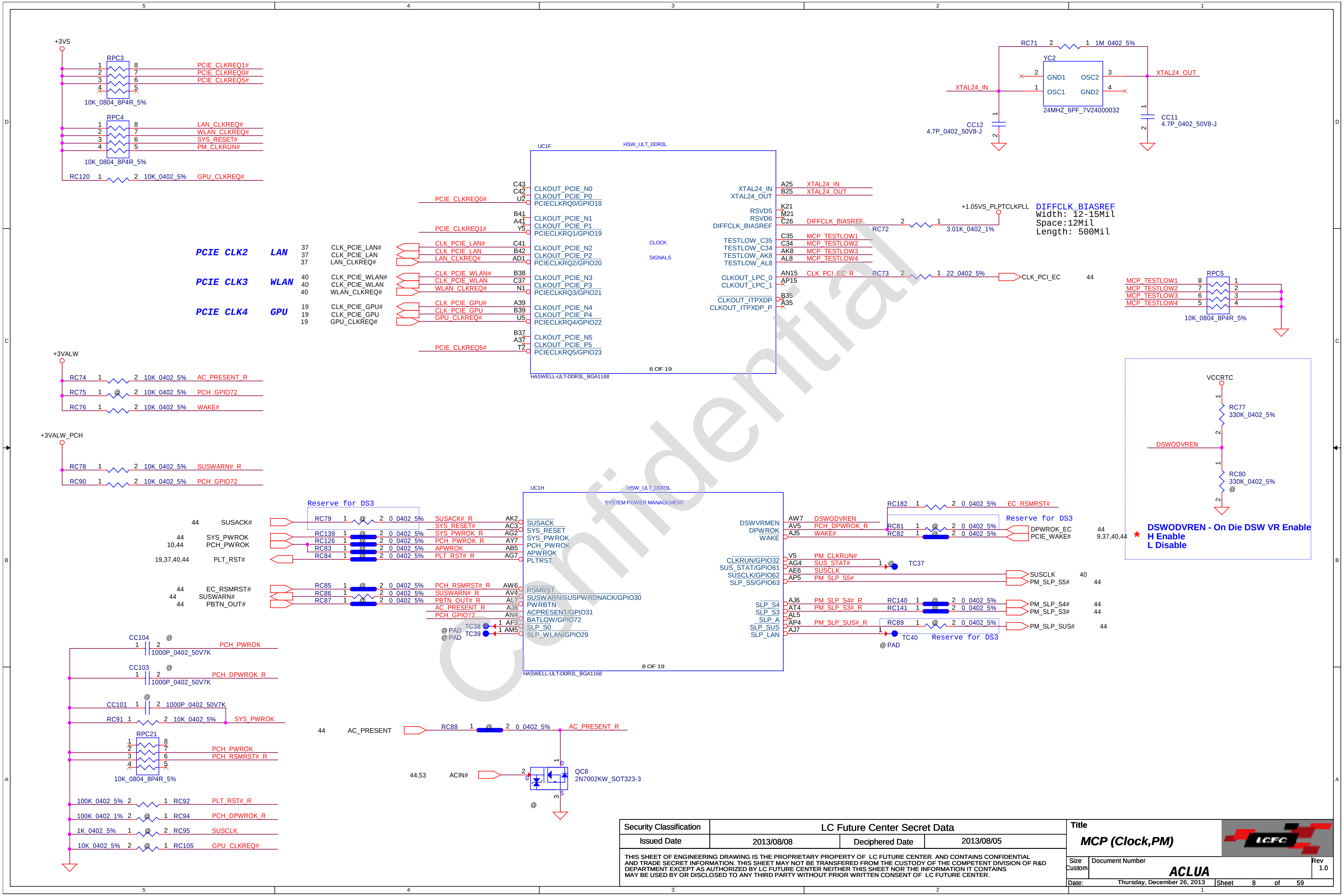
Title
MCP (RTC&AUDIO&SATA&S

Size	Document Number	Rev
C	ACLUA	1.0

Date: Thursday, December 26, 2013 Sheet 7 of 59


+3VS
RPC3
PCIE_CLKREQ1#
PCIE_CLKREQ0#
PCIE_CLKREQ5#
10K_0804_8P4R_5%
RPC4
LAN_CLKREQ#
WLAN_CLKREQ#
SYS_RESET#
PM_CLKRUN#
10K_0804_8P4R_5%
RC120 1 2 10K_0402_5% GPU_CLKREQ#
UC1F
HSW_ULT_DDR3L
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
PCIECLKRQ0/GPIO18
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
PCIECLKRQ1/GPIO19
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
PCIECLKRQ2/GPIO20
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
PCIECLKRQ3/GPIO21
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
PCIECLKRQ4/GPIO22
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
PCIECLKRQ5/GPIO23
CLOCK
SIGNALS
XTAL24_IN
XTAL24_OUT
RSVD5
RSVD6
DIFFCLK_BIASREF
TESTLOW_C35
TESTLOW_C34
TESTLOW_AK8
TESTLOW_AL8
CLKOUT_LPC_0
CLKOUT_LPC_1
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
6 OF 19
HASWELL-ULT-DDR3L_BGA1168
PCIE CLK2 LAN 37 CLK_PCIE_LAN# 37 CLK_PCIE_LAN 37 LAN_CLKREQ#
PCIE CLK3 WLAN 40 CLK_PCIE_WLAN# 40 CLK_PCIE_WLAN 40 WLAN_CLKREQ#
PCIE CLK4 GPU 19 CLK_PCIE_GPU# 19 CLK_PCIE_GPU 19 GPU_CLKREQ#
PCIE_CLKREQ0# PCIE_CLKREQ1# PCIE_CLKREQ5#
A25 XTAL24_IN
B25 XTAL24_OUT
C26 DIFFCLK_BIASREF RC72 2 1 3.01K_0402_1%
+1.05VS_PLPTCLKPLL
DIFFCLK_BIASREF
Width: 12-15Mil
Space:12Mil
Length: 500Mil
MCP_TESTLOW1 MCP_TESTLOW2 MCP_TESTLOW3 MCP_TESTLOW4
AN15 CLK_PCI_EC_R RC73 2 1 22_0402_5% CLK_PCI_EC 44
RPC5 10K_0804_8P4R_5%
RC71 2 1 1M_0402_5%
YC2 GND1 OSC2 OSC1 GND2
24MHZ_6PF_7V24000032
XTAL24_IN XTAL24_OUT
CC12 4.7P_0402_50V8-J
CC11 4.7P_0402_50V8-J
+3VALW
RC74 1 2 10K_0402_5% AC_PRESENT_R
RC75 1 @ 2 10K_0402_5% PCH_GPIO72
RC76 1 2 10K_0402_5% WAKE#
+3VALW_PCH
RC78 1 2 10K_0402_5% SUSWARN#_R
RC90 1 2 10K_0402_5% PCH_GPIO72
VCCRTC
RC77 330K_0402_5%
DSWODVREN
RC80 330K_0402_5% @
DSWODVREN - On Die DSW VR Enable
H Enable
L Disable
UC1H
HSW_ULT_DDR3L
SYSTEM POWER MANAGEMENT
Reserve for DS3
44 SUSACK#
44 SYS_PWROK
10,44 PCH_PWROK
19,37,40,44 PLT_RST#
44 EC_RSMRST#
44 SUSWARN#
44 PBTN_OUT#
RC79 RC139 RC126 RC83 RC84 0_0402_5%
SUSACK#_R SYS_RESET# SYS_PWROK_R PCH_PWROK_R APWROK PLT_RST#_R
RC85 RC86 RC87 0_0402_5%
PCH_RSMRST#_R SUSWARN#_R PBTN_OUT#_R AC_PRESENT_R PCH_GPIO72
SUSACK SYS_RESET SYS_PWROK PCH_PWROK APWROK PLTRST
RSMRST SUSWARN/SUSPWRDNACK/GPIO30 PWRBTN ACPRESENT/GPIO31 BATLOW/GPIO72 SLP_S0 SLP_WLAN/GPIO29
TC38 TC39 @PAD
DSWVRMEN DPWROK WAKE
CLKRUN/GPIO32 SUS_STAT/GPIO61 SUSCLK/GPIO62 SLP_S5/GPIO63
SLP_S4 SLP_S3 SLP_A SLP_SUS SLP_LAN
8 OF 19
HASWELL-ULT-DDR3L_BGA1168
RC182 1 2 0_0402_5% EC_RSMRST#
DSWODVREN PCH_DPWROK_R WAKE#
RC81 RC82 0_0402_5%
DPWROK_EC 44
PCIE_WAKE# 9,37,40,44
PM_CLKRUN# SUS_STAT# TC37 SUSCLK PM_SLP_S5#
SUSCLK 40
PM_SLP_S5# 44
PM_SLP_S4#_R PM_SLP_S3#_R RC140 RC141 0_0402_5%
PM_SLP_S4# 44
PM_SLP_S3# 44
PM_SLP_SUS#_R RC89 0_0402_5% PM_SLP_SUS# 44
TC40 Reserve for DS3 @PAD
CC104 @ 1000P_0402_50V7K PCH_PWROK
CC103 @ 1000P_0402_50V7K PCH_DPWROK_R
CC101 1000P_0402_50V7K
RC91 10K_0402_5% SYS_PWROK
RPC21 PCH_PWROK PCH_RSMRST#_R 10K_0804_8P4R_5%
100K_0402_5% RC92 PLT_RST#_R
100K_0402_1% RC94 PCH_DPWROK_R
1K_0402_5% RC95 SUSCLK
10K_0402_5% RC105 GPU_CLKREQ#
44 AC_PRESENT RC88 0_0402_5% AC_PRESENT_R
44,53 ACIN#
QC8 2N7002KW_SOT323-3

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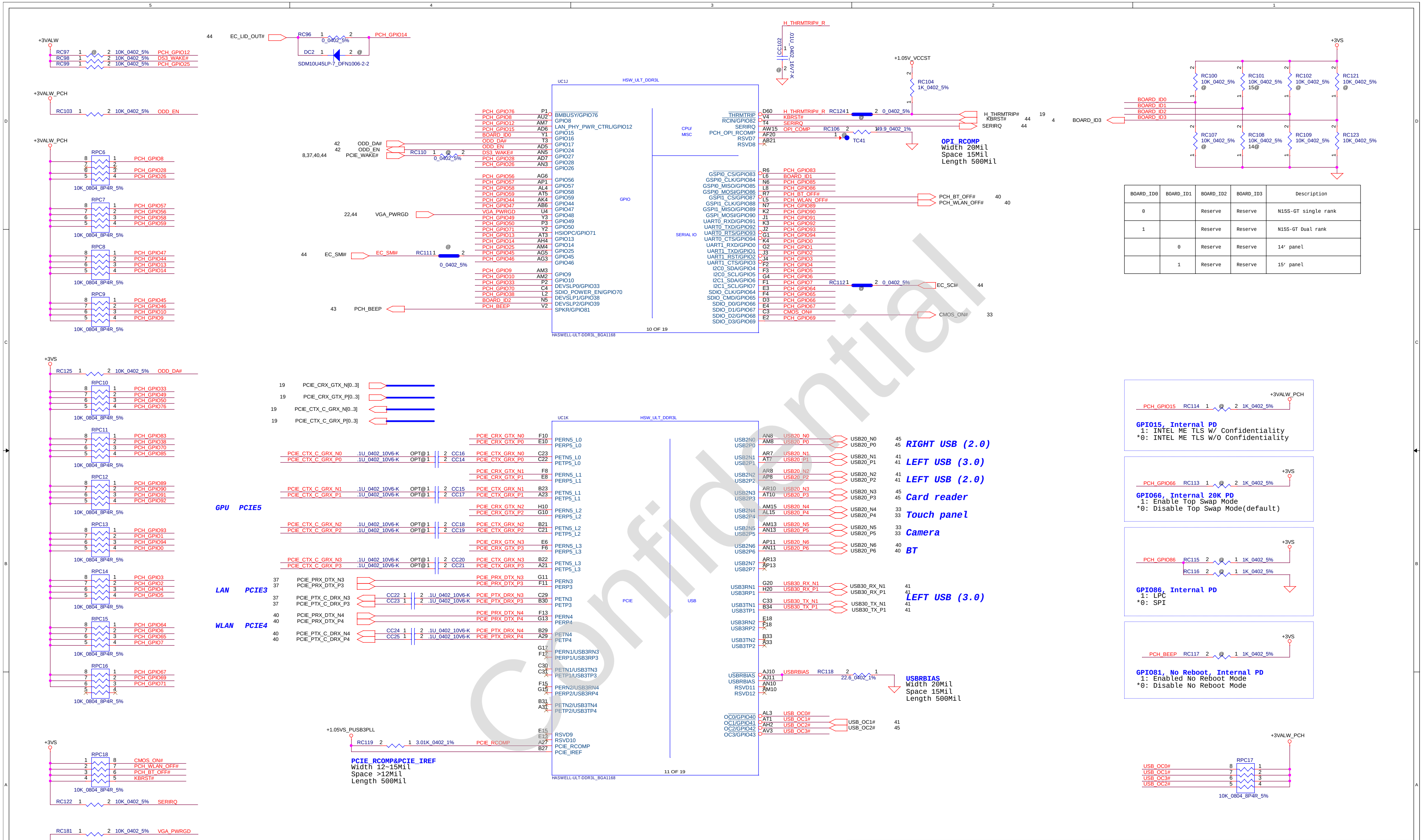
Title
MCP (Clock,PM)

Size Custom
Document Number **ACLUA**
Rev 1.0
Date: Thursday, December 26, 2013 Sheet 8 of 59



OPI_RCOMP
Width 20Mil
Space 15Mil
Length 500Mil

PCIE_RCOMP&PCIE_IREF
Width 12~15Mil
Space >12Mil
Length 500Mil

USBRBIAS
Width 20Mil
Space 15Mil
Length 500Mil

GPIO15, Internal PD
1: INTEL ME TLS W/ Confidentiality
*0: INTEL ME TLS W/O Confidentiality

GPIO66, Internal 20K PD
1: Enable Top Swap Mode
*0: Disable Top Swap Mode(default)

GPIO86, Internal PD
1: LPC
*0: SPI

GPIO81, No Reboot, Internal PD
1: Enabled No Reboot Mode
*0: Disable No Reboot Mode

BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description
0		Reserve	Reserve	N15S-GT single rank
1		Reserve	Reserve	N15S-GT Dual rank
	0	Reserve	Reserve	14′ panel
	1	Reserve	Reserve	15′ panel

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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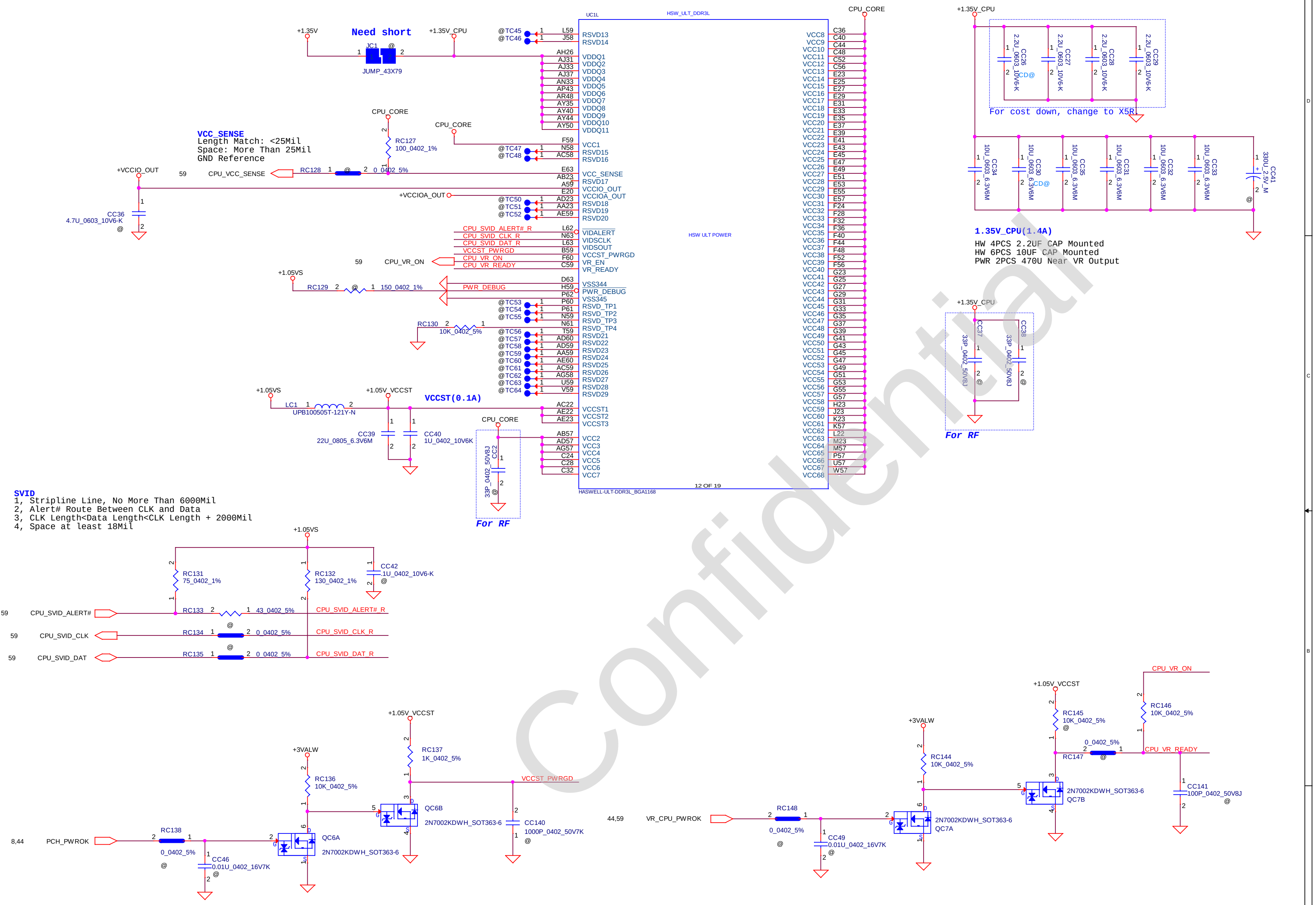
Title
MCP (GPIO,USB,PCIE)

Size Custom
Document Number **ACLUA**
Rev 1.0

Date: Monday, December 30, 2013



Need short

VCC_SENSE
Length Match: <25Mil
Space: More Than 25Mil
GND Reference

VCCST(0.1A)

For RF

For cost down, change to X5R

1.35V_CPU(1.4A)
HW 4PCS 2.2UF CAP Mounted
HW 6PCS 10UF CAP Mounted
PWR 2PCS 470U Near VR Output

For RF

SVID
1, Stripline Line, No More Than 6000Mil
2, Alert# Route Between CLK and Data
3, CLK Length<Data Length<CLK Length + 2000Mil
4, Space at least 18Mil

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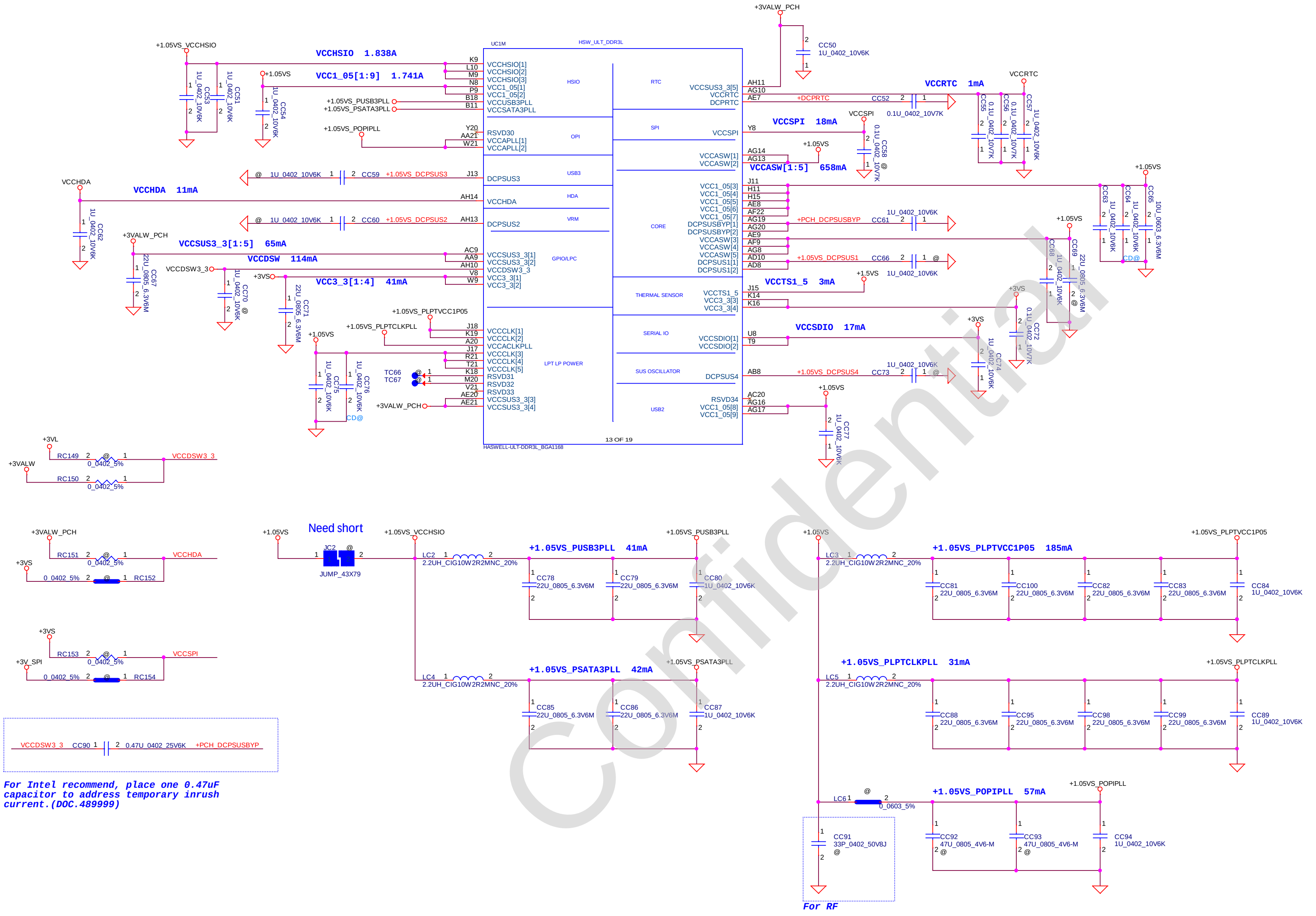
Title
MCP (Power)

Size: Custom
Document Number: ACLUA
Rev: 1.0
Date: Monday, December 30, 2013
Sheet 10 of 59

LCFC



For Intel recommend, place one 0.47uF capacitor to address temporary inrush current.(DOC.489999)

Security Classification	LC Future Center Secret Data			Title
Issued Date	2013/08/08	Deciphered Date	2013/08/05	MCP (Power2)

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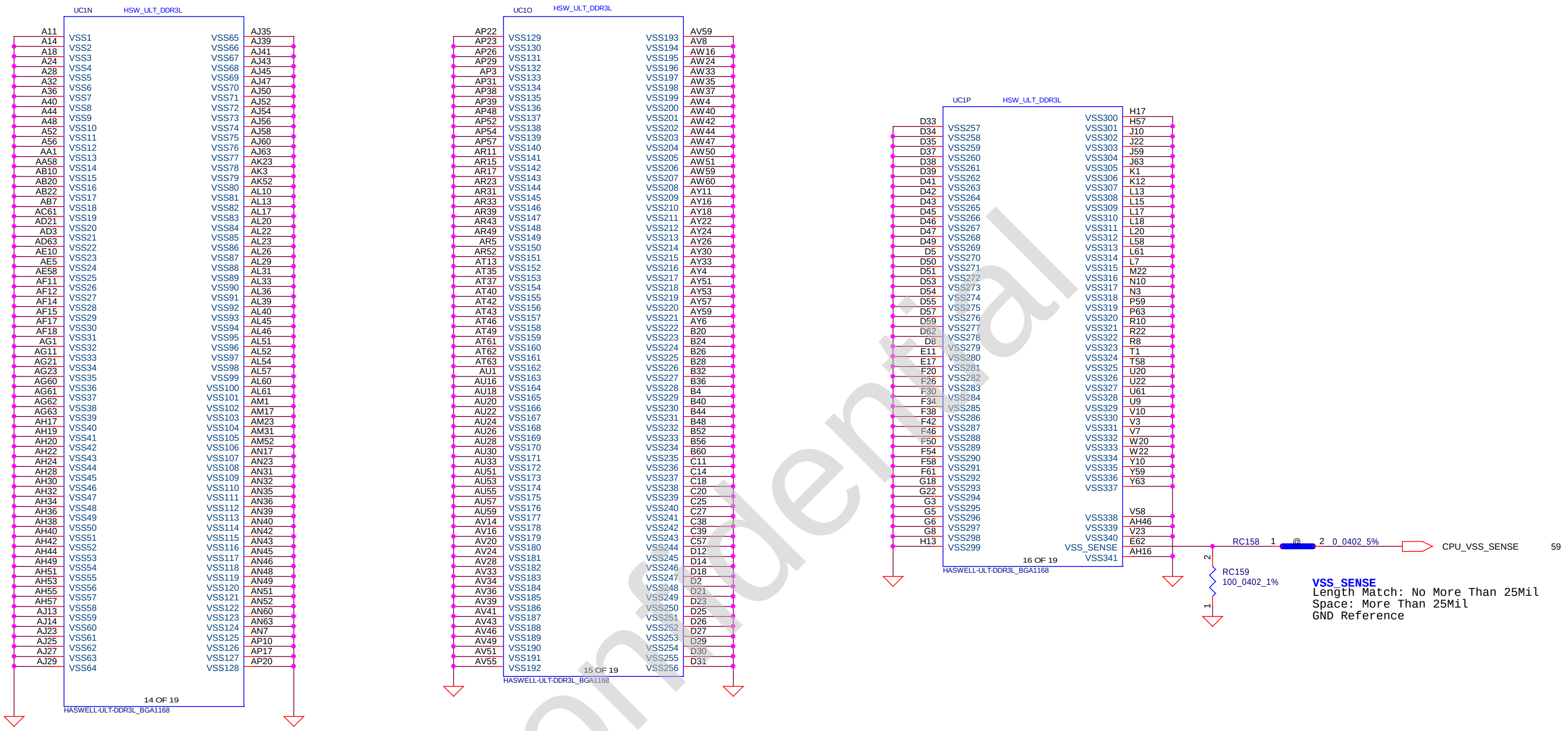
Size	Document Number	Rev
Custom	ACLUA	1.0

Date: Thursday, December 26, 2013 Sheet 11 of 59



VSS_SENSE
Length Match: No More Than 25Mil
Space: More Than 25Mil
GND Reference

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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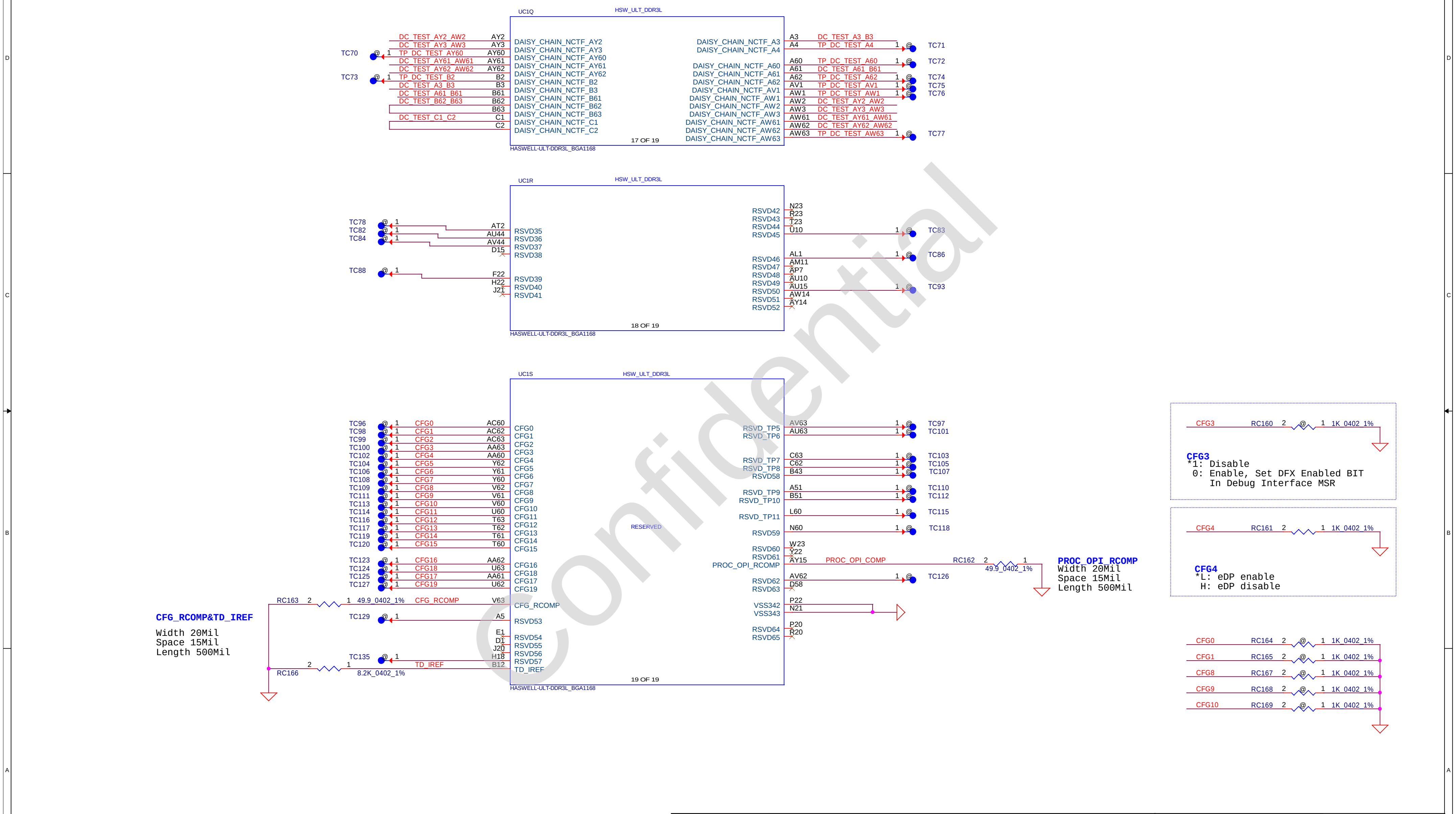
Title
MCP (VSS)

LCFC

Size
Custom
Document Number
ACLUA
Rev
1.0

Date: Thursday, December 26, 2013 Sheet 12 of 59



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Title
MCP (OTHER)

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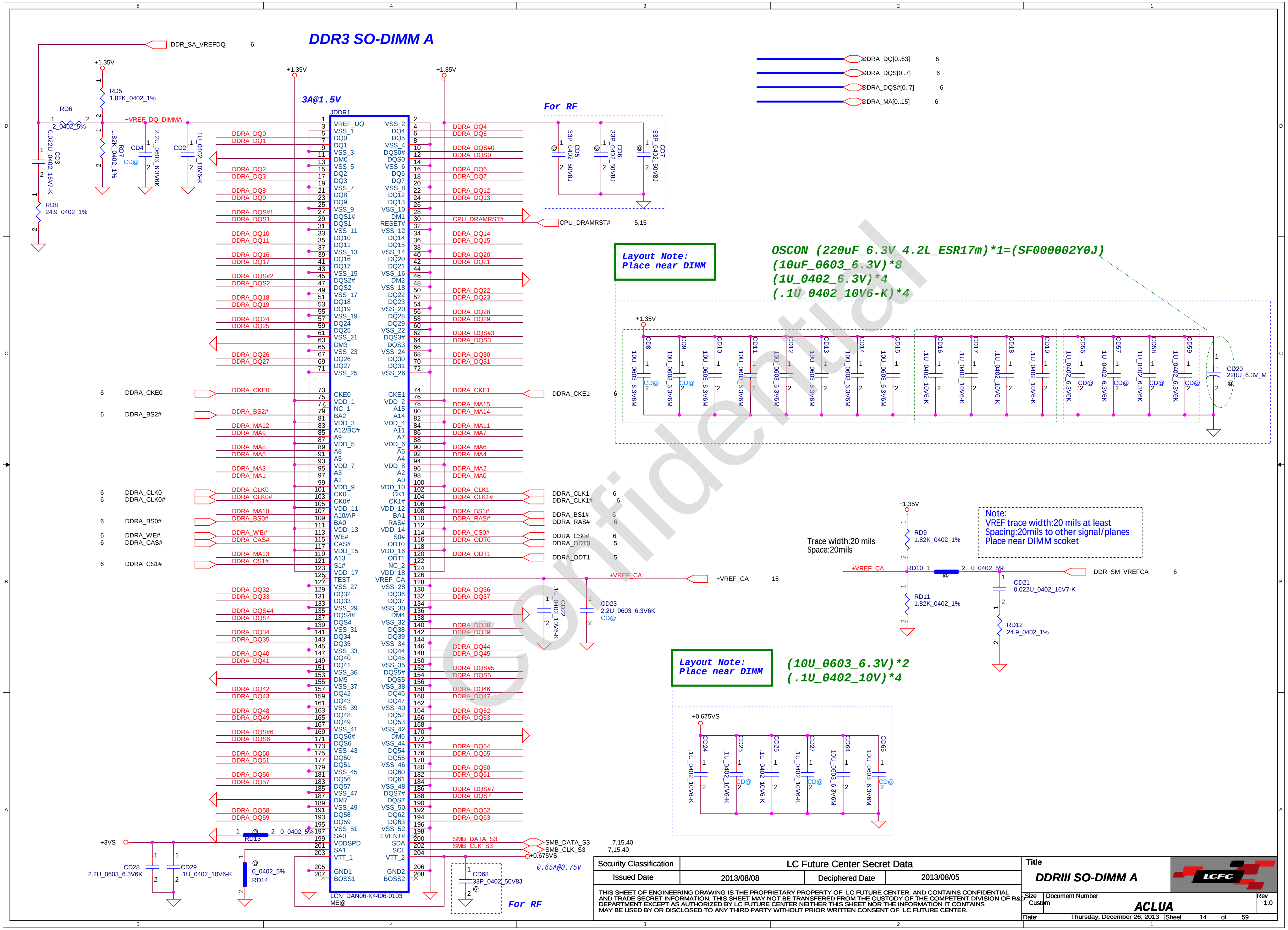
Rev 1.0
Date: Thursday, December 26, 2013
Sheet 13 of 59

DDR3 SO-DIMM A



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Title
DDRIII SO-DIMM A

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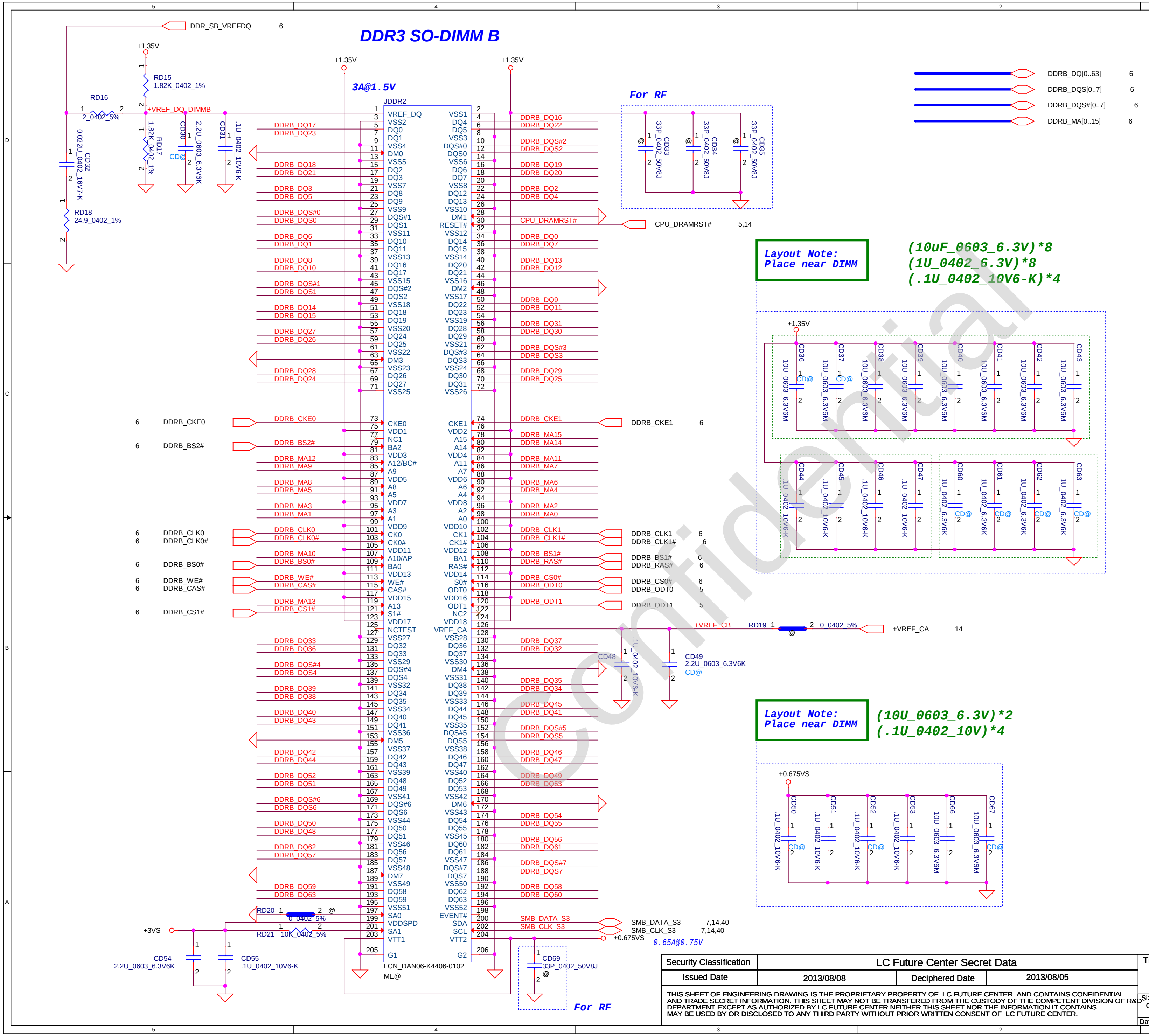
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 14 of 59

DDR3 SO-DIMM B



Swap Table

Pin Number	Pin Name	Net Name
5	DQ0	DDRB_DQ17
7	DQ1	DDRB_DQ23
15	DQ2	DDRB_DQ18
17	DQ3	DDRB_DQ21
4	DQ4	DDRB_DQ16
6	DQ5	DDRB_DQ22
16	DQ6	DDRB_DQ19
18	DQ7	DDRB_DQ20
10	DQS#0	DDRB_DQS#2
12	DQS0	DDRB_DQS2
21	DQ8	DDRB_DQ3
23	DQ9	DDRB_DQ5
33	DQ10	DDRB_DQ6
35	DQ11	DDRB_DQ1
22	DQ12	DDRB_DQ2
24	DQ13	DDRB_DQ4
34	DQ14	DDRB_DQ0
36	DQ15	DDRB_DQ7
27	DQS#1	DDRB_DQS#0
29	DQS1	DDRB_DQS0
39	DQ16	DDRB_DQ8
41	DQ17	DDRB_DQ10
51	DQ18	DDRB_DQ14
53	DQ19	DDRB_DQ15
40	DQ20	DDRB_DQ13
42	DQ21	DDRB_DQ12
50	DQ22	DDRB_DQ9
52	DQ23	DDRB_DQ11
45	DQS#2	DDRB_DQS#1
47	DQS2	DDRB_DQS1
57	DQ24	DDRB_DQ27
59	DQ25	DDRB_DQ26
67	DQ26	DDRB_DQ28
69	DQ27	DDRB_DQ24
56	DQ28	DDRB_DQ31
58	DQ29	DDRB_DQ30
68	DQ30	DDRB_DQ29
70	DQ31	DDRB_DQ25
62	DQS#3	DDRB_DQS#3
64	DQS3	DDRB_DQS3
129	DQ32	DDRB_DQ33
131	DQ33	DDRB_DQ36
141	DQ34	DDRB_DQ39
143	DQ35	DDRB_DQ38
130	DQ36	DDRB_DQ37
132	DQ37	DDRB_DQ32
140	DQ38	DDRB_DQ35
142	DQ39	DDRB_DQ34
135	DQS#4	DDRB_DQS#4
137	DQS4	DDRB_DQS4
147	DQ40	DDRB_DQ40
149	DQ41	DDRB_DQ43
157	DQ42	DDRB_DQ42
159	DQ43	DDRB_DQ44
146	DQ44	DDRB_DQ45
148	DQ45	DDRB_DQ41
158	DQ46	DDRB_DQ46
160	DQ47	DDRB_DQ47
152	DQS#5	DDRB_DQS#5
154	DQS5	DDRB_DQS5
163	DQ48	DDRB_DQ52
165	DQ49	DDRB_DQ51
175	DQ50	DDRB_DQ50
177	DQ51	DDRB_DQ48
164	DQ52	DDRB_DQ49
166	DQ53	DDRB_DQ53
174	DQ54	DDRB_DQ54
176	DQ55	DDRB_DQ55
169	DQS#6	DDRB_DQS#6
171	DQS6	DDRB_DQS6
181	DQ56	DDRB_DQ62
183	DQ57	DDRB_DQ57
191	DQ58	DDRB_DQ59
193	DQ59	DDRB_DQ63
180	DQ60	DDRB_DQ56
182	DQ61	DDRB_DQ61
192	DQ62	DDRB_DQ58
194	DQ63	DDRB_DQ60
186	DQS#7	DDRB_DQS#7
188	DQS7	DDRB_DQS7

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Title
DDRIII SO-DIMM B
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Size: Custom
Document Number: ACLUA
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 15 of 59

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title
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Size: Custom
Document Number: **ACLUA**
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 16 of 59

D D

C C

B B

A A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title

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LCFC

Size Custom
Document Number ***ACLUA***
Rev 1.0
Date: Thursday, December 26, 2013
Sheet 17 of 59

N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

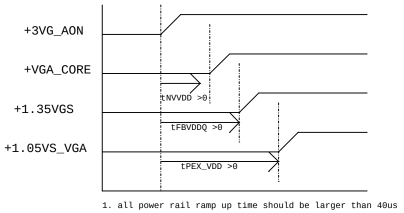
	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)			I/O and PLLVDD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)		(mA)	(W)	(mA)	(W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD		TBD	TBD	TBD	TBD

N15x Multi-level Straps

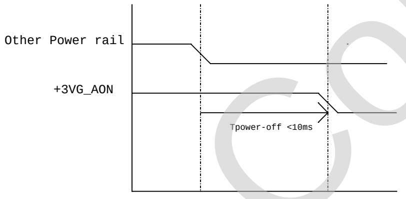
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence



1. all power rail ramp up time should be larger than 40us

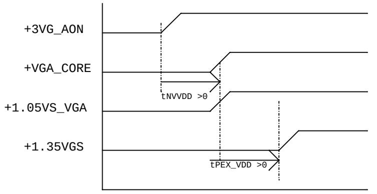


1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

N15S-GT Power Sequence



1. all power rail ramp up time should be larger than 40us

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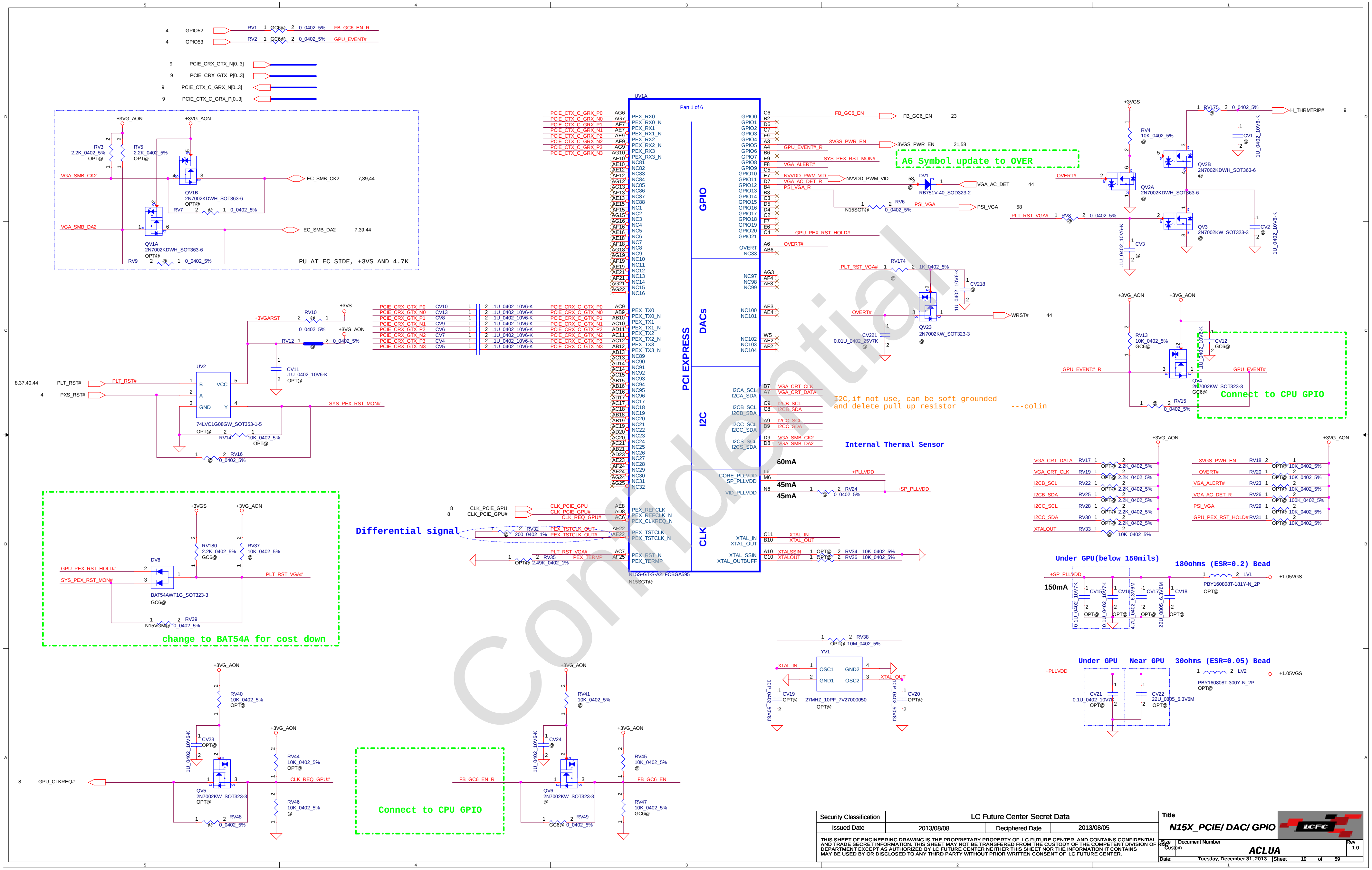
Title
VGA Notes List

Size	Document Number	Rev
C	ACLUA	1.0

Date: Thursday, December 26, 2013 Sheet 18 of 59



Security Classification	LC Future Center Secret Data	Title
Issued Date 2013/08/08	Deciphered Date 2013/08/05	N15X_PCIE/ DAC/ GPIO

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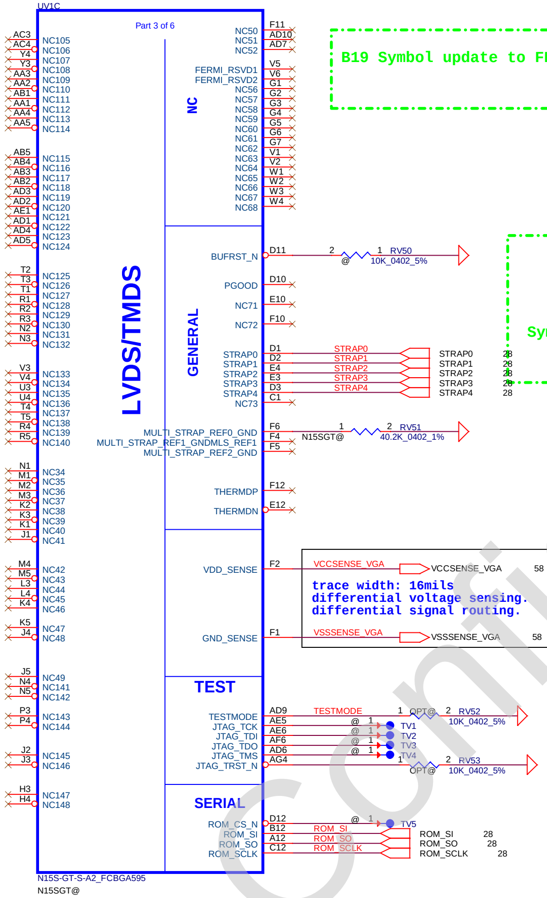

B19 Symbol update to FBA_CMD32

Symbol update to GPIO8

trace width: 16mils
differential voltage sensing.
differential signal routing.

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Title
N15X_LVDS/ HDMI/ THERM

Size C
Document Number
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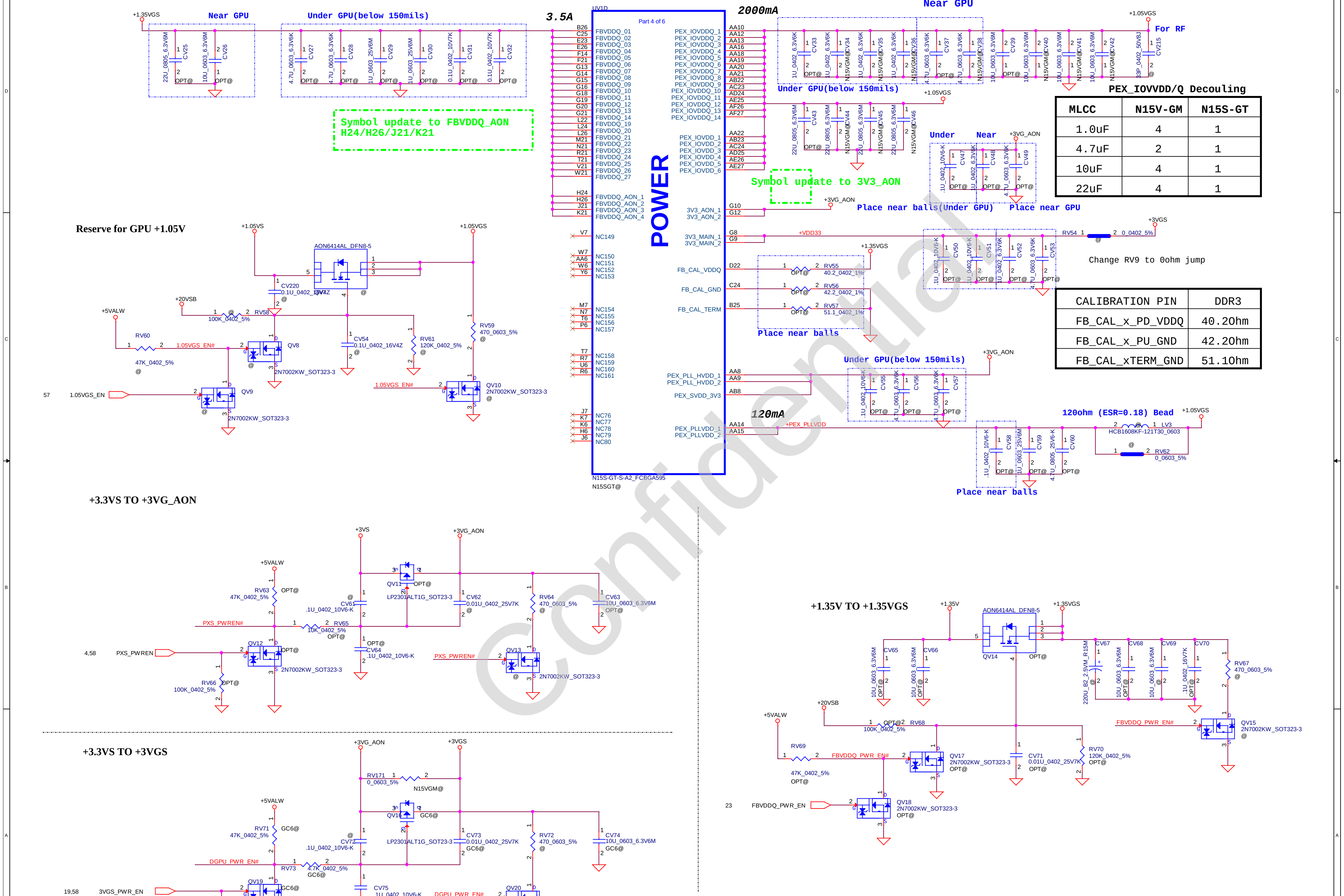
Rev 1.0
Date: Thursday, December 26, 2013
Sheet 20 of 59



PEX_IOVVDD/Q Decouling

MLCC	N15V-GM	N15S-GT
1.0uF	4	1
4.7uF	2	1
10uF	4	1
22uF	4	1

CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

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Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title
N15X_Power

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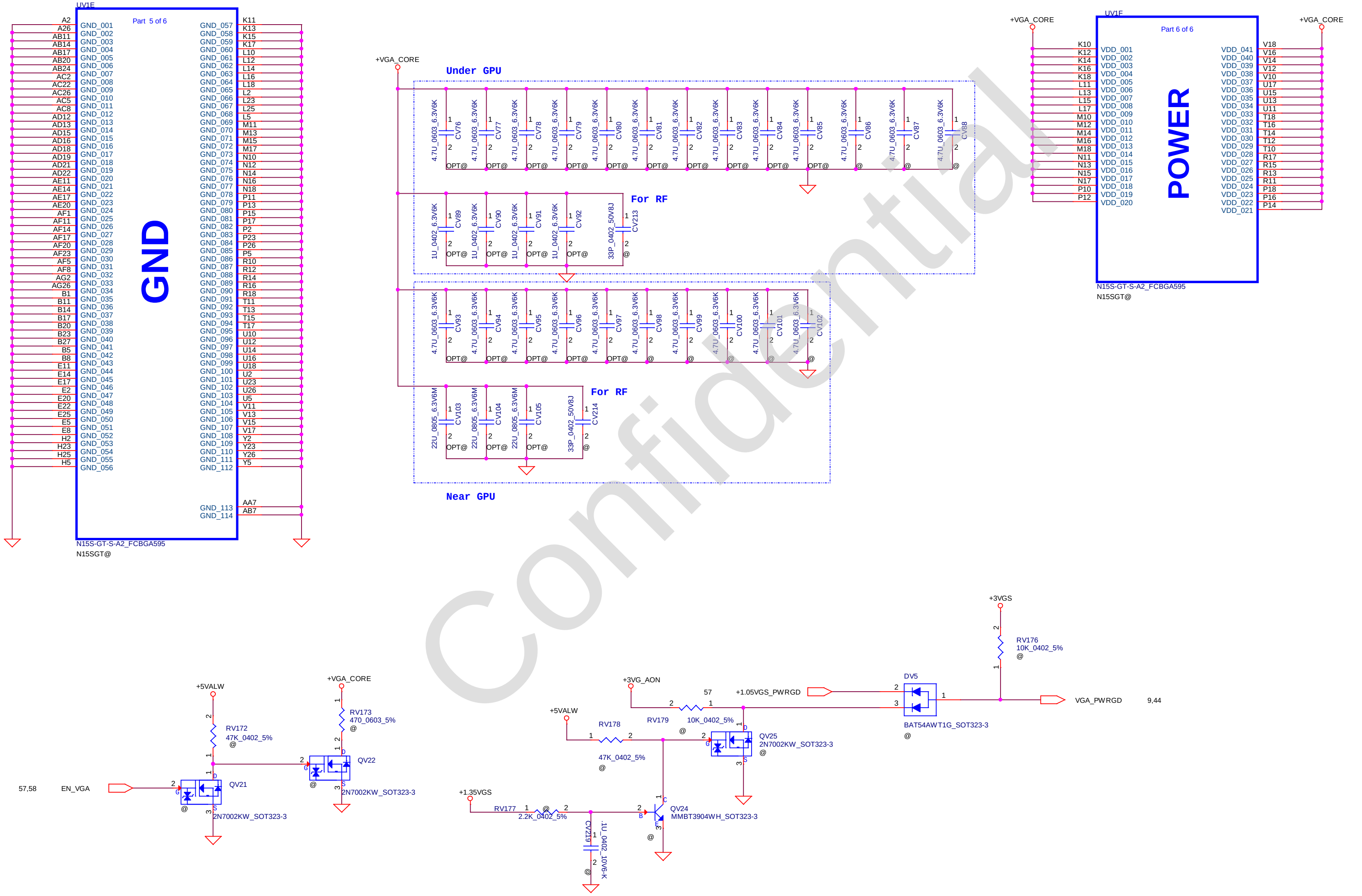
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 21 of 59



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Title
N15X_+VGA CORE, GND

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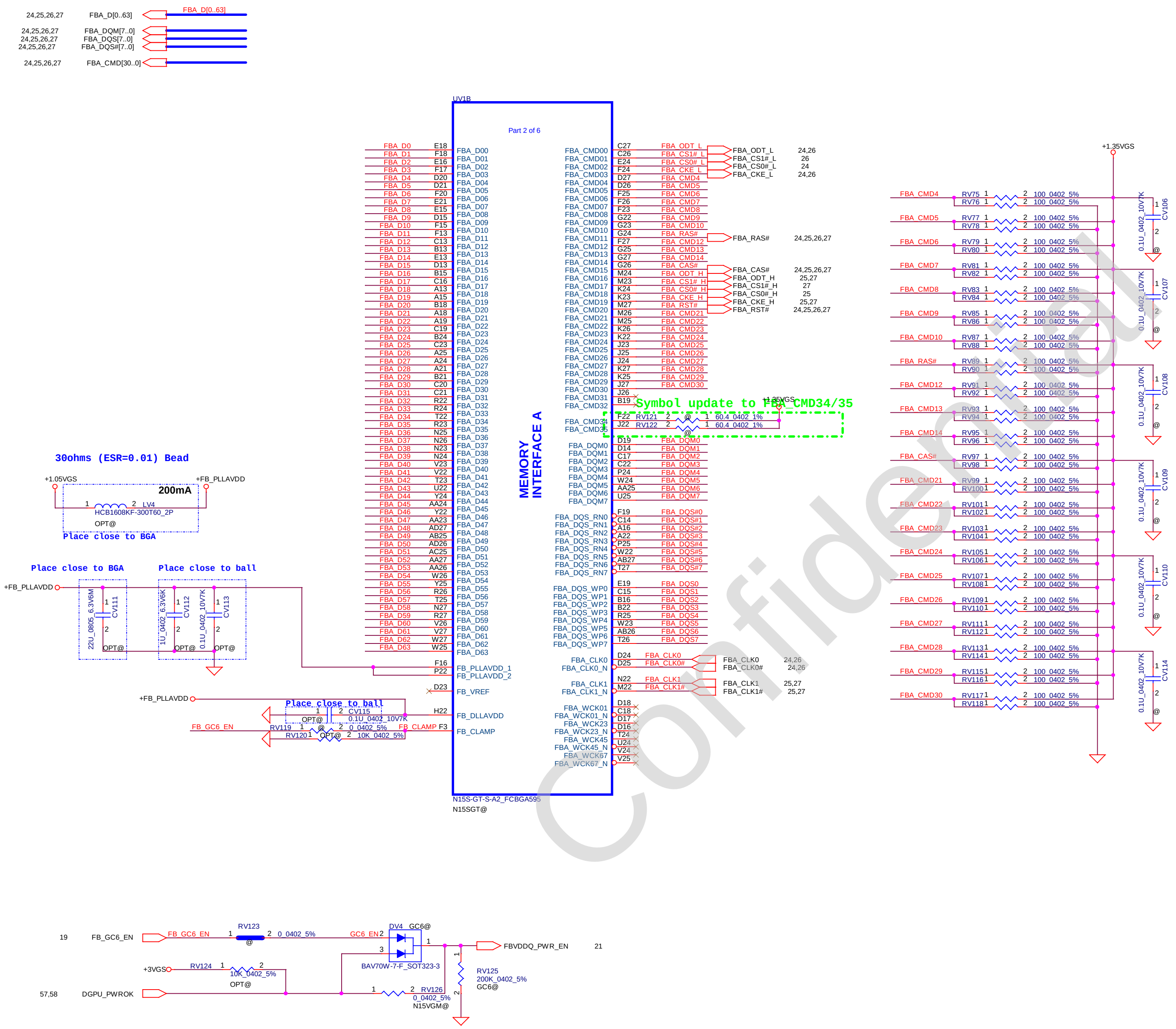


CMD mapping mod Mode E

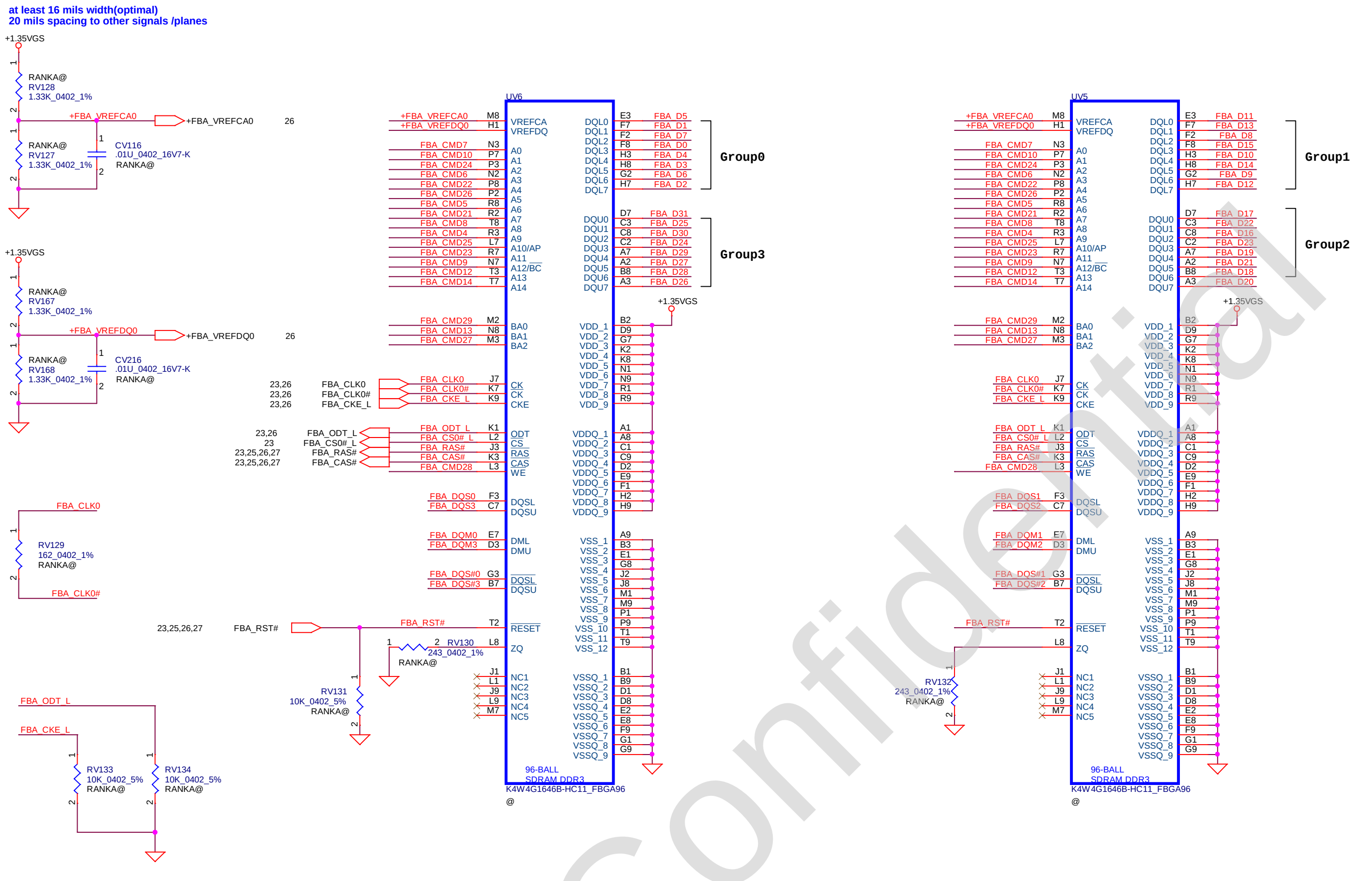
	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2

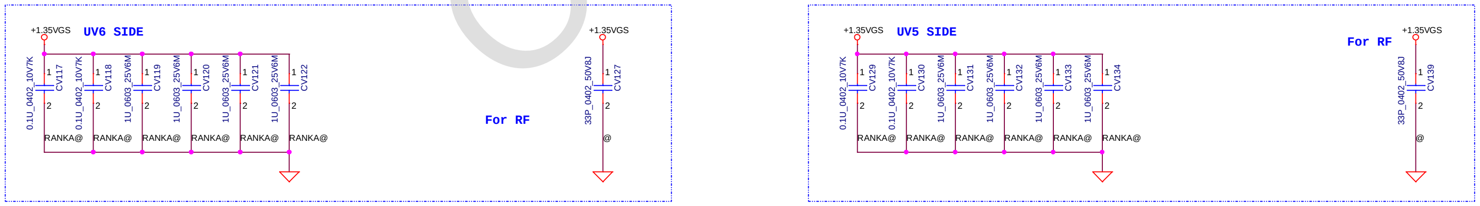
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

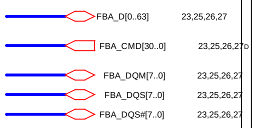
Title
N15X_MEM Interface

Size C
Document Number
ACLUA
Rev 1.0

Date: Thursday, December 26, 2013 Sheet 23 of 59







CMD mapping mod Mode E

	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2

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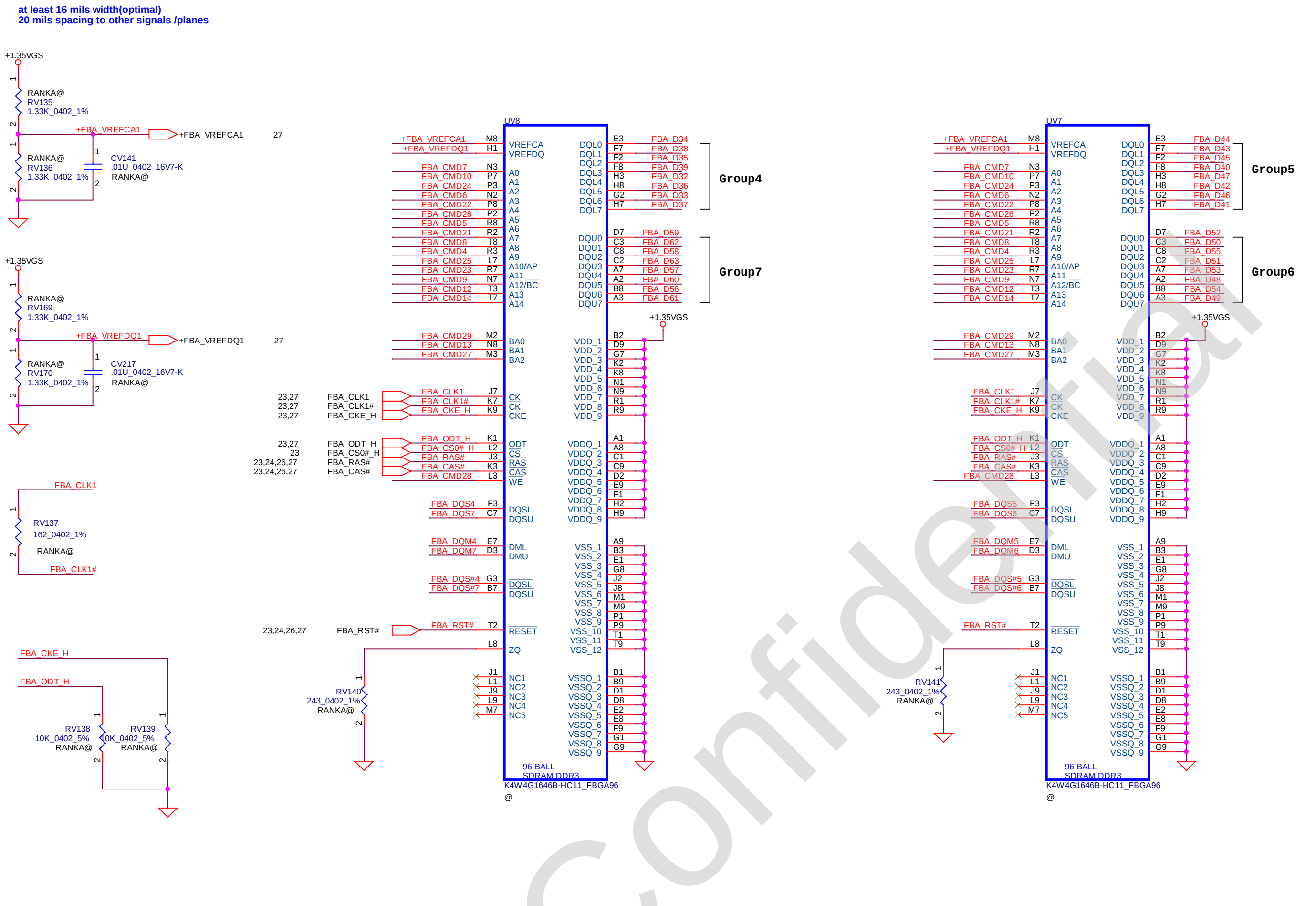
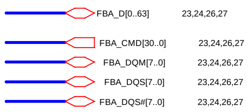
Title
DDR3 VRAM Rank0_L

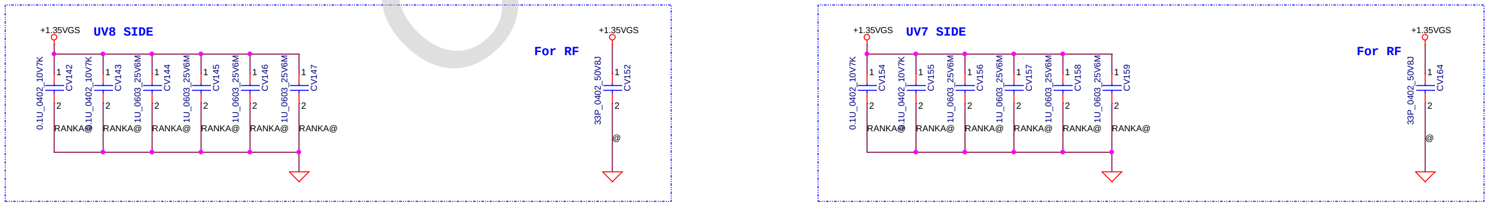
Size C
Document Number ACLUA
Rev 1.0
Date: Thursday, December 26, 2013
Sheet 24 of 59





CMD mapping mod Mode E

	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2



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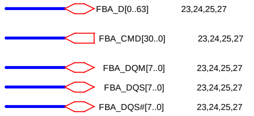
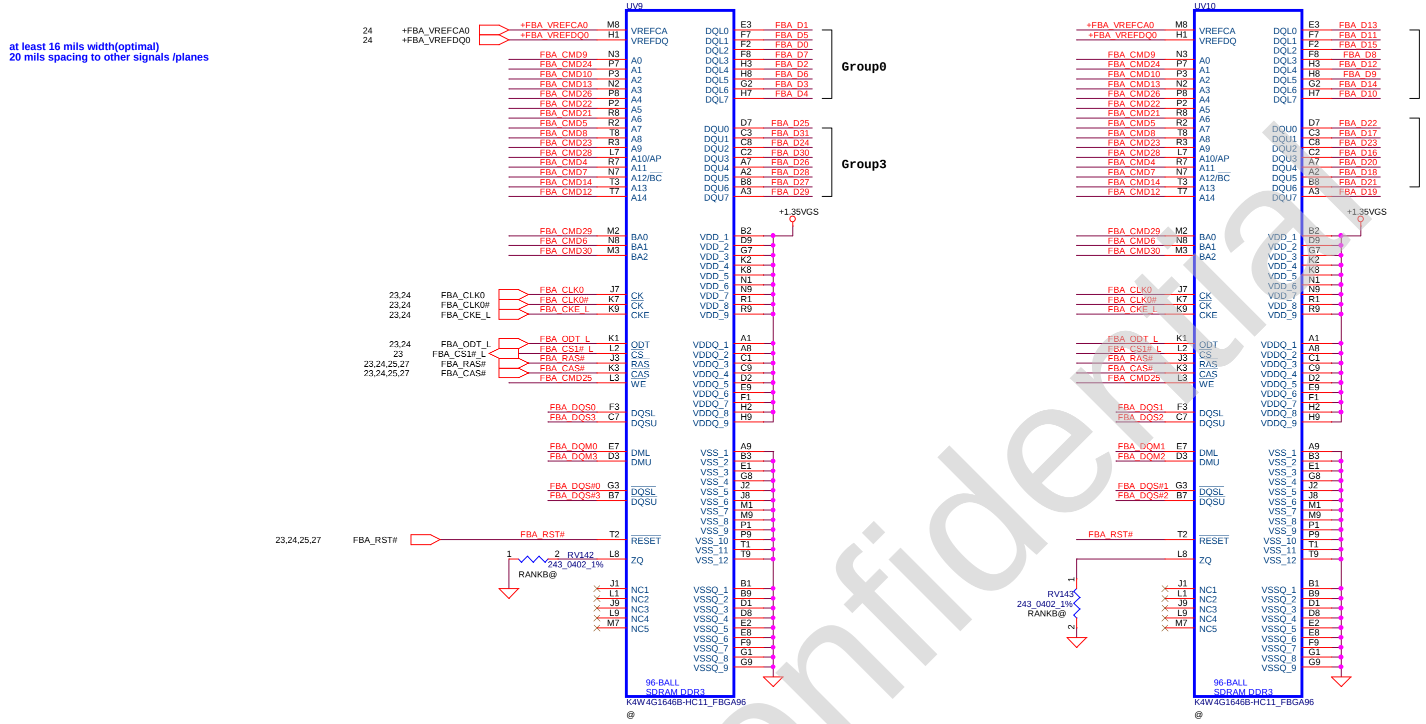
Title
DDR3 VRAM Rank0_H
LCFC
Size C
Document Number **ACLUA**
Rev 1.0
Date: Thursday, December 26, 2013


FBA_D[0..63] 23,24,25,27
FBA_CMD[30..0] 23,24,25,27
FBA_DQM[7..0] 23,24,25,27
FBA_DQS[7..0] 23,24,25,27
FBA_DQS#[7..0] 23,24,25,27

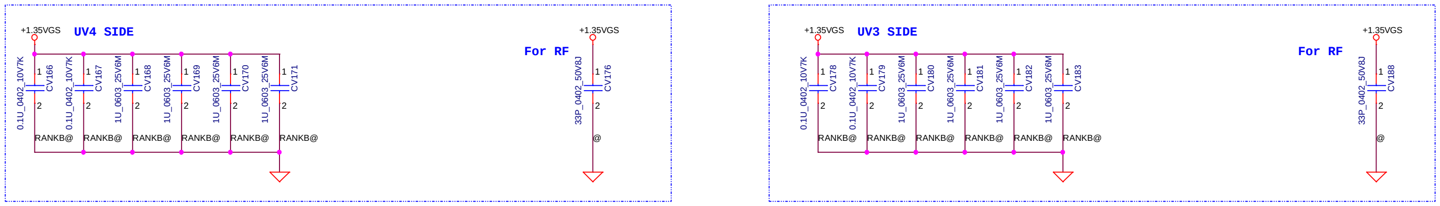


Group1

Group2

CMD mapping mod Mode E

	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2



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Issued Date	2013/08/08	Deciphered Date	2013/08/05

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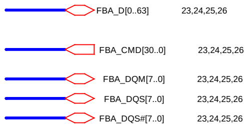
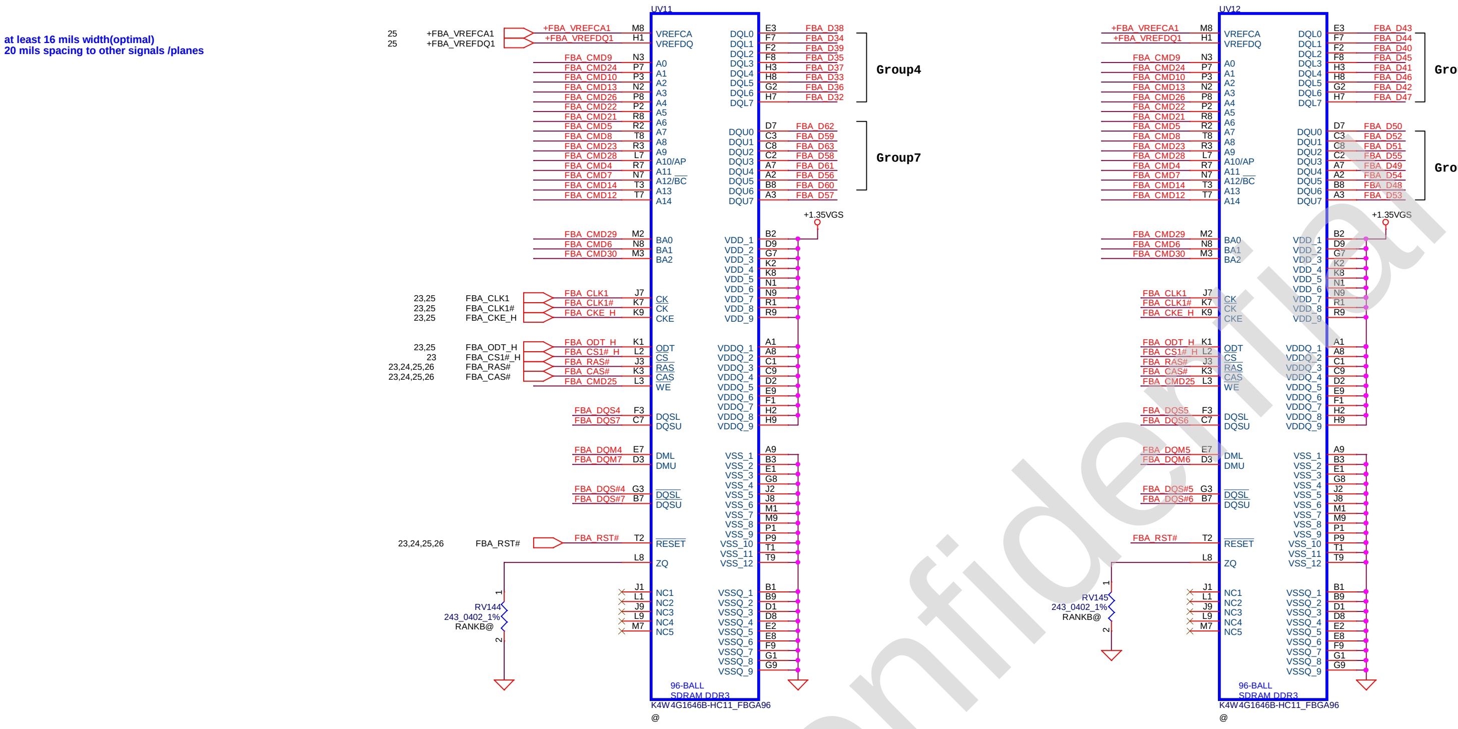
Title
DDR3 VRAM Rank1_L

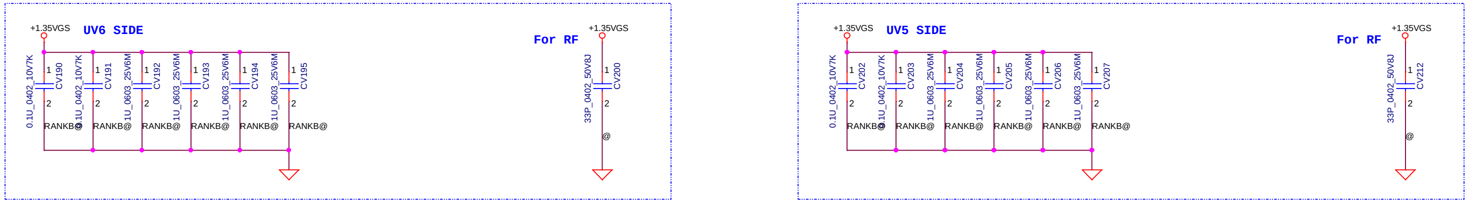
Size C
Document Number **ACLUA**
Rev 1.0
Date: Thursday, December 26, 2013
Sheet 26 of 59


FBA_D[0..63] 23,24,25,26
FBA_CMD[30..0] 23,24,25,26
FBA_DQM[7..0] 23,24,25,26
FBA_DQS[7..0] 23,24,25,26
FBA_DQS#[7..0] 23,24,25,26



CMD mapping mod Mode E

	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2



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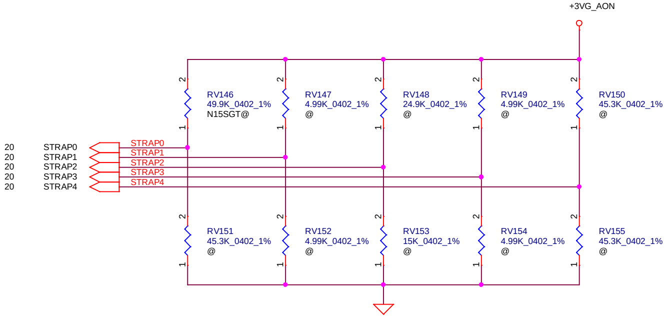
Title
DDR3 VRAM Rank1_H

Size C
Document Number **ACLUA**
Rev 1.0

Date: Thursday, December 26, 2013
Sheet 27 of 59



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

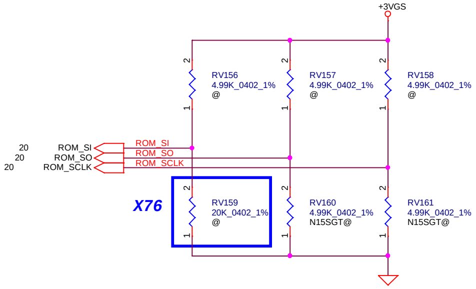
Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)



Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

X76

GPU	FB Memory (DDR3)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N15S-GT	Hynix 900MHz	H5TC4G63AFR-11C	0x3	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
		256M x 16	PD 20K							
	Micron 900MHz	MT41J256M16HA-093G:E	0x4							
		256M x 16	PD 24.9K							
	Samsung 900MHz	K4W4G1646D-BC1A	0x5							
		256M x 16	PD 30.1K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01	SA00005SH10
	X76409JVL51 (1G 32Mx16)	
Micron	X76409JVL02	SA00005M100
	X76409JVL02 (2G 64Mx32)	
Hynix		

GPU	FB Memory (DDR3)			STRAP3	STRAP2	STRAP1	STRAP0	STRAP4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GM	Hynix 900MHz	H5TC4G63AFR-11C		PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
		256M x 16	0x4								
	Micron 900MHz	MT41J256M16HA-093G:E		PU 10K	PU 10K	PD 10K	PU 10K				
		256M x 16	0xD								

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title
N15X_MISC

Size: C
Document Number: ACLUA
Rev: 1.0
Date: Thursday, December 26, 2013

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Title

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LCFC

Size	Document Number	Rev
Custom	**ACLUA**	1.0

Date: Thursday, December 26, 2013 Sheet 29 of 59

Security Classification	LC Future Center Secret Data		
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Title
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Size: Custom
Document Number: **ACLUA**
Rev: 1.0

Date: Thursday, December 26, 2013
Sheet 30 of 59

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Size	Document Number	Rev
Custom	ACLUA	1.0

Date: Thursday, December 26, 2013 Sheet 31 of 59

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title
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LCFC

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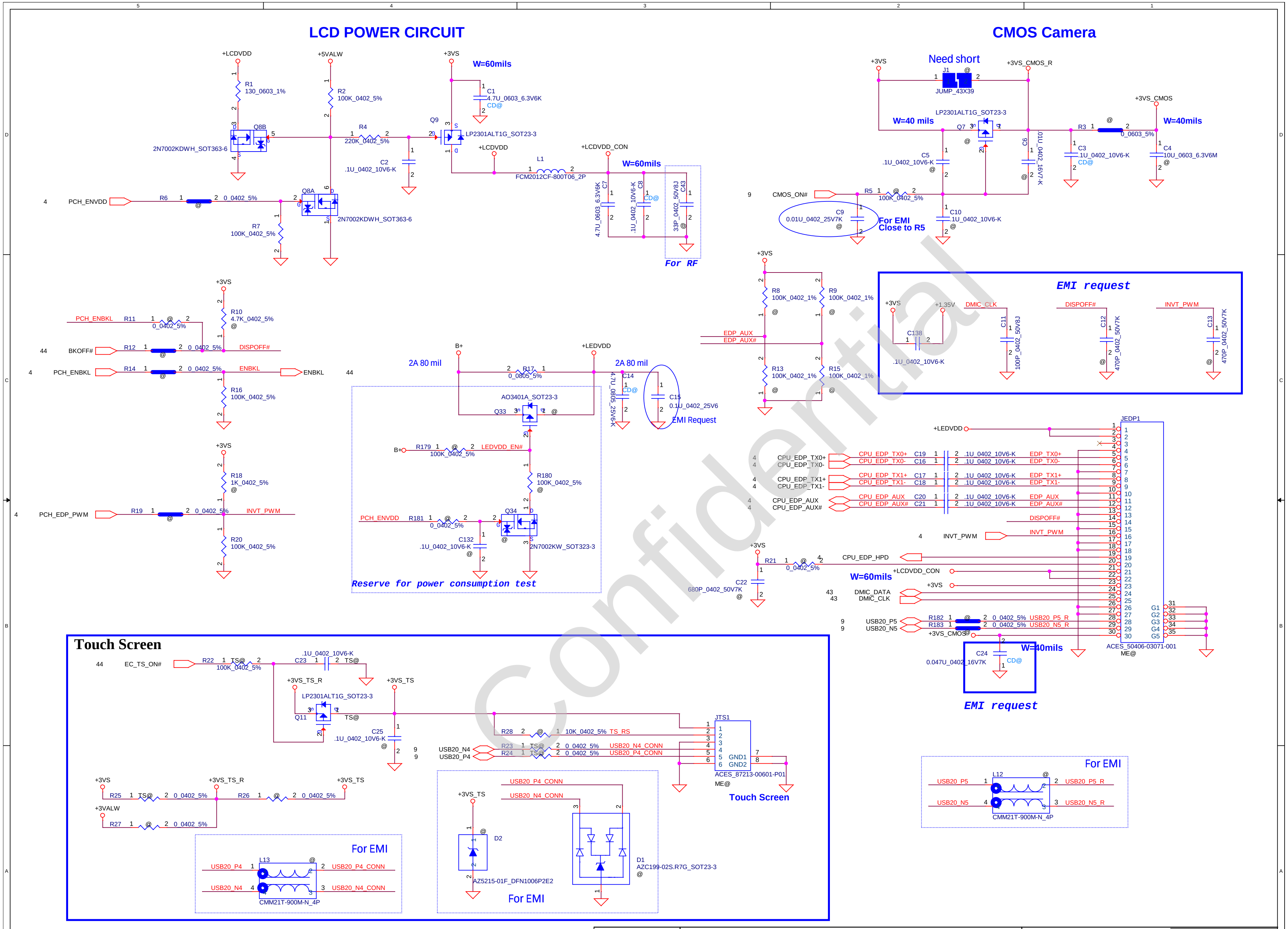
Document Number: ***ACLUA***
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 32 of 59



Security Classification	LC Future Center Secret Data			Title
Issued Date	2013/08/08	Deciphered Date	2013/08/05	eDP/ CMOS/Touch screen

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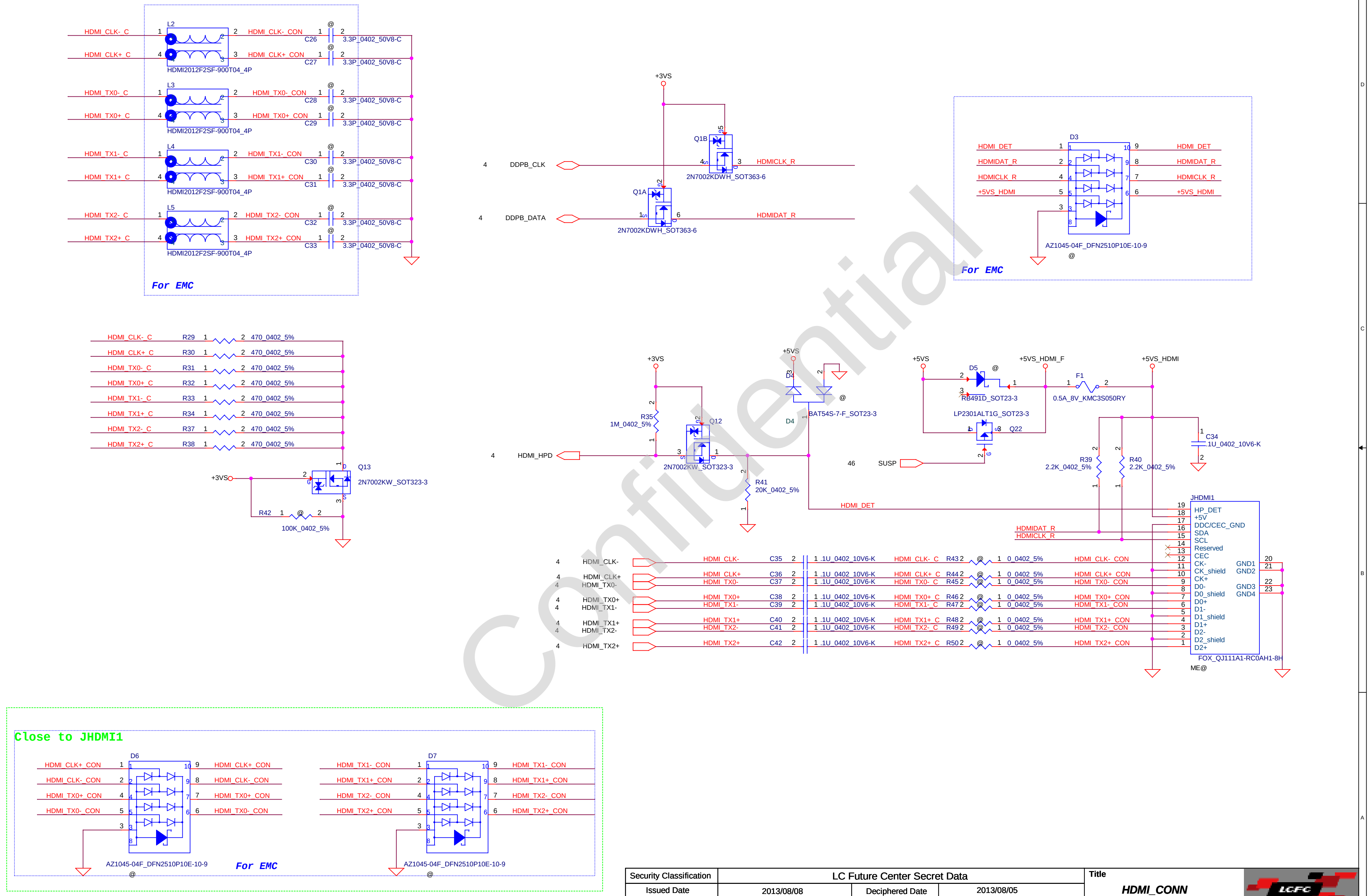
Size	Document Number	Rev
Custom	ACLUA	1.0

Date: Thursday, December 26, 2013 Sheet 33 of 59



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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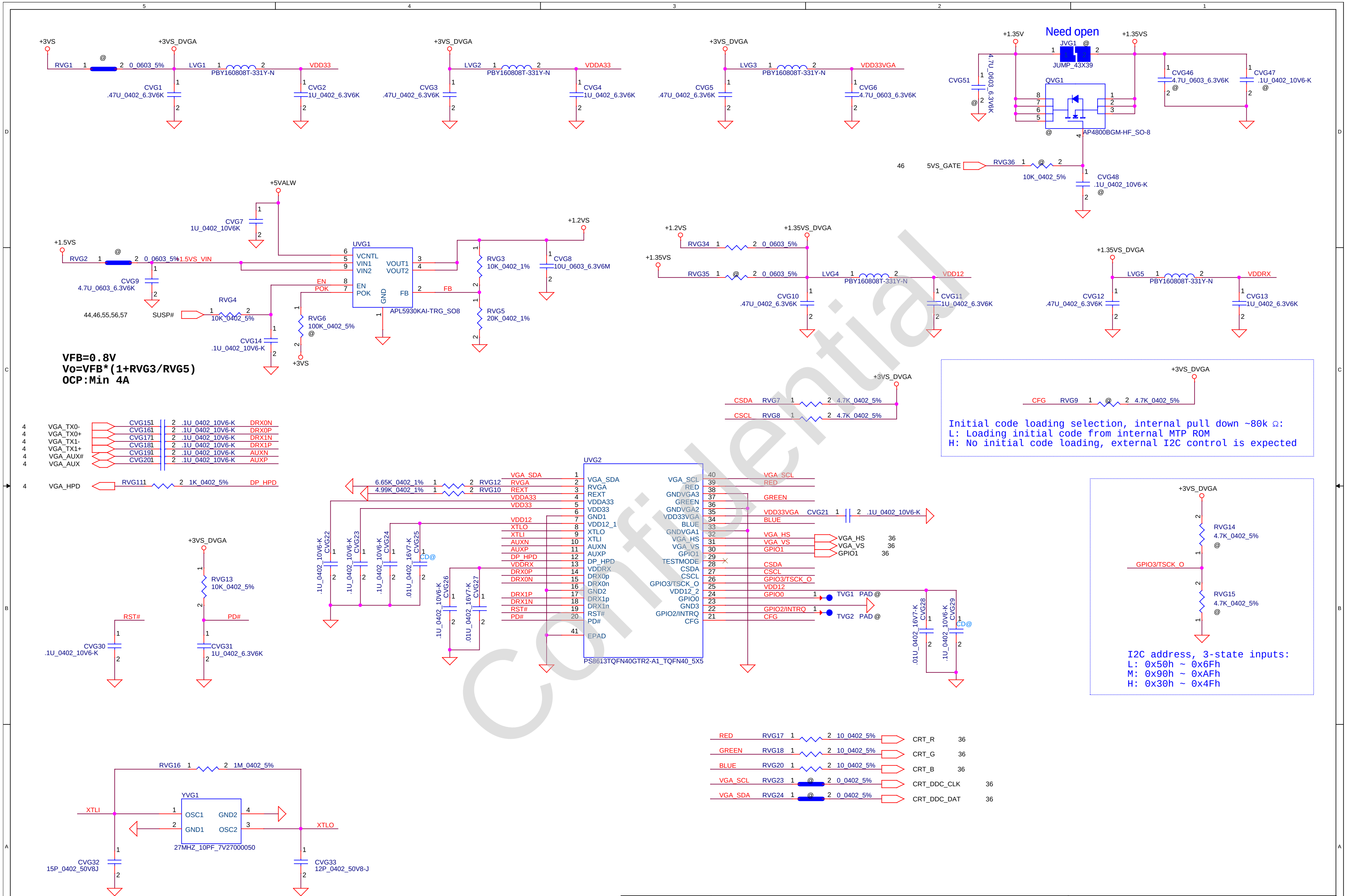
Title
HDMI_CONN

Size Custom
Document Number **ACLUA**
Rev 1.0

Date: Thursday, December 26, 2013 Sheet 34 of 59



VFB=0.8V
Vo=VFB*(1+RVG3/RVG5)
OCP:Min 4A

Initial code loading selection, internal pull down ~80k Ω:
L: Loading initial code from internal MTP ROM
H: No initial code loading, external I2C control is expected

I2C address, 3-state inputs:
L: 0x50h ~ 0x6Fh
M: 0x90h ~ 0xAFh
H: 0x30h ~ 0x4Fh

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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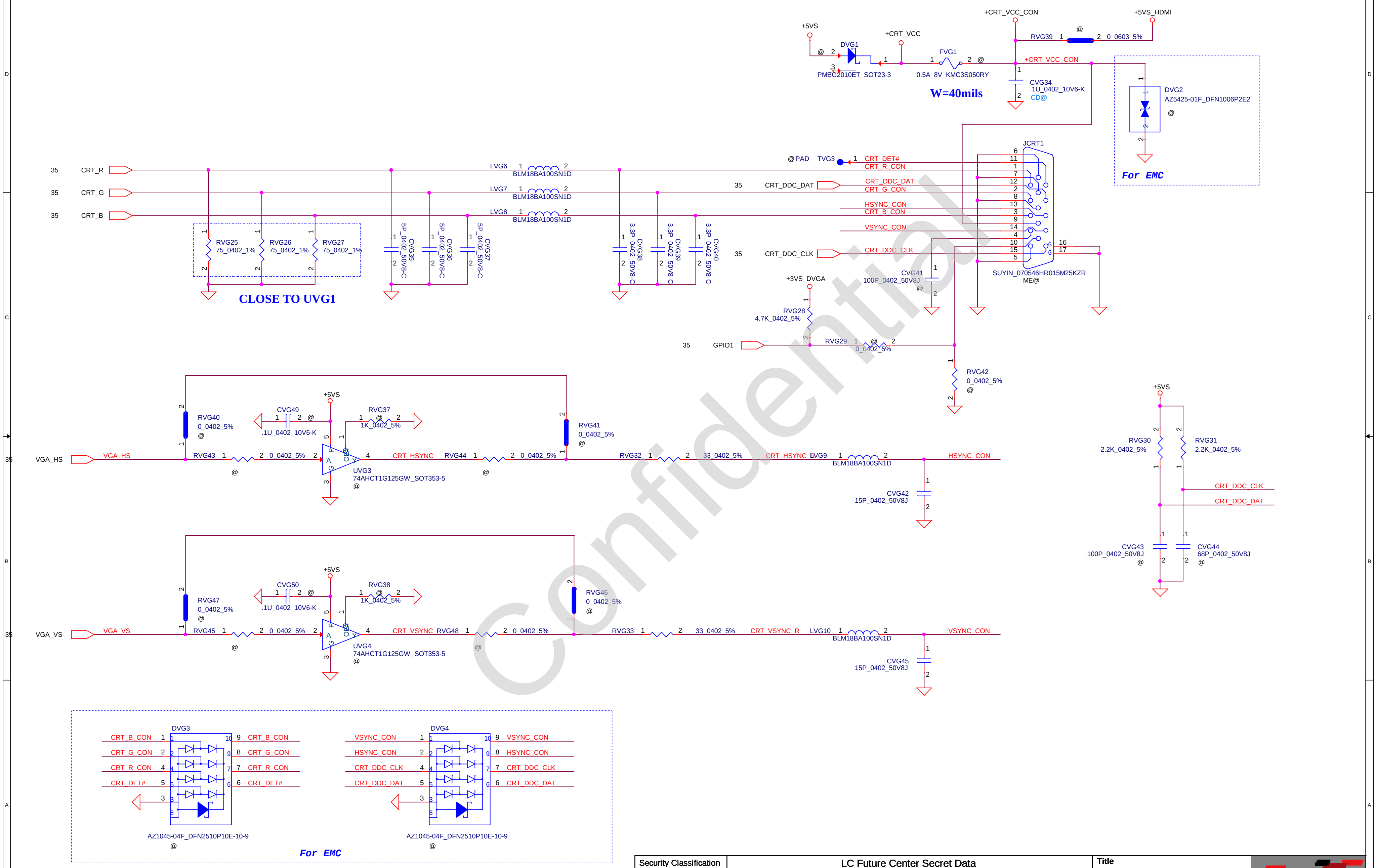
Title
DP to CRT Converter(PS8613)

Size	Document Number	Rev
Custom	ACLUA	1.0

Date: Thursday, December 26, 2013 Sheet 35 of 59

CRT Connector



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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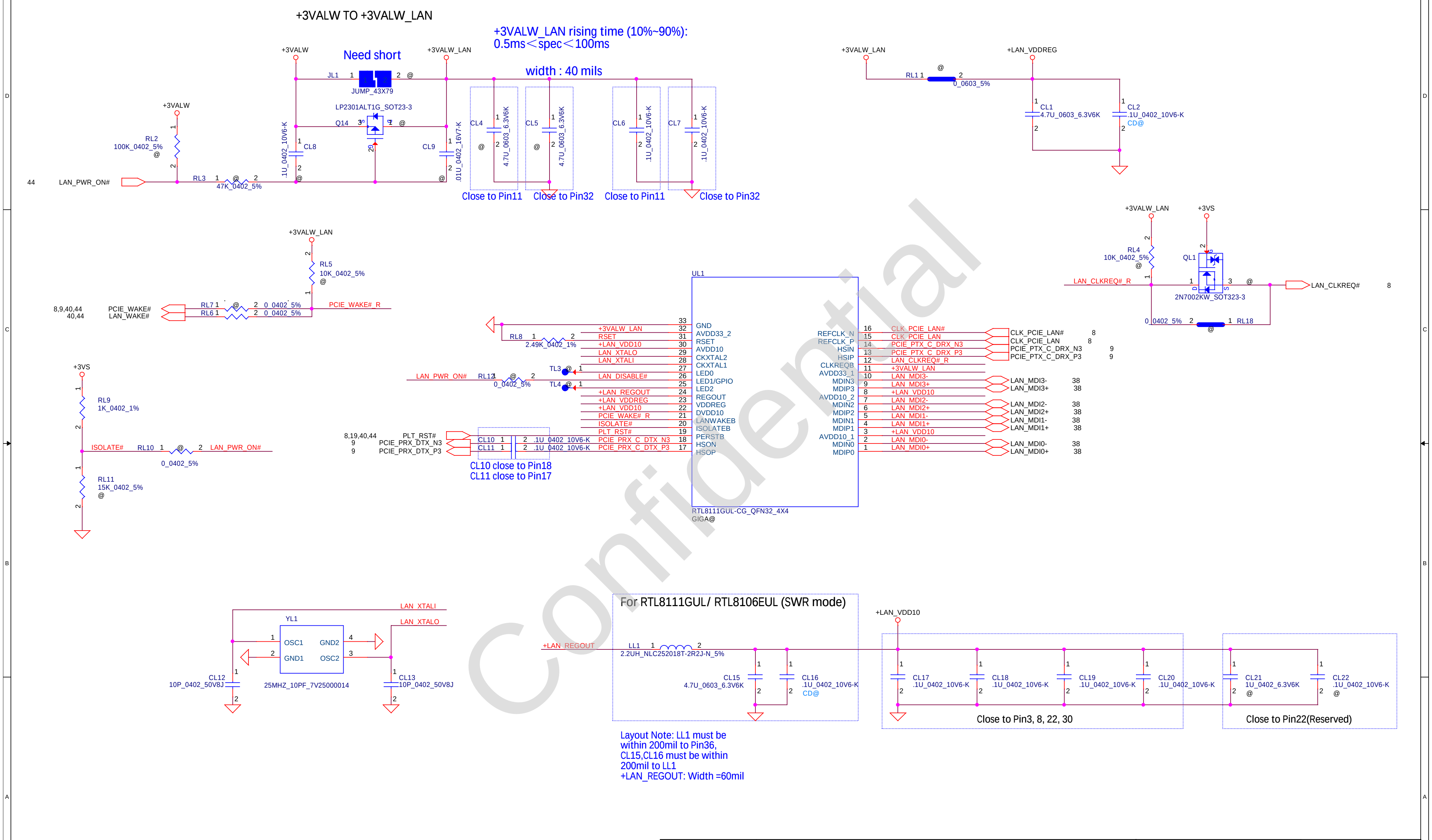
Title
CRT
Size Custom
Document Number ACLUA
Rev 1.0
Date: Thursday, December 26, 2013
Sheet 36 of 59



+3VALW_LAN rising time (10%~90%):
0.5ms＜spec＜100ms

Need short

width : 40 mils

Close to Pin11

Close to Pin32

Close to Pin11

Close to Pin32

CL10 close to Pin18
CL11 close to Pin17

For RTL8111GUL/ RTL8106EUL (SWR mode)

Close to Pin3, 8, 22, 30

Close to Pin22(Reserved)

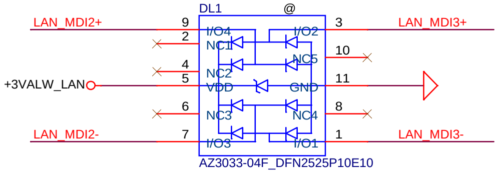
Layout Note: LL1 must be within 200mil to Pin36, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

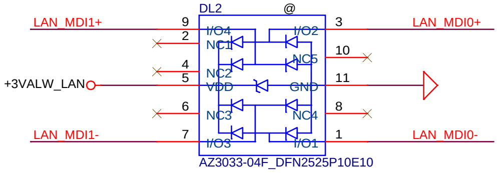
Title
LAN_RTL8111GUL/RTL8106EUL

Size: Custom
Document Number: ACLUA
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 37 of 59

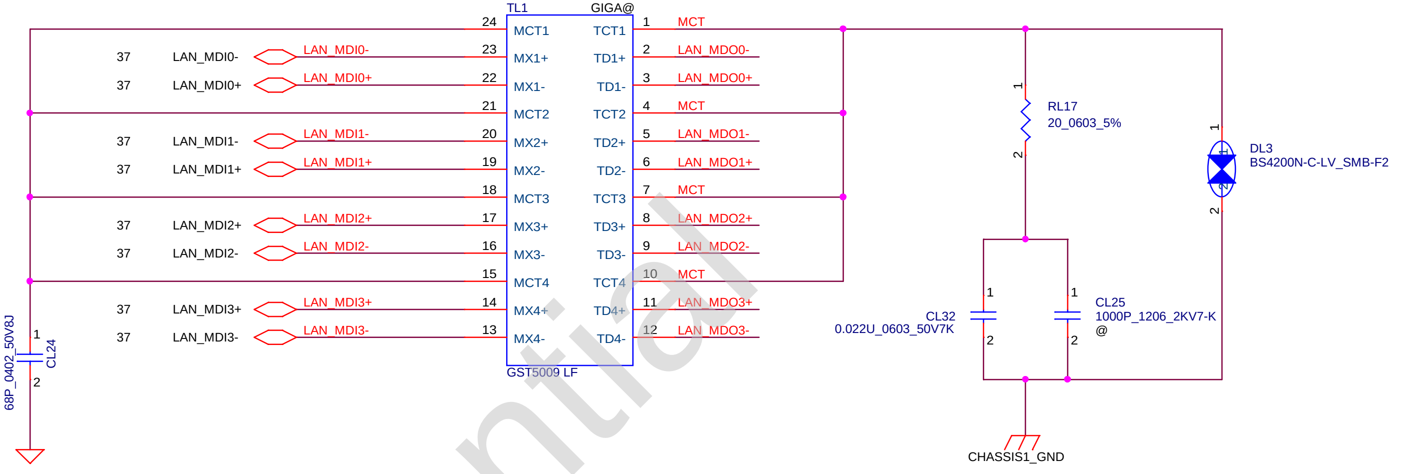
DL1/DL2
1'S PN:SC300003M00

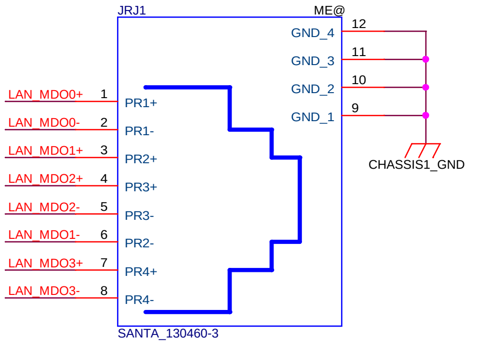


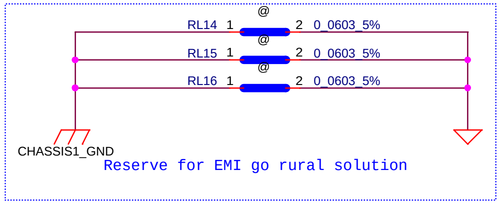
Place Close to TL1



Place Close to TL2







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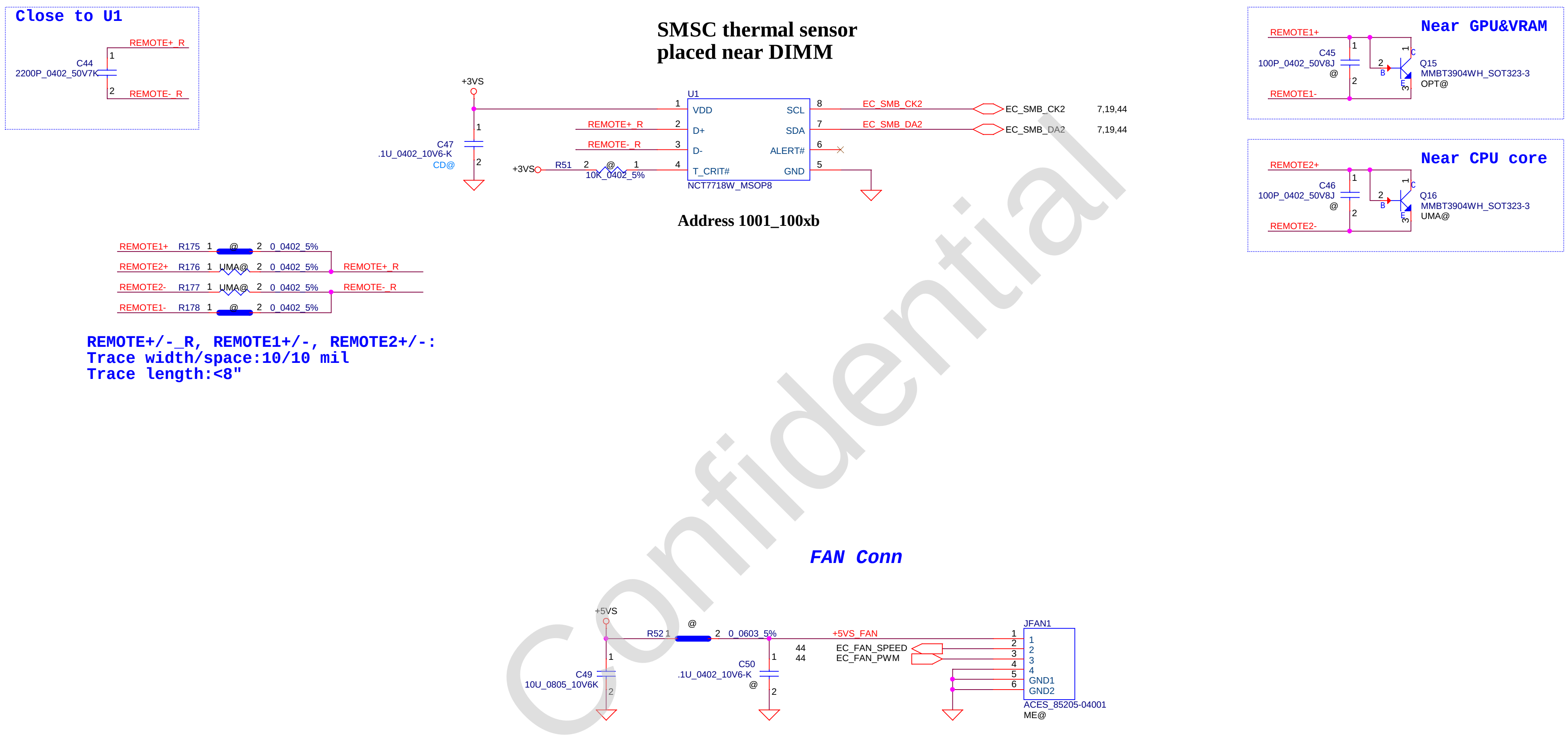
Title

LAN_Transformer

LCFC

Size	Document Number	Rev
B	ACLUA	1.0

Date: Friday, December 27, 2013 Sheet 38 of 59



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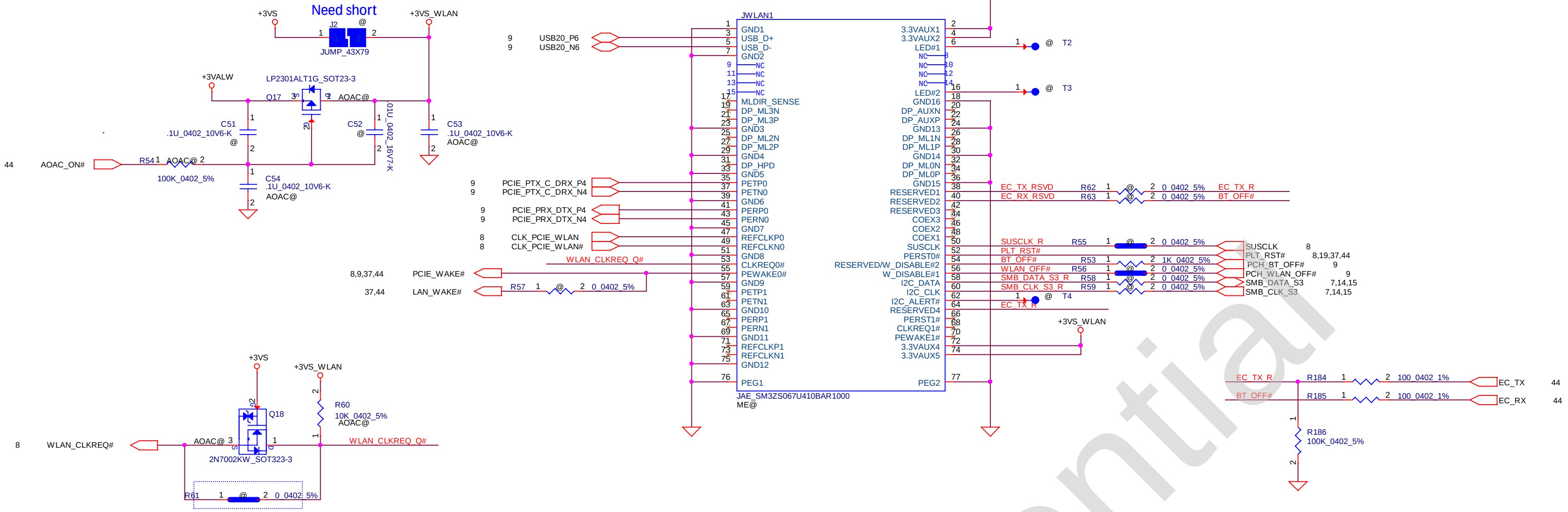
Title
Thermal sensor/FAN CONN

Size	Document Number	Rev
Custom	**ACLUA**	1.0

Date: Thursday, December 26, 2013 Sheet 39 of 59

Mini-Express Card(WLAN/WiMAX)



If support AOAC, NC R61;
if not support AOAC, stuff R61.

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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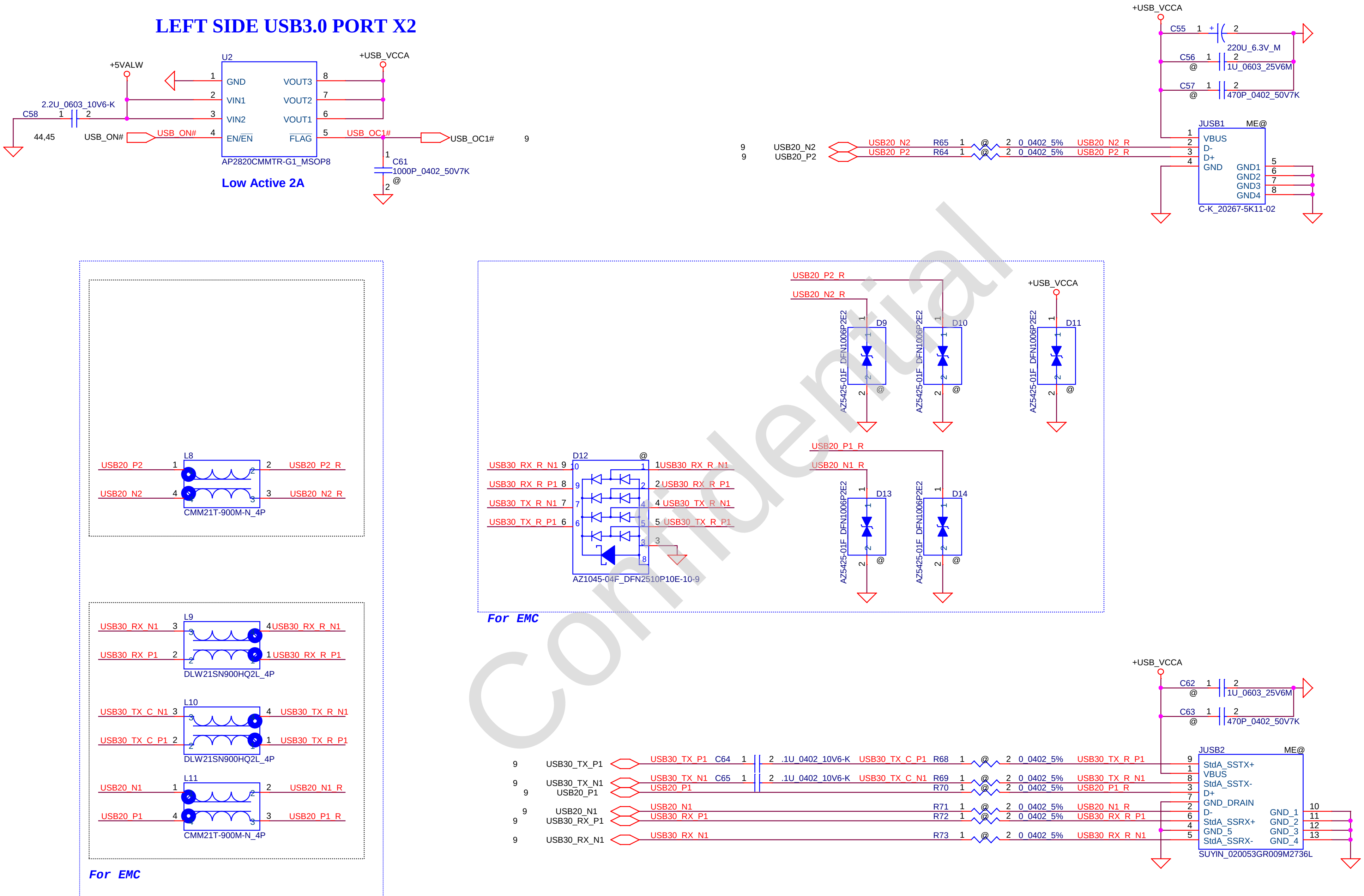
Title
NGFF WLAN

Size	Document Number	Rev
Custom	ACLUA	1.0

Date: Thursday, December 26, 2013 Sheet 40 of 59

LEFT SIDE USB3.0 PORT X2



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Issued Date	2013/08/08	Deciphered Date	2013/08/05

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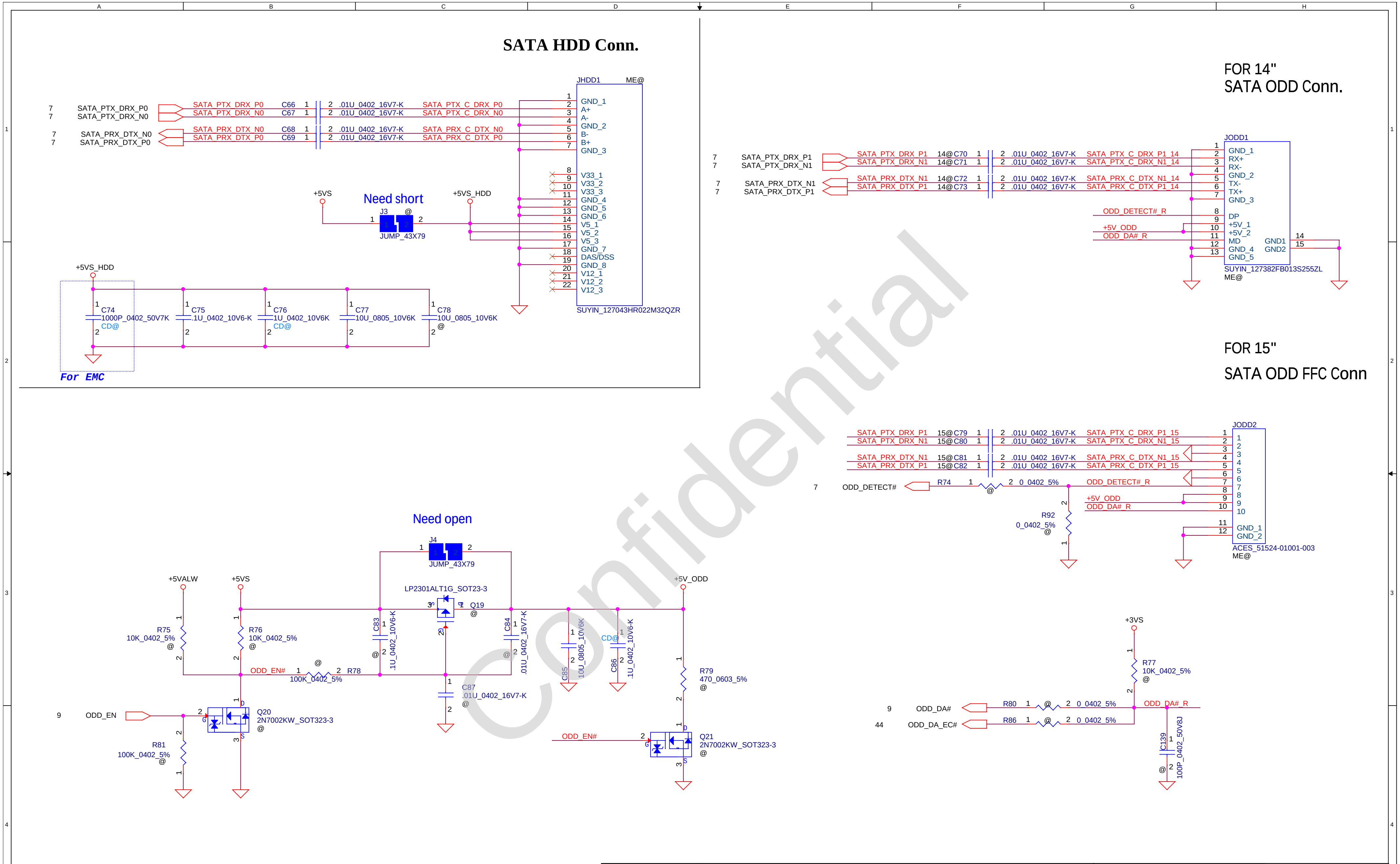
Title
USB2.0/USB3.0 PORT (LEFT)

Size	Document Number	Rev
Custom	ACLUA	1.0

Date: Thursday, December 26, 2013 Sheet 41 of 59



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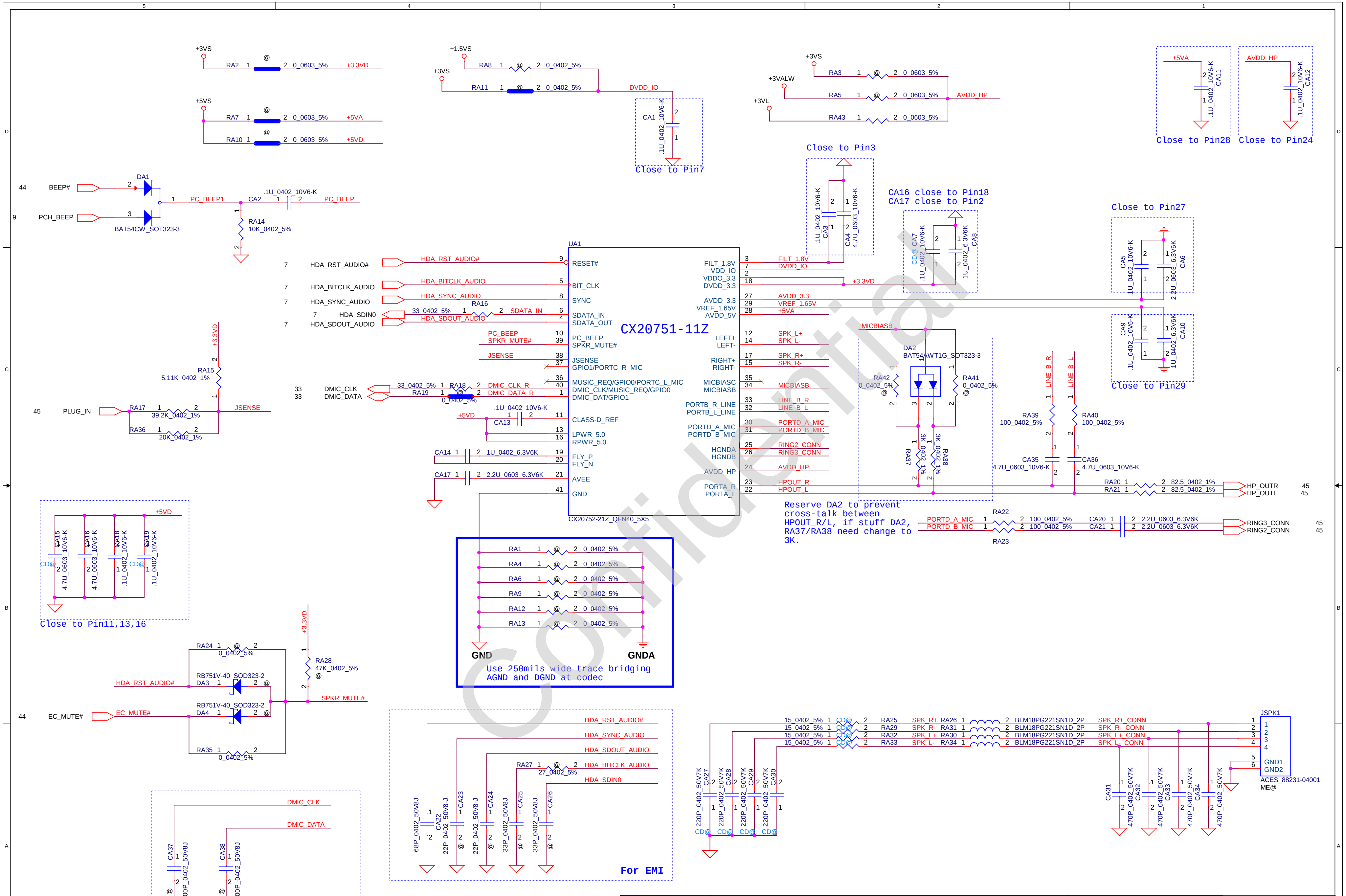
Title
HDD/ODD CONN
LCFC

Size	Document Number	Rev
Custom	ACLUA	1.0

Date: Thursday, December 26, 2013 Sheet 42 of 59



Close to Pin28

Close to Pin24

Close to Pin7

Close to Pin3

CA16 close to Pin18
CA17 close to Pin2

Close to Pin27

Close to Pin29

Reserve DA2 to prevent cross-talk between HPOUT_R/L, if stuff DA2, RA37/RA38 need change to 3K.

Close to Pin11,13,16

Use 250mils wide trace bridging AGND and DGND at codec

For EMI

For EMI

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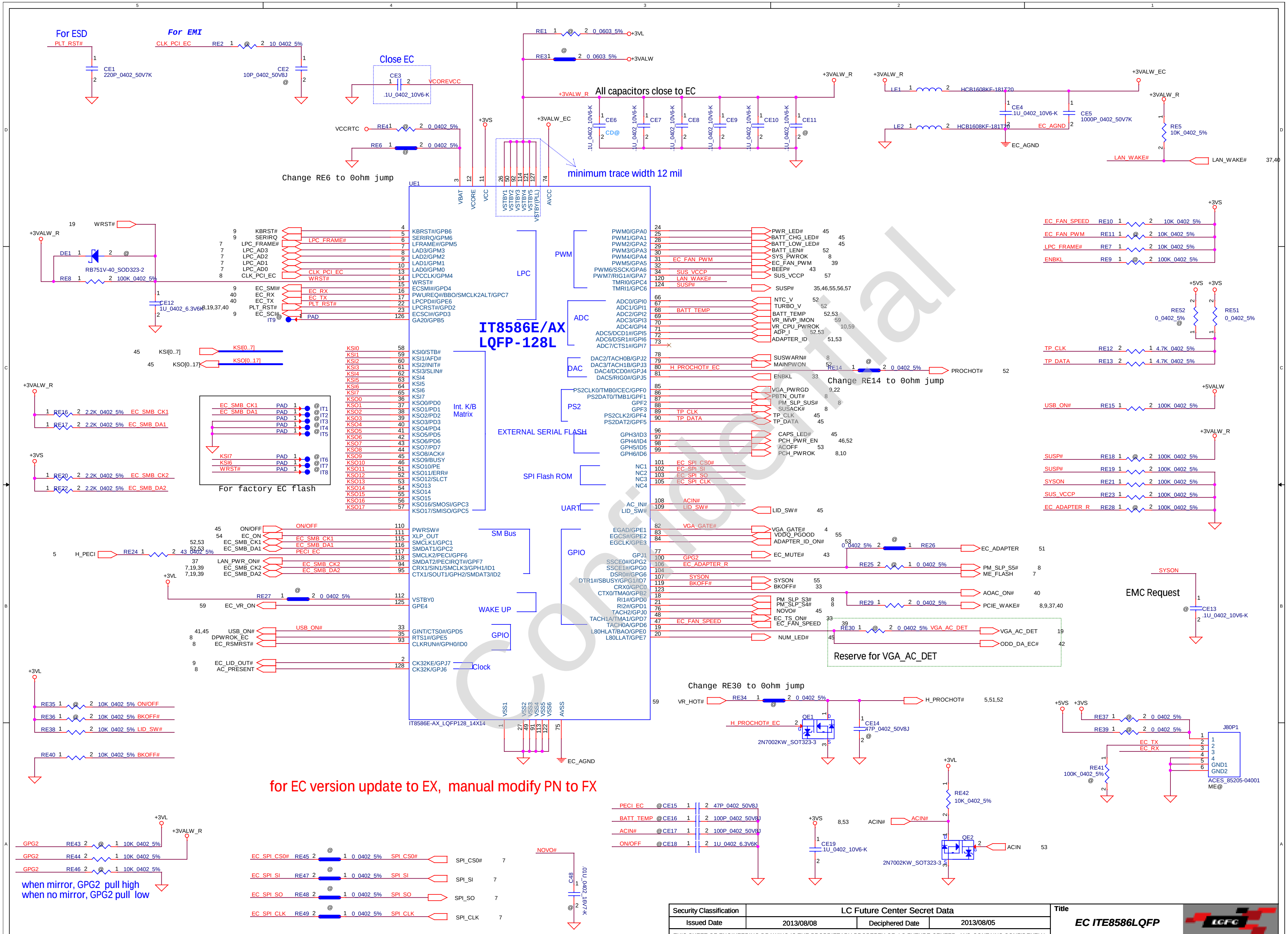
Title
Codec_CX20752

Size Custom
Document Number ACLUA
Rev 1.0

Date: Thursday, December 26, 2013 Sheet 43 of 59



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Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title
EC ITE8586LQFP

LCFC

Size	Document Number	Rev
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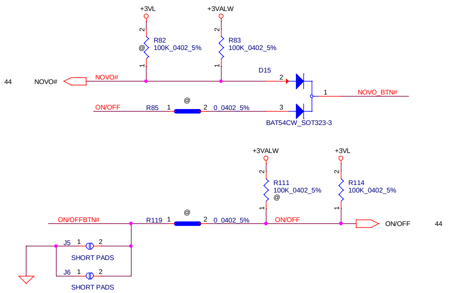
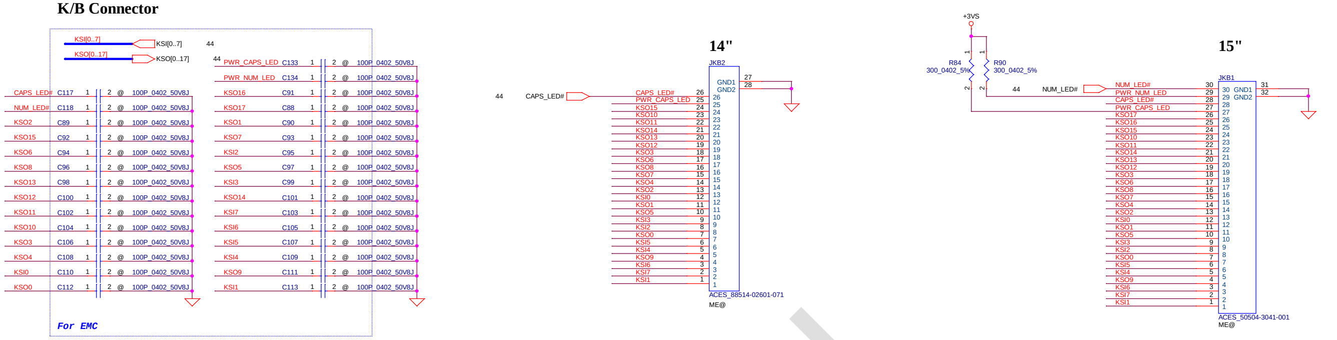
Date: Tuesday, December 31, 2013 | Sheet 44 of 59

ON/OFF switch

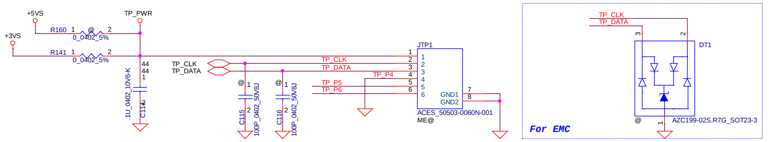


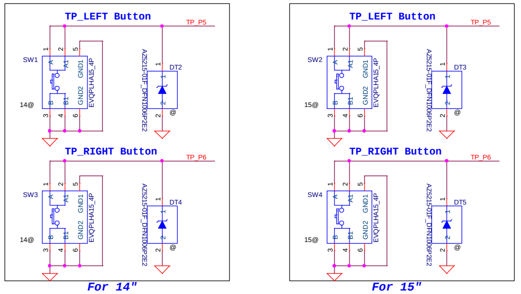
K/B Connector



	14"	15"
KB_1	KSI1_14	KSO0_15
KB_2	KSI7_14	KSI2_15
KB_3	KSI6_14	KSI3_15
KB_4	KSO9_14	KSO5_15
KB_5	KSI4_14	KSO1_15
KB_6	KSI5_14	KSI0_15
KB_7	KSO0_14	KSO2_15
KB_8	KSI2_14	KSO4_15
KB_9	KSI3_14	KSO7_15
KB_10	KSO5_14	KSO8_15
KB_11	KSO1_14	KSO6_15
KB_12	KSI0_14	KSO3_15
KB_13	KSO2_14	KSO12_15
KB_14	KSO4_14	KSO13_15
KB_15	KSO7_14	KSO14_15
KB_16	KSO8_14	KSO11_14
KB_17	KSO6_14	KSO10_15
KB_18	KSO3_14	KSO15_15
KB_19	KSO12_14	KSO16_15
KB_20	KSO13_14	KSO17_15
KB_21	KSO14_14	KB_LED_PWR_15
KB_22	KSO11_14	CAPS_LED#_15
KB_23	KSO10_14	VDD_15
KB_24	KSO15_14	NUM_LED#_15

TP/B Connector

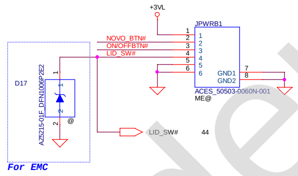




For 14"	
1	VDD
2	CLK
3	DAT
4	GND
5	TP-L
6	TP-R

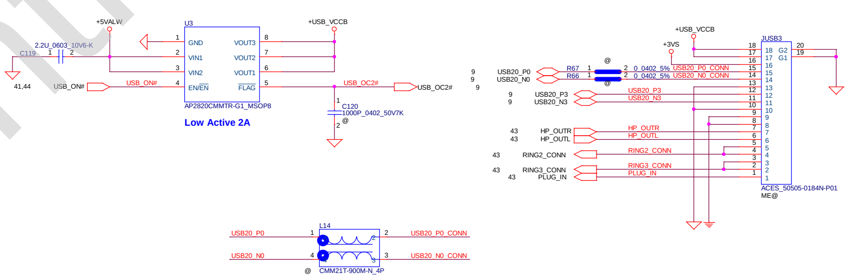
For 15"	
1	VDD
2	CLK
3	DAT
4	GND
5	TP-L
6	TP-R

PWR/B Connector

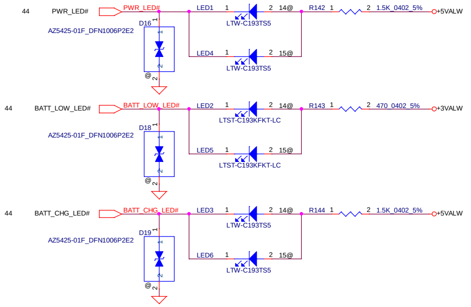


USB I/O Connector

Right Side USB2.0 Port X 1 (USB/B)



LED



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Title
KBD/PWR/IO/LED/TP Conn.

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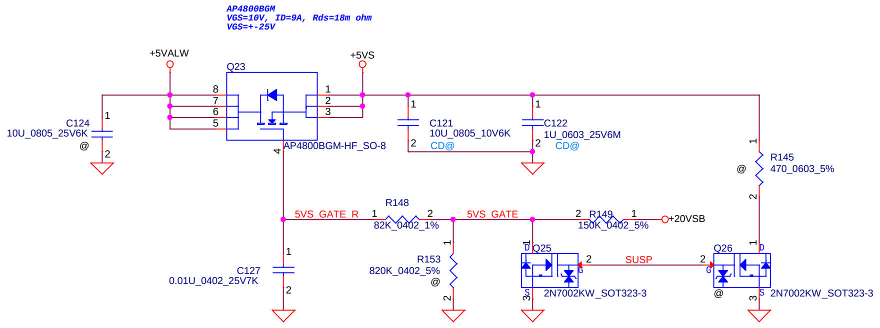
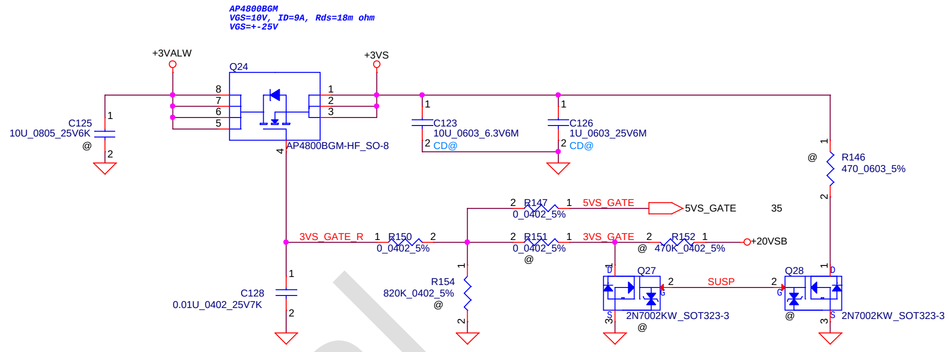
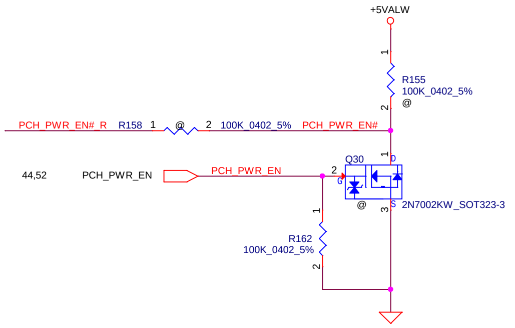
Date: Thursday, December 26, 2013 Sheet 45 of 59

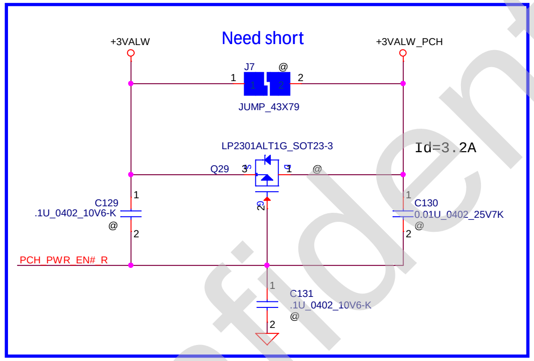
+5VALW to +5VS

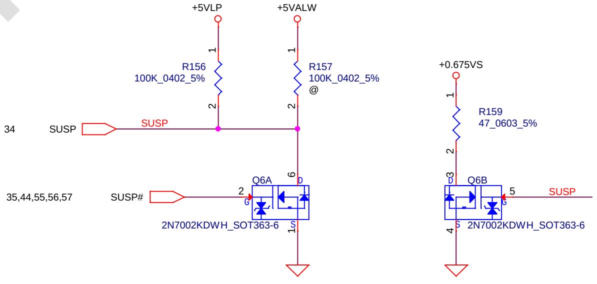


+3VALW to +3VS









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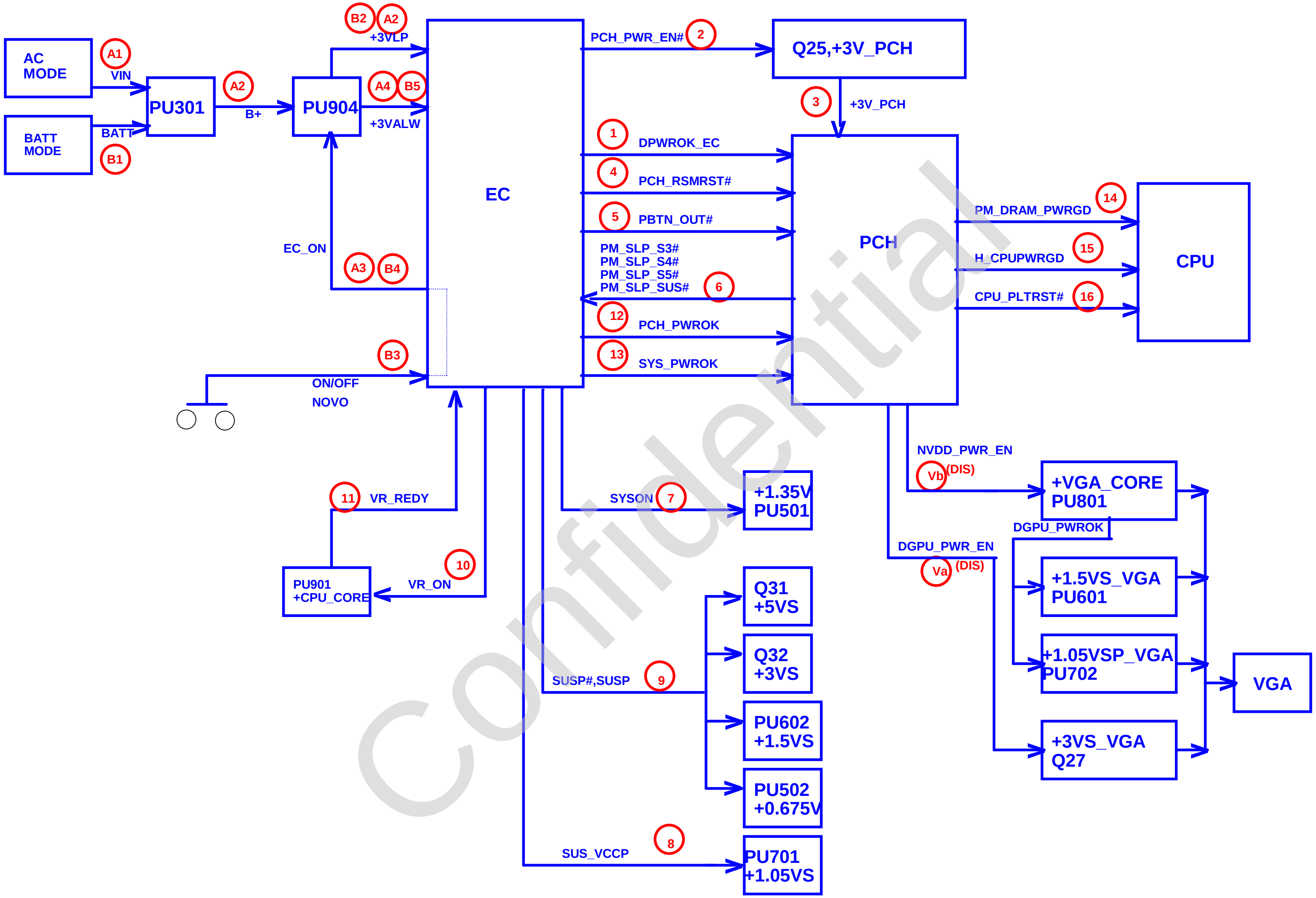
Title
DC V TO VS INTERFACE
Size Custom
Document Number ACLUA
Rev 1.0
Date: Thursday, December 26, 2013
Sheet 46 of 59



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title

Power sequence Block

Size	Document Number	Rev
Custom	**ACLUA**	1.0

Date: Thursday, December 26, 2013 Sheet 47 of 59

LAN chip

UL1 100M@
RTL8106EUL-CG
SA000060Q00

Transformer

TL1 100M@
TST1284A LF
SP050008C00

X76 BOM

ZZZ2 H4GX8T@ Hynix X7603212001
ZZZ3 M4GX8T@ Micron X7603212002
ZZZ4 H2GX4T@ Hynix X7603212003
ZZZ5 H2GX4M@ Hynix X7603212051
ZZZ6 M2GX4M@ Micron X7603212052
ZZZ7 M2GX4T@ Micron X7603212004
ZZZ8 S4GX8T@ Samsung X7603212054
ZZZ9 S2GX4T@ Samsung X7603212053

PCB_MB

ZZZ10 14@ PCB PN DAZ0TY00100
ZZZ11 15@ PCB PN DAZ0TZ00100

UV1 N15VGM@ NV N15V-GM GPU SA000064R00
RV155 N15VGM@ 10K_0402_1% SD03410028J
RV159 N15VGM@ 10K_0402_1% SD03410028J
RV160 N15VGM@ 10K_0402_1% SD03410028J
RV161 N15VGM@ 10K_0402_1% SD03410028J

Hynix 4G---256X16 *8 pcs X7603212001

UV5 H4T@ H5TC4G63AFR-11C SA00005YL00
UV6 H4T@ H5TC4G63AFR-11C SA00005YL00
UV7 H4T@ H5TC4G63AFR-11C SA00005YL00
UV8 H4T@ H5TC4G63AFR-11C SA00005YL00
RC100 H4T@ 10K_0402_5% SD02810028J
UV9 H4T@ H5TC4G63AFR-11C SA00005YL00
UV10 H4T@ H5TC4G63AFR-11C SA00005YL00
UV11 H4T@ H5TC4G63AFR-11C SA00005YL00
UV12 H4T@ H5TC4G63AFR-11C SA00005YL00
RV159 H4T@ 20K_0402_1% SD03420028J

Hynix 2G---256X16 *4 pcs X7603212051

UV5 H2M@ H5TC4G63AFR-11C SA00005YL00
UV6 H2M@ H5TC4G63AFR-11C SA00005YL00
UV7 H2M@ H5TC4G63AFR-11C SA00005YL00
UV8 H2M@ H5TC4G63AFR-11C SA00005YL00
RC107 H2M@ 10K_0402_5% SD02810028J
RV148 H2M@ 10K_0402_1% SD03410028J
RV151 H2M@ 10K_0402_1% SD03410028J
RV152 H2M@ 10K_0402_1% SD03410028J
RV154 H2M@ 10K_0402_1% SD03410028J

Micron 4G---256X16 *8 pcs X7603212002

UV5 M4T@ MT41J256M16HA-093G:E SA000060I10
UV6 M4T@ MT41J256M16HA-093G:E SA000060I10
UV7 M4T@ MT41J256M16HA-093G:E SA000060I10
UV8 M4T@ MT41J256M16HA-093G:E SA000060I10
RC100 M4T@ 10K_0402_5% SD02810028J
UV9 M4T@ MT41J256M16HA-093G:E SA000060I10
UV10 M4T@ MT41J256M16HA-093G:E SA000060I10
UV11 M4T@ MT41J256M16HA-093G:E SA000060I10
UV12 M4T@ MT41J256M16HA-093G:E SA000060I10
RV159 M4T@ 24.9K_0402_1% SD03424928J

Micron 2G---256X16 *4 pcs X7603212052

UV5 M2M@ MT41J256M16HA-093G:E SA000060I10
UV6 M2M@ MT41J256M16HA-093G:E SA000060I10
UV7 M2M@ MT41J256M16HA-093G:E SA000060I10
UV8 M2M@ MT41J256M16HA-093G:E SA000060I10
RC107 M2M@ 10K_0402_5% SD02810028J
RV146 M2M@ 10K_0402_1% SD03410028J
RV148 M2M@ 10K_0402_1% SD03410028J
RV149 M2M@ 10K_0402_1% SD03410028J
RV152 M2M@ 10K_0402_1% SD03410028J

Hynix 2G---256X16 *4 pcs X7603212003

UV5 H2T@ H5TC4G63AFR-11C SA00005YL00
UV6 H2T@ H5TC4G63AFR-11C SA00005YL00
UV7 H2T@ H5TC4G63AFR-11C SA00005YL00
UV8 H2T@ H5TC4G63AFR-11C SA00005YL00
RC107 H2T@ 10K_0402_5% SD02810028J
RV159 H2T@ 20K_0402_1% SD03420028J

Micron 2G---256X16 *4 pcs X7603212004

UV5 M2T@ MT41J256M16HA-093G:E SA000060I10
UV6 M2T@ MT41J256M16HA-093G:E SA000060I10
UV7 M2T@ MT41J256M16HA-093G:E SA000060I10
UV8 M2T@ MT41J256M16HA-093G:E SA000060I10
RC107 M2T@ 10K_0402_5% SD02810028J
RV159 M2T@ 24.9K_0402_1% SD03424928J

Samsung 4G---256X16 *8 pcs X7603212054

UV5 S4T@ K4W4G1646D-BC1A SA000063F10
UV6 S4T@ K4W4G1646D-BC1A SA000063F10
UV7 S4T@ K4W4G1646D-BC1A SA000063F10
UV8 S4T@ K4W4G1646D-BC1A SA000063F10
RC100 S4T@ 10K_0402_5% SD02810028J
UV9 S4T@ K4W4G1646D-BC1A SA000063F10
UV10 S4T@ K4W4G1646D-BC1A SA000063F10
UV11 S4T@ K4W4G1646D-BC1A SA000063F10
UV12 S4T@ K4W4G1646D-BC1A SA000063F10
RV159 S4T@ 30.1K_0402_1% SD03430128J

Samsung 2G---256X16 *4 pcs X7603212053

UV5 S2T@ K4W4G1646D-BC1A SA000063F10
UV6 S2T@ K4W4G1646D-BC1A SA000063F10
UV7 S2T@ K4W4G1646D-BC1A SA000063F10
UV8 S2T@ K4W4G1646D-BC1A SA000063F10
RC107 S2T@ 10K_0402_5% SD02810028J
RV159 S2T@ 30.1K_0402_1% SD03430128J

PR9440 27K_0402_1% N15VGM@
PR9434 7.5K_0402_1% N15VGM@
PR9436 0_0402_5% N15VGM@
PR9437 6.2K_0402_1% N15VGM@
PR9431 1.74K_0402_1% N15VGM@
PC1277 5600P_0402_25V7-K N15VGM@

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Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title
Virtual symbol

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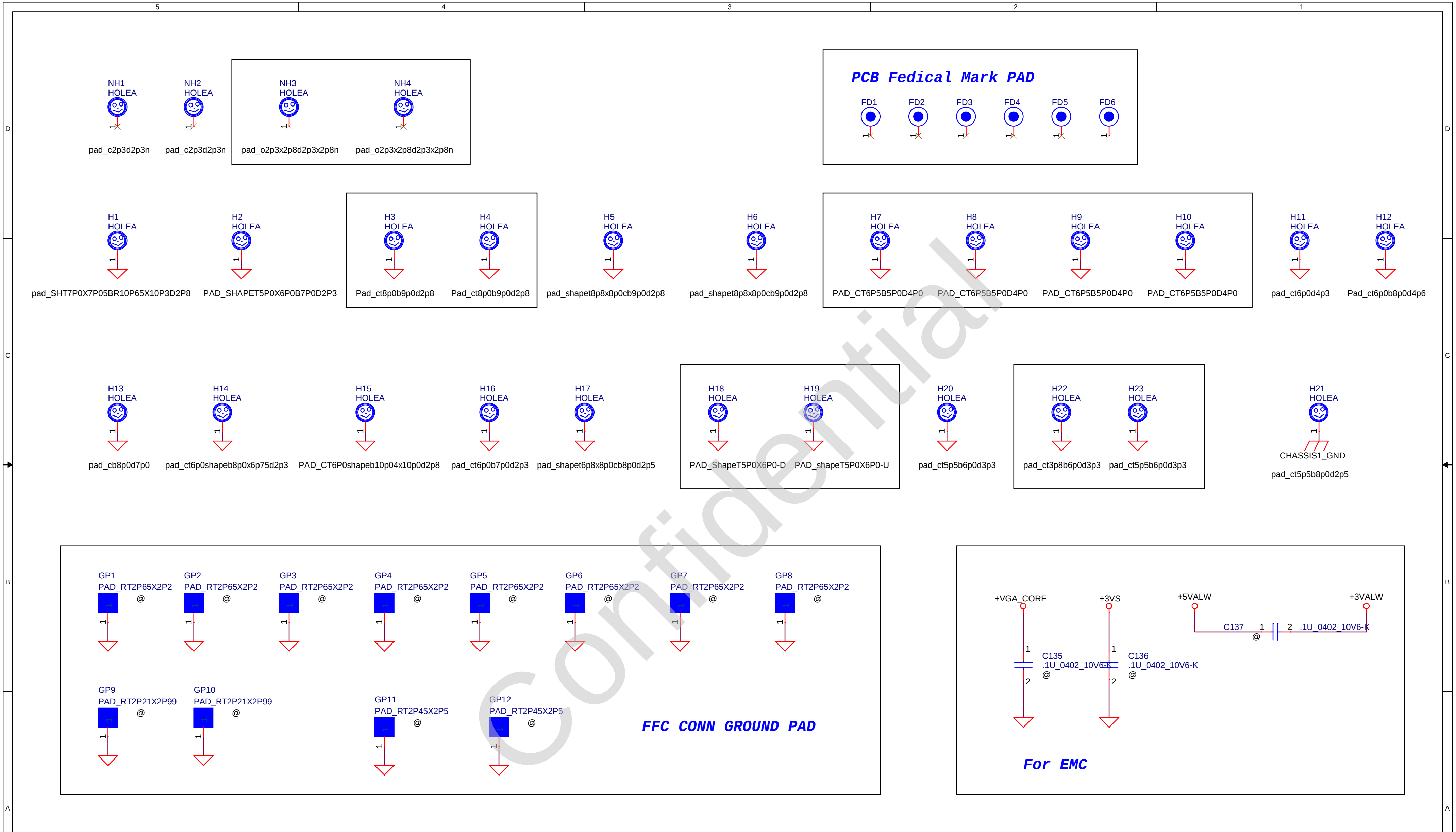
Date: Tuesday, December 31, 2013 Sheet 48 of 59



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Issued Date	2013/08/08	Deciphered Date	2013/08/05

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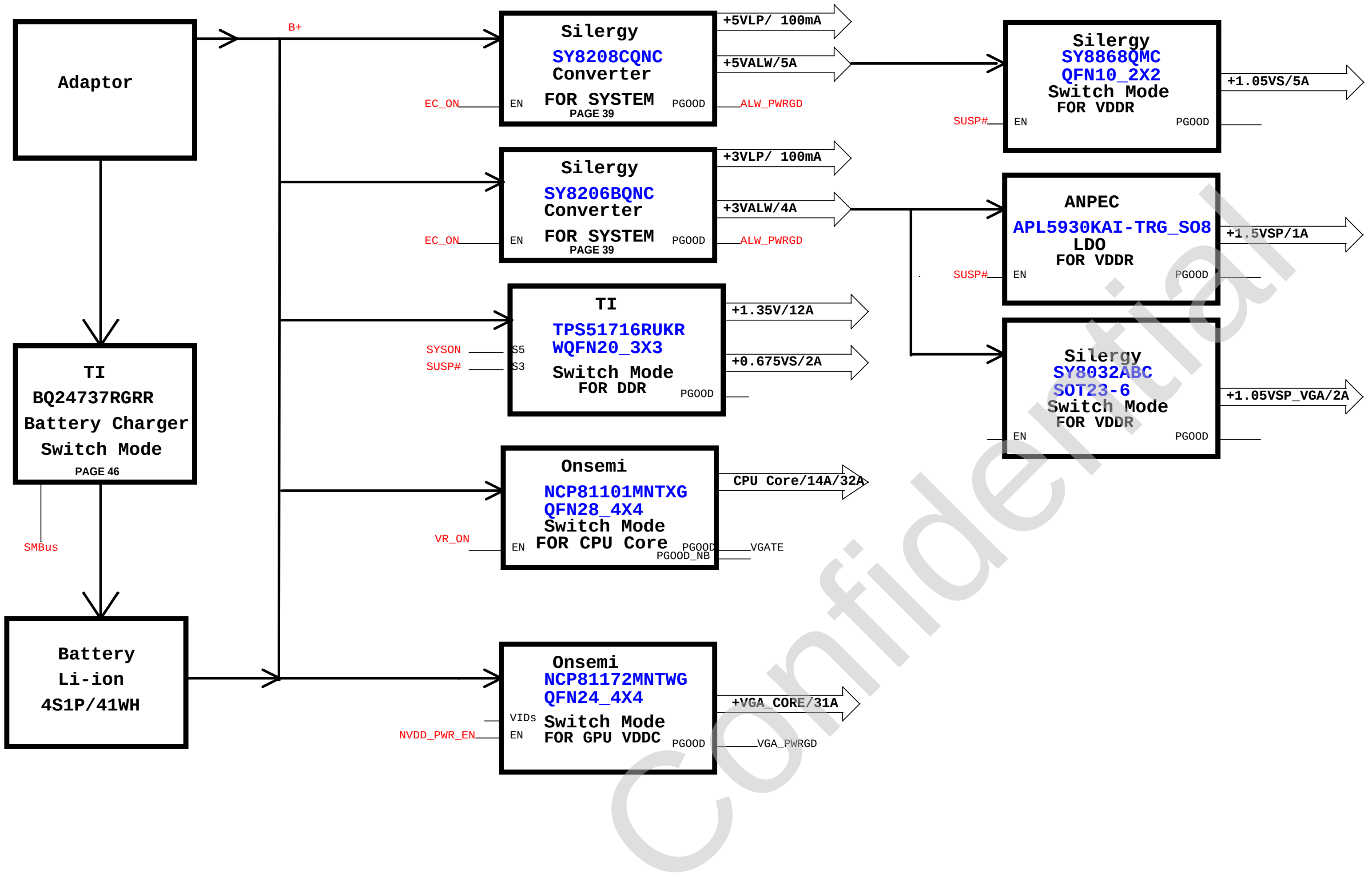
Title
Hole

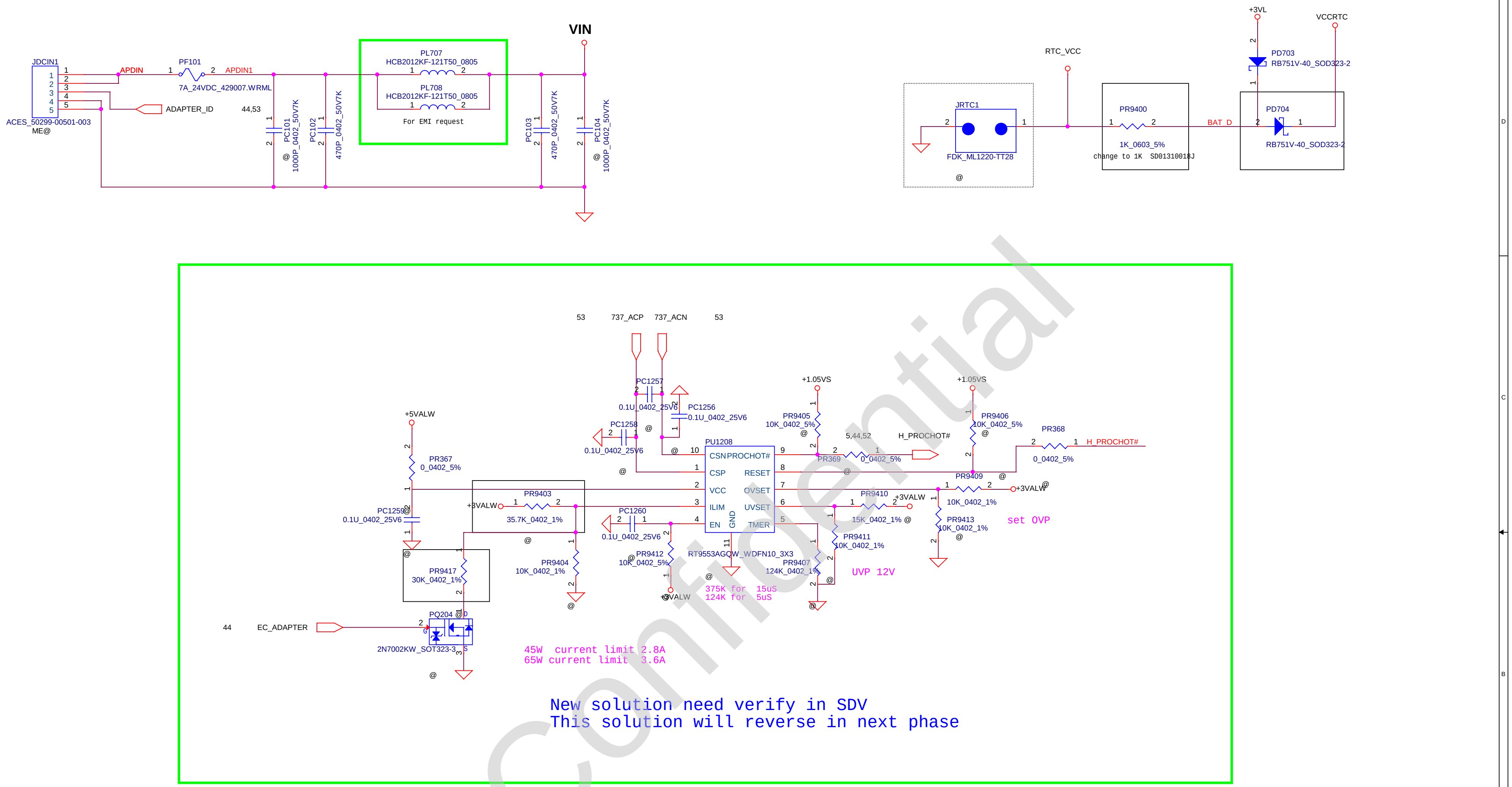
Size: B
Document Number: **ACLUA**
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 49 of 59



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title
Power Diagram

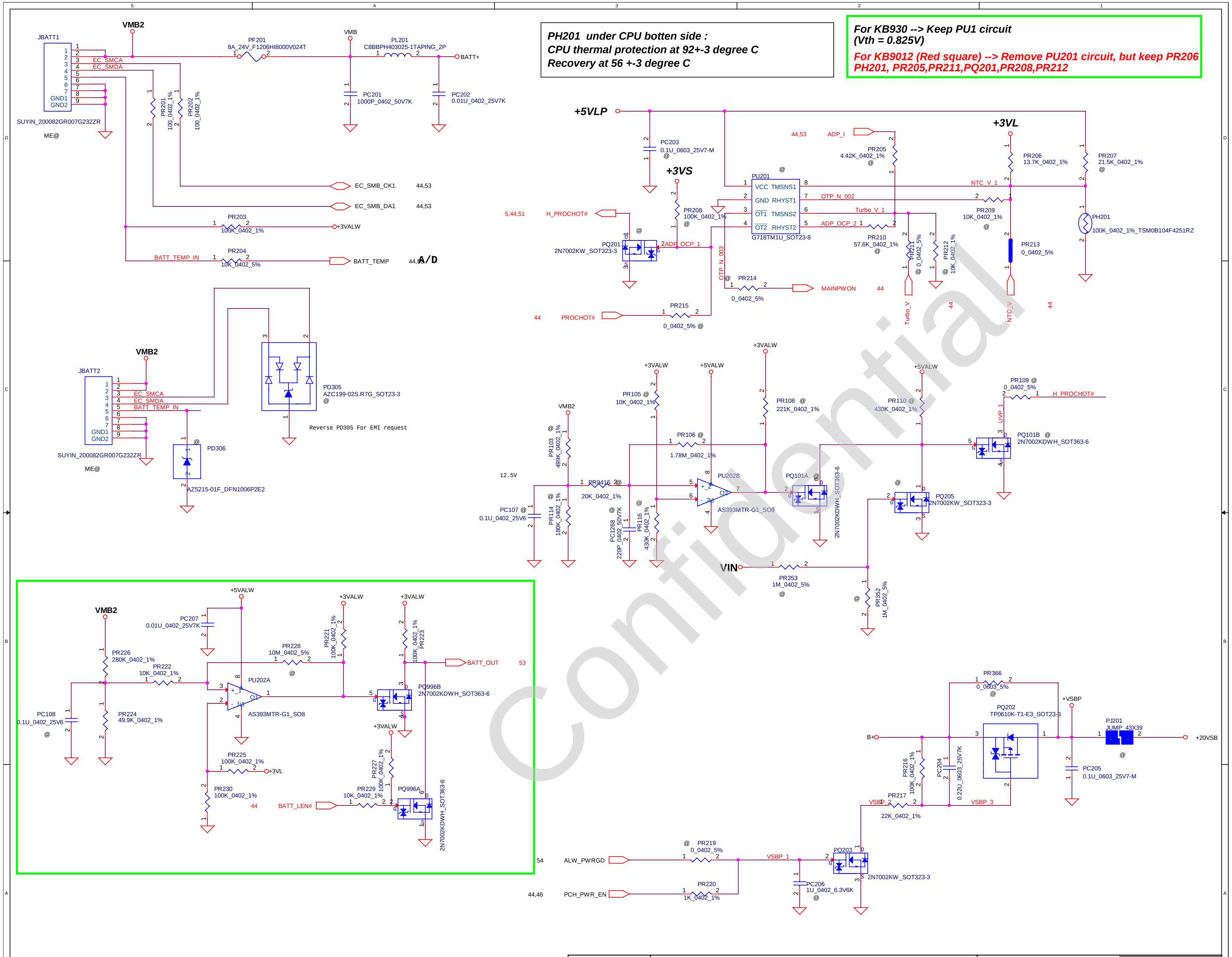
Size: Custom
Document Number: ACLUA
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 50 of 59



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title
DCIN / RTC

Size: Custom
Document Number: **ACLUA**
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 51 of 59



PH201 under CPU botten side :
CPU thermal protection at 92+-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205,PR211,PQ201,PR208,PR212

Security Classification	LC Future Center Secret Data		Title
Issued Date	2013/08/08	Deciphered Date 2013/08/05	**BATTERY CONN/OTP**

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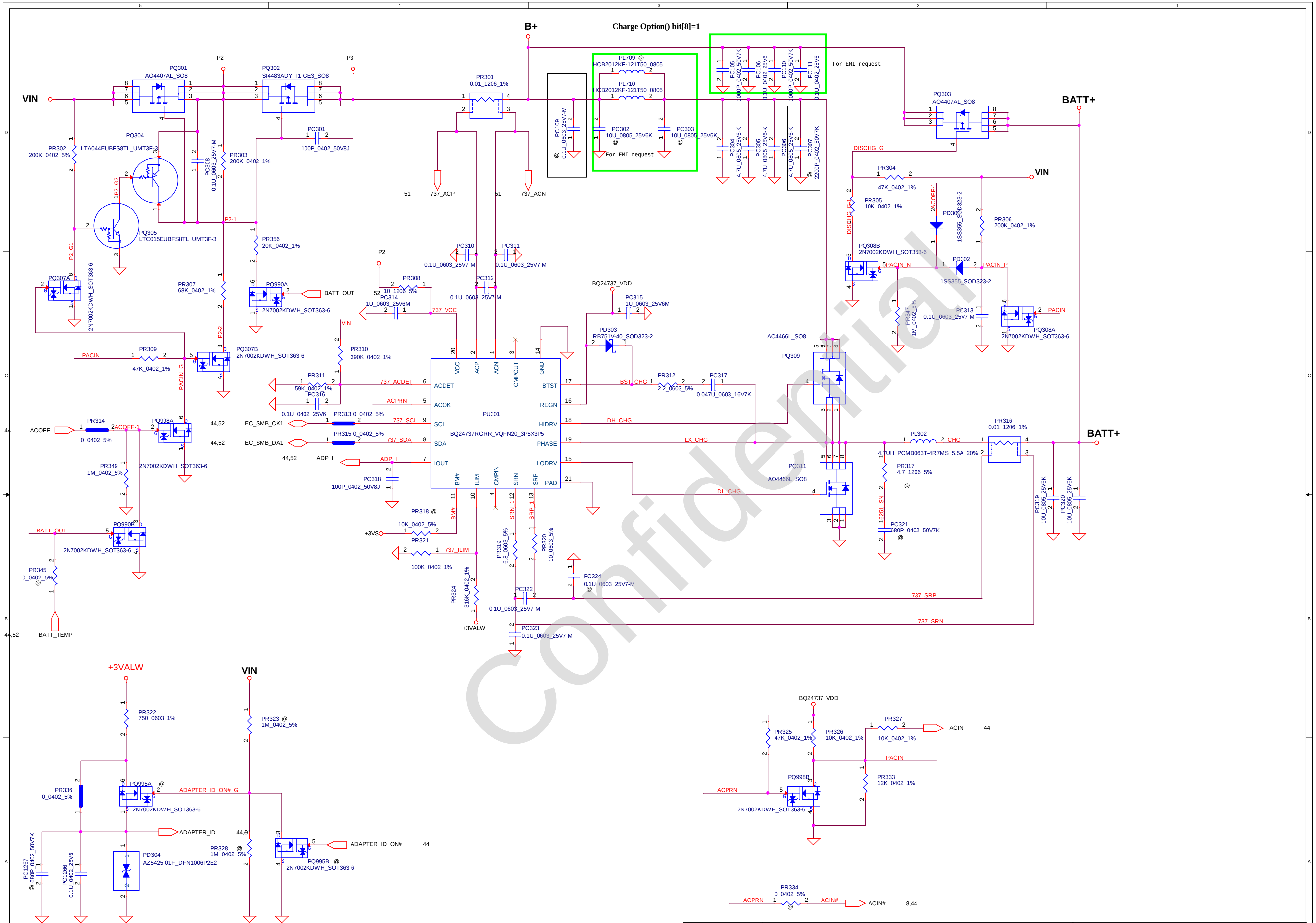
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 52 of 59



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Title
CHARGER

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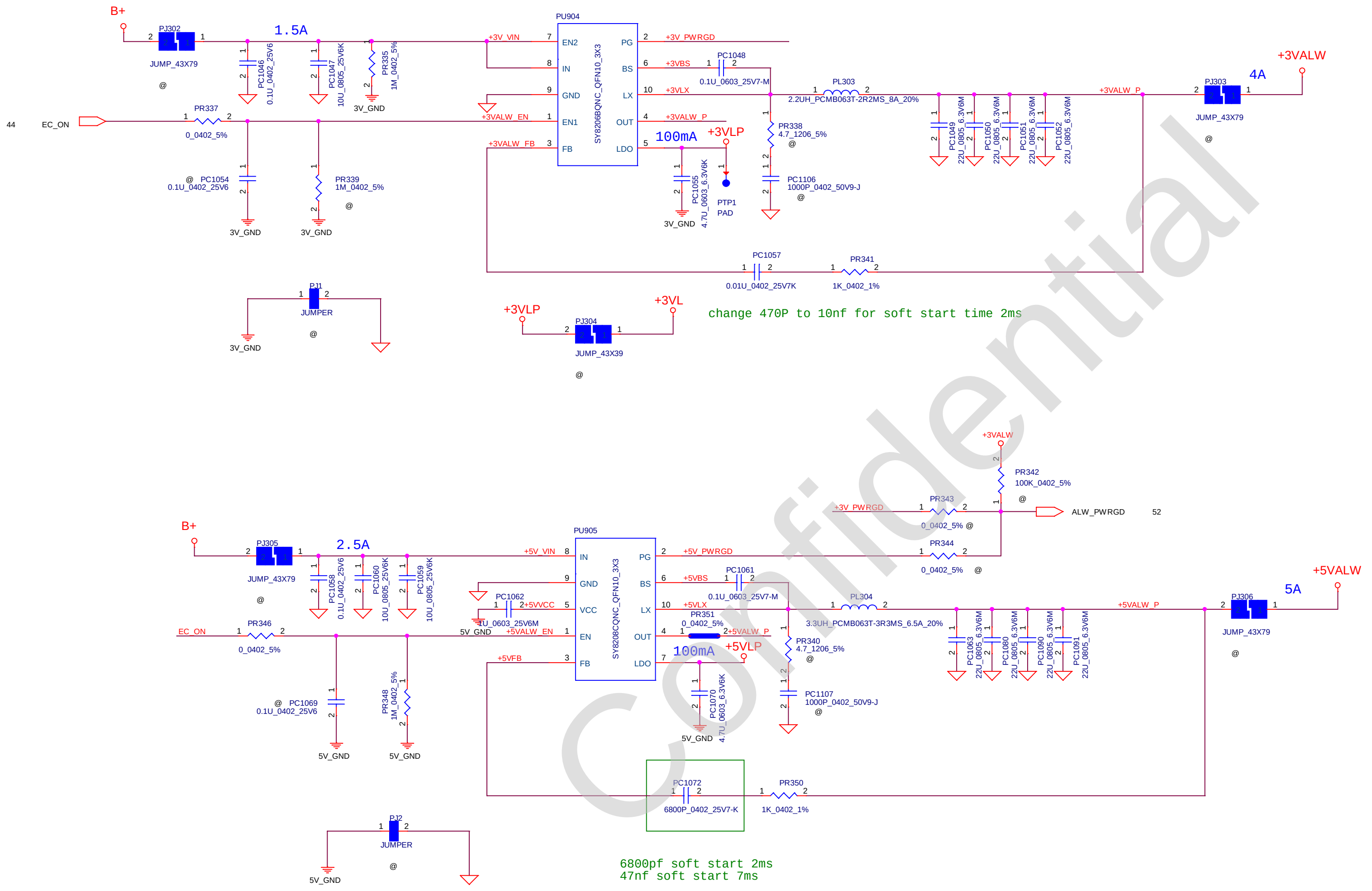
Date: Thursday, December 26, 2013 | Sheet 53 of 59



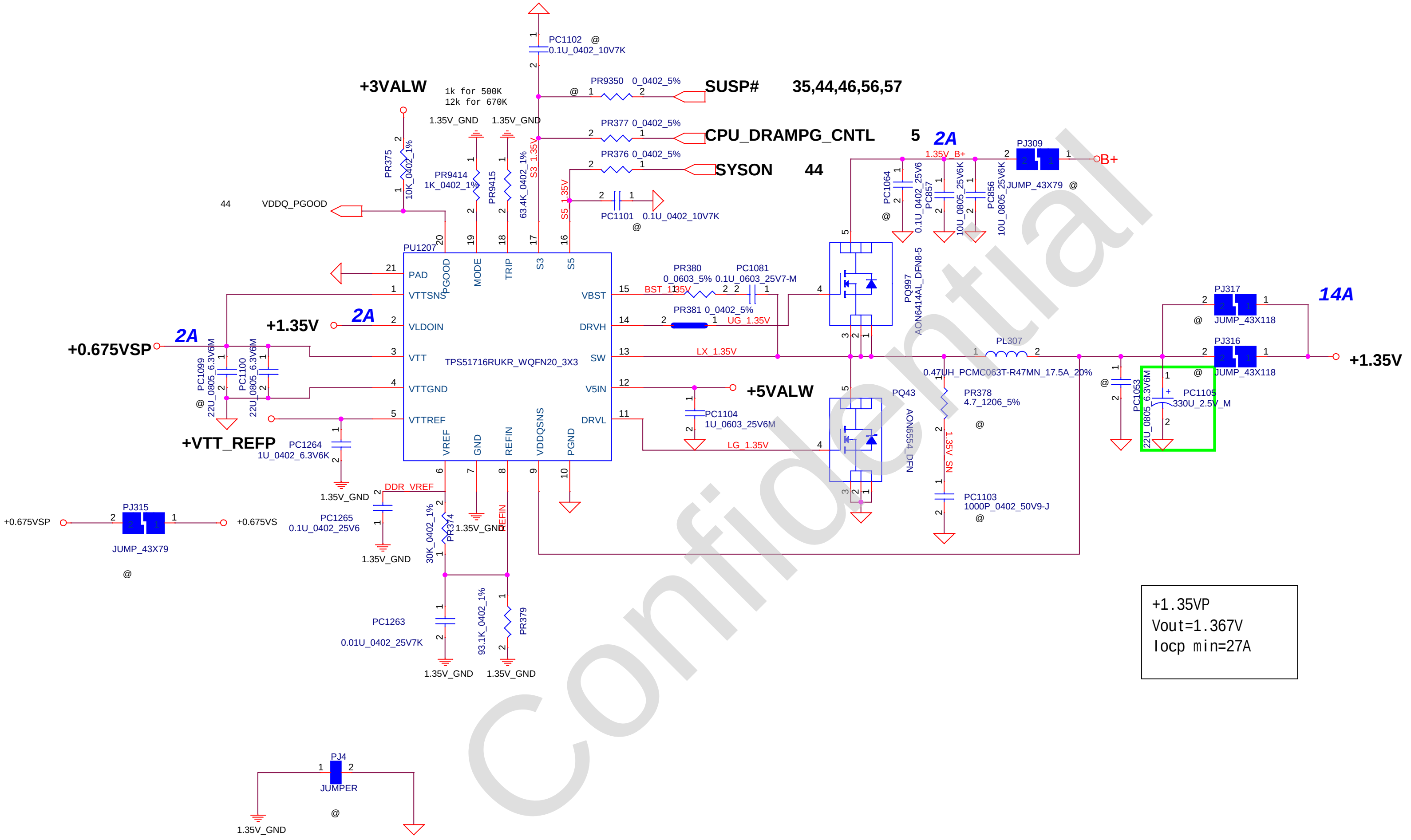
change 470P to 10nf for soft start time 2ms

6800pf soft start 2ms
47nf soft start 7ms

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title
PWR_3VALW/5VALW

Size: C
Document Number: **ACLUA**
Rev: 1.0
Date: Thursday, December 26, 2013
Sheet 54 of 59



+1.35VP
Vout=1.367V
Iocp min=27A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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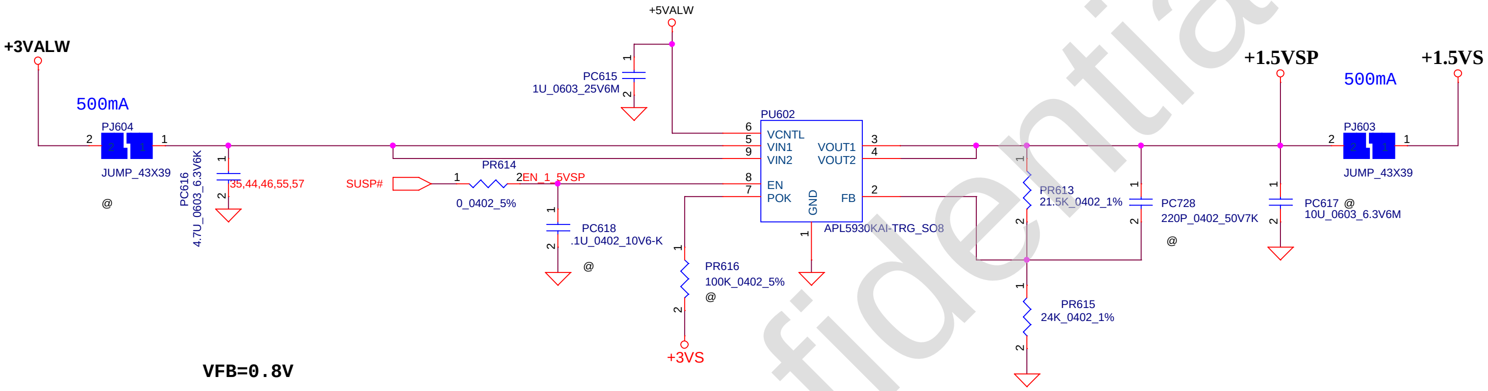
Title
1.35VS/+0.675VS

Size Custom
Document Number **ACLUA**
Rev 1.0
Date: Thursday, December 26, 2013
Sheet 55 of 59



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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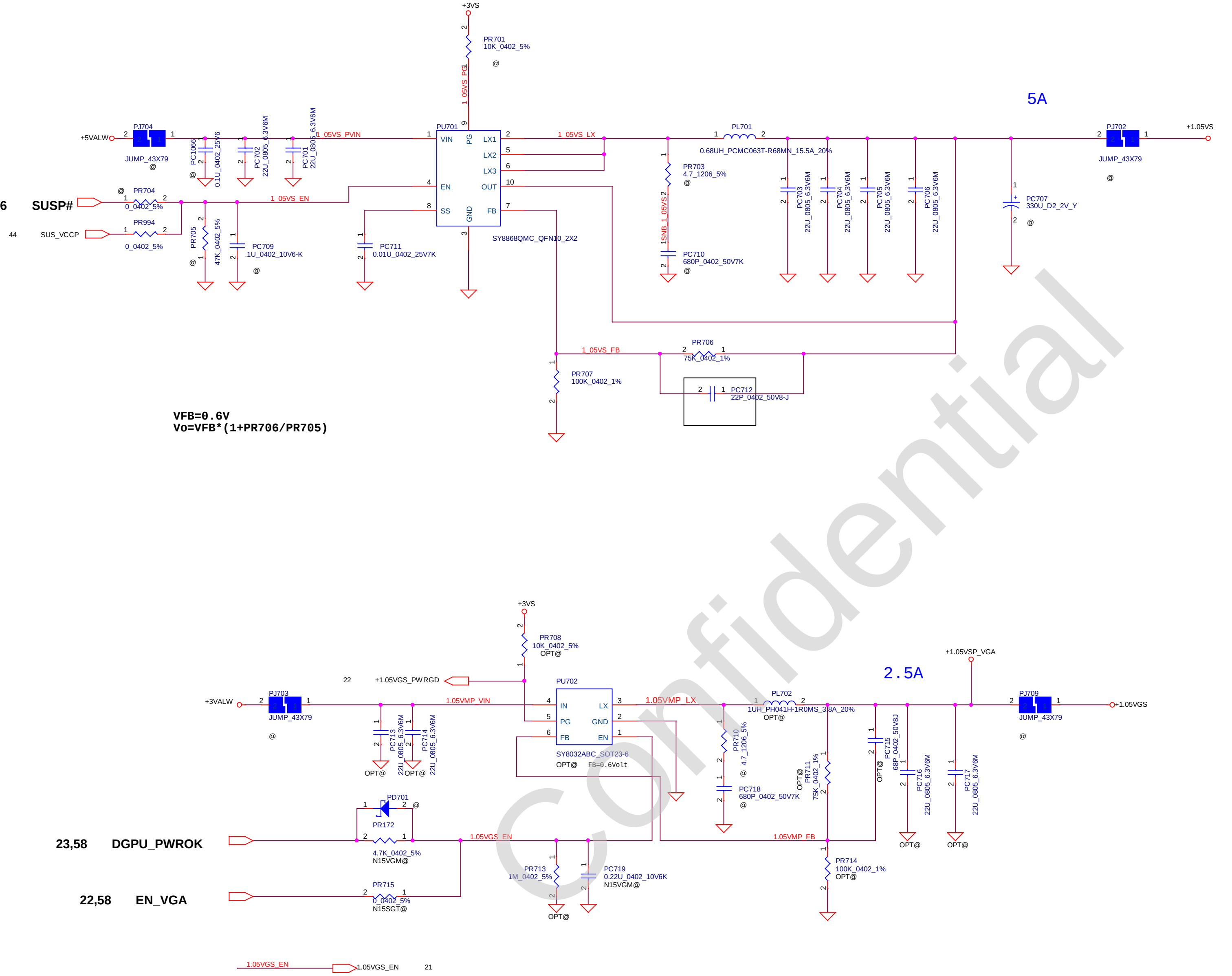
Title
+1.35VS_VGA/+1.5VS

Size Custom
Document Number
ACLUA
Rev 1.0

Date: Thursday, December 26, 2013
Sheet 56 of 59



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Issued Date	2013/08/08	Deciphered Date	2013/08/05

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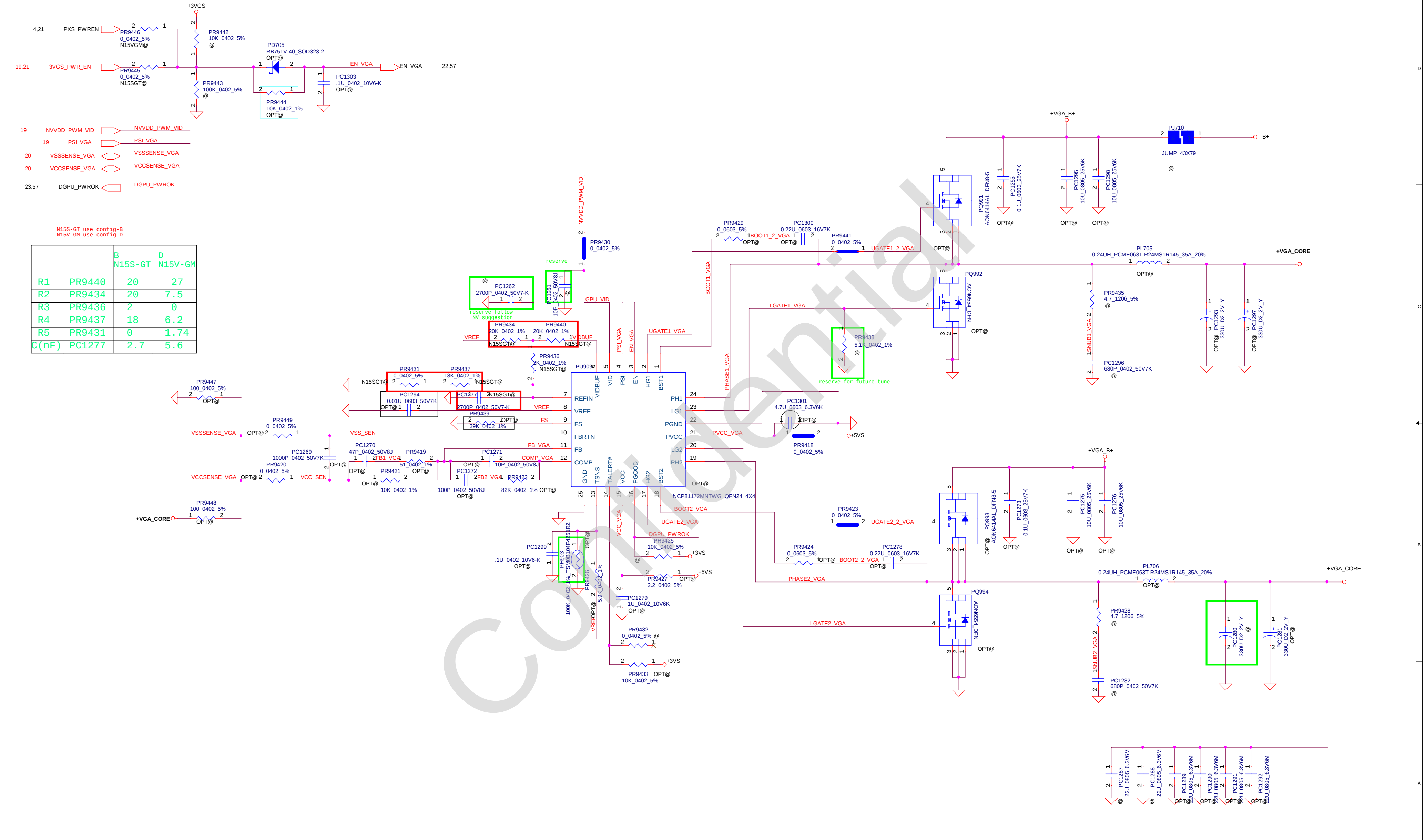
Title
+1.05VS/+1.05VS_VGA

Size Document Number
ACLUA
Rev
1.0

Date: Thursday, December 26, 2013 Sheet 57 of 59

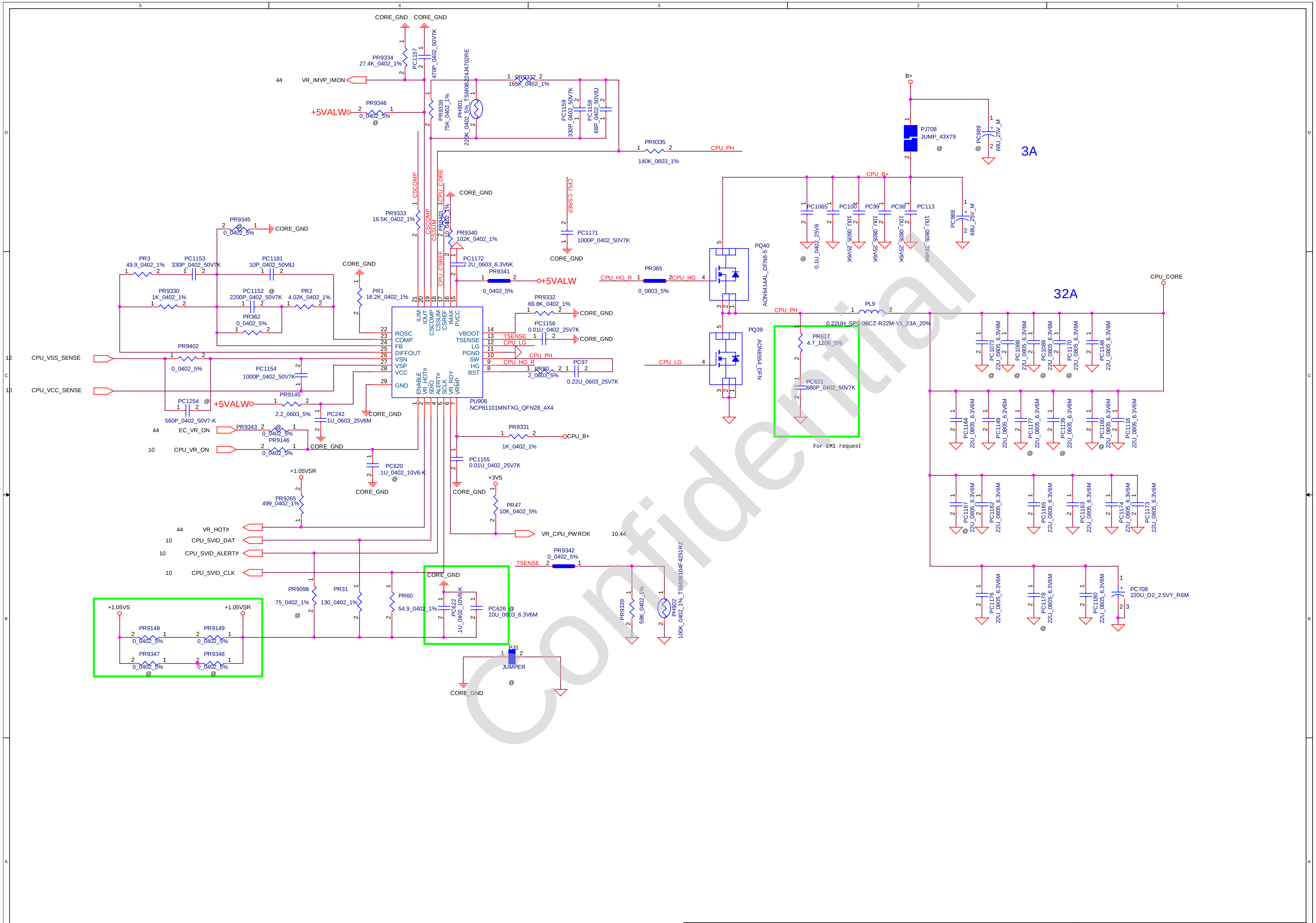


N15S-GT use config-B
N15V-GM use config-D

		B N15S-GT	D N15V-GM
R1	PR9440	20	27
R2	PR9434	20	7.5
R3	PR9436	2	0
R4	PR9437	18	6.2
R5	PR9431	0	1.74
C(nF)	PC1277	2.7	5.6

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title
PWR-VGA_CORE
LCFC
Size Custom
Document Number **ACLUA**
Rev 1.0
Date: Friday, December 27, 2013
Sheet 58 of 59



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title
PWR_CPU Core

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Date: Thursday, December 26, 2013 | Sheet 59 of 59