

Compal Confidential

VAWGA/B Schematics Document

AMD "Kabini" Platform

AMD 25W APU With Jaguar Core and Integrated Yangtze FCH + ATI Sun

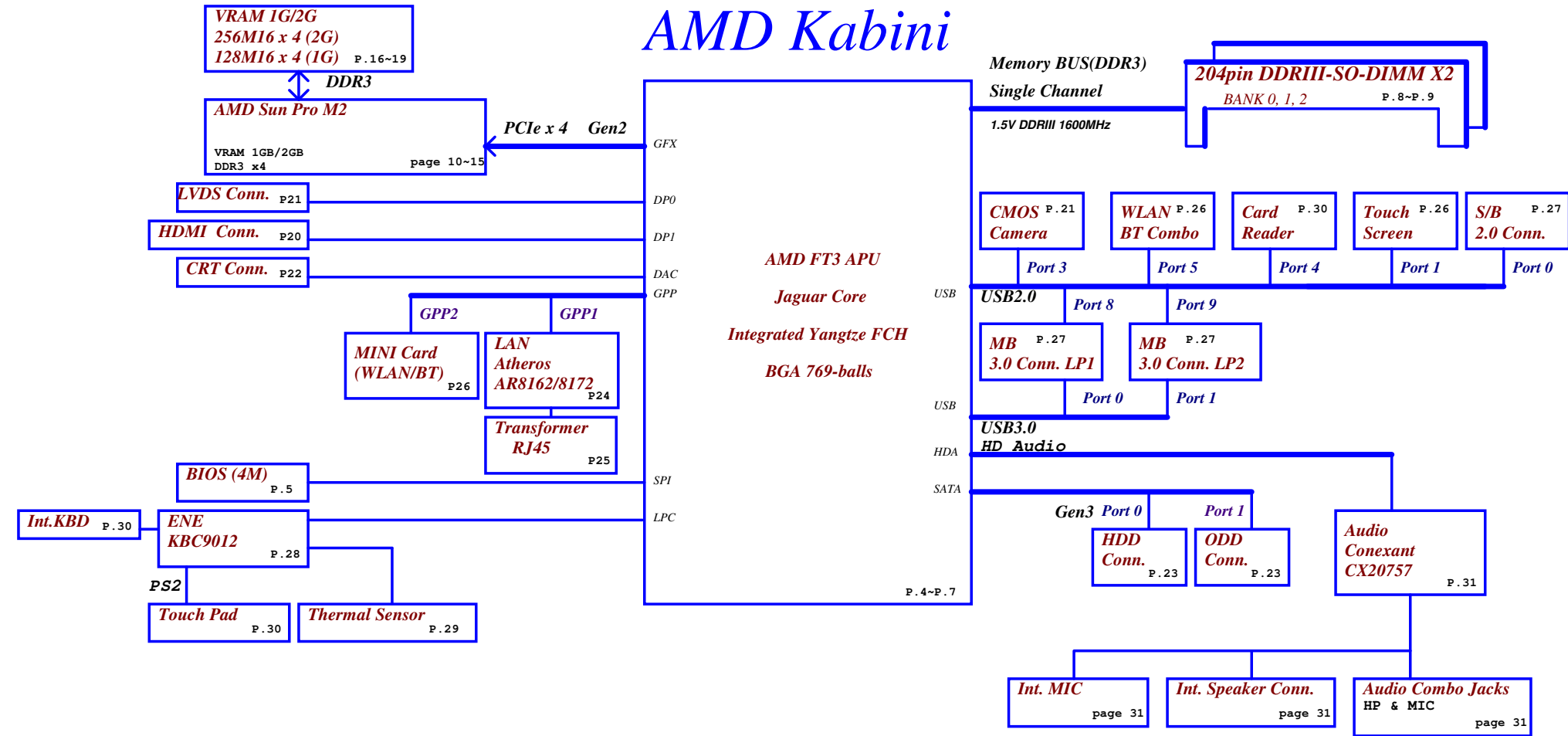
LA-9911P REV: 1.0

2013-04-01

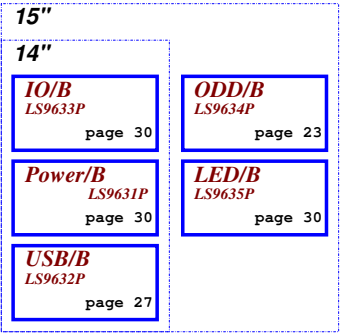
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/04/22	Deciphered Date	2015/04/22	Title	COVER PAGE
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				VAWGA/GB	1.0
				Date	Monday, April 01, 2013
				Sheet	1 of 48

Compal Confidential

Model Name : VAWGA/B



Sub-board



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/22	Deciphered Date	2015/04/22	Title	BLOCK DIAGRAMS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PRODUCT DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	VAWGA/GB
				Date	Thursday, March 28, 2013
				Sheet	2 of 48
				Rev	1.0

Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+3VGS	3.3V switched power rail for VGA	ON	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	ON	OFF	OFF
+1.5VGS	1.5V switched power rail for VGA	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON
+RTC_APU	RTC power	ON	ON	ON
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	V +3VS	X	X	X	X	V +3VS	X	V +3VS	X

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	Thermal Sensor	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			VGA Internal Thermal	1000 001X b	82H

APU SM Bus address

Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H
DDR DIMM2	1010 001Xb	A2H

BOARD ID Table

Board ID	PCB Revision
0	MP
1	PVT
2	DVT
3	EVT
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
R1562	100K +/- 5%			
Board ID	R1564	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

APU PCIE PORT LIST

Port	Device
0	
1	LAN
2	WLAN
3	

USB Port Table

USB 2.0	USB 3.0	Port	3 External USB Port
		0	RIGHT USB
		1	Touch Screen
		2	
		3	Camera
		4	CardReader
		5	WLAN/BT Combo
		6	LEFT USB (for colay)
		7	LEFT USB (for colay)
	XHCI	0	LEFT USB3.0
		1	LEFT USB3.0

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

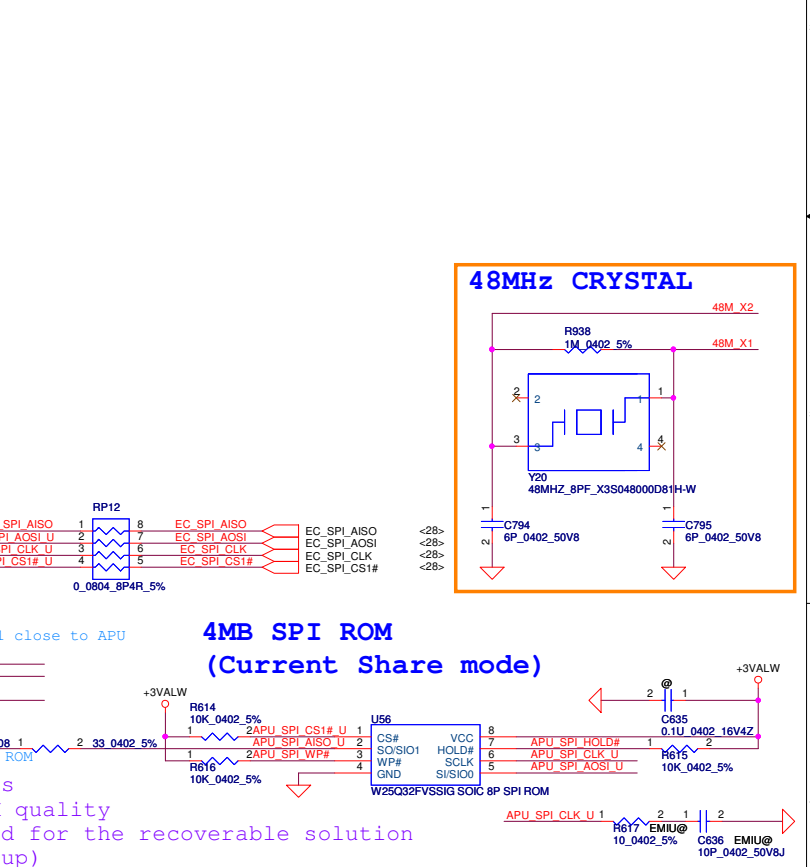
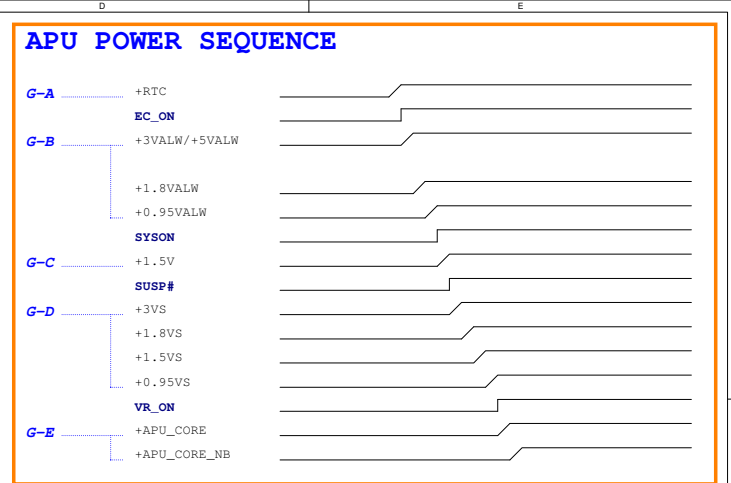
USB OC MAPPING

OC#	USB Port	
0	USB20 port0	
1	USB20 port1,2,8,9	USB30 port0,1
2		
3		

BOM Structure Table

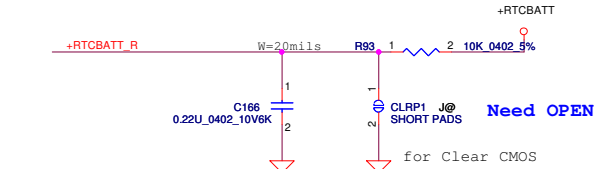
BOM Structure	BTO Item
A6@	A6 R3 BGA APU
A4@	A4 R3 BGA APU
E2@	E2 R3 BGA APU
E1@	E1 R3 BGA APU
E1PC@	E1 PC BGA APU
X4@	X4 ES2 BGA APU
X5@	X5 ES2 BGA APU
X2@	X2 ES2 BGA APU
EMICU@	CardReader EMI Un pop
EMICP@	CardReadear EMI pop
EMIUSB2RU@	Right USB2.0 port EMI un pop
EMIUSB2RP@	Right USB2.0 port EMI pop
USB2R@	Right USB2.0 port component
SUN@	SUN PRO GPU (R3 compal part)
MARS@	MARS XT GPU (R1 compal part)
14@	for 14" componect
15@	for 15" componect
PX@	Common VGA circuit
CMOS@	CMOS Camera part
HDMI@	HDMI part
EMIGASP@	Gastube
8162@	Ateros AR8162 LAN Chip
8172@	Ateros AR8172 LAN Chip
SWR@	LAN Switching mode
LDO@	LAN LDO mode
THERMAL@	Lenovo Thermal Sensor
ME@	ME part
UMA@	UMA part
@	Unpop
ZODD@	Zero Power ODD part
TS@	Touch Screen
EMIP@	EMI pop component
EMIU@	EMI Un pop component
ESDP@	ESD pop component
ESDU@	ESD Un pop component

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/04/22	Deciphered Date	2015/04/22	Title	NOTES LIST	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PRODUCT DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	VAWGA/GB	Rev 1.0
				Date	Monday, April 01, 2013	Sheet 3 of 48

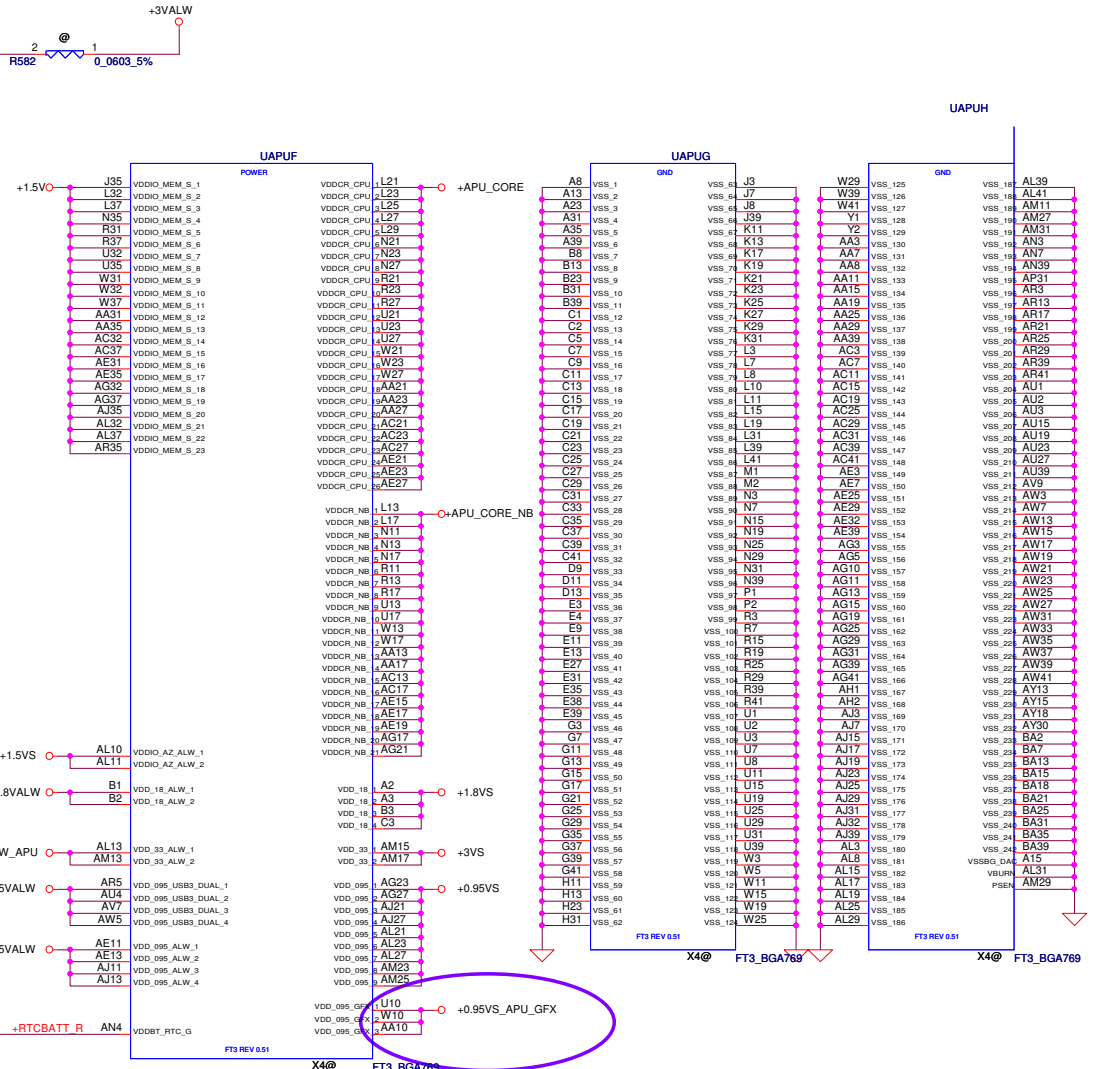


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/22	Deciphered Date	2015/04/22	Title	FT3 PCIE/SATA/CLK/USB/SPI
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FEDERAL DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				VAWGA/GB	1.0
Date: Thursday, March 28, 2013				Sheet	5 of 48

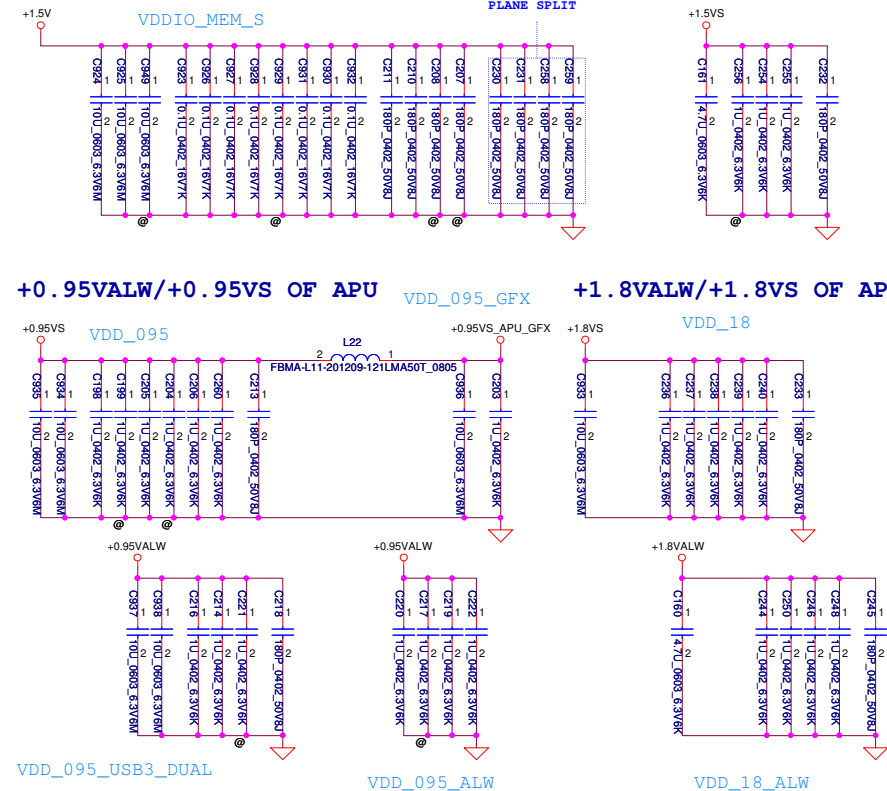
VDDBT_RTC_G



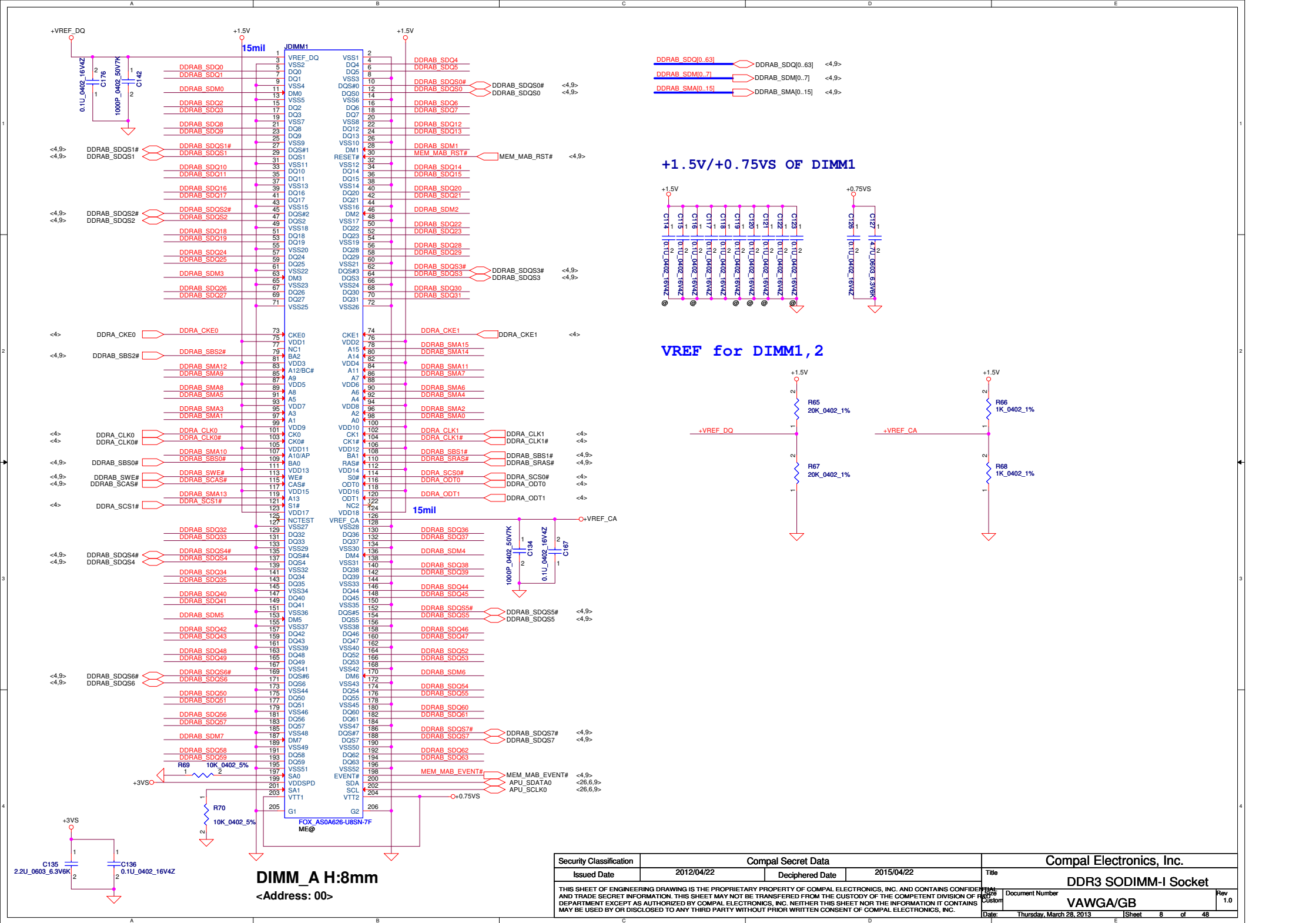
UAPUH

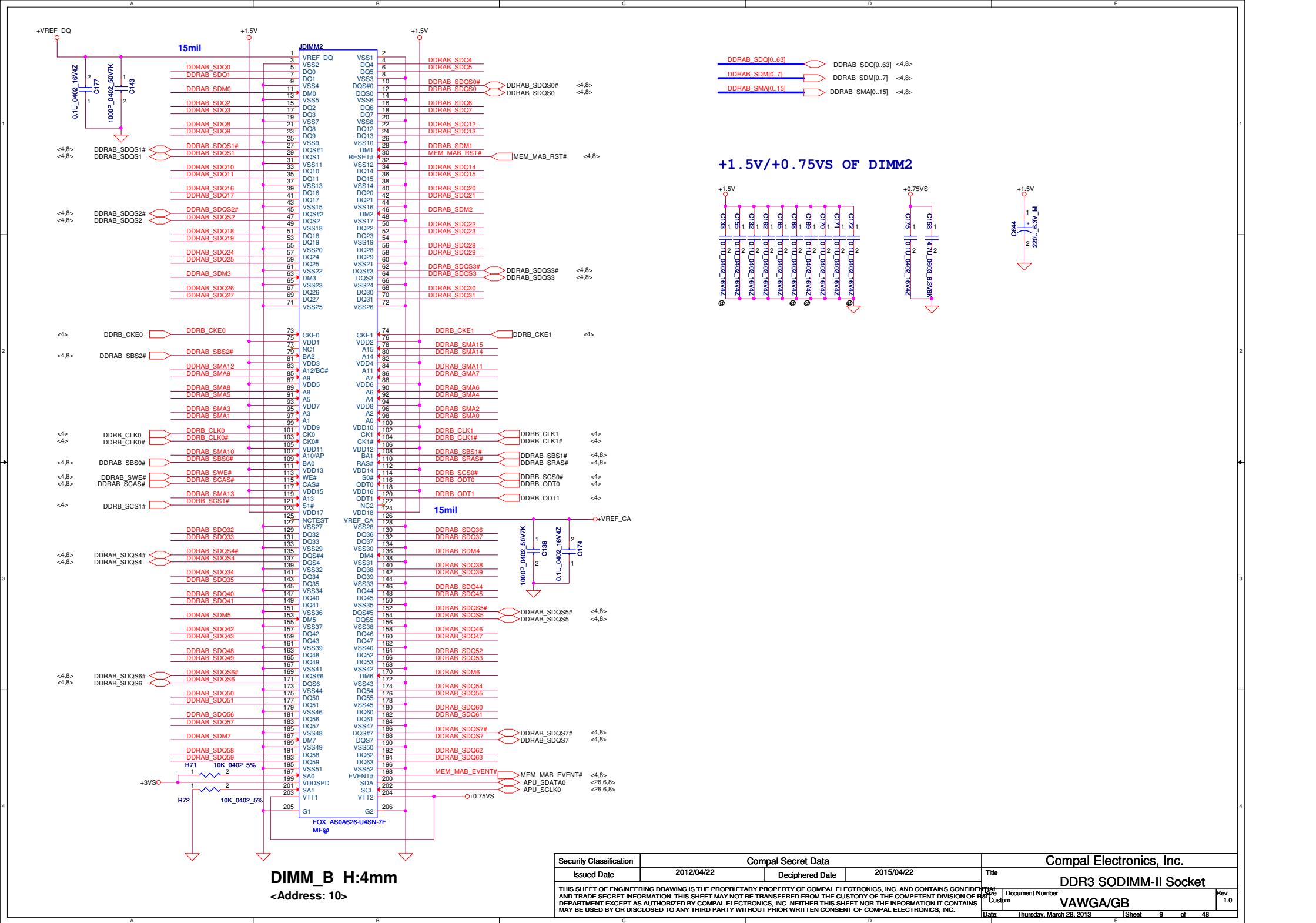


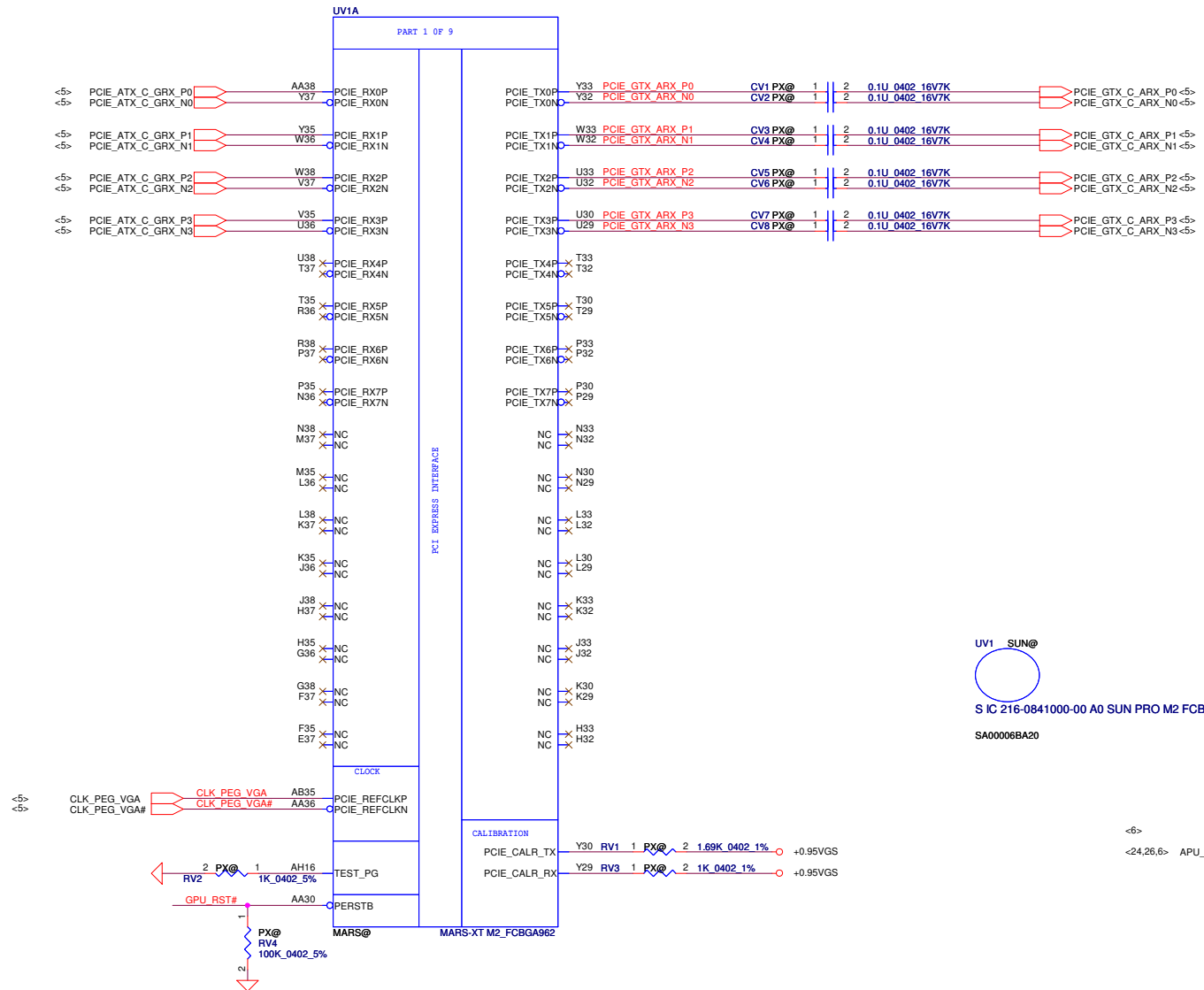
+1.8VALW/+1.8VS OF APU



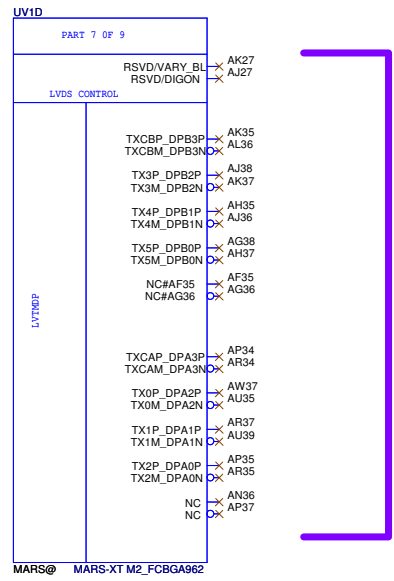
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/22	Deciphered Date	2015/04/22	Title	FT3 PWR/GND
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF CUSTOMER DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				VAWG/G/B	1.0
Date:		Thursday, March 28, 2013		Sheet	7 of 48





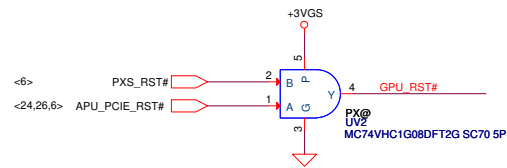


LVDS Interface



SUN NC

UV1 SUN@
S IC 216-0841000-00 A0 SUN PRO M2 FCBGA 962P C38
SA00006BA20

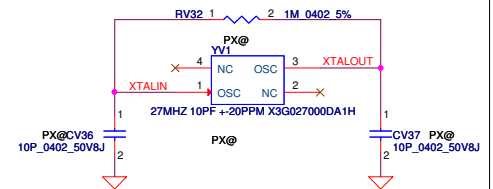
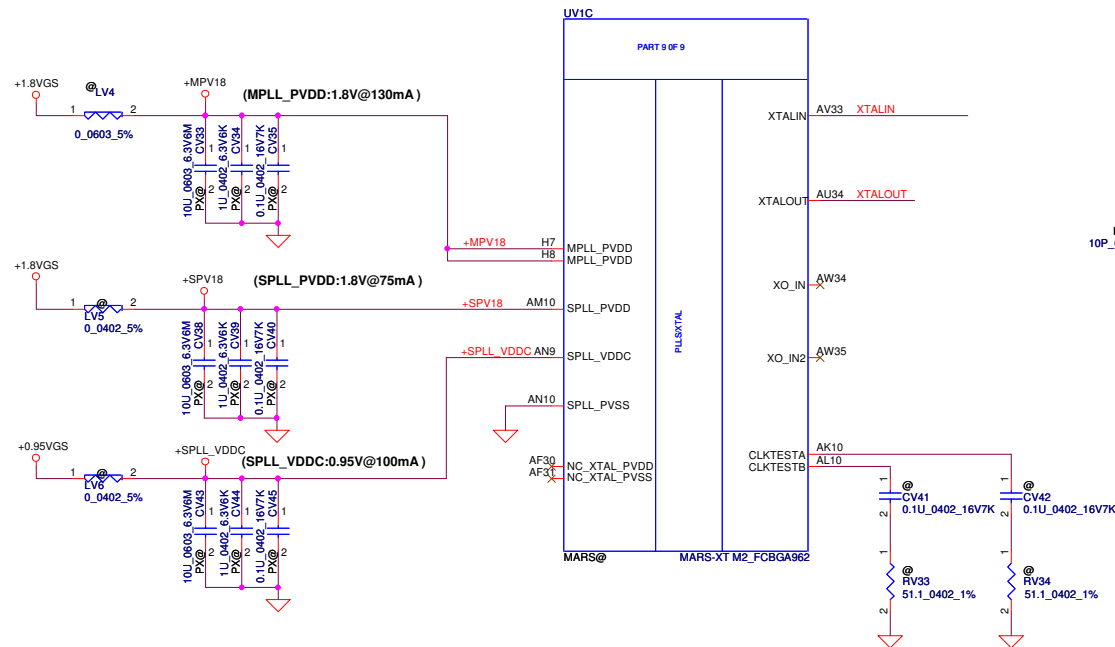


Security Classification		Compal Secret Data		Compal Electronics, Inc.									
Issued Date		2012/07/03		Deciphered Date		2013/07/03		Title					
								ATI MarsXTX M2 PCIE/LVDS					
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								Docu		Number		Rev	
								Custom		VAWGA/GB		1.0	
Date		Monday, April 01, 2013		Sheet		10		of 48					

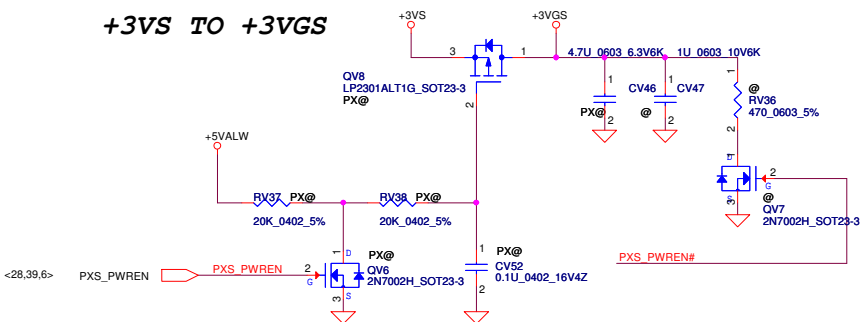
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

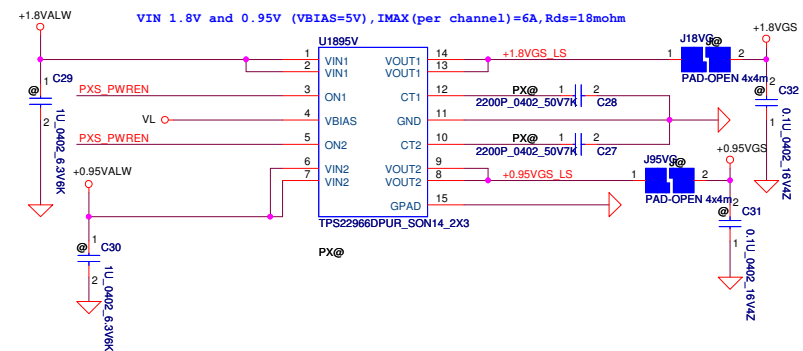
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



+3VS TO +3VGS

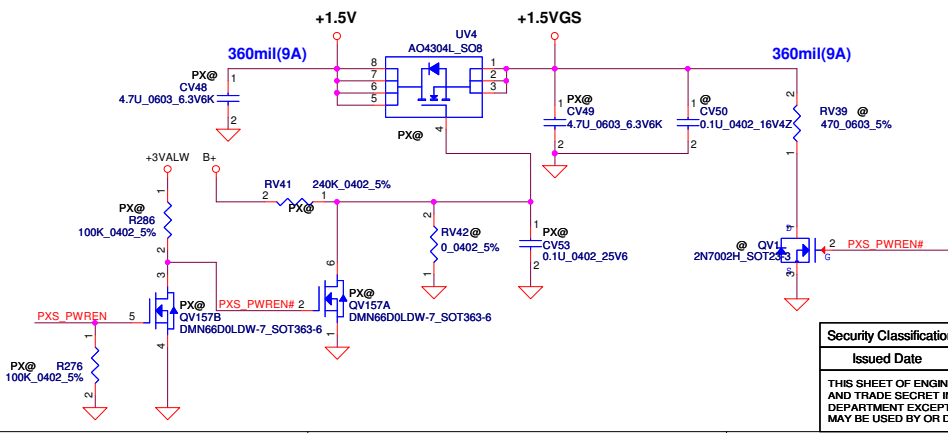


+1.8VALW TO +1.8VGS +0.95VALW TO +0.95VGS Load switch



+1.5V TO +1.5VGS

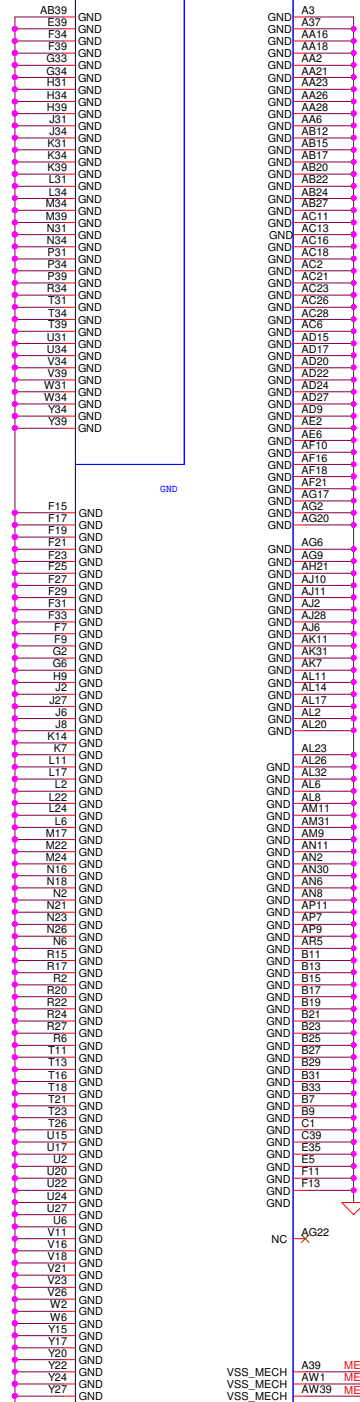
AO4430: Rds(on)=5.5mohm @ VGS=10V



Security Classification	Compal Secret Data		Title	
Issued Date	2012/07/03	Deciphered Date	2013/07/03	AT1 MarsXTX M2_BACO POWER
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 1.0
Date: Thursday, March 28, 2013				Sheet 12 of 48

UV1G

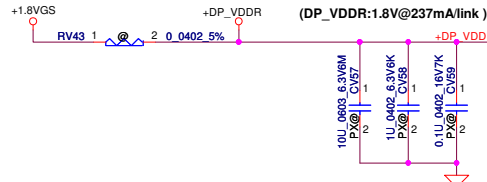
PART 6 OF 9



VSS_MECH A39 MECH#1 TV12 PAD
VSS_MECH AW1 MECH#2 TV13 PAD
VSS_MECH AW39 MECH#3 TV14 PAD

MARS@ MARS-XT M2_FCBGA962

DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1



UV1F

PART 8 OF 9

AN24 NC
AP25 NC
AP26 NC
AP27 NC
AV28 NC

AP20 NC
AP21 NC
AP22 NC
AP23 NC
AU28 NC
AV19 NC

AH34 DP_VDDR
AG34 DP_VDDR
AG34 DP_VDDR
AM37 DP_VDDR
AL38 DP_VDDR
AM32 DP_VDDR

CALIBRATION

AW28 NC
AW18 NC

DP_CALR

MARS@

MARS-XT M2_FCBGA962

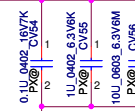
(DP_VDDC:0.95V@280mA/link)

DP_VDDC AP31
DP_VDDC AN33
DP_VDDC AL33
DP_VDDC AM39
DP_VDDC AK33
DP_VDDC AK34
DP_VDDC AN31

NC AP13
NC AP14
NC AP15

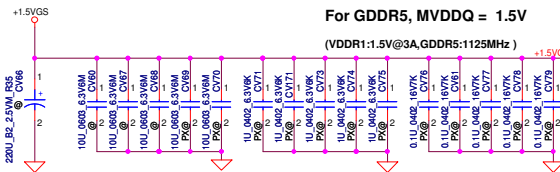
DP_GND

DP_VSSR AN27
DP_VSSR AP27
DP_VSSR AP28
DP_VSSR AW24
DP_VSSR AW26
DP_VSSR AN29
DP_VSSR AP29
DP_VSSR AP30
DP_VSSR AW30
DP_VSSR AW32
DP_VSSR AN17
DP_VSSR AP16
DP_VSSR AP17
DP_VSSR AW14
DP_VSSR AW16
DP_VSSR AN19
DP_VSSR AP18
DP_VSSR AP19
DP_VSSR AW20
DP_VSSR AW22
DP_VSSR AN34
DP_VSSR AP39
DP_VSSR AH39
DP_VSSR AL34
DP_VSSR AV27
DP_VSSR AR28
DP_VSSR AV17
DP_VSSR AR18
DP_VSSR AN38
DP_VSSR AM35
DP_VSSR AN32



DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2012/07/03				Title			
				Deciphered Date				2013/07/03			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev				ATI MarsXTX M2_PWR_GND			
				Document Number				Rev 1.0			
				Date				Thursday, March 28, 2013			
				Sheet				13 of 48			

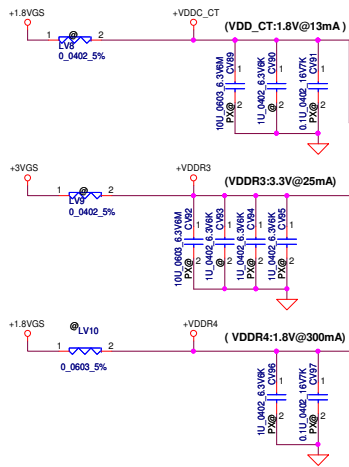


VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

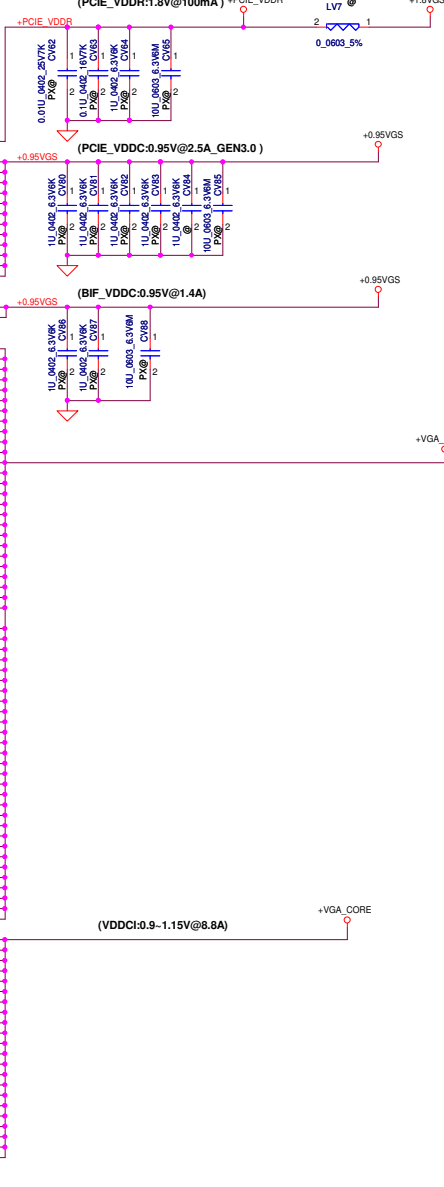
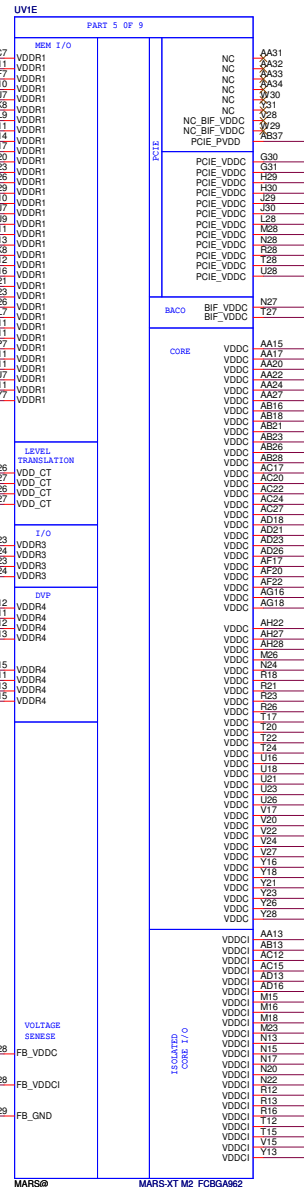
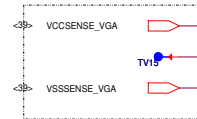
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



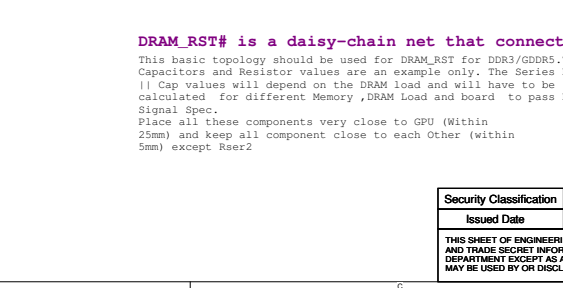
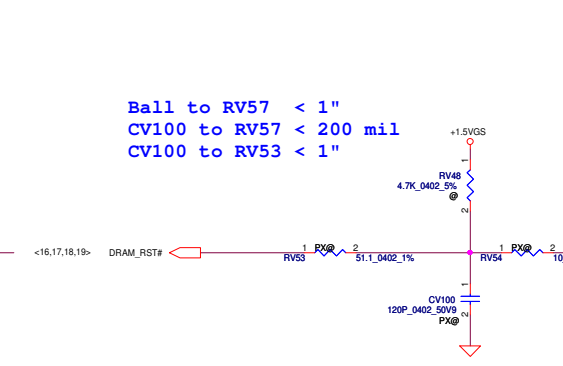
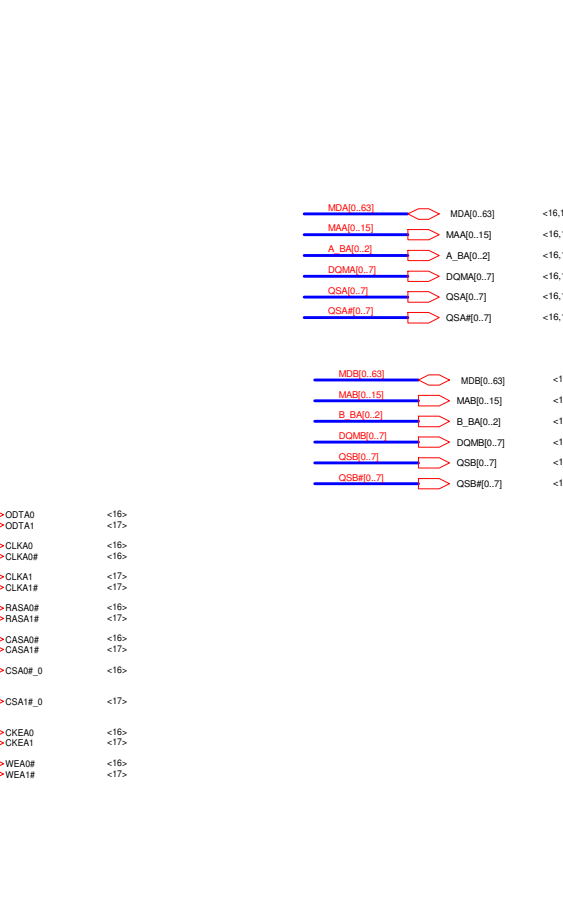
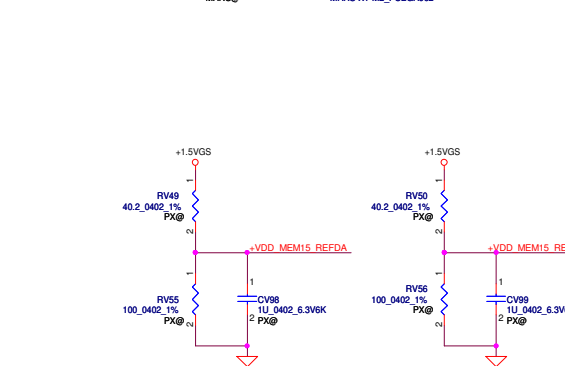
Route as differential pair



PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

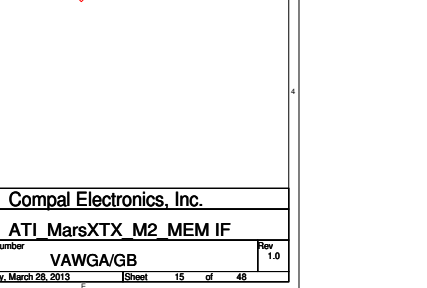
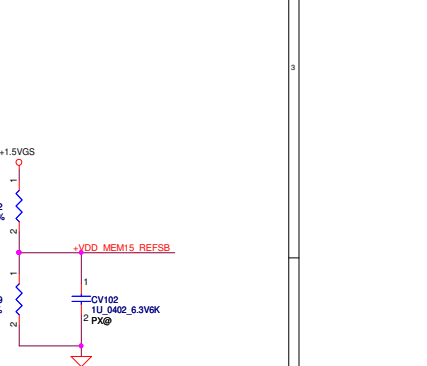
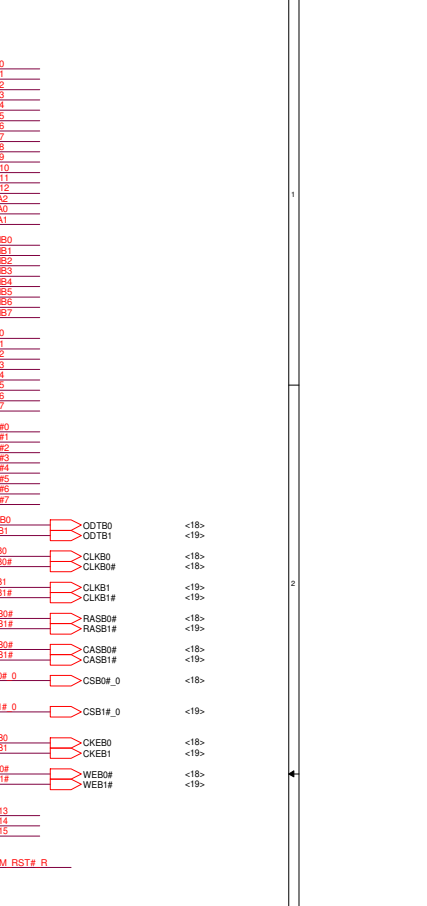
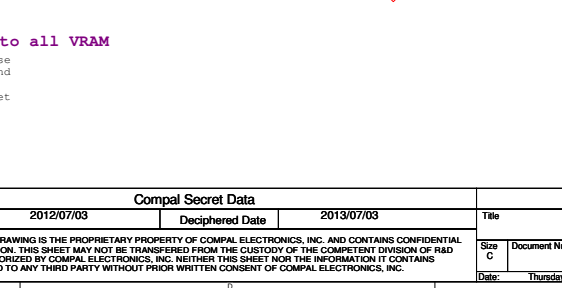
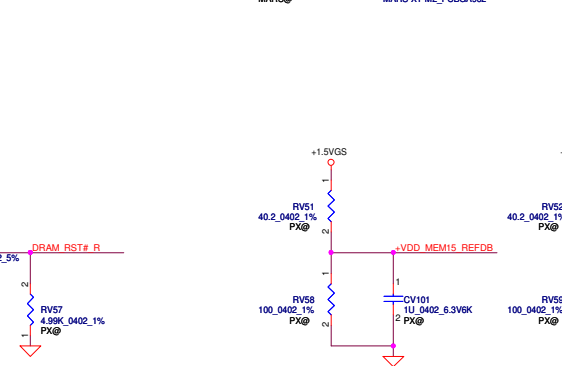
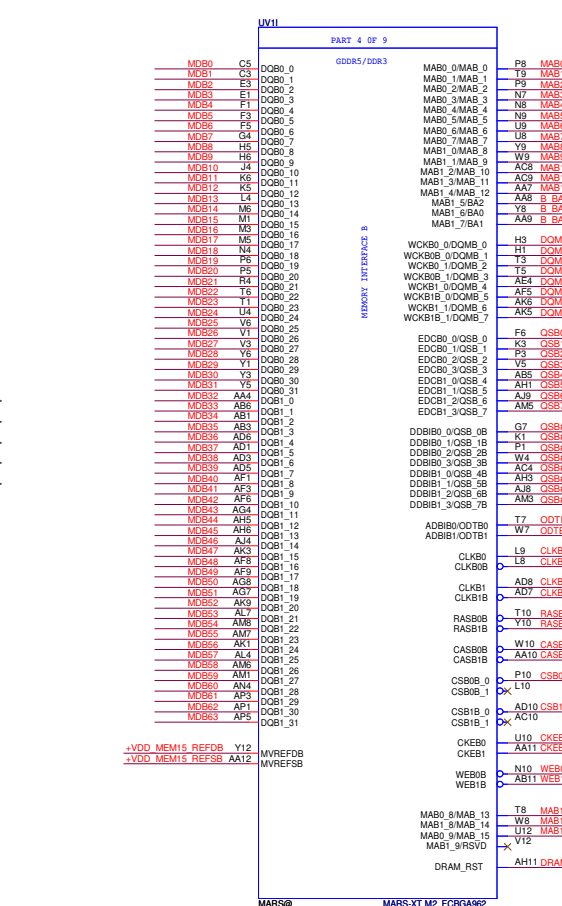
PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

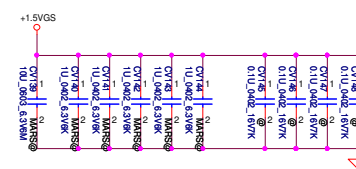
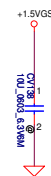
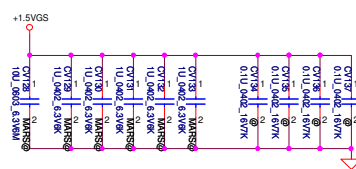
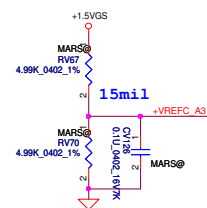
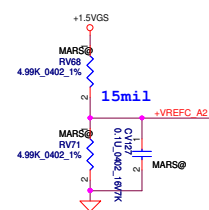
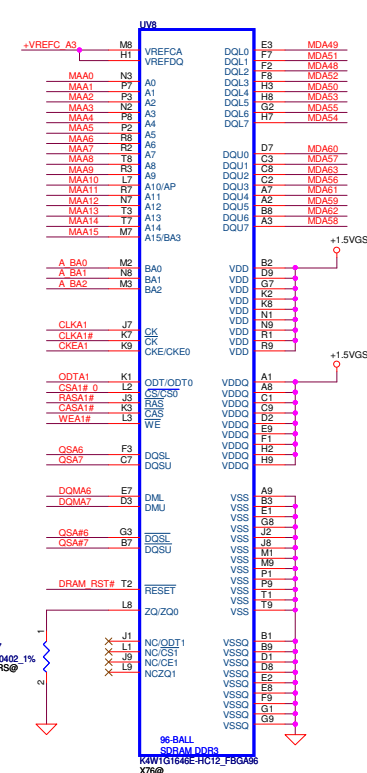
VGA_CORE Cap in power side sheet




Ball to RV57 < 1"
 CV100 to RV57 < 200 mil
 CV100 to RV53 < 1"


DRAM_RST# is a daisy-chain net that connects to all VRAM
 This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.
 Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2








Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2010/08/25	Deciphered Date		2012/08/25
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title	
				ATI Whistler M2 VRAM A	
Size C		Document Number			Rev 1.0
		VAWG/GB			
Date:		Thursday, March 28, 2013		Sheet	17 of 48

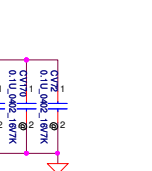
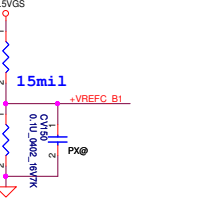
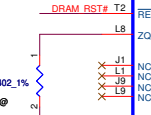
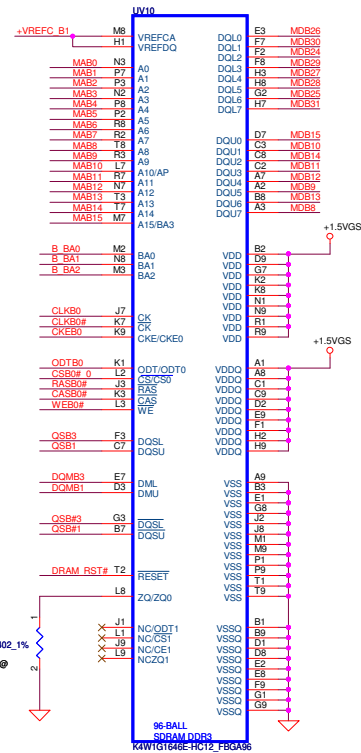
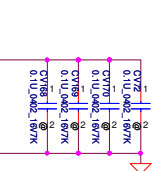
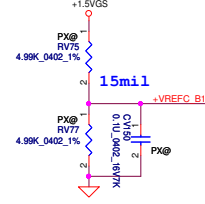
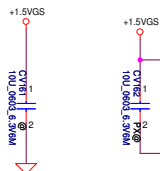
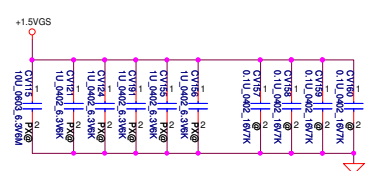
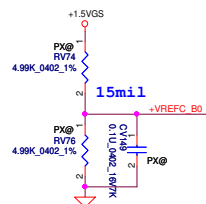
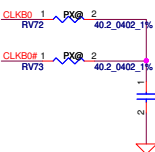
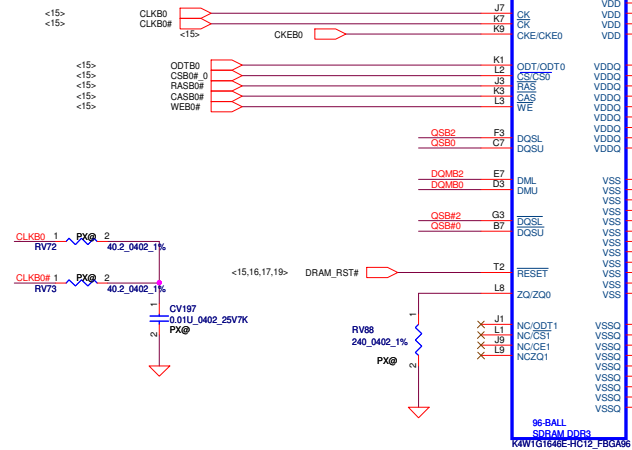
<15> MDB[0..31]  MDB[0..31]

<15,19> MAB[15..0]  MAB[15..0]

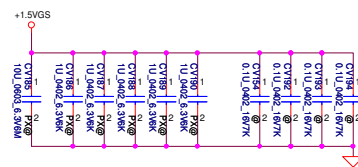
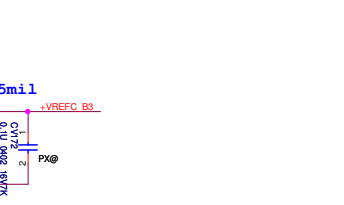
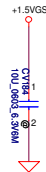
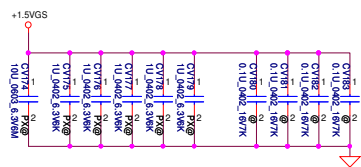
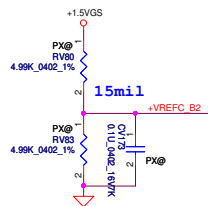
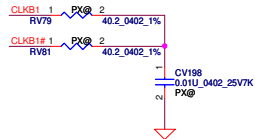
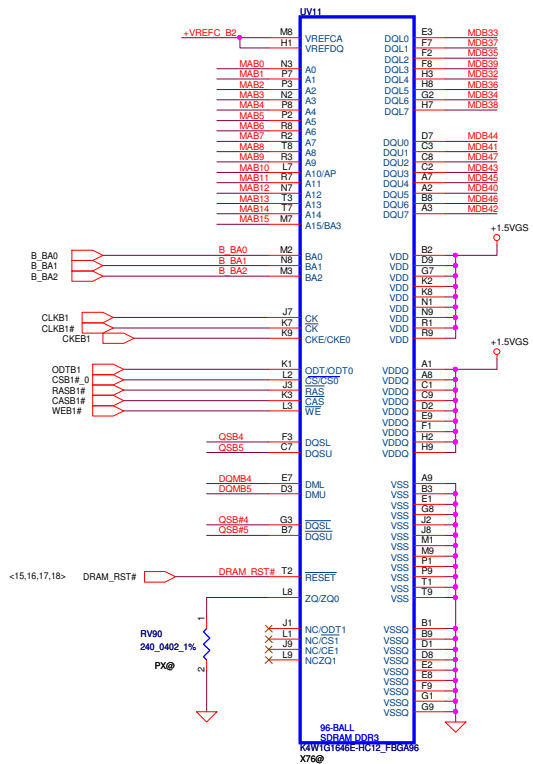
<15> DQMB[3..0]  DQMB[3..0]

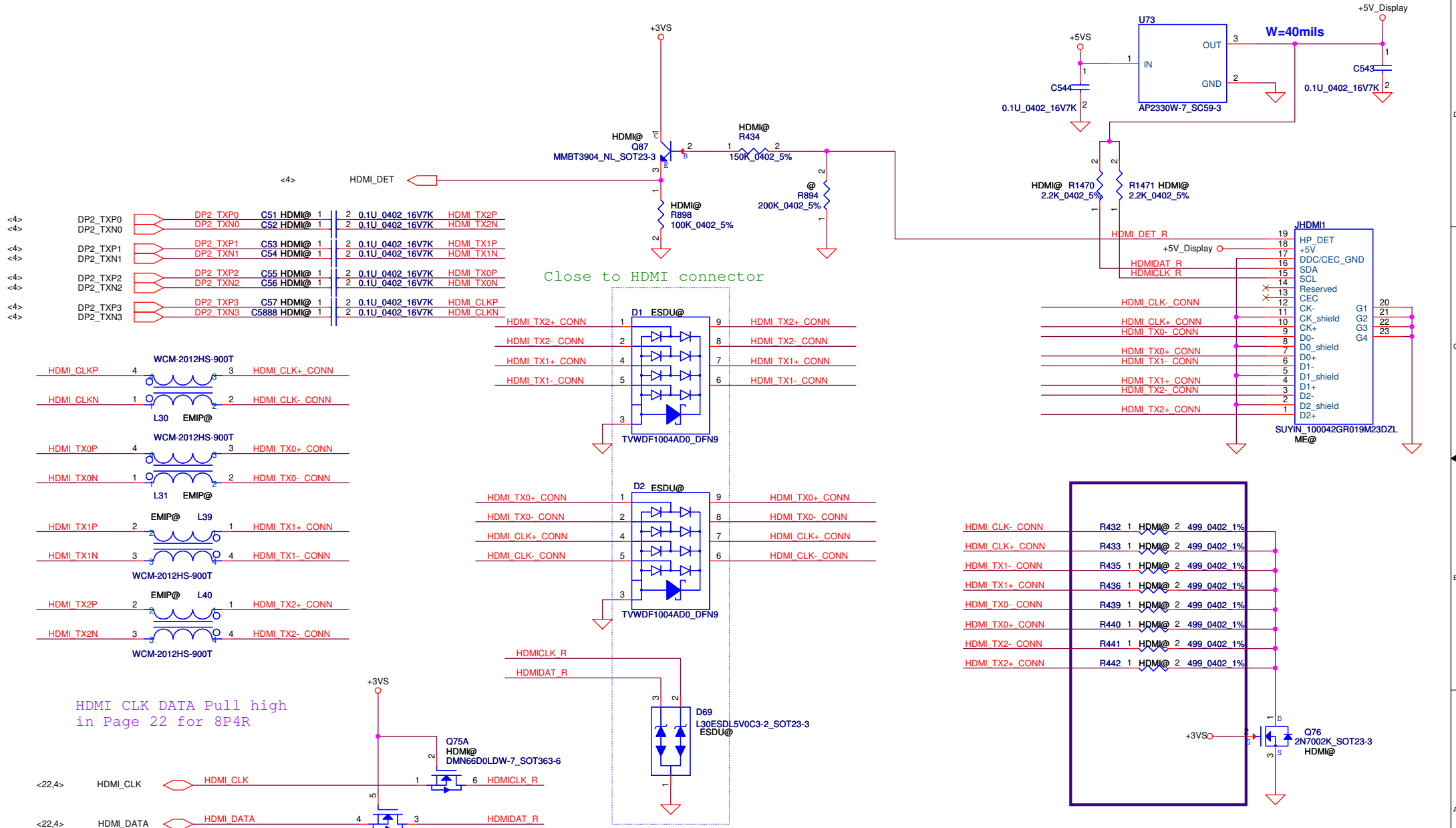
<15> QSB[3..0]  QSB[3..0]

<15> QSB# [3..0]  QSB# [3..0]



<15> MDB[32..63] MDB[32..63]
<15,18> MAB[15..0] MAB[15..0]
<15> DQMB[7..4] DQMB[7..4]
<15> QSB[7..4] QSB[7..4]
<15> QSBH[7..4] QSBH[7..4]

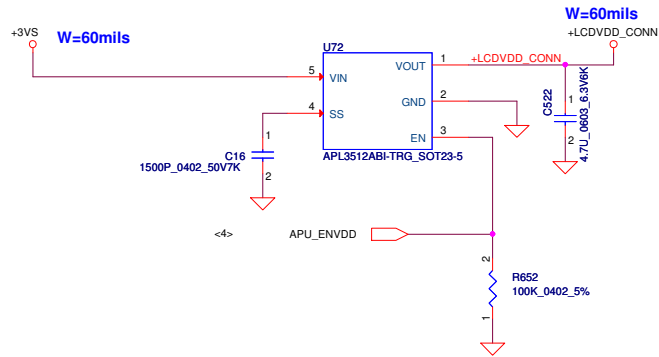




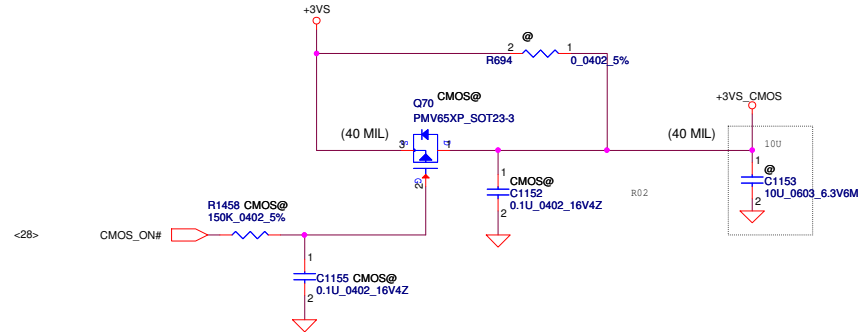
HDMI CLK DATA Pull high
in Page 22 for 8P4R

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/22	Deciphered Date	2015/04/22	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				HDMI CONN	
Date: Monday, April 01, 2013		Sheet 20 of 48		Rev 1.0	

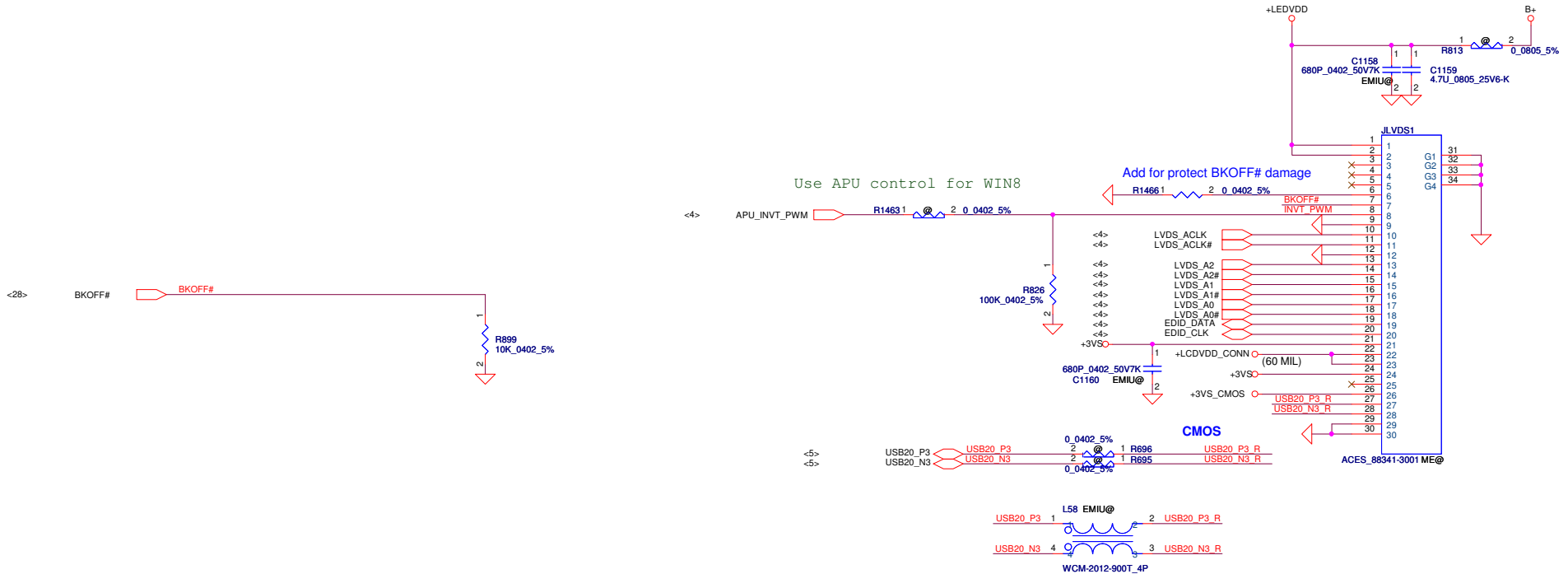
LCD POWER CIRCUIT



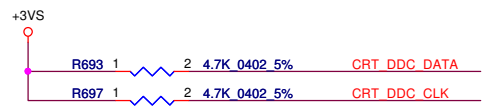
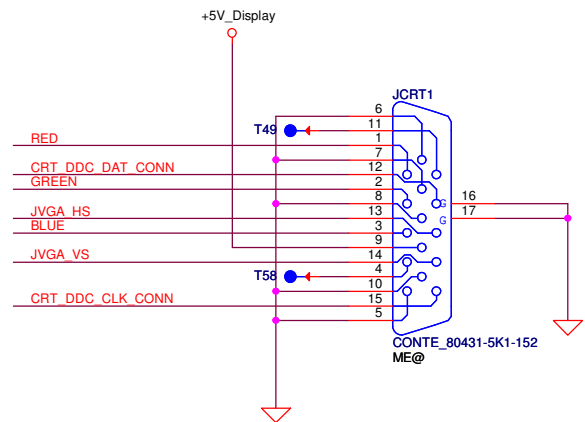
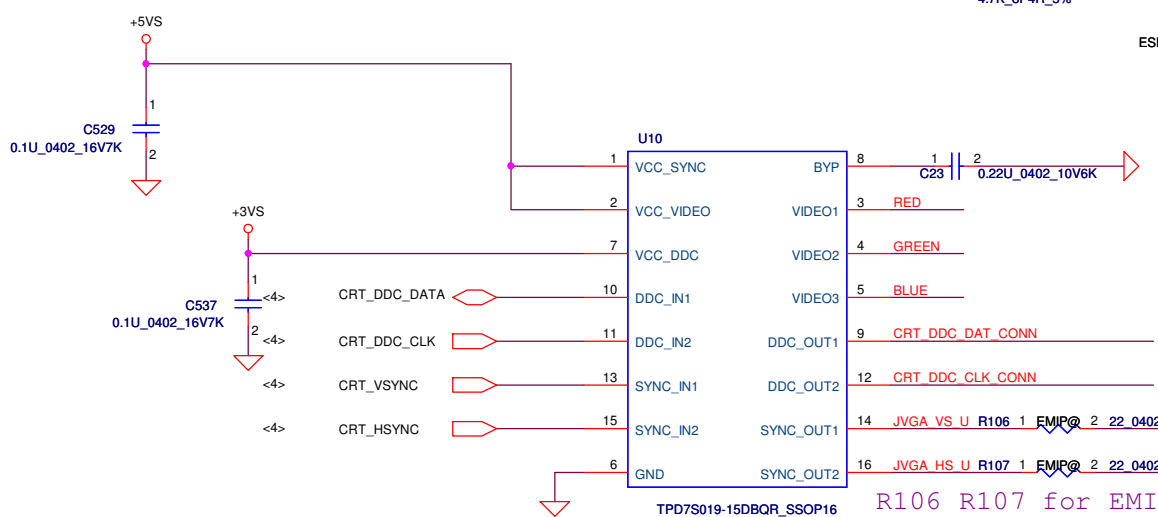
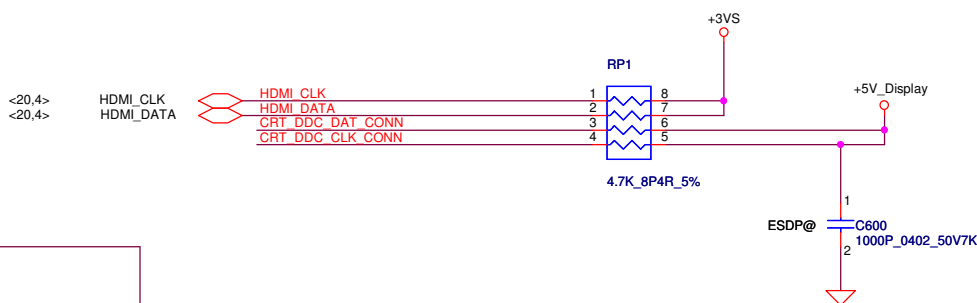
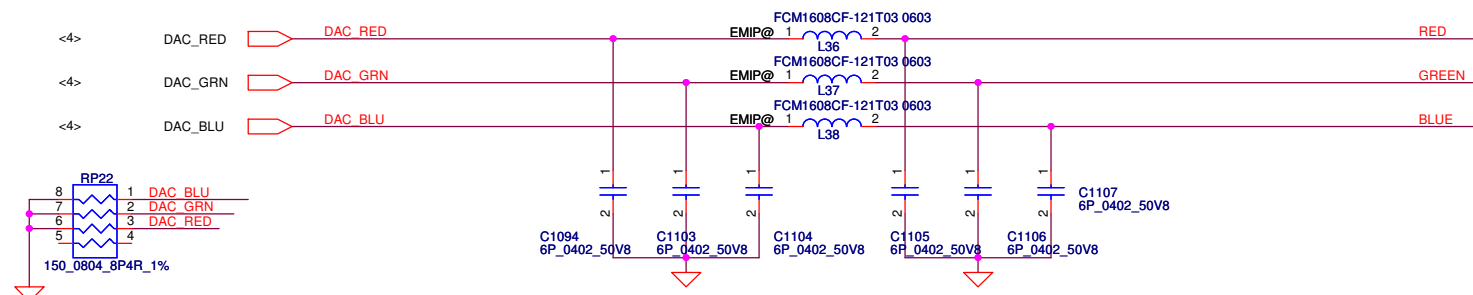
CMOS Camera



VGA LCD/PANEL BD. Conn.

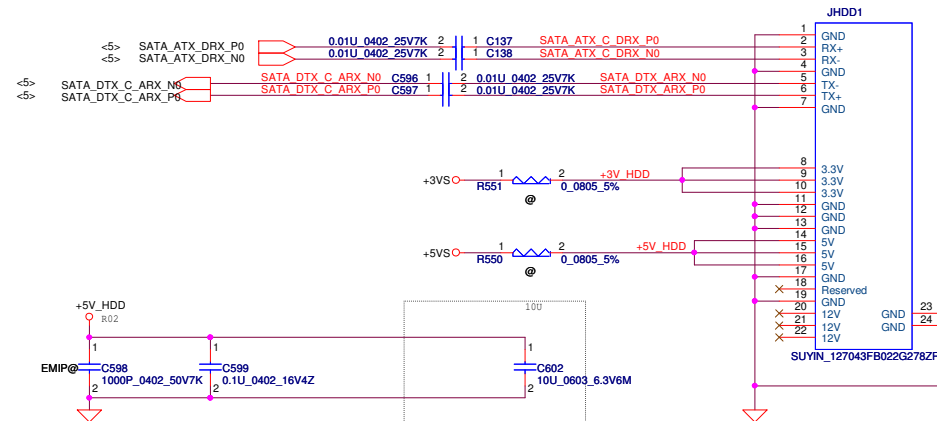


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/04/22	Deciphered Date	2015/04/22	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PRODUCT DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev	1.0
				Date: Thursday, March 28, 2013		
				Sheet 21 of 48		

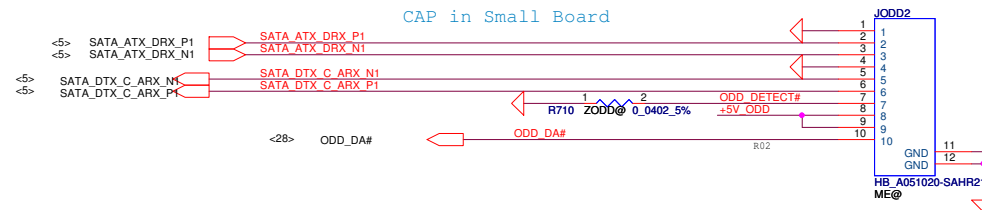


Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2012/04/22		Deciphered Date		2015/04/22		Title			
								CRT CONN			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Size B		Document Number		Rev 1.0	
								VAWGA/GB			
						Date		Thursday, March 28, 2013		Sheet 22 of 48	

SATA HDD Conn.

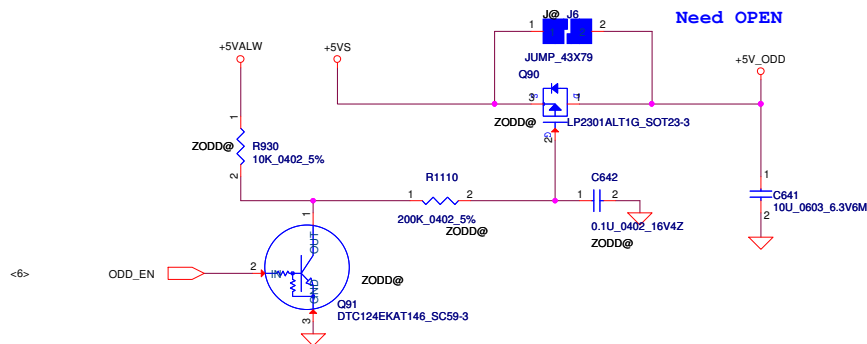


FOR 15"
SATA ODD FFC Conn.

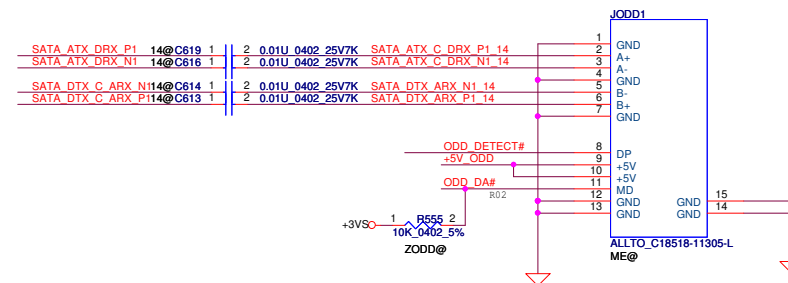


Co-lay

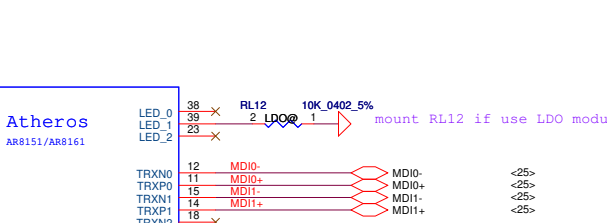
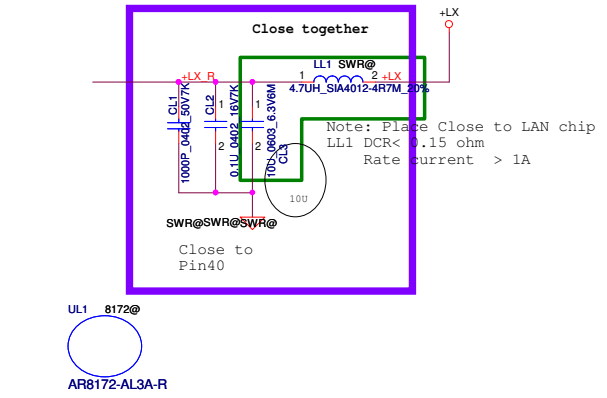
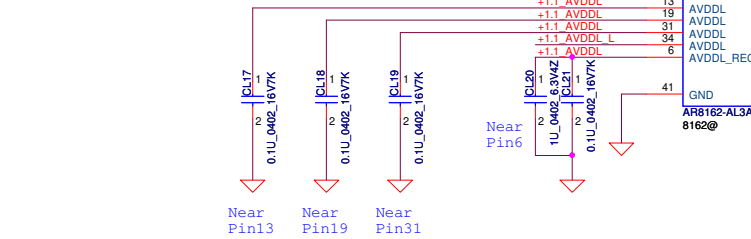
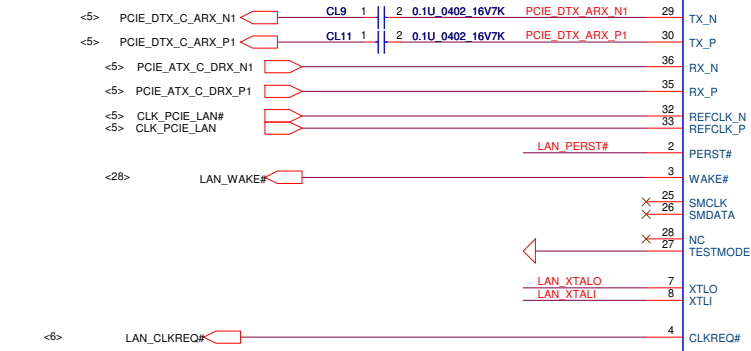
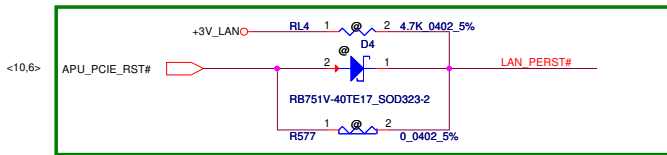
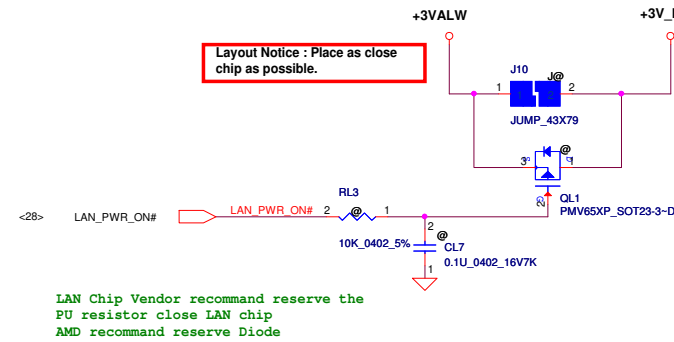
ODD Power Control

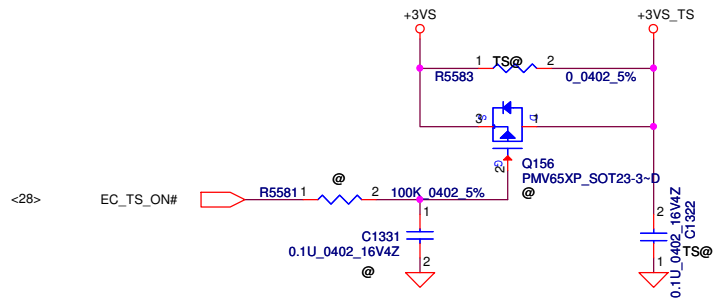


FOR 14"
SATA ODD Conn.

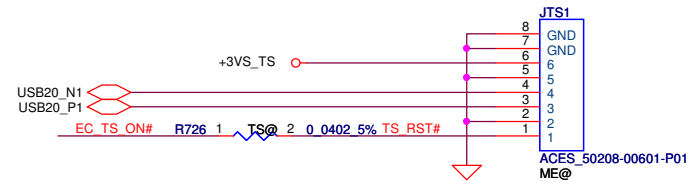


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/22	Deciphered Date	2015/04/22	Title	HDD/ODD/FAN/SCREW
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 1.0
				VAWG/G/B	
Date: Thursday, March 28, 2013		Sheet 23 of 48			

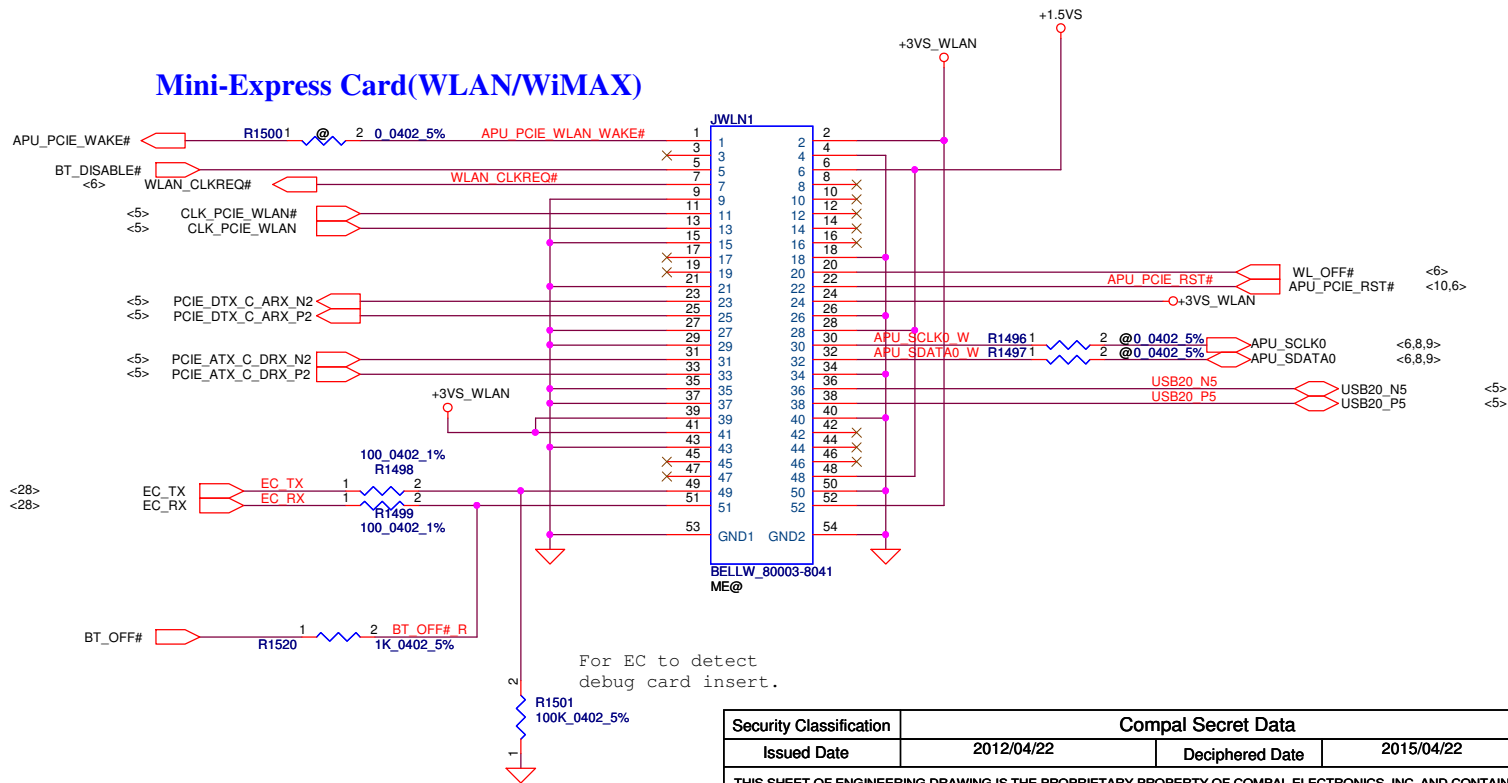




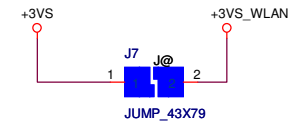
<5>
<5>



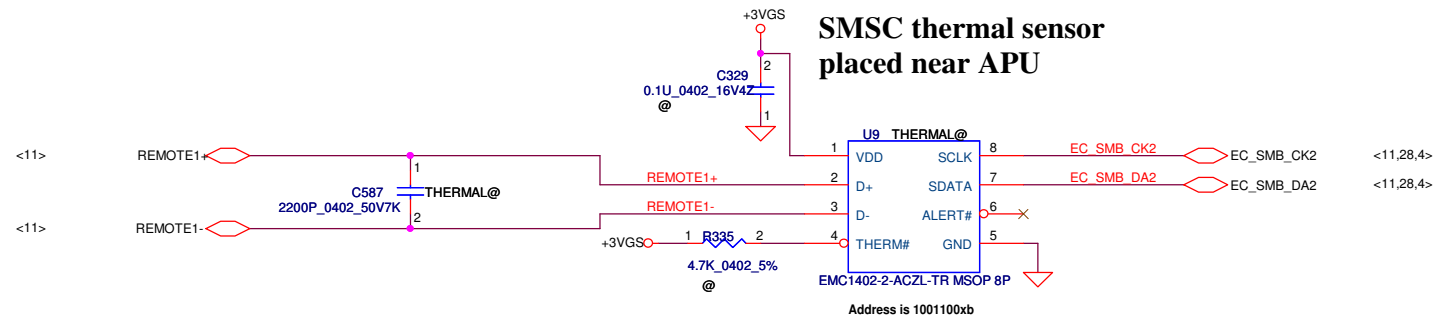
Mini-Express Card(WLAN/WiMAX)



For EC to detect
debug card insert.

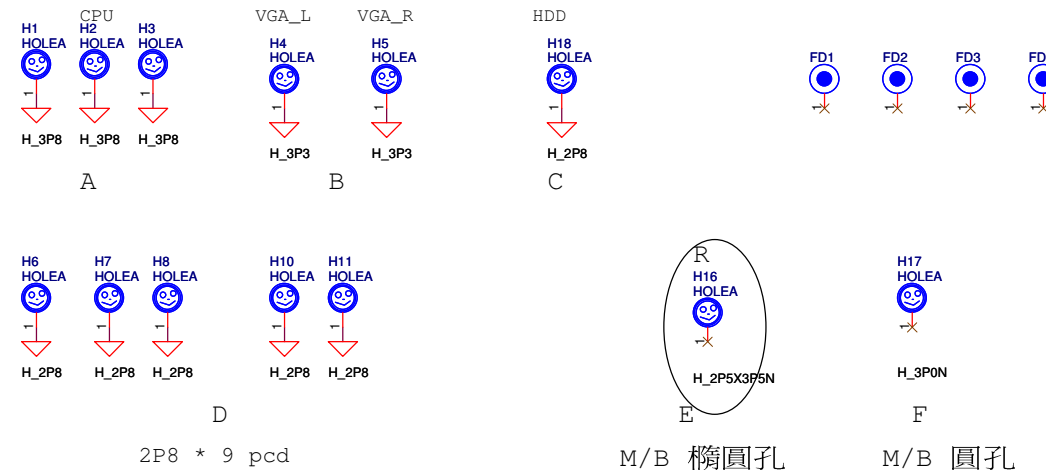
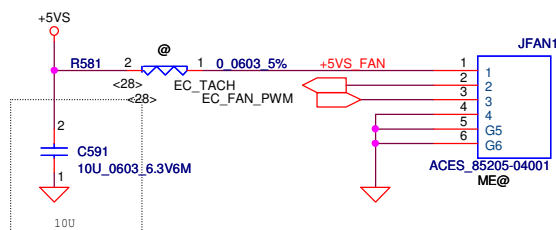


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2012/04/22				Deciphered Date			
2015/04/22				Title				MINI1 CARD (WLAN) / MINI2 CARD (Option)			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B				Document Number			
								VAWGA/GB			
								Date: Thursday, March 28, 2013			
								Sheet 26 of 48			
								Rev 1.0			

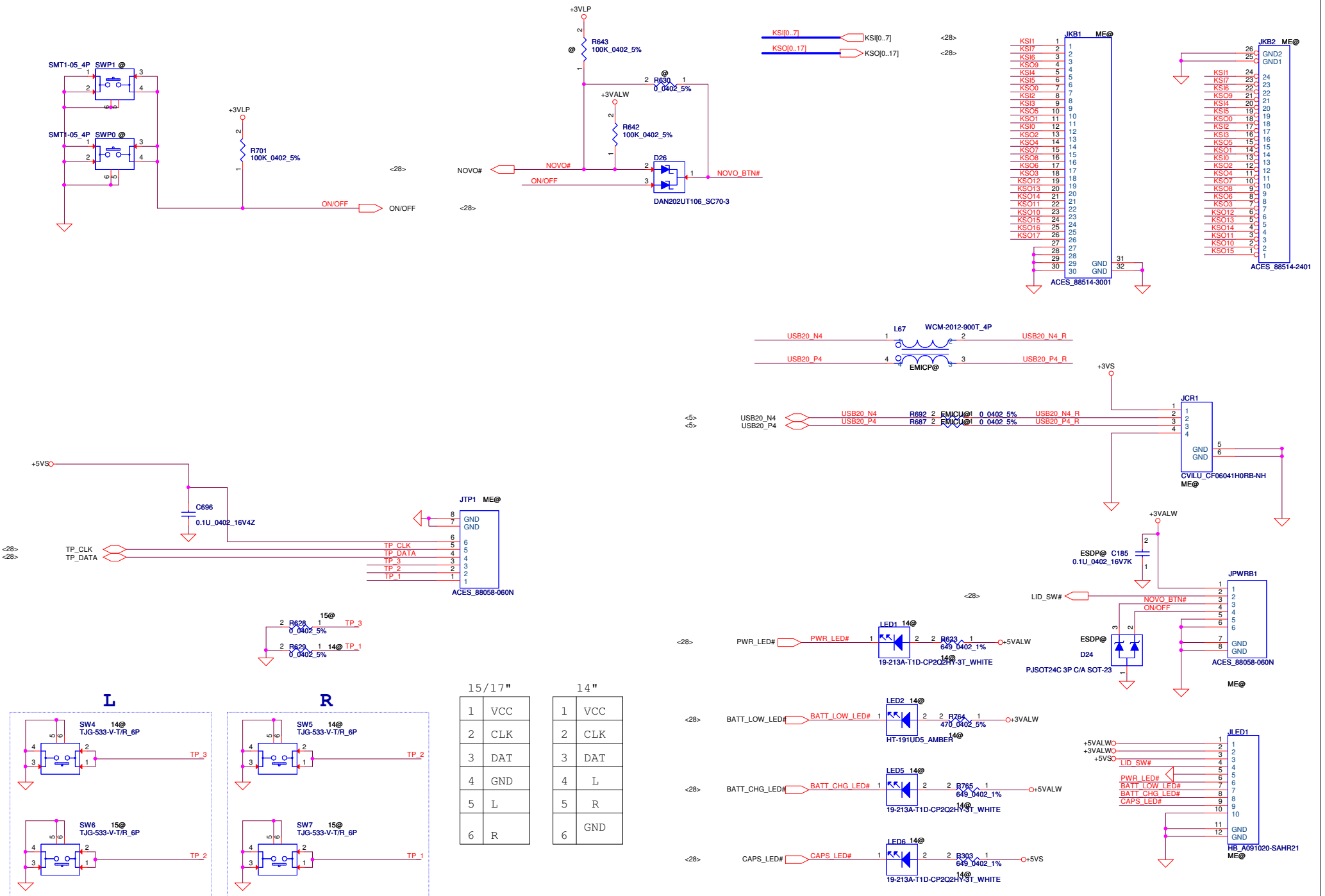


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn

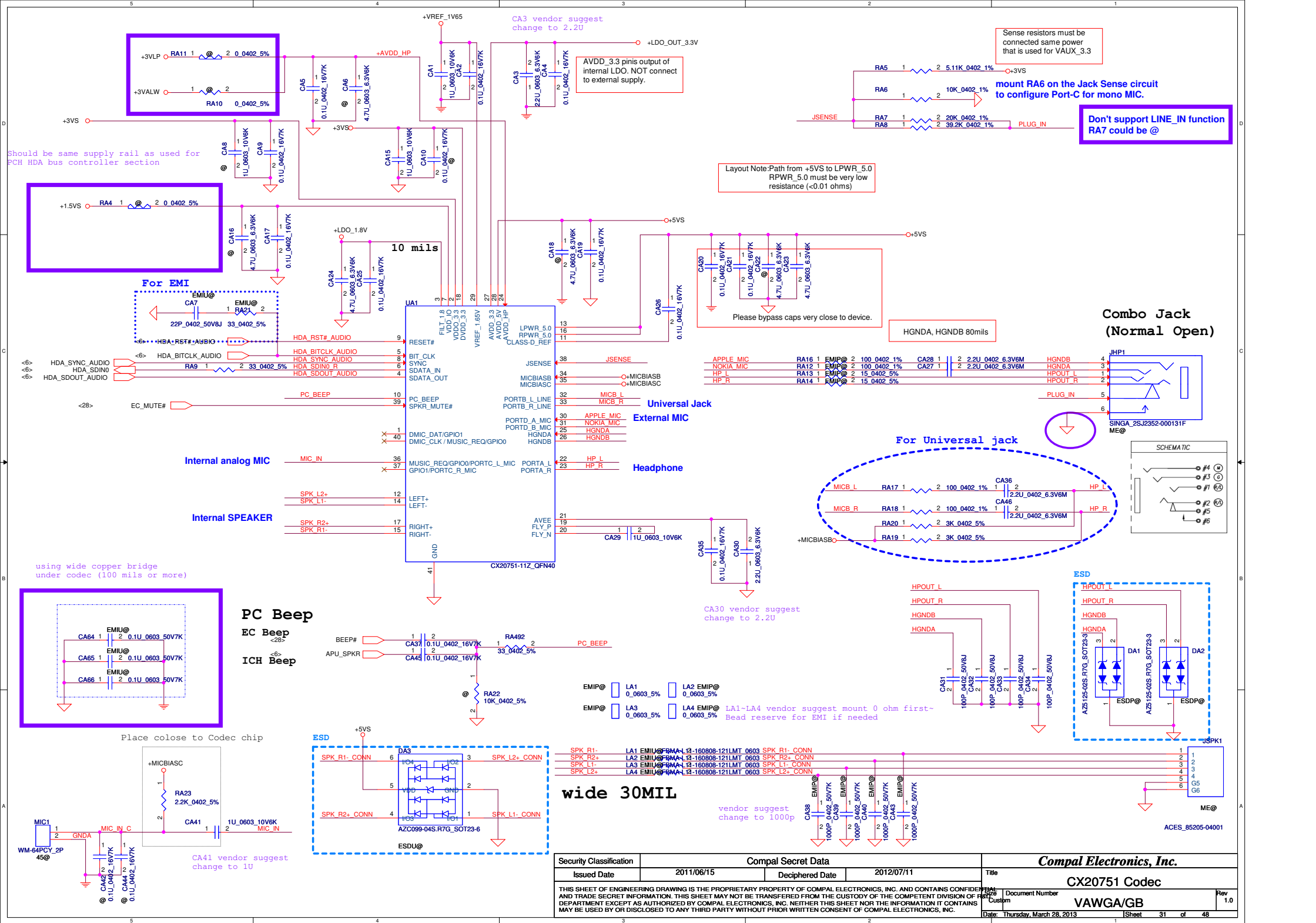


Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Fintek-Thermal IC/FAN/screw
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 1.0
				VAWGA/GB	
Date: Thursday, March 28, 2013				Sheet 29 of 48	



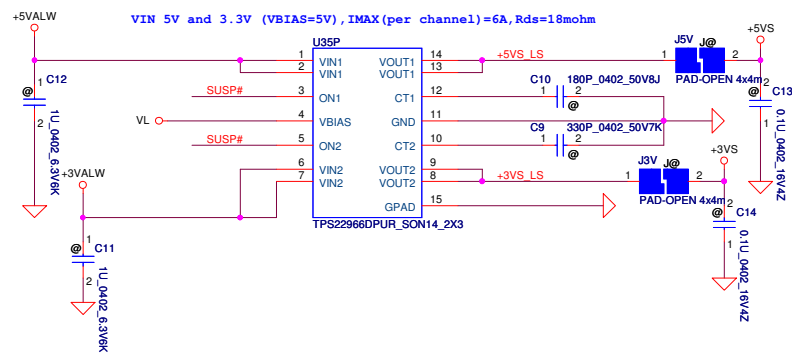
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2012/04/22		Deciphered Date		2015/04/22		Title	
										BIOS, I/O Port & K/B CONN/TP CONN/PBTN	
										Document Number	
										VAWGA/GB	
										Rev	
										1.0	
										Date	
										Thursday, March 28, 2013	
										Sheet	
										30	
										of	
										48	

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

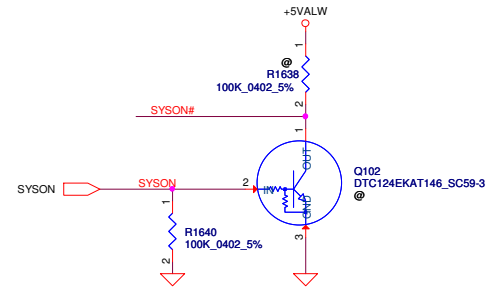
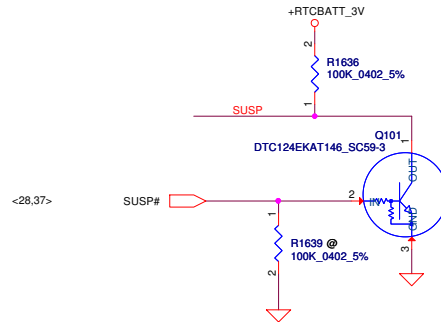
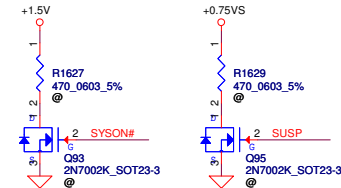
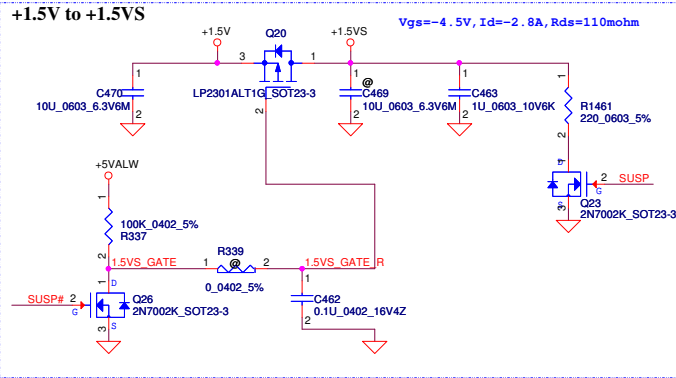
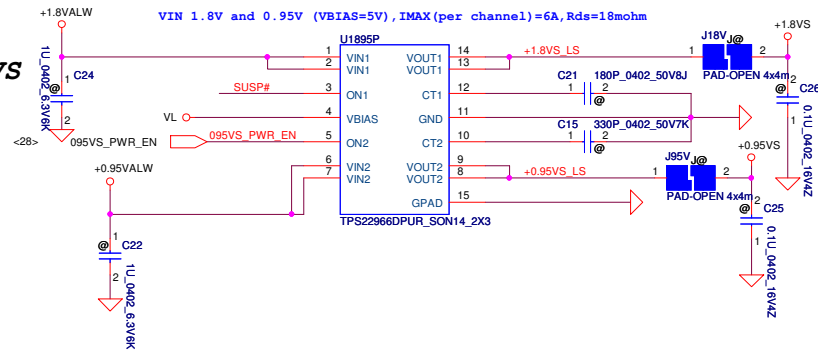


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	CX20751 Codec	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESPONSIBILITY TO ANY OTHER DIVISION OR PERSON WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc Number	Rev	
				Customer	1.0	
Date: Thursday, March 28, 2013				Sheet	31	of 48

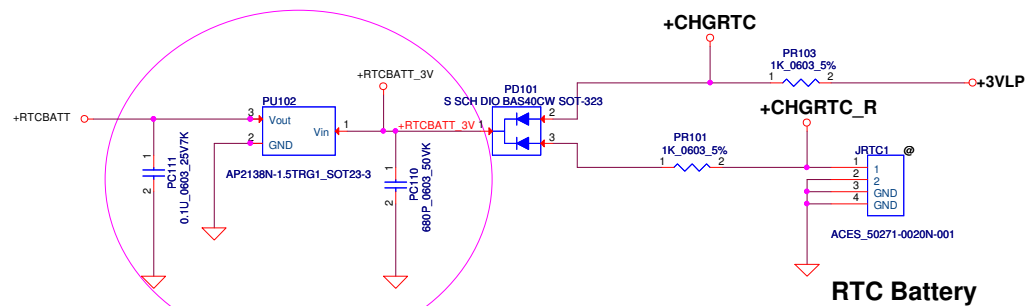
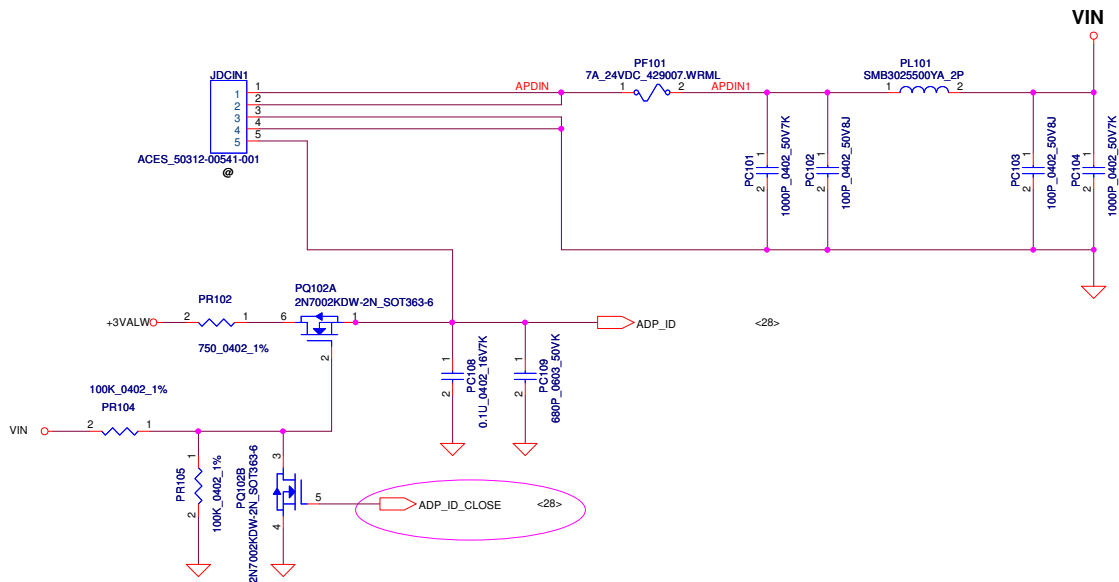
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



+1.8VALW TO +1.8VS
+0.95VALW TO +0.95VS
Load switch

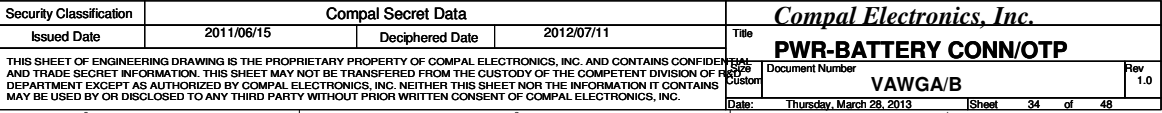


Security Classification		Compal Secret Data				Compal Electronics, Inc.				
Issued Date		2012/04/22		Deciphered Date		2015/04/22		Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PRODUCT DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		DC Interface								
		Document Number								Rev
		VAWG/GB								1.0
Date		Thursday, March 28, 2013				Sheet		32	of 48	

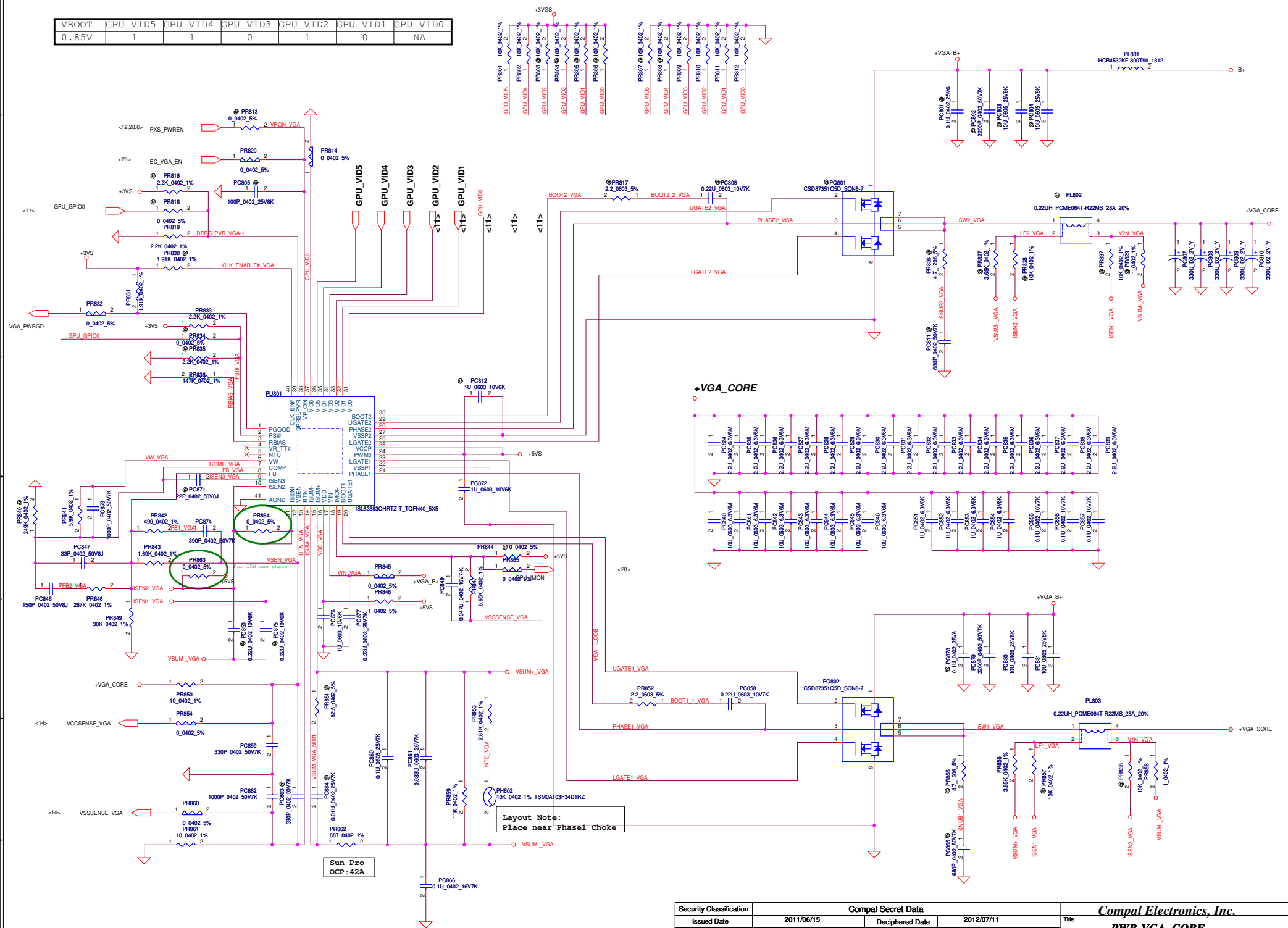


Need use +3.3V transfer to +1.5V LDO to APU side for Kaibini

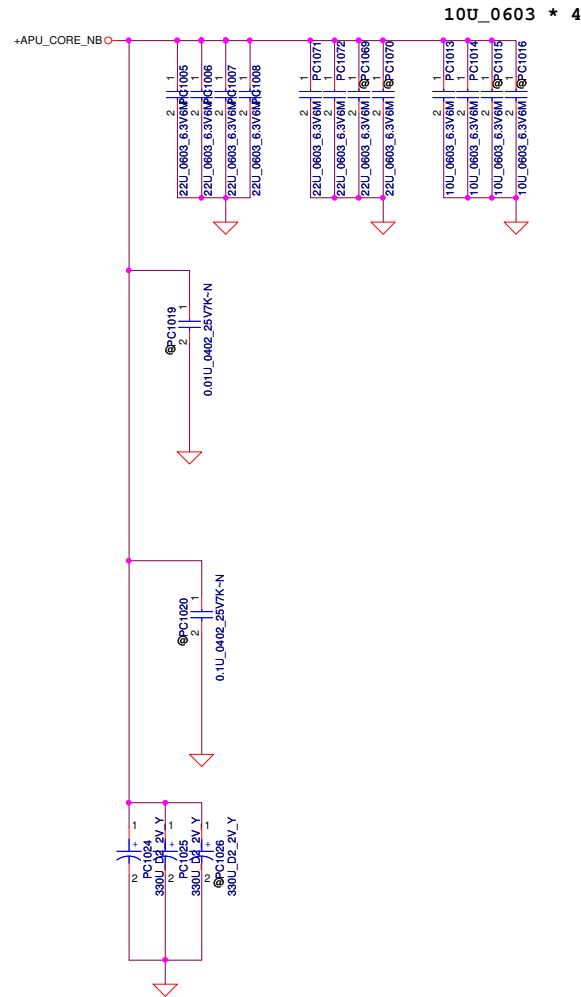
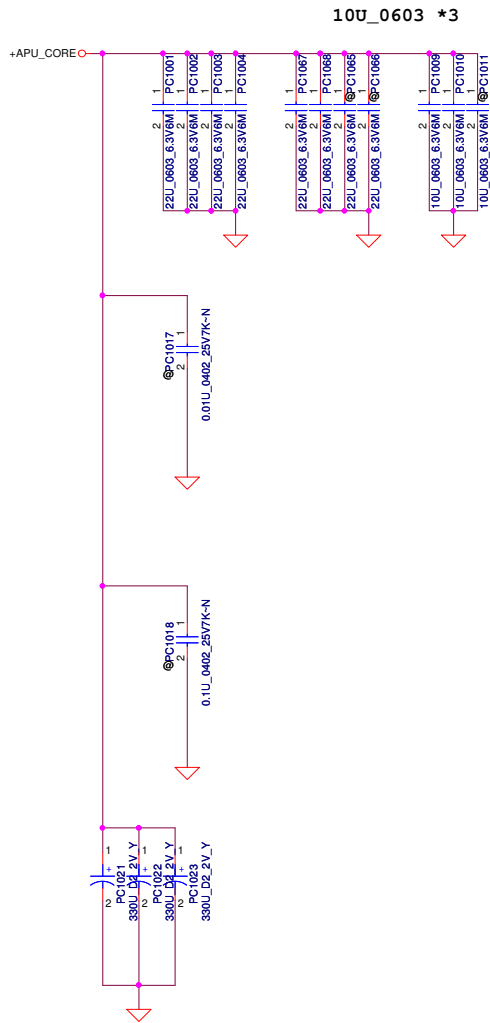
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	PWR-DCIN / RTC Battery
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF HEADQUARTERS OR ANY OTHER DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	VAWG/B
				Date:	Thursday, March 28, 2013
				Sheet	33 of 48
				Rev	1.0



VBOOT	GPU_VID5	GPU_VID4	GPU_VID3	GPU_VID2	GPU_VID1	GPU_VID0
0.85V	1	1	0	1	0	NA



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
				PWR-VGA_CORE	
				Document Number	
				VAWGA/GB	
				Rev	
				1.0	
				Date	
				Thursday, March 26, 2013	
				Sheet	
				39 of 48	



Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2011/07/08		Deciphered Date		2015/07/08		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FROM CUSTOMER TO CUSTOMER WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						PWR-PROCESSOR DECOUPLING			
						Document Number		Rev	
						VAWG/B		1.0	
						Date:		Sheet	
						Thursday, March 28, 2013		41 of 48	

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Version change list (P.I.R. List)

Page 1 of 1
for HW

Item	Reason for change	PG#	Modify List	Date	Phase
1	For share rom	28	Change SYS_PWRGD_EC from pin 86 to pin 32	12/17	DVT
2	For 095VS_PWR_EN pull down	28	Add R207	12/17	DVT
3	For VBIAS first raise up	12, 32	Change U1895V, U35P, U1895P VBIAS from +5VALW to VL	12/17	DVT
4	For follow VIWGP design	27	Change JUSB3 pin define	12/18	DVT
5	For Audio Precision	31	Change CA36, CA46 from 1U to 2.2U	12/21	DVT
6	For SYS_PWRGD_EC pull down	28	Add R208	12/24	DVT
7	For share rom	28	Change R1575, R1576 to 100K	12/24	DVT
8	For reserve EC +3VL	28 05	Add J11, J12 and modify +3VALW to +3V_EC	12/24	DVT
9	For share ROM	05	modify ROM net-name & resistor value	12/24	DVT
10	For common VIWGP design	22	modify R106, R107 to 22ohm	12/24	DVT
11	For power S3 reduction	28	Change EC_INVT_PWM to ADP_ID_CLOSE	12/25	DVT
12	For common VIWGP design	23	Change JODD1 symbol	12/27	DVT
13	For reserve wake on wlan function	26	Add R1500	12/27	DVT
14	For 1.5VS discharge	32	Change R339 to 0ohm, mount Q23 & R1461	12/29	DVT
15	For AMD suggest	4	Change R576 to 0ohm	12/29	DVT
16	For VGA sequence	12	Delete R123 & C40, change C28, C27 to 2200P	12/29	DVT
17	For +3VALW APU Power Consumption	7	Add R582	01/03	DVT
18	For ESD request	22 28 40	Add C600, C601, PC6601, PC6602	01/03	DVT
19	For no support DC wake & LID function	28	Pull high only SMB & RST use +3V_EC, other use +3VALW	01/04	DVT
20	For reserve cost down experiment	30	Add R630, R643	01/04	DVT
21	For Common VIWGP	30	Change SW4, SW5, SW6, SW7 footprint	01/04	DVT
22	For instant plug/unplug AC has beep sound	31	@RA22	01/04	DVT
23	For Crystal Capactance fine tune	5 6 12	Modify C794, C795, C682, C686, CV36, CV37 value	01/09	DVT

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PIR (PWR)	
Size Custom		Document Number		Rev	
Date		Thursday, March 28, 2013		Sheet 43 of 48	
C38-G series Chief River Schematic		1.0			

Version change list (P.I.R. List)

Page 1 of 1
for HW

Item	Reason for change	PG#	Modify List	Date	Phase
1	For EMI request	30	Change L67 to EMICP@, Change R692,R687 to EMICU@	02/02	PVT
2	For Share ROM recoverable solution as original method	05	Add RP12	02/02	PVT
3	For BIOS post time	06	Pull high PXS_PWREN to +3VS by RP14	02/02	PVT
4	For ZiZi noise	31	Change AVDD_HP from +3VS to +3VLP	02/02	PVT
5	For follow KABINI latest CRB	04	@ R576,C164,C342	02/02	PVT
6	For APU control PWM only	21	Delete R1465	02/02	PVT
7	For Corret Net-name to prevet confuse	04 21	Change TL_INVT_PWM, TL_ENVDD to APU_INVT_PWM, APU_ENVDD	02/02	PVT
8	For Reserve DDC CLK DATA pull high	22	Add R693, R697	02/02	PVT
9	For Common Intel project	30	Change R623,R765,R303 to 620ohm	02/02	PVT
10	For Common Intel project	23	Reserve R551	02/02	PVT
11	For reduce BOM	31	Delete RA3, and Change RA4 to short-pad	02/05	PVT
12	For reduce BOM	26	Change R1498,R1499 from 0 ohm to 100 ohm	02/05	PVT
13	For reduce BOM	11 12 13 14	Change RV43, LV1, LV2, LV3, LV4, LV5, LV6, RV16, RV17, LV7, LV8, LV9, LV10 to short-pad	02/05	PVT
14	For better location	14 18 19	CV72 <-> CV171 ; CV60 <-> CV70 ; CV154 <-> CV191	02/05	PVT
15	For reduce BOM	21	Change R1463 from 0 ohm to short-pad	02/06	PVT
16	For better audio precision performance	31	Change CA27,CA28 from 1U to 2.2U	02/08	PVT
17	For reduce BOM & layout concern	07	Delete C195	02/16	PVT
18	For test point request	22	Add T49, T58 on JCRT1	02/18	PVT
19	For ESD request	25	Add C173, C178	02/18	PVT
20	For reduce BOM	05	Change R112, R115, R116, R119, R125, R126 to short-pad	02/18	PVT
21	For Crystal timing	06	Change C682 from 18P to 22P	02/20	PVT
22	For ESD request	30	Change D24 from ESDU@ to ESDP@, Part number from SCA00000E00 to SCA00001G00	02/23	PVT
23	For EMI request	21 27 30	Change L58,L51,L55,L66,L67 from SM070000K00 to SM070000Z00	02/23	PVT

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PIR (PWR)	
Size		Document Number		Rev	
Custom		C38-G series Chief River Schematic		1.0	
Date		Thursday, March 28, 2013		Sheet 44 of 48	

*Page 1 of 1
for PWR*

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	PIR (PWR)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	C38-G series Chief River Schematic ^{1.0}
Date:		Thursday, March 28, 2013		Sheet	45 of 48

Mars XT VRAM STRAP

2G

1G

Vendor	PS_3[2]	PS_3[1]	PS_3[0]	R_pu	R_pd
K4W2G1646E-BC1A SA000068U00	0	0	0	RV20 NC	RV27 4.75K
MT41J128M16JT-093G:K SA000067500	0	0	1	RV20 8.45K	RV27 2K
H5TQ2G63DFR-N0C SA000065300	0	1	0	RV20 4.53K	RV27 2K
H5TC2G63FFR-11C SA00006H400	1	0	0	RV20 4.53K	RV27 4.99K
K4W1G1646G-BC11 SA00004GS00	0	1	1	RV20 6.98K	RV27 4.99K
H5TQ1G63EFR-11C SA000041SB0	1	1	1	RV20 4.75K	RV27 NC

MS2G@ X7646738L01
MM2G@ X7646738L02
OLDMH2G@ X7646738L09
NEWMH2G@ X7646738L10
MS1G@ X7646738L03
MH1G@ X7646738L04

SUN PRO VRAM STRAP

2G

1G

Vendor	PS_3[2]	PS_3[1]	PS_3[0]	R_pu	R_pd
K4W4G1646B-HC11 SA000068R00	0	0	0	RV20 NC	RV27 4.75K
MT41K256M16HA-107G:E SA000065D00	0	0	1	RV20 8.45K	RV27 2K
H5TQ4G63MFR-11C SA00006DG00	0	1	0	RV20 4.53K	RV27 2K
K4W2G1646E-BC1A SA000068U00	0	1	1	RV20 6.98K	RV27 4.99K
MT41J128M16JT-093G:K SA000067500	1	1	0	RV20 3.4K	RV27 10K
H5TC2G63FFR-11C SA00006H400	1	0	0	RV20 4.53K	RV27 4.99K
H5TQ2G63DFR-N0C SA000065300	1	1	1	RV20 4.75K	RV27 NC

SS2G@ X7646738L05
SM2G@ X7646738L06
SH2G@ TBD
SS1G@ X7646738L07
SM1G@ X7646738L08
NEWSH1G@ X7646738L13
OLDSH1G@ X7647538L01

Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

VDDR3(3.3VGS)

PCIE_VDDC(0.95VGSV)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

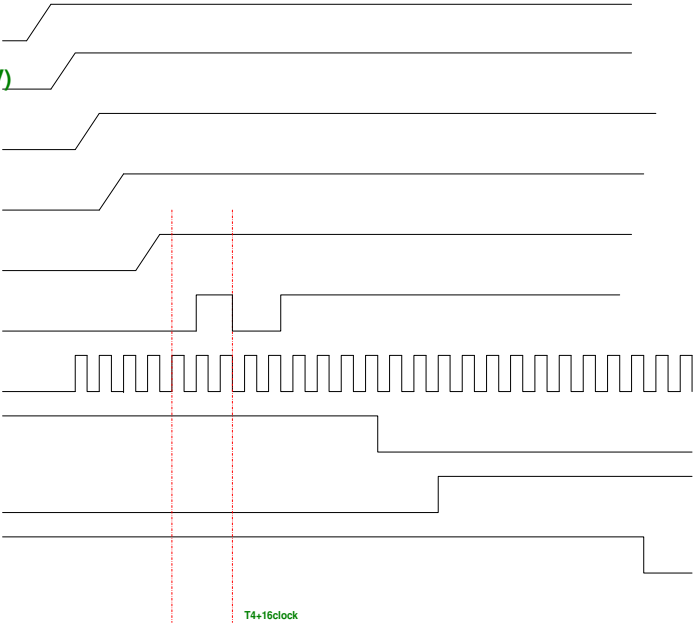
PERSTb

REFCLK

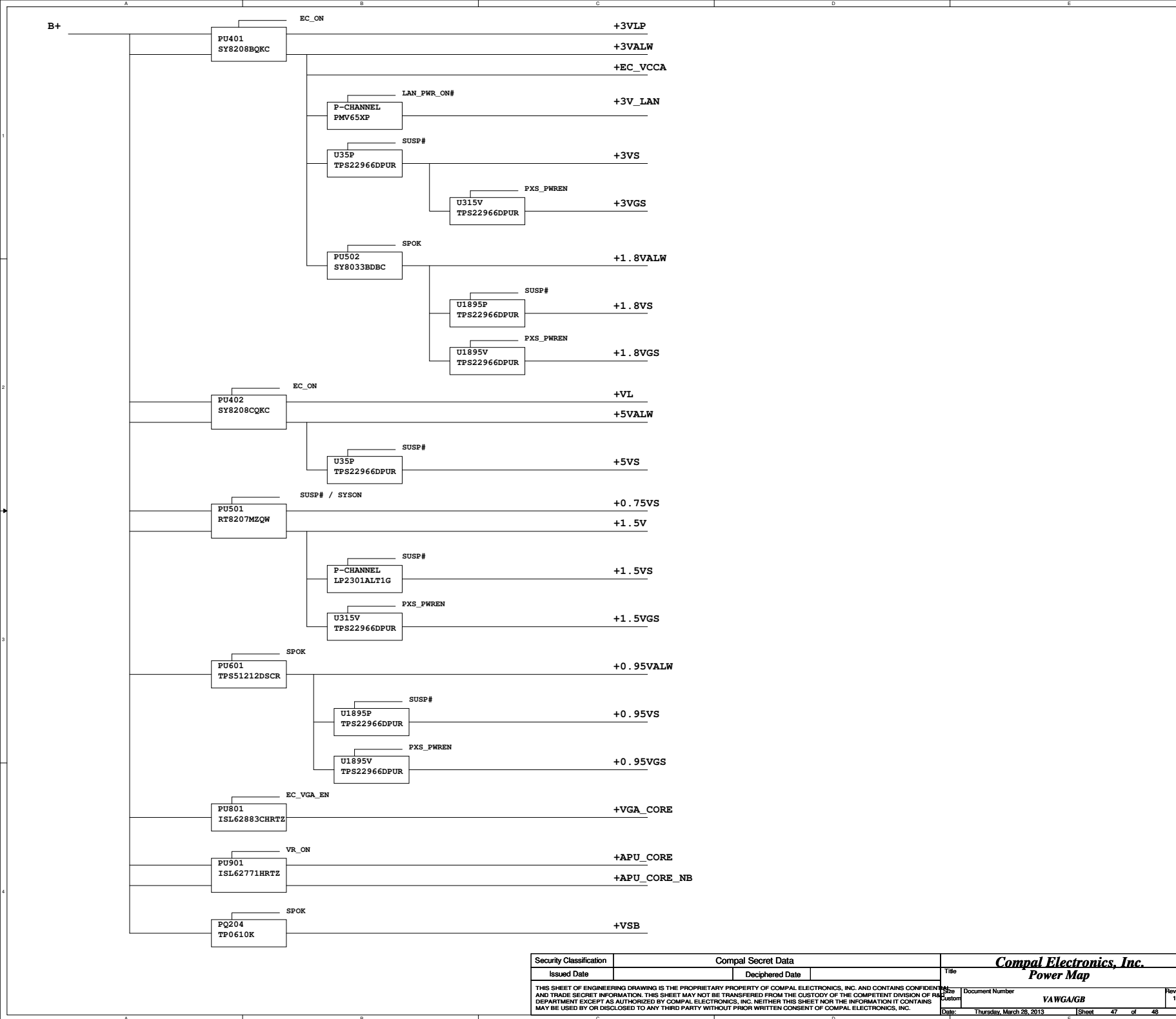
Straps Reset

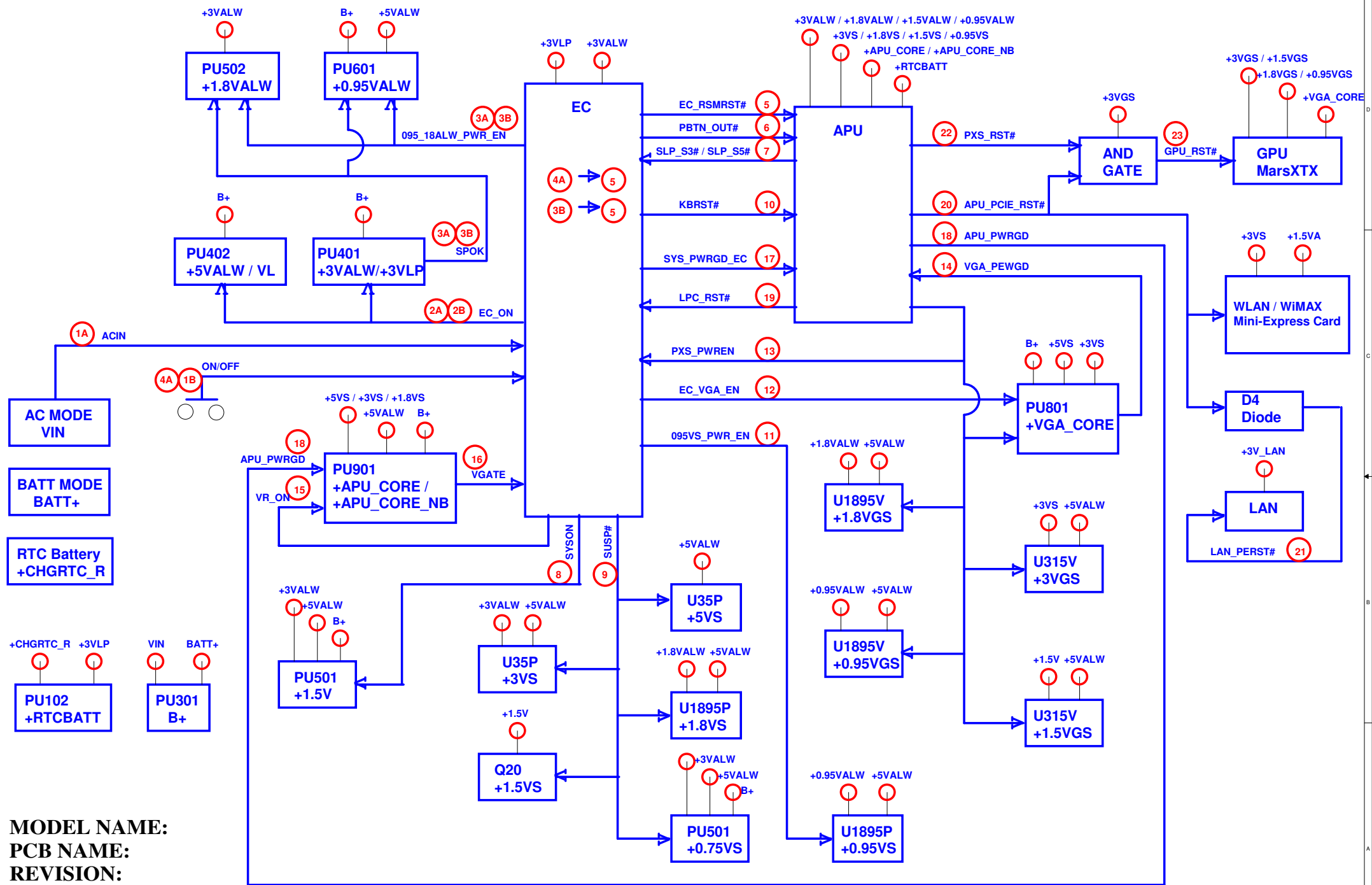
Straps Valid

Global ASIC Reset



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	VGA Notes List
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				VAWGA/GB	1.0
				Date	Thursday, March 28, 2013
				Sheet	46 of 48





MODEL NAME:
PCB NAME:
REVISION:
DATE: 2011/11/23

COMPAL CONFIDENTIAL

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	Power sequence
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF HEAD CUSTOMER DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 1.0
				Date:	Sheet of