Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M SFF core logic

ULV core logic board

2009/06/23

Security Classification	Compal Secret Data		
Issued Date	2006/02/20	Deciphered Date	2009/02/20

Compal Electronics, Inc.		
Title: *Cover Sheet*		
Size: Custom	Document Number: *LS-5341P*	Rev: 1.0
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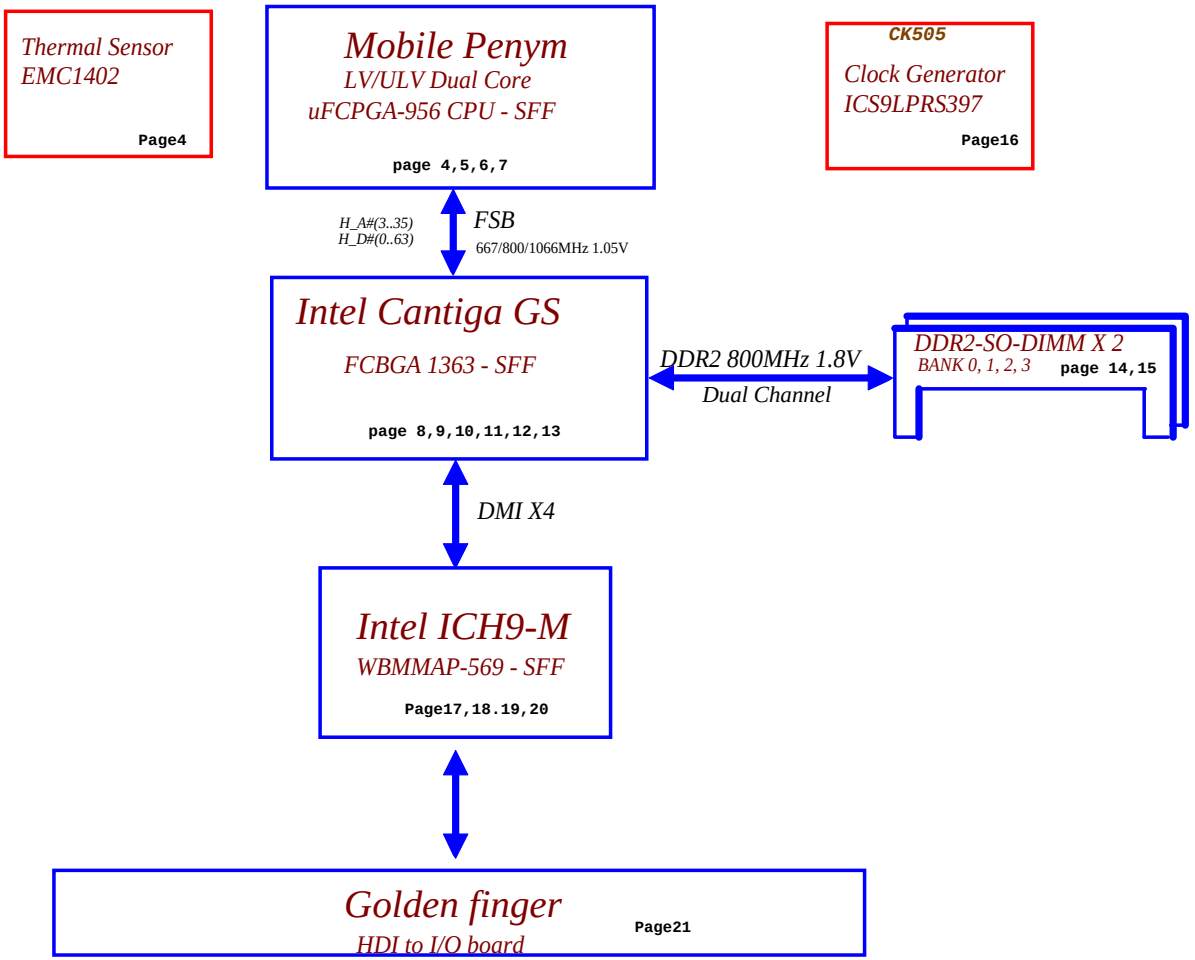
ULV



A31 :
CPU-->SA000038J1L(S IC AV80585VG0091M SLGAM R0 1.2G FCBGA 956P)
CPU-->SA00003BX1L(S IC A31 AV80585UG0132M QLKK R0 1.3G)
NB-->SA00002RQ0L(S IC AC82GS45 SLB92 B3 FCBGA 1363 A31 !)
SB-->SA00001YC3L(S IC AM82801IUX SLB8N A FCBGA ICH9M A31!)

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Title: Block Diagram			
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Voltage Rails (O MEANS ON X MEANS OFF)

power plane / State	+B	+5VALW +3VALW VL	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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Title: Notes List

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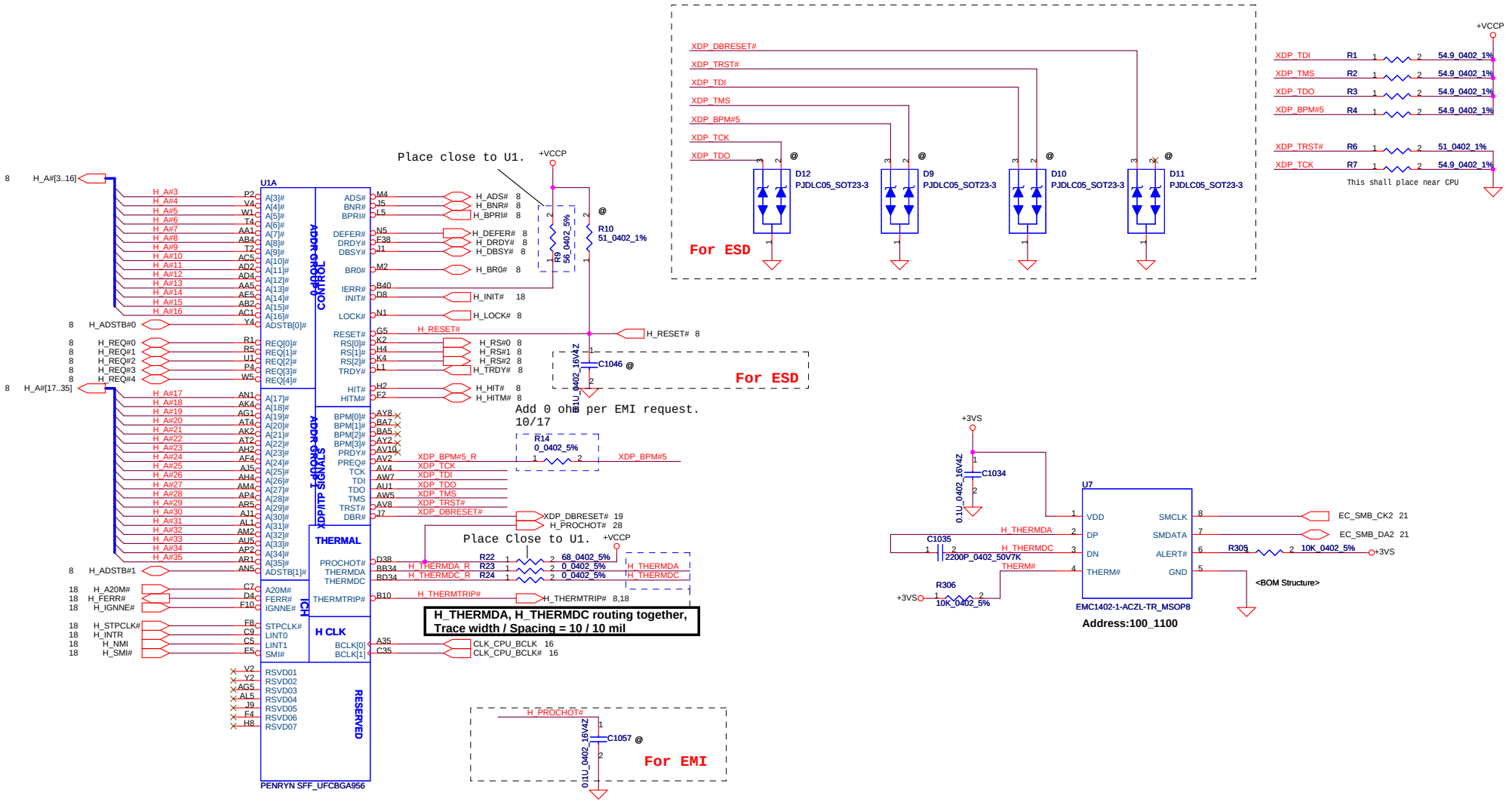

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Issued Date	2006/02/20	Deciphered Date	2009/02/20

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Title: **Penryn(1/3)-AGTL+/ITP-XDP**

Size	Document Number	Rev
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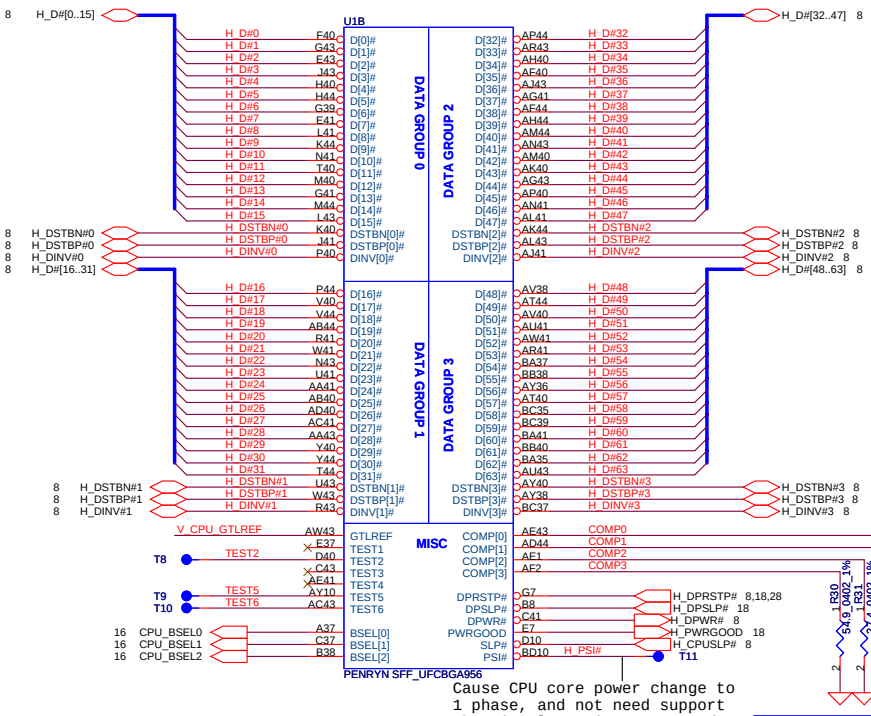
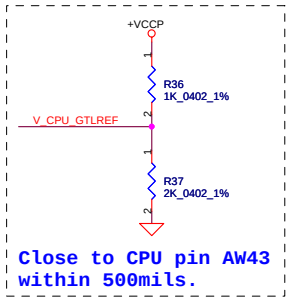


Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

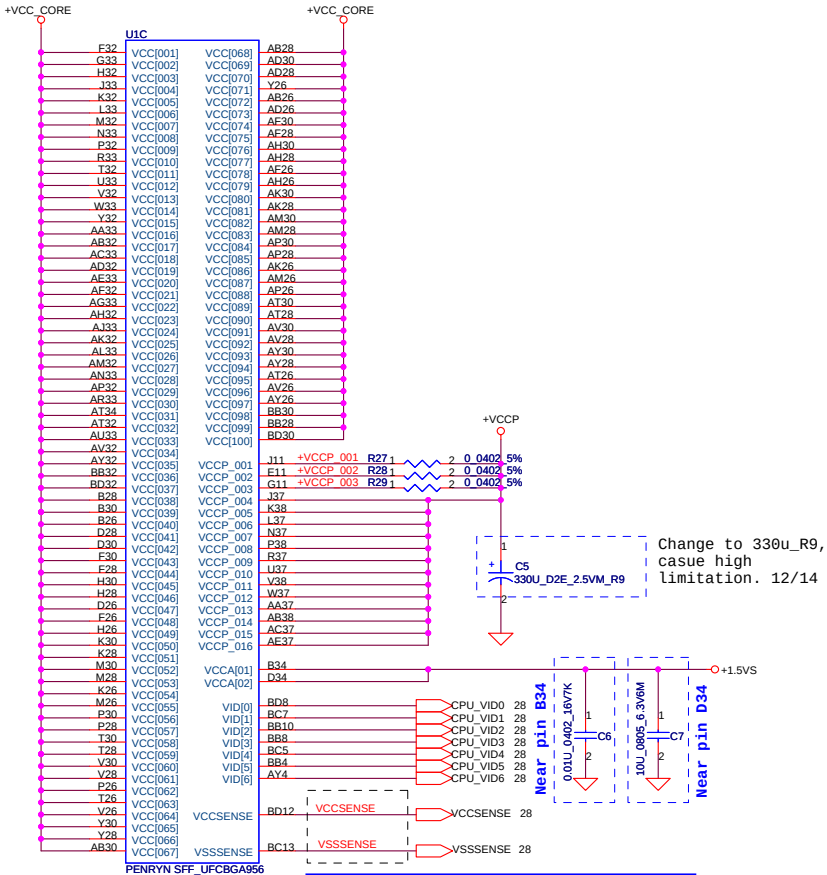
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

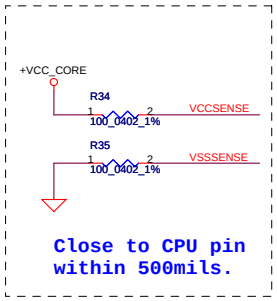
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



Close to CPU pin AW43 within 500mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

Security Classification	Compal Secret Data		
Issued Date	2006/02/20	Deciphered Date	2009/02/20

Compal Electronics, Inc.

Title: **Penryn(2/3)-AGTL+/ITP-XDP**

Size	Document Number	Rev
Custom	LS-5341P	1.0

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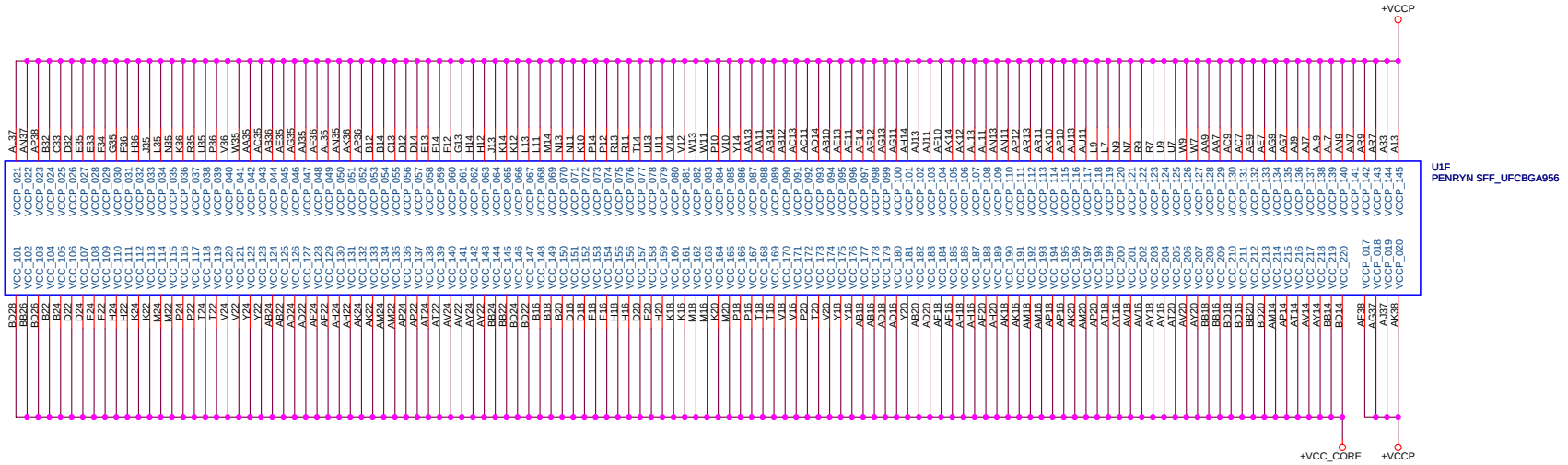

Security Classification	Compal Secret Data		
Issued Date	2006/02/20	Deciphered Date	2009/02/20

Compal Electronics, Inc.

Title: **Penryn(3/3)-Power**

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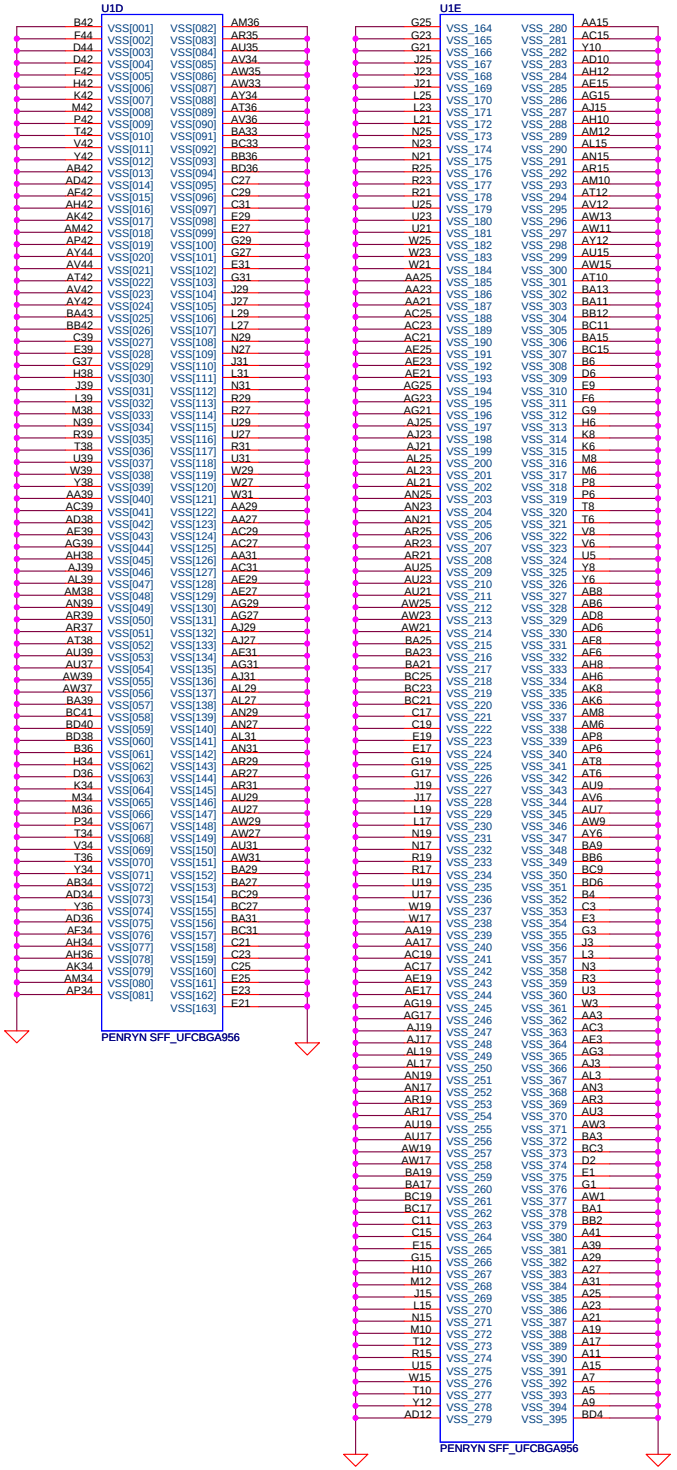
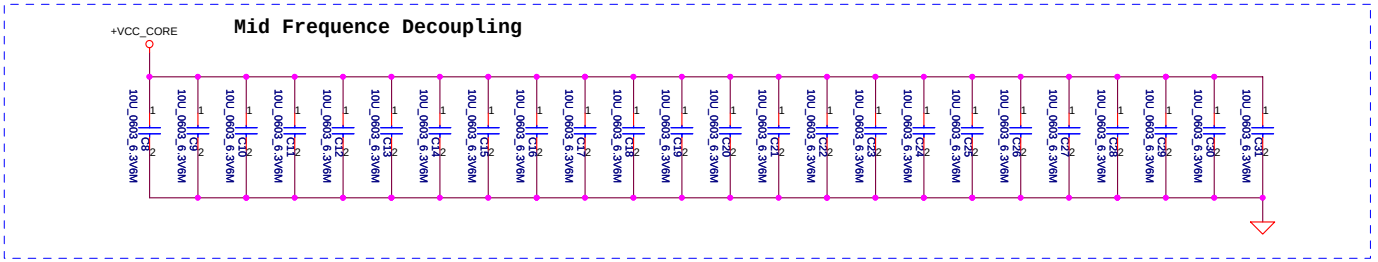
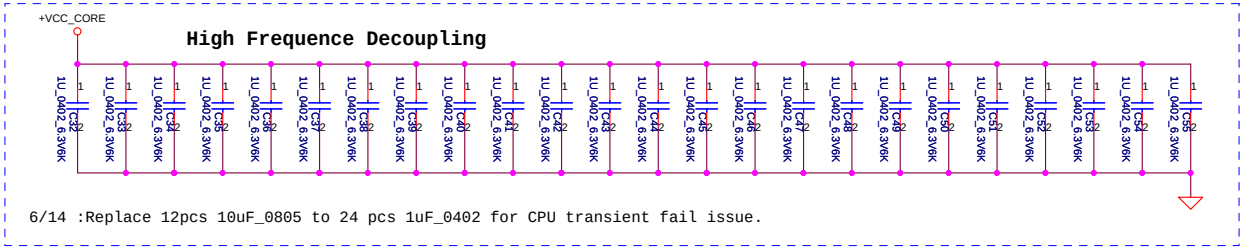
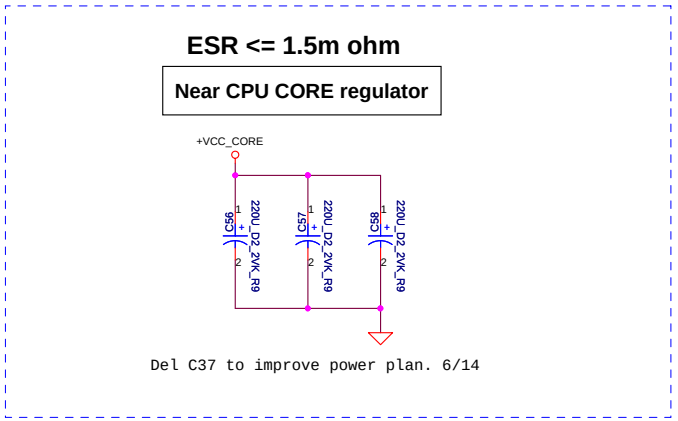


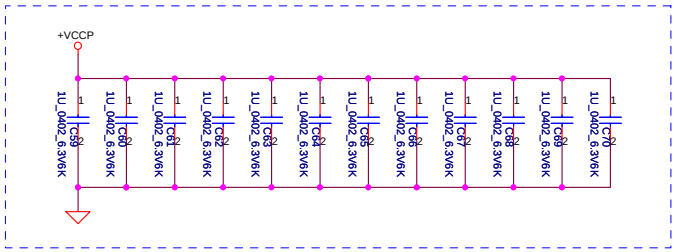




6/14 :Replace 12pcs 10uF_0805 to 24 pcs 1uF_0402 for CPU transient fail issue.



Del C37 to improve power plan. 6/14



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Title: **Penryn(3/3)-GND/Bypass**

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layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Trace < = 500mils

layout note:
Place them close to U4 pin BC51.

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

within 100 mils from NB

Near B6 pin

Layout Note: V_DDR_MCH_REF trace width and spacing is 20/20.

For ESD

CANTIGA GMCH SFF_FCBGA1363

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Compal Electronics, Inc.

Title: Cantiga(1/6)-AGTL/DMI/DDR

Size	Document Number	Rev
Custom	LS-5341P	1.0

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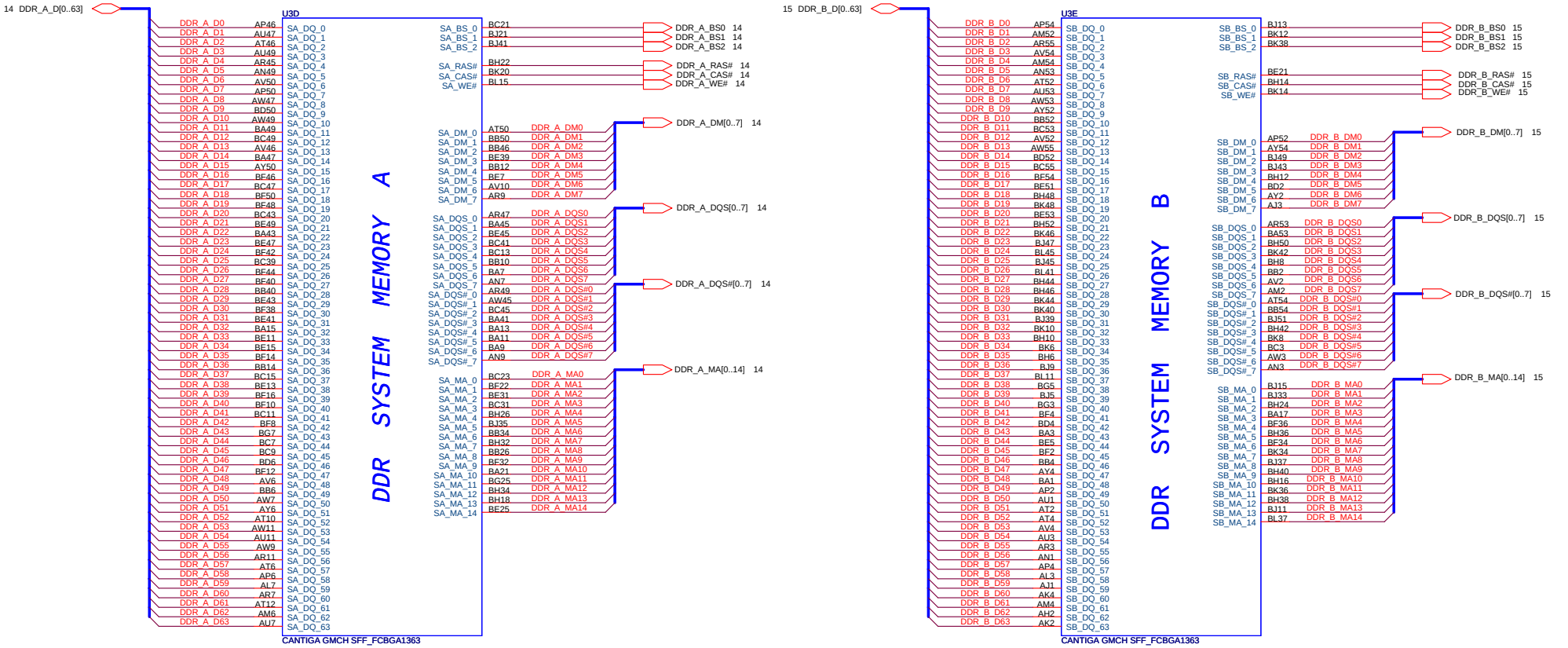

Security Classification	Compal Secret Data		
Issued Date	2006/02/20	Deciphered Date	2009/02/20

Compal Electronics, Inc.

Title: **Cantiga(2/6)-DDR2 A/B CH**

Size	Document Number	Rev
Custom	LS-5341P	1.0

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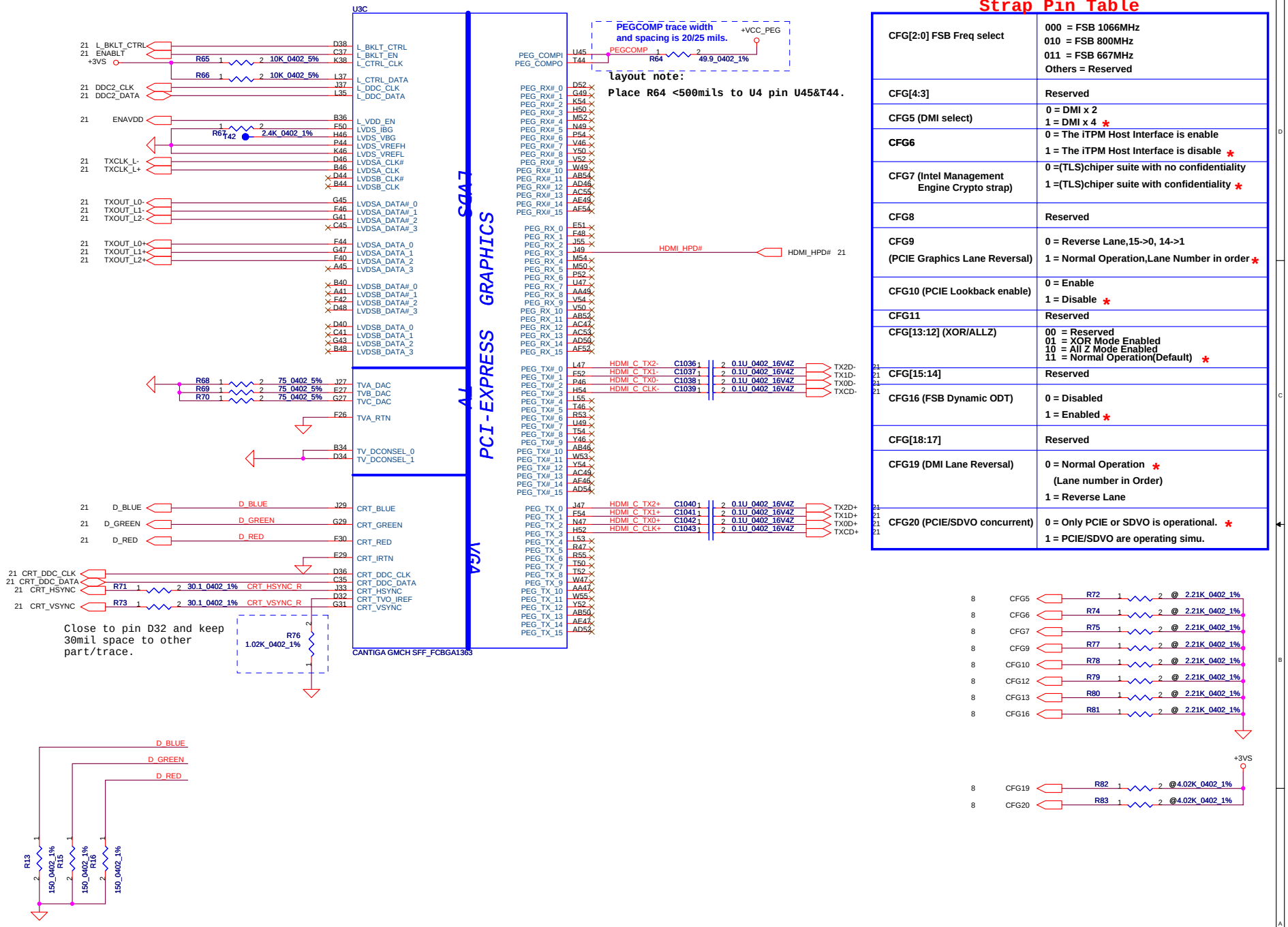

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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Title: **Cantiga(3/6)-VGA/LVDS/TV**

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Custom	LS-5341P	1.0

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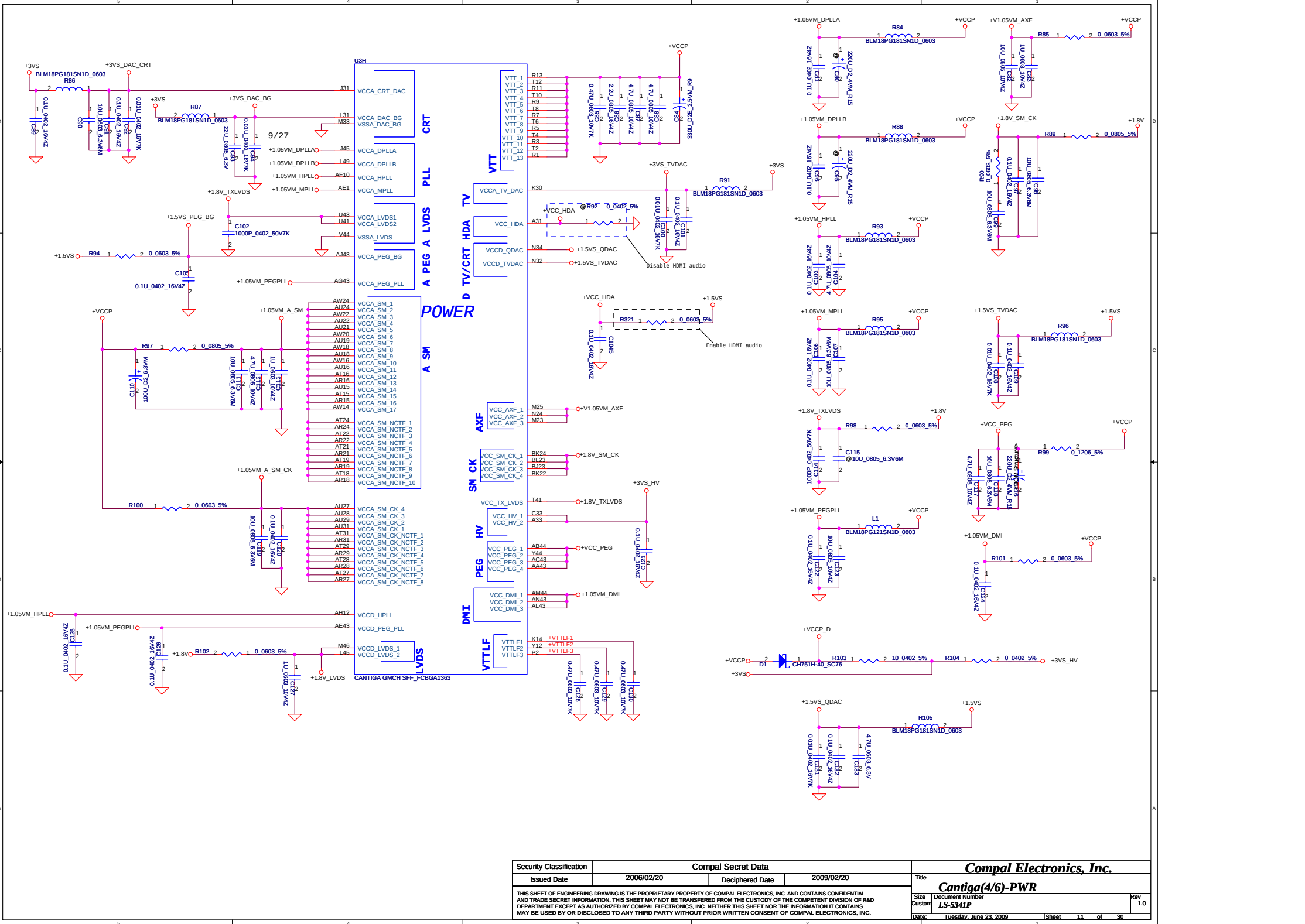

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **Cantiga(4/6)-PWR**

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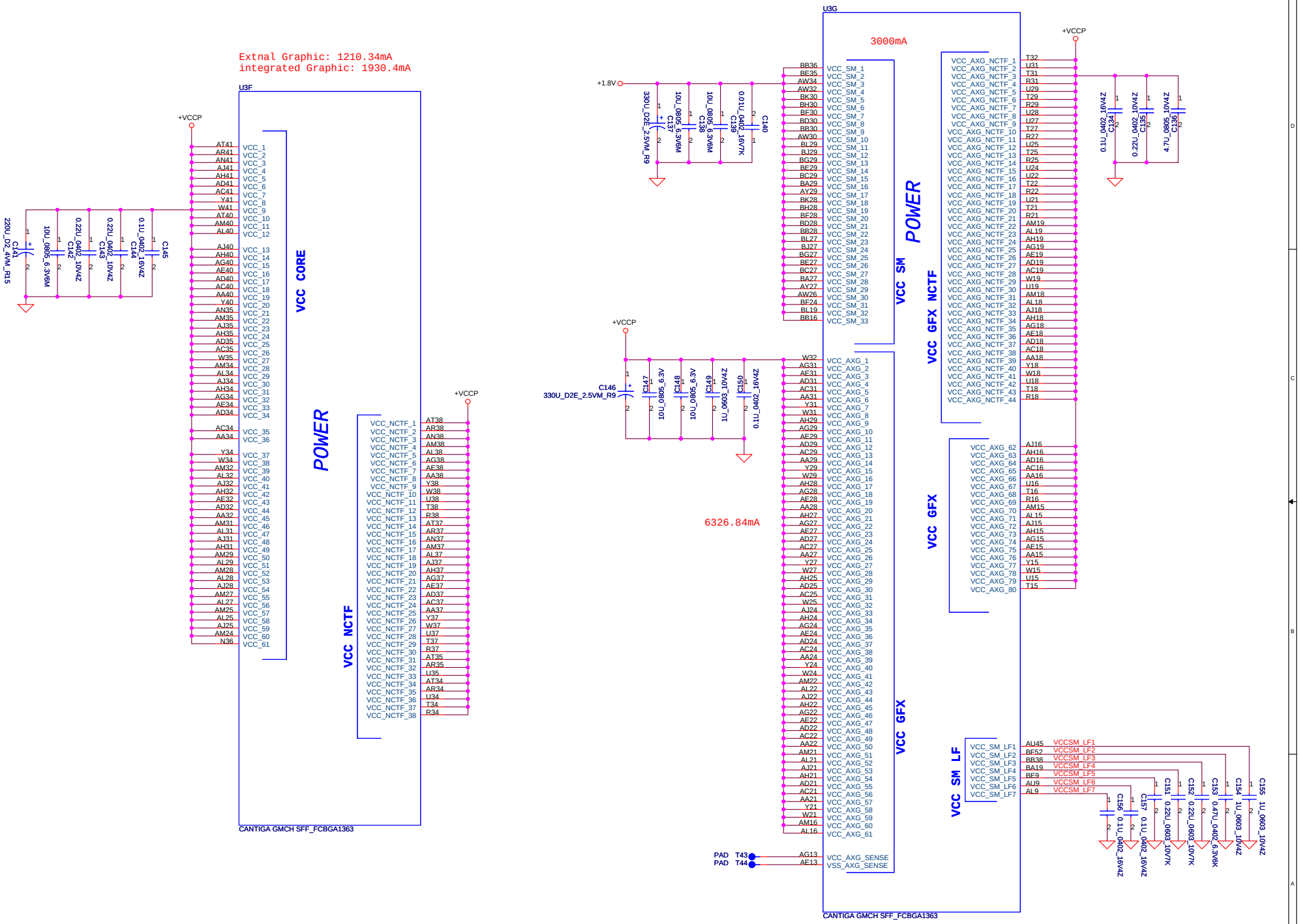

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Title: **Cantiga(5/6)-PWR/GND**

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Custom	LS-5341P	1.0

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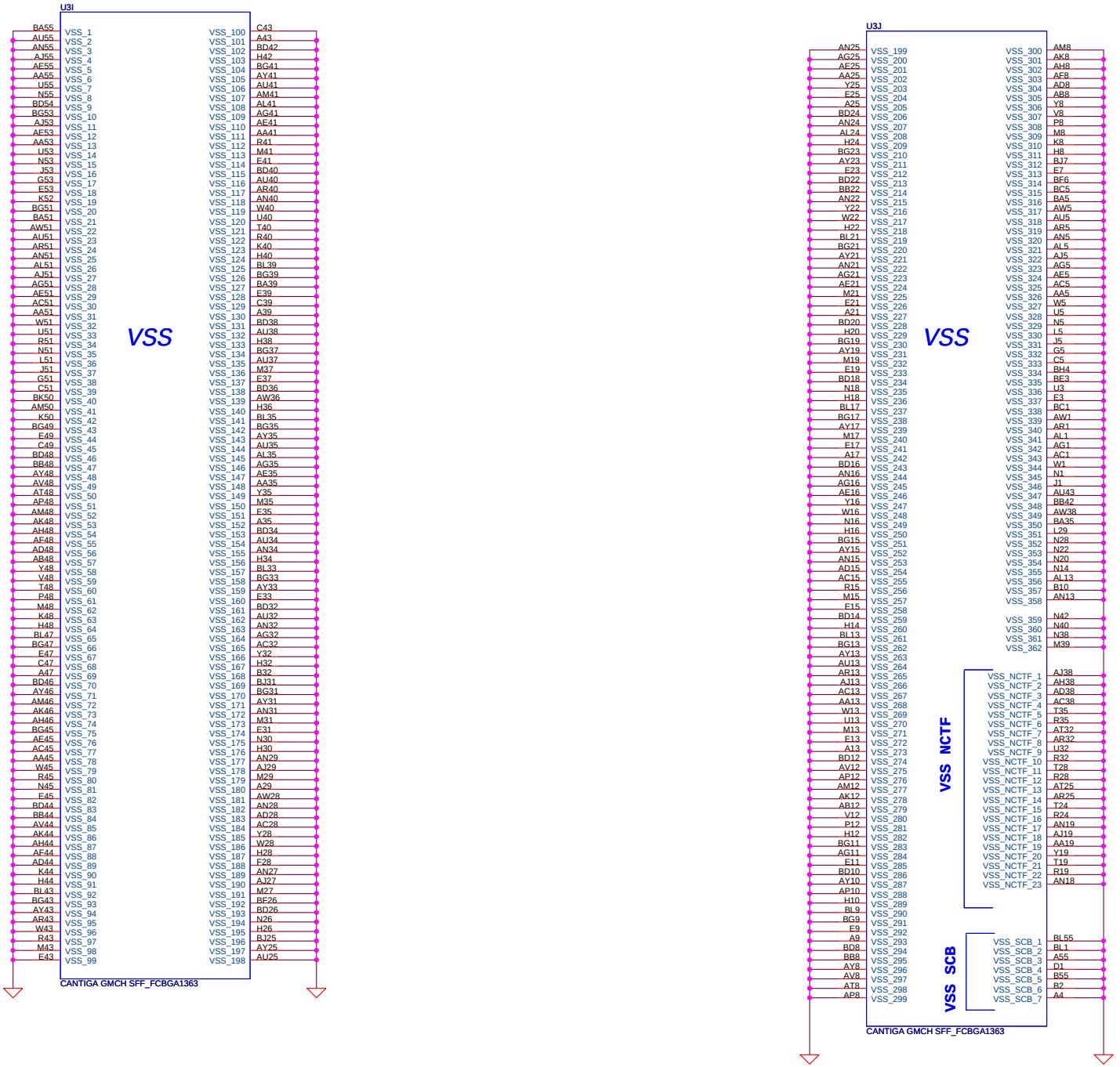

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Compal Electronics, Inc.

Title: **Cantiga(6/6)-PWR/GND**

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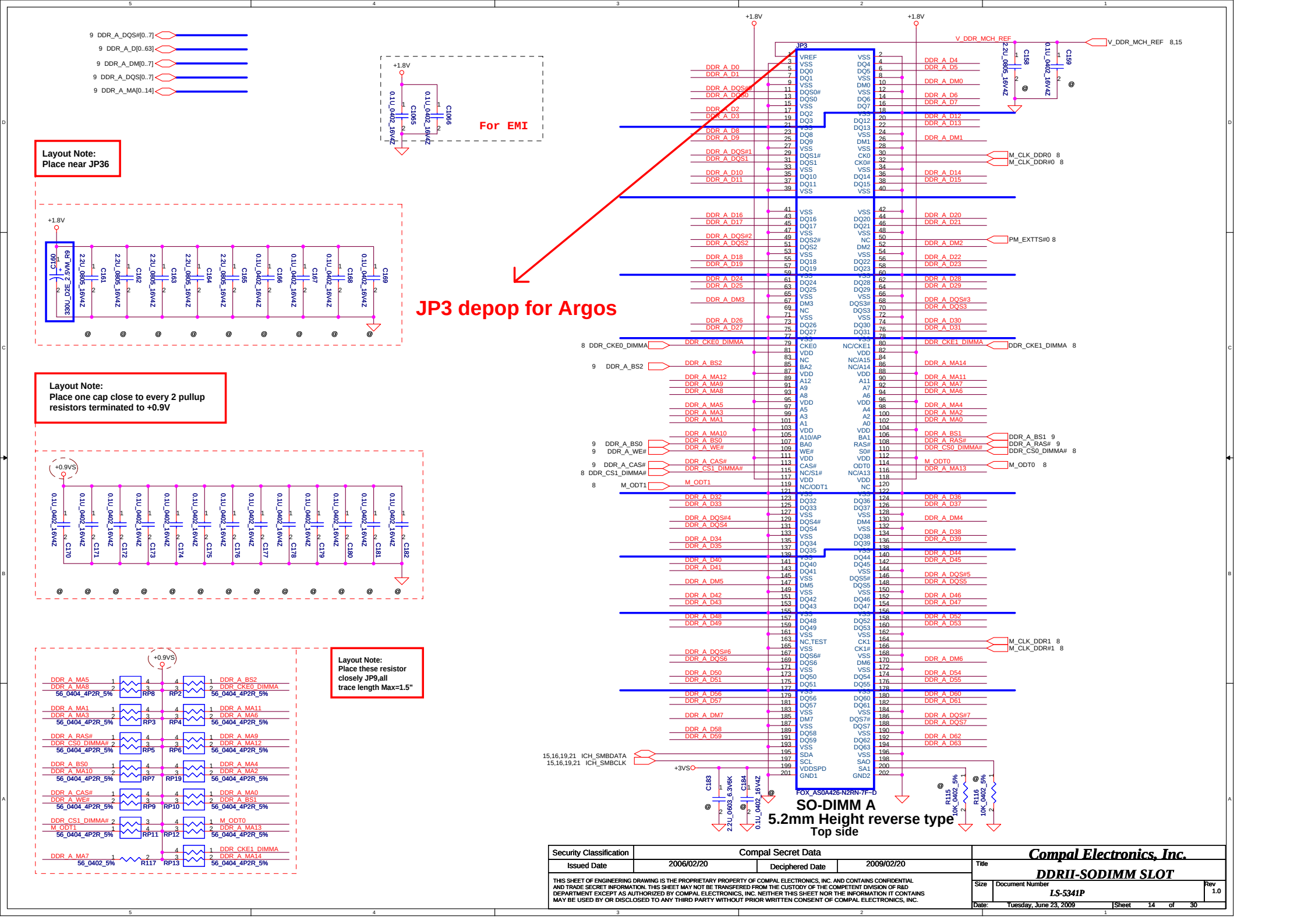

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Title: **DDRII-SODIMM SLOT**

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9 DDR_B_DQS#[0..7]
9 DDR_B_D[0..63]
9 DDR_B_DM[0..7]
9 DDR_B_DQS[0..7]
9 DDR_B_MA[0..14]

Layout Note:
Place near JP34

+1.8V
C187 330U_D2E_2.5VM_R9
C188 2.2U_0805_16V4Z
C189 2.2U_0805_16V4Z
C190 2.2U_0805_16V4Z
C191 2.2U_0805_16V4Z
C192 2.2U_0805_16V4Z
C193 0.1U_0402_16V4Z
C194 0.1U_0402_16V4Z
C195 0.1U_0402_16V4Z
C196 0.1U_0402_16V4Z

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

+0.9VS
C197 C198 C199 C200 C201 C202 C203 C204 C205 C206 C207 C208 C209 0.1U_0402_16V4Z

Layout Note:
Place these resistor closely JP10,all trace length Max=1.5"

+0.9VS
RP14 RP15 RP16 RP17 RP18 RP1 RP20 RP21 RP22 RP23 RP24 RP25 RP26 56_0404_4P2R_5%
R120 56_0402_5%

+1.8V
C1068 C1067 0.1U_0402_16V4Z
For EMI

+1.8V
V_DDR_MCH_REF
V_DDR_MCH_REF 8,14
C185 2.2U_0805_16V4Z
C186 0.1U_0402_16V4Z

JP4

		VREF	VSS	2			
		VSS	DQ4	4	DDR_B_D4		
DDR_B_D0	5	DQ0	DQ5	6	DDR_B_D5		
DDR_B_D1	7	DQ1	VSS	8			
	9	VSS	DM0	10	DDR_B_DM0		
DDR_B_DQS#0	11	DQS0#	VSS	12			
DDR_B_DQS0	13	DQS0	DQ6	14	DDR_B_D6		
	15	VSS	DQ7	16	DDR_B_D7		
DDR_B_D2	17	DQ2	VSS	18			
DDR_B_D3	19	DQ3	DQ12	20	DDR_B_D12		
	21	VSS	DQ13	22	DDR_B_D13		
DDR_B_D8	23	DQ8	VSS	24			
DDR_B_D9	25	DQ9	DM1	26	DDR_B_DM1		
	27	VSS	VSS	28			
DDR_B_DQS#1	29	DQS1#	CK0	30	M_CLK_DDR2	8	
DDR_B_DQS1	31	DQS1	CK0#	32	M_CLK_DDR#2	8	
	33	VSS	VSS	34			
DDR_B_D10	35	DQ10	DQ14	36	DDR_B_D14		
DDR_B_D11	37	DQ11	DQ15	38	DDR_B_D15		
	39	VSS	VSS	40			
	41	VSS	VSS	42			
DDR_B_D16	43	DQ16	DQ20	44	DDR_B_D20		
DDR_B_D17	45	DQ17	DQ21	46	DDR_B_D21		
	47	VSS	VSS	48			
DDR_B_DQS#2	49	DQS2#	NC	50	PM_EXTTS#1	8	
DDR_B_DQS2	51	DQS2	DM2	52	DDR_B_DM2		
	53	VSS	VSS	54			
DDR_B_D18	55	DQ18	DQ22	56	DDR_B_D22		
DDR_B_D19	57	DQ19	DQ23	58	DDR_B_D23		
	59	VSS	VSS	60			
DDR_B_D24	61	DQ24	DQ28	62	DDR_B_D28		
DDR_B_D25	63	DQ25	DQ29	64	DDR_B_D29		
	65	VSS	VSS	66			
DDR_B_DM3	67	DM3	DQS3#	68	DDR_B_DQS#3		
	69	NC	DQS3	70	DDR_B_DQS3		
	71	VSS	VSS	72			
DDR_B_D26	73	DQ26	DQ30	74	DDR_B_D30		
DDR_B_D27	75	DQ27	DQ31	76	DDR_B_D31		
	77	VSS	VSS	78			
DDR_CKE2_DIMMB	79	CKE0	NC/CKE1	80	DDR_CKE3_DIMMB	DDR_CKE3_DIMMB	8
	81	VDD	VDD	82			
	83	NC	NC/A15	84			
DDR_B_BS2	85	BA2	NC/A14	86	DDR_B_MA14		
	87	VDD	VDD	88			
DDR_B_MA12	89	A12	A11	90	DDR_B_MA11		
DDR_B_MA9	91	A9	A7	92	DDR_B_MA7		
DDR_B_MA8	93	A8	A6	94	DDR_B_MA6		
	95	VDD	VDD	96			
DDR_B_MA5	97	A5	A4	98	DDR_B_MA4		
DDR_B_MA3	99	A3	A2	100	DDR_B_MA2		
DDR_B_MA1	101	A1	A0	102	DDR_B_MA0		
	103	VDD	VDD	104			
DDR_B_MA10	105	A10/AP	BA1	106	DDR_B_BS1	DDR_B_BS1	9
DDR_B_BS0	107	BA0	RAS#	108	DDR_B_RAS#	DDR_B_RAS#	9
DDR_B_WE#	109	WE#	S0#	110	DDR_CS2_DIMMB#	DDR_CS2_DIMMB#	8
	111	VDD	VDD	112			
DDR_B_CAS#	113	CAS#	ODT0	114	M_ODT2	M_ODT2	8
DDR_CS3_DIMMB#	115	NC/S1#	NC/A13	116	DDR_B_MA13		
	117	VDD	VDD	118			
M_ODT3	119	NC/ODT1	NC	120			
	121	VSS	VSS	122			
DDR_B_D32	123	DQ32	DQ36	124	DDR_B_D36		
DDR_B_D33	125	DQ33	DQ37	126	DDR_B_D37		
	127	VSS	VSS	128			
DDR_B_DQS#4	129	DQS4#	DM4	130	DDR_B_DM4		
DDR_B_DQS4	131	DQS4	VSS	132			
	133	VSS	DQ38	134	DDR_B_D38		
DDR_B_D34	135	DQ34	DQ39	136	DDR_B_D39		
DDR_B_D35	137	DQ35	VSS	138			
	139	VSS	DQ44	140	DDR_B_D44		
DDR_B_D40	141	DQ40	DQ45	142	DDR_B_D45		
DDR_B_D41	143	DQ41	VSS	144			
	145	VSS	DQS5#	146	DDR_B_DQS#5		
DDR_B_DM5	147	DM5	DQS5	148	DDR_B_DQS5		
	149	VSS	VSS	150			
DDR_B_D42	151	DQ42	DQ46	152	DDR_B_D46		
DDR_B_D43	153	DQ43	DQ47	154	DDR_B_D47		
	155	VSS	VSS	156			
DDR_B_D48	157	DQ48	DQ52	158	DDR_B_D52		
DDR_B_D49	159	DQ49	DQ53	160	DDR_B_D53		
	161	VSS	VSS	162			
	163	NC,TEST	CK1	164	M_CLK_DDR3	8	
	165	VSS	CK1#	166	M_CLK_DDR#3	8	
DDR_B_DQS#6	167	DQS6#	VSS	168			
DDR_B_DQS6	169	DQS6	DM6	170	DDR_B_DM6		
	171	VSS	VSS	172			
DDR_B_D50	173	DQ50	DQ54	174	DDR_B_D54		
DDR_B_D51	175	DQ51	DQ55	176	DDR_B_D55		
	177	VSS	VSS	178			
DDR_B_D56	179	DQ56	DQ60	180	DDR_B_D60		
DDR_B_D57	181	DQ57	DQ61	182	DDR_B_D61		
	183	VSS	VSS	184			
DDR_B_DM7	185	DM7	DQS7#	186	DDR_B_DQS#7		
	187	VSS	DQS7	188	DDR_B_DQS7		
DDR_B_D58	189	DQ58	VSS	190			
DDR_B_D59	191	DQ59	DQ62	192	DDR_B_D62		
	193	VSS	DQ63	194	DDR_B_D63		
	195	SDA	VSS	196			
	197	SCL	SA0	198			
	199	VDDSPD	SA1	200			

14,16,19,21 ICH_SMBDATA
14,16,19,21 ICH_SMBCLK
+3VS
C210 2.2U_0603_6.3V6K
C211 0.1U_0402_16V4Z
CONN@ FOX_AS0A426-N4SN-7F
R118 10K_0402_5%
+3VS
R119 10K_0402_5%

SO-DIMM B
4mm Height standard
Bottom side

Security Classification	Compal Secret Data		
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Title: **DDRII-SODIMM SLOT**

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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	FSB MHz	SRC MHz	PCI MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3

Mount C157 & C166 tp solve WWAN noise issue. 1/23

Place close to U5

SA000020H10 for Compal
SA00001YJ20 for HP

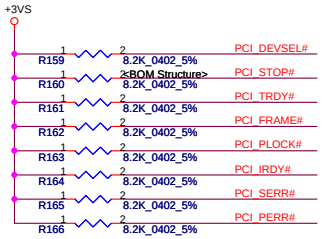
Security Classification	Compal Secret Data		
Issued Date	2006/02/20	Deciphered Date	2009/02/20

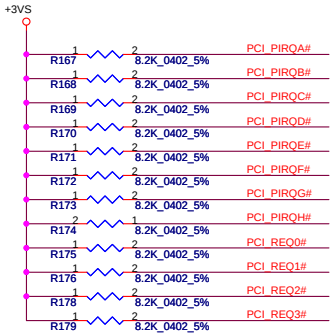
Compal Electronics, Inc.

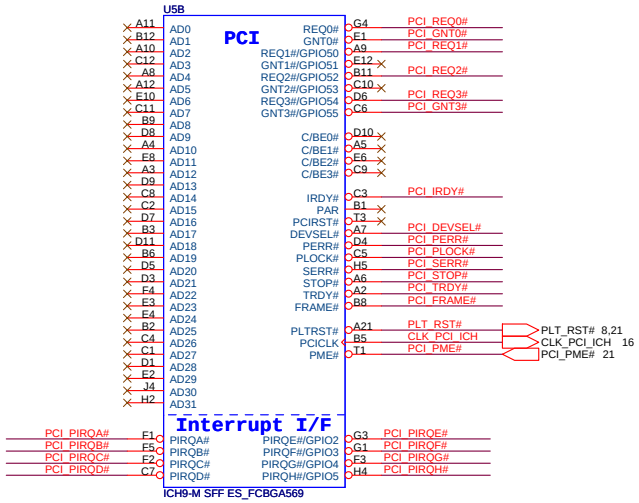
Title: CLOCK GENERATOR

Size: | Document Number: LS-5341P | Rev: 1.0

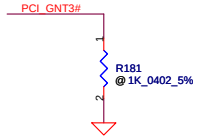
Date: Tuesday, June 23, 2009 | Sheet 16 of 30



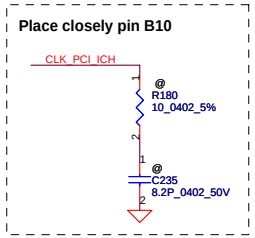


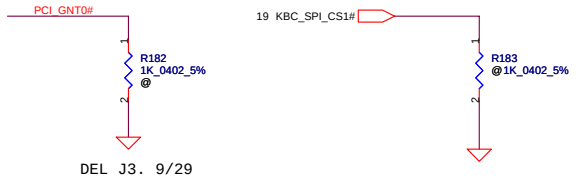


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

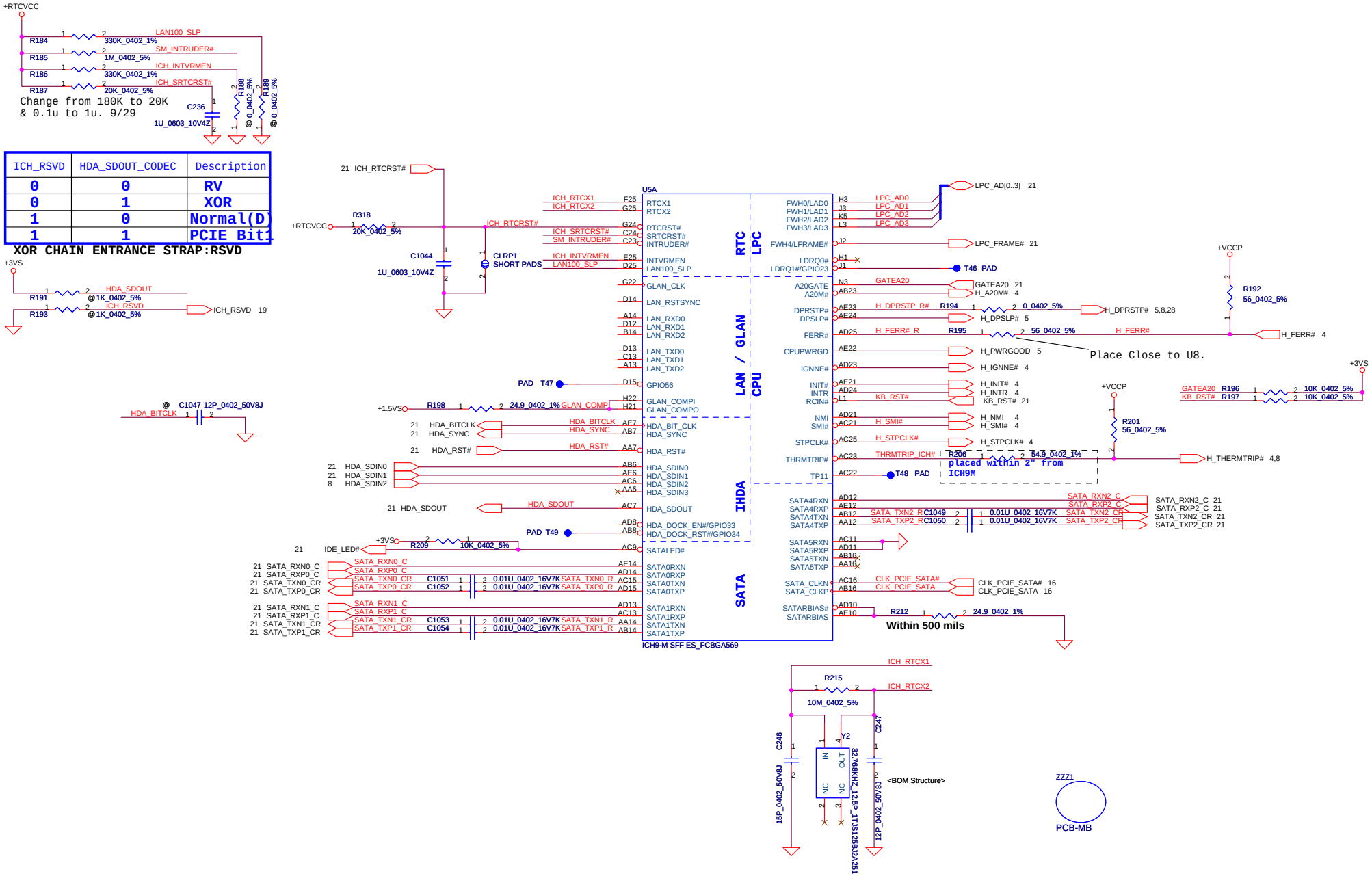




DEL J3. 9/29

Security Classification	Compal Secret Data		
Issued Date	2006/02/20	Deciphered Date	2009/02/20

Compal Electronics, Inc.			
Title	ICH9(1/4)-PCI/INT		
Size	Document Number		Rev
	LS-5341P		1.0
Date: Tuesday, June 23, 2009	Sheet 17 of 30		



Security Classification	Compal Secret Data		
Issued Date	2006/02/20	Deciphered Date	2009/02/20

Compal Electronics, Inc.

Title: **ICH9(2/4)_LAN,HD,IDE,LPC**

Size	Document Number	Rev
Custom	LS-5341P	1.0

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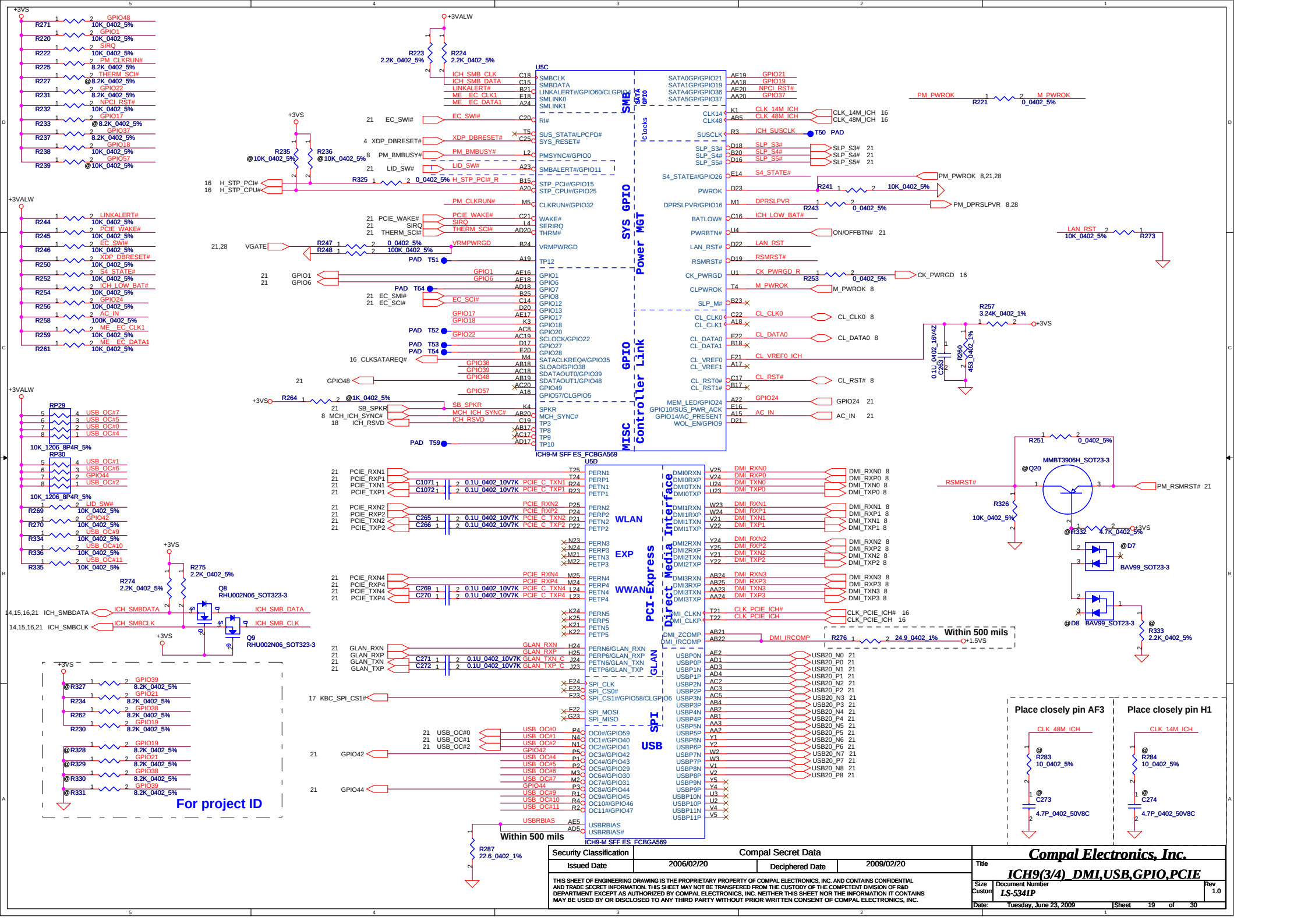
U5C
ICH9-M SFF ES_FCBGA569
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
U5D
PCI-Express
Direct Media Interface
WLAN
EXP
WWAN
GLAN
SPI
USB
ICH9-M SFF ES_FCBGA569
Within 500 mils
Within 500 mils
Place closely pin AF3
Place closely pin H1
For project ID
Compal Secret Data
Compal Electronics, Inc.
ICH9(3/4)_DMI,USB,GPIO,PCIE
LS-5341P
Tuesday, June 23, 2009
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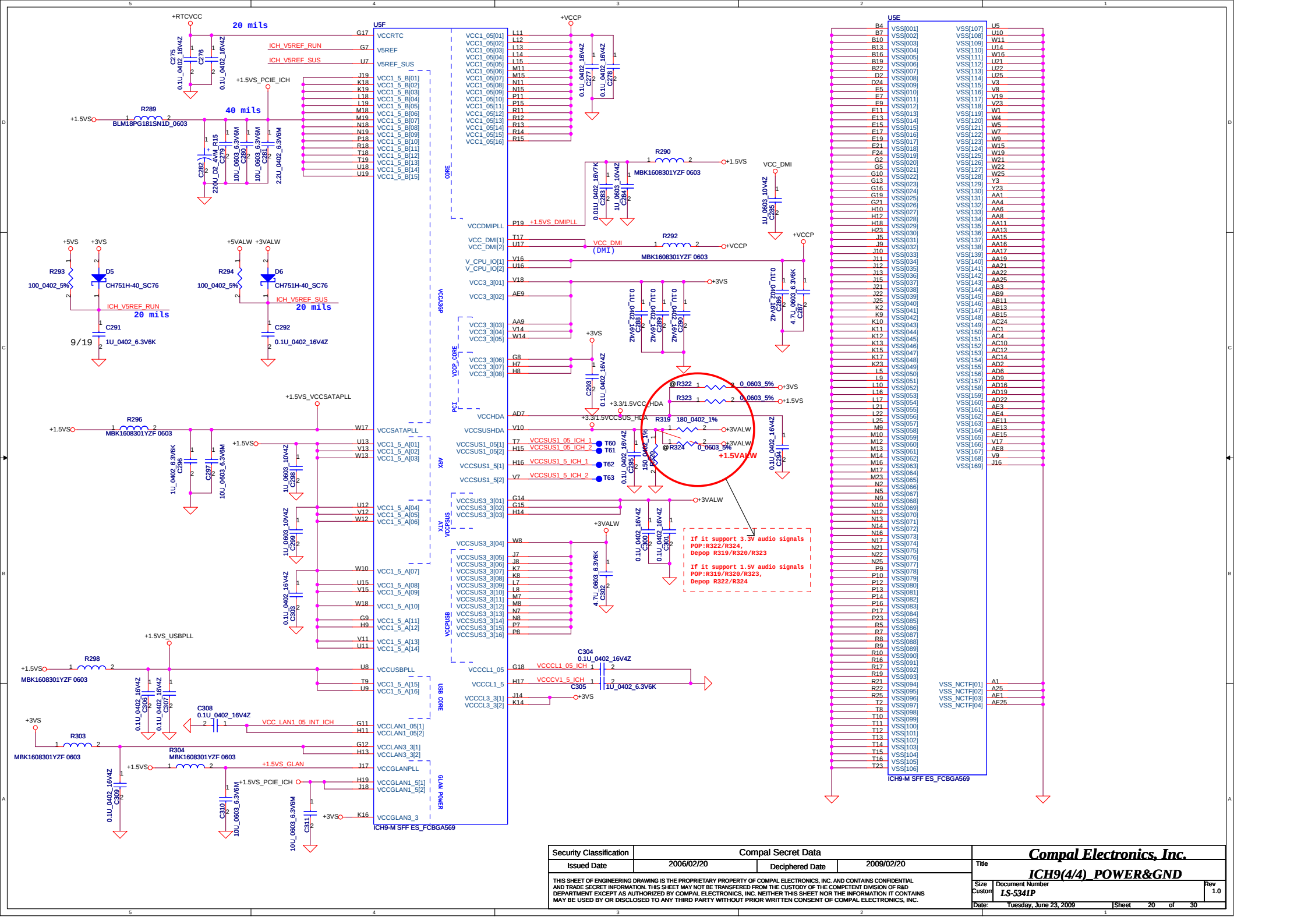
U5F
ICH9-M SFF ES_FCBGA569
U5E
ICH9-M SFF ES_FCBGA569
+RTCVCC
20 mils
40 mils
+1.5VS_PCIE_ICH
+1.5VS
+VCCP
VCC_DMI
+5VS
+3VS
+5VALW
+3VALW
+1.5VALW
+3.3/1.5VCC_HDA
+3.3/1.5VCCSUS_HDA
+1.5VS_VCCSATAPLL
+1.5VS_USBPLL
+1.5VS_GLAN
ICH_V5REF_RUN
ICH_V5REF_SUS
VCC_LAN1_05_INT_ICH
VCCCL1_05_ICH
VCCCV1_5_ICH
R289
BLM18PG181SN1D_0603
R290
MBK1608301YZF 0603
R292
R293
R294
100_0402_5%
D5
D6
CH751H-40_SC76
R296
R298
R303
R304
R319
180_0402_1%
R322
R323
0_0603_5%
@R322
@R324
C291
C292
9/19
1U_0402_6.3V6K
If it support 3.3V audio signals
POP:R322/R324,
Depop R319/R320/R323
If it support 1.5V audio signals
POP:R319/R320/R323,
Depop R322/R324
Security Classification
Compal Secret Data
Issued Date
2006/02/20
Deciphered Date
2009/02/20
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Compal Electronics, Inc.
Title
ICH9(4/4)_POWER&GND
Size
Custom
Document Number
LS-5341P
Rev
1.0
Date:
Tuesday, June 23, 2009
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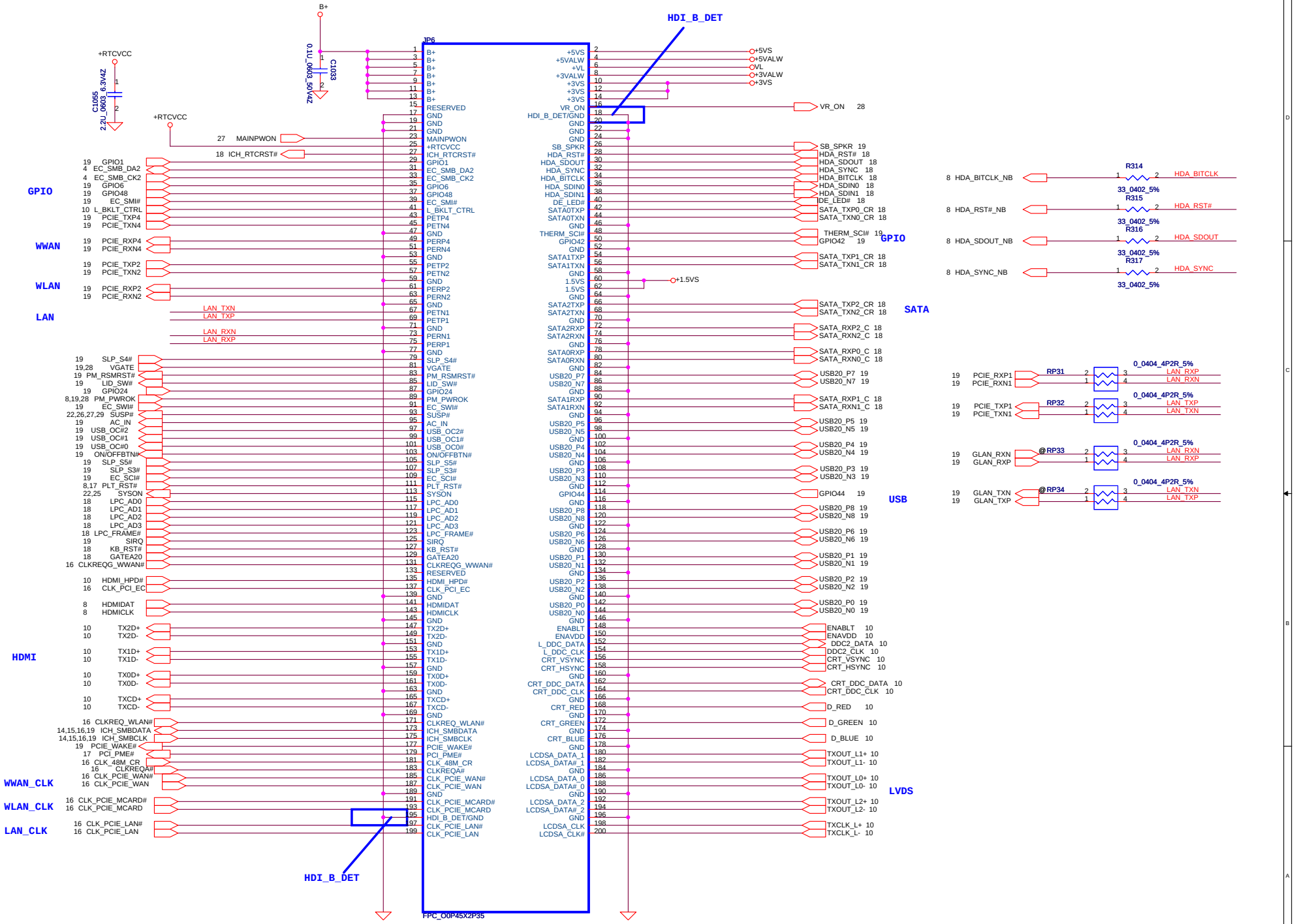
20
of
30



Security Classification	Compal Secret Data		
Issued Date	2006/02/20	Deciphered Date	2009/02/20

Compal Electronics, Inc.

Title: **LCD CONN & Q-Switch & GPIO Ext.**

Size	Document Number	Rev
	LS-5341P	1.0

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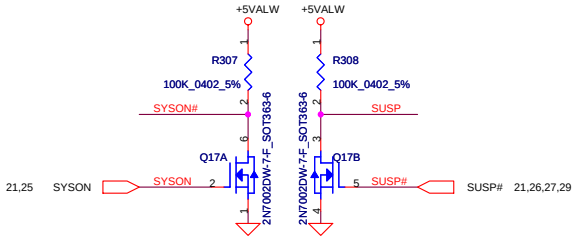

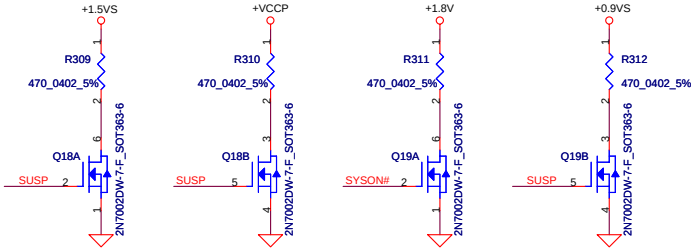

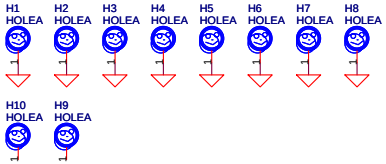

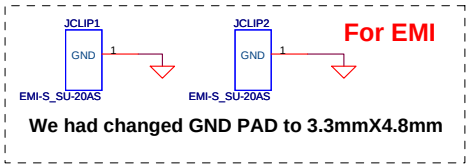

Security Classification	Compal Secret Data		
Issued Date	2006/02/20	Deciphered Date	2009/02/20

Compal Electronics, Inc.

Title: **LEDS & LID**

Size	Document Number	Rev
Custom	LS-5341P	1.0

Date: Tuesday, June 23, 2009 | Sheet 22 of 30

Version change list (P.I.R. List)

EE section

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve support to HDMI audio	11	Add R321 and C1045	2009/03/13	Rev02
2	Follow Intel DG CAP size	7	Change C8~C23 from 0805 to 0603 C59~C70 from 0603 to 0402	2009/03/13	Rev02
3	Reserve EMI solution	4	Add C1046	2009/03/19	Rev02
4	Reserve RF solution	18	Add C1047,C1048	2009/03/19	Rev02
5	Modify layout routing on DDR signals to meet Intel DG	14,15	1. JP3 modify to SP07F00176L (5.2mm reverse type) 2. JP4 modify to SP07000BR00 (4mm standard type)	2009/03/20	Rev02
6	Reserve support to 3.3V/1.5V audio signals	20	Add R322,R323 and R324	2009/03/23	Rev02
7	Follow Intel DG on SATA signals routing	18	Delete R210,R211,R213,R214,R216,R217,Add C1049~C1054	2009/03/23	Rev02
8	Reserve one CAP for RTC power	21	Add C1055	2009/03/25	Rev02
9	Reserve CAP for EMI	4,8	Add C1056~C1064	2009/03/25	Rev02
10	Reserve CAP for EMI	14,15	Add C1065~C1068	2009/03/26	Rev02
11	Follow Intel check list(REV2.1)	10	Change R67 to 2.4K ohm	2009/03/26	Rev02
12	Fix power derating for +VCC_PEG	11	Change R99 package from 0805 to 1206	2009/03/27	Rev02
13	Support Intel DPST function except GS40	10	Add L_BKLT_CTRL signal	2009/03/27	Rev02
14	Follow Intel recommend	8	Change R53 to 499 ohm	2009/04/23	Rev03
15	Remove CL_REF1 circuit w/o iAMT	19	Delete R265,R266 and C264	2009/04/23	Rev03
16	Reserve 0 ohm on PCI_STP# signal for seligo CLKGEN issue	19	Add R325 and delete R240	2009/04/23	Rev03
17	Add Intel resume reset circuit	19	Add Q20,R332,R333,D7 and D8 and change R251 to 0 ohm	2009/04/23	Rev03
18	Reserve Project ID	19	Add R327~R330	2009/04/23	Rev03
19	Modify EC_SCI# on GPIO for SW recommend	19	EC_SCI# change from GPIO7 to 12 and delete R263	2009/04/23	Rev03
20	Follow vendor recommend	16	Change R149 and R177 to 15ohm	2009/04/23	Rev03
21	Follow RF team recommend	16	Add C1069 and C1070	2009/04/23	Rev03
22	For Battery life on PCIe port	19	Reserve LOM PCIe signals between Port6 and Port1and add C1071,C1072,R337~R344	2009/04/27	Rev03
23	For Intel PCICLK routing buffer	16	Modify CLK_PCI_EC from PCICLK3 to PCICLK1	2009/04/27	Rev03
24	Fix USB initial when system boot	19	Add R334~R336	2009/05/05	Rev03
25	Fix crystal EA report	16,18	Change Y1 to SJ100003B00,C233,C234 to 22P and C246 to 15P	2009/05/05	Rev03
26	Reserve EMI solution for XDP	4	Add D9~D12 and delete C1058~C1064	2009/05/05	Rev03
27	For layout routing	21	R337~R344 change to RP31~RP34	2009/05/12	Rev03
28	For Intel DG	4,17,19	R10 change to depop,R172-->8.2K,R250-->10K,R230-->8.2K	2009/05/12	Rev03
29	For EMI recommend	16	R177 change to depop	2009/05/12	Rev03
30	For EMI recommend	14,15,22	Add JCLIP1 and JCLIP2 ,Pop C1065~C1068	2009/06/16	Rev1.0
31	For delete TP location to fix Intel recommend VCCP power rail	8	Del T12~T15,T16~T18 and T24,T26~T27	2009/06/16	Rev1.0
32	For Argos project cost down	14	Depop C158~C159,C161~C184	2009/06/16	Rev1.0

Security Classification	Compal Secret Data		
Issued Date	2006/02/20	Deciphered Date	2009/02/20

Compal Electronics, Inc.

Title: HW Changed-List History-1

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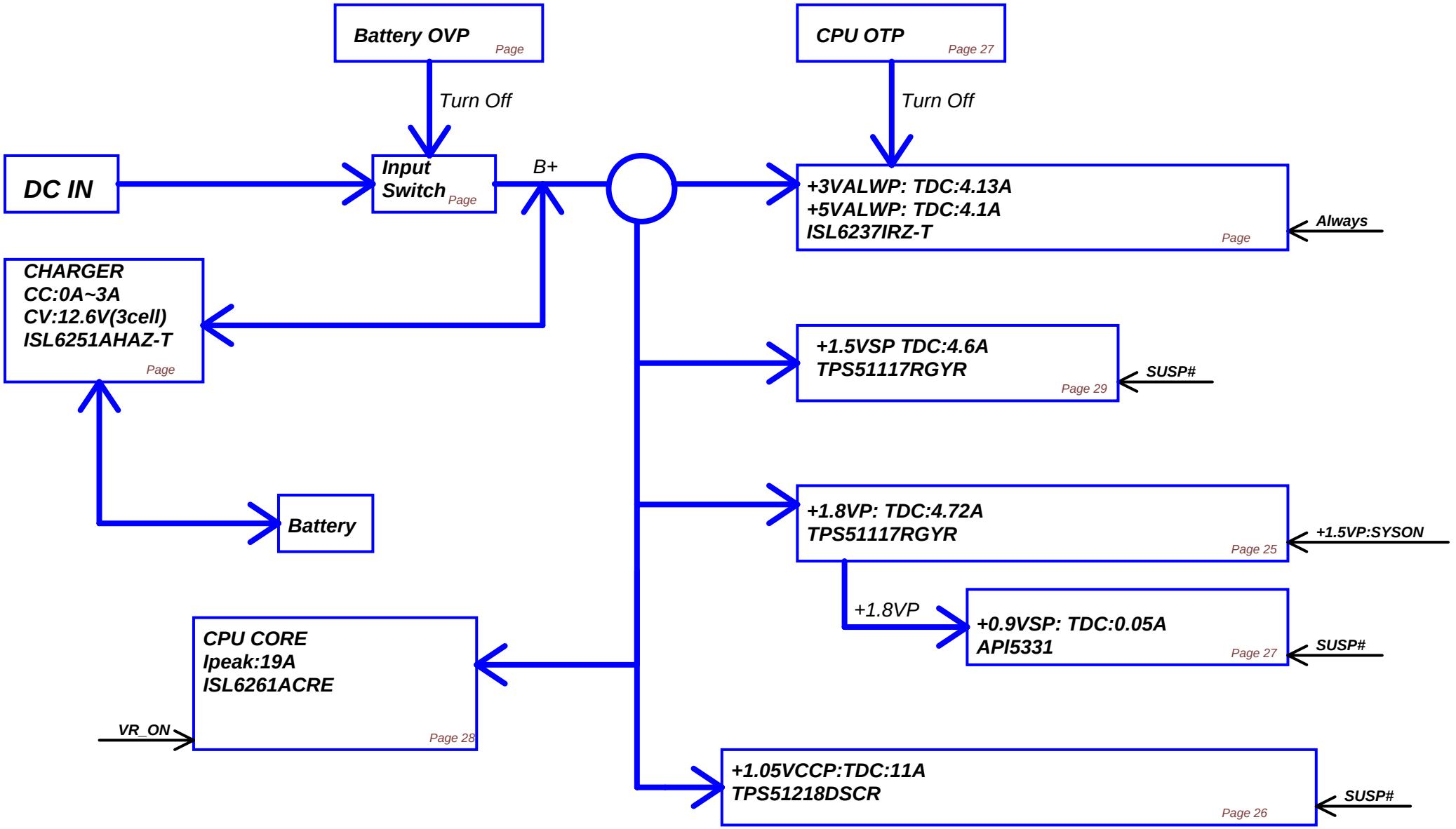
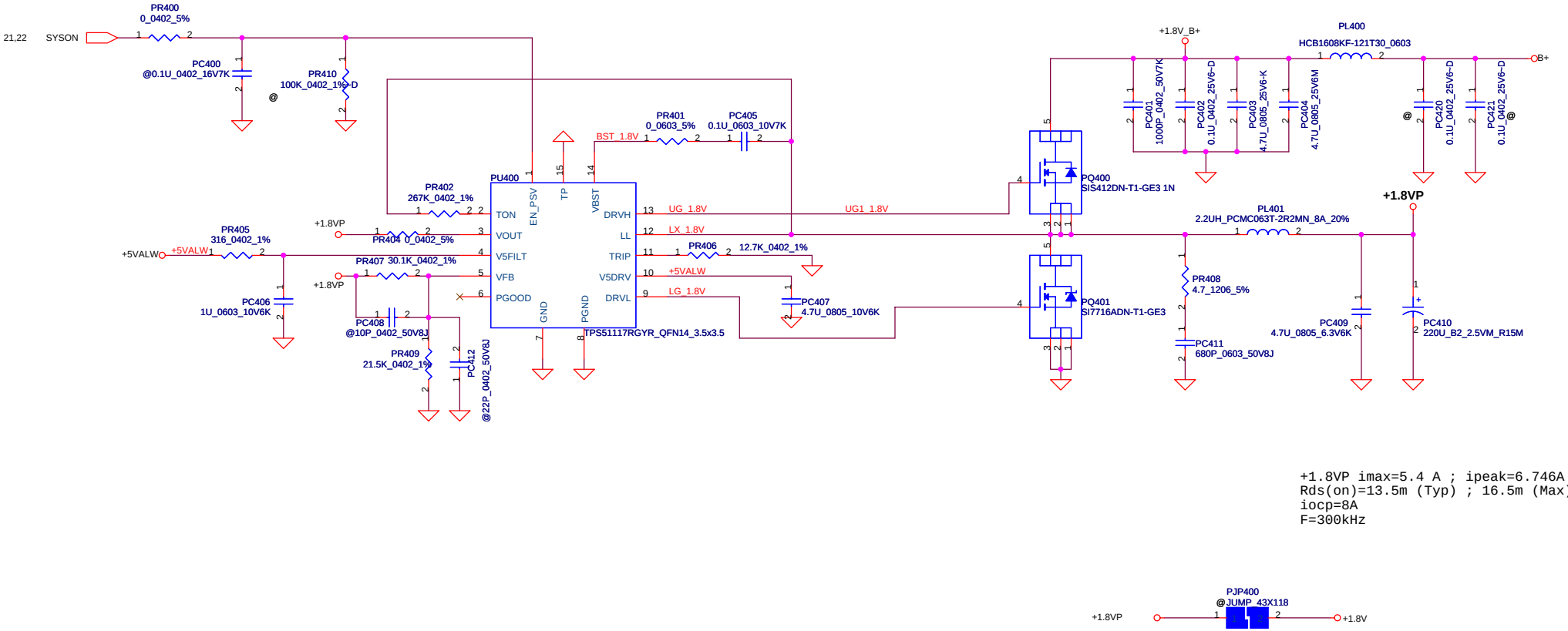
Argos Power block



Title	POWER BLOCK DIAGRAM	
Size	Document Number	Rev
Date: Tuesday, June 23, 2009	Sheet 24 of 30	



+1.8VP imax=5.4 A ; ipeak=6.746A
Rds(on)=13.5m (Typ) ; 16.5m (Max)
iocp=8A
F=300kHz

PJP400
@JUMP_43X118
+1.8VP
+1.8V

Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: **1.8VP**

Size	Document Number	Rev
	LS-5341P	1.0

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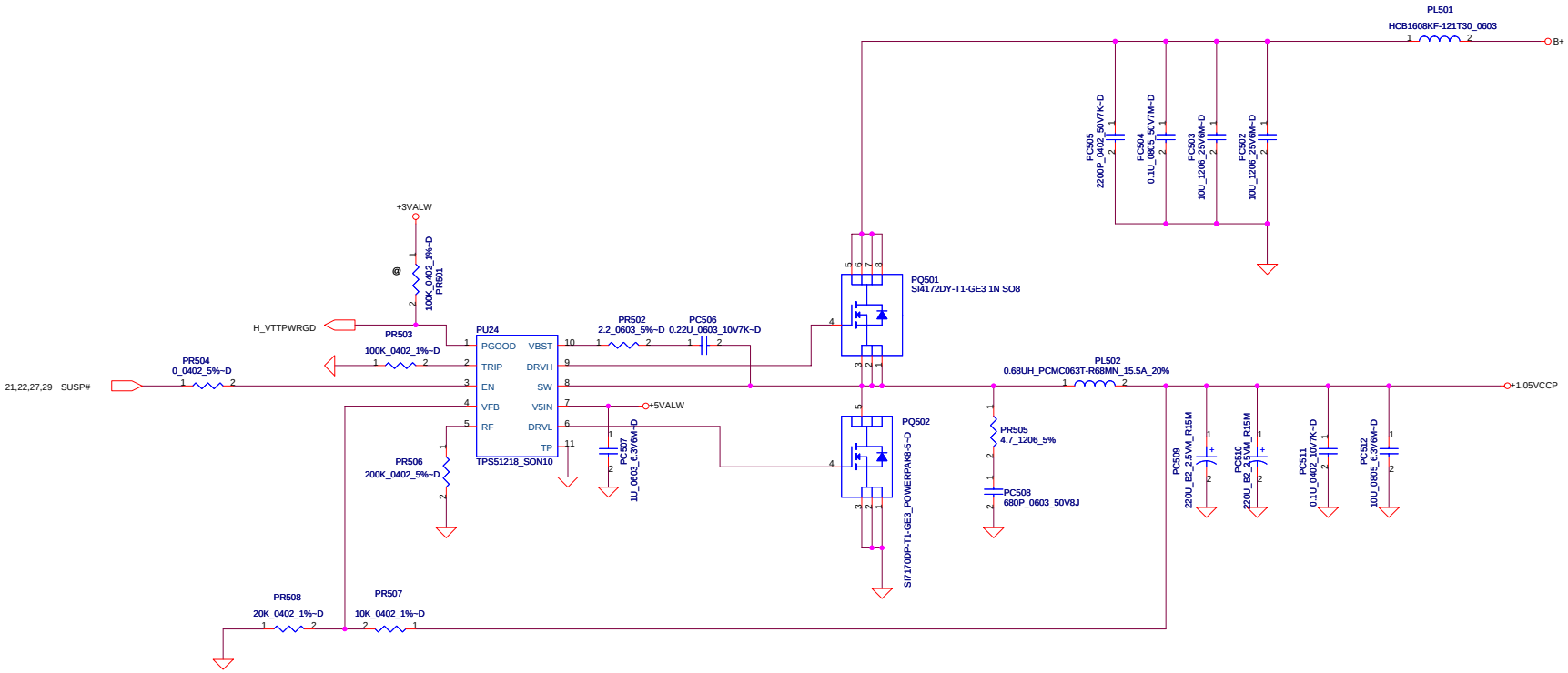
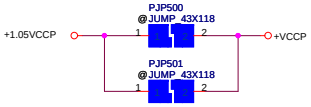


+1.05VCCP imax=12.32A ipeak=17.6A
Rds(on)=5.5m (Typ) ; 6.7m (Max)
iocp=A
F=350kHz



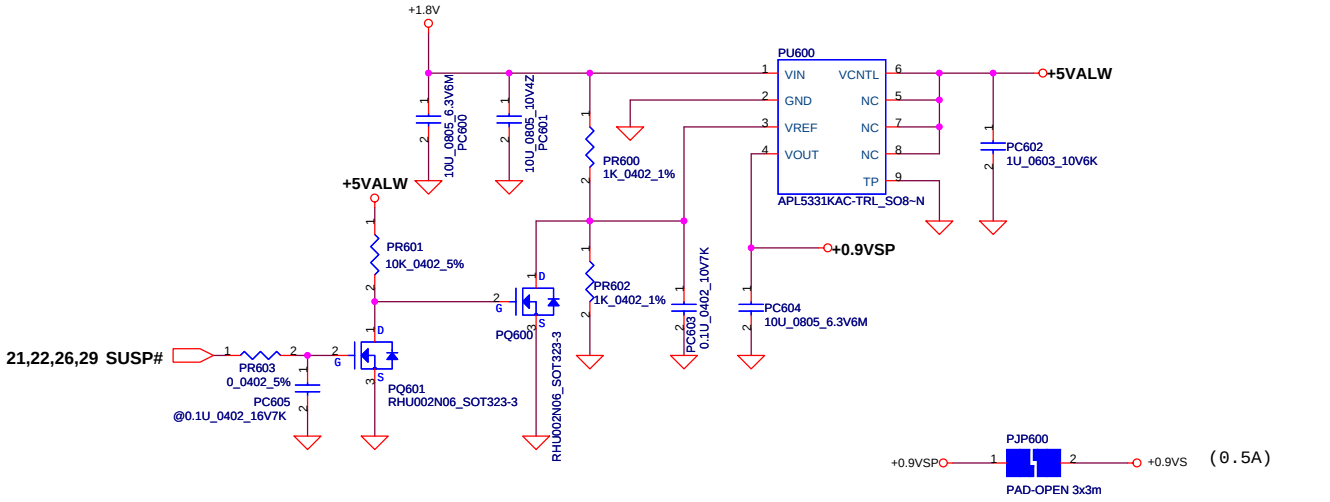
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

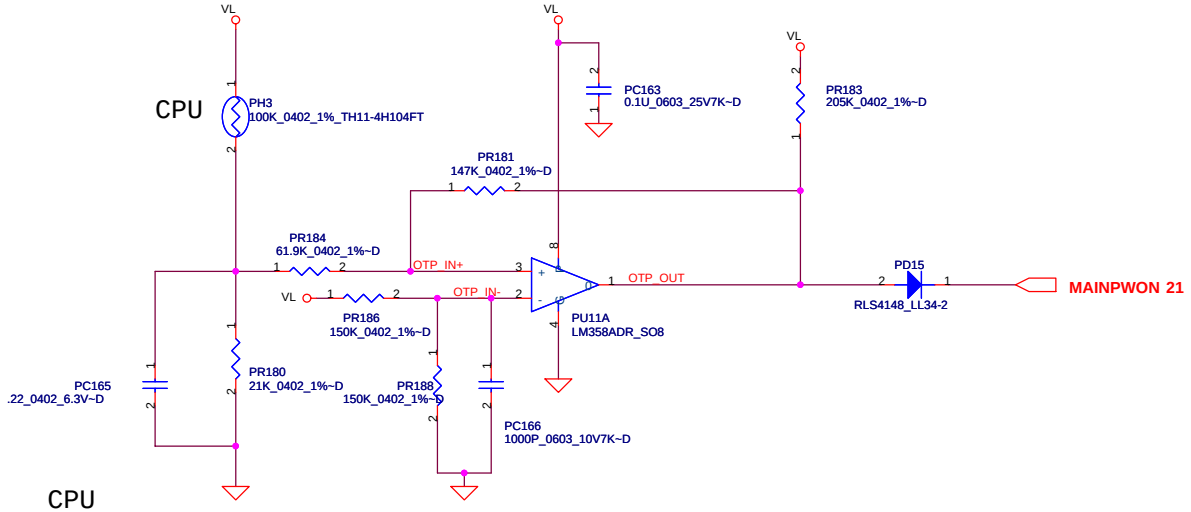
Compal Electronics, Inc.

Title: **1.05VCCP**

Size | Document Number: **LS-5341P** | Rev: 1.0

Date: Tuesday, June 23, 2009 | Sheet 26 of 30





PH3 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C

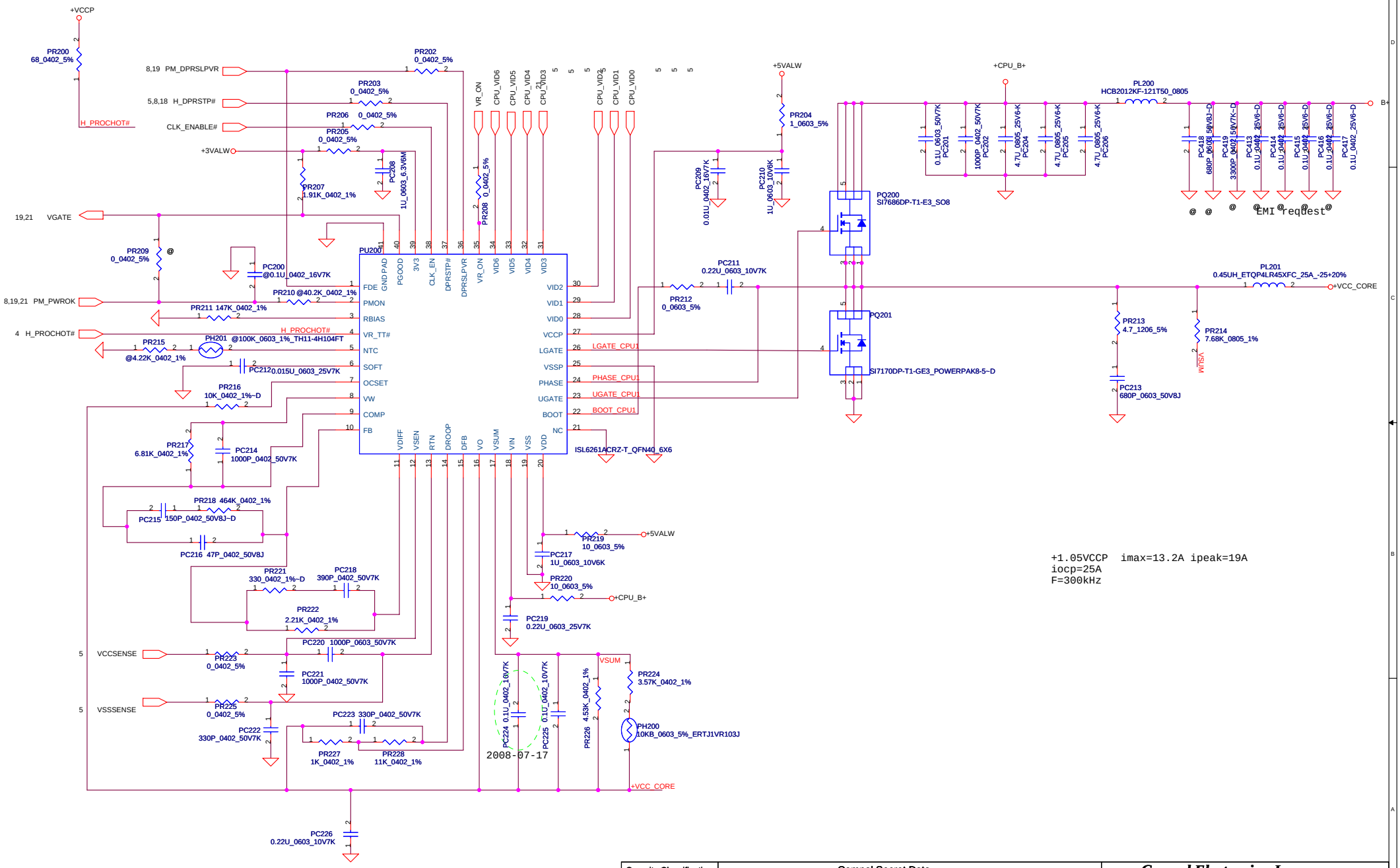
Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

Compal Electronics, Inc.

Title: **0.9VSP**

Size	Document Number	Rev
	LS-5341P	1.0

Date: Tuesday, June 23, 2009 | Sheet 27 of 30



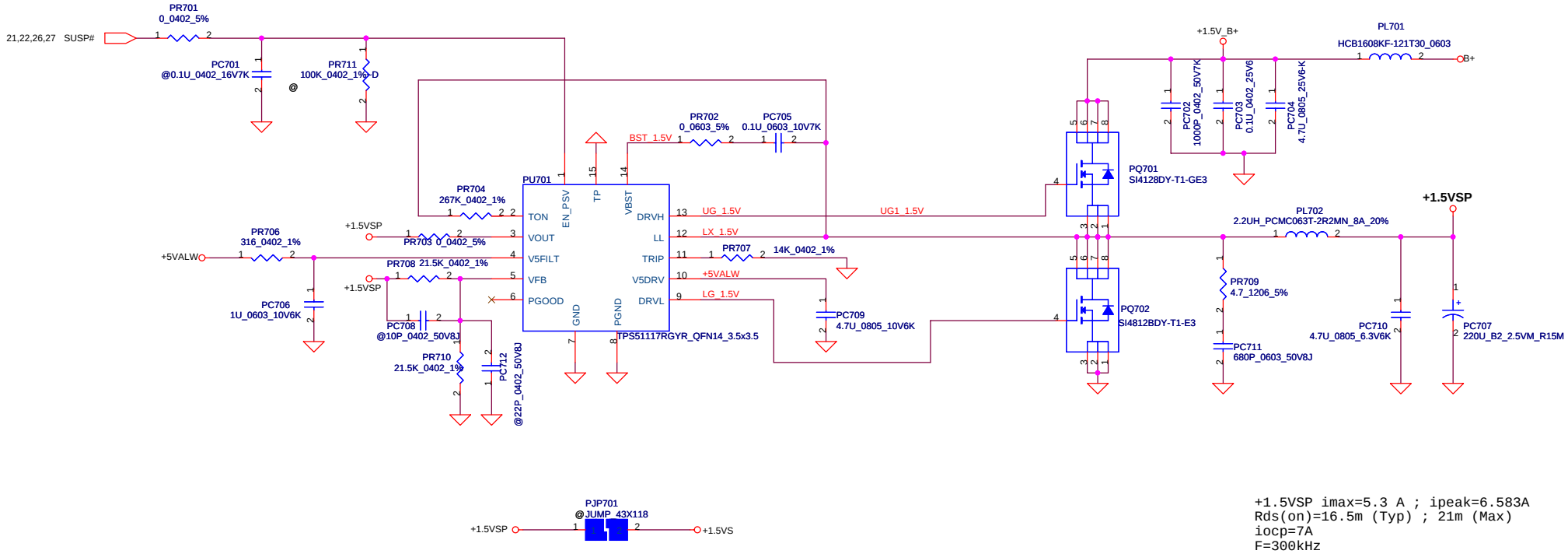
Security Classification	Compal Secret Data		
Issued Date	2005/06/23	Deciphered Date	2006/10/22

Compal Electronics, Inc.

Title: CPU_CORE

Size	Document Number	Rev
Custom	LS-5341P	1.0

Date: Tuesday, June 23, 2009 Sheet 28 of 30



+1.5VSP imax=5.3 A ; ipeak=6.583A
Rds(on)=16.5m (Typ) ; 21m (Max)
iocp=7A
F=300kHz

Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: **1.5VSP**

Size	Document Number	Rev
	LS-5341P	1.0

Date: Tuesday, June 23, 2009 | Sheet 29 of 30

Item	Reason for change	PG#	Modify List	Date	Phase
01	slove power on hard on DC mode	P27	change PC165 from 1000P to 0.22u PC166 from 1u to 1000P	06/22/09	X-build
02	slove power on hard on DC mode	P17	change PR68 from 100k to 0 ohm	06/22/09	X-build
03	Add AC-IN margin for Temp/Volt test	P15	change PR194 from 19.6k to 20.5k	06/22/09	X-build
04	Add AC-IN margin for Temp/Volt test	P15	change PU3 from BIT3021 to APL5156	06/22/09	X-build
05					
06					
07					
08					
09					
10					

Compal Electronics, Inc.

Title: GM VGA_CORE

Size: Custom | Document Number: LS-5341P | Rev:

Date: Tuesday, June 23, 2009 | Sheet 30 of 30