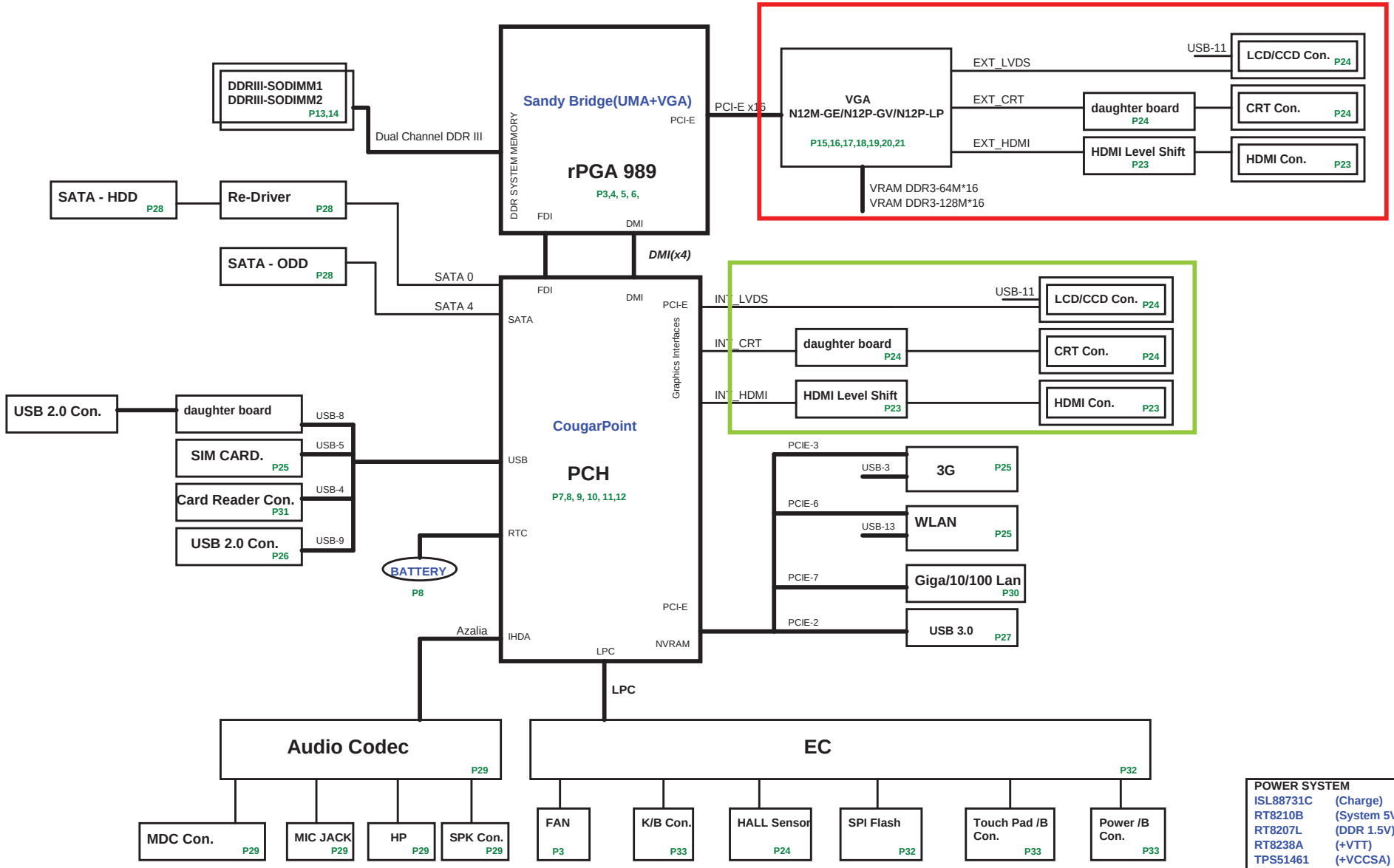
TE5 Block Diagram



POWER SYSTEM		
ISL88731C	(Charge)	P35
RT8210B	(System 5V/3V)	P36
RT8207L	(DDR 1.5V)	P37
RT8238A	(+VTT)	P38
TPS51461	(+VCCSA)	P39
ISL95835	(+VCC_CORE)	P40
G966A	(+1.8V)	P41
ISL95870A	(+GPU_CORE)	P42

Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Rev
	Block Diagram	1A

Date: Wednesday, January 05, 2011 Sheet 1 of 44

02

Table of Contents

PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-6	Processor
7-12	PCH
8	RTC
13-14	DDRIII SO-DIMM
15-21	VGA
23	HDMI comm part
24	LCD Panel
	CRT & CRT BUS SWITCH
	CCD
	HALL SENSOR&BACK LIGHT SWITCH
25	MINI Card (Wi-Fi & WIMAX)
	MINI Card 2nd
	MINI Card 3nd
26	USB 2.0
27	USB 3.0
28	SATA ODD
	Main SATA HDD & 2nd SATA HDD
29	Codec (CX20587)
30	Atheros LAN
31	3 IN 1 Card reader
32	EC NPCE791L
33	INT KeyBoard & K/B LED Power
	TP board
	Power SW
	HOLE
34	LED / EMI
35	Charger (ISL88731C)
36	System 5V/3V (RT8210B)
37	DDR1.5V(RT8207L)/1.05VSUS
38	+VTT/+1.05V (RT8238A)
39	+VCCAS(TPS51461)
40	+VCC_CORE(ISL95835HRTZ)
41	+1.8V (G966A)/Discharge
42	+GPU_CORE(ISL95870AHRUZ)

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

GND PLANE	PAGE
8769AGND	32
Audio_GND	29
Shield_GND	29
GND	ALL
ISL95870A_AGND	29

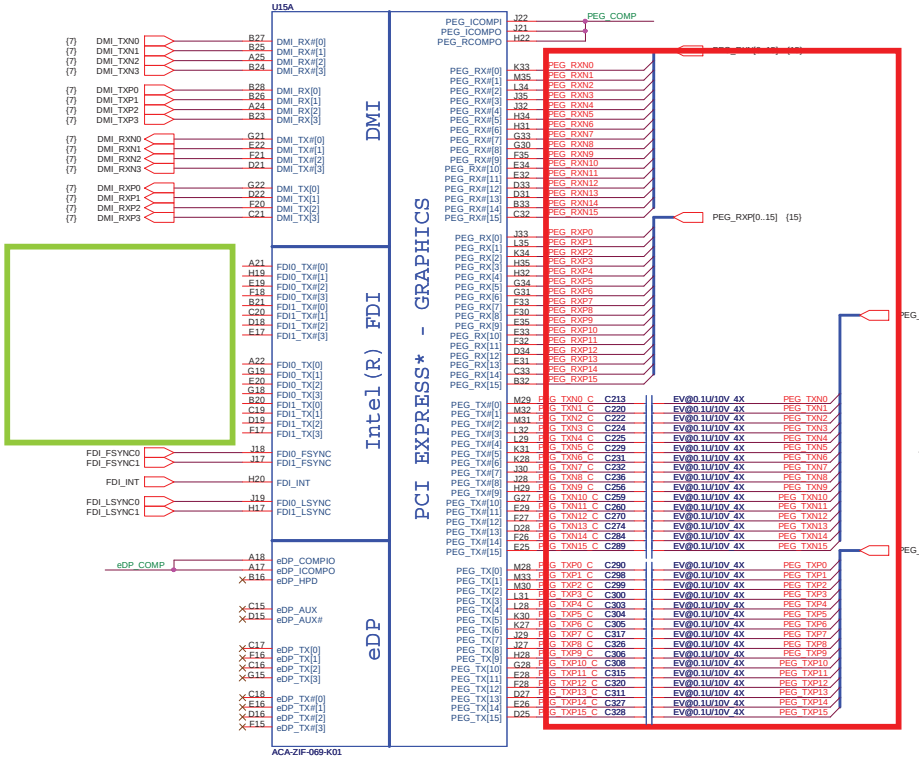
Quanta Computer Inc.

PROJECT : TE5

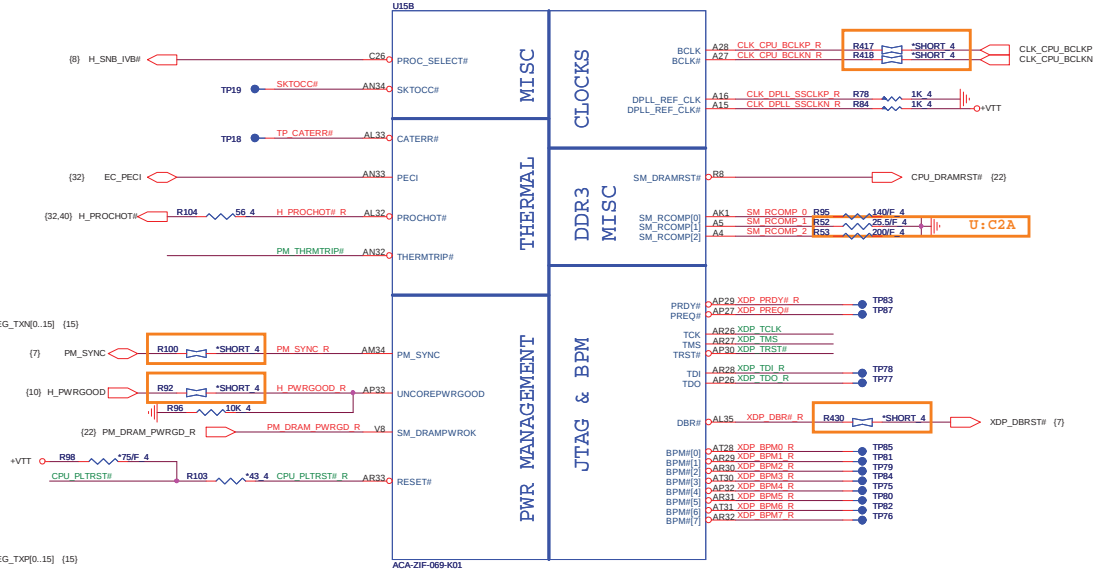
Size	Document Number	Rev
	POWER STAGE AND BOI-FUNCTION	1A

Date: Wednesday, January 05, 2011 Sheet 2 of 44

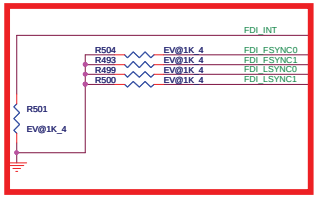
Sandy Bridge Processor (DMI,PEG,FDI) <CPU,VGA>



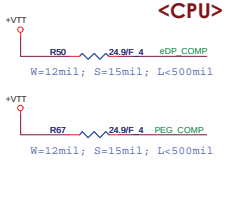
Sandy Bridge Processor (CLK,MISC,JTAG)<CPU>



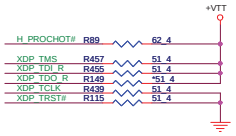
FDI Disabling (Discrete Only) <VGA>



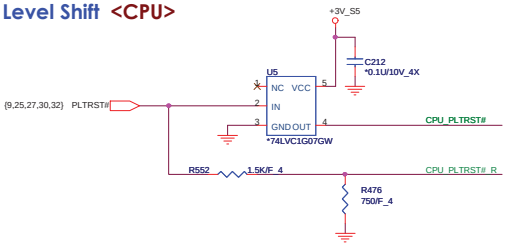
DP & PEG Compensation <CPU>



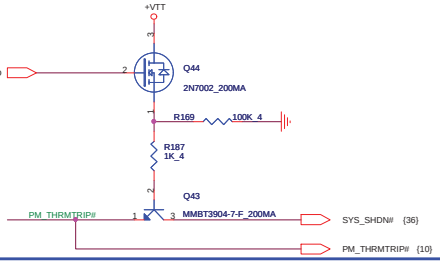
Processor pull-up <CPU>



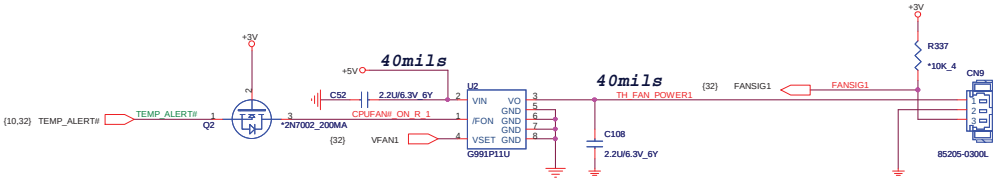
Level Shift <CPU>



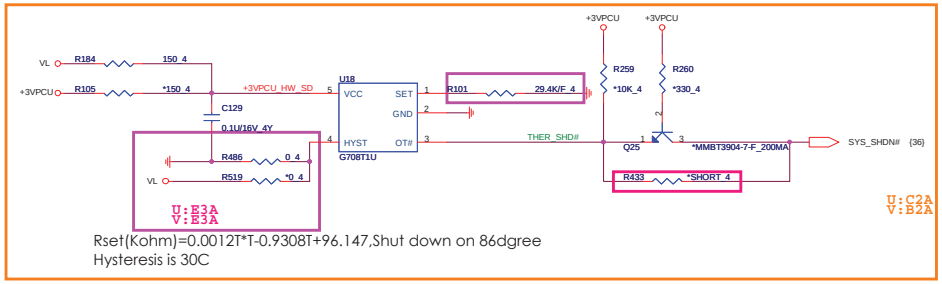
Thermal Trip <CPU>



FAN Control-->For one FAN solution <THC/THV>

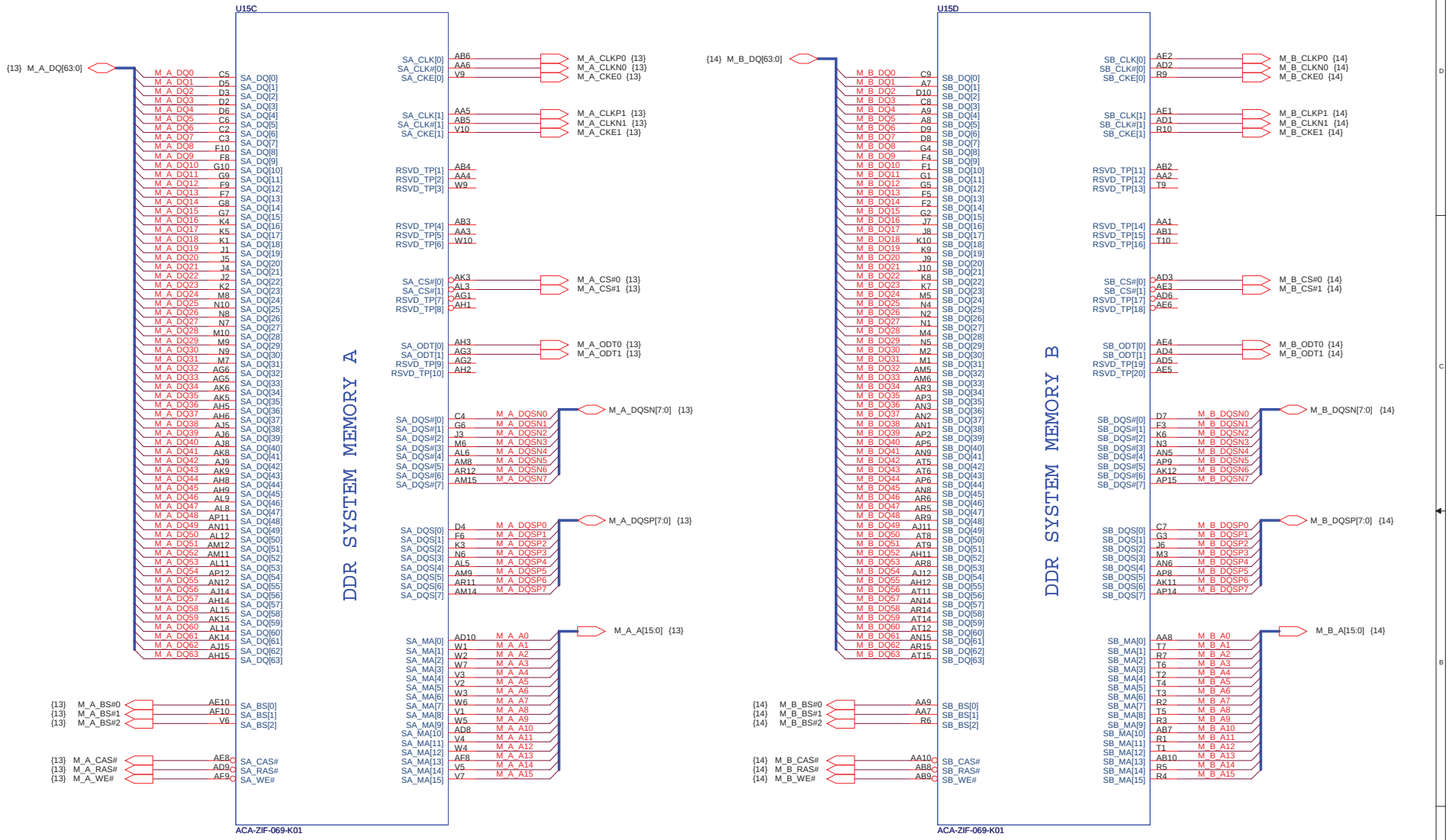


CPU Thermal sensor / MB Local TEMP <THC>



Quanta Computer Inc.	PROJECT : TE5
Size	Document Number: Sandy Bridge 1/4 — Rev 1A
Date: Wednesday, January 05, 2011	Sheet 3 of 44

Sandy Bridge Processor (DDR3)



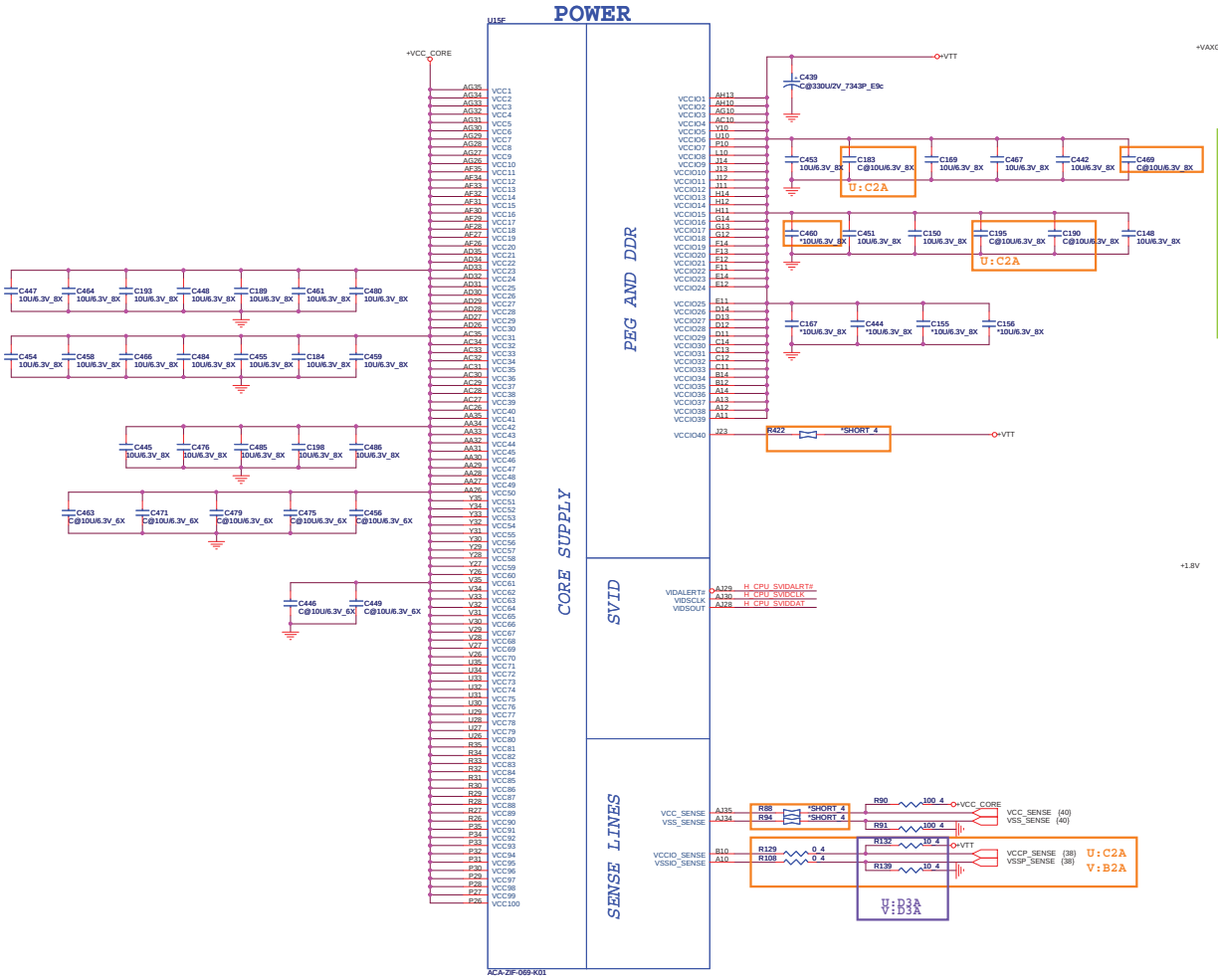
Quanta Computer Inc.

PROJECT : TE5

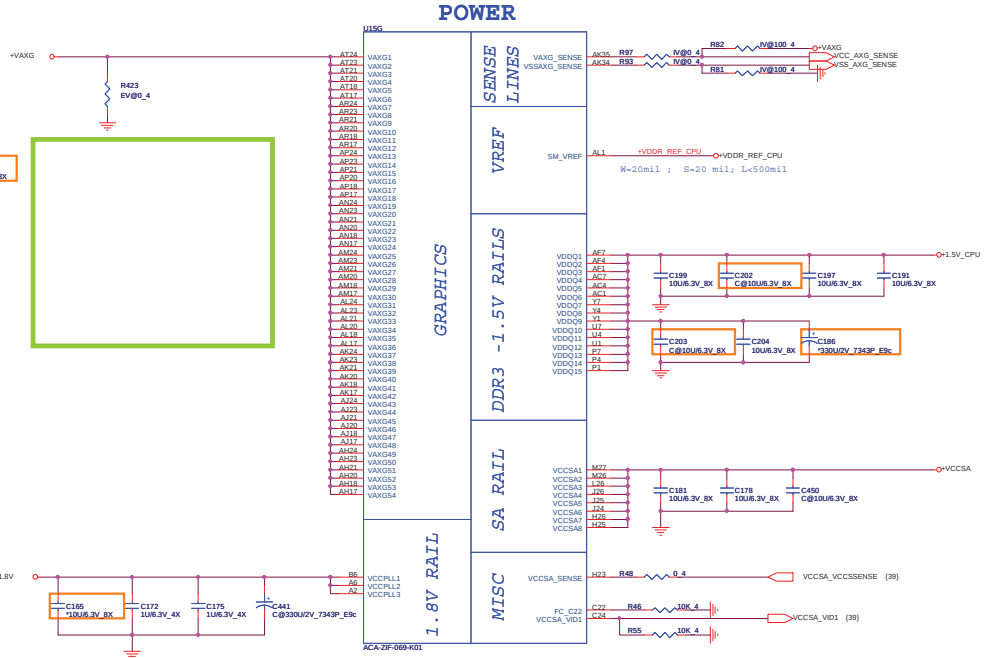
Size	Document Number	Rev
	Sandy Bridge 2/4	1A

Date: Wednesday, January 05, 2011 Sheet 4 of 44

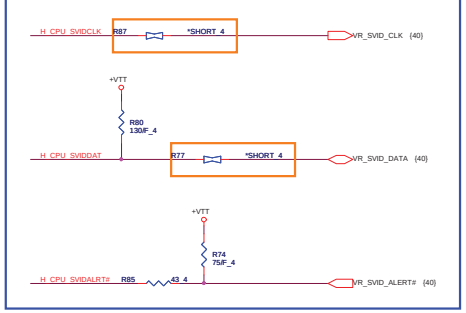
Sandy Bridge Processor (POWER)<CPU>



Sandy Bridge Processor (GRAPHIC POWER)<CPU,UGA>



Layout note: need routing together and ALERT need between CLK and DATA <CPU>



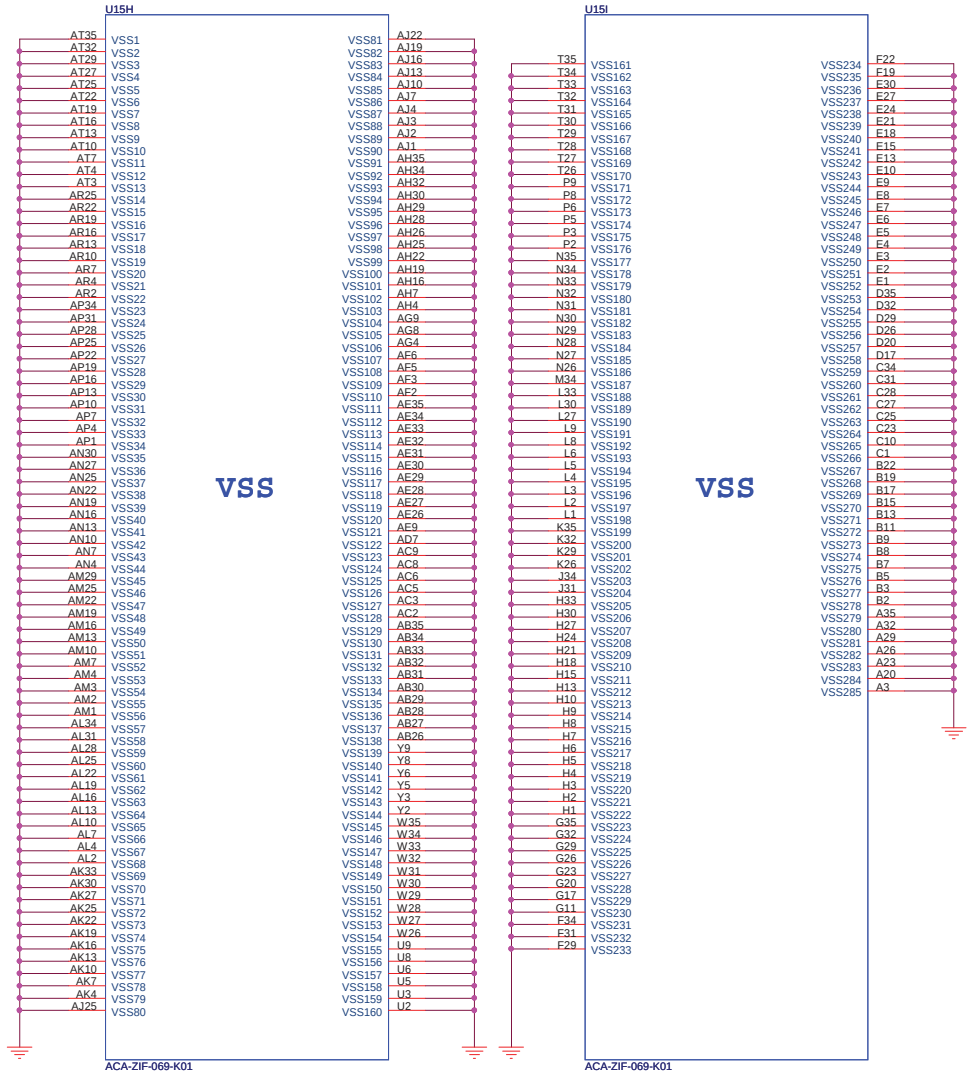
Quanta Computer Inc.

PROJECT : TE5

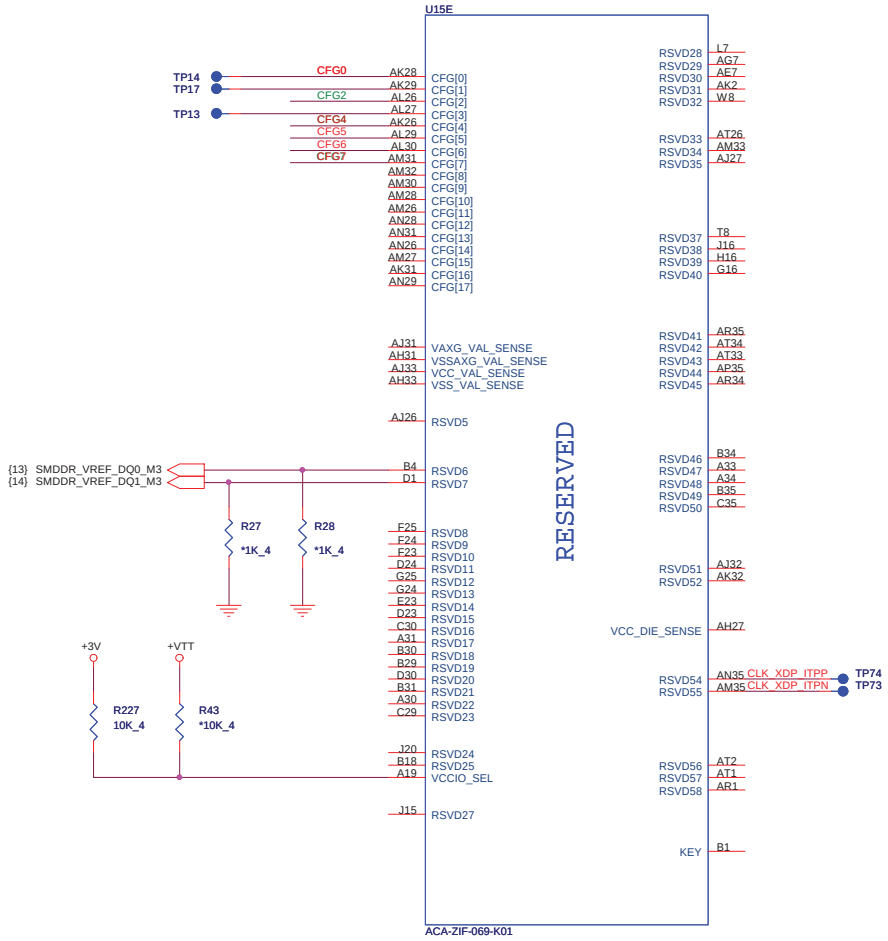
Size	Document Number	Rev
	Sandy Bridge 3/4	1A

Date: Wednesday, January 05, 2011 Sheet 5 of 44

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)<CPU>



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

<CPU>

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

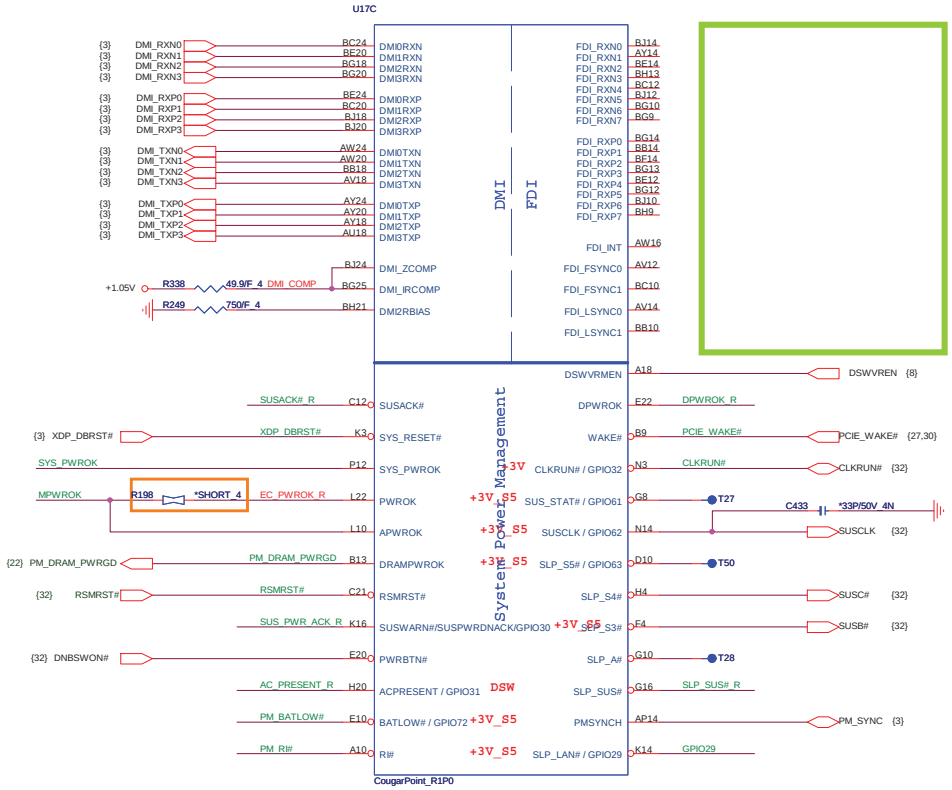
Quanta Computer Inc.

PROJECT : TE5

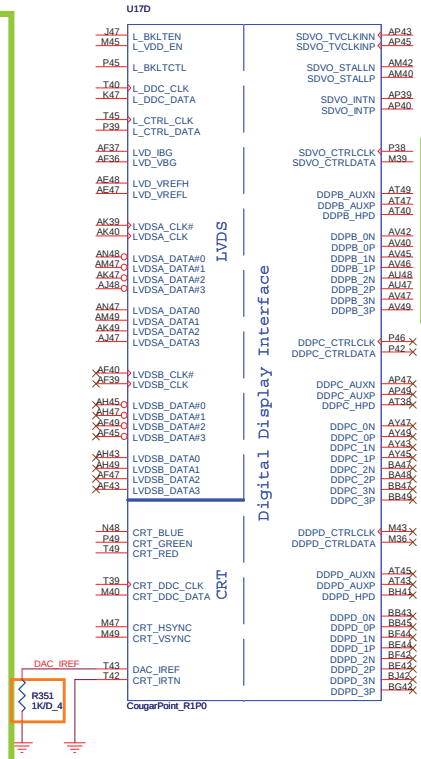
Size	Document Number	Rev
	Sandy Bridge 4/4	1A

Date: Wednesday, January 05, 2011 Sheet 6 of 44

Cougar Point (DMI,FDI,PM)<CLG>

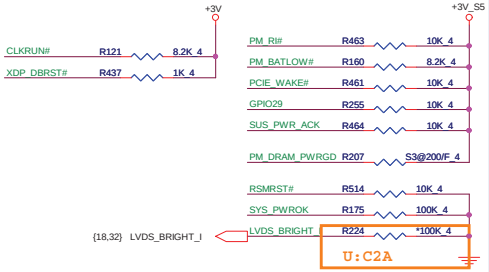


Cougar Point (LVDS,DDI)<CLG/UGA/HMG>

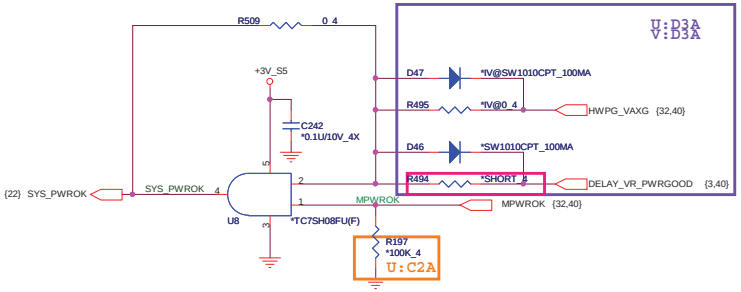


<CLG,UGA,HMG>

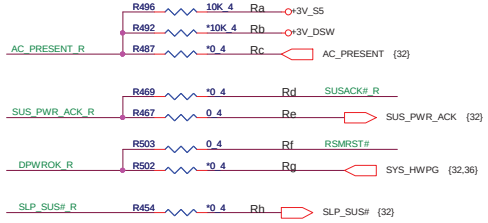
PCH Pull-high/low<CLG>



System PWR_OK <CLG>



Deep Sx <CLG>



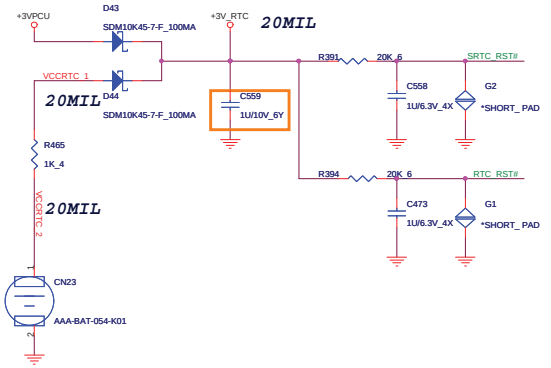
Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

Quanta Computer Inc.
PROJECT : TE5

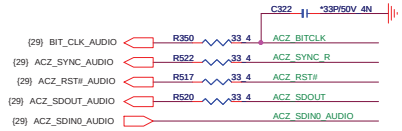
Size	Document Number	Rev
	Cougar Point 1/6	1A

Date: Wednesday, January 05, 2011 Sheet 7 of 44

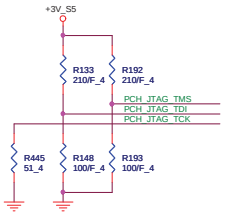
RTC Circuitry(RTC)



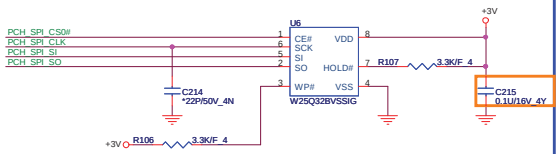
HDA Bus(CLG)



PCH JTAG Debug (CLG)

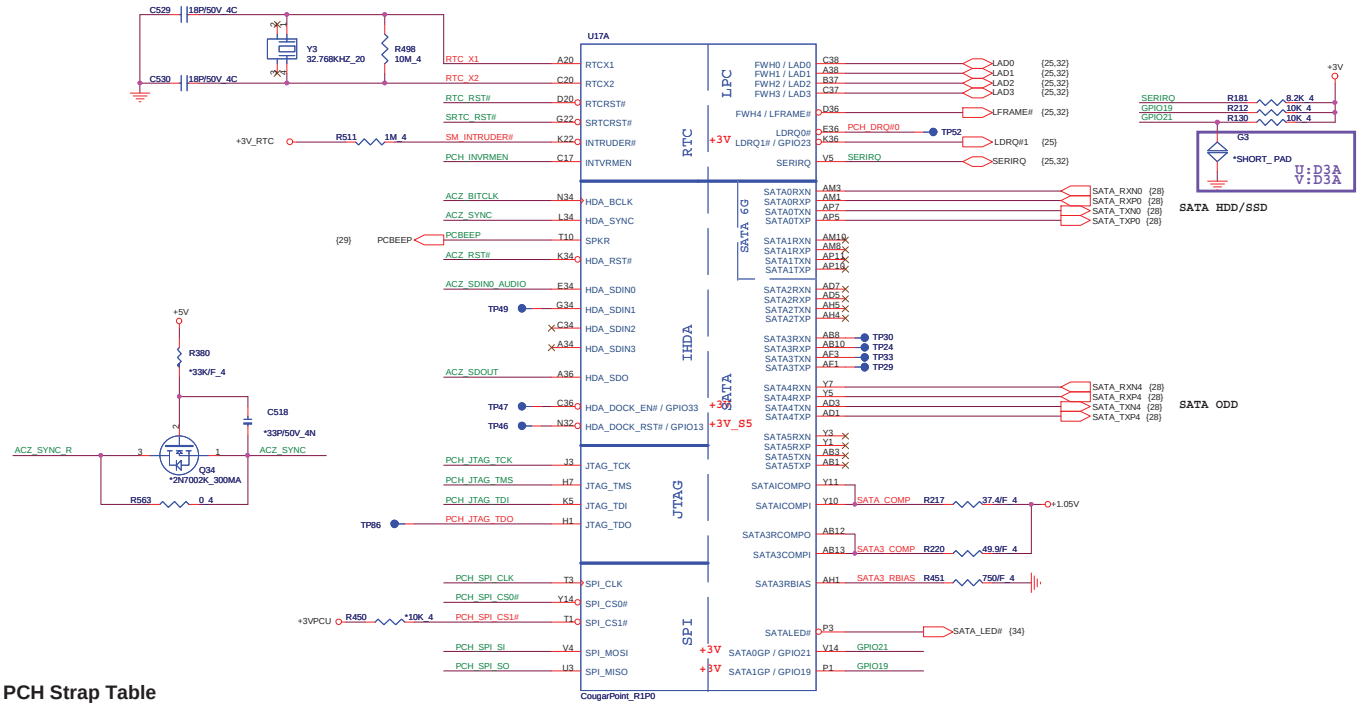


PCH Dual SPI (CLG)



PCH2 (CLG)

Cougar Point (HDA,JTAG,SATA)

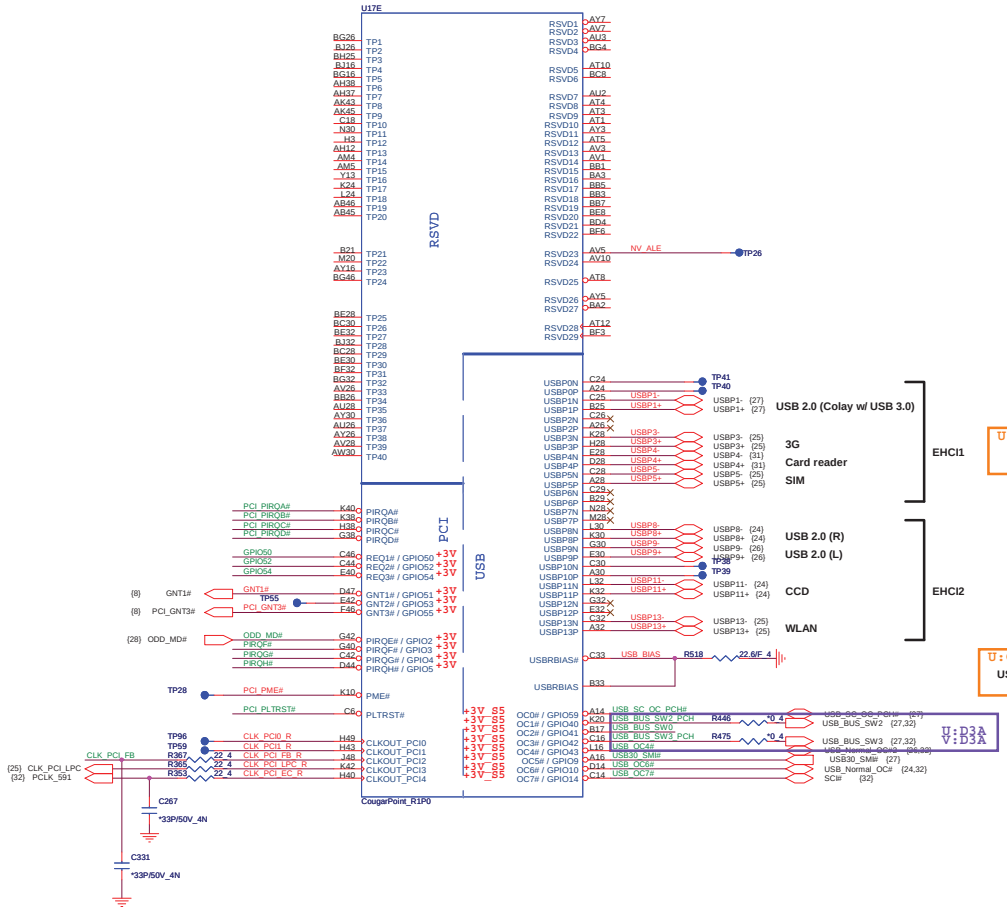


PCH Strap Table

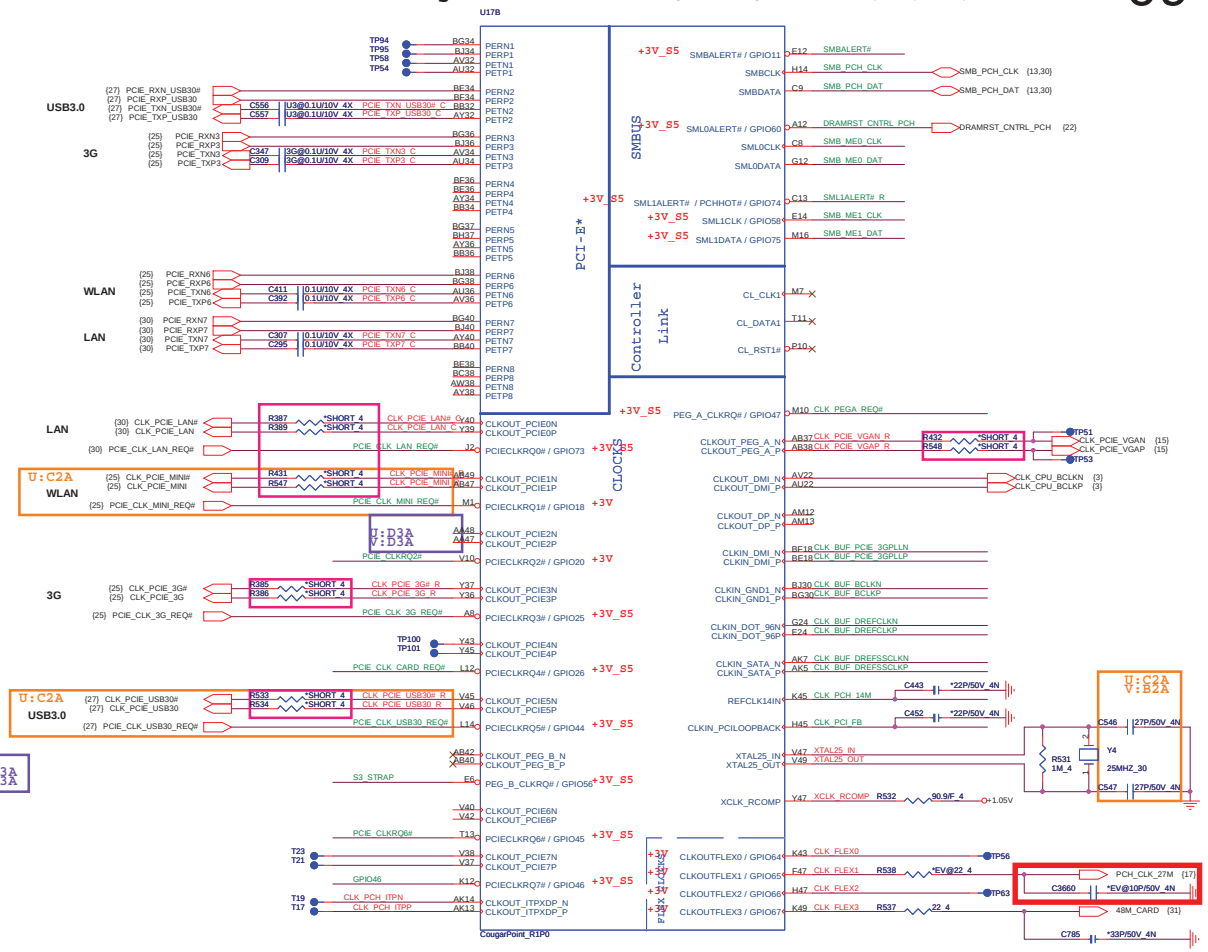
Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R116 *1K_4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R530 *1K_4 PCI_GNT3# {9}
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R497 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location 1 / 1 / SPI * 0 / 0 / LPC	R539 *1K_4 GNT1# {9} R449 *1K_4 GPIO19
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V R521 *1K_4 ACZ_SDOUT ACZ_SDOUT {32}
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R453 2.2K_4 +1.8V R452 1K_4 DF_TVS {10} H_SNB_IVB# {3}
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3V_S5 R206 *10K_4 R195 *1K_4 PLL_ODVR_EN {10}
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R525 1K_4 ACZ_SYNC
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect
GNT2#/ GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	+3V_S5 R313 1K_4 GPIO15 {10}
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP/ GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled
SATA2GP/ GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	DSWVREN {7} +3V_RTC R489 330K_4 R490 *330K_4

Quanta Computer Inc.
PROJECT : TE5
Size | Document Number: Cougar Point 2/6 | Rev 1A
Date: Wednesday, January 05, 2011 | Sheet 8 of 44

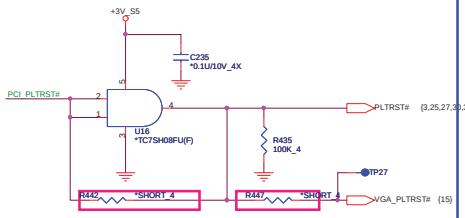
Cougar Point-M (PCI,USB,NVRAM) <CLG>



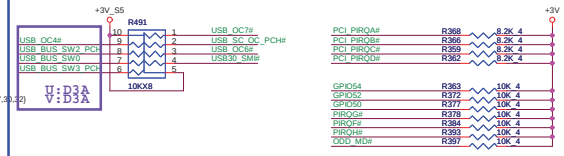
Cougar Point-M (PCI-E,SMBUS,CLK) <CLG,U3B,VGA,MNG>



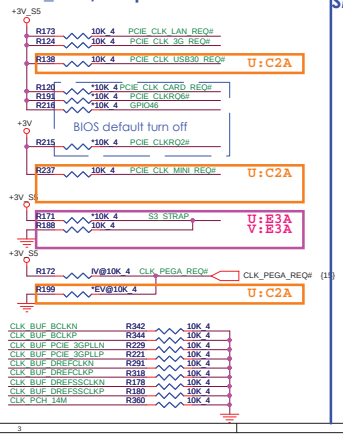
PLTRST# <CLG,VGA>



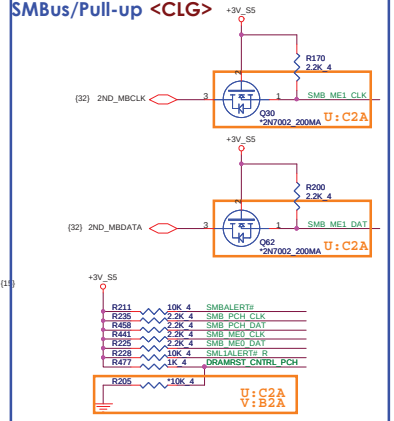
PCI/USBOC# Pull-up <CLG>



CLK_REQ/Strap Pin <CLG>



SMBus/Pull-up <CLG>



	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0	●	●	●	●	
CLK_FLEX1		●	●	●	
CLK_FLEX2	●	●	●	●	●
CLK_FLEX3		●	●	●	

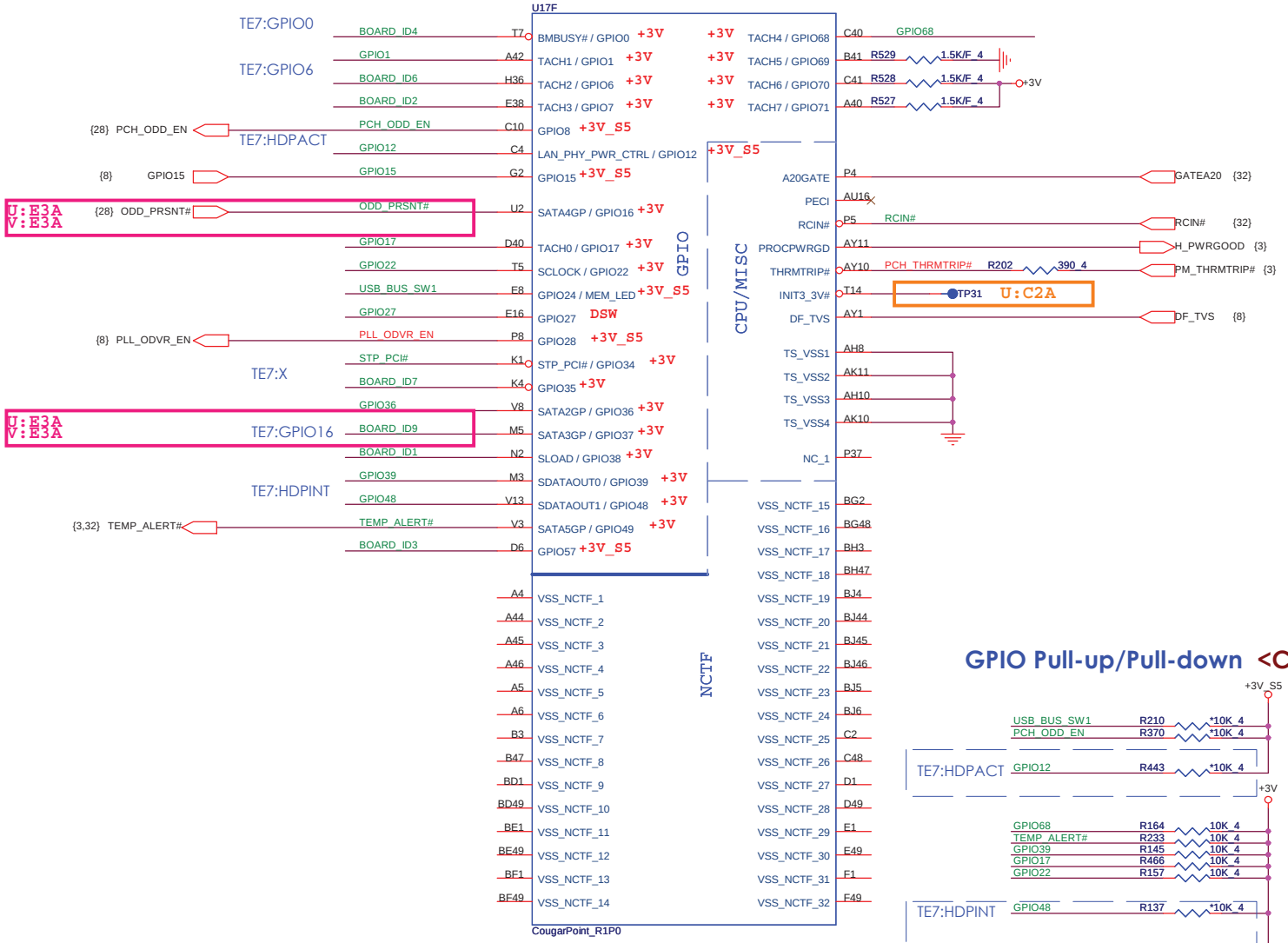
Quanta Computer Inc.

PROJECT : TE5

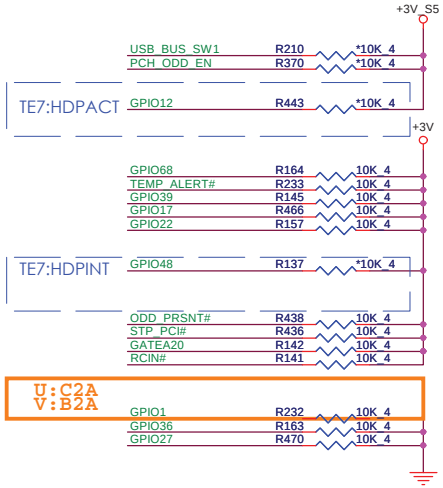
Size	Document Number	Rev
	Cougar Point 3/6	1A

Date: Wednesday, January 05, 2011 Sheet 9 of 44

Cougar Point (GPIO,VSS_NCTF,RSVD) <CLG>



GPIO Pull-up/Pull-down <CLG>

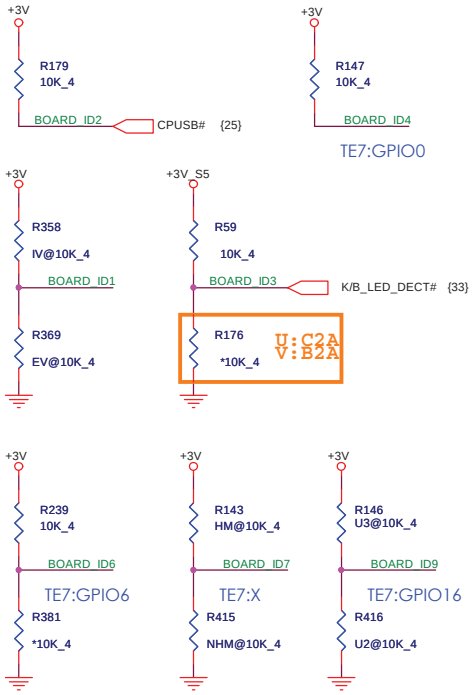


BOARD ID SETTING <CLG>

10

Board ID	ID1	ID2	ID3	ID4	ID6	ID7	ID9	GPIO1
UMA SKU VGA SKU	H L							
W/O 3G W/ 3G		H L						
W/O LED KB W/ LED KB			H L					
14" 15"				H L				
W/ MDC W/O MDC					H L			
W/ HDMI W/O HDMI						H L		
USB3.0 USB2.0							H L	
W/ G-sensor W/O G-sensor								H L

U:C2A



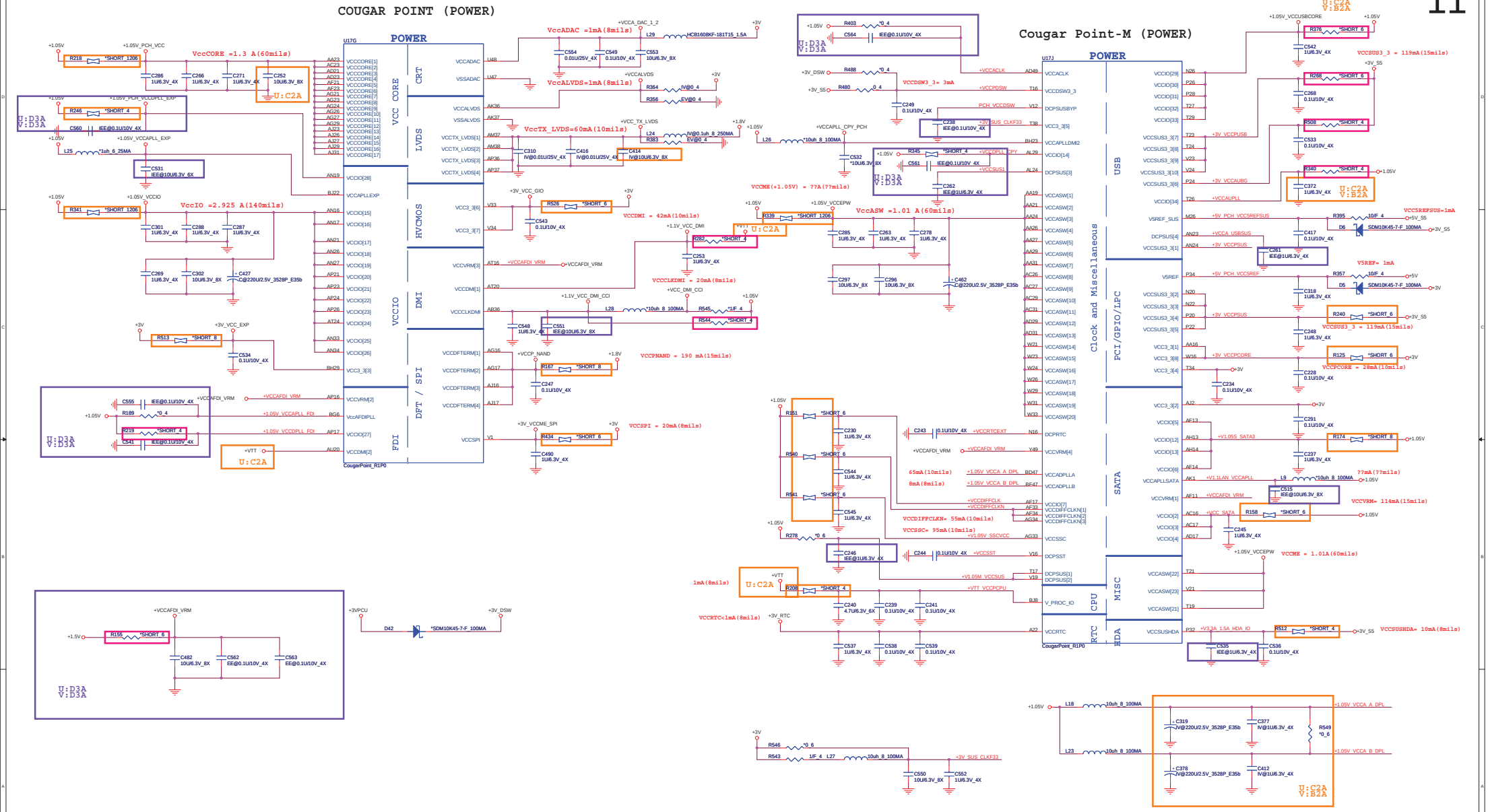
Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Rev
	Cougar Point 4/6	1A

Date: Wednesday, January 05, 2011 Sheet 10 of 44

COUGAR POINT (POWER)



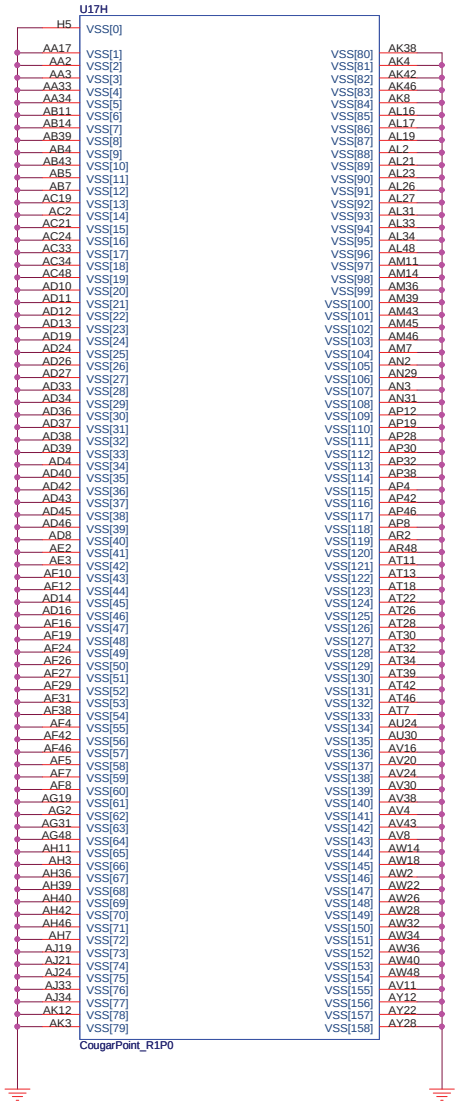
Quanta Computer Inc.

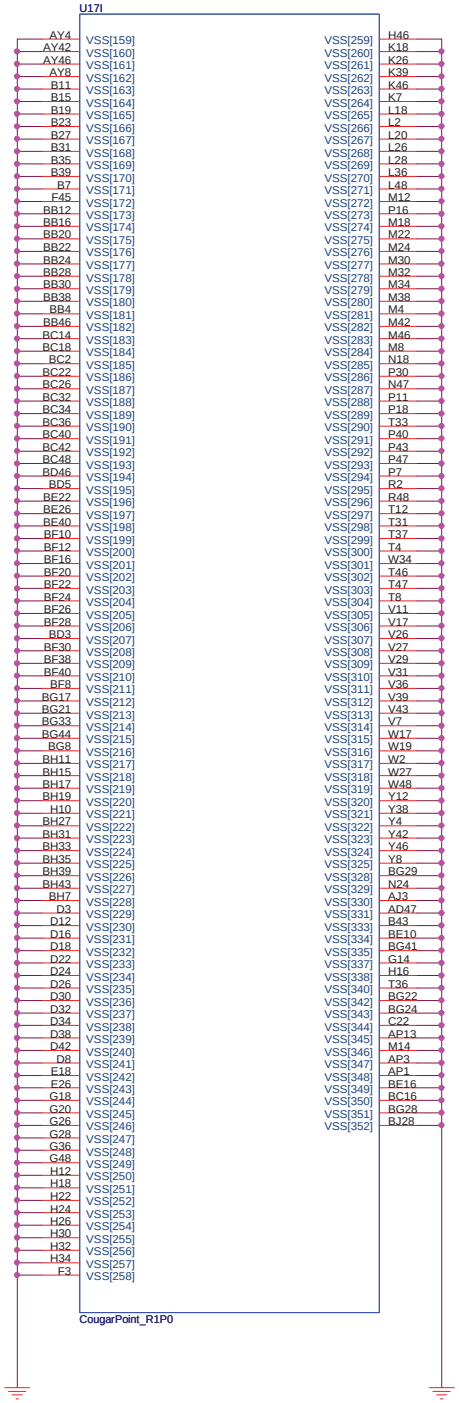
PROJECT : TE5

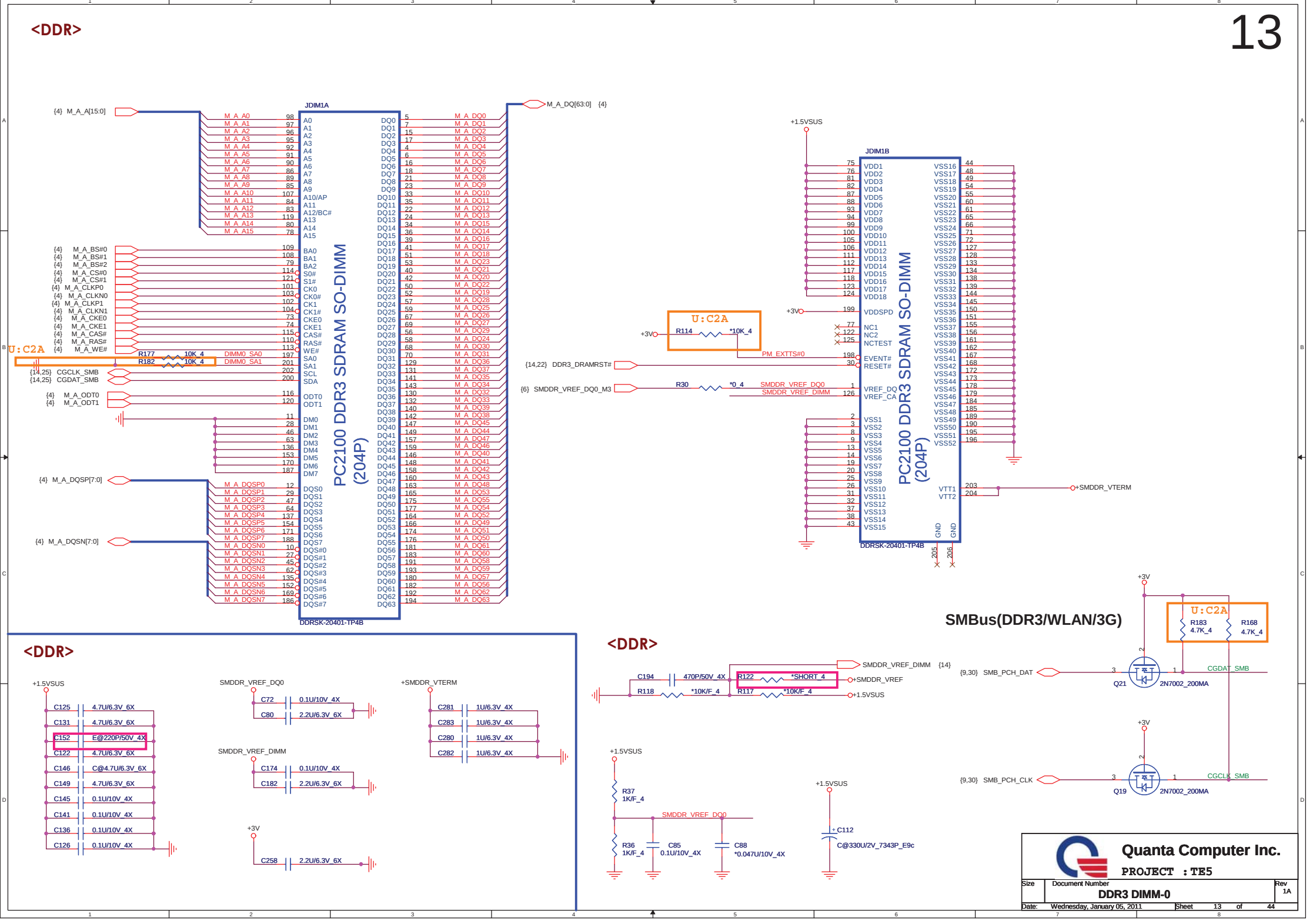
Size	Document Number	Rev
	Cougar Point 5/6	1A

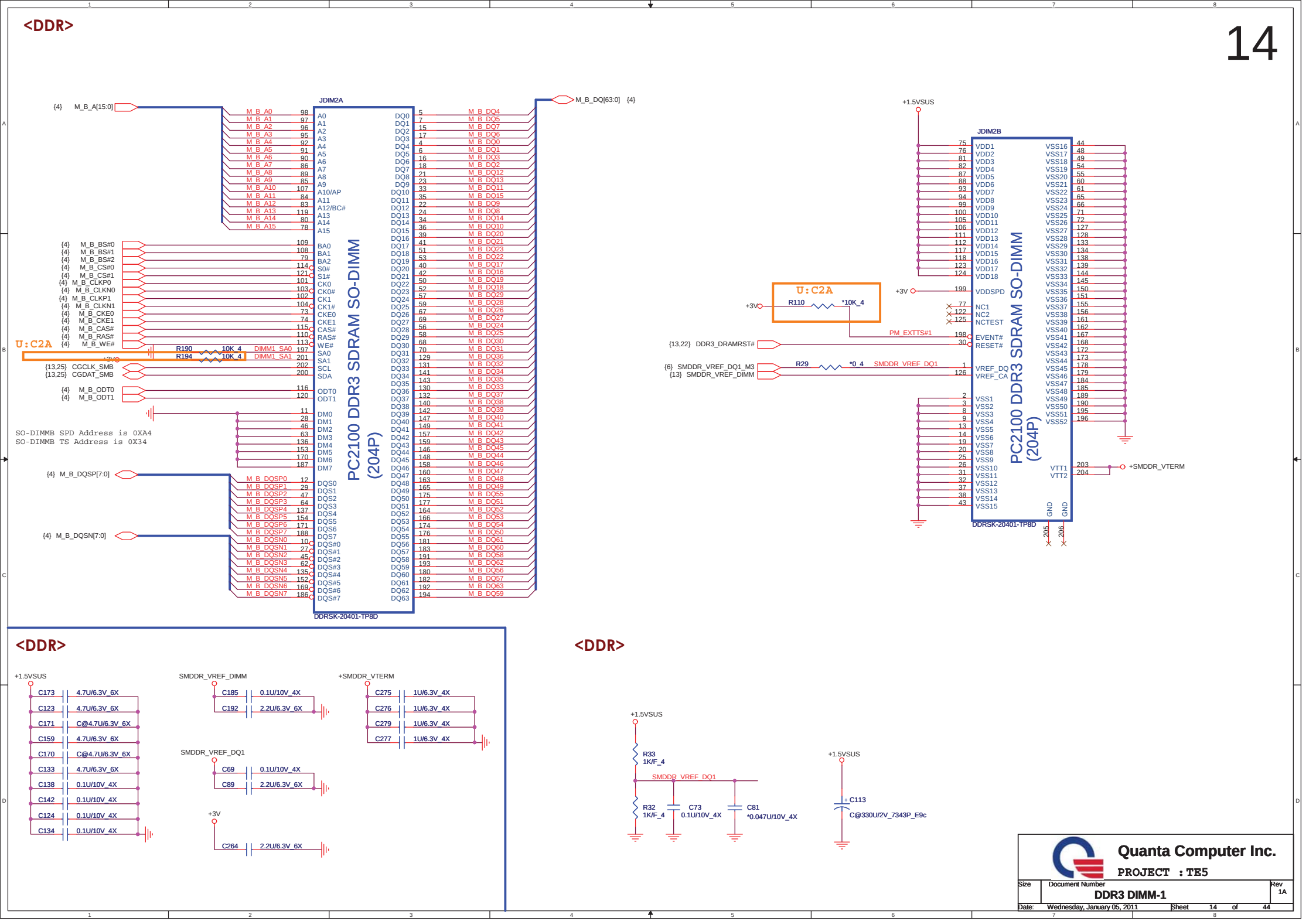
Date: Wednesday, January 05, 2011 Sheet 11 of 44

IBEX PEAK-M (GND)






<DDR>
JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDRSK-20401-TP4B
{4} M_A_A[15:0]
M_A_DQ[63:0] {4}
{4} M_A_BS#0
{4} M_A_BS#1
{4} M_A_BS#2
{4} M_A_CS#0
{4} M_A_CS#1
{4} M_A_CLKP0
{4} M_A_CLKN0
{4} M_A_CLKP1
{4} M_A_CLKN1
{4} M_A_CKE0
{4} M_A_CKE1
{4} M_A_CAS#
{4} M_A_RAS#
{4} M_A_WE#
U:C2A
R177 10K_4
R182 10K_4
DIMM0_SA0
DIMM0_SA1
{14,25} CGCLK_SMB
{14,25} CGDAT_SMB
{4} M_A_ODT0
{4} M_A_ODT1
{4} M_A_DQSP[7:0]
{4} M_A_DQSN[7:0]
+1.5VSUS
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDRSK-20401-TP4B
+3V
R114 *10K_4
PM_EXTTS#0
{14,22} DDR3_DRAMRST#
{6} SMDDR_VREF_DQ0_M3
R30 *0_4
SMDDR_VREF_DQ0
SMDDR_VREF_DIMM
+SMDDR_VTERM
<DDR>
+1.5VSUS
C125 4.7U/6.3V_6X
C131 4.7U/6.3V_6X
C152 E@220P/50V_4X
C122 4.7U/6.3V_6X
C146 C@4.7U/6.3V_6X
C149 4.7U/6.3V_6X
C145 0.1U/10V_4X
C141 0.1U/10V_4X
C136 0.1U/10V_4X
C126 0.1U/10V_4X
SMDDR_VREF_DQ0
C72 0.1U/10V_4X
C80 2.2U/6.3V_6X
SMDDR_VREF_DIMM
C174 0.1U/10V_4X
C182 2.2U/6.3V_6X
+3V
C258 2.2U/6.3V_6X
+SMDDR_VTERM
C281 1U/6.3V_4X
C283 1U/6.3V_4X
C280 1U/6.3V_4X
C282 1U/6.3V_4X
<DDR>
C194 470P/50V_4X
R118 *10K/F_4
R122 *SHORT_4
R117 *10K/F_4
SMDDR_VREF_DIMM {14}
+SMDDR_VREF
+1.5VSUS
+1.5VSUS
R37 1K/F_4
R36 1K/F_4
C85 0.1U/10V_4X
C88 *0.047U/10V_4X
SMDDR_VREF_DQ0
+1.5VSUS
C112
C@330U/2V_7343P_E9c
SMBus(DDR3/WLAN/3G)
+3V
U:C2A
R183 4.7K_4
R168 4.7K_4
{9,30} SMB_PCH_DAT
Q21 2N7002_200MA
CGDAT_SMB
{9,30} SMB_PCH_CLK
Q19 2N7002_200MA
CGCLK_SMB
Quanta Computer Inc.
PROJECT : TE5
Size
Document Number
DDR3 DIMM-0
Rev 1A
Date: Wednesday, January 05, 2011
Sheet 13 of 44

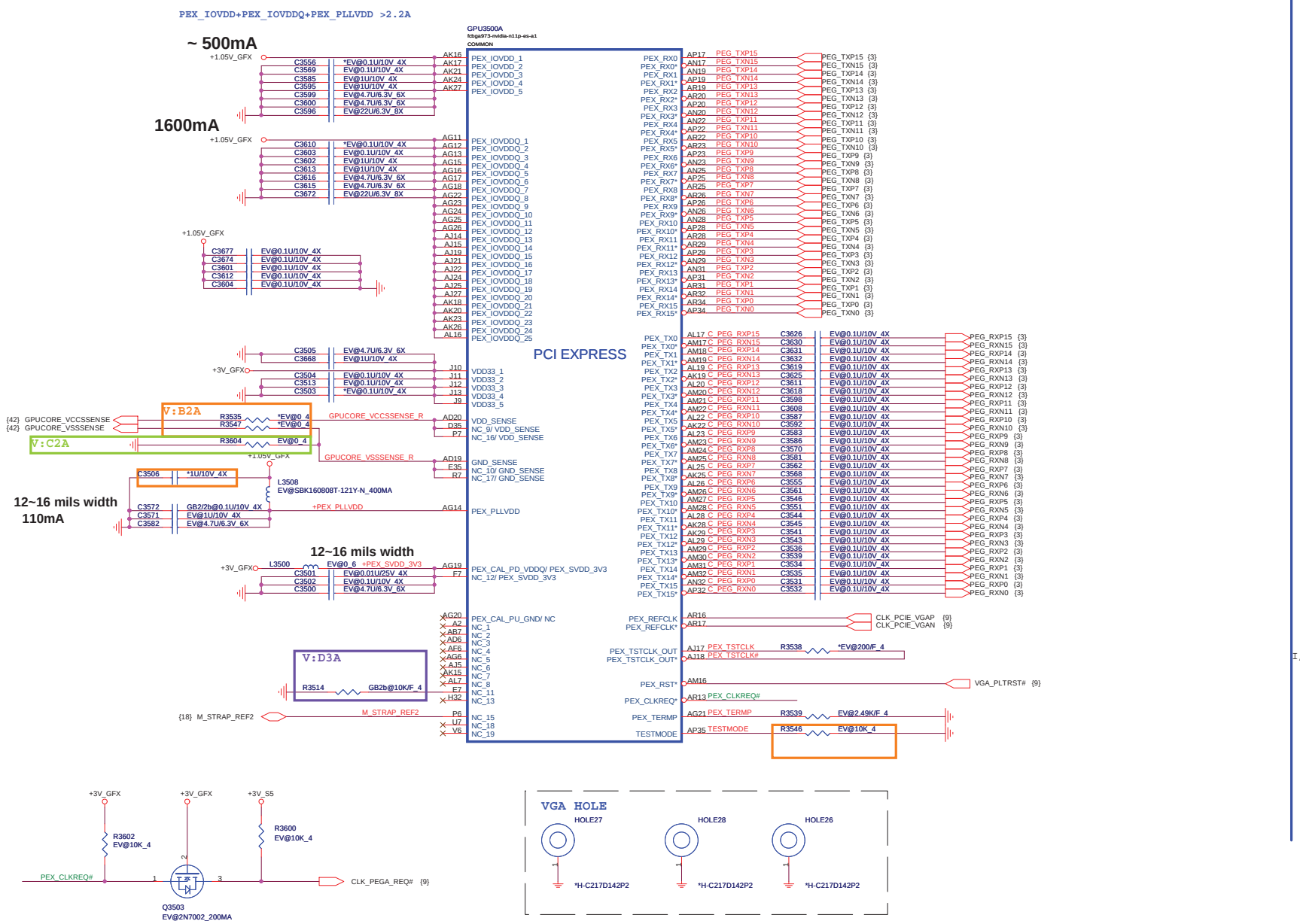


Quanta Computer Inc.

PROJECT : TE5

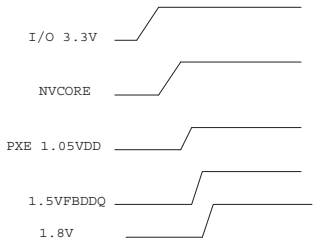
Size	Document Number	Rev
	DDR3 DIMM-1	1A

Date: Wednesday, January 05, 2011 Sheet 14 of 44



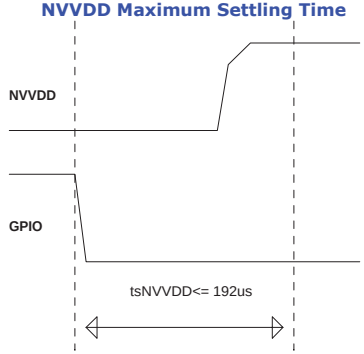
15-V

power up sequence

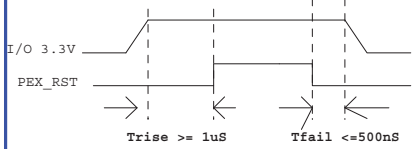


NB9M: VGACORE +0.90V (Normal) , +1.09V

NVDD Maximum Settling Time



PEX_RST timing



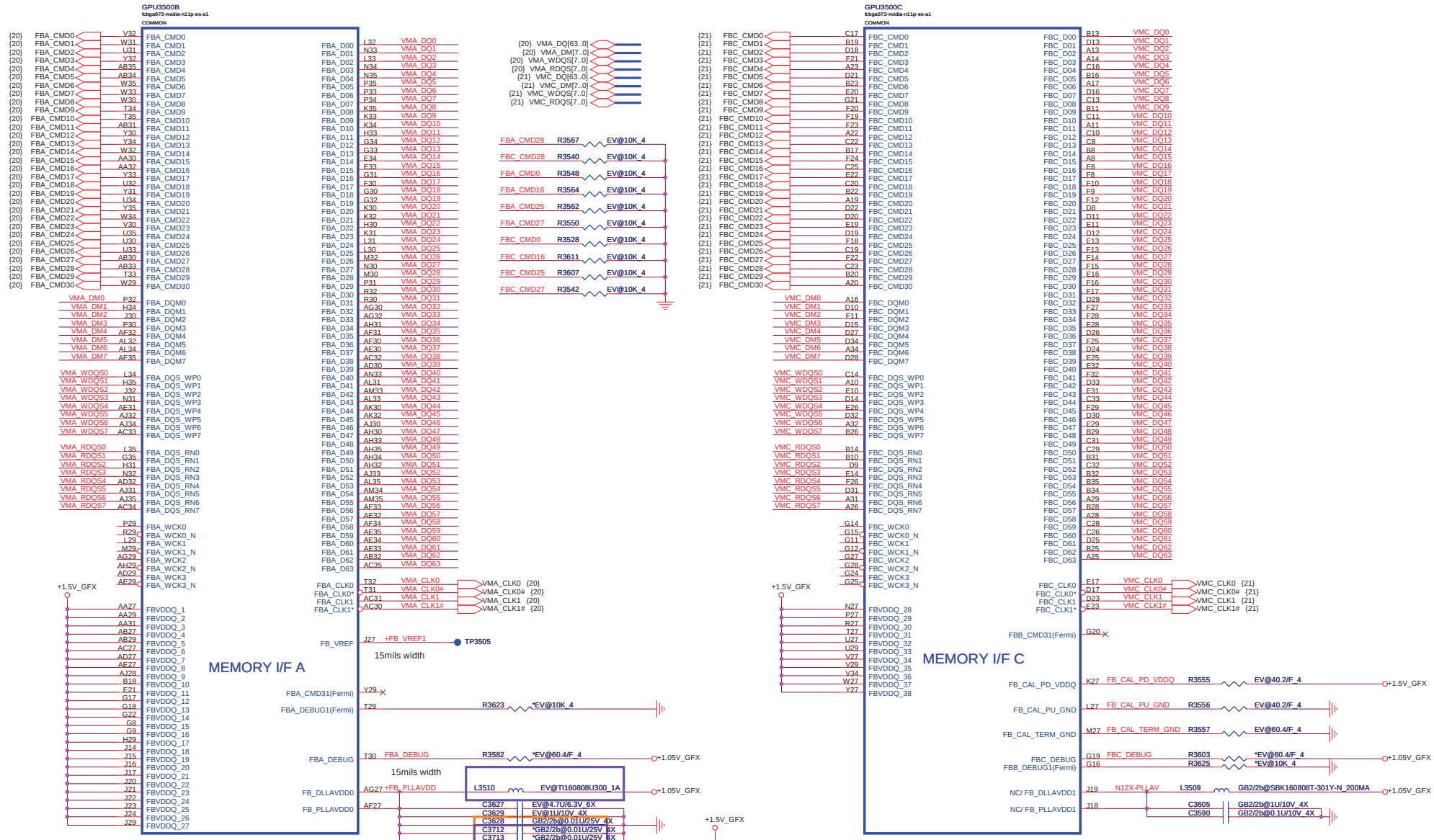
Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Rev
	N11x-Fermi PCIE	1A

Date: Wednesday, January 05, 2011 Sheet 15 of 44

16-V



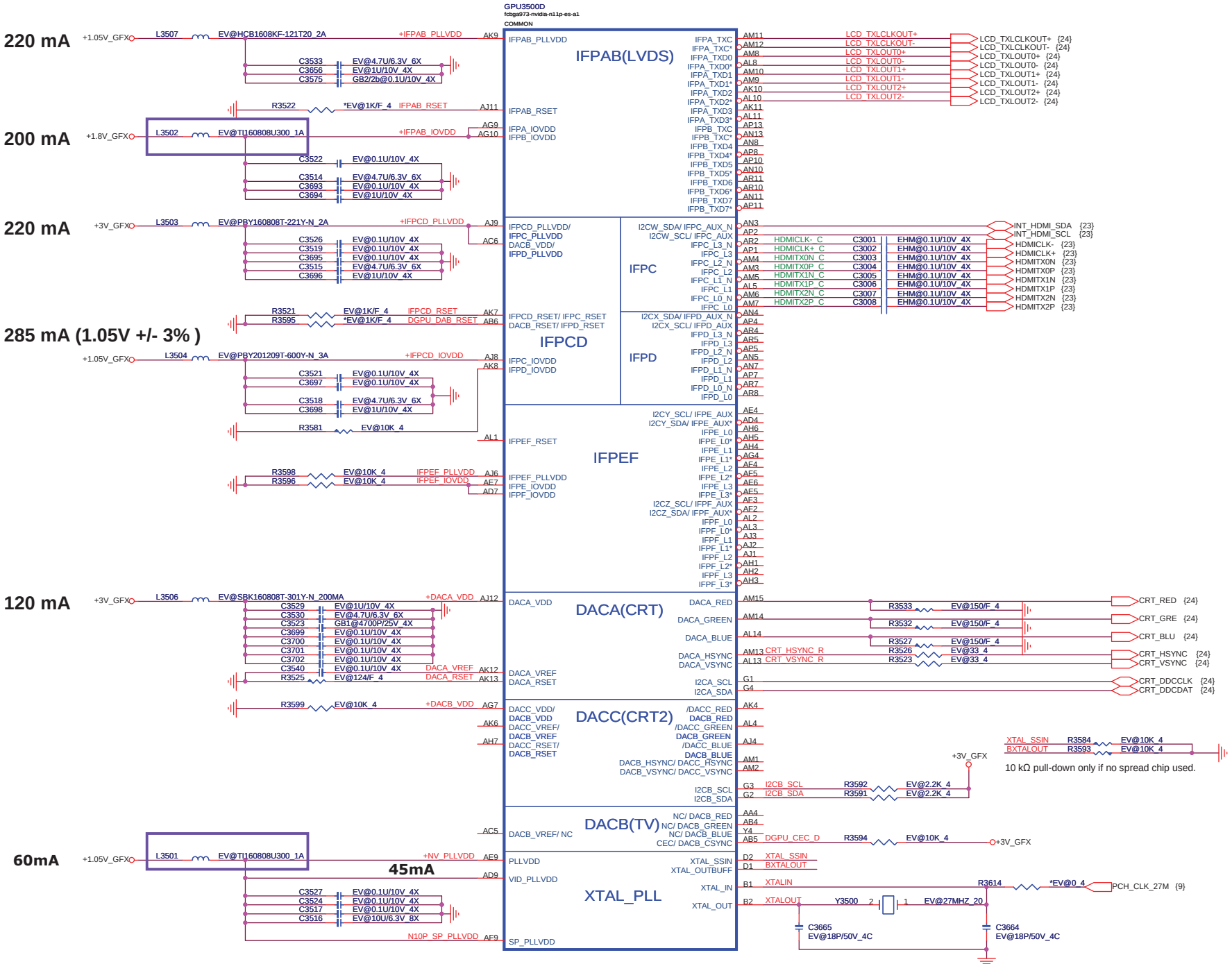
Size	Document Number	Rev
	N11x-Fermi (MEM I/F)	1A

Quanta Computer Inc.

PROJECT : TE5

Date: Wednesday, January 05, 2011 Sheet 16 of 44

17-V

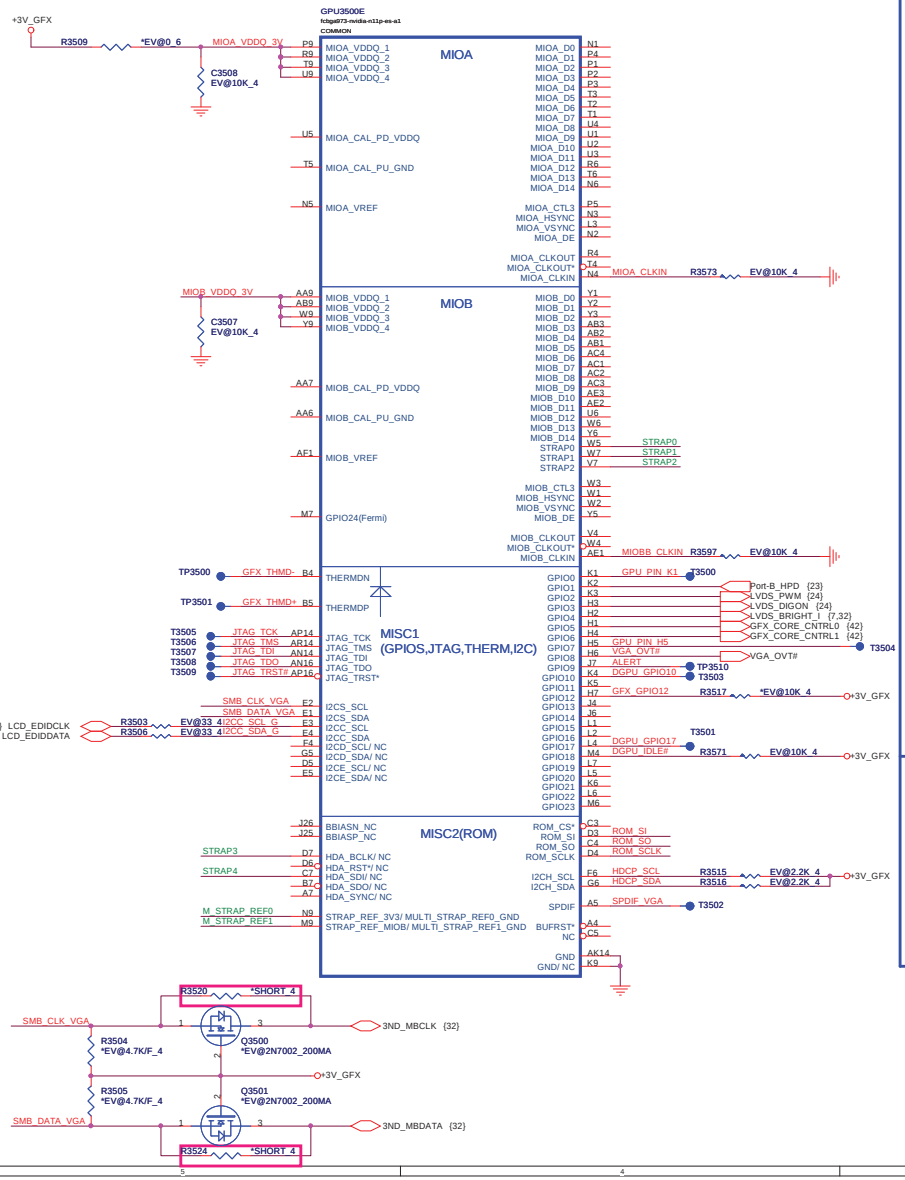


Quanta Computer Inc.

PROJECT : TE5

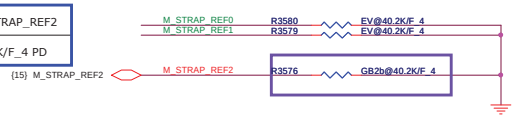
Size	Document Number	Rev
	N11x-Fermi (DISPLAY)	1A

Date: Wednesday, January 05, 2011 Sheet 17 of 44

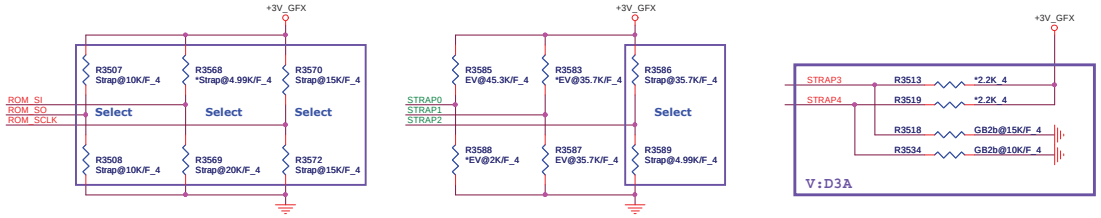


Strappin Model select

MODE	M_STRAP_REF0	M_STRAP_REF1	M_STRAP_REF2
Multi-level	40.2K/F_4 PD	40.2K/F_4 PD	40.2K/F_4 PD



MULTI level strap select



		Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N12M-GE	N12P-GV	N12P-LP	
ROM_SCLK		PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG PCI_DEVIDE[5]	PEX_PLL_EN_TERM	1010(15KPU)	1001(10KPU)	0010(15KPD)	
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	RAMCFG_T		RAMCFG_T	
ROM_SO	GB1/2	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001(10KPD)		0001(10KPD)	Need to Update
	GB2B	FB[1]	FB[0]				1001(10KPU)		
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]	1111(45KPU)	1111(45KPU)	1111(45KPU)	
STRAP1		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110(35KPD)	0110(35KPD)	0110(35KPD)	Need to Update
STRAP2		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1010(15KPU)	0000(5KPD)	1100(25KPU)	
STRAP3(Only GB2B)		SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED		0010(15KPD)		Need to Update
STRAP4(Only GB2B)		Reserve	Reserve	PCIE_MAX_SPEED	DP_PLL_VDD33V		0001(10KPD)		

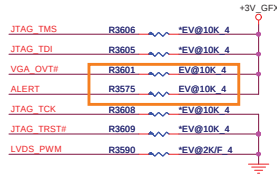
VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0x0 0000				
0x1 0001				
0x2 0010	DDR3 64Mx16x8, 128bit, 1GB	Hynix	H5TQ1G63DFR-12C(800MHz) / H5TQ1G63DFR-11C(900MHz)	PD 15K
0x3 0011	DDR3 64Mx16x8, 128bit, 1GB	Samsung	K4W1G1646E-HC12(800MHz) / K4W1G1646E-HC11(900MHz)	PD 20K
0x4 0101				
0x5 0110				
0x6 0110	DDR3 128Mx16x8, 128bit, 2GB	Hynix	H5TQ2G63BFR-12C(800MHz) / H5TQ2G63BFR-11C(900MHz)	PD 35K
0x7 0111	DDR3 128Mx16x8, 128bit, 2GB	Samsung	K4W2G1646C-HC1(800MHz)2 / K4W2G1646C-HC11(900MHz)	PD 45K

N12M-GE(QS)
Device Id=0x0A7A
STRAP2 =15K PU
ROM_SCLK=15K PU

N12P-GV(QS)
Device Id=-x1050
STRAP2 =5K PD
ROM_SCLK=10K PU

N12P-LP(QS)
Device Id=0x0DEC
STRAP2=25K PU
ROM_SCLK=15K PD



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Quanta Computer Inc.

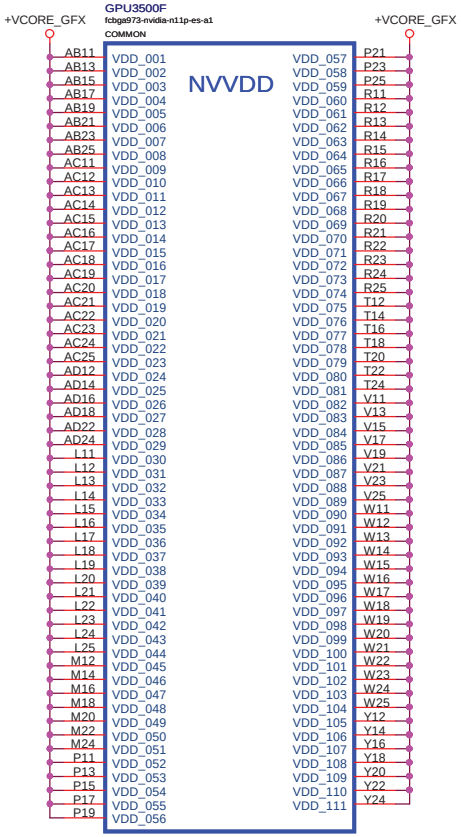
PROJECT : TE5

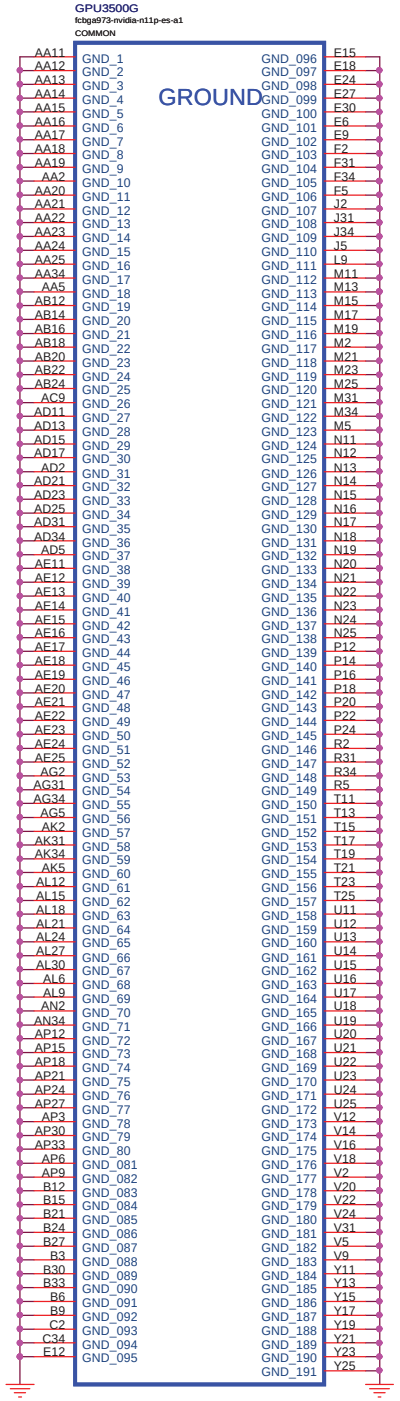
Size	Document Number	Rev
	N11x-Fermi (GND&Str&Ther)	1A

Date: Wednesday, January 05, 2011 Sheet 18 of 44

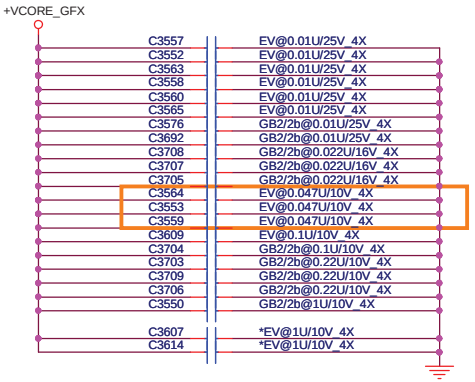
18-V

19-V





PLACE UNDER BALLS



PLACE NEAR BALLS

Quanta Computer Inc.

PROJECT : TE5

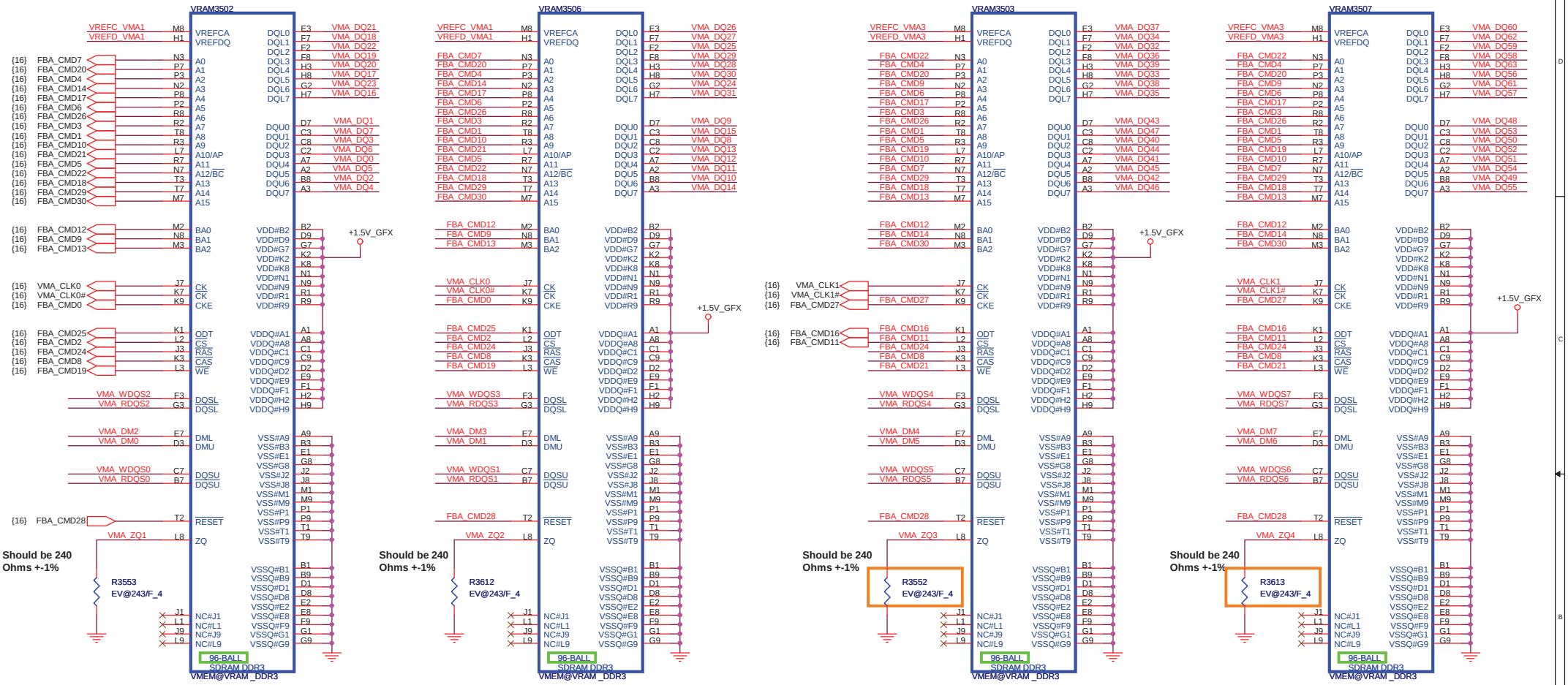
Size	Document Number	Rev
	N11x-Fermi (GND/Power)	1A

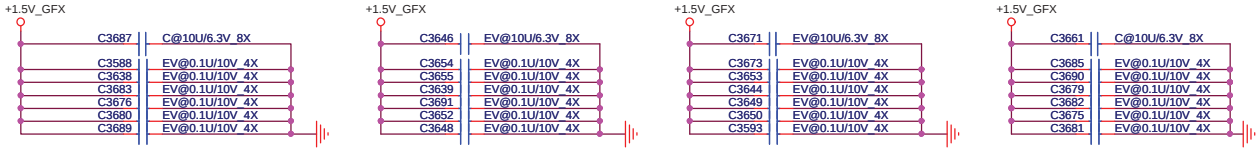
Date: Wednesday, January 05, 2011 Sheet 19 of 44

20-V

CHANNEL A: 256MB/512MB DDR3

{16} VMA_DQ[63..0]
{16} VMA_DM[7..0]
{16} VMA_WDQS[7..0]
{16} VMA_RDQS[7..0]





Quanta Computer Inc.

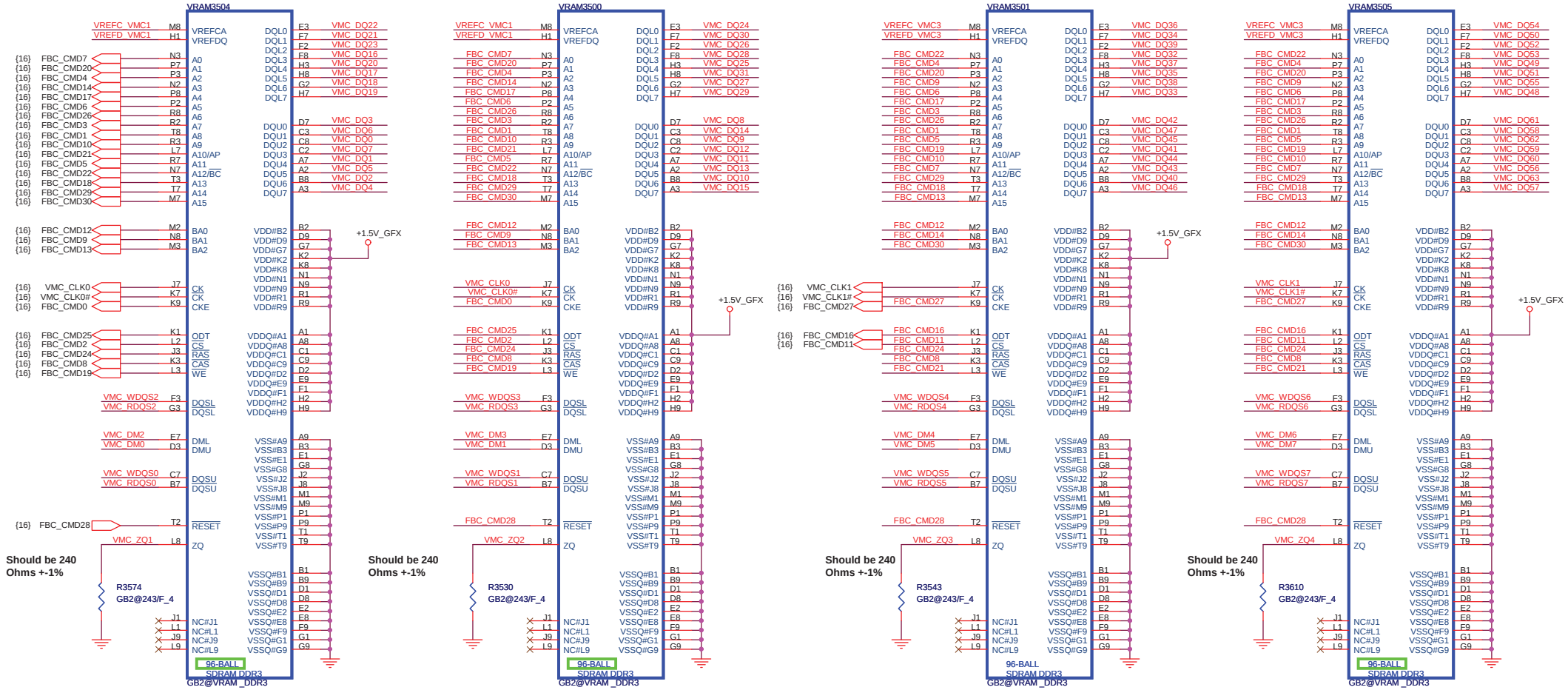
PROJECT : TE5

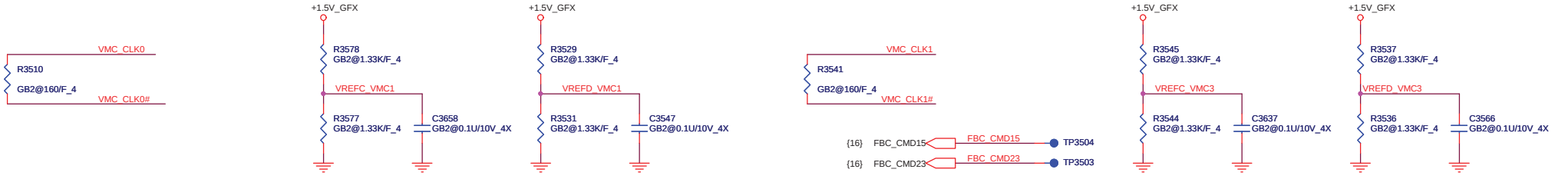
Size	Document Number	Rev
	N11x-Fermi VRAM A	1A

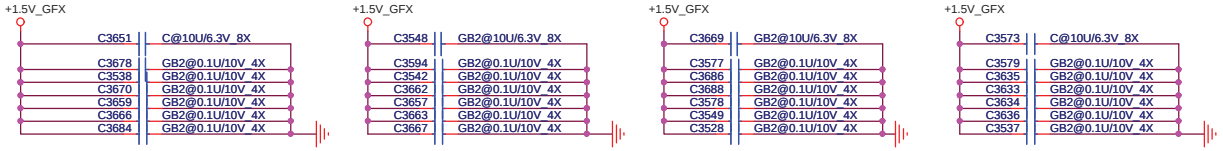
Date: Wednesday, January 05, 2011 Sheet 20 of 44

CHANNEL B: 256MB/512MB DDR3

{16} VMC_DQ[63..0]
{16} VMC_DM[7..0]
{16} VMC_WDQS[7..0]
{16} VMC_RDQS[7..0]







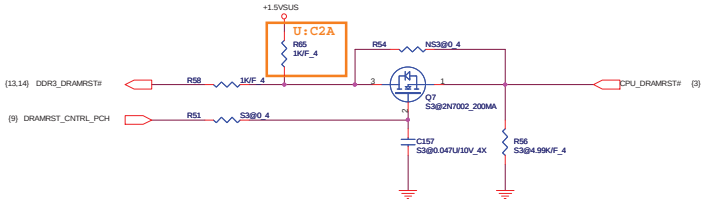
Quanta Computer Inc.

PROJECT : TE5

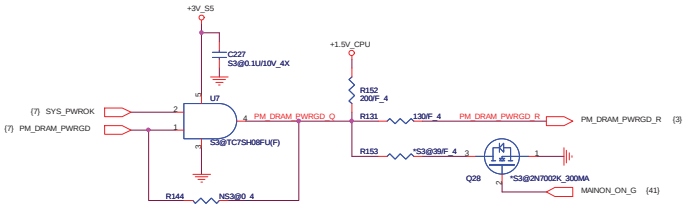
Size	Document Number	Rev
	N11x-Fermi VRAM B	1A

Date: Wednesday, January 05, 2011 Sheet 21 of 44

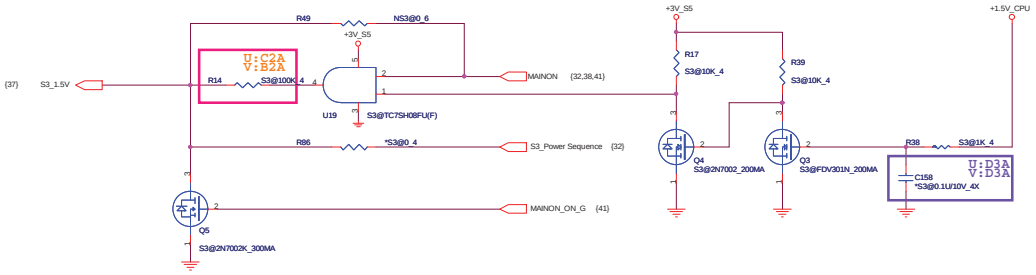
S3 power Reduction (SM_DRAMRST#) <S3P> <4>



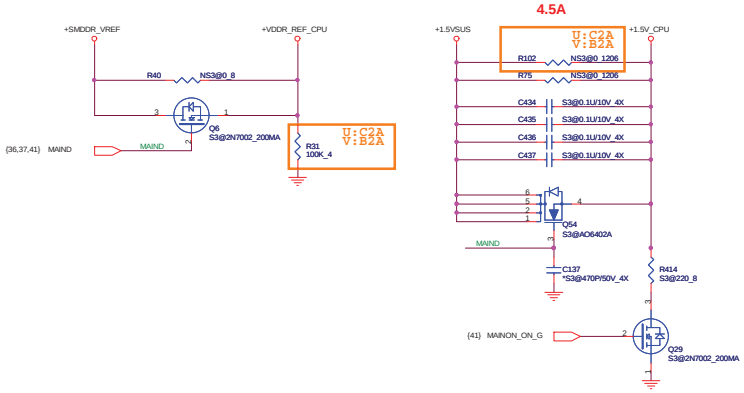
S3 power Reduction (SM_DRAMPWROK) <S3P> <3>



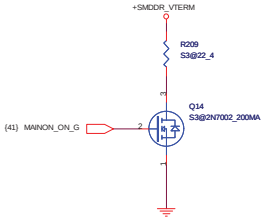
For S3 power Reduction Sequence <S3P> <3>



S3 power Reduction (CPU Power) <S3P> <5>



For S3 power Reduction VTT discharge <S3P> <13>



Quanta Computer Inc.

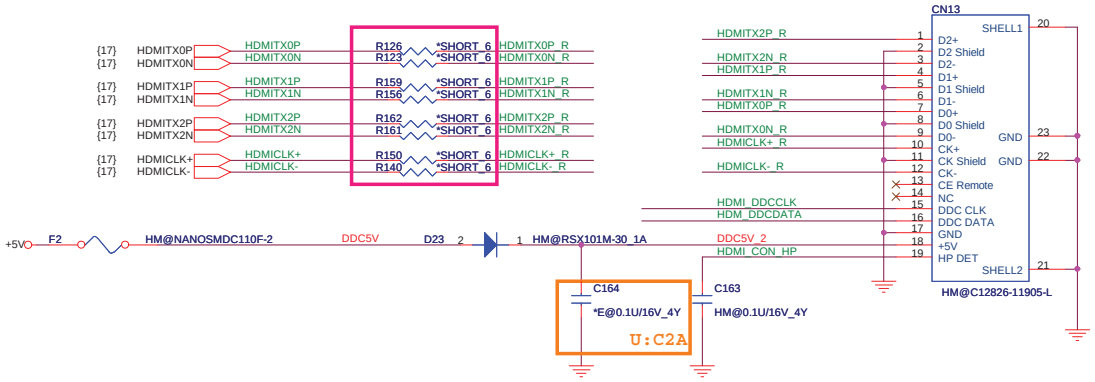
PROJECT : TE5

Size	Document Number	Rev
	S3 power Reduction	1A

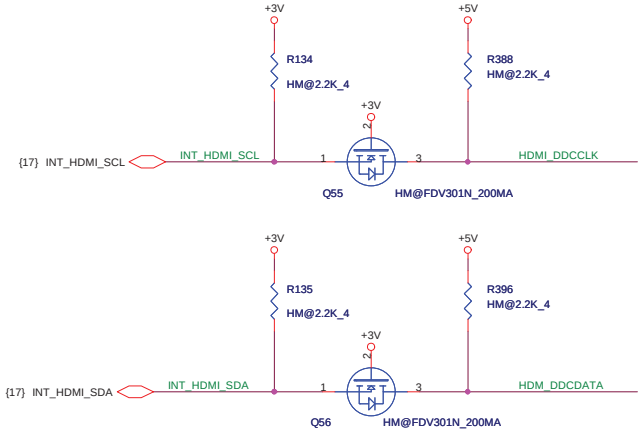
Date: Wednesday, January 05, 2011 Sheet 22 of 44

HDMI Conn [HDM]

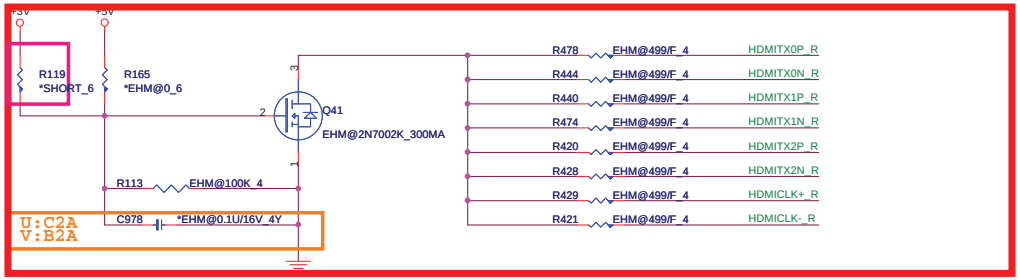
HDMI-CONN <HDM>



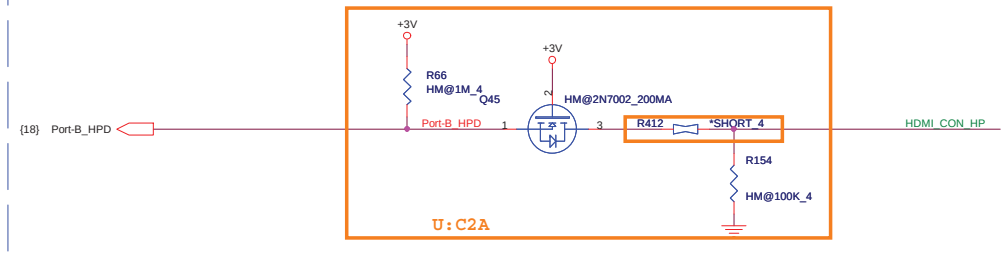
HDMI-SMBus <HDM>



HDMI-passive level shift <HMP/HMG>



HDMI-HPD <HMP/HMG>



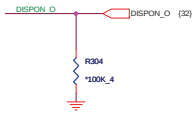
Quanta Computer Inc.

PROJECT : TE5

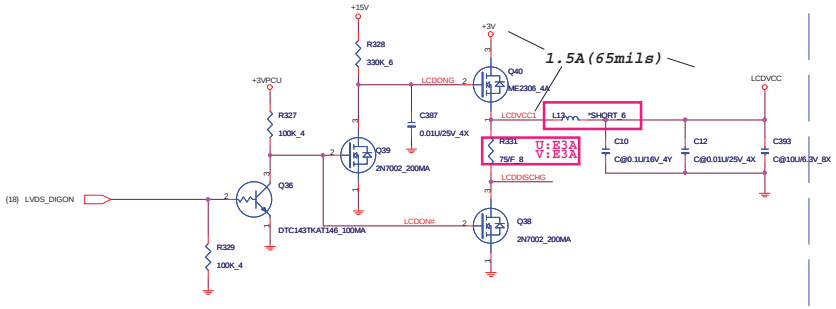
Size	Document Number	Rev
	HDMI CONN	1A

Date: Wednesday, January 05, 2011 Sheet 23 of 44

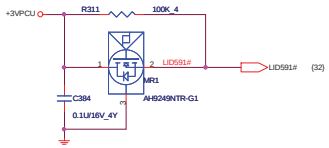
Panel backlight control <LDS>



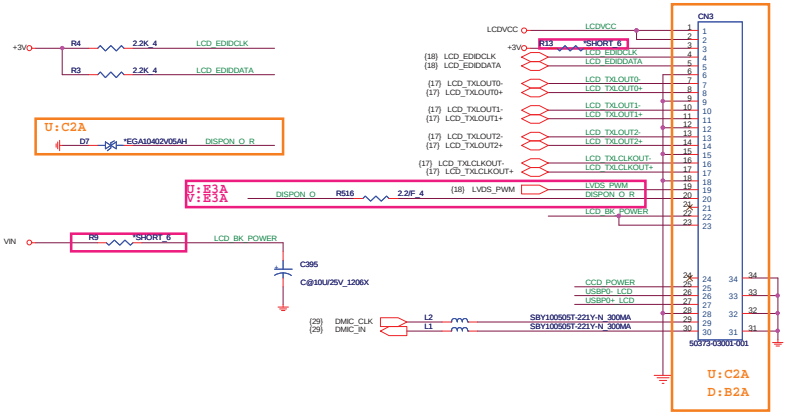
LCD POWER SWITCH <LDS>



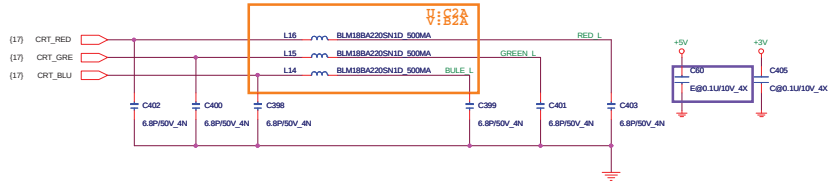
HALL Sensor <HSR>



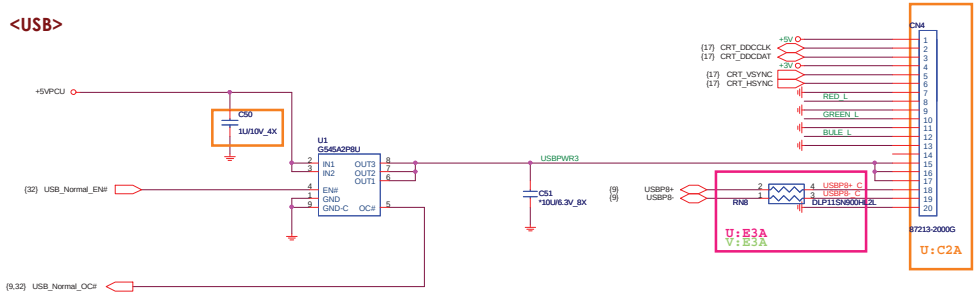
LCD Panel Module [LDS]



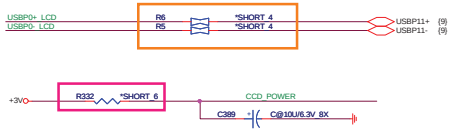
CRT <CRT>



USB for CRT BOARD (Right) <USB>



CCD [CCD]



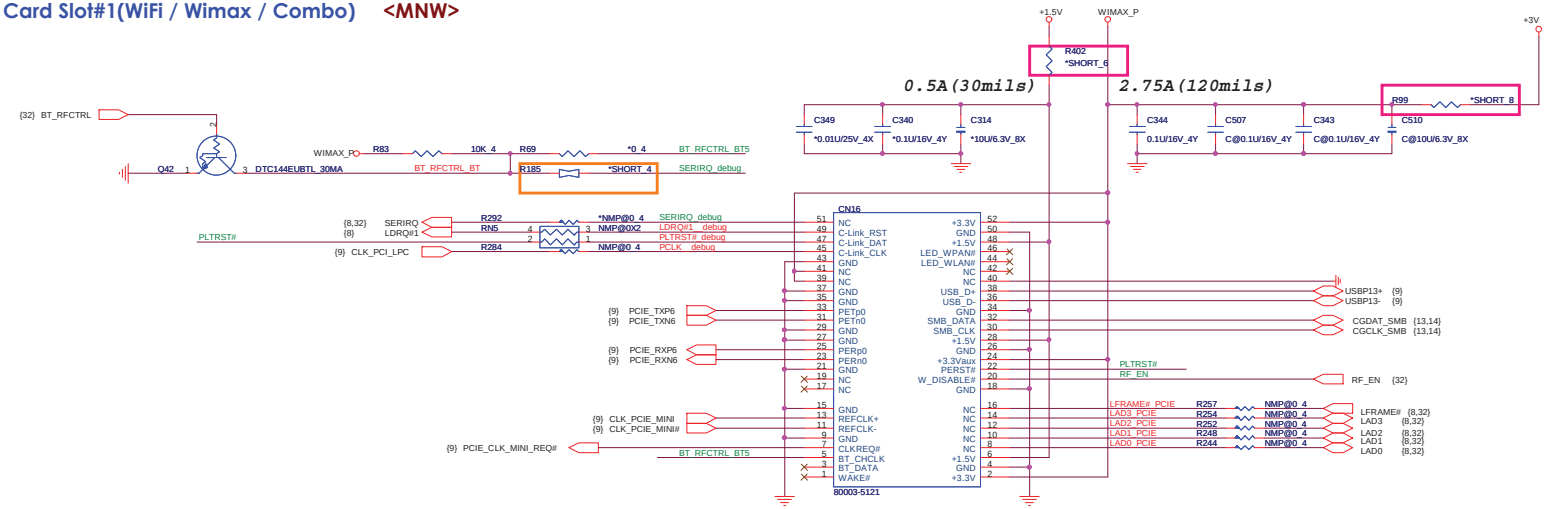
Quanta Computer Inc.

PROJECT : TE5

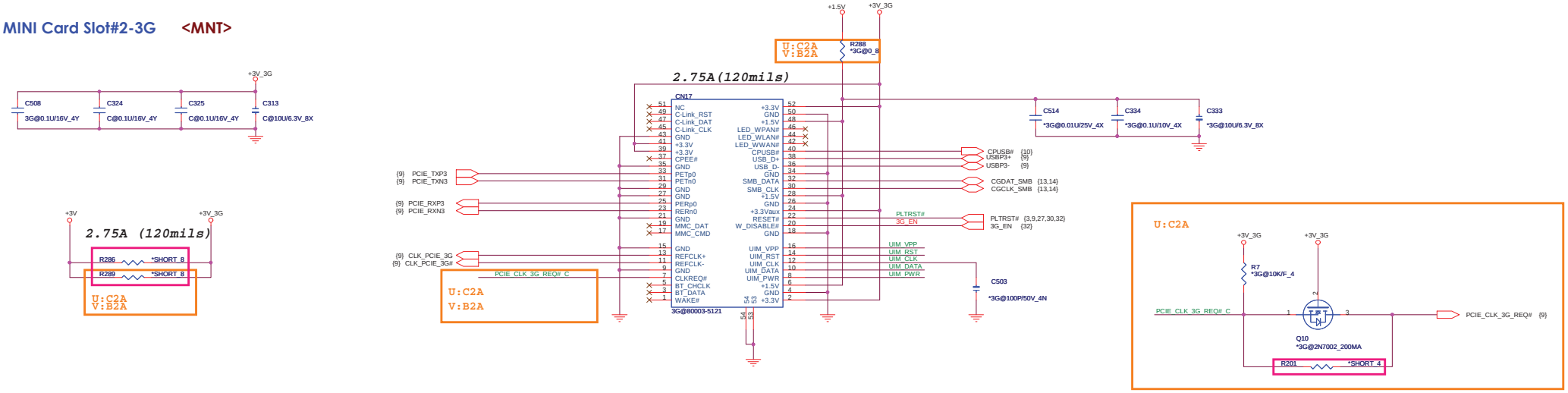
Size	Document Number	Rev
	LCD/LED Panel/CCD	1A

Date: Wednesday, January 05, 2011 Sheet 24 of 44

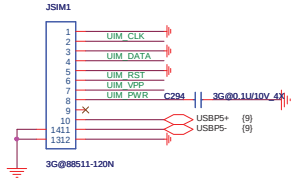
MINI Card Slot#1(WiFi / Wimax / Combo) <MNW>



MINI Card Slot#2-3G <MNT>

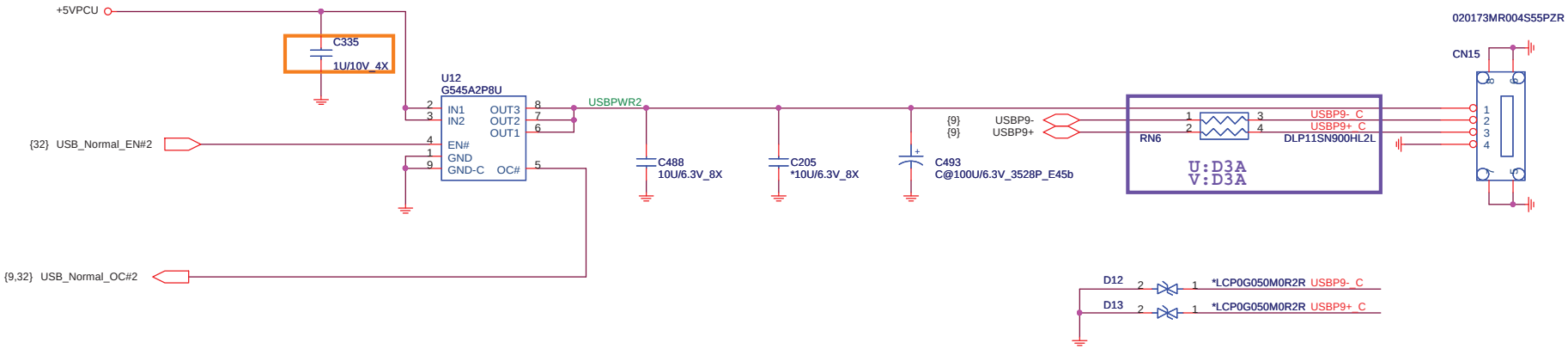


SIM CARD



Quanta Computer Inc.	PROJECT : TE5	
Size	Document Number: MINI CARD(WLAN/3G/SIM Card)	Rev 1A
Date: Wednesday, January 05, 2011	Sheet 25 of 44	

USB2.0 MB SIDE (Left) <USB>



Quanta Computer Inc.

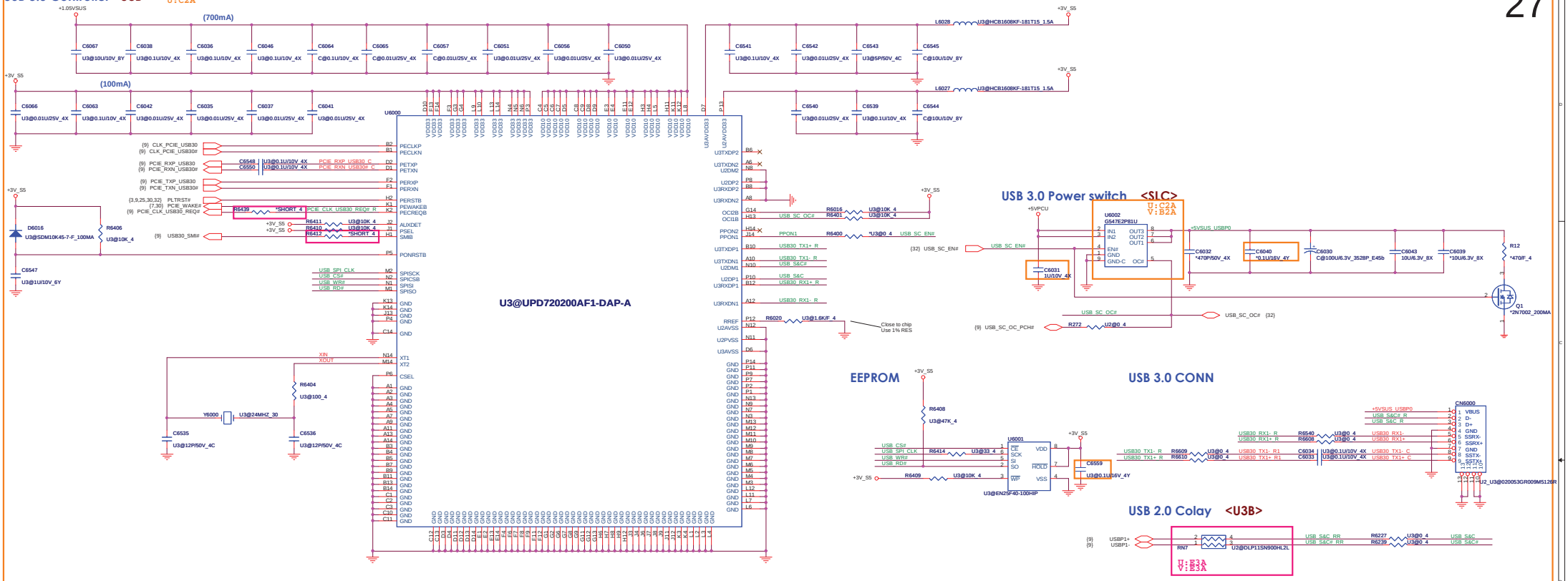
PROJECT : TE5

Size	Document Number	Rev
	TP/SW/ESATA/USB+Audio/LED	1A

Date: Wednesday, January 05, 2011 Sheet 26 of 44

USB 3.0 Controller <U3B>

U:C2A



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

Quanta Computer Inc.

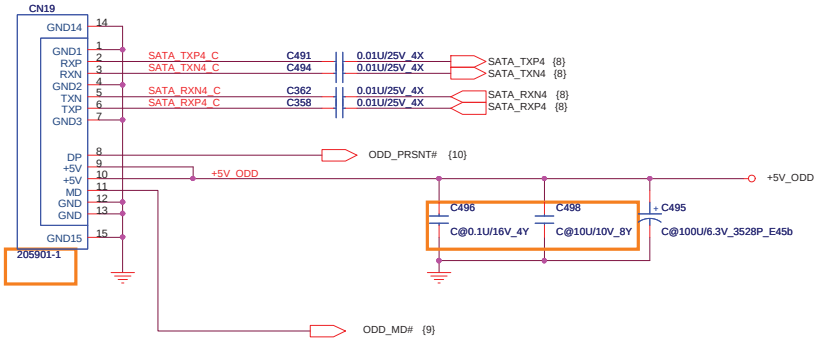
PROJECT : TE5

Size	Document Number	Rev
	MINI CARD(WLAN/3G/SIM Card)	1A

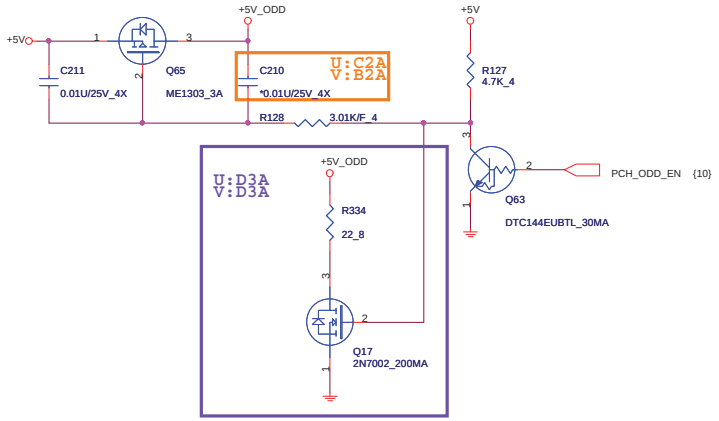
Date: Wednesday, January 05, 2011 Sheet 27 of 44

SATA ODD

[ODD]

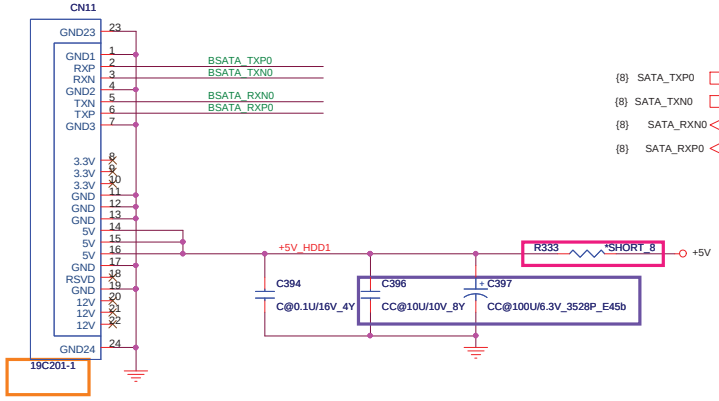


ODD Zero power . (Only for Intel) <OZP>

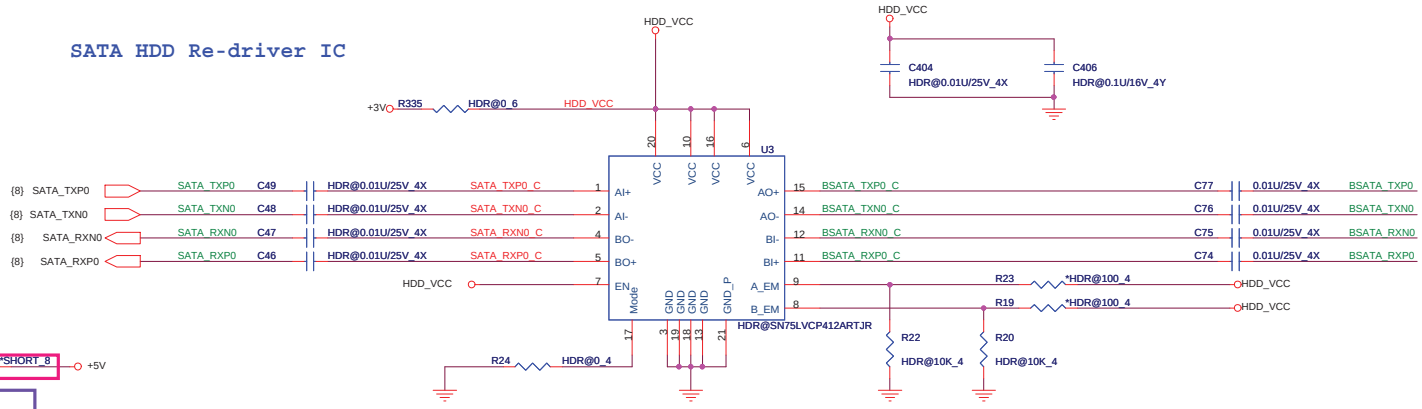


SATA HDD

[HDD]

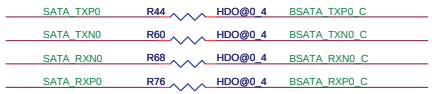


SATA HDD Re-driver IC



SATA Re-driver Bypass

Colay with Redriver IC



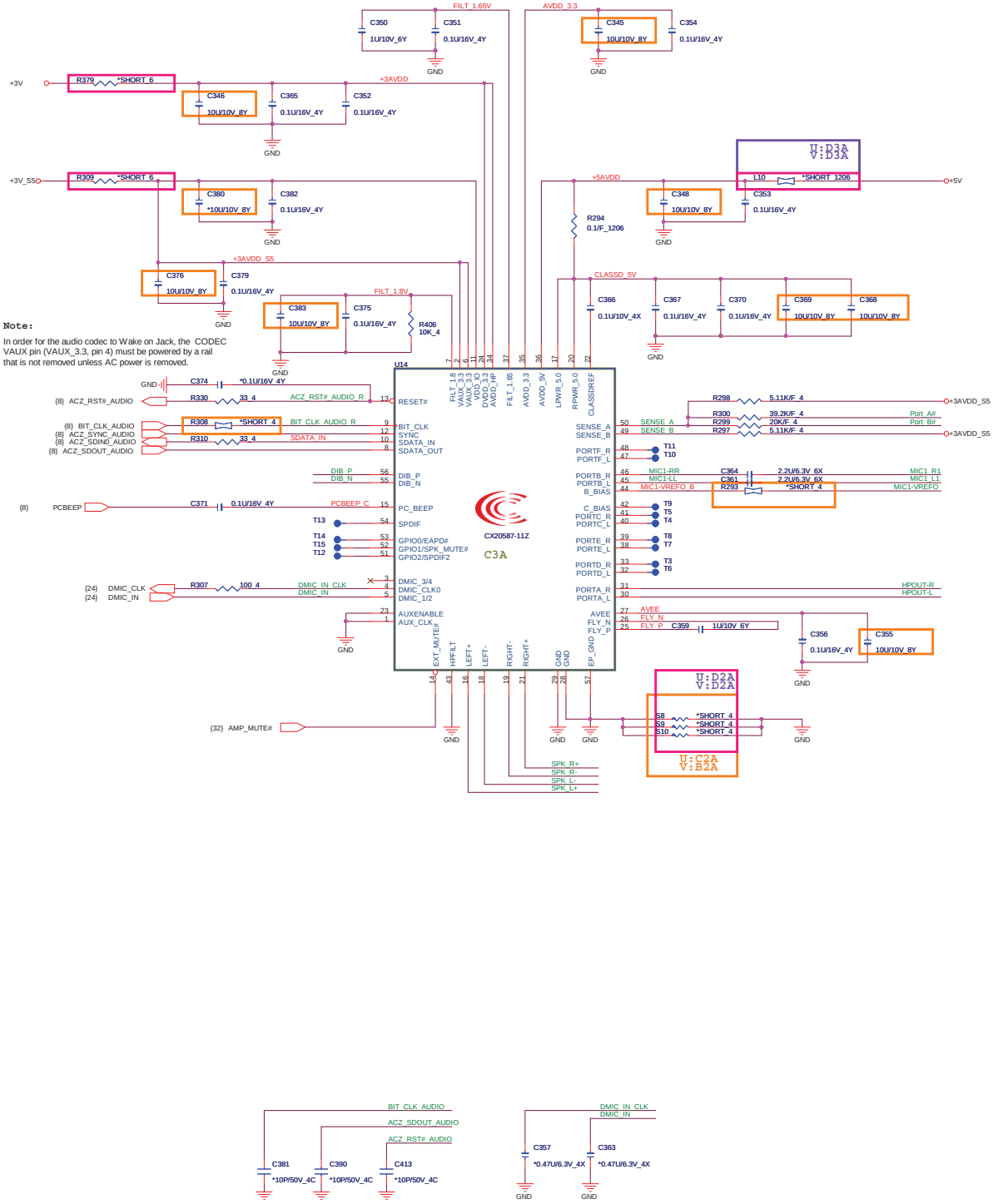
Quanta Computer Inc.

PROJECT : TE5

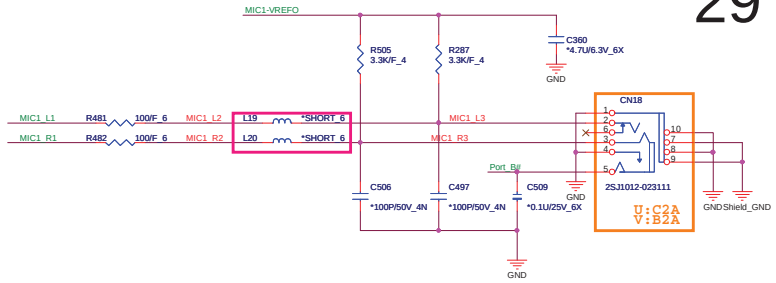
Size	Document Number	Rev
	HDD/ODD/MDC	1A

Date: Wednesday, January 05, 2011 Sheet 28 of 44

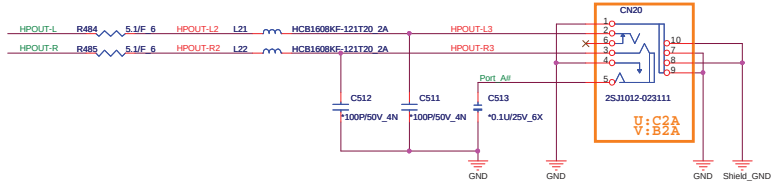
Codec(CX20587-11Z) <ADO/MDC/SLM>



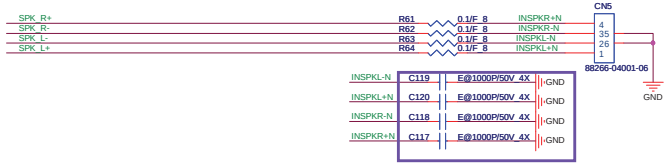
EXT MIC <ADO/SLM>



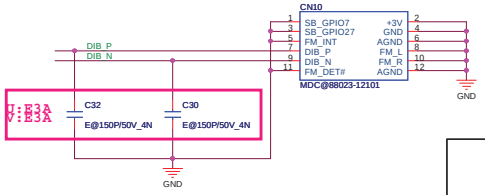
EXT H.P / Beats <ADO/AMP>



INT SPK <ADO>



MDC <MDC>



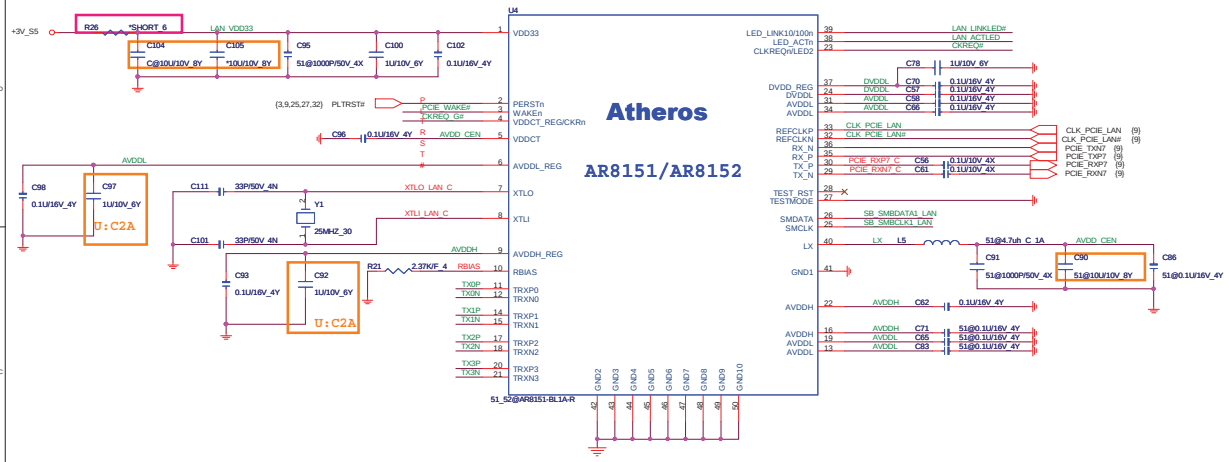
Quanta Computer Inc.

PROJECT : TE5

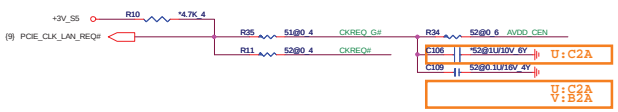
Size	Document Number	Rev
	Codec (CX20587)	1A

Date: Wednesday, January 05, 2011 Sheet 29 of 44

Atheros Lan <LAN/LN1/LNG>



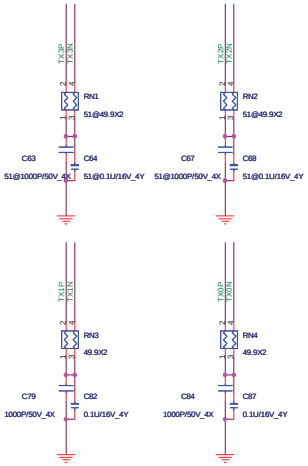
LAN-Wake up function <LAN>



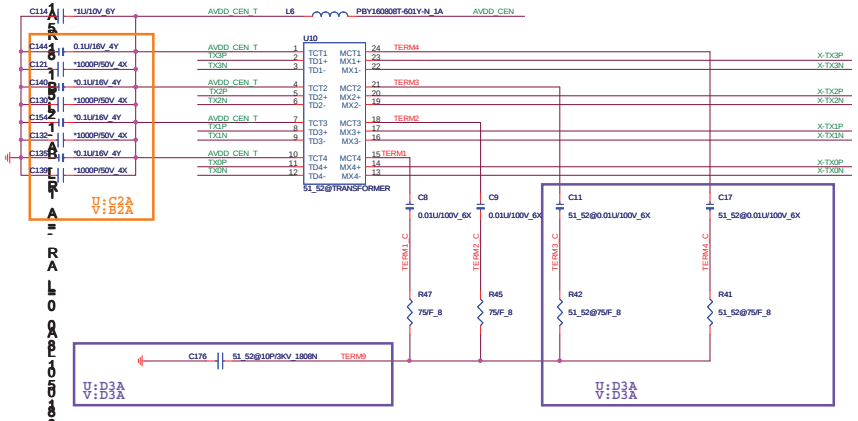
LAN-SM-Bus <LAN>

LAN-terminator <LAN/LN1/LNG>

PLACE NEAR LAN IC SIDE



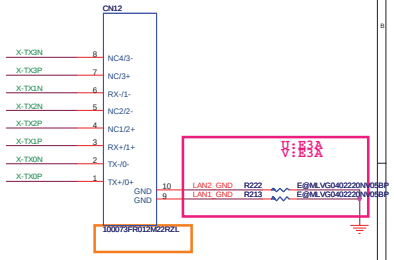
LAN-Transformer <LAN/LN1/LNG>



LAN-Strap function <LAN/LN1/LNG>

LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

LAN(RJ45)-CONN Interface <LAN>



GIGA-LAN-RTL8111E-CG
REV 1.0
2009/05/18

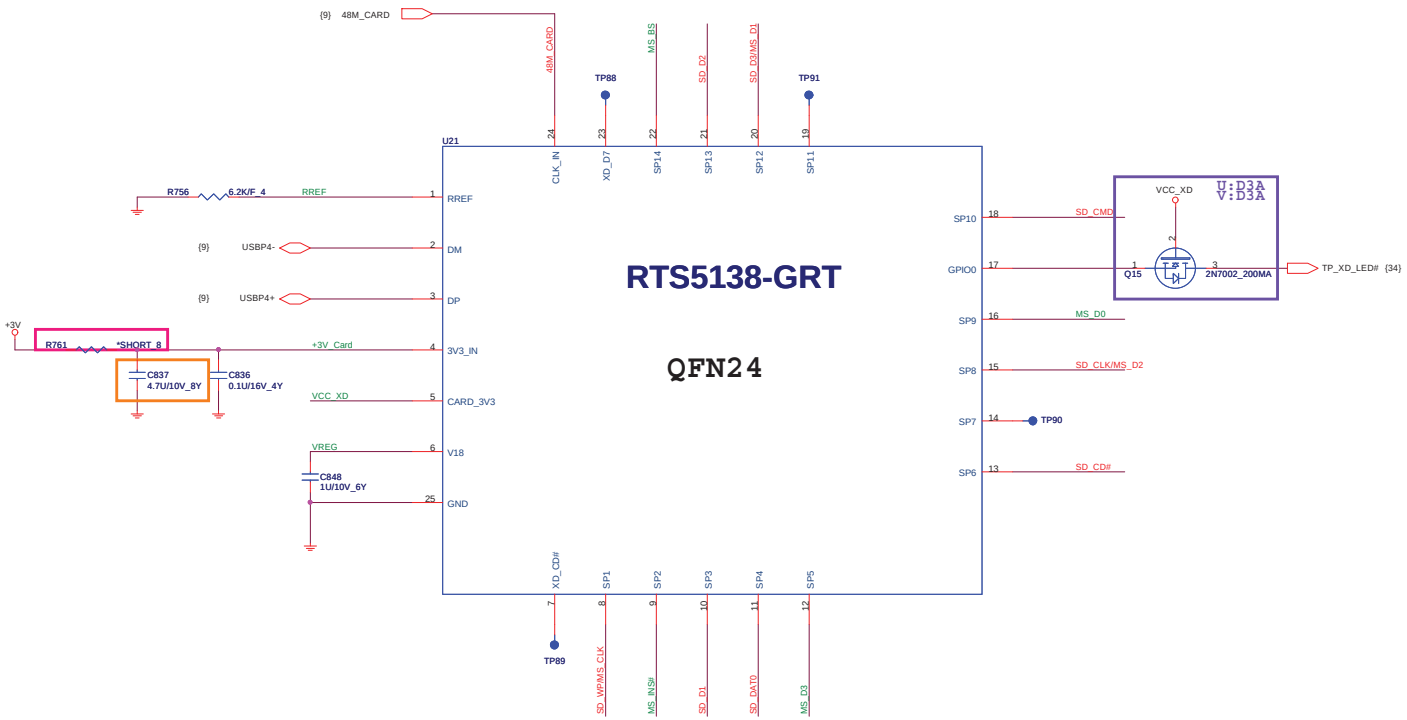
Quanta Computer Inc.
PROJECT : TE5

Size	Document Number	Rev
	Atheros Lan	1A

Date: Wednesday, January 05, 2011 Sheet 30 of 44

3 IN 1 CARD READER

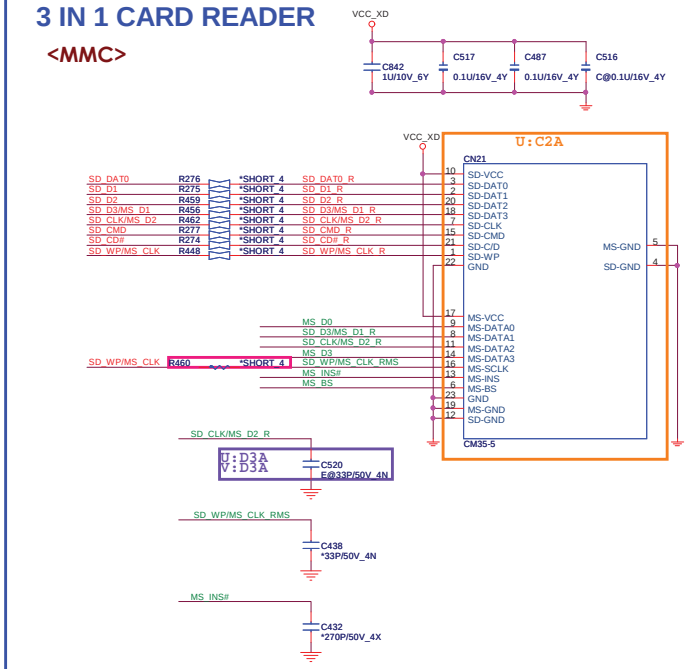
Card reader controller <MMC>



3 IN 1 CARD READER

<MMC>

31



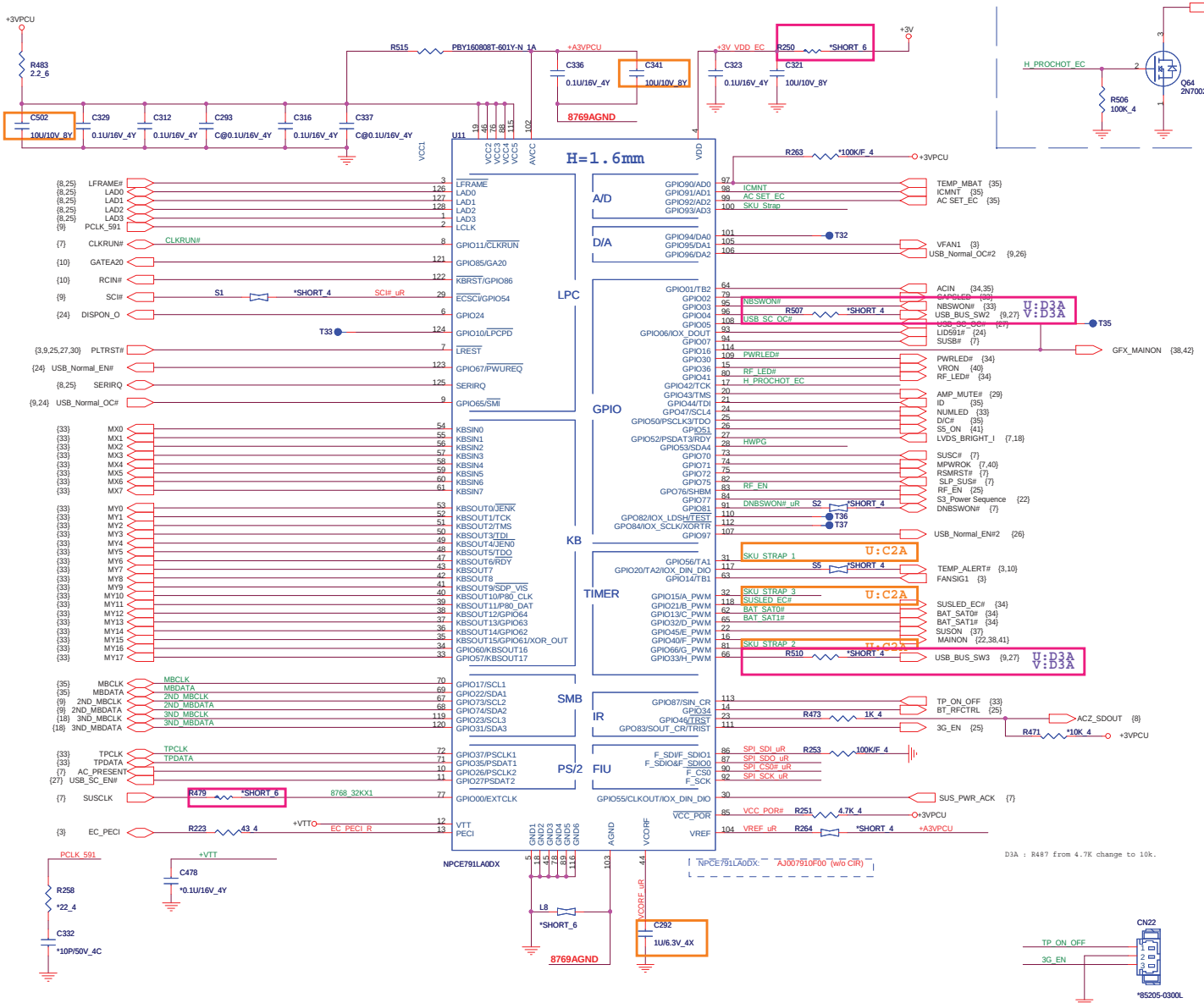
Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Rev
	RTS5138 (Card Reader)	1A

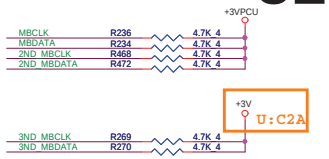
Date: Wednesday, January 05, 2011 Sheet 31 of 44

EC [KBC]



Intel Turbo mode only<CPU>

SM BUS PU/Address <KBC>

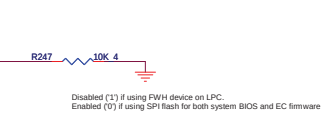


3Cell Battery protect & K/B LED Control <KBC>

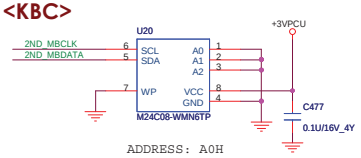
SKU_Strap — KB_LED {33}

TP <KBC>

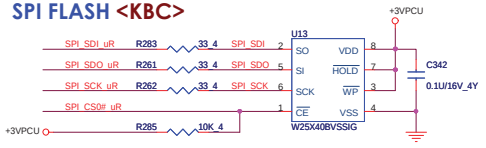
Strap <KBC>



ID EEPROM <KBC>



SPI FLASH <KBC>

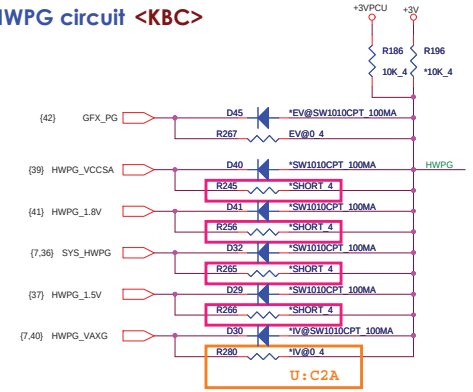


Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

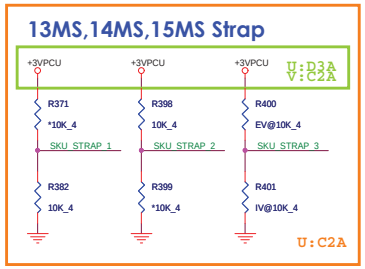
INTERNAL KEYBOARD STRIP SET <KBC>

MY0 R214 10K_4 +3VPCU

HWPG circuit <KBC>

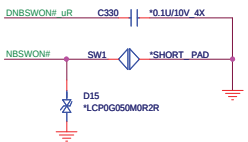


13MS,14MS,15MS Strap

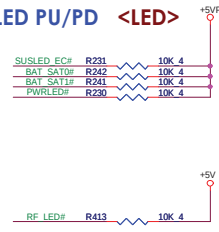


MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3
13" UMA	0	0	0
13" DIS	0	0	1
14" UMA	0	1	0
14" DIS	0	1	1
15" UMA	1	0	0
15" DIS	1	0	1

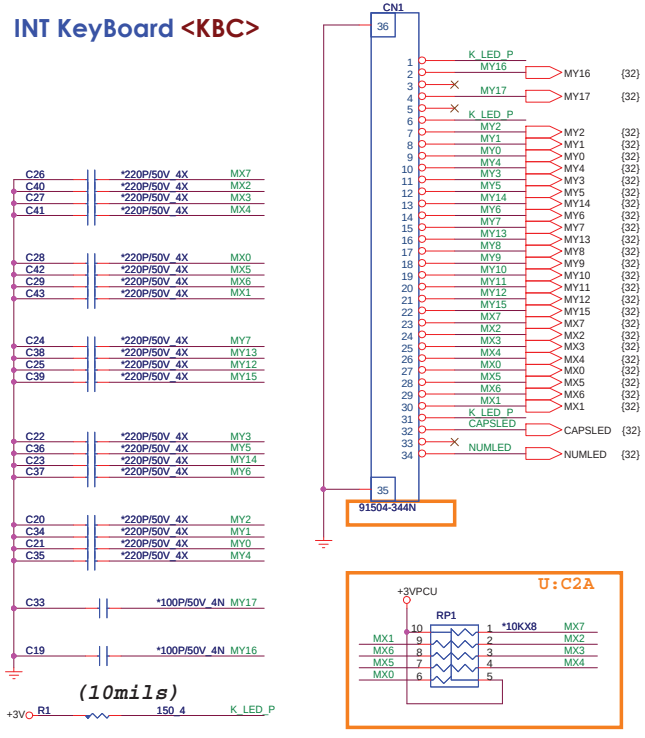
Power Button<KBC>



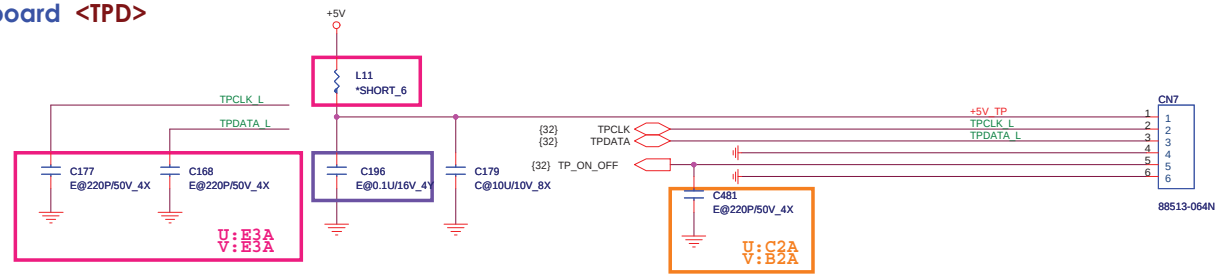
LED PU/PD <LED>



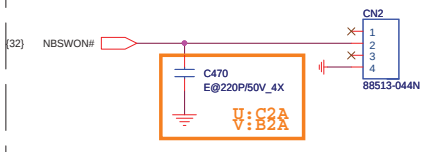
INT KeyBoard <KBC>



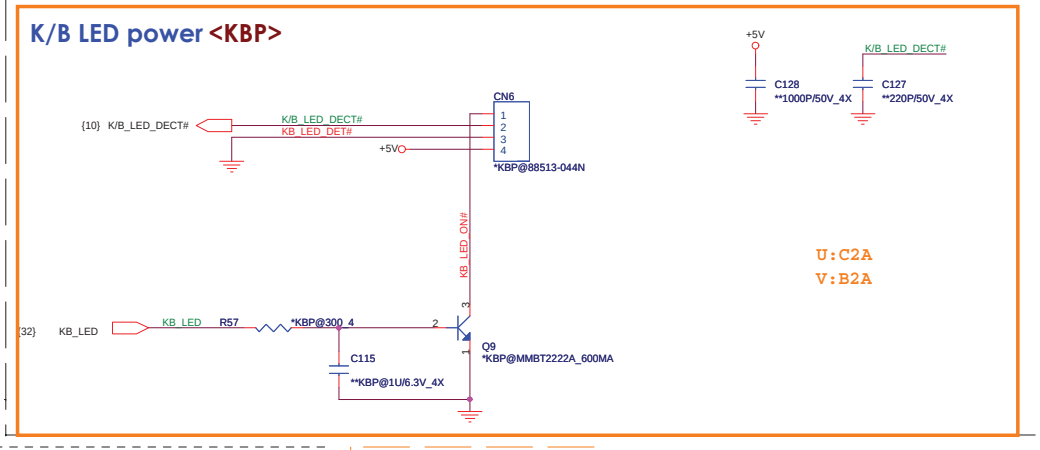
TP board <TPD>



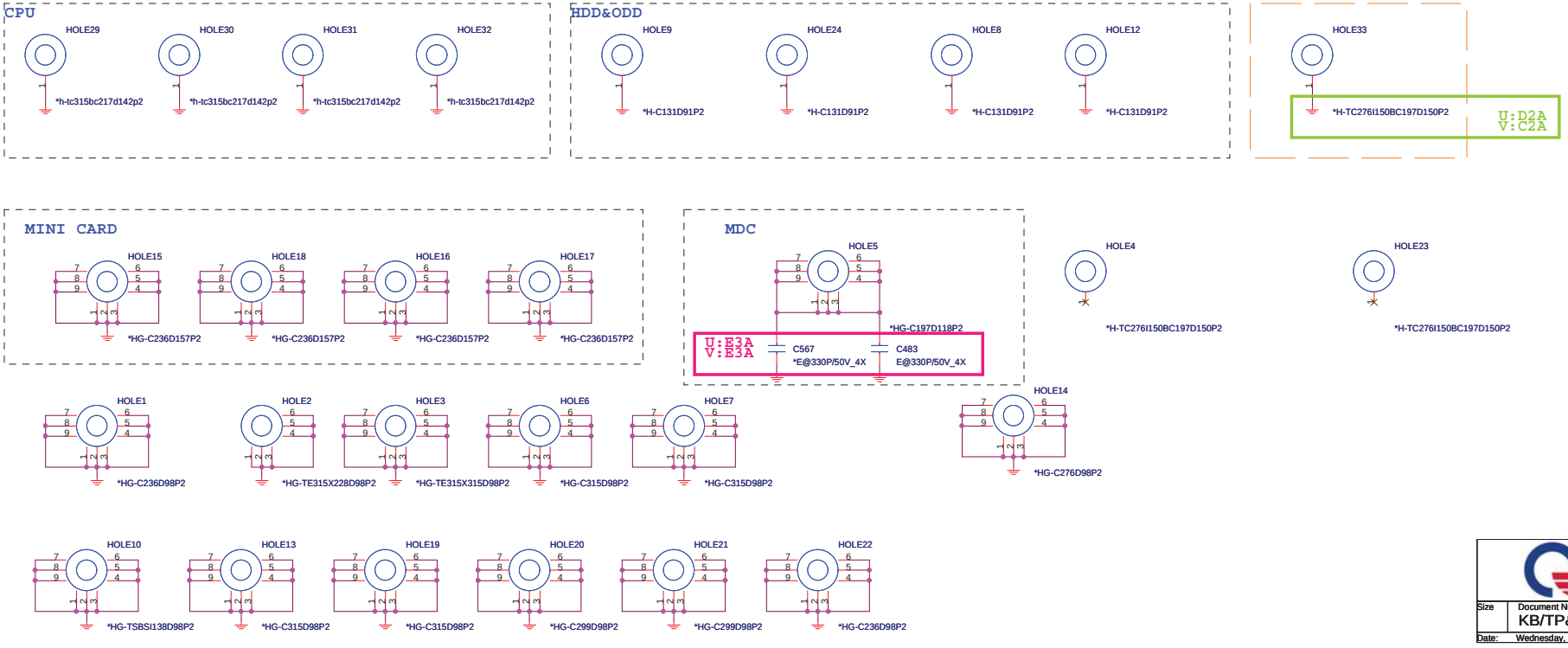
Power board <PSW>



K/B LED power <KBP>



HOLE



Quanta Computer Inc.

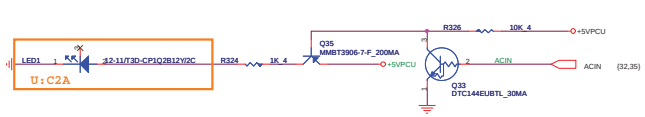
PROJECT : TE5

Size	Document Number	Rev
	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	1A

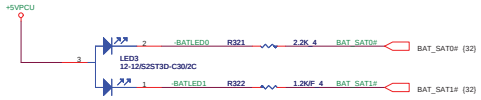
Date: Wednesday, January 05, 2011 Sheet 33 of 44

LED <LED>

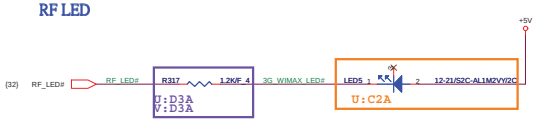
AC-IN



BATERRY

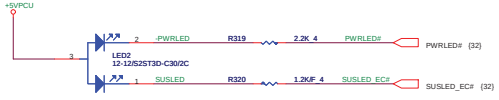


RF LED

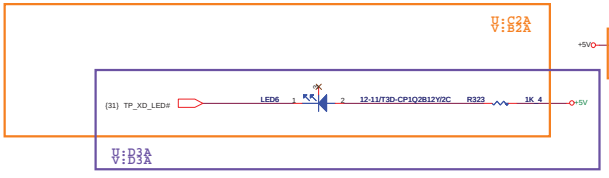


HDD/ODD

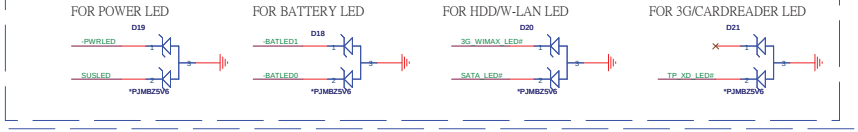
POWER



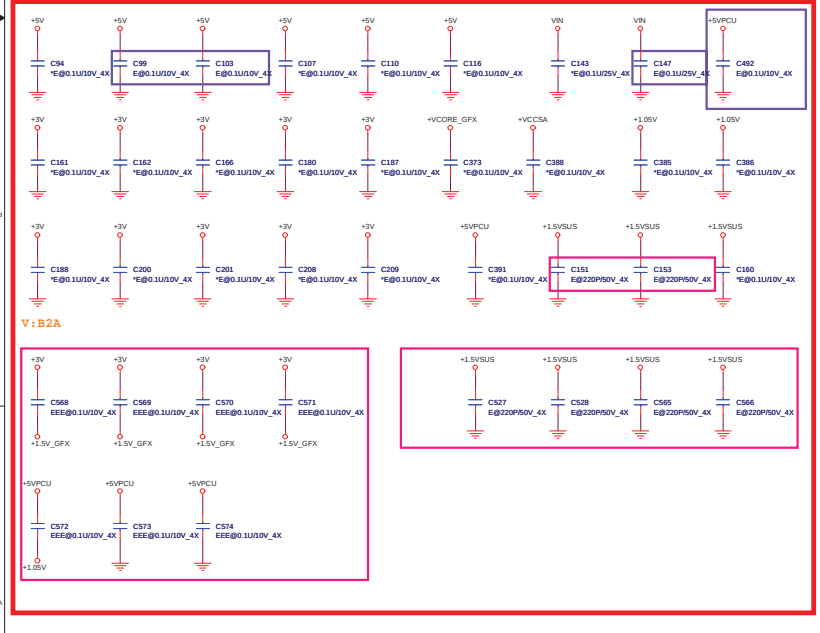
CARDREADER



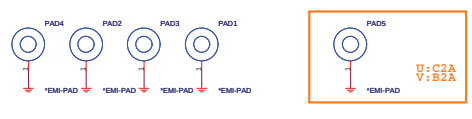
ESD Protect



EMI



EMI PAD

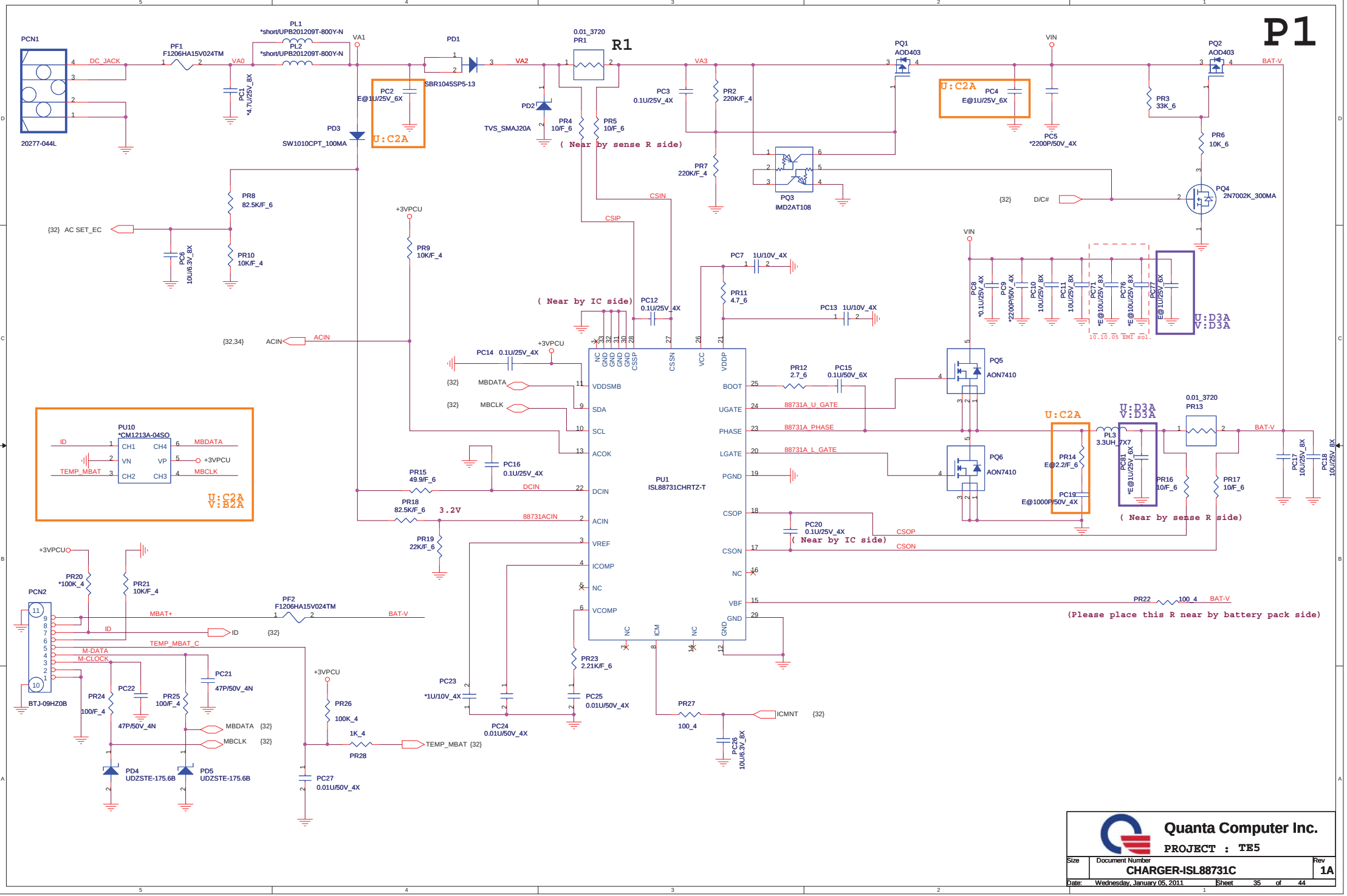


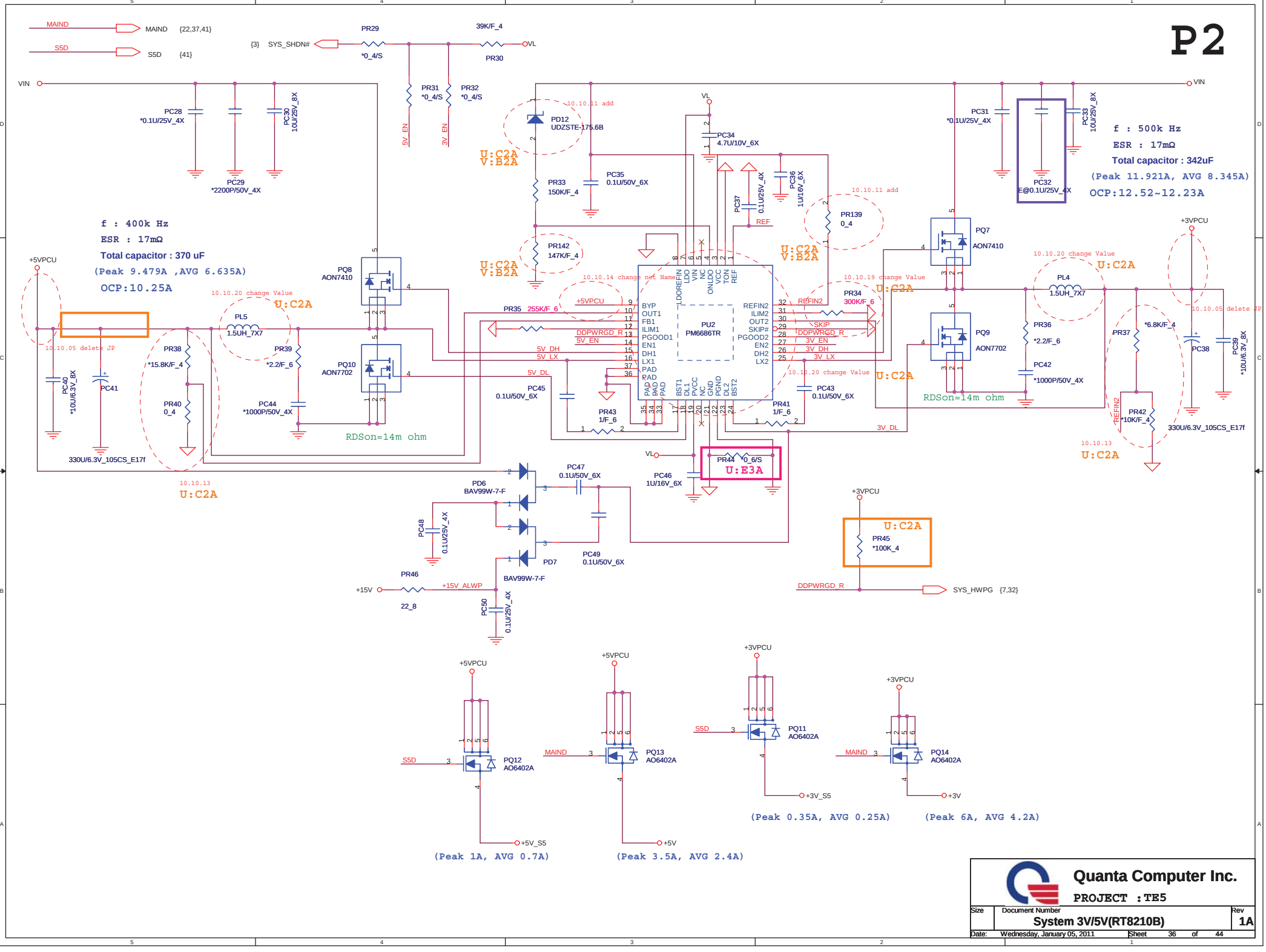
Quanta Computer Inc.

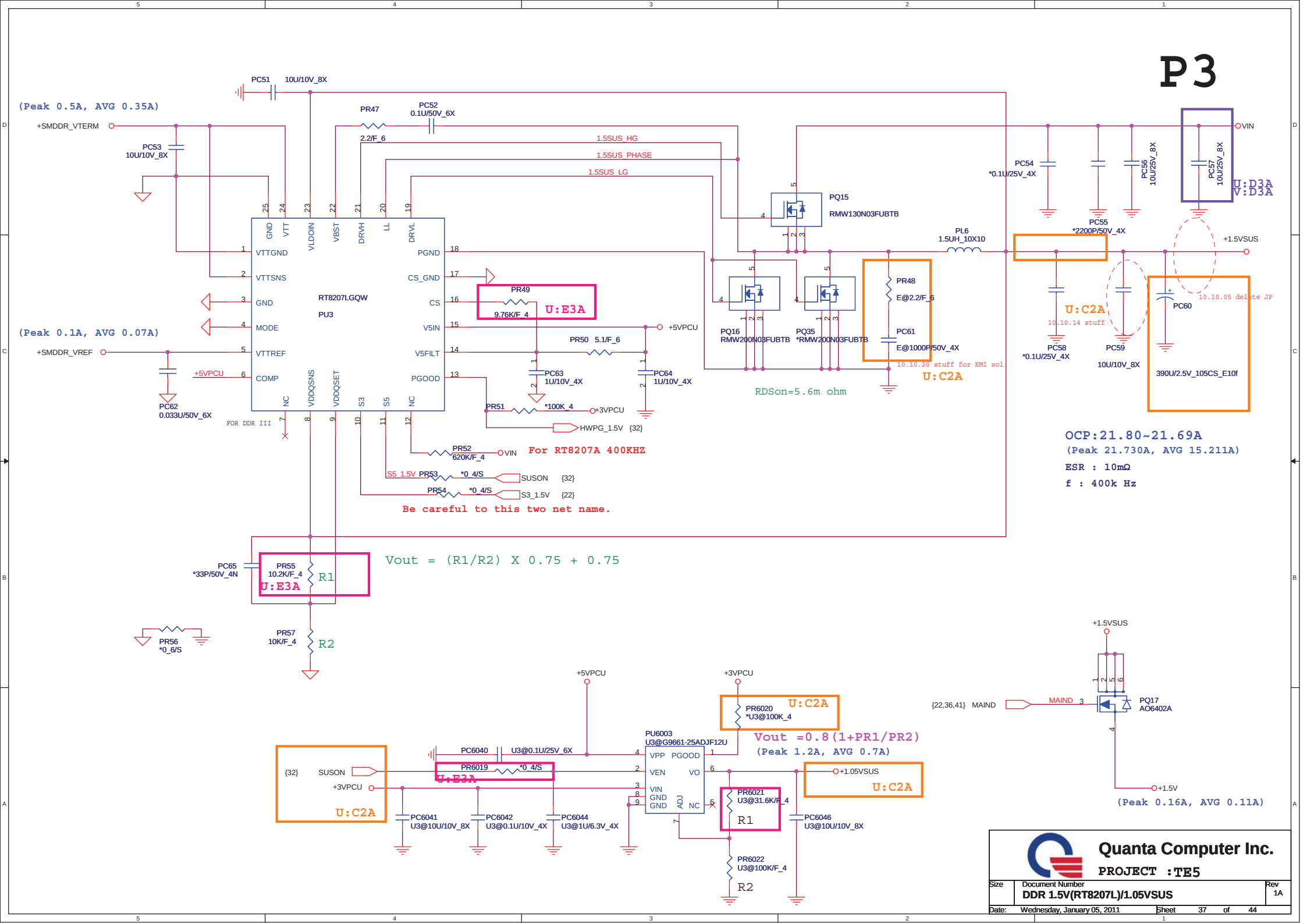
PROJECT : TE5

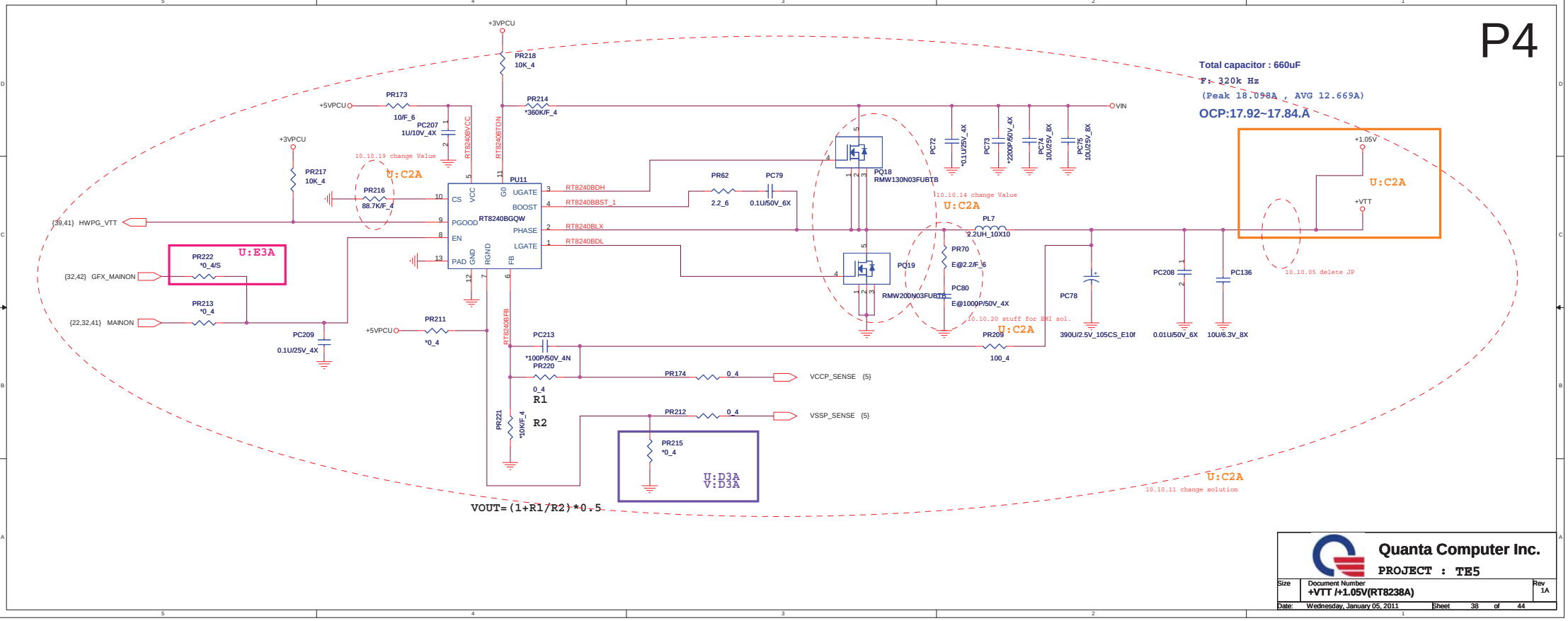
Size	Document Number	Rev
	LED/HOLE	1A

Date: Wednesday, January 05, 2011 Sheet 34 of 44


P1
PCN1
20277-044L
DC_JACK
PF1
F1206HA15V024TM
VA0
PC1
*4.7U/25V_8X
PL1
*short/UPB201209T-800Y-N
PL2
*short/UPB201209T-800Y-N
VA1
PD1
SBR1045SP5-13
VA2
PC2
E@1U/25V_6X
U:C2A
PD3
SW1010CPT_100MA
PD2
TVS_SMAJ20A
0.01_3720
PR1
R1
PR4
10/F_6
PR5
10/F_6
(Near by sense R side)
VA3
PC3
0.1U/25V_4X
PR2
220K/F_4
PR7
220K/F_4
PQ1
AOD403
PQ3
IMD2AT108
VIN
PC4
E@1U/25V_6X
PC5
*2200P/50V_4X
PQ2
AOD403
BAT-V
PR3
33K_6
PR6
10K_6
PQ4
2N7002K_300MA
{32} D/C#
CSIN
CSIP
PR8
82.5K/F_6
{32} AC SET_EC
PC6
10U/6.3V_8X
PR10
10K/F_4
+3VPCU
PR9
10K/F_4
PC7 1U/10V_4X
PR11
4.7_6
PC12
0.1U/25V_4X
(Near by IC side)
PC13 1U/10V_4X
PC8
*0.1U/25V_4X
PC9
*2200P/50V_4X
PC10
10U/25V_8X
PC11
10U/25V_8X
PC71
*E@10U/25V_8X
PC76
*E@10U/25V_8X
PC77
E@1U/25V_6X
10.10.05 EMI sol.
U:D3A
V:D3A
{32,34} ACIN
PC14 0.1U/25V_4X
{32} MBDATA
{32} MBCLK
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
NC
ICM
NC
GND
PU1
ISL88731CHRTZ-T
PR12
2.7_6
PC15
0.1U/50V_6X
88731A_U_GATE
88731A_PHASE
88731A_L_GATE
PQ5
AON7410
PQ6
AON7410
PU10
*CM1213A-04SO
CH1
CH4
VN
VP
CH2
CH3
ID
TEMP_MBAT
MBDATA
+3VPCU
MBCLK
U:C2A
V:B2A
PC16
0.1U/25V_4X
PR15
49.9/F_6
DCIN
PR18
82.5K/F_6
3.2V
88731ACIN
PR19
22K/F_6
PC20
0.1U/25V_4X
(Near by IC side)
CSOP
CSON
U:C2A
PR14
E@2.2/F_6
PC19
E@1000P/50V_4X
PL3
3.3UH_7X7
U:D3A
V:D3A
PC81
*E@10U/25V_6X
PR16
10/F_6
0.01_3720
PR13
PR17
10/F_6
(Near by sense R side)
PC17
10U/25V_8X
PC18
10U/25V_8X
PR22
100_4
BAT-V
(Please place this R near by battery pack side)
+3VPCU
PR20
*100K_4
PR21
10K/F_4
PCN2
BTJ-09HZ0B
MBAT+
PF2
F1206HA15V024TM
BAT-V
ID
{32}
TEMP_MBAT_C
M-DATA
M-CLOCK
PC21
47P/50V_4N
PR24
100/F_4
PC22
47P/50V_4N
PR25
100/F_4
MBDATA {32}
MBCLK {32}
PD4
UDZSTE-175.6B
PD5
UDZSTE-175.6B
+3VPCU
PR26
100K_4
1K_4
PR28
TEMP_MBAT {32}
PC27
0.01U/50V_4X
PC23
*1U/10V_4X
PC24
0.01U/50V_4X
PR23
2.21K/F_6
PC25
0.01U/50V_4X
PR27
100_4
ICMNT {32}
PC26
10U/6.3V_8X
Quanta Computer Inc.
PROJECT : TE5
Size
Document Number
CHARGER-ISL88731C
Rev
1A
Date: Wednesday, January 05, 2011
Sheet 35 of 44


P2
MAIND {22,37,41}
S5D {41}
{3} SYS_SHDN#
PR29 *0_4/S
39K/F_4 PR30
VL
VIN
PR31 *0_4/S
PR32 *0_4/S
5V_EN
3V_EN
PC28 *0.1U/25V_4X
PC29 *2200P/50V_4X
PC30 10U/25V_8X
10.10.11 add
PD12 UDZSTE-175.6B
U:C2A V:B2A
PR33 150K/F_4
PC35 0.1U/50V_6X
PC34 4.7U/10V_6X
PC37 0.1U/25V_4X
PC36 1U/16V_6X
REF
PR139 0_4
PR142 147K/F_4
PC31 *0.1U/25V_4X
PC32 E@0.1U/25V_4X
PC33 10U/25V_8X
f : 500k Hz
ESR : 17mΩ
Total capacitor : 342uF
(Peak 11.921A, AVG 8.345A)
OCP:12.52~12.23A
f : 400k Hz
ESR : 17mΩ
Total capacitor : 370 uF
(Peak 9.479A ,AVG 6.635A)
OCP:10.25A
+5VPCU
10.10.20 change Value
PL5 1.5UH_7X7
PR38 *15.8K/F_4
PR39 *2.2/F_6
PR40 0_4
PC40 *10U/6.3V_8X
PC41 330U/6.3V_105CS_E17f
PC44 *1000P/50V_4X
PQ8 AON7410
PQ10 AON7702
RDSon=14m ohm
10.10.05 delete JP
10.10.14 change net Name
PU2 PM6686TR
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD
LDOREFIN LDO VIN NC ONLDO VCC TON REF
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND PGND DL2 BST2
PR35 255K/F_6
DDPWRGD_R
5V_EN
5V_DH
5V_LX
5V_DL
PC45 0.1U/50V_6X
PR43 1/F_6
PR41 1/F_6
PR34 300K/F_6
REFIN2
SKIP
3V_EN
3V_DH
3V_LX
3V_DL
10.10.19 change Value
PC43 0.1U/50V_6X
PQ7 AON7410
PQ9 AON7702
PR36 *2.2/F_6
PC42 *1000P/50V_4X
PL4 1.5UH_7X7
+3VPCU
PR37 *6.8K/F_4
PC38 330U/6.3V_105CS_E17f
PC39 *10U/6.3V_8X
PR42 *10K/F_4
10.10.13
PR44 *0_6/S
PC46 1U/16V_6X
PC47 0.1U/50V_6X
PD6 BAV99W-7-F
PC48 0.1U/25V_4X
PC49 0.1U/50V_6X
PD7 BAV99W-7-F
PR46 22_8
+15V
+15V_ALWP
PC50 0.1U/25V_4X
PR45 *100K_4
SYS_HWPG {7,32}
PQ12 AO6402A
PQ13 AO6402A
PQ11 AO6402A
PQ14 AO6402A
+5V_S5
+5V
+3V_S5
+3V
(Peak 1A, AVG 0.7A)
(Peak 3.5A, AVG 2.4A)
(Peak 0.35A, AVG 0.25A)
(Peak 6A, AVG 4.2A)
Quanta Computer Inc.
PROJECT : TE5
Size
Document Number
System 3V/5V(RT8210B)
Rev
1A
Date: Wednesday, January 05, 2011
Sheet 36 of 44


P3
(Peak 0.5A, AVG 0.35A)
+SMDDR_VTERM
PC51 10U/10V_8X
PC53 10U/10V_8X
PR47 2.2/F_6
PC52 0.1U/50V_6X
1.5SUS_HG
1.5SUS_PHASE
1.5SUS_LG
RT8207LGQW
PU3
GND VTT VLDOIN VBST DRVH LL DRVL
VTTGND VTTSNS GND MODE VTTREF COMP
PGND CS_GND CS V5IN V5FILT PGOOD
NC VDDQSNS VDDQSET S3 S5 NC
FOR DDR III
(Peak 0.1A, AVG 0.07A)
+SMDDR_VREF
+5VPCU
PC62 0.033U/50V_6X
PR49 9.76K/F_4
U:E3A
PR50 5.1/F_6
+5VPCU
PC63 1U/10V_4X
PC64 1U/10V_4X
PR51 *100K_4
+3VPCU
HWPG_1.5V {32}
PR52 620K/F_4
VIN
For RT8207A 400KHZ
S5_1.5V PR53 *0_4/S
SUSON {32}
PR54 *0_4/S
S3_1.5V {22}
Be careful to this two net name.
PQ15 RMW130N03FUBTB
PQ16 RMW200N03FUBTB
PQ35 *RMW200N03FUBTB
RDSon=5.6m ohm
PR48 E@2.2/F_6
PC61 E@1000P/50V_4X
10.10.20 stuff for EMI sol
U:C2A
PL6 1.5UH_10X10
PC54 *0.1U/25V_4X
PC55 *2200P/50V_4X
PC56 10U/25V_8X
PC57 10U/25V_8X
U:D3A
V:D3A
VIN
+1.5VSUS
U:C2A
10.10.14 stuff
PC58 *0.1U/25V_4X
PC59 10U/10V_8X
PC60
10.10.05 delete JP
390U/2.5V_105CS_E10f
OCP:21.80~21.69A
(Peak 21.730A, AVG 15.211A)
ESR : 10mΩ
f : 400k Hz
PC65 *33P/50V_4N
PR55 10.2K/F_4
R1
U:E3A
Vout = (R1/R2) X 0.75 + 0.75
PR56 *0_6/S
PR57 10K/F_4
R2
+5VPCU
+3VPCU
PR6020 *U3@100K_4
U:C2A
Vout =0.8(1+PR1/PR2)
(Peak 1.2A, AVG 0.7A)
PU6003
U3@G9661-25ADJF12U
VPP PGOOD
VEN VO
VIN
GND
GND ADJ NC
PC6040 U3@0.1U/25V_6X
PR6019 *0_4/S
U:E3A
{32} SUSON
+3VPCU
U:C2A
PC6041 U3@10U/10V_8X
PC6042 U3@0.1U/10V_4X
PC6044 U3@1U/6.3V_4X
+1.05VSUS
U:C2A
PR6021 U3@31.6K/F_4
R1
PC6046 U3@10U/10V_8X
PR6022 U3@100K/F_4
R2
+1.5VSUS
{22,36,41} MAIND
MAIND
PQ17 AO6402A
+1.5V
(Peak 0.16A, AVG 0.11A)
Quanta Computer Inc.
PROJECT :TE5
Size
Document Number
DDR 1.5V(RT8207L)/1.05VSUS
Rev 1A
Date: Wednesday, January 05, 2011
Sheet 37 of 44

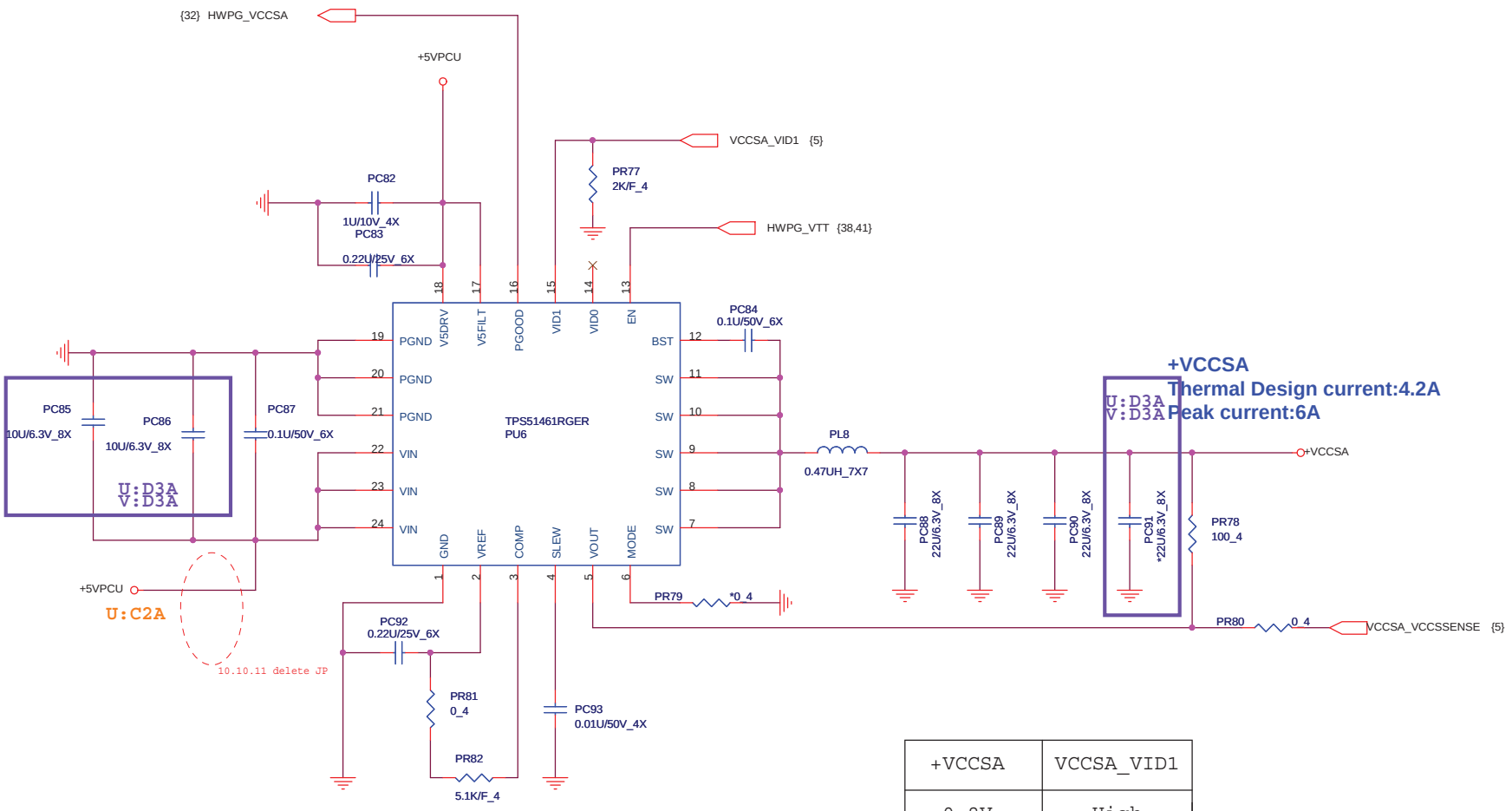


Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Rev
	+VTT /+1.05V(RT8238A)	1A

Date: Wednesday, January 05, 2011 Sheet 38 of 44



+VCCSA	VCCSA_VID1
0.8V	High
0.9V	Low

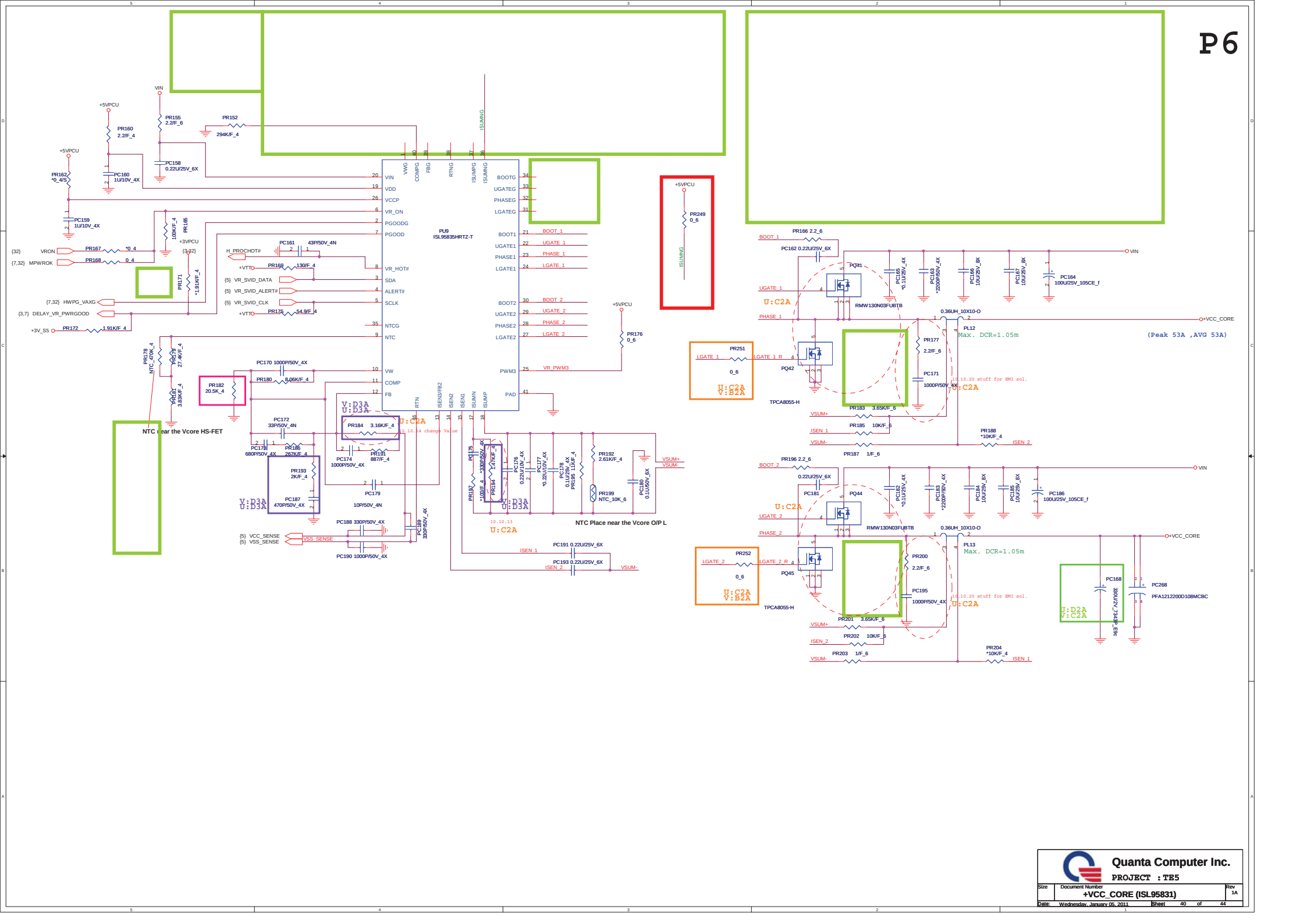
U:C2A

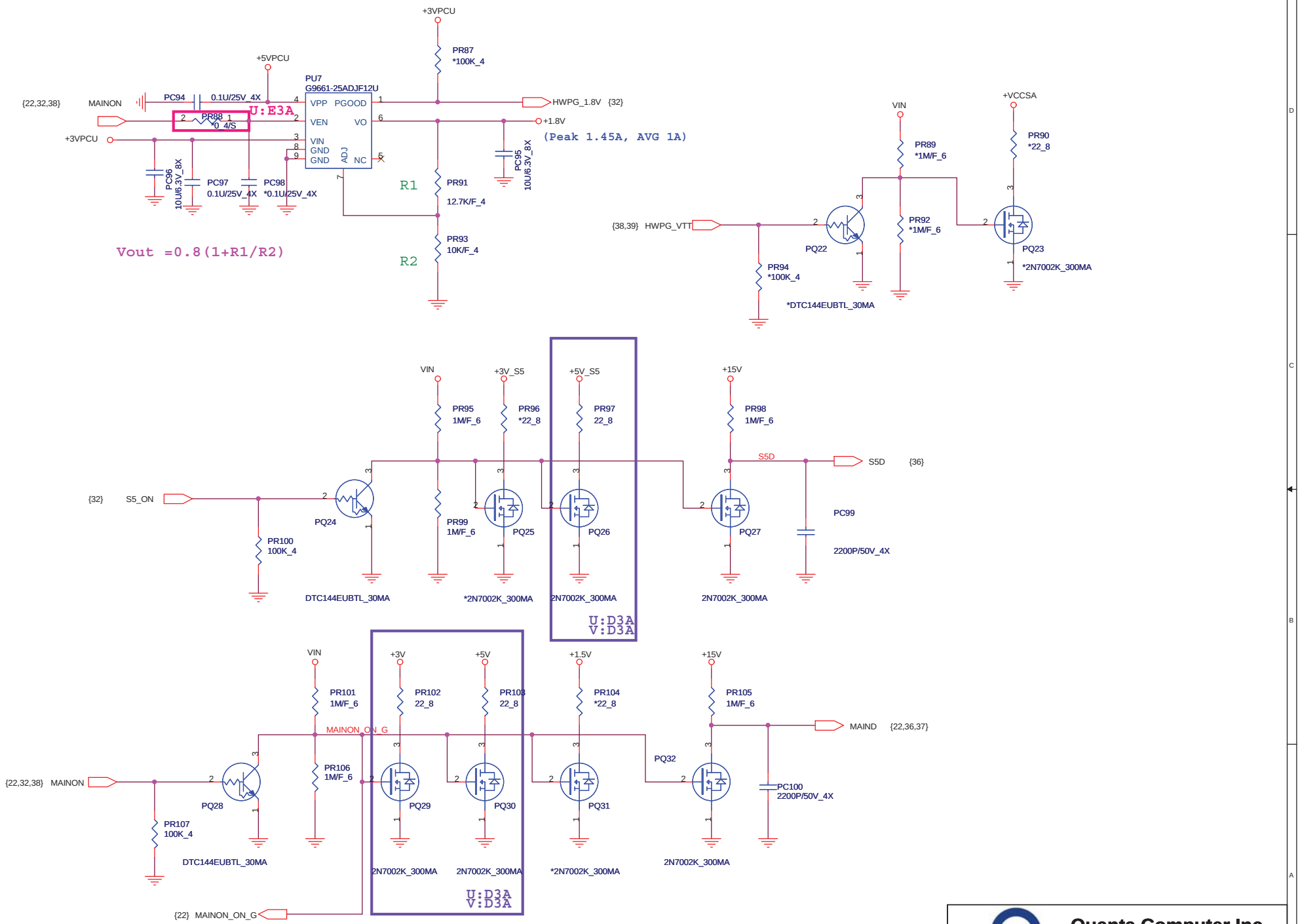
Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Rev
	+VCCSA ISL95870A)	1A

Date: Wednesday, January 05, 2011 Sheet 39 of 44


P6
PU9
ISL95835HRTZ-T
VIN
VDD
VCCP
VR_ON
PGOODG
PGOOD
VR_HOT#
SDA
ALERT#
SCLK
NTCG
NTC
VW
COMP
FB
VVG
COMPG
FBG
RTNG
ISUMPG
ISUMNG
BOOTG
UGATEG
PHASEG
LGATEG
BOOT1
UGATE1
PHASE1
LGATE1
BOOT2
UGATE2
PHASE2
LGATE2
PWM3
PAD
RTN
ISEN3/FB2
ISEN2
ISEN1
ISUMN
ISUMP
+5VPCU
+3VPCU
+3V_S5
VRON
MPWROK
HWPG_VAXG
DELAY_VR_PWRGOOD
H_PROCHOT#
VR_SVID_DATA
VR_SVID_ALERT#
VR_SVID_CLK
+VTT
VR_PWM3
VCC_SENSE
VSS_SENSE
VSUM+
VSUM-
ISEN_1
ISEN_2
NTC Near the Vcore HS-FET
NTC Place near the Vcore O/P L
PR155 2.2/F_6
PR152 294K/F_4
PR160 2.2/F_4
PR162 *0_4/S
PC158 0.22U/25V_6X
PC160 1U/10V_4X
PC159 1U/10V_4X
PR165 100K/F_4
PR171 *1.91K/F_4
PR167 *0_4
PR168 0_4
PR172 1.91K/F_4
PC161 43P/50V_4N
PR169 130/F_4
PR175 54.9/F_4
PR176 0_6
PR249 0_6
PR178 NTC_470K_4
PR179 27.4K/F_4
PR181 3.83K/F_4
PR182 20.5K_4
PC170 1000P/50V_4X
PR180 8.06K/F_4
PC172 33P/50V_4N
PC178 680P/50V_4X
PR186 267K/F_4
PR184 3.16K/F_4
PC174 1000P/50V_4X
PR191 887/F_4
PC179 10P/50V_4N
PR193 2K/F_4
PC187 470P/50V_4X
PC188 330P/50V_4X
PC189 330P/50V_4X
PC190 1000P/50V_4X
PC175 *330P/50V_4X
PR194 *1.47K/F_4
PR197 *100/F_4
PC176 0.22U/10V_4X
PC177 *0.22U/10V_4X
PC178 0.1U/25V_4X
PR195 11K/F_4
PR192 2.61K/F_4
PR199 NTC_10K_6
PC180 0.1U/50V_6X
PC191 0.22U/25V_6X
PC193 0.22U/25V_6X
PR166 2.2_6
PC162 0.22U/25V_6X
PC165 *0.1U/25V_4X
PC163 *220P/50V_4X
PC166 10U/25V_8X
PC167 10U/25V_8X
PC164 100U/25V_105CE_f
PQ41
RMW130N03FUBTB
PQ42
TPCA8055-H
PR251 0_6
PR177 2.2/F_6
PC171 1000P/50V_4X
PL12 0.36UH_10X10-O
Max. DCR=1.05m
(Peak 53A ,AVG 53A)
PR183 3.65K/F_6
PR185 10K/F_6
PR187 1/F_6
PR188 *10K/F_4
PR196 2.2_6
PC181 0.22U/25V_6X
PC182 *0.1U/25V_4X
PC183 *220P/50V_4X
PC184 10U/25V_8X
PC185 10U/25V_8X
PC186 100U/25V_105CE_f
PQ44
PQ45
PR252 0_6
PR200 2.2/F_6
PC195 1000P/50V_4X
PL13 0.36UH_10X10-O
Max. DCR=1.05m
PR201 3.65K/F_6
PR202 10K/F_6
PR203 1/F_6
PR204 *10K/F_4
PC168 330U/2V_7343P_EEK
PC268
PFA1212200D108MCBC
U:C2A
V:C2A
U:B2A
V:B2A
U:D2A
V:D2A
V:D3A
U:D3A
10.10.14 change Value
10.10.13
10.10.20 stuff for EMI sol.
Quanta Computer Inc.
PROJECT : TE5
Size
Document Number
+VCC_CORE (ISL95831)
Rev
1A
Date: Wednesday, January 05, 2011
Sheet 40 of 44



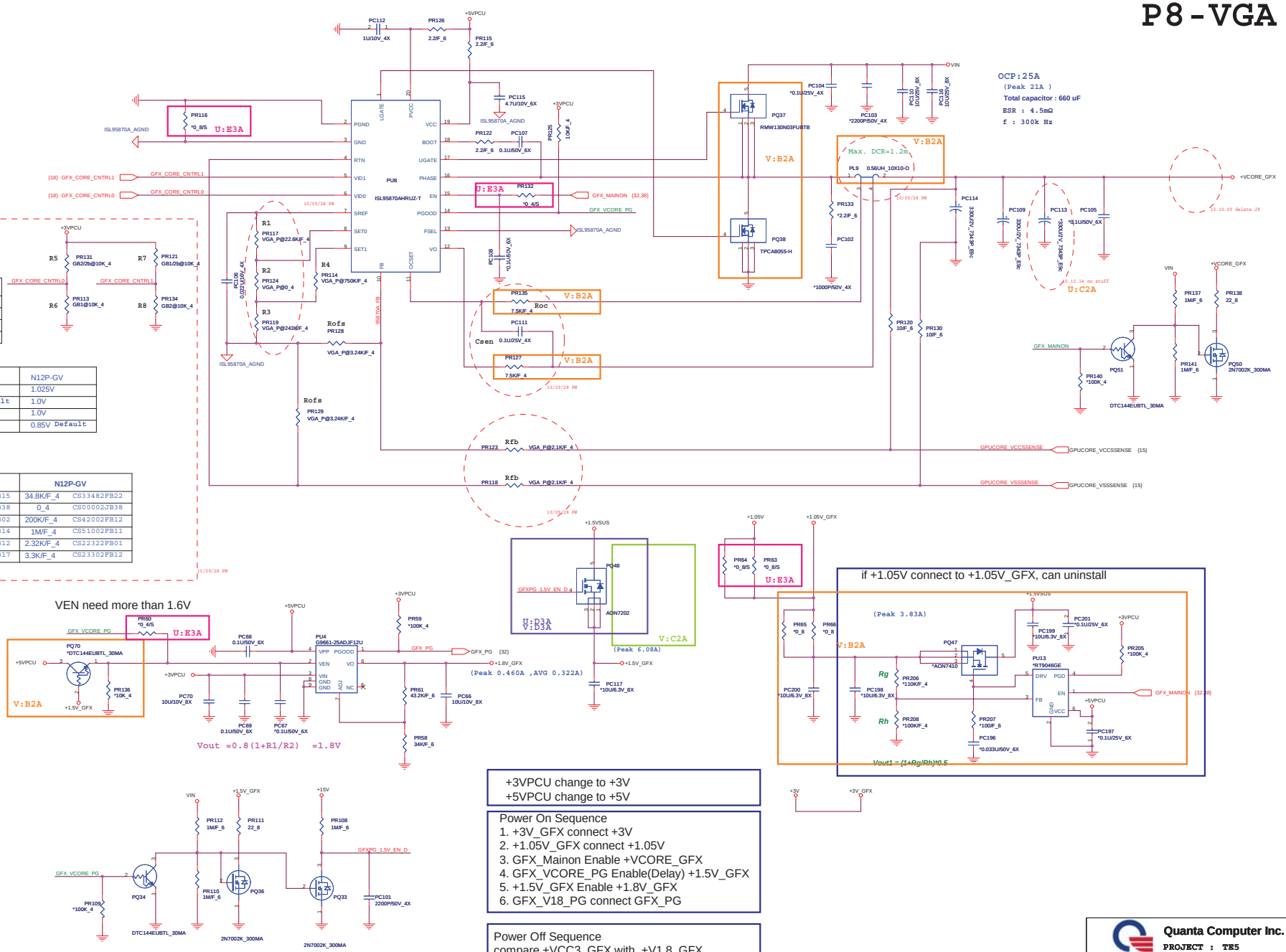
Quanta Computer Inc.

PROJECT :TE5

Size	Document Number	Rev
	Discharge	1A

Date: Wednesday, January 05, 2011 Sheet 41 of 44

P8-VGA



Need to consider DOS mode

Default		N12M-GE	N12P-LP	N12P-GV
PR131	R5	NC	10K CS31002JB28	10K CS31002JB28
PR113	R6	10K CS31002JB28	NC	NC
PR121	R7	10K CS31002JB28	NC	10K CS31002JB28
PR134	R8	NC	10K CS31002JB28	NC

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	N12M-GE	N12P-LP	N12P-GV
LOW	LOW	1.0V	0.925V	1.025V
LOW	HIGH	1.0V	0.90V Default	1.0V
HIGH	LOW	1.0V Default	0.9V	1.0V
HIGH	HIGH	0.85V	0.825V	0.85V Default

		N12M-GE		N12P-LP		N12P-GV	
R1	PR117	47.5K/F_4	CS34752FB14	22.6K/F_4	CS32262FB15	34.8K/F_4	CS3482FB22
R2	PR124	0_4	CS00002JB38	0_4	CS00002JB38	0_4	CS00002JB38
R3	PR119	270K/F_4	CS42702JB10	243K/F_4	CS42432FB02	200K/F_4	CS42002FB12
R4	PR114	1M/F_4	CS51002FB11	750K/F_4	CS47502FB14	1M/F_4	CS51002FB11
Rfb	PR118,PR123	2.32K/F_4	CS22322FB01	2.10K/F_4	CS22102FB12	2.32K/F_4	CS22322FB01
Rofs	PR128,PR129	3.3K/F_4	CS23302FB12	3.24K/F_4	CS23242FB17	3.3K/F_4	CS23302FB12

VEN need more than 1.6V

if +1.05V connect to +1.05V_GFX, can uninstall

+3VPCU change to +3V
+5VPCU change to +5V

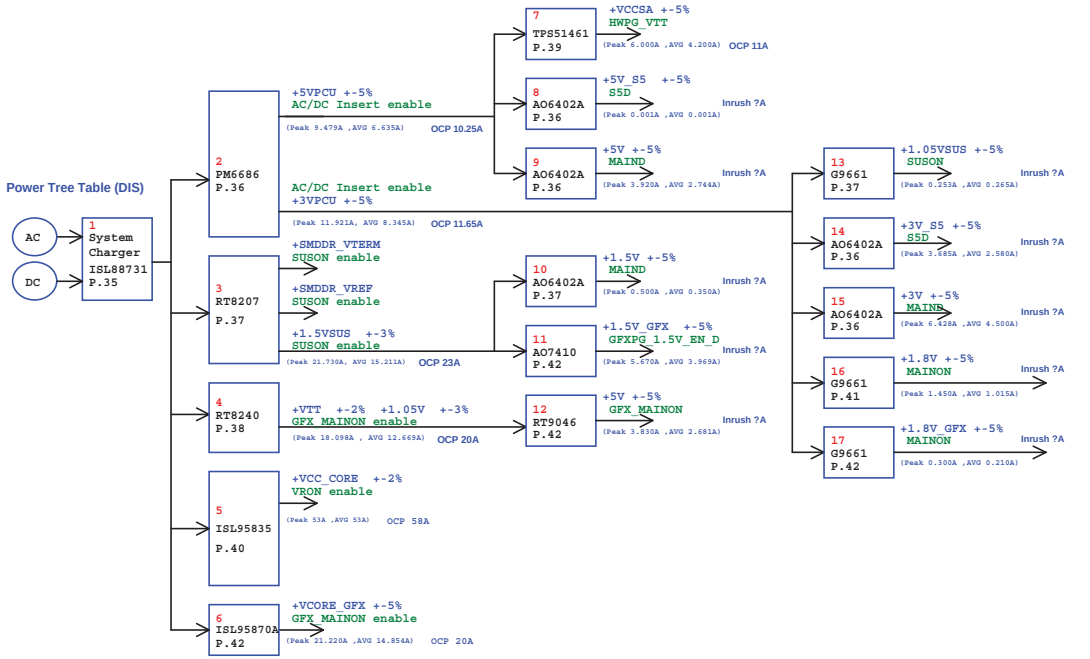
Power On Sequence
1. +3V_GFX connect +3V
2. +1.05V_GFX connect +1.05V
3. GFX_Mainon Enable +VCORE_GFX
4. GFX_VCORE_PG Enable(Delay) +1.5V_GFX
5. +1.5V_GFX Enable +1.8V_GFX
6. GFX_V18_PG connect GFX_PG

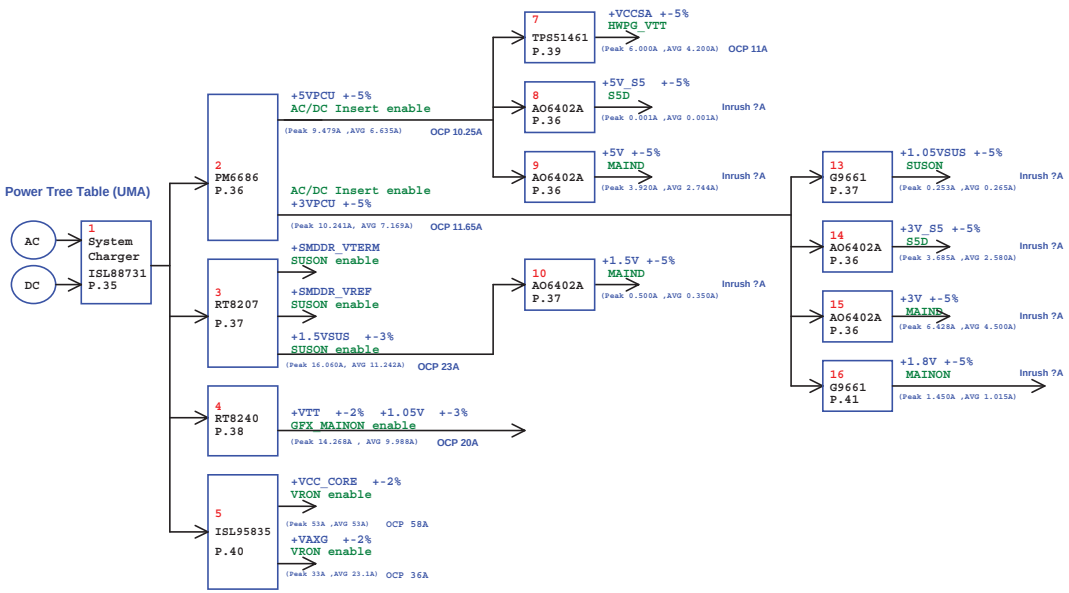
Power Off Sequence
compare +VCC3_GFX with +V1.8_GFX

Quanta Computer Inc.
PROJECT : TE5

Size	Document Number	Rev
	GPU	1A

Date: Wednesday, January 05, 2011 Sheet 42 of 44





Power Distribution List

Power	Distribution

Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Rev
	POWER TREE TABLE	1A

Date: Wednesday, January 05, 2011 Sheet 43 of 44

Model	REV	CHANGE LIST
TE5 MB	1A	PAGE 3: (UMA)--R52 change to 25.5/F_4
		PAGE 5: (UMA)--C183,C190,C195 change to 10U/6.3V_8X
		PAGE 7: (UMA)--R224,R197 change to NC
		PAGE 9: (UMA)--PCIE_CLK_USB30_REQ#, R138 pull up to +3V_S5
		PAGE 9: (UMA)--PCIE_CLK_MINI_REQ#, R237 pull up to +3V
		PAGE 9: (UMA)--R199 NC
		PAGE 9: (UMA)--Q30, Q62 NC
		PAGE 10: (UMA)--add TP31
		PAGE 10: (UMA)--change Board ID9 strap Function name
		PAGE 11: (UMA)--C252 change to 10U/6.3V_8X
		PAGE 11: (UMA)--Net +1.05V change to +VTT
		PAGE 11: (UMA)--R117,R182,R114 change to 10K_4
		PAGE 12: (UMA)--R190,R194,R110 change to 10K_4
		PAGE 23: (UMA)--C978 NC
		PAGE 23: (UMA)--R66,R412,R154,Q45 change Function code to HM@ and delete discrete HDMI-HPD reference
		PAGE 24: (UMA)--add D7
		PAGE 25: (UMA)--add R201,R7,Q10
		PAGE 27: (UMA)--USB3.0 change to NEC solution
		PAGE 30: (UMA)--C97,C92,C106 change to 1U/10V_6Y
		PAGE 31: (UMA)--CN21 Foot-print change to 3in1-cm35-5-21p
		PAGE 32: (UMA)--3ND_MBCLK,3ND_MBDATA R269,R270 pull up to +3V
		PAGE 32: (UMA)--add 13MS,14MS,15MS Strap pin SKU_STRAP_1,SKU_STRAP_2,SKU_STRAP_3
		PAGE 33: (UMA)--add PR1
		PAGE 34: (UMA)--LED1,LED4,LED5,LED6 change symbol and Foot-print
		PAGE 16: (VGA)--add R3712
		PAGE 19: (VGA)--R3711 change to 47U/6.3V_1206X
		PAGE 25: (ALL)--Net name PCIE_CLK_3G_REQ# change to PCIE_CLK_3G_REQ#_C
		PAGE 22: (ALL)--add R65
		PAGE 37: (ALL)--PC60 change to CC7390JMZ02
		PAGE 18: (VGA)--add R3601, R3575
		PAGE 24: (UMA)--CN4 Value change to 87213-2000G
		PAGE 22: (ALL)--add R102
		PAGE 33: (ALL)--Remove K/B LED power circuit
	2A	PAGE 15: (VGA)--delete R3535,R3547
		PAGE 22: (ALL)--add R31
		PAGE 22: (ALL)--add R102
		PAGE 40: (ALL)--add PC168
		PAGE 32: (ALL)--13MS,14MS,15MS Strap pull up voltage change to +3VPCU
		PAGE 34: (ALL)--add R213
		PAGE 42: (VGA)--add PQ49

MODEL TE5

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 204	PROJECT MODEL :	TE5	APPROVED BY:	Andy Wang	DATE:	2010/10/01
	PART NUMBER:		DRAWING BY:	Andy Wang	REVISON:	1A

Quanta Computer Inc.

PROJECT : TE5

Size | Document Number: Change list | Rev 1A

Date: Wednesday, January 05, 2011 Sheet 31 of 35

Model	REV	CHANGE LIST
TE5 MB	1A	PAGE 35: (COM)--add PC76 and PC77 for EMI Sol. (101005) PAGE 35~42: (COM)--delete PJP1 , PJP2 , PJP3 , PJP14 , PJP6 , PJP9 (101005) PAGE 38: (COM)--PC212 change to 0.1U/25V_6X (101005) PAGE 38: (COM)--PC216 change to 1.74K/F_4 (101005) PAGE 40: (COM)--PC153 and PC154 change to 330U/2V_7343P_E9C (101005) PAGE 36: (COM)--add PD12 , PR142 , PR139 (101011) PAGE 38: (COM)--Change VTT/1.05V solution (101011) PAGE 37: (COM)--PC59 stuff (101014) PAGE 38: (COM)--Change PQ18 and PQ19 Value (101014) PAGE 40: (COM)--Change PR184 Value ; PC151 stuff (101014) PAGE 42: (COM)--PC113 no stuff (101014) PAGE 35 , 37 , 38 , 40: (COM)--PR14 , PC19 , PR48 , PC61 , PR70 , PC80 , PR159 , PC157 , PR177 , PC171 , PR200 , PC195 stuff (101020) PAGE 36: (COM)--PU2 , PL4 , PL5 change Value (101020)

MODEL TE5

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 204	PROJECT MODEL :	TE5	APPROVED BY:	Andy Wang	DATE:	2010/10/01
	PART NUMBER:		DRAWING BY:	Andy Wang	REVISON:	1A

Quanta Computer Inc.

PROJECT : TE5

Size | Document Number: Change list | Rev 1A

Date: Wednesday, January 05, 2011 Sheet 31 of 35