Berry Discrete/UMA Schematics Document

AMD Danube CPU S1g4

AMD GPU Madison-LP/M96-LP M2

RS880M + SB820M

2010-03-08

REV : A00

DY : Nopop Component

<Core Design>

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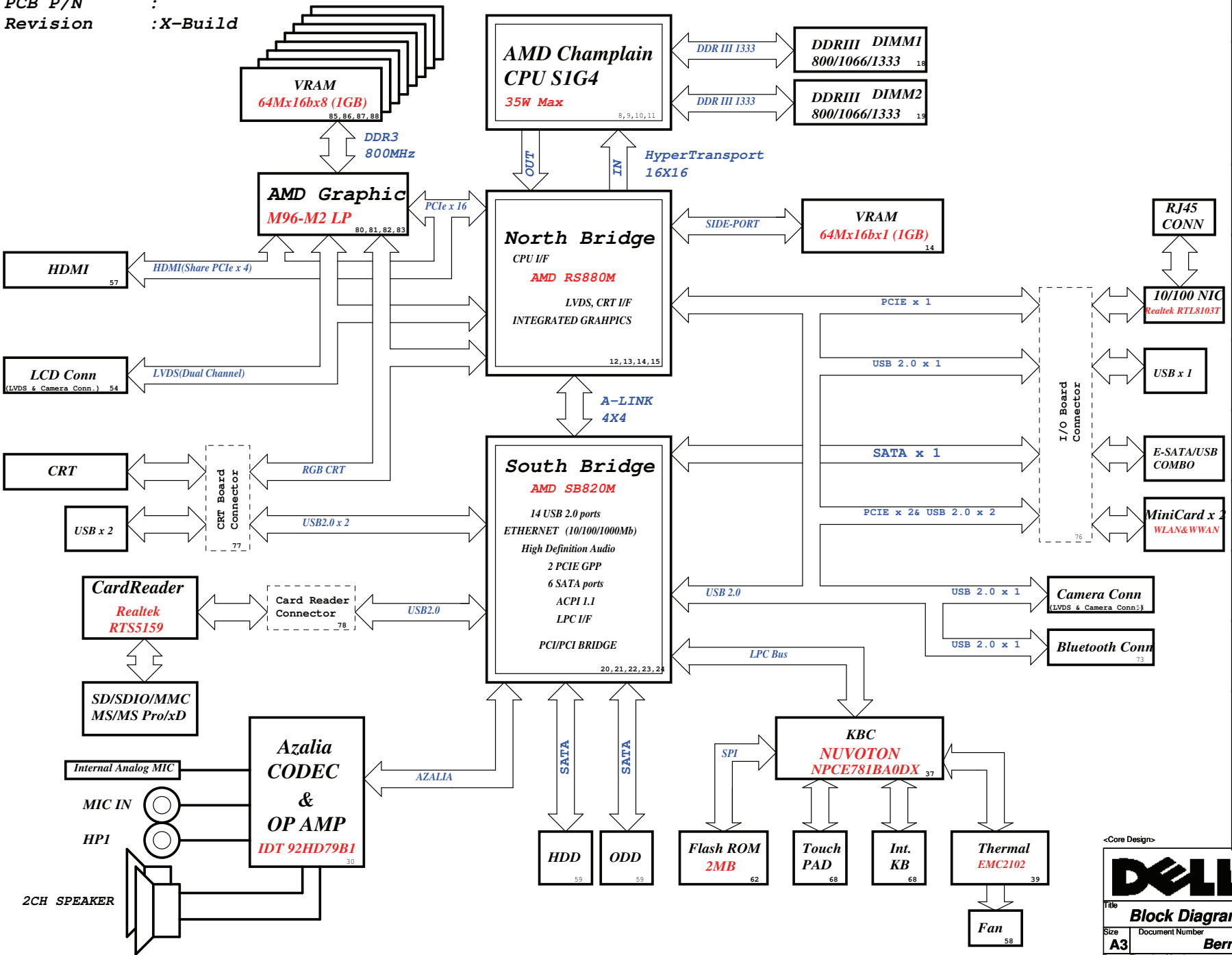
Title	Cover Page	
Size: A4	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Monday, March 08, 2010	Sheet 1 of 95	

Project code :91.4HH01.001
PCB P/N :
Revision :X-Build

Berry DG15 Discrete/UMA Block Diagram



CHARGER	
BQ24745	45
INPUTS	OUTPUTS
+DC_IN_SS +VCHGR	+PWR_SRC

SYSTEM DC/DC	
RT8205B	46
INPUTS	OUTPUTS
+PWR_SRC	+3.3V_RTC_LDO +5V_ALW +3.3V_ALW

CPU VDDR	
RT9025	48
INPUTS	OUTPUTS
+1.5V_SUS	+CPU_VDDR

CPU CORE	
ISL6265AHRTZ-T-GP	47
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE +VDDNB

AMD RS880M CORE	
RT8209	50
INPUTS	OUTPUTS
+PWR_SRC	+NB_VDDC

AMD SB820M S5 POWER	
RT9025	48
INPUTS	OUTPUTS
+3.3V_ALW	+1.1V_ALW

DDR III SUS&VTT	
RT8207	49
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS

DDR III SUS&VTT	
RT8207	49
INPUTS	OUTPUTS
+PWR_SRC	+0.75V_DDR_VTT

AMD GPU CORE	
RT8208B	89
INPUTS	OUTPUTS
+PWR_SRC	+VGA_CORE

PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

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Title: Block Diagram
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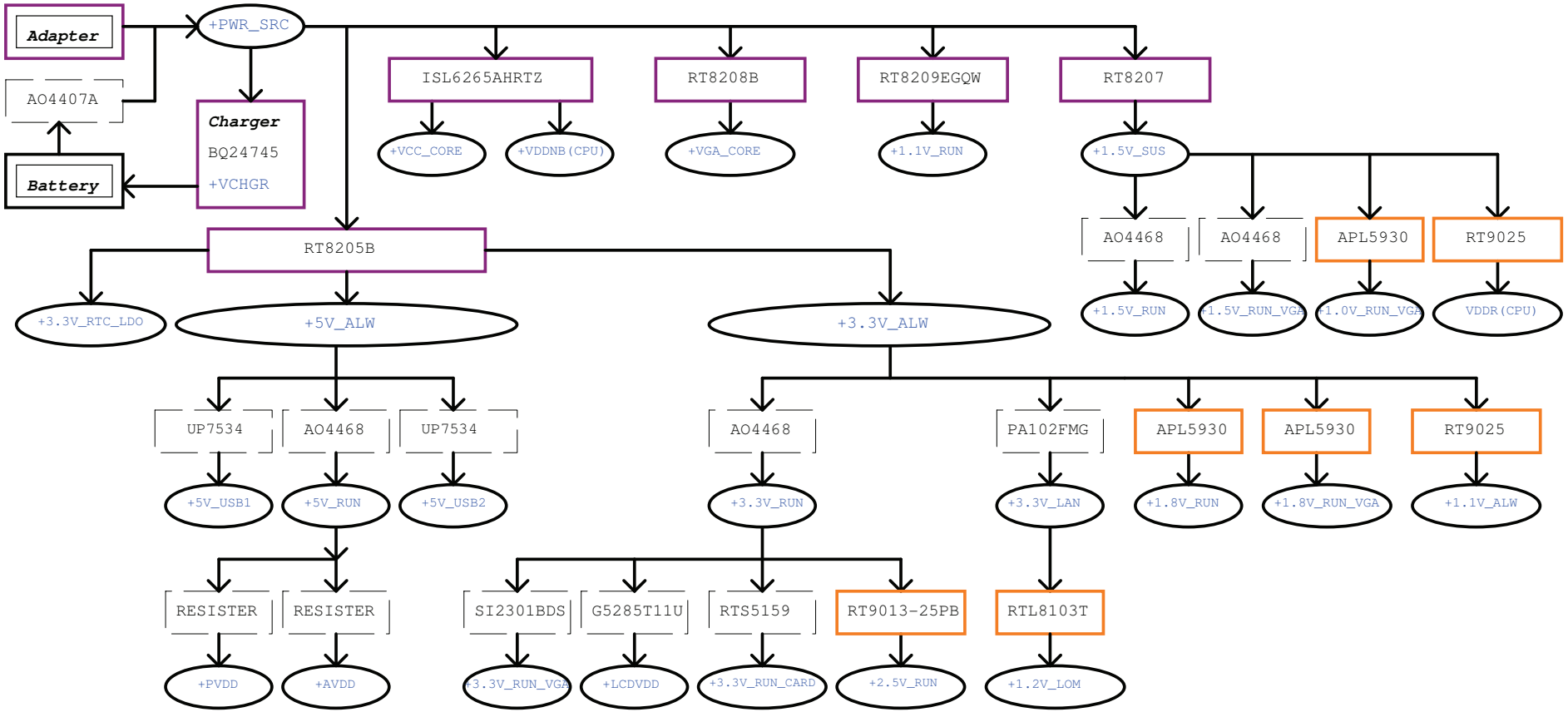
Power Block Diagram

Power Shape

Regulator | LDO | Switch



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Title	Power Block Diagram	
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
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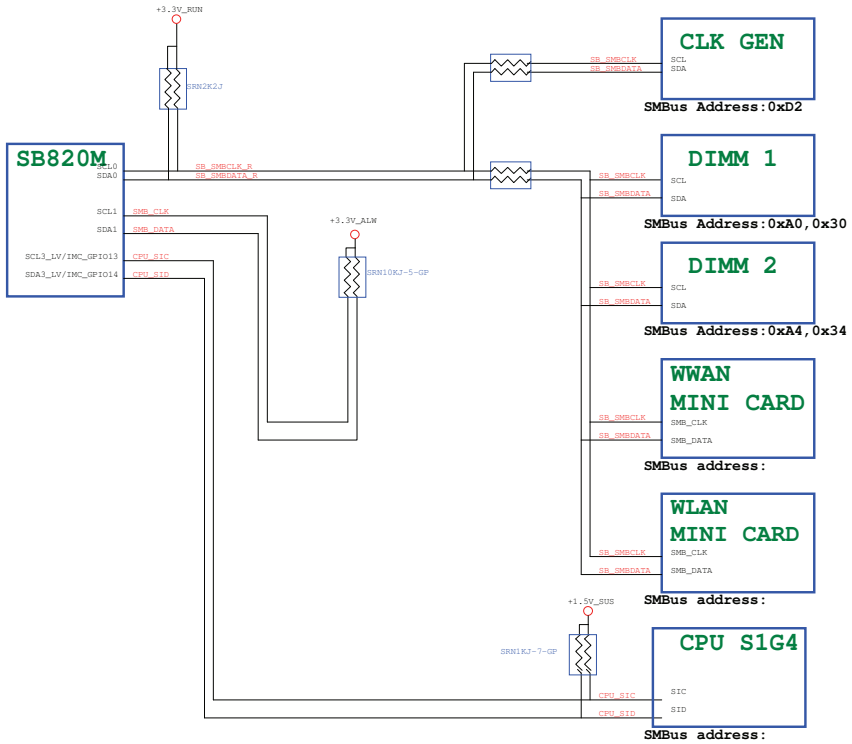
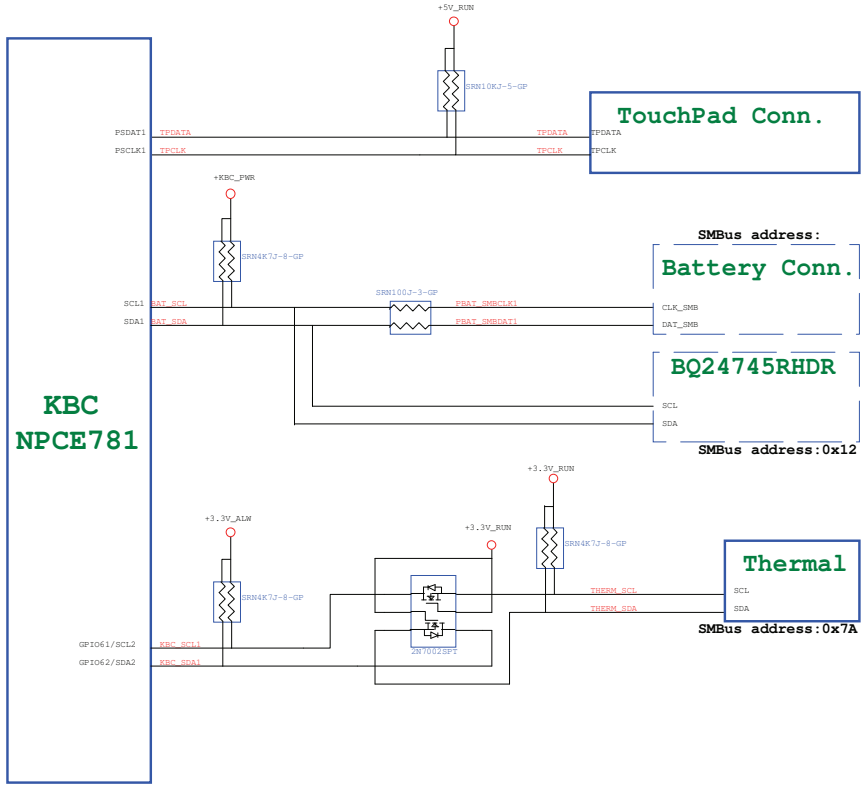
SB820M SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM		
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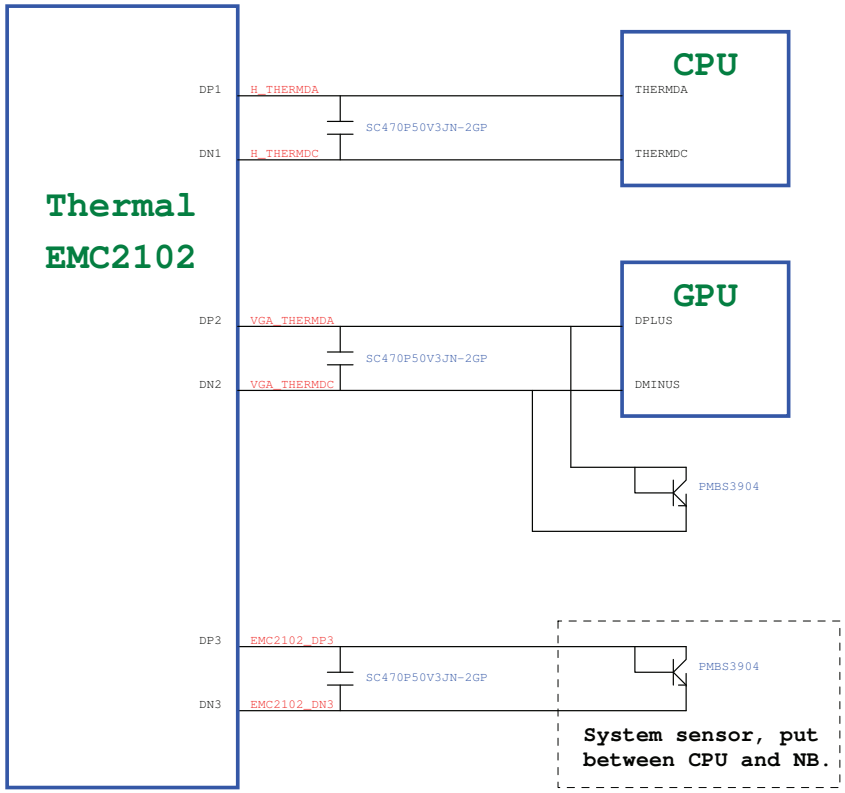
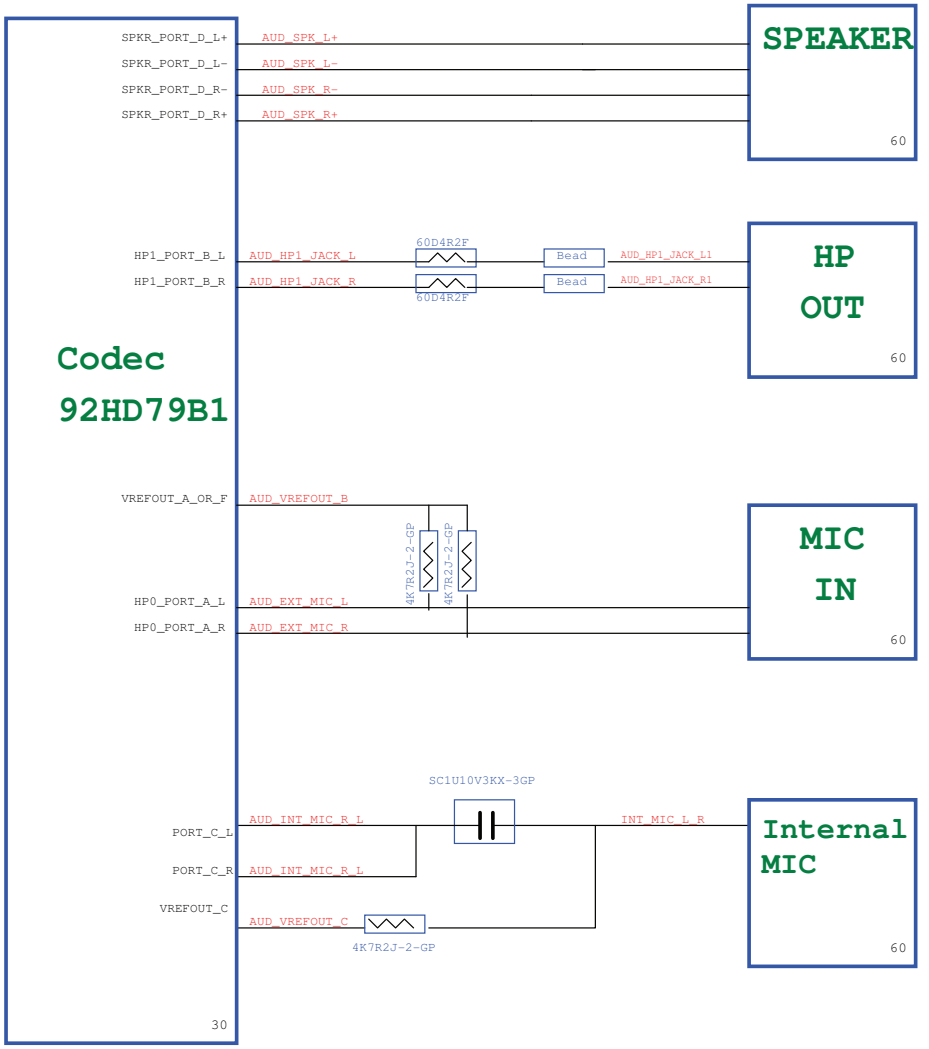
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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SB820M Strapping

Capture from 45484 Rev. 1.02 AMD SB8xx-Series Southbridge Design Guide

Name	Strap Name	Schematic Note
LPCCLK0	ECEnableStrap	Embedded Controller (EC) * 0 V - Disabled 3.3 V - Enabled
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	ROMTYPE_1 / ROMTYPE_0 / ROM TYPE 3.3V / 0V / SPI ROM 3.3V / 3.3V / Reserved 0V / 0V / Firmware Hub 0V / 3.3V / LPC ROM * (supports both LPC and PMC ROM types)
LPCCLK1	CLKGEN	Defines clock generator * 0V - External clock mode: Use 100-MHz PCIeR clock as reference clock and generate i nternal clocks only. 3.3V- Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks
PCICLK1	BIF_GEN2_ COMPLIANCE_Strap	Set PCIe to Gen II mode 0V- Force PCIe interface at Gen I mode * 3.3V- PCIe interfacce is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.
PCICLK2	BootFailTmrEn	Watchdog function * 0V- Disable the boot fail timer function 3.3V- Enable the boot fail timer function
PCICLK3	DefaultStrapMode	Default Debug Straps * 0V- Disable Debug Straps. 3.3V- Select external Debug Straps
PCICLK4	CPUClkSel	CPU/NB HT Clock Selection 0V- Reserved. * 3.3V- Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.
AZ_SDOUT	CoreSpeedMode	Slow down core clock for low power platform. * 0V- Performance mode 3.3V- Low Power mode

RS880M Strapping

Capture from 46113_rs880m_ds_nda_1.03

Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO _ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable * 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not 0: Available(UMA) 1: Not available(Discrete)
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. * 1: Use default values

USB Table

USB	
Pair	Device
0	USB0 (I/O Board/ESATA)
1	USB1 (I/O Board)
2	USB2 (CRT Board)
3	USB3 (CRT Board)
4	WLAN USB
5	WWAN USB
6	RESERVED
7	RESERVED
8	RESERVED
9	BLUETOOTH
10	CARD READER
11	CAMERA (LVDS CONN)
12	RESERVED
13	RESERVED

PCIE Routing

	RS880M
LANE0	MiniCard WLAN
LANE1	LAN
LANE2	MiniCard WWAN

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Title: Table of Content

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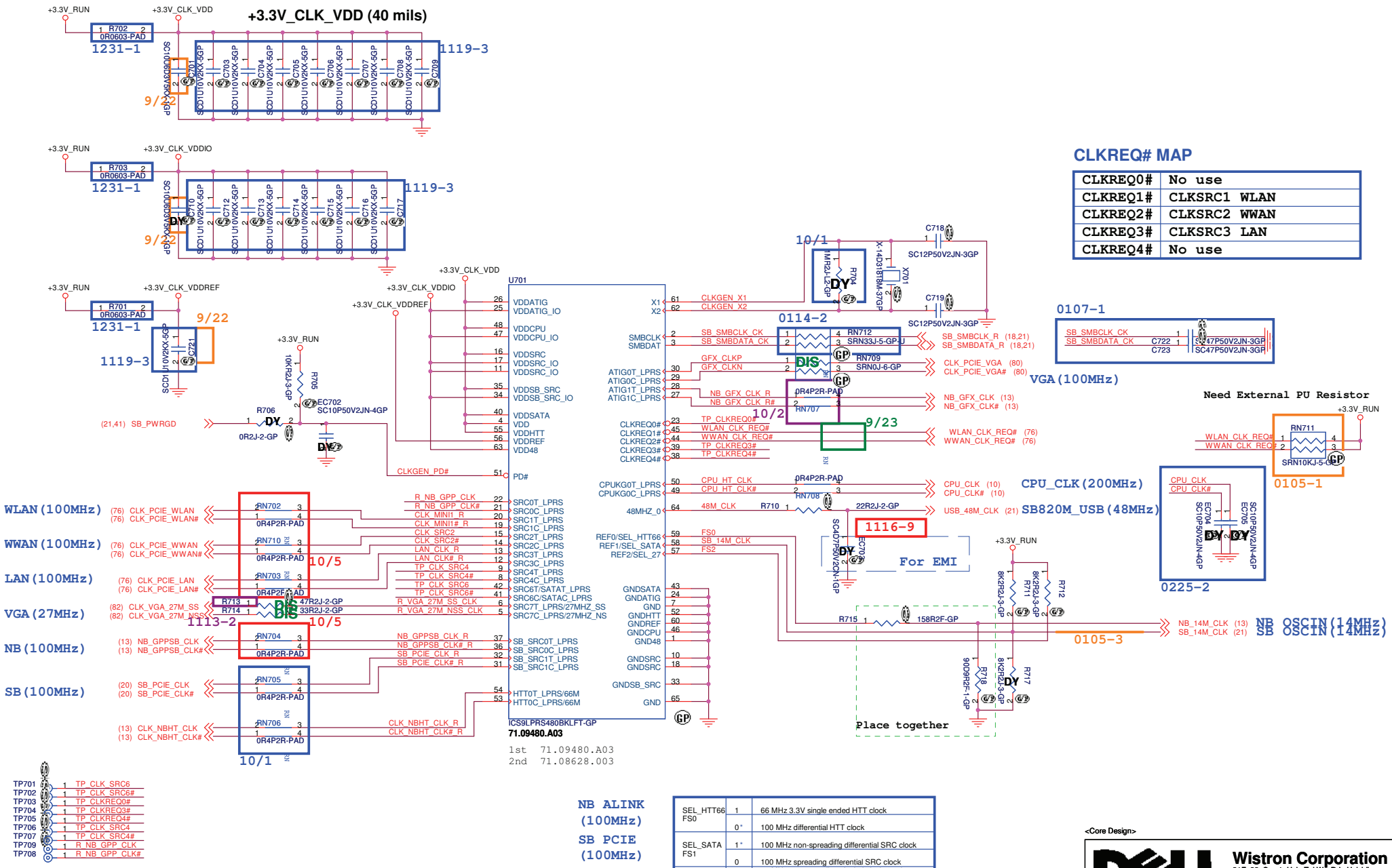

SEL_HTT66 FS0		
	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA FS1	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27MHz FS2	1*	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0	100MHz differential spreading SRC clock

* default

<Core Design>
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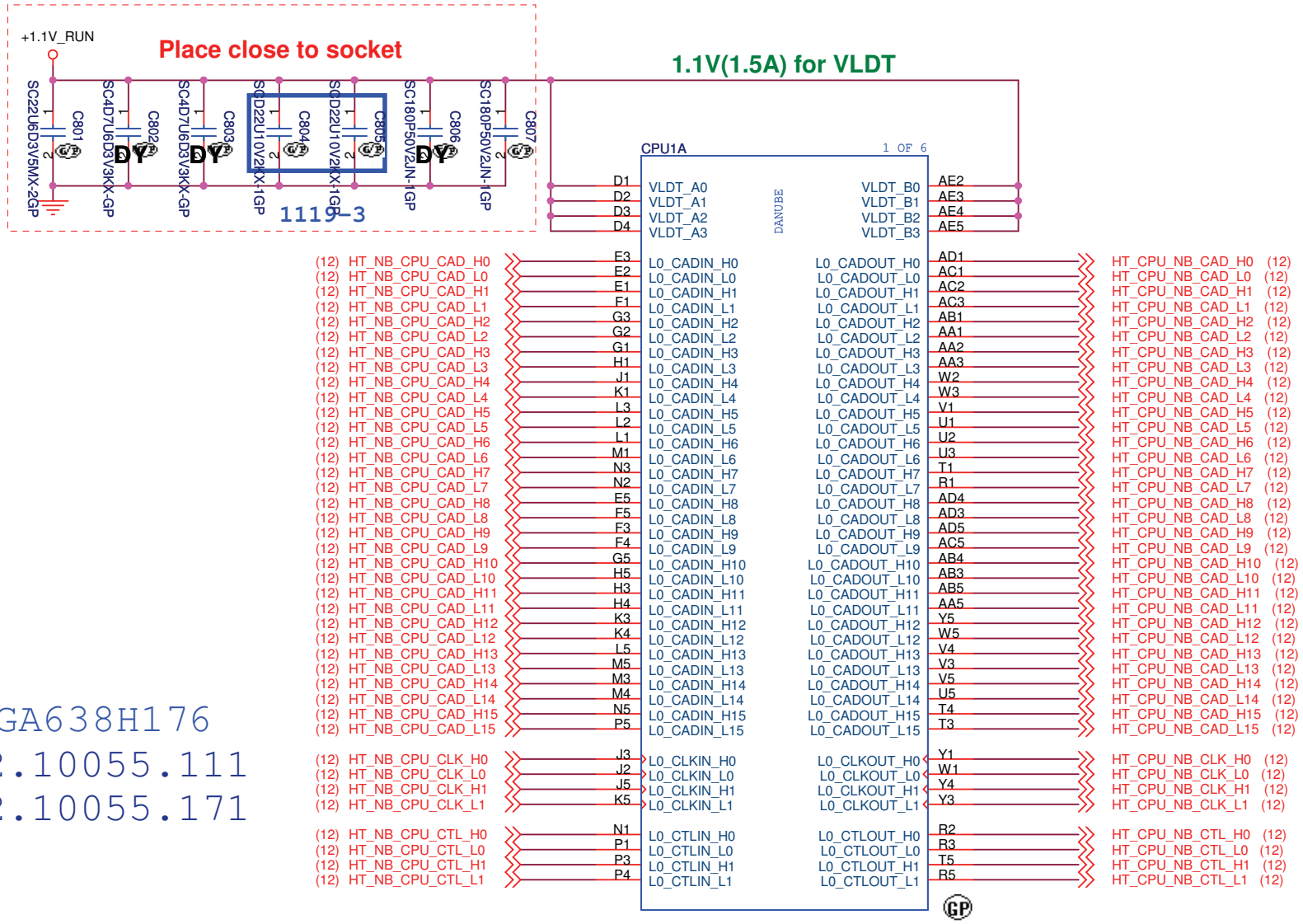
SSID = CPU



SKT-BGA638H176

1'nd 62.10055.111

2'nd 62.10055.171

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Title: ***CPU_HT_LINK I/F_(1/4)***

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

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SSID = CPU

1231-2

Set empty: C905,C906,C903,C909,C913,C910,C915

4.7UF*4
0.22UF*4
1000PF*4
180PF*4

+CPU_VDDR

Place near to CPU

1119-3 1231-2

0.9V, 1.25A--DDR1066
1.05V, 1.75A---DDR1333

CPU1B 2 OF 6

CPU1C 3 OF 6

1119-3

1119-1 CLOSE TO CPU

1117-8 Remove

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Title: CPU_DDR_(2/4)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

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SSID = CPU

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

2.5V(250mA) for VDDA

1119-1

+2.5V_RUN

L1001

PBY160808T-330Y-N-GP

33R, 3A

+2.5V_RUN_VDDA

11/6

Cloce To CPU

Close CPU

0108-5

CPU_CLK(200MHz)

For HDT DBG

10/5

1231-1

1231-2

1129-1

9/11 S1g4 no support LDTREQ#

CPU1D

4 OF 6

1225-4

9/25 9/14

S1G4 not support MEMHOT

11/11

9/22

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

HDT Connectors

1229-1

For old HDT tool (3.3V level)

0112-2

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Title: CPU_Control&Debug_(3/4)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

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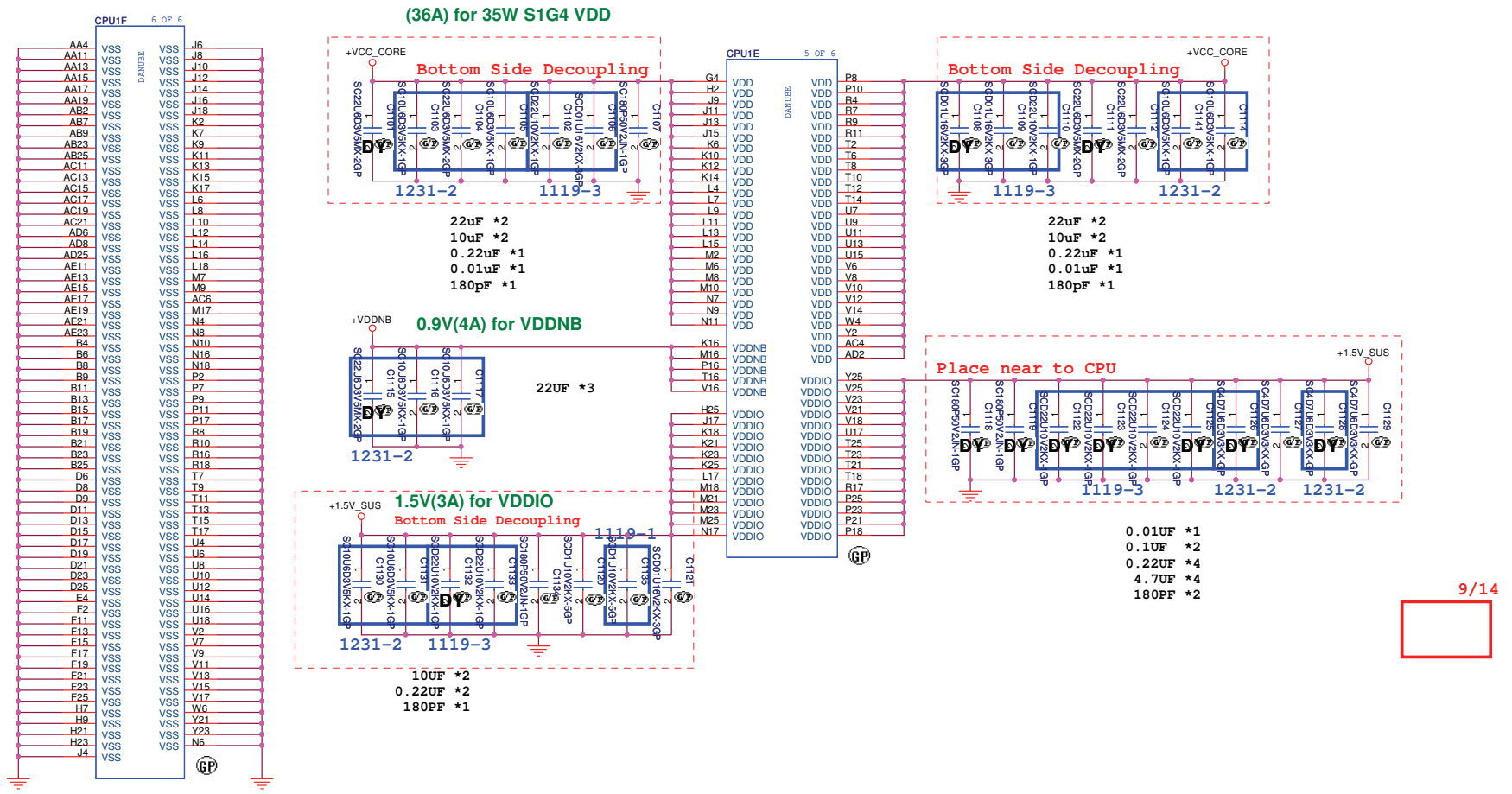
SSID = CPU



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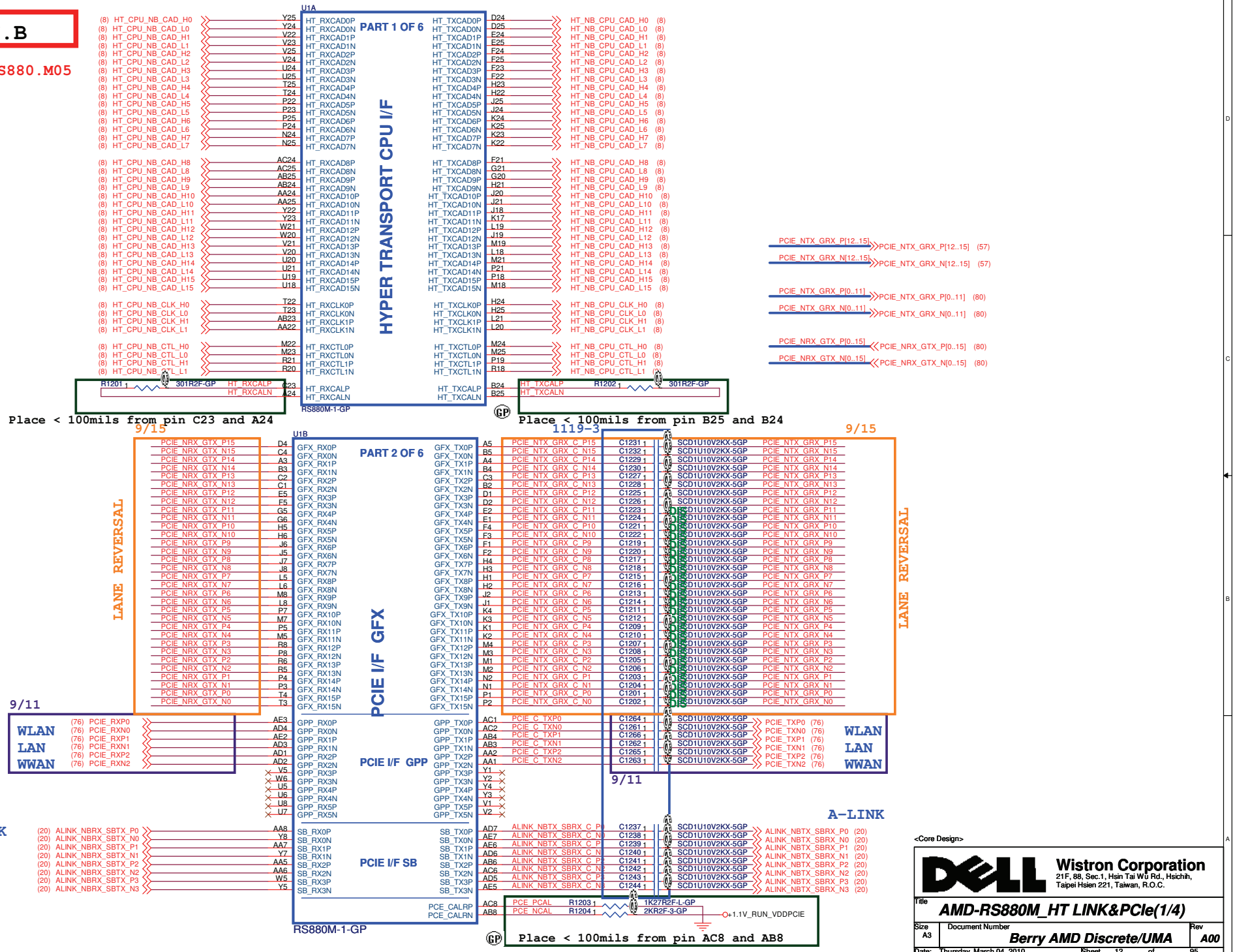
Title	CPU_Power_(4/4)	
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 11 of 95	

SSID = N.B

RS880M : 71.RS880.M05



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Title: AMD-RS880M_HT LINK&PCIe(1/4)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

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SSID = N.B

RS880M : 71.RS880.M05

UMA DAC Signal:
GREEN/BLUE: Connected to GND through two separate 150- 1% resistors.

RED: Connected to GND through two separate 133- 1% resistors.(For match resistor on CRT/B 150- 1%)

STRAP_DEBUG_BUS_GPIO_ENABLE# (RS880M use DAC_VSYNC)
Enables debug bus access through memory I/O pads and GPIOs.
*1 : Disable
0 : Enable

SIDE_PORT_EN# (RS880M use DAC_HSYNC)
1 = Memory Side port Not available DIS
0 = Memory Side port available UMA_SPM

LOAD_EEPROM_STRAPS#(RS880M use SUS_STAT#)
Selects Loading of STRAPS From EEPROM
*1 : use Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

*DEFAULT

+1.1V_RUN 1.1V, 65mA UMA L1308 BLM15AG221SS1D-GP 220R, 0.3A PLLVDD C1312 10/8 UMA/DIS

+1.8V_RUN 1.8V, 20mA UMA L1307 BLM15AG221SS1D-GP 220R, 0.3A PLLVDD18 C1313 UMA/DIS

+3.3V_RUN UMA R1342 0R3J-0-U-GP 0106-2

+3.3V_RUN_AVDD 3.3V, 110mA C1307 UMA/DIS 10/8

+1.8V_RUN UMA R1333 0R3J-0-U-GP

+1.8V_RUN_AVDDDI 1.8V, 20mA C1306 UMA/DIS

+1.8V_RUN 1119-1 UMA R1344 0R3J-0-U-GP

+1.8V_RUN_AVDDDQ 1.8V, 4mA C1308 SC2D2U6D3V3KX-GP UMA/DIS

Layout Note
Trace at least 15 mil

+1.8V_RUN 1.8V, 20mA L1301 BLM15AG221SS1D-GP 220R, 0.3A +1.8V_VDDA18HTPLL 1119-3 C1302 C1303 10/8

9/22 R1343 0R0603-PAD +1.8V_VDDA18PCIEPLL 1.8V, 120mA C1304 C1305 1119-3

SC22U6D3V5MX-2GP C1306

U1C

PART 3 OF 6

CRT/TVOUT
AVDD1 AVDD2 AVDDDI AVSSDI AVDDQ AVSSQ C_Pr Y COMP_Pb RED REDb GREEN GREENb BLUE BLUEb DAC_HSYNC DAC_VSYNC DAC_SCL DAC_SDA DAC_RSET

PLL PWR
PLLVDD PLLVDD18 PLLVSS VDDA18HTPLL VDDA18PCIEPLL1 VDDA18PCIEPLL2

LVTM
SYSRESET# POWERGOOD LDTSTOP# ALLOW_LDTSTOP

CLOCKs
HT_REFCLKP HT_REFCLKN REFCLK_P/OSCIN REFCLK_N GFX_REFCLKP GFX_REFCLKN GPP_REFCLKP GPP_REFCLKN GPPSB_REFCLKP GPPSB_REFCLKN

PM
I2C_CLK I2C_DATA DDC_DATA0/AUX0N DDC_CLK0/AUX0P DDC_CLK1/AUX1P DDC_DATA1/AUX1N STRP_DATA RESERVED AUX_CAL

MIS.
TXOUT_L0P TXOUT_L0N TXOUT_L1P TXOUT_L1N TXOUT_L2P TXOUT_L2N TXOUT_L3P TXOUT_L3N TXOUT_U0P TXOUT_U0N TXOUT_U1P TXOUT_U1N TXOUT_U2P TXOUT_U2N TXOUT_U3P TXOUT_U3N TXCLK_LP TXCLK_LN TXCLK_UP TXCLK_UN VDDLT18 VSSLTP18 VDDLT18_1 VDDLT18_2 VDDLT33_1 VDDLT33_2 VSSLT1 VSSLT2 VSSLT3 VSSLT4 VSSLT5 VSSLT6 VSSLT7 LVDS_DIGON LVDS_BLON LVDS_ENA_BL TMDS_HPD HPD SUS_STAT# THERMALDIODE_P THERMALDIODE_N TESTMODE

RS880M-1-GP

(77) M_RED R1326 150R2F-1-GP
(77) M_GREEN R1327 150R2F-1-GP
(77) M_BLUE R1328 150R2F-1-GP
9/22

UMA: DAC_CLK and DATA with 5V-tolerant. not need level shift

Trace at least 10 mil

(77) VGA_HSYNC VGA_HSYNC
(77) VGA_VSYNC VGA_VSYNC
(77) DDC_CLK_CON DDC_CLK_CON
(77) DDC_DATA_CON DDC_DATA_CON
R1306 715R2F-GP

(20,37,80) PLTRST#_NB_GPU
(41) NB_PWRGD_IN
9/16
SC180P50V2JN-1GP EC1301 SC180P50V2JN-1GP EC1302
NB_LDT_STOP#
NB_ALLOW_LDTSTOP

+1.1V_RUN R1312 4K7R2F-GP R1313 4K7R2F-GP
(7) NB_14M_CLK 1231-2 R1341 0R0402-PAD
NB_REFCLK_P NB_REFCLK_N

(7) CLK_NBHT_CLK
(7) CLK_NBHT_CLK#

(7) NB_GFX_CLK NB_GFX_CLK
(7) NB_GFX_CLK# NB_GFX_CLK#
10/2 TP1306 TP1307 NB_GPP_CLK NB_GPP_CLK#
SCD1U10V2KX-5GP C1315 10/7

(7) NB_GPPSB_CLK
(7) NB_GPPSB_CLK#

(55) LDDC_CLK
(55) LDDC_DATA
(57) NB_DDC_DATA0
(57) NB_DDC_CLK0
9/15

1120-6 STRP_DATA
TP1305 TP_NB_RESERVED
R1318 2KR2J-1-GP R1319 RS780_AUX_CAL 150R2F-1-GP

9/25
+1.5V_RUN R1309 300R2J-4-GP R1322 DY 0R2J-2-GP
+1.8V_RUN R1311 2K2R2J-2-GP 9/15
(10,20) CPU_LDT_STOP# U1301 A1 A2 GND VCC Y1 Y2 NC7WZ07P6X-1GP SCD1U10V2KX-5GP C1314 NB_LDT_STOP#

+1.8V_RUN R1315 1KR2J-1-GP
(20) ALLOW_LDTSTOP NB_ALLOW_LDTSTOP
R1316 0R0402-PAD
ALLOW_LDTSTOP:
1 = LDTSTOP# can be asserted
0 = LDTSTOP# has to be de-asserted

+3.3V_RUN R1302 3KR2J-2-GP R1303 3KR2J-2-GP
SPM_Disable VGA_VSYNC VGA_HSYNC
R1304 3KR2J-2-GP R1305 DY
SPM_Enable

VGA_TXAOUT0+ (55)
VGA_TXAOUT0- (55)
VGA_TXAOUT1+ (55)
VGA_TXAOUT1- (55)
VGA_TXAOUT2+ (55)
VGA_TXAOUT2- (55)
VGA_TXBOUT0+ (55)
VGA_TXBOUT0- (55)
VGA_TXBOUT1+ (55)
VGA_TXBOUT1- (55)
VGA_TXBOUT2+ (55)
VGA_TXBOUT2- (55)
VGA_TXACLK+ (55)
VGA_TXACLK- (55)
VGA_TXBCLK+ (55)
VGA_TXBCLK- (55)

+1.8V_RUN 1.8V, 15mA 1119-1 L1305 BLM15AG221SS1D-GP 220R, 0.3A UMA
1.8V, 300mA L1306 PBY160808T-221Y-N-GP 220R, 2A UMA
SCD1U10V2KX-5GP C1310 SC4D7U6D3V3KX-GP C1313 UMA/DIS
C1309 SC2D2U6D3V3KX-GP UMA/DIS

11/12-4
NB_LCDPWR_EN (55)
NB_BL_PWM (55)
NB_BL_EN (55)
RN1301 9/22 UMA SRN10KJ-5-GP

TP_TMDS_HPD TP1308 0225-1
HDMI_HPD_DET HDMI_HPD_DET (57,82)
R1317 UMA 0R2J-2-GP
NB_SUS_STAT# SUS_STAT# (21)

TESTMODE_NB R1320 1KR2F-GP

+3.3V_RUN 11/6 R1314 4K7R2J-2-GP NB_SUS_STAT# R1321 3KR2J-2-GP DY

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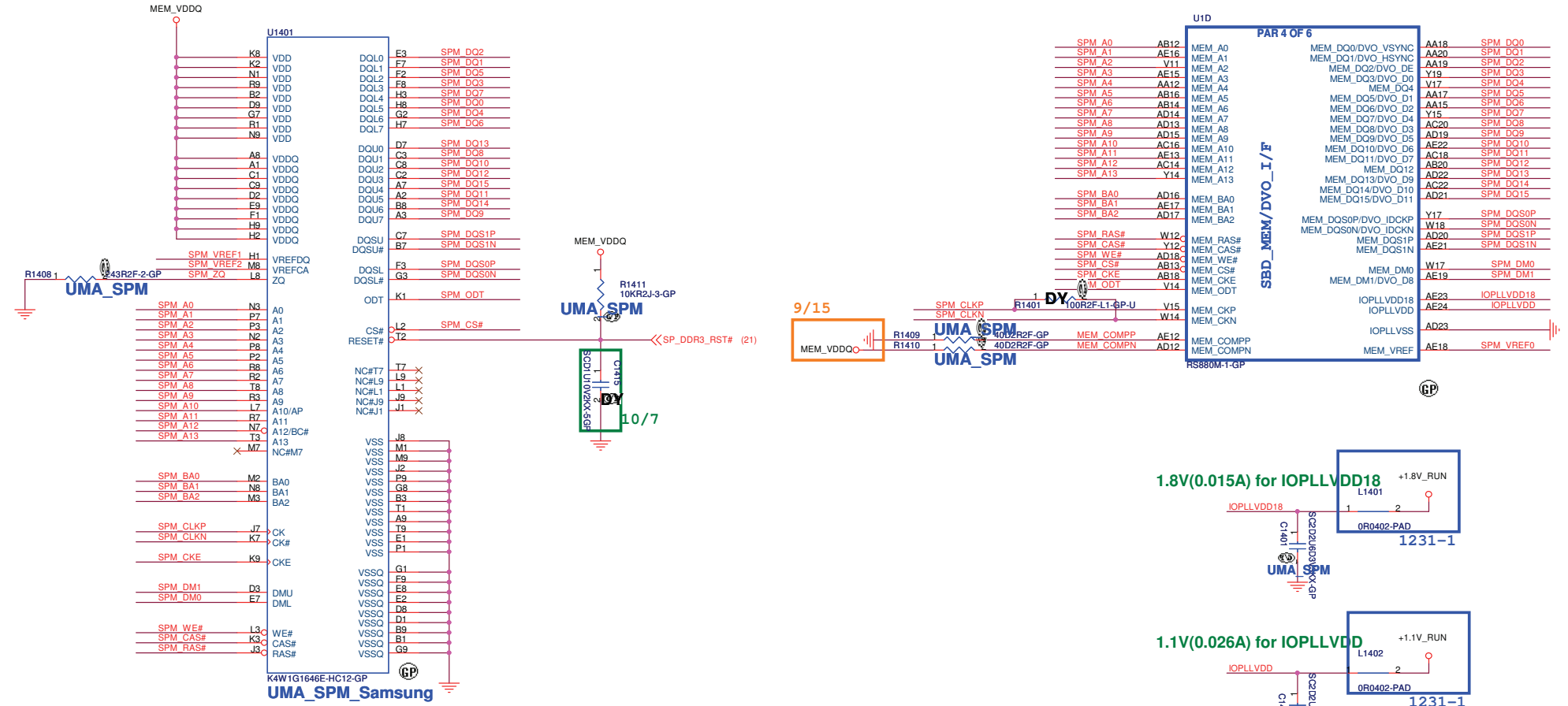
Title: AMD-RS880M_LVDS&CRT_(2/4)
Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00
Date: Thursday, March 04, 2010 | Sheet 13 of 95

SSID = N.B



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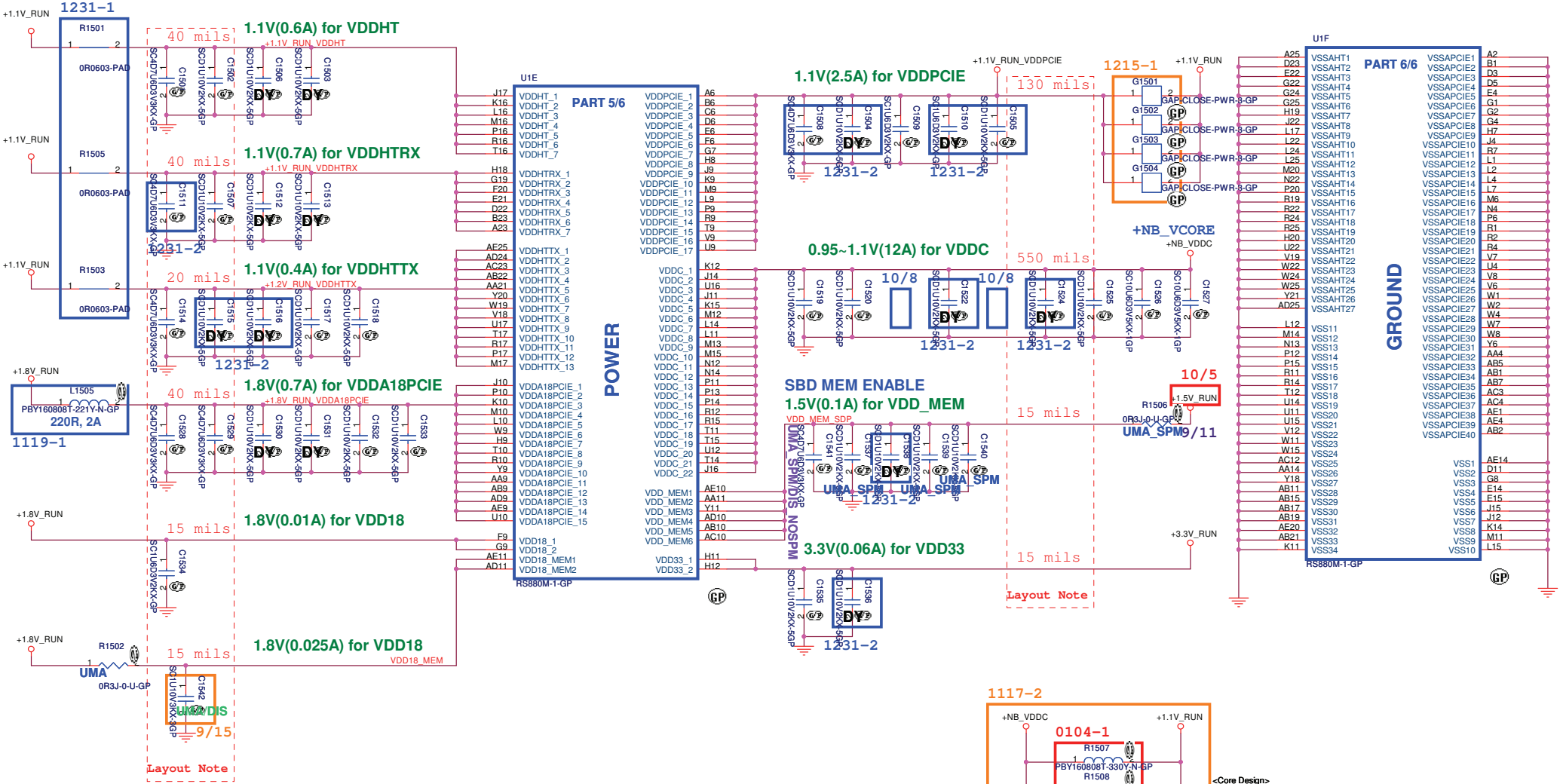
Title	AMD-RS880M_SidePort_(3/4)	
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 14 of 95	

SSID = N.B



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Title: AMD-RS880M_PWR&GD_(4/4)

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 15 of 95

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Title: Reserved

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 16 of 95

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Title: Reserved

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

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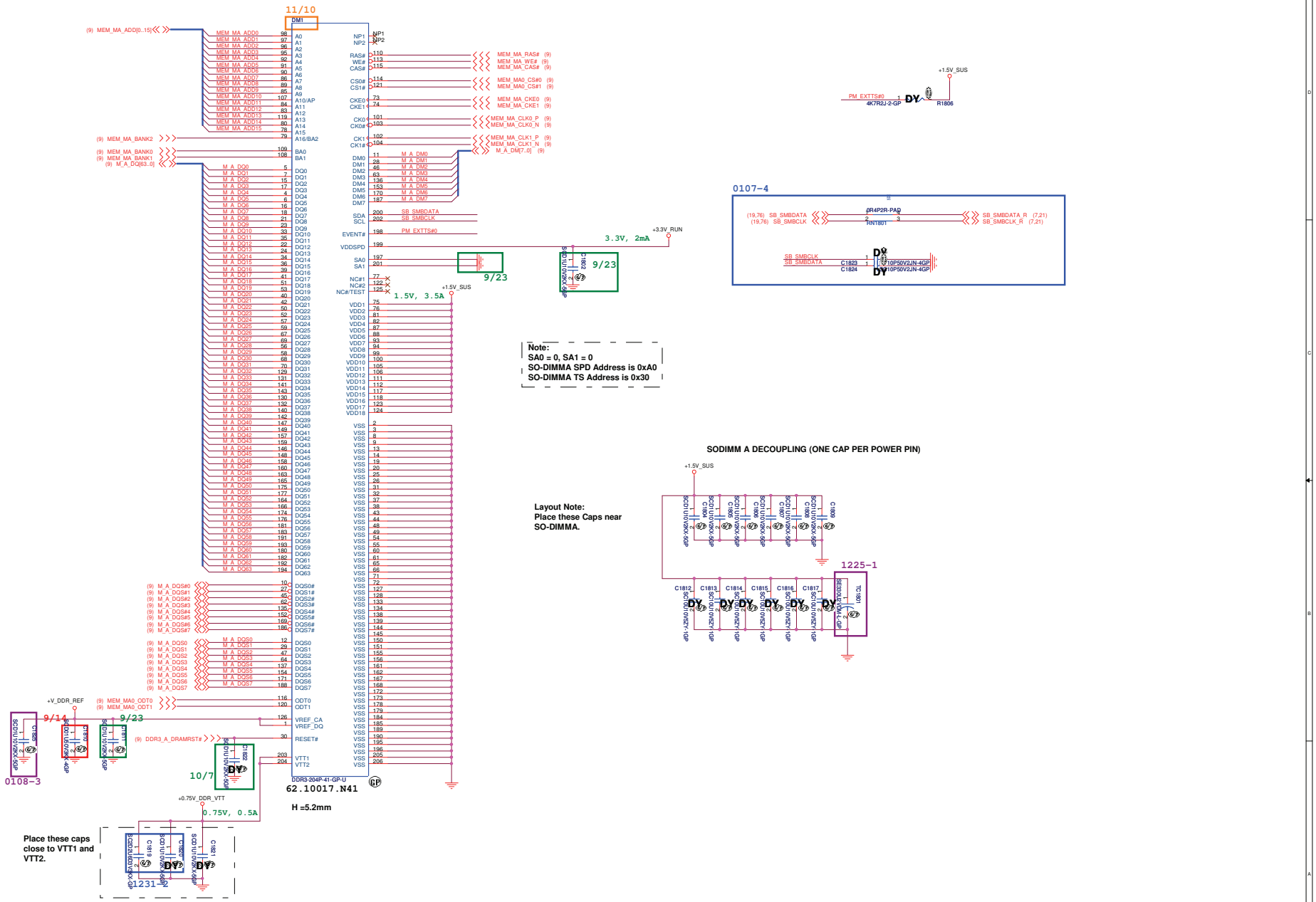
SSID = MEMORY



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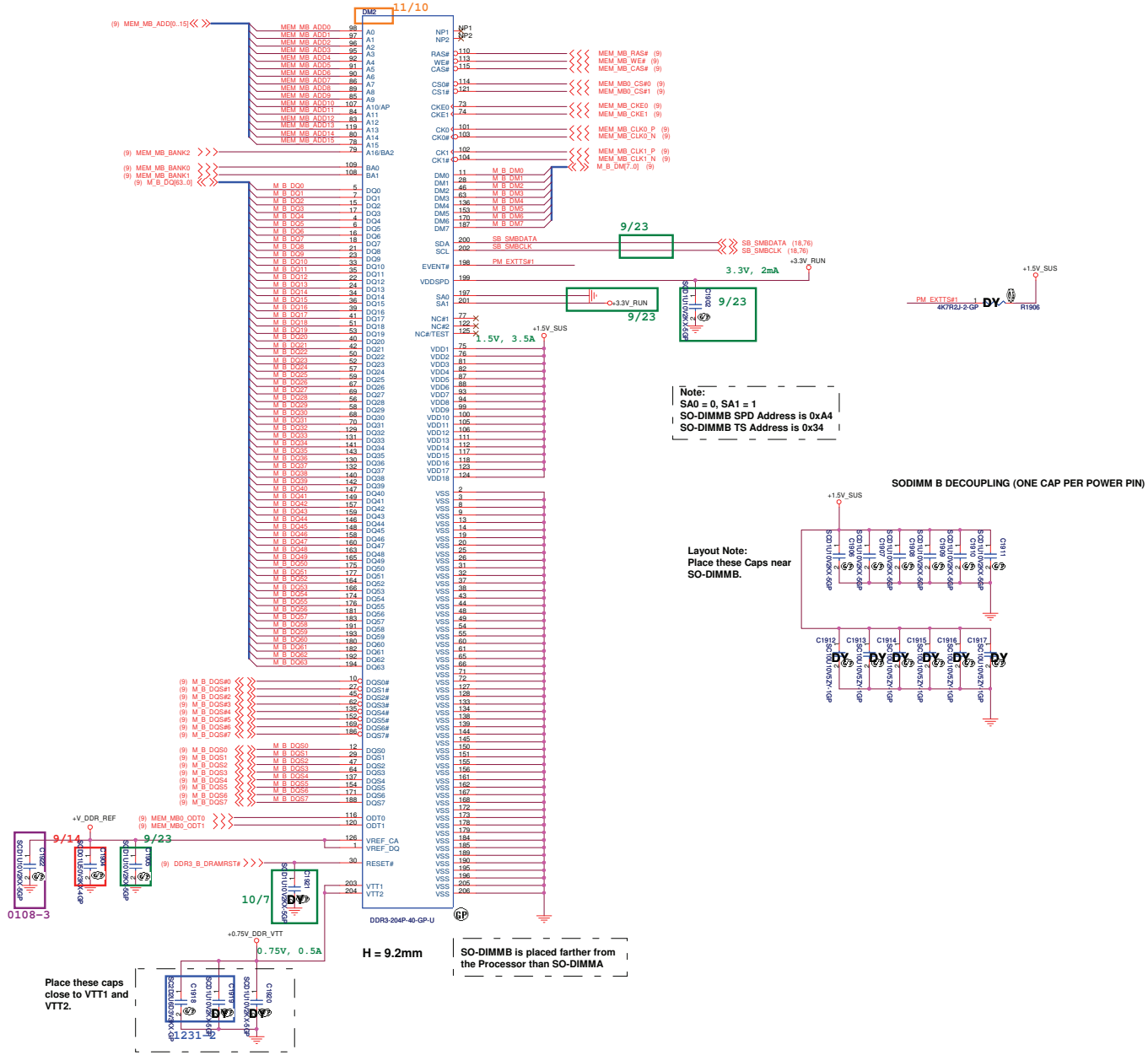
Title: DDR3-SODIMM1

Size | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 18 of 95

SSID = MEMORY



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 19 of 85

SSID = S.B

SB820M : 71.SB820.M02

U2A

Part 1 of 5

SB820M-1-GP

PCI EXPRESS INTERFACES

PCI CLKS

GPP_TX0P GPP_TX0N GPP_TX1P GPP_TX1N GPP_TX2P GPP_TX2N GPP_TX3P GPP_TX3N

GPP_RX0P GPP_RX0N GPP_RX1P GPP_RX1N GPP_RX2P GPP_RX2N GPP_RX3P GPP_RX3N

9/11

NOTE: SB8XX ONLY SUPPORTS 2 GPP
PORT 2 AND 3 IS NOT SUPPORTED. (From CRB)

Place R <100mils form pins AD29,AD28

9/23

9/16

9/22

9/24

9/25

STRAP PIN

1119-1

1231-1

11/6

11/12-1

1118-2

1113-1

LPC Bus Routing first connects to MINICARD then connects to KBC

to EC

1nd 82.30020.791
2nd 82.30020.851

<Core Design>

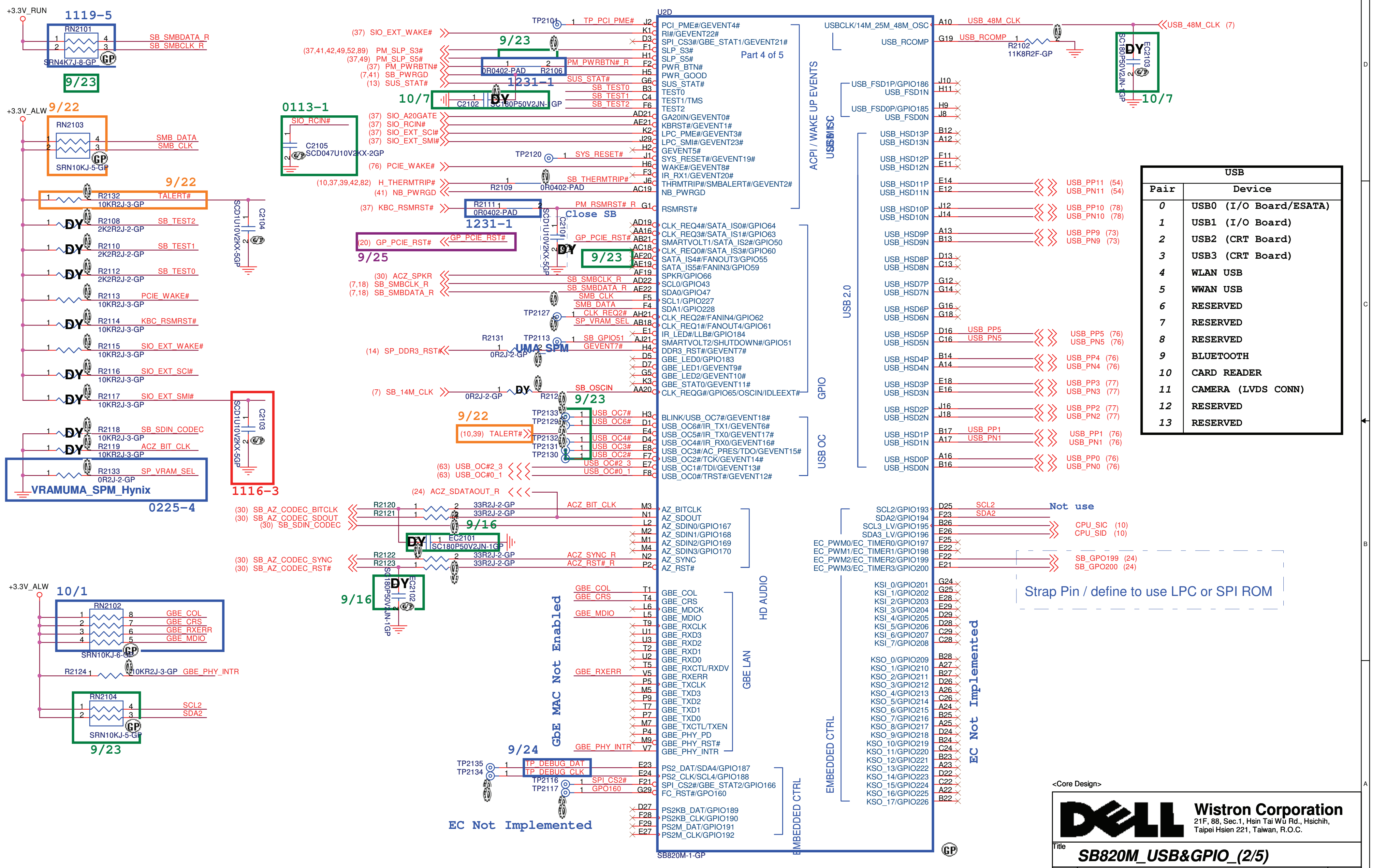
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_PCIE&PCI_(1/5)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Friday, March 05, 2010 | Sheet 20 of 95

SSID = S.B



Pair	Device
0	USB0 (I/O Board/ESATA)
1	USB1 (I/O Board)
2	USB2 (CRT Board)
3	USB3 (CRT Board)
4	WLAN USB
5	WWAN USB
6	RESERVED
7	RESERVED
8	RESERVED
9	BLUETOOTH
10	CARD READER
11	CAMERA (LVDS CONN)
12	RESERVED
13	RESERVED

<Core Design>

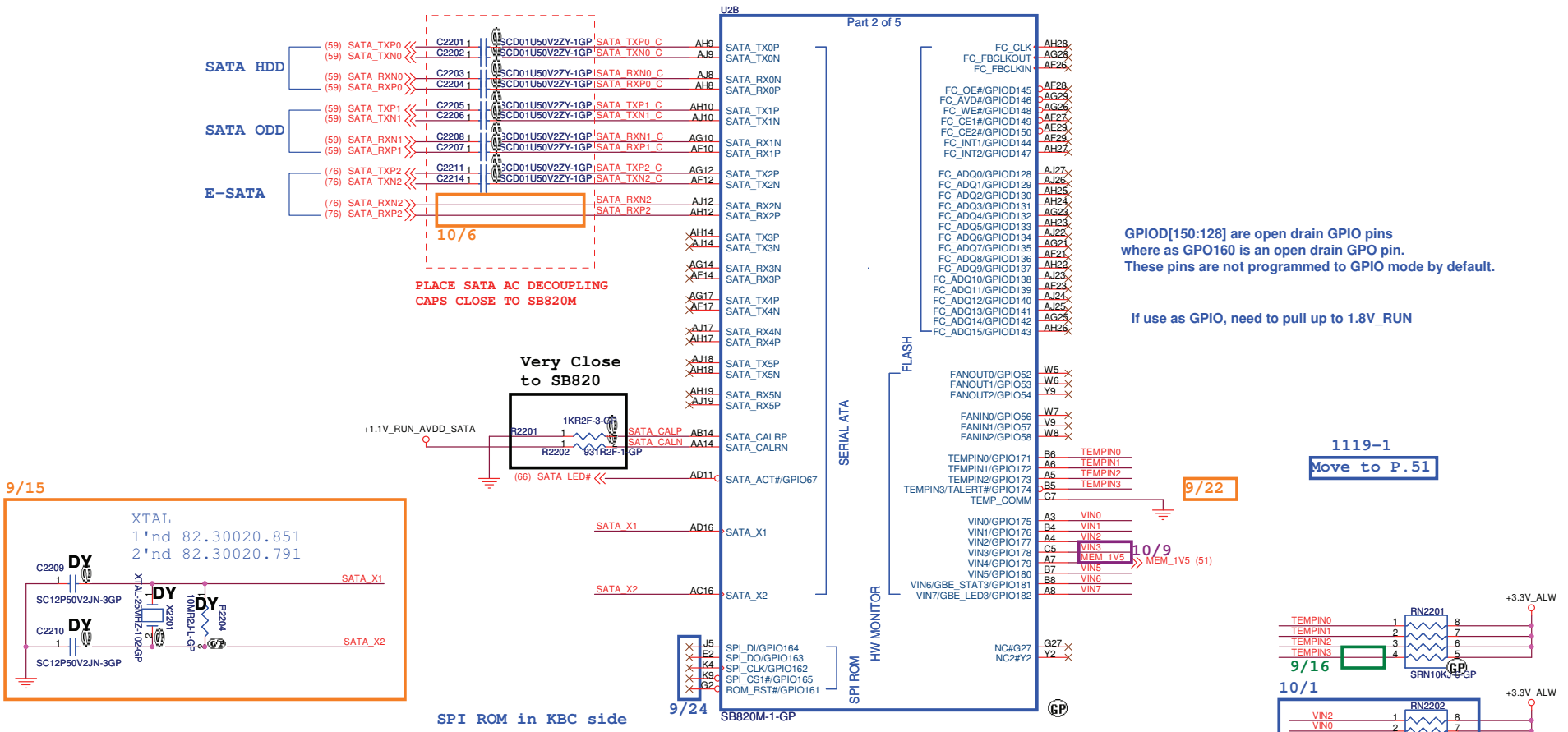
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_USB&GPIO_(2/5)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 21 of 95

SSID = S.B



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	SB820M_SATA-IDE_(3/5)	
Size A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 22 of 95	

SSID = S.B

78mA
0.15mA
11mA
690mA
15mA
1350mA
534mA
88mA
790mA
382mA
GBE PHY not used
49mA
113mA
15mA
58mA
9/17 16mA
12mA
5mA
65mA
46mA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

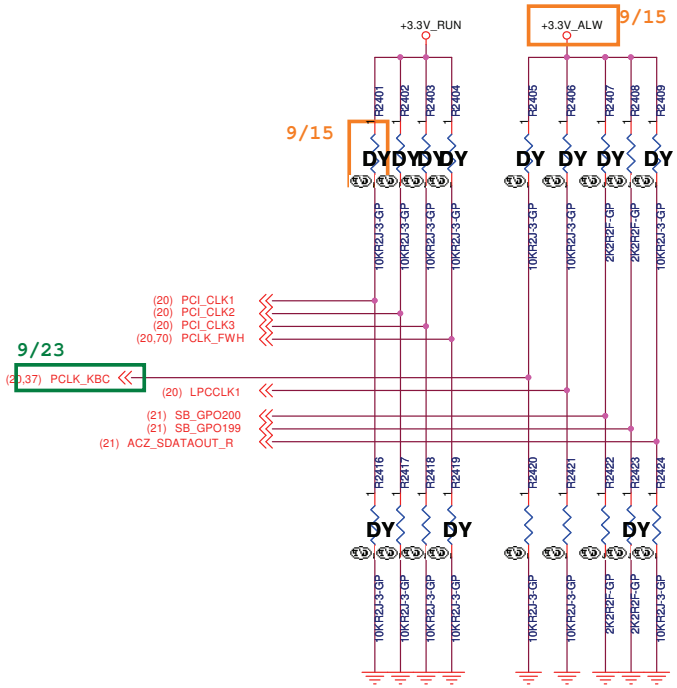
Title: SB820M_POWER&GND_(4/5)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

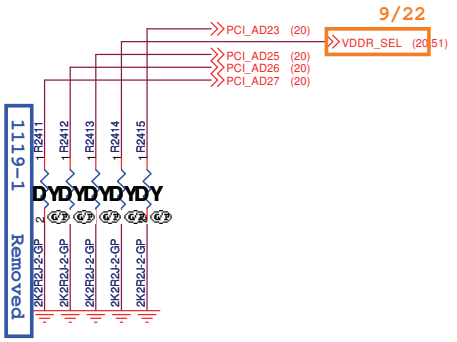
Date: Thursday, March 04, 2010 | Sheet 23 of 95

SSID = S.B

REQUIRED STRAPS



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCLK_KBC (PCI_CLK3)	PCLK_FWH (PCI_CLK4)	LPCCLK0	LPCCLK1	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT	H, H = Reserved H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820M has 15K internal PU FOR PCI_AD[27:23]

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_STRAPPING_(5/5)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Friday, March 05, 2010 | Sheet 24 of 95

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

Size	Document Number	Rev
	Berry AMD Discrete/UMA	***A00***

Date: Thursday, March 04, 2010 Sheet 25 of 95

(Blanking)

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 26 of 95

(Blanking)

<Core Design>

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Title: *Reserved*

Size | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 27 of 95

(Blanking)

<Core Design>

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Title: Reserved

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 28 of 95

(Blanking)

<Core Design>

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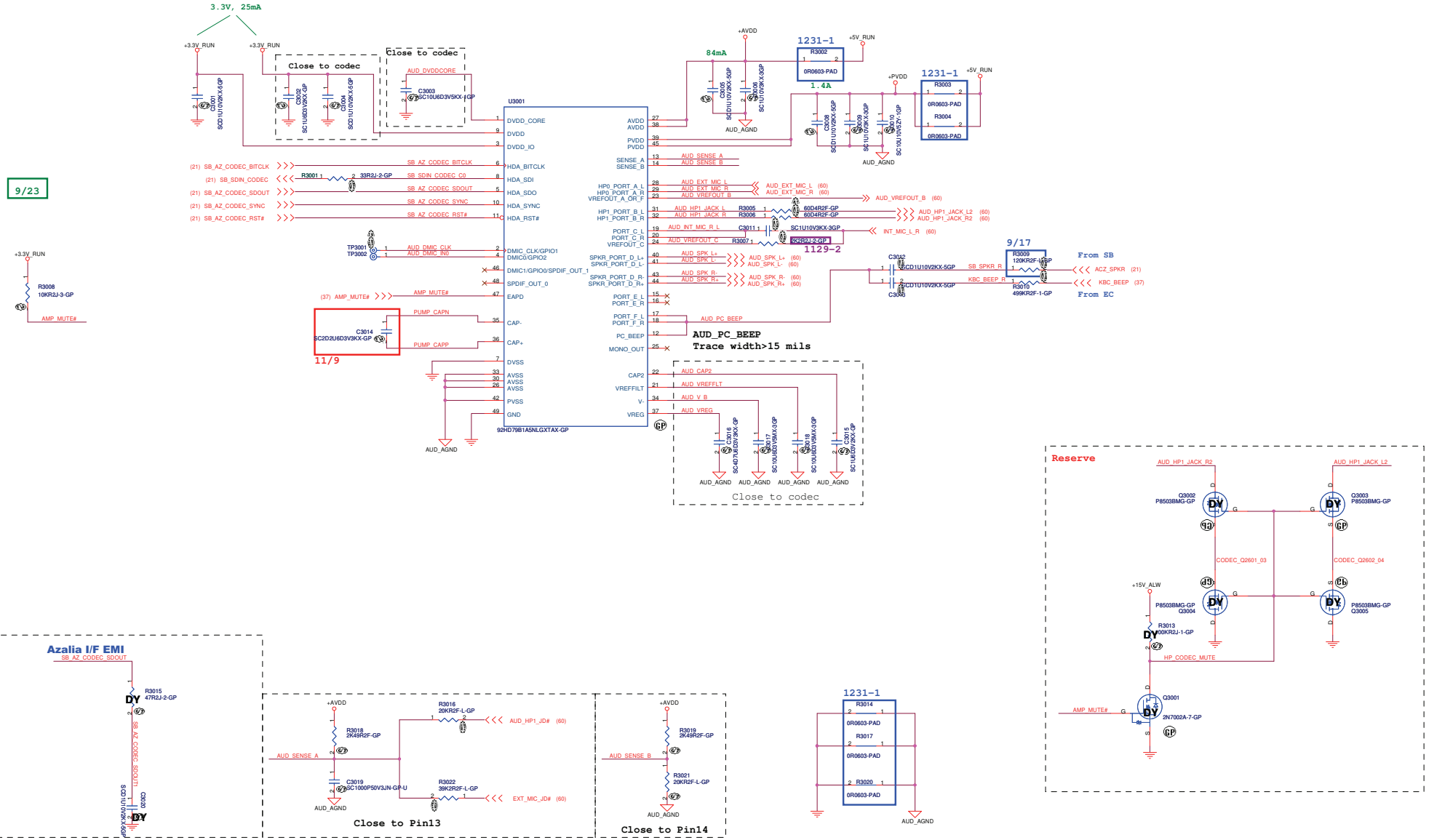
Title: Reserved

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 29 of 95

SSID = AUDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD79B1

Size: A2 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 30 of 85

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 31 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 Sheet 32 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 33 of 95

(Blanking)

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 34 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 35 of 95

(Blanking)

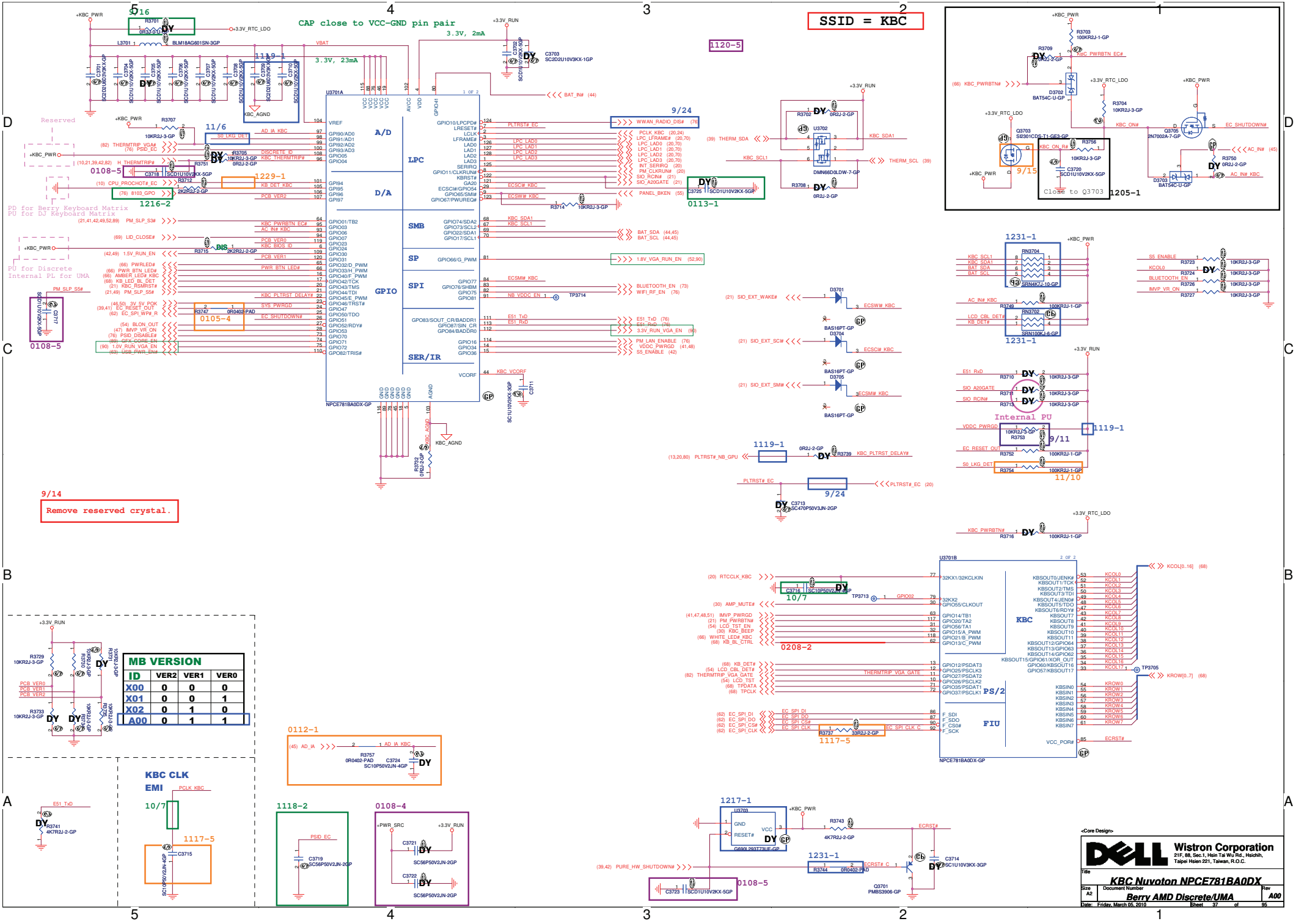
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 36 of 95


SSID = KBC
CAP close to VCC-GND pin pair
3.3V, 2mA
3.3V, 23mA
U3701A
NPCE781BA0DX-GP
KBC_AGND
Reserved
PD for Berry Keyboard Matrix
PU for DJ Keyboard Matrix
PU for Discrete
Internal PL for UMA
9/14
Remove reserved crystal.
MB VERSION
ID VER2 VER1 VER0
X00 0 0 0
X01 0 0 1
X02 0 1 0
A00 0 1 1
KBC CLK
EMI
Close to Q3703
Internal PU
U3701B
KBC
PS/2
FIU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC Nuvoton NPCE781BA0DX
Berry AMD Discrete/UMA
A00
Friday, March 05, 2010

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

Size	Document Number	Rev
A4	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 38 of 95

SSID = Thermal

+5V_RUN
5V, 600mA
C3901 SC10U10V5KX-2GP
C3902 SCD1U10V2KX-5GP
+3.3V_RUN
R3901 10KR2J-3-GP
R3915 DY 0R2J-2-GP
R3916 DY 10KR2J-3-GP
D3901 CH751H-40PT-GP
9/25
EMC2102_FAN_TACH
EMC2102_FAN_TACH (58)
EMC2102_FAN_DRIVE
EMC2102_FAN_DRIVE (58)
RN3901 SRN4K7J-8-GP
THERM_SCL (37)
THERM_SDA (37)
R3902 49D9R2F-GP
3.3V, 0.75mA
EMC2102_VDD_3D3
C3903 SCD1U10V2KX-5GP

Pleace near to CPU side

1.For CPU Sensor
Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing

(10) H_THERMDC
C3910 SC470P50V3JN-2GP DY
(10) H_THERMDA
C3904 SC470P50V3JN-2GP

(82) VGA_THERMDC
0107-5
Removed
C3905 SC470P50V3JN-2GP
(82) VGA_THERMDA

2.VGA Sensor
Layout notice :
Both VGA_THERMDA and VGA_THERMDC routing
10 mil trace width and 10 mil spacing.

VGA_THERMDC
Q3904 PMBS3904-1-GP UMA
0107-3
VGA_THERMDA

Q3901 PMBS3904-1-GP
C3906 DY SC470P50V3JN-2GP
C3907 SC470P50V3JN-2GP

3.HW T8 sensor
Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

U3901 EMC2102
GND
TACH
VDD_5Va
FANa
FANb
VDD_5Vb
SMCLK
SMDATA
VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3
NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15
NC#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#
EMC2102-DZK-GP

EMC2102_DN3
EMC2102_DP3

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

R3903 DY 0R2J-2-GP
ALERT# TALERT# (10,21)
CLK_32K
0105-4 Remove
EM2102_RESET# R3914 DY 0R2J-2-GP EC_RESET_OUT (37,41)

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

RN3902 SRN10KJ-5-GP
0226-1
THERM_POWER_OK#
THERMTRIP#
R3906 DY 0R2J-2-GP H_THERMTRIP# (10,21,37,42,82)

R3905 DY 10KR2J-3-GP EMC2102_SHDN
R3907 DY 10KR2J-3-GP EMC2102_FAN_mode
R3910 0R0402-PAD

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

THERM_SYS_SHDN#
R3908 10KR2J-3-GP
THERMAL_P_HW_SHT
1119-1
+KBC_PWR
R3909 10KR2J-3-GP
Q3902 2N7002A-7-GP
PURE_HW_SHUTDOWN# (37,42)

V_DEGREE
C3908 SCD1U10V2KX-5GP
R3911 10KR2F-2-GP
TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)
T8 shutdown is 88 deg-C.
C3909 SCD1U10V2KX-5GP
R3912 2K37R2F-GP

32K suspend clock output

Q3903 2N7002A-7-GP
(20) RTC_CLK
CLK_32K_R
R3913 10R2J-2-GP
CLK_32K
C3911 DY SC4D7P50V2CN-1GP
(42) RUN_ENABLE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102
Size: A3
Document Number: Berry AMD Discrete/UMA
Rev: A00
Date: Thursday, March 04, 2010
Sheet 39 of 95

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<Core Design>

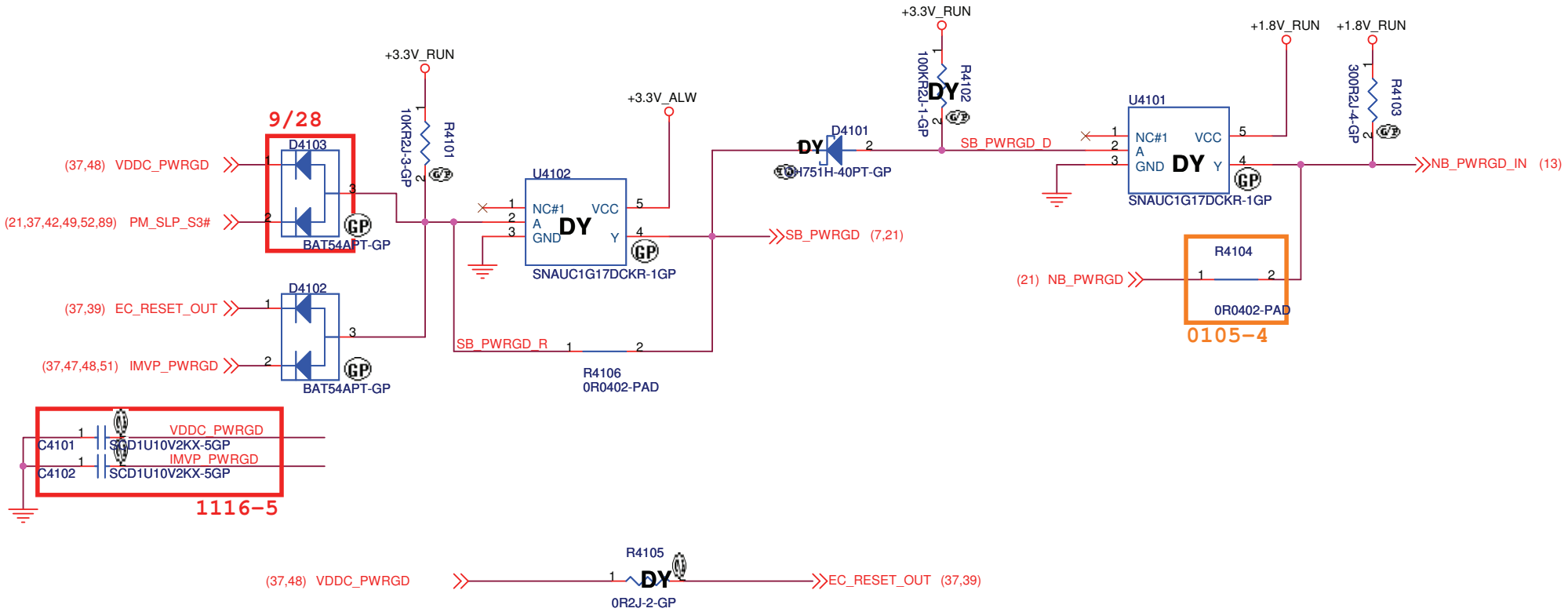
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

Date: Thursday, March 04, 2010 | Sheet 40 of 95

SSID = Reset.Suspend



<Core Design>

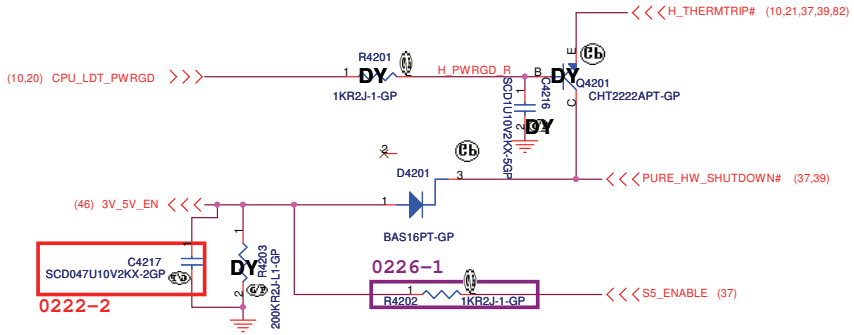
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power On Logic***

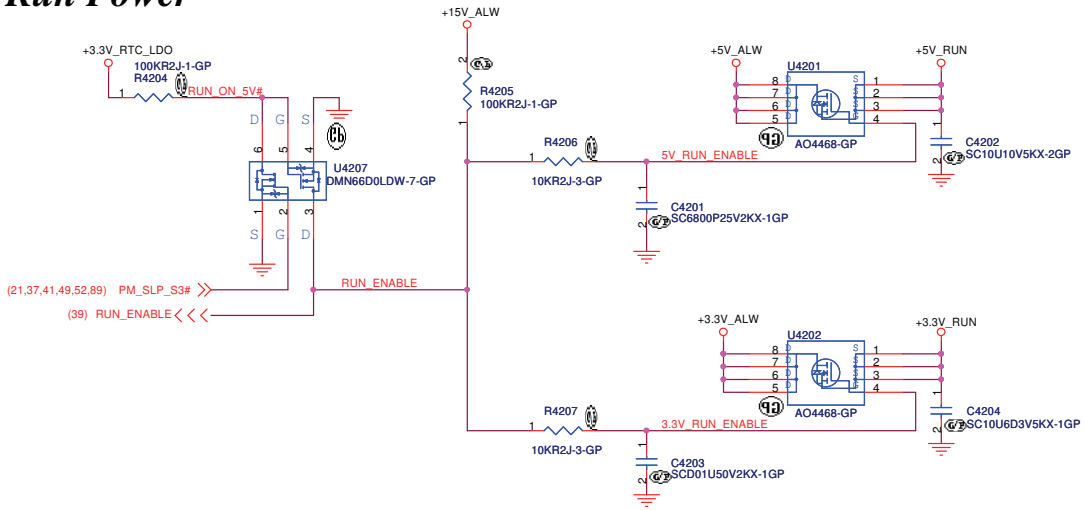
Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

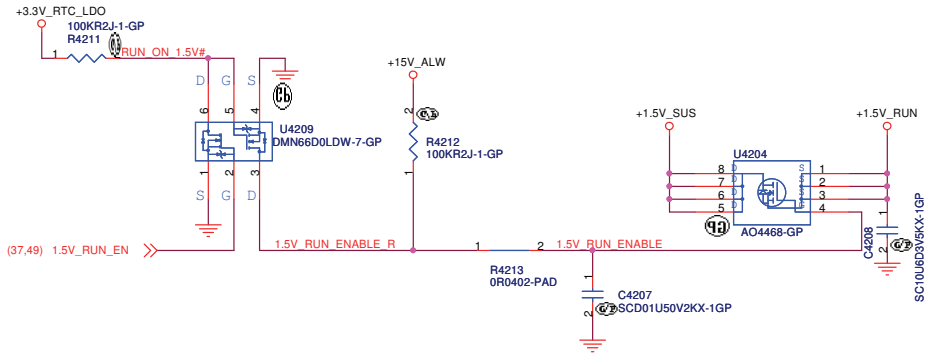
Date: Thursday, March 04, 2010 Sheet 41 of 95

SSID = Reset.Suspend

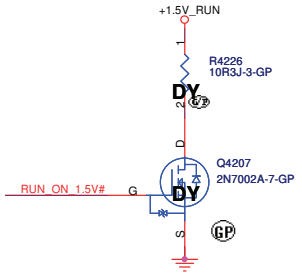


Run Power





1117-2
Remove



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 42 of 95

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

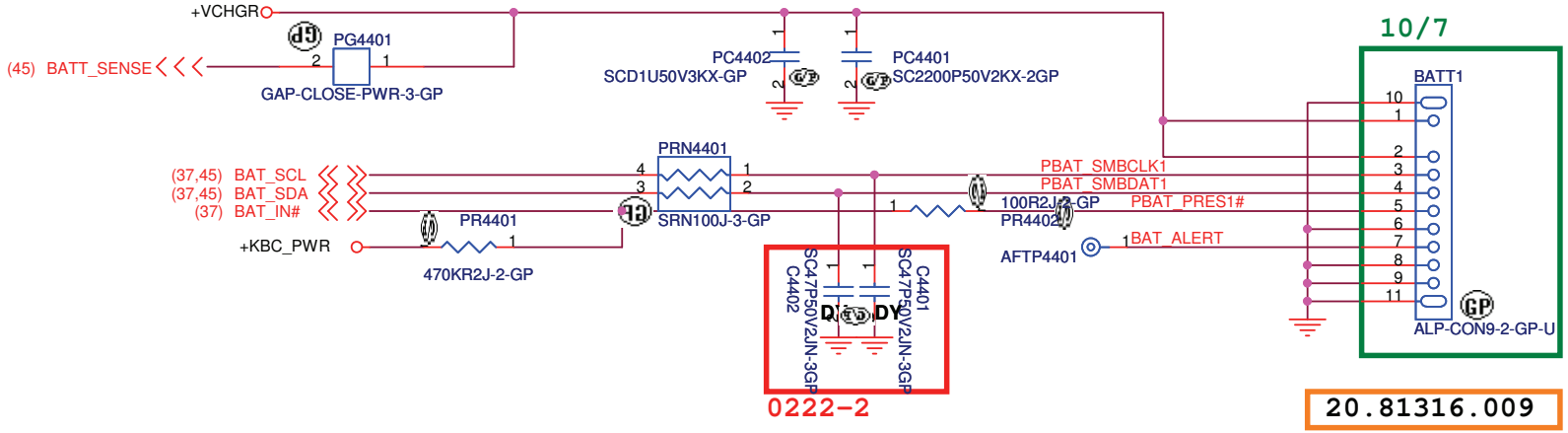
Title: Reserved

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 43 of 95

SSID = BATT CONN

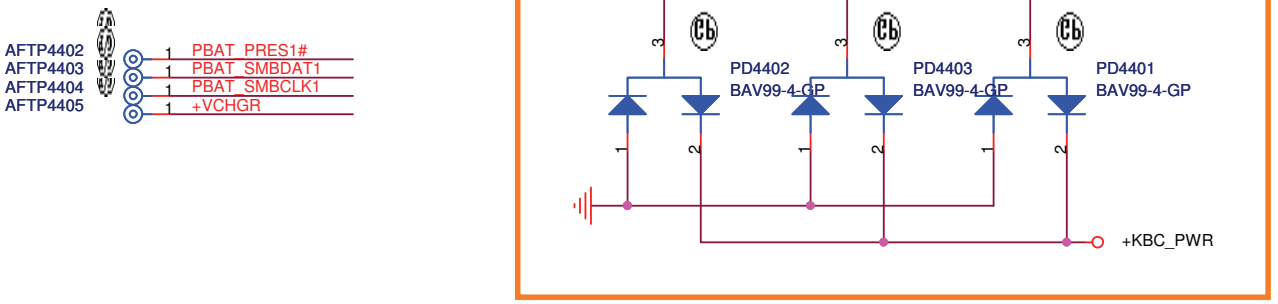
Batt Connecter



20.81316.009

For actual location, need to be swap all pin

Close to Batt Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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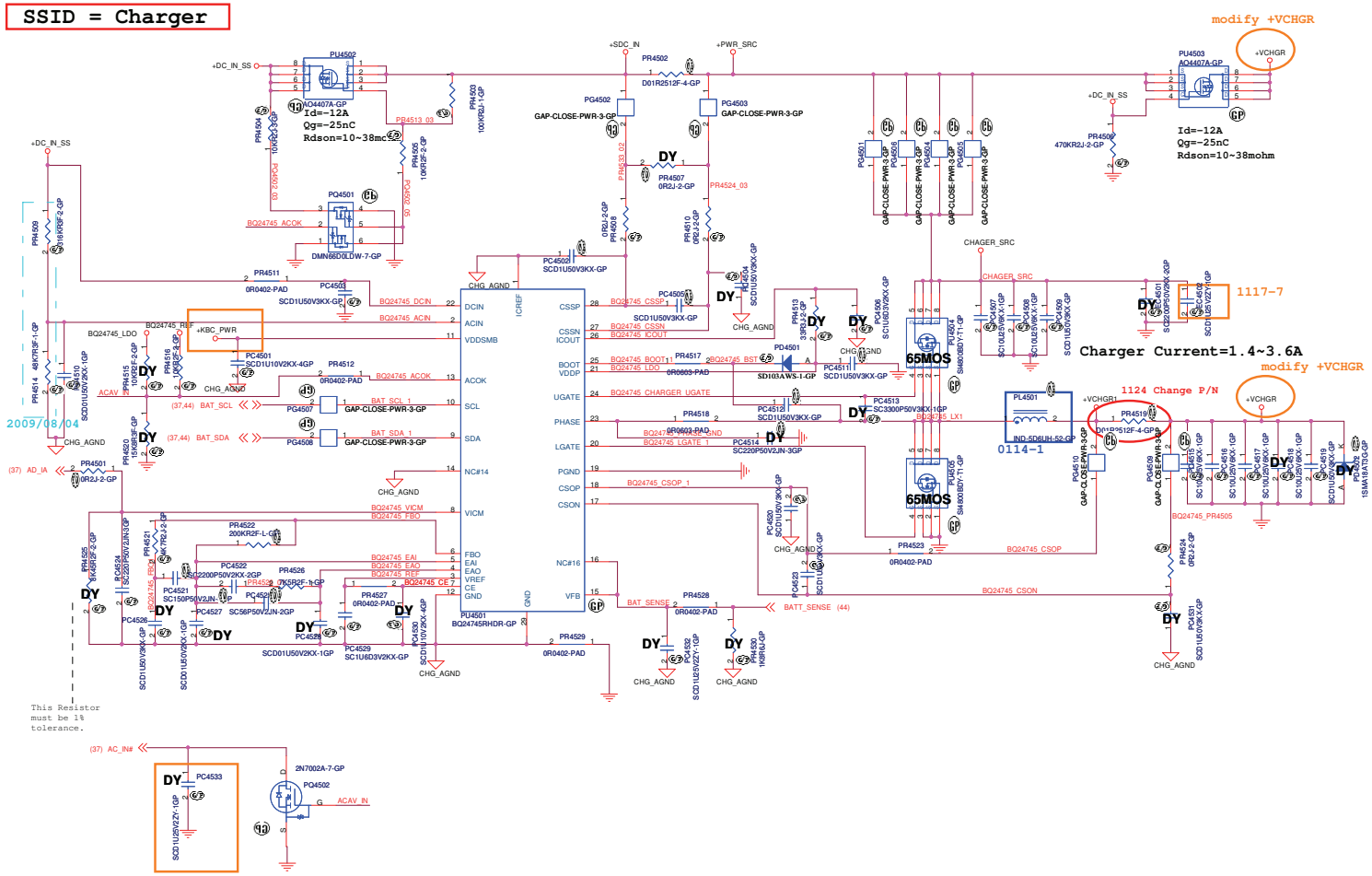
Title	BATT CONN	
Size: A4	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 44 of 95	

SSID = Charger



<Core Design>

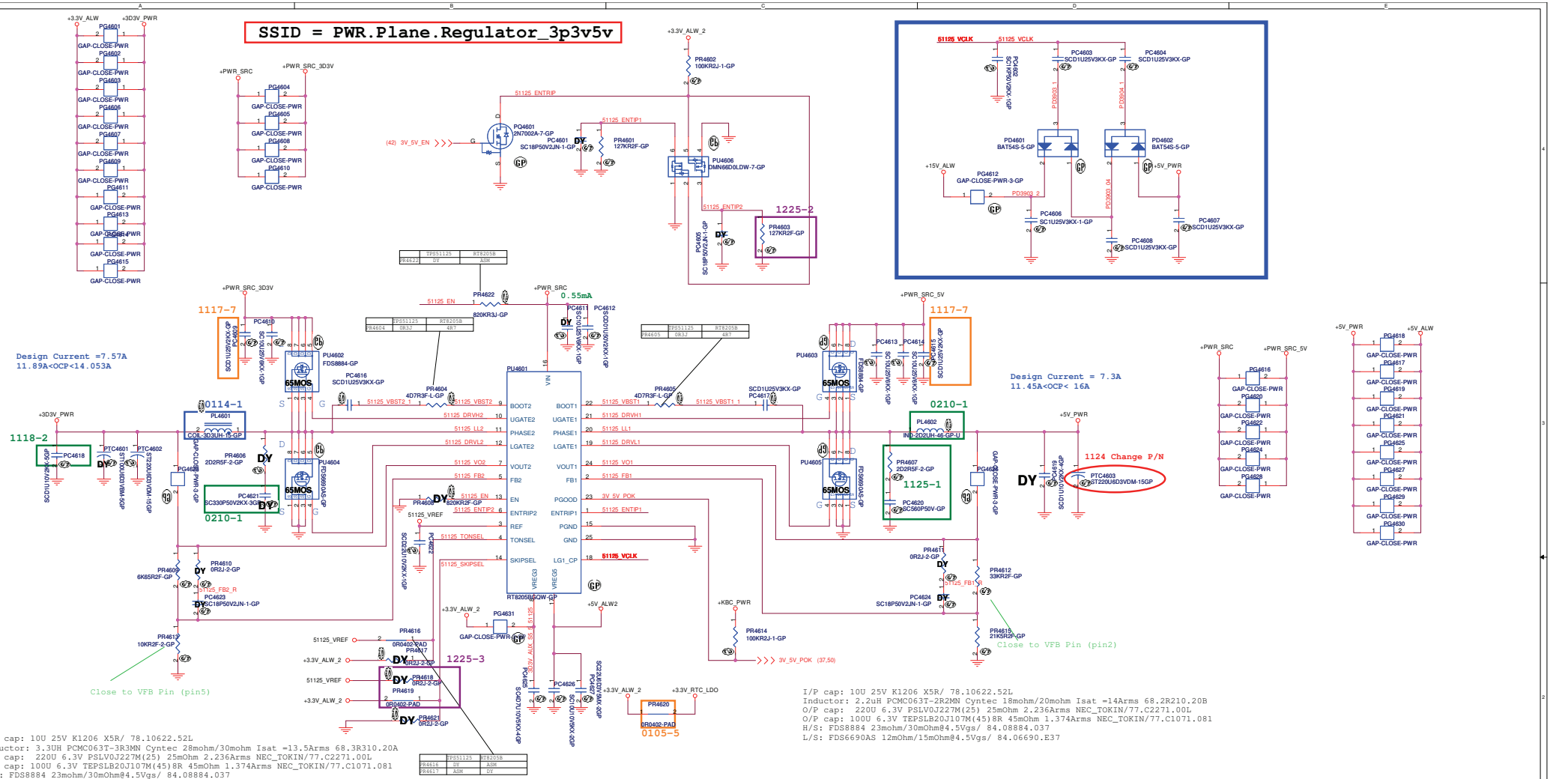
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size	Document Number	Rev
A2	Berry AMD Discrete/UMA	A00

Date: Monday, March 08, 2010 Sheet 45 of 85

SSID = PWR.Plane.Regulator_3p3v5v



TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B(74.08208.A73):

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

TPS51125	74.51125.073
RT8208BGQW	74.08208.A73

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205B_5V/3D3V

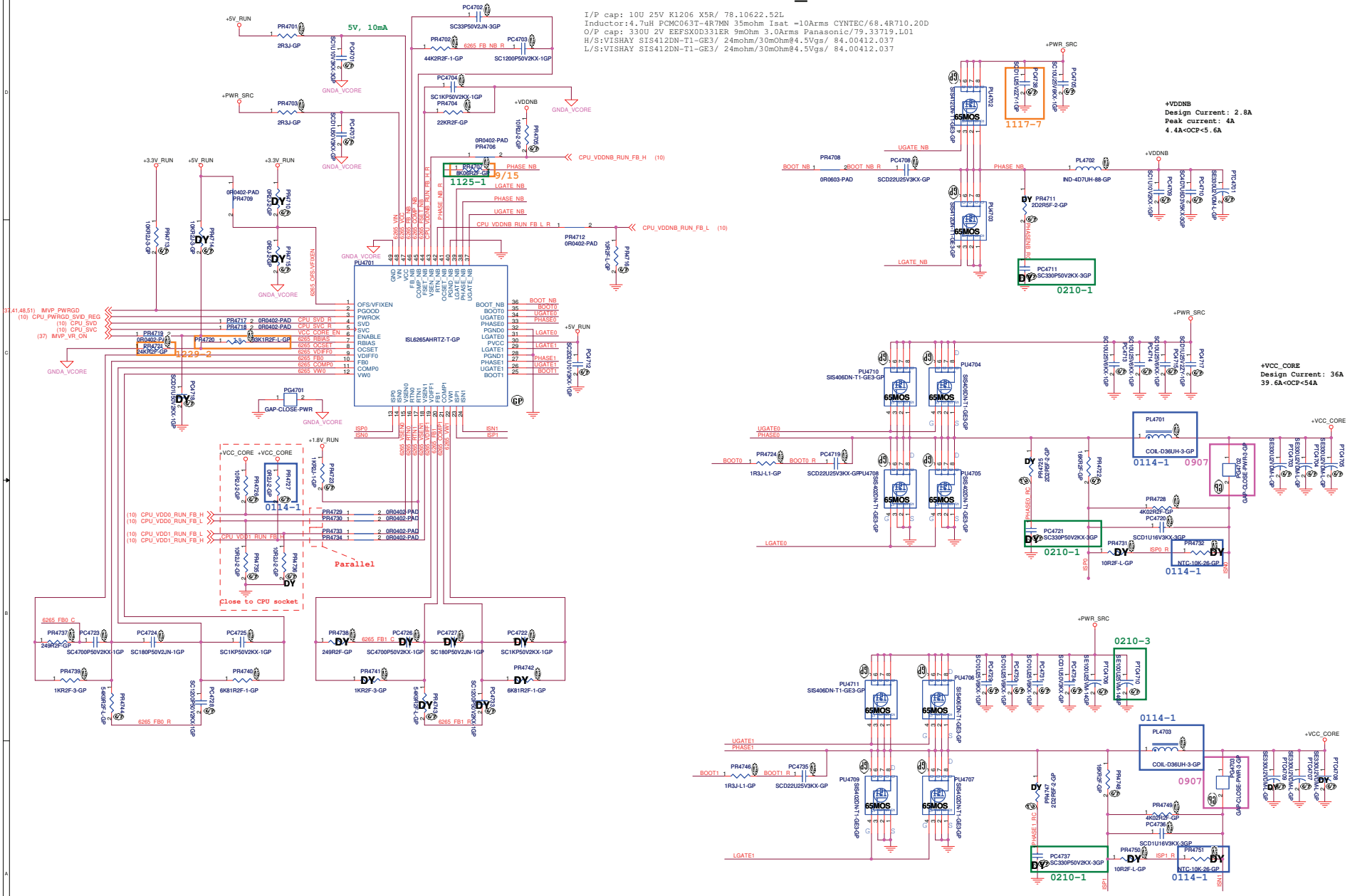
Size: A2 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 46 of 95

SSID = CPU.Regulator

ISL6265HRTZ-T for +VCC_CORE&+VDDNB

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:4.7uH PCMC063T-4R7MN 35mohm Isat =10Arms CYNTEC/68.4R710.20D
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S:VISHAY SiR462DP/ POWERPAK-8.2/810mOhm/ 4.5Vgs/ 84.00462.037
L/S:VISHAY SI7658ADP/ POWERPAK-2.3/ 2.8mOhm/ 4.5Vgs/ 84.07658.037

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +VCC_CORE&+VDDNB

Size	Document Number	Rev
A2	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 47 of 85

SSID = PWR.Plane.Regulator_+1.1V_RUN

1117-2

RT8209EGQW for +1.1V_RUN

0222-3 Remove

PWM TYPE	PRa	PRb
*RT8209B	10 ohm	4.7 ohm
~~TPS51117~~	300 ohm	0 ohm

*DEFAULT

PRa

PRb

5V, 1.25mA

PU4801 RT8209EGQW-GP

0222-3

1119-2

0114-1

0308-1

0210-1

Design Current = 7.4A
11.65A<OCP < 15.89A

Close to VFB Pin (pin5)

Vout=0.75V*(R1+R2)/R2

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN 33Arms CYNTEC/ 68.1R510.10J
O/P cap: 330U 2.5V EEFCX0E331QR 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR164DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

<Core Design>

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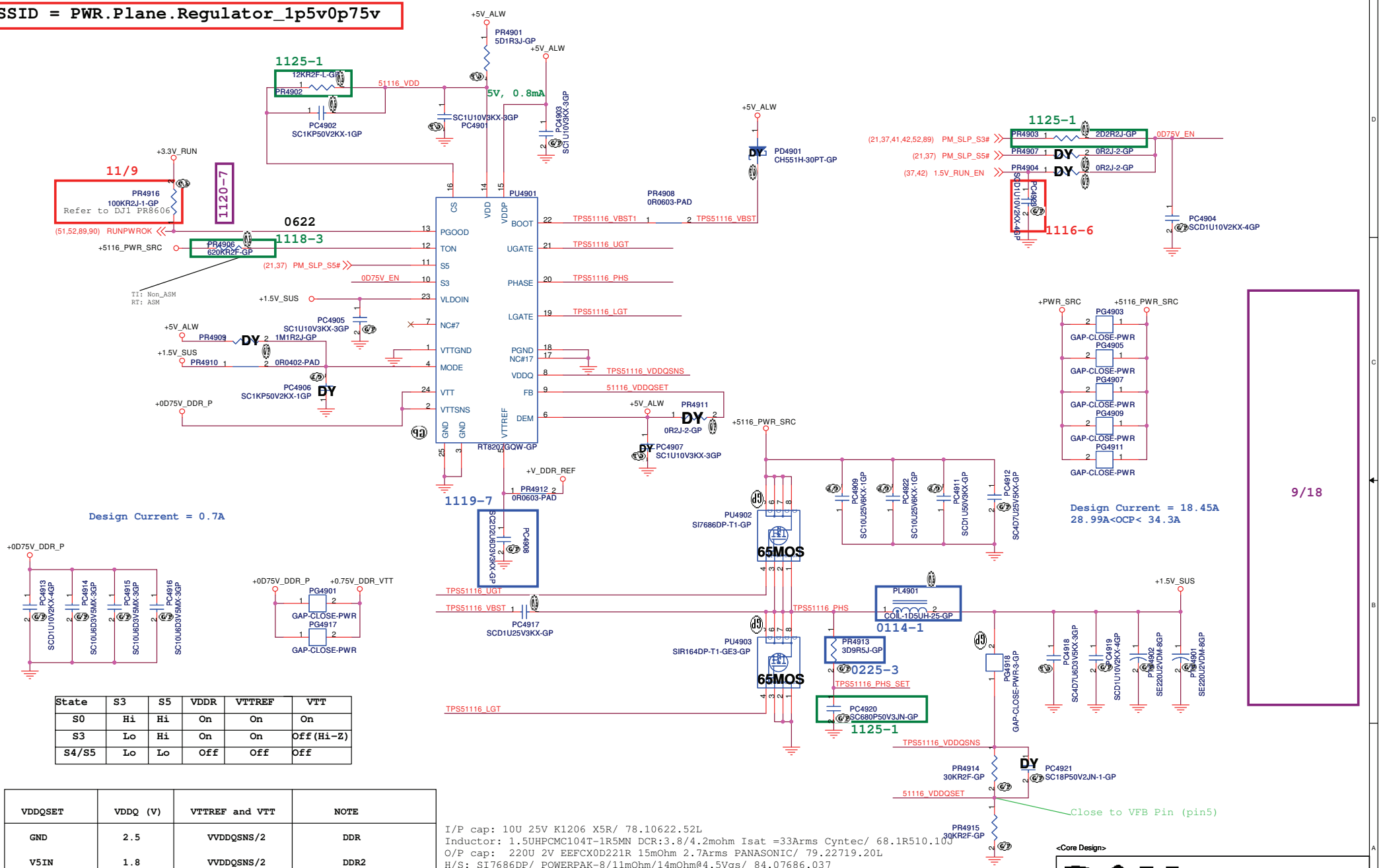
Title		
RT8209E_+1.1V_RUN		
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Monday, March 08, 2010	Sheet 48 of 95	

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10J
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR164DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

<Core Design>

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Title: RT8207_+1.5V_SUS

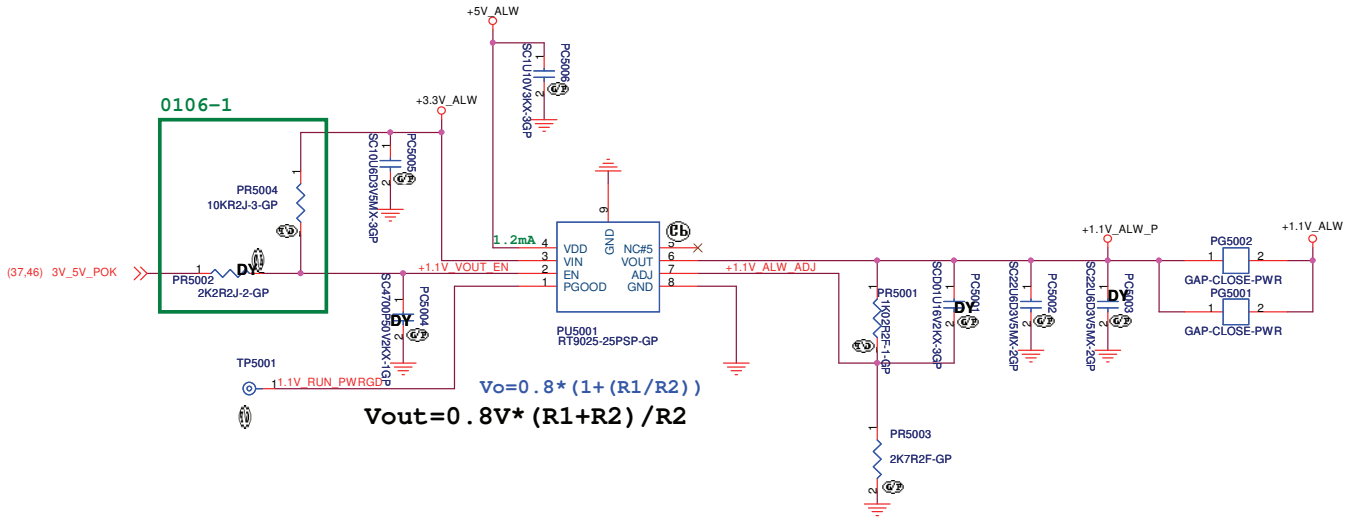
Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 49 of 95

SSID = PWR.Plane.Regulator_+1.1V_ALW

1117-2

RT9025 for +1.1V_ALW



<Core Design>

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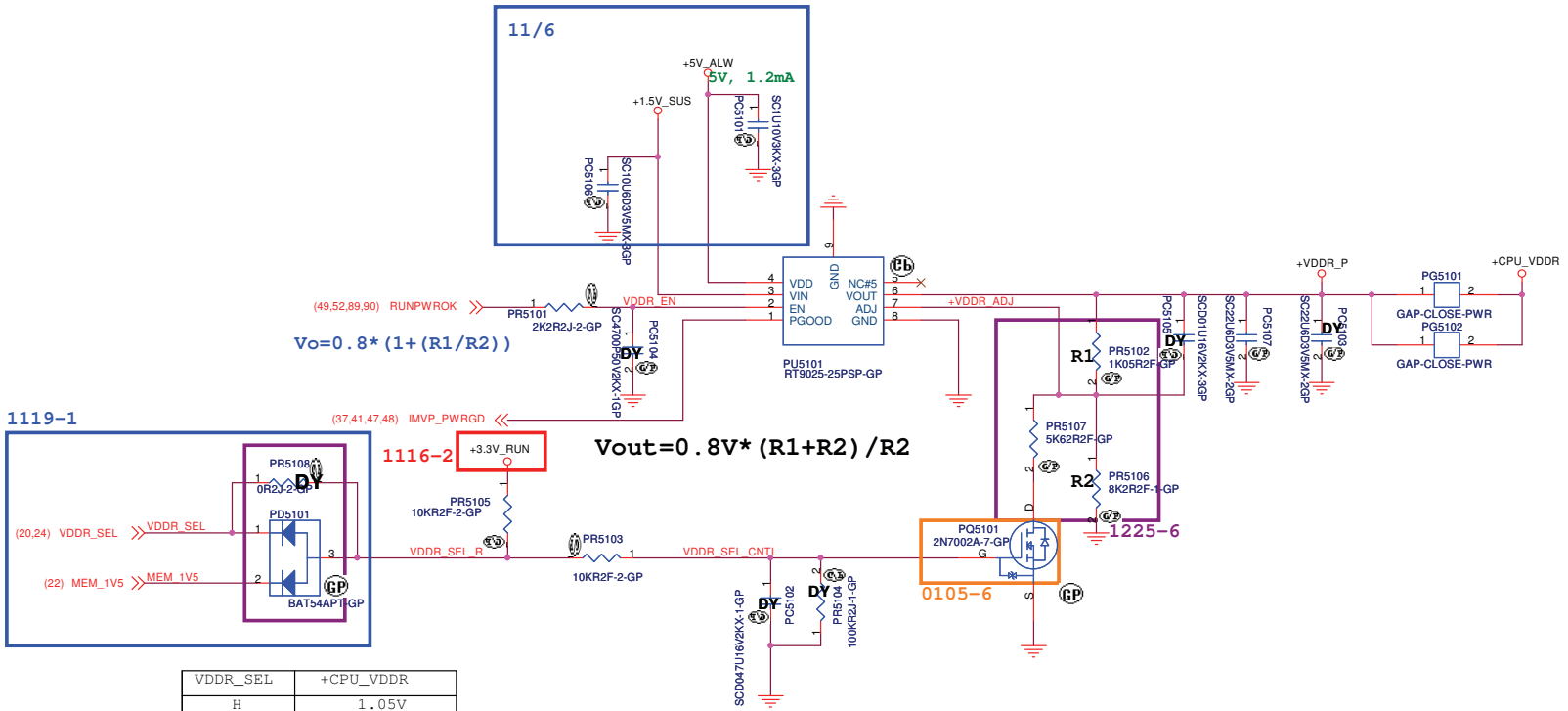
Title: RT9025_+1.1V_ALW

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 50 of 95

SSID = PWR.Plane.Regulator_VDDR

RT9025 for +VDDR



+1.5V_RUN +/- 5%
Design Current: 0.805A
Peak current 1.15A

VDDR_SEL	+CPU_VDDR
H	1.05V
L	0.9V

10/2

<Core Design>

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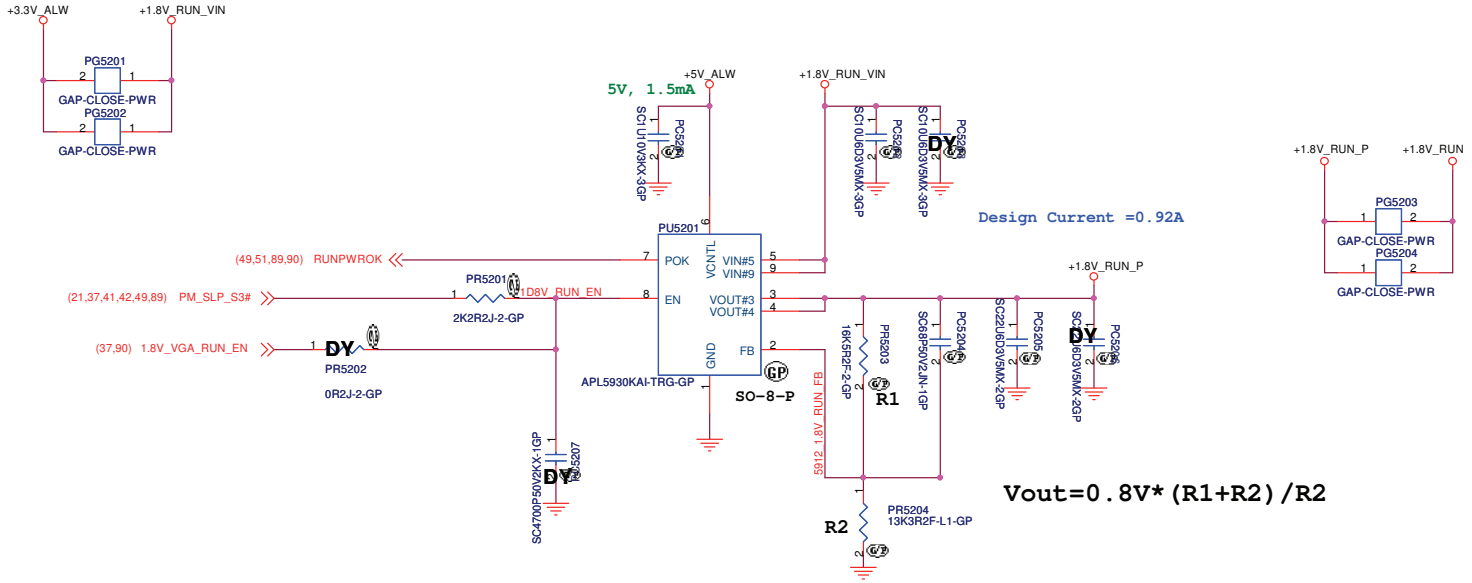
Title		
RT9025 +VDDR		
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 51 of 95	

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



SSID = PWR.Plane.Regulator_1p8v

<Core Design>

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Title: APL5930_+1.8V_RUN

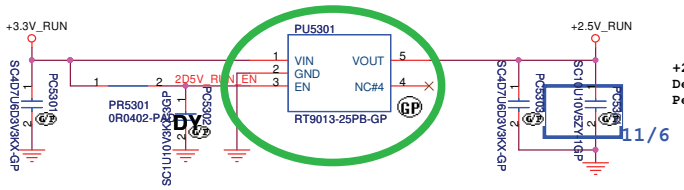
Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 52 of 95

SSID = PWR.Plane.Regulator_0P9v

SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN



+2.5V_RUN +/- 5%
Design Current: 175mA
Peak current 250mA

CHECK CURRENT IS ENOUGH OR NOT (CPU)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

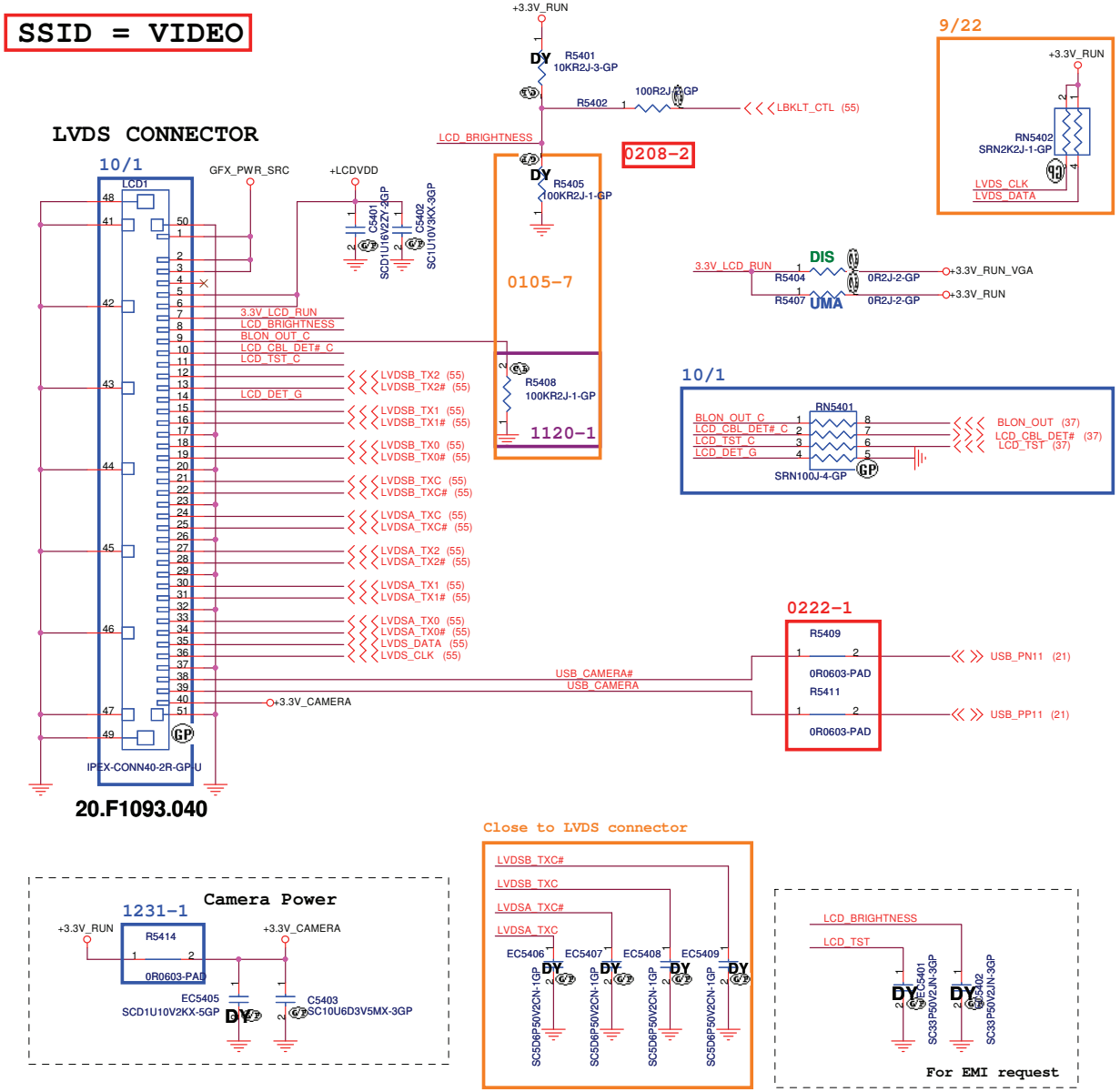
Title: VREG : +CPU_VDDR&+2.5V_RUN

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 53 of 95

SSID = VIDEO

LVDS CONNECTOR



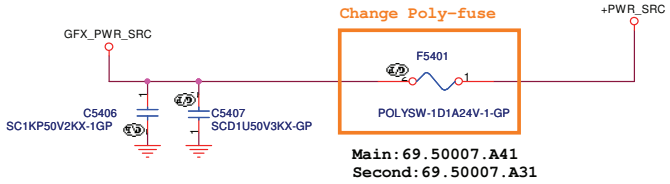
20.F1093.040

Camera Power

Close to LVDS connector

SSID = Inverter

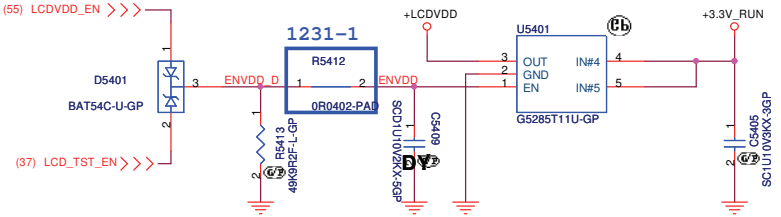
INVERTER POWER



Main:69.50007.A41
Second:69.50007.A31

SSID = VIDEO

LCD POWER



<Core Design>

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Title	LCD/Inverter Connector	
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 54 of 95	

SSID = VIDEO

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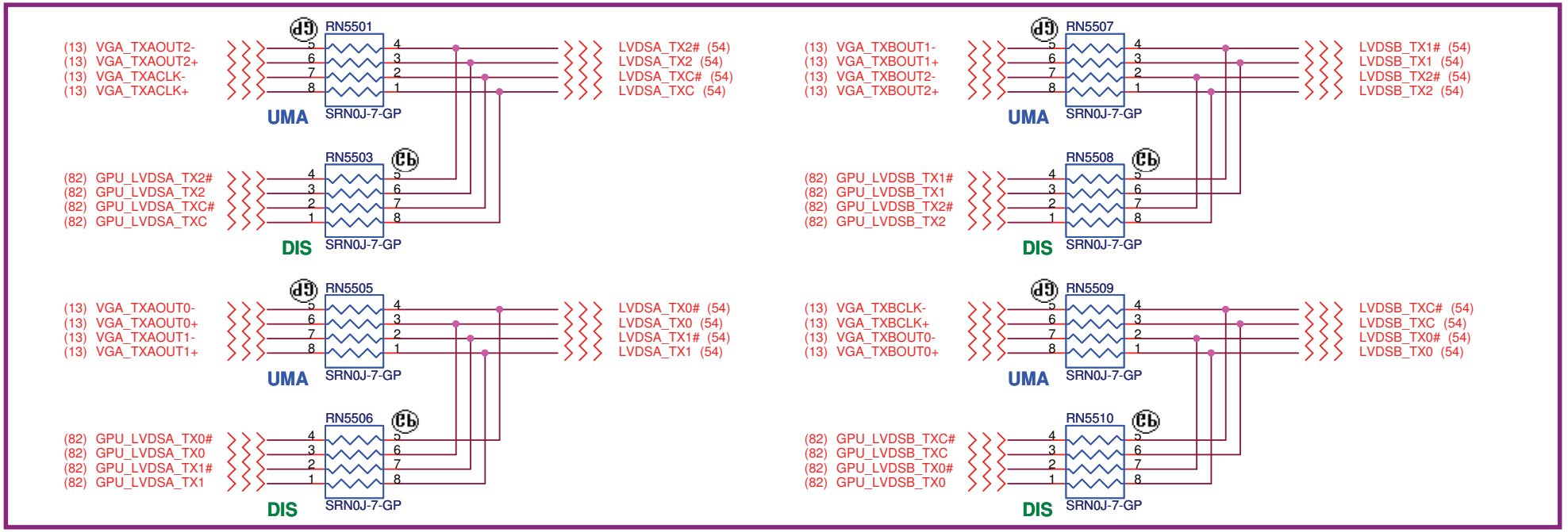
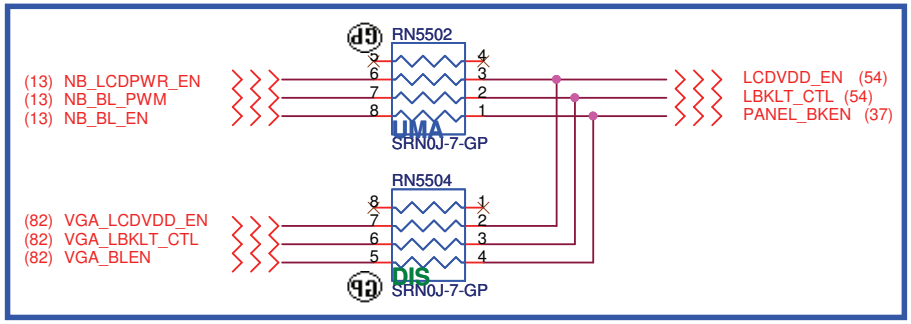
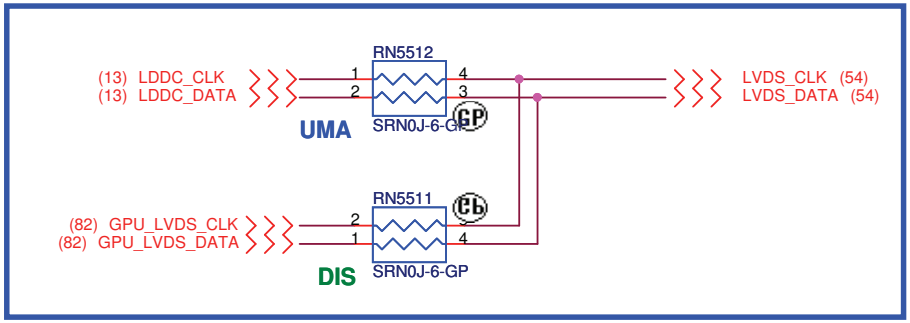


10/1



10/1



<Core Design>

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Title: ***LVDS_Switch***

Size	Document Number	Rev
	Berry AMD Discrete/UMA	***A00***

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 56 of 95

SSID = VIDEO

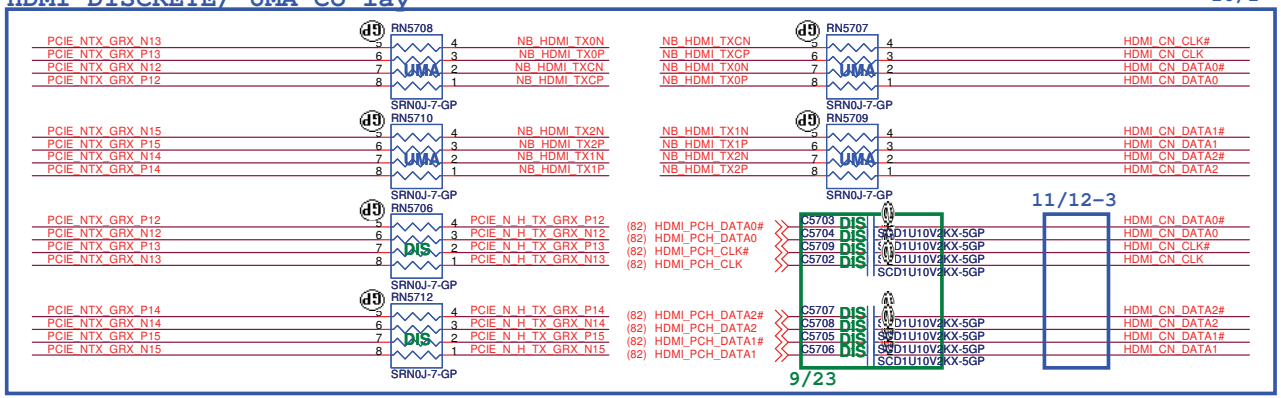
HDMI CONNECTOR

(12) PCIE_NTX_GRX_P[12..15] >>> PCIE_N_H_TX_GRX_P[12..15] (80)

(12) PCIE_NTX_GRX_N[12..15] >>> PCIE_N_H_TX_GRX_N[12..15] (80)

HDMI DISCRETE/ UMA Co-lay

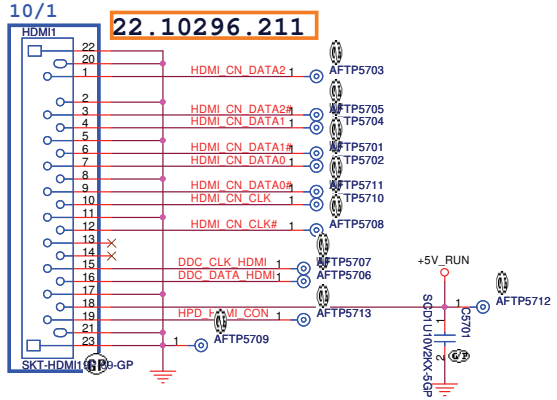
10/1



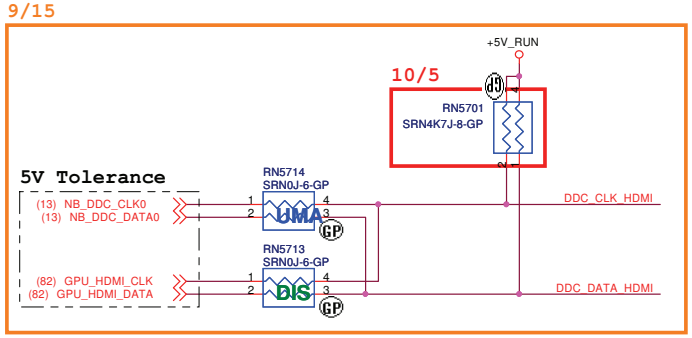
HDMI CONN

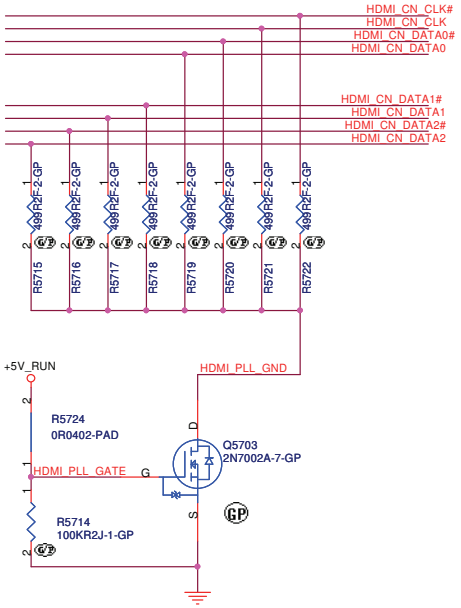
10/1

22.10296.211

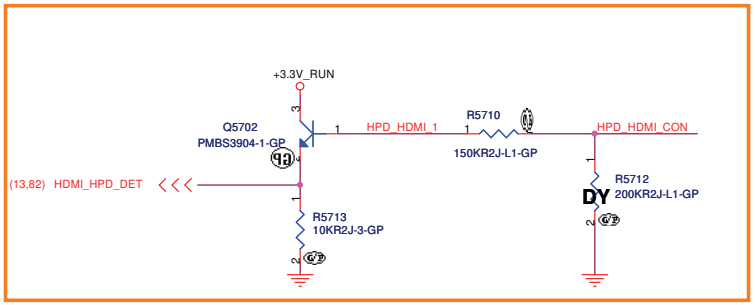


9/15





9/22



<Core Design>

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Title: HDMI Level Shifter/Connector

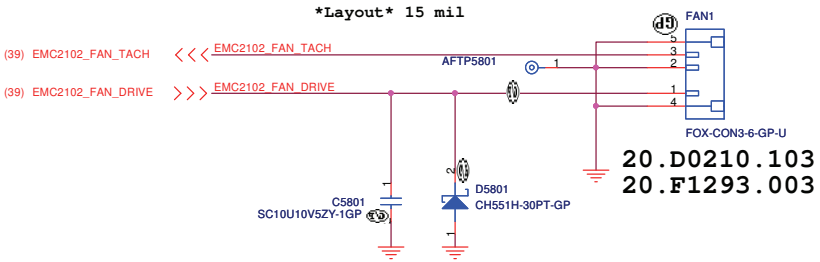
Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

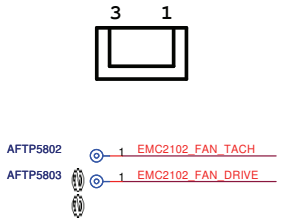
Date: Thursday, March 04, 2010 Sheet 57 of 95

SSID = User.Interface

SSID = Thermal

Fan Connector





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP/Fan Connector

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

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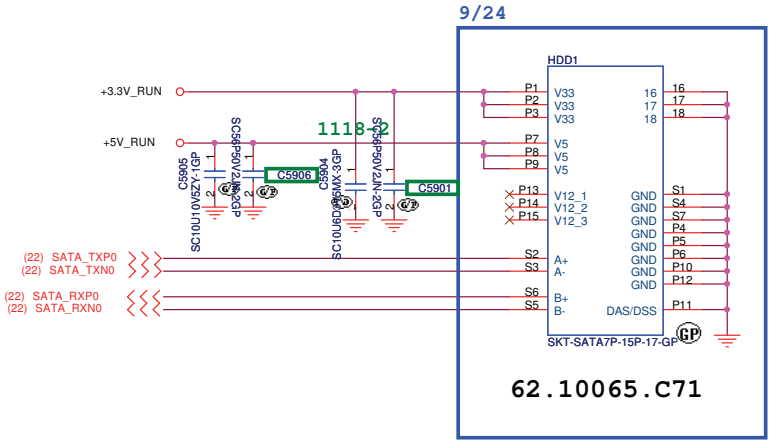
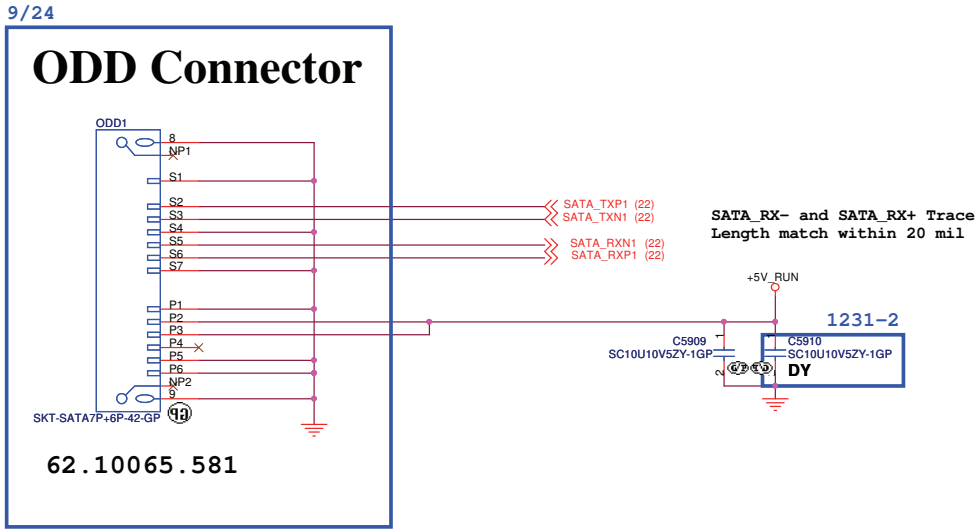
SSID = SATA

SATA HDD Connector



ODD Connector



<Core Design>

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Title: HDD/ODD

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

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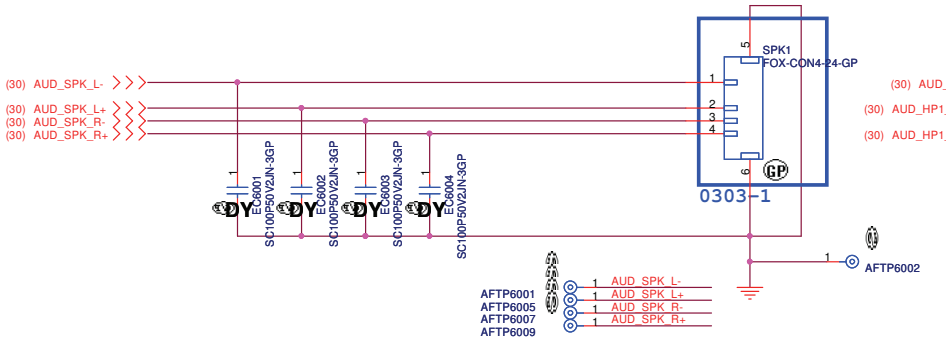
SSID = AUDIO

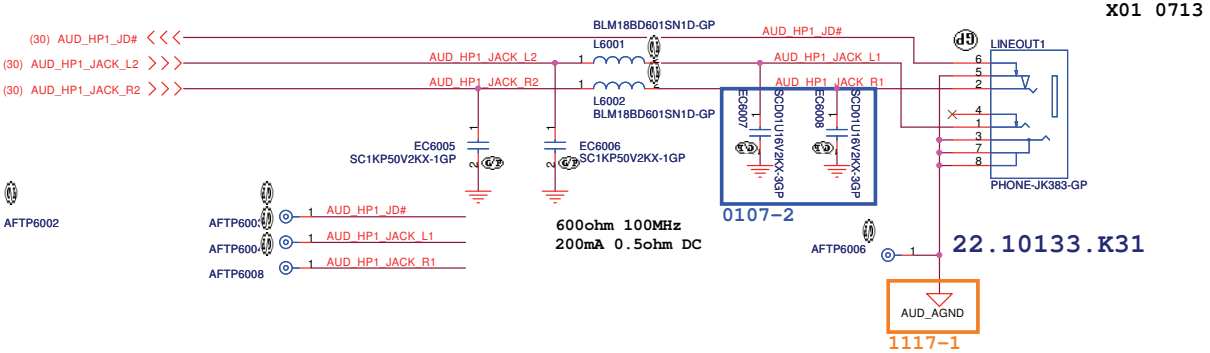
Speaker Connector

Main 20.F0693.004
SEC. 20.F0693.004

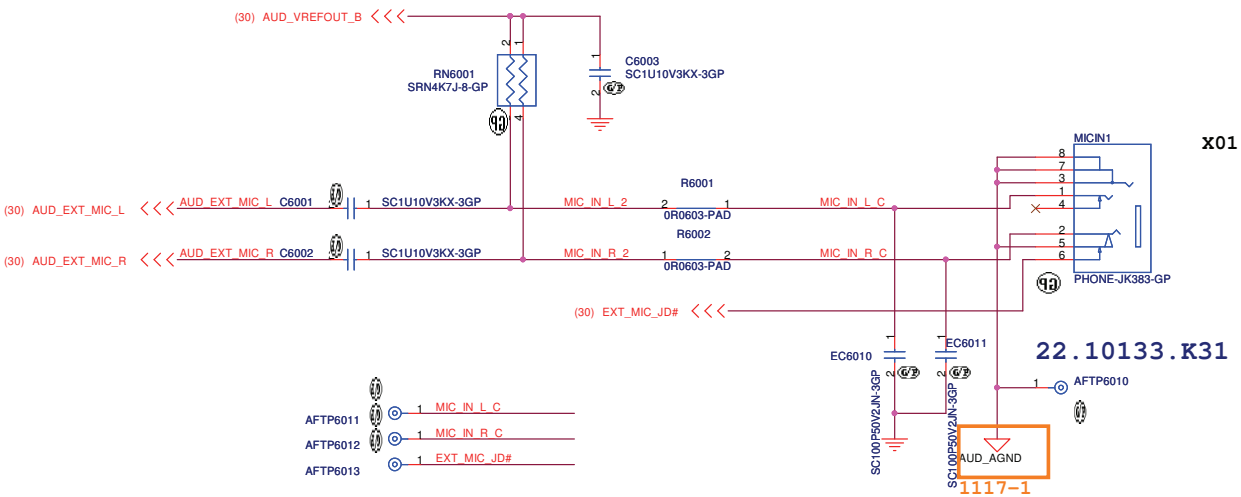


LINE1 OUT

X01 0713



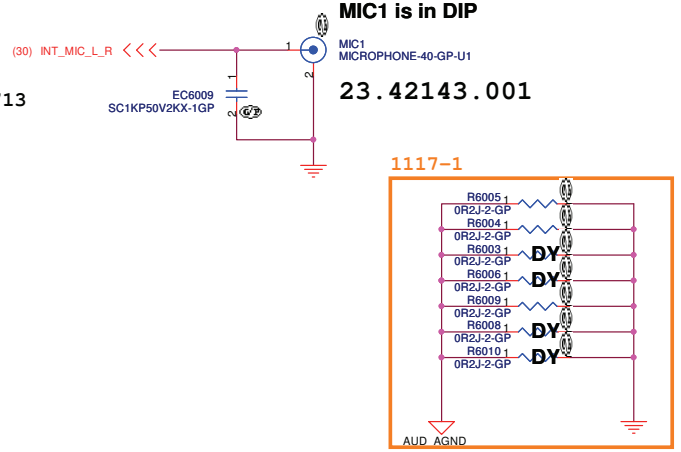
MIC IN



X01 0713

Internal Microphone

MIC1 is in DIP



<Core Design>

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Title		
Audio Jack		
Size: A3	Document Number: Berry	Rev: A00
Date: Thursday, March 04, 2010	Sheet 60 of 95	

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<Core Design>

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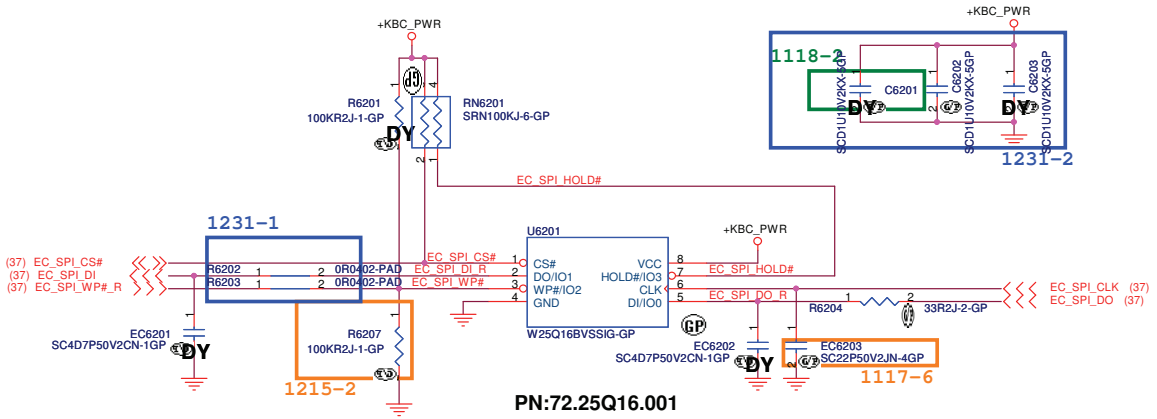
Title: Reserved

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 61 of 95

SSID = Flash.ROM

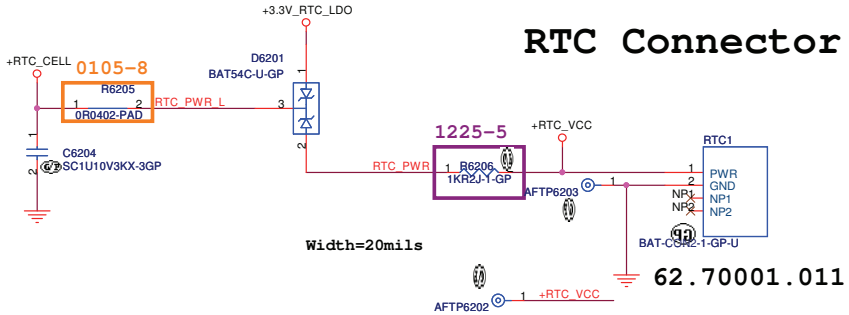
SPI FLASH ROM (16M bits) for KBC



PN:72.25Q16.001

SSID = RBATT

RTC Connector



62.70001.011

<Core Design>

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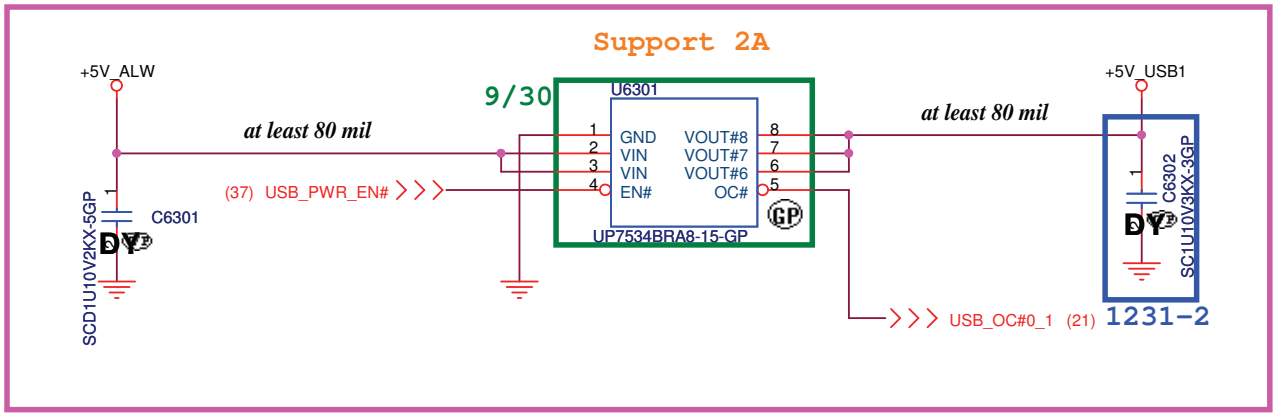
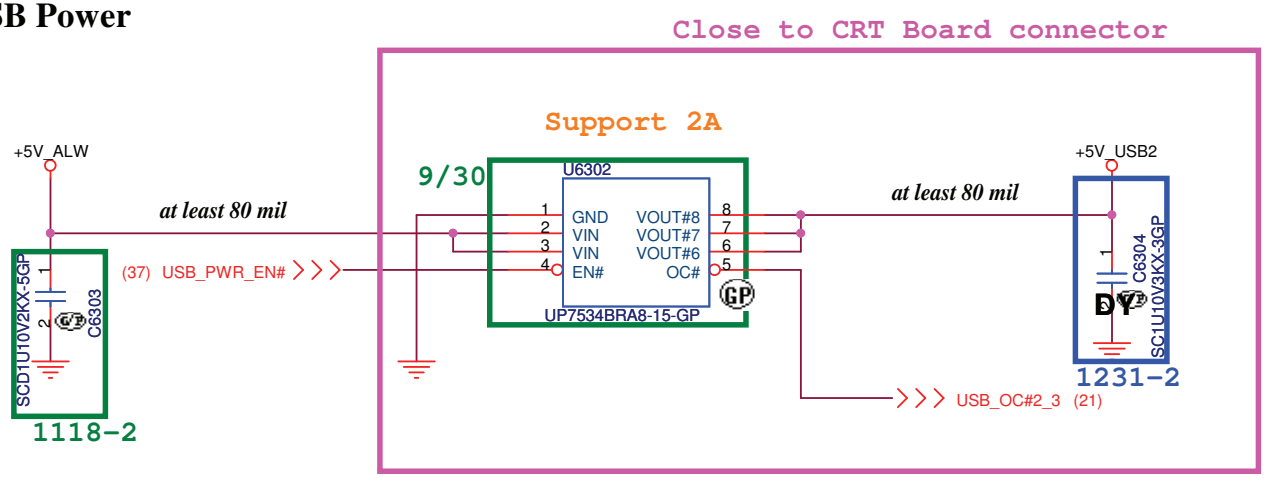
Title	Flash/RTC	
Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 62 of 95	

SSID = USB

IO Board USB Power



CRT Board USB Power



<Core Design>

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Title: USB Power SW

Size	Document Number	Rev
	Berry AMD Discrete/UMA	A00

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(Blanking)

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
Reserved

Size	Document Number	Rev
A4	Berry AMD Discrete/UMA	A00

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(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

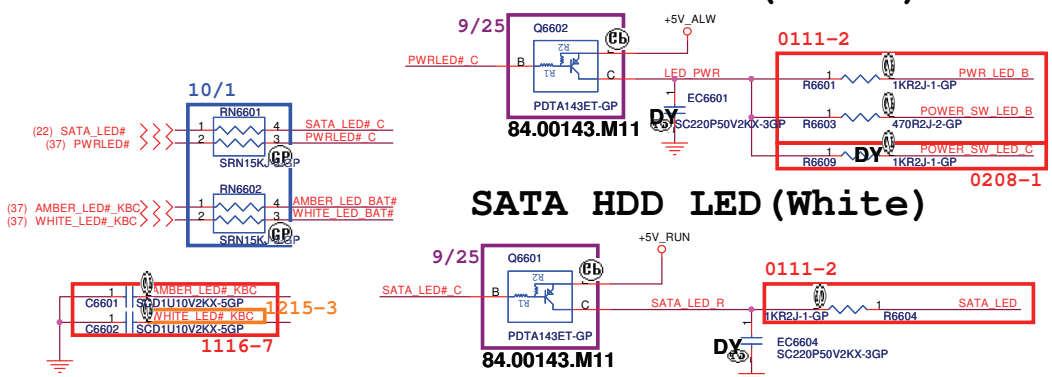
Title: Reserved

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 65 of 95

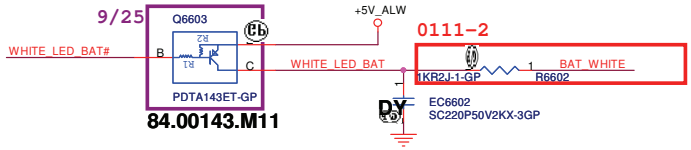
SSID = User.Interface

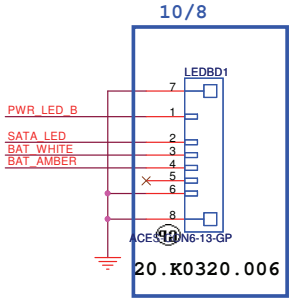
Power LED(White)



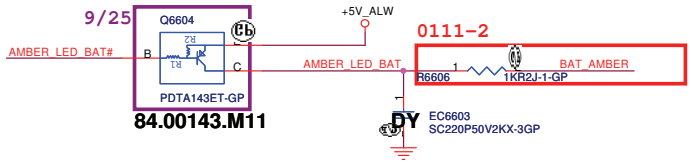
SATA HDD LED(White)

Battery LED1(White)

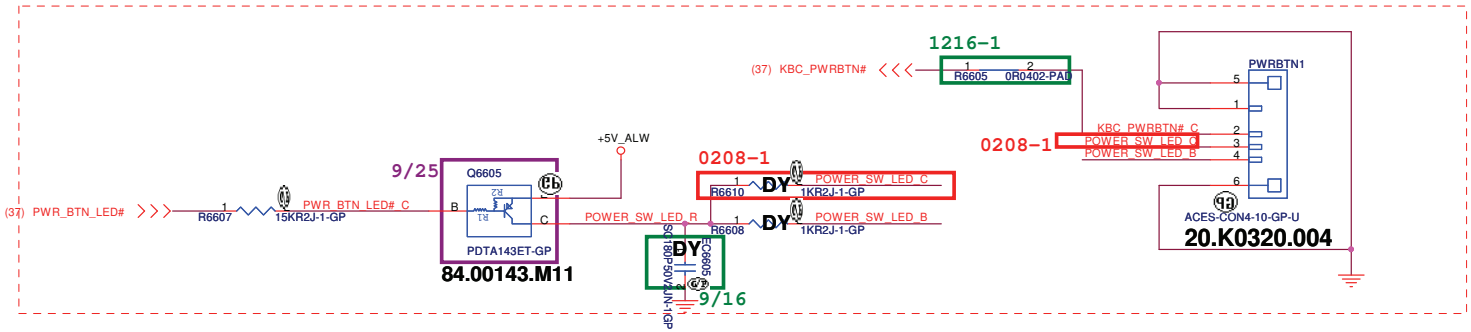




Battery LED2(Amber)



Power button LED(White)



<Core Design>

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Title: LED Bard/Power Button

Size	Document Number	Rev
A3	Berry	A00

Date: Thursday, March 04, 2010 Sheet 66 of 95

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry AMD Discrete/UMA* | Rev: *A00*

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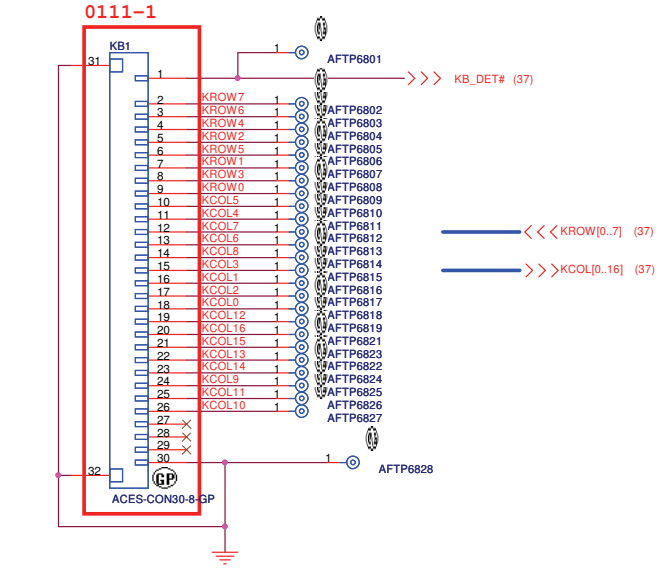
SSID = KBC

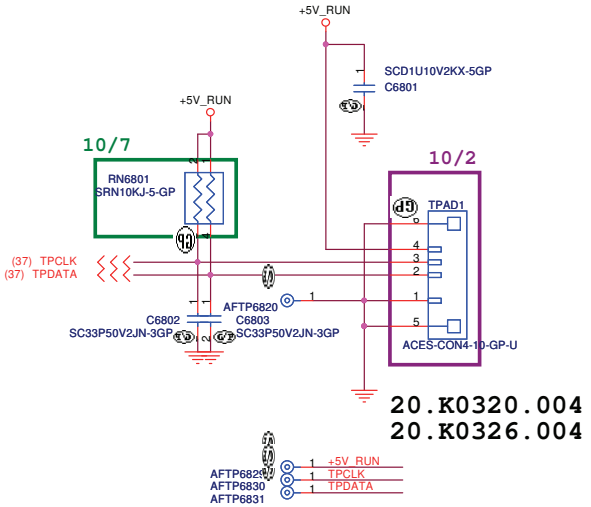
Internal KeyBoard Connector



20.K0524.030
20.K0461.030

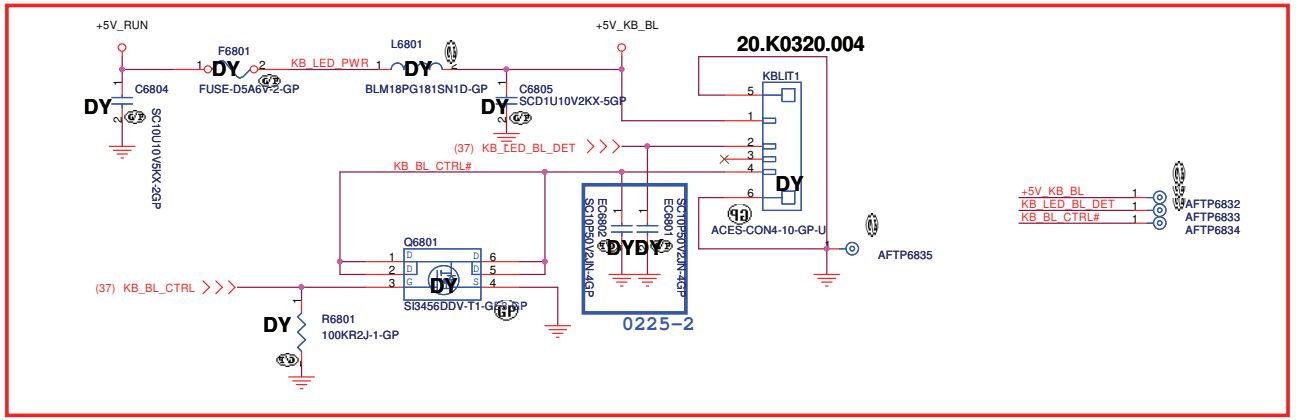
SSID = Touch.Pad

TouchPad Connector



20.K0320.004
20.K0326.004

KB Backlight Connector



<Core Design>

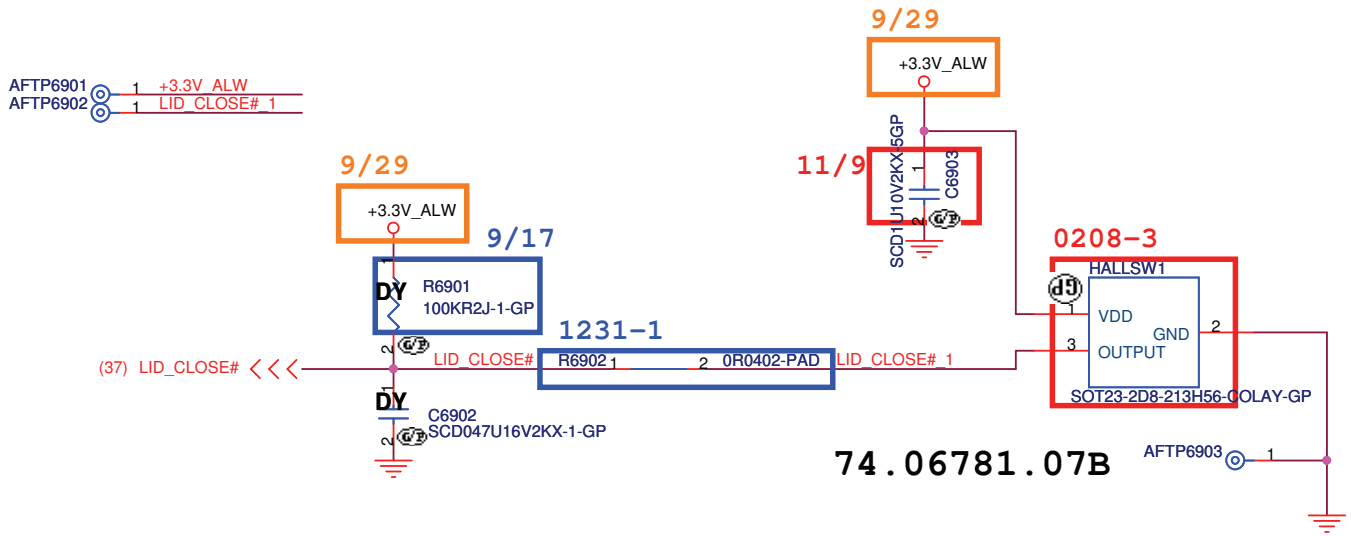
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 68 of 95

SSID = Hall.Sensor



<Core Design>

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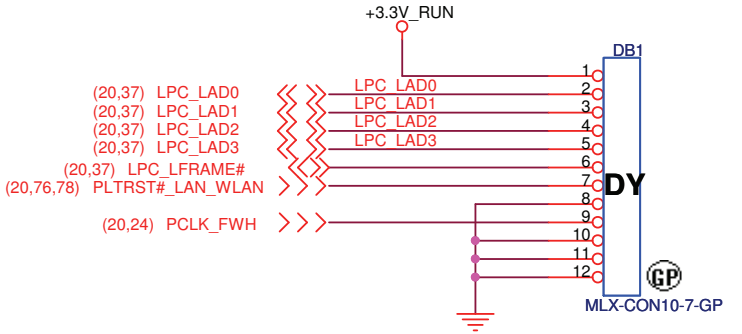
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Effect Sensor***

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 Sheet 69 of 95

SSID = Debug



20.D0183.110

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

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<Core Design>

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Title

RESERVED

Size	Document Number	Rev
A4	Berry AMD Discrete/UMA	A00

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<Core Design>

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Title: RESERVED

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

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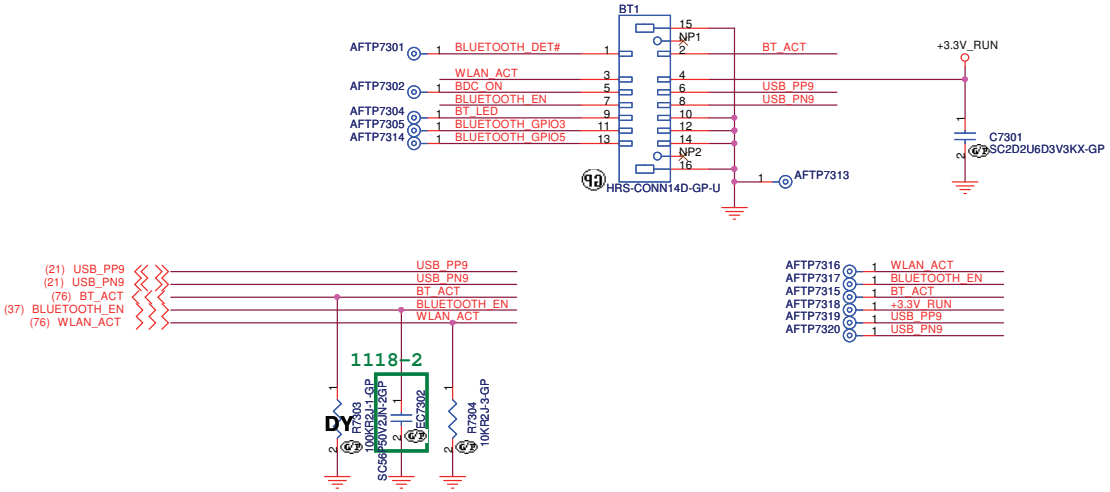
SSID = User.Interface

Bluetooth Module conn.



<Core Design>

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Title		
Bluetooth		
Size: A3	Document Number: Berry	Rev: A00
Date: Thursday, March 04, 2010	Sheet 73 of 95	

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 74 of 95

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<Core Design>

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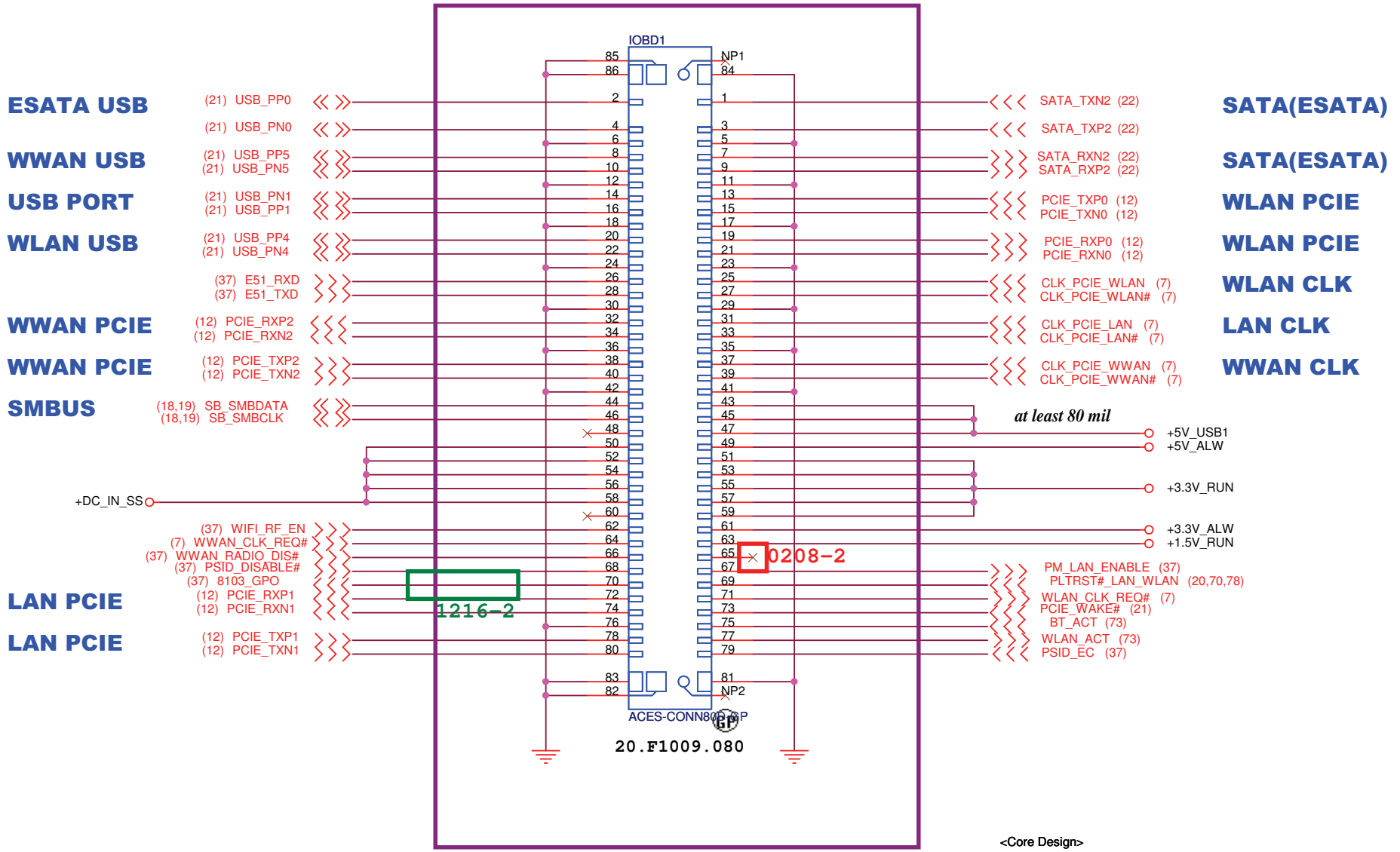
Title: Reserved

Size	Document Number	Rev
A4	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 75 of 95

SSID = Int.Conn

10/9



0107-6

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

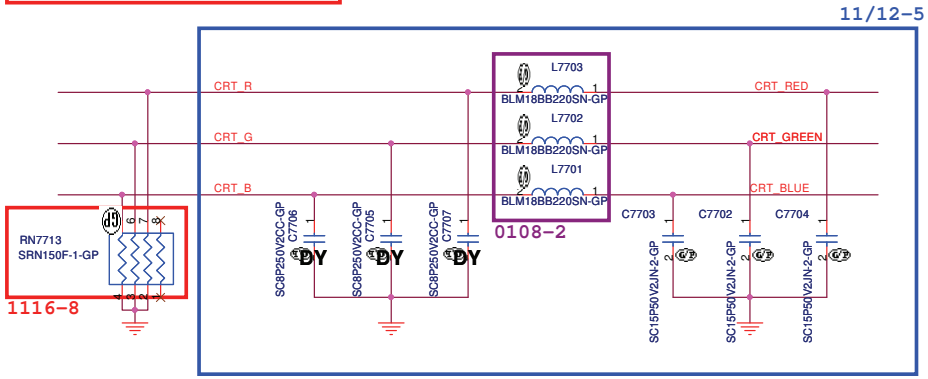
Title: **IO Board Connector**

Size	Document Number	Rev
A4	Berry AMD Discrete/UMA	A00

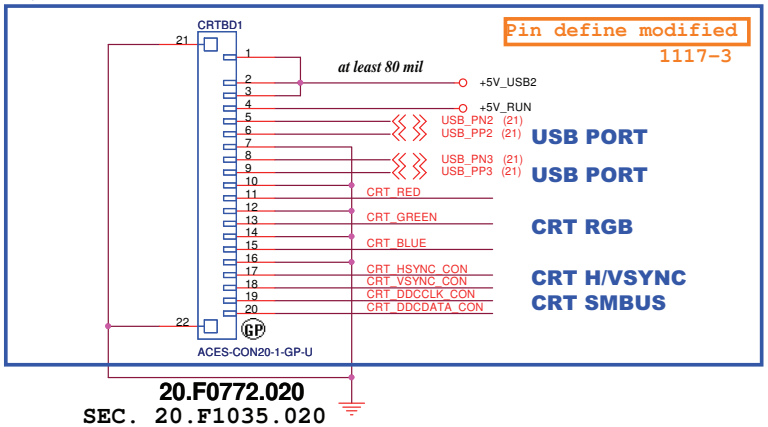
Date: Thursday, March 04, 2010 Sheet 76 of 95

SSID = Int.Conn

11/12-5



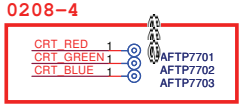
10/1 CRT Board Connector



20.F0772.020

SEC. 20.F1035.020

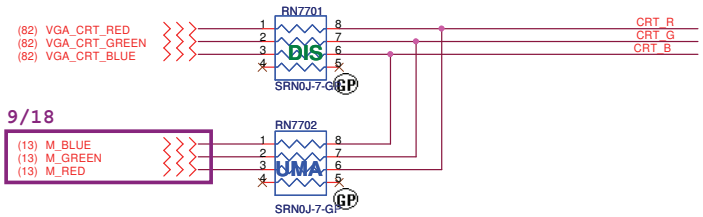
0208-4



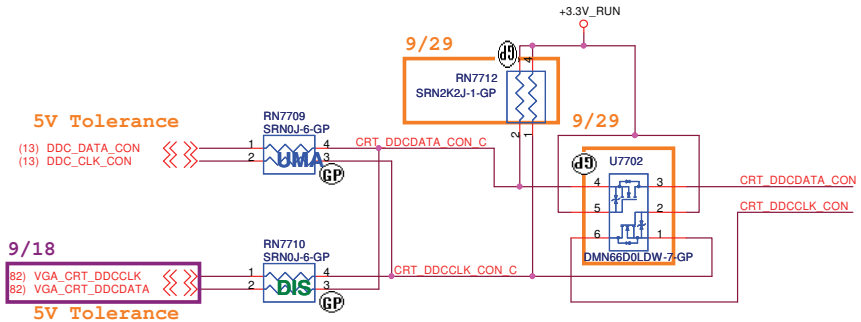
CRT RGB

Close to CRT Board CONN

Filter design on CRT Board



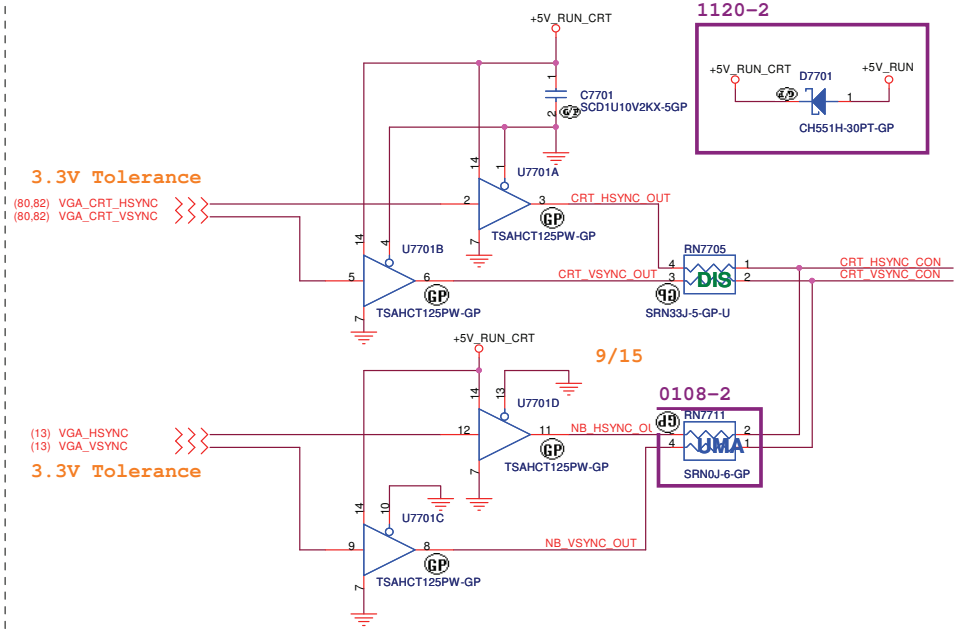
CRT DDCDATA & DDCCLK



Pull High 5V Design on CRT Board

CRT Hsync & Vsync level shift

Close to CRT Board CONN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Board Connector

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

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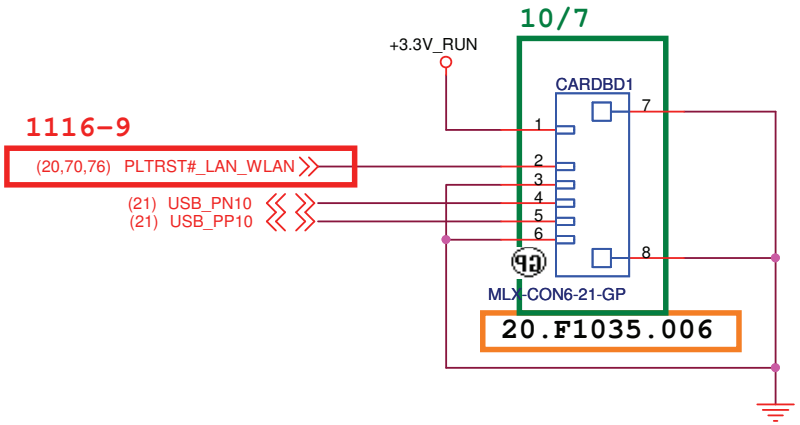
SSID = SDIO

Card Reader connector



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size	Document Number	Rev
A4	Berry AMD Discrete/UMA	A00

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H1 HTE95BE95R29-R-5-GP
H2 HTE95BE95R29-R-5-GP
H3 HTE95BE95R29-R-5-GP
H4 HTE95BE95R29-R-5-GP
H6 HTE95BE95R29-R-5-GP
H7 HTE95BE95R29-R-5-GP
H8 HTE95BE95R29-R-5-GP
H9 HTE95BE95R29-R-5-GP
H5 HOLE256R111-GP
H11 HOLE256R111-GP
H10 HOLE335R115-GP DY

CPU Thermal module hole
HTML1 HOLE197R166-GP DY
HTML2 HOLE197R166-GP DY
HTML3 HOLE197R166-GP DY

GPU Thermal module hole
HGPU1 STF237R117H83-1-GP

0210-2
stand off
HBT1 STF237R117H123-GP

EMI Reserve
+PWR_SRC
EC7901 SCD1U25V2KX-GP
EC7902 SCD1U25V2KX-GP
EC7904 DY SCD1U25V2KX-GP
EC7903 SCD1U25V2KX-GP
EC7905 DY SCD1U25V2KX-GP
EC7906 SCD1U25V2KX-GP

+VGA_CORE
1118-2
EC7907 SCD1U10V2KX-5GP
10/6
+3.3V_RUN
EC7910 DY SCD1U25V2KX-GP
+5V_ALW
EC7911 DY SCD1U25V2KX-GP
EC7912 DY SCD1U25V2KX-GP
10/5
SPR1 SPRING-58-GP DY

EMI Reserve 1117-4
+PWR_SRC
EC7924 DY SC10P50V2JN-4GP
+3.3V_RUN
EC7916 DY SC10P50V2JN-4GP
EC7920 DY SC10P50V2JN-4GP
EC7923 DY SC10P50V2JN-4GP
EC7917 DY SC10P50V2JN-4GP

+3.3V_RUN
EC7922 DY SC10P50V2JN-4GP
+5V_RUN
EC7915 DY SC10P50V2JN-4GP

+5V_RUN
EC7919 DY SC10P50V2JN-4GP
+VCC_CORE
EC7921 DY SC10P50V2JN-4GP

+5V_RUN
EC7914 DY SC10P50V2JN-4GP
+PWR_SRC
EC7913 DY SC10P50V2JN-4GP

+5V_RUN
EC7918 DY SC10P50V2JN-4GP
+1.5V_RUN

1118-2 RF Team Solution
+3.3V_ALW
C7909 DY SC56P50V2JN-2GP
C7906 DY SC56P50V2JN-2GP
+1.5V_RUN
C7905 DY SC56P50V2JN-2GP
C7904 DY SC56P50V2JN-2GP
+5V_RUN
C7902 DY SC56P50V2JN-2GP
C7917 DY SC56P50V2JN-2GP

+15V_ALW
C7907 DY SCD1U25V2KX-GP
C7915 DY SCD1U25V2KX-GP
C7911 DY SCD1U25V2KX-GP
+1.1V_RUN
C7910 DY SC56P50V2JN-2GP
C7908 DY SC56P50V2JN-2GP
+1.8V_RUN
C7919 DY SC56P50V2JN-2GP
+3.3V_RUN
C7920 DY SC56P50V2JN-2GP

0106-3 RF Team Solution
+PWR_SRC
C7922 DY SC56P50V2JN-2GP
+1.5V_SUS
C7921 DY SC56P50V2JN-2GP

0108-1 EMC reserved
+PWR_SRC
EC7927 DY SC56P50V2JN-2GP
+1.5V_SUS
EC7926 DY SC56P50V2JN-2GP
EC7925 DY SC56P50V2JN-2GP

0224-1
+PWR_SRC
EC7930 DY SC56P50V2JN-2GP
EC7931 DY SC56P50V2JN-2GP
0225-5
+DC_IN_SS
EC7928 DY SC56P50V2JN-2GP
+SDC_IN
EC7929 DY SC56P50V2JN-2GP

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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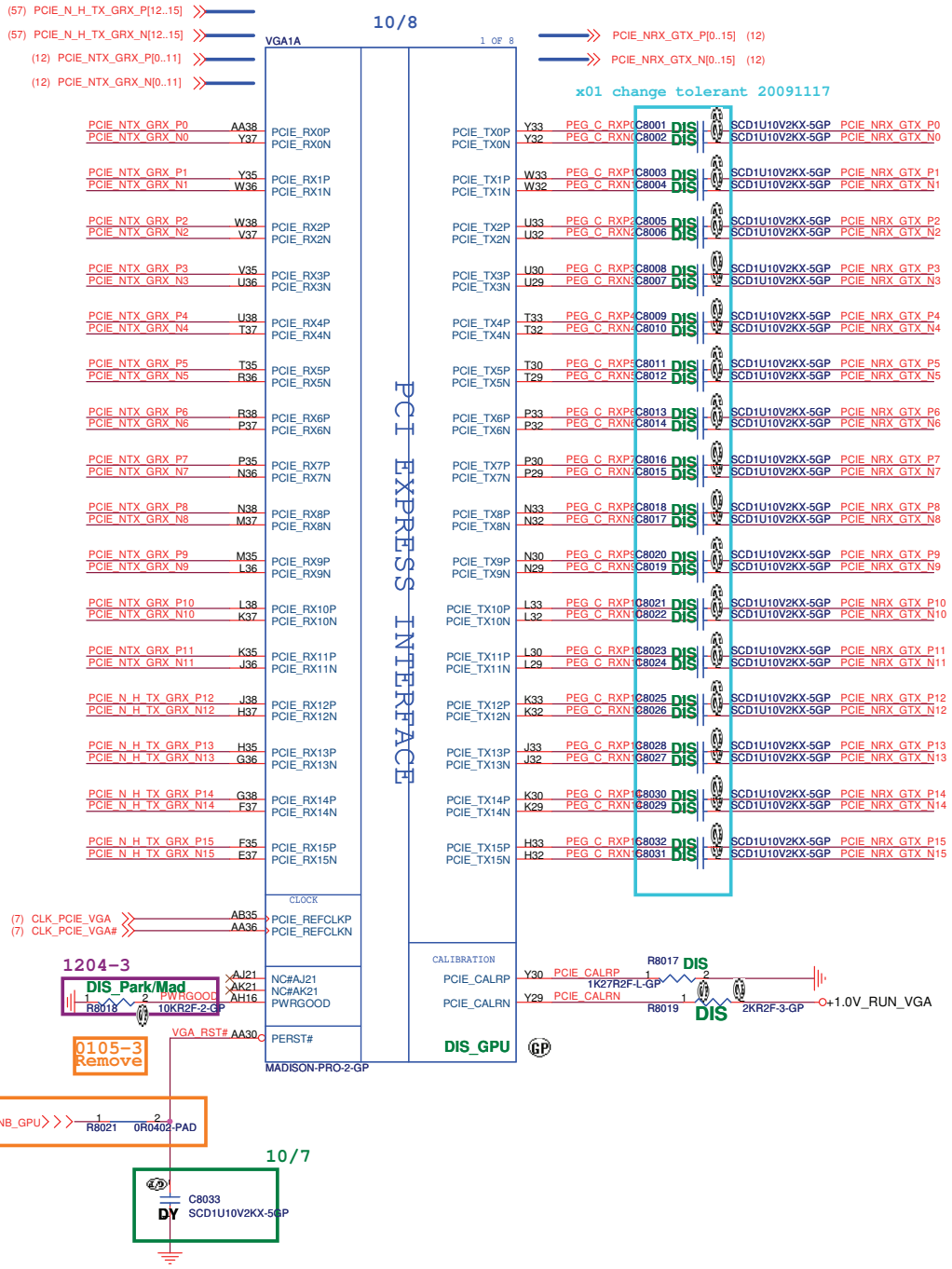
Title: UNUSED PARTS/EMI Capacitors
Size: A3 | Document Number: Berry | Rev: A00
Date: Thursday, March 04, 2010 | Sheet 79 of 95



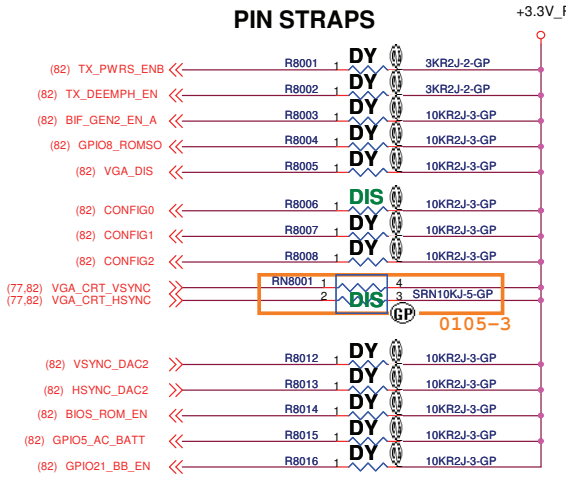
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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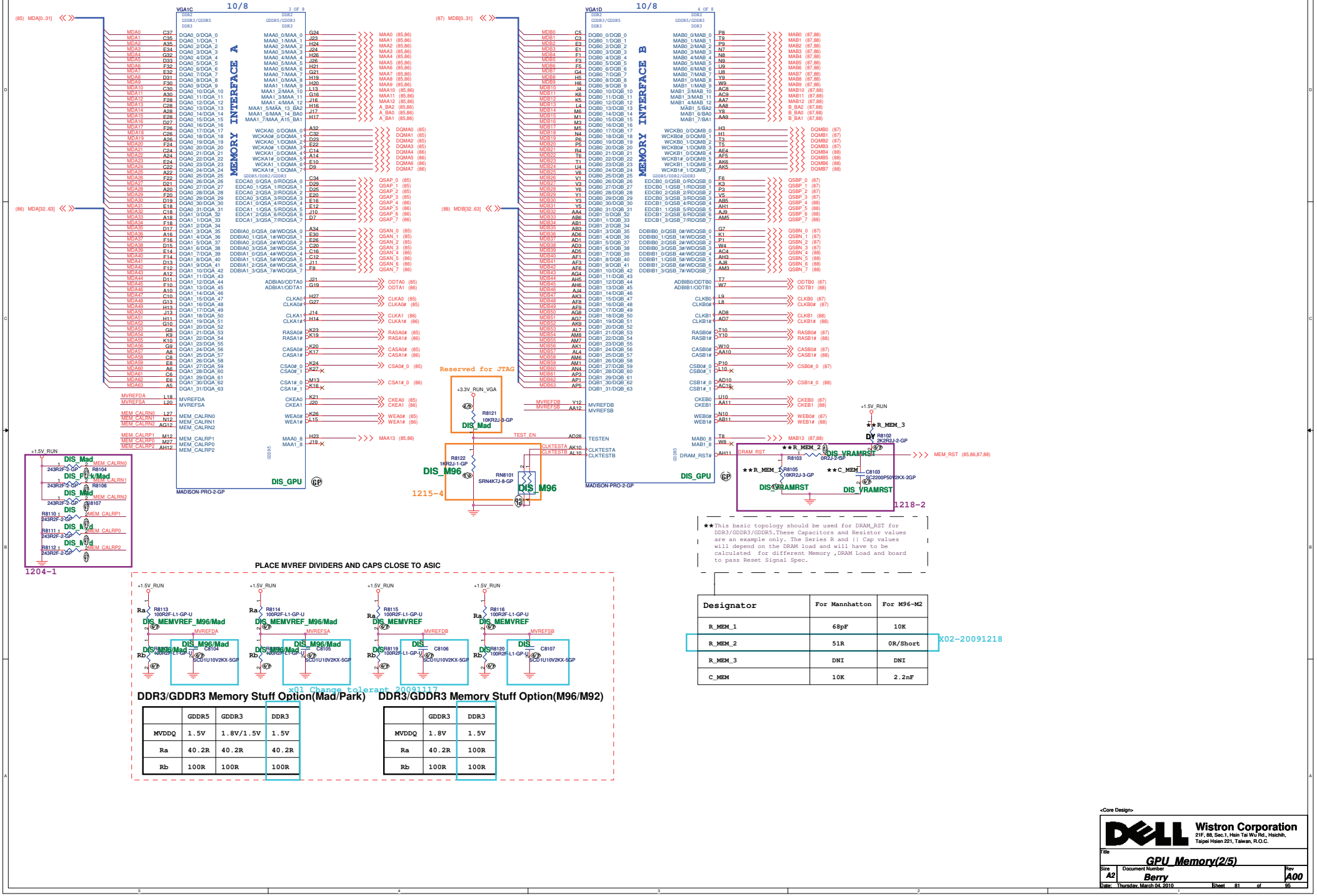
Title: GPU_PCIE/STRAPPING(1/5)

Size: A3 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 80 of 95



**This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For Mannhatton	For M96-M2
R_MEM_1	68pF	10K
R_MEM_2	51R	0R/Short
R_MEM_3	DNI	DNI
C_MEM	10K	2.2nF

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	100R
Rb	100R	100R

<Core Design>

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Title: GPU_Memory(2/5)

Size: A2 | Document Number: Berry | Rev: A00

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MEMORY ID Table

DVPDATA[0:3]	Description
1000	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz)
0000	DDR3 Samsung-K4W1G1646E-HC12 (800MHz)

DVPDATA[0:3] Default:Pull down

Madison Only JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode
TESTEN	"1"(PU)	"1"(PU)
JTAG_TRST#	"0"(PD)	"1"(PU)
JTAG_TCK	CLK	"1"(PU)
JTAG_TMS	"1"(PU)	"1"(PU)

LVDS Interface

DDC channel for LDVS

DDC channel for CRT

DDC channel for HDMI

DDC1/DDC2/DDC6 have 5V-tolerant

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

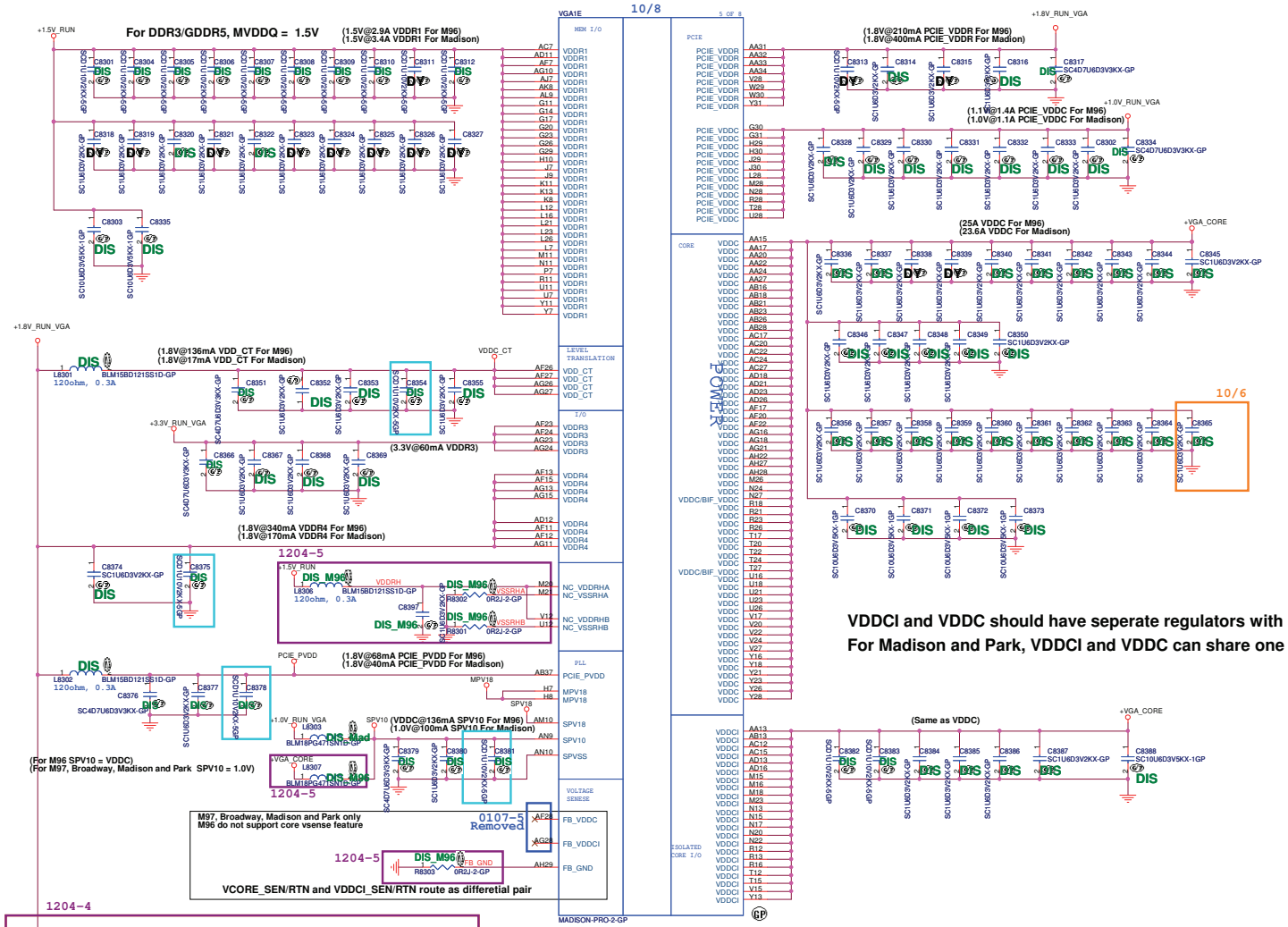
<Core Design>

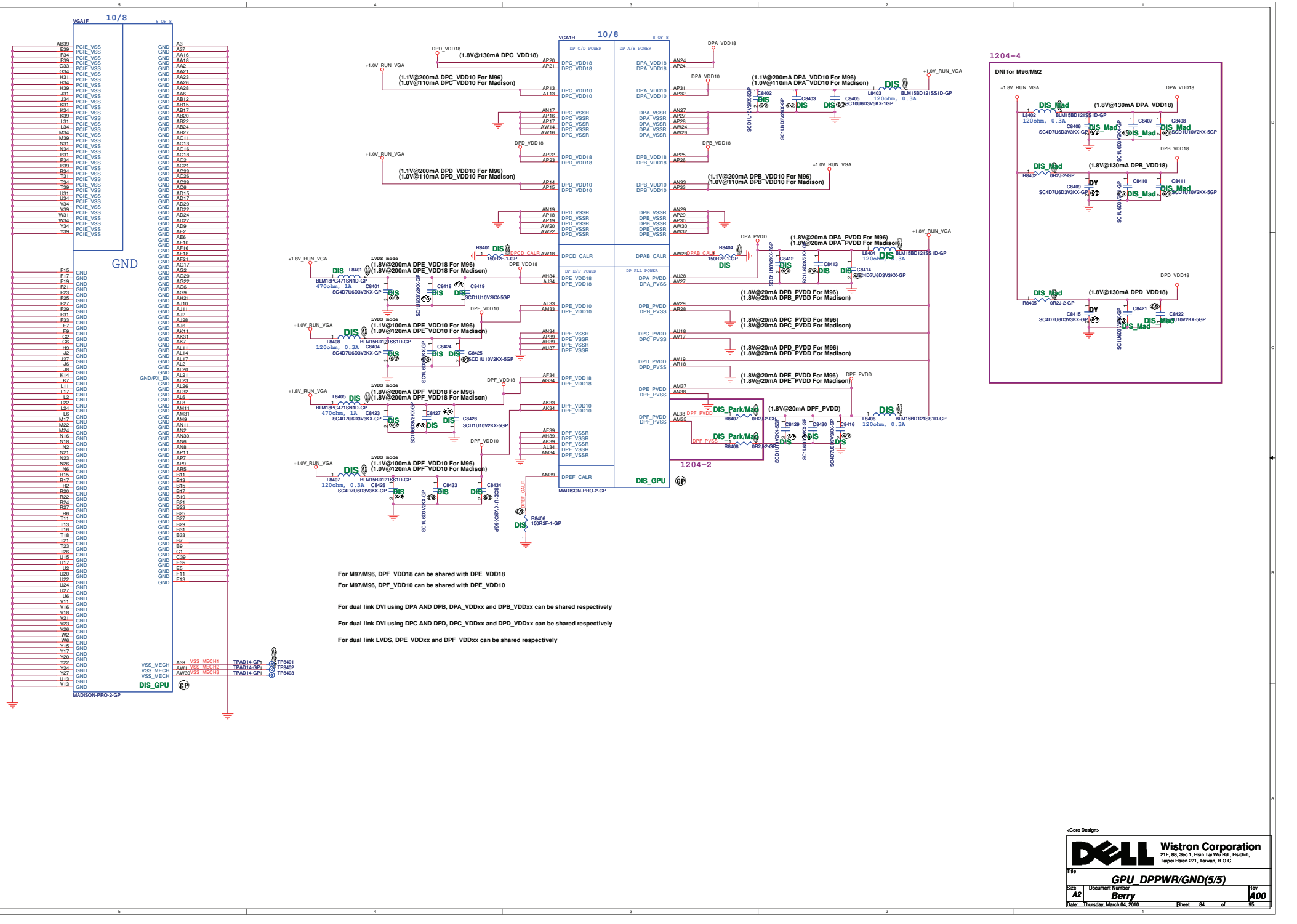
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 82 of 95


For DDR3/GDDR5, MVDDQ = 1.5V
(1.5V@2.9A VDDR1 For M96)
(1.5V@3.4A VDDR1 For Madison)
(1.8V@210mA PCIE_VDDR For M96)
(1.8V@400mA PCIE_VDDR For Madion)
(1.1V@1.4A PCIE_VDDC For M96)
(1.0V@1.1A PCIE_VDDC For Madison)
(25A VDDC For M96)
(23.6A VDDC For Madison)
(1.8V@136mA VDD_CT For M96)
(1.8V@17mA VDD_CT For Madison)
(3.3V@60mA VDDR3)
(1.8V@340mA VDDR4 For M96)
(1.8V@170mA VDDR4 For Madison)
(1.8V@68mA PCIE_PVDD For M96)
(1.8V@40mA PCIE_PVDD For Madison)
(VDDC@136mA SPV10 For M96)
(1.0V@100mA SPV10 For Madison)
(For M96 SPV10 = VDDC)
(For M97, Broadway, Madison and Park SPV10 = 1.0V)
(Same as VDDC)
M97, Broadway, Madison and Park only
M96 do not support core vsense feature
0107-5
Removed
VCORE_SEN/RTN and VDDCI_SEN/RTN route as differetial pair
(1.8V@50mA SPV18)
(1.8V@150mA MPV18)
VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator
NOTE1:
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134
NOTE2:
FB_VDDC, FB_VDDCI and FB_GND are not support on M96
NOTE3:
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.
NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GPU_POWER(4/5)
Berry
A00
Thursday, March 04, 2010
83
95



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
A2	Berry	A00

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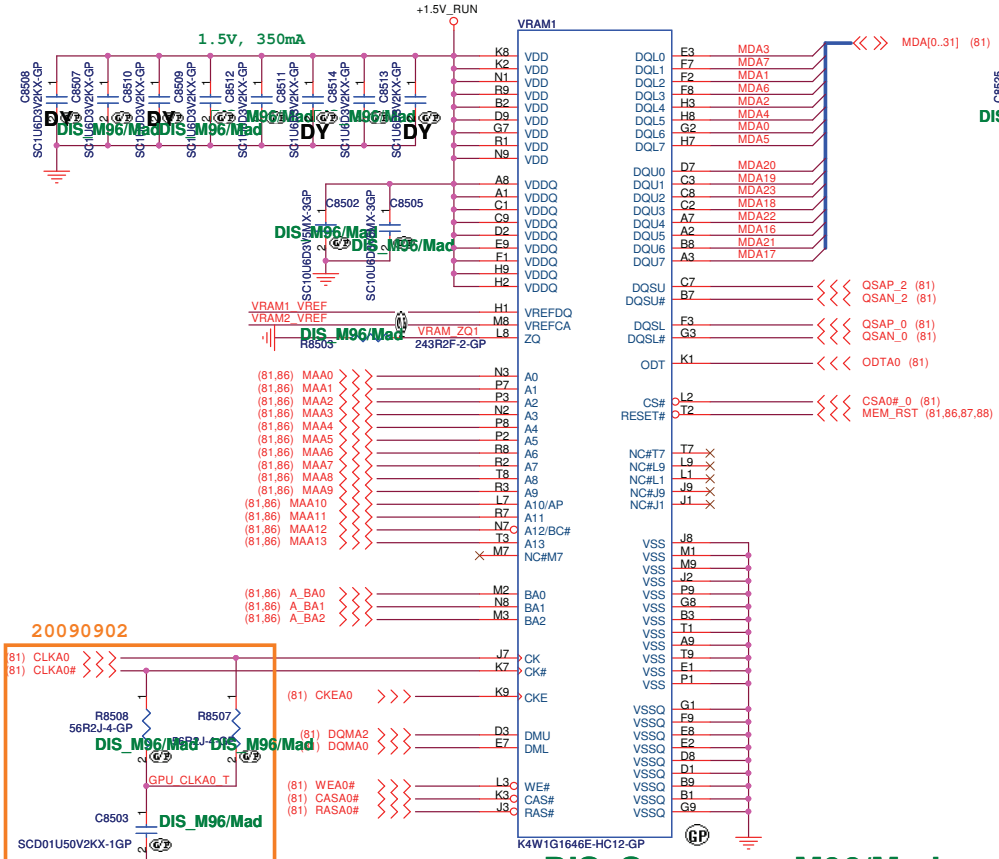
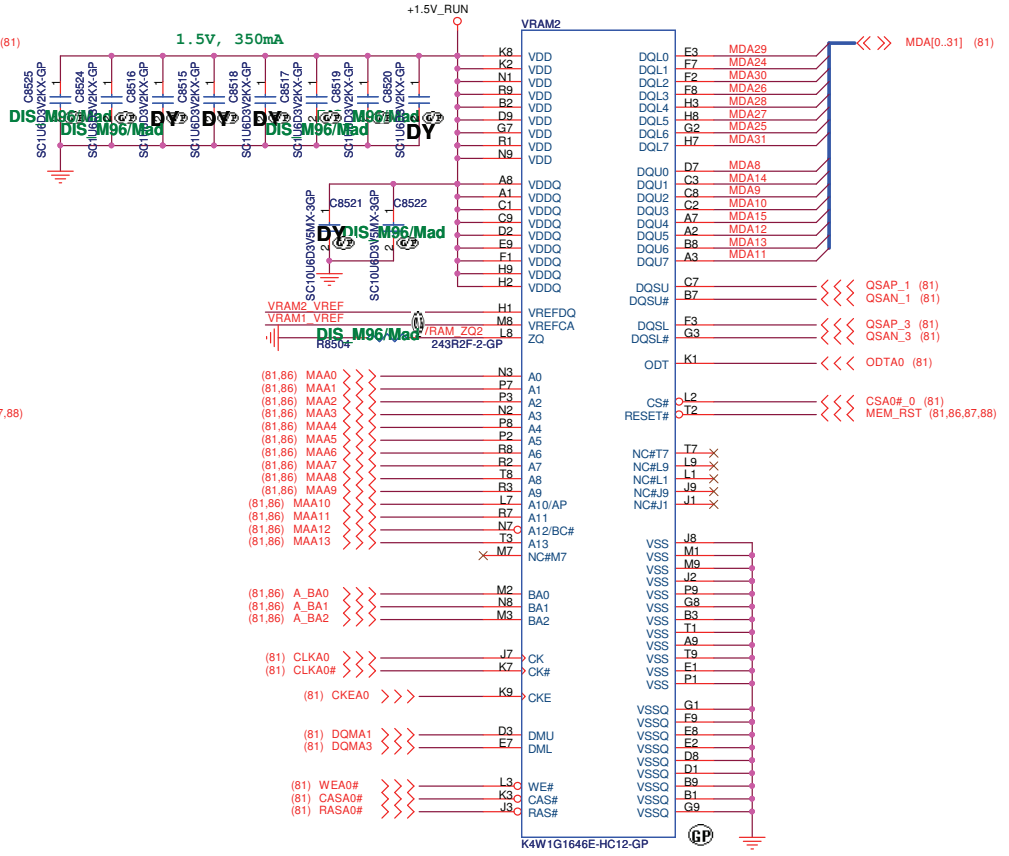
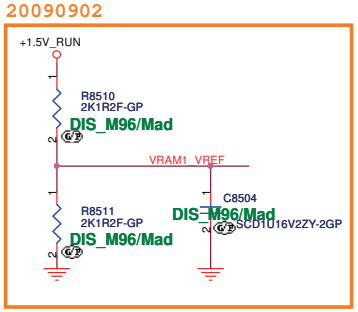


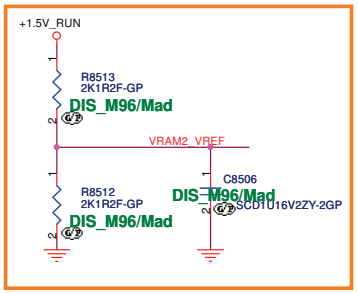


20090902

20090902



20090902



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Title: GPU-VRAM1,2 (1/4)

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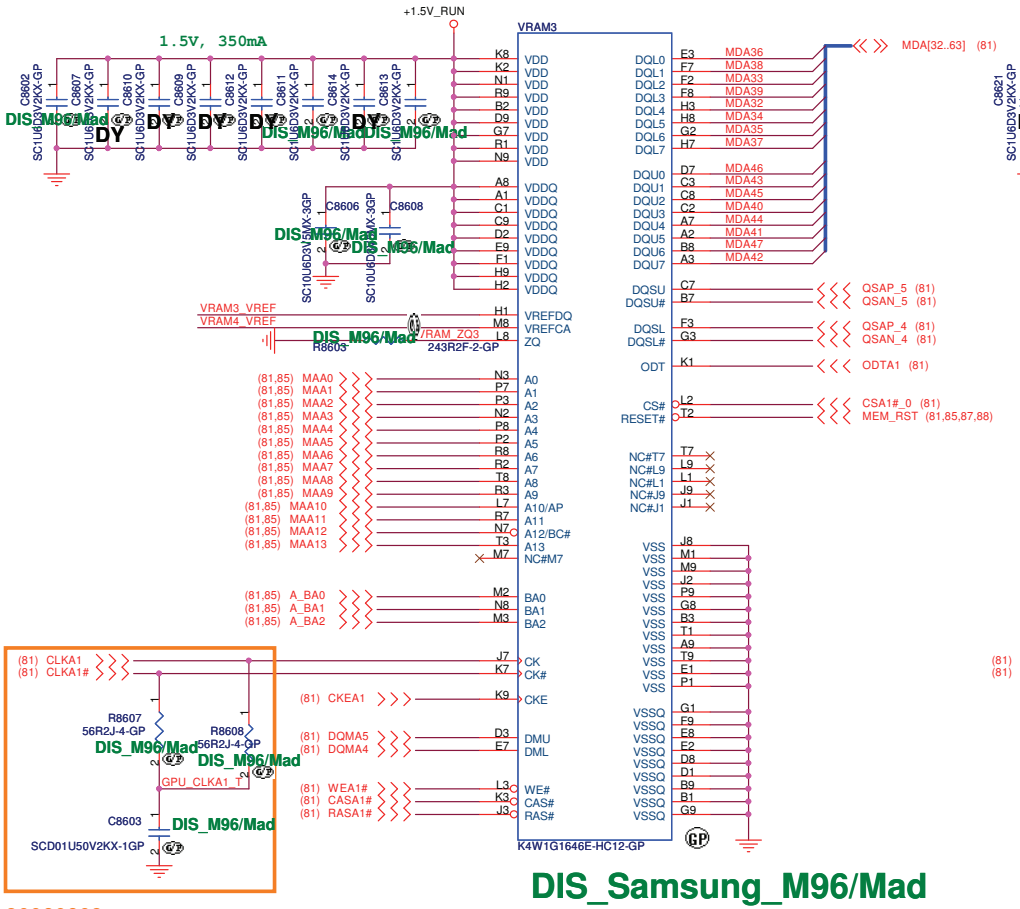

DIS_Samsung_M96/Mad

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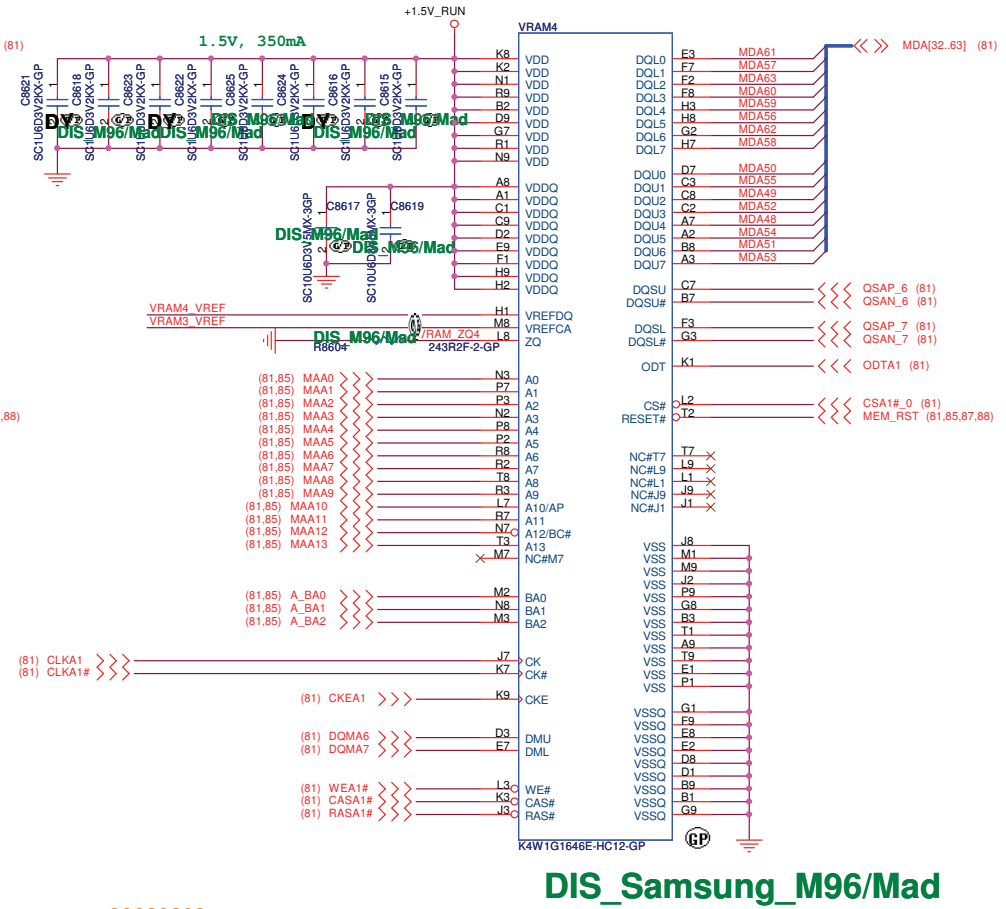

DIS_Samsung_M96/Mad

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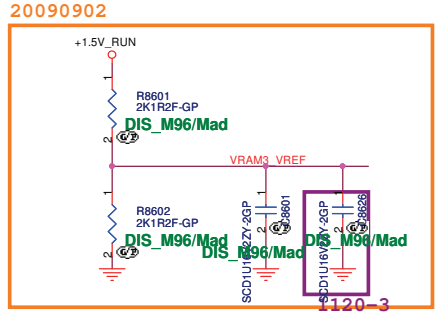

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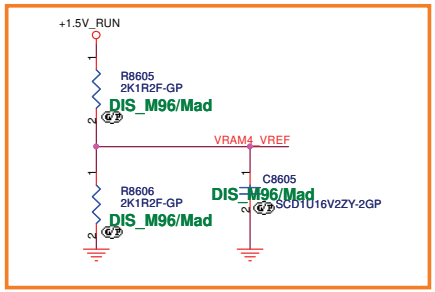

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Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
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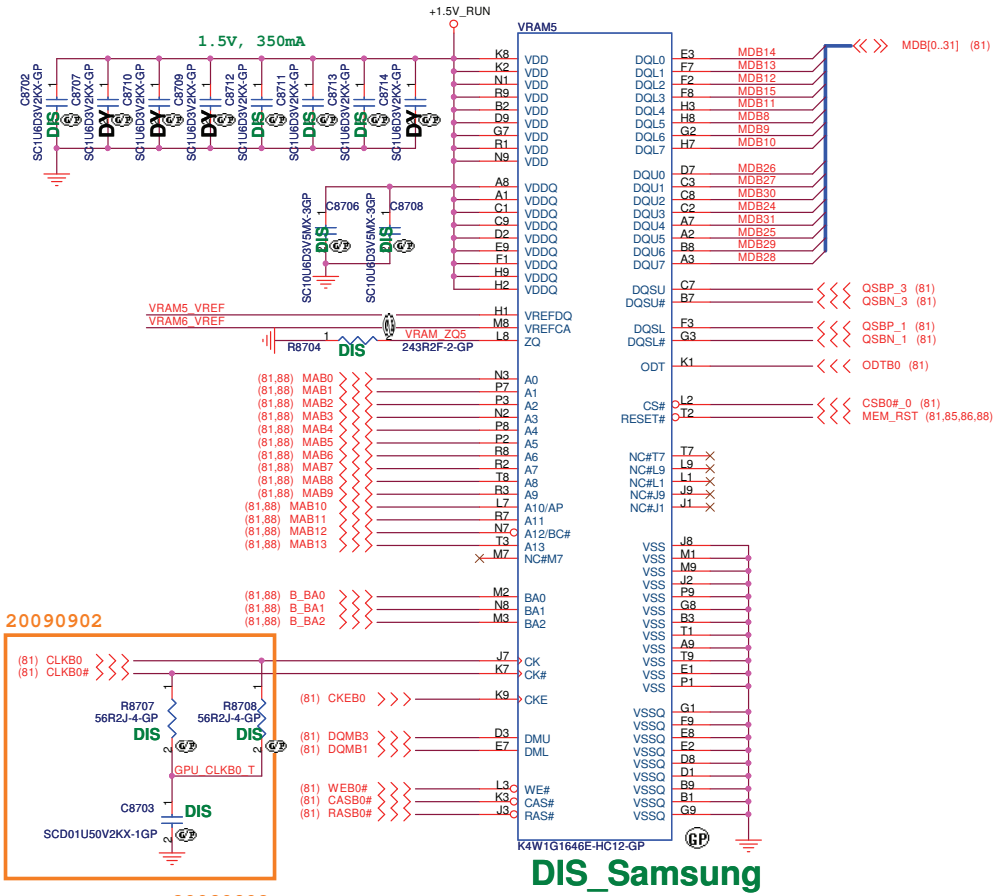

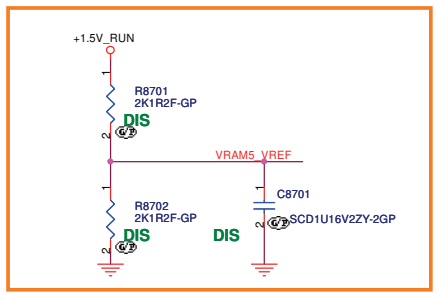

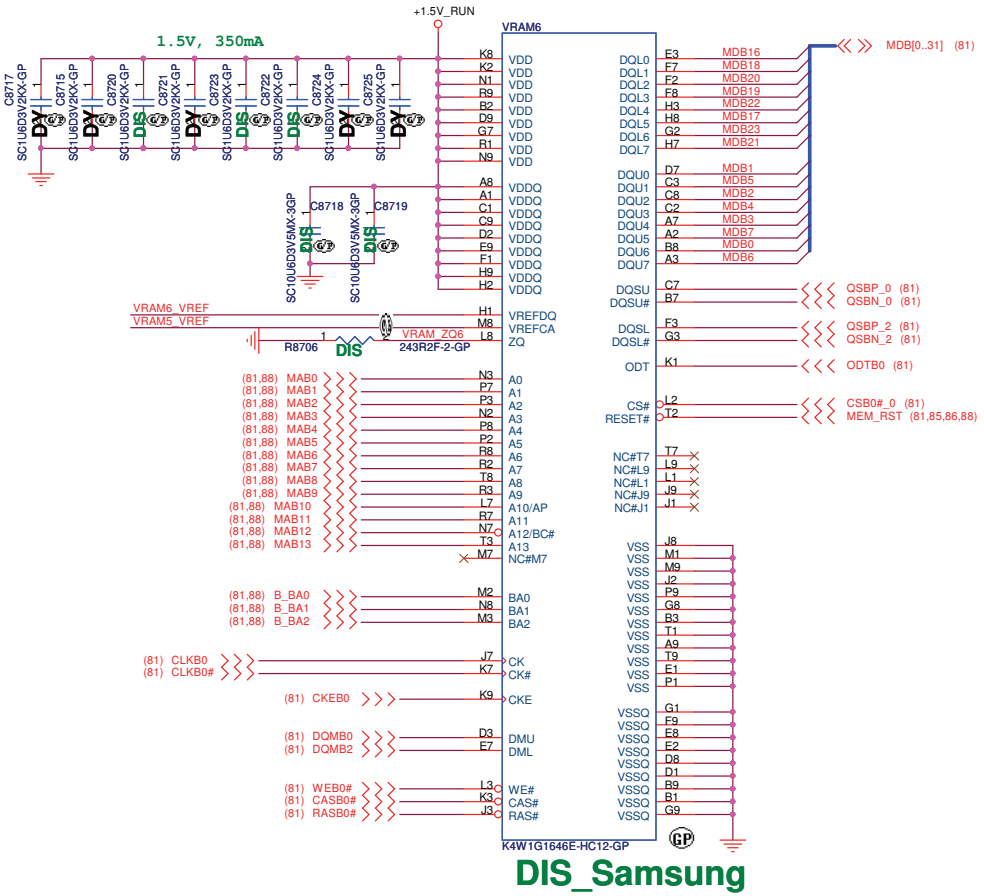

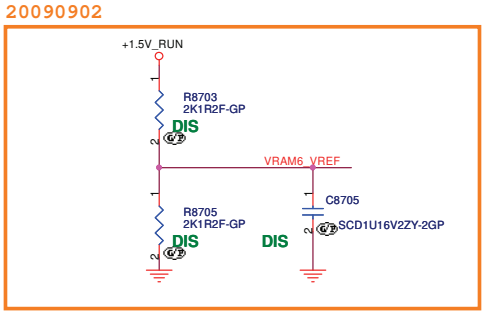

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Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
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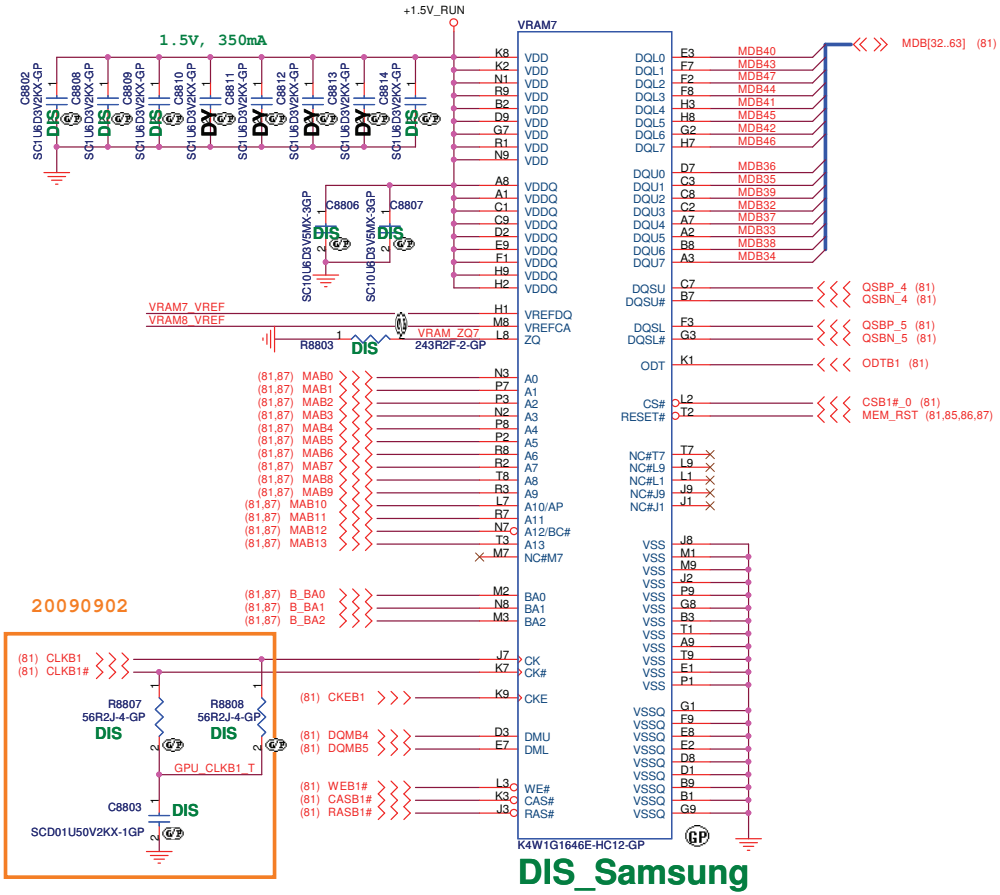

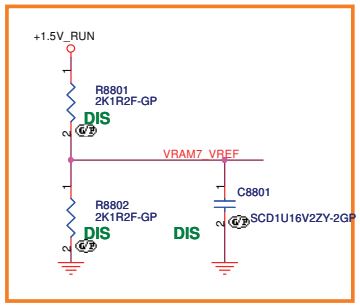

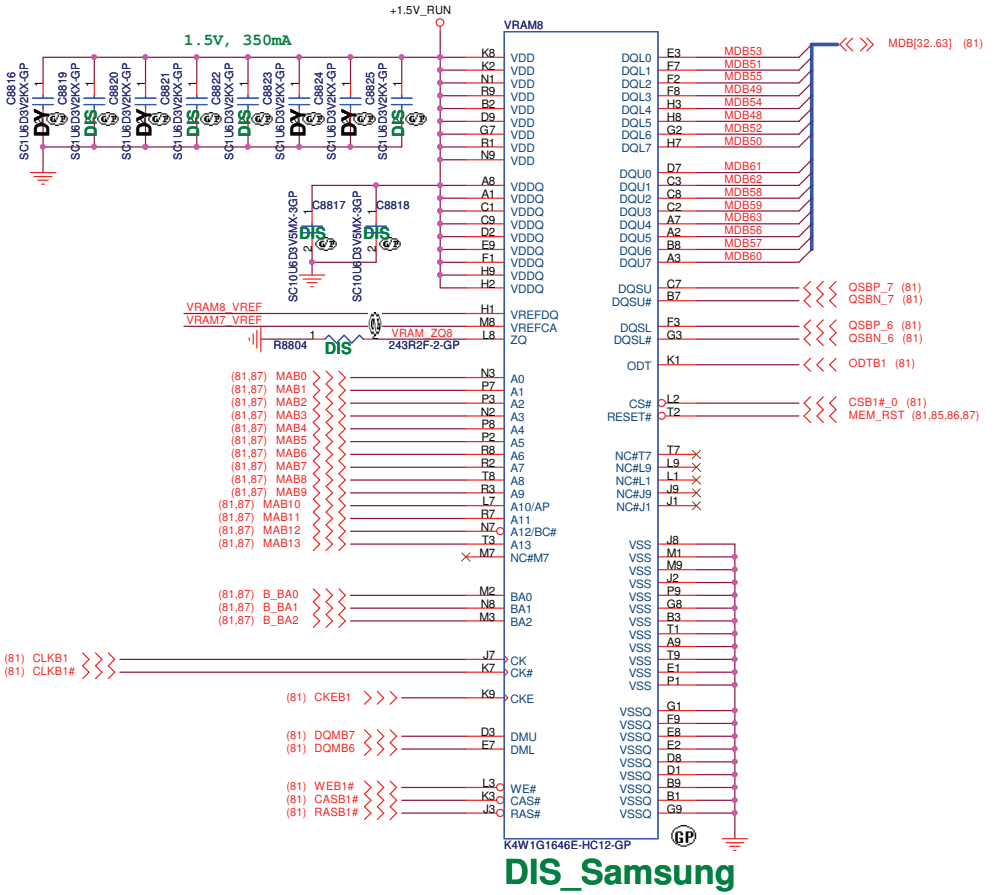

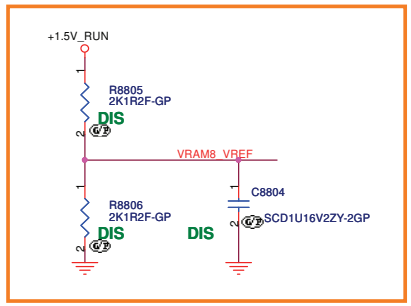

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Title: GPU-VRAM7,8 (4/4)
Size: A3
Document Number: Berry
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Date: Thursday, March 04, 2010
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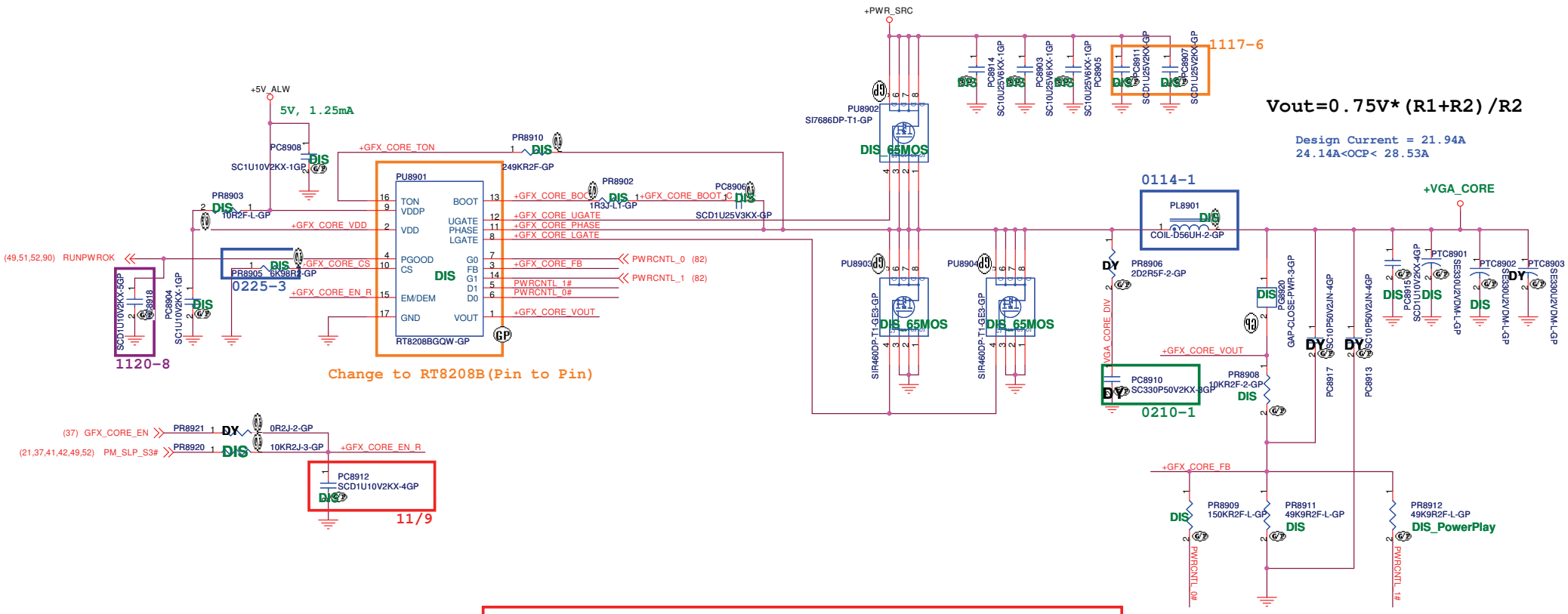
SSID = Video.PWR.Regulator

RT8208AGQW for +VCC_GFX_CORE



M96 Power Table

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.1V

PR8912=49.9KR
64.49925.6DL

Park Power Table

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.12V

PR8912=49.9KR
64.44225.6DL

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

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Title: RT8208B_+VCC_GFXCORE
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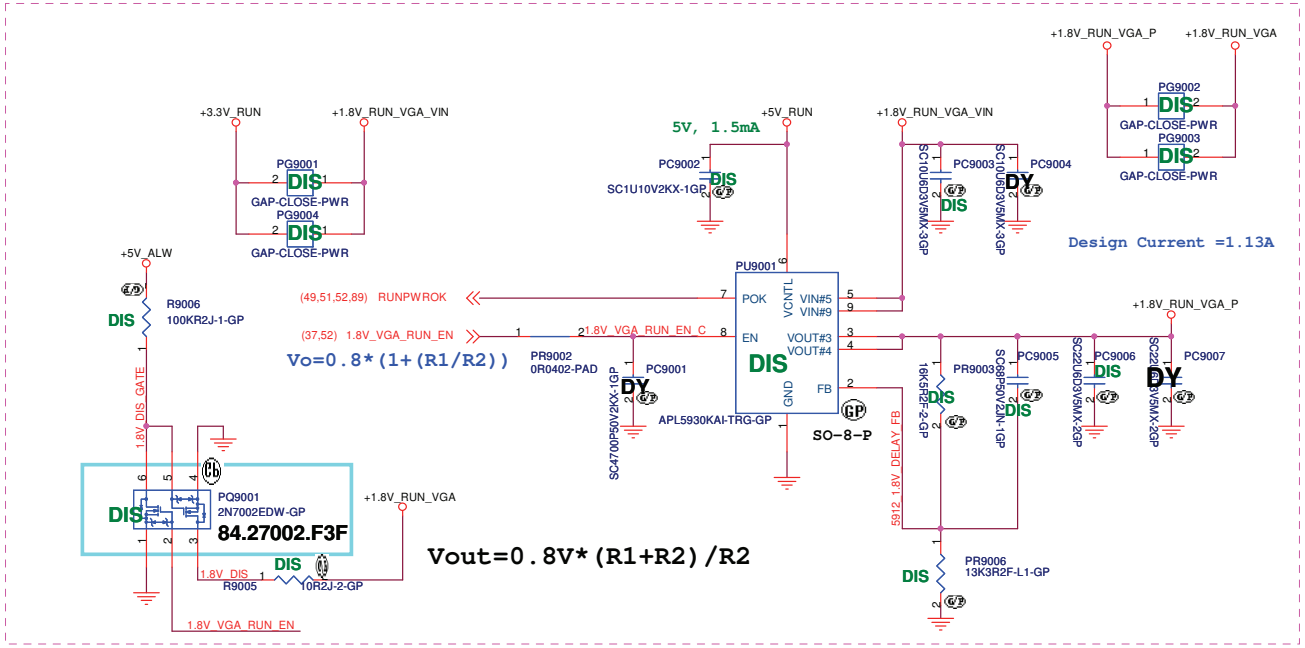
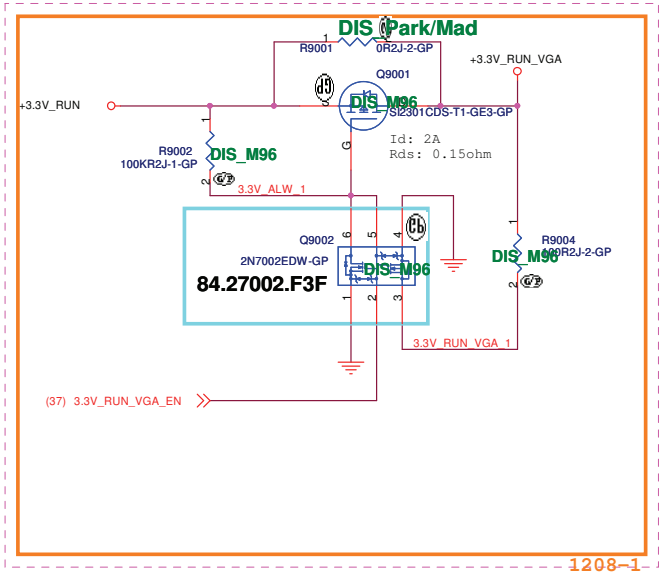
APL5930 for +1.8V_RUN_VGA

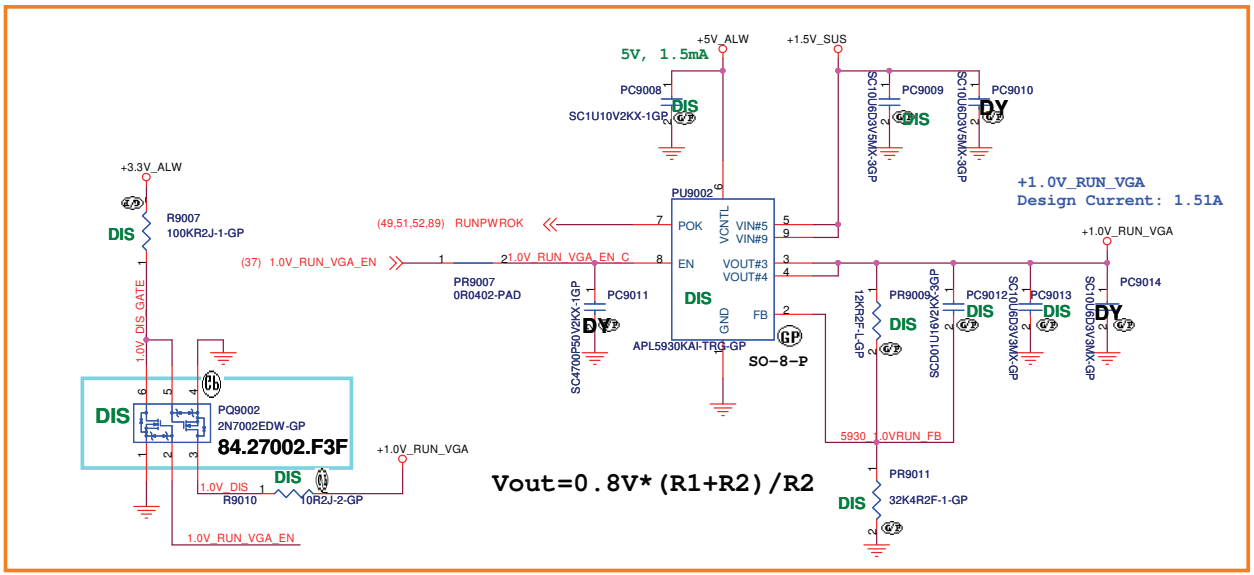


+3.3V_RUN_VGA



APL5930KAI for +1.0V_RUN_VGA

Will be Change to +1.0V_RUN_VGA



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Title: DISCRETE VGA POWER

Size	Document Number	Rev
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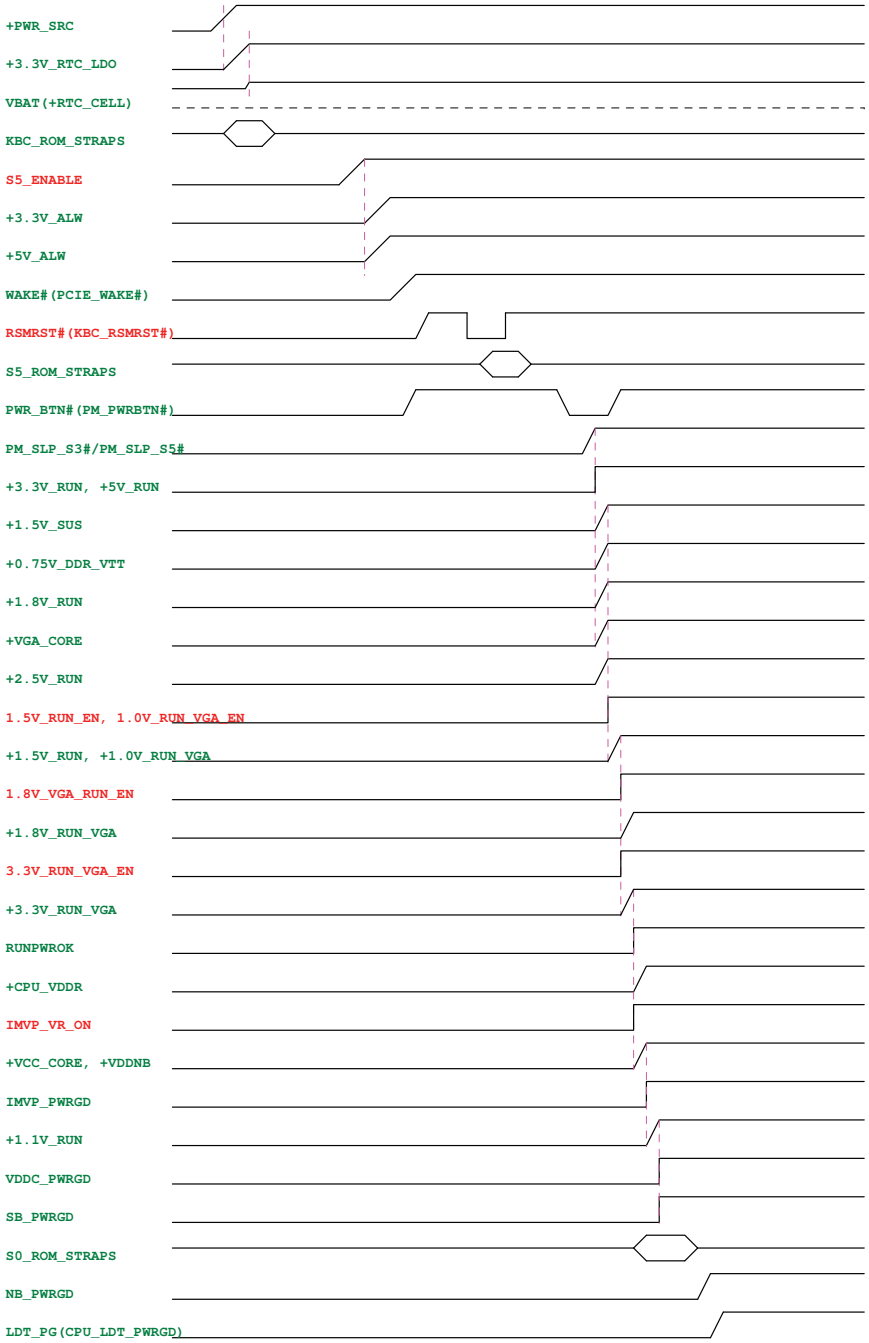
POWER SEQUENCE



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Title: POWER SEQUENCE

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

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Change notes - Page 1

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X01	11/6	1	10	Add C1002 10uF, C1007, EC1001 0.1uF, C1008 10pF.	Insure signal quality.	EE
		2	13	Change R1314 to 4.7K.	Meet CRB.	EE
		3	51	Swap PU5101 pin3, pin4.	Correct input voltage level.	EE
		4	82	Add R8210 0R.	Reserve GPU clock input source.	EE
	11/9	1	30	Change C3014 to 2.2uF.	Reduce package size.	EE
		2	69	Change C6903 to 0.1uF.	Reduce package size.	EE
		3	49	Add PR4916 100KR.	To prevent leakage in S3 status.	EE
	11/10	1	18,19	Change DIMM socket Part Number.	Request by ME.	ME
		2	37	Add R3754 100KR.	To detect leakage current.	EE
	11/11	1	10	Modify R1028 pull-up to +1.5V_RUN.	Solve leakage in S3 status.	EE
	11/12	1	20	Change C2011 to 18pF, C2012 to 15pF.	Set accurate clock frequency.	EE
		2	37	Add C3717 10pF.	Stable singal level.	EE
		3	57	Delete RN5711, RN5705.	Redundant parts.	EE
		4	13	Delete R1331, R1332, R1308.	Redundant parts.	EE
		5	77	Add Pi-filter.	Cure EMI.	EMC
	11/13	1	20	Change X2001 P/N.	Request by Sourcer.	Sourcer
		2	7	Change R713 to 47R.	Fine tune damping.	EE
		3	82	Add R8211 80.6R, R8220 150R.	Set a voltage divider to 1.8V level swing.	EE
		4	21	Add R2133 1KR.	For UMA VRAM vendor selection.	EE
	11/16	1	22	Delete RN2203 pin 4, pin 5 connection.	Solve S5 leakage.	EE
		2	51	Change PR5105 pull-up to +3.3V_RUN.	Prevent leakage.	EE
		3	21	Add C2103, C2104 0.1uF.	For signal stability.	EE
		4	37	Add C3718 0.1uF.	For signal stability.	EE
		5	41	Add C4101, C4102 0.1uF.	For signal stability.	EE
		6	49	Add PC4923 0.1uF.	For signal stability.	EE
		7	66	Add C6601, C6602 0.1uF.	For signal stability.	EE
		8	77	Add RN7713 150R.	Move impedance matching resistor from CRT/B to M/B.	EMC
		9	78	Change CARDBD1 pin 2 link to PLTRST#_LAN_WAN.	Change card reader chip to RTS5159 to solve EMI.	EMC
	11/17	1	30	Add R3014, R3017, R3020 0R to link AGND and GND.	Issue for pop noise when system boot.	EE
		2	42,48,50	Merge 1.1V power solution on main board.	Save components.	EE, Power
		3	77	Modify CRTBD1 pin define.	Relief EMI.	EMC
		4	79	Add some decoupled capacitors.	Request by EMC.	EMC
		5	37	Change R3737 to 33R, stuff C3715 10pF.	Request by EMC.	EMC
		6	62,89	Sutff EC6203 22pF, PC8911, PC8907 0.1uF.	Request by EMC.	EMC
		7	45,46,47	Stuff EC4502 0.1uF, PC4605, PC4609, PC4738 0.1uF.	Request by EMC.	EMC

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Title: Change notes

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Change notes - Page 2

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X01	11/17	8	9	Delete R904.	Remove redundant layout trace.	EE
	11/18	1	81	Swap R8105, C8103 location.	Meet CRB.	EE
		2	79	Add some decoupled capacitor.	By RF team request.	RF
		3	49	Change PR4903 to 620KR.	Change to common part.	Power
	11/19	1	All	Synchronize with DJ schematic.	Schematic standardlize.	EE
		2	48	Change P/N for PU4802, PU4803, PU4804, PU4805.	Rquest by Power team	Power
		3	All	Review all capacitors tolerance.	Total review for deratig.	EE
		4	21	Add RN2105 0R.	Reserve to fine tune signal quality.	EE
		5	21	Change RN2101 to 4.7KR.	Fine tuned value for signal.	EA
		6	37	Add RN3705, R3755 0R.	To isolate layout trace to DB1 connector.	EA
		7	49	Change PC4908 to 2.2uF.	Changed by EA report.	EA
	11/20	1	54	Modify R5408 connection.	To synchronize with DJ.	EE
		2	57	Add D7701.	To prevent leakage from RGB monitor.	EE
		3	86	Add C8626 0.1uF.	By EA report.	EA
		4	37	Add R3756 10KR, C3720 0.1uF.	Synchronize with DJ.	EE
		5	37	Delete RN3705, R3755.	For more layout space.	EE
		6	13	Delete TP1303, TP1304.	For more layout space.	EE
		7	49	Delete PR4905.	For more layout space.	EE
		8	89	Add PC8918 0.1uF.	Stable signal quality.	EE
	11/24	1	46,49	Change PU4601, PU4901 Power components.	Request by Power team.	Power
	11/25	1	46,47,49,89	Change power components.	Request by Power team.	Power
	11/29	1	10	Change C1008 to 10pF.	Fine tuned signal slew rate to meet specification.	EE
		2	30	Change R3007 to 2.2KR.	By FAE suggestion.	EE
X02	12/04	1	81	Set BOM mark R8104, R8106, R8107, R8110, R8111, R8112.	Implement co-layout Madison and M96.	EE
		2	82,84	Add R8407, R8408 0R.	Implement co-layout Madison and M96.	EE
		3	80	Add R8016 10KR.	Implement co-layout Madison and M96.	EE
		4	83,84	Set BOM mark.	Implement co-layout Madison and M96.	EE
		5	83	Add L8306, L8307, C8397, R8301, R8302, R8303.	Implement co-layout Madison and M96.	EE
	12/05	1	37	Change R3756, C3720 connection.	Correct soft-start for EC power.	EE
	12/08	1	90	Set BOM mark.	Implement co-layout Madison and M96.	EE
	12/15	1	15	Delete RN1501, Add G1501~G1504.	Synchronize with DJ and supply sufficient power rail.	EE
		2	62	Add R6207 100KR.	Insure SPI Write-Protect pin signal level.	EE
		3	66	Change C6602 net name.	Correct signal name.	EE
		4	81	Add R8122 1KR, RN8101 4.7KR.	Meet M96 schematic check list.	EE
		5	82	Swap CLK_VGA_27M_NSS and CLK_VGA_27M_SS connection.	Solve external RGB display tremble issue.	EE

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Title: Change notes

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VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X02	12/16	1	66	Change R6605 to 0R.	Assure power button level set to low.	EE
		2	37,76	Add net "8103_GPO".	Implement LAN DSM hardware function.	EE
	12/17	1	37	Add U3703.	To solve SPI WP signal malfunction on EC.	EE
	12/18	1	82	Add R8222 1MR.	Assure crystal resonant clock stable.	EE
		2	81	Set VRAM reset circuit.	Follow M96 reset circuit and reseve BOM option.	EE
	12/25	1	18	Change TC1801 to 330uF, 2V tolerance.	Implement common part for 1.5V power rail.	EE
		2	46	Change PR4603 to 127KR.	Set 5V current limitation.	Power
		3	46	Empty PR4618 and stuff PR4619.	Set Ultra-sonic mode to keep +15V_ALW voltage level.	Power
		4	10	Set RN1006 PU to +1.5V_SUS.	Follow AMD check list and cure +1.5V_RUN leakage.	EE
		5	62	Change R6206 to 1KR.	According to Safety request, verified OK.	Safety
		6	51	Change PR5102 1KR, PR5106 8.2KR, PR5107 5.62KR.	Set VDDR low voltage level to 0.9V.	EE
	12/29	1	10,37	Add Q1005, R1039, R1040.	Request by AMD to set CPU into HTC mode in DOS.	EE
		2	47	Change PR4720 93.1KR, PR4721 24KR.	Set power OCP value.	Power
	12/31	1	ALL	Change some resistors as short-pad or resistor array.	Save component counts.	EE
		2	ALL	Change some capacitors with smaller value or empty.	Save component counts.	EE
	01/04	1	15	Change R1507,R1508,R1509,R1510,R1511 to bead.	Filter power noise.	EMC
	01/05	1	7	Combine R707,R721 as RN711.	For more layout space.	EE
		2	81	Delete TP8101,TP8102.	Remove useless test point for more layout space.	EE
		3	7,80	Delete R716,R8020, combine R8009,R8010 as RN8001.	Redundant part.	EE
		4	37,39,41	R3747,R4104 short pad, delete R3722,R3904.	Redundant part.	EE
		5	46	Change PR4620 as short pad.	Redundant part.	EE
		6	51	Change PQ5101 with ESD protector.	Change to common part.	Power
		7	54	Empty R5405 and Stuff R5408.	Avoid LCD white panel.	EE
		8	62	Change R6205 to 0R.	Already have one 1KR ahead.	EE
	01/06	1	50	Add PR5004 10KR and empty PR5002.	Avoid +1.1V_ALW leakage in South Bridge.	EE
		2	13	Change R1342 to size 0603.	Synchronous schematic w/DJ.	EE
		3	79	Add R7921 and R7922.	Reserved RF team solution.	RF
	01/07	1	7	Add RN712,C722,C723	Reserve for SMBus signal quality tuning.	EE
		2	60	Change EC6007,EC6008 to 0.01uF.	According FAE Request.	IDT FAE
		3	39	Add Q3904.	According thermal team request.	Thermal
		4	21,18	Change location RN2105 to RN1801, add C1823,C1824.	For SMBus signal quality fine tune.	EE
		5	39,82,83	Remove C3912,TP8301,TP8302,TP8213.	Remove dummy part for more layout space.	EE
		6	76	Reserve C7601, C7602.	Fine tune USB signal quality.	EE
	01/08	1	79	Reserve EC7925,EC7926,EC7927.	Reserve by EMC team.	EMC
		2	77	Change RN7711 to 0R, L7701,L7702,L7703 to bead 22R.	According EMC measurement result.	EMC

0108

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Title: Change notes

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Change notes – Page 4

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X02	01/08	3	18,19	Add C1825,C1922.	Reduce V_REF ripple by EA team result.	EE
		4	37	Reserve C3721,C3722.	Prevent signal cross talk.	EE
		5	ALL	Change capacitors value and add C3723.	Ensure signal quality.	EE
	01/11	1	68	Change KB1 P/N.	According ME request.	ME
		2	66	Change R6601,R6602,R6604,R6606 to 1KR, R6603 to 470R.	Decrease LED brightness.	EE
	01/12	1	37	Add C3724, R3757.	To set accurate current detection in EC.	EE
		2	10	Add R1041 0R.	Add 0R for level shift off.	EE
	01/13	1	21,37	Add C3725, C2105.	Reserve for singal quality.	EE
	01/14	1	Power	Modify power team componets.	Request by Power Team.	Power
		2	7	Change RN712 to 22R.	Fine tuned damping resistor value.	EE
A00	02/08	1	66	Reserve R6609, R6610 1KR.	Add for future LED brightness balance.	EE
		2	68	Add keyboard back light circuit, remove R5403.	Add for keyboard with back light module.	EE
		3	69	Change HALLSW1 footprint for co-layout.	Change for co-layout different kind of HALLSW1.	EE
		4	77	Add AFTP7701, AFTP7702, AFTP7703.	Add AFTP test point for factory test.	EE
	02/10	1	Power	Update Obsolete parts.	Update obsolete parts due to policy.	Power
		2	79	Change HBT1 part number.	Change HBT1 part number to match ME EMN file.	ME
		3	47	Add PTC4710.	Add to solve board accoustic issue.	EE
	02/22	1	54	Remove co-layout pad.	As factory requst.	EE
		2	42	Add C4217, C4401, C4402.	Ensure signal quality.	EE
		3	48	Delete Power Gap.	Request by Power Team.	Power
	02/23	1	ALL	Change to short pad.	Change most of 0-ohm resistors to short pad.	EE
	02/24	1	7,68,79	Reserve C724, C725, C6806, C6807, EC7928-EC7932.	As EMC team request.	EMC
	02/25	1	13	Add TP1309.	As factory requset to add.	Factory
		2	7,68	Rename EMC capacitor to EC704,EC705,EC6801,EC6802.	Meet schematic standardization.	EE
		3	49,89	Change PR4913 to 3.9R, PR8905 to 6.98KR.	PR4913 for snubber, PR8905 for OCP.	Power
		4	21	Change R2133 to 0R.	Set GPIO input level from 0.5V to 0V.	EE
		5	79	Remove EC7928.	Layout space limitation.	EE
	02/26	1	39,42	Empty R3906 and Change R4202 from 0R to 1KR.	It is for solving T8 shutdown issue.	EE
	03/03	1	60	Change SPK1 part number.	Request by ME.	ME
	03/05	1	20,24,37	Empty R2029,R2404,R3751.	Saving unused components.	EE
	03/08	1	48	Stuff PU4803 and empty PU4804.	Place the H/S and L/S MOS at the same surface.	Power

0308-1

<Core Design>

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