VIQY0

(Y410)

NM_A031 Rev1.0 Schematic

Intel Haswell Processor with DDRIII + Lynx point PCH
nVIDIA N14P GT + 2nd VGA N14P GT

2013-03-19 Rev1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title **Cover Page**

LCFC

Size Custom
Document Number *Y410 NM-A031*
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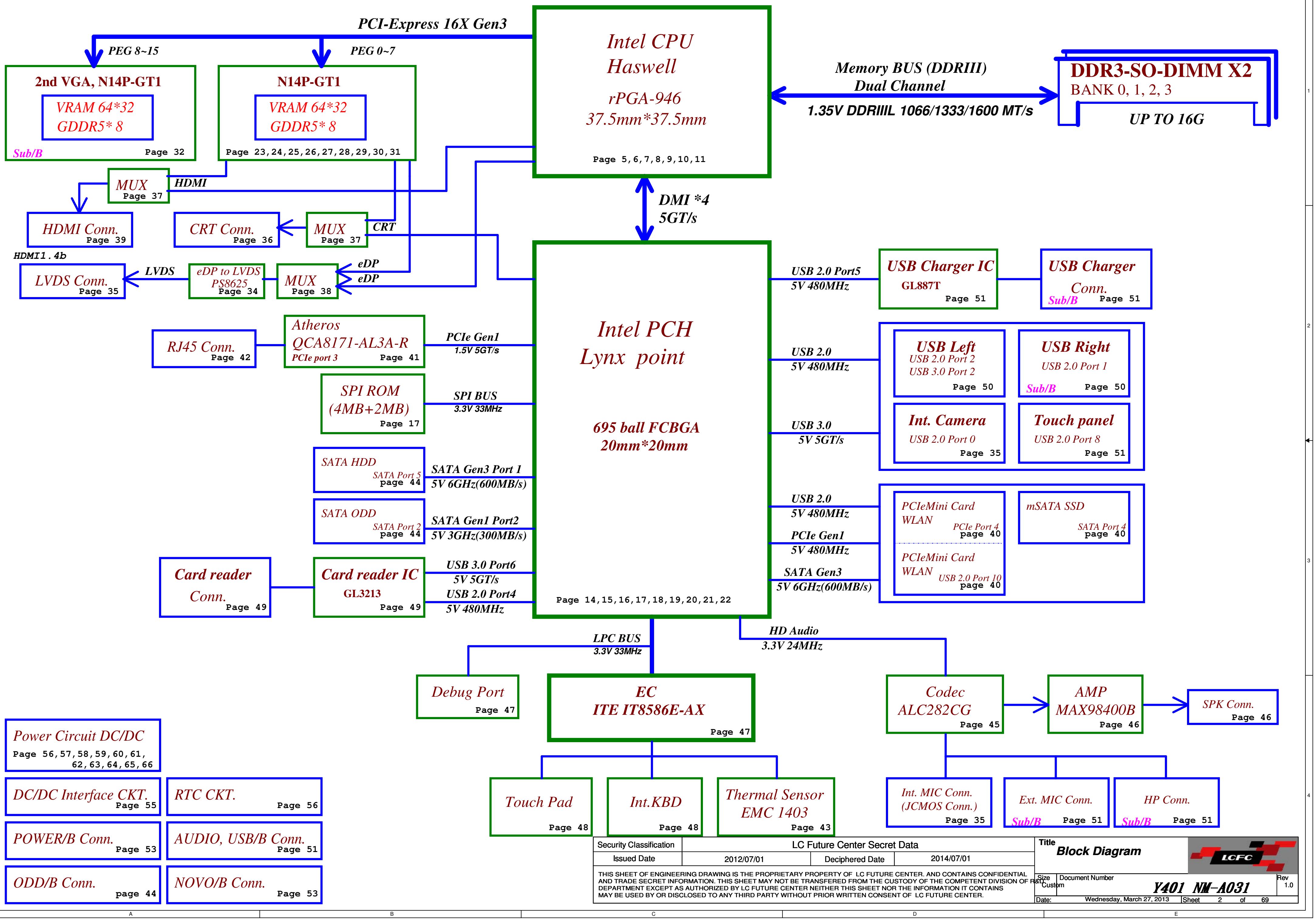

Security Classification	LC Future Center Secret Data			Title **Block Diagram**	LCFC
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
EHCI1	XHCI	0	Camera
		1	USB Port (Right Side)
	2	2	USB Port (Left Side)
		3	
	4	4	Card Reader
		5	USB Port (Right Side)
		6	
		7	
EHCI2		8	
		9	
		10	Mini Card(WLAN)
		11	
		12	
		13	

BOM Structure Table

BOM Structure	BTO Item
GT@	NV GT750M
GT1@	NV GT755M
CMOS@	CMOS Camera part
SURGE@	QCA8171 LAN surge part
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
@	Unpop
DS3@	Deep S3 support part
daul@	Support daul channel panel function
887T@	GENESYS 887T USB charger solution
887@	GENESYS 887 USB charger solution
TI@	TI USB charger solution
EDP@	Support EDP panel function
SLI@	For SLI function part
47W@	For 47W CPU part
37W@	For 37W CPU part

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
SMB_CLK_S3 SMB_DATA_S3	PCH +3VS	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIE PORT LIST

Port	Device
1	
2	
3	
4	LAN
5	WLAN
6	
7	
8	

Address

EC SM Bus1 address

Device	
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

ZZZ1

DAZ0SD00100

Security Classification	LC Future Center Secret Data		
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Title **Notes List**

LCFC

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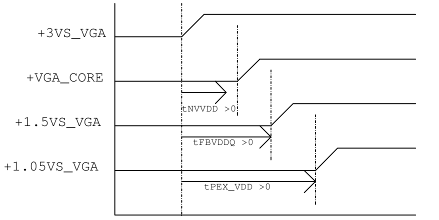
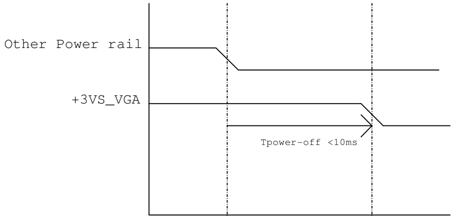
Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N14Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	IN	-	FB_CLAMP_MON
GPIO1	OUT	-	NA
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	NA
GPIO6	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO7	OUT	-	NA
GPIO8	OUT	-	OVERT#
GPIO9	OUT	-	VGA_ALERT#
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	NVVDD PWM_VID
GPIO12	IN	-	AC Power Detect Input (10K pull High)
GPIO13	OUT	-	DPRSLPVR_VGA
GPIO14	OUT	-	NA
GPIO15	IN	-	NA
GPIO16	OUT	-	NA
GPIO17	IN	-	VGA_EDP_HPD
GPIO18	IN	-	DGPU_HDMI_HPD
GPIO19	IN	-	NA



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N14P-GT (28nm)	0x0FCD

	setting	I2C Slave addrees ID
SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
	1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N14P-GT 28nm	PU 10K	PD 15K	PU 45K	PD 5K	PD 25K	PU 5K	PD 45K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU		N14P-GT	N14P-GT1	
FB Memory (GDDR5)		ROM_SI	ROM_SI	
Samsung 3000MHz	K4G20325FD-FC03			
	64Mx32		PD 30K	
Hynix 3000MHz	H5GQ2H24AFR-R0C			
	64Mx32		PD 25K	
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24AFR-T2C			
	64Mx32	PD 25K		

Security Classification	LC Future Center Secret Data		
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VGA Notes List
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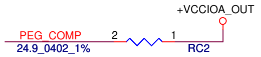
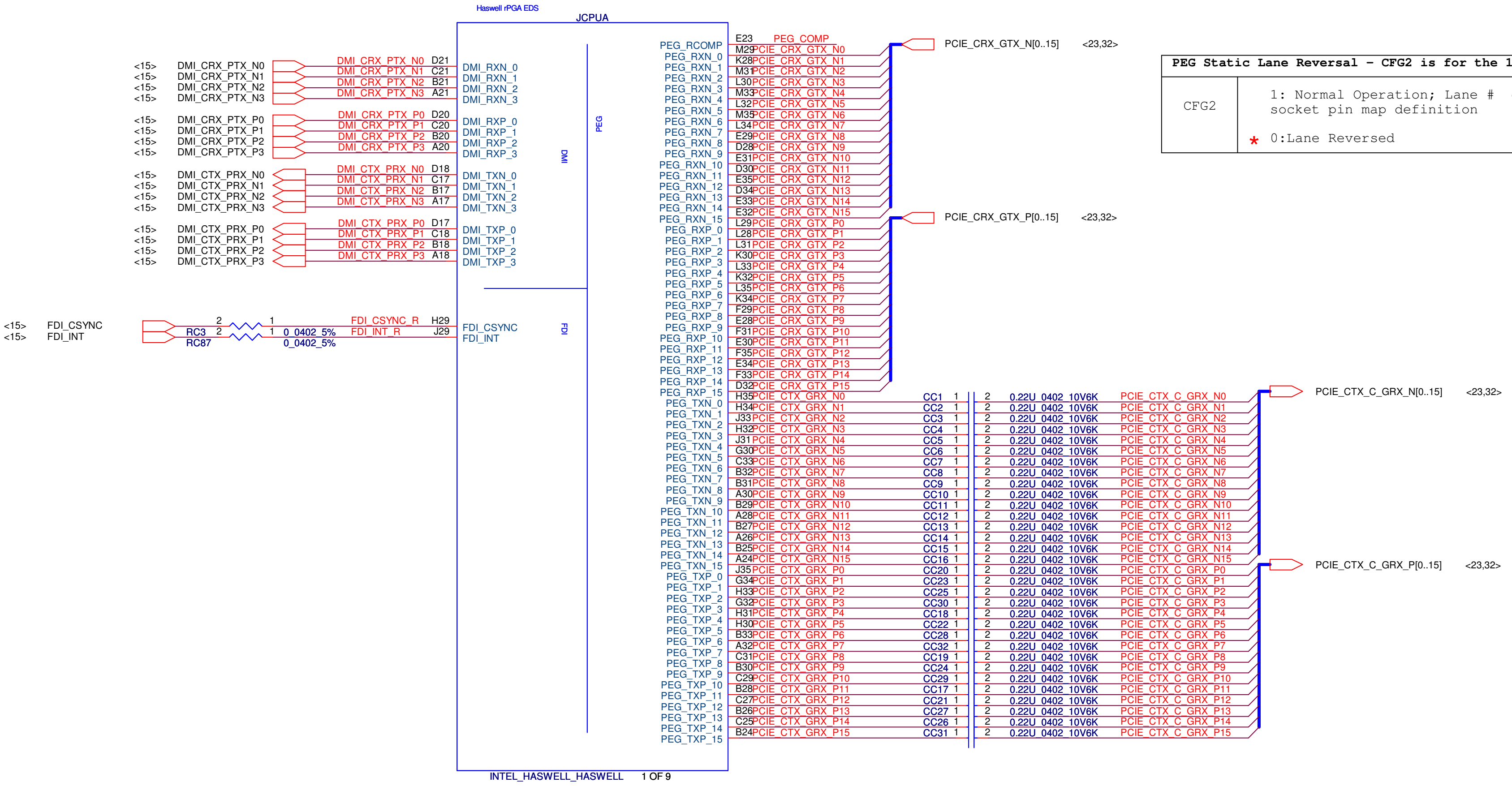


CAD Note:
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed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JCPUA
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<15> DMI_CTX_PRX_N1
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<15> DMI_CTX_PRX_P0
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<15> DMI_CTX_PRX_P3
DMI_CRX_PTX_N0 D21 DMI_RXN_0
DMI_CRX_PTX_N1 C21 DMI_RXN_1
DMI_CRX_PTX_N2 B21 DMI_RXN_2
DMI_CRX_PTX_N3 A21 DMI_RXN_3
DMI_CRX_PTX_P0 D20 DMI_RXP_0
DMI_CRX_PTX_P1 C20 DMI_RXP_1
DMI_CRX_PTX_P2 B20 DMI_RXP_2
DMI_CRX_PTX_P3 A20 DMI_RXP_3
DMI_CTX_PRX_N0 D18 DMI_TXN_0
DMI_CTX_PRX_N1 C17 DMI_TXN_1
DMI_CTX_PRX_N2 B17 DMI_TXN_2
DMI_CTX_PRX_N3 A17 DMI_TXN_3
DMI_CTX_PRX_P0 D17 DMI_TXP_0
DMI_CTX_PRX_P1 C18 DMI_TXP_1
DMI_CTX_PRX_P2 B18 DMI_TXP_2
DMI_CTX_PRX_P3 A18 DMI_TXP_3
DMI
PEG
<15> FDI_CSYNC
<15> FDI_INT
2
1
RC3
2
1
RC87
0_0402_5%
0_0402_5%
FDI_CSYNC_R H29 FDI_CSYNC
FDI_INT_R J29 FDI_INT
FDI
PEG_RCOMP E23 PEG_COMP
PEG_RXN_0 M29 PCIE_CRX_GTX_N0
PEG_RXN_1 K28 PCIE_CRX_GTX_N1
PEG_RXN_2 M31 PCIE_CRX_GTX_N2
PEG_RXN_3 L30 PCIE_CRX_GTX_N3
PEG_RXN_4 M33 PCIE_CRX_GTX_N4
PEG_RXN_5 L32 PCIE_CRX_GTX_N5
PEG_RXN_6 M35 PCIE_CRX_GTX_N6
PEG_RXN_7 L34 PCIE_CRX_GTX_N7
PEG_RXN_8 E29 PCIE_CRX_GTX_N8
PEG_RXN_9 D28 PCIE_CRX_GTX_N9
PEG_RXN_10 E31 PCIE_CRX_GTX_N10
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PEG_RXP_9 E28 PCIE_CRX_GTX_P9
PEG_RXP_10 F31 PCIE_CRX_GTX_P10
PEG_RXP_11 E30 PCIE_CRX_GTX_P11
PEG_RXP_12 F35 PCIE_CRX_GTX_P12
PEG_RXP_13 E34 PCIE_CRX_GTX_P13
PEG_RXP_14 F33 PCIE_CRX_GTX_P14
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PCIE_CRX_GTX_P[0..15] <23,32>
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PEG_TXN_2 J33 PCIE_CTX_GRX_N2 CC3 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N2
PEG_TXN_3 H32 PCIE_CTX_GRX_N3 CC4 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N3
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PEG_TXN_7 B32 PCIE_CTX_GRX_N7 CC8 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N7
PEG_TXN_8 B31 PCIE_CTX_GRX_N8 CC9 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N8
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Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
CPU (1/7) DMI, FDI, PEG

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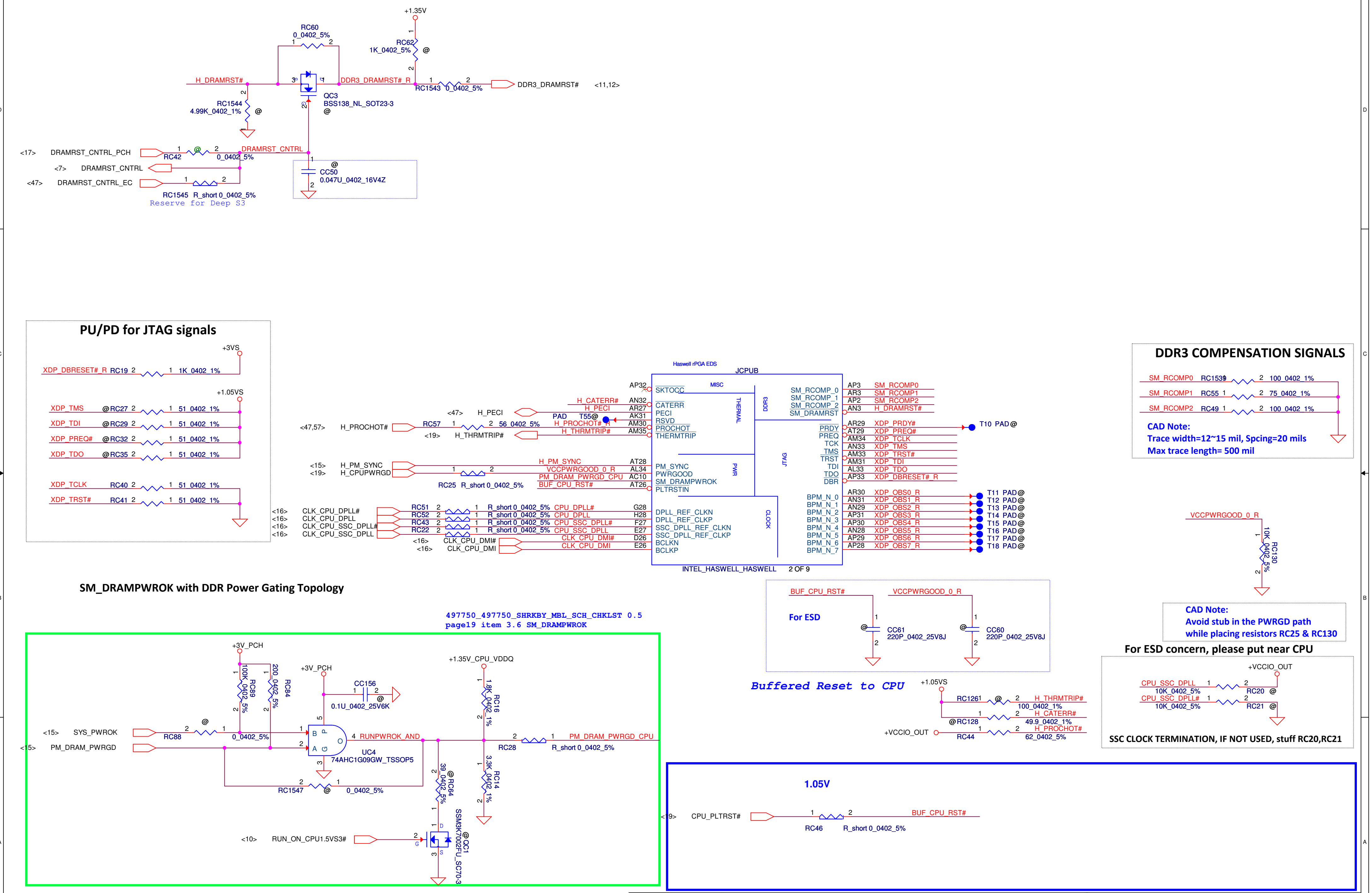
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RC60
0_0402_5%
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H_DRAMRST#
DDR3_DRAMRST#_R
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BSS138_NL_SOT23-3
RC1544
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CC50
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RC1545 R_short 0_0402_5%
Reserve for Deep S3
PU/PD for JTAG signals
+3VS
XDP_DBRESET#_R RC19 1K_0402_1%
+1.05VS
XDP_TMS @RC27 51_0402_1%
XDP_TDI @RC29 51_0402_1%
XDP_PREQ# @RC32 51_0402_1%
XDP_TDO @RC35 51_0402_1%
XDP_TCLK RC40 51_0402_1%
XDP_TRST# RC41 51_0402_1%
Haswell rPGA EDS
JCPUB
MISC
THERMAL
DDR3
JTAG
PWR
CLOCK
AP32 SKTOCC
AN32 H_CATERR# CATERR
AR27 H_PECI PECI
AK31 RSVD
AM30 H_PROCHOT#_R PROCHOT
AM35 H_THRMTRIP# THERMTRIP
<47> H_PECI
PAD T55@
<47,57> H_PROCHOT# RC57 56_0402_5%
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RC25 R_short 0_0402_5%
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PREQ AT29 XDP_PREQ#
TCK AM34 XDP_TCLK
TMS AN33 XDP_TMS
TRST AM33 XDP_TRST#
TDI AM31 XDP_TDI
TDO AL33 XDP_TDO
DBR AP33 XDP_DBRESET#_R
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BPM_N_1 AN31 XDP_OBS1_R T12 PAD@
BPM_N_2 AN29 XDP_OBS2_R T13 PAD@
BPM_N_3 AP31 XDP_OBS3_R T14 PAD@
BPM_N_4 AP30 XDP_OBS4_R T15 PAD@
BPM_N_5 AN28 XDP_OBS5_R T16 PAD@
BPM_N_6 AP29 XDP_OBS6_R T17 PAD@
BPM_N_7 AP28 XDP_OBS7_R T18 PAD@
INTEL_HASWELL_HASWELL 2 OF 9
DDR3 COMPENSATION SIGNALS
SM_RCOMP0 RC1539 100_0402_1%
SM_RCOMP1 RC55 75_0402_1%
SM_RCOMP2 RC49 100_0402_1%
CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil
VCCPWRGOOD_0_R
RC130 10K_0402_5%
CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC25 & RC130
BUF_CPU_RST#
VCCPWRGOOD_0_R
For ESD
CC61 220P_0402_25V8J
CC60 220P_0402_25V8J
For ESD concern, please put near CPU
Buffered Reset to CPU
+1.05VS
RC1261 H_THRMTRIP#
100_0402_1%
@RC128 H_CATERR#
49.9_0402_1%
+VCCIO_OUT RC44 H_PROCHOT#
62_0402_5%
+VCCIO_OUT
CPU_SSC_DPLL RC20 10K_0402_5%
CPU_SSC_DPLL# RC21 10K_0402_5%
SSC CLOCK TERMINATION, IF NOT USED, stuff RC20,RC21
SM_DRAMPWROK with DDR Power Gating Topology
497750_497750_SHRKBY_MBL_SCH_CHKLST 0.5
page19 item 3.6 SM_DRAMPWROK
+3V_PCH
RC89 100K_0402_5%
RC84 200_0402_5%
+3V_PCH
CC156 0.1U_0402_25V6K
+1.35V_CPU_VDDQ
RC16 1.8K_0402_1%
<15> SYS_PWROK RC88 0_0402_5%
<15> PM_DRAM_PWRGD
UC4 74AHC1G09GW_TSSOP5
RUNPWROK_AND
RC28 R_short 0_0402_5% PM_DRAM_PWRGD_CPU
RC1547 0_0402_5%
RC64 39_0402_5%
RC14 3.3K_0402_1%
<10> RUN_ON_CPU1.5VS3#
QC1 SSM3K7002FU_SC70-3
1.05V
<19> CPU_PLTRST# RC46 R_short 0_0402_5% BUF_CPU_RST#

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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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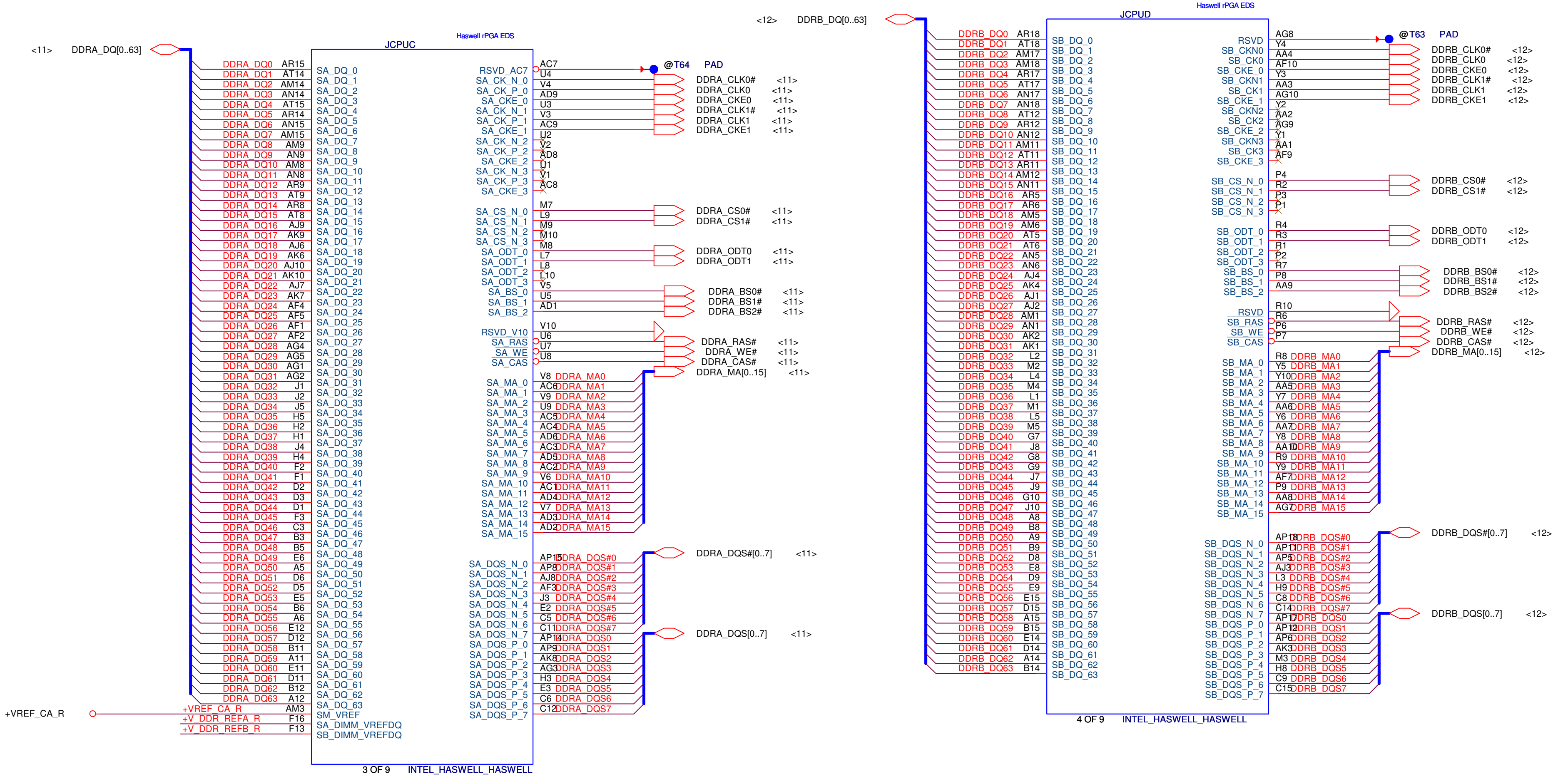
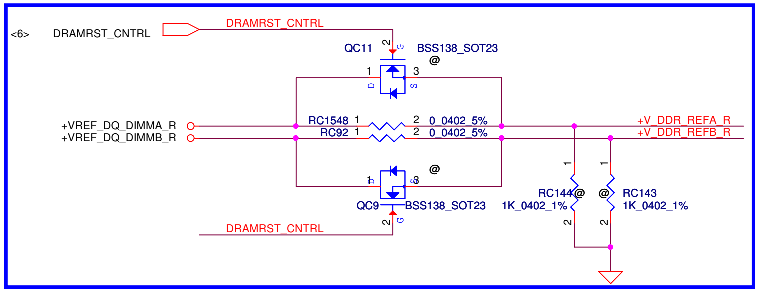
Title
CPU (2/7) PM, XDP, CLK

LCFC

Size Custom
Document Number Y401 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013
Sheet 6 of 69





6/8: Add M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title

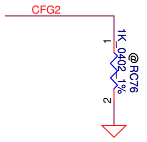
CPU (3/7) DDRIII

LCFC

Size	Document Number	Rev
Custom	Y401 NM-A031	1.0

Date: Wednesday, March 27, 2013 | Sheet 7 of 69

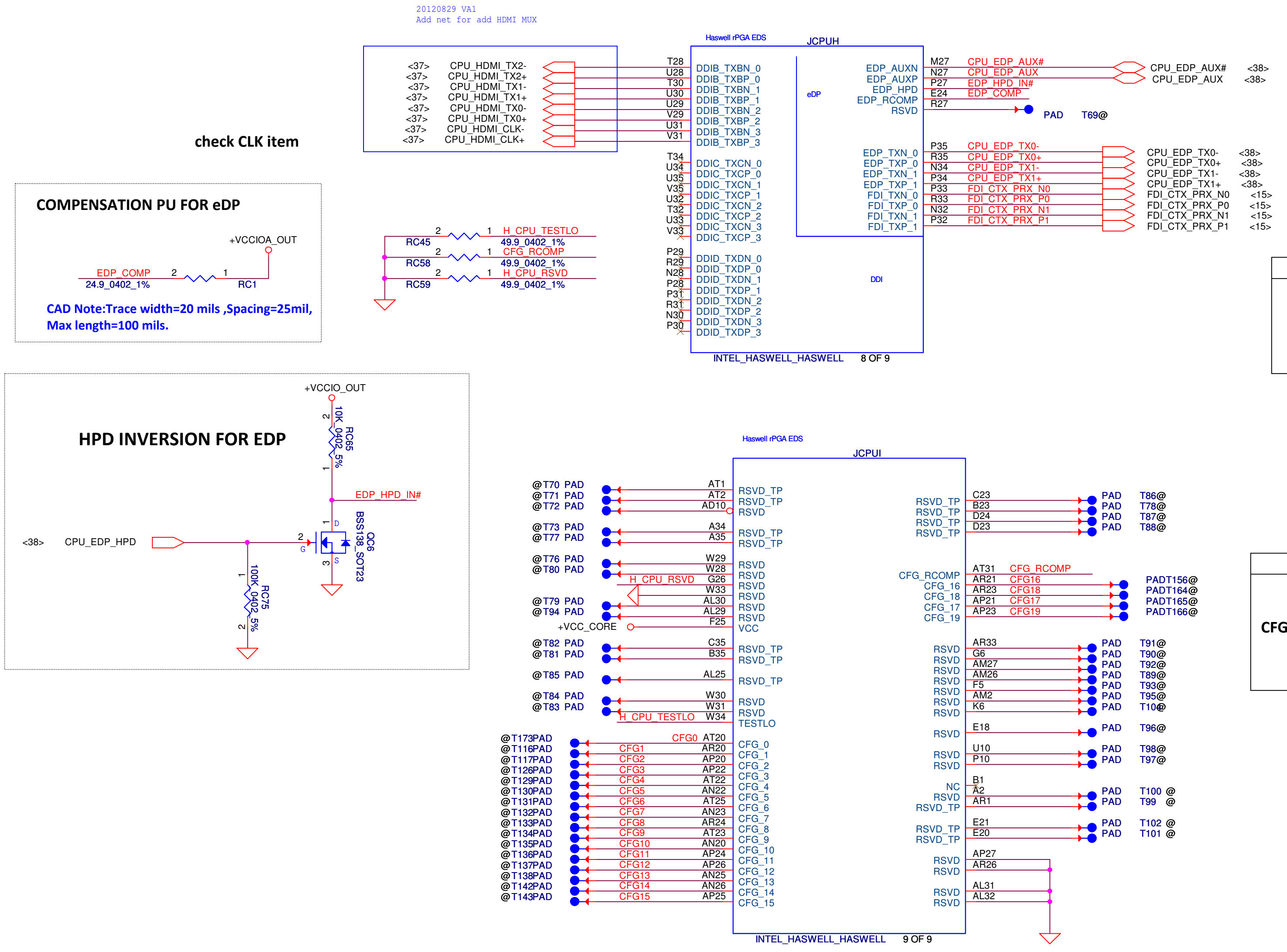
CFG STRAPS for CPU



PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	★ 1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

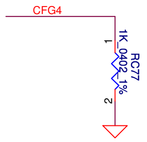
check CLK item



COMPENSATION PU FOR eDP

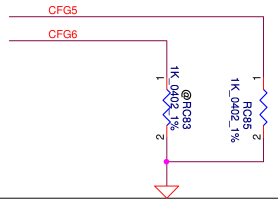
CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

HPD INVERSION FOR EDP



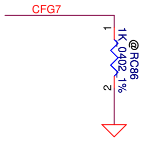
Display Port Presence Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps

CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled * 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING

CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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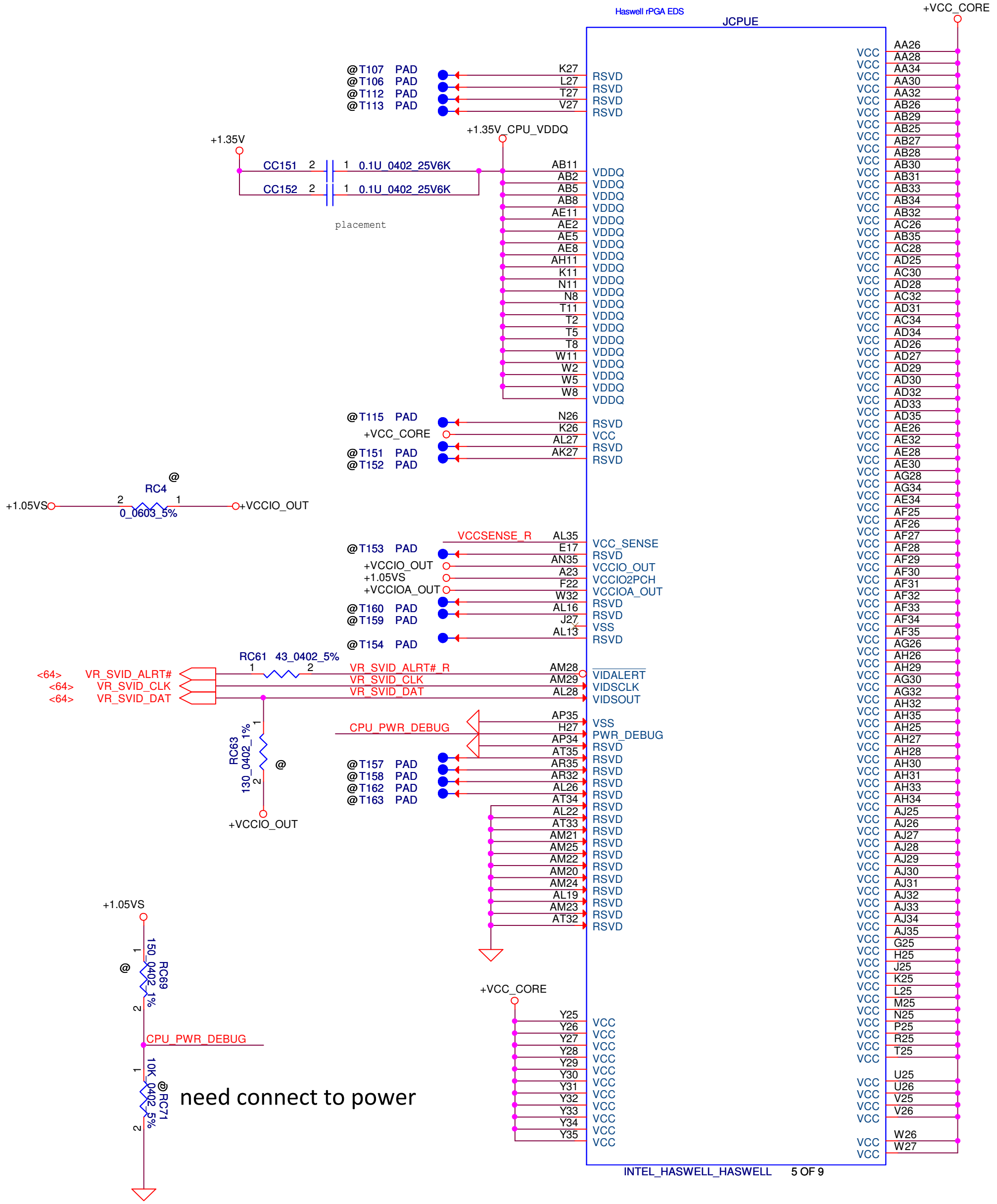
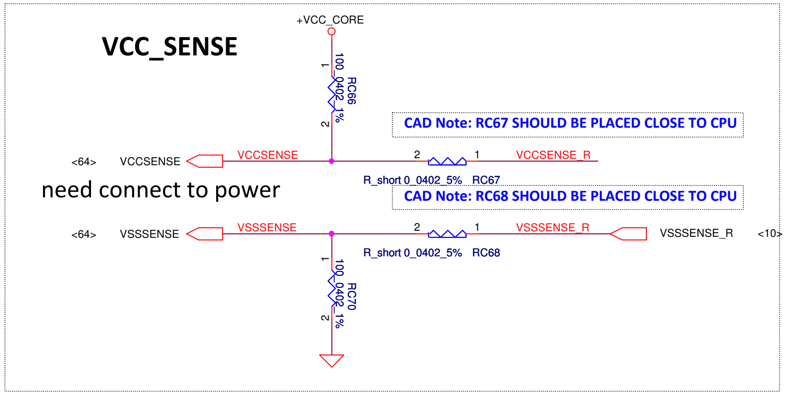
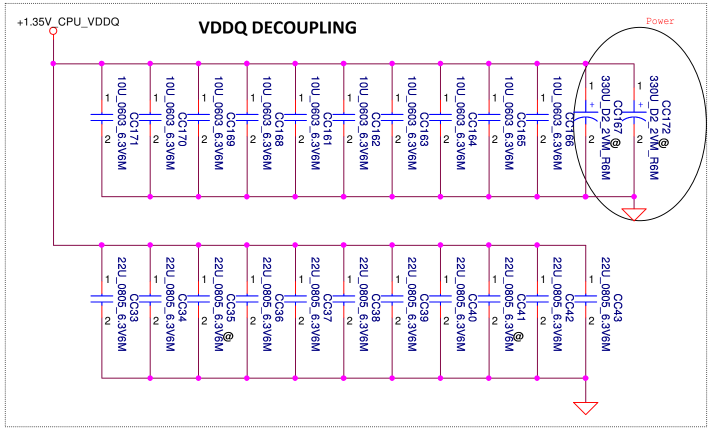
Title
CPU (4/7) RSVD,CFG

Size: Custom
Document Number: Y401 NM-A031
Rev: 1.0
Date: Wednesday, March 27, 2013
Sheet 8 of 69


Haswell rPGA EDS
JCPUE
+VCC_CORE
@T107 PAD
@T106 PAD
@T112 PAD
@T113 PAD
K27 L27 T27 V27
RSVD
+1.35V
+1.35V_CPU_VDDQ
CC151 2 1 0.1U_0402_25V6K
CC152 2 1 0.1U_0402_25V6K
placement
AB11 AB2 AB5 AB8 AE11 AE2 AE5 AE8 AH11 K11 N11 N8 T11 T2 T5 T8 W11 W2 W5 W8
VDDQ
@T115 PAD
+VCC_CORE
@T151 PAD
@T152 PAD
N26 K26 AL27 AK27
+1.05VS
RC4
@
2 1
0_0603_5%
+VCCIO_OUT
VCCSENSE_R
@T153 PAD
+VCCIO_OUT
+1.05VS
+VCCIOA_OUT
@T160 PAD
@T159 PAD
@T154 PAD
AL35 E17 AN35 A23 F22 W32 AL16 J27 AL13
VCC_SENSE
VCCIO_OUT
VCCIO2PCH
VCCIOA_OUT
RC61 43_0402_5%
<64> VR_SVID_ALRT#
<64> VR_SVID_CLK
<64> VR_SVID_DAT
VR_SVID_ALRT#_R
AM28 AM29 AL28
VIDALERT
VIDSCLK
VIDSOUT
RC63 130_0402_1%
@
+VCCIO_OUT
CPU_PWR_DEBUG
AP35 H27 AP34 AT35 AR35 AR32 AL26 AT34
VSS
PWR_DEBUG
@T157 PAD
@T158 PAD
@T162 PAD
@T163 PAD
AL22 AT33 AM21 AM25 AM22 AM20 AM24 AL19 AM23 AT32
+1.05VS
RC69 150_0402_1%
@
CPU_PWR_DEBUG
RC71 10K_0402_5%
@
need connect to power
+VCC_CORE
Y25 Y26 Y27 Y28 Y29 Y30 Y31 Y32 Y33 Y34 Y35
VCC
AA26 AA28 AA34 AA30 AA32 AB26 AB29 AB25 AB27 AB28 AB30 AB31 AB33 AB34 AB32 AC26 AB35 AC28 AD25 AC30 AD28 AC32 AD31 AC34 AD34 AD26 AD27 AD29 AD30 AD32 AD33 AD35 AE26 AE32 AE28 AE30 AG28 AG34 AE34 AF25 AF26 AF27 AF28 AF29 AF30 AF31 AF32 AF33 AF34 AF35 AG26 AH26 AH29 AG30 AG32 AH32 AH35 AH25 AH27 AH28 AH30 AH31 AH33 AH34 AJ25 AJ26 AJ27 AJ28 AJ29 AJ30 AJ31 AJ32 AJ33 AJ34 AJ35 G25 H25 J25 K25 L25 M25 N25 P25 R25 T25 U25 U26 V25 V26 W26 W27
INTEL_HASWELL_HASWELL
5 OF 9


VCC_SENSE

need connect to power


VDDQ DECOUPLING

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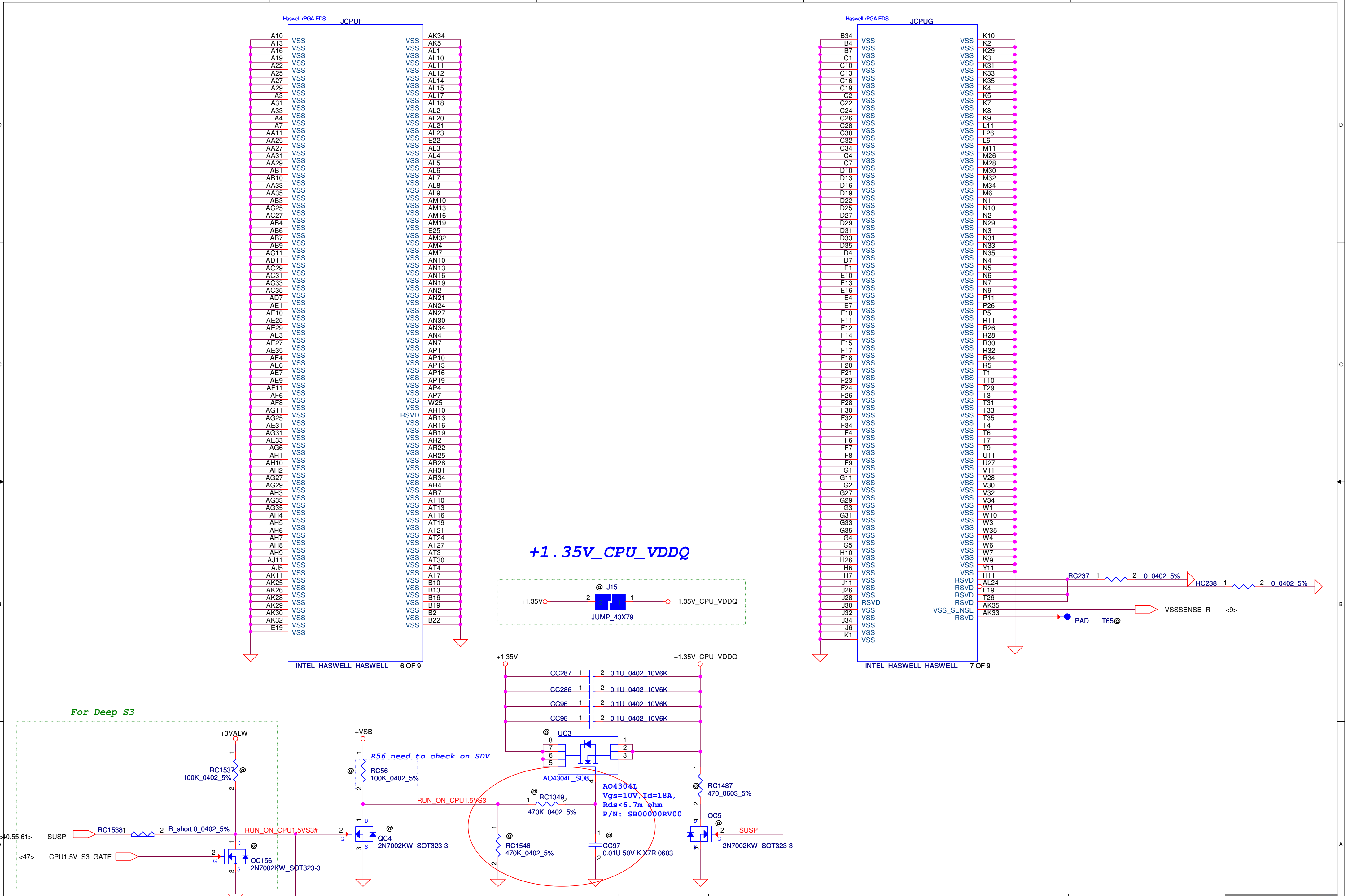
Title
CPU (5/7) PWR, BYPASS

Size Custom
Document Number Y401 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013
Sheet 9 of 69



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Title
CPU (6/7) PWR

LCFC

Size Custom
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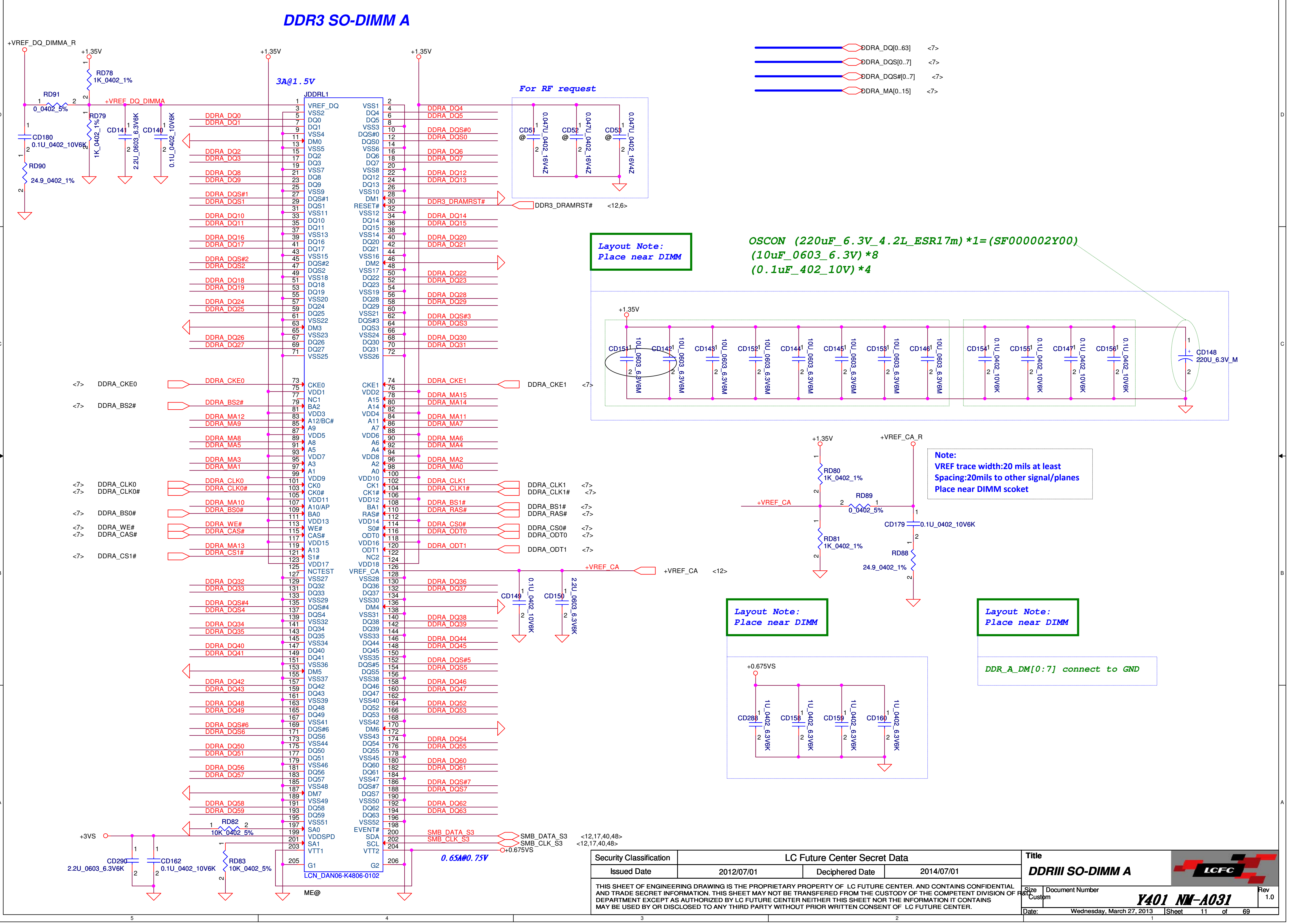
DDR3 SO-DIMM A



Layout Note:
Place near DIMM

OSCON (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM scoket

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

DDR_A_DM[0:7] connect to GND

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
DDRIII SO-DIMM A

Size: Custom
Document Number: Y401 NM-A031
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Date: Wednesday, March 27, 2013
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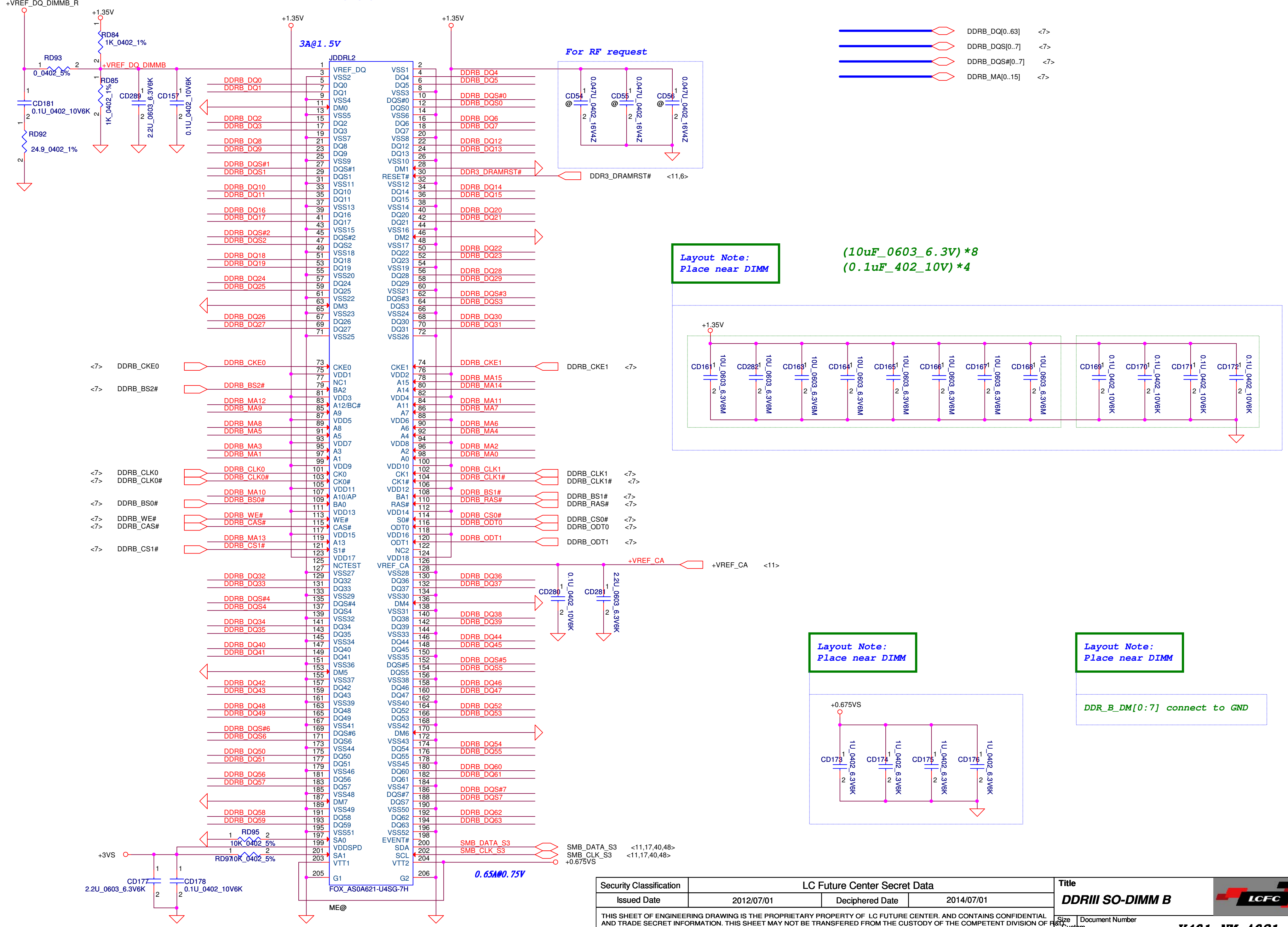
DDR3 SO-DIMM B



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Title
DDRIII SO-DIMM B

LCFC

Size: Custom
Document Number: Y401 NM-A031
Rev: 1.0
Date: Wednesday, March 27, 2013
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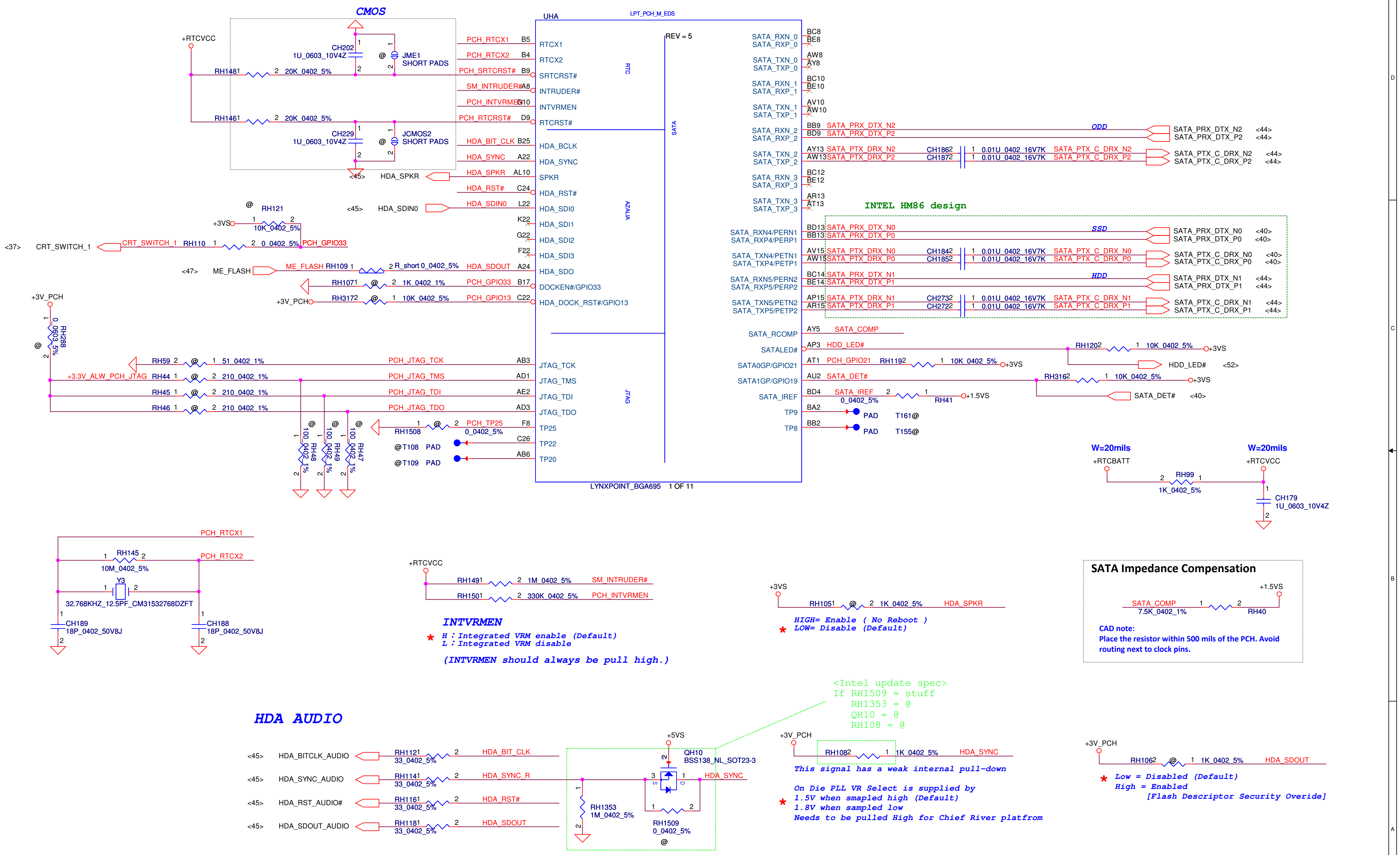
Place JUMPER under RAM door



INTEL HM86 design

W=20mils

W=20mils

INTVRMEN

★ H : Integrated VRM enable (Default)
L : Integrated VRM disable

(INTVRMEN should always be pull high.)

★ HIGH= Enable (No Reboot)
LOW= Disable (Default)

SATA Impedance Compensation

CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

<Intel update spec>
If RH1509 = stuff
RH1353 = @
QH10 = @
RH108 = @

HDA AUDIO

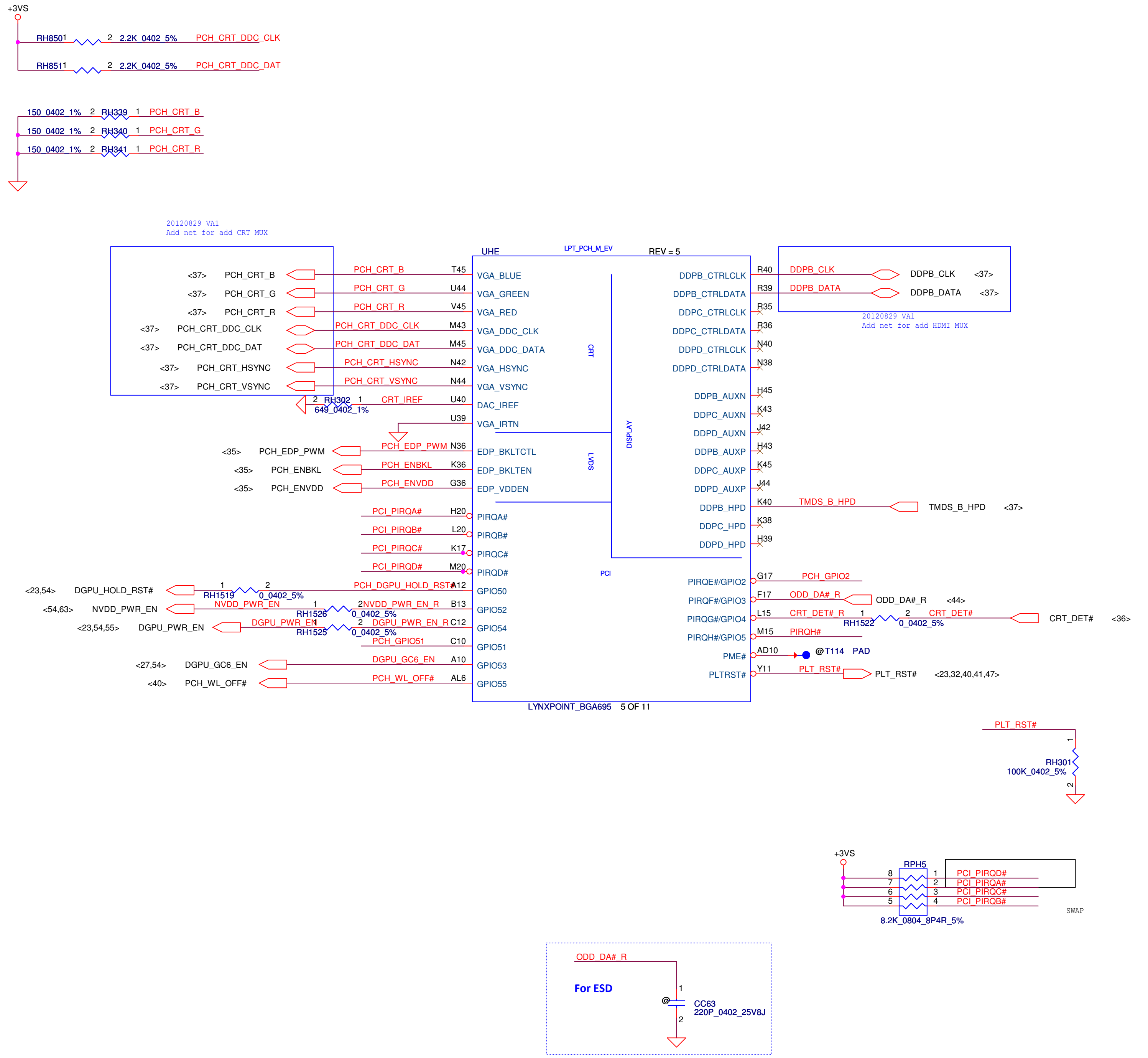
This signal has a weak internal pull-down

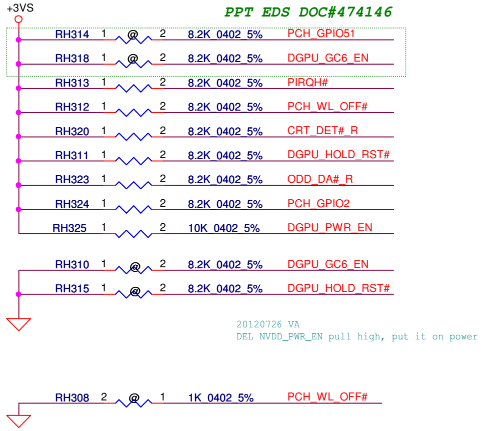
★ On Die PLL VR Select is supplied by
1.5V when smapled high (Default)
1.8V when sampled low
Needs to be pulled High for Chief River platfrom

★ Low = Disabled (Default)
High = Enabled
[Flash Descriptor Security Overide]

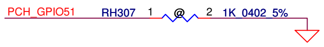
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
PCH (1/9) SATA,HDA,SPI, LPC
Size Custom
Document Number Y401 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013




+3VS
PPT EDS DOC#474146
RH314 1 @ 2 8.2K_0402_5% PCH_GPIO51
RH318 1 @ 2 8.2K_0402_5% DGPU_GC6_EN
RH313 1 2 8.2K_0402_5% PIRQH#
RH312 1 2 8.2K_0402_5% PCH_WL_OFF#
RH320 1 2 8.2K_0402_5% CRT_DET#_R
RH311 1 2 8.2K_0402_5% DGPU_HOLD_RST#
RH323 1 2 8.2K_0402_5% ODD_DA#_R
RH324 1 2 8.2K_0402_5% PCH_GPIO2
RH325 1 2 10K_0402_5% DGPU_PWR_EN
RH310 1 @ 2 8.2K_0402_5% DGPU_GC6_EN
RH315 1 @ 2 8.2K_0402_5% DGPU_HOLD_RST#
20120726 VA
DEL NVDD_PWR_EN pull high, put it on power
RH308 2 @ 1 1K_0402_5% PCH_WL_OFF#

A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled ***High=Default



Boot BIOS Strap

BBS_BIT1 (GPIO51)	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
* 1	1	SPI

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Title
PCH (2/9) PCIE, SMBUS, CLK

LCFC

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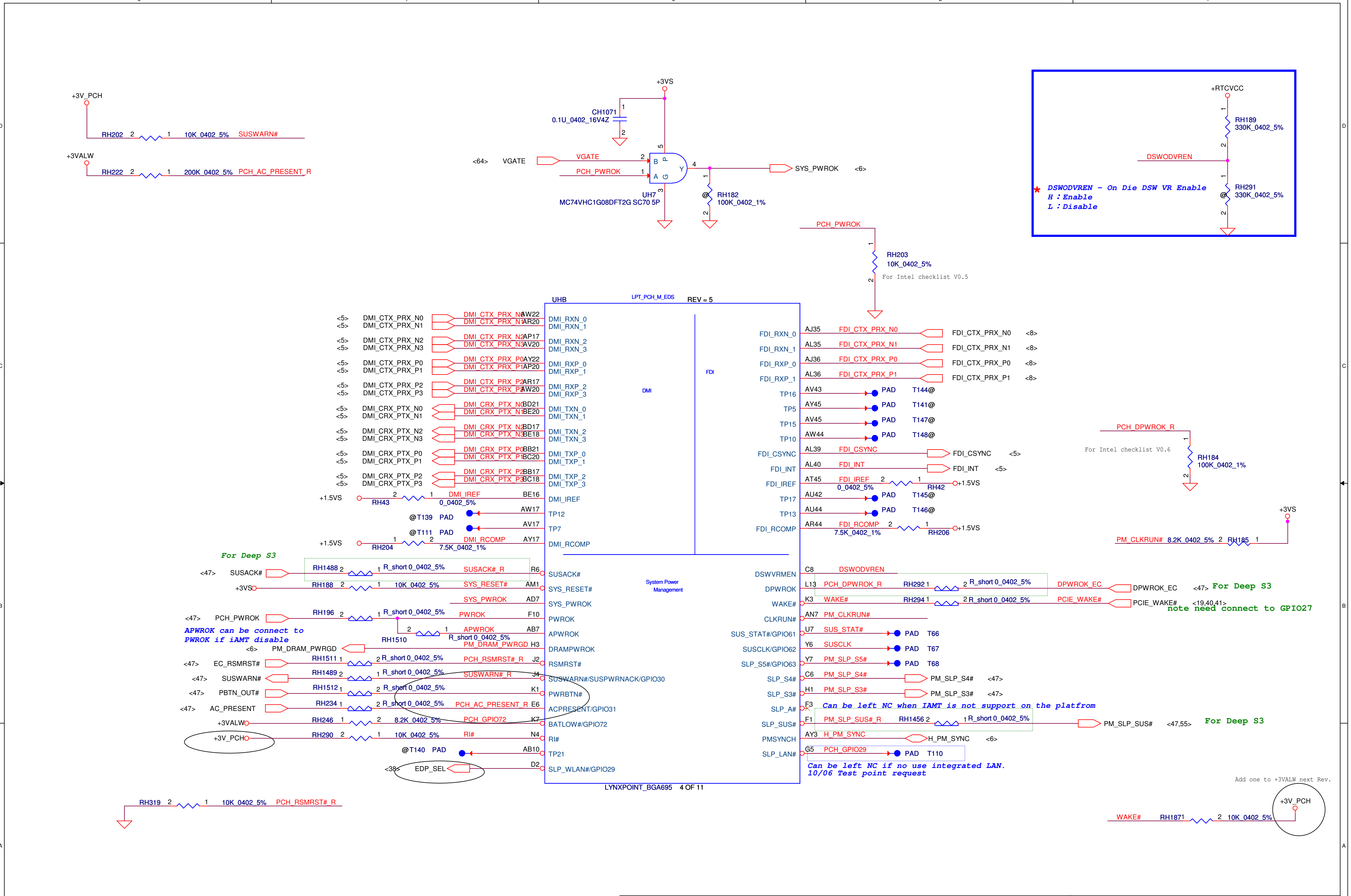
+3V_PCH
RH202 2 1 10K_0402_5% SUSWARN#
+3VALW
RH222 2 1 200K_0402_5% PCH_AC_PRESENT_R
+3VS
CH1071
0.1U_0402_16V4Z
<64> VGATE
VGATE
PCH_PWROK
B P
A G
Y
UH7
MC74VHC1G08DFT2G SC70 5P
SYS_PWROK <6>
@ RH182
100K_0402_1%
+RTCVCC
RH189
330K_0402_5%
DSWODVREN
@ RH291
330K_0402_5%
PCH_PWROK
RH203
10K_0402_5%
UHB
LPT_PCH_M_EDS
REV = 5
DMI
FDI
<5> DMI_CTX_PRX_N0 AW22 DMI_RXN_0
<5> DMI_CTX_PRX_N1 AR20 DMI_RXN_1
<5> DMI_CTX_PRX_N2 AP17 DMI_RXN_2
<5> DMI_CTX_PRX_N3 AV20 DMI_RXN_3
<5> DMI_CTX_PRX_P0 AY22 DMI_RXP_0
<5> DMI_CTX_PRX_P1 AP20 DMI_RXP_1
<5> DMI_CTX_PRX_P2 AR17 DMI_RXP_2
<5> DMI_CTX_PRX_P3 AW20 DMI_RXP_3
<5> DMI_CRX_PTX_N0 BD21 DMI_TXN_0
<5> DMI_CRX_PTX_N1 BE20 DMI_TXN_1
<5> DMI_CRX_PTX_N2 BD17 DMI_TXN_2
<5> DMI_CRX_PTX_N3 BE18 DMI_TXN_3
<5> DMI_CRX_PTX_P0 BB21 DMI_TXP_0
<5> DMI_CRX_PTX_P1 BC20 DMI_TXP_1
<5> DMI_CRX_PTX_P2 BB17 DMI_TXP_2
<5> DMI_CRX_PTX_P3 BC18 DMI_TXP_3
+1.5VS RH43 2 1 DMI_IREF 0_0402_5% BE16 DMI_IREF
@T139 PAD AW17 TP12
@T111 PAD AV17 TP7
+1.5VS RH204 1 2 DMI_RCOMP 7.5K_0402_1% AY17 DMI_RCOMP
FDI_RXN_0 AJ35 FDI_CTX_PRX_N0 FDI_CTX_PRX_N0 <8>
FDI_RXN_1 AL35 FDI_CTX_PRX_N1 FDI_CTX_PRX_N1 <8>
FDI_RXP_0 AJ36 FDI_CTX_PRX_P0 FDI_CTX_PRX_P0 <8>
FDI_RXP_1 AL36 FDI_CTX_PRX_P1 FDI_CTX_PRX_P1 <8>
TP16 AV43 PAD T144@
TP5 AY45 PAD T141@
TP15 AV45 PAD T147@
TP10 AW44 PAD T148@
FDI_CSYNC AL39 FDI_CSYNC FDI_CSYNC <5>
FDI_INT AL40 FDI_INT FDI_INT <5>
FDI_IREF AT45 FDI_IREF 2 1 +1.5VS 0_0402_5% RH42
TP17 AU42 PAD T145@
TP13 AU44 PAD T146@
FDI_RCOMP AR44 FDI_RCOMP 2 1 +1.5VS 7.5K_0402_1% RH206
PCH_DPWROK_R
RH184
100K_0402_1%
+3VS
PM_CLKRUN# 8.2K_0402_5% 2 RH185 1
System Power Management
<47> SUSACK# RH1488 2 1 R_short 0_0402_5% SUSACK#_R R6 SUSACK#
+3VS RH188 2 1 10K_0402_5% SYS_RESET# AM1 SYS_RESET#
SYS_PWROK AD7 SYS_PWROK
<47> PCH_PWROK RH196 2 1 R_short 0_0402_5% PWROK F10 PWROK
RH1510 2 1 R_short 0_0402_5% APWROK AB7 APWROK
<6> PM_DRAM_PWRGD PM_DRAM_PWRGD H3 DRAMPWROK
<47> EC_RSMRST# RH1511 1 2 R_short 0_0402_5% PCH_RSMRST#_R J2 RSMRST#
<47> SUSWARN# RH1489 2 1 R_short 0_0402_5% SUSWARN#_R J4 SUSWARN#/SUSPWRNACK/GPIO30
<47> PBTN_OUT# RH1512 1 2 R_short 0_0402_5% K1 PWRBTN#
<47> AC_PRESENT RH234 1 2 R_short 0_0402_5% PCH_AC_PRESENT_R E6 ACPRESENT/GPIO31
+3VALW RH246 1 2 8.2K_0402_5% PCH_GPIO72 K7 BATLOW#/GPIO72
+3V_PCH RH290 2 1 10K_0402_5% RI# N4 RI#
@T140 PAD AB10 TP21
<38> EDP_SEL D2 SLP_WLAN#/GPIO29
DSWVRMEN C8 DSWODVREN
DPWROK L13 PCH_DPWROK_R RH292 1 2 R_short 0_0402_5% DPWROK_EC DPWROK_EC <47>
WAKE# K3 WAKE# RH294 1 2 R_short 0_0402_5% PCIE_WAKE# PCIE_WAKE# <19,40,41>
CLKRUN# AN7 PM_CLKRUN#
SUS_STAT#/GPIO61 U7 SUS_STAT# PAD T66
SUSCLK/GPIO62 Y6 SUSCLK PAD T67
SLP_S5#/GPIO63 Y7 PM_SLP_S5# PAD T68
SLP_S4# C6 PM_SLP_S4# PM_SLP_S4# <47>
SLP_S3# H1 PM_SLP_S3# PM_SLP_S3# <47>
SLP_A# F3
SLP_SUS# F1 PM_SLP_SUS#_R RH1456 2 1 R_short 0_0402_5% PM_SLP_SUS# <47,55>
PMSYNCH AY3 H_PM_SYNC H_PM_SYNC <6>
SLP_LAN# G5 PCH_GPIO29 PAD T110
LYNXPOINT_BGA695 4 OF 11
RH319 2 1 10K_0402_5% PCH_RSMRST#_R
+3V_PCH
WAKE# RH1871 2 10K_0402_5%

DSWODVREN - On Die DSW VR Enable
H : Enable
L : Disable

For Intel checklist V0.5

For Intel checklist V0.6

For Deep S3

APWROK can be connect to
PWROK if iAMT disable

For Deep S3

note need connect to GPIO27

Can be left NC when IAMT is not support on the platfrom

For Deep S3

Can be left NC if no use integrated LAN.
10/06 Test point request

Add one to +3VALW next Rev.

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
PCH (3/9) PCIE, SMBUS, CLK

LCFC

Size: Custom
Document Number: Y401 NM-A031
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Date: Wednesday, March 27, 2013
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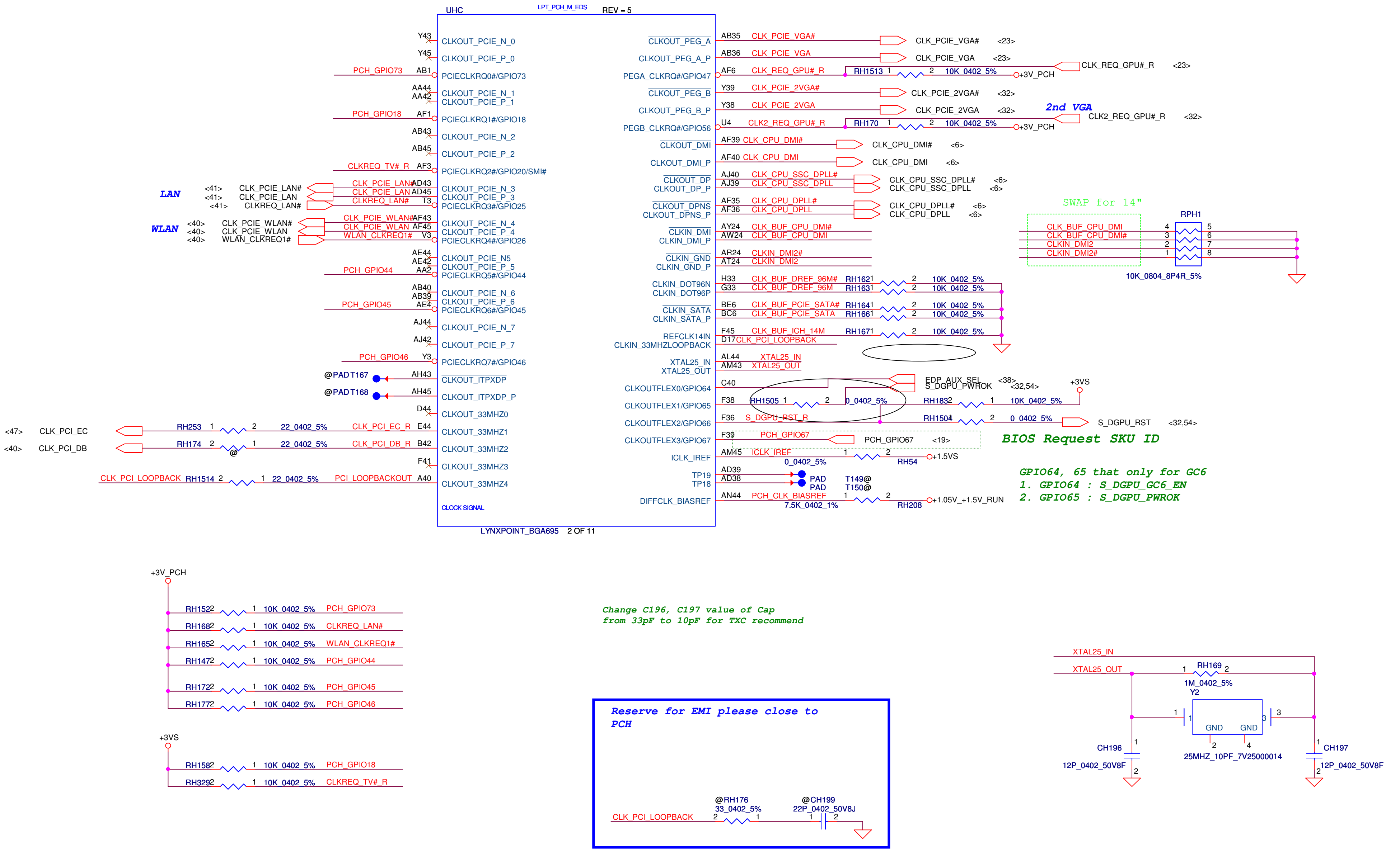

BIOS Request SKU ID

GPIO64, 65 that only for GC6
1. GPIO64 : S_DGPU_GC6_EN
2. GPIO65 : S_DGPU_PWROK

Change C196, C197 value of Cap
from 33pF to 10pF for TXC recommend

Reserve for EMI please close to PCH

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
PCH (3/9) DMI, FDI, PM

LCFC

Size: Custom
Document Number: Y401 NM-A031
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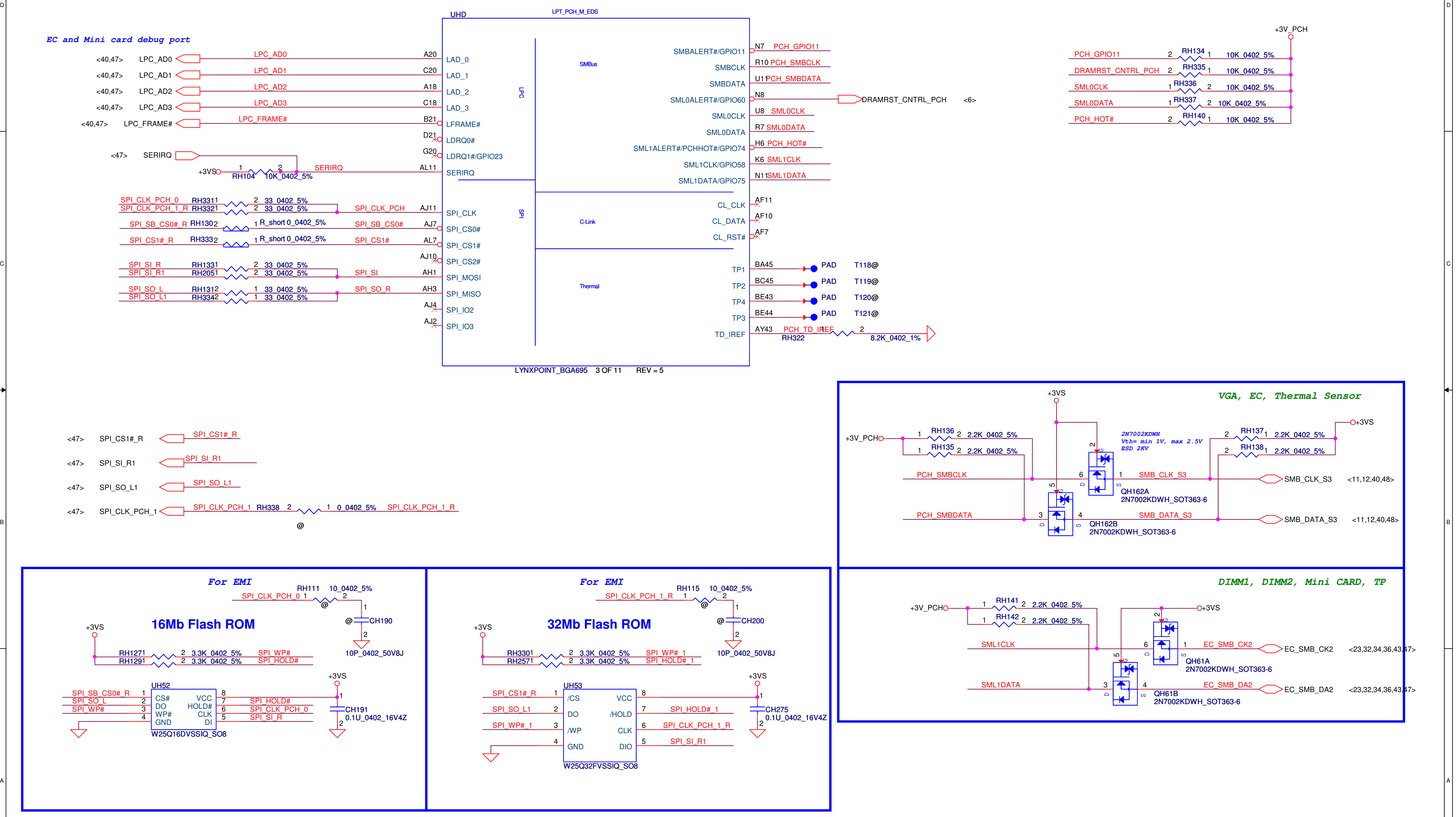
EC and Mini card debug port
UHD
LPT_PCH_M_EDS
<40,47> LPC_AD0
<40,47> LPC_AD1
<40,47> LPC_AD2
<40,47> LPC_AD3
<40,47> LPC_FRAME#
<47> SERIRQ
+3VS
RH104 10K_0402_5%
SERIRQ
LPC_AD0 A20 LAD_0
LPC_AD1 C20 LAD_1
LPC_AD2 A18 LAD_2
LPC_AD3 C18 LAD_3
LPC_FRAME# B21 LFRAME#
D21 LDRQ0#
G20 LDRQ1#/GPIO23
AL11 SERIRQ
LPC
SMBus
SMBALERT#/GPIO11 N7 PCH_GPIO11
SMBCLK R10 PCH_SMBCLK
SMBDATA U11 PCH_SMBDATA
SML0ALERT#/GPIO60 N8 DRAMRST_CNTRL_PCH <6>
SML0CLK U8 SML0CLK
SML0DATA R7 SML0DATA
SML1ALERT#/PCHHOT#/GPIO74 H6 PCH_HOT#
SML1CLK/GPIO58 K6 SML1CLK
SML1DATA/GPIO75 N11 SML1DATA
SPI_CLK_PCH_0 RH3311 33_0402_5%
SPI_CLK_PCH_1_R RH3321 33_0402_5%
SPI_SB_CS0#_R RH1302 R_short 0_0402_5%
SPI_CS1#_R RH333 R_short 0_0402_5%
SPI_SI_R RH1331 33_0402_5%
SPI_SI_R1 RH2051 33_0402_5%
SPI_SO_L RH1312 33_0402_5%
SPI_SO_L1 RH3342 33_0402_5%
SPI_CLK_PCH AJ11 SPI_CLK
SPI_SB_CS0# AJ7 SPI_CS0#
SPI_CS1# AL7 SPI_CS1#
AJ10 SPI_CS2#
SPI_SI AH1 SPI_MOSI
SPI_SO_R AH3 SPI_MISO
AJ4 SPI_IO2
AJ2 SPI_IO3
SPI
C-Link
CL_CLK AF11
CL_DATA AF10
CL_RST# AF7
Thermal
TP1 BA45 PAD T118@
TP2 BC45 PAD T119@
TP4 BE43 PAD T120@
TP3 BE44 PAD T121@
TD_IREF AY43 PCH_TD_IREF RH322 8.2K_0402_1%
LYNXPOINT_BGA695 3 OF 11 REV = 5
+3V_PCH
PCH_GPIO11 RH134 10K_0402_5%
DRAMRST_CNTRL_PCH RH335 10K_0402_5%
SML0CLK RH336 10K_0402_5%
SML0DATA RH337 10K_0402_5%
PCH_HOT# RH140 10K_0402_5%
<47> SPI_CS1#_R
<47> SPI_SI_R1
<47> SPI_SO_L1
<47> SPI_CLK_PCH_1 RH338 0_0402_5% SPI_CLK_PCH_1_R @
VGA, EC, Thermal Sensor
+3VS
+3V_PCH
RH136 2.2K_0402_5%
RH135 2.2K_0402_5%
RH137 2.2K_0402_5%
RH138 2.2K_0402_5%
2N7002KDWH Vth= min 1V, max 2.5V ESD 2KV
PCH_SMBCLK SMB_CLK_S3 SMB_CLK_S3 <11,12,40,48>
PCH_SMBDATA SMB_DATA_S3 SMB_DATA_S3 <11,12,40,48>
QH162A 2N7002KDWH_SOT363-6
QH162B 2N7002KDWH_SOT363-6
DIMM1, DIMM2, Mini CARD, TP
RH141 2.2K_0402_5%
RH142 2.2K_0402_5%
SML1CLK EC_SMB_CK2 EC_SMB_CK2 <23,32,34,36,43,47>
SML1DATA EC_SMB_DA2 EC_SMB_DA2 <23,32,34,36,43,47>
QH61A 2N7002KDWH_SOT363-6
QH61B 2N7002KDWH_SOT363-6
For EMI
RH111 10_0402_5% SPI_CLK_PCH_0 @
CH190 10P_0402_50V8J @
16Mb Flash ROM
RH1271 3.3K_0402_5% SPI_WP#
RH1291 3.3K_0402_5% SPI_HOLD#
UH52
SPI_SB_CS0#_R CS# VCC
SPI_SO_L DO HOLD# SPI_HOLD#
SPI_WP# WP# CLK SPI_CLK_PCH_0
GND DI SPI_SI_R
W25Q16DVSSIQ_SO8
CH191 0.1U_0402_16V4Z
For EMI
RH115 10_0402_5% SPI_CLK_PCH_1_R @
CH200 10P_0402_50V8J @
32Mb Flash ROM
RH3301 3.3K_0402_5% SPI_WP#_1
RH2571 3.3K_0402_5% SPI_HOLD#_1
UH53
SPI_CS1#_R /CS VCC
SPI_SO_L1 DO /HOLD SPI_HOLD#_1
SPI_WP#_1 /WP CLK SPI_CLK_PCH_1_R
GND DIO SPI_SI_R1
W25Q32FVSSIQ_SO8
CH275 0.1U_0402_16V4Z

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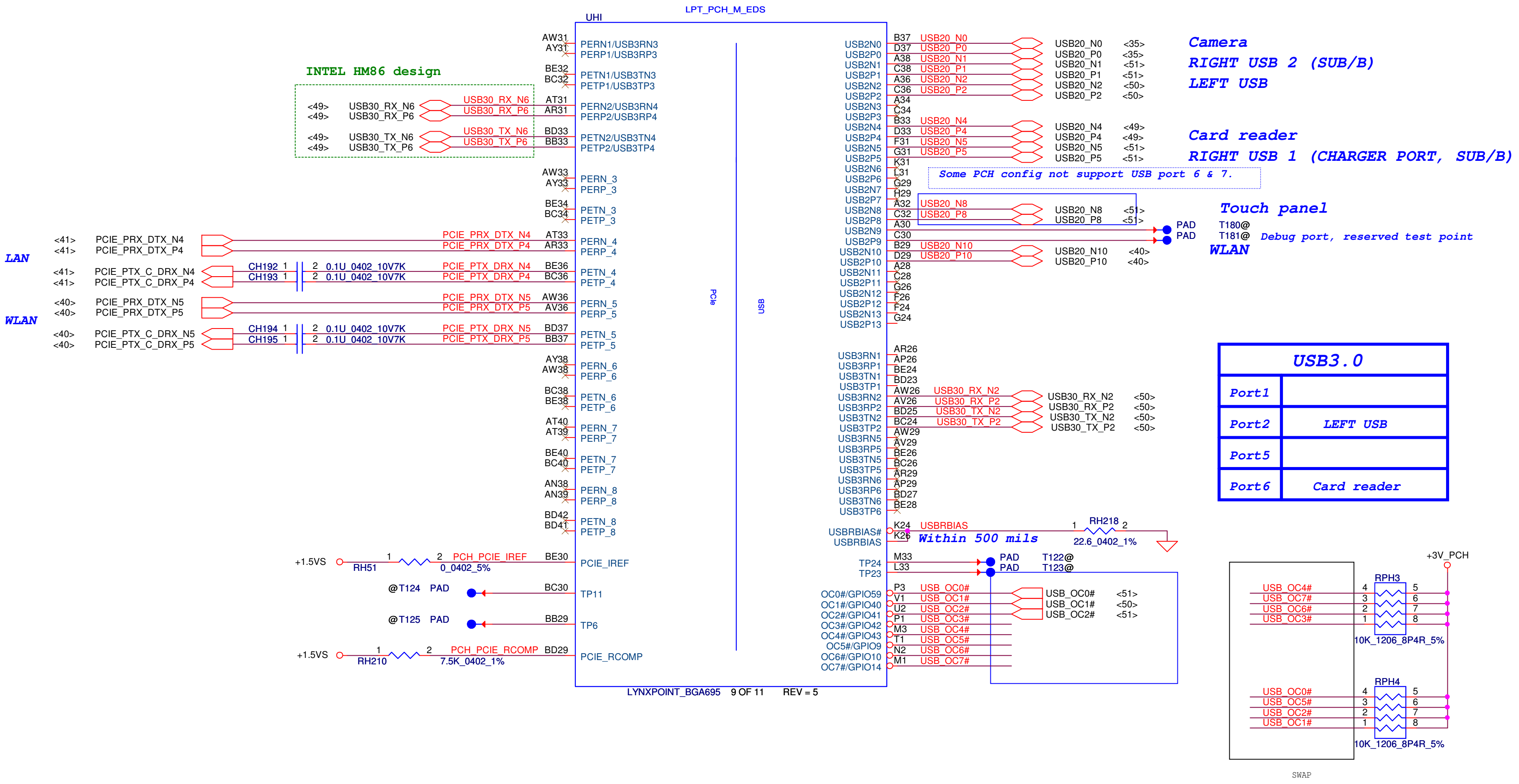
Title
PCH (5/9) LVDS, CRT,DP,HDMI

LCFC

Size Custom
Document Number **Y401 NM-A031**
Rev 1.0

Date: Wednesday, March 27, 2013 Sheet 17 of 69


LPT_PCH_M_EDS
UHI
INTEL HM86 design
<49> USB30_RX_N6 USB30_RX_N6 AT31 PERN1/USB3RN3
<49> USB30_RX_P6 USB30_RX_P6 AR31
<49> USB30_TX_N6 USB30_TX_N6 BD33
<49> USB30_TX_P6 USB30_TX_P6 BB33
AW31 PERN1/USB3RN3
AY31 PERP1/USB3RP3
BE32 PETN1/USB3TN3
BC32 PETP1/USB3TP3
PERN2/USB3RN4
PERP2/USB3RP4
PETN2/USB3TN4
PETP2/USB3TP4
AW33 PERN_3
AY33 PERP_3
BE34 PETN_3
BC34 PETP_3
LAN
<41> PCIE_PRX_DTX_N4 PCIE_PRX_DTX_N4 AT33 PERN_4
<41> PCIE_PRX_DTX_P4 PCIE_PRX_DTX_P4 AR33 PERP_4
<41> PCIE_PTX_C_DRX_N4 CH192 1 2 0.1U_0402_10V7K PCIE_PTX_DRX_N4 BE36 PETN_4
<41> PCIE_PTX_C_DRX_P4 CH193 1 2 0.1U_0402_10V7K PCIE_PTX_DRX_P4 BC36 PETP_4
WLAN
<40> PCIE_PRX_DTX_N5 PCIE_PRX_DTX_N5 AW36 PERN_5
<40> PCIE_PRX_DTX_P5 PCIE_PRX_DTX_P5 AV36 PERP_5
<40> PCIE_PTX_C_DRX_N5 CH194 1 2 0.1U_0402_10V7K PCIE_PTX_DRX_N5 BD37 PETN_5
<40> PCIE_PTX_C_DRX_P5 CH195 1 2 0.1U_0402_10V7K PCIE_PTX_DRX_P5 BB37 PETP_5
AY38 PERN_6
AW38 PERP_6
BC38 PETN_6
BE38 PETP_6
AT40 PERN_7
AT39 PERP_7
BE40 PETN_7
BC40 PETP_7
AN38 PERN_8
AN39 PERP_8
BD42 PETN_8
BD41 PETP_8
+1.5VS RH51 1 2 0_0402_5% PCH_PCIE_IREF BE30 PCIE_IREF
@T124 PAD BC30 TP11
@T125 PAD BB29 TP6
+1.5VS RH210 1 2 7.5K_0402_1% PCH_PCIE_RCOMP BD29 PCIE_RCOMP
PCIe
USB
LYNXPOINT_BGA695 9 OF 11 REV = 5
USB2N0 B37 USB20_N0 USB20_N0 <35>
USB2P0 D37 USB20_P0 USB20_P0 <35>
USB2N1 A38 USB20_N1 USB20_N1 <51>
USB2P1 C38 USB20_P1 USB20_P1 <51>
USB2N2 A36 USB20_N2 USB20_N2 <50>
USB2P2 C36 USB20_P2 USB20_P2 <50>
USB2N3 A34
USB2P3 C34
USB2N4 B33 USB20_N4 USB20_N4 <49>
USB2P4 D33 USB20_P4 USB20_P4 <49>
USB2N5 F31 USB20_N5 USB20_N5 <51>
USB2P5 G31 USB20_P5 USB20_P5 <51>
USB2N6 K31
USB2P6 L31
USB2N7 G29
USB2P7 H29
USB2N8 A32 USB20_N8 USB20_N8 <51>
USB2P8 C32 USB20_P8 USB20_P8 <51>
USB2N9 A30 PAD T180@
USB2P9 C30 PAD T181@
USB2N10 B29 USB20_N10 USB20_N10 <40>
USB2P10 D29 USB20_P10 USB20_P10 <40>
USB2N11 A28
USB2P11 C28
USB2N12 G26
USB2P12 F26
USB2N13 F24
USB2P13 G24
Camera
RIGHT USB 2 (SUB/B)
LEFT USB
Card reader
RIGHT USB 1 (CHARGER PORT, SUB/B)
Some PCH config not support USB port 6 & 7.
Touch panel
Debug port, reserved test point
WLAN
USB3RN1 AR26
USB3RP1 AP26
USB3TN1 BE24
USB3TP1 BD23
USB3RN2 AW26 USB30_RX_N2 USB30_RX_N2 <50>
USB3RP2 AV26 USB30_RX_P2 USB30_RX_P2 <50>
USB3TN2 BD25 USB30_TX_N2 USB30_TX_N2 <50>
USB3TP2 BC24 USB30_TX_P2 USB30_TX_P2 <50>
USB3RN5 AW29
USB3RP5 AV29
USB3TN5 BE26
USB3TP5 BC26
USB3RN6 AR29
USB3RP6 AP29
USB3TN6 BD27
USB3TP6 BE28
USBRBIAS# K24 USBRBIAS RH218 1 2 22.6_0402_1%
USBRBIAS K26
Within 500 mils
TP24 M33 PAD T122@
TP23 L33 PAD T123@
OC0#/GPIO59 P3 USB_OC0# USB_OC0# <51>
OC1#/GPIO40 V1 USB_OC1# USB_OC1# <50>
OC2#/GPIO41 U2 USB_OC2# USB_OC2# <51>
OC3#/GPIO42 P1 USB_OC3#
OC4#/GPIO43 M3 USB_OC4#
OC5#/GPIO9 T1 USB_OC5#
OC6#/GPIO10 N2 USB_OC6#
OC7#/GPIO14 M1 USB_OC7#
+3V_PCH
RPH3
USB_OC4# 4 5
USB_OC7# 3 6
USB_OC6# 2 7
USB_OC3# 1 8
10K_1206_8P4R_5%
RPH4
USB_OC0# 4 5
USB_OC5# 3 6
USB_OC2# 2 7
USB_OC1# 1 8
10K_1206_8P4R_5%
SWAP

USB3.0	
Port1	
Port2	LEFT USB
Port5	
Port6	Card reader

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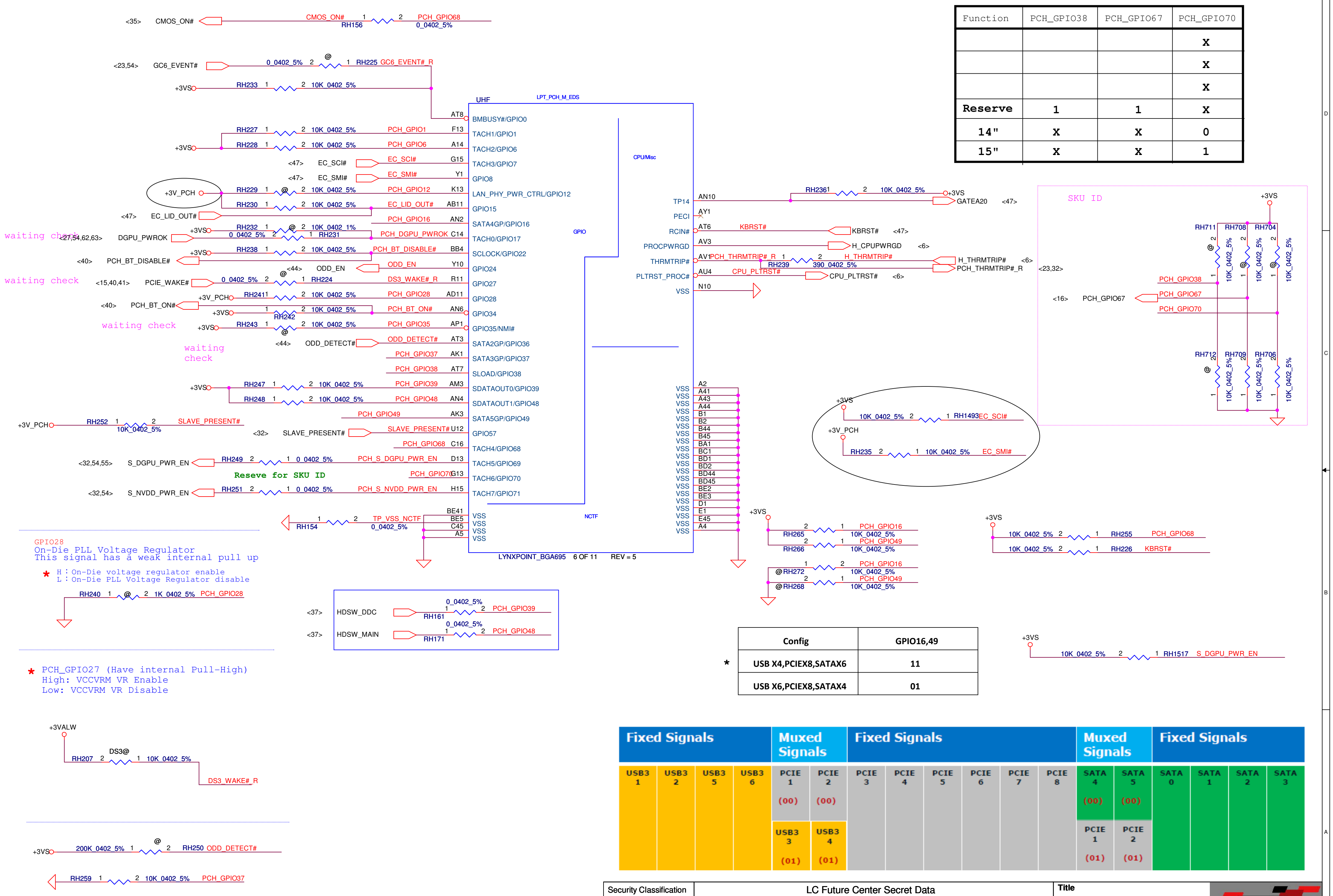
Title

PCH (5/9) PCI, USB

LCFC

Size: Custom
Document Number: Y401 NM-A031
Rev: 1.0
Date: Wednesday, March 27, 2013
Sheet 18 of 69



GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
			X
			X
			X
Reserve	1	1	X
14"	X	X	0
15"	X	X	1

Config	GPIO16,49
* USB X4,PCIEX8,SATAX6	11
USB X6,PCIEX8,SATAX4	01

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1 (00)	PCIE 2 (00)	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4 (00)	SATA 5 (00)	SATA 0	SATA 1	SATA 2	SATA 3
				USB3 3 (01)	USB3 4 (01)							PCIE 1 (01)	PCIE 2 (01)				

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Title
PCH (6/9) GPIO, CPU, MISC
LCFC
Size Custom
Document Number Y401 NM-A031
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Date: Wednesday, March 27, 2013
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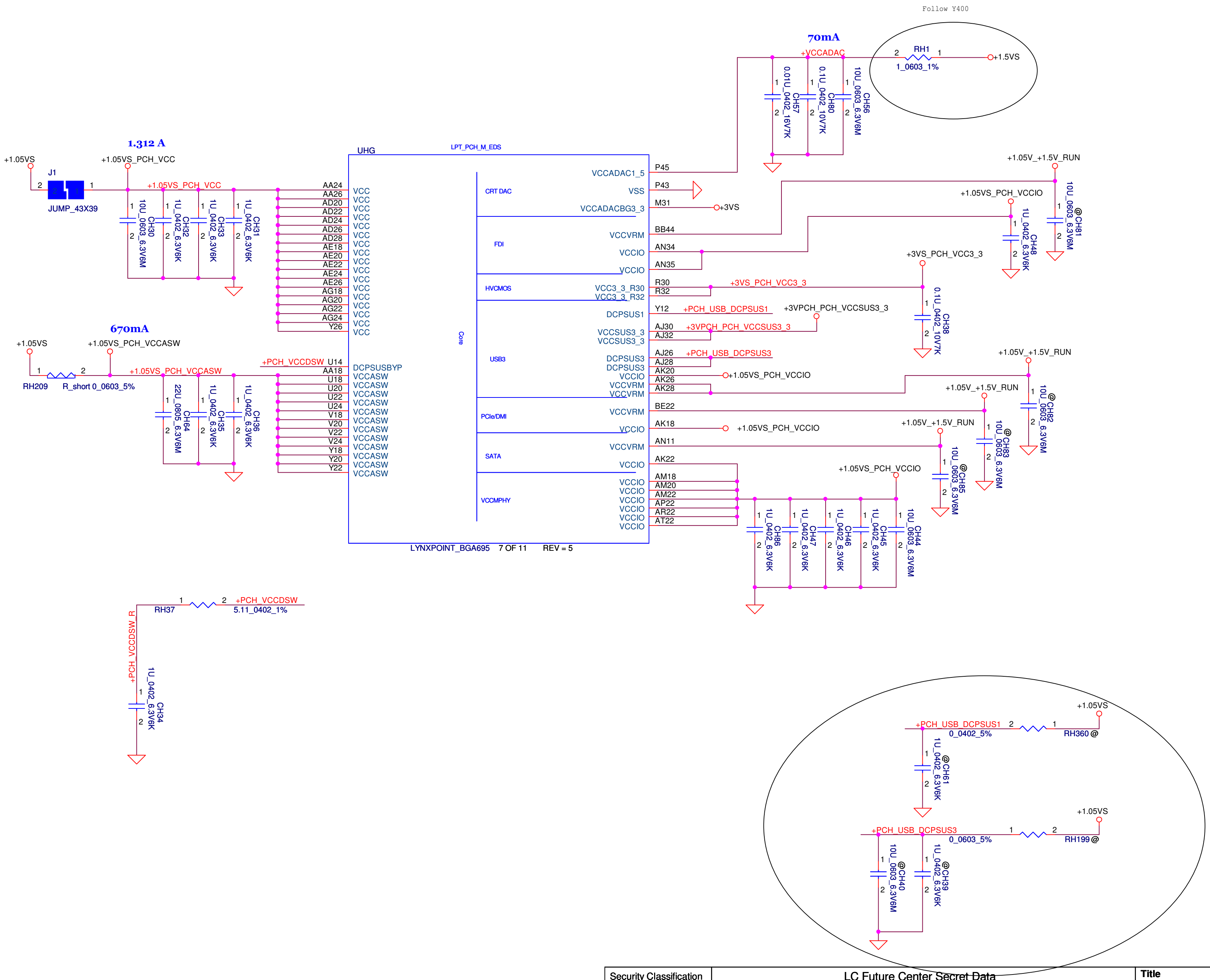

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Title
PCH (7/9) PWR

LCFC

Size: Custom
Document Number: Y401 NM-A031
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Date: Wednesday, March 27, 2013
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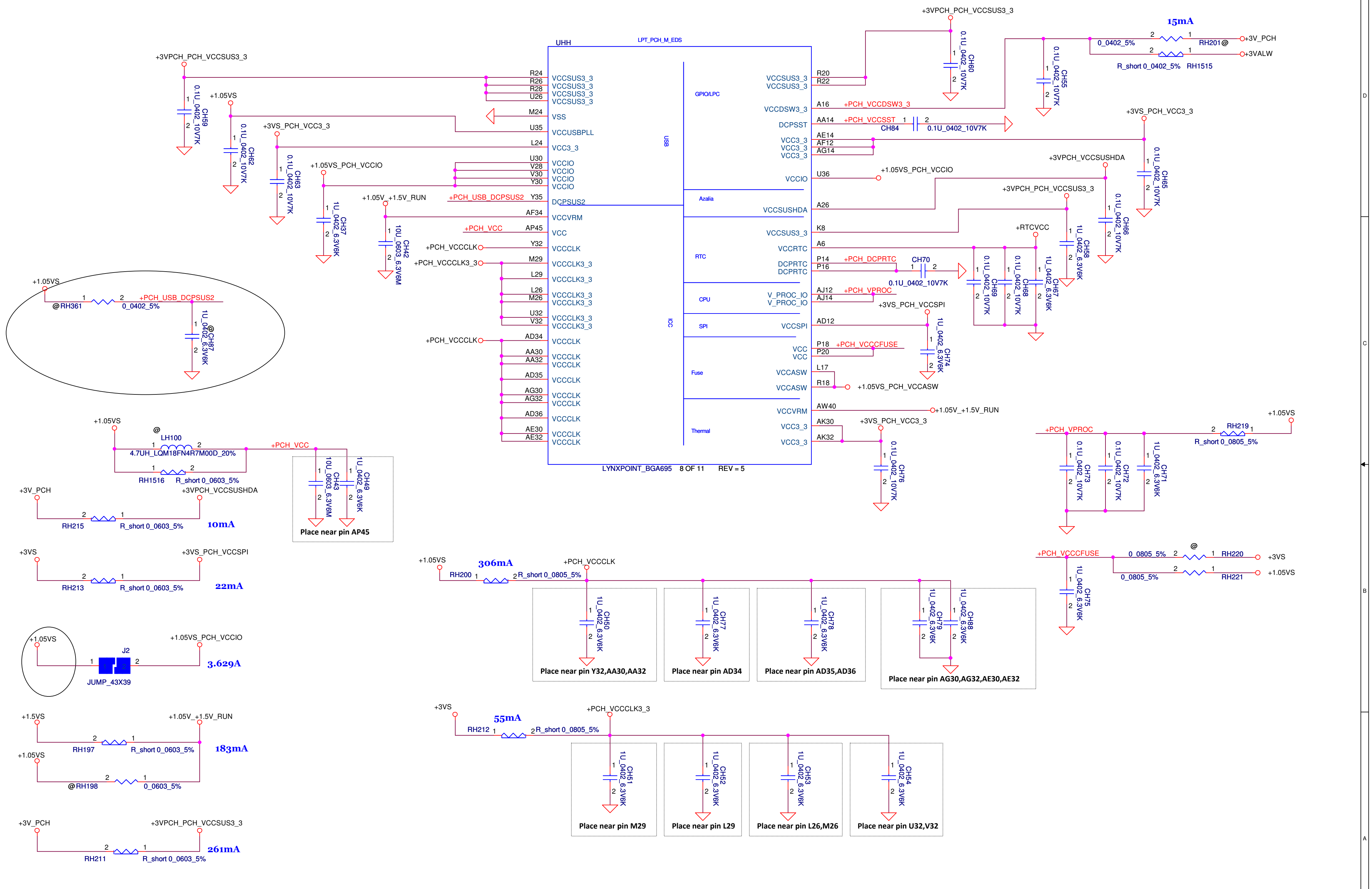

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Title
PCH (8/9) PWR

LCFC

Size Custom
Document Number Y401 NM-A031
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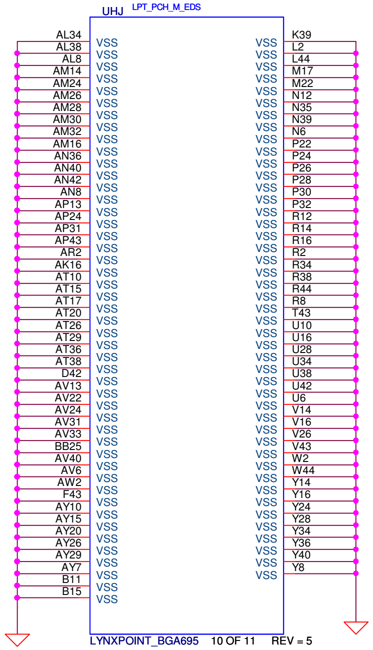

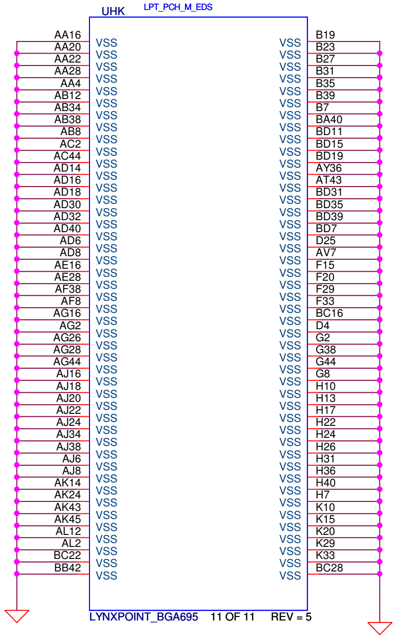

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Title
PCH (9/9) VSS

LCFC

Size: Custom
Document Number: Y401 NM-A031
Rev: 1.0
Date: Wednesday, March 27, 2013
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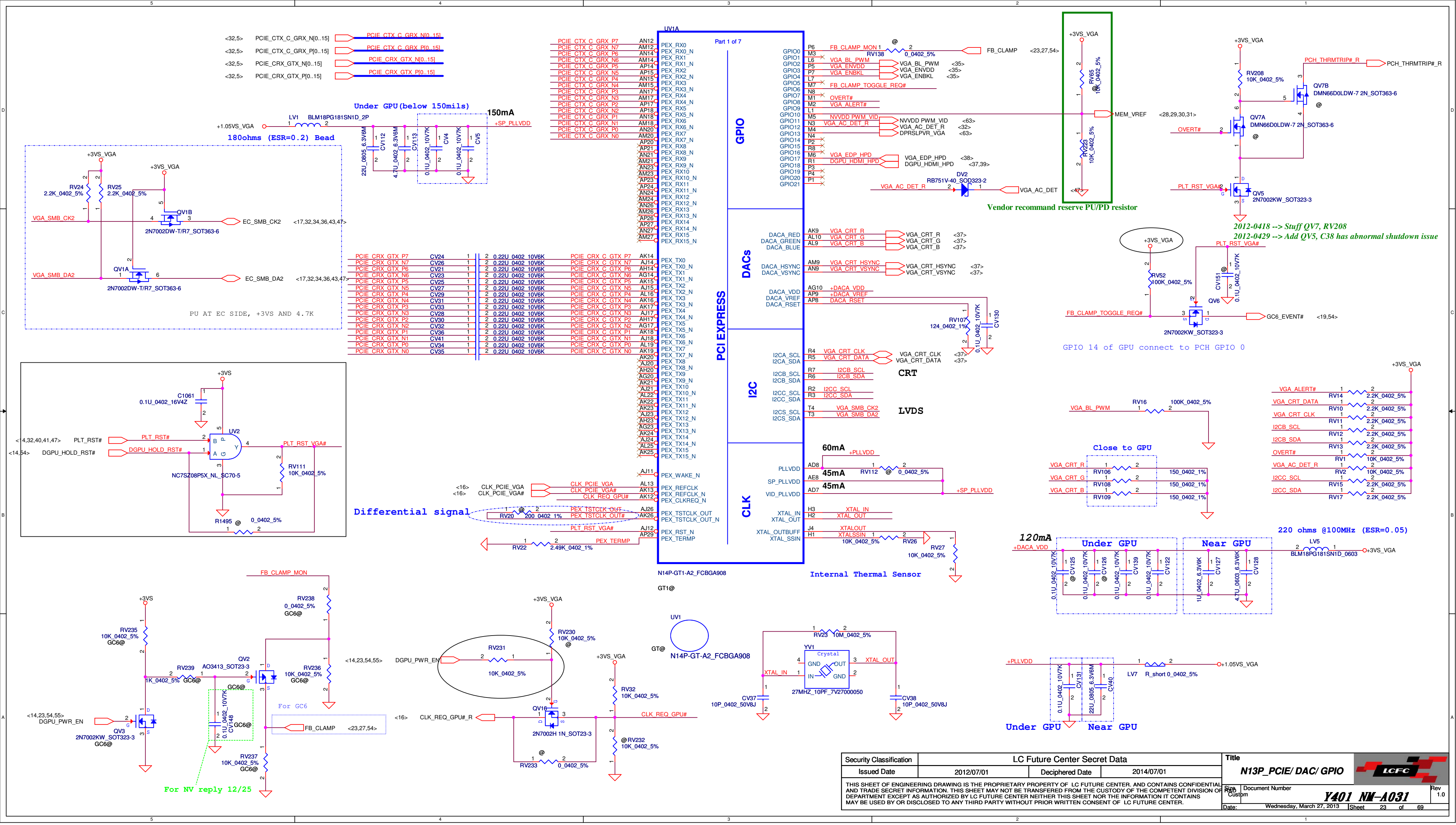

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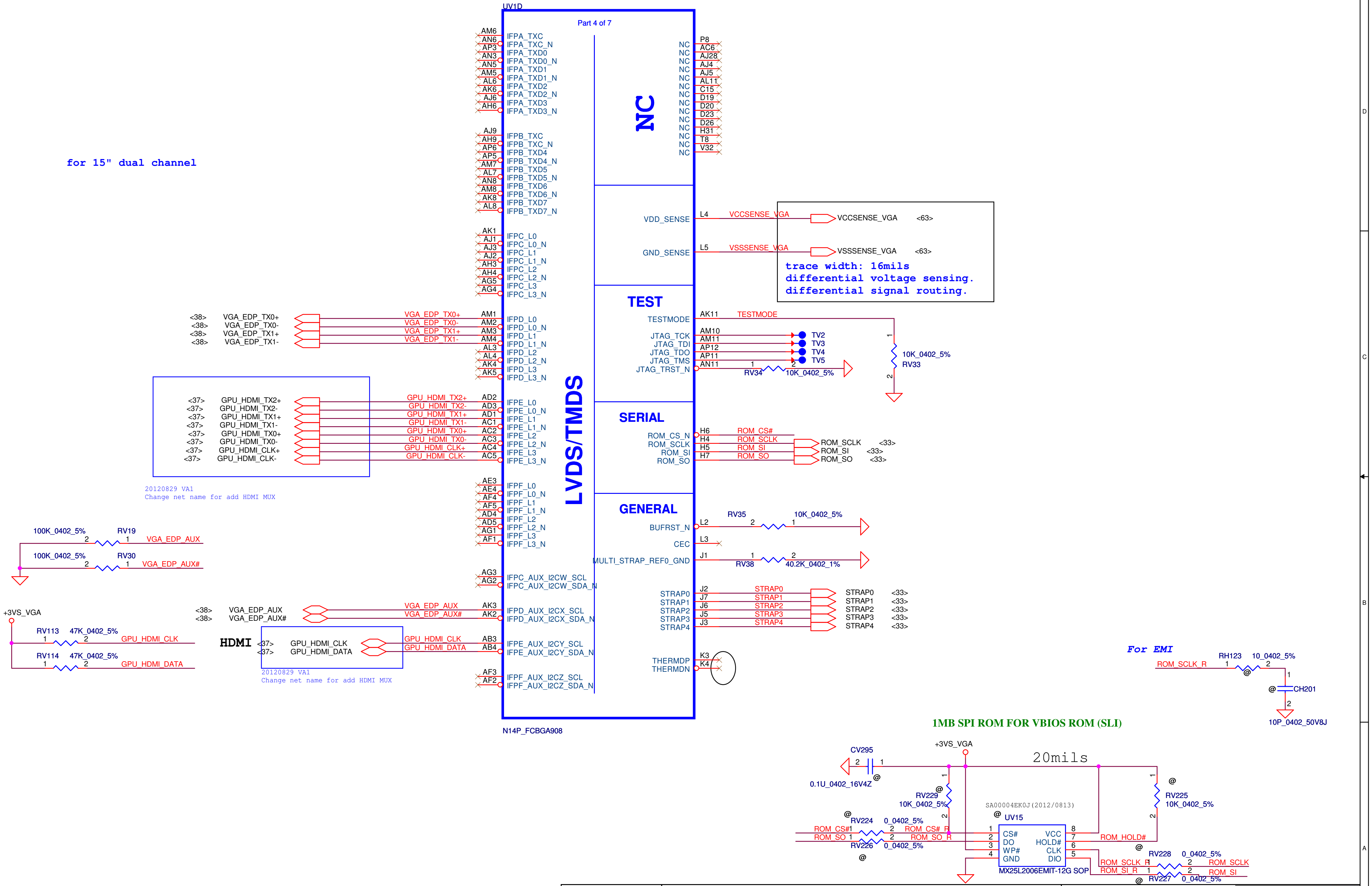
Title
N13P_PCIE/ DAC/ GPIO

Size Custom
Document Number Y401 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013
Sheet 23 of 69



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Title
N13P_LVDS/ HDMI/ THERM

LCFC

Size Custom
Document Number Y401 NM-A031
Rev 1.0

Date: Wednesday, March 27, 2013
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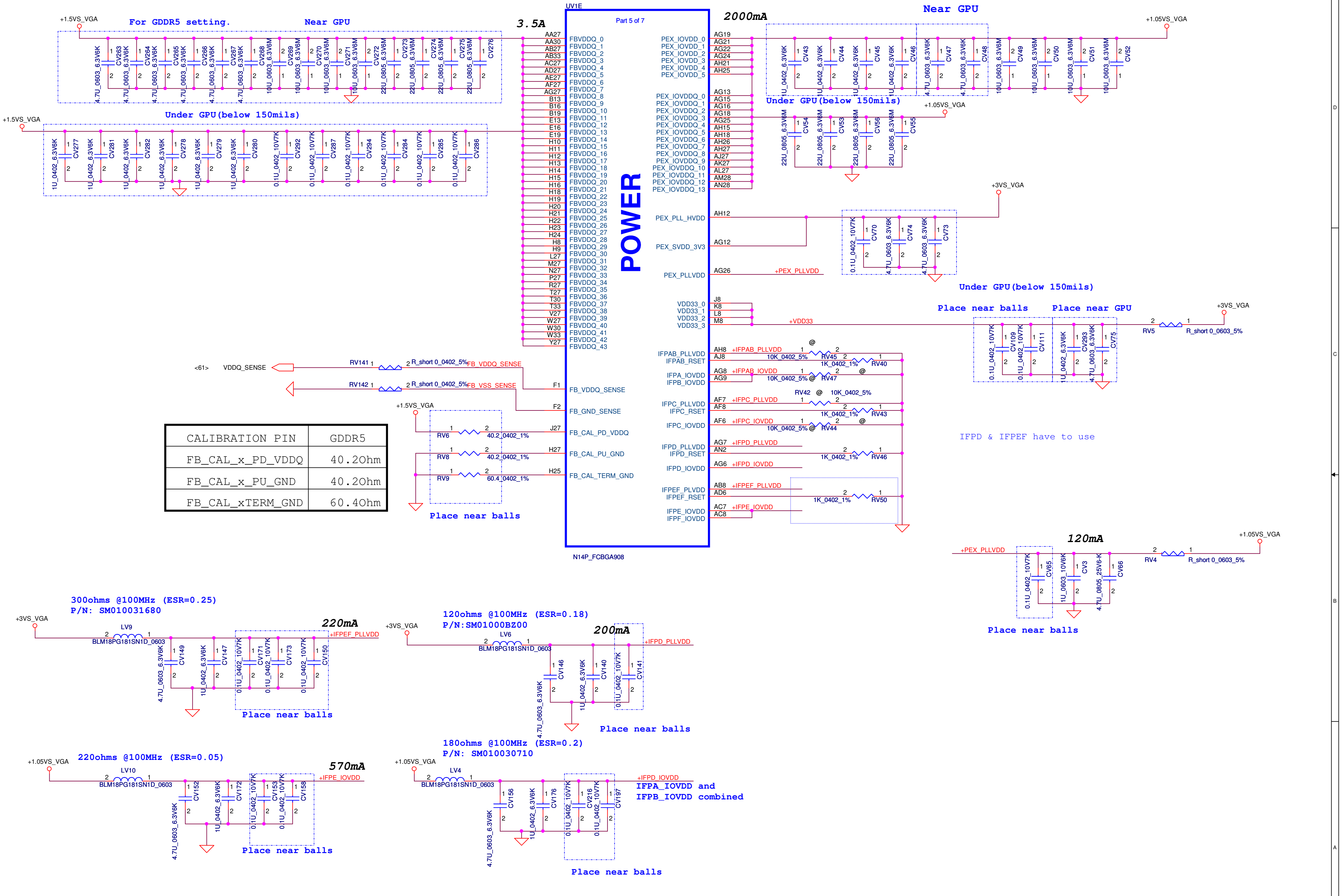

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_Power
Size Custom
Document Number Y401 NM-A031
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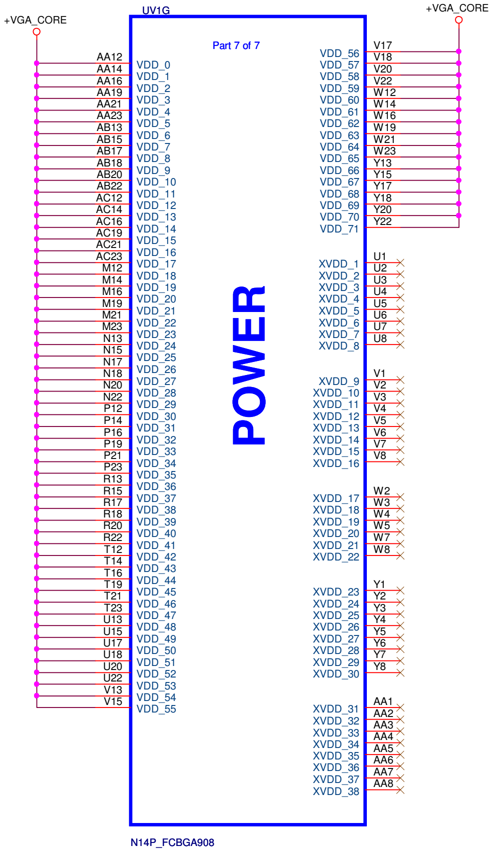

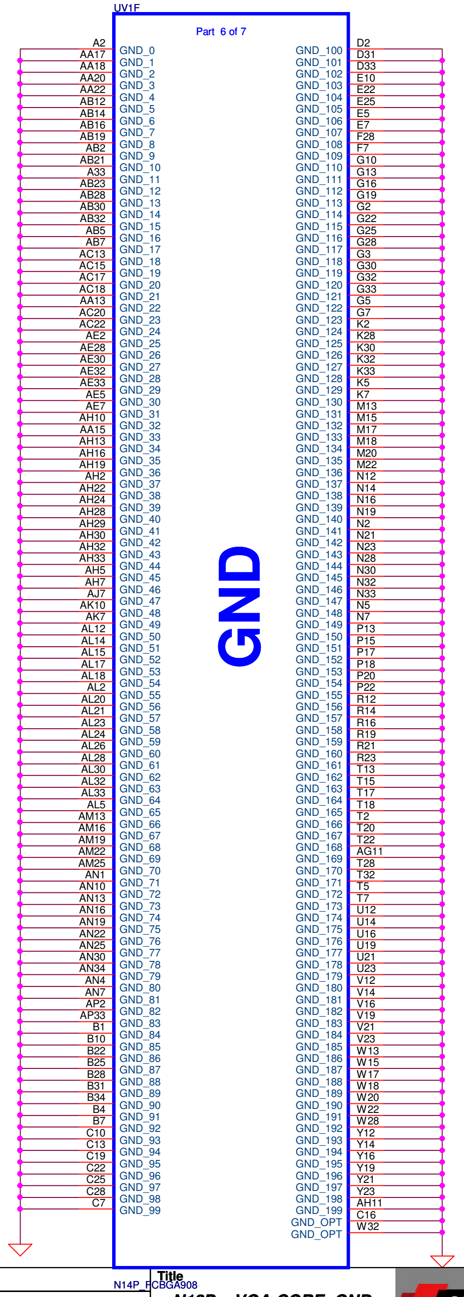

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Title
N13P_+VGA CORE, GND

Size: Custom
Document Number: Y401 NM-A031
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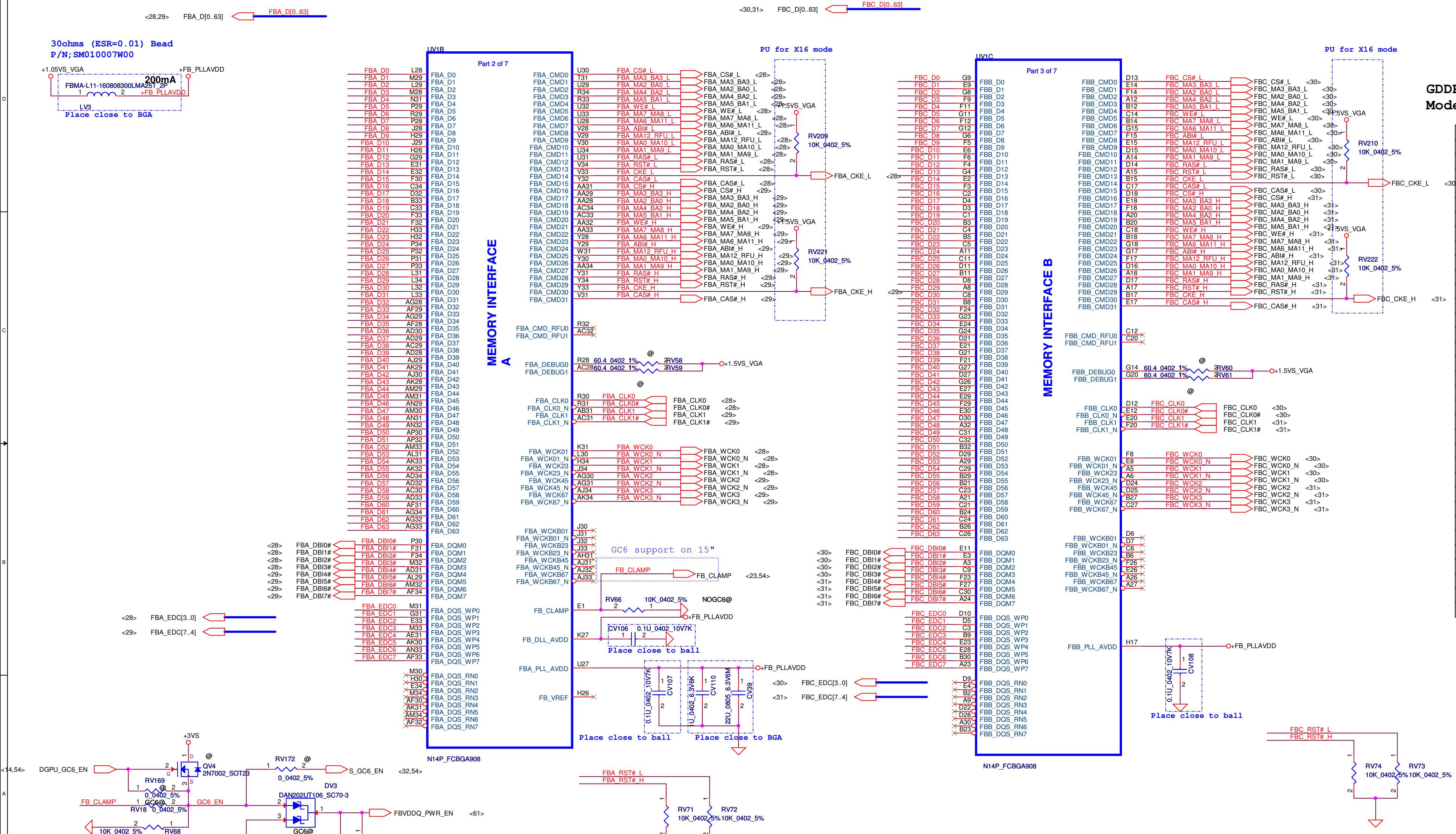


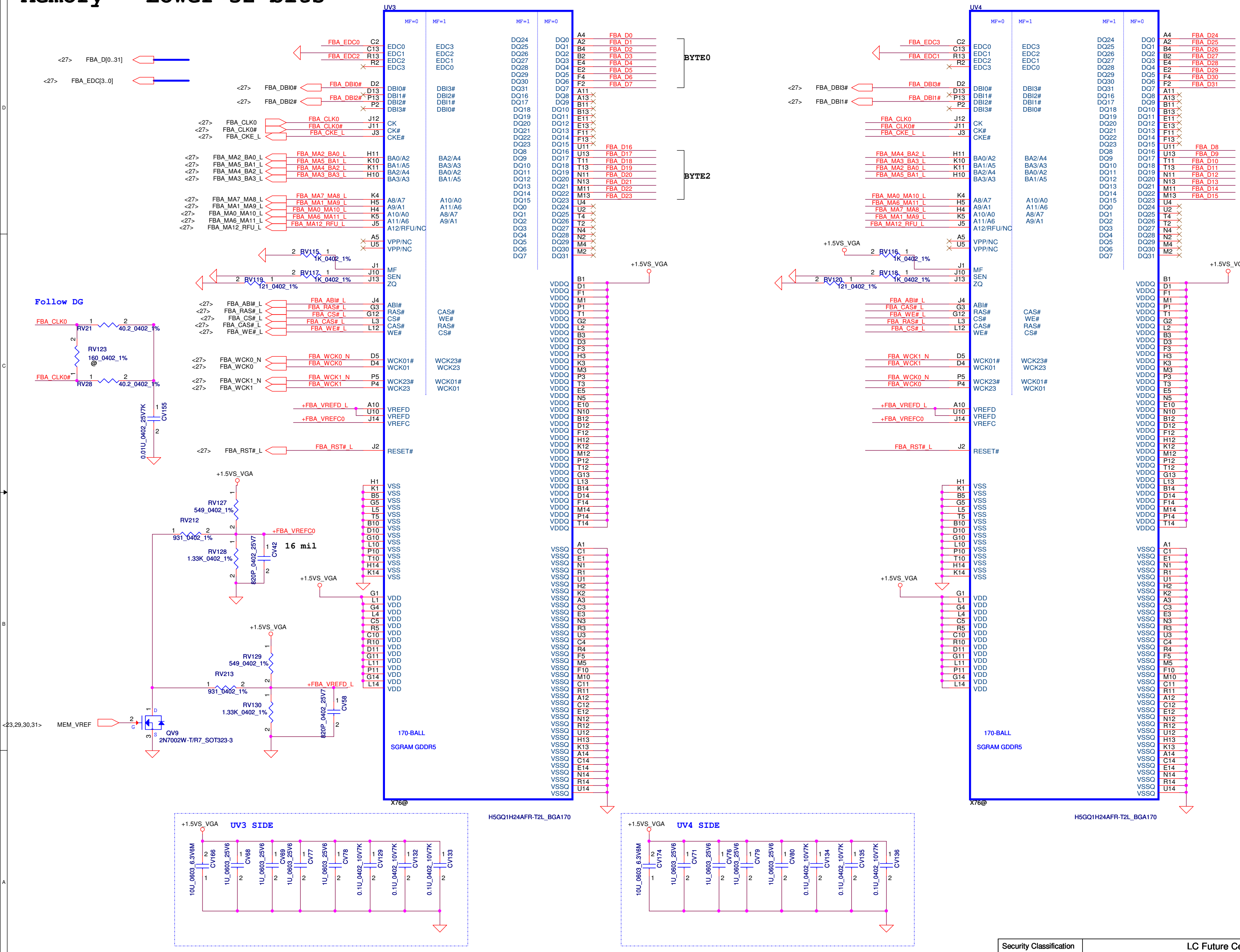
GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_MEM Interface
LCFC
Size Custom
Document Number Y401 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013
Sheet 27 of 69

Memory - Lower 32 bits



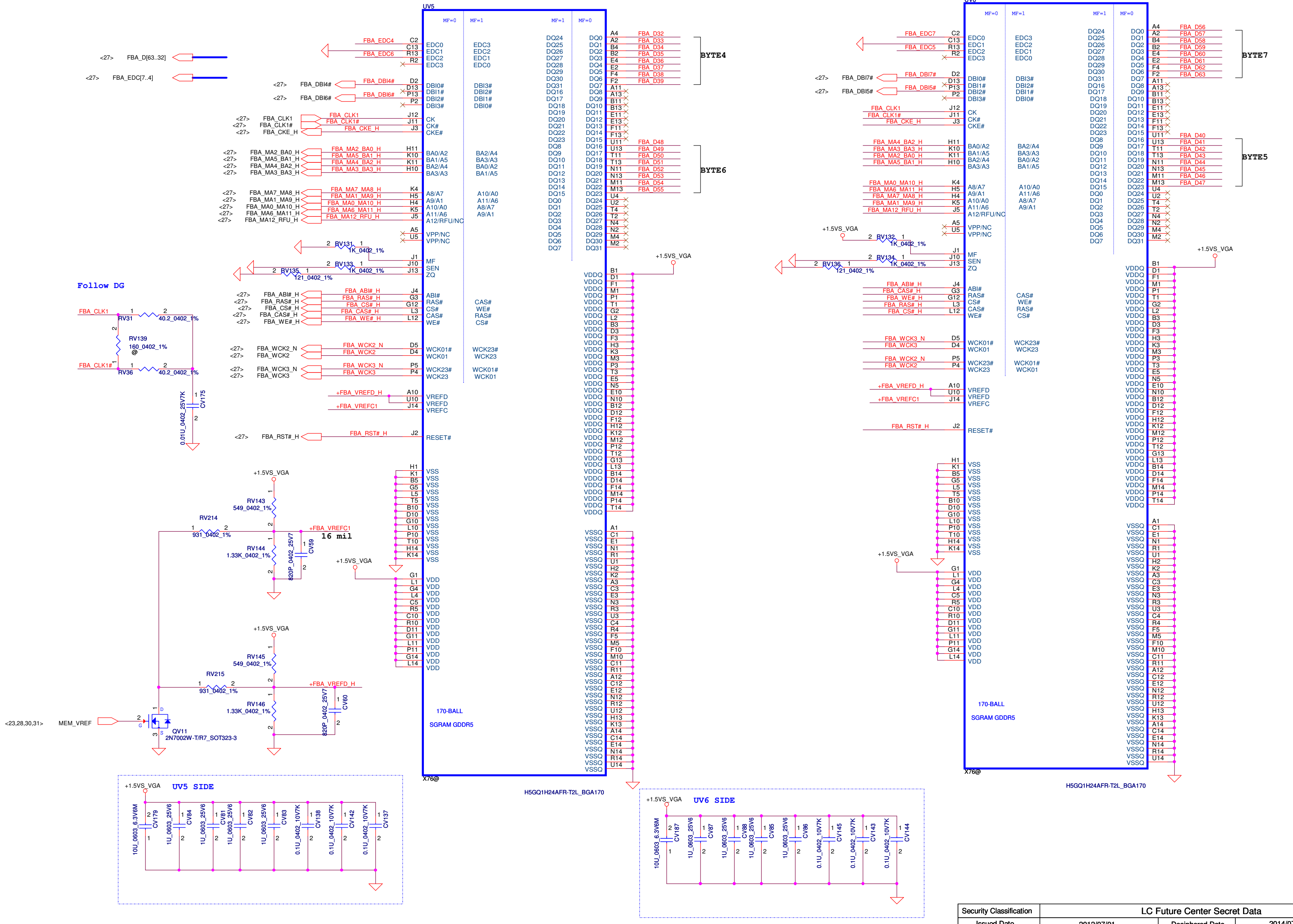
GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_GDDR5_A Lower
Size Custom
Document Number Y401 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013

Memory - Upper 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

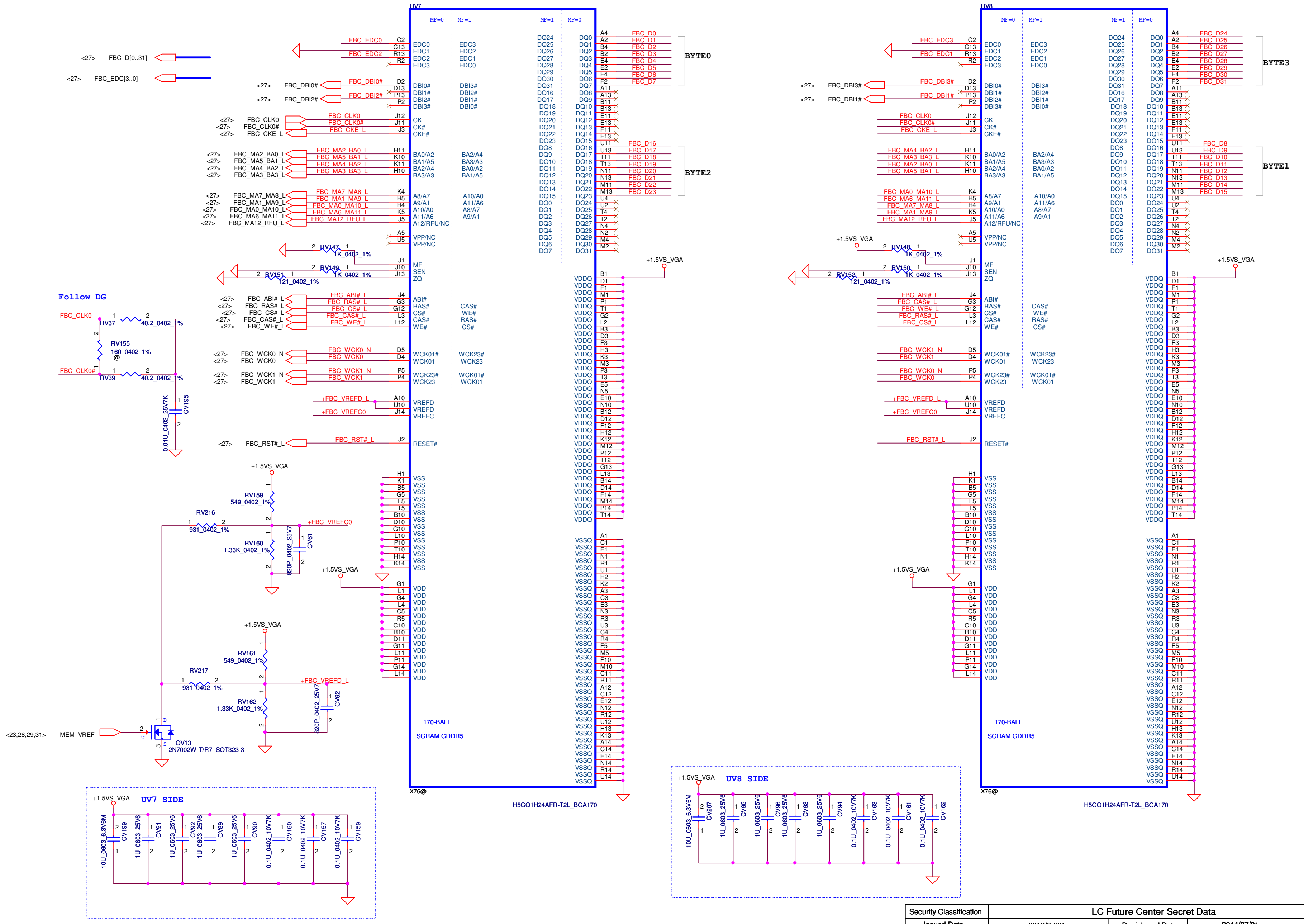
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_GDDR5_A Upper

Size Custom
Document Number Y401 NM-A031
Rev 1.0

Date: Wednesday, March 27, 2013

Memory Partition C - Lower 32 bits



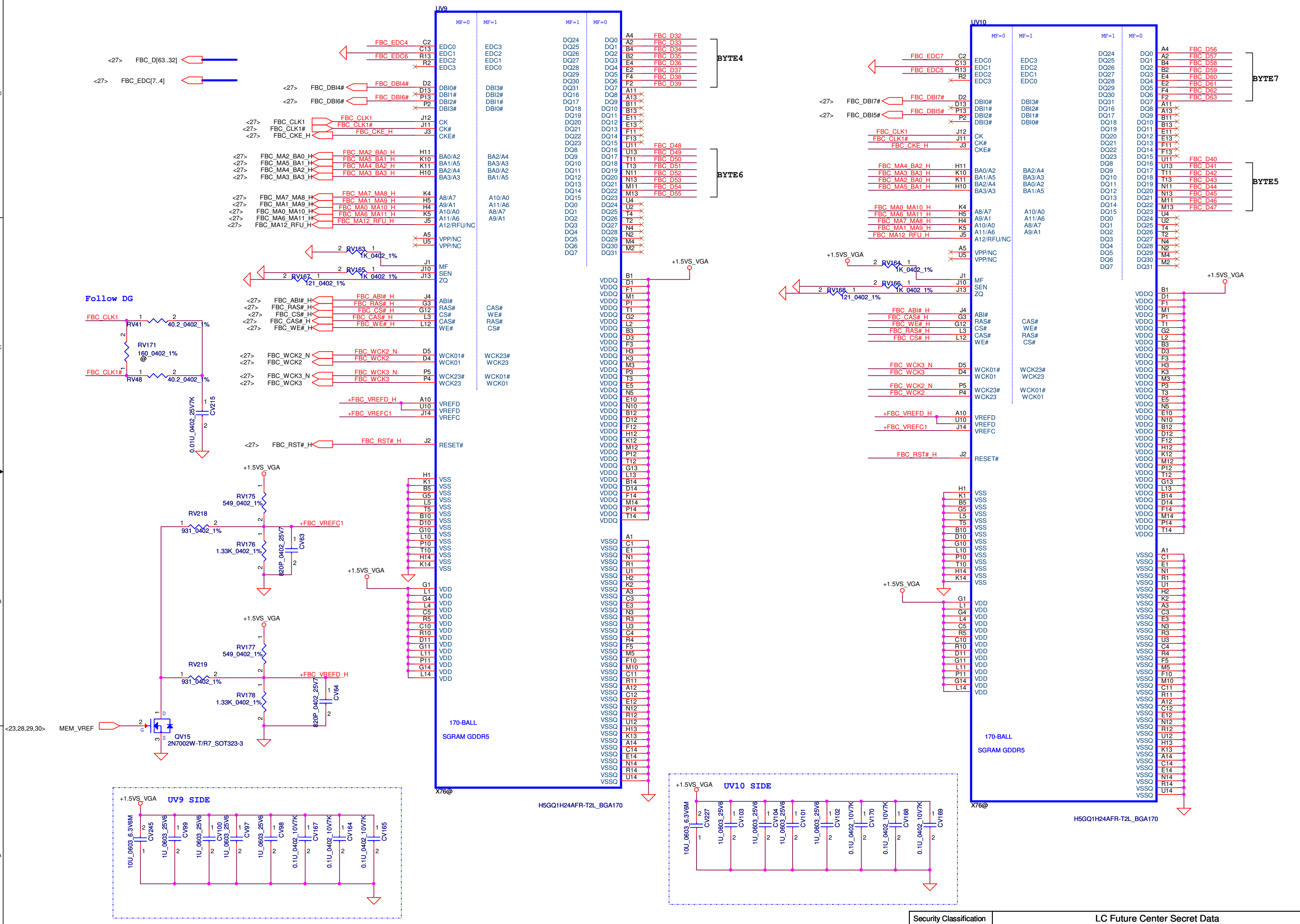
GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_GDDR5_C Lower
Size: Custom
Document Number: Y401 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013

Memory Partition C - Upper 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
N13P_GDDR5_C Upper

LCFC

Size: Custom
Document Number: Y401 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013
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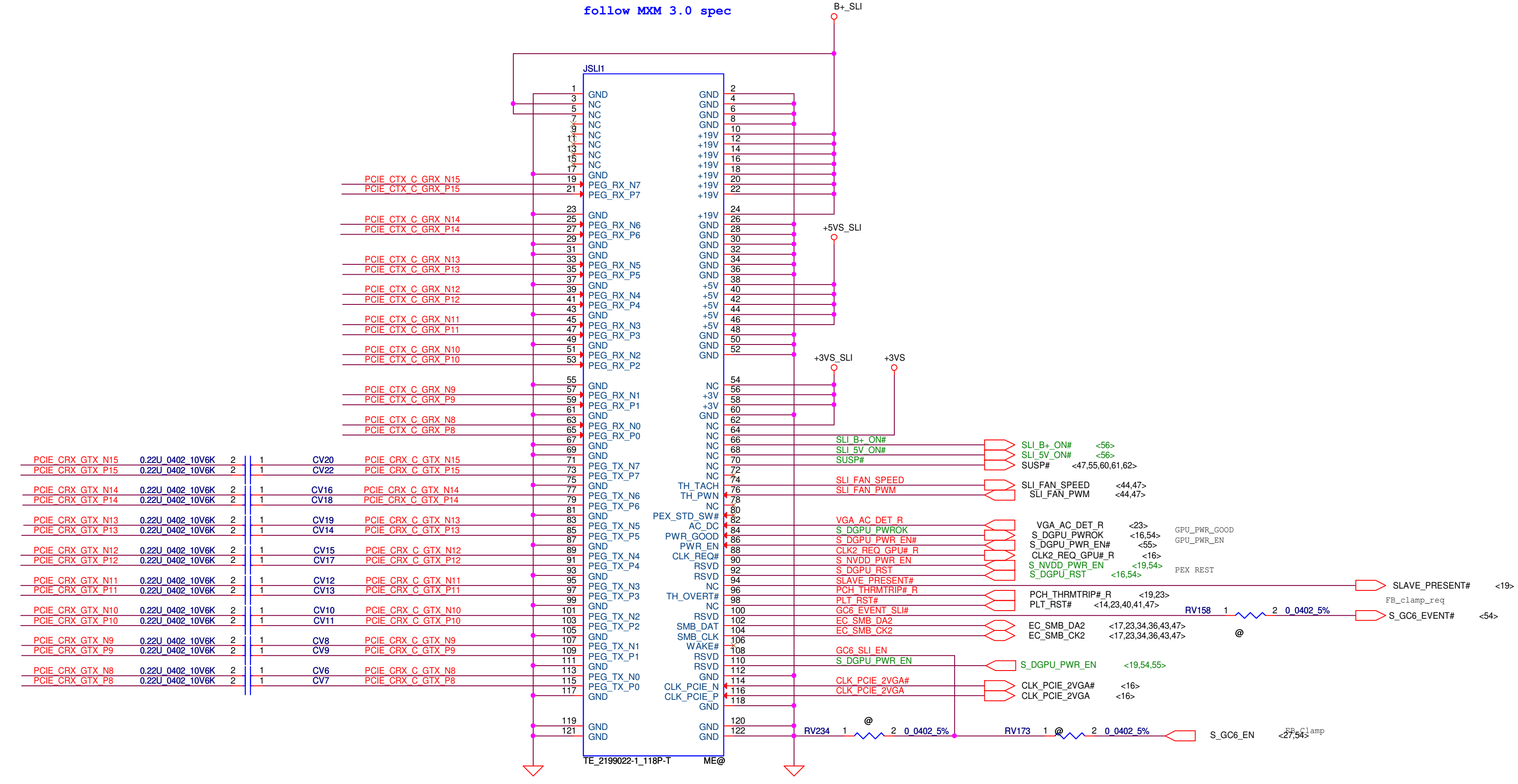
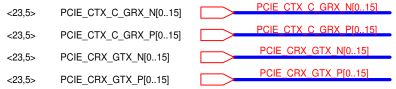
follow MXM 3.0 spec


B+_SLI
+5VS_SLI
+3VS_SLI
+3VS
JSLI1
GND
NC
PEG_RX_N7
PEG_RX_P7
PEG_RX_N6
PEG_RX_P6
PEG_RX_N5
PEG_RX_P5
PEG_RX_N4
PEG_RX_P4
PEG_RX_N3
PEG_RX_P3
PEG_RX_N2
PEG_RX_P2
PEG_RX_N1
PEG_RX_P1
PEG_RX_N0
PEG_RX_P0
PEG_TX_N7
PEG_TX_P7
PEG_TX_N6
PEG_TX_P6
PEG_TX_N5
PEG_TX_P5
PEG_TX_N4
PEG_TX_P4
PEG_TX_N3
PEG_TX_P3
PEG_TX_N2
PEG_TX_P2
PEG_TX_N1
PEG_TX_P1
PEG_TX_N0
PEG_TX_P0
+19V
+5V
+3V
TH_TACH
TH_PWN
PEX_STD_SW#
AC_DC
PWR_GOOD
PWR_EN
CLK_REQ#
RSVD
TH_OVERT#
SMB_DAT
SMB_CLK
WAKE#
CLK_PCIE_N
CLK_PCIE_P
TE_2199022-1_118P-T
ME@
PCIE_CTX_C_GRX_N15
PCIE_CTX_C_GRX_P15
PCIE_CTX_C_GRX_N14
PCIE_CTX_C_GRX_P14
PCIE_CTX_C_GRX_N13
PCIE_CTX_C_GRX_P13
PCIE_CTX_C_GRX_N12
PCIE_CTX_C_GRX_P12
PCIE_CTX_C_GRX_N11
PCIE_CTX_C_GRX_P11
PCIE_CTX_C_GRX_N10
PCIE_CTX_C_GRX_P10
PCIE_CTX_C_GRX_N9
PCIE_CTX_C_GRX_P9
PCIE_CTX_C_GRX_N8
PCIE_CTX_C_GRX_P8
PCIE_CRX_GTX_N15 0.22U_0402_10V6K CV20 PCIE_CRX_C_GTX_N15
PCIE_CRX_GTX_P15 0.22U_0402_10V6K CV22 PCIE_CRX_C_GTX_P15
PCIE_CRX_GTX_N14 0.22U_0402_10V6K CV16 PCIE_CRX_C_GTX_N14
PCIE_CRX_GTX_P14 0.22U_0402_10V6K CV18 PCIE_CRX_C_GTX_P14
PCIE_CRX_GTX_N13 0.22U_0402_10V6K CV19 PCIE_CRX_C_GTX_N13
PCIE_CRX_GTX_P13 0.22U_0402_10V6K CV14 PCIE_CRX_C_GTX_P13
PCIE_CRX_GTX_N12 0.22U_0402_10V6K CV15 PCIE_CRX_C_GTX_N12
PCIE_CRX_GTX_P12 0.22U_0402_10V6K CV17 PCIE_CRX_C_GTX_P12
PCIE_CRX_GTX_N11 0.22U_0402_10V6K CV12 PCIE_CRX_C_GTX_N11
PCIE_CRX_GTX_P11 0.22U_0402_10V6K CV13 PCIE_CRX_C_GTX_P11
PCIE_CRX_GTX_N10 0.22U_0402_10V6K CV10 PCIE_CRX_C_GTX_N10
PCIE_CRX_GTX_P10 0.22U_0402_10V6K CV11 PCIE_CRX_C_GTX_P10
PCIE_CRX_GTX_N9 0.22U_0402_10V6K CV8 PCIE_CRX_C_GTX_N9
PCIE_CRX_GTX_P9 0.22U_0402_10V6K CV9 PCIE_CRX_C_GTX_P9
PCIE_CRX_GTX_N8 0.22U_0402_10V6K CV6 PCIE_CRX_C_GTX_N8
PCIE_CRX_GTX_P8 0.22U_0402_10V6K CV7 PCIE_CRX_C_GTX_P8
SLI_B+_ON# SLI_B+_ON# <56>
SLI_5V_ON# SLI_5V_ON# <56>
SUSP# SUSP# <47,55,60,61,62>
SLI_FAN_SPEED SLI_FAN_SPEED <44,47>
SLI_FAN_PWM SLI_FAN_PWM <44,47>
VGA_AC_DET_R VGA_AC_DET_R <23>
S_DGPU_PWROK S_DGPU_PWROK <16,54>
S_DGPU_PWR_EN# S_DGPU_PWR_EN# <55>
CLK2_REQ_GPU#_R CLK2_REQ_GPU#_R <16>
S_NVDD_PWR_EN S_NVDD_PWR_EN <19,54>
S_DGPU_RST S_DGPU_RST <16,54>
GPU_PWR_GOOD
GPU_PWR_EN
PEX REST
SLAVE_PRESENT# SLAVE_PRESENT# <19>
PCH_THRMTRIP#_R PCH_THRMTRIP#_R <19,23>
PLT_RST# PLT_RST# <14,23,40,41,47>
GC6_EVENT_SLI#
RV158 1 2 0_0402_5%
@
FB_clamp_req
S_GC6_EVENT# <54>
EC_SMB_DA2 EC_SMB_DA2 <17,23,34,36,43,47>
EC_SMB_CK2 EC_SMB_CK2 <17,23,34,36,43,47>
GC6_SLI_EN
S_DGPU_PWR_EN S_DGPU_PWR_EN <19,54,55>
CLK_PCIE_2VGA# CLK_PCIE_2VGA# <16>
CLK_PCIE_2VGA CLK_PCIE_2VGA <16>
RV234 1 @ 2 0_0402_5%
RV173 1 @ 2 0_0402_5%
S_GC6_EN <27,54>
FB_Clamp

11/11 for 2nd VGA fan
need to notic EC


<23,5> PCIE_CTX_C_GRX_N[0..15] PCIE_CTX_C_GRX_N[0..15]
<23,5> PCIE_CTX_C_GRX_P[0..15] PCIE_CTX_C_GRX_P[0..15]
<23,5> PCIE_CRX_GTX_N[0..15] PCIE_CRX_GTX_N[0..15]
<23,5> PCIE_CRX_GTX_P[0..15] PCIE_CRX_GTX_P[0..15]

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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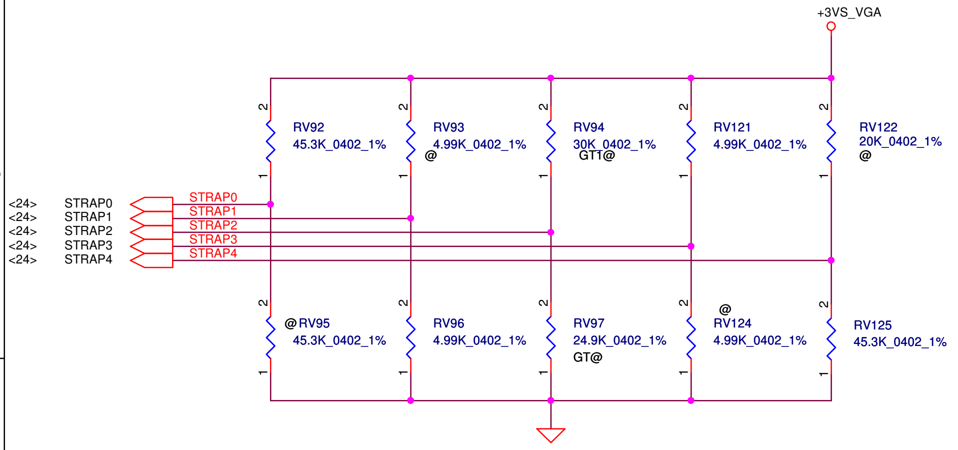
Title
VGA MXM

LCFC

Size: Custom
Document Number: **Y401 NM-A031**
Rev: 1.0
Date: Wednesday, March 27, 2013
Sheet 32 of 69

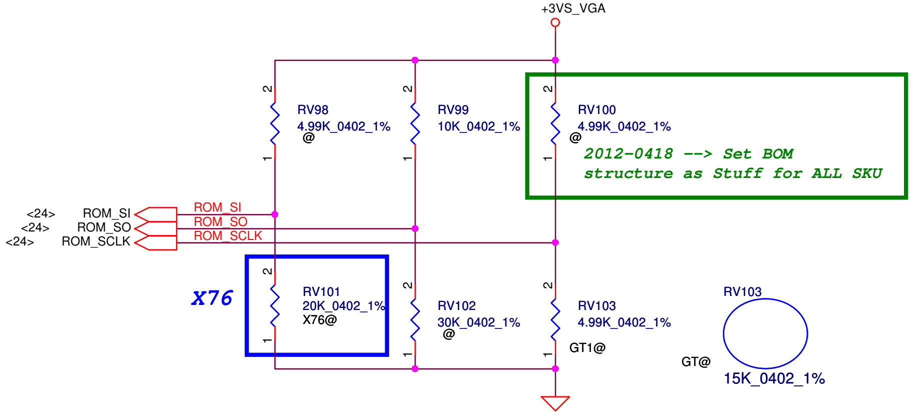


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present



3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0000	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

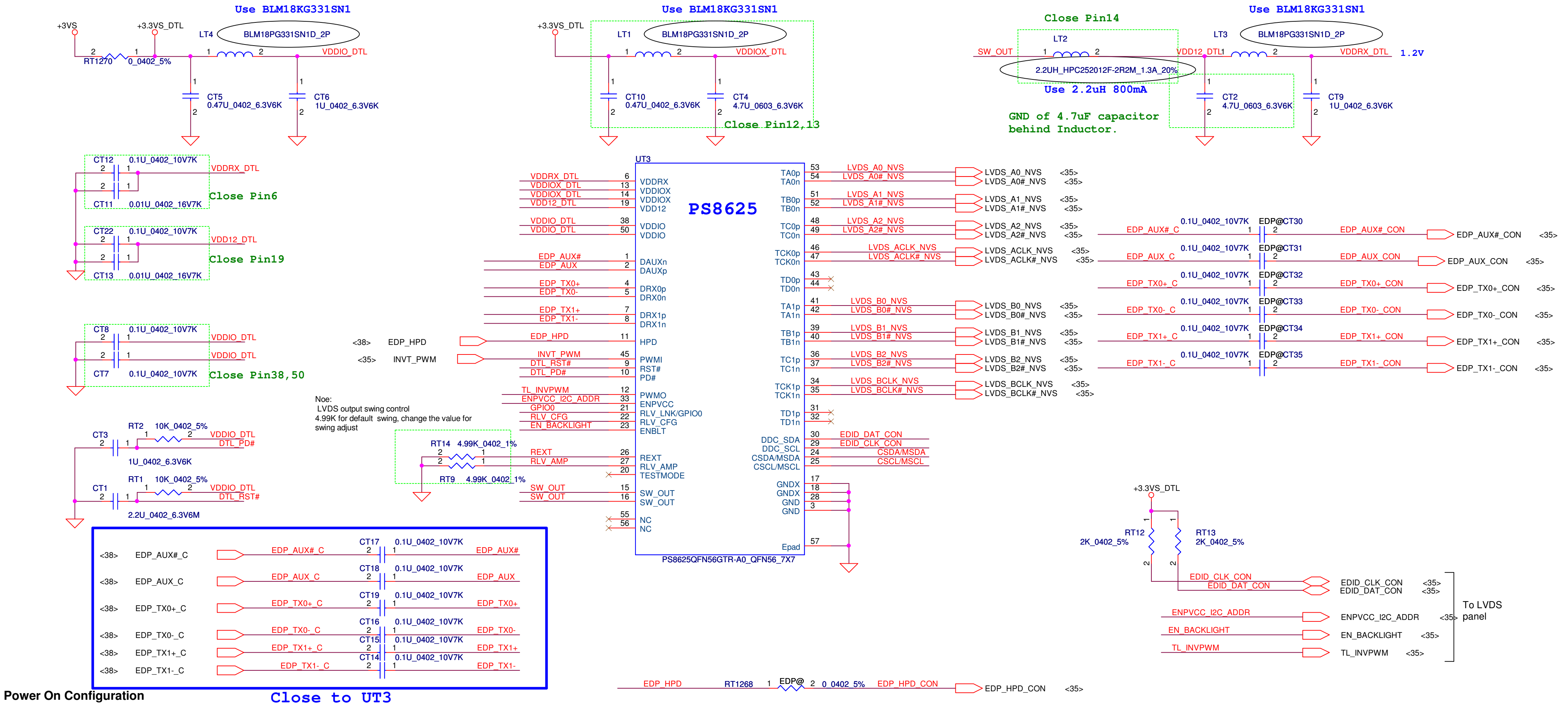
X76

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GT1 28nm	Samsung	K4G20325FD-FC04 2G 64Mx32	PD 30K	PU 10K	PD15K (ALL SKU)	PU 45K	PD 5K	PD 25K	PU 5K	PD 45K
		K4G20325FD-FC03 2G 64Mx32	PD 30K							
	Hynix									
		H5GQ2H24AFR-R0C 2G 64Mx32	PD 25K							
		H5GQ2H24AFR-T2C 2G 64Mx32	PD 25K							

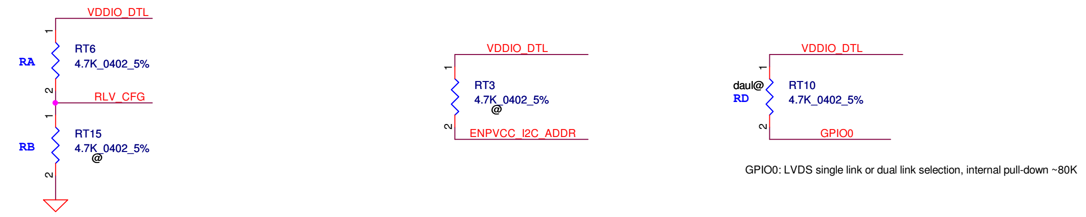
VRAM	*X76*	*VRAM P/N*
Samsung	X7600412001 (2G 64Mx32)	SA00005B71J
Hynix	X7600412002 (2G 64Mx32)	SA00004GD2J

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_MISC
LCFC
Size Custom
Document Number
Y401 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013
Sheet 33 of 69



Power On Configuration



GPIO0: LVDS single link or dual link selection, internal pull-down ~80K

Default	RLV_CFG	RA	RB
*	H:6-bit both VESA and JEIDA mapping	Stuff	NA
	M:8-bit JEIDA mapping	NA	Stuff
	L:8-bit VESA mapping	NA	NA

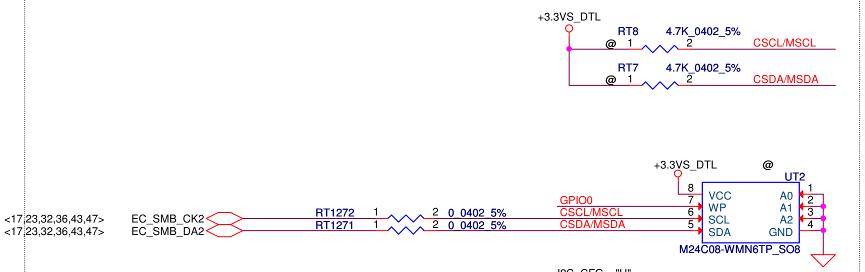
RLV_CFG: LVDS color depth and data mapping selection, internal pull-down ~80K

Default	ENPVCC_I2C_ADDR	RC	RD
	H:0x90h~0x9Fh	Stuff	NA
*	L:0x10h~0x1Fh	NA	NA

I2C_ADDR: I2C Slave address selection, internal pull-down ~80K

Default	GPIO0	RD
*	Single channel	NA
	Daul channel	Stuff

Initial Code EEPROM

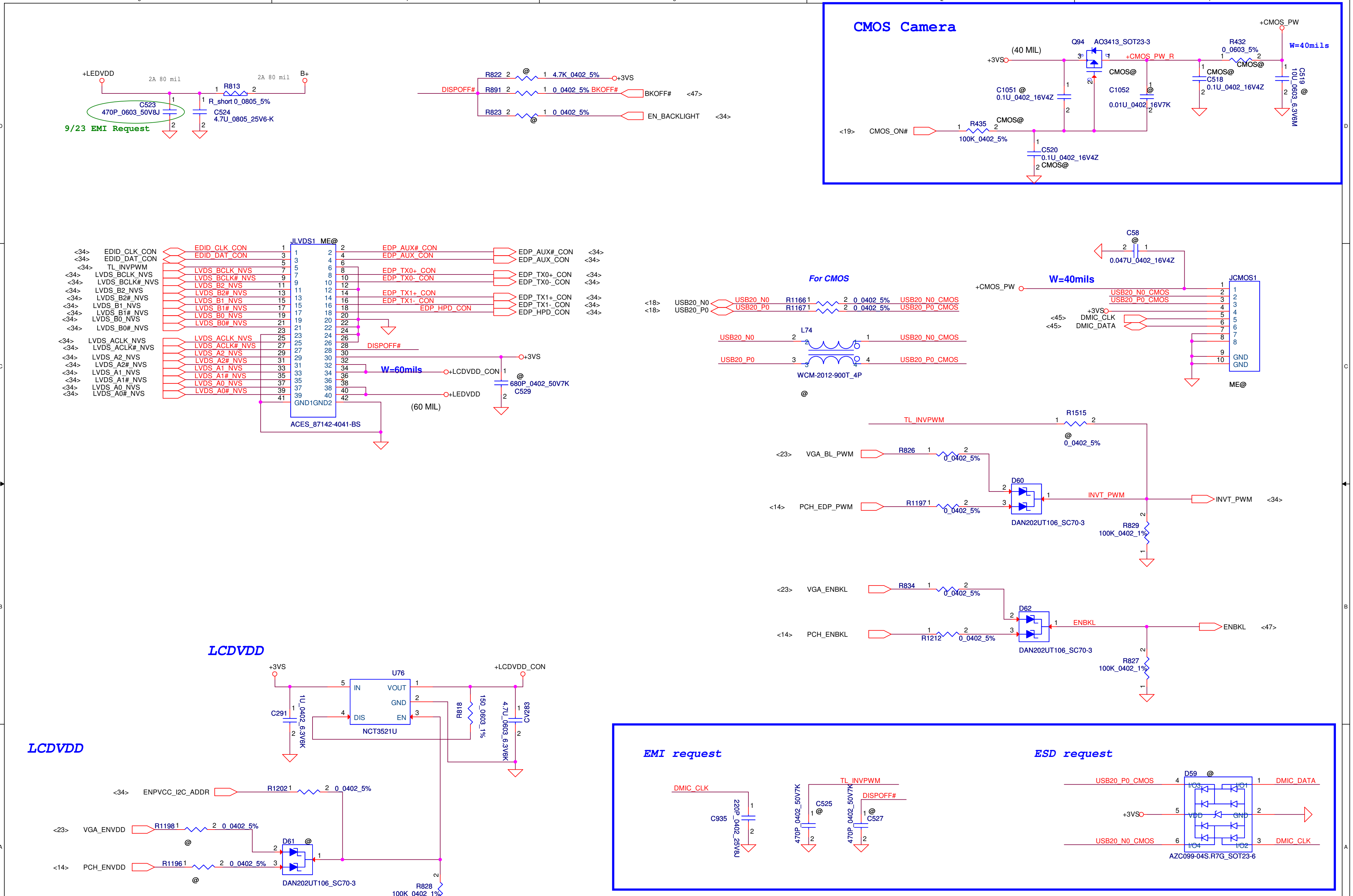


I2C_CFG = "H"
EEPROM for Initial Code
I2C Address: 0xA0
Suggest minimum 8Kbit

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
LVDS/ CMOS/ USB-ReDriver

Size: Custom
Document Number: Y501 NM-A032
Rev: 1.0
Date: Wednesday, March 27, 2013



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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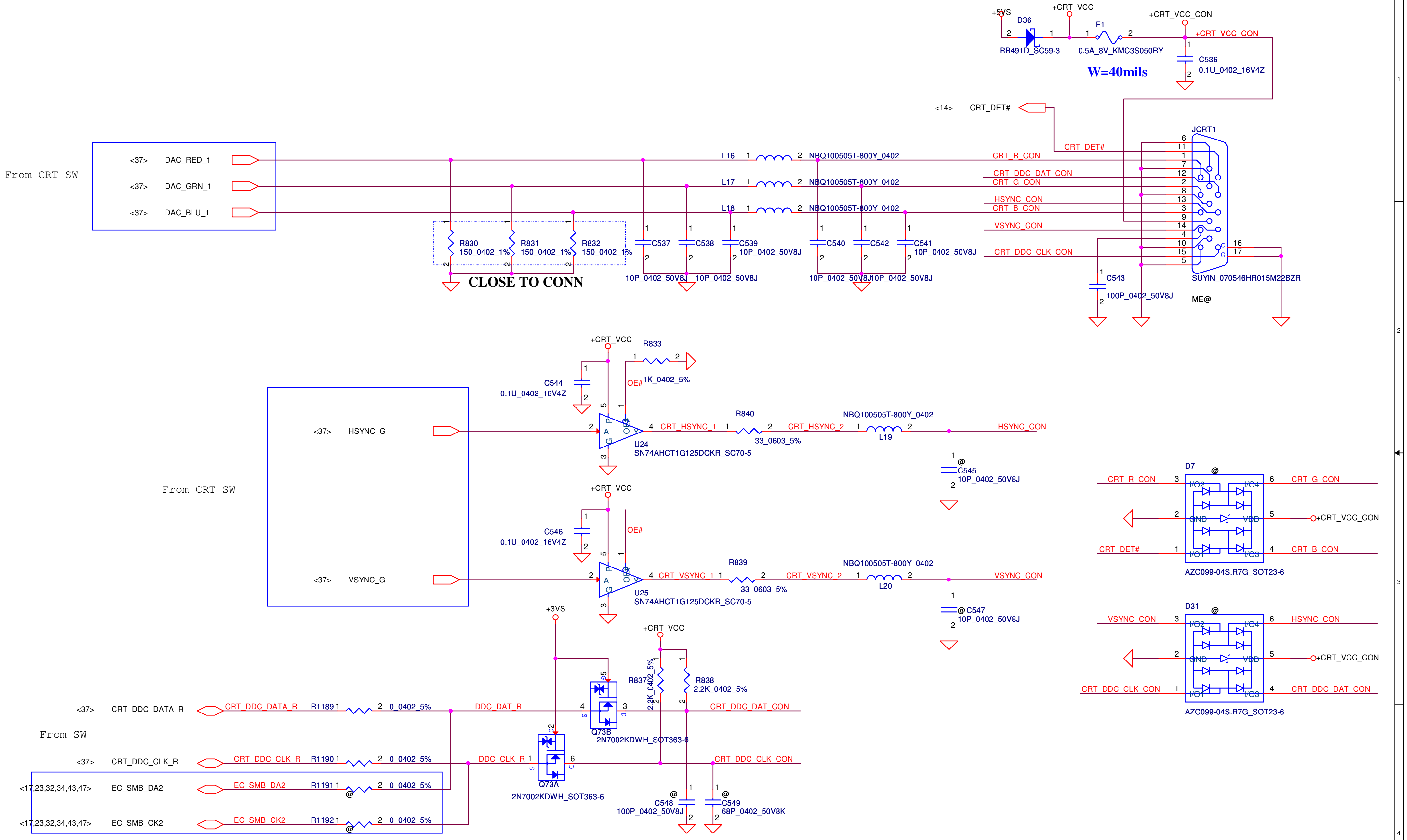
Title
LVDS/ CMOS/ USB-ReDriver

LCFC

Size	Document Number	Rev
Custom	Y401 NM-A031	1.0

Date: Wednesday, March 27, 2013 Sheet 35 of 69

CRT Connector



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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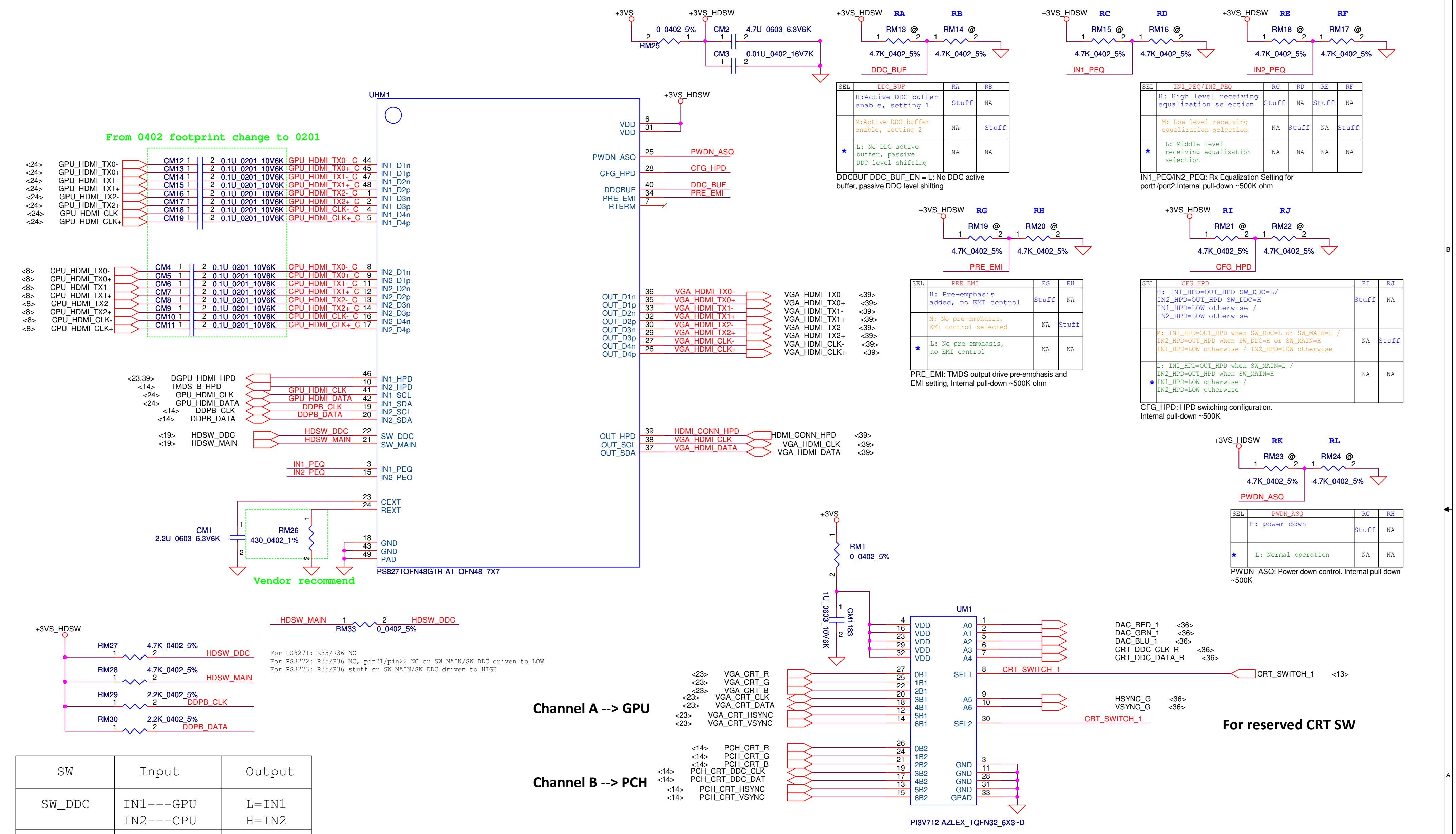
Title
CRT Connector

Size	Document Number	Rev
Custom	Y401 NM-A031	1.0

Date: Wednesday, March 27, 2013 Sheet 36 of 69



Channel A --> GPU

Channel B --> PCH

For reserved CRT SW

For PS8271: R35/R36 NC
For PS8272: R35/R36 NC, pin21/pin22 NC or SW_MAIN/SW_DDC driven to LOW
For PS8273: R35/R36 stuff or SW_MAIN/SW_DDC driven to HIGH

SEL	DDC_BUF	RA	RB
	H:Active DDC buffer enable, setting 1	Stuff	NA
	M:Active DDC buffer enable, setting 2	NA	Stuff
*	L: No DDC active buffer, passive DDC level shifting	NA	NA

DDCBUF DDC_BUF_EN = L: No DDC active buffer, passive DDC level shifting

SEL	IN1_PEQ/IN2_PEQ	RC	RD	RE	RF
	H: High level receiving equalization selection	Stuff	NA	Stuff	NA
	M: Low level receiving equalization selection	NA	Stuff	NA	Stuff
*	L: Middle level receiving equalization selection	NA	NA	NA	NA

IN1_PEQ/IN2_PEQ: Rx Equalization Setting for port1/port2.Internal pull-down ~500K ohm

SEL	PRE_EMI	RG	RH
	H: Pre-emphasis added, no EMI control	Stuff	NA
	M: No pre-emphasis, EMI control selected	NA	Stuff
*	L: No pre-emphasis, no EMI control	NA	NA

PRE_EMI: TMDS output drive pre-emphasis and EMI setting, Internal pull-down ~500K ohm

SEL	CFG_HPD	RI	RJ
	H: IN1_HPD=OUT_HPD SW_DDC=L/ IN2_HPD=OUT_HPD SW_DDC=H IN1_HPD=LOW otherwise / IN2_HPD=LOW otherwise	Stuff	NA
	M: IN1_HPD=OUT_HPD when SW_DDC=L or SW_MAIN=L / IN2_HPD=OUT_HPD when SW_DDC=H or SW_MAIN=H IN1_HPD=LOW otherwise / IN2_HPD=LOW otherwise	NA	Stuff
*	L: IN1_HPD=OUT_HPD when SW_MAIN=L / IN2_HPD=OUT_HPD when SW_MAIN=H IN1_HPD=LOW otherwise / IN2_HPD=LOW otherwise	NA	NA

CFG_HPD: HPD switching configuration.
Internal pull-down ~500K

SEL	PWDN_ASQ	RG	RH
	H: power down	Stuff	NA
*	L: Normal operation	NA	NA

PWDN_ASQ: Power down control. Internal pull-down ~500K

SW	Input	Output

SW_DDC	IN1---GPU
	IN2---CPU
		L=IN1
		H=IN2

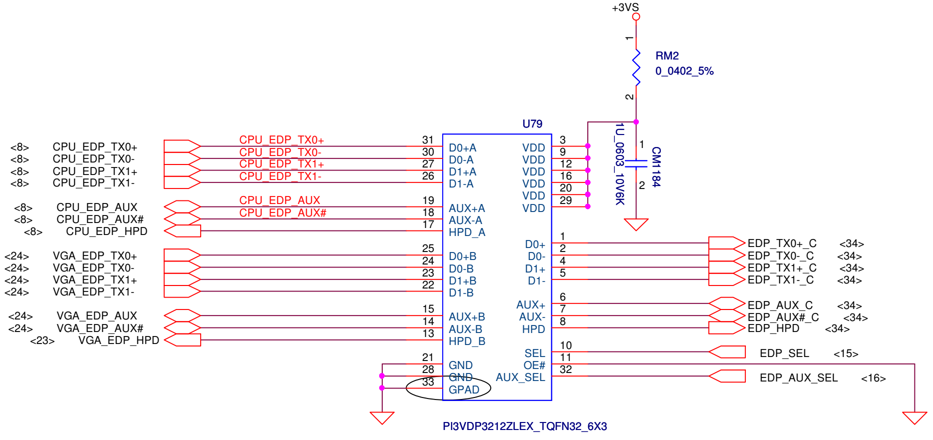
SW_MAIN	IN1---GPU
	IN2---CPU
		L=IN1
		H=IN2

Input SELx	Input/Output An	Function
L	nB1--GPU	An=nB1
H	nB2---PCH	An=nB2

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
HDMI and CRT SW

Size Custom
Document Number Y401 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013



OE#	SEL	AUX_SEL	FUNCTION
L	L	L	PORT A
L	L	H	PORT A-HS, PORT B-HPD/AUX
L	H	L	PORT B-HS, PORT A-HPD/AUX
L	H	H	PORT B
H	X	X	IC POWER DOWN

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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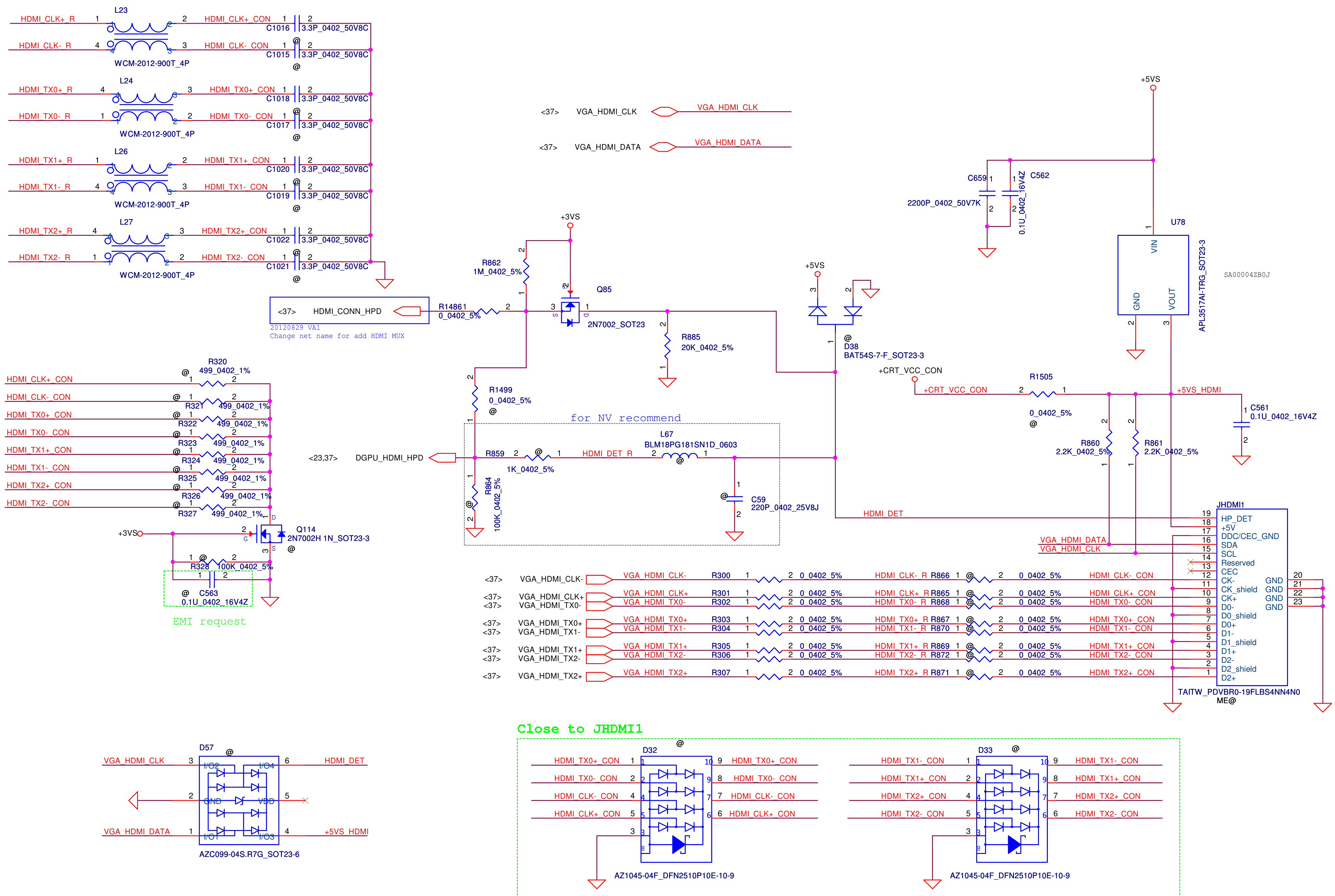
Title
eDP SW

Size Custom
Document Number **Y401 NM-A031**
Rev 1.0
Date: Wednesday, March 27, 2013
Sheet 38 of 69



46@

HDMI+HDCP

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
HDMI_CONN

LCFC

Size: Custom
Document Number: Y401 NM-A031
Rev: 1.0
Date: Wednesday, March 27, 2013
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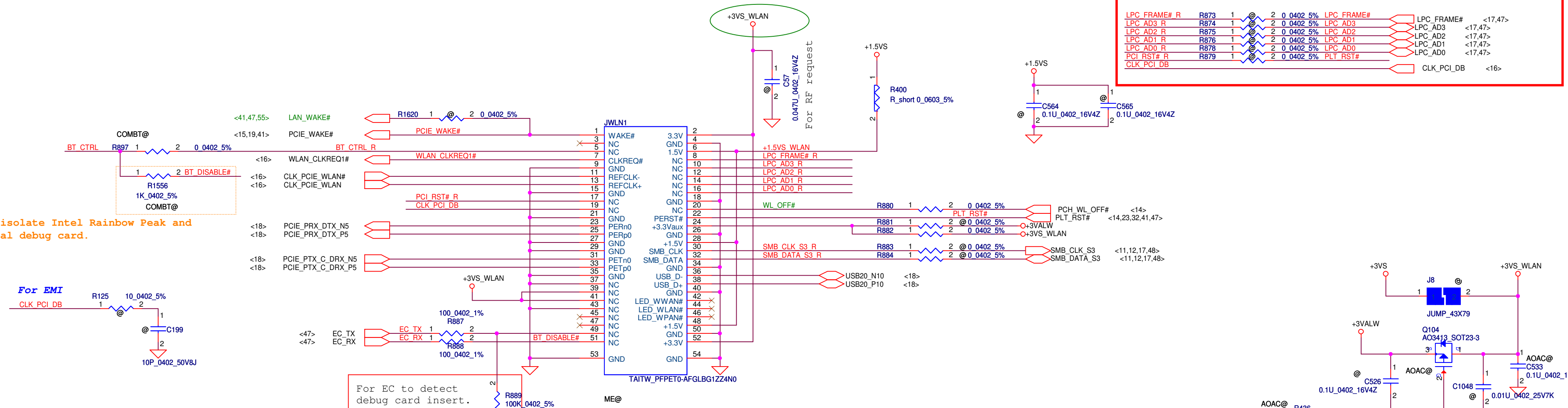
Mini-Express Card(WLAN/WiMAX)

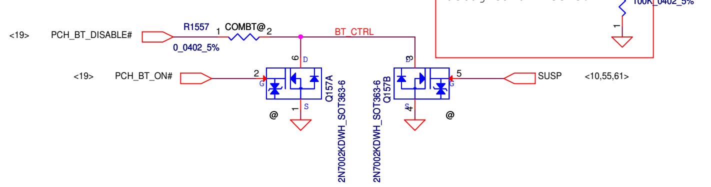
9/18 JP1 Pin2,24,52 contact to +3VS_WLAN for AOAC function

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



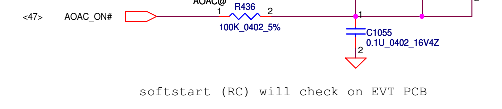
LPC_FRAME#_R R873 0_0402_5% LPC_FRAME# <17,47>
LPC_AD3_R R874 0_0402_5% LPC_AD3 <17,47>
LPC_AD2_R R875 0_0402_5% LPC_AD2 <17,47>
LPC_AD1_R R876 0_0402_5% LPC_AD1 <17,47>
LPC_AD0_R R878 0_0402_5% LPC_AD0 <17,47>
PCI_RST#_R R879 0_0402_5% PLT_RST#
CLK_PCI_DB <16>
+3VS_WLAN
C57 0.047U_0402_16V4Z
For RF request
+1.5VS
R400 R_short 0_0603_5%
C564 0.1U_0402_16V4Z
C565 0.1U_0402_16V4Z
<41,47,55> LAN_WAKE# R1620 0_0402_5%
<15,19,41> PCIE_WAKE#
COMBT@
BT_CTRL R897 0_0402_5% BT_CTRL_R
<16> WLAN_CLKREQ1#
R1556 1K_0402_5% COMBT@ BT_DISABLE#
<16> CLK_PCIE_WLAN#
<16> CLK_PCIE_WLAN
PCI_RST#_R
CLK_PCI_DB
<18> PCIE_PRX_DTX_N5
<18> PCIE_PRX_DTX_P5
<18> PCIE_PTX_C_DRX_N5
<18> PCIE_PTX_C_DRX_P5
JWLN1
WAKE# NC NC CLKREQ# GND REFCLK- REFCLK+ GND NC NC GND PERn0 PERp0 GND GND PETn0 PETp0 GND NC NC NC NC NC NC NC NC GND
3.3V GND 1.5V NC NC NC NC NC GND NC PERST# +3.3Vaux GND +1.5V SMB_CLK SMB_DATA GND USB_D- USB_D+ GND LED_WWAN# LED_WLAN# LED_WPAN# +1.5V GND +3.3V GND
TAITW_PFPET0-AFGLBG1ZZ4N0
+1.5VS_WLAN
LPC_FRAME#_R LPC_AD3_R LPC_AD2_R LPC_AD1_R LPC_AD0_R
WL_OFF# R880 0_0402_5% PCH_WL_OFF# <14>
PLT_RST# PLT_RST# <14,23,32,41,47>
R881 0_0402_5% +3VALW
R882 0_0402_5% +3VS_WLAN
SMB_CLK_S3_R R883 0_0402_5% SMB_CLK_S3 <11,12,17,48>
SMB_DATA_S3_R R884 0_0402_5% SMB_DATA_S3 <11,12,17,48>
USB20_N10 <18>
USB20_P10 <18>
+3VS_WLAN
100_0402_1% R887
<47> EC_TX
<47> EC_RX
R888 100_0402_1%
BT_DISABLE#
For EMI
R125 10_0402_5% CLK_PCI_DB
C199 10P_0402_50V8J
+3VS +3VS_WLAN
J8 JUMP_43X79
+3VALW
Q104 AO3413_SOT23-3
AOAC@ C533 0.1U_0402_16V4Z
AOAC@ C526 0.1U_0402_16V4Z
C1048 0.01U_0402_25V7K
ME@

For isolate Intel Rainbow Peak and Compal debug card.



<19> PCH_BT_DISABLE# R1557 COMBT@ 0_0402_5% BT_CTRL
<19> PCH_BT_ON#
Q157A 2N7002KDWH_SOT363-6
Q157B 2N7002KDWH_SOT363-6
SUSP <10,55,61>
R889 100K_0402_5%

For EC to detect debug card insert.



softstart (RC) will check on EVT PCB

9/18 Increase for Intel AOAC function

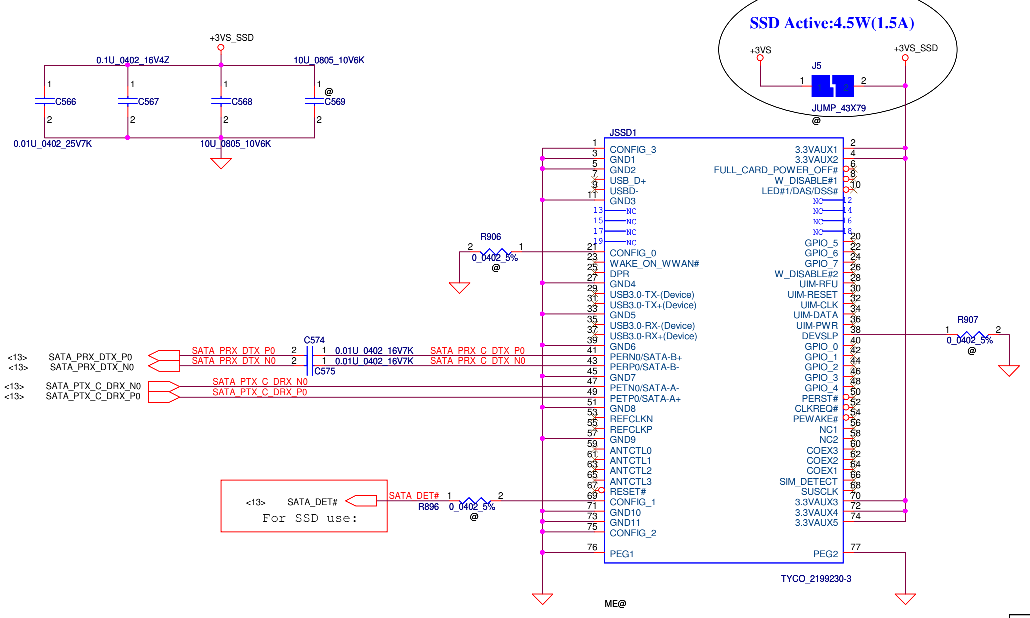
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
* BT_CRTL (GPIO22)	H	L
PCH_BT_ON#	L	H

NGFF(SSD)

Plane

SSD Active:4.5W(1.5A)



+3VS +3VS_SSD J5 JUMP_43X79
+3VS_SSD
C566 0.1U_0402_16V4Z
C567
C568 10U_0805_10V6K
C569 10U_0805_10V6K
0.01U_0402_25V7K
JSSD1
CONFIG_3 GND1 GND2 USB_D+ USBD- GND3 NC NC NC NC CONFIG_0 WAKE_ON_WWAN# DPR GND4 USB3.0-TX-(Device) USB3.0-TX+(Device) GND5 USB3.0-RX-(Device) USB3.0-RX+(Device) GND6 PERN0/SATA-B+ PERP0/SATA-B- GND7 PETN0/SATA-A- PETP0/SATA-A+ GND8 REFCLKN REFCLKP GND9 ANTCTL0 ANTCTL1 ANTCTL2 ANTCTL3 RESET# CONFIG_1 GND10 GND11 CONFIG_2 PEG1
3.3VAUX1 3.3VAUX2 FULL_CARD_POWER_OFF# W_DISABLE#1 LED#1/DAS/DSS# NC NC NC NC GPIO_5 GPIO_6 GPIO_7 W_DISABLE#2 UIM-RFU UIM-RESET UIM-CLK UIM-DATA UIM-PWR DEVSLP GPIO_0 GPIO_1 GPIO_2 GPIO_3 GPIO_4 PERST# CLKREQ# PEWAKE# NC1 NC2 COEX3 COEX2 COEX1 SIM_DETECT SUSCLK 3.3VAUX3 3.3VAUX4 3.3VAUX5 PEG2
TYCO_2199230-3
R906 0_0402_5%
R907 0_0402_5%
<13> SATA_PRX_DTX_P0 SATA_PRX_DTX_P0
<13> SATA_PRX_DTX_N0 SATA_PRX_DTX_N0
C574 0.01U_0402_16V7K SATA_PRX_C_DTX_P0
C575 0.01U_0402_16V7K SATA_PRX_C_DTX_N0
<13> SATA_PTX_C_DRX_N0
<13> SATA_PTX_C_DRX_P0
<13> SATA_DET# R896 0_0402_5%
ME@

For SSD use:

Security Classification	LC Future Center Secret Data			Title
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Mini-Card

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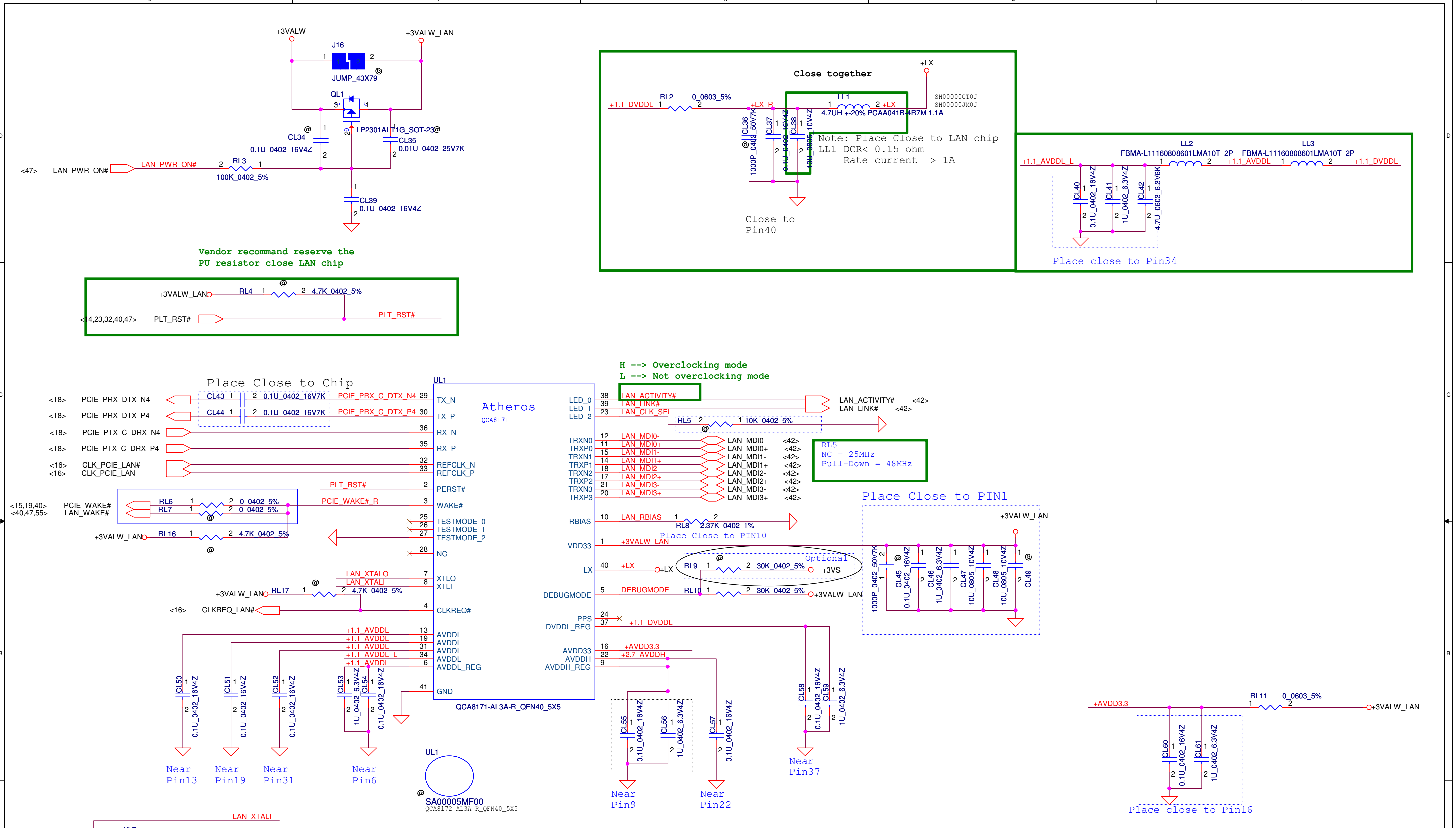
Size	Document Number	Rev
C	Y401 NM-A031	1.0

Date: Wednesday, March 27, 2013 Sheet 40 of 69

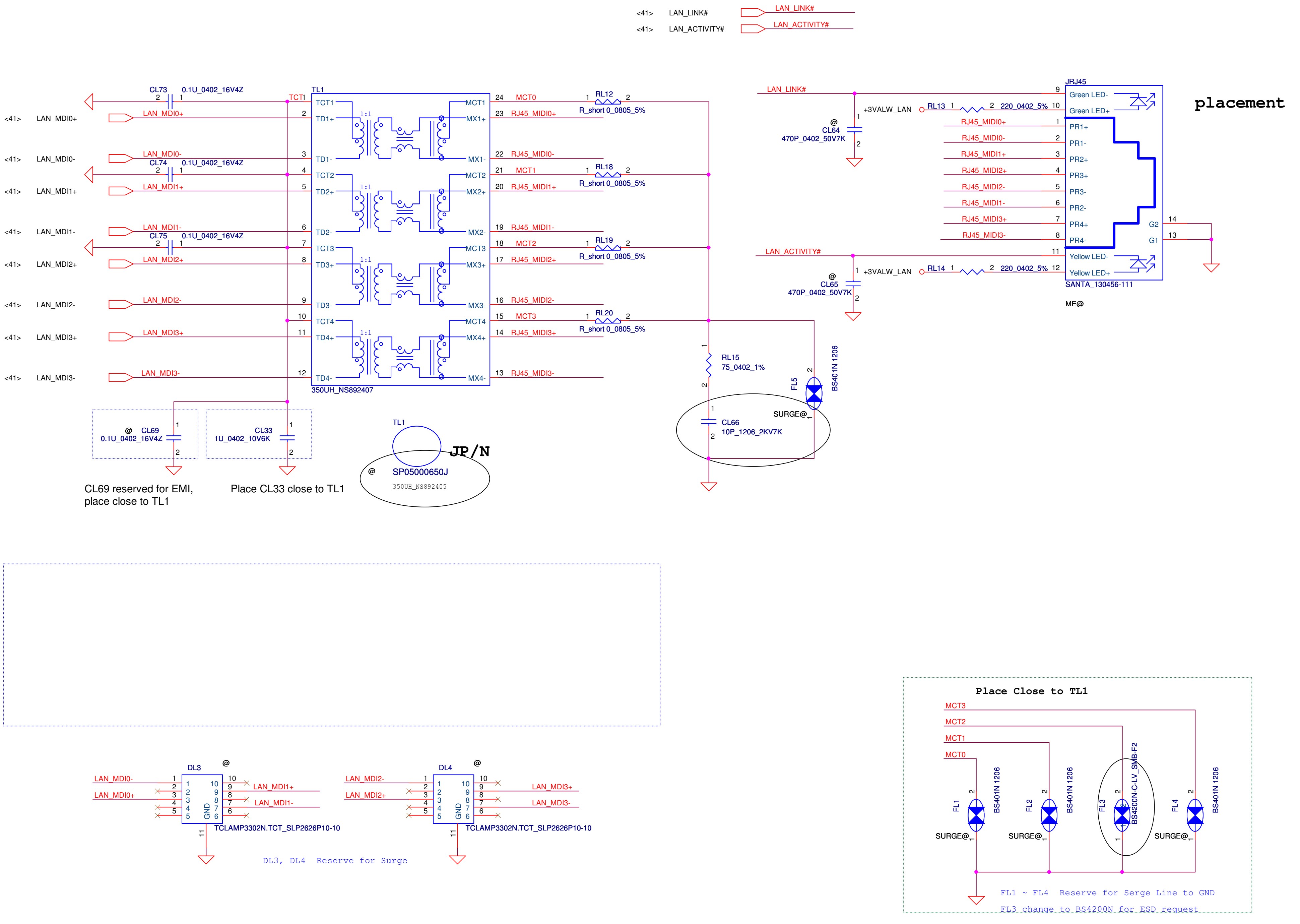


QCA8171/72 Pin defination difference.

	Pin17	Pin18	Pin19	Pin20	Pin21
QCA8171	LAN_MDI2+	LAN_MDI2-	+1.1_AVDDL	LAN_MDI3+	LAN_MDI3-
QCA8172	NC	NC	NC	NC	NC

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
LAN_QCA8171
Size Custom
Document Number **Y401 NM-A031**
Rev 1.0
Date: Wednesday, March 27, 2013



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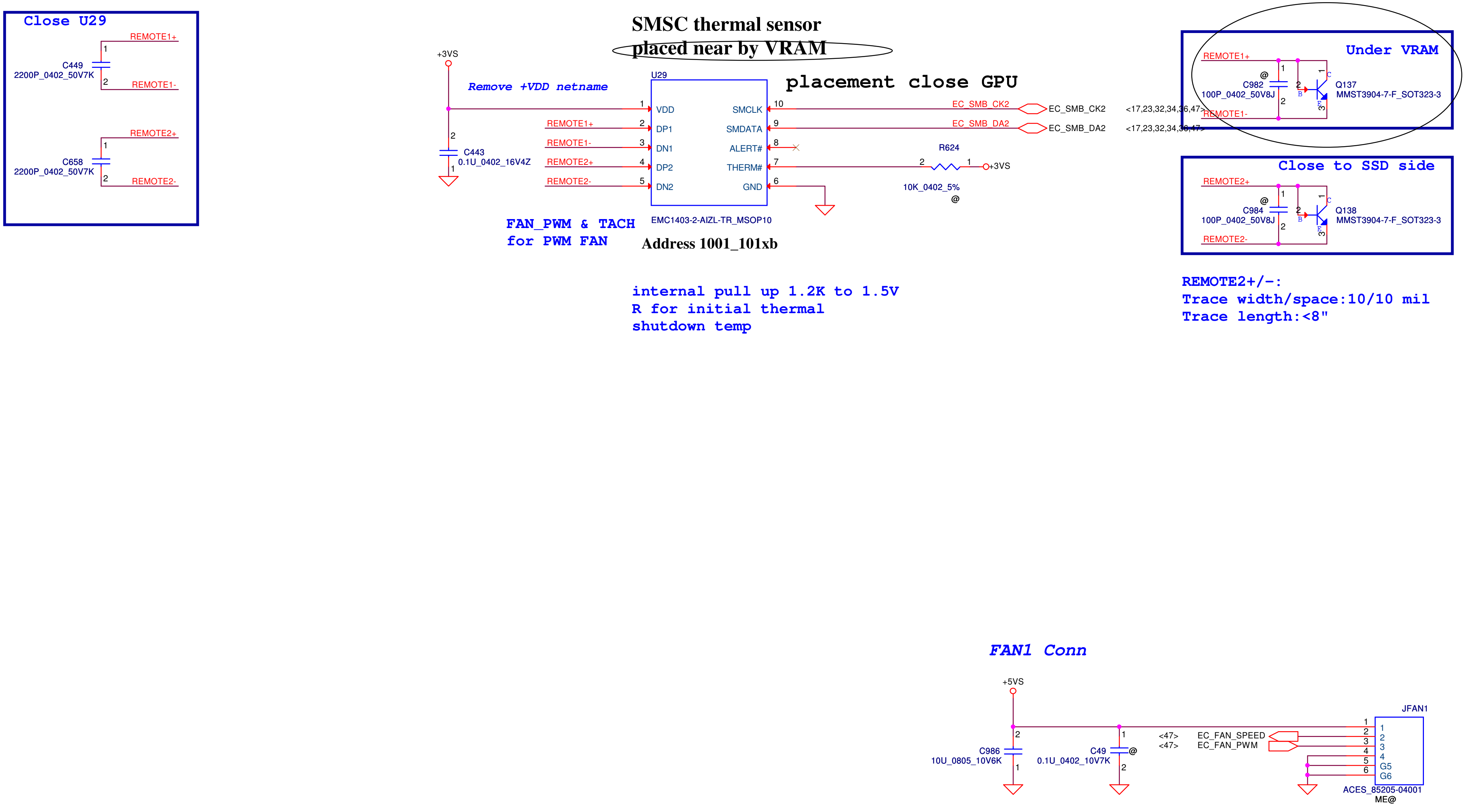
Title
LAN Transformer

LCFC

Size	Document Number	Rev
Custom	Y401 NM-A031	1.0

Date: Wednesday, March 27, 2013 Sheet 42 of 69



internal pull up 1.2K to 1.5V
R for initial thermal
shutdown temp

REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
VGA Thermal sensor/FAN CONN

LCFC

Size	Document Number	Rev
Custom	Y401 NM-A031	1.0

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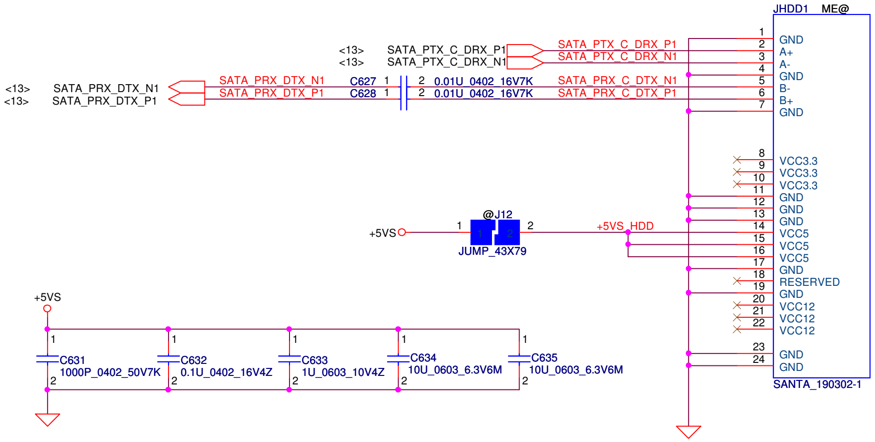
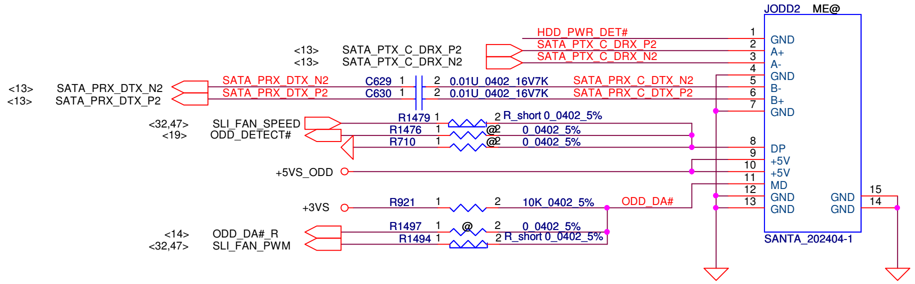
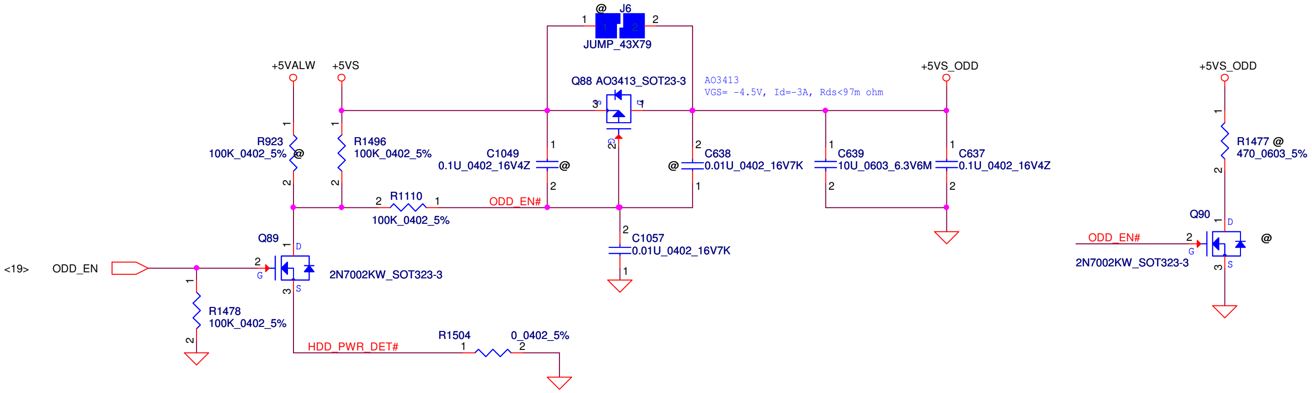
SATA HDD Conn.



SATA ODD Conn.



ODD Power Control



Security Classification	LC Future Center Secret Data			Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	HDD/ODD CONN	LCFC
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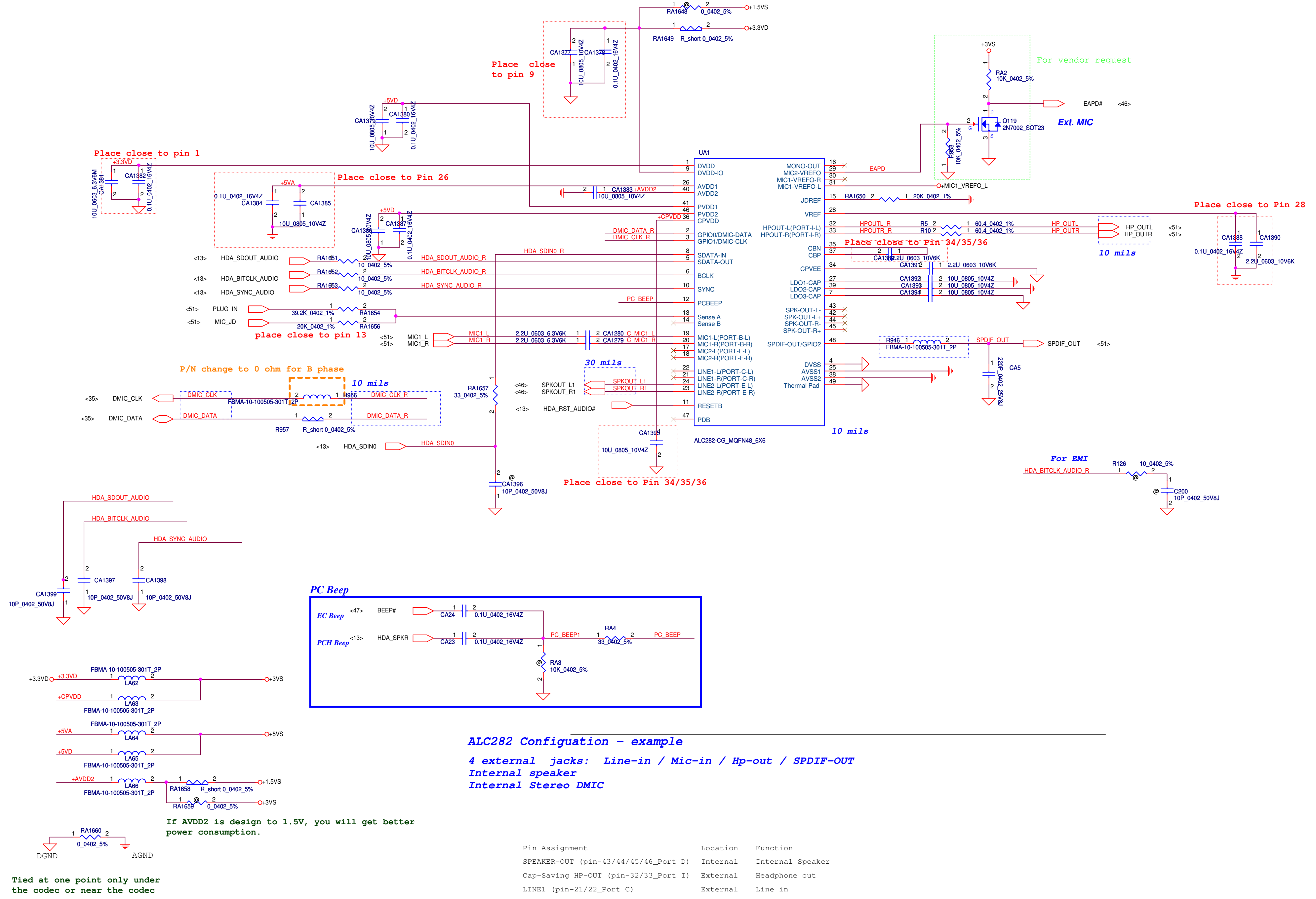
				Rev 1.0	
				Date: Wednesday, March 27, 2013	Sheet 44 of 69



If AVDD2 is design to 1.5V, you will get better power consumption.

Tied at one point only under the codec or near the codec

ALC282 Configuation - example

4 external jacks: Line-in / Mic-in / Hp-out / SPDIF-OUT
Internal speaker
Internal Stereo DMIC

Pin Assignment	Location	Function
SPEAKER-OUT (pin-43/44/45/46_Port D)	Internal	Internal Speaker
Cap-Saving HP-OUT (pin-32/33_Port I)	External	Headphone out
LINE1 (pin-21/22_Port C)	External	Line in
MIC1 (pin-19/20_Port B)	External	Mic in
MONO-OUT (pin-16)	NC	
MIC2 (pin-17/18_Port F)	NC	
DMIC1/2 (pin-2/3)	Internal	Internal Mic (Digital MIC)

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

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Title
Audio Codec
LCFC
Size C
Document Number **Y401 NM-A031**
Rev 1.0
Date: Wednesday, March 27, 2013
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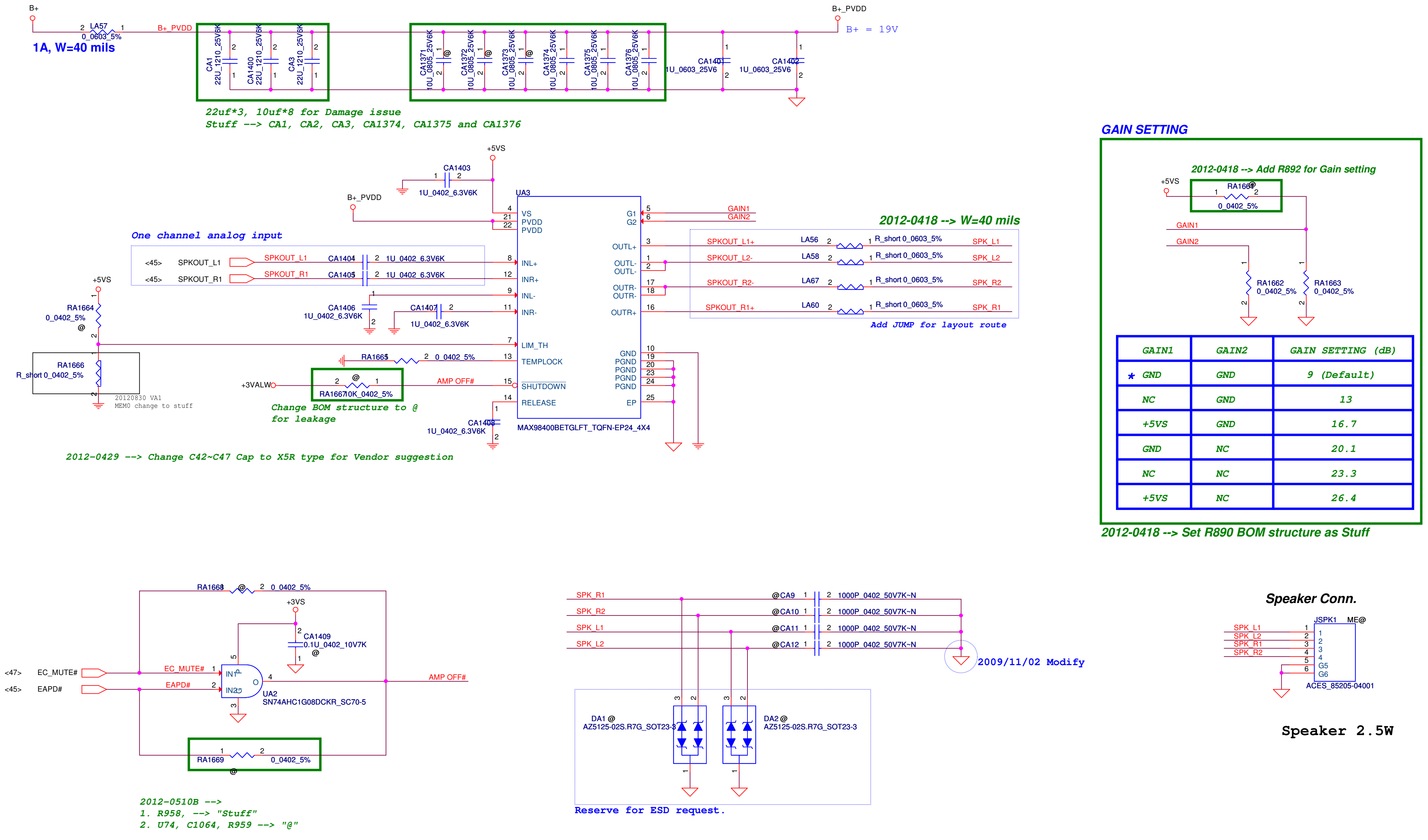

GAIN1	GAIN2	GAIN SETTING (dB)
* GND	GND	9 (Default)
NC	GND	13
+5VS	GND	16.7
GND	NC	20.1
NC	NC	23.3
+5VS	NC	26.4

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/03/09

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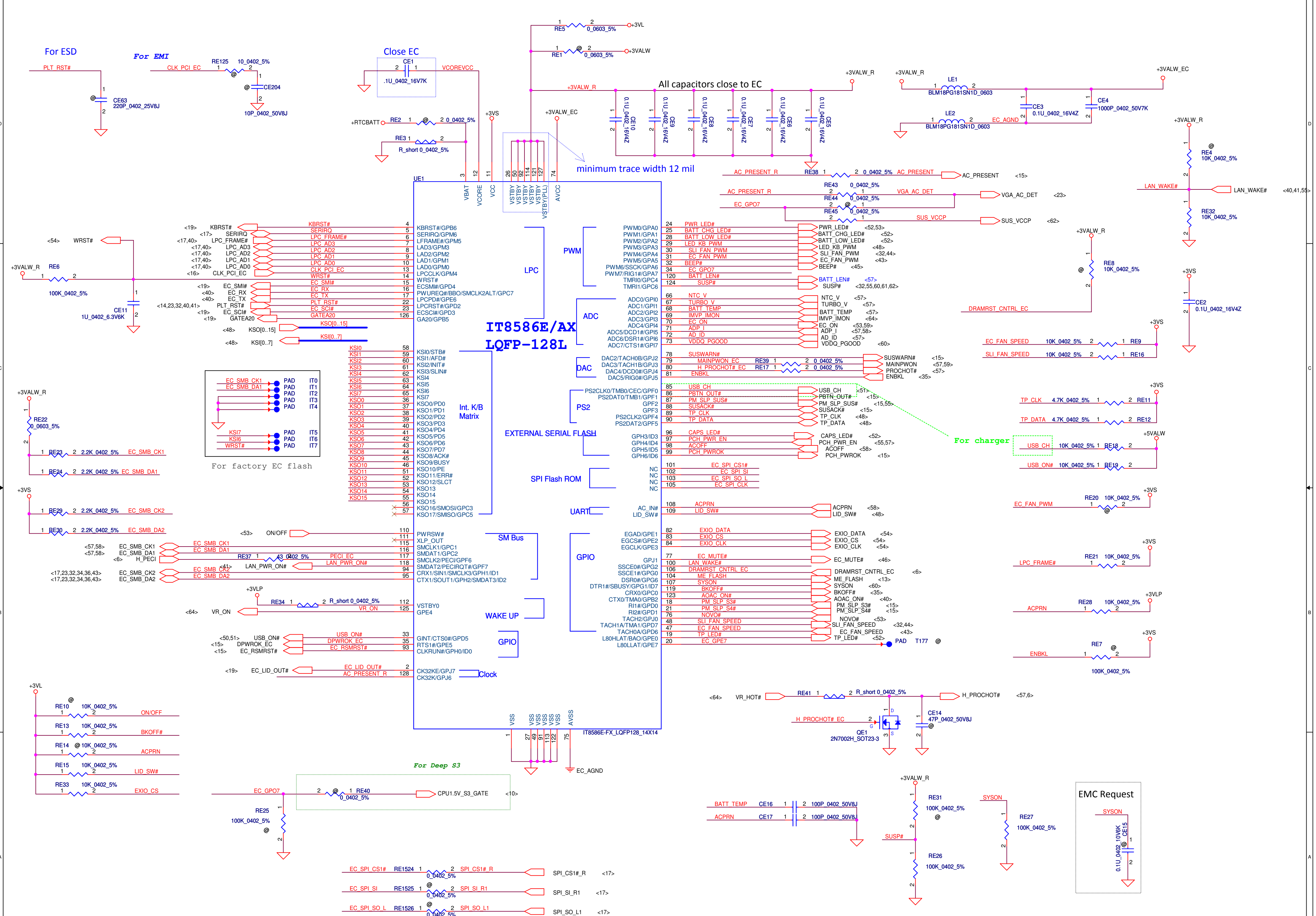
LCFC Electronics, Inc.

Title
AMP-MAX98400BETG+T

Size Custom
Document Number Y401 NM-A031
Rev 1.0

Date: Wednesday, March 27, 2013
Sheet 46 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

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Title
EC ITE8586LQFP

Size C
Document Number **Y401 NM-A031**
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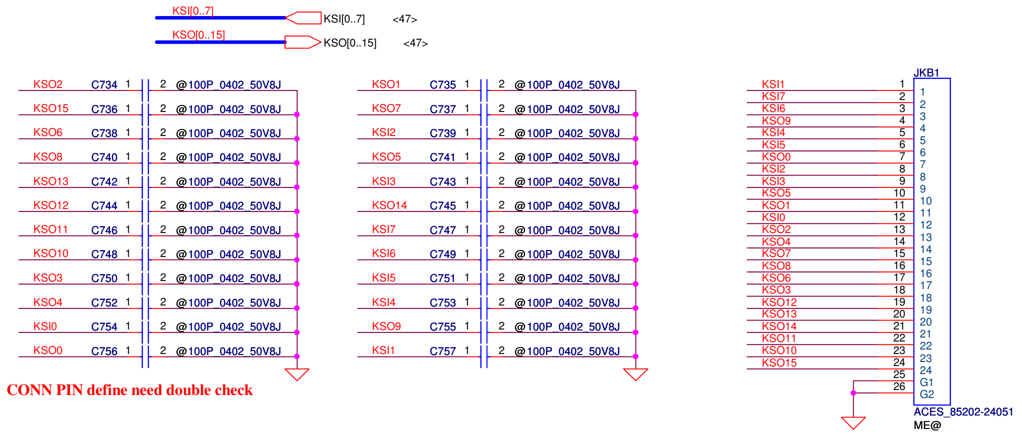
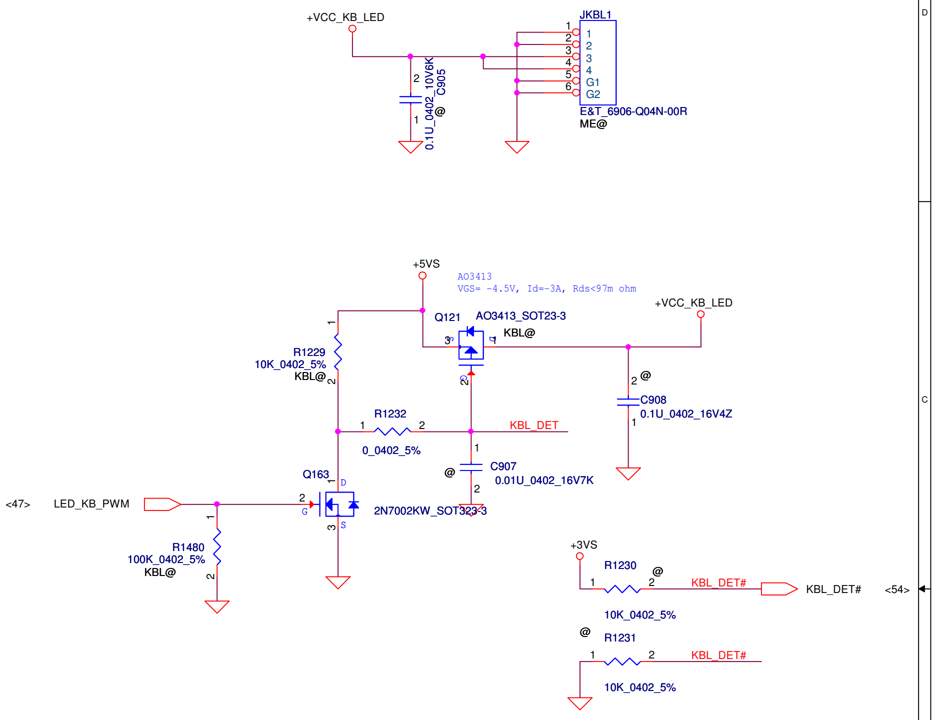
14" INT_KBD Conn.

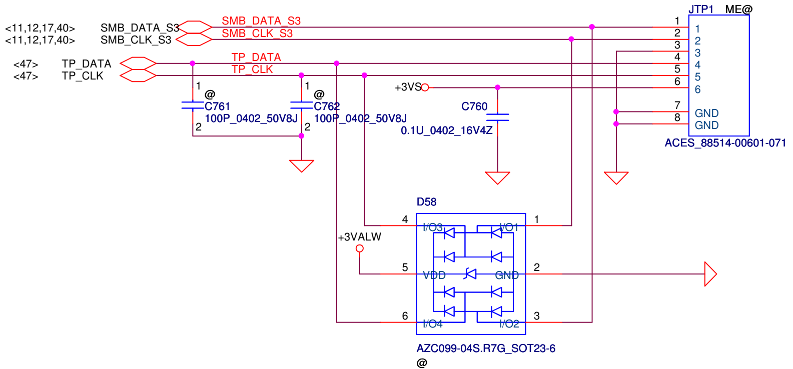

KSI[0..7]
KSI[0..7] <47>
KSO[0..15]
KSO[0..15] <47>
KSO2 C734 1 2 @100P_0402_50V8J
KSO15 C736 1 2 @100P_0402_50V8J
KSO6 C738 1 2 @100P_0402_50V8J
KSO8 C740 1 2 @100P_0402_50V8J
KSO13 C742 1 2 @100P_0402_50V8J
KSO12 C744 1 2 @100P_0402_50V8J
KSO11 C746 1 2 @100P_0402_50V8J
KSO10 C748 1 2 @100P_0402_50V8J
KSO3 C750 1 2 @100P_0402_50V8J
KSO4 C752 1 2 @100P_0402_50V8J
KSI0 C754 1 2 @100P_0402_50V8J
KSO0 C756 1 2 @100P_0402_50V8J
KSO1 C735 1 2 @100P_0402_50V8J
KSO7 C737 1 2 @100P_0402_50V8J
KSI2 C739 1 2 @100P_0402_50V8J
KSO5 C741 1 2 @100P_0402_50V8J
KSI3 C743 1 2 @100P_0402_50V8J
KSO14 C745 1 2 @100P_0402_50V8J
KSI7 C747 1 2 @100P_0402_50V8J
KSI6 C749 1 2 @100P_0402_50V8J
KSI5 C751 1 2 @100P_0402_50V8J
KSI4 C753 1 2 @100P_0402_50V8J
KSO9 C755 1 2 @100P_0402_50V8J
KSI1 C757 1 2 @100P_0402_50V8J
JKB1
KSI1 1
KSI7 2
KSI6 3
KSO9 4
KSI4 5
KSI5 6
KSO0 7
KSI2 8
KSI3 9
KSO5 10
KSO1 11
KSI0 12
KSO2 13
KSO4 14
KSO7 15
KSO8 16
KSO6 17
KSO3 18
KSO12 19
KSO13 20
KSO14 21
KSO11 22
KSO10 23
KSO15 24
25
26
G1
G2
ACES_85202-24051
ME@

CONN PIN define need double check

KB Lighting CONN.4pin

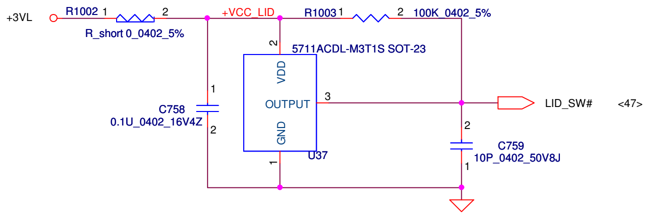


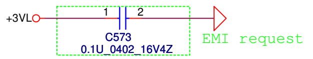
To TP/B Conn.



For ESD request

Lid Switch

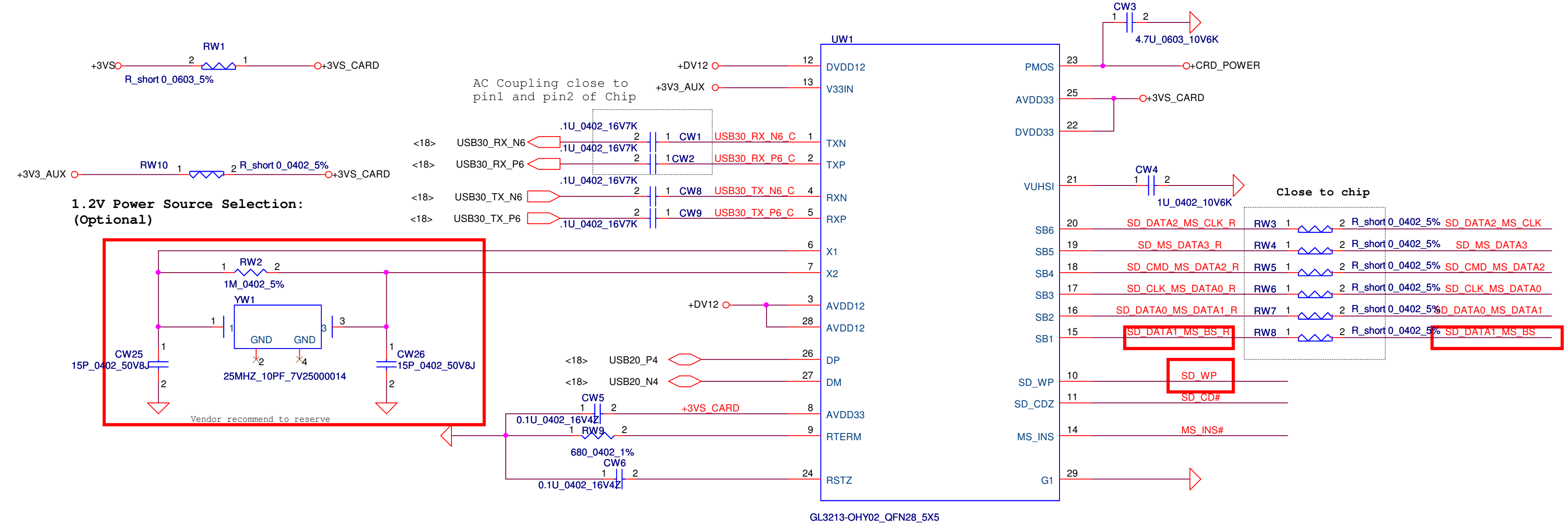


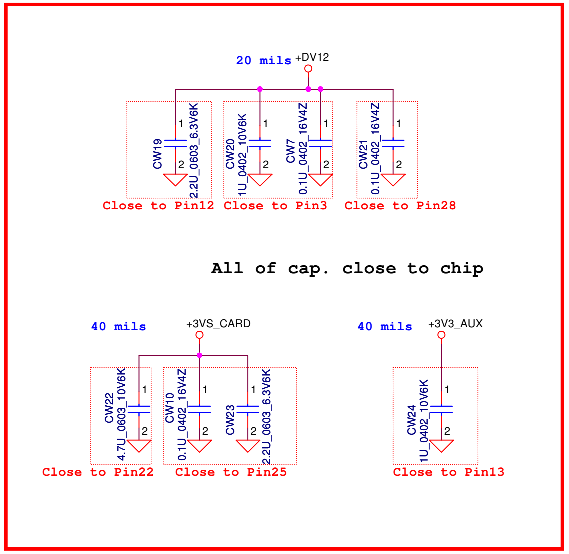


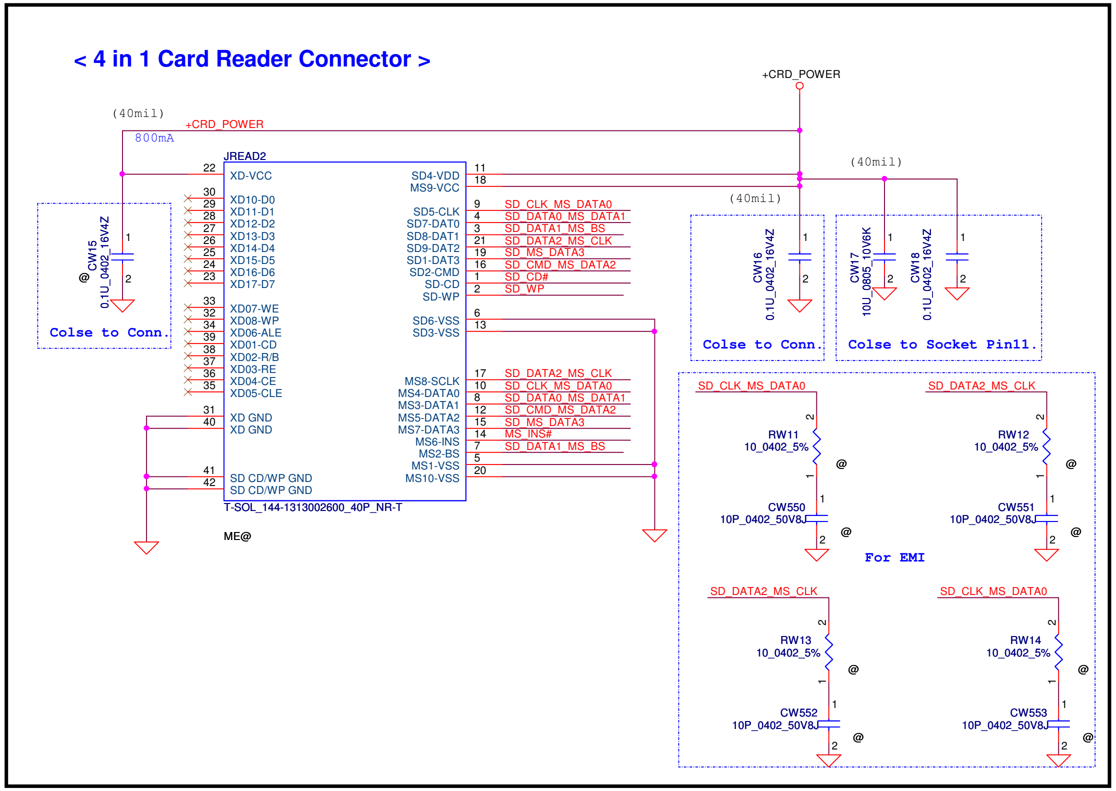
EMI request

Security Classification | LC Future Center Secret Data
Issued Date 2012/07/01 | Deciphered Date 2014/07/01

Title
KB/ KB-LIGHT/ LID IC
Size Custom
Document Number Y401 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013







Security Classification: LC Future Center Secret Data

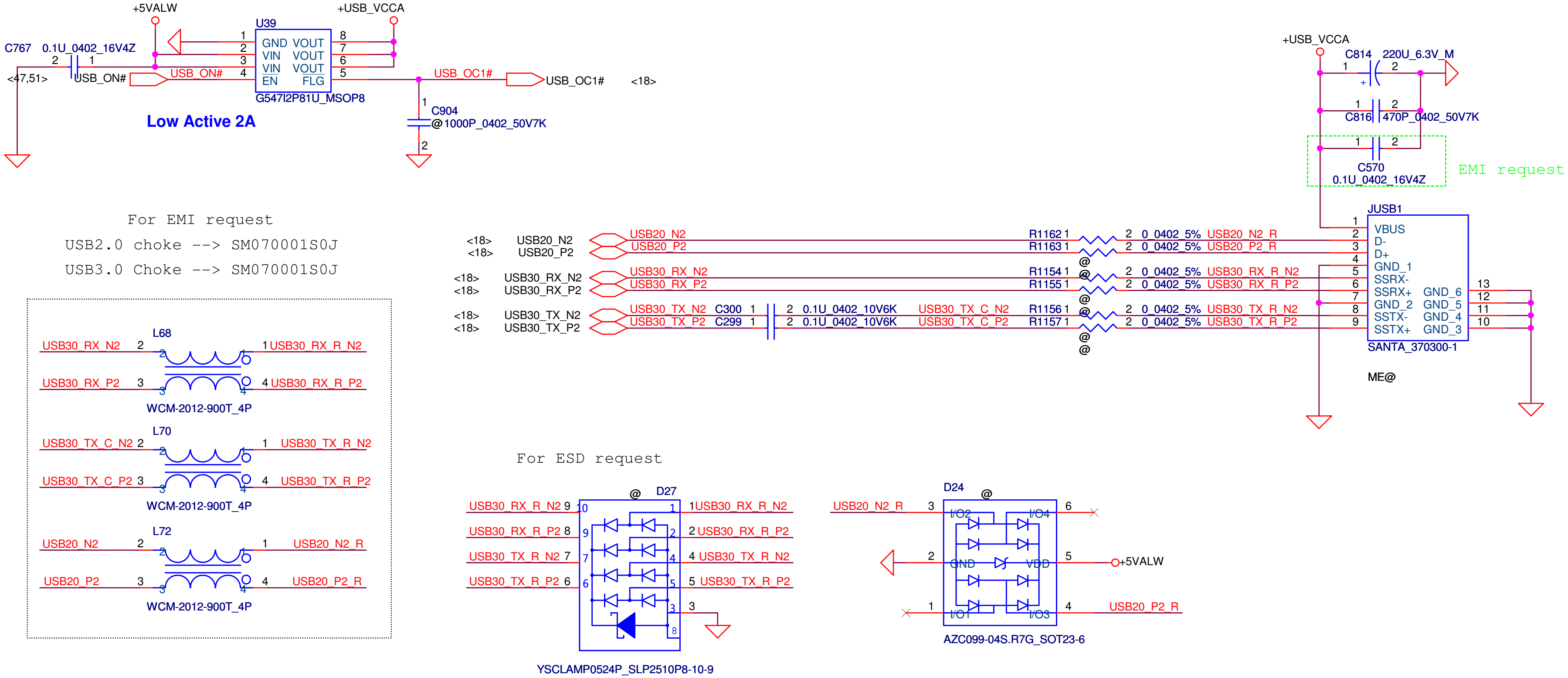
Issued Date: 2012/07/01
Deciphered Date: 2014/07/01

Title
Card reader GL3213

Size: Custom
Document Number: Y401 NM-A031
Rev: 1.0

Date: Wednesday, March 27, 2013

LEFT SIDE USB3.0 PORT X1



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

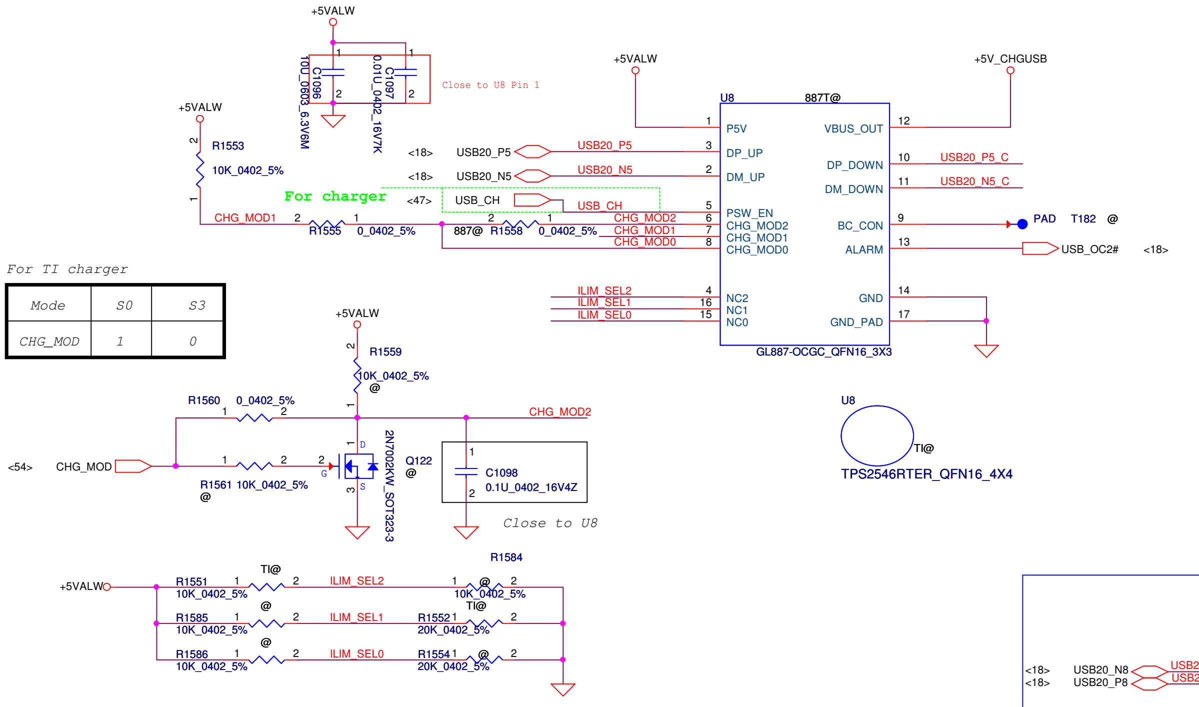
Title
USB 3.0 PORT (LEFT)

LCFC

Size	Document Number	Rev
Custom	Y401 NM-A031	1.0

Date: Wednesday, March 27, 2013 Sheet 50 of 69

Sleep & Charge
Right side USB Charger Port (USB_Port5, near JMIC1)



For TI charger

Mode	S0	S3
CHG_MOD	1	0

Genesys GL887

	CHG_MOD2	CHG_MOD1	CHG_MOD0	Charge Mode
	0	0	0	Charge Disable
*	0	1	0	CDP mode
	0	1	1	DCP mode
	1	0	0	Apple 1A mode
	1	0	1	Apple 2A mode
	1	1	0	Auto mode (DCP and Apple 1A)
*	1	1	1	Auto mode (DCP and Apple 2A)

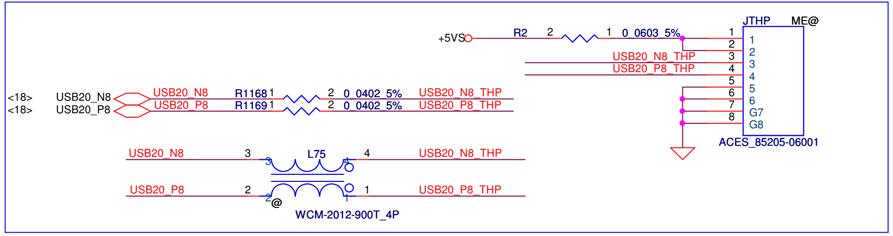
Genesys GL887T

	CHG_MOD2	CHG_MOD1	CHG_MOD0	Charge Mode
	0	0	0	Power down mode
	0	0	1	Auto 2A mode without wake up function
	X	1	0	BC1.2 SDP mode
*	0	1	1	Auto 2A mode with wake up function
	1	0	0	BC1.2 DCP mode
	1	0	1	Apple 2A mode
*	1	1	1	BC1.2 CDP mode with Smart CDP

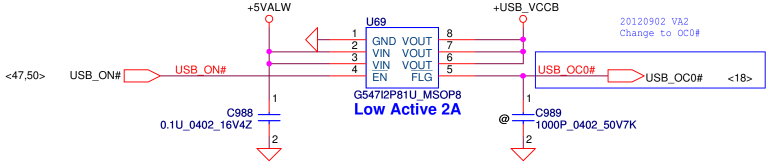
TI TPS2543

	CHG_MOD2	CHG_MOD1	CHG_MOD0	ILIM_SEL2	MODE
	0	0	0	X	**DCH** OUT held low /Data lines disconnected
*	1	1	1	1	**CDP** Data connected and Load detect active
	1	1	1	0	**SDP2** Data connected
	1	1	0	X	**SDP1** Data connected
	0	1	0	X	**SDP1** Data connected
	1	0	0	X	**DCP_Short** Stay in DCP BC1.2 Charging mode
	1	0	1	X	**DCP_Divider** Stay in DCP Divider1 Charging mode
*	0	1	1	X	**DCP_Auto** Data disconnected and Load detect active
	0	0	1	X	**DCP_Auto** Data disconnected and Load detect active

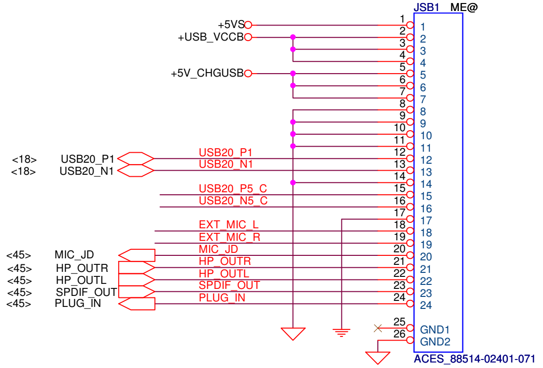
Touch panel



USB Power (USB20_P9)

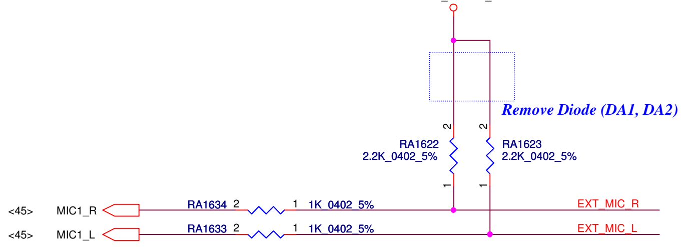


AUDIO/B Conn.



need change to 霧錫 material
COMPAL : SP010015W1J
Footprint : 88514-0240N-071

Ext. MIC



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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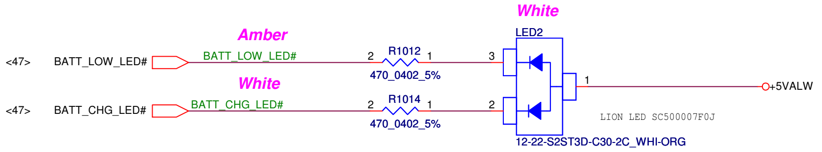
Title
AUDIO-B CONN/ USB CHARGER

LCFC

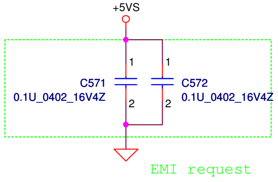
Size: Custom
Document Number: Y401 NM-A031
Rev: 1.0
Date: Wednesday, March 27, 2013
Sheet 51 of 69

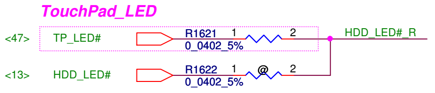
BATT CHARGE/LOW LED

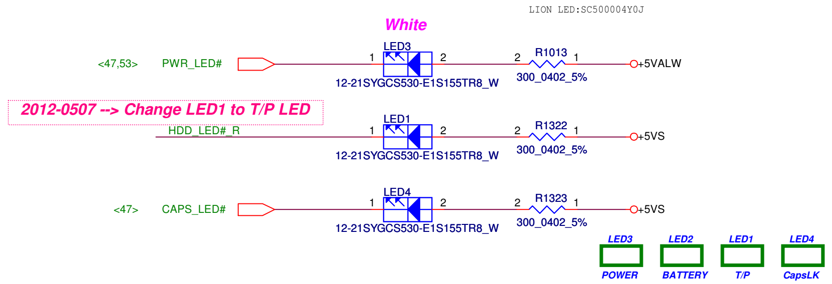


2012-0507 --> Add MOS solution onLED3, 2 to avoid the light blinked.

PWR LED HDD LED CapsLK LED







2012-0507 --> Change LED1 to T/P LED

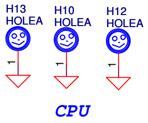
BlueTooth DC

Screw Hole

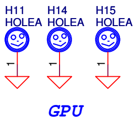
CPU and GPU: H_3P8X 6

MIN PCIE: H_3P3 X 1

C: H_3P8X 3



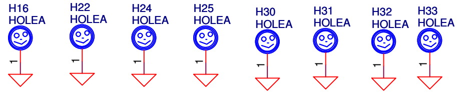
B: H_3P8X 3



E: H_3P3X 1

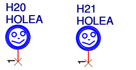
ME: H_8P0 X 8; H_3P3X 1; H_4P0X3P0N X 2; H_2P0X 1

A: H_2P8X 8



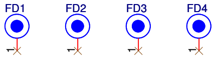
E: H_3P3X 1

H_4P0X3P0NX 3



H_2P0X 2

PCB Fedical Mark PAD



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

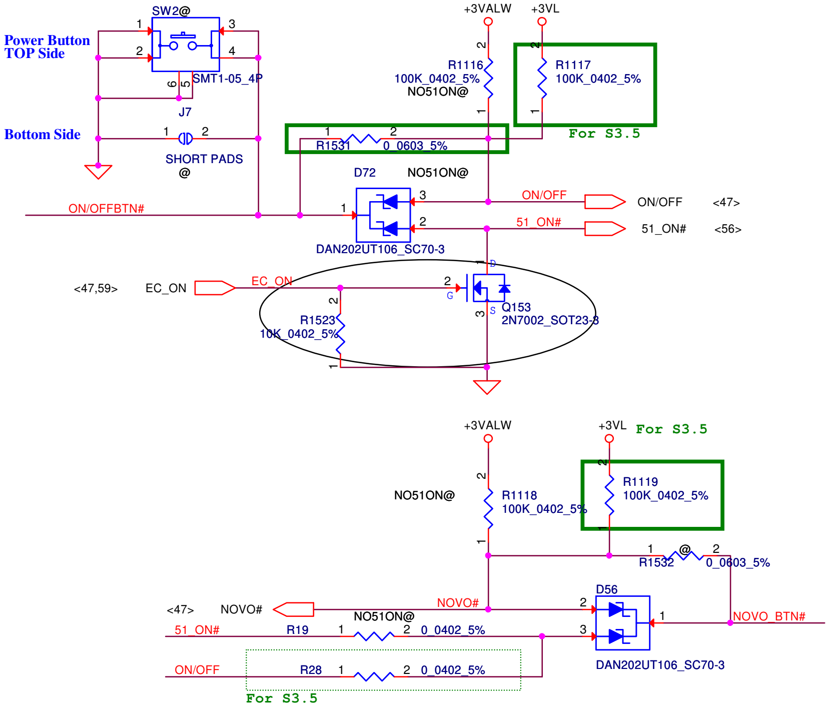
Title
LED

LCFC

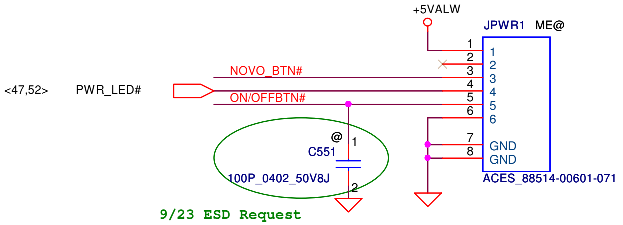
Size	Document Number	Rev
Custom	Y401 NM-A031	1.0

Date: Wednesday, March 27, 2013 Sheet 52 of 69

ON/OFF switch



Power Button/B link
to Function/B Conn. 10pin



EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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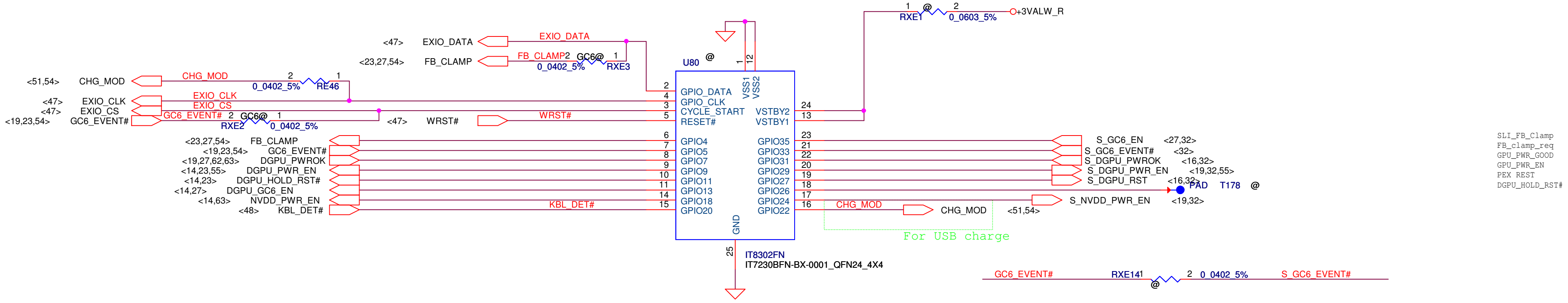
Title
ONOFF SW/ PWR-B CONN/ ISPD

LCFC

Size	Document Number	Rev
Custom	Y401 NM-A031	1.0

Date: Wednesday, March 27, 2013 Sheet 53 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

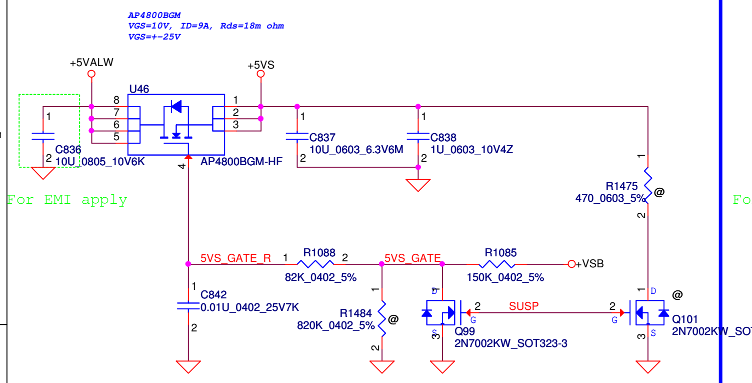
Title
EX IO

LCFC

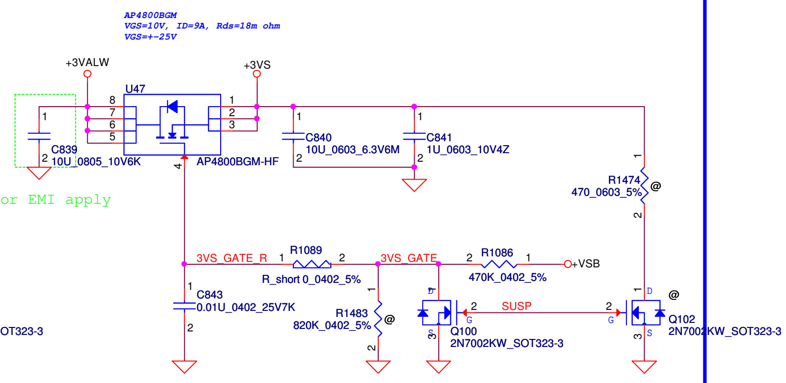
Size Custom
Document Number **Y501 NM-A031**
Rev 1.0

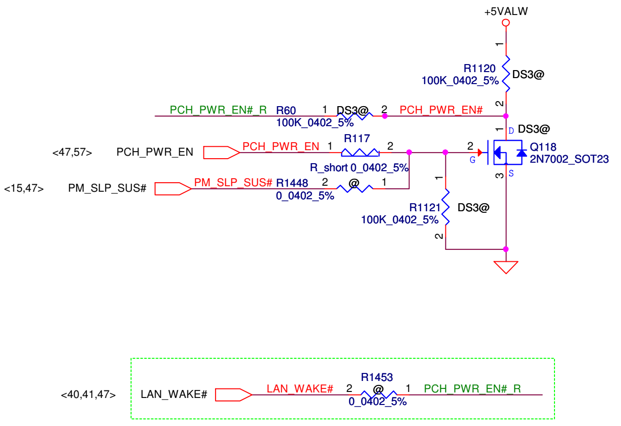
Date: Wednesday, March 27, 2013 Sheet 54 of 69

+5VALW to +5VS



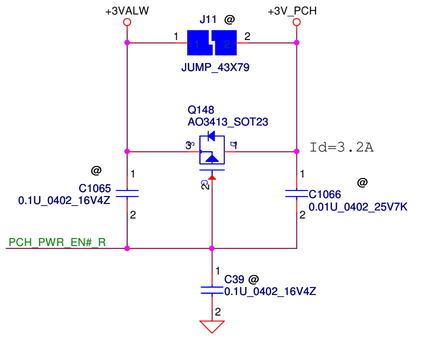
+3VALW to +3VS

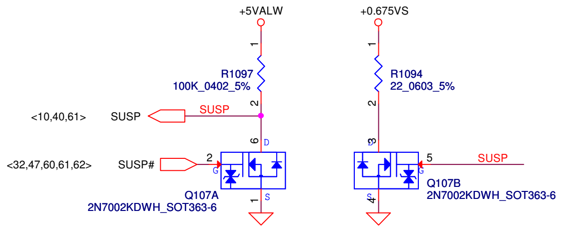




For B phase test,通知power 修改57頁 (反向)

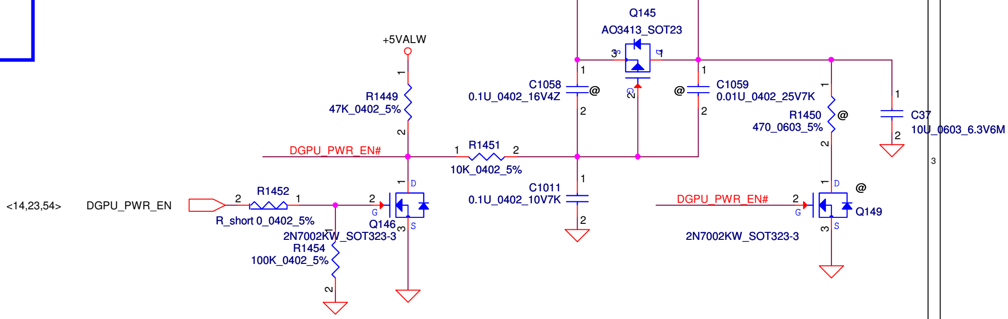
+3VALW to +3V_PCH





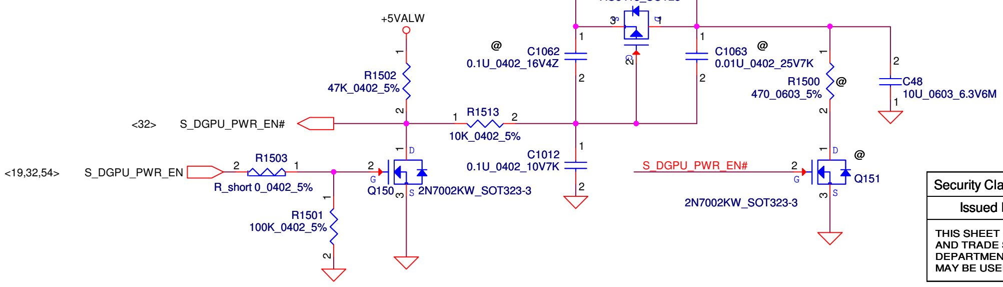
For Intel S3 Power Reduction.

+3VS to +3VS_VGA



+3VS to +3VS_SLI

2012-0419 ---> modify +3VS_SLI BOM structure to "SLI@"



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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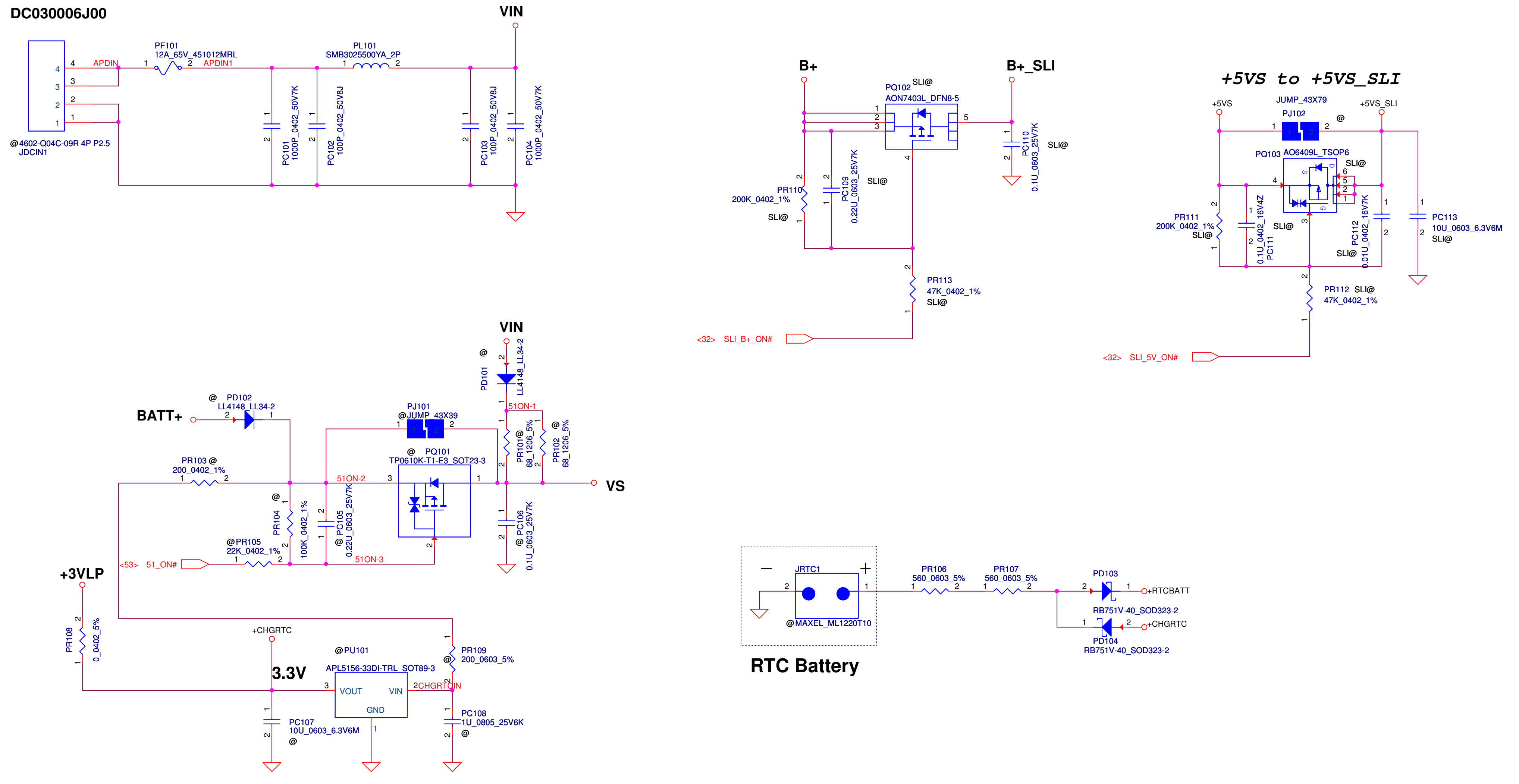
Title
DC V TO VS INTERFACE

LCFC

Size	Document Number	Rev
Custom	Y401 NM-A031	1.0

Date: Wednesday, March 27, 2013 | Sheet 55 of 69



Security Classification	LC Future Center Secret Data			Title
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Vin Detector

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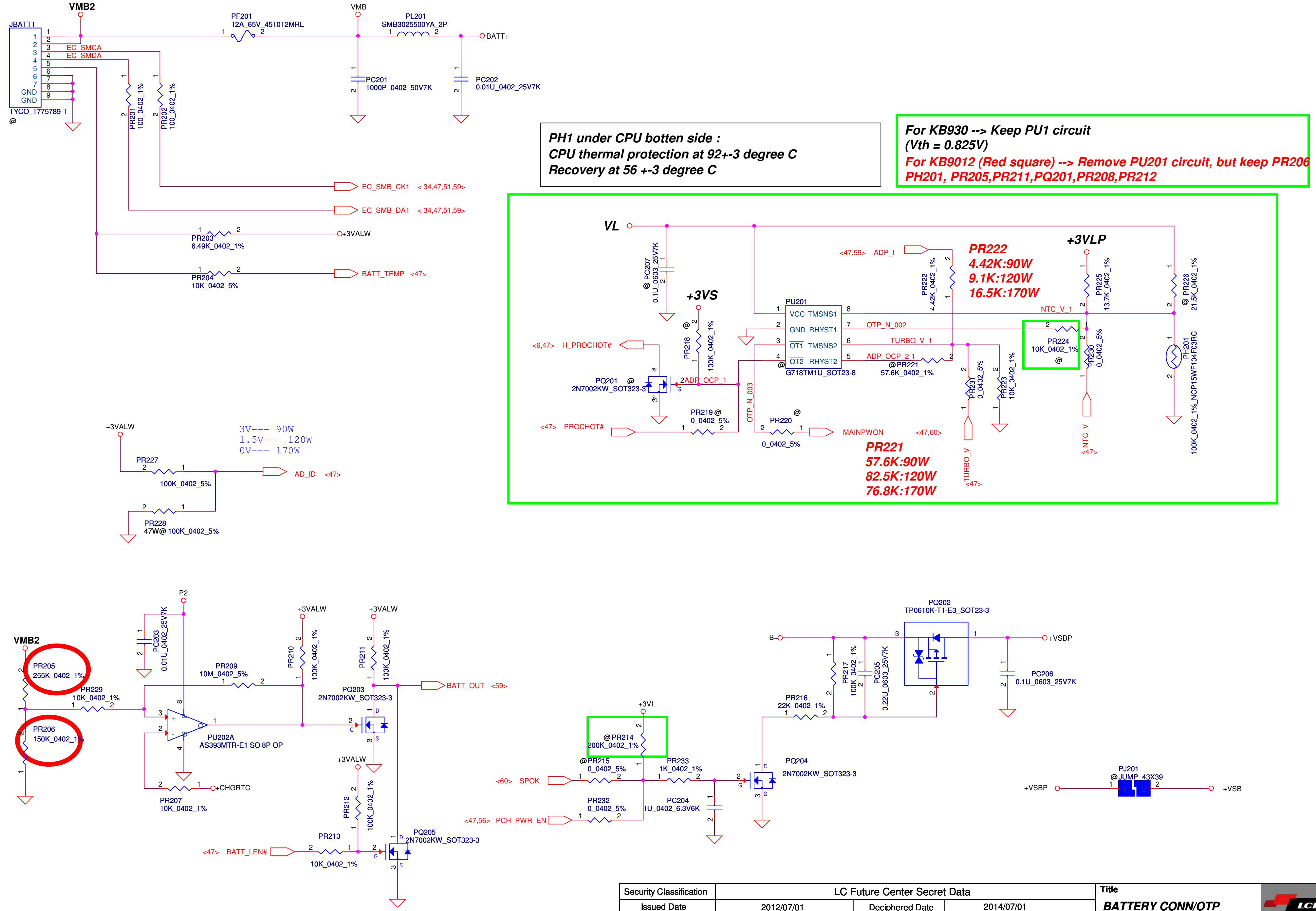
Size	Document Number	Rev
Custom	Y410 NM-A031	1.0

Date: Wednesday, March 27, 2013 Sheet 56 of 69



PH1 under CPU botten side :
CPU thermal protection at 92+-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205,PR211,PQ201,PR208,PR212

PR222
4.42K:90W
9.1K:120W
16.5K:170W

PR221
57.6K:90W
82.5K:120W
76.8K:170W

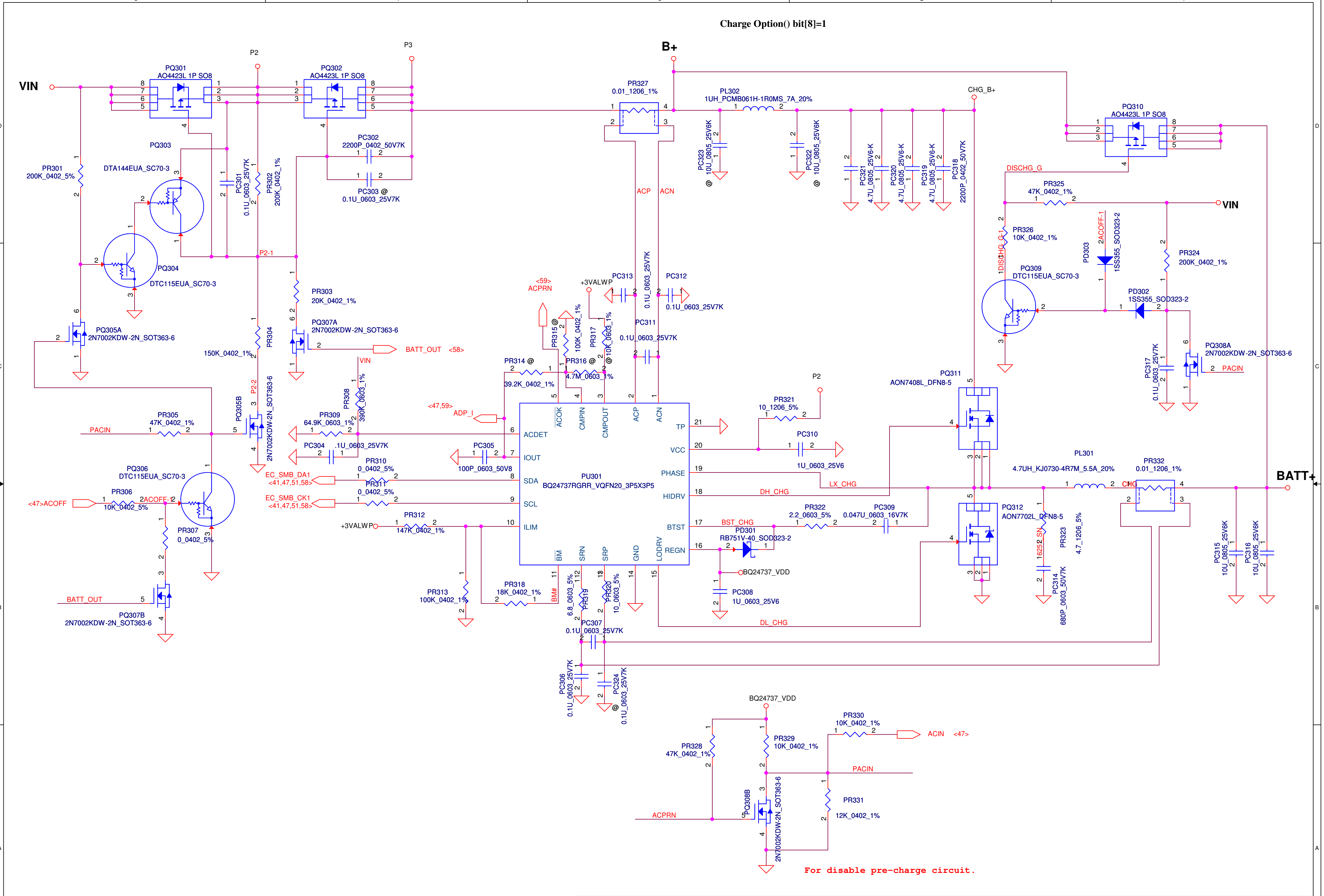
3V--- 90W
1.5V--- 120W
0V--- 170W

Security Classification | LC Future Center Secret Data
Issued Date 2012/07/01 | Deciphered Date 2014/07/01

Title
BATTERY CONN/OTP

Size Custom | Document Number Y410 NM-A031 | Rev 1.0

Date: Wednesday, March 27, 2013 | Sheet 57 of 69



Security Classification | LC Future Center Secret Data

Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01

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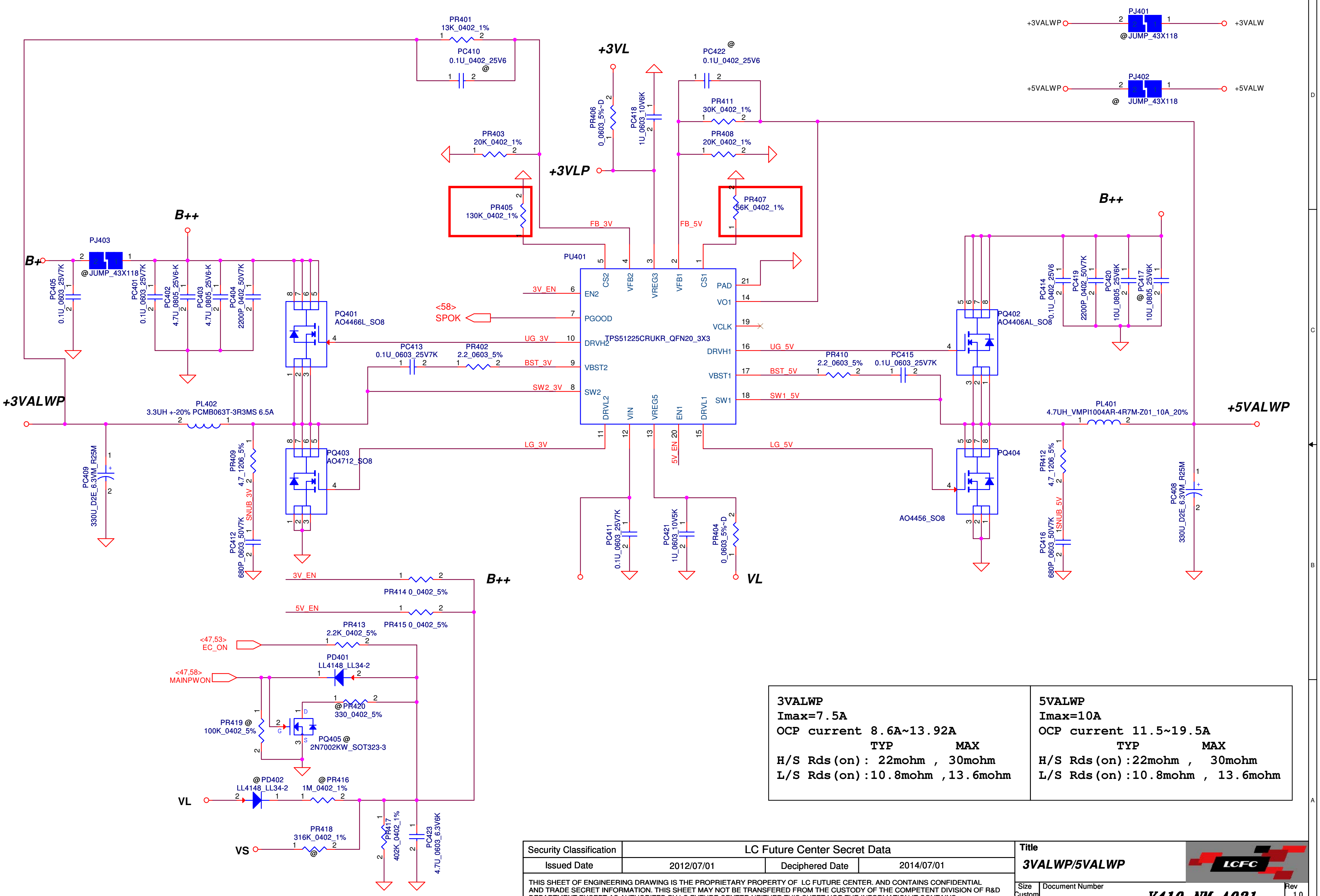
Title
CHARGER

Size Custom
Document Number **Y410 NM-A031**
Rev 1.0

Date: Wednesday, March 27, 2013
Sheet 58 of 69



3VALWP	5VALWP
Imax=7.5A	Imax=10A
OCP current 8.6A~13.92A	OCP current 11.5~19.5A
TYP MAX	TYP MAX
H/S Rds(on): 22mohm , 30mohm	H/S Rds(on):22mohm , 30mohm
L/S Rds(on):10.8mohm ,13.6mohm	L/S Rds(on):10.8mohm , 13.6mohm

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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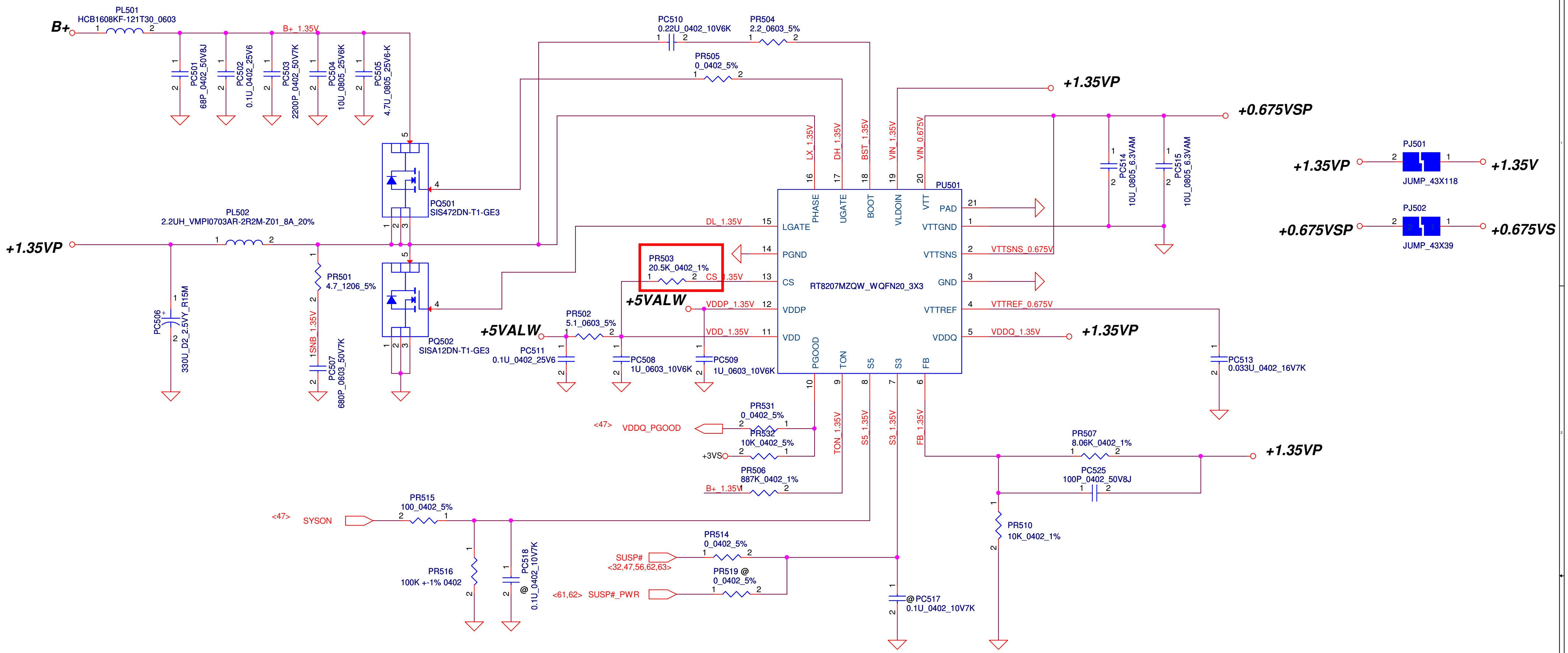
Title
3VALWP/5VALWP

LCFC

Size Custom
Document Number **Y410 NM-A031**
Rev 1.0

Date: Wednesday, March 27, 2013



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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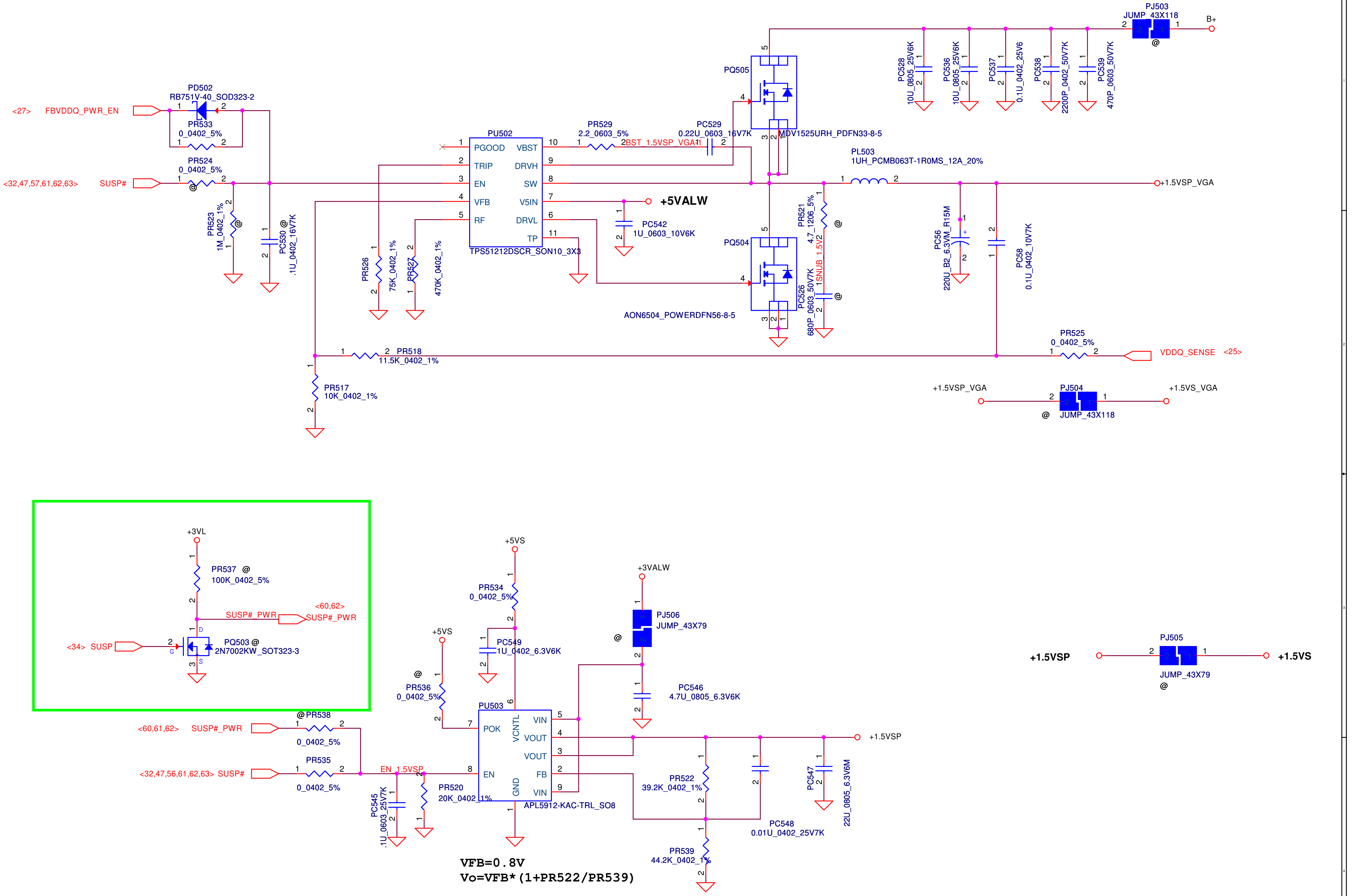
Title
1.35VP/0.675VSP

LCFC

Size	Document Number	Rev
Custom	Y410 NM-A031	1.0

Date: Wednesday, March 27, 2013 Sheet 60 of 69

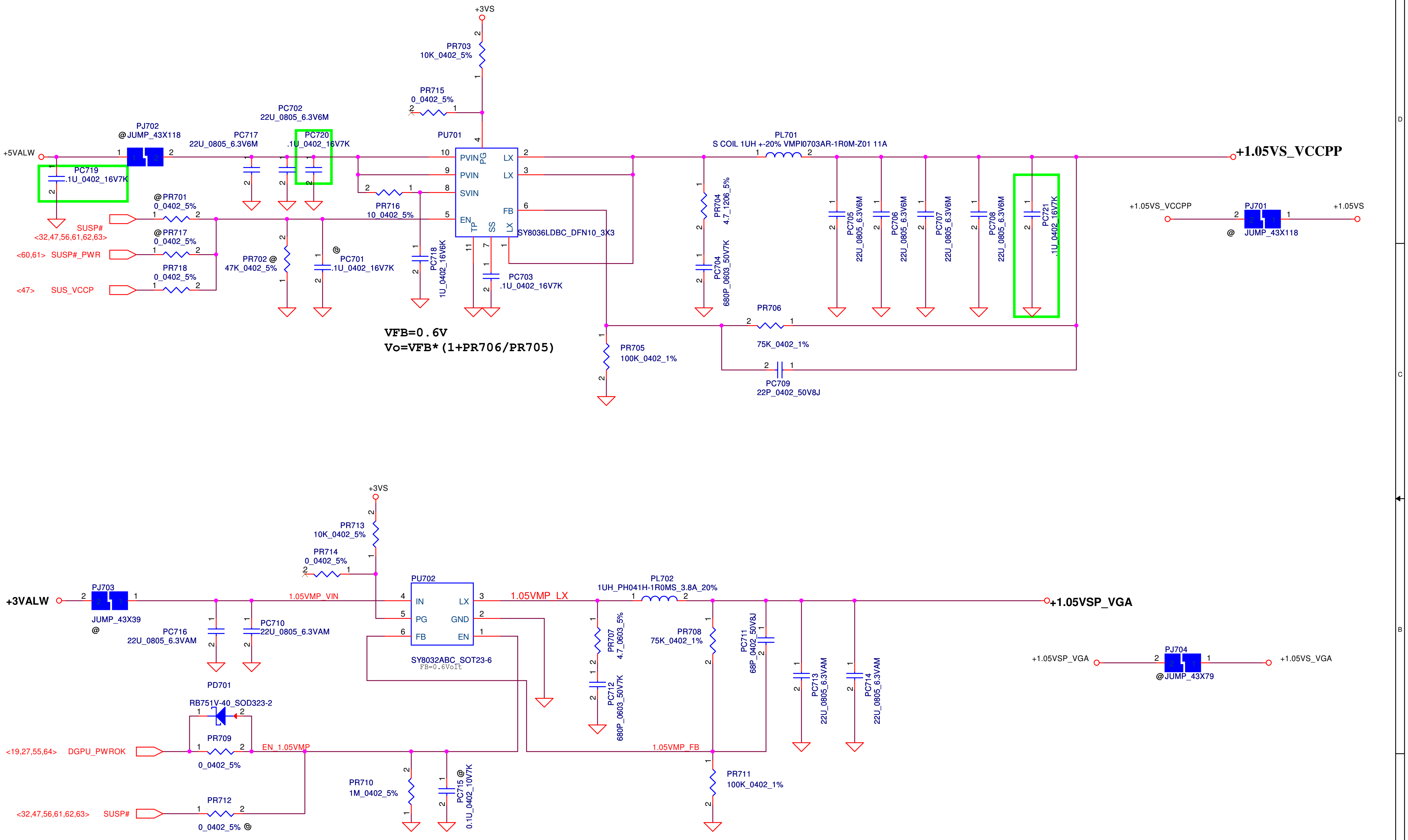


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
+1.5VS_VGA/+1.5VS

LCFC

Size Custom
Document Number Y410 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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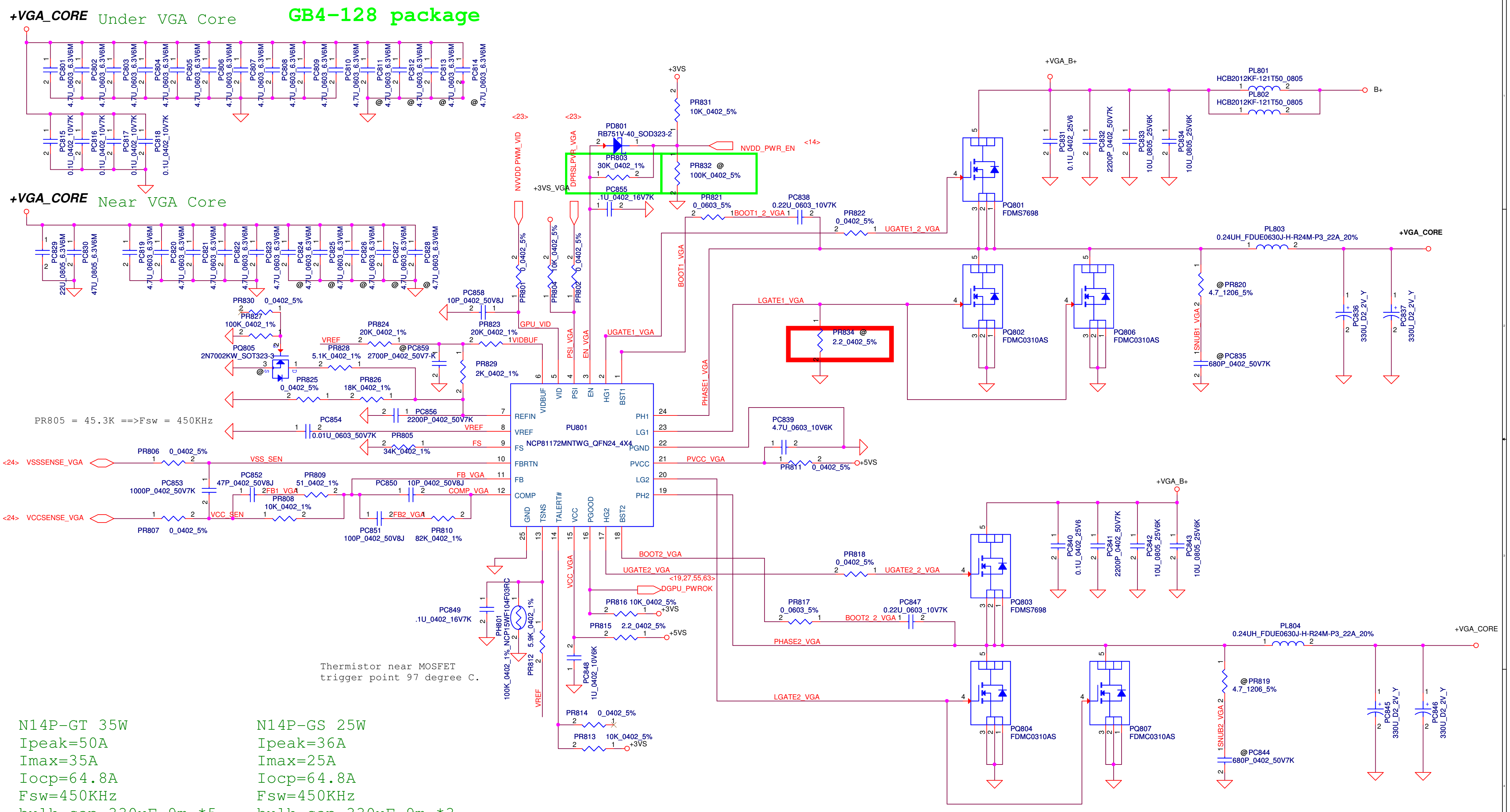
Title
+1.05VS/+1.05VS_VGA

Size	Document Number	Rev
Custom	Y410 NM-A031	1.0

Date: Wednesday, March 27, 2013 | Sheet 62 of 69



N14P-GT 35W
Ipeak=50A
Imax=35A
Iocp=64.8A
Fsw=450KHz
bulk cap 330uF 9m *5

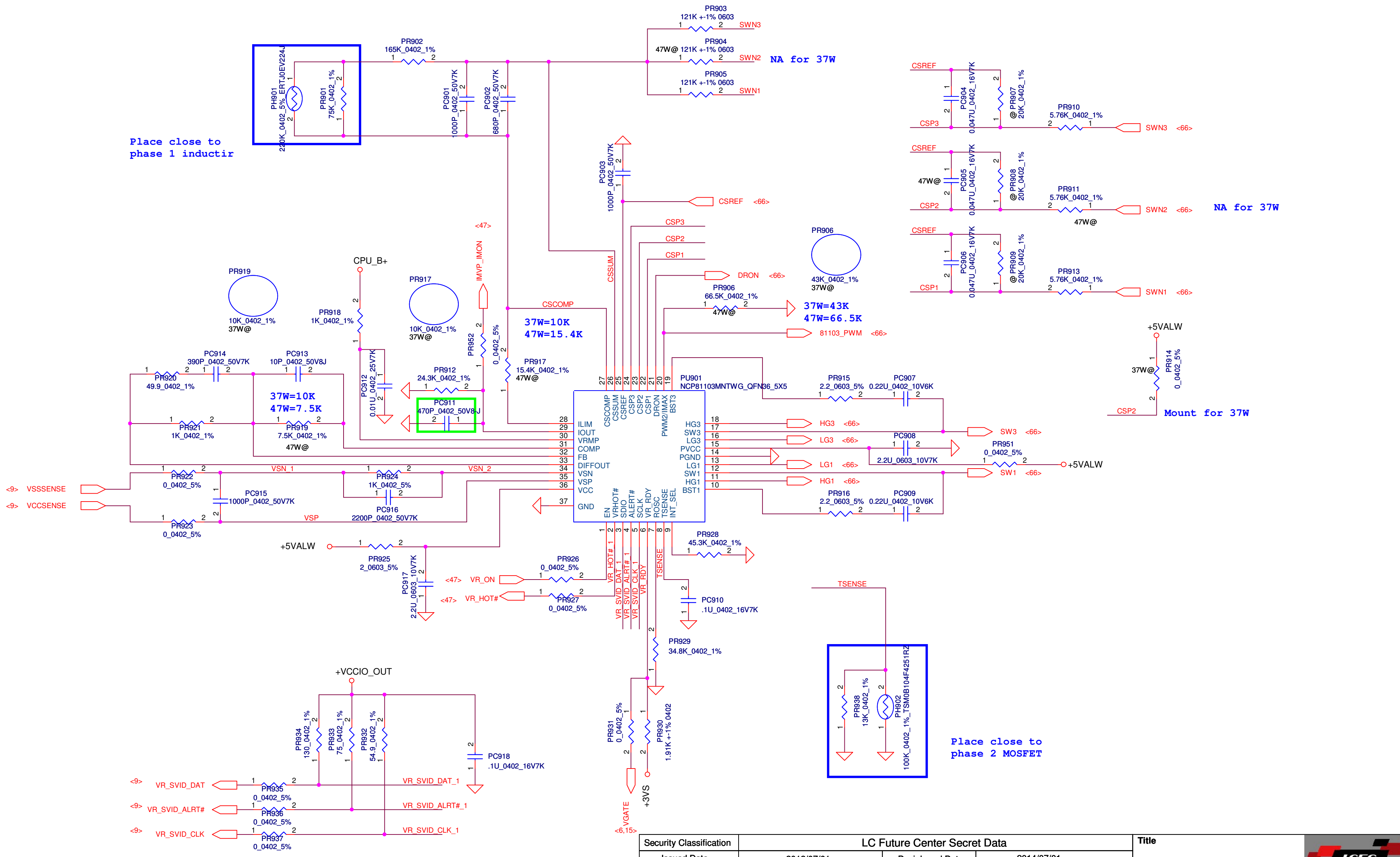
N14P-GS 25W
Ipeak=36A
Imax=25A
Iocp=64.8A
Fsw=450KHz
bulk cap 330uF 9m *3

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
VGA_CORE

Size Custom
Document Number
Y410 NM-A031
Rev 1.0

Date: Wednesday, March 27, 2013



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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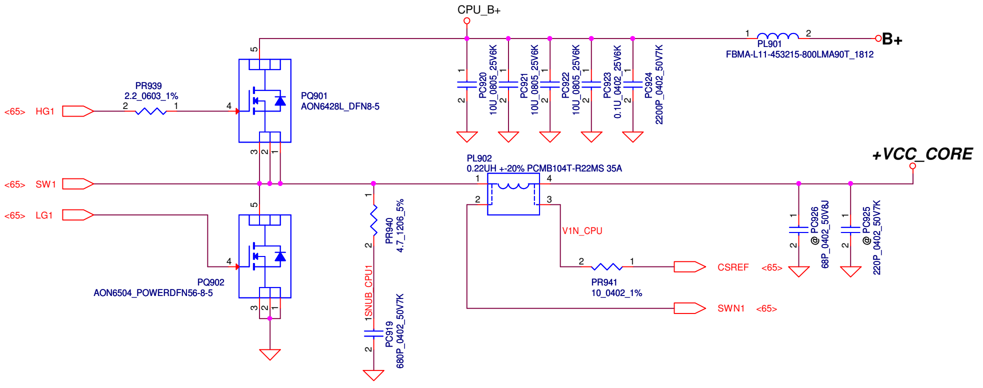
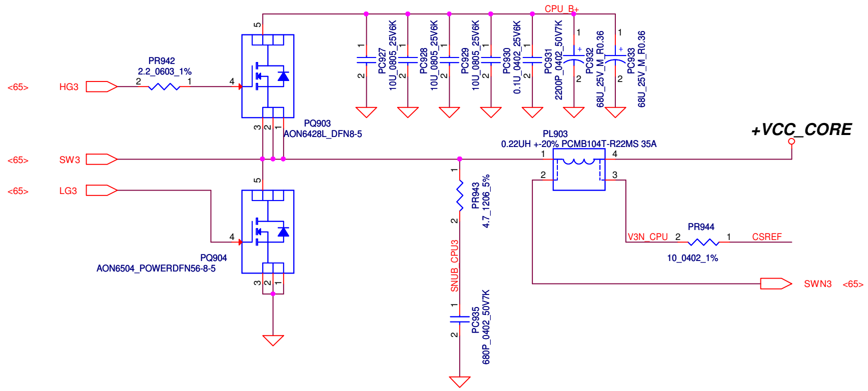
Title
CPU_CORE

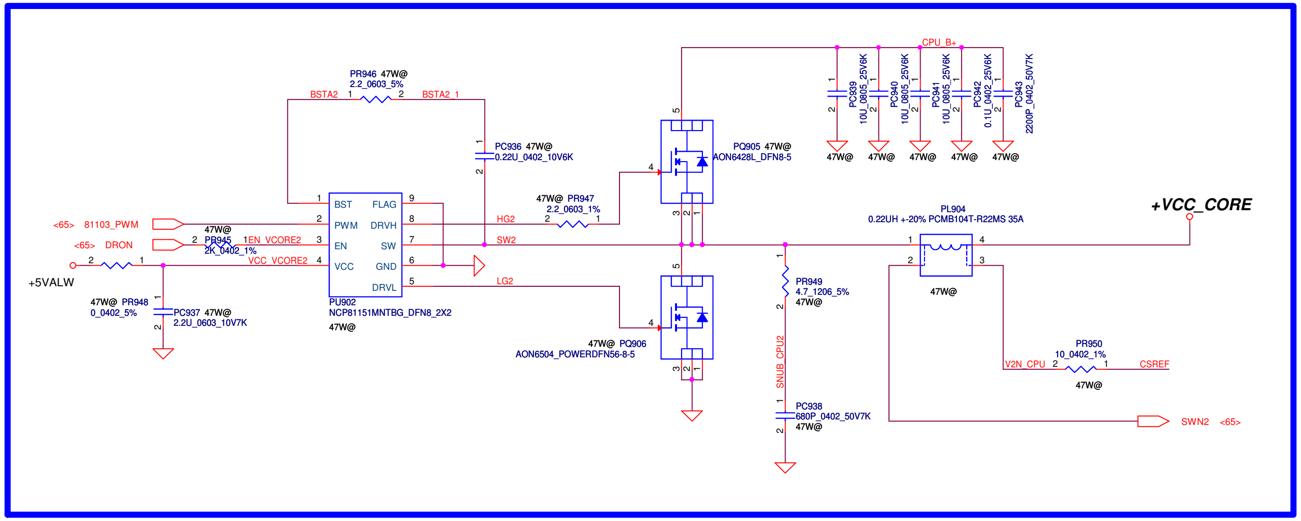
LCFC

Size	Document Number	Rev
Custom	Y410 NM-A031	1.0

Date: Wednesday, March 27, 2013 Sheet 64 of 69





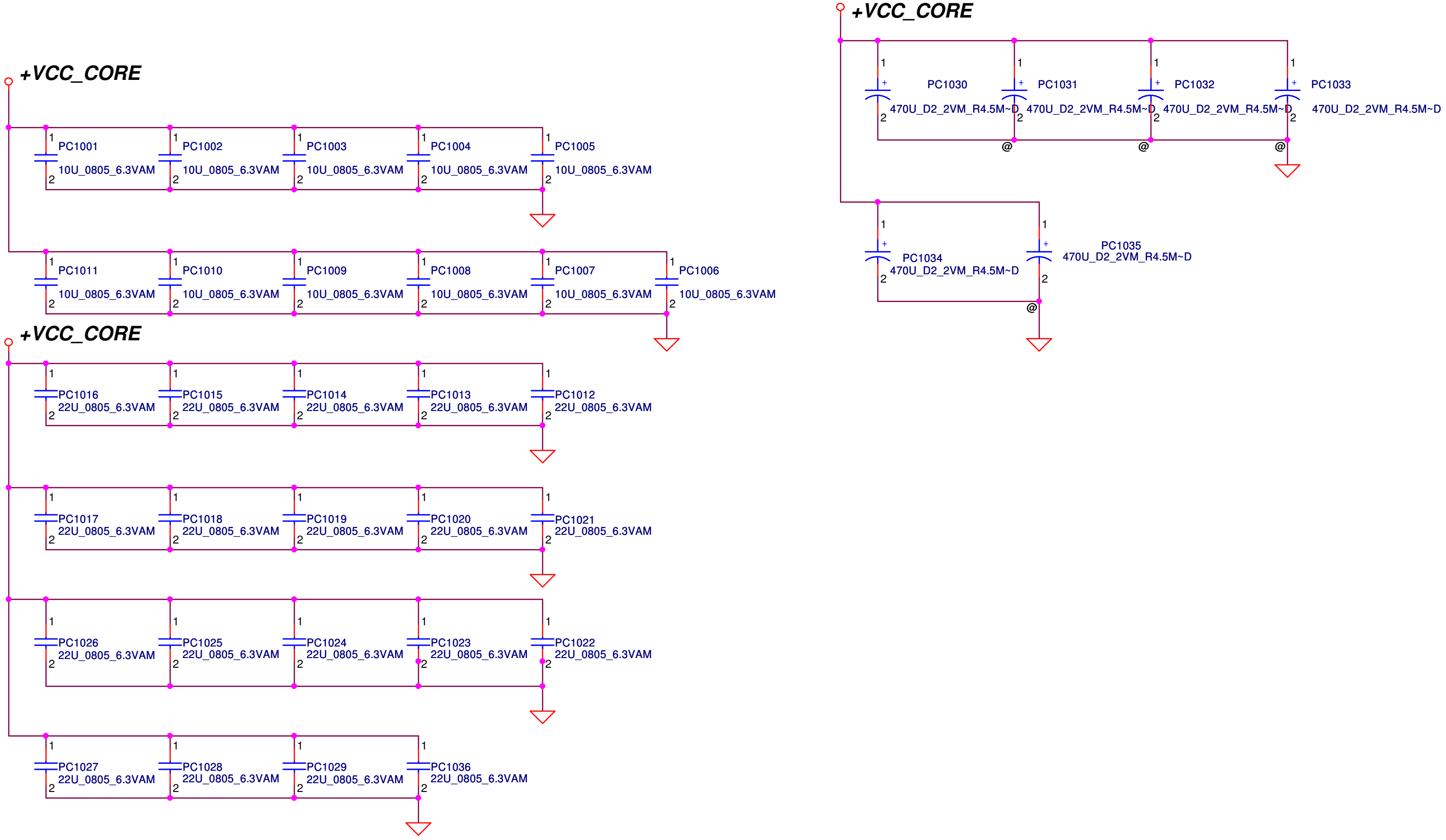


Mount for 47W

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
CPU_CORE
LCFC
Size Document Number
Y410 NM-A031
Rev 1.0
Date: Wednesday, March 27, 2013

Based on PDDG rev 0.7 Table 5-1.



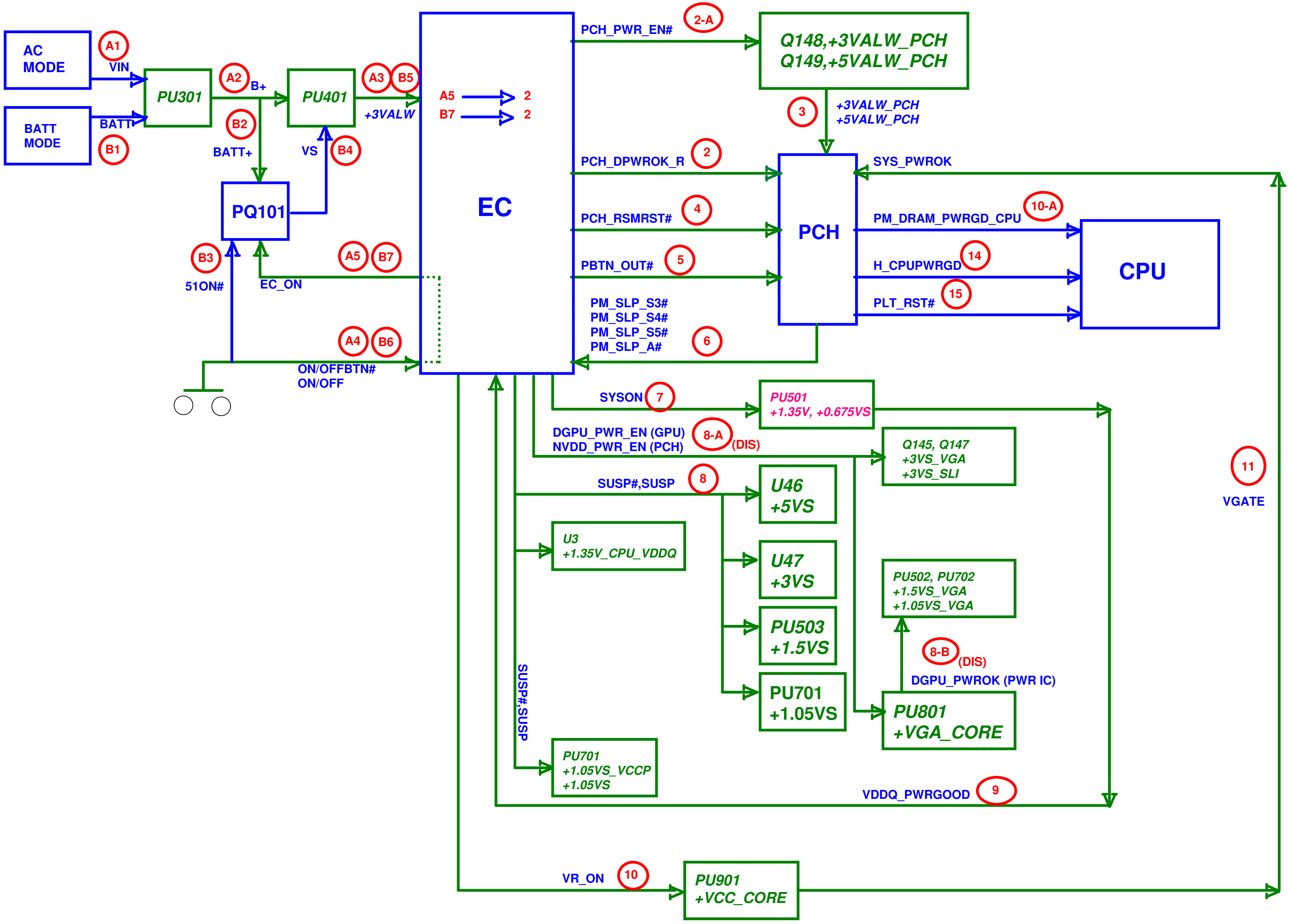
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
PROCESSOR DECOUPLING

LCFC

Size
Custom
Document Number
Y410 NM-A031
Rev
0.1

Date: Wednesday, March 20, 2013



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
Power Sequence
Size
Document Number
Y401 NM-A031
Rev
1.0
Date: Wednesday, March 27, 2013
Sheet 67 of 70

HW PIR (Product Improve Record)

QIQY5 LA-8691P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2012/03/09

NO	DATE	PAGE		MODIFICATION LIST	PURPOSE
01)	03/14	10	R64	Change R64 BOM structure from "@" to "DS3@"	For Deep S3 Function

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
HW-PIR

Size Custom
Document Number
Y490-LA8691P
Rev 1.0

Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1		51		201109/27	B test
2				201109/27	B test
3		51		201109/27	B test
4		53		201109/27	B test
5		56		201109/27	B test
6		56		201109/27	B test
7		57		201109/27	B test
8		55/58		201109/27	B test
9		59		201109/27	B test
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title
PIR (PWR)

Size: Custom
Document Number: Y490-LA8691P
Rev: 1.0

Date: Wednesday, March 27, 2013
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