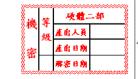
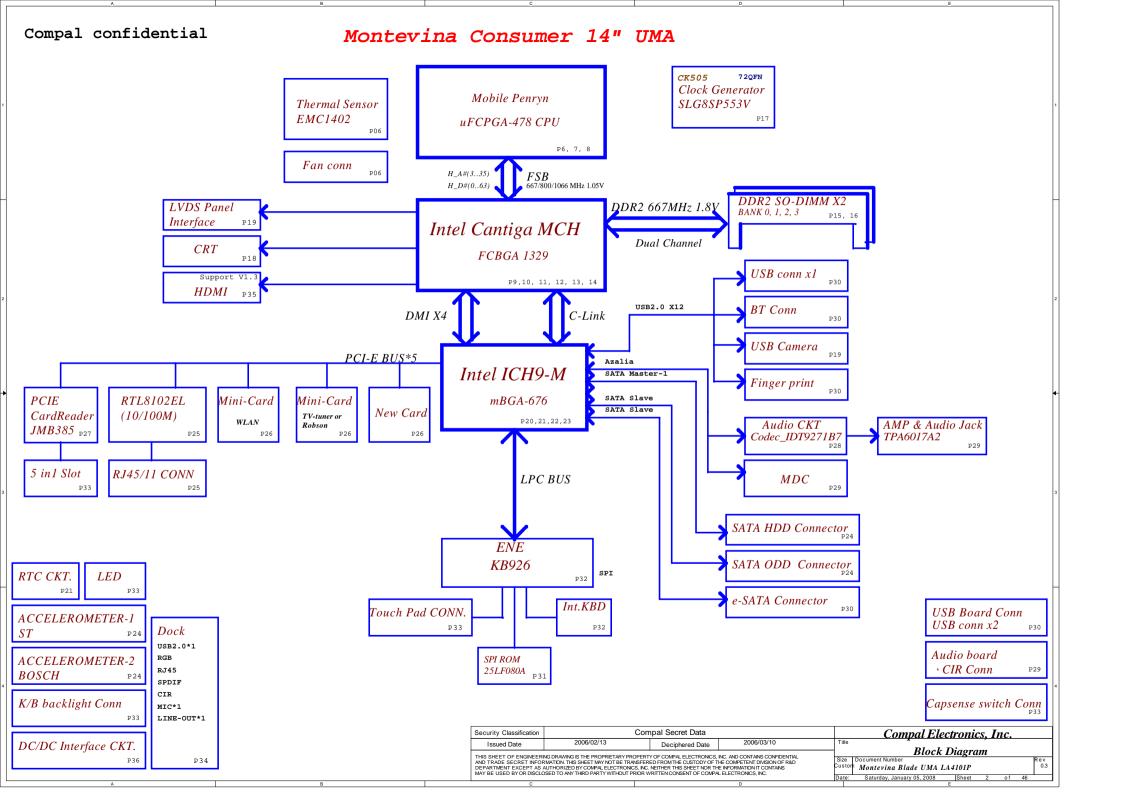
Compal confidential

Schematics Document
Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M core logic

2008-01-01



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Voltage Rails O MEANS ON X MEANS OFF power plane +5VALW +B +1.8V +5VS +3VS +3VALW +1.5VS +0.9V State +VCCP +CPU_CORE +2.5VS +1.8VS S0 0 0 0 0 S1 0 0 0 0 S3 X 0 0 0 S5 S4/AC X X 0 0 S5 S4/ Battery only 0 X X X S5 S4/AC & Battery don't exist X X X X

Symbol Note:



@:	means just reserve , no build
45@:	means need be mounted when 45 level assy or rework stage.
DEBUG@:	means just reserve for debug.
BATT @:	means need be mounted when 45 level assy or rework stage.
CONN@:	means ME part
ESATA @:	means just reserve for ESATA
GS @:	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @:	means just reserve for Multi Bay
NewC@:	means just reserve for New card
DOCK@:	means just reserve for Docking
Main@:	means just reserve for Main stream
OPP@:	means just reserve for OPP
2MiniC@:	means just reserve for 2nd Mini card slot
-	· · · · · · · · · · · · · · · · · · ·

USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	Dock
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCle assignment:

	TV /WWAN/Robeson
PCIe-2	
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	Card reader
PCIe-6	New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	Х	V	V	Х	Χ	Х	Х	Х	V	Х	Х
SMB_EC_CK2 SMB_EC_DA2	KB926	Х	Х	Х	V	Χ	Х	Х	X	Х	Х	Х
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	Х	Х	Х	Х	V	V	V	Х	Х	V	V
LCD_CLK LCD_DAT	Cantiga	Х	Х	Х	Х	Х	Х	Х	V	Х	Х	Х

43154432L01: Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/Multi@/2MiniC@

43154432L02: Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/2MiniC@

43154432L03: Main@/DEBUG@/DOCK@/NewC@/FP@/2MiniC@

43154432L04 : OPP@/DEBUG@ 43154432L05 : OPP@/DEBUG@

12C / SMBUS ADDRESSING

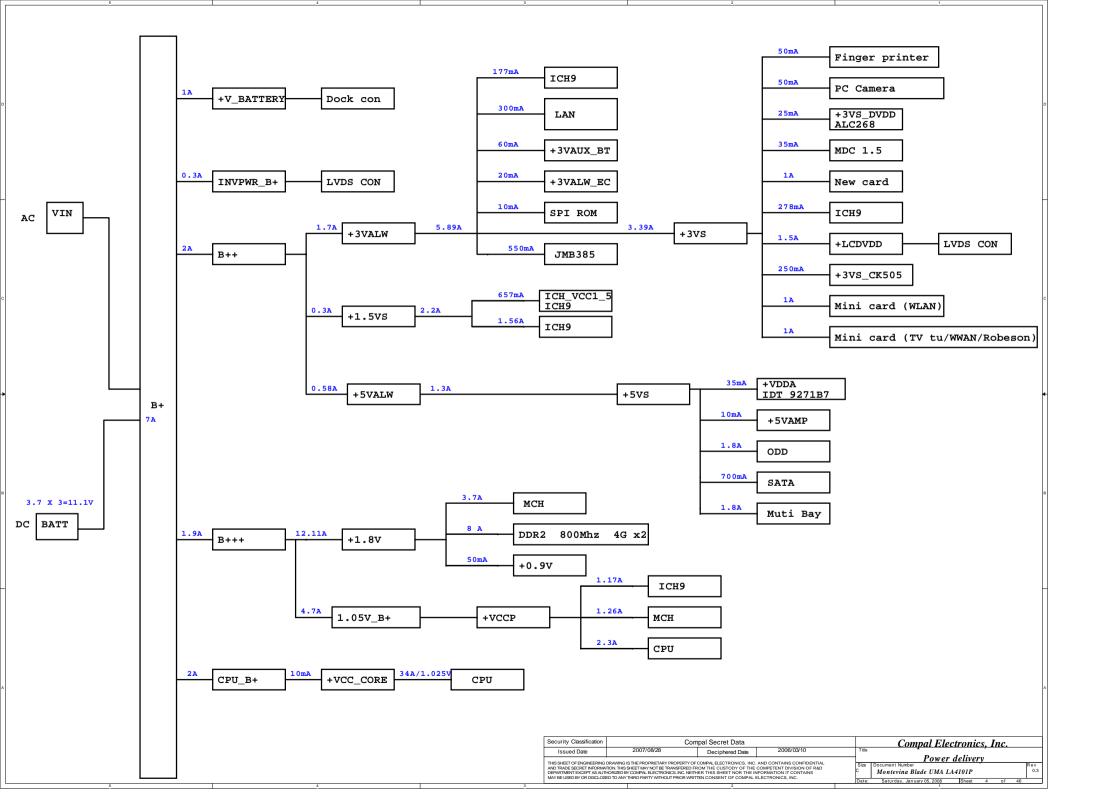
DEVICE	HEX	ADDRESS	
DDR SO-DIMM 0	A0	10100000	
DDR SO-DIMM 1	A4	10100100	
CLOCK GENERATOR (EXT.)	D2	11010010	

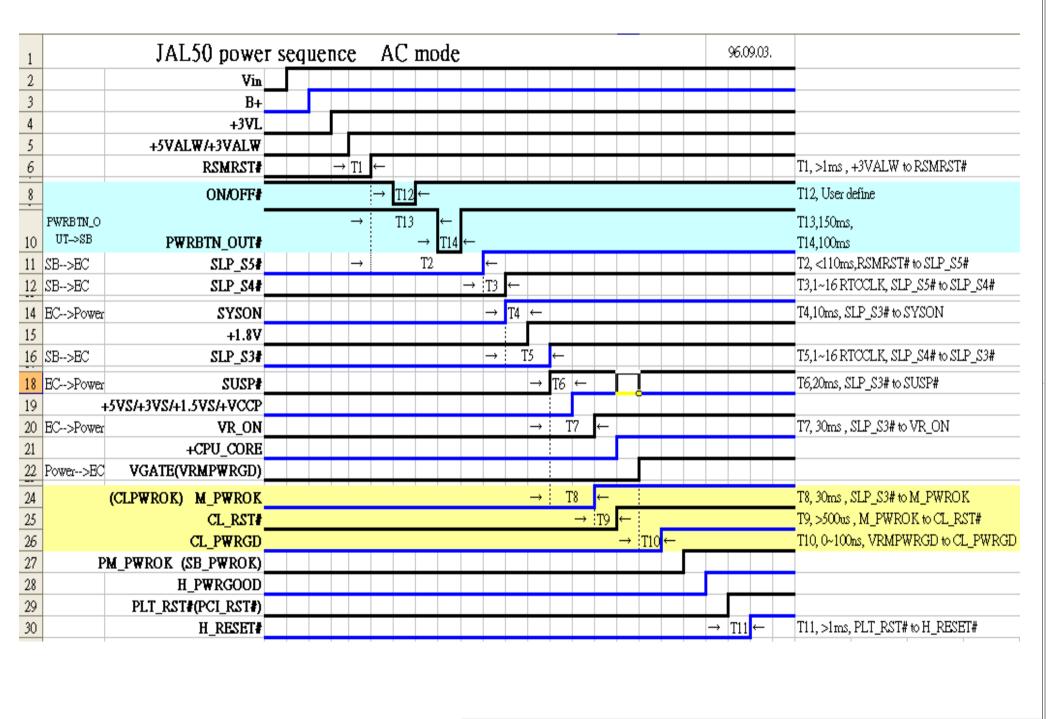
43154432L01: UMA GM PA FF (SI-1) 43154432L02: UMA GM PR FF (SI-1) 43154432L03: UMA GL PR FF-43154432L04: UMA GM OPP (SI-1)

43154432L05: UMA GL OPP

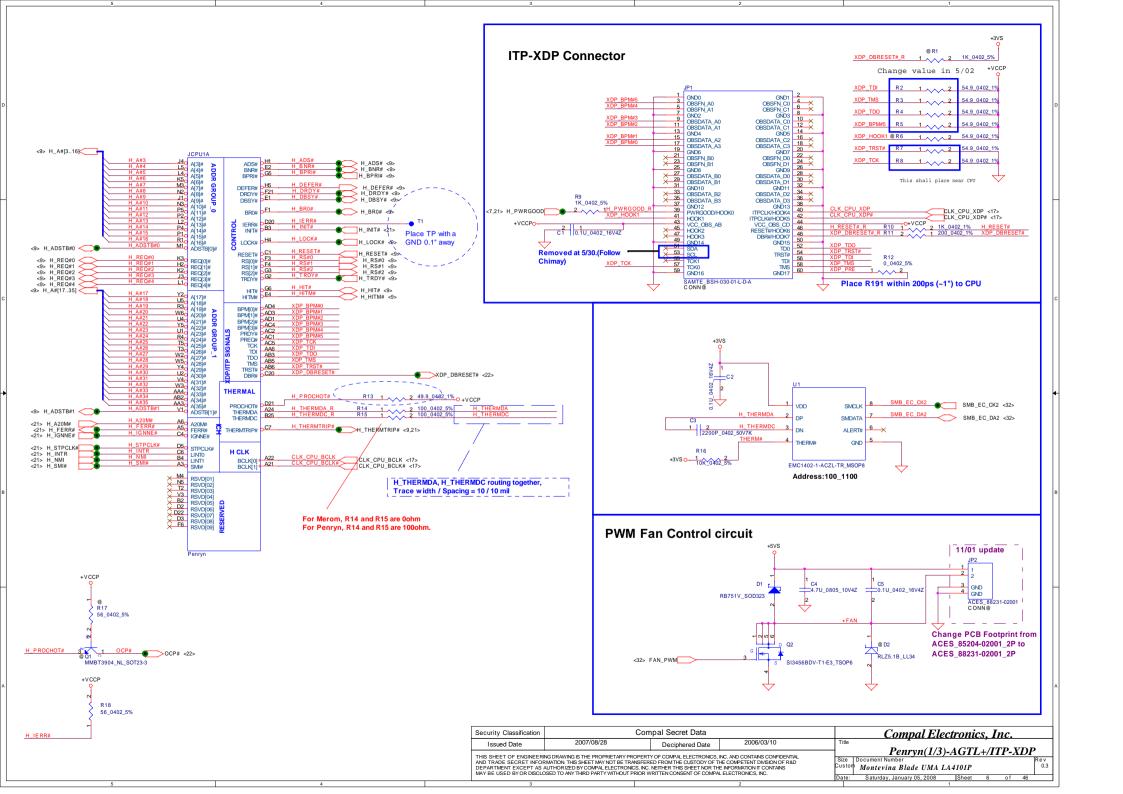
Cantiga GM45 B0(QR32): SA00001P930 ICH9M A2 ES2 Base: SA00002AN10

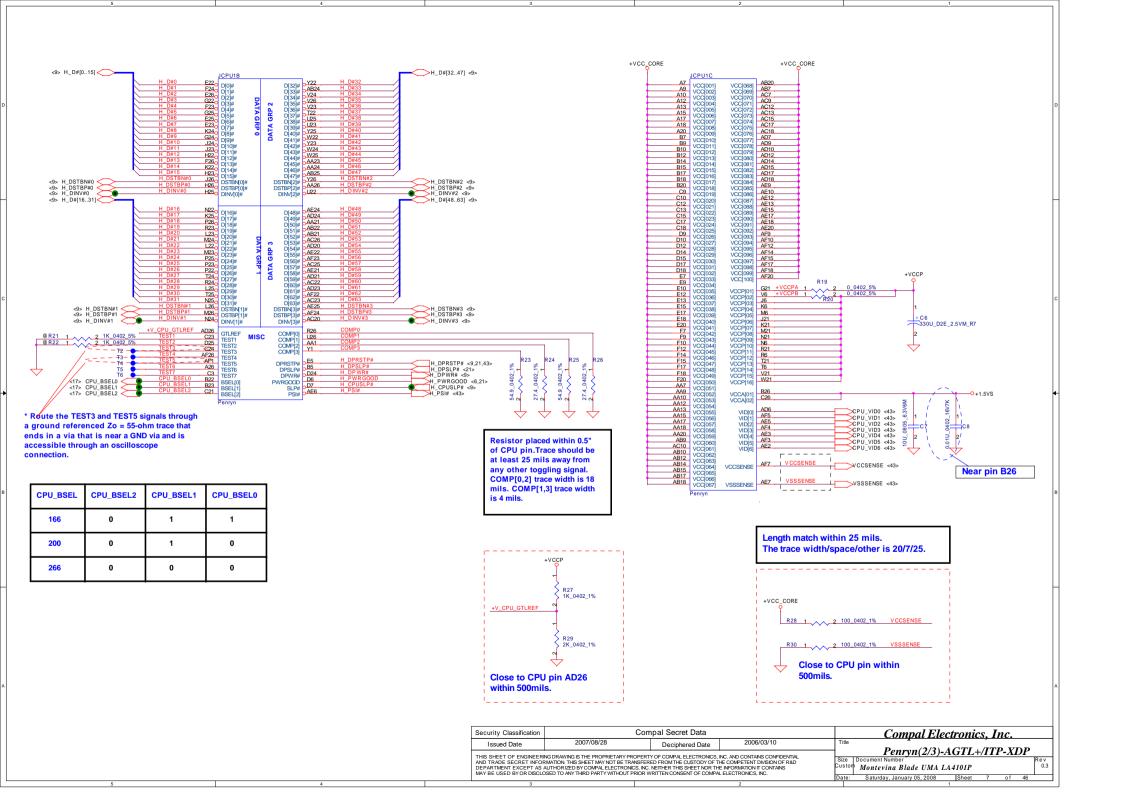
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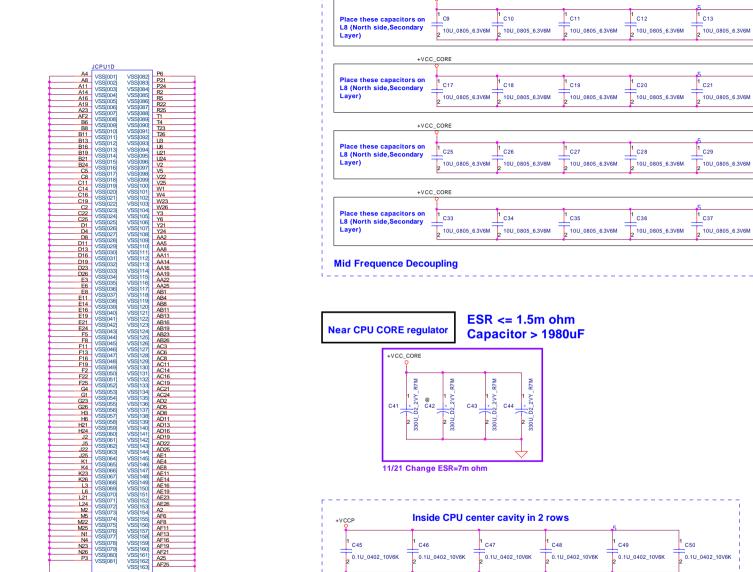




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+VCC_CORE

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AND TRADE SECRET INFOR DEPARTMENT EXCEPT AS	NG DRAWING IS THE PROPRIETARY PROPERT KMATION. THIS SHEET MAY NOT BE TRANSFER AUTHORIZED BY COMPAL ELECTRONICS, INC. ISED TO ANY THIRD PARTY WITHOUT PRIOR W	ED FROM THE CUSTODY OF T NEITHER THIS SHEET NOR TH	HE COMPETENT DIVISION OF R&D HE INFORMATION IT CONTAINS	Penryn(3/3)-AGTL+/ITP-XDP

1 C14

1 C22

1 C30

1 C38

10U_0805_6.3V6M

10U_0805_6.3V6M

C15

1 C23

1 C31

1 C39

10U_0805_6.3V6M

10U_0805_6.3V6N

10U_0805_6.3V6M 10U_0805_6.3V6M

10U_0805_6.3V6M 10U_0805_6.3V6M

C16

1 C24

1 C32

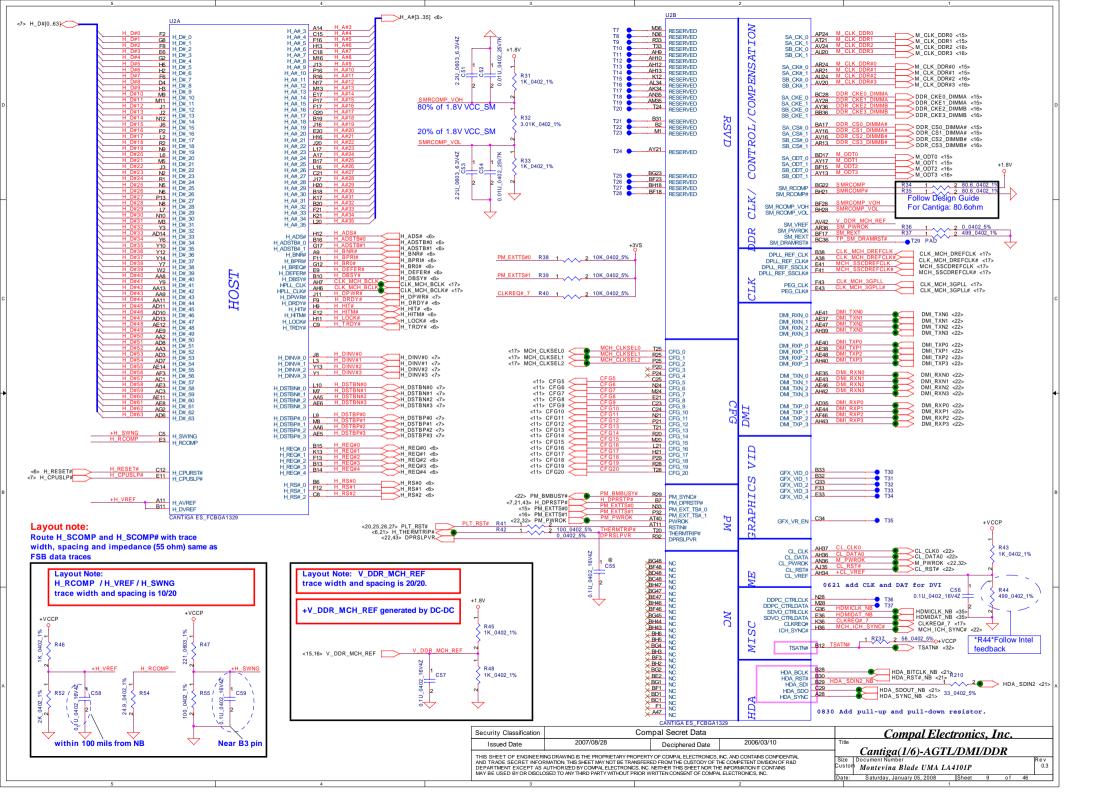
1 C40

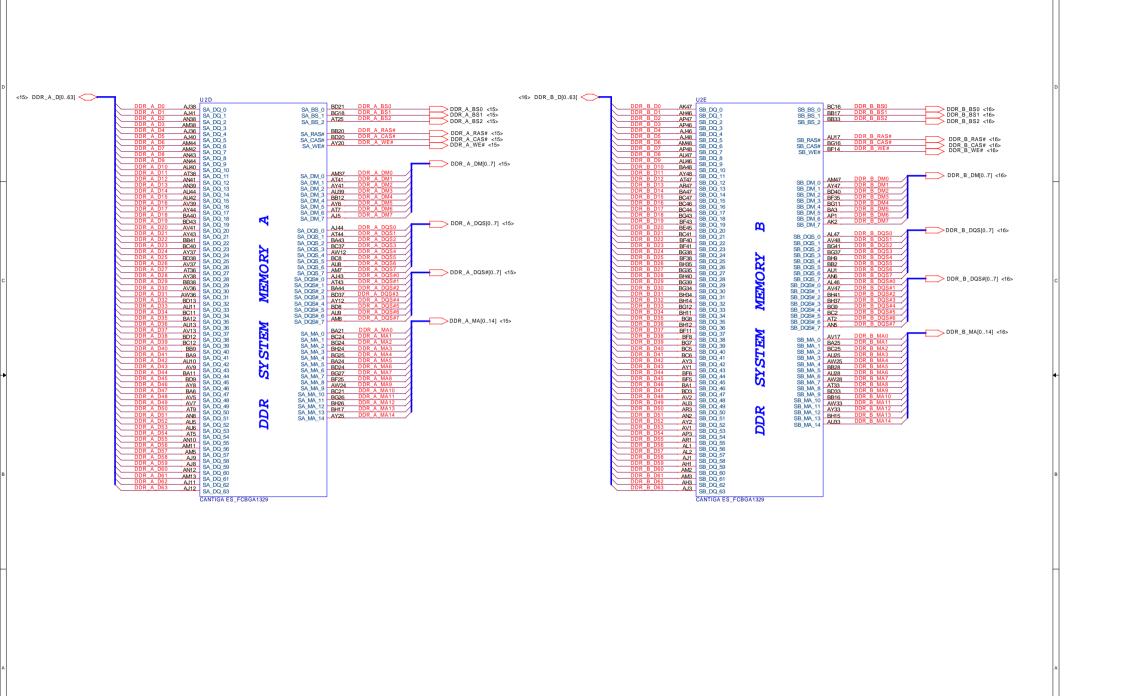
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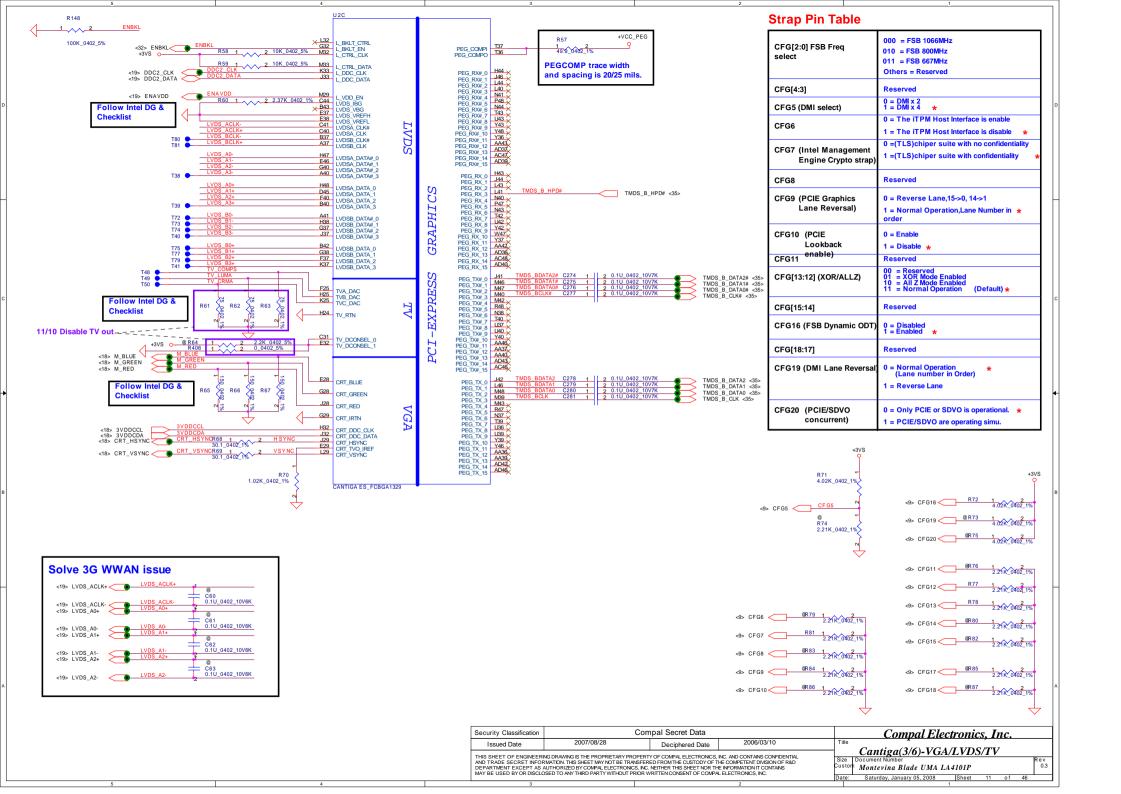
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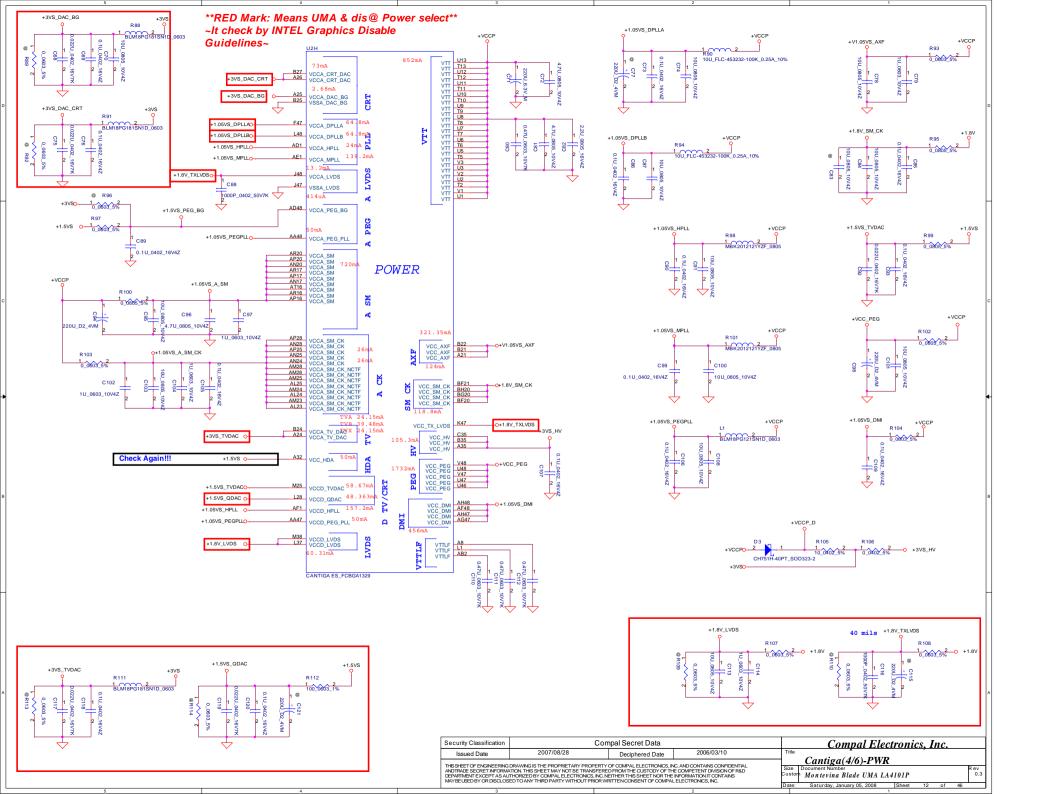
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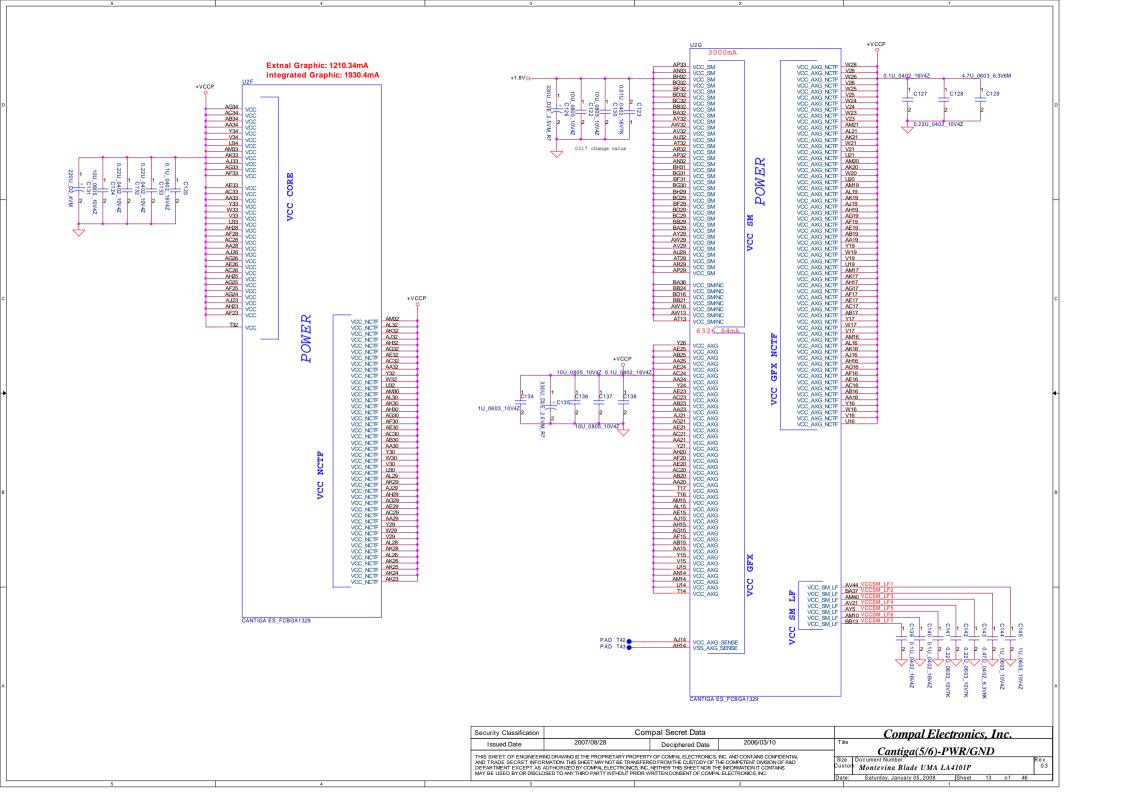


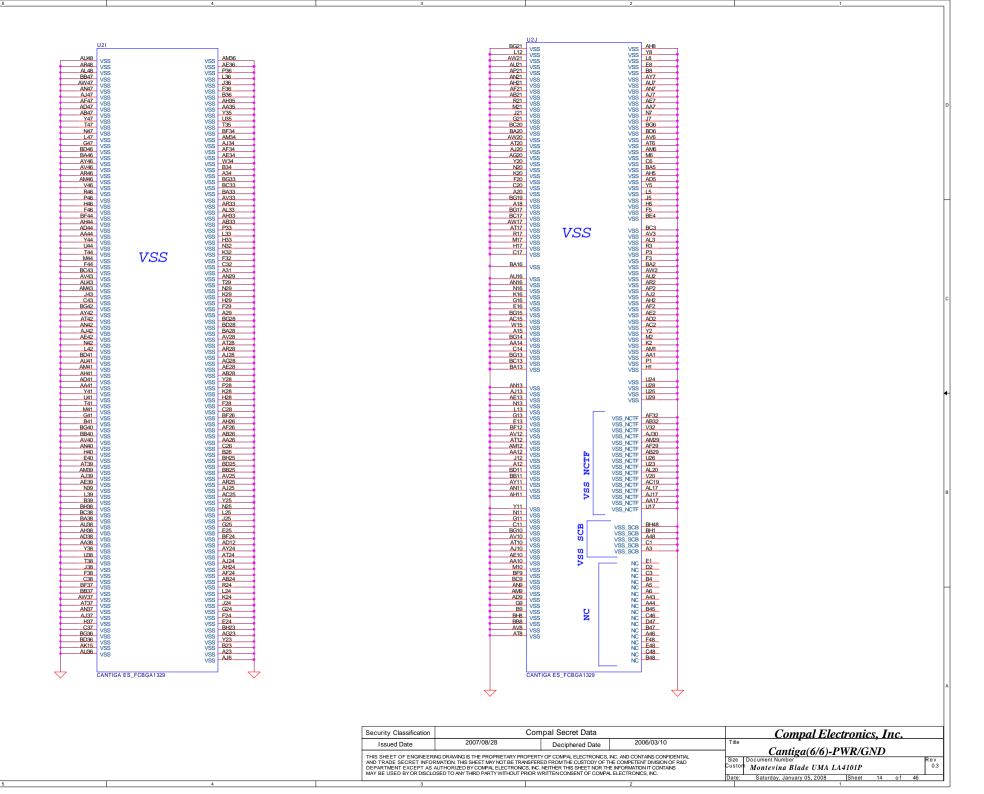


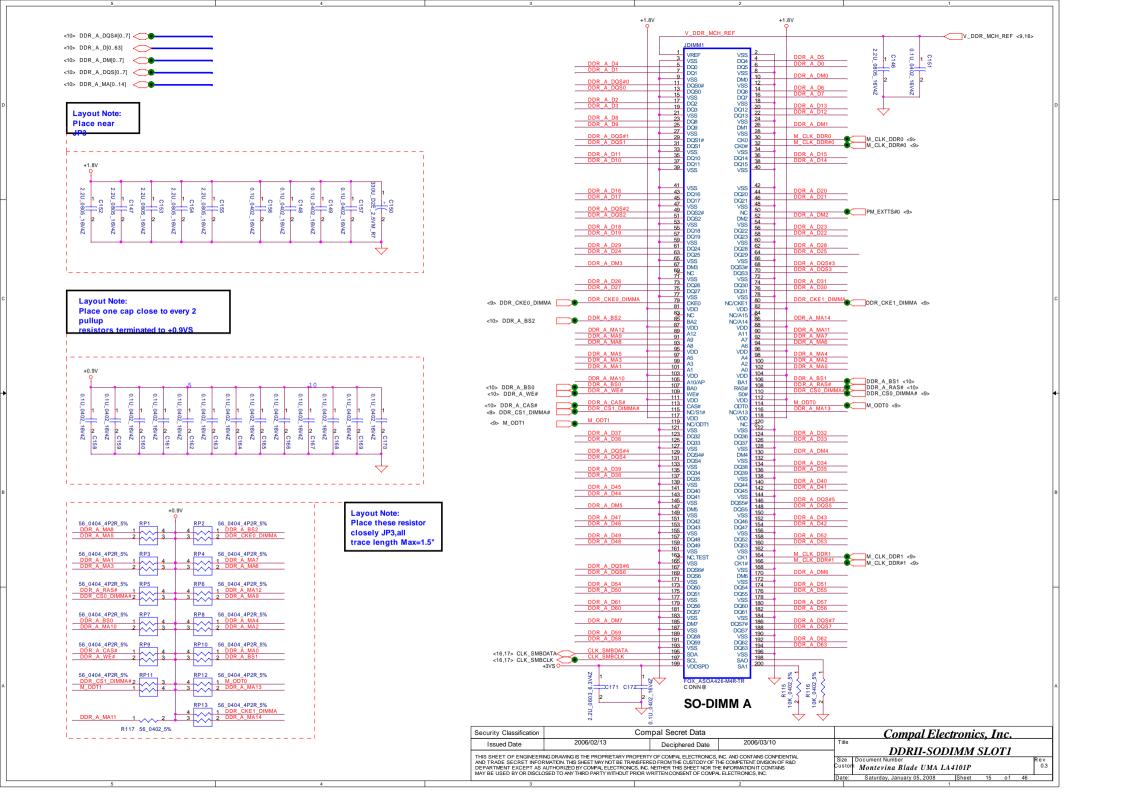
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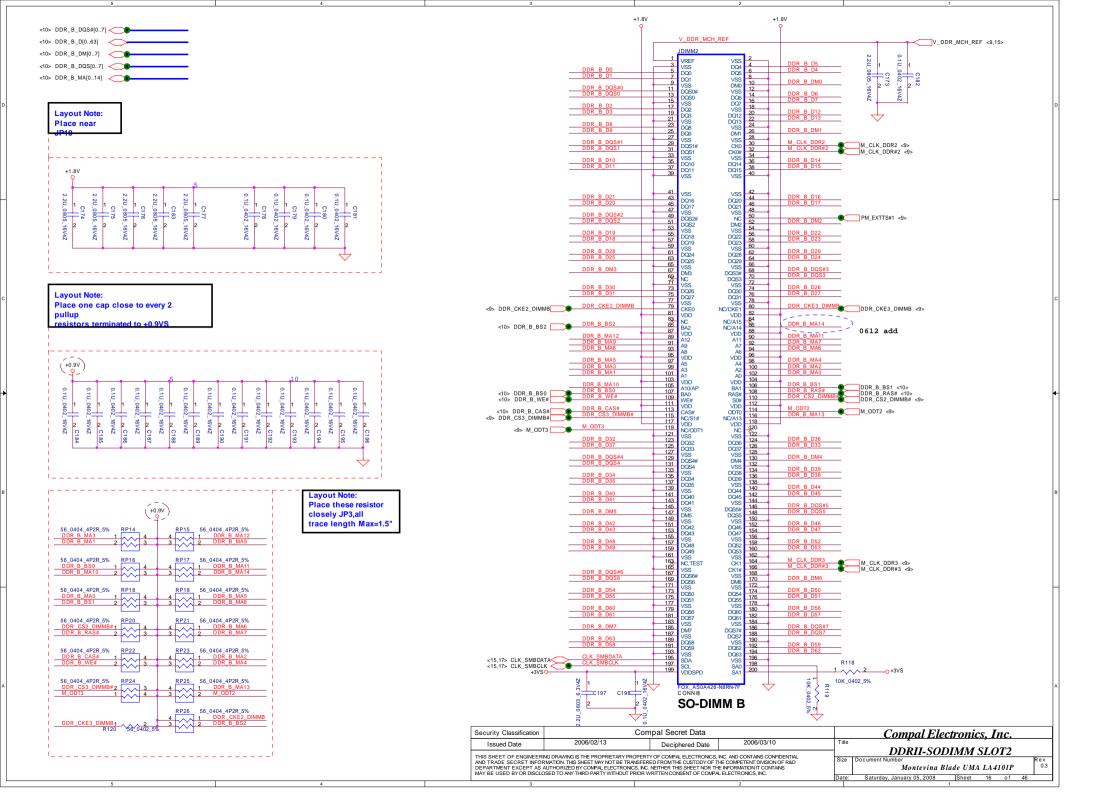


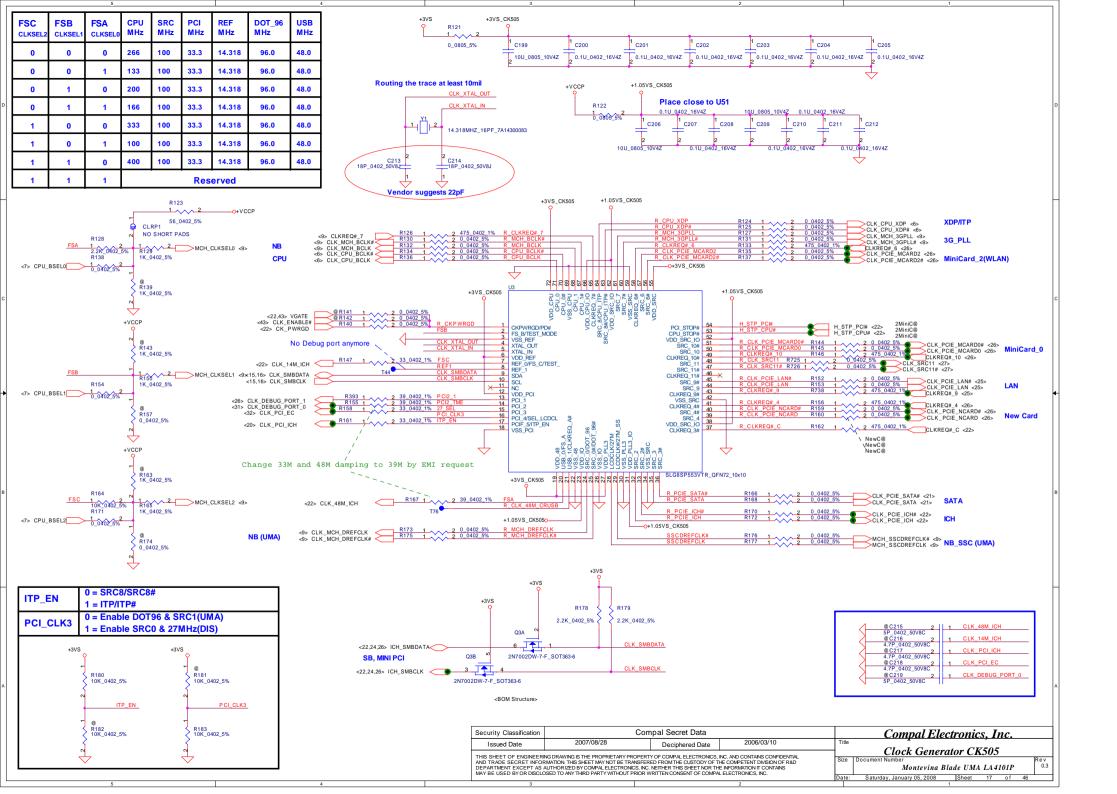


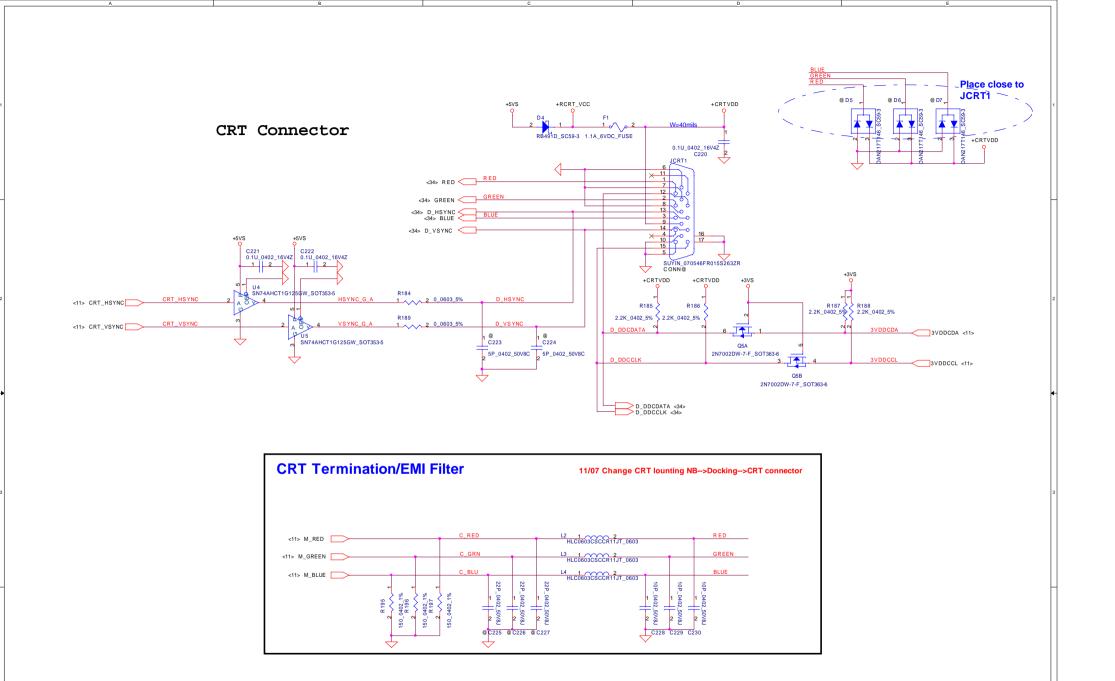




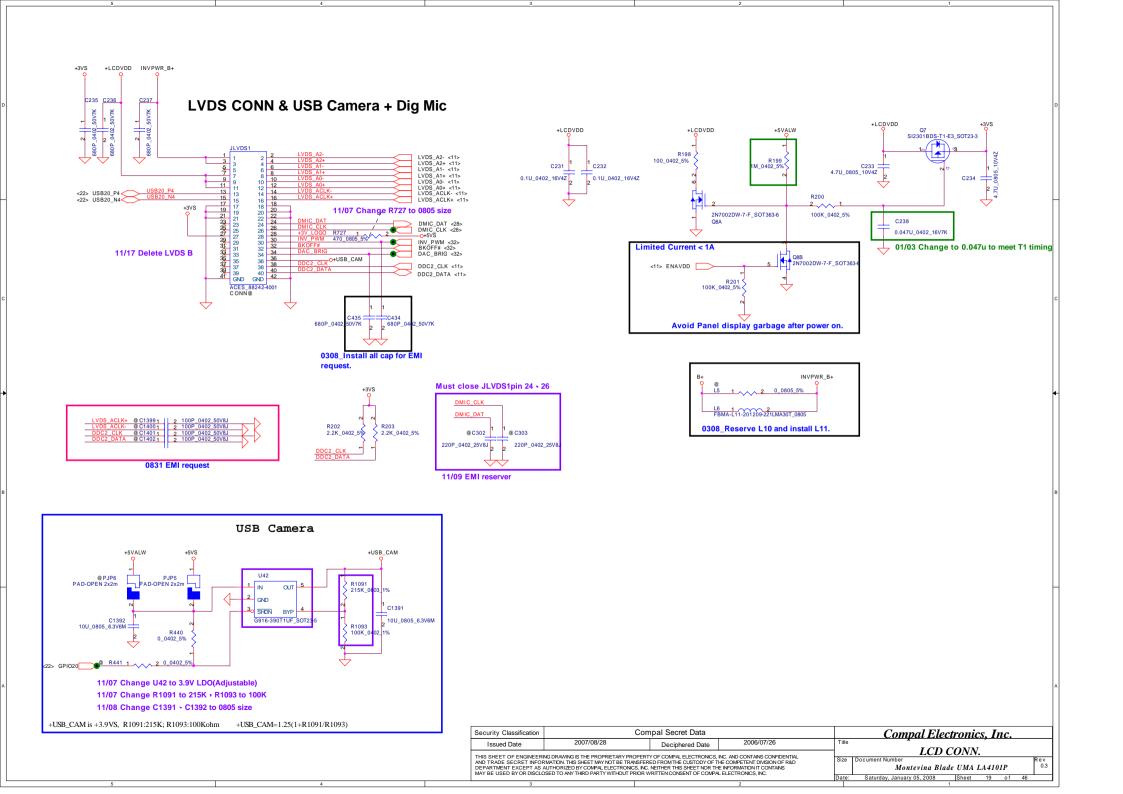


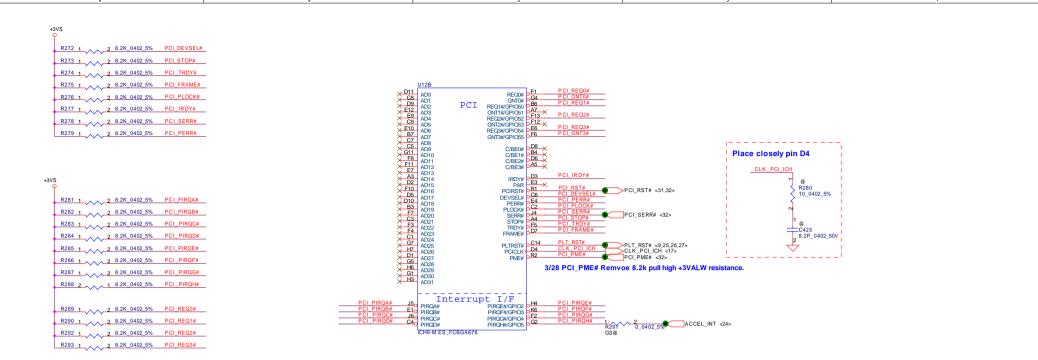


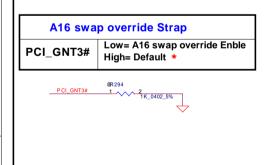




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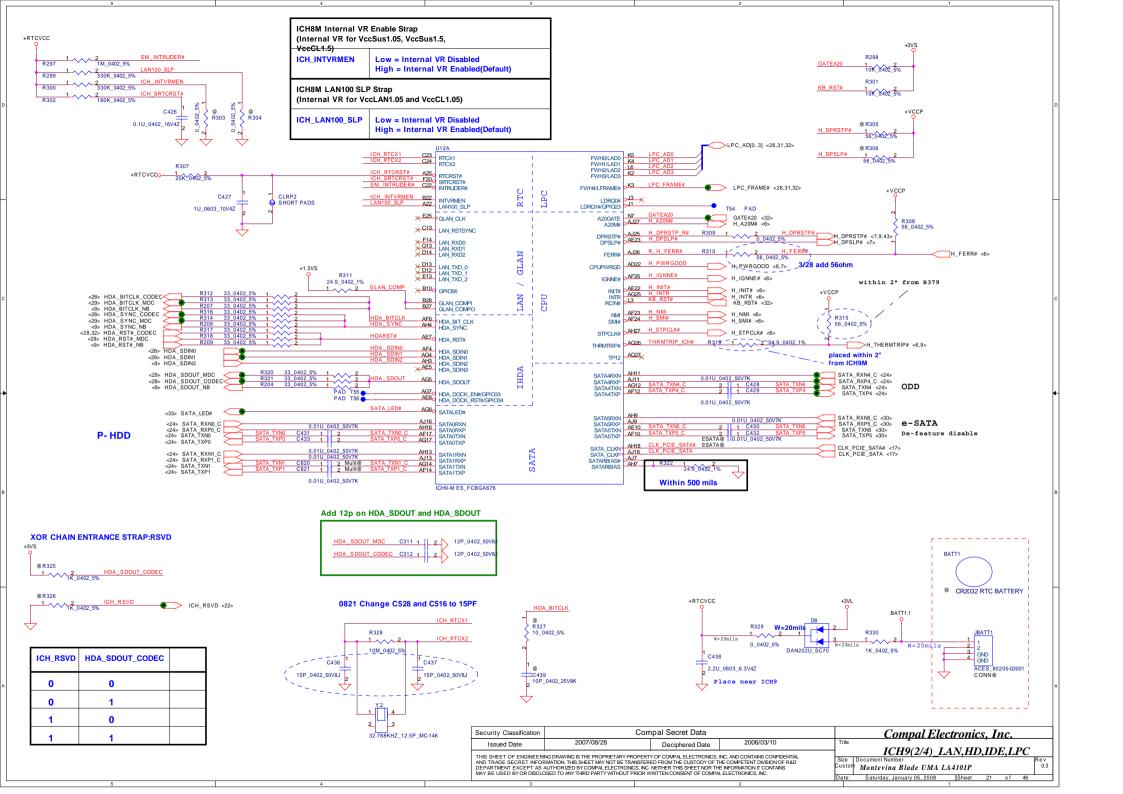


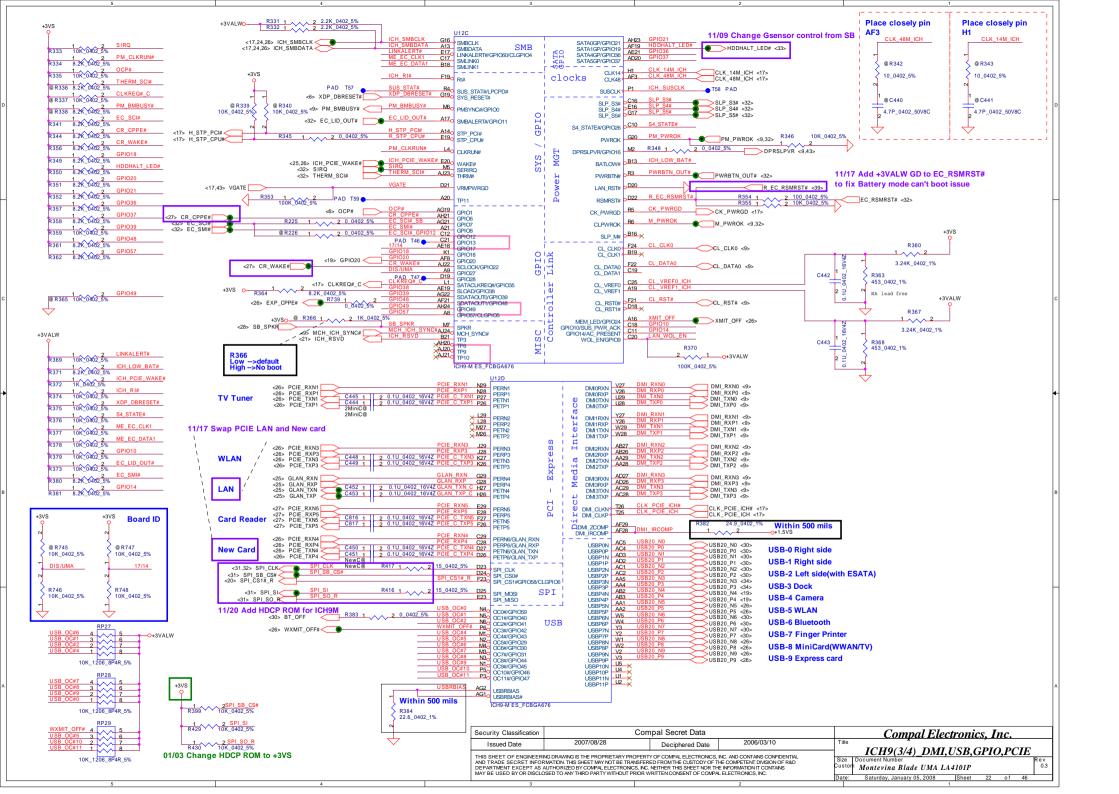


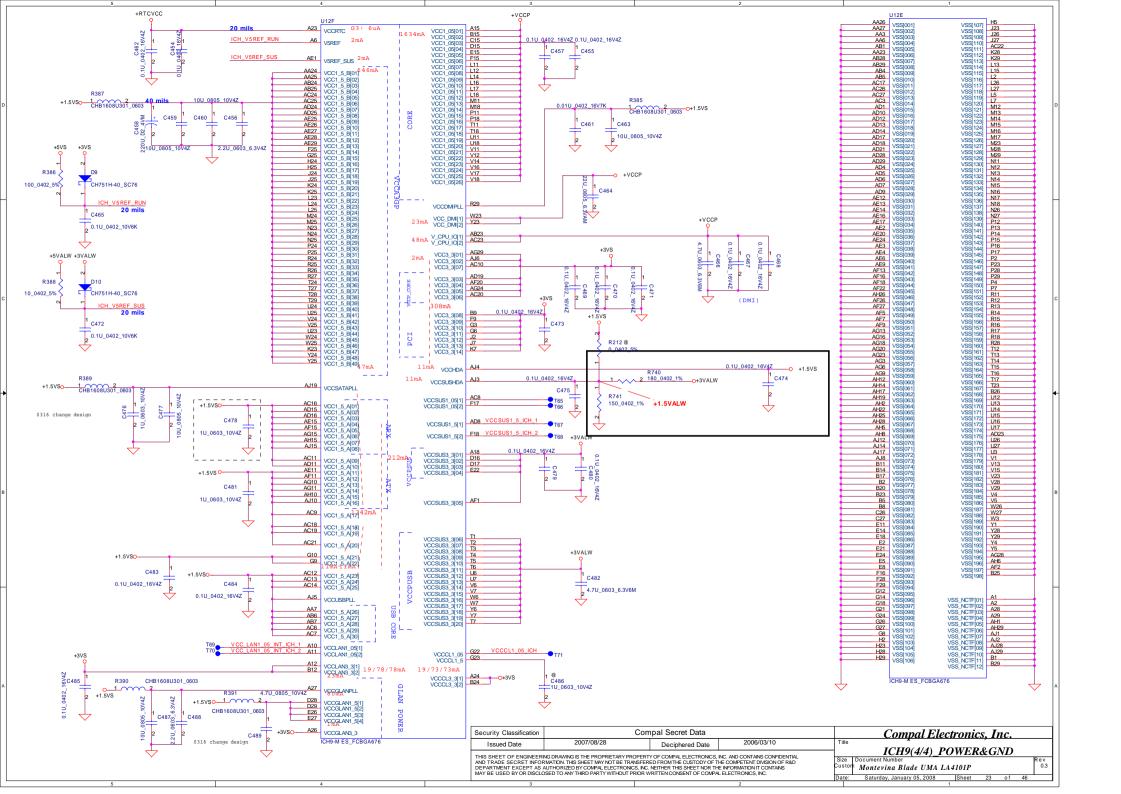


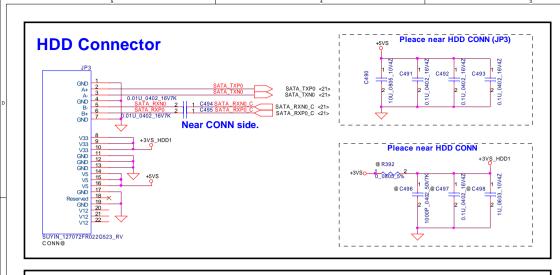
Boot BIOS Strap						
PCI_GNT0#	SPI_CS#1	Boot BIOS Location				
0	1	SPI				
1	0	PCI				
1	1	LPC *				
2> SPI_CS1#_R	SPI_CS1#_R PCI_GNT0#	#3VALW @ R295 1 K_0402_5% @ R296 1 K_0402_5%				

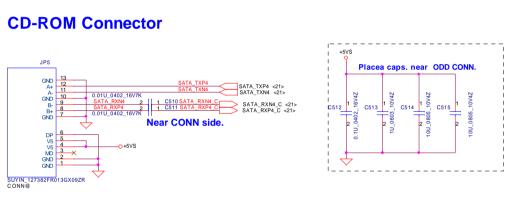
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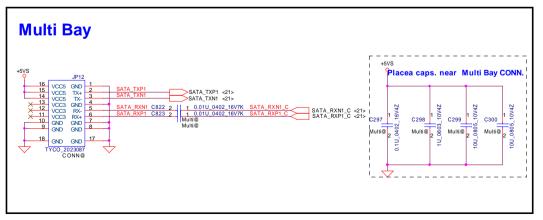


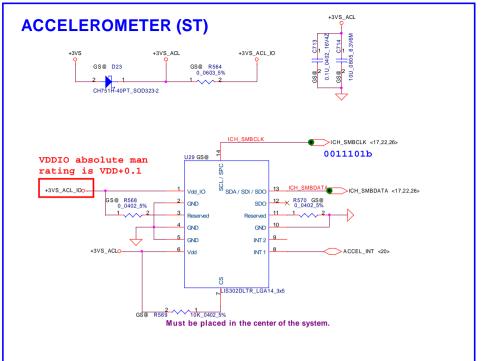


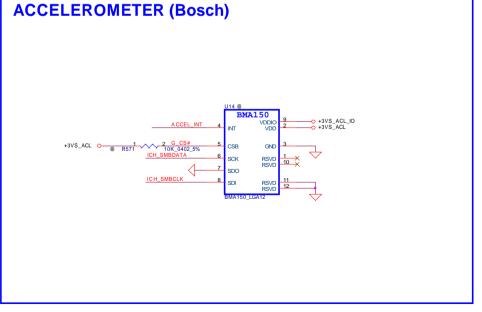






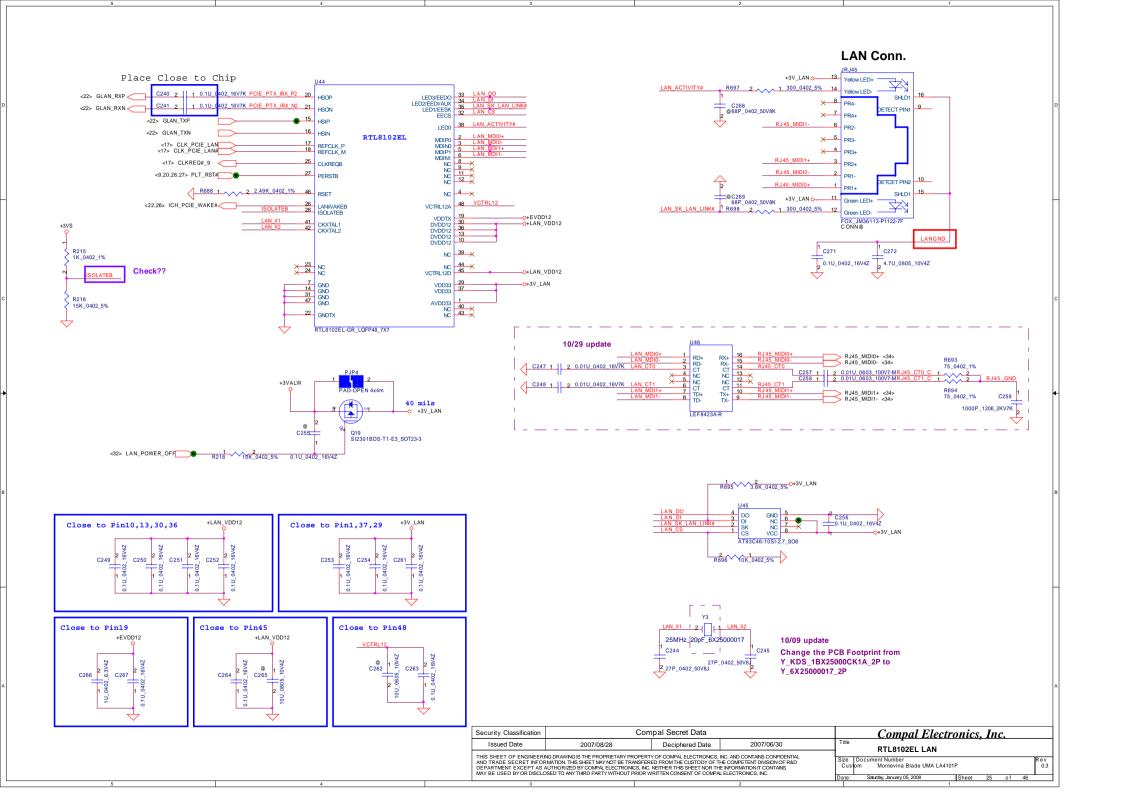


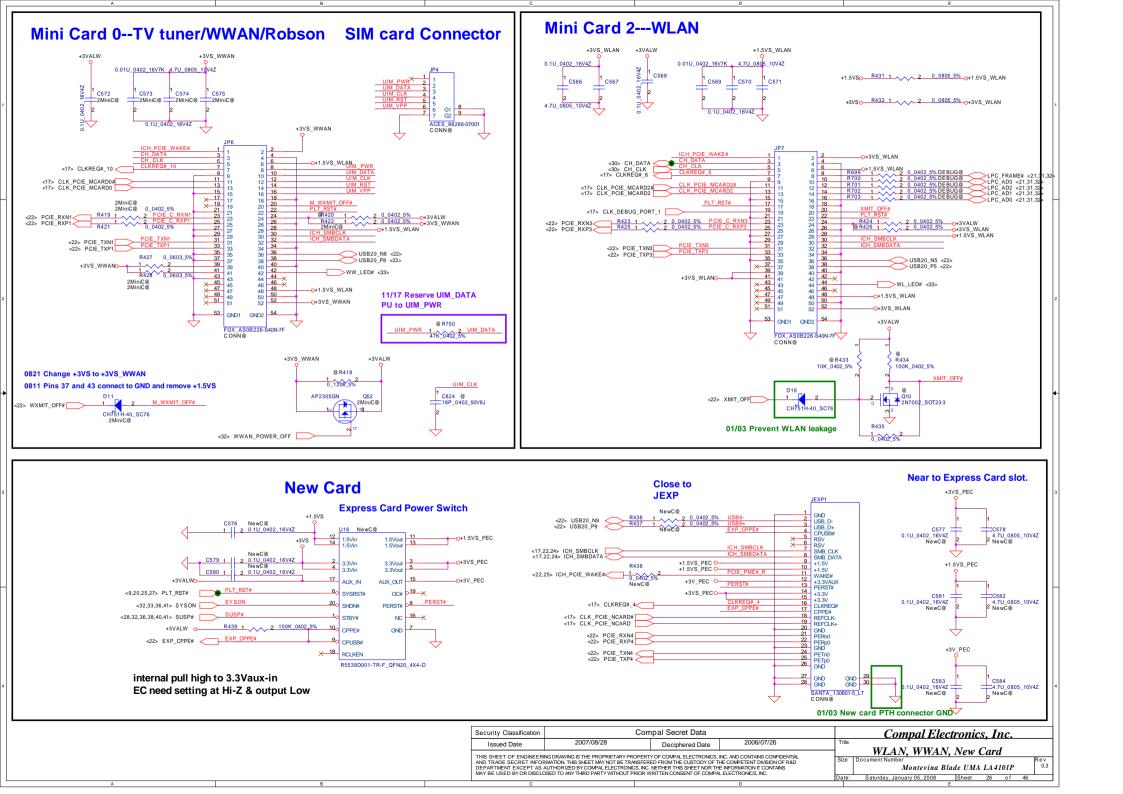


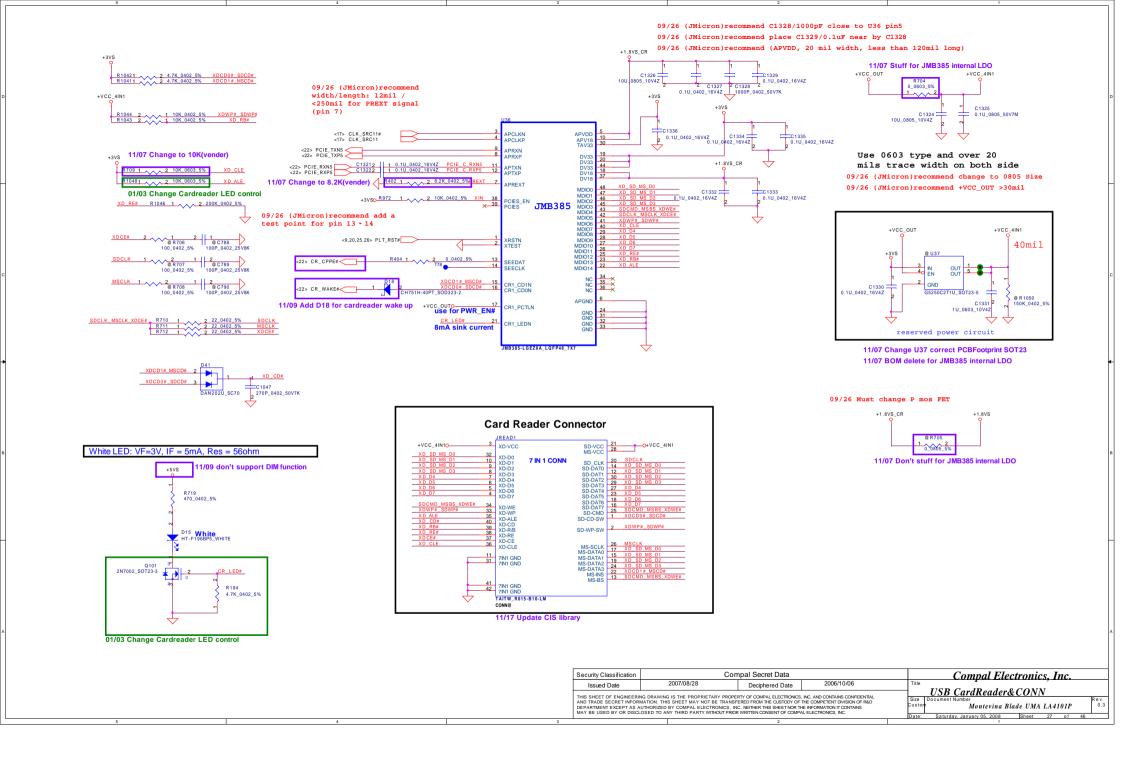


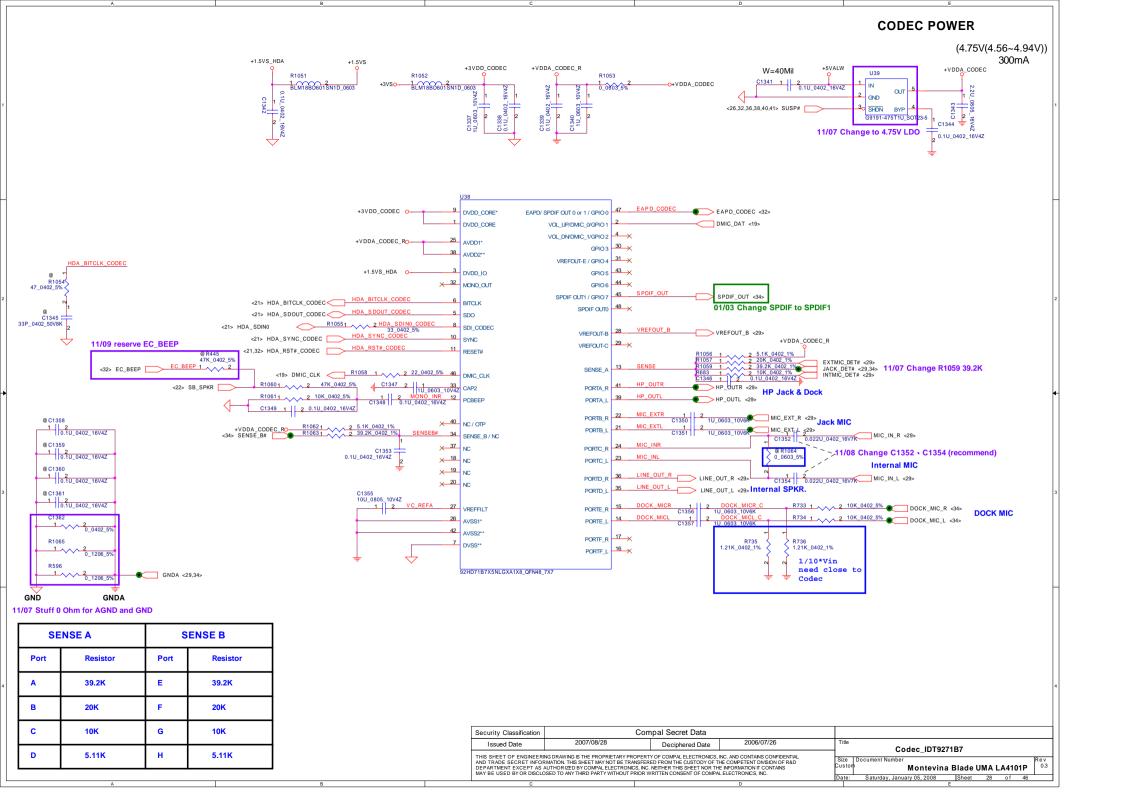


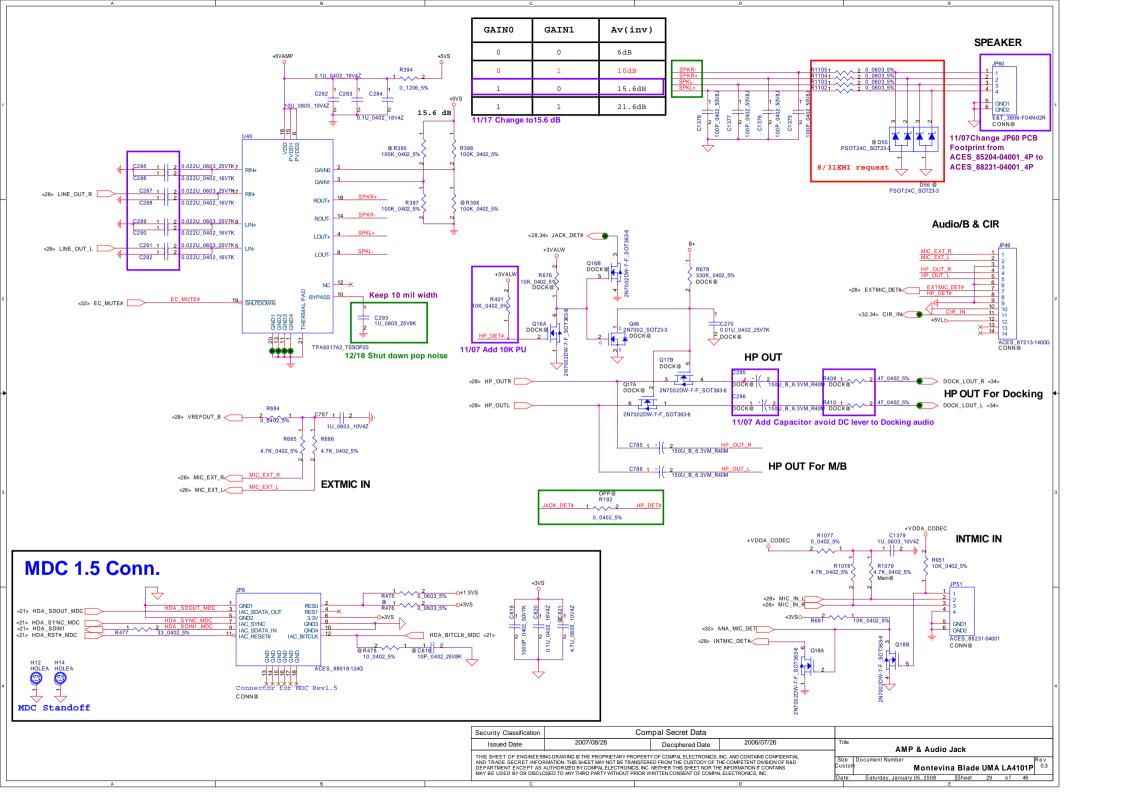
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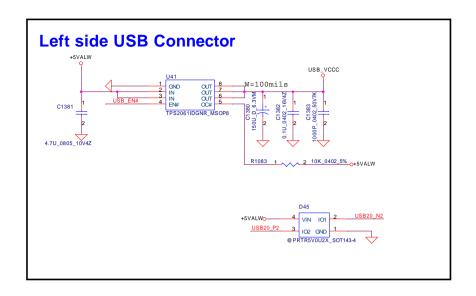


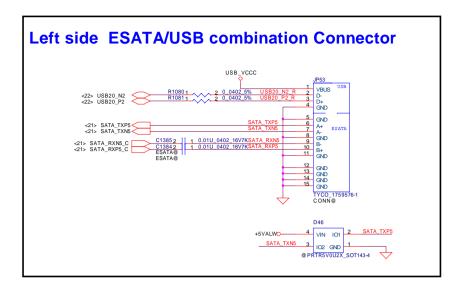


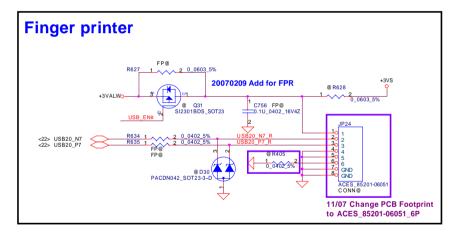


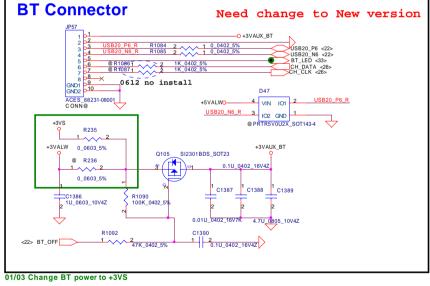


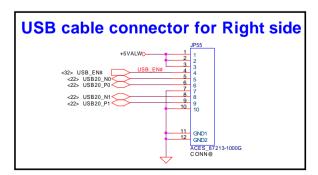




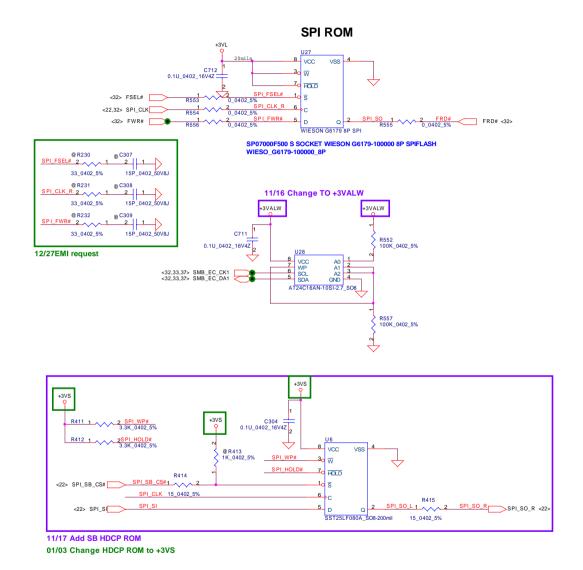


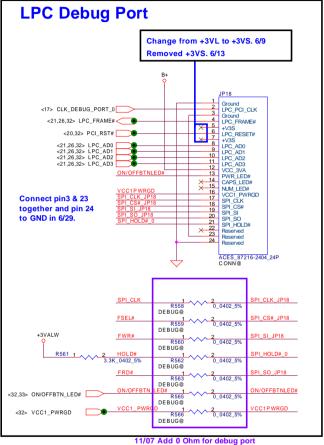




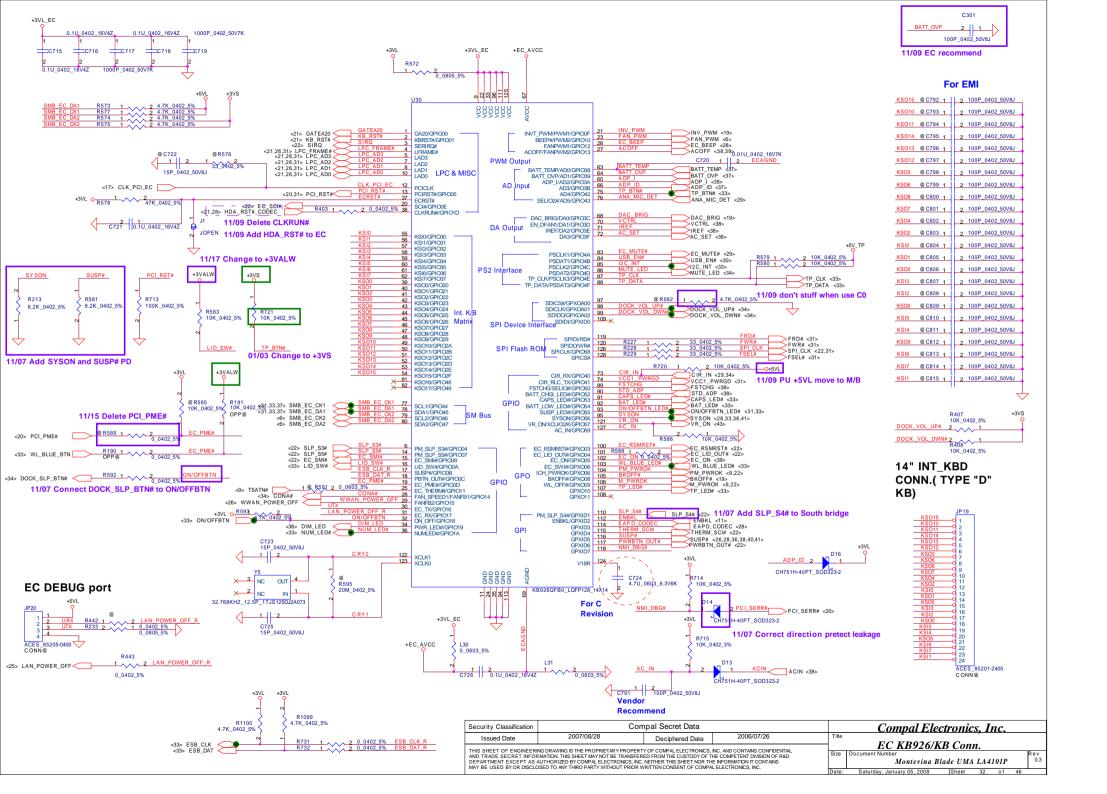


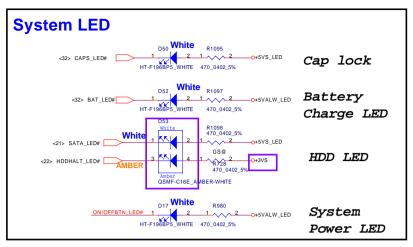
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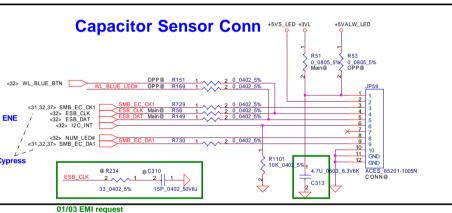


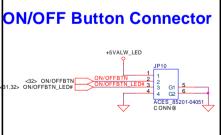


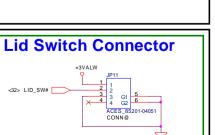
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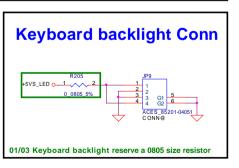




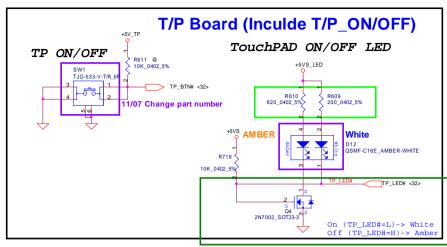


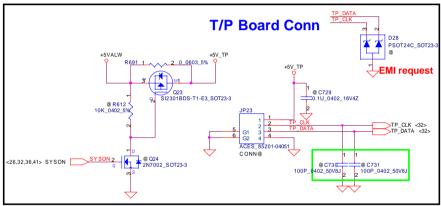


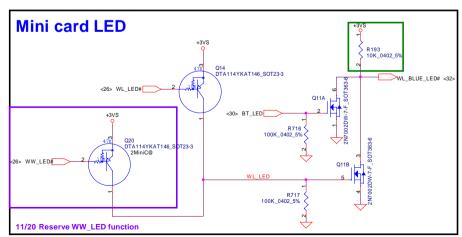




01/03 Change Lid switch connector type

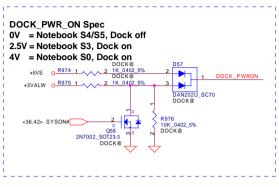


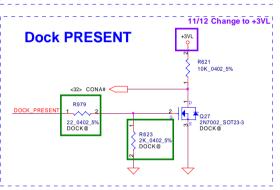


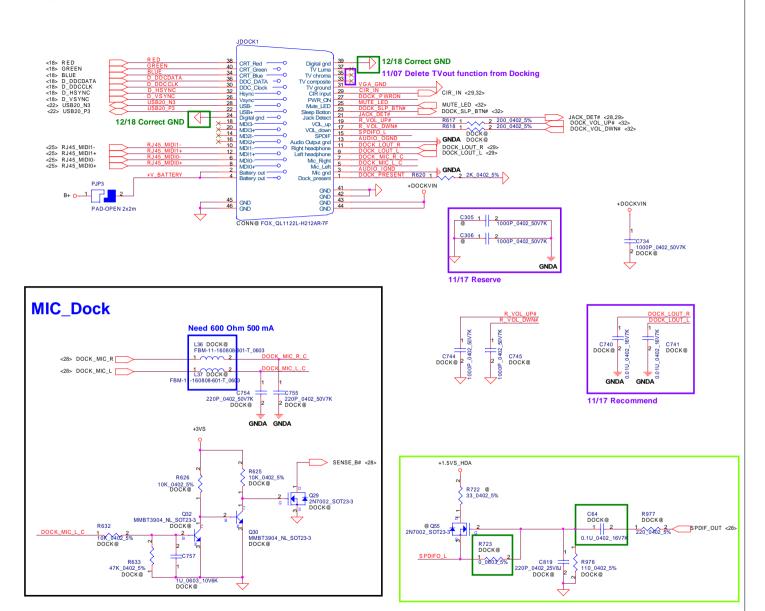


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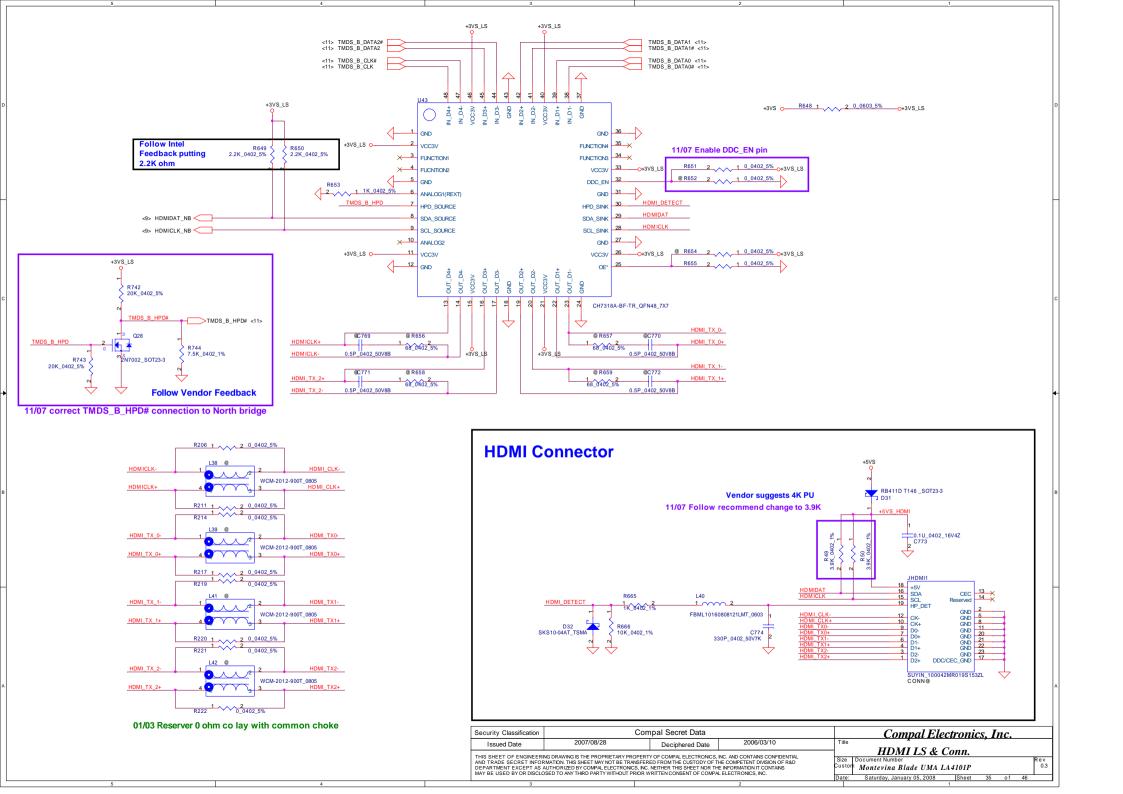
Atlas/ Saturn Dock

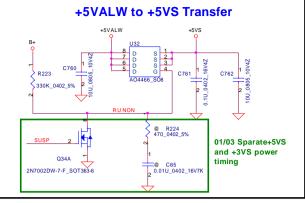


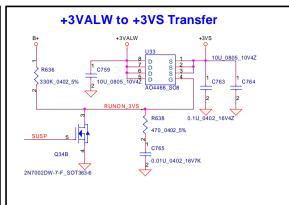


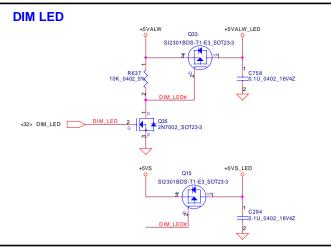


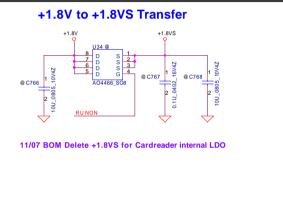
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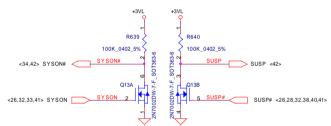


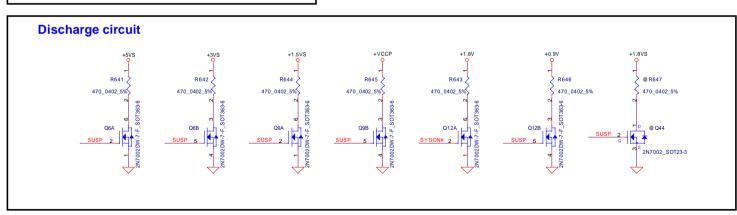


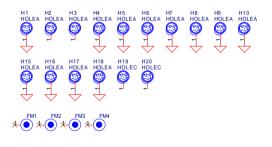




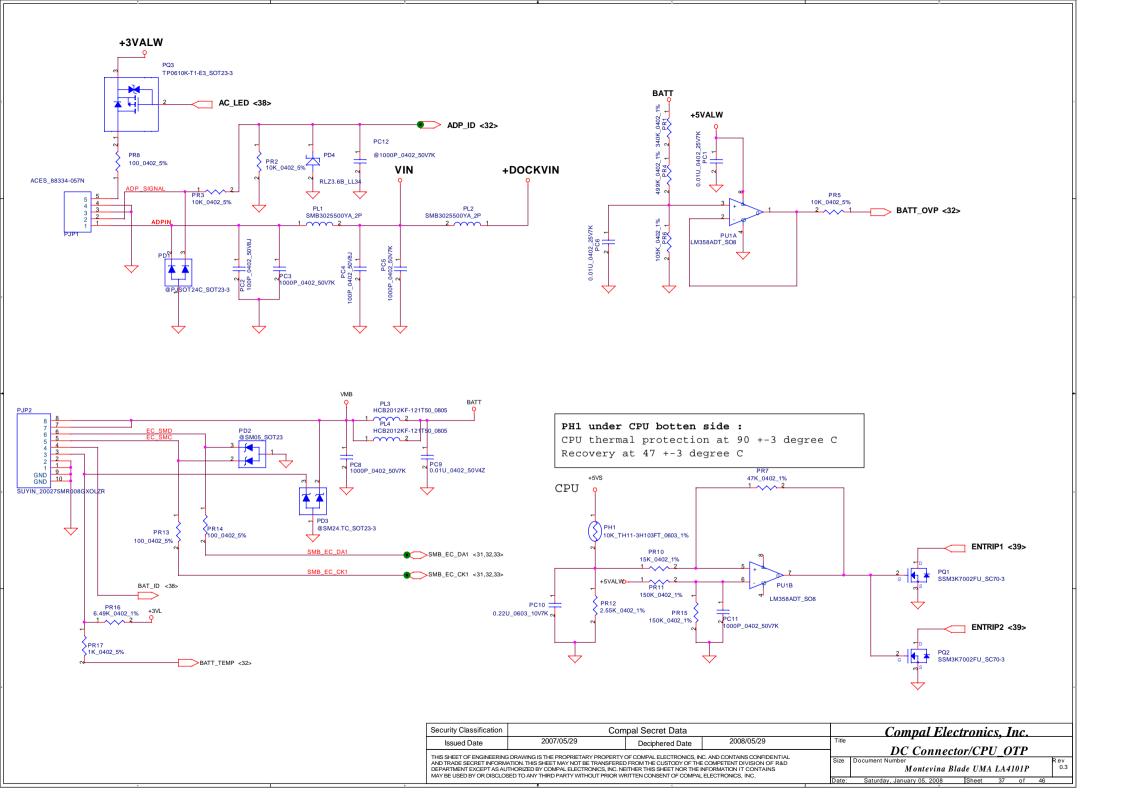


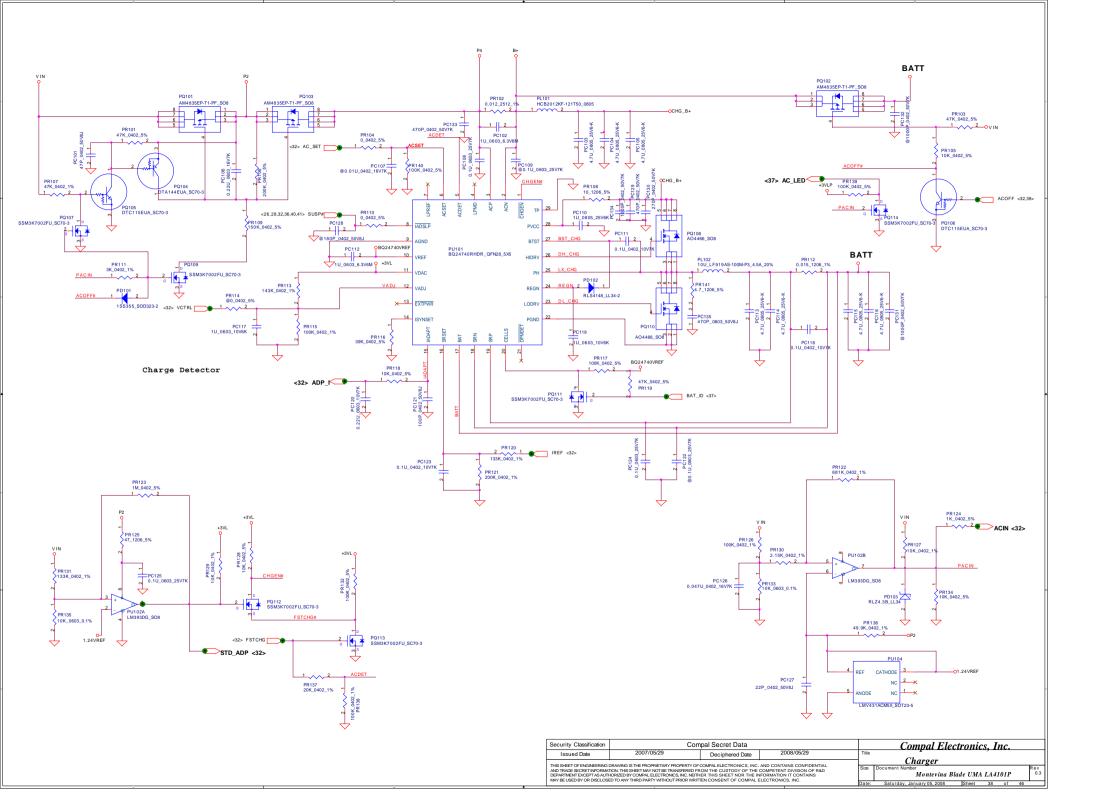


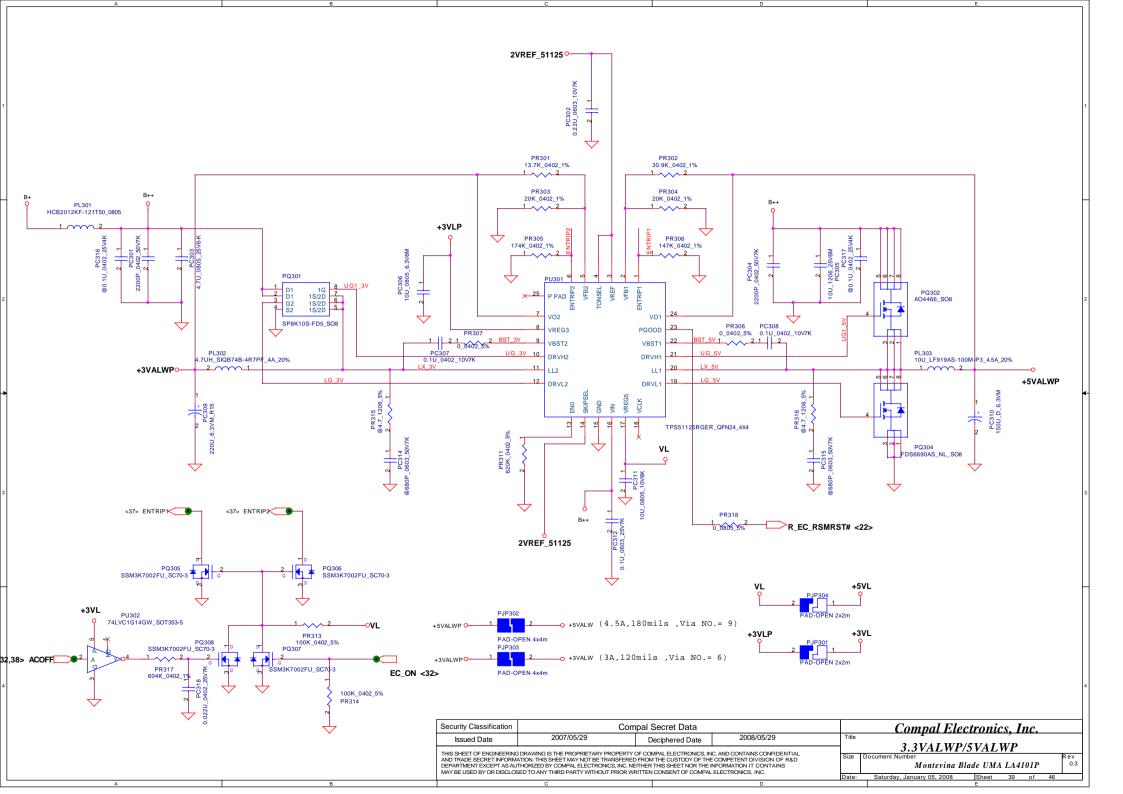


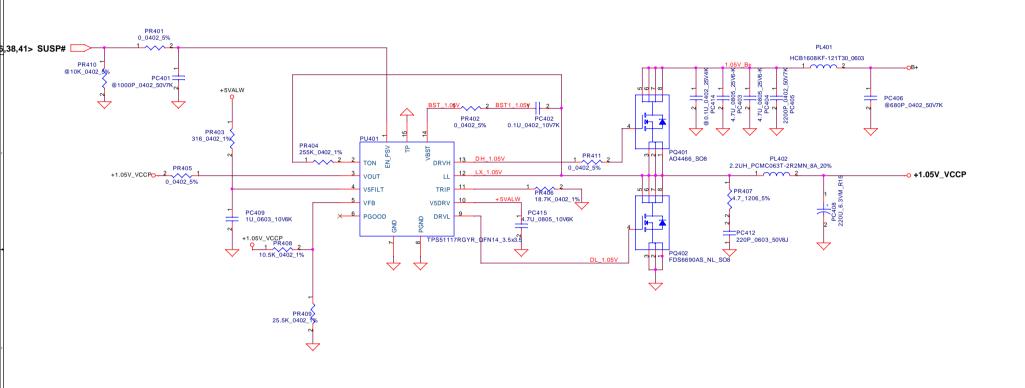


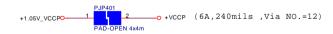
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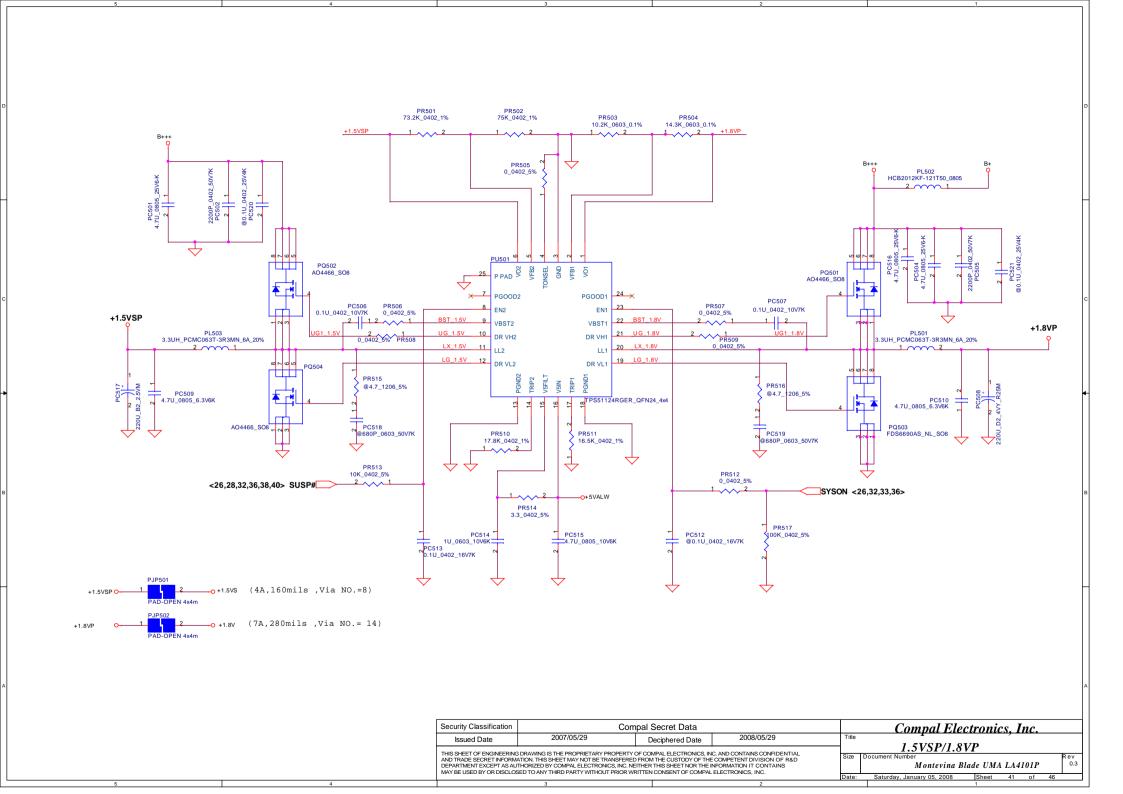


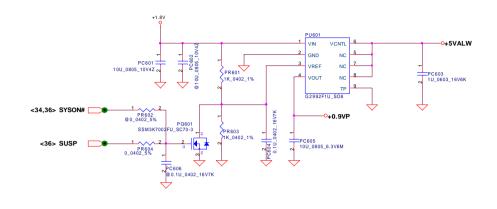






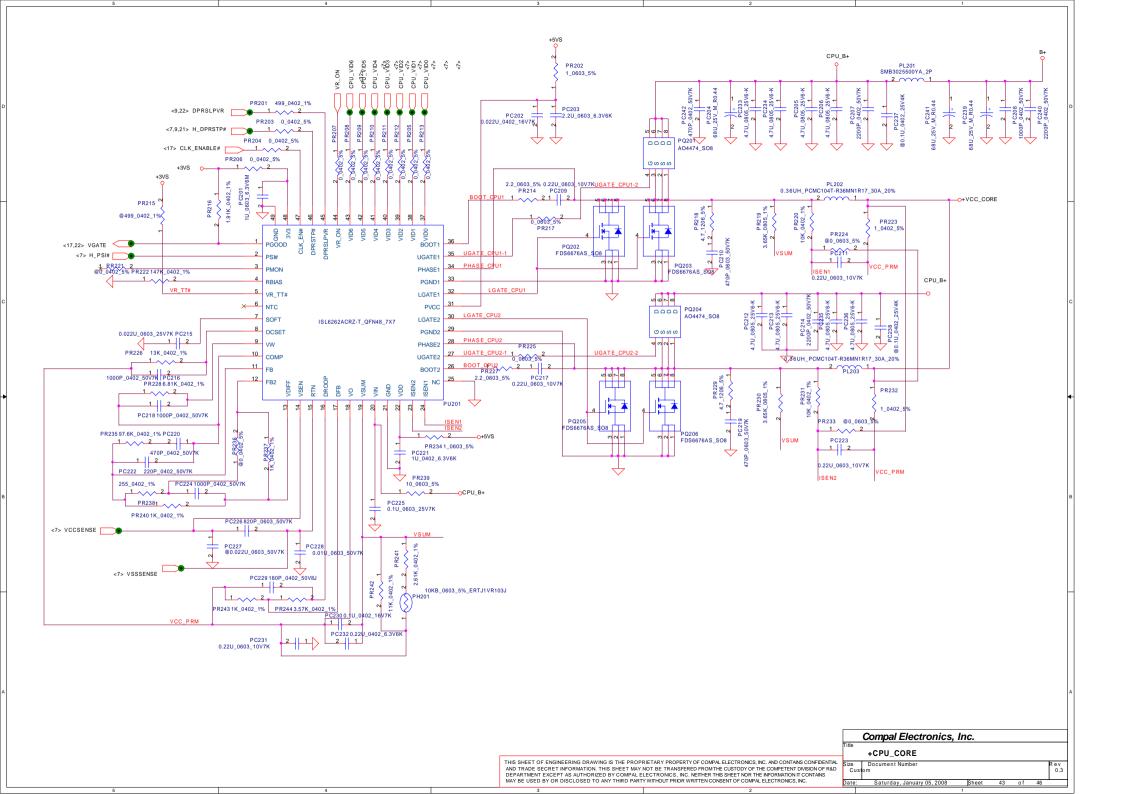
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tem	Fixed Issue (Reason for change)	PAGE	Modify List		Date	Phase		
1	Transation Fail	+ 08	C41 · C42 · C43 · C44 Change E	ESR=7m ohm	11/21	¦ SI-1		
2	Disable TV out function from Docking	¦ 11 · 34	R61 \ R62 \ R63 change to 75 Oh	nm · TV_DCONSEL_0 · TV_DCONSEL_1 connect to GND	11/07	¦ SI-1		
3	Update Connetor Library		CRT(JCRT1) · HDMI(JHDMI1) · E bay(JP12) · Dual LED(D53 · D12	SSATA(JP53) · Finger print(JJP24) · FAN(JP2) · Speaker(JP60) · Multi	11/17	 SI-1		
4	Delete LVDS B channel	11 \ 19	Schematic Delete	<u></u>	11/17	SI-1		
5	USB camera Footprint error	<u> </u>	Change U42 to G916-390T1UF S0	DT23, it adjustable mode, R1091=215K · R1093=100K	11/07	SI-1		
6	Reserve Card reader D3E function	22 \ 27	GPIO6= CR_CPPE# , GPIO22=0	CR_WAKE#	11/17	SI-1		
7	Swap PCIE LAN and New card	22	Swap PCIE4 and PICE6		11/17	¦ SI-1		
8	Add HDCP ROM for ICH9M	22 \ 31	Add HDCP ROM for ICH9M	PROM for ICH9M				
9	Change G sensor control from SB · LED drive by +5VS	22 \ 33	Change G sensor control from SB	sensor control from SB				
10	Avoid Battery mode can't boot issue	22 \ 39	Add +3VALW GD to EC_RSMRS	T# to fix Battery mode can't boot issue	11/17	SI-1		
11	Add G sensor ST and Bosch	24	Add G sensor ST and Bosch		11/17	SI-1		
12	Change LAN solution (Marvell to Realtek)	; 25 !	Change LAN solution (Marvell to R	Lealtek)	11/17	SI-1		
13	LAN can't work	25	U46 Change to correct transforme	r type	11/17	SI-1		
14	Cardreader schematic review and update, add D3E function	27	R709>10K \ R402>8.2K \ R704	4>Stuff、R705>@、U37>@、Cardreader LED>+5VS、add D3E func	tion 11/17	¦ SI-1		
15	Jack can't detect normal	+ 28	R1059 change from 39.2 to 39.2K	: :	11/17	SI-1		
16	Speaker work un normal	¦ 28	Add and Stuff C1362 \ R1065 \ R	: 596	11/17	SI-1		
17	HP audio team recommend	28 \ 29	C285~C292 \ C1352 \ C1354 cha	ange to 0.022U · Amp output setup to 15.6 dB · Reserve C305 · C306 for GN	NDA and GND	SI-1		
18	Audio jack can't detect normal	<u>.</u> . 29	Add Pull up resistor R401 to +3VA		11/17	SI-1		
19	Docking HP audio test fail	29	Add C295□BC296 to avoid DC lev	vel, and add R409 \ R410 to reduce HP out level	11/17	SI-1		
20	Leakage problem	32	Correct direction pretect leakage		11/07	¦ SI-1		
21	EC pin define update	32	Delete EC_PME# \ SYSON PU \ PU+5VL \ add 100P to BATT_OV	SUSP# PU \ LID_SW# change to +3VALW \ Delete CLKRUN# \ R582->@ t /P(EC_recommend)	for C0 chip \ CIR 11/07	¦ SI-1		
22	Can't Hibernation(SLP_S4#)	32	Connect SLP_S4# to SB		11/17	SI-1		
23	EC can't receive docking present	34	CONA# change +3VL		11/12	SI-1		
24	HDMI can't detect	35	DDC _EN must enable \ TMDS_I	B_HPD# inverse	11/07	SI-1		
25	LVDS power on timing	† ! 19	C238 change to 0.047u to meet TI	238 change to 0.047u to meet TI timing				
26	Prevent WWAN nosie		Add 12p on HDA_SDOUT and HDA_SDOUT					
27	Power leakage	¦ 21 · 31	Change HDCP ROM to +3VS pow	ver plane	01/03	SI-2		
28	Prevent WLAN leakage	+	Add Diode prevent WLAN leakage	e	01/03	SI-2		

Issued Date 2007/08/28 Deciphered Date 2006/07/26

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Fixed Issue (Reason for change)								$\overline{}$
(Itodoori or ordings)	PAGE	Modify List					Date	Phase
New card PTH connector GND	26	New card PTH connect	tor GND				01/03	SI-2
Change Cardreader LED control	27	Change Cardreader LE	ED control				01/03	SI-2
Change SPDIF to SPDIF1	28	Change to SPDIF1					 01/03	 SI-2
Shut down pop noise	29	Change C293 to 1U					01/03	SI-2
Change BT power to +3VS	30	Change BT power to +3	3VS				01/03	SI-2
EMI Request	31	SPI_FSEL# \ SPI_CLK	C_R \ SPI_FWR# re	eserver RC			01/03	SI-2
Reserver 0 ohm co lay with common choke	35	Reserver 0 ohm co lay v	with common choke	;			01/03	SI-2
Sparate+5VS and +3VS power timing	36	Sparate+5VS and +3V	S power timing				01/03	SI-2
Keyboard backlight reserve a 0805 size resistor	33	Keyboard backlight res	serve a 0805 size re	sistor			01/03	SI-2
Change Lid switch connector type	33	Change Lid switch conr	nector type				01/03	SI-2
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	Change Cardreader LED control Change SPDIF to SPDIF1 Shut down pop noise Change BT power to +3VS EMI Request Reserver 0 ohm co lay with common choke Sparate+5VS and +3VS power timing Keyboard backlight reserve a 0805 size resistor	Change Cardreader LED control 27 Change SPDIF to SPDIF1 28 Shut down pop noise 29 Change BT power to +3VS 30 EMI Request 31 Reserver 0 ohm co lay with common choke 35 Sparate+5VS and +3VS power timing 36 Keyboard backlight reserve a 0805 size resistor 33	Change Cardreader LED control 27 Change Cardreader LED Change SPDIF to SPDIF1 28 Change to SPDIF1 Shut down pop noise 29 Change C293 to 1U Change BT power to +3VS 30 Change BT power to + EMI Request 31 SPI_FSEL# \ SPI_CLI Reserver 0 ohm co lay with common choke 35 Reserver 0 ohm co lay Sparate+5VS and +3VS power timing 36 Sparate+5VS and +3V Keyboard backlight reserve a 0805 size resistor 33 Keyboard backlight reserve	Change Cardreader LED control Change SPDIF to SPDIF1 28 Change to SPDIF1 Shut down pop noise 29 Change BT power to +3VS 30 Change BT power to +3VS EMI Request 31 SPLESEL# SPLCLK.R · SPLEWR# n Reserver 0 ohm co lay with common choke 35 Reserver 0 ohm co lay with common choke Sparate+5VS and +3VS power timing Keyboard backlight reserve a 0805 size resistor Change Lid switch connector type 33 Change Lid switch connector type	Change SPDIF to SPDIF1 28 Change to SPDIF1 Shut down pop noise 29 Change C293 to 1U Change BT power to +3VS 30 Change BT power to +3VS EMI Request 31 SPLFSEL# - SPLCLK_R - SPLFWR# reserver RC Reserver 0 ohm to lay with common choke 35 Reserver 0 ohm to lay with common choke 35 Sparate-SVS and +3VS power timing 48 Sparate-SVS and +3VS power timing 59 Change Lid switch connector type 33 Change Lid switch connector type 33 Change Lid switch connector type	Change Cardreader LED control Change SPDIF to SPDIF1 28 Change to SPDIF1 Shut down pop noise 29 Change C233 to TU Change BT power to +3VS 30 Change BT power to +3VS 31 SPLFSEL# - SPL_CLK_R - SPL_FWR# reserver RC Reserver 0 ohm oo lay with common chake 35 Reserver 0 ohm oo lay with common chake Sparate-5VS and +3VS power timing 36 Sparate-5VS and +3VS power timing Keyboard backlight reserve a 0805 size resistor Change Lid switch connector type 33 Change Lid switch connector type 34 Change Lid switch connector type	Change SPDIF to SPDIF 1 28 Change SPDIF 1 29 Change SPDIF 1 29 Change SPDIF 1 29 Change SPDIF 1 20 Cha	Change SPDIF to SPDIF 1

Version Change List (P. I. R. List) for Power Circuit Request Title Date Issue Description Item Page# Solution Description Rev. Owner DC Connector Add PD4 & PC12 37 11/06 Compal Add PD4 & PC12 /CPU_OTP 2 39 3.3VALWP/5VALWP 11/06 | Compal for Layout Change PQ301 cancel PQ303 3 38 Charger Compal EMI solution Add pc128 +CPU CORE 11/06 Compal EMI solution 43 Add PC240 39 3.3VALWP/5VALWP 11/14 Compal Change PL303 and PC310 for Layout 6 38 Charger 12/31 Compal EMI solution Add PC129, PC130, PC131, PC132, PC133 43 +CPU_CORE 12/31 Compal EMI solution Add PC242 39 3.3VALWP/5VALWP 12/31 Compal PWR request Add PU302, control signal changed to ACOFF 11 12 13 Compal Electronics, Inc. Security Classification Compal Secret Data 2007/08/02 2008/08/02 Power Changed-List History-1 Issued Date THIS SHEET OF ENGINEERING DRAWNIG IS THE PROPRIETIARY PROPERTY OF COMPAL ELECTRONES, INC. AND CONTAINS CONFIDENTIAL AND ITRADE SECRET INFORMATION. THIS SHEET HAWN FOR BET ARRESTREED FROM THE CLISTION OF FIRE COMPETENT FOR OFF RAD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPALELECTRONGS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PRATY WITHOUT PRIOR WITHITEN CONSENT OF COMPALELECTRONGS. Montevina Blade UMA LA4101P Saturday, January 05, 2008 Sheet 46 of 46