# LCFC Confidential

## E555

## NM-A241 Schematics

AMD Kaveri 2.0 Processor with DDR3L + Bolton FCH

GPU AMD TOPAZ XT

2013-11-20

REV:0.2

| | | | |
|---|---|---|---|
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**Title**

**Cover Page**

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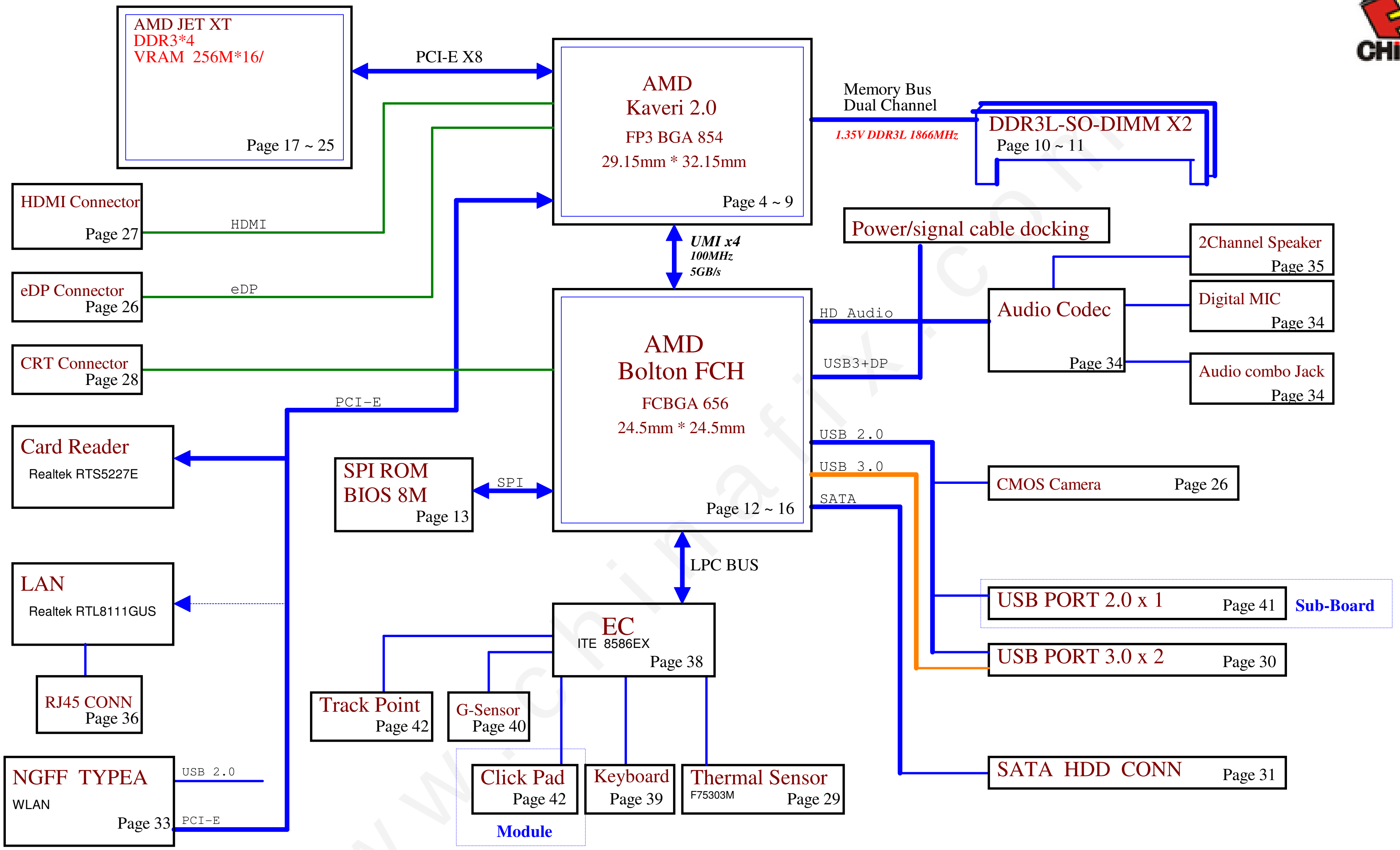
Model Name : AATE1



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## Voltage Rails ( O --> Means ON , X --> Means OFF )

| Power Plane / State | B+ | +3VALW<br>+5VALW | +1.5V | +5VS<br>+3VS<br>+0.675VS<br>+0.95VS_VDDP<br>+0.95VS_VDDR<br>+1.8VS_VDDA<br>+1.1VS<br>+VDD_CORE<br>+VDDNB_CORE<br>+VGA_CORE<br>+3VS_VGA<br>+1.8VS_VGA<br>+1.5VS_VGA<br>+0.95VS_VGA |
|---|---|---|---|---|
| S0 | O | O | O | O |
| S3 | O | O | O | X |
| S5 S4/AC Only | O | O | X | X |
| S5 S4 Battery only | O | X | X | X |
| S5 S4 AC & Battery don't exist | X | X | X | X |

| SIGNAL / STATE | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|---|---|---|---|---|---|---|---|---|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1(Power On Suspend) | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

## USB Port Table

| USB 2.0 | USB 3.0 | Port | Port | 3 External USB Port |
|---|---|---|---|---|
| EHCI | | | 0 | USB 2.0 Port |
| | | | 1 | |
| | | | 2 | |
| | | | 3 | |
| | | | 4 | |
| EHCI | | | 5 | Camera |
| | | | 6 | WLAN/BT |
| | | | 7 | FPR |
| | | | 8 | |
| | | | 9 | |
| | xHCI | 0 | 10 | USB 3.0 Port |
| | | 1 | 11 | |
| | xHCI | 2 | 12 | USB 3.0 Port |
| | | 3 | 13 | Docking port |

## BOM Structure Table

| BTO Item | BOM Structure |
|---|---|
| Un-mount | @ |
| Connector | ME@ |
| GPU | DIS@ |
| UMA | UMA@ |
| VRAM Option | X76@ |
| RF Part Option | RF@ |
| EMI Part Option | EMI@ |
| ESD Part Option | ESD@ |
| JET GPU | JET@ |
| TOPAZ GPU | TOPAZ@ |
| Quad Core APU | QC@ |
| 15 MB | 15@ |
| | |
| | |
| | |
| | |
| | |
| | |

## PCIE PORT LIST

| Port | Device |
|---|---|
| 0 | LAN |
| 1 | Card Reader |
| 2 | WLAN |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

## EC SM Bus1 address

| Device | Address |
|---|---|
| Smart Battery | 0001 011X b |

## EC SM Bus3 address

| Device | Address |
|---|---|
| Thermal Sensor | |

## FCH SM Bus address

| Device | Address |
|---|---|
| DDR DIMM1 | |
| DDR DIMM2 | |

ZZZ1

DAZ0TX00100

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**Notes List**

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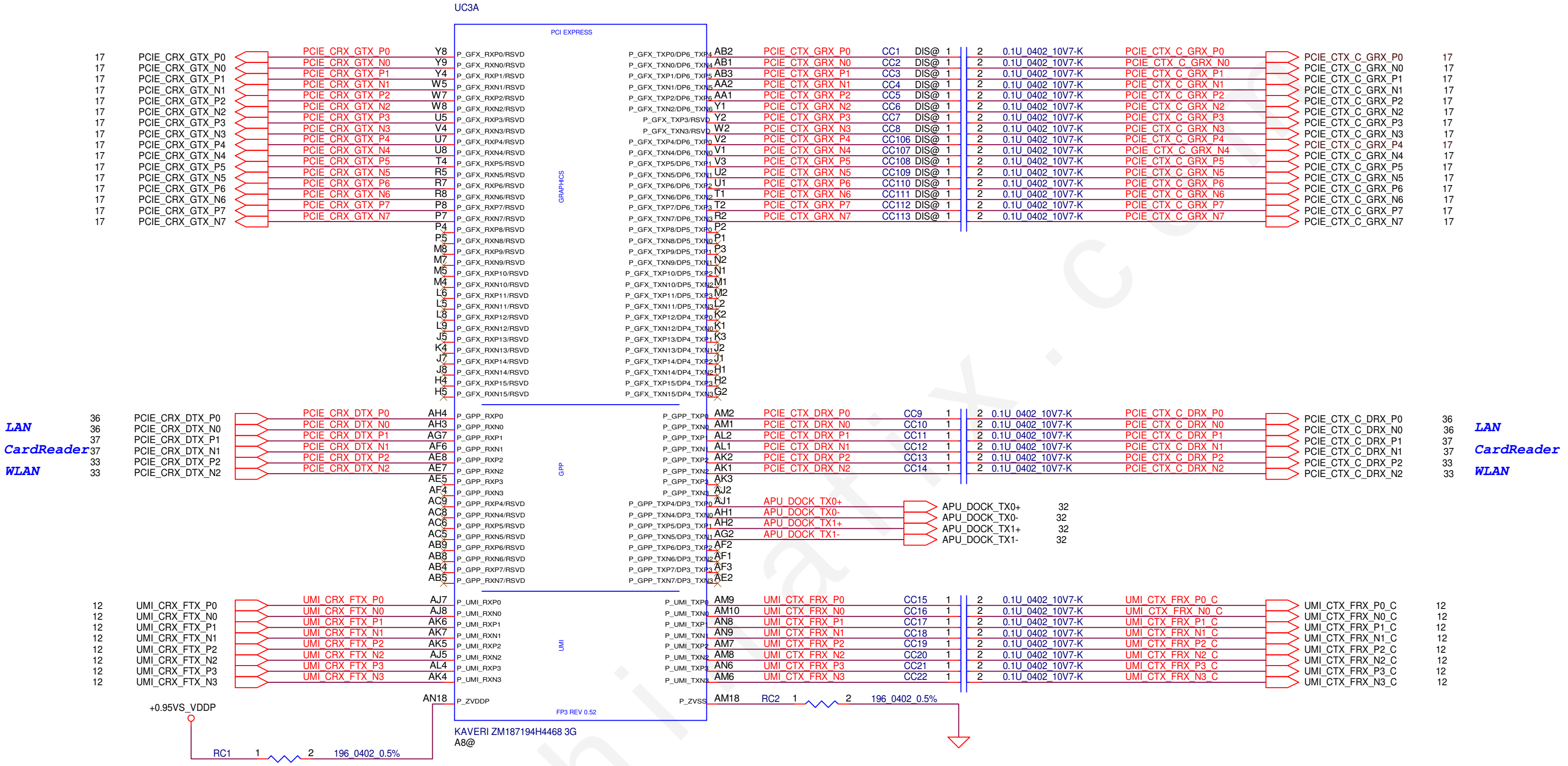

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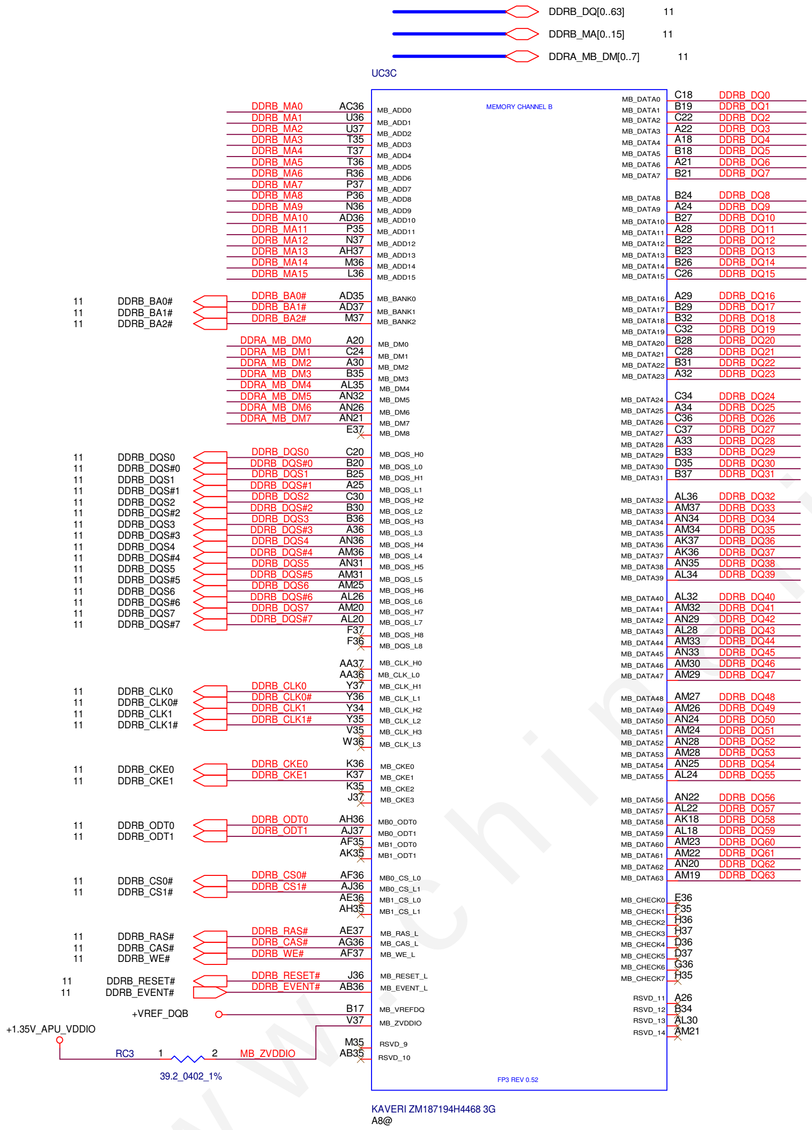

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Title
**APU DDRB/2**

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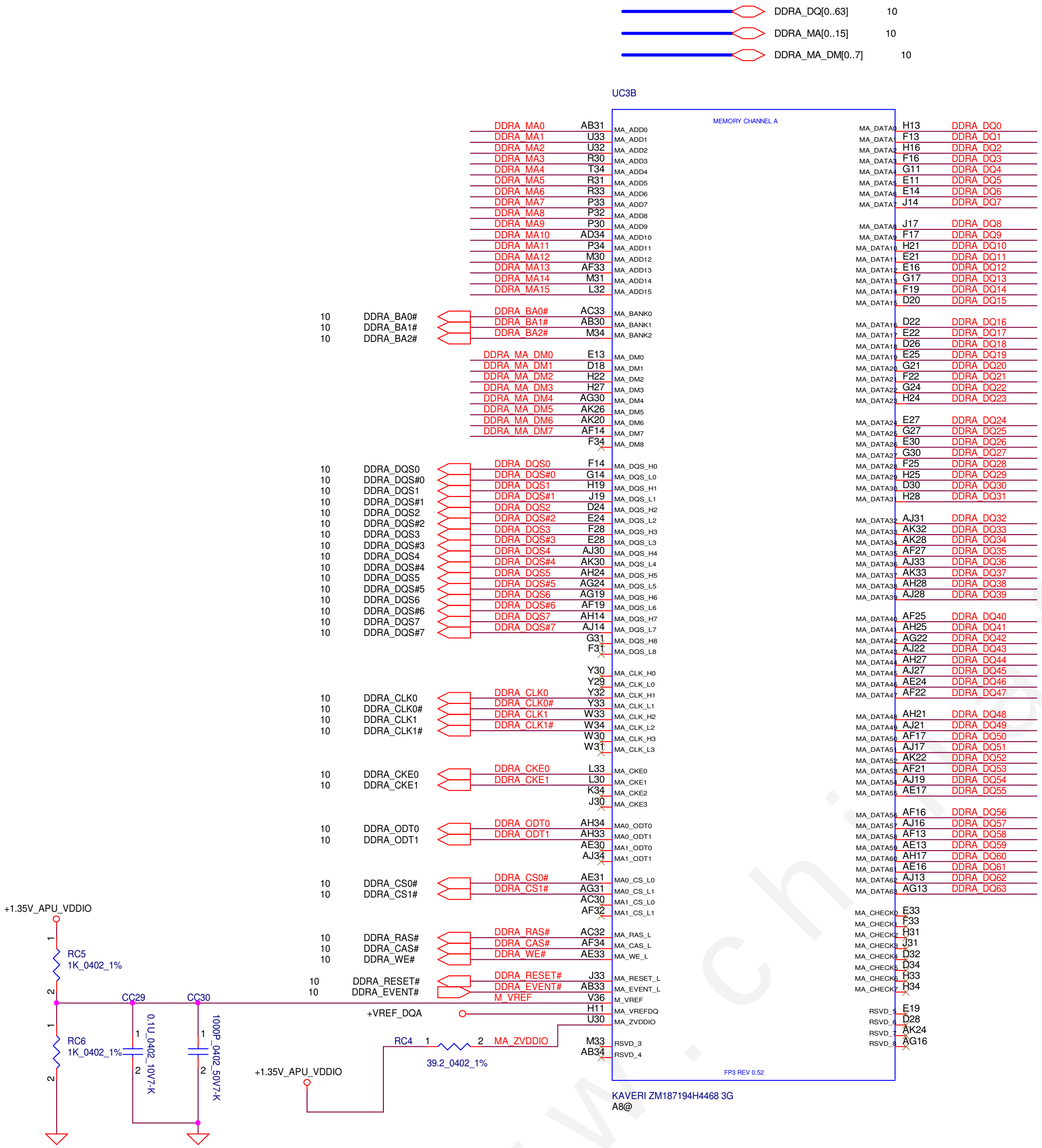

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**APU DDRA/1**

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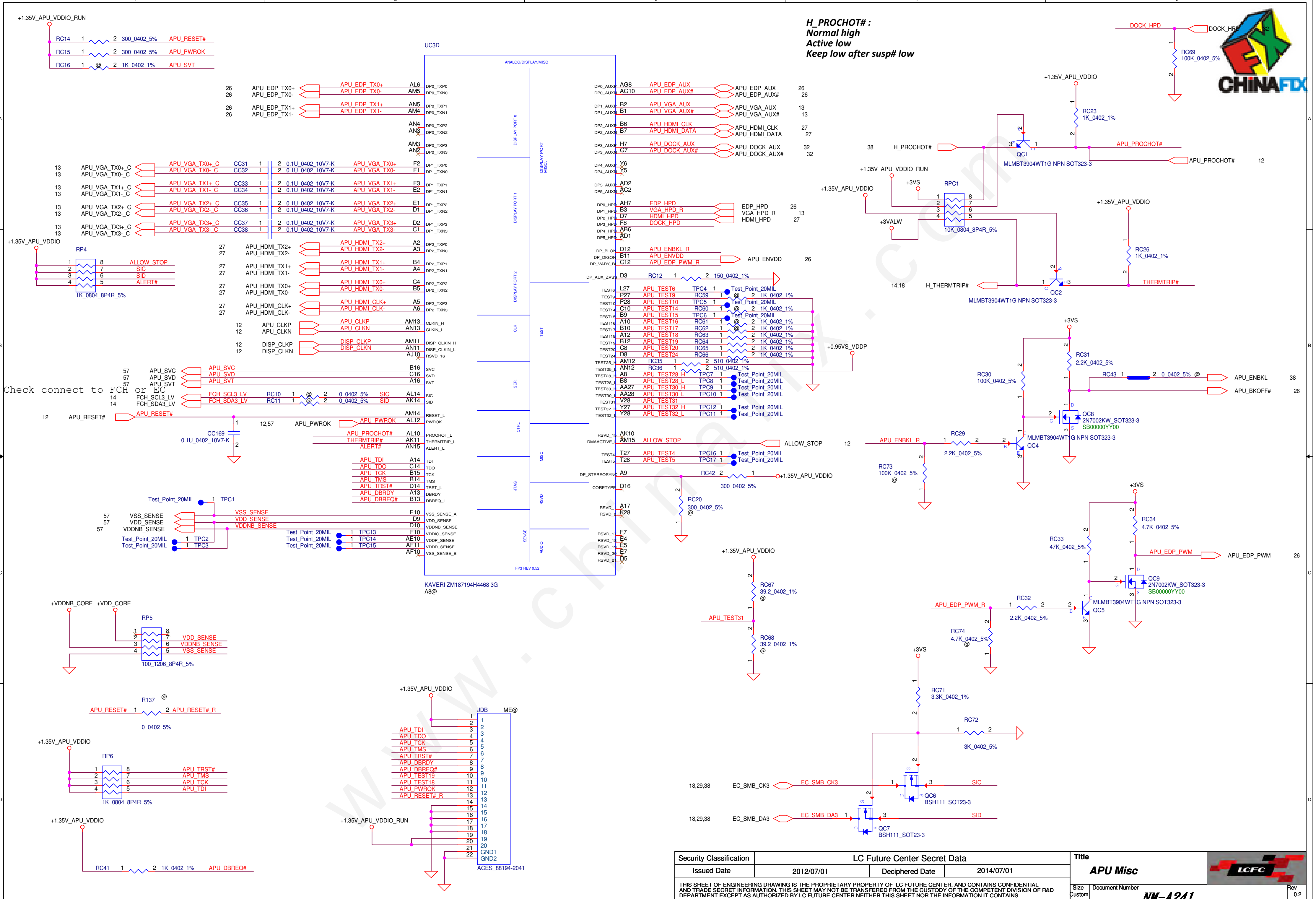

+1.35V_APU_VDDIO_RUN
RC14 300_0402_5% APU_RESET#
RC15 300_0402_5% APU_PWROK
RC16 1K_0402_1% APU_SVT
UC3D
ANALOG/DISPLAY/MISC
APU_EDP_TX0+ AL6 DP0_TXP0
APU_EDP_TX0- AM5 DP0_TXN0
APU_EDP_TX1+ AN5 DP0_TXP1
APU_EDP_TX1- AM4 DP0_TXN1
AN4 DP0_TXP2
AN3 DP0_TXN2
AM3 DP0_TXP3
AN2 DP0_TXN3
APU_VGA_TX0+_C CC31 0.1U_0402_10V7-K APU_VGA_TX0+ F2 DP1_TXP0
APU_VGA_TX0-_C CC32 0.1U_0402_10V7-K APU_VGA_TX0- F1 DP1_TXN0
APU_VGA_TX1+_C CC33 0.1U_0402_10V7-K APU_VGA_TX1+ F3 DP1_TXP1
APU_VGA_TX1-_C CC34 0.1U_0402_10V7-K APU_VGA_TX1- E2 DP1_TXN1
APU_VGA_TX2+_C CC35 0.1U_0402_10V7-K APU_VGA_TX2+ E1 DP1_TXP2
APU_VGA_TX2-_C CC36 0.1U_0402_10V7-K APU_VGA_TX2- D1 DP1_TXN2
APU_VGA_TX3+_C CC37 0.1U_0402_10V7-K APU_VGA_TX3+ D2 DP1_TXP3
APU_VGA_TX3-_C CC38 0.1U_0402_10V7-K APU_VGA_TX3- C1 DP1_TXN3
APU_HDMI_TX2+ A2 DP2_TXP0
APU_HDMI_TX2- A3 DP2_TXN0
APU_HDMI_TX1+ B4 DP2_TXP1
APU_HDMI_TX1- A4 DP2_TXN1
APU_HDMI_TX0+ C4 DP2_TXP2
APU_HDMI_TX0- B5 DP2_TXN2
APU_HDMI_CLK+ A5 DP2_TXP3
APU_HDMI_CLK- A6 DP2_TXN3
APU_CLKP AM13 CLKIN_H
APU_CLKN AN13 CLKIN_L
DISP_CLKP AM11 DISP_CLKIN_H
DISP_CLKN AN11 DISP_CLKIN_L
AJ10 RSVD_16
APU_SVC B16 SVC
APU_SVD C16 SVD
APU_SVT A16 SVT
FCH_SCL3_LV RC10 0_0402_5% SIC AL14 SIC
FCH_SDA3_LV RC11 0_0402_5% SID AK14 SID
APU_RESET# AM14 RESET_L
APU_PWROK AL12 PWROK
CC169 0.1U_0402_10V7-K
APU_PROCHOT# AL10 PROCHOT_L
THERMTRIP# AK11 THERMTRIP_L
ALERT# AN15 ALERT_L
APU_TDI A14 TDI
APU_TDO C14 TDO
APU_TCK B15 TCK
APU_TMS B14 TMS
APU_TRST# D14 TRST_L
APU_DBRDY A13 DBRDY
APU_DBREQ# B13 DBREQ_L
Test_Point_20MIL TPC1
VSS_SENSE E10 VSS_SENSE_A
VDD_SENSE D9 VDD_SENSE
VDDNB_SENSE D10 VDDNB_SENSE
TPC13 F10 VDDIO_SENSE
TPC14 AE10 VDDP_SENSE
TPC15 AF11 VDDR_SENSE
AF10 VSS_SENSE_B
TPC2 TPC3
DISPLAY PORT 0
DISPLAY PORT 1
DISPLAY PORT 2
DISPLAY PORT MISC
CLK
SER
CTRL
JTAG
SENSE
TEST
MISC
RSVD
AUDIO
FP3 REV 0.52
KAVERI ZM187194H4468 3G
A8@
DP0_AUXP AG8 APU_EDP_AUX
DP0_AUXN AG10 APU_EDP_AUX#
DP1_AUXP B2 APU_VGA_AUX
DP1_AUXN B1 APU_VGA_AUX#
DP2_AUXP B6 APU_HDMI_CLK
DP2_AUXN B7 APU_HDMI_DATA
DP3_AUXP H7 APU_DOCK_AUX
DP3_AUXN G7 APU_DOCK_AUX#
DP4_AUXP Y6
DP4_AUXN Y5
DP5_AUXP AD2
DP5_AUXN AC2
DP0_HPD AH7 EDP_HPD
DP1_HPD B3 VGA_HPD_R
DP2_HPD D7 HDMI_HPD
DP3_HPD F8 DOCK_HPD
DP4_HPD AB6
DP5_HPD AD1
DP_BLON D12 APU_ENBKL_R
DP_DIGON B11 APU_ENVDD
DP_VARY_BL C12 APU_EDP_PWM_R
DP_AUX_ZVSS D3 RC12 150_0402_1%
TEST6 L27 APU_TEST6 TPC4
TEST9 P27 APU_TEST9 RC59 1K_0402_1%
TEST10 P28 APU_TEST10 TPC5
TEST14 C10 APU_TEST14 RC60 1K_0402_1%
TEST15 B9 APU_TEST15 TPC6
TEST16 A10 APU_TEST16 RC61 1K_0402_1%
TEST17 B10 APU_TEST17 RC62 1K_0402_1%
TEST18 A12 APU_TEST18 RC63 1K_0402_1%
TEST19 B12 APU_TEST19 RC64 1K_0402_1%
TEST20 C8 APU_TEST20 RC65 1K_0402_1%
TEST24 D8 APU_TEST24 RC66 1K_0402_1%
TEST25_H AM12 RC35 510_0402_1%
TEST25_L AN12 RC36 510_0402_1%
TEST28_H A8 APU_TEST28_H TPC7
TEST28_L B8 APU_TEST28_L TPC8
TEST30_H AA27 APU_TEST30_H TPC9
TEST30_L AA28 APU_TEST30_L TPC10
TEST31 V28 APU_TEST31
TEST32_H Y27 APU_TEST32_H TPC12
TEST32_L Y28 APU_TEST32_L TPC11
RSVD_15 AK10
DMAACTIVE_L AM15 ALLOW_STOP
TEST4 T27 APU_TEST4 TPC16
TEST5 T28 APU_TEST5 TPC17
DP_STEREOSYNC A9 RC42 300_0402_5% +1.35V_APU_VDDIO
CORETYPE D16 RC20 300_0402_5%
RSVD_1 A17
RSVD_2 K28
RSVD_17 F7
RSVD_18 E4
RSVD_19 E5
RSVD_20 E7
RSVD_21 D5
+0.95VS_VDDP
+1.35V_APU_VDDIO
RP4 1K_0804_8P4R_5% ALLOW_STOP SIC SID ALERT#
DOCK_HPD RC69 100K_0402_5%
RC23 1K_0402_1%
QC1 MLMBT3904WT1G NPN SOT323-3
H_PROCHOT# APU_PROCHOT#
RPC1 10K_0804_8P4R_5% +3VS +3VALW
RC26 1K_0402_1%
H_THERMTRIP# THERMTRIP#
QC2 MLMBT3904WT1G NPN SOT323-3
RC31 2.2K_0402_5%
RC30 100K_0402_5%
RC43 0_0402_5% APU_ENBKL APU_BKOFF#
QC8 2N7002KW_SOT323-3 SB00000YY00
APU_ENBKL_R RC29 2.2K_0402_5%
QC4 MLMBT3904WT1G NPN SOT323-3
RC73 100K_0402_5%
RC34 4.7K_0402_5%
RC33 47K_0402_5%
APU_EDP_PWM
QC9 2N7002KW_SOT323-3 SB00000YY00
APU_EDP_PWM_R RC32 2.2K_0402_5%
QC5 MLMBT3904WT1G NPN SOT323-3
RC74 4.7K_0402_5%
RC67 39.2_0402_1%
APU_TEST31
RC68 39.2_0402_1%
RC71 3.3K_0402_1%
RC72 3K_0402_5%
EC_SMB_CK3 QC6 BSH111_SOT23-3 SIC
EC_SMB_DA3 QC7 BSH111_SOT23-3 SID
+VDDNB_CORE +VDD_CORE
RP5 100_1206_8P4R_5% VDD_SENSE VDDNB_SENSE VSS_SENSE
R137 0_0402_5% APU_RESET# APU_RESET#_R
RP6 1K_0804_8P4R_5% APU_TRST# APU_TMS APU_TCK APU_TDI
RC41 1K_0402_1% APU_DBREQ#
JDB ME@ ACES_88194-2041
APU_TDI APU_TDO APU_TCK APU_TMS APU_TRST# APU_DBRDY APU_DBREQ# APU_TEST19 APU_TEST18 APU_PWROK APU_RESET#_R
GND1 GND2

H_PROCHOT# :
Normal high
Active low
Keep low after susp# low

Check connect to FCH or EC

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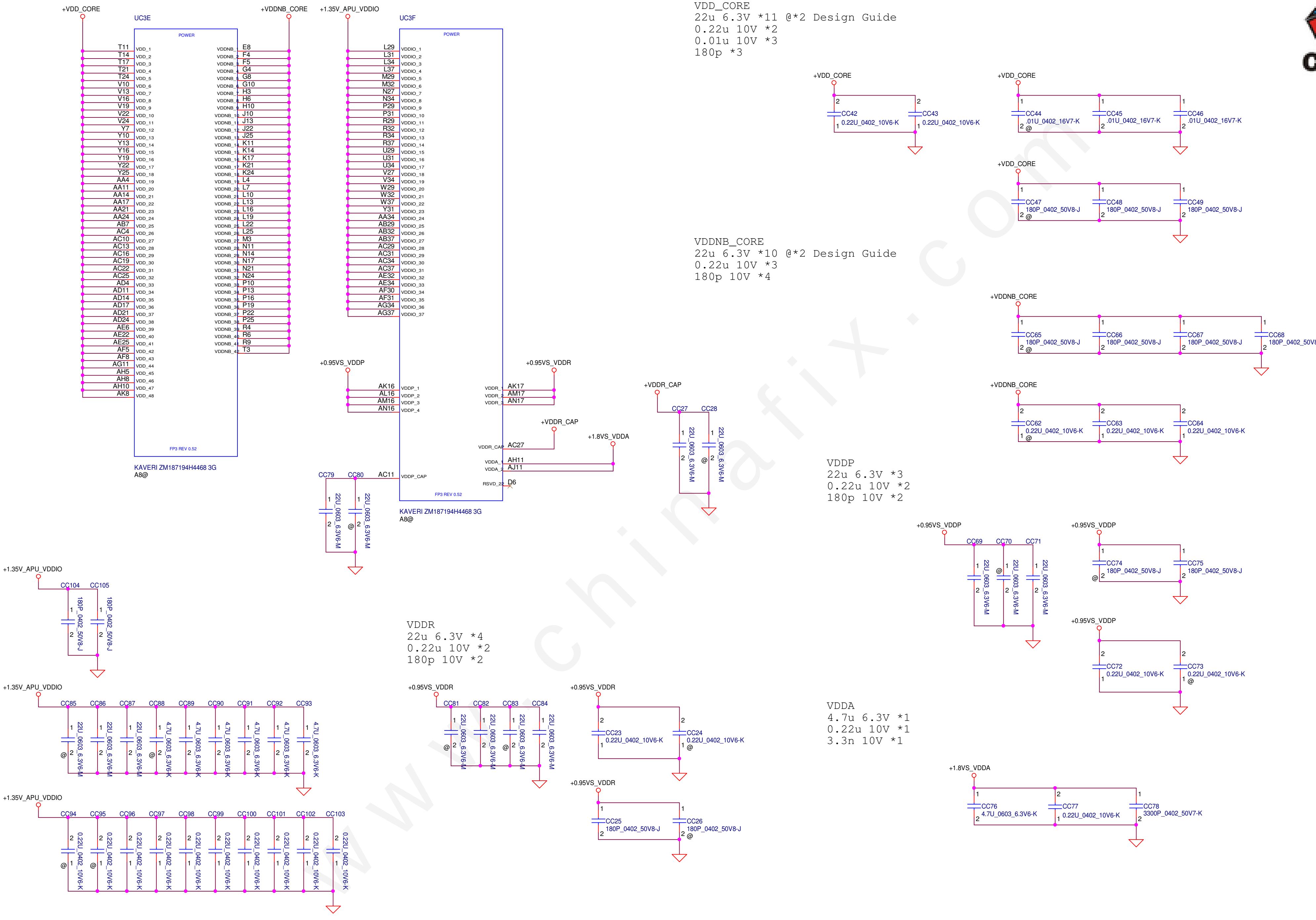

VDD_CORE
22u 6.3V *11 @*2 Design Guide
0.22u 10V *2
0.01u 10V *3
180p *3

VDDNB_CORE
22u 6.3V *10 @*2 Design Guide
0.22u 10V *3
180p 10V *4

VDDP
22u 6.3V *3
0.22u 10V *2
180p 10V *2

VDDR
22u 6.3V *4
0.22u 10V *2
180p 10V *2

VDDA
4.7u 6.3V *1
0.22u 10V *1
3.3n 10V *1

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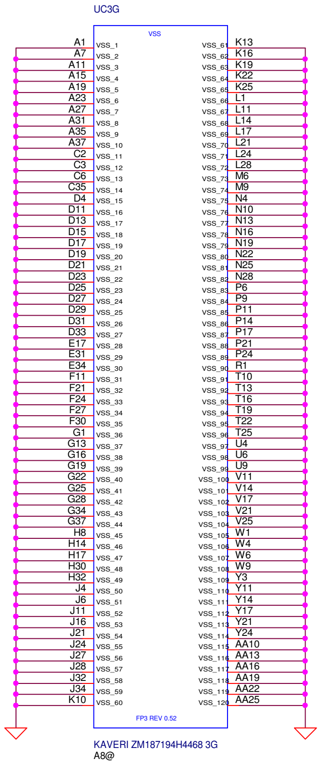

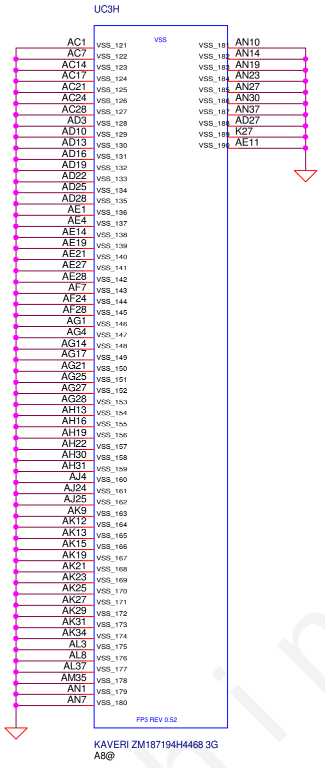

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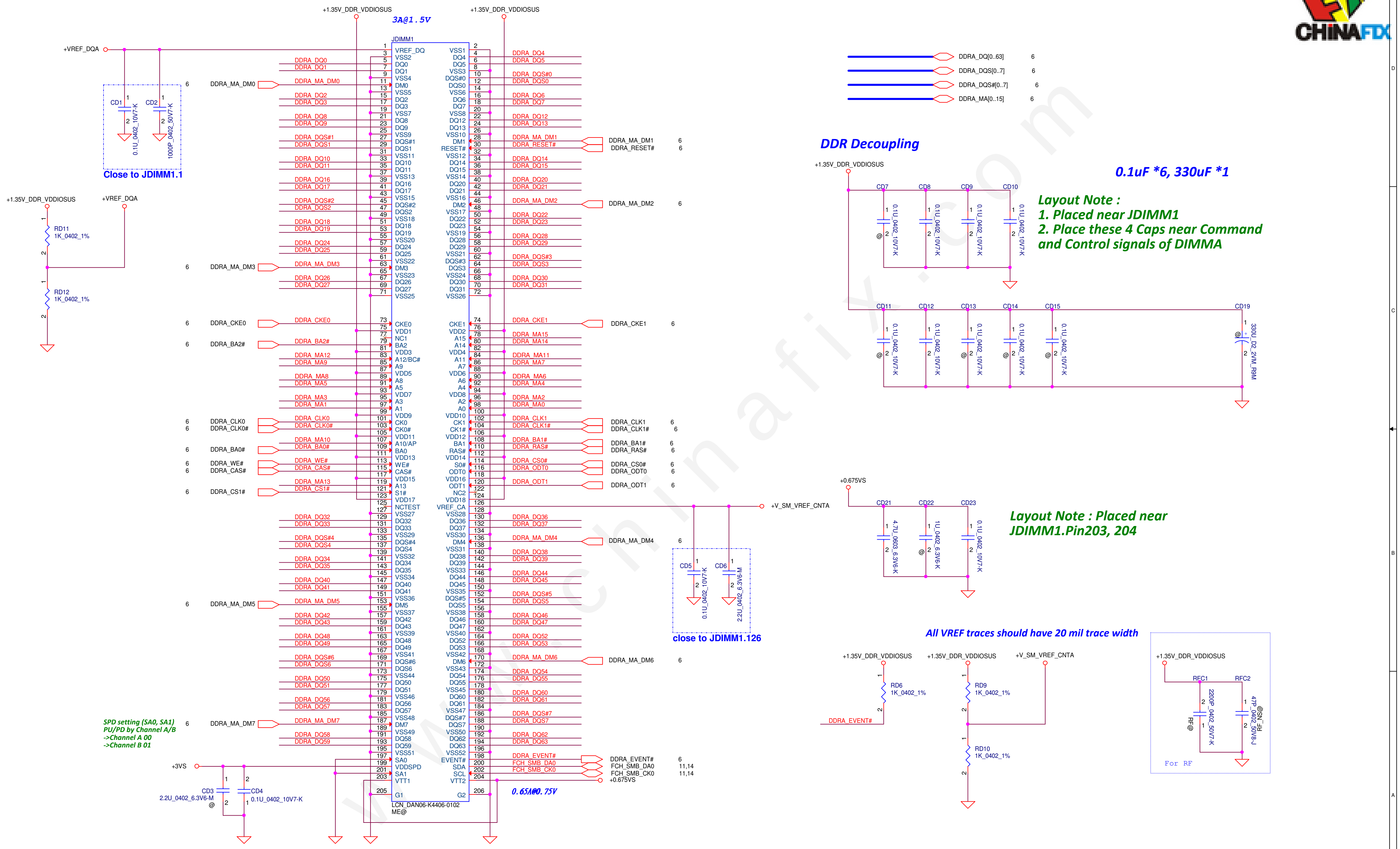
# DDR3L SO-DIMM A



Layout Note :
1. Placed near JDIMM1
2. Place these 4 Caps near Command and Control signals of DIMMA

Layout Note : Placed near JDIMM1.Pin203, 204

All VREF traces should have 20 mil trace width

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DDR3L SO-DIMMA/1

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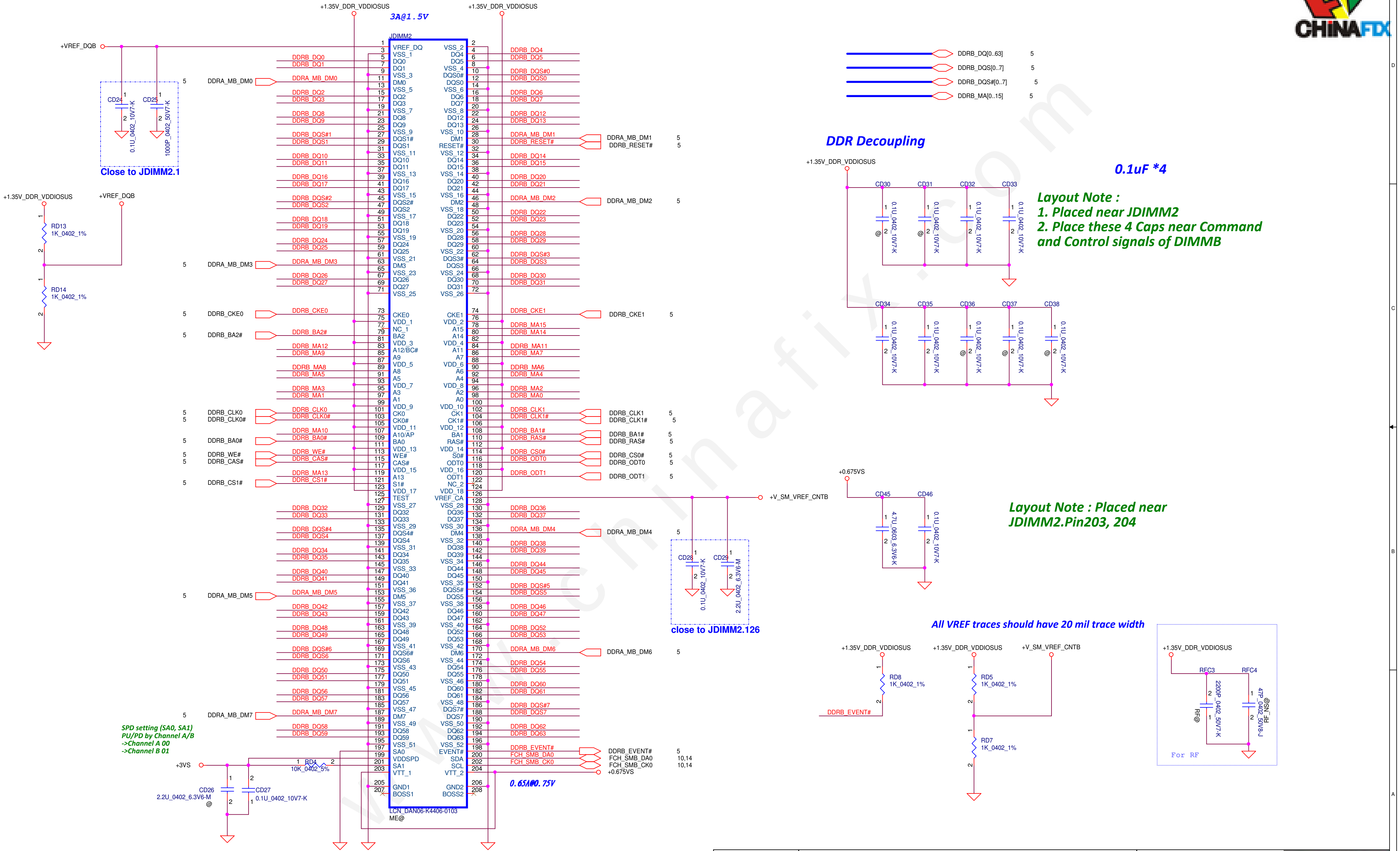
# DDR3L SO-DIMM B



SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

Layout Note :
1. Placed near JDIMM2
2. Place these 4 Caps near Command and Control signals of DIMMB

Layout Note : Placed near JDIMM2.Pin203, 204

All VREF traces should have 20 mil trace width

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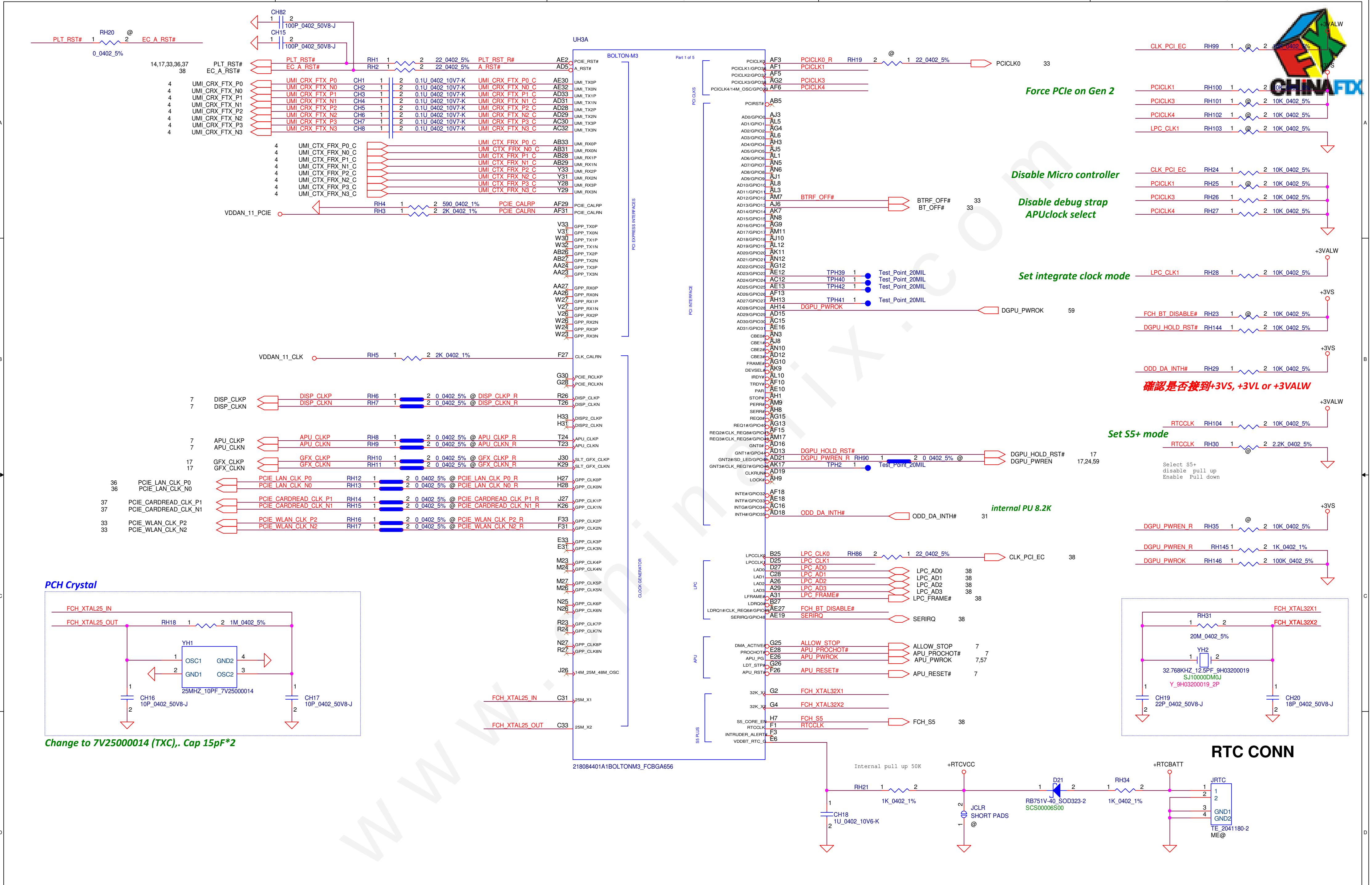

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FCH PCIe/PCI/LPC/APU/S5+

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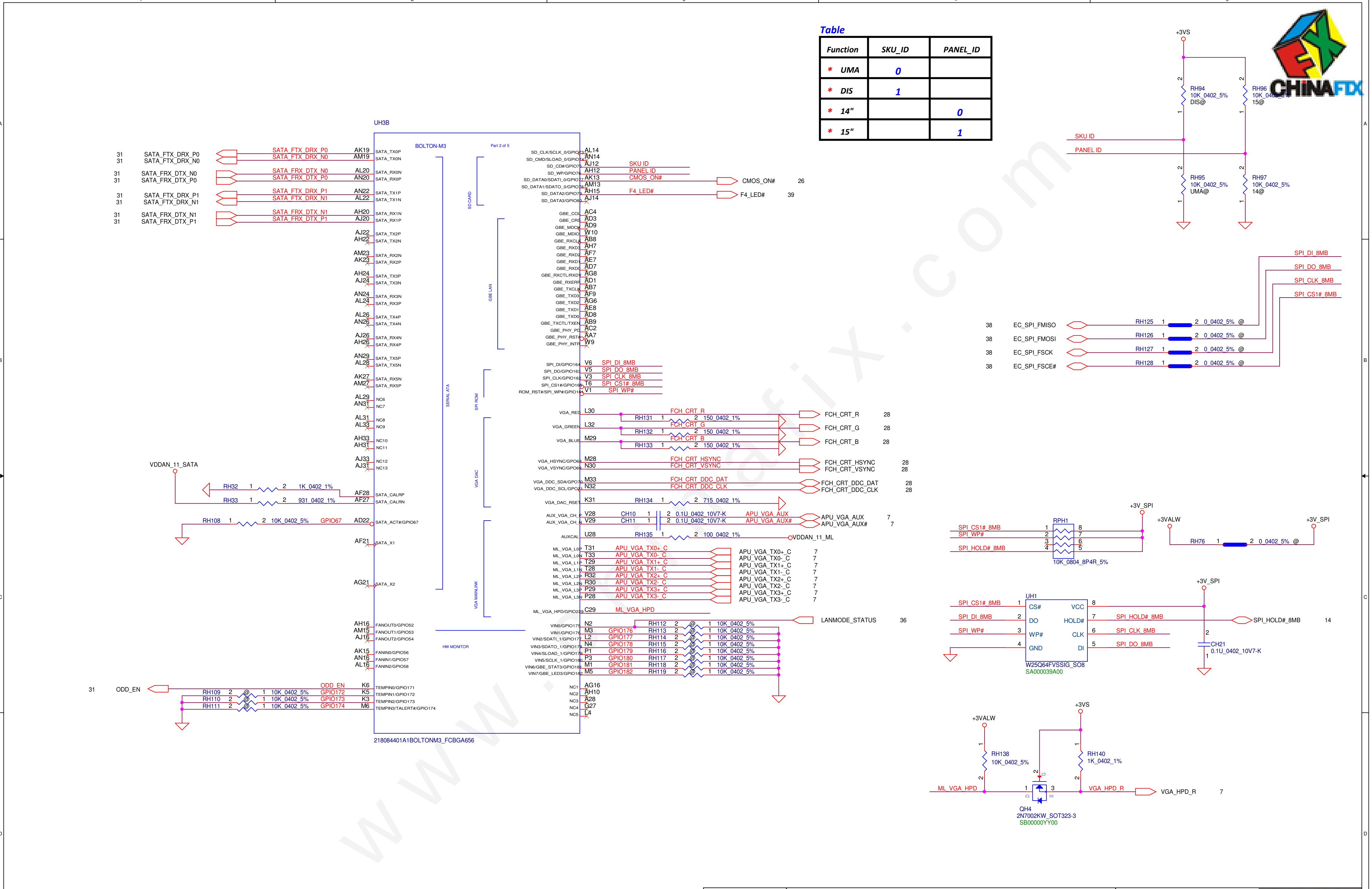
**Table**

| Function | SKU_ID | PANEL_ID |
|---|---|---|
| * UMA | 0 | |
| * DIS | 1 | |
| * 14" | | 0 |
| * 15" | | 1 |



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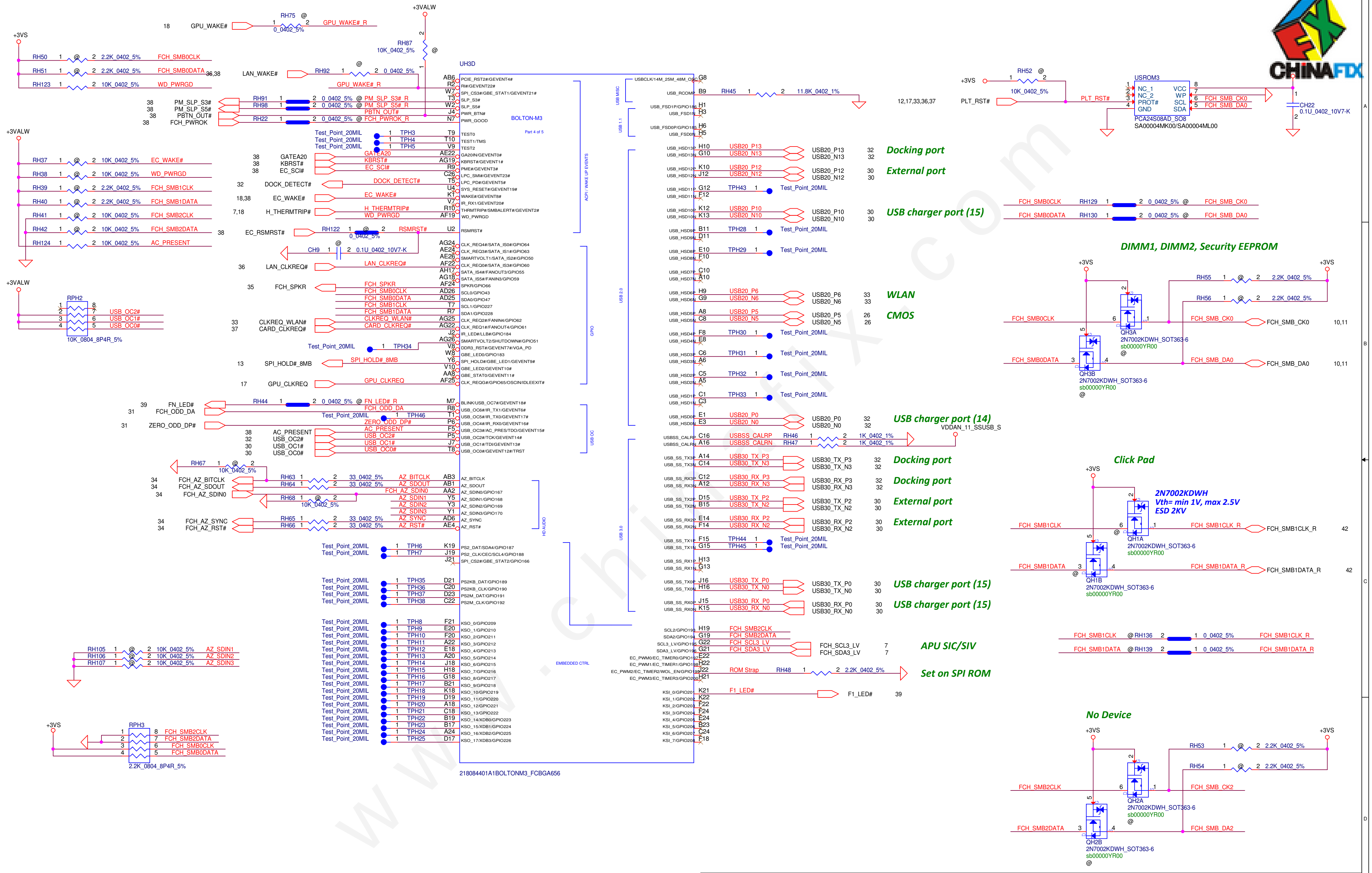
Title
FCH SATA/GBE/SPI

Size Custom
Document Number NM-A241
Rev 0.2
Date: Friday, June 13, 2014
Sheet 13 of 65



Security Classification | LC Future Center Secret Data

Issued Date 2012/07/01 Deciphered Date 2014/07/01

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Title
**FCH ACPI/USB/GPIO**

Size Custom
Document Number **NM-A241**
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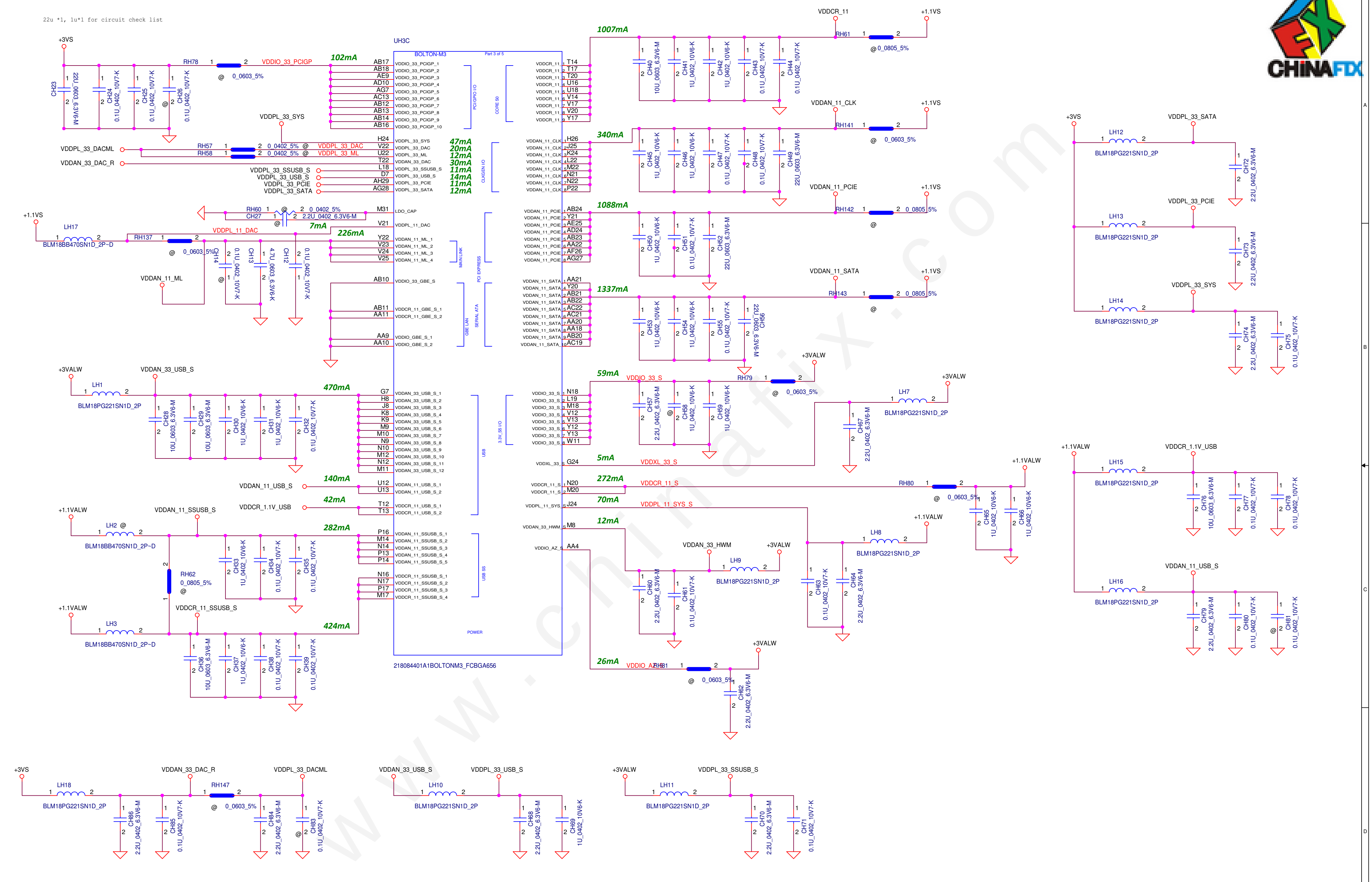
Date: Friday, June 13, 2014 Sheet 14 of 65

22u *1, 1u*1 for circuit check list



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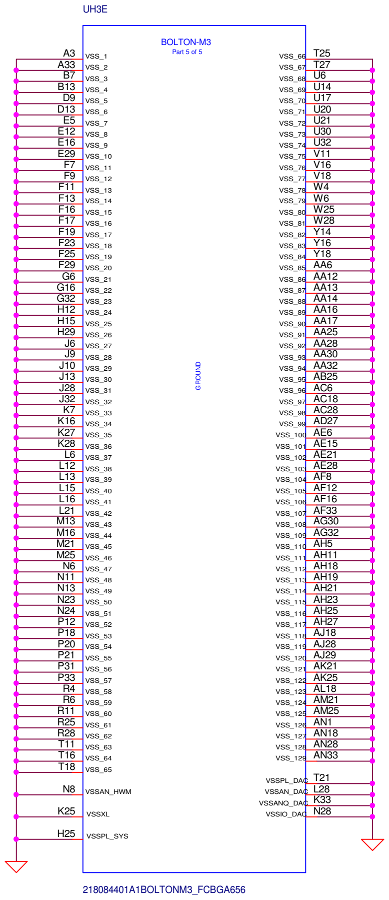
Title
**FCH POWER/GND**

Size Custom
Document Number **NM-A241**
Rev 0.2
Date: Friday, June 13, 2014
Sheet 15 of 65



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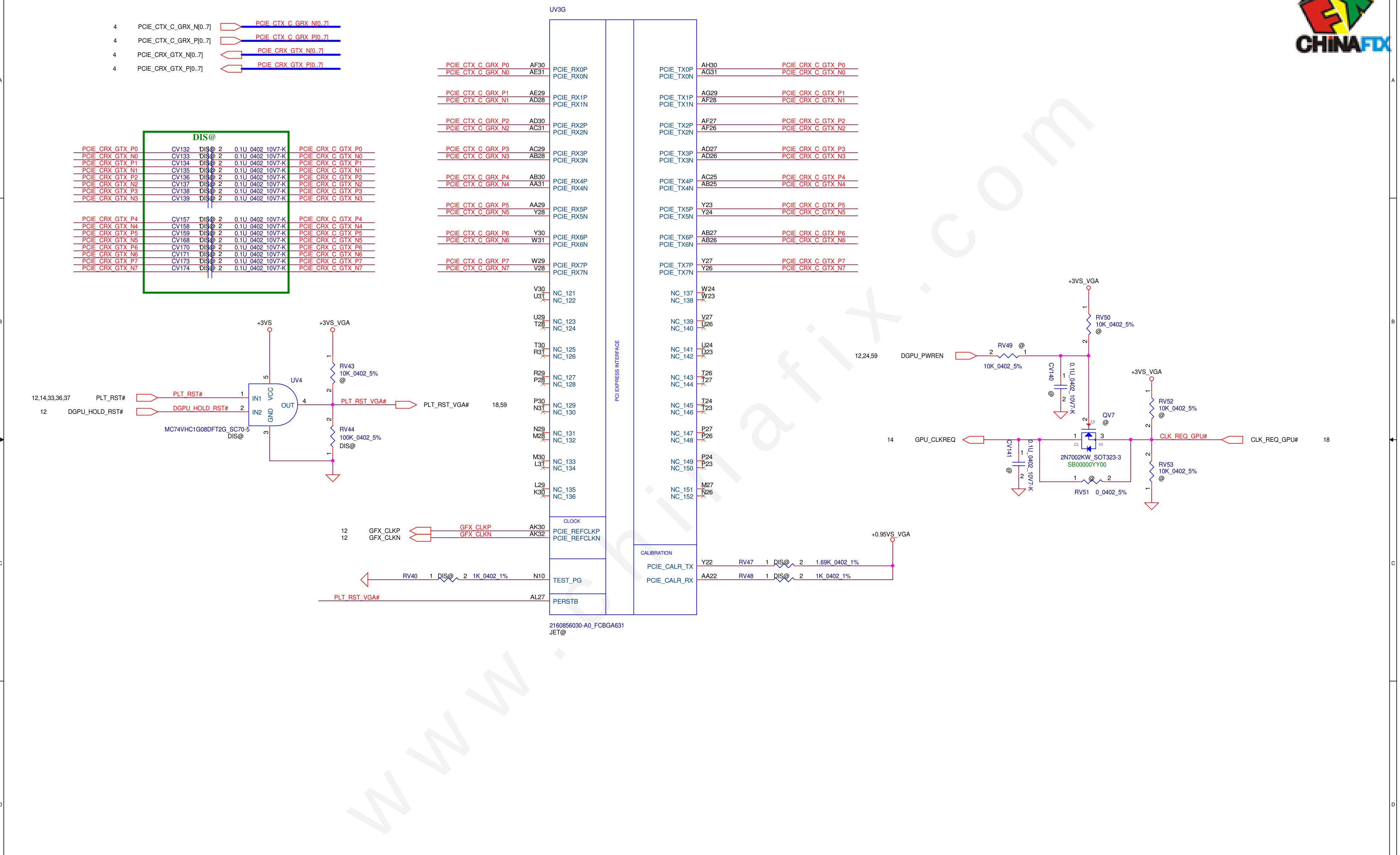
Title
**FCH GND**

LCFC

Size
Custom
Document Number
**NM-A241**
Rev
0.2

Date: Friday, June 13, 2014
Sheet 16 of 65



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| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

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Title

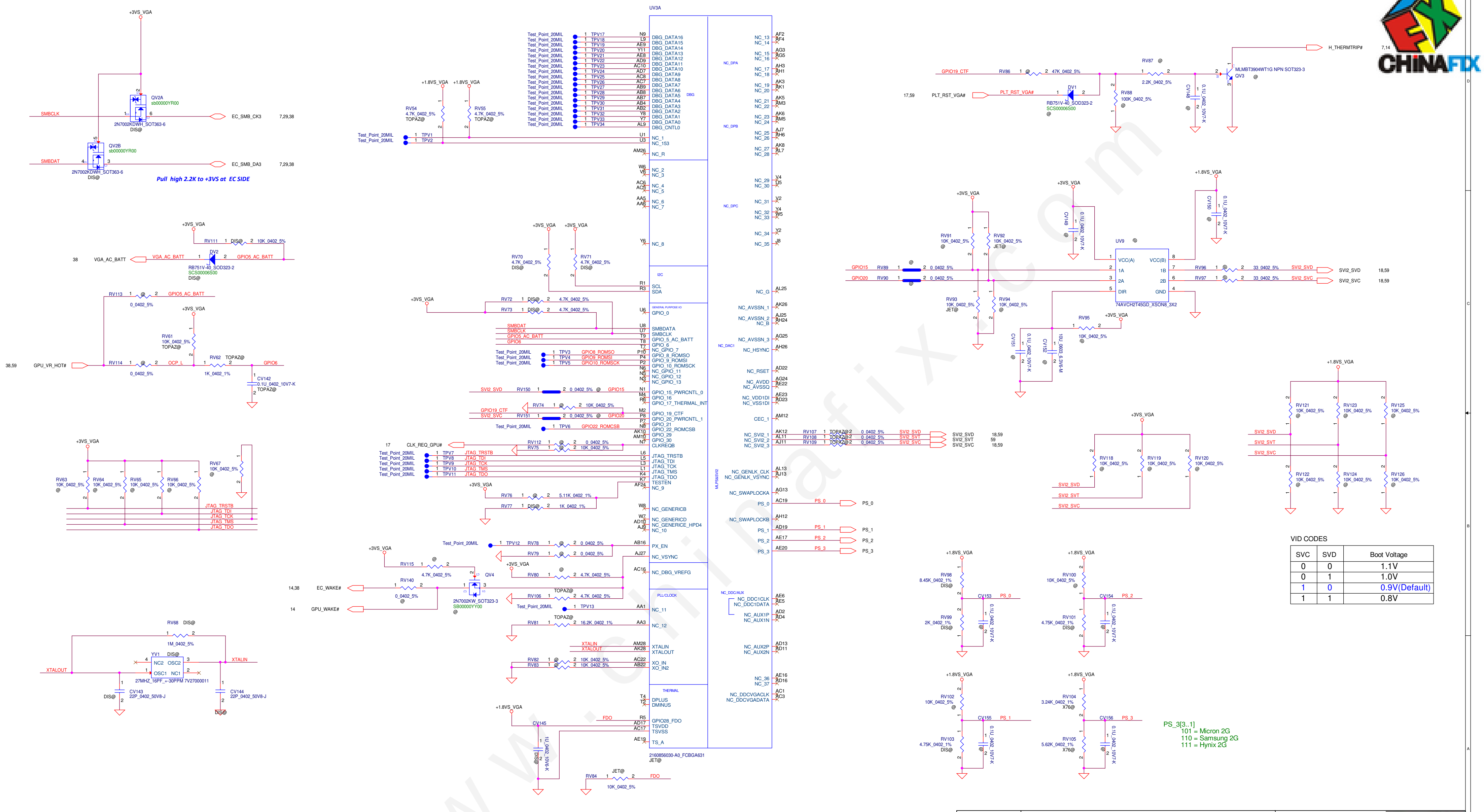
**Topaz & Jet PCIE**

Size Custom

Document Number **NM-A241**

Rev 0.2

Date: Friday, June 13, 2014 Sheet 17 of 65



VID CODES

| SVC | SVD | Boot Voltage |
|---|---|---|
| 0 | 0 | 1.1V |
| 0 | 1 | 1.0V |
| 1 | 0 | 0.9V(Default) |
| 1 | 1 | 0.8V |

PS_3[3..1]
101 = Micron 2G
110 = Samsung 2G
111 = Hynix 2G

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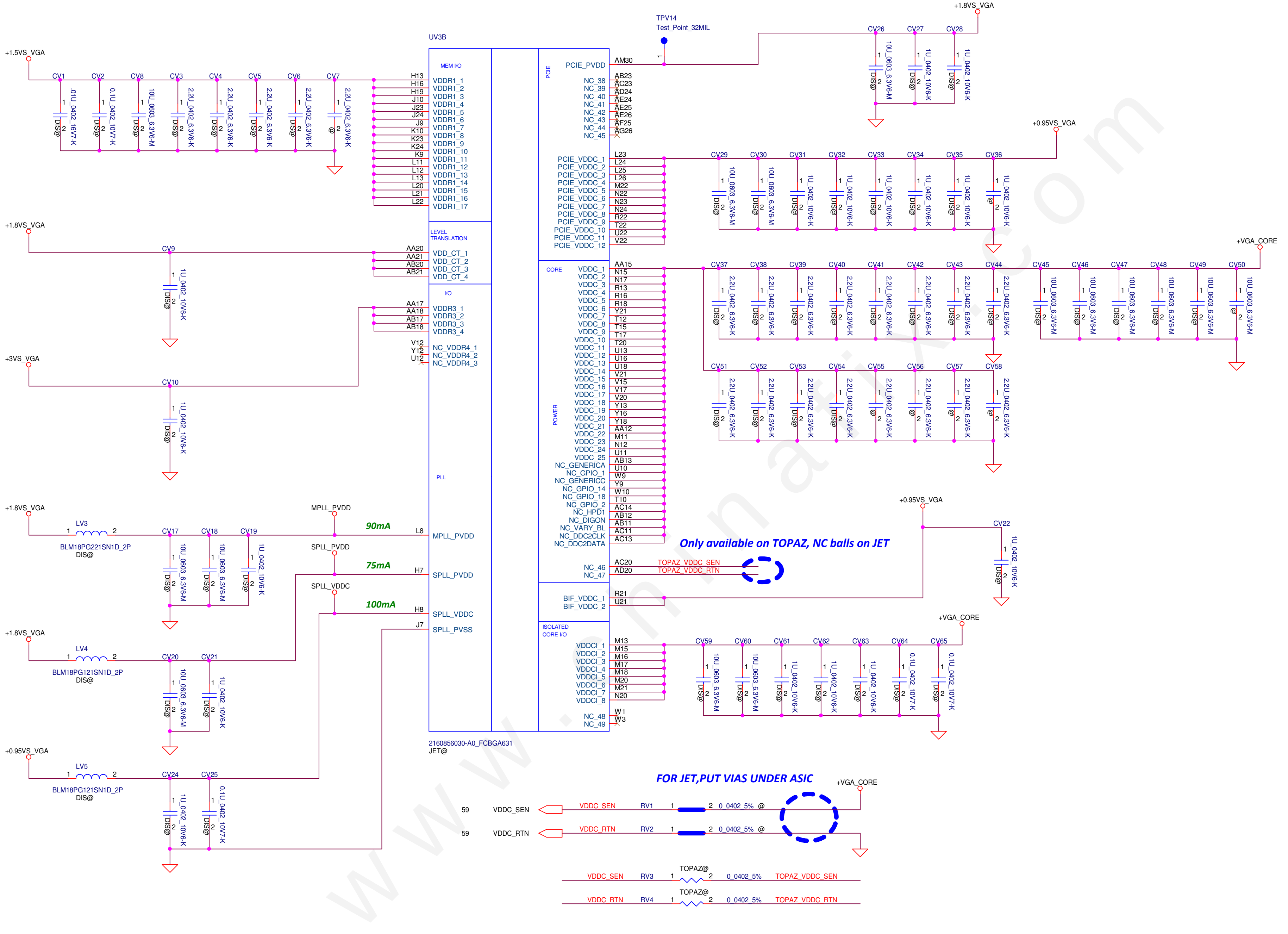
Title
**Topaz & Jet GPIO**

Size Custom
Document Number NM-A241
Rev 0.2
Date: Friday, June 13, 2014
Sheet 18 of 65



UV3B
+1.5VS_VGA
CV1 CV2 CV8 CV3 CV4 CV5 CV6 CV7
.01U_0402_16V7-K
0.1U_0402_10V7-K
10U_0603_6.3V6-M
22U_0402_6.3V6-K
MEM I/O
H13 H16 H19 J10 J23 J24 J9 K10 K23 K24 K9 L11 L12 L13 L20 L21 L22
VDDR1_1 … VDDR1_17
+1.8VS_VGA
CV9
1U_0402_10V6-K
LEVEL TRANSLATION
AA20 AA21 AB20 AB21
VDD_CT_1 VDD_CT_2 VDD_CT_3 VDD_CT_4
I/O
AA17 AA18 AB17 AB18
VDDR3_1 VDDR3_2 VDDR3_3 VDDR3_4
V12 Y12 U12
NC_VDDR4_1 NC_VDDR4_2 NC_VDDR4_3
+3VS_VGA
CV10
PLL
+1.8VS_VGA
LV3
BLM18PG221SN1D_2P
DIS@
MPLL_PVDD
90mA
L8 MPLL_PVDD
CV17 CV18 CV19
SPLL_PVDD
75mA
H7 SPLL_PVDD
SPLL_VDDC
100mA
H8 SPLL_VDDC
J7 SPLL_PVSS
LV4
BLM18PG121SN1D_2P
CV20 CV21
+0.95VS_VGA
LV5
CV24 CV25
0.1U_0402_10V7-K
2160856030-A0_FCBGA631
JET@
TPV14
Test_Point_32MIL
PCIE
PCIE_PVDD AM30
NC_38 … NC_45
AB23 AC23 AD24 AE24 AE25 AE26 AF25 AG26
+1.8VS_VGA
CV26 CV27 CV28
10U_0603_6.3V6-M
1U_0402_10V6-K
+0.95VS_VGA
PCIE_VDDC_1 … PCIE_VDDC_12
L23 L24 L25 L26 M22 N22 N23 N24 R22 T22 U22 V22
CV29 CV30 CV31 CV32 CV33 CV34 CV35 CV36
CORE
VDDC_1 … VDDC_25
AA15 N15 N17 R13 R16 R18 Y21 T12 T15 T17 T20 U13 U16 U18 V21 V15 V17 V20 Y13 Y16 Y18 AA12 M11 N12 U11
POWER
NC_GENERICA NC_GPIO_1 NC_GENERICC NC_GPIO_14 NC_GPIO_18 NC_GPIO_2 NC_HPD1 NC_DIGON NC_VARY_BL NC_DDC2CLK NC_DDC2DATA
AB13 U10 W9 Y9 W10 T10 AC14 AB12 AB11 AC11 AC13
+VGA_CORE
CV37 CV38 CV39 CV40 CV41 CV42 CV43 CV44 CV45 CV46 CV47 CV48 CV49 CV50
CV51 CV52 CV53 CV54 CV55 CV56 CV57 CV58
22U_0402_6.3V6-K
10U_0603_6.3V6-M
NC_46 AC20 TOPAZ_VDDC_SEN
NC_47 AD20 TOPAZ_VDDC_RTN
+0.95VS_VGA
CV22
BIF_VDDC_1 R21
BIF_VDDC_2 U21
ISOLATED CORE I/O
VDDCI_1 … VDDCI_8
M13 M15 M16 M17 M18 M20 M21 N20
NC_48 W1
NC_49 W3
+VGA_CORE
CV59 CV60 CV61 CV62 CV63 CV64 CV65
59 VDDC_SEN
59 VDDC_RTN
VDDC_SEN RV1 2 0_0402_5% @
VDDC_RTN RV2 2 0_0402_5% @
+VGA_CORE
TOPAZ@
VDDC_SEN RV3 0_0402_5% TOPAZ_VDDC_SEN
TOPAZ@
VDDC_RTN RV4 0_0402_5% TOPAZ_VDDC_RTN

*Only available on TOPAZ, NC balls on JET*

*FOR JET,PUT VIAS UNDER ASIC*

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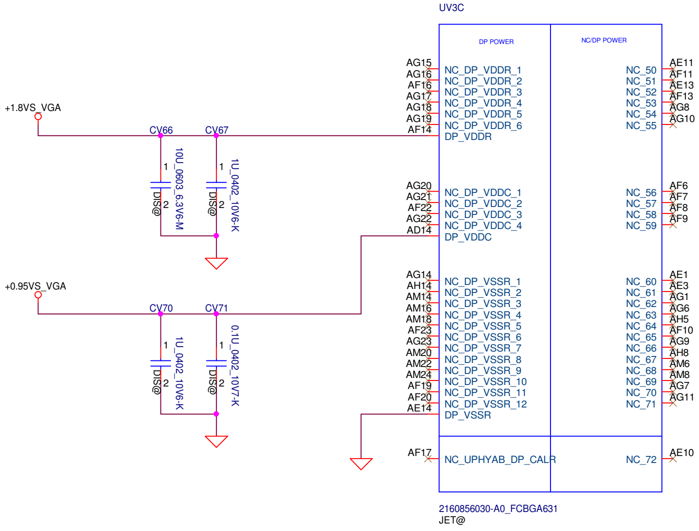
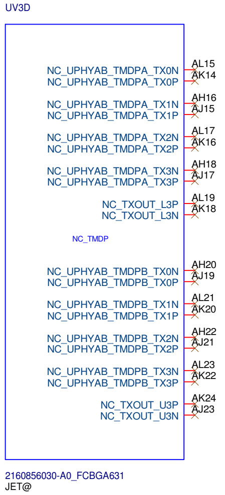
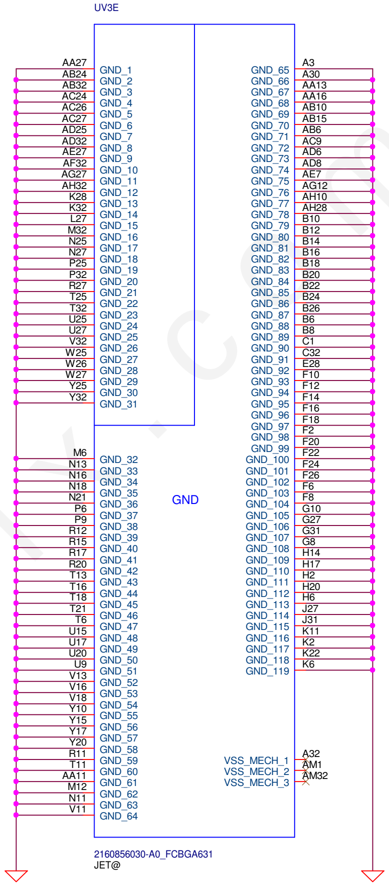
Title
**Topaz & Jet Core Power**

Size Custom
Document Number **NM-A241**
Rev 0.2
Date: Friday, June 13, 2014




UV3D
NC_UPHYAB_TMDPA_TX0N AL15
NC_UPHYAB_TMDPA_TX0P AK14
NC_UPHYAB_TMDPA_TX1N AH16
NC_UPHYAB_TMDPA_TX1P AJ15
NC_UPHYAB_TMDPA_TX2N AL17
NC_UPHYAB_TMDPA_TX2P AK16
NC_UPHYAB_TMDPA_TX3N AH18
NC_UPHYAB_TMDPA_TX3P AJ17
NC_TXOUT_L3P AL19
NC_TXOUT_L3N AK18
NC_TMDP
NC_UPHYAB_TMDPB_TX0N AH20
NC_UPHYAB_TMDPB_TX0P AJ19
NC_UPHYAB_TMDPB_TX1N AL21
NC_UPHYAB_TMDPB_TX1P AK20
NC_UPHYAB_TMDPB_TX2N AH22
NC_UPHYAB_TMDPB_TX2P AJ21
NC_UPHYAB_TMDPB_TX3N AL23
NC_UPHYAB_TMDPB_TX3P AK22
NC_TXOUT_U3P AK24
NC_TXOUT_U3N AJ23
2160856030-A0_FCBGA631
JET@



| ASIC Ball | Topaz | Jet |
|---|---|---|
| U10,T10<br>AB13,W9<br>AB11,AB12<br>AC11,AC13<br>AC14,Y9,W10 | VDDC | NC |
| AC20 | FB_VDDC | NC |
| AD20 | FB_VSS | NC |
| W1 | FB_VDDCI | NC |
| W3 | FB_VSS | NC |
| AJ11 | GPIO_SVC | NC_SVI2 |
| AK12 | GPIO_SVD | NC_SVI2 |
| AL11 | GPIO_SVT | NC_SVI2 |
| N6 | GPIO_11 | NC_GPIO11 |
| N5 | GPIO_12 | NC_GPIO12 |
| N3 | GPIO_13 | NC_GPIO13 |
| AJ27 | WAKEB | NC_VSYNC |
| T8 | PCC/GPIO_6 | GPIO_6 |
| AA3 | PLL_ANALOG_OUT | NC |
| AA1 | PLL_ANALOG_IN | NC |

| ASIC Ball | Topaz | Jet |
|---|---|---|
| U1 | BP_0 | NC |
| U3 | BP_1 | NC |
| AM26 | DIECRACKMON | NC |
| Y11 | NC | DBG_DATA13 |
| AE9 | NC | DBG_DATA14 |
| L9 | NC | DBG_DATA15 |
| N9 | NC | DBG_DATA16 |
| AE8 | NC | DBG_DATA12 |
| AL9 | NC | DBG_CNTL0 |
| H13,H16,H19,J10<br>J23,J24,J9,K10<br>K23,K24,K9,L11<br>L12,L13,L20,L21<br>L22 | VMEMIO | VDDR1 |
| AA17,AA18<br>AB17,AB18 | VDD_GPIO33 | VDDR3 |
| AA20,AA21<br>AB20,AB21 | VDD_GPIO18 | VDD_CT |

| | | | |
|---|---|---|---|
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Title
**Topaz & Jet DP Power/GND**
Size Custom
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Date: Friday, June 13, 2014
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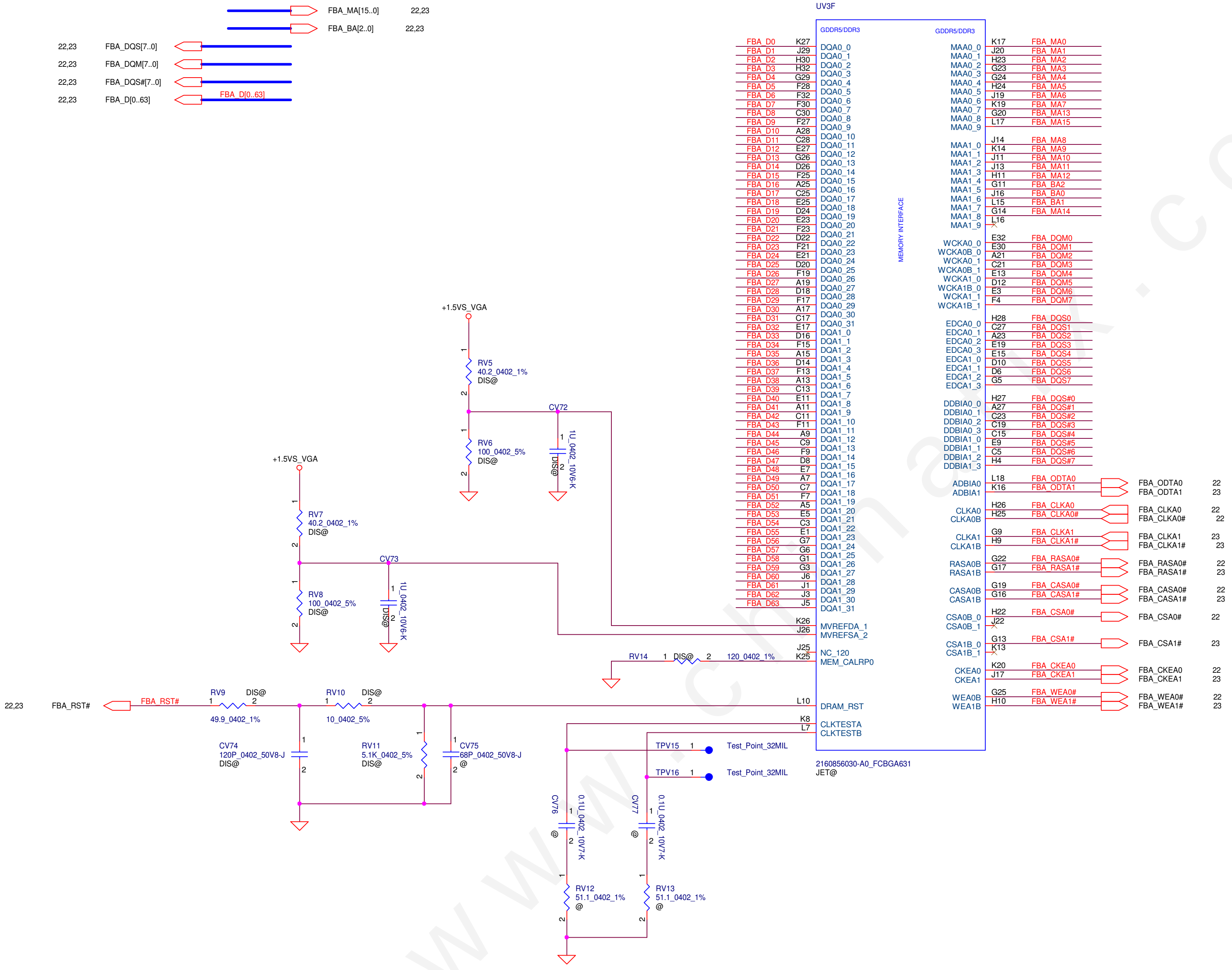

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|---|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 | Topaz & Jet MEM Interface |

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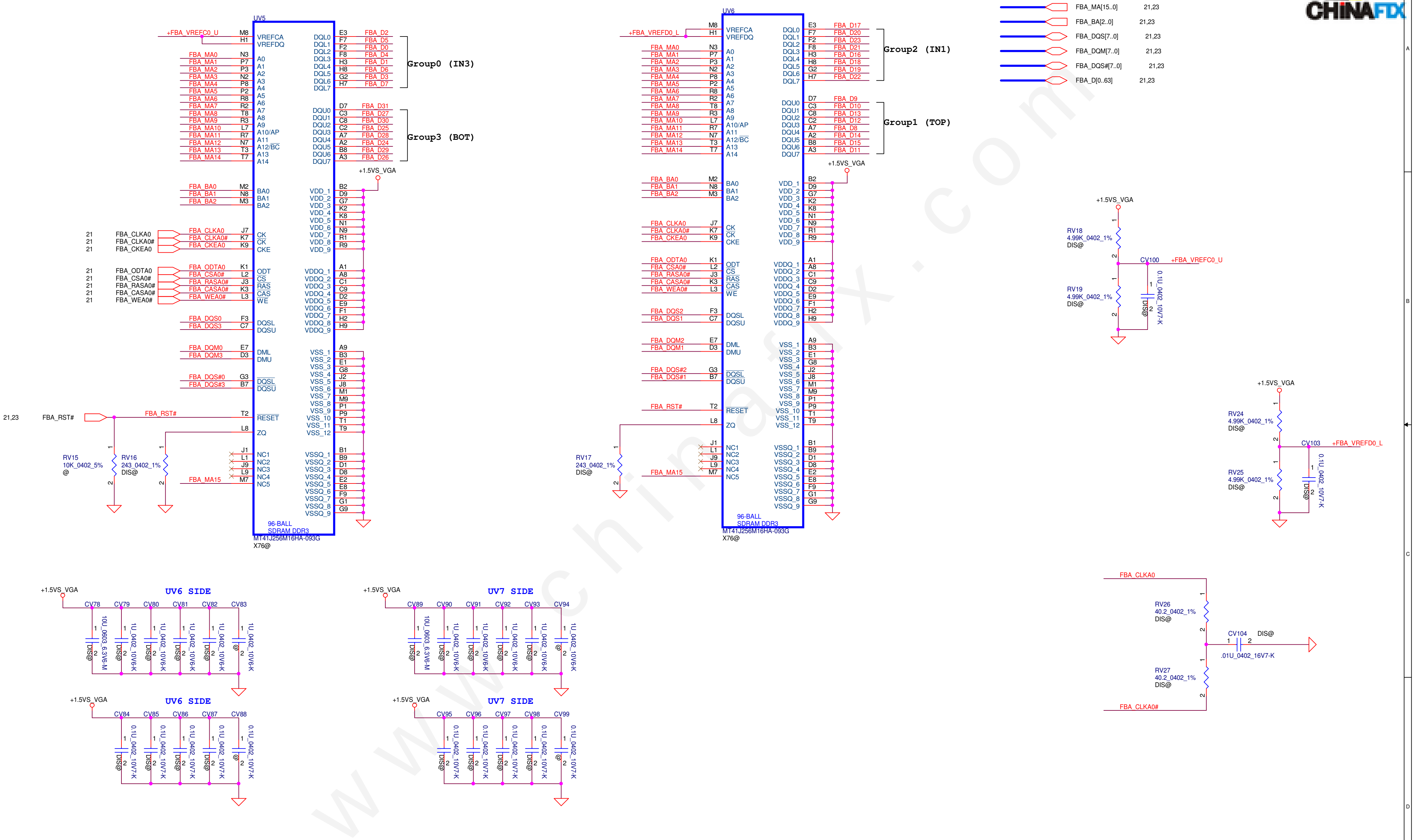
| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A241 | 0.2 |

Date: Friday, June 13, 2014 Sheet 21 of 65

# Memory Partition A - Lower 32 bits



| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

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Title
Topaz & Jet DDR3 VRAM 0

Size Custom
Document Number NM-A241
Rev 0.2
Date: Friday, June 13, 2014
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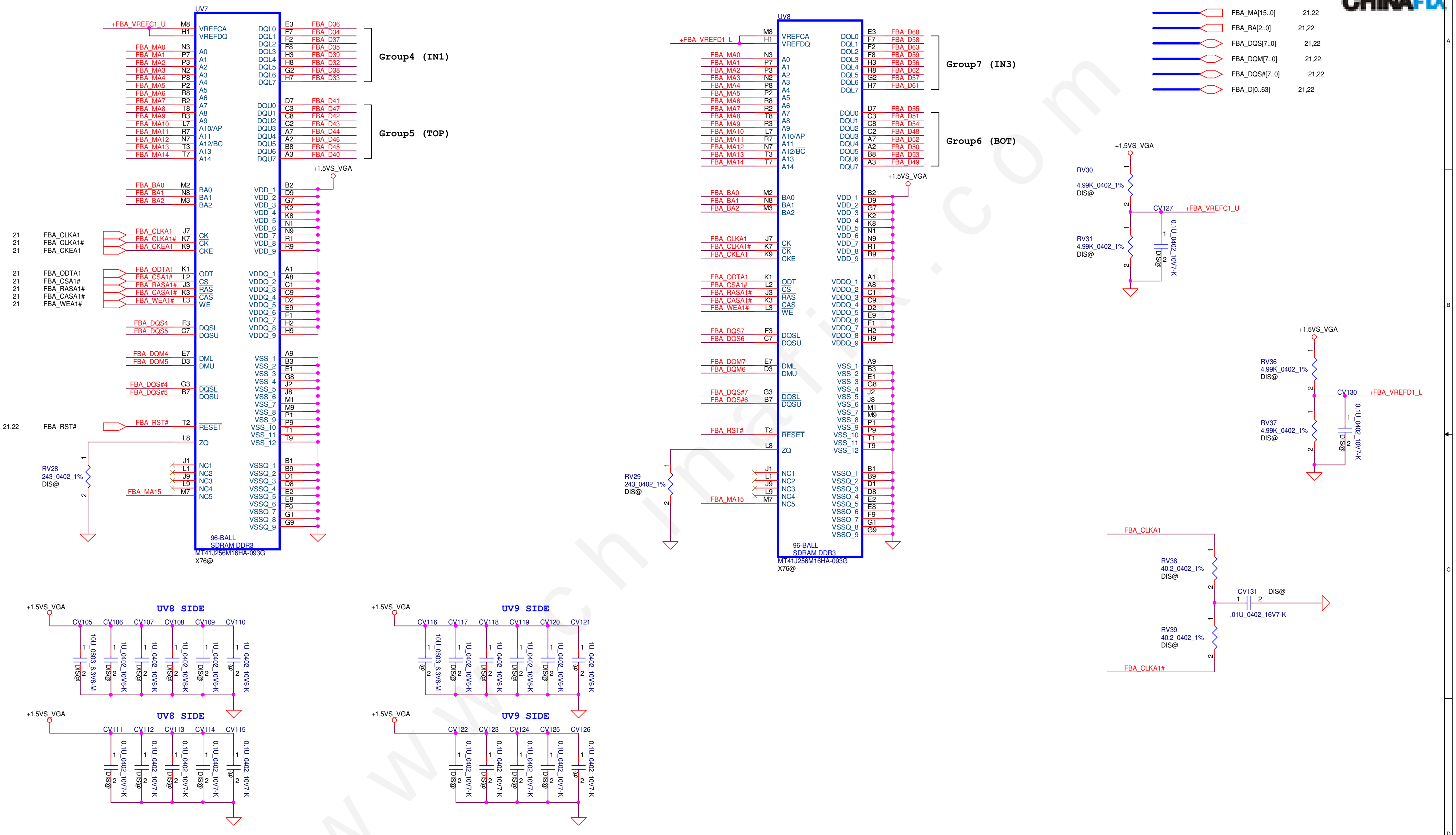
# Memory Partition A - Upper 32 bits



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|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

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Title
Topaz & Jet DDR3 VRAM 1

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A241 | 0.2 |

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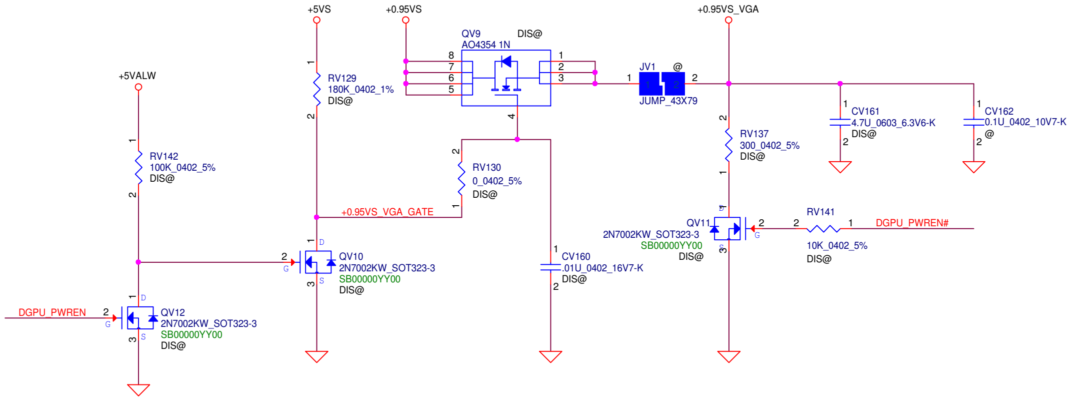
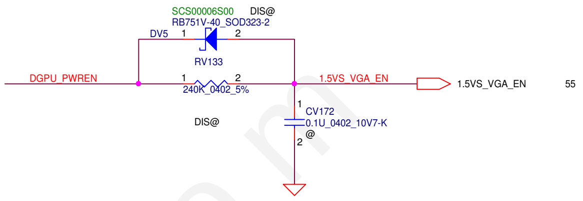
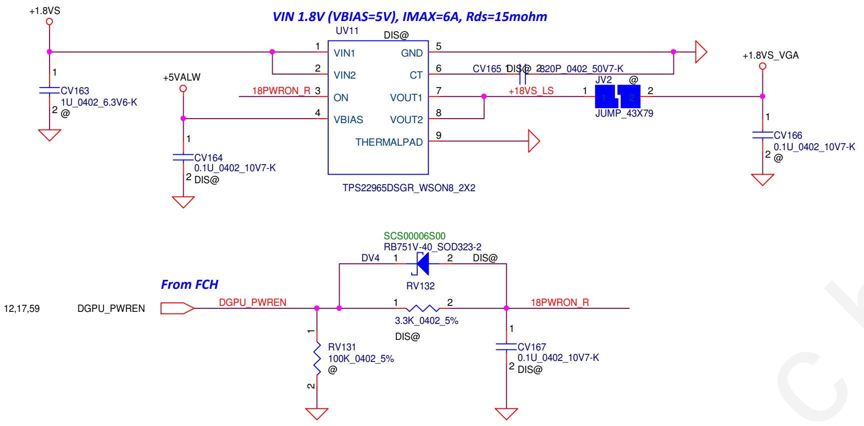
# +0.95VS to +0.95VS_VGA



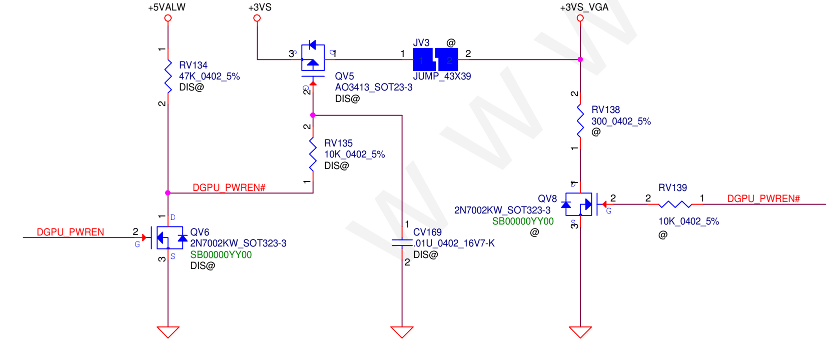
# +1.5VS to +1.5VS_VGA

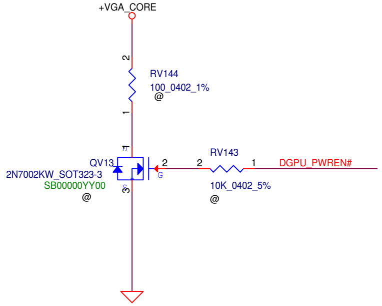


# +1.8VS to +1.8VS_VGA



# +3VS to +3VS_VGA





| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

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Title
Topaz & Jet SWITCH POWER
Size: Custom
Document Number: NM-A241
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| | | |
|---|---|---|
| PS_0[1]<br>PS_0[2]<br>PS_0[3] | ROM_CONFIG[0]<br>ROM_CONFIG[1]<br>ROM_CONFIG[2] | STRAP_BIOS_ROM_EN = 1<br>ROM_CONFIG[2:0] = [001]  256MB |
| PS_0[4] | N/A | 1  (Default) |
| PS_0[5] | N/A | 1  (Default) |
| PS_1[1] | STRAP_BIF_GEN3_EN_A | 0 = PCIe GEN3 is not supported |
| PS_1[2] | STRAP_BIF_CLK_PM_EN | 0 = The CLKREQB power management capability is disabled |
| PS_1[3] | N/A | 0  (Default) |
| PS_1[4] | STRAP_TX_CFG_DRV_FULL_SWING | 1 = The transmitter full-swing is enabled |
| PS_1[5] | STRAP_TX_DEEMPH_EN | 1 = Tx deemphasis enabled |
| PS_2[1] | N/A | 0  (Default) |
| PS_2[2] | N/A | 0  (Default) |
| PS_2[3] | STRAP_BIOS_ROM_EN | 0 = Disable the external BIOS ROM device |
| PS_2[4] | N/A | 1  (Default) |
| PS_2[5] | N/A | 1  (Default) |
| PS_3[1]<br>PS_3[2]<br>PS_3[3] | BOARD_CONFIG[0]<br>BOARD_CONFIG[1]<br>BOARD_CONFIG[2] | PS_3[3..1]<br>101 = Micron 2G<br>110 = Samsung 2G<br>111 = Hynix 2G |
| PS_3[4] | N/A | 1  (Default) |
| PS_3[5] | N/A | 1  (Default) |

| MLPS | Bit | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| PS_0[5:1] | 1 | 1 | 0 | 0 | 1 |
| PS_1[5:1] | 1 | 1 | 0 | 0 | 0 |
| PS_2[5:1] | 1 | 1 | 0 | 0 | 0 |
| PS_3[5:1] | 1 | 1 | X | X | X |

| | PS_0 | | PS_1 | | PS_2 | | PS_3 | |
|---|---|---|---|---|---|---|---|---|
| | RV98 | RV99 | RV102 | RV103 | RV100 | RV101 | RV104 | RV105 |
| Micron 2G | PU 8.45K | PD 2K | NC | PD 4.75K | NC | PD 4.75K | **PU 3.24K** | **PD 5.62K** |
| Samsung 2G | PU 8.45K | PD 2K | NC | PD 4.75K | NC | PD 4.75K | **PU 3.4K** | **PD 10K** |
| Hynix 2G | PU 8.45K | PD 2K | NC | PD 4.75K | NC | PD 4.75K | **PU 4.75K** | **NC** |

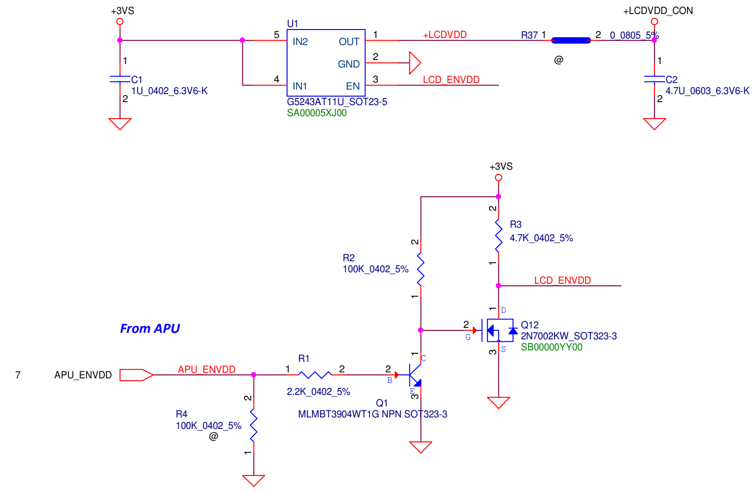
| | |
|---|---|
| 3.24K | SD03432418T |
| 5.62K | SD03456210T |
| 3.4K | SD03434010T |

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/12/05 | Deciphered Date | 2014/12/05 |

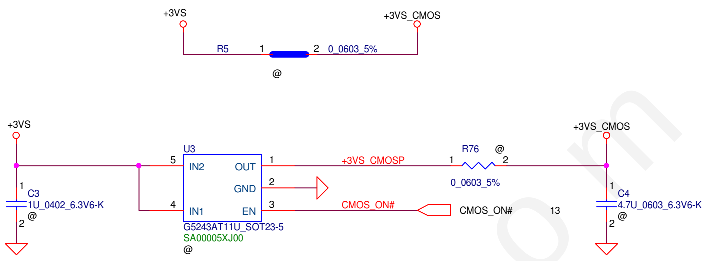
Title
**Topaz & Jet BLANK**

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A241 | 0.2 |

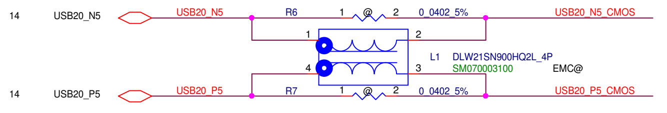
## LCDVDD Circuit

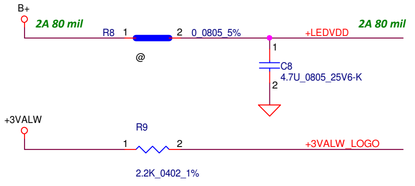


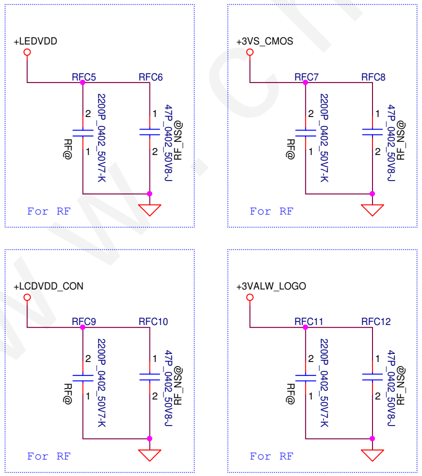
## CMOS Camera

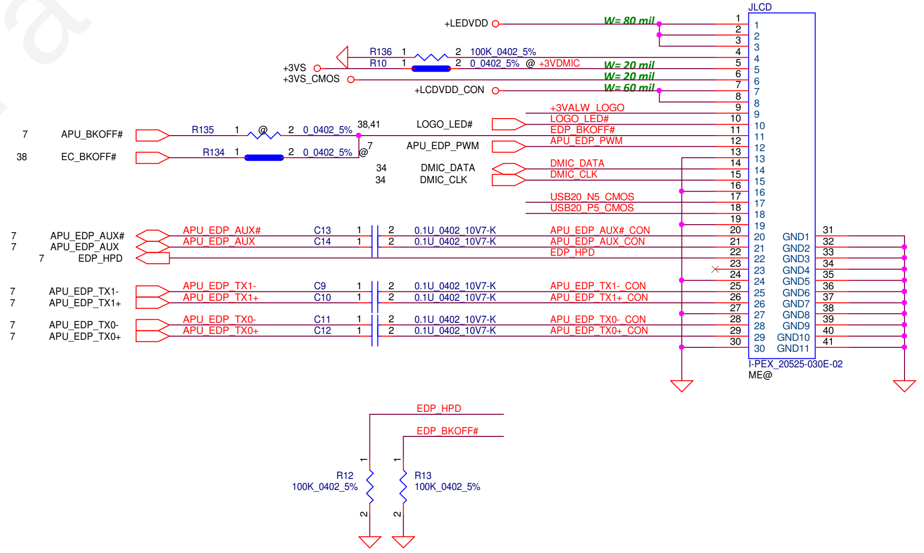


## CMOS USB Port5

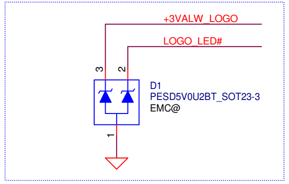








## ESD request



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|---|---|---|---|
| Issued Date | 2012/12/05 | Deciphered Date | 2014/12/05 |

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Title
**LCD/CMOS CONN**

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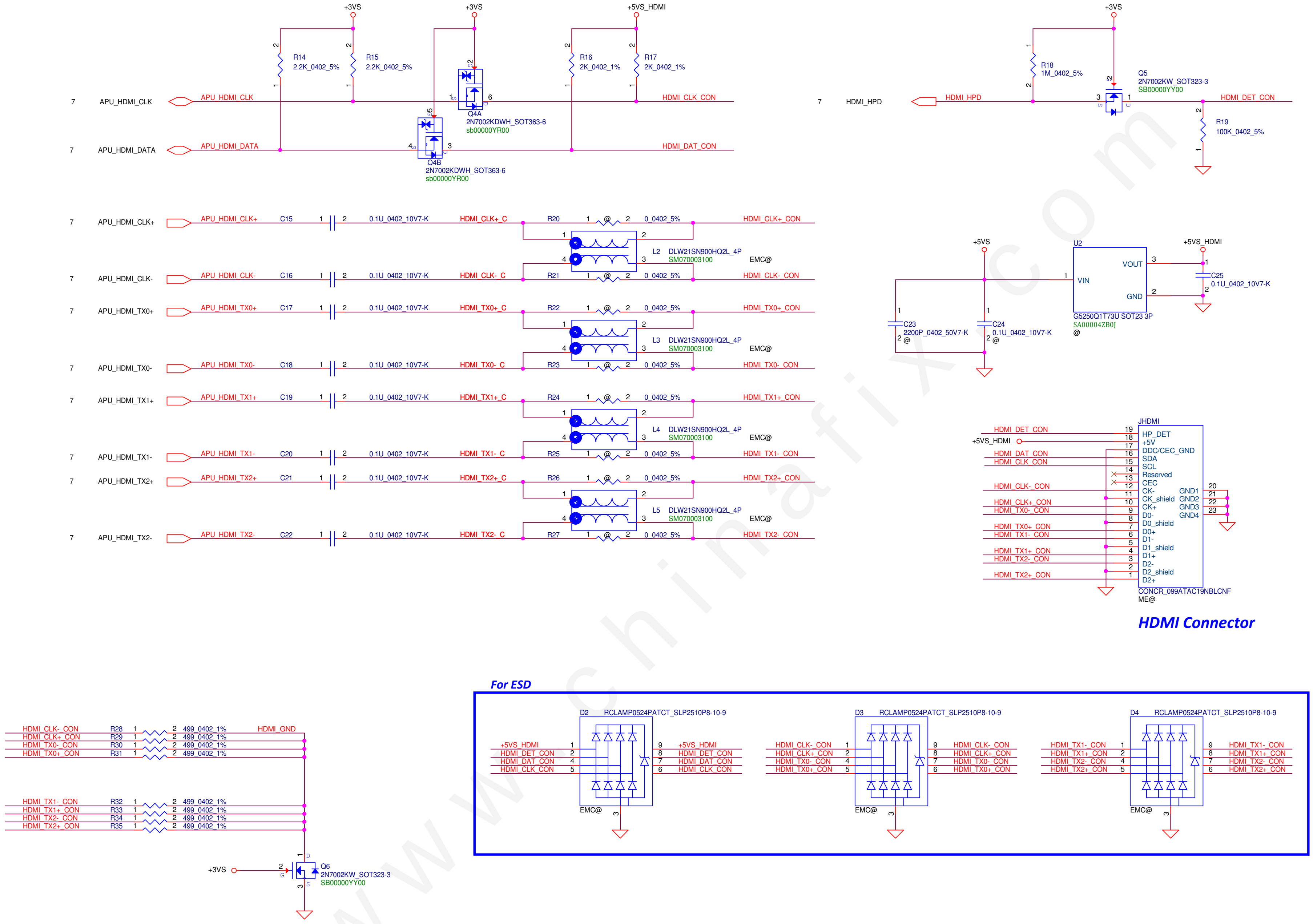
+3VS
+5VS_HDMI
R14 2.2K_0402_5%
R15 2.2K_0402_5%
R16 2K_0402_1%
R17 2K_0402_1%
R18 1M_0402_5%
R19 100K_0402_5%
7 APU_HDMI_CLK
APU_HDMI_CLK
HDMI_CLK_CON
7 APU_HDMI_DATA
APU_HDMI_DATA
HDMI_DAT_CON
Q4A 2N7002KDWH_SOT363-6 sb00000YR00
Q4B 2N7002KDWH_SOT363-6 sb00000YR00
7 HDMI_HPD
HDMI_HPD
HDMI_DET_CON
Q5 2N7002KW_SOT323-3 SB00000YY00
7 APU_HDMI_CLK+
7 APU_HDMI_CLK-
7 APU_HDMI_TX0+
7 APU_HDMI_TX0-
7 APU_HDMI_TX1+
7 APU_HDMI_TX1-
7 APU_HDMI_TX2+
7 APU_HDMI_TX2-
C15 C16 C17 C18 C19 C20 C21 C22 0.1U_0402_10V7-K
HDMI_CLK+_C HDMI_CLK-_C HDMI_TX0+_C HDMI_TX0-_C HDMI_TX1+_C HDMI_TX1-_C HDMI_TX2+_C HDMI_TX2-_C
R20 R21 R22 R23 R24 R25 R26 R27 0_0402_5%
L2 L3 L4 L5 DLW21SN900HQ2L_4P SM070003100 EMC@
HDMI_CLK+_CON HDMI_CLK-_CON HDMI_TX0+_CON HDMI_TX0-_CON HDMI_TX1+_CON HDMI_TX1-_CON HDMI_TX2+_CON HDMI_TX2-_CON
+5VS
U2 G5250Q1T73U SOT23 3P SA00004ZB0J @
VIN VOUT GND
C23 2200P_0402_50V7-K @
C24 0.1U_0402_10V7-K @
C25 0.1U_0402_10V7-K
JHDMI
19 HP_DET
18 +5V
17 DDC/CEC_GND
16 SDA
15 SCL
14 Reserved
13 CEC
12 CK-
11 CK_shield
10 CK+
9 D0-
8 D0_shield
7 D0+
6 D1-
5 D1_shield
4 D1+
3 D2-
2 D2_shield
1 D2+
20 GND1
21 GND2
22 GND3
23 GND4
CONCR_099ATAC19NBLCNF ME@
HDMI Connector
For ESD
D2 D3 D4 RCLAMP0524PATCT_SLP2510P8-10-9 EMC@
R28 R29 R30 R31 R32 R33 R34 R35 499_0402_1%
HDMI_GND
Q6 2N7002KW_SOT323-3 SB00000YY00

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Title
**HDMI CONN**

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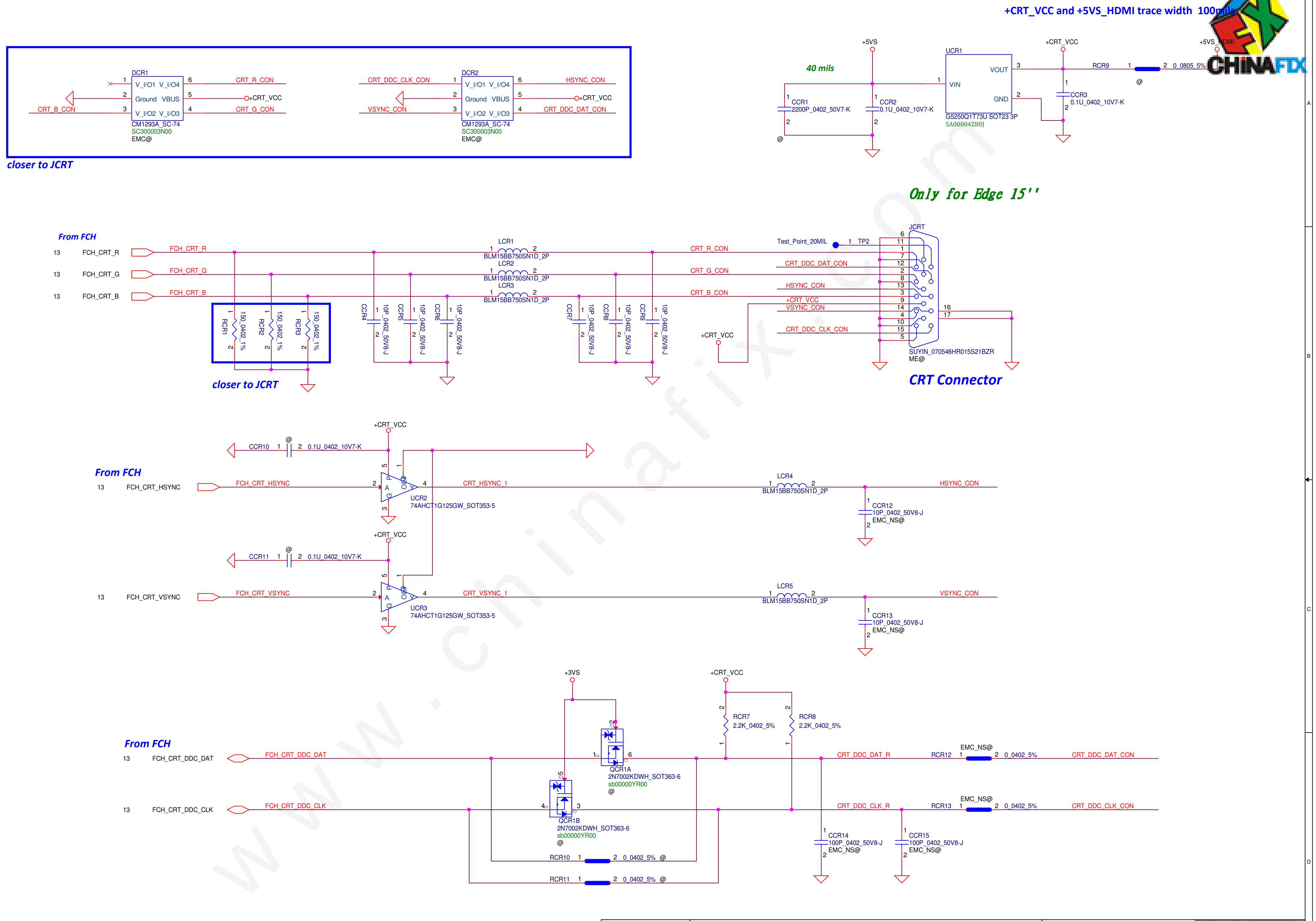

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Title
CRT CONN

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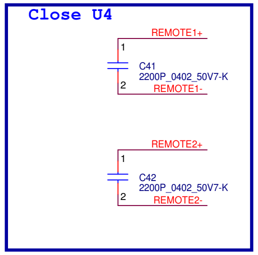
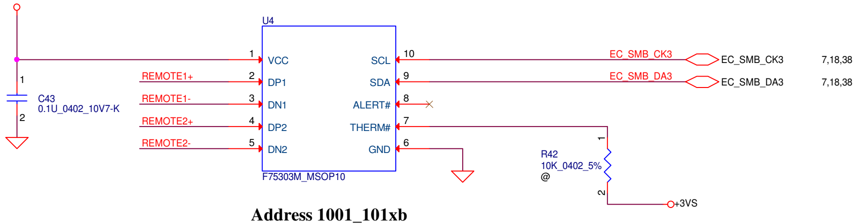
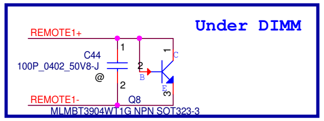


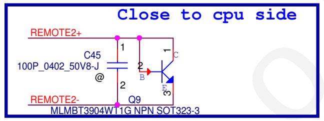
## thermal sensor
## placed near by VRAM



Address 1001_101xb

**internal pull up 1.2K to 1.5V**
**R for initial thermal**
**shutdown temp**





**REMOTE2+/-:**
**Trace width/space:10/10 mil**
**Trace length:<8"**

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|---|---|---|---|---|
| Issued Date | 2012/12/14 | Deciphered Date | 2012/12/21 | *Thermal sensor* |
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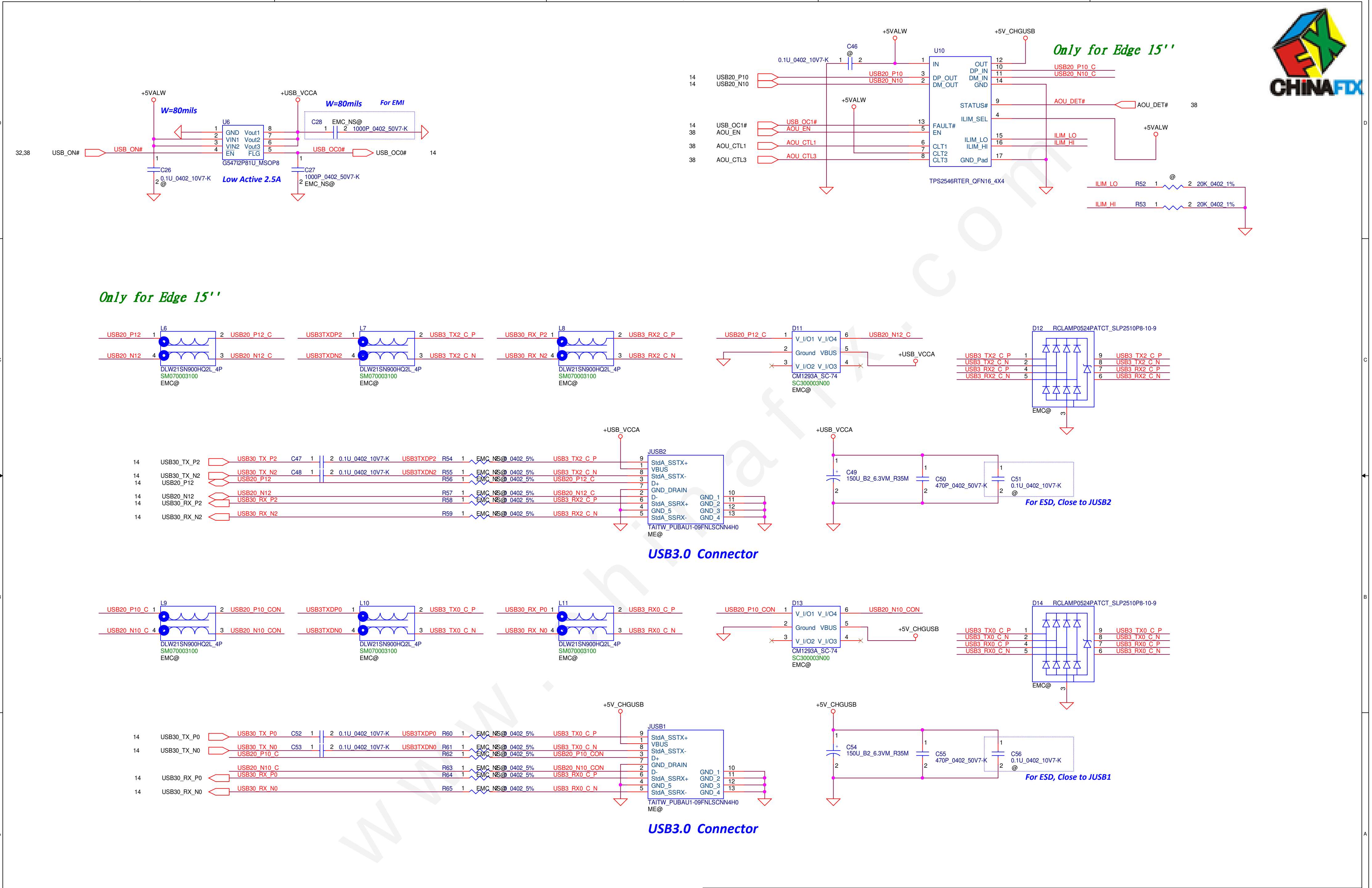

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|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date 2014/07/01 | USB CONN |
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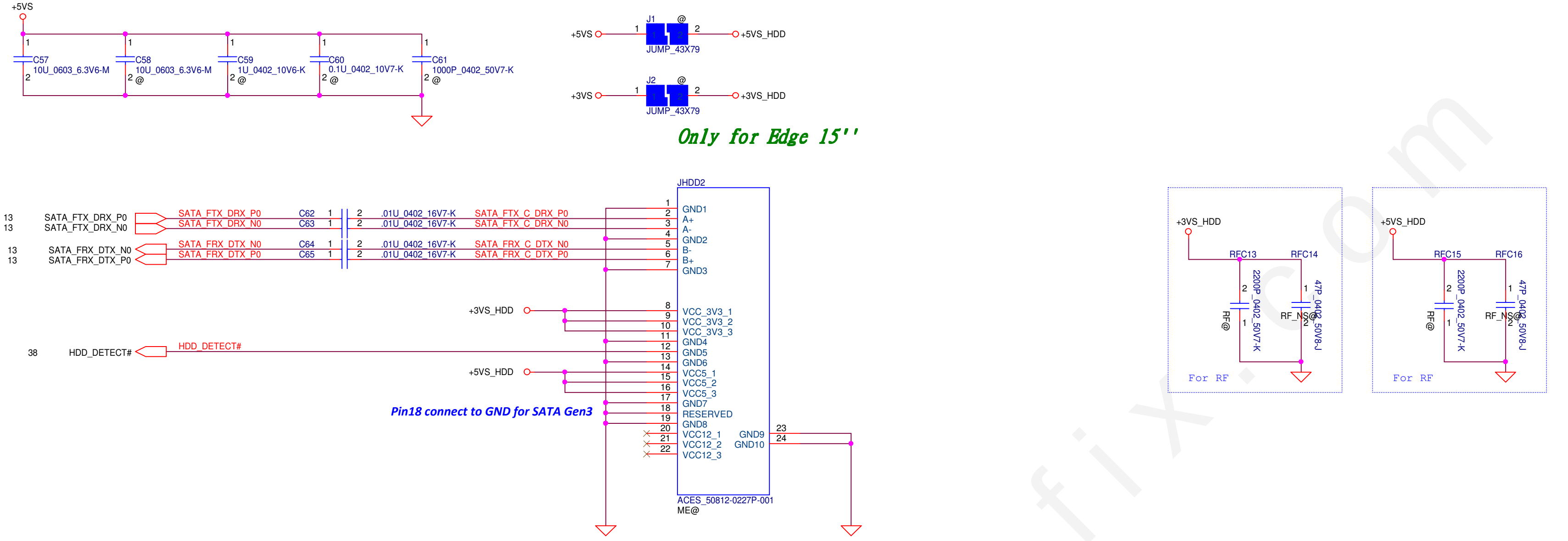
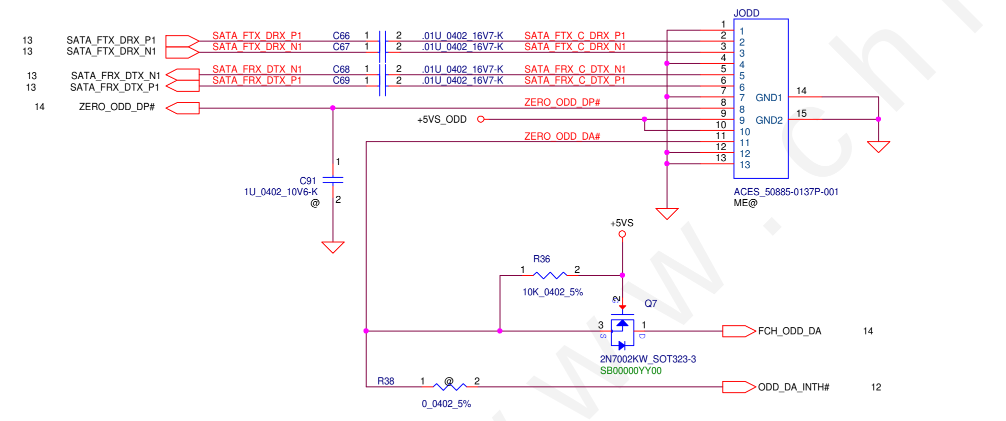
| | | | Date: Friday, June 13, 2014<br>Sheet 30 of 65 |

## SATA HDD



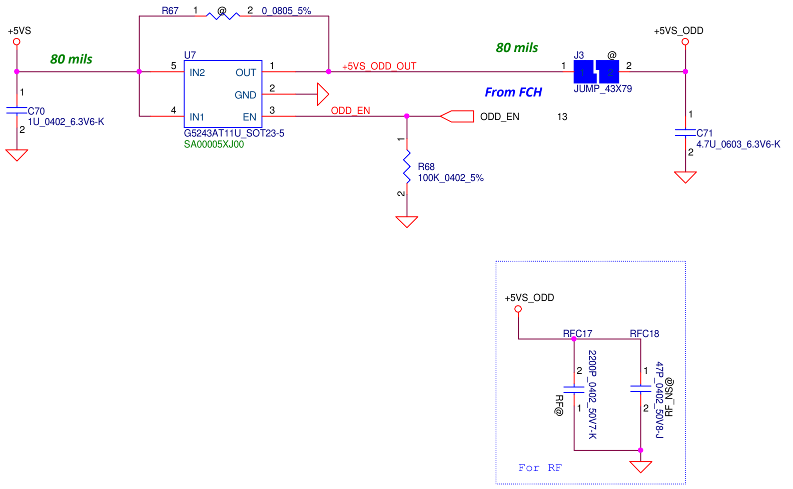
Only for Edge 15''

## SATA ODD & ODD Power Control



Only for Edge 15''

## +5VS TO +5VS_ODD



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Size: Custom
Document Number: NM-A241
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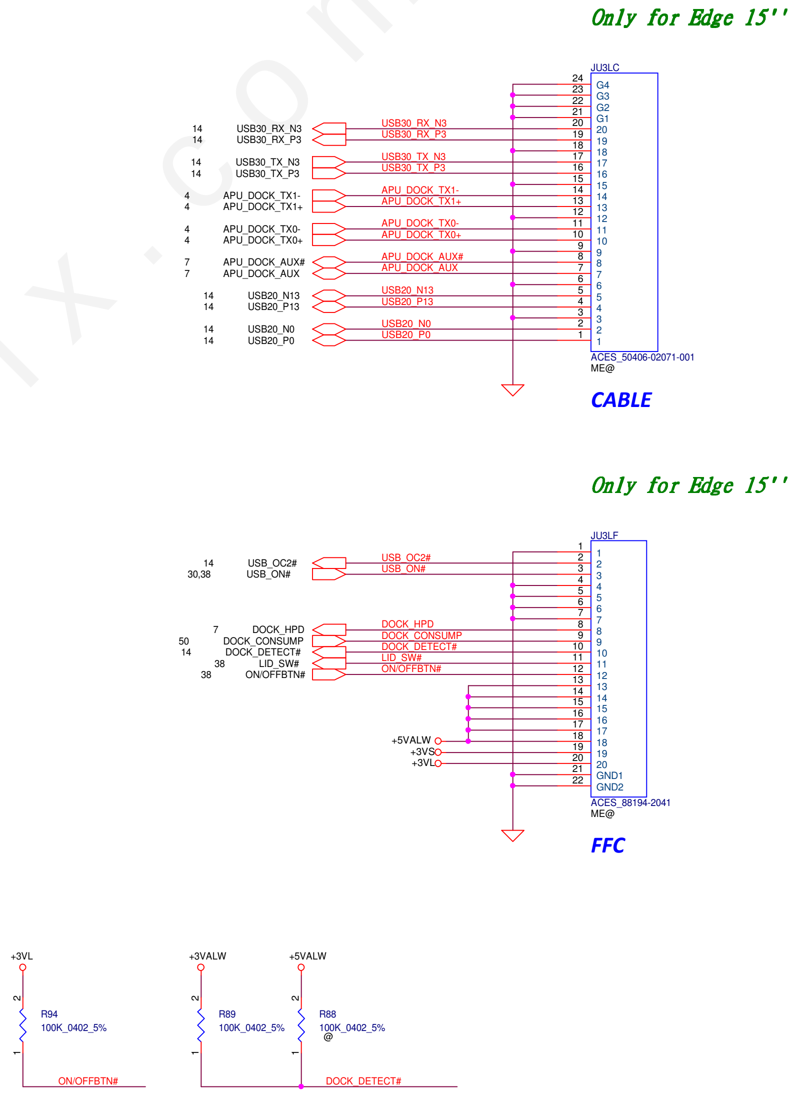

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/12/7 | Deciphered Date | 2014/12/7 |

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Title
One link DP CONN

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A241 | 0.2 |

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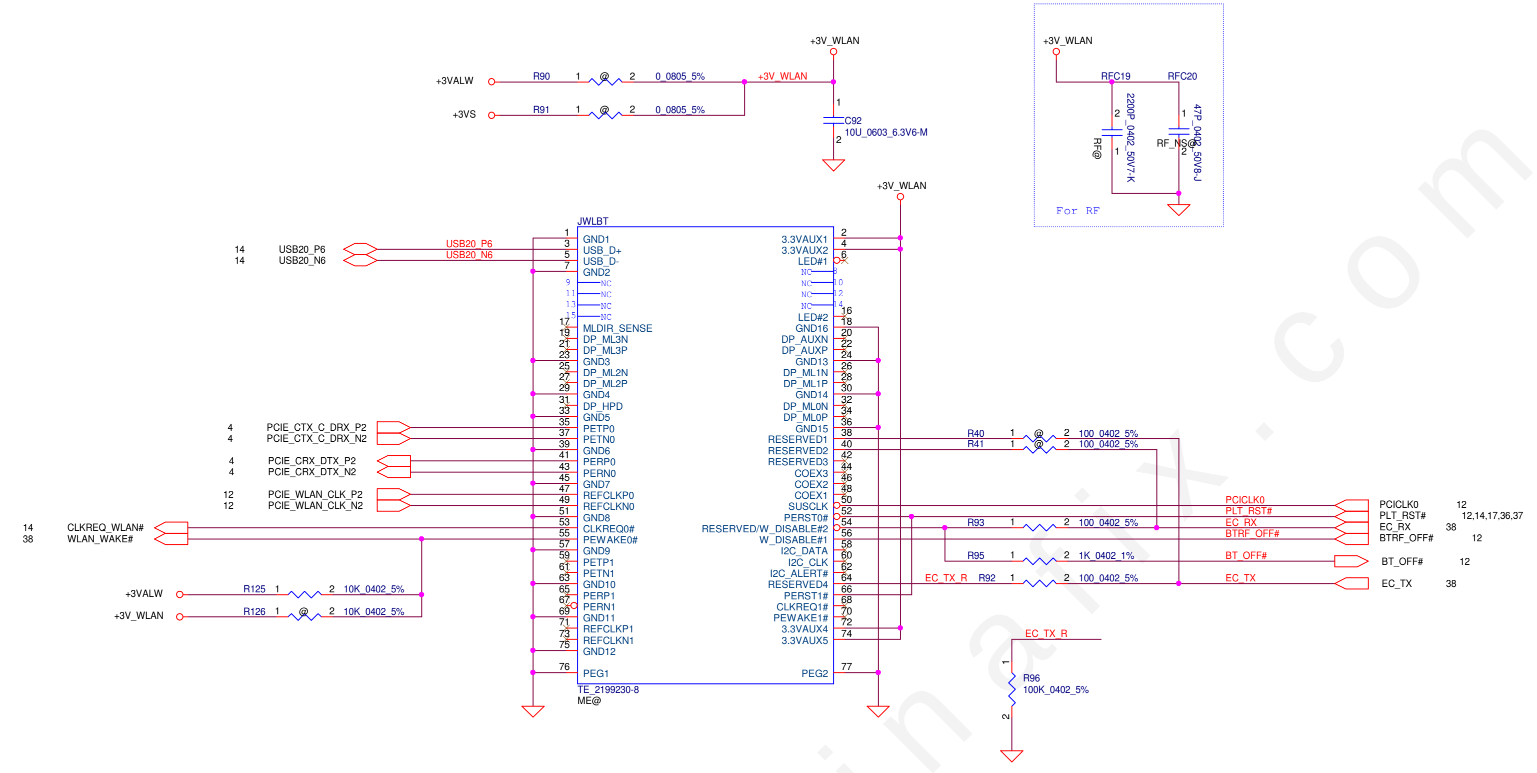
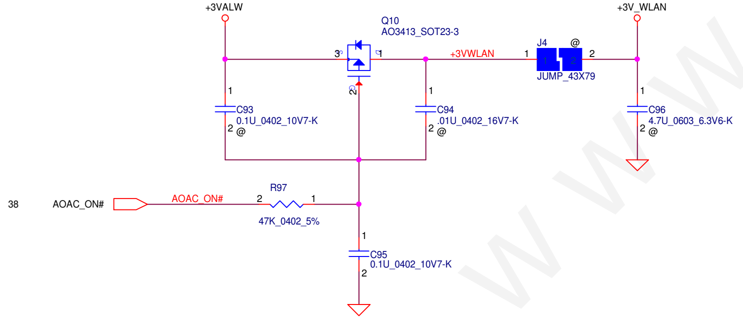
# NGFF typeA Card(WLAN)



1. softstart (RC) will check on EVT PCB
2. if AOAC enable +3V_WLAN always ON
   if AOAC disable +3V_WLAN is same as +3VS

# +3VALW to +3V_WLAN



| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2012/12/05 | Deciphered Date | 2014/12/05 |

Title
NGFF TYPEA WLAN CARD

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A241 | 0.2 |

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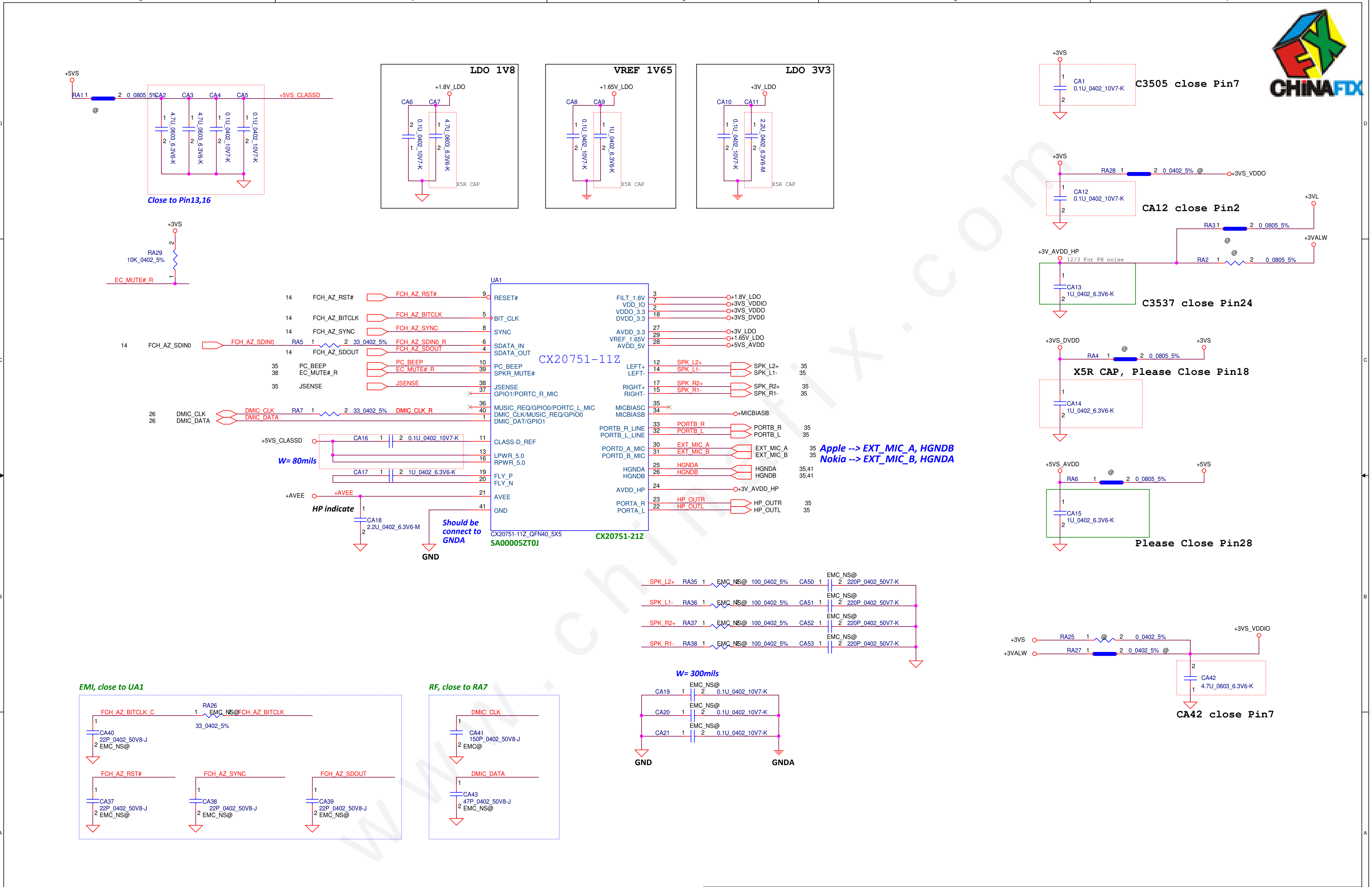

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|---|---|---|---|
| Issued Date | 2012/12/05 | Deciphered Date | 2014/12/05 |

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Title
**HDA-CX20751**

Size Custom
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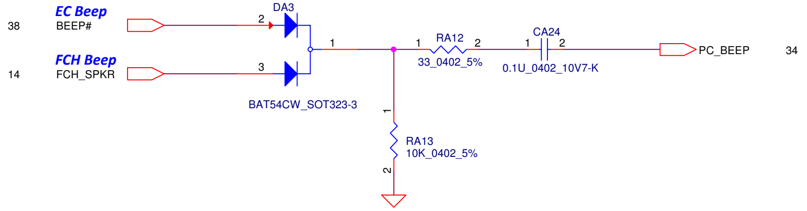
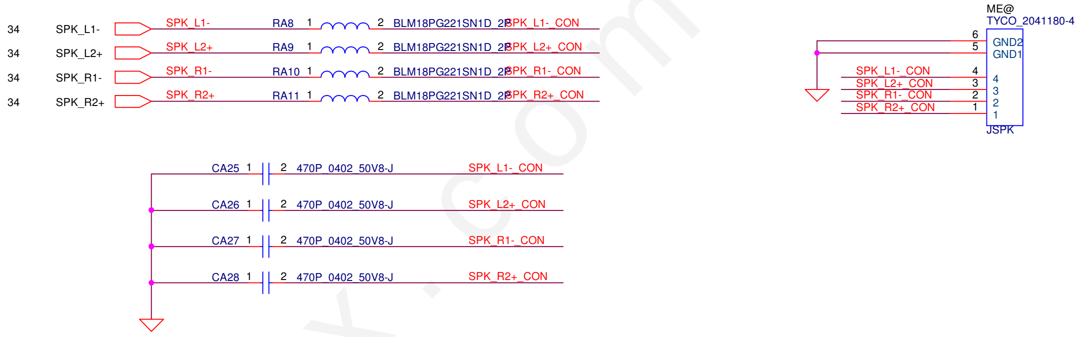
## PC Beep

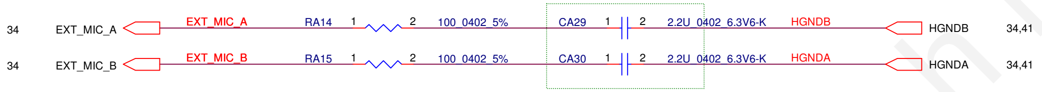


## Speaker

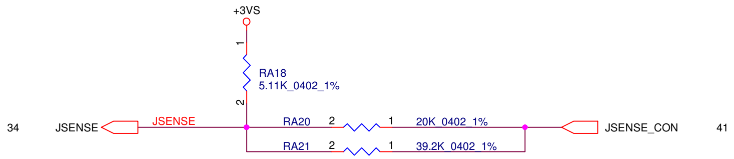

34 SPK_L1- SPK_L1- RA8 1 2 BLM18PG221SN1D_2P SPK_L1-_CON
34 SPK_L2+ SPK_L2+ RA9 1 2 BLM18PG221SN1D_2P SPK_L2+_CON
34 SPK_R1- SPK_R1- RA10 1 2 BLM18PG221SN1D_2P SPK_R1-_CON
34 SPK_R2+ SPK_R2+ RA11 1 2 BLM18PG221SN1D_2P SPK_R2+_CON
ME@
TYCO_2041180-4
6 GND2
5 GND1
SPK_L1-_CON 4 4
SPK_L2+_CON 3 3
SPK_R1-_CON 2 2
SPK_R2+_CON 1 1
JSPK
CA25 1 2 470P_0402_50V8-J SPK_L1-_CON
CA26 1 2 470P_0402_50V8-J SPK_L2+_CON
CA27 1 2 470P_0402_50V8-J SPK_R1-_CON
CA28 1 2 470P_0402_50V8-J SPK_R2+_CON

## EXT. MIC/LINE IN

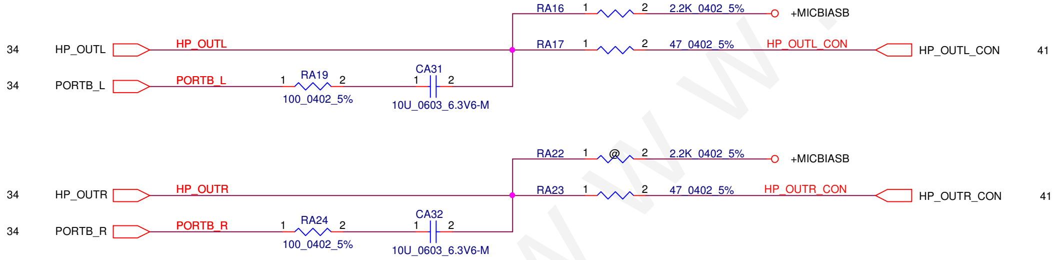
***Apple --> EXT_MIC_A, HGNDB***
***Nokia --> EXT_MIC_B, HGNDA***


34 EXT_MIC_A EXT_MIC_A RA14 1 2 100_0402_5% CA29 1 2 2.2U_0402_6.3V6-K HGNDB HGNDB 34,41
34 EXT_MIC_B EXT_MIC_B RA15 1 2 100_0402_5% CA30 1 2 2.2U_0402_6.3V6-K HGNDA HGNDA 34,41

***Changed CA29 & CA30 from 1uF to 2.2uF/X5R***
***to meet Port-D(headset-Mic) THD+N <= -65 dB***



## HeadPhone/LINE OUT


RA16 1 2 2.2K_0402_5% +MICBIASB
34 HP_OUTL HP_OUTL RA17 1 2 47_0402_5% HP_OUTL_CON HP_OUTL_CON 41
34 PORTB_L PORTB_L 1 RA19 2 100_0402_5% CA31 1 2 10U_0603_6.3V6-M
RA22 1 @ 2 2.2K_0402_5% +MICBIASB
34 HP_OUTR HP_OUTR RA23 1 2 47_0402_5% HP_OUTR_CON HP_OUTR_CON 41
34 PORTB_R PORTB_R 1 RA24 2 100_0402_5% CA32 1 2 10U_0603_6.3V6-M

***CA31, CA32 change to 4.7U for Quality requirement***

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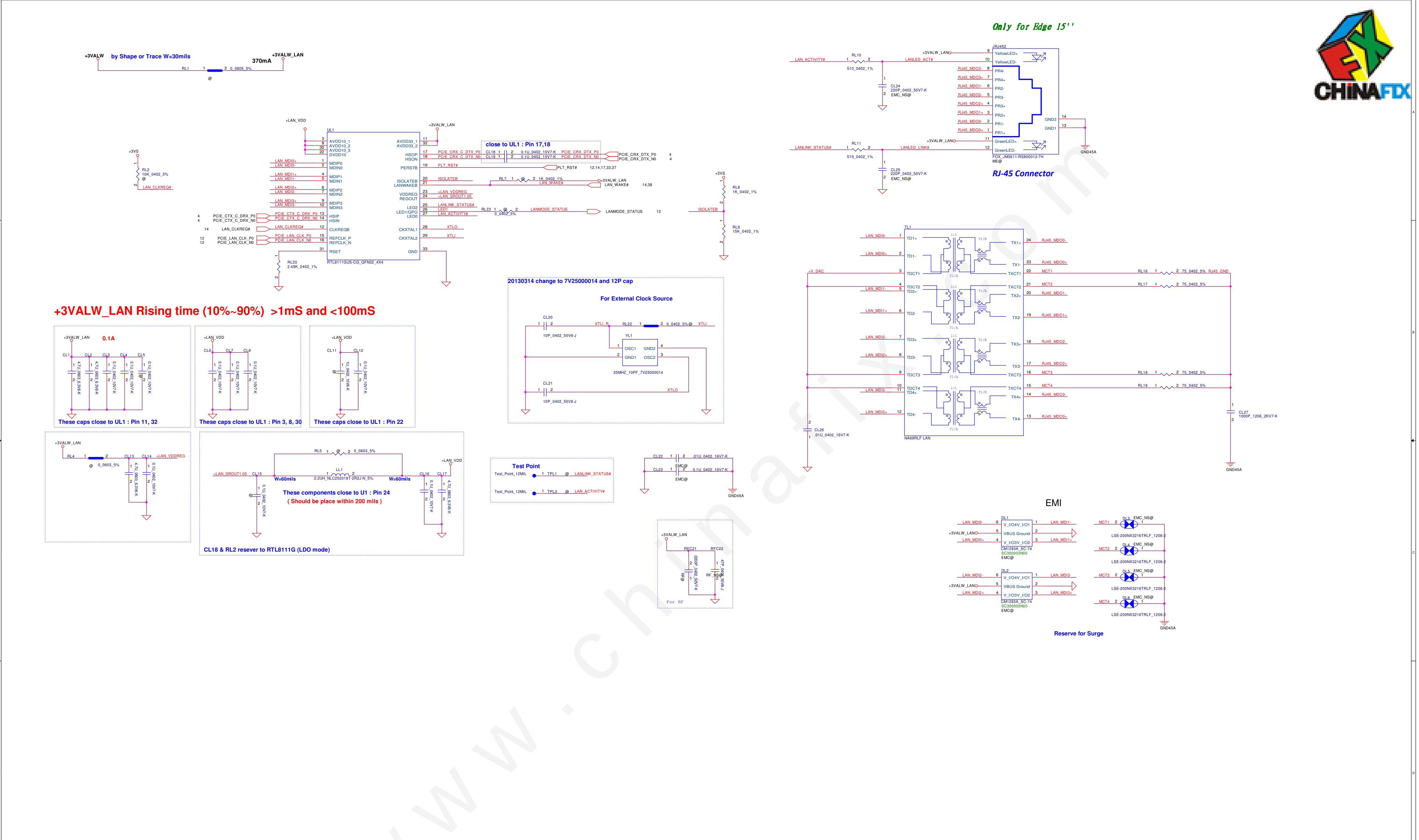

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Title
**LAN/RJ45 CONN**

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Date: Friday, June 13, 2014
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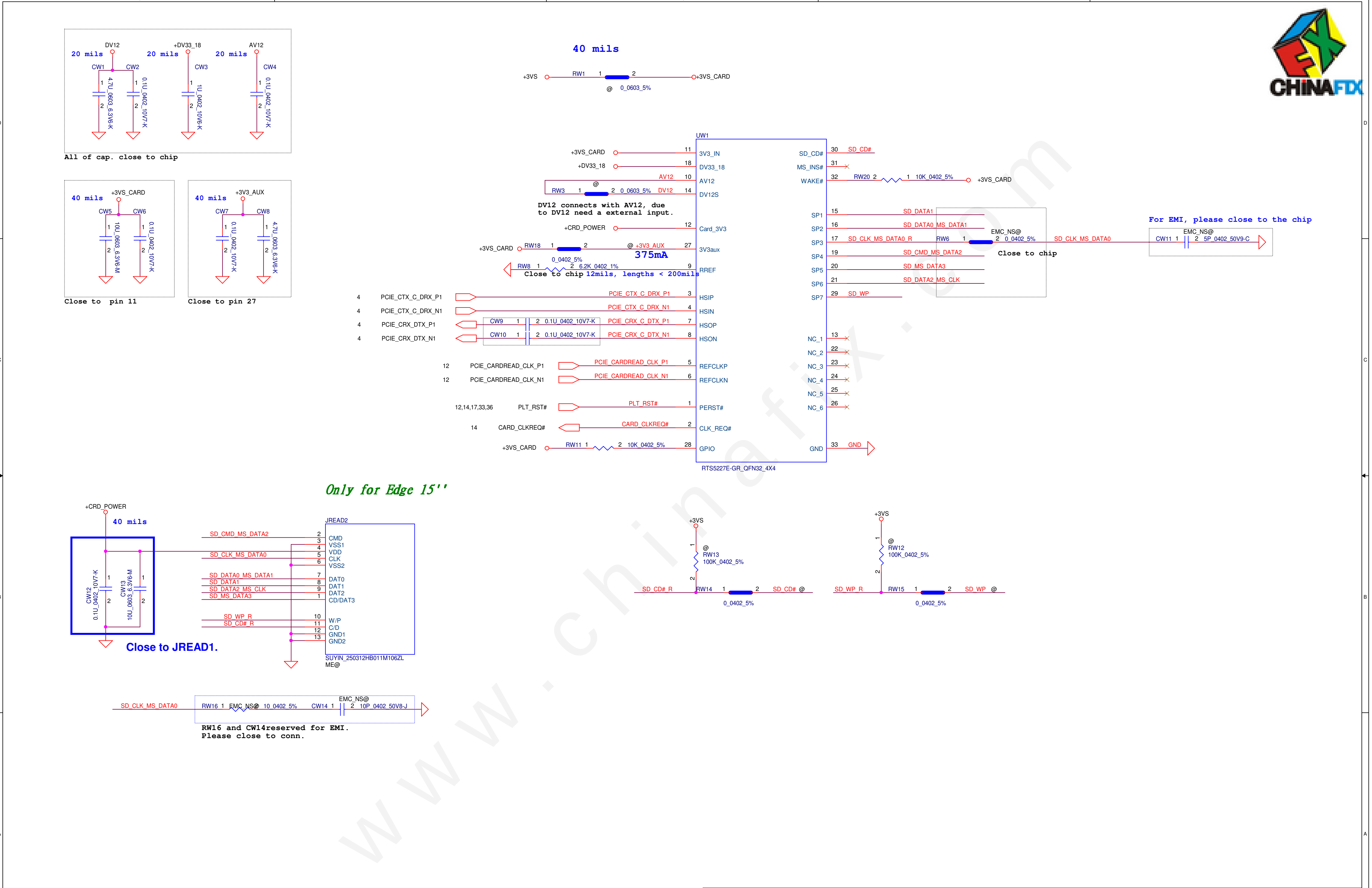

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| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

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Title
Card Reader

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Date: Friday, June 13, 2014
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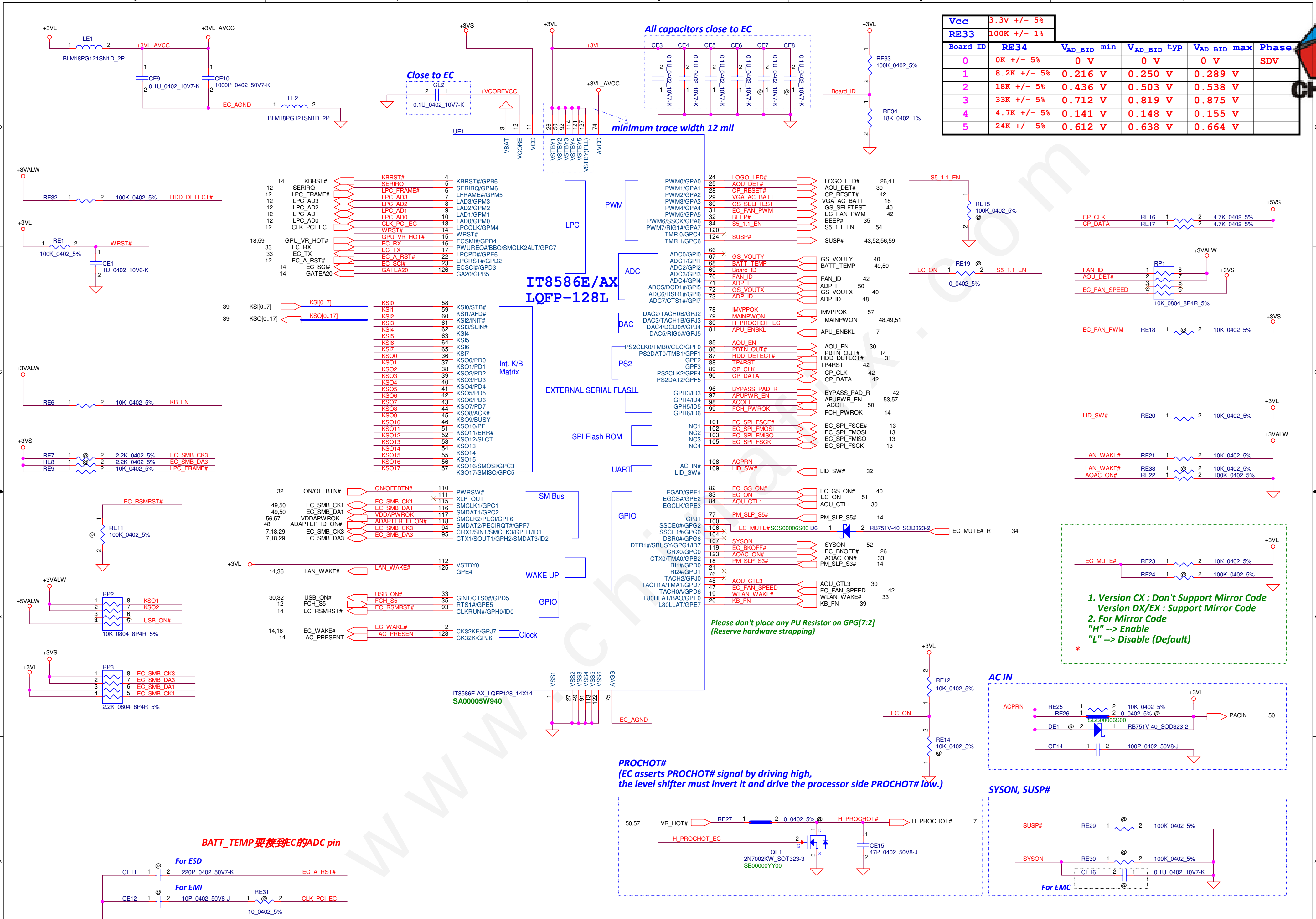

| Vcc | 3.3V +/- 5% |
|---|---|
| RE33 | 100K +/- 1% |

| Board ID | RE34 | $V_{AD\_BID}$ min | $V_{AD\_BID}$ typ | $V_{AD\_BID}$ max | Phase |
|---|---|---|---|---|---|
| 0 | 0K +/- 5% | 0 V | 0 V | 0 V | SDV |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | |
| 4 | 4.7K +/- 5% | 0.141 V | 0.148 V | 0.155 V | |
| 5 | 24K +/- 5% | 0.612 V | 0.638 V | 0.664 V | |

Please don't place any PU Resistor on GPG[7:2]
(Reserve hardware strapping)

1. Version CX : Don't Support Mirror Code
Version DX/EX : Support Mirror Code
2. For Mirror Code
"H" --> Enable
"L" --> Disable (Default)
*

PROCHOT#
(EC asserts PROCHOT# signal by driving high,
the level shifter must invert it and drive the processor side PROCHOT# low.)

BATT_TEMP要接到EC的ADC pin

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EC_IT8586E/FX
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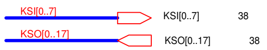
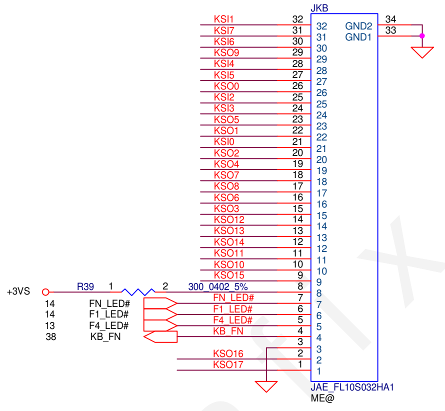
# KeyBoard CONN.(14")





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| Issued Date | 2012/12/05 | Deciphered Date | 2014/12/05 |

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**Title**
**KB**

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|---|---|---|
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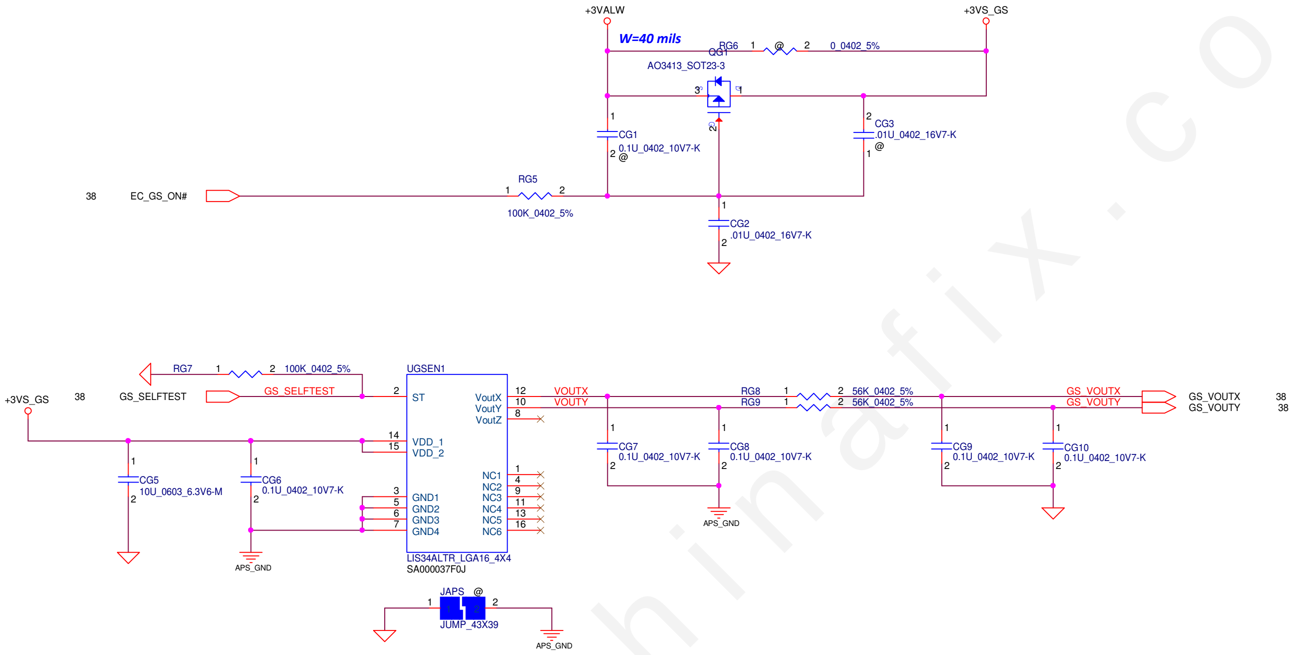
# APS G-Sensor



| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2012/12/05 | Deciphered Date | 2014/12/05 |

Title
**APS G-SENSOR**

Size: Custom
Document Number: NM-A241
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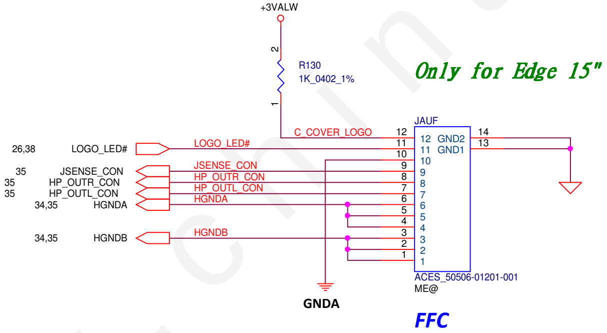

| | | | |
|---|---|---|---|
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**Title**

***Sub-board/Power Button***

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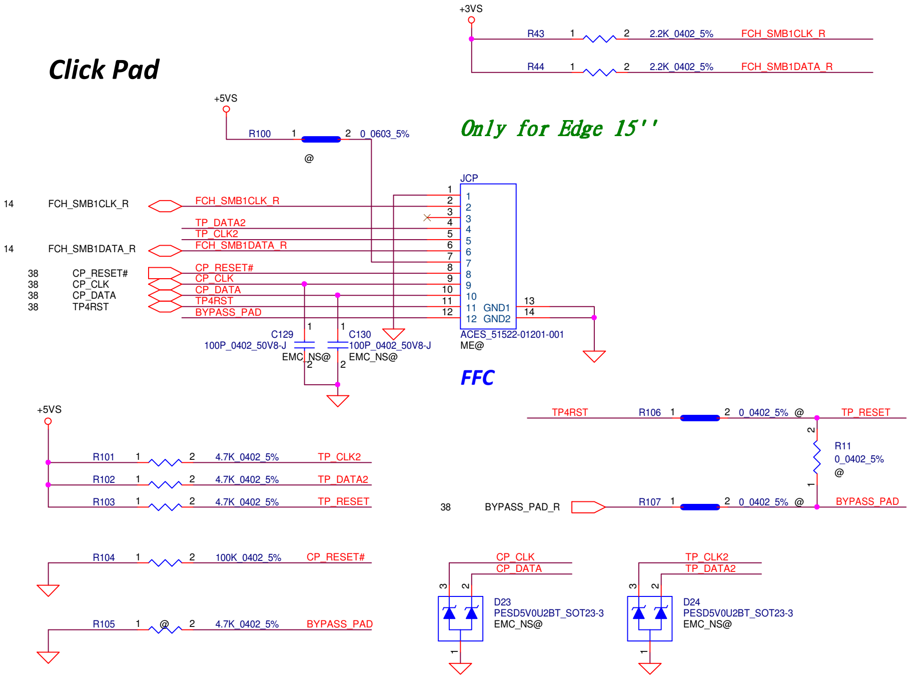
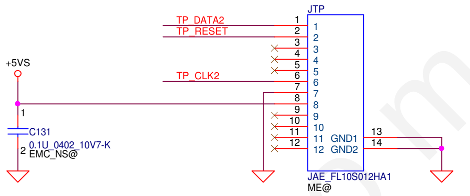
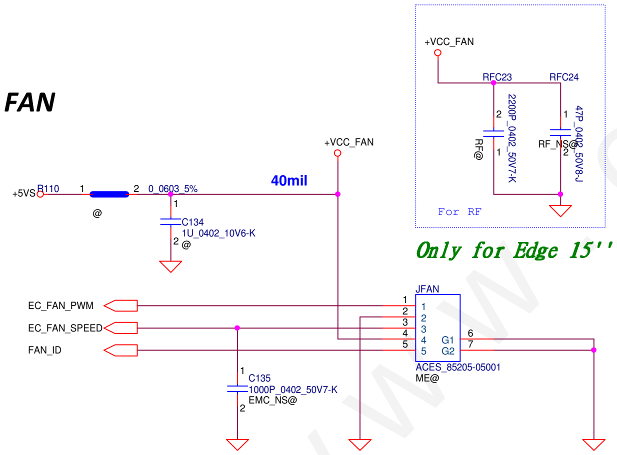
## Click Pad


+3VS
R43 1 2 2.2K_0402_5% FCH_SMB1CLK_R
R44 1 2 2.2K_0402_5% FCH_SMB1DATA_R
+5VS
R100 1 2 0_0603_5%
@
Only for Edge 15''
JCP
14 FCH_SMB1CLK_R
14 FCH_SMB1DATA_R
38 CP_RESET#
38 CP_CLK
38 CP_DATA
38 TP4RST
FCH_SMB1CLK_R
TP_DATA2
TP_CLK2
FCH_SMB1DATA_R
CP_RESET#
CP_CLK
CP_DATA
TP4RST
BYPASS_PAD
1
2
3
4
5
6
7
8
9
10
11 GND1
12 GND2
13
14
C129 100P_0402_50V8-J EMC_NS@
C130 100P_0402_50V8-J EMC_NS@
ACES_51522-01201-001
ME@
FFC
+5VS
R101 1 2 4.7K_0402_5% TP_CLK2
R102 1 2 4.7K_0402_5% TP_DATA2
R103 1 2 4.7K_0402_5% TP_RESET
R104 1 2 100K_0402_5% CP_RESET#
R105 1 @ 2 4.7K_0402_5% BYPASS_PAD
TP4RST R106 1 2 0_0402_5% @ TP_RESET
R11 0_0402_5% @
38 BYPASS_PAD_R R107 1 2 0_0402_5% @ BYPASS_PAD
CP_CLK
CP_DATA
D23 PESD5V0U2BT_SOT23-3 EMC_NS@
TP_CLK2
TP_DATA2
D24 PESD5V0U2BT_SOT23-3 EMC_NS@

## Track point



## FAN



## FingerPrint

Only for Edge 15''

FFC

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Title
CP/TP/FAN/FP CONN

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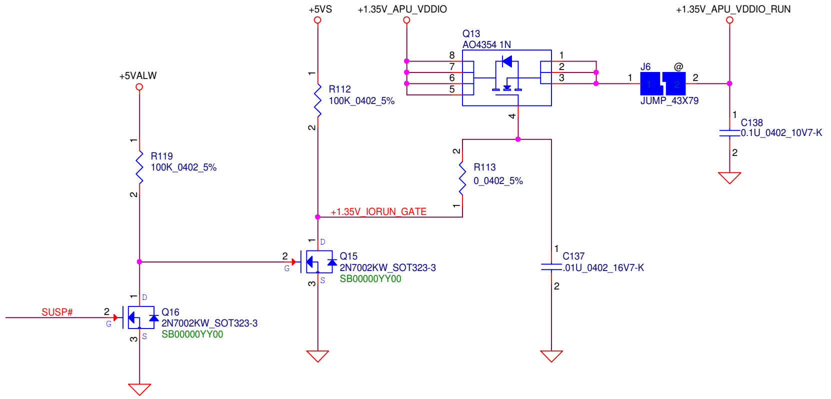
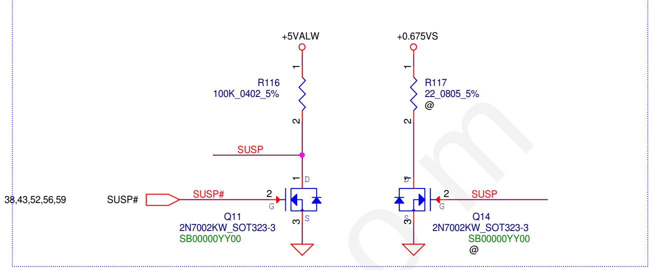
## +VDDIO to +VDDIO_RUN

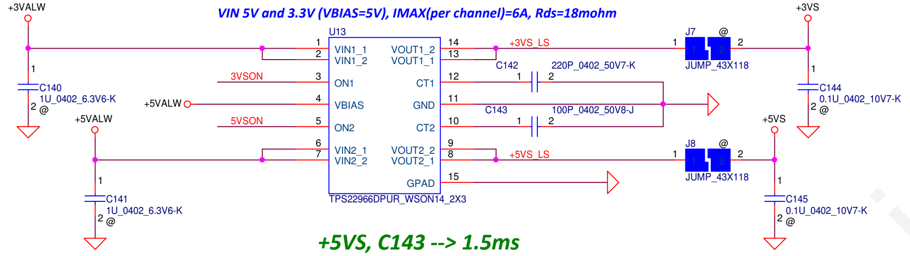


## For DisCharge



## +5VALW To +5VS
## +3VALW To +3VS

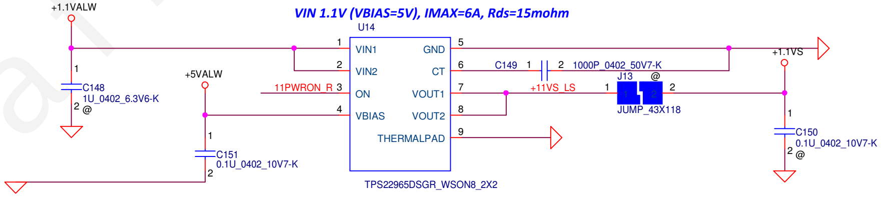
*VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=18mohm*

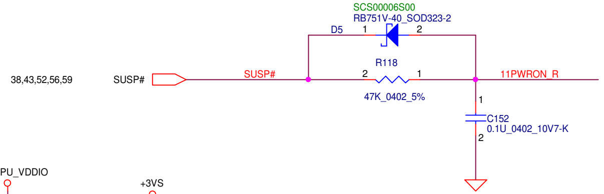


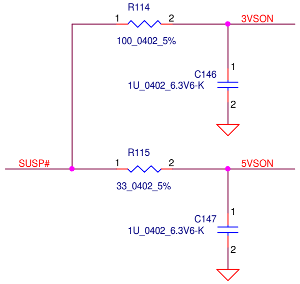
**+5VS, C143 --> 1.5ms**
**+3VS, C142 --> 2.5ms**

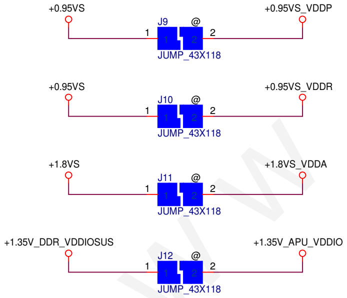
## +1.1VALW to +1.1VS

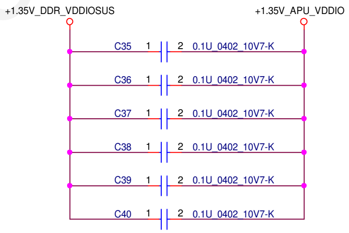
*VIN 1.1V (VBIAS=5V), IMAX=6A, Rds=15mohm*

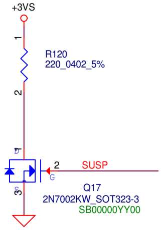












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Title
3VS/5VS/1.1VS/VDDIO_RUN

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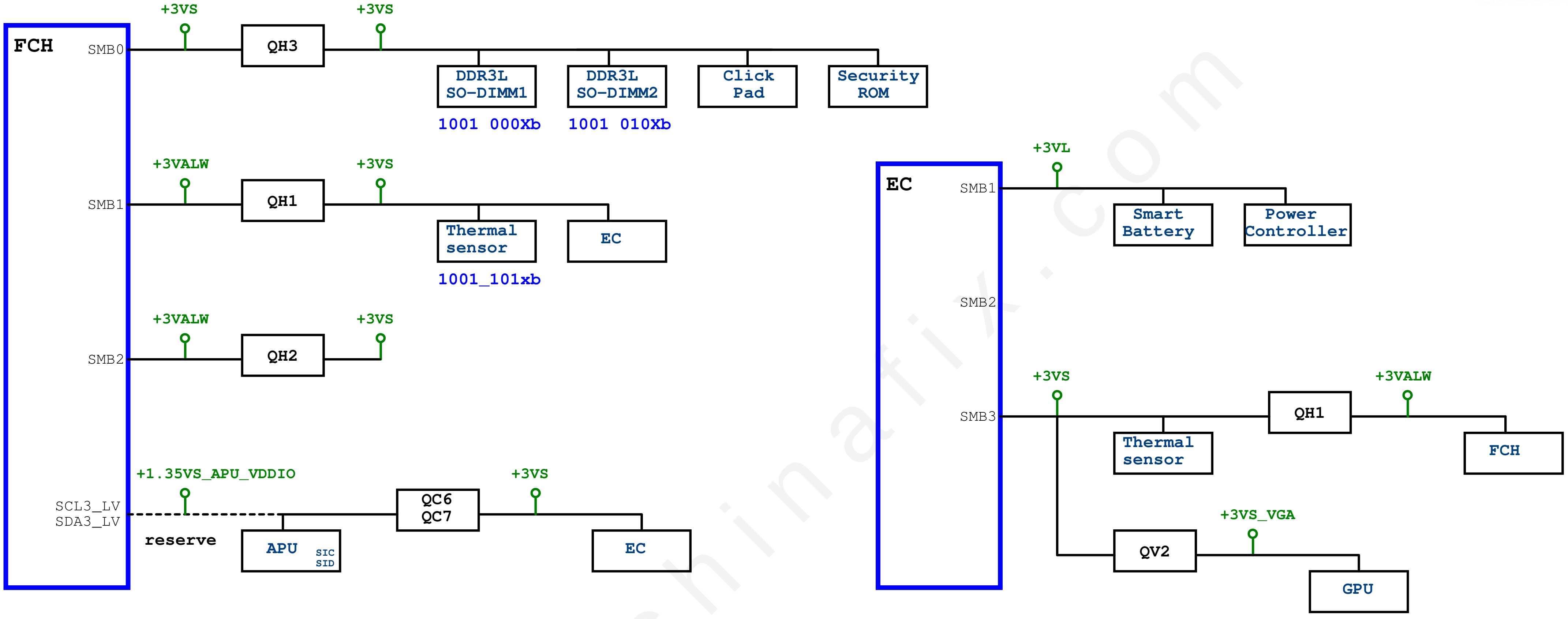
## *SMBus block diagram*



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Title
*SMBUS Block Diagram*

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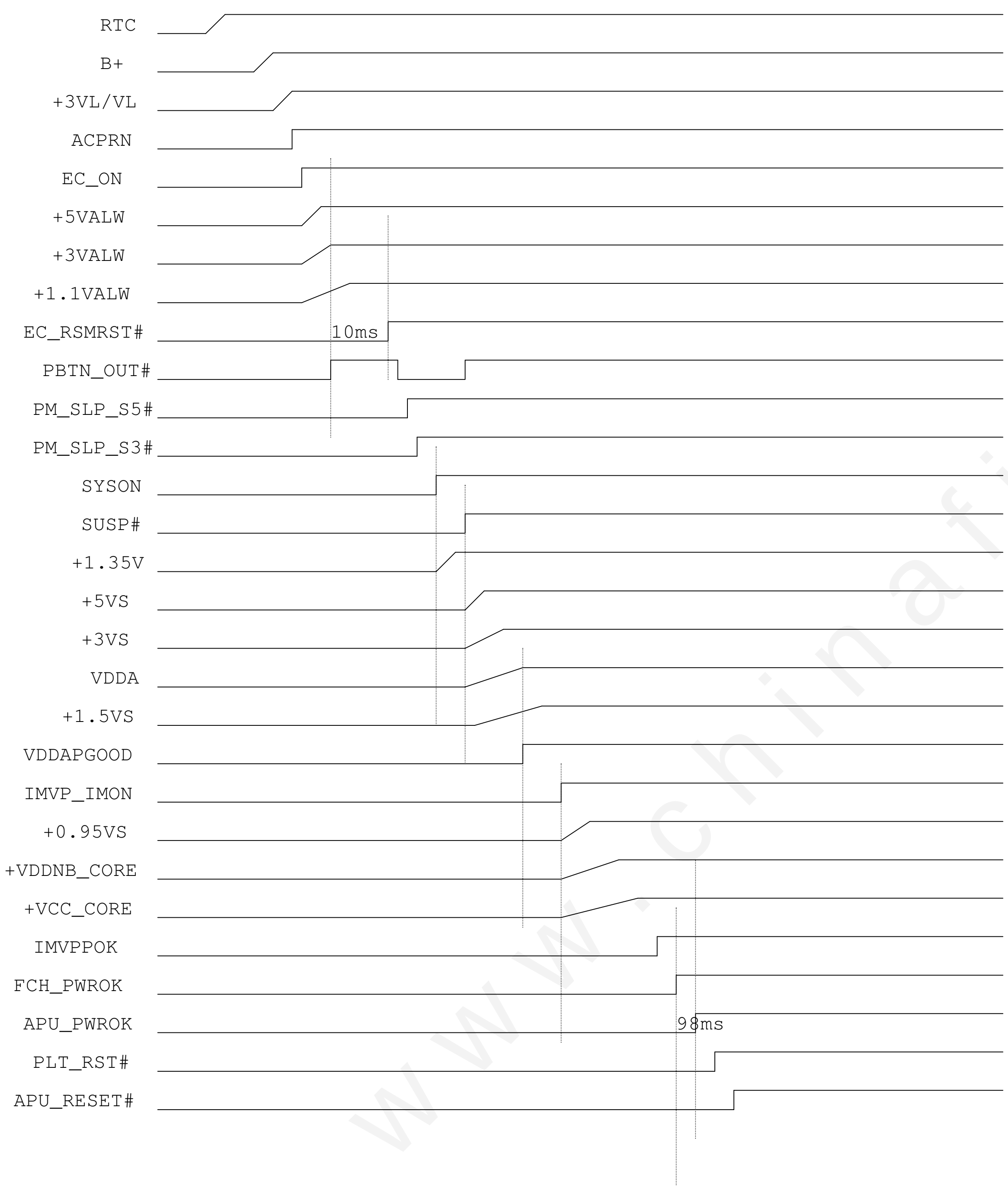

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| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

Title
**Power Sequence**

LCFC

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|---|---|---|
| Custom | NM-A241 | 0.2 |

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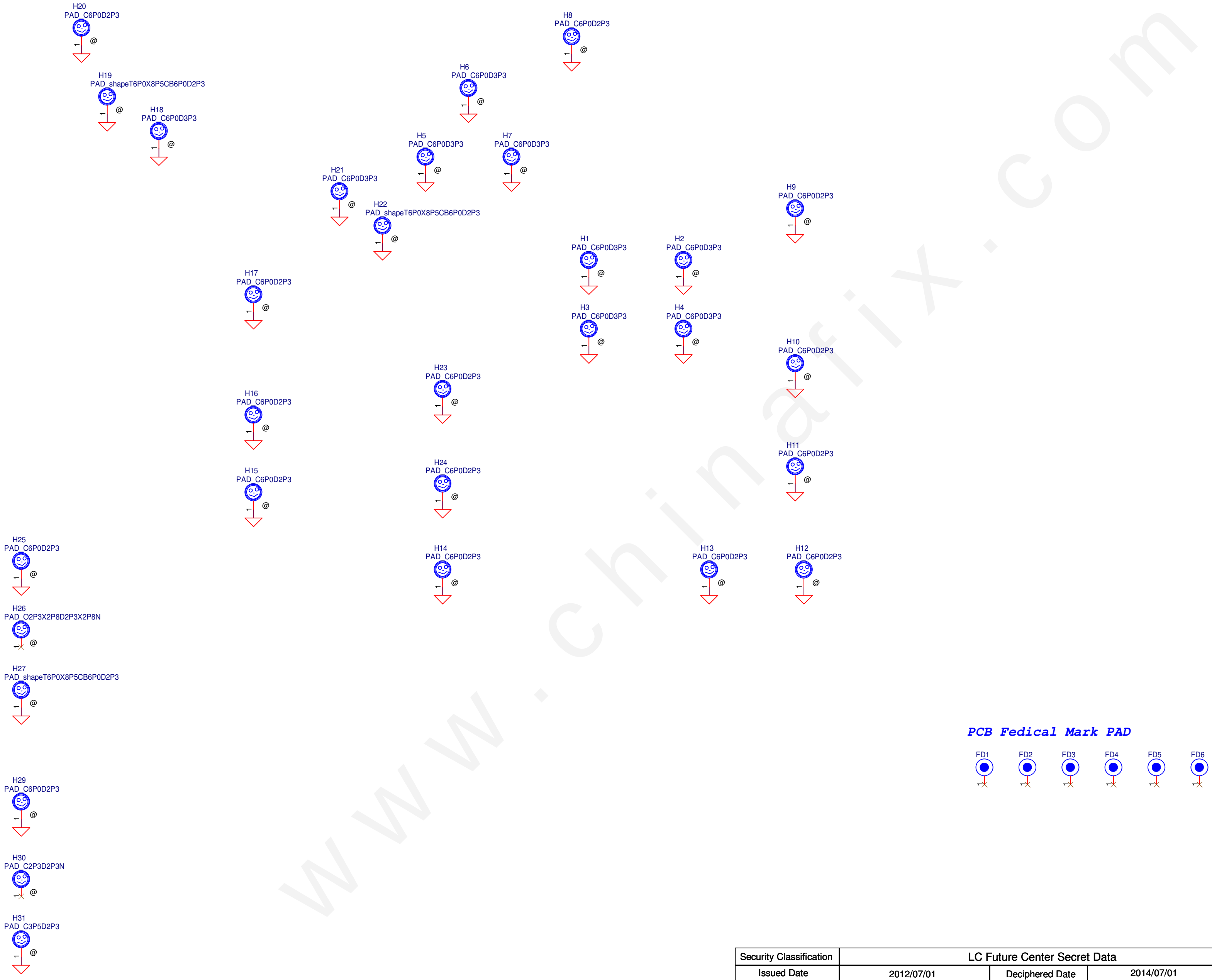
## Only for Edge 15" SCREW LOCATION



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Title
**SCREW**

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|---|---|---|
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POWER MAP

|  |  |  |  |
|---|---|---|---|
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| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

Title

**Power MAP**

|  |  |  |
|---|---|---|
| Size<br>Custom | Document Number<br>NM-A241 | Rev<br>0.2 |

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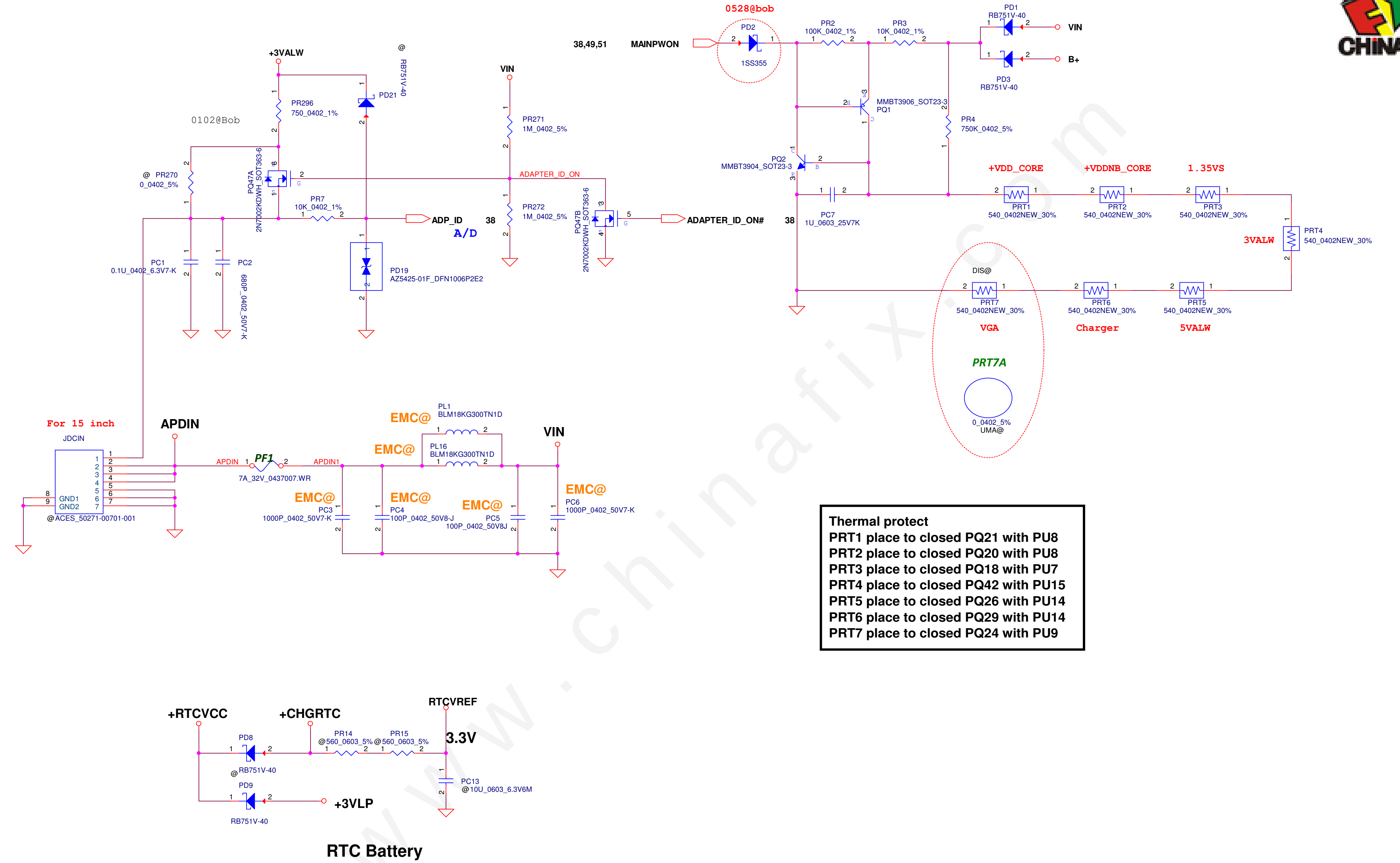

**Thermal protect**

**PRT1 place to closed PQ21 with PU8**

**PRT2 place to closed PQ20 with PU8**

**PRT3 place to closed PQ18 with PU7**

**PRT4 place to closed PQ42 with PU15**

**PRT5 place to closed PQ26 with PU14**

**PRT6 place to closed PQ29 with PU14**

**PRT7 place to closed PQ24 with PU9**

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|---|---|---|---|
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Title
**DCIN / Vin Detector**

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A241 | 0.2 |

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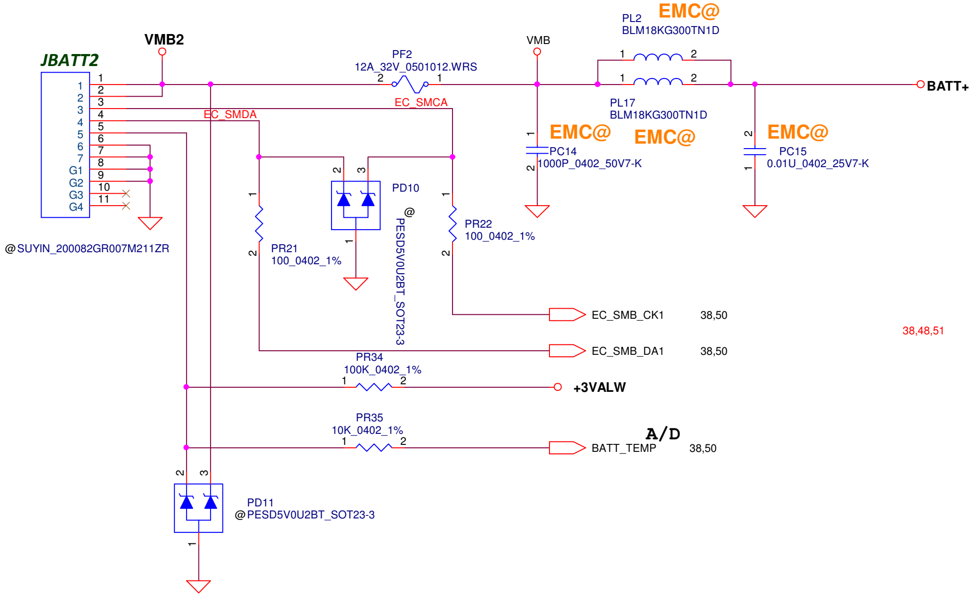
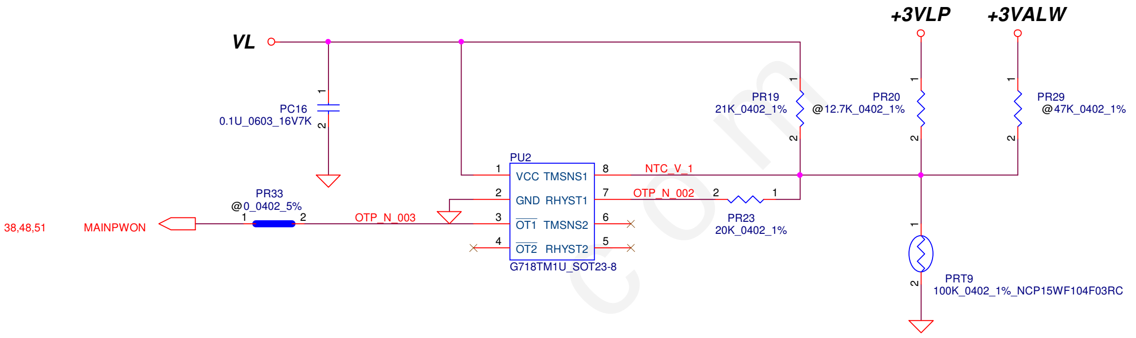
*PRT9 under CPU botten side :*
*CPU thermal protection at 104 +-3 degree C*
*Recovery at 78 +-3 degree C*





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|---|---|---|---|
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Title
**BATTERY CONN/OTP**

Size Custom
Document Number
**NM-A241**
Rev 0.2

Date: Friday, June 13, 2014
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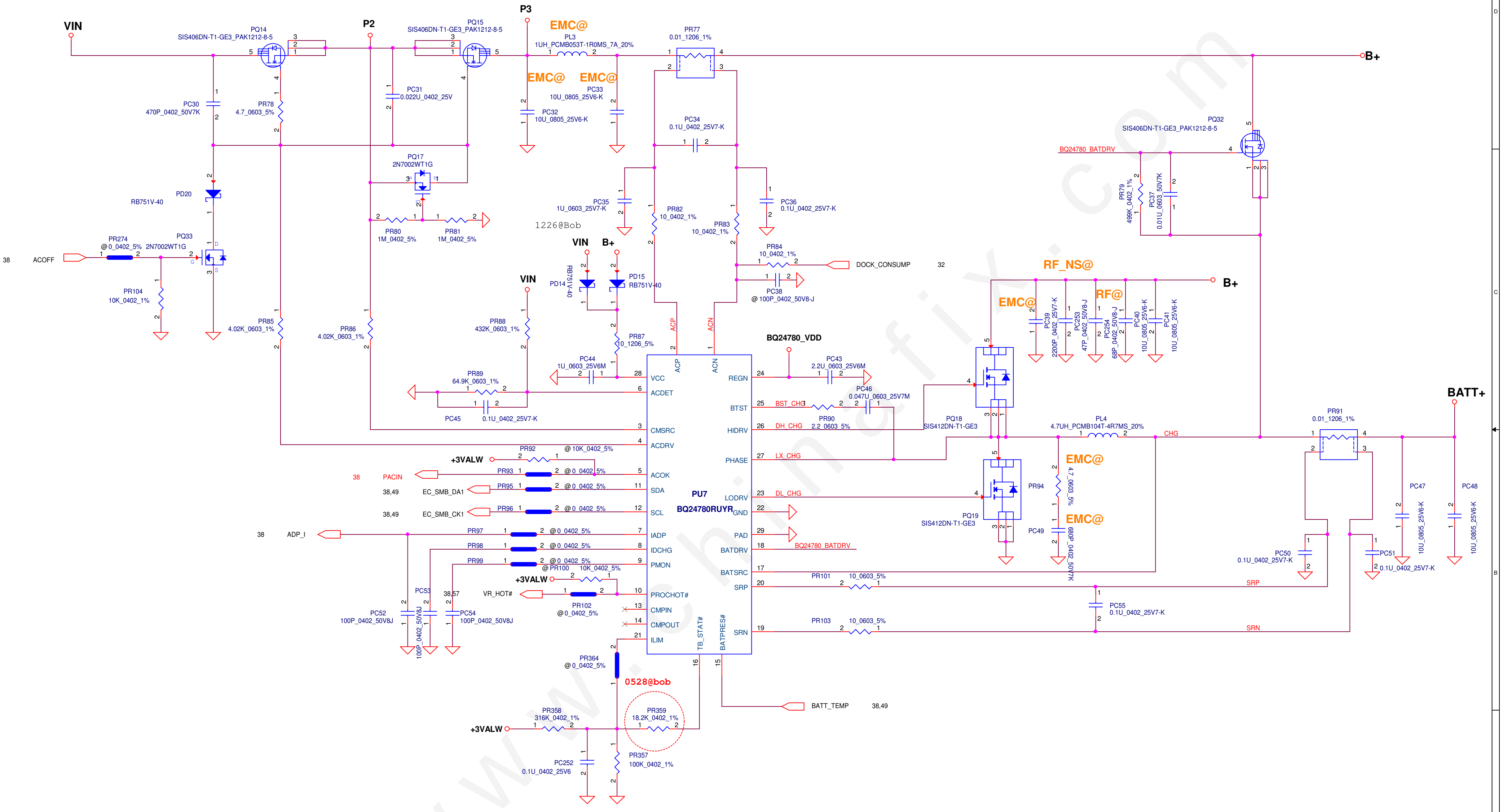

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Title
CHARGER

Size C
Document Number
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Date: Friday, June 13, 2014
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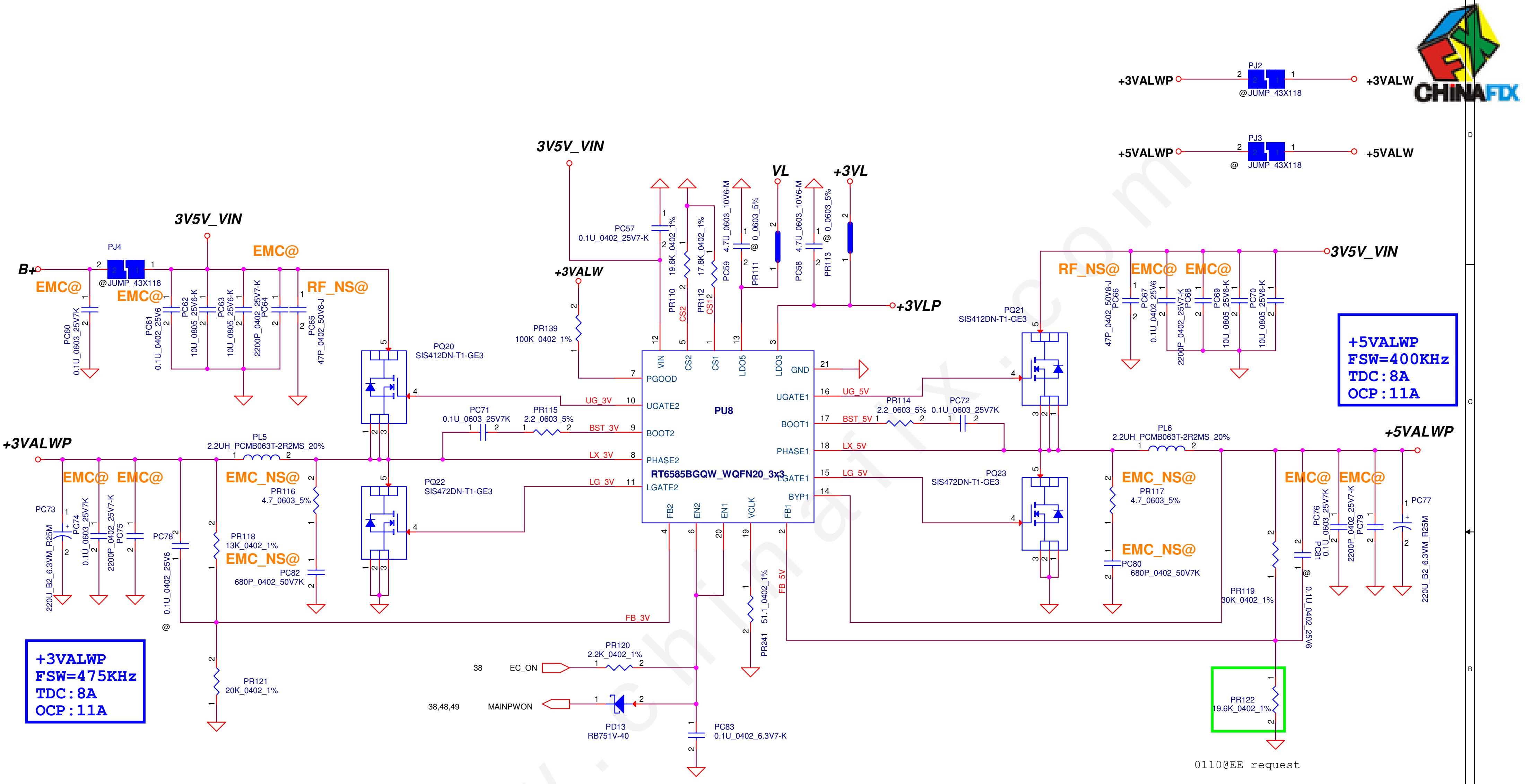

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Title
3VALWP/5VALWP

Size Custom
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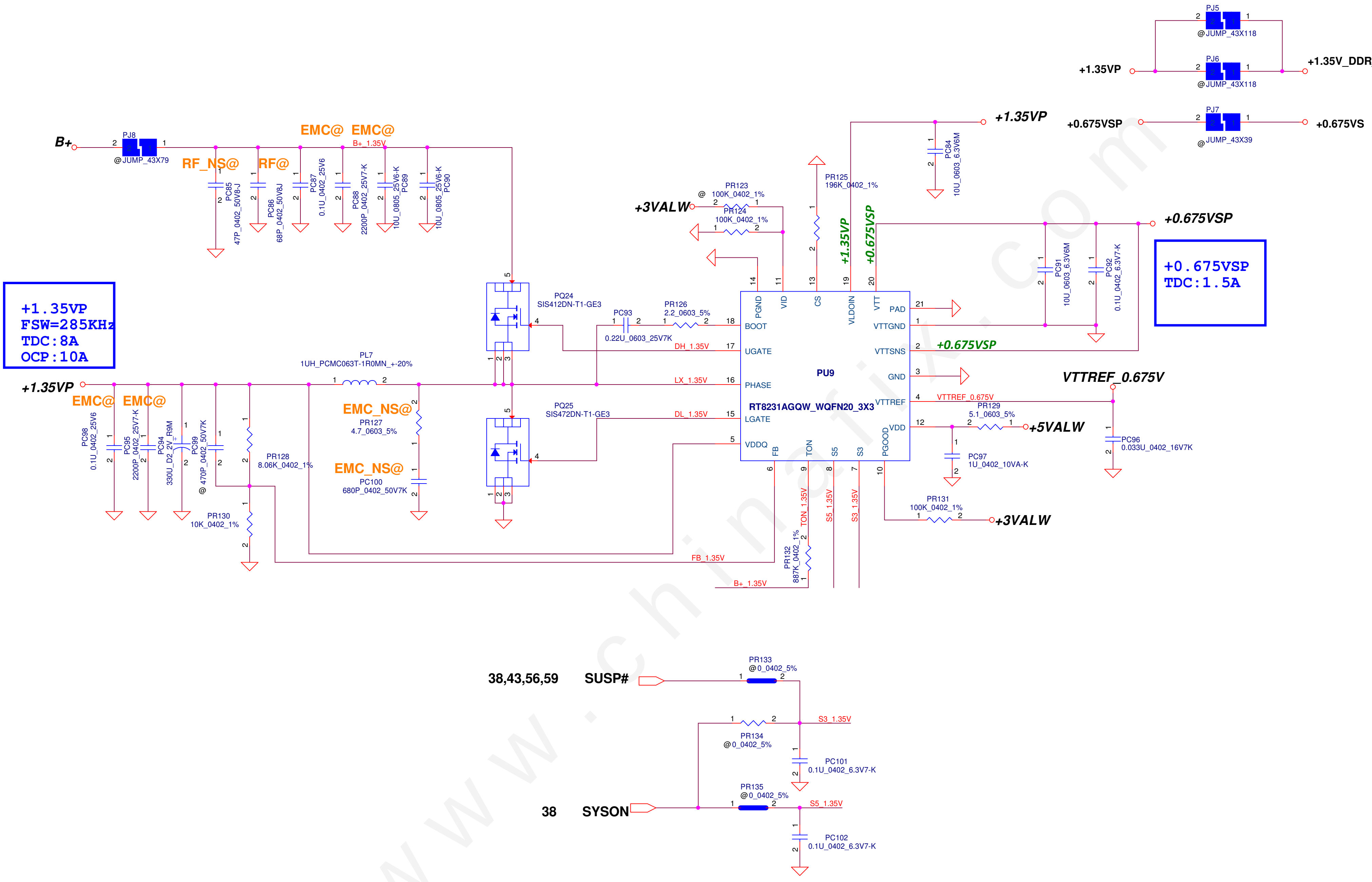

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Title
+1.35VP/+0.675VSP

LCFC

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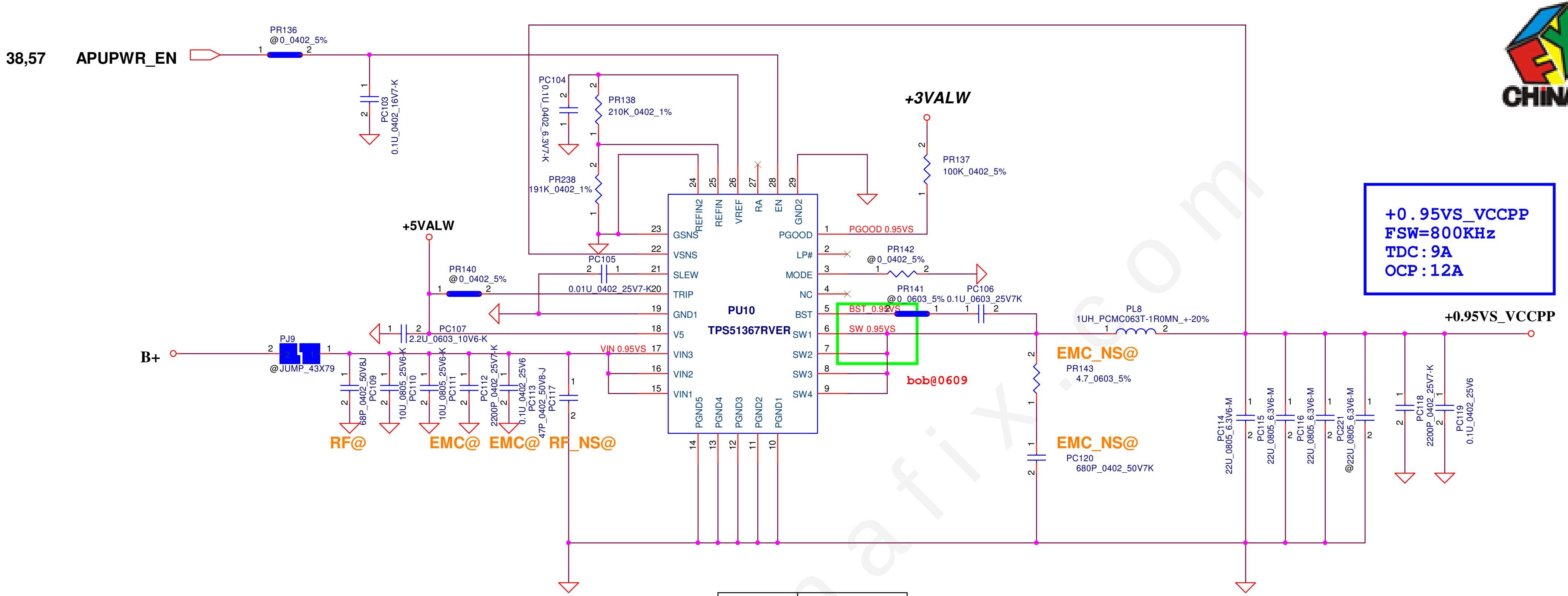
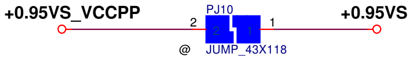


**+0.95VS_VCCPP**
**FSW=800KHz**
**TDC:9A**
**OCP:12A**

| Mode | Frequency |
|---|---|
| GND | 400KHz |
| Float | 800KHz |



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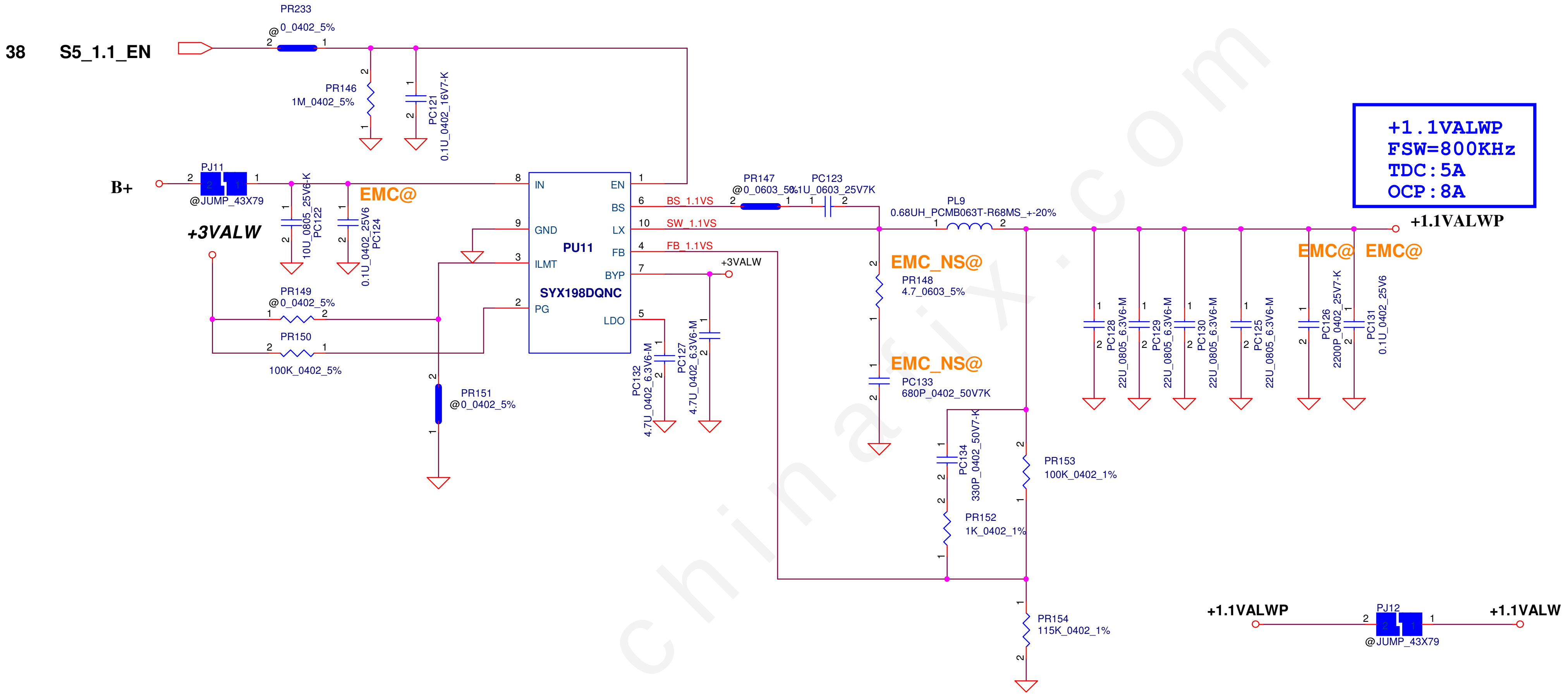
|---|---|---|---|
| Issued Date | 2013/08/01 | Deciphered Date | 2014/08/01 |

Title
*+0.95VS_VCCPP*

Size Custom
Document Number *NM-A241*
Rev 0.2

Date: Friday, June 13, 2014



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Title
+1.1VALWP

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|---|---|---|
| B | NM-A241 | 0.2 |

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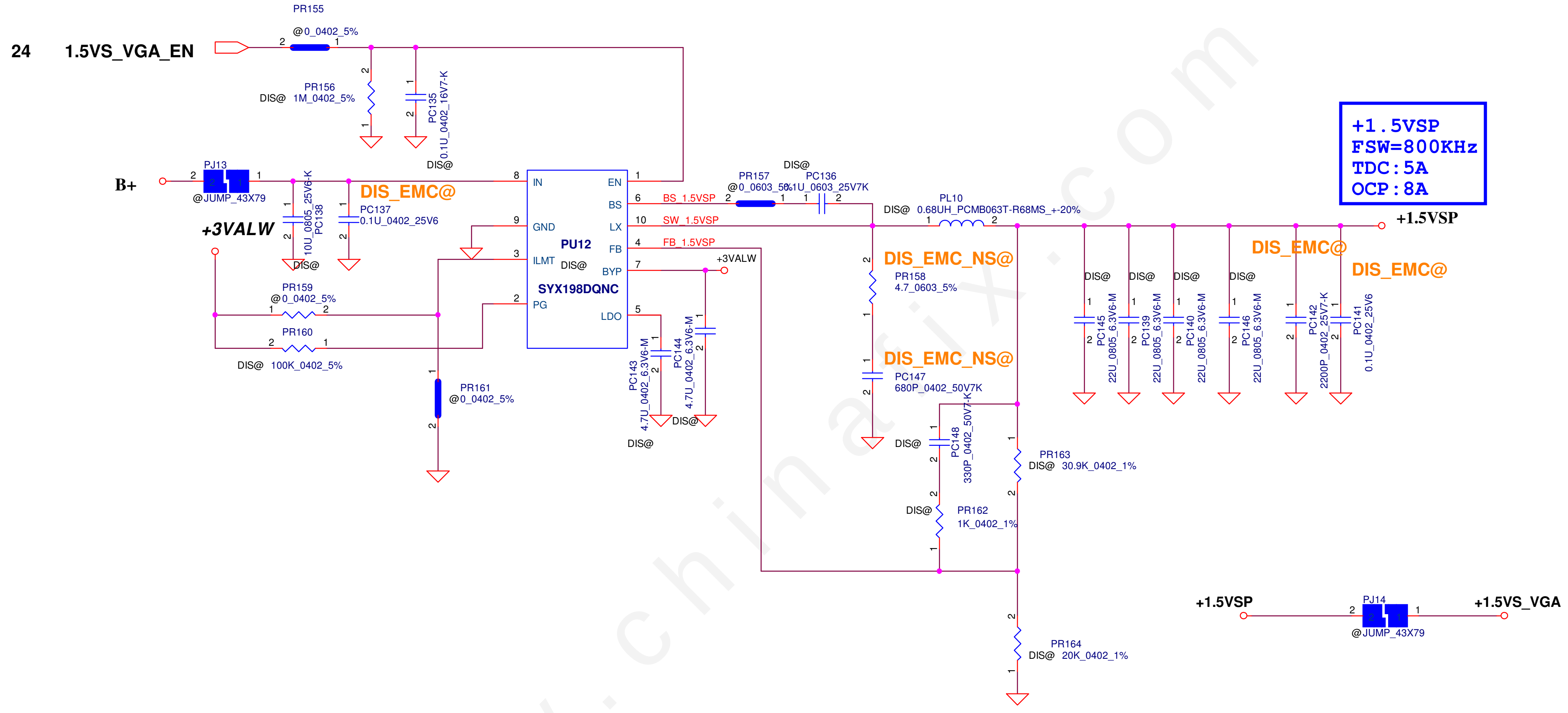

+1.5VSP
FSW=800KHz
TDC:5A
OCP:8A

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| Issued Date | 2013/08/01 | Deciphered Date | 2014/08/01 |

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Title
+1.5VSP

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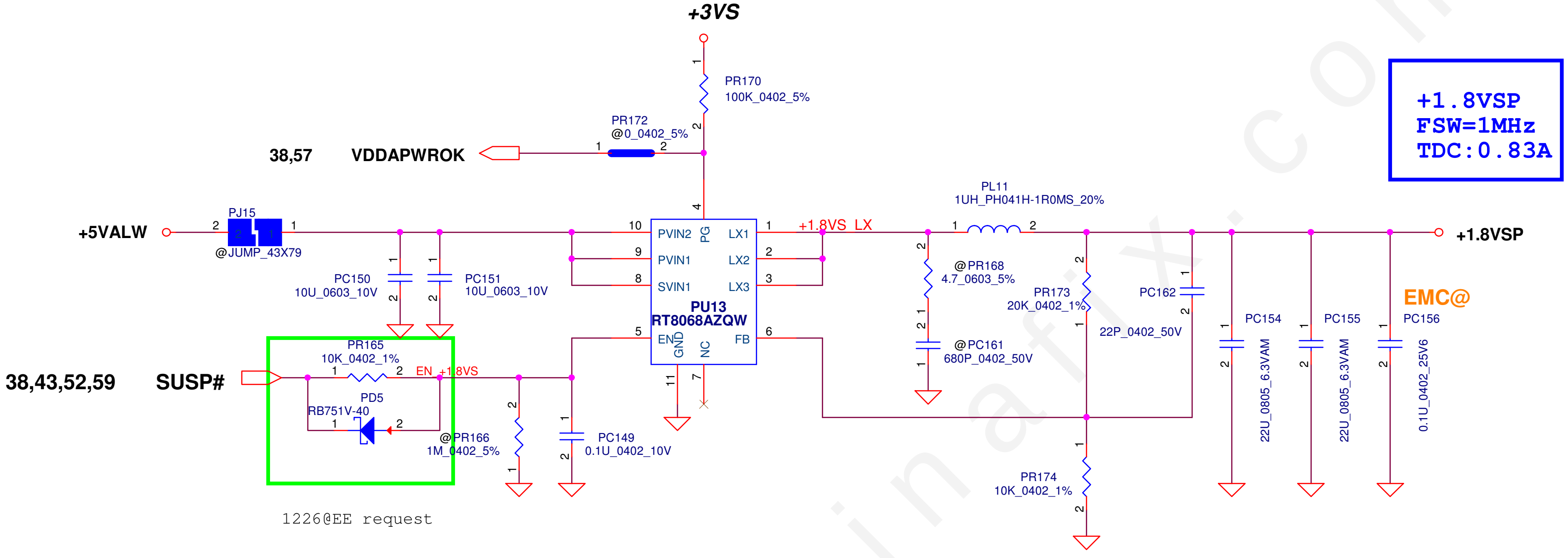
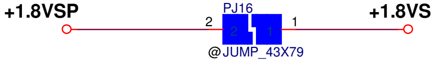


1226@EE request

+1.8VSP
FSW=1MHz
TDC:0.83A



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Title
+1.8VSP

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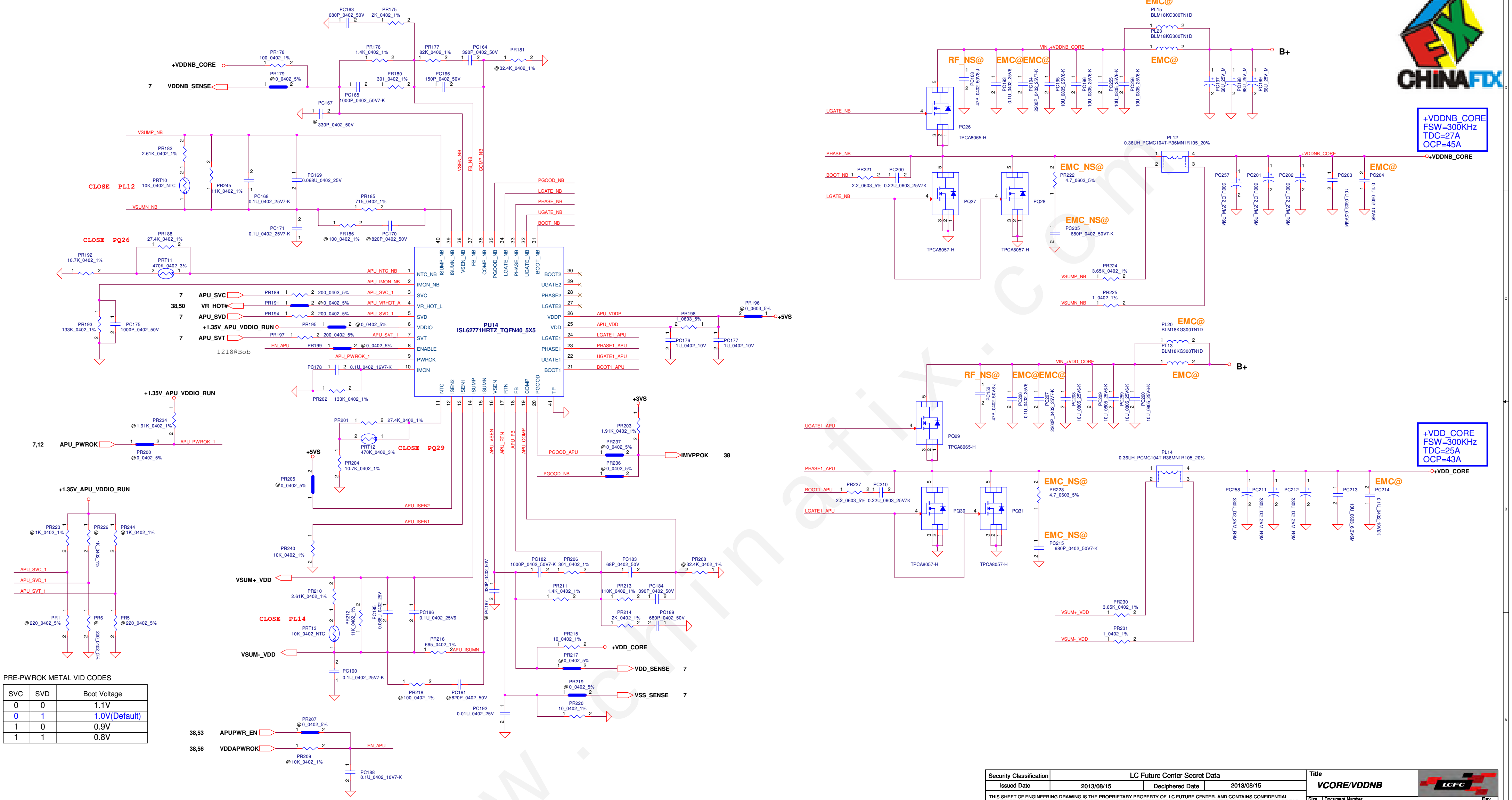

+VDDNB_CORE
FSW=300KHz
TDC=27A
OCP=45A

+VDD_CORE
FSW=300KHz
TDC=25A
OCP=43A

PRE-PWROK METAL VID CODES

| SVC | SVD | Boot Voltage |
|---|---|---|
| 0 | 0 | 1.1V |
| 0 | 1 | 1.0V(Default) |
| 1 | 0 | 0.9V |
| 1 | 1 | 0.8V |

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Title
**VCORE/VDDNB**

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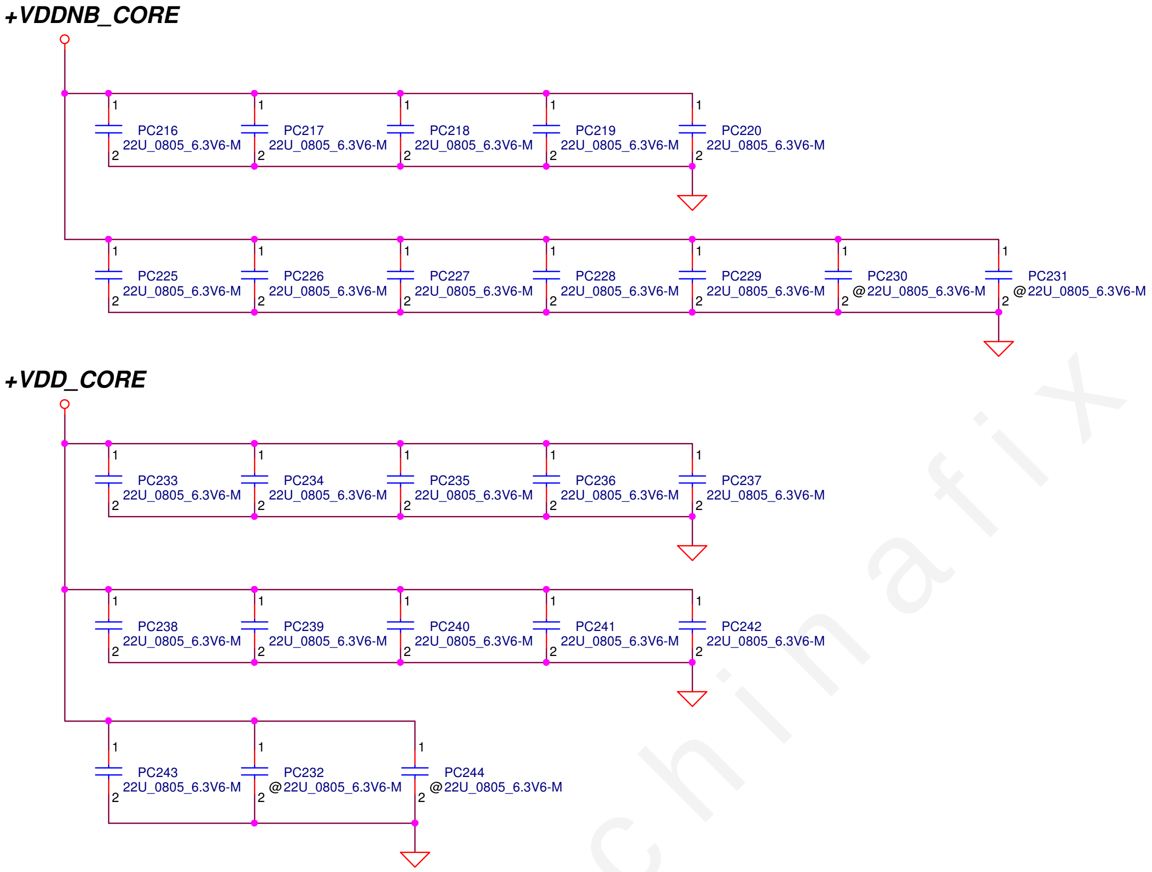

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Title
**VCCCPUCORE DECOUPLING**

LCFC

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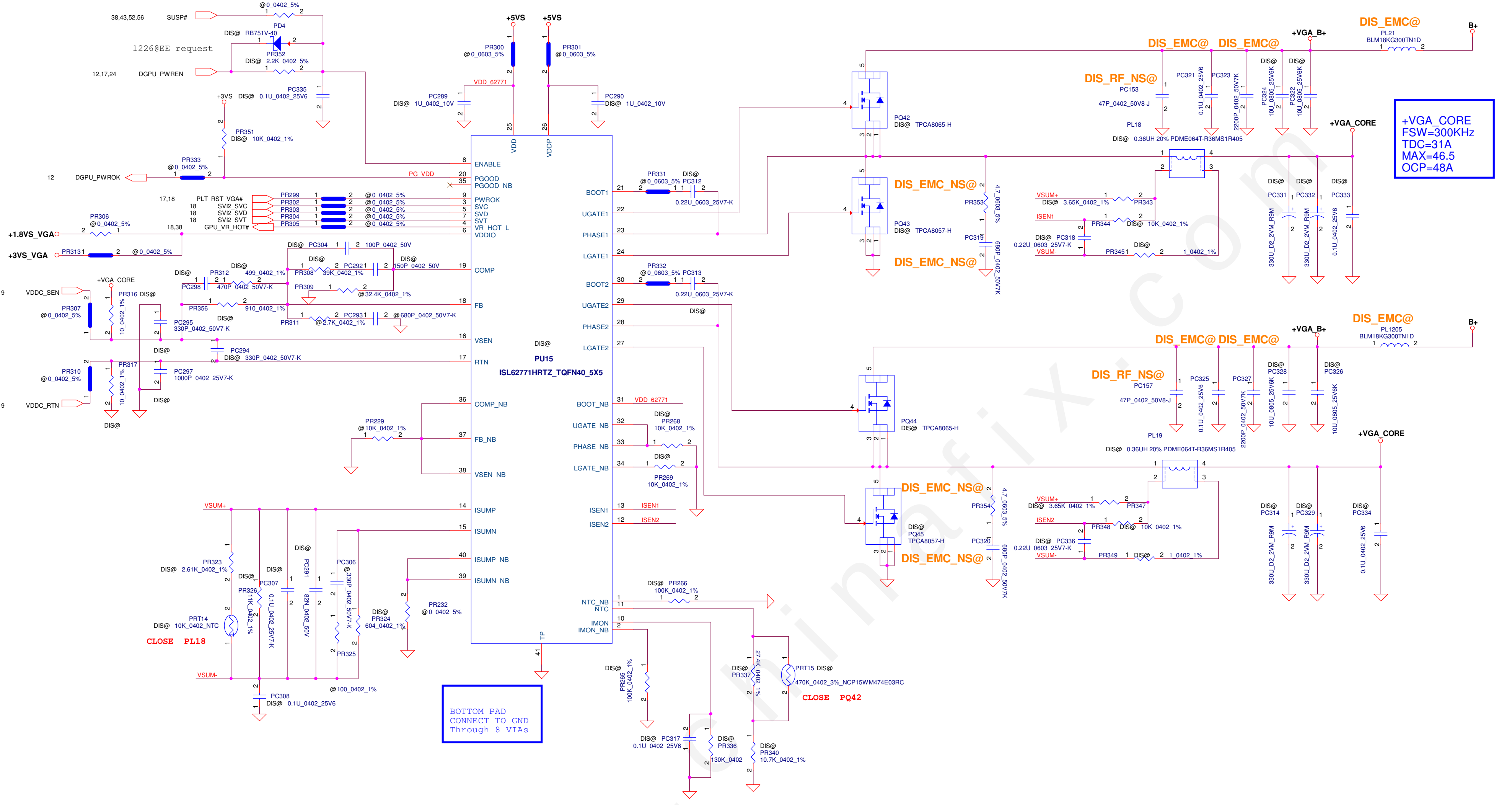
# ISL62771 Schematic for FT3 solution



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+VGA_CORE

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| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 1 | GPU power sequence tuning | 24<br>12 | 1.RV132 from 20K ohm change to 3.3K ohm<br>2.CV165 from 1000PF change to 820PF<br>3.RV129 from 51K ohm change to 180K ohm<br>4.RV133 from 47K ohm change to 240K ohm<br>5.Add DV5<br>6.RH145 pull down to 1K ohm<br>7.change RH35 to @<br>8.reserver GPU core discharge circuit(RV144, RV143,QV13) | 2013.12.26 | FVT |
| 2 | APU_RESET signal noise | 7 | 1.reserve CC169 | 2013.12.26 | FVT |
| 3 | EMI request | 36 | 1.CL27 change to 2000V | 2013.12.26 | FVT |
| 4 | Common design | 14 | 1.add RH92 to separate | 2013.12.26 | FVT |
| 5 | System power sequence | 43 | 1.add +3VS discharge circuit Q17,R120<br>2.change D5 to mount form @ | 2013.12.26 | FVT |
| 6 | Common design | 43 | 1.RA2 change to @ , Add RA3 connect to 3VL | 2013.12.26 | FVT |
| 7 | ECSL request | 40<br>24 | 1.SB000007H1J change to AOS AO3413 SB93413000J(QG1, QV5)<br>2.SB000002R0J change to LRC LMBT3904WT1G SB00000ZJ00 (Q1,Q8,Q9,QC1,QC2,QV3,,QC4,QC5)<br>3.SE000000KMT change to SE00000X30T(C1,C3,C70,C140,C141,C146,C147,C148, CA9,CA13,CA14,CA15,CA17,CD22,CV163) | 2013.12.26 | FVT |
| 8 | del double component | 38 | 1.Del RE2, RE3 | 2013.12.26 | FVT |
| 9 | modify SMBus issue | 7 | 1.QC7, QC6 gate G connect to 1.35V run del RC71,RC72 | 2013.12.26 | FVT |
| 10 | SMBus issue | 7 | 1.add RC21 | 2013.12.30 | FVT |
| 11 | Cost down component count | 38 | 1.RE30, RE29, RE11 change to @ | 2013.12.30 | FVT |
| 12 | Cost down component count | 14 | 1.RH87 change to @ | 2013.12.30 | FVT |
| 13 | Cost down | 15 | 1.RH62 change to mount, LH2 change to @ | 2013.12.30 | FVT |
| 14 | Cost down component count | 18 | 1.RV75 change to @ | 2013.12.30 | FVT |
| 15 | Cost down component count | 18 | 1.RV82, RV83 change to @ | 2013.12.30 | FVT |
| 16 | Cost down component count | 18 | 1.RV150, RV151 change to JET@ from @<br>2.RV125, RV122 change to @ form DIS@<br>3.CV149,CV150,RV96, RV97,RV95,CV152,CV151,UV9 change to @ form JET@ | 2013.12.30 | FVT |
| 17 | Cost down component count | 26<br>7 | 1.R4, RC73, RC74 change to@ | 2013.12.30 | FVT |
| 18 | Cost down component count | 7 | 1.RC17,18,13, 19 del add RP4 | 2013.12.30 | FVT |
| 19 | Cost down component count | 7 | 1.RC47,48,49 del add RP5 | 2013.12.30 | FVT |
| 20 | Cost down component count | 7 | 1.RC37,38,39,40 del add RP6 | 2013.12.30 | FVT |
| 21 | EC_MUTE# leakage issue | 38 | 1.add D6 | 2013.1.3 | FVT |

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| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 22 | for EC mirro function | 38 | add D6,RA29 and RE12 change to mount | 2013.01.06 | FVT |
| 23 | BIOS request | 14 | change GPIO ipin to G-event 5 | 2013.01.06 | FVT |
| 24 | PEG signal EA request | 7/17 | change PEG capacitor to 0.22u | 2013.01.06 | FVT |
| 25 | reduce component count | 7/17 | DEL RC45,R66, RH70,RH71,RH72,RH73,RH77,RV136,RW4,RW5,RW7,RW8,RW9,RW10 | 2013.01.06 | FVT |
| 26 | Pin define modify | 35 | JSPK | 2013.02.27 | SIV |
| 27 | modify BOM strcture | 7 | CC169 | 2013.02.27 | SIV |
| 28 | modify BOM strcture | 43 | QV13 change to Q13 | 2013.02.27 | SIV |
| 29 | modify BOM strcture | 24 | UV11 change to DIS@ form always mount | 2013.02.27 | SIV |
| 30 | remove FP function | 18 | DEL R111,D25,C136, JFPB | 2014.02.24 | SIV |
| 31 | reduce component count | | del 0402<br>R10 R106 R107 R134 RA28 RC43 RE26<br>RH6 RH7 RH8 RH9 RH10 RH11 RH12<br>RH13 RH14 RH15 RH16 RH17 RH44<br>RH22 RH57 RH58 RH76 RH91 RH98<br>RH90 RH122 RH125 RH126 RH127 RH128<br>RH129 RH130 RL22 RV150 RV151<br>0603<br>R5 R100 R110 RH78 RH79 RH80<br>RH81 RL4<br>0805<br>R8 R37 RA1 RA3 RA4 RA6 RH62 RH61 RH142<br>RH143<br>RL1 | 2014.02.24 | SIV |
| 32 | CP SMB issue | 14/42 | add R43,R44 for SMB pull up | 2014.02.24 | SIV |
| 33 | separate HDT connector<br>APU_RESET# signal | 7 | add R137@ | 2014.02.24 | SIV |
| 34 | remove GPU CTF function | 18 | DEL QV3,CV148,RV87,DV1,RV86,RV88,RV74 | 2014.02.24 | SIV |
| 35 | change BOM Structure | 4 | change CC1~CC8, CC106~CC113 to DIS@ | 2014.05.14 | SVT |
| 36 | Audio test request | 35 | CA 31, CA 32 change to 10u form 4.7u | 2014.05.28 | SVT |
| 37 | Power sequence modify | 43 | C142 change to 220p form 2200p<br>C143 change to 100p form 1000p | 2014.05.28 | SVT |

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