Enrico Caruso 14
Muxless Schematics Document
Ivy Bridge & Sandy Bridge
Intel PCH
2012-01-03
REV : X02

DY :	None Installed
PSL:	10mW internal schematic
UMA:	UMA ONLY installed
OPS:	Optimus solution installed.
Surge:	For GO Rural config stuff.
GIGA:	For GIGA LAN config stuff.
LPC :	Reserve for LPC debug card
POP :	Reserve for solve "POP" sound iuuse

<Variant Name>

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Title: Cover Page

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Block Diagram (Discrete)

##OnMainBoard

Hynix:72.52G63.A0U (HT31P$AA)
Samsung:72.42164.D0U (JP0F2$AA)

VRAM gDDR3 900MHz
1GB (128Mx16x4)
88,89,90,91

gDDR3 900MHz

N13M-GS
Xtal=27MHz
83.84,85,86,87

PCIe x 8
(Discrete only)

Intel CPU
Ivy Bridge & Sandy Bridge
4,5,6,7,8,9,10

DDRIII 1333/1600 Channel A
DDRIII 1333/1600 Channel B

DDRIII Slot 0 1333/1600 15
DDRIII Slot 1 1333/1600 14

FDIx4x2
DMIx4

10/100 /1000 LOM
Realtek RTL8111F (Giga LAN)
Realtek RTL8105E-VD (10M/100M)
Xtal=25MHz
31

PCIE x 1
PCIE x 1

RJ45 CONN 59

802.11a/b/g
Mini-Card WLAN+BT3.0 64

PCIE
100MHz
2.5Gbps

Intel
PCH
Panther Point
BGA989

HM75
12 USB 2.0/1.1 ports
High Definition Audio
6 SATA ports
8 PCIE ports
LPC I/F
ACPI 4.0a
17,18,19,20,21,22,23,24,25

CRT 50
LCD 49
HDMI 51

CRT
LVDS
HDMI

USB 2.0
480Mbps

USB 2.0 x 1
USB 2.0 x 1
USB 2.0 x 1
USB 2.0 x 2

CAMERA 49
M/B USB x1 (Left) 61
I/O board USB x2 (Right) 82

SD/MMC/MS/MS Pro 74
CardReader Realtek RTS5138 32
USB2.0

LPC Bus
33MHz

KBC
NUVOTON
NPCE885P
27

D/A

Thermal NCT7718W 28
Thermal G709 28
Fan Control G991P 28

PS/2
PS/2

Touch PAD 69
Int. KB 69

Audio board
Internal Analog MIC 58
HP1 82
MIC IN
2CH SPEAKER 58

Azalia CODEC
Cirrus CS4213D 29
AZALIA
24MHz

SATA
SATA 3Gbps
SPI

HDD 56
ODD 56
Flash ROM 8MB 60

SYSTEM DC/DC APL5916 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC VT1318+1323 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51219 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51125 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

SYSTEM DC/DC TPS51216R 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC VT1318+1323 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA ADP3211 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24707 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

Switches 93	
INPUTS	OUTPUTS
1D5V_S3	1D5V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0

PCB LAYER

L1:Top L4:Signal
L2:GND L5:VCC
L3:Signal L6:Bottom

Project code:
Inspiron:91.4TY01.001
Vostro :91.4UA01.001
PCB P/N :48.4TY02.0SC
Revision:11282-SC

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PCH Strapping

Chief River Schematic Checklist Revision 1.5

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature).
INIT3_3V#	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low. Leave as "No Connect".
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kOhms resistor
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
DF_TVS	This signal is a strap for selecting DMI and FDI termination voltage. For Ivy Bridge processor only implementation: DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor. For future processor compatibility: It needs to be connected to PROC_SELECT through a 1.0 kOhms ±5% series resistor. The PROC_SELECT signal would need a 2.2 kOhms ±5% pull-up resistor to PCH VccDFTERM.
SATA1GP/ GPIO19	Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Panther Point require SPI flash connected directly to the Panther Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. NOTE: PCI Boot BIOS destination is not supported on mobile.
SATA2GP/ GPIO36	Reserved. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_DOCK_EN# /GPIO33	High Definition Audio Dock Enable: This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the IntelR HD Audio dock signals to the corresponding Panther Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default).If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. Note: The weak internal pull-down is disabled after PLTRST# deasserts. Asserting the HDA_SDO high on the rising edge of PWROK will also halt Intel Management Engine after chipset bring up and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.This signal has a 20k internal pull down resistor.
HDA_SYNC	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform. Note: HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input.Therefore, platform may need to isolate this signal from the codec during the strap phase. Refer to the example circuits provided in the latest Chief River platform design guide.
GPIO15	TLS Confidentiality Low (0) Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE:The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality
L_DDC_DATA	LVDS Detected. When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. NOTE:The internal pull-down is disabled after PLTRST# deasserts.
SDVO_CTRLDATA	Port B Detected When '1'- Port B is detected; When '0'- Port B is not detected This signal has a weak internal pull-down. NOTE:The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected. When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE:The internal pull-down is disabled after PLTRST# deasserts.
DDPD_CTRLDATA	Port D Detected. When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE:The internal pull-down is disabled after PLTRST# deasserts.
GPIO28	The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.If not used, 8.2-k to 10-k pull-up to +V3.3A power-rail. GPIO28 signal also needs to be pulled up to 3.3V_SUS with 4.7K resistor to ensure proper strap setting when use as the chipset test interface.Refer to the latest platform debug design guide and platform design guide for more details. NOTE:This signal has a weak internal pull-up. The internal pull-up is disabled after RSMRST# deasserts.
GPIO29/ SLP_LAN#	GPIO29 is multiplexed with SLP_LAN#. If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN (no other implementation is supported). If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO. A soft strap determines the functionality of GPIO29, either as SLP_LAN# or GPIO. By default, the soft strap enables SLP_LAN# functionality on the pin. If the soft trap is changed to enable GPIO functionality, then SLP_LAN# functionality is no longer available, and the signal can be used as a normal GPIO (default to GPI).

Processor Strapping

Chief River Schematic Checklist Revision 1.5

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	**PCIe Static x16 Lane Numbering Reversal.**	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed	1
CFG[4]	**Display Port Presence strap**	1:Disabled - No Physical Display Port attached to Embedded DisplayPort No connect for disable 0:Enabled - An external Display Port device is connected to the Embedded Display Port Pull-down to GND through a 1K ± 5% resistor to enable port	1
CFG[6:5]	**PCIE Port Bifurcation Straps**	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	1
CFG[17:7]	**Reserved configuration lands. A test point may be placed on the board for these lands.**		

Power Plane

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 ~ 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	 CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

Sandy Bridge + Ivy Bridge Compatibility Requirements

Chief River Schematic Checklist Revision 1.5

Pin Name	Configuration	Schematic Notes
DDR3 VREF	**Sandy Bridge + Ivy Bridge**	DDR3 VREF M1 and M3 Guidelines are required. Note: The M3 traces are routed to the Sandy Bridge Processor reserved pins.
	Ivy Bridge	No change.
PROC_SELECT# & DF_TVS	**Sandy Bridge + Ivy Bridge**	Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1K ±5% series resistor. PROC_SELECT# also needs a 2.2K ±5% pull up resistor to PCH VccDFTERM rail.
	Ivy Bridge	No change.
VCCIO VR Implementation	**Sandy Bridge + Ivy Bridge**	The POR for Ivy Bridge mobile parts is now 1.05 V. There is no longer a requirement for a separate VCCIO VR for Sandy Bridge + Ivy Bridge compatibility.
	Ivy Bridge	No change.
VCCSA_SEL connection to VCCSA_VID[1:0] lines	**Sandy Bridge + Ivy Bridge**	VCCSA_SELECT[0:1] which should be connected to VID[1:0] of the System Agent (SA) VR controller.
	Ivy Bridge	No change.
Layout Requirement on PCI Express Gen3	**Sandy Bridge + Ivy Bridge**	The total motherboard length for a pair of consecutive PCI Express Tx lanes be length matched within 100 mils (2.54 mm)
	Ivy Bridge	No change.
GT Core VR Implementation	**Sandy Bridge + Ivy Bridge**	Depending on the PDDG specifications, some IVB GT2 SKUs may require a new VR controller and 2 phase VCC GT core VR.
	Ivy Bridge	No change.
Processor PCI Express Graphics Guidelines	**Sandy Bridge + Ivy Bridge (PCIe Gen3):**	To support Gen 3 PCI Express Graphic, the value of the AC coupling capacitor should be 180 - 265 nF.
	Ivy Bridge	No change.

PCIE Routing

LANE1	X
LANE2	X
LANE3	Mini Card1(WLAN)
LANE4	x
LANE5	X
LANE6	Onboard LAN
LANE7	X
LANE8	X

USB Table

Pair	Device
0	X
1	USB Ext. port 1
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	x
11	Mini Card1 (WLAN)
12	CAMERA
13	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

<Variant Name>

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Title: Table of Content

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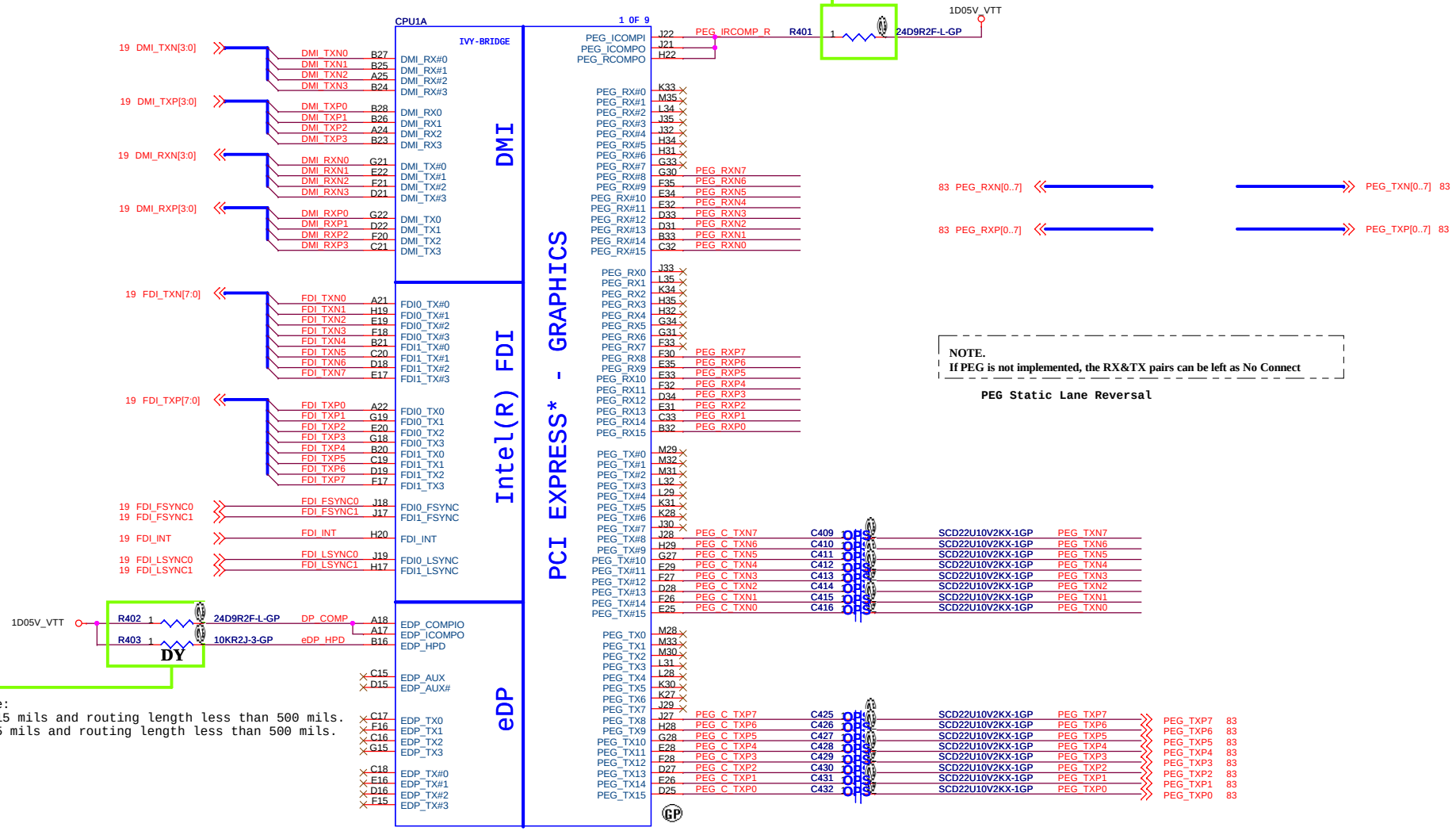
SSID = CPU

Layout Note:
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Layout Note:
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

62.10055.551

2nd = 22.10252.171

3rd = 62.10040.821

<Variant Name>

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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
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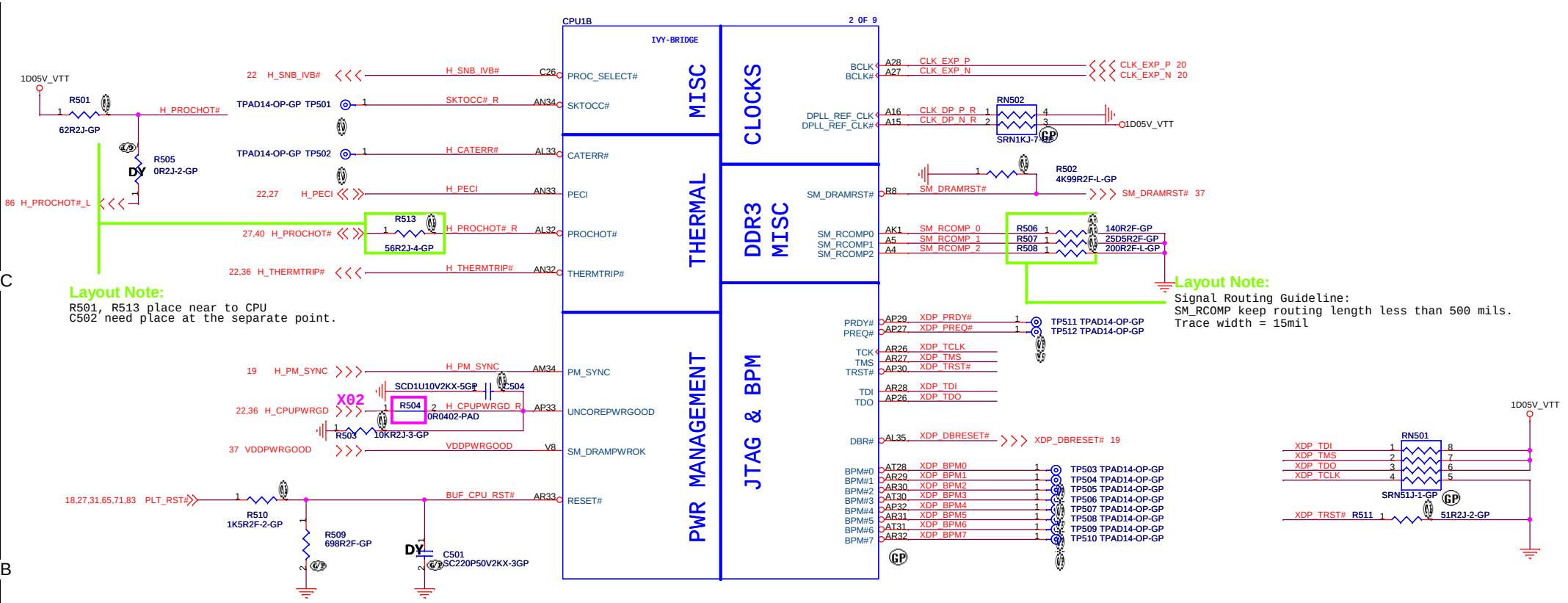

Layout Note:
R501, R513 place near to CPU
C502 need place at the separate point.

Layout Note:
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.
Trace width = 15mil

<Variant Name>

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Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
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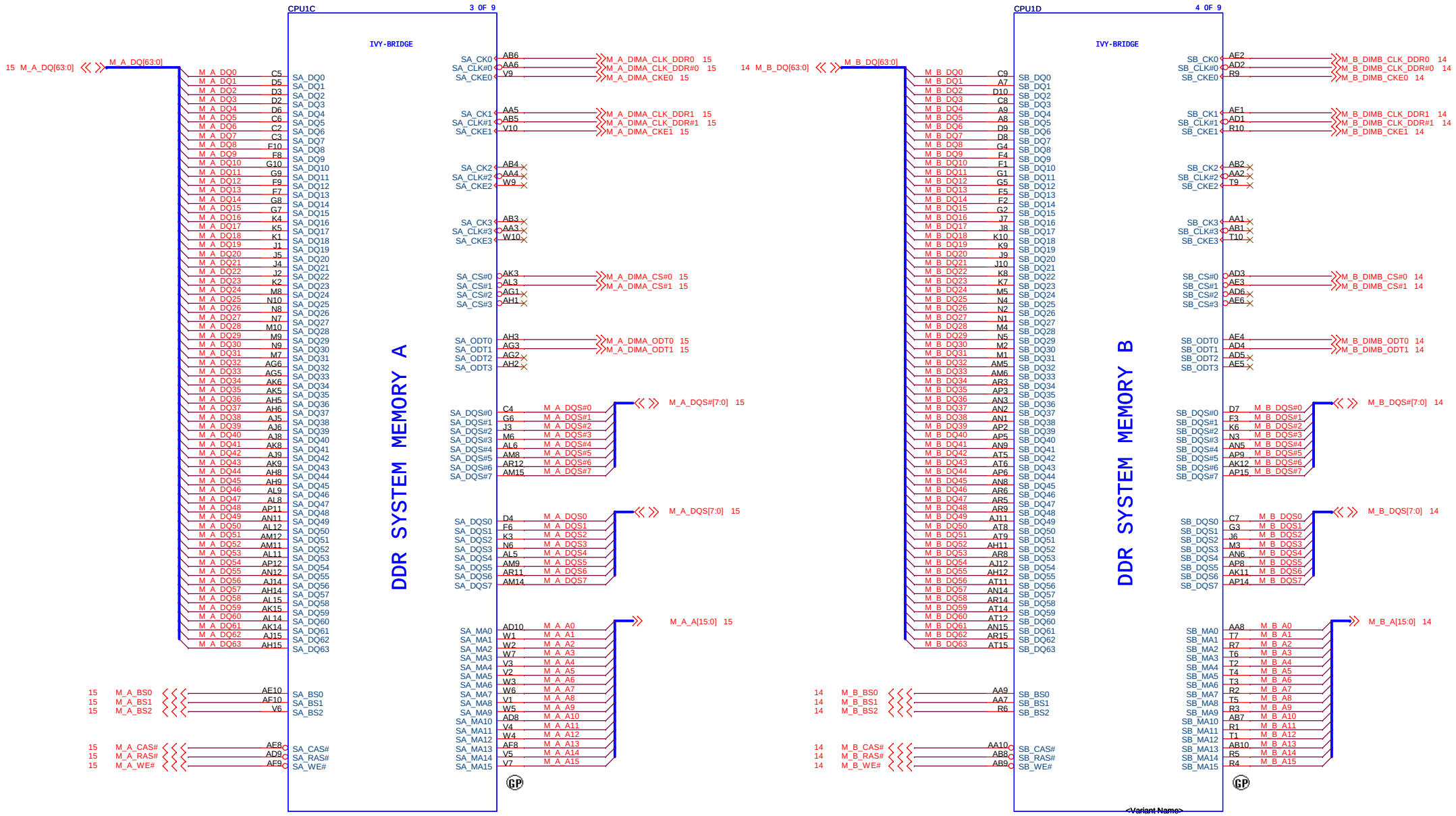
SSID = CPU



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Title: CPU (DDR)		
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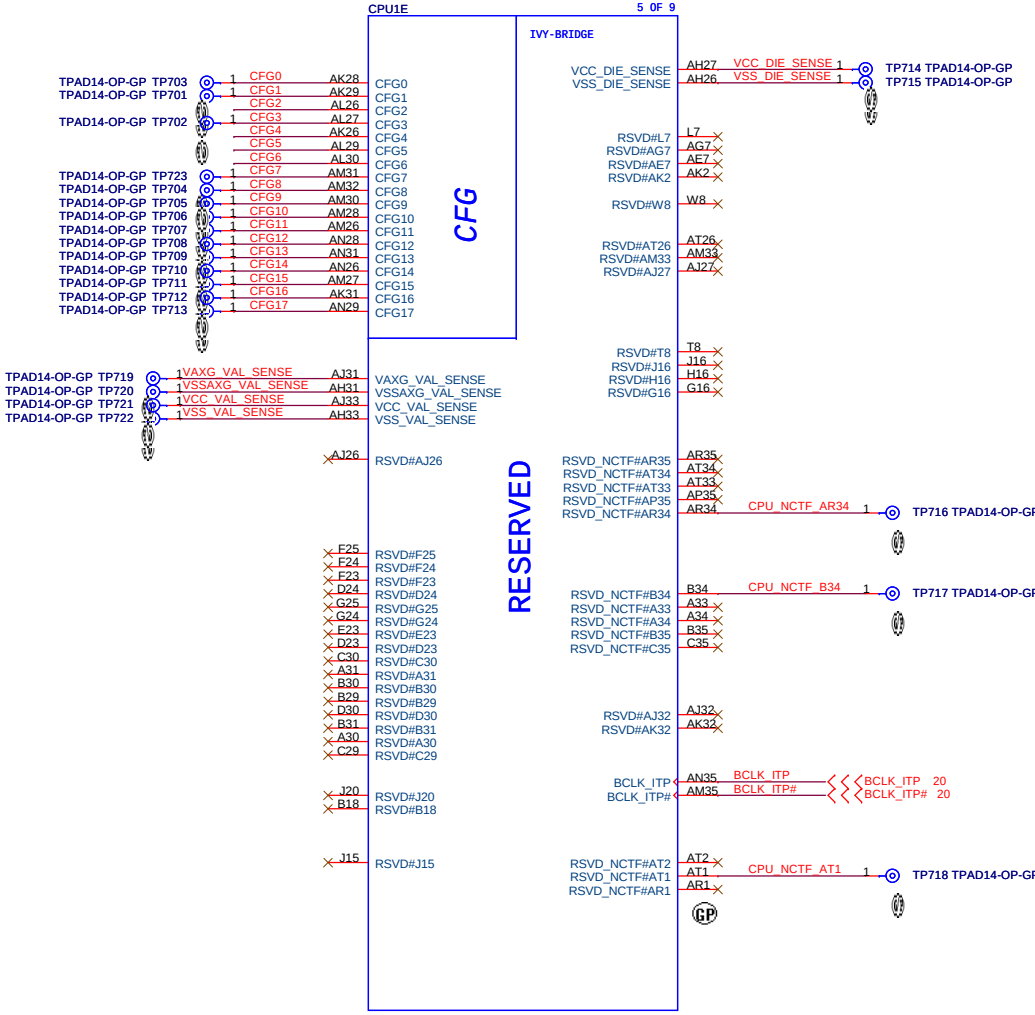
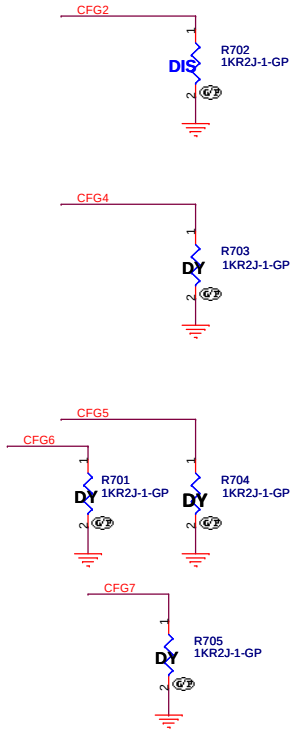
SSID = CPU





PEG Static Lane Reversal

CFG[2]	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

Display Port Presence Strap

CFG[4]	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps

CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Title: CPU (RESERVED)

Size	Document Number	Rev
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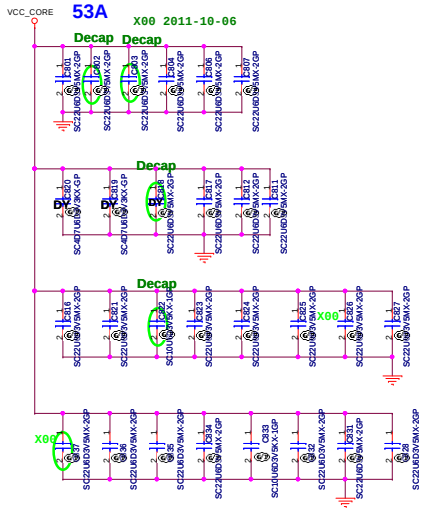
SSID = CPU

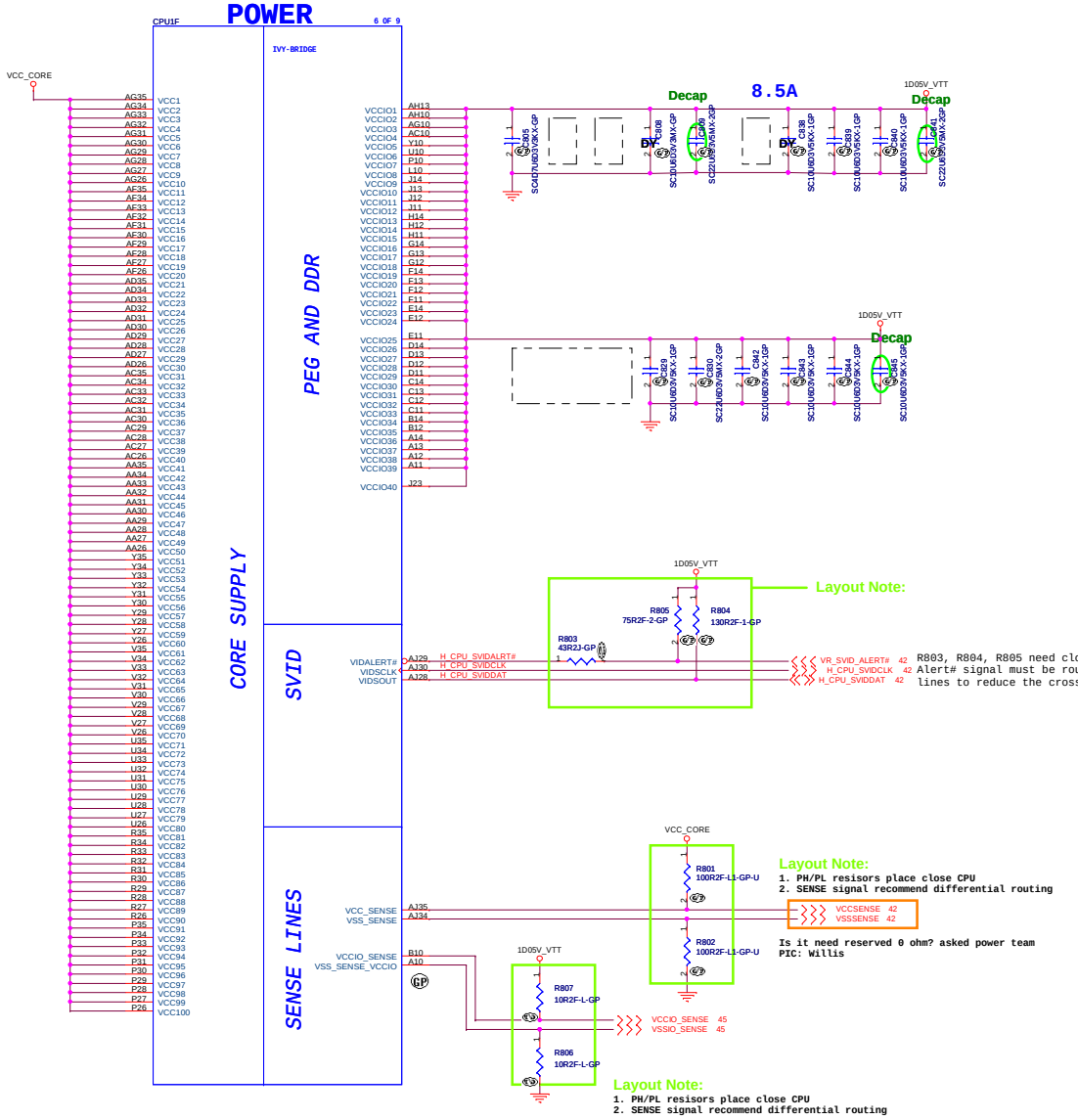
Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE(DC)	0.3~1.35	53
VAXG(DC)	0~1.3	33
VCCIO	1	8.5
VDDQ	1.5	10
VCCSA	0.9	6
VCCPLL	1.8	1.5

Refer to PDDG rev 0.8

PROCESSOR CORE POWER



POWER



<variant_name>

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Title: CPU (VCC_CORE)

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SSID = CPU

POWER

Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE(DC)	0.3~1.35	53
VAXG(DC)	0~1.3	33
VCCIO	1	8.5
VDDQ	1.5	10
VCCSA	0.9	6
VCCPLL	1.8	1.5

Refer to PDDG rev 0.8

CPU1G — IVY-BRIDGE — 7 OF 9

SENSE LINES

VAXG_SENSE (AK35) / VSSAXG_SENSE (AK34) → VCC_AXG_SENSE 42 / VSS_AXG_SENSE 42

VCC_AXG_SENSE / VSS_AXG_SENSE → R906 100R2F-L1-GP-U, R907 100R2F-L1-GP-U

Layout Note:
+V_SM_VREF_CNT should have 10 mil trace width

Layout Note:
1. PH/PL resisors place close CPU
2. SENSE signal recommend differential routing

VREF

SM_VREF (AL1) → +V_SM_VREF_CNT 37

SA_DIMM_VREFDQ (B4) / SB_DIMM_VREFDQ (D1) → DDR_WR_VREFA / DDR_WR_VREFB

GRAPHICS

VAXG1–VAXG54

VCC_GFXCORE — 33A — Decap — De-Cap 22uF x 1 X00-05/30

C901 C902 C906 C908 C920 (SC22U6D3V5MX-2GP)

C900 C927 C928 C929 C921 C924 C926 (SC22U6D3V5MX-2GP)

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

Do not have 2 x 470 uF

DDR3 -1.5V RAILS

1D5V_S0 — 10A — Decap

VDDQ1–VDDQ15

C909 C910 C911 C912 C913 C914 (SC10U6D3V5KX-1GP / SC22U6D3V5MX-2GP)

TC915 ST330U2VDM-4-GP

79.33719.20L
2nd = 77.C3371.13L

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

Do not have 1 x 330 uF

SA RAIL

0D85V_S0 — 6A

VCCSA1–VCCSA8

C934 C936 C935 (SC10U6D3V5KX-1GP)

R910 10R2J-2-GP

VCCSA_SENSE (H23) → 0D85V_S0

R910 close to pin H23.

VCCSA Output Decoupling Recommendation:
1 x 330 uF, 6m
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

Do not have 1 x 330 uF

1.8V RAIL

1D8V_S0 — 1.5A

VCCPLL1–VCCPLL3

C838 C823 C837 (SC10U6D3V5KX-1GP / SC1U10V2KX-1GP)

NEC, 330uF, 2.5V, B2
ESR=9m
Iripple=3.073A

VCCPLL Output Decoupling Recommendation:
1 x 330 uF, 6m
2 x 1 uF (0402) Bottom socket Cavity
1 x 10 uF (0805) Bottom socket edge

Do not have 1 x 330 uF

MISC

VCCSA_VID0 (C22) / VCCSA_VID1 (C24) → VCCSA_SEL0 / VCCSA_SEL1 48

VCCIO_SEL (A19) ← H_SNB_IVB#_PWRCTRL — TP901 TPAD14-OP-GP

VCCIO_SEL:
SNB: Floating
IVY: GND

VCCSA_SEL0 / VCCSA_SEL1 → RN901 SRN1KJ-7-GP (DY)

CRB: 10K
DG: 1K

VCCSA Power Select		
Voltage(V)	VID[0]	VID[1]
0.9	0	0
LV & ULV 0.85	0	1
Others 0.8		
0.725	1	0
0.675	1	1

DDR_WR_VREFA / DDR_WR_VREFB → RN902 SRN1KJ-7-GP (DY)

<Variant Name>

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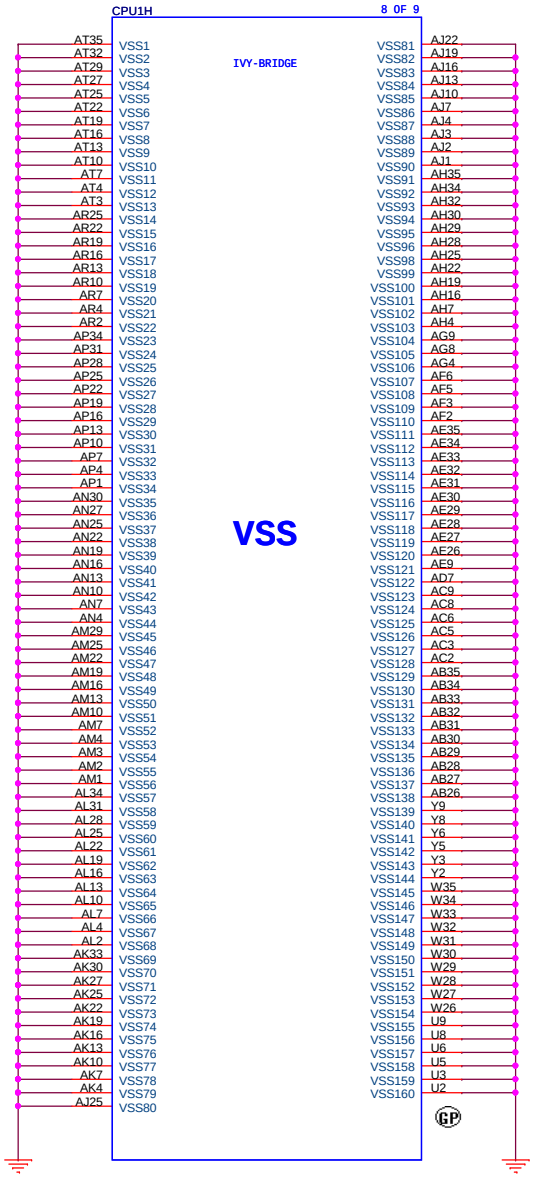
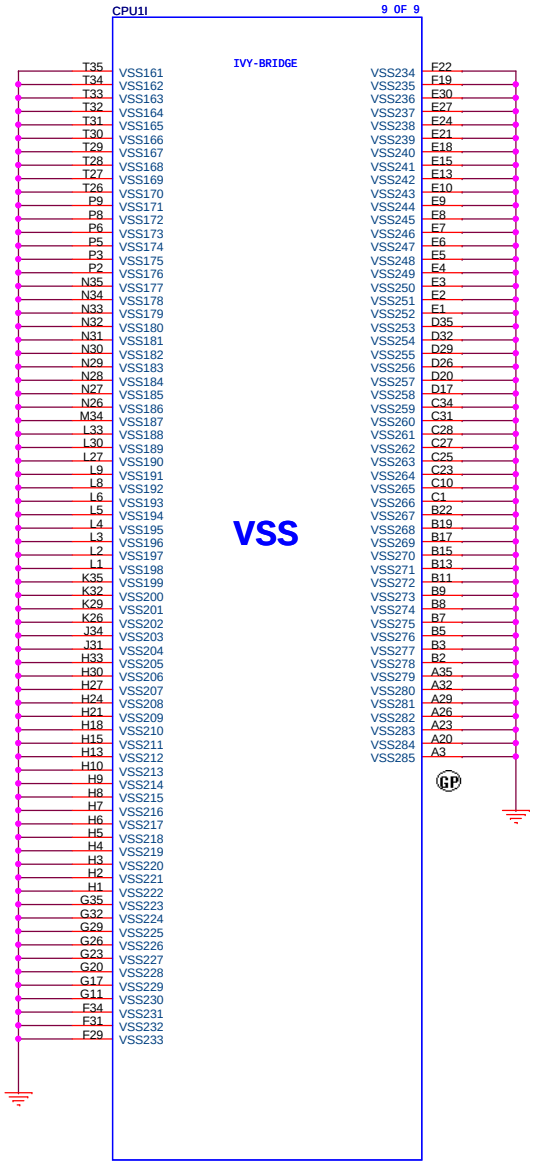
SSID = CPU





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Friday, December 30, 2011 | Sheet 10 of 104

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XDP

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Friday, December 30, 2011 | Sheet 11 of 104

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

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SSID = MEMORY

DDR_VREF_S3

X02

R1405
0R0402-PAD

M_VREF_CA_DIMM1

C1423 SC1U10V2KX-5GP
DY
C1425 SC1U10V3KX-1GP
C1424 SC1U10V2KX-5GP

DDR_VREF_S3

X02

R1404
0R0402-PAD

M_VREF_DQ_DIMM1

C1411 SC1U10V2KX-5GP
DY
C1412 SC2D2U10V3KX-1GP
C1413 SC1U10V2KX-5GP

0D75V_S0

Place these caps close to VTT1 and VTT2.

C1419 SC10U6D3V2KX-GP
DY
C1420 SC10U6D3V2KX-GP
C1421 SC10U6D3V2KX-GP
DY
C1422 SC10U6D3V2KX-GP
DY
C1418 SC10U6D3V6KX-1GP

DM2

M_B_A[15:0] 6

M_B_A0 98
M_B_A1 97
M_B_A2 96
M_B_A3 95
M_B_A4 92
M_B_A5 91
M_B_A6 90
M_B_A7 86
M_B_A8 89
M_B_A9 85
M_B_A10 107
M_B_A11 84
M_B_A12 83
M_B_A13 119
M_B_A14 80
M_B_A15 78

6 M_B_BS2 79
6 M_B_BS0 109
6 M_B_BS1 108
6 M_B_DQ[63:0]

M_B_DQ0 5
M_B_DQ1 7
M_B_DQ2 15
M_B_DQ3 17
M_B_DQ4 4
M_B_DQ5 6
M_B_DQ6 16
M_B_DQ7 18
M_B_DQ8 21
M_B_DQ9 23
M_B_DQ10 33
M_B_DQ11 35
M_B_DQ12 22
M_B_DQ13 24
M_B_DQ14 34
M_B_DQ15 36
M_B_DQ16 39
M_B_DQ17 41
M_B_DQ18 51
M_B_DQ19 53
M_B_DQ20 40
M_B_DQ21 42
M_B_DQ22 50
M_B_DQ23 52
M_B_DQ24 57
M_B_DQ25 59
M_B_DQ26 67
M_B_DQ27 69
M_B_DQ28 58
M_B_DQ29 58
M_B_DQ30 68
M_B_DQ31 70
M_B_DQ32 129
M_B_DQ33 131
M_B_DQ34 141
M_B_DQ35 143
M_B_DQ36 130
M_B_DQ37 132
M_B_DQ38 140
M_B_DQ39 142
M_B_DQ40 147
M_B_DQ41 149
M_B_DQ42 157
M_B_DQ43 159
M_B_DQ44 146
M_B_DQ45 148
M_B_DQ46 158
M_B_DQ47 160
M_B_DQ48 163
M_B_DQ49 165
M_B_DQ50 175
M_B_DQ51 177
M_B_DQ52 164
M_B_DQ53 166
M_B_DQ54 174
M_B_DQ55 176
M_B_DQ56 181
M_B_DQ57 183
M_B_DQ58 191
M_B_DQ59 193
M_B_DQ60 180
M_B_DQ61 182
M_B_DQ62 192
M_B_DQ63 194

M_B_DQS#0 10
M_B_DQS#1 27
M_B_DQS#2 45
M_B_DQS#3 62
M_B_DQS#4 135
M_B_DQS#5 152
M_B_DQS#6 169
M_B_DQS#7 186

M_B_DQS#[7:0] 6

M_B_DQS0 12
M_B_DQS1 29
M_B_DQS2 47
M_B_DQS3 64
M_B_DQS4 137
M_B_DQS5 154
M_B_DQS6 171
M_B_DQS7 188

M_B_DQS[7:0] 6

6 M_B_DIMB_ODT0 116
6 M_B_DIMB_ODT1 120

M_VREF_CA_DIMM1 126
M_VREF_DQ_DIMM1 1

15,37 DDR3_DRAMRST# 30

0D75V_S0 203 204

NP1 NP2
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2
BA0 BA1
RAS# WE# CAS#
CS0# CS1#
CKE0 CKE1
CK0 CK0# CK1 CK1#
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
SDA SCL
EVENT#
VDDSPD
SA0 SA1
NC#1 NC#2 NC#/TEST
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18
VSS
DQS0# DQS1# DQS2# DQS3# DQS4# DQS5# DQS6# DQS7#
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
ODT0 ODT1
VREF_CA VREF_DQ
RESET#
VTT1 VTT2

DDR3-204P-48-GP

M_B_RAS# 6
M_B_WE# 6
M_B_CAS# 6
M_B_DIMB_CS#0 6
M_B_DIMB_CS#1 6
M_B_DIMB_CKE0 6
M_B_DIMB_CKE1 6
M_B_DIMB_CLK_DDR0 6
M_B_DIMB_CLK_DDR#0 6
M_B_DIMB_CLK_DDR1 6
M_B_DIMB_CLK_DDR#1 6

PCH_SMBDATA 15,20,65
PCH_SMBCLK 15,20,65
TS#_DIMM0_1 15
SA0_DIM1
SA1_DIM1

1D5V_S3

3D3V_S0

R1402 10KR2J-3-GP
SA1_DIM1
SA0_DIM1
R1401 10KR2J-3-GP

C1401 SCD1U10V2KX-5GP
DY
C1402 SC2D2U10V3KX-1GP

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

TS#_DIMM0_1
R1403 10KR2J-3-GP
3D3V_S0

SODIMM A DECOUPLING

1D5V_S3

79.33719.20L
2nd = 77.C3371.13L

TC1401 ST330U2V0M14-GP
DY
C1403 SC10U6D3V6KX-1GP
C1404 SC10U6D3V6KX-1GP
DY
C1405 SCD1U10V2KZ-1GP
C1406 SC10U6D3V6KX-1GP
DY
C1407 SC10U6D3V6KX-1GP
DY
C1408 SCD1U10V2KZ-1GP
C1409 SC10U6D3V6KX-1GP
DY
C1410 SC10U6D3V6KX-1GP

Decap Decap Decap Decap
C1415 SCD1U10V2KX-GP
C1416 SCD1U10V2KX-GP
C1417 SCD1U10V2KX-GP
C1418 SCD1U10V2KX-GP

Layout Note:
Place these Caps near SO-DIMMA.

X00

1D5V_S0 1D5V_S3

C1426 DY SCD1U10V2KX-5GP
C1427 DY SCD1U10V2KX-5GP
C1428 DY SCD1U10V2KX-5GP
C1429 DY SCD1U10V2KX-5GP

Layout Note:
For S3 reduction circuit's 1D5V return pass.

62.10017.P41
2nd = 62.10017.P61
3rd = 62.10017.N41

<Variant Name>

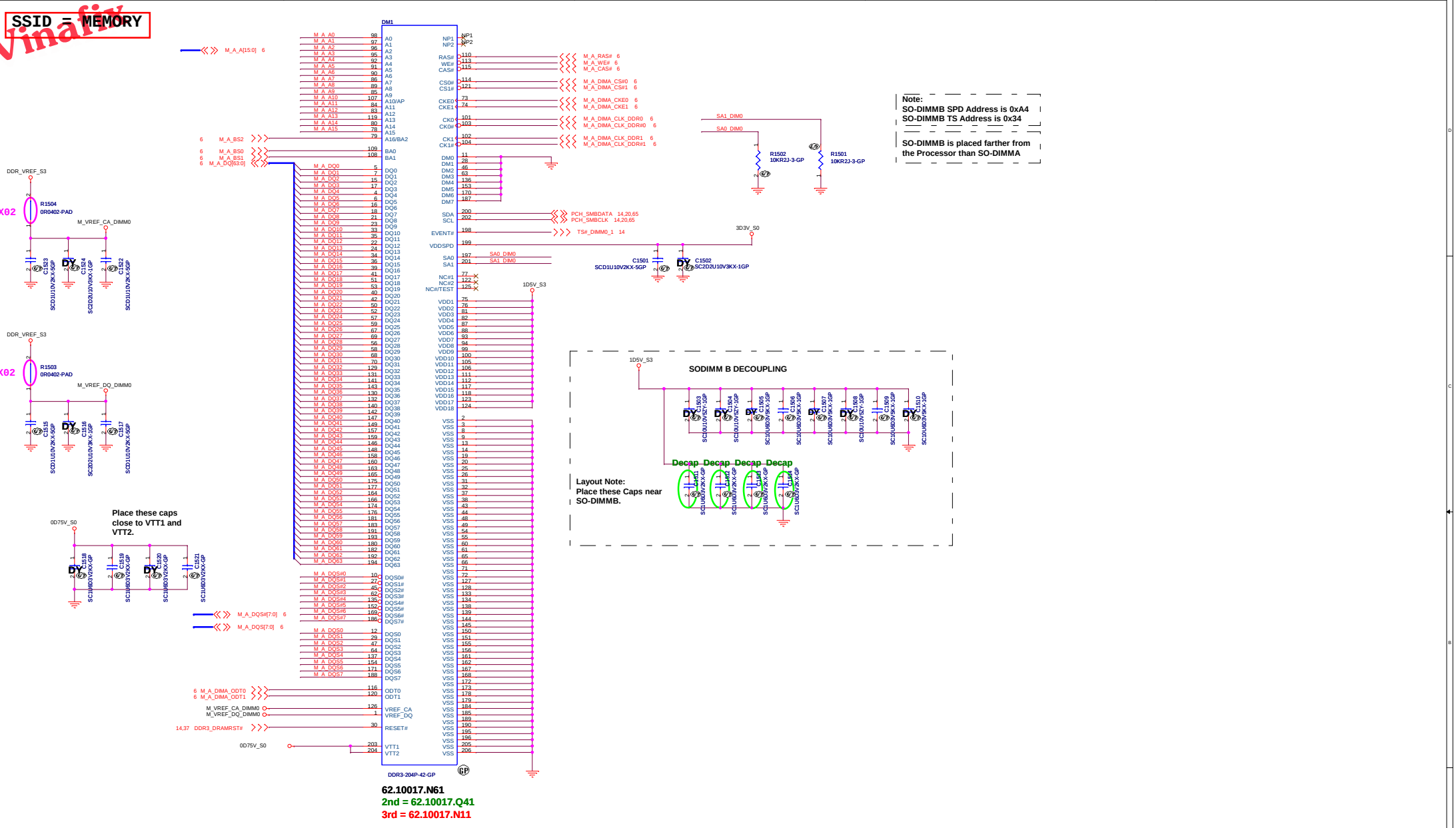
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: A2 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Tuesday, January 03, 2012 | Sheet 14 of 104

SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

62.10017.N61
2nd = 62.10017.Q41
3rd = 62.10017.N11

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size	Document Number	Rev
A2	Enrico Caruso 14 MLK DIS	X02

Date: Tuesday, January 03, 2012 Sheet 15 of 104

(Blanking)

<Variant Name>

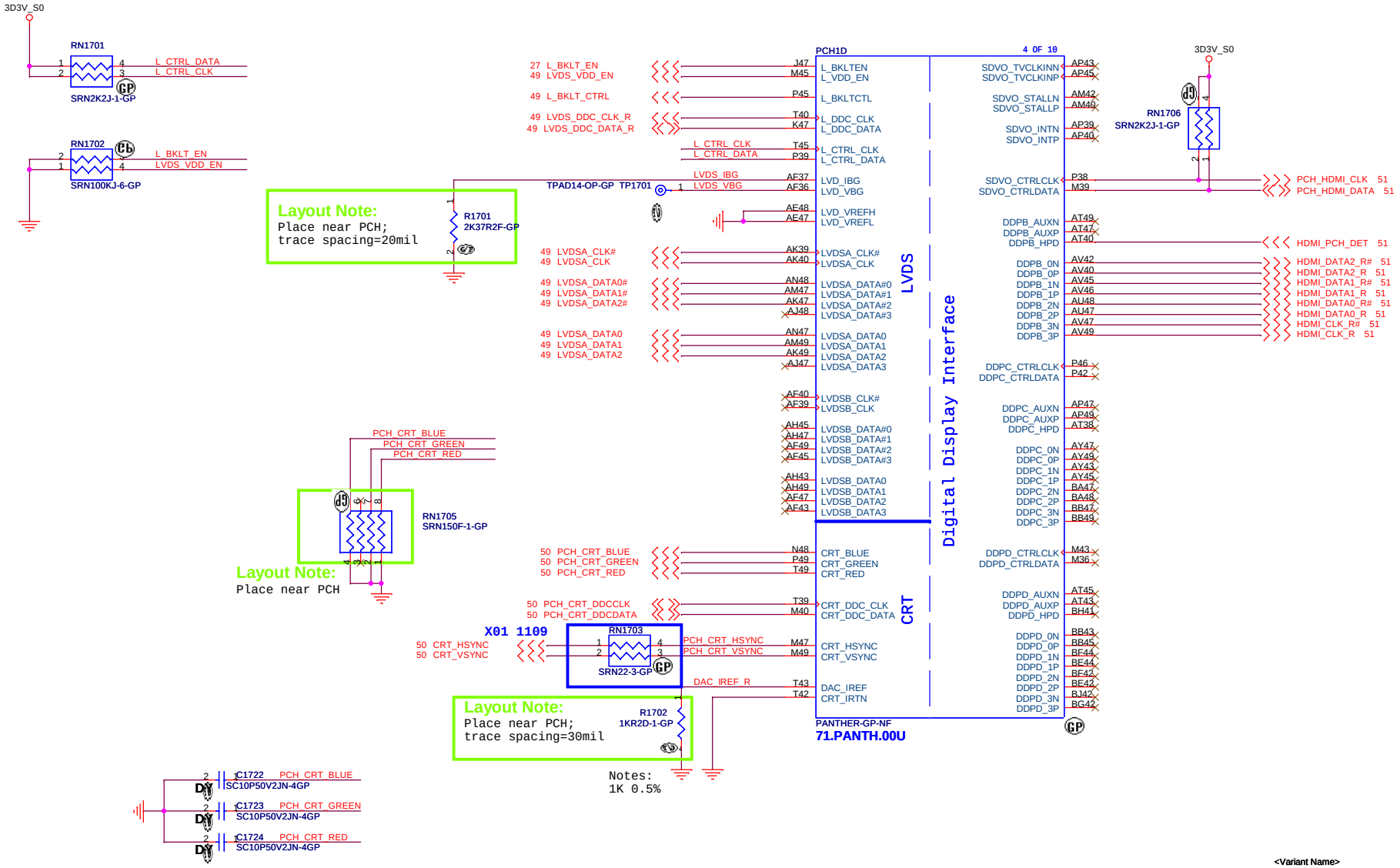
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico Caruso 14 MLK DIS*	*X02*

Date: Friday, December 30, 2011 Sheet 16 of 104

SSID = PCH



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

Date: Tuesday, January 03, 2012 Sheet 17 of 104

SSID = PCH

USB Table

Pair	Device
0	NC
1	USB2.0 port1
2	NC
3	NC
4	NC
5	Card reader
6	NC
7	NC
8	USB2.0 port2
9	USB2.0 port3
10	NC
11	Mini Card1
12	CAMERA
13	NC

USB3.0/2.0 Mapping Table

USB 3.0 Port	USB 2.0 port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

USB2.0 Signal Group

Layout Note:
1. USBRBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil

Boot Bios Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

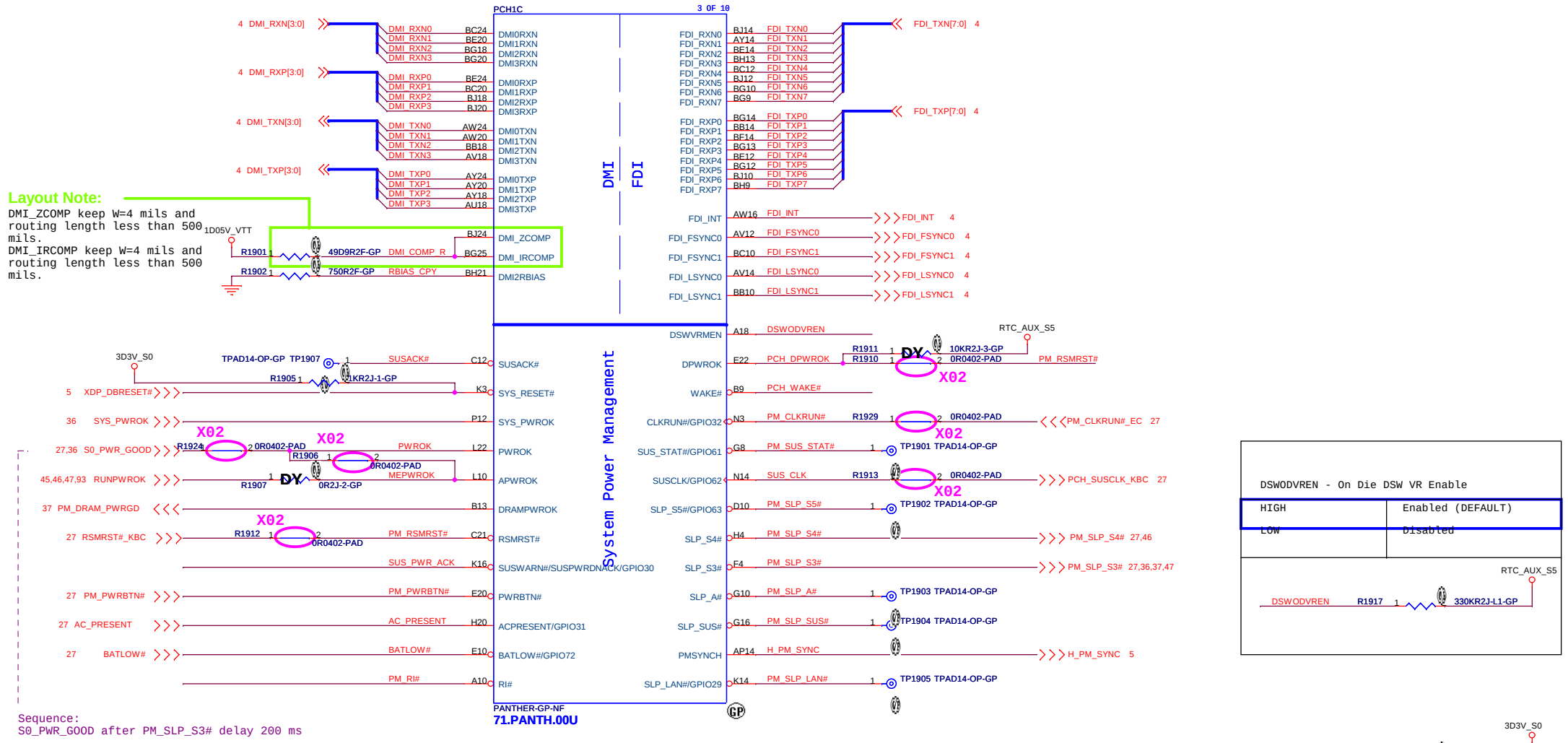
A16 Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02
Date: Tuesday, January 03, 2012 | Sheet 18 of 104

SSID = PCH



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5
DSWODVREN R1917 330KR2J-1-GP

Sequence:
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

3D3V_S0
PM_CLKRUN# R1919 8K2R2J-3-GP

3D3V_S5
RN1901 SRN10KJ-6-GP
BATLOW#
PCH_WAKE#
PM_RI#
SUS_PWR_ACK
R1909 100KR2J-1-GP AC_PRESENT
R1922 10KR2J-3-GP PM_PWRBTN#
R1920 10KR2J-3-GP PM_SLP_LAN#
R1908 10KR2J-3-GP PM_RSMRST#
R1926 100KR2J-1-GP SYS_PWROK
R1904 100KR2J-1-GP PWROK

PCIE_WAKE#:
CRB: 1K
CEKLT: 10K

PCH_SUSCLK_KBC
EC1901 SC4D7P50V2CN-1GP

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCH (DMI/FDI/PM)		
Size A3	Document Number: Enrico Caruso 14 MLK DIS	Rev X02
Date: Tuesday, January 03, 2012	Sheet 19 of 104	

SSID = PCH

X00

S5 power rail CLKREQ#:
PCIECLKRQ[0]#
PCIECLKRQ[7:2]#

PCIE_CLK_RQ0#
PCIE_CLK_RQ4#
PCIE_CLK_RQ3#

RN2001
SRN10KJ-L3-GP

PCIE_CLK_REQ0# → EC_SW#
PCIE_CLK_REQ4# → PCIE_CLK_LAN_REQ#
PCIE_CLK_REQ3# → CLK_PCIE_NEW_REQ#
3D3V_S5 → PEG_B_CLKRQ#

PCIE_CLK_RQ5#
PCIE_CLK_RQ7#
PCIE_CLK_RQ6#

PCH1B — 2 OF 10

BG34 PERN1 / BJ34 PERP1 / AV32 PETN1 / AU32 PETP1	NC	
BE34 PERN2 / BF34 PERP2 / BB32 PETN2 / AY32 PETP2	NC	
BG36 PERN3 / BJ36 PERP3 / AV34 PETN3 / AU34 PETP3	NC	
BF36 PERN4 / BE36 PERP4 / AY34 PETN4 / BB34 PETP4	WLAN	PCI-E*
BG37 PERN5 / BH37 PERP5 / AY36 PETN5 / BB36 PETP5	NC	
BJ38 PERN6 / BG38 PERP6 / AU36 PETN6 / AV36 PETP6	LAN	
BG40 PERN7 / BJ40 PERP7 / AY40 PETN7 / BB40 PETP7	NC	
BE38 PERN8 / BC38 PERP8 / AW38 PETN8 / AY38 PETP8	NEW CARD	

65 PCIE_RXN4 / 65 PCIE_RXP4 / 65 PCIE_TXN4 / 65 PCIE_TXP4
C2005 SCD1U10V2KX-5GP PCIE_TXN4_C
C2006 SCD1U10V2KX-5GP PCIE_TXP4_C

31 PCIE_RXN2 / 31 PCIE_RXP2 / 31 PCIE_TXN2 / 31 PCIE_TXP2
C2001 SCD1U10V2KX-5GP PCIE_TXN2_C
C2002 SCD1U10V2KX-5GP PCIE_TXP2_C

S0 power rail CLKREQ#:
PCIECLKRQ[2:1]#

CLKOUT termination
place close to PCH <500mil

X00

RN2018
SRN10KJ-5-GP

CLK_PCIE_WLAN_REQ# / CLK_PCIE_WWAN_REQ# → PCIE_CLK_RQ2# / PCIE_CLK_RQ1#

Layout Note:

Y40 CLKOUT_PCIE0N / Y39 CLKOUT_PCIE0P	PCIE_CLK_REQ0# → J2 PCIECLKRQ0#/GPIO73	N/A
AB49 CLKOUT_PCIE1N / AB47 CLKOUT_PCIE1P	CLK_PCIE_WWAN_REQ# → M1 PCIECLKRQ1#/GPIO18	N/A
AA48 CLKOUT_PCIE2N / AA47 CLKOUT_PCIE2P	CLK_PCH_SRC2_N / CLK_PCH_SRC2_P	WLAN CLK
	65 CLK_PCIE_WLAN# / 65 CLK_PCIE_WLAN / 65 CLK_PCIE_WLAN_REQ# — RN2012 0R4P2R-PAD — X02 1229 — V10 PCIECLKRQ2#/GPIO20	
Y37 CLKOUT_PCIE3N / Y36 CLKOUT_PCIE3P	PCIE_CLK_REQ3# → A8 PCIECLKRQ3#/GPIO25	N/A
Y43 CLKOUT_PCIE4N / Y45 CLKOUT_PCIE4P	PCIE_CLK_REQ4# → L12 PCIECLKRQ4#/GPIO26	N/A
V45 CLKOUT_PCIE5N / V46 CLKOUT_PCIE5P	CLK_PCH_SRC5_N / CLK_PCH_SRC5_P	LAN CLK
	31 CLK_PCIE_LAN# / 31 CLK_PCIE_LAN / 31 PCIE_CLK_LAN_REQ# — RN2014 0R4P2R-PAD — X02 1229 — L14 PCIECLKRQ5#/GPIO44	
AB42 CLKOUT_PEG_B_N / AB40 CLKOUT_PEG_B_P	PEG_B_CLKRQ# → E6 PEG_B_CLKRQ#/GPIO56	N/A
V40 CLKOUT_PCIE6N / V42 CLKOUT_PCIE6P	PCIE_CLK_REQ6# → T13 PCIECLKRQ6#/GPIO45	N/A
V38 CLKOUT_PCIE7N / V37 CLKOUT_PCIE7P	CLK_PCIE_NEW_REQ# → K12 PCIECLKRQ7#/GPIO46	New Card CLK
AK14 CLKOUT_ITPXDP_N / AK13 CLKOUT_ITPXDP_P	PCIE_CLK_XDP_N_R / PCIE_CLK_XDP_P_R	

7 BCLK_ITP# / 7 BCLK_ITP — RN2023 DY — SRN0J-6-GP

CLOCKS

PANTHER-GP-NF
71.PANTH.00U

SMBUS

SMBALERT#/GPIO11 E12	EC_SW#	EC_SW# 27
SMBCLK H14	SMB_CLK	
SMBDATA C9	SMB_DATA	
SML0ALERT#/GPIO60 A12	DRAMRST_CNTRL_PCH	DRAMRST_CNTRL_PCH 37
SML0CLK C8	SML0_CLK	
SML0DATA G12	SML0_DATA	
SML1ALERT#/PCHHOT#/GPIO74 C13	PCH_GPIO74	
SML1CLK/GPIO58 E14	SML1_CLK	SML1_CLK 27
SML1DATA/GPIO75 M16	SML1_DATA	SML1_DATA 27

Controller Link

CL_CLK1 M7	CL_CLK	TP2001 TPAD14-OP-GP
CL_DATA1 T11	CL_DATA	TP2002 TPAD14-OP-GP
CL_RST1# P10	CL_RST#	TP2003 TPAD14-OP-GP

FLEX CLOCKS

PEG_A_CLKRQ#/GPIO47 M10	PEG_CLKREQ#	PEG_CLKREQ# 83
CLKOUT_PEG_A_N AB37 / CLKOUT_PEG_A_P AB38	CLKOUT_PEG_A_N / CLKOUT_PEG_A_P	CLK_PCIE_VGA# 83 / CLK_PCIE_VGA 83
CLKOUT_DMI_N AV22 / CLKOUT_DMI_P AU22	CLKOUT_DMI_N / CLKOUT_DMI_P	CLK_EXP_N 5 / CLK_EXP_P 5
CLKOUT_DP_N AM12 / CLKOUT_DP_P AM13		
CLKIN_DMI_N BF18 / CLKIN_DMI_P BE18	CLK_BUF_EXP_N / CLK_BUF_EXP_P	RN2019 SRN10KJ-5-GP
CLKIN_GND1_N BJ30 / CLKIN_GND1_P BG30	CLK_BUF_CPYCLK_N / CLK_BUF_CPYCLK_P	RN2008 SRN10KJ-5-GP
CLKIN_DOT_96N G24 / CLKIN_DOT_96P E24	CLK_BUF_DOT96_N / CLK_BUF_DOT96_P	RN2020 SRN10KJ-5-GP
CLKIN_SATA_N AK7 / CLKIN_SATA_P AK5	CLK_BUF_CKSSCD_N / CLK_BUF_CKSSCD_P	RN2021 SRN10KJ-5-GP
REFCLK14IN K45	CLK_BUF_REF14	R2008 10KR2J-3-GP
CLKIN_PCILOOPBACK H45	CLK_PCI_FB	CLK_PCI_FB 18
XTAL25_IN V47 / XTAL25_OUT V49	XTAL25_IN / XTAL25_OUT	22 BOARD_ID2
XCLK_RCOMP Y47	XCLK_RCOMP	R2007 90D9R2F-1-GP +VCCDIFFCLKN
CLKOUTFLEX0/GPIO64 K43	JTAG_TCK	R2001 DY 22R2J-2-GP JTAG_TCK_VGA 86
CLKOUTFLEX1/GPIO65 F47	CLK_PCH_48M_L	X00 R2002 22R2J-2-GP CLK_PCH_48M 32
CLKOUTFLEX2/GPIO66 H47	CLK_27M_VGA_R	TP2006 TPAD14-OP-GP
CLKOUTFLEX3/GPIO67 K49	BOARD_ID1	

Layout Note:
CLKOUT termination
place close to PCH <500mil

RN2016 0R4P2R-PAD
RN2010 0R4P2R-PAD
X02 1229

X02 1223
3D3V_S5 — R2005 10KR2J-3-GP — PEG_CLKREQ# — R2004 10KR2J-3-GP DY

SMB_CLK / SMB_DATA — RN2003 SRN2K2J-1-GP
SML0_DATA / SML0_CLK — RN2004 SRN2K2J-1-GP
SML1_CLK / SML1_DATA — RN2005 SRN2K2J-1-GP
PCIE_CLK_REQ6# / PCH_GPIO74 — RN2006 SRN10KJ-5-GP
DRAMRST_CNTRL_PCH — R2009 1KR2J-1-GP

3D3V_S0 — RN2009 SRN4K7J-5-GP
3rd = 84.DMN66.03F
2nd = 84.2N702.A3F
84.2N702.F3F
SML1_DATA — Q2002 ME2N7002DKW-G-GP — THM_SML1_DATA 28,86
SML1_CLK — THM_SML1_CLK 28,86

CRB : 1K
CHKLT: 10K

3D3V_S0 — RN2007 SRN2K2J-1-GP
3rd = 84.DMN66.03F
2nd = 84.2N702.A3F
84.2N702.F3F
SMB_DATA — Q2001 ME2N7002DKW-G-GP — PCH_SMBDATA 14,15,65
SMB_CLK — PCH_SMBCLK 14,15,65

XTAL25_IN — X2001 — C2008 SC15P50V2JN-2-GP
R2006 1M1R2J-GP
C2007 SC15P50V2JN-2-GP
XTAL25_OUT — XTAL-25MHZ-155-GP1
82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61

3D3V_S0 — X00 — R2013 10KR2J-3-GP — R2012 10KR2J-3-GP
BOARD_ID2 / BOARD_ID1
R2011 10KR2J-3-GP DY — R2010 10KR2J-3-GP DY

BIOS UMA/Discrete Strap pin

	BOARD_ID1	BOARD_ID2
PX(AMD)	0	0
DIS	0	1
UMA	1	0
Optimus(NV)	1	1

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)
Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02
Date: Tuesday, January 03, 2012 | Sheet 20 of 104

SSID = PCH

Layout Note:
Place it at the open door location.

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

Table 165. RTC Routing Guidelines

Signal Name	Trace Width (W) and Spacing (S)	Stackup (MS/SL/DSL)	Total Length	Reference Figure	Notes
RTCX1 RTCX2	W = 4 mils (0.102 mm) S > 15 mils (0.381 mm)	MS	Max = 1000 mils (25.4 mm)	Figure 183	1
RTCX1 RTCX2	W = 3.5 mils (0.089 mm) S > 15 mils (0.381 mm)	SL			
RTCX1 RTCX2	W = 4.5 mils (0.114 mm) S > 15 mils (0.381 mm)	DSL			
RTCRST# SRTCRST#	W = 4 mils (0.102 mm) S > 15 mils (0.381 mm)	MS	Max = 8000 mils (203.2 mm)	Figure 184 Figure 185	1, 2
RTCRST# SRTCRST#	W = 3.5 mils (0.089 mm) S > 15 mils (0.381 mm)	SL			
RTCRST# SRTCRST#	W = 4.5 mils (0.114 mm) S > 15 mils (0.381 mm)	DSL			

NOTES:
1. Impedance Target 50 Ω ±15% for Microstrip and 50 Ω ±10% for Stripline and Dual-Stripline.
2. RC time delay between 18 ms-25 ms must be met.

RTC_AUX_S5 — RN2106 SRN20KJ-1-GP — C2104 SC1U6D3V2KX-GP — G2101 GAP-OPEN

27 RTCRST_ON — Q2102 2N7002BK-GP — R2125 10KR2J-3-GP — 84.07002.I31 — 2nd = 84.2N702.W31 — 3rd = 84.2N702.J31

C2103 SC1U6D3V2KX-GP — R2104 1M1R2J-GP — R2105 330KR2F-L-GP

PCH1A — 1 OF 10 — PANTHER-GP-NF — 71.PANTH.00U

RTC_X1	A20	RTCX1
RTC_X2	C20	RTCX2
RTC_RST#	D20	RTCRST#
SRTC_RST#	G22	SRTCRST#
SM_INTRUDER#	K22	INTRUDER#
PCH_INTVRMEN	C17	INTVRMEN
HDA_BITCLK	N34	HDA_BCLK
HDA_SYNC	L34	HDA_SYNC
HDA_SPKR	T10	SPKR
HDA_RST#	K34	HDA_RST#
HDA_SDIN0	E34	HDA_SDIN0
	G34	HDA_SDIN1
	C34	HDA_SDIN2
	A34	HDA_SDIN3
HDA_SDOUT	A36	HDA_SDO
PCH_GPIO33	C36	HDA_DOCK_EN#/GPIO33
PCH_GPIO13	N32	HDA_DOCK_RST#/GPIO13
PCH_JTAG_TCK_BUF	J3	JTAG_TCK
PCH_JTAG_TMS	H7	JTAG_TMS
PCH_JTAG_TDI	K5	JTAG_TDI
PCH_JTAG_TDO	H1	JTAG_TDO
PCH_SPI_CLK	T3	SPI_CLK
PCH_SPI_CS0#	Y14	SPI_CS0#
	T1	SPI_CS1#
PCH_SPI_SI	V4	SPI_MOSI
	U3	SPI_MISO

RTC: RTC_X1, RTC_X2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN

IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO

JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO

SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

LPC: FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME#, LDRQ0#, LDRQ1#/GPIO23, SERIRQ

SATA: SATA 6G ports, SATAICOMPO, SATAICOMPI, SATA3RCOMPO, SATA3COMPI, SATA3RBIAS, SATALED#, SATA0GP/GPIO21, SATA1GP/GPIO19

LPC_AD[3..0] — LPC_AD0 — LPC_AD1 — LPC_AD2 — LPC_AD3 — LPC_FRAME# — KB_DET# 69 — INT_SERIRQ 27

HDD1
SATA_RXN0 56 — SATA_RXP0 56 — SATA_TXN0 56 — SATA_TXP0 56

ODD
SATA_RXN4 56 — SATA_RXP4 56 — SATA_TXN4 56 — SATA_TXP4 56

ESATA

SATA_COMP — R2112 37D4R2F-GP
SATA3_COMP — R2113 49D9R2F-GP
RBIAS_SATA3 — R2114 750R2F-GP

Layout Note:
Place close PCH(<500mil)

SATA_LED# 68 — SATA_DET#0 — BBS_BIT0 18

Layout Note: Place close together.

29 HDA_CODEC_SDOUT — 33R2J-2-GP — R2123 HDA_SDOUT
29 HDA_CODEC_RST# — RN2102 SRN33J-5-GP-U — HDA_RST#
29 HDA_CODEC_BITCLK — HDA_BITCLK

Layout Note:
HDA_SDO and HDA_BCLK must be length matched to within 500 mils

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

27 ME_UNLOCK — R2107 1KR2J-1-GP — HDA_SDOUT

TPAD14-OP-GP TP2105 — PCH_GPIO33
TPAD14-OP-GP TP2106 — PCH_GPIO13

X00
1D05V_VTT — follow DPDG 1.3
R2111 DY 51R2J-2-GP — PCH_JTAG_TCK_BUF
R2118 DY 51R2J-2-GP — PCH_JTAG_TMS
R2119 DY 51R2J-2-GP — PCH_JTAG_TDI
R2120 DY 51R2J-2-GP — PCH_JTAG_TDO

+3VS_+1.5VS_HDA_IO — R2102 DY 1KR2J-1-GP — HDA_SDOUT

3D3V_S0 — R2106 DY 1KR2J-1-GP — HDA_SPKR

No Reboot Strap	
HDA_SPKR	Low = Default * High = No Reboot

27,60 SPI_CLK_R — R2108 33R2J-2-GP — PCH_SPI_CLK
27,60 SPI_CS0#_R — R2109 33R2J-2-GP — PCH_SPI_CS0#
27,60 SPI_SI_R — R2110 33R2J-2-GP — PCH_SPI_SI
60 SPI_SO_R

+3VS_+1.5VS_HDA_IO — R2103 1KR2J-1-GP — HDA_SYNC

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V High = 1.5V *

RUN_ENABLE — Q2101 2N7002BK-GP
29 HDA_CODEC_SYNC — R2124 33R2J-2-GP — HDA_CODEC_SYNC_R — HDA_SYNC
R2117 100KR2J-1-GP
84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31

HDA_CODEC_BITCLK — DY EC2102 SC4D7P50V2CN-1GP
HDA_CODEC_SDOUT — DY EC2103 SC4D7P50V2CN-1GP

HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

Layout Note:
close to branch point

RTC_X1 — R2101 10MR2J-L-GP — RTC_X2
X2101 X-32D768KHZ-40GPU
C2101 SC15P50V2JN-2-GP — C2102 SC15P50V2JN-2-GP
82.30001.841
2nd = 82.30001.A41

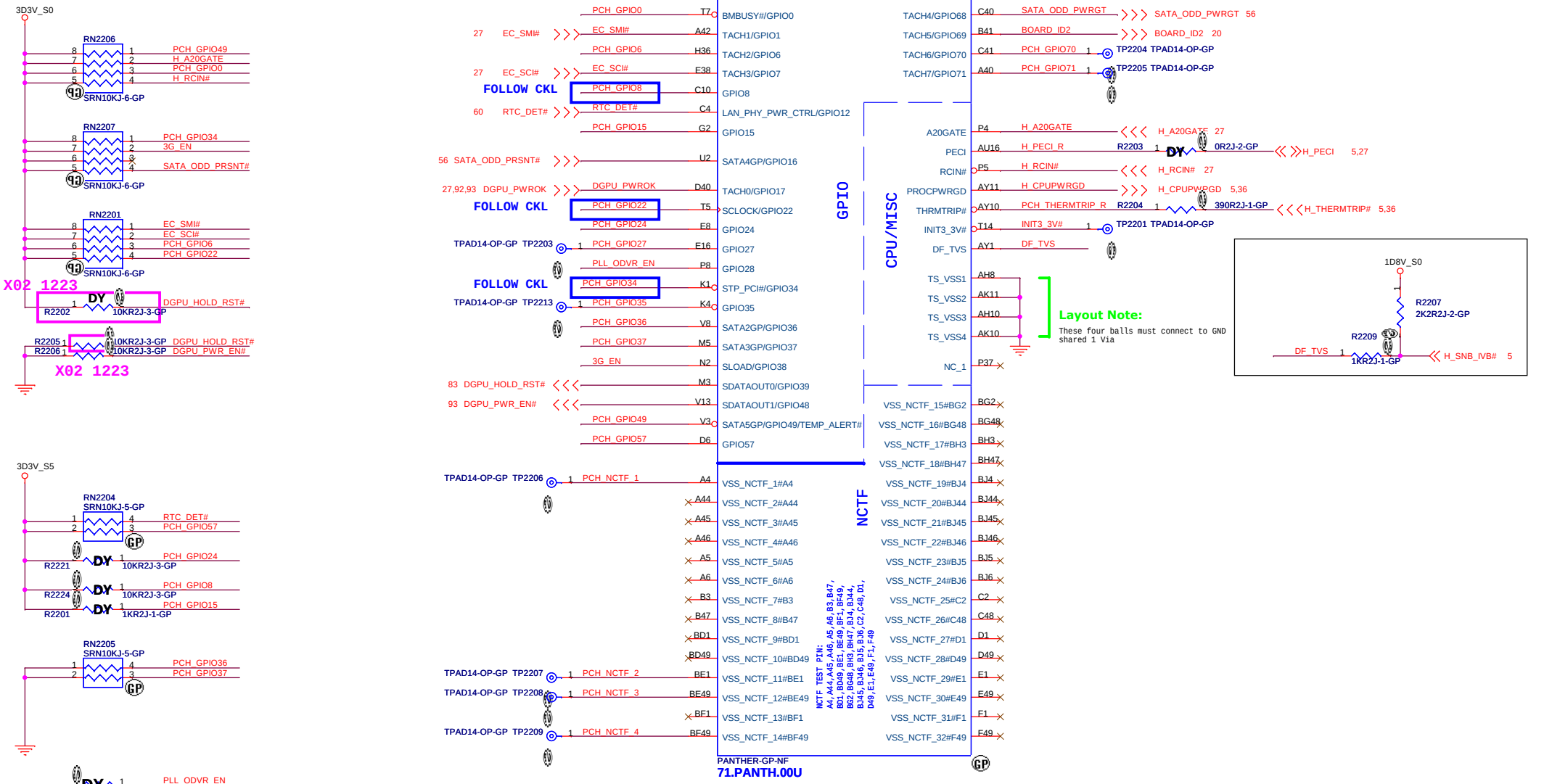
INT_SERIRQ — RN2103 SRN10KJ-5-GP — SATA_DET#0 — 3D3V_S0

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/HDA)
Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02
Date: Tuesday, January 03, 2012 | Sheet 21 of 104

SSID = PCH



PLL ON DIE VR ENABLE	
GPIO28 (PLL_ODVR_EN)	Weakly internal pull up 20k. High - Enable LOW - Disable

<Variant Name>

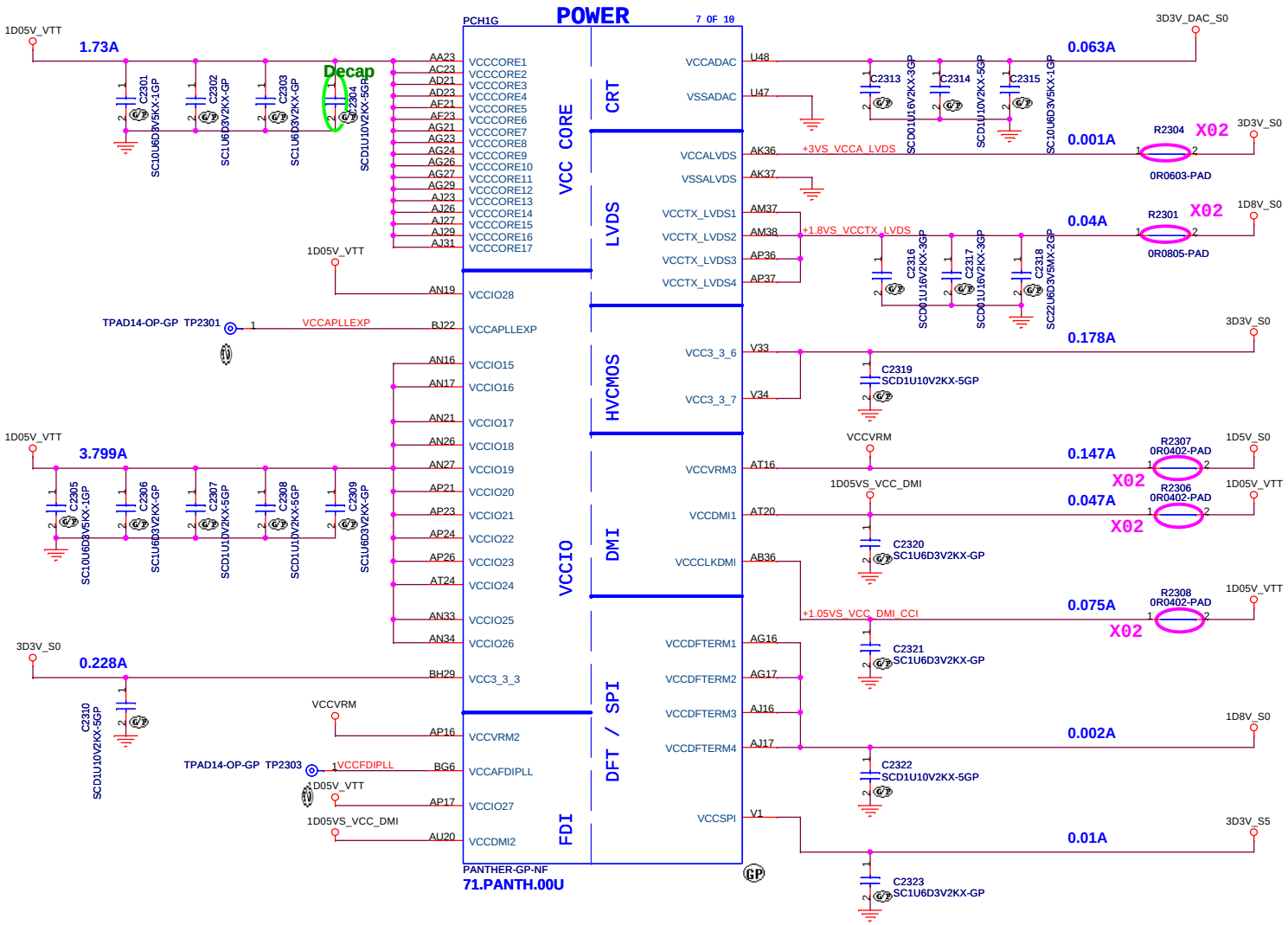
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

Date: Tuesday, January 03, 2012 Sheet 22 of 104

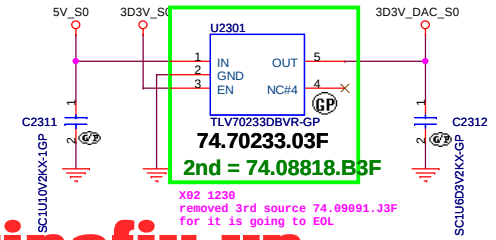
SSID = PCH



Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccClkDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.05
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to PCH EDS V1.5
(General DC Characteristicschipset)

X00



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Friday, December 30, 2011 | Sheet 23 of 104

SSID = PCH

POWER

PCH1J

10 OF 10

PANTHER-GP-NF

71.PANTH.00U

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccClkDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.05
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to PCH EDS V1.5 (General DC Characteristicschipset)

VCCSUSHDA need to be at either 3.3V or 1.5V.
All the Core Voltages need to be at the same level either 3.3 V or 1.5 V.

<Variant Name>

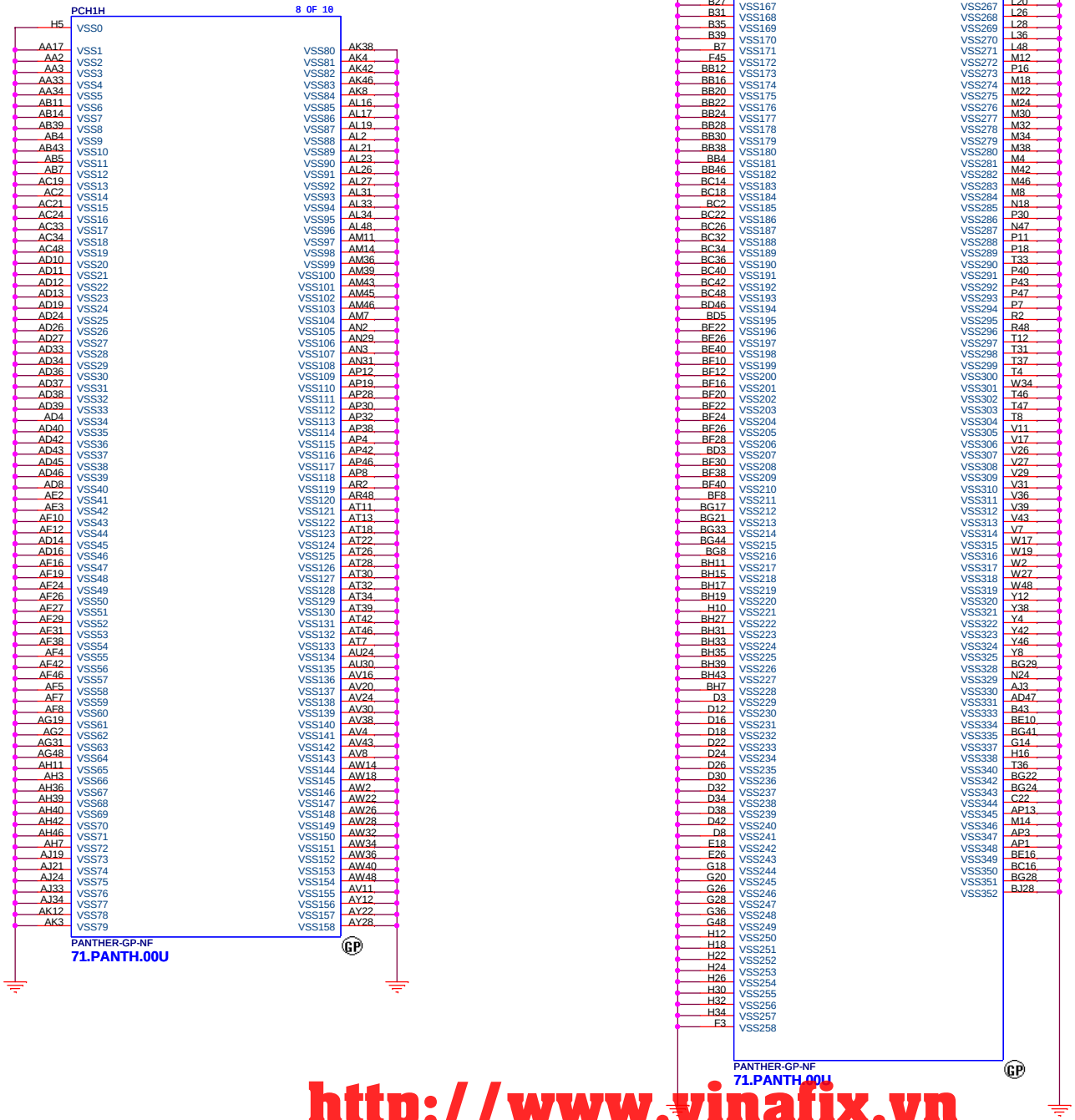
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER2)

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Friday, December 30, 2011 | Sheet 24 of 104

SSID = PCH



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Friday, December 30, 2011 | Sheet 25 of 104

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

Date: Friday, December 30, 2011 Sheet 26 of 104

SSID = KBC

PCB VER AD(GPIO91)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DV14_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
DV14_DIS	100.0K	20.0K(64.20025.6DL)	2.75V
DV15_UMA with HDMI	100.0K	33.0K(64.33025.6DL)	2.48V
DV15_UMA without HDMI	100.0K	47.0K(64.47025.6DL)	2.24V
TBD	100.0K	64.9K(64.64925.6DL)	2.0V
TBD	100.0K	76.8K(64.76825.6DL)	1.87V
TBD	100.0K	100.0K(64.10035.6DL)	1.65V
TBD	100.0K	143.0K(64.14335.6DL)	1.358V
TBD	100.0K	174.0K(64.17435.6DL)	1.204V
TBD	100.0K	215.0K(64.21535.6DL)	1.048V

Layout Note:
Need very close to EC

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

20100712 V1.5

C502 : check list 1.5

Power Switch Logic(PSL)

SPI Shared Flash ROM

KBC CLK EMI

EC GPIO standard PH/PL

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795

Size	Document Number	Rev
A2	Enrico Caruso 14 MLK DIS	X02

Date: Tuesday, January 03, 2012 Sheet 27 of 104

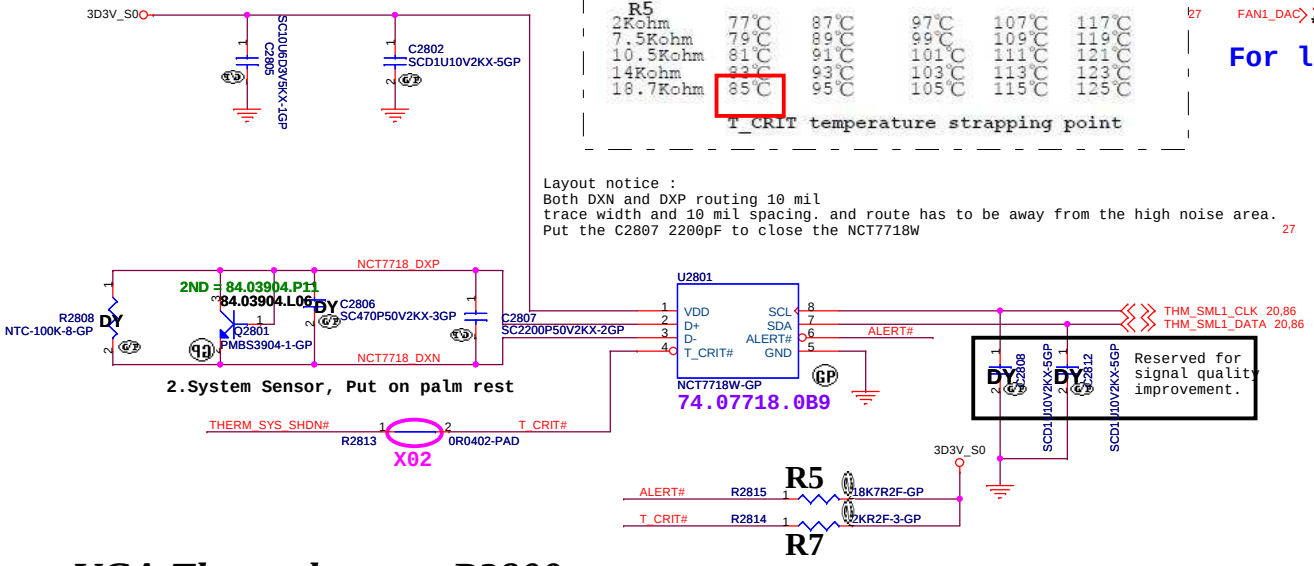
SSID = Thermal

Thermal sensor NCT7718W

ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

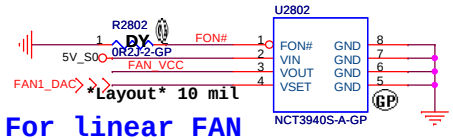
T_CRIT temperature strapping point



Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing. and route has to be away from the high noise area.
Put the C2807 2200pF to close the NCT7718W

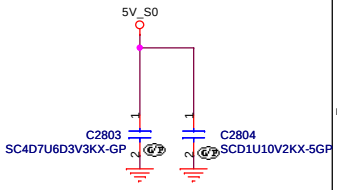
2.System Sensor, Put on palm rest

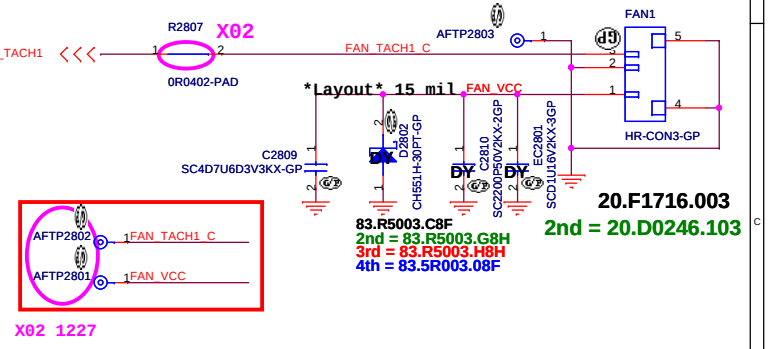
Fan controller G991



For linear FAN

74.03940.A71
2nd = 74.02793.A31
3rd = 74.00991.031



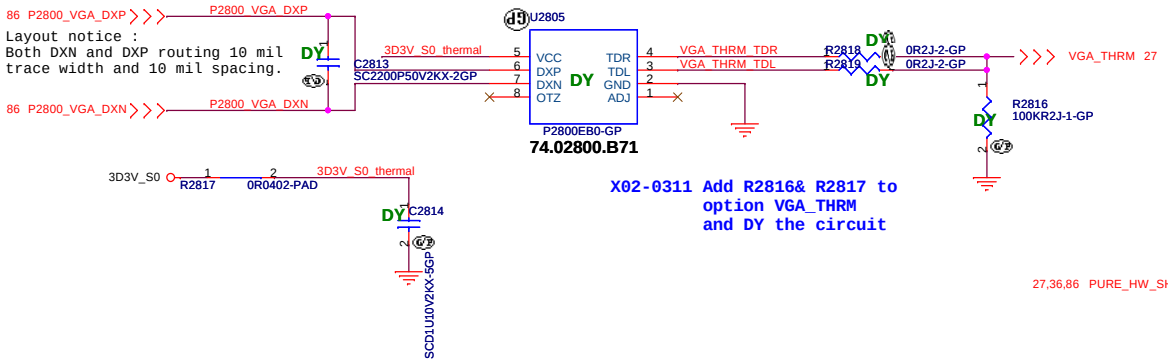


20.F1716.003
2nd = 20.D0246.103

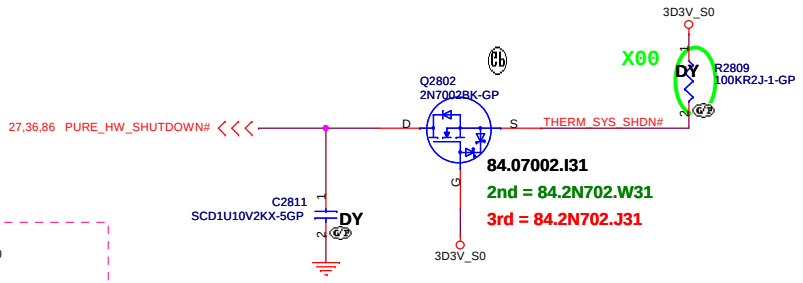
83.R5003.C8F
2nd = 83.R5003.G8H
3rd = 83.R5003.H8H
4th = 83.5R003.08F

X02 1227

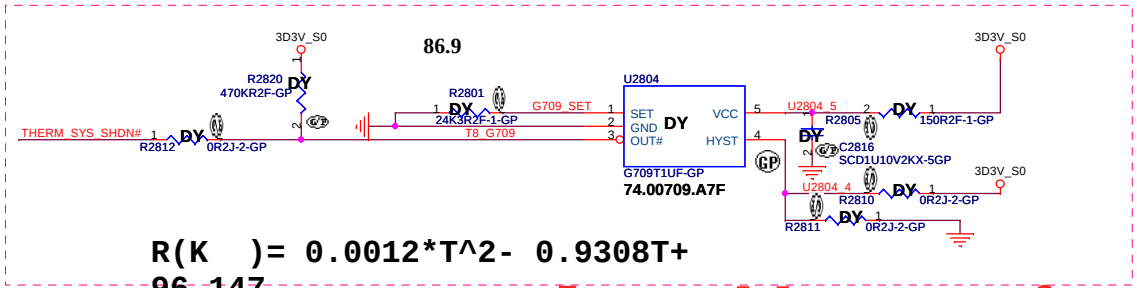
VGA Thermal sensor P2800



X02-0311 Add R2816& R2817 to option VGA_THRM and DY the circuit



84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31



R(K)= 0.0012*T^2- 0.9308T+ 96.147

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793
Size: A3
Document Number: Enrico Caruso 14 MLK DIS
Rev: X02
Date: Tuesday, January 03, 2012
Sheet 28 of 104

SSID = AUDIO

X01 1111

From PCH

From EC

AUD_PC_BEEP X02 1230
Trace width>15 mils

83.00054.Q81
2nd = 83.R2003.E81
3rd = 83.00054.X81
4th = 83.BAT54.081

U2901
CS4213D-CNZR-GP
71.04213.003

Depop sound

83.00016.K11
2nd = 83.00016.F11

84.T3906.A11
2nd = 84.03906.F11

84.03904.L06
2ND = 84.03904.P11

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec CS4213D

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Tuesday, January 03, 2012 | Sheet 29 of 104

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

Date: Friday, December 30, 2011 Sheet 30 of 104

LAN CHIP

X02-20110414

60 mils

68.4R750.20C
2nd = 68.4R71G.10G
3rd = 68.4R71E.10R

40 mils

84.03904.L06
2nd = 84.03904.P11

84.02130.031
2nd = 84.00102.031
3rd = 84.03413.A31

84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31

RTL8105E-VD : 71.08105.B03
RTL8111F : 71.08111.N03

For Switch Regulator enable

R3116
RTL8111E-Stuff
RTL8105E-DY

X01 1116

82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61

<Variant Name>

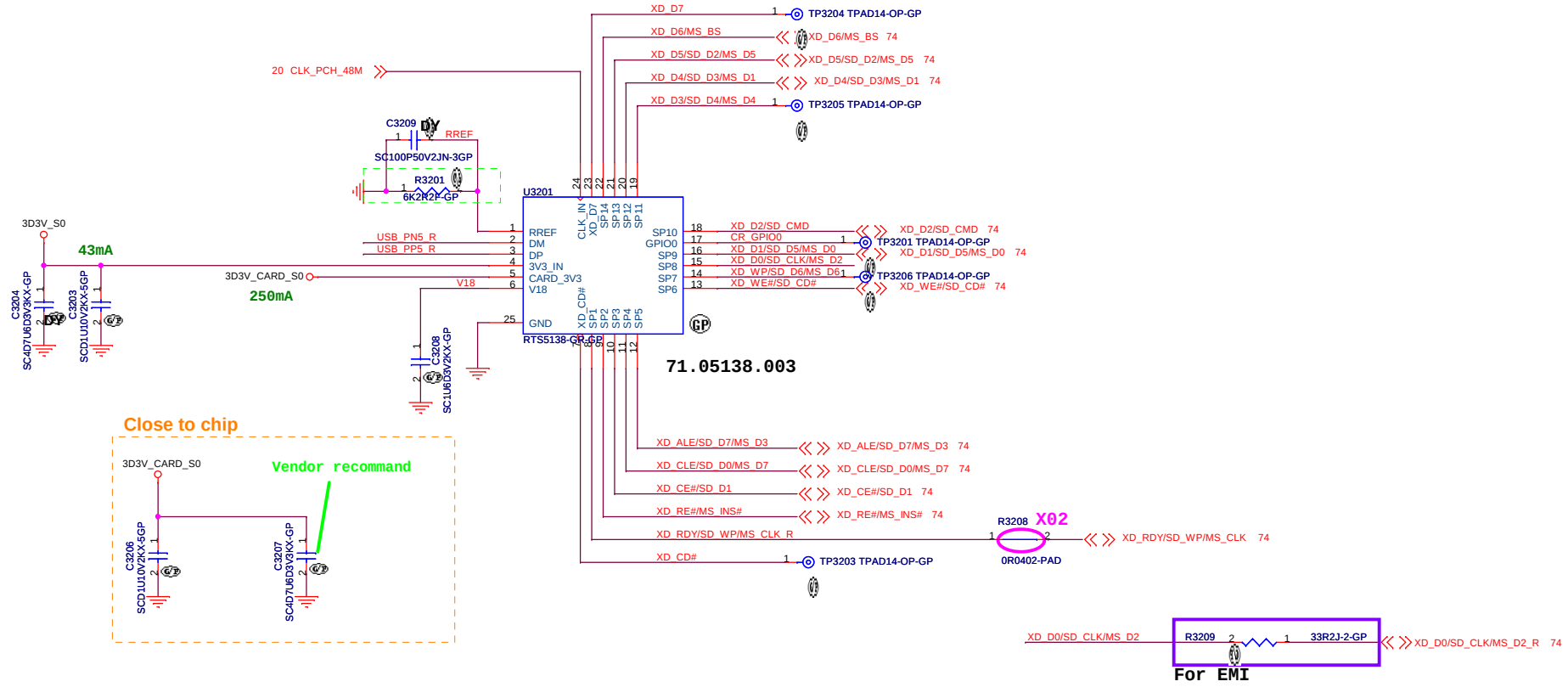
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LOM

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Tuesday, January 03, 2012 | Sheet 31 of 104

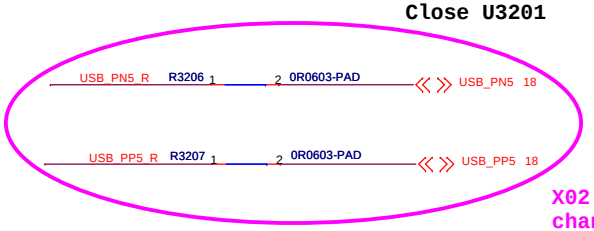
SSID = SDIO



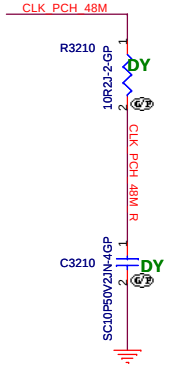
Close to chip

For EMI

Close U3201



X02 1229
changed R3206,R3207 to short pad,
removed TR3201 CMC footprint



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Card Reader-RTS5138	
Size A3	Document Number: Enrico Caruso 14 MLK DIS	Rev X02
Date: Tuesday, January 03, 2012	Sheet 32 of 104	

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico Caruso 14 MLK DIS*	*X02*

Date: Friday, December 30, 2011 Sheet 33 of 104

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico Caruso 14 MLK DIS*	*X02*

Date: Friday, December 30, 2011 Sheet 34 of 104

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

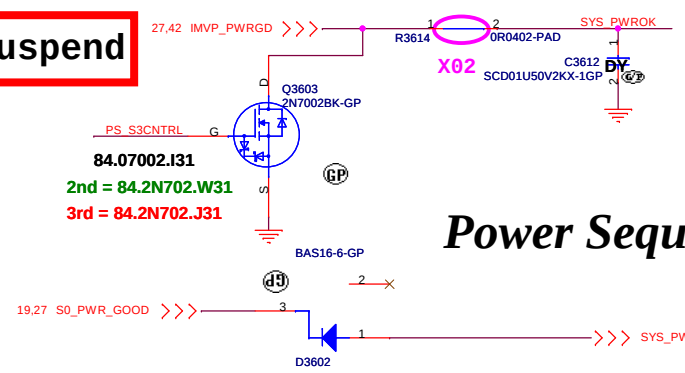
Title: *Reserved*

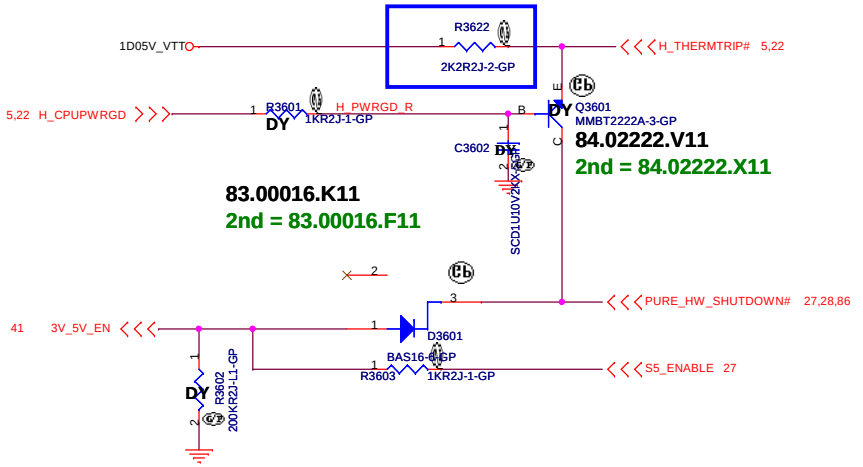
Size	Document Number	Rev
A3	*Enrico Caruso 14 MLK DIS*	*X02*

Date: Friday, December 30, 2011 Sheet 35 of 104

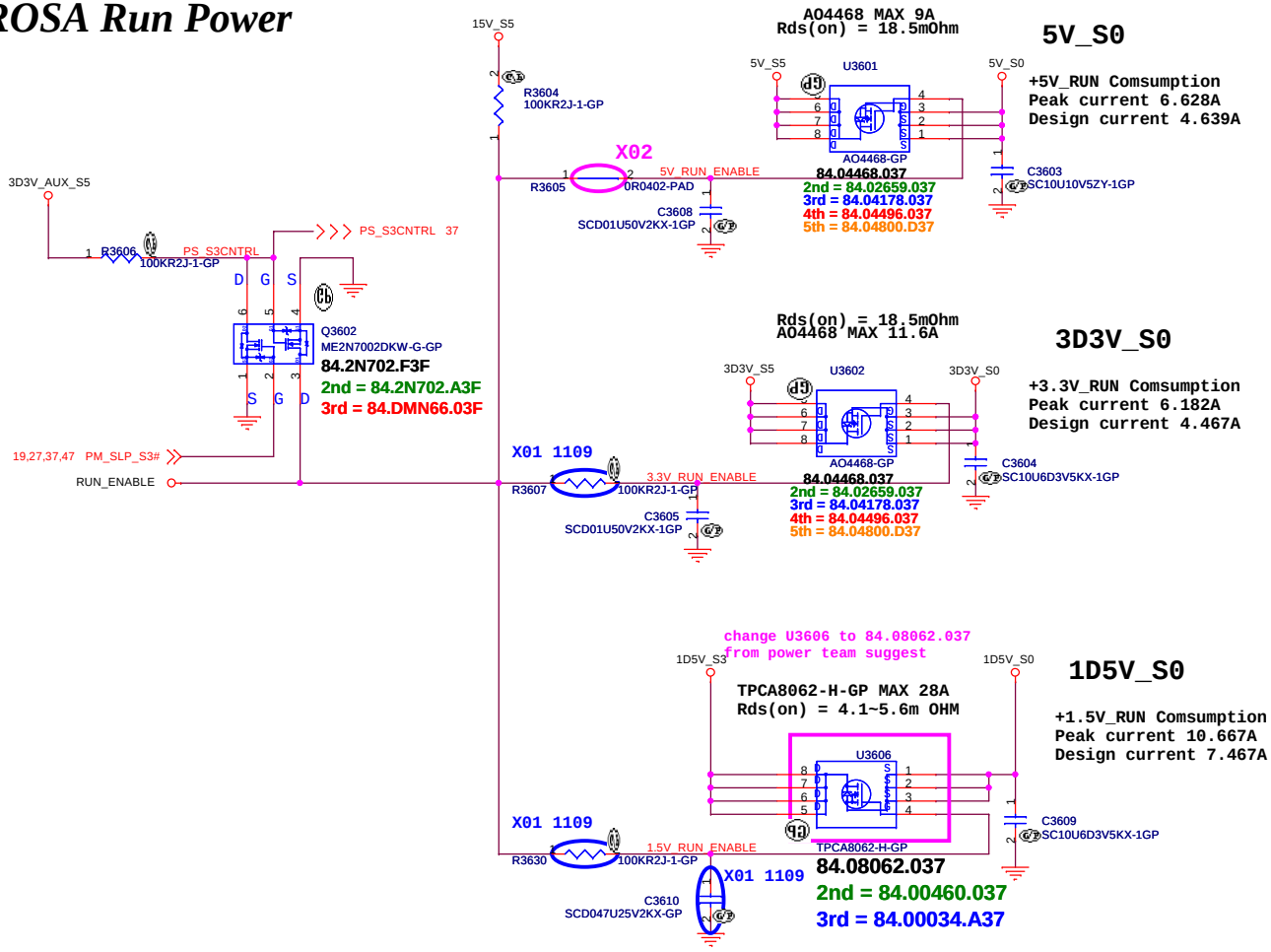
SSID = Reset.Suspend

Power Sequence





ROSA Run Power



<Variant Name>

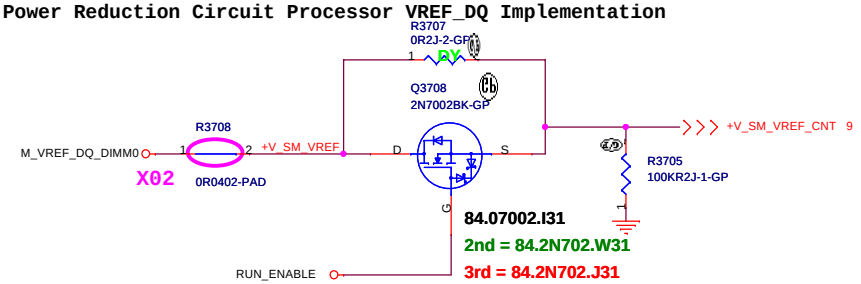
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

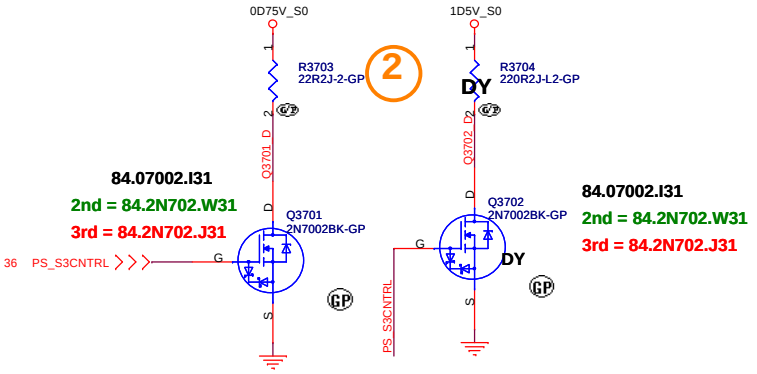
Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

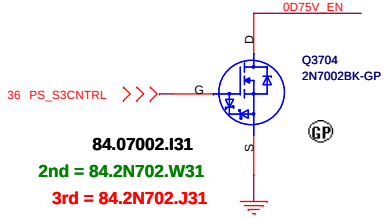
Date: Tuesday, January 03, 2012 Sheet 36 of 104

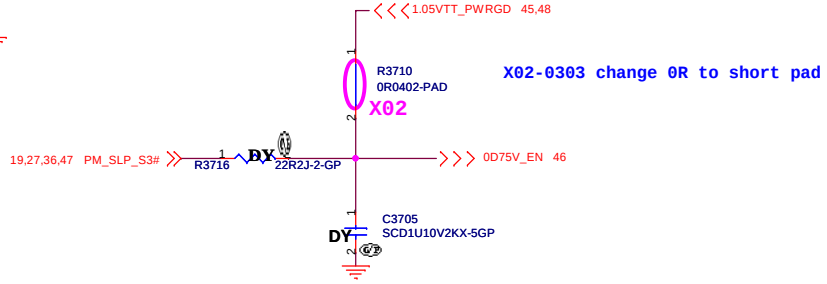
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



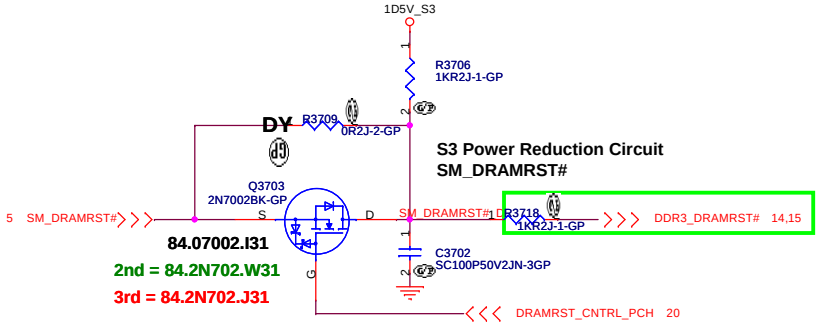
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

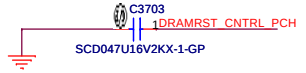




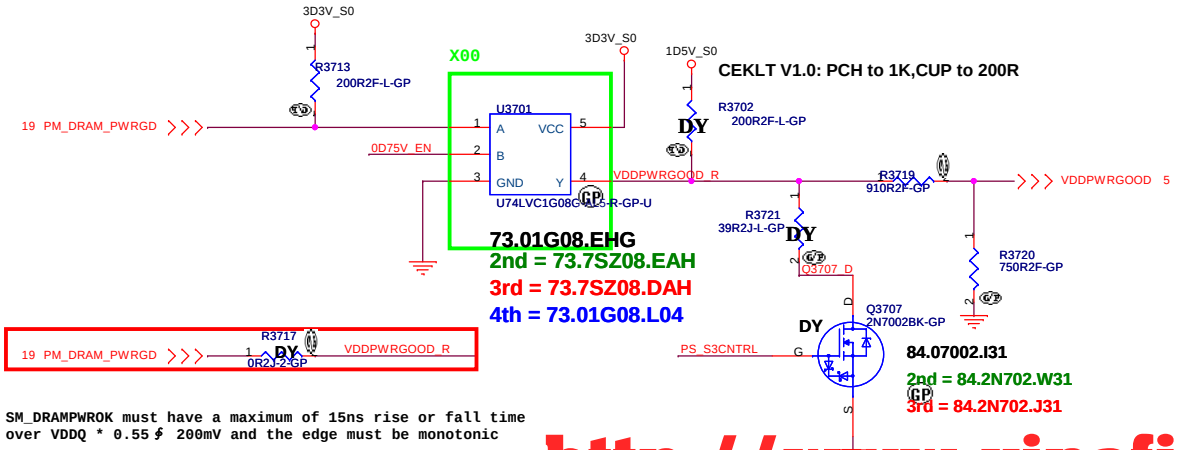


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK





Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55 ≯ 200mV and the edge must be monotonic

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

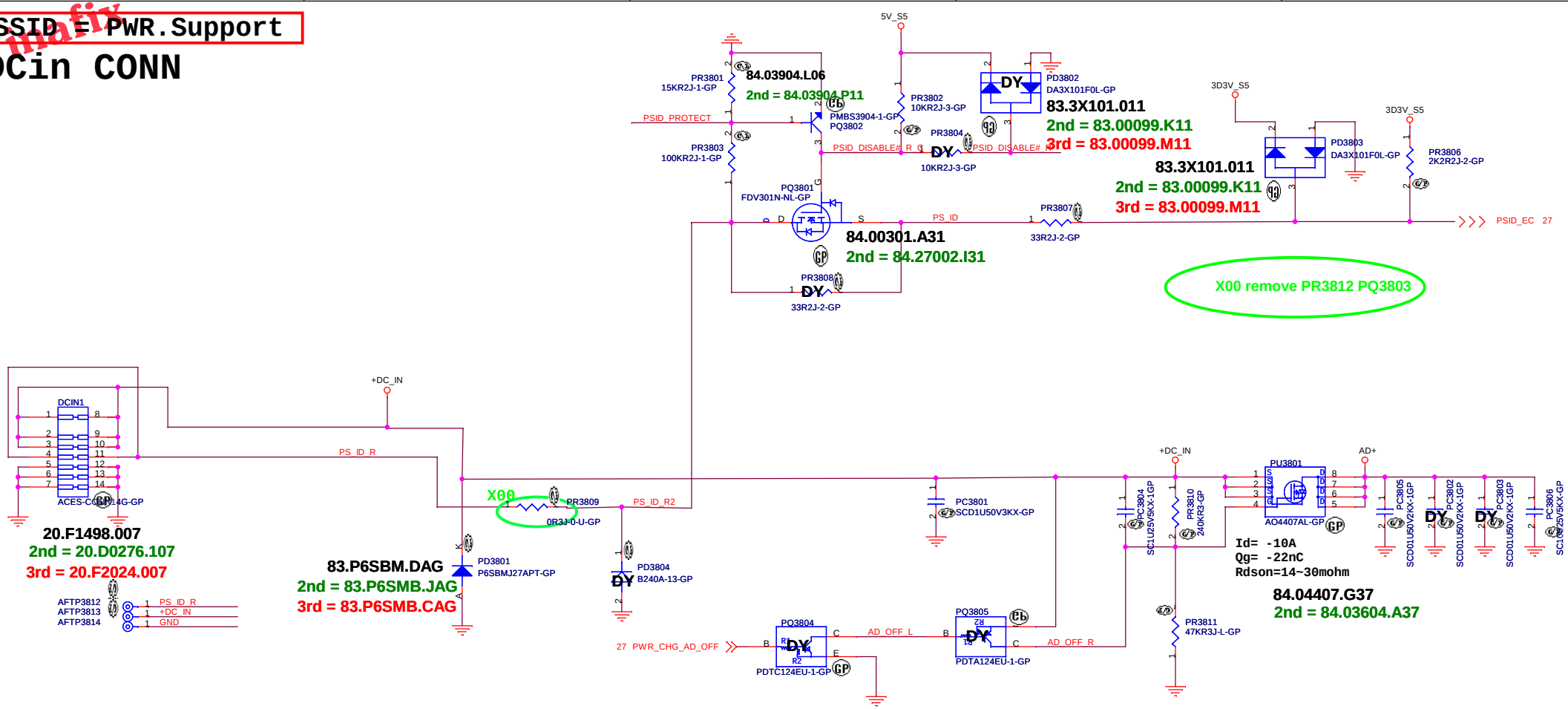
Title: S3 Reduction Circuit

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Tuesday, January 03, 2012 | Sheet 37 of 104

SSID = PWR.Support

DCin CONN



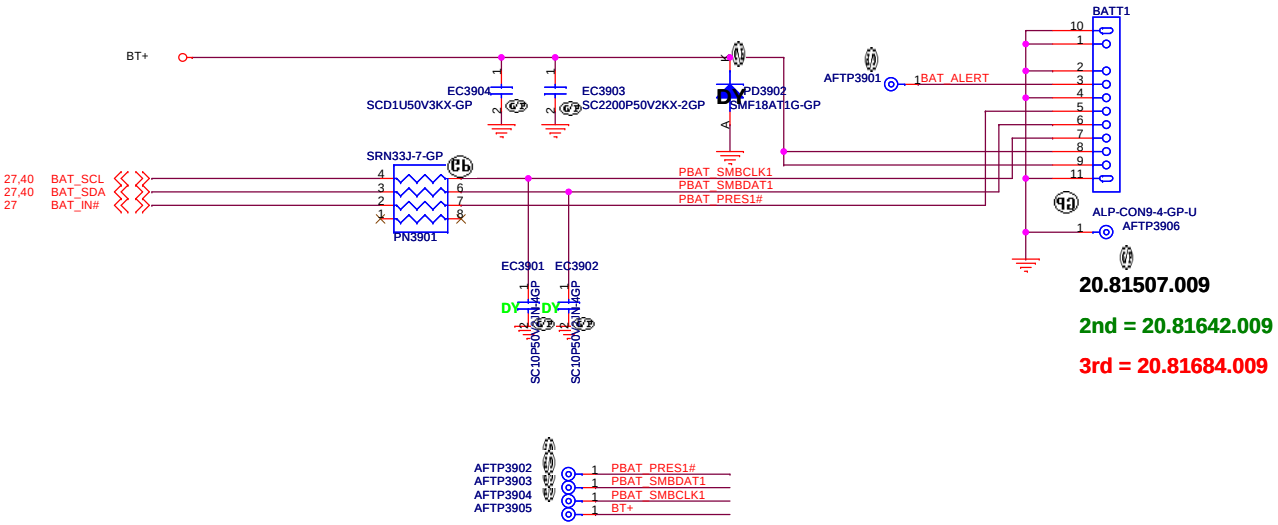
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DCIN Jack	
Size: A3	Document Number: Enrico Caruso 14 MLK DIS	Rev: X01
Date: Tuesday, January 03, 2012	Sheet 38 of 104	

SSID = PWR.Support

Batt Connecter



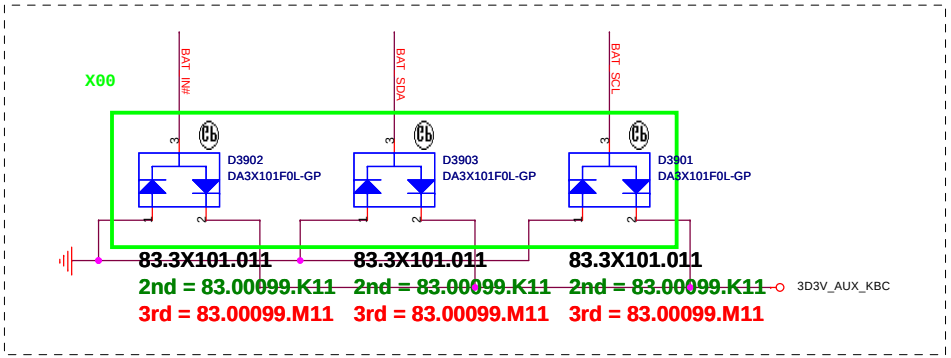
20.81507.009

2nd = 20.81642.009

3rd = 20.81684.009

For actual location, need to be swap all pin

Placement: Close to Batt Connector



83.3X101.011 83.3X101.011 83.3X101.011

2nd = 83.00099.K11 2nd = 83.00099.K11 2nd = 83.00099.K11

3rd = 83.00099.M11 3rd = 83.00099.M11 3rd = 83.00099.M11

<Variant Name>

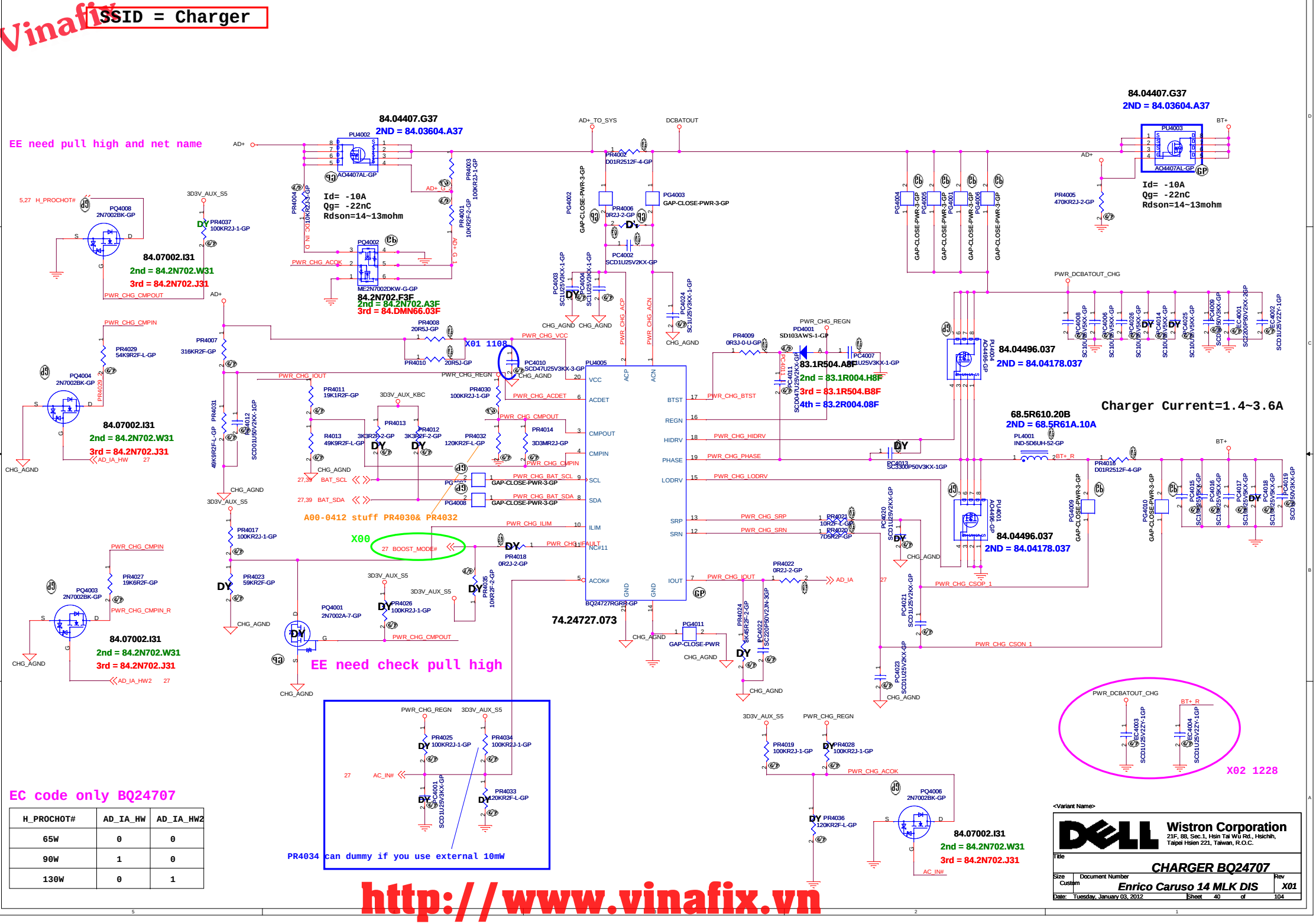
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X01

Date: Tuesday, January 03, 2012 | Sheet 39 of 104

SSID = Charger



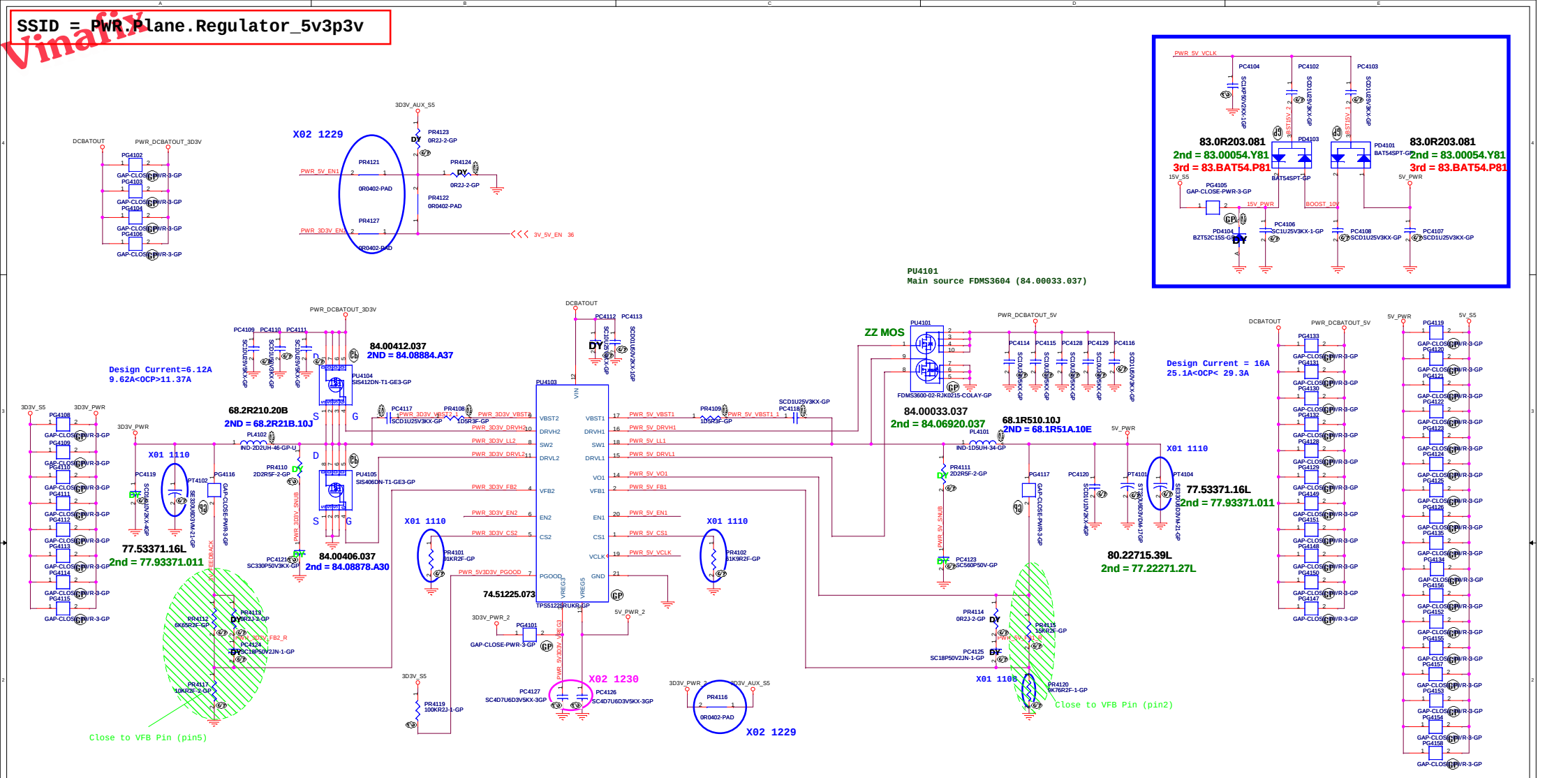
H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24707
Size: Custom | Document Number: Enrico Caruso 14 MLK DIS | Rev: X01
Date: Tuesday, January 03, 2012 | Sheet 40 of 104

SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/78.10622.51L
Inductor: 2.2U PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP POL 330U6.3V M6.3*5.7 15mOhm / 77.53371.04L
H/S: SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S: SI7716ADN-T1-GE3 / 13.5mOhm/16.5mOhm@4.5Vgs / 84.07716.037

I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.50UH PCMC104T-1R5 Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 220U 6.3V PSLV0J227M 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: CHIP CAP POL 330U6.3V M6.3*5.7 15mOhm / 77.53371.04L
H/S,L/S: FDMS3604S / 7.5mohm/9.8mOhm@4.5Vgs, 2.6mohm/3.2mOhm@4.5Vgs/ 84.03604.037

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3V/5V TPS51225

Size	Document Number	Rev
A2	Enrico Caruso 14 MLK DIS	X01

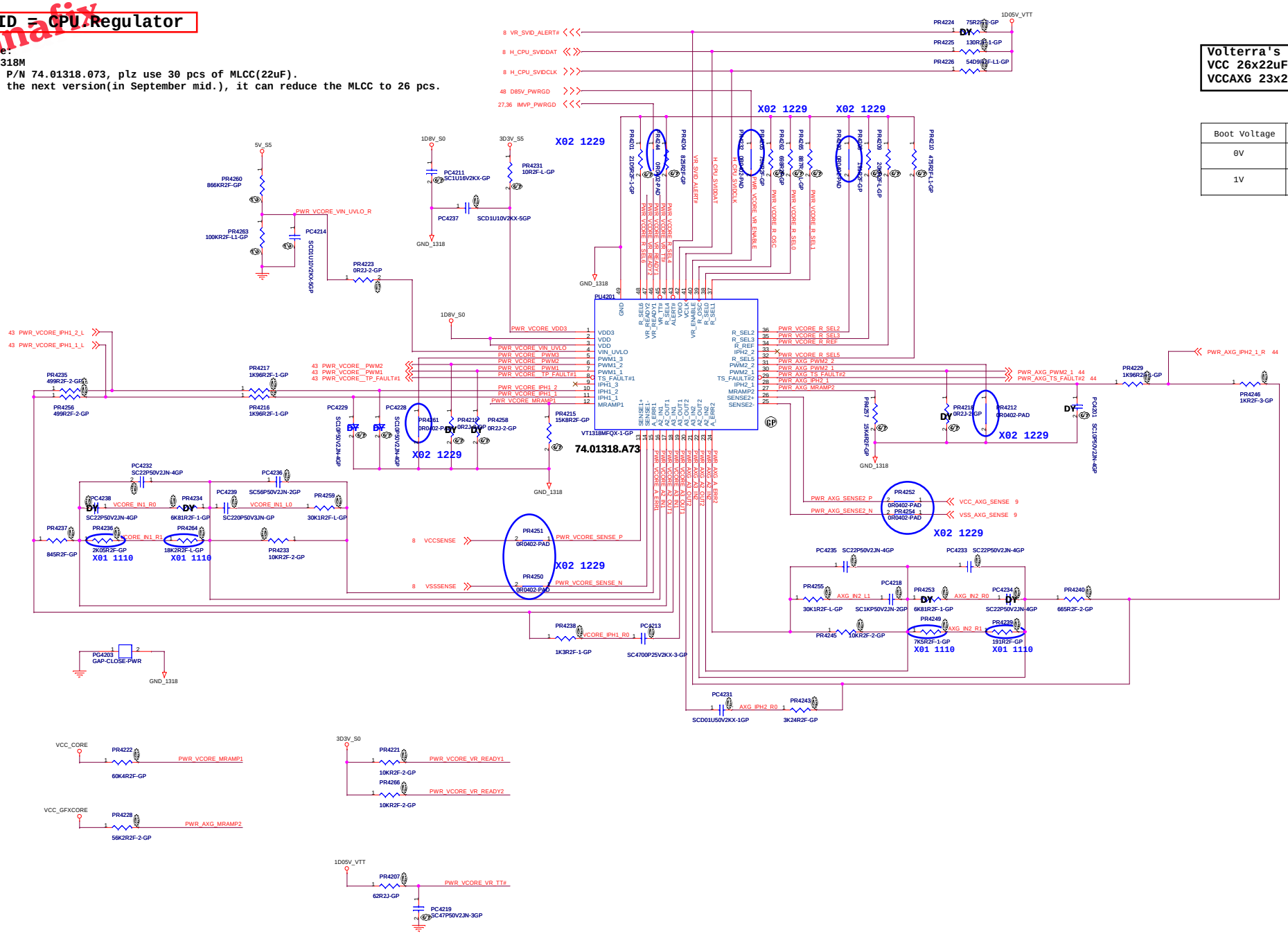
Date: Tuesday, January 03, 2012 Sheet 41 of 104

SSID = CPU.Regulator

Note:
VT1318M
For P/N 74.01318.073, plz use 30 pcs of MLCC(22uF).
For the next version(in September mid.), it can reduce the MLCC to 26 pcs.

Volterra's suggestion:
VCC 26x22uF for 2-PHASE VCC
VCCAXG 23x22uF for 1-PHASE VCCAXG

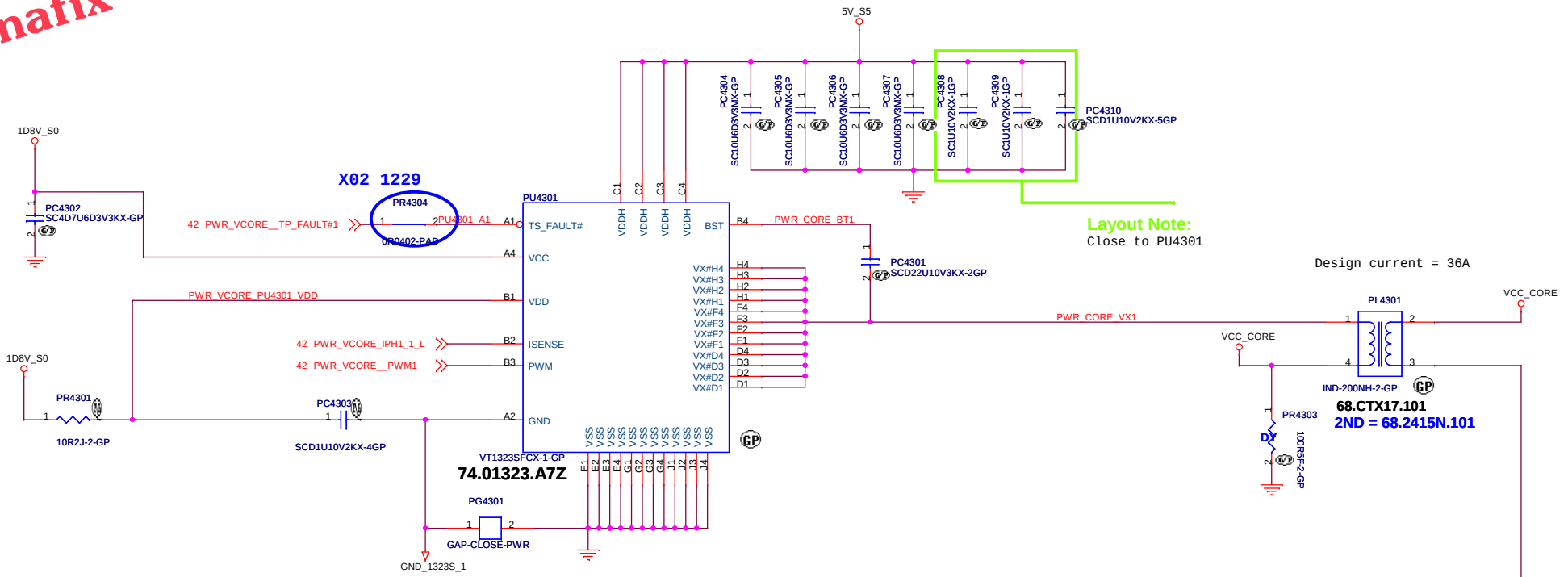
Boot Voltage	PR4265	PR4204
0V	887ohm	825ohm
1V	215ohm	191ohm

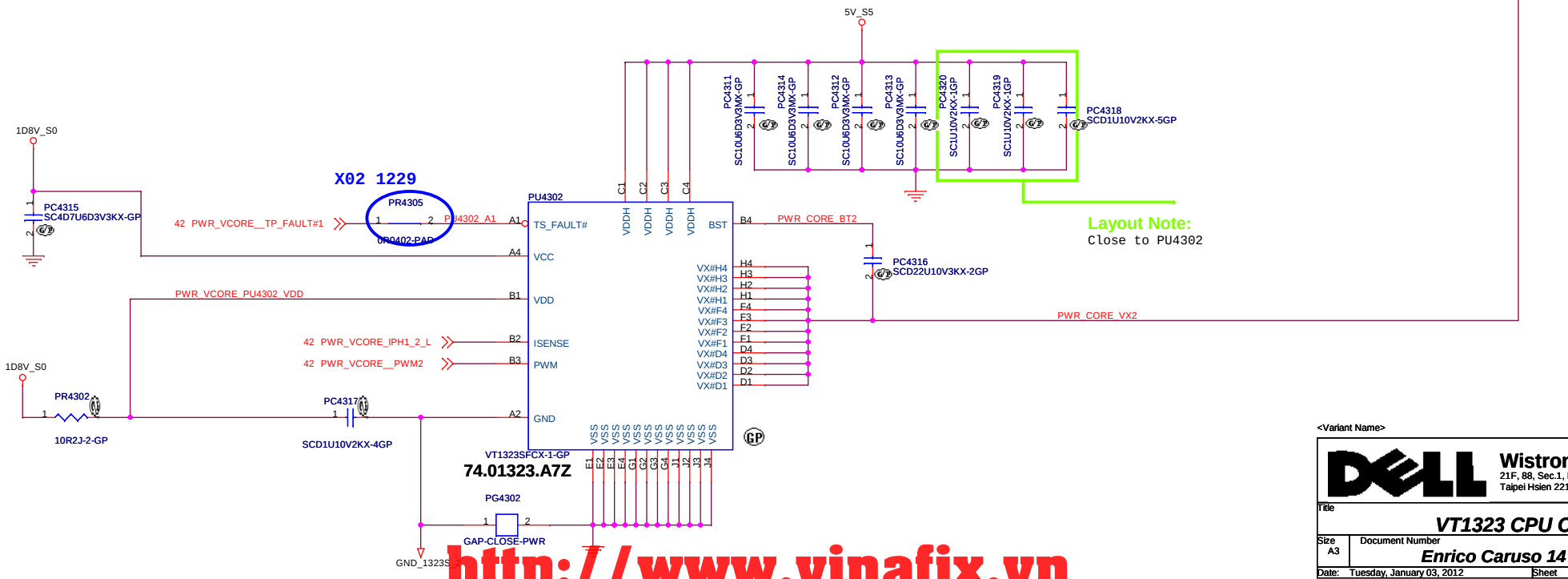


<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1318 CPU CORE(1/3)
Size: A2 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X01
Date: Tuesday, January 03, 2012 | Sheet 42 of 104





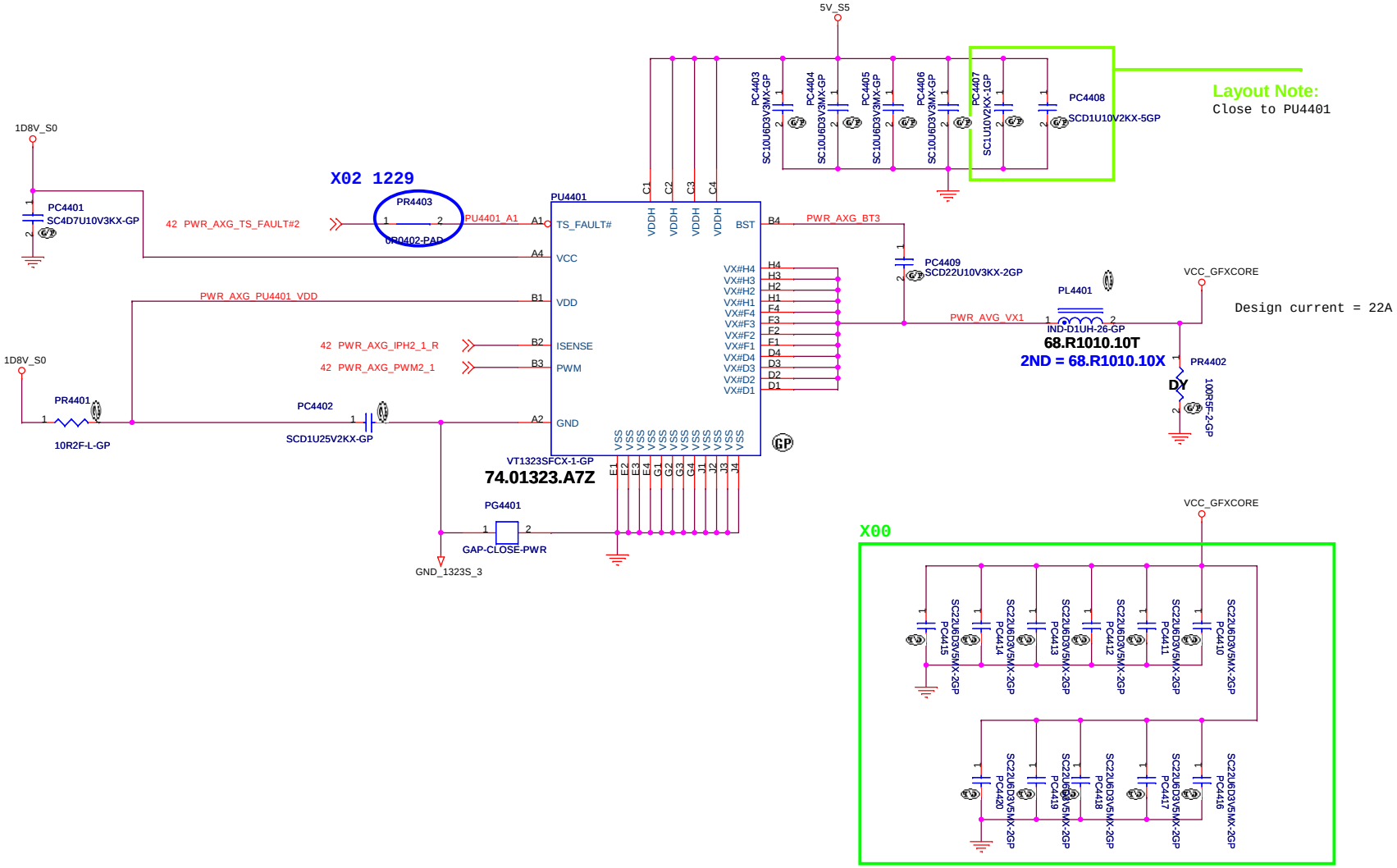
<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1323 CPU CORE(2/3)

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X01

Date: Tuesday, January 03, 2012 | Sheet 43 of 104



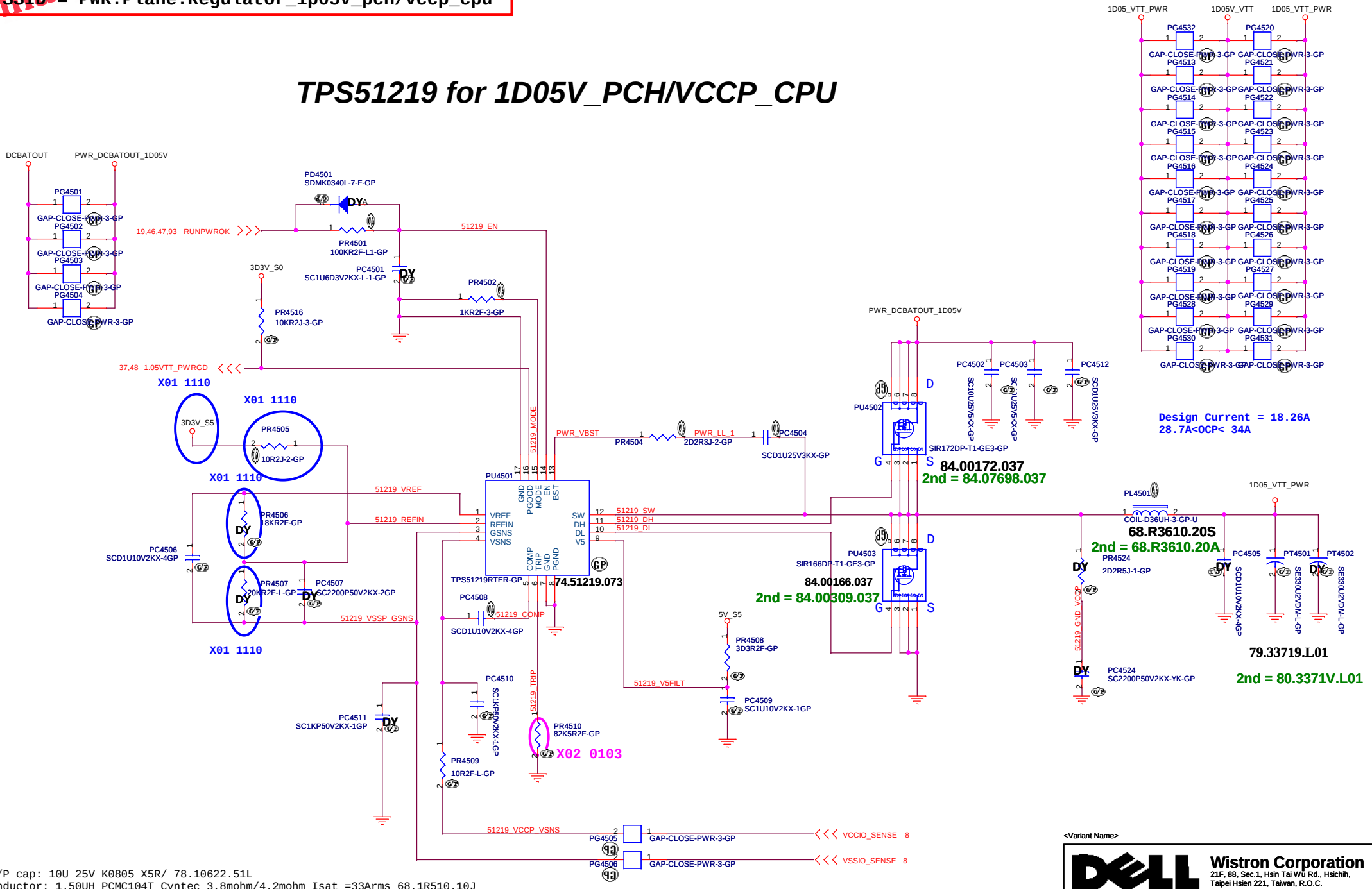
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VT1323 CPU CORE(3/3)	
Size A3	Document Number: Enrico Caruso 14 MLK DIS	Rev X01
Date: Tuesday, January 03, 2012	Sheet 44 of 104	

SSID = PWR.Plane.Regulator_1p05v_pch/vccp_cpu

TPS51219 for 1D05V_PCH/VCCP_CPU



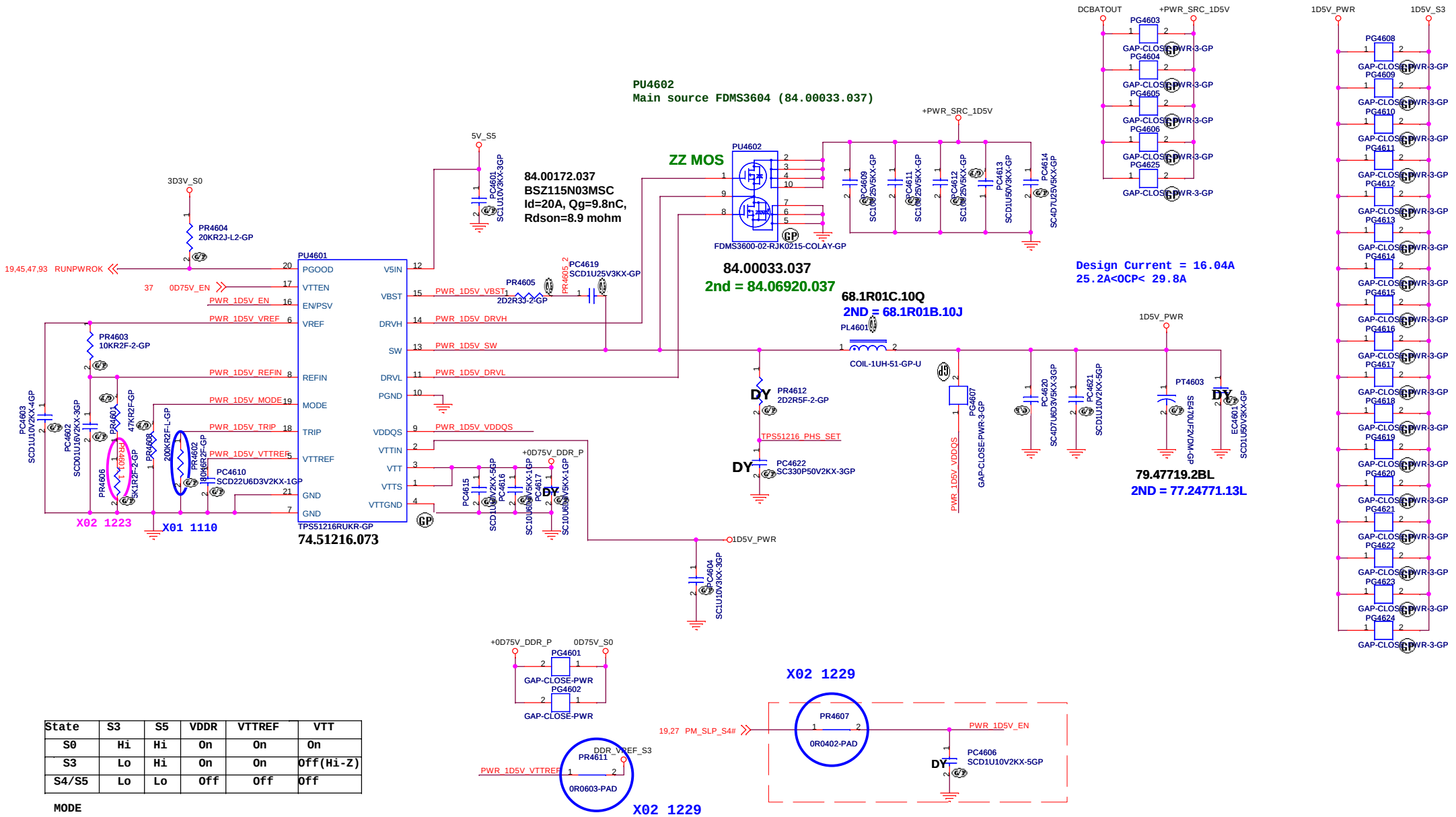
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.50UH PCMC104T Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
H/S: SIR172DP / 10.3mohm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SiR166DP / 0.32mohm/0.4mOhm@4.5Vgs/ 84.00166.037

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51219 1D05V_PCH/VCCP_CPU
Size: A3
Document Number: Enrico Caruso 14 MLK DIS
Rev: X01
Date: Tuesday, January 03, 2012
Sheet 45 of 104

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 1.0UH PCMB104T-1R0M Cyntec 3mohm/3.3mohm Isat =28Arms68.1R01C.10Q
O/P cap: CHIP CAP 470UF 2V EEFSX0D471X 6mOhm 3.5Arm/Panasonic/79.47719.2BL
H/S,L/S: FDMS3604S / 7.5mohm/9.8mOhm@4.5Vgs, 2.6mohm/3.2mOhm@4.5Vgs/ 84.03604.037

<Variant Name>

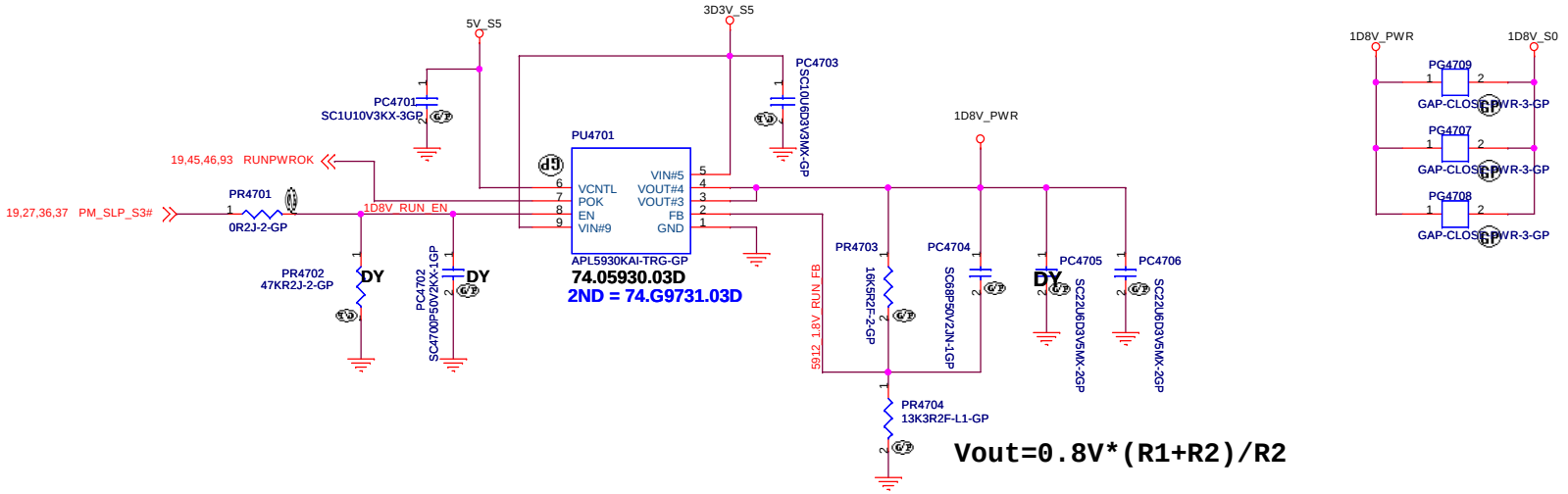
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51216_+1.5V_SUS
Size: A3
Document Number: Enrico Caruso 14 MLK DIS
Rev: X01
Date: Tuesday, January 03, 2012
Sheet 46 of 104

SSID = PWR.Plane.Regulator_1p8v

APL5930 for 1D8V_S0

+1.8V_RUN
Design current = 1.086A

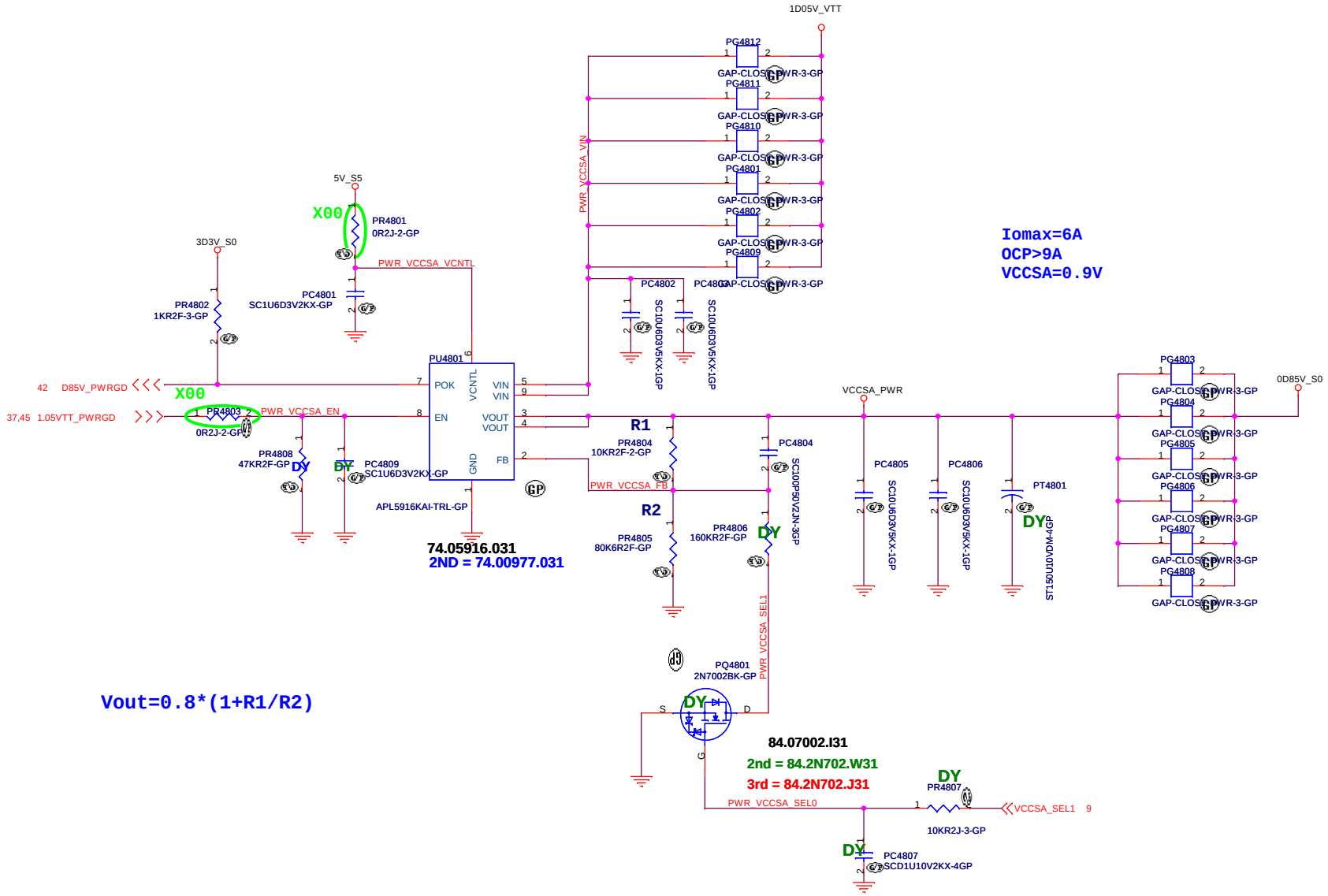


<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5930 1D8V_S0		
Size: A3	Document Number: Enrico Caruso 14 MLK DIS	Rev: X01
Date: Tuesday, January 03, 2012	Sheet 47 of 104	

APL5916 for VCCSA



<Variant Name>

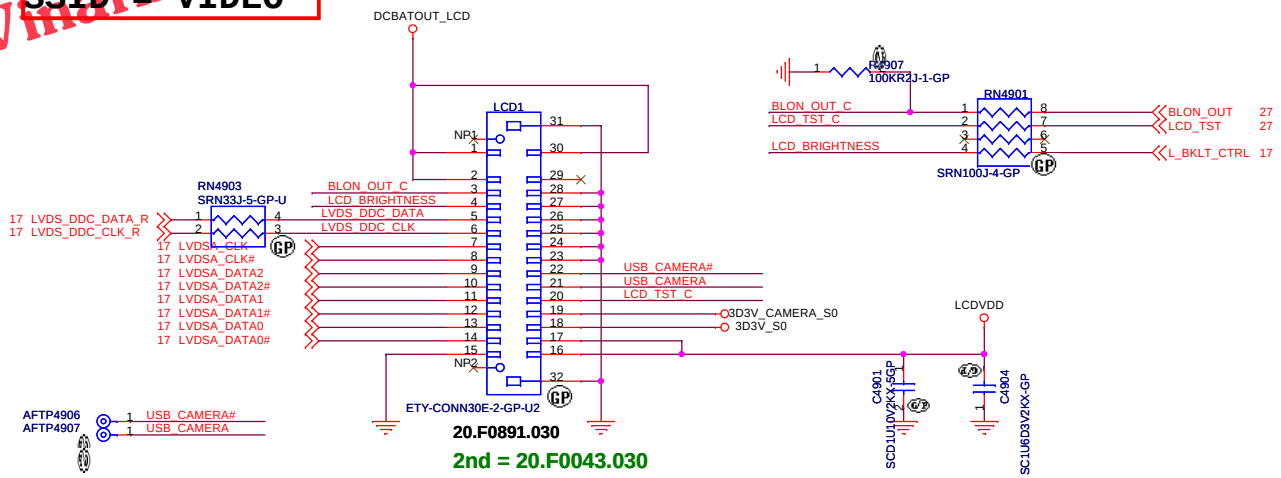
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

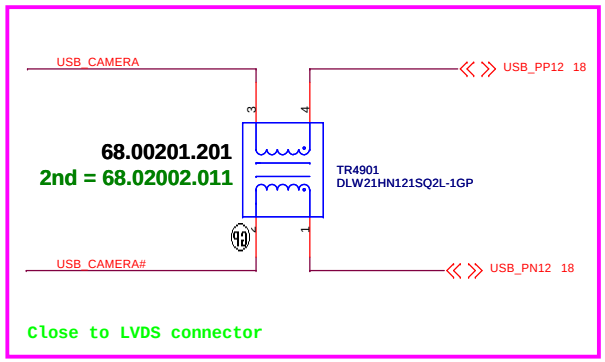
Title: APL5916_VCCSA

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X01

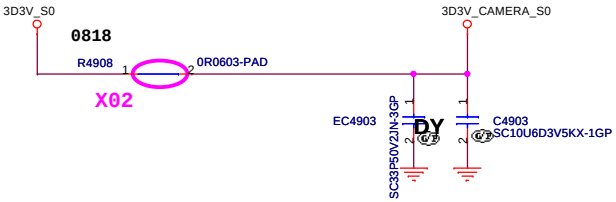
Date: Tuesday, January 03, 2012 | Sheet 48 of 104

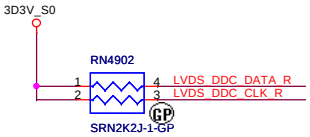
SSID = VIDEO



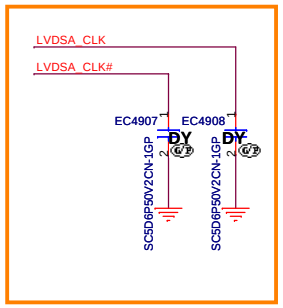


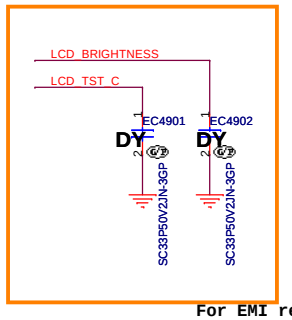
X02 0103
remove R4903,R4904 co-lay position





Close to LVDS connector

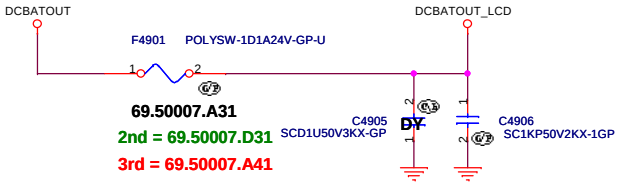


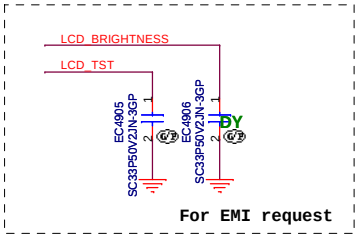


For EMI request

SSID = Inverter

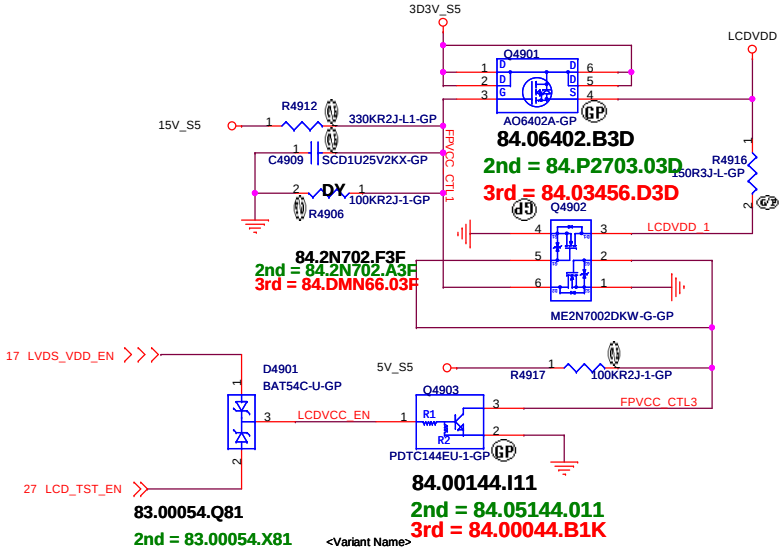
INVERTER POWER





SSID = VIDEO

LCD POWER

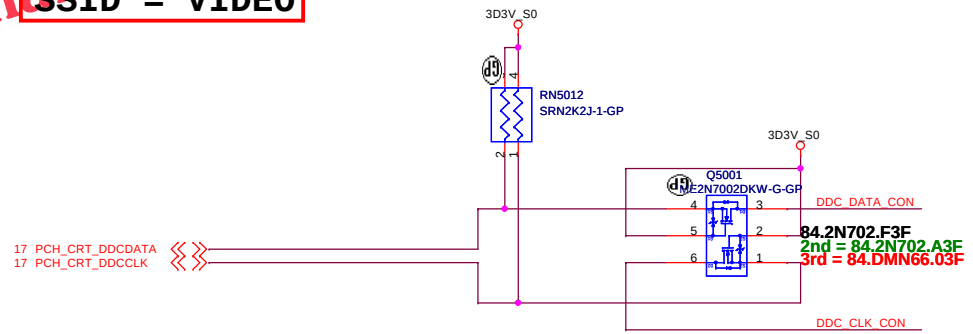


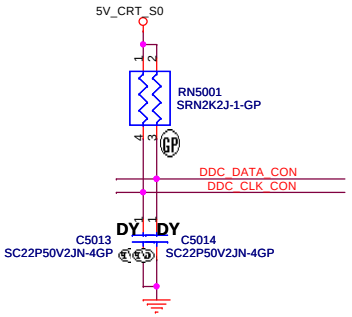
<Variant Name>

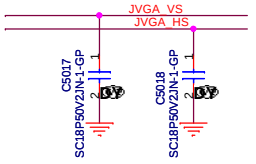
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

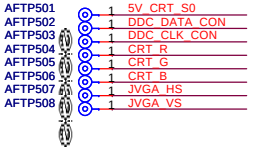
Title: LCD Connector
Size: A3
Document Number: Enrico Caruso 14 MLK DIS
Rev: X02
Date: Tuesday, January 03, 2012
Sheet 49 of 104

SSID = VIDEO

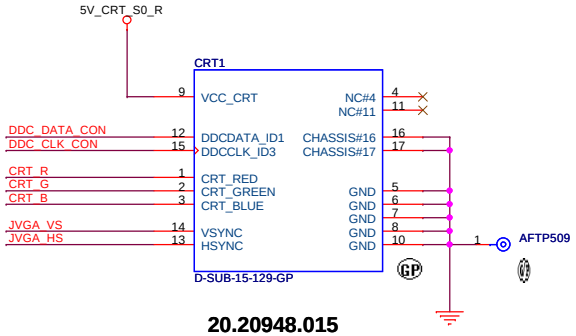








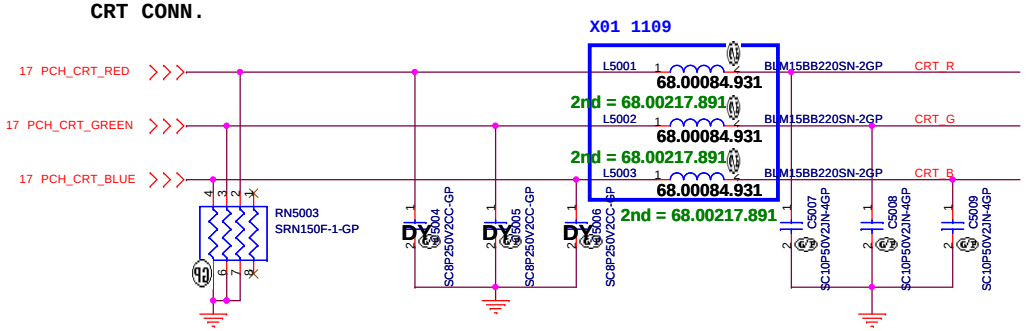
11/29 change CRT1 to 20.20927.015

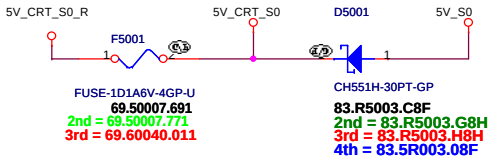


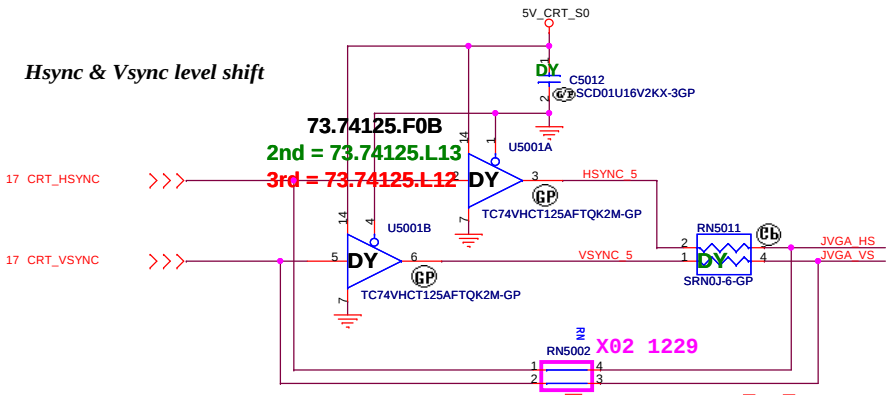
20.20948.015
2nd = 20.20945.015

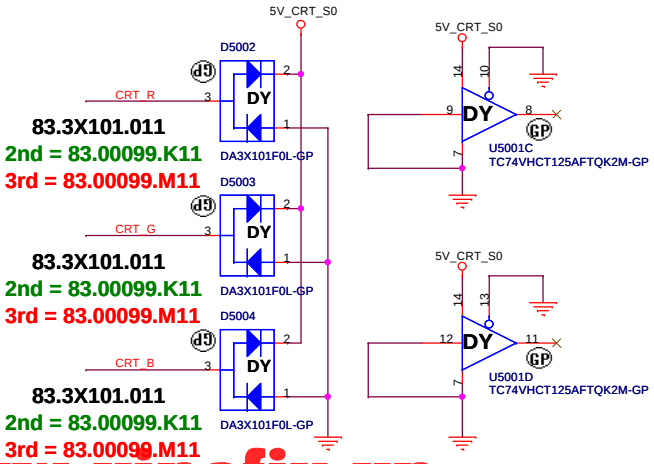
Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.









CLOSE TO TRANSFORMER

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

Date: Tuesday, January 03, 2012 Sheet 50 of 104

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN

X02 1229

HDMI_CLK_R_C 1 R5101 2 HDMI_CLK_R_C_CON
0R0402-PAD

HDMI_DATA1_R_C 1 R5106 2 HDMI_DATA1_R_C_CON
0R0402-PAD

HDMI_CLK_R_C# 1 R5102 2 HDMI_CLK_R_C#_CON
0R0402-PAD

changed R5101,R5102 to short pad,
removed TR5101 CMC footprint

HDMI_DATA1_R_C# 1 R5105 2 HDMI_DATA1_R_C#_CON
0R0402-PAD

changed R5105,R5106 to short pad,
removed TR5103 CMC footprint

HDMI_DATA0_R_C 1 R5104 2 HDMI_DATA0_R_C_CON
0R0402-PAD

HDMI_DATA2_R_C 1 R5108 2 HDMI_DATA2_R_C_CON
0R0402-PAD

HDMI_DATA0_R_C# 1 R5103 2 HDMI_DATA0_R_C#_CON
0R0402-PAD

changed R5103,R5104 to short pad,
removed TR5102 CMC footprint

HDMI_DATA2_R_C# 1 R5107 2 HDMI_DATA2_R_C#_CON
0R0402-PAD

changed R5107,R5108 to short pad,
removed TR5104 CMC footprint

HDMI_PLL_GND

Q5103
2N7002BK-GP

R5123
0R2J-2-GP

5V_S0

R5113
100KR2J-1-GP

84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31

HDMI1
SKT-HDMI19P-63-GP-U

HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
DDC_CLK_HDMI
DDC_DATA_HDMI

5V_CRT_S0_R

C5102
SCD1U10V2KX-5GP

22.10296.171
2nd = 22.10296.581
3rd = 22.10296.451

HPD_HDMI_CON

3D3V_S0

Q5102
PMBS3904-1-GP
84.03904.L06
2ND = 84.03904.P11

R5111
150KR2J-L1-GP
HDMI_HPD_B

R5110
200KR2J-L1-GP
DY

HDMI_HPD_E

R5125
0R0402-PAD
X02

HDMI_PCH_DET 17

R5112
10KR2J-3-GP

17 HDMI_CLK_R#
17 HDMI_CLK_R
C5103
C5104
SCD1U10V2KX-5GP
HDMI_CLK_R_C#
HDMI_CLK_R_C

17 HDMI_DATA0_R#
17 HDMI_DATA0_R
C5105
C5106
SCD1U10V2KX-5GP
HDMI_DATA0_R_C#
HDMI_DATA0_R_C

17 HDMI_DATA1_R#
17 HDMI_DATA1_R
C5110
C5107
SCD1U10V2KX-5GP
HDMI_DATA1_R_C#
HDMI_DATA1_R_C

17 HDMI_DATA2_R#
17 HDMI_DATA2_R
C5108
C5109
SCD1U10V2KX-5GP
HDMI_DATA2_R_C#
HDMI_DATA2_R_C

RN5106
SRN680J-GP

RN5107
SRN680J-GP

HDMI_PLL_GND

5V_CRT_S0_R

3D3V_S0

RN5101
SRN2K2J-1-GP

Q5104
NE2N7002DKW-G-GP

DDC_CLK_HDMI

17 PCH_HDMI_CLK
17 PCH_HDMI_DATA

84.2N702.F3F
2nd = 84.2N702.A3F
3rd = 84.DMN66.03F

DDC_DATA_HDMI

Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector
Size: A3
Document Number: Enrico Caruso 14 MLK DIS
Rev: X02
Date: Tuesday, January 03, 2012
Sheet 51 of 104

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico Caruso 14 MLK DIS*	*X02*

Date: Friday, December 30, 2011 Sheet 52 of 104

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS Switch

Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

Date: Friday, December 30, 2011 Sheet 53 of 104

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico Caruso 14 MLK DIS*	*X02*

Date: Friday, December 30, 2011 Sheet 54 of 104

SSID = User.Interface

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

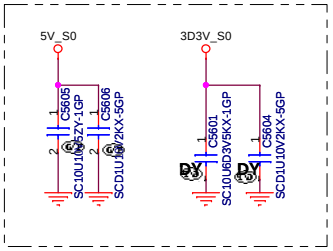
Title: ITP/Fan Connector

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

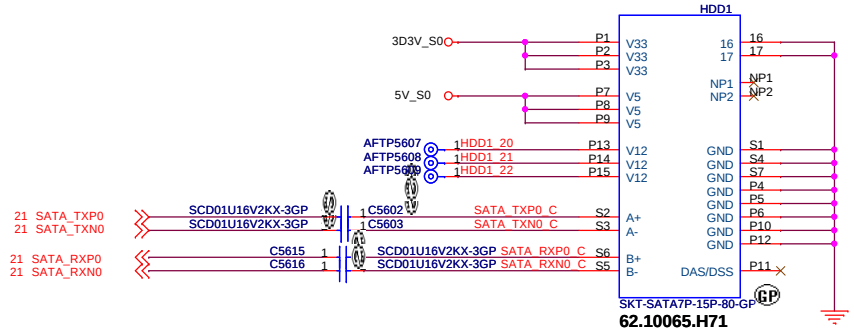
Date: Friday, December 30, 2011 | Sheet 55 of 104

SSID = SATA

SATA HDD Connector

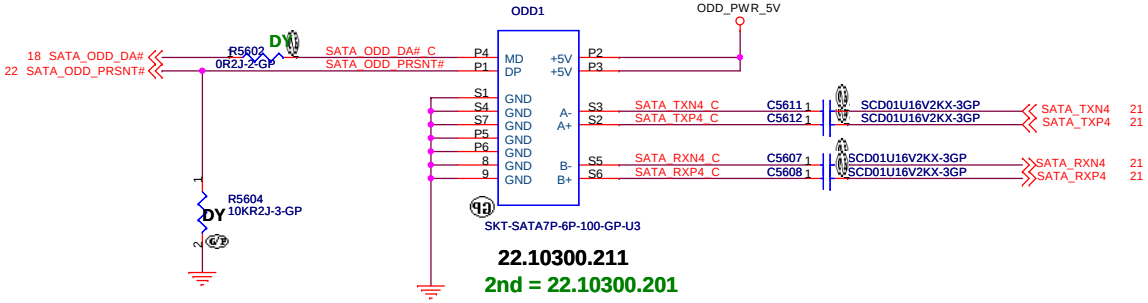


Close to HDD1



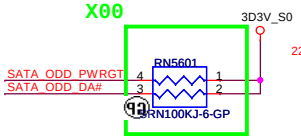
2nd = 62.10065.H81

ODD Connector



22.10300.211

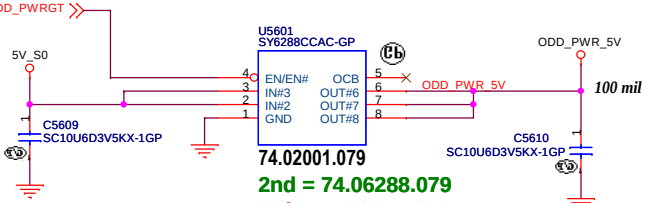
2nd = 22.10300.201



follow CKL1.5

SUPPORT ZERO SATA ODD

SATA Zero Power ODD



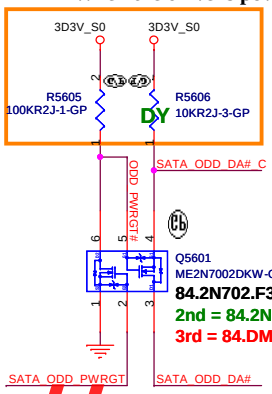
74.02001.079

2nd = 74.06288.079

3rd = 74.02311.079

Current limit
Active High
typ =>2.5A

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



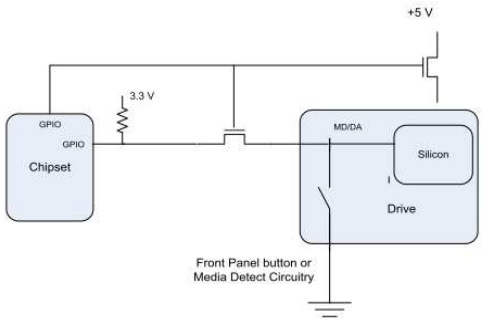
84.2N702.F3F

2nd = 84.2N702.A3F

3rd = 84.DMN66.03F

A00-0408 Add R5606 to pull high 3.3V_S0
Change pull high to 3.3V_S0

A00-0415 Dummy R5606



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Tuesday, January 03, 2012 | Sheet 56 of 104

SSID = ESATA

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

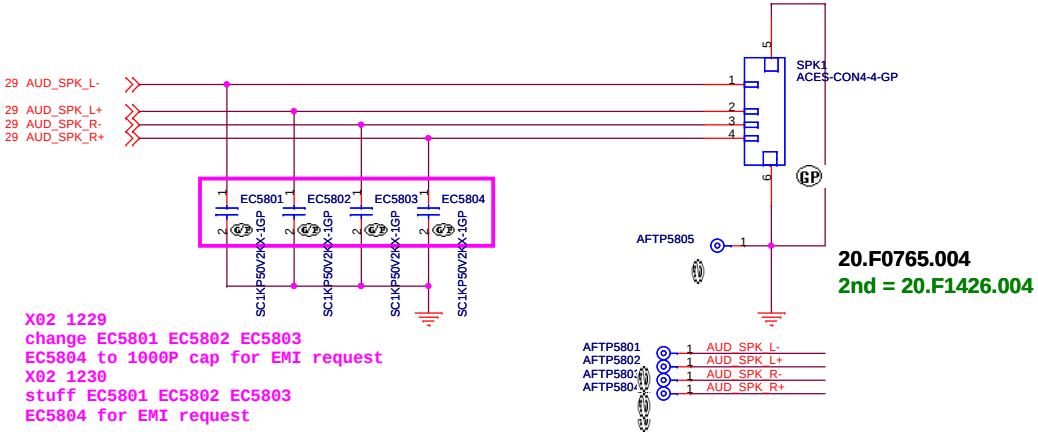
Title: ESATA

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Friday, December 30, 2011 | Sheet 57 of 104

SSID = AUDIO

Speaker Connector



20.F0765.004

2nd = 20.F1426.004

X02 1229
change EC5801 EC5802 EC5803
EC5804 to 1000P cap for EMI request
X02 1230
stuff EC5801 EC5802 EC5803
EC5804 for EMI request

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPEAKER CONN

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

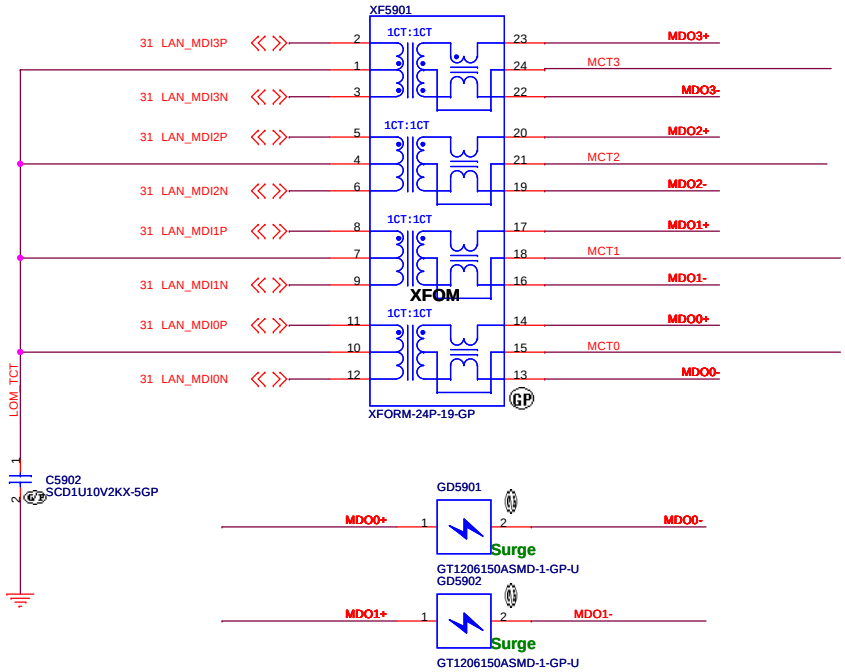
Date: Tuesday, January 03, 2012 | Sheet 58 of 104

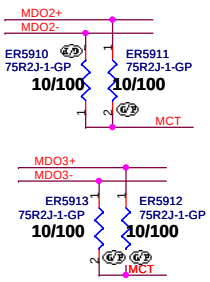
SSID = LOM

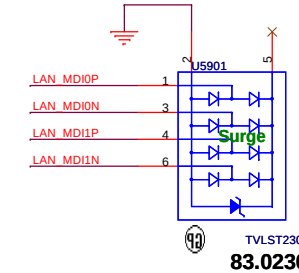
LAN TransFormer

Giga Main: 68.IH106.30C
Giga 2ND: 68.05009.30A

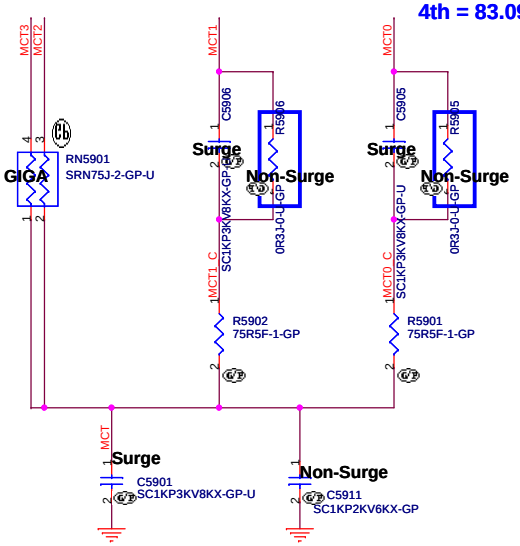
10/100 Main: 68.HH085.301





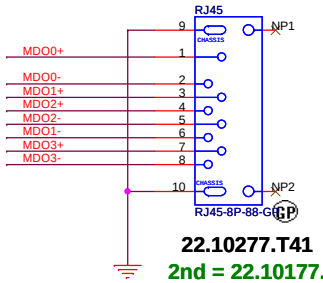


83.02304.0AE
2nd = 83.42236.0AE
3rd = 83.08902.0AE
4th = 83.09904.AAE

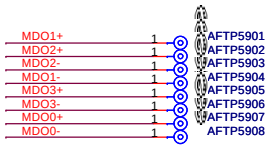


0722 : change to gas tube

RJ45



22.10277.T41
2nd = 22.10177.J61



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XFOM&RJ45

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A3	Enrico Caruso 14 MLK DIS	X02

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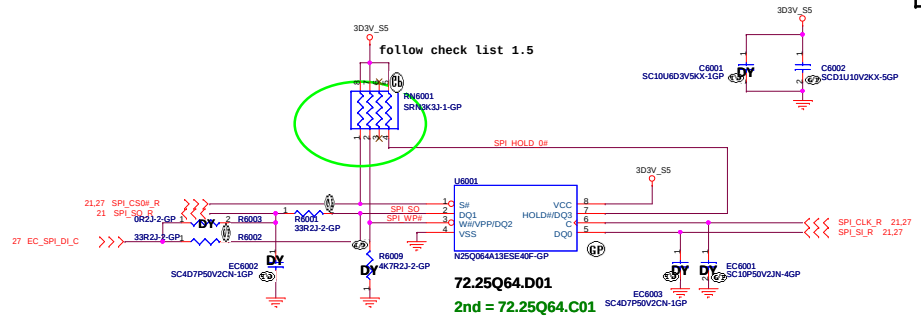
SSID = Flash.ROM

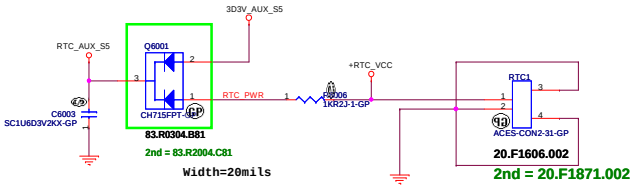
PCH
SPI
KBC

SPI Flash ROM(8M) for PCH

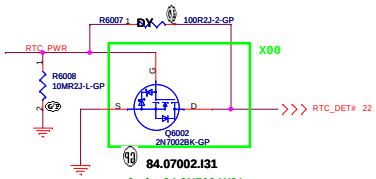


72.25Q64.D01
2nd = 72.25Q64.C01
3rd = 72.25Q64.B01
4th = 72.25640.D01

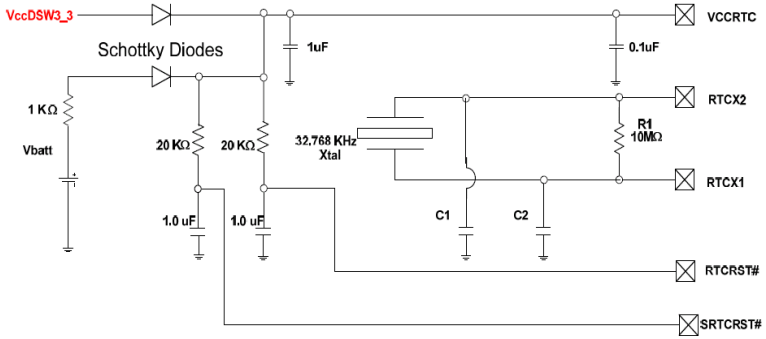
SSID = RBATT



83.R0304.B81
2nd = 83.R2004.C81
20.F1606.002
2nd = 20.F1871.002



84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31



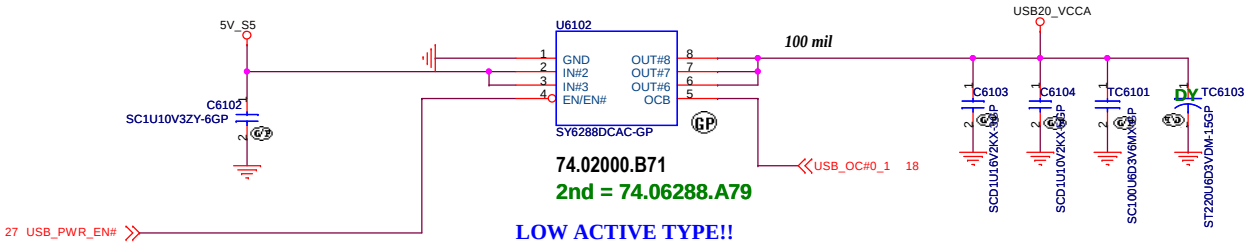
VccRTC is now connected to VccDSW3_3 through the Schottky diode instead of the 3.3V Sus well.

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Flash/RTC*
Size: A2
Document Number: Enrico Caruso 14 MLK DIS
Rev: X02
Date: Tuesday, January 03, 2012
Sheet 60 of 104

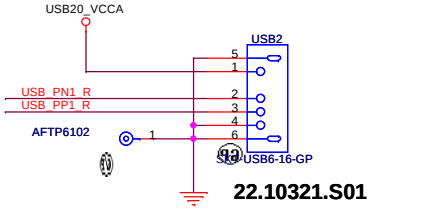
SSID = USB



74.02000.B71

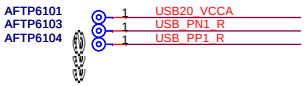
2nd = 74.06288.A79

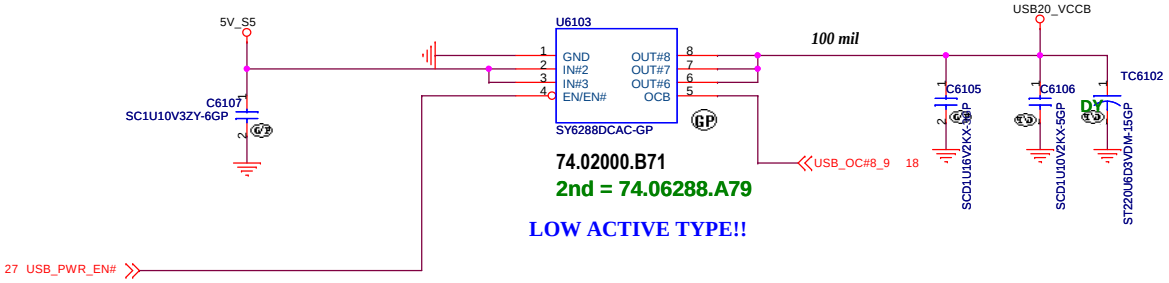
LOW ACTIVE TYPE!!



22.10321.S01

2nd = 22.10341.831





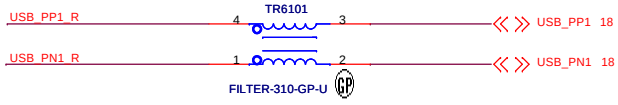
74.02000.B71

2nd = 74.06288.A79

LOW ACTIVE TYPE!!

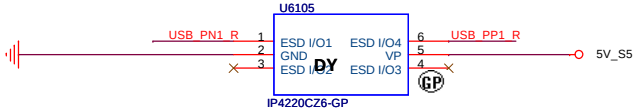
X02 1230

removed R6102,R6103 co-lay position



69.10084.101

2nd = 69.10166.001



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

Size | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Tuesday, January 03, 2012 | Sheet 61 of 104

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

Date: Friday, December 30, 2011 Sheet 62 of 104

SSID = User.Interface

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth

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A3	Enrico Caruso 14 MLK DIS	X02

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RESERVED

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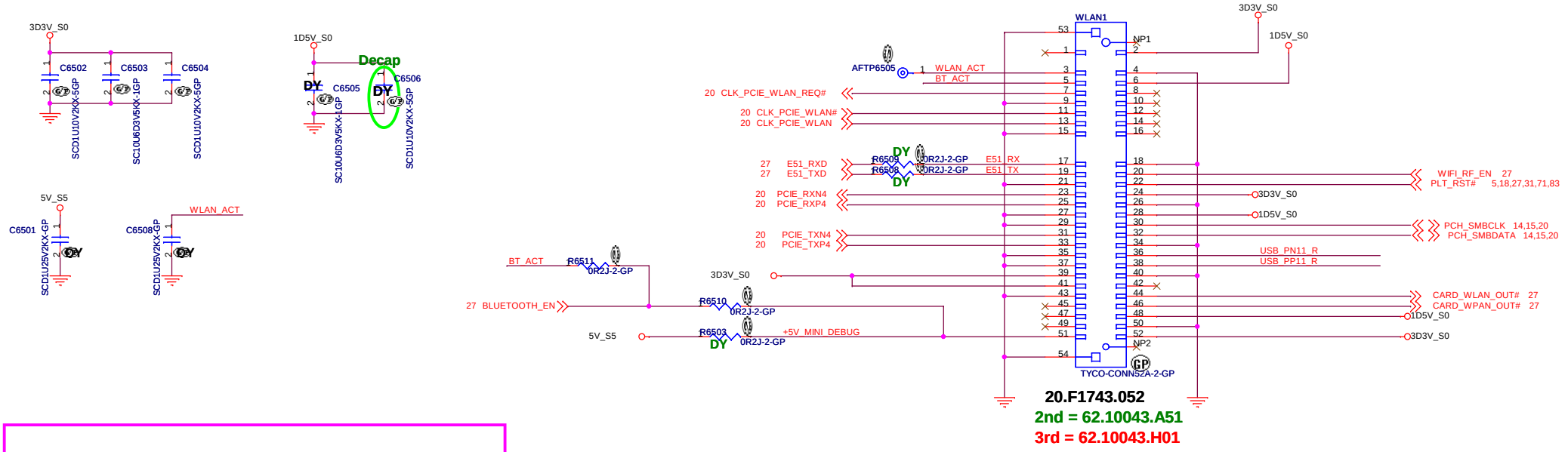
SSID = Wireless

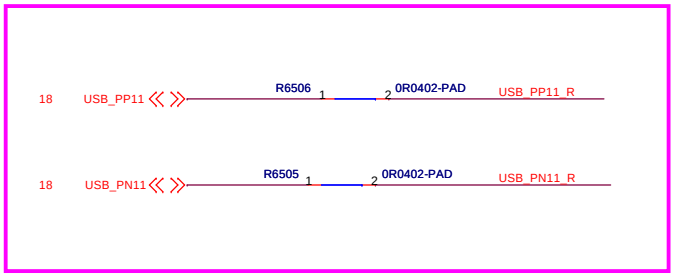
Mini Card Connector(802.11a/b/g)



20.F1743.052

2nd = 62.10043.A51

3rd = 62.10043.H01



X02 1229
changed R6505,R6506 to short pad,
removed TR6501 CMC footprint

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Tuesday, January 03, 2012 | Sheet 65 of 104

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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A3	*Enrico Caruso 14 MLK DIS*	*X02*

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

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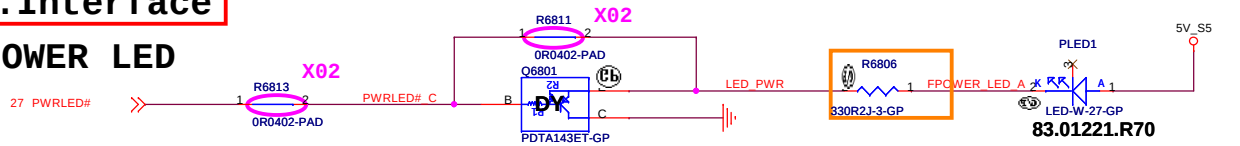
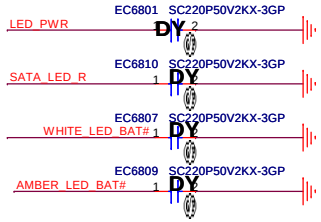
SSID = User.Interface

FRONT POWER LED

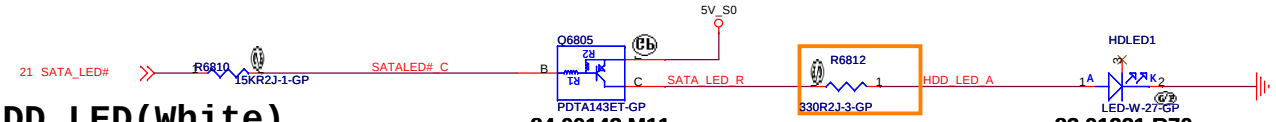


84.00143.M11
2nd = 84.02143.011
3rd = 84.00143.N11

83.01221.R70
2nd = 83.00110.R70
3rd = 83.01105.070



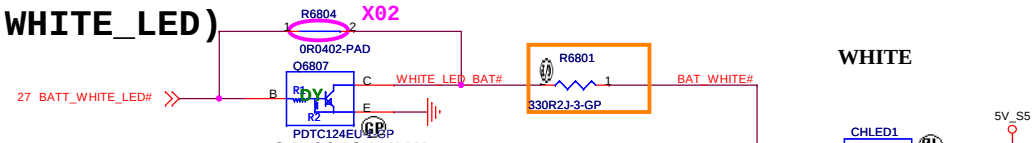
SATA HDD LED(White)



84.00143.M11
2nd = 84.02143.011
3rd = 84.00143.N11

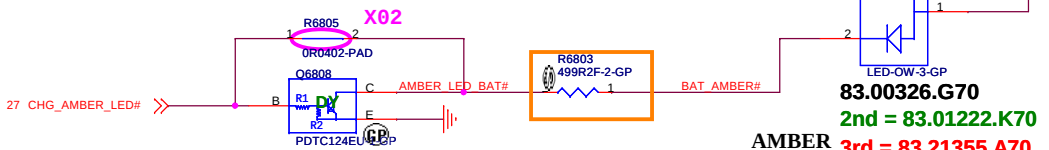
83.01221.R70
2nd = 83.00110.R70
3rd = 83.01105.070

Battery LED2(WHITE_LED)



84.00124.H1K

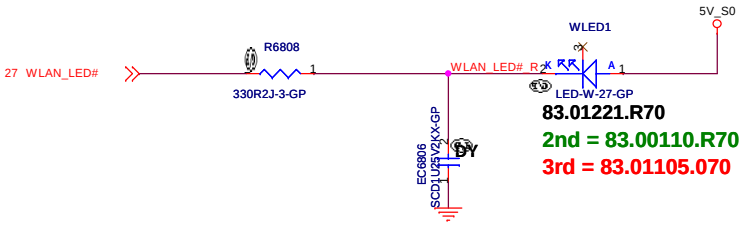
83.00326.G70
2nd = 83.01222.K70
3rd = 83.21355.A70



Battery LED1(AMBER_LED)

84.00124.H1K

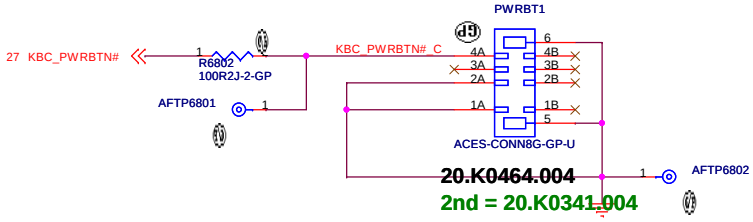
Wireless LED



83.01221.R70
2nd = 83.00110.R70
3rd = 83.01105.070

Place EC6806 near LED2

Power button



20.K0464.004
2nd = 20.K0341.004

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

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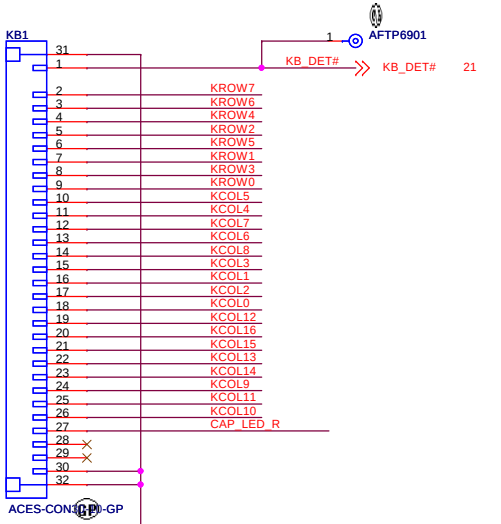
SSID = KBC



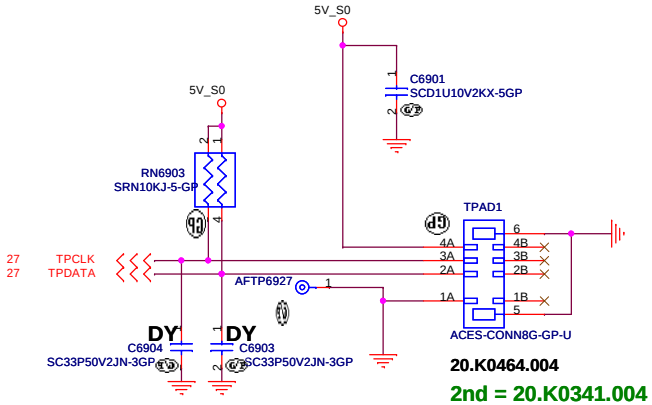
20.K0592.030

2nd = 20.K0621.030

3rd = 20.K0565.030

SSID = Touch.Pad

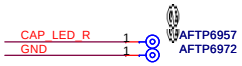
TouchPad Connector



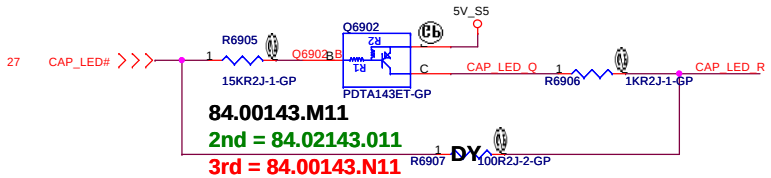
20.K0464.004

2nd = 20.K0341.004

SSID = User.Interface



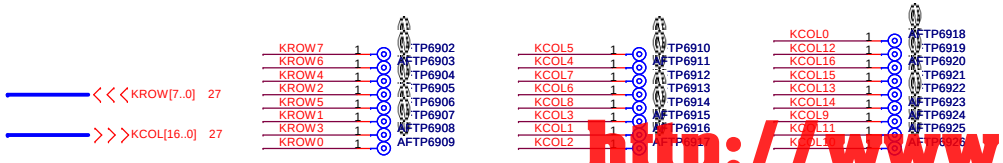
CAP LED CONTROL



84.00143.M11

2nd = 84.02143.011

3rd = 84.00143.N11



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Hall Sensor

Size	Document Number	Rev
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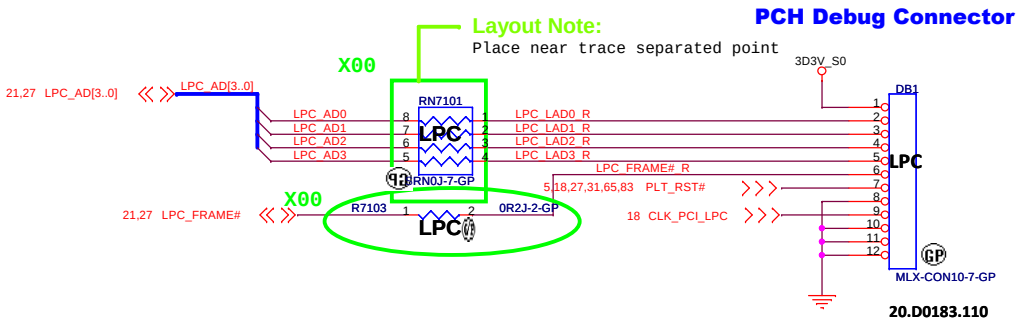

<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Debug connector

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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A3	*Enrico Caruso 14 MLK DIS*	*X02*

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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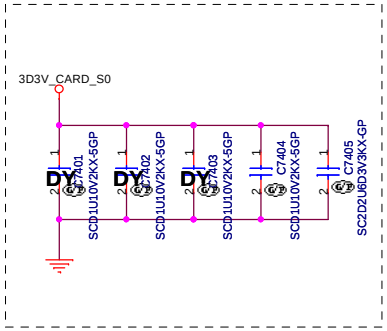
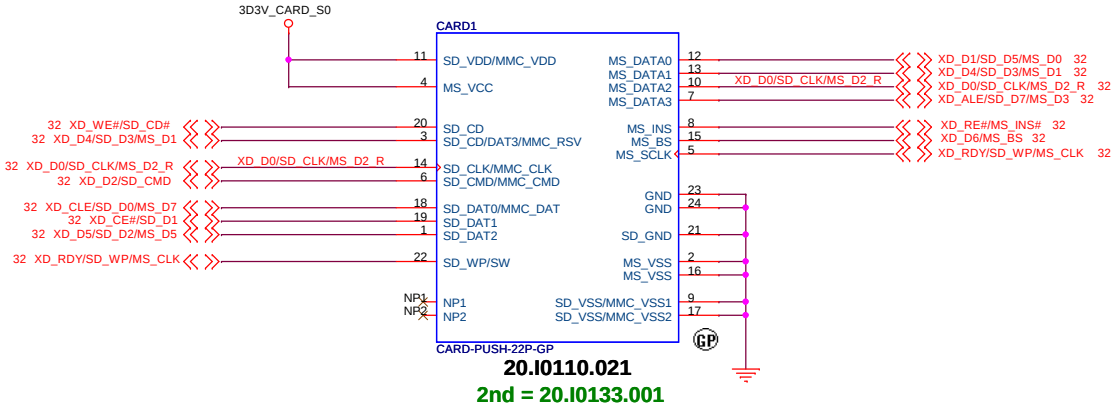
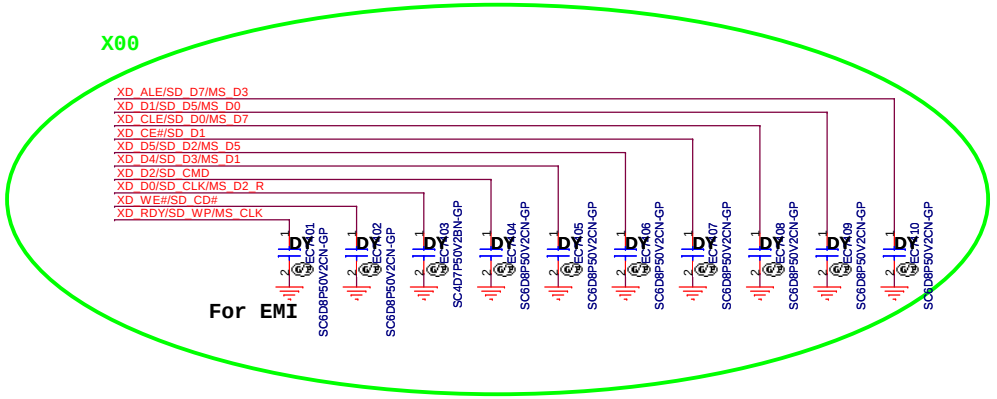
SSID = SDIO





20.I0110.021

2nd = 20.I0133.001



<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SD/XD/MS/MMC Card CONN

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

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SSID = ExpressCard

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Express Card

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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A3	*Enrico Caruso 14 MLK DIS*	*X02*

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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Date: Friday, December 30, 2011 Sheet 78 of 104

SSID = User.Interface

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<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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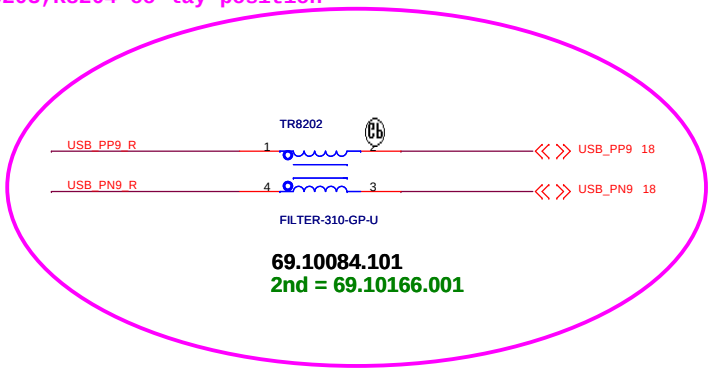
A3	*Enrico Caruso 14 MLK DIS*	*X02*

Date: Friday, December 30, 2011 Sheet 81 of 104

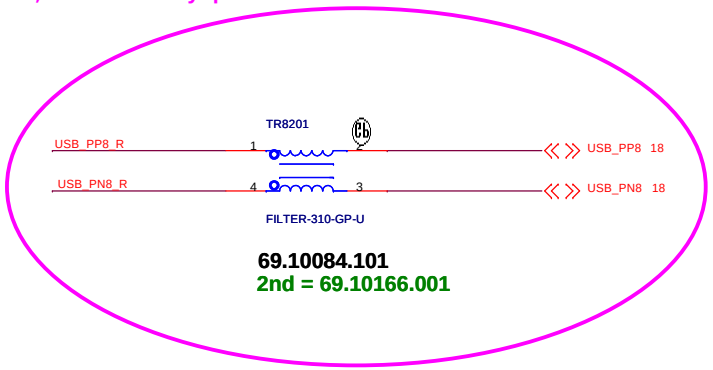
SSID = USB

X02 1230
removed R8203,R8204 co-lay position



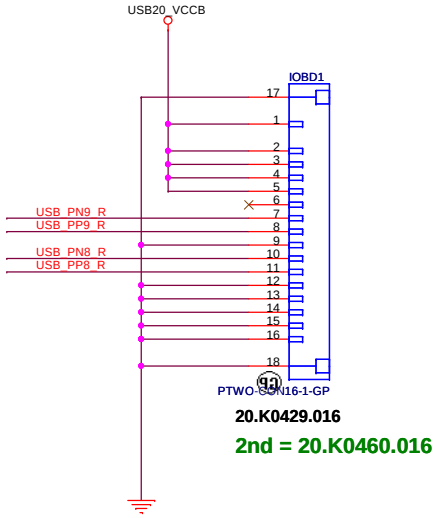
69.10084.101
2nd = 69.10166.001

X02 1230
removed R8201,R8202 co-lay position



69.10084.101
2nd = 69.10166.001

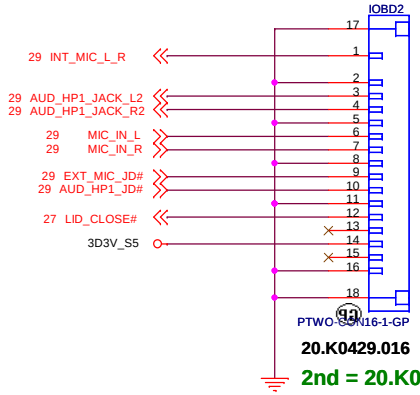
IOBD1 is for USB board



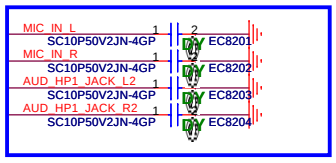
20.K0429.016
2nd = 20.K0460.016

SSID = Audio

IOBD2 is for Audio board



20.K0429.016
2nd = 20.K0460.016



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

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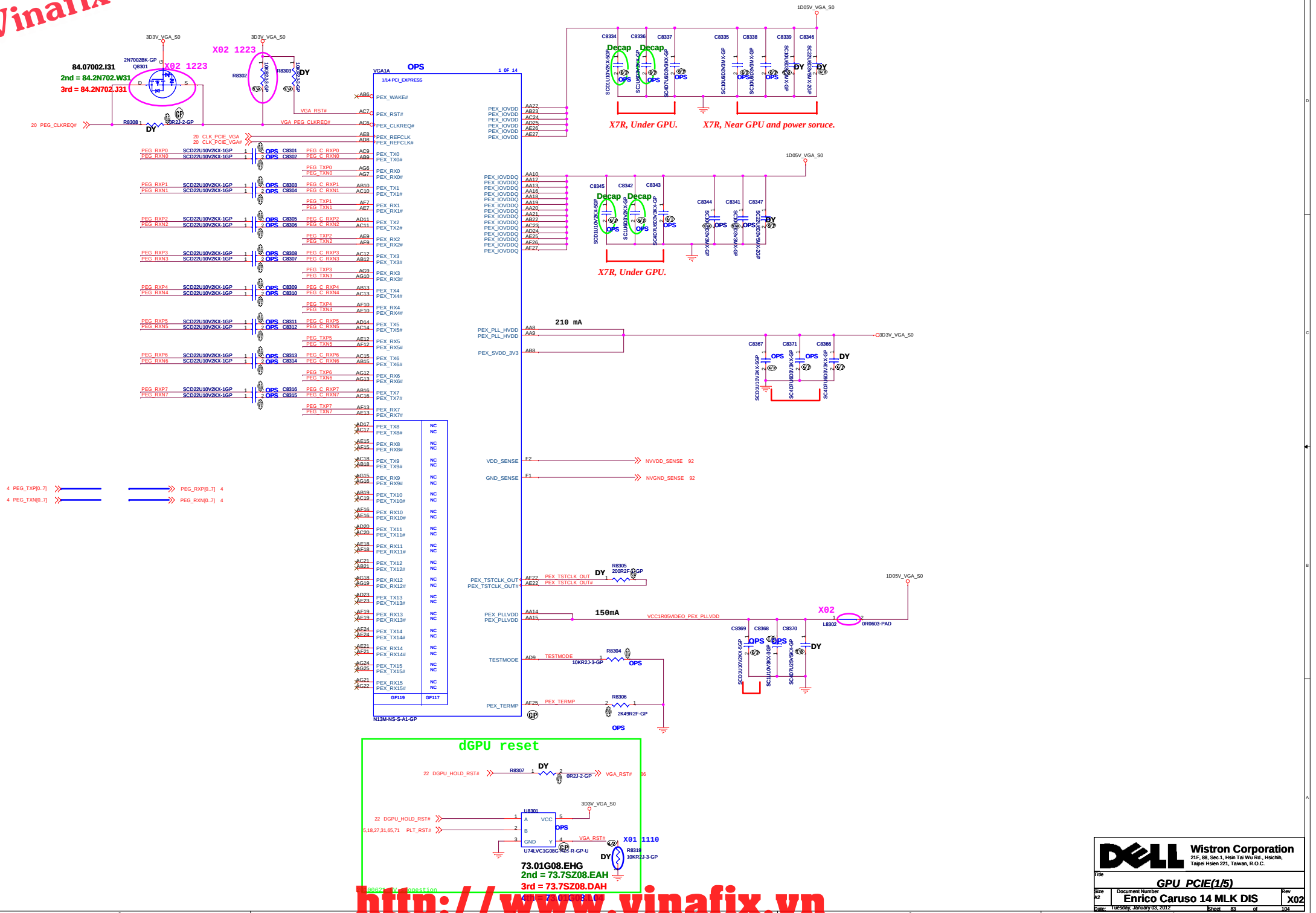

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GPU_PCIE(1/5)
Size	A2
Document Number	Enrico Caruso 14 MLK DIS
Rev	X02
Date	Tuesday, January 03, 2012
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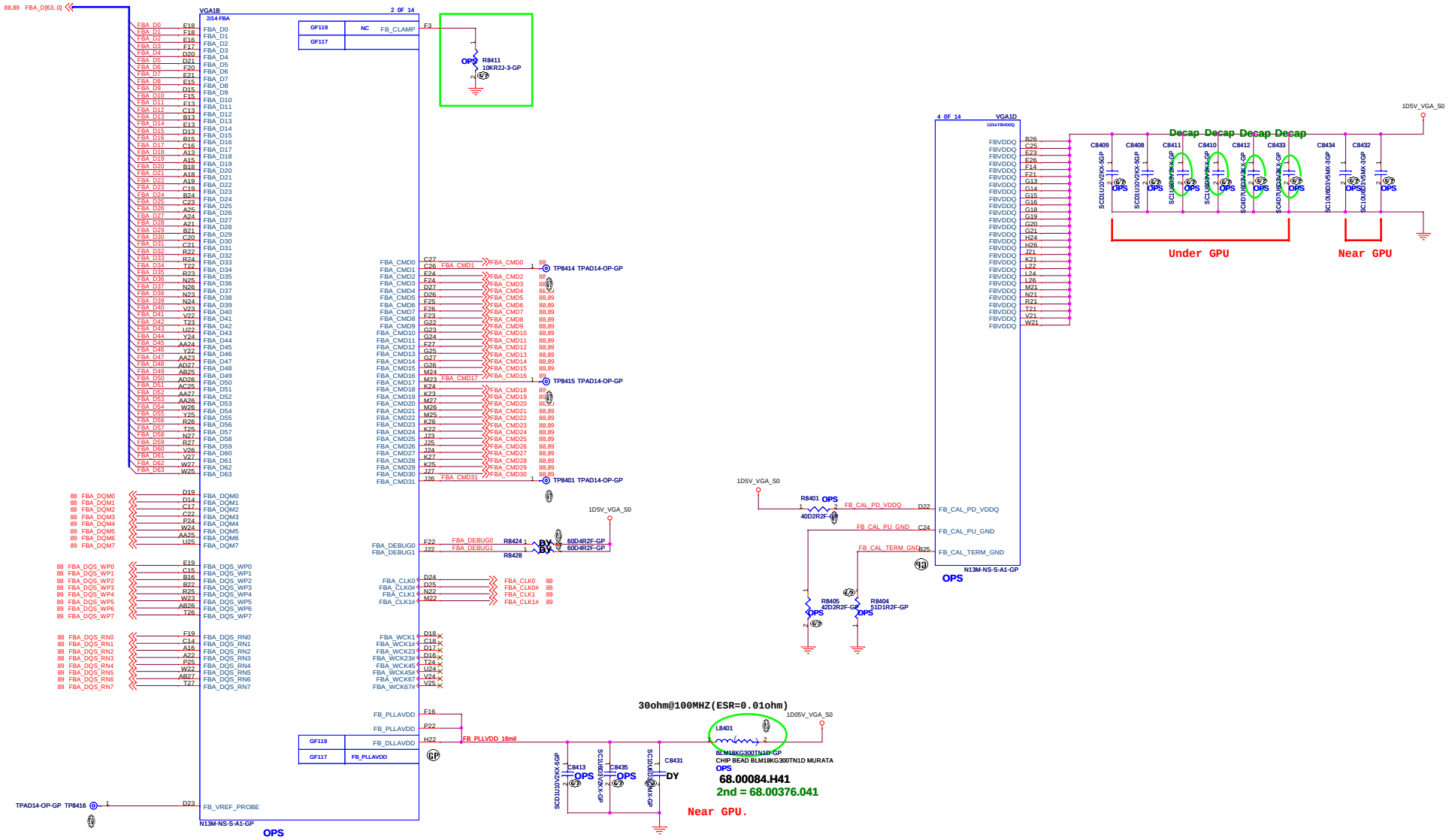

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_Memory(2/5)

Size	Document Number	Rev
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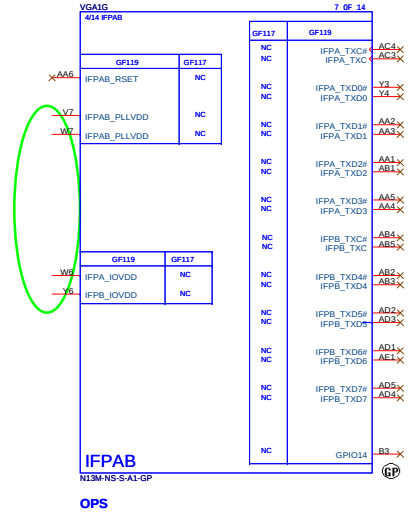
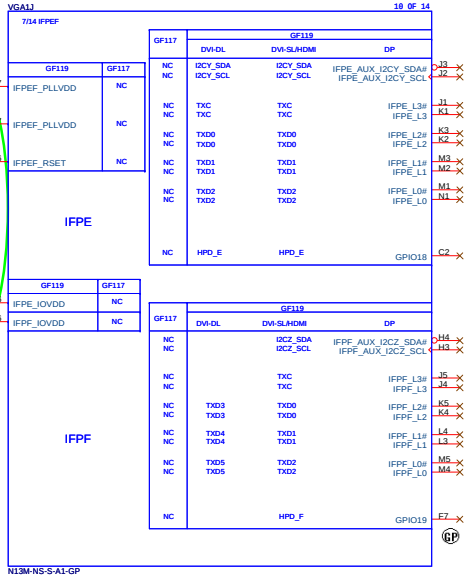
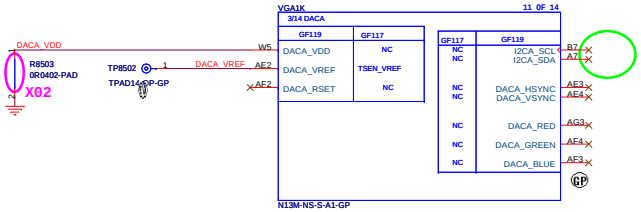
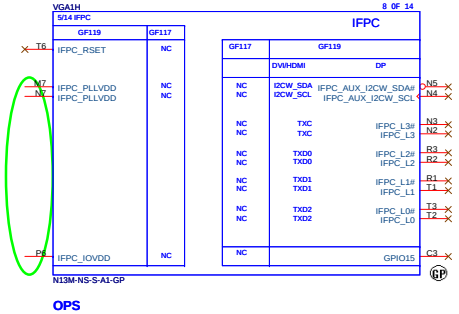
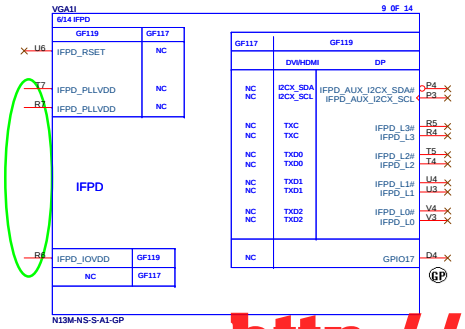
LVDS











Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT(3/5)

Size: A2 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

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1.05V +/- 3%
150mA
1.05VUVS

X7R, Under GPU.

82.30034.641
2nd = 82.30034.651
3rd = 82.30034.681

I2CA=>CRT, I2CC=>LVDS.

X02 1230
add R8608,Q8603;change Q8603.2 to OVER_CURRENT_P8 from AC_PRESENT for OC trigger IPCC fuction

GPIO12
1 - > normal mode
0 -> P8 mode

84.2N702.F3F
2nd = 84.2N702.A3F
3rd = 84.DMN66.03F

84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31

Hynix:72.52G63.A0U (HT31P$AA)
Samsung:72.42164.D0U (JP0F2$AA)

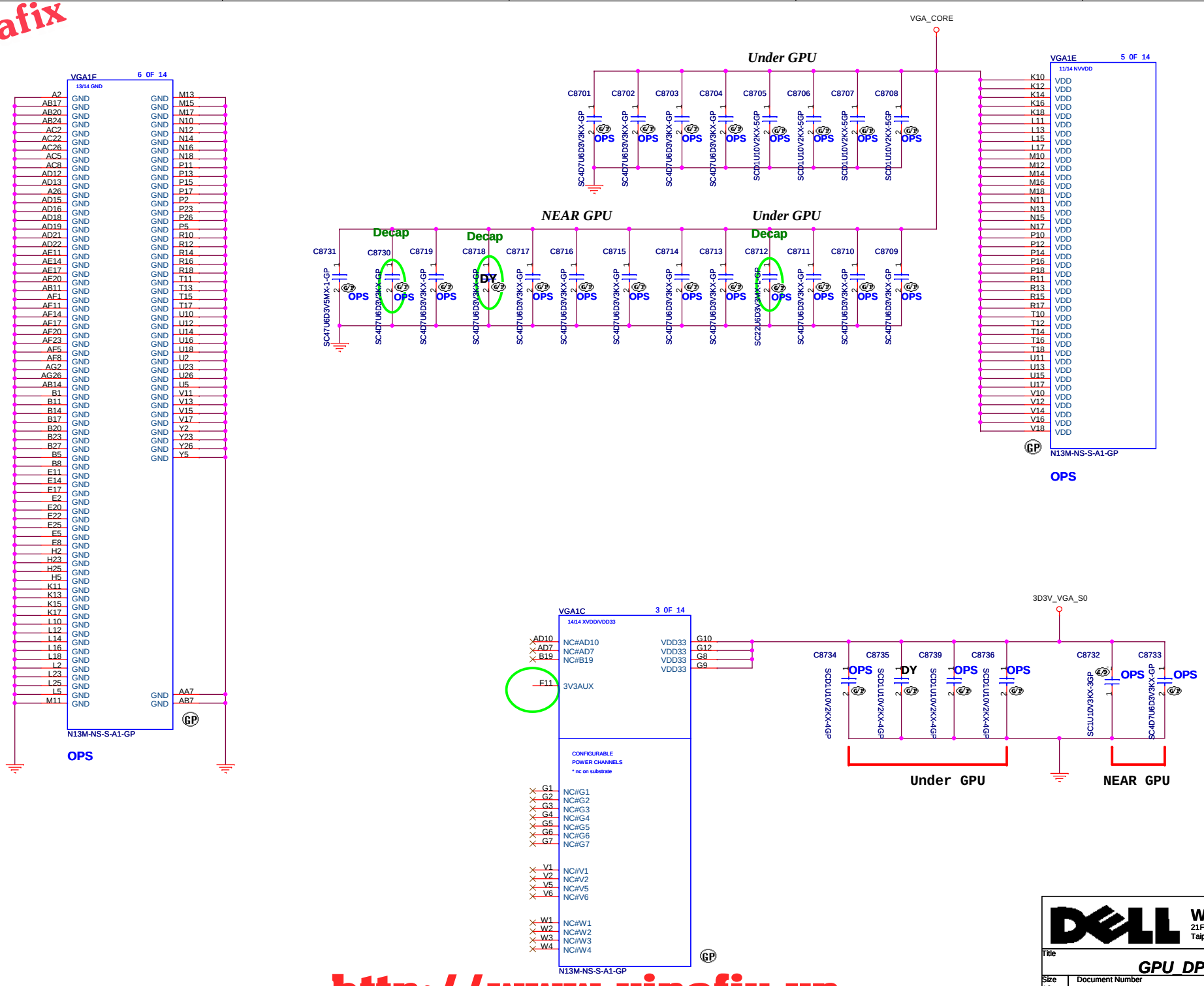
Strap Pin Nmae	Strap mapping	Resistance	Polarity(Samsung0*$)	Polarity(Hynix0*6)
ROM_SCLK	SMB_ALT_ADDR	10K ohm	pull down to GND	pull down to GND
ROM_SI	SUB_VENDOR	10K ohm	pull down to GND if no VBIOS ROM	pull down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10K ohm	pull down to GND(no display)	pull down to GND(no display)
STRAP0	RAM_CFG[0]	10K ohm	pull down to GND	pull down to GND
STRAP1	RAM_CFG[1]	10K ohm	pull up to 3.3V	pull up to 3.3V
STRAP2	RAM_CFG[2]	10K ohm	pull down to GND	pull up to 3.3V
STRAP3	RAM_CFG[3]	10K ohm	pull up to 3.3V	pull down to GND
STRAP4	PCIE_MAX_SPEED	10K ohm	pull down to GND	pull down to GND

N13x GPUs do not support CEC.Leave the CEC pin as NC

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

GPU_GPIO(4/5)

Enrico Caruso 14 MLK DIS X02



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GPU_DPPWR/GND(5/5)
Size	A3
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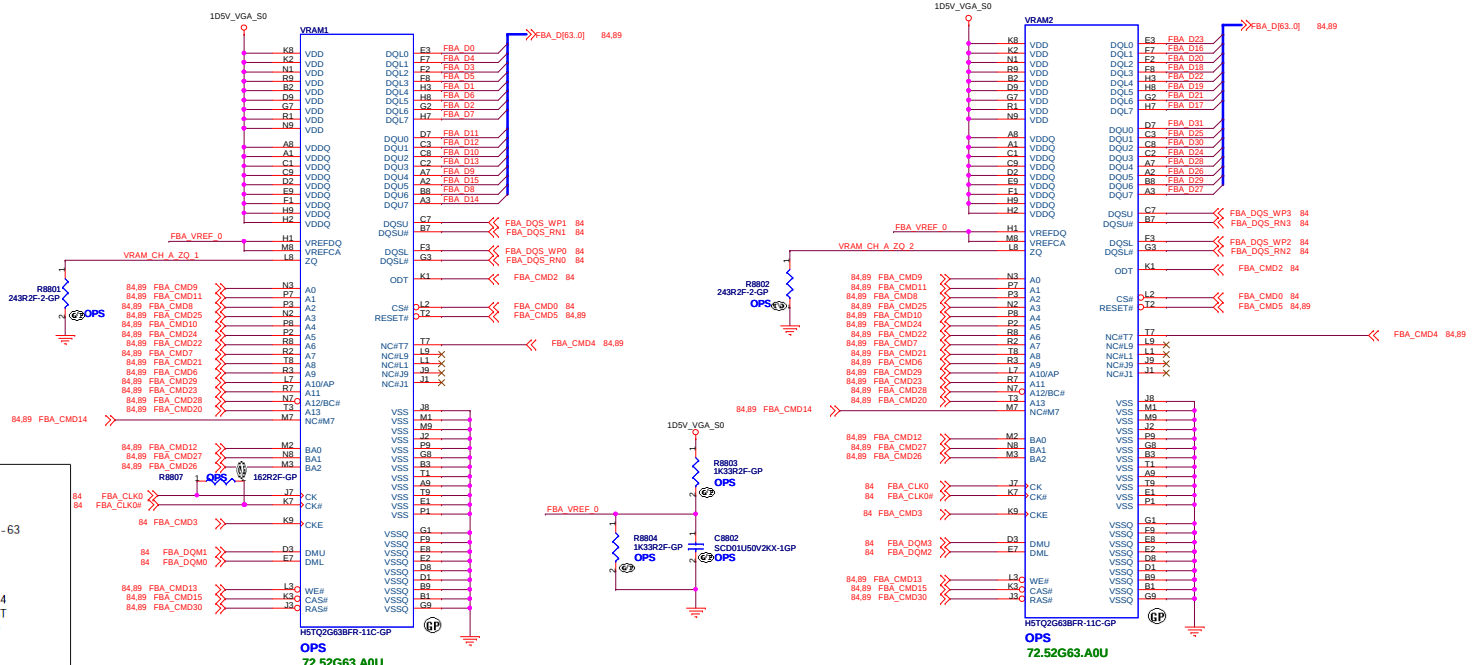


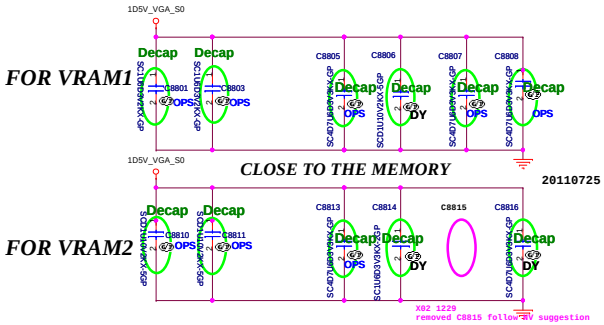
MODE D

GF1XX SDDR3 CMD MAPPING

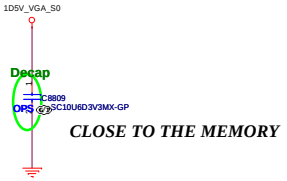
	0-31	32-63
CMD0	CS0*	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	AO	AO
CMD10	A4	A4
CMD11	A1	A1
CMD12	BAO	BAO
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0*
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
CMD31		

* A15 is not required for any x16 device, even up to 4Gb density
* A15 is only needed if we support x8 configurations, and only at 4Gb

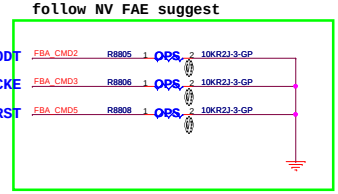
DG requires 4x0.1uF and 8x1.0uF per VRAM chip



20110725 for Vendor



follow NV FAE suggest



Wistron Corporation
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Title: GPU VRAM1,2 (1/4)

Size: A2 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

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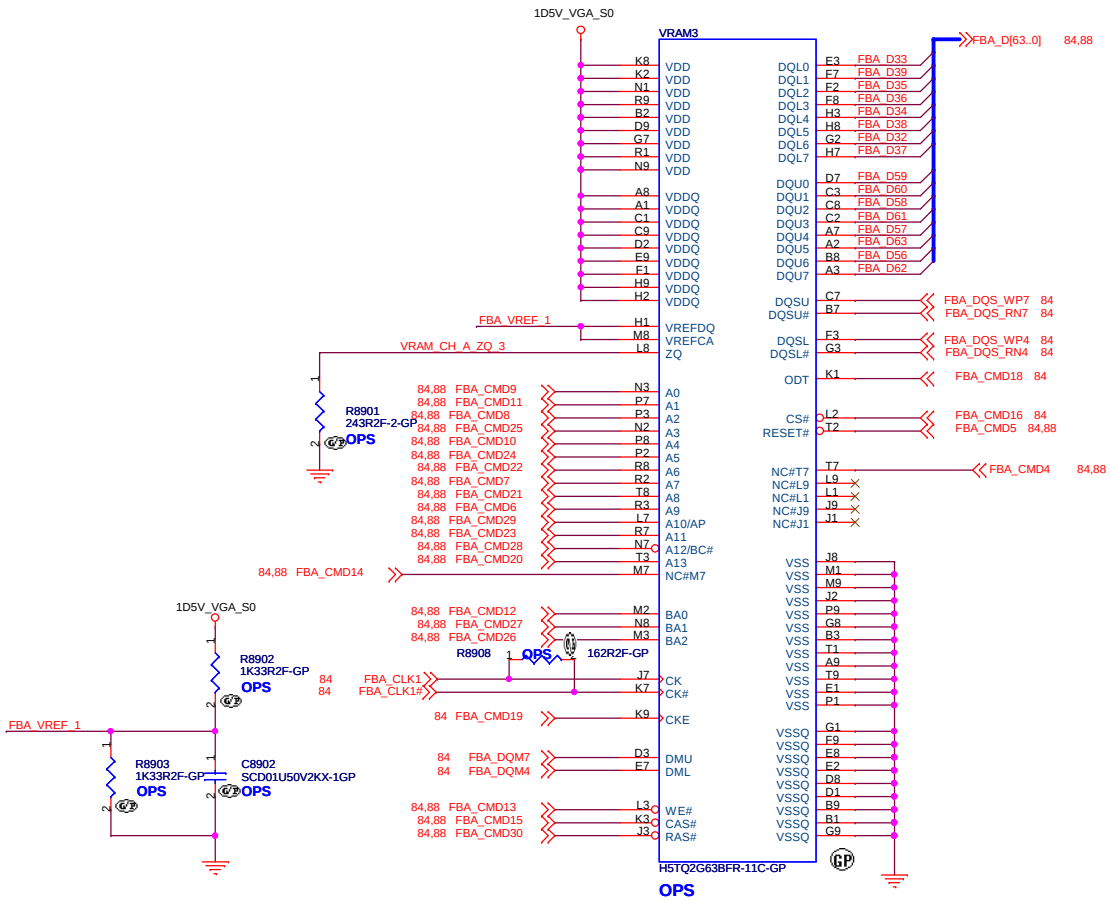

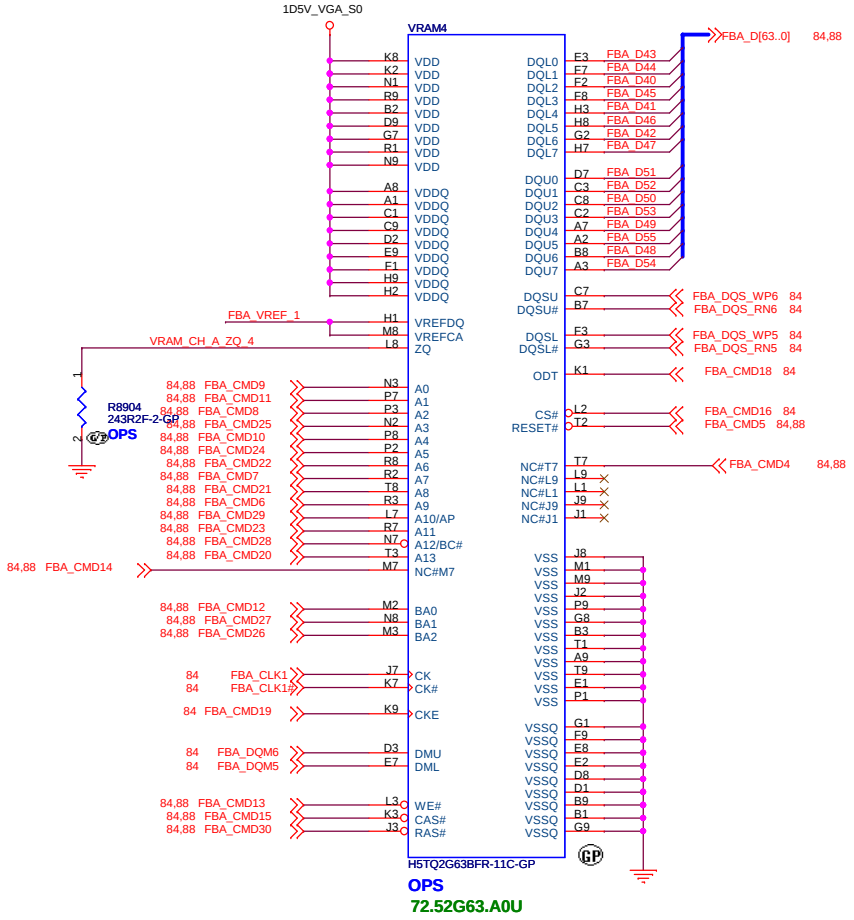

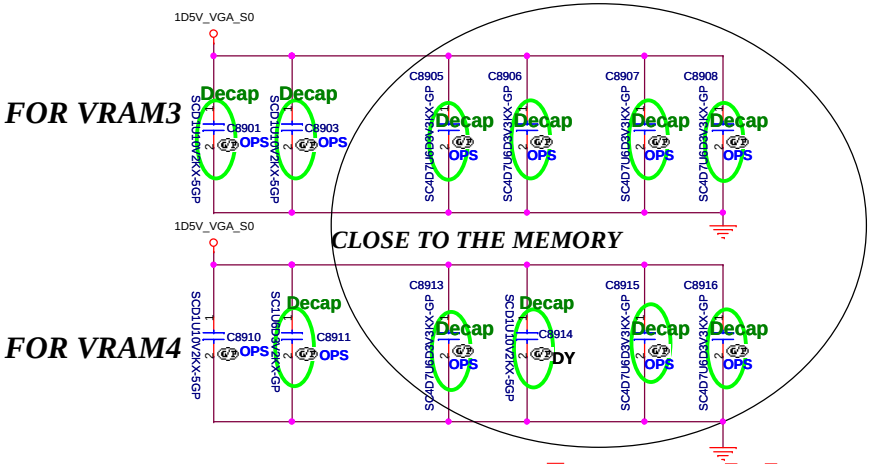

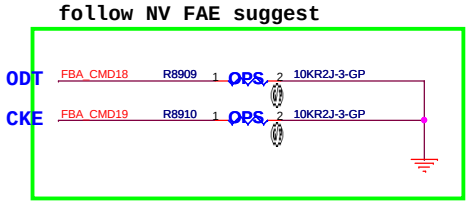

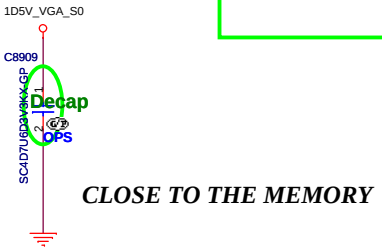

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU VRAM3,4 (2/4)
Size: Custom
Document Number: Enrico Caruso 14 MLK DIS
Rev: X02
Date: Tuesday, January 03, 2012
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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

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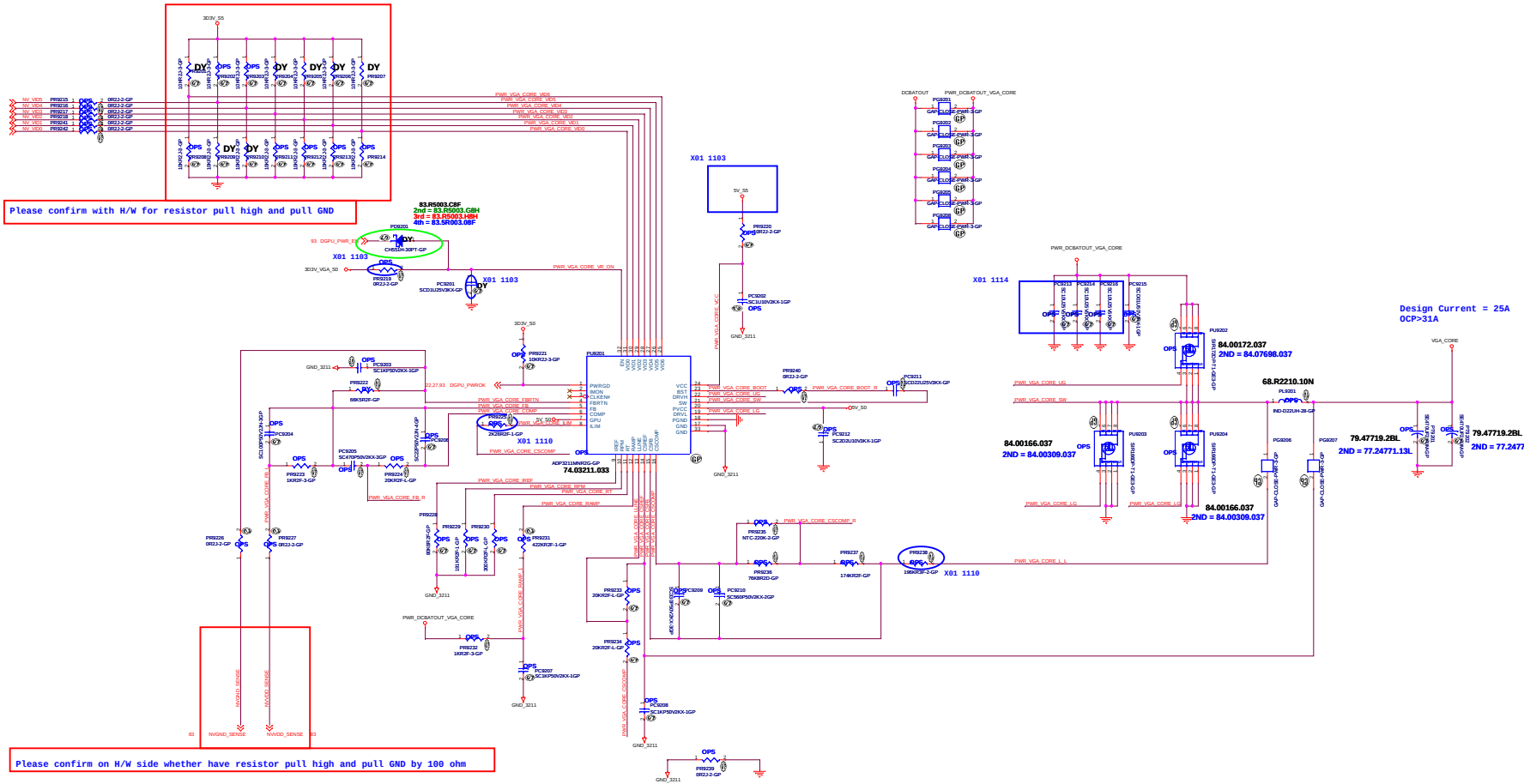
V-BOOT	VID0	VID1	VID2	VID3	VID4	VID5	VID6
0.9000V	0	0	0	0	1	1	0



DELL	Wistron Corporation		
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	ADP3211 +VGA_CORE		
Size: Custom	Document Number: Enrico Caruso 14	Rev: X01	
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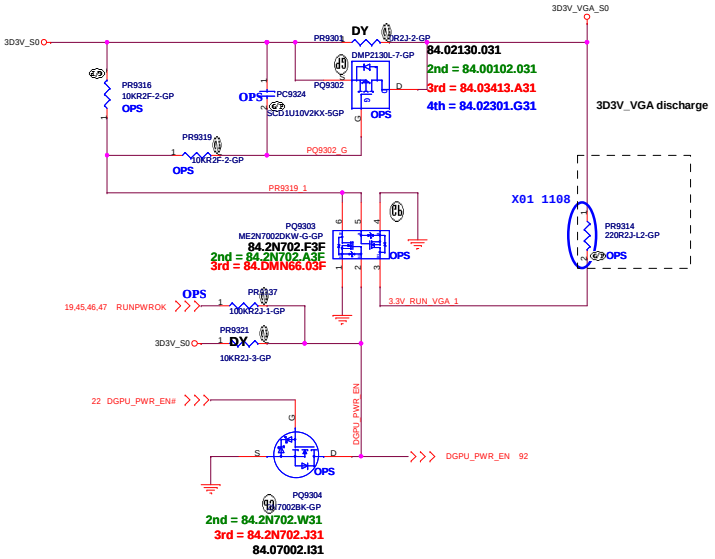
3D3V_S0 to 3D3V_VGA_S0 Transfer



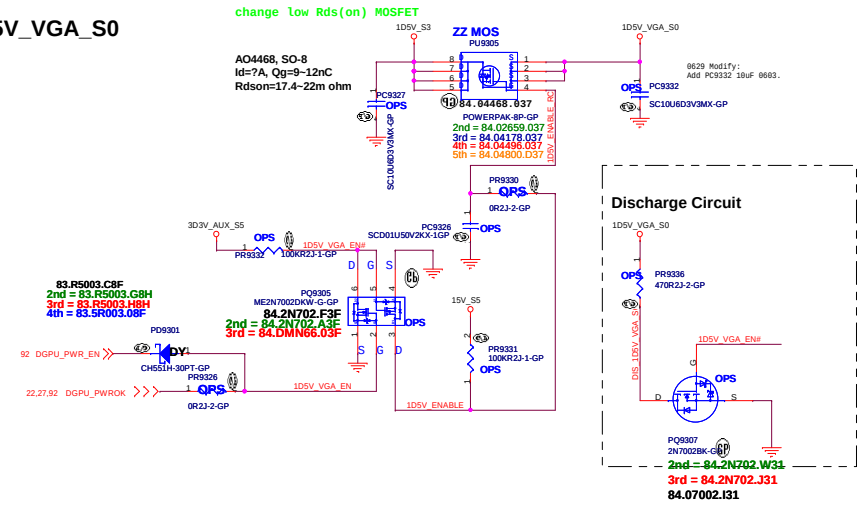
	DGPU_PWR_EN#
dGPU mode	L
IGPU	H
IGPU with BACO	L

NV do not need 1.8V

1D5V_VGA_S0

change low Rds(on) MOSFET

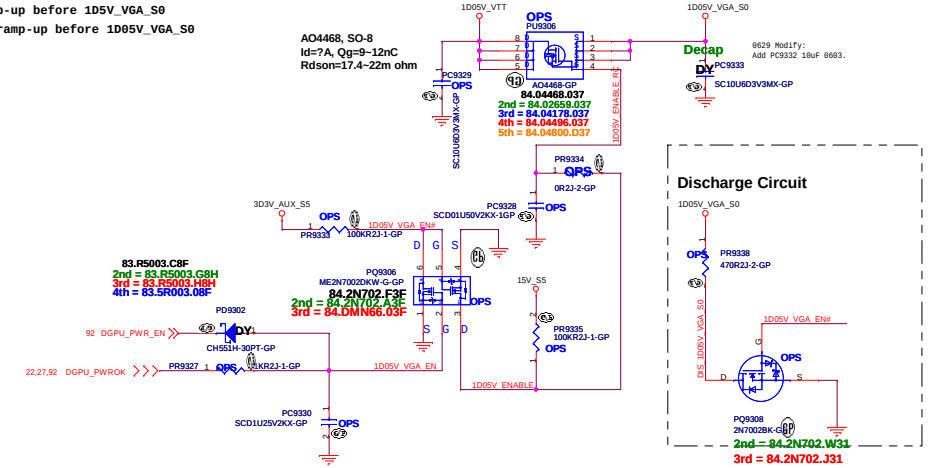
AO4468, SO-8
Id=?A, Qg=9~12nC
Rdson=17.4~22m ohm



1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D5V_VGA_S0 should ramp-up before 1D05V_VGA_S0

AO4468, SO-8
Id=?A, Qg=9~12nC
Rdson=17.4~22m ohm



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size: A2 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X01

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
LVDS_Switch

Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

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(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CRT_Switch*

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

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SSID = SDIO

(Blanking)

<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TOUCH PANEL

Size: A3 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

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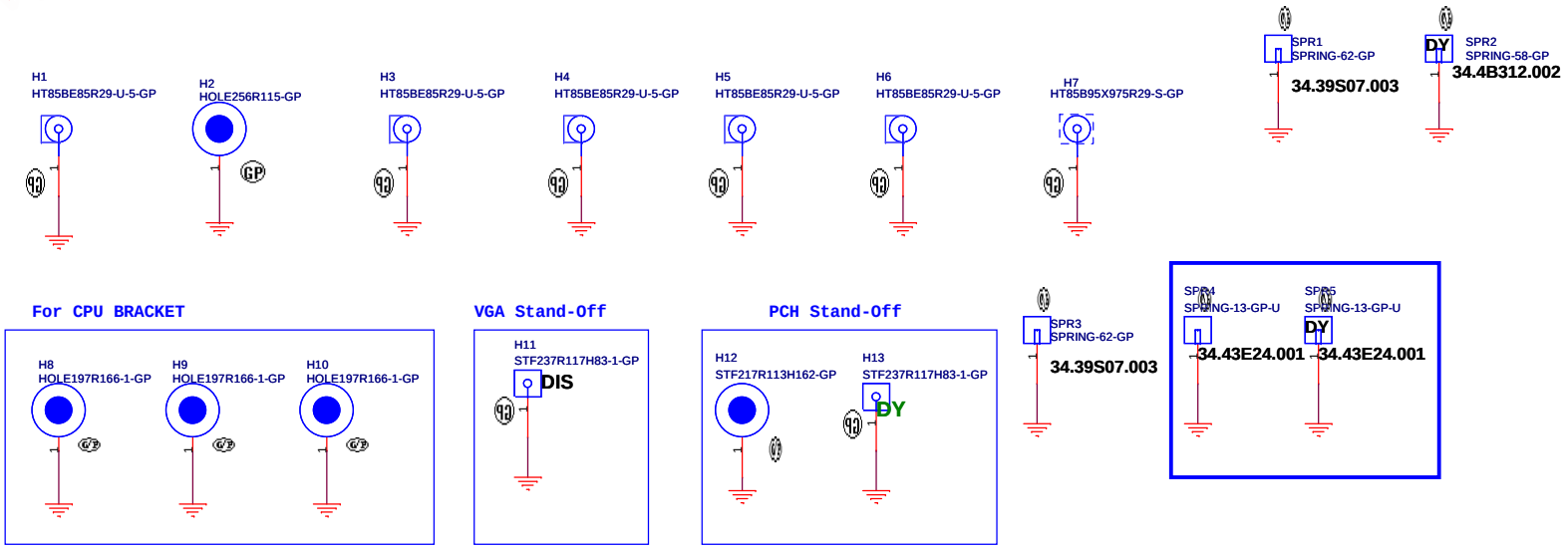
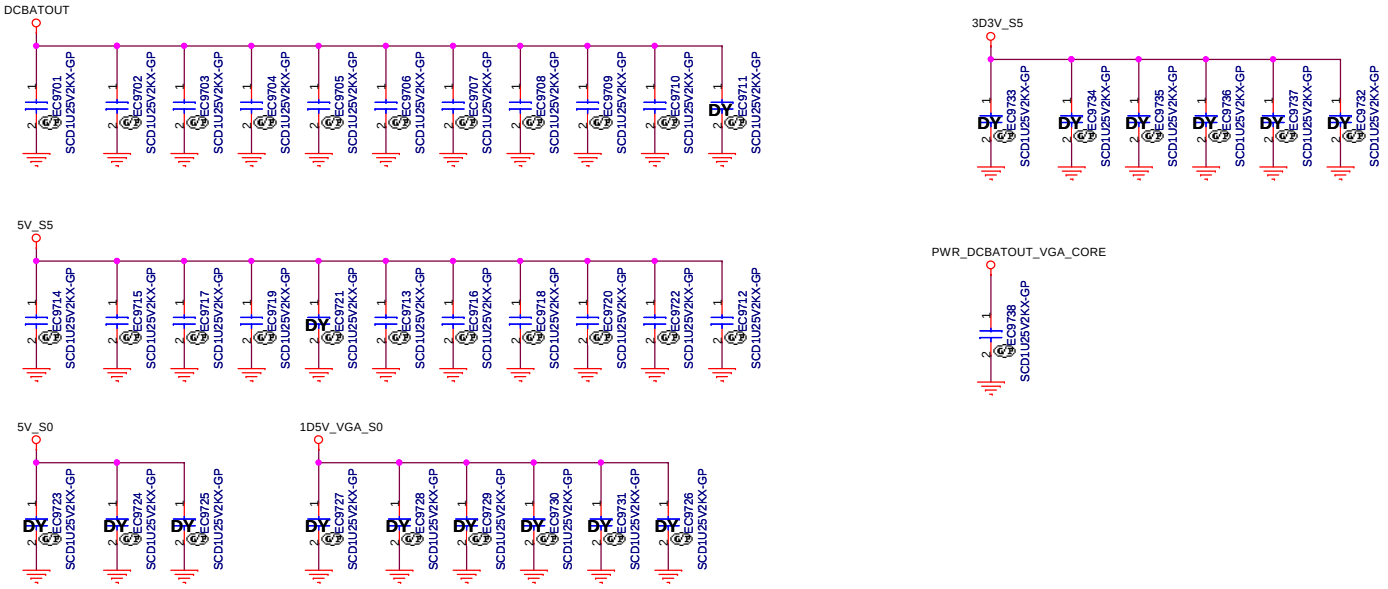
SSID = Mechanical



SSID = EMI



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: UNUSED PARTS/EMI Capacitors

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A3	Enrico Caruso 14 MLK DIS	X02

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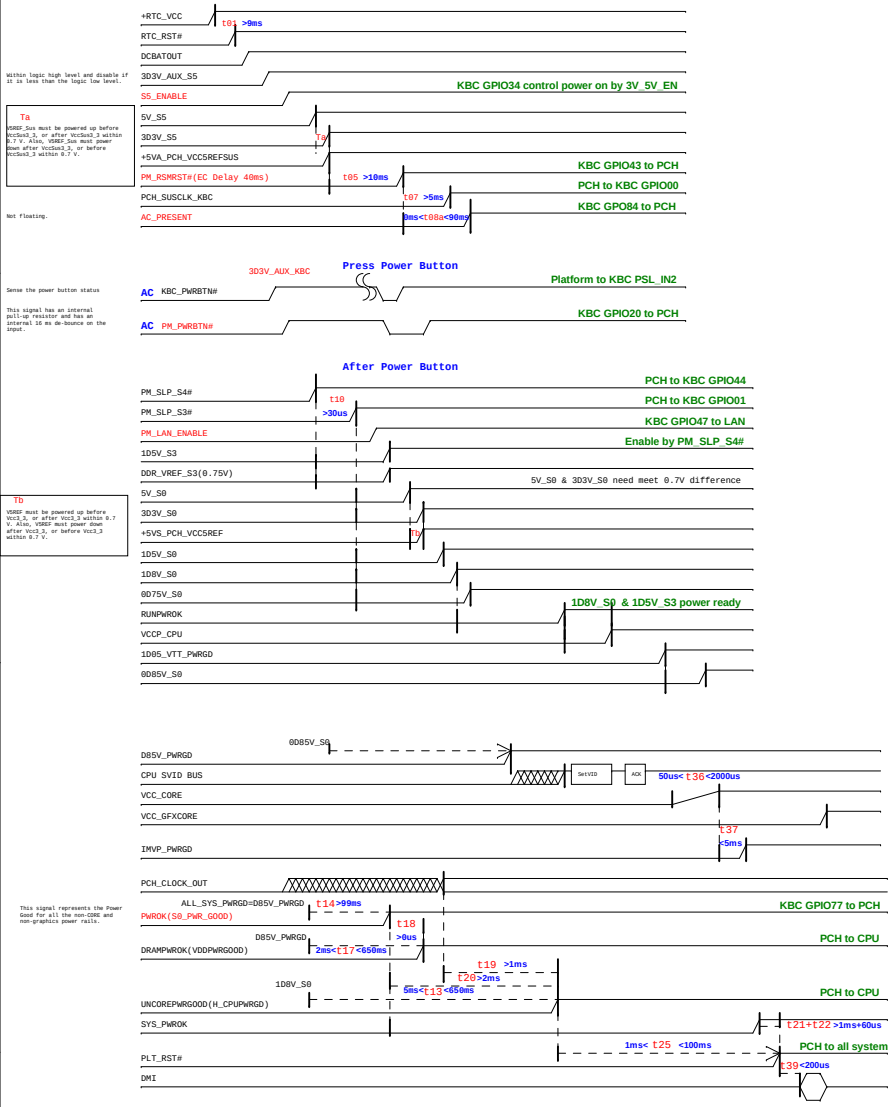
Chief River Platform Power Sequence

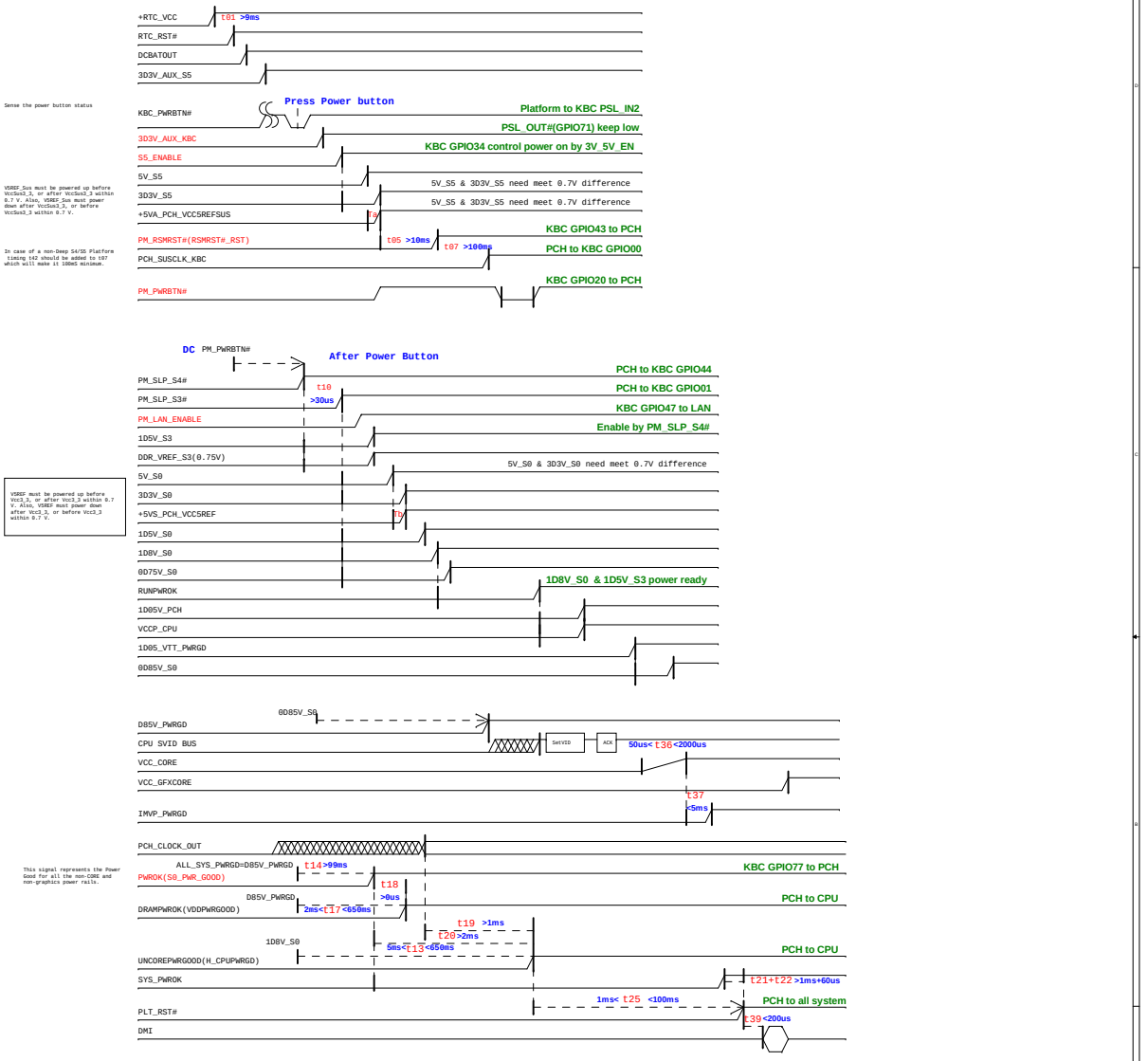
(AC mode)

Red Words: Controlled by EC GPIO

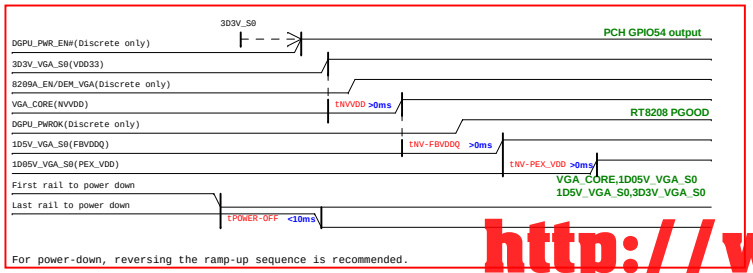


(DC mode)

Red Words: Controlled by EC GPIO



N13M-GS Power-Up/Down Sequence



<Variant Name>

Wistron Corporation
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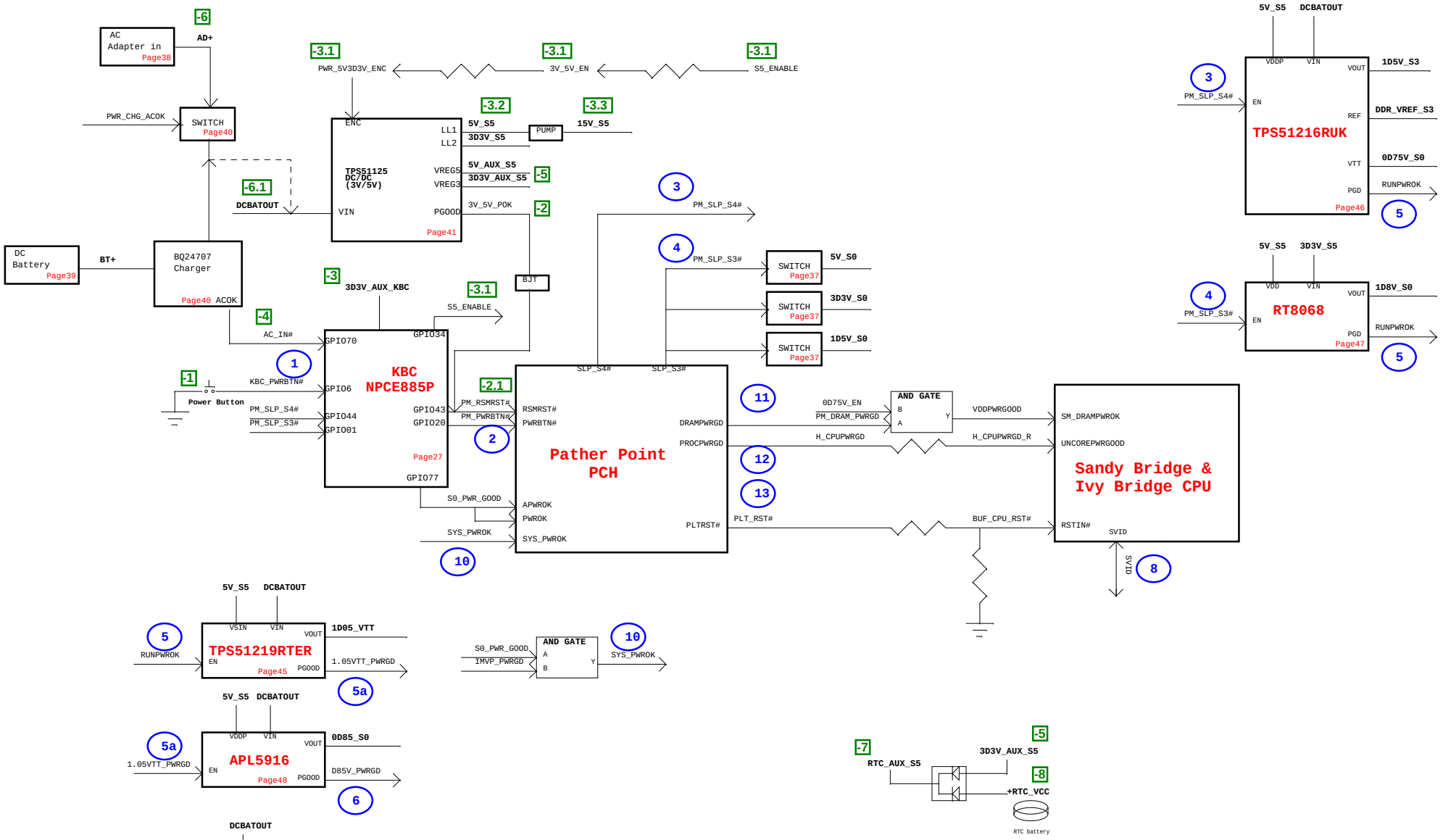
Title: Power Sequence

Size: A1 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

Date: Friday, December 30, 2011 | Sheet 58 of 60

DV14 MLK Chief River POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 13

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence Diagram

Size: A2 | Document Number: Enrico Caruso 14 MLK DIS | Rev: X02

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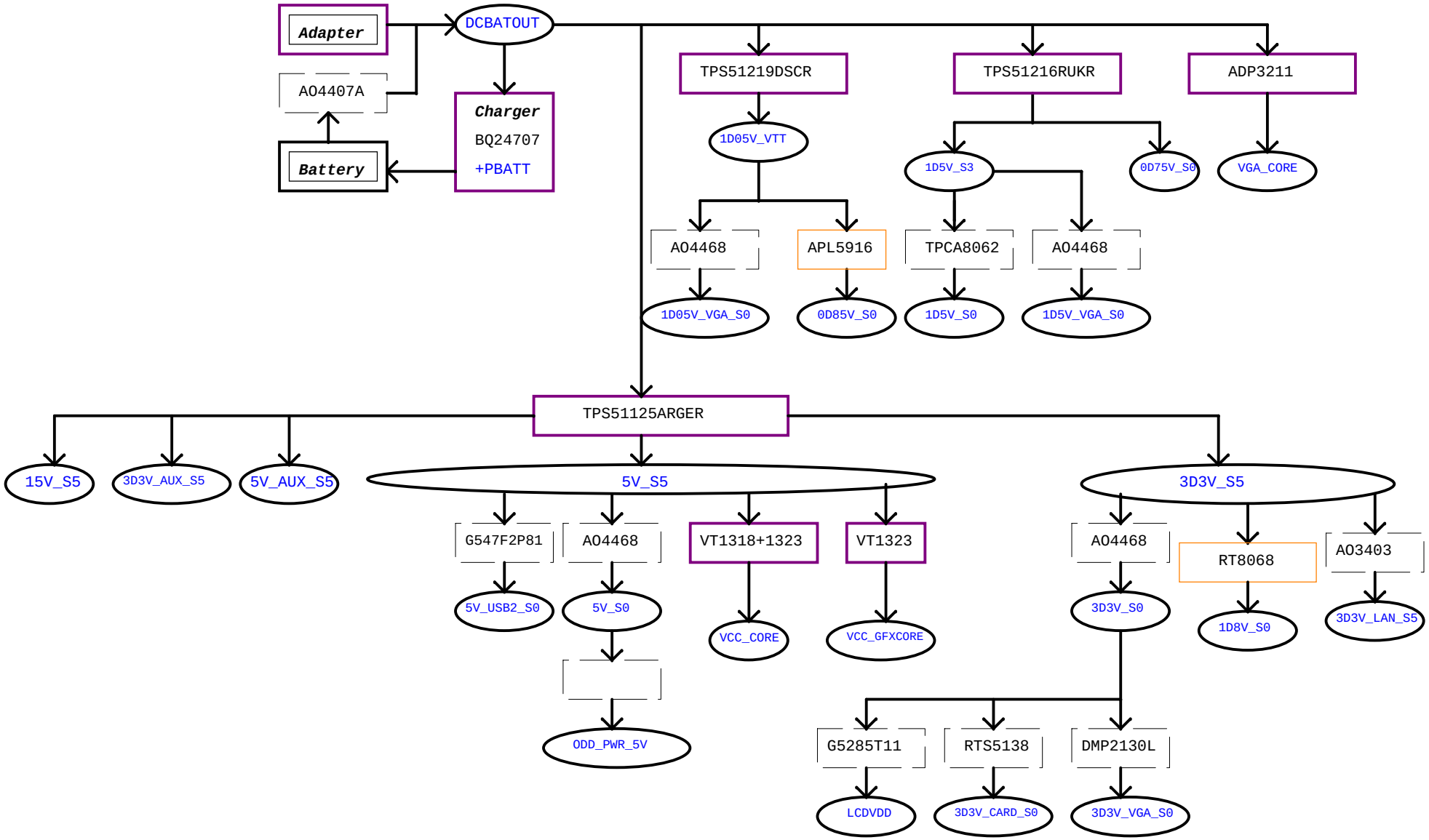

Power Shape

Regulator	LDO	Switch

<Variant Name>

Wistron Corporation
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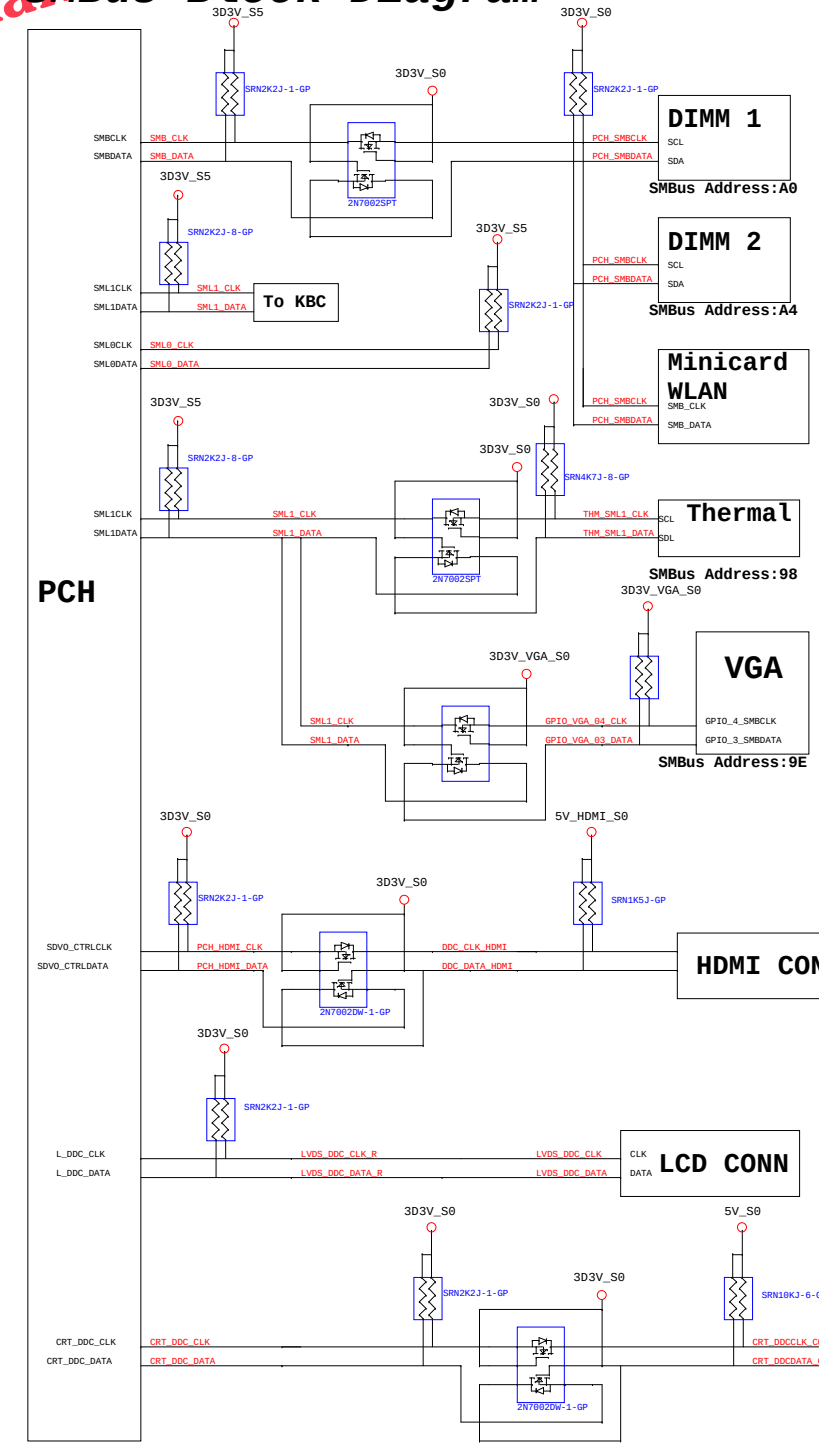
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

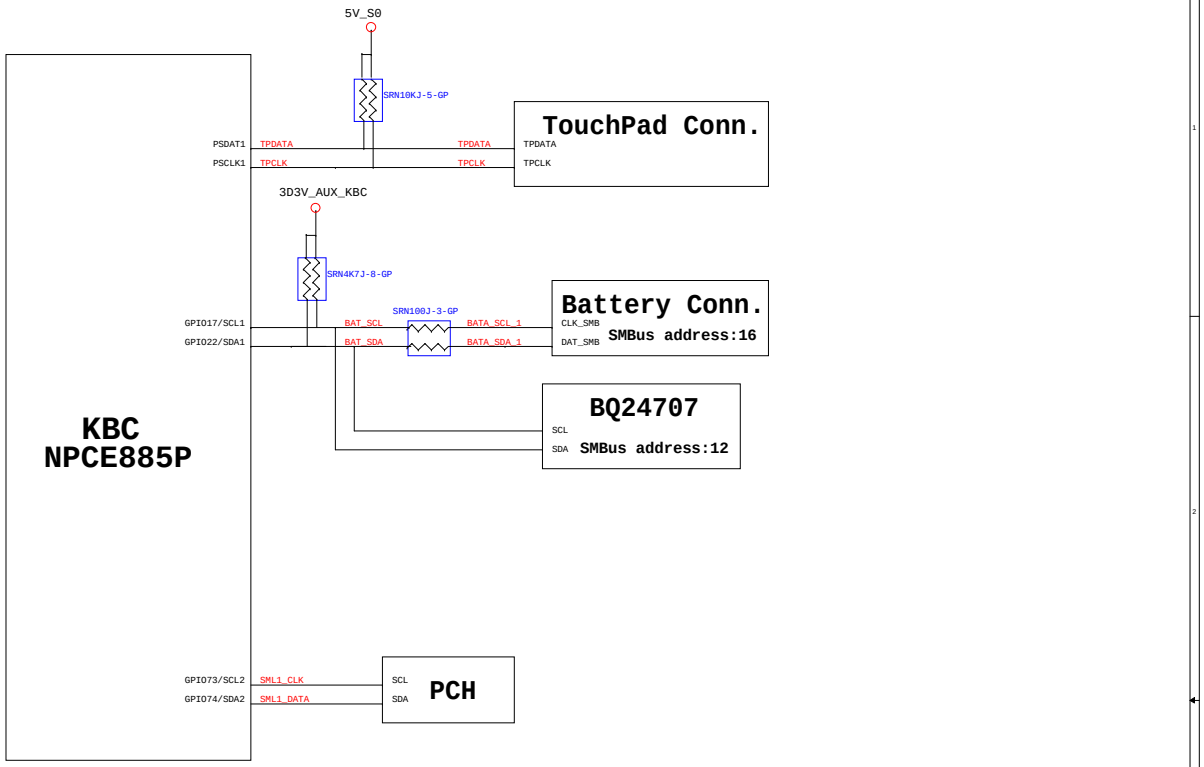
Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

Date: Friday, December 30, 2011 Sheet 100 of 104

PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	Enrico Caruso 14 MLK DIS	X02

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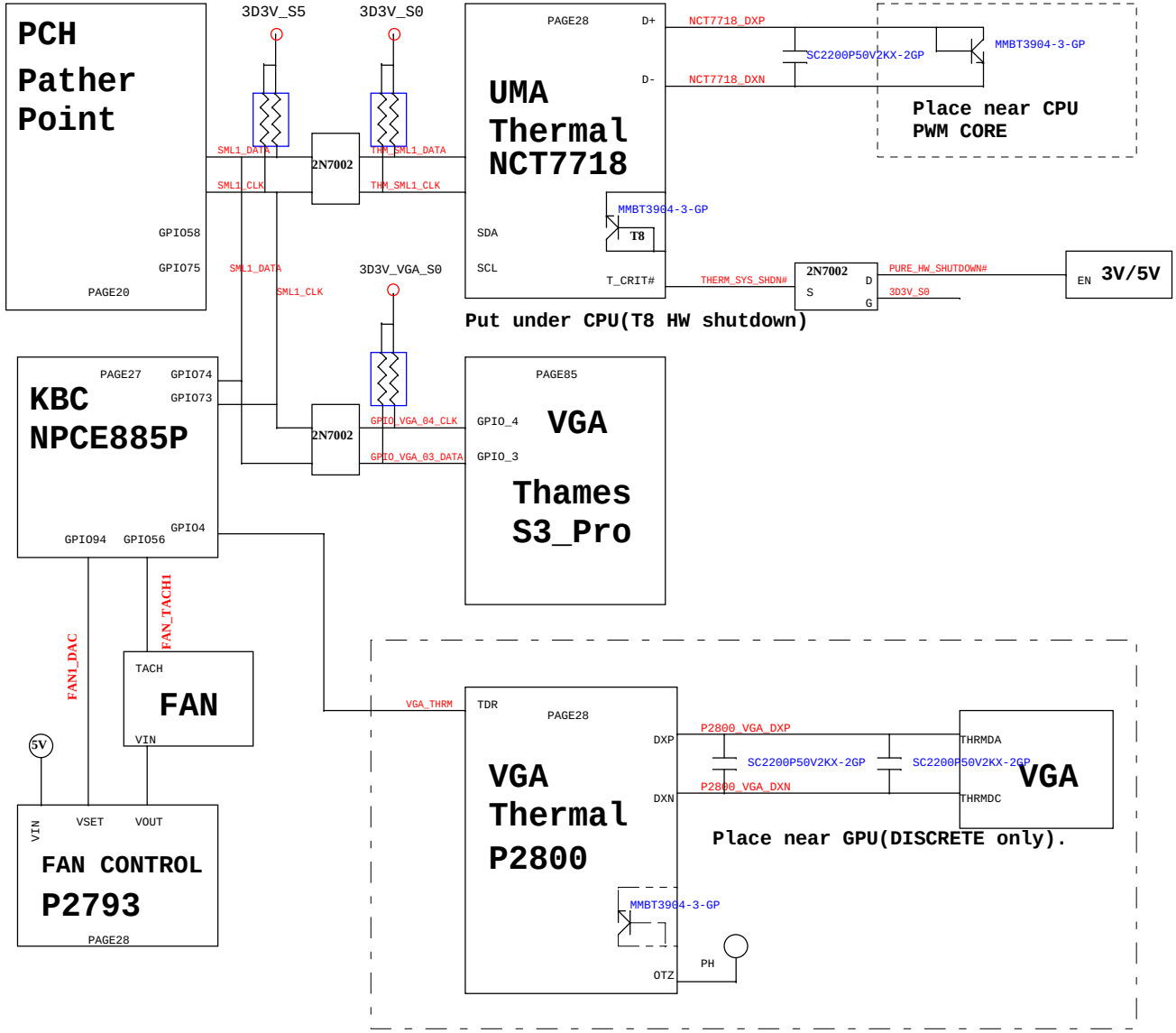
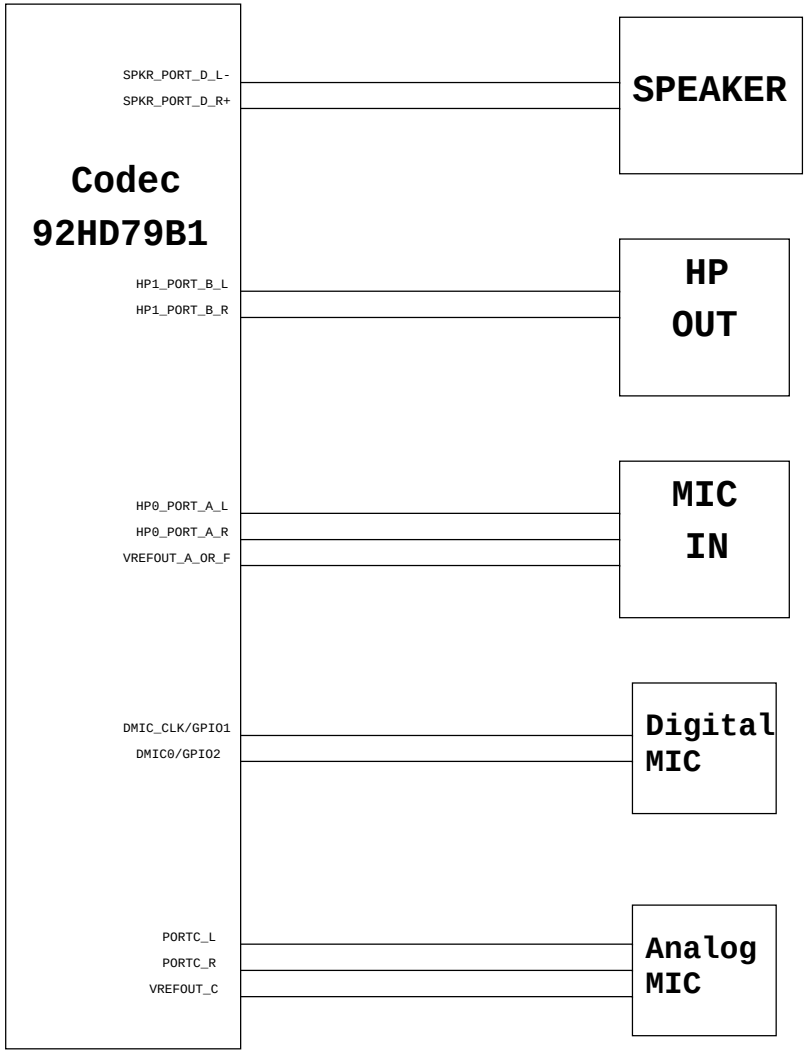
Thermal Block Diagram



Audio Block Diagram



<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

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VERSION	DATA	PAGE	Change Iteam
X01	11/03	92	change PU9201 pin24 from 5V_S0 to 5V_S5 to avoid 5V_S0 leakage issue
	11/03	92	change PR9219 from 10K to 0ohm and DY PC9201 to adjust VGA_CORE sequence
	11/03	93	change PR9314 from 470 ohm to 220ohm to adjust 3D3V_VGA_S0 power down sequence
	11/08	40	change PC4010 from 78.47422.2QL to 78.47422.2BL to correct wistron Part number
	11/08	86	change VGA strap pin follow NV FAE suggest
	11/08	42	change PR4120 from 10K to 9.76K to adjust 5V_S5 from 5.0V to 5.07V
	11/09	36	change R3605 from 10K to 0 ohm,R3607 and R3630 from 10K to 100K, C3610 from 0.01 uF to 0.047 uF to adjust 3D3V_S0, 5V_S0 and 1D5V_S0 power sequence
	11/09	17	change RN1703 from 33 ohm to 22 ohm to solve CRT HSYNC and VSYNC rise and fail time issue
	11/09	50	change L5001 L5002 L5003 to 68.00084.931 to solve CRT RGB rise and fall time fail issue
	11/09	40 38 97	stuff EC4002,EC9709,EC9701,EC9705,EC9708,EC9702,EC9703,EC9704,EC9738,EC9710,EC4001, EC9707,EC9713,EC9715,EC9716,EC9720,EC9718,EC9712,EC9714,PC4120,EC9717,EC9719, EC9722,PC3801,EC9706,SPR1,SPR3,SPR4 for EMI request
	11/09	27	change R2724 from 10K to 20K for PCB version change
	11/09	86	change ROM_SLK_D4 to SMB_ALT_ADDR follow NV Design Guide
	11/09	86	change ROM_SO_C4 to VGA_DEVICE follow NV Design Guide
	11/09	86	change ROM_SI_D3 to SUB_VENDOR follow NV Design Guide
	11/09	86	change STRAP0_STRAP3 to RAM_CFG[0]_RAM_CFG[3] follow NV Design Guide
	11/09	86	change STRAP4 to PCIE_MAX_SPEED follow NV Design Gide
	11/10	22 83	dummy R8319 R8307 R2205 stuff U8301 and add R2202 to pull high DGPU_HOLD_RST# to 3D3V_S0 follow NV FAE suggest
	11/10	21	seperate RN2203 to R2205 and R2206 for bom control
	11/11	41	change PR4102 from 51K to 61.9K to set 5V OCP
	11/11	41	change PR4101 from 120K to 91K to set 3.3V OCP
	11/11	42	change PR4236 from 1.78K to 2.05K for CPU Loadline adjustment
	11/11	42	change PR4264 from 20K to 18.2K for CPU Loadline adjustment
	11/11	42	change PR4239 from 0 ohm to 191 ohm for GFX Loadline adjustment
	11/11	42	change PR4249 from 7.87K to 7.5K for GFX Loadline adjustment
	11/11	46	change PR4602 from 52.3K to 80.6K to Set 1.5V OCP
	11/11	92	change PR9238 from 133K to 196K and PR9225 from 3.83K to 2.26K for Loadline adjustment follow Nvidia SPEC
	11/11	45	dummy PR4506 and PR4507, Pop PR4505 and 3D3V_S0 change 3D3V_S5 for power team request
	11/11	29	install R2909,R2910,D2902 as to audio chip will change to 4213D
	11/14	92	change PC9213 PC9214 PC9216 to 78.10622.51L for power team request
	11/15	29	change R2909 R2910 to 0 ohm for vendor request
	11/15	61 82	stuff TR8201 TR8202 TR6101,dummy R6102 R6203 R8201 R8202 R8203 R8204 for EMI request
	11/16	39	add test point AFTP3902

VERSION	DATA	PAGE	Change Iteam
X01	11/16	31	change C3102 C3103 to 15pF for vendor suggest
	11/16	86	change C8610 C8611 to 10pF for vendor suggest
	11/23	88 89	change R8807 R8908 from 80.6 ohm to 162 ohm for NV FAE suggest
	11/24	83	change L8302 to 0 ohm for NV FAE suggest
X02	12/16	20	reserve R2005 10K Pull High for PEG-CLKREQ#_L
	12/16	29	change R2945 to 2.2K,accuracy 'J' follow vendor suggestion to solve internal mic too low issue
	12/22	88	DY C8815 C8816,stuff C8809 to avoid HDD interfere.
	12/23	22	DY R2202,stuff R2205 to pull low DGPU_HOLD_RST# to follow NV Design Guide
	12/23	20 83	DY R2004,stuff R2005 to pull high PEG_CLKREQ# to 3D3V_S5,stuff R8302 to pull high VGA_PEG_CLKREQ#,stuff Q8301 follow NV suggestion
	12/27	28	exchange the name of AFTP2801 and AFTP2802 to stay same with UMA for AFTP request
	12/28	40	add 0.1uF caps EC4004(BT+_R to GND) and EC4003(PWR_DCBATOUT_CHG to GND) to reduce EMI noise
	12/28	27	change R2724 from 20K to 33K for PCB version change
	12/29	88	remove C8815 to avoid HDD interfere follow NV suggestion
	12/29	32 51 65	changed R3206,R3207 to short pad,removed TR3201 CMC footprint;changed R5101,R5102,R5103, R5104,R5105,R5106,R5107,R5108 to short pad,removed TR5101,TR5102,TR5103,TR5104,CMC footprint;changed R6505,R6506 to short pad,removed TR6501 CMC footprint follow EMI suggestion
	12/29	5 14 15 18 19 23 24 27 28 29 31 32 36 37 44 46 51 65 68 83 86	change R504 R1404 R1405 R1503 R1504 R1807 R1906 R1910 R1912 R1913 R1924 R1929 R2306 R2307 R2308 R2402 R2403 R2404 R2720 R2723 R2733 R2761 R2764 R2765 R2766 R2767 R2768 R2778 R2792 R2794 R2807 R2813 R2905 R2906 R3105 R3208 R3605 R3614 R3708 R3710 R5101 R5102 R5103 R5104 R5105 R5106 R5107 R5108 R5125 R6505 R6506 R6510 R6511 R6804 R6805 R6811 R6813 R8503 R8607 / L8302 L8601 R2304 R2412 R3104 R3115 R3117 R3206 R3207 R4908 / R2301 R2911 R2912 / RN2010 RN2012 RN2014 RN2016 RN5002 / PR4212 PR4116 PR4121 PR4127 PR4252 PR4254 PR4251 PR4250 PR4261 PR4220 PR4232 PR4244 PR4304 PR4305 PR4403 PR4611 PR4607 from 0ohm to short pad
	12/29	58	change EC5801 EC5802 EC5803 EC5804 to 1000P cap for EMI request
	12/30	29	add 100K R2913 resistor in AUD_PC_BEEP let voltage can be discharged fast
	12/30	61 82	remove R6102,R6103;R8201,R8202;R8203,R8204 co-lay position;use CMC solution
	12/30	27	change R2735 from 10K to 20K to reduce inrush current of 3D3V_AUX_KBC
	12/30	41	change PC4126,PC4127 to 4.7u from 10u follow power team's suggestion
	12/30	27 86	remove TP2713,add R2713 for pull high OVER_CURRENT_P8# to 3D3V_AUX_KBC;add R8608,Q8603; change Q8603.2 to OVER_CURRENT_P8# from AC_PRESENT for OC trigger IPCC function
	12/30	58	stuff 1000pf EC5801 EC5802 EC580 EC5804 for EMI request
	01/03	49	remove R4903,R4904 co-lay position;use CMC solution
	01/03	45	change PR4510 to 82.5K from 69.8K to modify OCP follow power team's suggestion

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02

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VERSION	DATA	PAGE	Change Iteam

VERSION	DATA	PAGE	Change Iteam

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