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UMA & Optimus Schematics Document

Sandy Bridge

Intel PCH

2010-10-27

REV : -1

DY :None Installed
UMA:UMA platform installed
OPS:Optimus

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

Size: A3 | Document Number: LA470 | Rev: -1

Date: Thursday, December 16, 2010 | Sheet 1 of 97

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Block Diagram (UMA/Optimus co-lay)

##OnMainBoard

POWER BD

Finger Printer BD

IO BD (Cardreader+Audio+USB)

LED BD

USB

VRAM 2GB/1GB/512MB 88,89,90,91

DDR3 800MHz

NVIDIA N12P-GE/GV N12M-GE 83.84,85,86,87

PCIe x 16 (Discrete only)

Intel CPU

Sandy Bridge

DDRIII: 1066/1333/1666 MHz

4,5,6,7,8,9,10

DDRIII 1066/1333/1666 Channel A

DDRIII 1066/1333/1666 Channel B

DDRIII Slot 0 1066/1333/1666 14

DDRIII Slot 1 1066/1333/1666 15

Project code : 91.4KZ01.001
PCB P/N : 48.4KZ01.011
Revision : 10250-1

HDMI 51

LCD 49

CRT 50

FDI x 4 x 2 (UMA only)

DMI x 4

HDMI

LVDS

RGB CRT

Intel PCH Cougar Point

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1

17,18,19,20,21,22,23,24,25

Bluetooth 63

CAMERA 49

Finger Print BD

Finger Print 64

I/O BD

SD/MMC+/MS/ MS Pro/xD 74

CardReader Realtek RTS5139

USB2.0 x 3

USB 2.0 x 1

AZALIA

PCIE x 1

GLAN RTL8111E 31

RJ45 CONN 59

PCIE x 1/USB2.0 x 1

Mini-Card WLAN 65

SATA x 1/USB2.0 x 1

Mini-Card WWAN 66

SIM 66

USB 2.0 x 3

MB USB x 3

USB 2.0 x 1/SATA x 1

E-SATA/USB comb 57

SATA x 2

HDD 56

ODD 56

Internal DMIC

HP1

MIC IN

I/O BD

Azalia CODEC Codec_ALC272 29

2CH SPEAKER

SPI

Flash ROM 4MB 60

LPC Bus

LPC debug port 71

KBC NUVOTON NPCE795G 27

SMBus

G-Sensor 79

Touch PAD 69

Int. KB 69

Thermal EMC2103-2-AP 28

Fan 28

SYSTEM DC/DC RT8208A 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC NCP6131 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51123 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51218 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208A 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC RT8015B 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9091-180T11U 24,93	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S5
3D3V_S0	1D8V_VGA_S0

LDO RT9026 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

<Variant Name>

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Title: Block Diagram

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

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Name	Schematics Notes
SPKR	**Reboot option at power up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Variant Name>

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Title: Table of Content

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SSID = CPU

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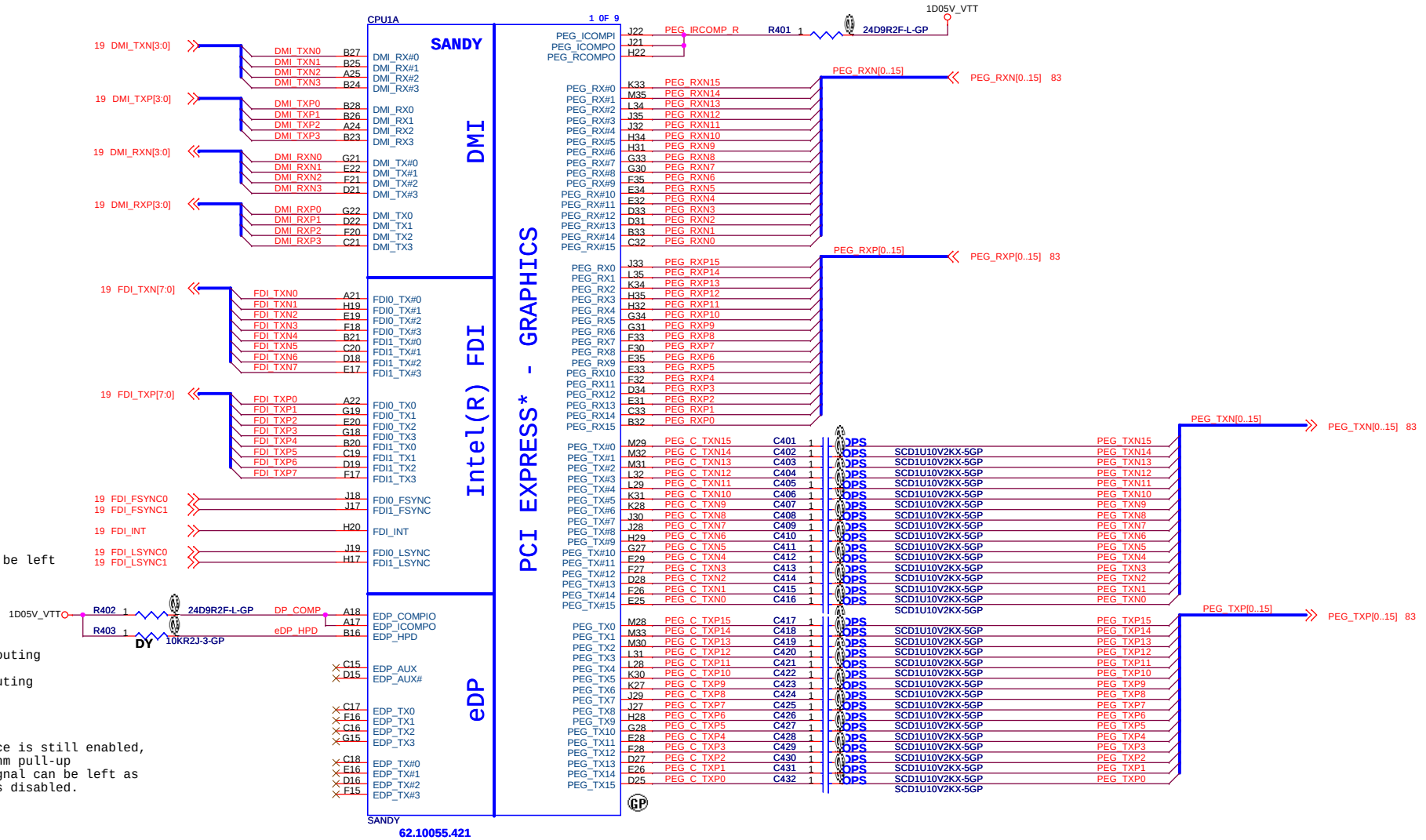
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
EDP_ICOMPO and EDP_COMPIO should not be left floating.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-k ohm pull-up resistor on the motherboard. This signal can be left as no connect if entire eDP interface is disabled.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

<Variant Name>

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Title	CPU (PCIE/DMI/FDI)
Size A3 / Document Number	LA470 / Rev -1
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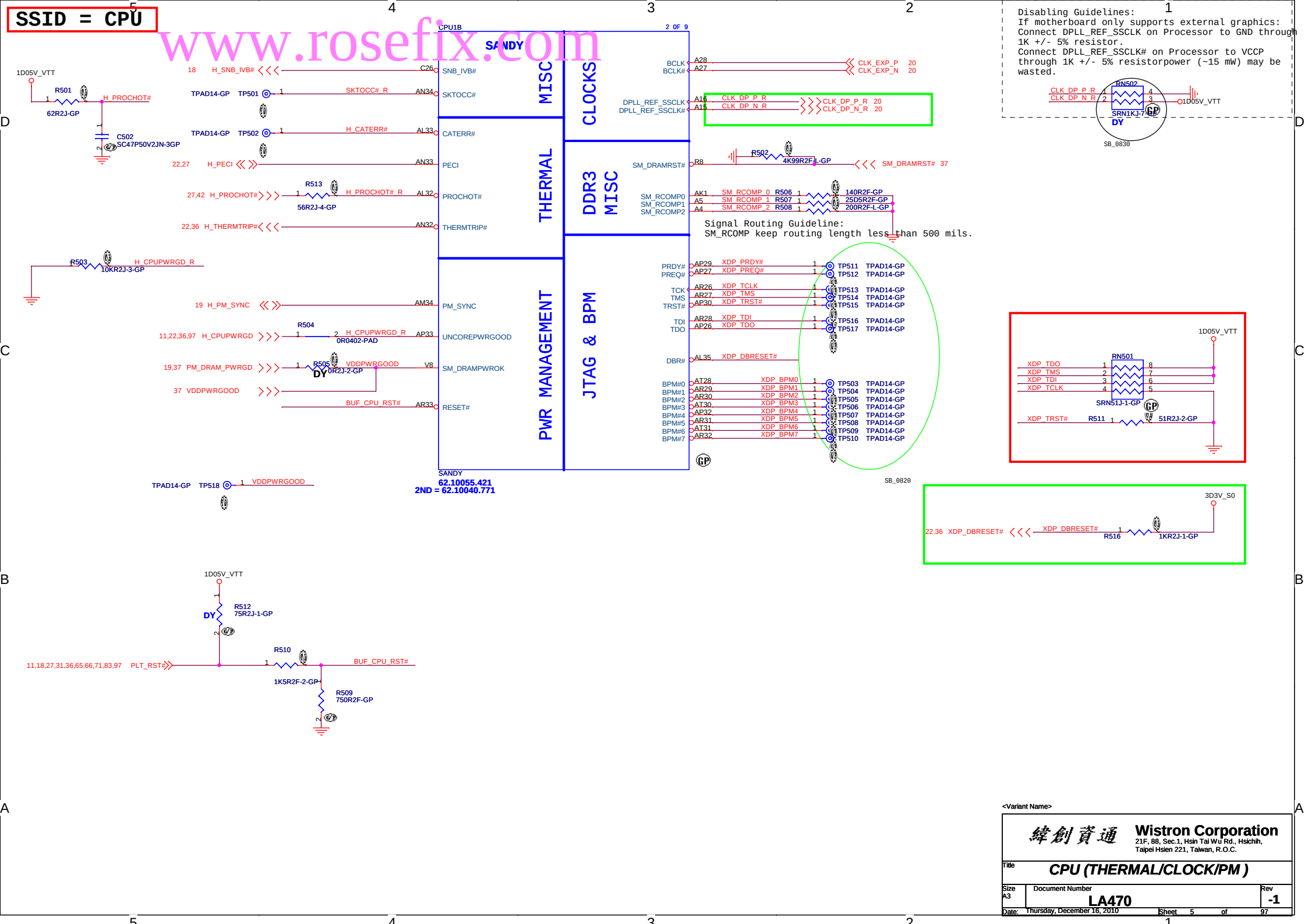
SSID = CPU
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CPU1B
2 OF 9
SANDY
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
SANDY
62.10055.421
2ND = 62.10040.771
SB_0820
Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.
SB_0830
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.
1D05V_VTT
R501
62R2J-GP
H_PROCHOT#
C502
SC47P50V2JN-3GP
18 H_SNB_IVB#
TPAD14-GP TP501
SKTOCC# R
TPAD14-GP TP502
H_CATERR#
22,27 H_PECI
27,42 H_PROCHOT#
R513
56R2J-4-GP
H_PROCHOT# R
22,36 H_THERMTRIP#
R503
10KR2J-3-GP
H_CPUPWRGD_R
19 H_PM_SYNC
11,22,36,97 H_CPUPWRGD
R504
0R0402-PAD
19,37 PM_DRAM_PWRGD
R505
0R2J-2-GP
VDDPWRGOOD
37 VDDPWRGOOD
BUF_CPU_RST#
TPAD14-GP TP518
VDDPWRGOOD
BCLK
BCLK#
CLK_EXP_P 20
CLK_EXP_N 20
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
CLK_DP_P_R
CLK_DP_N_R
CLK_DP_P_R 20
CLK_DP_N_R 20
SM_DRAMRST#
R502
4K99R2F-L-GP
SM_DRAMRST# 37
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
SM_RCOMP_0 R506 140R2F-GP
SM_RCOMP_1 R507 25D5R2F-GP
SM_RCOMP_2 R508 200R2F-L-GP
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
XDP_PRDY#
XDP_PREQ#
XDP_TCLK
XDP_TMS
XDP_TRST#
XDP_TDI
XDP_TDO
XDP_DBRESET#
TP511 TPAD14-GP
TP512 TPAD14-GP
TP513 TPAD14-GP
TP514 TPAD14-GP
TP515 TPAD14-GP
TP516 TPAD14-GP
TP517 TPAD14-GP
BPM#0
BPM#1
BPM#2
BPM#3
BPM#4
BPM#5
BPM#6
BPM#7
XDP_BPM0
XDP_BPM1
XDP_BPM2
XDP_BPM3
XDP_BPM4
XDP_BPM5
XDP_BPM6
XDP_BPM7
TP503 TPAD14-GP
TP504 TPAD14-GP
TP505 TPAD14-GP
TP506 TPAD14-GP
TP507 TPAD14-GP
TP508 TPAD14-GP
TP509 TPAD14-GP
TP510 TPAD14-GP
RN501
SRN51J-1-GP
XDP_TDO
XDP_TMS
XDP_TDI
XDP_TCLK
XDP_TRST#
R511
51R2J-2-GP
3D3V_S0
22,36 XDP_DBRESET#
R516
1KR2J-1-GP
R512
75R2J-1-GP
11,18,27,31,36,65,66,71,83,97 PLT_RST#
R510
1K5R2F-2-GP
R509
750R2F-GP
<Variant Name>
Wistron Corporation
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Title
CPU (THERMAL/CLOCK/PM)
Size A3
Document Number
LA470
Rev -1
Date: Thursday, December 16, 2010
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SSID = CPU

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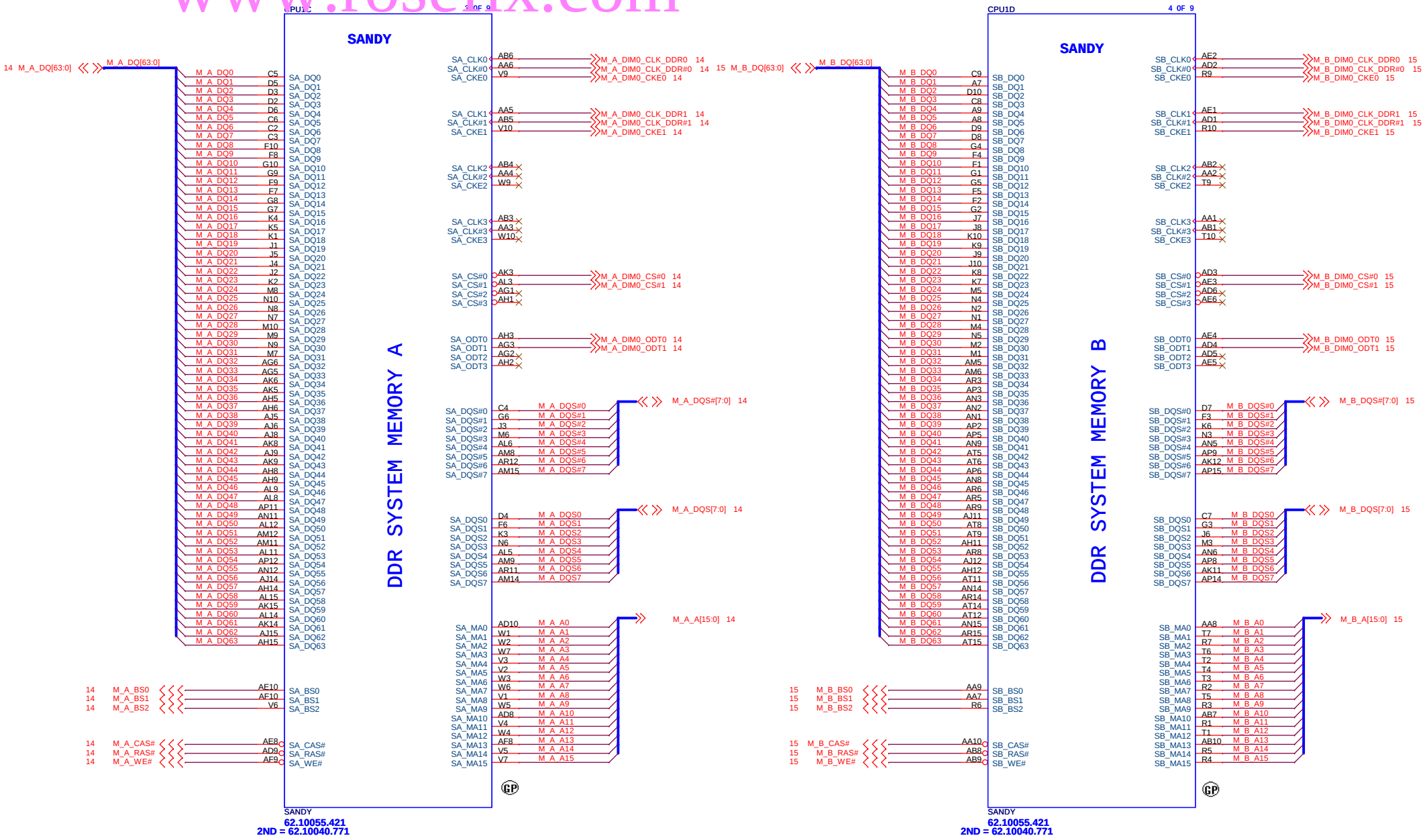

<Variant Name>

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Title: CPU (DDR)

Size	Document Number	Rev
A3	LA470	-1

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SSID = CPU

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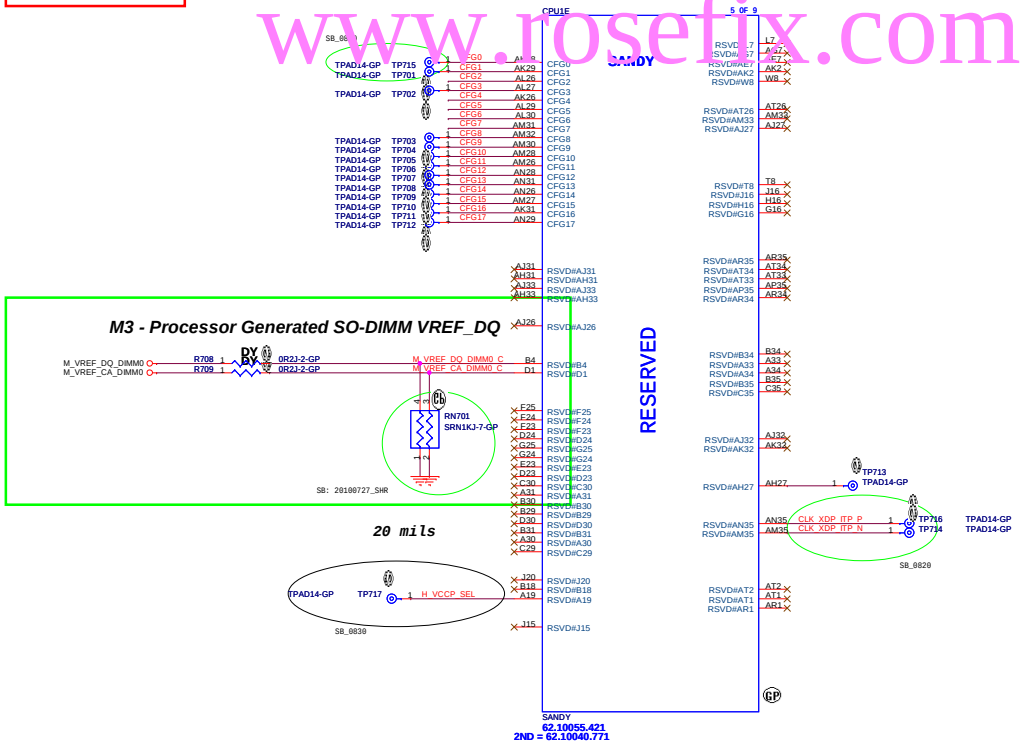
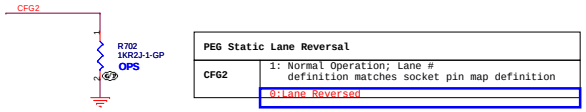
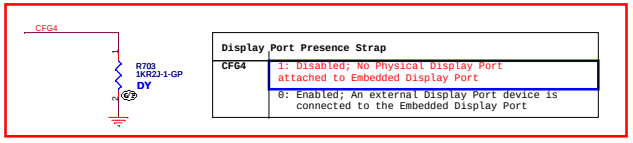
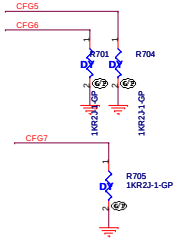




PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

<Variant Name>

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Title: CPU (RESERVED)

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SSID = CPU

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POWER

PROCESSOR CORE POWER

53A

VCC_CORE

C801 SC10U6D3V5KX-1GP
C802 SC10U6D3V5KX-1GP
C803 SC10U6D3V5KX-1GP
C804 SC10U6D3V5KX-1GP
C811 SC10U6D3V5KX-1GP

C815 SC10U6D3V5KX-1GP
C817 SC10U6D3V5KX-1GP
C818 SC10U6D3V5KX-1GP
C819 SC10U6D3V5KX-1GP
C820 SC10U6D3V5KX-1GP

C816 SC10U6D3V5KX-1GP
C821 SC10U6D3V5KX-1GP
C822 SC10U6D3V5KX-1GP
C823 SC10U6D3V5KX-1GP
C824 SC10U6D3V5KX-1GP
C825 SC10U6D3V5KX-1GP
C826 SC10U6D3V5KX-1GP
C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP
C836 SC10U6D3V5KX-1GP
C835 SC10U6D3V5KX-1GP
C834 SC10U6D3V5KX-1GP
C833 SC10U6D3V5KX-1GP
C832 SC10U6D3V5KX-1GP
C831 SC10U6D3V5KX-1GP
C828 SC10U6D3V5KX-1GP

VCC_CORE

CPU1F

6 OF 9

SANDY

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26
AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26
AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26
AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26
AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26
Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26
V35 V34 V33 V32 V31 V30 V29 V28 V27 V26
U35 U34 U33 U32 U31 U30 U29 U28 U27 U26
R35 R34 R33 R32 R31 R30 R29 R28 R27 R26
P35 P34 P33 P32 P31 P30 P29 P28 P27 P26
— all VCC

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 F14 E12
VCCIO: E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11
VCCIO: J23

1D05V_VTT

C805 C806 C807 C808 C809 C810 C838 C839 C840 C841 — SC10U6D3V5KX-1GP

1D05V_VTT

C812 C813 C814 C829 C830 C842 C843 C844 C845 — SC10U6D3V5KX-1GP

R804 need to close to CPU

1D05V_VTT

SB_0819

H_CPU_SVIDDAT_R R804 1 130R2F-1-GP

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 1 43R2J-GP
VIDSCLK AJ30 H_CPU_SVIDCLK_R R805 1 2 0R0402-PAD
VIDSOUT AJ28 H_CPU_SVIDDAT_R R806 1 2 0R0402-PAD

VR_SVID_ALERT# 42
H_CPU_SVIDCLK 42
H_CPU_SVIDDAT 42

VCC_CORE

R801, R802 need to close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE AJ35
VSS_SENSE AJ34

VCCSENSE 42
VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10
VSSIO_SENSE A10

VCCIO_SENSE 45
VSSIO_SENSE 45

SANDY
62.10055.421
2ND = 62.10040.771

<Variant Name>

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: LA470 | Rev: -1

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SSID = CPU

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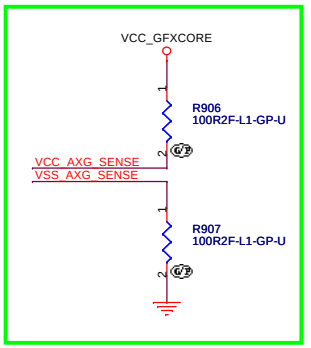
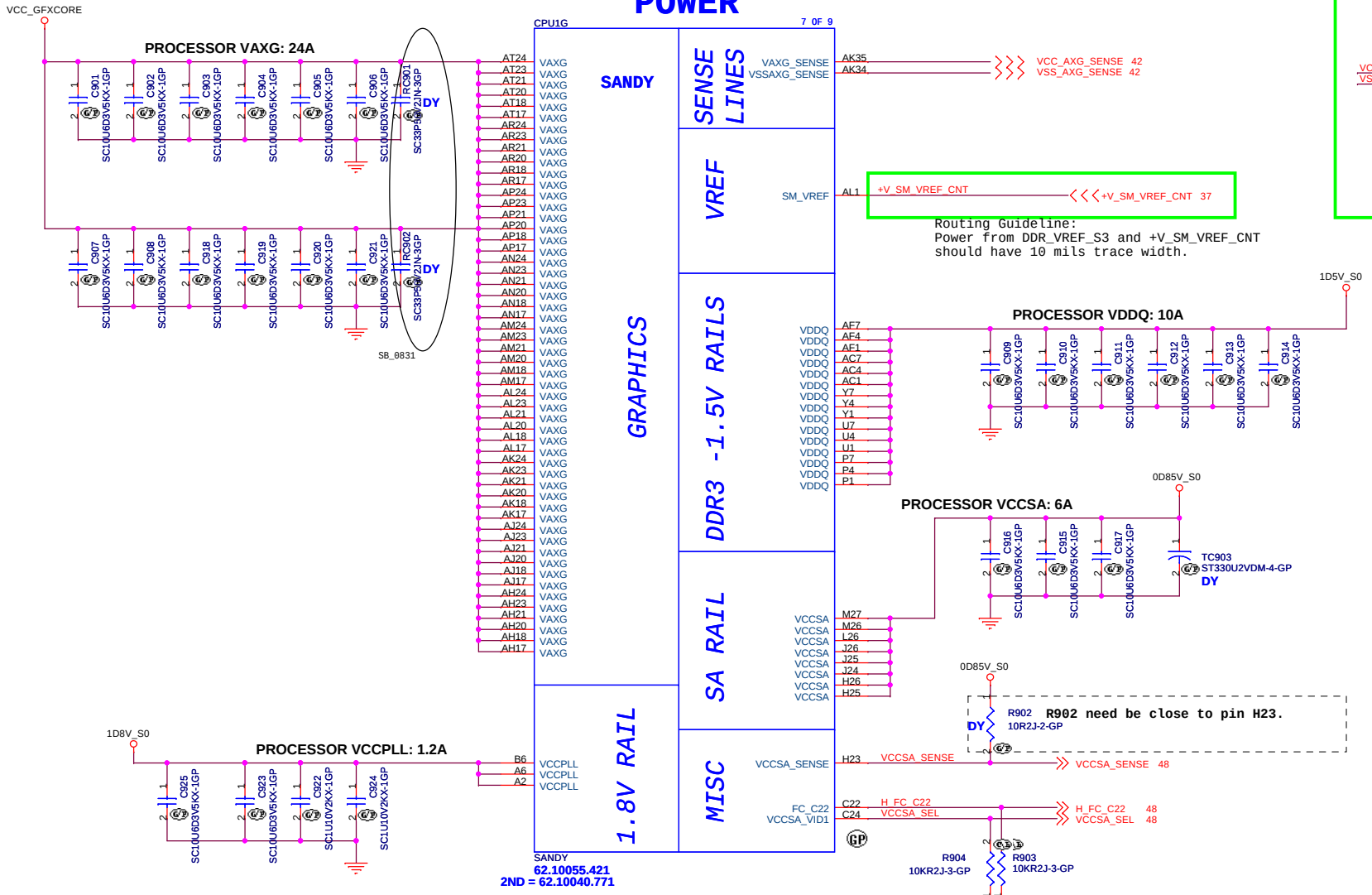
POWER

Close to CPU





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VCC_GFXCORE)	
Size A3	Document Number LA470	Rev -1
Date: Thursday, December 16, 2010	Sheet 9 of 97	

SSID = CPU

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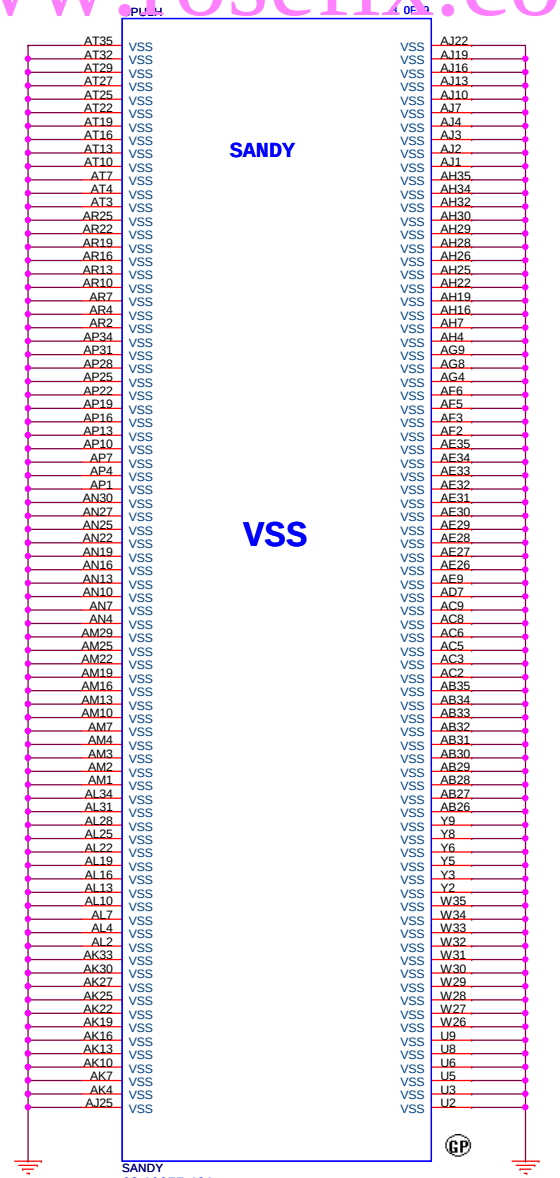

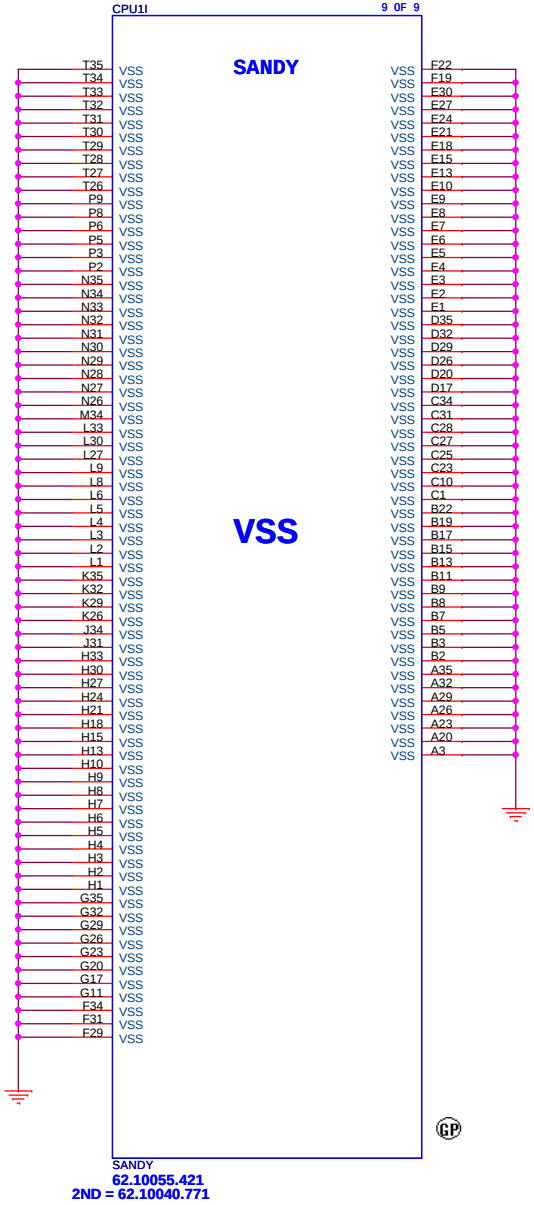

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VSS)	
Size A3	Document Number LA470	Rev -1
Date: Thursday, December 16, 2010	Sheet 10 of 97	

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***XDP***		
Size: A3	Document Number: **LA470**	Rev: **-1**
Date: Thursday, December 16, 2010	Sheet 11 of 97	

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(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, December 16, 2010 Sheet 12 of 97

www.rosefix.com

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, December 16, 2010 Sheet 13 of 97

SSID = MEMORY

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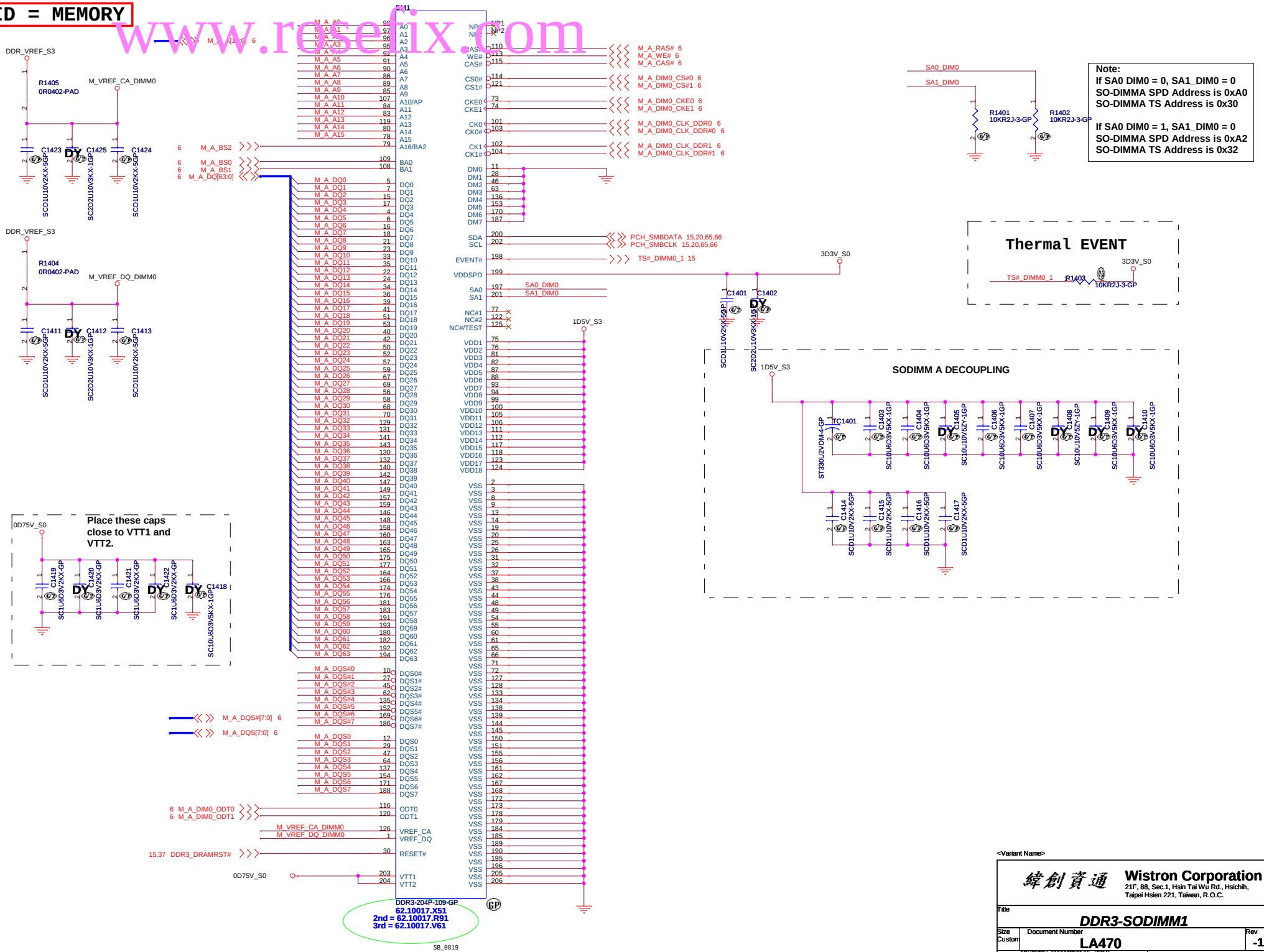

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM1***

Size	Document Number	Rev
Custom	LA470	-1

Date: Thursday, December 16, 2010 Sheet 14 of 97

SSID = MEMORY

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DM2

M_B_A[15:0] 6

M_B_BS2 6

M_B_BS0 6
M_B_BS1 6
M_B_DQ[63:0] 6

M_B_DQS#[7:0] 6

M_B_DQS[7:0] 6

M_B_DIM0_ODT0 6
M_B_DIM0_ODT1 6

M_VREF_CA_DIMM0
M_VREF_DQ_DIMM0

14,37 DDR3_DRAMRST#

0D75V_S0

M_VREF_CA_DIMM0

C1523 SCD1U10V2KX-5GP
DY C1524 SC22D2U10V3KX-1GP
C1522 SCD1U10V2KX-5GP

Place these caps close to VTT1 and VTT2.

0D75V_S0
DY C1518 SC1U6D3V2KX-GP
C1519 SC1U6D3V2KX-GP
DY C1520 SC1U6D3V2KX-GP
C1521 SC1U6D3V2KX-GP

M_B_RAS# 6
M_B_WE# 6
M_B_CAS# 6

M_B_DIM0_CS#0 6
M_B_DIM0_CS#1 6

M_B_DIM0_CKE0 6
M_B_DIM0_CKE1 6

M_B_DIM0_CLK_DDR0 6
M_B_DIM0_CLK_DDR#0 6

M_B_DIM0_CLK_DDR1 6
M_B_DIM0_CLK_DDR#1 6

PCH_SMBDATA 14,20,65,66
PCH_SMBCLK 14,20,65,66

TS#_DIMM0_1 14

SA0_DIM1
SA1_DIM1

1D5V_S3

3D3V_S0

R1501 10KR2J-3-GP
R1502 10KR2J-3-GP

SA1_DIM1
SA0_DIM1

DY C1501 SCD1U10V2KX-5GP
C1502 SC2D2U10V3KX-1GP

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

SODIMM B DECOUPLING

1D5V_S3
DY C1503 SC10U10V5ZY-1GP
DY C1504 SC10U10V5ZY-1GP
C1505 SC10U6D3V5KX-1GP
C1506 SC10U6D3V5KX-1GP
C1507 SC10U6D3V5KX-1GP
DY C1508 SC10U10V5ZY-1GP
C1509 SC10U6D3V5KX-1GP
DY C1510 SC10U6D3V5KX-1GP

C1511 SC1U10V2KX-5GP
C1512 SC1U10V2KX-5GP
C1513
C1514 SC1U10V2KX-5GP

H = 8mm

DDR3-204P-108-GP
62.10017.X41
2nd = 62.10017.M51
3rd = 62.10017.V51

SB_0819

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
Custom	LA470	-1

Date: Thursday, December 16, 2010 Sheet 15 of 97

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR3-SODIMM2*

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, December 16, 2010 Sheet 16 of 97

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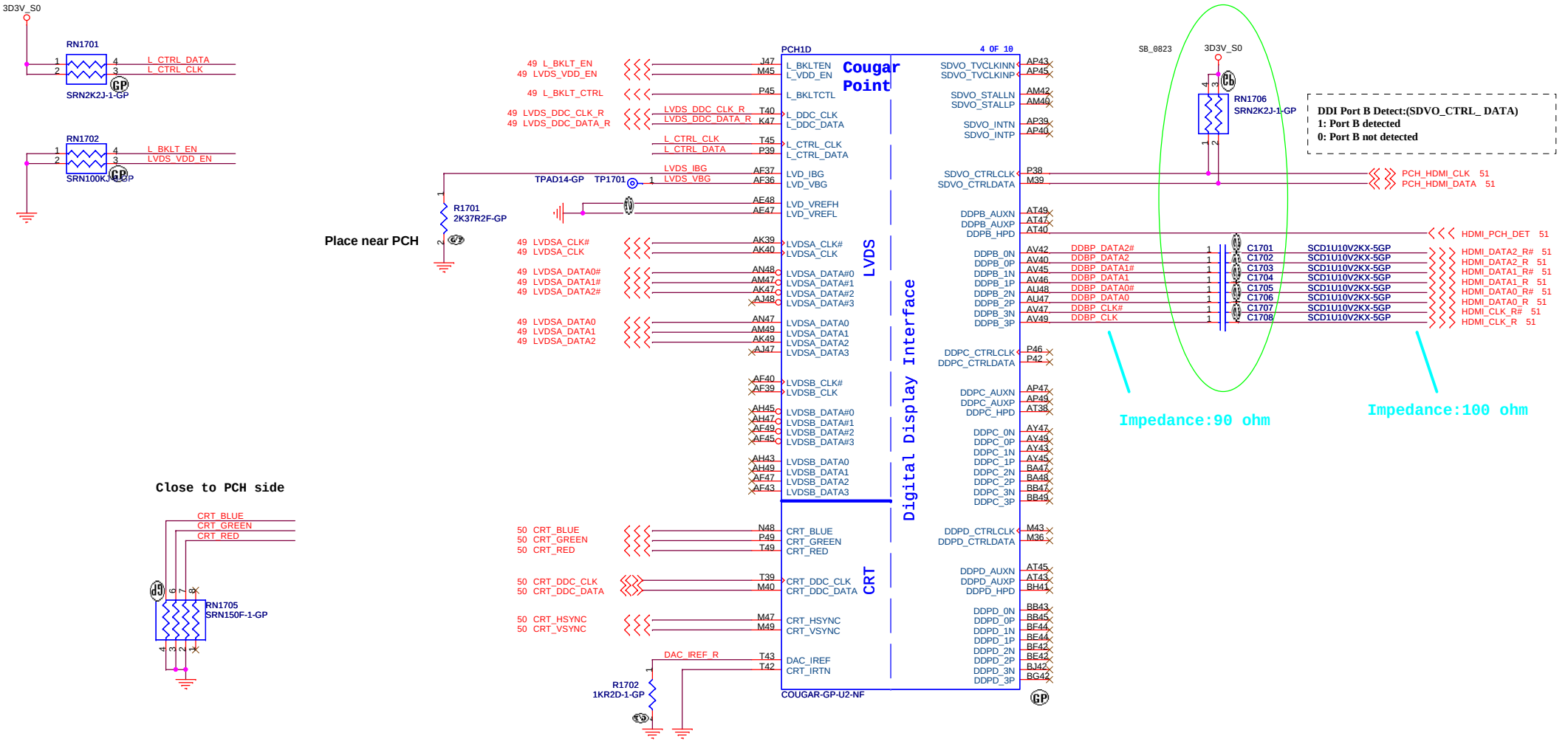

<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (LVDS/CRT/DDI)		
Size: A3	Document Number: LA470	Rev: -1
Date: Thursday, December 16, 2010	Sheet 17 of 97	

SSID = PCH

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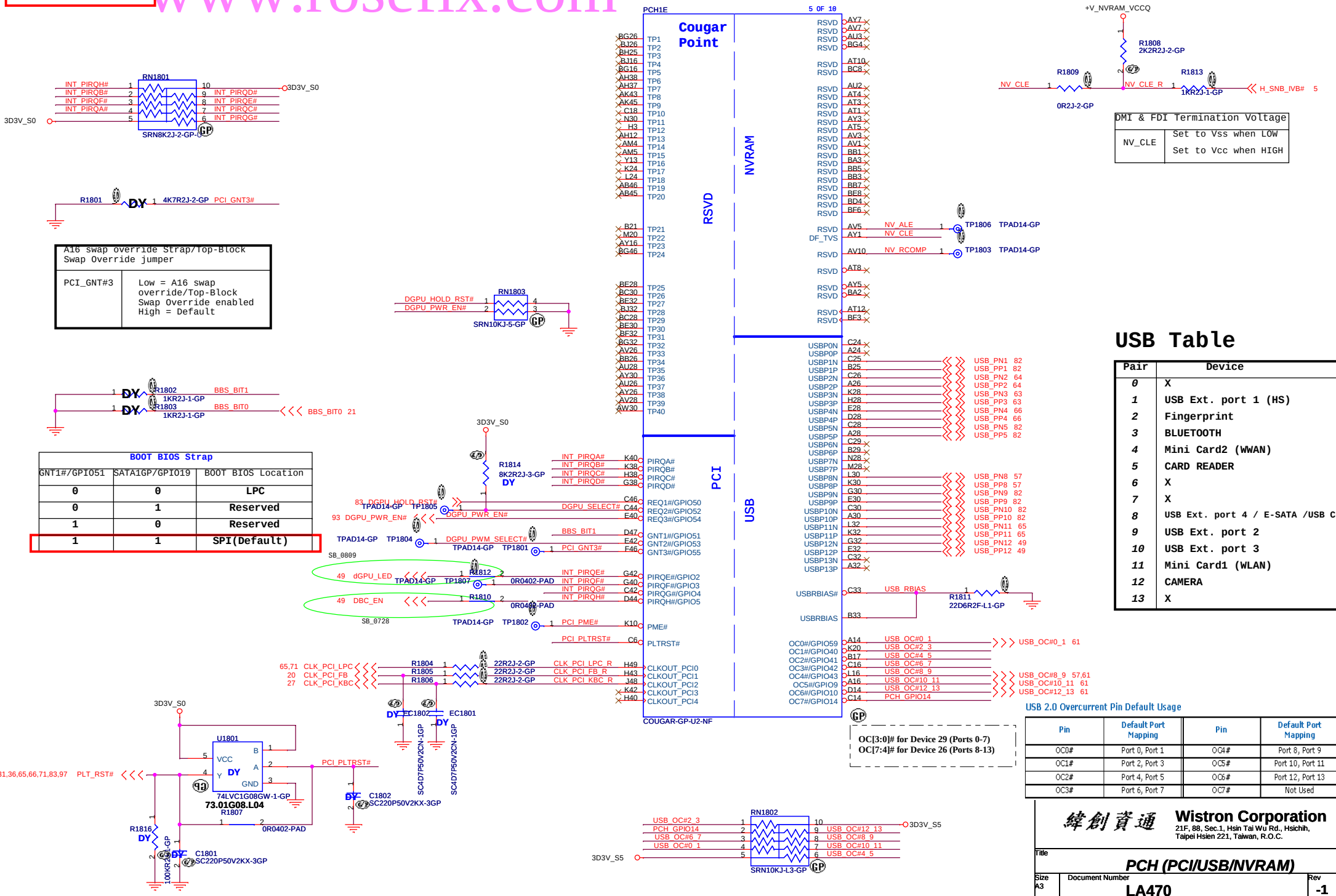


USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGE
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	X

USB 2.0 Overcurrent Pin Default Usage

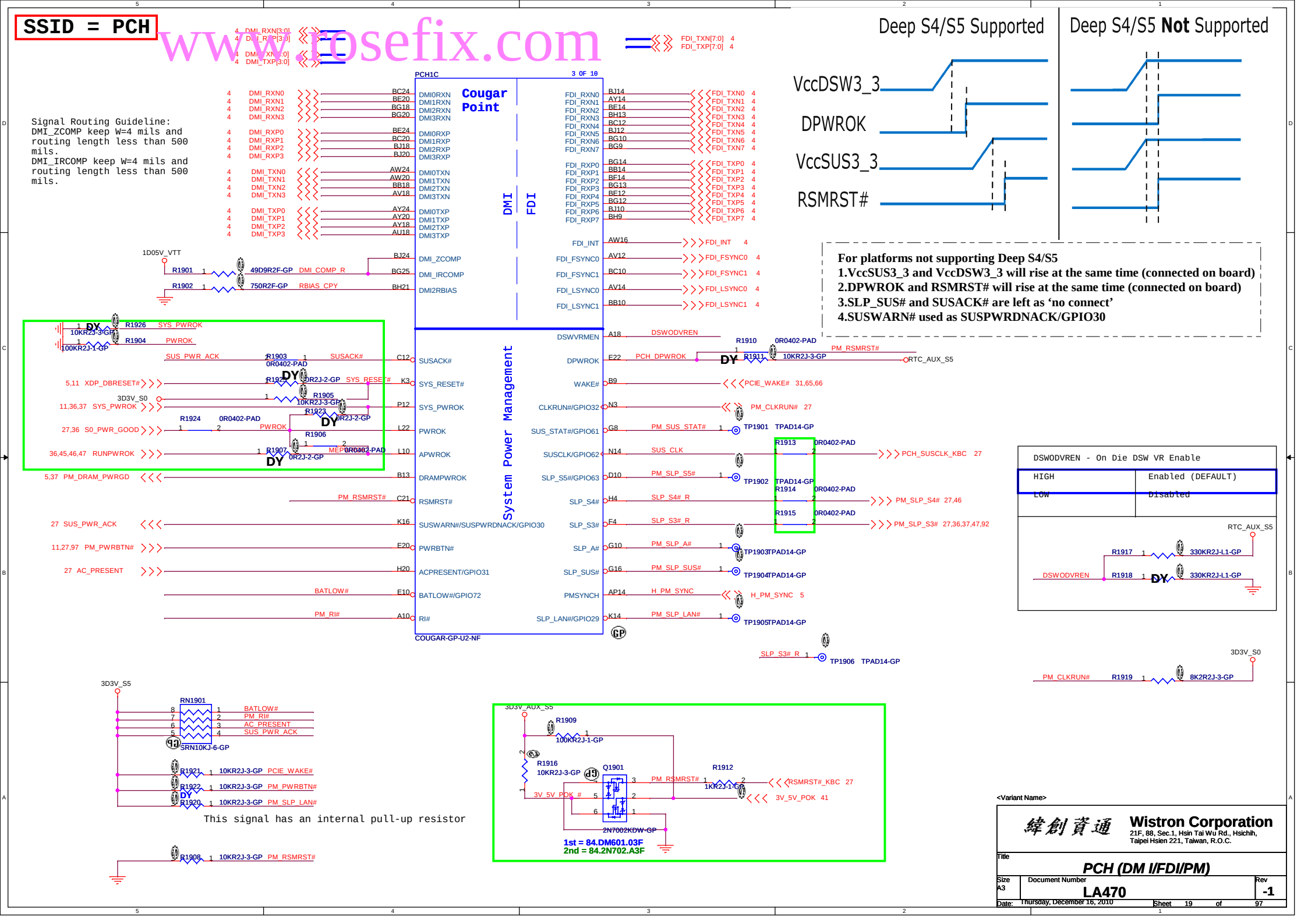
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size: A3 | Document Number: LA470 | Rev: -1

Date: Thursday, December 16, 2010 | Sheet 18 of 97


SSID = PCH
www.rosefix.com
Deep S4/S5 Supported
Deep S4/S5 Not Supported
VccDSW3_3
DPWROK
VccSUS3_3
RSMRST#
Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.
For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30
PCH1C
3 OF 10
Cougar Point
DMI
FDI
System Power Management
COUGAR-GP-U2-NF
DSWODVREN - On Die DSW VR Enable
HIGH
Enabled (DEFAULT)
LOW
Disabled
This signal has an internal pull-up resistor
1st = 84.DM601.03F
2nd = 84.2N702.A3F
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (DM I/FDI/PM)
Size A3
Document Number LA470
Rev -1
Date: Thursday, December 16, 2010
Sheet 19 of 97

SSID = PCH

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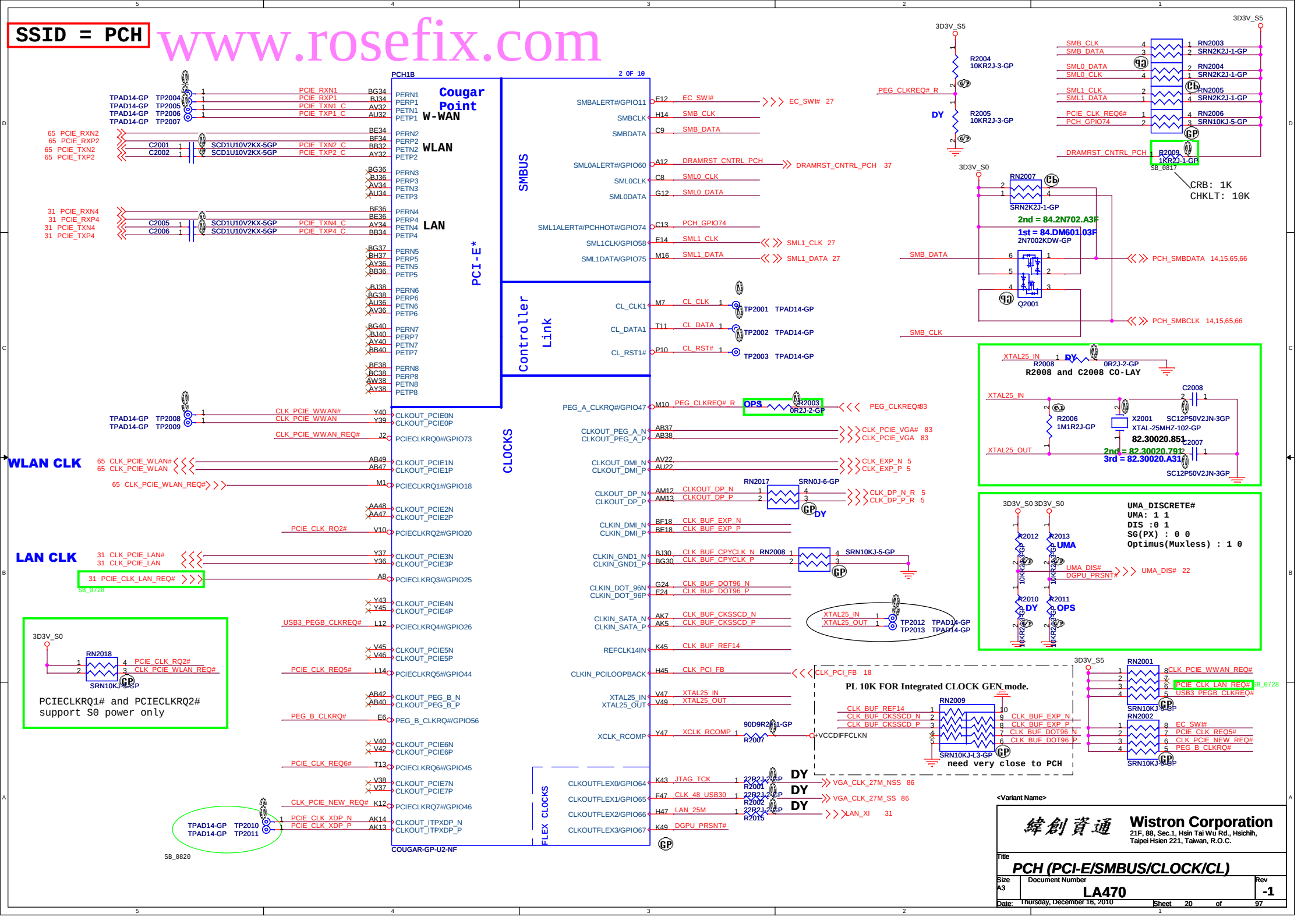

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A3 | Document Number: LA470 | Rev: -1

Date: Thursday, December 16, 2010 | Sheet 20 of 97

SSID = PCH

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INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

PCH1A — Cougar Point — 1 OF 10

RTC_X1 A20 — RTC_X2 C20 — RTC_RST# D20 — SRTC_RST# G22 — SM_INTRUDER# K22 — PCH_INTVRMEN C17 — RTC

HDA_BITCLK N34 — HDA_SYNC L34 — SPKR T10 — HDA_RST# K34 — HDA_SDIN0 E34 — HDA_SDIN1 G34 — HDA_SDIN2 C34 — HDA_SDIN3 A34 — HDA_SDO A36 — HDA_DOCK_EN#/GPIO33 C36 — HDA_DOCK_RST#/GPIO13 N32 — IHDA

JTAG_TCK J3 — JTAG_TMS H7 — JTAG_TDI K5 — JTAG_TDO H1 — JTAG

SPI_CLK T3 — SPI_CS0# Y14 — SPI_CS1# T1 — SPI_MOSI V4 — SPI_MISO U3 — SPI

LPC: FWH0/LAD0 C38 LPC_AD0 — FWH1/LAD1 A38 LPC_AD1 — FWH2/LAD2 B37 LPC_AD2 — FWH3/LAD3 C37 LPC_AD3 — FWH4/LFRAME# D36 LPC_FRAME# 27,65,71 — LDRQ0# E36 — LDRQ1#/GPIO23 K36 APS_LED_R 68 — SERIRQ V5 INT_SERIRQ 27

SATA 6G:
SATA0RXN AM3 / SATA0RXP AM1 / SATA0TXN AP7 SATA_TXN0_C C2105 / SATA0TXP AP5 SATA_TXP0_C C2106 — SCD01U16V2KX-3GP — SATA_RXN0_C 56 / SATA_RXP0_C 56 / SATA_TXN0 56 / SATA_TXP0 56 — HDD1
SATA1RXN AM10 / SATA1RXP AM8 / SATA1TXN AP11 SATA_TXN1_C C2112 / SATA1TXP AP10 SATA_TXP1_C C2111 — SCD01U16V2KX-3GP — SATA_RXN1_C 66 / SATA_RXP1_C 66 / SATA_TXN1 66 / SATA_TXP1 66 — SATA SSD
SATA2RXN AD7 / SATA2RXP AD5 / SATA2TXN AH5 / SATA2TXP AH4
SATA3RXN AB8 / SATA3RXP AB10 / SATA3TXN AF3 / SATA3TXP AF1
SATA4RXN Y7 / SATA4RXP Y5 / SATA4TXN AD3 SATA_TXN4_C C2109 / SATA4TXP AD1 SATA_TXP4_C C2110 — SCD01U16V2KX-3GP — SATA_RXN4_C 56 / SATA_RXP4_C 56 / SATA_TXN4 56 / SATA_TXP4 56 — ODD
SATA5RXN Y3 / SATA5RXP Y1 / SATA5TXN AB3 SATA_TXN5_C C2107 / SATA5TXP AB1 SATA_TXP5_C C2108 — SCD01U16V2KX-3GP — SATA_RXN5_C 57 / SATA_RXP5_C 57 / SATA_TXN5 57 / SATA_TXP5 57 — ESATA

Move Cap close to Device or Connector.

SATAICOMPO Y11 — SATAICOMPI Y10 SATA_COMP R2112 37D4R2F-GP 1D05V_VTT
SATA3RCOMPO AB12 — SATA3COMPI AB13 SATA3_COMP R2113 49D9R2F-GP 1D05V_VTT
SATA3RBIAS AH1 RBIAS_SATA3 R2114 806R2F-GP SB_0902
SATALED# P3 SATA_LED# 68
SATA0GP/GPIO21 V14 SATA_DET#0
SATA1GP/GPIO19 P1 BBS_BIT0 BBS_BIT0 18

COUGAR-GP-U2-NF

RTC_X1 — R2101 10MR2J-L-GP — RTC_X2 — X2101 X-32D768KHZ-34GPU — C2101 SC5D6P50V2CN-1GP — C2102 SC5D6P50V2CN-1GP

RN2104 SRN20KJ-GP-U — C2103 SC1U6D3V2KX-GP — C2104 SC1U6D3V2KX-GP — G2101 CAP-OPEN

RTC_AUX_S5 — R2104 1M1R2J-GP — R2105 330KR2F-L-GP

SHR_V1.4 SB_0809
29 HDA_CODEC_SYNC — R2122 33R2J-2-GP — HDA_SYNC
29 HDA_CODEC_SDOUT — R2123 33R2J-2-GP — HDA_SDOUT

29 HDA_CODEC_RST# — RN2102 SRN33J-5-GP-U — HDA_RST#
29 HDA_CODEC_BITCLK — HDA_BITCLK

+3VS_+1.5VS_HDA_IO — R2102 1KR2J-1-GP — HDA_SDOUT — DY

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

NO REBOOT STRAP

3D3V_S0 — R2106 1KR2J-1-GP — HDA_SPKR — DY

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

27 ME_UNLOCK — R2107 1KR2J-1-GP — HDA_SDOUT — TPAD14-GP TP2105 — PCH_GPIO33

TPAD14-GP TP2101 — PCH_JTAG_TCK_BUF
TPAD14-GP TP2102 — PCH_JTAG_TMS
TPAD14-GP TP2103 — PCH_JTAG_TDI
TPAD14-GP TP2104 — PCH_JTAG_TDO

27,60 SPI_CLK_R — R2108 33R2J-2-GP — PCH_SPI_CLK
27,60 SPI_CS0#_R — R2109 33R2J-2-GP — PCH_SPI_CS0#
27,60 SPI_SI_R — R2110 33R2J-2-GP — PCH_SPI_SI
27,60 SPI_SO_R

+3VS_+1.5VS_HDA_IO — R2103 1KR2J-1-GP — HDA_SYNC

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

3D3V_S0 — RN2103 SRN10KJ-GP
SATA_LED# — INT_SERIRQ — SATA_DET#0

SB_0817
PCH_JTAG_TCK_BUF — R2121 4K7R2J-2-GP
PCH_GPIO33 — R2125 1KR2J-1-GP — DY

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: A3 | Document Number: LA470 | Rev: -1
Date: Thursday, December 16, 2010 | Sheet 21 of 97

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SSID = PCH

Note
For PCH debug with XDP, need to NC STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

3D3V_S0 — R2202 1 — 200KR2F-L-GP — SATA_ODD_PRSNT#

20100625 V1.2

3D3V_S0 — RN2203 — H_A20GATE, H_RCIN# — SRN10KJ-5-GP

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

3D3V_S0 — R2224 10KR2J-3-GP — PCH_TEMP_ALERT#
PCH_GPIO27 — DY R2223 10KR2J-3-GP
DY R2225 10KR2J-3-GP

3D3V_S0 — RN2201 — PSW_CLR#, DGPU_HPD_INTR#, EC_SCI# — SRN10KJ-8-GP

RN2202 — MFG_MODE, S_GPIO, EC_SCI#, PCH_GPIO22 — SRN10KJ-8-GP
PCH_GPIO48 — R2227 10KR2J-3-GP

3D3V_S5 — RN2205 — PCH_GPIO12, USB3_PWR_ON — SRN10KJ-8-GP

PCH_GPIO15 — R2201 1KR2J-1-GP
PCH_GPIO24 — R2221 10KR2J-3-GP
20100625 V1.2
PLL_ODVR_EN — R2226 10KR2J-3-GP

NC_FP_DET# — R2220 10KR2J-3-GP
20100705

PCH1F — 6 OF 10 — Cougar Point

S_GPIO — R2218 100R2J-2-GP	GPIO0	T7	BMBUSY#/GPIO0
EC_SMI#	GPIO1	A42	TACH1/GPIO1
DGPU_HPD_INTR#	GPIO6	H36	TACH2/GPIO6
27 EC_SCI#	GPIO7	E38	TACH3/GPIO7
ICC_EN#	GPIO8	C10	GPIO8
PCH_GPIO12	GPIO12	C4	LAN_PHY_PWR_CTRL/GPIO12
PCH_GPIO15	GPIO15	G2	GPIO15
56 SATA_ODD_PRSNT# — R2213 0R0402-PAD	GPIO16	U2	SATA4GP/GPIO16
92,93 DGPU_PWROK	GPIO17	D40	TACH0/GPIO17
49 Color_Engine# — R2228 0R0402-PAD — SB_0728	GPIO22	T5	SCLOCK/GPIO22
TPAD14-GP TP2202	GPIO24/MEM_LED	E8	GPIO24/MEM_LED
PCH_GPIO27	GPIO27	E16	GPIO27
PLL_ODVR_EN	GPIO28	P8	GPIO28
PSW_CLR#	STP_PCI#/GPIO34	K1	STP_PCI#/GPIO34
TPAD14-GP TP2204 — GAP-OPEN G2201	GPIO35	K4	GPIO35
DMI_OVRVLTG	SATA2GP/GPIO36	V8	SATA2GP/GPIO36
FDI_OVRVLTG	SATA3GP/GPIO37	M5	SATA3GP/GPIO37
MFG_MODE	SLOAD/GPIO38	N2	SLOAD/GPIO38
GFX_CRB_DET	SDATAOUT0/GPIO39	M3	SDATAOUT0/GPIO39
TP2209 PCH_GPIO48	SDATAOUT1/GPIO48	V13	SDATAOUT1/GPIO48
PCH_TEMP_ALERT#	SATA5GP/GPIO49	V3	SATA5GP/GPIO49
USB3_PWR_ON	GPIO57	D6	GPIO57

CPU/MISC

TACH4/GPIO68	C40	SATA_ODD_PWRGT 56
TACH5/GPIO69	B41	UMA_DIS# 20
TACH6/GPIO70	C41	VRAM_SIZE1
TACH7/GPIO71	A40	VRAM_SIZE2
A20GATE	P4	H_A20GATE 27
PECI	AU16	H_PECI_R — DY R2203 0R2J-2-GP — H_PECI 5,27
RCIN#	P5	H_RCIN# 27
PROCPWRGD	AY11	H_CPUPWRGD 5,11,36,97
THRMTRIP#	AY10	PCH_THERMTRIP_R R2204 390R2J-1-GP — H_THERMTRIP# 5,36
INIT3_3V#	T14	INIT3_3V# — TP2201 TPAD14-GP

3D3V_S0 — R2205 10KR2J-3-GP — DY — GFX_CRB_DET — R2206 100KR2J-1-GP

PCH_THERMTRIP_R — R2222 — 1D05V_VTT — DY 56R2J-4-GP

TS_VSS1, TS_VSS2, TS_VSS3, TS_VSS4, NC_1 — TS_VSS — R2219 0R0402-PAD

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

NCTF

NCTF_VSS#A4	A4	NCTF_VSS#BG2
NCTF_VSS#A44	A44	NCTF_VSS#BG48
NCTF_VSS#A45	A45	NCTF_VSS#BH3
NCTF_VSS#A46	A46	NCTF_VSS#BH47
NCTF_VSS#A5	A5	NCTF_VSS#BJ4
NCTF_VSS#A6	A6	NCTF_VSS#BJ44
NCTF_VSS#B3	B3	NCTF_VSS#BJ45
NCTF_VSS#B47	B47	NCTF_VSS#BJ46
NCTF_VSS#BD1	BD1	NCTF_VSS#BJ5
NCTF_VSS#BD49	BD49	NCTF_VSS#BJ6
NCTF_VSS#BE1	BE1	NCTF_VSS#C2
NCTF_VSS#BE49	BE49	NCTF_VSS#C48
NCTF_VSS#BF1	BF1	NCTF_VSS#D1
NCTF_VSS#BF49	BF49	NCTF_VSS#D49
		NCTF_VSS#E1
		NCTF_VSS#E49
		NCTF_VSS#F1
		NCTF_VSS#F49

NCTF TEST PIN: A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49, BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48, D1, D49, E1, E49, F1, F49

COUGAR-GP-U2-NF

SB_0811
SHR_V1.5
TPAD14-GP TP2210
TPAD14-GP TP2211
TPAD14-GP TP2212

3D3V_S0 — R2207 10KR2J-3-GP — DY — FDI_OVRVLTG
TPAD14-GP TP2207
TPAD14-GP TP2208 — R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

3D3V_S0 — R2209 10KR2J-3-GP — DY — DMI_OVRVLTG — R2210 10KR2J-3-GP

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

ICC_EN# — R2211 1KR2J-1-GP

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

3D3V_S0 — R2214 10KR23-3-GP (2G) — R2216 10KR23-3-GP (1G)
VRAM_SIZE1
VRAM_SIZE2
R2215 10KR23-3-GP — R2217 10KR23-3-GP
1G_512M_UMA 2G_512M_UMA

[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN — DY R2212 1KR2J-1-GP

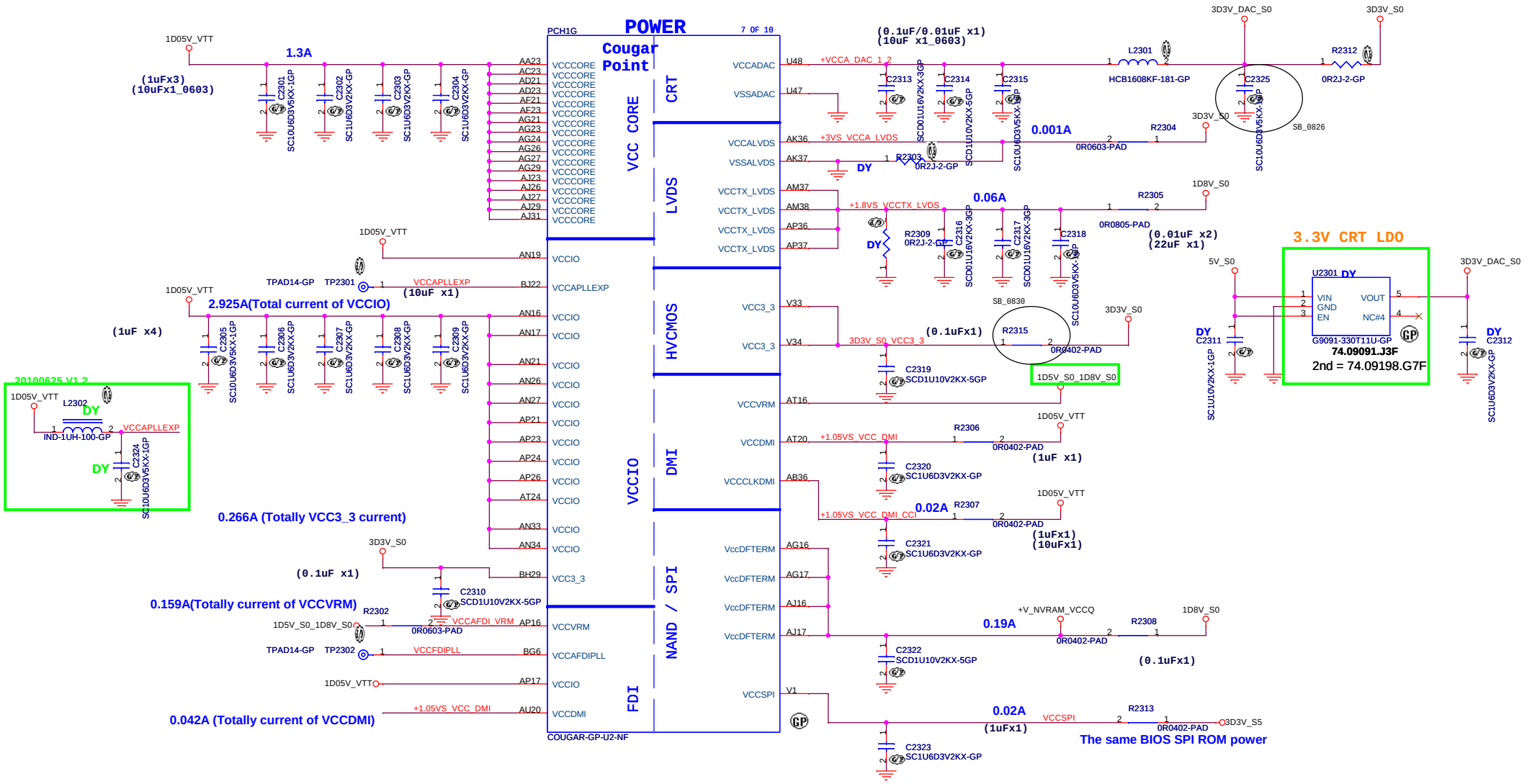
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)
Size: A3 | Document Number: LA470 | Rev: -1
Date: Thursday, December 16, 2010 | Sheet 22 of 97

SSID = PCH 6A

www.rosefix.com



VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop
co-operate with R2103

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, December 16, 2010 Sheet 23 of 97

SSID = PCH

www.rosefix.com

POWER

Cougar Point

10 OF 10

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

COUGAR-GP-U2-NF

0.002A

0.097A (Totally current of VCCSUS3_3)

0.001A

1.01A (Total current of VCCASW)

0.08A

0.16A (Totally current of VCCVRM)

0.055A

0.095A

0.01A

6uA

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

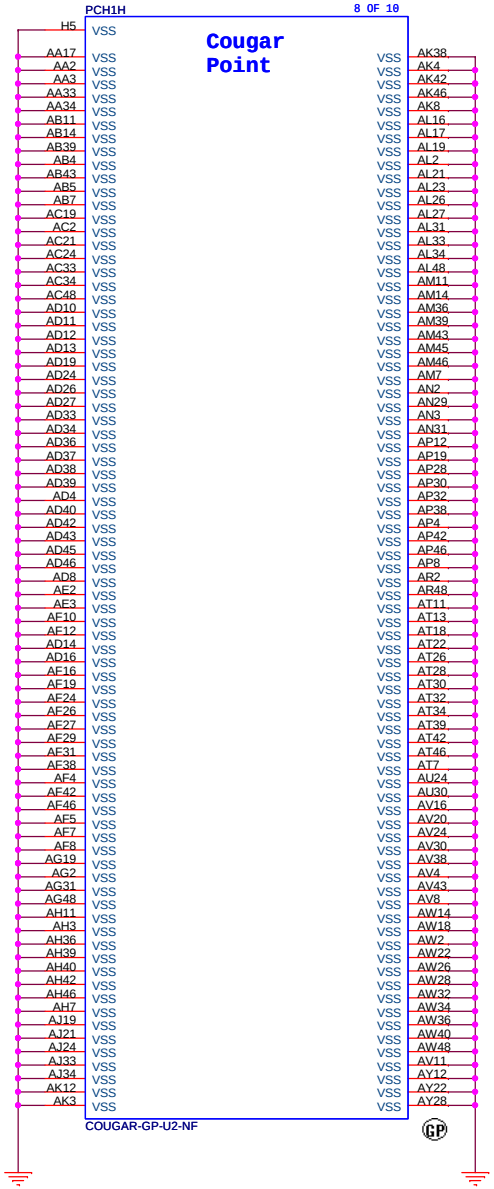
Title: PCH (POWER2)

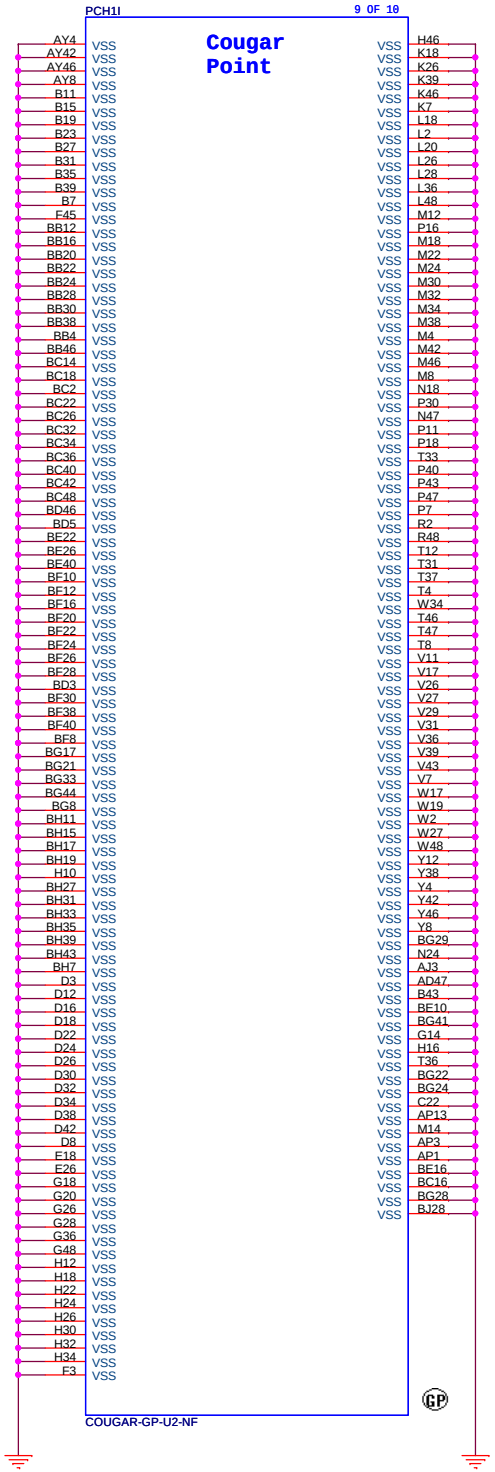
Size: A3 | Document Number: LA470 | Rev: -1

Date: Thursday, December 16, 2010 | Sheet 24 of 97

SSID = PCH

www.rosefix.com





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, December 16, 2010 Sheet 25 of 97

www.rosefix.com

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, December 16, 2010 Sheet 26 of 97

www.rosefix.com

SSID = KBC

PCB Version A,D (Pin98)	Pull Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	0.0 K	10.0 K	3.0 V
SB	0.0 K	20.0 K	2.75 V
SC	0.0 K	33.0 K	2.48 V
-1	100.0 K	47.0 K	2.24 V
Reserved	100.0 K	64.9 K	2.0 V
Reserved	100.0 K	76.8 K	1.87 V
Reserved	100.0 K	100.0 K	1.65 V

65W_90W#
High: 65W / Low 90W

G Sensor ID:
High: ST
Low:ADI

NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L..

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

<---------- TP
<---------- BATTERY / CHARGER
<---------- PCH / eDP

R2701 and C2716
Need very close to EC

EC GPIO standard PH/PL

EC_GPIO47 High Active

Prevent BIOS data loss solution

LILI Multi GPIO setting

MODEL_ID_A0 (Pin100)	Pull-Low Register	Pull-High Register	Voltage
V/B 47 UMA	100.0 K	33.0 K (63.33334 1.DL)	2.481 V
V/B 47 OPTIMUS	100.0 K	47.0 K (63.47334 1.DL)	2.245 V

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795
Size: A1 | Document Number: LA470 | Rev: -1
Date: Thursday, DECEMBER 20, 2007 | Sheet 27 of 37

SSID = Thermal

Thermal sensor

www.rosefix.com

Close to PCH on top side.

SA_0905 change to 390p

3
Q6
MMBT3904WT1G-GP
C183
SC390P50V2KX-GP

2
Q42
MMBT3904WT1G-GP
C434
SC390P50V2KX-GP
DY

2200p close to smsc2103 chip
REMOTE2-
REMOTE2+
C569
SC2200P50V2KX-2GP

between CPU, VGA and DIMM on bottom side

T8

1
Q9
MMBT3904WT1G-GP

2200p close to smsc2103 chip
H_THERMDA
H_THERMDC
C389
SC2200P50V2KX-2GP

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width
and spacing. Locate Capacity near Thermal diode.

4 WIRE PWM Fan Control circuit

Close to connector

5V_S0
SA_0905
D2801
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
DY
C39
SC4D7U6D3V3KX-GP
R2801
0R0603-PAD-PAD
R426
10KR2J-3-GP
SB_0819
FAN_TACH
FAN_PWM
5V_S0_FAN
FAN_PWM_C
R427
0R0402-PAD
EC2801
EC2802
SC1KP50V2KX-1GP
DY
20100707_EMI
FAN1
ACES-CON4-4-GP
20.F0765.004
2nd = 20.F1808.004

3D3V_S0
R280
6K8R2J-GP
SHDN_SEL

SHDN --> 2N3904 ON External diode

3D3V_S0
R260
68R2-GP
C388
SCD1U10V2KX-4GP
2103_VDD
U31
H_THERMDA
H_THERMDC
REMOTE2+
REMOTE2-
SC 1203
THERM_SCI#
TP66
TPAD14-GP
R272
0R0402-PAD
THERM_SYS_SHDN#
THERM_SCI#_R
27,86 SMBC_THERM
27,86 SMBD_THERM
VDD
DP1
DN1
DP2/DN3
ND2/DP3
SYS_SHDN#
ALERT#
SMCLK
SMDATA
GPIO1
GPIO2
TACH
PWM
TRIP_SET
SHDN_SEL
GND
GND
EMC2103-2-AP-GP
2103_4
2103_5
TP65 TPAD14-GP
TP67 TPAD14-GP
TRIP_SET R276
649R2F-GP
T8 = 98
TRIP_SET: 649 ohm => 87 dgree C
RN49
SRN10KJ-5-GP
3D3V_S0
D2802
CH551H-30PT-GP
FAN_TACH
FAN_PWM
2ND = 83.5R003.08F
3rd = 83.R5003.G8F
83.R5003.C8F

pin6, ALERT# OD
pin7, SYS_SHDN# OD

AFTP2803
AFTP2802
AFTP2801
FAN_PWM_C
FAN_TACH
5V_S0_FAN
SB_0825

3D3V_AUX_S5
D2803
BAT54PT-GP
83.00054.T81
2ND = 83.BAT54.D81
3rd = 83.BAT54.S81
DY
27,36,86 PURE_HW_SHUTDOWN#
R2812
10KR2J-2-GP
DY
C2811
SCD1U10V2KX-4GP
DY
Q2802
2N7002K-2-GP
1st = 84.2N702.031
2ND = 84.2N702.J31
SB_0812
THERM_SYS_SHDN#
R2810
0R2J-2-GP
DY
R2811
0R2J-2-GP
3D3V_S0
IMVP_PWRGD 36,42
3D3V_S0
R2809
100KR2J-1-GP

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL SENSOR SMSC EMC2103

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, December 16, 2010 Sheet 28 of 97

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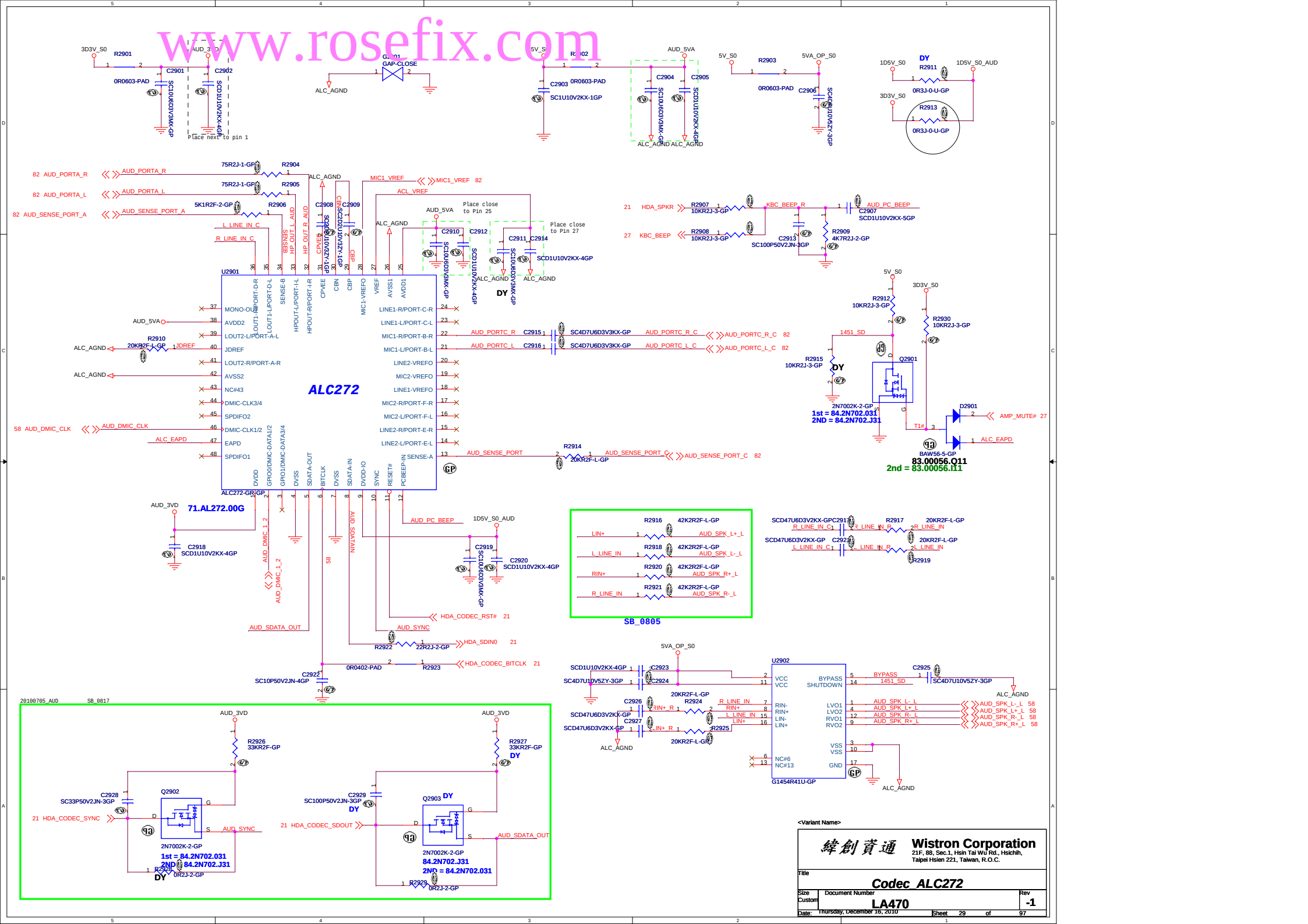

www.rosefix.com

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio AMP***

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, December 16, 2010 Sheet 30 of 97

www.rosefix.com

25MHz XTAL

LAN_XTAL0 — X2 — LAN_XTAL1
XTAL-25MHZ-102-GP
82.30020.851
2ND = 82.30020.791
3rd = 82.30020.A31
R3130 1M1R2J-GP
SB_0824
C3103 25C12P50V2JN-3GP
C3148 25C12P50V2JN-3GP

R3123 2K49R2F-GP — LAN_RSET
LAN_ACT_LED# 59

LAN_EESK — R3127 0R0402-PAD — SPEED_100# 59

3D3V_S0 (main pwr if have no ASF)
R3136 1KR2J-1-GP
RTL_ISOLATE#
R3119 15KR2J-1-GP

U3101 RTL8111E-VB-GR-GP

49	GND		
1	MDIP0	59	MDI0+
2	MDIN0	59	MDI0-
3	AVDD10	1D05V_LAN_S5	
4	MDIP1	59	MDI1+
5	MDIN1	59	MDI1-
6	AVDD10	1D05V_LAN_S5	
7	MDIP2	59	MDI2+
8	MDIN2	59	MDI2-
9	AVDD10	1D05V_LAN_S5	
10	MDIP3	59	MDI3+
11	MDIN3	59	MDI3-
12	AVDD33	3D3V_LAN_S5	
36	REGOUT	1D05V_LAN_REGOUT	
35	VDDREG	3D3V_LAN_VDDSREG	
34	VDDREG		
33	ENSWREG	LAN_ENSWREG	
32	EEDI/SDA	LAN_EEDI	
31	LED3/EEDO	LAN_EEDO	
30	EECS/SCL	LAN_EECS	
29	DVDD10	1D05V_LAN_S5	
28	LANWAKE#	PCIE_WAKE#	
27	DVDD33	3D3V_LAN_S5	
26	ISOLATE#	RTL_ISOLATE#	
25	PERST#	PLT_RST#	5,11,19,27,36,65,66,71,83,97
48	AVDD33		
47	AVDD33		
46	RSET		
45	AVDD10		
44	CKXTAL2	LAN_XTAL0	
43	CKXTAL1	LAN_XTAL1	
42	AVDD33		
41	DVDD10		
40	LED0	GPO	
39	DVDD33		
38	GPO/SMBALERT	LAN_EESK	
37	LED1/EESK		
13	DVDD10		
14	SMBCLK		
15	SMBDATA		
16	CLKREQ#		
17	HSIP		
18	HSIN		
19	REFCLK_P		
20	REFCLK_N		
21	EVDD10		
22	HSOP		
23	HSON		
24	GND		

20 LAN_XI — R3132 DY 0R2J-2-GP — LAN_XTAL1

Pin-XTAL2 is External Clock Input Pin.
R3121 is need when using external clock source.

3D3V_LAN_VDDSREG
R2J-2-GP R3125 — 3D3V_LAN_S5
R3102 0ohm PAD For Enable Switch Regulator.
R3103 0ohm Res For Disable Switch Regulator.
TP3102 TPAD14-GP
R3124 0R2J-2-GP DY

3D3V_LAN_S5
High:Link up
Low:Link down
GPO — R3120 1KR2J-1-GP
LAN_EECS — R3122 10KR2J-3-GP
LAN_EEDI — R3126 10KR2J-3-GP
SMB_LAN_DATA — R3128 10KR2J-3-GP
The SM DATA with 10K ohm pull GND.

Make sure PCIE_Wake# & PCIE_CLK_LAN_RQ1#connected to 10K resistor pull high close to PCH side

1D05V_LAN_S5
R3121 SMB_LAN_DATA
LAN_CLKREQ# — 0R0402-PAD
SB_0728
20 PCIE_CLK_LAN_REQ#
20 PCIE_TXP4
20 PCIE_TXN4
20 CLK_PCIE_LAN
20 CLK_PCIE_LAN#
1D05V_LAN_EVDD10
20 PCIE_RXP4 — PCIE_RXP4_C — C3145 SCD1U10V2KX-4GP
20 PCIE_RXN4 — PCIE_RXN4_C — C3147 SCD1U10V2KX-4GP

3D3V_LAN_S5
R3135 DY 0R3J-0-U-GP
3D3V_S5
C3151 SCD1U10V2KX-4GP
C3152 SCD1U16V2ZY-2GP
R3133 100KR2J-1-GP
Q3103 -1 0114 AO3419L-GP
LAN_PWR_ON_T
C3150 SC1U10V2KX-1GP
Q3104 2N7002K-1-GP
27 LAN_PWR_ON
84.2N702.031
2nd = 84.2N702.J31

SB_0812
20100705_Standard
vendor advice change
1D05V_LAN_REGOUT — L3102 IND-4D7UH-159-GP — 1D05V_LAN_S5
C3146 SC4D7U6D3V3KX-GP
C3129 SCD1U10V2KX-4GP
L3101 adopt spec.
C3104 change to 4.7uF X5R type capacitor

Layout Note: Close to U3101 pin C3106 ~ C3112
C3130 C3131 C3132 C3133 C3134 C3138 C3139 SCD1U16V2ZY-2GP

R3131 0R0603-PAD — 1D05V_LAN_EVDD10
C3128 SC1U10V2KX-1GP
C3149 SCD1U16V2ZY-2GP
Layout Note: Close to U3101 pin C3113&C3114
C3113 value modify to 1uF capacitor

3D3V_LAN_S5
R3134 0R0603-PAD — 3D3V_LAN_VDDSREG
C3135 C3140 C3141 C3142 C3143 C3144 SCD1U16V2ZY-2GP
Layout Note: Close to U3101 pin C3115 ~ C3120
C3136 SCD1U16V2ZY-2GP
C3137 SC4D7U6D3V3KX-GP
C3122 change to 4.7uF X5R type capacitor

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8111E
Size: A3 | Document Number: LA470 | Rev: -1
Date: Thursday, December 16, 2010 | Sheet 31 of 97

www.rosefix.com

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5159 (CARD READER)***

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, December 16, 2010 Sheet 32 of 97

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, December 16, 2010 Sheet 33 of 97

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, December 16, 2010 Sheet 34 of 97

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

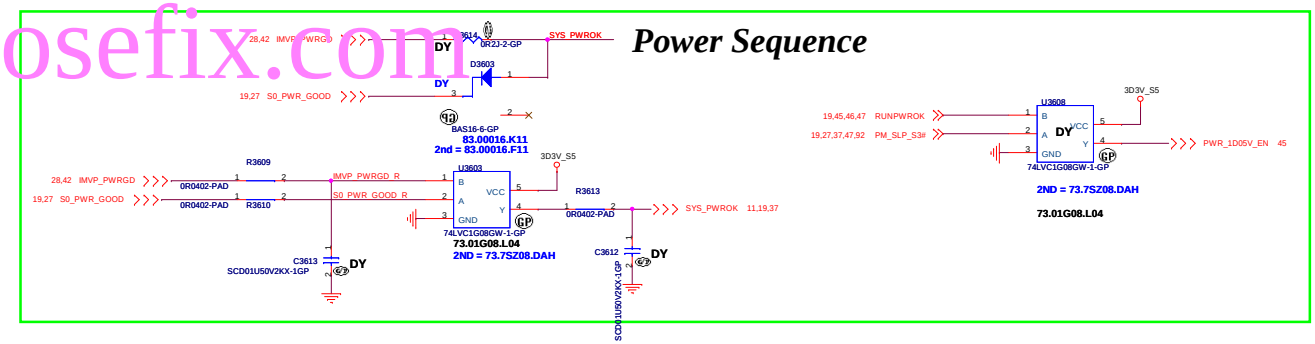
Title
USB 3.0 Controller

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, December 16, 2010 Sheet 35 of 97

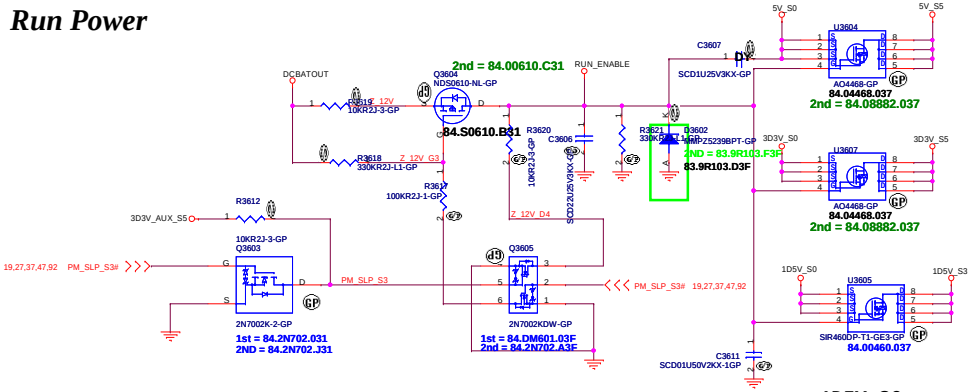
www.rosefix.com

Power Sequence



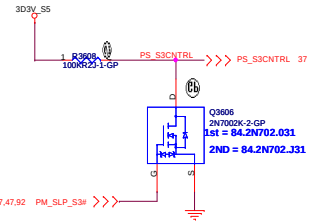
SSID = Reset.Suspend

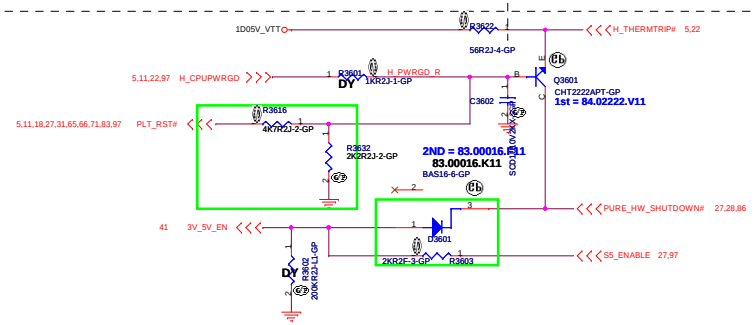
Run Power



1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

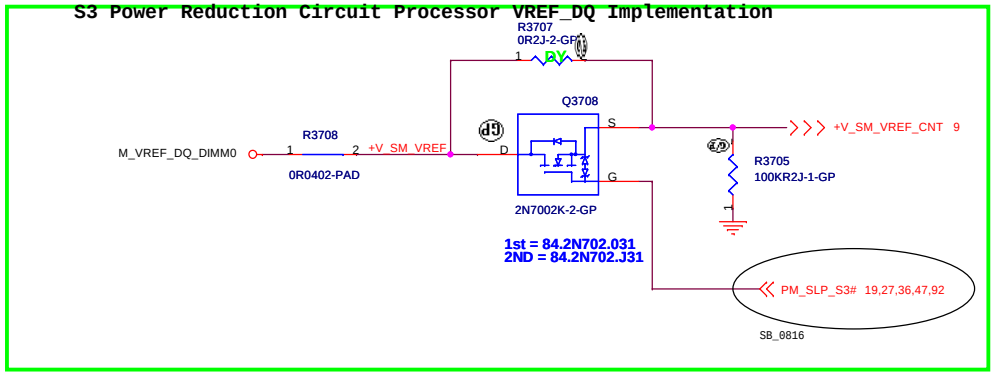
Title: **Power Plane Enable**

Size	Document Number	Rev
A2	LA470	-1

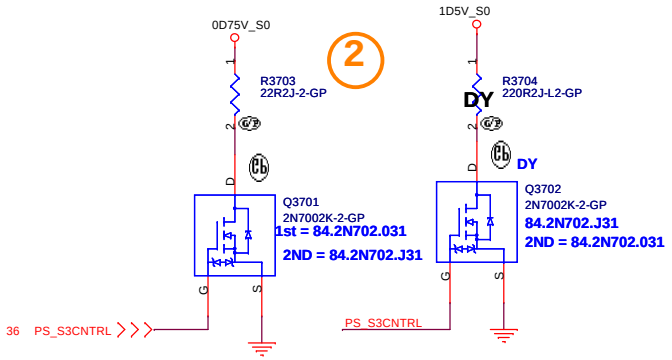
Date: Thursday, December 16, 2010 Sheet 36 of 97

www.rosefix.com

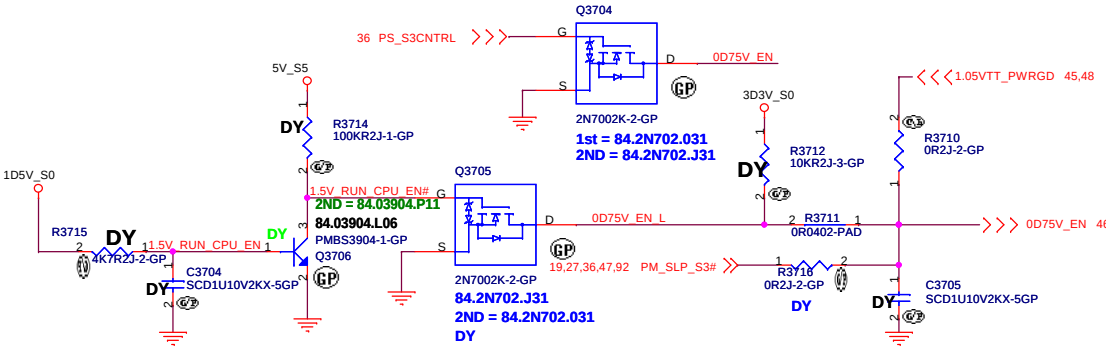
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



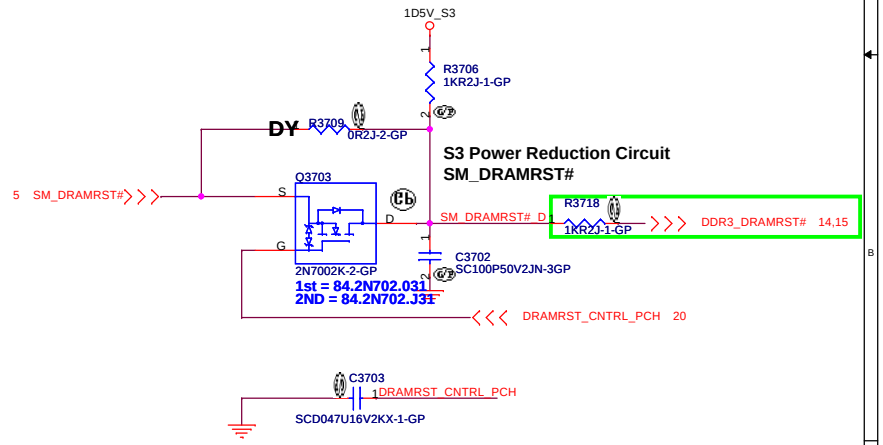
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



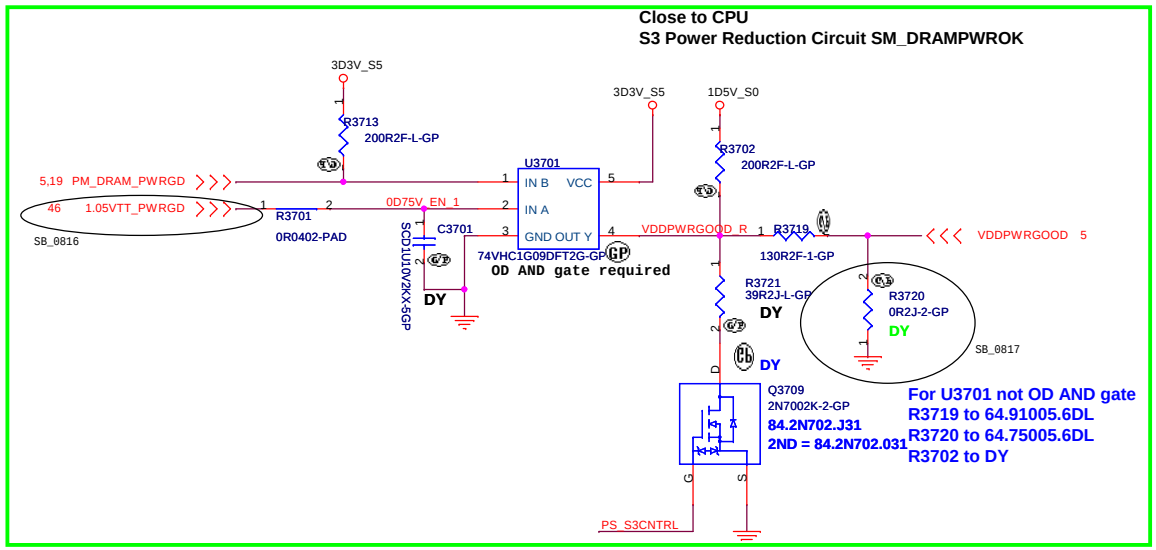
5 S3 Power Reduction X01 20091111



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

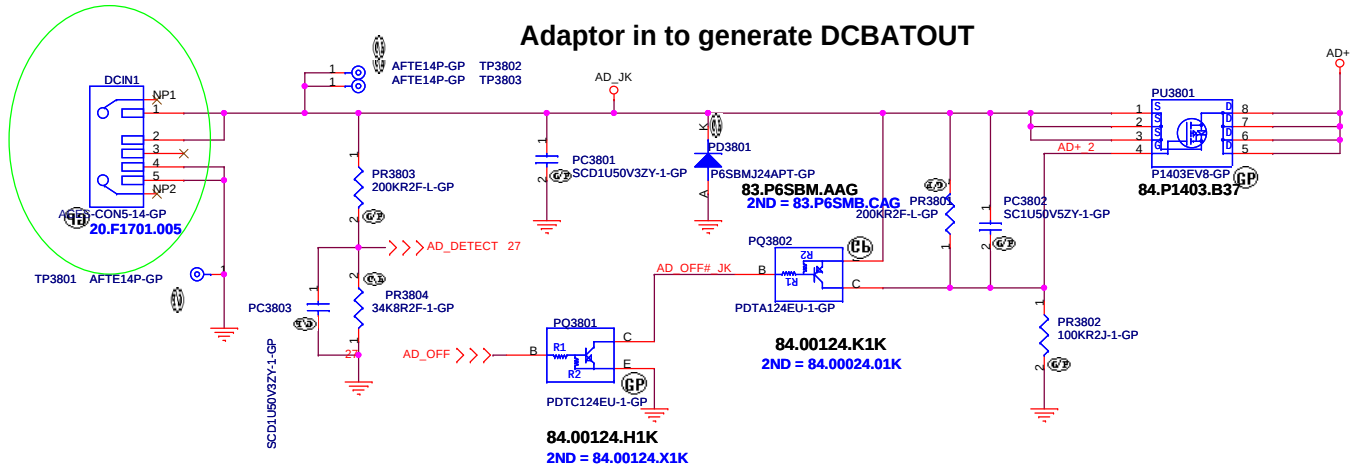
Title: ADAPTER

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, December 16, 2010 Sheet 37 of 97

www.rosefix.com

Adaptor in to generate DCBATOUT



JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN_JACK*		
Size	Document Number: **LA470**	Rev: **-1**
Date: Thursday, December 16, 2010	Sheet 38 of 97	

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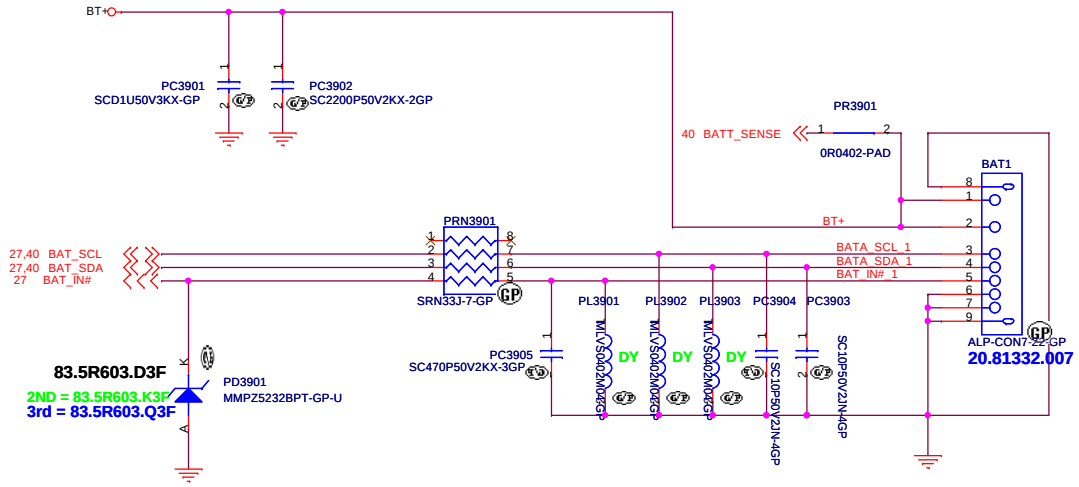
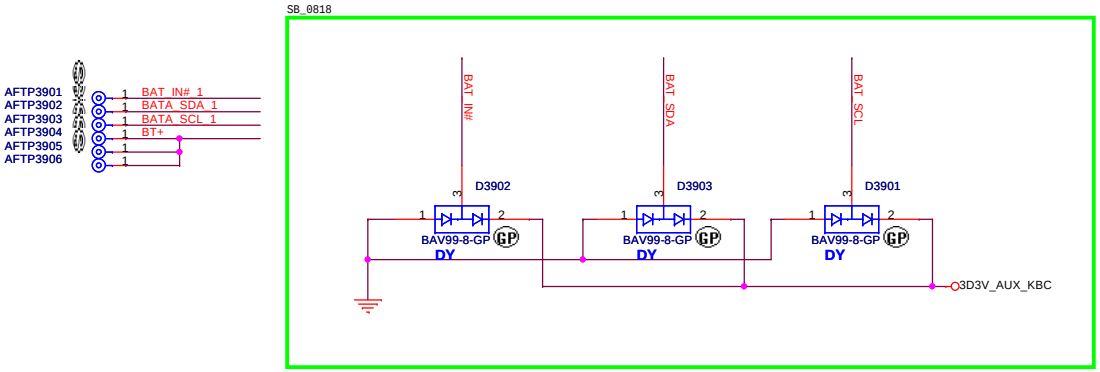
BATTERY CONNECTOR





DY ???

JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT_CONN	
Size	Document Number LA470	Rev -1
Date: Thursday, December 16, 2010	Sheet 39 of 97	

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AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

NEAR

AD+
PU4001
P1403EV8-GP
84.P1403.B37
PR4002 100KR2J-1-GP
AD+_G_2
PR4001 10KR2F-2-GP
PR4003 49K9R2F-L-GP
AD+_G_1
DC_IN_D
PQ4001 2N7002KDW-GP
1st = 84.DM601.03F
2nd = 84.2N702.A3F
BQ24745_ACOK
PR4006 316KR3F-2-GP
PC4001 SC1U25V3KX-1GP
AD+
PD4001 1SS400GPT-GP
83.00400.C1F
2nd = 83.1S400.B2F
AD+_TO_SYS
PR4004 D01R3721F-GP-U
DCBATOUT
PU4002 P1403EV8-GP
84.P1403.B37
PD4002 SMF18A-GP
83.SMF18.AAH
PR4005 470KR2J-2-GP
BT+
20100518 WAYNE
PG4001 GAP-CLOSE-PWR-3-GP
PG4002 GAP-CLOSE-PWR-3-GP
PC4018 SCD1U50V3KX-GP
CHG_AGND
STOP_CHG#
connects to KBC
3D3V_AUX_S5
PR4009 10KR2F-2-GP
STOP_CHG#
BQ24745_VREF
R1
PR4007 121KR2F-L-GP
BOM Ctrl
20100707
CHG_ICREF
R2
PR4008 49K9R2F-L-GP
PC4002 SCD1U50V3KX-GP
DY
BQ24745_CSSP
PC4003 SCD1U50V3KX-GP
PC4004 SCD1U50V3KX-GP
79.10712.L02
PC4025 SE100U25VM-L1-GP
PC4023 SC10U25V6KX-1GP
PC4005 SC10U25V6KX-1GP
PC4006 SCD1U25V2ZY-1GP
PU4003 BQ24745RHDR-GP
BQ24745_DCIN
BQ24745_ACIN
3D3V_AUX_S5
PR4010 49K9R2F-L-GP
PC4007 SCD01U50V2KX-1GP
AC_IN
PR4011
BQ24745_ACOK
PC4008 SC1U10V3KX-3GP
GAP-CLOSE-PWR-3-GP
27,39 BAT_SCL
27,39 BAT_SDA
CHG_AGND
PR4012 0R0402-PAD
BQ24745_CSSN
BQ24745_ICOUT
BQ24745_BST
BQ24745_VDDP
PD4003 CH520S-30PT-GP
PC4009 SC1U10V3KX-3GP
PU4004 SIS412DN-T1-GE3-GP
83.R0203.08F
2nd = 83.1R003.I8F
24745_HIGH_G
PC4017 SCD1U50V3KX-GP
BQ24745_LX1
PL4001 IND-5D6UH-39-GP
68.5R610.10P
PR4017 D01R3721F-GP-U
BT+_R
SC_1021
24745_LOW_G
PU4005 SIS412DN-T1-GE3-GP
PC4016 SCD1U50V3KX-GP
PG4003 GAP-CLOSE-PWR-3-GP
PG4004 GAP-CLOSE-PWR-3-GP
20100518 WAYNE
PC4020 SC10U25V6KX-1GP
PC4021 SC10U25V6KX-1GP
PC4022 SCD1U50V3KX-GP
MAX8731A_CSIP
MAX8731A_CSIN
AD_IA
PR4013 0R0402-PAD
SC150P50V2JN-3GP
PC4010
PR4014 4K7R2J-2-GP
PR4015 200KR2F-1-GP
PC401 SC220P50V2KX-3GP
PC4012 SC2200P50V2KX-2GP
PR4016 7K5R2F-1-GP
PC4013 SC56P50V2JN-2GP
PC4014 SC1U10V3KX-3GP
74.24745.073
BATT_SENSE
BATT_SENSE 39
PC4015 SCD1U25V2ZY-1GP
PR4018 0R0402-PAD
BQ24745_VREF
PRN4001 SRN100KJ-5-GP
AC_IN
CHG_ON#
BQ24745_CHG_ON
SC_1019
SB_0812
PQ4002 2N7002K-2-GP
1st = 84.2N702.031
2ND = 84.2N702.J31
C4001 SCD1U10V2KX-4GP
AC_IN to KBC

JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger_BQ24745
Size: Document Number: LA470
Rev: -1
Date: Thursday, December 16, 2010
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SSID = PWR.Plane.Regulator.5v3p3v

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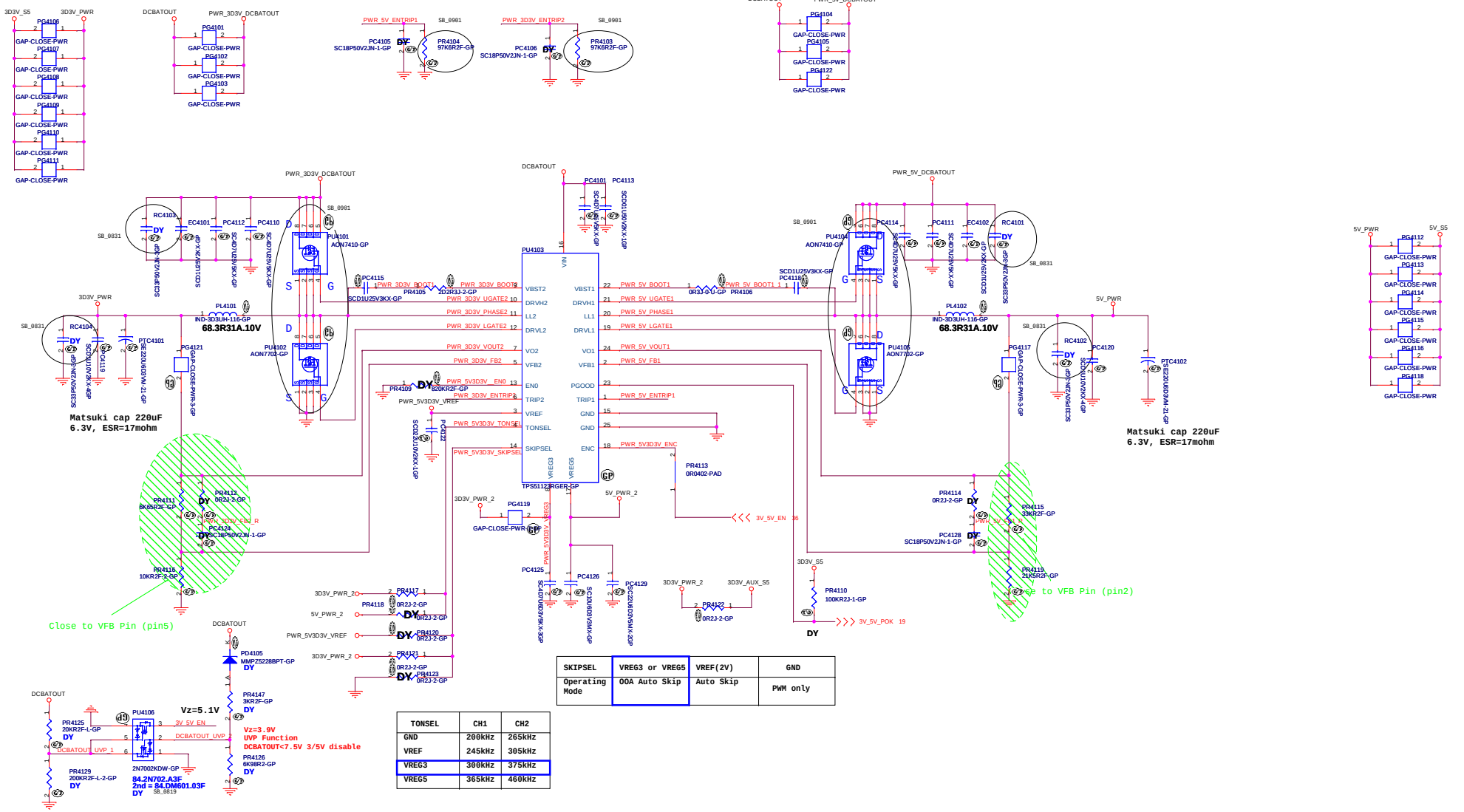

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

JV10-CS

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC 3D3V5V

Size: | Document Number: LA470 | Rev: -1

Date: Thursday, December 16, 2010 | Sheet 41 of 97

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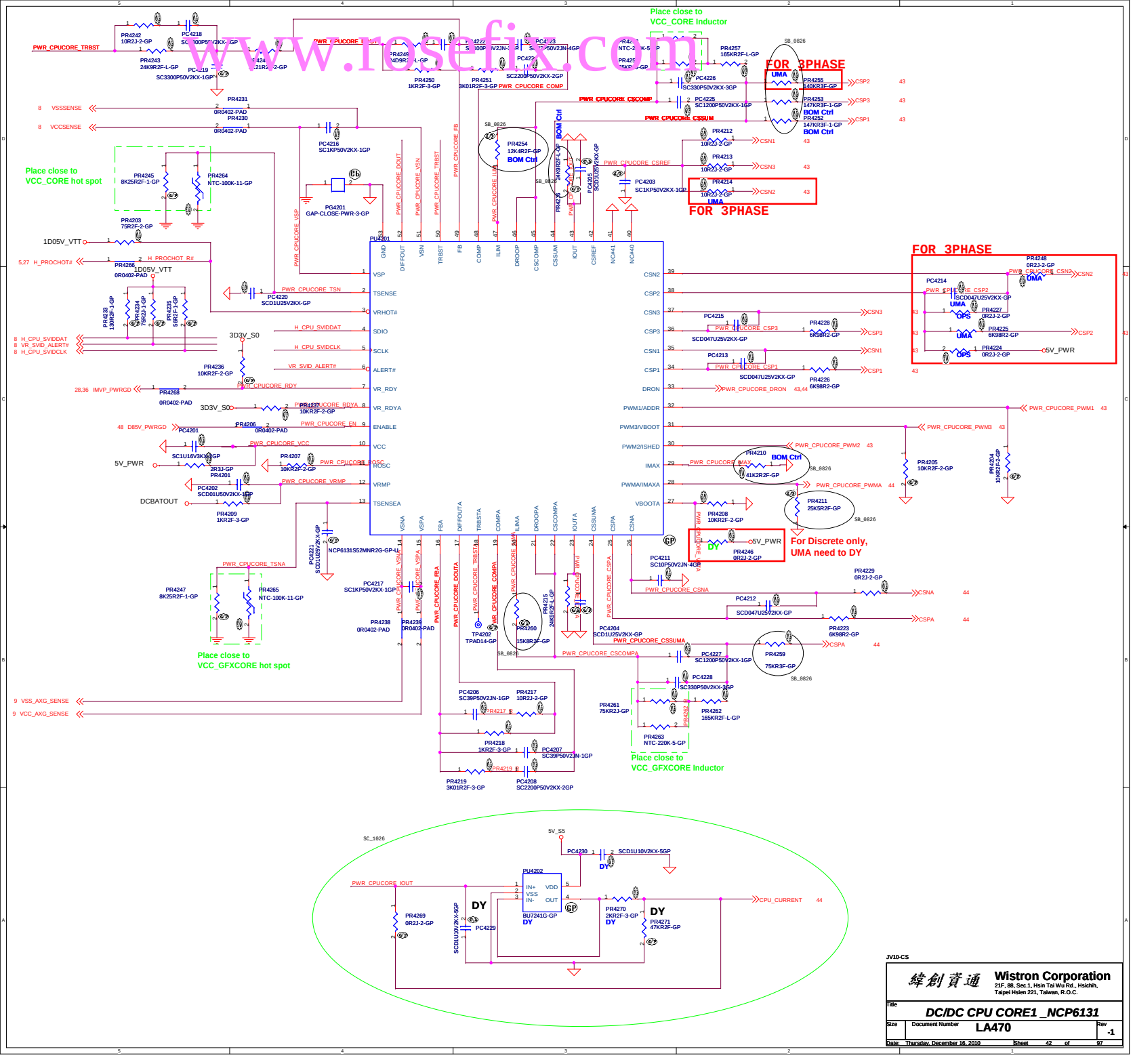
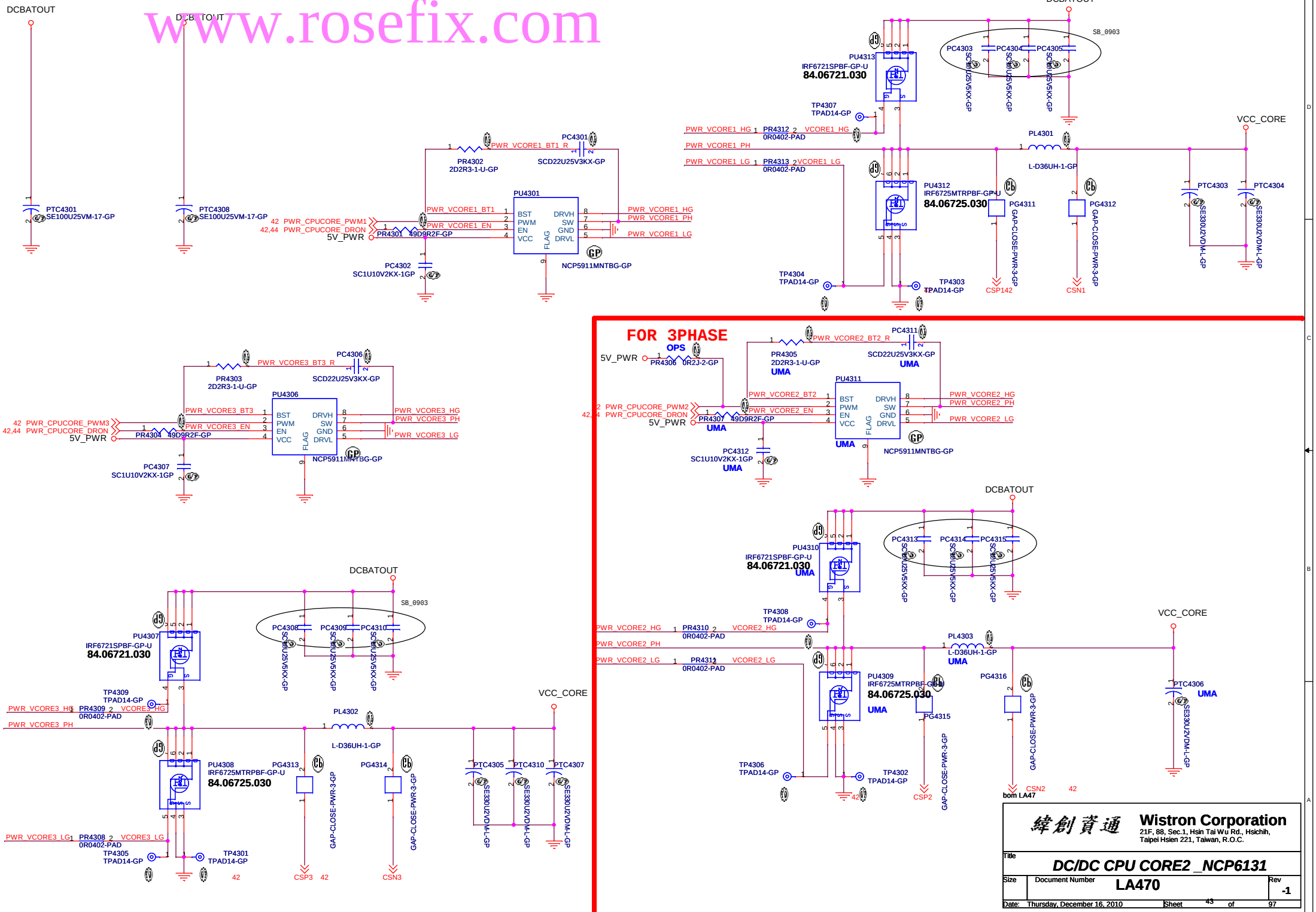
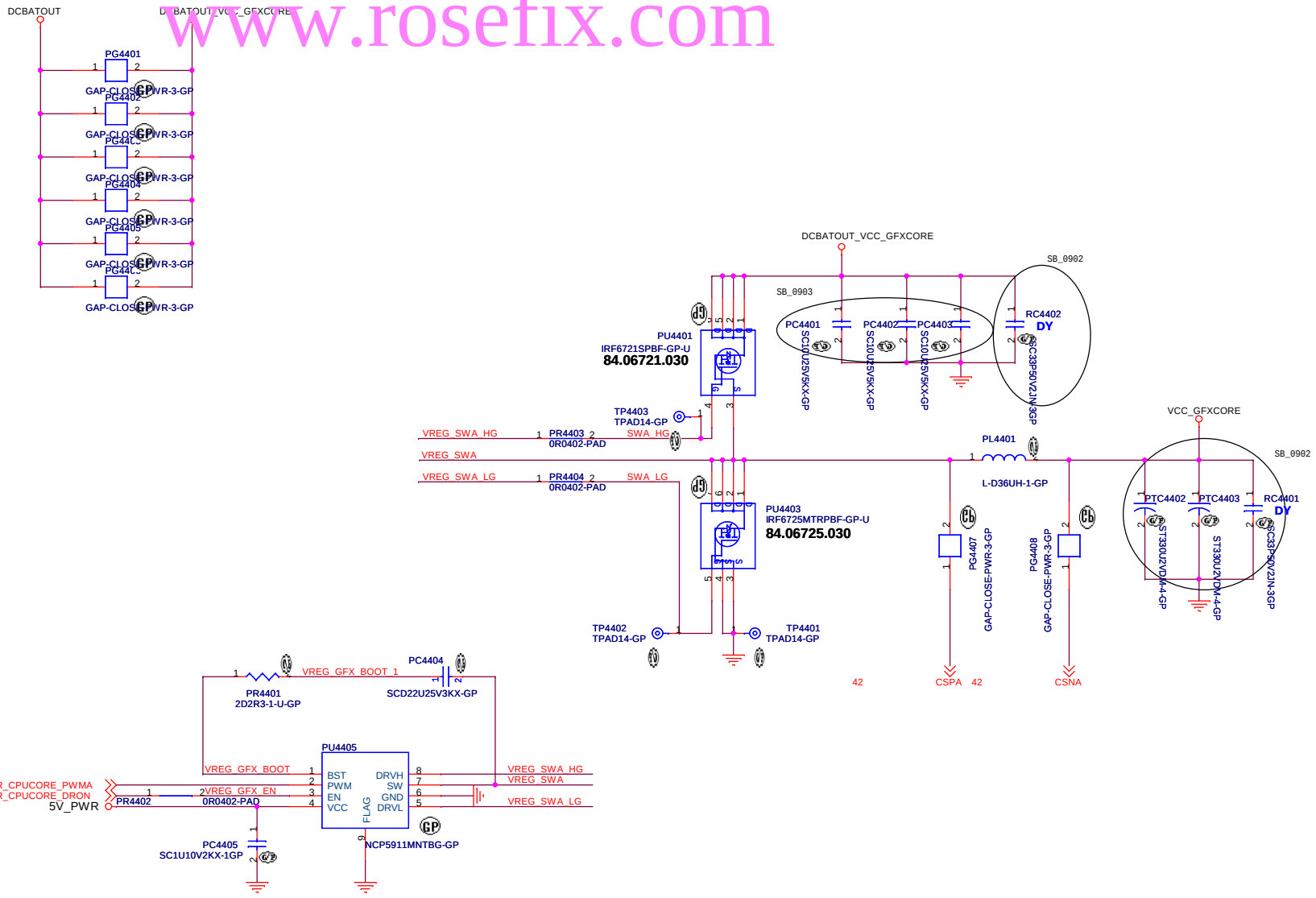


www.rosefix.com



www.rosefix.com



JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DC/DC CPU CORE3 _NCP6131***	
Size	Document Number **LA470**	Rev **-1**
Date: Thursday, December 16, 2010	Sheet 44 of 97	

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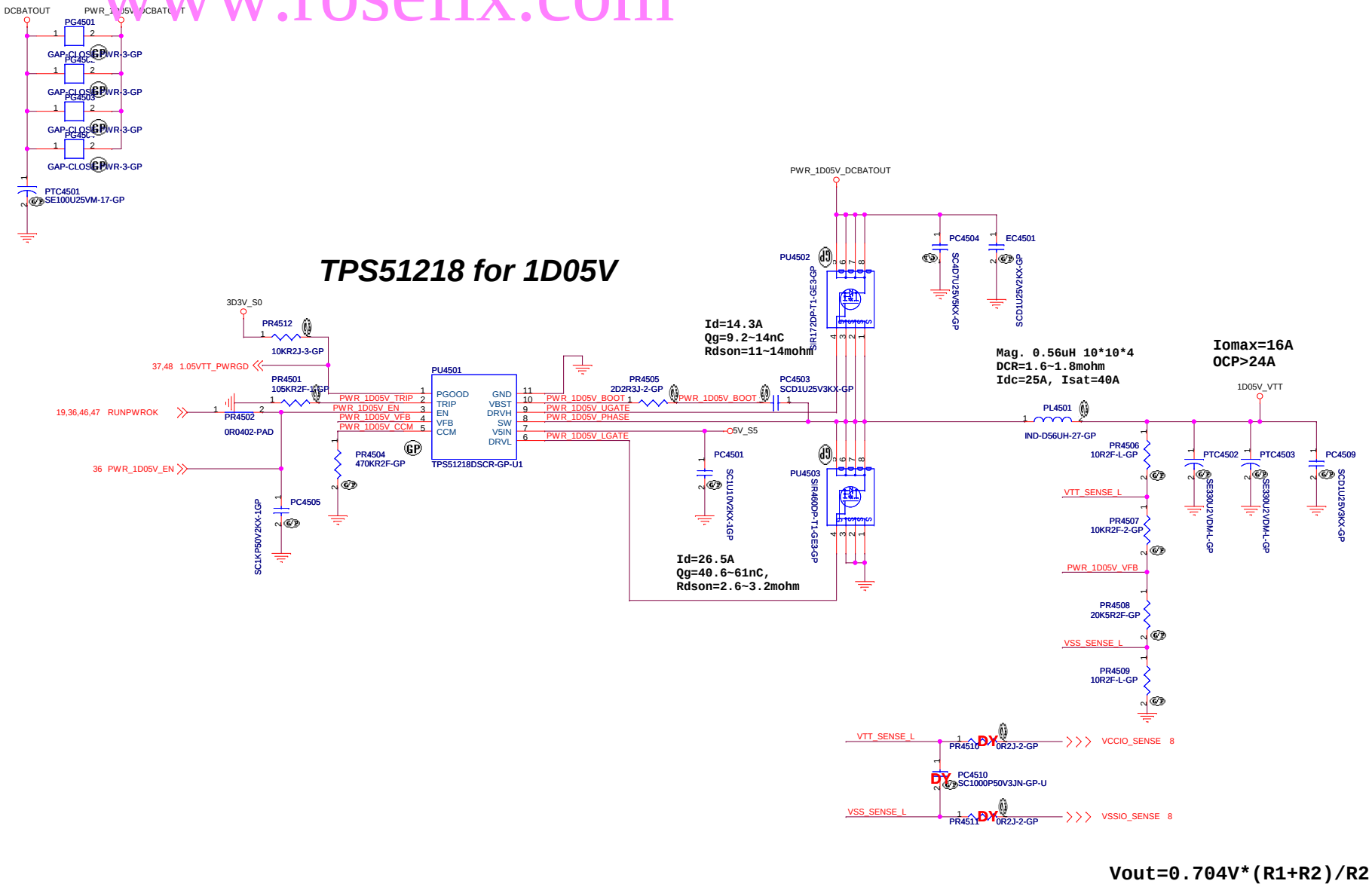

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51218_1D05V	
Size	Document Number	Rev -1
Date: Thursday, December 16, 2010	Sheet 45 of 97	

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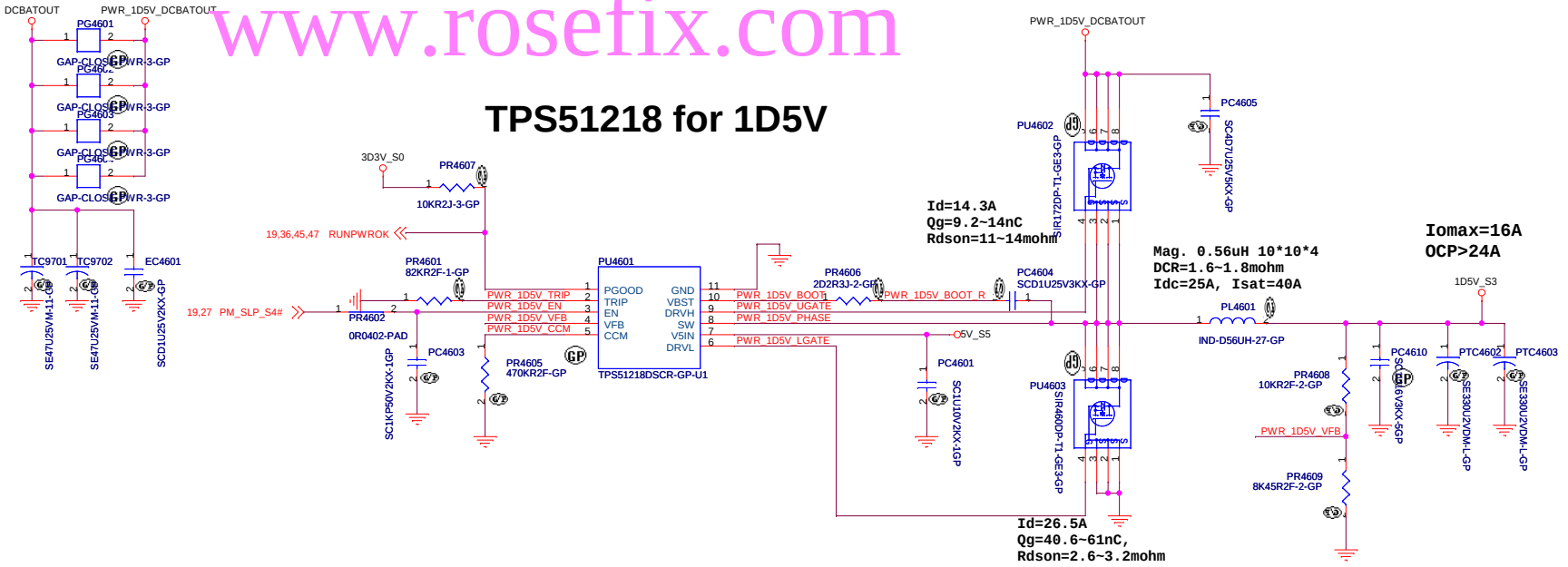
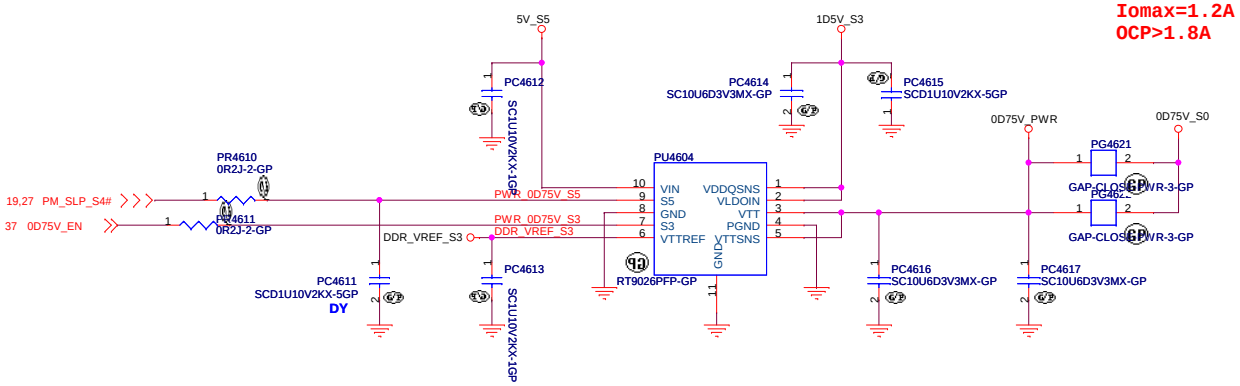
TPS51218 for 1D5V



RT9026 for 0D75V_S3



CADIZ-CP

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
TPS51128_1D5V & RT9026PFP-GP_0D75V

Size	Document Number	Rev
		-1

Date: Thursday, December 16, 2010 Sheet 46 of 97

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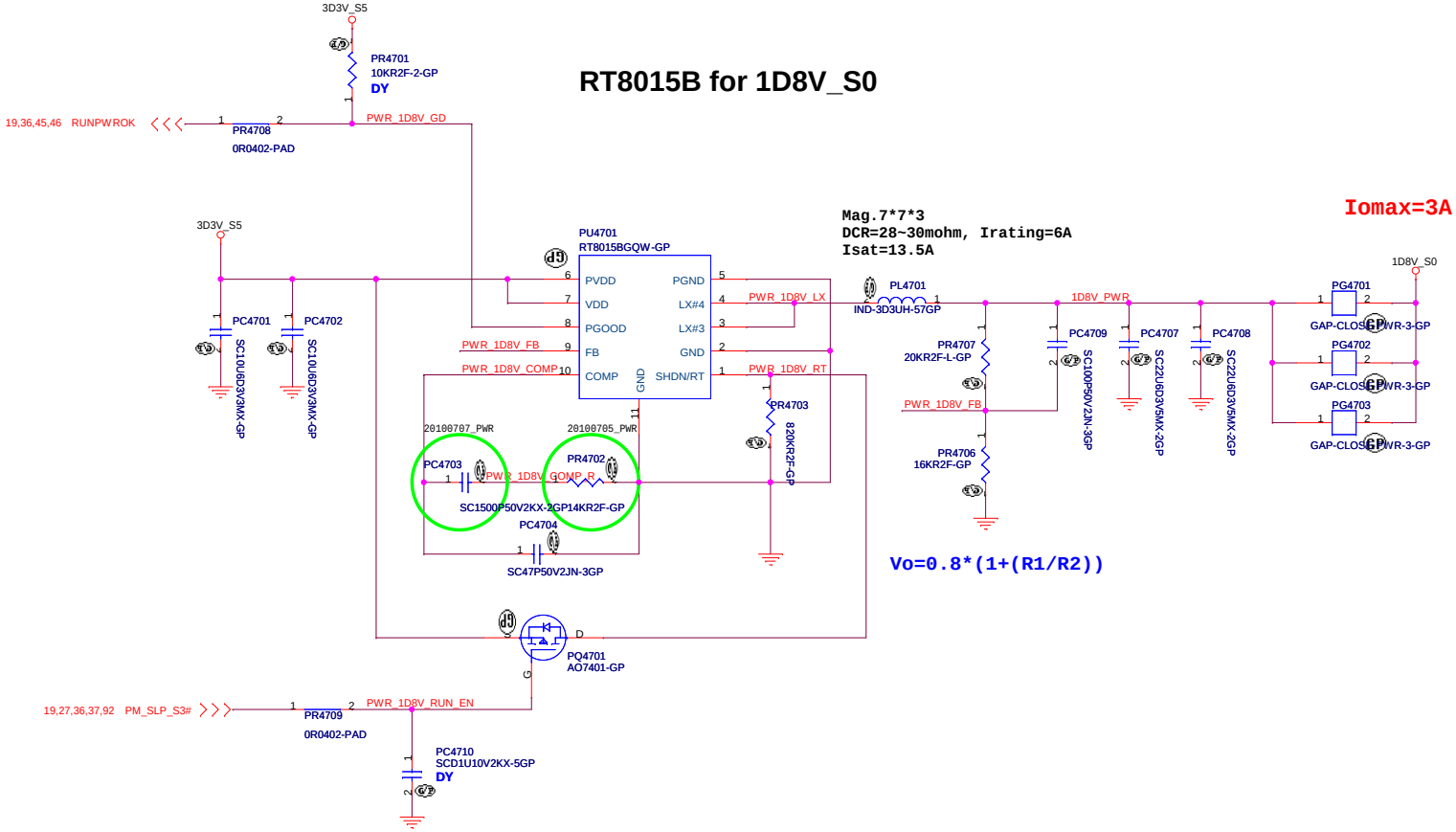
RT8015B for 1D8V_S0



JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	PWM_1D8V_RT8015B	
Size	Document Number LA470	Rev -1
Date: Thursday, December 16, 2010	Sheet 47 of 97	

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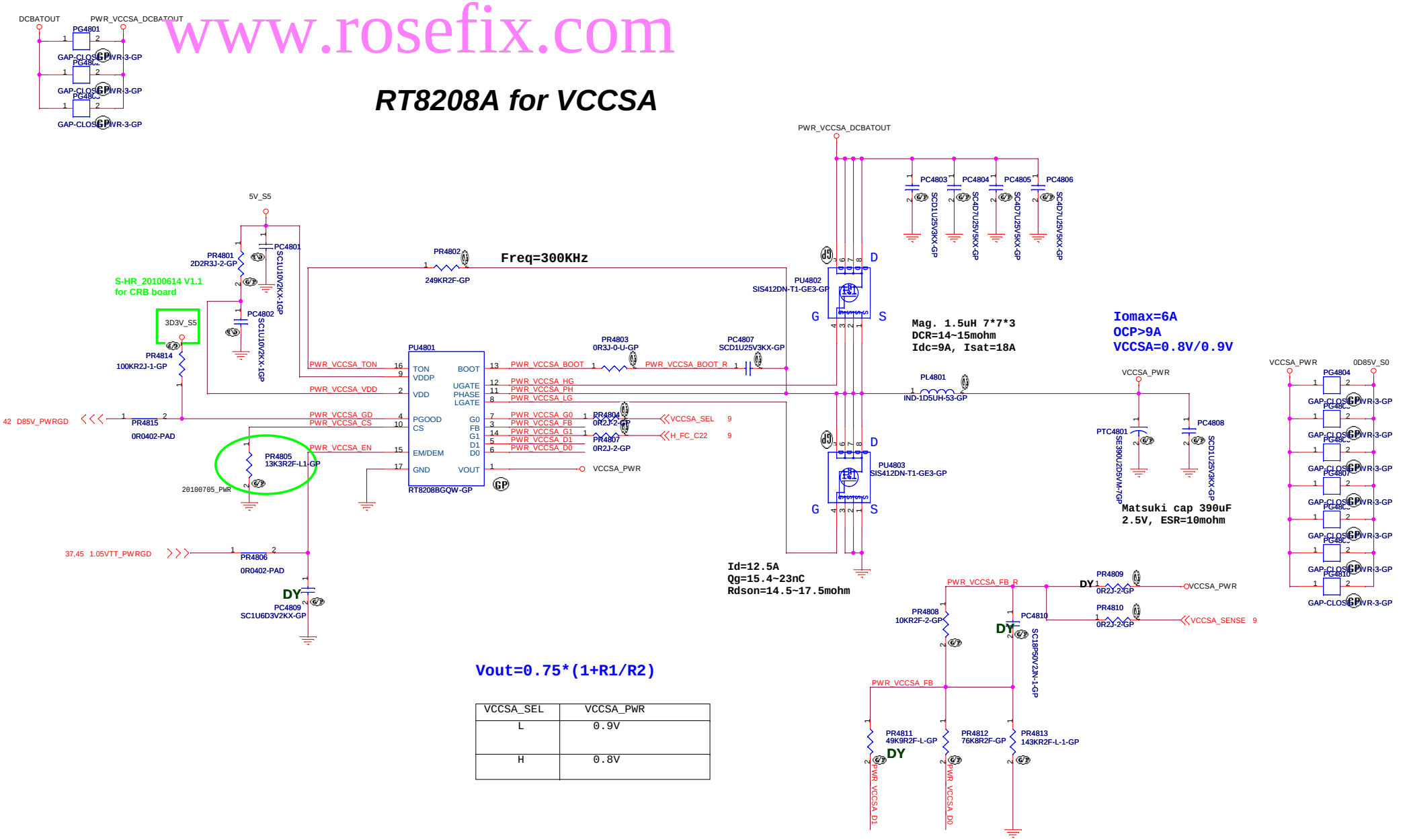
RT8208A for VCCSA



Vout=0.75*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_VCCSA

Size | Document Number: LA470 | Rev: -1

Date: Thursday, December 16, 2010 | Sheet 48 of 97

SSID = VIDEO

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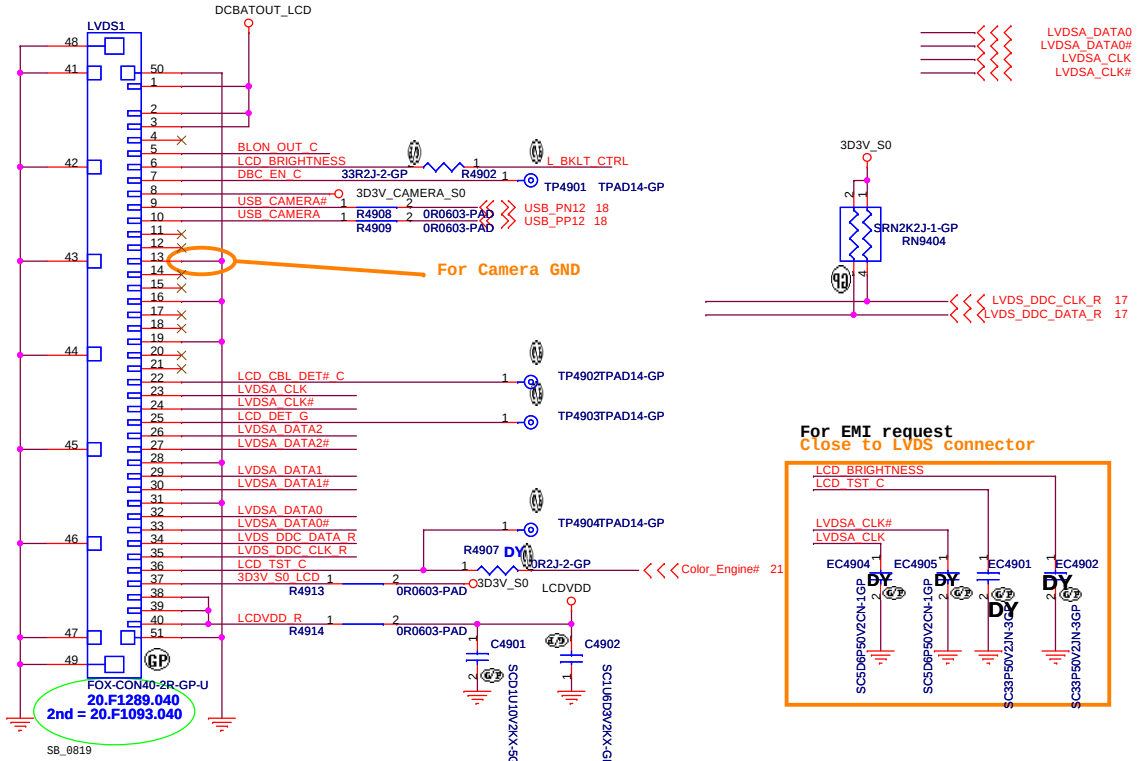
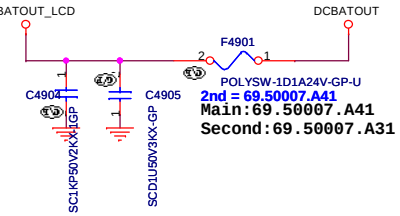
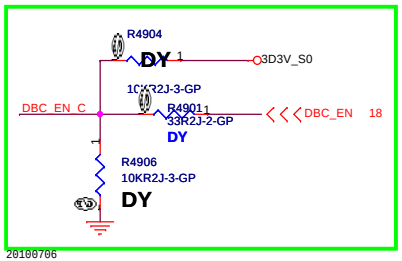
LVDS CONNECTOR

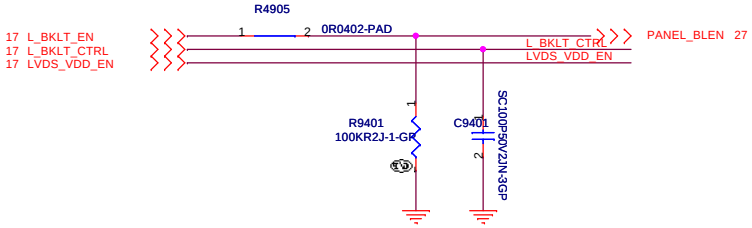


For EMI request
Close to LVDS connector

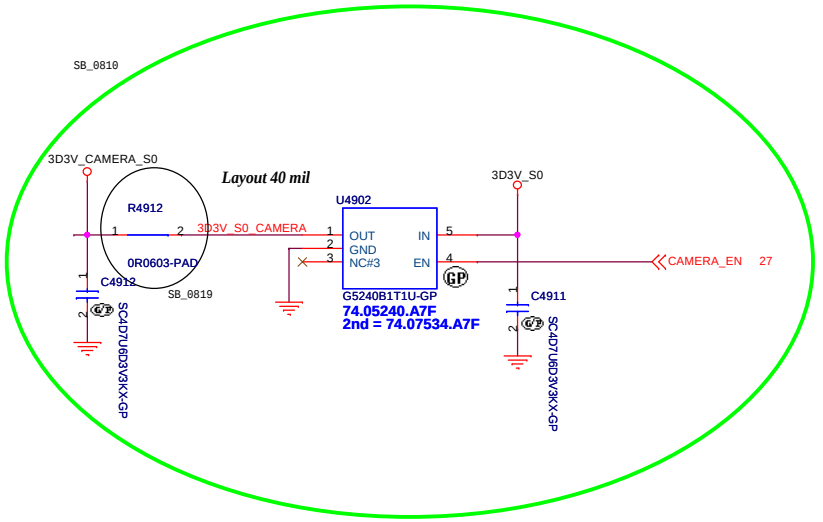




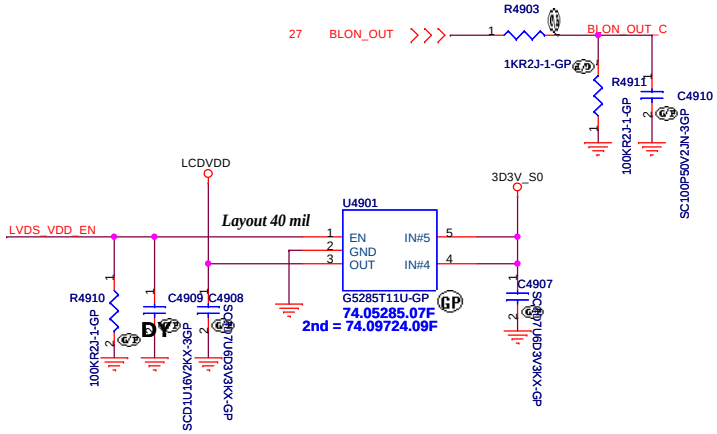
Panel BL brightness/Power En/BL En



CAMERA POWER



SSID = VIDEO



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
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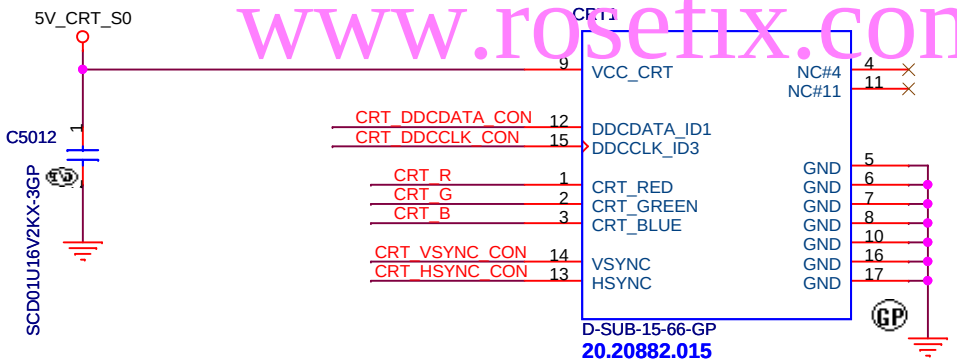
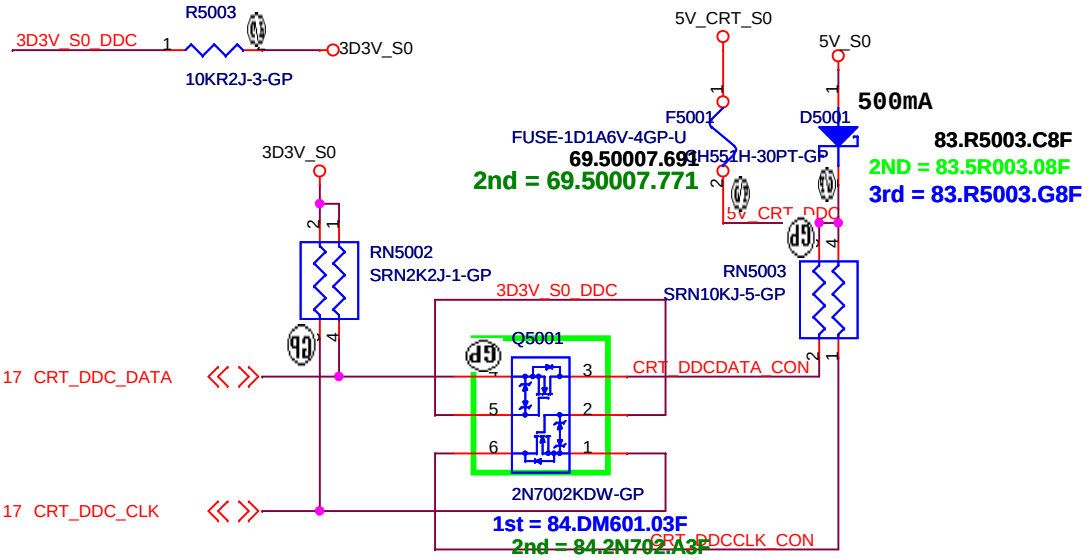
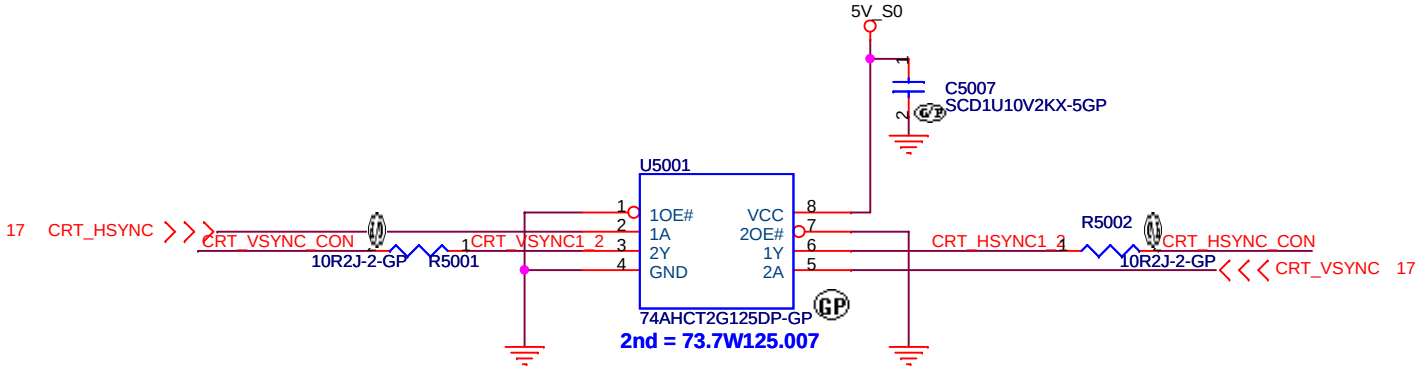


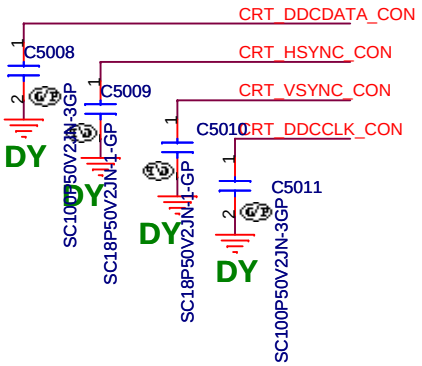
CRT DDCDATA & DDCCLK level shift

Pull High 5V Design on CRT Board

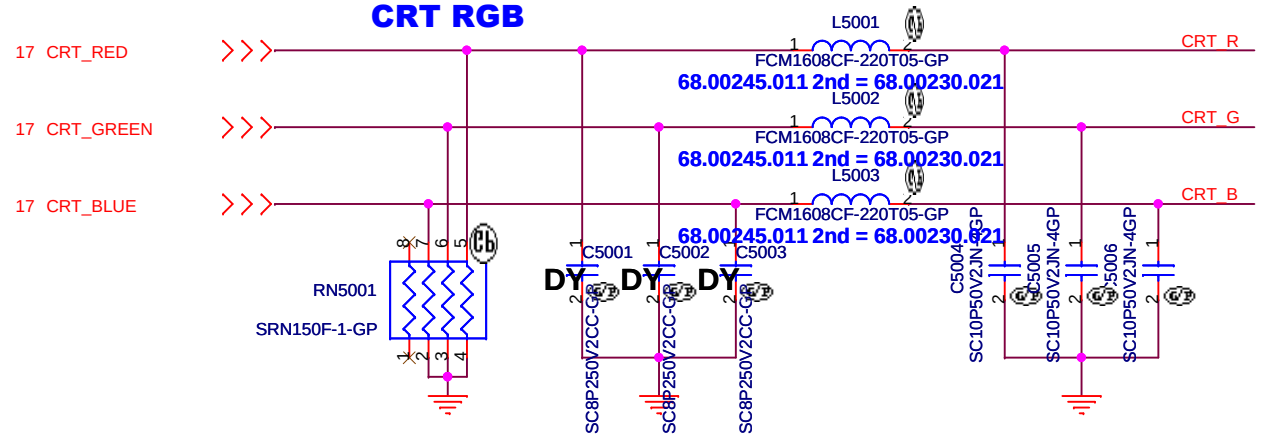


CRT Hsync & Vsync level shift





CRT RGB



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緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Connector

Size	Document Number	Rev
A4	LA470	-1

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SSID = VIDEO

HDMI CONNECTOR

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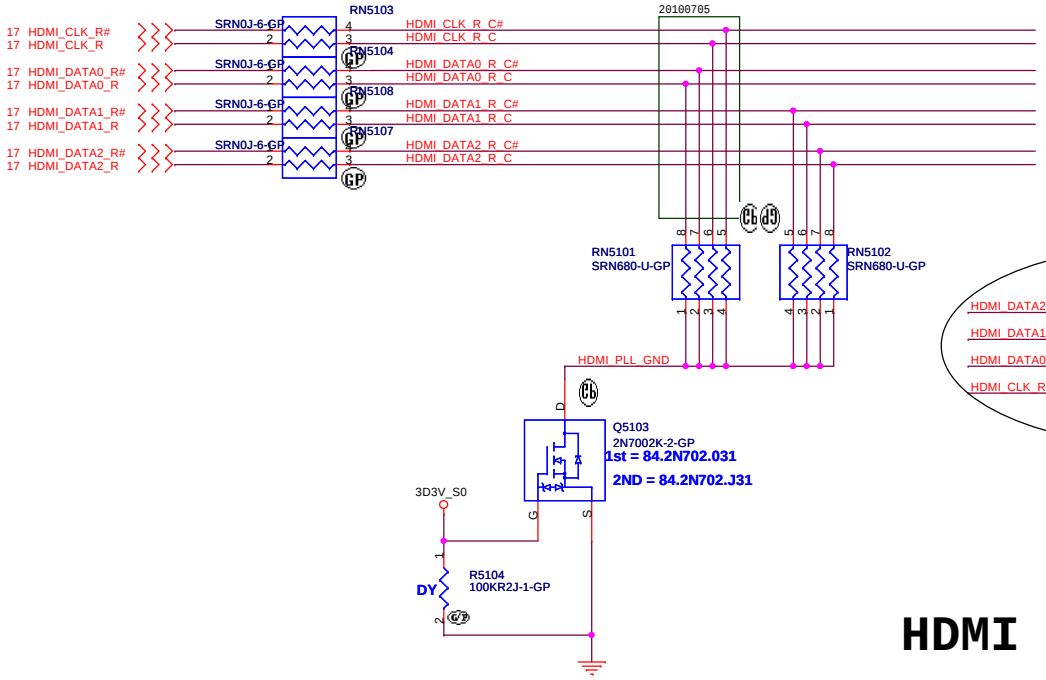
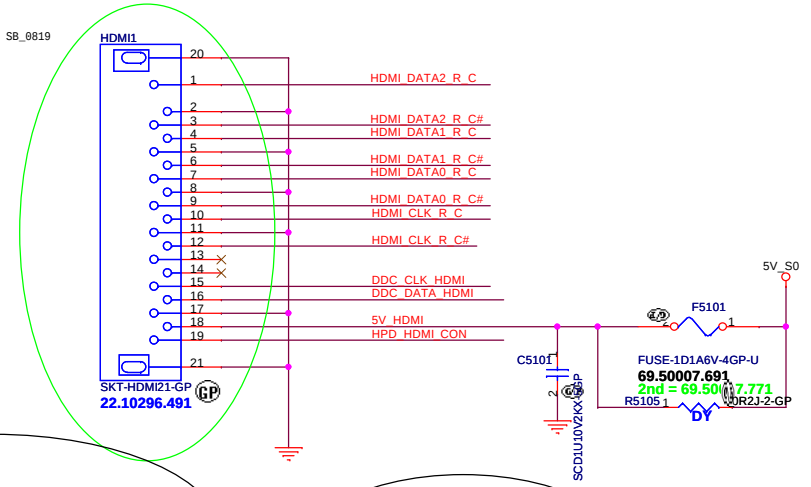
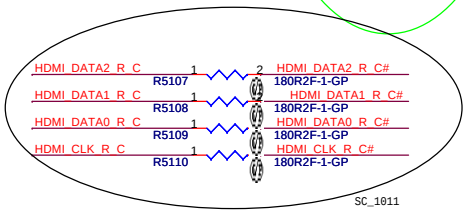
HDMI Passive Level Shifter

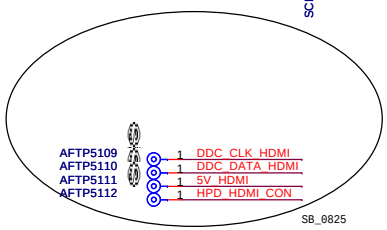
Close to HDMI Connector



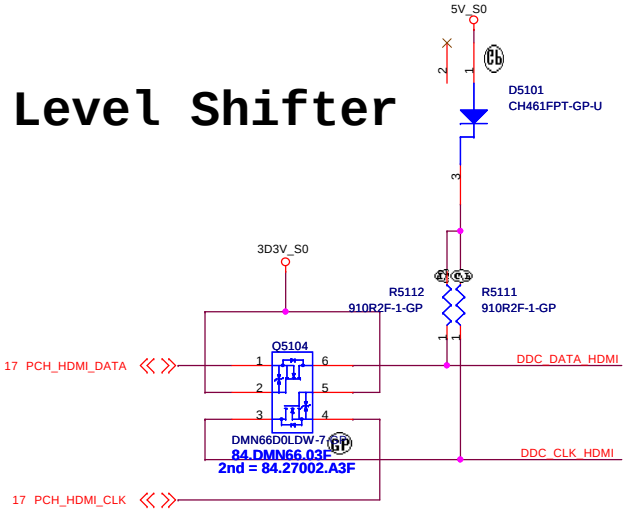
HDMI CONN

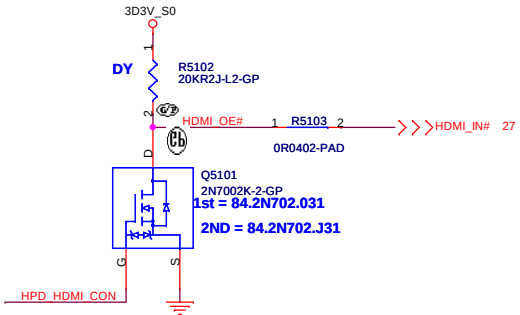


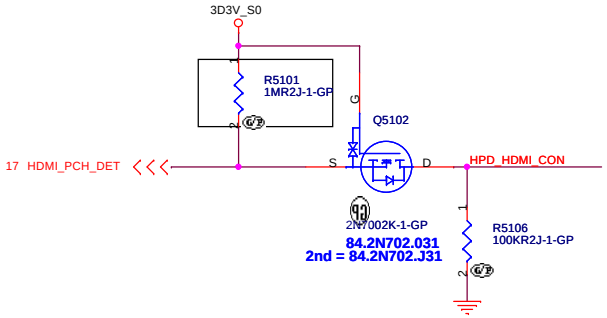




HDMI DDC Passive Level Shifter







<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	LA470	-1

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www.rosefix.com

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*

Size: A3 | Document Number: LA470 | Rev: -1

Date: Thursday, December 16, 2010 | Sheet 52 of 97

www.rosefix.com

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *S-VIDEO*

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, December 16, 2010 Sheet 53 of 97

www.rosefix.com

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	-1

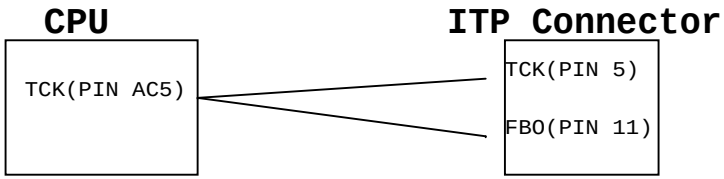
Date: Thursday, December 16, 2010 Sheet 54 of 97

www.rosefix.com

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Variant Name>

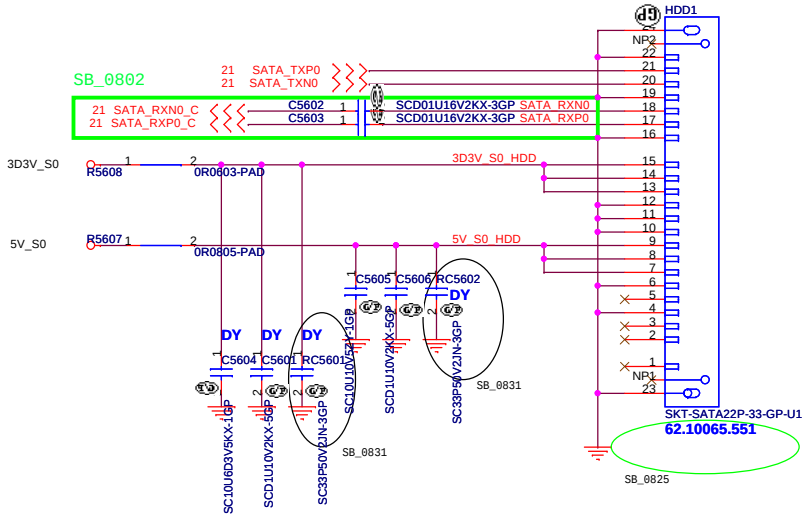
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP		
Size: A4	Document Number: LA470	Rev: -1
Date: Thursday, December 16, 2010	Sheet 55 of 97	

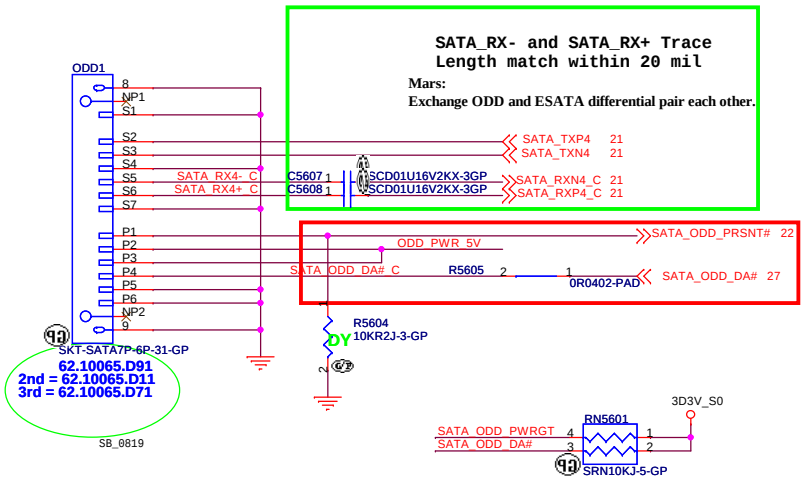
SSID = SATA

www.rosefix.com

SATA HDD Connector

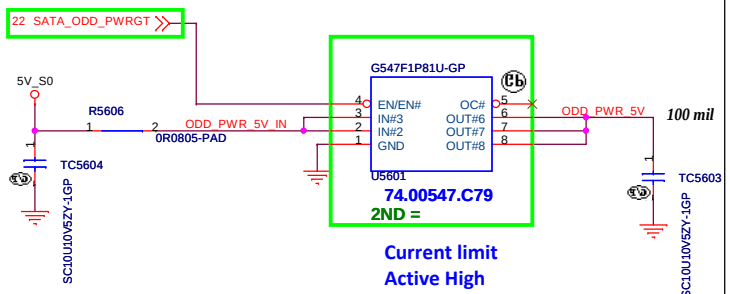


ODD Connector



SUPPORT ZERO SATA ODD

SATA Zero Power ODD



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD/ODD	
Size A3	Document Number LA470	Rev -1
Date: Thursday, December 16, 2010	Sheet 56 of 97	

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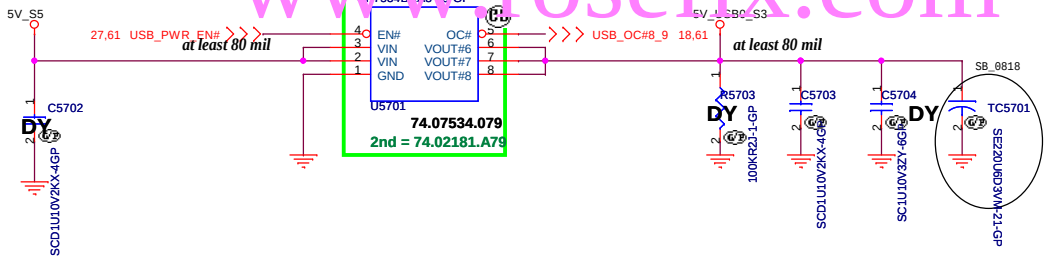
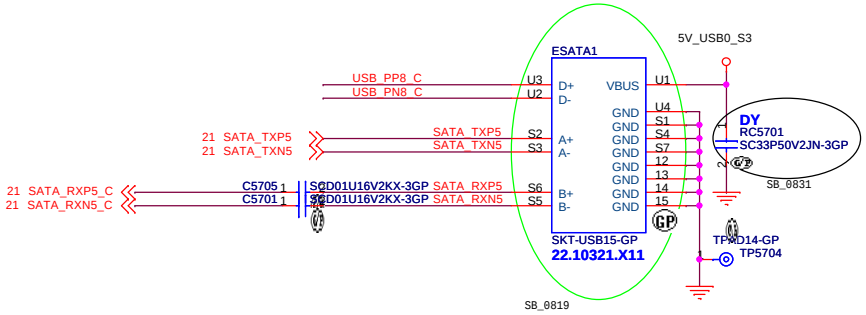
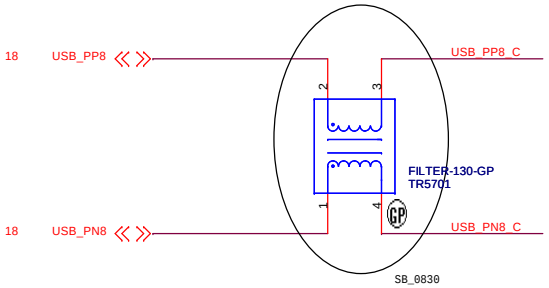
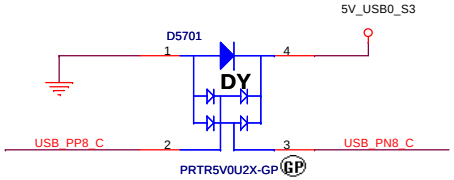
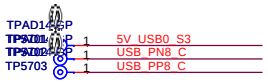
USB Power











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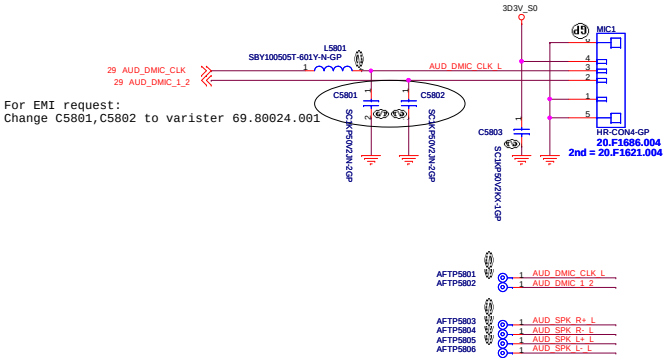
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **E-SATA**		
Size: A3	Document Number: **LA470**	Rev: **-1**
Date: Thursday, December 16, 2010	Sheet 57 of 97	

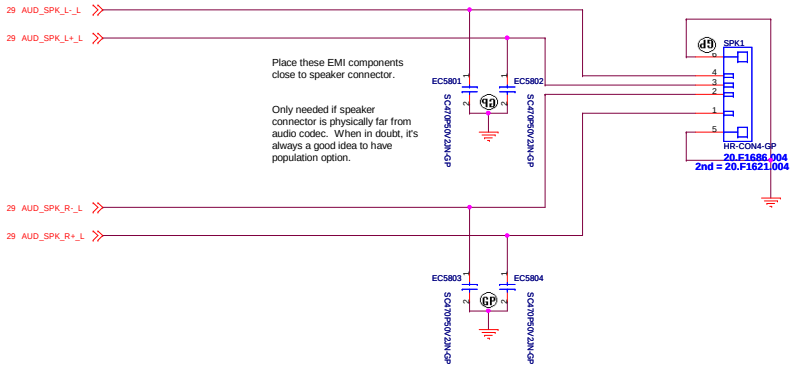
www.rosefix.com



For EMI request:
Change C5801,C5802 to varister 69.80024.001

INTERNAL STEREO SPEAKERS

Port G



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

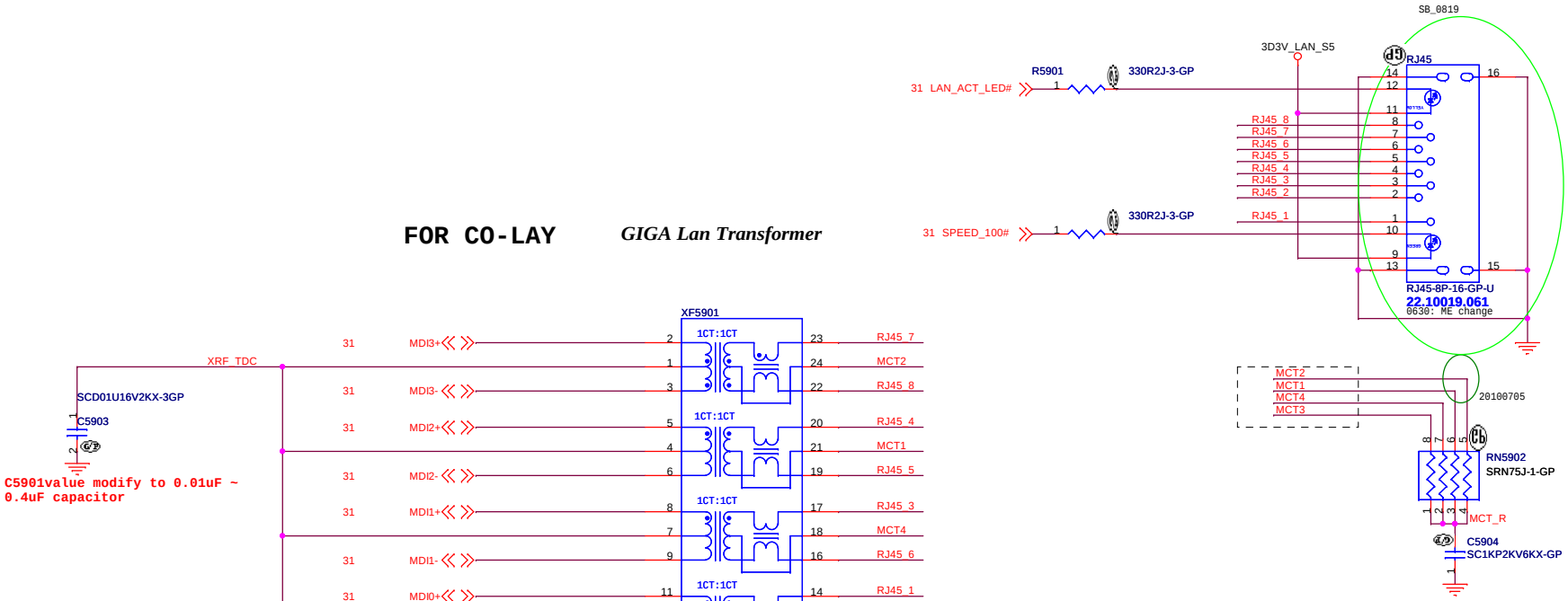
Title: MIC/SPEAKER/AUDIO JACK

Size	Document Number	Rev
A2	LA470	-1

Date: Thursday, December 16, 2010 Sheet 58 of 97

www.rosefix.com

LAN Connector



1st
68.IH601.301(Taimag) for 1000
68.HH035.301(Taimag) for 10/100
2nd
68.2413S.30A(Lankom) for 1000
68.H6441.301(Lankom) for 10/100

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45 / Transformer

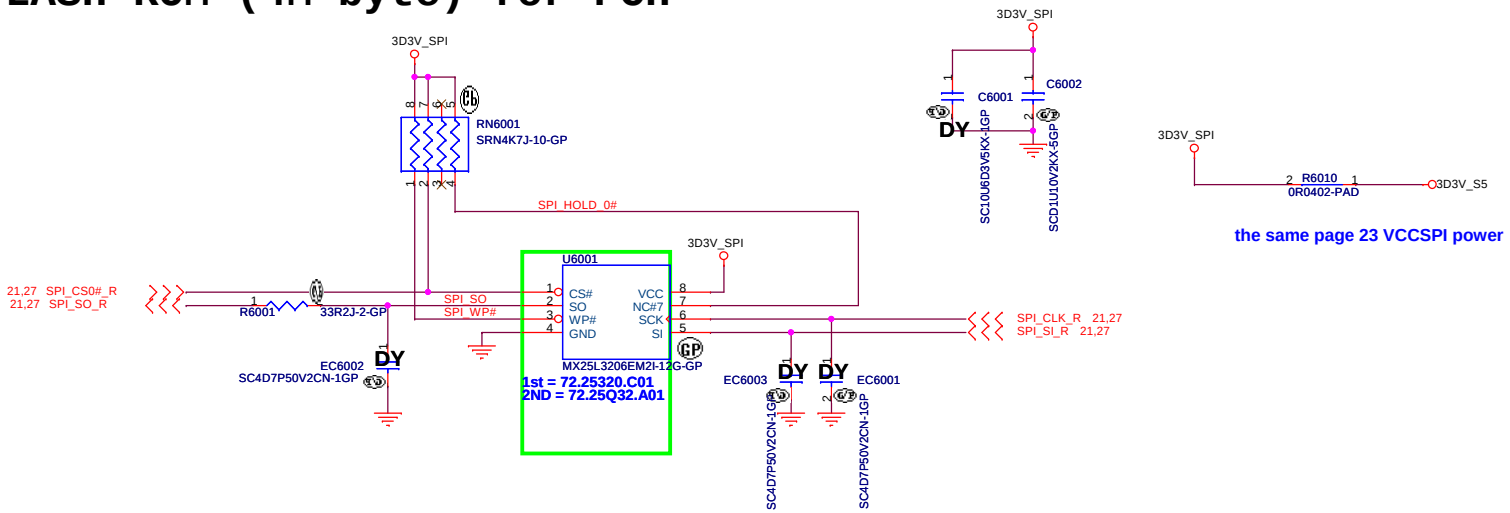
Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, December 16, 2010 Sheet 59 of 97

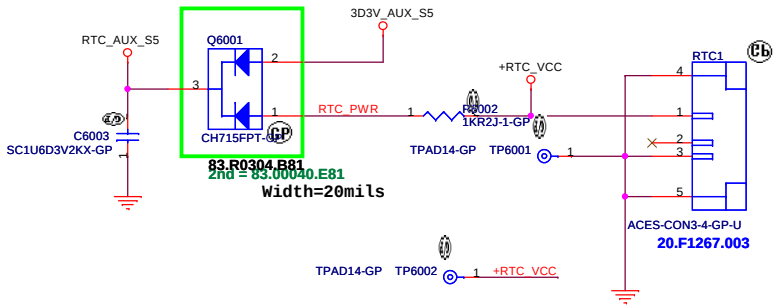
www.rosefix.com

SSID = Flash ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Flash/RTC*	
Size A3	Document Number LA470	Rev -1
Date: Thursday, December 16, 2010	Sheet 60 of 97	

SSID = USB

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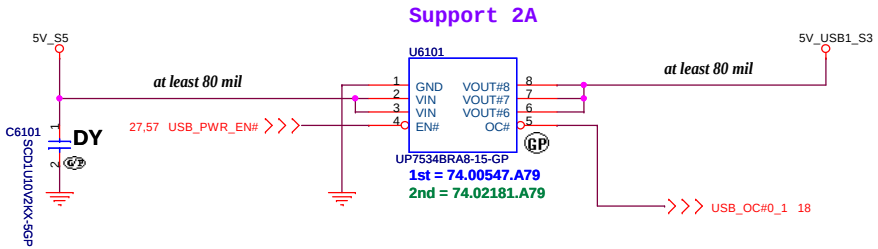
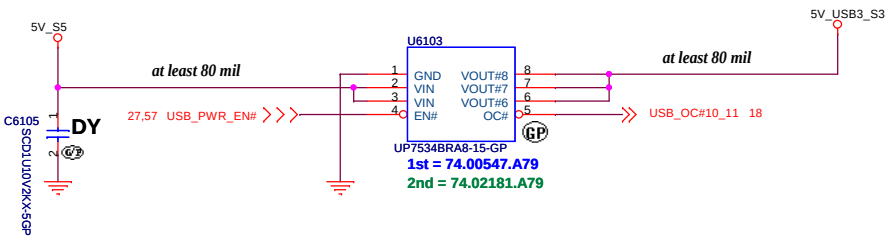
IO Board USB Power



Sub-USB Board Power



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

Size: A3 | Document Number: LA470 | Rev: -1

Date: Thursday, December 16, 2010 | Sheet 61 of 97

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(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB 3.0 Port*

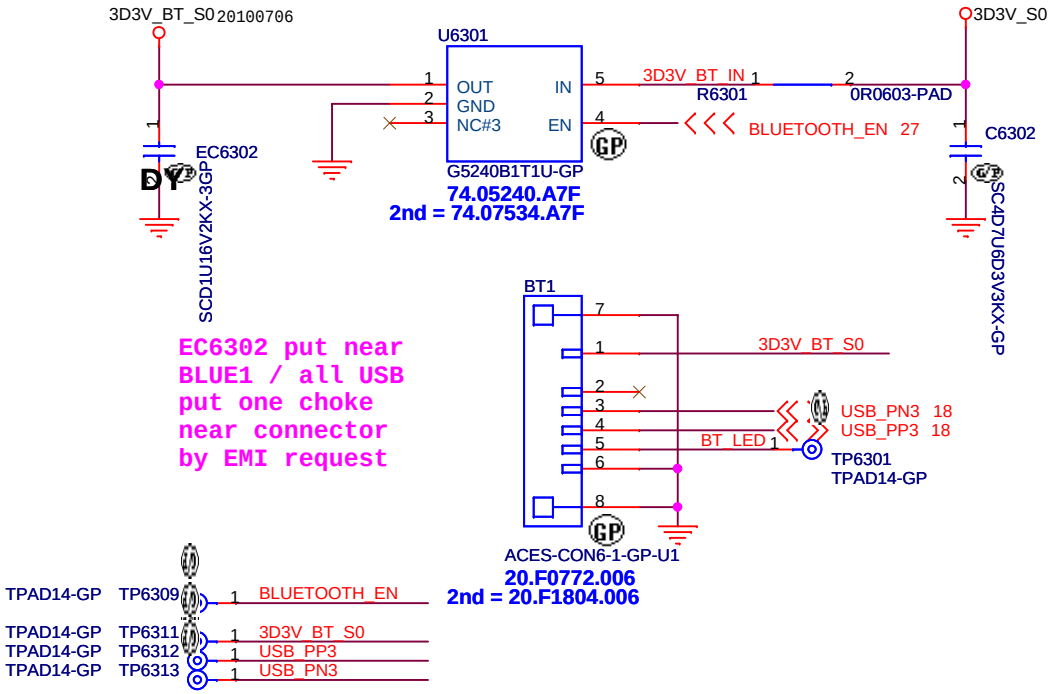
Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, December 16, 2010 Sheet 62 of 97

www.nosefix.com

SSID = Wlan.Interface
Bluetooth Module conn.

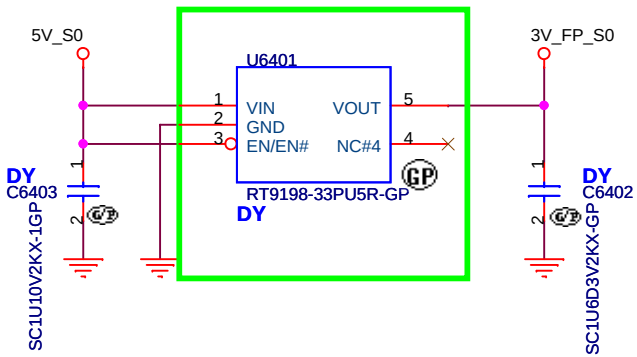
Bluetooth Module



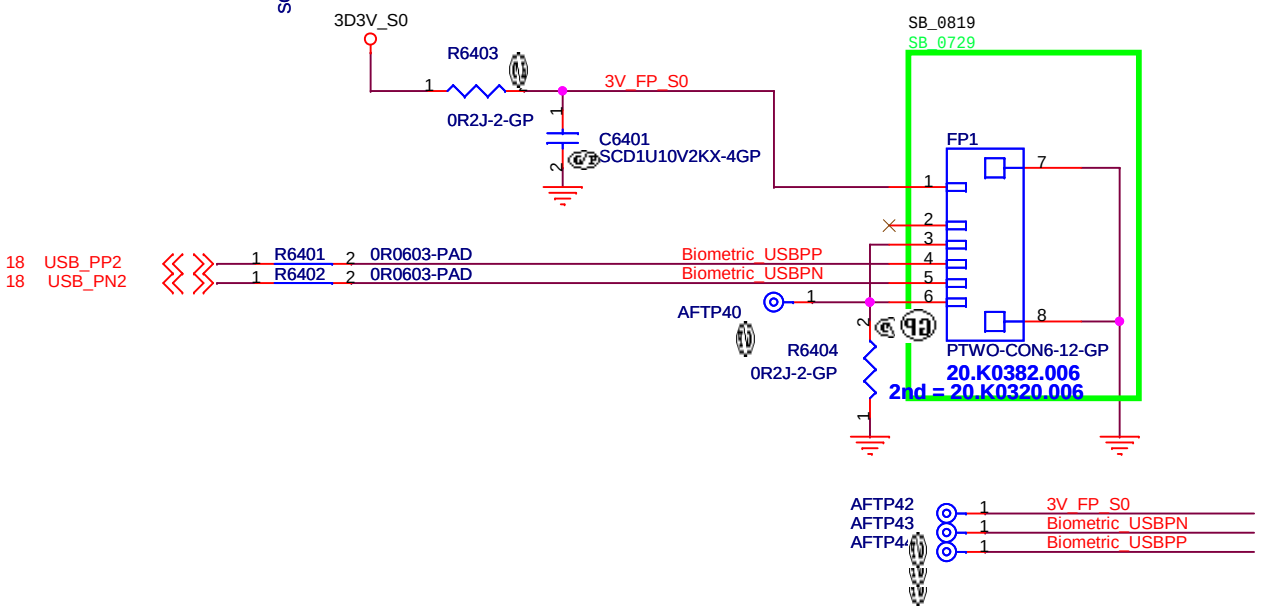
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Bluetooth***	
Size A4	Document Number **LA470**	Rev **-1**
Date: Thursday, December 16, 2010	Sheet 63 of 97	

www.rosefix.com



Finger Printer Connector



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

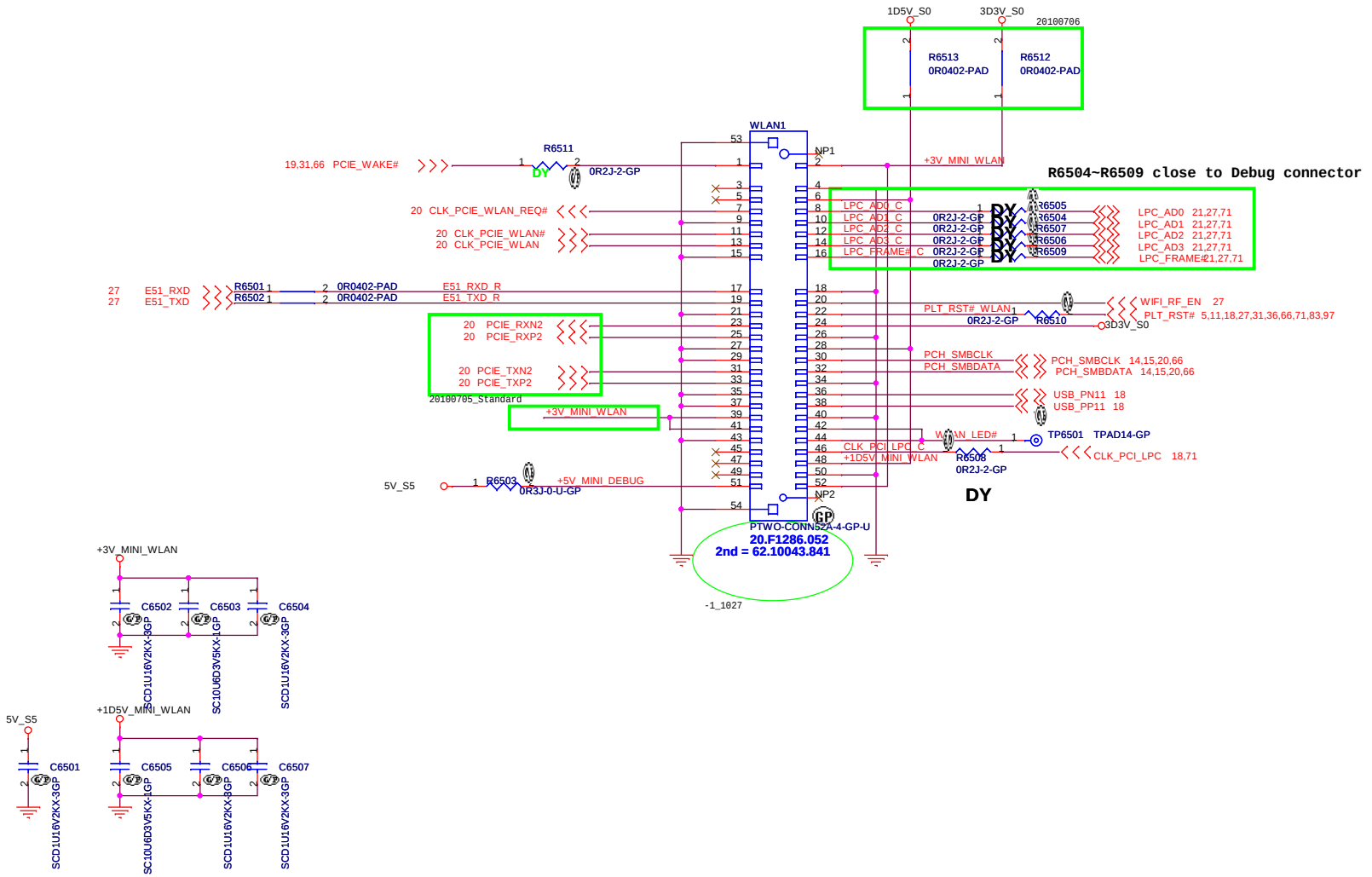
Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, December 16, 2010 Sheet 64 of 97

SSID = Wireless

www.rosefix.com

Mini Card Connector(802.11a/b/g/n)



<Variant Name>

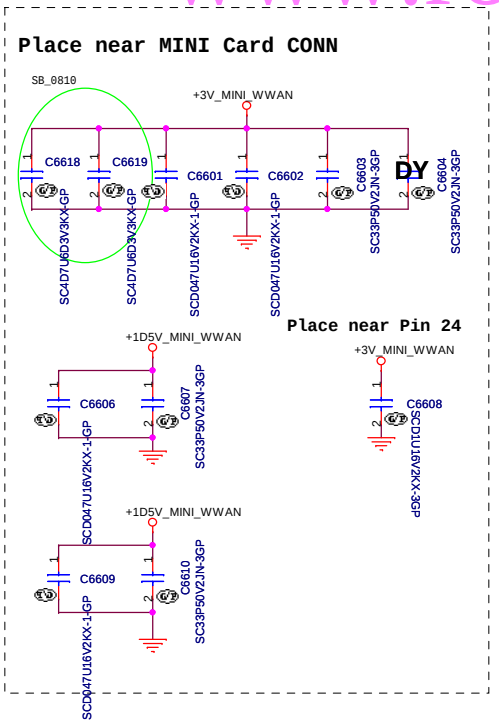
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

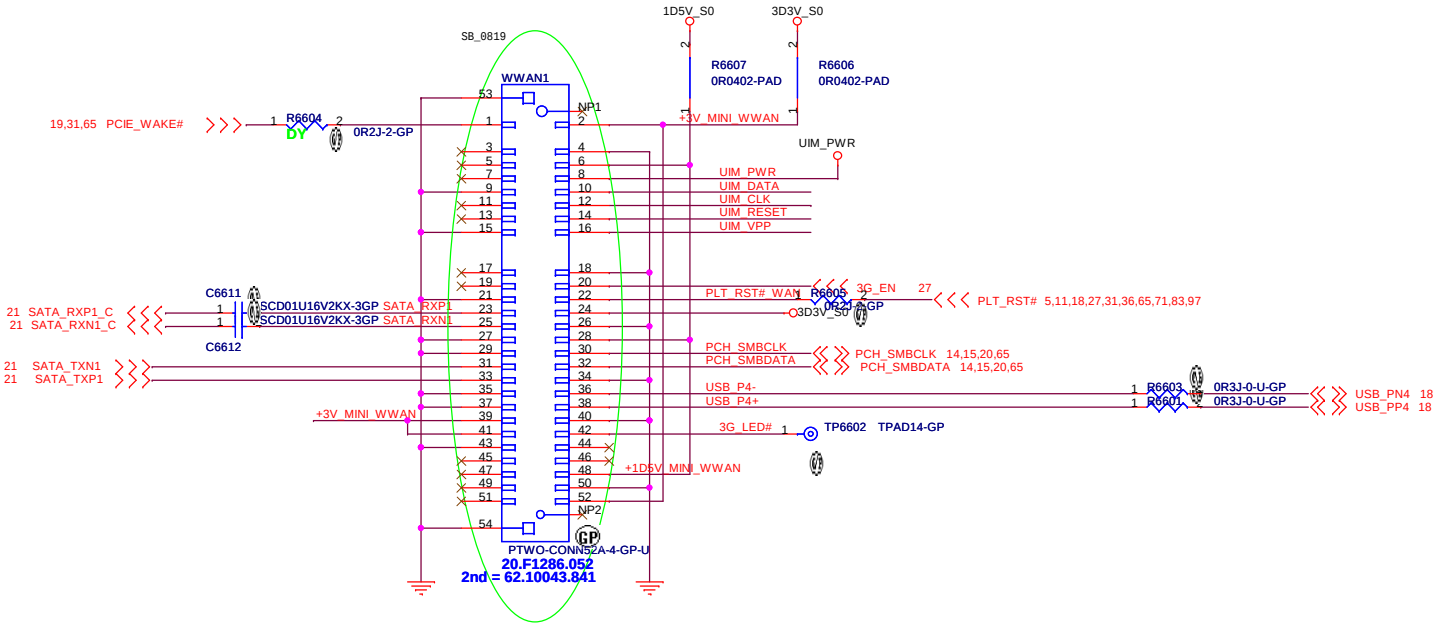
Title	MINICARD(WLAN)/ITP CONN	
Size A3	Document Number LA470	Rev -1
Date: Thursday, December 16, 2010	Sheet 65 of 97	

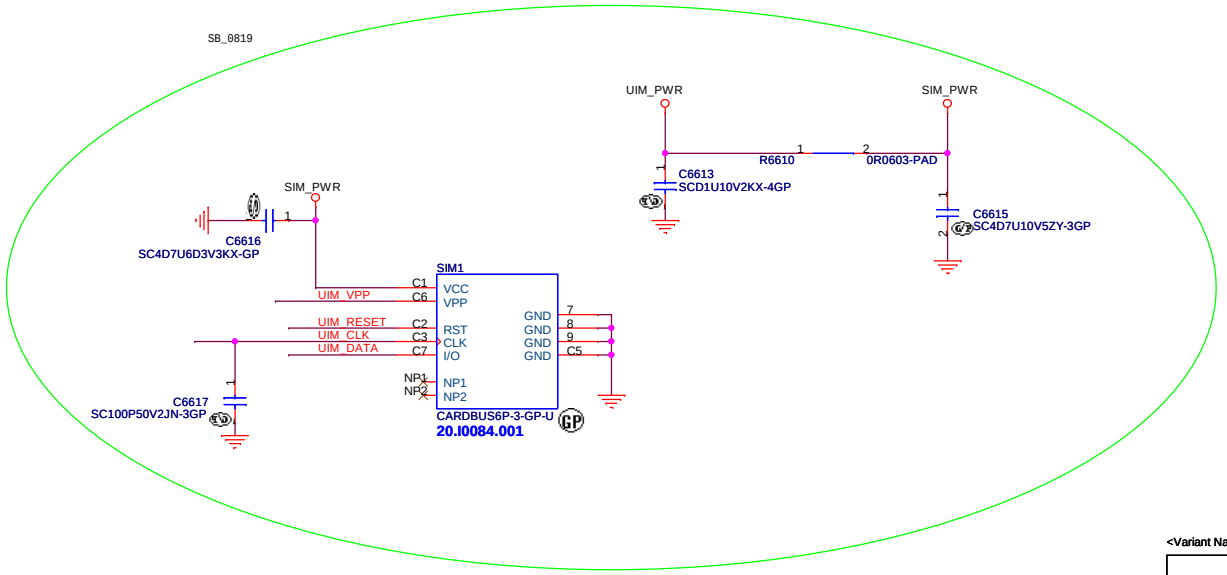
SSID = Wireless

www.rosefix.com

Mini Card Connector(WWAN)







<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size	Document Number	Rev
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Date: Thursday, December 16, 2010 Sheet 66 of 97

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
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Date: Thursday, December 16, 2010 Sheet 67 of 97

SSID = User.Interface

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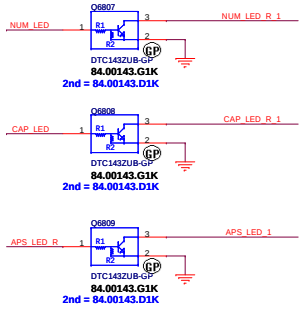
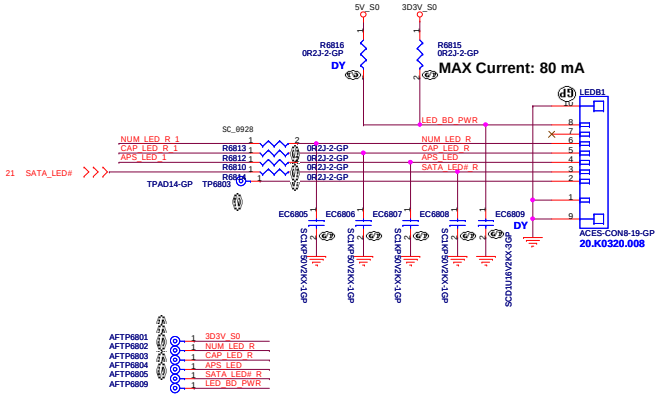
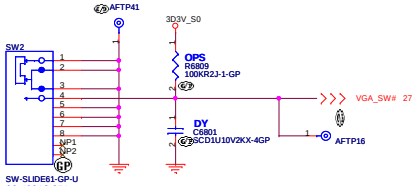
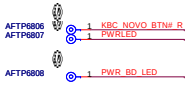
Power button LED



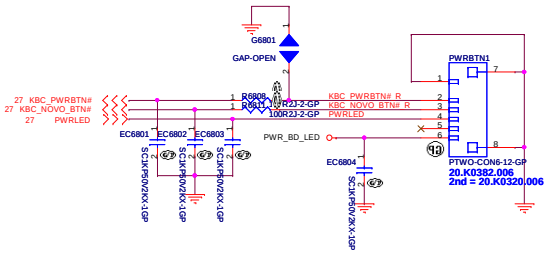
LED Bord CONN.

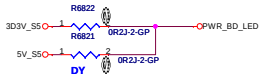


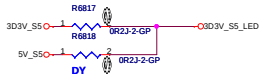


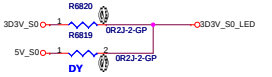


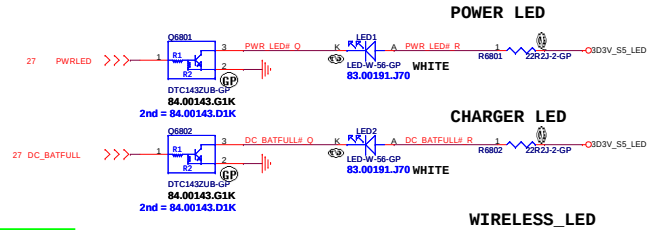
Power button LED(White)











bom LA47

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size	Document Number	Rev
A2	LA470	-1

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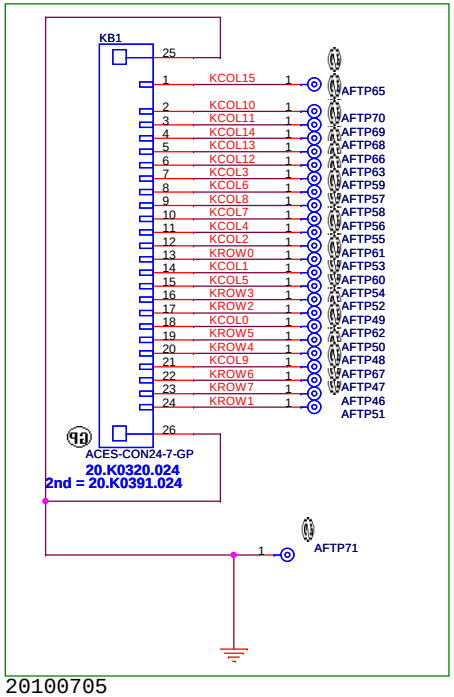
SSID = KBC

Internal KeyBoard Connector



KROW[0..7] 27

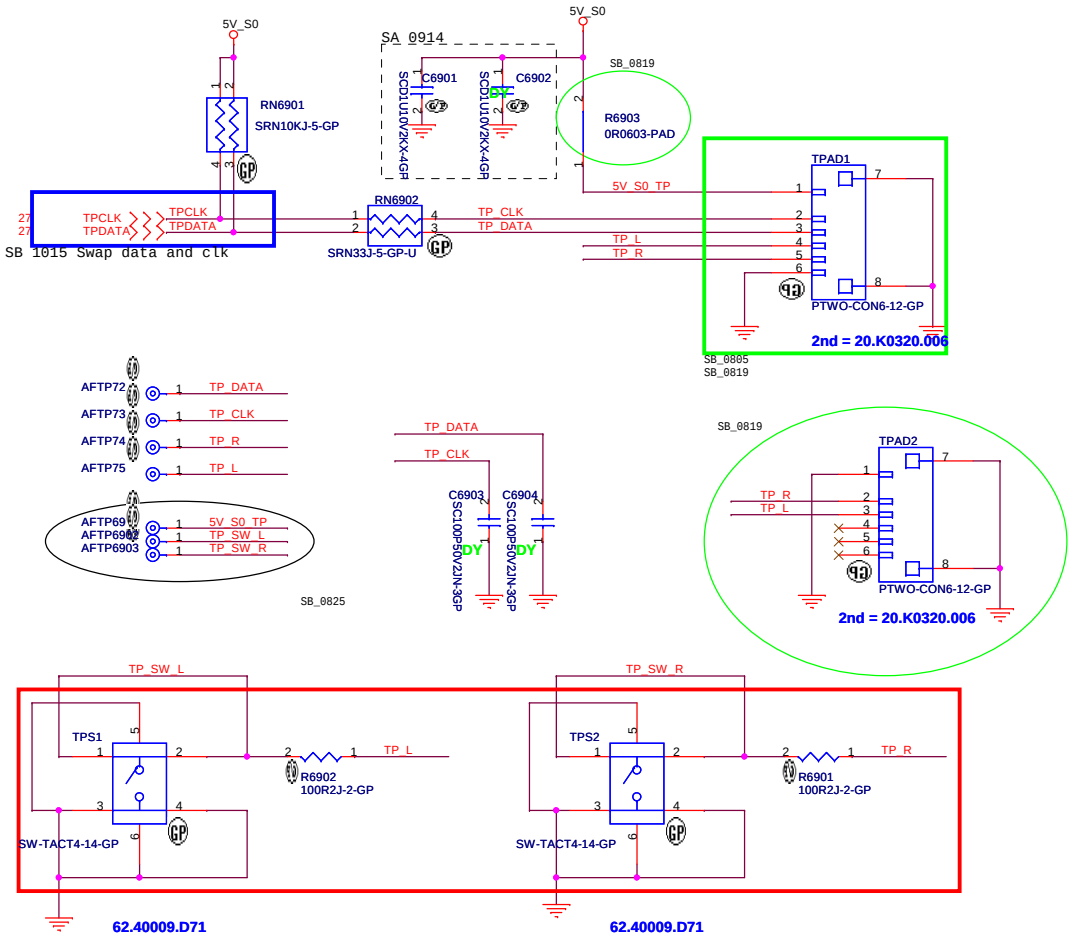
KCOL[0..15] 27

20100705

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

SSID = Touch.Pad



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
A3	LA470	-1

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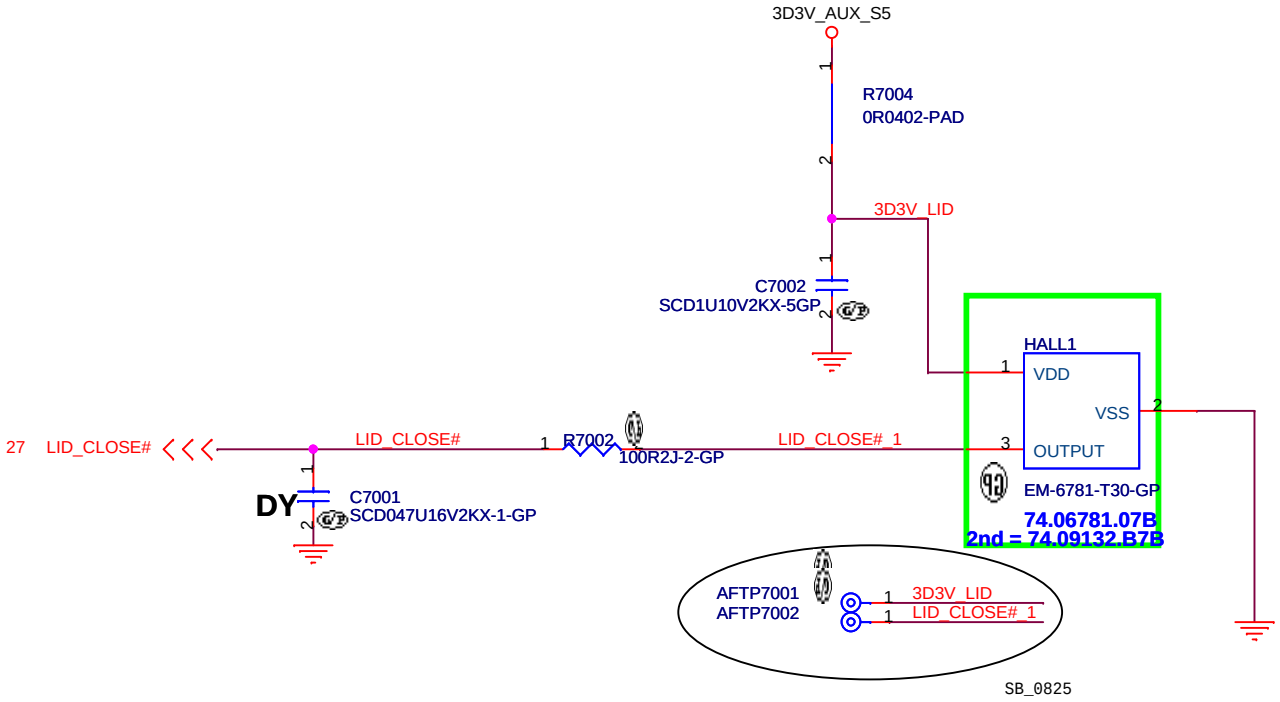
www.rosefix.com



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Hall Sensor

Size	Document Number	Rev
A4	LA470	-1

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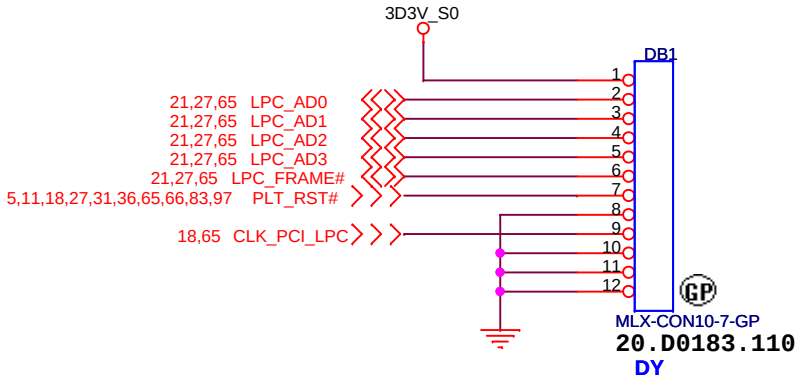
www.rosefix.com



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	LA470	-1

Date: Thursday, December 16, 2010 Sheet 71 of 97

www.rosefix.com

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A3	LA470	-1

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www.rosefix.com

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size	Document Number	Rev
A3	LA470	-1

Date: Thursday, December 16, 2010 Sheet 74 of 97

www.rosefix.com

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***New Card***		
Size: A3	Document Number: **LA470**	Rev: **-1**
Date: Thursday, December 16, 2010	Sheet 75 of 97	

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
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(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

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(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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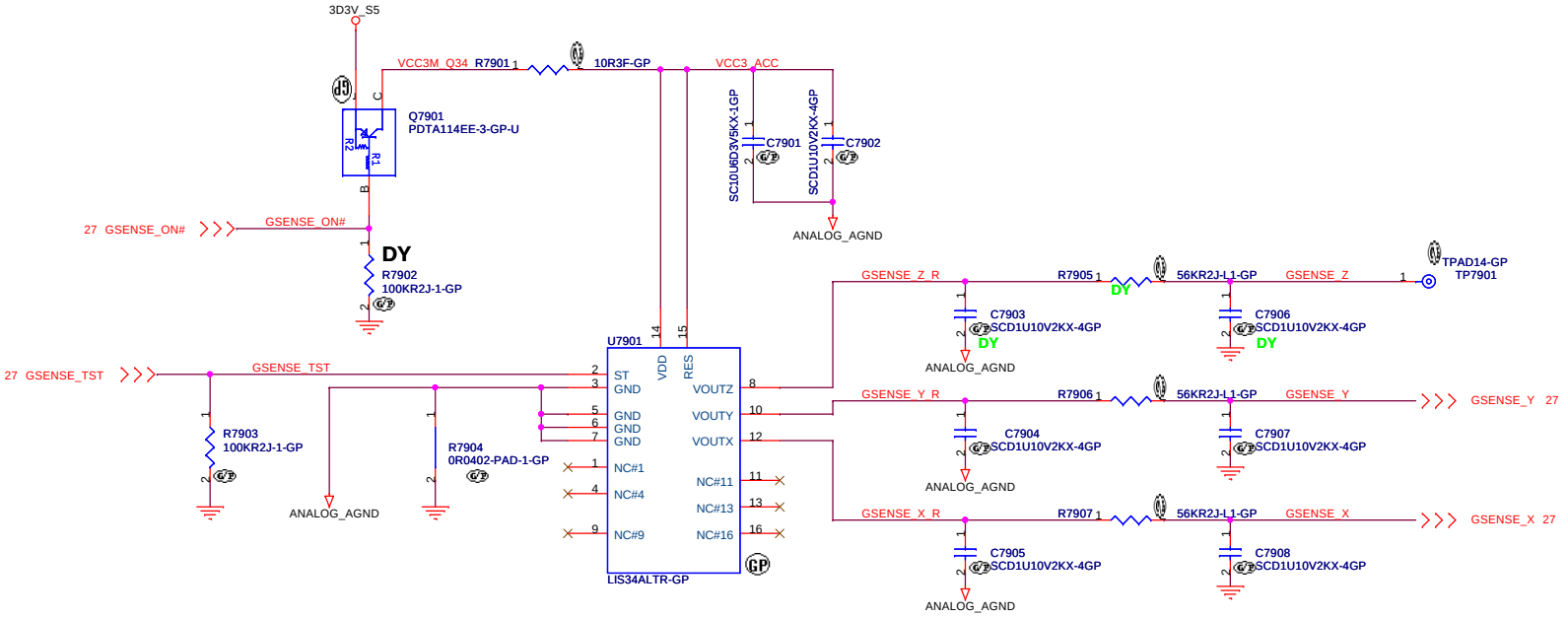
www.rosefix.com

G-Sensor



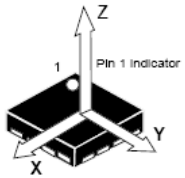
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **G-Sensor**

Size: Custom | Document Number: **LA470** | Rev: **-1**

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(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
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(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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Date: Thursday, December 16, 2010 Sheet 81 of 97

IO Board CONN 80 pin

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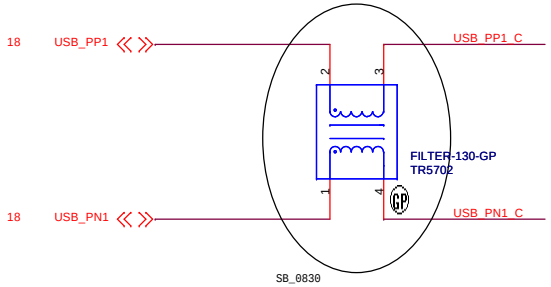
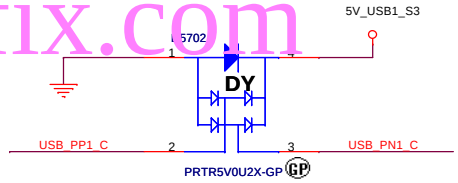
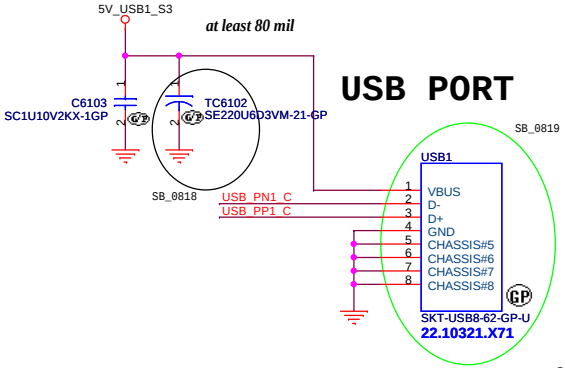
USB1



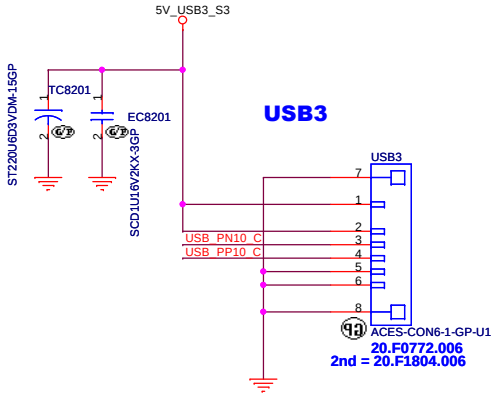


USB PORT

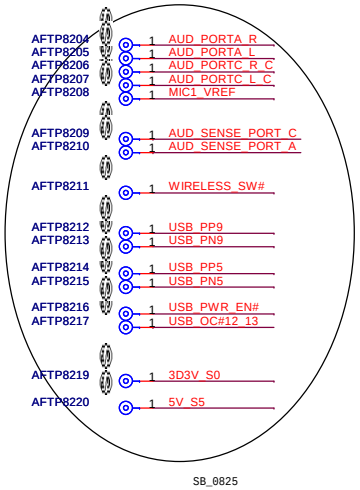


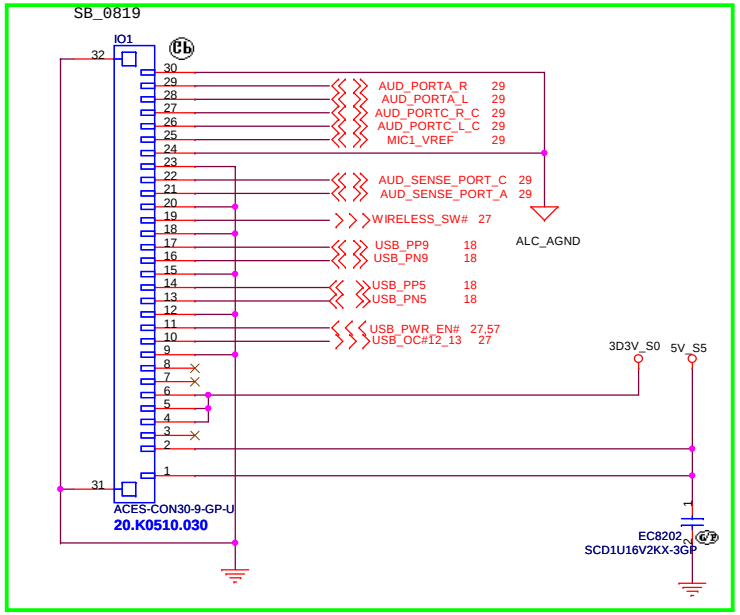
Mars:
Exchange ODD and ESATA differential pair each other.

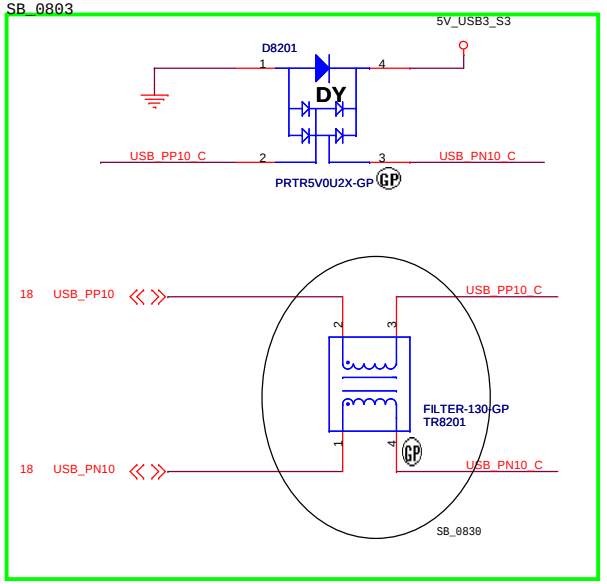
USB Board CONN.

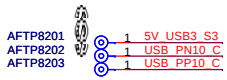


I/O Board CONN.









<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	IO Board Connector	
Size A3	Document Number LA470	Rev -1
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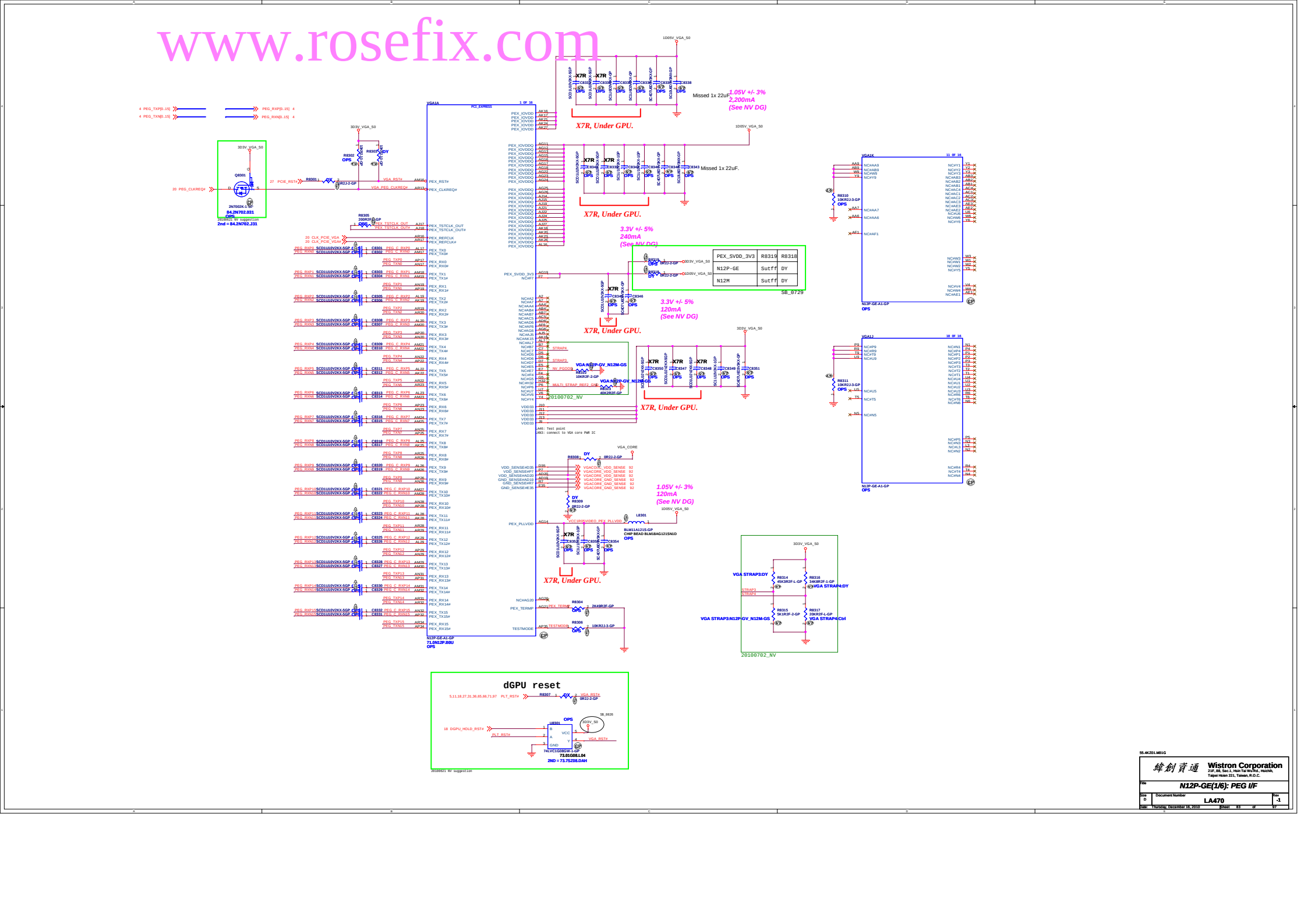

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Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	N12P-GE(1/6): PEG I/F
Size: D	Document Number: LA470
Rev: -1	
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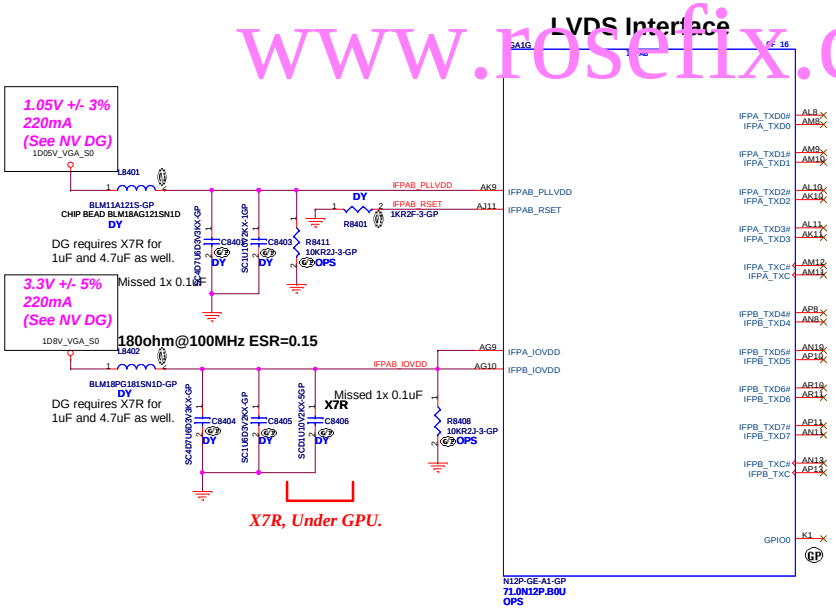
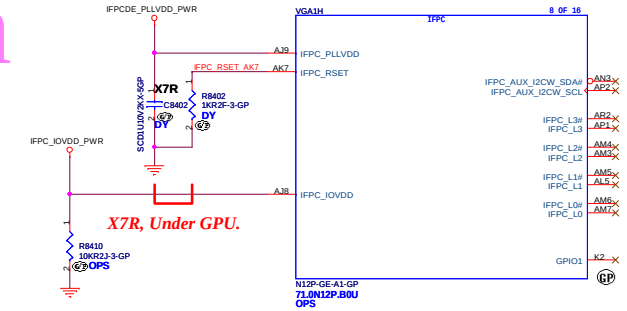
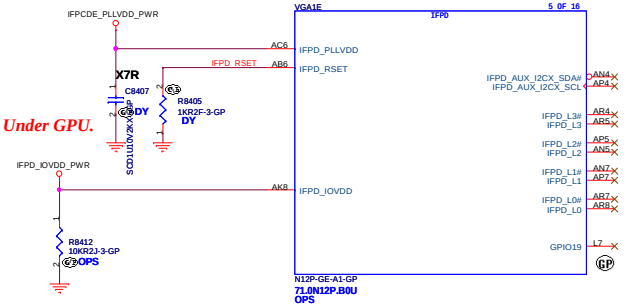
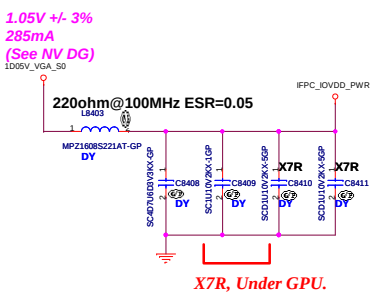
LVDS Interface

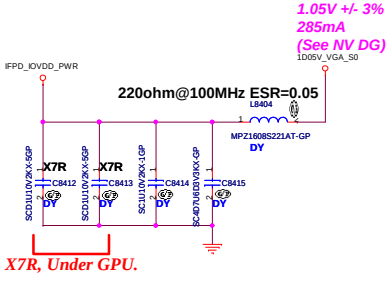


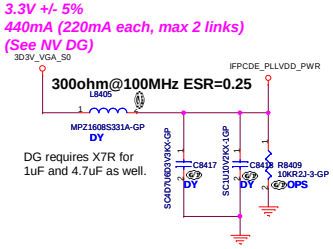


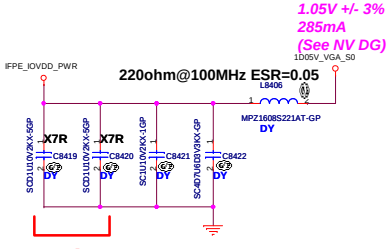
HDMI Interface

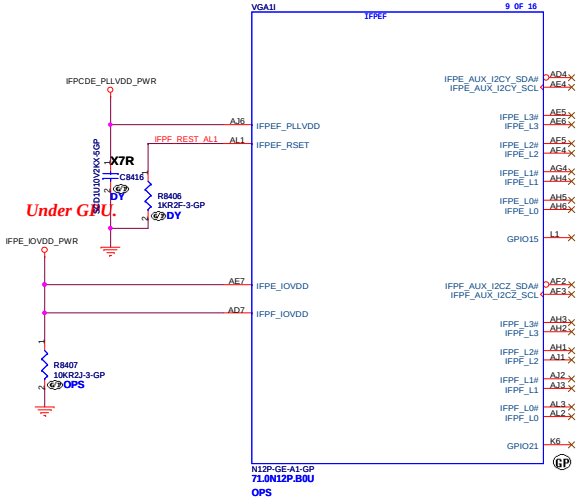












<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N12P-Q1/Q3 (2/6): DIGITAL OUT

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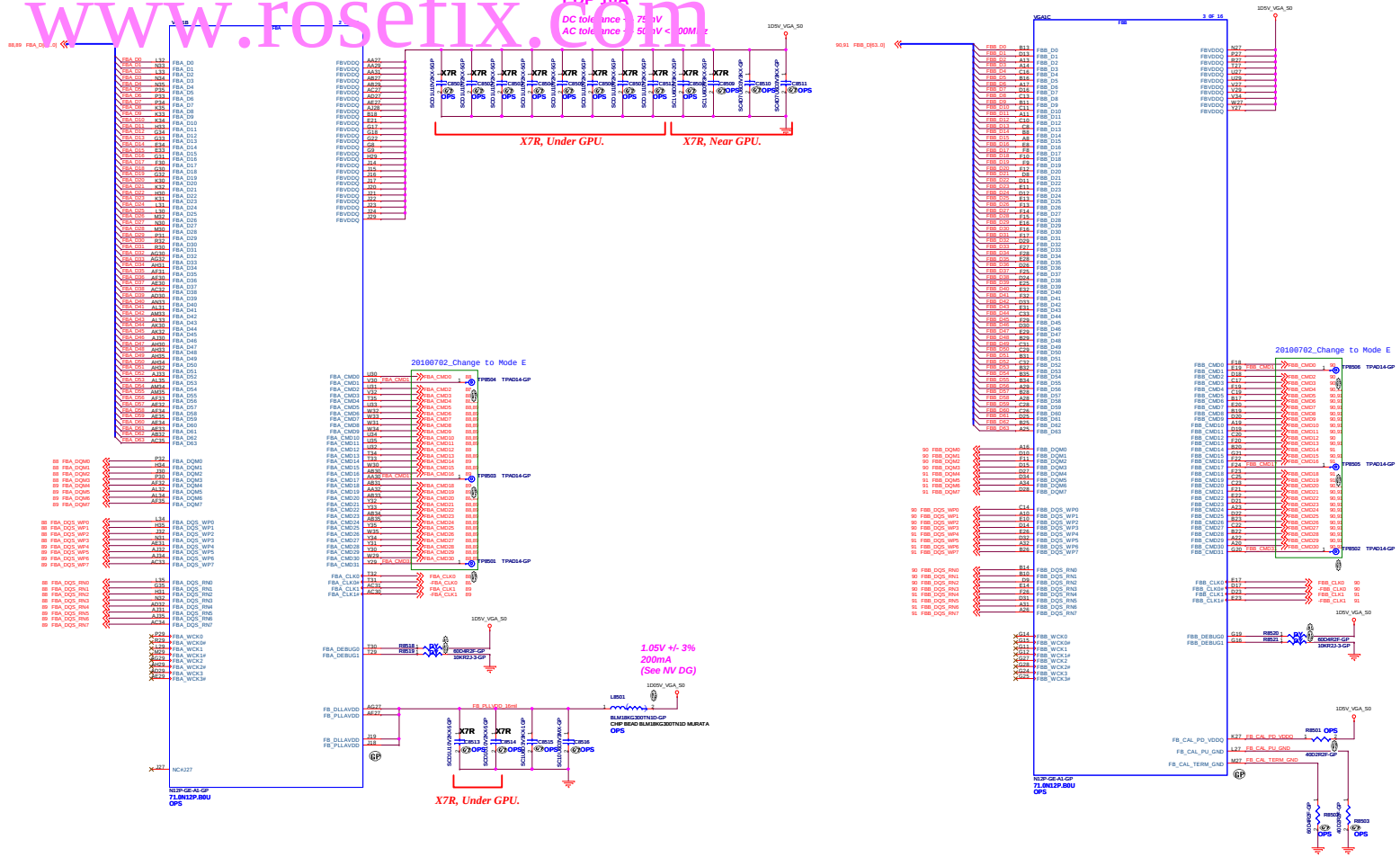
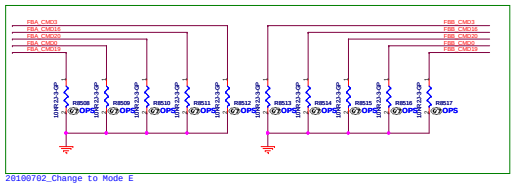


FBCLK Termination place on VRAM side

FBCLK Termination	R8504~R8507
N12P	Sutff 162 ohm 64.16205.6DL
N12M-GE only	Stuff 243 ohm 64.24305.6DL



FBCLK Termination place on VRAM side

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: N12P-Q1/Q3 (3/6): VRAM I/F
Size: A1 | Document Number: LA470 | Rev: -1
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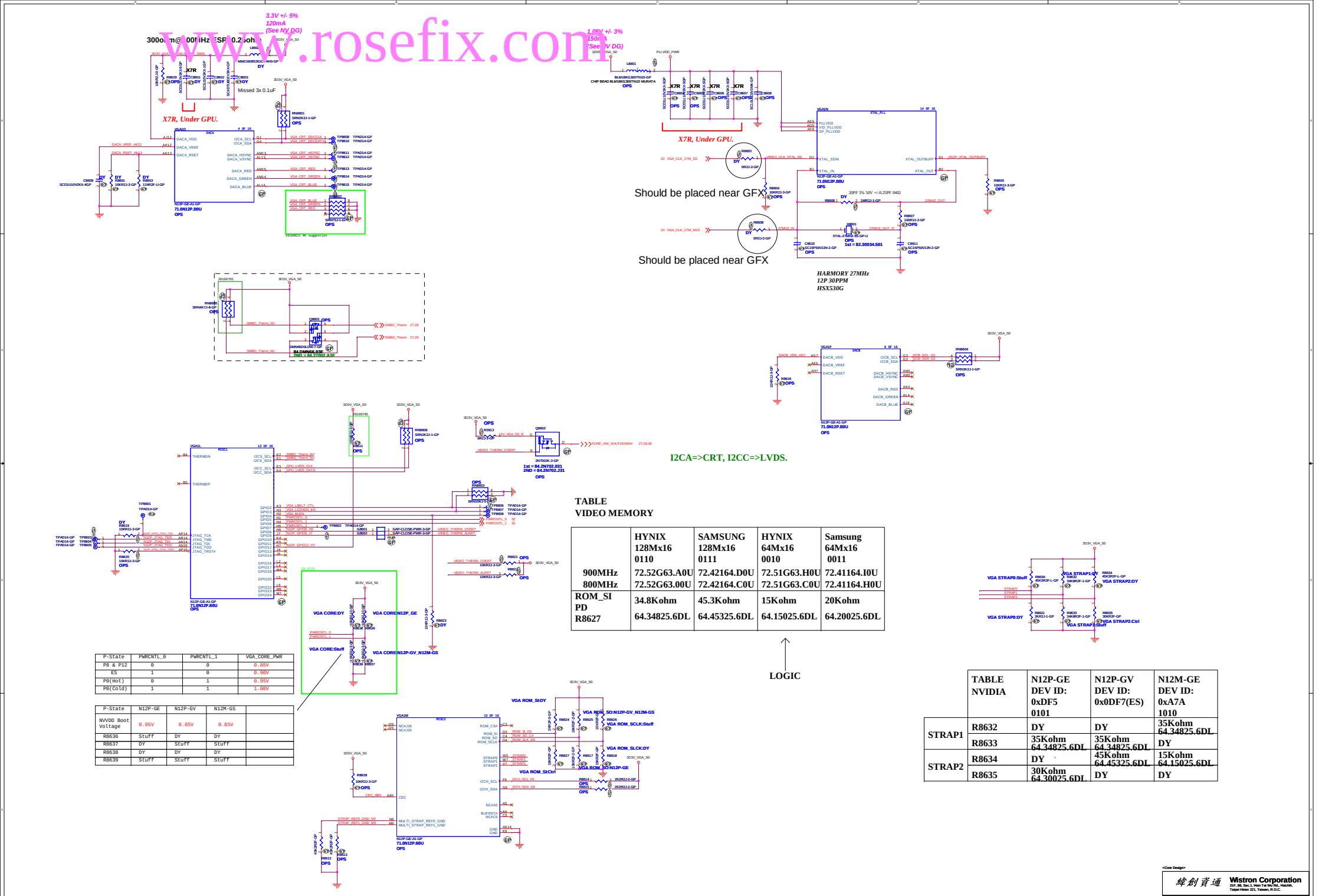

TABLE
VIDEO MEMORY

	HYNIX 128Mx16 0110	SAMSUNG 128Mx16 0111	HYNIX 64Mx16 0010	Samsung 64Mx16 0011
900MHz	72.52G63.A0U	72.42164.D0U	72.51G63.H0U	72.41164.I0U
800MHz	72.52G63.00U	72.42164.C0U	72.51G63.C0U	72.41164.H0U
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

P-State	PWRCNTL_0	PWRCNTL_1	VGA_CORE_PWR
P8 & P12	0	0	0.85V
ES	1	0	0.90V
P0(Hot)	0	1	0.95V
P0(Cold)	1	1	1.00V

P-State	N12P-GE	N12P-GV	N12M-GS	
NVVDD Boot Voltage	0.95V	0.85V	0.85V	
R8636	Stuff	DY	DY	
R8637	DY	Stuff	Stuff	
R8638	DY	DY	DY	
R8639	Stuff	Stuff	Stuff	

TABLE NVIDIA	N12P-GE DEV ID: 0xDF5 0101	N12P-GV DEV ID: 0x0DF7(ES)	N12M-GE DEV ID: 0xA7A 1010
STRAP1	R8632	DY	DY	35Kohm 64.34825.6DL
	R8633	35Kohm 64.34825.6DL	35Kohm 64.34825.6DL	DY
STRAP2	R8634	DY	45Kohm 64.45325.6DL	15Kohm 64.15025.6DL
	R8635	30Kohm 64.30025.6DL	DY	DY

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Title: N12P-Q1/Q3 (4/6): GPIO
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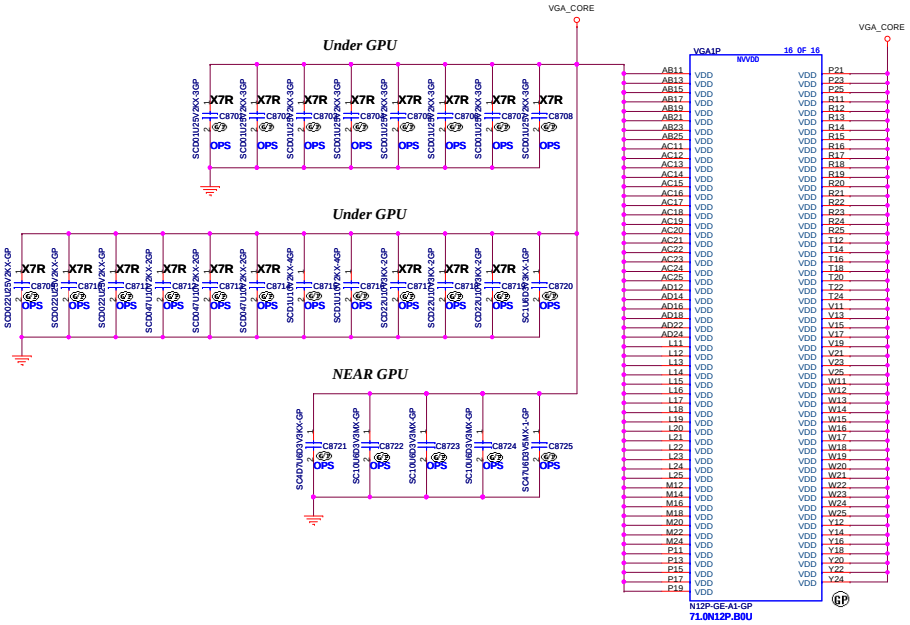

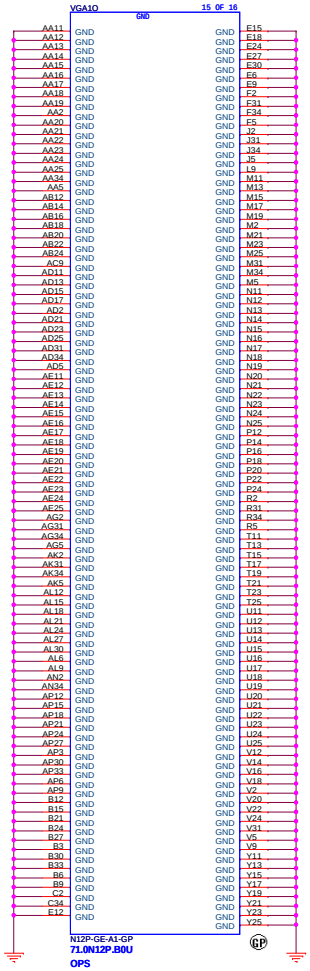

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N12P-Q1/Q3 (5/6): POWER

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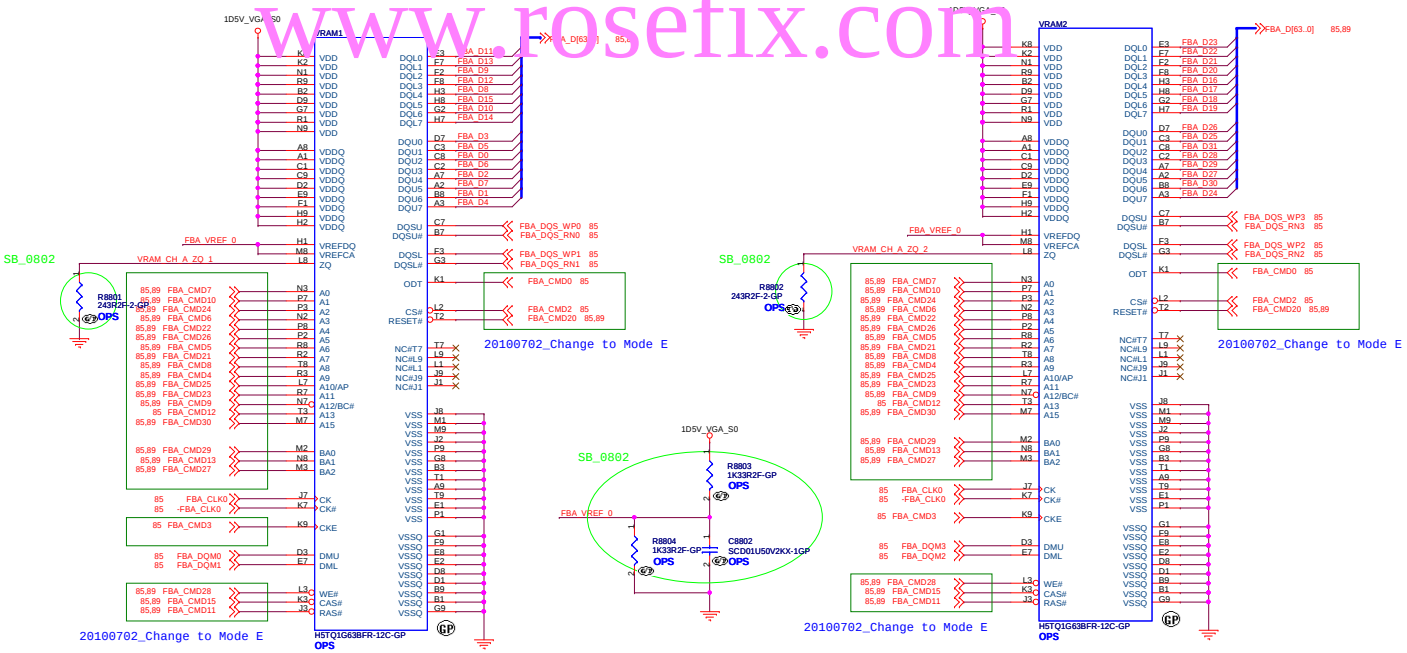
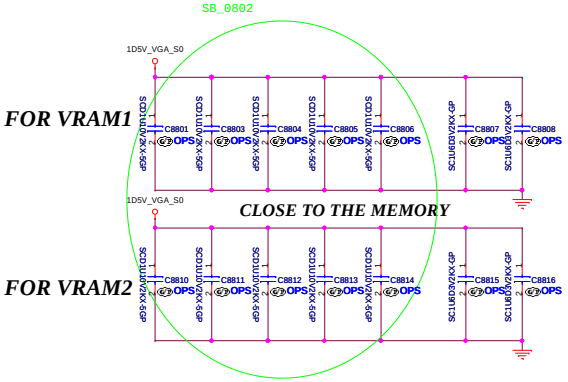
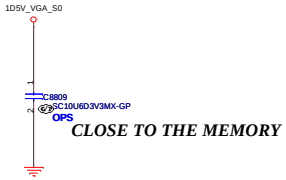


FB CMD mapping Mode D-N12x



DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VIDEO FRAME BUFFER PORT A

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM CHANNEL-A**

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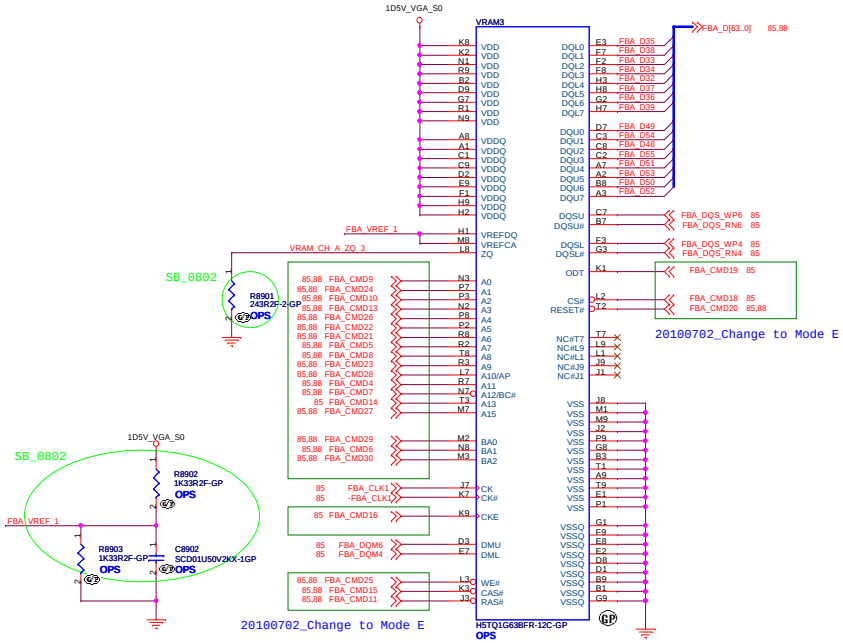
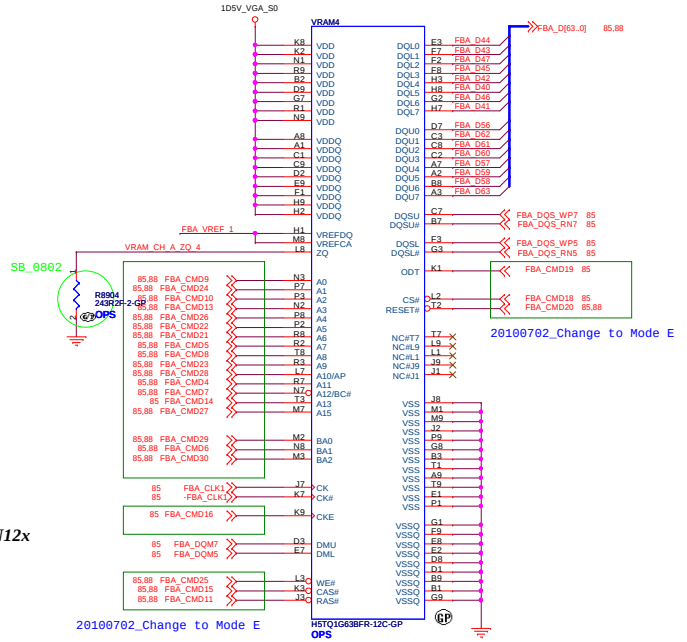
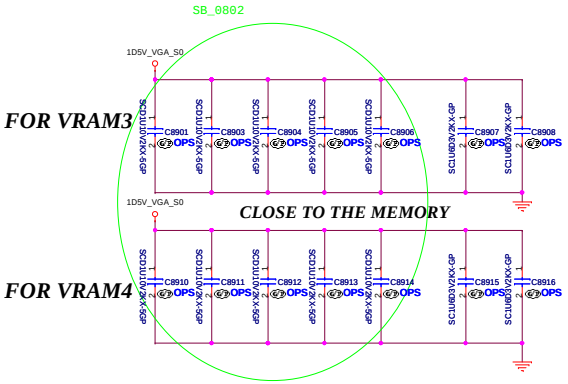


FB CMD mapping Mode D-N12x

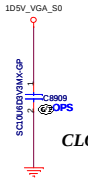




FOR VRAM3

FOR VRAM4

CLOSE TO THE MEMORY



CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM CHANNEL-A**

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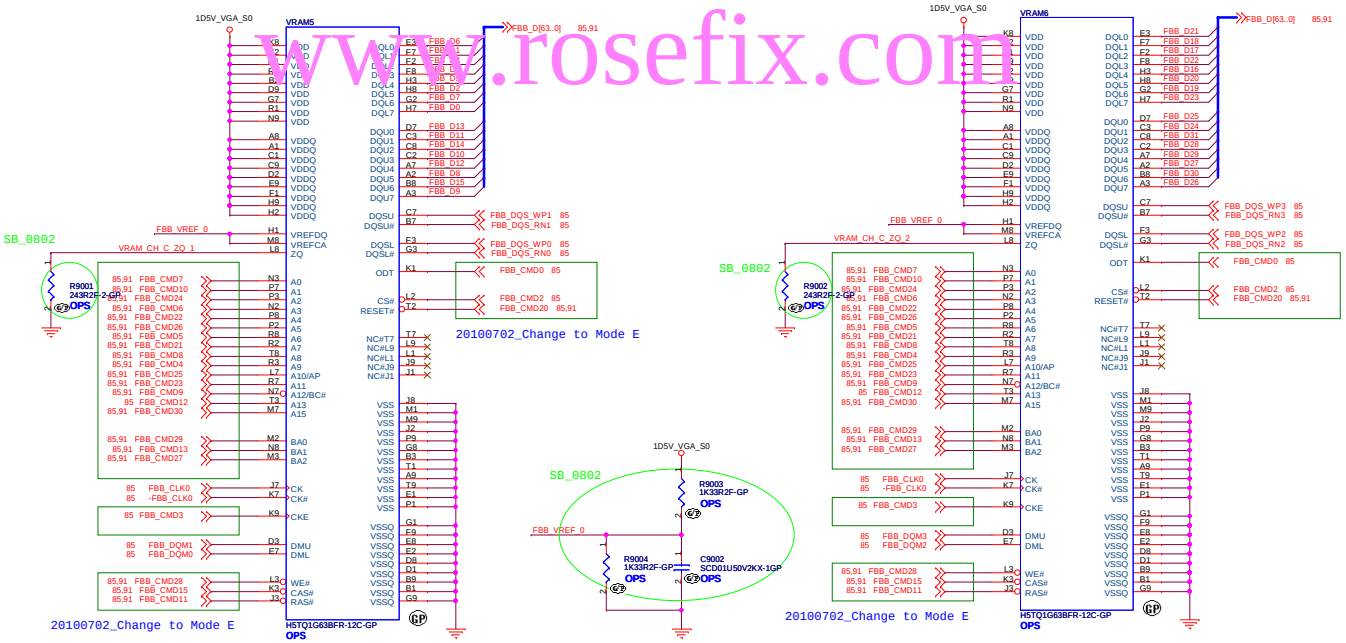
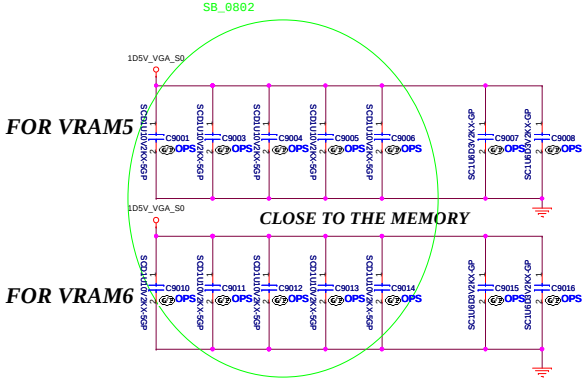
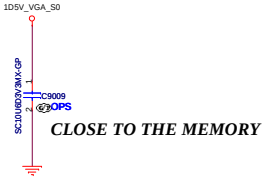




DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VIDEO FRAME BUFFER PORT C

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM CHANNEL-C***

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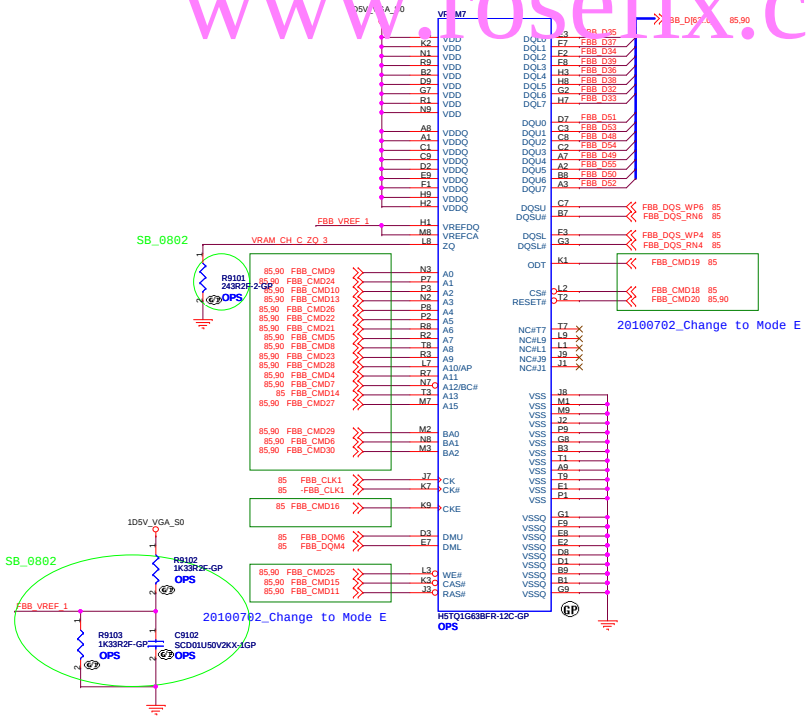

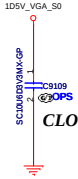

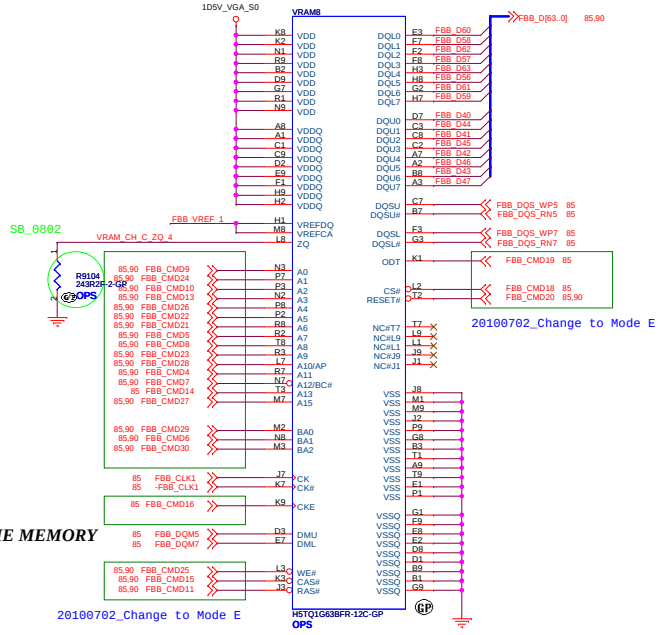

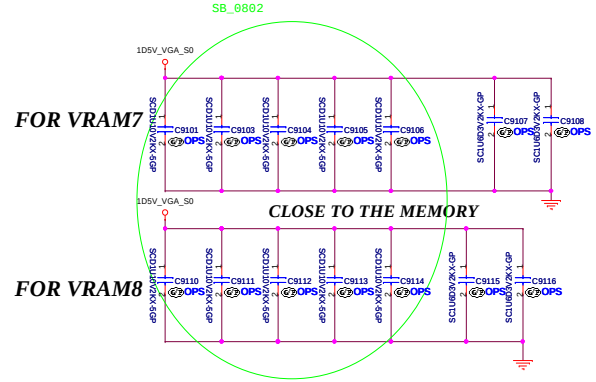

VIDEO FRAME BUFFER PORT C

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM CHANNEL-C***

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SSID = PWR.Plane.Regulator_GFX

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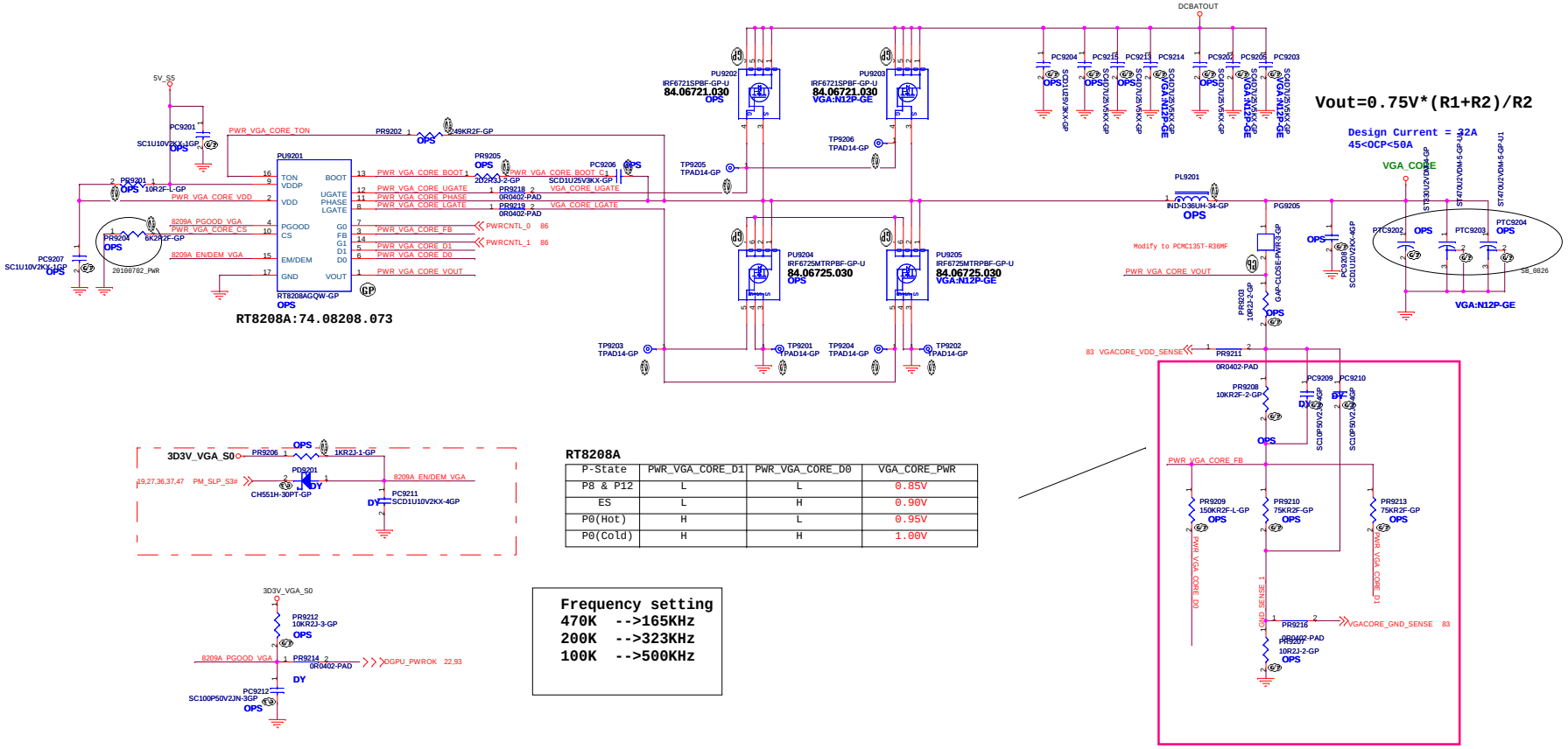

RT8208A			
P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 & P12	L	L	0.85V
ES	L	H	0.90V
P0(Hot)	H	L	0.95V
P0(Cold)	H	H	1.00V

Frequency setting
470K --->165KHz
200K --->323KHz
100K --->500KHz

JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC/DC_VGA CORE_RT8208A	
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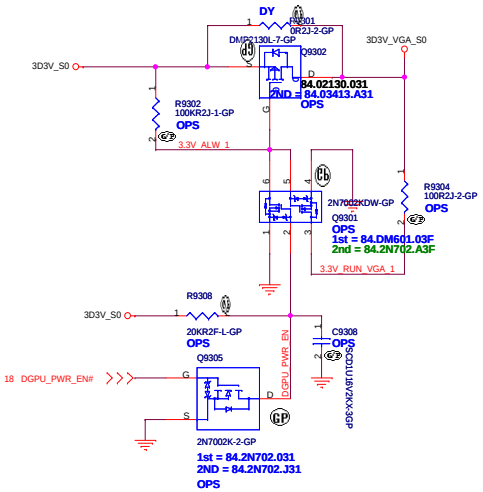
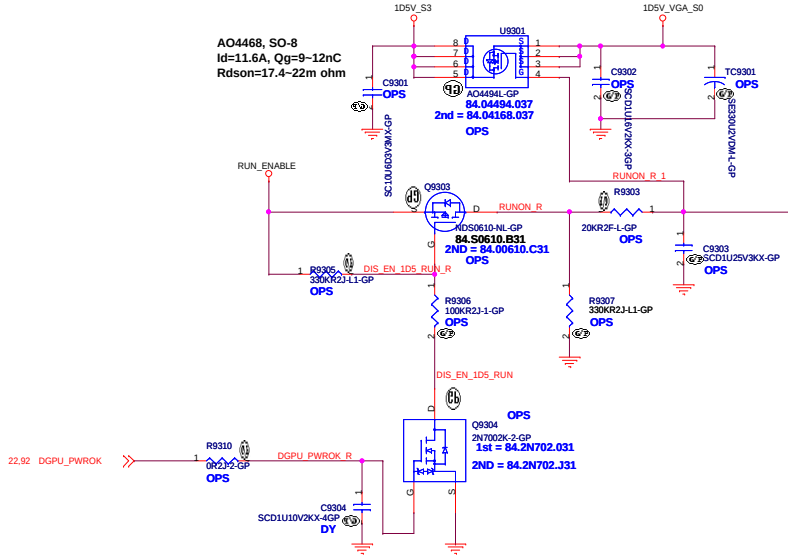
+3VS to 3.3V_DELAY Transfer

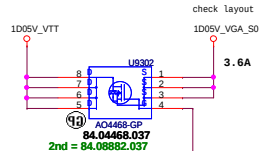


1D5V_VGA_S0

AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm

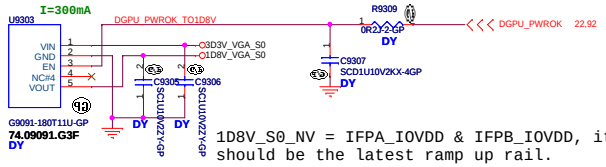


1.05V to 1.05V_VGA_S0 Transfer



20100707

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

JV10-CS

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Title: DISCRETE VGA POWER		
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Title: LVDS_Switch

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Title: *CRT_Switch*

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Title

TOUCH PANEL

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CPU Plate

H1 HOLE276R178-GP — ZZ.00PAD.N11
H2 HOLE276R178-GP — ZZ.00PAD.N11
H3 HOLE276R178-GP — ZZ.00PAD.N11

VGA Std-Off

H4 STF237R128H42-1-GP — 34.4GD01.001
H5 STF237R128H42-1-GP — 34.4GD01.001

Structure boss

H7 HOLE335R115-GP — ZZ.00PAD.D01
H9 HOLE335R115-GP — ZZ.00PAD.D01
H10 HOLE335R115-GP — ZZ.00PAD.D01
H11 HOLE335R115-GP — ZZ.00PAD.D01
H8 HOLE256R115-GP — ZZ.00PAD.D11
H12 HOLE256R115-GP — ZZ.00PAD.D11
H13 HOLE256R115-GP — ZZ.00PAD.D11
H15 HOLE256R115-GP — ZZ.00PAD.D11

Check test point

5,11,18,27,31,36,65,66,71,83 PLT_RST# — AFTP1
3D3V_S0 — AFTP7
3D3V_AUX_S5 — AFTP8
3D3V_S5 — AFTP9
5V_S5 — AFTP10
11,19,27 PM_PWRBTN# — AFTP11
5,11,22,36 H_CPUPWRGD — AFTP12
27,36 S5_ENABLE — AFTP13

Test Point放在Dimm Door打開可量測處

MiniPCI Std-Off

H14 STF256R89H178-GP — 34.4B417.001

1D05V_VTT

R9701 100R2J-2-GP DY — VTT_RUNPWR
Q9701 2N7002A-7-GP DY
16,31,33,40,42 PS_S3CNTRL — PS_S3CNTRL

1D8V_S0

R9702 100R2J-2-GP DY — 1D8V_RUNPWR
Q9702 2N7002A-7-GP DY
PS_S3CNTRL

1D5V_S0

R9703 100R2J-2-GP DY — 1D5V_RUNPWR
Q9703 2N7002A-7-GP DY
PS_S3CNTRL

3D3V_S0

R9704 100R2J-2-GP DY — 3D3V_RUNPWR
Q9704 2N7002A-7-GP DY
PS_S3CNTRL

5V_S0

R9705 100R2J-2-GP DY — 5V_RUNPWR
Q9705 2N7002A-7-GP DY
PS_S3CNTRL

AD+

EC9702 SCD1U25V2KX-GP
EC9703 SCD1U25V2KX-GP
EC9704 SCD1U25V2KX-GP DY

DCBATOUT

EC9705 SCD1U25V2KX-GP

VCC_CORE

R9706 100R2J-2-GP DY — CORE_RUNPWR
Q9706 2N7002A-7-GP DY
PS_S3CNTRL

VCC_GFXCORE

R9707 100R2J-2-GP DY — GFX_RUNPWR
Q9707 2N7002A-7-GP DY
PS_S3CNTRL

0D75V_S0

R9708 22R2J-2-GP DY — 0D75V_RUNPWR
Q9708 2N7002A-7-GP DY
PS_S3CNTRL

0D85V_S0

R9709 100R2J-2-GP DY — 1D05V_RUNPWR
Q9709 2N7002A-7-GP DY
PS_S3CNTRL

For Discharge

3D3V_S5
R9710 100KR2J-1-GP DY
Q9710 2N7002A-7-GP DY
PM_SLP_S4
16,31,33,40,42 PM_SLP_S4#

1D5V_S3
R9711 100R2J-2-GP DY — 3D3V_RUNPWR
Q9711 2N7002A-7-GP DY

<Variant Name>

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