JE40 HR
DIS/UMA/Muxless Schematics Document
Sandy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
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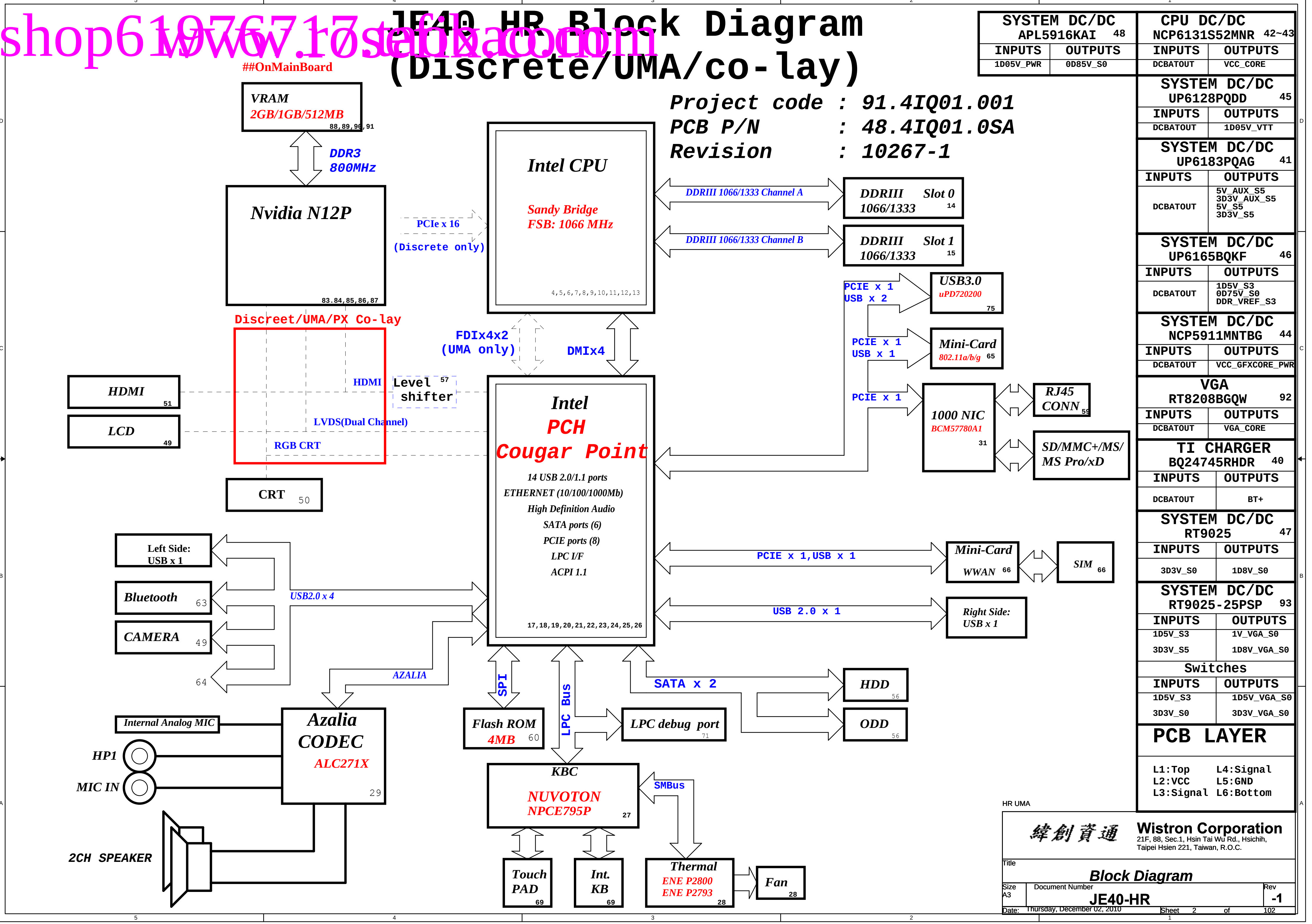

PCH Strapping

Name	Schematic Notes
SPKR	**Reboot option (if power up):** Connect to Vcc3_3 with 8.2-kΩ pull-up resistor. **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

SANDY

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DMI

19 DMI_TXN[3:0]
DMI_TXN0 B27
DMI_TXN1 B25
DMI_TXN2 A25
DMI_TXN3 B24
DMI_RX#0
DMI_RX#1
DMI_RX#2
DMI_RX#3

19 DMI_TXP[3:0]
DMI_TXP0 B28
DMI_TXP1 B26
DMI_TXP2 A24
DMI_TXP3 B23
DMI_RX0
DMI_RX1
DMI_RX2
DMI_RX3

19 DMI_RXN[3:0]
DMI_RXN0 G21
DMI_RXN1 E22
DMI_RXN2 F21
DMI_RXN3 D21
DMI_TX#0
DMI_TX#1
DMI_TX#2
DMI_TX#3

19 DMI_RXP[3:0]
DMI_RXP0 G22
DMI_RXP1 D22
DMI_RXP2 F20
DMI_RXP3 C21
DMI_TX0
DMI_TX1
DMI_TX2
DMI_TX3

Intel(R) FDI

19 FDI_TXN[7:0]
FDI_TXN0 A21
FDI_TXN1 H19
FDI_TXN2 E19
FDI_TXN3 F18
FDI_TXN4 B21
FDI_TXN5 C20
FDI_TXN6 D18
FDI_TXN7 E17
FDI0_TX#0
FDI0_TX#1
FDI0_TX#2
FDI0_TX#3
FDI1_TX#0
FDI1_TX#1
FDI1_TX#2
FDI1_TX#3

19 FDI_TXP[7:0]
FDI_TXP0 A22
FDI_TXP1 G19
FDI_TXP2 E20
FDI_TXP3 G18
FDI_TXP4 B20
FDI_TXP5 C19
FDI_TXP6 D19
FDI_TXP7 F17
FDI0_TX0
FDI0_TX1
FDI0_TX2
FDI0_TX3
FDI1_TX0
FDI1_TX1
FDI1_TX2
FDI1_TX3

19 FDI_FSYNC0 J18
19 FDI_FSYNC1 J17
FDI0_FSYNC
FDI1_FSYNC

19 FDI_INT H20
FDI_INT

19 FDI_LSYNC0 J19
19 FDI_LSYNC1 H17
FDI0_LSYNC
FDI1_LSYNC

eDP

1D05V_VTT
R402 1 24D9R2F-L-GP DP_COMP A18
R403 1 10KR2J-3-GP eDP_HPD A17
B16
EDP_COMPIO
EDP_ICOMPO
EDP_HPD

C15 EDP_AUX
D15 EDP_AUX#

C17 EDP_TX0
F16 EDP_TX1
C16 EDP_TX2
G15 EDP_TX3

C18 EDP_TX#0
E16 EDP_TX#1
D16 EDP_TX#2
F15 EDP_TX#3

JE40 delete eDP function

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

PCI EXPRESS* - GRAPHICS

1D05V_VTT
PEG_ICOMPI J22
PEG_ICOMPO J21
PEG_RCOMPO H22
PEG_IRCOMP_R
R401 1 24D9R2F-L-GP

PEG_RX#0 K33 PEG_RXN15
PEG_RX#1 M35 PEG_RXN14
PEG_RX#2 L34 PEG_RXN13
PEG_RX#3 J35 PEG_RXN12
PEG_RX#4 J32 PEG_RXN11
PEG_RX#5 H34 PEG_RXN10
PEG_RX#6 H31 PEG_RXN9
PEG_RX#7 G33 PEG_RXN8
PEG_RX#8 G30 PEG_RXN7
PEG_RX#9 F35 PEG_RXN6
PEG_RX#10 E34 PEG_RXN5
PEG_RX#11 E32 PEG_RXN4
PEG_RX#12 D33 PEG_RXN3
PEG_RX#13 D31 PEG_RXN2
PEG_RX#14 B33 PEG_RXN1
PEG_RX#15 C32 PEG_RXN0
PEG_RXN[0..15] 83

PEG_RX0 J33 PEG_RXP15
PEG_RX1 L35 PEG_RXP14
PEG_RX2 K34 PEG_RXP13
PEG_RX3 H35 PEG_RXP12
PEG_RX4 H32 PEG_RXP11
PEG_RX5 G34 PEG_RXP10
PEG_RX6 G31 PEG_RXP9
PEG_RX7 F33 PEG_RXP8
PEG_RX8 F30 PEG_RXP7
PEG_RX9 E35 PEG_RXP6
PEG_RX10 E33 PEG_RXP5
PEG_RX11 E32 PEG_RXP4
PEG_RX12 D34 PEG_RXP3
PEG_RX13 E31 PEG_RXP2
PEG_RX14 C33 PEG_RXP1
PEG_RX15 B32 PEG_RXP0
PEG_RXP[0..15] 83

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

PEG_TX#0 M29 PEG_C_TXN15 C401 DIS_PX_Muxless Do Not Stuff PEG_TXN15
PEG_TX#1 M32 PEG_C_TXN14 C402 DIS_PX_Muxless Do Not Stuff PEG_TXN14
PEG_TX#2 M31 PEG_C_TXN13 C403 DIS_PX_Muxless Do Not Stuff PEG_TXN13
PEG_TX#3 L32 PEG_C_TXN12 C404 DIS_PX_Muxless Do Not Stuff PEG_TXN12
PEG_TX#4 L29 PEG_C_TXN11 C405 DIS_PX_Muxless Do Not Stuff PEG_TXN11
PEG_TX#5 K31 PEG_C_TXN10 C406 DIS_PX_Muxless Do Not Stuff PEG_TXN10
PEG_TX#6 K28 PEG_C_TXN9 C407 DIS_PX_Muxless Do Not Stuff PEG_TXN9
PEG_TX#7 J30 PEG_C_TXN8 C408 DIS_PX_Muxless Do Not Stuff PEG_TXN8
PEG_TX#8 J28 PEG_C_TXN7 C409 DIS_PX_Muxless Do Not Stuff PEG_TXN7
PEG_TX#9 H29 PEG_C_TXN6 C410 DIS_PX_Muxless Do Not Stuff PEG_TXN6
PEG_TX#10 G27 PEG_C_TXN5 C411 DIS_PX_Muxless Do Not Stuff PEG_TXN5
PEG_TX#11 E29 PEG_C_TXN4 C412 DIS_PX_Muxless Do Not Stuff PEG_TXN4
PEG_TX#12 F27 PEG_C_TXN3 C413 DIS_PX_Muxless Do Not Stuff PEG_TXN3
PEG_TX#13 D28 PEG_C_TXN2 C414 DIS_PX_Muxless Do Not Stuff PEG_TXN2
PEG_TX#14 F26 PEG_C_TXN1 C415 DIS_PX_Muxless Do Not Stuff PEG_TXN1
PEG_TX#15 E25 PEG_C_TXN0 C416 DIS_PX_Muxless Do Not Stuff PEG_TXN0
PEG_TXN[0..15] 83

PEG_TX0 M28 PEG_C_TXP15 C417 DIS_PX_Muxless Do Not Stuff PEG_TXP15
PEG_TX1 M33 PEG_C_TXP14 C418 DIS_PX_Muxless Do Not Stuff PEG_TXP14
PEG_TX2 M30 PEG_C_TXP13 C419 DIS_PX_Muxless Do Not Stuff PEG_TXP13
PEG_TX3 L31 PEG_C_TXP12 C420 DIS_PX_Muxless Do Not Stuff PEG_TXP12
PEG_TX4 L28 PEG_C_TXP11 C421 DIS_PX_Muxless Do Not Stuff PEG_TXP11
PEG_TX5 K30 PEG_C_TXP10 C422 DIS_PX_Muxless Do Not Stuff PEG_TXP10
PEG_TX6 K27 PEG_C_TXP9 C423 DIS_PX_Muxless Do Not Stuff PEG_TXP9
PEG_TX7 J29 PEG_C_TXP8 C424 DIS_PX_Muxless Do Not Stuff PEG_TXP8
PEG_TX8 J27 PEG_C_TXP7 C425 DIS_PX_Muxless Do Not Stuff PEG_TXP7
PEG_TX9 H28 PEG_C_TXP6 C426 DIS_PX_Muxless Do Not Stuff PEG_TXP6
PEG_TX10 G28 PEG_C_TXP5 C427 DIS_PX_Muxless Do Not Stuff PEG_TXP5
PEG_TX11 E28 PEG_C_TXP4 C428 DIS_PX_Muxless Do Not Stuff PEG_TXP4
PEG_TX12 F28 PEG_C_TXP3 C429 DIS_PX_Muxless Do Not Stuff PEG_TXP3
PEG_TX13 D27 PEG_C_TXP2 C430 DIS_PX_Muxless Do Not Stuff PEG_TXP2
PEG_TX14 F26 PEG_C_TXP1 C431 DIS_PX_Muxless Do Not Stuff PEG_TXP1
PEG_TX15 D25 PEG_C_TXP0 C432 DIS_PX_Muxless Do Not Stuff PEG_TXP0
PEG_TXP[0..15] 83

GP

Stuff to disable internal graphics function for power saving.

FDI_LSYNC0
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC1
FDI_INT

R404 Do Not Stuff DIS
RN401 Do Not Stuff DIS

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Title: CPU (PCIE/DMI/FDI)

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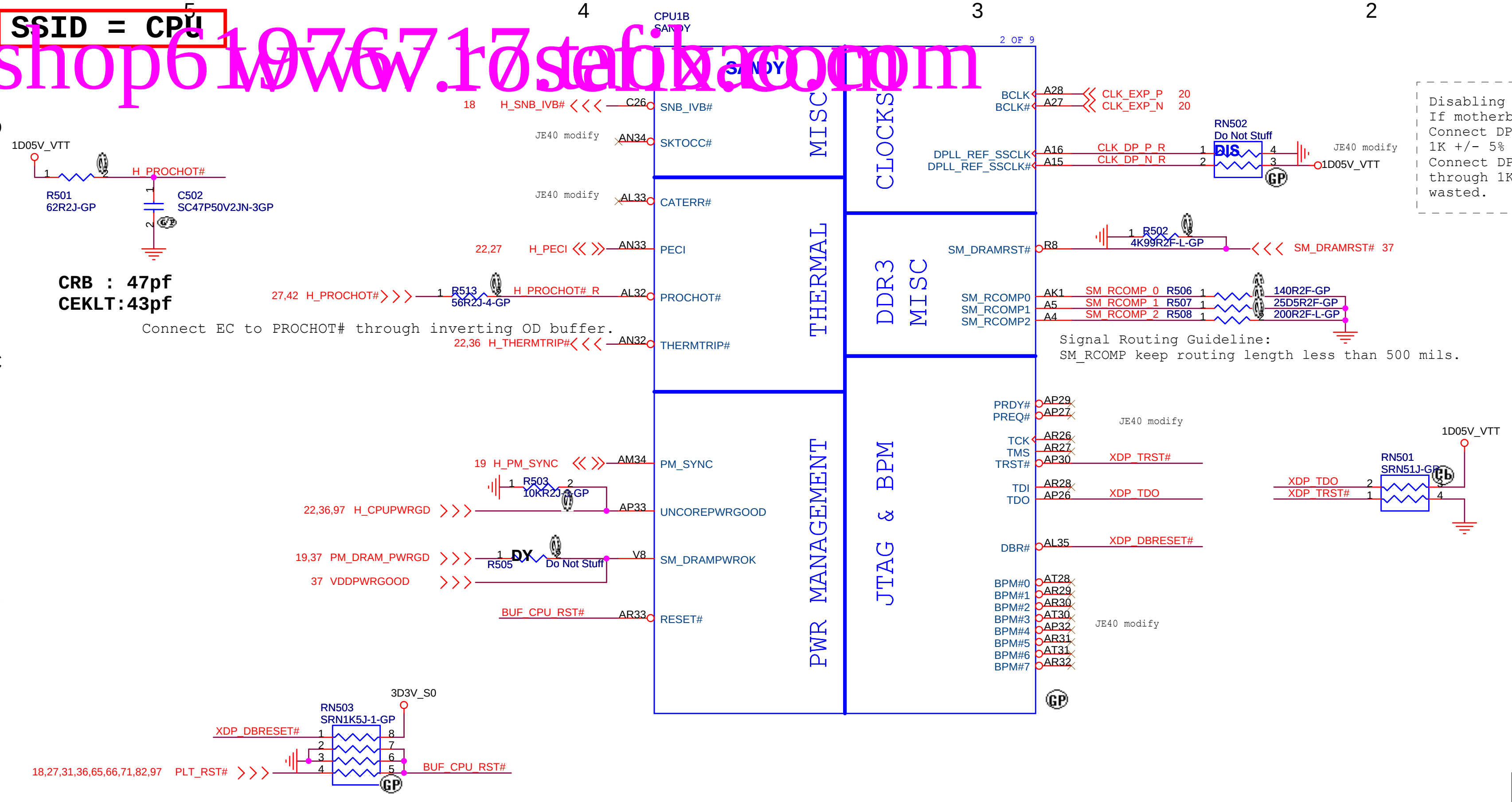
SSID = CPU


CPU1B
SANDY
2 OF 9
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
SNB_IVB#
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
BCLK
BCLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#0
BPM#1
BPM#2
BPM#3
BPM#4
BPM#5
BPM#6
BPM#7
18 H_SNB_IVB#
JE40 modify
1D05V_VTT
H_PROCHOT#
R501
62R2J-GP
C502
SC47P50V2JN-3GP
22,27 H_PECI
27,42 H_PROCHOT#
R513
56R2J-4-GP
H_PROCHOT#_R
22,36 H_THERMTRIP#
19 H_PM_SYNC
R503
10KR2J-3-GP
22,36,97 H_CPUPWRGD
19,37 PM_DRAM_PWRGD
R505
DX
Do Not Stuff
37 VDDPWRGOOD
BUF_CPU_RST#
CLK_EXP_P 20
CLK_EXP_N 20
RN502
Do Not Stuff
DIS
CLK_DP_P_R
CLK_DP_N_R
R502
4K99R2F-L-GP
SM_DRAMRST# 37
SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
R506
R507
R508
140R2F-GP
25D5R2F-GP
200R2F-L-GP
XDP_TRST#
XDP_TDO
XDP_DBRESET#
RN501
SRN51J-GP
3D3V_S0
RN503
SRN1K5J-1-GP
18,27,31,36,65,66,71,82,97 PLT_RST#

CRB : 47pf
CEKLT:43pf

Connect EC to PROCHOT# through inverting OD buffer.

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

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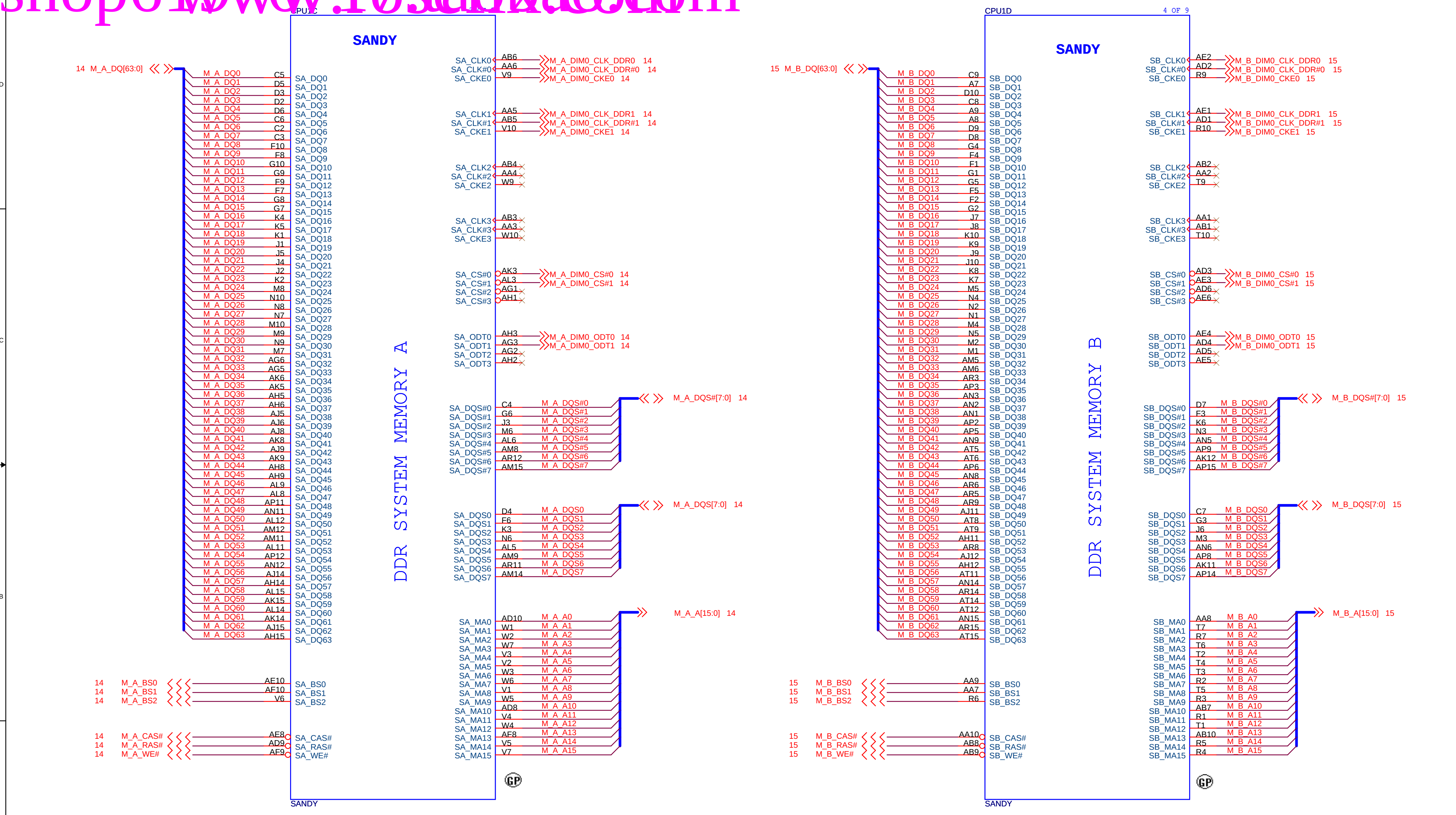

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Title: **CPU (DDR)**

Size: A3 | Document Number: **JE40-HR** | Rev: -1

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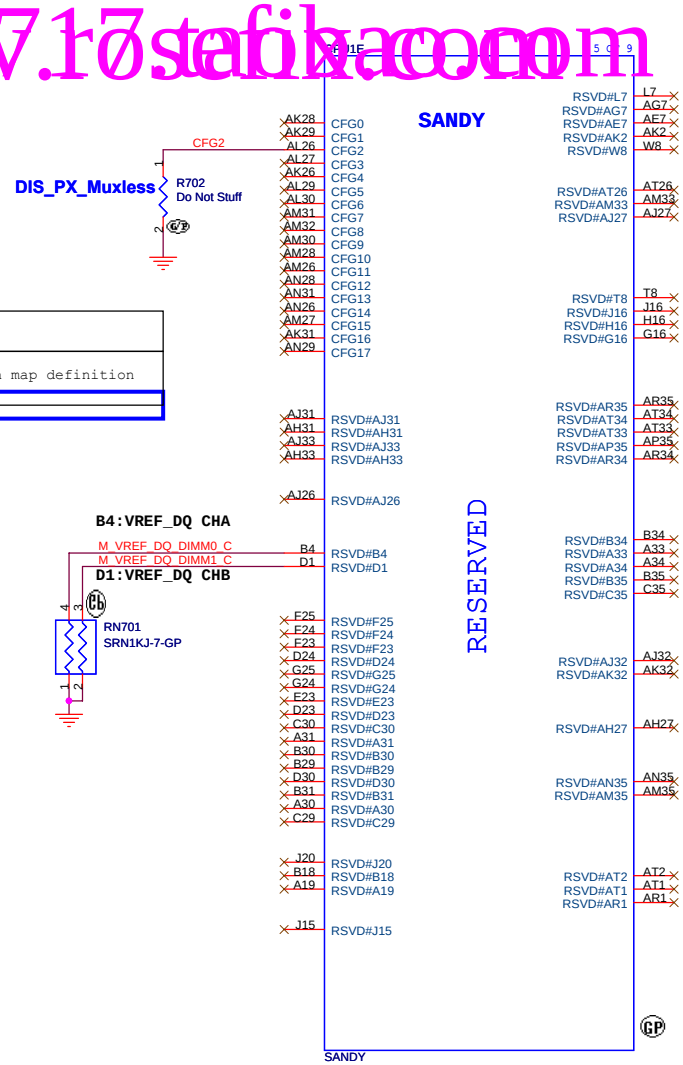
SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

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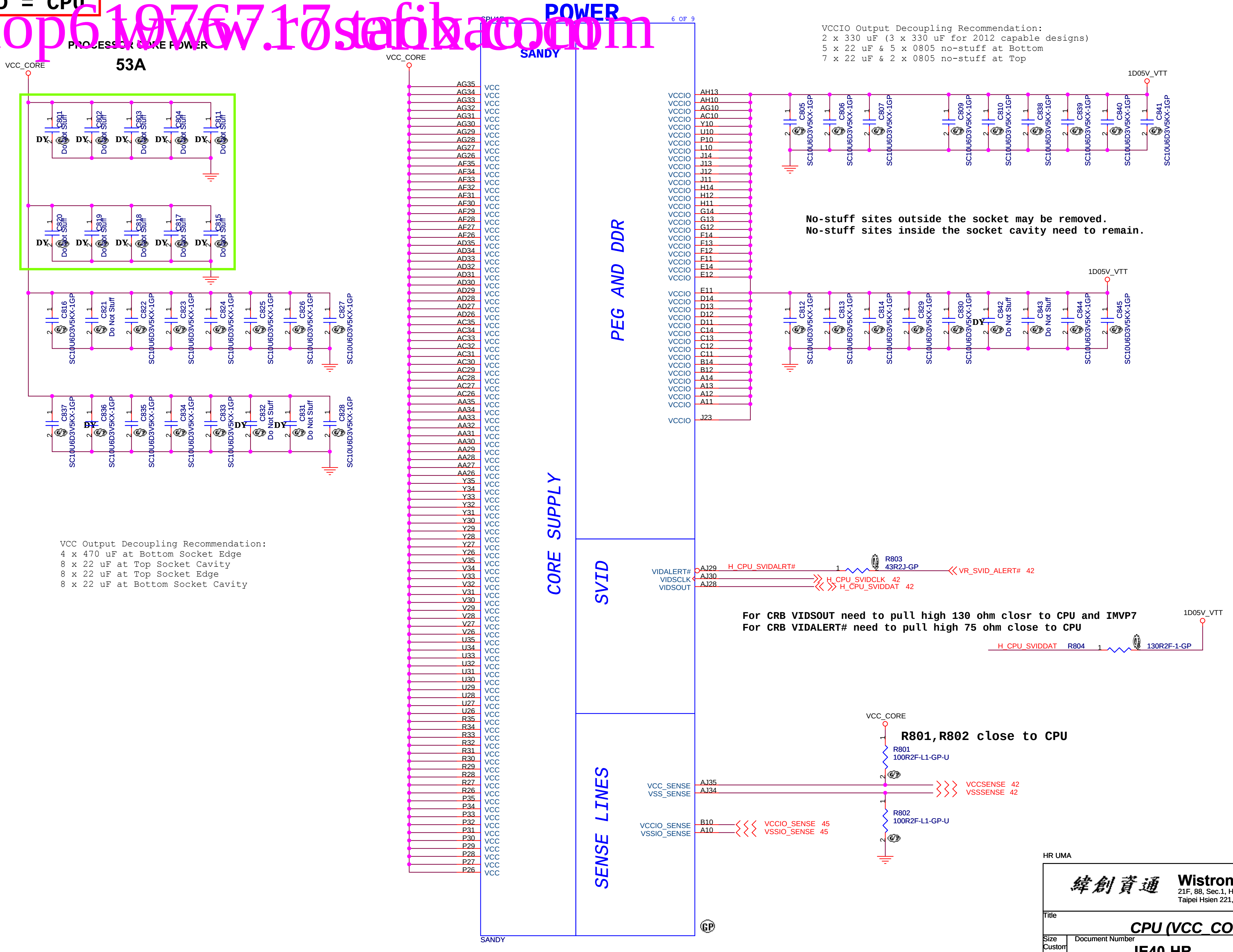
SSID = CPU

POWER



VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

R801,R802 close to CPU

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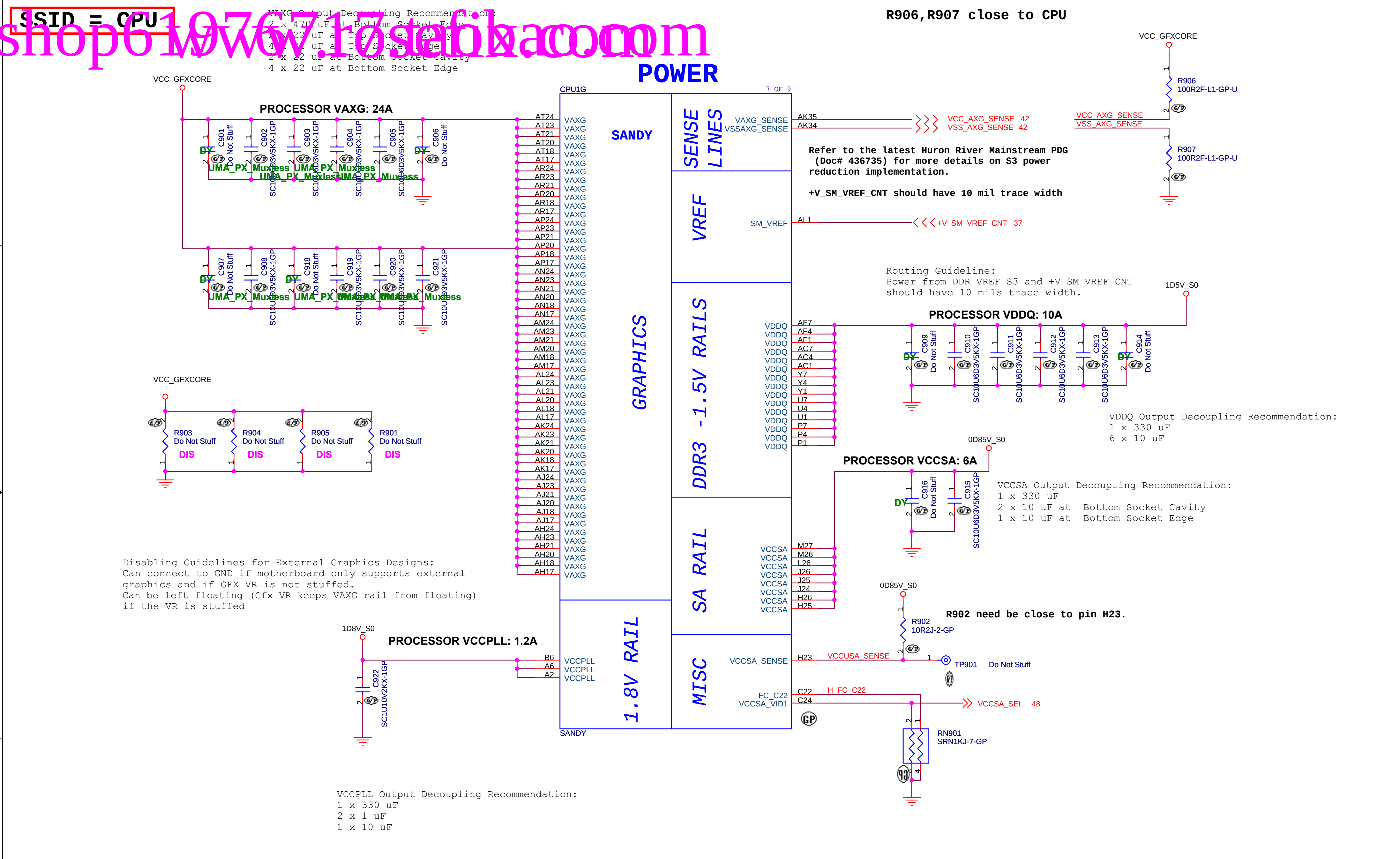

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Title: **CPU (VCC_GFXCORE)**

Size	Document Number	Rev
A3	JE40-HR	-1

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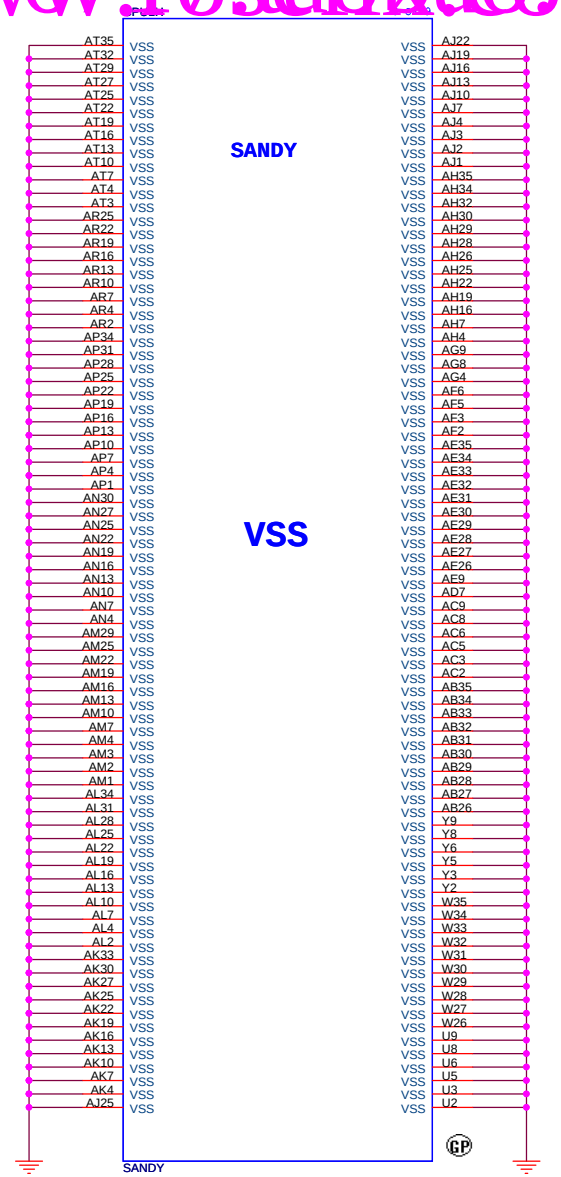
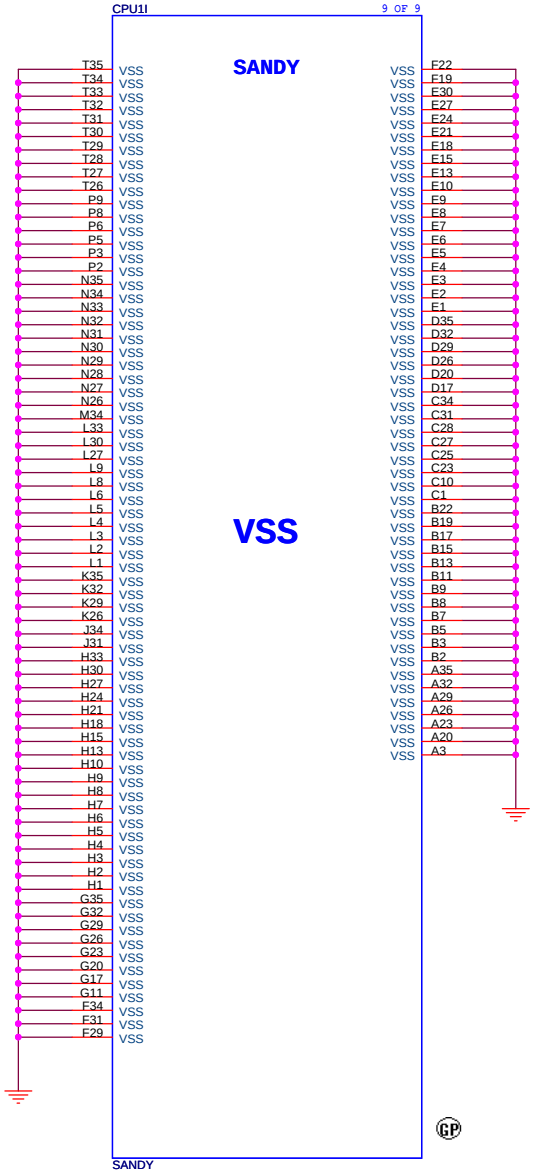
SSID = CPU





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Title: CPU (VSS)		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 10 of 102	

JE40 delete XDP function

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: XDP

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 11 of 102

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HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 12 of 102

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HR UMA

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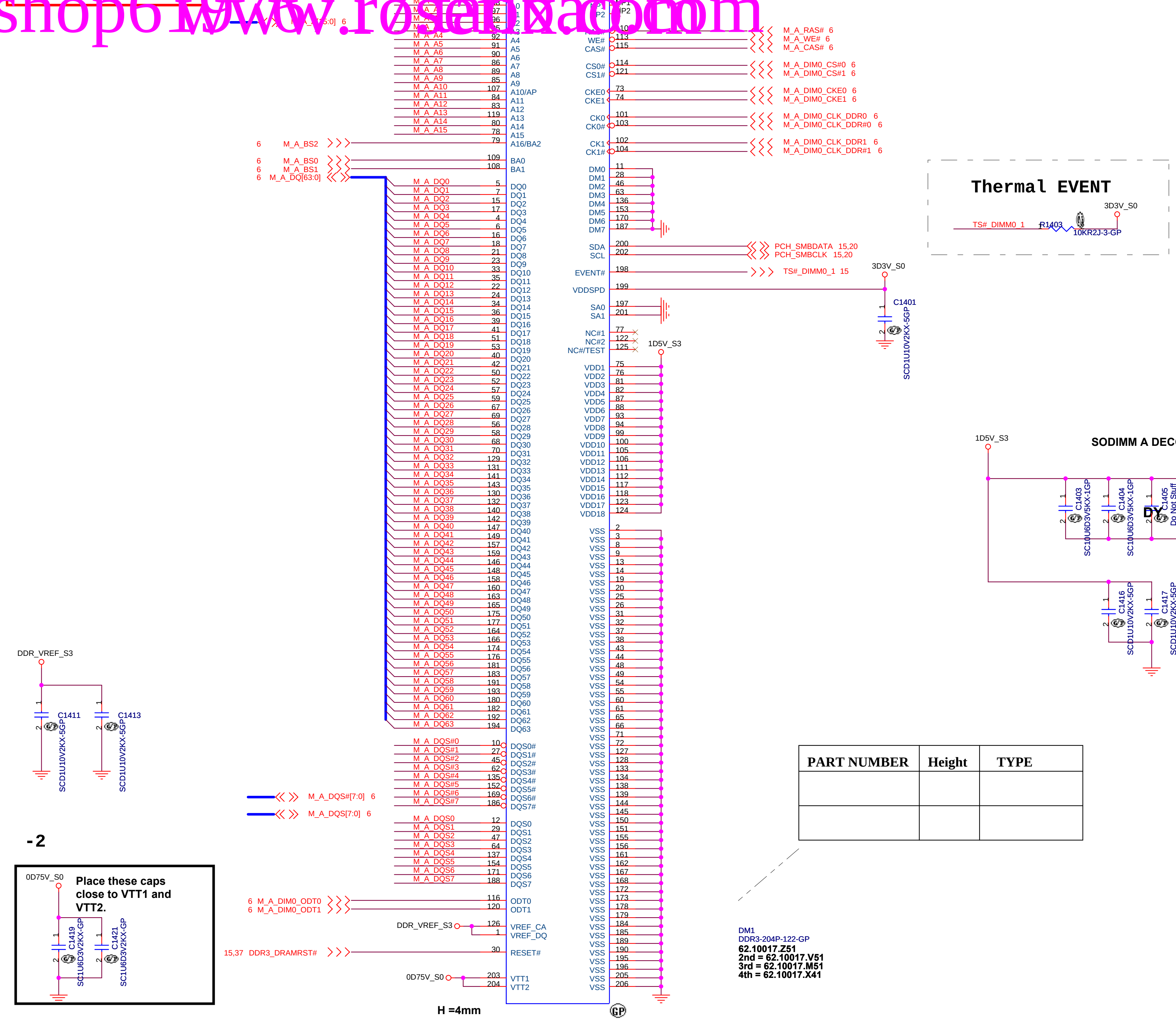
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 13 of 102

SSID = MEMORY


M_A_A[15:0]
M_A_BS2
M_A_BS0
M_A_BS1
M_A_DQ[63:0]
A16/BA2
BA0
BA1
M_A_RAS# 6
M_A_WE# 6
M_A_CAS# 6
M_A_DIM0_CS#0 6
M_A_DIM0_CS#1 6
M_A_DIM0_CKE0 6
M_A_DIM0_CKE1 6
M_A_DIM0_CLK_DDR0 6
M_A_DIM0_CLK_DDR#0 6
M_A_DIM0_CLK_DDR1 6
M_A_DIM0_CLK_DDR#1 6
PCH_SMBDATA 15,20
PCH_SMBCLK 15,20
TS#_DIMM0_1 15
EVENT#
VDDSPD
SA0
SA1
NC#1
NC#2
NC#/TEST
3D3V_S0
1D5V_S3
C1401
SCD1U10V2KX-5GP
Thermal EVENT
TS#_DIMM0_1
R1403
10KR2J-3-GP
SODIMM A DECOUPLING
Layout Note:
Place these Caps near SO-DIMMA.
C1403
C1404
C1405
C1406
C1407
C1408
C1409
C1410
C1416
C1417
DY
Do Not Stuff
3G_RF
DDR_VREF_S3
C1411
C1413
SCD1U10V2KX-5GP
M_A_DQS#[7:0] 6
M_A_DQS[7:0] 6
0D75V_S0
Place these caps close to VTT1 and VTT2.
C1419
C1421
SC1U6D3V2KX-GP
M_A_DIM0_ODT0
M_A_DIM0_ODT1
ODT0
ODT1
VREF_CA
VREF_DQ
15,37 DDR3_DRAMRST#
RESET#
VTT1
VTT2
H =4mm
DM1
DDR3-204P-122-GP
62.10017.Z51
2nd = 62.10017.V51
3rd = 62.10017.M51
4th = 62.10017.X41

-2

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

PART NUMBER	Height	TYPE

HR UMA

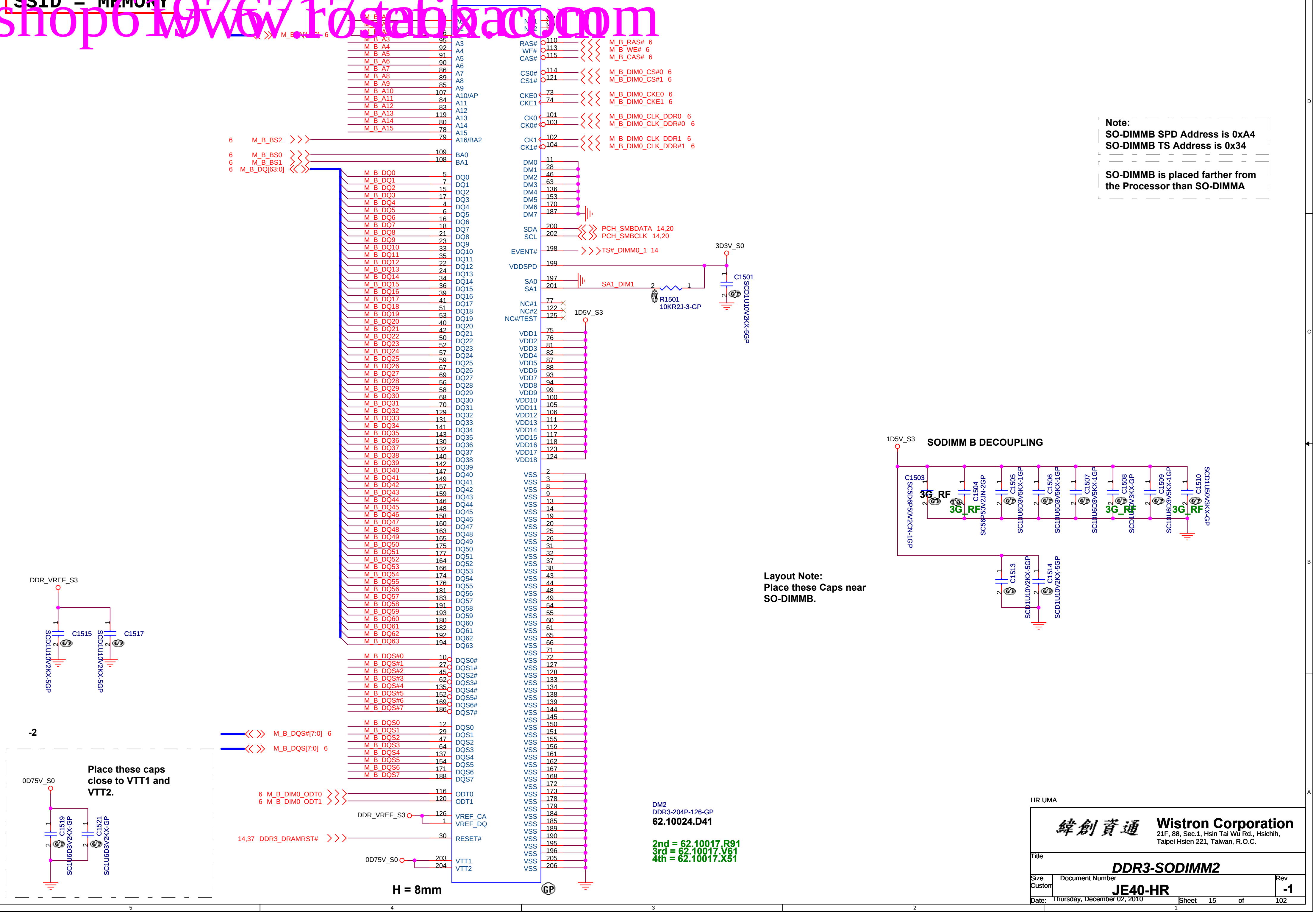
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 14 of 102

SSID = MEMORY



M_B_A[15:0] 6
M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14 M_B_A15
A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2
6 M_B_BS2
6 M_B_BS0
6 M_B_BS1
6 M_B_DQ[63:0]
BA0 BA1
M_B_DQ0 … M_B_DQ63
DQ0 … DQ63
M_B_DQS#0 … M_B_DQS#7
DQS0# … DQS7#
M_B_DQS0 … M_B_DQS7
DQS0 … DQS7
M_B_DQS#[7:0] 6
M_B_DQS[7:0] 6
6 M_B_DIM0_ODT0
6 M_B_DIM0_ODT1
ODT0 ODT1
DDR_VREF_S3
VREF_CA VREF_DQ
14,37 DDR3_DRAMRST#
RESET#
0D75V_S0
VTT1 VTT2
H = 8mm
RAS# WE# CAS#
M_B_RAS# 6
M_B_WE# 6
M_B_CAS# 6
CS0# CS1#
M_B_DIM0_CS#0 6
M_B_DIM0_CS#1 6
CKE0 CKE1
M_B_DIM0_CKE0 6
M_B_DIM0_CKE1 6
CK0 CK0#
M_B_DIM0_CLK_DDR0 6
M_B_DIM0_CLK_DDR#0 6
CK1 CK1#
M_B_DIM0_CLK_DDR1 6
M_B_DIM0_CLK_DDR#1 6
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
SDA SCL
PCH_SMBDATA 14,20
PCH_SMBCLK 14,20
EVENT#
TS#_DIMM0_1 14
VDDSPD
3D3V_S0
SA0 SA1
SA1_DIM1
R1501
10KR2J-3-GP
C1501
SCD1U10V2KX-5GP
NC#1 NC#2 NC#/TEST
1D5V_S3
VDD1 … VDD18
VSS
DM2
DDR3-204P-126-GP
62.10024.D41
2nd = 62.10017.R91
3rd = 62.10017.V61
4th = 62.10017.X51
DDR_VREF_S3
C1515 SCD1U10V2KX-5GP
C1517 SCD1U10V2KX-5GP
-2
0D75V_S0
C1519 SC1U6D3V2KX-GP
C1521 SC1U6D3V2KX-GP
Place these caps close to VTT1 and VTT2.
1D5V_S3
SODIMM B DECOUPLING
C1503 SC5D6P50V2CN-1GP
3G_RF
C1504 SC56P50V2JN-2GP
C1505 SC10U6D3V5KX-1GP
C1506 SC10U6D3V5KX-1GP
C1507 SC10U6D3V5KX-1GP
C1508 SCD1U50V3KX-GP
C1509 SC10U6D3V5KX-1GP
C1510 SCD1U50V3KX-GP
C1513 SCD1U10V2KX-5GP
C1514 SCD1U10V2KX-5GP

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

Layout Note:
Place these Caps near SO-DIMMB.

HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR3-SODIMM2	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 15 of 102	

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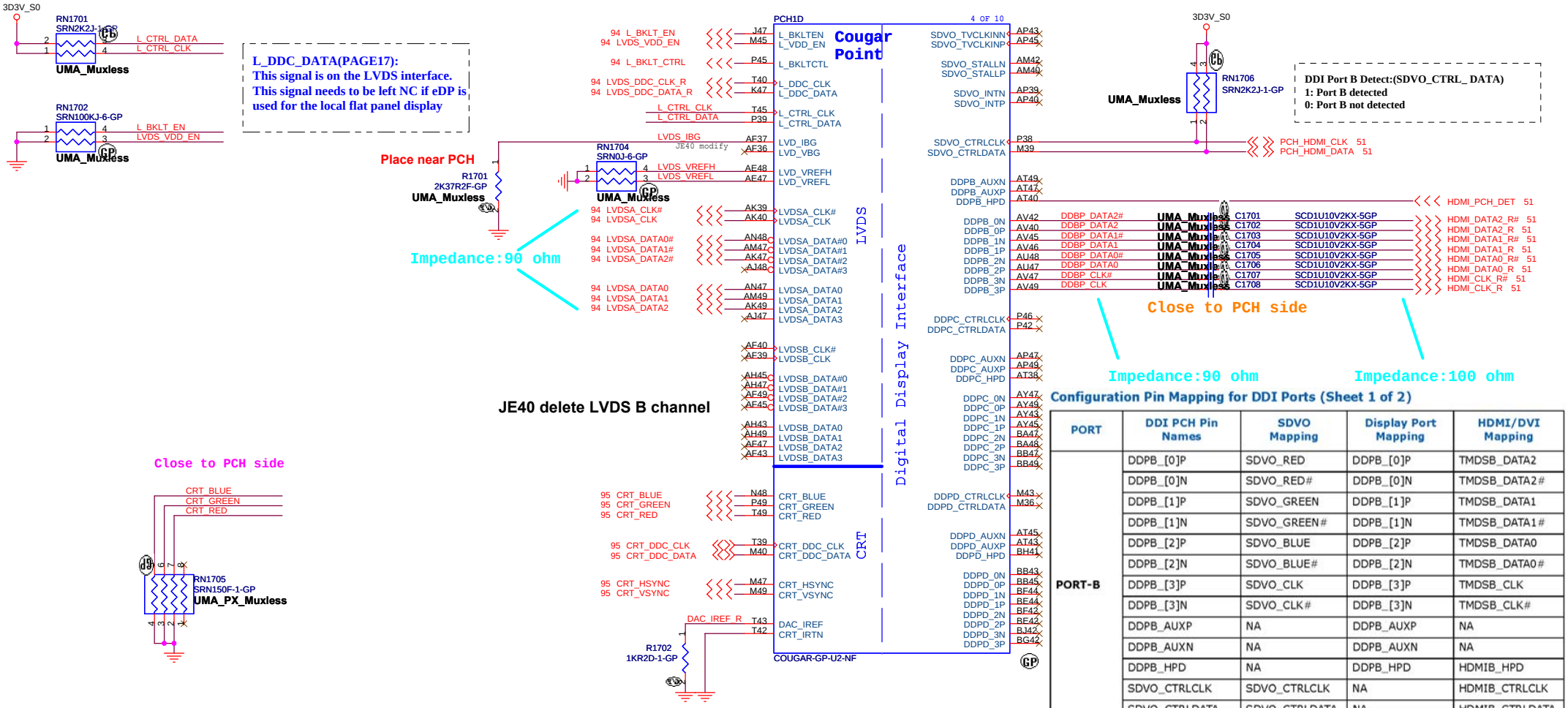
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 16 of 102



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 17 of 102

SSCD = PCH

RN1801
SRN8K2J-2-GP-U

INT_PIRQH# 1
INT_PIRQB# 2
INT_PIRQF# 3
INT_PIRQA# 4
5

10 3D3V_S0
9 INT_PIRQD#
8 INT_PIRQE#
7 INT_PIRQC#
6 USB30_SMI#

3D3V_S0

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

check R1808 R1809 阻值

CRB : 2.2K
CEKLT: 1K

1D8V_S0
R1808 2K2R2J-2-GP
NV_CLE 1
R1809 1KR2J-1-GP
H_SNB_IVB# 5

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

RN1803
SRN10KJ-5-GP

DGPU_HOLD_RST# 2
DGPU_PWR_EN# 1
4

USB Ext. port 1 (HS)
External debug port use on Huron river platform

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

PCH1E 5 OF 10

Cougar Point

RSVD
NVRAM
PCI
USB

COUGAR-GP-U2-NF

SB add USB port 5

JE40 co-lay USB2.0

JE40 modify 07/16

Do Not Stuff TP1806 — 83 DGPU_HOLD_RST# — DGPU_SELECT#
93 DGPU_PWR_EN#
Do Not Stuff TP1804 — DGPU_PWM_SELECT#

R1813 Do Not Stuff
56 SATA_ODD_DA#
82 USB30_SMI#

5,27,31,36,65,66,71,82,97 PLT_RST#

71 CLK_PCI_LPC
20 CLK_PCI_FB
27 CLK_PCI_KBC
R1804 22R2J-2-GP CLK_PCI_LPC_R
R1805 22R2J-2-GP CLK_PCI_FB_R
R1806 22R2J-2-GP CLK_PCI_KBC_R

EC1803 DY Do Not Stuff
EC1802 DY Do Not Stuff
EC1801 DY Do Not Stuff

KBC CLK EMI

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

USB_RBIAS
R1811 22D6R2F-L1-GP

3D3V_S5
R1820 10KR2J-3-GP

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

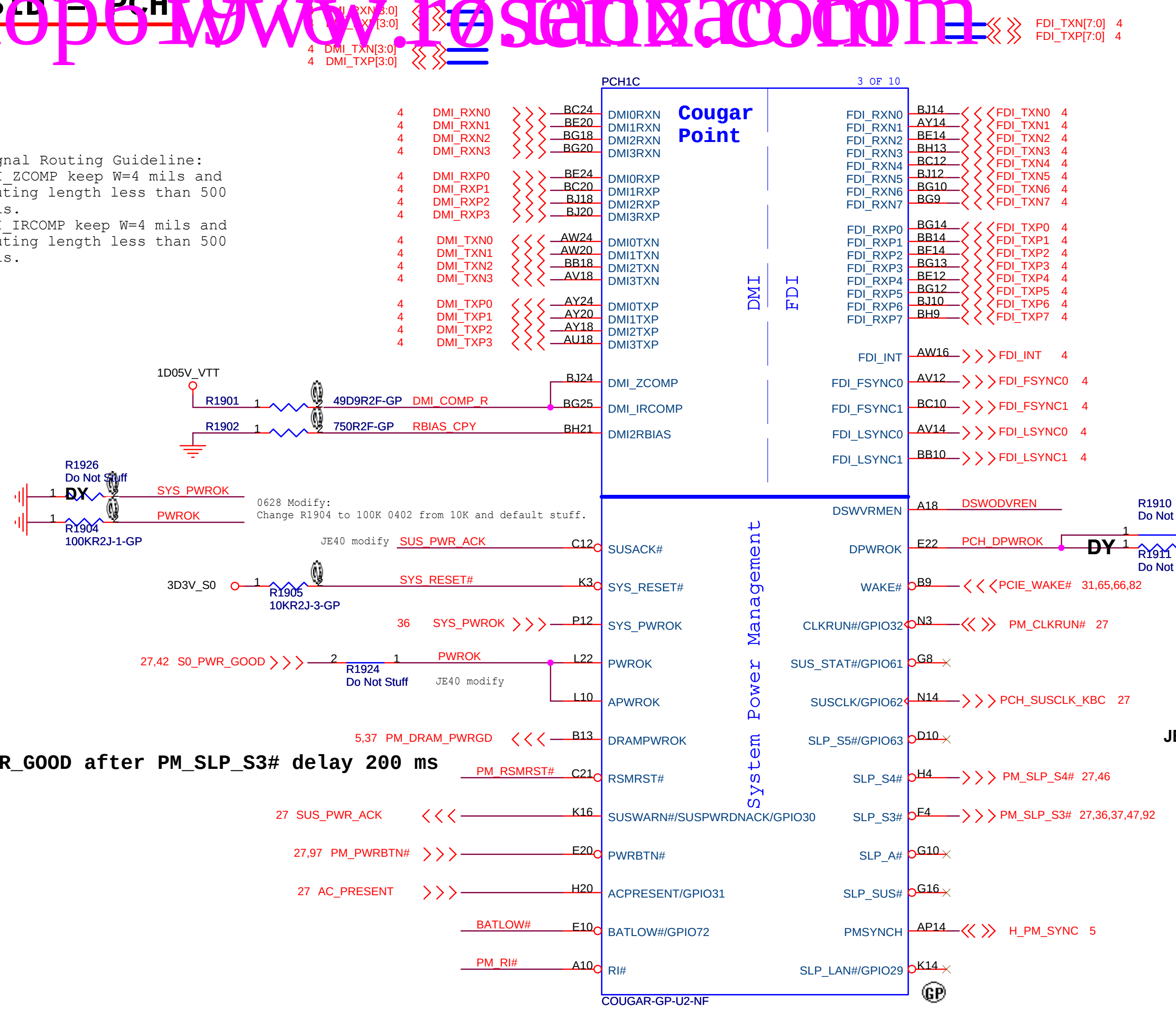
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 18 of 102

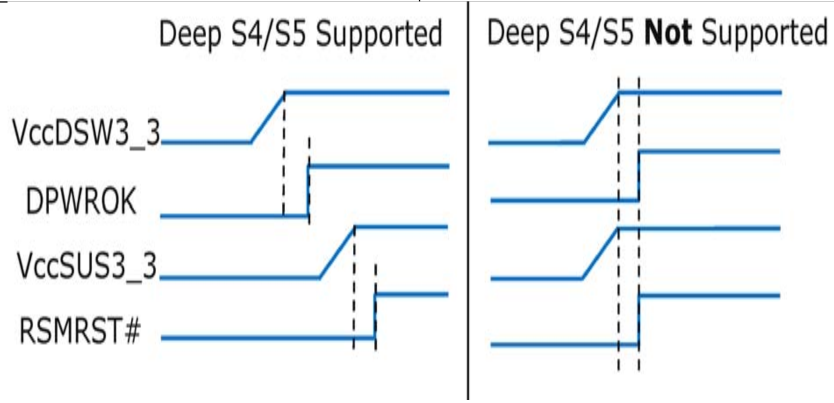
SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



PCH1C
3 OF 10
Cougar Point
DMI
FDI
System Power Management
DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3
DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3
DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3
DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3
DMI_ZCOMP
DMI_IRCOMP
DMI2RBIAS
FDI_RXN0 FDI_RXN1 FDI_RXN2 FDI_RXN3 FDI_RXN4 FDI_RXN5 FDI_RXN6 FDI_RXN7
FDI_RXP0 FDI_RXP1 FDI_RXP2 FDI_RXP3 FDI_RXP4 FDI_RXP5 FDI_RXP6 FDI_RXP7
FDI_TXN[7:0] 4
FDI_TXP[7:0] 4
DMI_TXN[3:0]
DMI_TXP[3:0]
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1
1D05V_VTT
R1901 49D9R2F-GP DMI_COMP_R
R1902 750R2F-GP RBIAS_CPY
R1926 Do Not Stuff
DY
SYS_PWROK
PWROK
R1904 100KR2J-1-GP
0628 Modify:
Change R1904 to 100K 0402 from 10K and default stuff.
JE40 modify SUS_PWR_ACK
3D3V_S0
R1905 10KR2J-3-GP
SYS_RESET#
36 SYS_PWROK
27,42 S0_PWR_GOOD
R1924 Do Not Stuff
JE40 modify
5,37 PM_DRAM_PWRGD
PM_RSMRST#
27 SUS_PWR_ACK
27,97 PM_PWRBTN#
27 AC_PRESENT
BATLOW#
PM_RI#
SUSACK#
SYS_RESET#
SYS_PWROK
PWROK
APWROK
DRAMPWROK
RSMRST#
SUSWARN#/SUSPWRDNACK/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
RI#
DSWVRMEN
DPWROK
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#/GPIO29
DSWODVREN
PCH_DPWROK
R1910 Do Not Stuff
R1911 Do Not Stuff
PM_RSMRST#
RTC_AUX_S5
PCIE_WAKE# 31,65,66,82
PM_CLKRUN# 27
PCH_SUSCLK_KBC 27
PM_SLP_S4# 27,46
PM_SLP_S3# 27,36,37,47,92
H_PM_SYNC 5
COUGAR-GP-U2-NF

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

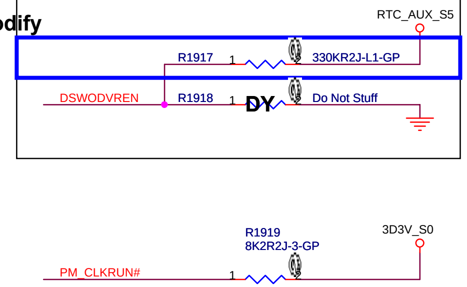


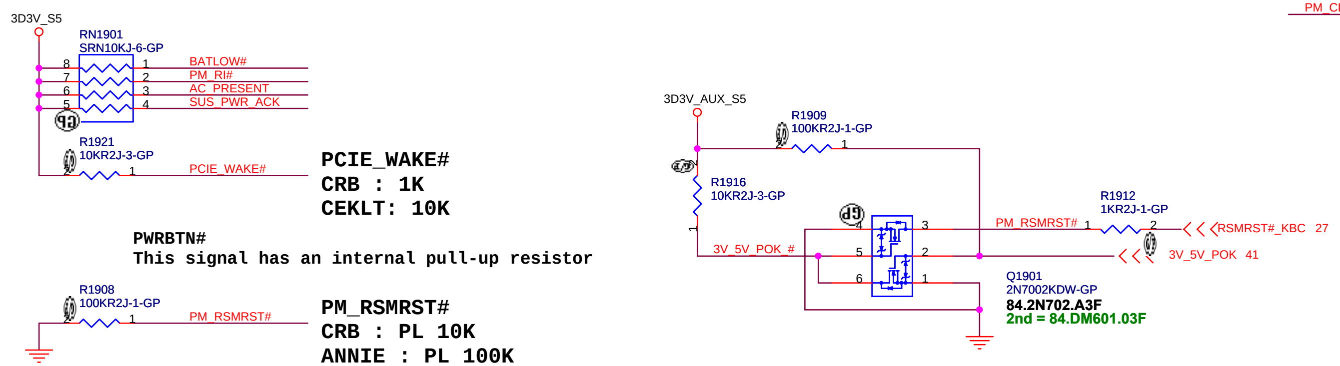
For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

JE40 modify 07/16

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SB modify





3D3V_S5
RN1901 SRN10KJ-6-GP
BATLOW#
PM_RI#
AC_PRESENT
SUS_PWR_ACK
R1921 10KR2J-3-GP
PCIE_WAKE#
R1908 100KR2J-1-GP
PM_RSMRST#
3D3V_AUX_S5
R1909 100KR2J-1-GP
R1916 10KR2J-3-GP
3V_5V_POK_#
R1912 1KR2J-1-GP
RSMRST#_KBC 27
3V_5V_POK 41
Q1901 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K

HR UMA

SSID = PCH

PCH1B

Cougar Point

W-WAN
WLAN
Card Reader
LAN
USB3.0
Intel GBE LAN
Dock
NEW CARD

PCI-E*

SMBUS

Controller Link

2 OF 10

JE40 delete New Card function

JE40 delete XDP function

CRB : 1K
CEKLT: 10K

For DIS_PX mode or MXM mode.

JE40 modify

CLOCKS

FLEX CLOCKS

WWAN CLK
WLAN CLK
LAN CLK
USB3.0 CLK

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

R2008 and C2008 CO-LAY

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0

need very close to PCH

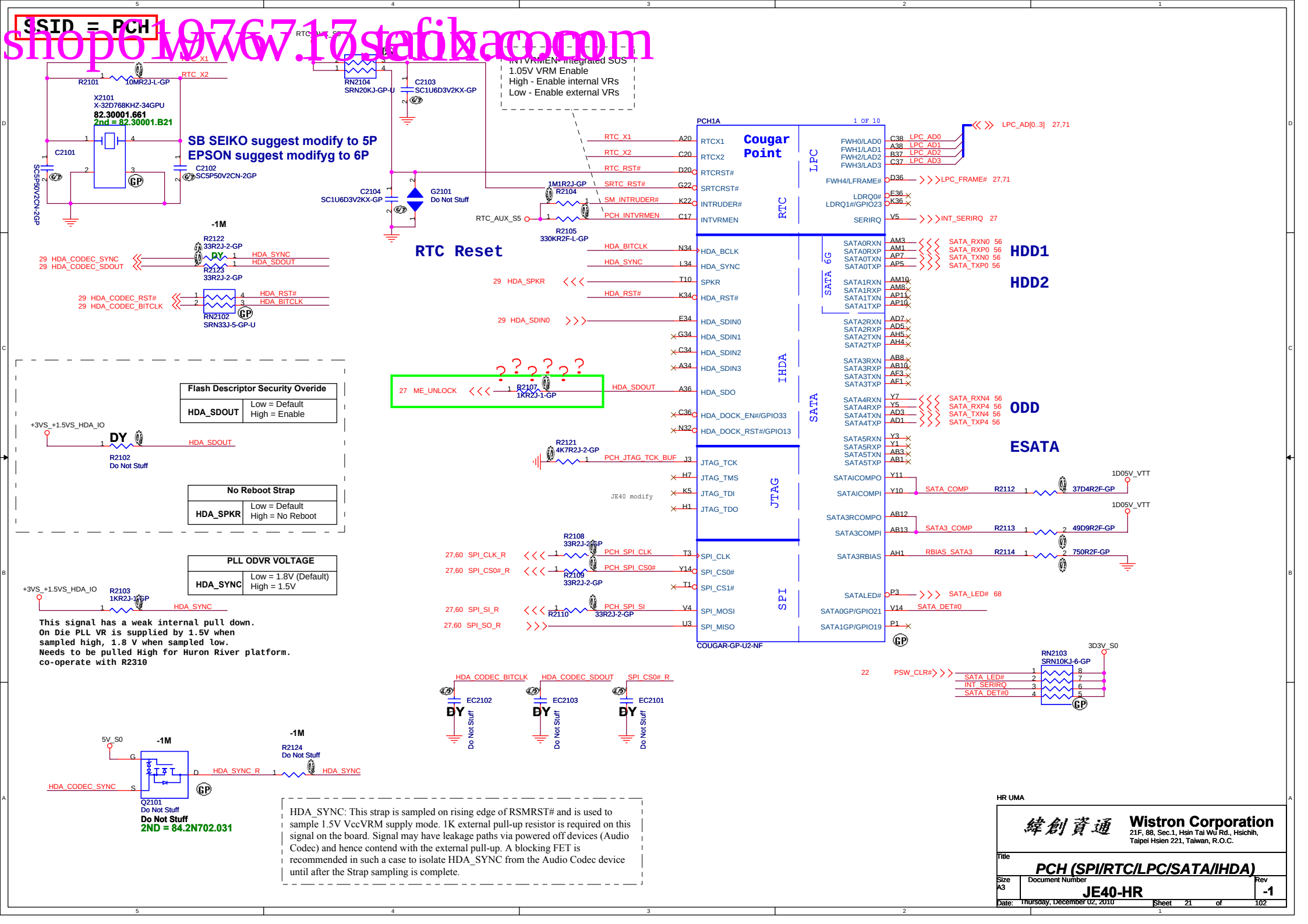
RTS

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

COUGAR-GP-U2-NF

HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: PCH (PCI-E/SMBUS/CLOCK/CL)		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 20 of 102	



HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PCH (SPI/RTC/LPC/SATA/IHDA)***	
Size: A3	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 21 of 102	

SSID = PCH

Note:
For PCH debug with XDP, need to NO Stuff R2218

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

Pass Word Clear

JE40 delete G Sensor

SB add Zero ODD function

SB 公板 check different , check need modify or not check intel , R2204

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

SB VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

VRAM Size

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

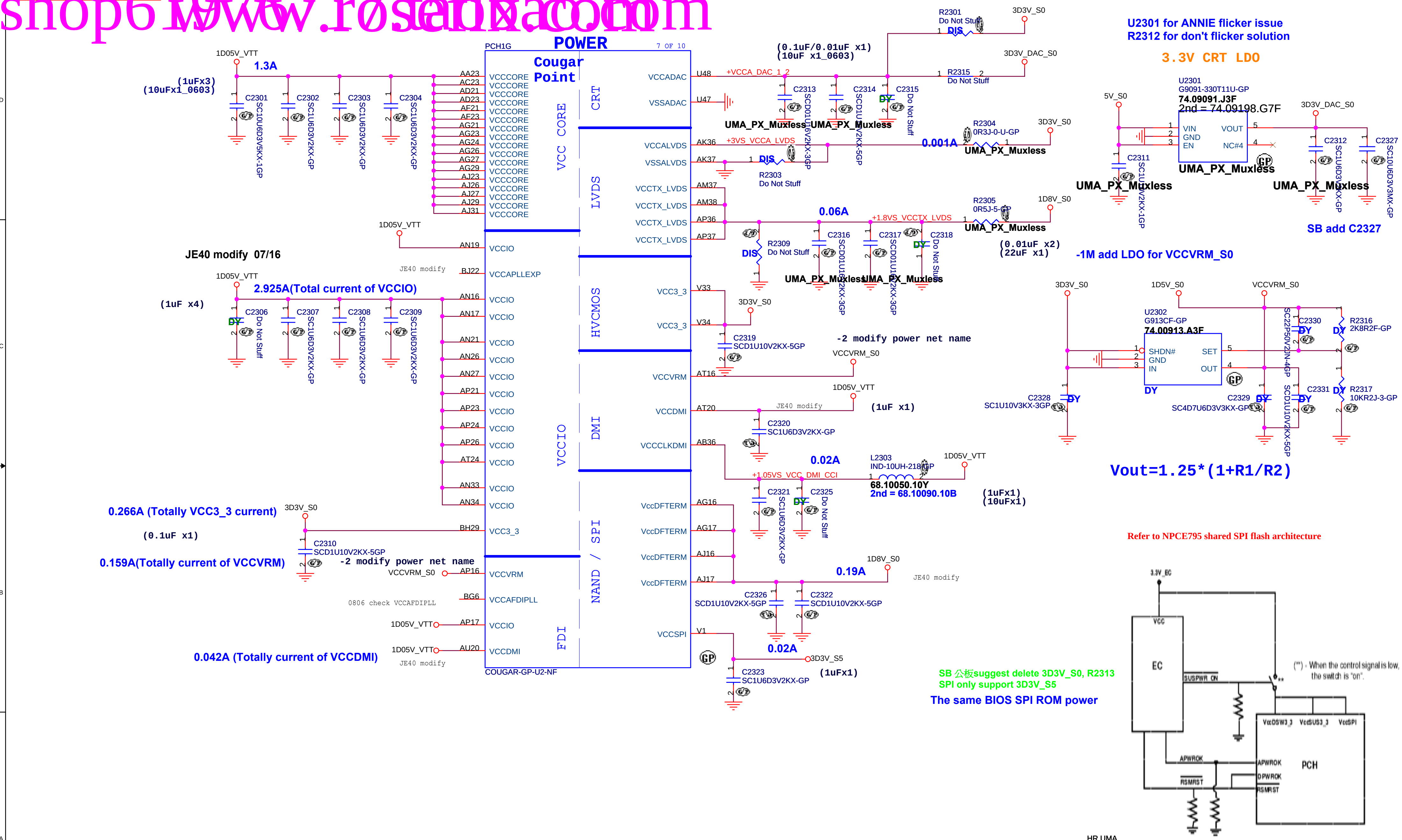
HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

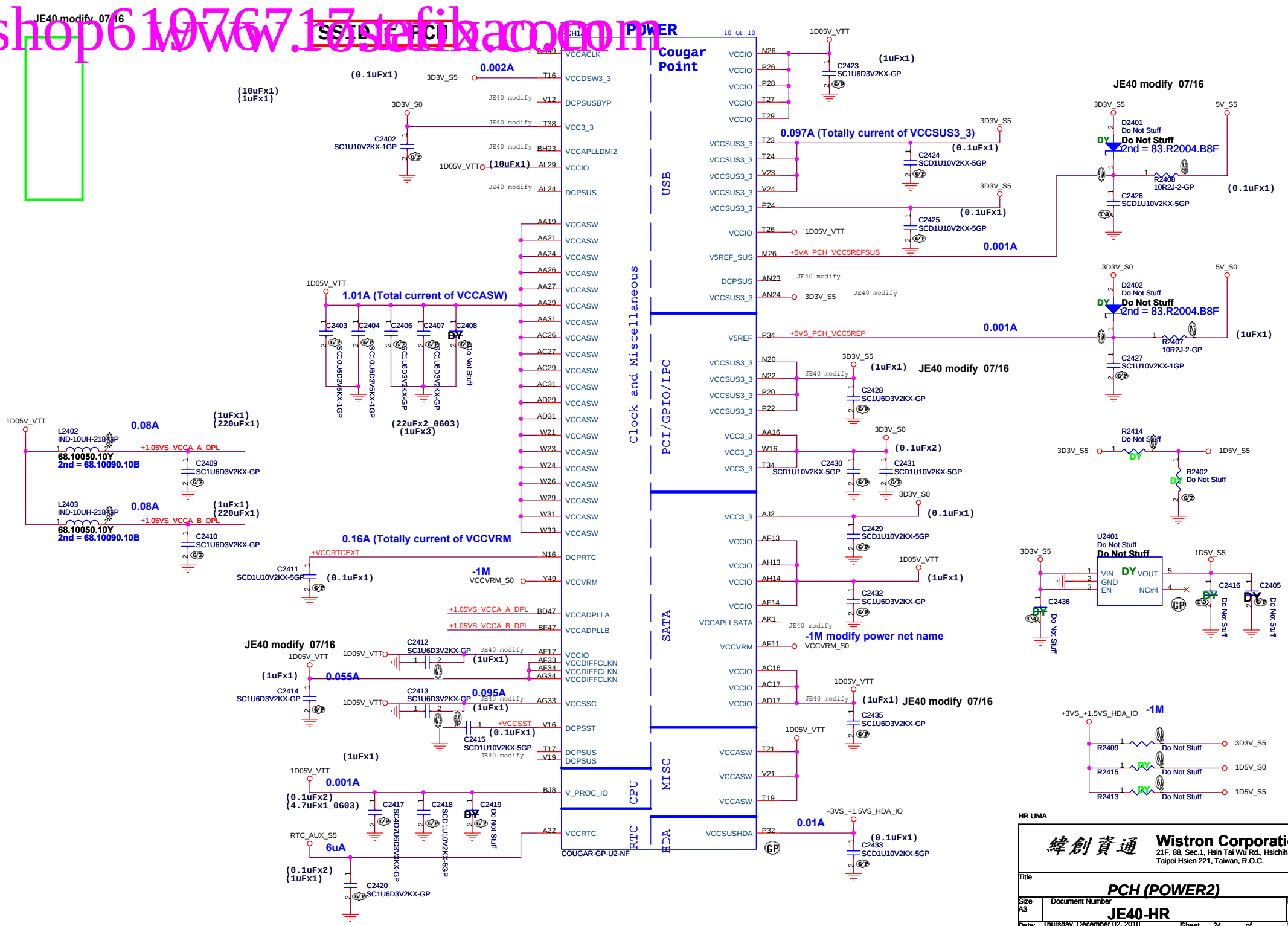
Size	Document Number	Rev
A3	JE40-HR	-1

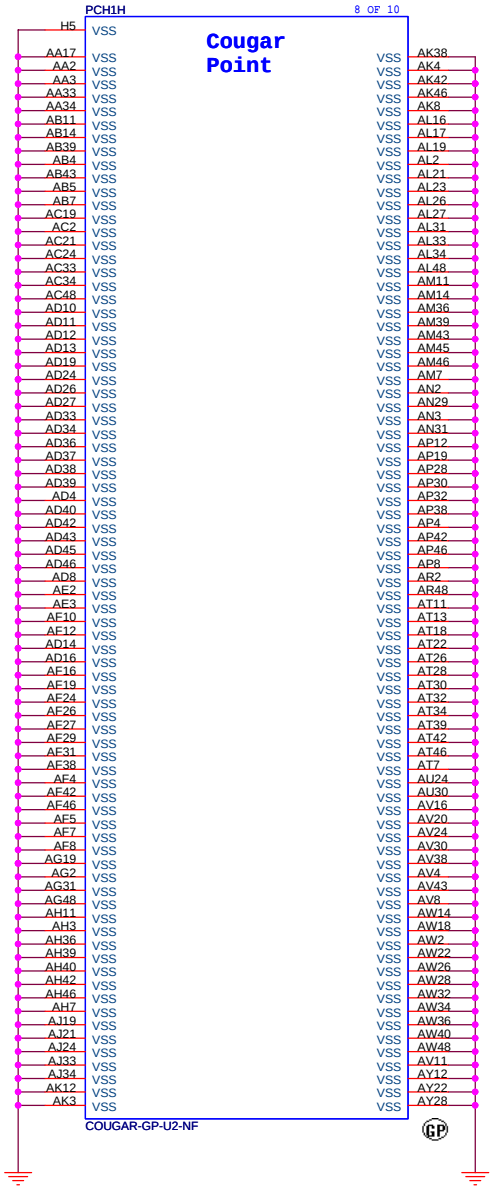
Date: Thursday, December 02, 2010 Sheet 22 of 102

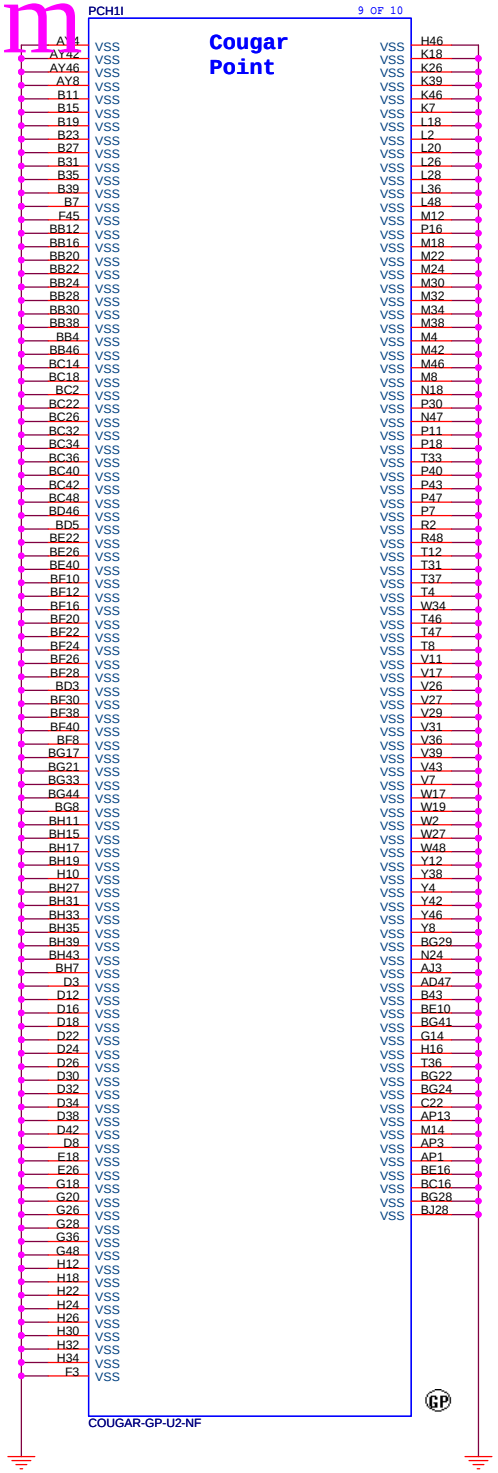


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	**PCH (POWER1)**	
Size A3	Document Number **JE40-HR**	Rev **-1**
Date: Thursday, December 02, 2010	Sheet 23 of 102	







HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 25 of 102

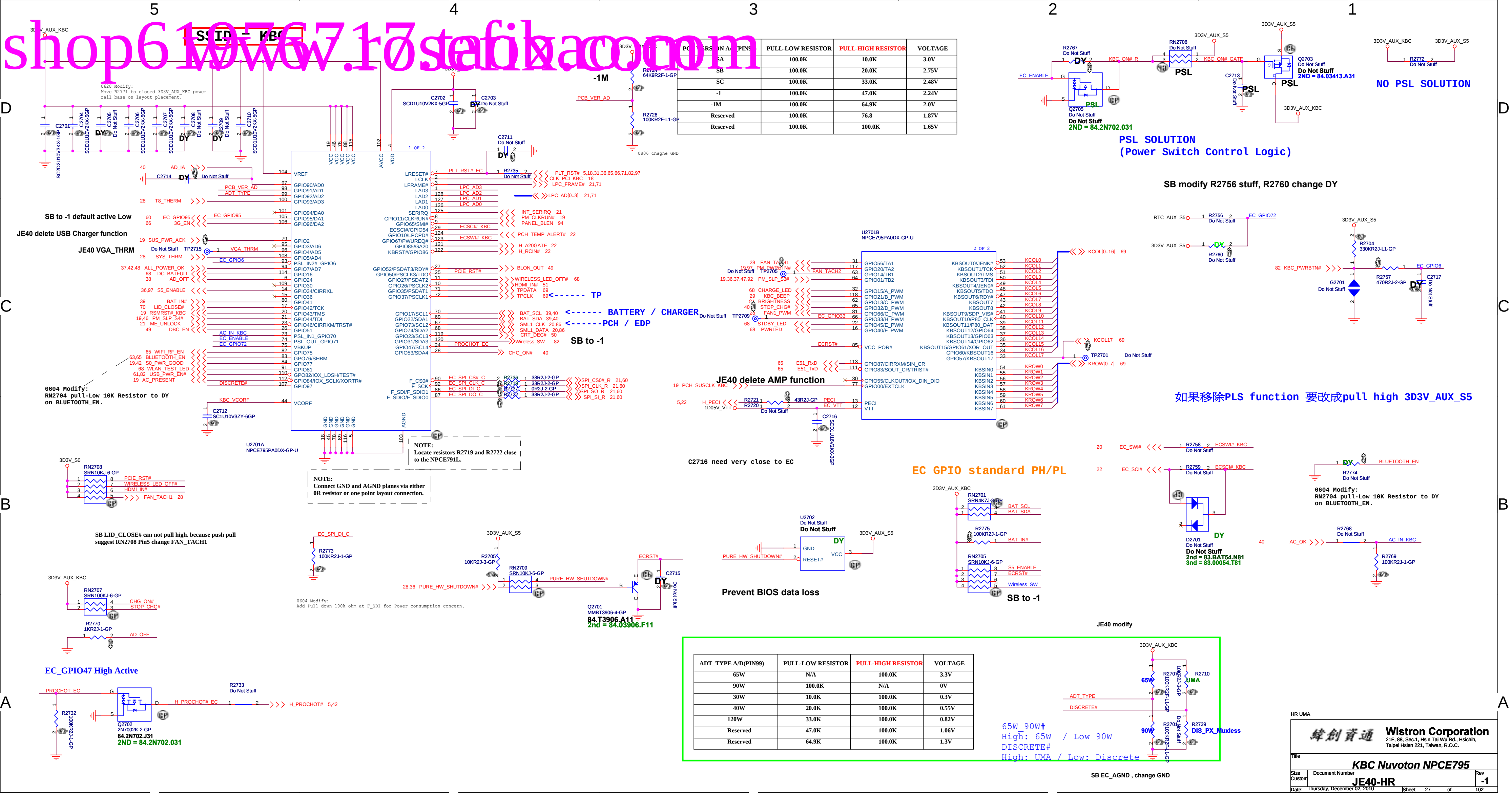
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Clock(colay)***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 26 of 102


SSID = KBC
3D3V_AUX_KBC
0628 Modify: Move R2771 to closed 3D3V_AUX_KBC power rail base on layout placement.
SB to -1 default active Low
JE40 delete USB Charger function
JE40 VGA_THRM
0604 Modify: RN2704 pull-Low 10K Resistor to DY on BLUETOOTH_EN.
U2701A NPCE795PA0DX-GP-U
NOTE: Locate resistors R2719 and R2722 close to the NPCE791L.
NOTE: Connect GND and AGND planes via either 0R resistor or one point layout connection.
SB LID_CLOSE# can not pull high, because push pull suggest RN2708 Pin5 change FAN_TACH1
0604 Modify: Add Pull down 100k ohm at F_SDI for Power consumption concern.
EC_GPIO47 High Active
TP
BATTERY / CHARGER
PCH / EDP
SB to -1
-1M
0806 chagne GND
PSL SOLUTION
(Power Switch Control Logic)
NO PSL SOLUTION
SB modify R2756 stuff, R2760 change DY
U2701B NPCE795PA0DX-GP-U
JE40 delete AMP function
C2716 need very close to EC
EC GPIO standard PH/PL
如果移除PLS function 要改成pull high 3D3V_AUX_S5
0604 Modify: RN2704 pull-Low 10K Resistor to DY on BLUETOOTH_EN.
Prevent BIOS data loss
SB to -1
JE40 modify
65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
SB EC_AGND , change GND

PCB VERSION A/D(PIN9?)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
-1M	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

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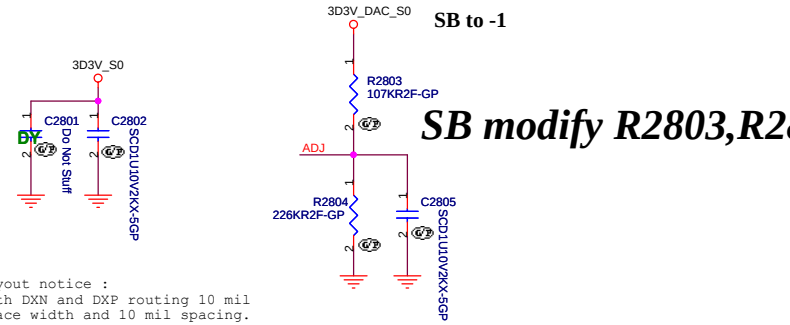
Title: KBC Nuvoton NPCE795

Document Number: JE40-HR — Rev -1

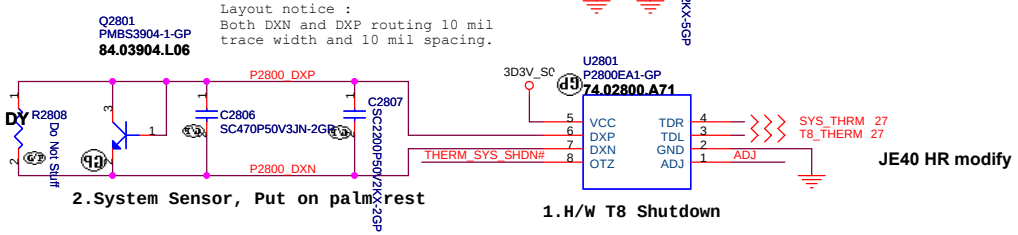
Date: Thursday, December 02, 2010 — Sheet 27 of 102

SSID = Thermal_Thermal sensor P2800

Thermal sensor P2800



SB modify R2803,R2804 setting



JE40 HR modify

ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

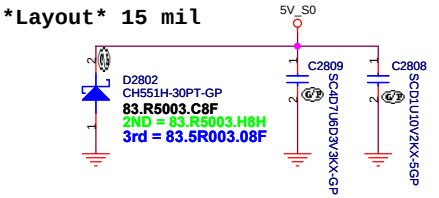
RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

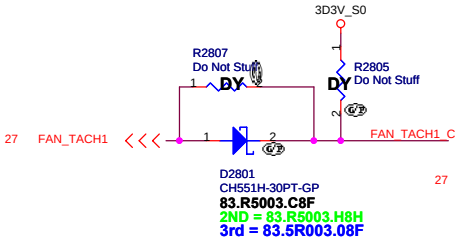
VGA Thermal sensor P2800

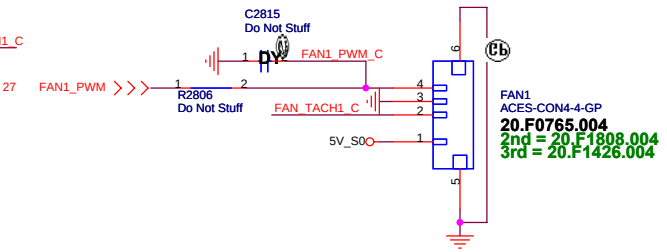
SMBUS modify to Page 84

Fan controller P2793

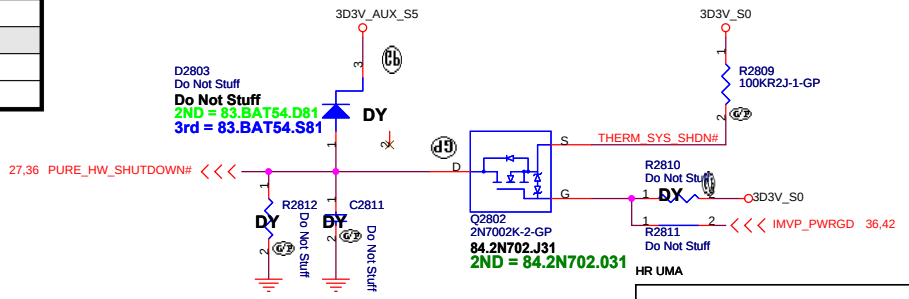
Layout 15 mil







For PWM FAN



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793

Size	Document Number	Rev
Custom	JE40-HR	-1

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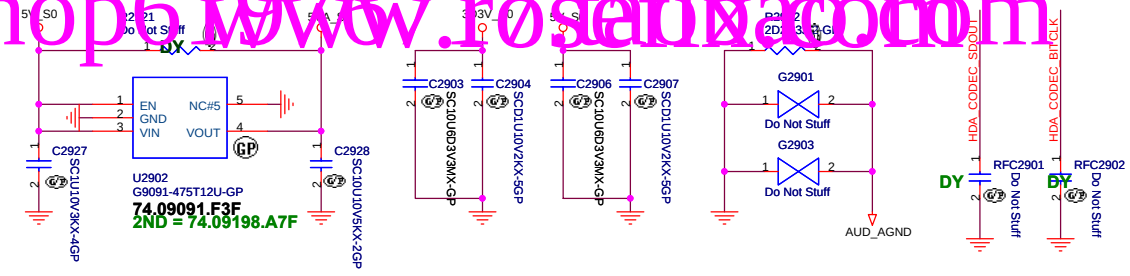
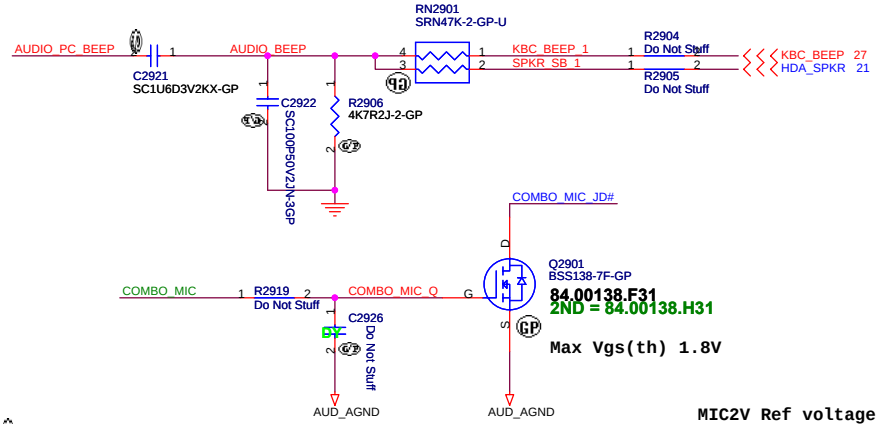


-1 PVDD timeing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎

CLOSE TO PIN1 and 9

CLOSE TO PIN39 and 46



MIC2V Ref voltage is 2.5V becasue Vgs(th)concern cann't use 2N702 for desing

HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 29 of 102

AUDIO OP AMP CIRCUIT

JE40 delete AMP function

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Audio AMP*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 30 of 102	

SB modify L3101,2,4,5,6 to 0 ohm

SB modify R3102 DY, R3104 to pull low

SB mmodify vendor suggest

SB delete EEPROM

128K byte

SB delete R3112

SB delete R3117

SB delete R3129 for LDO power

Card-reader Off-Page

Check VDDO_CR power plan

SB for B version

SB for B version can no use LDO delete LDO

SB to -1 modify to short pad

SB C3134, C3135 change 15P

68.00248.011
2nd = 68.00217.241

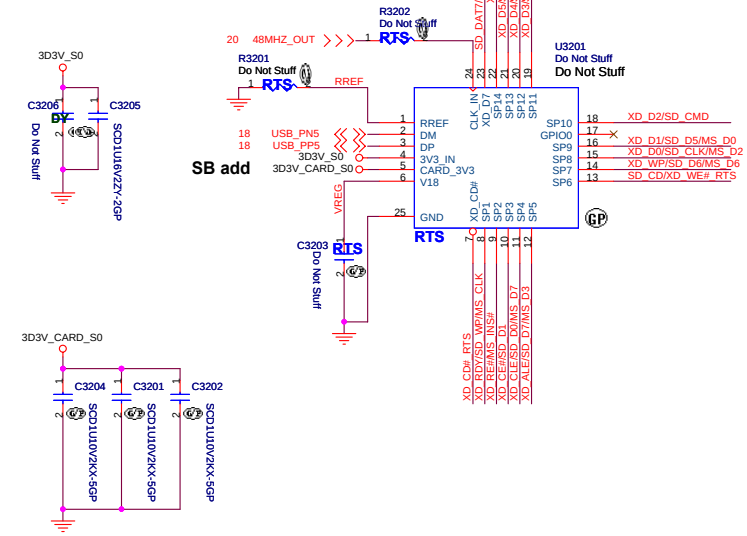
82.30020.851

71.57785.M02
Change:71.57785.M03

10月底改打71.57785.M03

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	BCM57780
Size: Custom	Document Number: JE40-HR
Rev	-1
Date: Thursday, December 02, 2010	Sheet 31 of 102

SB modify add 0 ohm



Near CARD1 Pin11, Pin18, Pin22

RN3209 Do Not Stuff
XD_RDY/SD_WP/MS_CLK — MS-SCLK_17 74, SD-WP_2 74, XD-R/-B_38 74

RN3203 Do Not Stuff
XD_CE#/SD_D1, XD_CE#/SD_D1, XD_RE#/MS_INS#, XD_RE#/MS_INS# — SD-DAT1_3 74, XD_CE#_36 74, MS_INS#_14 74, XD_RE#_37 74

RN3202 Do Not Stuff
XD_ALE/SD_D7/MS_D3, XD_ALE/SD_D7/MS_D3, XD_CLE/SD_D0/MS_D7, XD_CLE/SD_D0/MS_D7 — MS-DATA3_15 74, XD_ALE_34 74, SD_DAT0_4 74, XD_CLE_35 74

RN3211 Do Not Stuff
XD_D0/SD_CLK/MS_D2, XD_WP/SD_D6/MS_D6 — SD-CLK_9 74, MS-DATA2_12 74, XD_D0_30 74, XD_WP_32 74

RN3204 Do Not Stuff
XD_D2/SD_CMD, XD_D2/SD_CMD, XD_D1/SD_D5/MS_D0, XD_D1/SD_D5/MS_D0 — SD_CMD_16 74, XD_D2_28 74, MS_DATA0_10 74, XD_D1_29 74

RN3207 Do Not Stuff
XD_D4/SD_D3/MS_D1, XD_D4/SD_D3/MS_D1, XD_D4/SD_D3/MS_D1, XD_D3/SD_D4/MS_D4 — SD-DATA3_19 74, MS-DATA1_8 74, XD_D4_26 74, XD_D3_27 74

RN3201 Do Not Stuff
XD_D6/MS_BS, XD_D6/MS_BS, XD_D5/SD_D2/MS_D5, XD_D5/SD_D2/MS_D5 — MS_BS_7 74, XD_D6_24 74, SD-DATA1_21 74, XD_D5_25 74

RN3216 Do Not Stuff
SD_DAT7/XD_D7/MS_D7_RTS, XD_CD#_RTS, SD_CD/XD_WE#_RTS — XD_D7_23 74, XD_CD#_39 74, SD_CD/XD_WE#_1_33_43 74

RN3210 SRN0J-7-GP
31 SD_CLK/XD_R/B# — MS-SCLK_17 74, SD-CLK_9 74, XD-R/-B_38 74
31 XD_CD# — XD_CD#_39 74

RN3206 SRN0J-7-GP
31 XD_CE#/MS_INS# — MS_INS#_14 74, XD_CE#_36 74
31 XD_WP#/SD_WP# — SD-WP_2 74, XD_WP_32 74

SB to -1

-1M

R3205 100R2J-2-GP
31 SD_DAT1/XD_D1/MS_D1 — MS-DATA1_8 74

RN3213 SRN47J-4-GP
31 SD_DAT1/XD_D1/MS_D1, 31 SD_DAT1/XD_D1/MS_D1, 31,74 SD_CD/XD_WE# — SD-DAT1_3 74, XD_D1_29 74, SD_CD/XD_WE#_1_33_43 74

R3206 100R2J-2-GP
31 SD_DAT0/XD_D0/MS_D2 — MS_DATA0_10 74

RN3214 SRN47J-4-GP
31 SD_DAT0/XD_D0/MS_D2, 31 SD_DAT0/XD_D0/MS_D2, 31 XD_RE# — SD_DATA0_4 74, XD_D0_30 74, XD_RE#_37 74

R3203 100R2J-2-GP
31 SD_DAT3/XD_D3/MS_D2 — MS-DATA3_15 74

RN3205 SRN47J-7-GP
31 SD_DAT3/XD_D3/MS_D2, 31 SD_DAT3/XD_D3/MS_D2 — SD-DATA3_19 74, XD_D3_27 74

R3204 100R2J-2-GP
31 SD_CMD/XD_CLE/MS_B — MS_BS_7 74

RN3208 SRN47J-7-GP
31 SD_CMD/XD_CLE/MS_B, 31 SD_CMD/XD_CLE/MS_B — SD_CMD_16 74, XD_CLE_35 74

R3207 100R2J-2-GP
31 SD_DAT2/XD_D2/MS_D2 — MS-DATA2_12 74

RN3212 SRN47J-4-GP
31 SD_DAT2/XD_D2/MS_D2, 31 SD_DAT2/XD_D2/MS_D2, 31 XD_ALE — SD-DATA1_21 74, XD_D2_28 74, XD_ALE_34 74

RN3215 SRN47J-4-GP
31 SD_DAT4/XD_D4/MS_D4 — XD_D4_26 74
31 SD_DAT5/XD_D5/MS_D5 — XD_D5_25 74
31 SD_DAT6/XD_D6/MS_D6 — XD_D6_24 74
31 SD_DAT7/XD_D7/MS_D7 — XD_D7_23 74

HR UMA

-1M

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RTS5159 (CARD READER)	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 32 of 102	

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HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 33 of 102	

(Blanking)

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

Size	Document Number	Rev
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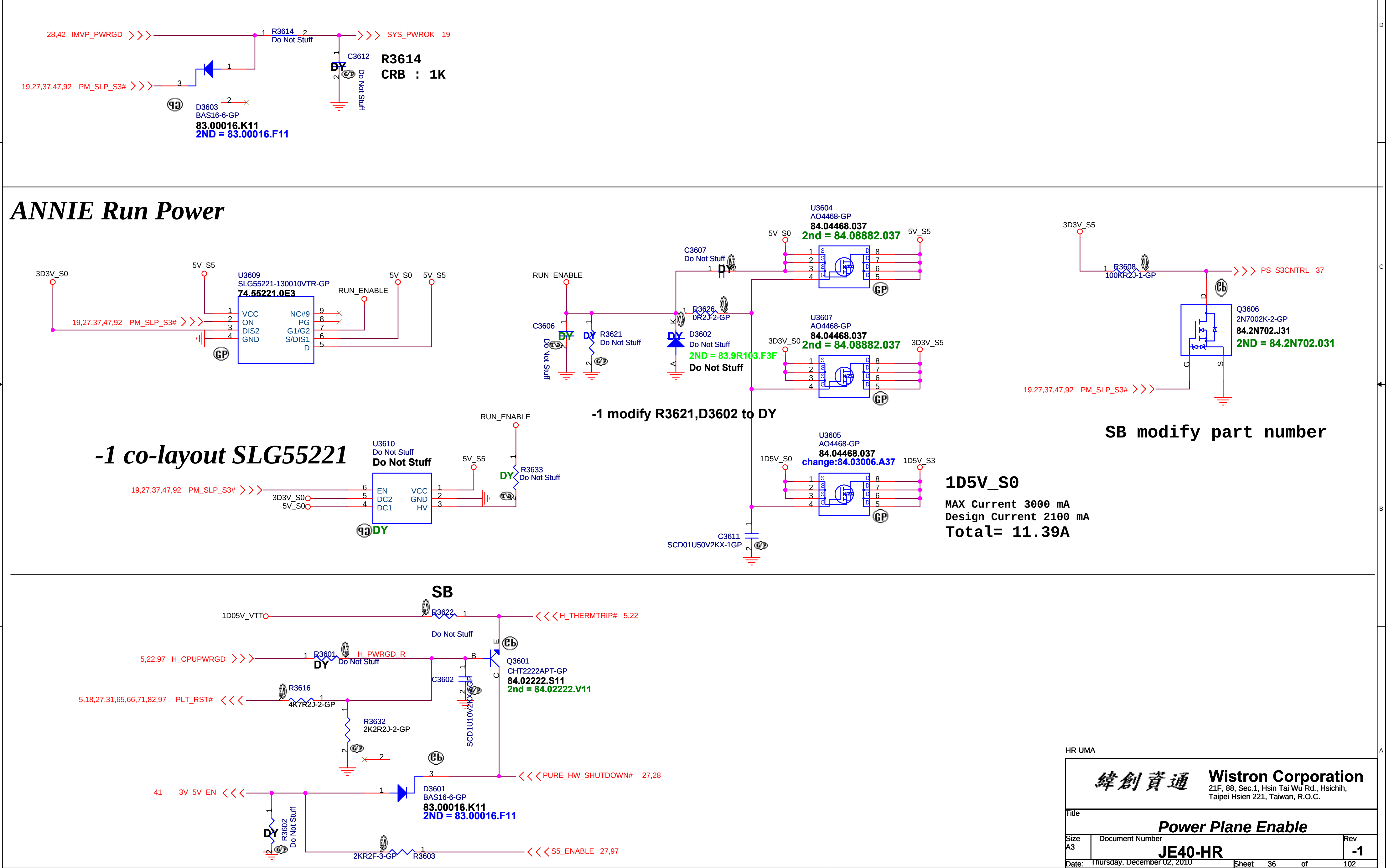
Power Sequence

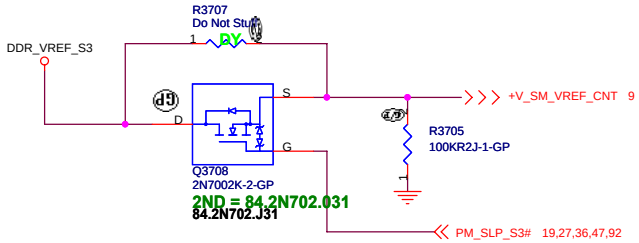

28,42 IMVP_PWRGD
R3614
Do Not Stuff
SYS_PWROK 19
19,27,37,47,92 PM_SLP_S3#
C3612
DY
Do Not Stuff
R3614
CRB : 1K
D3603
BAS16-6-GP
83.00016.K11
2ND = 83.00016.F11
ANNIE Run Power
3D3V_S0
5V_S5
U3609
SLG55221-130010VTR-GP
74.55221.0E3
RUN_ENABLE
5V_S0
5V_S5
VCC
ON
DIS2
GND
NC#9
PG
G1/G2
S/DIS1
D
19,27,37,47,92 PM_SLP_S3#
C3606
R3621
Do Not Stuff
R3626
0R2J-2-GP
D3602
Do Not Stuff
2ND = 83.9R103.F3F
Do Not Stuff
C3607
Do Not Stuff
U3604
AO4468-GP
84.04468.037
2nd = 84.08882.037
U3607
AO4468-GP
84.04468.037
2nd = 84.08882.037
3D3V_S0
3D3V_S5
U3605
AO4468-GP
84.04468.037
change:84.03006.A37
1D5V_S0
1D5V_S3
C3611
SCD01U50V2KX-1GP
-1 modify R3621,D3602 to DY
3D3V_S5
R3608
100KR2J-1-GP
PS_S3CNTRL 37
Q3606
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
19,27,37,47,92 PM_SLP_S3#
SB modify part number
-1 co-layout SLG55221
U3610
Do Not Stuff
Do Not Stuff
RUN_ENABLE
5V_S5
R3633
Do Not Stuff
19,27,37,47,92 PM_SLP_S3#
3D3V_S0
5V_S0
EN
DC2
DC1
VCC
GND
HV
1D5V_S0
MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A
SB
1D05V_VTT
R3622
Do Not Stuff
H_THERMTRIP# 5,22
5,22,97 H_CPUPWRGD
R3601
Do Not Stuff
H_PWRGD_R
C3602
SCD1U10V2KX-5GP
Q3601
CHT2222APT-GP
84.02222.S11
2nd = 84.02222.V11
5,18,27,31,65,66,71,82,97 PLT_RST#
R3616
4K7R2J-2-GP
R3632
2K2R2J-2-GP
PURE_HW_SHUTDOWN# 27,28
41 3V_5V_EN
D3601
BAS16-6-GP
83.00016.K11
2ND = 83.00016.F11
R3602
Do Not Stuff
2KR2F-3-GP
R3603
S5_ENABLE 27,97

HR UMA

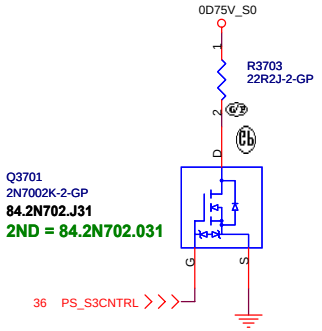
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Power Plane Enable		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 36 of 102	

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

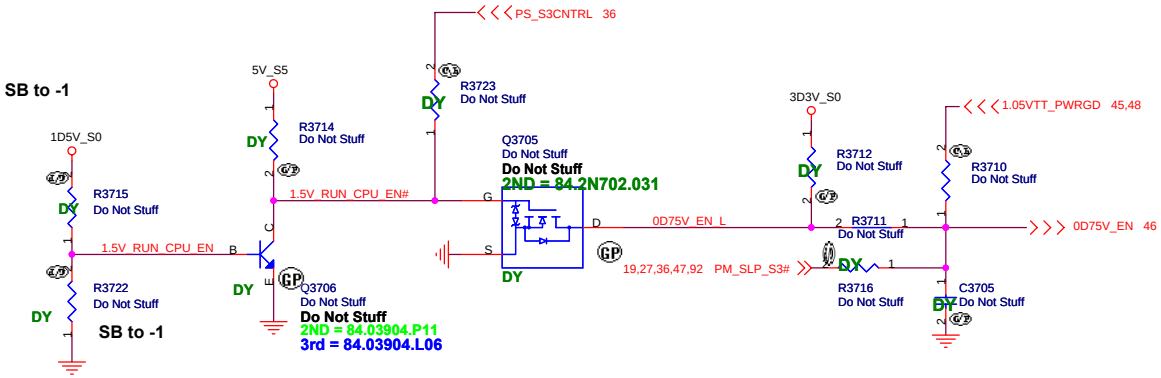


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

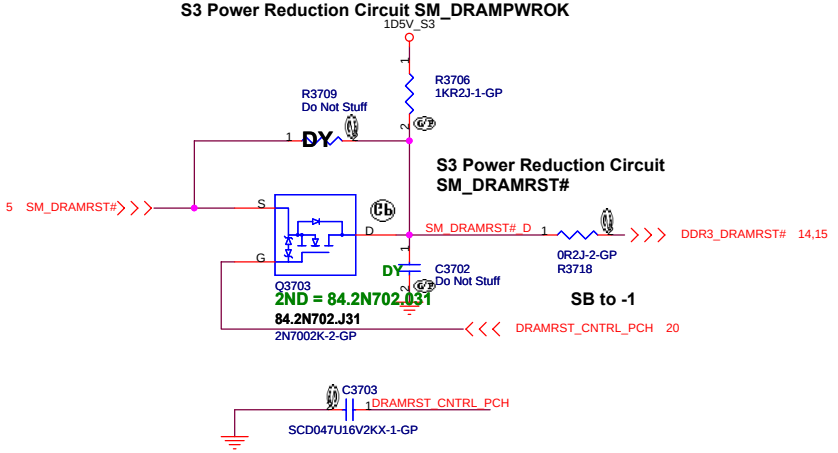


⑤ S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

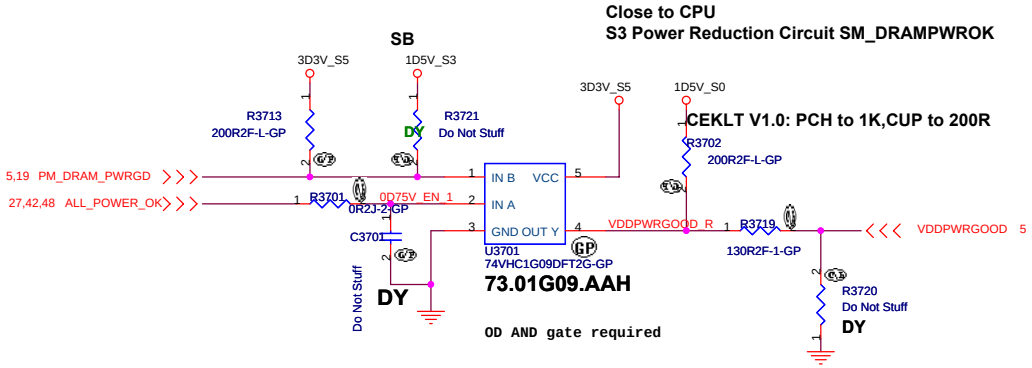
SB to -1 reserve R3723



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time
over VDDQ * 0.55± 200mV and the edge must be monotonic

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

Size	Document Number	Rev
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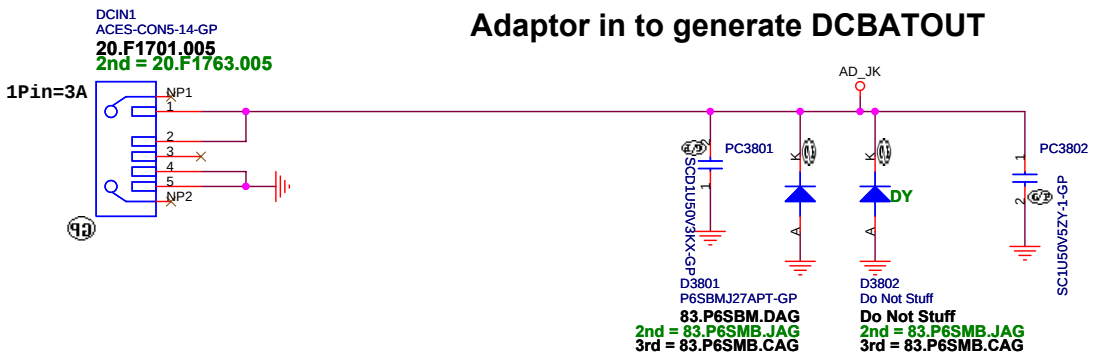
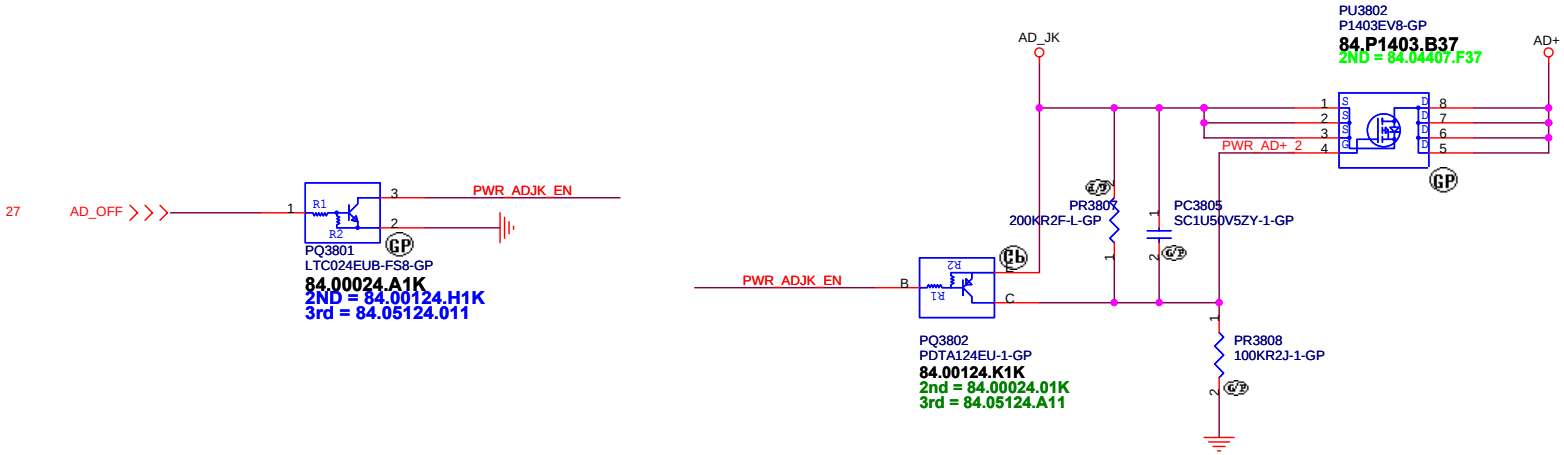
Adaptor in to generate DCBATOUT



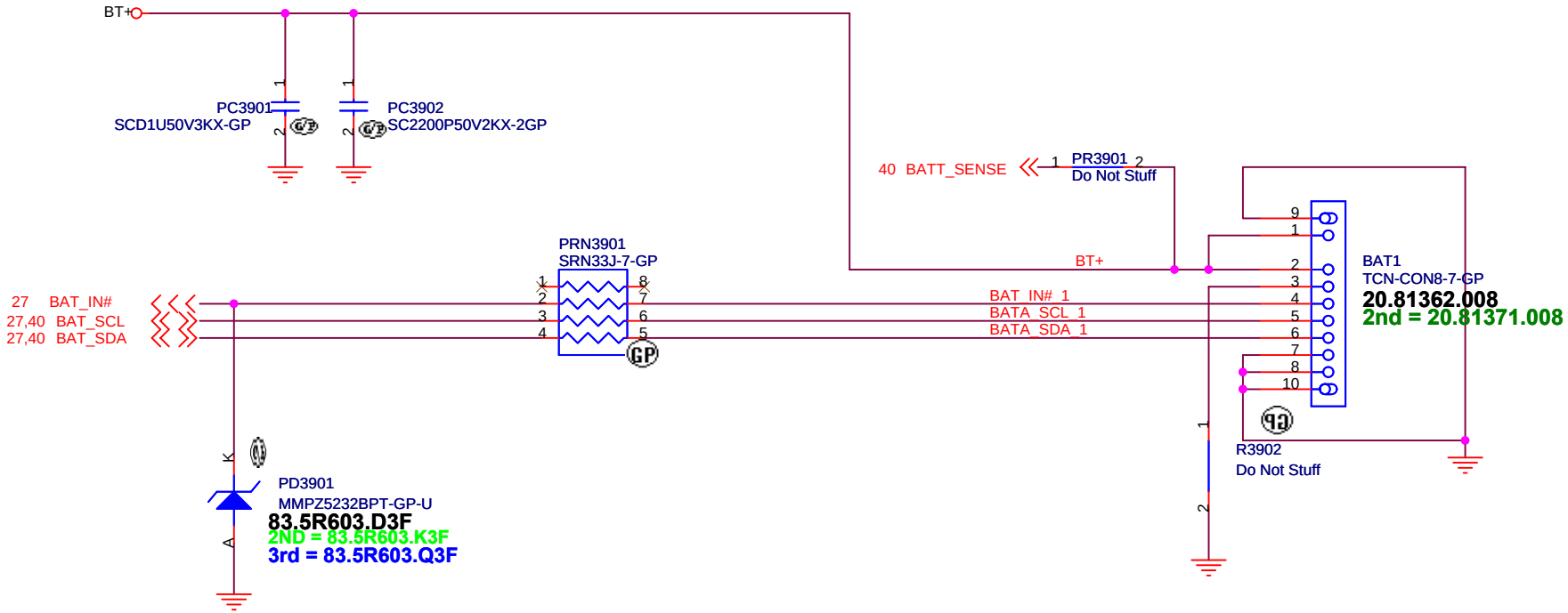
JE40 change DCIN1 part number



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN JACK*		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 38 of 102	

BATTERY CONNECTOR



EC Protect

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BATT CONN		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 39 of 102	

AD+ total power	R1	R2
65w	121k	49.9k
90w	121k	49.9k

AD+ total power	R1	R2
90w	137k	49.9k

NEAR

ADD A 24V ZENAR

20100706 Wayne

20100721

20101018

JE40 HR RF

-1M

-1M

AC_OK to KBC

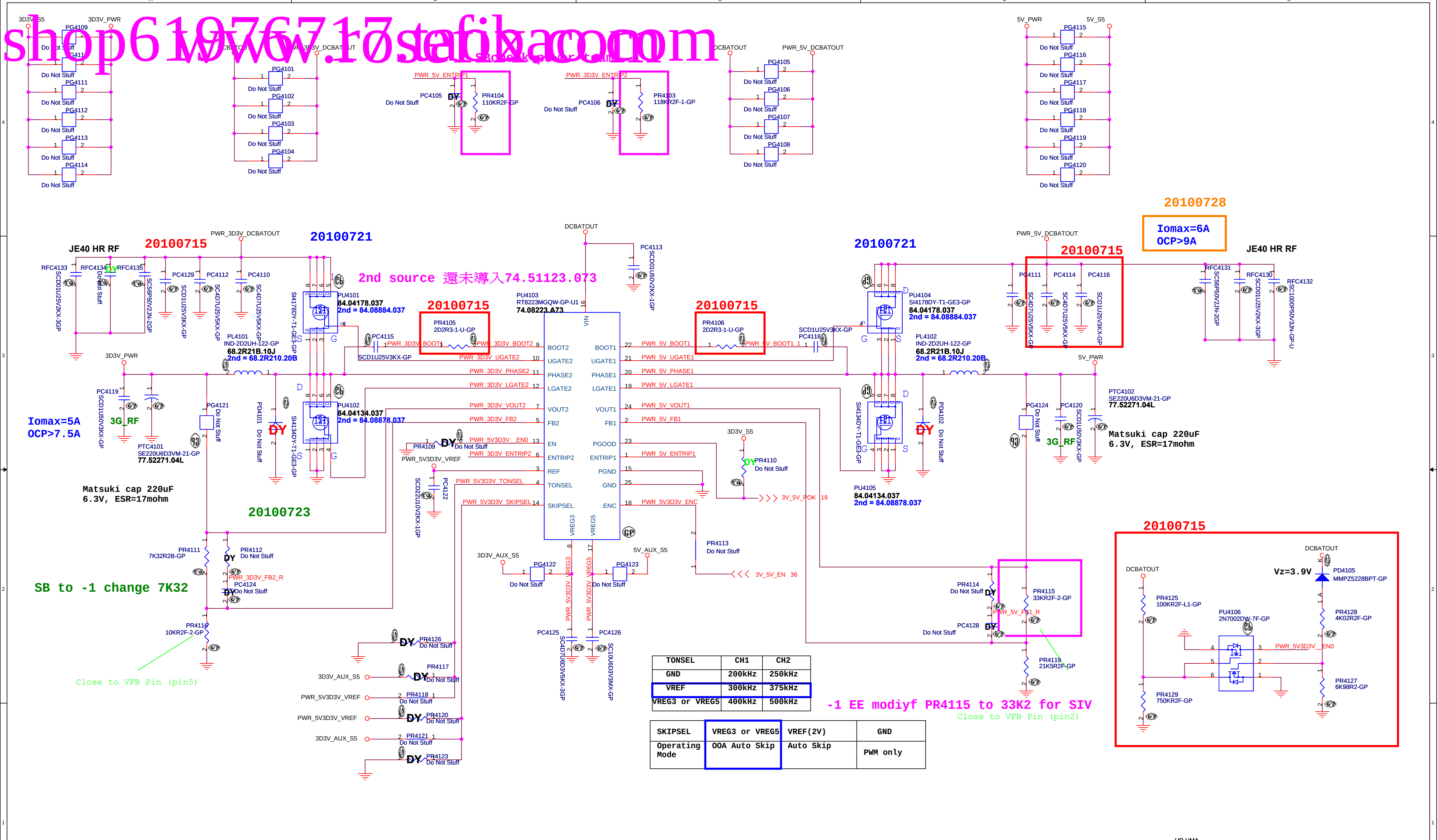
HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 40 of 102


JE40 HR RF
20100715
20100721
2nd source 還未導入74.51123.073
20100728
Iomax=6A
OCP>9A
Iomax=5A
OCP>7.5A
Matsuki cap 220uF
6.3V, ESR=17mohm
20100723
SB to -1 change 7K32
Close to VFB Pin (pin5)
-1 EE modiyf PR4115 to 33K2 for SIV
Close to VFB Pin (pin2)
Vz=3.9V
PU4103
RT8223MQW-GP-U1
74.08223.A73
PU4101
84.04178.037
2nd = 84.08884.037
PU4102
84.04134.037
2nd = 84.08878.037
PU4104
SI4178DY-T1-GE3-GP
84.04178.037
2nd = 84.08884.037
PU4105
84.04134.037
2nd = 84.08878.037
PL4101
IND-2D2UH-122-GP
68.2R21B.10J
2nd = 68.2R210.20B
PL4102
IND-2D2UH-122-GP
68.2R21B.10J
2nd = 68.2R210.20B
PTC4101
SE220U6D3VM-21-GP
77.52271.04L
PTC4102
SE220U6D3VM-21-GP
77.52271.04L
PR4105
2D2R3-1-U-GP
PR4106
2D2R3-1-U-GP
PR4115
33KR2F-2-GP
PR4119
21K5R2F-GP
PR4111
7K32R2B-GP
PR4116
10KR2F-2-GP
PR4125
100KR2F-L1-GP
PR4128
4K02R2F-GP
PR4127
6K98R2-GP
PR4129
750KR2F-GP
PU4106
2N7002DW-7F-GP
PD4105
MMPZ5228BPT-GP
DCBATOUT
PWR_3D3V_DCBATOUT
PWR_5V_DCBATOUT
3D3V_PWR
5V_PWR
3D3V_S5
5V_S5
3D3V_AUX_S5
5V_AUX_S5
PWR_5V3D3V_VREF
3V_5V_POK 19
3V_5V_EN 36
Do Not Stuff

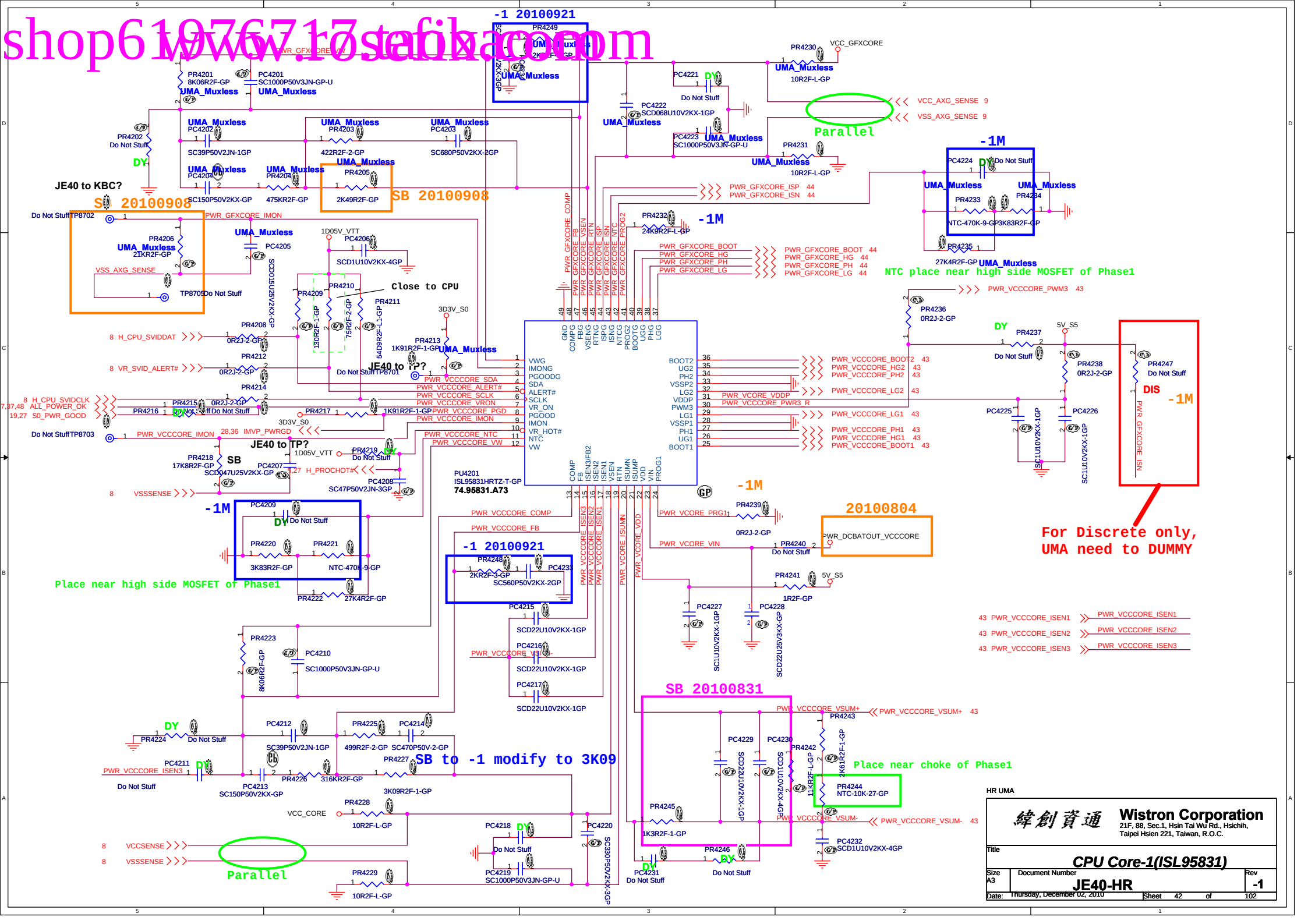
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

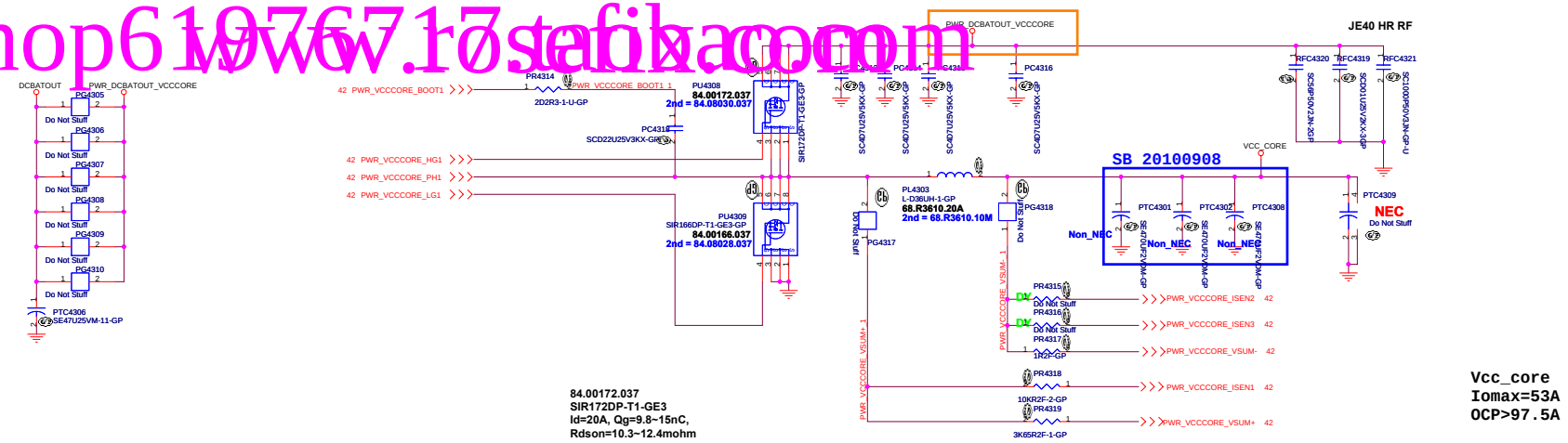
SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

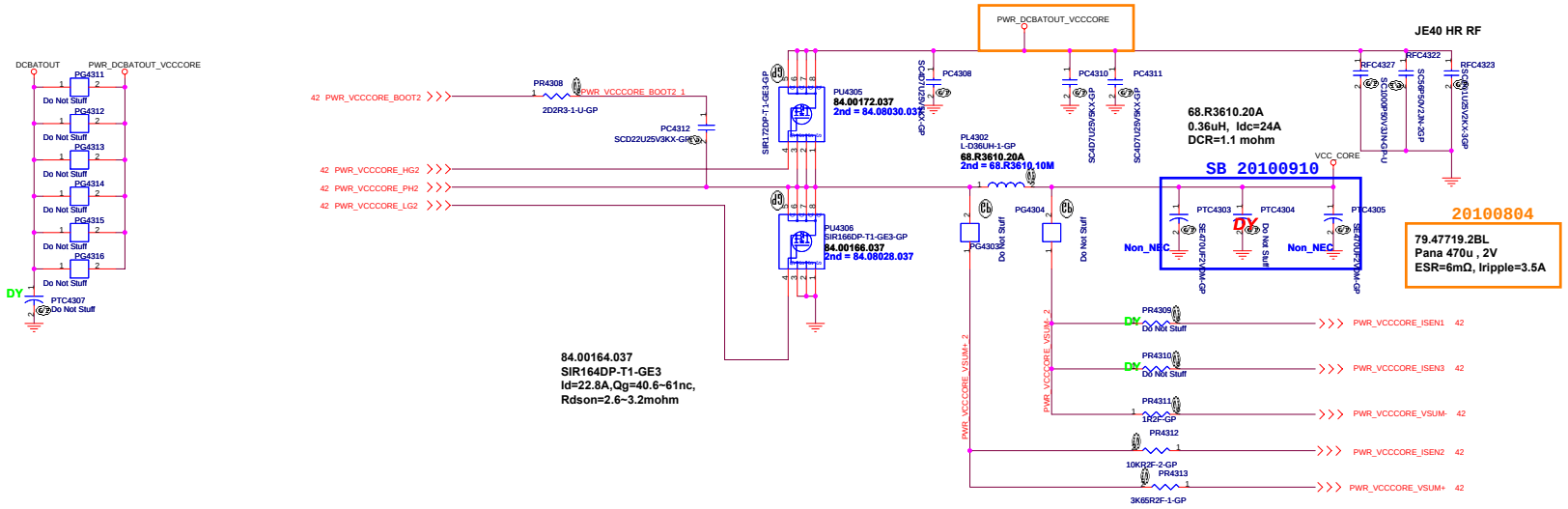
HR UMA

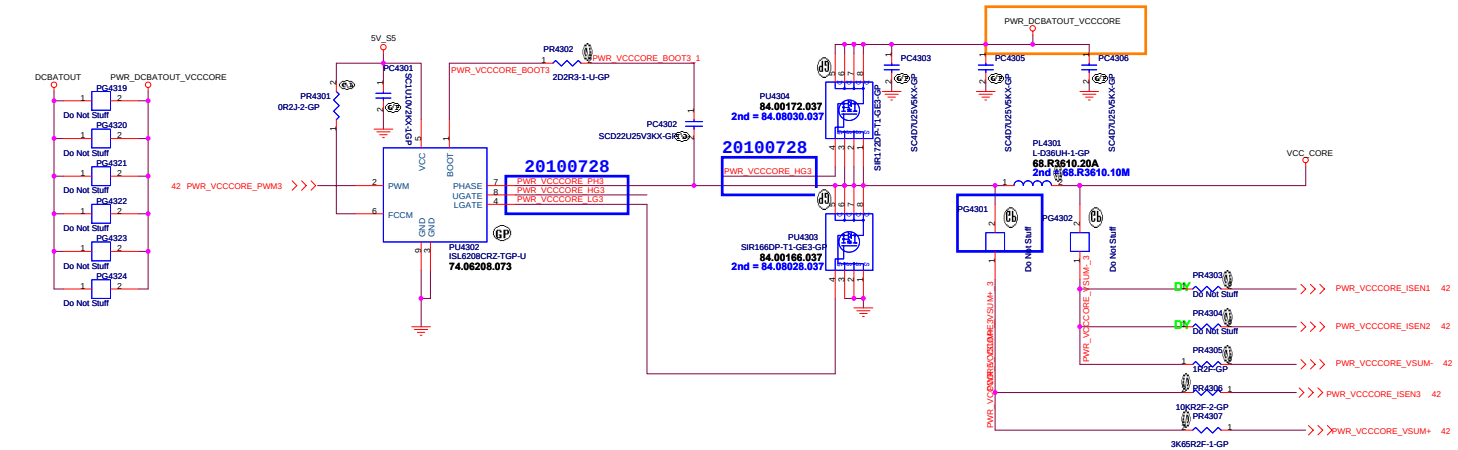
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	5V/3D3V(RT8223M)	
Size Custom	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010	Sheet 41 of 102	









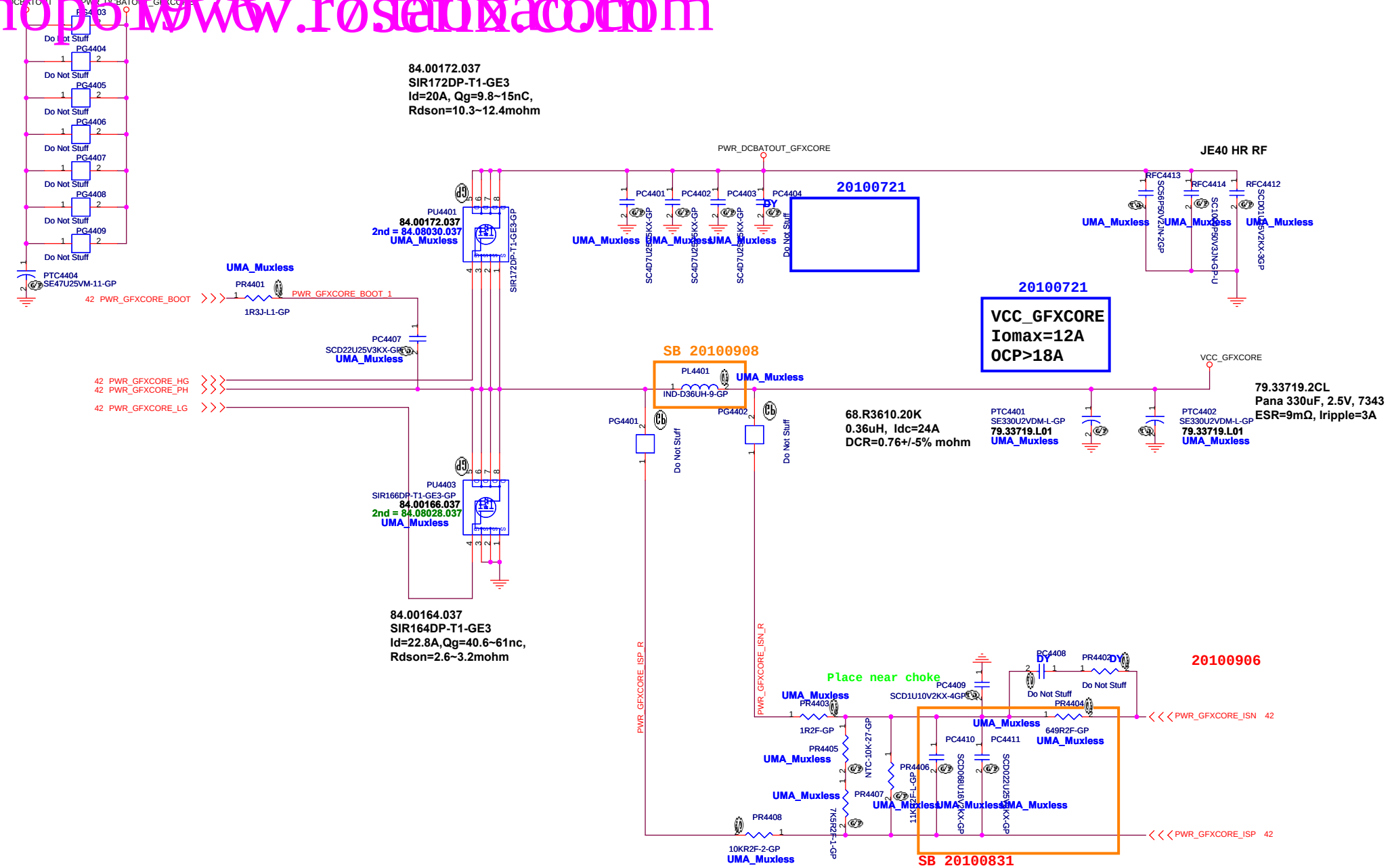
HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Core-2(ISL95831)

Size: A2 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 43 of 102



HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU Core-3(ISL95831)	
Size A3	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010	Sheet 44 of 102	

TPS51218D for 1D05V

DCBATOUT
PWR_DCBATOUT_1D05V
PG4501 Do Not Stuff
PG4502 Do Not Stuff
PG4503 Do Not Stuff
PG4504 Do Not Stuff
PTC4501 Do Not Stuff
DY

PWR_DCBATOUT_1D05V
JE40 HR RF
RFC4512 SC56P50V2JN-2GP
RFC4513 SC100P50V3JN-GP-U
RFC4514 SCD01U25V2KX-3GP

1D05V_VTT PG4513 Do Not Stuff
1D05V_PWR PG4505 Do Not Stuff
PG4514 Do Not Stuff
PG4506 Do Not Stuff
PG4515 Do Not Stuff
PG4507 Do Not Stuff
PG4516 Do Not Stuff
PG4508 Do Not Stuff
PG4517 Do Not Stuff
PG4510 Do Not Stuff
PG4518 Do Not Stuff
PG4509 Do Not Stuff
PG4519 Do Not Stuff
PG4511 Do Not Stuff
PG4520 Do Not Stuff
PG4512 Do Not Stuff

PWR_DCBATOUT_1D05V
PC4504 SC47U25V5KX-GP
PC4506 SC47U25V5KX-GP
PC4507 SCD01U25V2KX-3GP
PC4511 SCD1U25V3KX-GP

20100728
Id=12.9A
Qg=9.8~15nC
Rdson=10.3~12.4mohm

PU4502
84.15N03.037
2nd = 84.08065.037
RMW150N03FUBGPJ

20100728
Iomax=14A
OCP>21A

2nd source 還未導入74.08237.073

Freq=360KHz

Mag. 0.56uH 10*10*4
DCR=1.6~1.8mohm
Idc=25A, Isat=40A

3D3V_S0
PR4516 10KR2J-3-GP
37,48 1.05VTT_PWRGD
46,47 RUNPWROK
PR4512 0R2J-2-GP
PC4505 SC1KP50V2KX-1GP
PR4504 82KR2F-1-GP
PR4503 470KR2F-GP

SB 20100831

PU4501
TPS51218DSCR-GP-U1
74.51218.073
PGOOD GND
TRIP VBST
EN DRVH
VFB SW
RF V5IN
DRVL
PWR_1D05V_IMAX
PWR_1D05V_EN
PWR_1D05V_VFB
PWR_1D05V_CCM
PWR_1D05V_BOOT
PWR_1D05V_UGATE
PWR_1D05V_PHASE
PWR_1D05V_LGATE

PR4505 2D2R3-1-U-GP
PC4503 SCD1U25V3KX-GP
PWR_1D05V_BOOT_R
5V_S5

PU4503
84.18003.037
2nd = 84.08062.037
RMW180N03FUBTB-GP

20100906
PL4501
IND-D56UH-27-GP
68.R5610.10P
2nd = 68.R5610.20H

1D05V_PWR
PC4508 SC18P50V2JN-1GP DY
PC4509 SCD1U50V3KX-GP 1G_RF
PTC4502 Do Not Stuff
PTC4503 SE330U2VDM-L-GP
Do Not Stuff 79.33719.L01
2nd = 77.C3371.0512nd = 77.C3371.051

PR4506 10R2F-L-GP
VTT_SENSE_L
PR4507 10KR2F-2-GP
PWR_1D05V_VFB
PR4508 20KR2F-L-GP
VSS_SENSE_L
PR4509 10R2F-L-GP
20100728

20100728
Id=19.4A
Qg=16.8~25.5nC
Rdson=4.9~6.1mohm

VTT_SENSE_L
PR4510 DY Do Not Stuff
PC4510 DY Do Not Stuff
VSS_SENSE_L
PR4511 DY Do Not Stuff
VCCIO_SENSE
VSSIO_SENSE

20100728
Vout=0.704*(1+R1/R2)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1D05V(TPS51218D)
Size: A3
Document Number: JE40-HR
Rev: -1
Date: Thursday, December 02, 2010
Sheet 45 of 102

S3ID - PWR_Plane_Regulator_1p5v0p75v

DCBATOUT

PWR_DCBATOUT_1D5V

PG4601 Do Not Stuff
PG4602 Do Not Stuff
PG4603 Do Not Stuff
PG4604 Do Not Stuff
PTC4601 Do Not Stuff

DY

19,27 PM_SLP_S4# → PR4612 Do Not Stuff → PWR_1D5V_EN

PC4612 Do Not Stuff

DY

20100805

RT8207L for 1D5V

SB 20100831

PWR_1D5V_VCC5
PR4604 5D1R2F-GP
5V_S5
PC4606 SC1U10V2KX-1GP
PC4602 SC1K50V2KX-1GP
PR4603 12K4R2F-GP
PWR_1D5V_CS
PWR_1D5V_VDDP
PR4605 Do Not Stuff
C694 SC1U10V2KX-1GP

3D3V_S5
PR4602 10KR2F-2-GP

Close to pin23

45,47 RUNPWROK
PWR_DCBATOUT_1D5V
PR4610 620KR2F-GP
PWR_1D5V_TON

20100728

PWR_1D5V_EN
PWR_0D75V_EN
PWR_1D5V_VTTIN
PC4603 SC10U6D3V5MX-3GP

1D5V_S3
PG4605 Do Not Stuff
PG4606 Do Not Stuff
PG4607 Do Not Stuff

DDR_VREF_PWR

Close to pin23

20100728

Iomax=1A
OCP>1.5A

Close to output cap pin1, not inside of the output cap

PU4601 RT8207LGQW-GP-U1 74.08207.B73

CS, VDD, VDDP, BOOT, UGATE, PHASE, LGATE, PGND, NC#17, VDDQ, FB, DEM, VTTREF, PGOOD, TON, S5, S3, VLDOIN, NC#7, VTTGND, MODE, VTT, VTTSNS, GND, GND

PWR_1D5V_BOOT
PWR_1D5V_UGATE
PWR_1D5V_PHASE
PWR_1D5V_LGATE
PWR_1D5V_VDDQ
PWR_1D5V_FB
5V_S5

PR4606 2D2R3-1-U-GP
PWR_1D5V_PHASE_L
PC4609 SCD1U25V3KX-GP

-1 PR4608 需要將來都改32k4R

R1 PR4608 33KR2F-GP
DY PC4610 Do Not Stuff
R2 PR4609 30KR2F-GP

2nd source 還未導入74.51116.073

PR4607 Do Not Stuff
DDR_VREF_S3
PWR_1D5V_VTTREF
PC4608 SCD033U16V2KX-GP

Close to PIN9

37 0D75V_EN → PR4615 Do Not Stuff → PWR_0D75V_EN

+0.75VS
Iomax: 1.2A

0D75V_S0
PG4608 Do Not Stuff
PG4609 Do Not Stuff
DDR_VREF_PWR
PC4604 SC10U6D3V5MX-3GP
PC4605 Do Not Stuff
DY

PWR_DCBATOUT_1D5V

JE40 HR RF

RFC4617 SC10U25V2KX-3GP
RFC4618 SC1000P50V3JN-GP-U
RFC4616 SC56P50V2JN-2GP

20100906

PC4611 PC4614 PC4616 PC4617 SC4D7U25V5KX-GP
PC4615 SCD1U25V3KX-GP

20100728

Id=12.9A
Qg=9.8~15nC
Rdson=10.3~12.4mohm

PU4602
84.15N03.037
2nd = 84.08065.037
RMW150N03FUB-GP-U1

PU4603
84.18003.037
2nd = 84.18002.037
RMW180N03FUBTB-GP

20100728

Id=19.4A
Qg=16.8~25.5nC
Rdson=4.9~6.1mohm

Mag. 1.0uH 10*10*4
DCR=2.9~3.3mohm
Idc=18A, Isat=36A

Iomax=12A
OCP>20A

PL4601
IND-1UH-93-GP
68.1R01B.10J
2nd = 68.1R01C.10Q

1D5V_S3
PC4613 Do Not Stuff
DY
PTC4602 SE390U2D5VM-7GP
79.3971V.30L
2nd = 79.3971V.6AL

Matsuki cap 390uF
2.5V, ESR=10mohm

Vout=0.75*(1+R1/R2)

SB R4608 chekc 修改31K6R
Vout 需再1.55V 以上

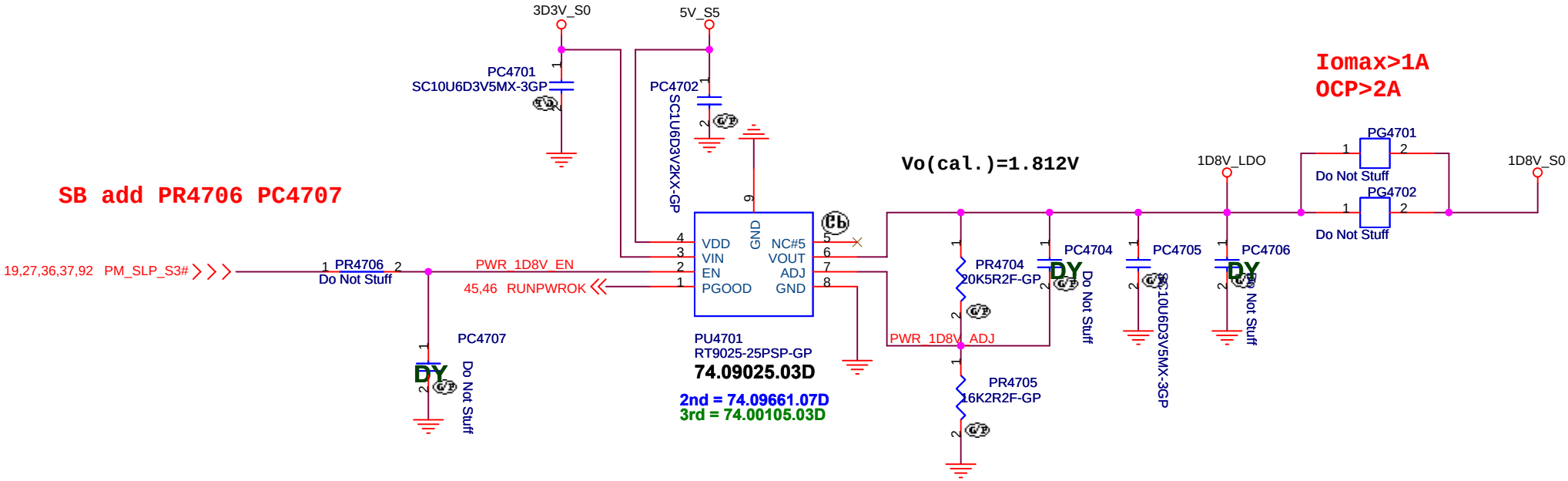
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS5111
Size: Custom
Document Number: JE40-HR
Rev: -1
Date: Thursday, December 02, 2010
Sheet 46 of 102

SSID = PWR.Plane.Regulator_1p8V

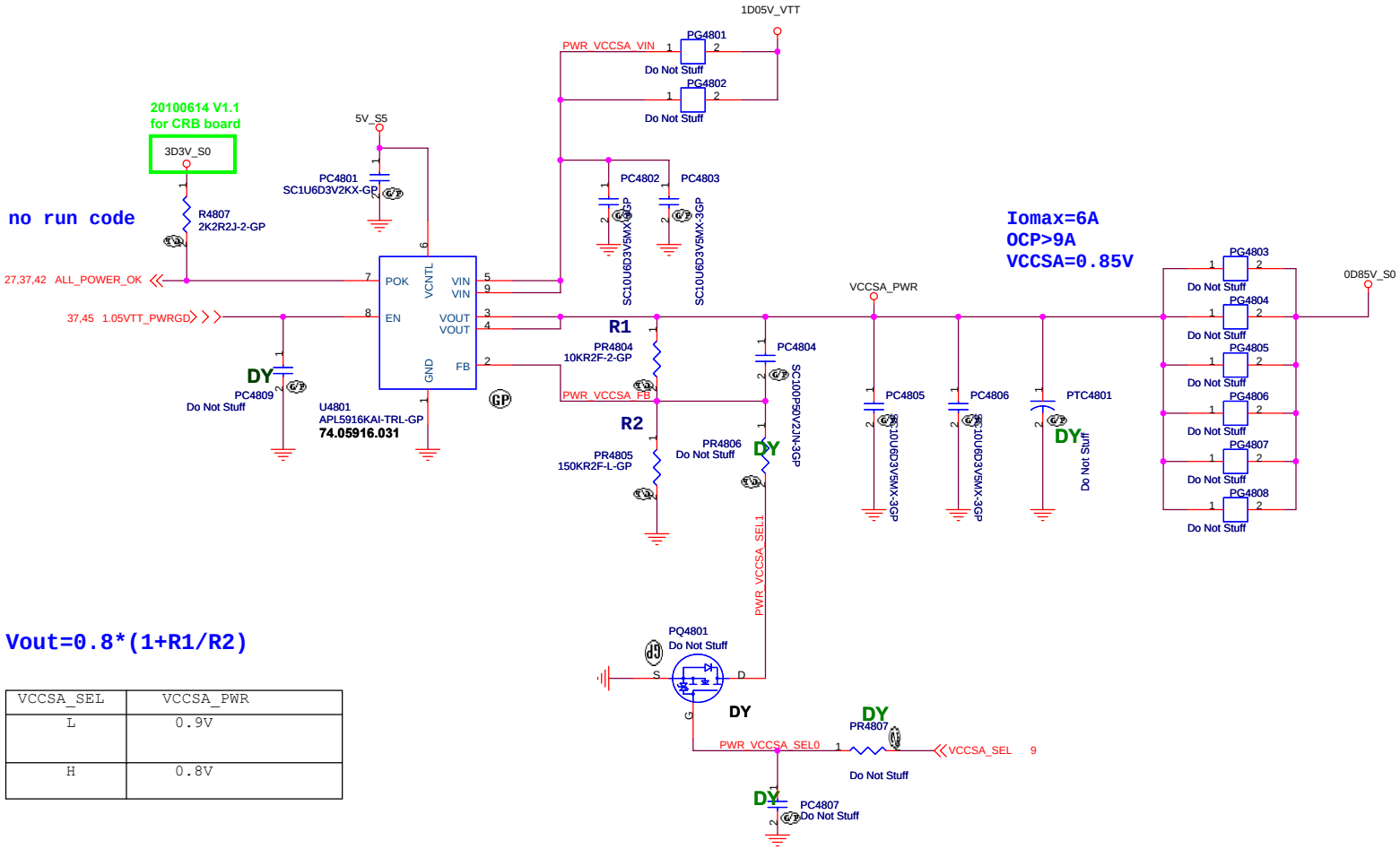
RT9025 for 1D8V_S0



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LDO_1D8V(RT9025)*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 47 of 102	

APL5916 for VCCSA



SB modify 2K2 for no run code

Iomax=6A
OCP>9A
VCCSA=0.85V

Vout=0.8*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

HR UMA

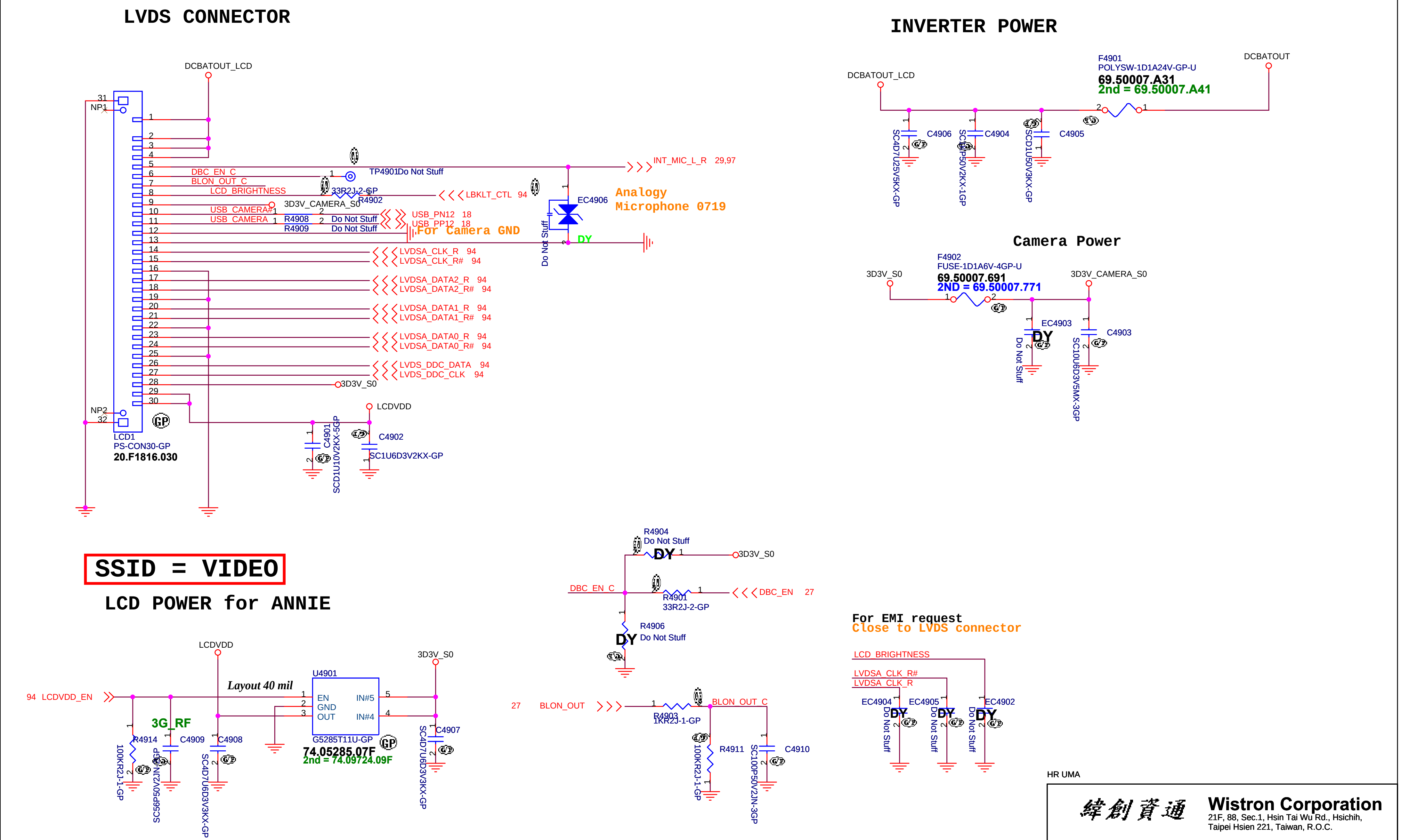
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LDO VCCSA(APL5916)***

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 48 of 102

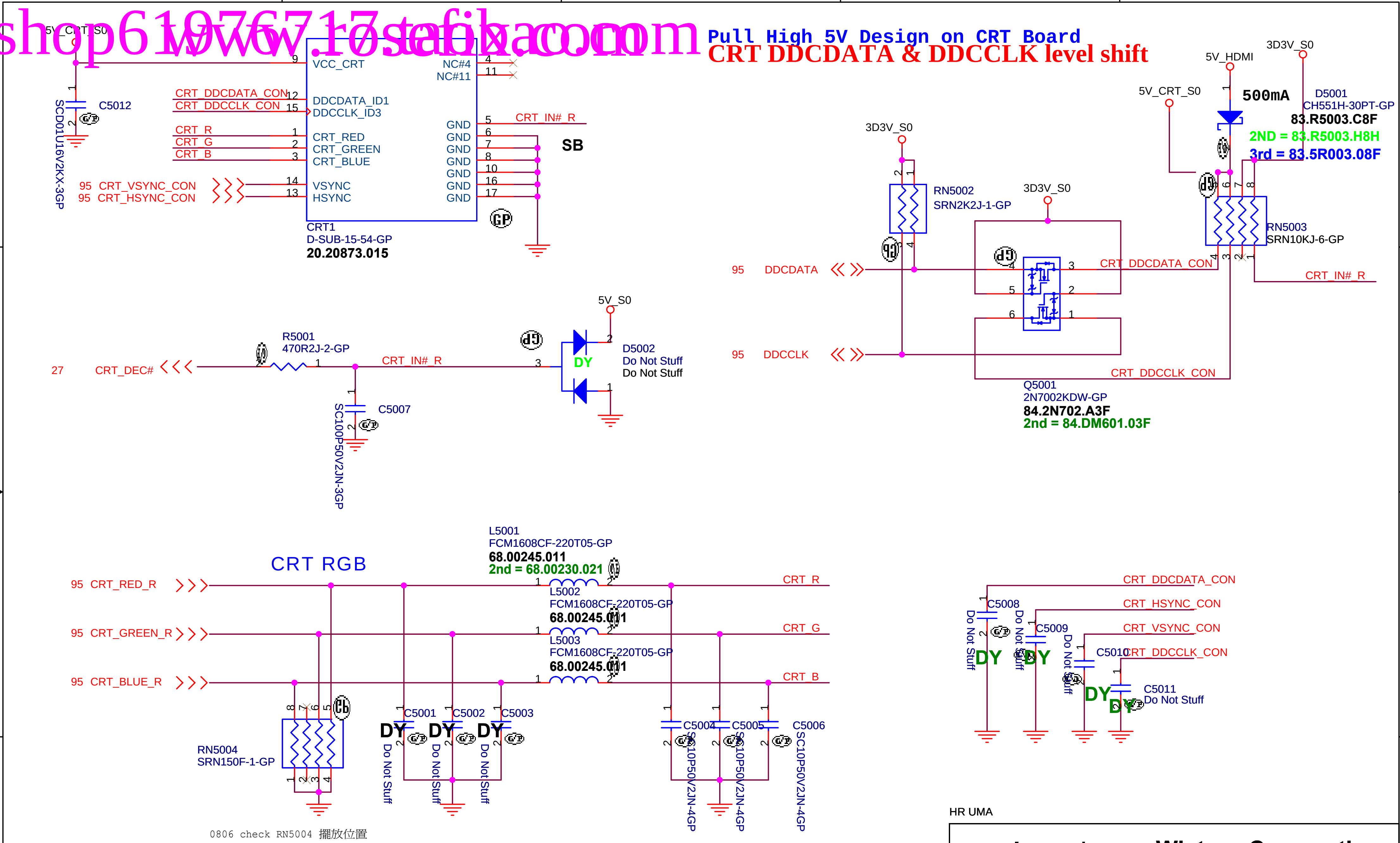
SSID = VIDEO


LVDS CONNECTOR
INVERTER POWER
DCBATOUT_LCD
DCBATOUT
F4901
POLYSW-1D1A24V-GP-U
69.50007.A31
2nd = 69.50007.A41
C4906
C4904
C4905
SC4D7U25V5KX-GP
SC1KP50V2KX-1GP
SCD1U50V3KX-GP
Camera Power
F4902
FUSE-1D1A6V-4GP-U
69.50007.691
2ND = 69.50007.771
3D3V_S0
3D3V_CAMERA_S0
EC4903
C4903
Do Not Stuff
SC10U6D3V5MX-3GP
DY
INT_MIC_L_R 29,97
TP4901 Do Not Stuff
DBC_EN_C
BLON_OUT_C
LCD_BRIGHTNESS
33R2J-2-GP
R4902
LBKLT_CTL 94
USB_CAMERA#
USB_CAMERA
R4908
R4909
Do Not Stuff
USB_PN12 18
USB_PP12 18
For Camera GND
EC4906
Analogy Microphone 0719
LVDSA_CLK_R 94
LVDSA_CLK_R# 94
LVDSA_DATA2_R 94
LVDSA_DATA2_R# 94
LVDSA_DATA1_R 94
LVDSA_DATA1_R# 94
LVDSA_DATA0_R 94
LVDSA_DATA0_R# 94
LVDS_DDC_DATA 94
LVDS_DDC_CLK 94
LCDVDD
C4901
C4902
SCD1U10V2KX-5GP
SC1U6D3V2KX-GP
LCD1
PS-CON30-GP
20.F1816.030
R4904
Do Not Stuff
R4901
33R2J-2-GP
DBC_EN 27
R4906
27 BLON_OUT
R4903
1KR2J-1-GP
R4911
C4910
100KR2J-1-GP
SC100P50V2JN-3GP
For EMI request
Close to LVDS connector
LVDSA_CLK_R#
LVDSA_CLK_R
EC4904
EC4905
EC4902
SSID = VIDEO
LCD POWER for ANNIE
94 LCDVDD_EN
Layout 40 mil
U4901
EN
GND
OUT
IN#5
IN#4
G5285T11U-GP
74.05285.07F
2nd = 74.09724.09F
3G_RF
R4914
C4909
C4908
C4907
100KR2J-1-GP
SC56P50V2JN-2GP
SC4D7U6D3V3KX-GP

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**LCD Connector**	
Size: Custom	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 49 of 102	


Pull High 5V Design on CRT Board
CRT DDCDATA & DDCCLK level shift
5V_CRT_S0
C5012
SCD01U16V2KX-3GP
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_R
CRT_G
CRT_B
95 CRT_VSYNC_CON
95 CRT_HSYNC_CON
VCC_CRT
NC#4
NC#11
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
GND
CRT_IN#_R
SB
CRT1
D-SUB-15-54-GP
20.20873.015
5V_HDMI
3D3V_S0
500mA
D5001
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
RN5002
SRN2K2J-1-GP
RN5003
SRN10KJ-6-GP
95 DDCDATA
95 DDCCLK
Q5001
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
5V_S0
R5001
470R2J-2-GP
27 CRT_DEC#
D5002
Do Not Stuff
Do Not Stuff
DY
C5007
SC100P50V2JN-3GP
CRT RGB
L5001
FCM1608CF-220T05-GP
68.00245.011
2nd = 68.00230.021
L5002
FCM1608CF-220T05-GP
68.00245.011
L5003
FCM1608CF-220T05-GP
68.00245.011
95 CRT_RED_R
95 CRT_GREEN_R
95 CRT_BLUE_R
RN5004
SRN150F-1-GP
C5001
C5002
C5003
C5004
C5005
C5006
SC10P50V2JN-4GP
C5008
C5009
C5010
C5011
CRT_HSYNC_CON
CRT_VSYNC_CON
0806 check RN5004 擺放位置

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

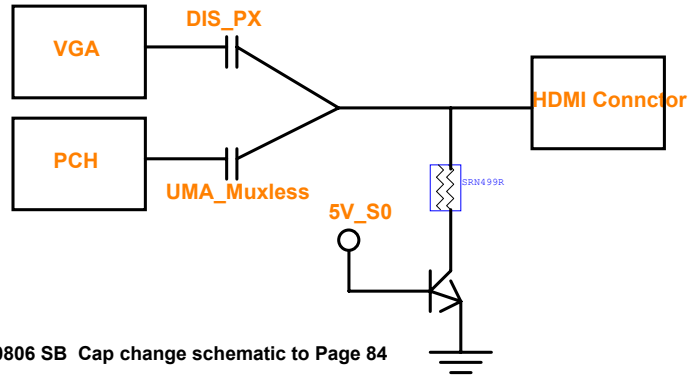
Title	*CRT Connector*	
Size A4	Document Number **JE40-HR**	Rev **-1**
Date: Thursday, December 02, 2010	Sheet 50 of 102	

SSID = VIDEO

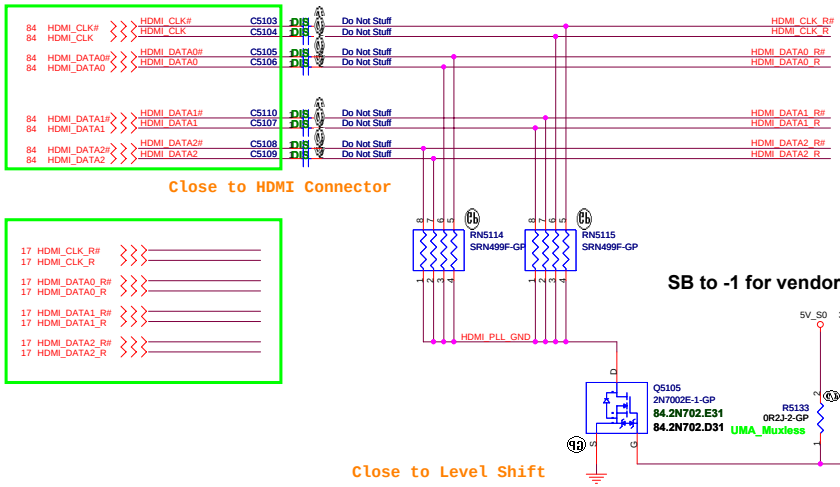
HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister

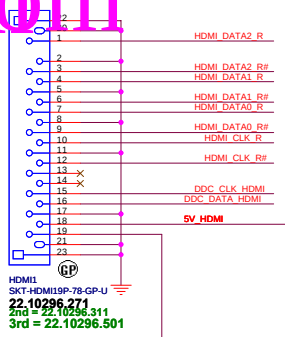
HDMI DISCRETE/ UMA Co-lay

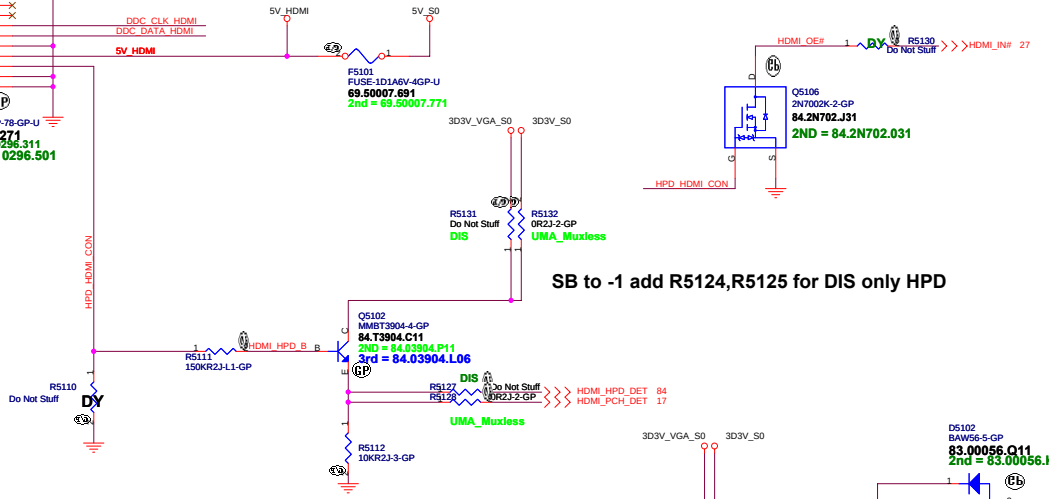


0806 SB Cap change schematic to Page 84



HDMI CONN





HR UMA

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	HDMI Level Shifter/Connector
Size: Custom	Document Number: JE40-HR
Rev	-1
Date: Thursday, December 02, 2010	Sheet 51 of 102

LED BACKLIGHT CONVERTER POWER

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 52 of 102

(Blanking)

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *S-VIDEO*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 53 of 102	

(Blanking)

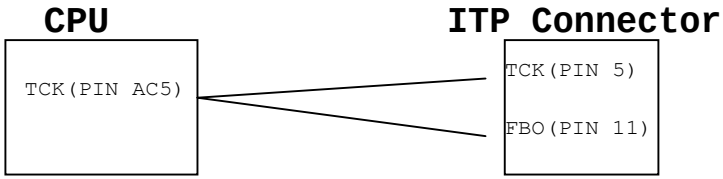
HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 54 of 102	

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



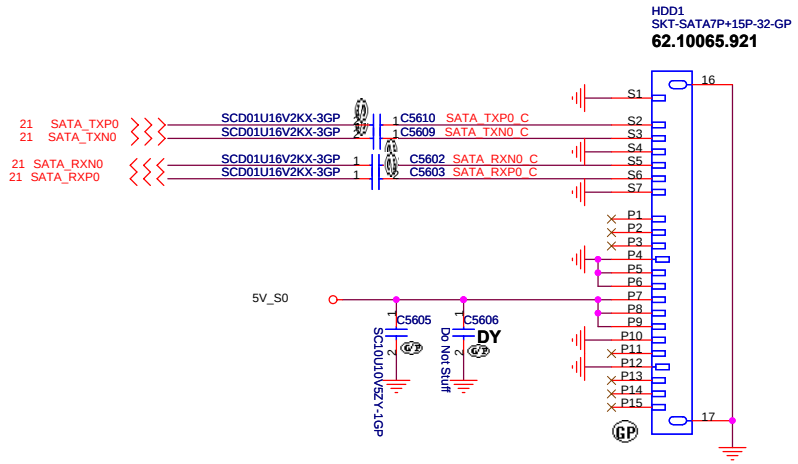
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

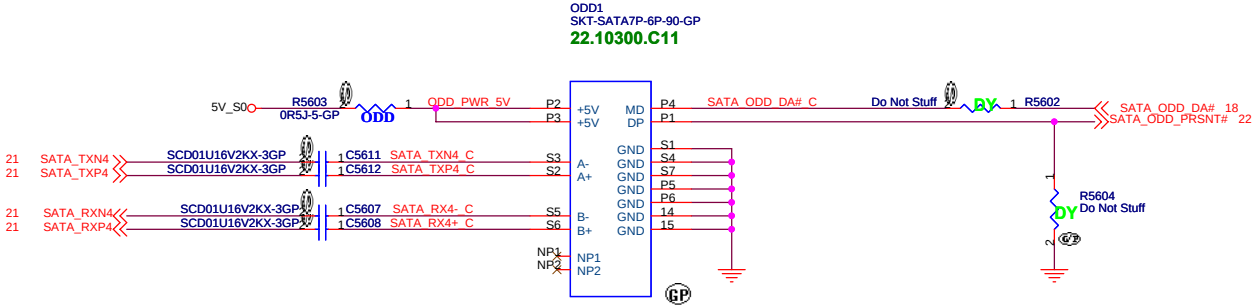
Title: ITP		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 55 of 102	

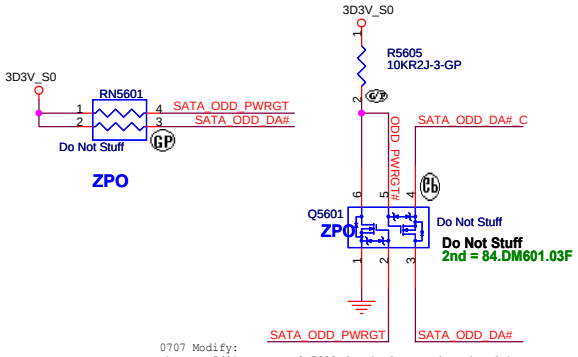
SSID = SATA

SATA HDD Connection



ODD Connector



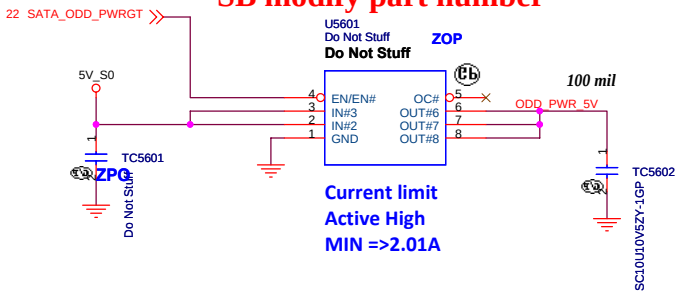


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD/ODD		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 56 of 102	

ESATA Power

USB CHARGER

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: E-SATA/USB CHARGER

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 57 of 102

SSID = AUDIO

Speaker Connector

LINE1 OUT
SPDIF

JE40 Modify LINE OUT

Audio at small board

MIC IN

Internal
Microphone

JE40 delete Line in function

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

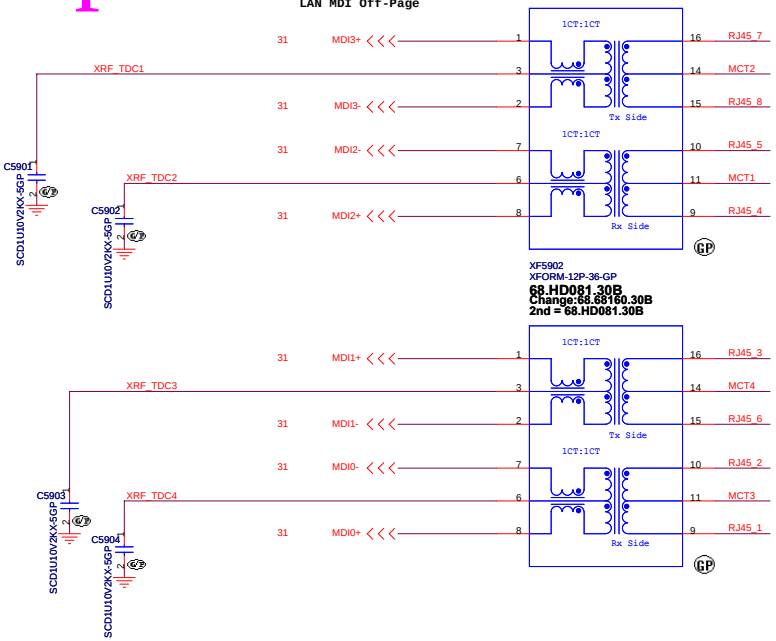
Title: ***Audio Jack***

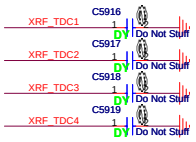
Size	Document Number	Rev
A3	JE40-HR	-1

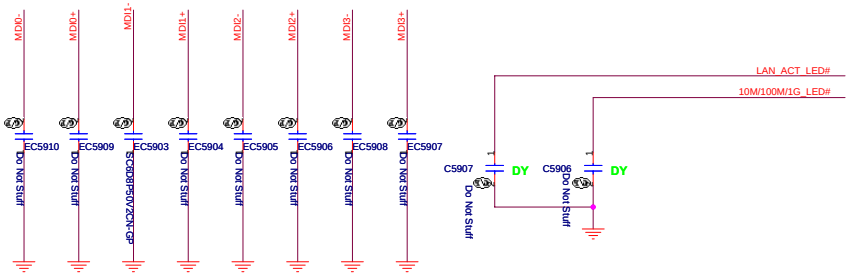
Date: Thursday, December 02, 2010 Sheet 58 of 102

SSID = LOM

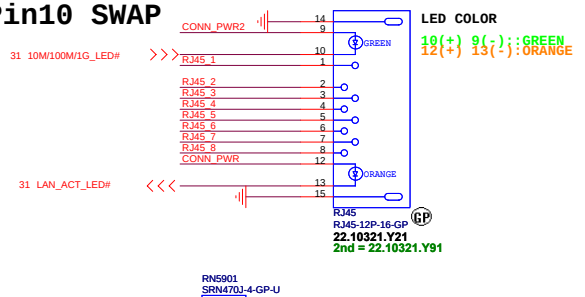
LAN MDI Off-Page

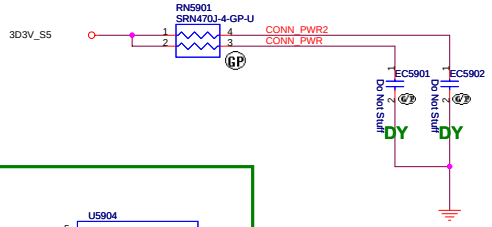




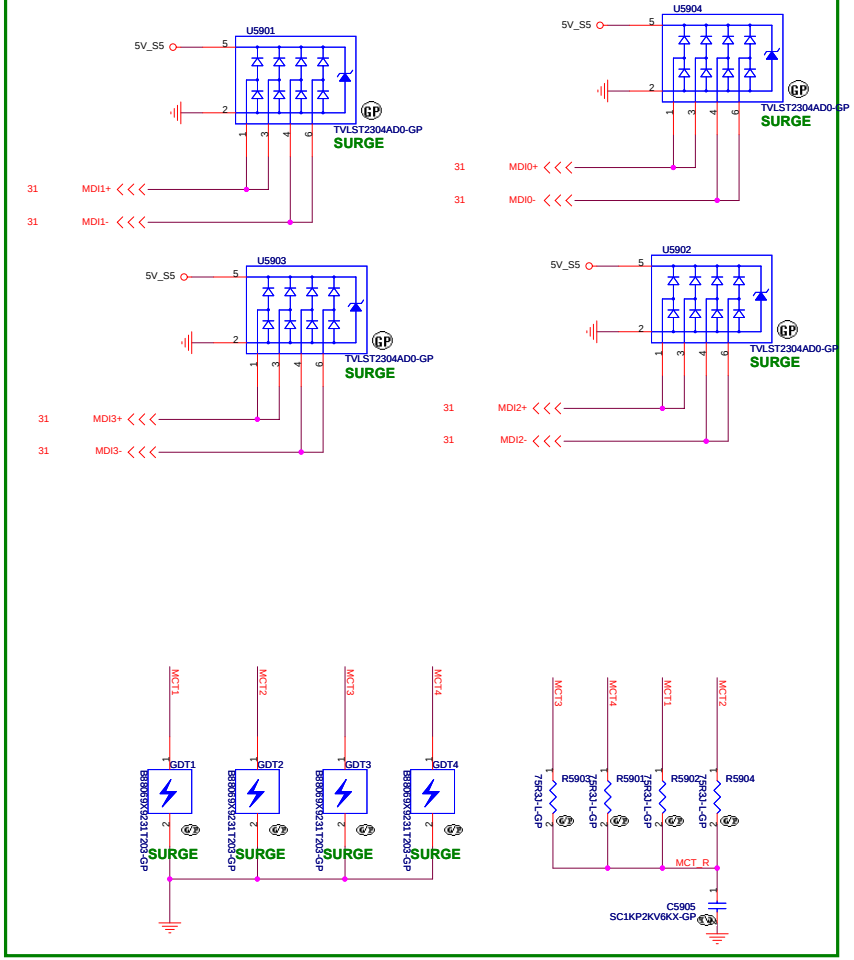


SB modiyf Pin9 Pin10 SWAP





SB modify For EMI



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

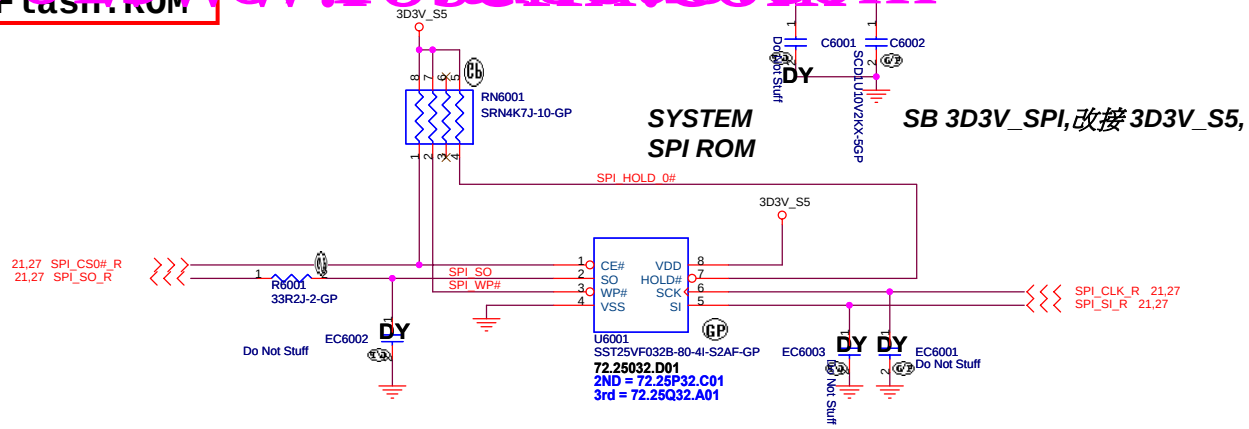
Title: LAN CONNECTOR

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 59 of 102

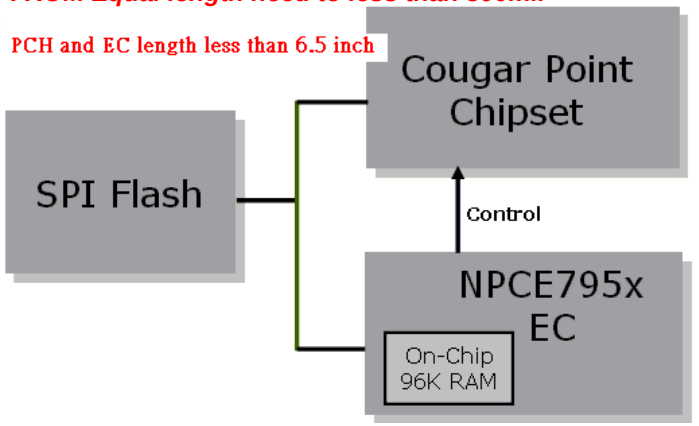
SPI FLASH ROM (4M byte) for PCH

SSID = Flash.ROM

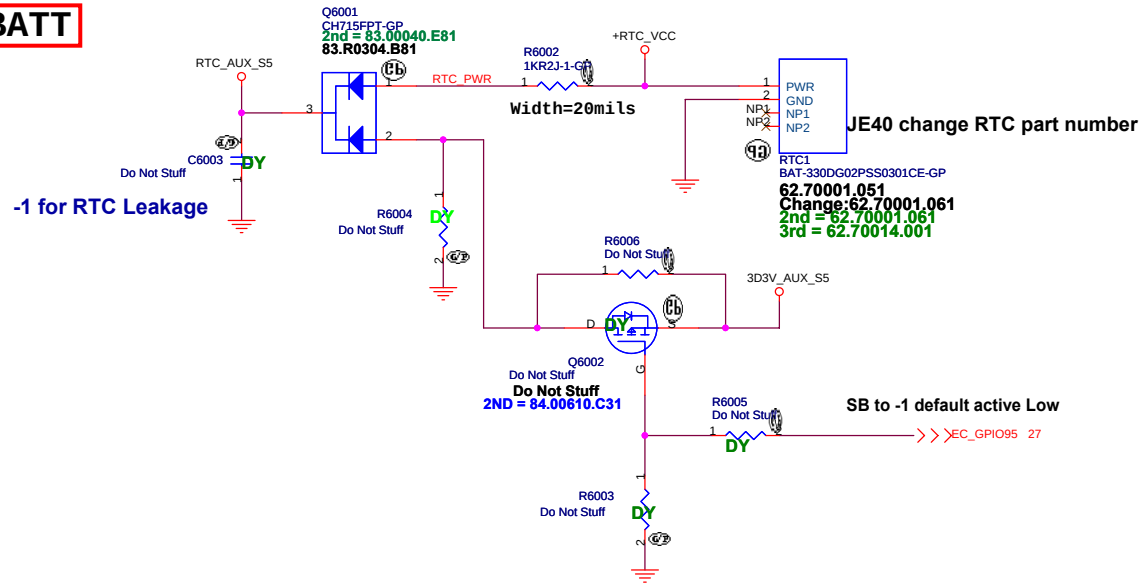


SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch



SSID = RBATT



HR UMA

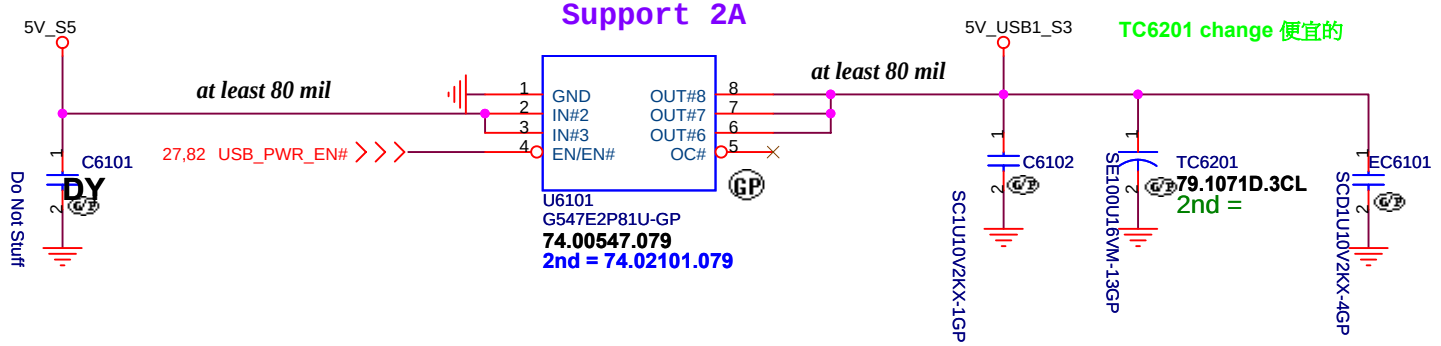
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

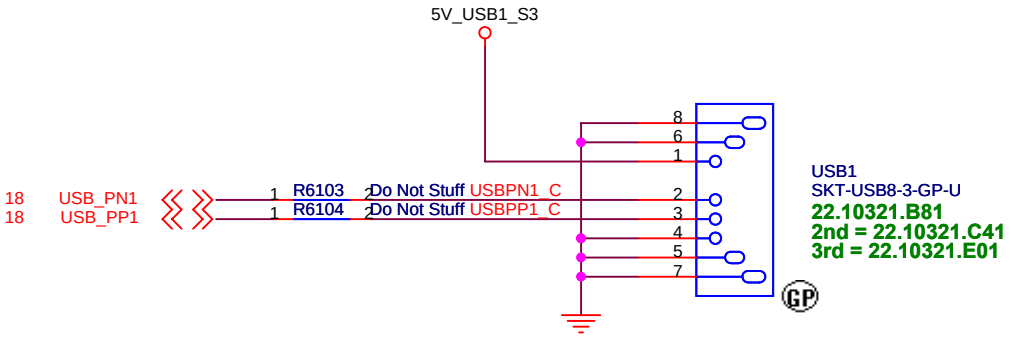
Title	Flash/RTC	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 60 of 102	

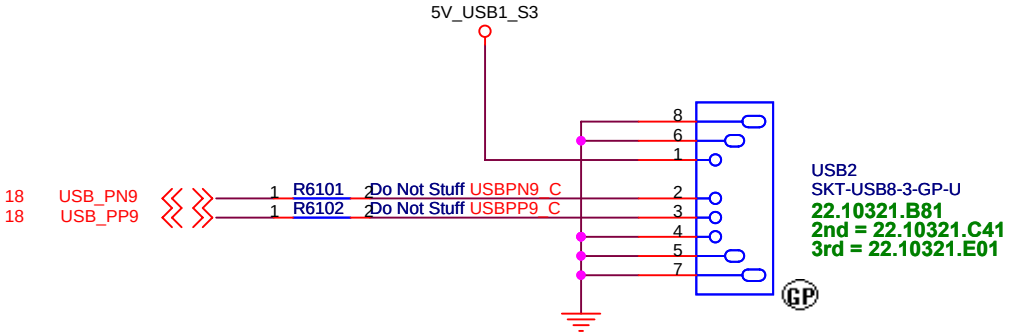
SSID = USB

IO Board USB Power

Change Main source
Support 2A







HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

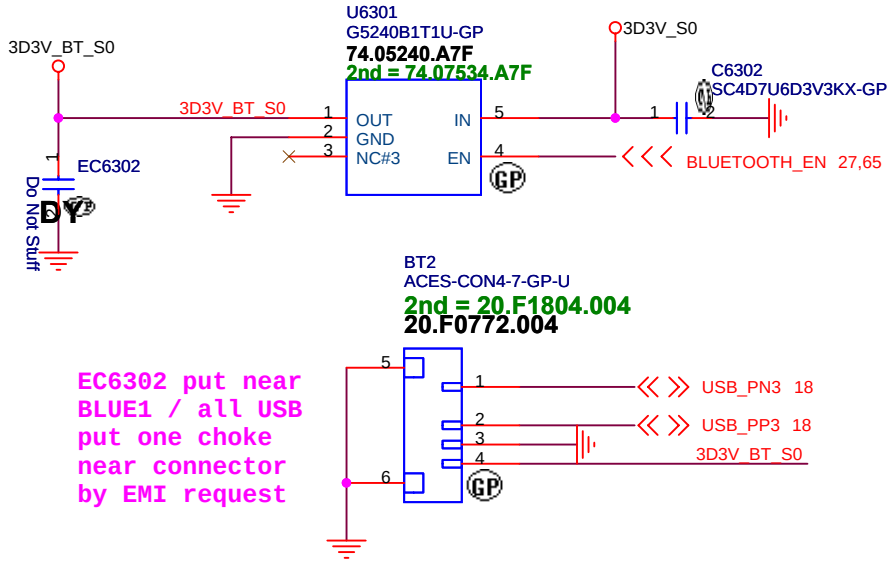
Title: ***USB 3.0 Port***

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 62 of 102

SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module

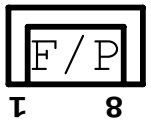


HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Bluetooth*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 63 of 102	

Finger printer

JE40 delete FP function



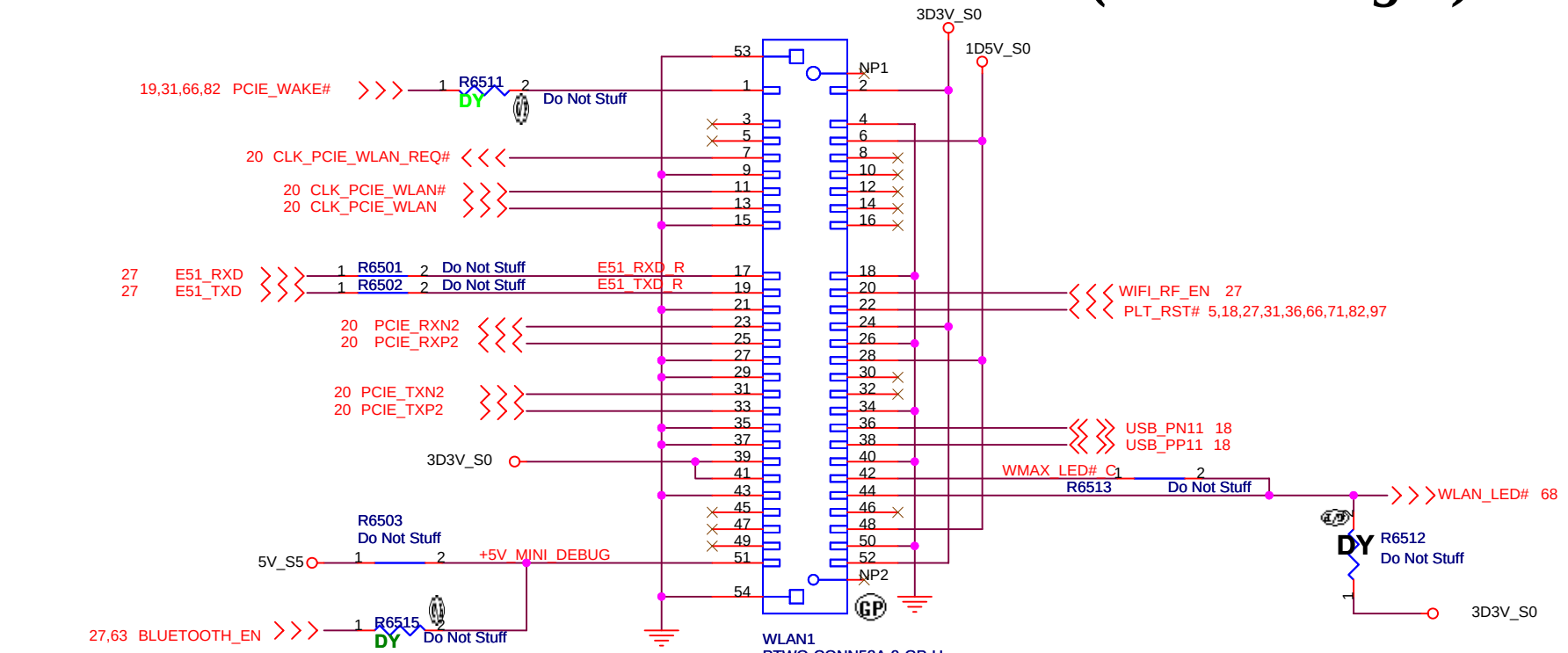
HR UMA

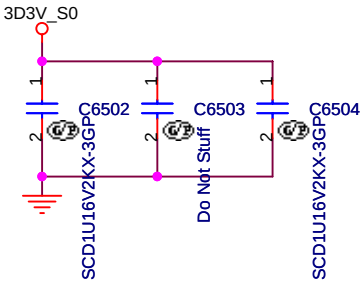
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 64 of 102	

SSID = Wireless

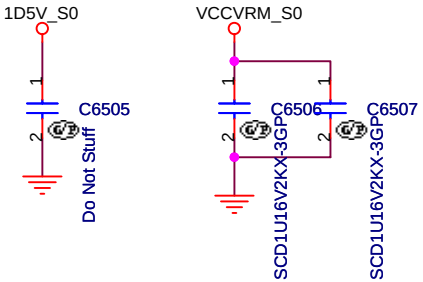
Mini Card Connector(802.11a/b/g/n)

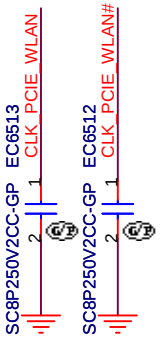




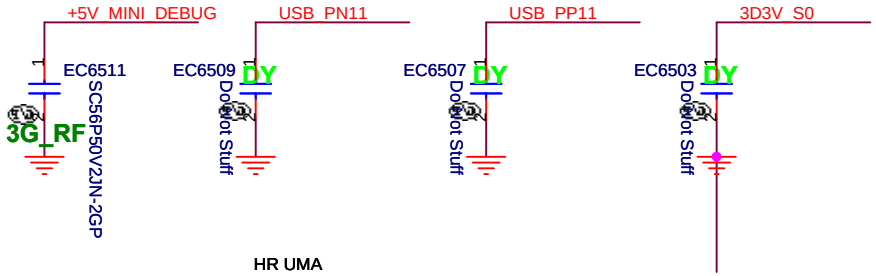
SB modify for SIV

-2





RF suggestion



HR UMA

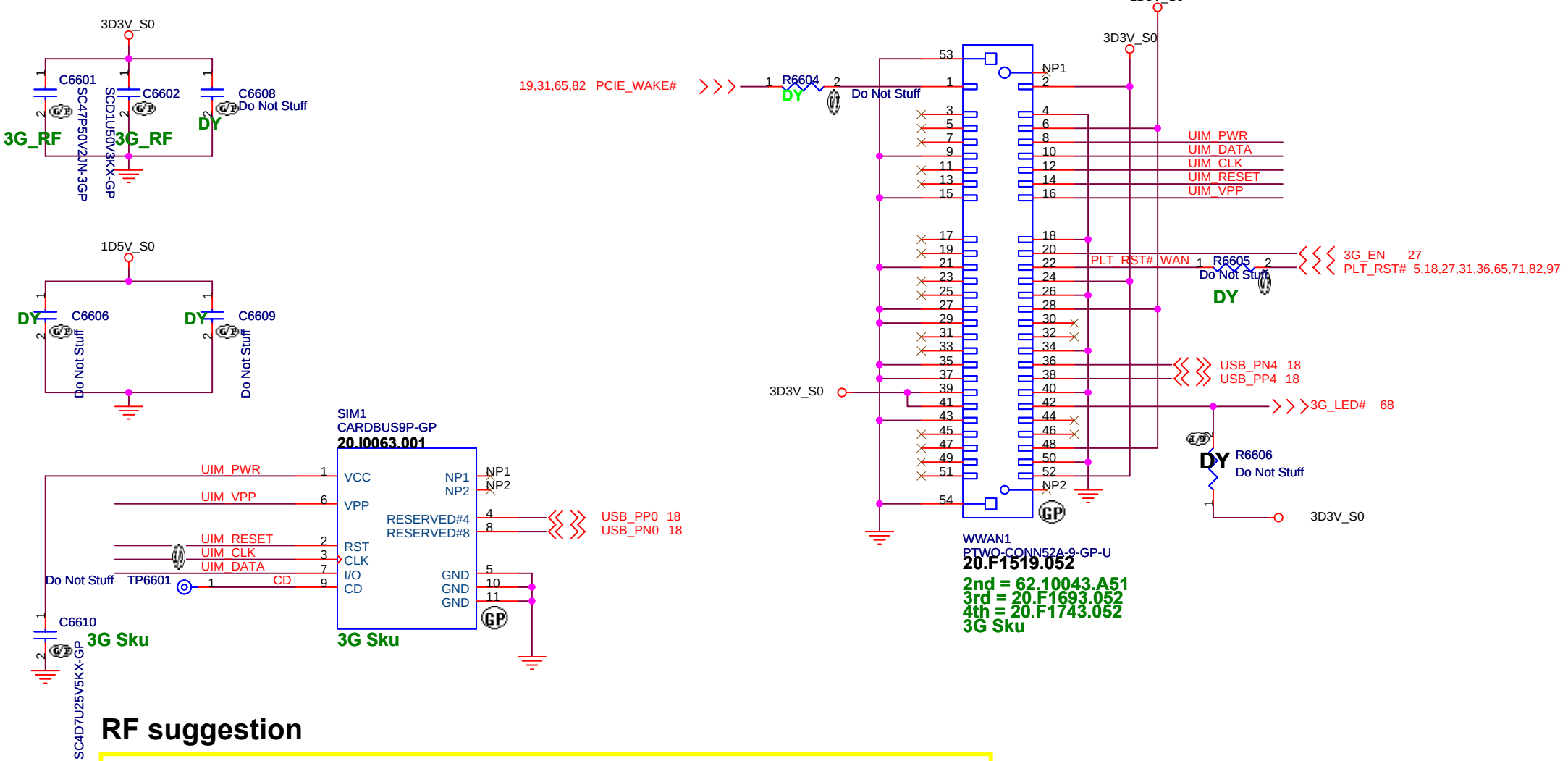
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINICARD(WLAN)/ITP CONN		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 65 of 102	

SSID = Wireless

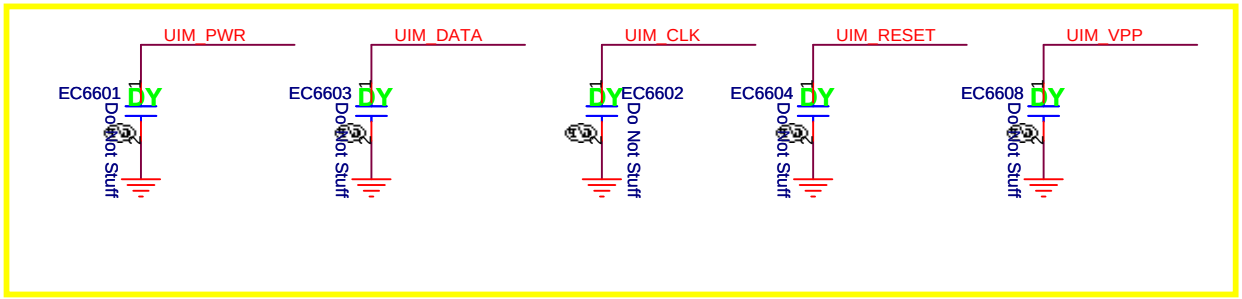
Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN



RF suggestion



HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size	Document Number	Rev
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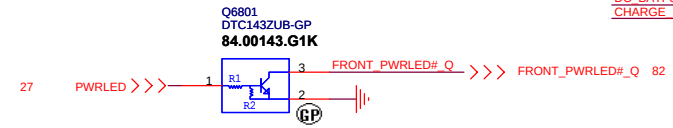
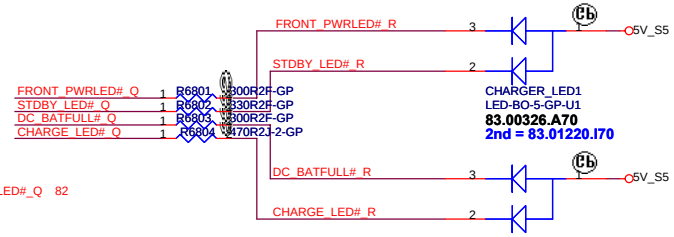
HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 67 of 102	

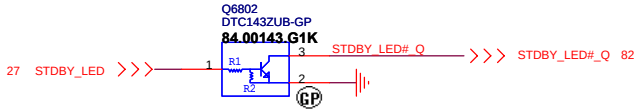
SSID = User_Interface

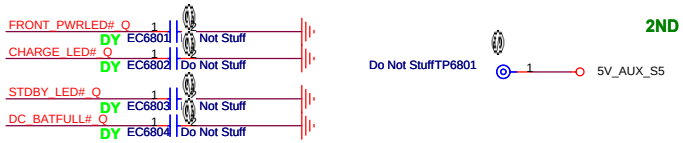
Power button LED



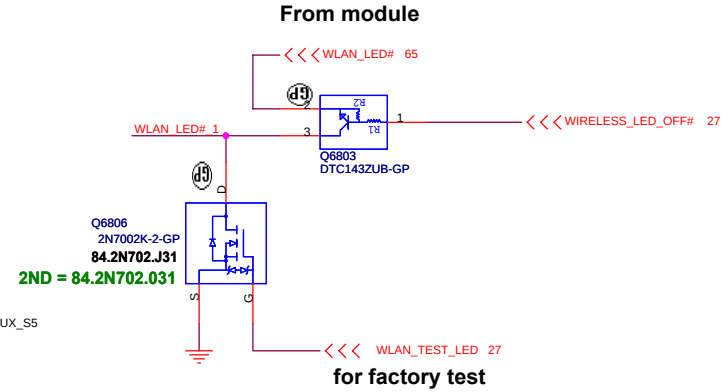


Power STDBY_LED

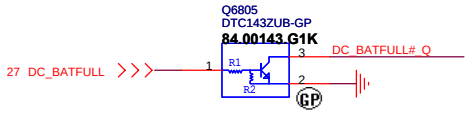




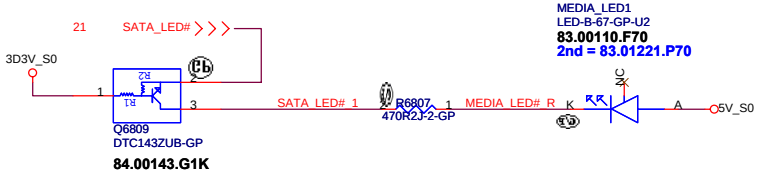
WLAN_LED



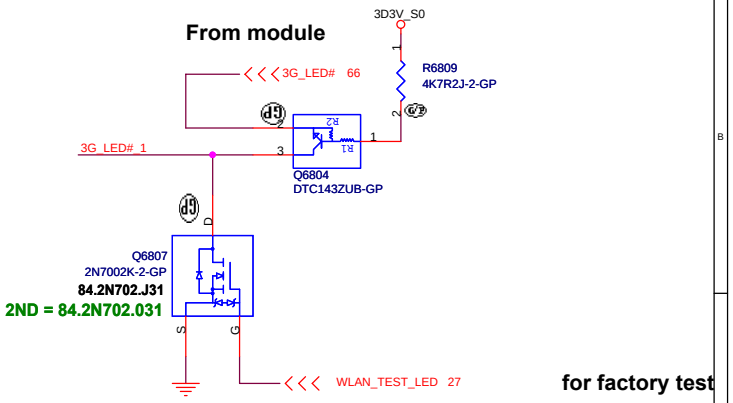
Battery LED2(DC_BATFULL)



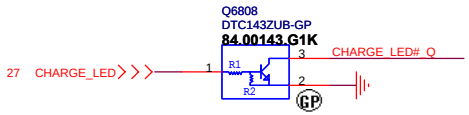
SATA HDD LED

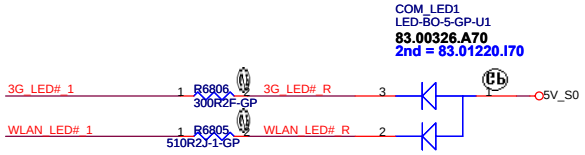


3G LED



Battery LED1(CHARGE)





HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LED Bard/Power Button	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 68 of 102	

SSID = KBC

Internal KeyBoard Connector

20.K0320.026
2nd = 20.K0382.026
KB1
ACES-CON26-6GP-U

27 TPCLK
27 TPDATA

KCOL0 KCOL1 KCOL2 KCOL3 KCOL4 KCOL5 KCOL6 KCOL7 KCOL8 KCOL9 KCOL10 KCOL11 KCOL12 KCOL13 KCOL14 KCOL15 KCOL16 KCOL17

KROW0 KROW1 KROW2 KROW3 KROW4 KROW5 KROW6 KROW7

KROW[0..7] 27
KCOL[0..16] 27
KCOL17 27

MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1

SB to -1 modify Part number

TOUCH PAD

5V_S0

RN6901
SRN4K7J-8-GP

EC6902
SC56P50V2JN-2GP
3G_RF

EC6902
SC56P50V2JN-2GP
3G_RF

RN6902
SRN33J-5-GP-U

TP_CLK
TP_DATA

TPAD1
ACES-CON6-13-GP
20.K0320.006
2nd = 20.K0382.006

TP_LEFT
TP_RIGHT

TP_DATA
TP_CLK
TP_LEFT
TP_RIGHT

EC6903 EC6904 EC6905 EC6906
DDY
Do Not Stuff

FFC 異面

SW_R1
SW-TACT-5P-9-GP
62.40089.141
Change:62.40089.221

TP_RIGHT

SW_L1
SW-TACT-5P-9-GP
62.40089.141
Change:62.40089.221

TP_LEFT

HR UMA

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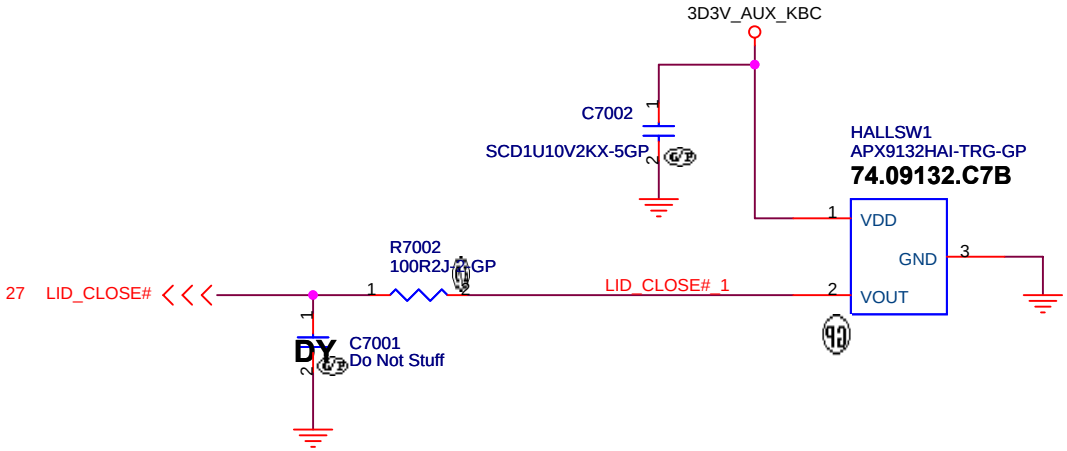
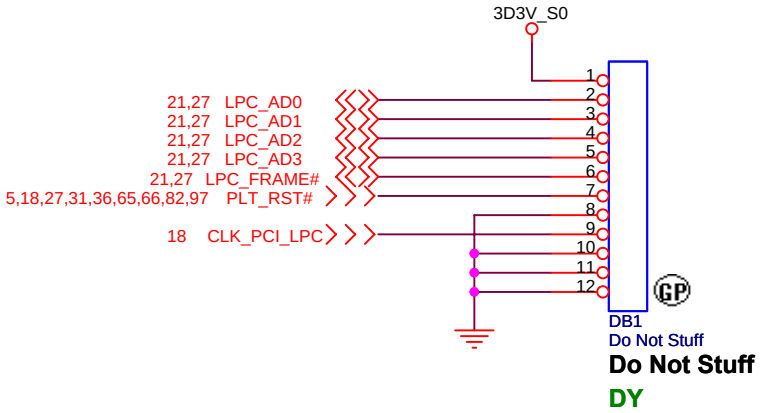
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Key Board/Touch Pad	
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010	Sheet 69 of 102	



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Hall Sensor*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 70 of 102	



HR UMA

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Title: ***Dubug connector***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 71 of 102

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Title: *Reserved*

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 72 of 102

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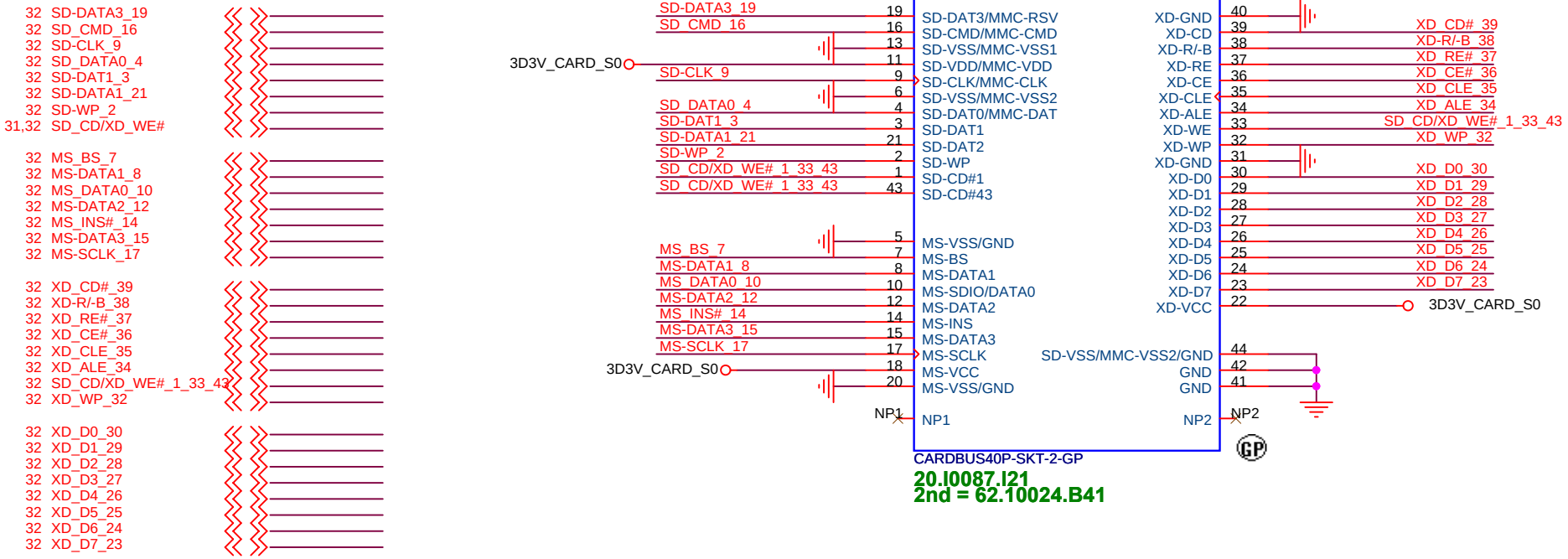
Title: *Reserved*

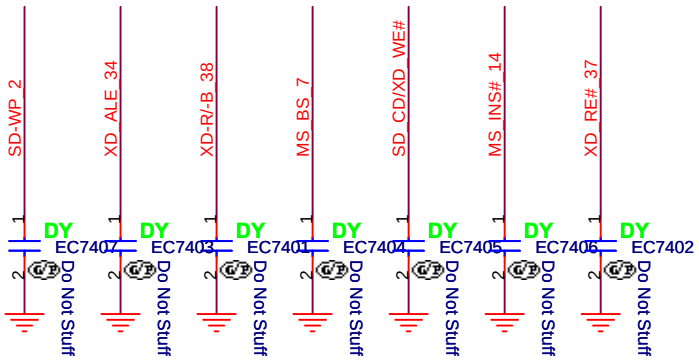
Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 73 of 102

SD/XD/MS Card Reader

SSID = SDIO





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Title: **CARD Reader CONN**

Size	Document Number	Rev
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Date: Thursday, December 02, 2010 Sheet 74 of 102

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

HR UMA

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Title: New Card

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 75 of 102

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Title: *Reserved*

Size	Document Number	Rev
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Title: ***Reserved***

Size	Document Number	Rev
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Title: ***Reserved***

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SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

JE40 delete G Sensor Function

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

HR UMA

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Title: *Free Fall Sensor*

Size	Document Number	Rev
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Date: Thursday, December 02, 2010

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Title: *Reserved*

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HR UMA

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Title: ***Reserved***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
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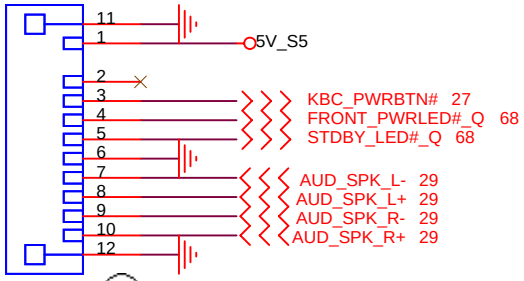
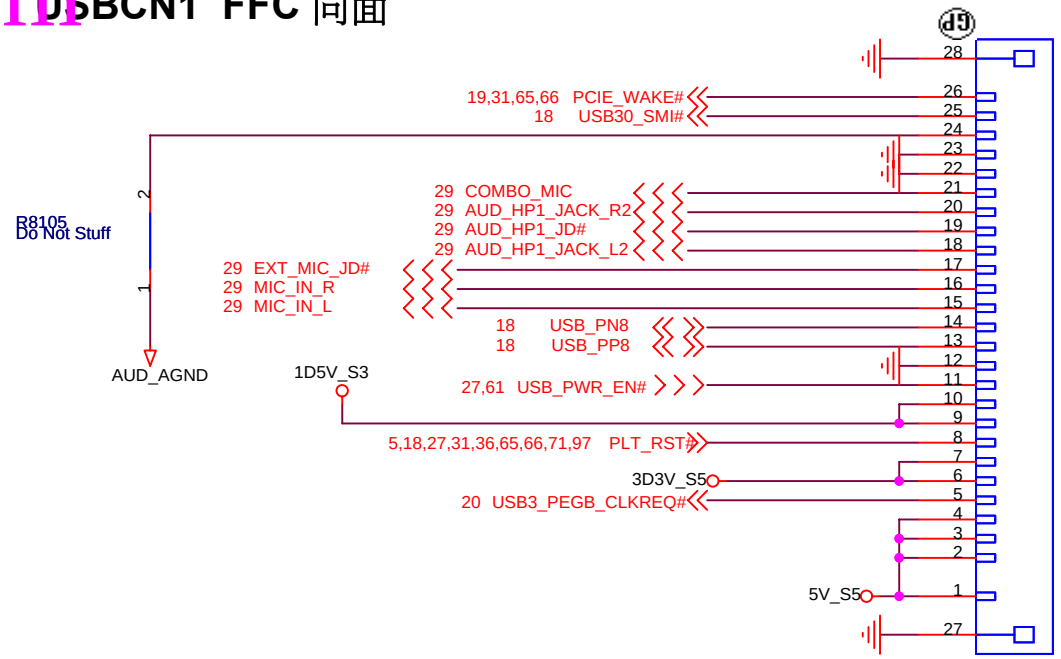
PWRCN1 FFC 異面



PWRCN1
ACES-CON10-20-GP
20.K0422.010
2nd = 20.K0382.010

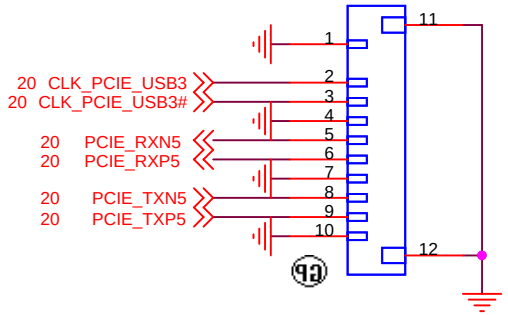
USBCN1 FFC 同面



USBCN1
ACES-CON26-11-GP
20.K0315.026
2nd = 20.K0370.026

0806 change 10Pin

USBCN2
ACES-CON10-18-GP
20.K0315.010
2nd = 20.K0392.010

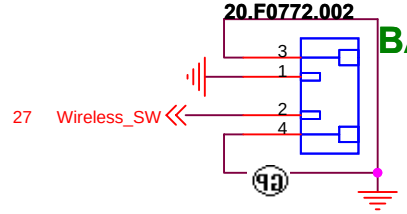


USBCN2 FFC 同面

-1 add RF connector
BAE40 Only

RF_CN1
ACES-CON2-11-GP
20.F0772.002

BAE40



Cabele Wire to BD

HR UMA

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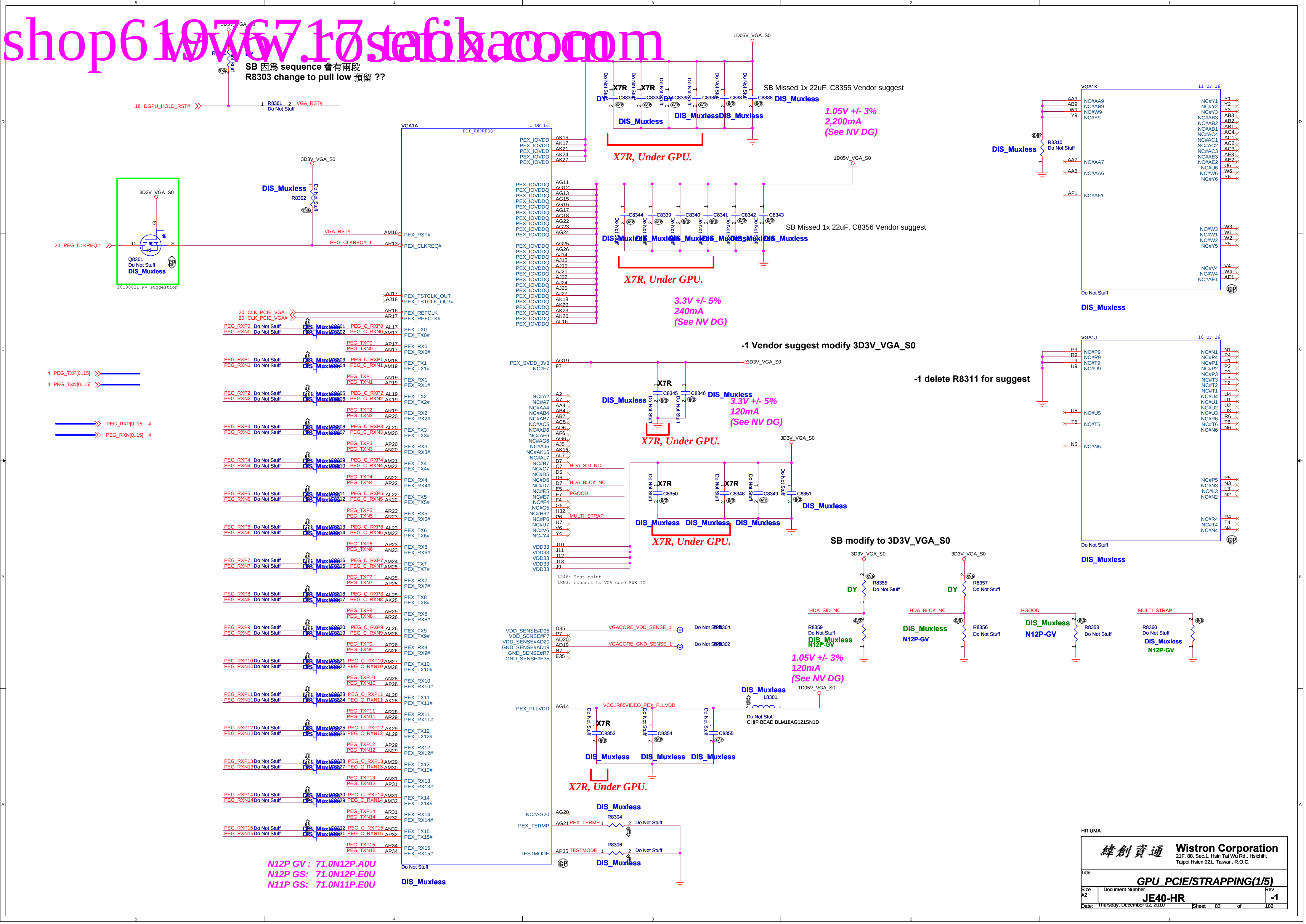
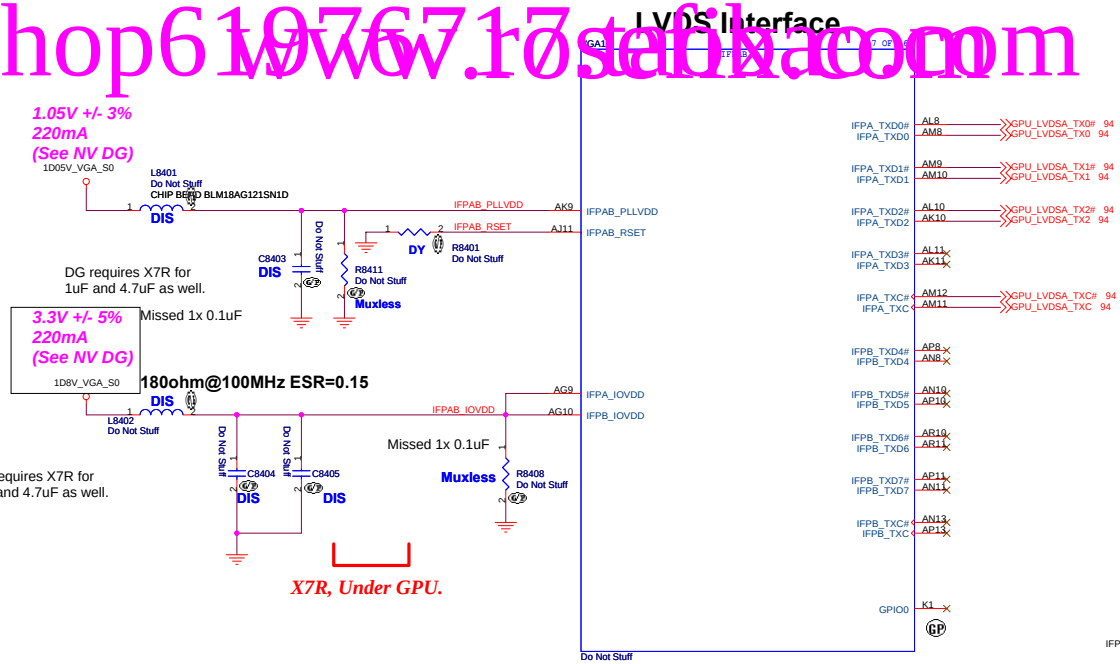
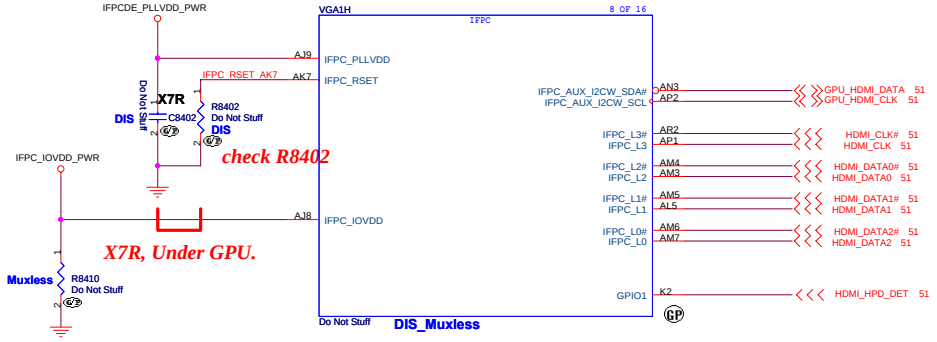
Title: *IO Board Connector*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 82 of 102	

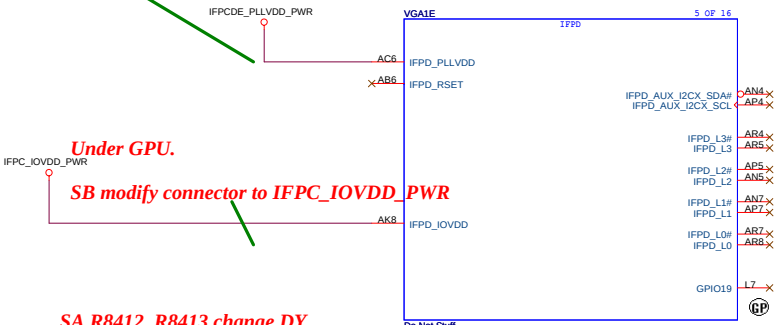

SB 因爲 sequence 會有兩段
R8303 change to pull low 預留 ??
18 DGPU_HOLD_RST#
R8361 Do Not Stuff
VGA_RST#
1D05V_VGA_S0
SB Missed 1x 22uF. C8355 Vendor suggest
DIS_Muxless
1.05V +/- 3%
2,200mA
(See NV DG)
X7R, Under GPU.
VGA1A
PCI_EXPRESS
1 OF 16
3D3V_VGA_S0
R8302
Do Not Stuff
Q8301
Do Not Stuff
DIS_Muxless
20100621 NV suggestion
20 PEG_CLKREQ#
PEX_RST#
PEX_CLKREQ#
PEX_IOVDD
PEX_IOVDDQ
SB Missed 1x 22uF. C8356 Vendor suggest
3.3V +/- 5%
240mA
(See NV DG)
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
20 CLK_PCIE_VGA
20 CLK_PCIE_VGA#
PEX_REFCLK
PEX_REFCLK#
4 PEG_TXP[0..15]
4 PEG_TXN[0..15]
PEG_RXP[0..15] 4
PEG_RXN[0..15] 4
-1 Vendor suggest modify 3D3V_VGA_S0
-1 delete R8311 for suggest
PEX_SVDD_3V3
3.3V +/- 5%
120mA
(See NV DG)
HDA_SID_NC
HDA_BLCK_NC
PGOOD
MULTI_STRAP
VDD33
LA46: Test point
LRN3: connect to VGA core PWR IC
SB modify to 3D3V_VGA_S0
R8355 Do Not Stuff
R8357 Do Not Stuff
R8359 Do Not Stuff
R8356 Do Not Stuff
R8358 Do Not Stuff
R8360 Do Not Stuff
N12P-GV
VGACORE_VDD_SENSE_1
VGACORE_GND_SENSE_1
Do Not Stuff
1.05V +/- 3%
120mA
(See NV DG)
PEX_PLLVDD
VCC1R05VIDEO_PEX_PLLVDD
L8301
Do Not Stuff
CHIP BEAD BLM18AG121SN1D
PEX_TERMP
R8304
R8306
TESTMODE
N12P GV : 71.0N12P.A0U
N12P GS: 71.0N12P.E0U
N11P GS: 71.0N11P.E0U
VGA1K
11 OF 16
R8310 Do Not Stuff
VGA1J
10 OF 16
HR UMA
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU_PCIE/STRAPPING(1/5)
Size A2
Document Number
JE40-HR
Rev -1
Date: Thursday, December 02, 2010
Sheet 83 of 102

LVDS Interface





SB modify connector to IFPCDE_PLLVDD_PWR



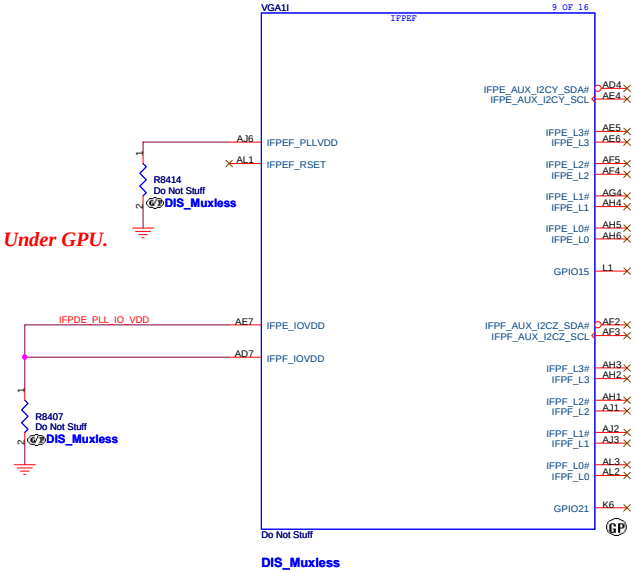
Under GPU.

IFPC_IOVDD_PWR

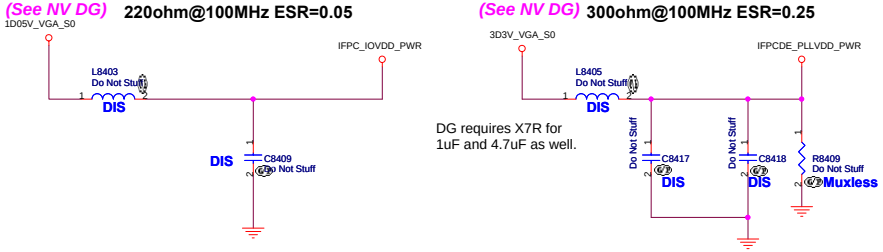
SB modify connector to IFPC_IOVDD_PWR

SA R8412, R8413 change DY

SB R8412, R8413 change delete

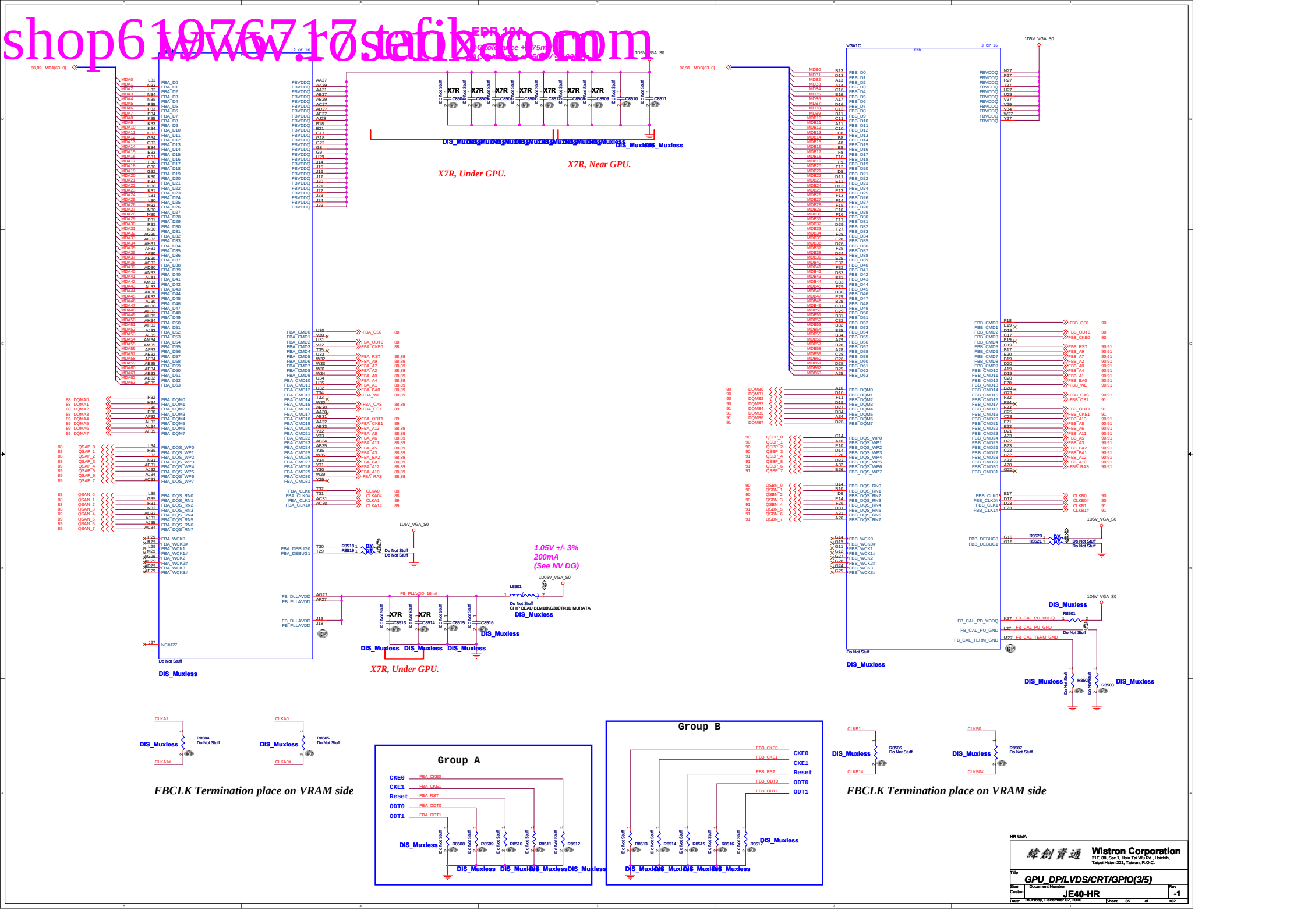


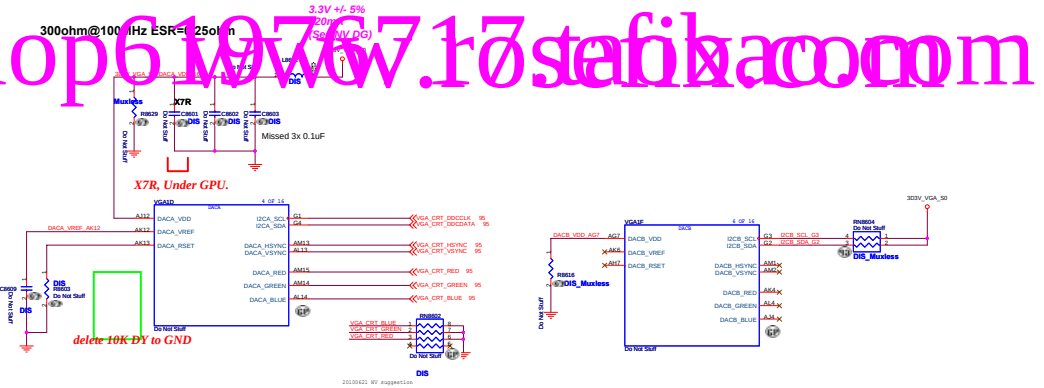
HDMI Interface

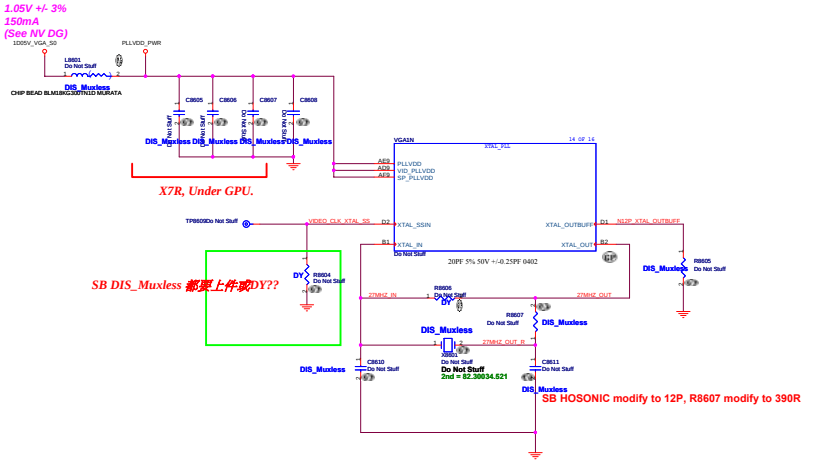


HR UMA

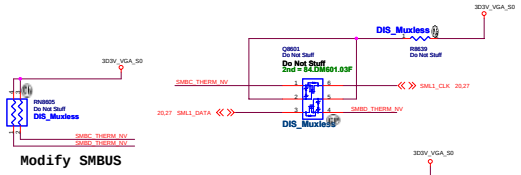
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU Memory(2/5)		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 84 of 102	

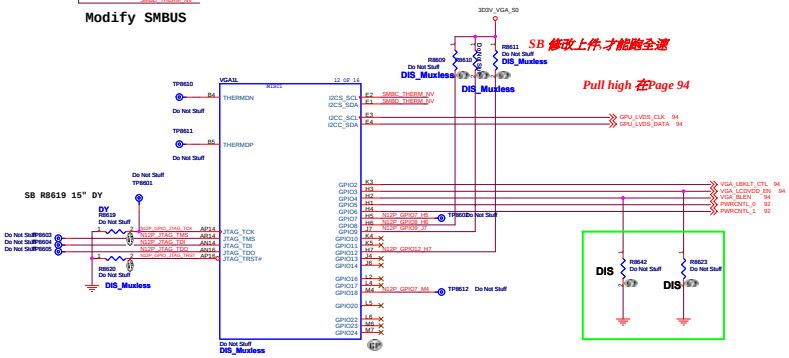




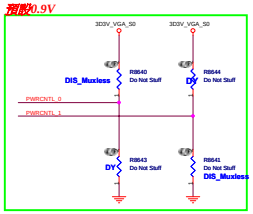


VGA Thermal sensor P2800



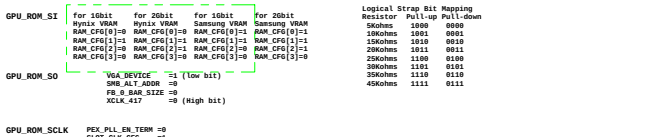


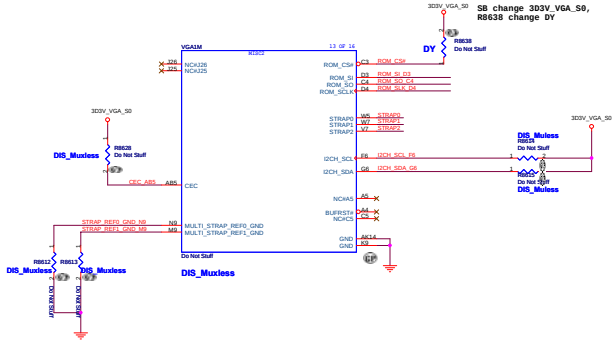
SJM50-CP SUPPORT							
P-STATE	NVVDD_ALT_V1	NVVDD_ALT_V0	N11M-GE1	N11M-GE2	N11M-GP1	N11P-GE1	N12P-GE Fermi
P12	0	0	0.85V	0.85V	0.85V	0.80V	0.85V
P8	0	1	0.85V	0.85V	0.85V	0.85V	0.9V
P0	1	0	1.03V	1.03V	1.03V	0.95V	0.95V

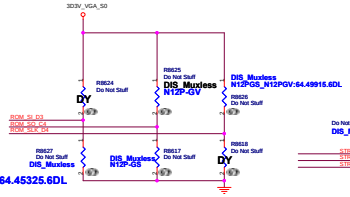


NVIDIA TABLE

	Hynix 2G 0110 128*16*8 800MHZ	Hynix 1G 0000 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL







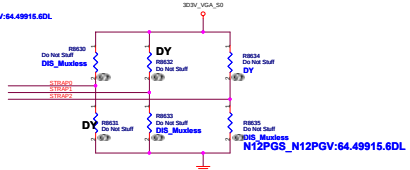


TABLE NVIDIA

71.0N12P.E0U

-1 modify N12P GV setting
71.0N12P.A0U

	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x1050	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2 PU	25Kohm 64.24925.6DL	45Kohm ES 45K QS 5K 64.49915.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

STRAP0 USER[0]=1 USER[1]=1 USER[2]=1 USER[3]=1 — N12P-GS — N12P-GV — N11P-GE Pull Low — N11P-GS Pull Low — N12P-GE

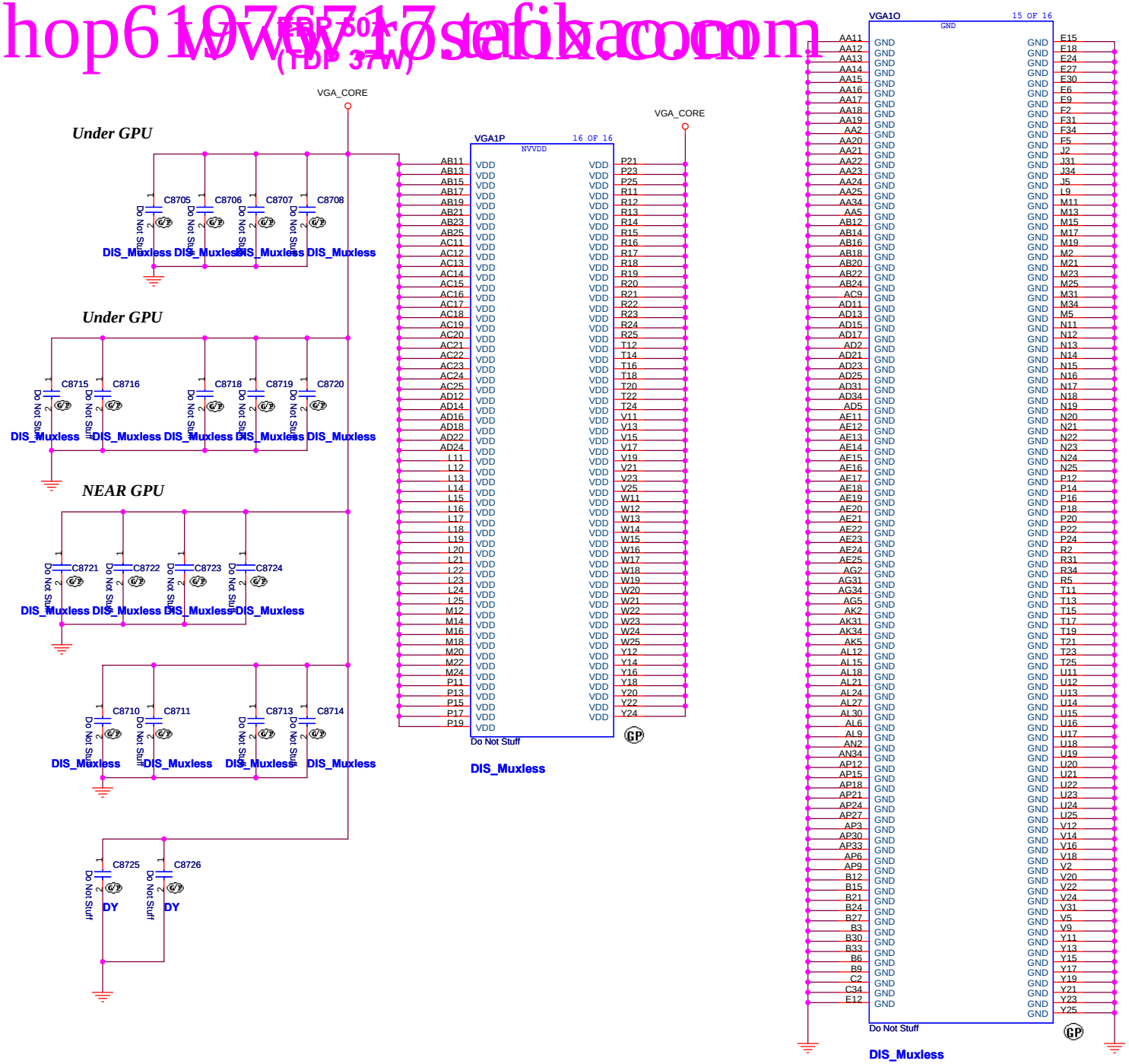
USE 1111 (45K)

STRAP1 3GIO_PADCFG[0]=1 3GIO_PADCFG[1]=1 3GIO_PADCFG[2]=1 3GIO_PADCFG[3]=1 — 0 1 1 0

USE 0110 (35K)

STRAP2
PCI_DEVID[0]=1 N12P-GS GF108-730-A1 0x0DF4 (0X4) (0100)
PCI_DEVID[1]=0 N12P-GV1 GF108-705-A1 0x0DF7 (0X7) (0111)
PCI_DEVID[2]=0 N11P-GS Fermi 0x0DF0 (0000)
PCI_DEVID[3]=0 N11P-GE Fermi 0x0DF1 (0001)

Wistron Corporation	GPU_POWER(4/5)			
8F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	Size: A1	Document Number: JE40-HR	Rev: -1	
	Date: Thursday, December 02, 2010	Sheet: 85 of 102		



HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU DPPWR/GND(5/5)

Size	Document Number	Rev
A3	JE40-HR	-1

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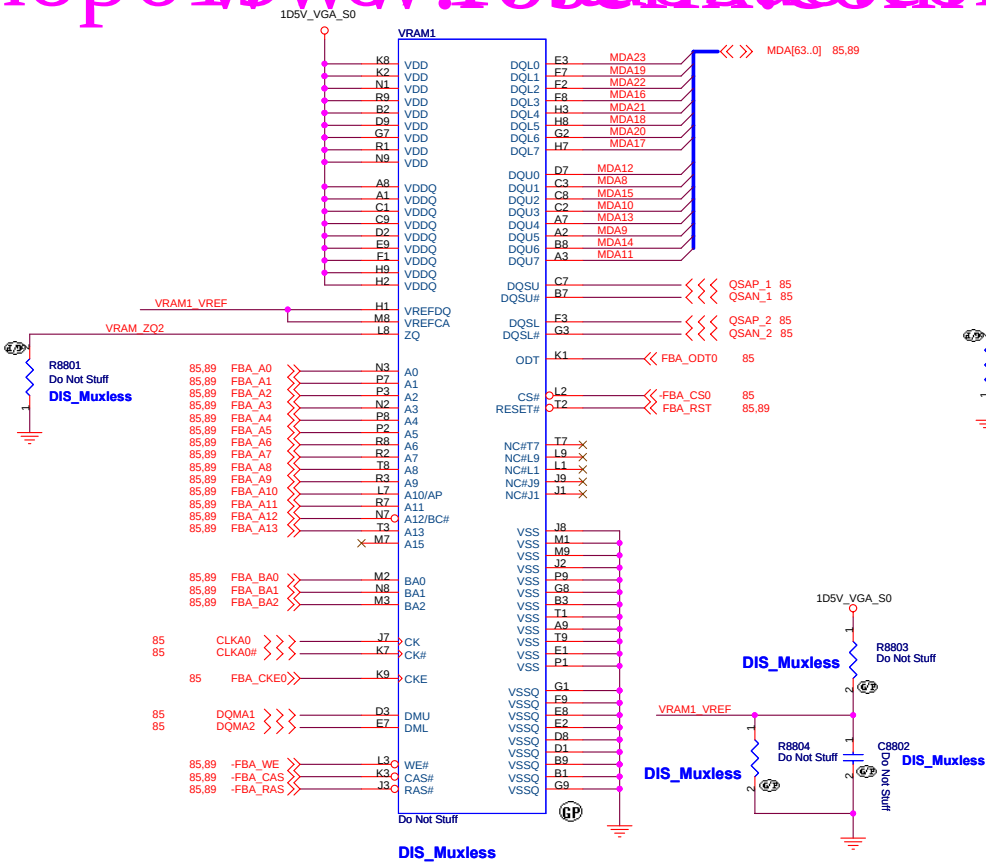
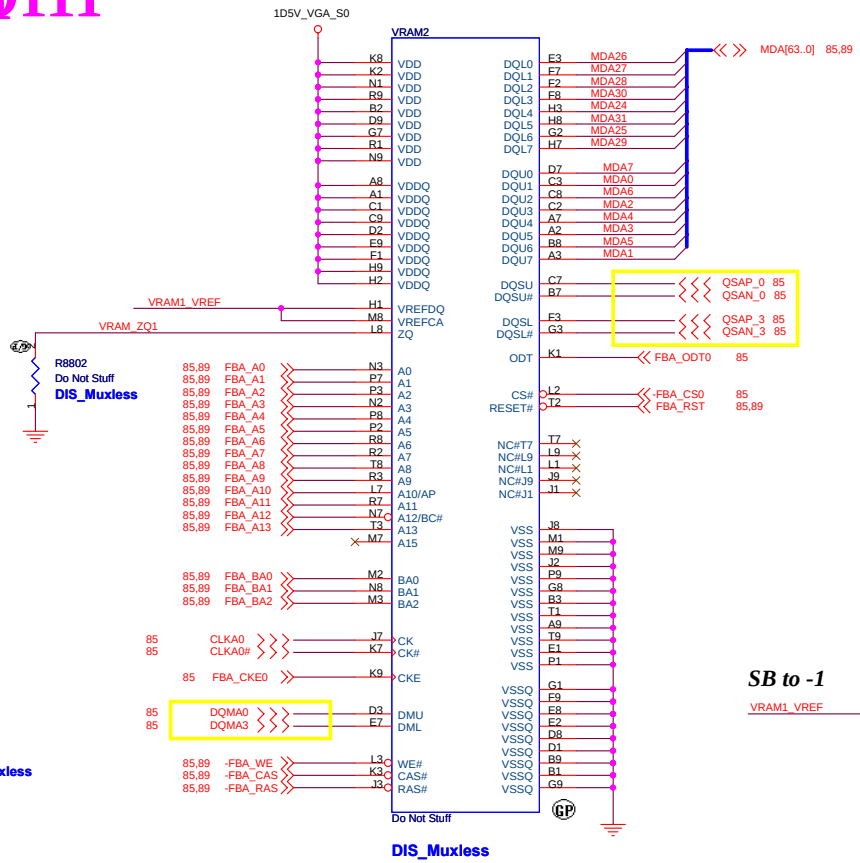
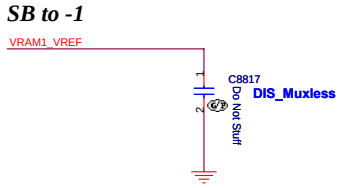




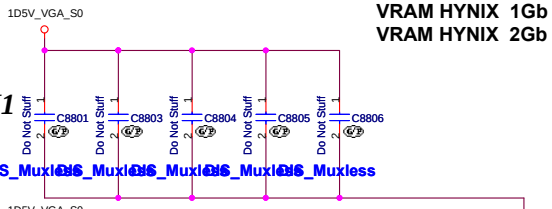
FB CMD mapping Mode D-N12x



VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

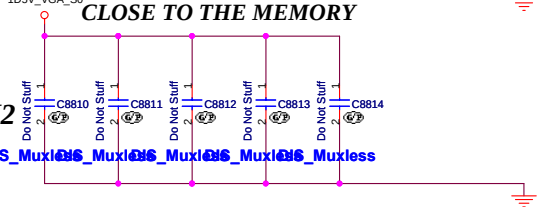
DG requires 4x0.1uF and 8x1.0uF per VRAM chip

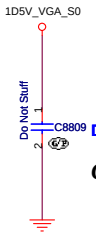
FOR VRAM1



CLOSE TO THE MEMORY

FOR VRAM2





CLOSE TO THE MEMORY

HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: Custom | Document Number: JE40-HR | Rev: -1

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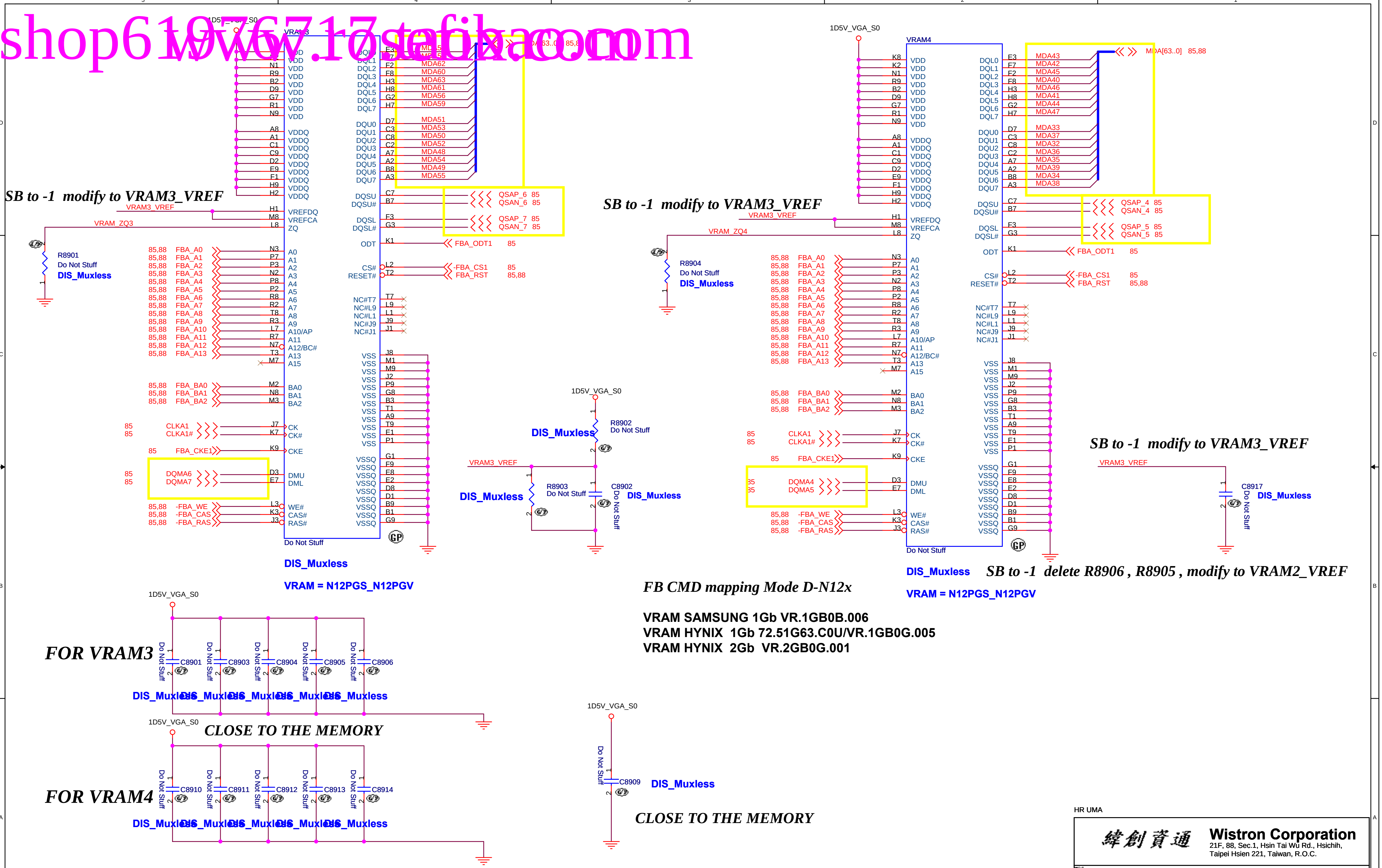
VRAM3
VRAM4
1D5V_VGA_S0
SB to -1 modify to VRAM3_VREF
SB to -1 modify to VRAM3_VREF
SB to -1 modify to VRAM3_VREF
SB to -1 delete R8906 , R8905 , modify to VRAM2_VREF
VRAM3_VREF
VRAM_ZQ3
VRAM_ZQ4
R8901
Do Not Stuff
DIS_Muxless
R8904
R8902
R8903
C8902
C8917
MDA[63..0] 85,88
QSAP_6 85
QSAN_6 85
QSAP_7 85
QSAN_7 85
QSAP_4 85
QSAN_4 85
QSAP_5 85
QSAN_5 85
FBA_ODT1 85
FBA_CS1 85
FBA_RST 85,88
CLKA1
CLKA1#
FBA_CKE1
DQMA6
DQMA7
DQMA4
DQMA5
FBA_WE
FBA_CAS
FBA_RAS
VRAM = N12PGS_N12PGV
FB CMD mapping Mode D-N12x
VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001
FOR VRAM3
FOR VRAM4
C8901
C8903
C8904
C8905
C8906
C8910
C8911
C8912
C8913
C8914
C8909
CLOSE TO THE MEMORY
CLOSE TO THE MEMORY

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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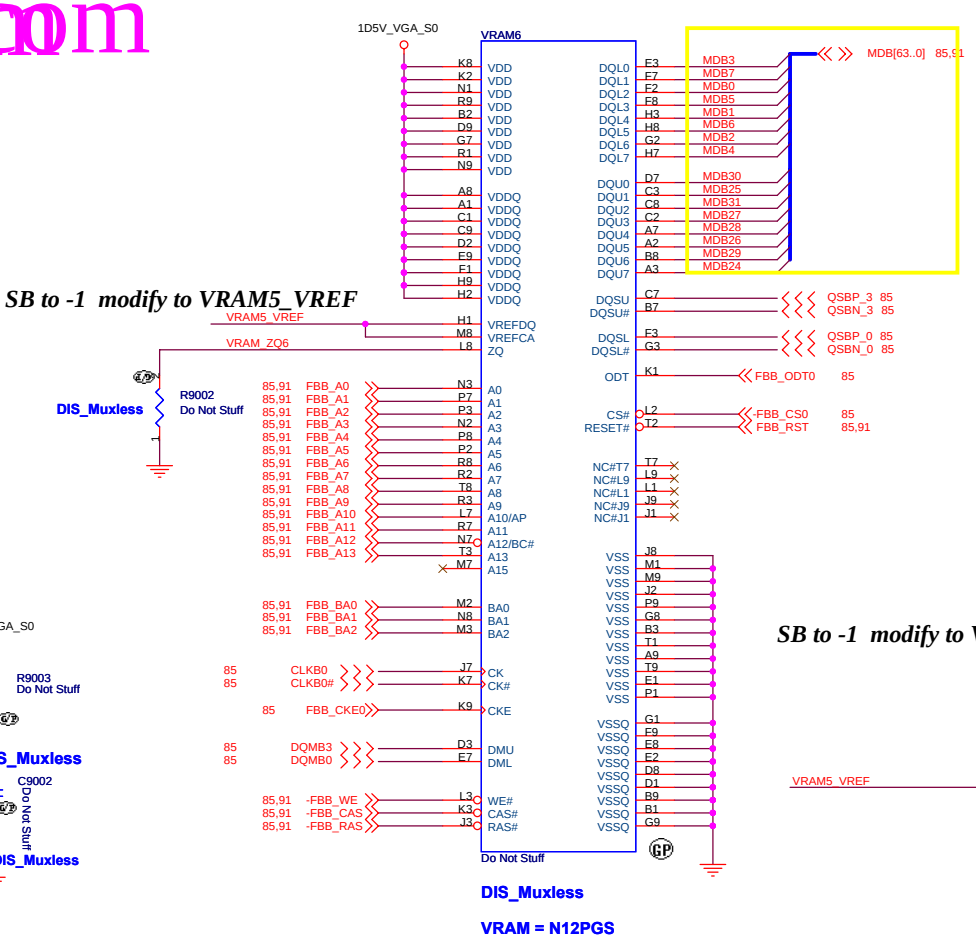
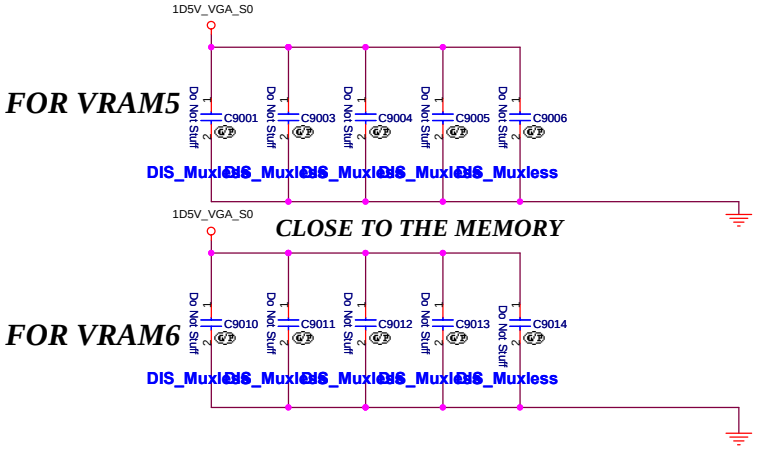
Title: **GPU-VRAM3,4 (2/4)**

Size: Custom | Document Number: **JE40-HR** | Rev: **-1**

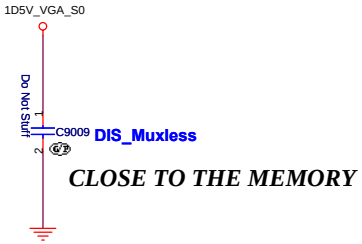
Date: Thursday, December 02, 2010 | Sheet 89 of 102



VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



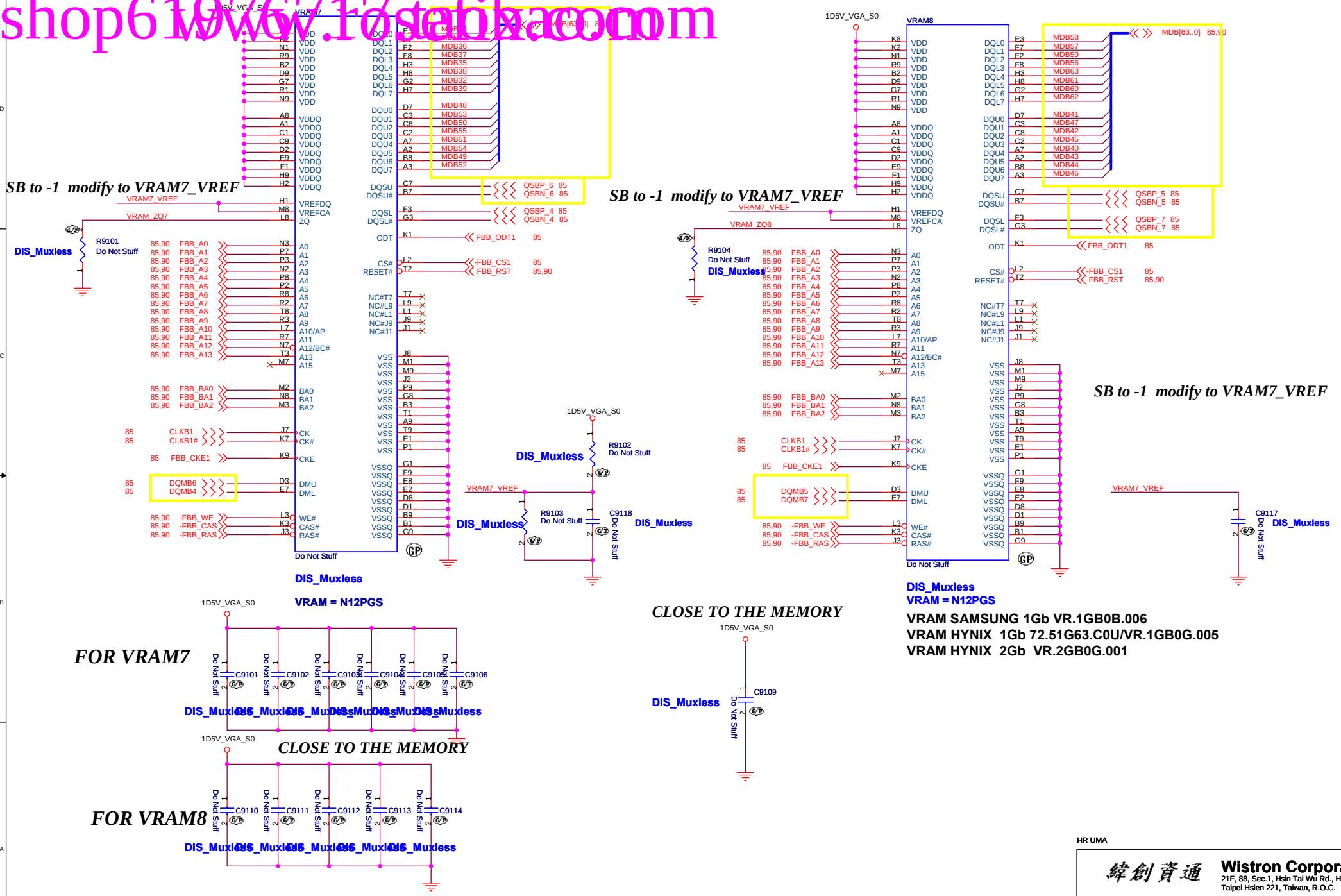
DG requires 4x0.1uF and 8x1.0uF per VRAM chip



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)
Size: Custom | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 90 of 102



HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM7,8 (4/4)**

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Custom	JE40-HR	-1

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20100715

S3.D = PWR.Plane.Regulator_GFX

20100719

SB 20100831

SB 20100831

RT8208A

N12P GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.00V
	H	H	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

N12P GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.025V
	H	H	

Vout=0.75V*(R1+R2)/R2

Design Current = 21.94A
24.14A<OCP< 28.53A

Vout=0.75V*(R1+R2)/R2

SB to -1 modify PR9213 VGA_Core to 1.05V

HR UMA	
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	RT8208B +VGA_CORE
Size: Custom	Document Number: JE40-HR
Rev	-1
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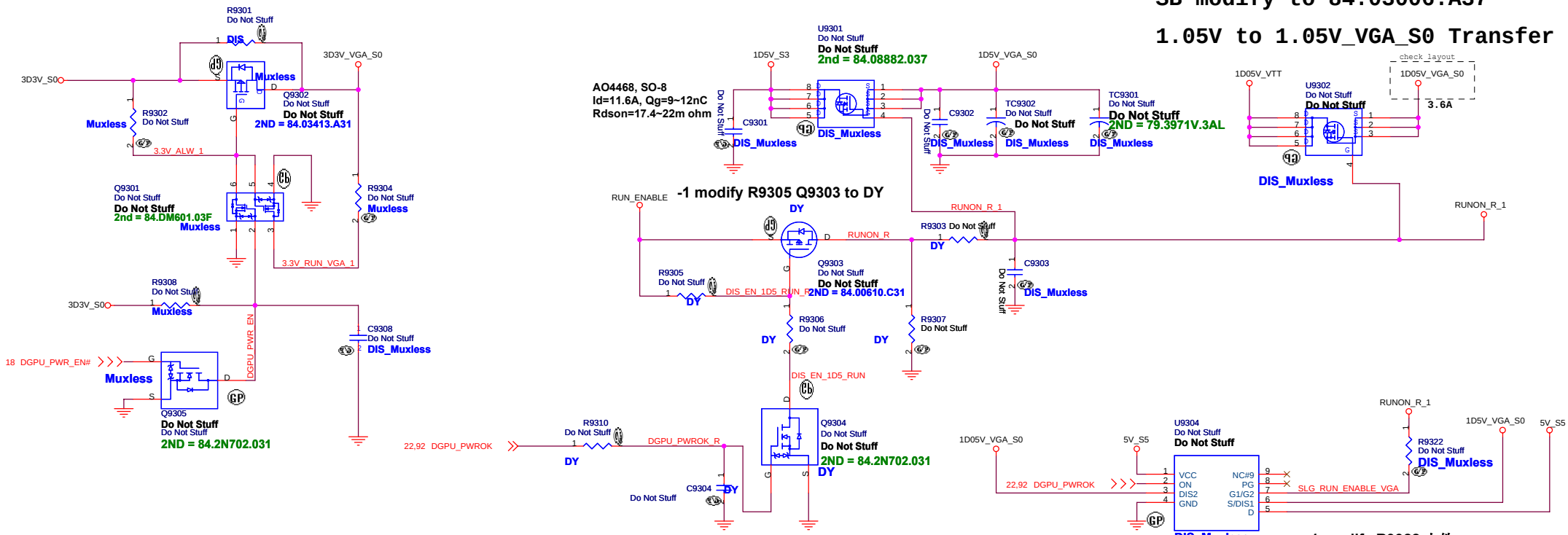
+3VS to 3.3V_DELAY Transfer

1D5V_VGA_S0

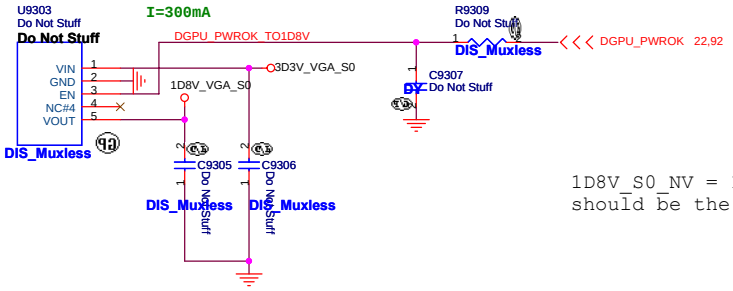
SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer



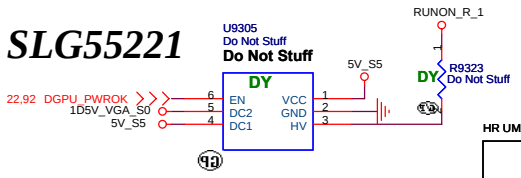
RT9025 for 1D8V_VGA

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

-1 co-layout SLG55221



HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size: Custom | Document Number: JE40-HR | Rev: -1

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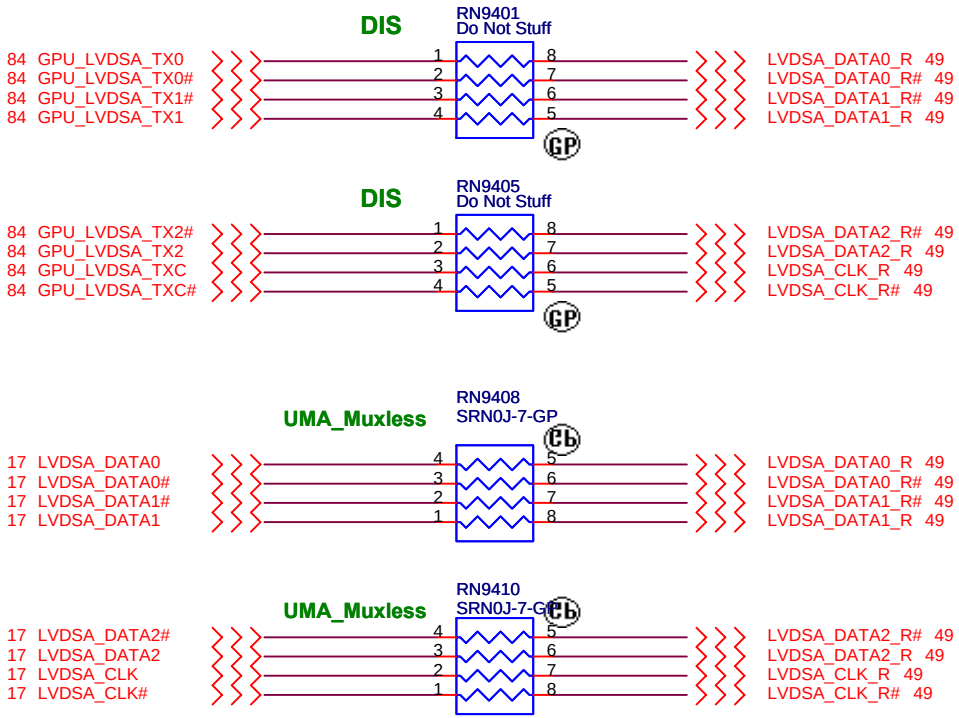
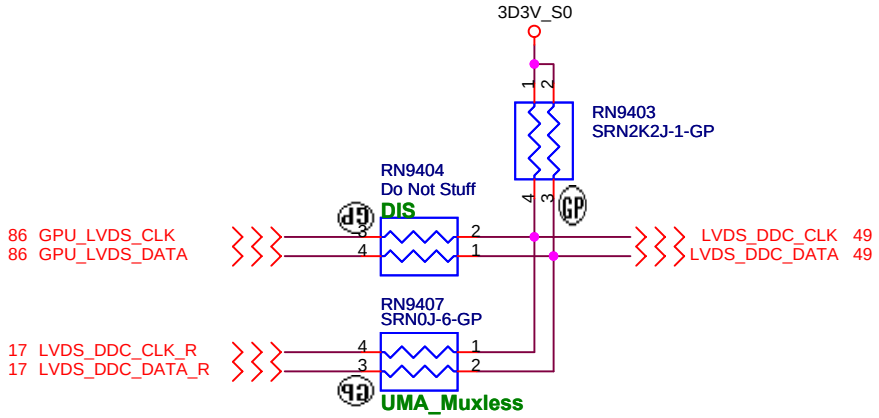
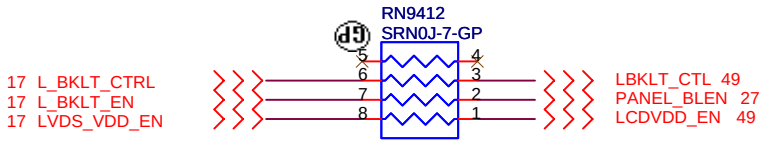
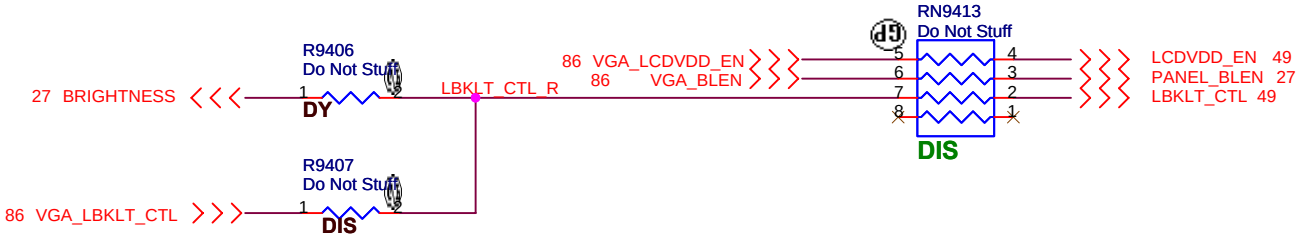




Panel BL brightness/Power En/BL En





HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

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Close to CRT Board CONN

CRT DDCDATA & DDCCLK

RN9501
Do Not Stuff

86 VGA_CRT_BLUE
86 VGA_CRT_GREEN
86 VGA_CRT_RED

CRT_BLUE_R 50
CRT_GREEN_R 50
CRT_RED_R 50

DIS

RN9503
SRN0J-6-GP

17 CRT_DDC_DATA
17 CRT_DDC_CLK

DDCDATA 50
DDCCLK 50

5V Tolerance

UMA_Muxless

Pull high 在CRT

RN9502
SRN0J-7-GP

17 CRT_RED
17 CRT_GREEN
17 CRT_BLUE

CRT_RED_R 50
CRT_GREEN_R 50
CRT_BLUE_R 50

UMA_Muxless

RN9504
Do Not Stuff

86 VGA_CRT_DDCDATA
86 VGA_CRT_DDCCLK

DDCDATA
DDCCLK

DIS

SB to -1 modify 4 port Logic

3D3V_S0

RN9505
SRN0J-6-GP

dGPU_SELECT_A
dGPU_SELECT_B

UMA_Muxless

3D3V_S0

RN9506
Do Not Stuff

dGPU_SELECT_B
dGPU_SELECT_A

DIS

CRT Hsync & Vsync level shift

L=>B0 -DIS
H=>B1 -UMA

dGPU_SELECT_A

5V_S0

For DIS CRT

U9506B
TC74VHCT125AFTQK2M-GP
73.74125.F0B
2nd = 73.74125.L13

86 VGA_CRT_VSYNC

CRT_VSYNC1_1

For UMA CRT

5V_S0

dGPU_SELECT_B

U9506C
TC74VHCT125AFTQK2M-GP
73.74125.F0B
2nd = 73.74125.L13

17 CRT_VSYNC

5V_S0

For DIS CRT

U9506A
TC74VHCT125AFTQK2M-GP
73.74125.F0B
2nd = 73.74125.L13

86 VGA_CRT_HSYNC

CRT_HSYNC1_1

For UMA CRT

5V_S0

dGPU_SELECT_B

U9506D
TC74VHCT125AFTQK2M-GP
73.74125.F0B
2nd = 73.74125.L13

17 CRT_HSYNC

SB to -1 modify R9503,R9504 to 10 ohm

CRT_HSYNC1_1 1 R9504 10R2J-2-GP CRT_HSYNC_CON 50

CRT_VSYNC1_1 1 R9503 10R2J-2-GP CRT_VSYNC_CON 50

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Switch

Size: A3 | Document Number: JE40-HR | Rev: -1

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SSID = SPIC

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TOUCH PANEL***

Size	Document Number	Rev
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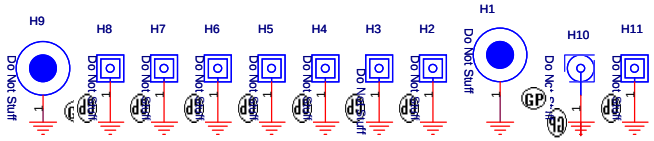
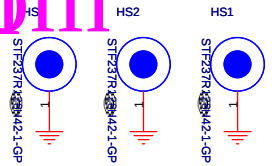
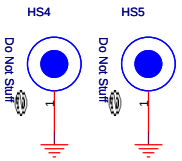


CPU

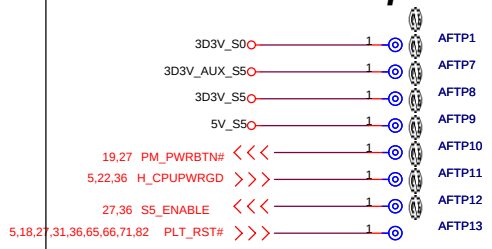


VGA



DIS_Muxless DIS_Muxless

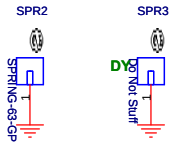
Check test point



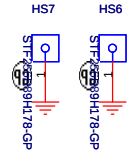
Test Point放在Dimm Door打開可量測處

SB to -1 BOM add SPR2

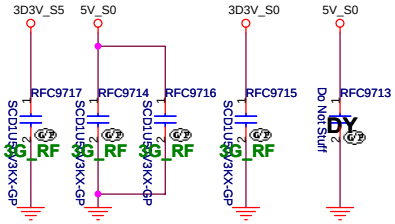
-2 delete SPR5

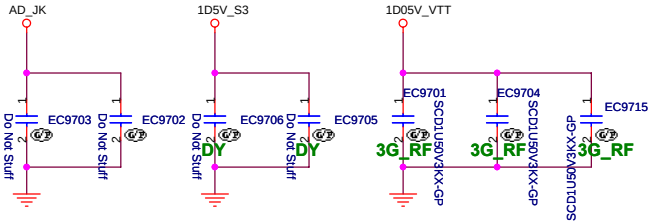


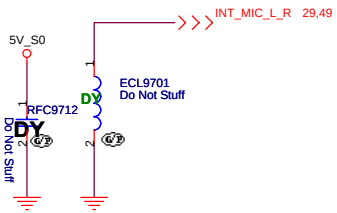
Change:34.40V16.001

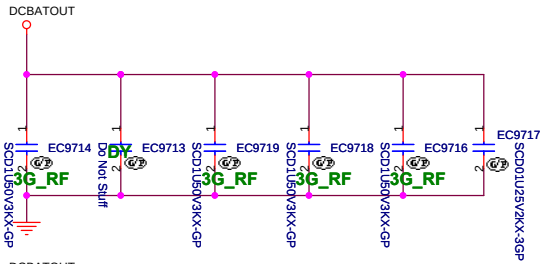


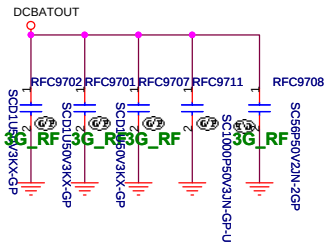
3G Sku

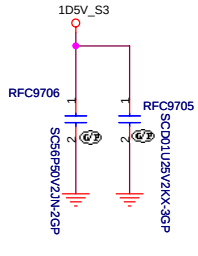


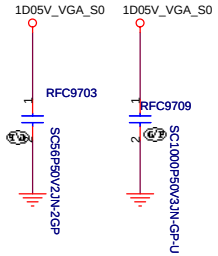


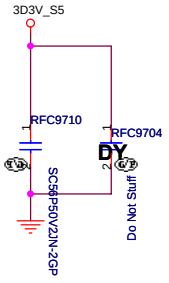


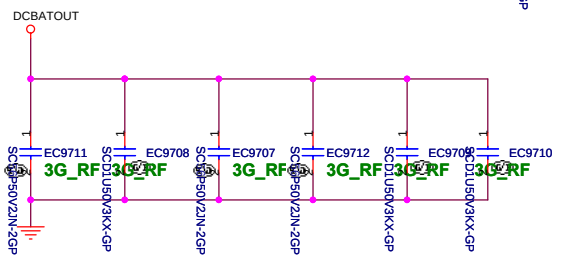












HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	JE40-HR	-1

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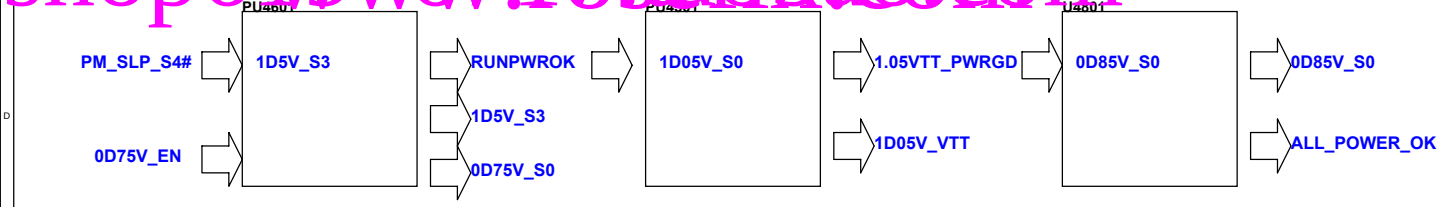
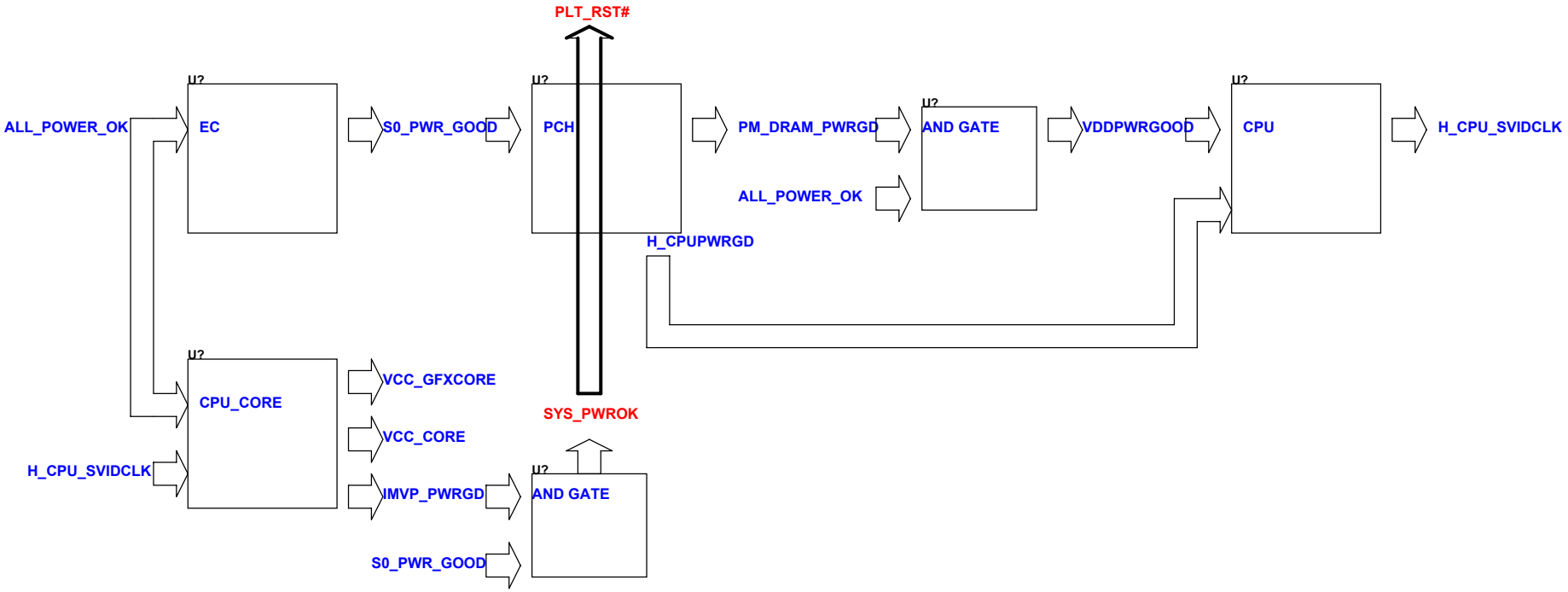
Power Sequence





HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

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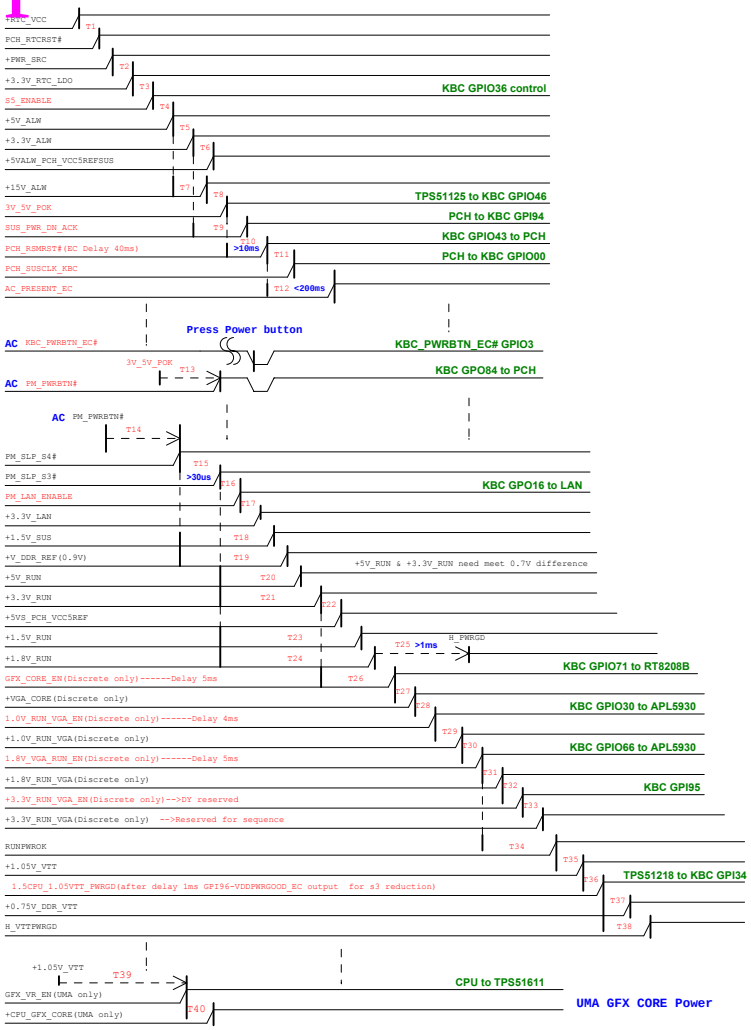
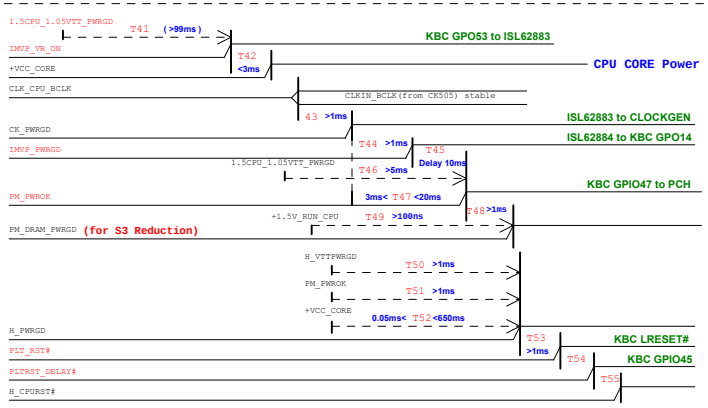
Intel-Power up Sequence

red word: KBC GPIO

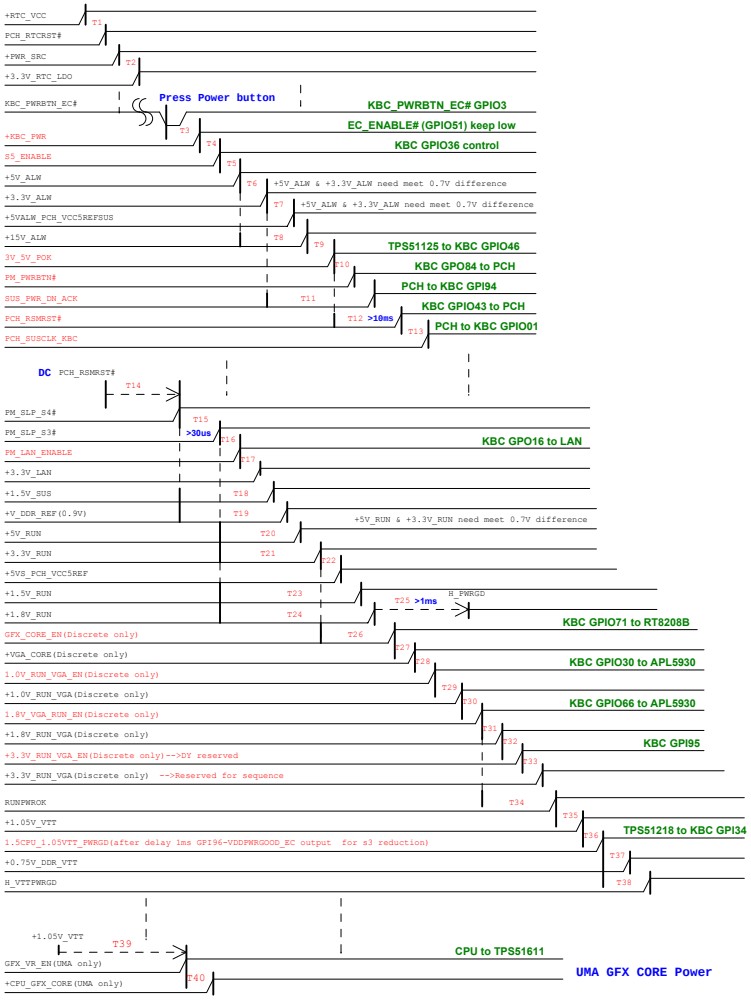
(AC mode)

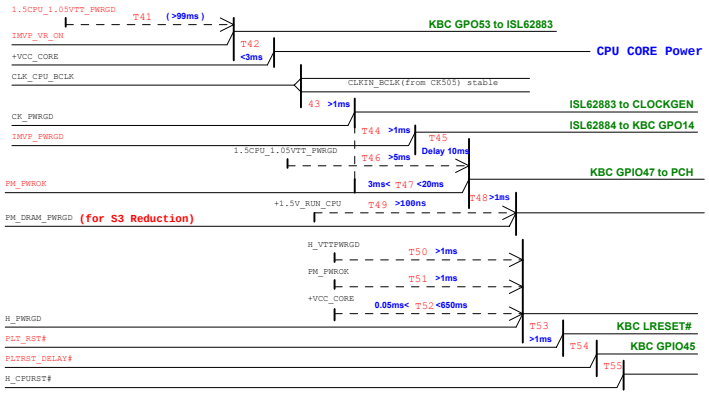




(DC mode)

red word: KBC GPIO





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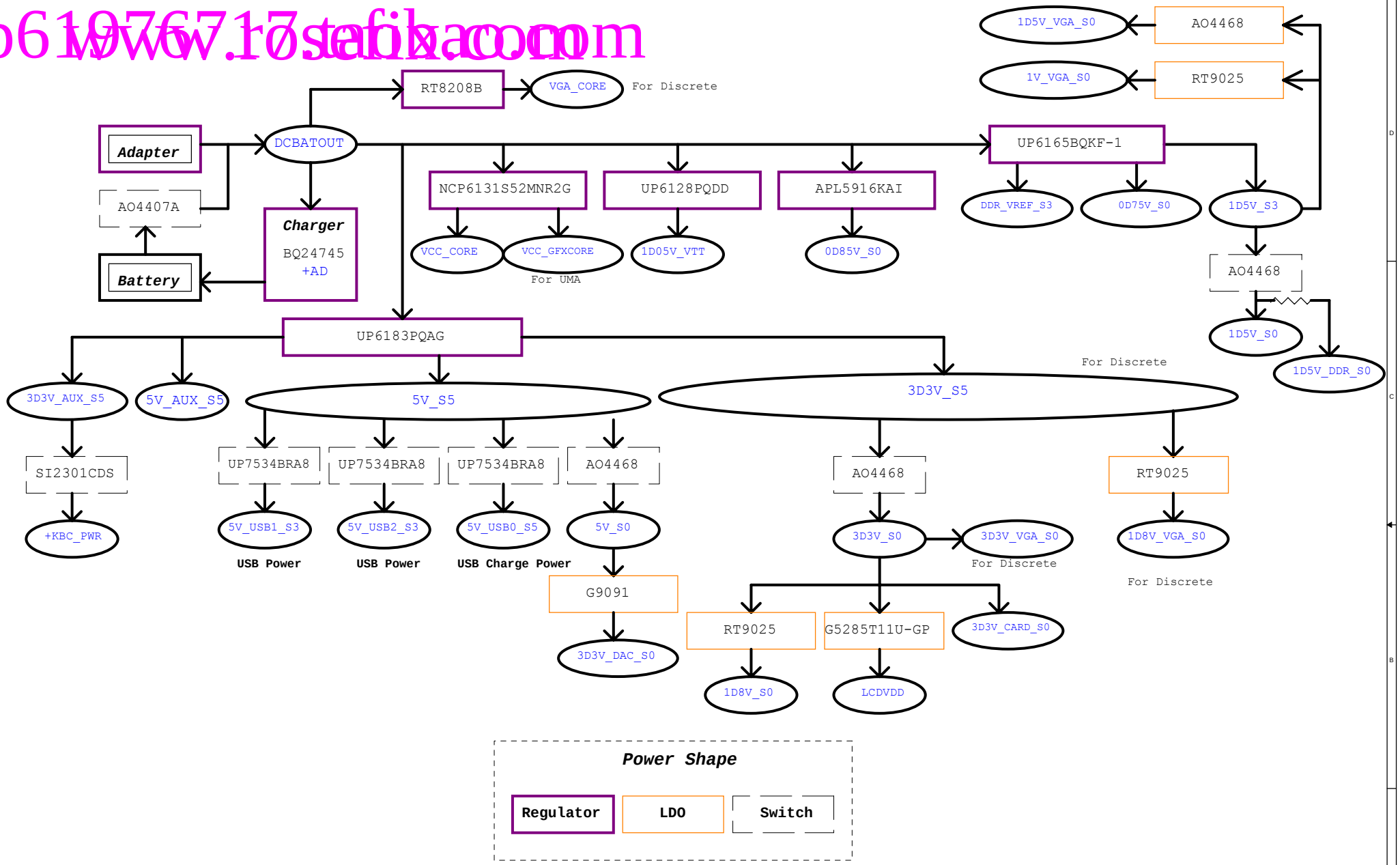

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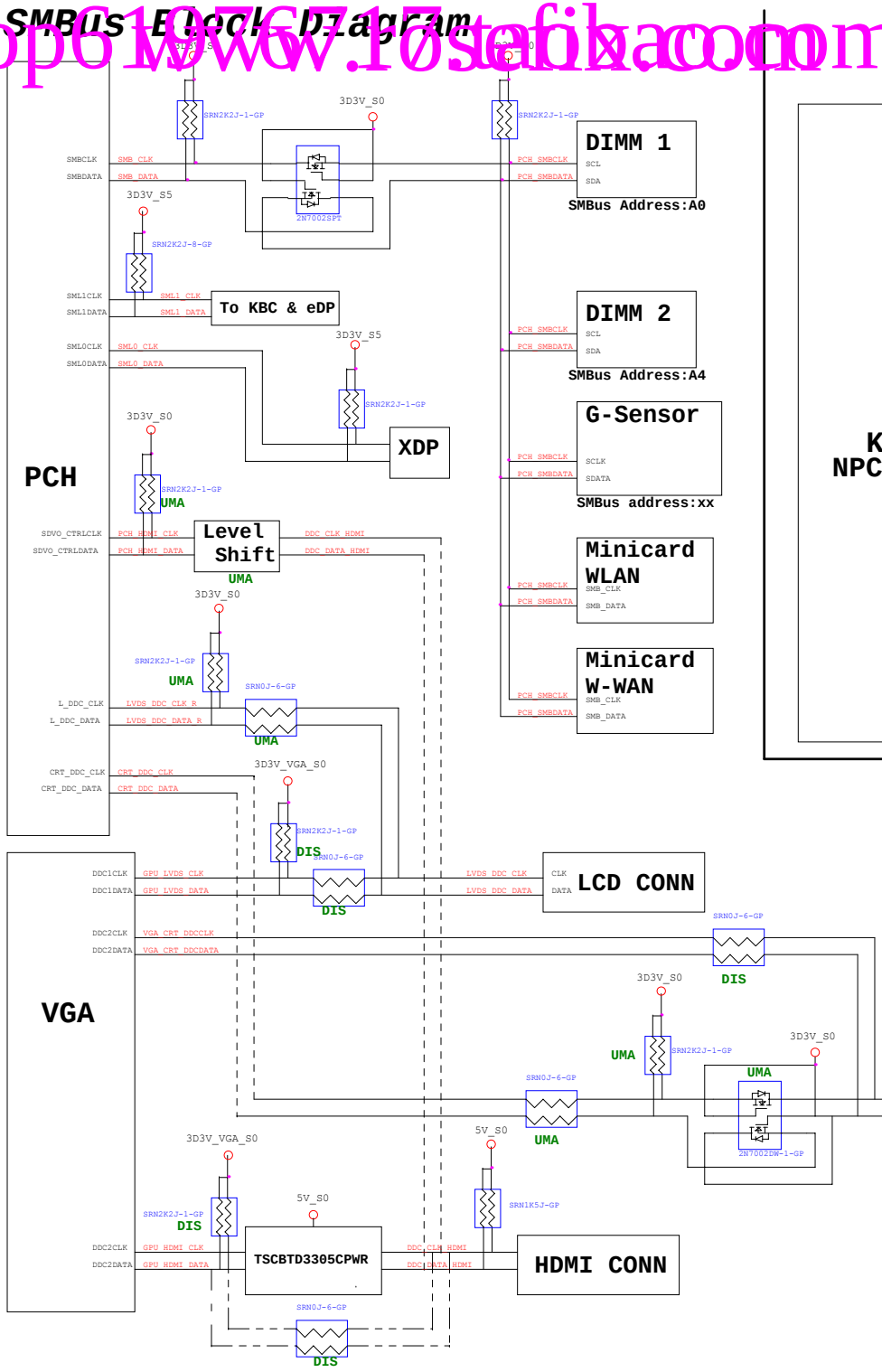
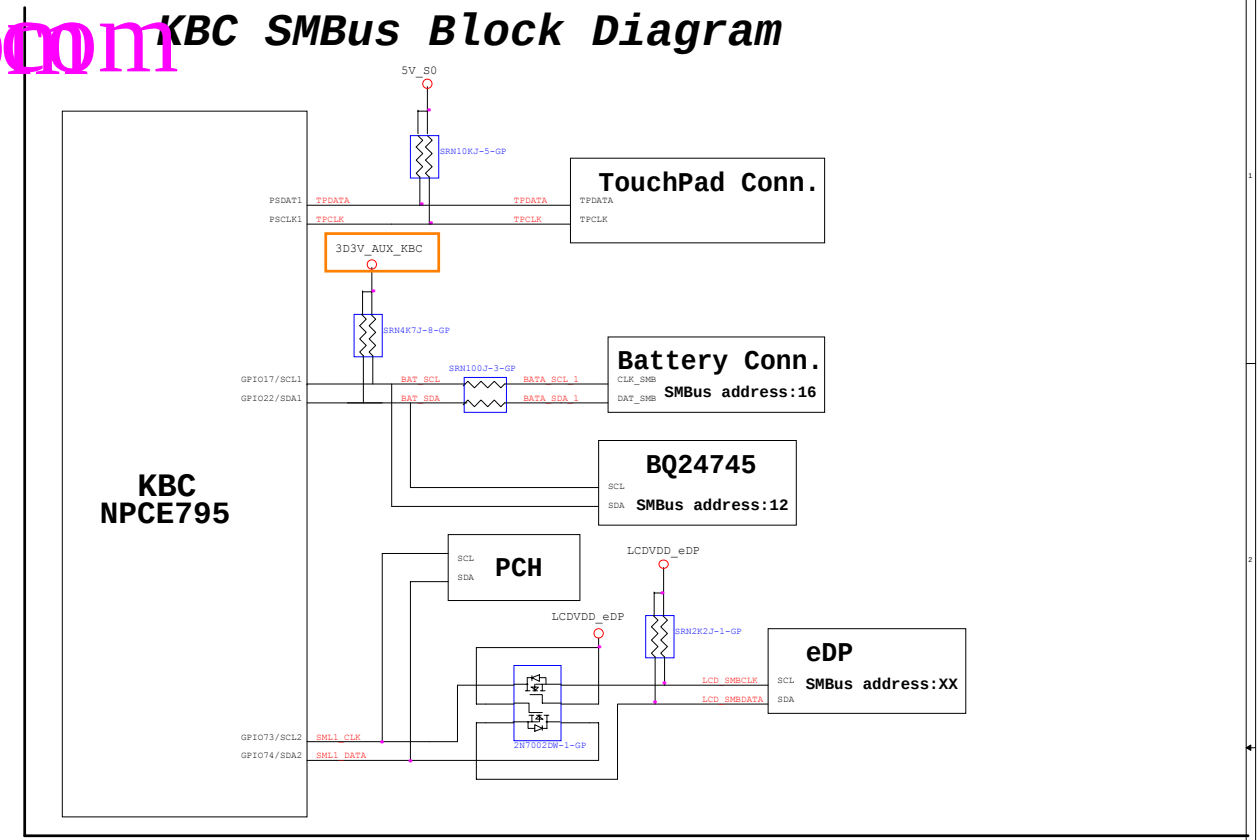
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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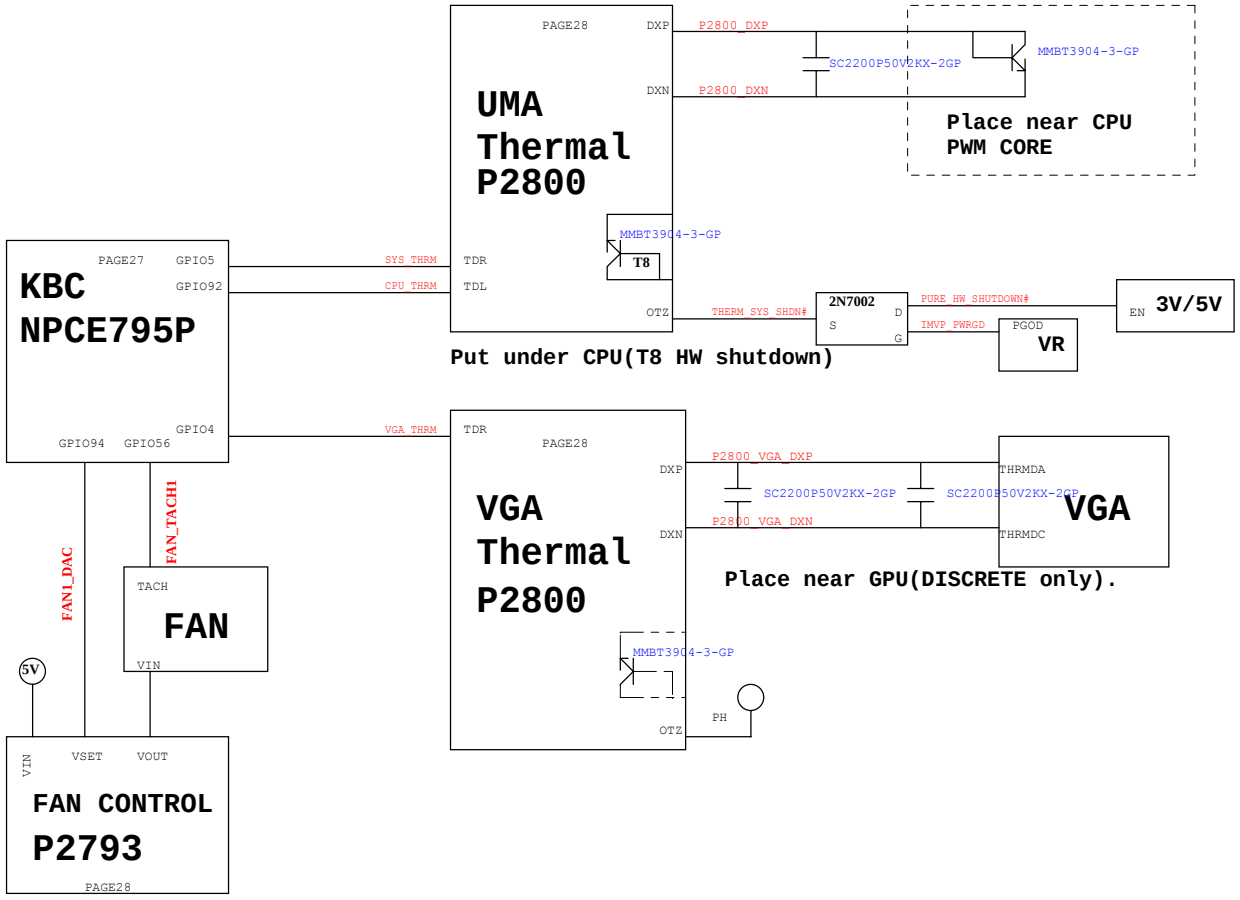
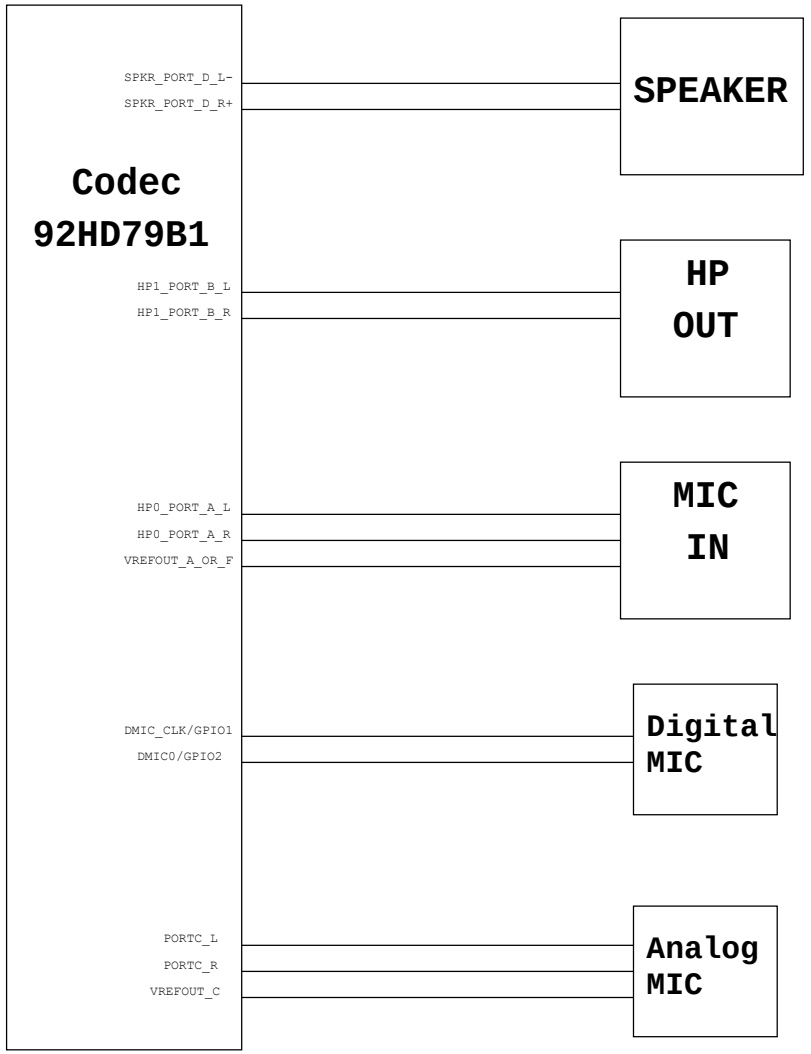
Thermal Block Diagram



Audio Block Diagram



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