

Model Name : ZIWB0/ZIWB1/ZIWE0
File Name :

Compal Confidential

ZIWB0/ZIWB1/ZIWE0 UMA M/B Schematics Document

Intel Bay Trail M

2014-02-10

REV:1.0

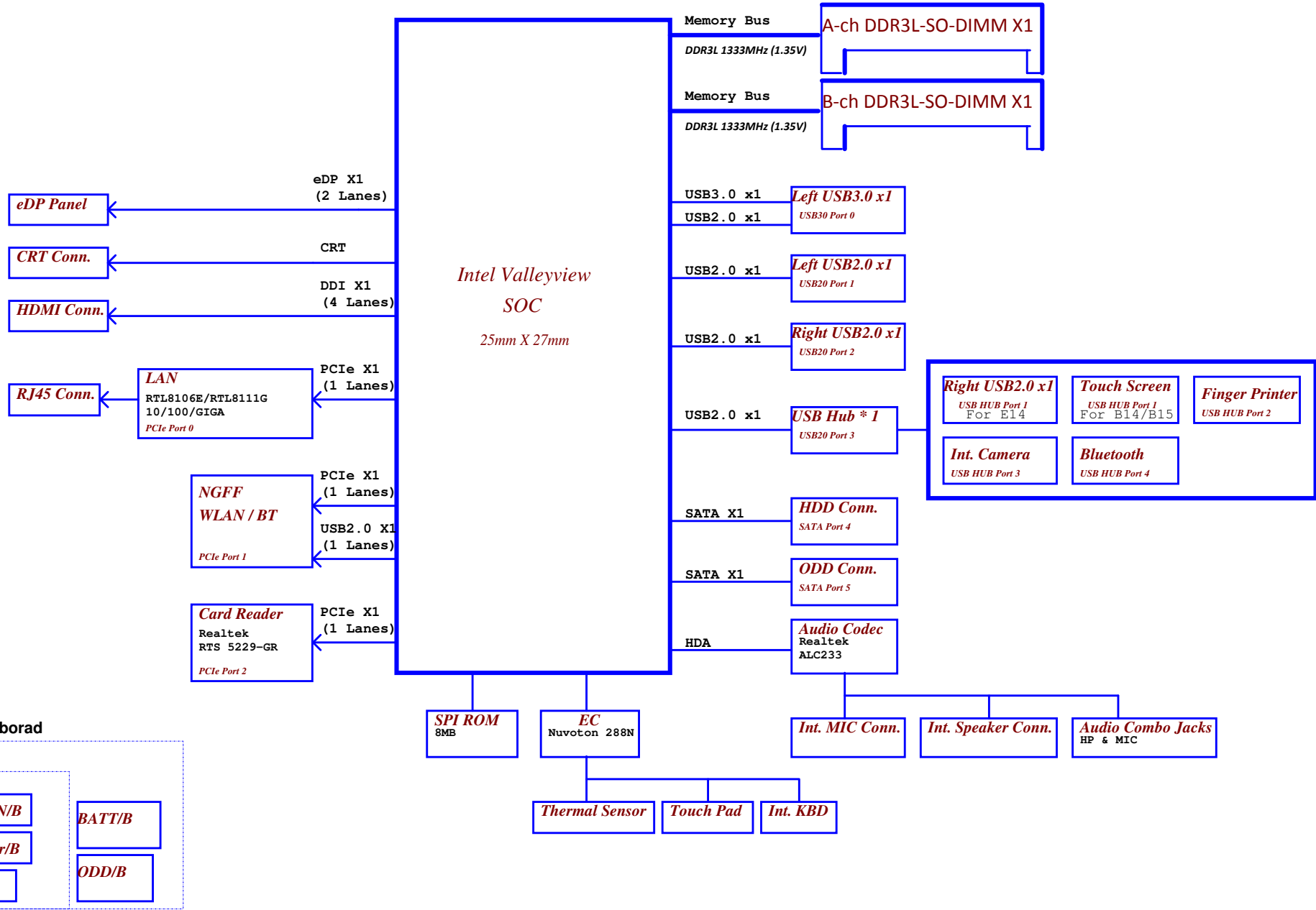
14PCB@
DA1 PCB

Part Number	Description
DA60013Z010	REV1.0 M/B

15PCB@
DA2 PCB

Part Number	Description
DA60013Z110	REV1.0 M/B

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				Cover Page		
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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	ME@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
ESD requirement	ESD@
ESD requirement unpop	@ESD@
Touch Screen	TS@
B/E series sku	B14@
B/E series sku	B15@
B/E series sku	E14@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
Charger	0b00010010 (0x12H)

SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

EC SM Bus2 address

Device	Address
GPU	0x9E
Thermal	1001_101xb

43 level BOM table

43 Level	Description	BOM Structure



S IC FH8065301616203 SR1SF B3 1.86G C38!
Part Number = SA00007E860



S IC FH8065301616103 SR1SE B3 2.17G C38!
Part Number = SA00007E990



S IC FH8065301619509 SR1SJ B3 1.86G C38!
Part Number = SA00007EO50

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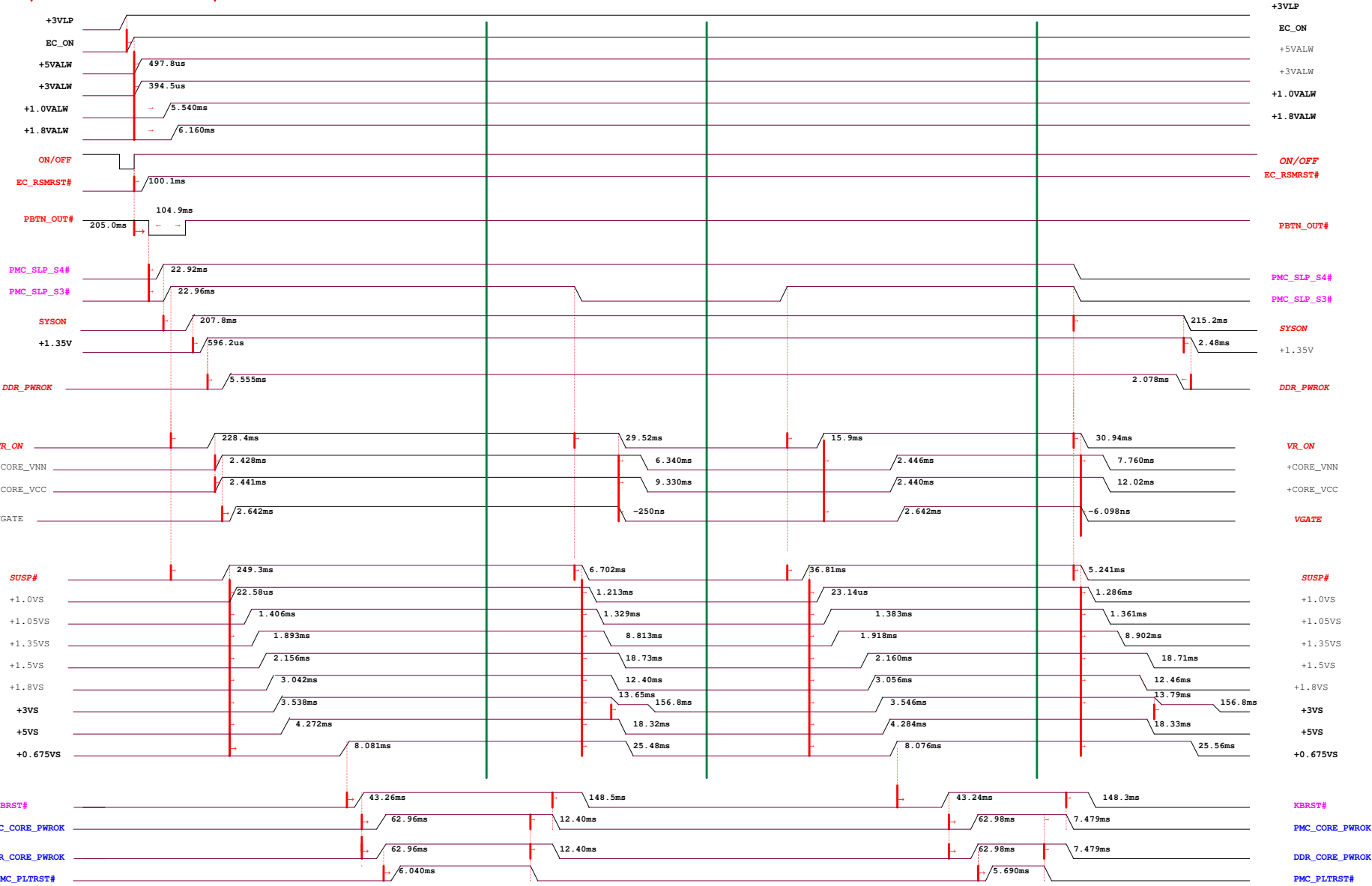
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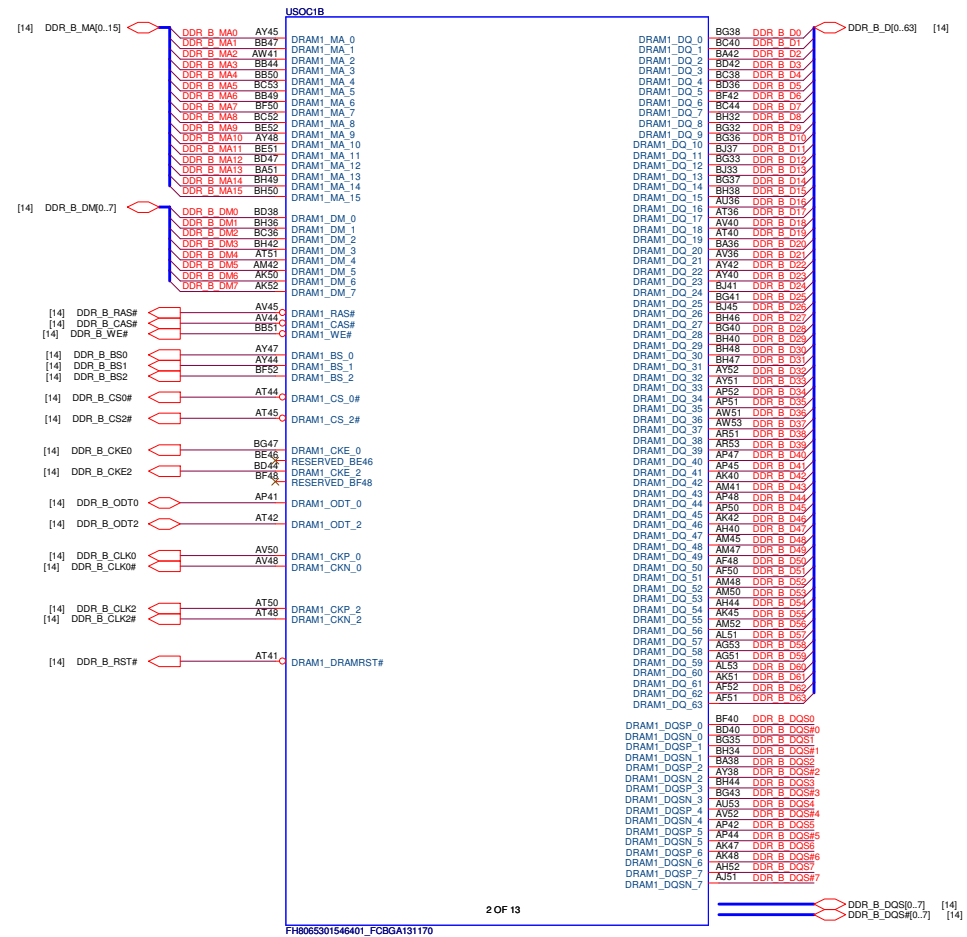
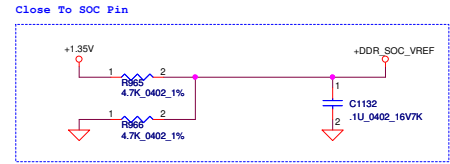
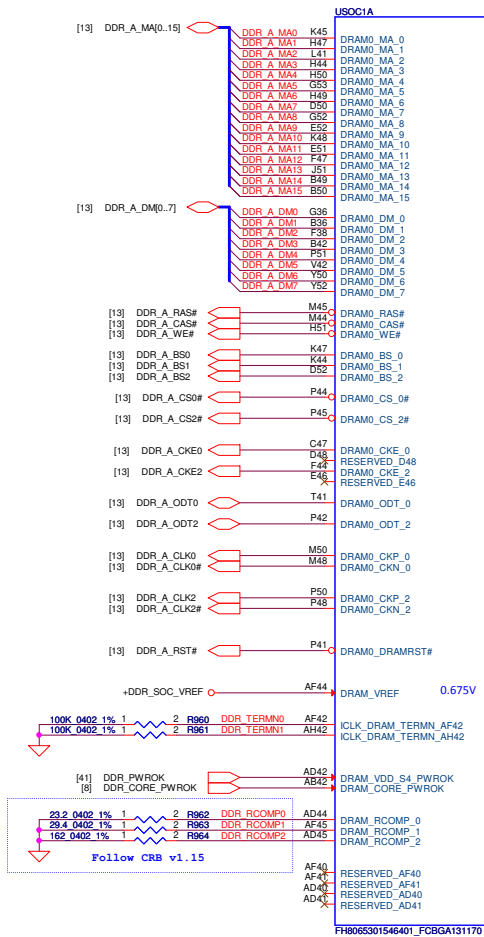
S3

S3 Resume

Power Off

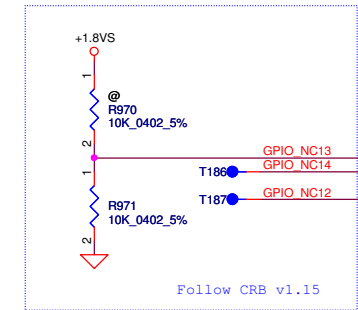
Plug in





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HDMI

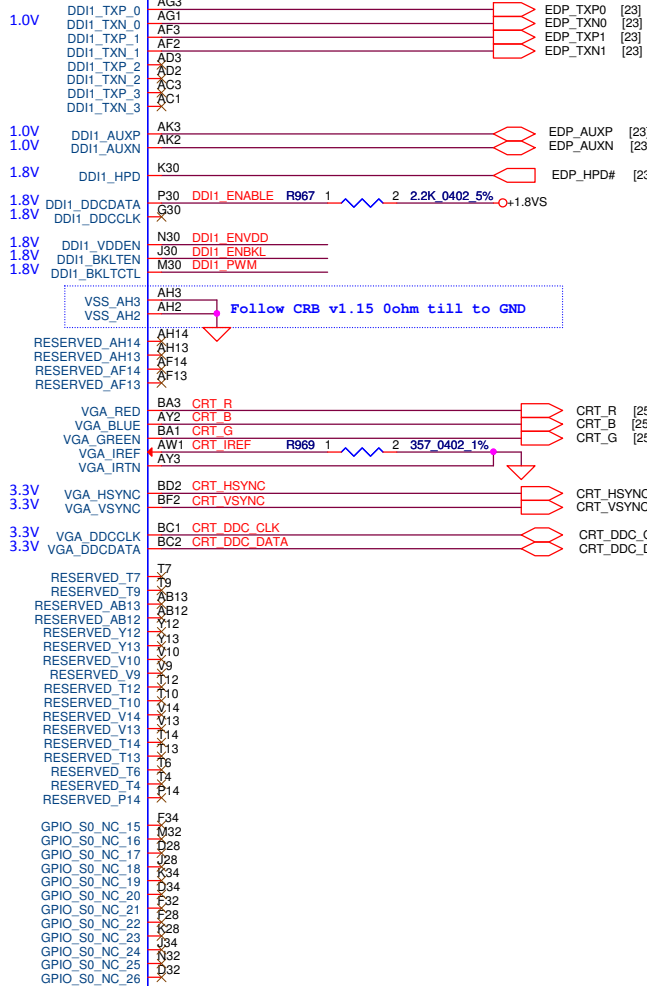


GPIO_S0_NC[13]:
Multiplexed with Hardware Straps Pin:MDSI_DDCDATA

USOC1C

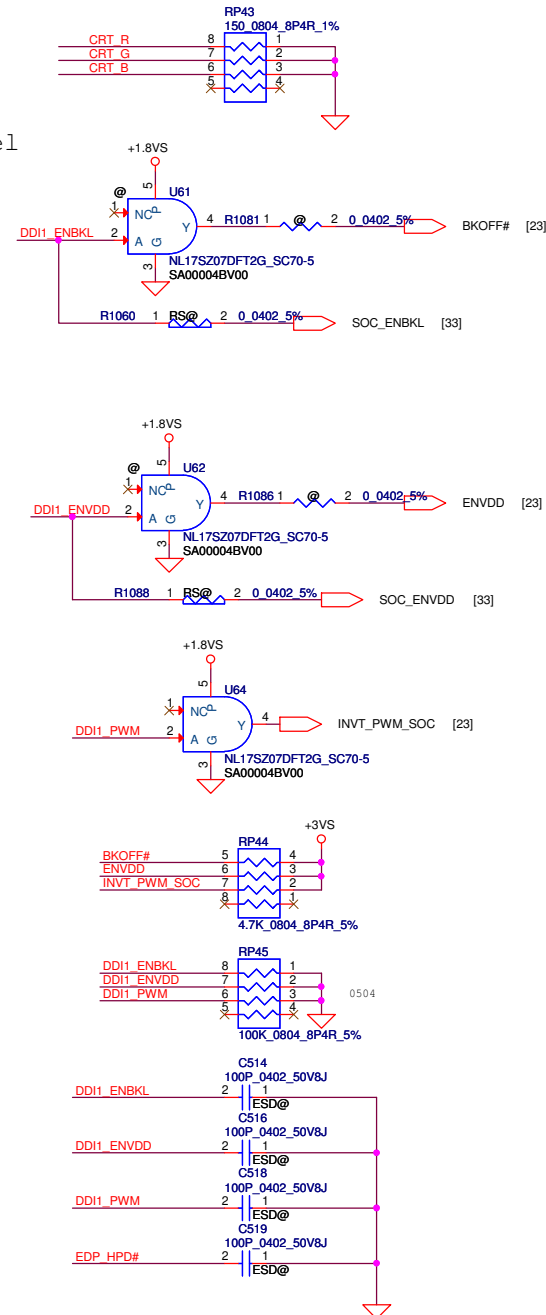
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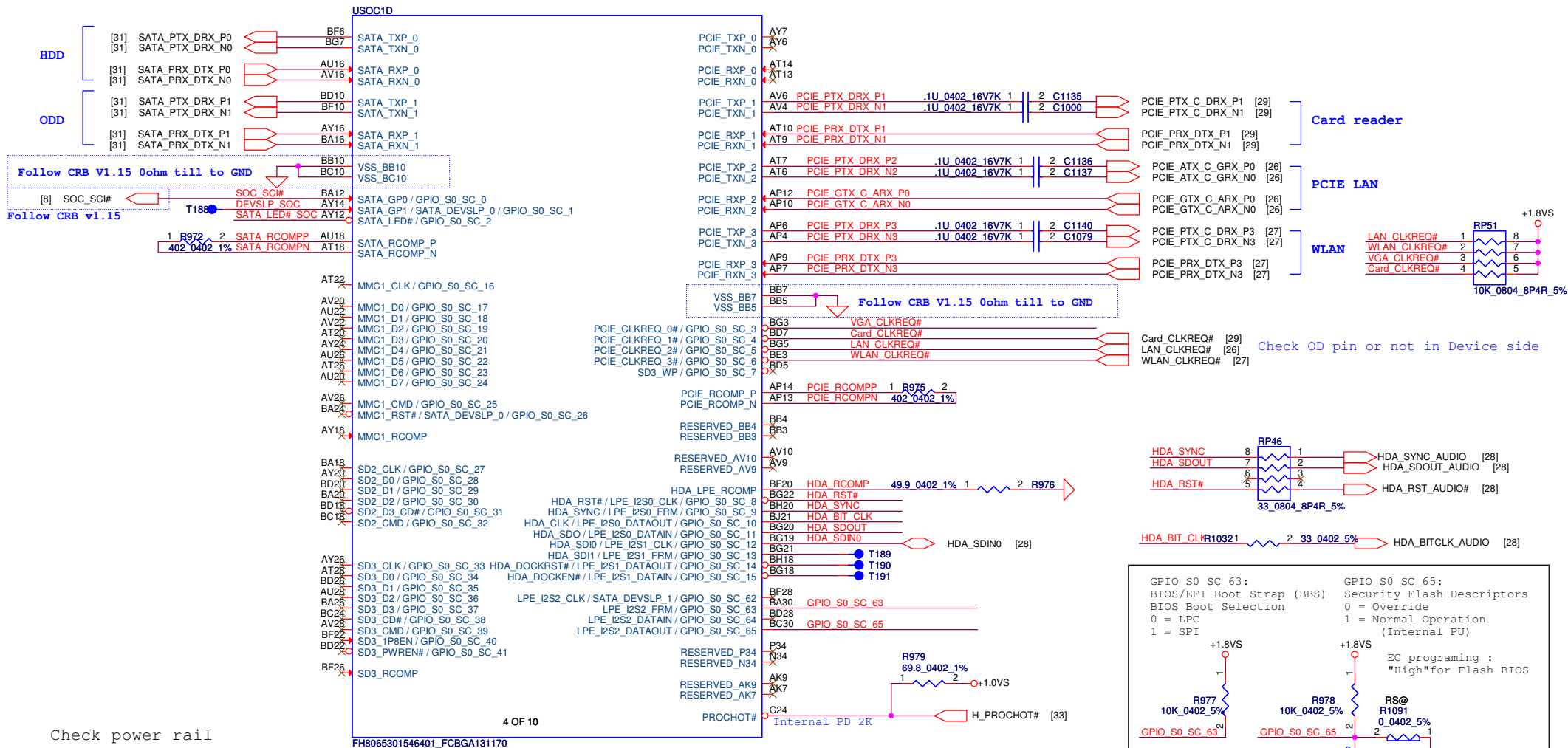


eDP Panel

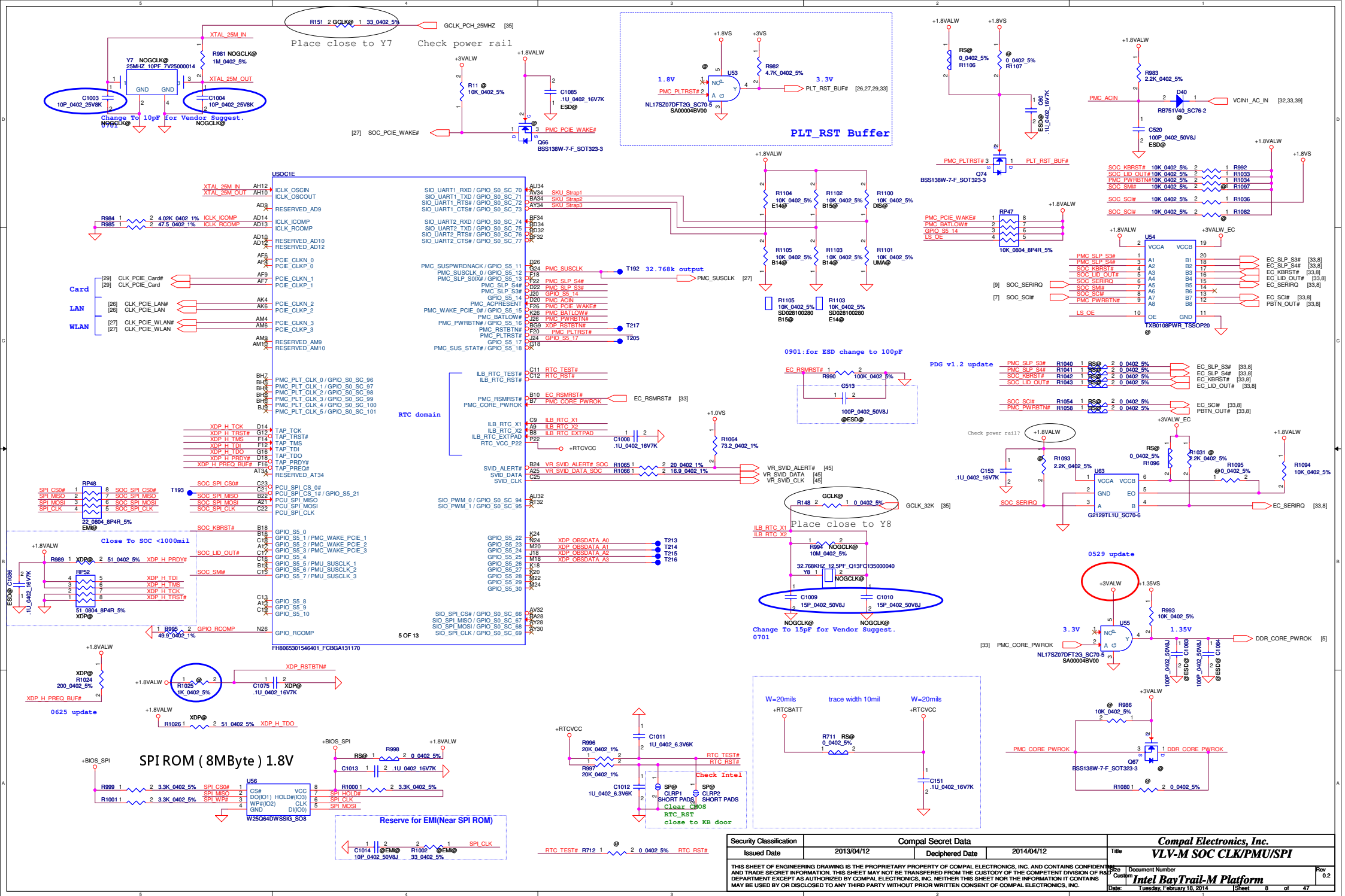
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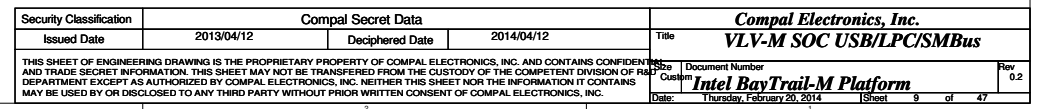


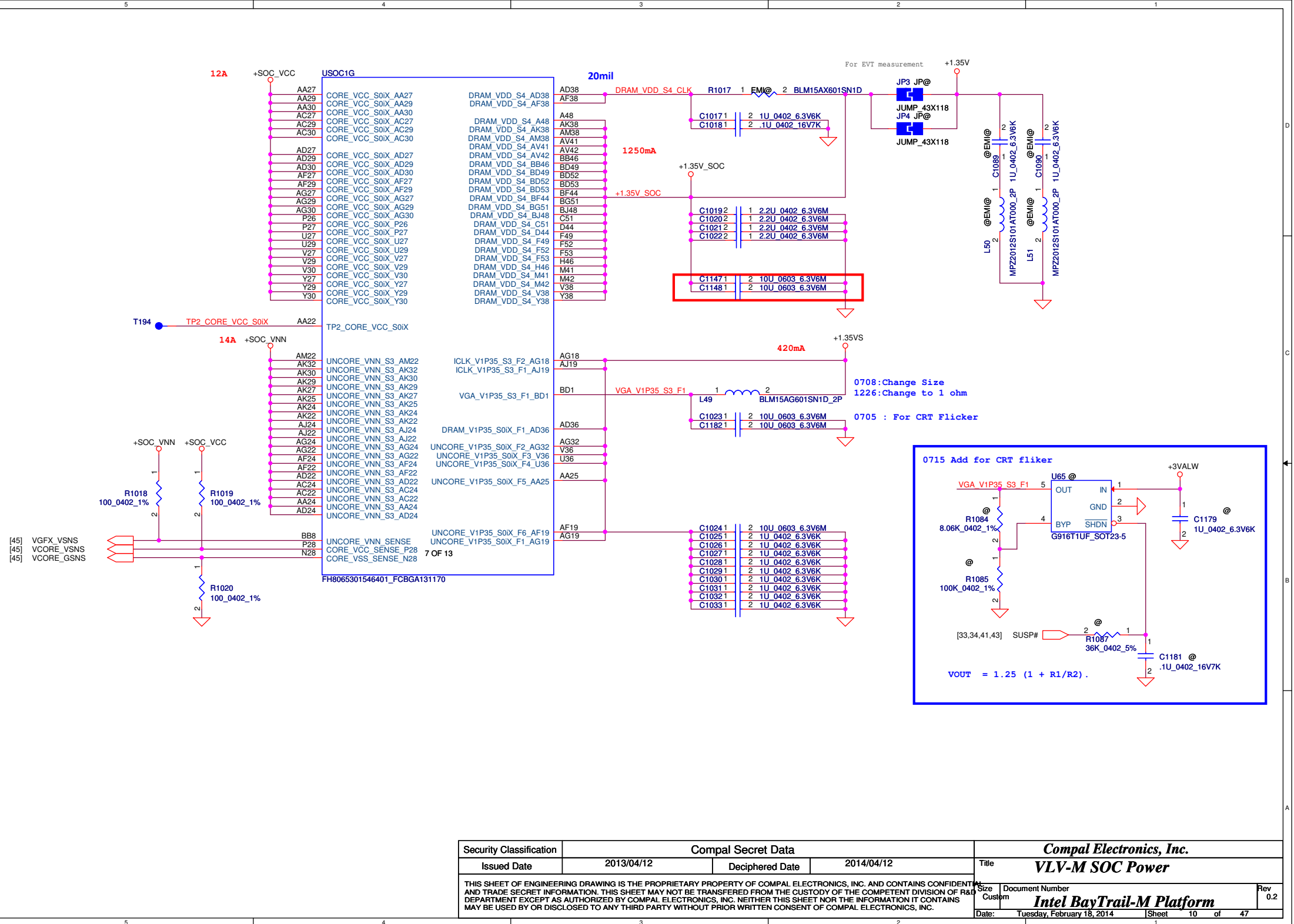
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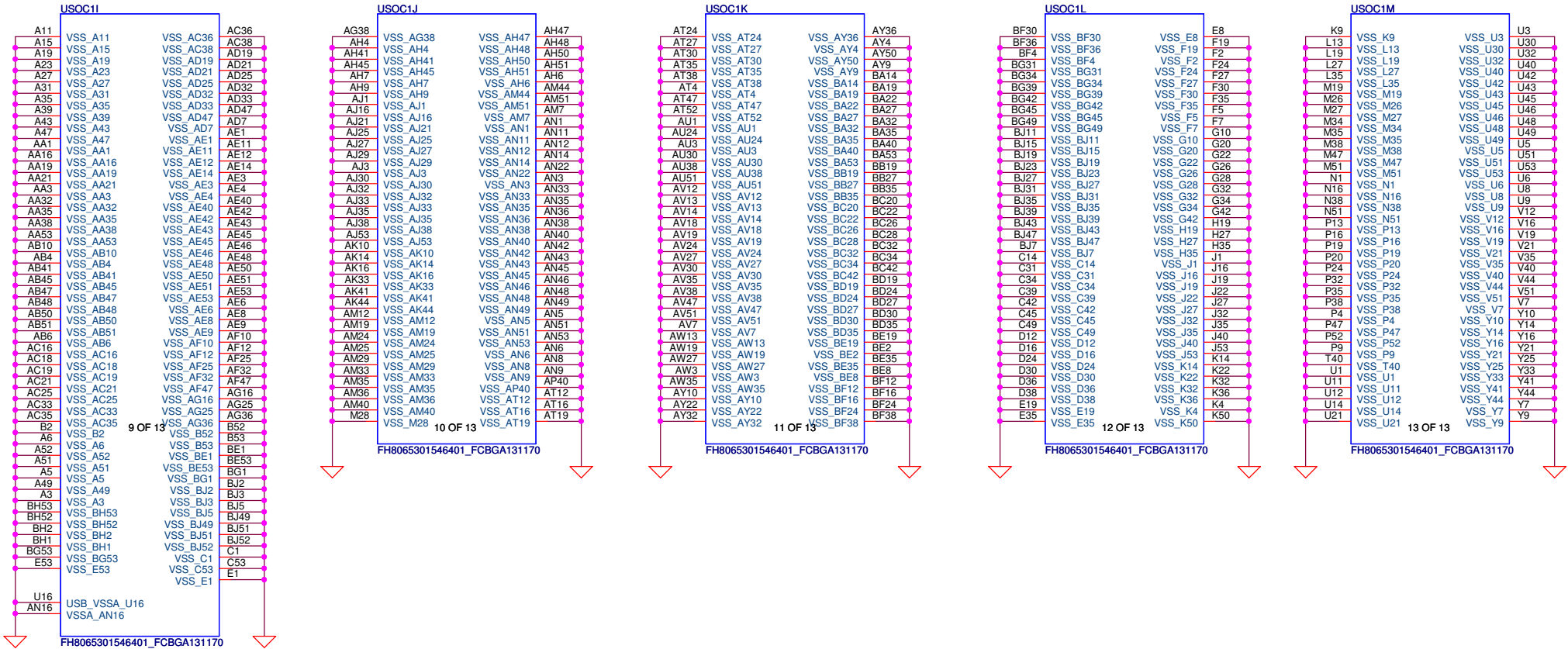


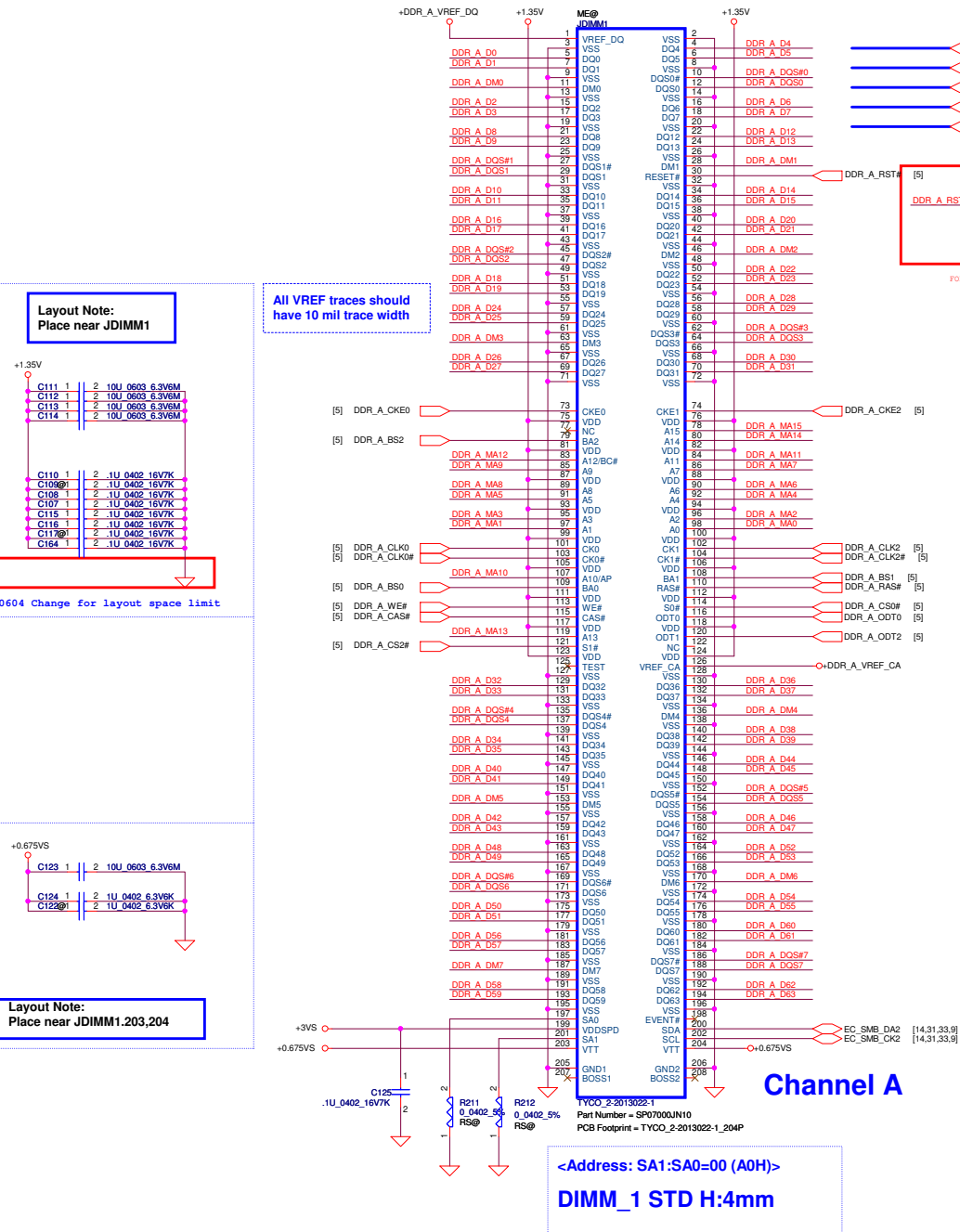
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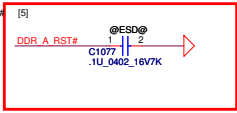


Layout Note:
Place near JDIMM1

All VREF traces should
have 10 mil trace width

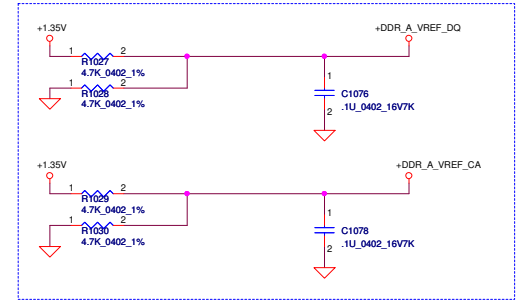
0604 Change for layout space limit

Layout Note:
Place near JDIMM1.203,204



FOR ENI/ESD Require 01/15

Signal voltage level = 0.675 V
PLACE TWO 4.7K RESISTORS CLOSE TO
DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
Decoupling caps are needed; one 0.1 uF placed close to VREF pins of each DDR3 SODIMM.

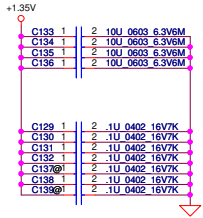


Channel A

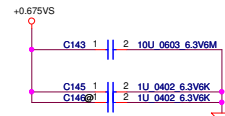
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DIMM_1 STD H:4mm

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					DDR3L DIMMA	
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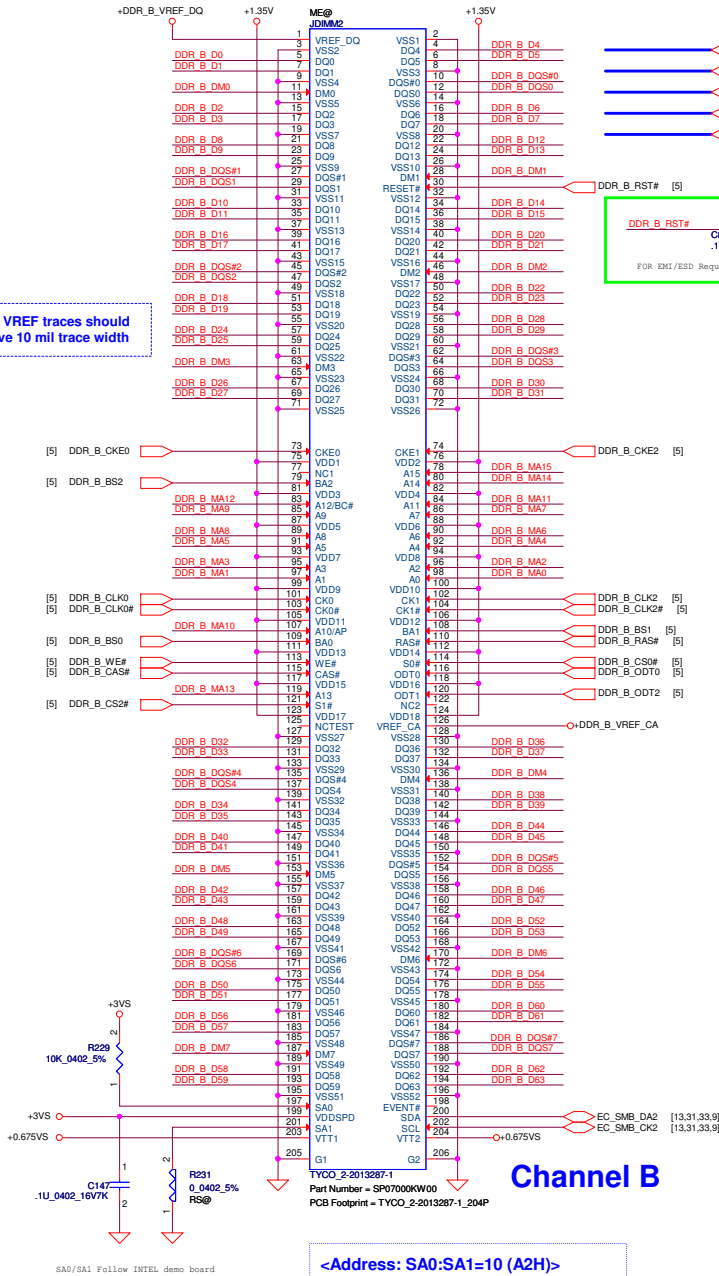
Layout Note:
Place near JDIMM2



All VREF traces should
have 10 mil trace width

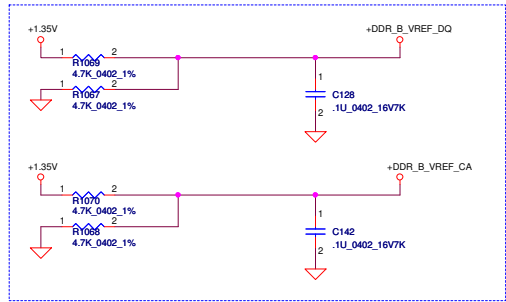


Layout Note:
Place near JDIMM2.203,204

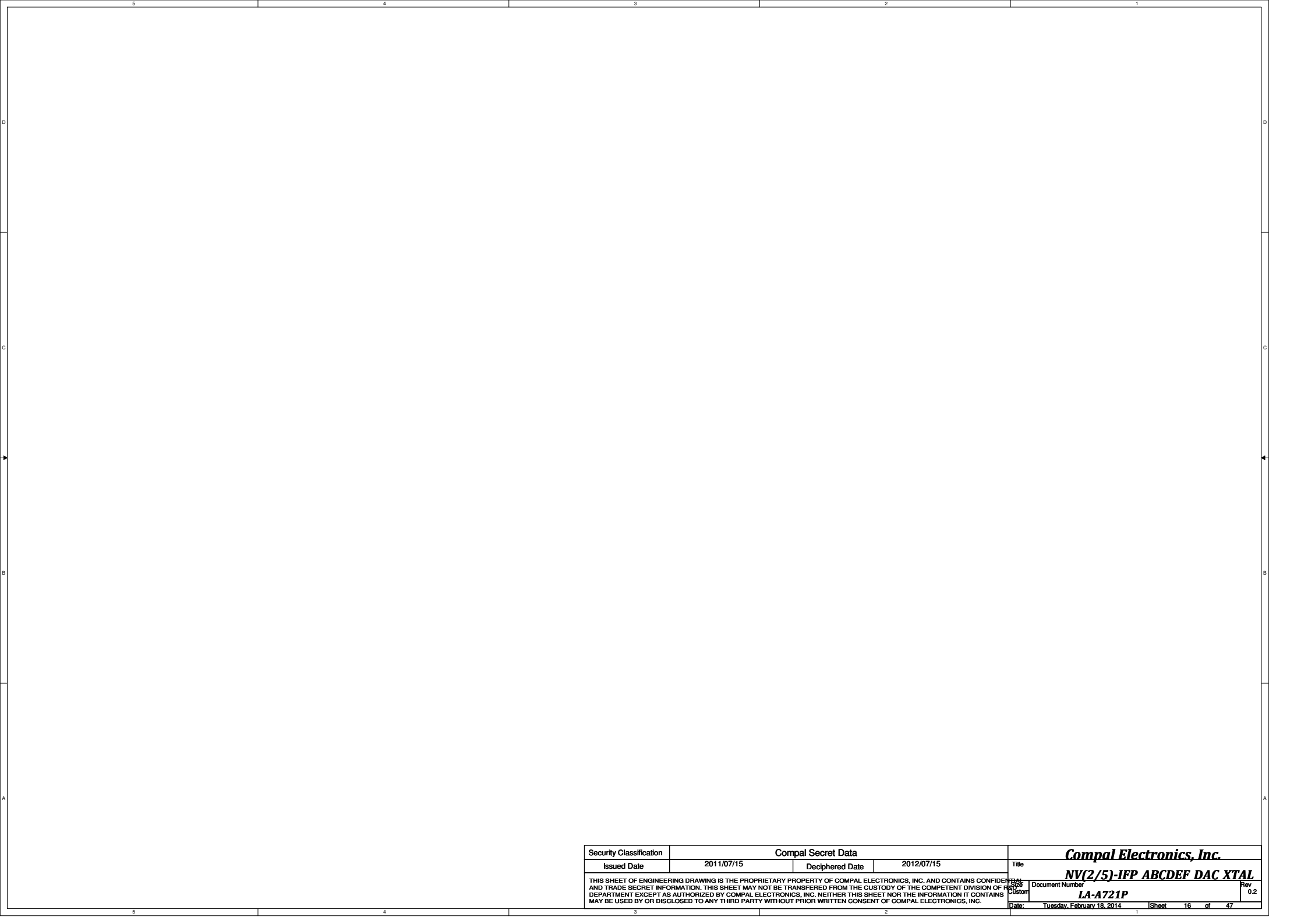


Channel B

<Address: SA0:SA1=10 (A2H)>
DIMM_2 REV H:4mm

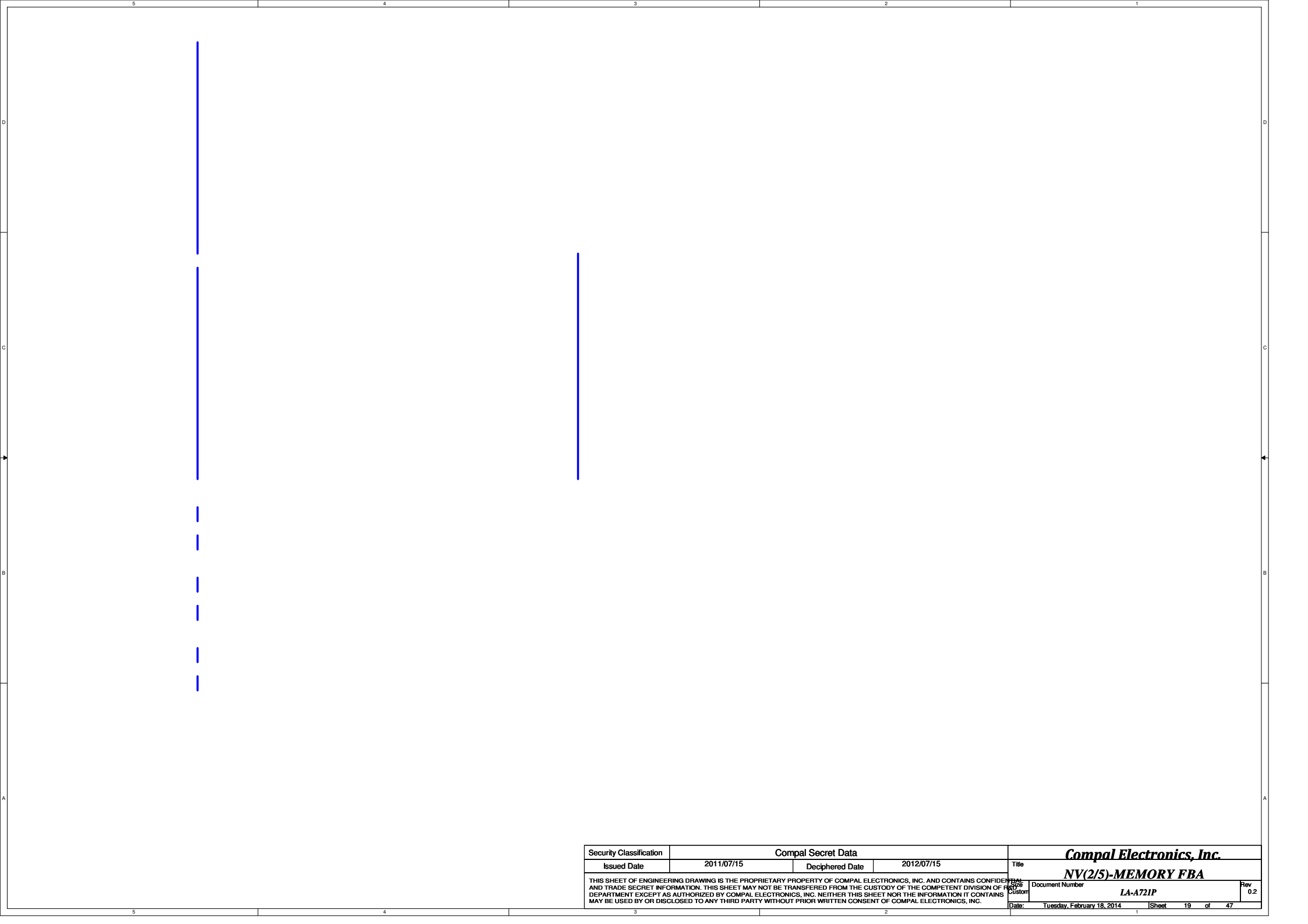


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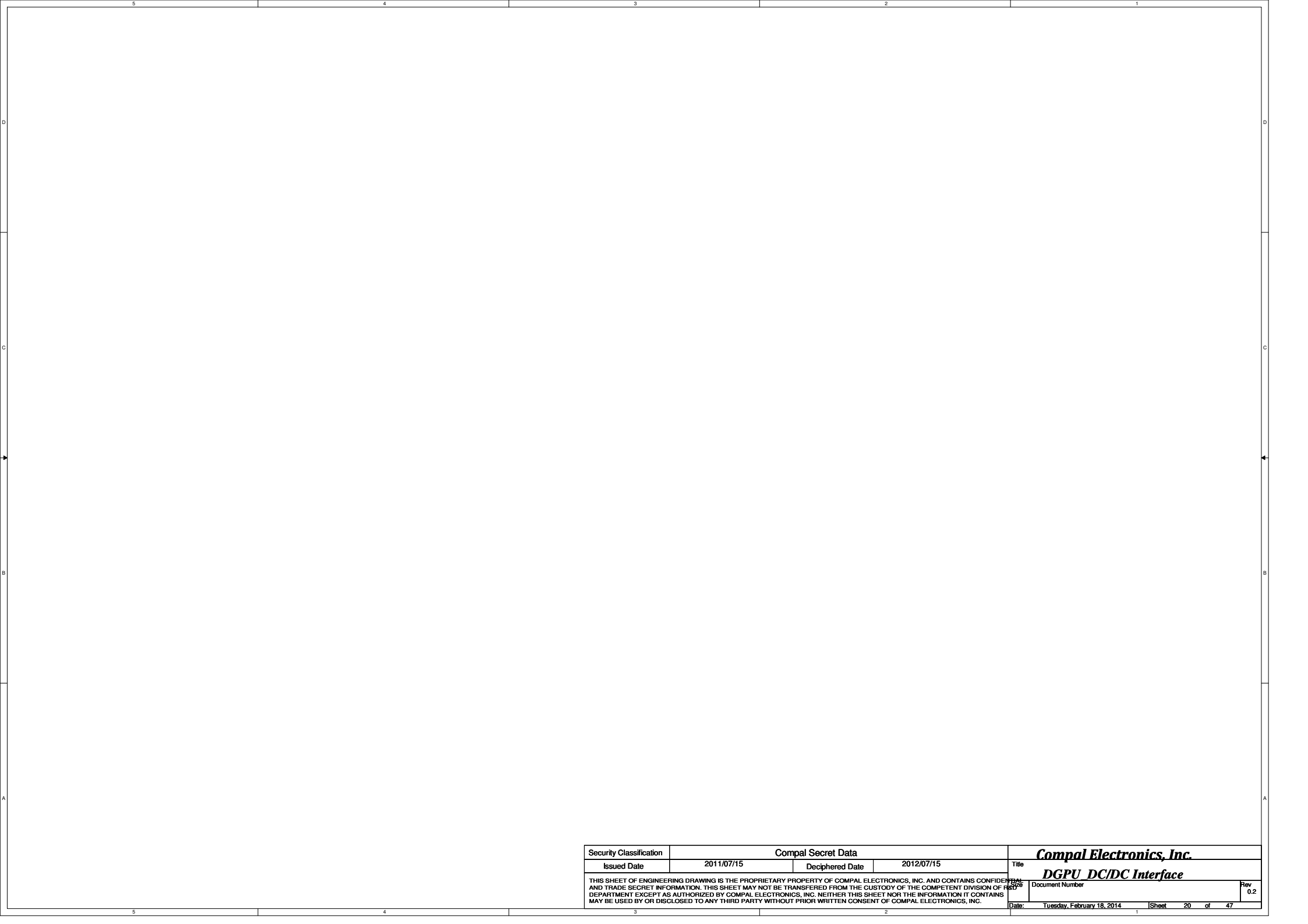


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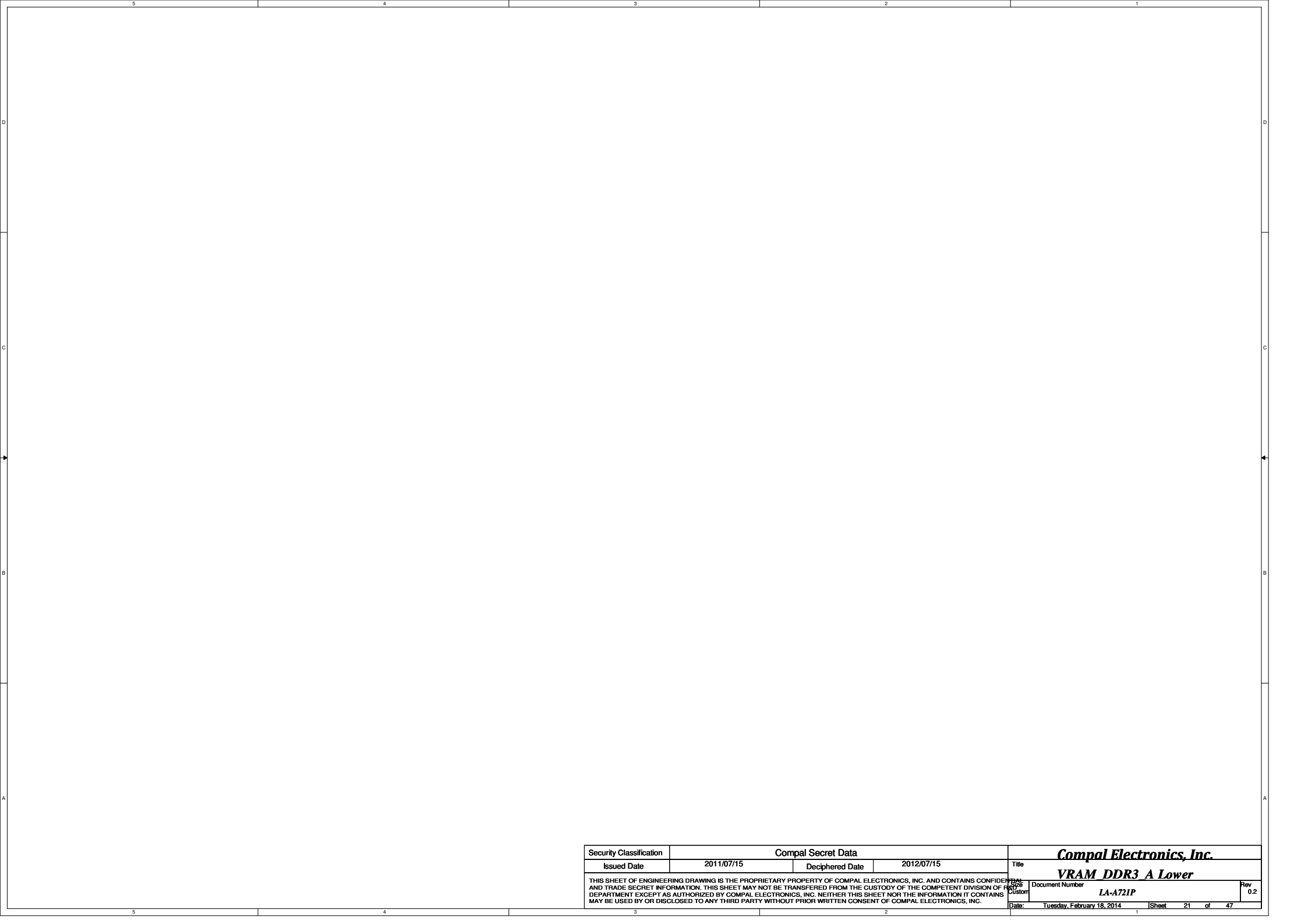
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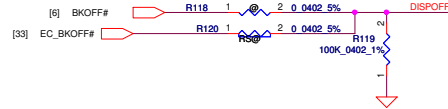
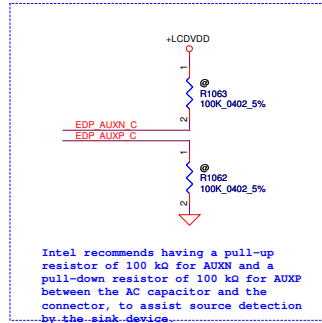
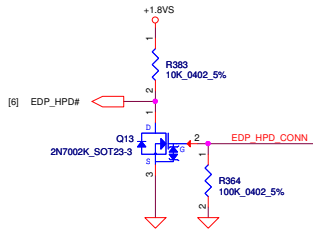
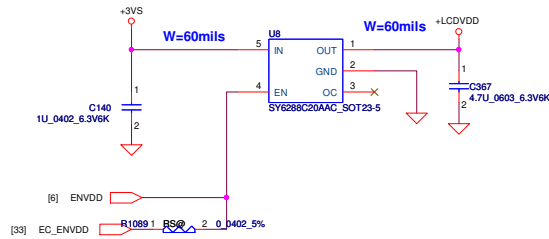
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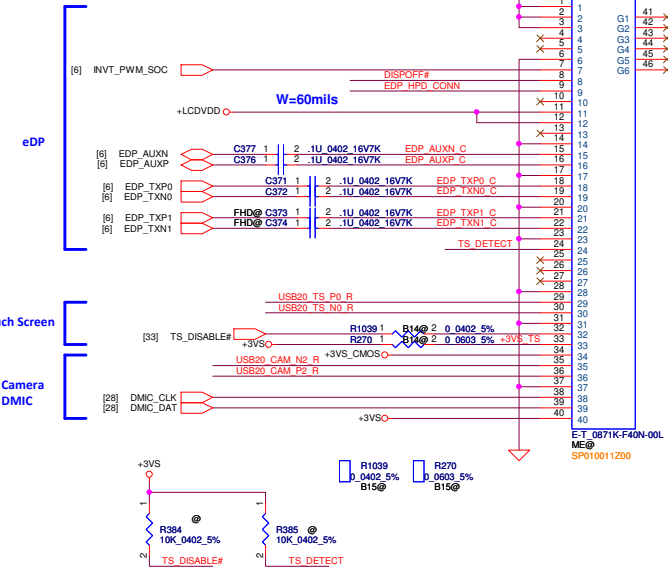
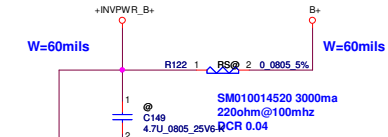
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Issued Date	2011/07/15	Deciphered Date	2012/07/15	VRAM DDR3 A Lower	
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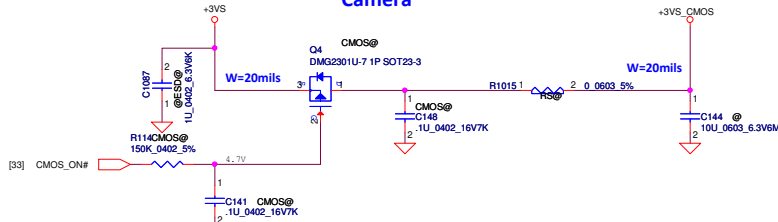
LCD POWER CIRCUIT



LCD/ LED PANEL Conn.

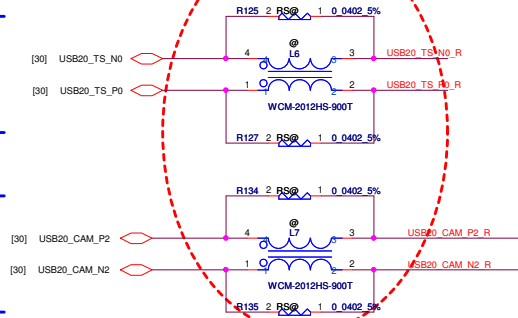


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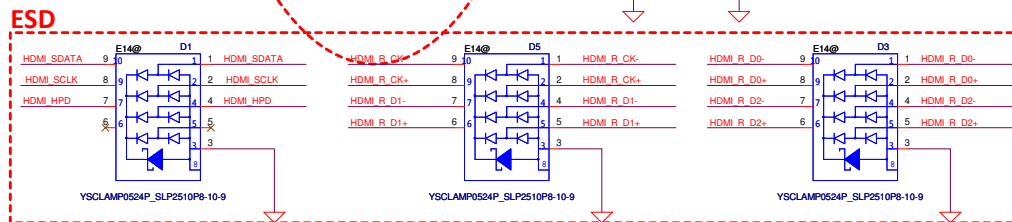
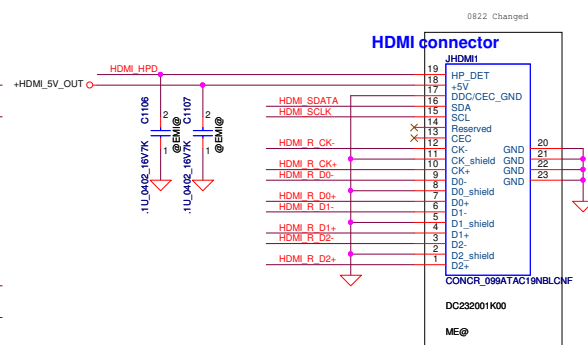
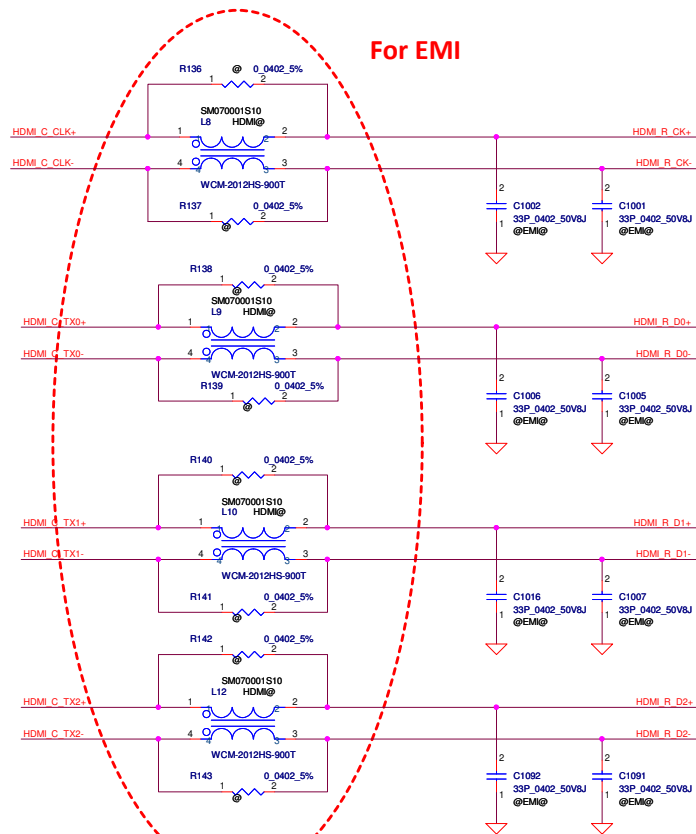
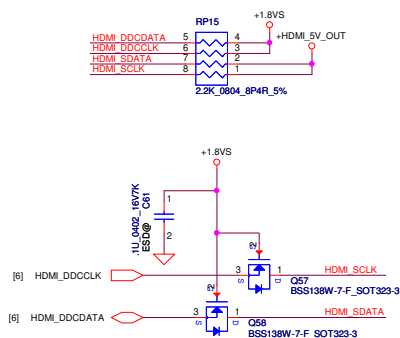
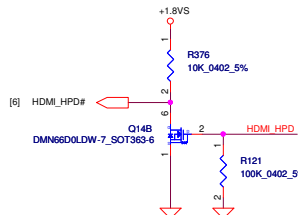
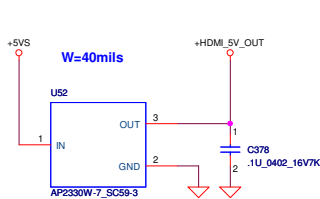
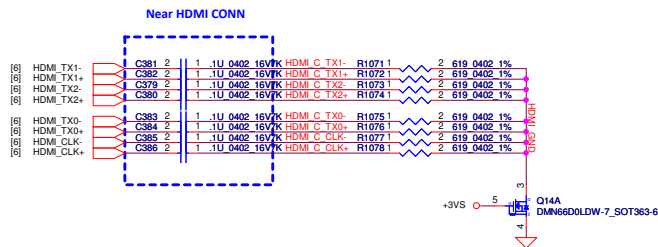


Camera

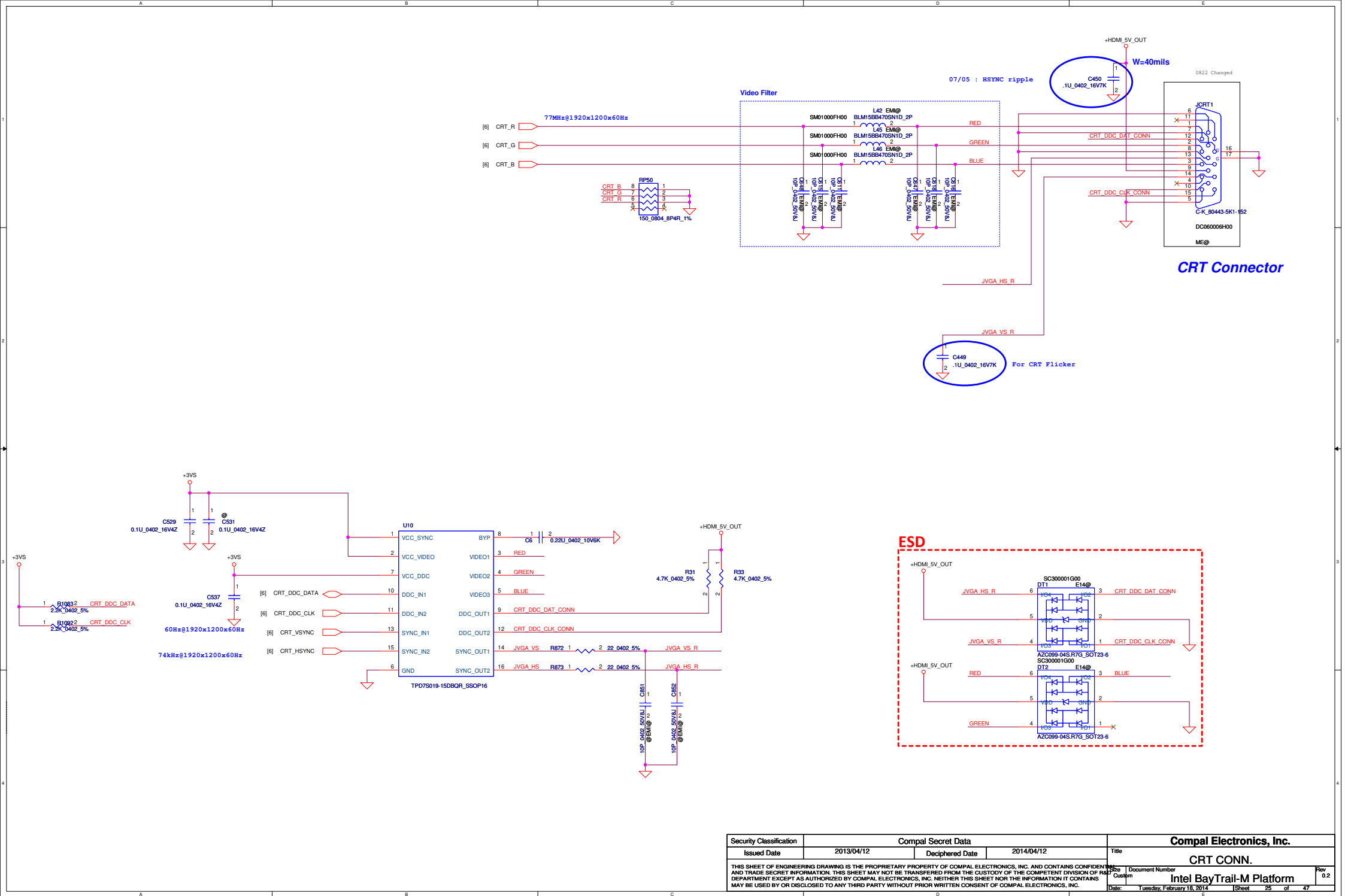
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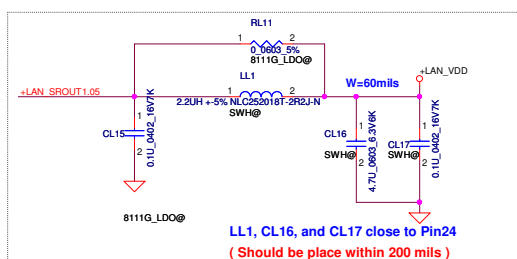
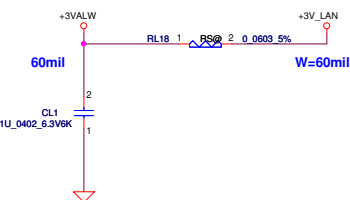


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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title
				eDP CONN.
				Intel BayTrail-M Platform
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Issued Date			2013/04/12	Deciphered Date	2014/04/12	Title
						HDMI CONN.
						Intel BayTrail-M Platform
						Rev 0.2
						Date: Tuesday, February 18, 2014
						Sheet 24 of 47



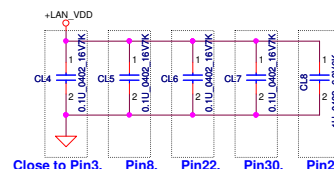
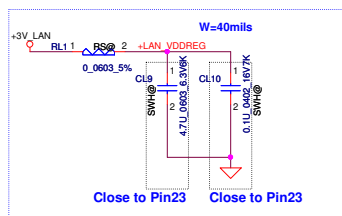
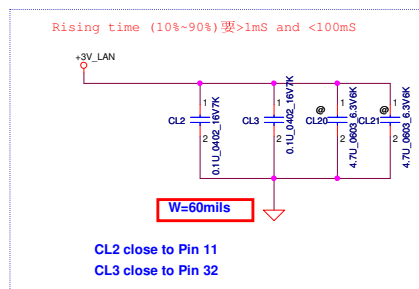


SA00005V700

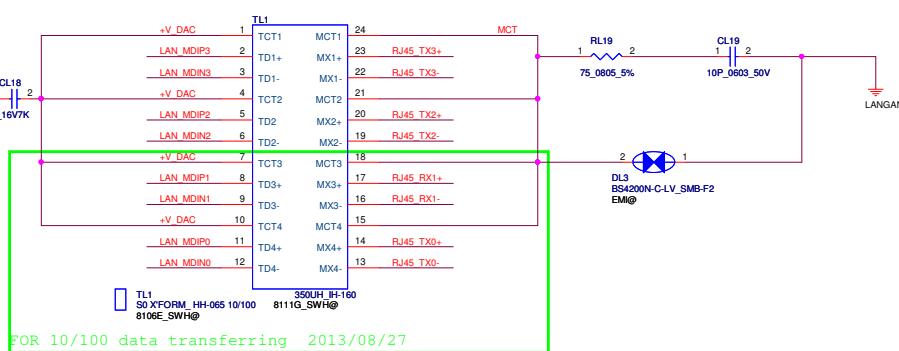
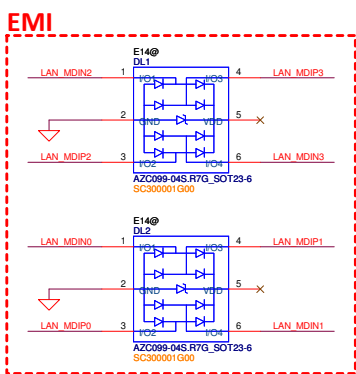
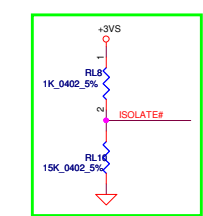
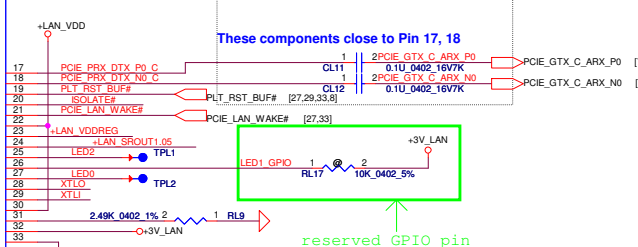
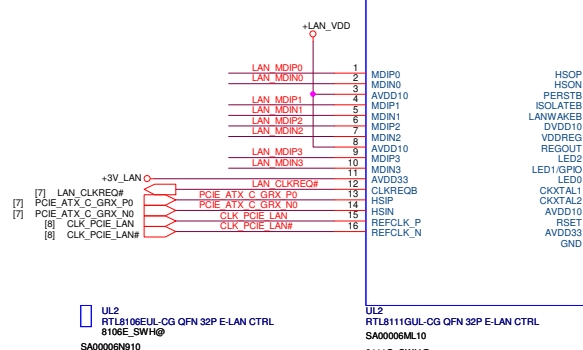
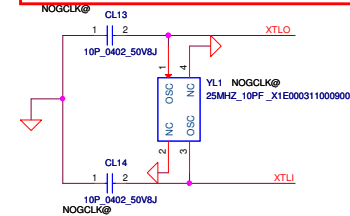
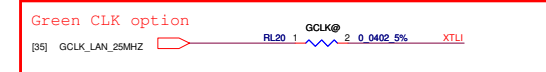
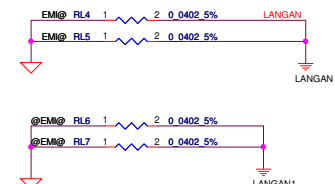
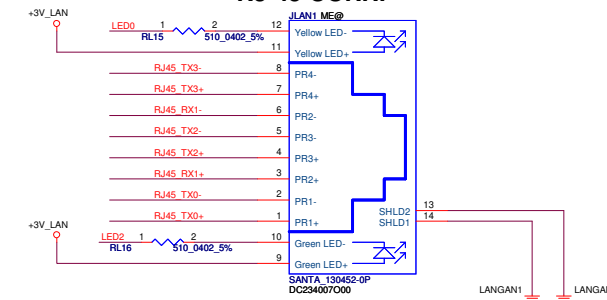
SA000065V00

	1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
RTL8111G	LDO	X	X	X	O	O
RTL8111G	External	X	X	X	X	O
RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
RTL8106E	LDO	X	X	X	X	X

Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.

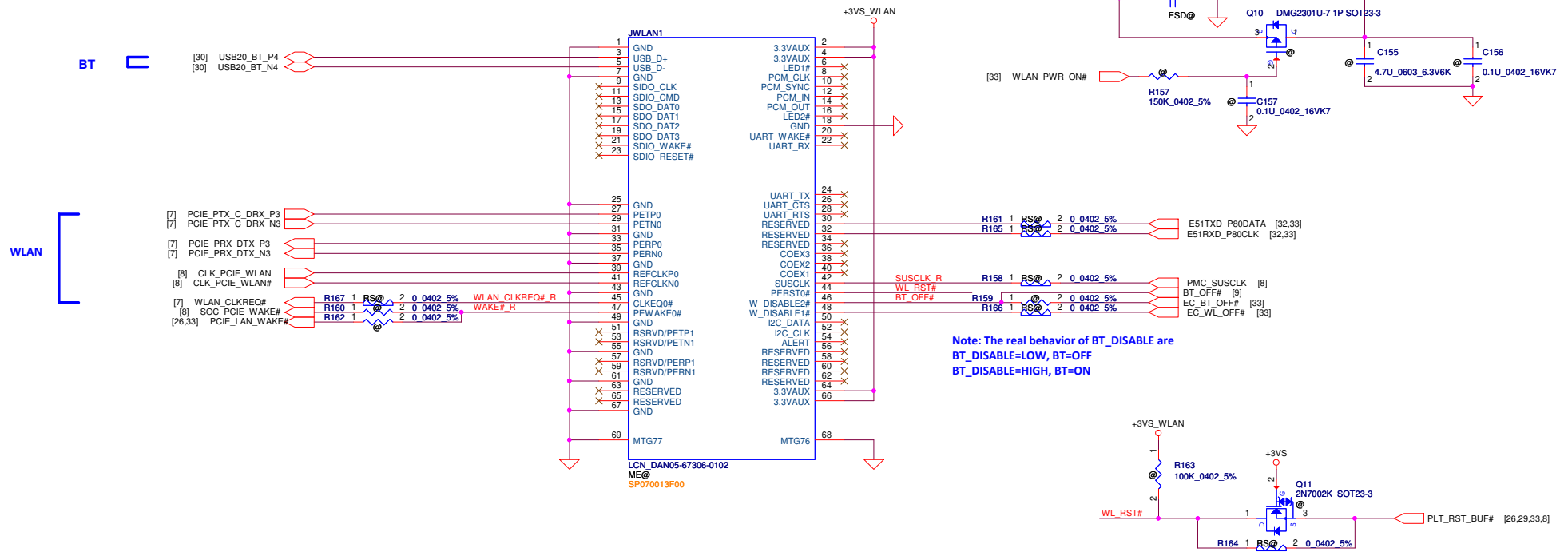


RJ-45 CONN.

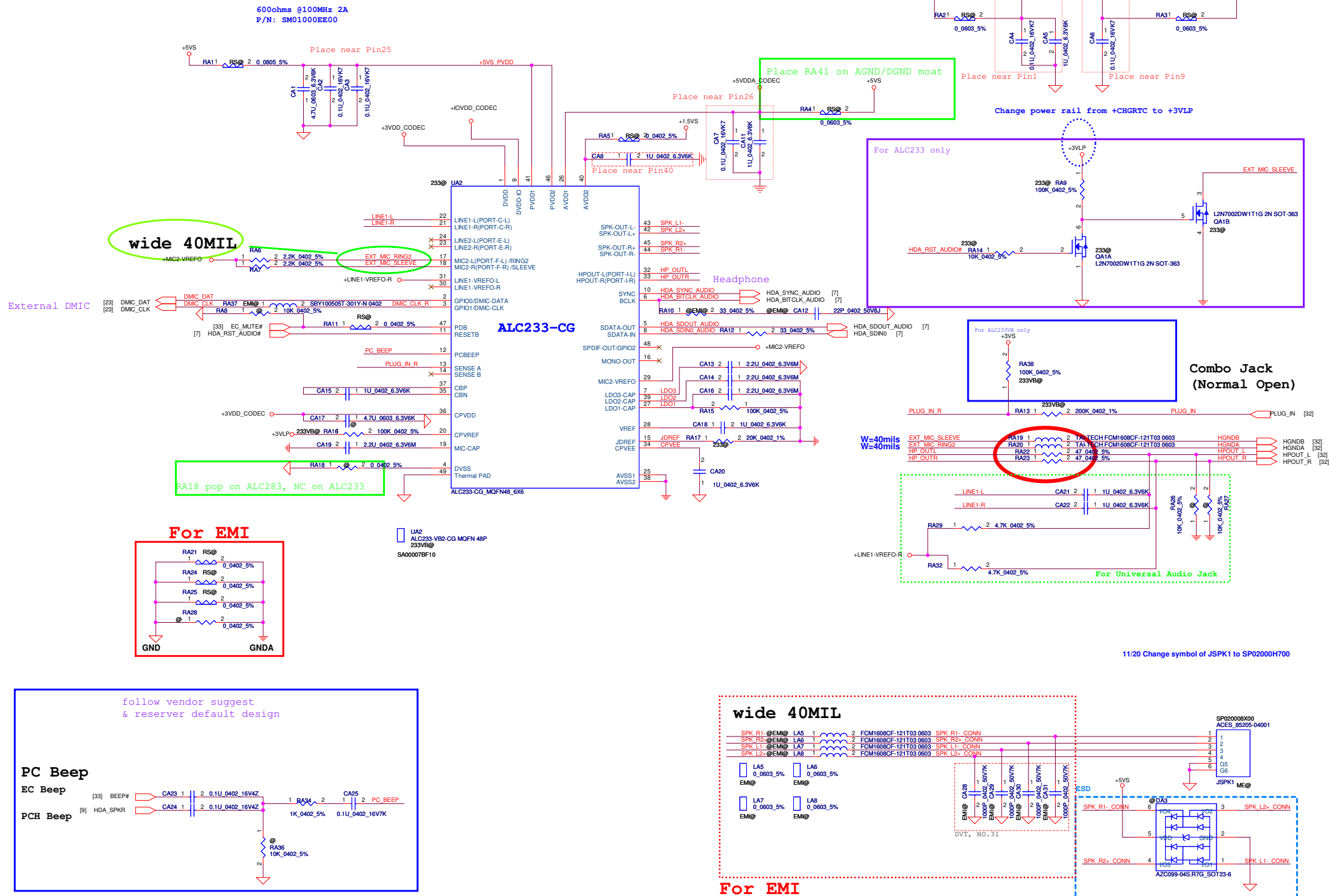


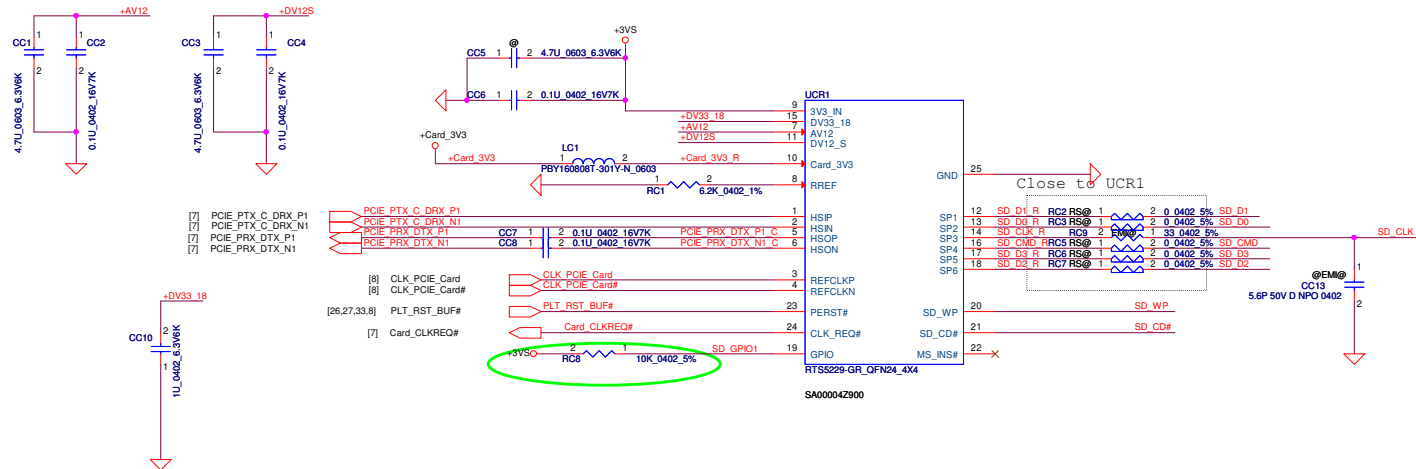
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Document Number
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Date: Tuesday, February 18, 2014				Sheet 26 of 47

NGFF for WLAN / BT(Key E)

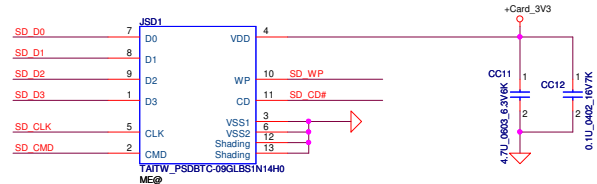


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				Document Number	0.2
				Intel BayTrail-M Platform	
				Date:	Tuesday, February 18, 2014
				Sheet	27 of 47

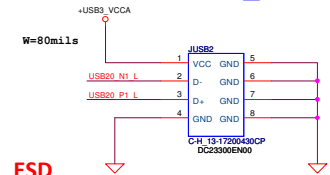
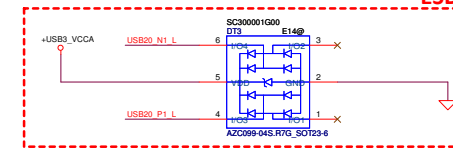
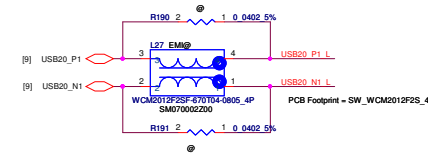
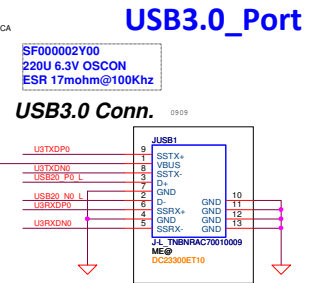
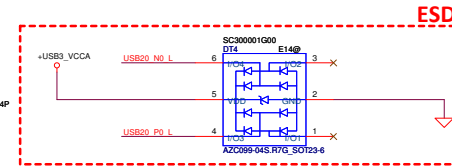
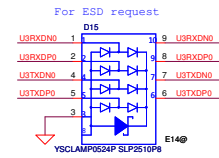
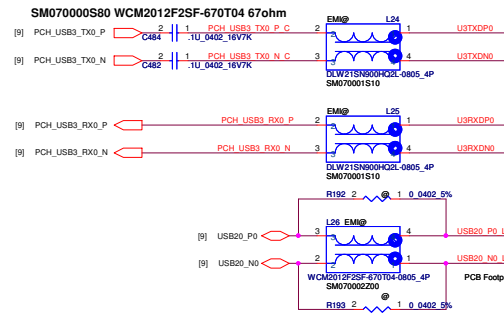
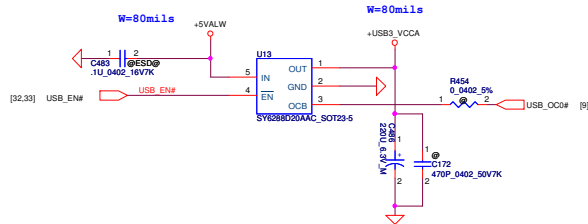




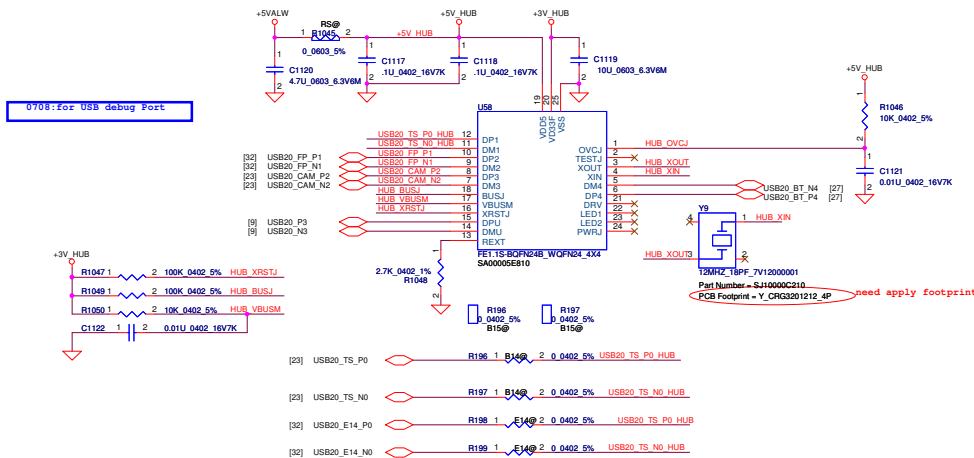
SD/SDXC



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Date:	Tuesday, February 18, 2014	Sheet	29	of	47

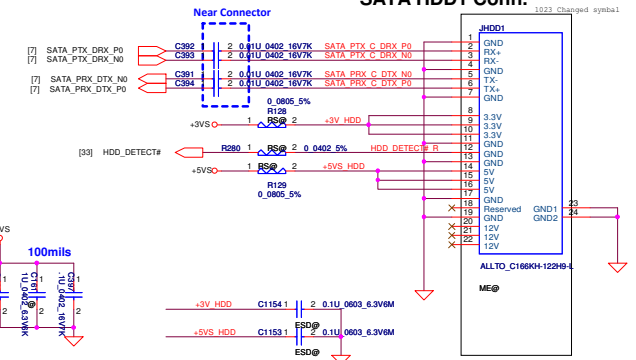


USB2.0 HUB

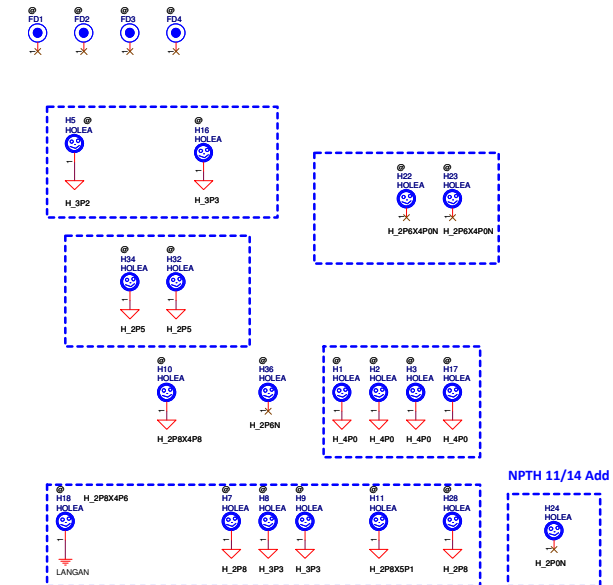
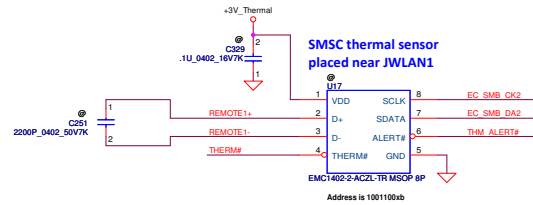
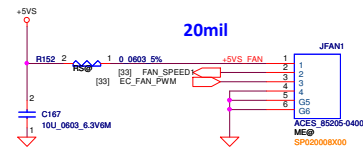


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Issued Date	2013/04/12	Deciphered Date	2014/04/12	USB Conn & Hub FE1.1S	
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				Document Number	0.2
				Intel BayTrail-M Platform	
				Date: Tuesday, February 18, 2014	Sheet 30 of 47

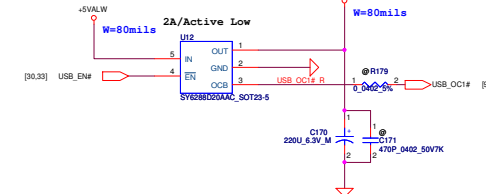
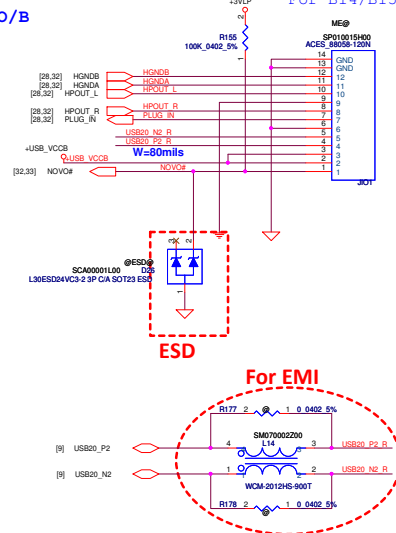
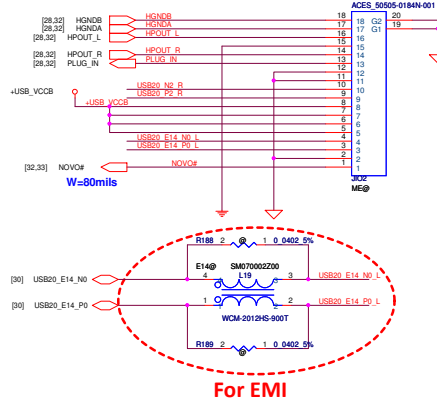
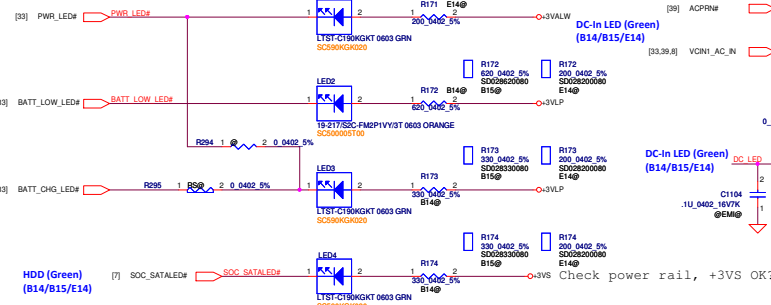
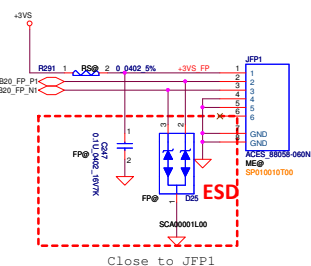
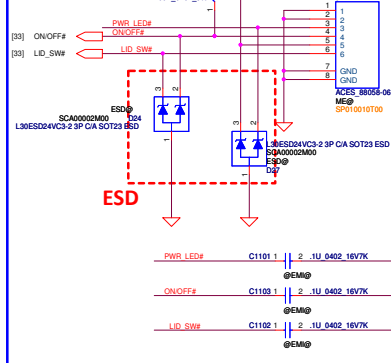
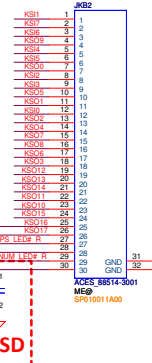
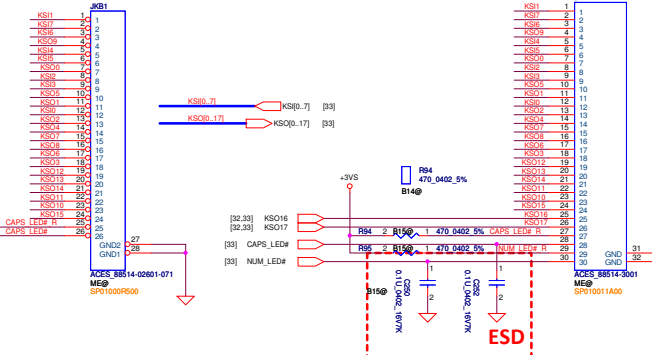
SATA HDD1 Conn.



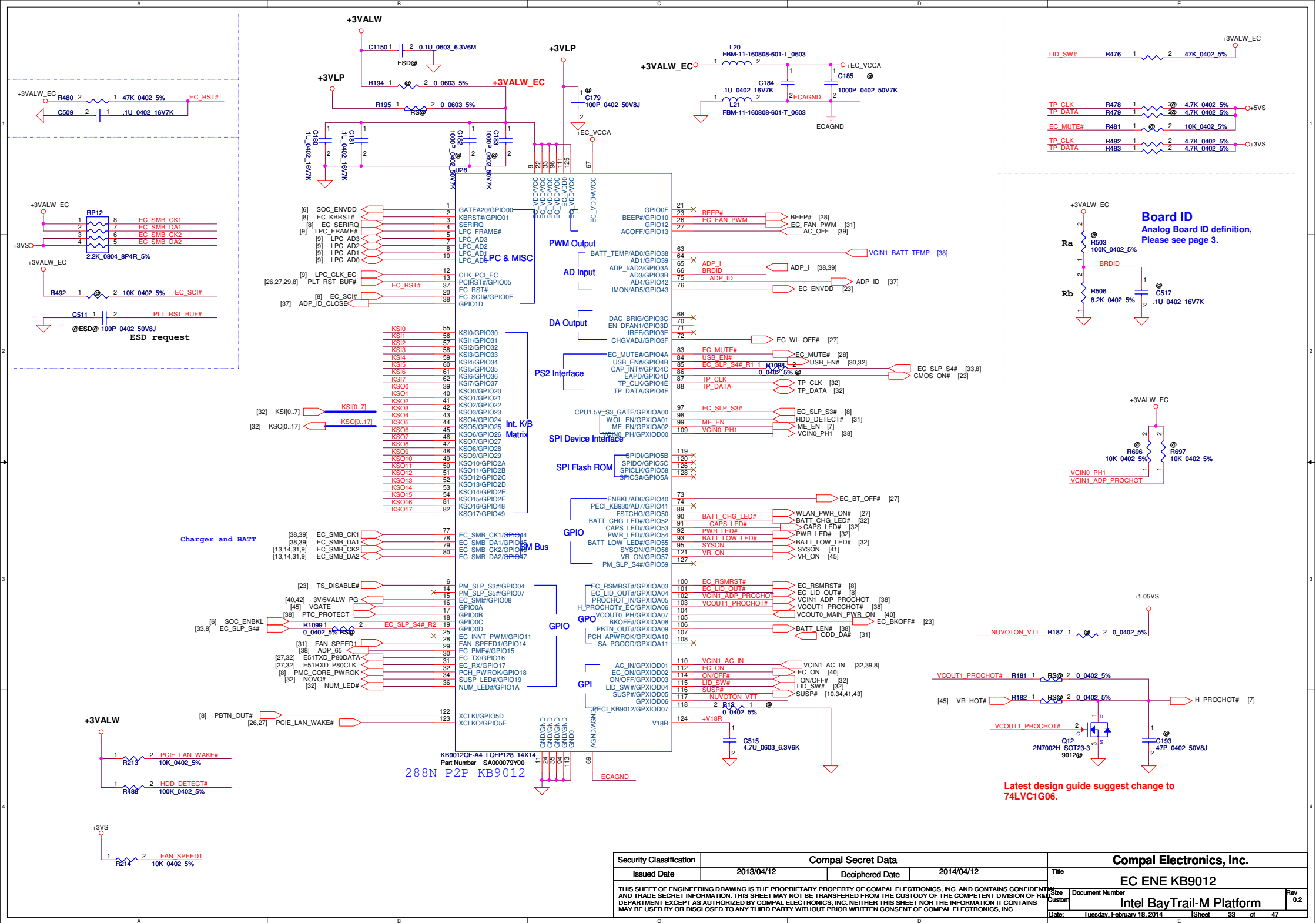
SATA ODD Conn.



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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	HDD/ODD/FAN/Screw Hole
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				Customer	Intel Bay/Trail-M Platform
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Size	Document Number	New 0/1
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				Size		Document Number	
				Custom		Intel BayTrail-M Platform	
				Date:		Tuesday, February 18, 2014	
				Sheet		33 of 47	

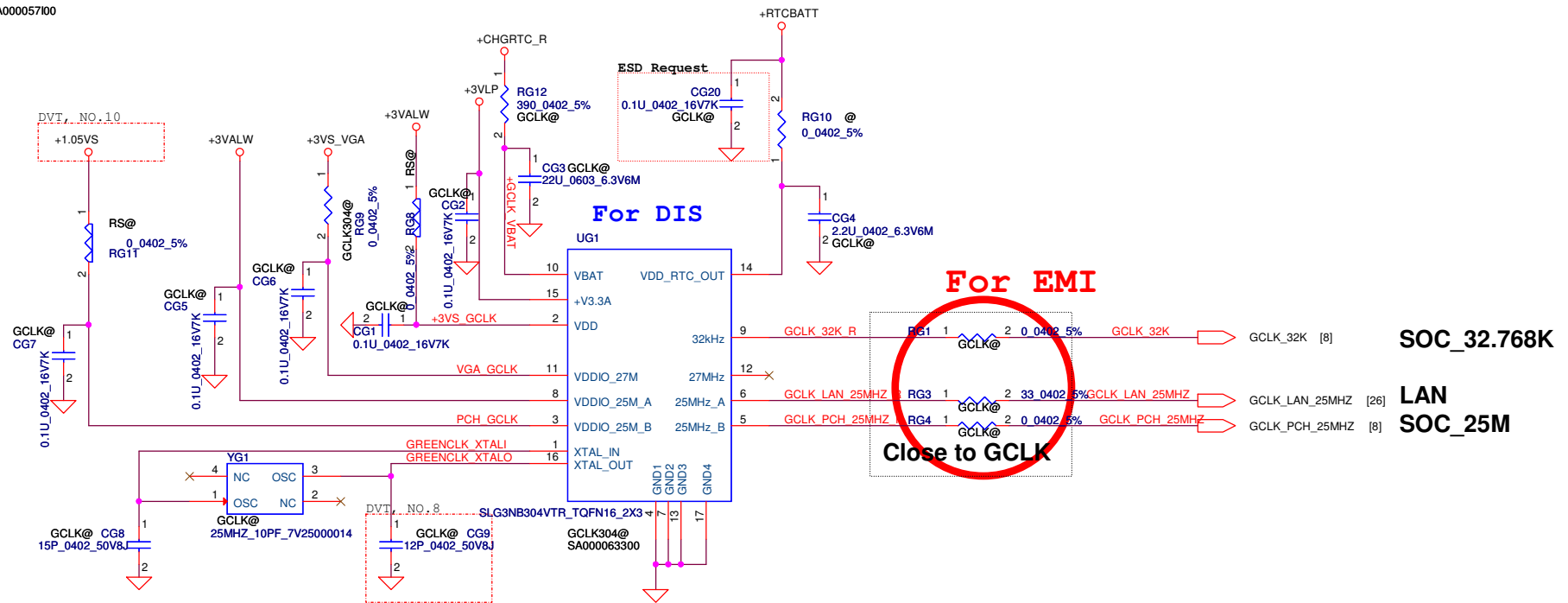
For UMA

UG1 UMA@

SLG3NB244VTR_TQFN16_2X3

SA000057100

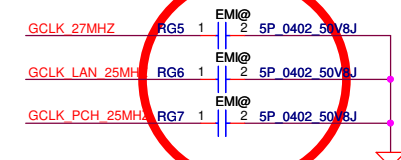
Every power trace need:
W=20mils



For EMI

Close to GCLK

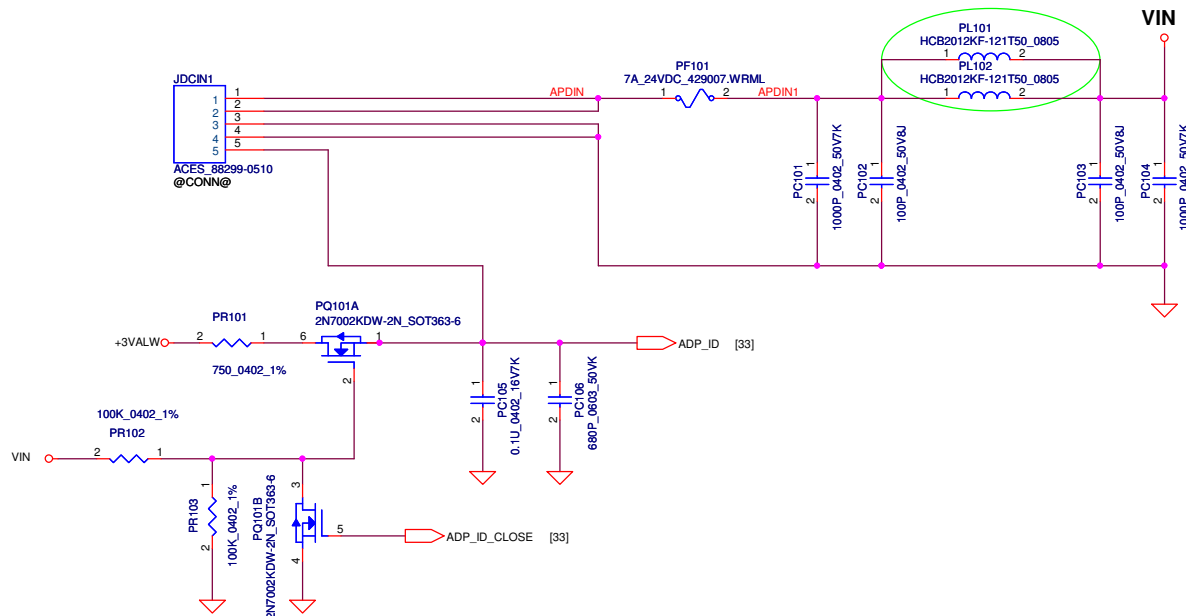
Reserved for Swing Level adjustment
(Close GCLK side)



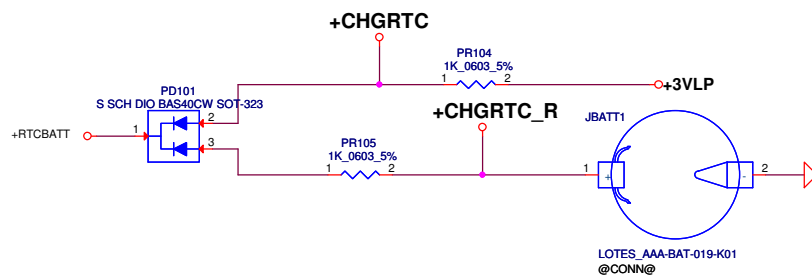
For EMI

Security Classification		Compal Secret Data		Title	
Issued Date	2012/10/11	Deciphered Date	2014/10/11	P35-GCLK	
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Date: Tuesday, February 18, 2014				Sheet 35	of 47

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
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				B	Intel BayTrail-M Platform	0.2
				Date:	Tuesday, February 18, 2014	Sheet 36 of 47

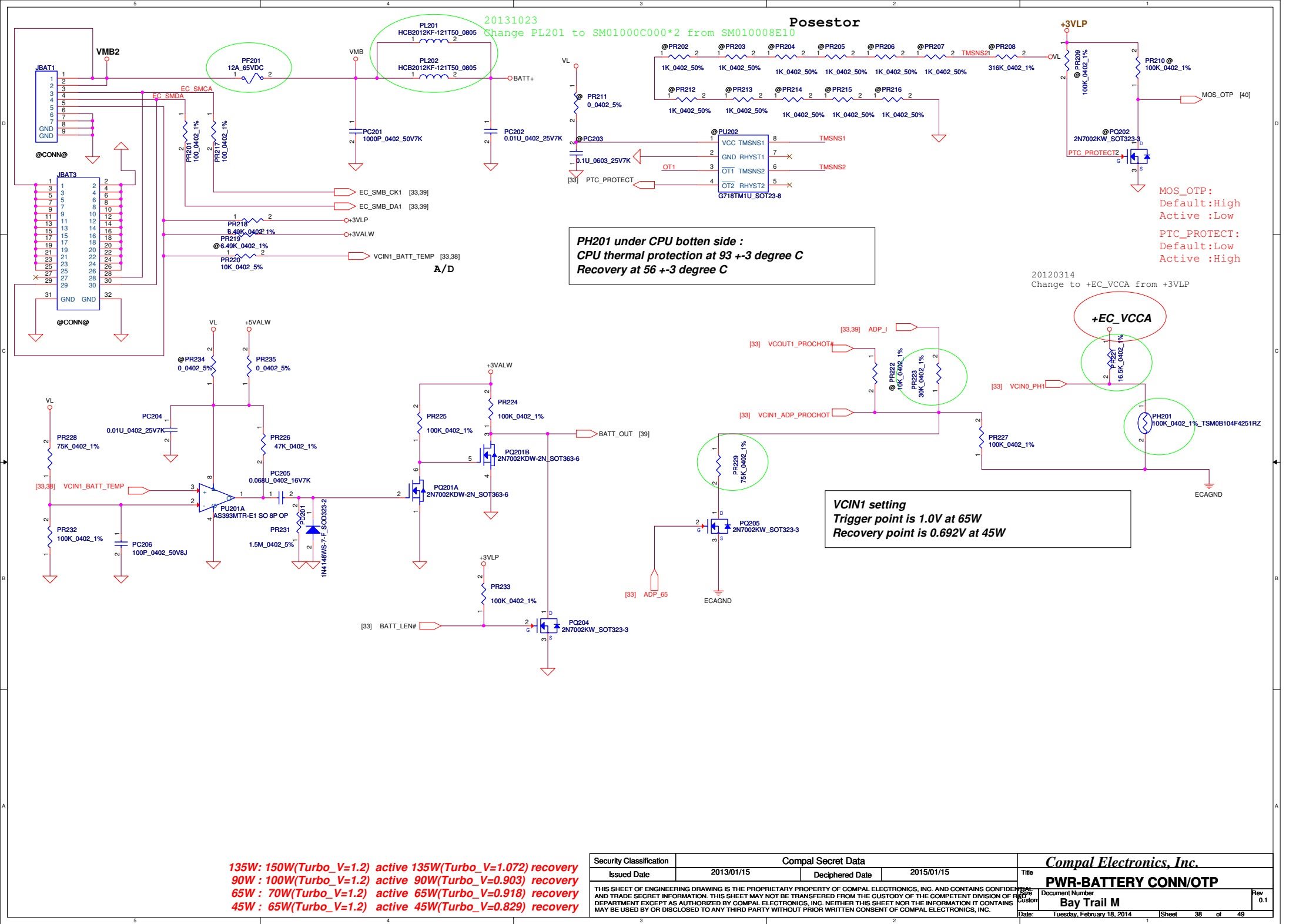


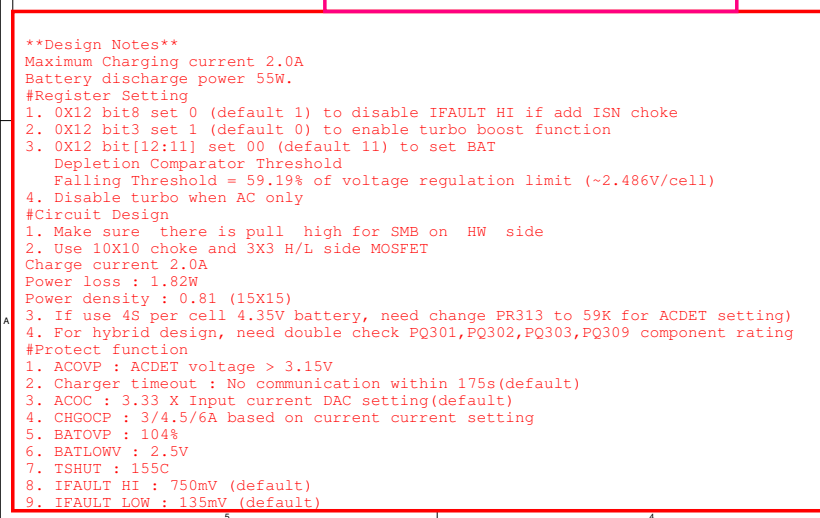
20131023
Change PL101 to SM01000C000*2 from SM010008E10



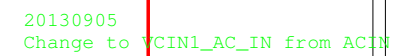
RTC Battery

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/12/01	Deciphered Date	2013/07/10	Title
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				Size Custom
				Bay Trail M
				Rev 0.1
				Date:
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20131028
1.Change PQ314 to SB000009Q80 2M7002 from BJT SB301150200



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Issued Date	2012/07/24		Deciphered Date	2012/07/24		Title	Charger BQ24727		
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							BE BDW	0.1	
						Date:	Tuesday, February 18, 2014	Sheet	39

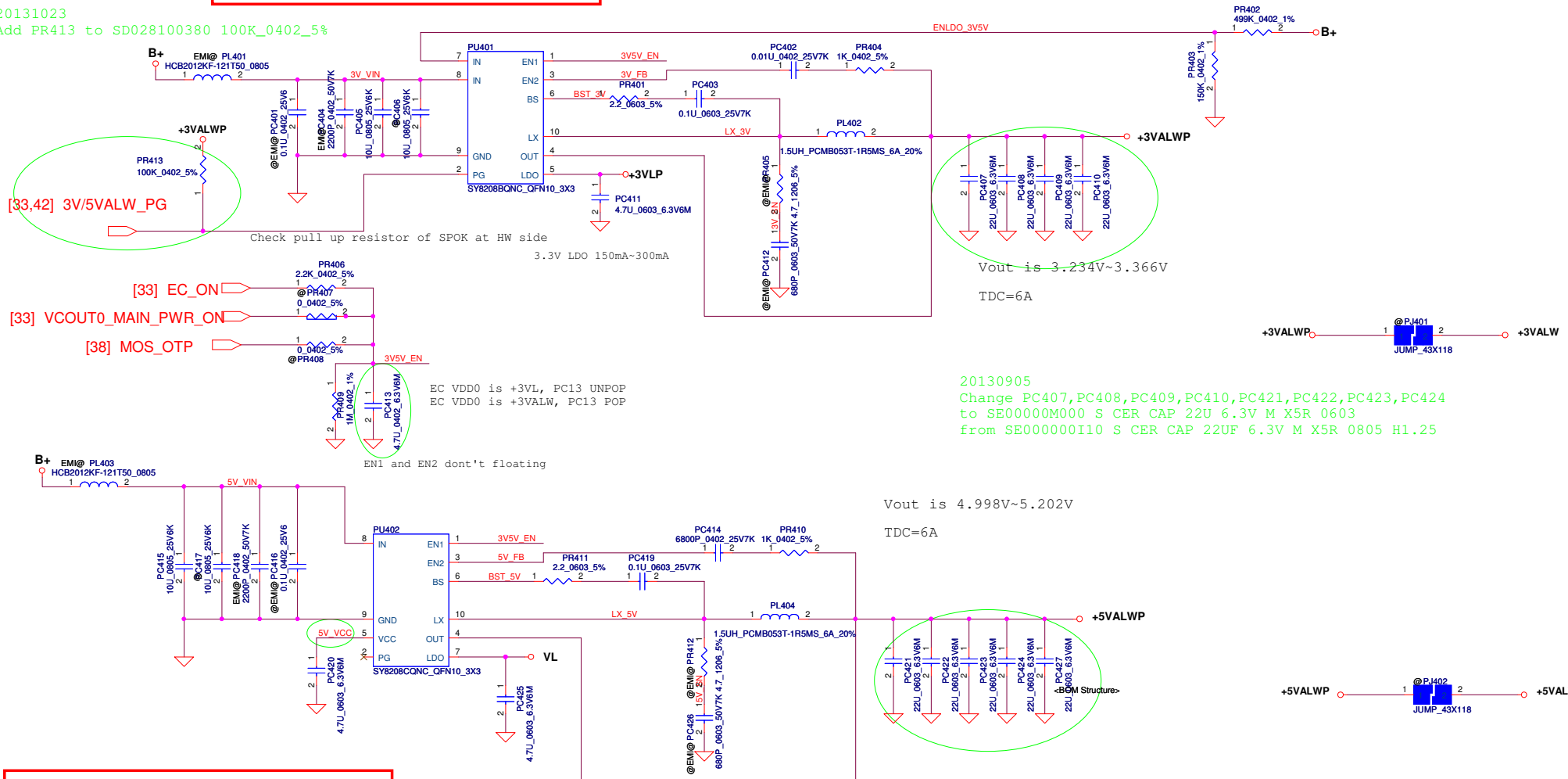
Module model information

SY8208B_V2.mdd

EN1 and EN2 don't floating

20130905
Change to 3V/5VALW_PG from SPOK

20131023
Add PR413 to SD028100380 100K_0402_5%



Module model information

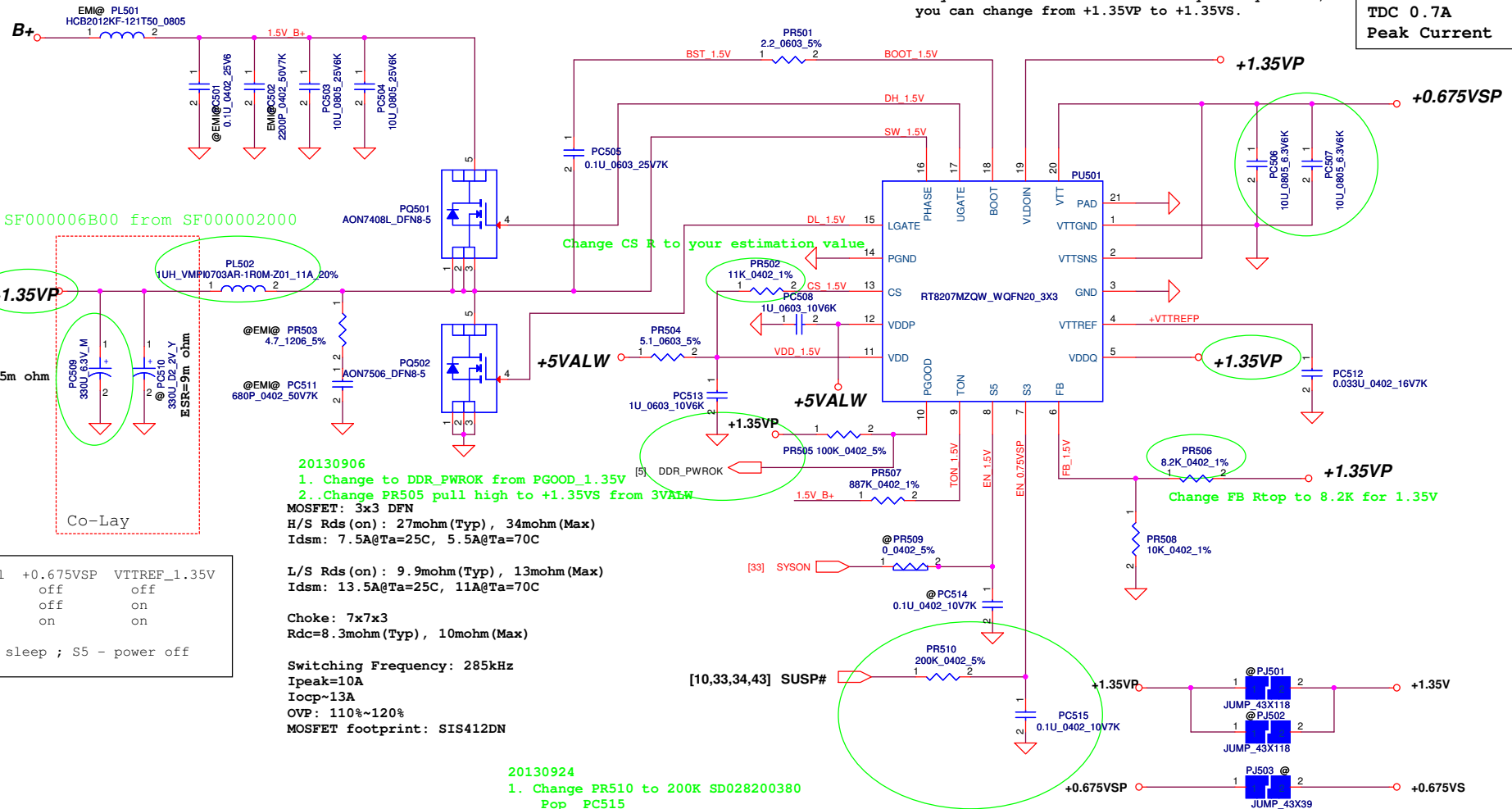
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RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

20130906

1. Change to DDR_PWROK from PGOOD_1.35V
2. Change PR505 pull high to +1.35VS fr

MOSFET: 3x3 DFN

H/S Rds(on): 27mohm(Typ), 34mohm(Max)

Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm (Typ) , 10mohm (Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
MOSFET footprint: SIS412DN

20130924

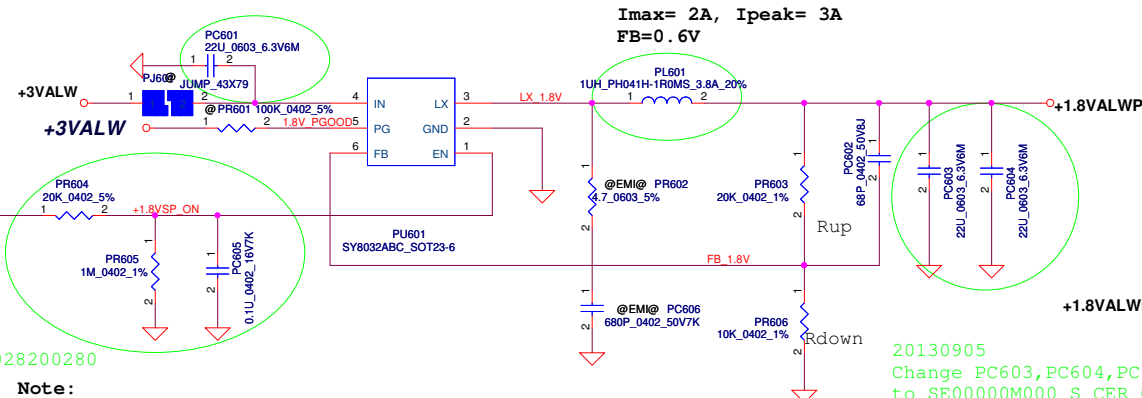
1. Change PR510 to 200K SD028200380
Pop PC515

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Module model information

SY8032_V1.mdd

20130913
Need to change PC702 to 0603 from 0805



20130905
Change to 3V/5VALW_PG from SPOK

20130924
Change PR604 to 20K SD028200280
Pop PC605 to 0.1u

20130905
Change PC603, PC604, PC617, PC618 to SE00000M000 S CER CAP 22U 6.3V M X5R 0603 from SE000000I10 S CER CAP 22UF 6.3V M X5R 0805 H1.25

$V_{out}=0.6V * (1+R_{up}/R_{down})$

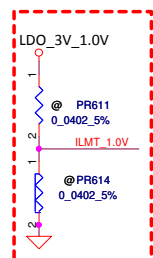
20130924
1. Change PR607 to 10K SD028100280
Pop PC607 to 0.1U_0402_16V7K SE076104K80

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

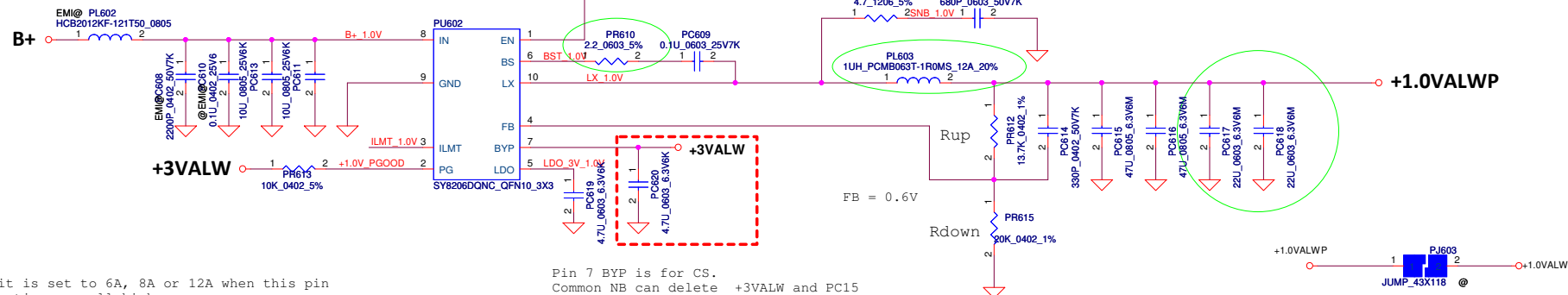
20130905
Change to 3V/5VALW_PG from SPOK

SY8206D_V1.mdd

Module model information



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high



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2013/07/10				Title				PWR-1.8VALW/1.0VALW			
Size				Document Number				Rev			
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Module model information

20130913
Need to change PC702 to 0603 from 0805

Imax= 2A, Ipeak= 3A
FB=0.6V

DIS:SY8003
UMA:SY8032

20130924
Change PR701 to 2.55k 1% SD034255180
Pop PC703 to 0.1u
unpop PR710

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

$$V_{out}=0.6V \cdot (1+R_{up}/R_{down})$$

20130905
Change PR702 to 75K SD034750280
PR705 to 100K SD034100380

20130905
Change PC701,PC703,PC704,PC711
to SE00000M000 S CER CAP 22U 6.3V M X5R 0603
from SE000000I10 S CER CAP 22UF 6.3V M X5R 0805 H1.25

change input cap from 0805 to 0603

2013/5/13
Change PR714 from 100kto 47k
Change PR720 from 47kto 100k

VFB=0.6V
Vout=0.6V * (1+Rup/Rdown)
Vout=1.011V

Ultra Low Dropout 0.23V(typical) at 3A Output Current

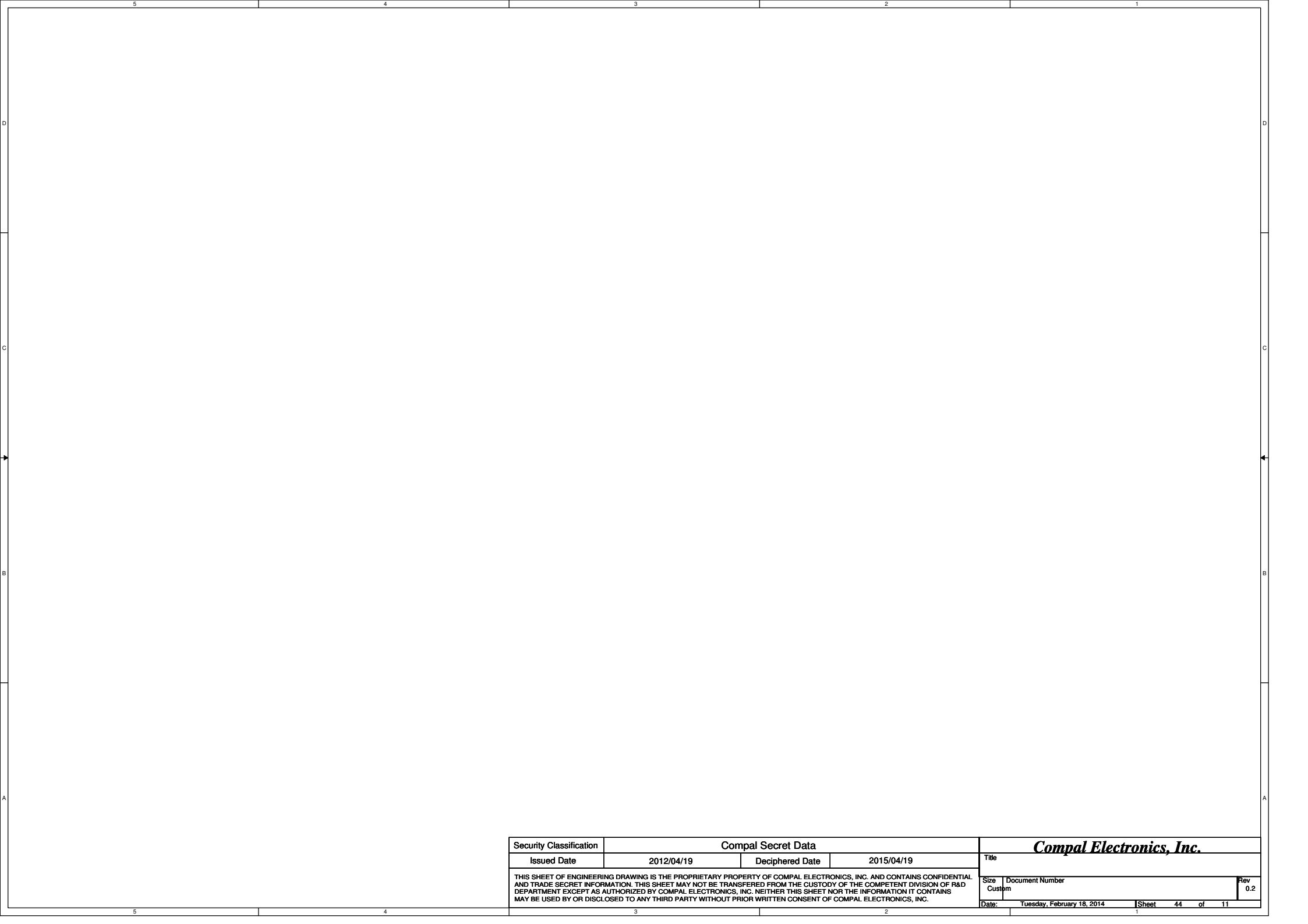
2013/5/13
Change PR716 from 47kto 100k

20130924
Change PR706 to 51K SD028510280
Pop PC710 0.15U_0402_10V6K SE00000H300
unpop PR708

$$V_{out}=0.8V \cdot (1+R_{up}/R_{down})$$

$$V_{out}=1.512V$$

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Power module of ISL95833 VR
for 4.5W processor

PR15 and PR27
27.4K ohm for 100 degree
61.9K ohm for 110 degree

Alert assert
threshold: 100C

Close GFX choke

Close GFX L/S MOS

+3VALW

+5VALW

VR_Hot# assert
threshold: 100C

Close CPU L/S MOS

Close CPU choke

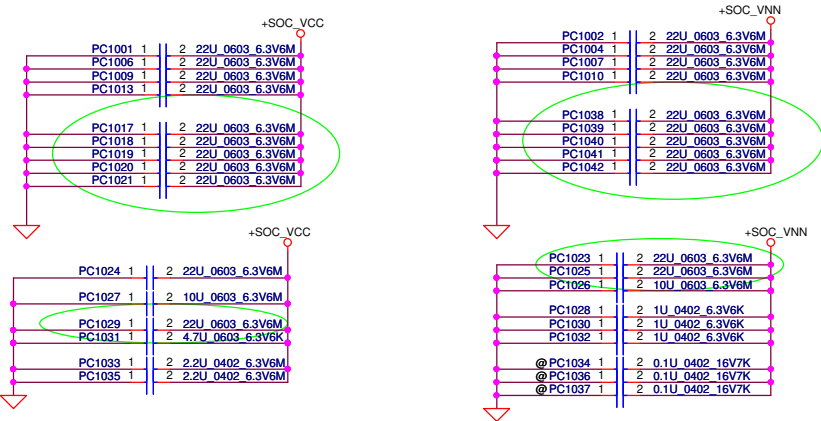
SOC_VNN OCP is around 21A
SOC_VCC OCP is around 19A

20130905
1. Del PC940 33U_25V_M
2. Change PC939 to 68U_25V_M R0.36 SF000000W00
From 33U_25V_M SF000005200

0.22uH DCR= 0.97+-5% m ohm, Idc-Isat= 25-34A

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22uF 0805 size change to 0603



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