2-Phase Synchronous-Rectified Buck Controller for Mobile GPU Power

General Description

The uP1658P is a 2/1-phase synchronous-rectified buck controller specifically designed to work with 4.5V ~ 26V input voltage and deliver high quality output voltage for high-performance graphic processor power.

The uP1658P adopts proprietary RCOT™ technology, providing flexible selection of output LC filter and excellent transient response to load and line change.

The uP1658P supports NVIDIA Open Voltage Regulator-2 with PWMVID feature. The PWMVID input is buffered and filtered to generate accurate reference voltage, and the output voltage is precisely regulated to the reference input.

The uP1658P uses MOSFET $R_{DS(ON)}$ current sensing for channel current balance. The uP1658P also implements a multi-function pin (OCS/CB) for OCP threshold selection and current balance adjustment.

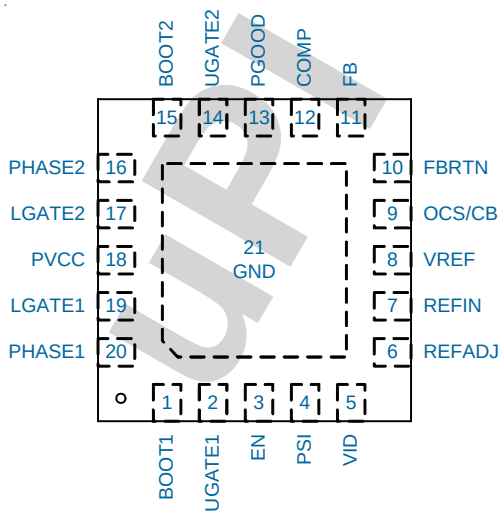
Other features include power saving control input, and a delayed power good output. This part is available in WQFN3x3 - 20L package.

Ordering Information

Order Number	Package	Top Marking
uP1658PQKF	WQFN3x3-20L	uP1658P

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



Features

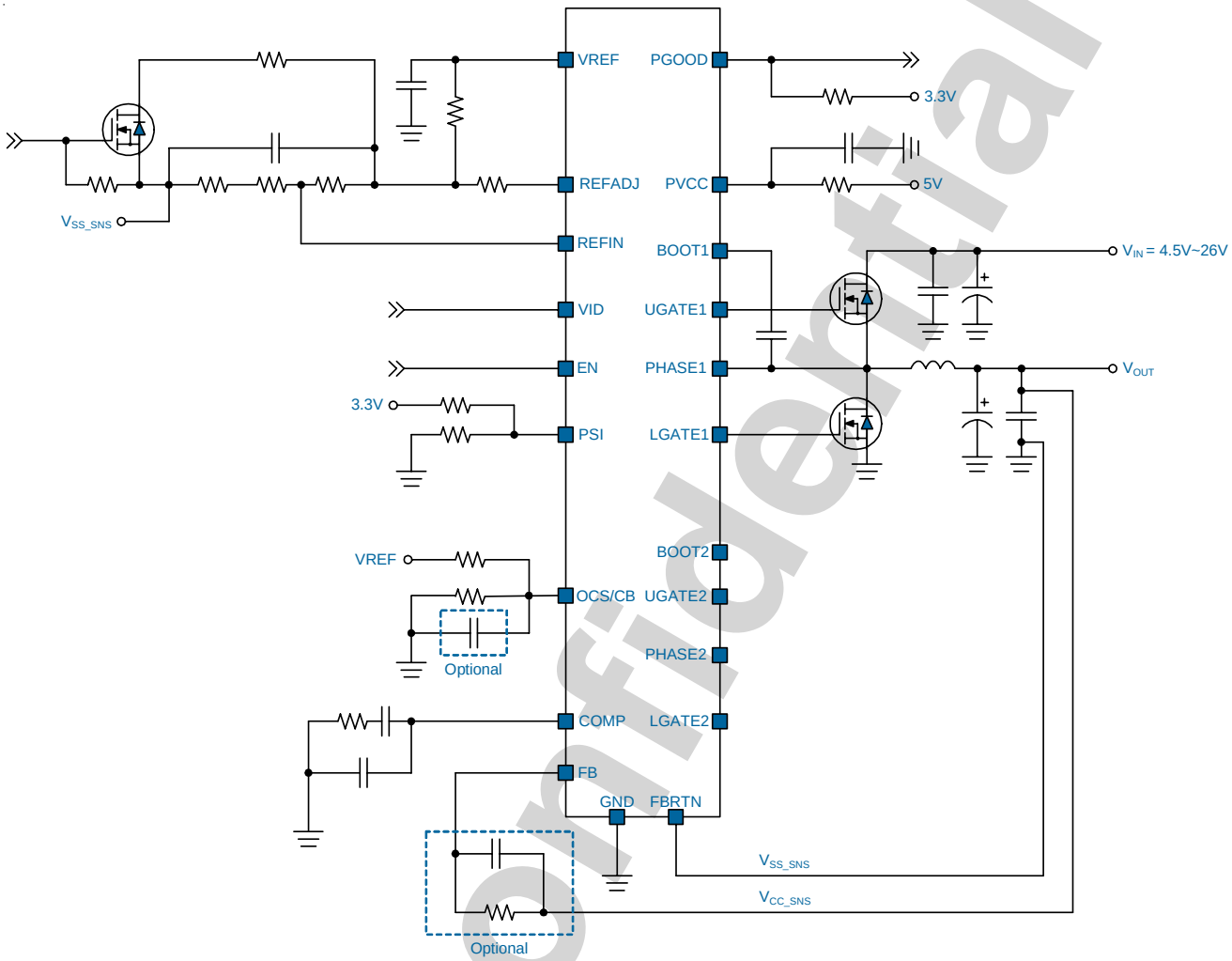
- Support NVIDIA's Open VReg Type-2 PWMVID Technology
- Wide Input Voltage Range 4.5V ~ 26V
- Robust Constant On-Time Control
- 2/1 Phase Operation
- Two Integrated MOSFET Drivers with Shoot-Through Protection and Internal Bootstrap Switch
- Adjustable Current Balancing by $R_{DS(ON)}$ Current Sensing
- Multi-Function Pin (OCS/CB) for OCP Threshold Selection and Current Balance Adjustment
- Typical 300kHz Operation Frequency
- External Compensation
- Support NVIDIA PWMVID Function
- Dynamic Output Voltage Adjustment
- Power Good Indication
- Over Voltage Protection
- Under Voltage Protection
- Over Temperature Protection
- RoHS Compliant and Halogen Free

Applications

- Middle-High End GPU Core Power
- High End Desktop PC Memory Core Power
- Low Output Voltage, High Power Density DC-DC Converters
- Voltage Regulator Modules

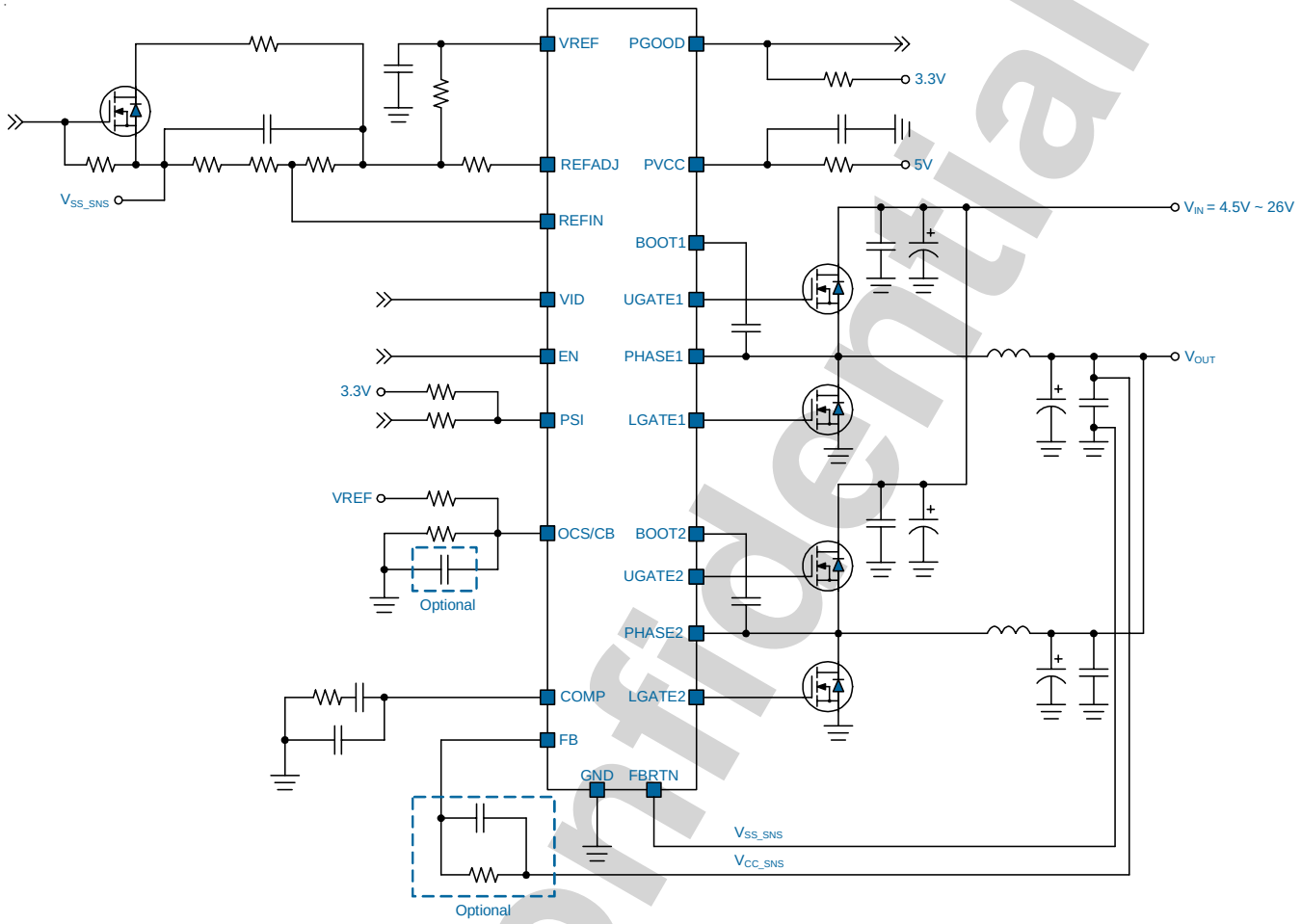
Typical Application Circuit

1-Phase Mode



Typical Application Circuit

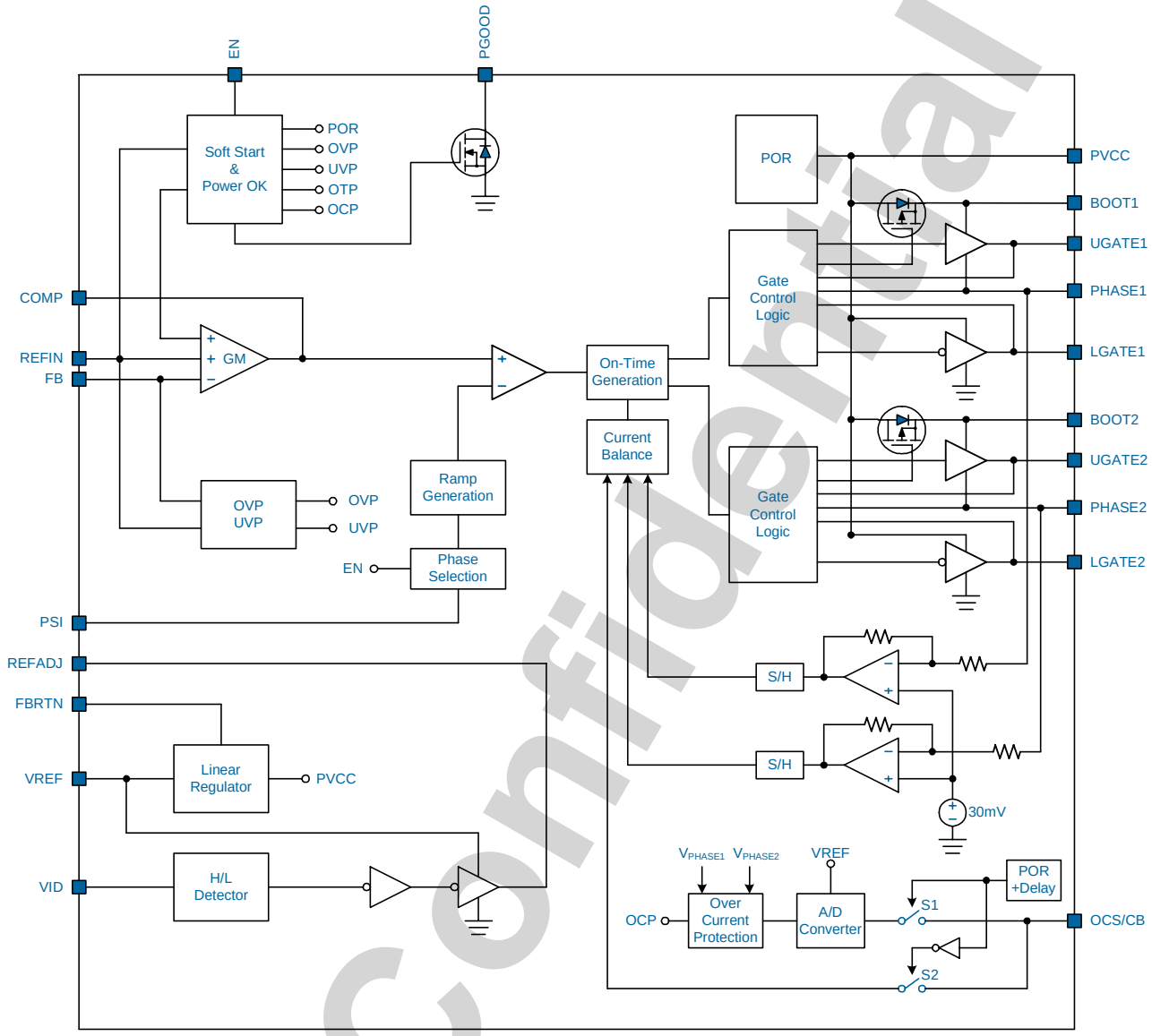
2-Phase Mode



Functional Pin Description

Name	Pin Function
BOOT1	**BOOT for Phase 1.** Connect a capacitor from this pin to PHASE1 to form a bootstrap circuit for upper gate driver of the phase 1.
UGATE1	**Upper Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 upper MOSFET.
PSI	**Power Saving Input.** An input pin receiving power saving control signal from GPU.
VID	**VID.** PWMVID input pin.
REFADJ	**Reference Adjustment.** PWMVID output pin. Connect this pin with an RC integrator to generate REFIN voltage.
REFIN	**Reference Input.** Connect this pin to an external reference voltage through a resistor or connect to the output of the REFADJ circuit. Pulling low this pin below REFIN disable threshold will shutdown the uP1658P.
VREF	**Reference Voltage.** 2V LDO voltage output pin. Connect an at least 1uF decoupling capacitor between this pin and GND.
OCS/CB	**OCP Setting and Current Balance.** Connect a resistive voltage divider from VREF to GND to set OCP threshold and adjust current balance.
FBRTN	**Return for the Reference Circuit.** Connect this pin to the ground point where output voltage is to be regulated.
FB	**Feedback Pin.** This pin is the inverting input of the error amplifier.
COMP	**Compensation Output.** This pin is the output of the error amplifier.
EN	**Enable.** Chip enable.
PGOOD	**Power Good Indication.** Connect this pin to a voltage source with a pull-up resistor. Open-drain structure.
UGATE2	**Upper Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 upper MOSFET.
BOOT2	**BOOT for Phase 2.** Connect a capacitor from this pin to PHASE2 to form a bootstrap circuit for upper gate driver of the phase 2.
PHASE2	**Phase Pin for Phase 2.** This pin is the return path of upper gate driver for phase 2. Connect a capacitor from this pin to BOOT2 to form a bootstrap circuit for upper gate driver of the phase 2.
LGATE2	**Lower Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 lower MOSFET.
PVCC	**Supply Input for the IC.** Voltage power supply of the IC. Connect this pin to a 5V supply and decouple using at least a 1uF ceramic capacitor.
LGATE1	**Lower Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 lower MOSFET.
PHASE1	**Phase Pin for Phase 1.** This pin is the return path of upper gate driver for phase 1. Connect a capacitor from this pin to BOOT1 to form a bootstrap circuit for upper gate driver of the phase 1.
Exposed Pad	**Ground.** Tie this pin to ground island/plane through the lowest impedance connection available.

Functional Block Diagram



Functional Description

The uP1658P is a 2/1-phase synchronous-rectified buck controller specifically designed to work with 4.5V ~ 26V input voltage and deliver high quality output voltage for high-performance graphic processor power.

The uP1658P adopts proprietary RCOT™ technology, providing flexible selection of output LC filter and excellent transient response to load and line change.

The uP1658P supports NVIDIA Open Voltage Regulator-2 with PWMVID feature. The PWMVID input is buffered and filtered to generate accurate reference voltage, and the output voltage is precisely regulated to the reference input.

The uP1658P uses MOSFET $R_{DS(ON)}$ current sensing for channel current balance. The uP1658P also implements a multi-function pin (OCS/CB) for OCP threshold selection and current balance adjustment.

Other features include power saving control input, and a power good output. This part is available in WQFN3x3 - 20L package.

Supply Input and Power On Reset

The uP1658P receives supply input from PVCC pin to provide power to MOSFET gate drivers and internal control circuit. The logic input to EN pin controls the enable/disable state of this chip. The uP1658P continuously monitors PVCC and EN voltages to ensure all power voltages are ready for normal operation. The PVCC POR level is typically 4.1V. The EN high level is typically 1.6V.

The uP1658P integrates floating MOSFET gate driver that are powered from the PVCC pin. A bootstrap switch is embedded to facilitate PCB design and reduce the total BOM cost. No external Schottky diode is required in real applications. An external Schottky diode with lower voltage drop can improve the power conversion efficiency.

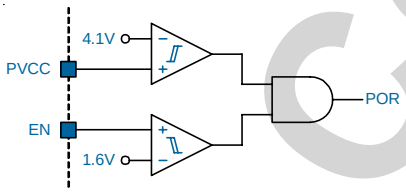


Figure 1. Circuit of Power Ready Detection

Phase Number of Operation (Hard-wire Programming)

The uP1658P supports 2/1 phase operation. The maximum phase number of operation is determined by checking the PSI pin voltage during POR. If PSI pin is connected to a voltage source higher than (52% of PVCC) during POR, the uP1658P enters 2-phase operation. If PSI pin voltage is lower than (44% of PVCC) during POR, uP1658P enters *always 1-phase* configuration, and the uP1658P will enter soft-start sequence with 1-phase operation after POR. Once selected, the maximum phase number of operation is latched and can only be changed at the next POR. Since the phase number programming is determined by comparing the PSI pin voltage with the PVCC voltage, the sequence of PSI pin voltage and PVCC should be taken care that the PSI pin voltage must be ready before controller POR.

Voltage Control Loop and PWMVID Function

Figure 2 illustrates the voltage control loop of the uP1658P. FB and REFIN are negative and positive inputs of the Error Amplifier respectively. The Error Amplifier modulates the COMP voltage V_{COMP} of buck converter to force FB voltage V_{FB} follows V_{REFIN}.

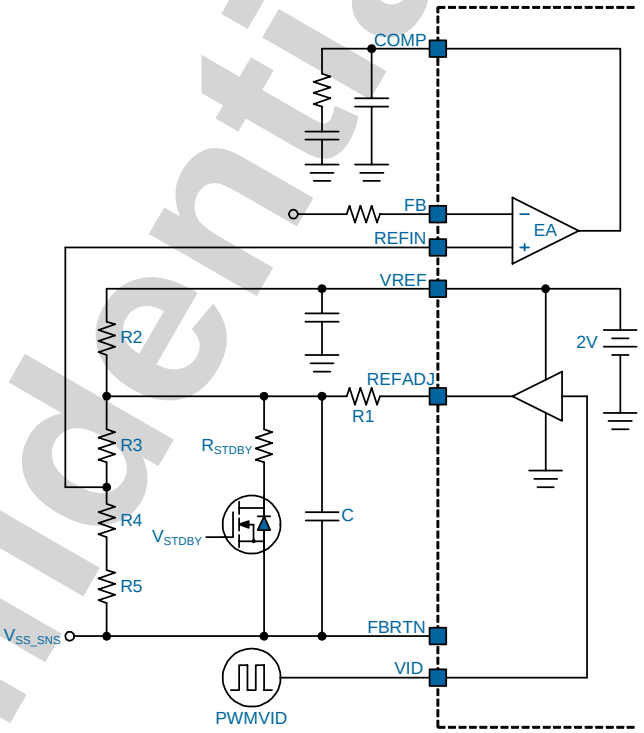


Figure 2. Voltage Control Loop

The PWMVID signal from GPU is applied to the VID pin, which is the input pin of the internal buffer. This buffer plays the role of level shifting, and the output of this buffer is injected into the external RC integrator to generate REFIN voltage, which can be calculated as:

$$V_{REFIN} =$$

$$V_{VREF} \times D \times \frac{R2 // (R3+R4+R5)}{R1+R2 // (R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5} +$$

$$V_{VREF} \times \frac{R1 // (R3+R4+R5)}{R2+R1 // (R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5}$$

where V_{REFIN} is the DC voltage of REFIN, V_{VREF} is the voltage of VREF (typically 2V), and D is the duty cycle of PWMVID input. The VREF pin is an internal LDO, therefore an output decoupling capacitor is required. Recommend connecting at least a 1uF capacitor from VREF pin to local GND. DO NOT connect the VREF decoupling capacitor to FBRTN.

Boot Voltage and Standby Mode

The new generation PWMVID structure includes two operation modes other than normal operation: boot mode and standby mode. During boot mode, the GPU stops sending PWMVID signal and the input of the PWMVID buffer is floating. The REFADJ pin enters high impedance state after the VID pin enters tri-state region, and the REFIN voltage can then be calculated as:

$$V_{REFIN,BOOT} = V_{VREF} \times \frac{R4+R5}{R2+R3+R4+R5}$$

During standby mode, other than GPU stopping the PWMVID transaction, an external system standby signal additionally controls the entry of standby mode. An additional external switch should be connected in parallel with the original PWMVID resistors as shown in Figure 3 to generate the standby mode voltage:

$$V_{REFIN,STDBY} = V_{VREF} \times \frac{(R3+R4+R5)//R_{STDBY}}{R2+(R3+R4+R5)//R_{STDBY}} \times \frac{R4+R5}{R3+R4+R5}$$

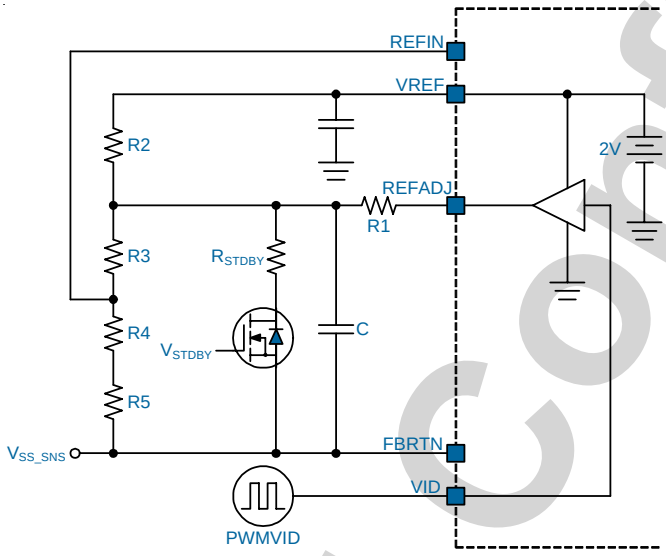


Figure 3. Standby Mode Configuration

OCP Setting and Current Balance Offset

Figure 4 shows the multi-function OCS/CB pin for OCP threshold selection and current balance. After PVCC is higher than POR threshold, S_1 is turned on and the OCS/CB pin is internally connected to an internal 2V voltage source. Since the OCS/CB pin is latched at 2V during POR, the OCS current flowing out of OCS/CB pin is determined by R2 in figure 3. The OCS current can be calculated as:

$$I_{OCS(S1\_on)} = \frac{V_{OCS}}{R2} = \frac{2}{R2}$$

After the I_{OCS} is generated (during S1 is turned on), the internal A/D converter at the OCS/CB pin will sample/hold the I_{OCS}, and the uP1658P will determine the OCS level according to the following table:

OC Level	I_{OCS} Range	$V_{PHASE,MAX}$ (GND-PHASE)
1	< 10uA	40 mV
2	10uA ~ 20uA	60 mV
3	20uA ~ 30uA	80 mV
4	30uA ~ 50uA	100 mV
5	50uA ~ 80uA	130 mV
6	80uA ~ 130uA	160 mV
7	130uA ~ 200uA	220 mV
8	> 200uA	280 mV

where the $V_{PHASE,MAX}$ is the per-phase GND-PHASE voltage when the power stage low-side MOSFETs is turned-on. For example, if the sampled I_{OCS} is 25uA, the latched OC level is level 3, and the maximum GND-PHASE voltage is 80mV, which means the uP1658P triggers OC shutdown when per-phase $I_{SD,LMOS}$*$R_{DS(ON),LMOS}$ exceeds 80mV. Since the OCS mechanism detects per-phase current for OCP triggering, the total OCP threshold can be calculated as:

$$I_{MAX,total} = N \times \frac{V_{PHASE,MAX}}{R_{DS(ON)}}$$

where N is operating phase number, $V_{PHASE,MAX}$ is the per-phase GND-PHASE voltage when the power stage low-side MOSFETs is turned-on, and $R_{DS(ON)}$ is the on-resistance of equivalent per-phase power stage low side MOSFET. After any phase's current exceeds $I_{MAX,per\text{-}phase}$ and sustained 6us, the over current protection is triggered and shuts down the uP1658P and turns off all high-side and low-side MOSFETs, and this latched-off protection can only be reset by PVCC re-POR or EN restart.

After the I_{OCS} is sampled and the OC level is determined, the uP1658P turns off S1 and turns on S2 for current balance adjustment. When S2 is turned on, the OCS/CB pin voltage is determined by the external voltage divider, and the OCS/CB voltage V_{CB} is connected to the internal current balance circuit for phase current offset adjustment. The phase current adjustment is achieved as the following table:

V_{CB}	Current Balance
> 1.5V	Decrease phase2's current
1.1V < V_{CB} < 1.5V	Remain unchanged
< 1.1V	Decrease phase1's current

For example, when the V_{CB} is >1.5V, the uP1658P will decrease phase2 on-time in purpose of decreasing phase2 current, and larger V_{CB} leads to less phase2 current. Similarly, when the V_{CB} is <1.1V, the phase1's current will be decreased, and smaller V_{CB} leads to less phase1 current. When V_{CB} is between 1.1V and 1.5V, the current balance offset function is disabled, and the current balance is only determined by internal current balance loop.

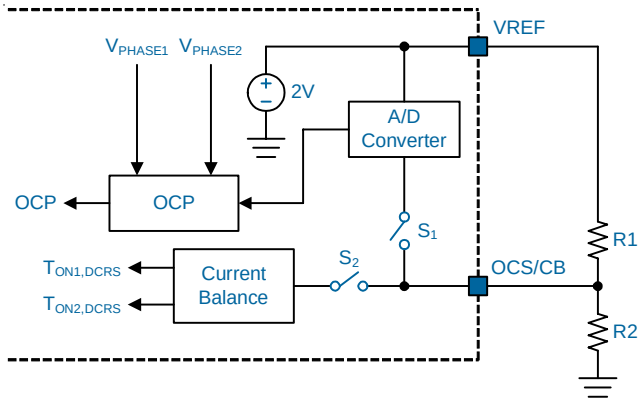


Figure 4. OCS/CB Pin for OCP Threshold Selection and Current Balance Offset

Soft-Start Sequence

A built-in soft-start function is used to prevent surge current from power supply input during power on. The error amplifier is a three-input device. Reference voltage (V_{REFIN}) or the internal soft-start voltage (V_{SS}) whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. After EN goes high, there is typical 300us delay time for OCP setting and controller self-calibration. Internal soft-start voltage starts to ramp up linearly to PVCC with a slew rate determined by V_{REFIN} after the soft-start cycle is initiated. The output voltage will follow the internal soft-start voltage (V_{SS}) and ramp up linearly to its target level. The output voltage ramp-up time is typically 1.4ms. The UVP is activated typically 50us after the end of soft-start (internal UVP_EN signal go high). If there is no any fault detected at the end of soft-start, controller then asserts POK when output voltage reaches 90% of V_{REFIN} with typical 100us delay time. The following graph shows the uP1658P soft-start sequence.

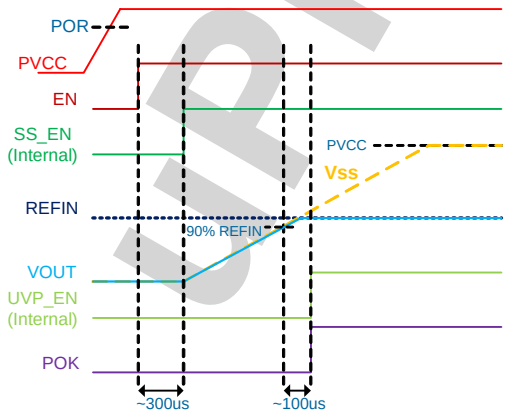


Figure 5. Soft-Start Sequence

Power Saving Mode

The uP1658P provides power saving features for platform designers to program platform specific power saving configuration. There are four operation modes: full-phase CCM, single-phase USM, single-phase FCCM, and single-phase PSM. The uP1658P switches between these four operation modes according to the input voltage level of the PSI pin. Figure 6 shows typical PSI application circuit, and Table 1 shows recommended PSI setting voltage level of four operation modes. In single-phase operation, the uP1658P auto-selects phase 1 to be the operating phase. In PSM, the uP1658P automatically reduces switching frequency at light load to maintain high efficiency. As the load current decreases, the rectifying MOSFET is turned off when zero inductor current is detected, and the converter runs in discontinuous conduction mode. In USM, the operation of the converter is also a discontinuous conduction mode similar to PSM, and additionally the USM control circuit monitors both high-side and low-side MOSFETs and force to change into the ON state to avoid the switching frequency falling within audible region.

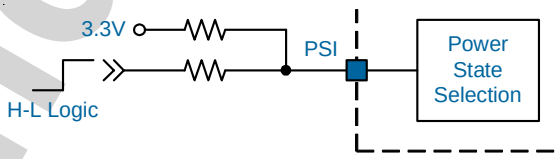


Figure 6. PSI application circuit

Table 1. Recommended PSI Setting

Operation Mode	Recommended Voltage Setting at PSI
Full-Phase CCM	3.3V
Single-Phase USM	2V
Single-Phase FCCM	1.2V
Single-Phase PSM	GND

Over Voltage Protection (OVP)

The OVP is triggered if V_{FB} > 1.4xV_{REFIN} sustained 6us. When OVP is activated, the uP1658P turns on all low-side MOSFET and turns off all high-side MOSFET. The over voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Under Voltage Protection (UVP)

The under voltage protection is triggered if V_{FB} < 0.5xV_{REFIN} sustained 10us. When UVP is activated, the uP1658P turns off all high-side and low-side MOSFET. The under voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Over Temperature Protection (OTP)

The uP1658P monitors the temperature of itself. If the temperature exceeds typical 150°C, the uP1658P is forced into shutdown mode. The over temperature protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, PVCC ---------- -0.3V to +6.5V

BOOTx to PHASEx

DC ---------- -0.3V to +6V

PHASEx to GND

DC ---------- -0.7V to +28V

< 100ns ---------- -8V to +36V

BOOTx to GND

DC ---------- -0.3V to +34V

< 100ns ---------- -5V to +42V

UGATEx to PHASEx

DC ---------- -0.3V to +6V

< 100ns ---------- -5V to +7V

LGATEx to GND

DC ---------- -0.3V to +6V

< 100ns ---------- -5V to +7V

Other Pins ---------- -0.3V to +6V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

HBM (Human Body Mode) ---------- 2kV

MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

WQFN3x3 - 20L θ_{JA} ---------- 68°C/W

WQFN3x3 - 20L θ_{JC} ---------- 6°C/W

Power Dissipation, P_D @ T_A = 25°C

WQFN3x3 - 20L θ_{JC} ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Input Voltage, V_{IN} ---------- 3V to 26V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(PVCC = 5V, T_A = 25°C, unless otherwise specified)

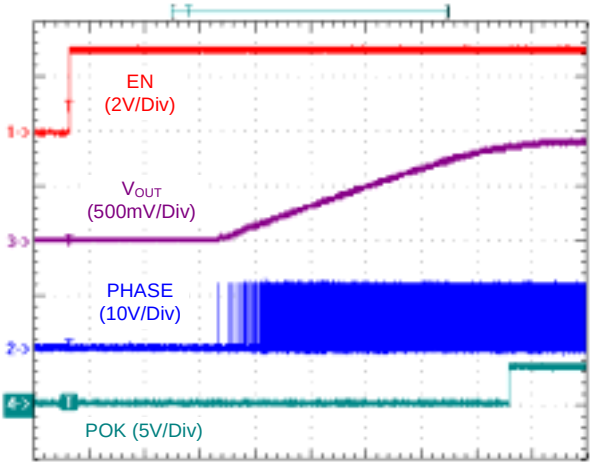
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Current	I_{PVCC}	V_{REFIN} = 0.9V, EN = 3.3V, V_{FB} = 1V, no switching	--	2	--	mA
Shutdown Current	I_{SHDN}	EN = 0V	--	2	--	uA
PVCC POR Threshold	$V_{PVCCRTH}$	V_{PVCC} Rising.	3.9	4.1	4.3	V
PVCC POR Hysteresis	$V_{PVCCHYS}$		--	0.3	--	V
VREF Voltage Accuracy			1.98	2	2.02	V
VREF Maximum Output Current			10	--	--	mA
Control Input: EN						
Logic Low Threshold			--	--	0.8	V
Logic High Threshold			2.4	--	--	V
Internal Pull-down Current			--	10	--	uA
Reference Voltage						
REFIN Disable Threshold			--	--	0.13	V
External Rererence Voltage Range	V_{REFIN}		0.27	--	2	V
On Time						
One Shot Width	T_{ON}	V_{IN} = 12V, V_{OUT} = 1.1V for F_{SW} = 300kHz	--	280	--	ns
Minimum Off Time	T_{OFF_MIN}		--	350	--	ns
USM Frequency						
USM Frequency	f_{USM}	USM	25	--	--	kHz
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	30	--	--	MHz
Slew Rate	SR	Guaranteed by Design	3	6	--	V/us
Trans-conductance	GM	R_{LOAD} = 20kΩ	--	2300	--	uA/V
Maximum Current (Source & Sink)	I_{COMP}	V_{COMP} = 1.6V	250	300	--	uA
Current Sense Amplifier						
Input Offset Voltage	V_{OS}		-1	--	1	mV
Max Sourcing Current			100	--	--	uA
FBRTN						
FBRTN Current	I_{FBRTN}	EN = 3.3V, no switching	--	--	500	uA
Soft Start						
Soft Start Period	T_{SS}	From EN = high to PGOOD = high	--	1.4	--	ms

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWMVID Buffer						
VID Input Low Level	V_{OL}		--	1	--	V
VID Input High Level	V_{OH}		--	2	--	V
VID Tri-state Delay			--	100	--	ns
REFADJ Output Low Voltage	V_{IL}	I_{SINK} = 1mA	--	--	0.05	V
REFADJ Output High Voltage	V_{IH}	I_{SRC} = 1mA	1.95	--	--	V
VREFADJ Source Resistance	R_{BF_SRC}	I_{SRC} = 1mA	--	20	--	Ω
VREFADJ Sink Resistance	R_{BF_SNK}	I_{SNK} = 1mA	--	20	--	Ω
PSI						
Power Saving Input Threshold	V_{PSI}	Multi-phase CCM	52	--	--	% of PVCC
		USM	36	--	44	% of PVCC
		Single-phase FCCM	20	--	28	% of PVCC
		PSM	--	--	12	% of PVCC
Gate Drivers						
Upper Gate Source	R_{UG_SRC}	I_{UG} = -80mA	--	1	2	Ω
Upper Gate Sink	R_{UG_SNK}	I_{UG} = 80mA	--	0.5	1	Ω
Lower Gate Source	R_{LG_SRC}	I_{LG} = -80mA	--	1	2	Ω
Lower Gate Sink	R_{LG_SNK}	I_{LG} = 80mA	--	0.4	0.8	Ω
Dead Time	T_{DT}		--	30	--	ns
Internal Bootstrap Switch						
On Resistance	R_{ST}	I_F = 10mA	--	80	--	Ω
Reverse Leakage Current	I_{ST}	V_{BOOTX} = 26V	--	0.01	1.5	uA
Zero Current Detection Threshold						
Zero Current Threshold	V_{ZC}	GND-PHASE	--	2	--	mV
Protection						
OCP Setting Voltage	V_{OCS}		--	2	--	V
OVP Threshold	V_{OVP}	V_{FB}/V_{REFIN}	140	--	--	%
UVP Threshold	V_{UVP}	V_{FB}/V_{REFIN}	--	--	50	%
OTP Threshold			150	--	--	°C
Power Good Indicator						
Power Good Indicator		I_{SINK} = 4mA	--	--	0.3	V

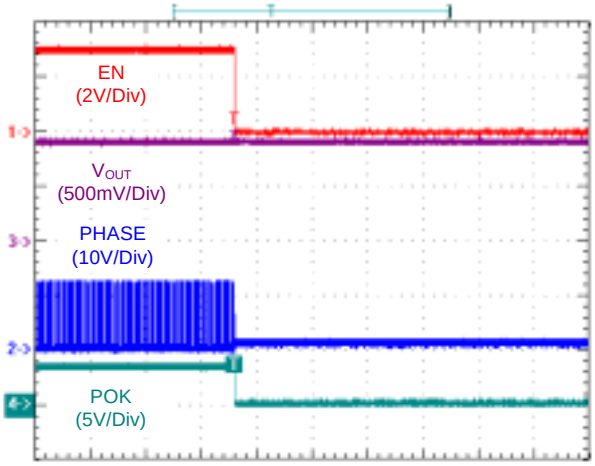
Typical Operation Characteristics

EN Turn On



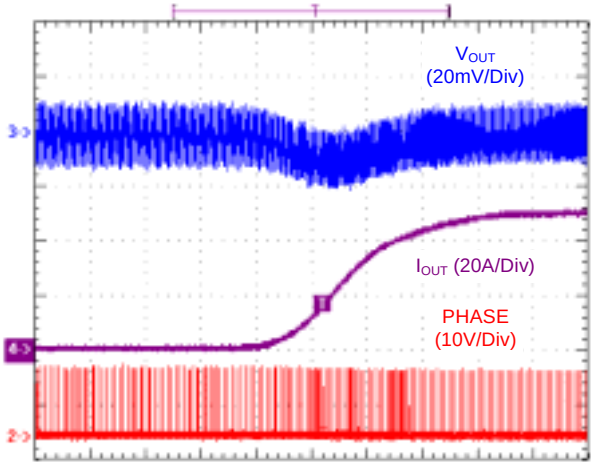
Time (200us/Div)
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 0A

EN Turn Off



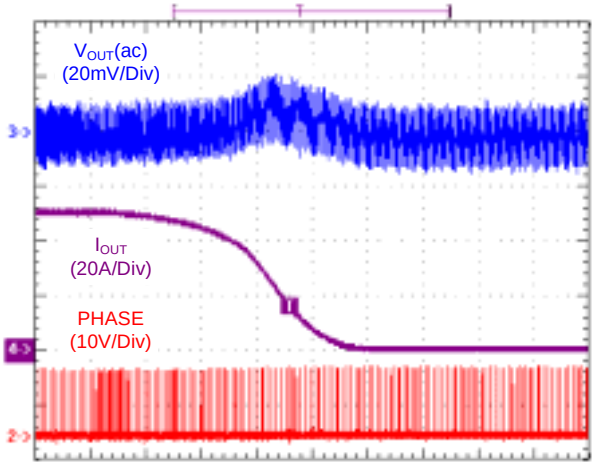
Time (100us/Div)
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 0A

Transient: Undershoot



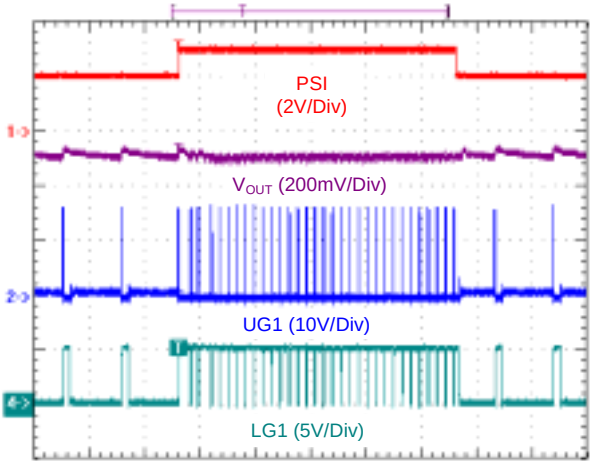
Time (40us/Div)
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 0A - 50A

Transient: Overshoot



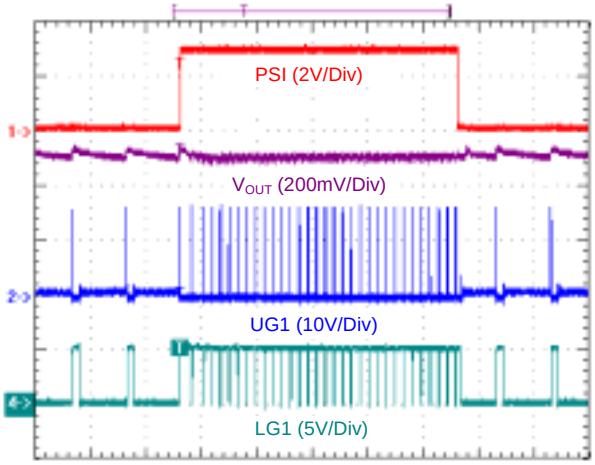
Time (40us/Div)
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 50A - 0A

PSI Toggle: USM ←→ Multi CCM



Time (20us/Div)
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 0.5A

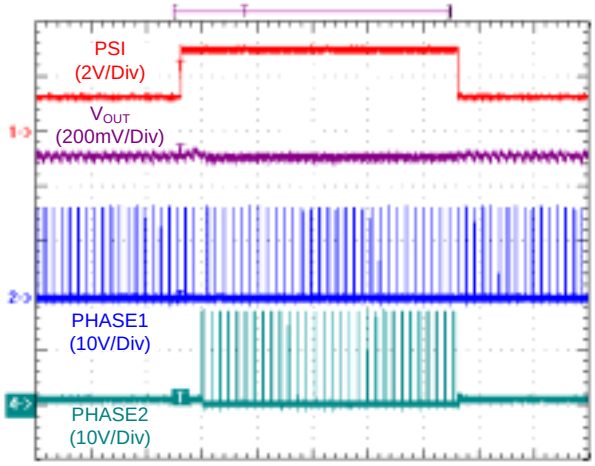
PSI Toggle: PSM ←→ Multi CCM



Time (20us/Div)
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 0.5A

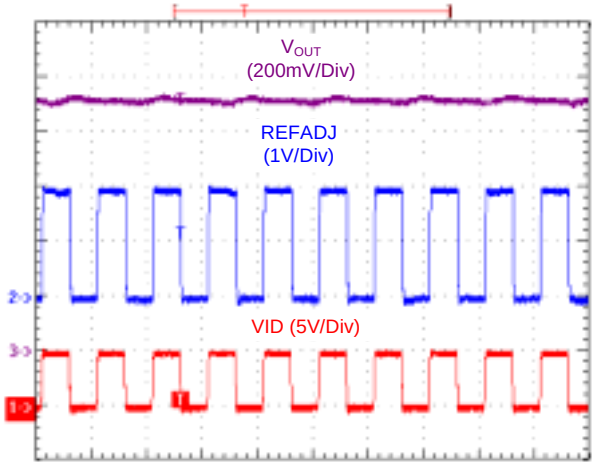
Typical Operation Characteristics

PSI Toggle: Single CCM ↔ Multi CCM



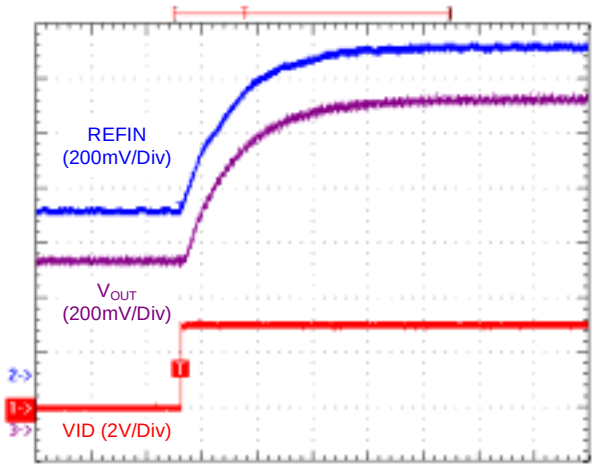
Time (20us/Div)
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 0.5A

PWMVID: 50%, 1.125MHz



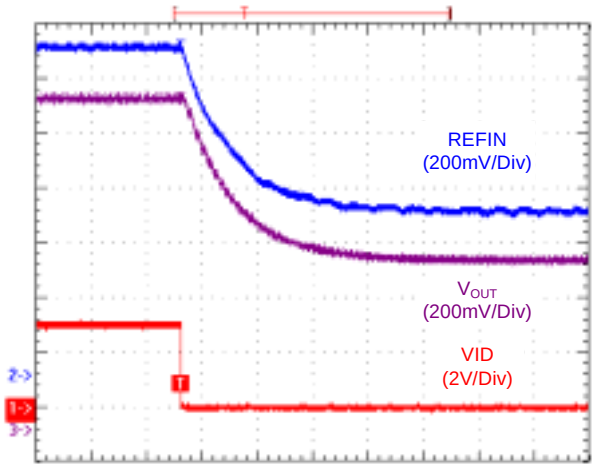
Time (1us/Div)
V_{IN} = 12V, No load

VID: 0% → 100%



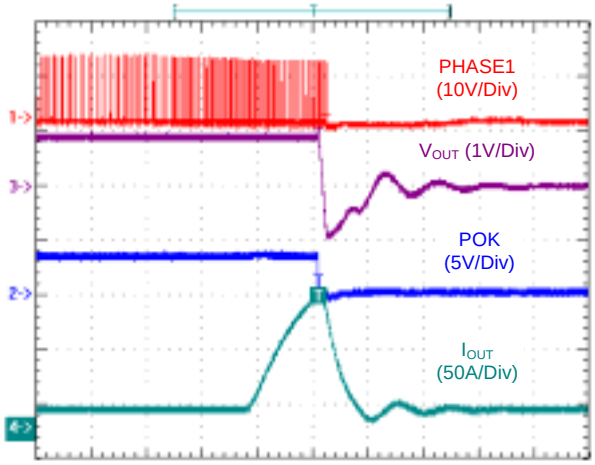
Time (20us/Div)
V_{IN} = 12V, No load

VID: 100% → 0%



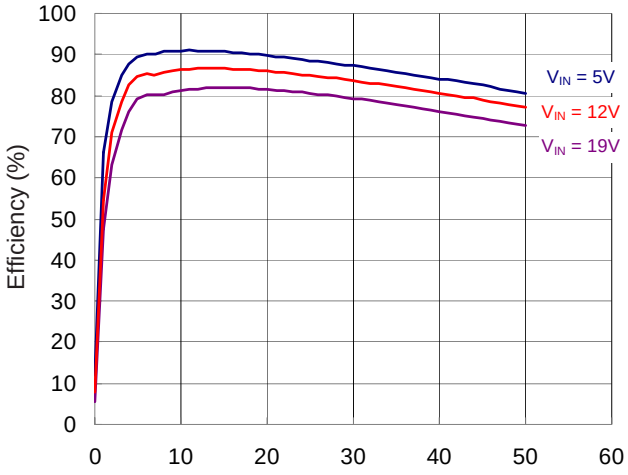
Time (20us/Div)
V_{IN} = 12V, No load

Short Circuit Protection



Time (40us/Div)
V_{IN} = 12V, V_{OUT} = 0.9V

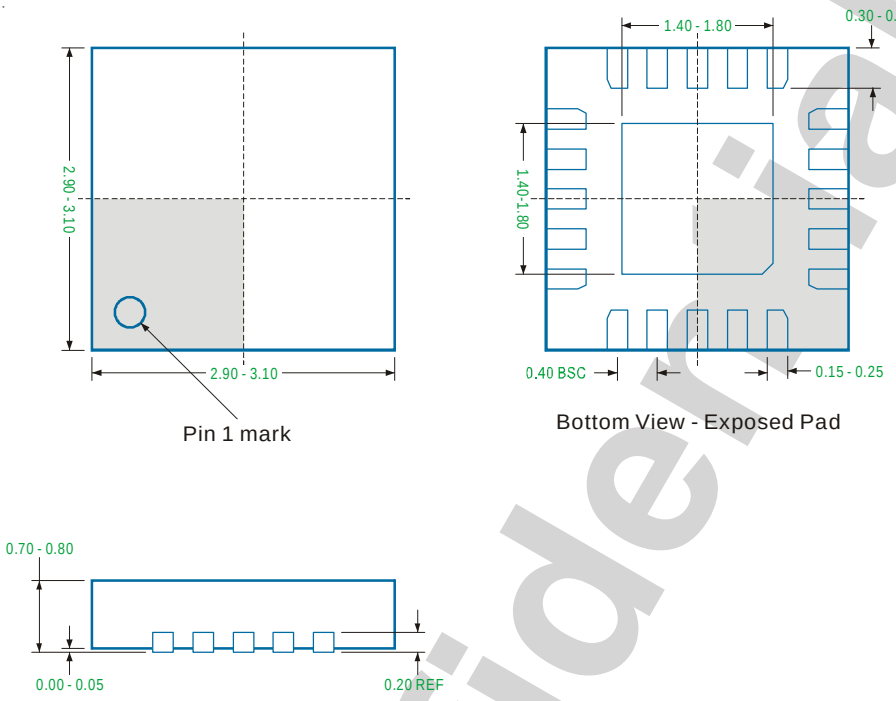
Efficiency vs. Output Current



V_{CC} = 5V, V_{OUT} = 0.9V

Package Information

WQFN3x3 - 20L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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uPI Semiconductor Corp.

Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064