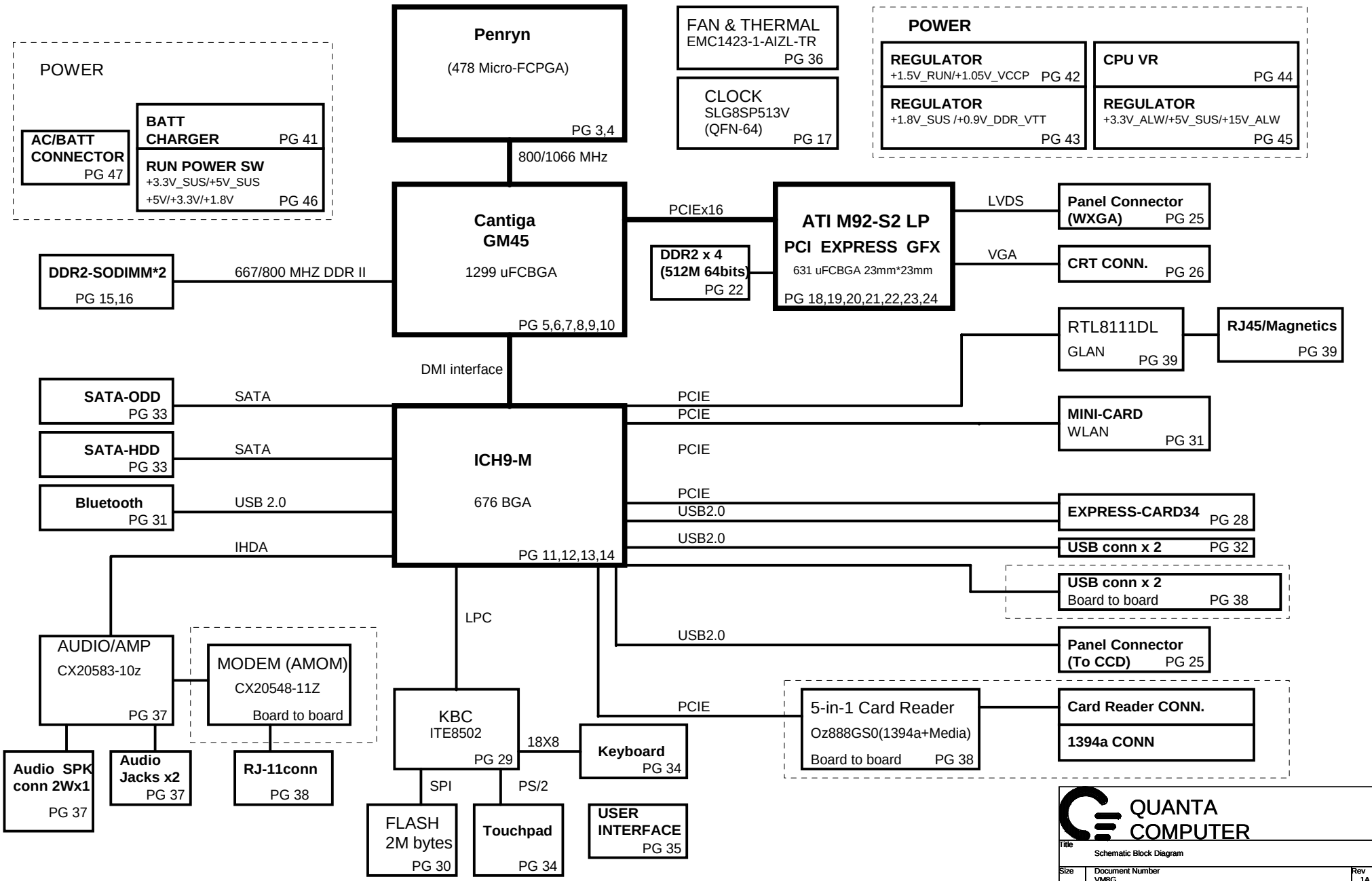
OolongTea Block Diagram

VER : A1A



QUANTA COMPUTER

Title	Schematic Block Diagram	
Size	Document Number VM8G	Rev 1A
Date: Wednesday, February 18, 2009	Sheet 1 of 58	

Table of Contents

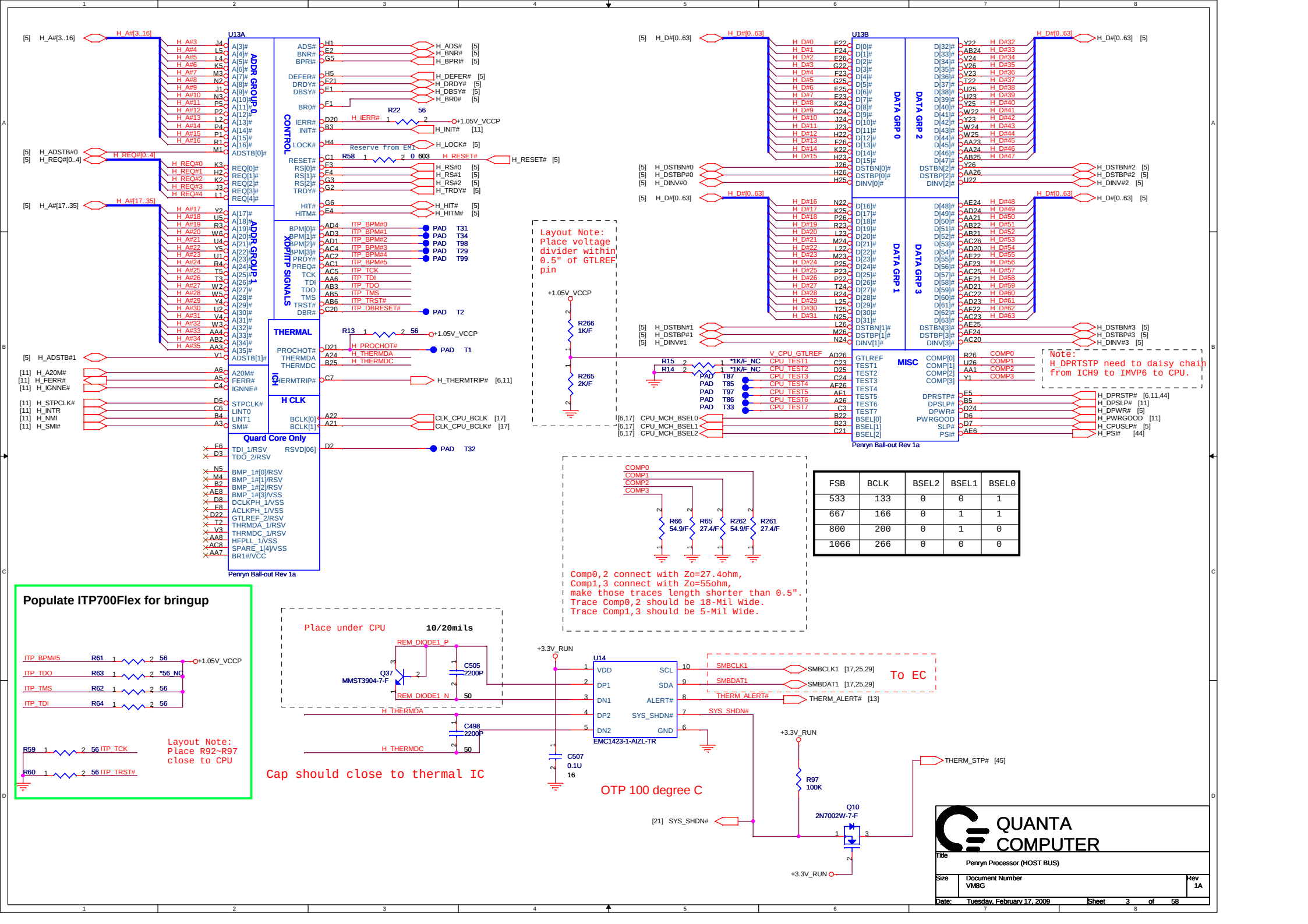
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,25,30,39,41,42,43,44,45,49,50	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,29,30,35,39,40,41,43,45,46,47	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	42,43,45,46,47,49	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	25,45,46	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	39	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,32,35,44,45,46,49,50	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,19,25,28,35,42,44,46,49	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,42,43,46,49	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,43,46	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,26,33,34,35,36,37,46,50	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,6,8,9,11,12,13,14,15,17,19,25,26,27,28,29, 31,33,35,36,37,39,46,50	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,28,31,42,46,50	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,42,50	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,44	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	25	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	33	Module Power	MODC_EN#	
+5V_HDD	+5V	33	HDD Power	HDDC_EN#	
+PBATT	+10V~+17V		MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V		SECOND BATTERY	CHG_SBATT	
+1.1V_GFX_PCIE	+1.1V	20	GFX PCIE POWER	GFX_RUN_ON	
+VCC_GFX_CORE	+0.9~+1.1	20,23,49	GFX CORE POWER	GFX_RUN_ON	

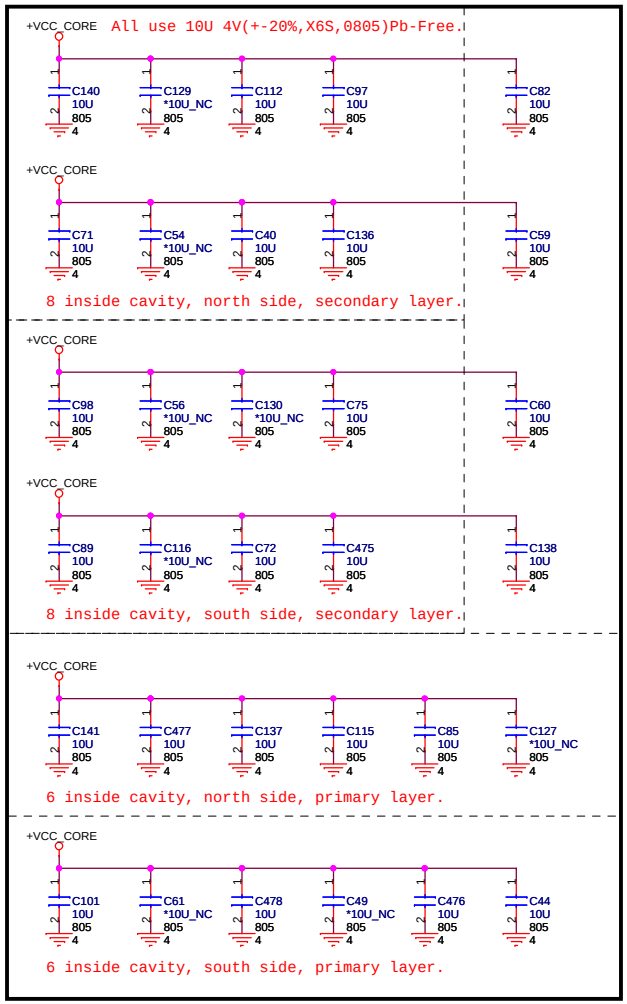
GND PLANE	PAGE	DESCRIPTION
GND	ALL	

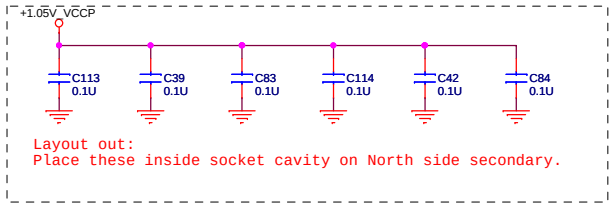
QUANTA COMPUTER

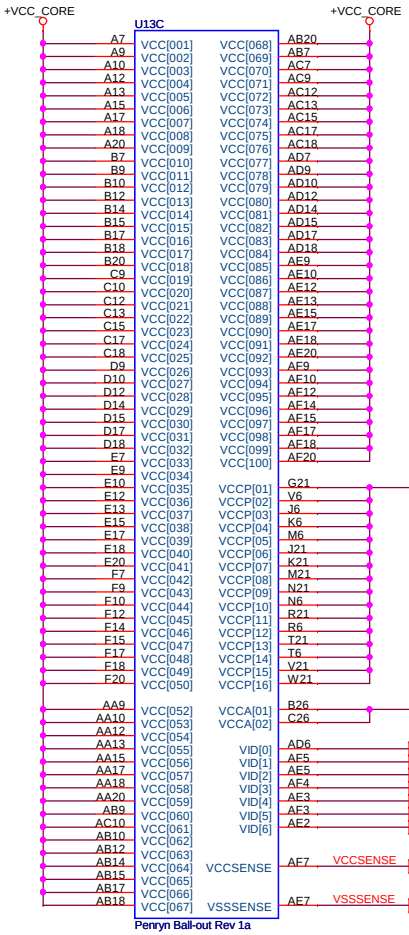
Title	Index & Power Status	
Size	Document Number VM8G	Rev 1A
Date: Saturday, February 14, 2009	Sheet 2 of 58	

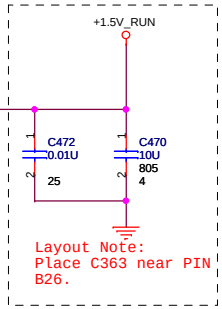


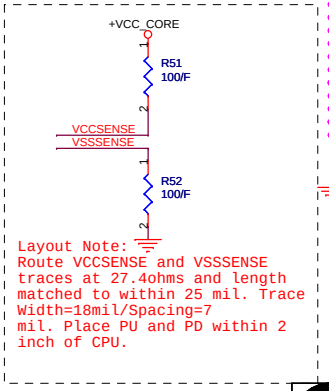
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0

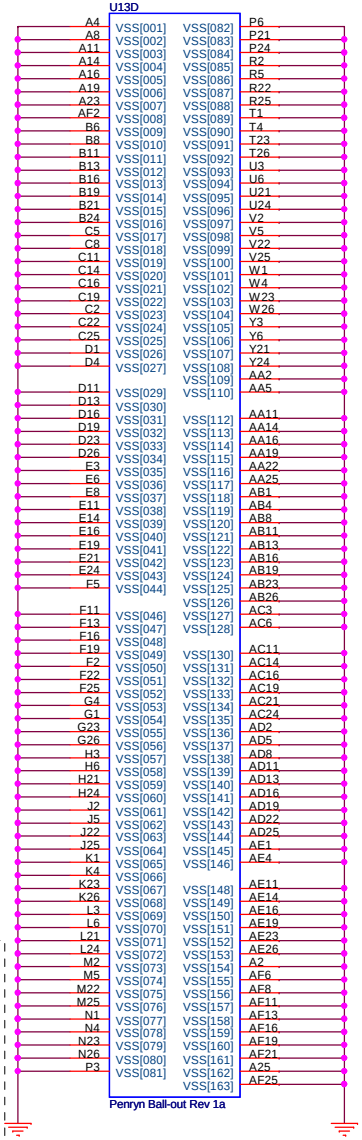






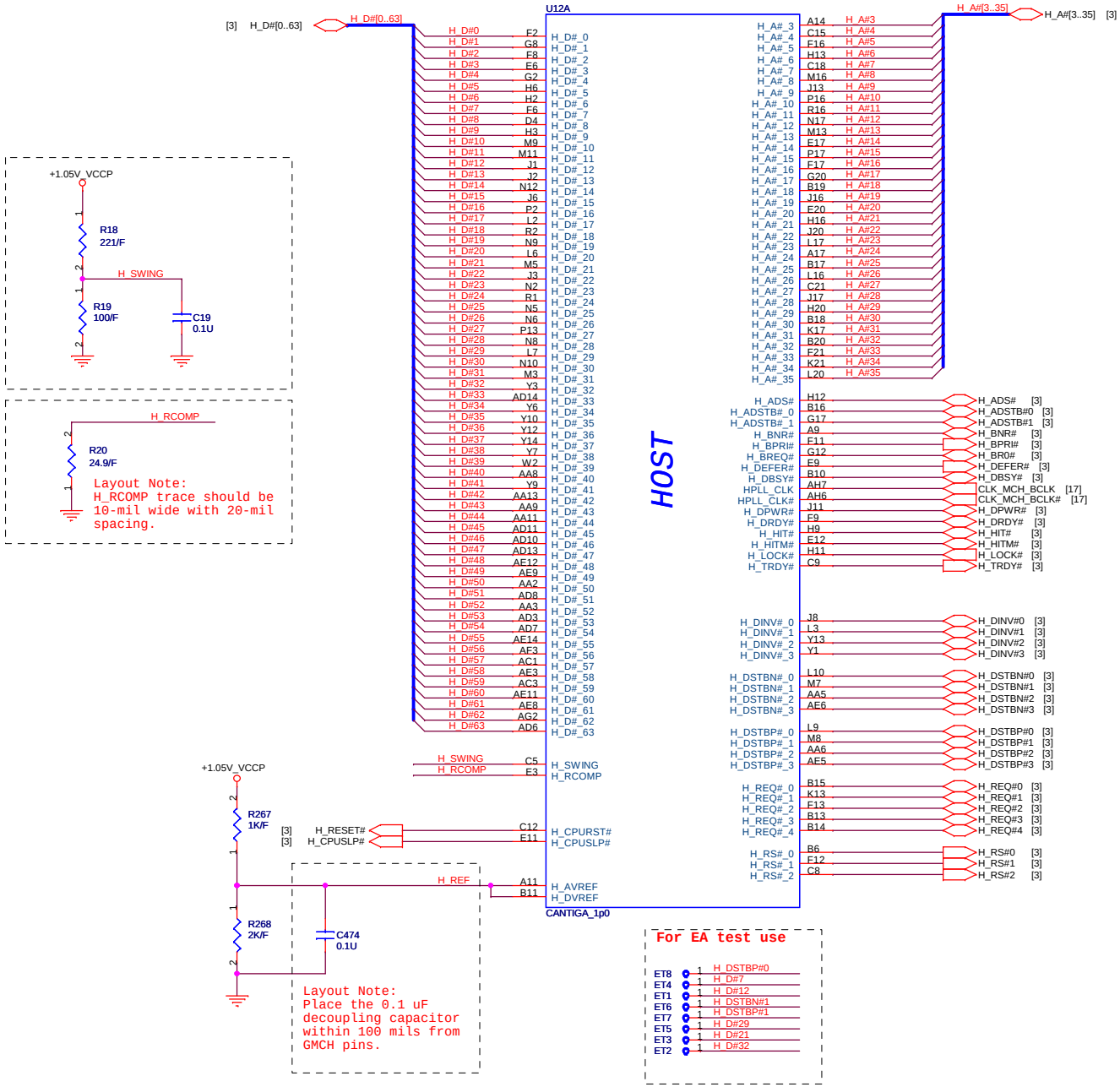






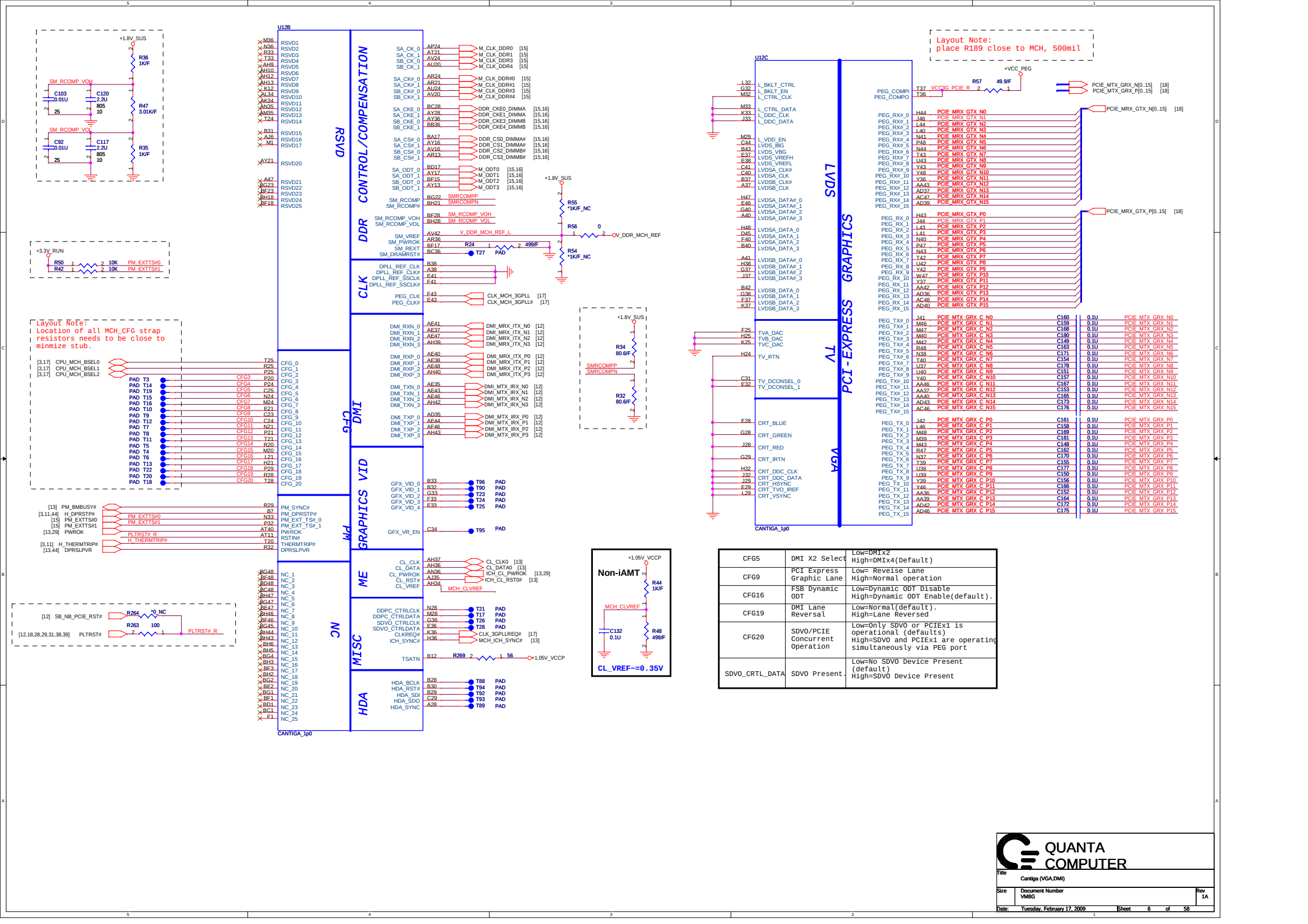
QUANTA COMPUTER

Title	Penryn Processor (POWER)	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 4 of 58	

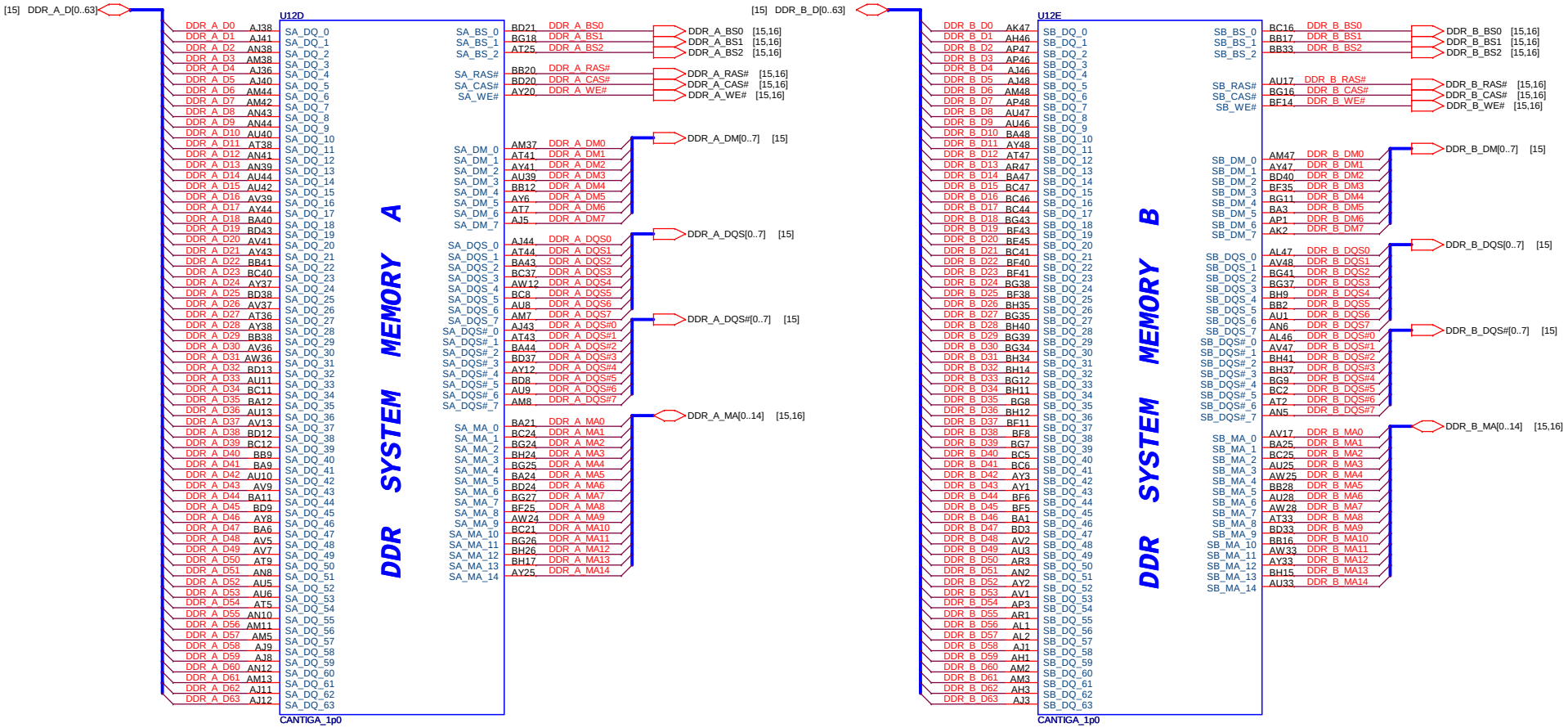


QUANTA COMPUTER

Title	Cantiga (HOST)	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 5 of 58	

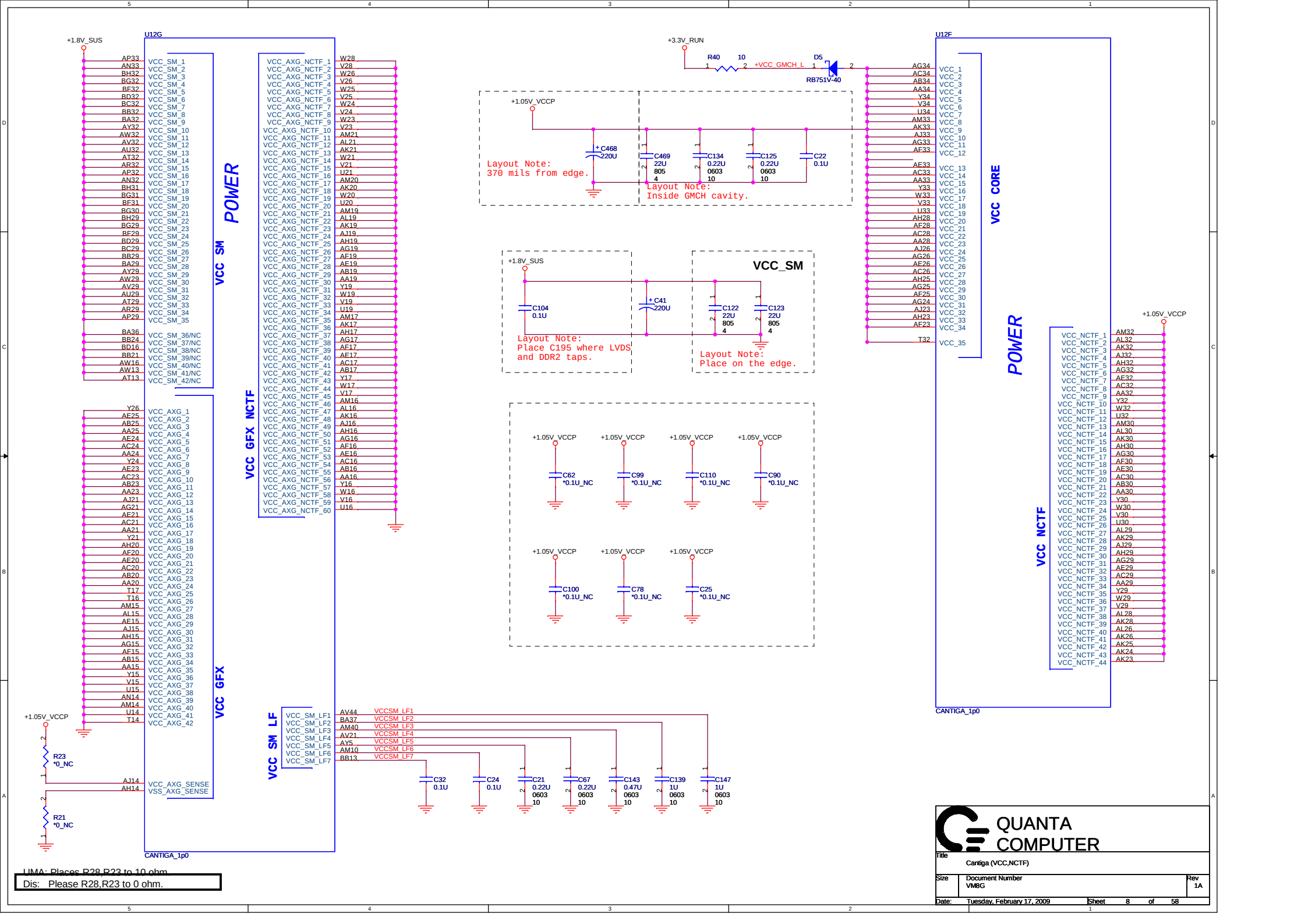


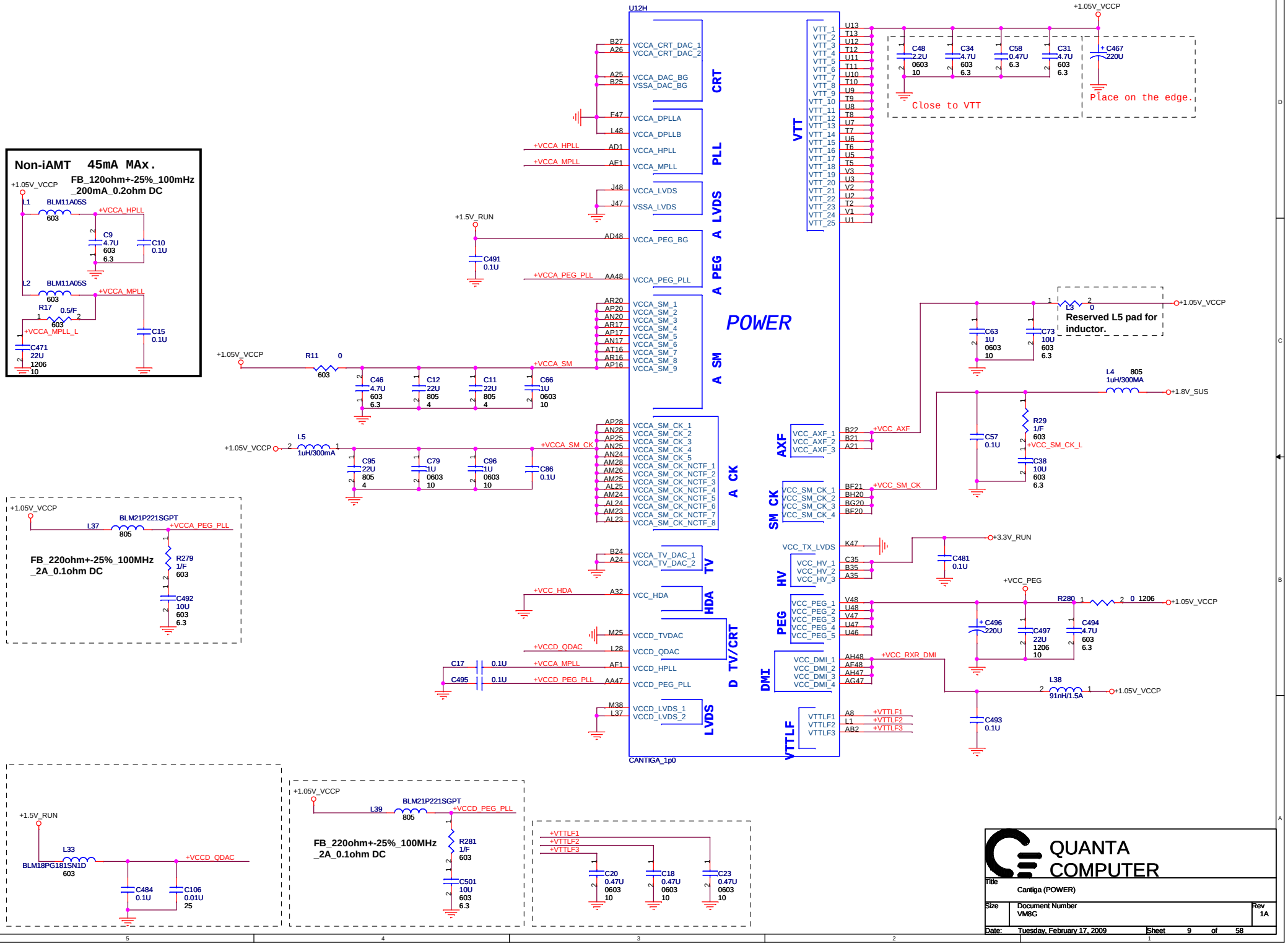
CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

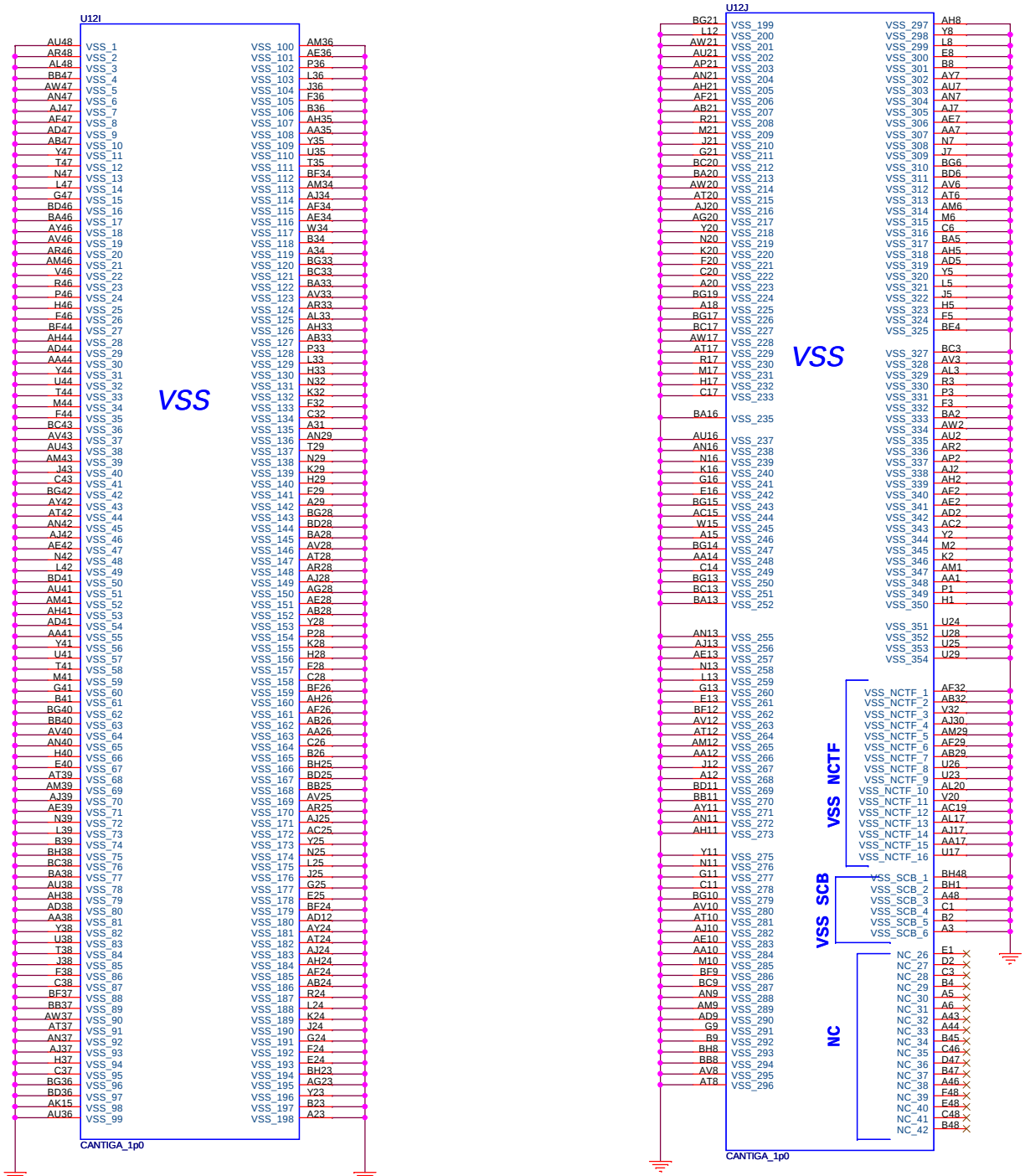


QUANTA COMPUTER

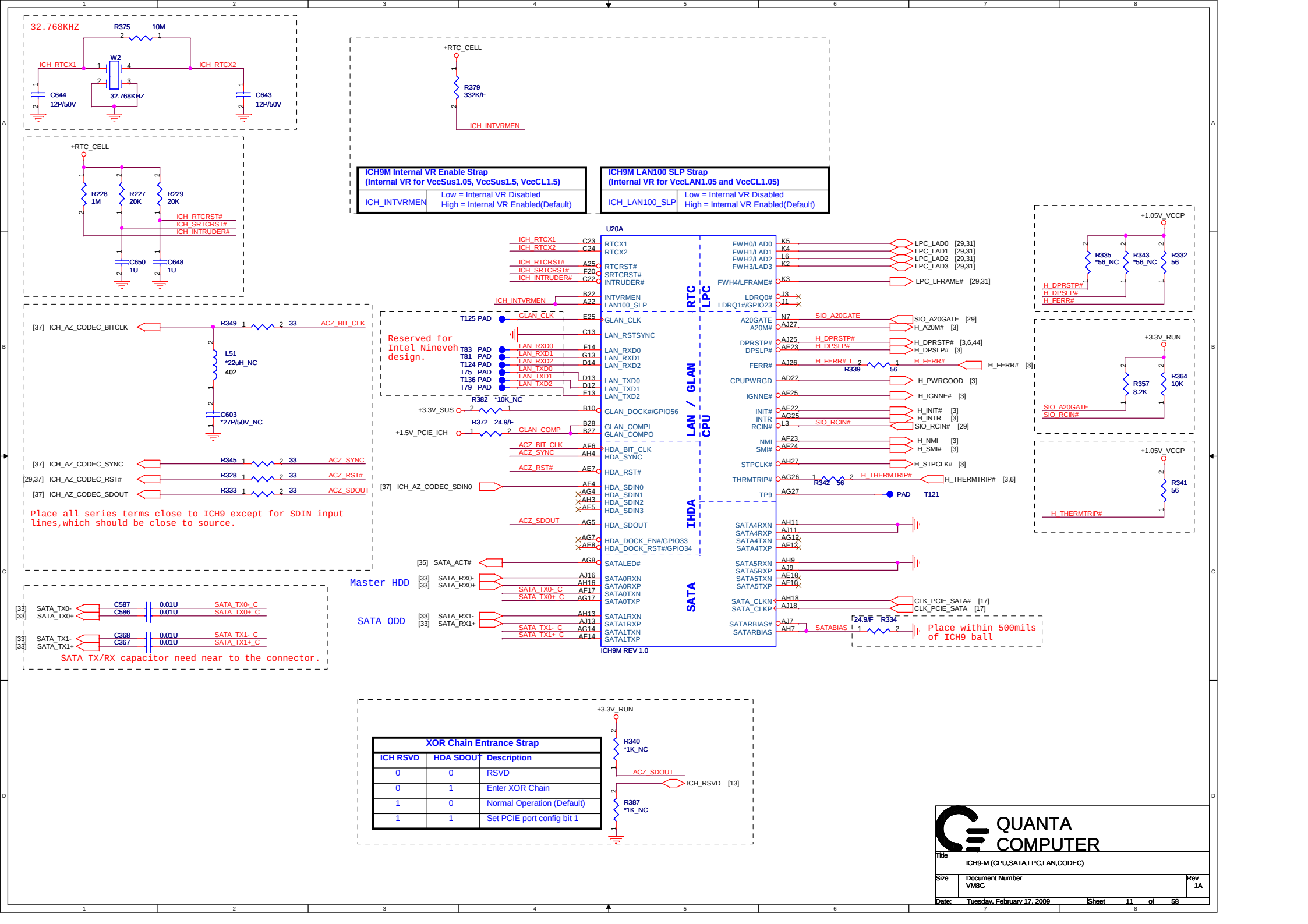
Title	Cantiga (DDR2)	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 7 of 58	


U12G
+1.8V_SUS
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
VCC_SM_26
VCC_SM_27
VCC_SM_28
VCC_SM_29
VCC_SM_30
VCC_SM_31
VCC_SM_32
VCC_SM_33
VCC_SM_34
VCC_SM_35
VCC_SM_36/NC
VCC_SM_37/NC
VCC_SM_38/NC
VCC_SM_39/NC
VCC_SM_40/NC
VCC_SM_41/NC
VCC_SM_42/NC
VCC SM
POWER
VCC_AXG_1
VCC_AXG_2
VCC_AXG_3
VCC_AXG_4
VCC_AXG_5
VCC_AXG_6
VCC_AXG_7
VCC_AXG_8
VCC_AXG_9
VCC_AXG_10
VCC_AXG_11
VCC_AXG_12
VCC_AXG_13
VCC_AXG_14
VCC_AXG_15
VCC_AXG_16
VCC_AXG_17
VCC_AXG_18
VCC_AXG_19
VCC_AXG_20
VCC_AXG_21
VCC_AXG_22
VCC_AXG_23
VCC_AXG_24
VCC_AXG_25
VCC_AXG_26
VCC_AXG_27
VCC_AXG_28
VCC_AXG_29
VCC_AXG_30
VCC_AXG_31
VCC_AXG_32
VCC_AXG_33
VCC_AXG_34
VCC_AXG_35
VCC_AXG_36
VCC_AXG_37
VCC_AXG_38
VCC_AXG_39
VCC_AXG_40
VCC_AXG_41
VCC_AXG_42
VCC GFX
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
VCC_AXG_NCTF_18
VCC_AXG_NCTF_19
VCC_AXG_NCTF_20
VCC_AXG_NCTF_21
VCC_AXG_NCTF_22
VCC_AXG_NCTF_23
VCC_AXG_NCTF_24
VCC_AXG_NCTF_25
VCC_AXG_NCTF_26
VCC_AXG_NCTF_27
VCC_AXG_NCTF_28
VCC_AXG_NCTF_29
VCC_AXG_NCTF_30
VCC_AXG_NCTF_31
VCC_AXG_NCTF_32
VCC_AXG_NCTF_33
VCC_AXG_NCTF_34
VCC_AXG_NCTF_35
VCC_AXG_NCTF_36
VCC_AXG_NCTF_37
VCC_AXG_NCTF_38
VCC_AXG_NCTF_39
VCC_AXG_NCTF_40
VCC_AXG_NCTF_41
VCC_AXG_NCTF_42
VCC_AXG_NCTF_43
VCC_AXG_NCTF_44
VCC_AXG_NCTF_45
VCC_AXG_NCTF_46
VCC_AXG_NCTF_47
VCC_AXG_NCTF_48
VCC_AXG_NCTF_49
VCC_AXG_NCTF_50
VCC_AXG_NCTF_51
VCC_AXG_NCTF_52
VCC_AXG_NCTF_53
VCC_AXG_NCTF_54
VCC_AXG_NCTF_55
VCC_AXG_NCTF_56
VCC_AXG_NCTF_57
VCC_AXG_NCTF_58
VCC_AXG_NCTF_59
VCC_AXG_NCTF_60
VCC GFX NCTF
+1.05V_VCCP
R23
*0_NC
R21
*0_NC
AJ14
AH14
VCC_AXG_SENSE
VSS_AXG_SENSE
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
VCC SM LF
VCCSM_LF1
VCCSM_LF2
VCCSM_LF3
VCCSM_LF4
VCCSM_LF5
VCCSM_LF6
VCCSM_LF7
C32 0.1U
C24 0.1U
C21 0.22U 0603 10
C67 0.22U 0603 10
C143 0.47U 0603 10
C139 1U 0603 10
C147 1U 0603 10
CANTIGA_1p0
+3.3V_RUN
R40 10
+VCC_GMCH_L
D5
RB751V-40
+1.05V_VCCP
C468 220U
C469 22U 805 4
C134 0.22U 0603 10
C125 0.22U 0603 10
C22 0.1U
Layout Note:
370 mils from edge.
Layout Note:
Inside GMCH cavity.
+1.8V_SUS
C104 0.1U
C41 220U
VCC_SM
C122 22U 805 4
C123 22U 805 4
Layout Note:
Place C195 where LVDS
and DDR2 taps.
Layout Note:
Place on the edge.
+1.05V_VCCP
C62 *0.1U_NC
C99 *0.1U_NC
C110 *0.1U_NC
C90 *0.1U_NC
C100 *0.1U_NC
C78 *0.1U_NC
C25 *0.1U_NC
U12F
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
VCC CORE
POWER
VCC_NCTF_1
VCC_NCTF_2
VCC_NCTF_3
VCC_NCTF_4
VCC_NCTF_5
VCC_NCTF_6
VCC_NCTF_7
VCC_NCTF_8
VCC_NCTF_9
VCC_NCTF_10
VCC_NCTF_11
VCC_NCTF_12
VCC_NCTF_13
VCC_NCTF_14
VCC_NCTF_15
VCC_NCTF_16
VCC_NCTF_17
VCC_NCTF_18
VCC_NCTF_19
VCC_NCTF_20
VCC_NCTF_21
VCC_NCTF_22
VCC_NCTF_23
VCC_NCTF_24
VCC_NCTF_25
VCC_NCTF_26
VCC_NCTF_27
VCC_NCTF_28
VCC_NCTF_29
VCC_NCTF_30
VCC_NCTF_31
VCC_NCTF_32
VCC_NCTF_33
VCC_NCTF_34
VCC_NCTF_35
VCC_NCTF_36
VCC_NCTF_37
VCC_NCTF_38
VCC_NCTF_39
VCC_NCTF_40
VCC_NCTF_41
VCC_NCTF_42
VCC_NCTF_43
VCC_NCTF_44
VCC NCTF
+1.05V_VCCP
CANTIGA_1p0
UMA: Places R28,R23 to 10 ohm.
Dis: Please R28,R23 to 0 ohm.
QUANTA COMPUTER
Title
Cantiga (VCC,NCTF)
Size
Document Number
VM8G
Rev
1A
Date: Tuesday, February 17, 2009
Sheet 8 of 58


Non-iAMT 45mA MAx.
FB_120ohm+-25%_100mHz
_200mA_0.2ohm DC
+1.05V_VCCP
L1 BLM11A05S 603
+VCCA_HPLL
C9 4.7U 603 6.3
C10 0.1U
L2 BLM11A05S 603
+VCCA_MPLL
R17 0.5/F 603
+VCCA_MPLL_L
C15 0.1U
C471 22U 1206 10
U12H
CANTIGA_1p0
VCCA_CRT_DAC_1
VCCA_CRT_DAC_2
VCCA_DAC_BG
VSSA_DAC_BG
CRT
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
PLL
VCCA_LVDS
VSSA_LVDS
LVDS
+1.5V_RUN
C491 0.1U
VCCA_PEG_BG
+VCCA_PEG_PLL
VCCA_PEG_PLL
A PEG
POWER
VCCA_SM_1
VCCA_SM_2
VCCA_SM_3
VCCA_SM_4
VCCA_SM_5
VCCA_SM_6
VCCA_SM_7
VCCA_SM_8
VCCA_SM_9
A SM
+1.05V_VCCP
R11 0 603
C46 4.7U 603 6.3
C12 22U 805 4
C11 22U 805 4
C66 1U 0603 10
+VCCA_SM
L5 1uH/300mA
C95 22U 805 4
C79 1U 0603 10
C96 1U 0603 10
C86 0.1U
+VCCA_SM_CK
VCCA_SM_CK_1
VCCA_SM_CK_2
VCCA_SM_CK_3
VCCA_SM_CK_4
VCCA_SM_CK_5
VCCA_SM_CK_NCTF_1
VCCA_SM_CK_NCTF_2
VCCA_SM_CK_NCTF_3
VCCA_SM_CK_NCTF_4
VCCA_SM_CK_NCTF_5
VCCA_SM_CK_NCTF_6
VCCA_SM_CK_NCTF_7
VCCA_SM_CK_NCTF_8
A CK
VCCA_TV_DAC_1
VCCA_TV_DAC_2
TV
+VCC_HDA
VCC_HDA
HDA
VCCD_TVDAC
+VCCD_QDAC
VCCD_QDAC
C17 0.1U
+VCCA_MPLL
C495 0.1U
+VCCD_PEG_PLL
VCCD_HPLL
VCCD_PEG_PLL
D TV/CRT
VCCD_LVDS_1
VCCD_LVDS_2
LVDS
VTT
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT_14
VTT_15
VTT_16
VTT_17
VTT_18
VTT_19
VTT_20
VTT_21
VTT_22
VTT_23
VTT_24
VTT_25
+1.05V_VCCP
C48 2.2U 0603 10
C34 4.7U 603 6.3
C58 0.47U 6.3
C31 4.7U 603 6.3
+ C467 220U
Close to VTT
Place on the edge.
AXF
VCC_AXF_1
VCC_AXF_2
VCC_AXF_3
+VCC_AXF
SM CK
VCC_SM_CK_1
VCC_SM_CK_2
VCC_SM_CK_3
VCC_SM_CK_4
+VCC_SM_CK
L3 0
Reserved L5 pad for inductor.
C63 1U 0603 10
C73 10U 603 6.3
L4 805 1uH/300MA
+1.8V_SUS
C57 0.1U
R29 1/F 603
+VCC_SM_CK_L
C38 10U 603 6.3
HV
VCC_TX_LVDS
VCC_HV_1
VCC_HV_2
VCC_HV_3
+3.3V_RUN
C481 0.1U
PEG
VCC_PEG_1
VCC_PEG_2
VCC_PEG_3
VCC_PEG_4
VCC_PEG_5
+VCC_PEG
R280 0 1206
+1.05V_VCCP
+ C496 220U
C497 22U 1206 10
C494 4.7U 603 6.3
DMI
VCC_DMI_1
VCC_DMI_2
VCC_DMI_3
VCC_DMI_4
+VCC_RXR_DMI
L38 91nH/1.5A
C493 0.1U
VTTLF
VTTLF1
VTTLF2
VTTLF3
+VTTLF1
+VTTLF2
+VTTLF3
+1.05V_VCCP
L37 BLM21P221SGPT 805
+VCCA_PEG_PLL
FB_220ohm+-25%_100MHz
_2A_0.1ohm DC
R279 1/F 603
C492 10U 603 6.3
+1.5V_RUN
L33 BLM18PG181SN1D 603
+VCCD_QDAC
C484 0.1U
C106 0.01U 25
+1.05V_VCCP
L39 BLM21P221SGPT 805
+VCCD_PEG_PLL
FB_220ohm+-25%_100MHz
_2A_0.1ohm DC
R281 1/F 603
C501 10U 603 6.3
+VTTLF1
+VTTLF2
+VTTLF3
C20 0.47U 0603 10
C18 0.47U 0603 10
C23 0.47U 0603 10
QUANTA COMPUTER
Title
Cantiga (POWER)
Size
Document Number
VM8G
Rev
1A
Date: Tuesday, February 17, 2009
Sheet 9 of 58



QUANTA COMPUTER		
Title	Cantiga (VSS)	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 10 of 58	


32.768KHZ
R375 10M
W2
ICH_RTCX1
ICH_RTCX2
C644 12P/50V
32.768KHZ
C643 12P/50V
+RTC_CELL
R379 332K/F
ICH_INTVRMEN
ICH9M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)
ICH_INTVRMEN
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
ICH9M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
ICH_LAN100_SLP
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
+RTC_CELL
R228 1M
R227 20K
R229 20K
ICH_RTCRST#
ICH_SRTCRST#
ICH_INTRUDER#
C650 1U
C648 1U
U20A
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
ICH9M REV 1.0
Reserved for Intel Nineveh design.
T125 PAD
T83 PAD
T81 PAD
T124 PAD
T75 PAD
T136 PAD
T79 PAD
R382 *10K_NC
R372 24.9/F
+3.3V_SUS
+1.5V_PCIE_ICH
[37] ICH_AZ_CODEC_BITCLK
R349 33
ACZ_BIT_CLK
L51 *22uH_NC 402
C603 *27P/50V_NC
[37] ICH_AZ_CODEC_SYNC
R345 33
ACZ_SYNC
[29,37] ICH_AZ_CODEC_RST#
R328 33
ACZ_RST#
[37] ICH_AZ_CODEC_SDOUT
R333 33
ACZ_SDOUT
Place all series terms close to ICH9 except for SDIN input lines,which should be close to source.
[37] ICH_AZ_CODEC_SDIN0
[35] SATA_ACT#
Master HDD
[33] SATA_RX0-
[33] SATA_RX0+
SATA_TX0- C
SATA_TX0+ C
SATA ODD
[33] SATA_RX1-
[33] SATA_RX1+
SATA_TX1- C
SATA_TX1+ C
[33] SATA_TX0-
[33] SATA_TX0+
C587 0.01U
C586 0.01U
SATA_TX0- C
SATA_TX0+ C
[33] SATA_TX1-
[33] SATA_TX1+
C368 0.01U
C367 0.01U
SATA_TX1- C
SATA_TX1+ C
SATA TX/RX capacitor need near to the connector.
LPC_LAD0 [29,31]
LPC_LAD1 [29,31]
LPC_LAD2 [29,31]
LPC_LAD3 [29,31]
LPC_LFRAME# [29,31]
SIO_A20GATE [29]
H_A20M# [3]
H_DPRSTP# [3,6,44]
H_DPSLP# [3]
H_FERR# [3]
H_PWRGOOD [3]
H_IGNNE# [3]
H_INIT# [3]
H_INTR [3]
SIO_RCIN# [29]
H_NMI [3]
H_SMI# [3]
H_STPCLK# [3]
H_THERMTRIP# [3,6]
CLK_PCIE_SATA# [17]
CLK_PCIE_SATA [17]
Place within 500mils of ICH9 ball
+1.05V_VCCP
R335 *56_NC
R343 *56_NC
R332 56
+3.3V_RUN
R357 8.2K
R364 10K
R341 56
XOR Chain Entrance Strap
ICH RSVD | HDA SDOUT | Description
0 | 0 | RSVD
0 | 1 | Enter XOR Chain
1 | 0 | Normal Operation (Default)
1 | 1 | Set PCIE port config bit 1
+3.3V_RUN
R340 *1K_NC
R387 *1K_NC
ACZ_SDOUT
ICH_RSVD [13]
QUANTA COMPUTER
Title: ICH9-M (CPU,SATA,LPC,LAN,CODEC)
Size
Document Number: VM8G
Rev: 1A
Date: Tuesday, February 17, 2009
Sheet 11 of 58

Place TX DC blocking caps close ICH9.

[31] PCIE_TX2-
[31] PCIE_TX2+
C622 0.1U PCIE_TXN2_C
C623 0.1U PCIE_TXP2_C

[28] PCIE_TX4-
[28] PCIE_TX4+
C629 0.1U PCIE_TXN4_C
C631 0.1U PCIE_TXP4_C

[38] PCIE_TX5-
[38] PCIE_TX5+
C445 0.1U PCIE_TXN5_C
C448 0.1U PCIE_TXP5_C

[39] PCIE_TX6-/GLAN_TX-
[39] PCIE_TX6+/GLAN_TX+
C637 0.1U GLAN_TXN_C
C645 0.1U GLAN_TXP_C

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

U20D

MiniWWAN
[31] PCIE_RX2-
[31] PCIE_RX2+
PCIE_TXN2_C
PCIE_TXP2_C

MiniWLAN

MiniWPAN

[28] PCIE_RX4-
[28] PCIE_RX4+
PCIE_TXN4_C
PCIE_TXP4_C

Express Card

[38] PCIE_RX5-
[38] PCIE_RX5+
PCIE_TXN5_C
PCIE_TXP5_C

1394+Cardreader

[39] PCIE_RX6-/GLAN_RX-
[39] PCIE_RX6+/GLAN_RX+
GLAN_TXN_C
GLAN_TXP_C

Giga Bit LOM

PCI-Express / Direct Media Interface

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP

DMI0RXN DMI0RXP DMI0TXN DMI0TXP
DMI1RXN DMI1RXP DMI1TXN DMI1TXP
DMI2RXN DMI2RXP DMI2TXN DMI2TXP
DMI3RXN DMI3RXP DMI3TXN DMI3TXP
DMI_CLKN DMI_CLKP
DMI_ZCOMP DMI_IRCOMP

DMI_MTX_IRX_N0 [6]
DMI_MTX_IRX_P0 [6]
DMI_MRX_ITX_N0 [6]
DMI_MRX_ITX_P0 [6]
DMI_MTX_IRX_N1 [6]
DMI_MTX_IRX_P1 [6]
DMI_MRX_ITX_N1 [6]
DMI_MRX_ITX_P1 [6]
DMI_MTX_IRX_N2 [6]
DMI_MTX_IRX_P2 [6]
DMI_MRX_ITX_N2 [6]
DMI_MRX_ITX_P2 [6]
DMI_MTX_IRX_N3 [6]
DMI_MTX_IRX_P3 [6]
DMI_MRX_ITX_N3 [6]
DMI_MRX_ITX_P3 [6]
CLK_PCIE_ICH# [17]
CLK_PCIE_ICH [17]

DMI_COMP R350 24.9/F +1.5V_PCIE_ICH
Place within 500mils of ICH9

SPI
SPI_CLK_R SPI_CS#0_R ICH_SPI_CS1#_R
T127 PAD T128 PAD T139 PAD
SPI_CLK SPI_CS0# SPI_CS1#/GPIO58/CLGPIO6
SPI_MOSI_R SPI_MISO_R
T129 PAD T70 PAD
SPI_MOSI SPI_MISO

USB
[32] USB_OC0_1#
[38] USB_OC_3#
OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8#/GPIO44 OC9#/GPIO45 OC10#/GPIO46 OC11#/GPIO47

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P

ICH_USBP0- [32]
ICH_USBP0+ [32]
ICH_USBP1- [32]
ICH_USBP1+ [32]
ICH_USBP2- [38]
ICH_USBP2+ [38]
ICH_USBP3- [38]
ICH_USBP3+ [38]
ICH_USBP4- [25]
ICH_USBP4+ [25]
ICH_USBP6- [31]
ICH_USBP6+ [31]
ICH_USBP7- [28]
ICH_USBP7+ [28]
ICH_USBP8- [31]
ICH_USBP8+ [31]

R348 22.6/F USBRBIAS
Places within 500 mils of the ICH9
USBRBIAS USBRBIAS#

ICH9M REV 1.0

Side Pair Left
Side Pair Left
Side Pair Right
Side Pair Right
Camera
Mini Card (WWAN)
Bluetooth
Express Card
Mini Card (WLAN)

PCI Pullups

RP40 +3.3V_RUN
PCI_FRAME# PCI_TRDY# PCI_DEVSEL# PCI_REQ1# +3.3V_RUN
PCI_PLOCK# PCI_STOP# PCI_PIRQD# PCI_PERR#

RP39 +3.3V_RUN
PCI_IRDY# PCI_PIRQC# PCI_PIRQE# PCI_PIRQB# +3.3V_RUN
PCI_PIRQA# PCI_REQ0# ICH_IRQH_GPIO5 PCI_SERR#

PCI_REQ2# R383 8.2K +3.3V_RUN

RP38 +3.3V_SUS
OC7# OC6# OC5# OC4# +3.3V_SUS
OC9# USB_OC_3# USB_OC0_1# OC8#
10KX8
OC10# R363 10K
OC11# R354 10K +3.3V_SUS

+3.3V_RUN
SB_WLAN_PCIE_RST# R368 8.2K
SB_NB_PCIE_RST# R369 8.2K
SB_LOM_PCIE_RST# R223 8.2K
BIOS should not enable the internal GPIO pull up resistor.

U20B

PCI
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
REQ0# GNT0# REQ1#/GPIO50 GNT1#/GPIO51 REQ2#/GPIO52 GNT2#/GPIO53 REQ3#/GPIO54 GNT3#/GPIO55
C/BE0# C/BE1# C/BE2# C/BE3#
IRDY# PAR PCIRST# DEVSEL# PERR# PLOCK# SERR# STOP# TRDY# FRAME#
PLTRST# PCICLK PME#

PCI_REQ0# PCI_GNT0# PCI_REQ1# PCI_GNT1# PCI_REQ2# PCI_GNT2# PCI_GNT3#
PAD T126
PAD T135
PAD T82
PAD T74
SB_LOM_PCIE_RST# [39]
Add SB_LOM_PCIE_RST#

PCI_IRDY# PCI_DEVSEL# PCI_PERR# PCI_PLOCK# PCI_SERR# PCI_STOP# PCI_TRDY# PCI_FRAME#

PLTRST# CLK_PCI_ICH
PLTRST# [6,18,28,29,31,38,39]
CLK_PCI_ICH [17]

Interrupt I/F
PCI_PIRQA# PCI_PIRQB# PCI_PIRQC# PCI_PIRQD#
PIRQA# PIRQB# PIRQC# PIRQD#
PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5
PCI_PIRQE# SB_WLAN_PCIE_RST# SB_NB_PCIE_RST# ICH_IRQH_GPIO5
SB_WLAN_PCIE_RST# [31]
SB_NB_PCIE_RST# [6]
PAD T72

ICH9M REV 1.0

CLK_PCI_ICH
R370 *10_NC
C634 *8.2P_NC
Reserved for EMI.Place resister and cap close to ICH.

QUANTA COMPUTER

Title	ICH9-M (USB,DMI,PCIE,PCI)		
Size	Document Number VM8G		Rev 1A
Date:	Tuesday, February 17, 2009	Sheet 12 of 58	

Non-iAMT

+3.3V_SUS

RP43 2.2KX2: ICH_SMBDATA, ICH_SMBCLK

Non-iAMT ASF 2.0

+3.3V_SUS

RP41 *10KX2_NC: ICH_SMLINK0, ICH_SMLINK1

ICH_SMBCLK R230 0 ICH_SMLINK0

ICH_SMBDATA R380 0 ICH_SMLINK1

Non-iAMT

+3.3V_SUS

R386 10K RSV_ICH_CL_RST1#

R242 10K ICH_RI#

R381 10K SIO_EXT_SCI#

R384 1K PCIE_WAKE#

Place these close to ICH9.

CLK_ICH_48M — R347 *10_NC — C600 *4.7P_NC — 50

CLK_ICH_14M — R371 *10_NC — C635 *4.7P_NC — 50

+3.3V_RUN

R331 8.2K

U20C

SMBCLK G16 — [28] ICH_SMBCLK — ICH_SMBCLK

SMBDATA A13 — [28] ICH_SMBDATA — ICH_SMBDATA

LINKALERT#/GPIO60/CLGPIO6 E17 — T146 PAD — RSV_ICH_CL_RST1#

SMLINK0 C17 — T140 PAD — ICH_SMLINK0

SMLINK1 B18 — T145 PAD — ICH_SMLINK1

RI# F19 — ICH_RI#

SUS_STAT#/LPCPD# R4 — T122 PAD — RSV_LPCPD#

SYS_RESET# G19 — +3.3V_SUS — R232 1K

PMSYNC#/GPIO0 M6 — [6] PM_BMBUSY#

SMBALERT#/GPIO11 A17 — [31] USB_MCARD1_DET# — USB_MCARD1_DET# — R378 0

STP_PCI#/GPIO15 A14 — [17] H_STP_PCI#

STP_CPU#/GPIO25 E19 — [17] H_STP_CPU#

CLKRUN#/GPIO32 L4 — [29] CLKRUN# — CLKRUN#

WAKE# E20 — [28,31,39] PCIE_WAKE# — PCIE_WAKE#

SERIRQ M5 — [29] IRQ_SERIRQ — IRQ_SERIRQ

THRM# AJ23 — [3] THERM_ALERT# — THERM_ALERT#

VRMPWRGD D21 — [29,44] IMVP_PWRGD — IMVP_PWRGD

TP8 A20 — T134 PAD

TACH1/GPIO1 AG19 — T118 PAD

TACH2/GPIO6 AH21 — T111 PAD

TACH3/GPIO7 AG21 — [29] SIO_EXT_WAKE#

GPIO8 A21 — [29] SIO_EXT_SMI# — SIO_EXT_SMI#

LANPHYPC/GPIO12 C12 — [29] SIO_EXT_SCI# — SIO_EXT_SCI#

ENGDET/GPIO13 C21 — T141 PAD

TACH0/GPIO17 AE18 — T117 PAD

GPIO18 K1 — [31] PCIE_MCARD1_DET# — PCIE_MCARD1_DET# — R361 4.7K

GPIO20 AF8 — T108 PAD

SCLOCK/GPIO22 AJ22 — T116 PAD

QRT_STATE0/GPIO27 A9 — T143 PAD

QRT_STATE1/GPIO28 D19 — T71 PAD

SATACLKREQ#/GPIO35 L1 — [17] SATA_CLKREQ#

SLOAD/GPIO38 AE19 — [18] PLTRST_DELAY# — PLTRST_DELAY#

SDATAOUT0/GPIO39 AG22 — T112 PAD

SDATAOUT1/GPIO48 AF21 — T119 PAD

GPIO49 AH24 — T115 PAD

GPIO57/CLGPIO5 A8 — T144 PAD

SPKR M7 — [37] SPKR — SPKR

MCH_SYNC# AJ24 — [6] MCH_ICH_SYNC# — MCH_ICH_SYNC# — R336 0

TP3 B21 — [11] ICH_RSVD

TP9 AH20 — T114 PAD — TP9

TP10 AJ20 — T113 PAD — TP10

TP11 AJ21 — T110 PAD — TP11

SATA0GP/GPIO21 AH23

SATA1GP/GPIO19 AE19

SATA4GP/GPIO36 AE21

SATA5GP/GPIO37 AD20

CLK14 H1 — CLK_ICH_14M — CLK_ICH_14M [17]

CLK48 AF3 — CLK_ICH_48M — CLK_ICH_48M [17]

SUSCLK P1 — ICH_SUSCLK — PAD T123

SLP_S3# C16 — SIO_SLP_S3# [29]

SLP_S4# E16 — PAD T78

SLP_S5# G17 — SIO_SLP_S5# [29]

S4_STATE#/GPIO26 C10

PWROK G20 — PWROK — PWROK [6,29]

DPRSLPVR/GPIO16 M2 — DPRSLPVR — DPRSLPVR [6,44]

BATLOW# B13 — ICH_BATLOW# — R377 8.2K — +3.3V_SUS

PWRBTN# R3 — SIO_PWRBTN# [29]

LAN_RST# D20 — RSV_ICH_LAN_RST# — PAD T84

RSMRST# D22 — ICH_RSMRST# — ICH_RSMRST# [29]

CK_PWRGD R5 — CLK_PWRGD [17]

CLPWROK R6 — ICH_CL_PWROK — ICH_CL_PWROK [6,29]

SLP_M# B16 — PAD T131

CL_CLK0 F24 — CL_CLK0 [6]

CL_CLK1 B19 — RSV_ICH_CL_CLK1 — PAD T133

CL_DATA0 F22 — CL_DATA0 [6]

CL_DATA1 C19 — RSV_ICH_CL_DATA1 — PAD T132

CL_VREF0 C25 — CL_VREF0

CL_VREF1 A19

CL_RST0# F21 — ICH_CL_RST0# [6]

CL_RST1# D18 — CL_RST1# — PAD T77

MEM_LED/GPIO24 A16 — RSV_GPIO24 — PAD T137

ALERT#/GPIO10 C18 — RSV_GPIO10 — PAD T73

NETDETECT/GPIO14 C11 — RSV_GPIO14 — PAD T142

WOL_EN/GPIO9 C20 — RSV_WOL_EN — PAD T76

R243 8.2K — +3.3V_SUS

SMB | SATA GPIO | Clocks | SYS GPIO | Power MGT | GPIO | Controller Link | MISC

ICH9M REV 1.0

Non-iAMT

PWROK — R245 10K

DPRSLPVR — R358 100K

ICH_RSMRST# — R226 10K

RSV_ICH_LAN_RST# — R246 10K

ICH_CL_PWROK — R360 1M

+3.3V_SUS

RSV_GPIO10 — R244 10K

Option to " Disable " clkrun. Pulling it down will keep the clks running.

+3.3V_RUN

R366 8.2K — CLKRUN#

R367 *10_NC

R330 10K PLTRST_DELAY#

+3.3V_RUN

R365 100K PCIE_MCARD1_DET#

+3.3V_RUN

R337 *10K_NC MCH_ICH_SYNC# R

R355 10K IRQ_SERIRQ

R338 10K THERM_ALERT#

+3.3V_SUS

R385 10K RSV_WOL_EN

R231 10K SIO_EXT_SMI#

R376 100K USB_MCARD1_DET#

+3.3V_RUN

R356 *1K_NC — SPKR

No Reboot strap.

SPKR	Low = Default. High = No Reboot.

SMbus address D2

These are for backdrive issue.

+3.3V_RUN

RP42 2.2KX2

[28] ICH_SMBDATA — Q42 2N7002W-7-F — SDATA [15,31]

+3.3V_RUN

[28] ICH_SMBCLK — Q41 2N7002W-7-F — SCLK [15,31]

Non-iAMT

+3.3V_RUN

R389 3.24K/F

CL_VREF0

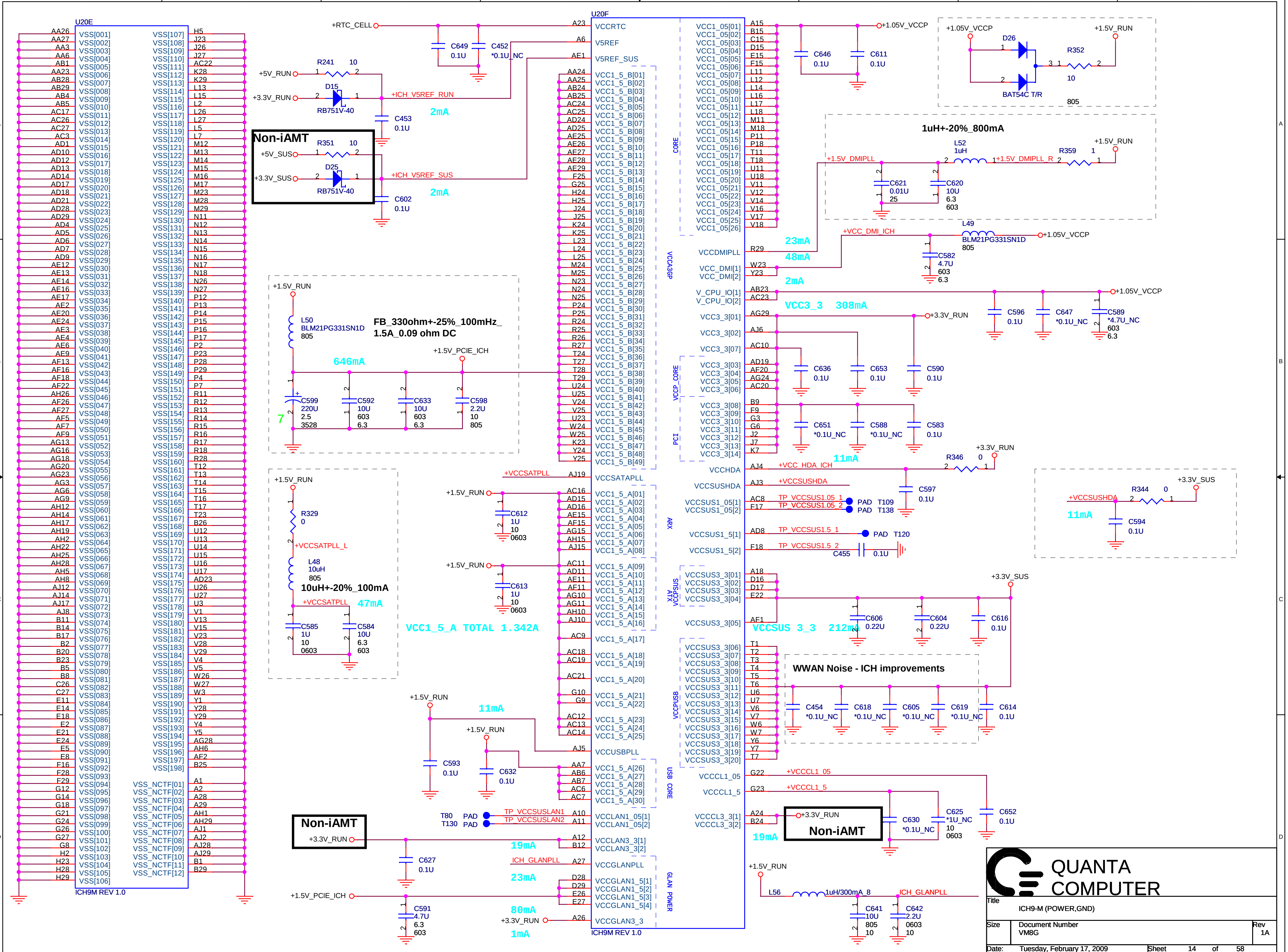
C456 0.1U

R388 453/F

CL_VREF0/1 ~=0.405V

QUANTA COMPUTER

Title	ICH9-M (PM,GPIO,SMB,CL)	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 13 of 58	



QUANTA COMPUTER

Title: ICH9-M (POWER,GND)

Size	Document Number	Rev
	VM8G	1A

Date: Tuesday, February 17, 2009 — Sheet 14 of 58

A is required to route to Top SoDIMM for AMTto function.
Ch.A SODIMM needs to be populated for Intel AMT support.

PC4800 DDR2 SDRAM SO-DIMM (200P)

CN4

DDR2_SODIMM

CLOCK 0,1
CKE 0,1

SMbus address A0

CN3

2-1734073-2

CLOCK 2,3
CKE 2,3

SMbus address A4

Non-iAMT

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

Place these Caps near So-Dimm1.

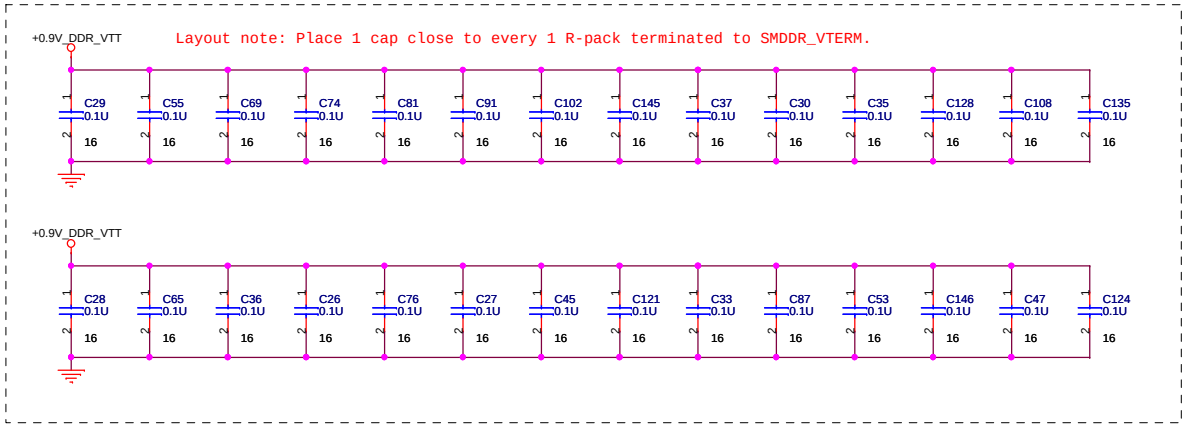
Place these Caps near So-Dimm2.

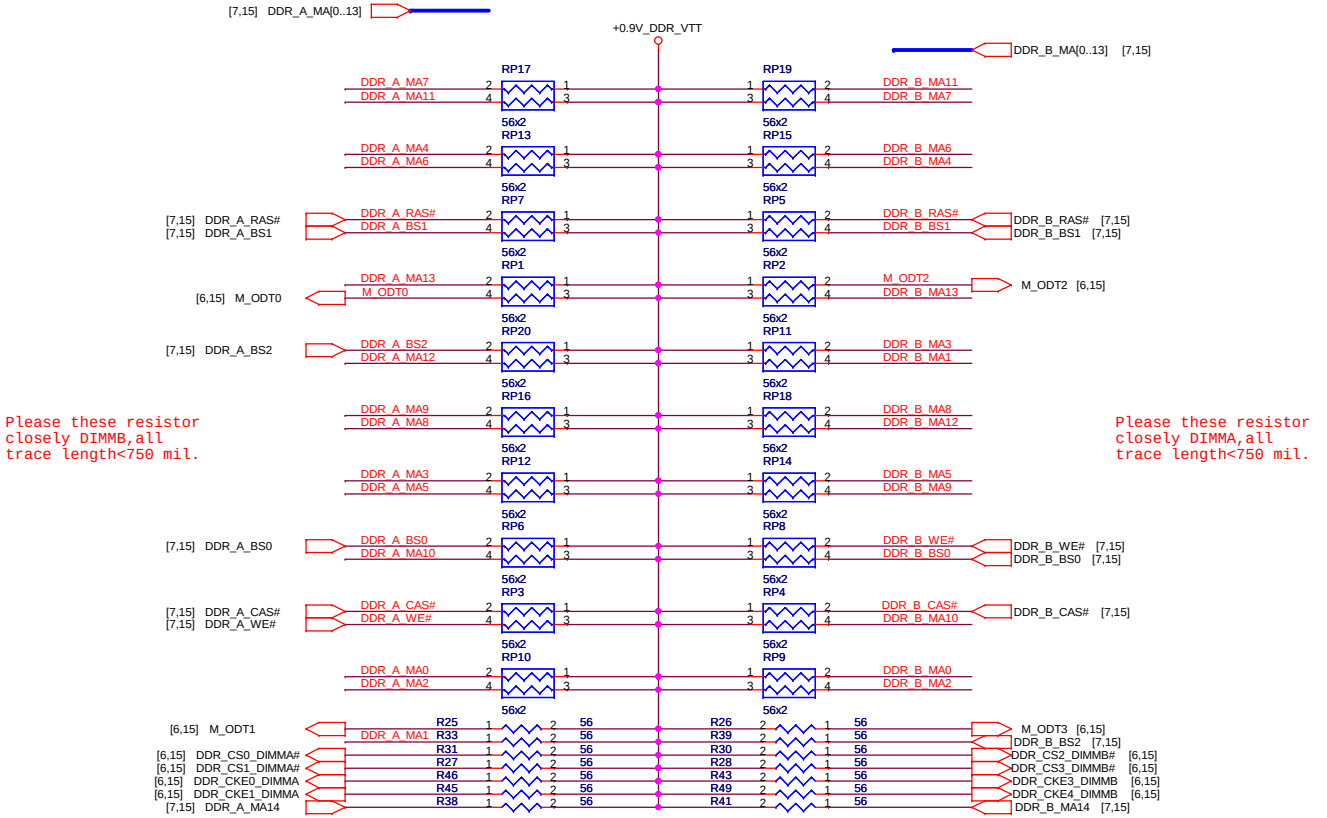
QUANTA COMPUTER

Title: DDR2 SO-DIMM (200P) X 2

Size: | Document Number: VM8G | Rev: 1A

Date: Tuesday, February 17, 2009 | Sheet 15 of 58





Please these resistor closely DIMMB,all trace length<750 mil.

Please these resistor closely DIMMA,all trace length<750 mil.

QUANTA COMPUTER

Title	DDR2 RES ARRAY	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 16 of 58	

Add capacitor pads for improving WWAN.

C391 20P 50 FSA
C361 1 2 *27P_NC 50 FSC
C380 1 2 *27P_NC 50 PCI_SIO
C386 1 2 *27P_NC 50 PCI_ICH

Y2
CLK_XTAL_IN 1 2 CLK_XTAL_OUT
14.318MHZ
C359 33P 50
C360 33P 50
14.318MHz

U8
CK505
QFN64
SLG8SP513V

+CK_VDD_PCI 9 VDD_PCI
4 VDD_REF
+CK_VDD_PLL3 23 VDD_PLL3
+CK_VDD_48 16 VDD_48
+CK_VDD_SRC 46 VDD_SRC
62 VDD_CPU
+CK_VDD_MAIN 19 VDD_IO
27 VDD_IO
33 VDD_IO
43 VDD_IO
52 VDD_IO
56 VDD_IO
15 GND
18 GND
22 GND
26 GND
30 GND
36 GND
49 GND
59 GND
1 GND

CPU-0 61 CPU_BCLK
CPU-0# 60 CPU_BCLK#
CPU-1 58 MCH_BCLK
CPU-1# 57 MCH_BCLK#
SRC-8/CPU_ITP 54 PCIE_MINI1
SRC-8#/CPU_ITP# 53 PCIE_MINI1#
SRC-0/DOT96 20 SRC0
SRC-0#/DOT96# 21 SRC0#
SRC-1/SE1 24 27M_NSS
SRC-1#/SE2 25 27M_SS
SRC-2/SATA 28 PCIE_SATA
SRC-2#/SATA# 29 PCIE_SATA#
CR#_C/SRC-3 31 PCIE_CARD
CR#_D/SRC-3# 32 PCIE_CARD#
SRC-4 34 MCH_3GPLL
SRC-4# 35 MCH_3GPLL#
PCI_STOP#/SRC-5 45
CPU_STOP#/SRC5-5# 44
SRC-6 48 PCIE_EXPCARD
SRC-6# 47 PCIE_EXPCARD#
CR#_F/SRC-7 51 MINI1CLK_REQ#_C
CR#_E/SRC-7# 50 CARD_CLK_REQ#_C
SRC-9 37
SRC-9# 38
SRC-10 41 PCIE_ICH
SRC-10# 42 PCIE_ICH#
CR#_H/SRC-11 40 PCIE_LOM
CR#_G/SRC-11# 39 PCIE_LOM#
GND 65

RP26 0x2: CLK_CPU_BCLK [3], CLK_CPU_BCLK# [3]
RP27 0x2: CLK_MCH_BCLK [5], CLK_MCH_BCLK# [5]
RP28 0x2: CLK_PCIE_MINI1 [31], CLK_PCIE_MINI1# [31]
RP34 0x2: CLK_PCIE_VGA [18], CLK_PCIE_VGA# [18]
RP35 0x2: CLK_VGA_27M_NSS [19], CLK_VGA_27M_SS [19]
RP36 0x2: CLK_PCIE_SATA [11], CLK_PCIE_SATA# [11]
RP33 0x2: CLK_PCIE_CARD [38], CLK_PCIE_CARD# [38]
RP32 0x2: CLK_MCH_3GPLL [6], CLK_MCH_3GPLL# [6]
H_STP_PCI# [13], H_STP_CPU# [13]
RP29 0x2: CLK_PCIE_EXPCARD [28], CLK_PCIE_EXPCARD# [28]
Express Card
R145 475/F MINI1CLK_REQ# → MINI1CLK_REQ# [31]
R146 475/F CARD_CLK_REQ# → CARD_CLK_REQ# [28]
RP30 0x2: CLK_PCIE_ICH [12], CLK_PCIE_ICH# [12]
RP31 0x2: CLK_PCIE_LOM [39], CLK_PCIE_LOM# [39]

[13] SATA_CLKREQ# → SATA_CLKREQ# R164 475/F
[6] CLK_3GPLLREQ# → CLK_3GPLLREQ# R166 475/F
[31] CLK_LPC_DEBUG → CLK_LPC_DEBUG R168 33
[29] CLK_PCI_8512 → CLK_PCI_8512 R169 33
[12] CLK_PCI_ICH → CLK_PCI_ICH R171 33
[13] CLK_ICH_48M → CLK_ICH_48M R178 33
[3,6] CPU_MCH_BSEL0 → R181 2.2K
[3,6] CPU_MCH_BSEL1 → R143 0
[3,6] CPU_MCH_BSEL2 → R161 10K
[13] CLK_ICH_14M → CLK_ICH_14M R162 33
[13] CLK_PWRGD

SATA_CLKREQ#_C
CLK_3GPLLREQ#_C
PCI_PCCARD
PCI_SIO
27M_SEL
PCI_ICH

FSA 17 FSA/USB48
FSB 64 FSB/TEST_MODE
FSC 5 FSC/TEST_SEL/REF
55 RESET#
63 CK_PWRGD/PD#
CLK_XTAL_OUT 2 XOUT
CLK_XTAL_IN 3 XIN
[3,25,29] SMBDAT1 → SMBDAT1 6 SDATA
[3,25,29] SMBCLK1 → SMBCLK1 7 SCLK

CR#_A/PCI-0
CR_B/PCI-1
TME/PCI-2
SRC5_EN/PCI-3
27M_SEL/PCI-4
ITP_EN/PCIF-5#

+3.3V_RUN
H_STP_PCI# R156 10K
H_STP_CPU# R160 10K

+3.3V_RUN
CLK_3GPLLREQ# R165 10K
SATA_CLKREQ# R163 10K
MINI1CLK_REQ# R144 10K

PCI_SIO R167 *10K_NC

+3.3V_RUN
R172 *10K_NC
PCI_ICH
R173 10K

+3.3V_RUN
R170 10K
27M_SEL

ITP_EN

PCI_ICH	10K-pull
0	Disable
1	Enable

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

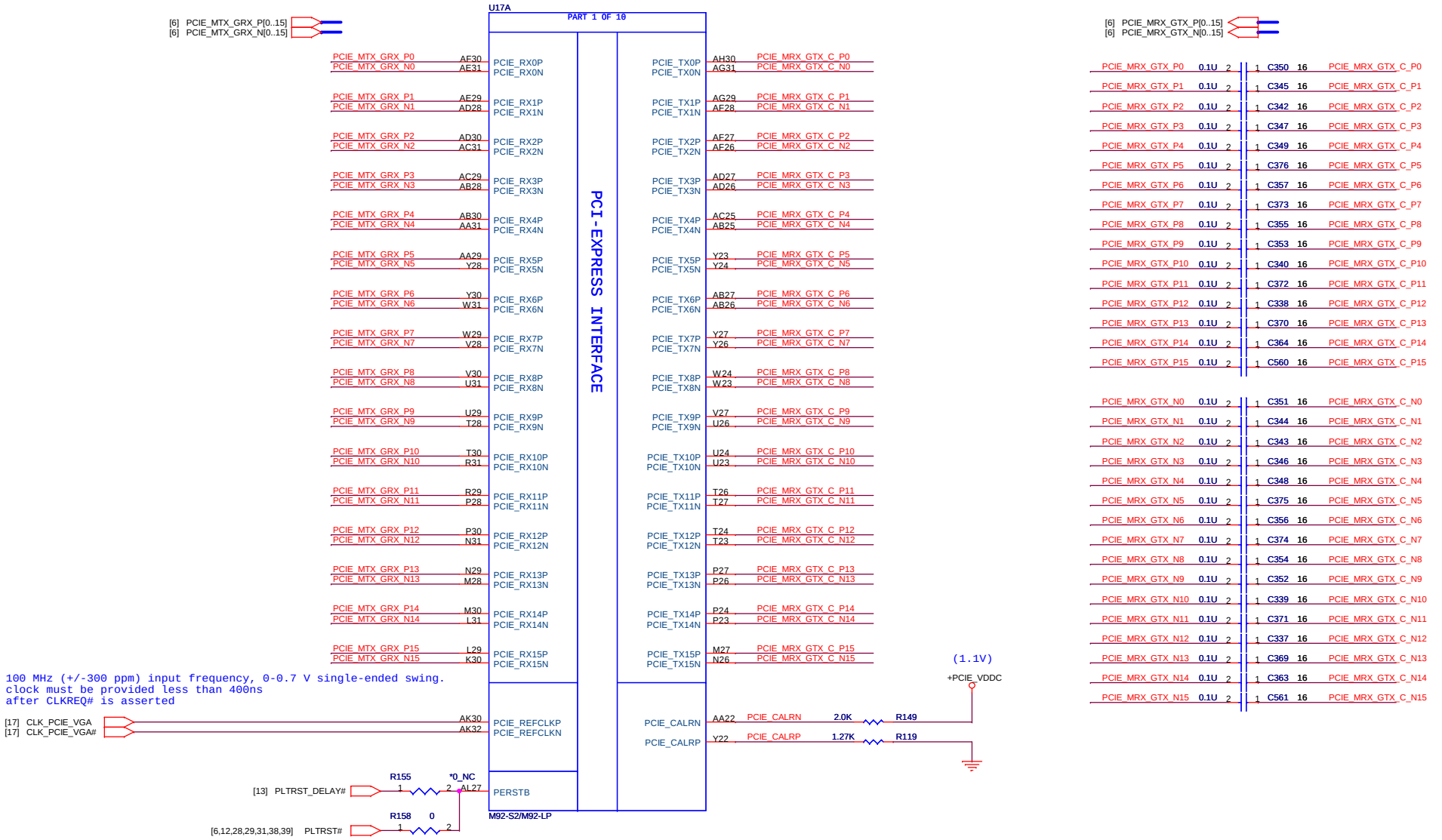
UMA without iAMT

+3.3V_RUN
L25 BLM21PG600SN1D 805 120 ohms@100Mhz
+CK_VDD_MAIN
C329 0.1U 16
C328 0.1U 16
C366 0.1U 16
C382 0.1U 16
C395 0.1U 16
C394 0.1U 16
C387 *10U_NC 603 6.3 16

L24 BLM21PG600SN1D 805 120 ohms@100Mhz
R134 2.2 +CK_VDD_PCI
C331 0.1U 16
R179 2.2 +CK_VDD_PLL3
C393 0.1U 16
R175 2.2 +CK_VDD_48
C390 0.1U 16
C398 4.7U 603 6.3
R140 2.2 +CK_VDD_SRC
C327 0.1U 16

QUANTA COMPUTER

Title	CLOCK GENERATOR	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 17 of 58	



QUANTA COMPUTER

Title	M92-S2_PCIE	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 18 of 58	

MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB		0	0	0
256MB		0	0	1
64MB		0	1	0
512MB		1	0	0

2

+3.3V_DELAY

2

R296 1 2 *10K_NC RAM_CFG0
R289 1 2 *10K_NC RAM_CFG1
R287 1 2 10K_NC RAM_CFG2

GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	FM8 setting
GPIO0	GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable) 0 : Default. (Driver Controlled Gen2) 1 : Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO_5_AC_BATT 0 : Battery saving mode = 0.0 V 1 : AC (Performance mode) = 3.3 V	0
GPIO6	ATI Internal use only	0

+3.3V_DELAY

R288 1 2 *10K_NC GPIO0
R293 1 2 *10K_NC GPIO1
R93 1 2 *10K_NC GPIO2
R294 1 2 *10K_NC GPIO3
R291 1 2 *10K_NC GPIO4
R91 1 2 *10K_NC GPIO5
R90 1 2 *10K_NC GPIO6

R298 1 2 *10K_NC TEMP_FAIL#
R290 1 2 10K GFX_CLKREQ#
R128 1 2 10K VGASYNC
R124 1 2 10K VGAHSYNC

R131 1 2 *10K_NC VGASYNC
R117 1 2 *10K_NC VGAHSYNC
R299 1 2 10K TEMP_FAIL#

+1.8V_RUN

52

R95 1 2 *10K_NC RAM_TYPE_CFG0
R300 1 2 10K RAM_TYPE_CFG1
R292 1 2 *10K_NC RAM_TYPE_CFG2
R301 1 2 *10K_NC RAM_TYPE_CFG3

Memory Straps	RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Vendor PN
500MHz 512MB(64M*16) Hynix	0	0	1	0	AKD5LG-TW01(FR)	H5PS1G63EFR-20L
Remove Qimonda Source						
500MHz 512MB(64M*16) Samsung	0	0	0	1	AKD5LG-T507(IE)	K4N1G164QE-HC20
Remove						

52

Q9
SI2303BDS-T1-E3
+3.3V_DELAY
+3.3V_RUN
R94 100K
Q8 2N7002W-7-F
R85 0
C212 *0.1U_NC
16
OPTIONAL RC NETWORK TO FINE TUNE POWER SEQUENCING

[29,42,43,46] RUN_ON R77 0_NC
[29] GFX_ON R78 0
GFX_RUN_ON [49]
C201 *0.1U_NC

OSC_SPREAD R109 *0_NC
[17] CLK_VGA_27M_SS R107 *0_NC CLK_VGA_27M_SSIN_R
R106 *10K_NC
[17] CLK_VGA_27M_NSS R110 100/F R112 120/F R322 0
OSC_OUT R320 *182R_NC
R321 *221/F_NC XTALIN [23]
R313 *1M_NC
Y3 *27MHZ_NC
R319 *0_NC XTALOUT [23]
R317 *1M_NC
C557 *12P_NC
C556 *12P_NC

Spread Spectrum
If U4, the discrete spread spectrum chip is not used, then pop R48 in order to pull-down BXTALOUT for EMI reasons.

+3.3V_RUN
R174 *10K_NC
R177 *10K_NC
R180 *10K_NC
OSC_OUT
OSC_SPREAD
R176 *0_NC
U9
XIN/CLKIN XOUT
VSS VDD
SO PD#
SSCLK REFCLK
*P1819GF-08SR_NC
+3VL
L26 *BLM11A05S_NC
+3.3V_RUN
C388 *10U_NC
905 10
C389 *0.1U_NC
16

	S0
-1.75% (DOWN)	0

As M82 design, for GPIO use

U17B
PART 2 OF 10

DVP PORT
U1 DVPCLK
AC7 DVPCNTL_0
Y2 DVPCNTL_1
U5 DVPCNTL_2
AA1 DVPCNTL_MVP_0
Y4 DVPCNTL_MVP_1
Y7 DVPDATA_0
V2 DVPDATA_1
Y8 DVPDATA_2
W4 DVPDATA_3
AB7 DVPDATA_4
W1 DVPDATA_5
AB8 DVPDATA_6
W3 DVPDATA_7
AB9 DVPDATA_8
W5 DVPDATA_9
AC6 DVPDATA_10
W6 DVPDATA_11
AD7 DVPDATA_12
AA3 DVPDATA_13
AC8 DVPDATA_14
AA5 DVPDATA_15
AE8 DVPDATA_16
AA6 DVPDATA_17
AE9 DVPDATA_18
AB4 DVPDATA_19
AD9 DVPDATA_20
AB2 DVPDATA_21
AC10 DVPDATA_22
AC5 DVPDATA_23

RAM_TYPE_CFG0
RAM_TYPE_CFG1
RAM_TYPE_CFG2
RAM_TYPE_CFG3

I/O
GPIO0 U6 GPIO_0
GPIO1 U10 GPIO_1
GPIO2 T10 GPIO_2
GPIO3 U8 GPIO_3_SMBDATA
GPIO4 U7 GPIO_4_SMBCLK
GPIO5 T9 GPIO_5_AC_BATT
GPIO6 T8 GPIO_6_TACH
T7 GPIO_7_BLON
T46 PAD P10 GPIO_8_ROMSO
T105 PAD P4 GPIO_9_ROMSI
T100 PAD P2 GPIO_10_ROMSCK
N6 GPIO_11
N5 GPIO_12
N3 GPIO_13
T104 PAD Y9 GPIO_14_HPD2
N1 GPIO_15_PWRCNTL_0
M4 GPIO_16_SSIN
R6 GPIO_17_THERMAL_INT
T42 PAD W10 GPIO_18_HPD3
M2 GPIO_19_CTF
P8 GPIO_20_PWRCNTL_1
P7 GPIO_21_BB_EN
T44 PAD N8 GPIO_22_ROMCSB
N7 GPIO_23_CLKREQB
L6 JTAG_TRSTB
T103 PAD L5 JTAG_TDI
T101 PAD L3 JTAG_TCK
T102 PAD L1 JTAG_TMS
T35 PAD K4 JTAG_TDO

[29] PANEL_BKEN
RAM_CFG0
RAM_CFG1
RAM_CFG2
[49] GFX_CORE_CNTRL0 R297 0
[21] THERMAL_INT# R295 *0_NC
[49] GFX_CORE_CNTRL1 R83 0
[20] BB_ENA
CLK_VGA_27M_SSIN_R
TEMP_FAIL#
GFX_CLKREQ#
R286 1K

T48 PAD AB13 GENERICA
T105 PAD W8 GENERICB
T43 PAD W9 GENERICC
T107 PAD W7 GENERICD
T50 PAD AD10 GENERICE_HPD4
T49 PAD AC14 HPD1
AC16 VREFG
+1.8V_RUN
R310 499/F
R311 249/F
C533 0.1U

RESERVED
T45 PAD N10 NC_PWRGOOD
T58 PAD AB22 RSVD#8
T57 PAD AC22 RSVD#9
T40 PAD L9 NC#1
T38 PAD N9 NC#2
T51 PAD AB16 RSVD#3
AB12 RSVD#2
AB11 RSVD#1
[25] ENVDD
[25] BIA_PWM
R159 *0
R157 10K
R154 1K
AF24 TESTEN

M92-S2/M92-LP

DAC1
R AM26 RB AK26
G AL25 GB AJ25
B AH24 BB AG25
HSYNC AH26
VSYNC AJ27
AVDD AG24
AVSSQ AE22
VDD1DI AE23
VSS1DI AD23
RSET AD22 R116 499R

VGA_RED [26]
VGA_GRN [26]
VGA_BLU [26]
VGAHSYNC [26]
VGAVSYNC [26]
+1.8V_RUN
L45 BLM15BD121SN1D
C545 0.01U C546 0.1U C547 1U C544 4.7uF
+AVDD
L43 BLM15BD121SN1D
C537 0.01U C536 0.1U C535 1U
+VDD1DI
Place very close to ASIC balls.

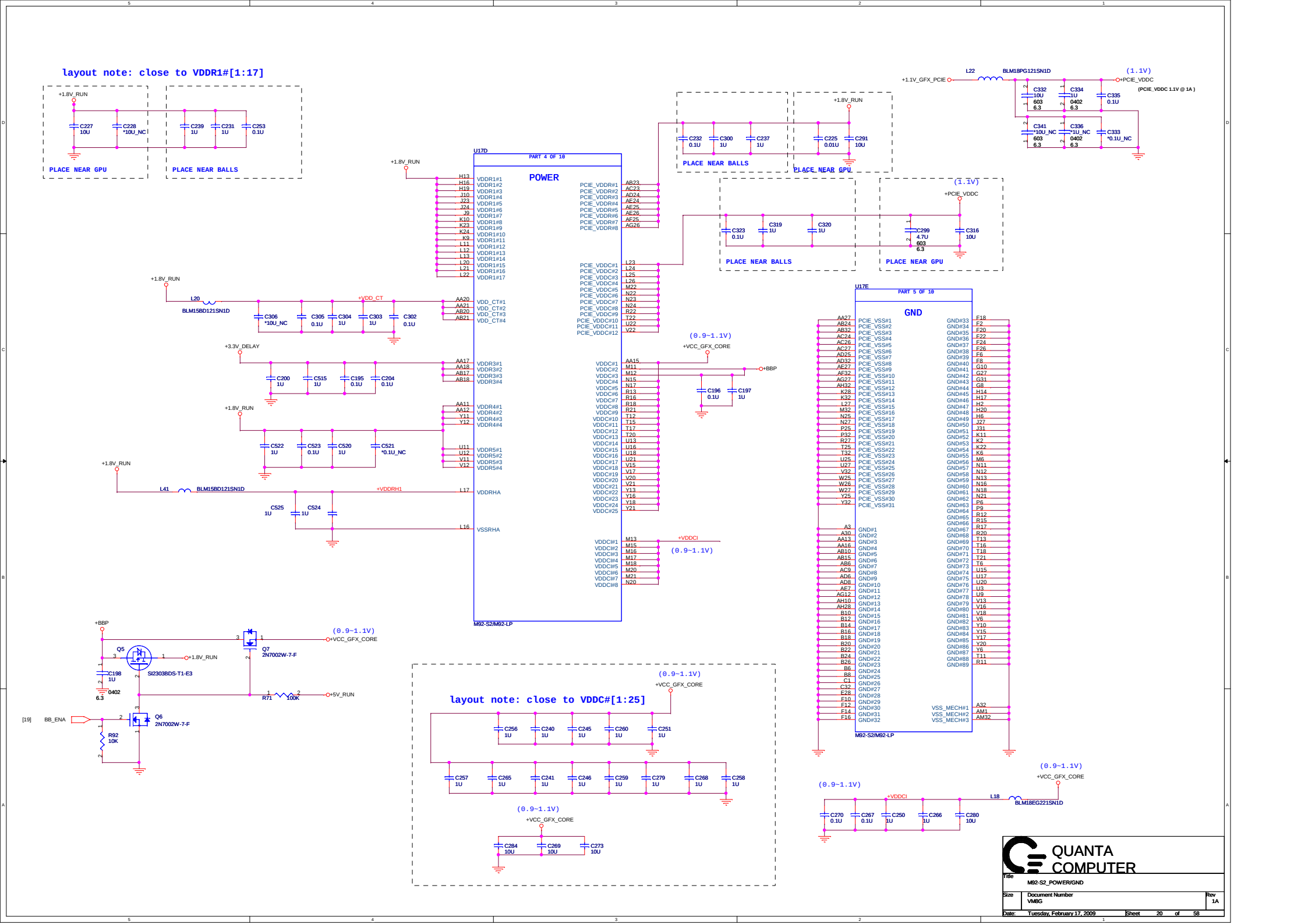
DAC2
R2 AM12 R2B AK12
G2 AL11 G2B AJ11
B2 AK10 B2B AL9
H2SYNC AL13
V2SYNC AJ13
C AH12
Y AM10
COMP AJ9
A2VDD AE20
A2VDDQ AE17
A2VSSQ AE19
VDD2DI AD19
VSS2DI AC19
R2SET AG13 R307 715
+3.3V_DELAY
C224 *0.1U_NC
+A2VDDQ
L42 BLM15BD121SN1D
C532 0.1U C531 1U
+1.8V_RUN
C516 *0.1U_NC
R2SET

VGA_BLU
VGA_GRN
VGA_RED
R120 150/F R127 150/F R130 150/F

DIS only
Layout Note:
Place 150 ohm termination resistors close to ATI CHIP.

QUANTA COMPUTER

Title	M92-S2_IO	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 19 of 58	


layout note: close to VDDR1#[1:17]
+1.8V_RUN
C227 10U
C228 *10U_NC
C239 1U
C231 1U
C253 0.1U
PLACE NEAR GPU
PLACE NEAR BALLS
U17D
PART 4 OF 10
POWER
M92-S2/M92-LP
VDDR1#1
VDDR1#2
VDDR1#3
VDDR1#4
VDDR1#5
VDDR1#6
VDDR1#7
VDDR1#8
VDDR1#9
VDDR1#10
VDDR1#11
VDDR1#12
VDDR1#13
VDDR1#14
VDDR1#15
VDDR1#16
VDDR1#17
PCIE_VDDR#1
PCIE_VDDR#2
PCIE_VDDR#3
PCIE_VDDR#4
PCIE_VDDR#5
PCIE_VDDR#6
PCIE_VDDR#7
PCIE_VDDR#8
PCIE_VDDC#1
PCIE_VDDC#2
PCIE_VDDC#3
PCIE_VDDC#4
PCIE_VDDC#5
PCIE_VDDC#6
PCIE_VDDC#7
PCIE_VDDC#8
PCIE_VDDC#9
PCIE_VDDC#10
PCIE_VDDC#11
PCIE_VDDC#12
VDDC#1
VDDC#2
VDDC#3
VDDC#4
VDDC#5
VDDC#6
VDDC#7
VDDC#8
VDDC#9
VDDC#10
VDDC#11
VDDC#12
VDDC#13
VDDC#14
VDDC#15
VDDC#16
VDDC#17
VDDC#18
VDDC#19
VDDC#20
VDDC#21
VDDC#22
VDDC#23
VDDC#24
VDDC#25
VDDC#1
VDDC#2
VDDC#3
VDDC#4
VDDC#5
VDDC#6
VDDC#7
VDDC#8
C232 0.1U
C300 1U
C237 1U
C225 0.01U
C291 10U
C323 0.1U
C319 1U
C320 1U
C299 4.7U
C316 10U
(1.1V)
+PCIE_VDDC
L22
BLM18PG121SN1D
+1.1V_GFX_PCIE
C332 10U
C334 1U
C335 0.1U
C341 *10U_NC
C336 *1U_NC
C333 *0.1U_NC
(PCIE_VDDC 1.1V @ 1A)
L20
BLM15BD121SN1D
+VDD_CT
C306 *10U_NC
C305 0.1U
C304 1U
C303 1U
C302 0.1U
VDD_CT#1
VDD_CT#2
VDD_CT#3
VDD_CT#4
+3.3V_DELAY
C200 1U
C515 1U
C195 0.1U
C204 0.1U
VDDR3#1
VDDR3#2
VDDR3#3
VDDR3#4
C522 1U
C523 0.1U
C520 1U
C521 *0.1U_NC
VDDR4#1
VDDR4#2
VDDR4#3
VDDR4#4
VDDR5#1
VDDR5#2
VDDR5#3
VDDR5#4
L41
BLM15BD121SN1D
+VDDRH1
C525 1U
C524 1U
VDDRHA
VSSRHA
L17
L16
(0.9~1.1V)
+VCC_GFX_CORE
C196 0.1U
C197 1U
+BBP
+VDDCI
U17E
PART 5 OF 10
GND
M92-S2/M92-LP
PCIE_VSS#1
PCIE_VSS#2
PCIE_VSS#3
PCIE_VSS#4
PCIE_VSS#5
PCIE_VSS#6
PCIE_VSS#7
PCIE_VSS#8
PCIE_VSS#9
PCIE_VSS#10
PCIE_VSS#11
PCIE_VSS#12
PCIE_VSS#13
PCIE_VSS#14
PCIE_VSS#15
PCIE_VSS#16
PCIE_VSS#17
PCIE_VSS#18
PCIE_VSS#19
PCIE_VSS#20
PCIE_VSS#21
PCIE_VSS#22
PCIE_VSS#23
PCIE_VSS#24
PCIE_VSS#25
PCIE_VSS#26
PCIE_VSS#27
PCIE_VSS#28
PCIE_VSS#29
PCIE_VSS#30
PCIE_VSS#31
GND#1
GND#2
GND#3
GND#4
GND#5
GND#6
GND#7
GND#8
GND#9
GND#10
GND#11
GND#12
GND#13
GND#14
GND#15
GND#16
GND#17
GND#18
GND#19
GND#20
GND#21
GND#22
GND#23
GND#24
GND#25
GND#26
GND#27
GND#28
GND#29
GND#30
GND#31
GND#32
GND#33
GND#34
GND#35
GND#36
GND#37
GND#38
GND#39
GND#40
GND#41
GND#42
GND#43
GND#44
GND#45
GND#46
GND#47
GND#48
GND#49
GND#50
GND#51
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GND#56
GND#57
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GND#60
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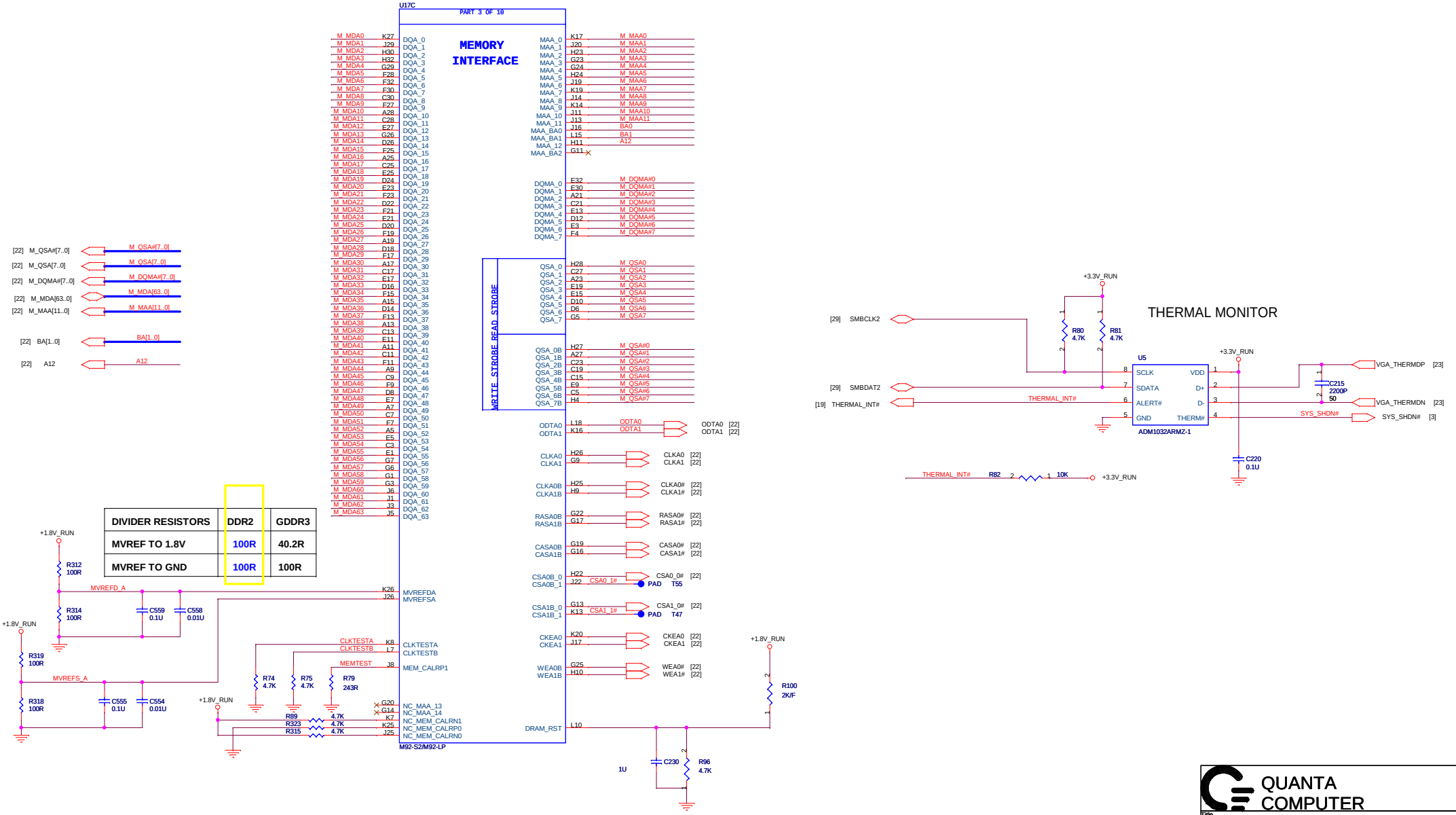
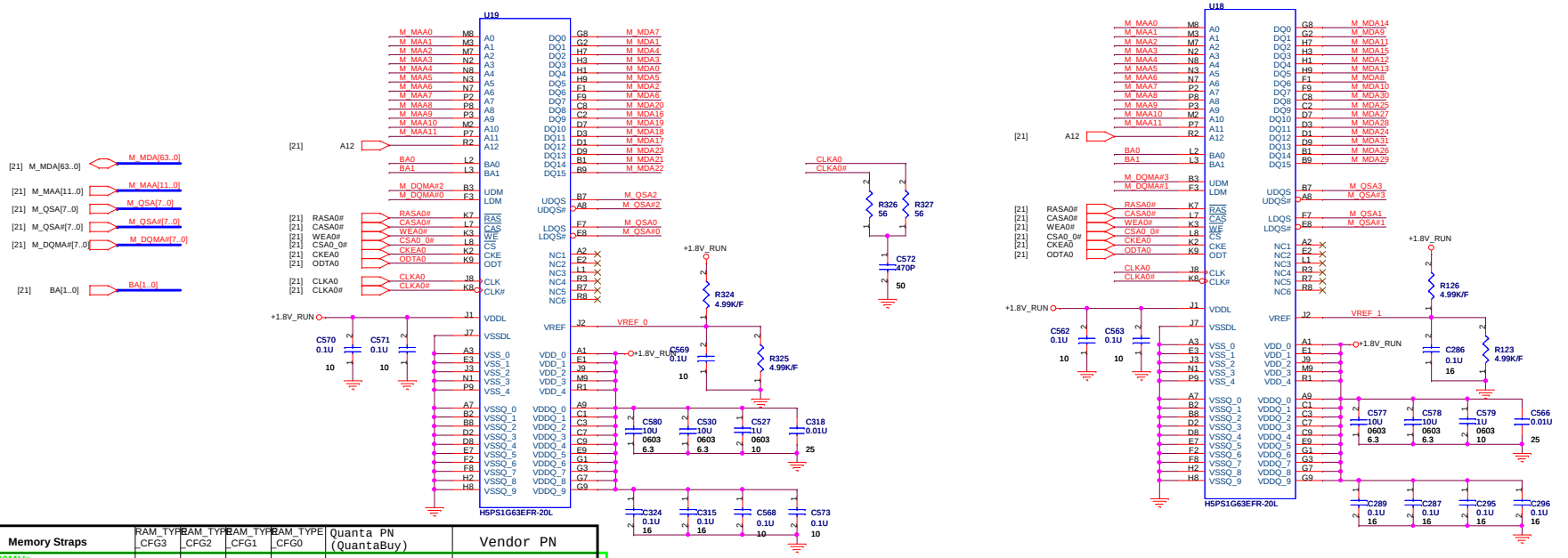
GND#79
GND#80
GND#81
GND#82
GND#83
GND#84
GND#85
GND#86
GND#87
GND#88
GND#89
VSS_MECH#1
VSS_MECH#2
VSS_MECH#3
+BBP
Q5
SI2303BDS-T1-E3
Q7
2N7002W-7-F
C198 1U
0402
6.3
R71 100K
+5V_RUN
[19] BB_ENA
Q6
2N7002W-7-F
R92 10K
layout note: close to VDDC#[1:25]
C256 1U
C240 1U
C245 1U
C260 1U
C251 1U
C257 1U
C265 1U
C241 1U
C246 1U
C259 1U
C279 1U
C268 1U
C258 1U
C284 10U
C269 10U
C273 10U
L18
BLM18EG221SN1D
C270 0.1U
C267 0.1U
C250 1U
C266 1U
C280 10U
QUANTA COMPUTER
Title
M92-S2_POWER/GND
Size
Document Number
VM8G
Rev
1A
Date: Tuesday, February 17, 2009
Sheet 20 of 58

MEMORY INTERFACE



Title	MEMORY/THERM		
Size	Document Number VM8G		Rev 1A
Date: Tuesday, February 17, 2009	Sheet 21 of 58		

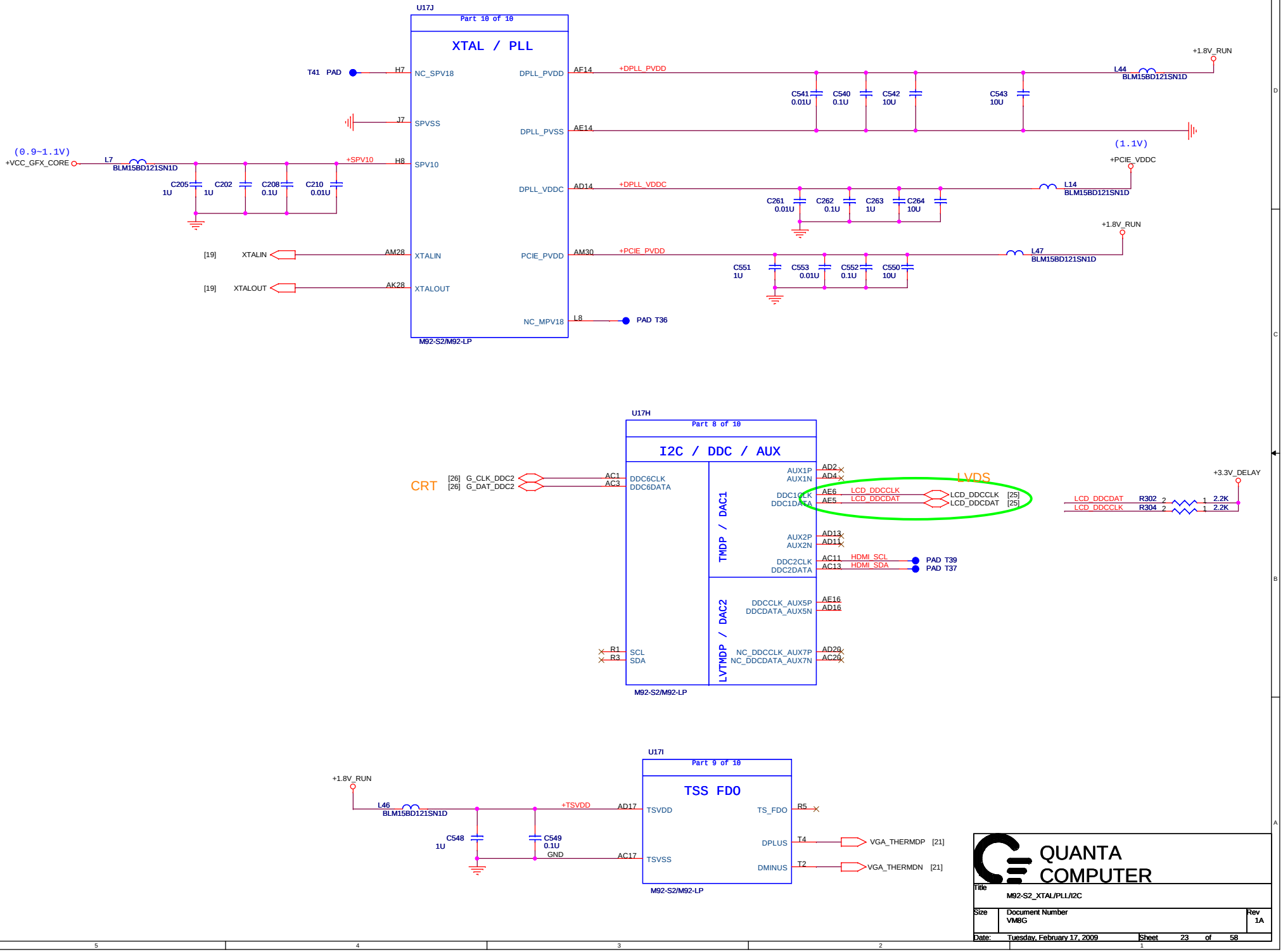
DDR2 64MbitX16 MEMORY



Memory Straps	RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Vendor PN
500MHz 512MB(64M*16) Hynix	0	0	1	0	AKD5LG-TW01(FR)	H5PS1G63EFR-20L
Remove Qimonda						
500MHz 512MB(64M*16) Samsung	0	0	0	1	AKD5LG-T507(IE)	K4N1G164QE-HC20
Remove						

QUANTA COMPUTER

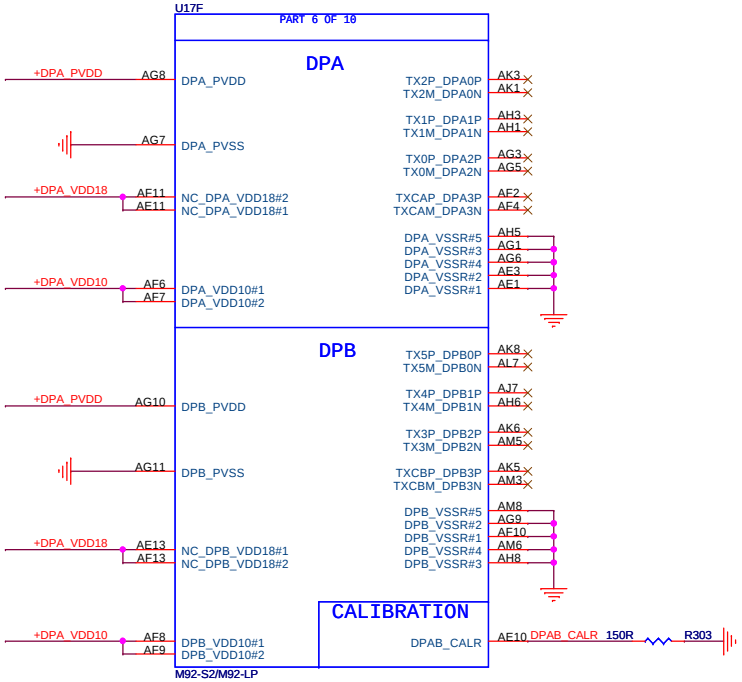
Title	M92-S2_DDR2_512M	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 22 of 58	



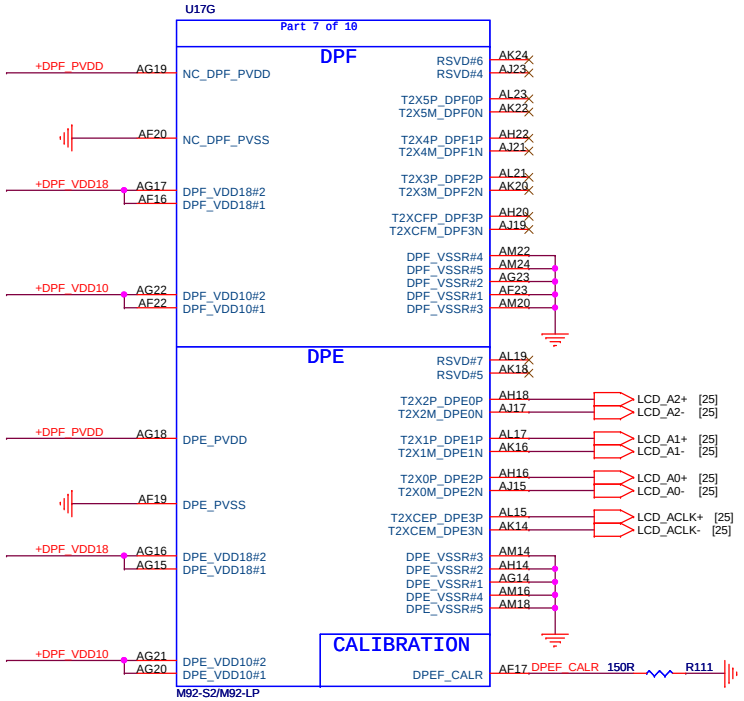
QUANTA COMPUTER

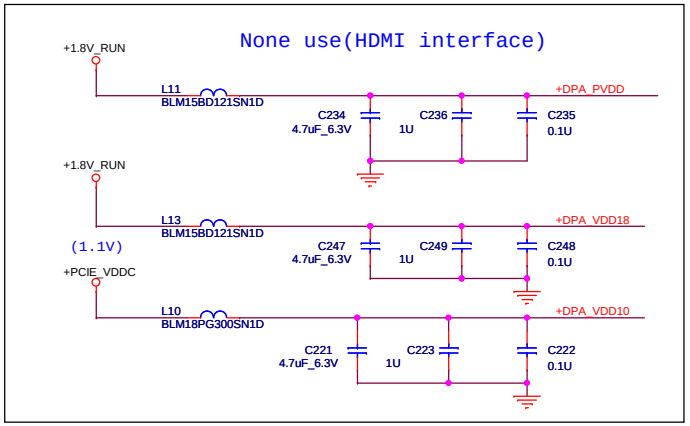
Title	M92-S2_XTAL/PLL/I2C	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 23 of 58	

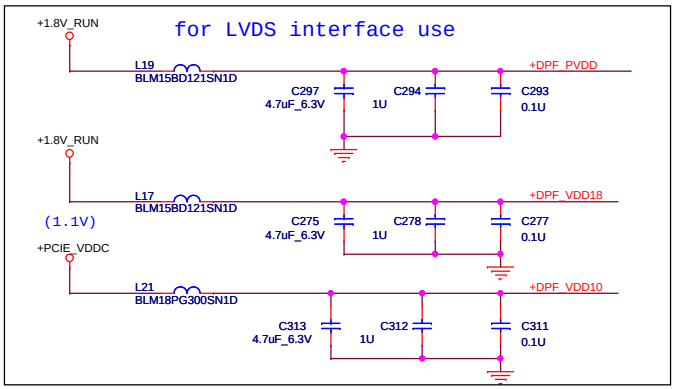
TMDP(HDMI) INTERFACE



LVDS INTERFACE

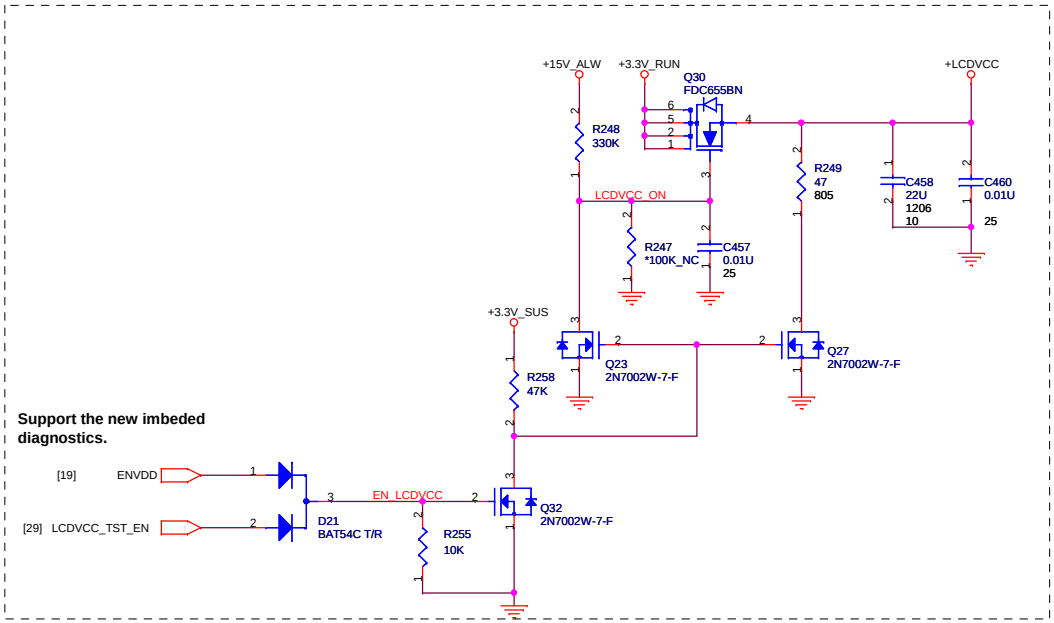


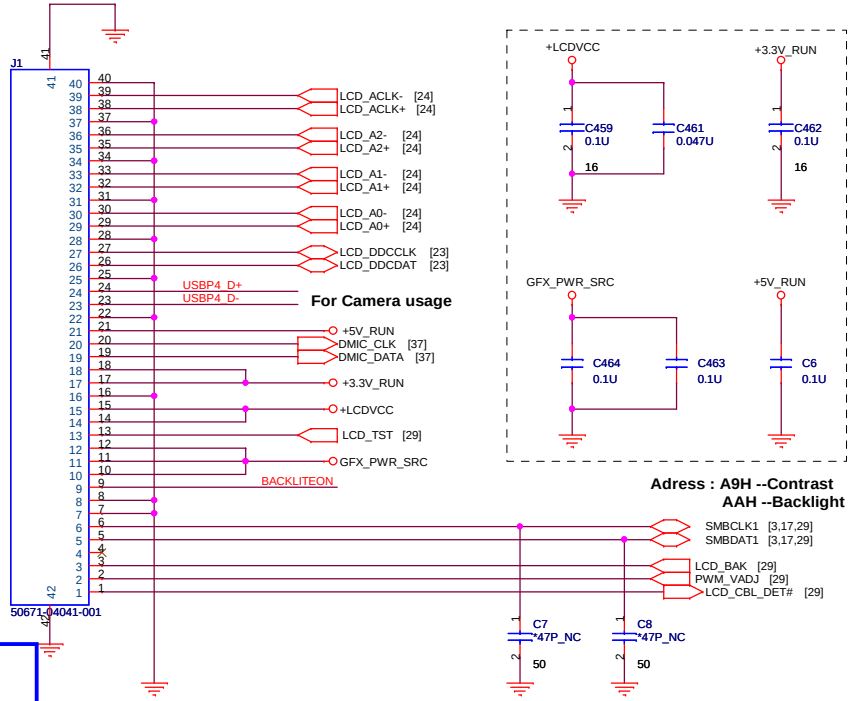




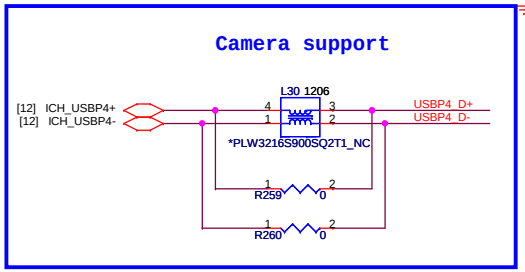
QUANTA COMPUTER

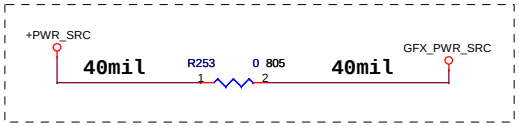
Title	M92-S2_TMDP I/F	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 24 of 58	

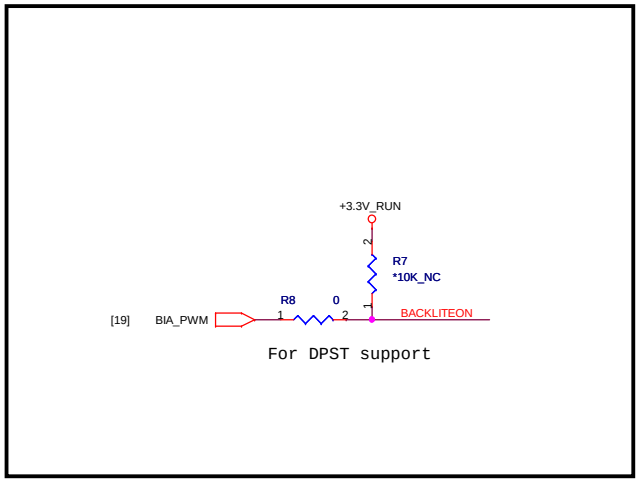




Adress : A9H --Contrast
AAH --Backlight

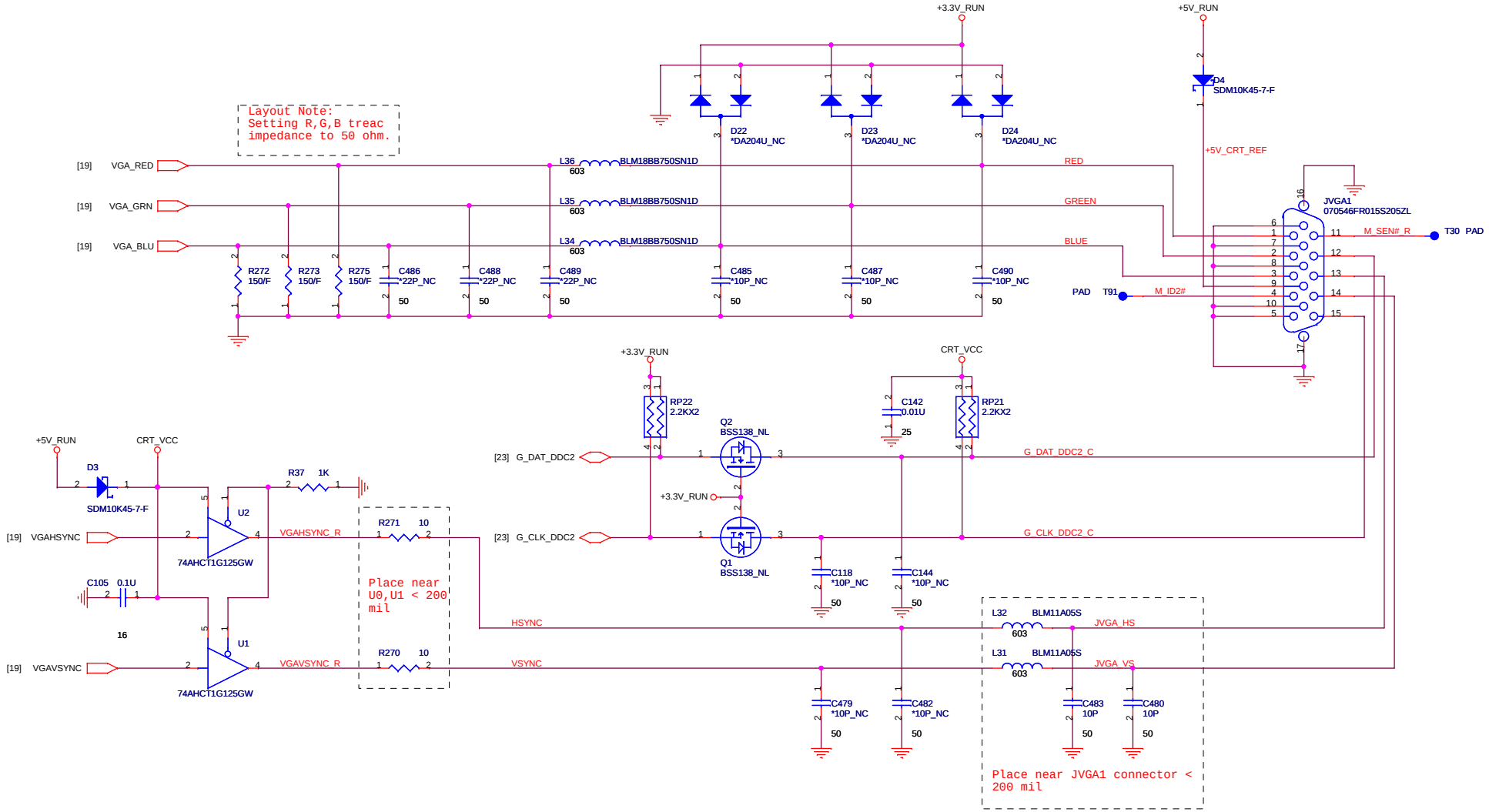






QUANTA COMPUTER

Title	LCD CONN & CK-SSCD	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 25 of 58	



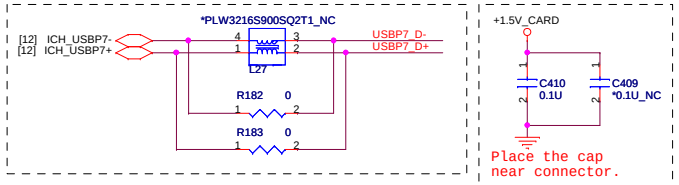
QUANTA COMPUTER

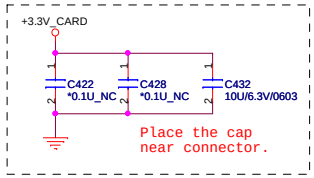
Title	CRT&TV CONN	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 26 of 58	

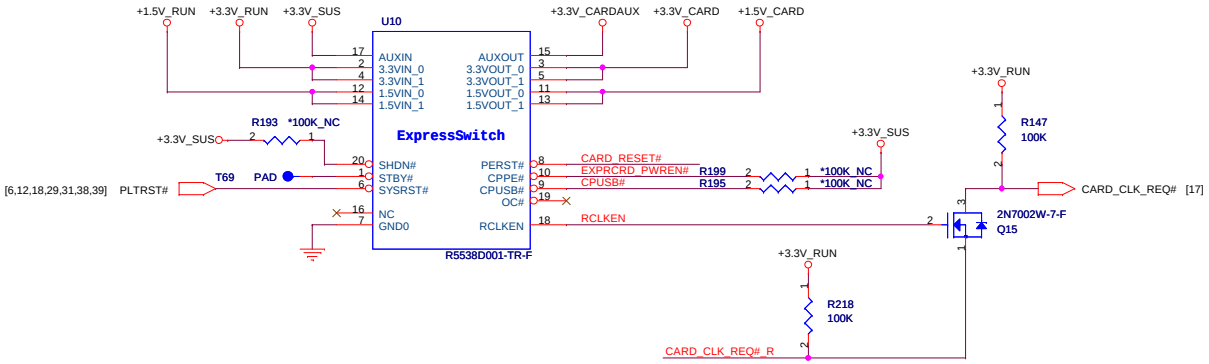
QUANTA COMPUTER

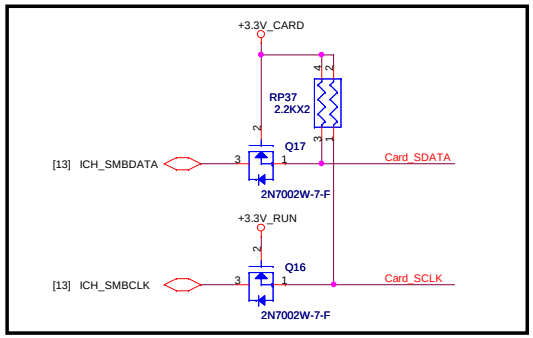
Title	Card Reader-RTS5158E	
Size	Document Number VM8G	Rev 1A
Date: Saturday, February 14, 2009	Sheet 27 of 58	

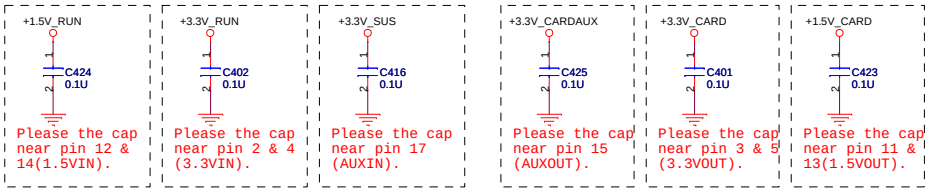
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



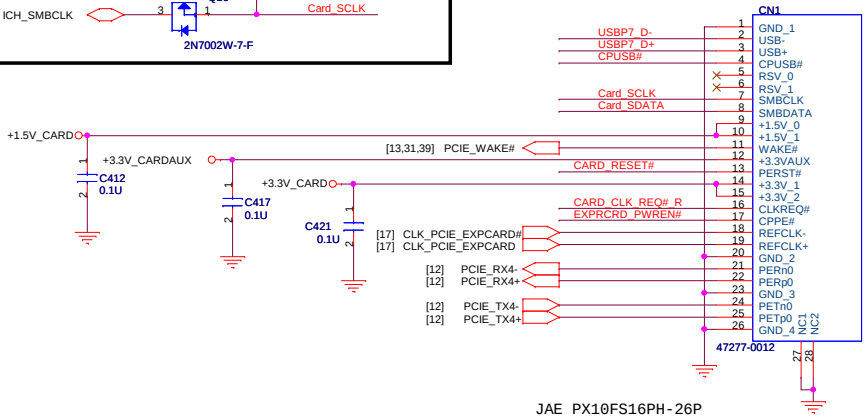








Express Card

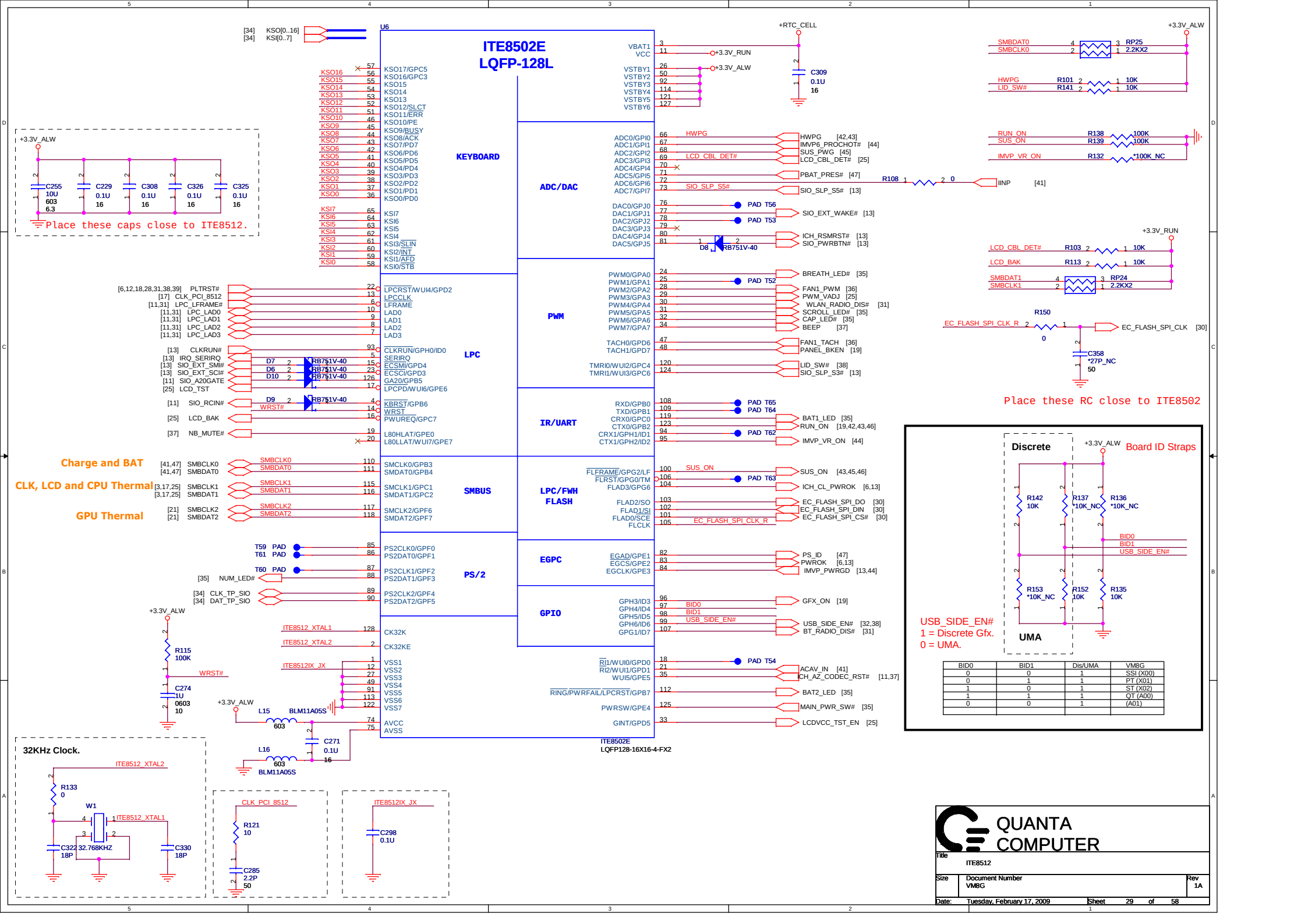


JAE PX10FS16PH-26P

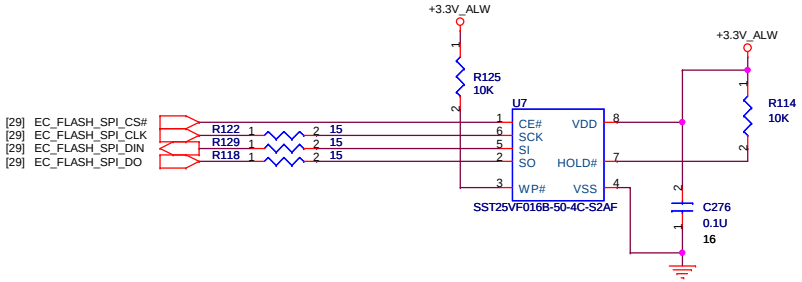
*Express Card cage

QUANTA COMPUTER

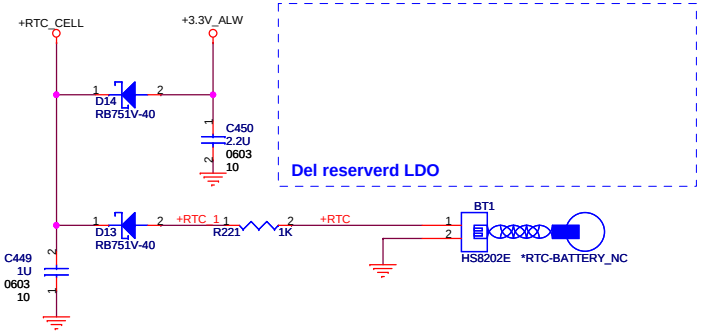
Title	Express Card	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 28 of 58	


ITE8502E
LQFP-128L
U6
KEYBOARD
ADC/DAC
PWM
LPC
IR/UART
SMBUS
LPC/FWH
FLASH
EGPC
PS/2
GPIO
Place these caps close to ITE8512.
Place these RC close to ITE8502
Charge and BAT
CLK, LCD and CPU Thermal
GPU Thermal
32KHz Clock.
Discrete
Board ID Straps
UMA
USB_SIDE_EN#
1 = Discrete Gfx.
0 = UMA.
QUANTA COMPUTER
ITE8512
VM8G
Tuesday, February 17, 2009

16Mbit (2M Byte), SPI

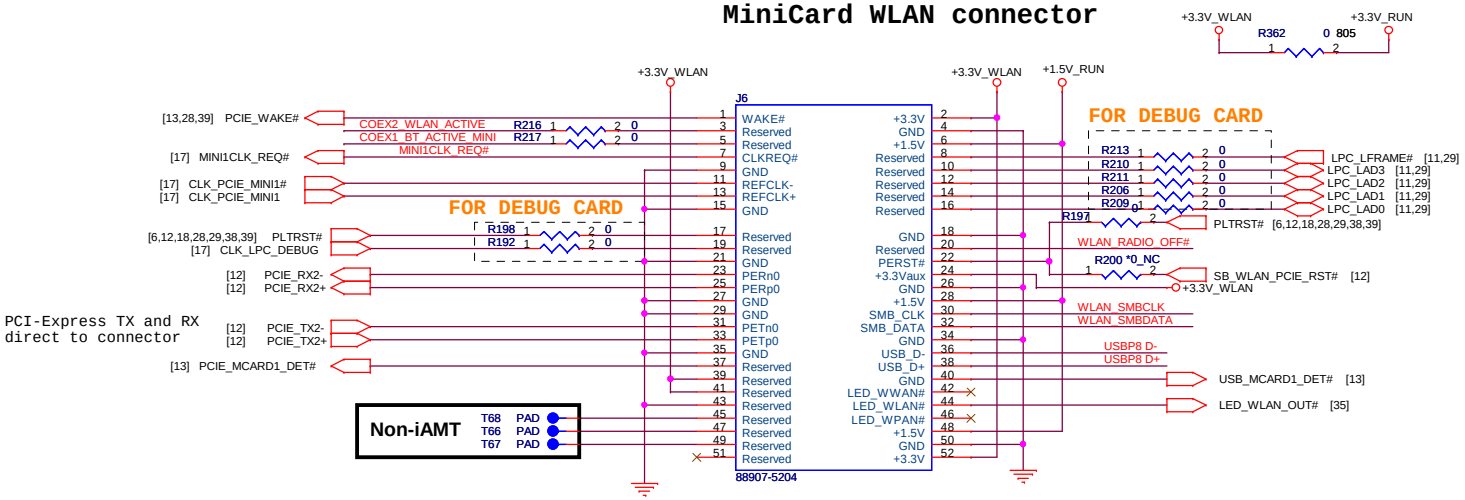


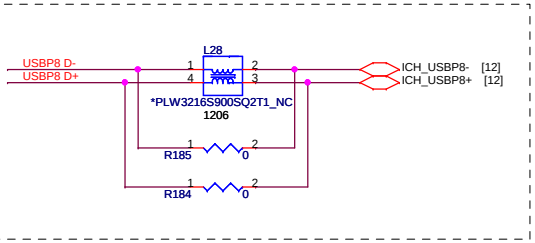
RTC BATTERY

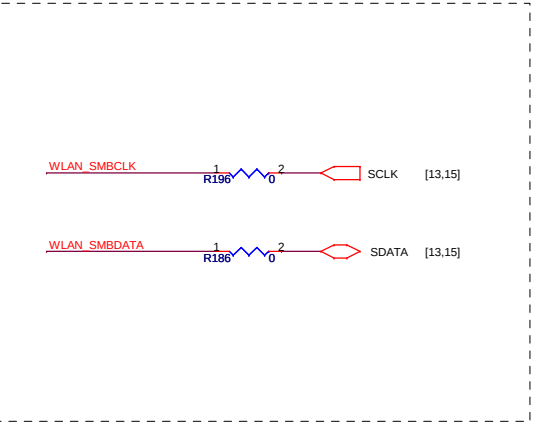


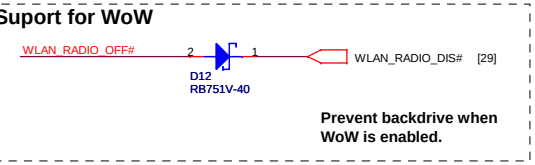
Title	FLASH/RTC	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 30 of 58	

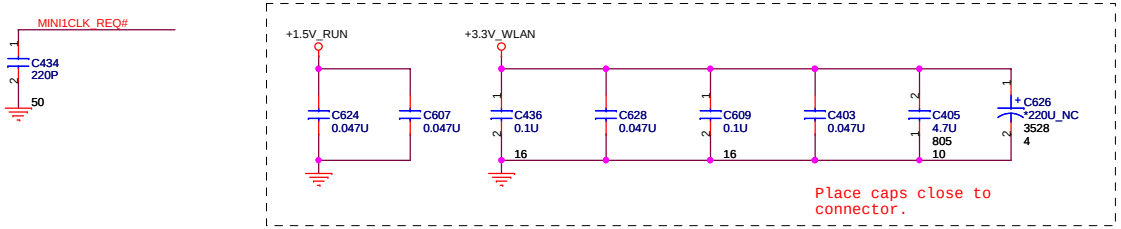
MiniCard WLAN connector



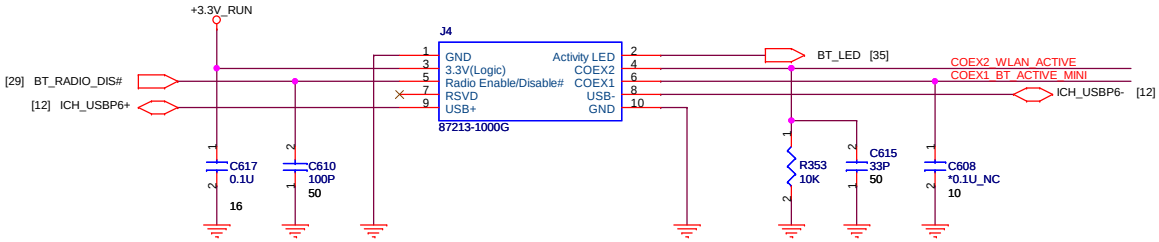






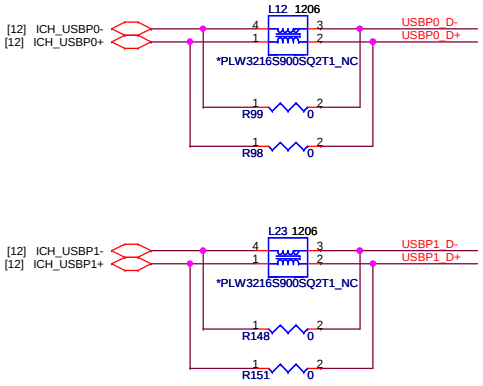


Bluetooth

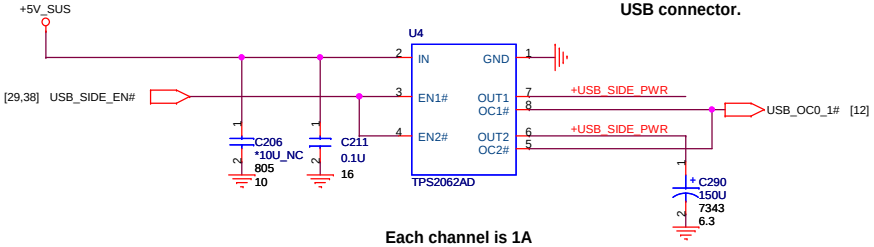


QUANTA COMPUTER		
Title: MINI Card (WLAN)/BT		
Size	Document Number: VM8G	Rev: 1A
Date: Tuesday, February 17, 2009	Sheet 31 of 58	

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

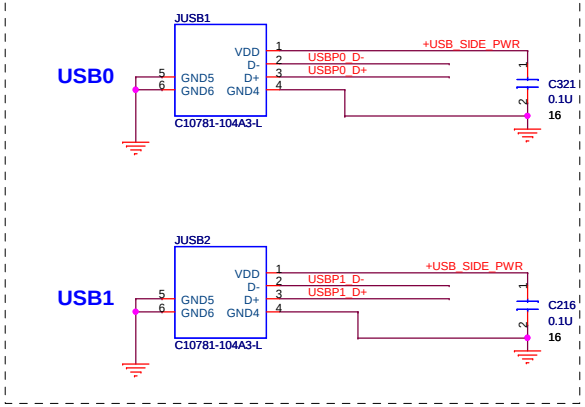


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

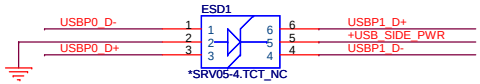


Place one 150uF cap by each USB connector.

Each channel is 1A



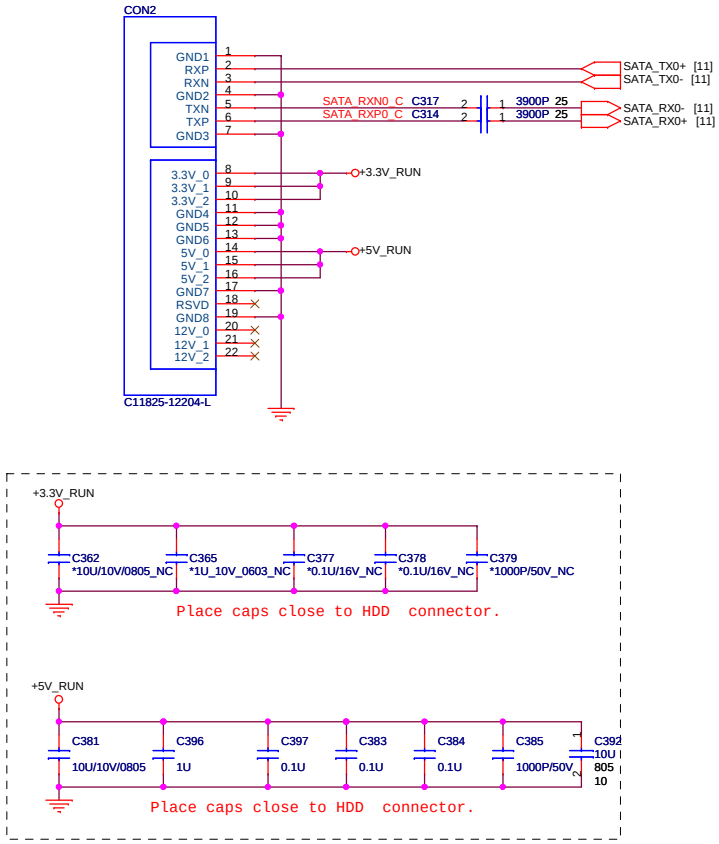
Place ESD diodes as close as USB connector.



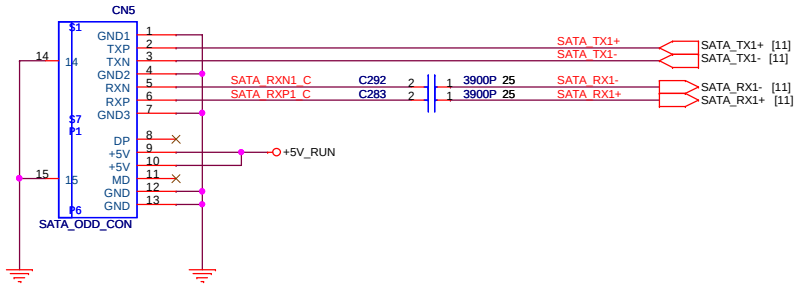
QUANTA COMPUTER

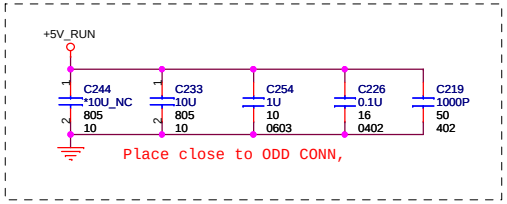
Title	USB	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 32 of 58	

SATA HDD Connector.



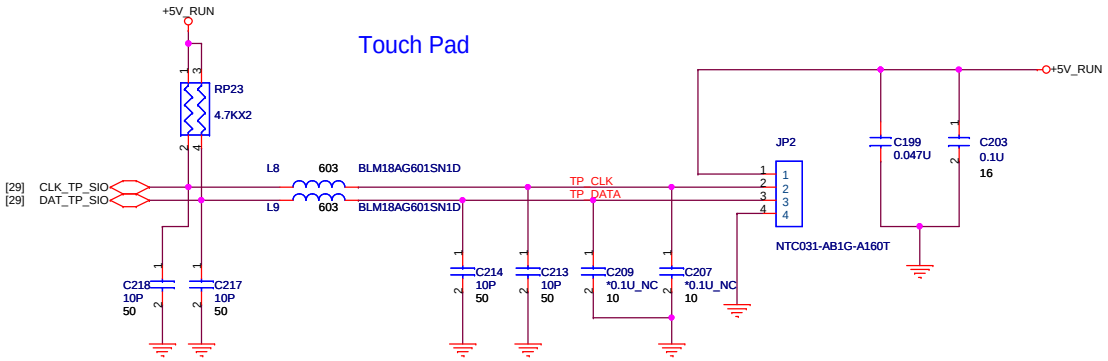
SATA ODD Connector.



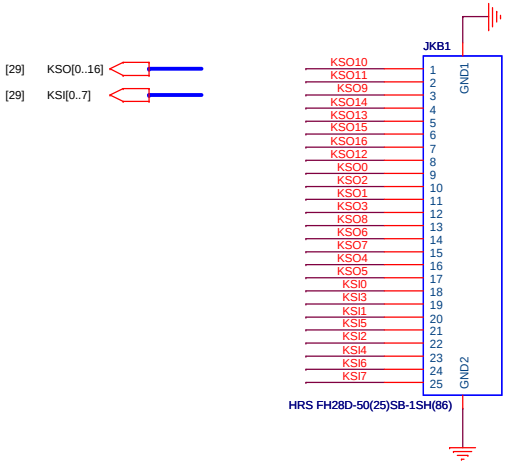


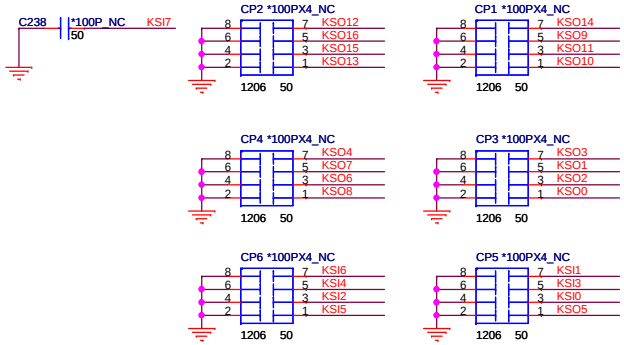
QUANTA COMPUTER		
Title: SATA (HDD&CD_ROM)		
Size	Document Number: VM8G	Rev: 1A
Date: Tuesday, February 17, 2009	Sheet 33 of 58	

Touch Pad



KEYBOARD CONNECTOR





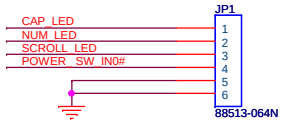
100P CAPS CLOSE TO JKB1

QUANTA COMPUTER

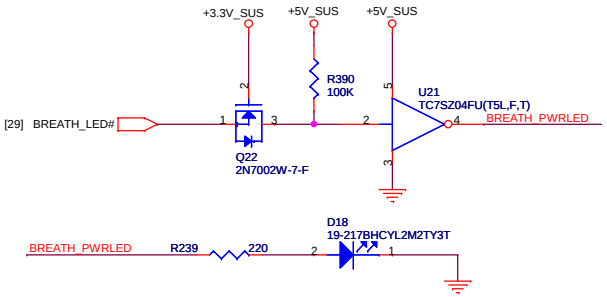
Title	TOUCH PAD, BULE TOOTH & FIR	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 34 of 58	

Keyboard LED

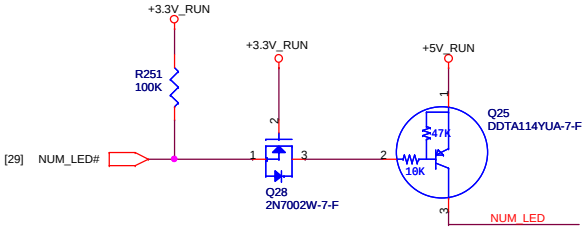
Dash board connector

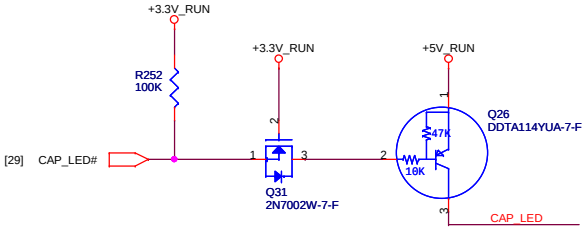


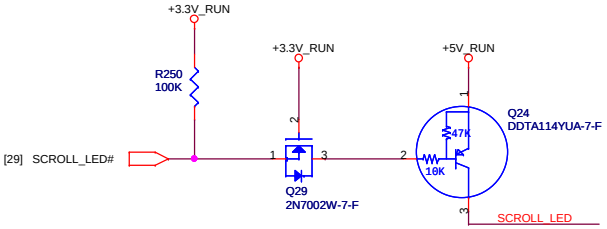
Power & Suspend.



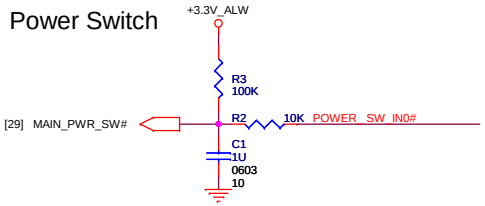
Keyboard LED



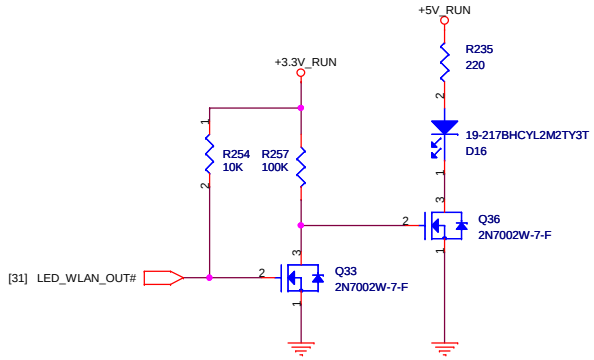




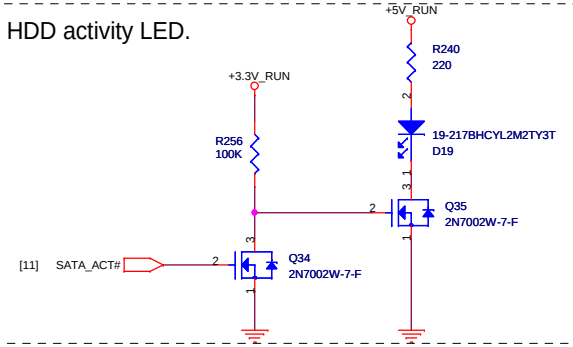
Power Switch



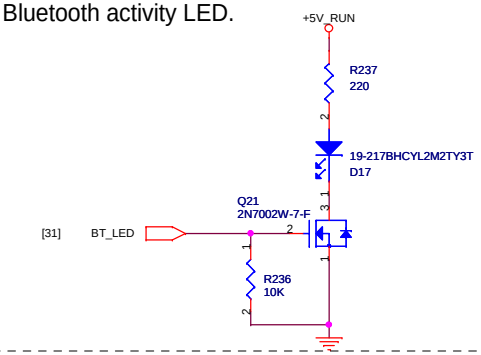
WLAN



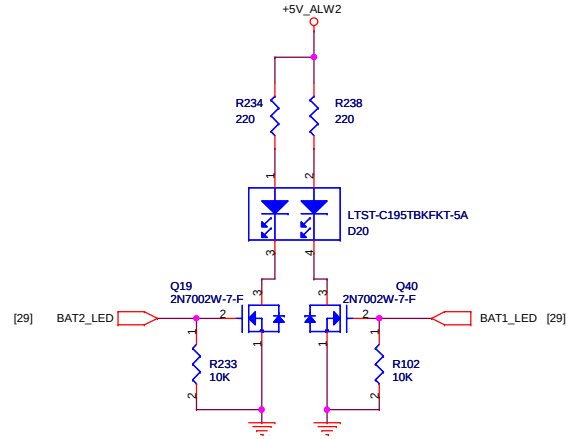
HDD activity LED.



Bluetooth activity LED.

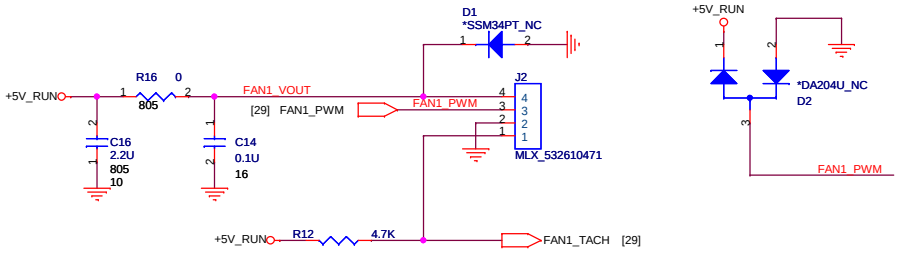


Battery status.



QUANTA COMPUTER

Title	SWITCH, KEYBOARD & LED	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 35 of 58	



QUANTA COMPUTER

Title	FAN & THERMAL	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 36 of 58	

AUDIO CODEC

Put the RC close to U23 pin 6, reserve for EMI

Add PC beep for system error circuit No9 10.14
Del PC beep No9 10.15

Speakers conn

Add resisters for fine tune use

Jack Sense

PC BEEP

Close to U1

Change Beep design

Change size and PN

R1412,R1413 Close to J0

Close to U31

Audio Jacks

HP JACKN

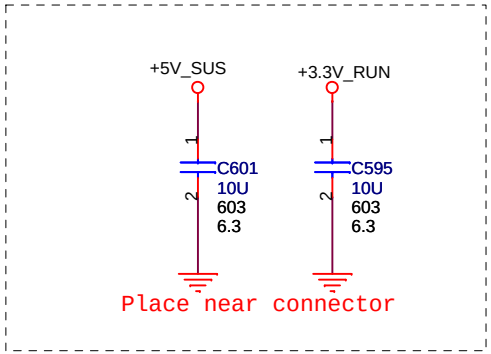
MIC JACK

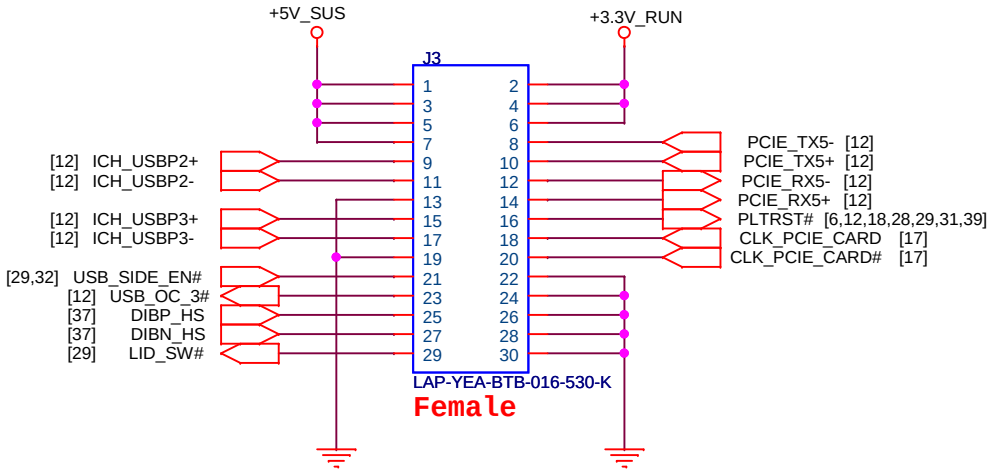
L24.L25,L30,L31,
FB_600ohm+-25%_100MHz
_200mA_0.6ohm DC

GAIN	R10 Pull-up
-46 dB	R10 Omit
-18 dB	R10 Populate

QUANTA COMPUTER

Title		
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 37 of 58	

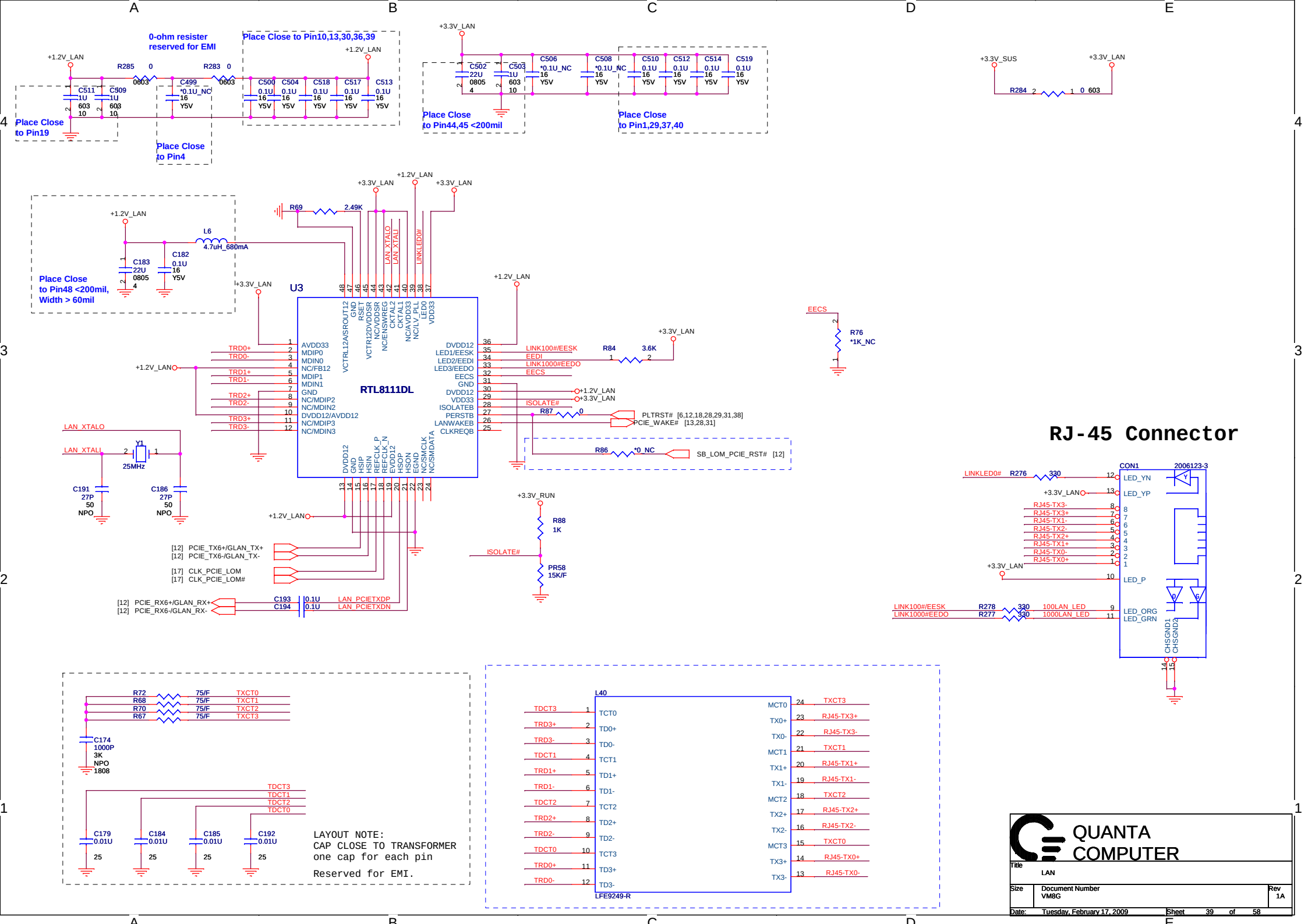




Board to board connector (Modem Card + Cardreader+1394a+ 2 USB Port)

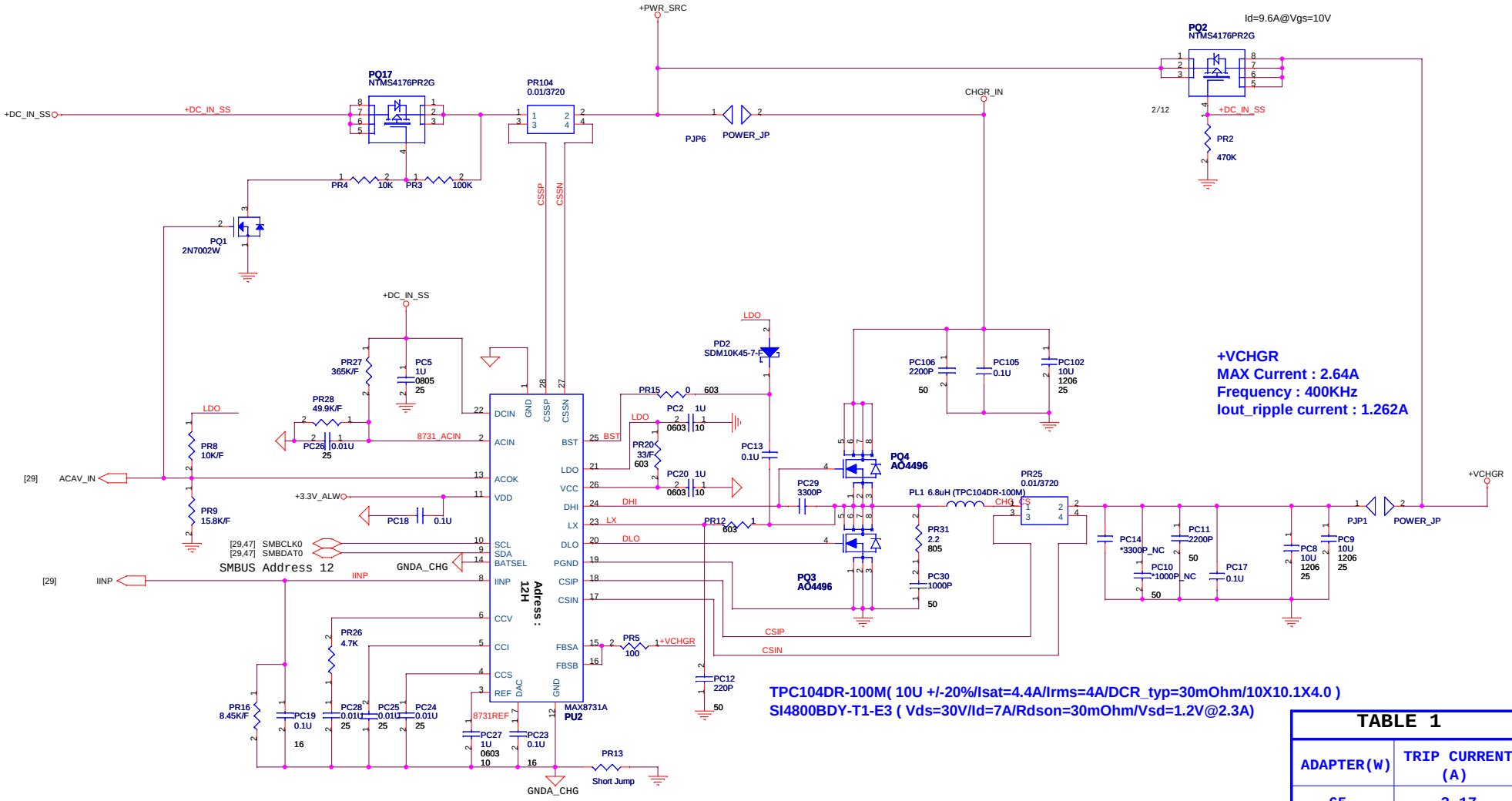
QUANTA COMPUTER

Title		
Size	Document Number VM8G	Rev 2A
Date: Tuesday, February 17, 2009	Sheet 38 of 58	


0-ohm resister
reserved for EMI
Place Close to Pin10,13,30,36,39
Place Close
to Pin19
Place Close
to Pin4
Place Close
to Pin44,45 <200mil
Place Close
to Pin1,29,37,40
Place Close
to Pin48 <200mil,
Width > 60mil
RTL8111DL
U3
L6
4.7uH_680mA
25MHz
LAYOUT NOTE:
CAP CLOSE TO TRANSFORMER
one cap for each pin
Reserved for EMI.
LFE9249-R
RJ-45 Connector
QUANTA
COMPUTER
LAN
VM8G
Tuesday, February 17, 2009

QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number VM8G	Rev 1A
Date: Saturday, February 14, 2009	Sheet 40 of 58	



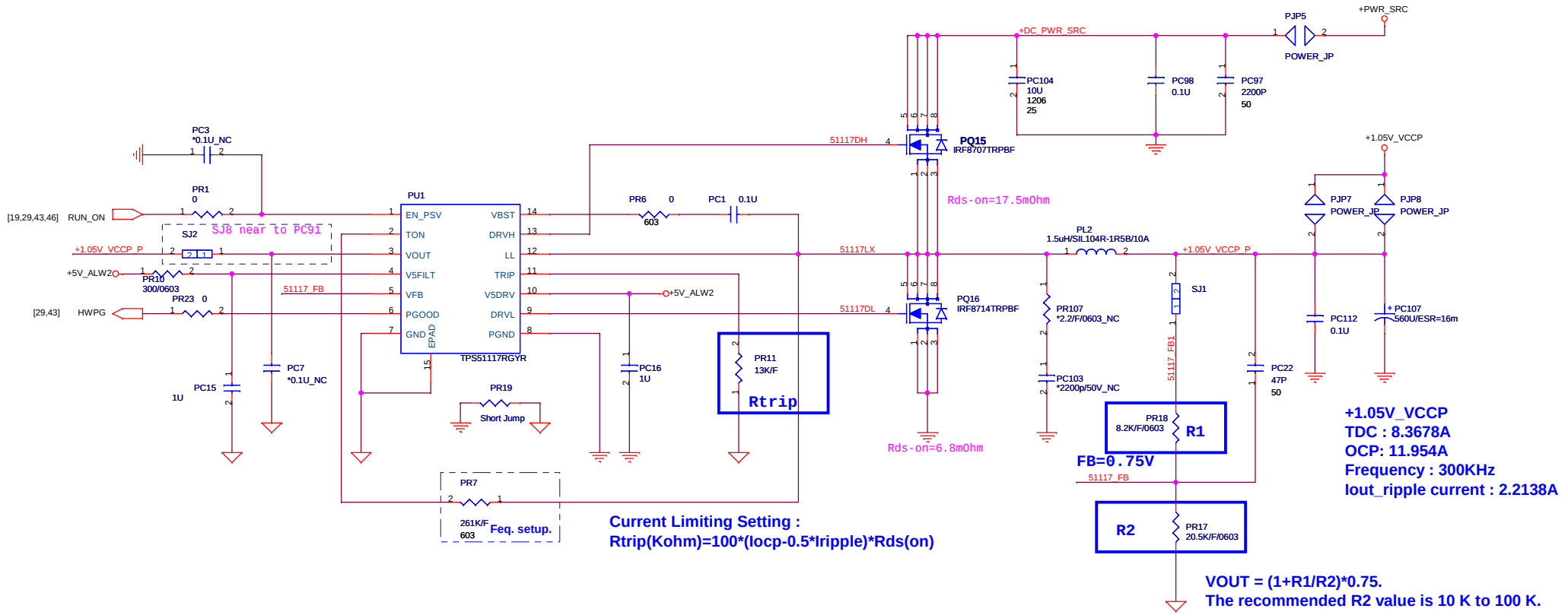
+VCHGR
MAX Current : 2.64A
Frequency : 400KHz
Iout_ripple current : 1.262A

TPC104DR-100M(10U +/-20%/Isat=4.4A/Irms=4A/DCR_typ=30mOhm/10X10.1X4.0)
SI4800BDY-T1-E3 (Vds=30V/Id=7A/Rdson=30mOhm/Vsd=1.2V@2.3A)

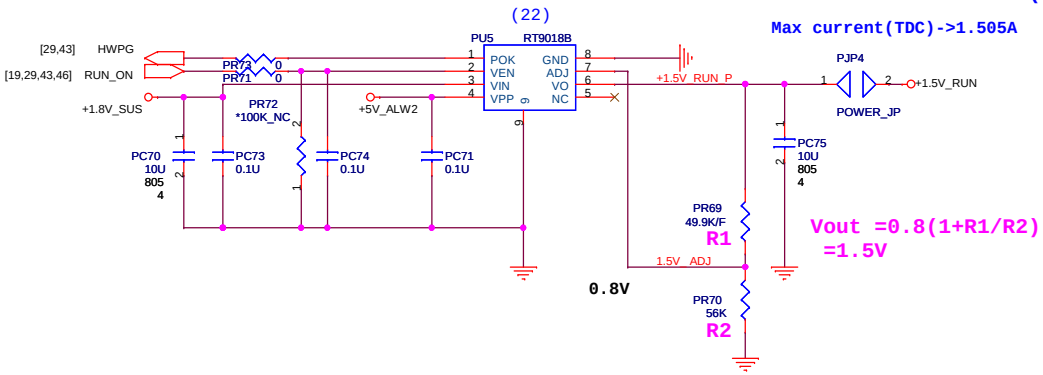
TABLE 1	
ADAPTER(W)	TRIP CURRENT (A)
65	3.17
90	4.43
130	6.43
150	7.43
200	9.75
230	11.28

QUANTA COMPUTER

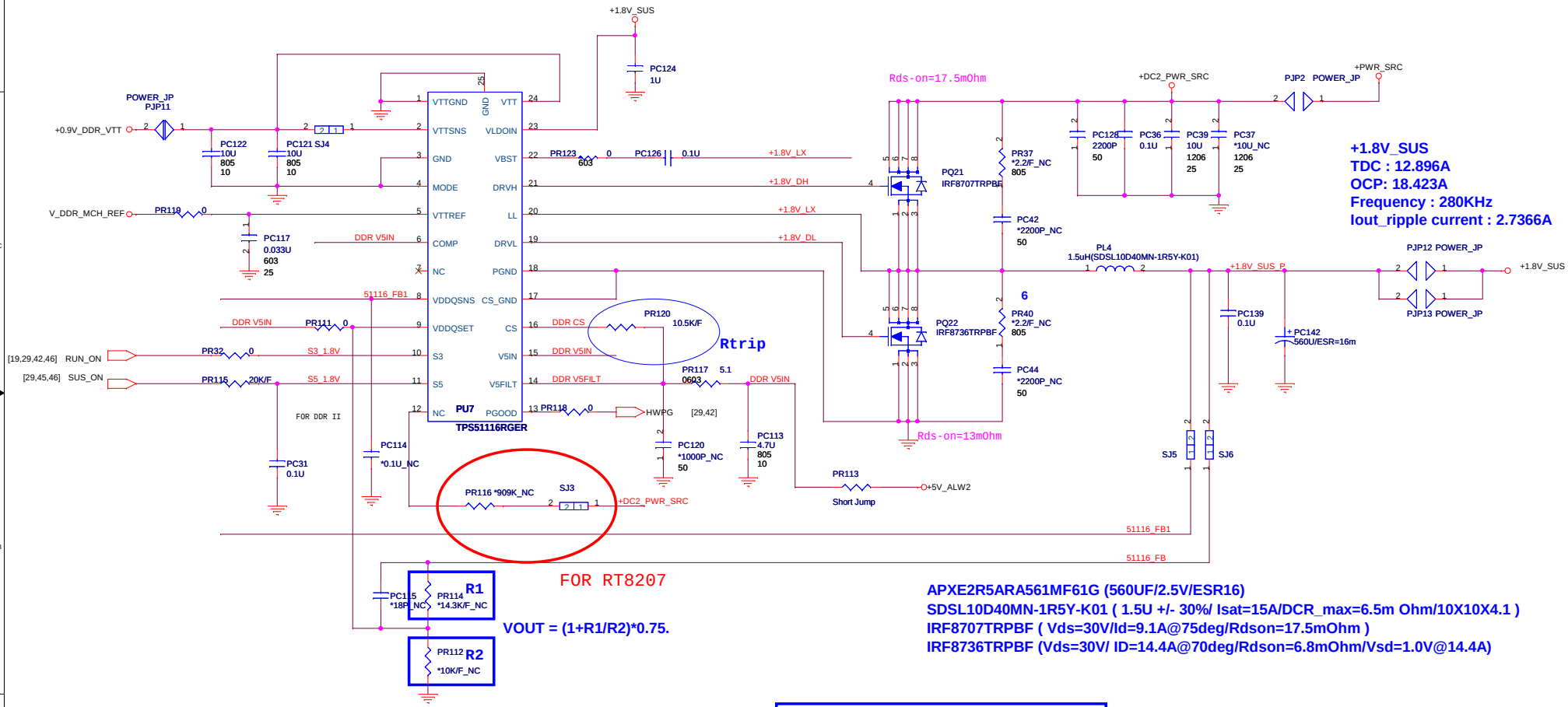
Title	Charger (MAX8731A)	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 41 of 58	



APXE2R5ARA561MF61G (560UF/2.5V/ESR16)
SIL104R-1R5B (1.5U +/- 30%/ Isat=10A/DCR_max=8.1m Ohm/10X10X3.8)
IRF8707TRPBF (Vds=30V/Id=9.1A@75deg/Rdson=17.5mOhm)
IRF8714TRPBF (Vds=30V/ ID=11A@70deg/Rdson=13mOhm/Vsd=1.0V@11A)



QUANTA COMPUTER		
Title: 1.05_VCCP & 1.5V_RUN		
Size	Document Number: VM8G	Rev: 1A
Date: Tuesday, February 17, 2009	Sheet 42 of 58	



QUANTA COMPUTER

Title	1.8VSUS & 0.9VTT (TPS51116)	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 43 of 58	

+PWR_SRC

C473 *100U_NC 25 | C466 *100U_NC 25 | C465 *100U_NC 25

Layout Note:
Need to add 100uF cap on PWR_SRC for cap singing.
Place on PWR_SRC near +VCC_CORE.

+VCC_CORE
TDC : 35A
MAX:47A
Frequency : 300KHz
Iout_ripple current : 9.64A of each phase.

MAX17410

MAT
ERTJ0EV474J
Close to Phase 1 Inductor

Parallel

Close to Phase 1 Inductor

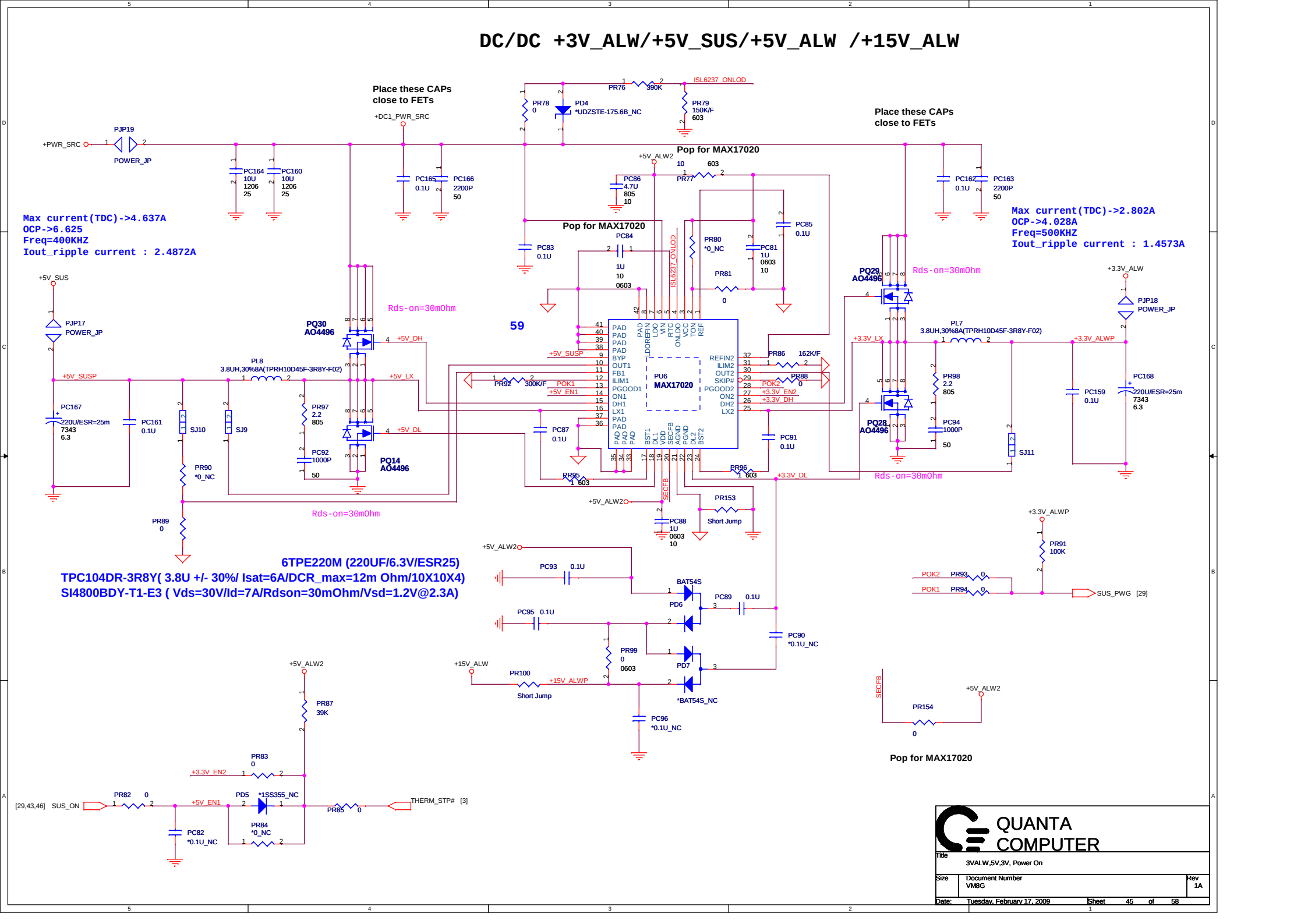
D6 D5 D4 D3 D2 D1 D0	Output
0 0 0 0 0 0 0	1.500V
0 0 0 0 0 0 1	1.4875
0 0 0 0 1 0 1	1.4375
0 0 0 0 1 1 1	1.4125
0 0 0 1 0 0 0	1.4000
0 0 1 0 0 0 1	1.2875
0 0 1 1 0 0 0	1.2000
0 0 1 1 1 0 0	1.1500
0 1 0 1 0 0 0	1.0000
0 1 0 1 0 1 1	0.9625
0 1 1 1 1 0 0	0.7500
1 0 0 0 1 0 0	0.6500
1 0 1 0 0 0 0	0.5000
1 1 0 0 0 0 0	0.3000

ETQP4LR36WFC (0.36U +/- 20%/ Isat=24A/DCR_max=1.1m Ohm/11.5X10X4)
NTMFS4921NT1G (Vds=30V/Id=10.2A@85deg/Rdson=10.5mOhm)
NTMFS4946NT1G (Vds=30V/ ID=14.6A@85deg/Rdson=5.1mOhm/Vsd=1.0V@30A)
EEFSX0D331YR (330UF/2V/ESR9)

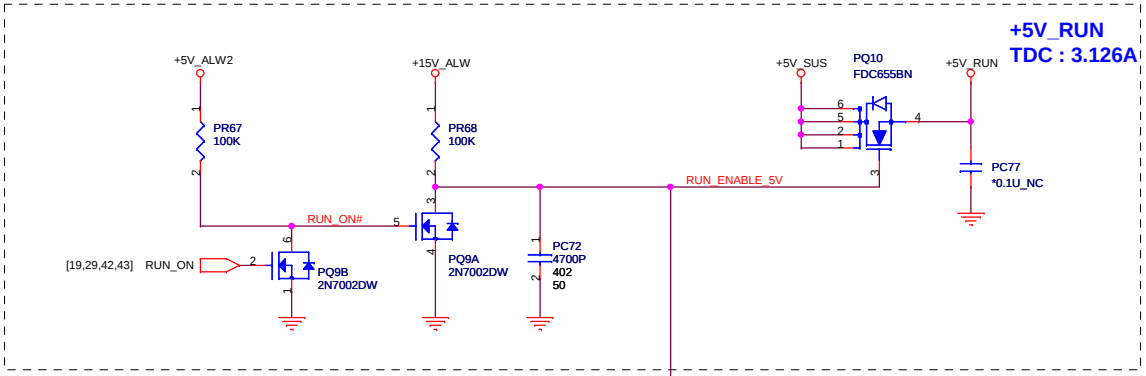
QUANTA COMPUTER

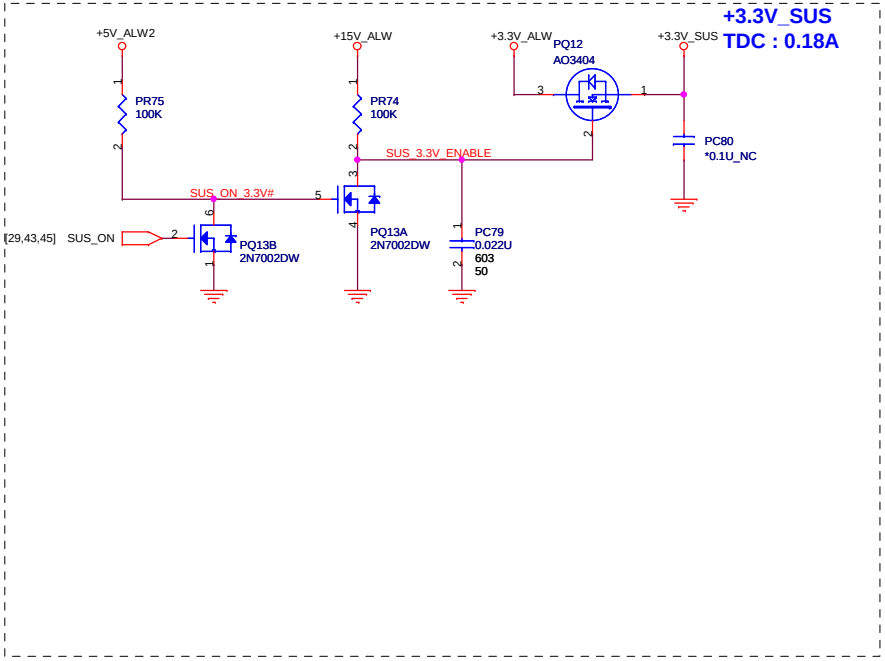
Title	CPU_Core_2Phase (MAX17410)	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 44 of 58	

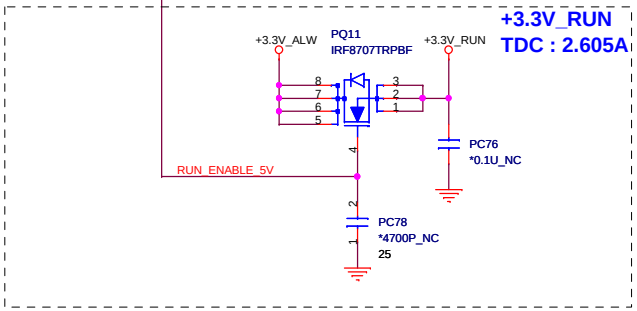
DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

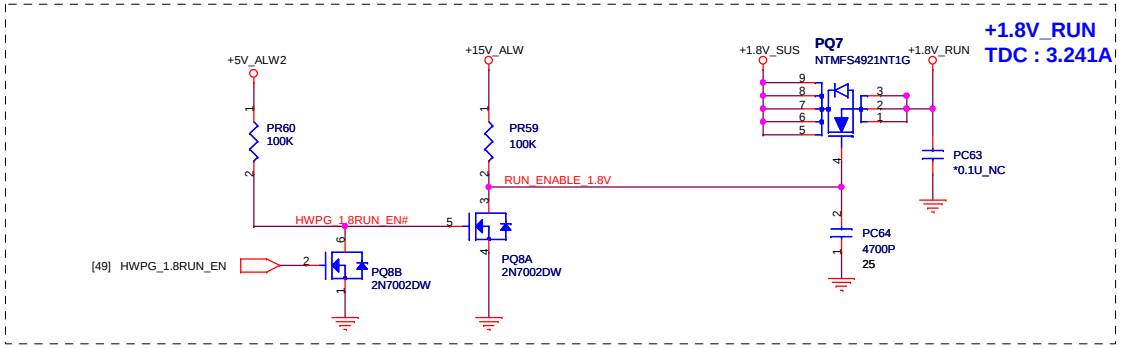


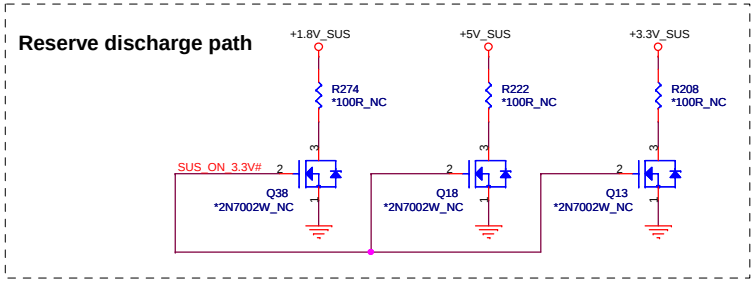
QUANTA COMPUTER		
Title	3VALW,5V,3V, Power On	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 45 of 58	

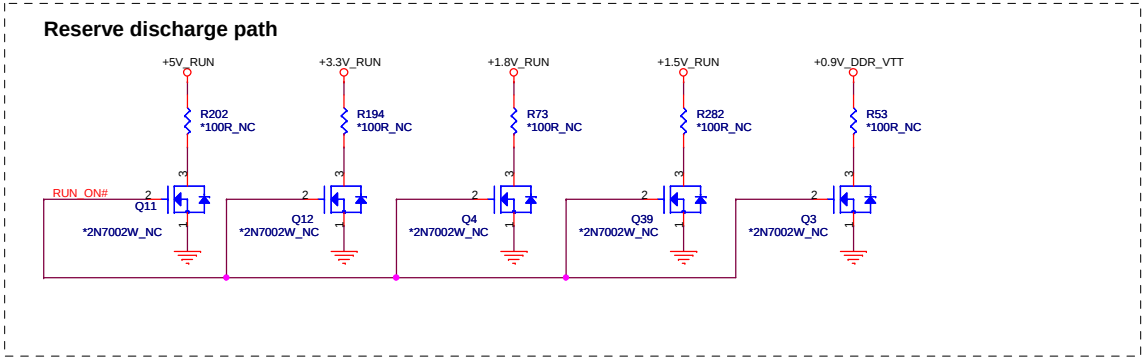






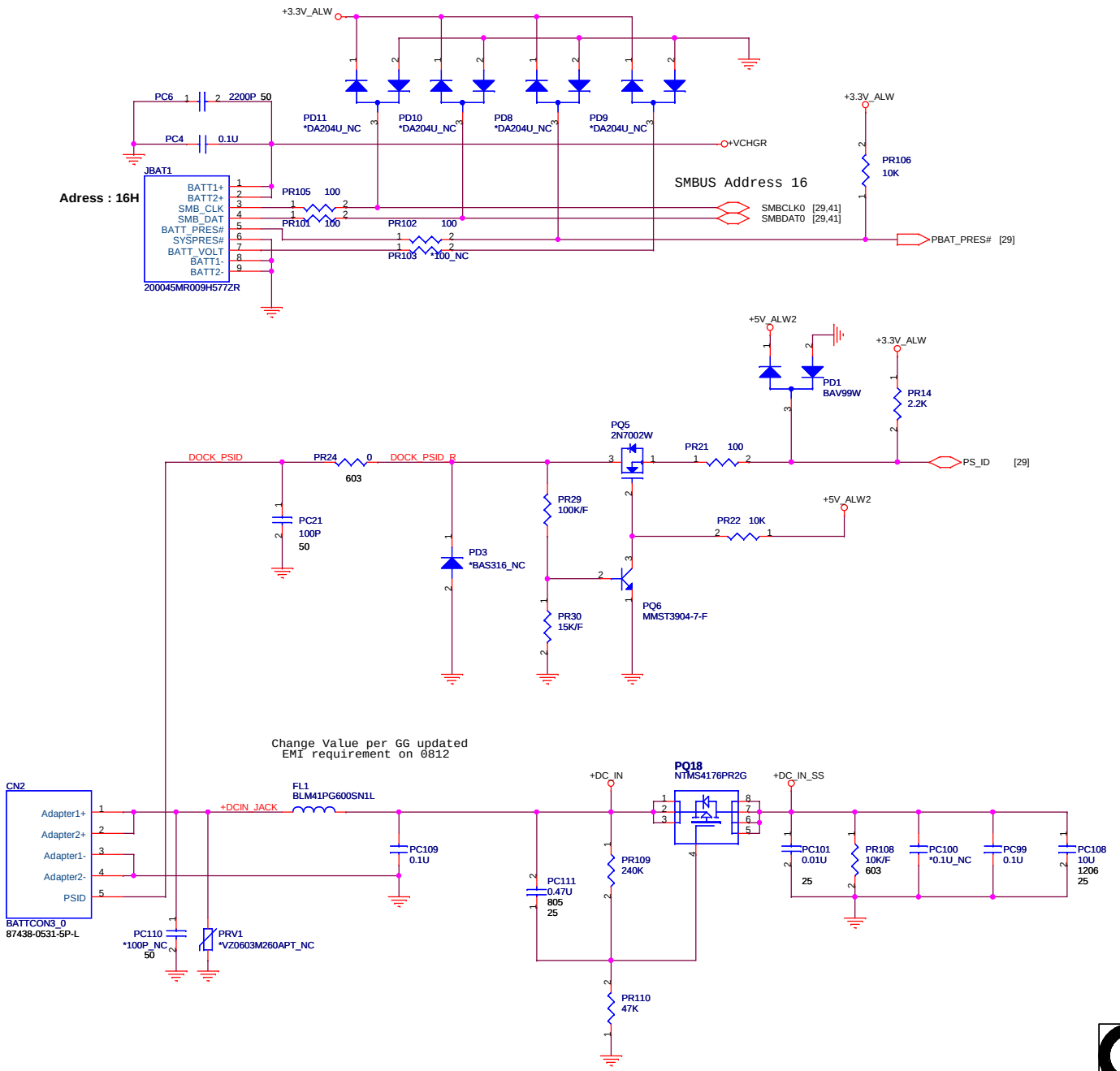






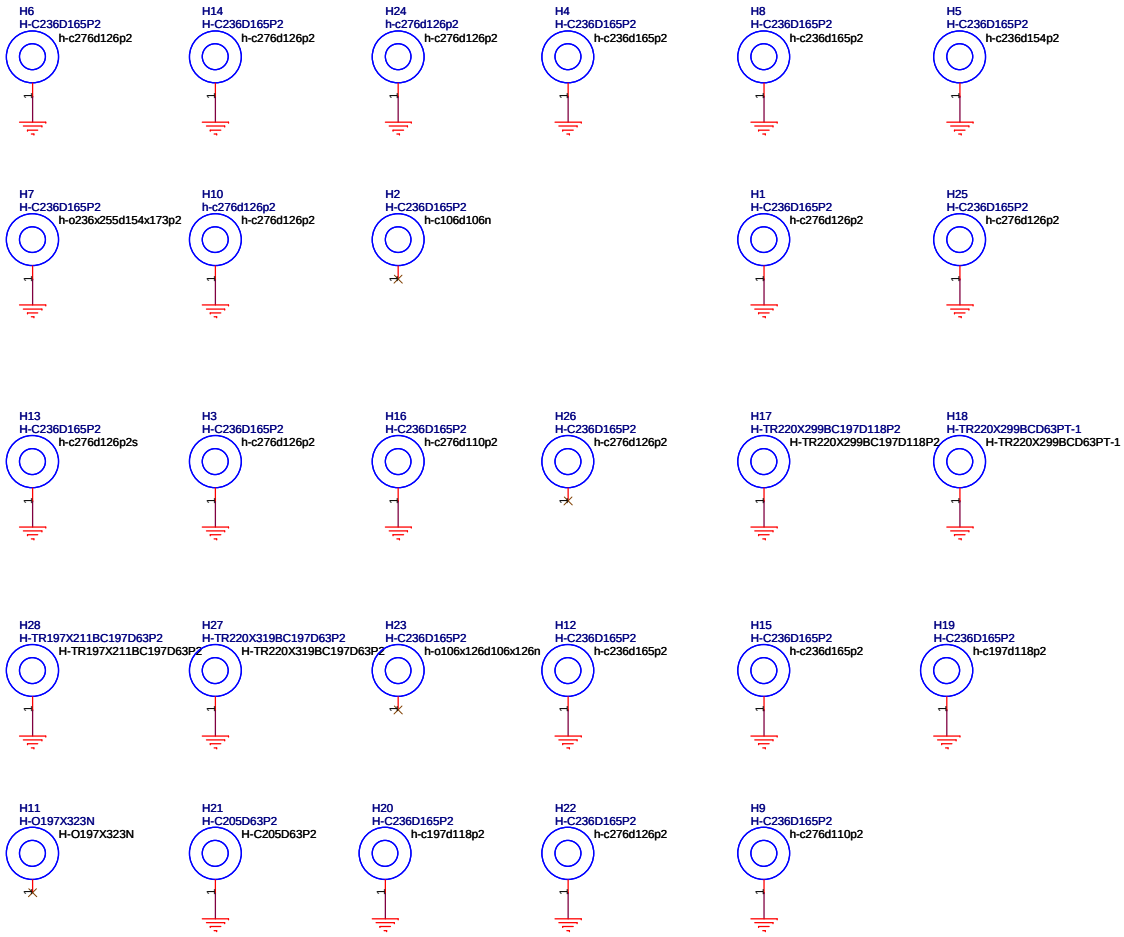
QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 46 of 58	



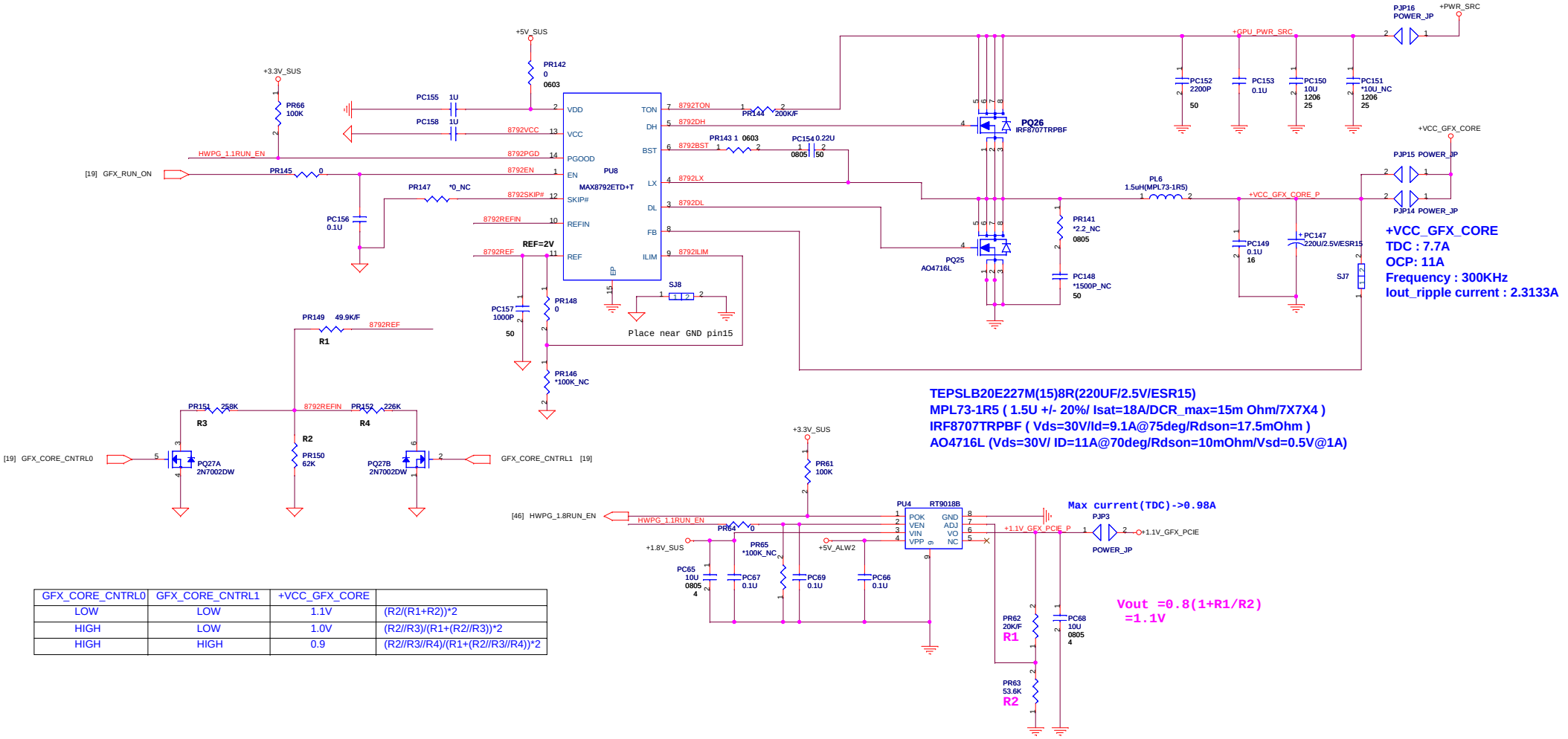
QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 47 of 58	



QUANTA COMPUTER

Title	SCREW PAD	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 48 of 58	



GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE	
LOW	LOW	1.1V	(R2//(R1+R2))*2
HIGH	LOW	1.0V	(R2//R3)/(R1+(R2//R3))*2
HIGH	HIGH	0.9	(R2//R3//R4)/(R1+(R2//R3//R4))*2

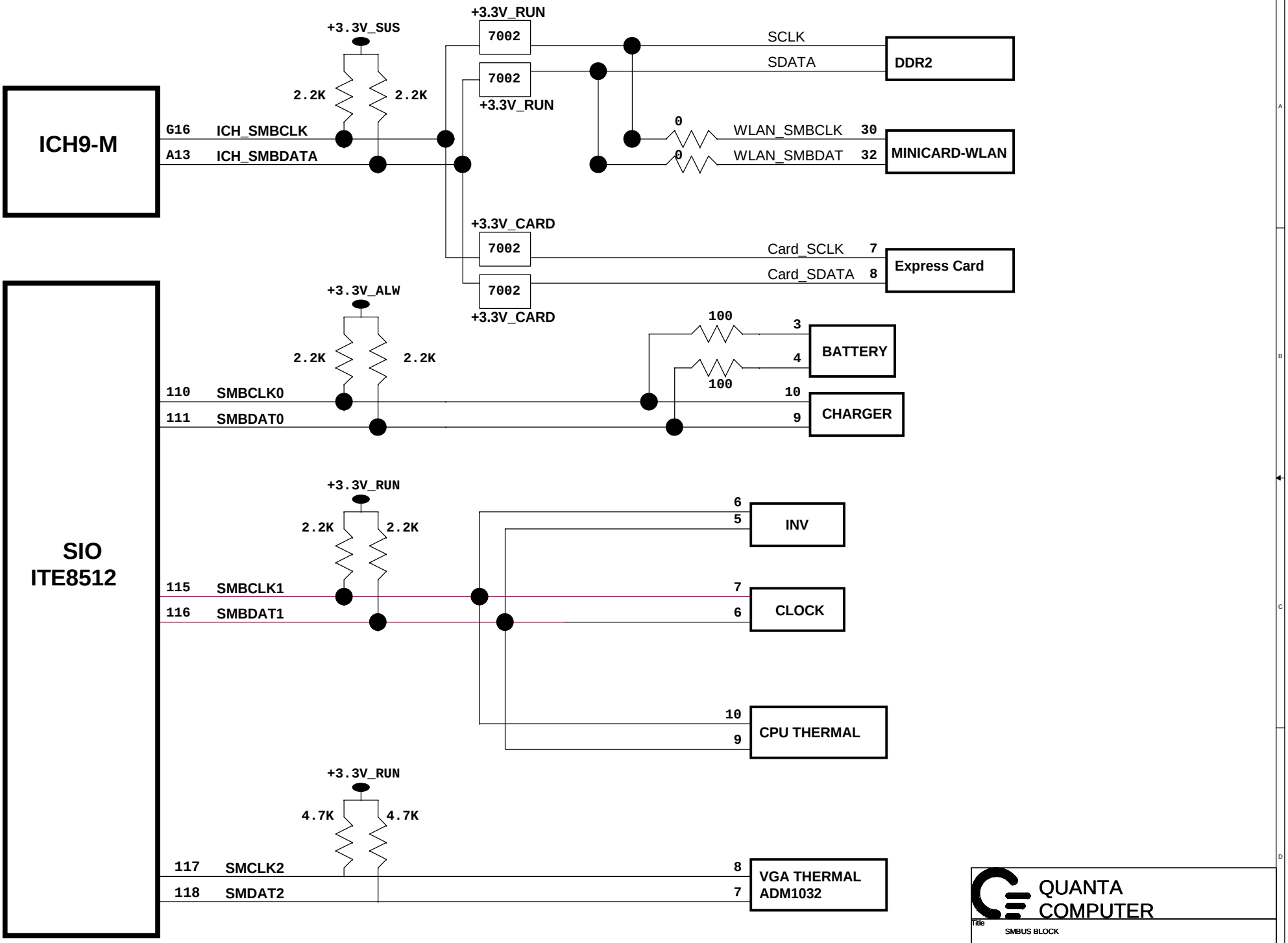
QUANTA COMPUTER

Title	+VCC_GFX_CORE(MAX8792)	
Size	Document Number VM8G	Rev 1A
Date: Tuesday, February 17, 2009	Sheet 49 of 58	

Reserved for EMI.

QUANTA COMPUTER

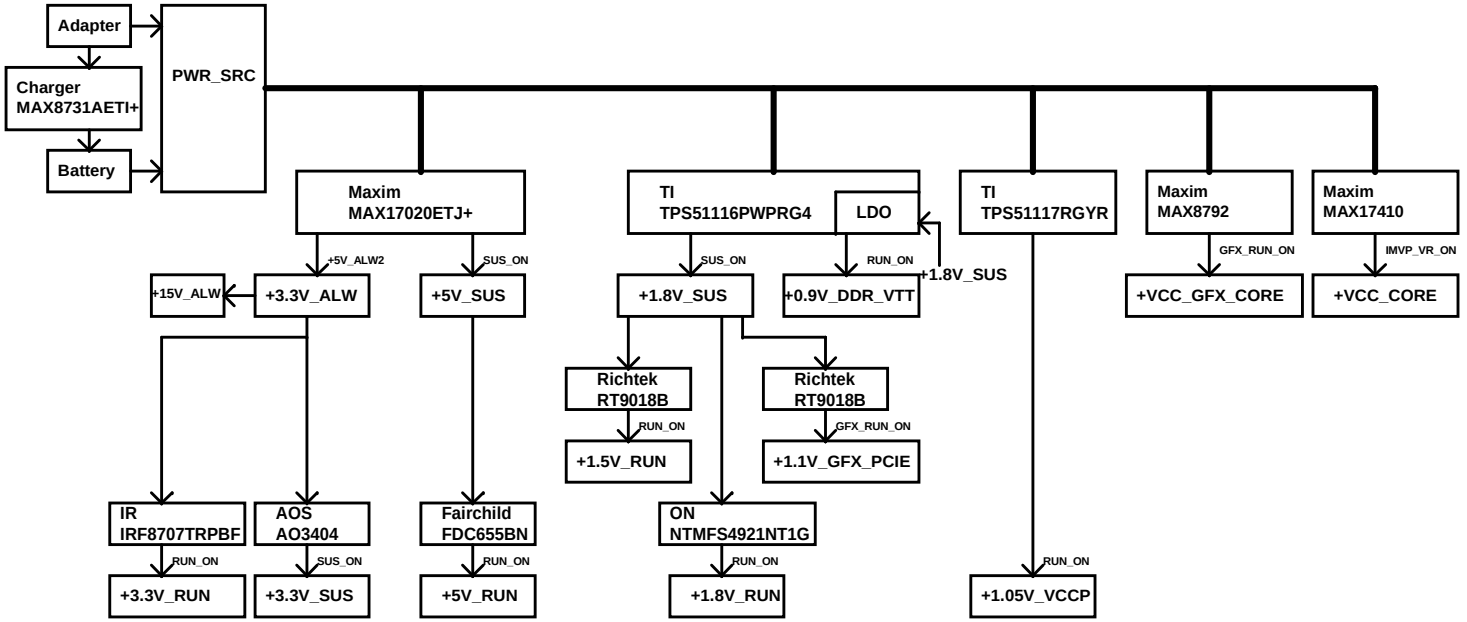
Title	EMI CAP	
Size	Document Number VM8G	Rev 1A
Date: Saturday, February 14, 2009	Sheet 50 of 58	



QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number VM8G	Rev 1A
Date: Saturday, February 14, 2009	Sheet 51 of 58	

VER : 1A



QUANTA COMPUTER

Title	Power Block Diagram	
Size	Document Number VM8G	Rev 1A
Date: Saturday, February 14, 2009	Sheet 52 of 58	