

Genesis-1 Block Diagram

LGS-1 91.4RQ01.001

JULY. 18, 2011

PCB Layer Stackup

L1:Component
L2:GND
L3:Signal 1
L4:VCC
L5:Signal 2
L6:Signal 3
L7:VCC
L8:Signal 4
L9:GND
L10:Component

Battery Charger/Selector

BQ24760 75

INPUTS	OUTPUTS
VINT20	CHARGER_OUT12

System DC/DC

TPS51220ARSN 79

VINT20	VCC5M
	VCC3M

CPU DC/DC

VT1318M/VT1324S 80

VCC5M_OUT	VCCCPUCORE
-----------	------------

GMCH GFX CORE

VT1324S 81

VCC5M_OUT	VCCGFXCORE
-----------	------------

VCC1R5B

VT355FCX 86

VCC5M_OUT	VCC1R5B
-----------	---------

VCC0R675B

MAX1510 87

VCC1R35A
VT356FCX 88

VCC5M_OUT	VCC1R35A
VCC1R35A	VCC0R675B

VCC1R8B

BD9139 89

VCC5M_OUT	VCC1R8B
-----------	---------

VCC1R05AMT

VT356FCX 85

VCC5M_OUT	VCC1R05LAN
-----------	------------

VCC1R05B_VTT

VT356 84

VCC5M_OUT	VCC1R05B_VTT
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VCCSA

VT371 90

VCC5M_OUT	VCCSA
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File

Block Diagram

Size
A3

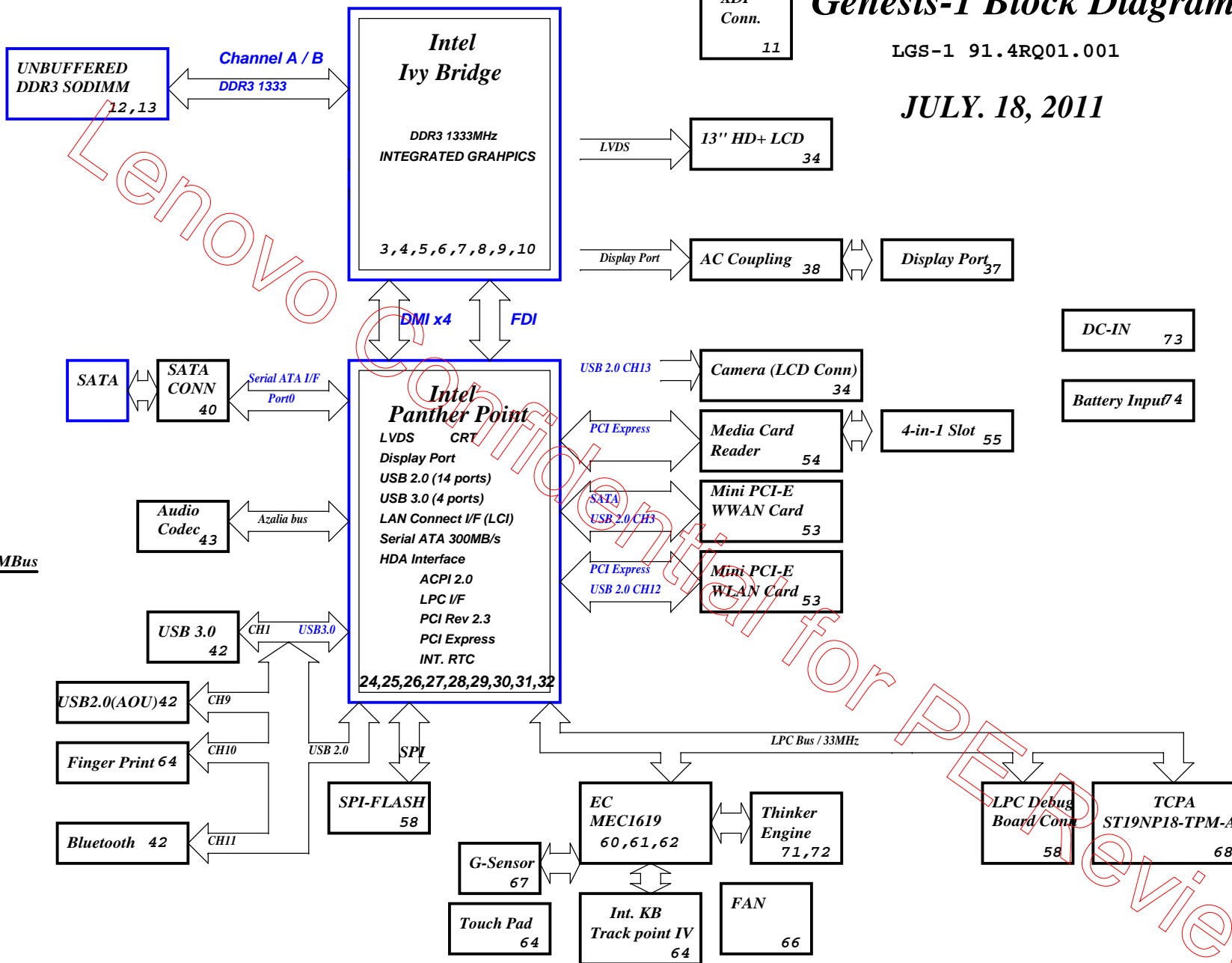
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Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

IBEXPEAK-M	39	38	48	49	Planar ID Version	Planar PCB Version
PLANAR_IDn	3	2	1	0		
	0	0	0	0	Genesis-1 initial	N/A
	0	0	0	1	FVT	N/A
	0	0	1	0	SIT	SC
	0	0	1	1		
	0	1	0	0		
	0	1	0	1		
	0	1	1	0		<Core Design>
	0	1	1	1		
	1	0	0	0		
	1	0	0	1		
	1	0	1	0		

[illegible]

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Title

Reference

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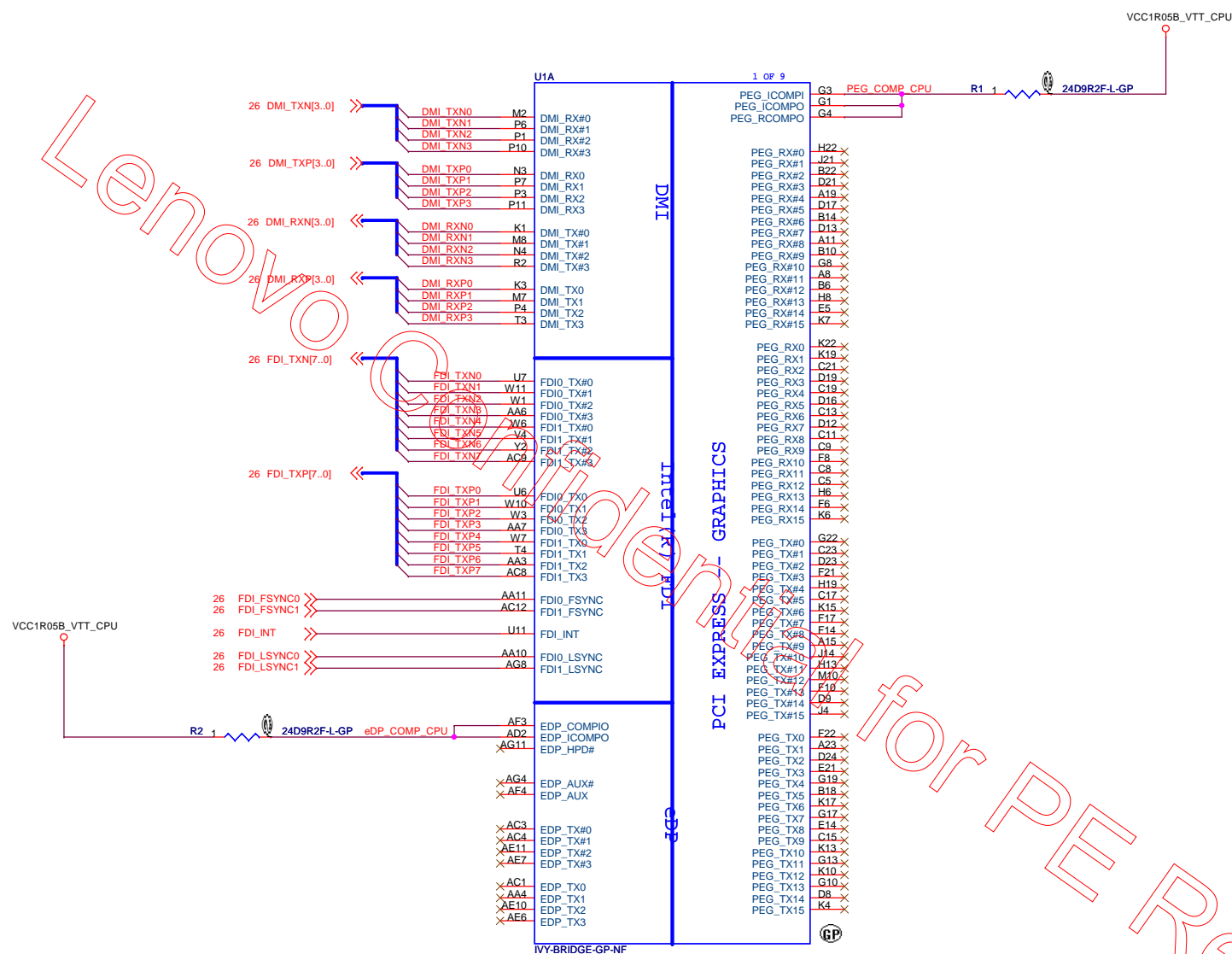
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Title **CPU(1/8):DMI/EDP/PEG/FDI**

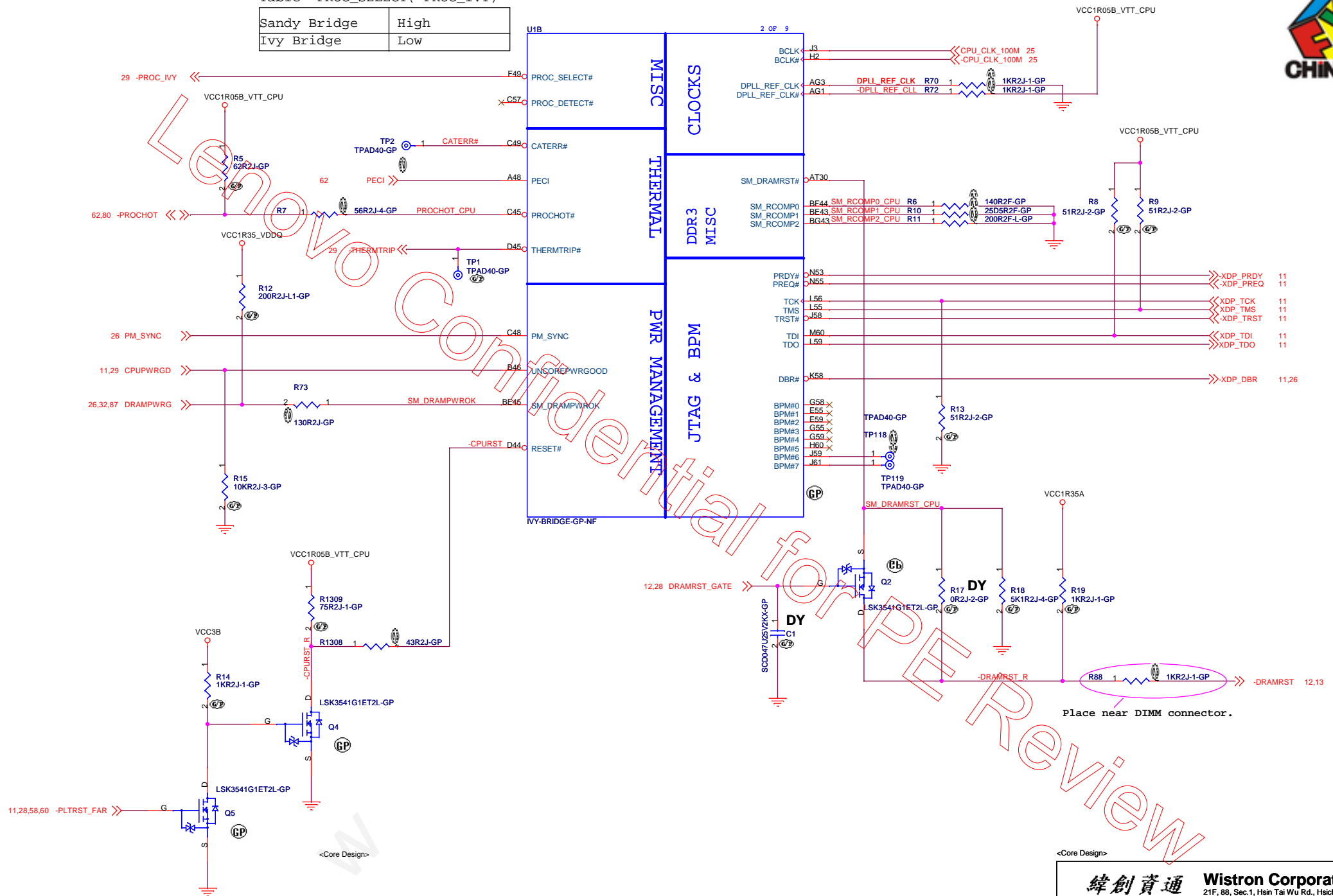
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Table -PROC_SELECT(-PROC_IVY)

Sandy Bridge	High
Ivy Bridge	Low



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Title CPU(2/8):CLK/MISC/JTAG

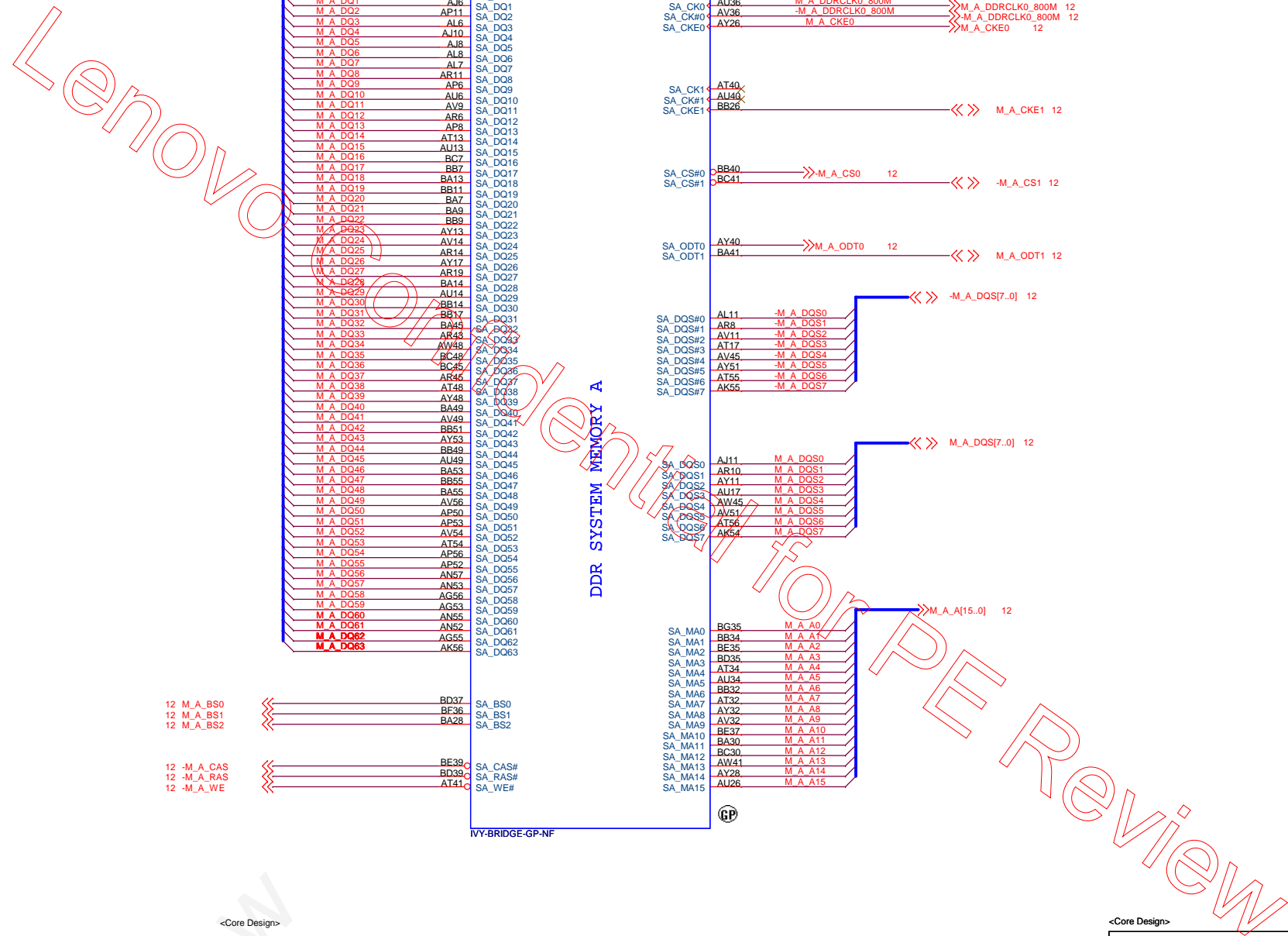
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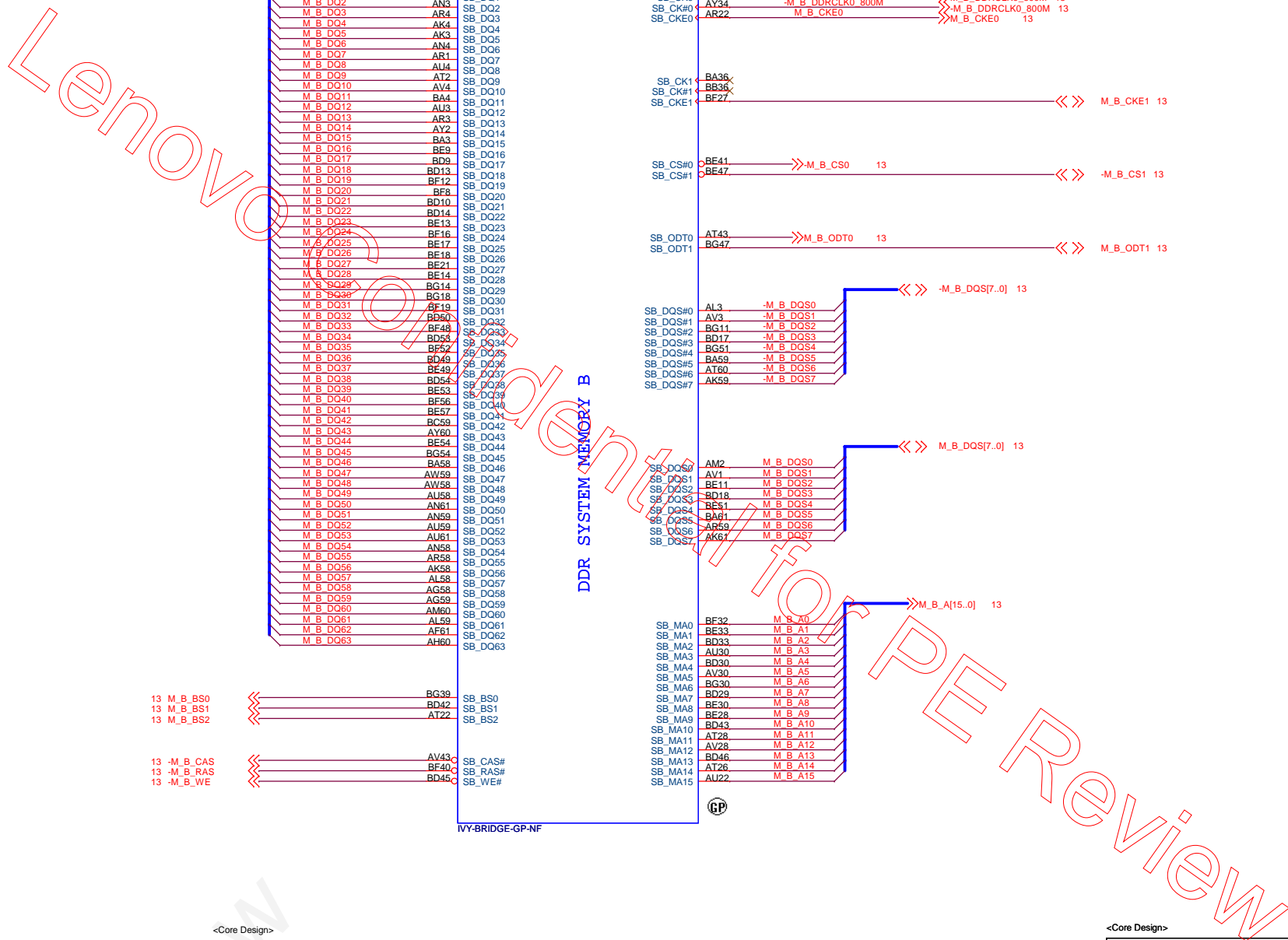
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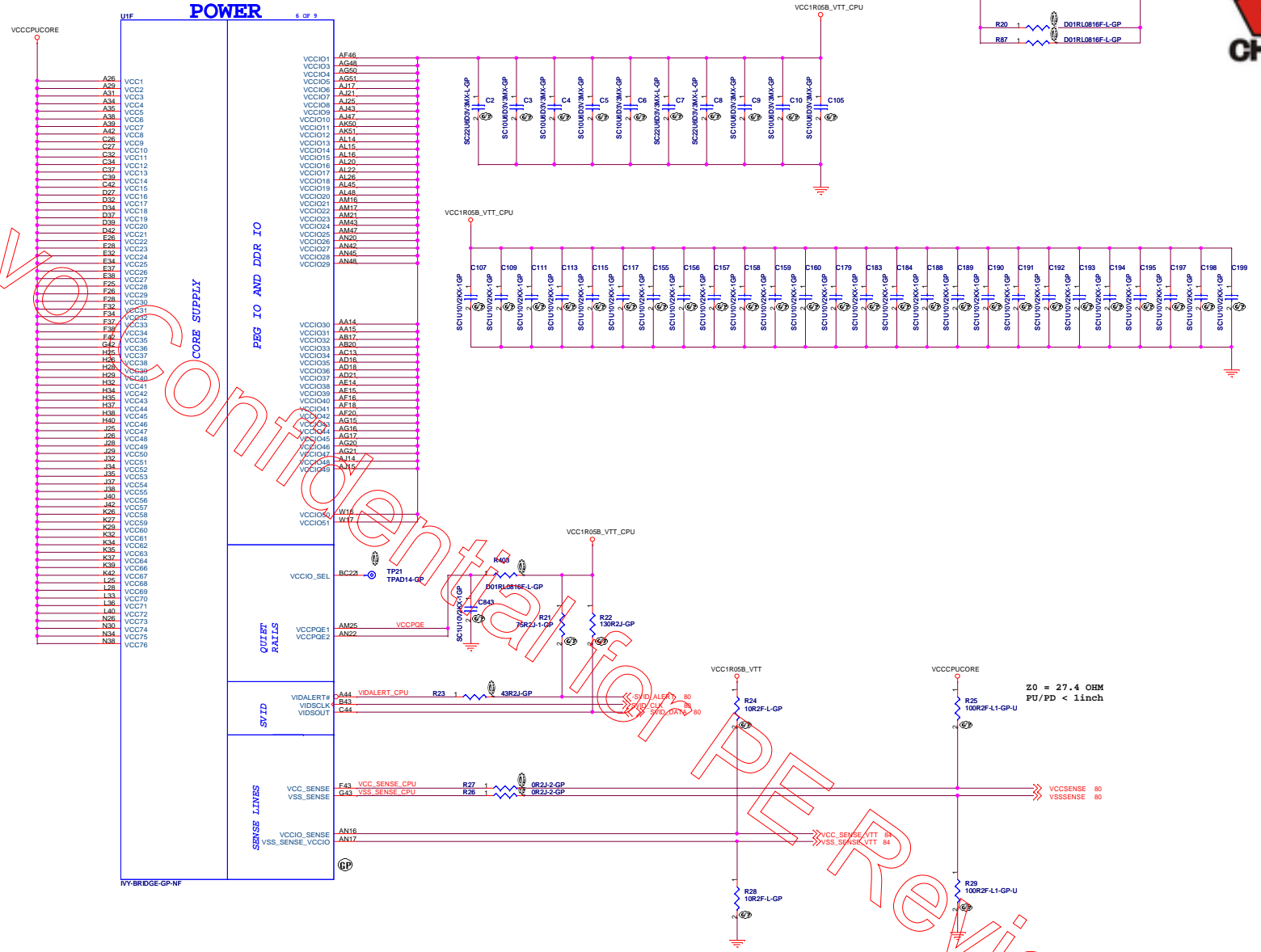


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Title			
CPU(4/8):DDR3 Channel-B			
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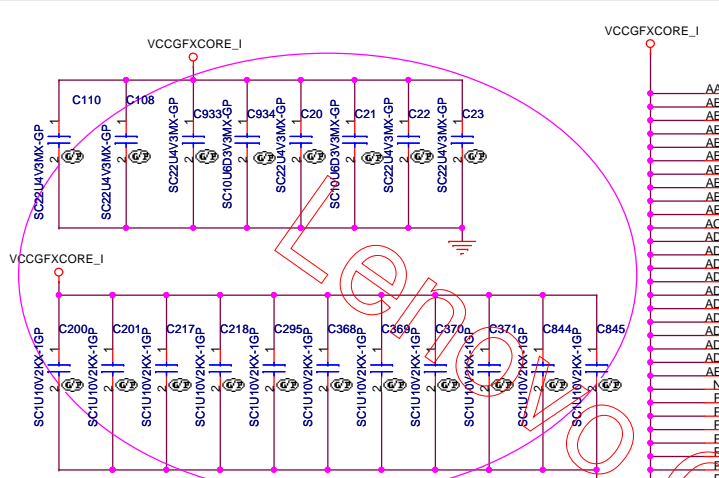
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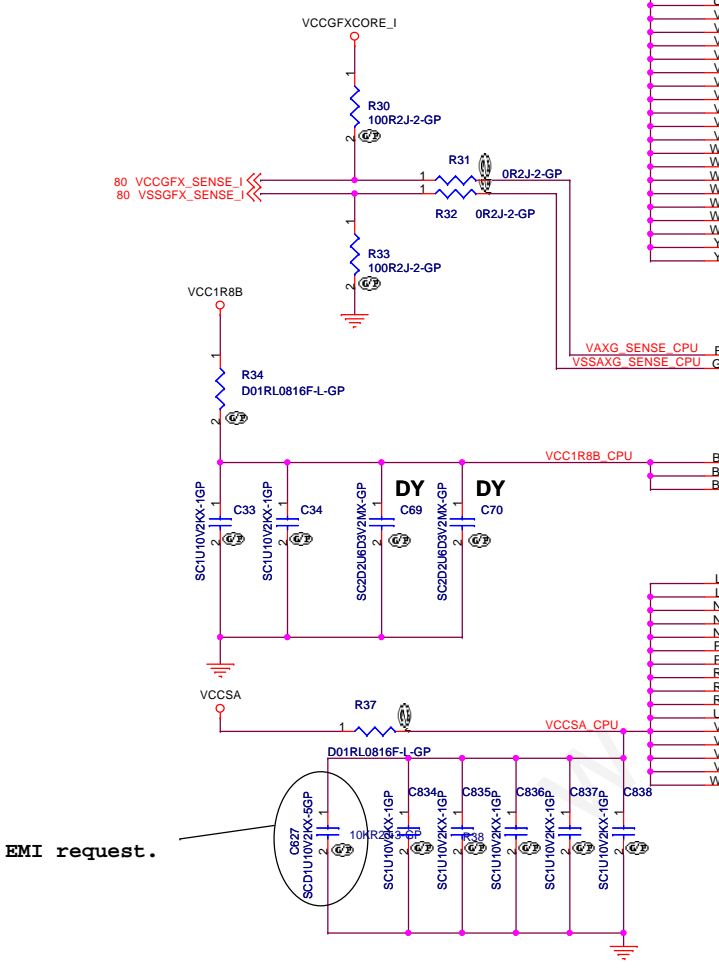


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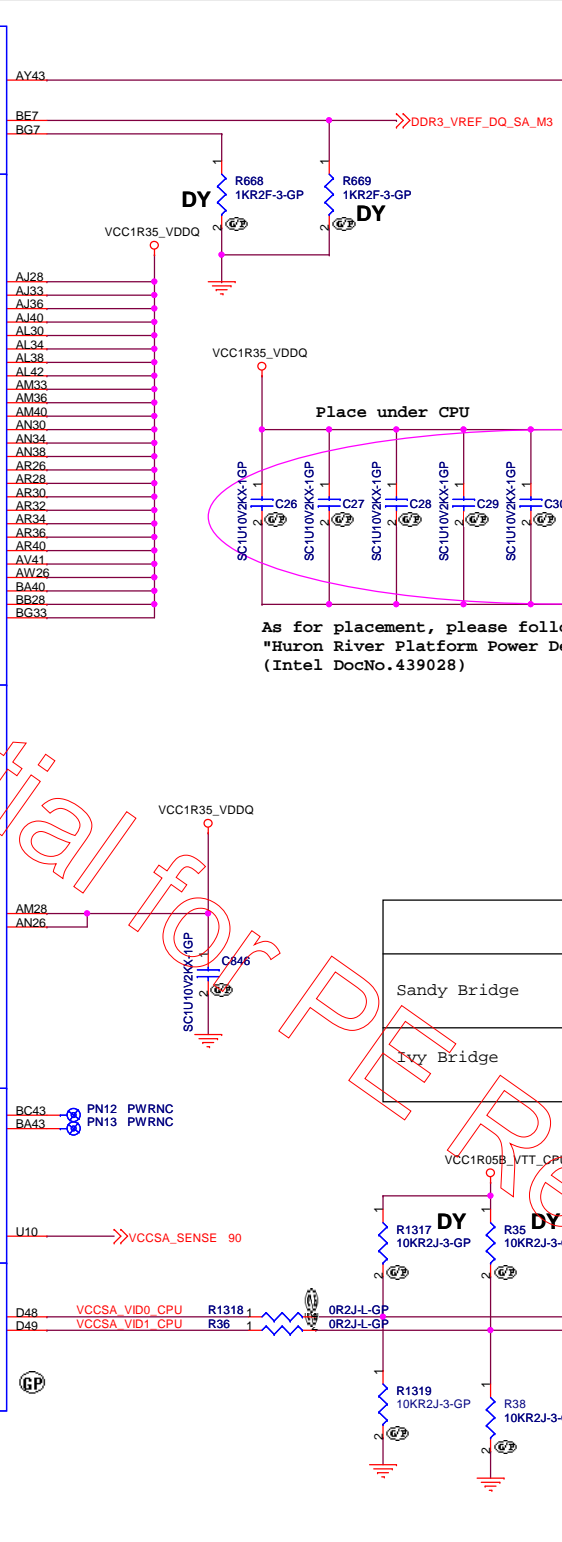
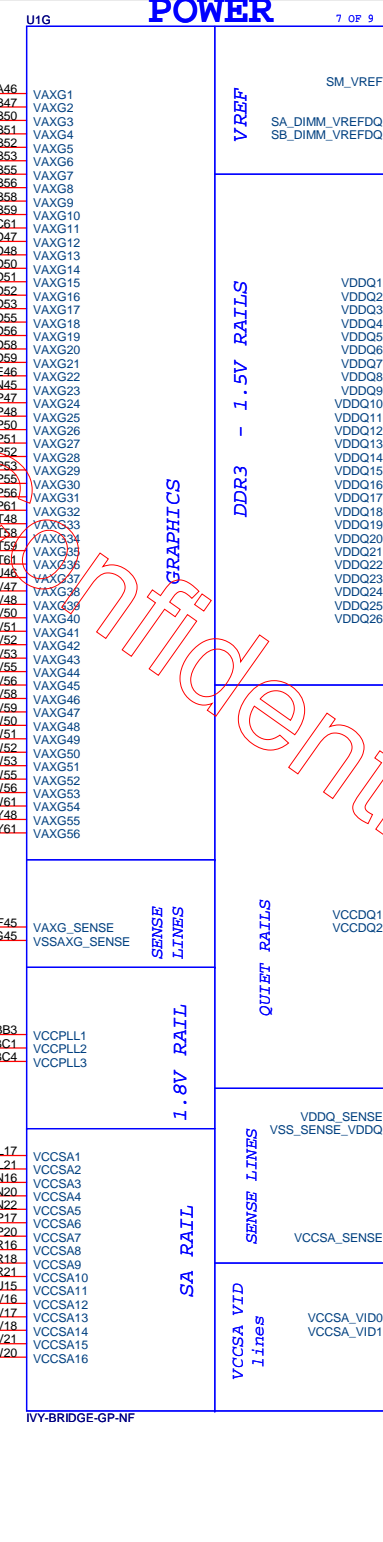
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As for placement, please follow
 "Chief River Platform Power Delivery Design Guide"
 (Intel DocNo.458544)



EMI request.



NEED SC2D2U4V2MX-1GP
78.22510.5FL

Place near CPU

Place under CPU

As for placement, please follow
 "Huron River Platform Power Delivery Design Guide Rev1.0"
 (Intel DocNo.439028)

	VCCSA_SEL0	VCCSA_SEL1	VCCSA
Sandy Bridge	LOW 0	0	0.90V
	0	1	0.80V
Ivy Bridge	High 1	0	0.725V
	1	1	0.675V

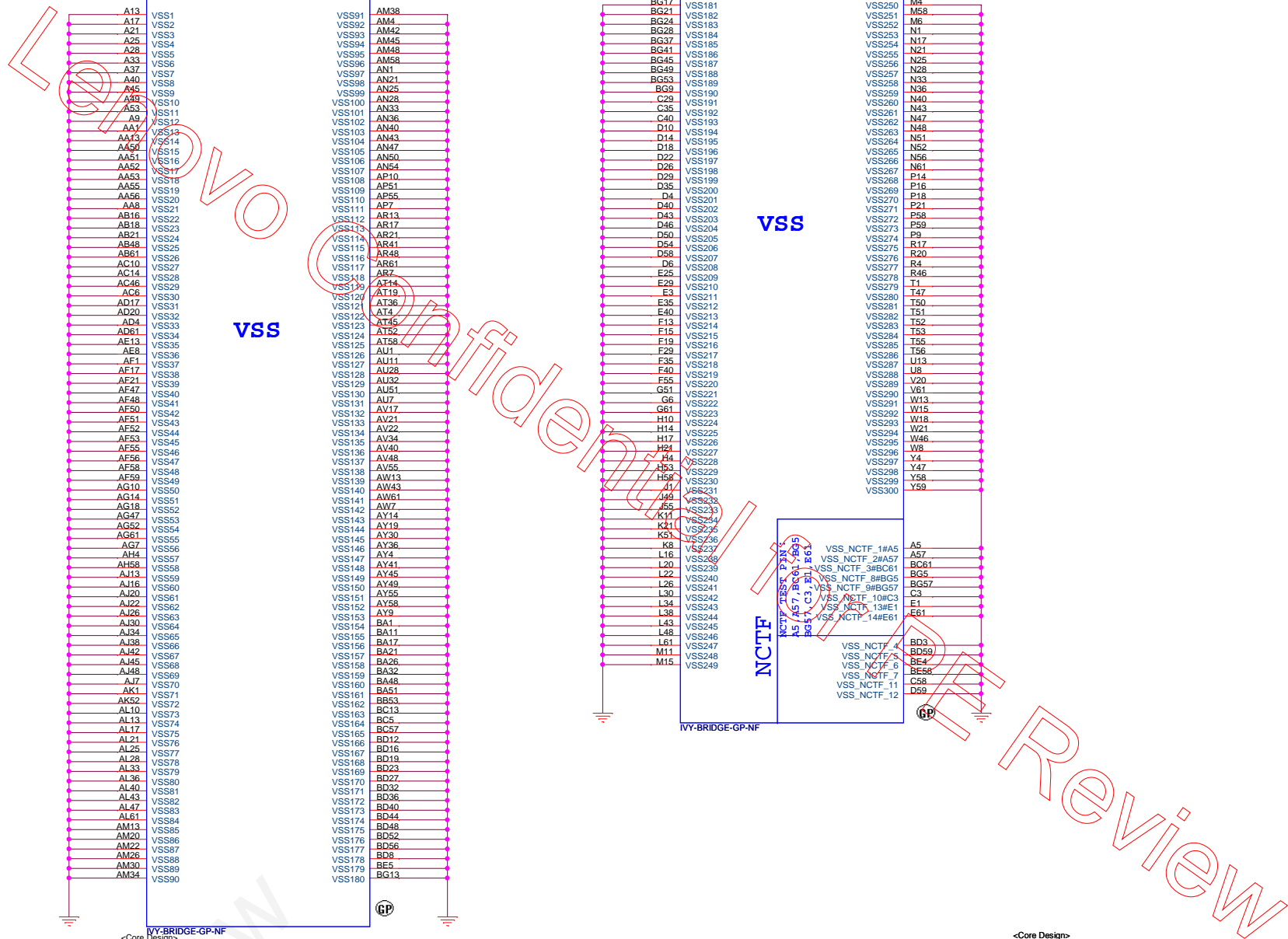
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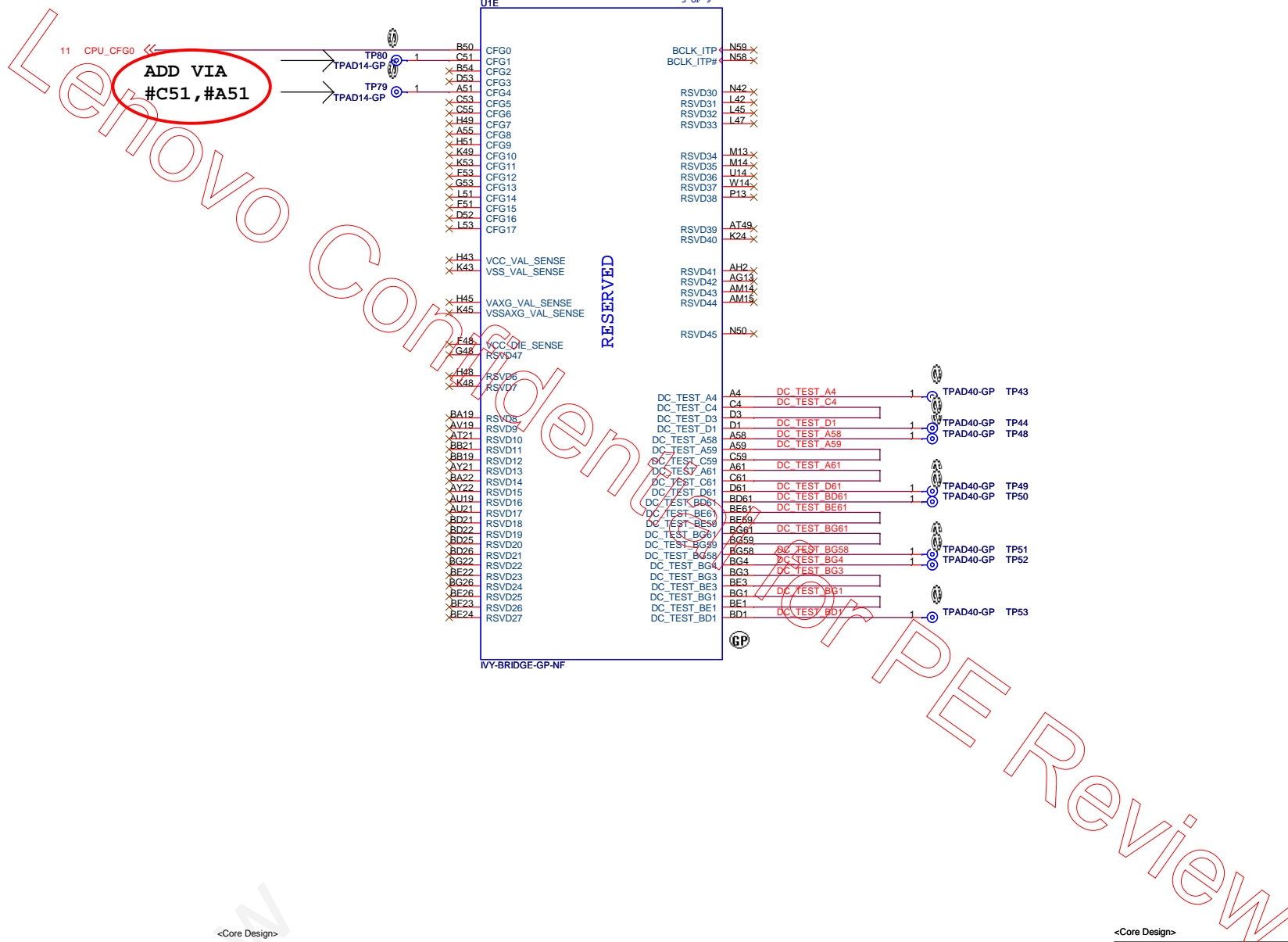
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Title: **CPU(6/8):Graphics Power**

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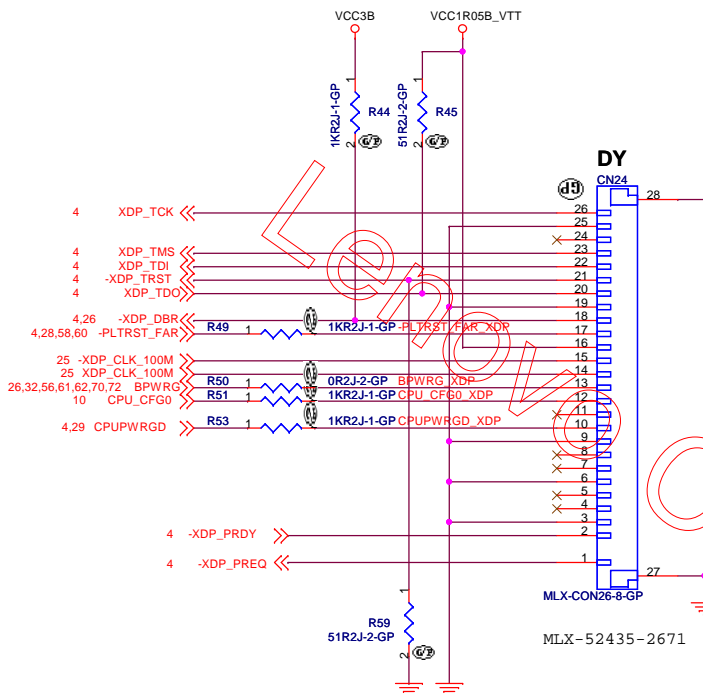


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Title			CPU(8/8):CFG/Reserved	
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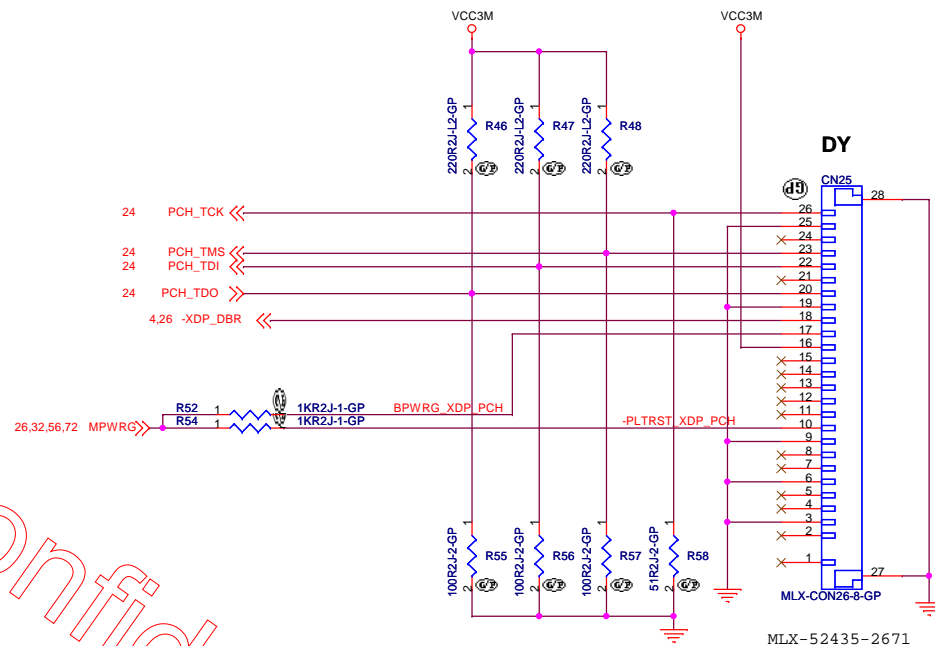


DEBUG Interface for Processor.

XDP1 NOTE:"ASM" FOR PDV/SDV ONLY

		ENABLE	DISABLE
TDO	R45	ASM	DY
TRST#	R59	ASM	ASM
DBRST#	R44	ASM	ASM
RESET#	R49	ASM	DY
CFG0	R51	ASM	DY
PWRGD	R53	ASM	DY
BPWRG	R50	ASM	DY
	CN24	ASM	DY

PDV Logic



DEBUG Interface for PCH.

XDP2 NOTE:"ASM" FOR PDV/SDV ONLY

		ENABLE	DISABLE
TDO	R46	220	DY
	R55	100	DY
TMS	R48	220	DY
	R57	100	DY
TDI	R47	220	DY
	R56	100	DY
TCK	R58	51	51
MPWRG	R52	ASM	DY
	R54	ASM	DY
	CN25	ASM	DY

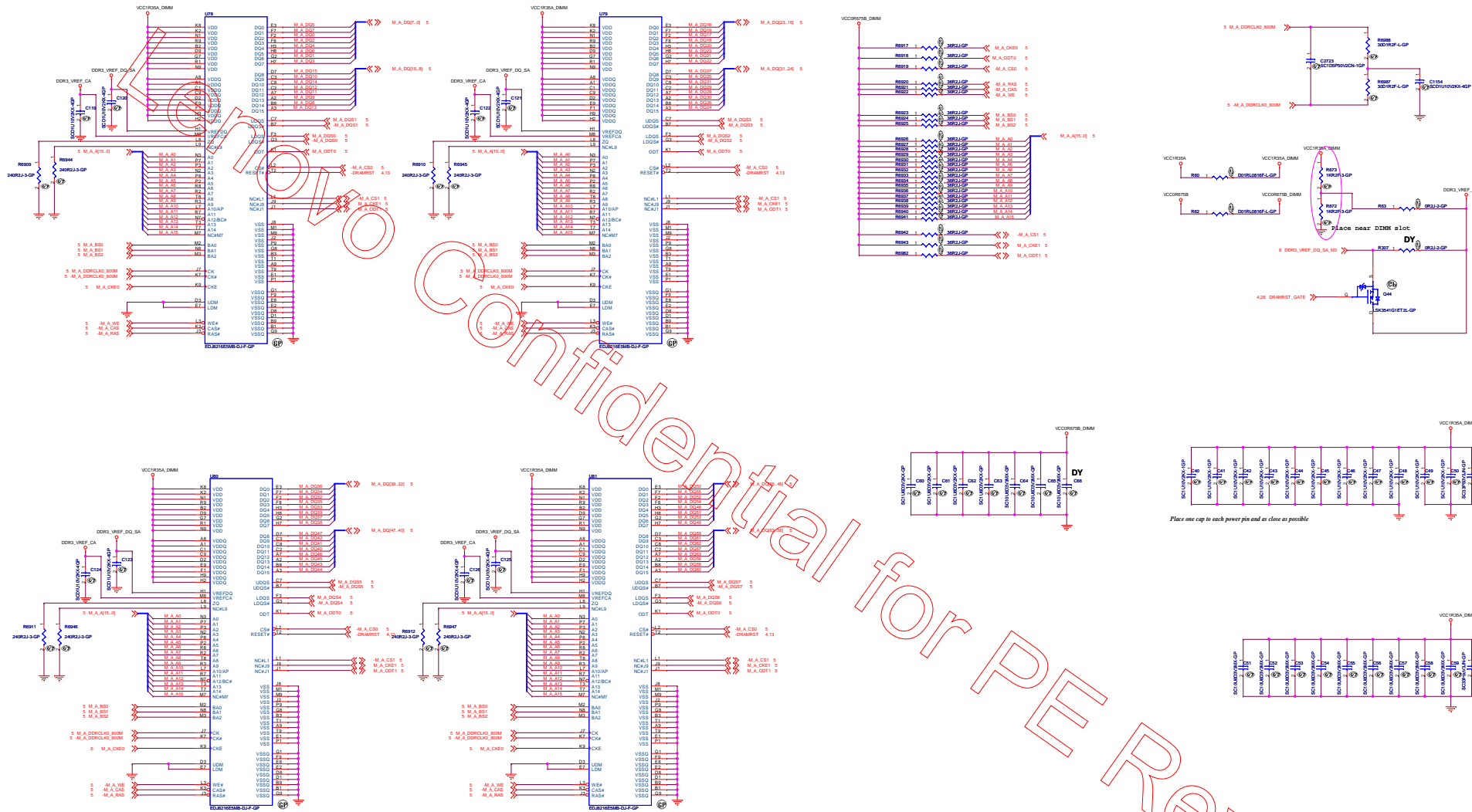
PDV Logic

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Title			XDP Connector
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Place one cap to each power pin and as close as possible



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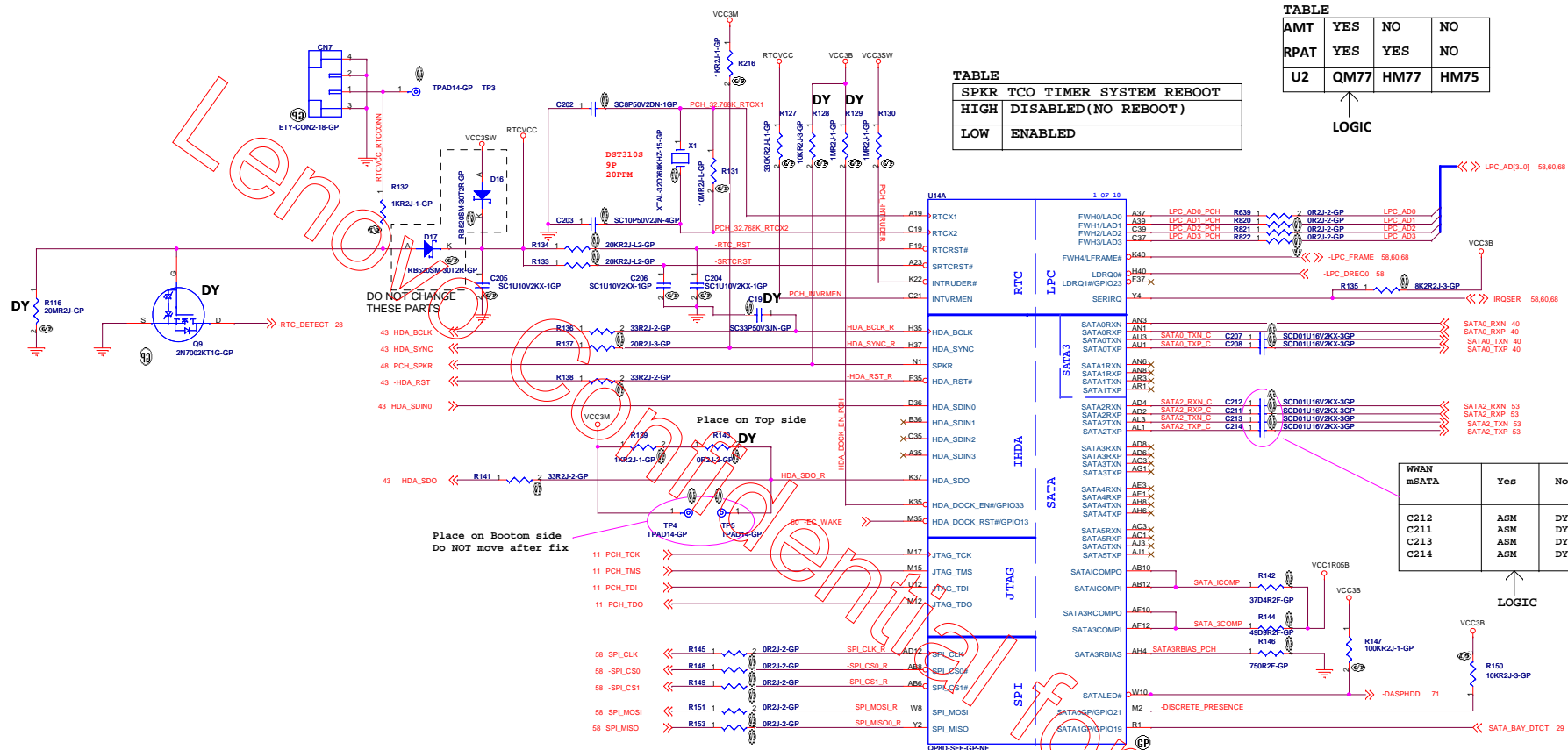


TABLE	SPKR	TCO	TIMER	SYSTEM	REBOOT
HIGH	DISABLED	(NO	REBOOT)		
LOW	ENABLED				

TABLE	AMT	YES	NO	NO
RPAT	YES	YES	NO	NO
U2	QM77	HM77	HM75	

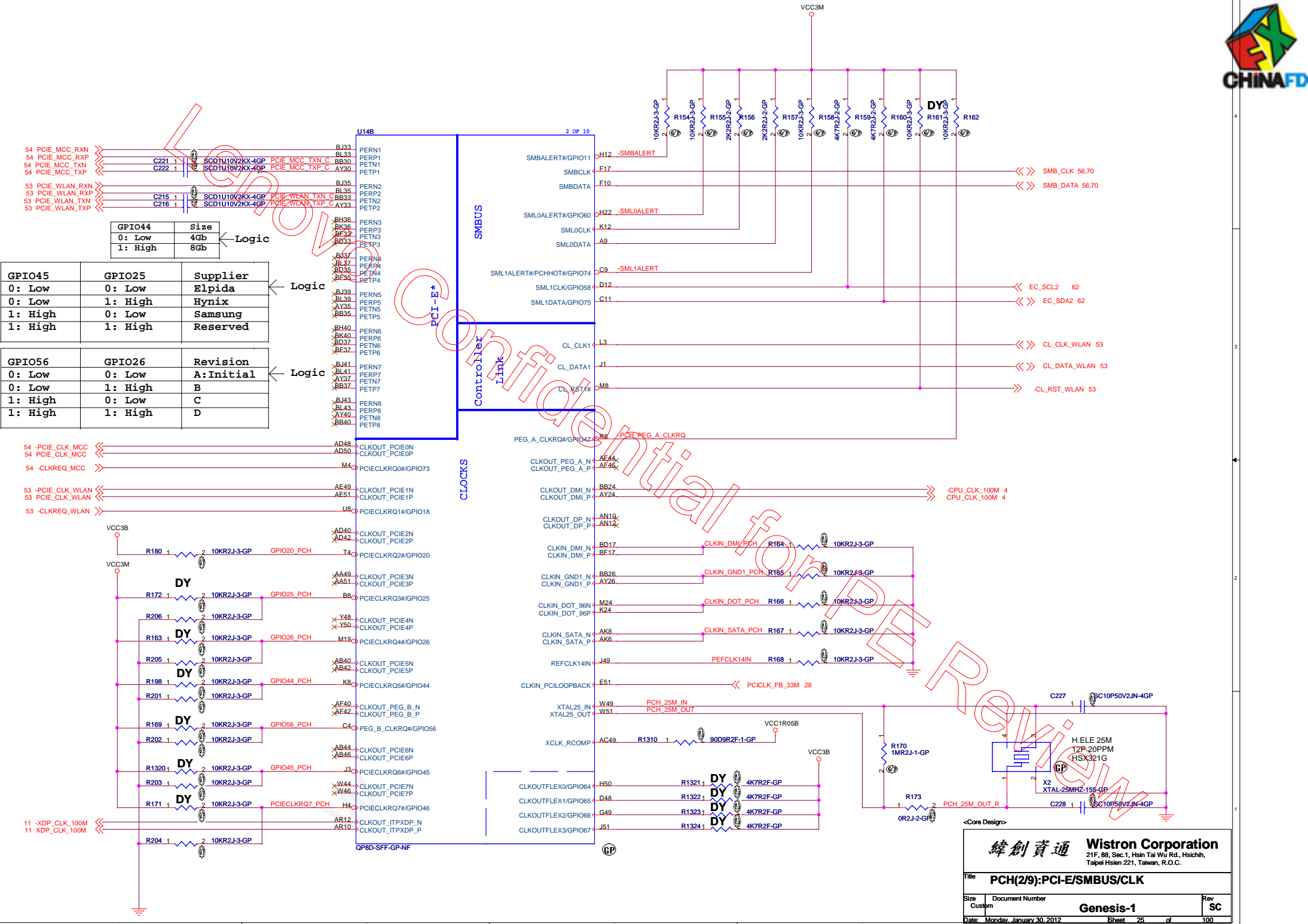
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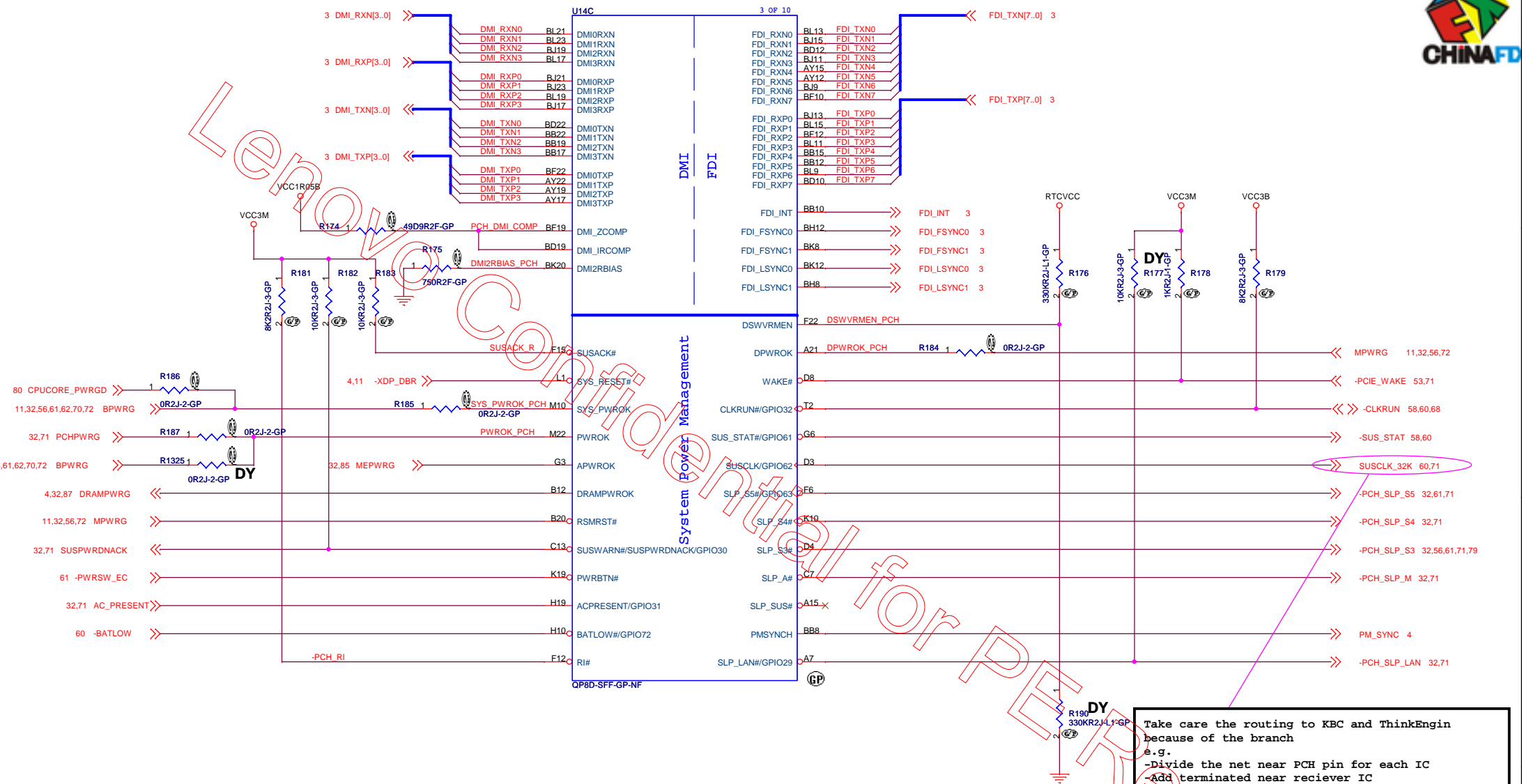
WWAN	Yes	No
C212	ASM	DY
C211	ASM	DY
C213	ASM	DY
C214	ASM	DY

LOGIC

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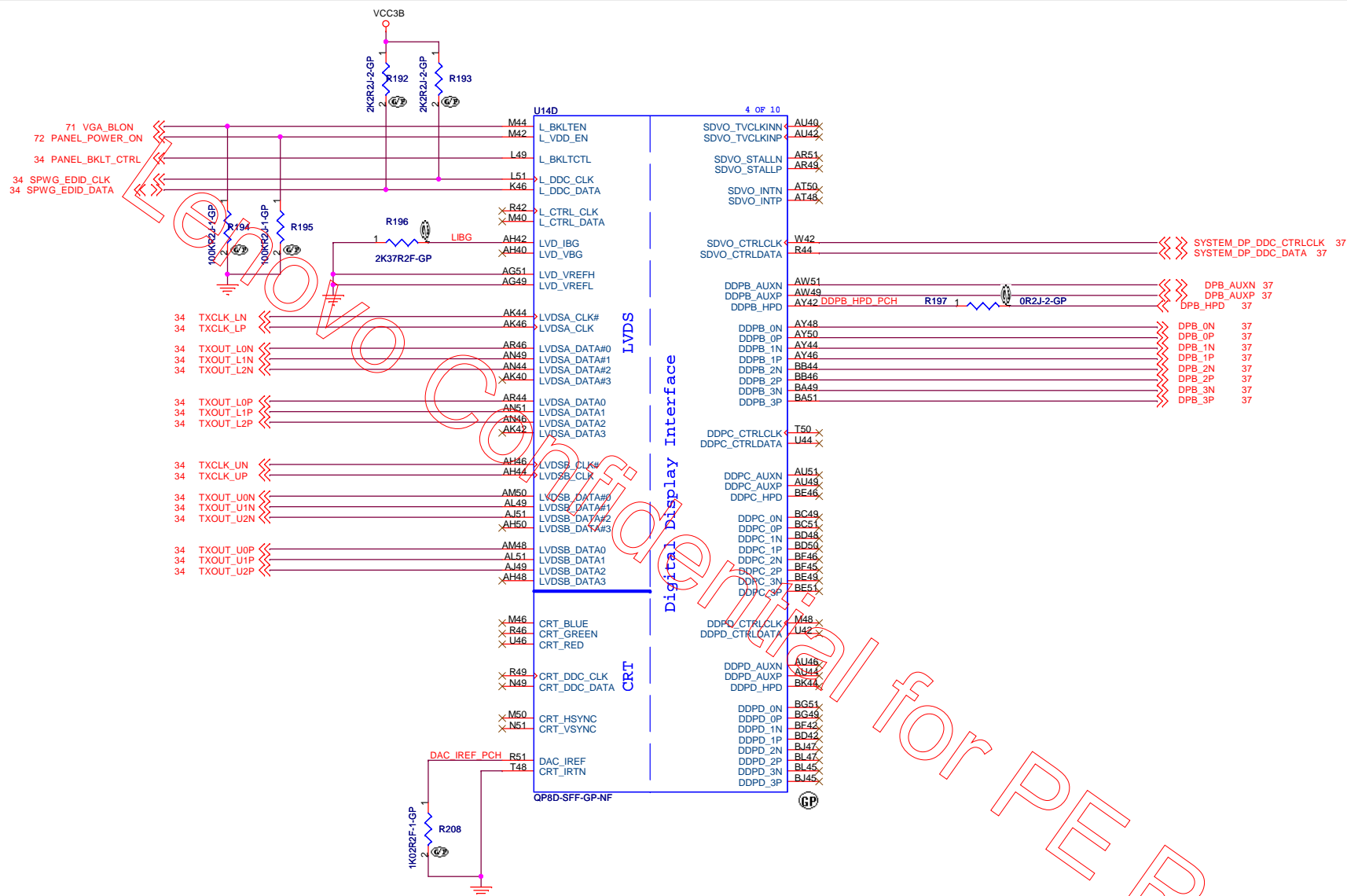


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Title PCH(3/9):DMI/FDI/PM		
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Title	PCH(4/9):LVDS/CRT/DDI
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Title	PCH(5/8) :PCI/USB/NVM
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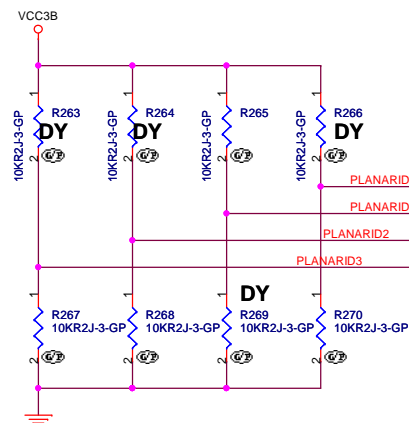
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GPIO8	INTEGRATED CLOCKING
HIGH	DISABLE(BTM)
LOW	ENABLE(FCIM)

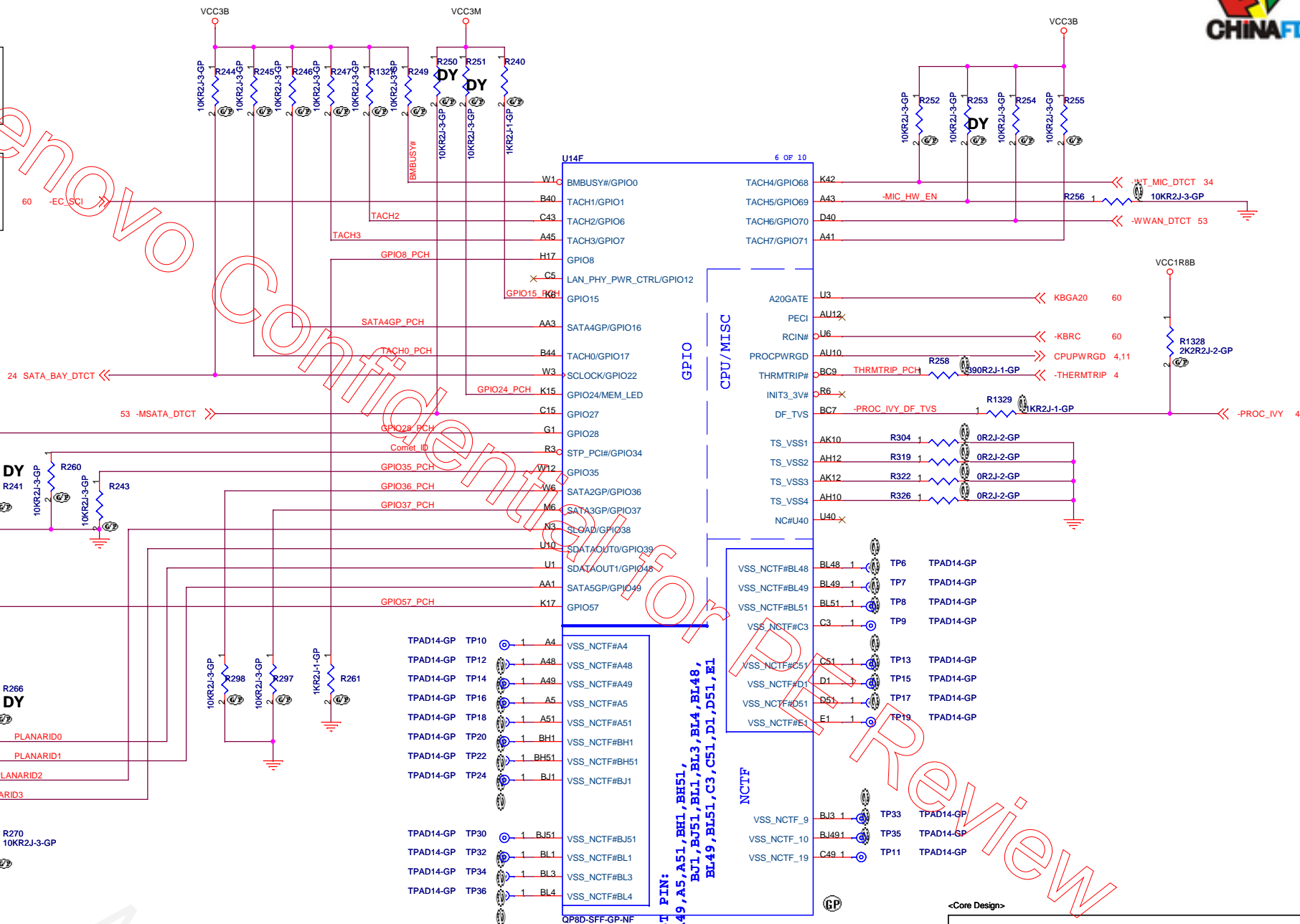
GPIO15	ME CRYPTO STRAP
HIGH	WITH CONFIDENTIALITY
LOW	NO CONFIDENTIALITY



PLANAR ID: 0000 for Initial Assessment

0001 for FVT

0010 for SIT



NCTF TEST PIN:

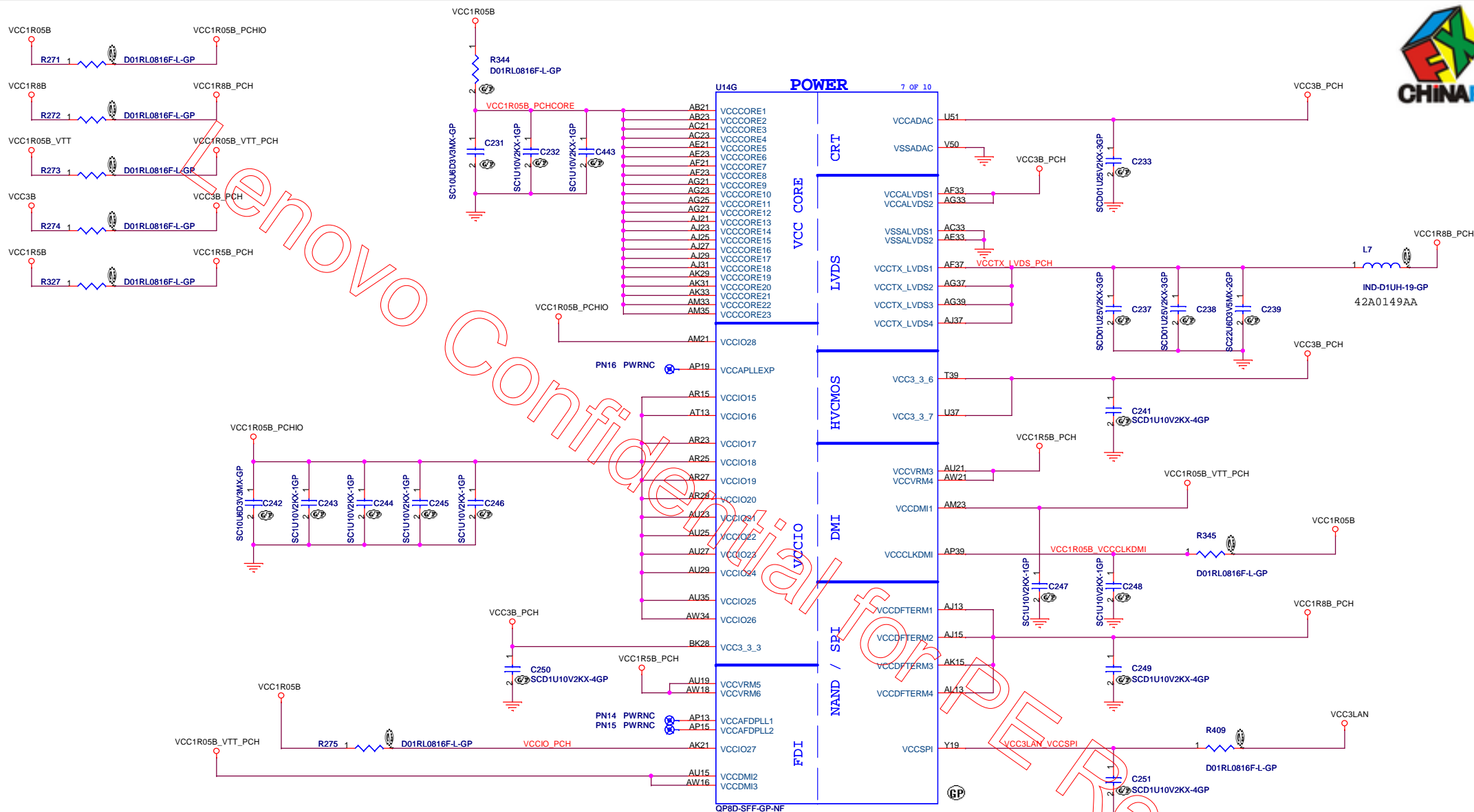
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Title **PCH(6/9):GPIO/NCTF/RSVD**

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Title	PCH(7/9):Power
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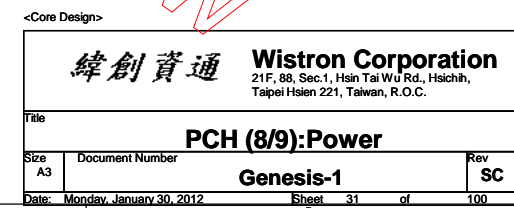
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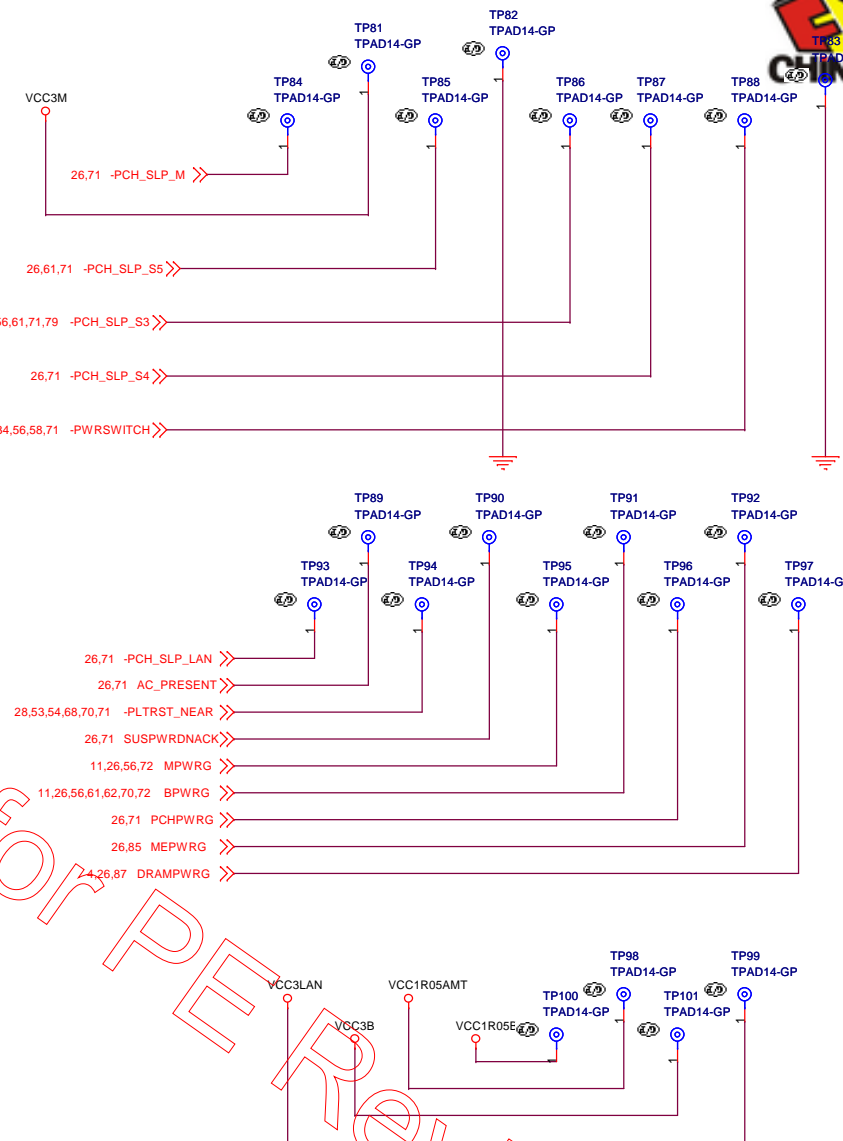
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TEST PAD FOR METS/APS



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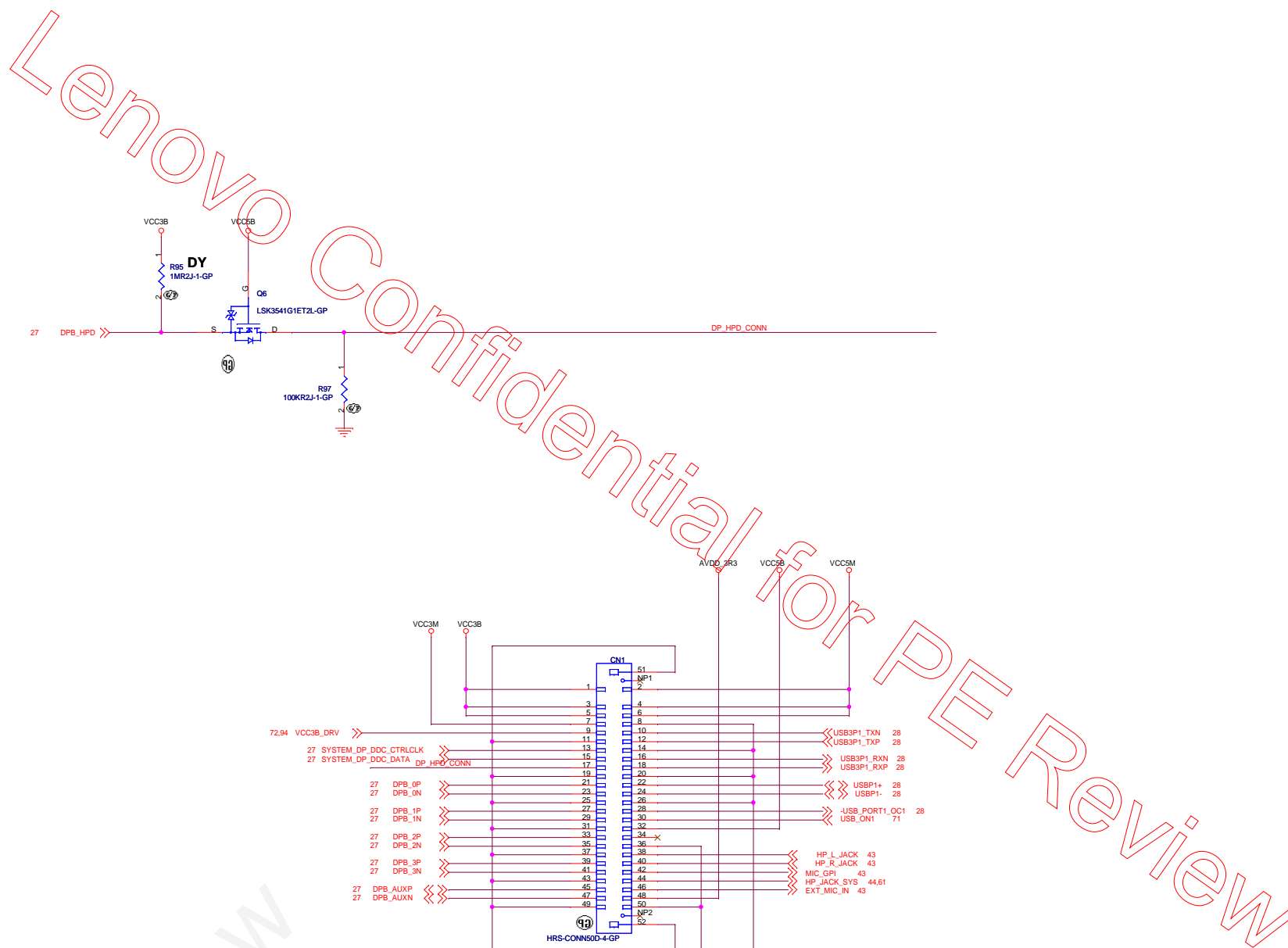
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Display Port Connector			Rev
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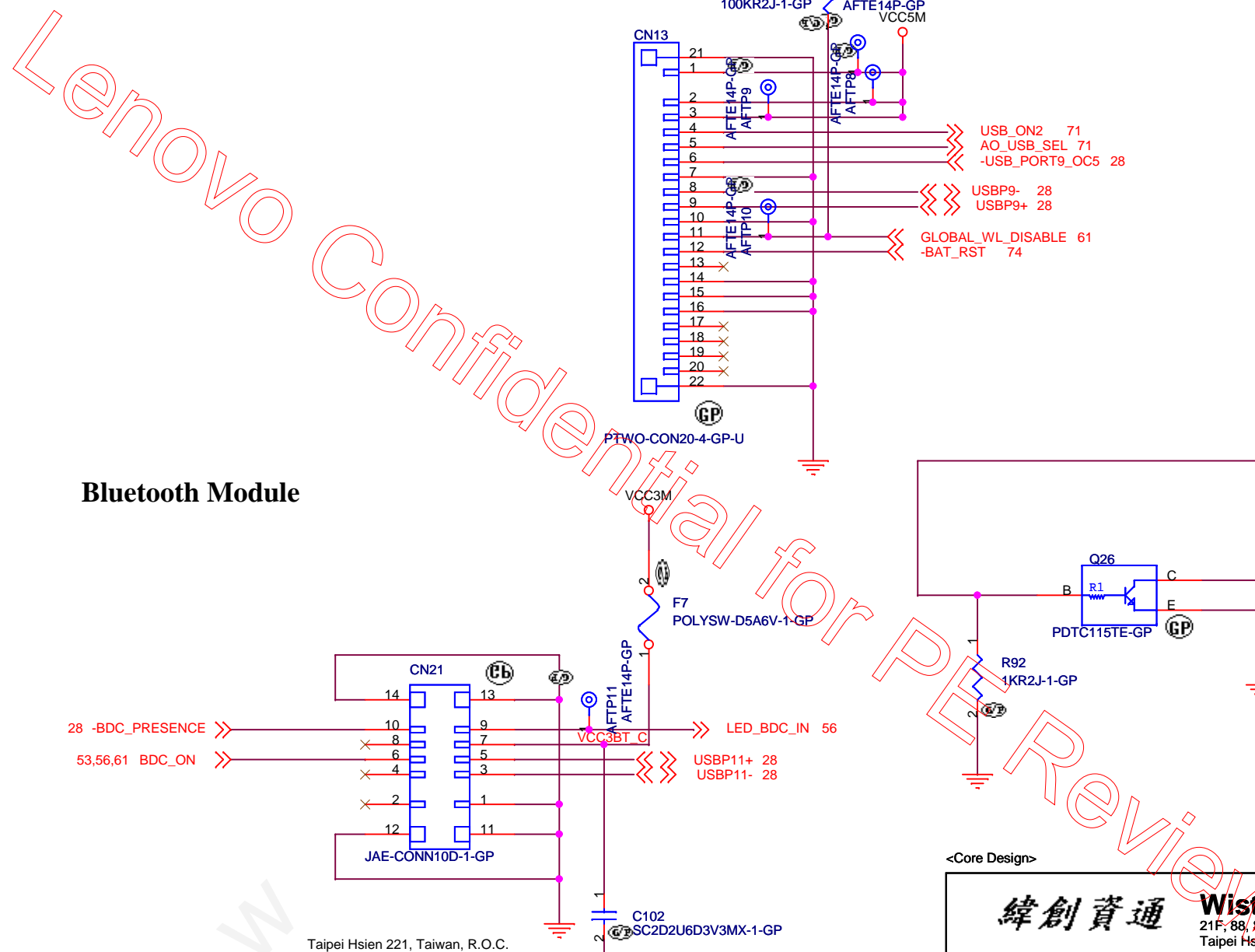
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Title

USB Connector & BT

Size
A4

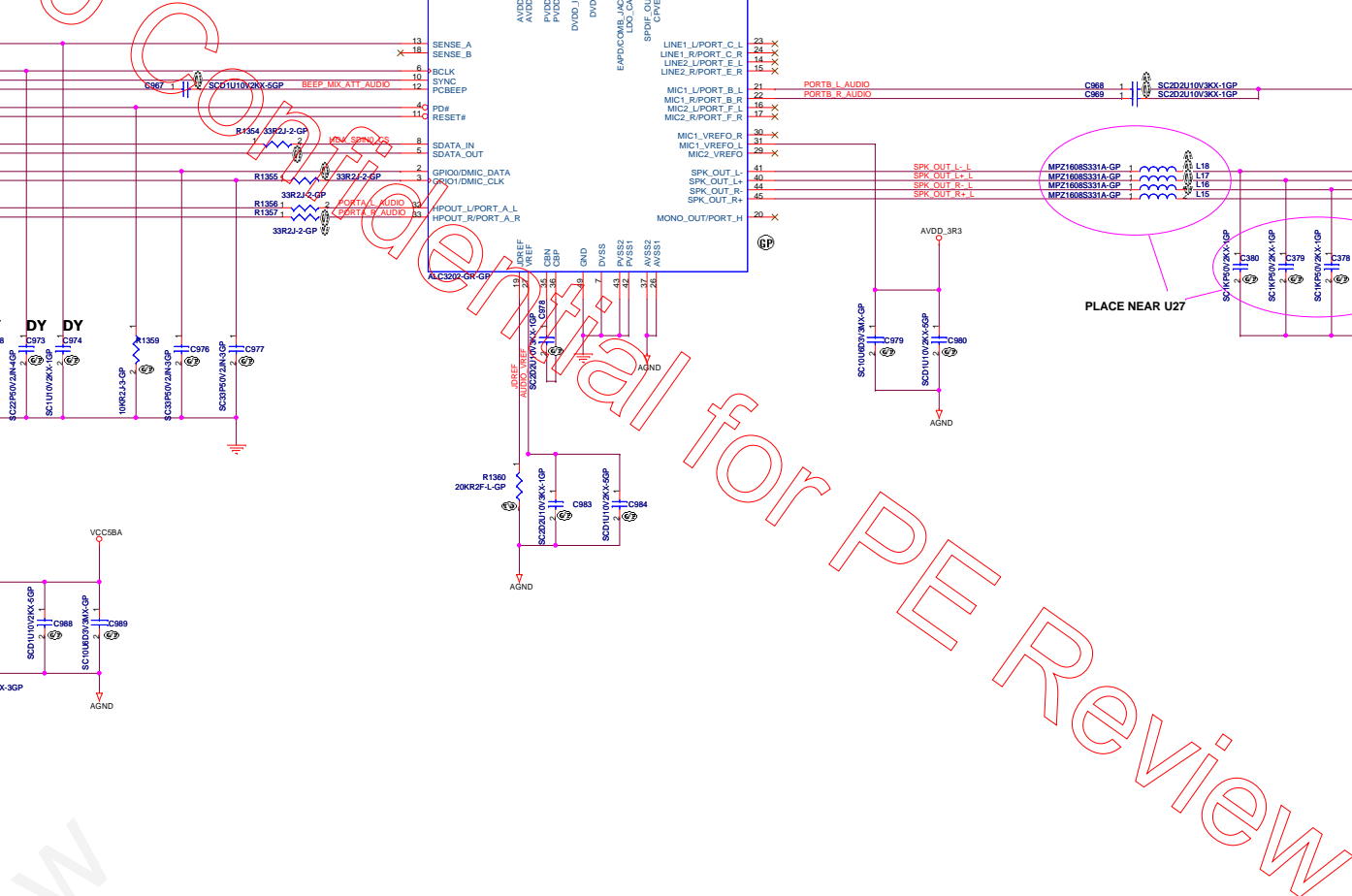
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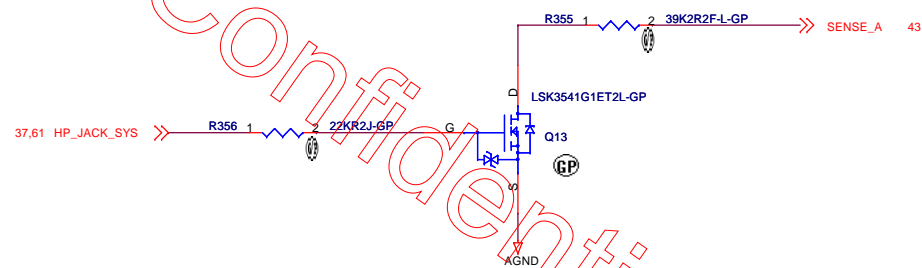
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File		AUDIO JACK SENSE	
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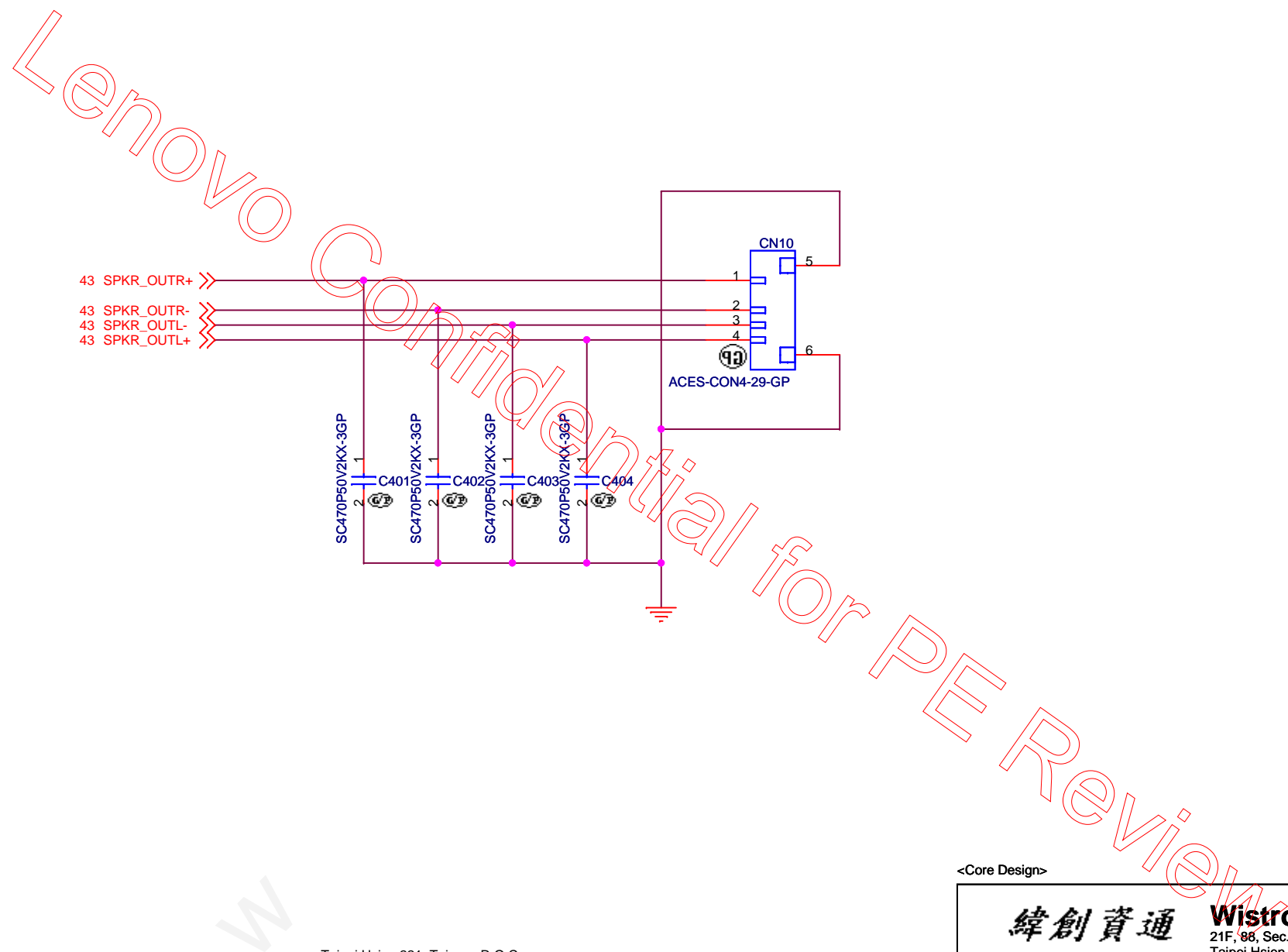
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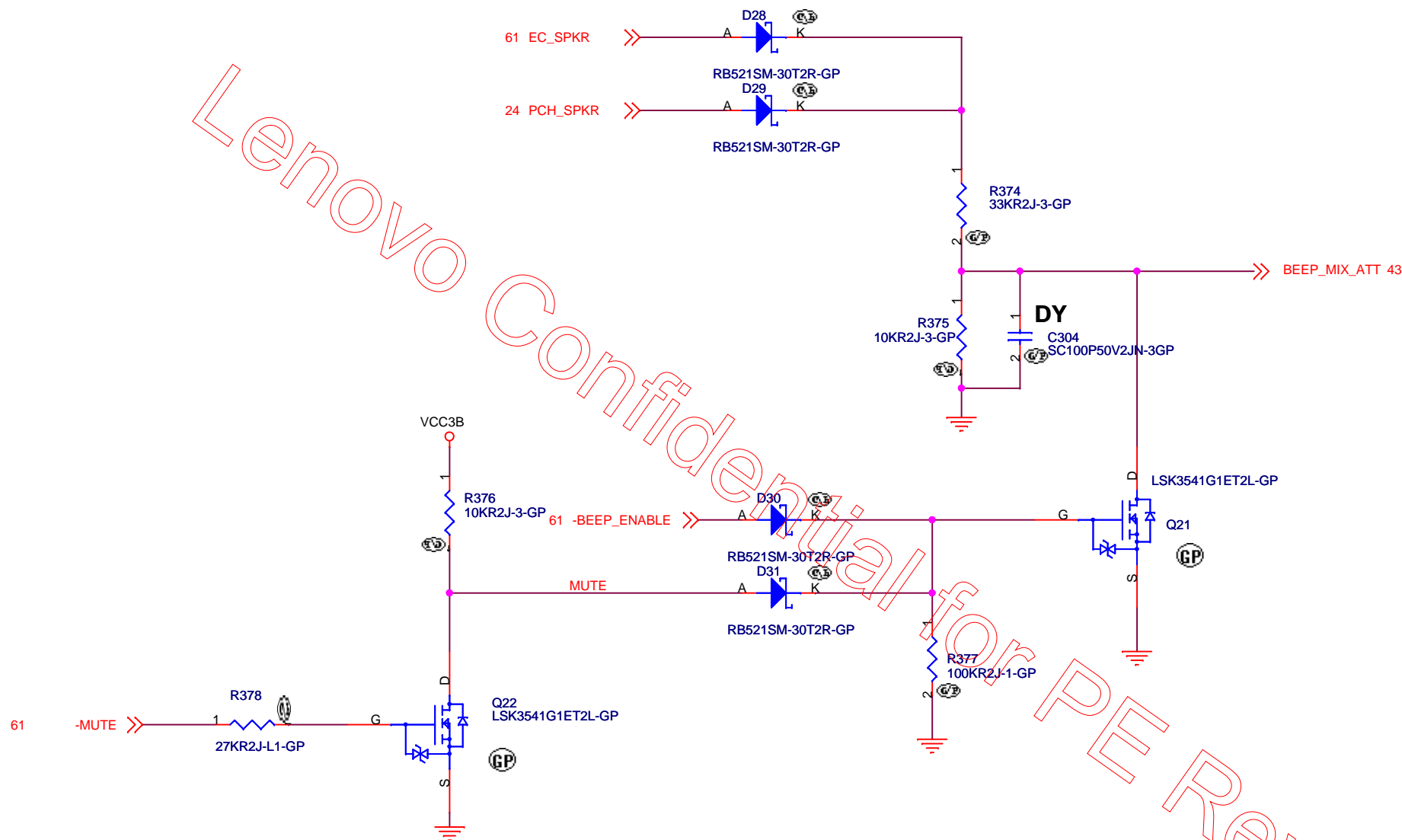
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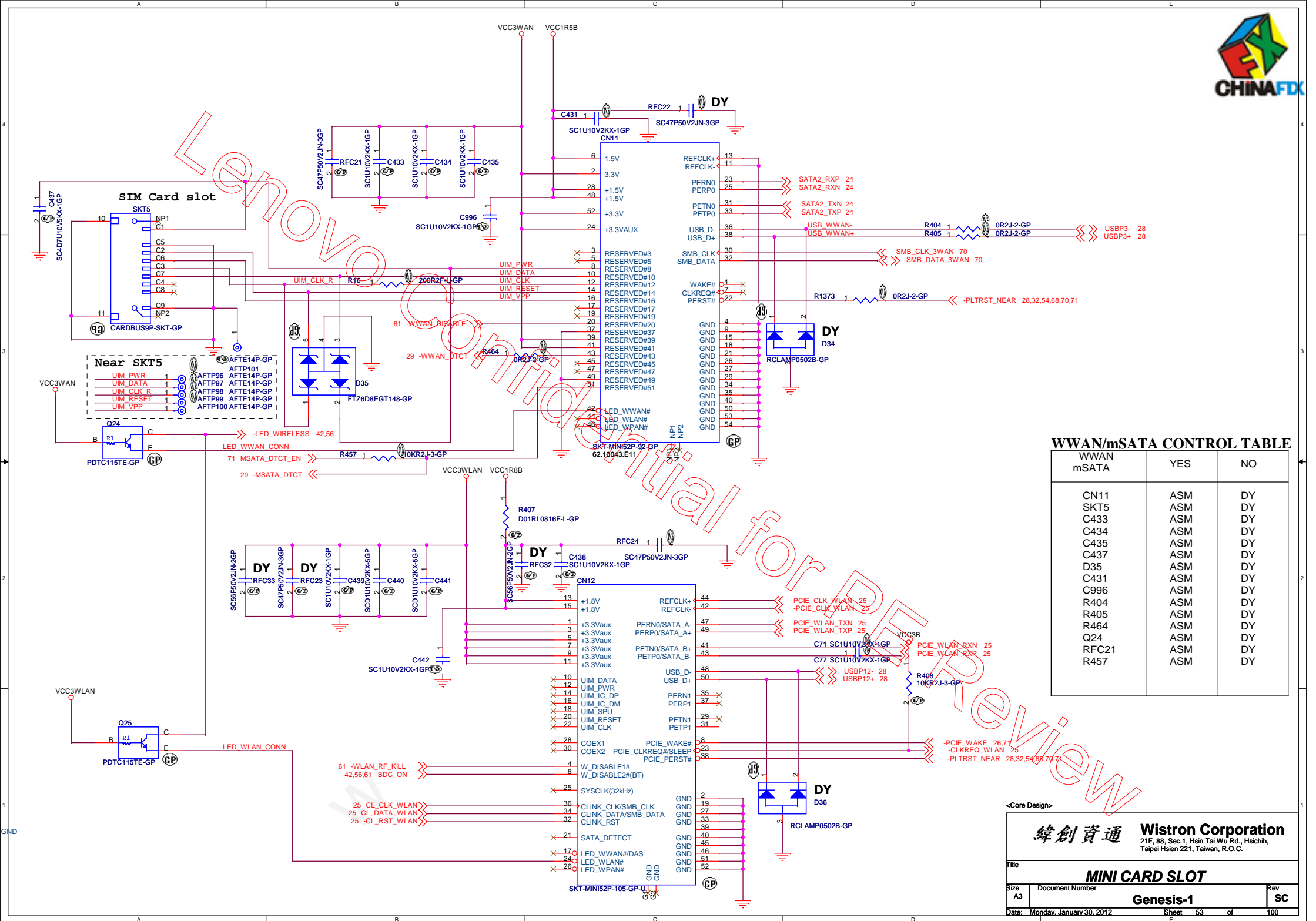
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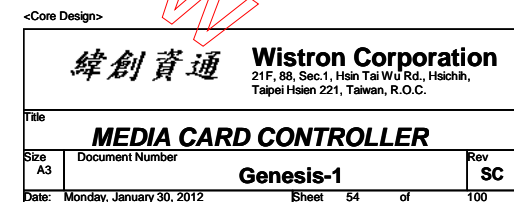
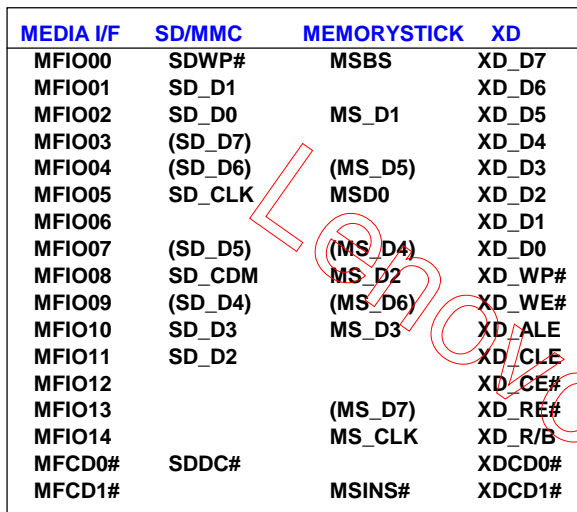
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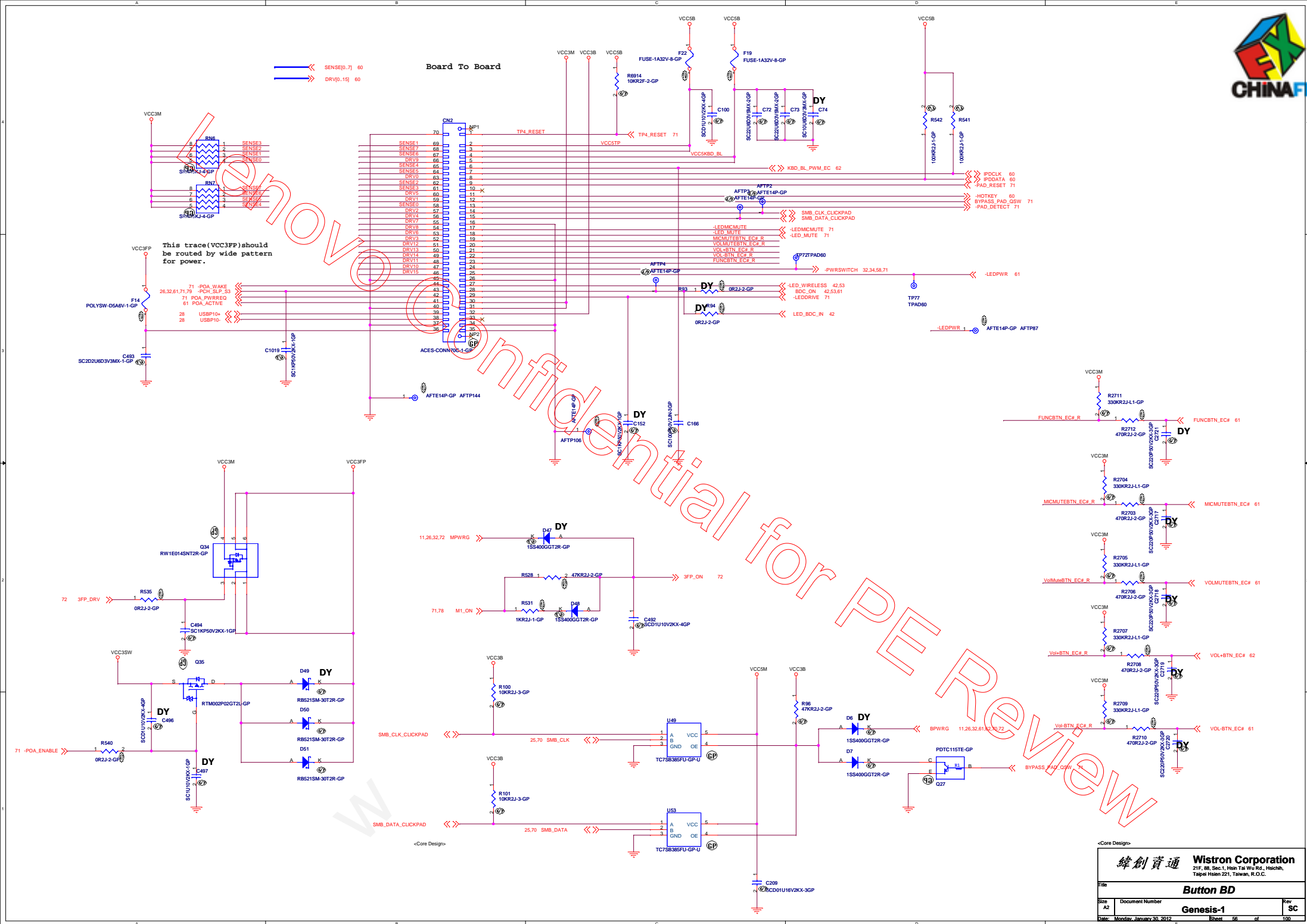
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Media Card Slot

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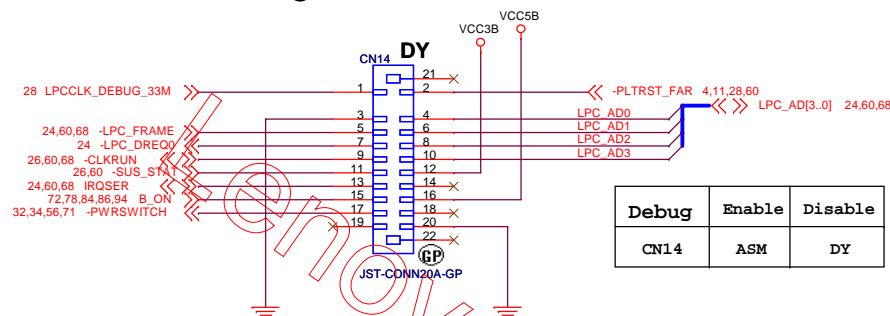
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Debug card connector

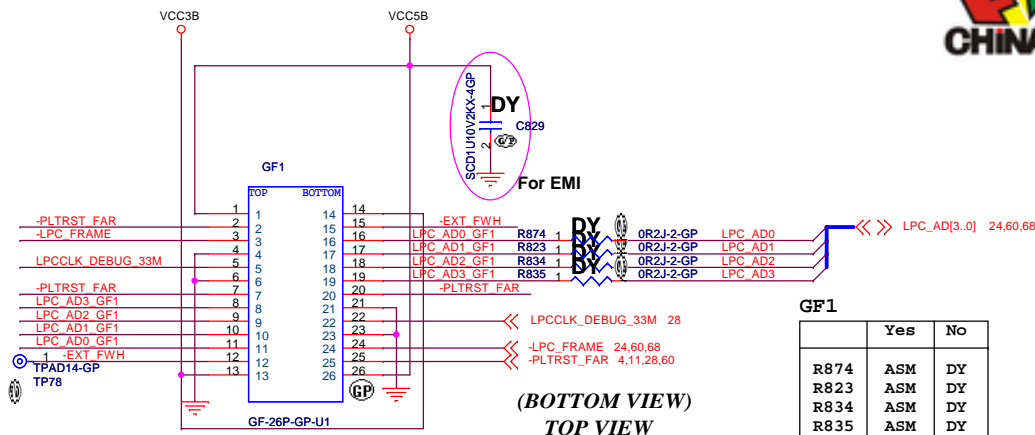


Put "easy-to-access" place

4M

SO8	4M	Marconix	MX25L3206EM2I-12G	72.25320.C01
		Winbond	W25Q032BVSSIG	72.25Q32.A01
	8M	Eon	EN25QH32-104HIP	72.02532.B01
		Numonyx	N25Q032A13ESEC0	72.25Q32.C01
SO8	8M	Marconix	MX25L6406EM2I-12G	72.25640.D01
		Winbond	W25Q064CVSSIG	72.25Q64.B01
	16M	Eon	EN25QH64-104HIP	72.02564.001
		Numonyx	N25Q064A13ESEC0	72.25Q64.G01
WS08	16M	Marconix	MX25L12836EZNI-10G	wait for P/N
		Winbond	W25Q128BVEIG	72.25128.I01
	32M	Marconix	MX25L12835EZNI-10G	wait for P/N
		Numonyx	N25Q128A13EF8C0	

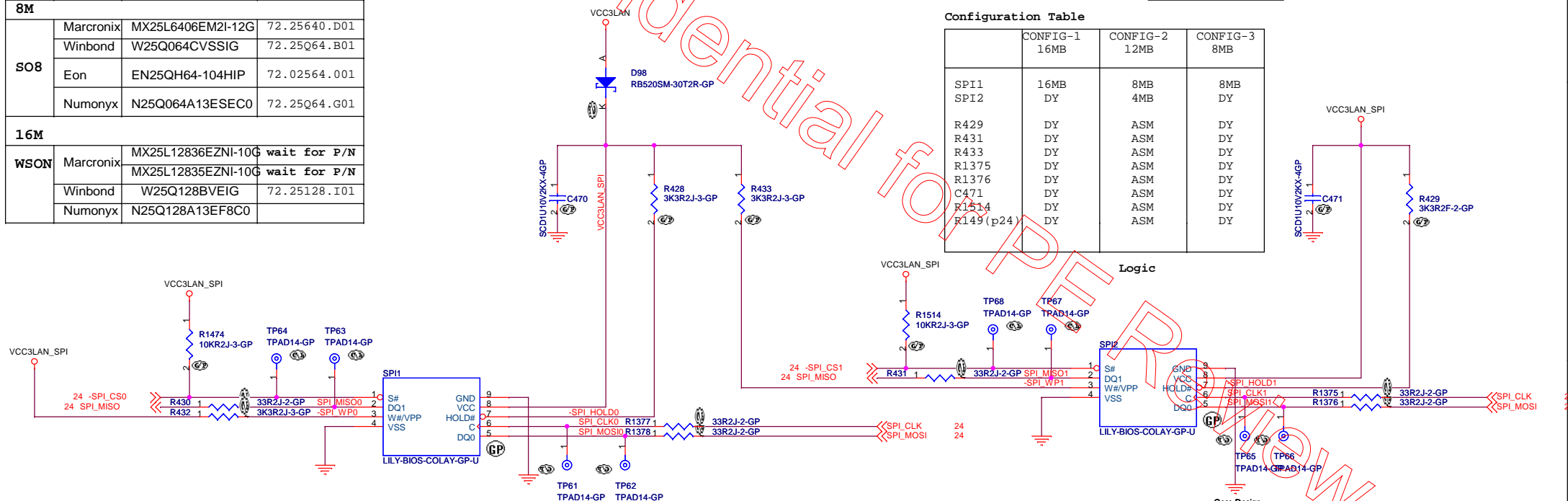
Golden Finger for Debug Board



Configuration Table

	CONFIG-1 16MB	CONFIG-2 12MB	CONFIG-3 8MB
SPI1	16MB	8MB	8MB
SPI2	DY	4MB	DY
R429	DY	ASM	DY
R431	DY	ASM	DY
R433	DY	ASM	DY
R1375	DY	ASM	DY
R1376	DY	ASM	DY
C471	DY	ASM	DY
R1514	DY	ASM	DY
R149 (p24)	DY	ASM	DY

Logic



SO8 and WSON8 are both supported!

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Title			
SPI&LPC debug card			
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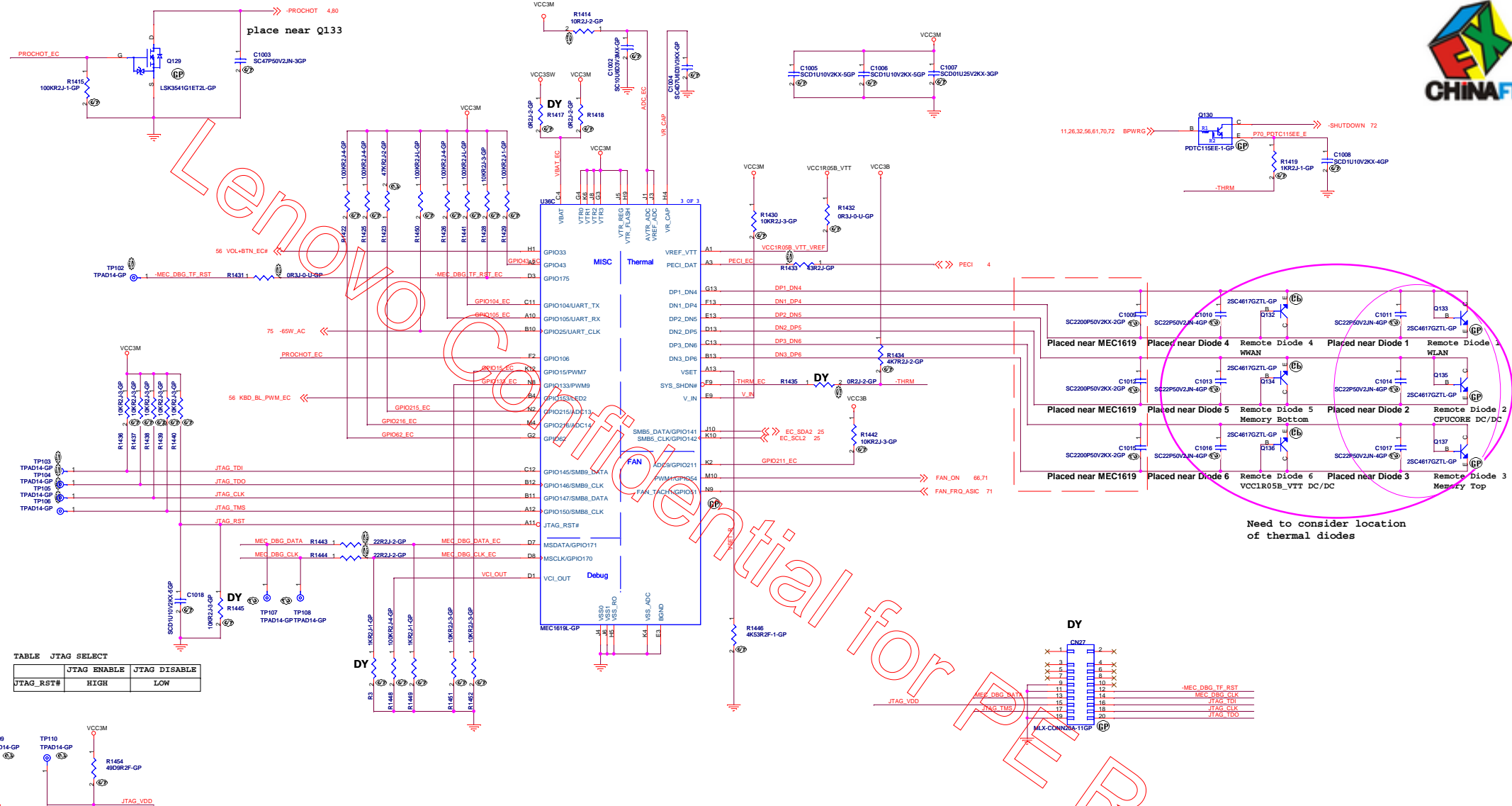


TABLE JTAG SELECT

JTAG_RST#	JTAG ENABLE	JTAG DISABLE
HIGH	Enable	Disable
LOW	Disable	Enable

JTAG debug port

	Enable	Disable
R1440	ASM	DY
R1445	DY	ASM
R1454	ASM	DY

↑
LOGIC

trace FIFO debug port

	Enable	Disable
R1443	ASM	DY
R1444	ASM	DY
R3	DY	ASM

↑

Need to consider location of thermal diodes

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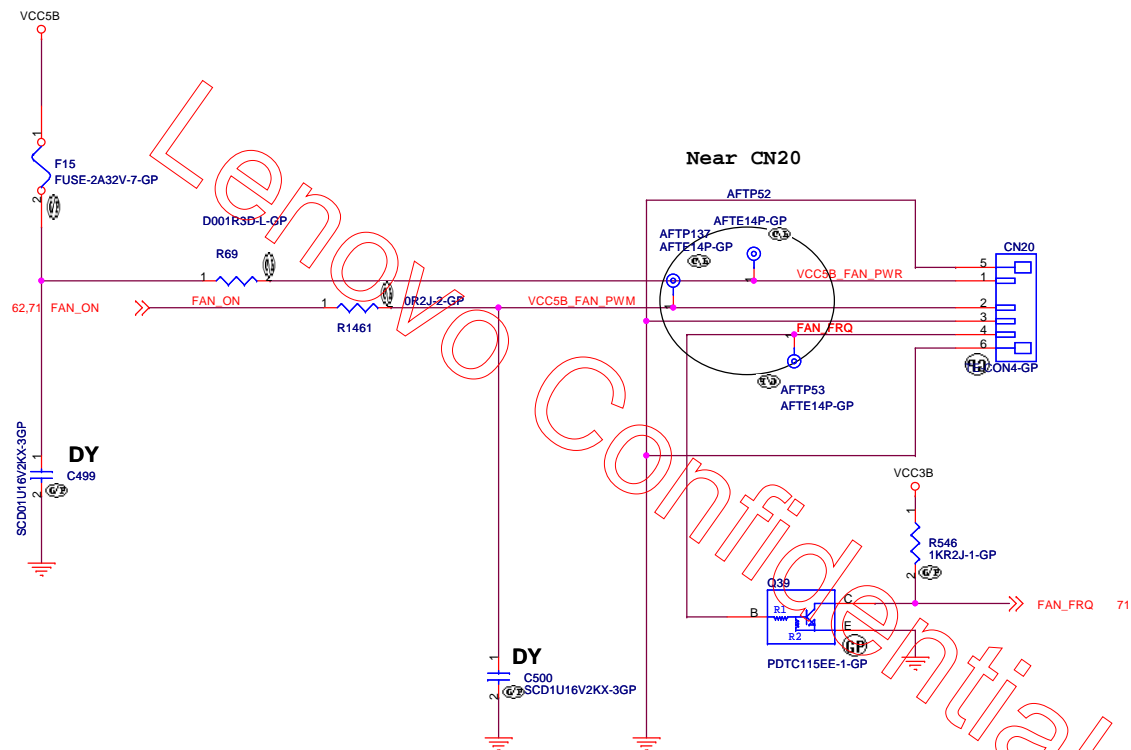
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File

FAN Control

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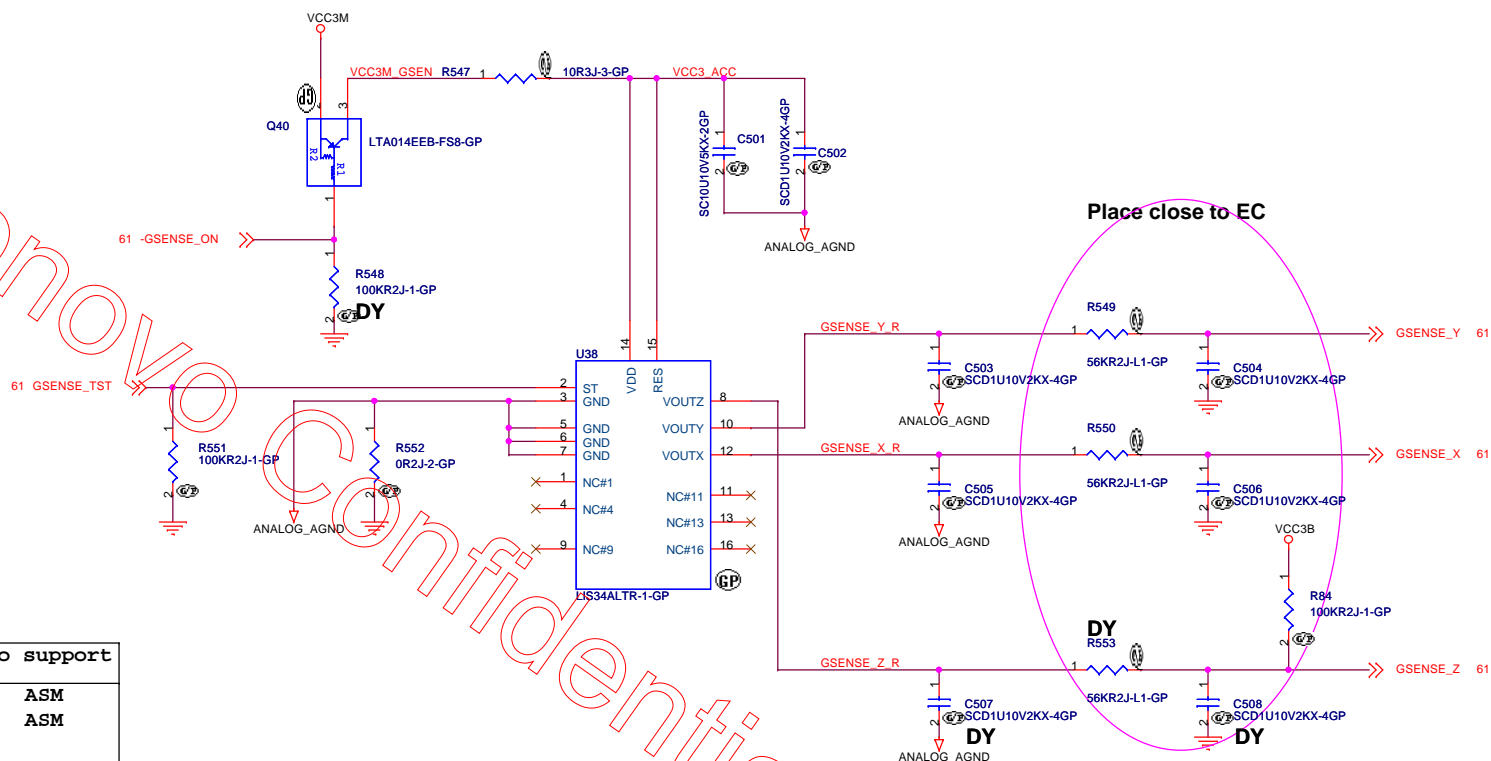
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G-sensor	support	no support
R548	DY	ASM
R551	ASM	ASM
U38	ASM	DY
Q40	ASM	DY
R547	ASM	DY
C501	ASM	DY
C502	ASM	DY
R552	ASM	DY
C503	ASM	DY
R549	ASM	DY
C504	ASM	DY
C505	ASM	DY
R550	ASM	DY
C506	ASM	DY
C507	DY	DY
R553	DY	DY
C508	DY	DY
R84	ASM	ASM

U38

Primary	STMicro LIS34AL	41R0828AA
Second	Kionix KXTC8-2850	74.KXTC8.0BZ
Third		

Layout Comment :

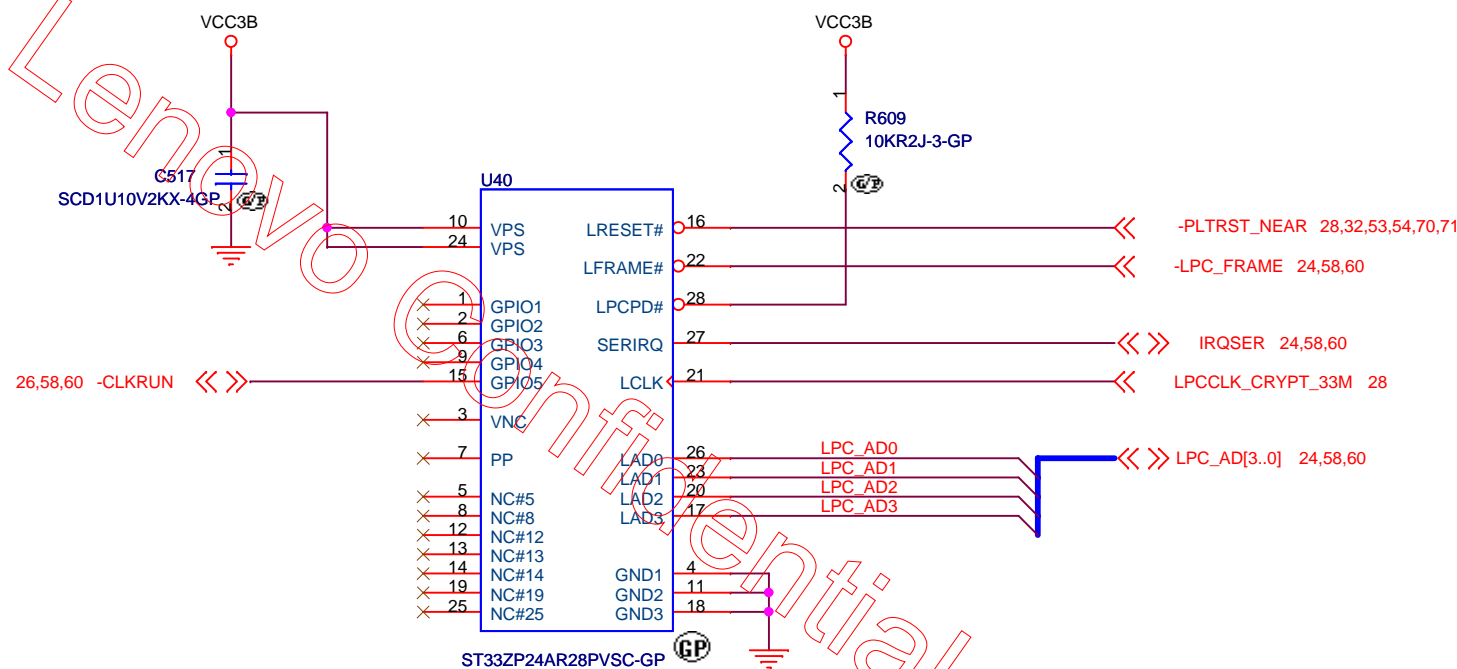
(1) Avoid routing under DCDC switching area.

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Title			G-SENSOR	
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	TPM P/N	Firmware
SDV / FVT	ST33ZP24AR28PVRC	1.2.C.0
SIT	ST33ZP24AR28PVSC	1.2.D.0

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Title

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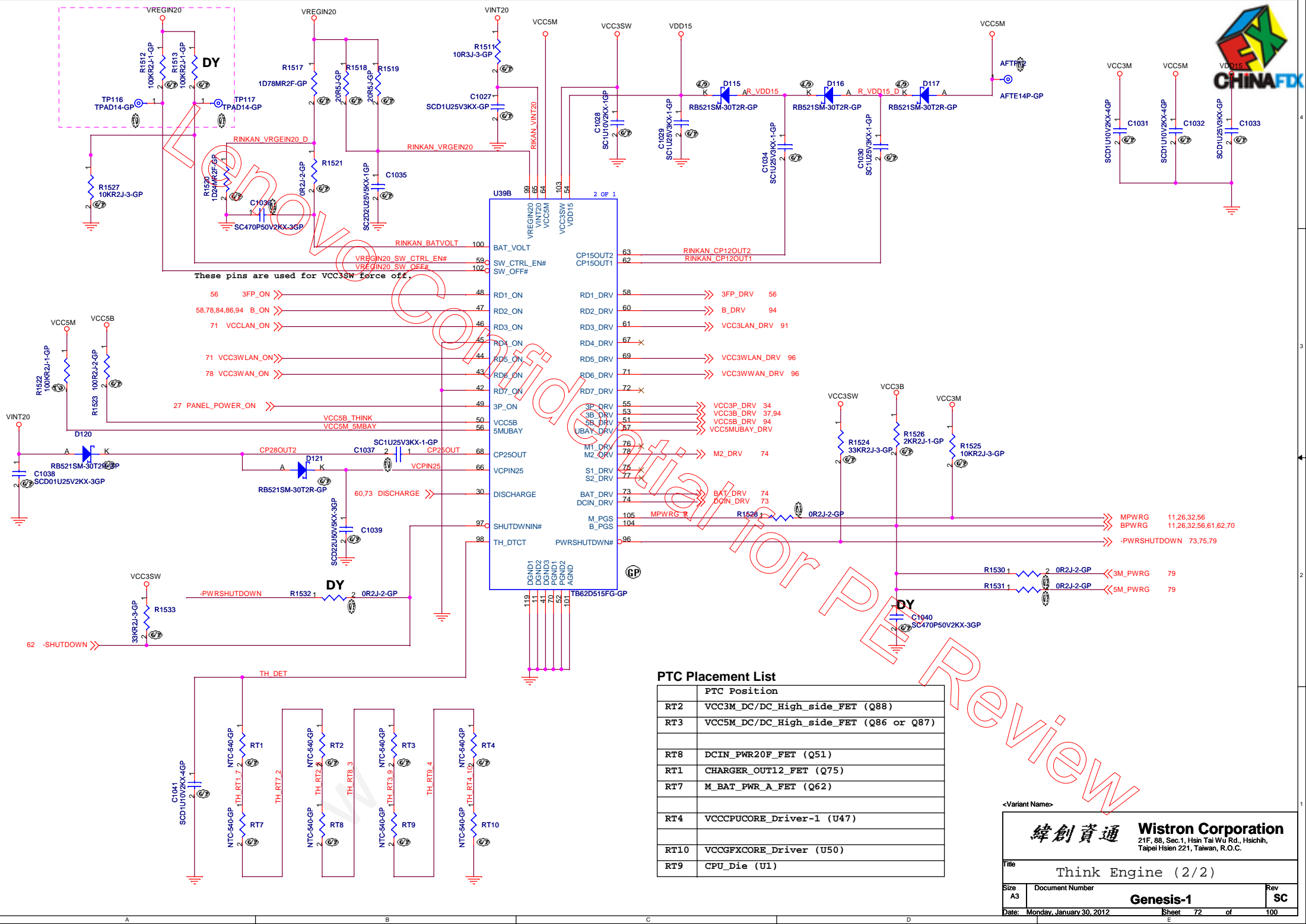
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LOGIC



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EPPROM/SMBUS SW			
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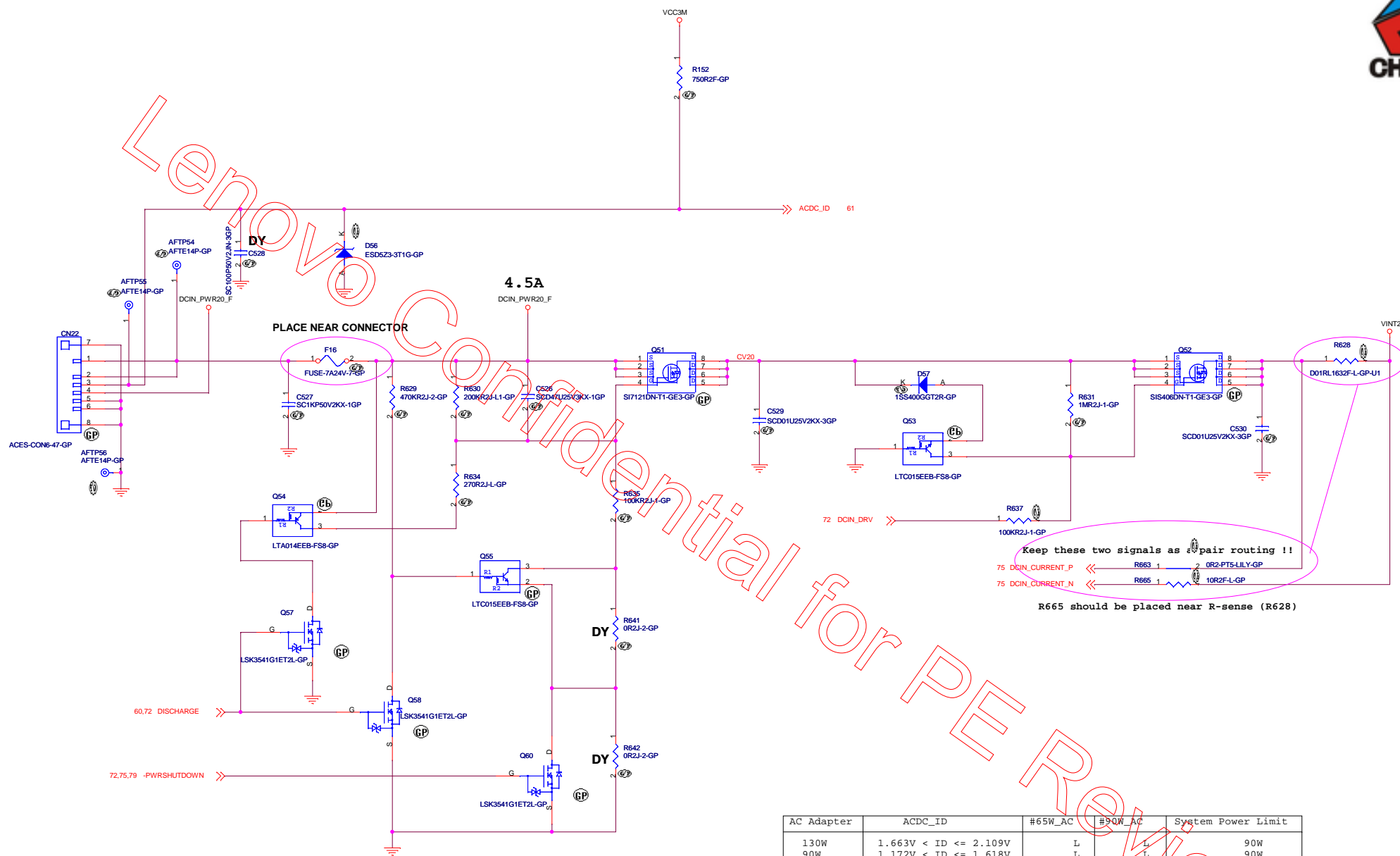
These pins are used for VCC3SW force off.

PTC Placement List

	PTC Position
RT2	VCC3M_DC/DC_High_side_FET (Q88)
RT3	VCC5M_DC/DC_High_side_FET (Q86 or Q87)
RT8	DCIN_PWR20F_FET (Q51)
RT1	CHARGER_OUT12_FET (Q75)
RT7	M_BAT_PWR_A_FET (Q62)
RT4	VCCCPUCORE_Driver-1 (U47)
RT10	VCCGFXCORE_Driver (U50)
RT9	CPU_Die (U1)

<Variant Name>

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Keep these two signals as a pair routing !!

75 DCIN_CURRENT_P << R663 1 2 OR2-PT5-LILY-GP

75 DCIN_CURRENT_N << R665 1 2 10R2F-L-GP

R665 should be placed near R-sense (R628)

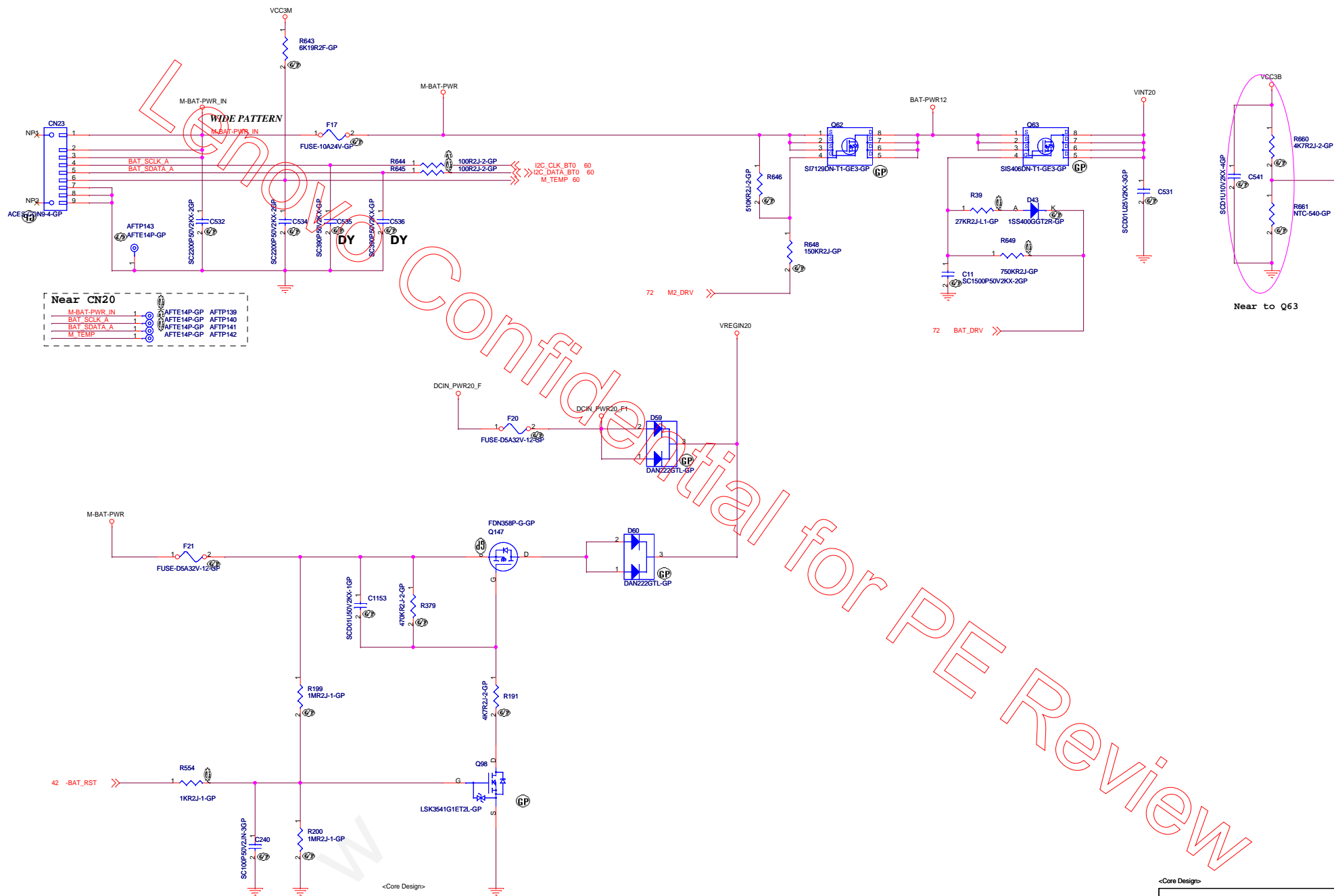
AC Adapter	ACDC_ID	#65W_AC	#90W_AC	System Power Limit
130W	1.663V < ID <= 2.109V	L	L	90W
90W	1.172V < ID <= 1.618V	L	L	90W
65W	0.693V < ID <= 1.134V	L	H	65W
45W	0.234V < ID <= 0.663V	H	H	45W

PEAK SHIFT	YES	NO
R629	ASM	NO-ASM
Q58	ASM	NO-ASM
Q55	ASM	NO-ASM

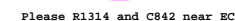
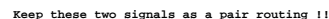
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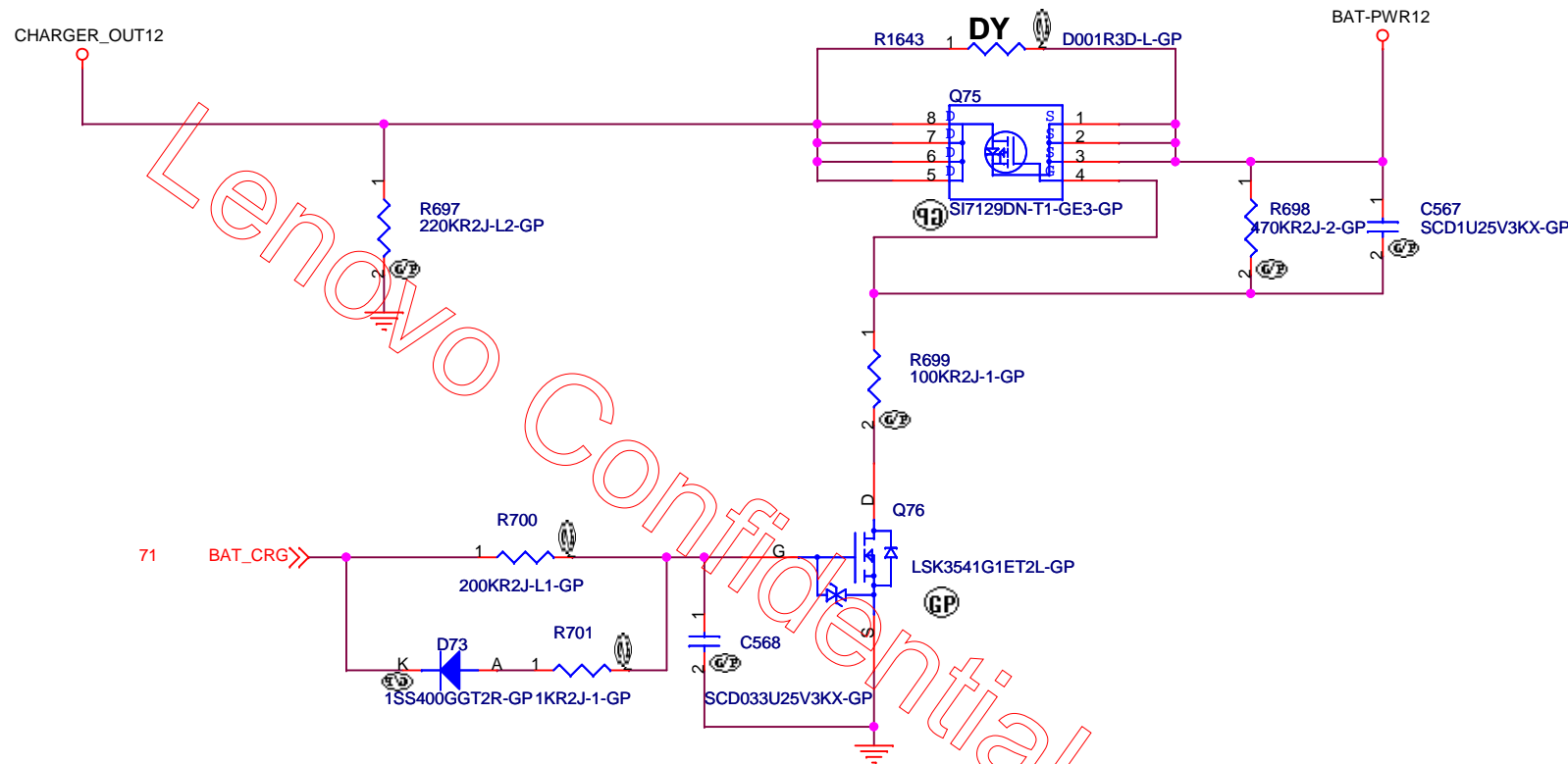
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Title

CHARGER SELECT

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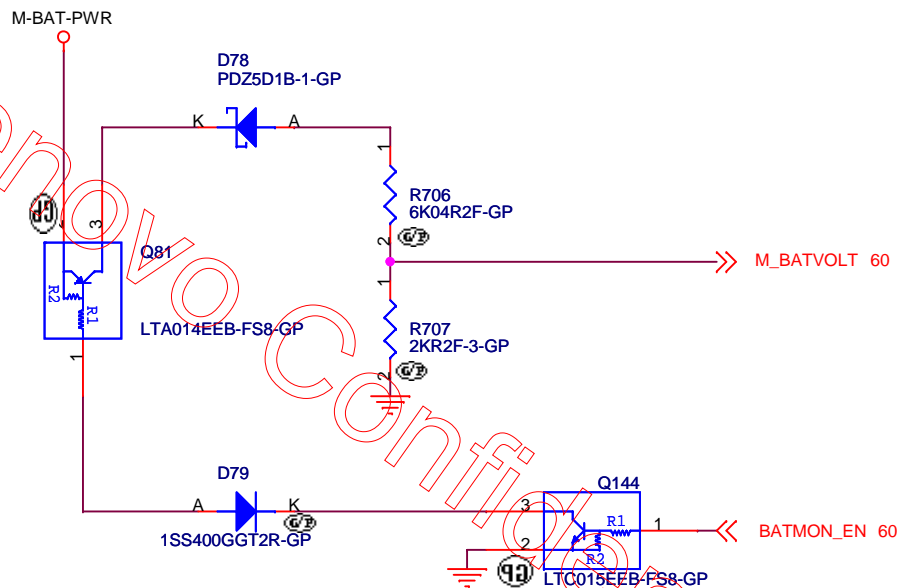
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$$V_{OUT} = 0.249 (V_{BAT} - 5)$$



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Title

BATTERY MONITOR

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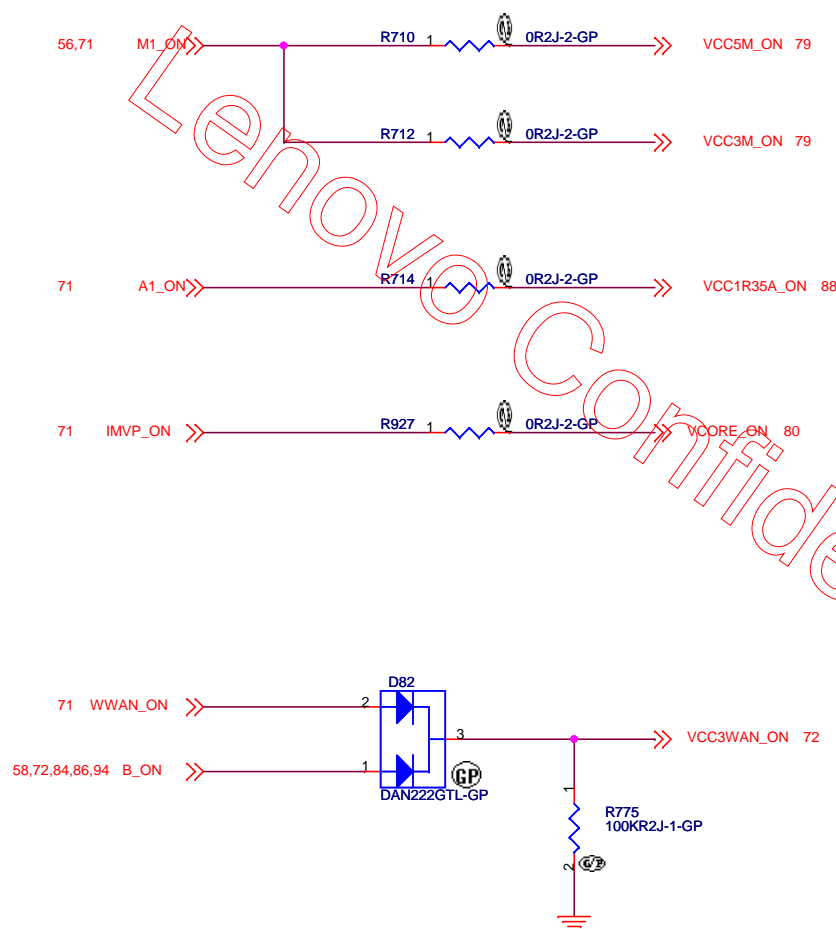
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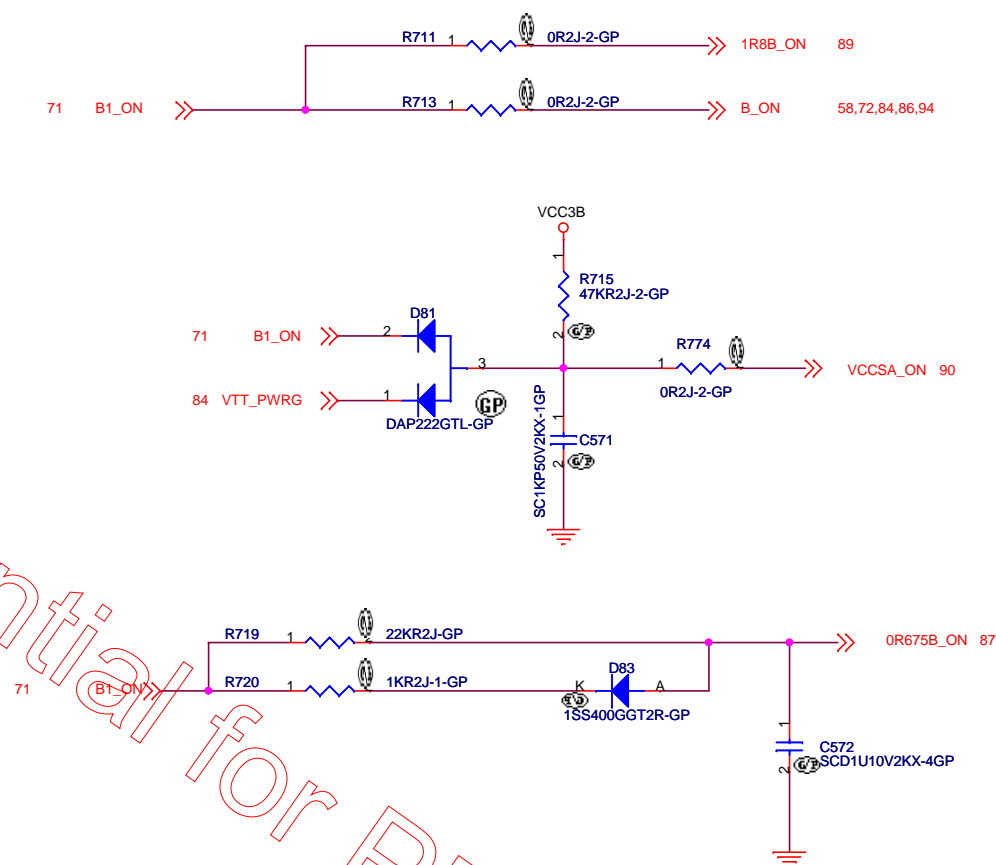
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AOAC	YES	NO
D82	ASM	DY
R775	ASM	ASM
	100Kohm	0ohm

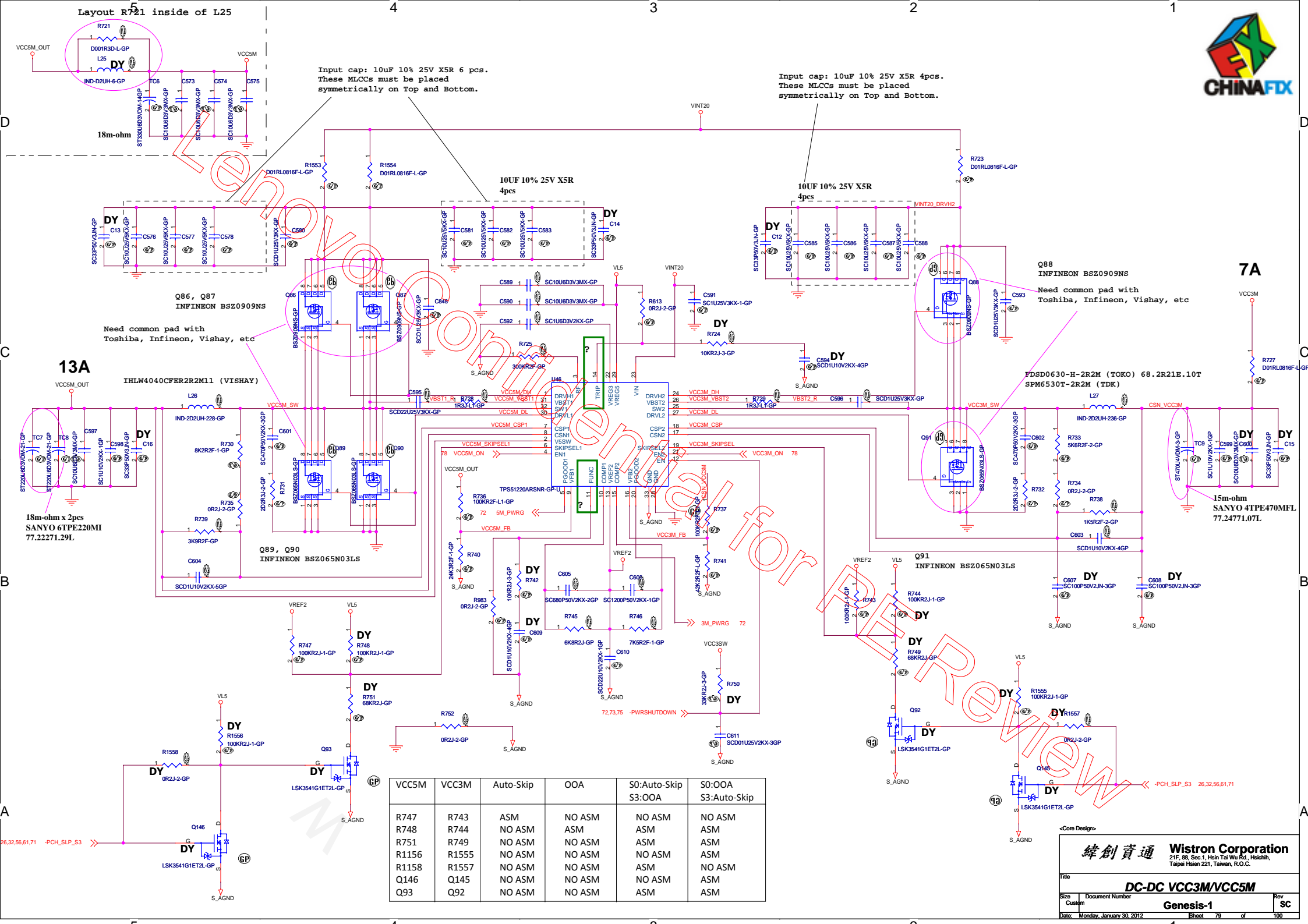
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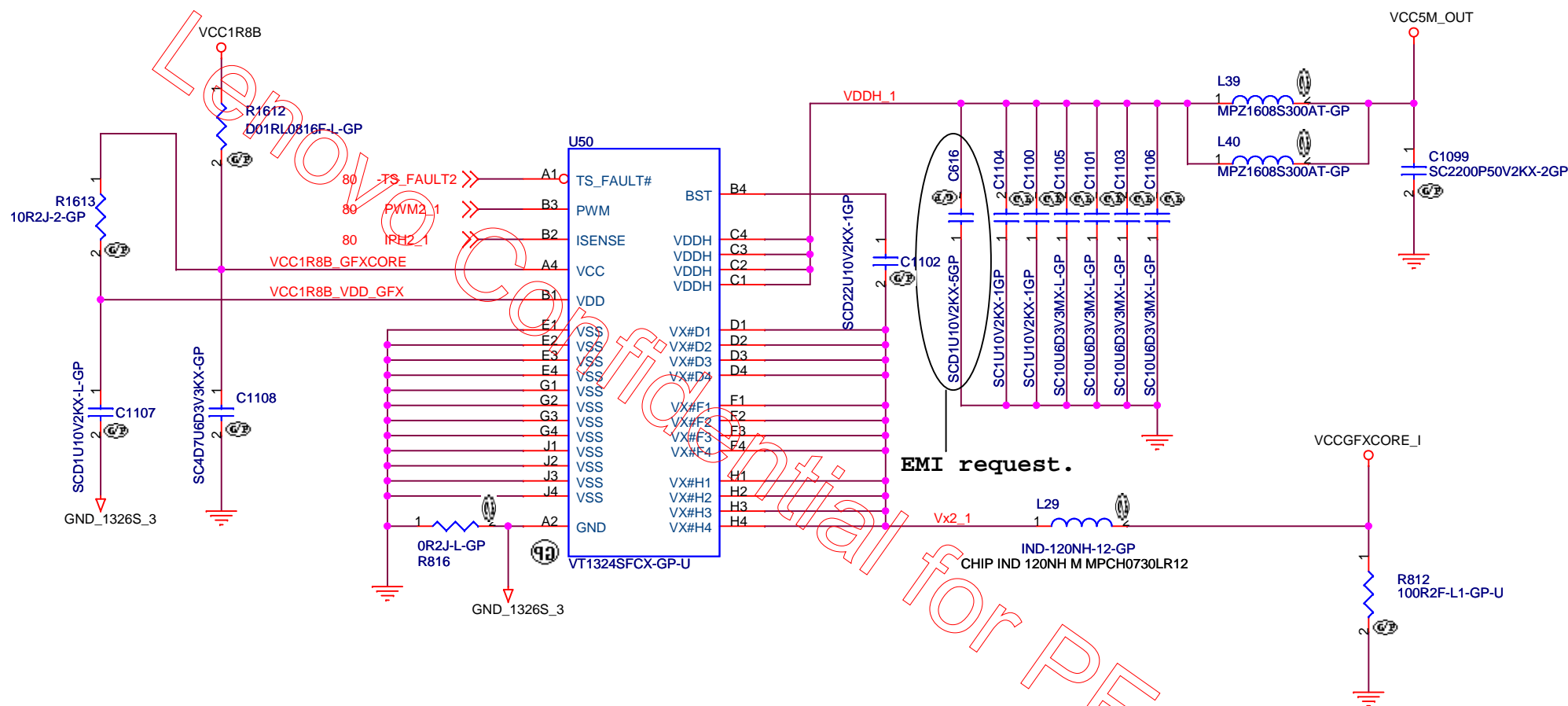
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POWER SEQUENCE			
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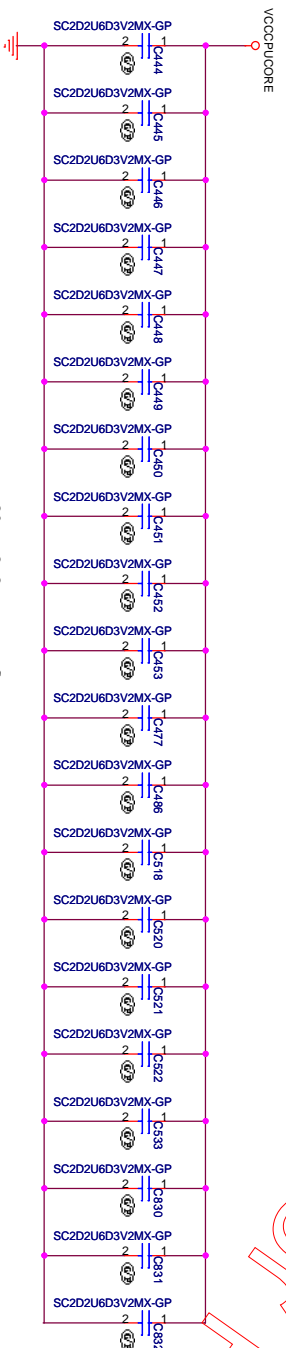
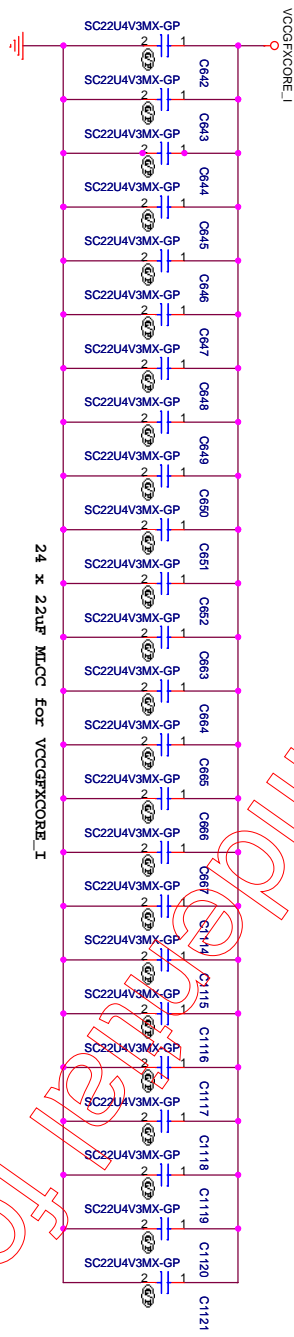
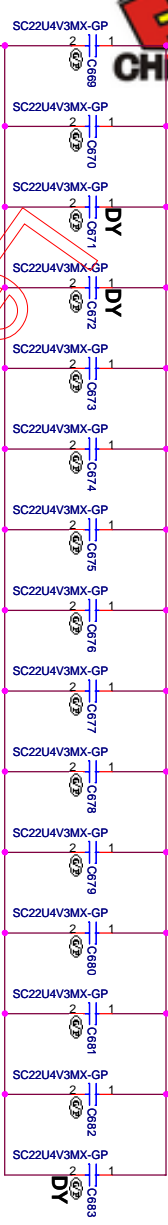
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Title
VCCGFXCORE

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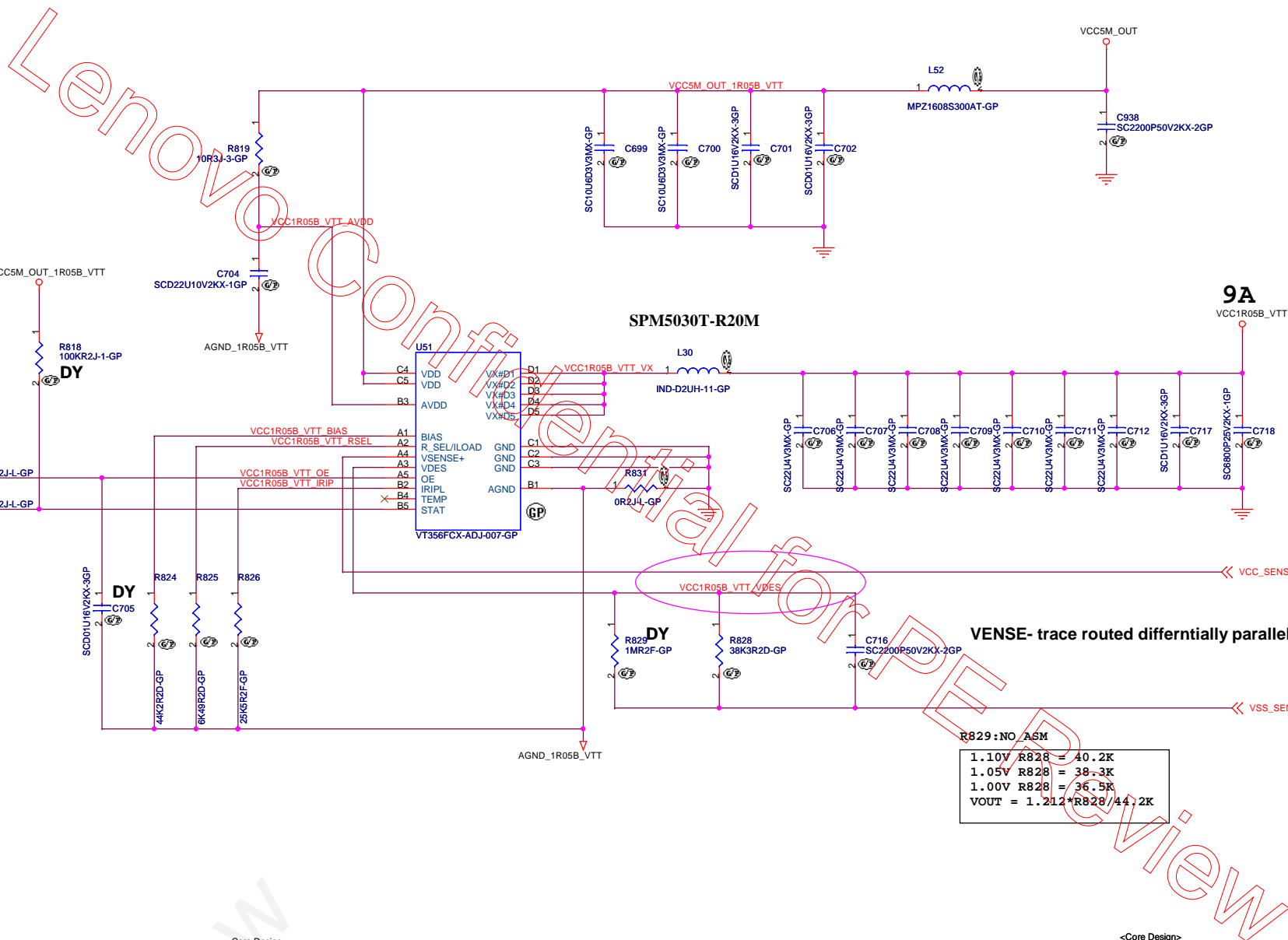
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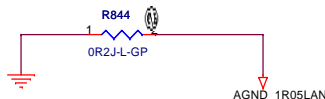
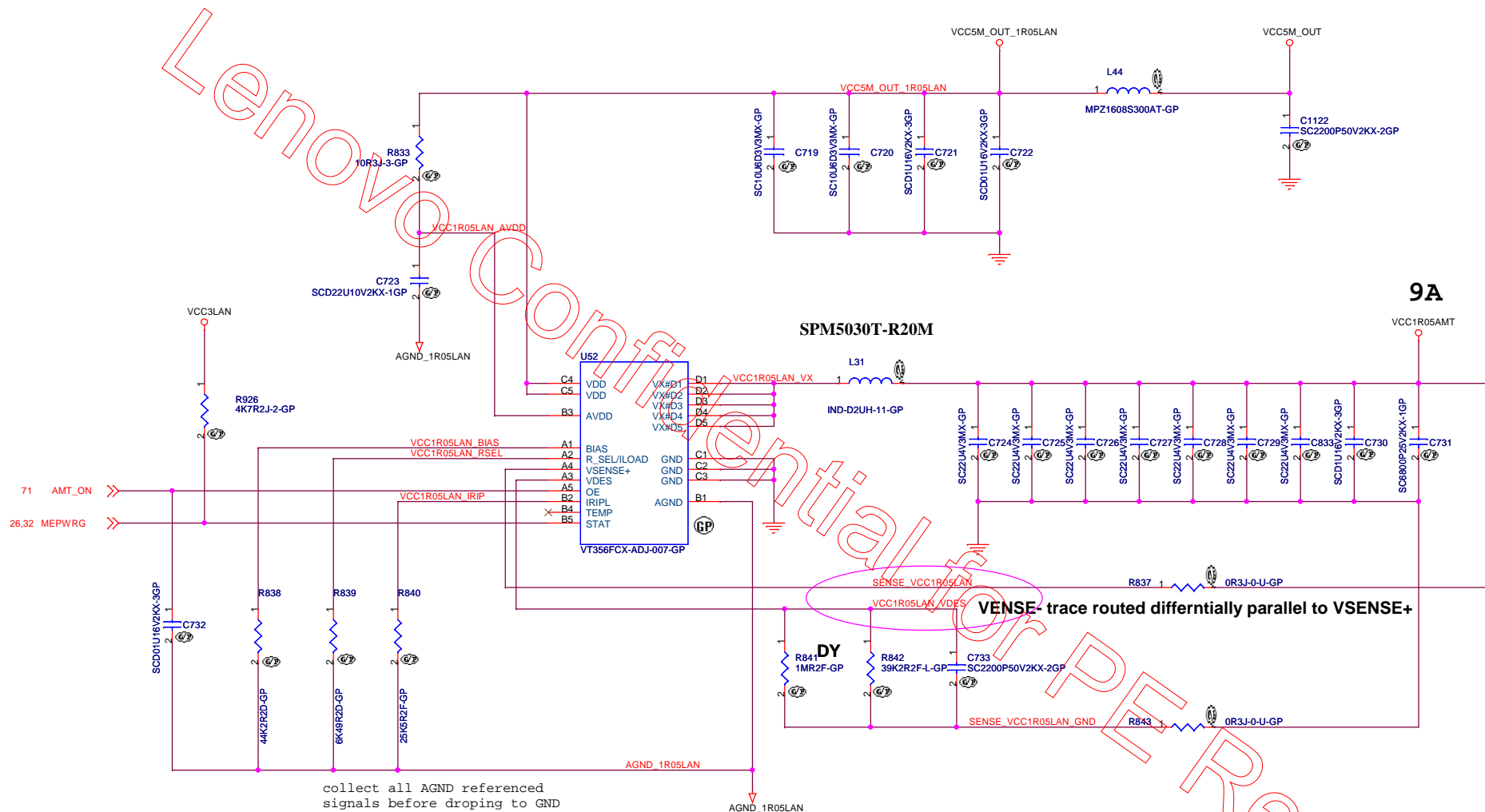
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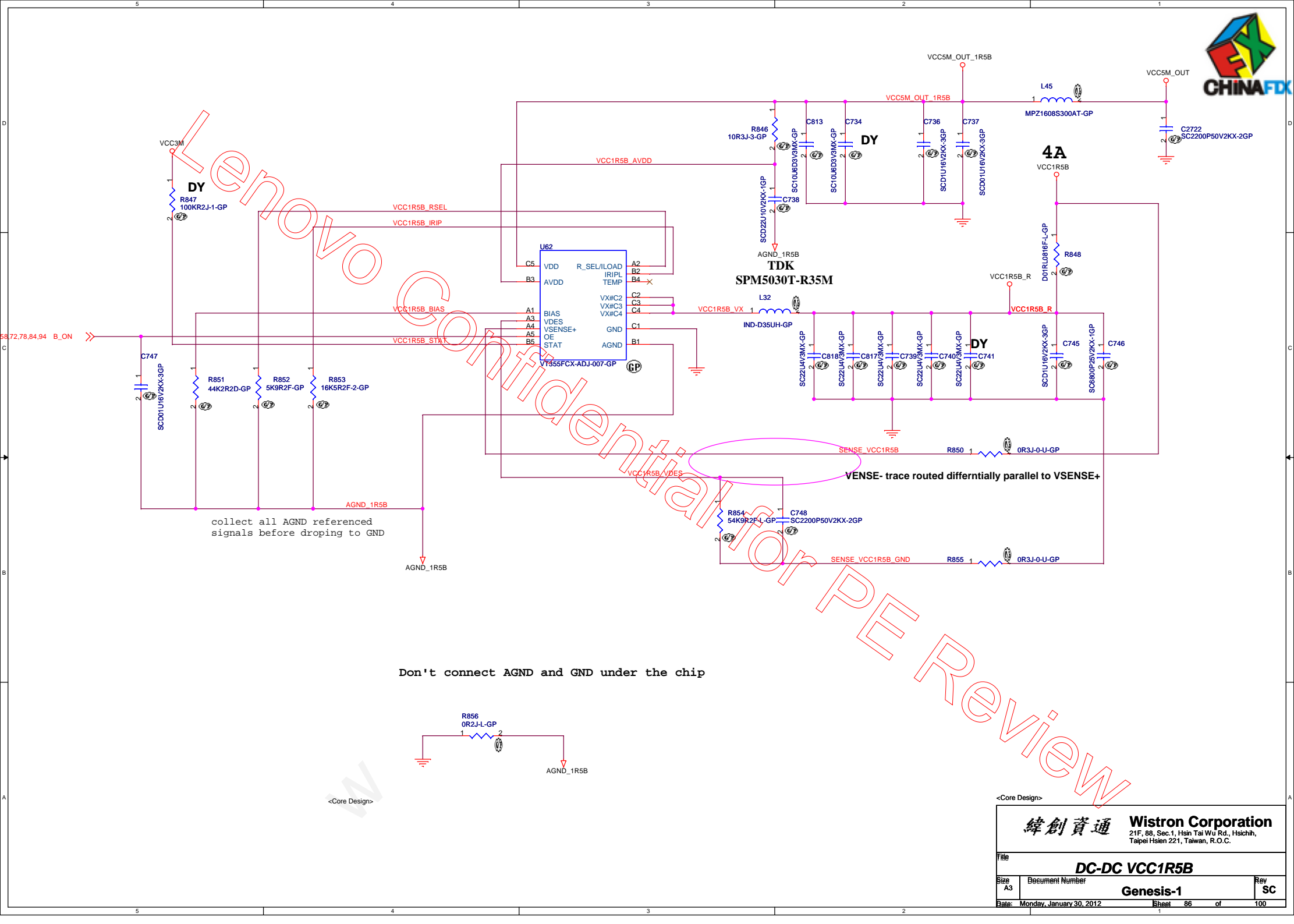
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collect all AGND referenced signals before dropping to GND

Don't connect AGND and GND under the chip

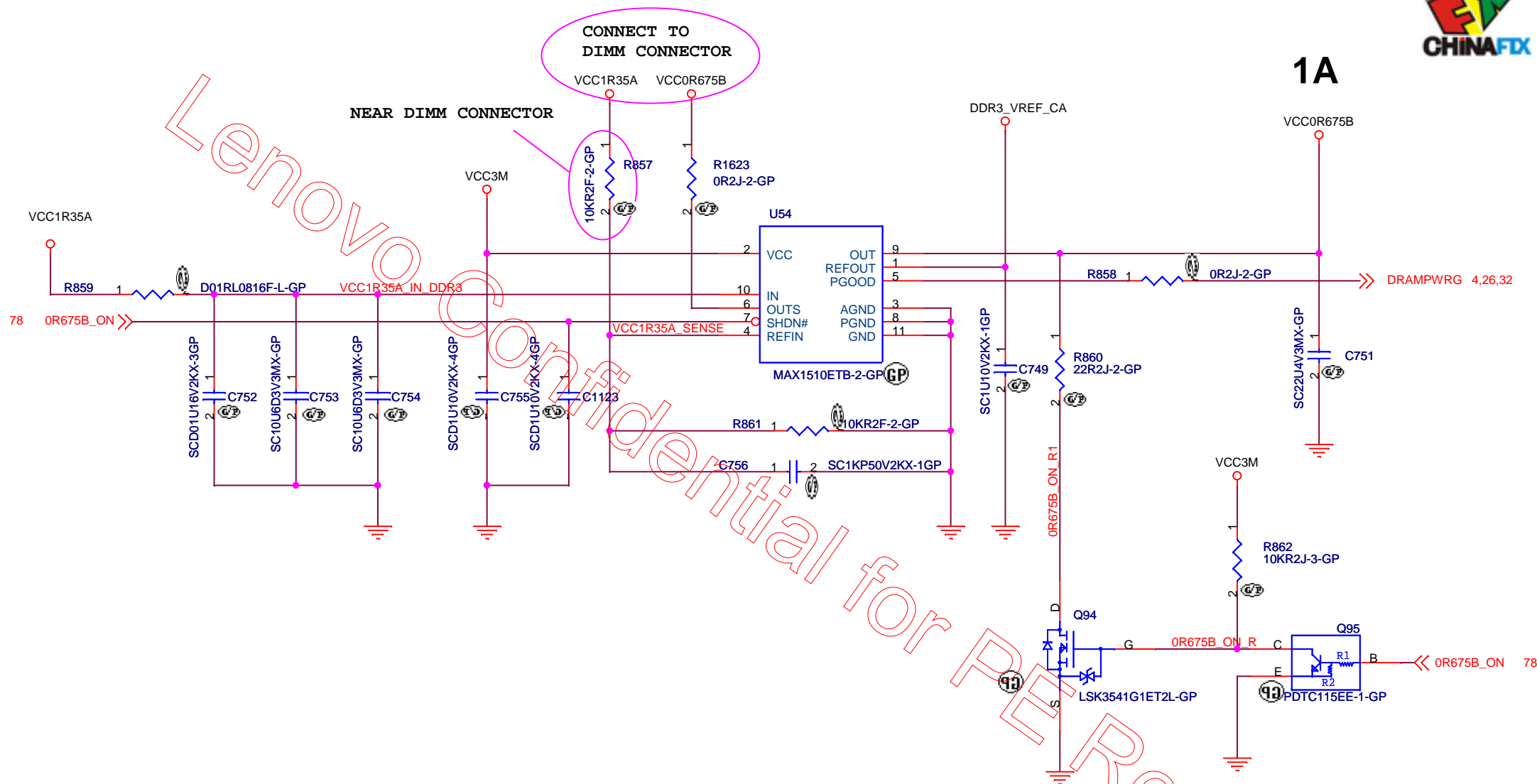
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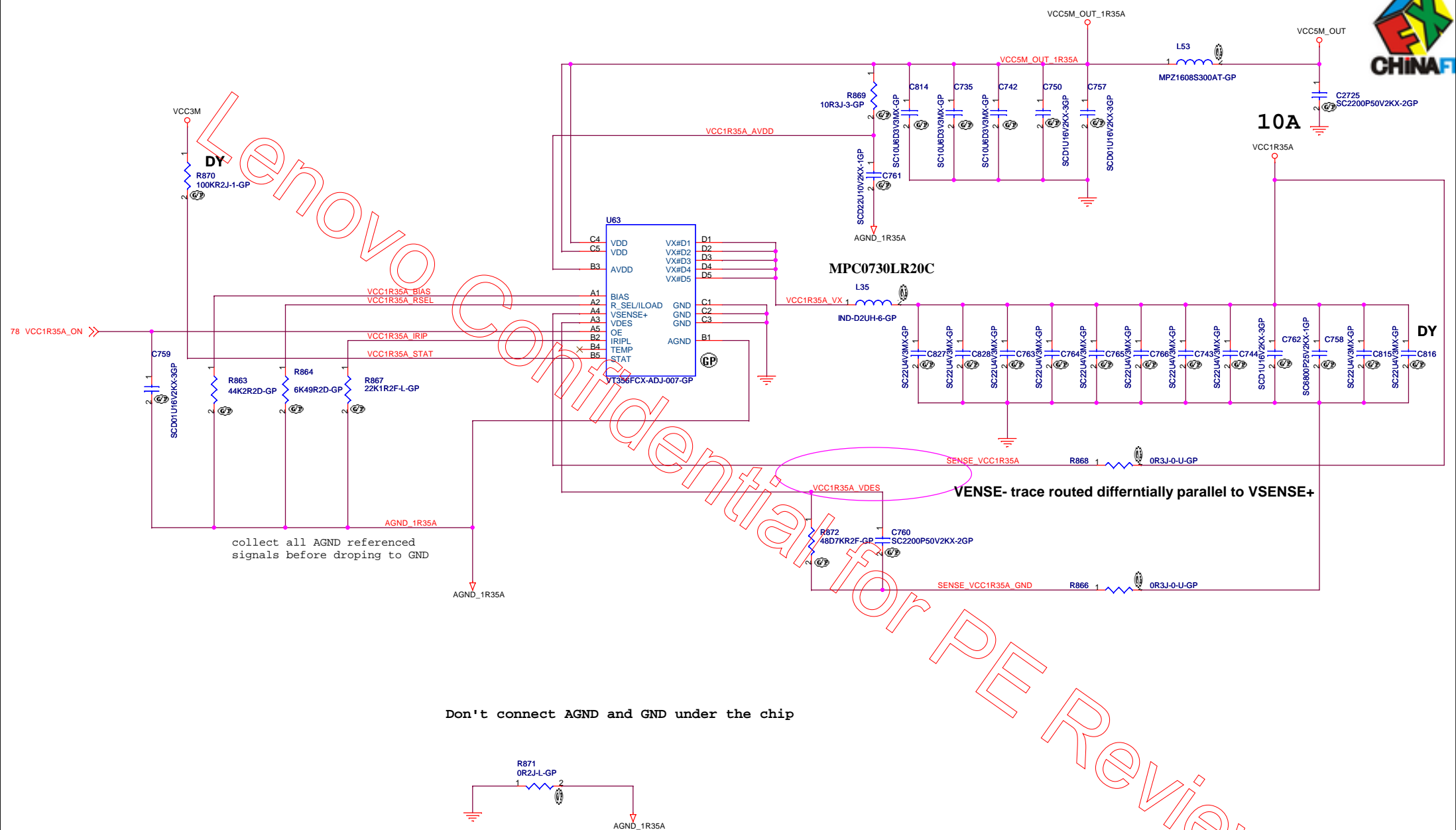
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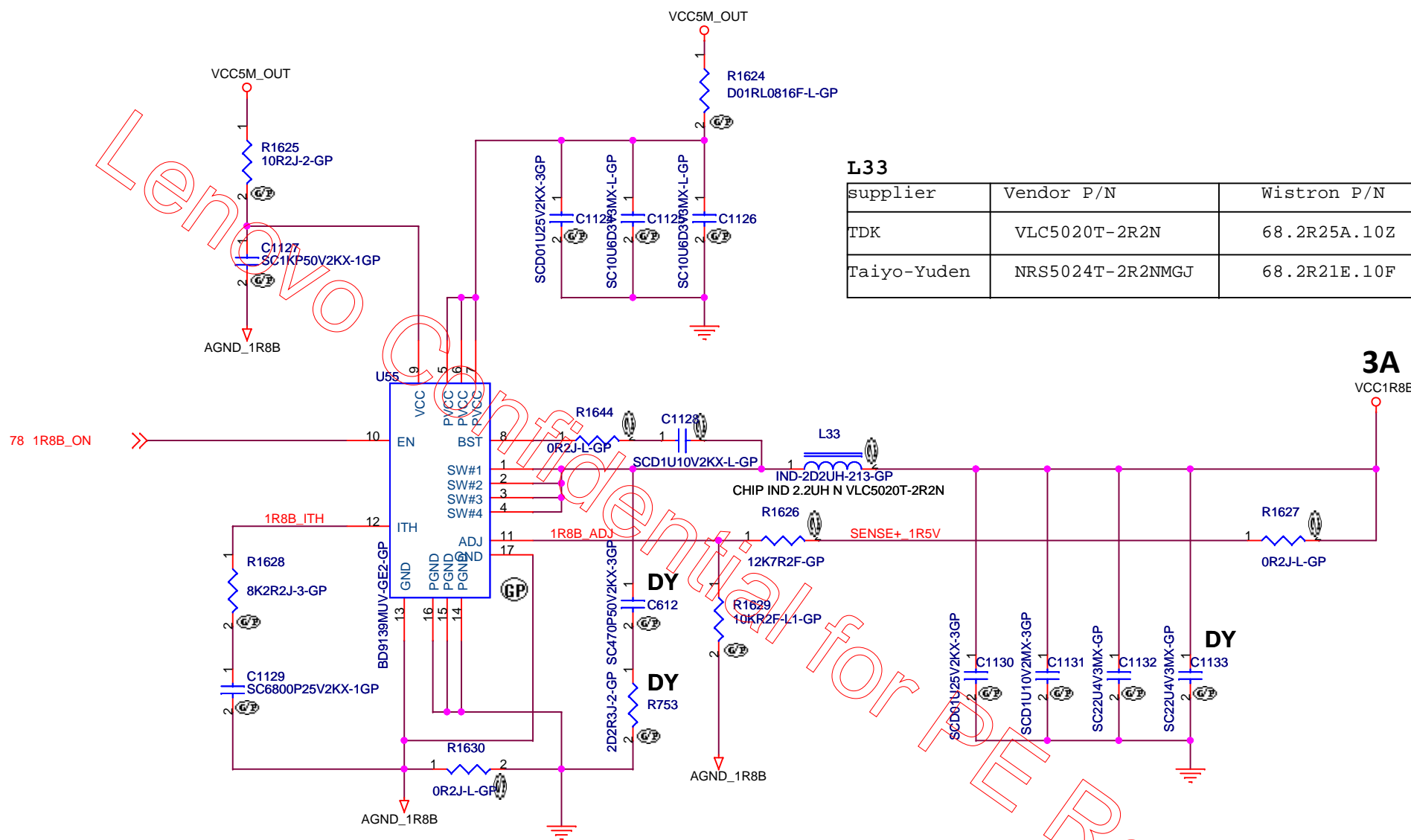
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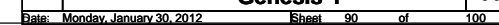
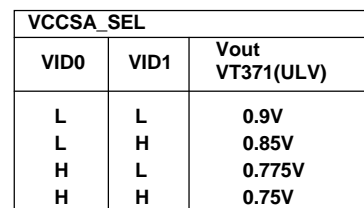
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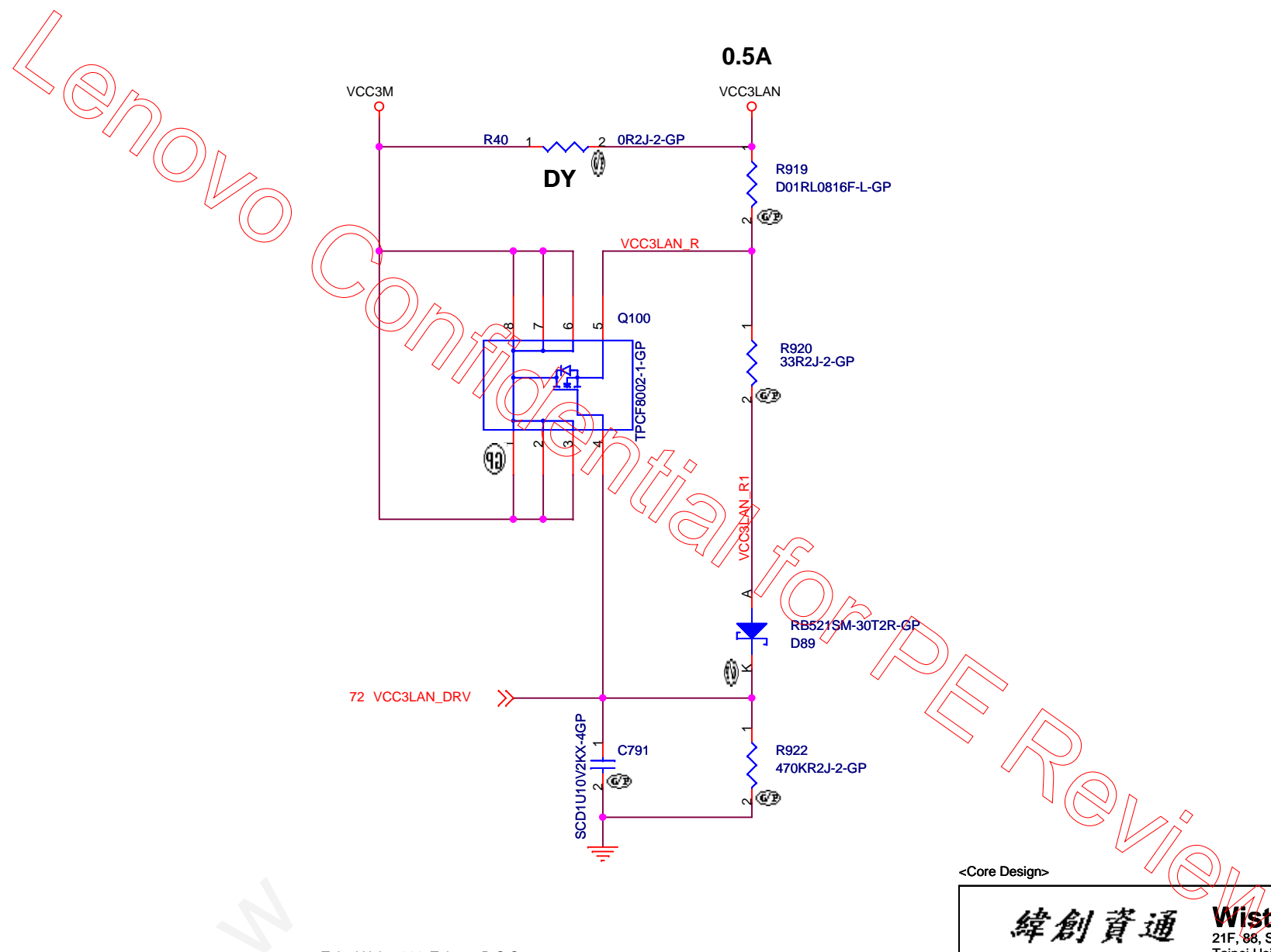
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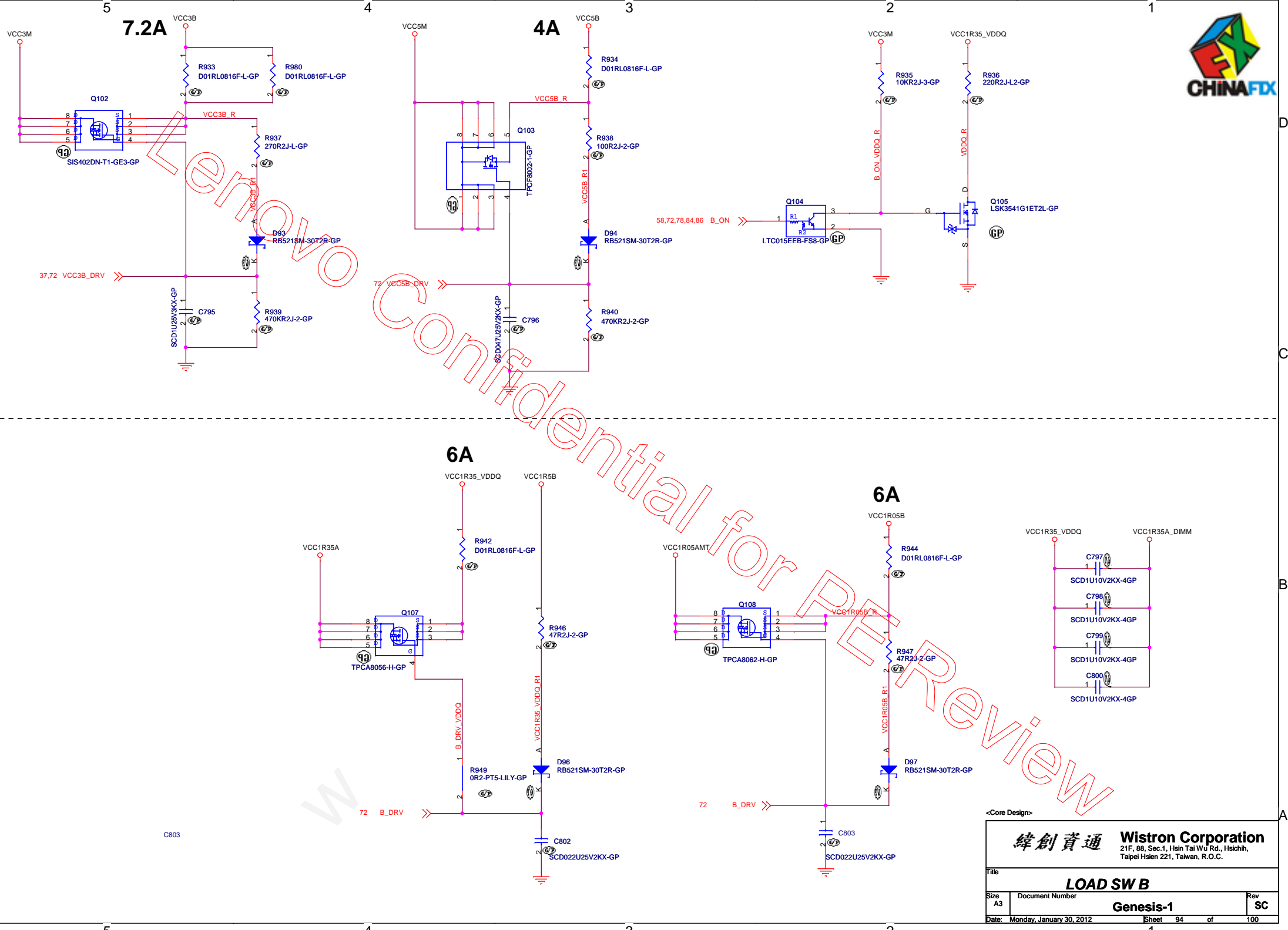
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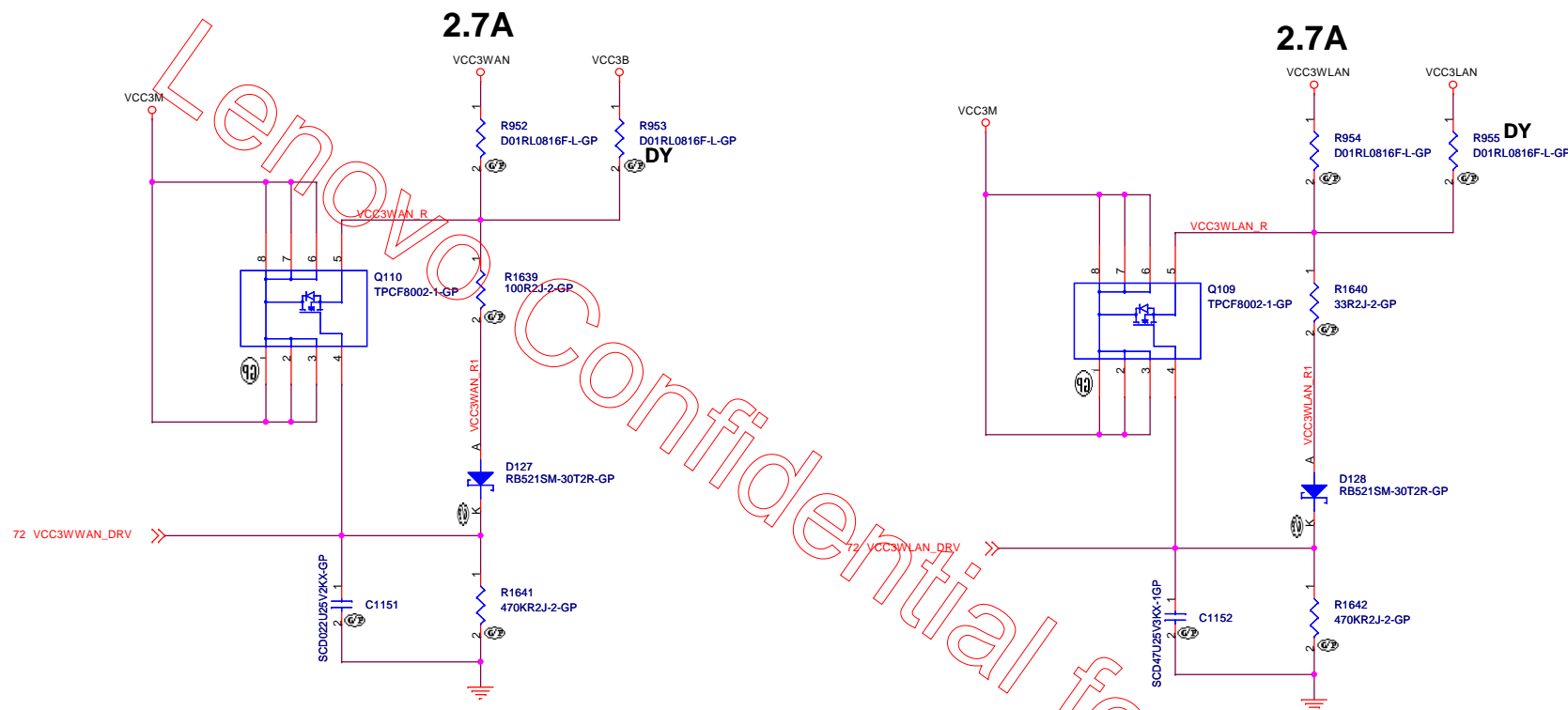
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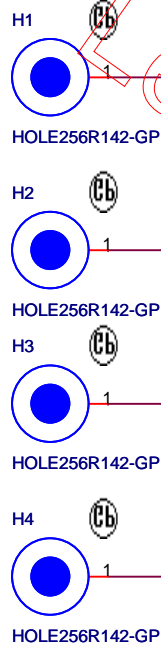
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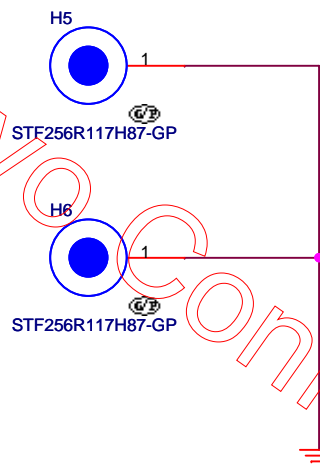
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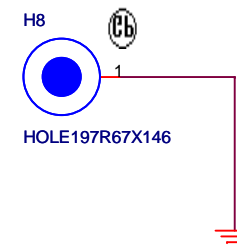
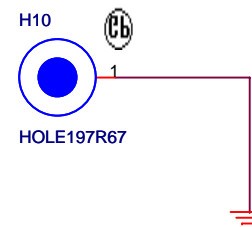
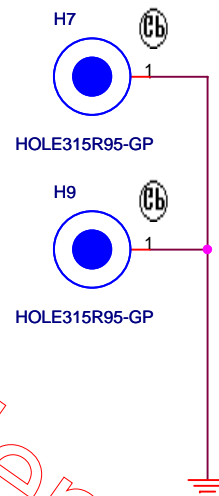
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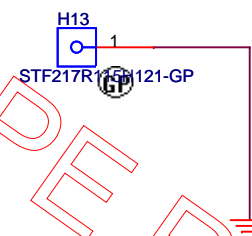
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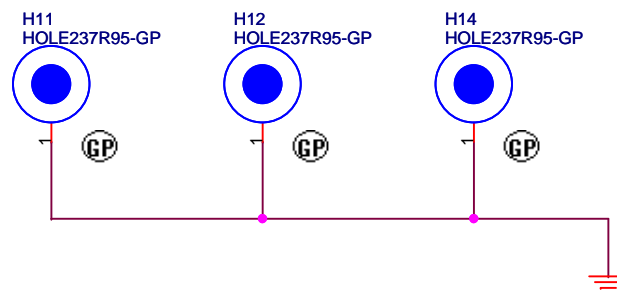
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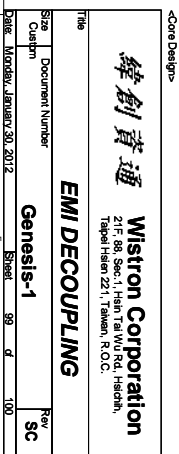
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Long power trace EMI decoupling caps





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