Compal Confidential

QIWY3 M/B Schematics Document

Intel IVY Bridge Processor with DDRIII + Panther Point PCH
nVIDIA N13X

2011-12-23

REV:1.0

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Title: Cover Page		
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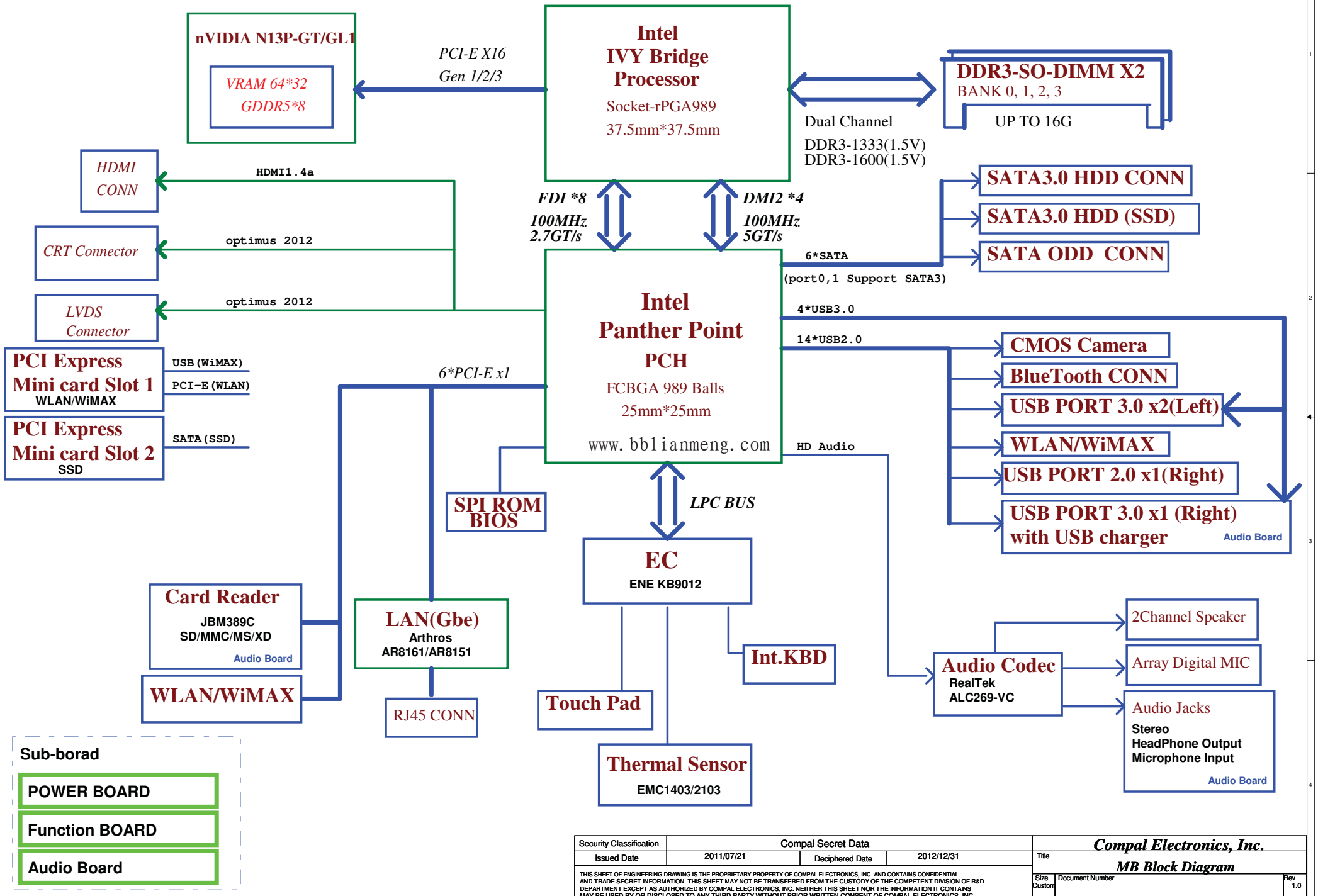
File Name : Y480

Chief River



Sub-borad

- POWER BOARD
- Function BOARD
- Audio Board

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Title	MB Block Diagram		
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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%					
Ra/Rc/Re	10K +/- 5%					
Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Project	
0	0	0 V	0 V	0 V	QIWY3	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	QIWY3	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	QIWY3	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	QIWY3	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	QIWY4	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	QIWY4	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	QIWY4	PVT
7	NC	2.500 V	3.300 V	3.300 V	QIWY4	MP

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
EHCI1	XHCI 1	0	USB Port (Right Side)
	XHCI 2	1	
	XHCI 3	2	USB Port (Left Side)
	XHCI 4	3	USB Port (Left Side)
		4	
		5	Camera
		6	
		7	
EHCI2		8	
		9	USB Port (Right Side)
		10	Mini Card(WLAN)
		11	
		12	Mini Card(TV)
		13	Blue Tooth

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	TV
4	Card Reader
5	
6	
7	
8	

BOM Structure Table

BOM Structure	BTO Item
OPTI@	OPTIMUS part
HDMI@	HDMI part
TV@	TV module part
CHG@	USB charger part
NOCHG@	No USB charger part
BT@	Blue Tooth part
CMOS@	CMOS Camera part
8161@	AR8161 LAN part
8151@	AR8151 LAN part
8161S@	AR8161 LAN surge part
8151S@	AR8151 LAN surge part
SURGE@	AR8151&8161 LAN surge part
61@	X76 P/N for AR8161
51@	X76 P/N for AR8151
X76@	X76 Level part for VRAM
S1G@	X76 P/N for Samsun VRAM 1G
S2G@	X76 P/N for Samsun VRAM 2G
H1G@	X76 P/N for Hynix VRAM 1G
H2G@	X76 P/N for Hynix VRAM 2G
GL@	N13P-GL part
GT@	N13P-GT part
GE@	N13E-GE part
GTGE@	N13P-GT&N13E-GE common part
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
1403@	EMC1403 thermal part
2103@	EMC2103 thermal part
KBL@	K/B Light part
ME@	ME part
@	Unpop

SMBUS Control Table

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

ZZZ1

DA80000Q800

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Title: *Notes List*

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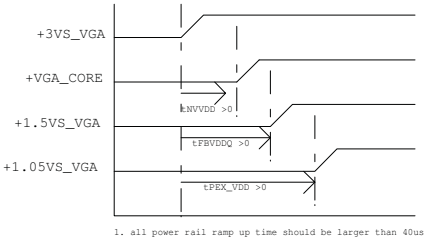
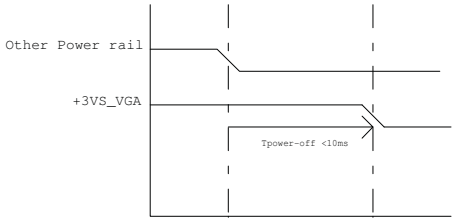
Hot plug detect for IFP link C

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GC6 event
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GT (28nm)	0x0FDB
N13E-GE (28nm)	0x0FDB
N13P-GL1 (40nm)	0x0DE9

GPU	ROM_SO	ROM_SCLK	STRAP4	STRAP3	STRAP2	STRAP1	STRAP0
N13P-GT	PU 10K	PU 5K	PD 45K	PD 5K	PD 10K	PD 35K	PU 45K
N13E-GE	PU 10K	PU 5K	PD 45K	PD 5K	PD 25K	PD 35K	PU 45K
N13P-GL	PD 10K	PD 15K	NC	NC	PU 10K	PD 45K	PU 45K

GPU		N13P-GT	N13E-GE	N13P-GL
FB Memory (GDDR5)		ROM_SI	ROM_SI	ROM_SI
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K	PD 45K	PD 45K
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K	PD 35K	PD 35K
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K	PD 30K	PD 30K
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K	PD 25K	PD 25K

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Title: VGA Notes List

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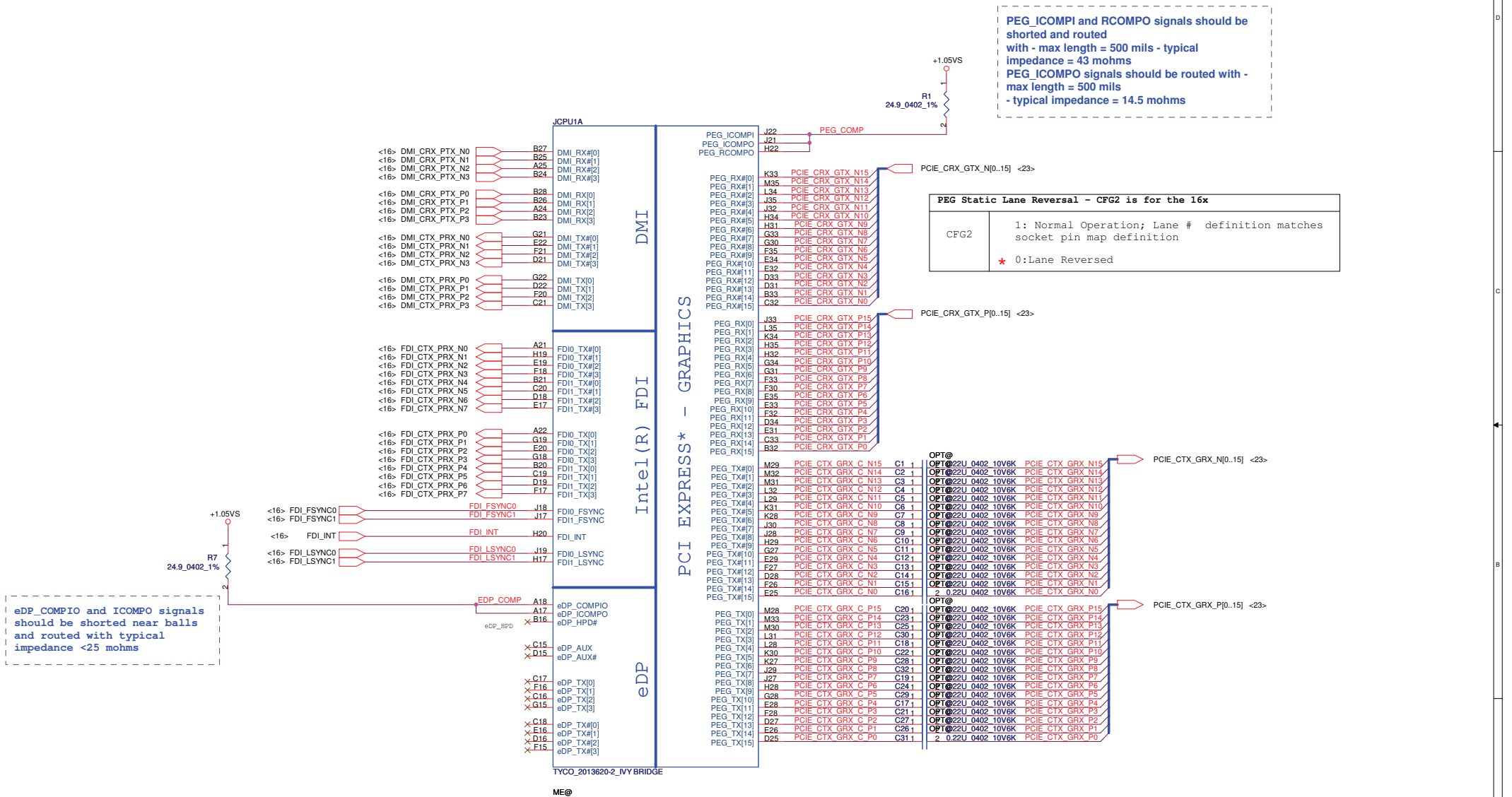

Security Classification	Compal Secret Data		
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Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
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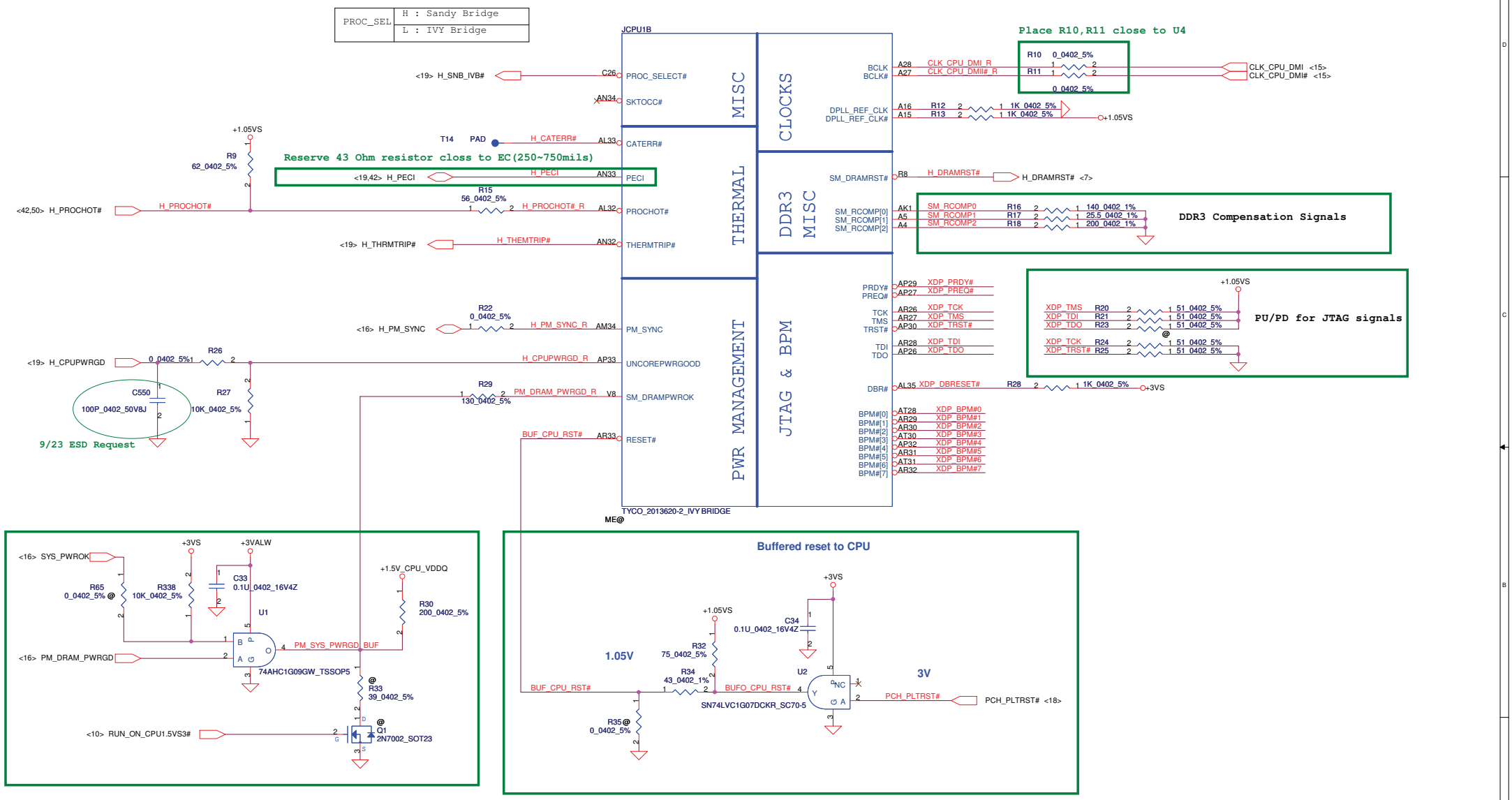

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	PROCESSOR(2/7) PM,XDP,CLK		
Size: Custom	Document Number: QIWY3 LA-8001P		Rev: 1.0
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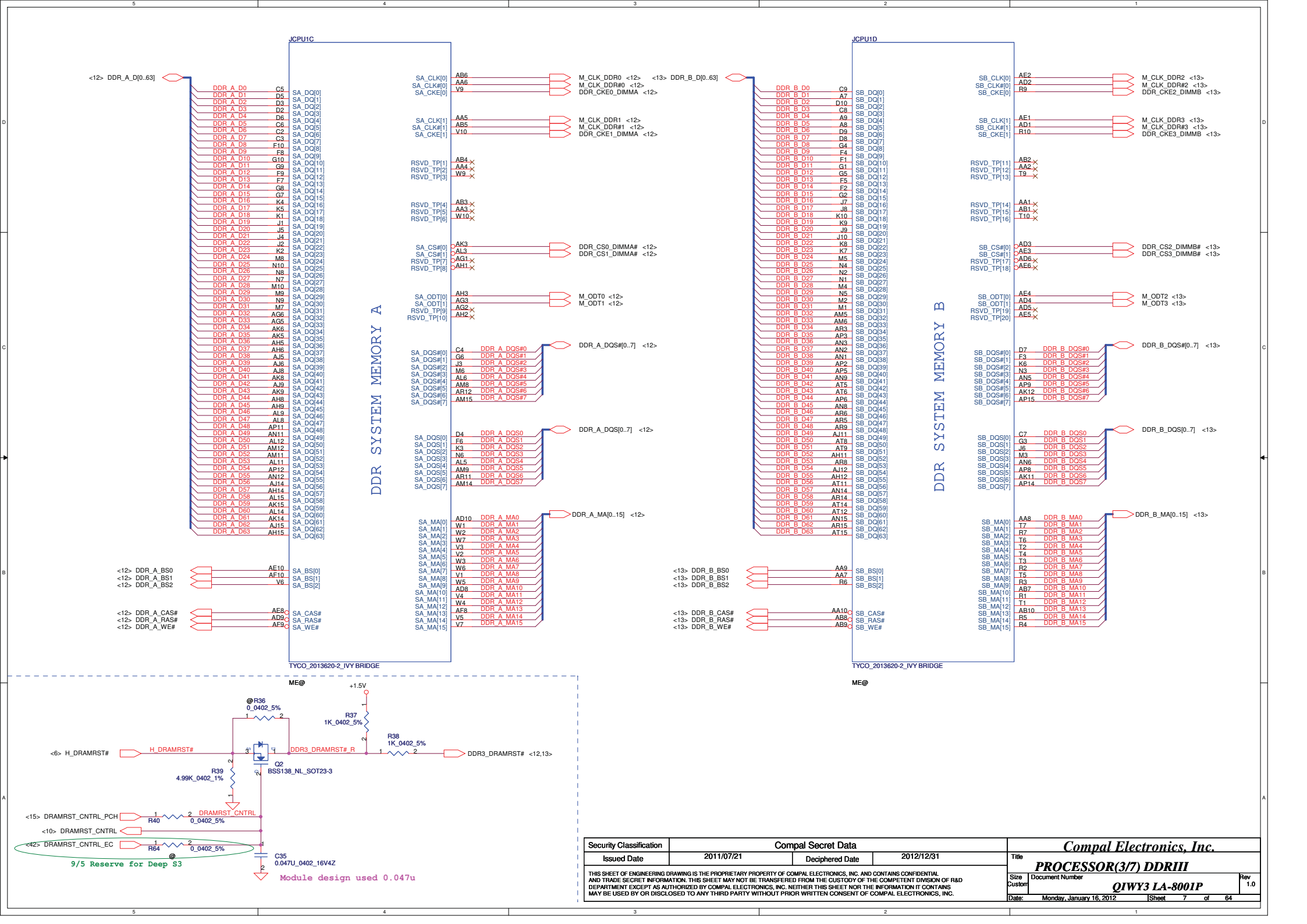

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	PROCESSOR(3/7) DDRIII		
Size: Custom	Document Number: QIWY3 LA-8001P		Rev: 1.0
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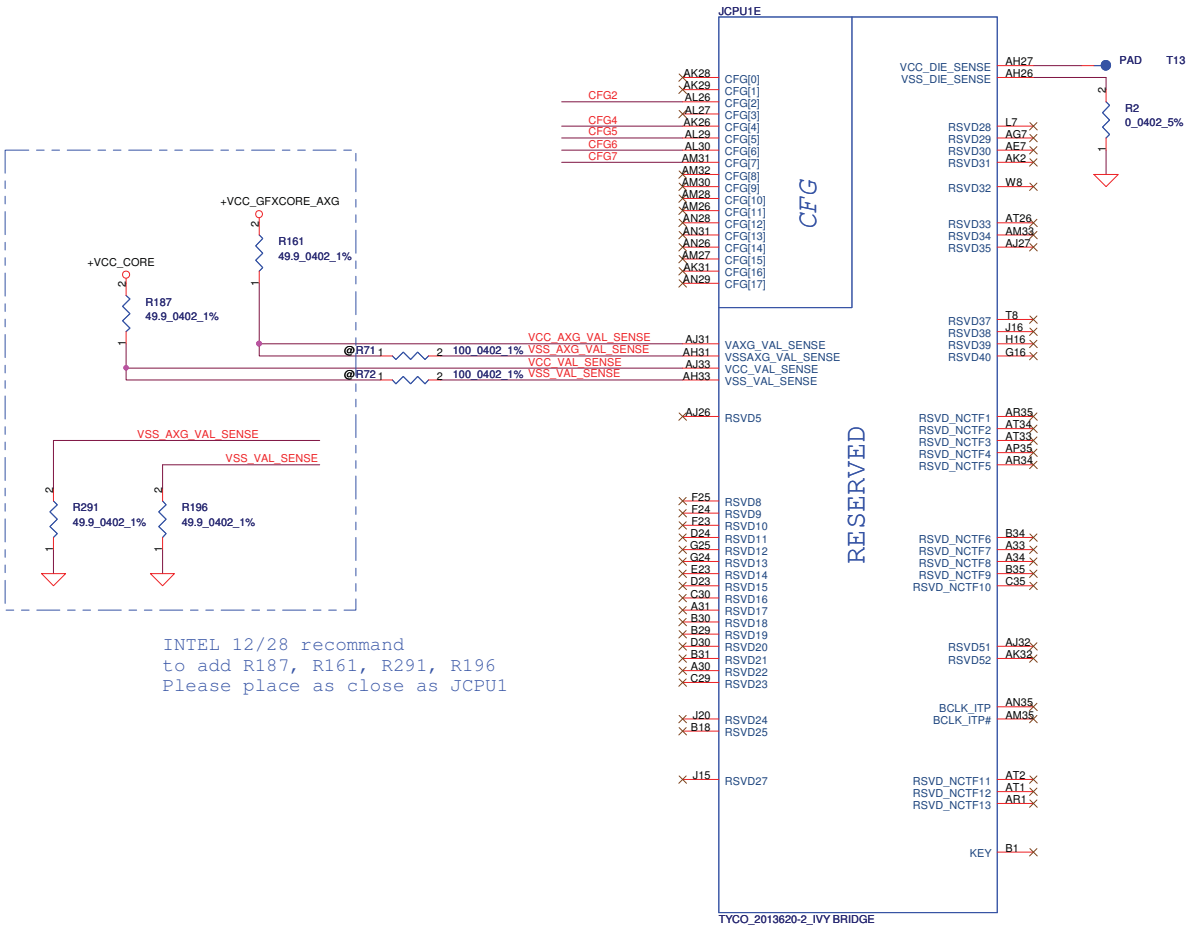
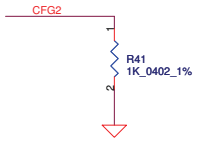
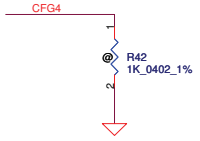
CFG Straps for Processor



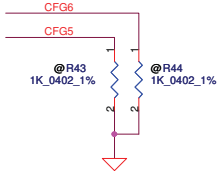
INTEL 12/28 recommand
to add R187, R161, R291, R196
Please place as close as JCPU1



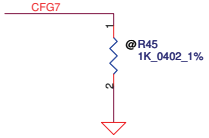
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

CORE SUPPLY

PEG AND DDR

8.5A

+1.05VS

AH13	VCCIO1
AH10	VCCIO2
AG10	VCCIO3
AC10	VCCIO4
Y10	VCCIO5
U10	VCCIO6
P10	VCCIO7
L10	VCCIO8
J14	VCCIO9
J13	VCCIO10
J12	VCCIO11
J11	VCCIO12
H14	VCCIO13
H12	VCCIO14
H11	VCCIO15
G14	VCCIO16
G13	VCCIO17
G12	VCCIO18
F14	VCCIO19
F13	VCCIO20
F12	VCCIO21
F11	VCCIO22
E14	VCCIO23
E12	VCCIO24
E11	VCCIO25
D14	VCCIO26
D13	VCCIO27
D12	VCCIO28
D11	VCCIO29
C14	VCCIO30
C13	VCCIO31
C12	VCCIO32
C11	VCCIO33
B14	VCCIO34
B12	VCCIO35
A14	VCCIO36
A13	VCCIO37
A12	VCCIO38
A11	VCCIO39
J23	VCCIO40

SVID

+1.05VS

Place the PU resistor close to CPU

C36 0.1U_0402_10V7K

R46 75_0402_5%

VIDALERT#
VIDSCLK
VIDSOUT

AJ29	H_CPU_SVIDALRT#	R47	1	2	43_0402_5%
AJ30	H_CPU_SVIDCLK	R48	1	2	0_0402_5%
AJ28	H_CPU_SVIDDAT	R49	1	2	0_0402_5%

VR_SVID_ALRT# <57>
VR_SVID_CLK <57>
VR_SVID_DAT <57>

R50 2 1 130_0402_5% +1.05VS

Place the PU resistor close to CPU

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

SENSE LINES

+VCC_CORE

R51 100_0402_1%

VCC_SENSE
VSS_SENSE

AJ35	VCCSENSE_R	R52	1	2	0_0402_5%
AJ34	VSSSENSE_R	R53	1	2	0_0402_5%

VCCSENSE <57>
VSSSENSE <57>

R1294 2 1 10_0402_1% +1.05VS

@R731 2 100_0402_1%

R54 100_0402_1%

VCCIO_SENSE
VSS_SENSE_VCCIO

B10 VCCIO_SENSE <55>
A10 VSSIO_SENSE VSSIO_SENSE <55>

R1297 10_0402_1%

VSS_SENCE 100ohm +-1% pull-down to GND near processor

TYCO_2013620-2_VX BRIDGE

ME@

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Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

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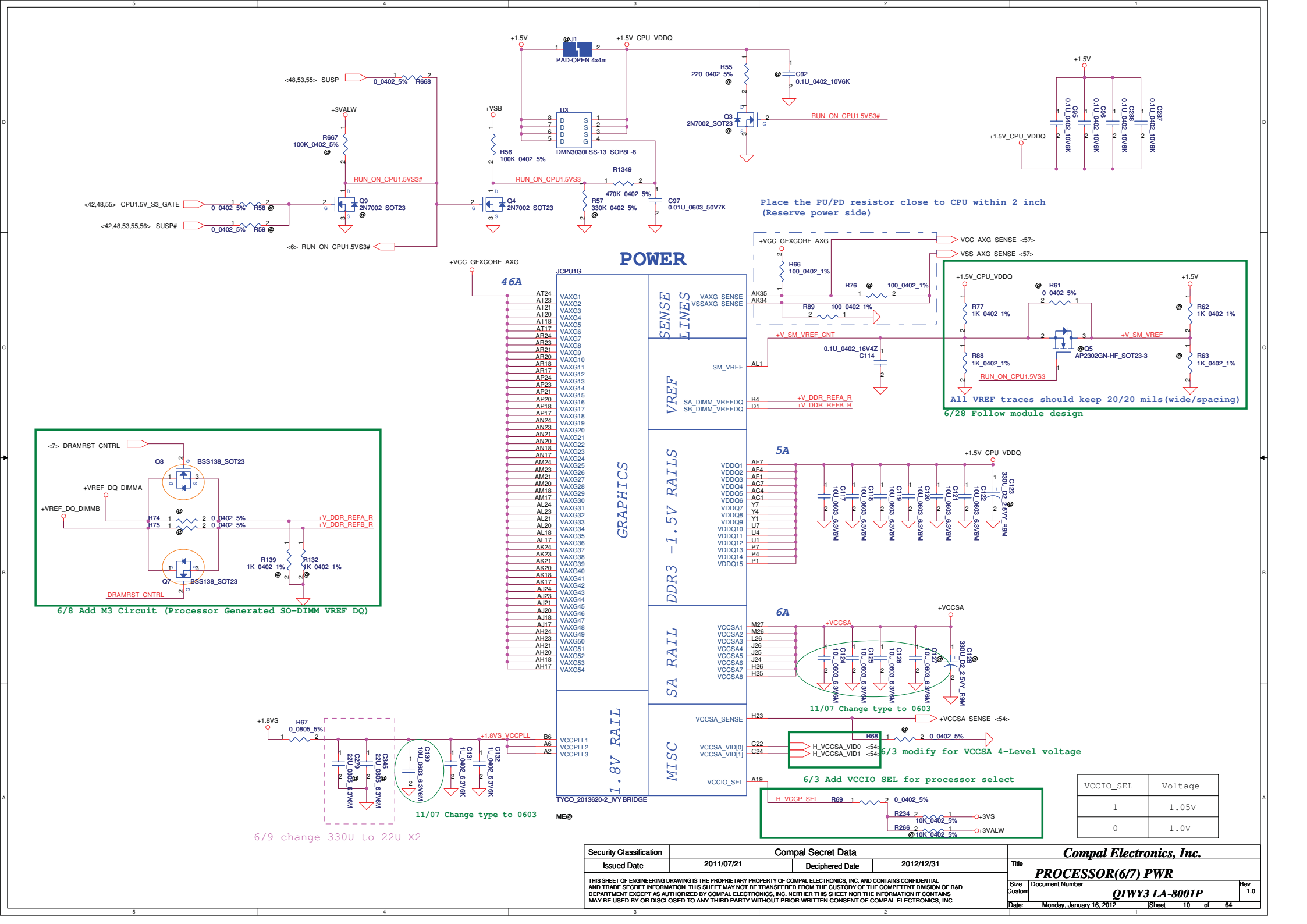
POWER



VCCIO_SEL	Voltage
1	1.05V
0	1.0V

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size: Custom | Document Number: QIWY3 LA-8001P | Rev: 1.0

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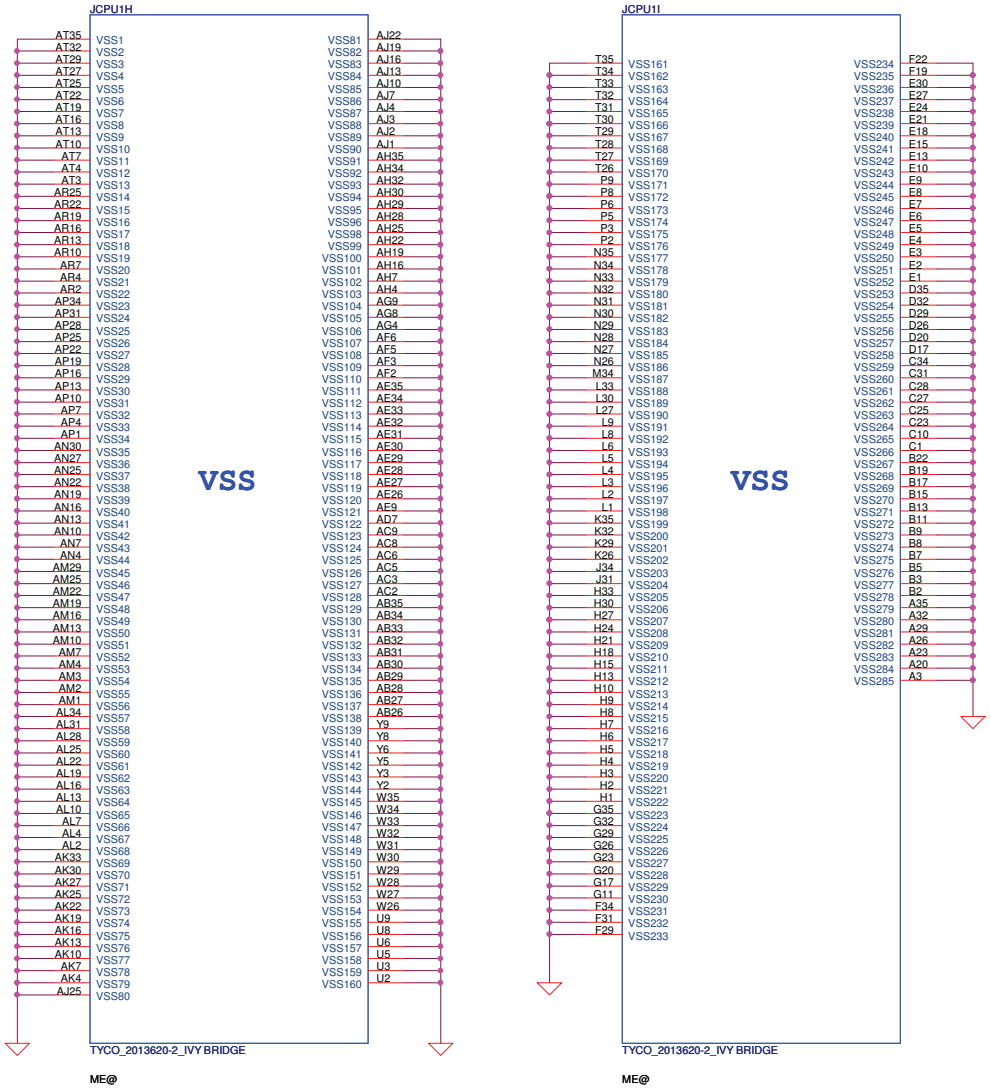

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	QIWY3 LA-8001P	1.0

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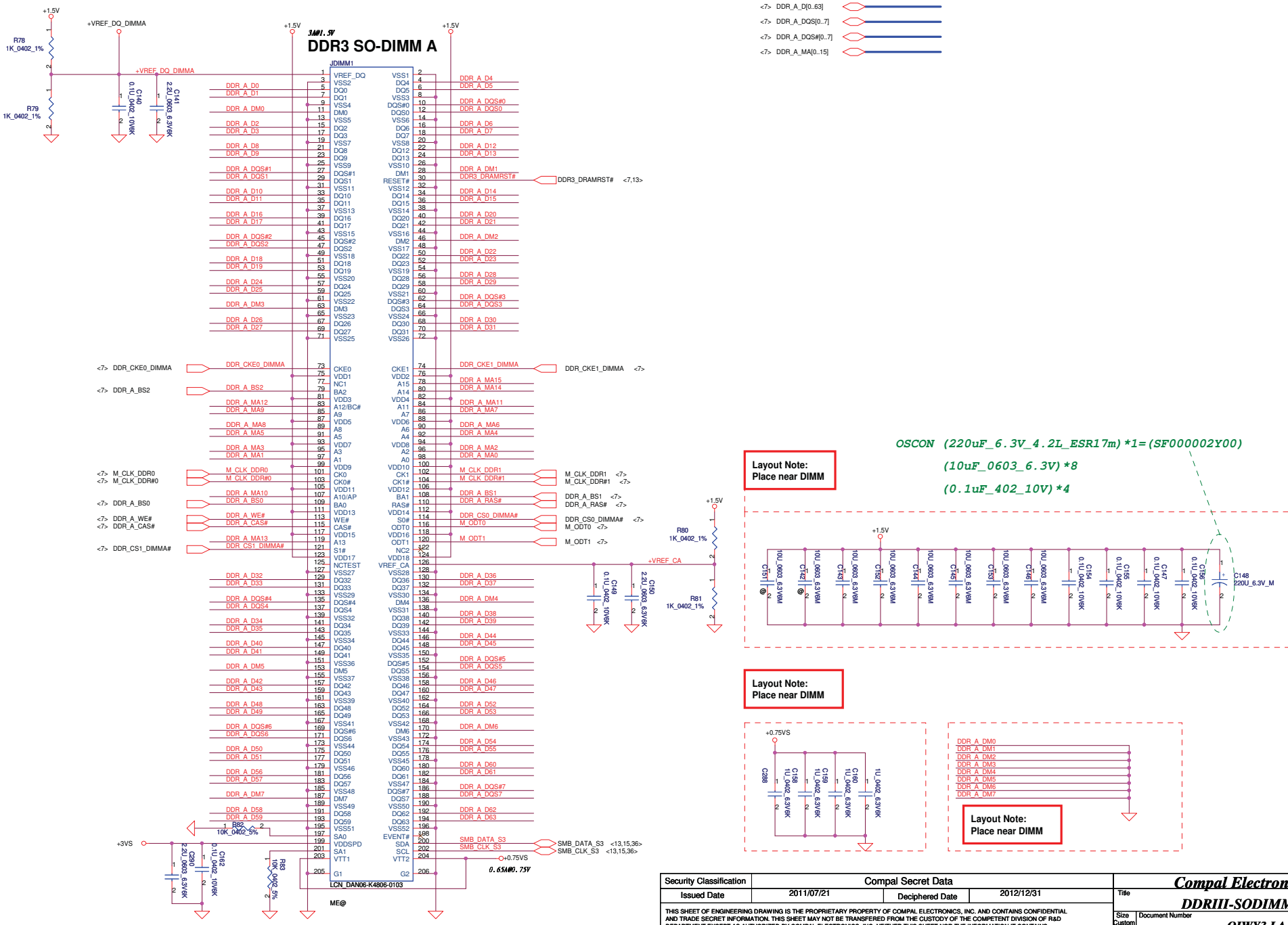

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size	Document Number	Rev
Custom	QIWY3 LA-8001P	1.0

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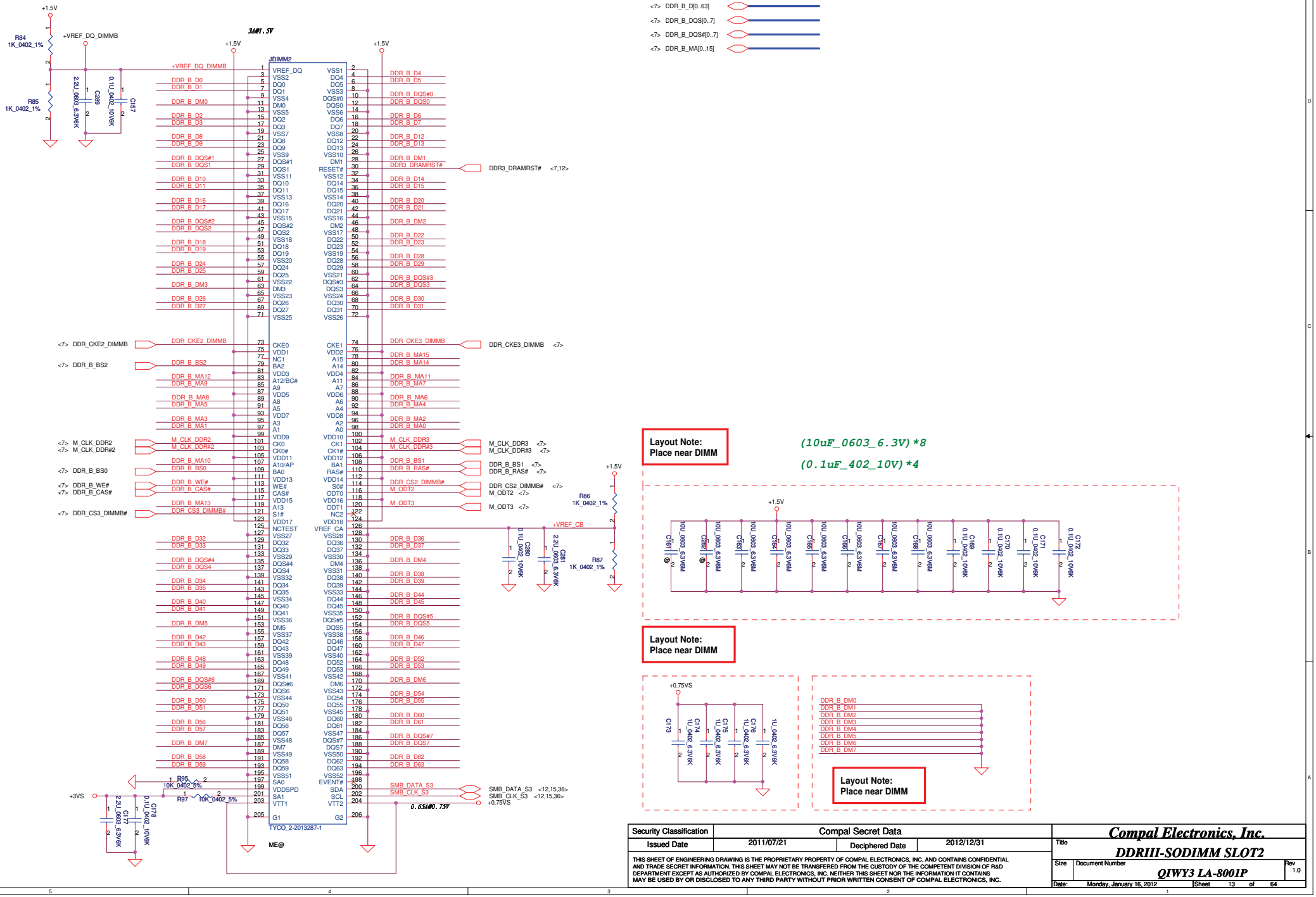


Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size	Document Number	Rev
	QIWY3 LA-8001P	1.0

Date: Monday, January 16, 2012 | Sheet 13 of 64

W=20mils
+RTCVCC
R99
1K_0402_5%
C179
1U_0603_10V4Z
W=20mils
+RTCBATT
CLRP1
SHORT PADS

PCH_RTCX1
R98
10M_0402_5%
PCH_RTCX2
Y1
32.768KHZ_12.5PF_CM31532768DZFT
15P_0402_50V8J
C180
C181
18P_0402_50V8J

CMOS

+RTCVCC
R101 1M_0402_5% SM_INTRUDER#
R102 330K_0402_5% PCH_INTVRMEN

INTVRMEN
* H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

+3VS
R105 @ 1K_0402_5% HDA_SPKR
* HIGH= Enable (No Reboot)
LOW= Disable (Default)

+3V_PCH
R106 @ 1K_0402_5% HDA_SDOUT
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3V_PCH
R108 1K_0402_5% HDA_SYNC
This signal has a weak internal pull-down

* On Die PLL VR Select is supplied by
1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Chief River platfrom

+3V_PCH
R121 200_0402_5% @ PCH_JTAG_TDO
R122 200_0402_5% @ PCH_JTAG_TMS
R123 200_0402_5% @ PCH_JTAG_TDI
R125 100_0402_1% @
R126 100_0402_1% @
R128 100_0402_1% @

+RTCVCC
C183 1U_0603_10V4Z
R103 20K_0402_5%
R100 20K_0402_5%
C182 1U_0603_10V4Z
CLRP2 SHORT PADS
CLRP3 SHORT PADS

U4A

PCH_RTCX1	A20	RTCX1	RTC
PCH_RTCX2	C20	RTCX2	
PCH_RTCRST#	D20	RTCRST#	
PCH_SRTCRST#	G22	SRTCRST#	
SM_INTRUDER#	K22	INTRUDER#	
PCH_INTVRMEN	C17	INTVRMEN	
HDA_BIT_CLK	N34	HDA_BCLK	IHDA
HDA_SYNC	L34	HDA_SYNC	
<41> HDA_SPKR	T10	SPKR	
HDA_RST#	K34	HDA_RST#	
<41> HDA_SDIN0	E34	HDA_SDIN0	
	G34	HDA_SDIN1	
	C34	HDA_SDIN2	
	A34	HDA_SDIN3	
<42> ME_FLASH R109 0_0402_5% HDA_SDOUT	A36	HDA_SDO	
R107 @ 1K_0402_1% PCH_GPIO33	C36	HDA_DOCK_EN# / GPIO33	
+3V_PCH R317 10K_0402_5% PCH_GPIO13	N32	HDA_DOCK_RST# / GPIO13	
PCH_JTAG_TCK	J3	JTAG_TCK	JTAG
PCH_JTAG_TMS	H7	JTAG_TMS	
PCH_JTAG_TDI	K5	JTAG_TDI	
PCH_JTAG_TDO	H1	JTAG_TDO	
SPI_CLK_PCH	T3	SPI_CLK	SPI
SPI_SB_CS0#	Y14	SPI_CS0#	
SPI_SB_CS1#	T1	SPI_CS1#	
SPI_SI	V4	SPI_MOSI	
SPI_SO_R	U3	SPI_MISO	

PANTHER-POINT_FCBGA989

11/08 Follow DG change to +5VS

<41> HDA_BITCLK_AUDIO R112 33_0402_5% R114 HDA_BIT_CLK
<41> HDA_SYNC_AUDIO R116 33_0402_5% HDA_SYNC_R
<41> HDA_RST_AUDIO# R118 33_0402_5% HDA_RST#
<41> HDA_SDOUT_AUDIO R110 33_0402_5% HDA_SDOUT

+5VS
Q10 BSS138_NL_SOT23-3
HDA_SYNC
R1353 1M_0402_5%

FWH0 / LAD0	C38	LPC_AD0	LPC
FWH1 / LAD1	A38	LPC_AD1	
FWH2 / LAD2	B37	LPC_AD2	
FWH3 / LAD3	C37	LPC_AD3	
FWH4 / LFRAME#	D36	LPC_FRAME#	
LDRQ0#	E36		
LDRQ1# / GPIO23	K36		
SERIRQ	V5	SERIRQ	

LPC_AD0 <36,42>
LPC_AD1 <36,42>
LPC_AD2 <36,42>
LPC_AD3 <36,42>
EC and Mini card debug port
LPC_FRAME# <36,42>
R104 10K_0402_5% +3VS
SERIRQ <42>

SATA0RXN	AM3	SATA_DTX_C_IRX_N0	SATA 6G
SATA0RXP	AM1	SATA_DTX_C_IRX_P0	
SATA0TXN	AP7	SATA_ITX_C_DRX_N0 0.01U_0402_16V7K	C184 SATA_ITX_DRX_N0
SATA0TXP	AP5	SATA_ITX_C_DRX_P0 0.01U_0402_16V7K	C185 SATA_ITX_DRX_P0
SATA1RXN	AM10	SATA_DTX_C_IRX_N1	
SATA1RXP	AM8	SATA_DTX_C_IRX_P1	
SATA1TXN	AP11	SATA_ITX_C_DRX_N1 0.01U_0402_16V7K	C273 SATA_ITX_DRX_N1
SATA1TXP	AP10	SATA_ITX_C_DRX_P1 0.01U_0402_16V7K	C272 SATA_ITX_DRX_P1
SATA2RXN	AD7	SATA_DTX_C_IRX_N2	
SATA2RXP	AD5	SATA_DTX_C_IRX_P2	
SATA2TXN	AH5	SATA_ITX_C_DRX_N2 0.01U_0402_16V7K	C186 SATA_ITX_DRX_N2_CONN
SATA2TXP	AH4	SATA_ITX_C_DRX_P2 0.01U_0402_16V7K	C187 SATA_ITX_DRX_P2_CONN
SATA3RXN	AB8		SATA
SATA3RXP	AB10		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	Y7		
SATA4RXP	Y5		
SATA4TXN	AD3		
SATA4TXP	AD1		
SATA5RXN	Y3		
SATA5RXP	Y1		
SATA5TXN	AB3		
SATA5TXP	AB1		
SATAICOMPO	Y11	R111 37.4_0402_1% +1.05VS_VCC_SATA	
SATAICOMPI	Y10	SATA_COMP	
SATA3RCOMPO	AB12	R113 49.9_0402_1% +1.05VS_SATA3	
SATA3COMPI	AB13	SATA3_COMP	
SATA3RBIAS	AH1	RBIAS_SATA3 R115 750_0402_1%	
SATALED#	P3	SATALED# R120 10K_0402_5% +3VS	
SATA0GP / GPIO21	V14	PCH_GPIO21 R119 10K_0402_5% +3VS	
SATA1GP / GPIO19	P1	BBS_BIT0_R R1418 @ 0_0402_5% SATA_DET# <36>	
		R316 10K_0402_5% +3VS	

SSD
HDD
ODD

SPI ROM FOR ME
& Non-share ROM.

2MB P/N : SA00003FO10

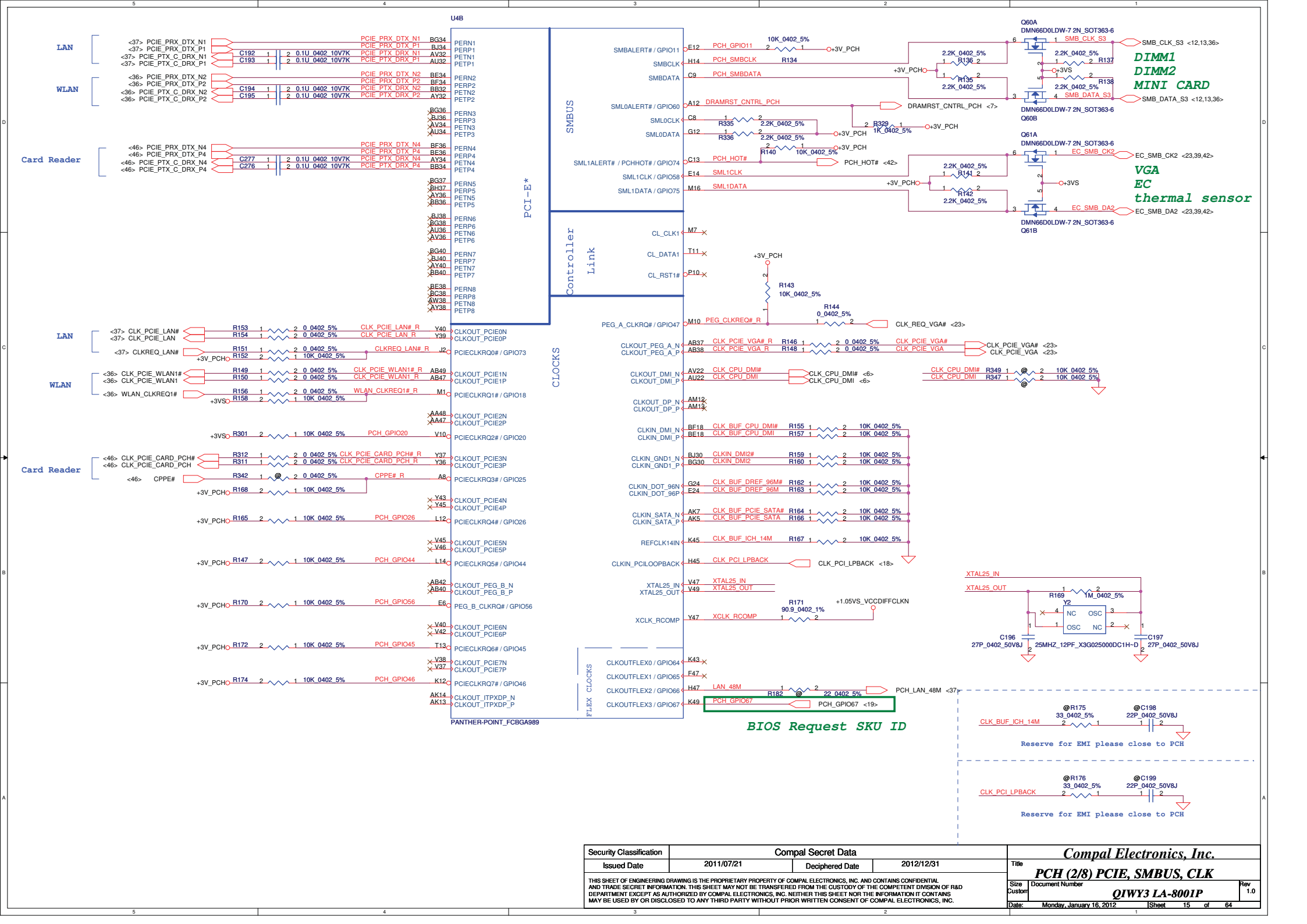
+3VS
R292 SPI_WP#_1 3.3K_0402_5%
R246 SPI_HOLD#_1 3.3K_0402_5%
R303 0_0402_5%
SPI_SB_CS1# SPI_SB_CS1#_R
SPI_SO_R SPI_SO_L1
SPI_WP#_1
R294 33_0402_5%
U9
CS# VCC
DO(IO1) HOLD#(IO3)
WP#(IO2) CLK
GND DI(IO0)
W25Q16BVSSIG_SO8
+3VS
C275 0.1U_0402_16V4Z
R299 33_0402_5%
SPI_HOLD#_1
SPI_CLK_PCH_1
SPI_SI_R1
SPI_CLK_PCH
SPI_SI
R199 33_0402_5%

4MB P/N : SA00003K800

+3VS
R127 SPI_WP# 3.3K_0402_5%
R129 SPI_HOLD# 3.3K_0402_5%
R130 0_0402_5%
SPI_SB_CS0# SPI_SB_CS0#_R
SPI_SO_R SPI_SO_L
SPI_WP#
R131 33_0402_5%
U5
CS# VCC
DO HOLD#
WP# CLK
GND DI
W25Q32BVSSIG_SO8
+3VS
C191 0.1U_0402_16V4Z
R298 33_0402_5%
SPI_HOLD#
SPI_CLK_PCH_0
SPI_SI_R
SPI_CLK_PCH
SPI_SI
R133 33_0402_5%
SPI_CLK_PCH
R124 33_0402_5% @
C190 22P_0402_50V8J @

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.
Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: QIWY3 LA-8001P | Rev: 1.0
Date: Monday, January 16, 2012 | Sheet 14 of 64



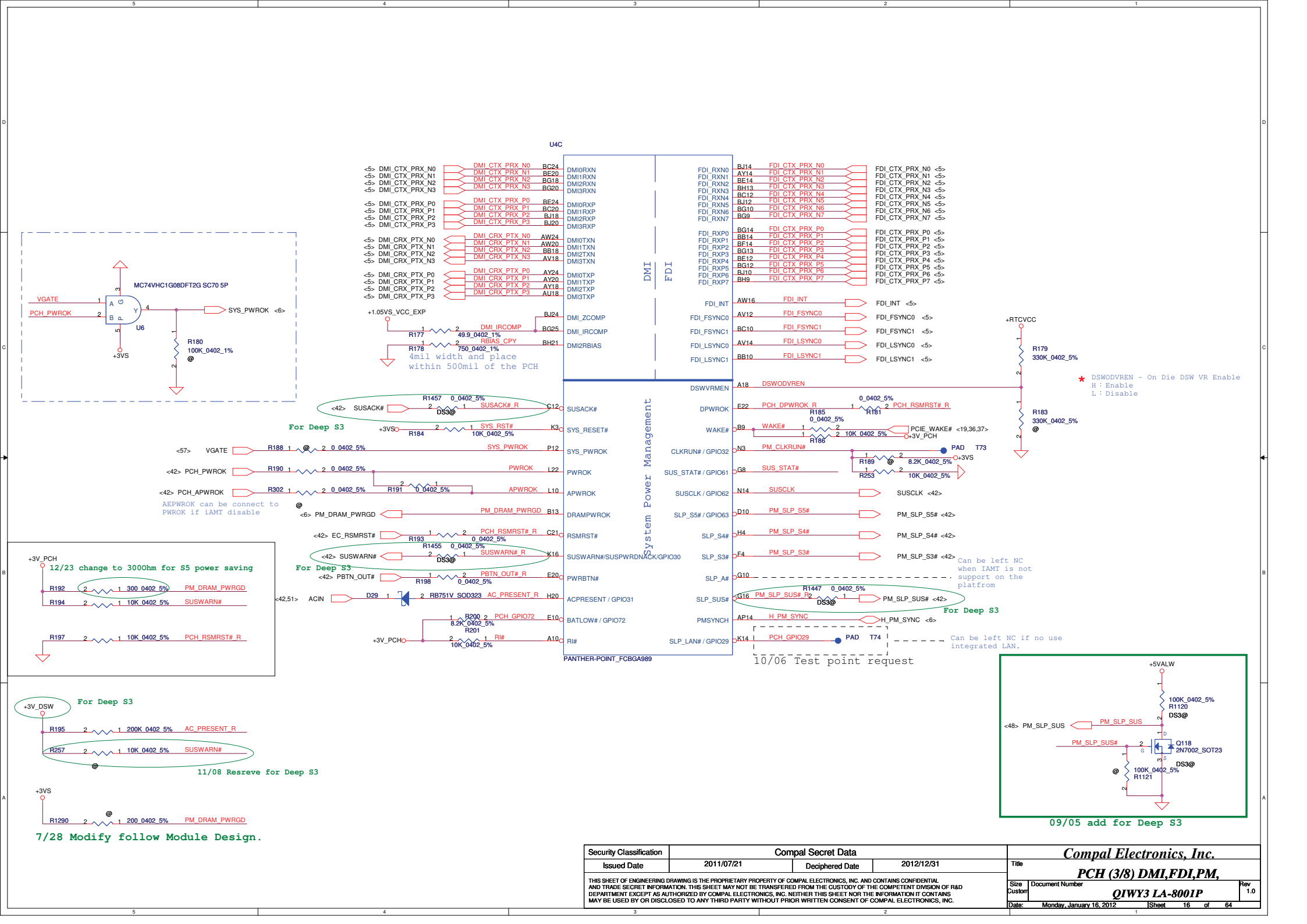
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

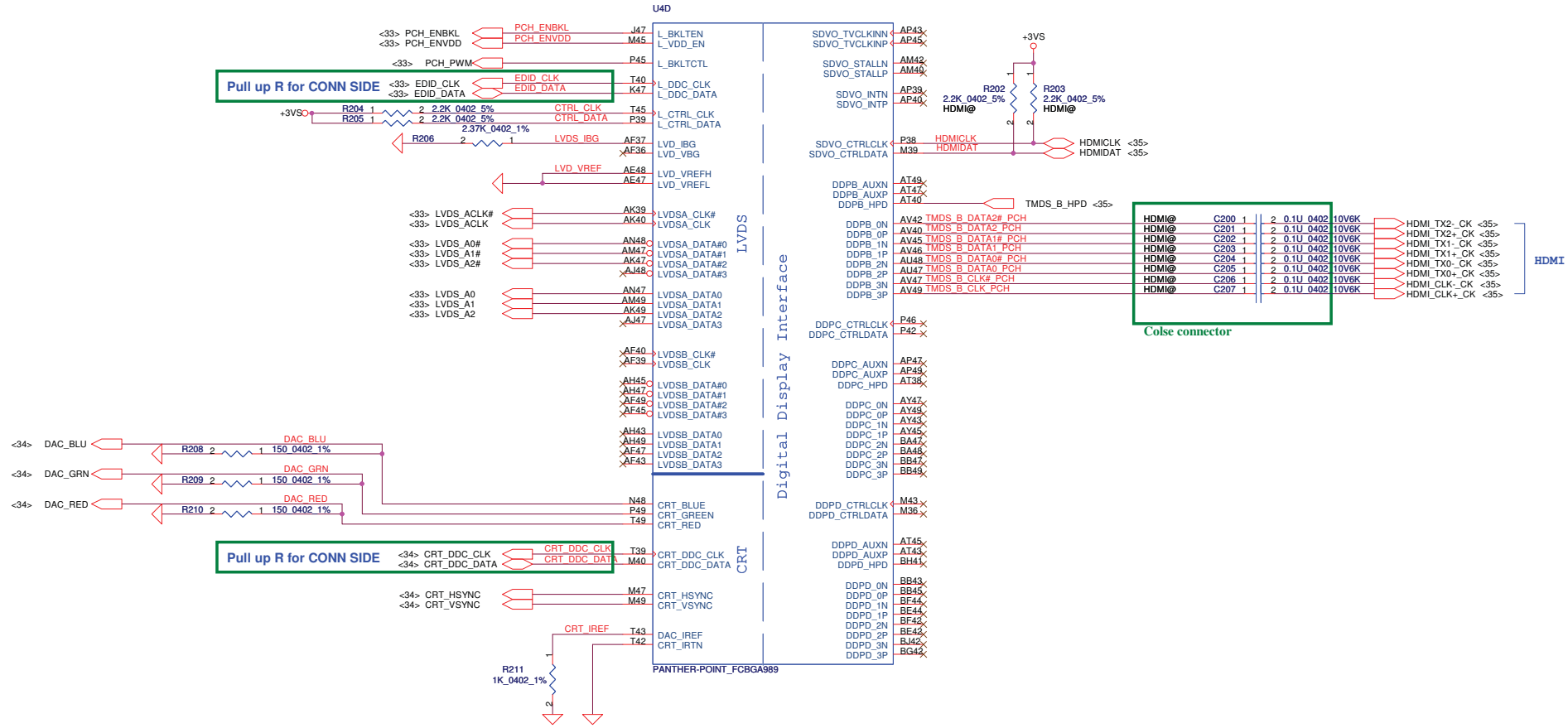
Size	Document Number	Rev
Custom	QIWY3 LA-8001P	1.0

Date: Monday, January 16, 2012 Sheet 15 of 64



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	PCH (3/8) DMI,FDI,PM,		
Size: Custom	Document Number: QIWY3 LA-8001P		Rev: 1.0
Date: Monday, January 16, 2012	Sheet 16 of 64		



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size: Custom | Document Number: QIWY3 LA-8001P | Rev: 1.0

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PPT EDS DOC#474146

USB30

PORT1	RIGHT USB (SUB/B)
PORT2	
PORT3	LEFT USB
PORT4	LEFT USB

USB DEBUG=PORT1 AND PORT9

USBP0N / USBP0P	RIGHT USB (SUB/B)
USBP2N / USBP2P	LEFT USB
USBP3N / USBP3P	LEFT USB
USBP4N / USBP4P	
USBP5N / USBP5P	USB Camera
USBP6N / USBP6P	
USBP7N / USBP7P	
USBP8N / USBP8P	
USBP9N / USBP9P	RIGHT USB (Cable)
USBP10N / USBP10P	WLAN
USBP11N / USBP11P	
USBP12N / USBP12P	
USBP13N / USBP13P	Bluetooth

Some PCH config not support USB port 6 & 7.

Within 500 mils

A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default ★

Boot BIOS Strap bit1 BBS1			
	Bit11	Bit10	Boot BIOS Destination
GNT1#/ GPIO51	0	1	Reserved
	1	0	Reserved
	1	1 ★	SPI (Default)
	0	0	LPC

GPIO53=This Signal has a weak internal pull-up.
NOTE: The internal pull-up is disabled after PLTRST# deasserts.

7/9 Reserve

PANTHER-POINT_FCBGA989

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

Size: Custom | Document Number: QIWY3 LA-8001P | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 18 of 64

Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70	PCH_GPIO69
SG	0	0	X	X
Reserve	0	1	X	X
DIS	1	0	X	X
UMA	1	1	X	X
14"	X	X	0	0
14"L	X	X	0	1
15"	X	X	1	0
Reserve	X	X	1	1

MB ID

+3VS R711 R708 R704 R703 R712 R709 R706 R705 10K_0402_5%

PCH_GPIO38 PCH_GPIO67 PCH_GPIO69 PCH_GPIO70

<15> PCH_GPIO67

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+3V_PCH R280 10K_0402_5% EC_SMI#
R235 1K_0402_5%
R240 1K_0402_5% PCH_GPIO28

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

+3V_DSW AOAC@ R207 10K_0402_5%
R245 10K_0402_5% AOAC_WAKE#

+3VS R250 200_0402_5% PCH_GPIO36
R264 10K_0402_5%

+3VS R244 10K_0402_5% PCH_GPIO37
R259 10K_0402_5%

<23> GC6_EVENT# GC6_EVENT#

+3VS R233 10K_0402_5%

+3VS R227 10K_0402_5% PCH_GPIO1
R228 10K_0402_5% PCH_GPIO6

<42> EC_SCI# EC_SCI#
<42> EC_SMI# EC_SMI#

+3V_PCH R229 10K_0402_5% PCH_GPIO12
R230 10K_0402_5% EC_LID_OUT#

<42> EC_LID_OUT#

+3VS R231 10K_0402_5% PCH_GPIO16
R232 10K_0402_1%

<27,53,56> DGPU_PWROK R339 0_0402_5% DGPU_PWROK_R

<36> BT_DISABLE +3VS R238 10K_0402_5% BT_DISABLE

<40> ODD_EN ODD_EN

AOAC@
<16,36,37> PCIE_WAKE# 0_0402_5% R224 AOAC_WAKE#

+3V_PCH R241 10K_0402_5% PCH_GPIO28
<36,44> PCH_BT_ON# +3VS R242 10K_0402_5% PCH_BT_ON#
R243 10K_0402_5% PCH_GPIO35

PCH_GPIO36
PCH_GPIO37
PCH_GPIO38

+3VS R247 10K_0402_5% PCH_GPIO39
R248 10K_0402_5% PCH_GPIO48
+3VS R249 10K_0402_5% PCH_GPIO49
+3V_PCH R251 10K_0402_5% PCH_GPIO57

U4F

T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40 PCH_GPIO68
A42	TACH1 / GPIO1	TACH5 / GPIO69	B41 PCH_GPIO69
H36	TACH2 / GPIO6	TACH6 / GPIO70	C41 PCH_GPIO70
E38	TACH3 / GPIO7	TACH7 / GPIO71	A40
C10	GPIO8		
C4	LAN_PHY_PWR_CTRL / GPIO12		
G2	GPIO15	A20GATE	P4
U2	SATA4GP / GPIO16	PECI	AU16 PCH_PECI_R 0_0402_5% R237 H_PECI <6,42>
D40	TACH0 / GPIO17	RCIN#	P5 KBRST# KBRST# <42>
T5	SCLOCK / GPIO22	PROCPWRGD	AY11 H_CPUPWRGD <6>
E8	GPIO24	THRMTRIP#	AY10 PCH_THRMTRIP#_R R239 390_0402_5% H_THRMTRIP# H_THRMTRIP# <6>
E16	GPIO27	INIT3_3V#	T14 PCH_THRMTRIP#_R <23>
P8	GPIO28	DF_TVS	AY1 NV_CLE
K1	STP_PCI# / GPIO34	TS_VSS1	AH8
K4	GPIO35	TS_VSS2	AK11
V8	SATA2GP / GPIO36	TS_VSS3	AH10
M5	SATA3GP / GPIO37	TS_VSS4	AK10
N2	SLOAD / GPIO38	NC_1	P37
M3	SDATAOUT0 / GPIO39		
V13	SDATAOUT1 / GPIO48	VSS_NCTF_15	BG2
V3	SATA5GP / GPIO49 / TEMP_ALERT#	VSS_NCTF_16	BG48
D6	GPIO57	VSS_NCTF_17	BH3
		VSS_NCTF_18	BH47
A4	VSS_NCTF_1	VSS_NCTF_19	BJ4
A44	VSS_NCTF_2	VSS_NCTF_20	BJ44
A45	VSS_NCTF_3	VSS_NCTF_21	BJ45
A46	VSS_NCTF_4	VSS_NCTF_22	BJ46
A5	VSS_NCTF_5	VSS_NCTF_23	BJ5
A6	VSS_NCTF_6	VSS_NCTF_24	BJ6
B3	VSS_NCTF_7	VSS_NCTF_25	C2
B47	VSS_NCTF_8	VSS_NCTF_26	C48
BD1	VSS_NCTF_9	VSS_NCTF_27	D1
BD49	VSS_NCTF_10	VSS_NCTF_28	D49
BE1	VSS_NCTF_11	VSS_NCTF_29	E1
BE49	VSS_NCTF_12	VSS_NCTF_30	E49
BF1	VSS_NCTF_13	VSS_NCTF_31	F1
BF49	VSS_NCTF_14	VSS_NCTF_32	F49

GPIO | CPU/MISC | NCTF

PANTHER-POINT_FCBGA989

9/18 Reseve for SKU ID

+3VS R236 10K_0402_5% GATEA20 <42>

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

+3VS PCH_GPIO68 R255 10K_0402_5%
KBRST# R226 10K_0402_5%

PROC_SEL	H : Sandy Bridge
	L : INV Bridge

+1.8VS R216 2.2K_0402_5%
NV_CLE R217 1K_0402_5% H_SNB_IVB# <6>
CLOSE TO THE BRANCHING POINT

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: QIWY3 LA-8001P | Rev: 1.0

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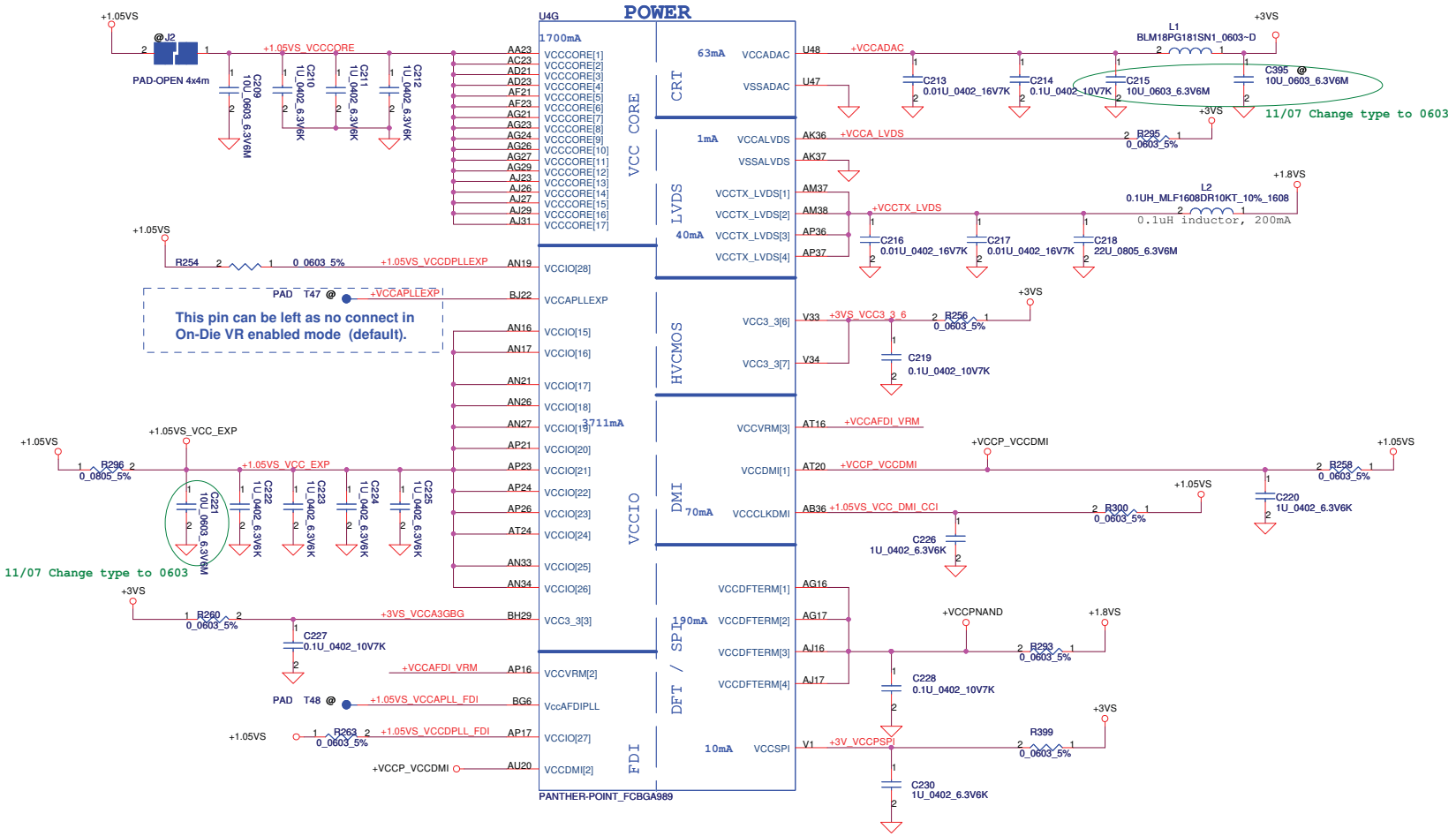


PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: QIWY3 LA-8001P | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 20 of 64

Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec

VCCDMI = 42mA detal waiting for newest spec

POWER

U4J

PANTHER-POINT_FCBGA989

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

CPU

MISC

RTC

HDA

For Deep S3

11/07 Change type to 0603

On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2
,VCCAPLLSATA

On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2
,VCCAPLLSATA

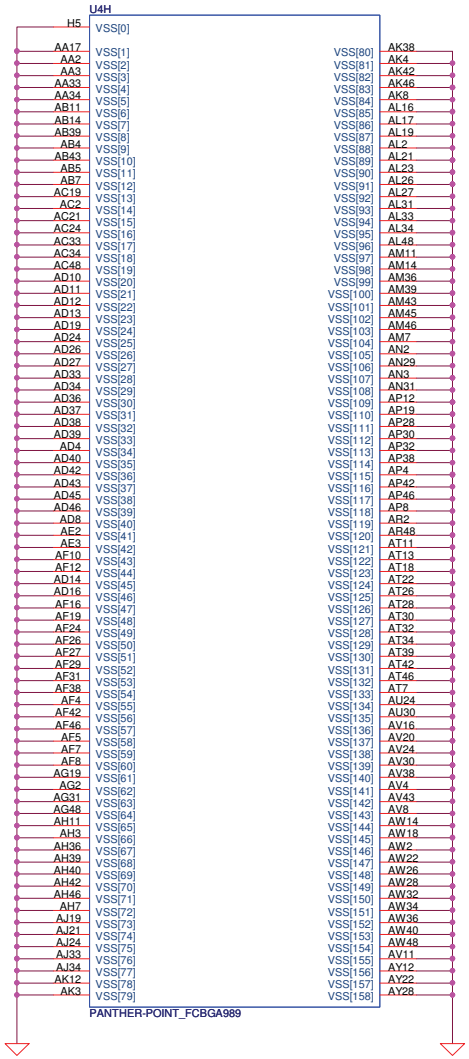
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

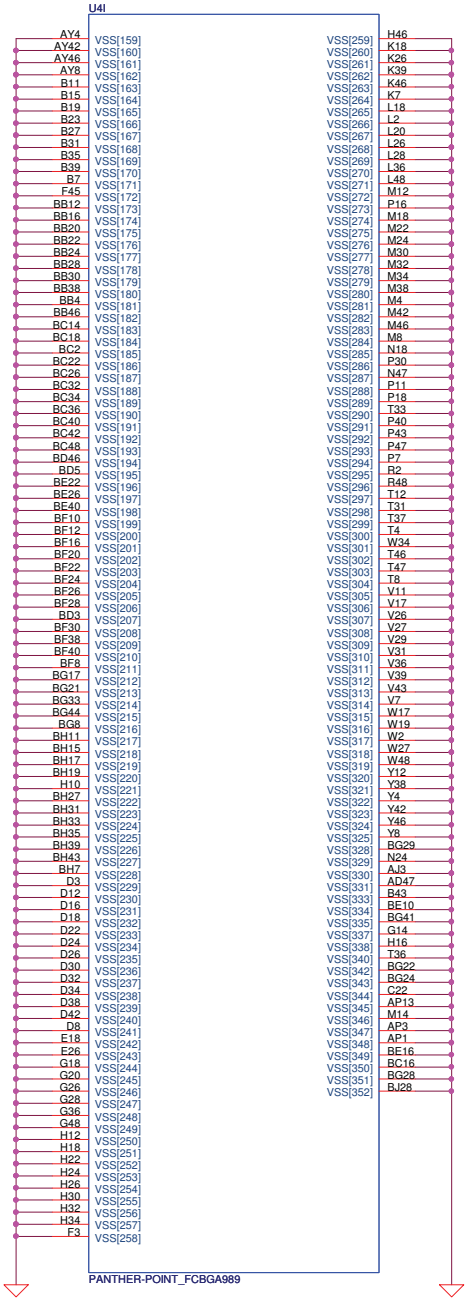
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: QIWY3 LA-8001P | Rev: 1.0

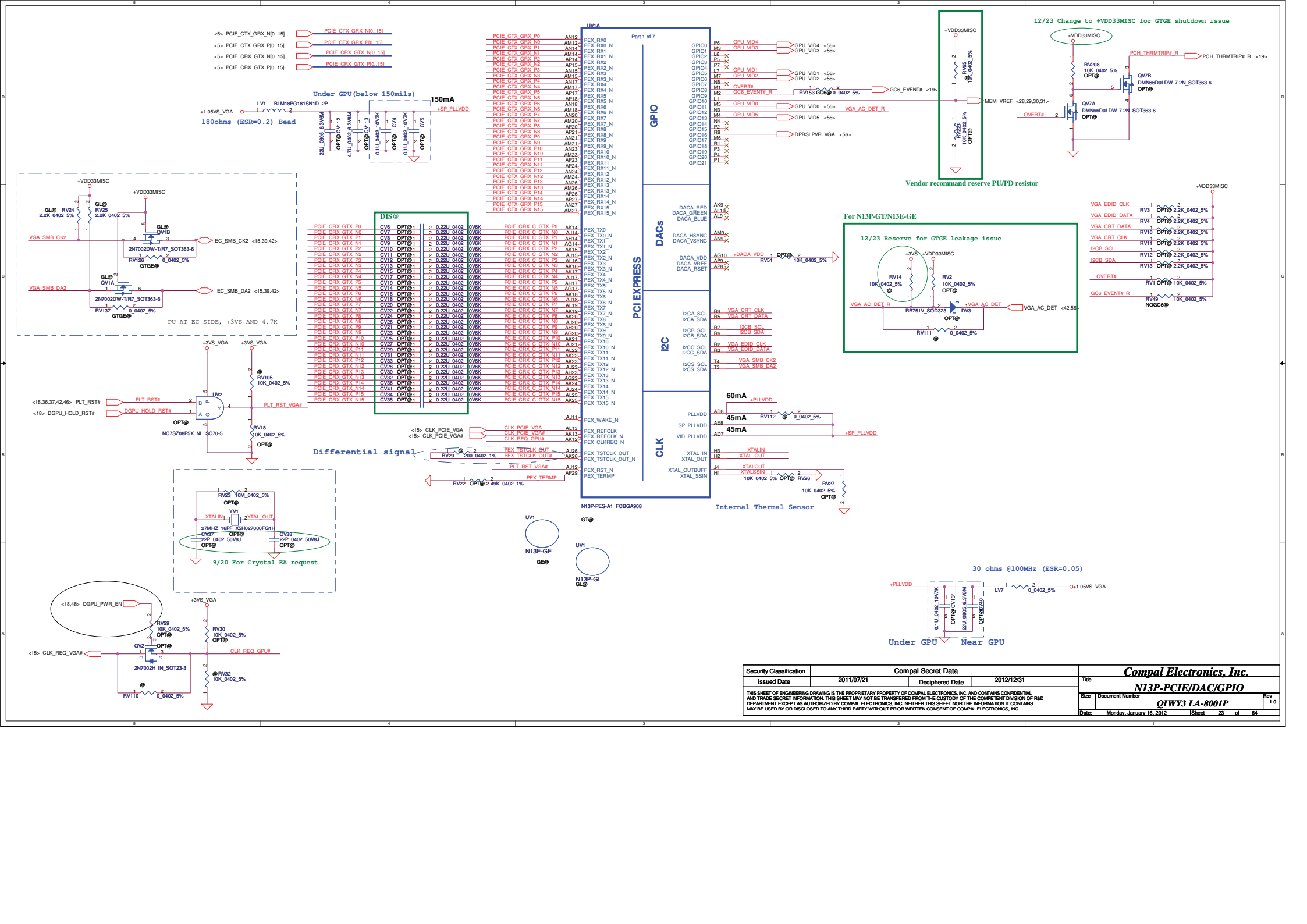
Date: Monday, January 16, 2012 | Sheet 21 of 64





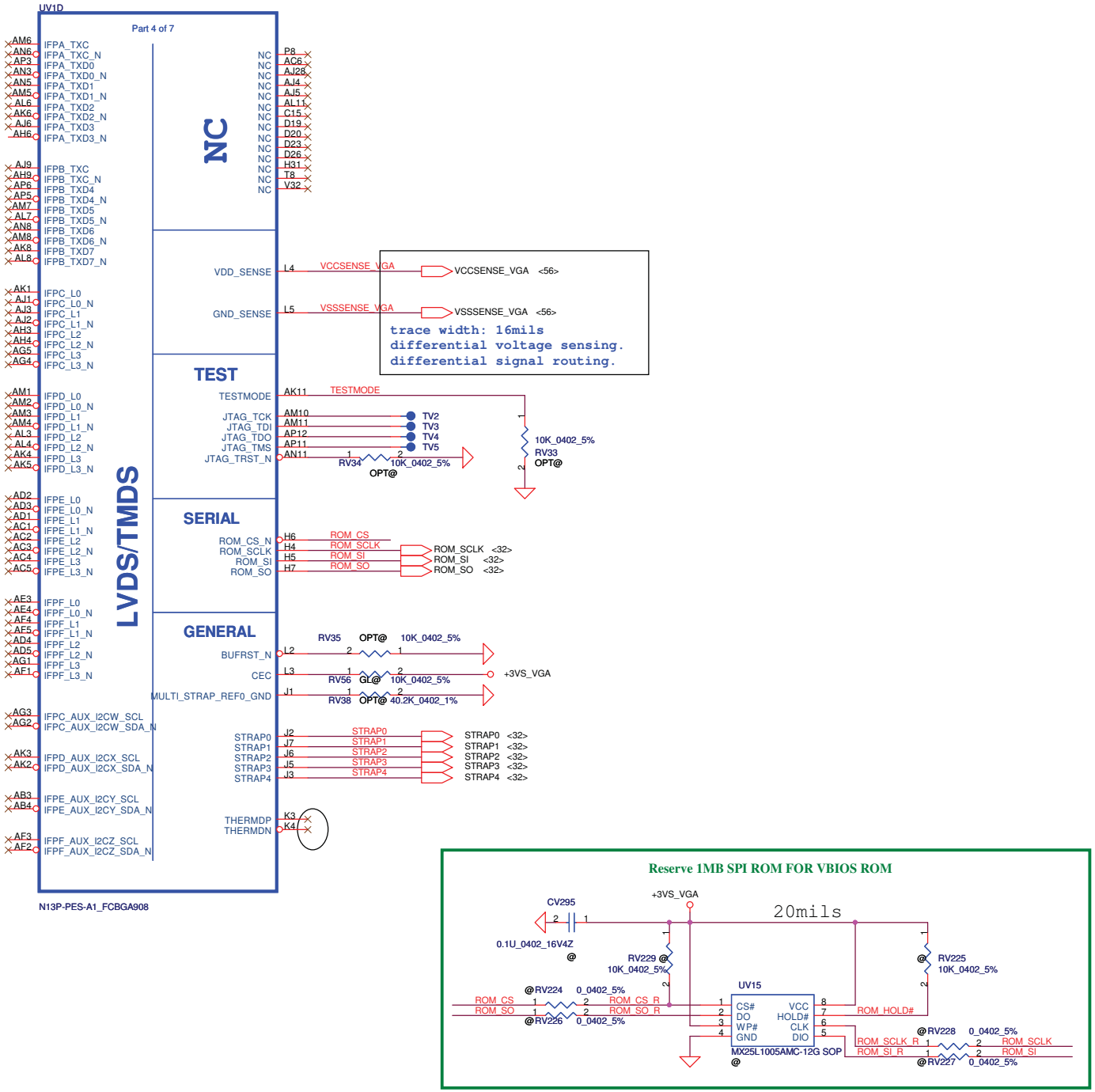
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.		
Title	PCH (9/9) VSS	
Size: Custom	Document Number: QIWY3 LA-8001P	Rev: 1.0
Date: Monday, January 16, 2012	Sheet 22 of 64	



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	N13P-PCIE/DAC/GPIO		
Size	Document Number		Rev
	Q1WY3 LA-8001P		1.0
Date: Monday, January 16, 2012	Sheet 23 of 64		



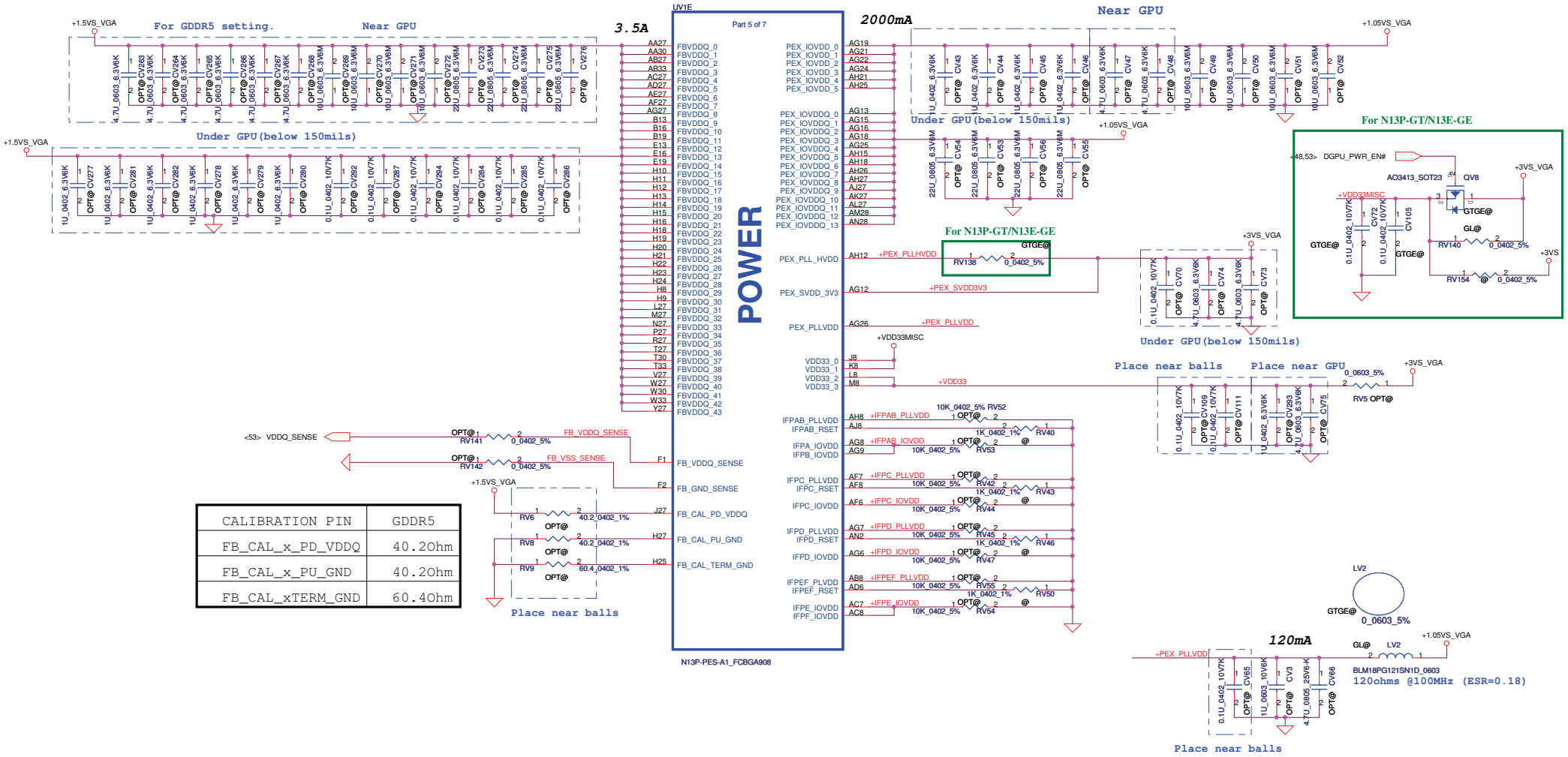
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **N13P-LVDS/HDMI/DP/THM**

Size	Document Number	Rev
	QIWY3 LA-8001P	1.0

Date: Monday, January 16, 2012 | Sheet 24 of 64



CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

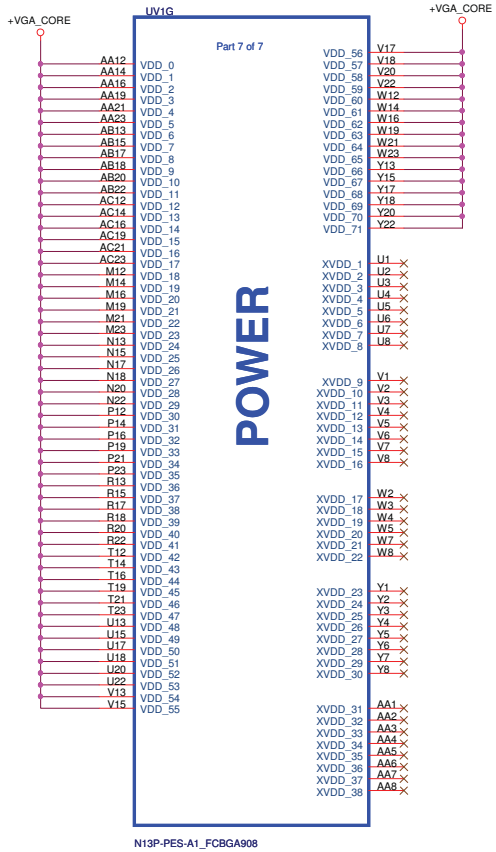
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

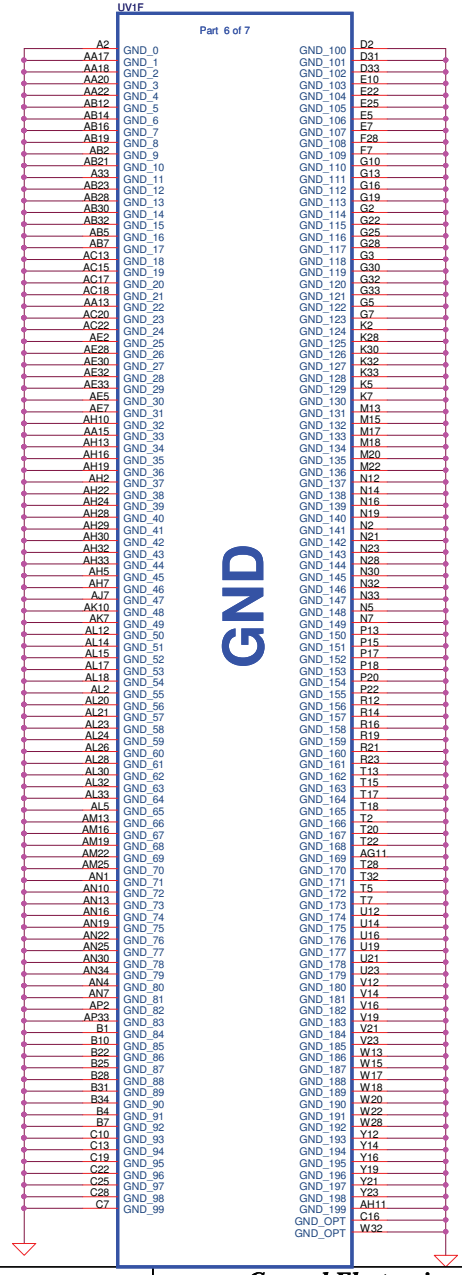
Compal Electronics, Inc.

Title: N13P-POWER

Size: | Document Number: QIWY3 LA-8001P | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 25 of 64





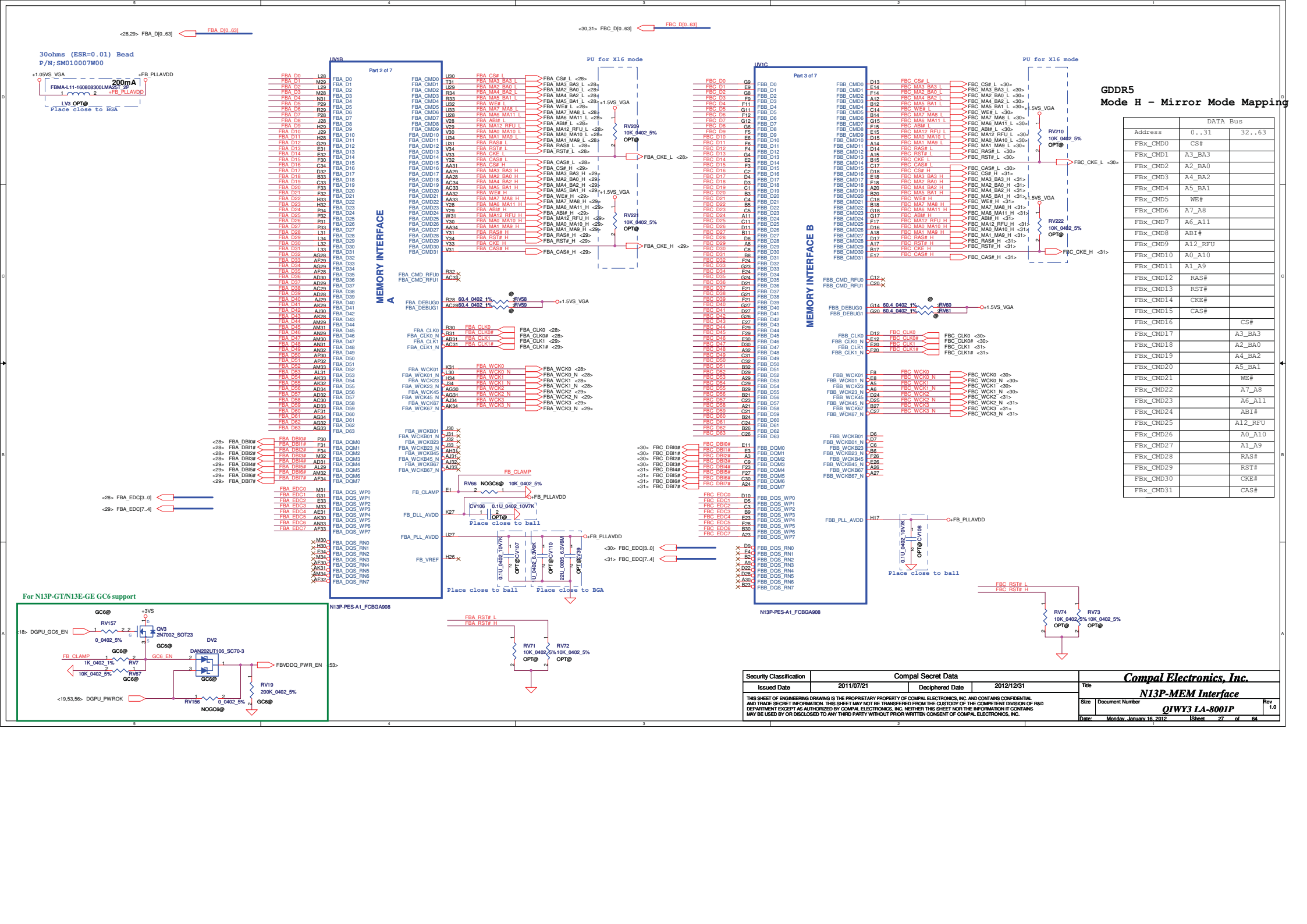
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P-VGA CORE, GND

Size	Document Number	Rev
	QIWY3 LA-8001P	1.0

Date: Monday, January 16, 2012 | Sheet 26 of 64



	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

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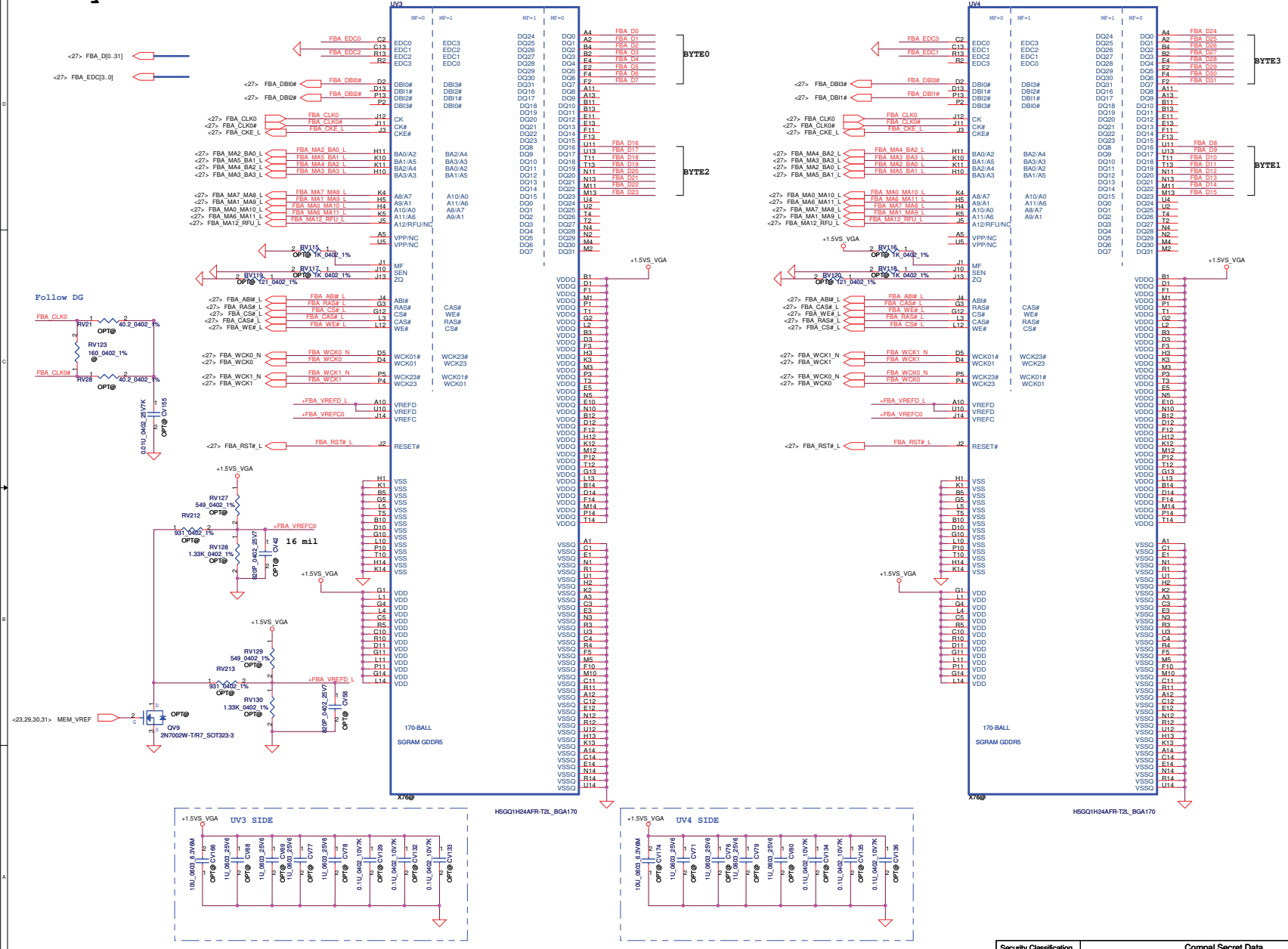
Compal Electronics, Inc.

Title: N13P-MEM Interface

Size: | Document Number: QIWY3 LA-8001P | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 27 of 64

Memory Partition A - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P-VRAM A Lower

Size: | Document Number: QIWY3 LA-8001P | Rev: 1.0

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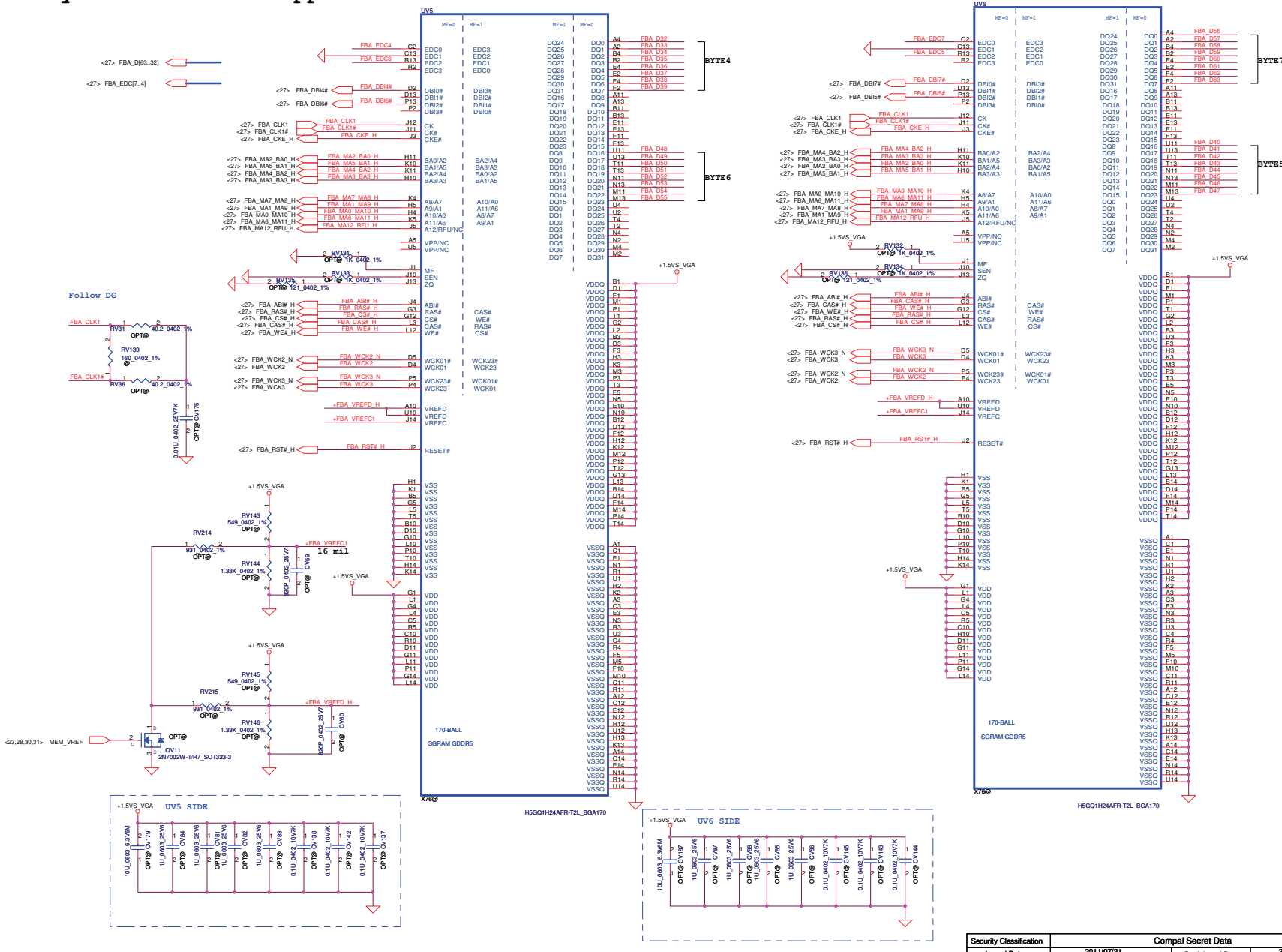
Memory Partition A - Upper 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

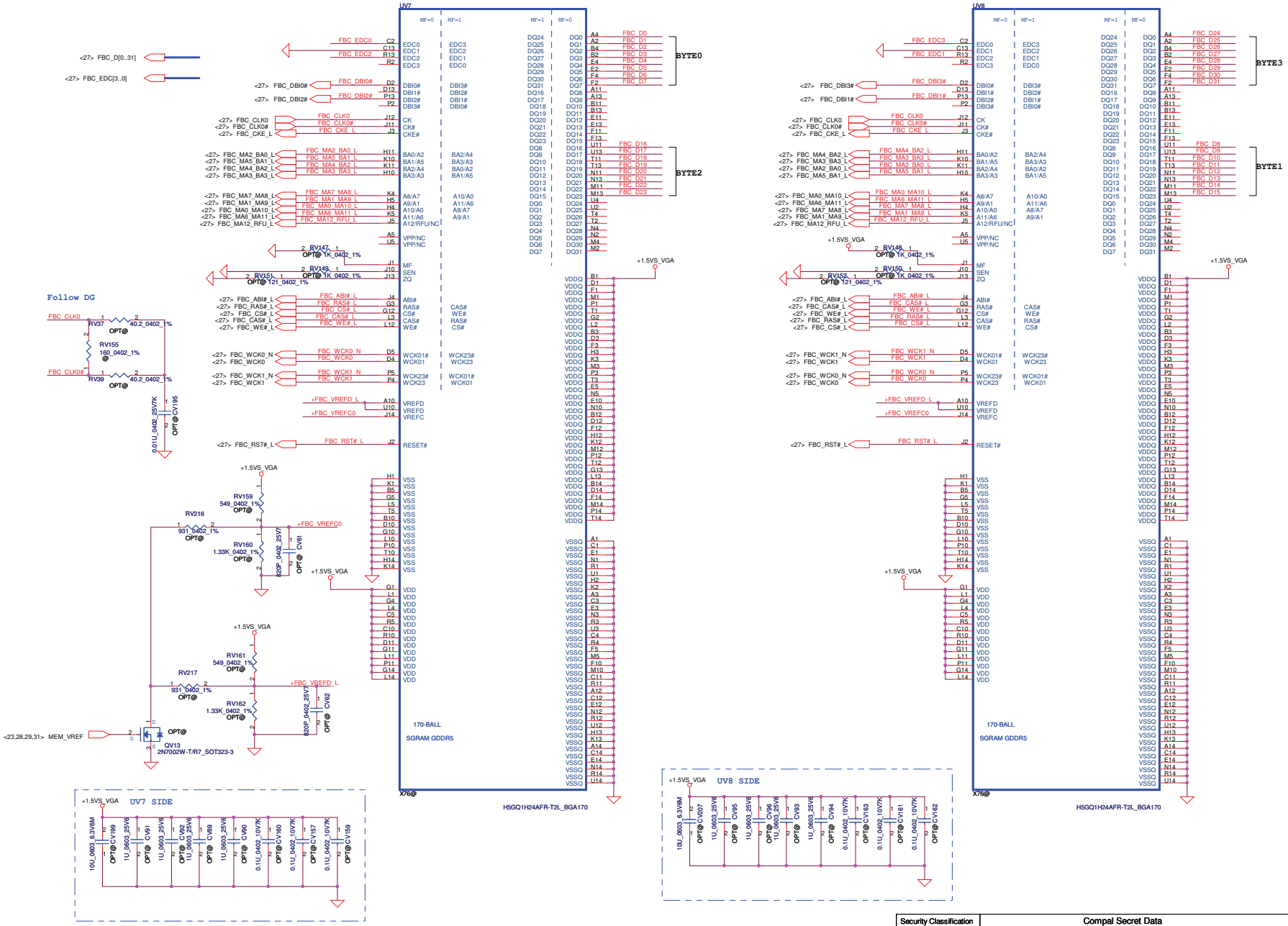
Compal Electronics, Inc.

Title: **N13P-VRAM A Upper**

Size	Document Number	Rev
	QIWY3 LA-8001P	1.0

Date: Monday, January 16, 2012 | Sheet 29 of 64

Memory Partition C - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: NI3P-VRAM C Lower

Size: Custom | Document Number: QIWY3 LA-8001P | Rev: 1.0

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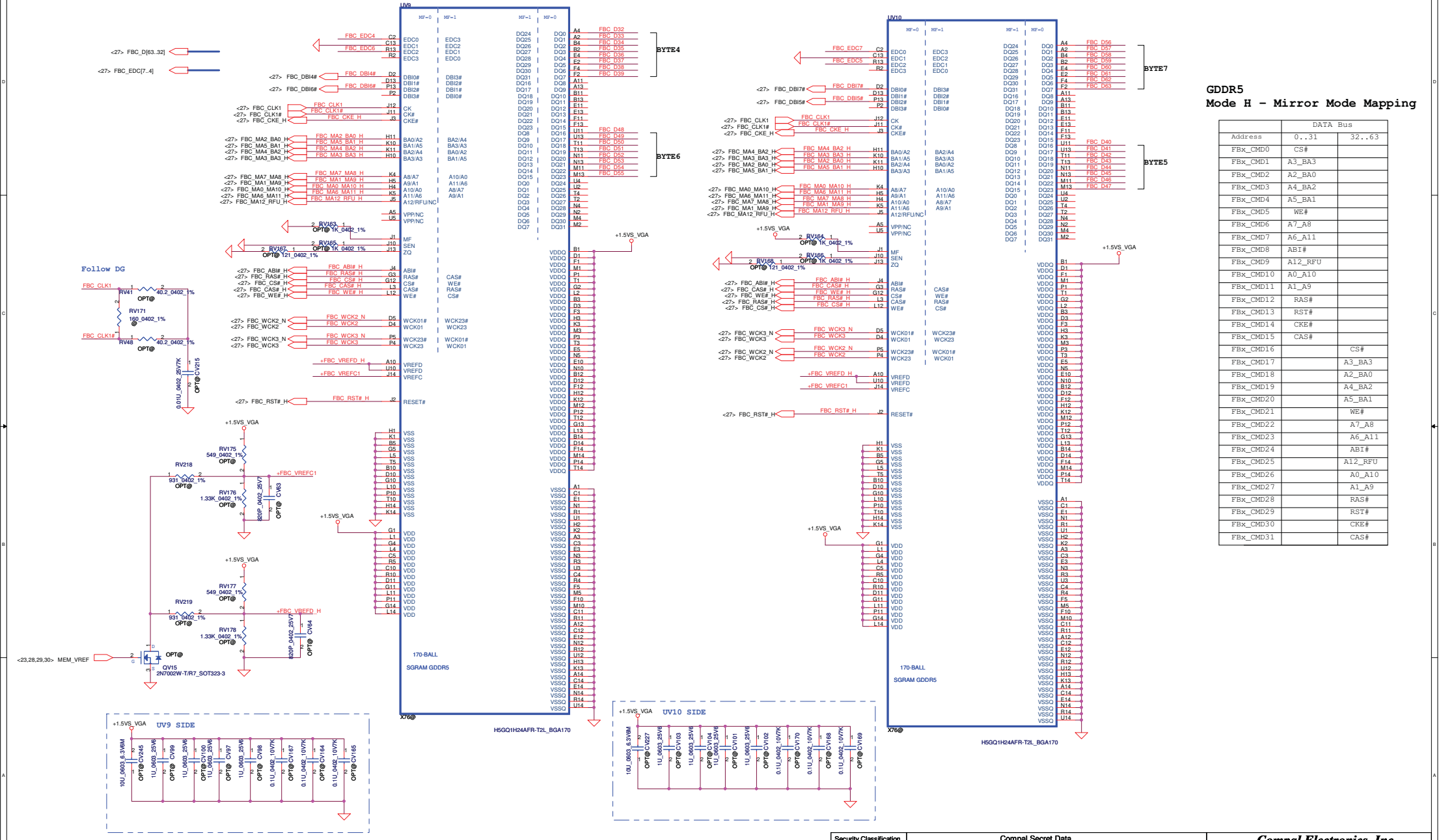
Memory Partition C – Upper 32 bits



GDDR5
Mode H – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Compal Electronics, Inc.

Title: N13P-VRAM C Upper

Size: Custom | Document Number: QIWY3 LA-8001P | Rev: 1.0

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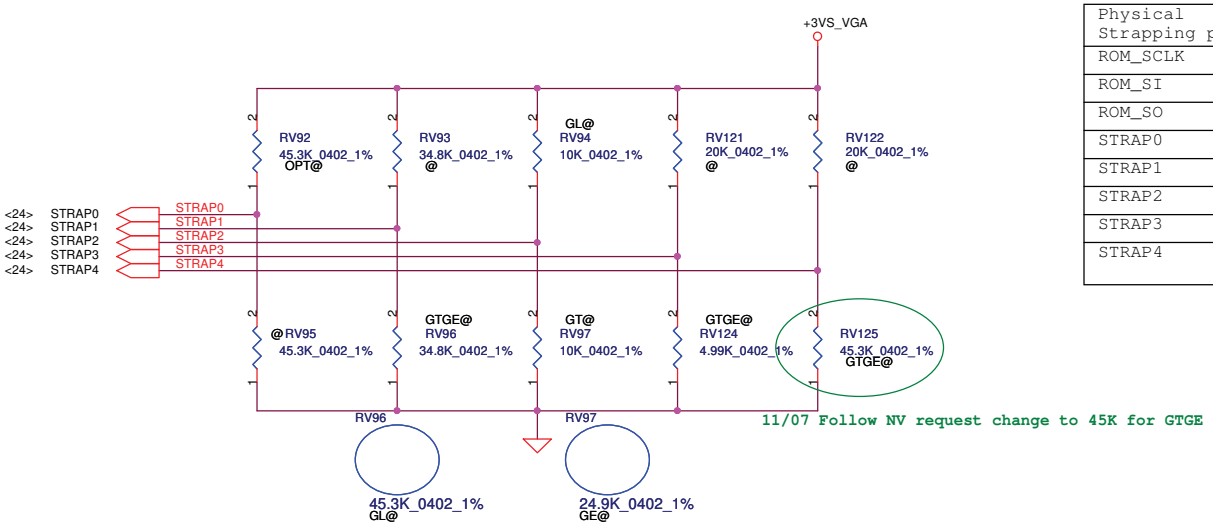
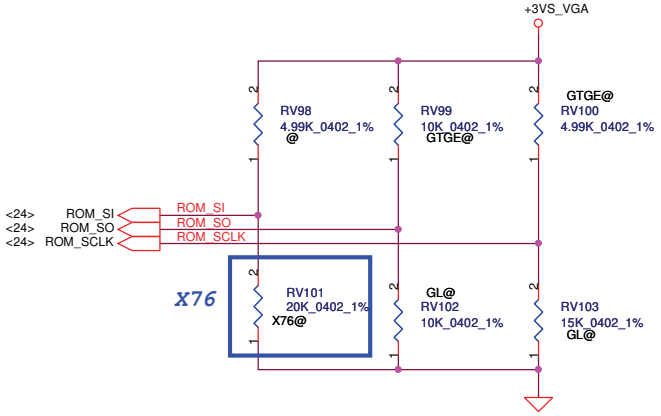


11/07 Follow NV request change to 45K for GTGE



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **N13P_MISC**

Size	Document Number	Rev
Custom	QIWY3 LA-8001P	1.0

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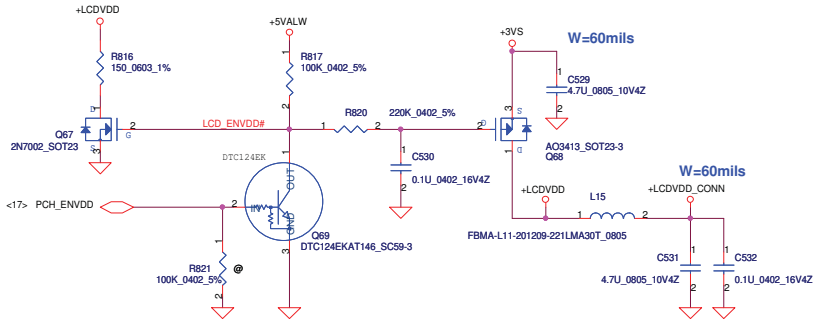
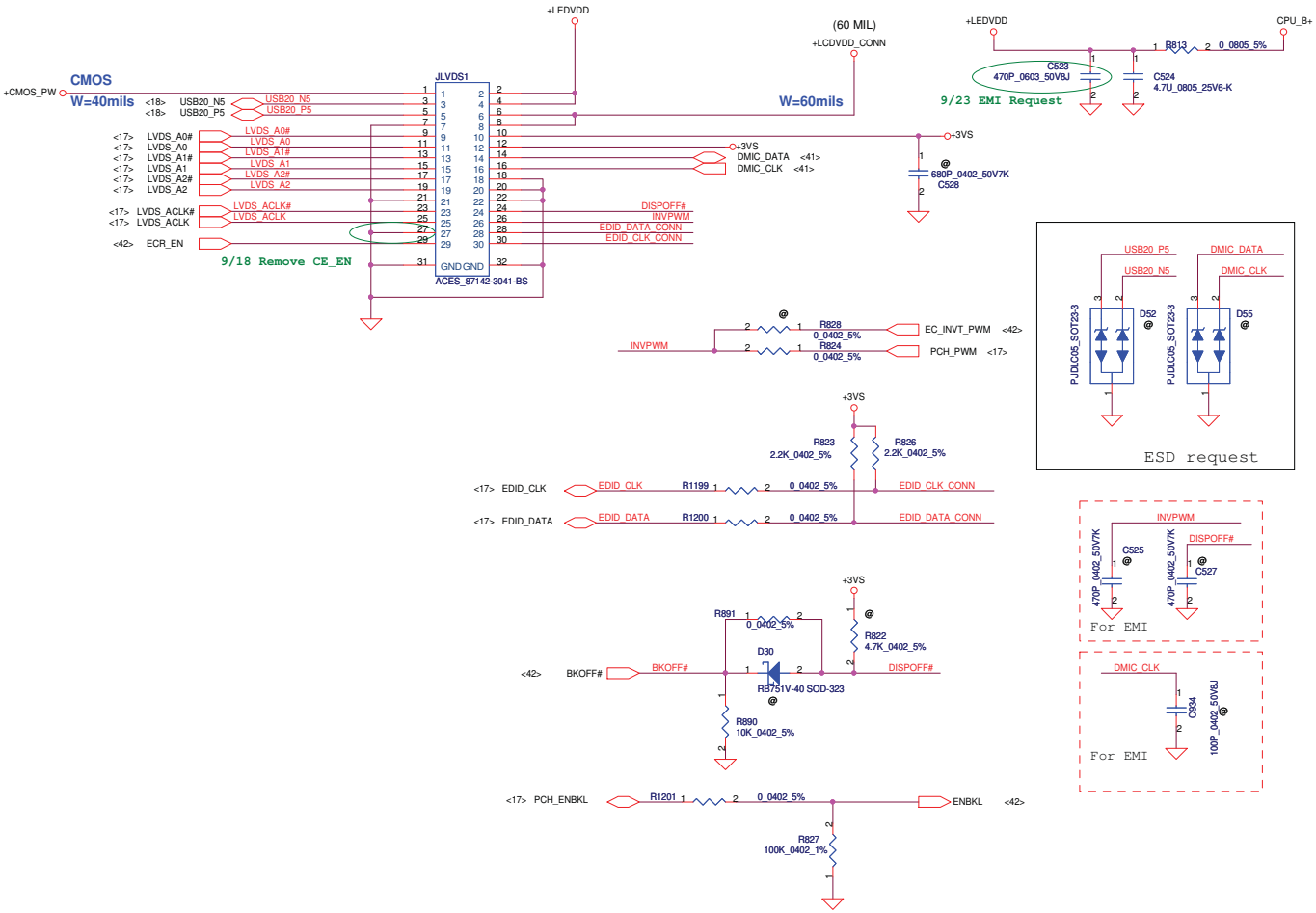
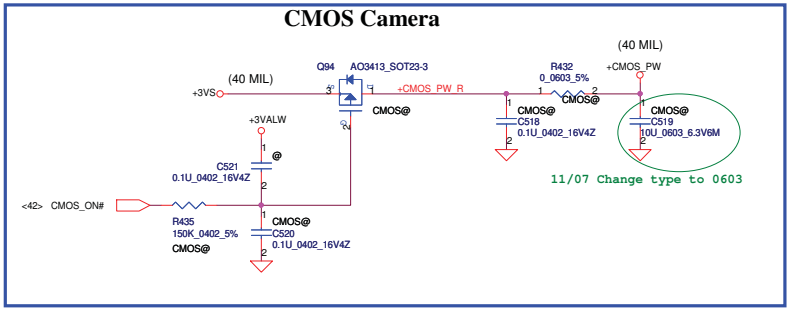






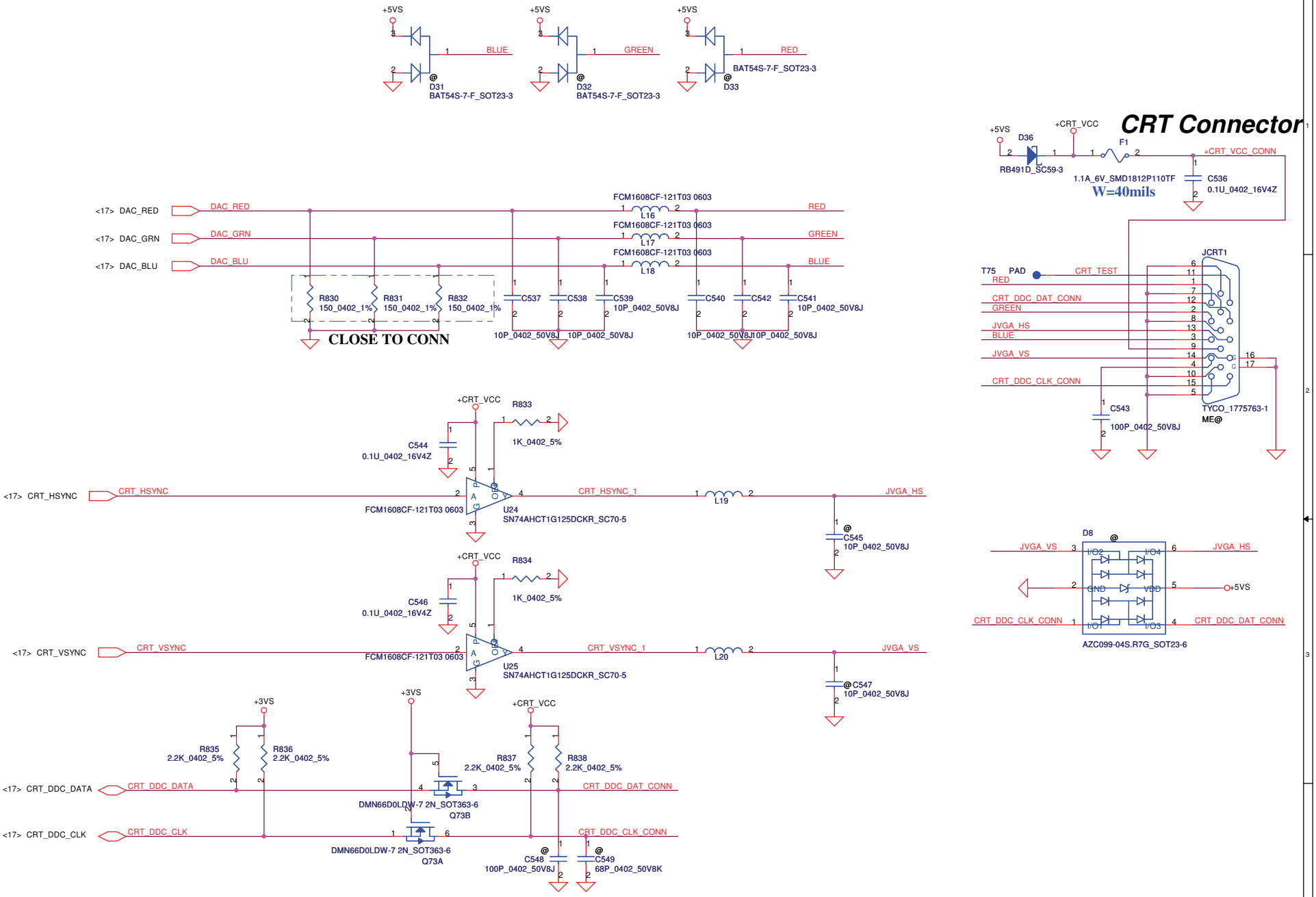
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size	Document Number	Rev
Custom	QIWY3 LA-8001P	1.0

Date: Monday, January 16, 2012 | Sheet 33 of 64



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
Custom	QIWY3 LA-8001P	1.0

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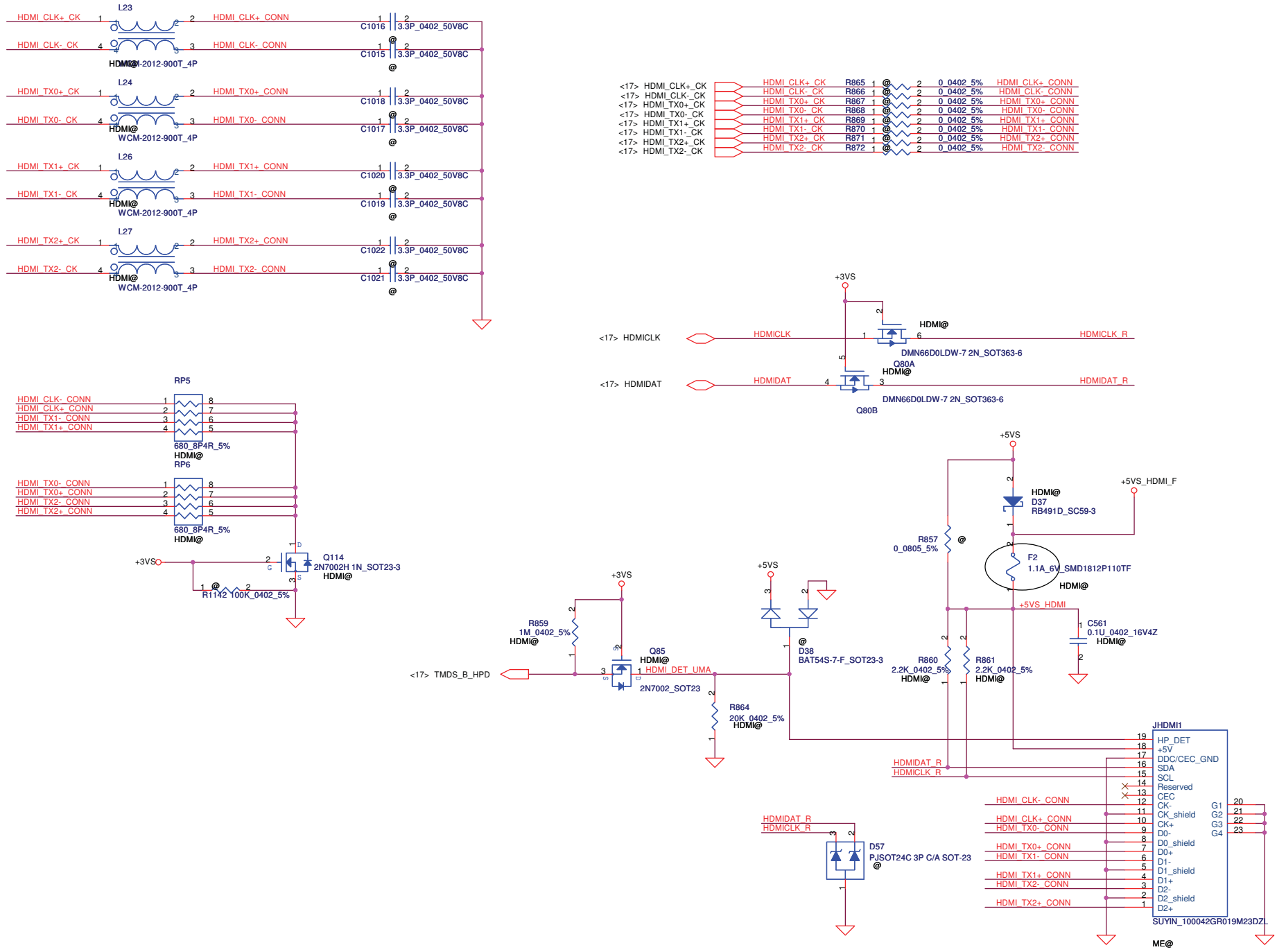

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
Custom	QIWY3 LA-8001P	1.0

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Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R873	@	0 0402 5%	LPC_FRAME#	LPC_FRAME# <14,42>
LPC_AD3 R	R874	@	0 0402 5%	LPC_AD3	LPC_AD3 <14,42>
LPC_AD2 R	R875	@	0 0402 5%	LPC_AD2	LPC_AD2 <14,42>
LPC_AD1 R	R876	@	0 0402 5%	LPC_AD1	LPC_AD1 <14,42>
LPC_AD0 R	R878	@	0 0402 5%	LPC_AD0	LPC_AD0 <14,42>
PCI_RST# R	R879	@	0 0402 5%	PLT_RST#	
CLK_PCI_DB					CLK_PCI_DB <18>

+3VS J3 +3VS_WLAN
JUMP_43X79 @
C563 0.1U_0402_16V4Z
@ C570 10U_0603_6.3V6M
11/08 Reserve

9/18 JP1 Pin2,24,52 contact to +3VS_WLAN for AOAC function

Mini-Express Card(WLAN/WiMAX)

JP1
TAITW_PFPET0-AFGLBG1ZZ4N0
ME@

1	WAKE#	3.3V	2
3	NC	GND	4
5	NC	1.5V	6
7	CLKREQ#	NC	8
9	GND	NC	10
11	REFCLK-	NC	12
13	REFCLK+	NC	14
15	GND	NC	16
17	NC	GND	18
19	NC	NC	20
21	GND	PERST#	22
23	PERn0	+3.3Vaux	24
25	PERp0	GND	26
27	GND	+1.5V	28
29	GND	SMB_CLK	30
31	PETn0	SMB_DATA	32
33	PETp0	GND	34
35	GND	USB_D-	36
37	NC	USB_D+	38
39	NC	GND	40
41	NC	LED_WWAN#	42
43	NC	LED_WLAN#	44
45	NC	LED_WPAN#	46
47	NC	+1.5V	48
49	NC	GND	50
51	NC	+3.3V	52
53	GND	GND	54

<19,44> PCH_BT_ON# — R892 @ 1 2 0 0402 5%
<19> BT_DISABLE — R897 1 2 0 0402 5%
<16,19,37> PCIE_WAKE# / <44> BT_ACTIVE — R877 1 2 @0 0402 5%
PCIE_WAKE# / BT_ACTIVE / BT_DISABLE_R / WLAN_CLKREQ1#
<15> WLAN_CLKREQ1#
<15> CLK_PCIE_WLAN1# / <15> CLK_PCIE_WLAN1
PCI_RST# R / CLK_PCI_DB
<15> PCIE_PRX_DTX_N2 / <15> PCIE_PRX_DTX_P2
<15> PCIE_PTX_C_DRX_N2 / <15> PCIE_PTX_C_DRX_P2
+3VS_WLAN
<42,43> EC_TX / <42,43> EC_RX — EC_TX / EC_RX — R887 100_0402_1% — R888 100_0402_1%
For EC to detect debug card insert.
R889 100K 0402_5%

+3VS_WLAN_AOAC
R289 0_0603_5%
+1.5VS_WLAN
+1.5VS
C564 0.1U_0402_16V4Z
C565 0.1U_0402_16V4Z

LPC_FRAME# R
LPC_AD3 R
LPC_AD2 R
LPC_AD1 R
LPC_AD0 R

R880 1 2 0 0402 5% WL_RST# — PCH_WL_OFF# <18> — 2 0 0402 5% 1 PLT_RST# R1343 — PLT_RST# <18,23,37,42,46>
R881 1 2 @0 0402 5% +3VALW
R882 1 2 0 0402 5% +3VS_WLAN_AOAC
R883 1 2 @0 0402 5% SMB_CLK_S3 <12,13,15>
R884 1 2 @0 0402 5% SMB_DATA_S3 <12,13,15>
USB20_N10 <18>
USB20_P10 <18>

+3VS_WLAN — R267 2 1 0 0603 5% — +3VS_WLAN_AOAC
+3VALW
Q104 AO3413_SOT23-3
AOAC@
AOAC@ C533 0.1U_0402_16V4Z
<42> AOAC_ON# — R436 150K_0402_5% AOAC@ — AOAC@ C526 0.1U_0402_16V4Z

9/18 Increase for Intel AOAC function

Mini-Express Card(SSD)

SSD Active:4.5W(1.5A)

+3VS_SSD
0.1U_0402_16V4Z — C566 — C567 — C568 — @ C569 — 10U_0603_6.3V6M
0.01U_0402_25V7K — 10U_0603_6.3V6M
11/07 Change type to 0603

+3VS J5 +3VS_SSD
JUMP_43X79 @

JP3
TAITW_PFPET0-AFGLBG1ZZ4N0
ME@

1	WAKE#	3.3V	2
3	NC	GND	4
5	NC	1.5V	6
7	CLKREQ#	NC	8
9	GND	NC	10
11	REFCLK-	NC	12
13	REFCLK+	NC	14
15	GND	NC	16
17	NC	GND	18
19	NC	NC	20
21	GND	PERST#	22
23	PERn0	+3.3Vaux	24
25	PERp0	GND	26
27	GND	+1.5V	28
29	GND	SMB_CLK	30
31	PETn0	SMB_DATA	32
33	PETp0	GND	34
35	GND	USB_D-	36
37	NC	USB_D+	38
39	NC	GND	40
41	NC	LED_WWAN#	42
43	NC	LED_WLAN#	44
45	NC	LED_WPAN#	46
47	NC	+1.5V	48
49	NC	GND	50
51	NC	+3.3V	52
53	GND	GND	54

0.01U_0402_16V7K
<14> SATA_DTX_C_IRX_P0 / <14> SATA_DTX_C_IRX_N0 — C572 SATA_DTX_IRX_P0 / C573 SATA_DTX_IRX_N0
0.01U_0402_16V7K
<14> SATA_ITX_DRX_N0 / <14> SATA_ITX_DRX_P0 — SATA_ITX_DRX_N0 / SATA_ITX_DRX_P0
+3VS_SSD
<42,43> EC_TX / <42,43> EC_RX — EC_TX / EC_RX — R893 100_0402_1% — R894 100_0402_1%
<14> SATA_DET# — SATA_DET#
For SSD use:

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **Mini-Card**

Size	Document Number	Rev
	QIWY3 LA-8001P	1.0

Date: Monday, January 16, 2012 Sheet 36 of 64

	LX Voltage <Pin 40>	Configure
AR8151	+1.7V <VDDCT>	R1356,C955
AR8161	+1.1V <DVDDL,AVDDL>	R1357,R1372,L76

+3VALW
+3V_LAN
J18
JUMP_43X79
AO3413_SOT23
Q150
R145
<42> LAN_PWR_ON#
LAN_PWR_ON#
10K_0402_5%
C976
0.1U_0402_16V7K

11/08 Increase for LAN S5 power saving

Layout Notice : Place as close chip as possible.

Close together
+1.7_VDDCT
R1356 8151@0_0402_5%
R1357 8161@0_0402_5%
+1.1_DVDDL
+LX_R
+LX
L74
4.7UH_SIA4012-4R7M_20%
C935 1000P_0402_50V7K
C936 0.1U_0402_16V4Z
C937 10U_0603_6.3V6M
Note: Place Close to LAN chip
L39 DCR< 0.15 ohm
Rate current > 1A
11/07 Change type to 0603
Close to Pin40

L75 FBMA-L11160808601LMA10T_2P
L76 FBMA-L11160808601LMA10T_2P
+1.1_AVDDL_L
+1.1_AVDDL
+1.1_DVDDL
8161@
C967 0.1U_0402_16V4Z
C980 1U_0402_6.3V4Z
C278 4.7U_0603_6.3V6K
Place close to Pin34

Vendor recommand reseve the PU resistor close LAN chip

+3V_LAN
R345 4.7K_0402_5%
<18,23,36,42,46> PLT_RST#
PLT_RST#

Place Close to Chip

U63
Atheros
AR8151/AR8161
AR8161-AL3A-R_QFN40_5X5
SA00003LE20
8151@
8161@

<15> PCIE_PRX_DTX_N1	C946 0.1U_0402_16V7K	PCIE_PRX_C_DTX_N1	29 TX_N
<15> PCIE_PRX_DTX_P1	C947 0.1U_0402_16V7K	PCIE_PRX_C_DTX_P1	30 TX_P
<15> PCIE_PTX_C_DRX_N1			36 RX_N
<15> PCIE_PTX_C_DRX_P1			35 RX_P
<15> CLK_PCIE_LAN#			32 REFCLK_N
<15> CLK_PCIE_LAN			33 REFCLK_P
		PLT_RST#	2 PERST#
<16,19,36> PCIE_WAKE#	R1369 0_0402_5%	PCIE_WAKE#_R	3 WAKE#
<42> LAN_WAKE#	R1370 0_0402_5%		
			25 SMCLK
			26 SMDATA
+3V_LAN	R343 4.7K_0402_5% BOM Structure CDH@		
			28 NC
			27 TESTMODE
		LAN_XTALO	7 XTLO
		LAN_XTALI	8 XTLI
+3V_LAN	R344 4.7K_0402_5%		
<15> CLKREQ_LAN#			4 CLKREQ#
			41 GND

Vendor recommand reseve the PU resistor close LAN chip

LED_0	38	ACTIVITY
LED_1	39	LAN_LINK#
LED_2	23	
TRXN0	12	MDI0-
TRXP0	11	MDI0+
TRXN1	15	MDI1-
TRXP1	14	MDI1+
TRXN2	18	MDI2-
TRXP2	17	MDI2+
TRXN3	21	MDI3-
TRXP3	20	MDI3+
RBIAS	10	LAN_RBIAS R1371 2.37K_0402_1%
VDD33	1	+3V_LAN
LX	40	+LX
VDDCT/ISOLAN	5	+1.7_VDDCT
DVDDL/PPS DVDDL_REG/DVDDL	24	+1.1_DVDDL_R R1366 0_0402_5% +1.1_DVDDL
	37	+1.1_DVDDL
AVDDH/AVDD33 AVDDH AVDDH_REG	16	+AVDDH_AVDD3.3
	22	+2.7_AVDDH
	9	+2.7_AVDDH
	13	+1.1_AVDDL AVDDL
	19	+1.1_AVDDL AVDDL
	31	+1.1_AVDDL AVDDL
	34	+1.1_AVDDL_L AVDDL
	6	+1.1_AVDDL AVDDL_REG/AVDDL

H --> Overclocking mode
L --> Not overclocking mode
R31 10K_0402_5%
ACTIVITY <38>
LAN_LINK# <38>
MDI0- <38>
MDI0+ <38>
MDI1- <38>
MDI1+ <38>
MDI2- <38>
MDI2+ <38>
MDI3- <38>
MDI3+ <38>
Place Close to PIN1
R1372 8161@ 30K_0402_5%
+3VS
C955 0.1U_0402_16V4Z
1000P_0402_50V7K
C850 0.1U_0402_16V4Z
C851 1U_0402_6.3V4Z
C852 10U_0603_6.3V6M
C853 10U_0603_6.3V6M
C954
11/07 Change type to 0603

C956 C957 C958 C959 C960 C961 C962 C963 C964 C965 C966
0.1U_0402_16V4Z
1U_0402_6.3V4Z
Near Pin13
Near Pin19
Near Pin31
Near Pin6
Near Pin9
Near Pin22
Near Pin37
Near Pin24
8151@
For AR8151: Stuff C966,R1366
For AR8161: NC

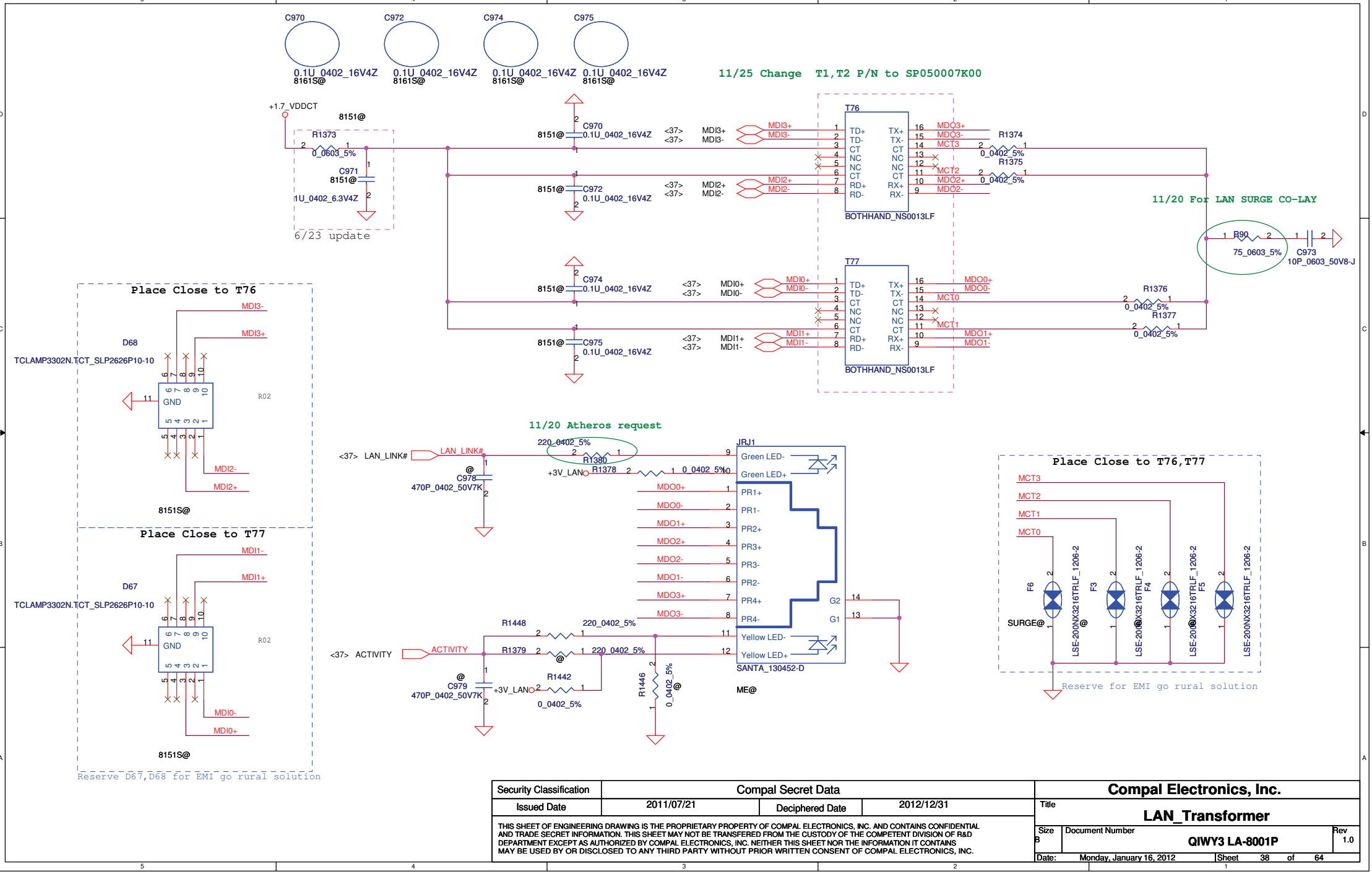
<15> PCH_LAN_48M
C981 3.3P_0402_50V8
Place Close to C968
Y6
25MHZ_12PF_X3G025000DC1H~D
C968 C969 33P_0402_50V8J
9/20 For Crystal EA request

Place Close to LAN chip
MDI0+ R1358 8151@ 49.9_0402_1%
MDI0- R1359 8151@ 49.9_0402_1%
MDI1+ R1360 8151@ 49.9_0402_1%
MDI1- R1361 8151@ 49.9_0402_1%
MDI2+ R1362 8151@ 49.9_0402_1%
MDI2- R1363 8151@ 49.9_0402_1%
MDI3+ R1364 8151@ 49.9_0402_1%
MDI3- R1365 8151@ 49.9_0402_1%
C938 C939 C940 C941 C942 C943 C944 C945
1000P_0402_50V7K
0.1U_0402_16V4Z
Note : C938, C940, C942, 944, reserved for EMI.
For AR8151: Stuff 49.9K and 0.1u
For AR8161: NC

+3V_LAN
+2.7_AVDDH
+AVDDH_AVDD3.3
R1367 8161@ 0_0402_5%
R1368 8151@ 0_0402_5%
C948 0.1U_0402_16V4Z
C949 1U_0402_6.3V4Z
Place close to Pin16
For AR8151: Stuff R1368 for +AVDD3.3
For AR8161: Stuff R1367,C949 for +AVDDH

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	LAN-AR8151/8161		
Size Custom	Document Number QIWY3 LA-8001P		Rev 1.0
Date: Monday, January 16, 2012	Sheet 37 of 64		



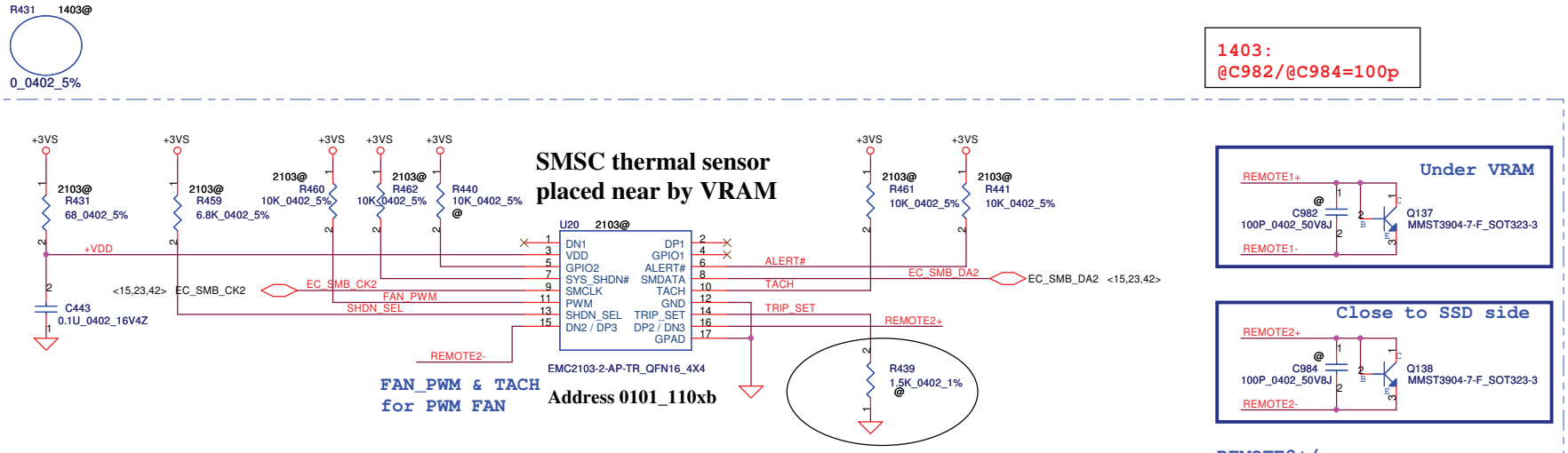
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

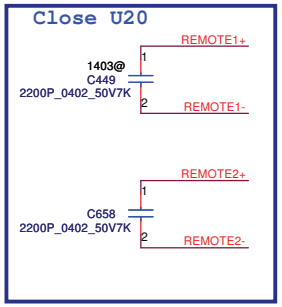
Compal Electronics, Inc.

Title: **LAN_Transformer**

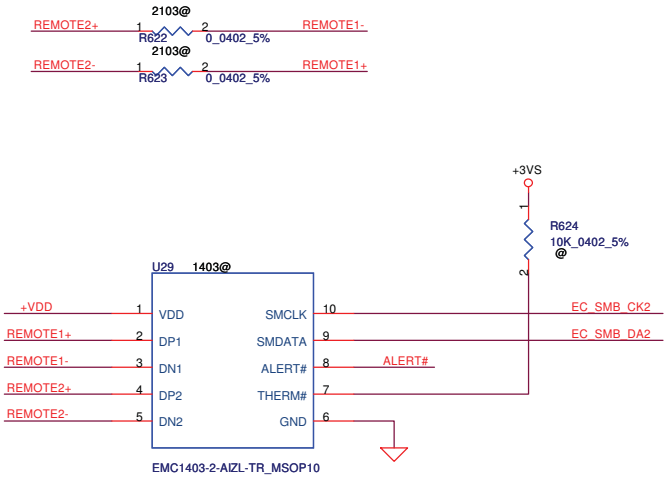
Size	Document Number	Rev
B	QIWY3 LA-8001P	1.0

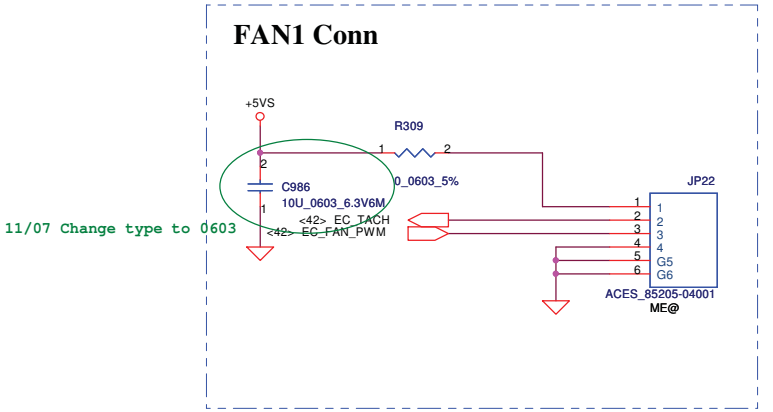
Date: Monday, January 16, 2012 Sheet 38 of 64





Shutdown Temp	TRIP_SET R1387(1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm





Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

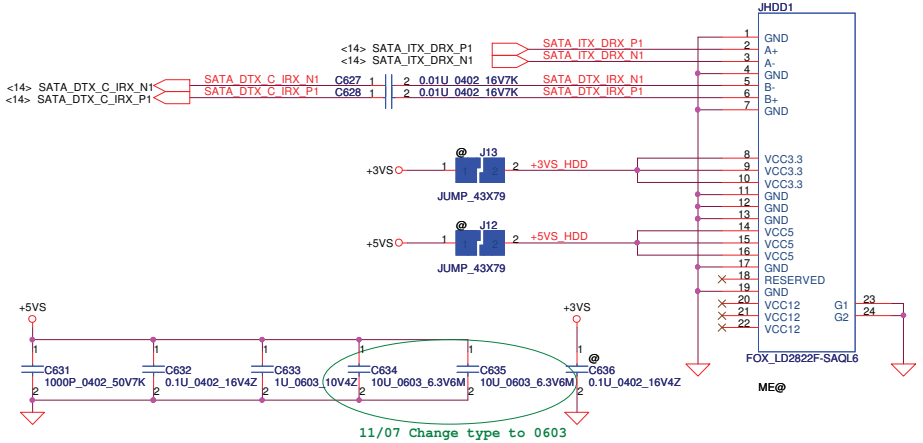
Compal Electronics,Ltd.

Title: EMC1403/2103_Thermal sensor/FAN

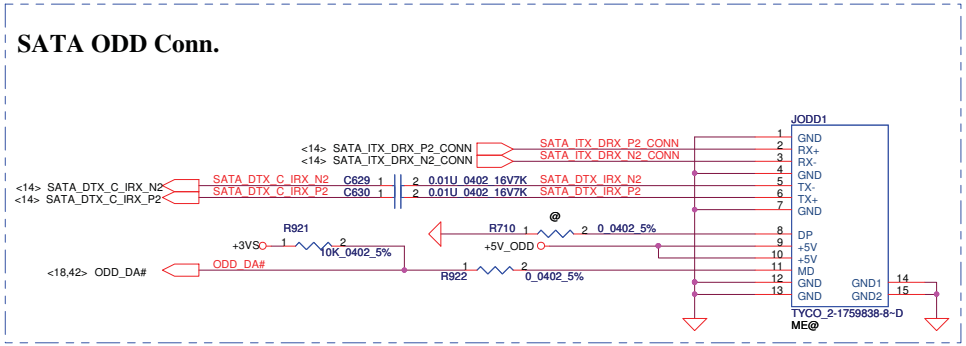
Size: Custom | Document Number: QIWY3 LA-8001P | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 39 of 64

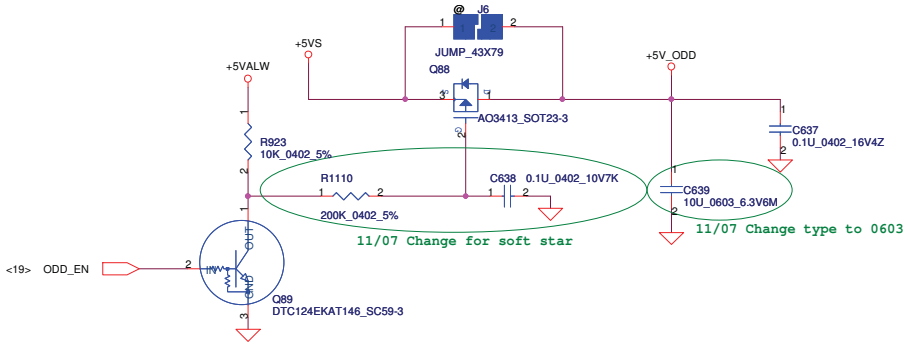
SATA HDD Conn.



SATA ODD Conn.

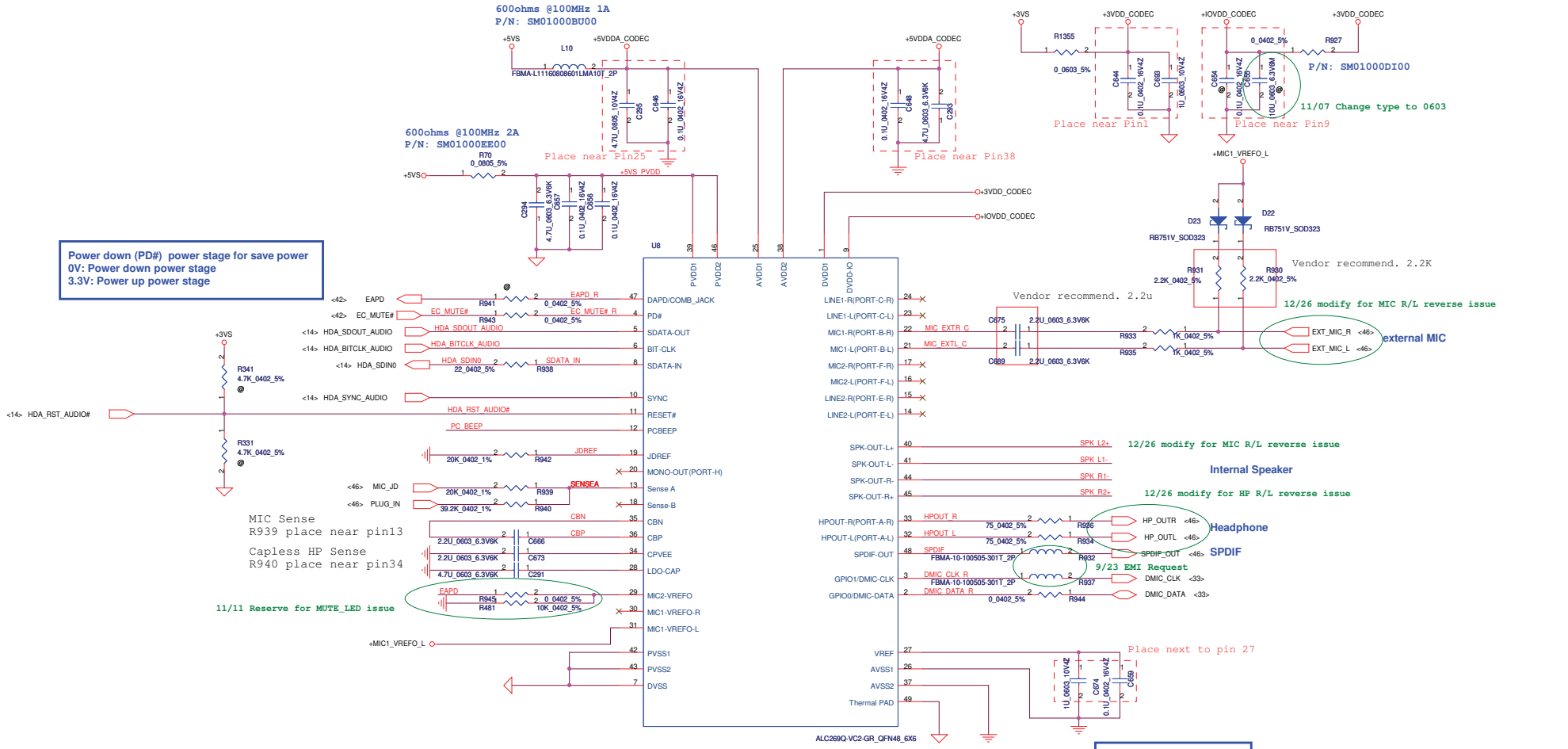


ODD Power Control

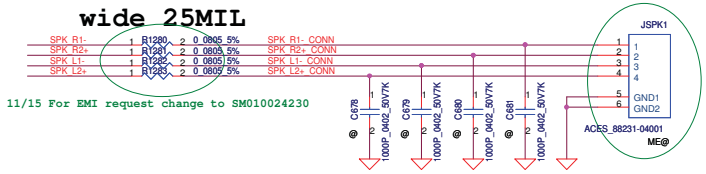


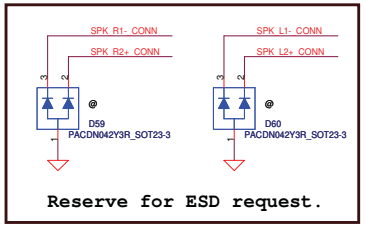
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

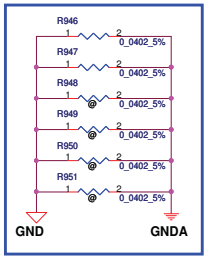
Compal Electronics, Inc.	
Title	HDD/ODD Connector
Size B	Document Number QIWY3 LA-8001P
Rev	1.0
Date: Monday, January 16, 2012	Sheet 40 of 64

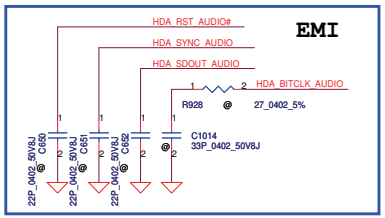


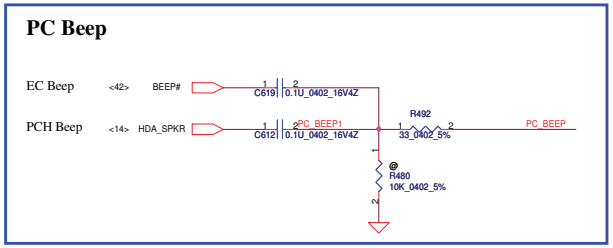
Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in











Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

Title: HD Audio Codec_ALC269Q-VC

Size: C | Document Number: QIWY3 LA-8001P | Rev: 1.0

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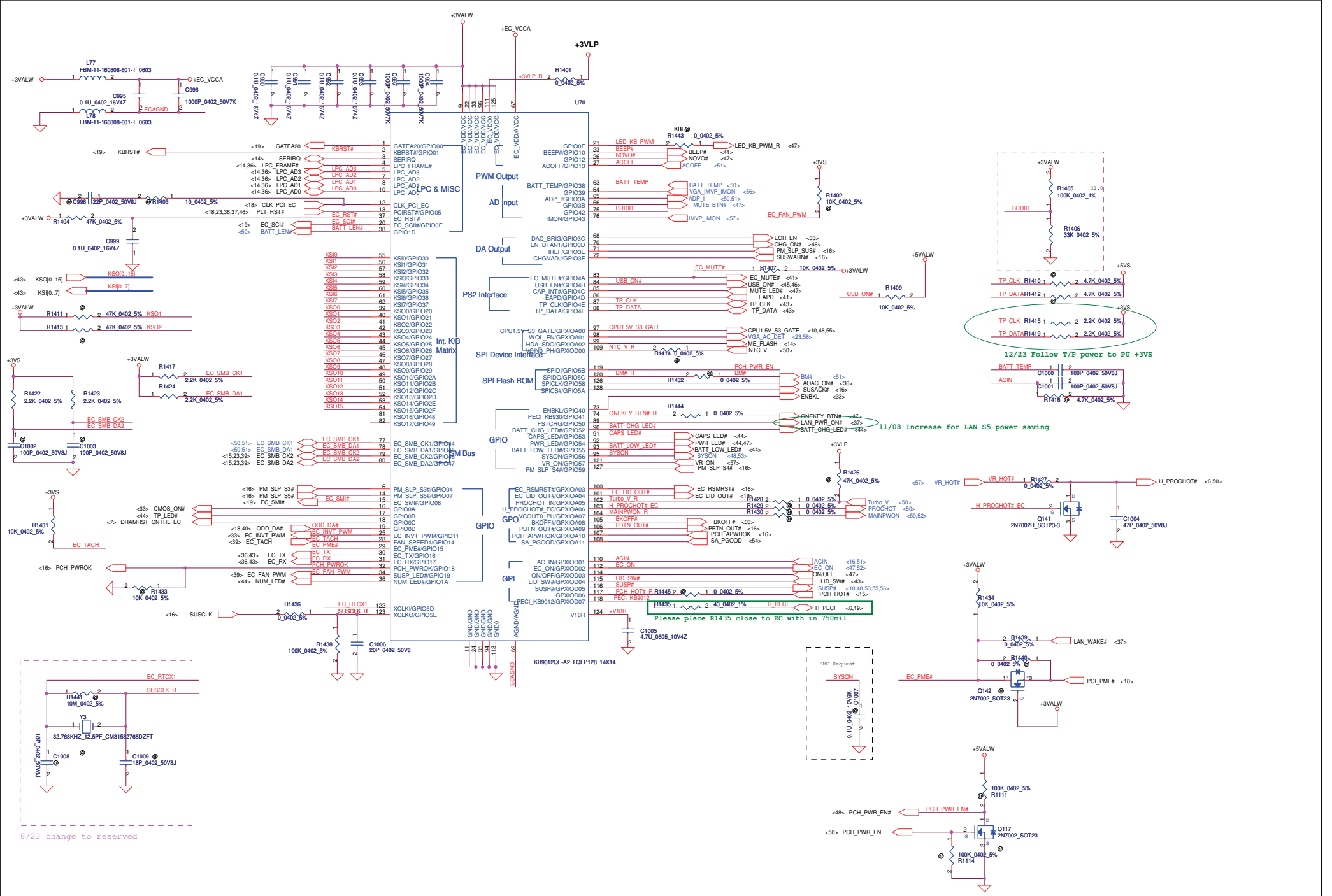

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
C	QIWY3 LA-8001P	1.0

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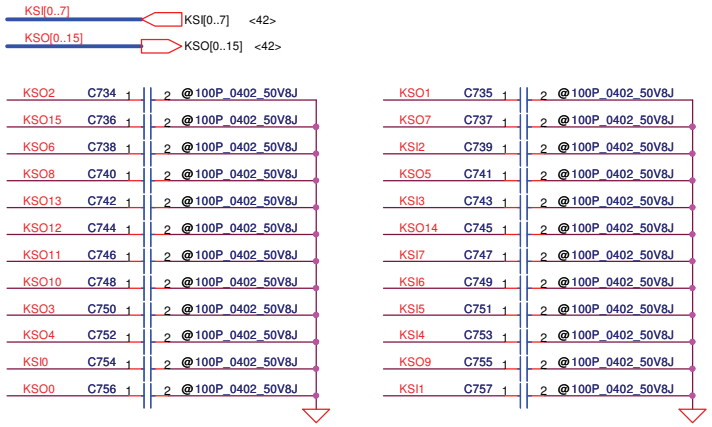
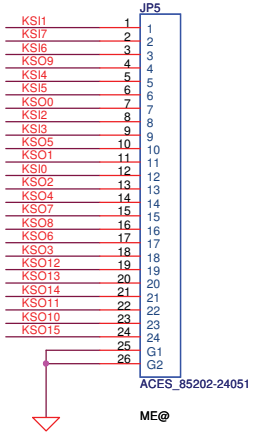
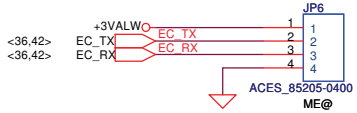
INT_KBD Conn.



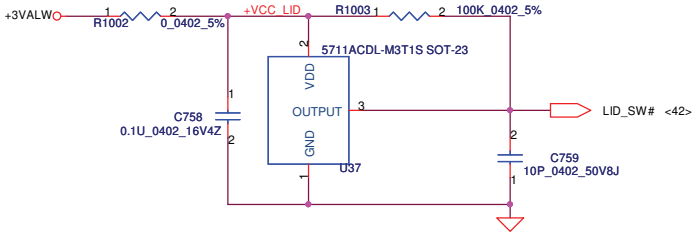
CONN PIN define need double check



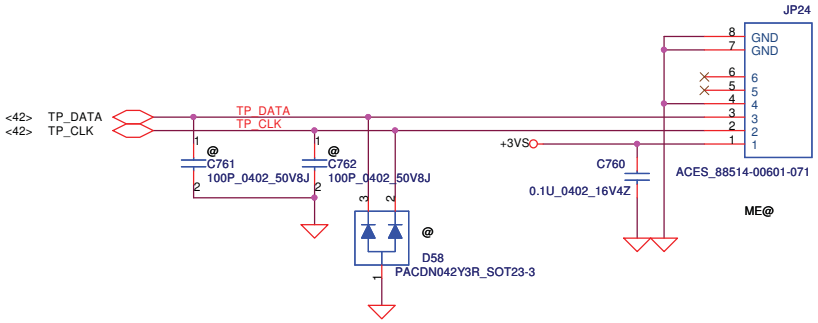
EC DEBUG PORT



Lid Switch



To TP/B Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **KB /SW /LPC Debug Conn.**

Size	Document Number	Rev
B	QIWY3 LA-8001P	1.0

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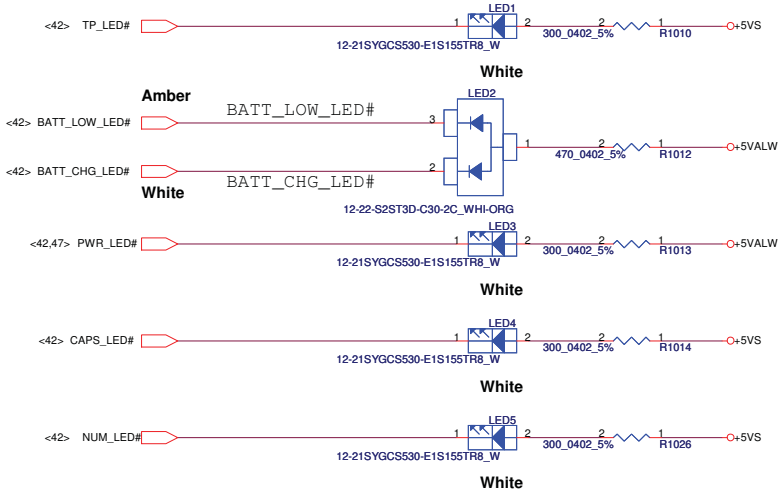
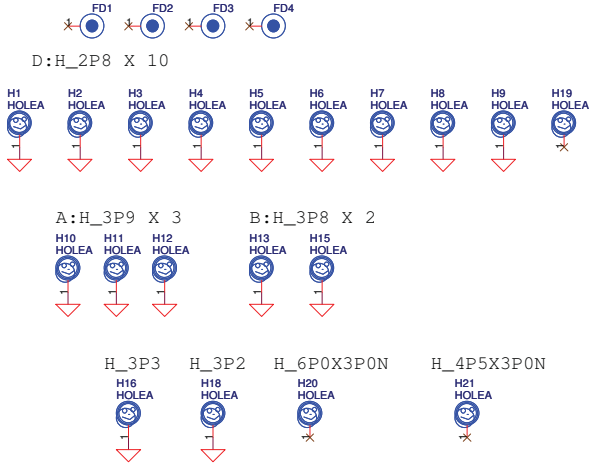
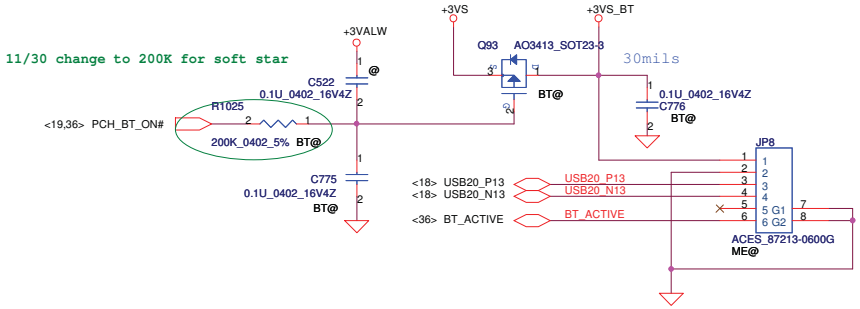
LED





BT MODULE CONN



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: LED/EC SPI ROM/BT

Size	Document Number	Rev
B	QIWY3 LA-8001P	1.0

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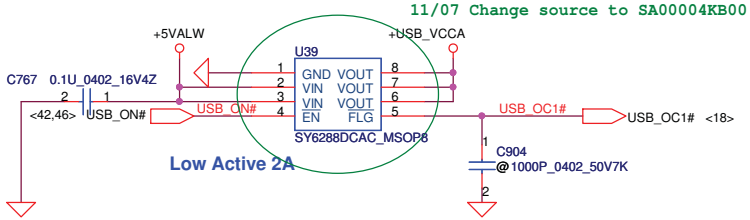
LEFT SIDE USB3.0 PORT X2

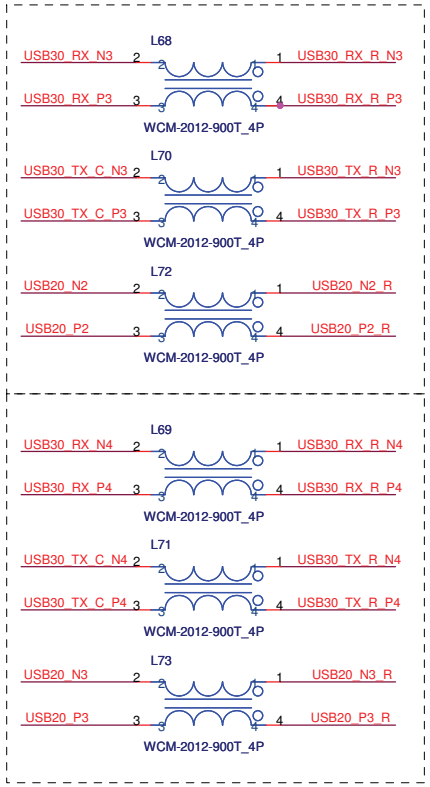
11/07 Change source to SA00004KB00

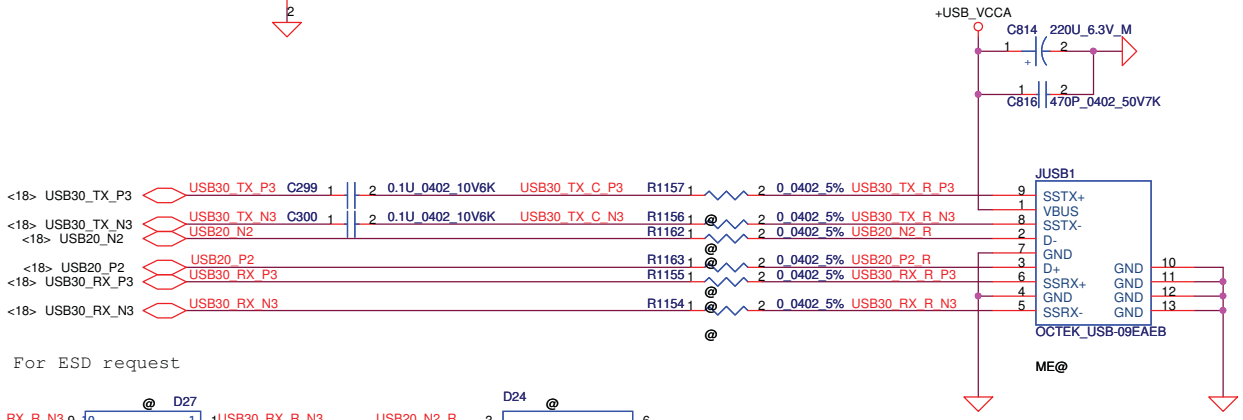


For EMI request

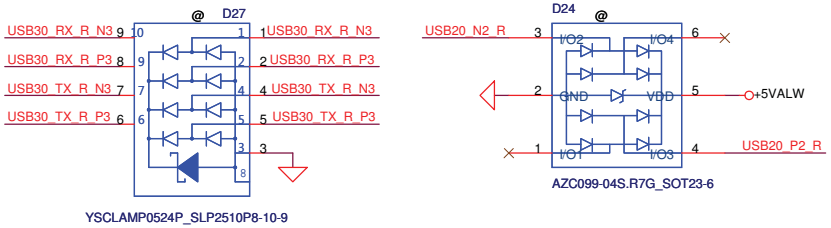
USB2.0 choke --> SM070000I00

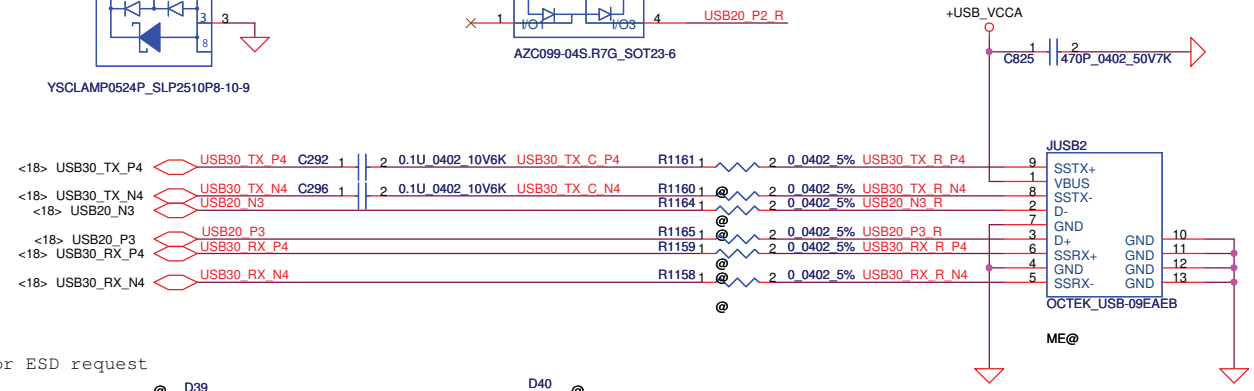
USB3.0 Choke --> SM070001U00



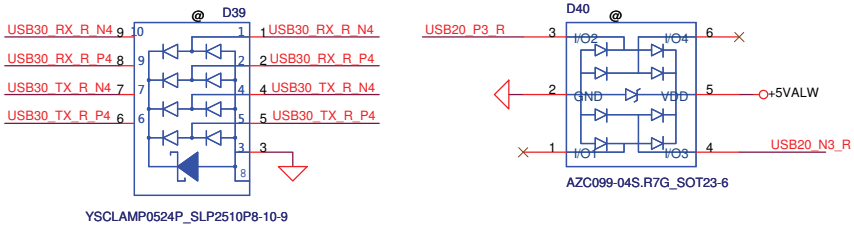


For ESD request





For ESD request



Security Classification	Compal Secret Data For EMI request		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **USB3.0 ports**

Size	Document Number	Rev
Custom	QIWY3 LA-8001P	1.0

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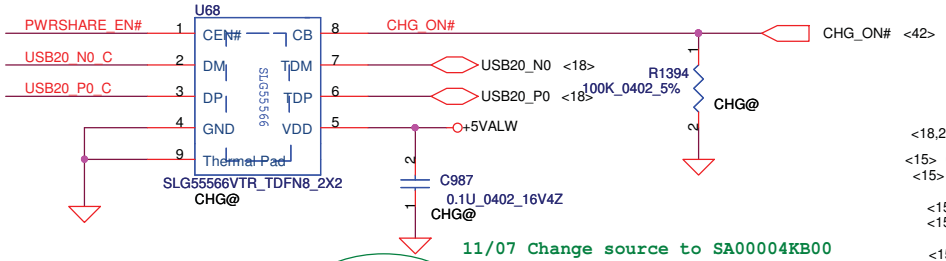
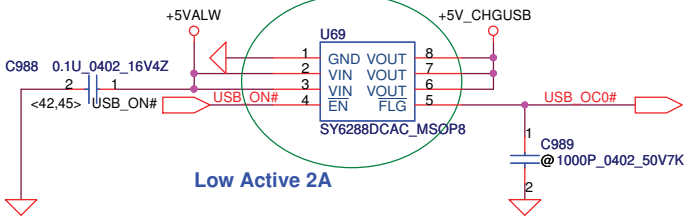
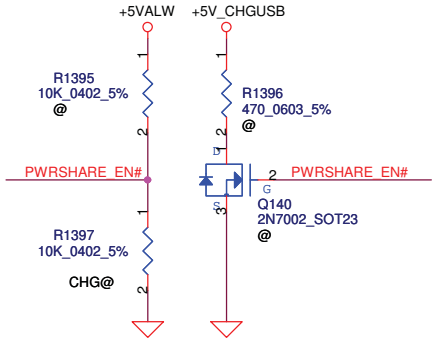
Right side USB Charger

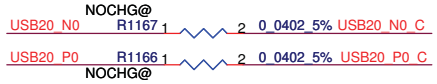


11/07 Change source to SA00004KB00



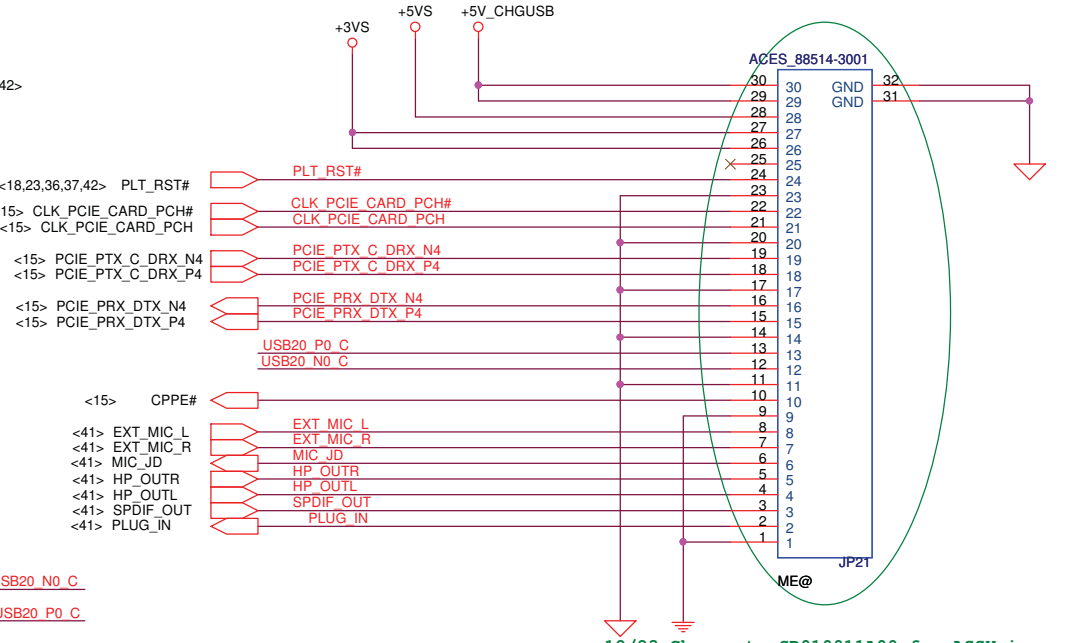
Low Active 2A





CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM

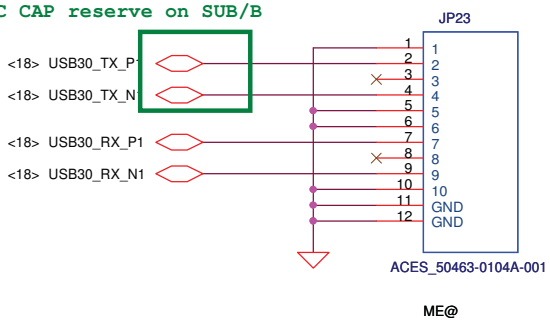
USB2.0/3.0 choke and ESD diode at sub-B.



12/23 Change to SP010011A00 for ASSY issue

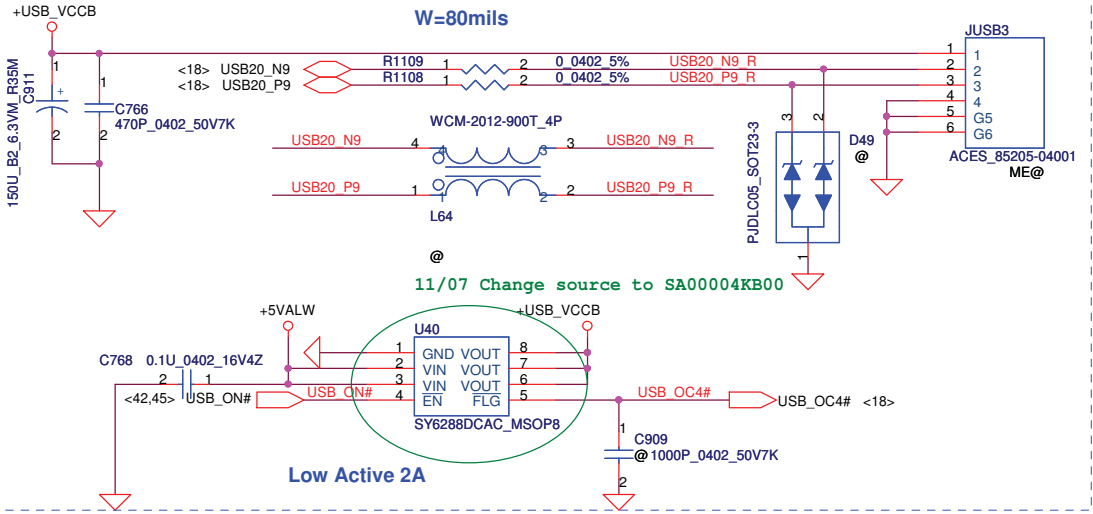
Right side USB3.0 port (Option)

AC CAP reserve on SUB/B



Right USB Conn.(Cable)

W=80mils



Low Active 2A

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **Audio B Conn/USB charger**

Size	Document Number	Rev
Custom	QIWY3 LA-8001P	1.0

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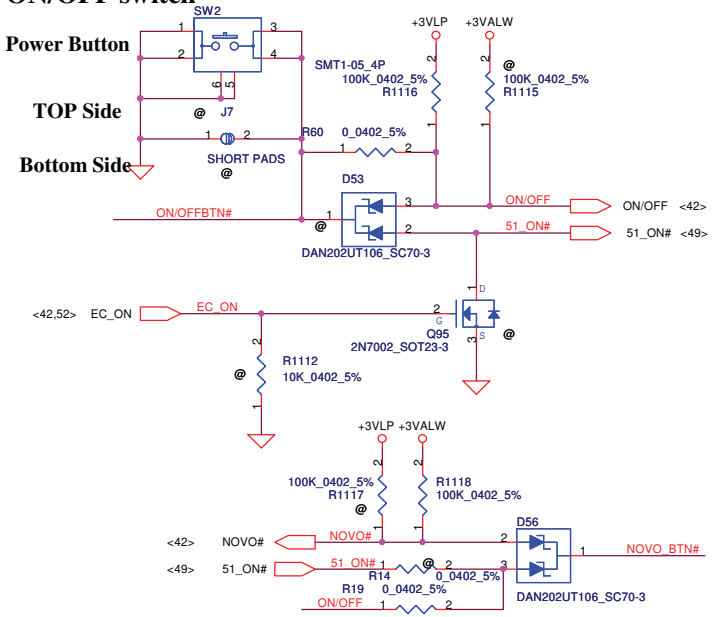
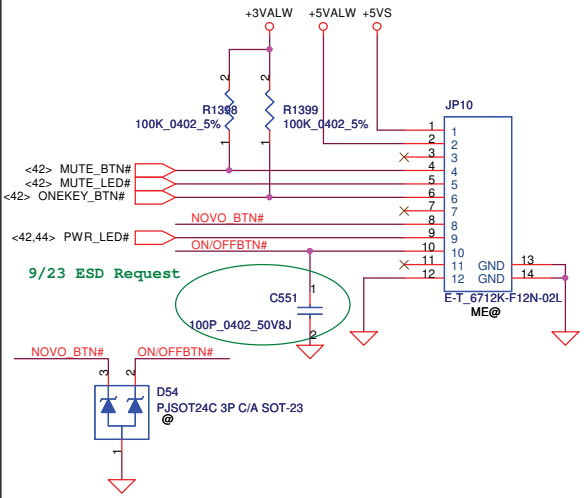
ON/OFF switch

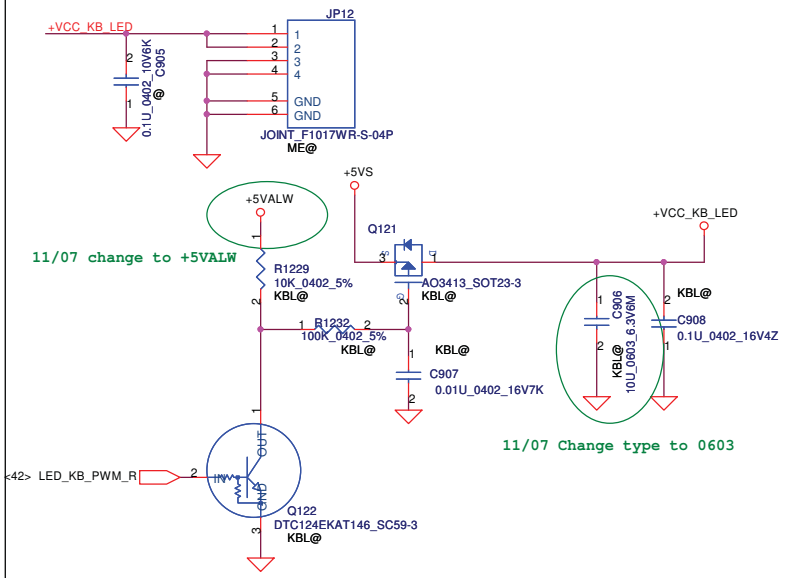


Power Button/B link to Function/B Conn. 10pin



EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

KB Lighting CONN.4pin



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

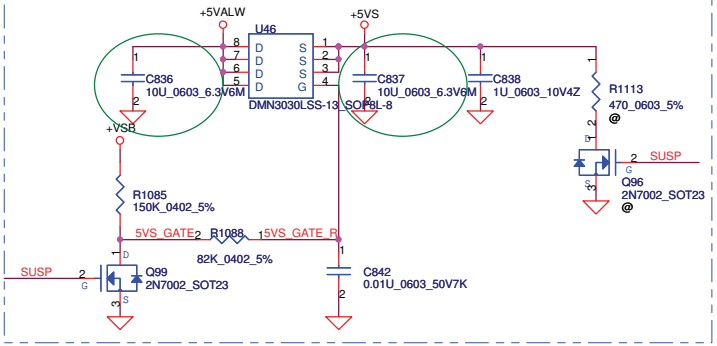
Title: *other IO connector*

Size	Document Number	Rev
Custom	*QIWY3 LA-8001P*	1.0

Date: Monday, January 16, 2012 Sheet 47 of 64

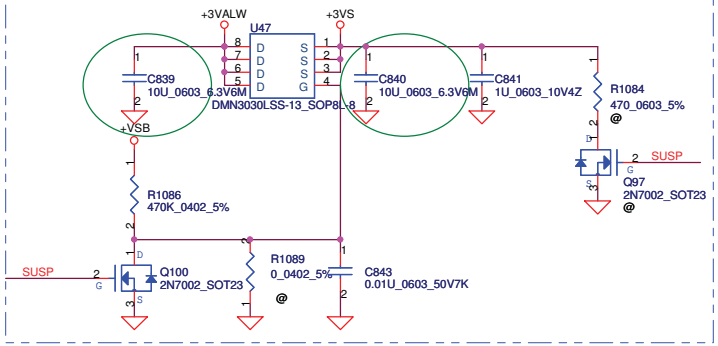
+5VALW TO +5VS

11/07 Change type to 0603



+3VALW TO +3VS

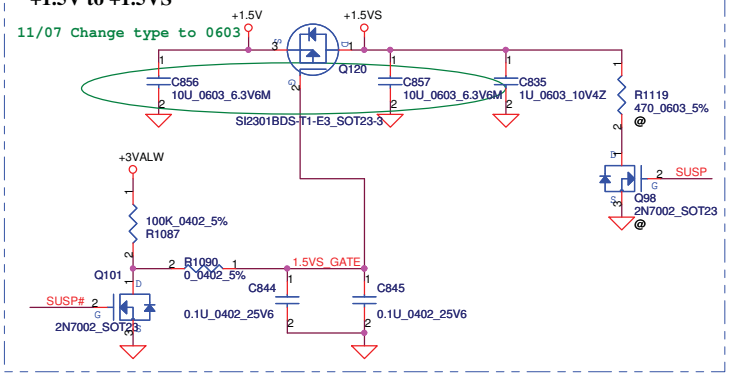
11/07 Change type to 0603



+1.5V to +1.5VS

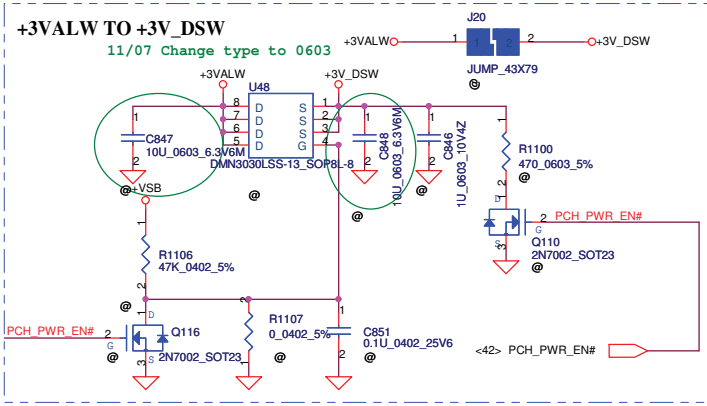
7/26 change SI4800 to SI2301

11/07 Change type to 0603

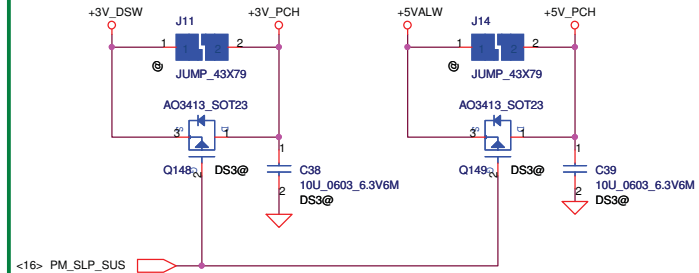


+3VALW TO +3V_DSW

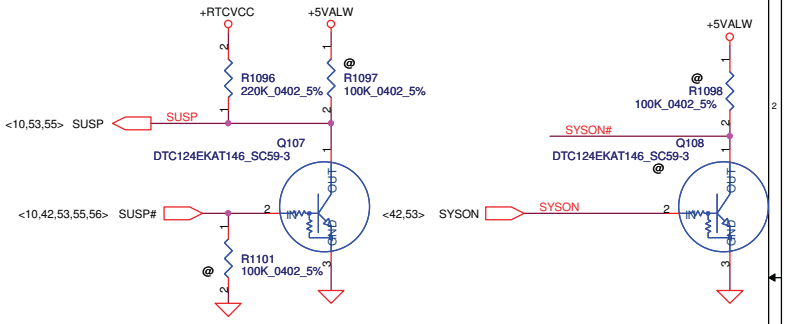
11/07 Change type to 0603



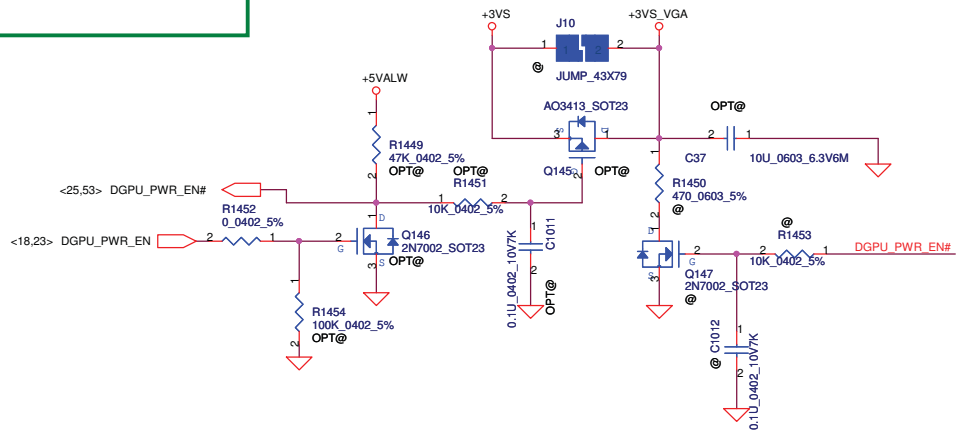
+3V_DSW to +3V_PCH +5VALW to +5V_PCH

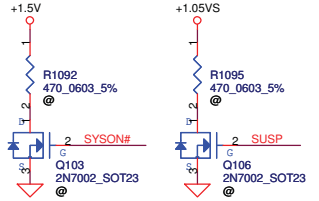


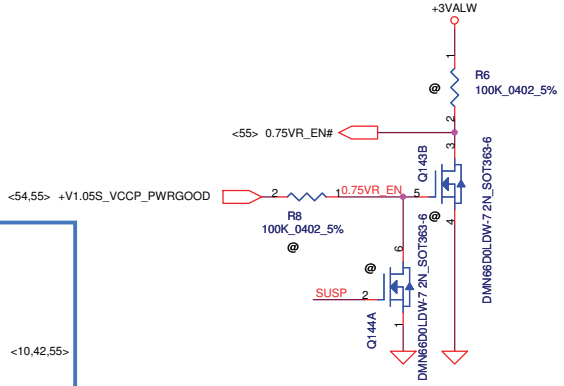
09/05 add for Deep S3

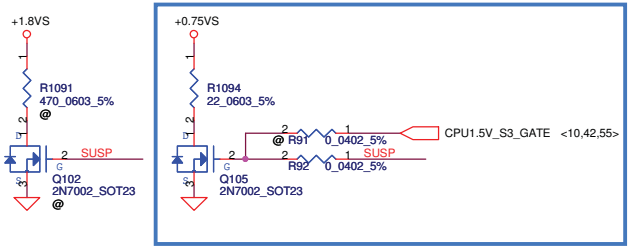


+3VS to +3VS_VGA









For Intel S3 Power Reduction.

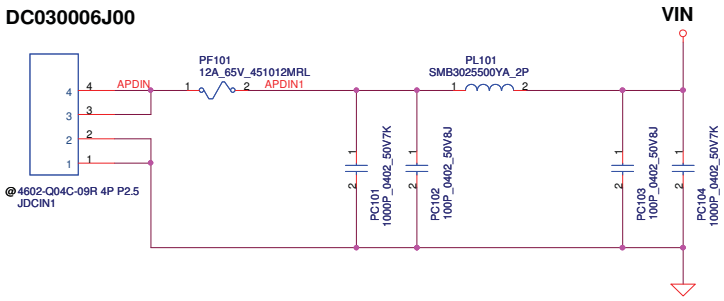
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

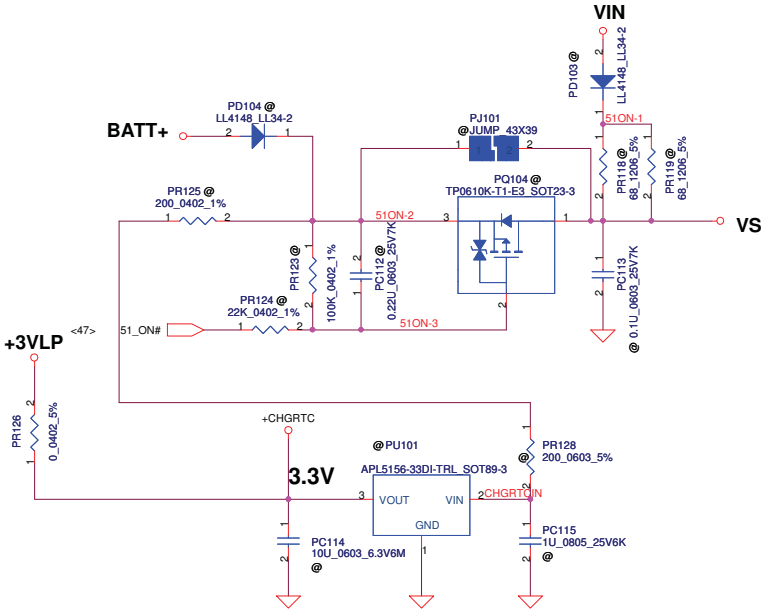
Compal Electronics, Inc.

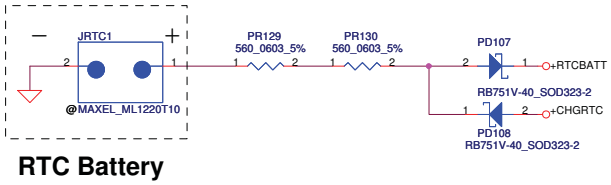
Title: **DC Interface**

Size	Document Number	Rev
Custom	QIWY3 LA-8001P	1.0

Date: Monday, January 16, 2012 | Sheet 48 of 64







RTC Battery

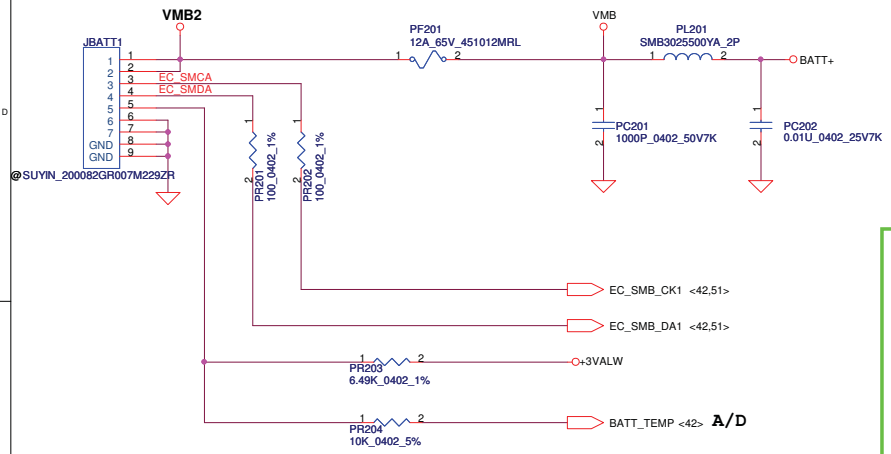
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

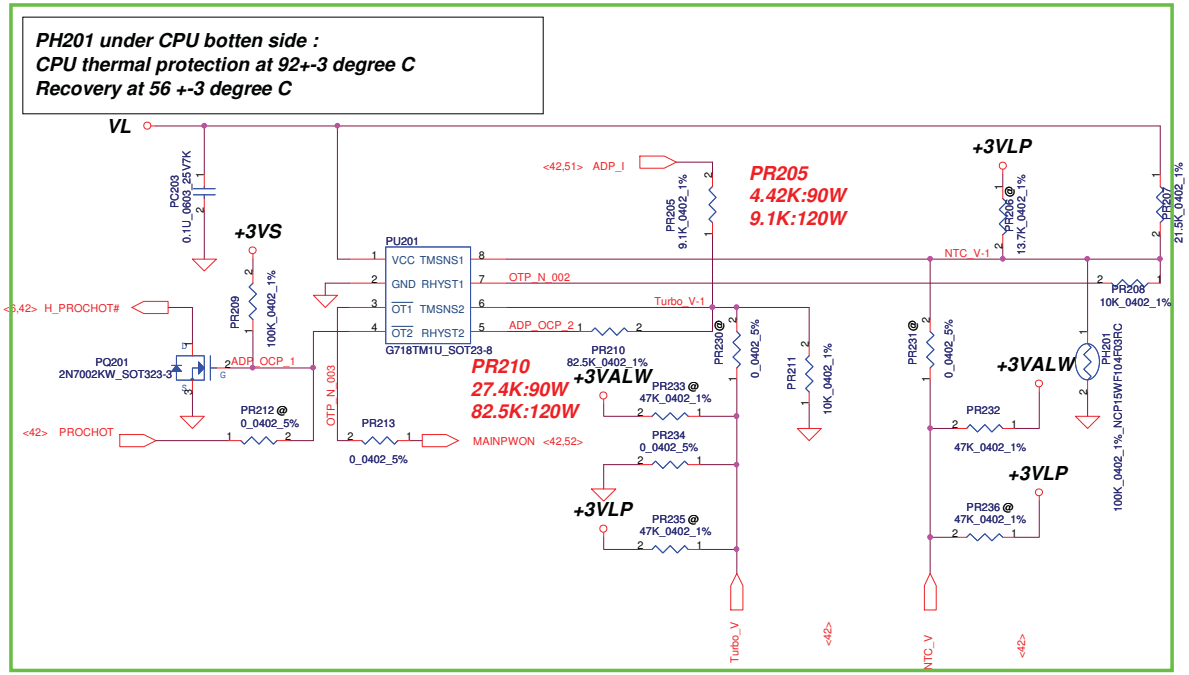
Compal Electronics, Inc.

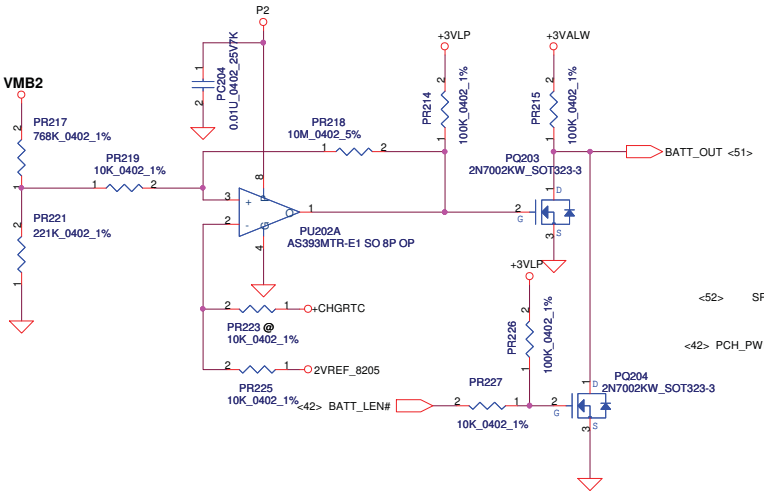
Title: Vin Detector

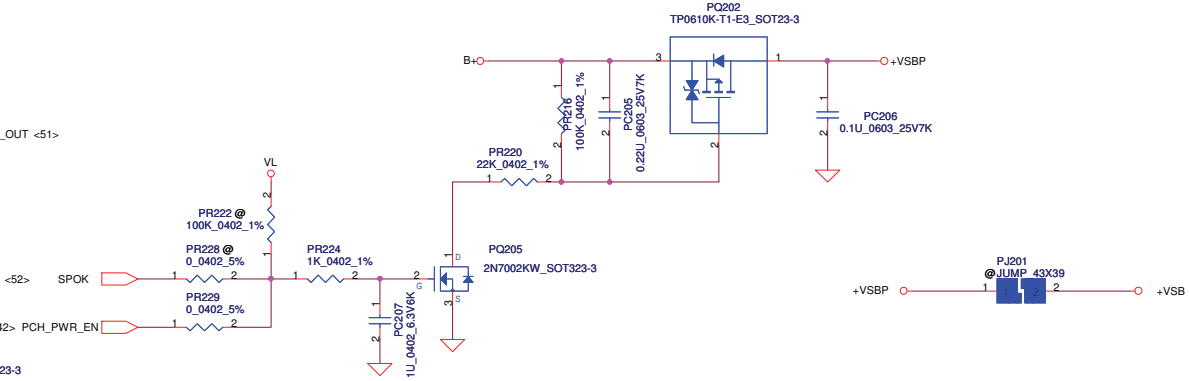
Size: Custom | Document Number: QIWY3 | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 49 of 64









Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: BATTERY CONN/OTP

Size	Document Number	Rev
Custom	QIWY3	1.0

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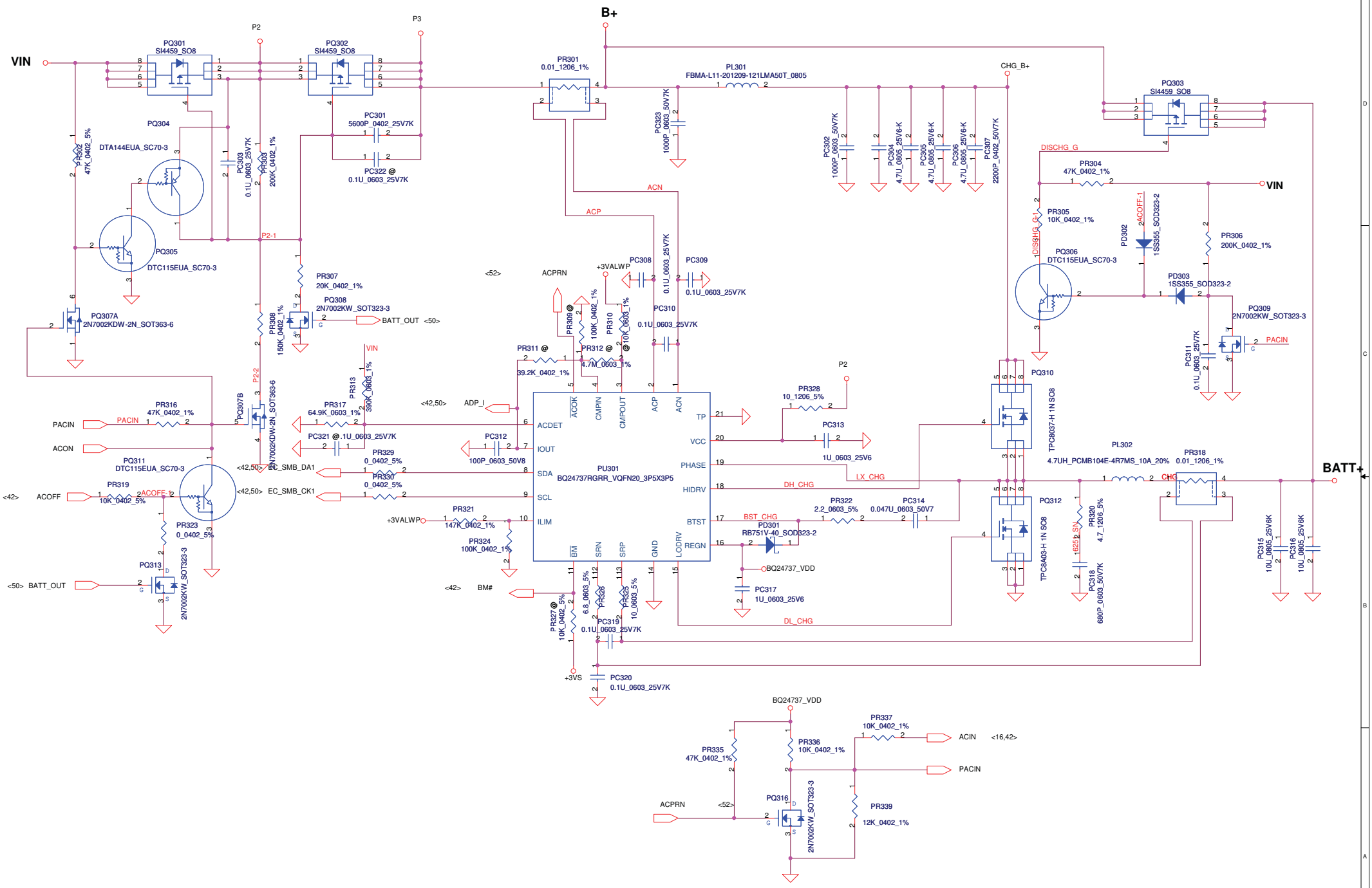


Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

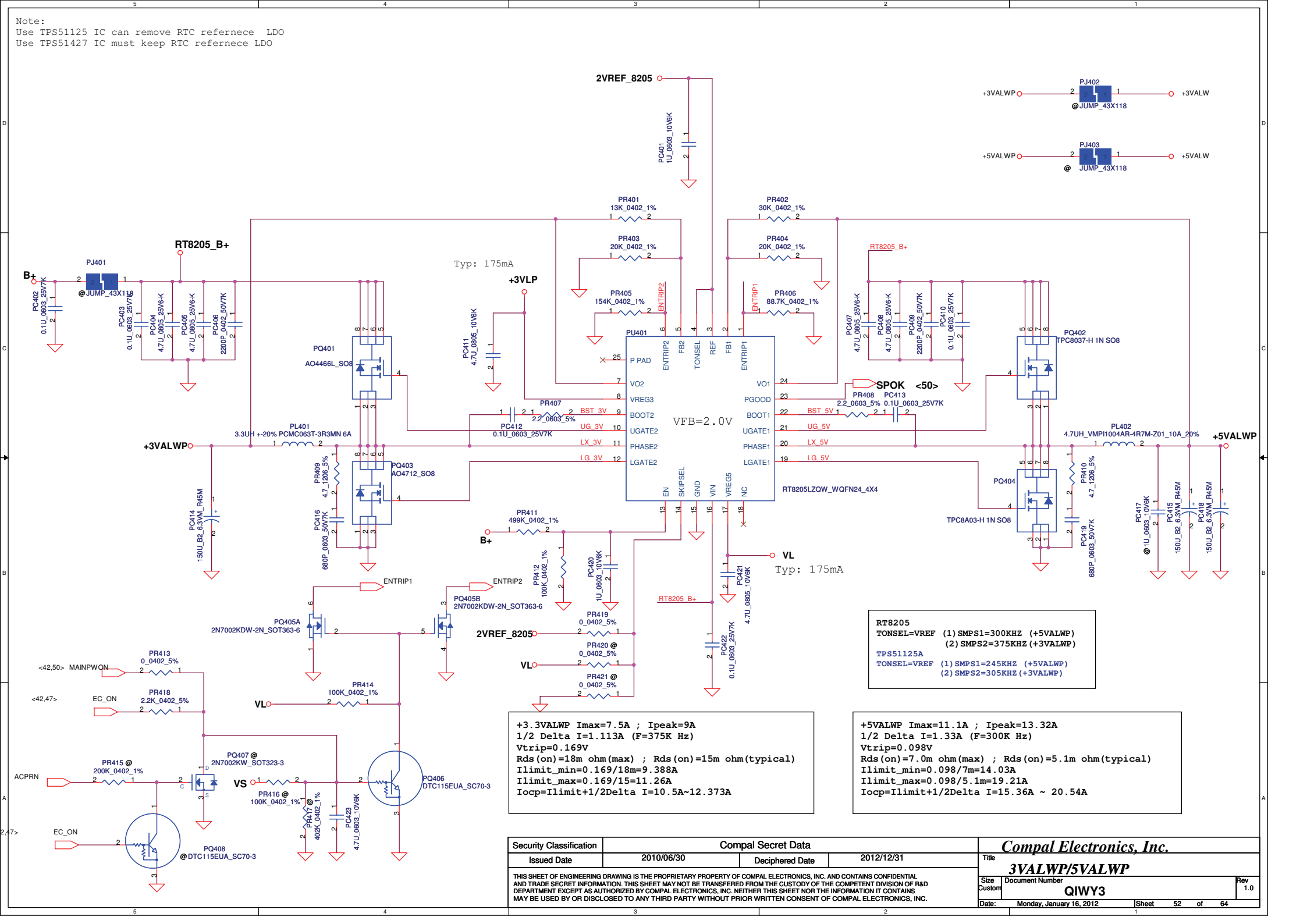
Compal Electronics, Inc.

Title

Size	Document Number	Rev
		1.0

Date: Monday, January 16, 2012 | Sheet 51 of 64

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)
TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ(+3VALWP)

+3.3VALWP Imax=7.5A ; Ipeak=9A
1/2 Delta I=1.113A (F=375K Hz)
Vtrip=0.169V
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=0.169/18m=9.388A
Ilimit_max=0.169/15=11.26A
Iocp=Ilimit+1/2Delta I=10.5A~12.373A

+5VALWP Imax=11.1A ; Ipeak=13.32A
1/2 Delta I=1.33A (F=300K Hz)
Vtrip=0.098V
Rds(on)=7.0m ohm(max) ; Rds(on)=5.1m ohm(typical)
Ilimit_min=0.098/7m=14.03A
Ilimit_max=0.098/5.1m=19.21A
Iocp=Ilimit+1/2Delta I=15.36A ~ 20.54A

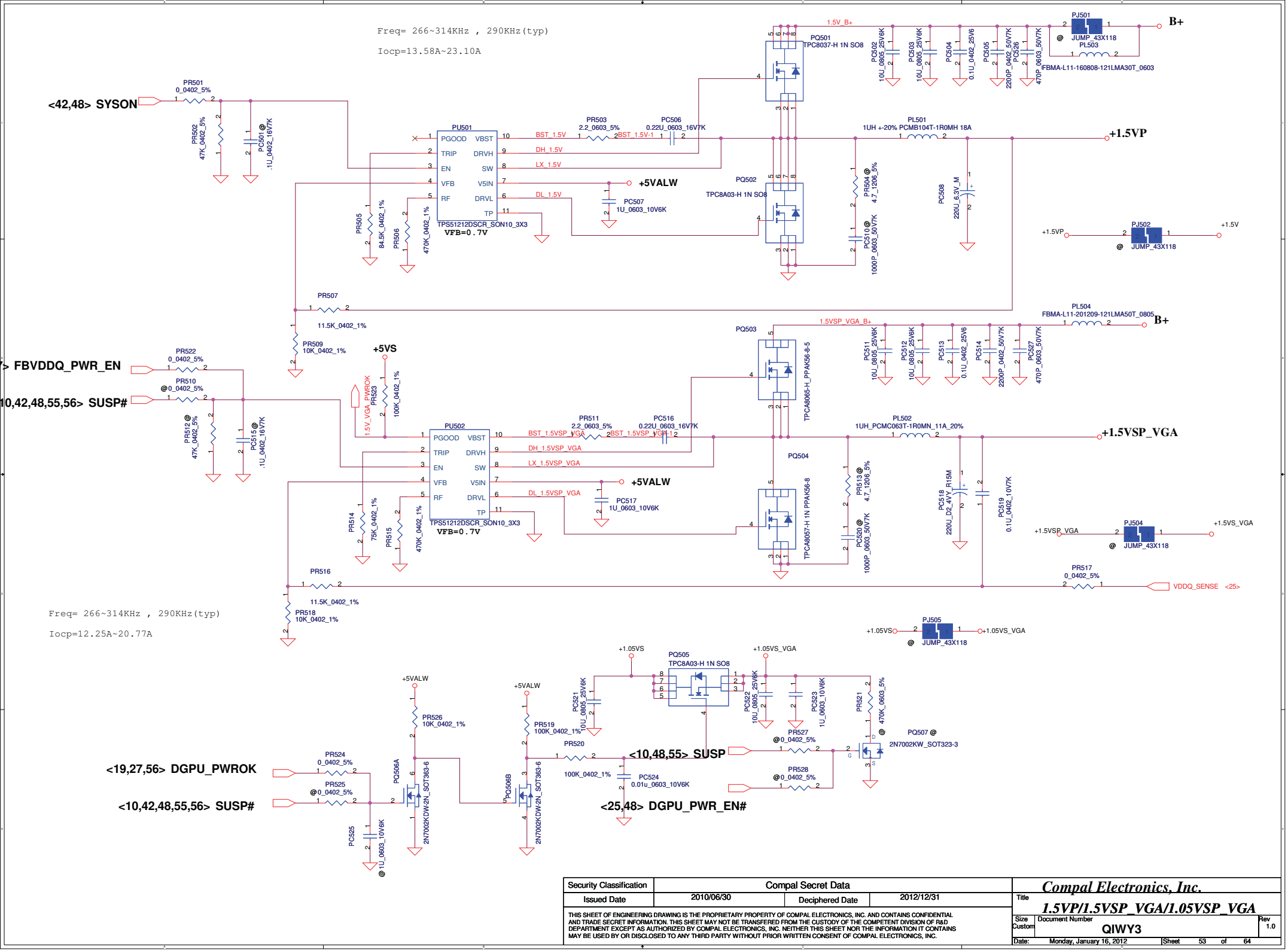
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: QIWY3 | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 52 of 64



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: 1.5VP/1.5VSP_VGA/1.05VSP_VGA

Size: Custom | Document Number: QIWY3 | Rev: 1.0

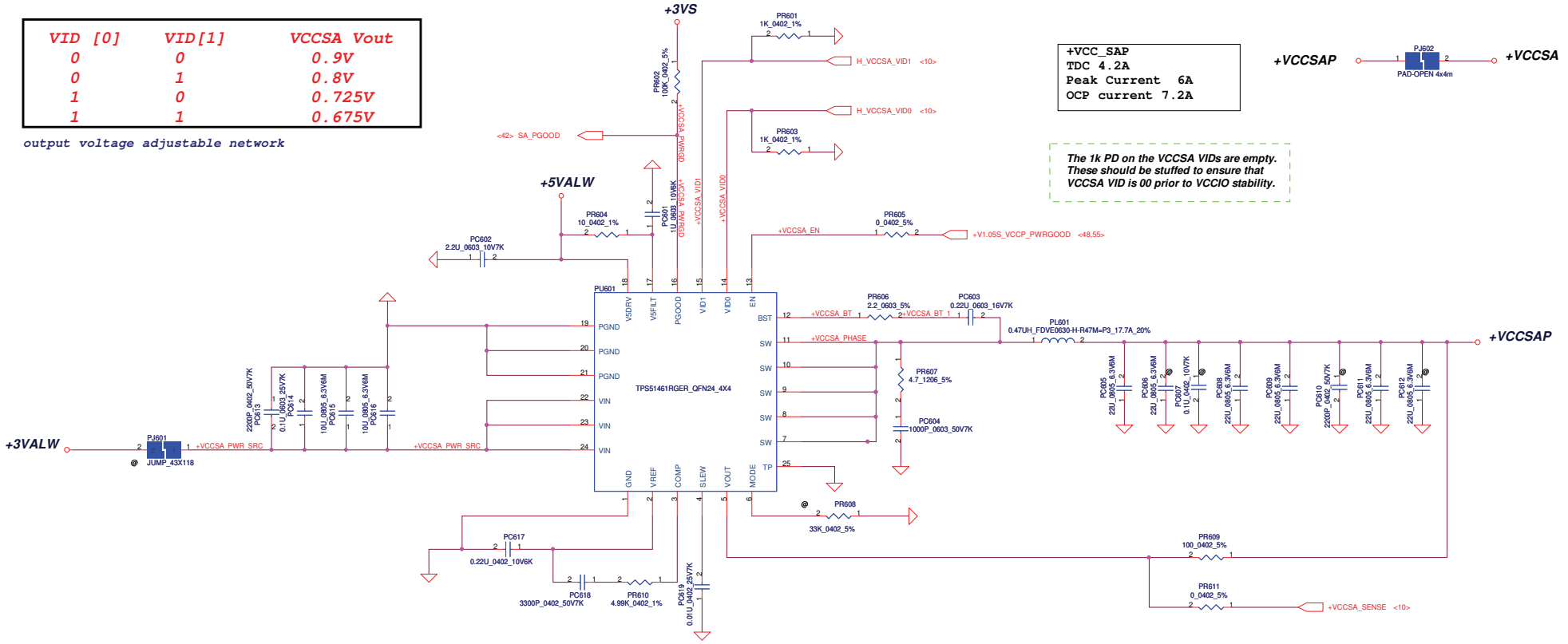
Date: Monday, January 16, 2012 | Sheet 53 of 64

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



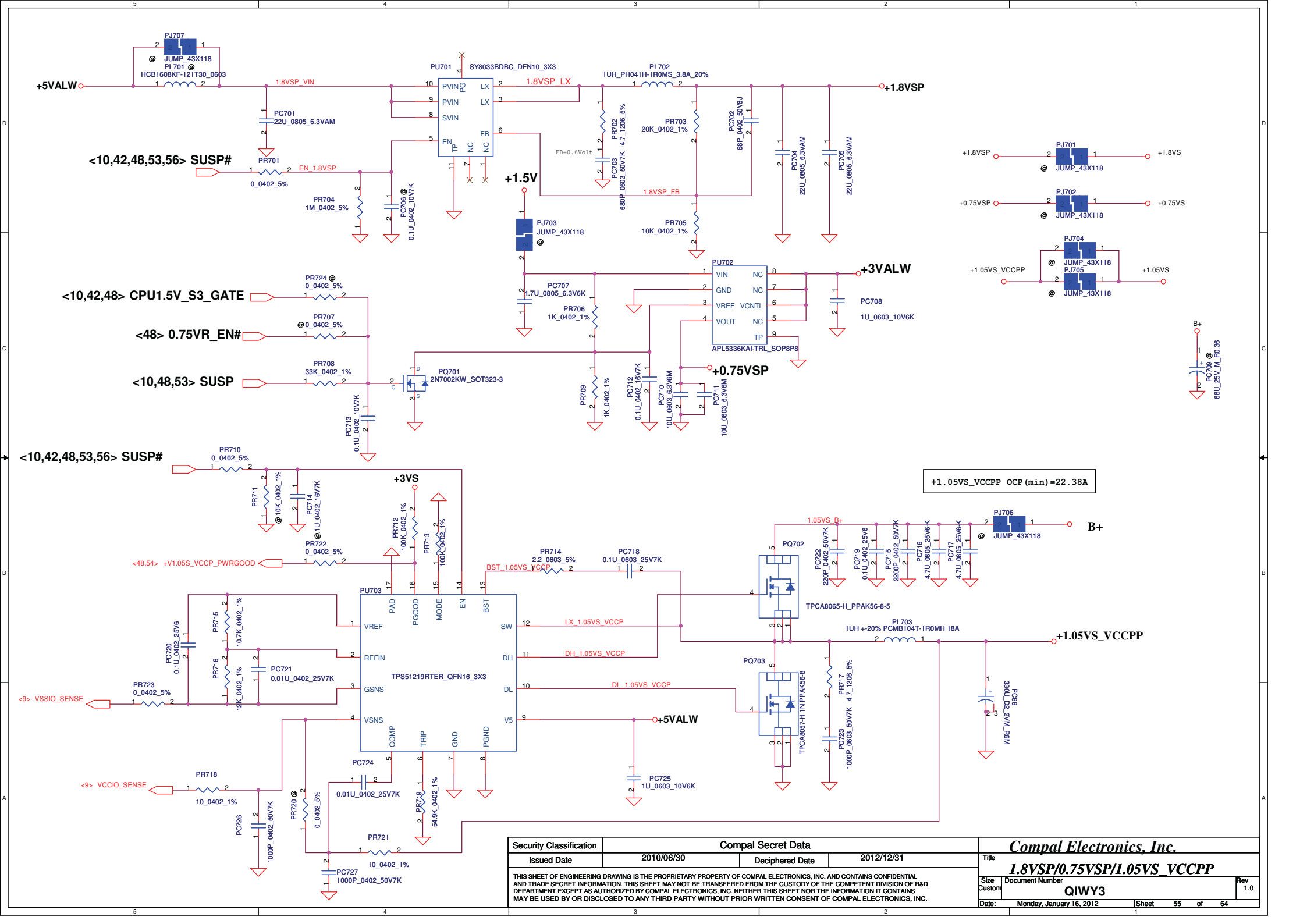
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: VCCSAP/1.05S_VCCPP

Size	Document Number	Rev
C	QIWY3	1.0

Date: Monday, January 16, 2012 Sheet 54 of 64



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	1.8VSP/0.75VSP/1.05VS_VCCPP		
Size: Custom	Document Number: QIWY3		Rev: 1.0
Date: Monday, January 16, 2012	Sheet 55 of 64		

GL1:0.9V(110000)
GT:0.975V(101010)

PQ801@GL1
PQ802@GL1

PQ806@GL1
PQ808@GL1

+VGA_CORE Under VGA Core

+VGA_CORE Near VGA Core

PC818
PC825,PC827,PC828,PC829
PC839,PC841,PC844,PC845

Layout Note:
Place near Phase1 Choke

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

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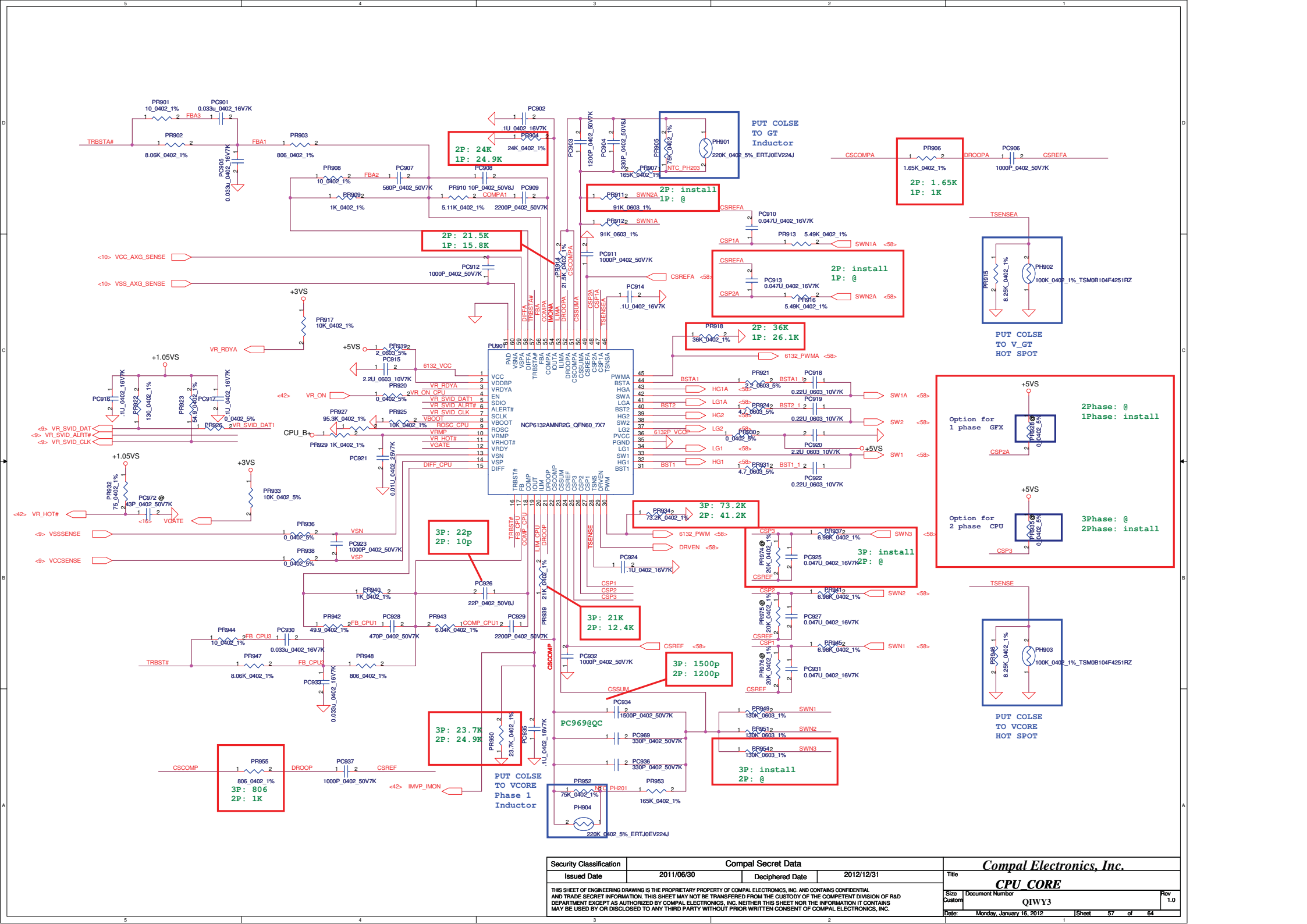
Compal Electronics, Inc.

Title: VGA_COREP

Size: | Document Number: QIWY3 LA-8001P | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 56 of 64



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

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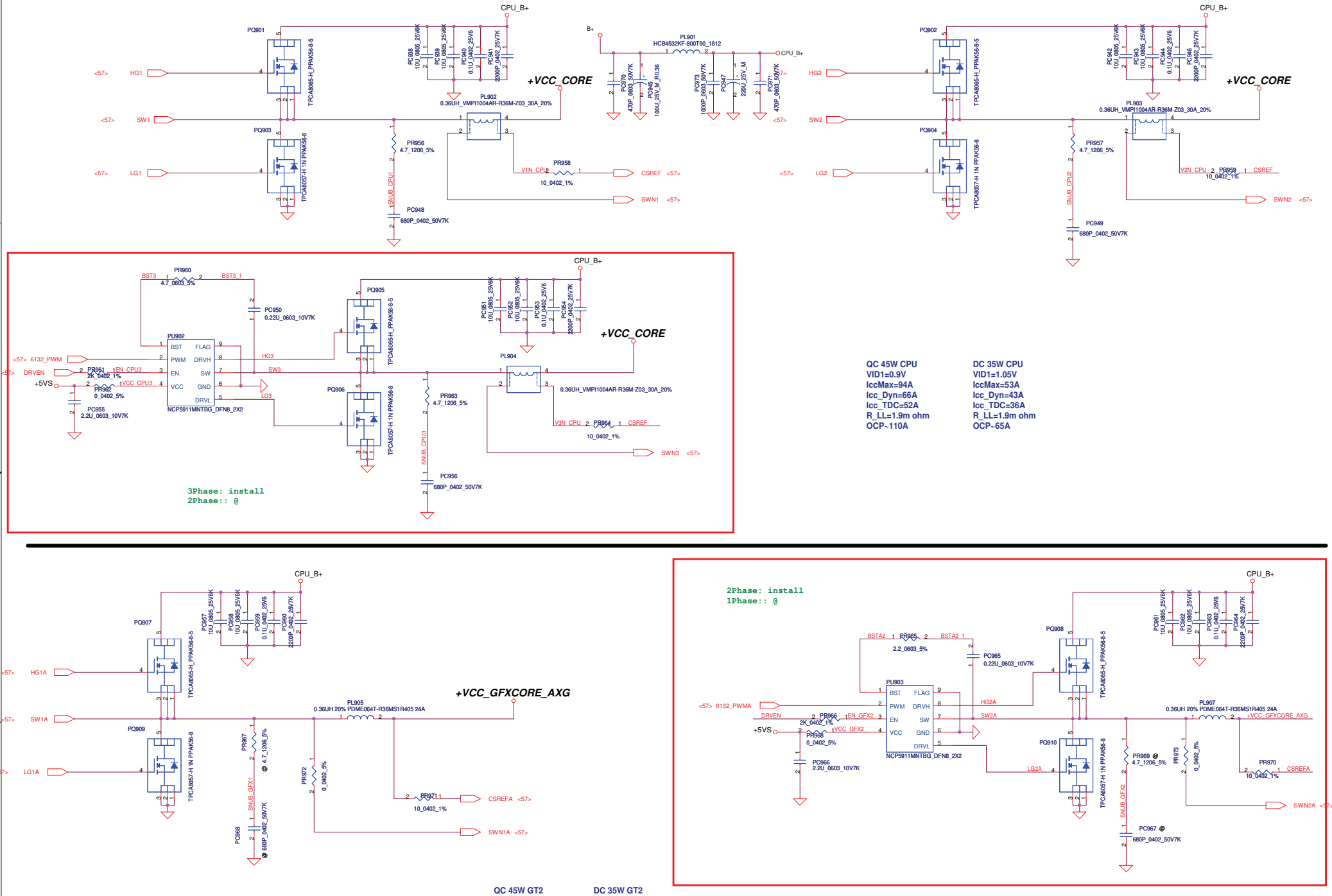
Compal Electronics, Inc.

Title: CPU_CORE

Size	Document Number	Rev
Custom	QIWY3	1.0

Date: Monday, January 16, 2012 | Sheet 57 of 64



Compal Electronics, Inc.

Title: CPU_CORE

Size: C | Document Number: QIWY3 | Rev: 1.0

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+CPU_CORE

+VCC_CORE

PC1 10U_0805_6.3VAM
PC2 10U_0805_6.3VAM
PC3 10U_0805_6.3VAM
PC4 10U_0805_6.3VAM
PC5 10U_0805_6.3VAM
PC6 10U_0805_6.3VAM
PC7 10U_0805_6.3VAM
PC8 10U_0805_6.3VAM
PC9 10U_0805_6.3VAM
PC10 10U_0805_6.3VAM
PC11 10U_0805_6.3VAM

+VCC_CORE

PC20 22U_0805_6.3V6M
PC21 22U_0805_6.3V6M
PC22 22U_0805_6.3V6M
PC23 22U_0805_6.3V6M
PC24 22U_0805_6.3V6M
PC44 22U_0805_6.3V6M
PC45 22U_0805_6.3V6M
PC46 22U_0805_6.3V6M
PC47 22U_0805_6.3V6M
PC48 22U_0805_6.3V6M
PC61 22U_0805_6.3V6M
PC62 22U_0805_6.3V6M
PC63 22U_0805_6.3V6M
PC64 22U_0805_6.3V6M
PC65 22U_0805_6.3V6M
PC69 22U_0805_6.3V6M
PC70 22U_0805_6.3V6M
PC71 22U_0805_6.3V6M
PC72 22U_0805_6.3V6M

+VCC_CORE

PC73 330U_D2_2VM_R9M
PC74 330U_D2_2VM_R9M
PC75@DC 330U_D2_2VM_R9M
PC76 330U_D2_2VM_R9M
PC77 @ 330U_D2_2VM_R9M
PC78 470U_D2_2VM_R9M

PC8,PC21,PC22,PC63

DC:PC73,PC74,PC76(330uF/9m)+PC78(330uF/6m)
QC:PC73,PC74,PC75,PC76(330uF/9m)+PC78(470uF/9m)

+VCC_GFXCORE_AXG

+VCC_GFXCORE_AXG

PC12 22U_0805_6.3V6M
PC13 22U_0805_6.3V6M
PC14 22U_0805_6.3V6M
PC15 22U_0805_6.3V6M
PC16 22U_0805_6.3V6M
PC17 22U_0805_6.3V6M
PC18 22U_0805_6.3V6M
PC19 22U_0805_6.3V6M
PC36 22U_0805_6.3V6M
PC37 22U_0805_6.3V6M
PC38 22U_0805_6.3V6M
PC39 22U_0805_6.3V6M
PC40 22U_0805_6.3V6M
PC41 22U_0805_6.3V6M
PC42 22U_0805_6.3V6M
PC43 22U_0805_6.3V6M
PC57 330U_D2_2VM_R9M
PC58 330U_D2_2VM_R9M
PC59 330U_D2_2VM_R9M

PC59@DC

PC38,PC39,PC40,PC41

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

+1.05VS

+1.05VS

PC25 22U_0805_6.3V6M
PC26 22U_0805_6.3V6M
PC27 22U_0805_6.3V6M
PC28 22U_0805_6.3V6M
PC29 22U_0805_6.3V6M
PC30 22U_0805_6.3V6M
PC31 22U_0805_6.3V6M
PC32 22U_0805_6.3V6M
PC33 22U_0805_6.3V6M
PC34 22U_0805_6.3V6M
PC35 22U_0805_6.3V6M
PC49 22U_0805_6.3V6M
PC50 22U_0805_6.3V6M
PC51 22U_0805_6.3V6M
PC52 22U_0805_6.3V6M
PC53 22U_0805_6.3V6M
PC54 22U_0805_6.3V6M
PC55 22U_0805_6.3V6M
PC56 22U_0805_6.3V6M
PC67 330U_D2_2VM_R6M
PC68 330U_D2_2VM_R6M

PC32,PC49,PC54,PC55,PC56

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size | Document Number: QIWY3 LA-8001P | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 59 of 64

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve 0.1uF for Charger IC	51	Reserve PC321	2011/09/27	B test
2	EMI Request		change PR322,PR407,PR408,PR503,PR511,PR606,PR804,PR827 to 2.2 ohm add PC526,PC527,PC970,PC971(470pF)	2011/09/27	B test
3	Combine 1.05V	51	Remove one power rail +V1.05S_VCCPP Pop PR722,PR712,PR718	2011/09/27	B test
4	Discharge for +1.05VS_VGA by NV Request	53	Reserve PR528	2011/09/27	B test
5	Set VGA_CORE VBOOT voltage	56	unpop PR806 change PR813 to 147K ohm	2011/09/27	B test
6	For VGA_CORE power saving by NV Request	56	add PR838 0ohm	2011/09/27	B test
7	for CPU_CORE load line adjust	57	add PC969	2011/09/27	B test
8	to prevent MOS over temperature	55/58	change PQ702,PQ901,PQ902,PQ905 TPCA8065	2011/09/27	B test
9	for CPU_CORE test	59	Reserve PC77,PC78	2011/09/27	B test
10	for debug	51	add PR329,PR330	2011/11/30	C test
11	for VCCIO remote sense	55	add PR723	2011/11/30	C test
12	RC filter to reduce noise	55	add PR721,PC727	2011/11/30	C test
13	G718 for adapter and OTP	50	pop PC203,PQ201,PR209,PU201,PR213 unpop PR206	2011/11/30	C test
14	for CPU transient	58	change PR911,PR912 to 91K	2011/11/30	C test
15	for EMI Request		add PL301,PC503,PL504,PL801 add PC302,PC323,PC424,PC526,PC722,PC970,PC974	2011/11/30	C test
16	HW reqeust	50 55	reserve connect PCH_PWR_EN for power sequence reserve connect CPU1.5V_S3_GATE for power sequence	2011/11/30	C test
17	for thermal request to reduce temperature	53	change PQ503,PQ504	2011/11/30	C test
18	adjust 1.5VSP_VGA OCP	53	change PR514 to 49.9K	2011/11/30	C test
19	For HW power sequence adjustment	50	change PR222,PR228 to NA change PR229 to 0 ohm	2011/12/02	C test
20	To adjust +5VALW by HW request	52	change PR404 to 19.6K	2011/12/16	C test
21	Using G718 to replace KB9012 function need to add or reserve resistor	50	Add PR232 and reserve PR233 pull high to +3VALW Add PR234 pull down	2011/12/28	Pre MP

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
22	TI 's suggestion that snubber should be first at R than C	54	change PR607 and PC604 order	2011/12/28	Pre MP
23	Reserve resistor for adjust current balance	57	Reserve PR974,PR975,PR976	2011/12/28	Pre MP
24	To reduce noise	58	change PC945 to 220uF	2011/12/28	Pre MP

QIWY3 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				EVT TO DVT
1		P7	Reserve R64	Reserve EC DRAMRST control pin for Deep S3
2		P16	Reserve R1457,R1455,R1447	Reserve SUSACK#,SUSWARN#,SLP_SUS# control signal for Deep S3
3		P16	Reserve Q118,R1120,R1121	Reverse SLP_SUS# to control +3V_PCH&+5V_PCH
4		P16	Change AC_PRESENT Pull high source to +3V_DSW	For Deep S3 function
5		P21	Remove R289	+5V_PCH control circuit change for Deep S3
6		P36	Reserve J8,Q104,C533,C526,R436	Reserve for AOAC function
7		P36	Change JP1 pin2,24,52 power source to +3VS_WLAN_AOAC	Reserve for AOAC function
8		P42	Change EC GPIO pin setting (Impact pin 18,71,72,126,128)	For DeepS3/AOAC function
9		P48	Reserve J11,J14,Q148,Q149,C38,C39	+3V_PCH&+5V_PCH control circuit for Deep S3
10		P45	change U49 symbol (without GND pad)	For DFx issue
11		P46	change U40,U69 symbol (without GND pad)	For DFx issue
12		P47	change JP10 type to SP01001B800	For DFx issue
13		P19	Reserve R207,R224 to contact WLAN wake even	Reserve for AOAC function
14		P41	Change JSPK1 type to SP02000H700	For DFx issue
14		P19	Reserve R704 and R706 for GPIO69 PU&PD	For SKU ID
15		P23	Change CV37,CV38 to 22P	For Crystal EA request
16		P37	Change C968,C969 to 33P	For Crystal EA request
				DVT TO PVT
1		P14	Change power source to +5VS (Q10 pin 2)	Follow intel Design Guide
2		P16	Reserve R257 PU 10K to +3V_DSW	For Deep S3 function
3		P40	Change R1110 to 200K,C638 to 0.1u	For ODD soft star
4		P10	Change C124,C125,C126,C127,C130 to 0603 type	For commond design
5		P20	Change C215,C221,C395 to 0603 type	For commond design
6		P21	Change C231 to 0603 type	For commond design
7		P33	Change C519 to 0603 type	For commond design
8		P36	Change C568,C569 to 0603 type	For commond design
9		P37	Change C937,C954,C953 to 0603 type	For commond design
10		P39	Change C986 to 0603 type	For commond design
11		P40	Change C634,C635,C639 to 0603 type	For commond design
12		P41	Change C655 to 0603 type	For commond design
13		P48	Change C836,C837,C839,C840,C847 C848,C856,C857 to 0603 type	For commond design
14		P47	Change C906 to 0603 type	For commond design
15		P47	Modify gate powr rail of MOS to +5VALW	Avoid leakage issue.
16		P45	Change U39 source to SA00004KB00	For main source issue
17		P46	Change U40,U69 source to SA00004KB00	For main source issue
18		P37	Add Q150,R145,C976	For LAN power control
19		P42	Reserve LAN_PWR_ON# net on EC pin 89	For LAN power control
20		P41	Stuff R945,R481 for EAPD contact U8 pin29	For MUTE_LED issue
21		P38	Add R90	For LAN SURGE CO-LAY
22		P38	Add R1380	Atheros request

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				PVT TO SVT
1		P46	change JP21 type (SP010011A00)	For ASSY issue
2		P23	RV208 change to contact +VDD33MISC	For N13P-GT/N13E-GE shutdown issue
3		P23	Reserve RV14	For N13P-GT/N13E-GE +VDD33MISC leakage issue
4		P41	Swap HP R/L	For HP R/L reverse issue
5		P42	Add R1415,R1419	T/P SM BUS pull high voltage change

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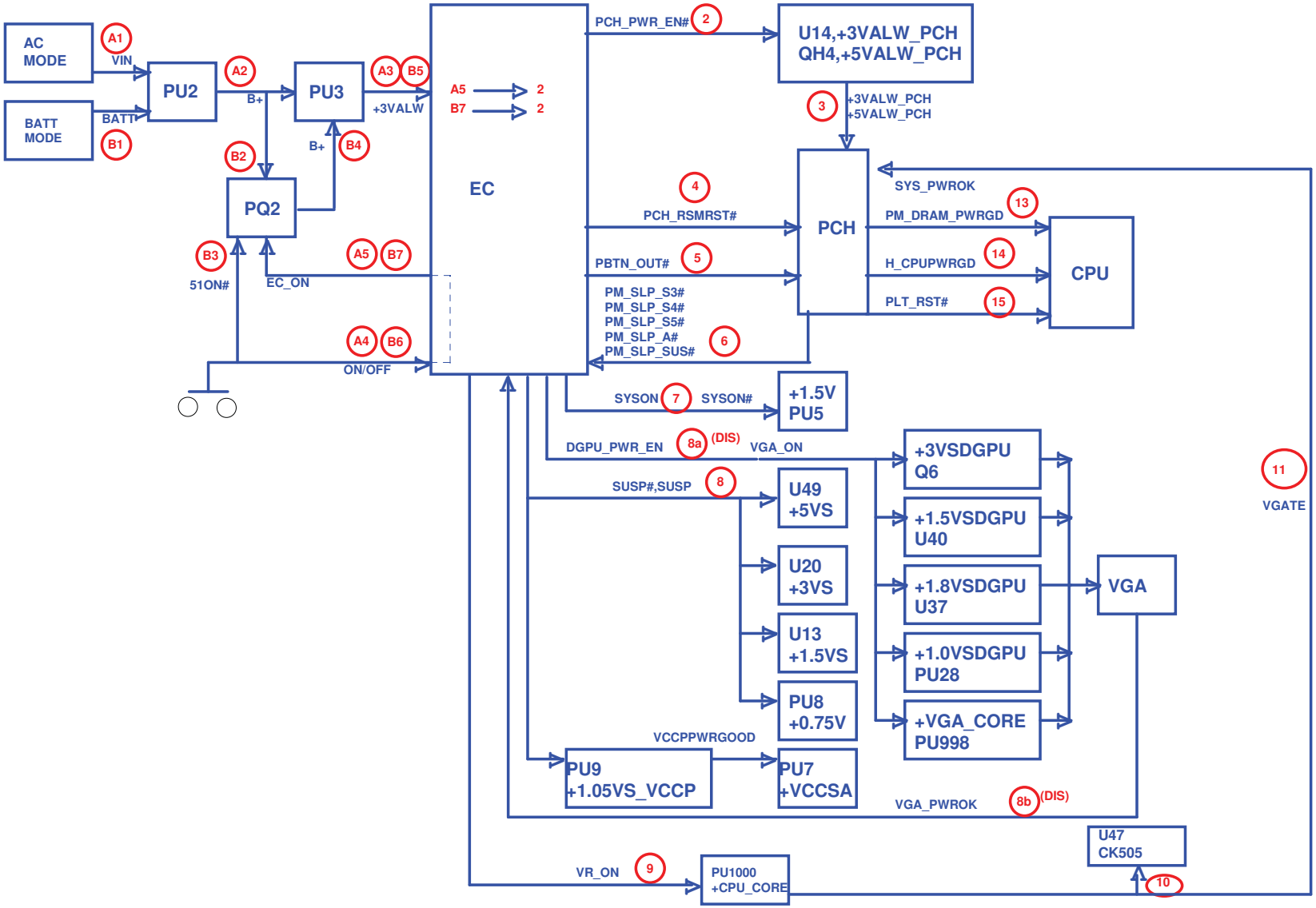

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