TWS Shark Bay DIAGRAM

01

www.laptopschematics.com

+3V/+5V S5 PG.34

+1.05V PG.35

CPU Core PG.38~39

DDR3L PG.36

Charge PG.33

Dis-Charge PG.37

+VGACORE PG.40

+1.5V_GFX PG.41

+1.05V_GFX/3V_GFX PG.42

SODIMM1 Max. 4GB PG.12 — 1600MT/s DDR3 L Channel A

SODIMM2 Max. 4GB PG.13 — 1600MT/s DDR3 L Channel B

INTEL Haswell
Processor : Daul / Quad Core
Power : 37 / 47 (Watt)
Package : rPGA947
Size : 37.5 x 37.5 (mm)
PG.2~5

PCI-E x8

nVIDIA N14P-GS
GB4128
FCBGA908
29mm X 29mm
PG.14~18

eDP (5.4Gb/s)

DDI (5.4Gb/s)

DDR3 900MHz

VRAM 128Mx16x8,128bit PG.19~20

FDI DMI

HDD PG.32 — SATA0 6GB/s SATA0

ODD PG.32 — SATA4 3GB/s SATA4

mSATA PG.32 — SATA1 6GB/s SATA1

INTEL PCH
Lynx Point
Power : 3.5 Watt
Package : FCBGA695
Size : 20 x 20 (mm)
PG.6~11

eDP — RTD 2136S DP to LVDS Converter PAGE 22 — LVDS Interface — LVDS PG.23

DP Port B — HDMI PG.21

CRT — CRT PG.21

USB 3.0 PORT1 — USB3.0 Ports X1 PG.27

USB Charge SLG55583A DRE rof PG.27

USB 2.0 PORT0 DRE rof — PORT9,11 — USB2.0 Ports X2 PG.26

PORT4 — Webcam PG.23

PCI-E x 1 LANE2 — LAN RTL8111GS-CG GbE PG.30

PCI-E x 1 LANE1 — WLAN BT COMBO PG.29 — USB 2.0 PORT10

PCI-E x 1 LANE3 — Card Reader 5227-GRT PG.25

Accelerometer PG.24 — SMBUS

KBC IT8528E PG.31 — LPC

KB PG.27 | TP PG.32 | ROM PG.31 | FAN PG.32

TPM SLB9635TT1.2

AUDIO CODEC ALC282-CG PG.26

Speaker DRE rof PG.26

HP/MIC PG.26

Analog MIC PG.26

Stackup DRE rof

TOP
GND
IN1
IN2
VCC
BOT

NB5

PROJECT : TWS DRE rof
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Friday, August 16, 2013 | Sheet 1 of 43

Haswell Processor (DMI,PEG,FDI)

Haswell Processor (CLK,MISC,JTAG)

02

U23A DRE rof

DMI_TXN0 D21 DMI_RX#[0]
DMI_TXN1 C21 DMI_RX#[1]
DMI_TXN2 B21 DMI_RX#[2]
DMI_TXN3 A21 DMI_RX#[3]
DMI_TXP0 D20 DMI_RX[0]
DMI_TXP1 C20 DMI_RX[1]
DMI_TXP2 B20 DMI_RX[2]
DMI_TXP3 A20 DMI_RX[3]
DMI_RXN0 D18 DMI_TX#[0]
DMI_RXN1 C17 DMI_TX#[1]
DMI_RXN2 B17 DMI_TX#[2]
DMI_RXN3 A17 DMI_TX#[3]
DMI_RXP0 D17 DMI_TX[0]
DMI_RXP1 C18 DMI_TX[1]
DMI_RXP2 B18 DMI_TX[2]
DMI_RXP3 A18 DMI_TX[3]

DMI

FDI_TXN0 P33 FDI_TX#[0]
FDI_TXN1 N32 FDI_TX#[1]
FDI_TXP0 R33 FDI_TX[0]
FDI_TXP1 P32 FDI_TX[1]
FDI_INT J29 FDI_INT
FDI_CSYNC R102 *0_4/S FDI_CSYNC_R H29 FDI_CSYNC

FDI

DPB_LANE0_N T28 DDIB_TX#[0]
DPB_LANE1_N T30 DDIB_TX#[1]
DPB_LANE2_N U29 DDIB_TX#[2]
DPB_LANE3_N U31 DDIB_TX#[3]
DPB_LANE0_P U28 DDIB_TX[0]
DPB_LANE1_P U30 DDIB_TX[1]
DPB_LANE2_P V29 DDIB_TX[2]
DPB_LANE3_P V31 DDIB_TX[3]
DDIC_TX#[0] T34
DDIC_TX#[1] U35
DDIC_TX#[2] U32
DDIC_TX#[3] U33
DDIC_TX[0] U34
DDIC_TX[1] V35
DDIC_TX[2] T32
DDIC_TX[3] V33
DDID_TX#[0] P29
DDID_TX#[1] N28
DDID_TX#[2] P31
DDID_TX#[3] N30
DDID_TX[0] R29
DDID_TX[1] P28
DDID_TX[2] R31
DDID_TX[3] P30

Intel(R) DDI

IN_D2# IN_D1# IN_D0# IN_CLK# IN_D2 IN_D1 IN_D0 IN_CLK

FDI_CSYNC & FDI_INT
Trace length < 10000 Mils
Impendance = 50 ohm

eDP_RCOMP E24
EDP_DISP_UTIL R71 *0_4 INT_eDP_HPD_Q R27 EDP_DISP_UTIL
eDP_HPD P27
EDP_AUXP N27 EDP_AUX
EDP_AUXN M27 EDP_AUX#
EDP_TXP0 R35 EDP_TX[0]
EDP_TXP1 P34 EDP_TX[1]
EDP_TXN0 P35 EDP_TX#[0]
EDP_TXN1 N34 EDP_TX#[1]

eDP

HSW_RPGA_EDS_PGA

PCI EXPRESS* - GRAPHICS

PEG_COMP
PEG_RCOMPO E23

PEG_RX#[0..7] 14
PEG_RX#[0] M29 PEG_RX#0
PEG_RX#[1] K28 PEG_RX#1
PEG_RX#[2] M31 PEG_RX#2
PEG_RX#[3] L30 PEG_RX#3
PEG_RX#[4] M33 PEG_RX#4
PEG_RX#[5] L32 PEG_RX#5
PEG_RX#[6] M35 PEG_RX#6
PEG_RX#[7] L34 PEG_RX#7
PEG_RX#[8] E29
PEG_RX#[9] D28
PEG_RX#[10] E31
PEG_RX#[11] D30
PEG_RX#[12] E35
PEG_RX#[13] D34
PEG_RX#[14] E33
PEG_RX#[15] E32

PEG_RX[0..7] 14
PEG_RX[0] L29 PEG_RX0
PEG_RX[1] L28 PEG_RX1
PEG_RX[2] L31 PEG_RX2
PEG_RX[3] K30 PEG_RX3
PEG_RX[4] L33 PEG_RX4
PEG_RX[5] K32 PEG_RX5
PEG_RX[6] L35 PEG_RX6
PEG_RX[7] K34 PEG_RX7
PEG_RX[8] F29
PEG_RX[9] E28
PEG_RX[10] F31
PEG_RX[11] E30
PEG_RX[12] F35
PEG_RX[13] E34
PEG_RX[14] F33
PEG_RX[15] D32

PEG_TX#[0] H35 C_PEG_TX#0
PEG_TX#[1] H34 C_PEG_TX#1
PEG_TX#[2] J33 C_PEG_TX#2
PEG_TX#[3] H32 C_PEG_TX#3
PEG_TX#[4] J31 C_PEG_TX#4
PEG_TX#[5] G30 C_PEG_TX#5
PEG_TX#[6] C33 C_PEG_TX#6
PEG_TX#[7] B32 C_PEG_TX#7
PEG_TX#[8] B31
PEG_TX#[9] A30
PEG_TX#[10] B29
PEG_TX#[11] A28
PEG_TX#[12] B27
PEG_TX#[13] A26
PEG_TX#[14] B25
PEG_TX#[15] A24

PEG_TX[0] J35 C_PEG_TX0
PEG_TX[1] G34 C_PEG_TX1
PEG_TX[2] H33 C_PEG_TX2
PEG_TX[3] G32 C_PEG_TX3
PEG_TX[4] H31 C_PEG_TX4
PEG_TX[5] H30 C_PEG_TX5
PEG_TX[6] B33 C_PEG_TX6
PEG_TX[7] A32 C_PEG_TX7
PEG_TX[8] C31
PEG_TX[9] B30
PEG_TX[10] C29
PEG_TX[11] B28
PEG_TX[12] C27
PEG_TX[13] B26
PEG_TX[14] C25
PEG_TX[15] B24

36 DDR_VR_PWRGD
6 SYS_PWROK

U23B

SKTOCC# AP32
CATERR# AN32
PECI AR27
FC_AK31 AK31
PROCHOT# AM30
THERMTRIP# AM35
PM_SYNC AT28
UNCOREPWRGOOD AL34
SM_DRAMPWROK AC10
RESET# AT26

MISC
THERMAL
PWR MANAGEMENT

HSW_RPGA_EDS_PGA

H_PECI (50ohm)
Route on microstrip only
Spacing > 18 mils
Trace Length: 15 inch

TP70 SKTOCC#
TP62 TP_CATERR#

HPECI Ra,Ca need placement close to EC.
Ra
Ca
9,31 EC_PECI R514 43_4 H_PECI
C602 *47P/50V_4

4/30 CRB 1.0 Add
+VCCST

PROCHOT# (50ohm)
Trace Length <11 inches
31,38 H_PROCHOT# R124 56.2/F_4 H_PROCHOT#_R
C73 47P/50V_4
Cb need placment near VR
Cb

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
9,31 PM_THRMTRIP#R PM_THRMTRIP#_R
Rb need placment near PCH
4/30 CRB 1.0 Add
+1.05V R196 *1K/F_4
Rb

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches
6 PM_SYNC R512 *0_4/S PM_SYNC_R
C214 *0.1U/10V_4

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches
9 H_PWRGOOD R106 *0_4/S H_PWRGOOD_R
R101 10K_4

PM_DRAM_PWRGD_R
CPU RESET#
9,31 CPU_PLTRST#R
R517 *750/F_4
8,14,24,25,29,30,31 PLTRST# CPU_PLTRST#R
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches
R516 *1.5K/F_4

Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impendence 90 ohm

CLOCKS
BCLK CLK_CPU_BCLKP E26 D26 CLK_CPU_BCLKN
SSC_DPLL_REF_CLK E27 CLK_DPLL_SSCLKP
SSC_DPLL_REF_CLK# F27 CLK_DPLL_SSCLKN
DPLL_REF_CLK H28 CLK_DPLL_NSCCLKP
DPLL_REF_CLK# G28 CLK_DPLL_NSCCLKN

DDR3 MISC
SM_DRAMRST# AN3 CPU_DRAMRST#
SM_RCOMP[0] AP3 SM_RCOMP_0 R153 100/F_4
SM_RCOMP[1] AR3 SM_RCOMP_1 R157 75/F_4
SM_RCOMP[2] AP2 SM_RCOMP_2 R158 100/F_4
SM_RCOMP[0] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[1] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[2] W:12mils/S:15mils/L: 500mils,

JTAG & BPM
PRDY# AR29 XDP_PRDY# TP73
PREQ# AT29 XDP_PREQ# TP72
CPU XDP
TCK AM34 XDP_TCLK TP7
TMS AN33 XDP_TMS TP10
TRST# AM33 XDP_TRST# TP9
TDI AM31 XDP_TDI_R TP12
TDO AL33 XDP_TDO TP11
DBR# AP33 XDP_DBRST# R582 *1K_4 +3V XDP_DBRST# 6
BPM#[0] AR30 XDP_BPM0 TP64
BPM#[1] AN31 XDP_BPM1 TP71
BPM#[2] AN29 XDP_BPM2 TP74
BPM#[3] AP31 XDP_BPM3 TP63
BPM#[4] AP30 XDP_BPM4 TP66
BPM#[5] AN28 XDP_BPM5 TP75
BPM#[6] AP29 XDP_BPM6 TP69
BPM#[7] AP28 XDP_BPM7 TP67

SM_DRAMPWROK Processor Input.

To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWRGOOD

+3VS5
PM_DRAM_PWRGD_C (50ohm)
Trace Length: < 1 inches
R143 100K_4 R142 100K_4
C265 0.1U/10V_4
+1.35VSUS
DG 498556 -> 1.8K
R133 1.8K/F_4
DDR_VR_PWRGD R141 *0_4 SYS_PWROK
R141不上件 2013/02/20
U7 74AHC1G09GW
4PM_DRAM_PWRGD_C
R134 0_4 R137 *0_4 PM_DRAM_PWRGD_R
PM_DRAM_PWRGD
R132 3.3K_4
DG 498556 -> 3.3K
C271 *0.1U/10V_4
PM_DRAM_PWRGD (50ohm)
Trace Length: 2~7 inches
PM_DRAM_PWRGD_R (50ohm)
Trace Length: 0.5~1 inches
DDR_VR_PWRGD D11 *MEK500V-40
DDR_VR_PWRGD (50ohm)
Trace Length: 2~7 inches
C269 *0.1U/10V_4

DDR3 DRAM RESET

DDR3_DRAMRST#_R (50ohm)
Trace Length < 6 inches
+1.35VSUS R160 *1K_4
12,13 DDR3_DRAMRST# R159 *0_4/S CPU_DRAMRST#
C289 *0.1U/10V_4
PM_DRAM_PWRGD 6

+VCCIO_OUT 4,38
+VCCIOA_OUT 4
+1.05V 4,9,10,27,35,42
+1.35VSUS 4,12,13,36
+3VS5 6,7,9,10,24,27,28,29,31,34,36,37,42
+3V 6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,28,29,30,31,32,37,38,40

4/30 CRB V1.0 -> 10K
+VCCIO_OUT
R75 10K_4
INT_eDP_HPD_Q
Q7 2N7002
R68 100K_4
EDP_HPD 22,23

PEG x8 disable (UMA only remove)

14 PEG_TX[0..7]
C_PEG_TX0 C146 0.22U/10V_4 PEG_TX0
C_PEG_TX1 C135 0.22U/10V_4 PEG_TX1
C_PEG_TX2 C144 0.22U/10V_4 PEG_TX2
C_PEG_TX3 C137 0.22U/10V_4 PEG_TX3
C_PEG_TX4 C133 0.22U/10V_4 PEG_TX4
C_PEG_TX5 C147 0.22U/10V_4 PEG_TX5
C_PEG_TX6 C138 0.22U/10V_4 PEG_TX6
C_PEG_TX7 C149 0.22U/10V_4 PEG_TX7
0.22uF AC coupling Caps for PCIE GEN1/2/3

14 PEG_TX#[0..7]
C_PEG_TX#0 C145 0.22U/10V_4 PEG_TX#0
C_PEG_TX#1 C134 0.22U/10V_4 PEG_TX#1
C_PEG_TX#2 C143 0.22U/10V_4 PEG_TX#2
C_PEG_TX#3 C136 0.22U/10V_4 PEG_TX#3
C_PEG_TX#4 C132 0.22U/10V_4 PEG_TX#4
C_PEG_TX#5 C148 0.22U/10V_4 PEG_TX#5
C_PEG_TX#6 C131 0.22U/10V_4 PEG_TX#6
C_PEG_TX#7 C139 0.22U/10V_4 PEG_TX#7
0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation DRE rof

+VCCIOA_OUT R112 24.9/F_4 eDP_RCOMP
eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils
+VCCIOA_OUT R118 24.9/F_4 PEG_COMP
PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

Processor pull-up (CPU) DRE rof

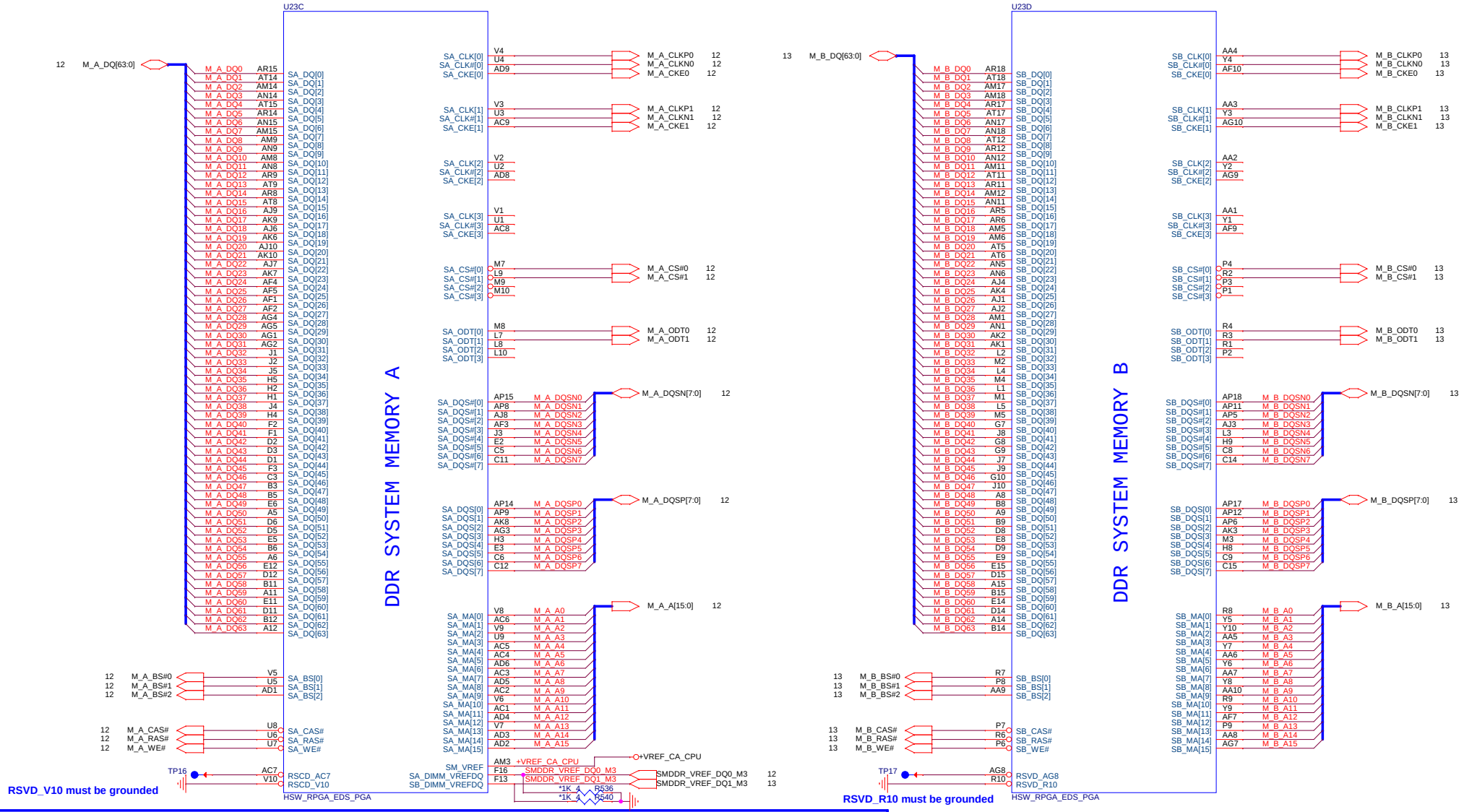
H_PROCHOT# R123 62_4 +VCCIO_OUT
CLK_DPLL_SSCLKP R105 *10K_4
CLK_DPLL_SSCLKN R99 *10K_4
XDP_TDO R115 51_4
XDP_TMS R110 *51_4 +1.05V
XDP_TDI_R R120 *51_4
XDP_PREQ# R519 *51_4
XDP_TCLK R90 51_4
XDP_TRST# R97 51_4
check

NB5

PROJECT : TWS DRE rof
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HAS 1/4 (PCIE&DMI&FDI)	1A
Date: Friday, August 16, 2013	Sheet 2 of 43	

Haswell Processor (DDR3)



Haswell Processor (POWER)

04

POWER

+VCCIN 95A

+1.35VSUS 4.2A

U23F

HSW_RPGA_EDS_PGA

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

VCC Output Decoupling Recommendations

470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

+VCCIOA_OUT 2
+VCCIO_OUT 2,38
+VCCIO_PCH 10
+1.5V 6,7,8,10,26,29,32,36

+1.05V 2,9,10,27,35,42
+VCC_CORE 38,39
+VCCST 2
+1.35VSUS 2,12,13,36

HW Thrm Protect

+3VPCU

For 65 degree, 1.8v limit, (SW)

R492 20K/F_4

For 75 degree, 1.2v limit, (HW)

THRM_MOINTOR1 31

R495 100K_6 NTC

C598 *0.1U/10V_4

4/30: CRB 1.0 add

+1.05V R119 *0_8 +VCCST

C240 *10U/6.3V_6

C245 *10U/6.3V_6

Power Test Propose

+1.05V R94 150/F_4 PWR_DEBUG_R R92 *10K_4

+1.05V R109 *0_8 +VCCIO_OUT C217 *4.7U/6.3V_6

+1.05V R515 0_6 +VCCIO_PCH

CRB 1.0 stuff C600 *4.7U/6.3V_6

4/30: DG 498550

Haswell PWR_DEBUG requires a 150-Ohm pull-up resistor to PCH 1.05-V VCC Core when routed to XDP

CPU VDDQ

Layout note: It is recommended to shield VIDSOUT signal by routing it in between the VIDSCLK and VIDALERT# signals.

SVID CLK

H_CPU_SVIDCLK VR_SVID_CLK 38

SVID DATA

+VCCIO_OUT R129 130/F_4

Place PU resistor close to CPU

DG V0.7 -> 110 Ohm
SCH V0.7 -> 130 Ohm

H_CPU_SVIDDAT VR_SVID_DATA 38

Place PU resistor close to CPU
The VIDALERT# signal must have a damping resistor to prevent overshoot

SVID ALERT

C218 *0.1U/10V_4

+VCCIO_OUT R126 75/F_4

DG V0.7 -> 44 Ohm
SCH V0.7 -> 43 Ohm

H_CPU_SVIDALRT# R128 43_4 VR_SVID_ALERT# 38

Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

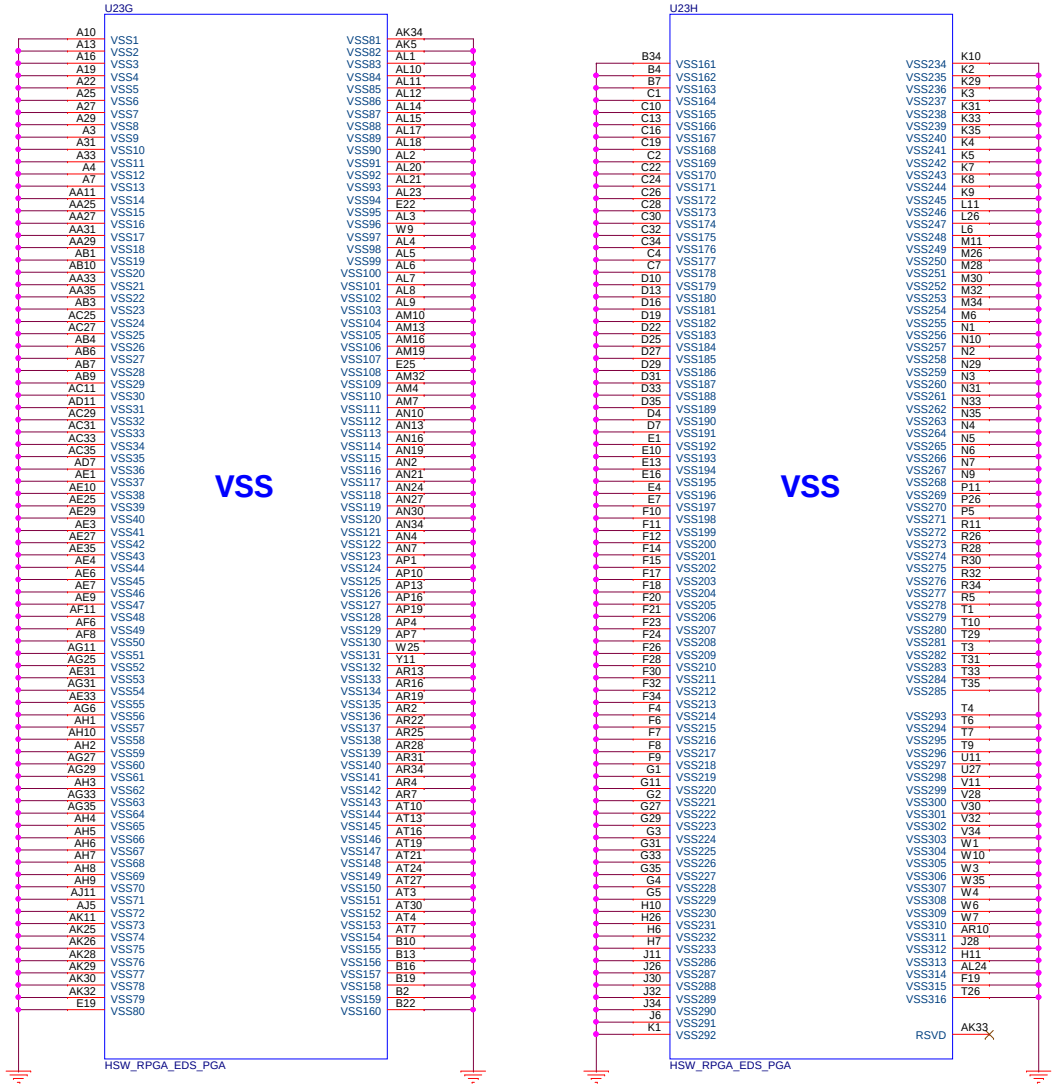
NB5

PROJECT : TWS
Quanta Computer Inc.

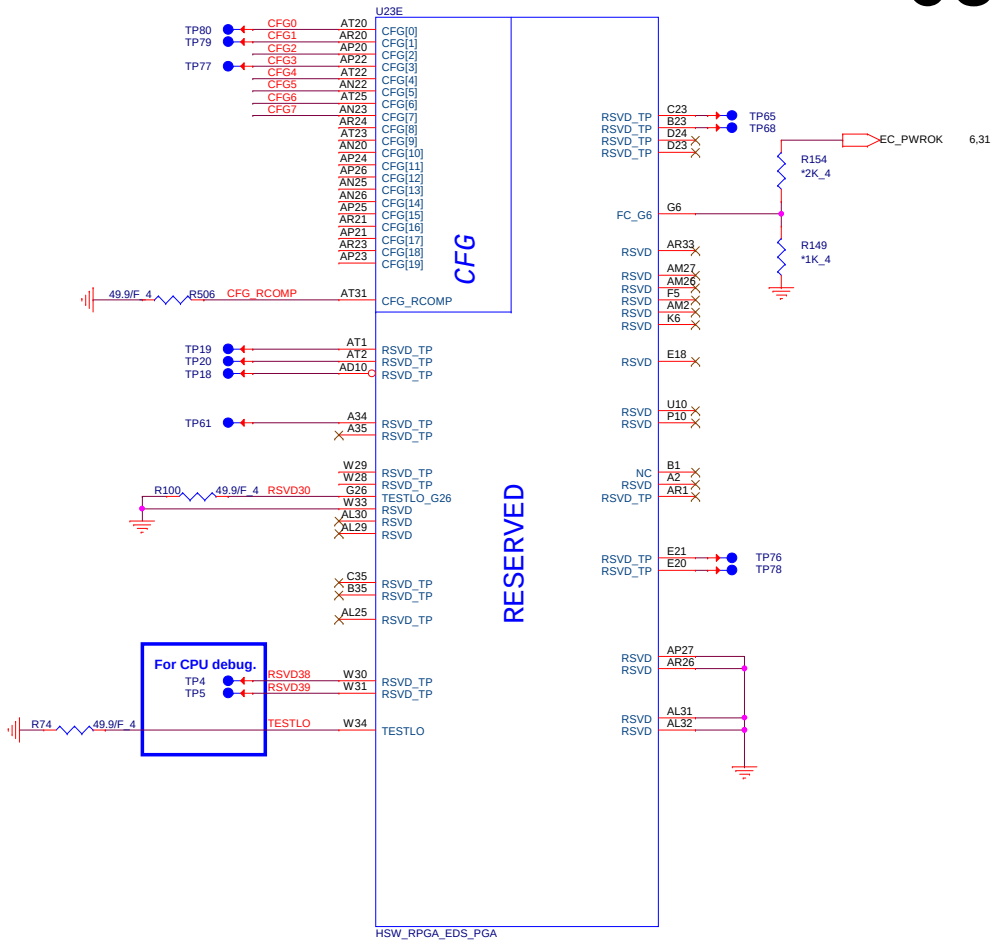
Size	Document Number	Rev
Custom	HAS 3/4 (POWER)	1A

Date: Friday, August 16, 2013 Sheet 4 of 43

Haswell Processor (GND)



Haswell Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

CFG3 R524 *1K_4

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG2 R534 *1K_4
CFG4 R533 1K_4
CFG7 R523 *1K_4
CFG5 R530 1K_4
CFG6 R518 *1K_4

NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HAS 4/4 (GND)	1A

Date: Friday, August 16, 2013 Sheet 5 of 43

Lynx Point (DMI,FDI,PM)

Lynx Point (DDI)

06

U25C

U25D

DMI

FDI

System Power Management

LVDS

CRT

Digital Display Interface

INT. HDMI

5/16 for DS3

for DS3

PD Res place close to PCH

PCH to Res routeing 37.5 ohm Impedance.
Res to connector filter routeing 50ohm Impedance.

DG V0.7 -> 33 ohm
SCH V0.7 -> 0 ohm

DAC_IREF (50ohm)
Trace length < 500 MILS
Trace spacing = 30 MILS

Reserve from EMI request

Reserve for power on sequence

PCH Nut: QCI P/N: MBUL1001010 (Location:H13,H14)

LPT_PCH_M_EDS/BGA

PCH Pull-high/low(CLG)

for DS3

EDS V0.7 -> BATLOW# is in SUS well
SCH V0.7 -> BATLOW# pull up to DS3 power

DG V0.7 say that PWRBTN# is internal pulled-up in PCH to 3.3 V DSW through a weak pull-up resistor (24 kΩ nominal)

System PWR_OK(CLG)

INT HDMI Detect Function

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

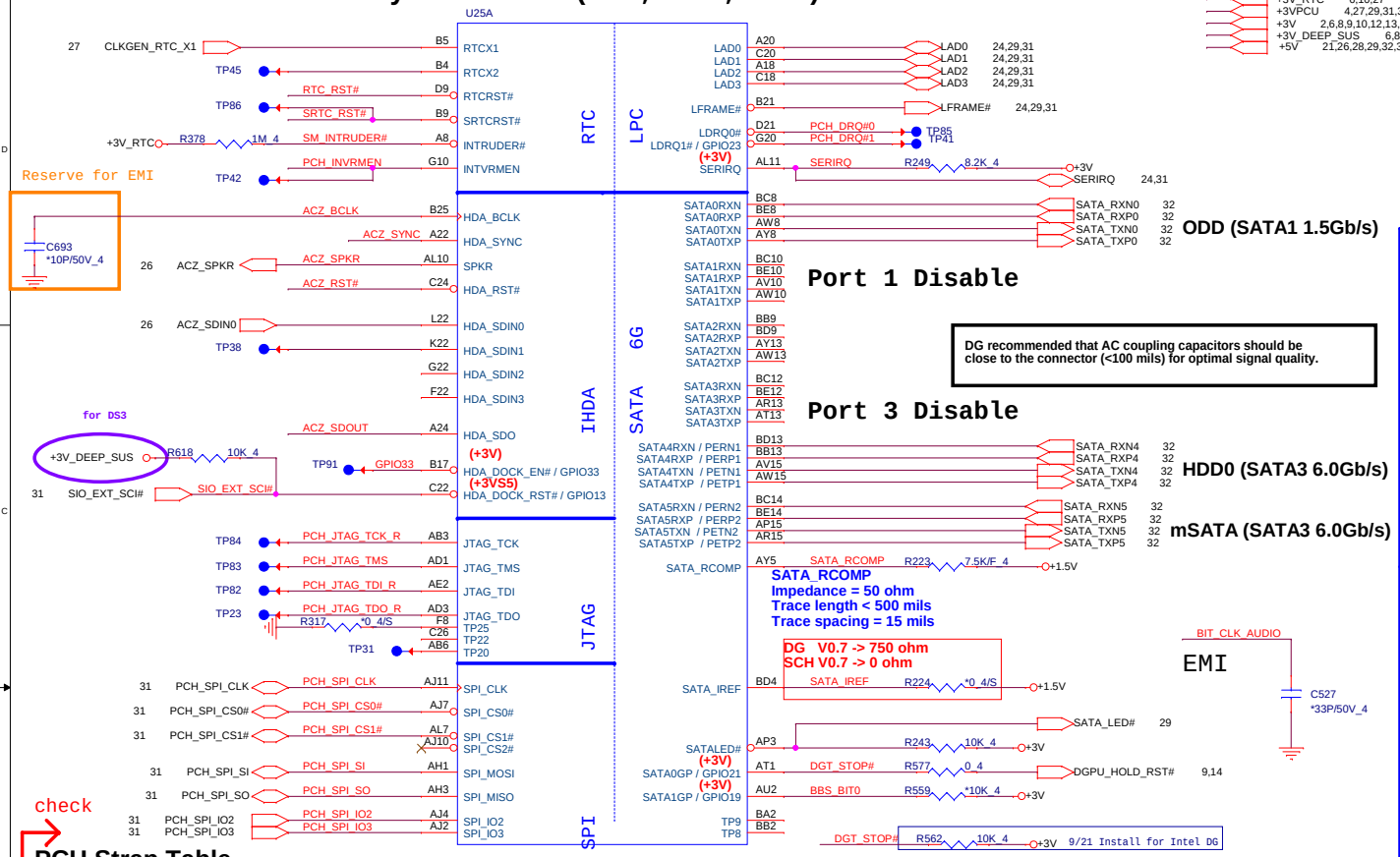
PROJECT : TWS
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A

Date: Friday, August 16, 2013 Sheet 6 of 43

Lynx Point (HDA,JTAG,SATA)



+1.05V 2,4,9,10,27,35,42
+3V_RTC 6,10,27
+3VPCU 4,27,29,31,32,33,34
+3V 2,6,8,9,10,12,13,14,17,21,22,23,24,25,26,28,29,30,31,32,37,38,40
+3V_DEEP_SUS 6,8,9,10,29
+5V 21,26,28,29,32,37,40

PCH Strap Table

LPT_PCH_M_EDS/BGA

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R269 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (Int PU)	R267 *1K_4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Disable 1 = Enable	PCH_INVRMEN R346 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0; GNT0# 1 0; Boot Location SPI LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1# R565 *1K_4 BBS_BIT0 R622 *1K_4 BBS_BIT1 8
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R619 *1K_4 ACZ_SYNC +3V power leakage in S3 AC mode: Please always remove pull high. (Intel release document: 已經有做strap pin) 2012/12/17
HDA_SDO	Flash Descriptor Security	PWROK	0 = Security Effect (Int PD) 1 = Can be Overridden	31 GPIO33_E ACZ_SDOUT R617 *1K_4 +VCC_HDA_IO
GPIO8	RSVD	RSMRST#	Internel PU	R595 *1K_4 BT_OFF# 9,29
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Int PU)	R598 *1K_4 PLL_ODVR_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R256 *1K_4 +3V
SUSCLK / GPIO62	On-die PLL Voltage Regulator	PWROK	0 = Disable 1 = Enable (Int PU)	6 PCH_SUSCLK_L R315 *1K_4 R310 *1K_4 +3V

RTC Clock 32.768KHz

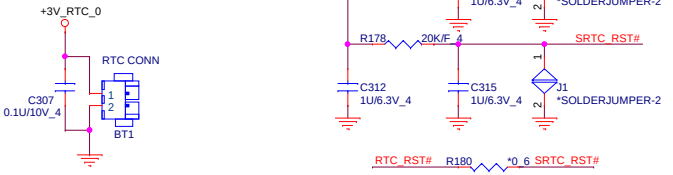
07

CB USE GREEN CLK

RTC Circuitry(RTC)

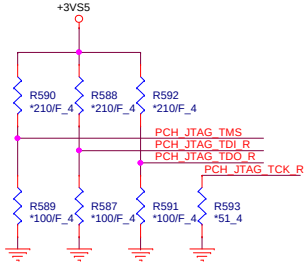
RTC Power trace width 20mils.

30mils



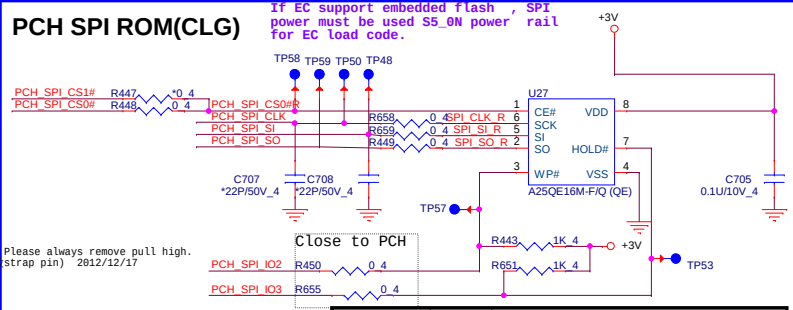
HDA Bus(CLG)

PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)

If EC support embedded flash , SPI power must be used S5_ON power rail for EC load code.



Vender	Size	P/N
AMIC	2MB	AKE38ZN0803 (A25QE16M-F/Q (QE))
WIN	2MB	AKE38FP0N03 (W25Q16DVSSIQ)
Socket		DFHS08FS023

NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

Date: Friday, August 16, 2013 Sheet 7 of 43

Lynx Point (PCI,USB,NVRAM)

Lynx Point (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

USB3.0

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

PCIE Clock

SMBus/Pull-up(CLG)

Reserve SMT_INT# for JW3.

check

MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

7/4: GPIO14 change netname to RF_PWR_OFF# for CB

7/4: 33MHz for CB TPM

4/30: CRB 1.0 =>rename PCH_TP26

10/23 EMI Jerry Change C534 C535 from 22P(CH02206JB08) to 18P(CH01806JB07)

CLOCK TERMINATION for FCIM

Remove for UMA only.

+1.05V	2,4,9,10,27,35,42
+1.5V	6,7,10,26,29,32,36
+3VS5	2,6,7,9,10,24,27,28,29,31,34,36,37,42
+3V	2,6,7,9,10,12,13,14,17,21,22,23,24,25,26,28,29,30,31,32,37,38,40
+3V_DEEP_SUS	6,7,9,10,29

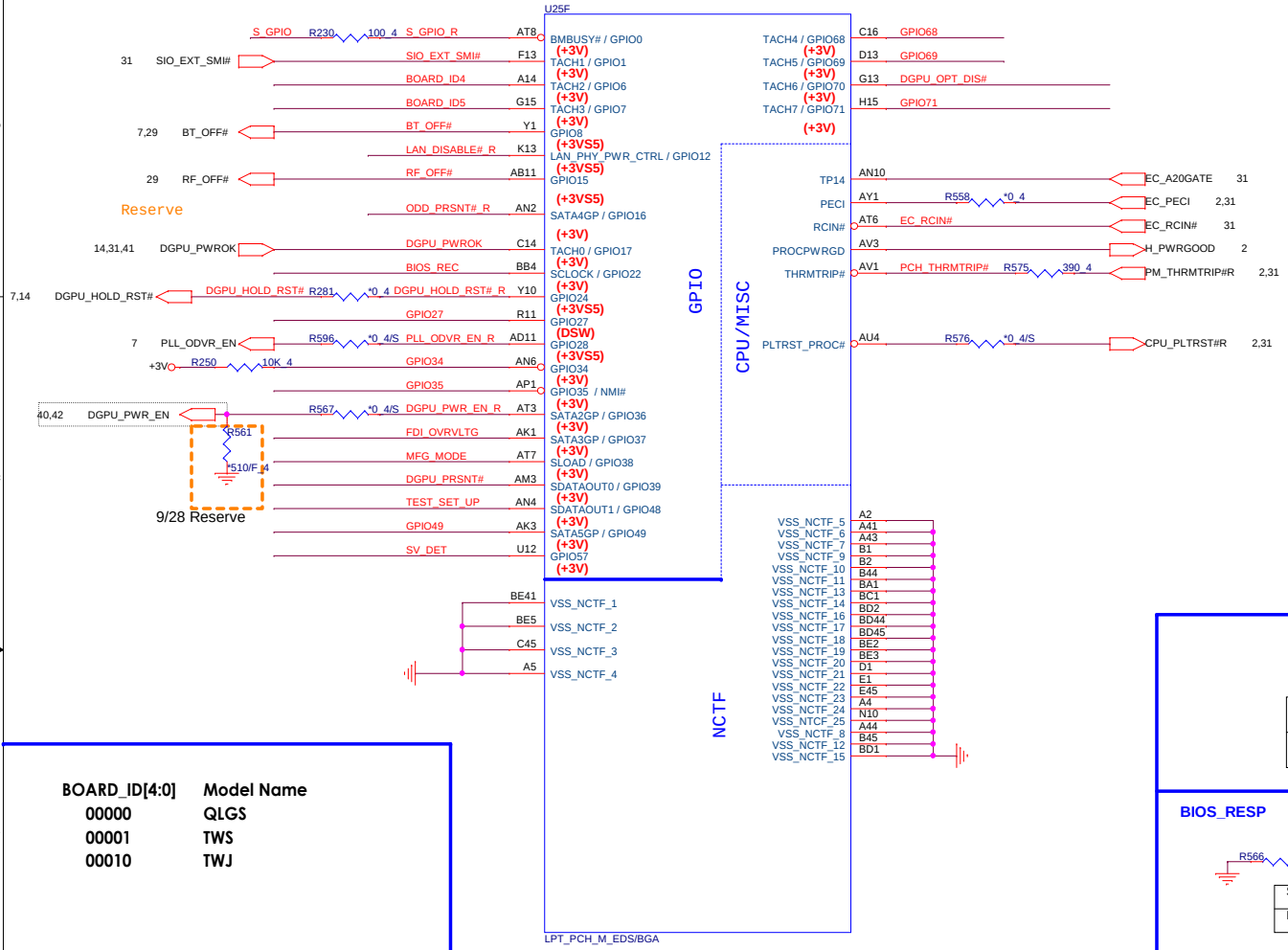
PROJECT : TWS
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	1A

Date: Friday, August 16, 2013 Sheet 8 of 43

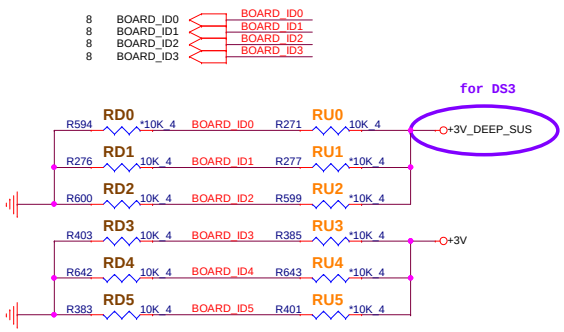
Lynx Point (GPIO,VSS_NCTF,RSVD)



BOARD_ID[4:0]	Model Name
00000	QLGS
00001	TWS
00010	TWJ

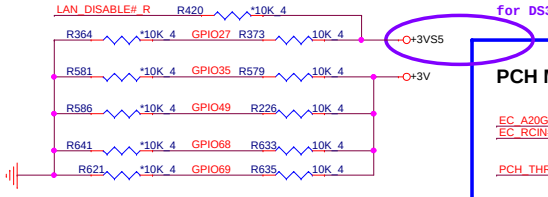
HSW BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO45	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO4	MODEL BIT3
BOARD_ID4	GPIO6	MODEL BIT4
BOARD_ID5	GPIO7	No Dolby=0, Dolby=1
GPIO71	GPIO71	Reserve
GPIO35	GPIO35	Reserve
GPIO49	GPIO49	Reserve
GPIO68	GPIO68	Reserve
GPIO69	GPIO69	Reserve
DGPU_PRSNT	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

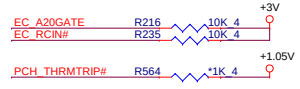


GPIO068	Hi	Lo
	LVDS interface	eDP interface

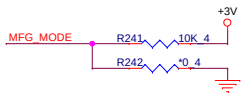
+3V_DEEP_SUS 6,7,8,10,29
+3VS5 2,6,7,10,24,27,28,29,31,34,36,37,42
+3V 2,6,7,8,10,12,13,14,17,21,22,23,24,25,26,28,29,30,31,32,37,38,40
+5VS5 26,27,28,34,35,36,37,38,39,40,41



PCH MISC PU /PD

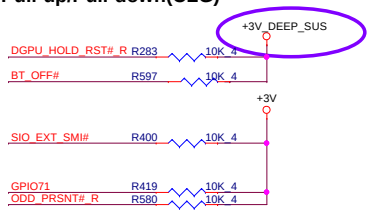


MFG-TEST



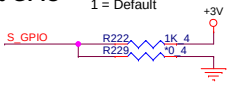
GPIO Pull-up/Pull-down(CLG)

for DS3

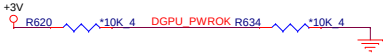


Swap GPIO

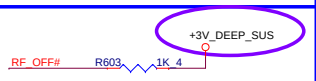
0 = SGPIO
1 = Default



DGPU_PWROK UMA=0



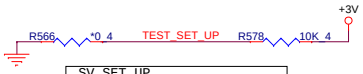
for DS3



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable

BIOS RECOVERY	High = Disable (Default) Low = Enable

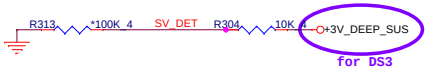
BIOS_RESP



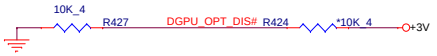
SV_SET_UP
High = Strong (Default)

SV Detect

0 = SV Detect
1 = Default



DGPU_OPT_DIS# GPIO70 Optimus=0, Dis only=1



SATA3GP/GPIO37 TLS Confidentiality

0 = TLS no confidentiality (Int PD)
1 = TLS with confidentiality

GFX Present GPIO39 Optimus=1, UMA=0

	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

GPIO36 Internal PD

NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A
Date: Friday, August 16, 2013	Sheet 9 of 43	

Lynx Point (POWER)

+3V 2,6,7,8,9,12,13,14,17,21,22,23,24,25,26,28,29,30,31,32,37,38,40
+3V_DEEP_SUS 6,7,8,9,29
+5VS5 26,27,28,34,35,36,37,38,39,40,41
+5V 21,26,28,29,32,37,40

+VCCIO_PCH 4
+1.05V 2,4,9,27,35,42
+1.5V 6,7,8,26,29,32,36
+3VS5 2,6,7,9,24,27,28,29,31,34,36,37,42

Lynx Point (POWER)

POWER

U25J

0.15A (20mils)
+1.05V +VCCAXCK_VRM_R +VCCAXCK_VRM
R237 *1/F_4 L22 *10uH/100MA_8
+1.5V R200 *0_8/S
C340 10U/6.3V_6
AF34 VCCVRM[5]

+VCC_AXCK_DCB +V1.05S_VCC_AXCK_DCB
+1.05V R246 *0_8/S L26 0_6
AP45 VCC[3]
1.09A (40mils)
C379 *10U/6.3V_6 C378 1U/6.3V_4

50mA (10mils)
+3V R374 *0_8/S 1U/6.3V_4 C516 +V3.3S_VCC_FLEX0 M29 VCCCLK3_3[1]
+3V R371 *0_8/S 1U/6.3V_4 C467 +V3.3S_VCC_FLEX1 L29 VCCCLK3_3[2]
+3V R370 *0_8/S 1U/6.3V_4 C454 +V3.3S_VCC_FLEX23 L26 VCCCLK3_3[3]
M26 VCCCLK3_3[4]
+3V R354 *0_8/S 1U/6.3V_4 C440 +V3.3S_VCC_ASEPCI U32 VCCCLK3_3[5]
V32 VCCCLK3_3[6]

+V1.05S_VCC_SSCFF
0.3A (20mils)
+1.05V R355 *0_8/S 1U/6.3V_4 C509 Y32 VCCCLK[1]
+VCCCLKF135
+1.05V R284 *0_8/S 1U/6.3V_4 C418 AD34 VCCCLK[2]
+V1.05S_VCC_SSCFF AA30 VCCCLK[3]
AA32 VCCCLK[4]
+V1.05S_VCCCLKF100
+1.05V R309 *0_8/S 1U/6.3V_4 C455 AD35 VCCCLK[5]
+V1.05S_VCCSSCF100
+1.05V R272 *0_8/S 1U/6.3V_4 C401 AG30 VCCCLK[6]
AG32 VCCCLK[7]
+V1.05S_VCCCLKF100 AD36 VCCCLK[8]
+V1.05S_VCCSSCF100 AE30 VCCCLK[9]
AE32 VCCCLK[10]

0.15A (20mils)
+1.5V R227 *0_8/S +V1.5S_VCCATS AW40 VCCVRM[6]
0.13A (20mils)
+3V R322 *0_8/S 0.1U/10V_4 C487 +V3.3S_VCCPTS AK30 VCC3_3[7]
AK32 VCC3_3[8]

4mA (10mils)
+VCCIO_PCH *0_8/S R556 +V1.05S_VCCPCPU
C682 0.1U/10V_4
C683 0.1U/10V_4
C681 1U/6.3V_4
AJ12 V_PROC_IO[1]
AJ14 V_PROC_IO[2]

for DS3
0.261A (40mils)
+3V_DEEP_SUS *0_8/S R353 +VCCPRTCSUS_3P3 K8 VCCSUS3_3[9]
1U/6.3V_4 C504
+3V_RTC A6 VCCRTC
0.1U/10V_4 C512
0.1U/10V_4 C508
1U/6.3V_4 C513
0.1U/10V_4 C453 +VCCRTCEXT
P14 DCPRTC[1]
P16 DCPRTC[2]

LPT_PCH_M_EDS/BGA

Clock and Miscellaneous
USB
GPIO/LPC
FUSE
THERMAL
CPU
SATA
RTC
HDA

0.26A (40mils)
VCCSUS3_3[3] R24 +V3.3A_VCCPUSB R372 *0_8/S +3V_DEEP_SUS
VCCSUS3_3[4] R26 0.1U/10V_4 C452
VCCSUS3_3[5] R28
VCCSUS3_3[6] U26
for DS3

VCCUSBPLL U35 +V1.05S_VCCAUSB 0.1U/10V_4 C476 R325 *0_8/S +1.05V
VCC3_3[3] L24 +V3.3S_VCCAUBG 0.1U/10V_4 C466 R369 *0_8/S +3V
VCCIO[11] U30
VCCIO[12] V28
VCCIO[13] V30
VCCIO[14] Y30 +V1.05S_VCCUSBCORE 1U/6.3V_4 C441 R305 *0_8/S +1.05V
3.629A (160mils)
VSS M24
DCPSUS2 Y35 +V1.05M_VCCDUSBSUS *1U/6.3V_4 C445
28mA (10mils)

0.26A (40mils)
VCCSUS3_3[7] R20 +3V_DEEP_SUS
VCCSUS3_3[8] R22
15mA (10mils)
VCCDSW3_3 A16 +VCCPDSW R349 *0_6/S +3VS5
for DS3
C496 0.1U/10V_4
VCC3_3[4] AE14 +V3.3S_VCCPCORE R557 *0_8/S +3V
VCC3_3[5] AF12
VCC3_3[6] AG14 0.01U/25V_4 C684

VCCIO[15] U36 +V1.05S_VCCAUX R318 *0_8/S +1.05V
DCPSST AA14 +VCCSST 0.1U/10V_4 C404

VCC[1] P18 +V3.3S_VCCPFUSE R390 *0_8/S +3V
VCC[2] P20 R412 *0_6 +1.05V
1U/6.3V_4 C524
VCCASW[12] L17 PCH_VCC_1_1_20 R294 *0_6/S +1.05V
VCCASW[13] R18 PCH_VCC_1_1_21 R289 *0_6/S +1.05V

PCH VRM Power
+V1.05S_VCCAPLL_SATA3
VCCVRM[7] AN11 *10uH/100MA_8 L20 +1.05V
*0_8/S R198 +1.5V
*10U/6.3V_6 C333
VCCIO[16] AK22 +V1.05S_VCC_EXP
3.629A (160mils)

10mA (10mils)
+VCC_HDA_IO
VCCSUSHDA A26 *0_6/S R638 +3V_DEEP_SUS
0.1U/10V_4 C692
for DS3

+3V_DEEP_SUS
for DS3
C546 0.1U/10V_4

PCH band gap Power
+3VS5 Q27 *2N7002 +3V_BG
3 1
2
37 MAIND

POWER

U25G

1.29A (60mils)
+V1.05S_PCH_VCC
1U/6.3V_4 C403
1U/6.3V_4 C410
1U/6.3V_4 C417
10U/6.3VS_6 C400
VCCCORE[1] AA24
VCCCORE[2] AA26
VCCCORE[3] AD20
VCCCORE[4] AD22
VCCCORE[5] AD24
VCCCORE[6] AD26
VCCCORE[7] AD28
VCCCORE[8] AE18
VCCCORE[9] AE20
VCCCORE[10] AE22
VCCCORE[11] AE24
VCCCORE[12] AE26
VCCCORE[13] AG18
VCCCORE[14] AG20
VCCCORE[15] AG22
VCCCORE[16] AG24
VCCCORE[17] Y26
VCC CORE

0.67A (40mils)
+1.05V +V1.05M_VCCASW
C459 1U/6.3V_4
C432 1U/6.3V_4
C366 22U/6.3VS_6
VCCASW[1] AA18
VCCASW[2] U18
VCCASW[3] U20
VCCASW[4] U22
VCCASW[5] U24
VCCASW[6] V18
VCCASW[7] V20
VCCASW[8] V24
VCCASW[9] Y18
VCCASW[10] Y20
VCCASW[11] Y22
VCCASW[12] V22

1U/6.3V_4 C407 R280 5.11/F_4 +PCH_VCCDSW U14
3.629A (160mils) +V1.05S_VCC_EXP
DCPSUSBYP

VCCIO[1] AM18
VCCIO[2] AM20
VCCIO[3] AM22
VCCIO[4] AP22
VCCIO[5] AR22
VCCIO[6] AT22
VCCMPHY

0.261A (40mils)
+3V_DEEP_SUS +3V_DEEP_SUS
0.098A (20mils)
*1U/6.3V_4 C391 +VCCA_USBSUS AJ26
*10U/6.3V_6 C402 AJ28
DCPSUS3_3[1]
DCPSUS3_3[2]
VCCSUS3_3[1] AJ30
VCCSUS3_3[2] AJ32

PCH VRM Power
+1.05V +1.5V L18 *10uH/100mA_8 +VCCAPLL_USB3 AK26
*10U/6.3V_6 C341 0.476A (30mils) AK28
VCCVRM[1]
VCCVRM[2]
+V1.05S_VCC_EXP AK20
*1U/6.3V_4 C435 +V1.05M_VCCSUS Y12
98mA (15mils)
DCPSUS1

PCH VRM Power
+1.05V +1.5V L24 *1uH/25mA_6 +V1.05S_VCCAPLL_FDI BB44
R225 *0_8/S *10U/6.3V_6 C359
0.179A (20mils)
VCCVRM[3]
+V1.05S_VCC_EXP AN34 VCCIO[8]
3.629A (160mils) AN35 VCCIO[9]

USB3
DMI / PCIE
HVCMOS
CRT
SPI
FDI

LPT_PCH_M_EDS/BGA

+VCCA_DAC_1_2 +1.5V
70mA (15 mils)
L28 HCB1608KF-181T15/1.5A_6
VCCADAC1_5 P45
C409 10U/6.3V_6
C430 0.1U/10V_4
C431 0.01U/25V_4
VSS P43 R288 *0_6
R282 *0_8 +1.5V_LDO

13mA (10mils)
VCCADACBG3_3 M31 +V3.3S_ADACBG R615 *0_8/S +3V
R614 *0_8 +3V_BG

133mA (20mils)
VCC3_3[1] R30
VCC3_3[2] R32 +V3.3S_VCC_GIO R342 *0_8/S +3V
0.1U/10V_4 C457

PCH VRM Power
+V1.05S_VCCAPLL_EXP +1.05V
VCCVRM[4] BE22 L19 *1uH/25mA_6 +1.5V
*10U/6.3V_6 C345
VCCIO[10] AK18 +V1.05S_VCC_EXP
3.629A (160mils)

+V3.3M_VCCPSPI
VCCSPI AD12 R286 *0_8/S +3V
1U/6.3V_4 C413
22mA (10mils)

If EC support embedded flash , SPI power must be used S5_ON power rail for EC load code.

If have power noise issue then stuff it.
+3V +1.5V_LDO
C464 *1U/6.3V_4
U14 VIN VOUT EN GND NC
* G9090-150T11U

PCH VCCIO Power
+1.05V +V1.05S_VCC_EXP 3.629A (160mils)
Near Pin AN34,AN35
C372 10U/6.3V_6 C390 1U/6.3V_4 C361 1U/6.3V_4 C383 1U/6.3V_4 C387 1U/6.3V_4 C388 1U/6.3V_4

01/02: C Stage ADD
for DS3 function
+3VS5 +3VS5 +3V_DEEP_SUS
C932 1U/6.3V_4
R821 100K/F_4
Q66 AO3409
R834 100K/F_4
C933 .1U/10V_4
R823 22_8
10,31 SLP_SUS_ON R820 0_4
Q67A 2N7002KDW R833 0_4
C943 *1U/6.3V_4
C934 *1U/6.3V_4
Q67B 2N7002KDW

PCH DS3 PWR
+3VS5 +3V_DEEP_SUS
R423 *0_8
C550 *1U/6.3V_4
U19 IN IN ON/OFF OUT GND
10,31 SLP_SUS_ON SLP_SUS_ON
R422 *100K/F_4
*G5243AT11U

NB5

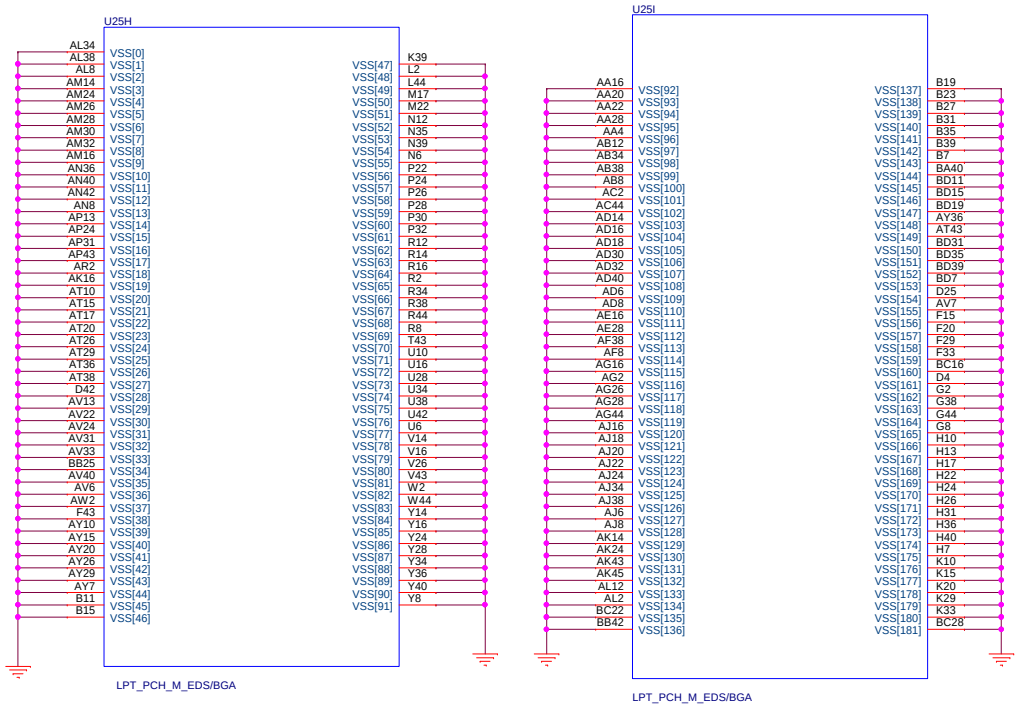
PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1A

Date: Friday, August 16, 2013 Sheet 10 of 43

SI change for DEEP S3

Lynx Point (GND)

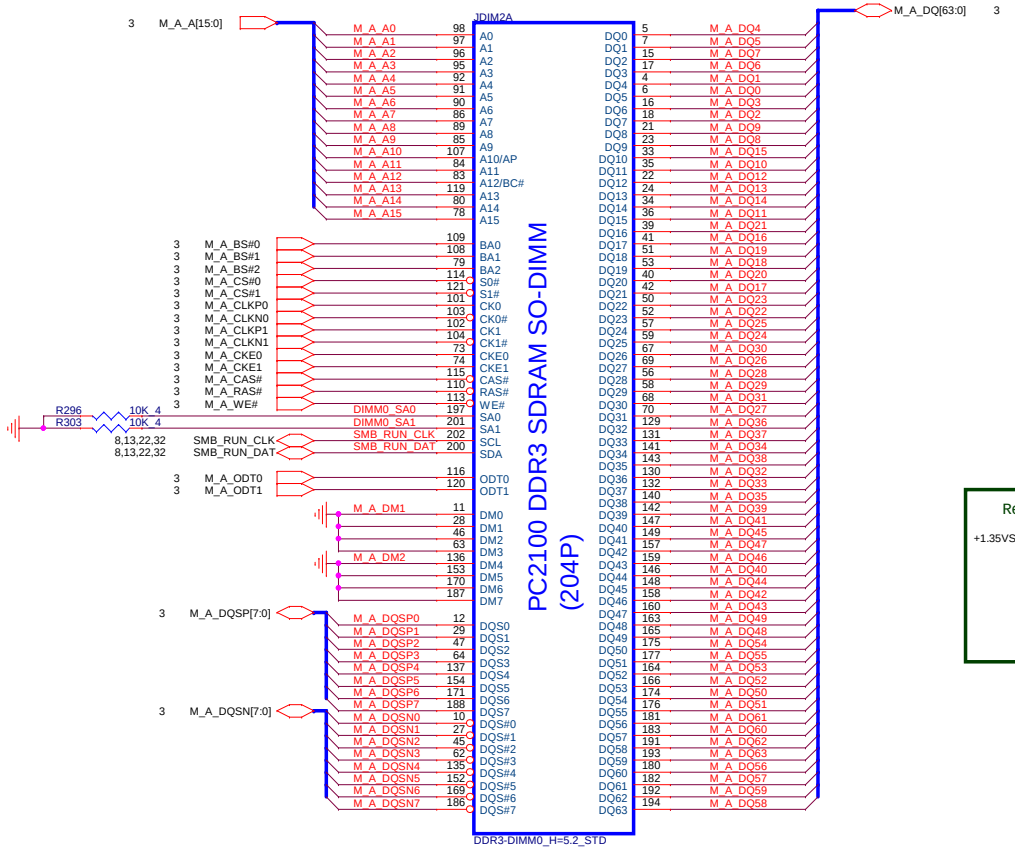


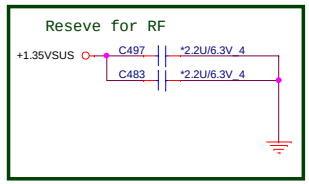
NB5

PROJECT : TWS
Quanta Computer Inc.

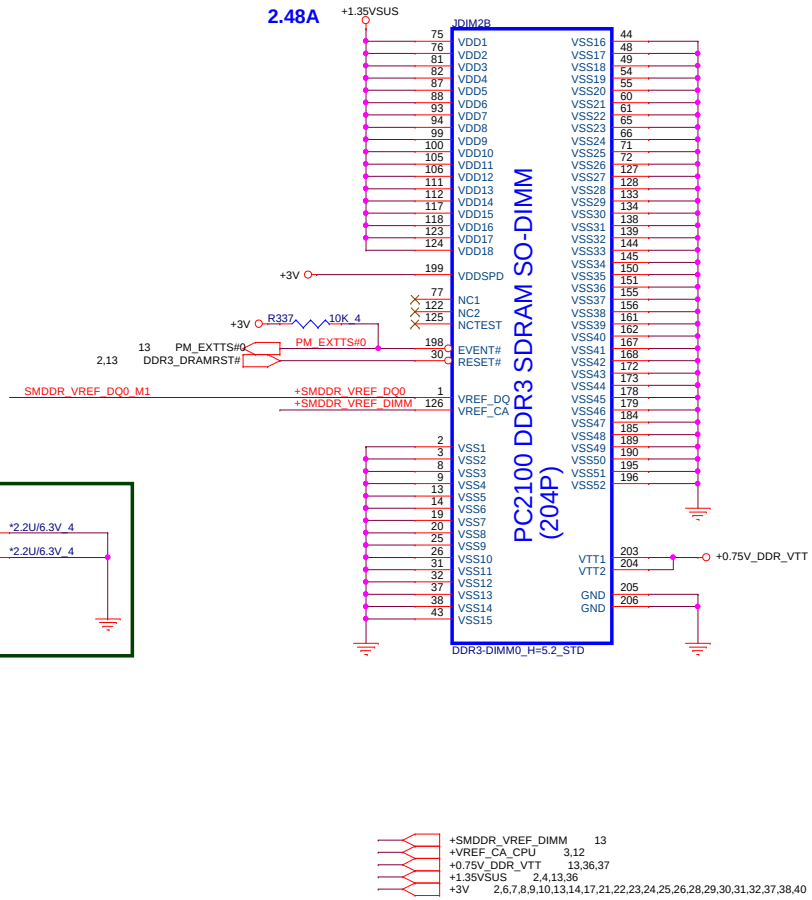
Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

Date: Friday, August 16, 2013 Sheet 11 of 43





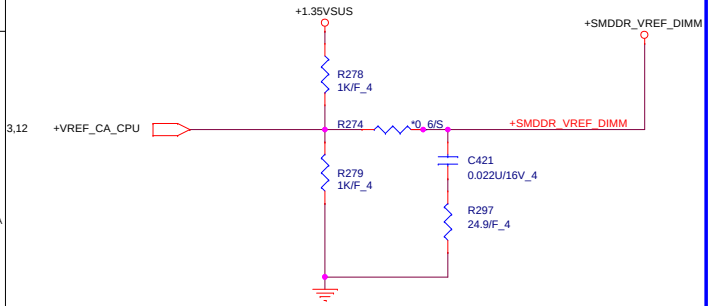
2.48A



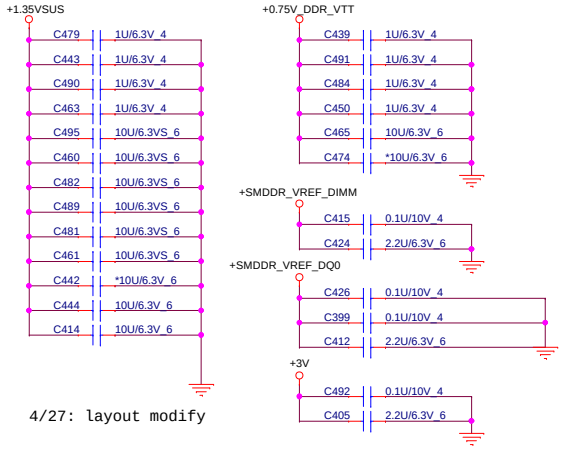
+SMDDR_VREF_DIMM 13
+VREF_CA_CPU 3,12
+0.75V_DDR_VTT 13,36,37
+1.35VSUS 2,4,13,36
+3V 2,6,7,8,9,10,13,14,17,21,22,23,24,25,26,28,29,30,31,32,37,38,40

+VREF_CA_CPU 3,12

10/4 : INTEL suggestion



Place these Caps near So-Dimm0.

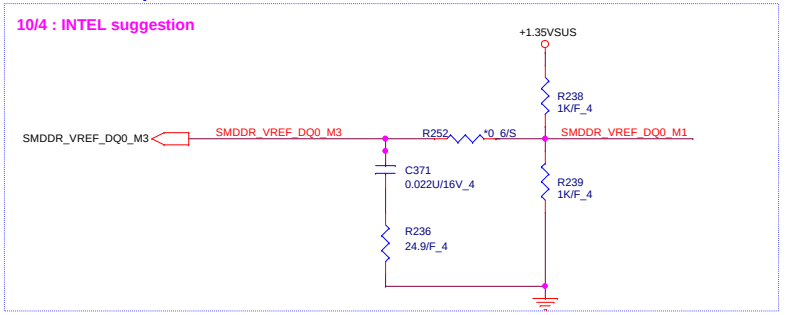


4/27: layout modify

VREF DQ0 M1 Solution

Place these Caps near So-Dimm0.

10/4 : INTEL suggestion

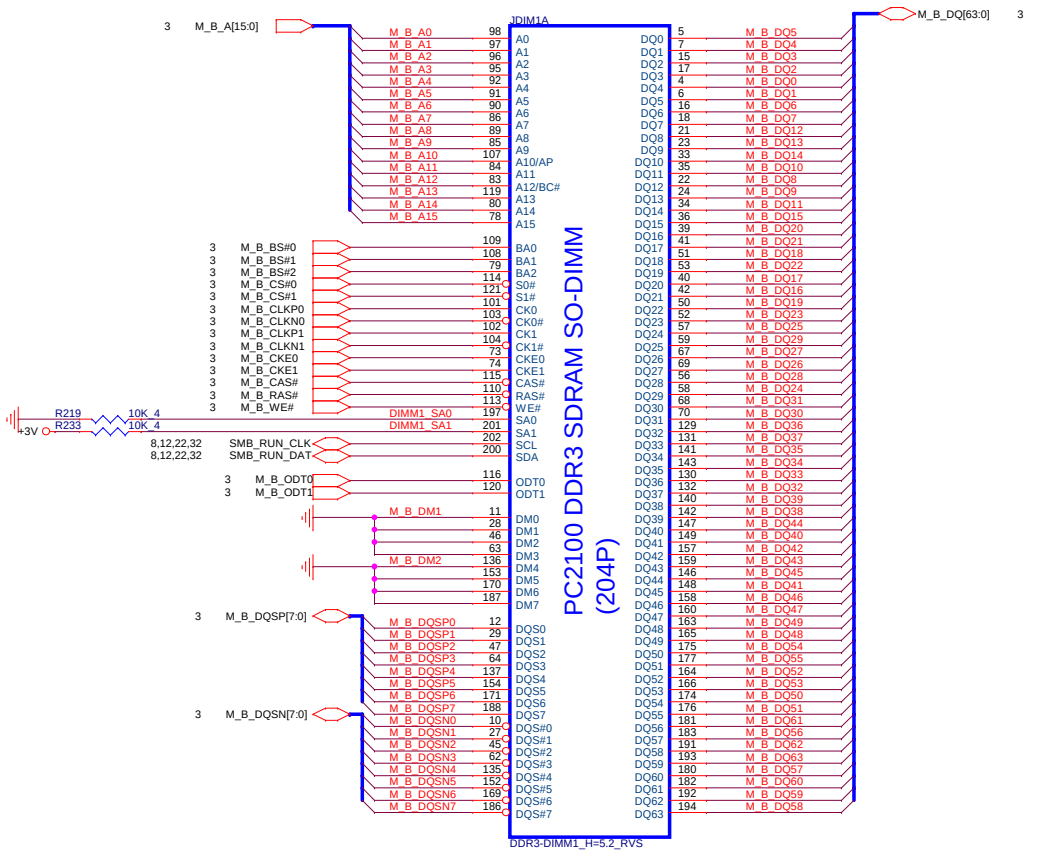


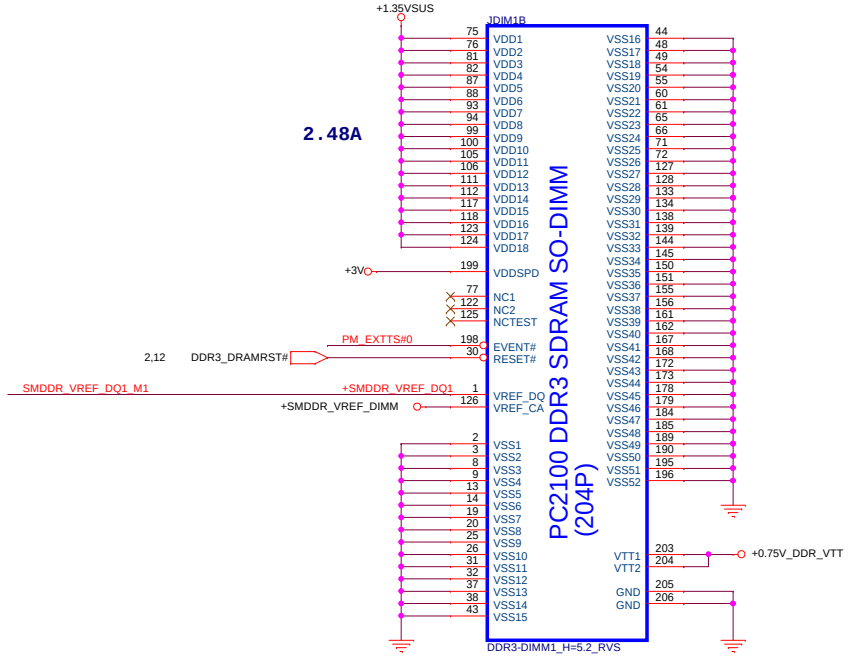
NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A

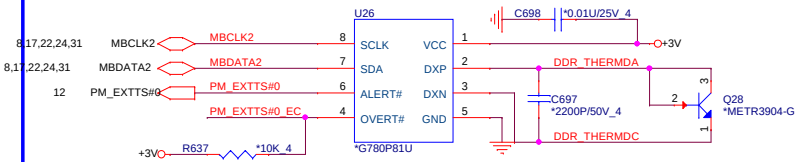
Date: Friday, August 16, 2013 Sheet 12 of 43



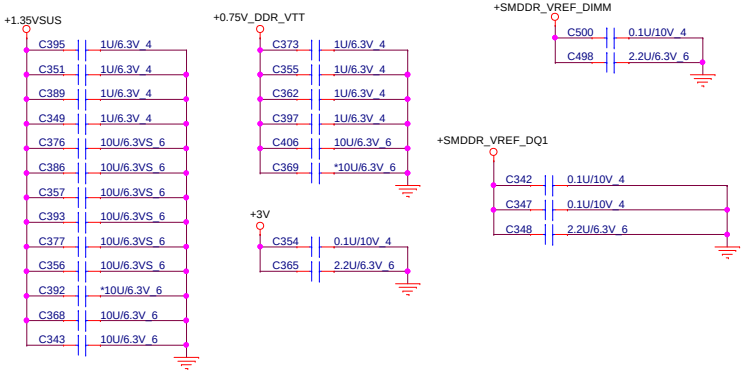


+0.75V_DDR_VTT 12,36,37
+1.35VSUS 2,4,12,36
+3V 2,6,7,8,9,10,12,14,17,21,22,23,24,25,26,28,29,30,31,32,37,38,40
+SMDDR_VREF_DIMM 12

DDR3 Thermal Sensor

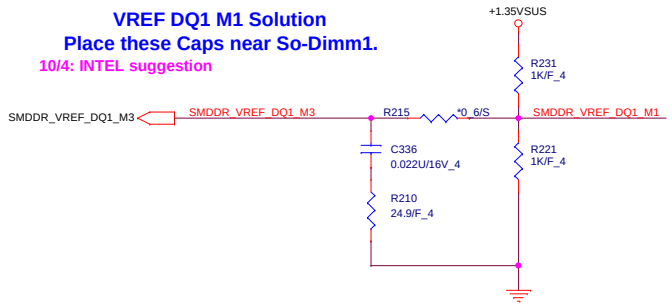


Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution
Place these Caps near So-Dimm1.

10/4: INTEL suggestion



NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A

Date: Friday, August 16, 2013 Sheet 13 of 43

U22A
N14M-GS

[PEG Interface]

PEX_IOVDD/Q : 3300mA

+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C109 22U/6.3VS_6
C105 22U/6.3VS_6
C101 22U/6.3VS_6
C102 22U/6.3VS_6
C158 10U/6.3VS_6
C160 10U/6.3VS_6
C110 10U/6.3VS_6
C113 10U/6.3VS_6

PLACE NEAR BALLS

C152 1U/6.3V_4
C162 1U/6.3V_4
C153 1U/6.3V_4
C154 1U/6.3V_4

PLACE UNDER BGA

C159 4.7U/6.3V_6
C156 4.7U/6.3V_6

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6

AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
AL27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13

VDD33 : 85mA

+3V_GFX

PLACE CLOSE TO BGA

C635 4.7U/6.3V_6
C616 2.2U/6.3V_4

PLACE CLOSE TO GPU BALLS

C226 1U/6.3V_4
C212 0.1U/10V_4
C202 0.1U/10V_4
C219 0.1U/10V_4

J8 VDD33_1
K8 VDD33_2
L8 VDD33_3
M8 VDD33_4

PEX_RX0 AN12 PEG_TX0 2
PEX_RX0_N AM12 PEG_TX#0 2
PEX_RX1 AN14 PEG_TX1 2
PEX_RX1_N AM14 PEG_TX#1 2
PEX_RX2 AP14 PEG_TX2 2
PEX_RX2_N AP15 PEG_TX#2 2
PEX_RX3 AN15 PEG_TX3 2
PEX_RX3_N AM15 PEG_TX#3 2
PEX_RX4 AN17 PEG_TX4 2
PEX_RX4_N AM17 PEG_TX#4 2
PEX_RX5 AP17 PEG_TX5 2
PEX_RX5_N AP18 PEG_TX#5 2
PEX_RX6 AN18 PEG_TX6 2
PEX_RX6_N AM18 PEG_TX#6 2
PEX_RX7 AN20 PEG_TX7 2
PEX_RX7_N AM20 PEG_TX#7 2
PEX_RX8 AP20
PEX_RX8_N AP21
PEX_RX9 AN21
PEX_RX9_N AM21
PEX_RX10 AN23
PEX_RX10_N AM23
PEX_RX11 AP23
PEX_RX11_N AP24
PEX_RX12 AN24
PEX_RX12_N AM24
PEX_RX13 AN26
PEX_RX13_N AM26
PEX_RX14 AP26
PEX_RX14_N AP27
PEX_RX15 AN27
PEX_RX15_N AM27

PEX_TX0 AK14 C_PEG_RX0 C116 0.22U/10V_4 PEG_RX0 2
PEX_TX0_N AJ14 C_PEG_RX#0 C115 0.22U/10V_4 PEG_RX#0 2
PEX_TX1 AH14 C_PEG_RX1 C112 0.22U/10V_4 PEG_RX1 2
PEX_TX1_N AG14 C_PEG_RX#1 C111 0.22U/10V_4 PEG_RX#1 2
PEX_TX2 AK15 C_PEG_RX2 C118 0.22U/10V_4 PEG_RX2 2
PEX_TX2_N AJ15 C_PEG_RX#2 C117 0.22U/10V_4 PEG_RX#2 2
PEX_TX3 AL16 C_PEG_RX3 C119 0.22U/10V_4 PEG_RX3 2
PEX_TX3_N AK16 C_PEG_RX#3 C120 0.22U/10V_4 PEG_RX#3 2
PEX_TX4 AK17 C_PEG_RX4 C123 0.22U/10V_4 PEG_RX4 2
PEX_TX4_N AJ17 C_PEG_RX#4 C124 0.22U/10V_4 PEG_RX#4 2
PEX_TX5 AH17 C_PEG_RX5 C122 0.22U/10V_4 PEG_RX5 2
PEX_TX5_N AG17 C_PEG_RX#5 C121 0.22U/10V_4 PEG_RX#5 2
PEX_TX6 AK18 C_PEG_RX6 C127 0.22U/10V_4 PEG_RX6 2
PEX_TX6_N AJ18 C_PEG_RX#6 C128 0.22U/10V_4 PEG_RX#6 2
PEX_TX7 AL19 C_PEG_RX7 C125 0.22U/10V_4 PEG_RX7 2
PEX_TX7_N AK19 C_PEG_RX#7 C126 0.22U/10V_4 PEG_RX#7 2
PEX_TX8 AK20
PEX_TX8_N AJ20
PEX_TX9 AH20
PEX_TX9_N AG20
PEX_TX10 AK21
PEX_TX10_N AJ21
PEX_TX11 AL22
PEX_TX11_N AK22
PEX_TX12 AK23
PEX_TX12_N AJ23
PEX_TX13 AH23
PEX_TX13_N AG23
PEX_TX14 AK24
PEX_TX14_N AJ24
PEX_TX15 AL25
PEX_TX15_N AK25

PEX_REFCLK AL13 CLK_PCIE_VGA 8
PEX_REFCLK_N AK13 CLK_PCIE_VGA# 8

PEX_TSTCLK_OUT AJ26 PEX_TSTCLK R478 *200_4
PEX_TSTCLK_OUT_N AK26 PEX_TSTCLK#

PEX_WAKE AJ11
PEX_RST_N AJ12 VGA_RST# R477 *0_4/S PEGX_RST#

PEX_CLKREQ_N AK12 PEX_CLKREQ# R529 10K_4 +3V_GFX

PEX_TERMP AP29 PEX_TERMP R473 2.49K/F_4

TESTMODE AK11 TESTMODE R476 10K_4

PEX_PLLVDD AG26 PEX_PLLVDD

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12

PEX_SVDD_3V3 : 210mA
0.1U/10V_4 C155
4.7U/6.3V_6 C587
4.7U/6.3V_6 C106
PLACE NEAR BGA

+3V_GFX

3.3V_AUX_NC P8

VDD_SENSE L4 VGPU_CORE_SENSE 40

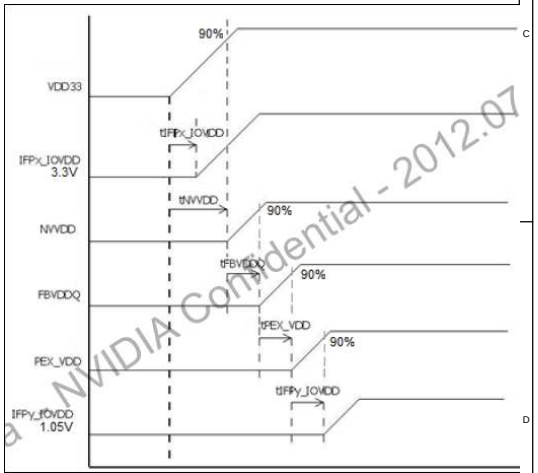
GND_SENSE L5 VSS_GPU_SENSE 40

+1.05V_GFX
R67 *0_6
L9 HCB1608KF-300T30
C114 4.7U/6.3V_6 PLACE NEAR BGA CLOSE TO CAPS
C130 1U/6.3V_4 PLACE UNDER BGA
C129 0.1U/10V_4 PLACE NEAR BALLS

+3V_GFX R539 4.7K_4 CLK_PEGA_REQ# 8
9,14,31,41 DGPU_PWROK
Q26 DTC144EUA
PEX_CLKREQ# Q25 *DTC144EUA
+3V
U6 MC74VHC1G08DFT2G
C244 0.1U/10V_4
2,8,24,25,29,30,31 PLTRST#
7,9 DGPU_HOLD_RST#
PEGX_RST# 17
R130 100K_4

+3V_GFX
+3V
R3006 *4.7K_4
4.7K_4 R3005
DGPU_PWROK 9,14,31,41
Q3003 DTC144EUA
R3007 100K/F_4
DGPU_PGOK-1
R3003 4.7K_4
+1.05V_GFX DGPU_POK4
Q3001 MMBT3904-7-F
C3003 1000P/50V_4
C3001 *1000P/50V_4

For DGPU_PWROK sequence to early issue(B Stage)



17,18,42 +3V_GFX
15,18,19,20,41 +1.5V_GFX
15,16,42 +1.05V_GFX
2,6,7,8,9,10,12,13,17,21,22,23,24,25,26,28,29,30,31,32,37,38,40 +3V

NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
A3	N14M-GS - 1/5 (PCIE)	1A

Date: Friday, August 16, 2013 Sheet 14 of 43

U22B
N14M-GS
[MEMORY I/F A]

U22C
N14M-GS
MEMORY I/F C

PVBDDQ : 5000mA

PLACE CLOSE TO GPU BALLS

PLACE CLOSE TO BGA

PLACE NEAR BGA CLOSE TO CAPS

+FB_PLLAVDD : 62mA

PLACE CLOSE TO BALL

PROJECT : TWS
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	N14M-GS - 2/5 (Memory)	1A

Date: Friday, August 16, 2013 | Sheet 15 of 43

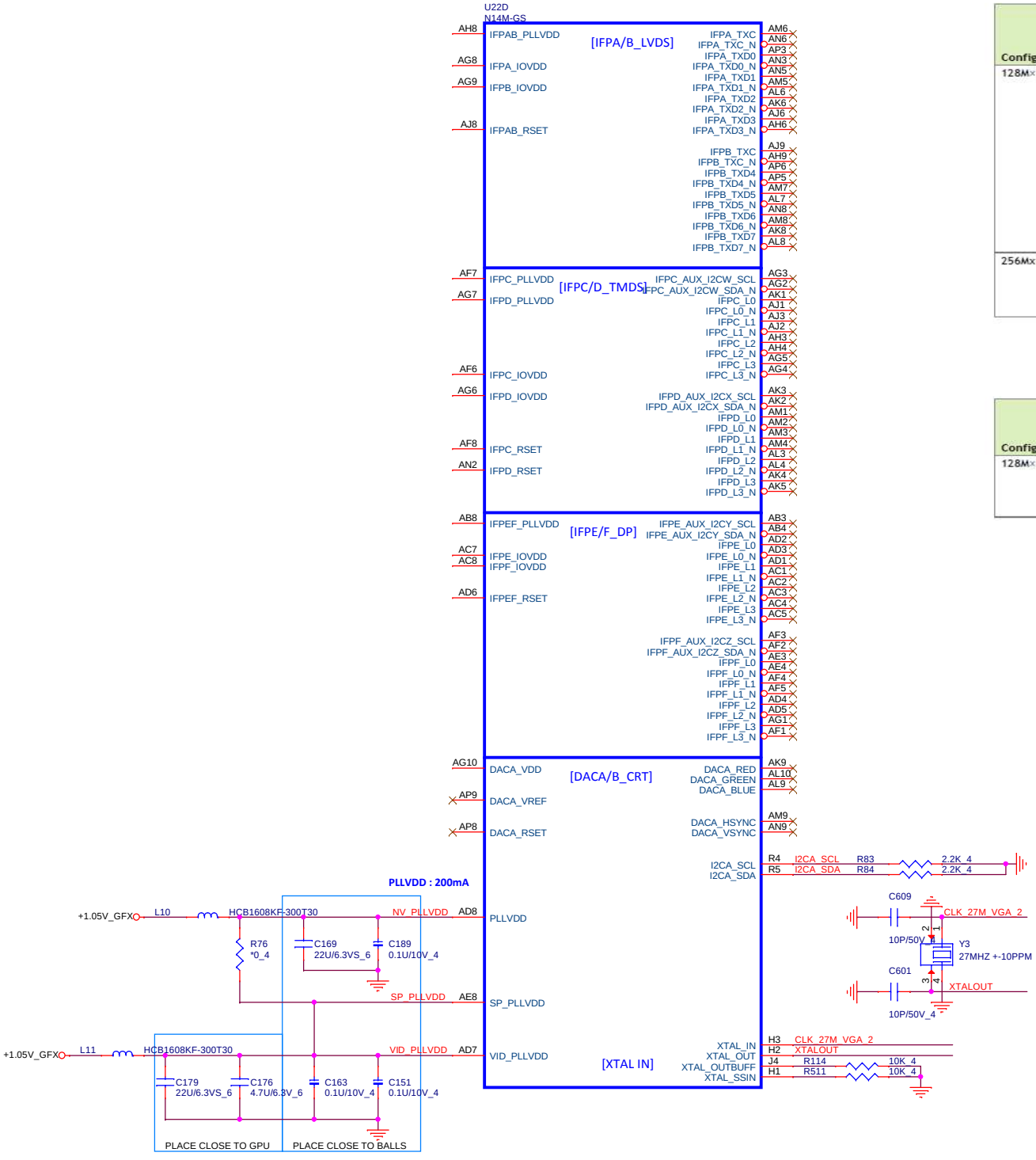


Table 3. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M×16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production Candidate
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production Candidate
				MT41J128M16JT-107G:K	900	1150	Production Candidate
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	N/A	Production Candidate
				H5TQ2G63DFR-11C	900	N/A	Production Candidate
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production Candidate
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production Candidate

Table 4. N14M-GS/LP and N14P-GV2 DDR3L Recommended Memories 128Mx16 Configuration.

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M×16 DDR3L	Samsung	0xA	1.35 V/ 1.35 V	K4W2G1646E-BY11	900	1204	Production Candidate
	Micron	0x8	1.35 V/ 1.35 V	MT41K128M16JT-107G:K	900	N/A	Production Candidate

Table 5. N14P-GS/LP/GE/GT DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M×16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production Candidate
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production Candidate
				MT41J128M16JT-107G:K	900	1150	Production Candidate
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	N/A	Production Candidate
				H5TQ2G63DFR-11C	900	N/A	Production Candidate
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production Candidate
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production Candidate

Table 6. N14P-GS/LP/GE/GT DDR3L Recommended Memories 128Mx16 Configuration.

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M×16 DDR3L	Samsung	0xA	1.35 V/ 1.35 V	K4W2G1646E-BY11	900	1204	Production Candidate
	Micron	0x8	1.35 V/ 1.35 V	MT41K128M16JT-107G:K	900	N/A	Production Candidate

NB5

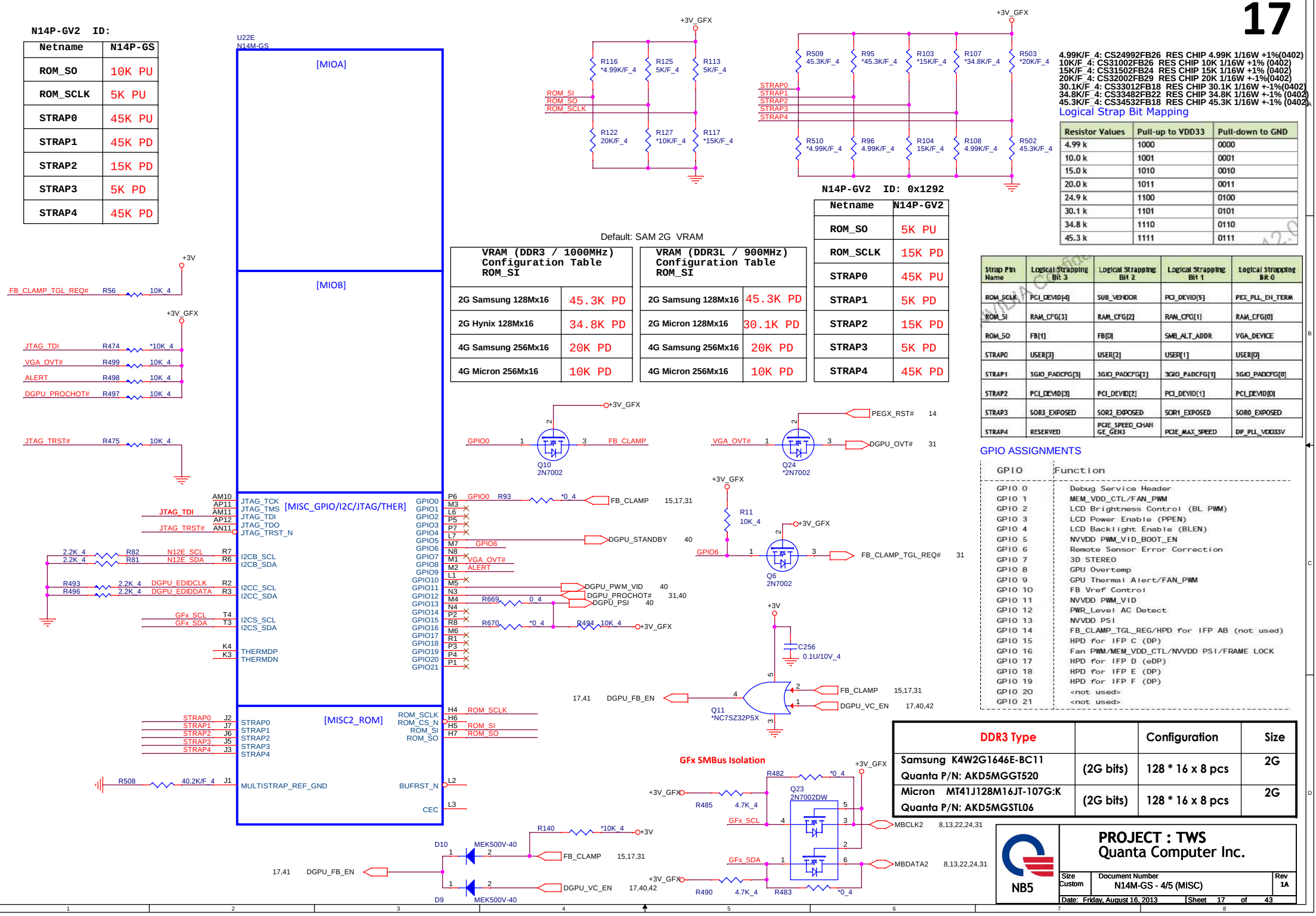
PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
A3	N14M-GS - 3/5 (Display)	1A

Date: Friday, August 16, 2013 Sheet 16 of 43

N14P-GV2 ID:

Netname	N14P-GS
ROM_SO	10K PU
ROM_SCLK	5K PU
STRAP0	45K PU
STRAP1	45K PD
STRAP2	15K PD
STRAP3	5K PD
STRAP4	45K PD



4.99K/F_4: CS24992FB26 RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
15K/F_4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
30.1K/F_4: CS33012FB18 RES CHIP 30.1K 1/16W +-1%(0402)
34.8K/F_4: CS33482FB22 RES CHIP 34.8K 1/16W +-1% (0402)
45.3K/F_4: CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

Logical Strap Bit Mapping

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

N14P-GV2 ID: 0x1292

Netname	N14P-GV2
ROM_SO	5K PU
ROM_SCLK	15K PD
STRAP0	45K PU
STRAP1	5K PU
STRAP2	15K PD
STRAP3	5K PD
STRAP4	45K PD

Default: SAM 2G VRAM

VRAM (DDR3 / 1000MHz) Configuration Table ROM_SI

2G Samsung 128Mx16	45.3K PD
2G Hynix 128Mx16	34.8K PD
4G Samsung 256Mx16	20K PD
4G Micron 256Mx16	10K PD

VRAM (DDR3L / 900MHz) Configuration Table ROM_SI

2G Samsung 128Mx16	45.3K PD
2G Micron 128Mx16	30.1K PD
4G Samsung 256Mx16	20K PD
4G Micron 256Mx16	10K PD

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	SGIO_PADCFG[3]	SGIO_PADCFG[2]	SGIO_PADCFG[1]	SGIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

GPIO ASSIGNMENTS

GPIO	Function
GPIO 0	Debug Service Header
GPIO 1	MEM_VDD_CTL/FAN_PWM
GPIO 2	LCD Brightness Control (BL PWM)
GPIO 3	LCD Power Enable (PPEN)
GPIO 4	LCD Backlight Enable (BLEN)
GPIO 5	NVVDD PWM_VID_BOOT_EN
GPIO 6	Remote Sensor Error Correction
GPIO 7	3D STEREO
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert/FAN_PWM
GPIO 10	FB Vref Control
GPIO 11	NVVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	NVVDD PSI
GPIO 14	FB_CLAMP_TGL_REG/HPD for IFP AB (not used)
GPIO 15	HPD for IFP C (DP)
GPIO 16	Fan PWM/MEM_VDD_CTL/NVVDD PSI/FRAME LOCK
GPIO 17	HPD for IFP D (eDP)
GPIO 18	HPD for IFP E (DP)
GPIO 19	HPD for IFP F (DP)
GPIO 20	<not used>
GPIO 21	<not used>

DDR3 Type		Configuration	Size
Samsung K4W2G1646E-BC11 Quanta P/N: AKD5MGGT520	(2G bits)	128 * 16 x 8 pcs	2G
Micron MT41J128M16JT-107G:K Quanta P/N: AKD5MGSTL06	(2G bits)	128 * 16 x 8 pcs	2G

NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N14M-GS - 4/5 (MISC)	1A

Date: Friday, August 16, 2013 Sheet 17 of 43

VDD/XVDD : 25.72A

+VGACORE

U22F
N14M-GS

[GPU VDD]

AA12	VDD_001	XVDD_001	U1
AA14	VDD_002	XVDD_002	U2
AA16	VDD_003	XVDD_003	U3
AA19	VDD_004	XVDD_004	U4
AA21	VDD_005	XVDD_005	U5
AA23	VDD_006	XVDD_006	U6
AB13	VDD_007	XVDD_007	U7
AB15	VDD_008	XVDD_008	U8
AB17	VDD_009	XVDD_009	V1
AB18	VDD_010	XVDD_010	V2
AB20	VDD_011	XVDD_011	V3
AB22	VDD_012	XVDD_012	V4
AC12	VDD_013	XVDD_013	V5
AC14	VDD_014	XVDD_014	V6
AC16	VDD_015	XVDD_015	V7
AC19	VDD_016	XVDD_016	V8
AC21	VDD_017	XVDD_017	W2
AC23	VDD_018	XVDD_018	W3
M12	VDD_019	XVDD_019	W4
M14	VDD_020	XVDD_020	W5
M16	VDD_021	XVDD_021	W7
M19	VDD_022	XVDD_022	W8
M21	VDD_023	XVDD_023	Y1
M23	VDD_024	XVDD_024	Y2
N13	VDD_025	XVDD_025	Y3
N15	VDD_026	XVDD_026	Y4
N17	VDD_027	XVDD_027	Y5
N18	VDD_028	XVDD_028	Y6
N20	VDD_029	XVDD_029	Y7
N22	VDD_030	XVDD_030	Y8
P12	VDD_031	XVDD_031	AA1
P14	VDD_032	XVDD_032	AA2
P16	VDD_033	XVDD_033	AA3
P19	VDD_034	XVDD_034	AA4
P21	VDD_035	XVDD_035	AA5
P23	VDD_036	XVDD_036	AA6
R13	VDD_037	XVDD_037	AA7
R15	VDD_038	XVDD_038	AA8
R17	VDD_039		
R18	VDD_040		
R20	VDD_041		
R22	VDD_042		
T12	VDD_043		
T14	VDD_044		
T16	VDD_045		
T19	VDD_046		
T21	VDD_047		
T23	VDD_048		
U13	VDD_049		
U15	VDD_050		
U17	VDD_051		
U18	VDD_052		
U20	VDD_053		
U22	VDD_054		
V13	VDD_055		
V15	VDD_056		
V17	VDD_057		
V18	VDD_058		
V20	VDD_059		
V22	VDD_060		
W12	VDD_061		
W14	VDD_062		
W16	VDD_063		
W19	VDD_064		
W21	VDD_065		
W23	VDD_066		
Y13	VDD_067		
Y15	VDD_068		
Y18	VDD_069		
Y17	VDD_070		
Y20	VDD_071		
Y22	VDD_072		

U22G
N14M-GS

[GPU GND]

A2	GND_1	GND_101	D2
AA17	GND_2	GND_102	D31
AA18	GND_3	GND_103	D33
AA20	GND_4	GND_104	E10
AA22	GND_5	GND_105	E22
AB12	GND_6	GND_106	E25
AB14	GND_7	GND_107	E5
AB16	GND_8	GND_108	E7
AB19	GND_9	GND_109	F28
AB2	GND_10	GND_110	F7
AB21	GND_11	GND_111	G10
A33	GND_12	GND_112	G13
AB23	GND_13	GND_113	G16
AB28	GND_14	GND_114	G19
AB30	GND_15	GND_115	G2
AB32	GND_16	GND_116	G22
AB5	GND_17	GND_117	G25
AB7	GND_18	GND_118	G28
AC13	GND_19	GND_119	G3
AC15	GND_20	GND_120	G30
AC17	GND_21	GND_121	G32
AC18	GND_22	GND_122	G33
AA13	GND_23	GND_123	G7
AC20	GND_24	GND_124	K2
AC22	GND_25	GND_125	K28
AE2	GND_26	GND_126	K30
AE28	GND_27	GND_127	K32
AE30	GND_28	GND_128	K33
AE32	GND_29	GND_129	K5
AE33	GND_30	GND_130	K7
AE5	GND_31	GND_131	M13
AE7	GND_32	GND_132	M15
AH10	GND_33	GND_133	M17
AA15	GND_34	GND_134	M18
AH13	GND_35	GND_135	M20
AH16	GND_36	GND_136	M22
AH19	GND_37	GND_137	N12
AH2	GND_38	GND_138	N14
AH22	GND_39	GND_139	N16
AH24	GND_40	GND_140	N19
AH28	GND_41	GND_141	N2
AH29	GND_42	GND_142	N21
AH30	GND_43	GND_143	N23
AH32	GND_44	GND_144	N28
AH33	GND_45	GND_145	N30
AH5	GND_46	GND_146	N32
AH7	GND_47	GND_147	N33
AJ7	GND_48	GND_148	N5
AK10	GND_49	GND_149	N7
AK7	GND_50	GND_150	P13
AL12	GND_51	GND_151	P15
AL14	GND_52	GND_152	P17
AL15	GND_53	GND_153	P18
AL17	GND_54	GND_154	P20
AL18	GND_55	GND_155	P22
AL2	GND_56	GND_156	R12
AL20	GND_57	GND_157	R14
AL21	GND_58	GND_158	R16
AL23	GND_59	GND_159	R19
AL24	GND_60	GND_160	R21
AL26	GND_61	GND_161	R23
AL28	GND_62	GND_162	T13
AL30	GND_63	GND_163	T15
AL32	GND_64	GND_164	T17
AL33	GND_65	GND_165	T18
AL5	GND_66	GND_166	T2
AM13	GND_67	GND_167	T20
AM16	GND_68	GND_168	T22
AM19	GND_69	GND_169	AG11
AM22	GND_70	GND_170	T28
AM25	GND_71	GND_171	T32
AN1	GND_72	GND_172	T5
AN10	GND_73	GND_173	T7
AN13	GND_74	GND_174	U12
AN16	GND_75	GND_175	U14
AN19	GND_76	GND_176	U16
AN22	GND_77	GND_177	U19
AN25	GND_78	GND_178	U21
AN30	GND_79	GND_179	U23
AN34	GND_80	GND_180	V12
AN4	GND_81	GND_181	V14
AN7	GND_82	GND_182	V16
AP2	GND_83	GND_183	V19
AP33	GND_84	GND_184	V21
B1	GND_85	GND_185	V23
B10	GND_86	GND_186	W13
B22	GND_87	GND_187	W15
B25	GND_88	GND_188	W17
B28	GND_89	GND_189	W18
B31	GND_90	GND_190	W20
B34	GND_91	GND_191	W22
B4	GND_92	GND_192	W28
B7	GND_93	GND_193	Y12
C10	GND_94	GND_194	Y14
C13	GND_95	GND_195	Y16
C19	GND_96	GND_196	Y19
C22	GND_97	GND_197	Y21
C25	GND_98	GND_198	Y23
C28	GND_99	GND_199	AH11
C7	GND_100	GND_200	
		GND_OPT_1	C16
		GND_OPT_2	W32

+VGACORE

PLACE UNDER GPU

C200	1U/6.3V_4
C165	1U/6.3V_4
C180	1U/6.3V_4
C184	1U/6.3V_4
C167	1U/6.3V_4
C183	0.1U/10V_4
C170	0.1U/10V_4
C209	0.1U/10V_4
C196	0.1U/10V_4
C161	4.7U/6.3V_6
C195	4.7U/6.3V_6
C104	4.7U/6.3V_6
C103	4.7U/6.3V_6
C210	4.7U/6.3V_6
C205	4.7U/6.3V_6
C108	4.7U/6.3V_6
C107	4.7U/6.3V_6
C194	4.7U/6.3V_6
C181	4.7U/6.3V_6
C166	4.7U/6.3V_6
C178	4.7U/6.3V_6
C193	4.7U/6.3V_6
C168	4.7U/6.3V_6
C206	4.7U/6.3V_6

PLACE NEAR GPU

C585	4.7U/10V_6
C91	4.7U/10V_6
C99	4.7U/10V_6
C90	4.7U/10V_6
C92	4.7U/10V_6
C584	22U/6.3VS_6
C100	47U/6.3V_6_S

C192	100U/6.3V_1206

PLACE TO GPU CENTER

for meet Power down sequence for +3V_GFX

+VGACORE — D23 — *MEK500V-40 — +3V_GFX

+1.5V_GFX — D22 — *MEK500V-40

120808 Del DGPU_PWROK circuit because all +1.05V_GFX/+1.5V_GFX power solution have PG connector to PCH

40	+VGACORE
14,15,16,42	+1.05V_GFX
15,19,20,41	+1.5V_GFX
14,17,42	+3V_GFX
2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,28,29,30,31,32,37,38,40	+3V

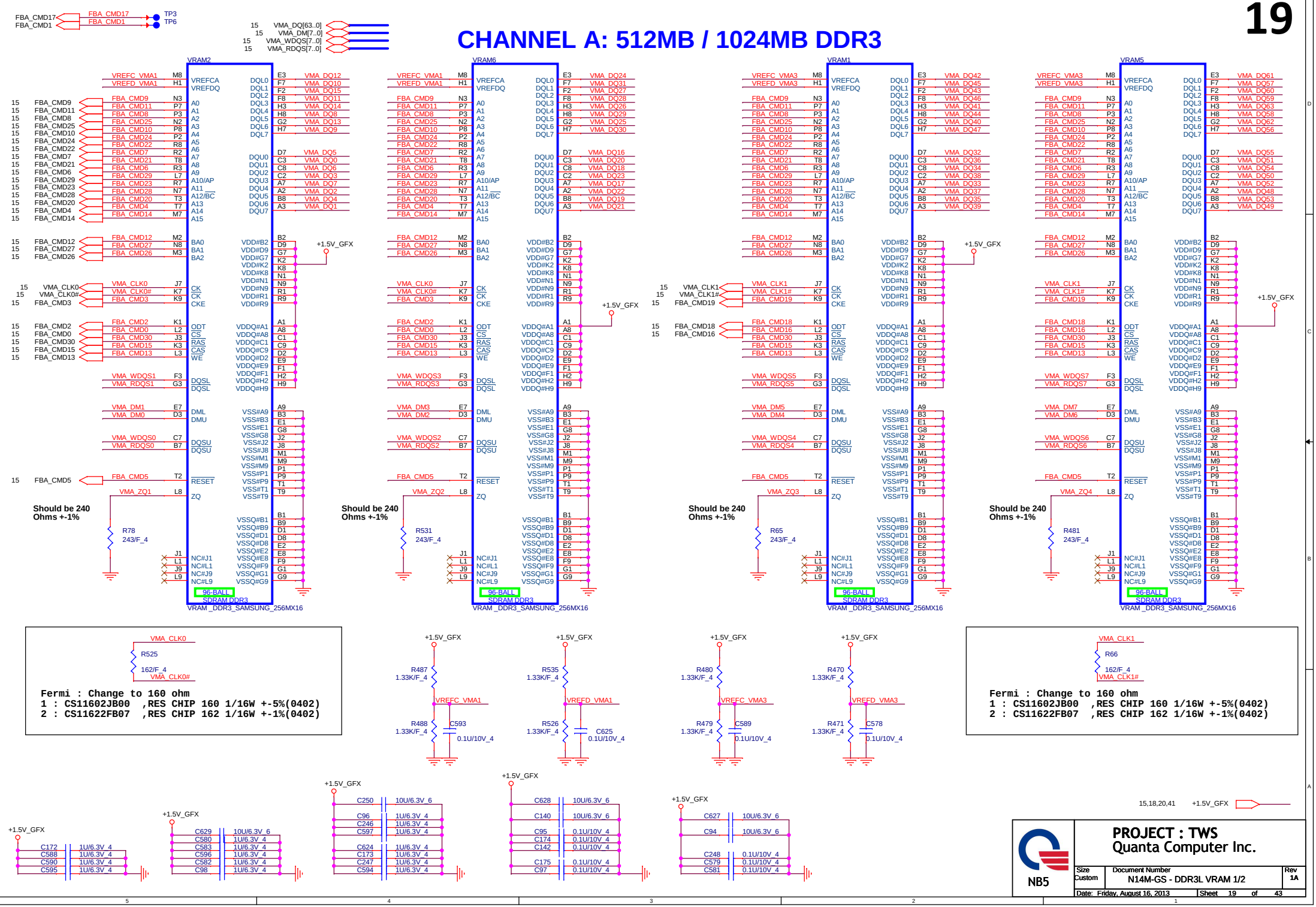
NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N14M-GS - 5/5 (Power)	1A

Date: Friday, August 16, 2013 | Sheet 18 of 43

CHANNEL A: 512MB / 1024MB DDR3



NB5
PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N14M-GS - DDR3L VRAM 1/2	1A

Date: Friday, August 16, 2013 Sheet 19 of 43

15 VMC_DQ[63..0]
15 VMC_DM[7..0]
15 VMC_WDQS[7..0]
15 VMC_RDQS[7..0]

CHANNEL B: 256MB/512MB DDR3

VRAM3 — 96-BALL SDRAM DDR3 — *VRAM _DDR3_SAMSUNG_64MX16

VREFC_VMC1 M8 / VREFD_VMC1 H1
FBC_CMD9 N3, FBC_CMD11 P7, FBC_CMD8 P3, FBC_CMD25 N2, FBC_CMD10 P8, FBC_CMD24 P2, FBC_CMD22 R8, FBC_CMD7 R2, FBC_CMD21 T8, FBC_CMD6 R3, FBC_CMD29 L7, FBC_CMD23 R7, FBC_CMD28 N7, FBC_CMD20 T3, FBC_CMD4 T7, FBC_CMD14 M7
FBC_CMD12 M2, FBC_CMD27 N8, FBC_CMD26 M3
VMC_CLK0 J7, VMC_CLK0# K7, FBC_CMD3 K9
FBC_CMD2 K1, FBC_CMD0 L2, FBC_CMD30 J3, FBC_CMD15 K3, FBC_CMD13 L3
VMC_WDQS2 F3, VMC_RDQS2 G3
VMC_DM2 E7, VMC_DM1 D3
VMC_WDQS1 C7, VMC_RDQS1 B7
FBC_CMD5 T2
VMC_ZQ1 L8
DQL0–DQL7: VMC_DQ18, VMC_DQ22, VMC_DQ16, VMC_DQ21, VMC_DQ19, VMC_DQ17, VMC_DQ20, VMC_DQ23
DQU0–DQU7: VMC_DQ10, VMC_DQ13, VMC_DQ11, VMC_DQ15, VMC_DQ9, VMC_DQ14, VMC_DQ8, VMC_DQ12
+1.5V_GFX
Should be 240 Ohms +-1%
R169 *243/F_4
NC#J1, NC#L1, J9, NC#J9, NC#L9

VRAM8 — 96-BALL SDRAM DDR3 — *VRAM _DDR3_SAMSUNG_64MX16

VREFC_VMC1 M8 / VREFD_VMC1 H1
FBC_CMD9 N3, FBC_CMD11 P7, FBC_CMD8 P3, FBC_CMD25 N2, FBC_CMD10 P8, FBC_CMD24 P2, FBC_CMD22 R8, FBC_CMD7 R2, FBC_CMD21 T8, FBC_CMD6 R3, FBC_CMD29 L7, FBC_CMD23 R7, FBC_CMD28 N7, FBC_CMD20 T3, FBC_CMD4 T7, FBC_CMD14 M7
FBC_CMD12 M2, FBC_CMD27 N8, FBC_CMD26 M3
VMC_CLK0 J7, VMC_CLK0# K7, FBC_CMD3 K9
FBC_CMD2 K1, FBC_CMD0 L2, FBC_CMD30 J3, FBC_CMD15 K3, FBC_CMD13 L3
VMC_WDQS3 F3, VMC_RDQS3 G3
VMC_DM3 E7, VMC_DM0 D3
VMC_WDQS0 C7, VMC_RDQS0 B7
FBC_CMD5 T2
VMC_ZQ2 L8
DQL0–DQL7: VMC_DQ25, VMC_DQ29, VMC_DQ27, VMC_DQ31, VMC_DQ26, VMC_DQ30, VMC_DQ24, VMC_DQ28
DQU0–DQU7: VMC_DQ3, VMC_DQ6, VMC_DQ1, VMC_DQ7, VMC_DQ0, VMC_DQ5, VMC_DQ2, VMC_DQ4
+1.5V_GFX
Should be 240 Ohms +-1%
R553 *243/F_4
NC#J1, NC#L1, J9, NC#J9, NC#L9

VRAM4 — 96-BALL SDRAM DDR3 — *VRAM _DDR3_SAMSUNG_64MX16

VREFC_VMC3 M8 / VREFD_VMC3 H1
FBC_CMD9 N3, FBC_CMD11 P7, FBC_CMD8 P3, FBC_CMD25 N2, FBC_CMD10 P8, FBC_CMD24 P2, FBC_CMD22 R8, FBC_CMD7 R2, FBC_CMD21 T8, FBC_CMD6 R3, FBC_CMD29 L7, FBC_CMD23 R7, FBC_CMD28 N7, FBC_CMD20 T3, FBC_CMD4 T7, FBC_CMD14 M7
FBC_CMD12 M2, FBC_CMD27 N8, FBC_CMD26 M3
VMC_CLK1 J7, VMC_CLK1# K7, FBC_CMD19 K9
FBC_CMD18 K1, FBC_CMD16 L2, FBC_CMD30 J3, FBC_CMD15 K3, FBC_CMD13 L3
VMC_WDQS4 F3, VMC_RDQS4 G3
VMC_DM4 E7, VMC_DM5 D3
VMC_WDQS5 C7, VMC_RDQS5 B7
FBC_CMD5 T2
VMC_ZQ3 L8
DQL0–DQL7: VMC_DQ36, VMC_DQ34, VMC_DQ39, VMC_DQ32, VMC_DQ37, VMC_DQ35, VMC_DQ38, VMC_DQ33
DQU0–DQU7: VMC_DQ47, VMC_DQ42, VMC_DQ45, VMC_DQ41, VMC_DQ44, VMC_DQ43, VMC_DQ46, VMC_DQ40
+1.5V_GFX
Should be 240 Ohms +-1%
R150 *243/F_4
NC#J1, NC#L1, J9, NC#J9, NC#L9

VRAM7 — 96-BALL SDRAM DDR3 — *VRAM _DDR3_SAMSUNG_64MX16

VREFC_VMC3 M8 / VREFD_VMC3 H1
FBC_CMD9 N3, FBC_CMD11 P7, FBC_CMD8 P3, FBC_CMD25 N2, FBC_CMD10 P8, FBC_CMD24 P2, FBC_CMD22 R8, FBC_CMD7 R2, FBC_CMD21 T8, FBC_CMD6 R3, FBC_CMD29 L7, FBC_CMD23 R7, FBC_CMD28 N7, FBC_CMD20 T3, FBC_CMD4 T7, FBC_CMD14 M7
FBC_CMD12 M2, FBC_CMD27 N8, FBC_CMD26 M3
VMC_CLK1 J7, VMC_CLK1# K7, FBC_CMD19 K9
FBC_CMD18 K1, FBC_CMD16 L2, FBC_CMD30 J3, FBC_CMD15 K3, FBC_CMD13 L3
VMC_WDQS6 F3, VMC_RDQS6 G3
VMC_DM6 E7, VMC_DM7 D3
VMC_WDQS7 C7, VMC_RDQS7 B7
FBC_CMD5 T2
VMC_ZQ4 L8
DQL0–DQL7: VMC_DQ53, VMC_DQ55, VMC_DQ51, VMC_DQ49, VMC_DQ50, VMC_DQ52, VMC_DQ48, VMC_DQ54
DQU0–DQU7: VMC_DQ59, VMC_DQ60, VMC_DQ58, VMC_DQ63, VMC_DQ57, VMC_DQ62, VMC_DQ56, VMC_DQ61
+1.5V_GFX
Should be 240 Ohms +-1%
R546 *243/F_4
NC#J1, NC#L1, J9, NC#J9, NC#L9

VMC_CLK0 — R543 *162/F_4 — VMC_CLK0#

Fermi : Change to 160 ohm (WJ)
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

+1.5V_GFX: R555 *1.33K/F_4, R552 *1.33K/F_4 — VREFC_VMC1 — C669 *0.1U/10V_4
+1.5V_GFX: R550 *1.33K/F_4, R549 *1.33K/F_4 — VREFD_VMC1 — C659 *0.1U/10V_4

VMC_CLK1 — R155 *162/F_4 — VMC_CLK1#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

+1.5V_GFX: R162 *1.33K/F_4, R161 *1.33K/F_4 — VREFC_VMC3 — C288 *0.1U/10V_4
+1.5V_GFX: R547 *1.33K/F_4, R545 *1.33K/F_4 — VREFD_VMC3 — C655 *0.1U/10V_4

+1.5V_GFX: C309, C665, C290, C652 *1U/6.3V_4
+1.5V_GFX: C276, C646, C284, C660, C654, C666 *10U/6.3V_6 / *1U/6.3V_4
+1.5V_GFX: C277, C649, C301, C656, C274, C676, C648, C650 *0.1U/10V_4
+1.5V_GFX: C677, C279, C296, C675, C272, C651, C674, C653 *1U/6.3V_4

15 FBC_CMD17 — FBC_CMD17 — TP14
15 FBC_CMD1 — FBC_CMD1 — TP15

900MHz VRAM size:(WJ)
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

15,18,19,41 +1.5V_GFX

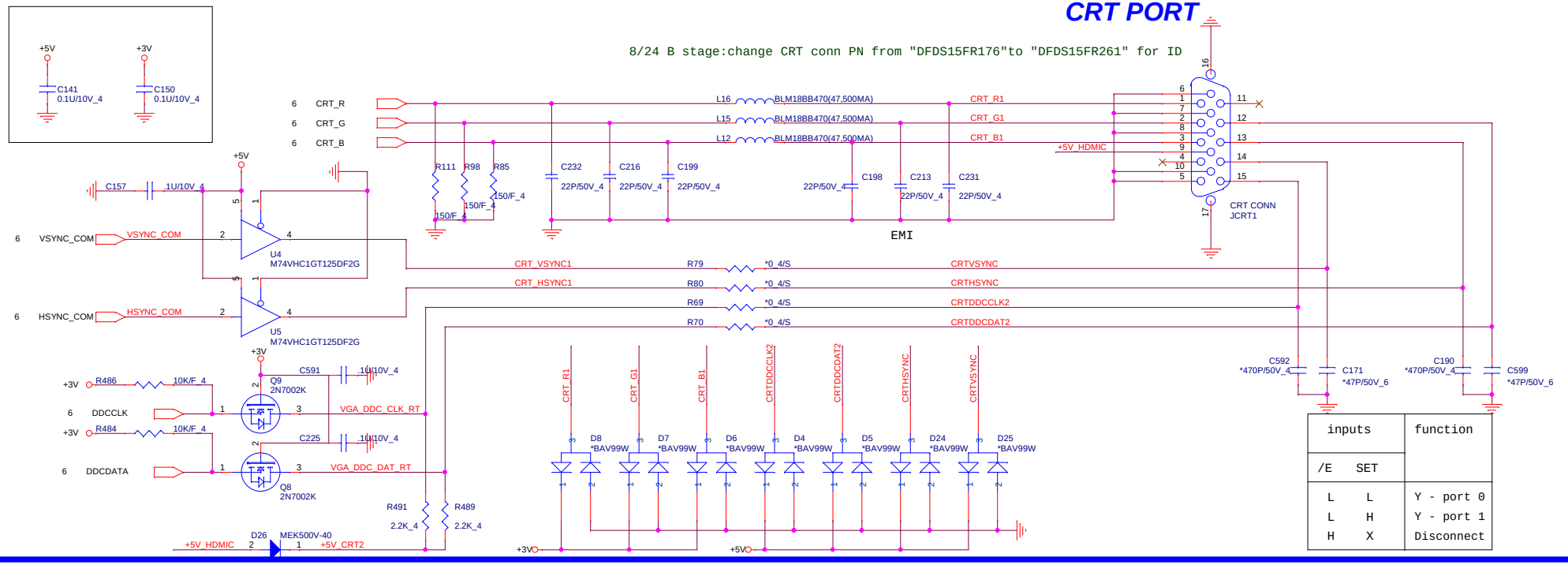
NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N14M-GS - DDR3L VRAM 2/2	1A
Date: Friday, August 16, 2013	Sheet 20 of 43	

CRT PORT

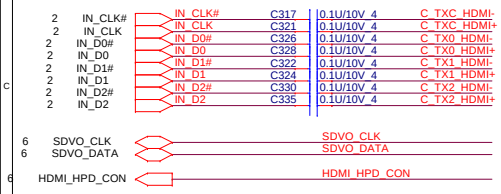
8/24 B stage:change CRT conn PN from "DFDS15FR176"to "DFDS15FR261" for ID



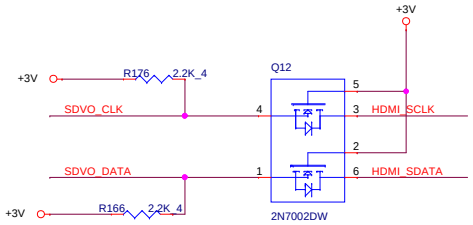
inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

HDMI PORT

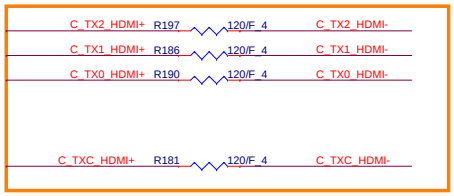
close to HDMI conn

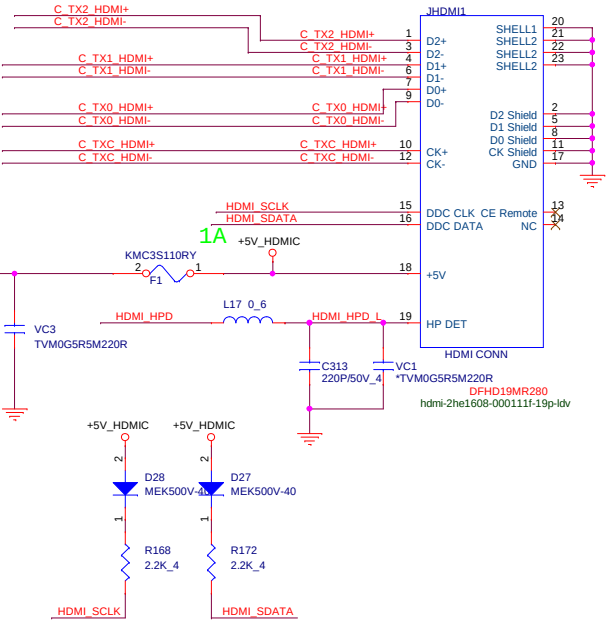


Close to HDMI Connector

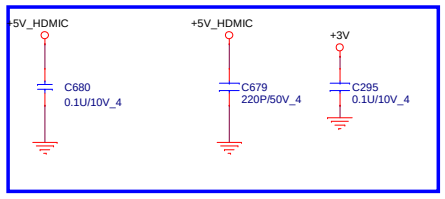


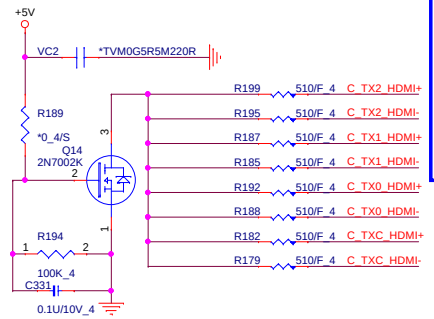
EMI request

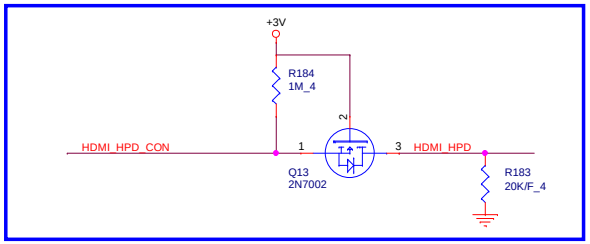




EMI request





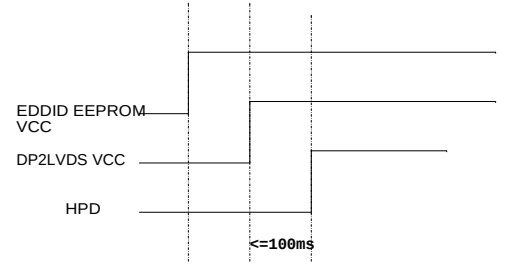


26,28,29,32,37,40 +5V
2,6,7,8,9,10,12,13,14,17,22,23,24,25,26,28,29,30,31,32,37,38,40 +3V
26,27,28,34,35,36,37,38,39,40,41 +5VS5

NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT,Hole	1A
Date: Friday, August 16, 2013	Sheet 21 of 43	



Reserve for co layout EDP CON, EDP only please stuff

RTD2136 Dual Channel only

Pine 18: keep 80 Mile Trace

RTD2136S

Default

Reserve

IC body need GND pad

Use 1% Res on R7034

		PIN 47	
		0	1
PIN 48	0	X	EP mode
	1	ROM	EEPROM

L69: need use CV-4709MN00 for Vendor suggestion

keep 80 Mile Trace

USING 60R 2A

CLOSE TO Pin22

Close to Pin18

USING 60R 1A

Close to Pin5

Close to Pin17

Close to Pin11

Close to Pin43

SWR MODE	LDO MODE
Stuff L69	Stuff R9095

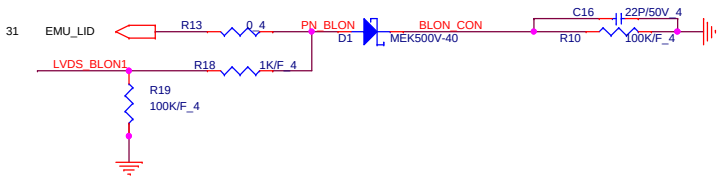
PROJECT : TWS
Quanta Computer Inc.

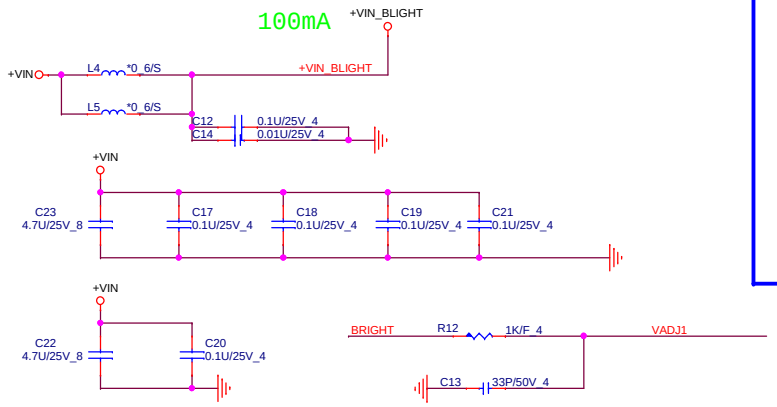
NB5

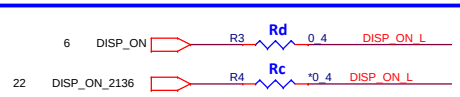
Size	Document Number	Rev
Custom	RTD2136S	1A

Date: Friday, August 16, 2013 Sheet 22 of 43

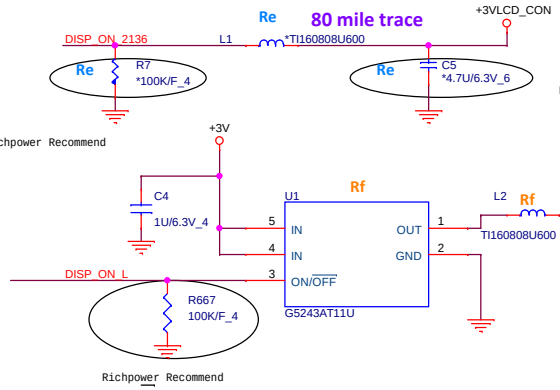
LID Switch

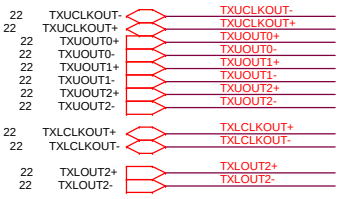


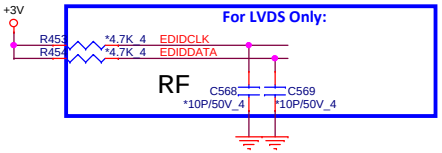


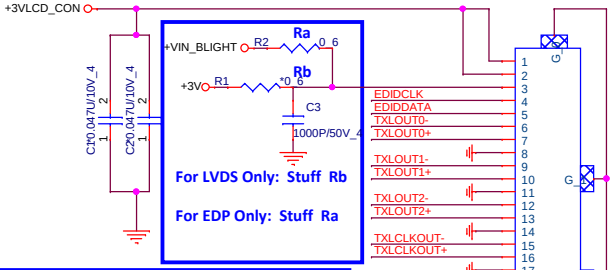


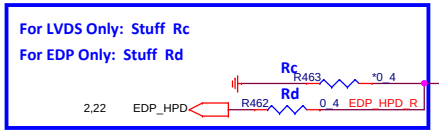
For EDP Only: stuff Rd,Rf
For LVDS Only use power switch: stuff Rc,Rf
For LVDS Only non-use power switch: stuff Re

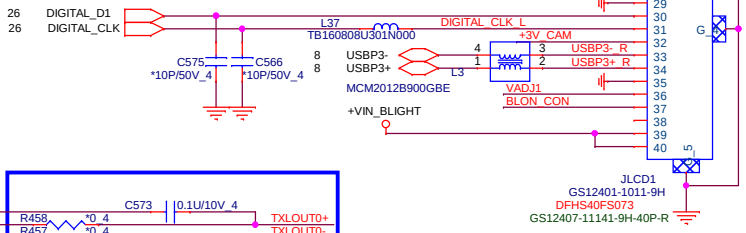


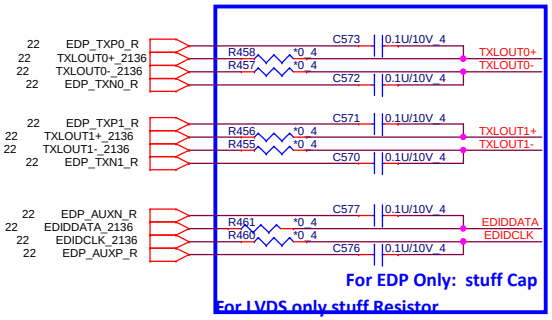


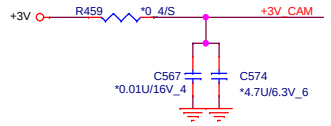


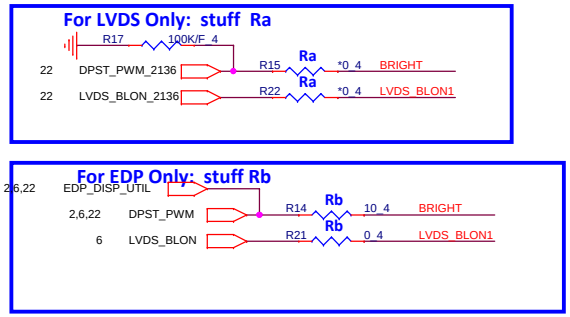


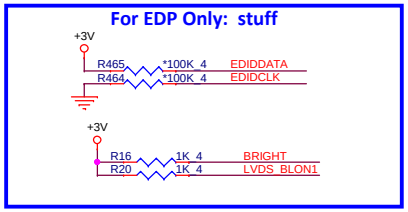












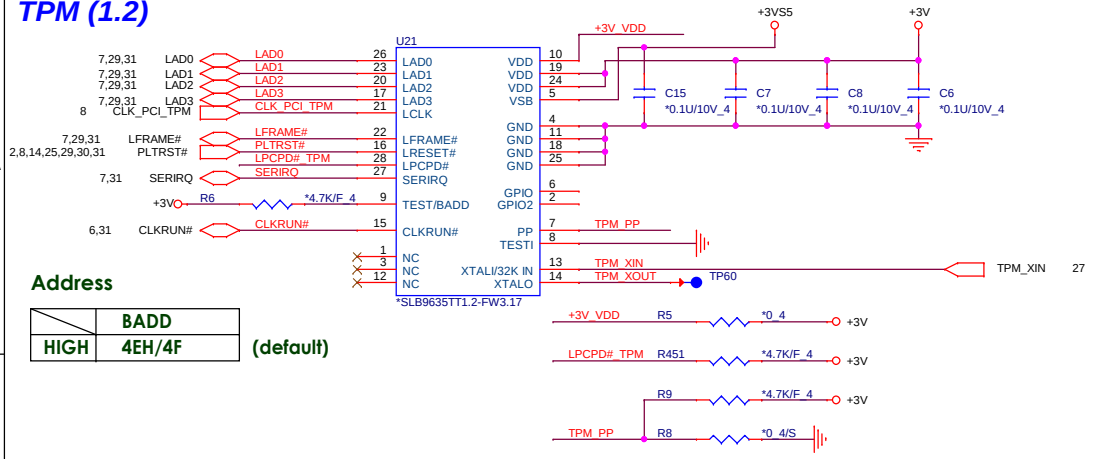
NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

Date: Friday, August 16, 2013 Sheet 23 of 43

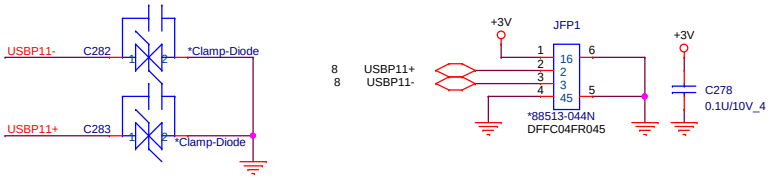
TPM (1.2)



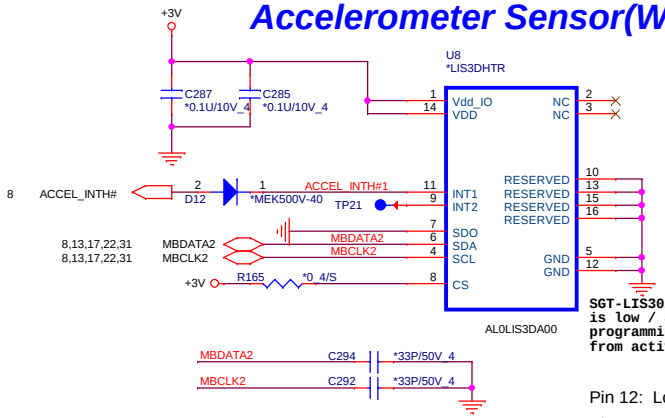
Address

	BADD
HIGH	4EH/4F (default)

Finger Printer



Accelerometer Sensor(WJ) IN the center of main board



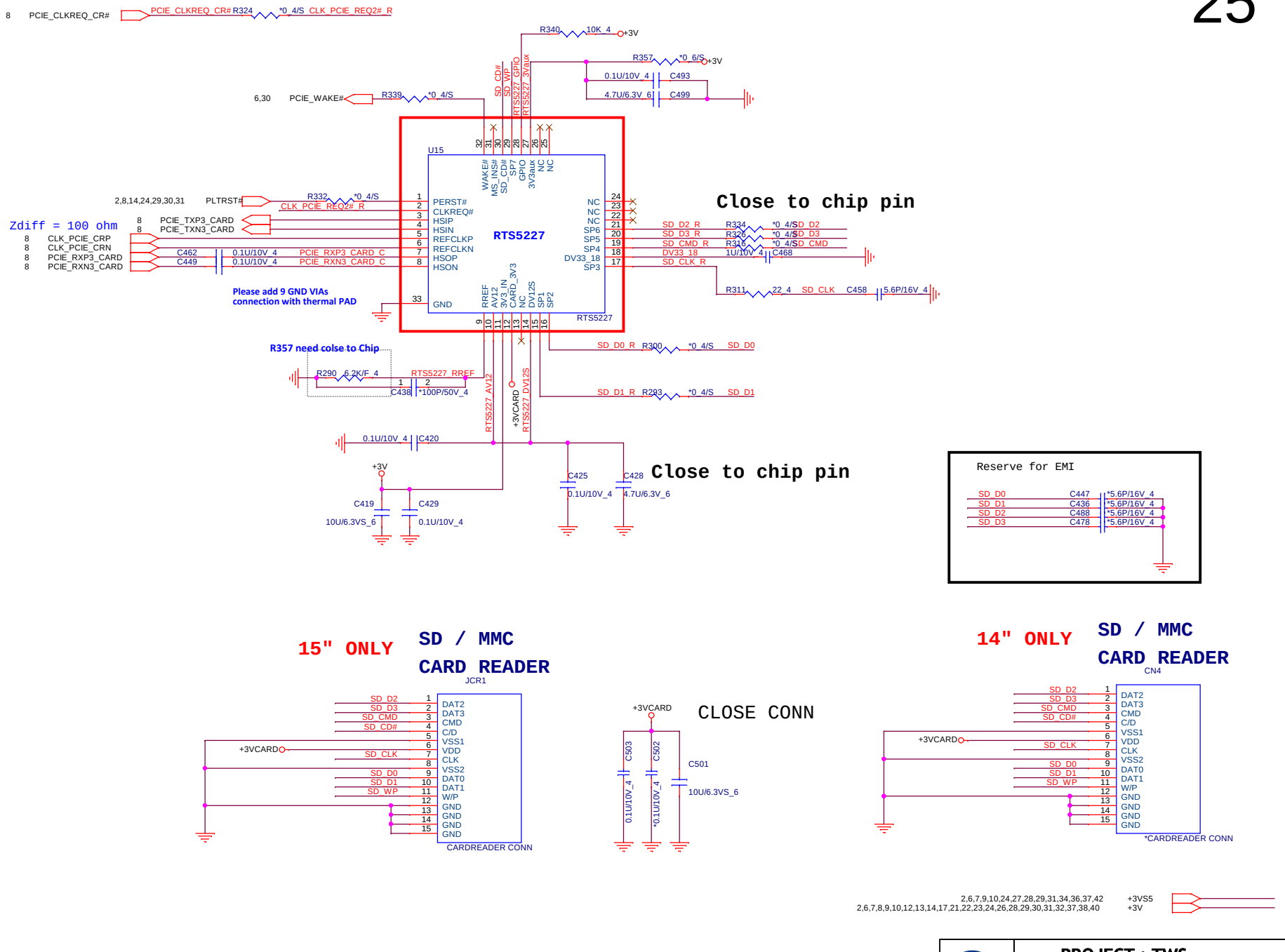
SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

Pin 12: Low 38hex

Pin 12: unconnected/floating 3Ahex

2,6,7,8,9,10,12,13,14,17,21,22,23,25,26,28,29,30,31,32,37,38,40 +3V
4,27,29,31,32,33,34 +3VPCU
21,26,28,29,32,37,40 +5V

NB5	PROJECT : TWS Quanta Computer Inc.		
	Size: Custom	Document Number: TPM/FP/G Sensor	Rev: 1A
	Date: Friday, August 16, 2013	Sheet 24 of 43	



NB5	PROJECT : TWS Quanta Computer Inc.	
Size: Custom	Document Number: RTS5227 & CR SOCKET	Rev: 1A
Date: Friday, August 16, 2013	Sheet 25 of 43	

Audio Jack type:
Normal Open
Combo Jack(IPHONE)

Close to Pin 41
Close to Pin 36
Close to Pin 9
Close to PIN1
Close to Pin 46
Close to PIN40
Close to PIN26
Close to PIN28
Close to Pin 13
Close to INT SPEAKER CONN
Close to INT SPEAKER CONN
Close to CODEC and around AGND & GND
Middle of CODEC & Bead

Moat
Analog
Digital
>40mils trace

ALC282-CG
Digital
Analog

TO Digital MIC
TO Audio Jack MIC
TO Internal Speakers

AGND SHIELD
AGND SHIELD
AGND SHIELD

check value

Moat
40mils

Speaker 4 ohm: 40mils

place to near U37 or under U37.

FOR EMI

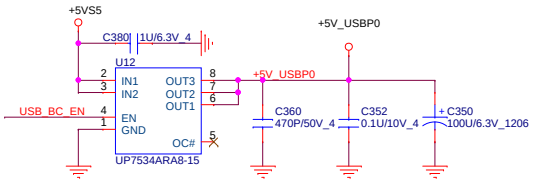
DUAL USB CONN
CN2
INT SPEAKER CONN
CN3
DFHD04MR752
88266-0400-4P-L

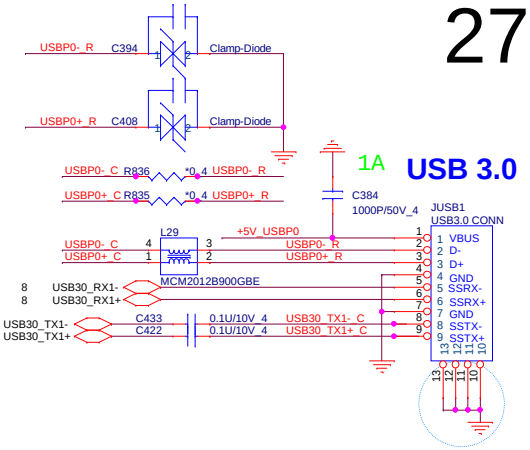
PROJECT : TWS
Quanta Computer Inc.
NB5

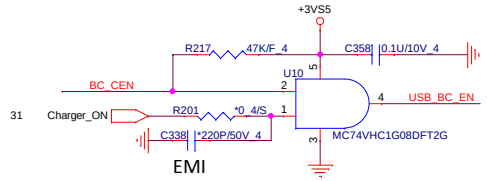
Size	Document Number	Rev
Custom	Azalia ALC282-CG	1A

Date: Friday, August 16, 2013 Sheet 26 of 43

USB3.0/USB2.0 COMBO



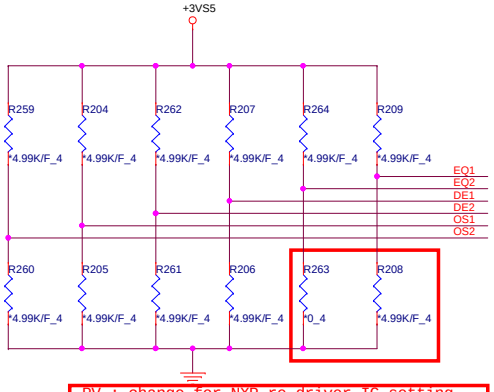




OSx	Transition Bit Amplitude
NC(default)	1000
0	870
1	1085
EQx	Equalization dB
NC(default)	0
0	7
1	15

DEx	OSx=NC	OSx=0	OSx=1
NC	-3.5dB	-2.2dB	-4.4dB
0	-6.0dB	-5.2dB	-6.0dB
1	-8.5dB	-8.9dB	-7.6dB

EN_RXD	DEVICE FUNCTION
1(default)	Normal operating mode
0	Sleep mode
CM	DEVICE FUNCTION
0(default)	Normal operating mode
1	Compliance mode



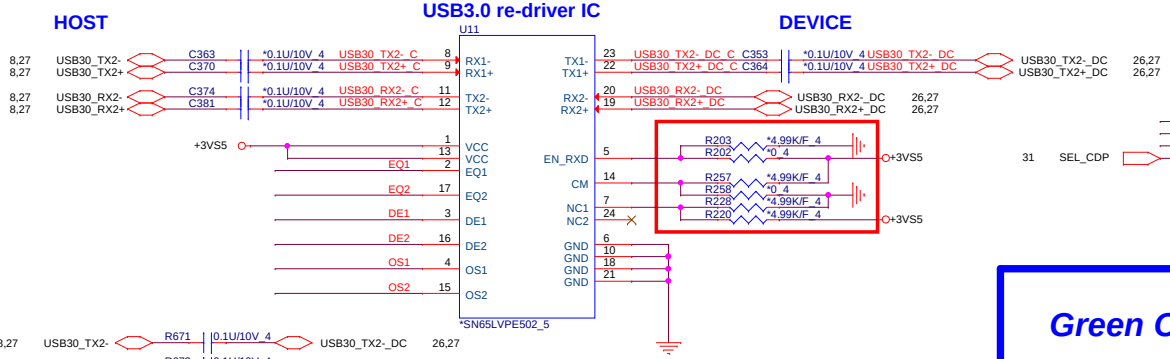
PV : change for NXP re-driver IC setting

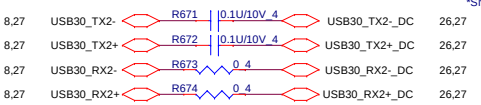
12/21 add R696/R695 for TI signal measure

HOST

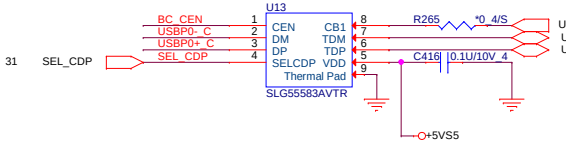
USB3.0 re-driver IC

DEVICE

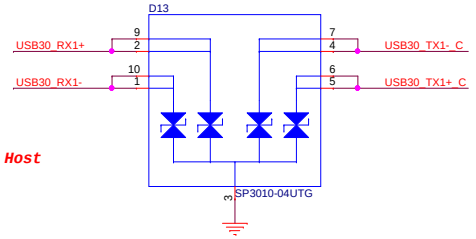




Charge USB



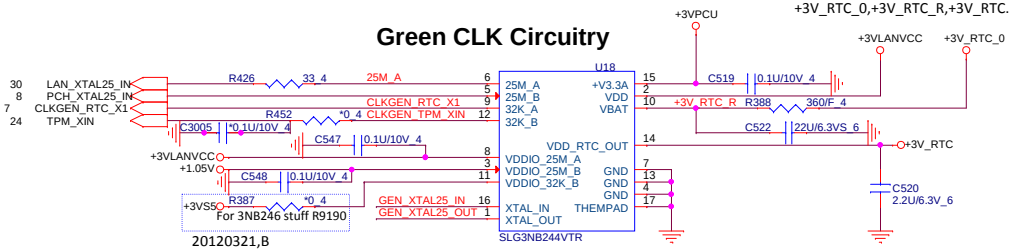
To Host

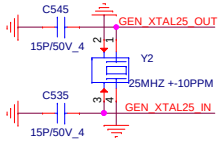


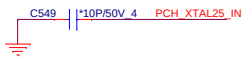
Green CLK Circuitry

20mils width(min)

+3V_RTC_0,+3V_RTC_R,+3V_RTC..



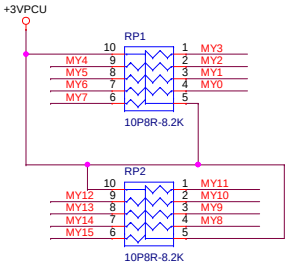


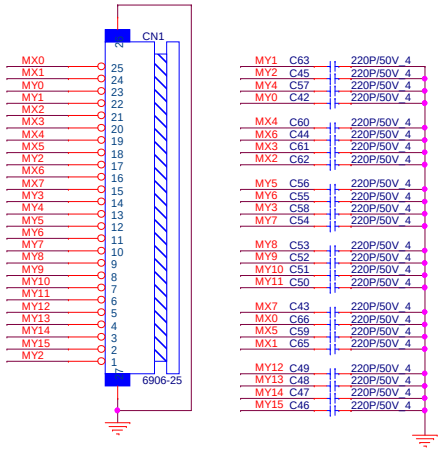


FOR TPM option

	TPM	Non-TPM
R525	Stuff	NA
U5	AL3NB246000	AL3NB244000

Keyboard Connector





31 MY[0..15] MY[0..15]

31 MX[0..7] MX[0..7]

NB5

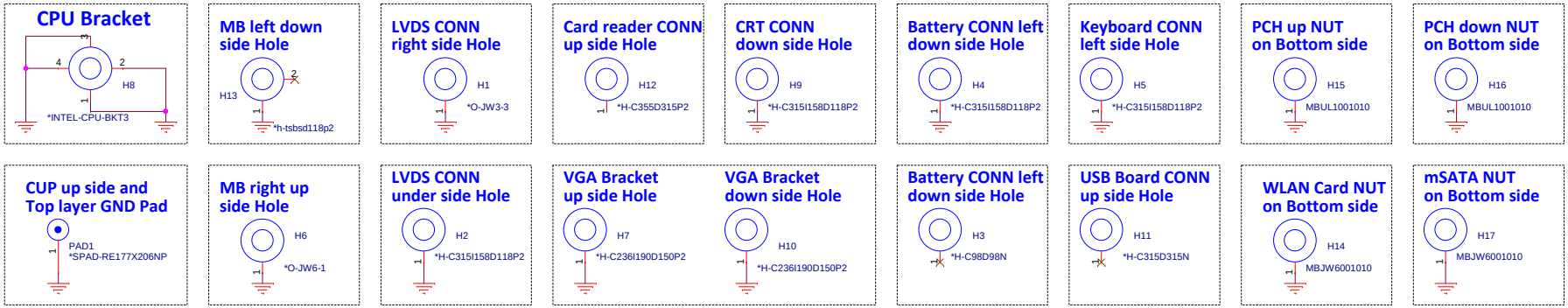
PROJECT : TWS

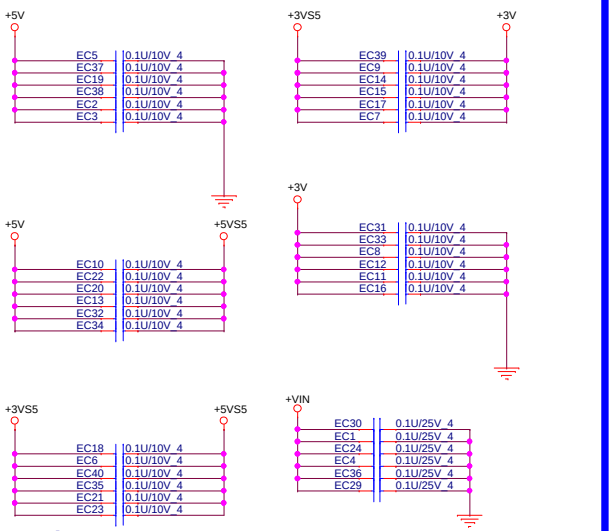
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB3.0/Charge USB/KBD/Green CLK	1A

Date: Friday, August 16, 2013 Sheet 27 of 43

Hole





EMI/ESD

Stitching Cap(each 1" place one cap)

NB5

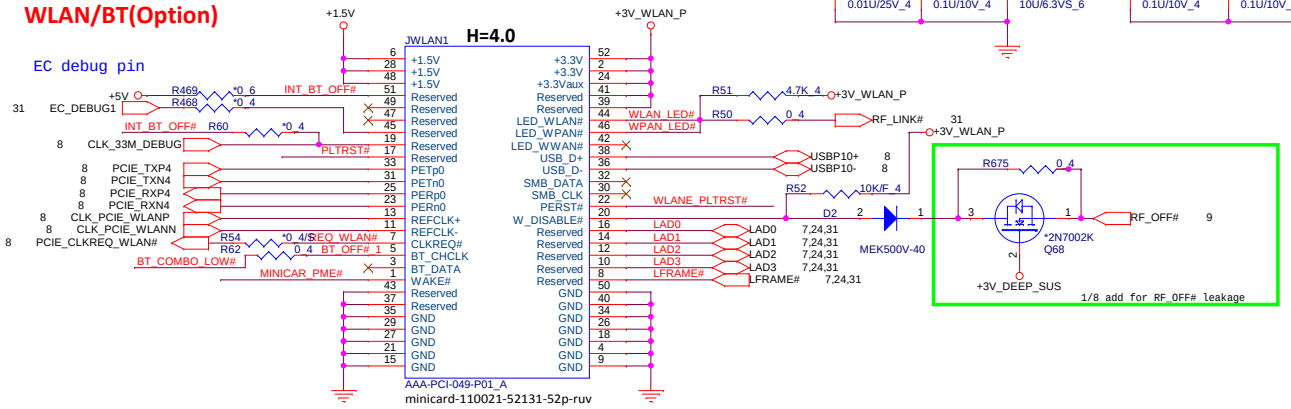
PROJECT : TWS
Quanta Computer Inc.

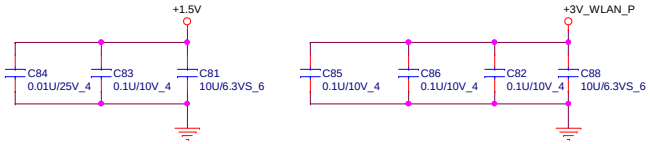
Size	Document Number	Rev
Custom	Hole / EMI Cap	1A

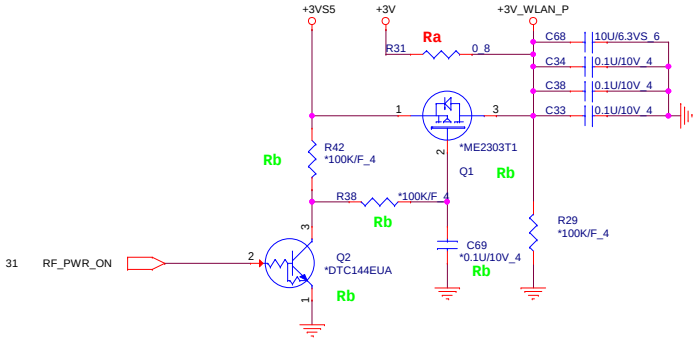
Date: Friday, August 16, 2013 | Sheet 28 of 43

Mini Card WLAN/BT(Option)

EC debug pin



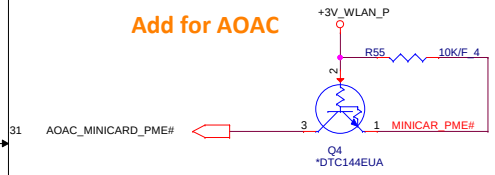




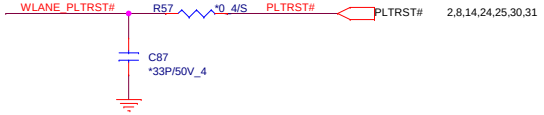
Avoid leakage issue

Support Wake Function(Reserve)

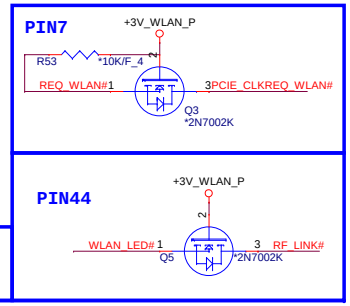
Add for AOAC

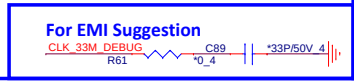


Mini Card Reset

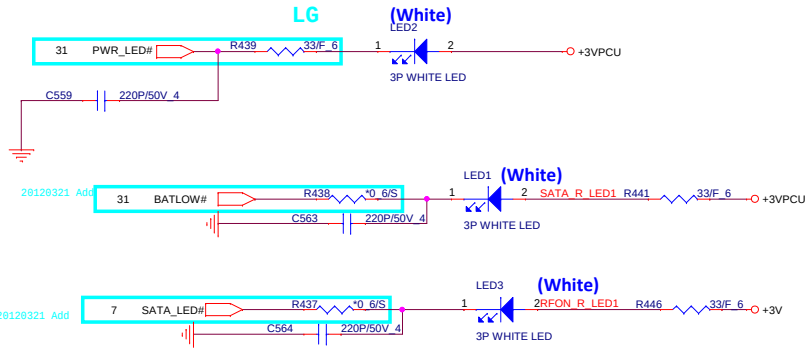


non-AOAC	LG	Ra
AOAC	CB	Rb

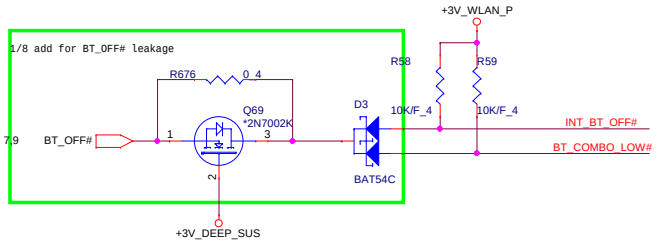




LED Status



PIN19,51



9/4 Intel COMBO card control circuit
1.add R1001,R1002,Q1001
2.add net name"INT_BT_COMBO_EN#" -> "INT_BT_OFF#"

2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,28,30,31,32,37,38,40 +3V
21,26,28,32,37,40 +5V
4,27,31,32,33,34 +3VPCU
6,7,8,10,26,32,36 +1.5V

NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN & LED	1A
Date: Friday, August 16, 2013	Sheet 29 of 43	

LAN conn

For EMI 0 ~ 22 ohm

R170 *10_4 LAN_XTAL1 XTAL1 XTAL2
Y1 *25MHz
C299 *33P/50V_4
C297 *33P/50V_4

Power trace Layout 寬度> 60mil
next ver need to add 0805 0 ohm & 0.1u cap for 10/100
>60mil
>60mil
+1.05V_LAN_REGOUT L39 4.7UH,+-20%,650MA_1210
Trace<30 mil
Width > 60 mil
Ca C678 0.1U/10V_4
Cb C670 4.7U/6.3V_6

For GbE
Stuff La, Ca ,Cb

For 10/100
NA: La, Ca ,Cb

For GbE
* Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3, 8, 22, 30

For 10/100 NA Ce,Cf
* Place Cc , Cd close to each VDD10 pin-- 8, 30 only,

+1.05V_LAN
Cc C661 0.1U/10V_4
Cd C662 0.1U/10V_4
Ce C668 0.1U/10V_4
Cf C664 0.1U/10V_4
Cg C671 *1U/6.3V_4
Cf C667 *1U/6.3V_4
reserve for colay

For GbE
* Place Cg close to each VDD10 pin-- 22 (reserve)

For 10/100
* Place Cf close to each VDD10 pin-- 30 (reserve)

For 10/100
* Stuff Ce and Cf only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32

Power trace Layout 寬度> 40mil
+3V_LAN
+3VLANVCC
C293 0.1U/10V_4 Ca
C658 0.1U/10V_4 Cb
C305 *0.1U/10V_4 Ce
C657 *0.1U/10V_4 Cf
reserve for colay

* Place Cc and Cd close to each VDD33 pin-- 23, 32
C663 4.7U/6.3V_6 Cc
C306 0.1U/10V_4 Cd
Remove For Not Using SWR mode

For GIGA
Stuff Cc ,Cd

For 10/100
NA: Cc, Cd

+1.05V_LAN
R164 0_4 LAN_XTAL25_IN 27
R163 2.49K/F_4 LANRSET
+3V_LAN
TP81 TP13 TP22
U9
RSET VDD10 XTAL2 XTAL1 LAN_TX# LAN_GLED#
AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 LED0/GPO LED2(LED1)
GND 33
Please add 9 GND VIAs connection with thermal PAD
RTL8111GSH
MDI0+ 1 MDI0- 2 VDD10 3 MDI1+ 4 MDI1- 5 MDI2+ 6 MDI2- 7 VDD10 8
MDIP0 MDIN0 AVDD10(NC) MDIP1 MDIN1 MDIP2(NC) MDIN2(NC) AVDD10
REGOUT(NC) VDDREG(VDD33) DVDD10(NC) LANWAKEB ISOLATEB PERSTB HSON HSOP
24 +1.05V_LAN_REGOUT
23 DVDDL R175 *0_4/S +3V_LAN
22 VDD10 +1.05V_LAN_REGOUT
21 PCIE_WAKE# +1.05V_LAN
20 ISOLATEB PCIE_WAKE# 6,25
19 PLTRST# 2,8,14,24,25,29,31
18 PCIE_RXN2_LAN_L C303 0.1U/10V_4 PCIE_RXN2_LAN 8
17 PCIE_RXP2_LAN_L C302 0.1U/10V_4 PCIE_RXP2_LAN 8
MDP3(NC) MDN3(NC) AVDD33(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_N
9 10 11 12 13 14 15 16
MDI3+ MDI3-
+3V_LAN
PCIE_CLKREQ_LAN# R167 *0_4/S LAN_CLKRQ
8 PCIE_CLKREQ_LAN#
CLK_PCIE_LANN CLK_PCIE_LANP PCIE_TXN2_LAN PCIE_TXP2_LAN
CLK_PCIE_LANN 8 CLK_PCIE_LANP 8 PCIE_TXN2_LAN 8 PCIE_TXP2_LAN 8

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)
+3V R174 1K_4 ISOLATEB R173 15K/F_4

pin23 trace >40 mil
pin24 trace >60 mil

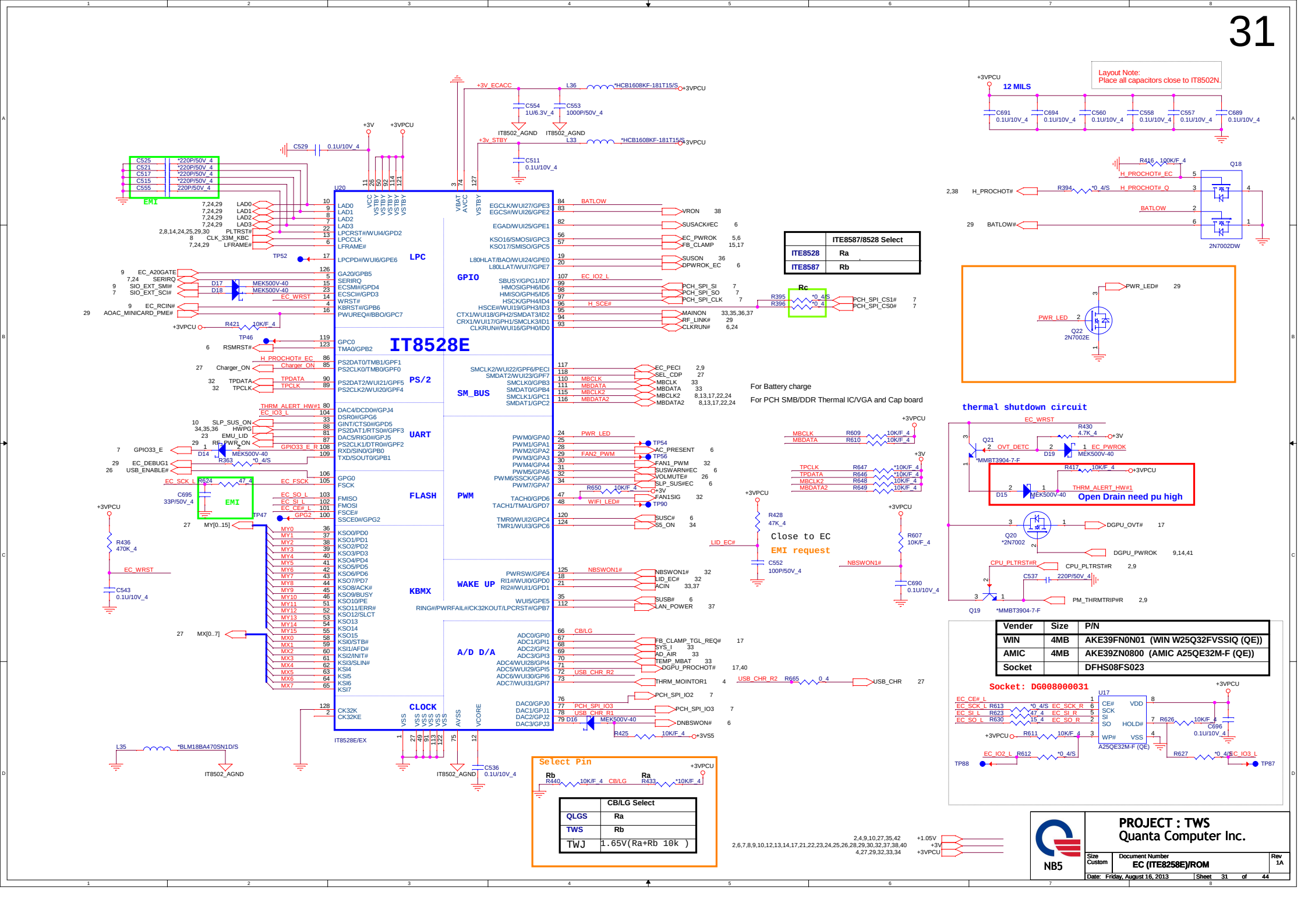
R151 *0_4/S
R138 *0_4/S
R139 *0_4/S
R152 *0_4/S
LAN_AGND

U24
MDI0+ 2 MDI0- 3 MDI1+ 5 MDI1- 6 MDI2+ 8 MDI2- 9 MDI3+ 11 MDI3- 12
TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-
MX1+ MX1- MX2+ MX2- MX3+ MX3- MX4+ MX4-
TRA_V_DAC 1 TRA_V_DAC 4 TRA_V_DAC 7 TRA_V_DAC 10
TCT1 TCT2 TCT3 TCT4
MCT1 MCT2 MCT3 MCT4
23 LAN_MX0+ 22 LAN_MX0- 20 LAN_MX1+ 19 LAN_MX1- 17 LAN_MX2+ 16 LAN_MX2- 14 LAN_MX3+ 13 LAN_MX3-
24 LAN_MCTG3 21 LAN_MCTG2 18 LAN_MCTG1 15 LAN_MCTG0
NS892407
C280 *0.01U/100V_06
C275 *0.01U/100V_06
C273 *0.01U/100V_06
C270 *0.01U/100V_06
R145 75/F_4
R146 75/F_4
R147 75/F_4
R148 75/F_4
LAN_MCTG
C647 0.01U/25V_4
C645 10P/3KV_1808
LAN_AGND

For GiGA
BOT:GST5009B LF,DB0Z06LAN00
For 10/100
BOT: TST1284R LF DB0EL5LAN00
2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,28,29,31,32,37,38,40
27,37
+3V
+3VLANVCC

+3VLANVCC
JRJ1 RJ45_CONN
LAN_TX# R156 330/F_4 LED_AMB_N
C286 1000P/50V_4
LAN_MX3- LAN_MX3+ LAN_MX1- LAN_MX2- LAN_MX2+ LAN_MX1+ LAN_MX0- LAN_MX0+
LED_AMB_P A1 LED_AMB_N A2
RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+
GND1 GND
LAN_AGND
+3VLANVCC
LAN_GLED# R144 330/F_4 LED_GRE_N
C268 1000P/50V_4
LED_GRE_P B1 LED_GRE_N B2
C291 1000P/50V_4 LAN_TX#
C266 1000P/50V_4 LAN_GLED#
EMI request
C311 0.1U/10V_4 +3V
9/27 EMI request

PROJECT : TWS
Quanta Computer Inc.
NB5
Size Custom
Document Number RTL 8111GS/RJ45
Rev 1A
Date: Friday, August 16, 2013
Sheet 30 of 43

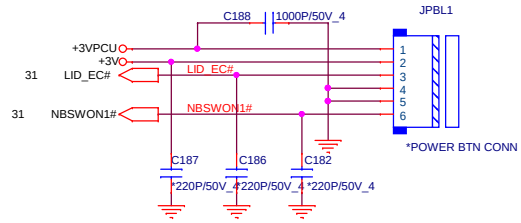

IT8528E
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
IT8528E/EX
EMI
Layout Note:
Place all capacitors close to IT8502N.
12 MILS
ITE8587/8528 Select
ITE8528 Ra
ITE8587 Rb
For Battery charge
For PCH SMB/DDR Thermal IC/VGA and Cap board
thermal shutdown circuit
Open Drain need pu high
Close to EC
EMI request
Select Pin
CB/LG Select
QLGS Ra
TWS Rb
TWJ 1.65V(Ra+Rb 10k)
Vender Size P/N
WIN 4MB AKE39FN0N01 (WIN W25Q32FVSSIQ (QE))
AMIC 4MB AKE39ZN0800 (AMIC A25QE32M-F (QE))
Socket DFHS08FS023
Socket: DG008000031
PROJECT : TWS
Quanta Computer Inc.
NB5
EC (ITE8258E)/ROM
Date: Friday, August 16, 2013
Sheet 31 of 44

Left side

Power Botton Connector

For LG

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



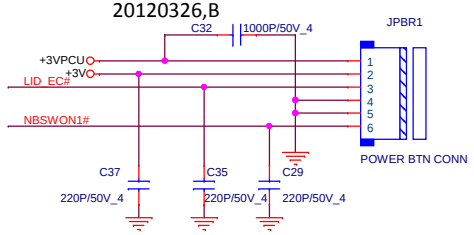
Right side

Power Botton Connector(2)

For CB

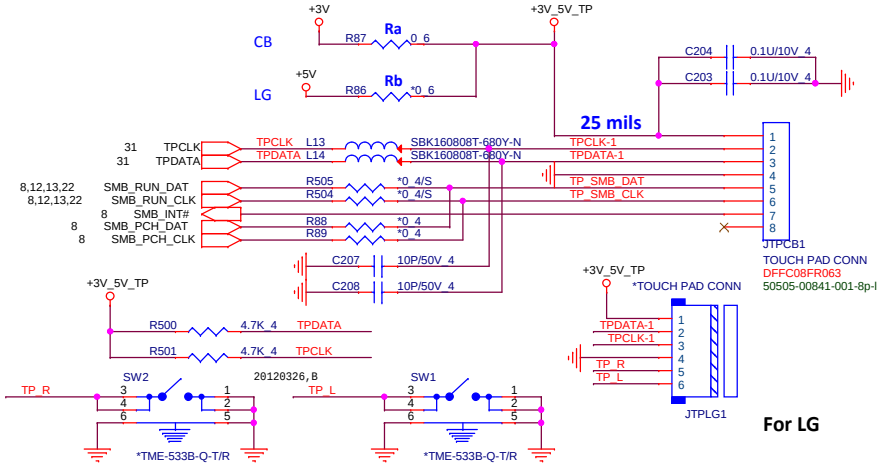
20120326,B

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

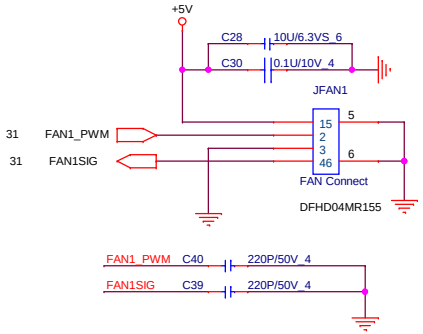


Touch Pad Connector

	Ra	Rb	JTPCB1	JTPLG1, SW1, SW2
CB	V	X	V	X
LG	X	V	X	V

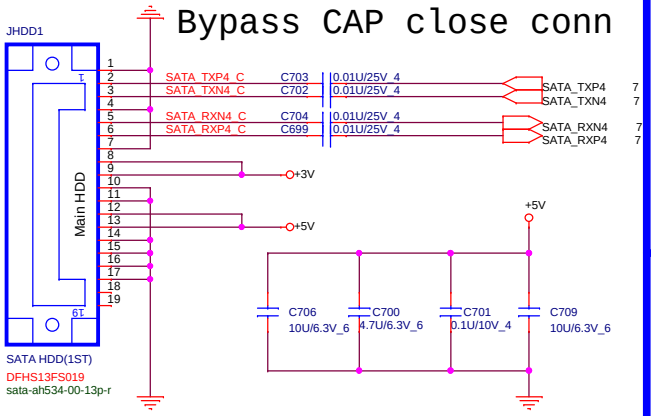


CPU FAN

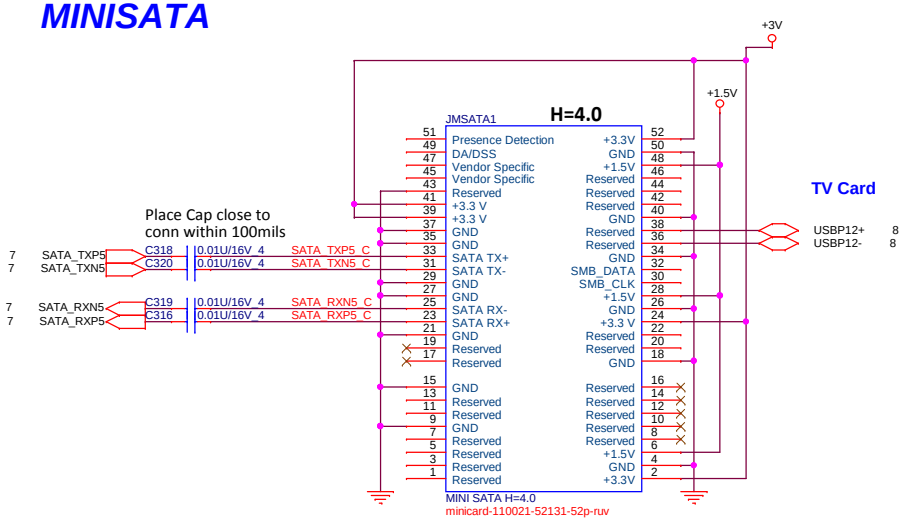


SATA HDD CONNECTOR

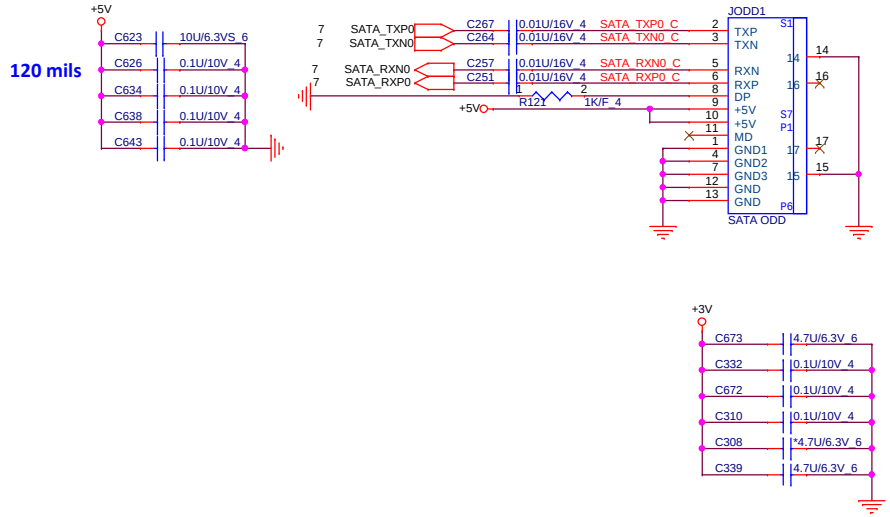
Bypass CAP close conn

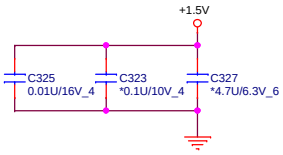


MINISATA



SATA ODD Connector





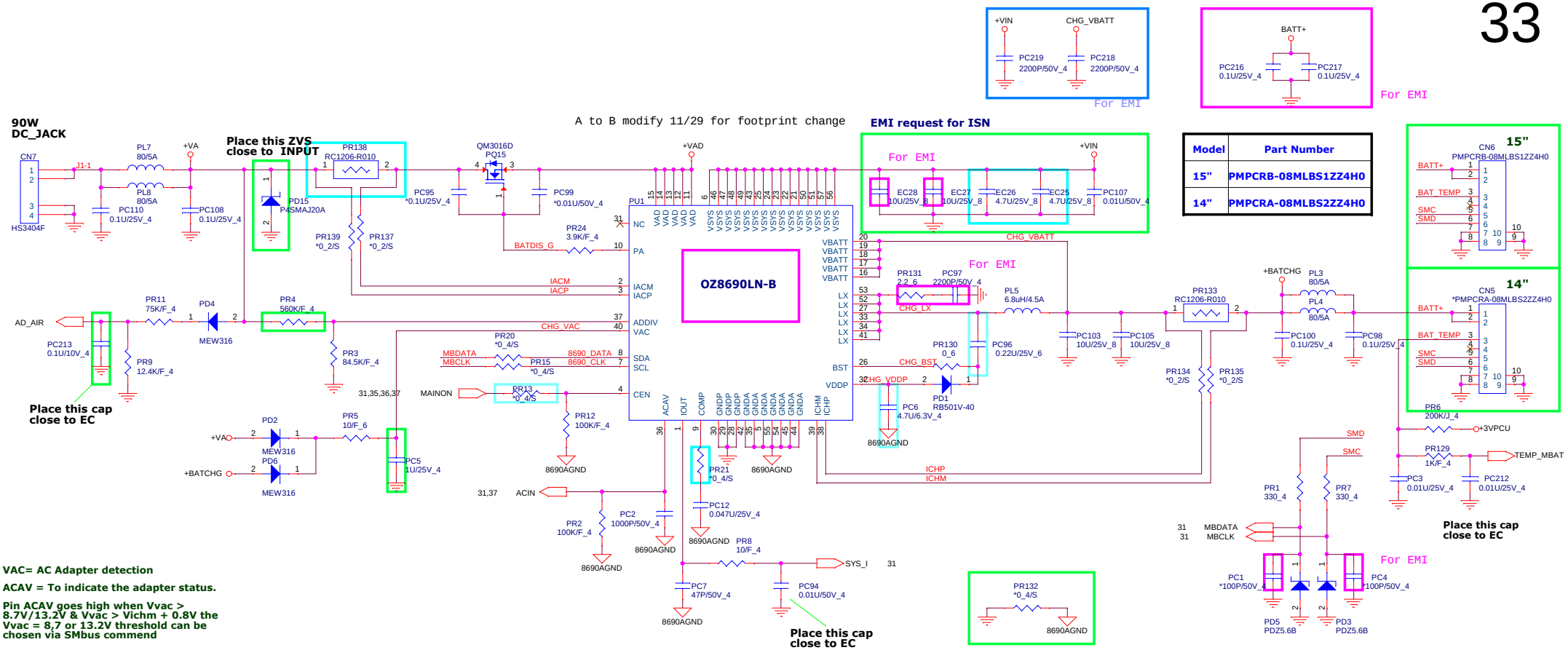
4,27,29,31,33,34 +3VPCU
21,26,28,29,37,40 +5V
2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,28,29,30,31,37,38,40 +3V

NB5

PROJECT : TWS
Quanta Computer Inc.

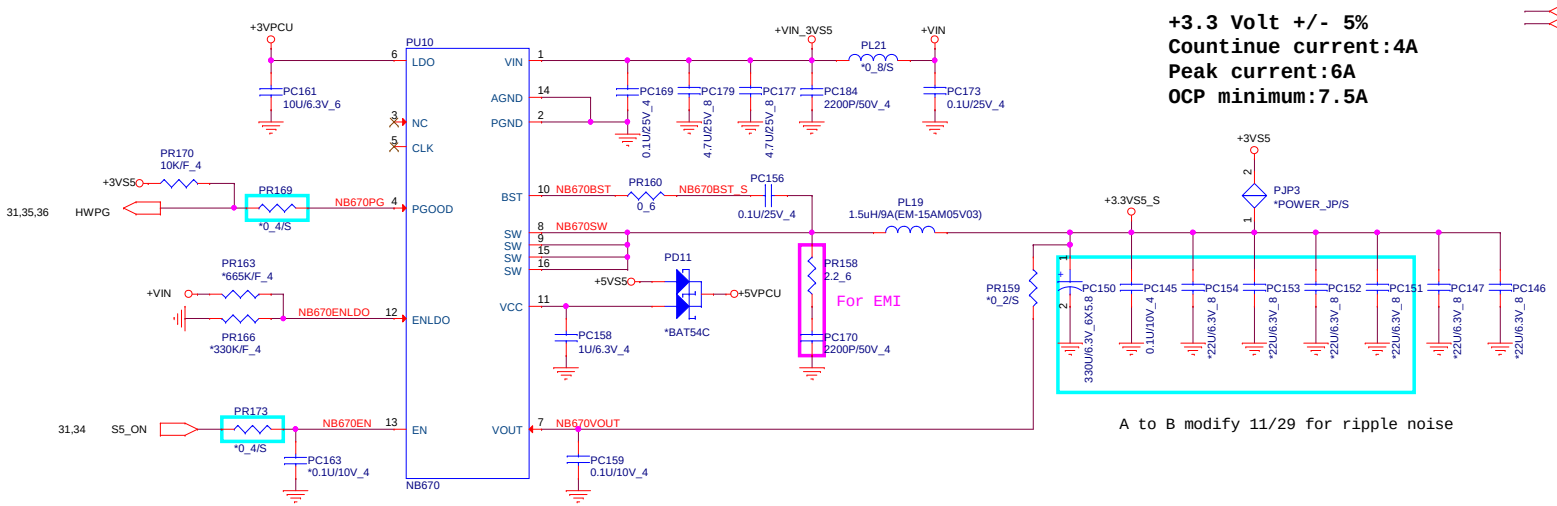
Size	Document Number	Rev
Custom	SW/TP/FAN/HDD/ODD/mSATA	1A

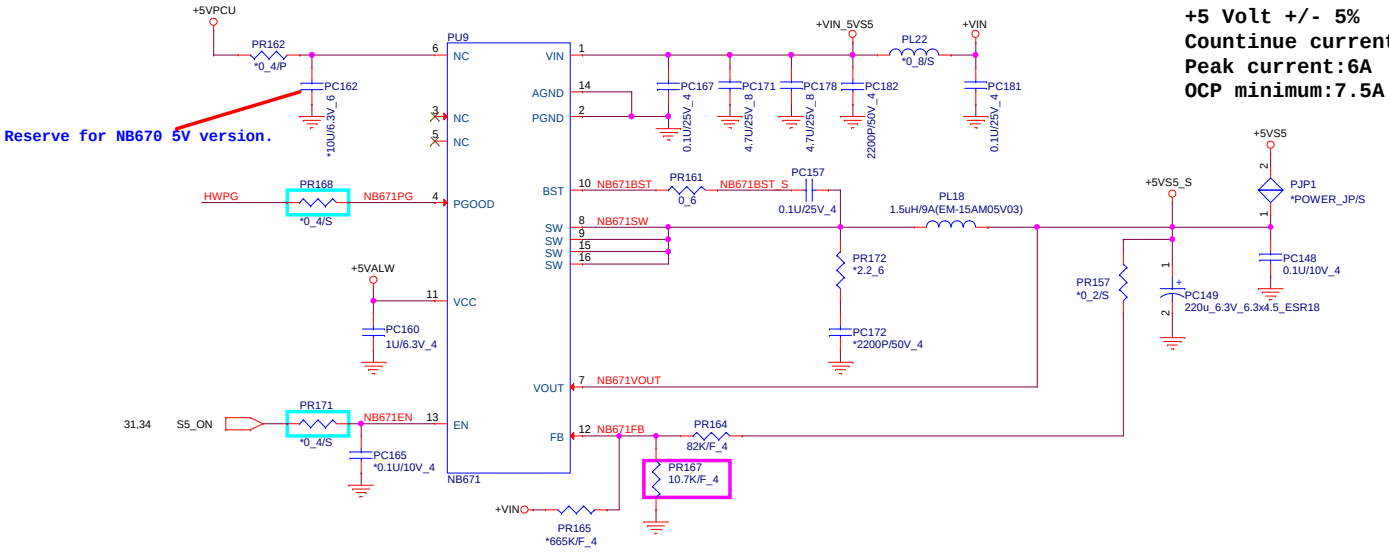
Date: Friday, August 16, 2013 | Sheet 32 of 43



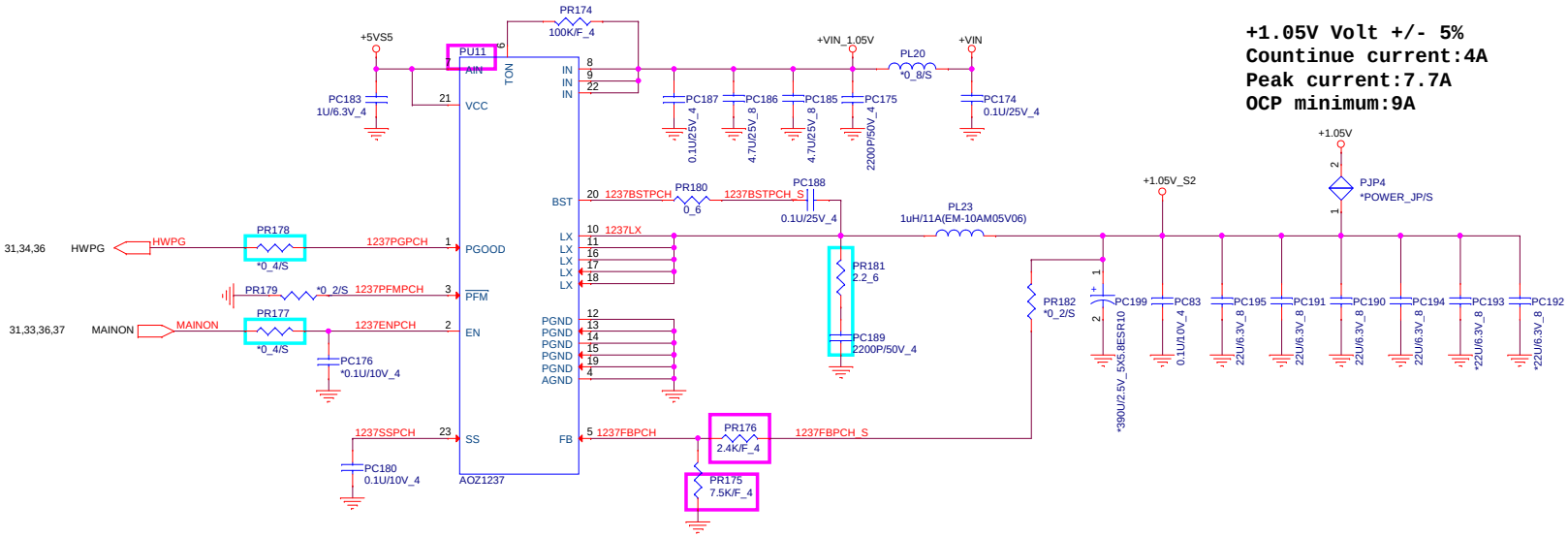
Model	Part Number
15"	PMPCRB-08MLBS1ZZ4H0
14"	PMPCRA-08MLBS2ZZ4H0

DC/DC +3VS5/+5VS5

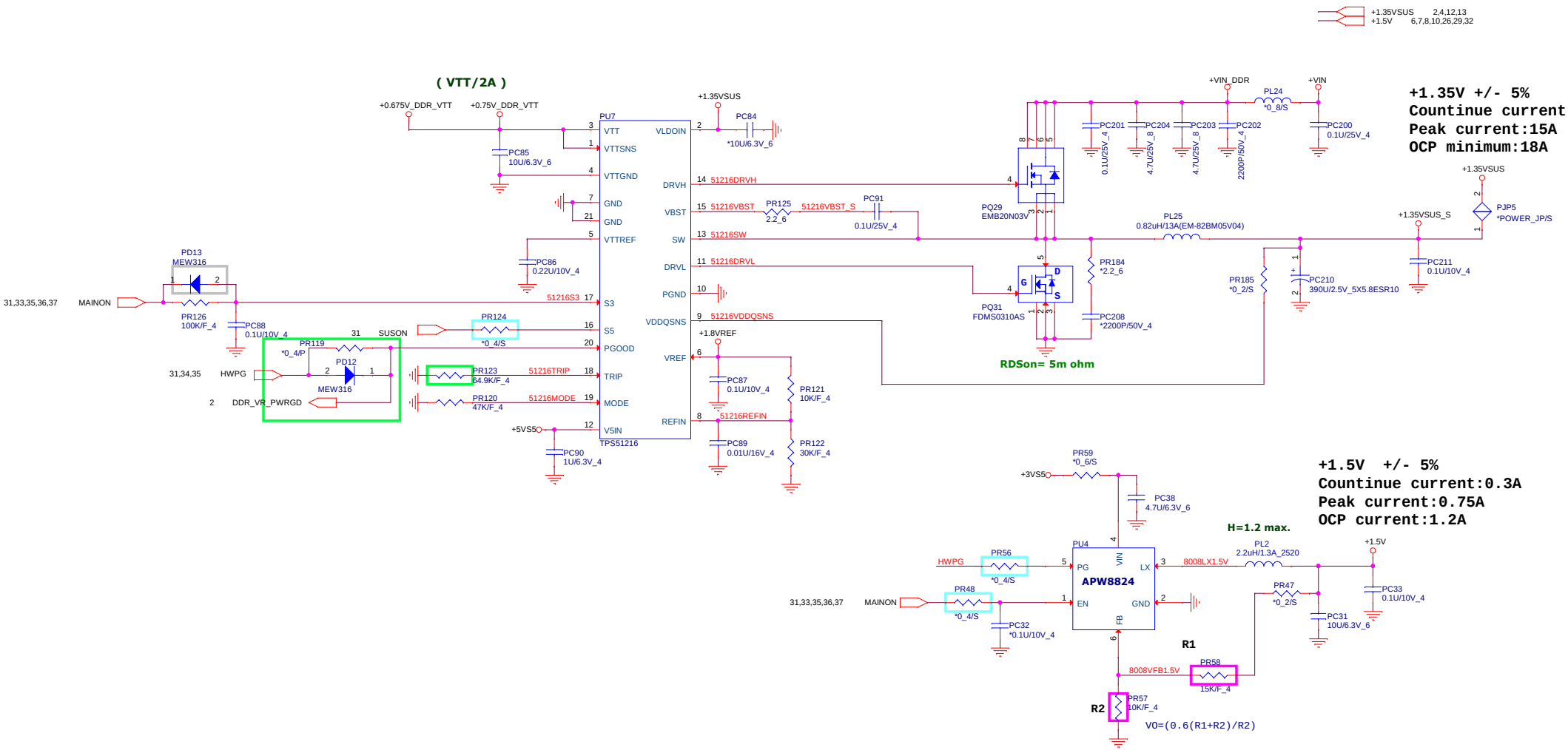




NB5	PROJECT : TWS Quanta Computer Inc.	
Size: Custom	Document Number: 3/5VPCU(RT8243A)	Rev: 1A
Date: Friday, August 16, 2013	Sheet 34 of 43	

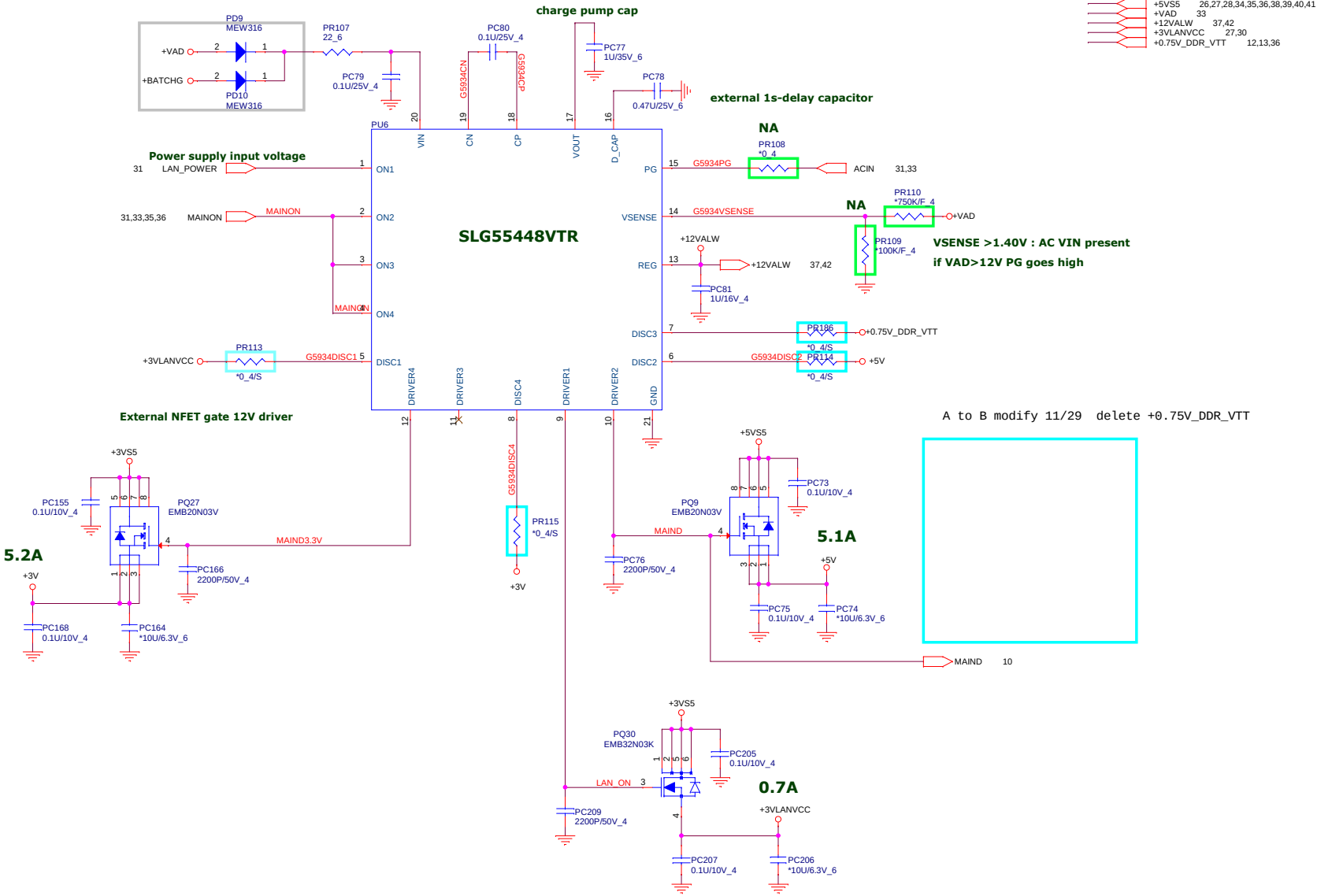


NB5	PROJECT : TWS Quanta Computer Inc.		
	Size: Custom	Document Number: 1.05V(RT8228BZ)	Rev: 1A
	Date: Friday, August 16, 2013	Sheet 35 of 43	

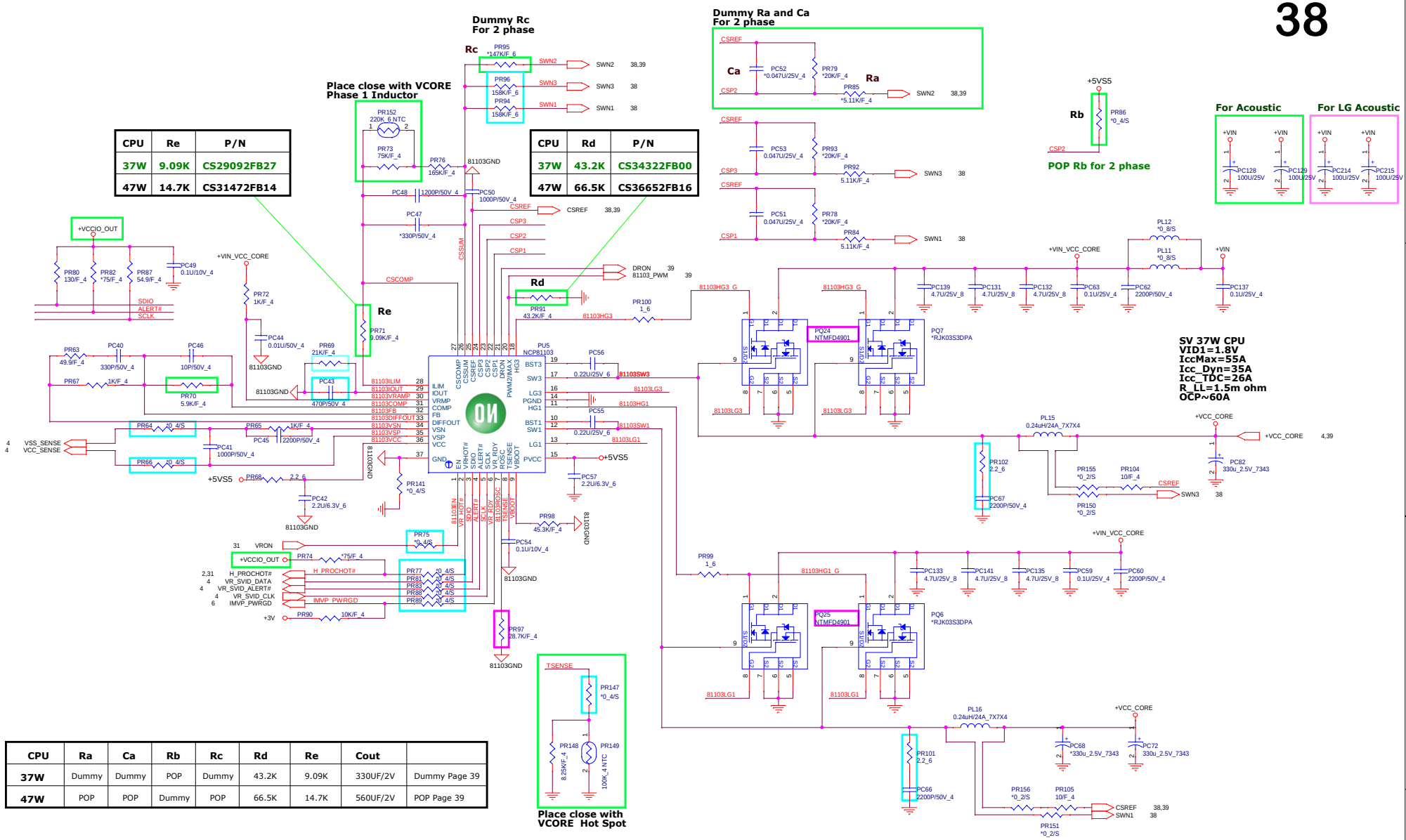


NB5	PROJECT : TWS Quanta Computer Inc.		
	Size: Custom	Document Number: DDR3L(APW8819)	Rev: 1A
	Date: Friday, August 16, 2013	Sheet 36 of 43	

+5V 21,26,28,29,32,40
+VIN 23,28,33,34,35,36,38,40,41,42
+1.5V 6,7,8,10,26,29,32,36
+3VS5 2,6,7,9,10,24,27,28,29,31,34,36,42
+5VS5 26,27,28,34,35,36,38,39,40,41
+VAD 33
+12VALW 37,42
+3VLANVCC 27,30
+0.75V_DDR_VTT 12,13,36



PROJECT : TWS	Quanta Computer Inc.
NB5	
Size: Custom	Document Number: Dis-charge IC (G5934)
Rev: 1A	
Date: Friday, August 16, 2013	Sheet 37 of 43

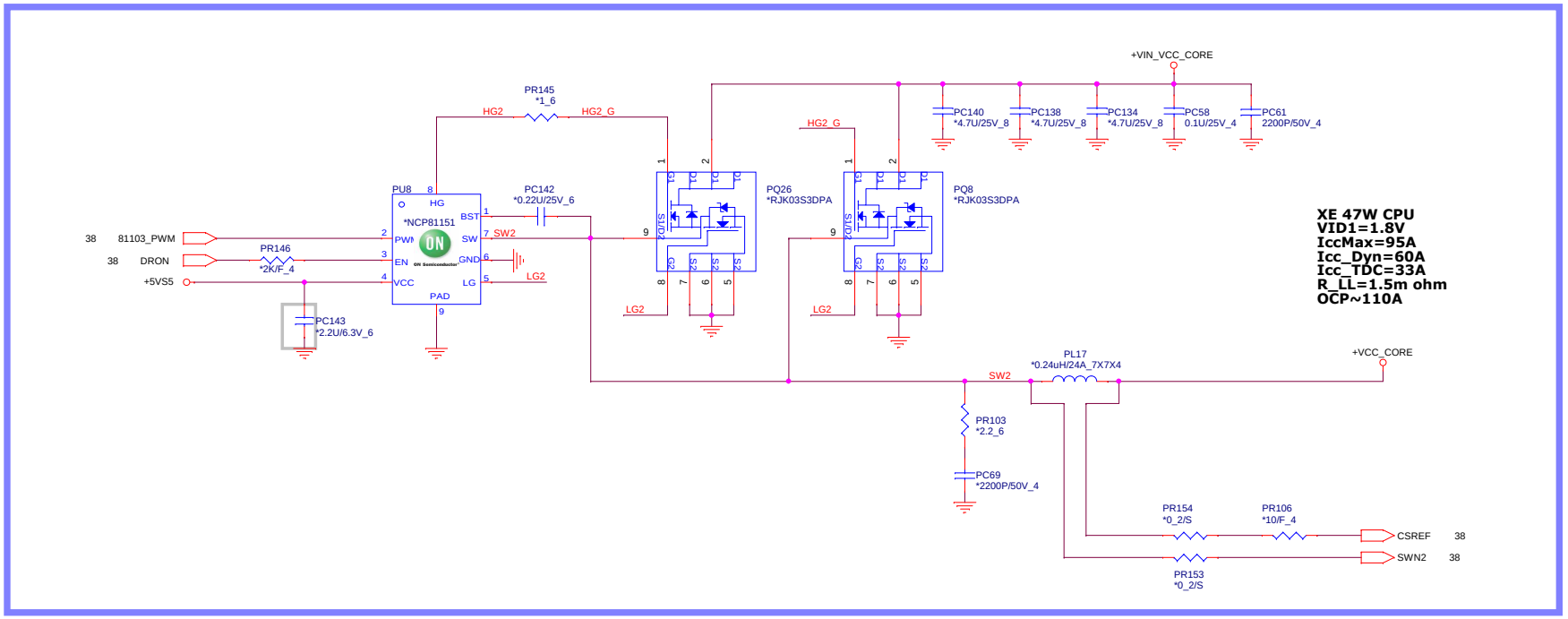


CPU	Re	P/N
37W	9.09K	CS29092FB27
47W	14.7K	CS31472FB14

CPU	Rd	P/N
37W	43.2K	CS34322FB00
47W	66.5K	CS36652FB16

CPU	Ra	Ca	Rb	Rc	Rd	Re	Cout	
37W	Dummy	Dummy	POP	Dummy	43.2K	9.09K	330UF/2V	Dummy Page 39
47W	POP	POP	Dummy	POP	66.5K	14.7K	560UF/2V	POP Page 39

Size	C
Document Number	Dis-charge IC (G5934)
Rev	1A
Date	Friday, August 16, 2013
Sheet	38 of 43

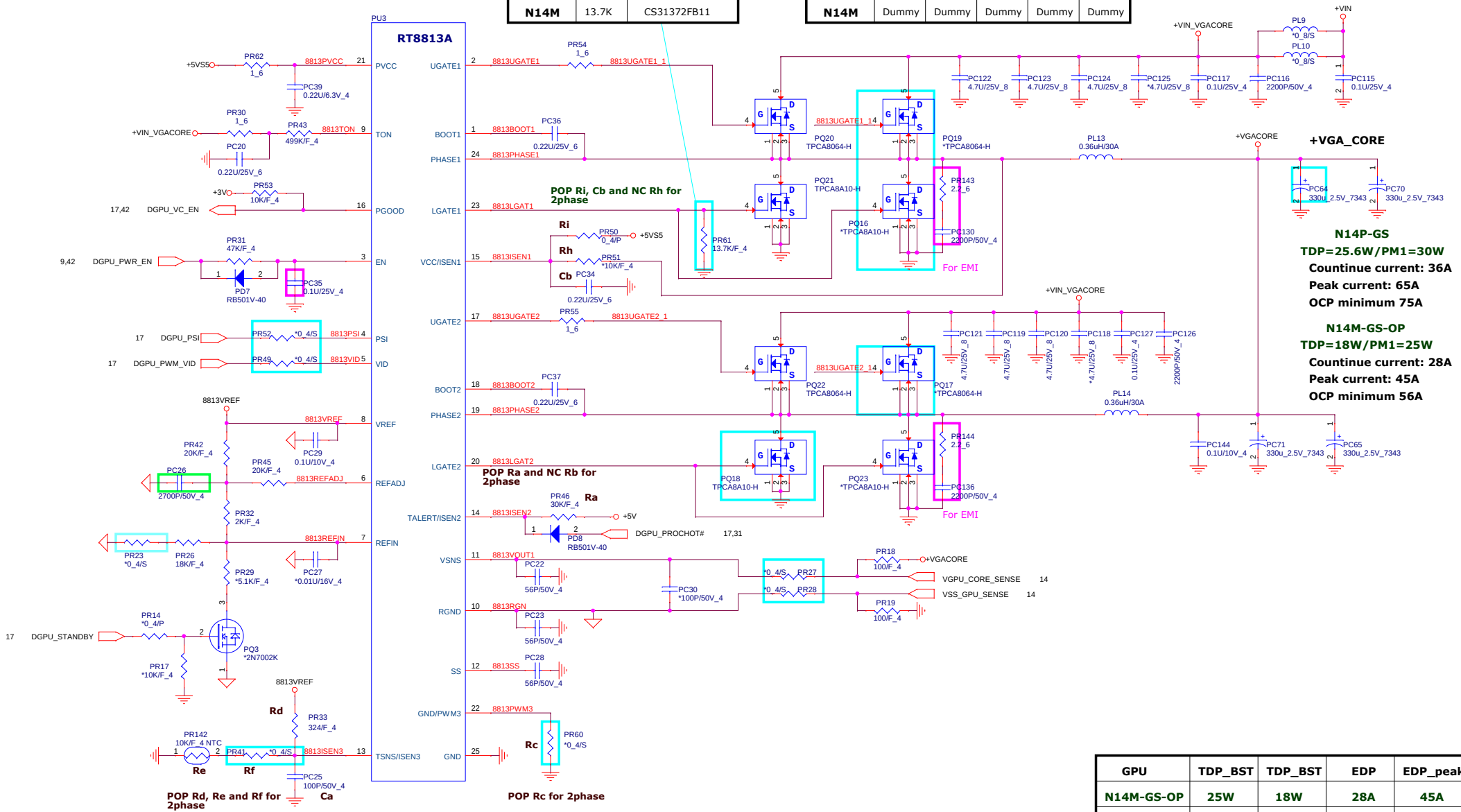


+VCC_CORE 4,38

NB5	PROJECT : TWS Quanta Computer Inc.	
Size: Custom	Document Number: NCP81151	Rev: 1A
Date: Friday, August 16, 2013	Sheet 39 of 43	

VGA OCP	PR61	P/N
N14P	9.31K	CS29312FB13
N14M	13.7K	CS31372FB11

VGA	PQ19	PQ16	PQ17	PQ18	PC64
N14P	POP	POP	POP	POP	POP
N14M	Dummy	Dummy	Dummy	Dummy	Dummy



N14P-GS
TDP=25.6W/PM1=30W
Countinue current: 36A
Peak current: 65A
OCP minimum 75A

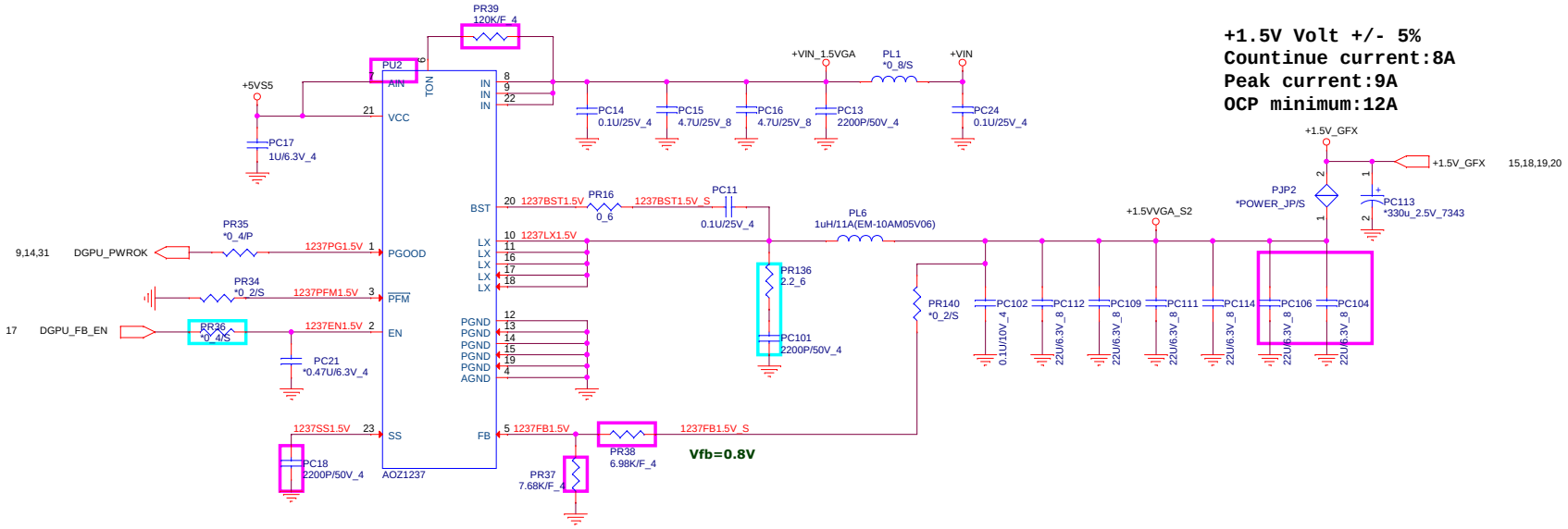
N14M-GS-OP
TDP=18W/PM1=25W
Countinue current: 28A
Peak current: 45A
OCP minimum 56A

GPU	TDP_BST	TDP_BST	EDP	EDP_peak
N14M-GS-OP	25W	18W	28A	45A
N14P-GS	30W	25.6W	36A	65A

NB5

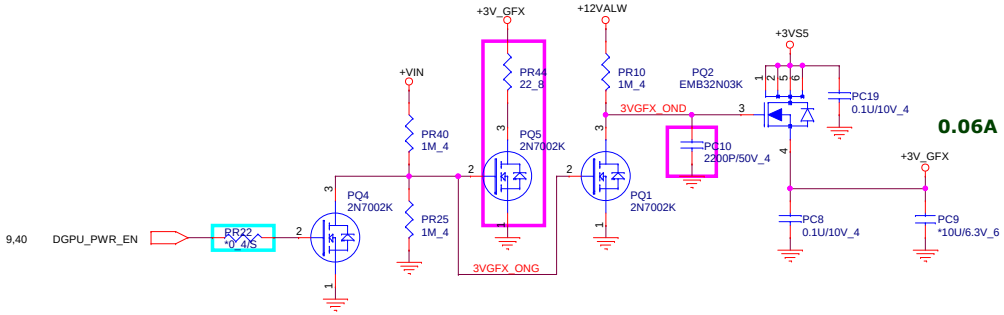
PROJECT : TWS
Quanta Computer Inc.

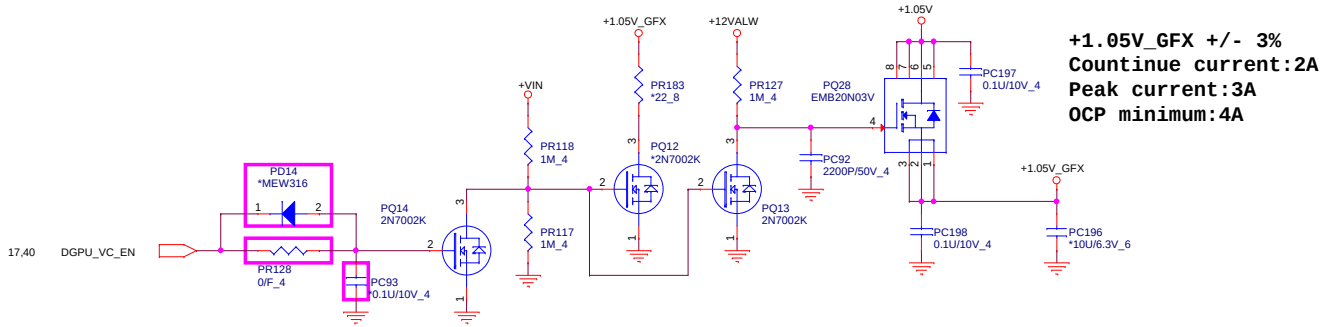
Size	Document Number	Rev
Custom	+VGA CORE (NCP3218G)	1A
Date: Friday, August 16, 2013	Sheet 40 of 43	



+1.5V Volt +/- 5%
Countinue current:8A
Peak current:9A
OCP minimum:12A

NB5	**PROJECT : TWS** Quanta Computer Inc.	
Size: Custom	Document Number: **+VGA POWER**	Rev: 1A
Date: Friday, August 16, 2013	Sheet 41 of 43	





NB5

PROJECT : TWS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A
Date: Friday, August 16, 2013	Sheet 42 of 43	