Diamond-3 Intel Calpella Platform with Discrete GFX

01

POWER

REGULATOR +1.05V_VTT	**CPU Core** VCC_CORE
REGULATOR 1.5VSUS, 0.75VSMDDR_VTERM,SMDDR_VREF	**DC/DC** 3.3PCU, 5VPCU, 15VPCU
REGULATOR +1.8V	**VGA Core** +VCC_GFX_CORE,+1.1V_GFX_PCIE

POWER

- **SYSTEM RESET CIRCUIT**
- **BATT CHARGER**
- **AC/BATT CONNECTOR**
- **RUN POWER SW** 3VSUS, 5VSUS, 3V_S5, 5V_S5 +3V, +5V

FAN / THERMAL G990P11U PG 3

CLOCK GEN SLG8SP585V(QFN32) PG 3 — 14.318MHz

DDR3 - SODIMM0 H=5.2 PG 14

DDR3 - SODIMM1 H=9.2 PG 15

Dual Channel DDR3 800/1067 1.5V

Arrandale (rPGA 989) P 4,5,6,7

PCIEx16

VRAM DDR3 x 4 (512M) PG 21

PCI-Express GFX AMD M92-S2 XT PG 16,17,18,19,20,21,22

LVDS — **LCD Connector** PG 23

DISPLAY PORT — **Display Port CONN.** PG 24

DISPLAY PORT — **DISPLAY PORT SWITCH** PI2PCIE412-DZHE PG 24

DISPLAY PORT(DP1)

DISPLAY PORT(DP0) — **Dock** P 40

VGA — **CRT Switch** SN74CBT3257CPWR PG 25

- **CRT CONN.(System)** PG 25
- **CRT CONN.(Dock)** PG 41

USB I/F
VGA I/F
RJ45
Dock Ctrl
DVI
Display Port(DP0,DP1)

SATA-ODD PG 29

SATA-HDD PG 29

32.768KHz — FDI — DMI X 4

PCH
Ibex Peak-M
Intel(R) 5 Series Express Chipset
P 8,9,10,11,12,13

SATA — **Re-Driver** PG 30 — **eSATA/USB Combo** PG 30

USB2.0 x 1 — **LAN (DOCK)** PG 41

AC-DC / **Battery** — **DC-DC**

Audio SPK conn PG 26

Audio Combo Jacks PG 26

Audio HP/MIC (Dock) PG 41

AUDIO ALC269 PG 26

SATA / SATA / IHDA

Camera + D-MIC PG 23 — USB2.0

FLASH 4Mbyts PG 42 — SPI

Bluetooth PG 36 — USB2.0

Biometric PG 31 — USB2.0

Card Reader /Finger Print /RF CONN. PG 31 — PCIEx1 / USB2.0

USB2.0 x 3 — **USB conn x 3** PG 30,31

PCIEx1 — **LAN Switch** PI3L500-AZFEX PG 27 — 25MHz — **LAN** RTL8111DL PG 28 — **RJ45/Magnetics** PG 28

PCIEx1 / USB2.0 — **EXPRESS-CARD** R5538 PG 34

PCIEx1 / USB2.0 — **MINI-CARD** WLAN/WiMAX PG 33

PCIEX1 / USB2.0 — **MINI-CARD** WWAN PG 32

32.768KHz — LPC — LPC

KBC ITE8502 PG 35

SPI / PS/2

- **FLASH 2Mbyts** PG 35
- **Touchpad** PG 37
- **Keyboard** PG 37
- **Accelerometer (APS)** PG 39
- **Discrete TPM** PG 39

PCB STACK UP 8L

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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17	HDMI PORT(PS8101)
18	CRT CONN
19	AUDIO CODEC(ALC269Q)
20	LAN(8111DL)
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22	USB X2/SIM_CARD/LEDs/RF
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25	MINI-Card (WLAN)
26	ONFI
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37	Charger (ISL88731)
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	16,36,37,38,39,40,41,42	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	9,12,34	RTC		S0~S5
3VPCU	+3.3V	9,16,20,23,28,32,34,36,37,40,42	ITE8502 POWER	3V5V_EN	S0~S5
5VPCU	+5V	36,37,38,39,40,42	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	16,31,36,38,39,40	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	20,36	LAN POWER	LAN_ON	
5V_S5	+5V	12,22,23,36	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	8,9,10,11,12,36	Sys Management,PCH Resume Well, Intel HD Audio,USB,WLAN,WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	16,32,36,41,42	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	8,23,27,34,36,42	SLP_S4# CTRLD POWER	SUSON	S0~S3
1.5VSUS	+1.5V	4,6,12,14,15,36,38,39	DDR3 SODIMM POWER	SUSON	S0~S3
0.75VSMDDR_VTERM	+0.75V	14,15,36,38	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	8,12,16,17,18,19,21,28,30,34,36,37	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3,4,8,9,10,11,12,14,15,16,17,18,19,20,21,22 23,24,25,26,27,29,30,31,32,33,34,36,37,38, 39,40,41,42,43	SLP_S3# CTRLD POWER	MAINON	S0
+1.8V	+1.8V	6,12,26,36,42	LVDS,NVM POWER	MAINON	S0
+1.5V	+1.5V	12,24,25,27,38,39	Mini PCIe,Express Card POWER	MAIND	S0
+1.05V_VTT	+1.05V	3,4,6,8,10,11,12,36,39,41,43	AuBurndale VTT POWER/PCH CORE POWER	MAINON	S0
+VCC_GFX_CORE		6,36,42	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		6,36,41	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	16	LCD Power	ENVDD	S0
+5V_ODD	+5V	21	ODD Power	MAINON#	S0
+5V_HDD	+5V	21	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	37	MAIN BATTERY	CHG_PBATT	S0~S5

PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Index & Power Status	1A

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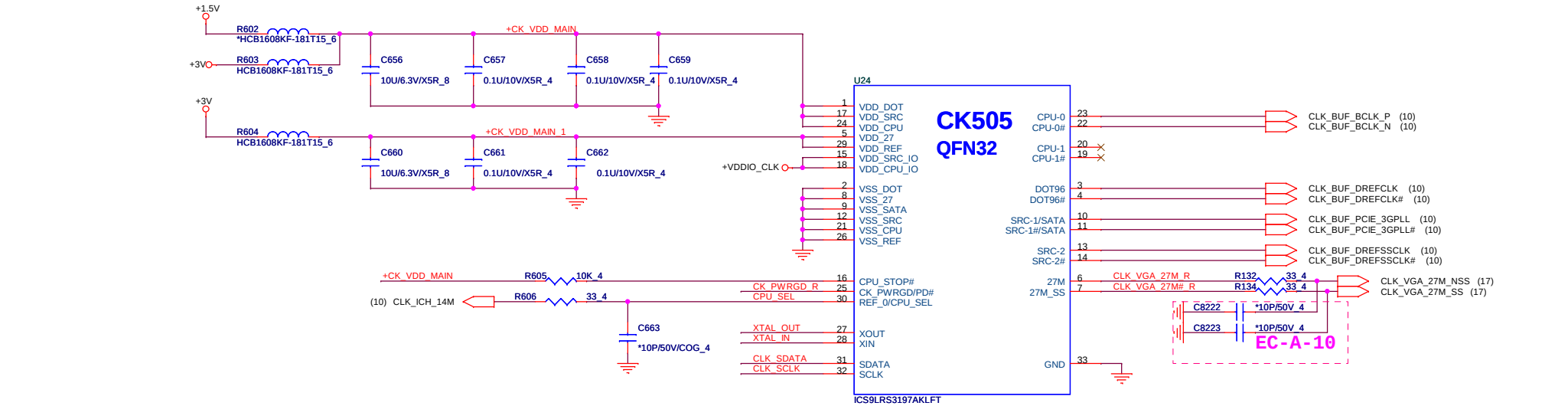
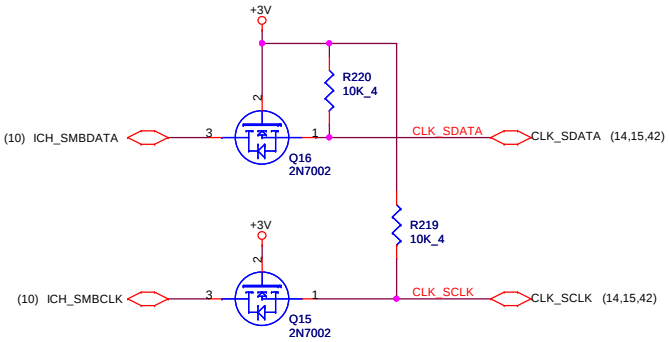
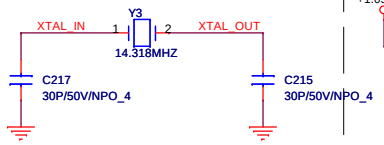
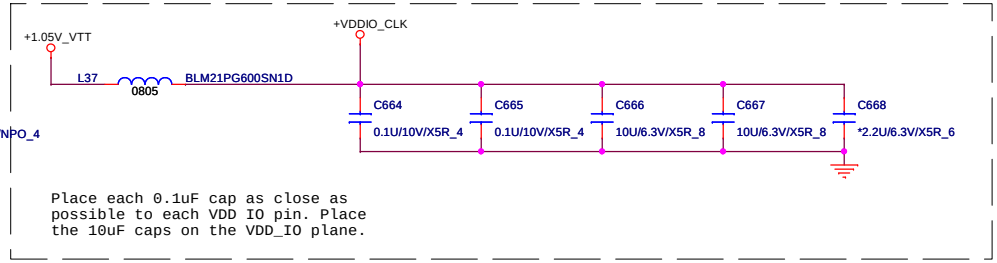
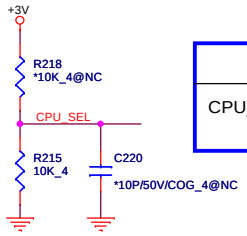
(4,8,9,10,11,12,14,15,17,23,24,25,26,28,29,30,31,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(4,6,8,9,10,11,12,44,47,49) +1.05V_VTT



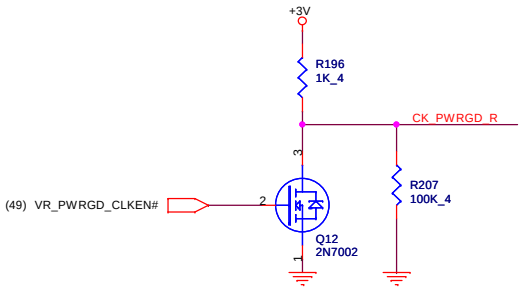








	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz



PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	1A

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ARRANDALE PROCESSOR (DMI,PEG,FDI)

ARRANDALE PROCESSOR (CLK,MISC,JTAG)

04

(3,8,9,10,11,12,14,15,17,23,24,25,26,28,29,30,31,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(3,6,8,9,10,11,12,44,47,49) +1.05V_VTT
(14,15,44,46,50) 1.5VSUS

U34A

DMI_TXN0 A24 DMI_RX#[0]
DMI_TXN1 C23 DMI_RX#[1]
DMI_TXN2 B22 DMI_RX#[2]
DMI_TXN3 A21 DMI_RX#[3]
DMI_TXP0 B24 DMI_RX[0]
DMI_TXP1 D23 DMI_RX[1]
DMI_TXP2 B23 DMI_RX[2]
DMI_TXP3 A22 DMI_RX[3]
DMI_RXN0 D24 DMI_TX#[0]
DMI_RXN1 G24 DMI_TX#[1]
DMI_RXN2 F23 DMI_TX#[2]
DMI_RXN3 H23 DMI_TX#[3]
DMI_RXP0 D25 DMI_TX[0]
DMI_RXP1 F24 DMI_TX[1]
DMI_RXP2 E23 DMI_TX[2]
DMI_RXP3 G23 DMI_TX[3]

DMI

FDI_TX#[0] E22
FDI_TX#[1] D21
FDI_TX#[2] D19
FDI_TX#[3] D18
FDI_TX#[4] G21
FDI_TX#[5] E19
FDI_TX#[6] F21
FDI_TX#[7] G18
FDI_TX[0] D22
FDI_TX[1] C21
FDI_TX[2] D20
FDI_TX[3] C18
FDI_TX[4] G22
FDI_TX[5] E20
FDI_TX[6] F20
FDI_TX[7] G19
FDI_FSYNC[0] F17
FDI_FSYNC[1] E17
FDI_INT C17
FDI_LSYNC[0] F18
FDI_LSYNC[1] D17

Intel(R) FDI

R9 1K/F_4 FDI_SYNC
R7 1K/F_4 FDI_SYNC

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI B26
PEG_ICOMPO A26
PEG_RCOMPO B27
PEG_RBIAS A25
R336 49.9/F_4
R338 750/F_4
PEG_RXN[0..15] (16)

PEG_RX#[0] K35 PEG_RXN15
PEG_RX#[1] J34 PEG_RXN14
PEG_RX#[2] J33 PEG_RXN13
PEG_RX#[3] G35 PEG_RXN12
PEG_RX#[4] G32 PEG_RXN11
PEG_RX#[5] F34 PEG_RXN10
PEG_RX#[6] F31 PEG_RXN9
PEG_RX#[7] D35 PEG_RXN8
PEG_RX#[8] E33 PEG_RXN7
PEG_RX#[9] C33 PEG_RXN6
PEG_RX#[10] D32 PEG_RXN5
PEG_RX#[11] B32 PEG_RXN4
PEG_RX#[12] C31 PEG_RXN3
PEG_RX#[13] B28 PEG_RXN2
PEG_RX#[14] B30 PEG_RXN1
PEG_RX#[15] A31 PEG_RXN0

PEG_RXP[0..15] (16)

PEG_RX[0] J35 PEG_RXP15
PEG_RX[1] H34 PEG_RXP14
PEG_RX[2] H33 PEG_RXP13
PEG_RX[3] F35 PEG_RXP12
PEG_RX[4] G33 PEG_RXP11
PEG_RX[5] E34 PEG_RXP10
PEG_RX[6] F32 PEG_RXP9
PEG_RX[7] D34 PEG_RXP8
PEG_RX[8] F33 PEG_RXP7
PEG_RX[9] B33 PEG_RXP6
PEG_RX[10] D31 PEG_RXP5
PEG_RX[11] A32 PEG_RXP4
PEG_RX[12] C30 PEG_RXP3
PEG_RX[13] A28 PEG_RXP2
PEG_RX[14] B29 PEG_RXP1
PEG_RX[15] A30 PEG_RXP0

PEG_TX#[0] L33 PEG_C_TXN15
PEG_TX#[1] M35 PEG_C_TXN14
PEG_TX#[2] M33 PEG_C_TXN13
PEG_TX#[3] M30 PEG_C_TXN12
PEG_TX#[4] L31 PEG_C_TXN11
PEG_TX#[5] K32 PEG_C_TXN10
PEG_TX#[6] M29 PEG_C_TXN9
PEG_TX#[7] J31 PEG_C_TXN8
PEG_TX#[8] K29 PEG_C_TXN7
PEG_TX#[9] H30 PEG_C_TXN6
PEG_TX#[10] H29 PEG_C_TXN5
PEG_TX#[11] F29 PEG_C_TXN4
PEG_TX#[12] E28 PEG_C_TXN3
PEG_TX#[13] D29 PEG_C_TXN2
PEG_TX#[14] D27 PEG_C_TXN1
PEG_TX#[15] C26 PEG_C_TXN0

PEG_TX[0] L34 PEG_C_TXP15
PEG_TX[1] M34 PEG_C_TXP14
PEG_TX[2] M32 PEG_C_TXP13
PEG_TX[3] L30 PEG_C_TXP12
PEG_TX[4] M31 PEG_C_TXP11
PEG_TX[5] K31 PEG_C_TXP10
PEG_TX[6] M28 PEG_C_TXP9
PEG_TX[7] H31 PEG_C_TXP8
PEG_TX[8] K28 PEG_C_TXP7
PEG_TX[9] G30 PEG_C_TXP6
PEG_TX[10] G29 PEG_C_TXP5
PEG_TX[11] F28 PEG_C_TXP4
PEG_TX[12] E27 PEG_C_TXP3
PEG_TX[13] D28 PEG_C_TXP2
PEG_TX[14] C27 PEG_C_TXP1
PEG_TX[15] C25 PEG_C_TXP0

IC_AUB_CFD_rPGA_R0P9

U34B

H_COMP3 AT23 COMP3
H_COMP2 AT24 COMP2
H_COMP1 G16 COMP1
H_COMP0 AT26 COMP0
TP21 TP_SKT0CC# AH24 SKTOCC#
H_CATERR# AK14 CATERR#
(11) H_PECI H_PECI_ISO AT15 PECI
(49) H_PROCHOT# AN26 H_PROCHOT# PROCHOT#
(11) PM_THRMTRIP# AK15 THERMTRIP#
TP22 H_CPURST# AP26 RESET_OBS#
(8) PM_SYNC AL15 PM_SYNC
SYS_AGENT_PWROK AN14 VCCPWRGOOD_1
AN27 VCCPWRGOOD_0
TP24 (8) PM_DRAM_PWRGD PM_DRAM_PWRGD AK13 SM_DRAMPWROK
H_VTTPWRGD AM15 VTTPWRGOOD
TP123 H_PWRGD_XDP AM26 TAPPWRGOOD
(10,28,31,32,33,34,39,42) PLTRST# R214 1.5K/F_4 AL14 RSTIN#
R213 750/F_4

MISC THERMAL PWR MANAGEMENT

IC_AUB_CFD_rPGA_R0P9

CLOCKS

BCLK A16 CLK_CPU_BCLK (11)
BCLK# B16 CLK_CPU_BCLK# (11)
BCLK_ITP AR30 TP75
BCLK_ITP# AT30 TP76
PEG_CLK E16 CLK_PCIE_3GPLL (10)
PEG_CLK# D16 CLK_PCIE_3GPLL# (10)
DPLL_REF_SSCLK A18
DPLL_REF_SSCLK# A17

DDR3 MISC

SM_DRAMRST# F6 CPUDRAMRST#
SM_RCOMP[0] AL1 SM_RCOMP_0
SM_RCOMP[1] AM1 SM_RCOMP_1
SM_RCOMP[2] AN1 SM_RCOMP_2
+1.05V_VTT
PM_EXT_TS#[0] AN15 R200 10K_4
PM_EXT_TS#[1] AP15 R197 10K_4
R201 0_4 PM_EXTTS#0 (14)
R198 0_4 PM_EXTTS#1 (15)

JTAG & BPM

PRDY# AT29 XDP_PRDY# TP61
PREQ# AP27 XDP_PREQ# TP62
TCK AN28 XDP_TCK TP19
TMS AP28 XDP_TMS TP20
TRST# AT27 XDP_TRST# TP59
TDI AT29 XDP_TDI_R TP56
TDO AR27 XDP_TDO_R TP60
TDI_M AR29 XDP_TDI_M TP57
TDO_M AP29 XDP_TDO_M TP58
DBR# AN25 XDP_DBRESET# (8)
BPM#[0] AJ22 XDP_OBS0 TP77
BPM#[1] AK22 XDP_OBS1 TP78
BPM#[2] AK24 XDP_OBS2 TP79
BPM#[3] AJ24 XDP_OBS3 TP80
BPM#[4] AJ25 XDP_OBS4 TP81
BPM#[5] AH22 XDP_OBS5 TP118
BPM#[6] AK23 XDP_OBS6 TP119
BPM#[7] AH23 XDP_OBS7 TP120

Layout Note:
Place this test point on top side

U23
74AHCT1G08GW
(35,42,46,47,48,49,50,51) HWPG
R212 2K/F_4 H_VTTPWRGD
R211 1K_4

For S3 Power Saving

3V_S5 +1.5VCPU
R611 8.2K_4
0.1U/10V/X7R_4 C669
R612 *1.1K/F_4
+1.5VCPU_PG 2 DRAMPWRGD_CPU R613 1.5K/F_4 PM_DRAM_PWRGD
U51
TC7SH08FU(F)
R617 750/F_4

For S3 Power Saving

3V_S5
R610 10K_4
R608 10K_4
+1.5VCPU_PG +1.5VCPU_PG (46)
Q30
MMBT3904
R614 10K_4
Q32
PDTC143TT
C671 1U/6.3V/X5R_4

For S3 Power Saving

1.5VSUS
R607 1K_4
R609 *0_4
Q31
ME2N7002E
(14,15) DDR3_DRAMRST# CPUDRAMRST#
(35) DRAMRST_CTRL_EC R615 *0_4
(10) DRAMRST_CTRL_PCH R618 0_4
R616 100K_4
C670 0.047U/10V_4

+1.05V_VTT
XDP_TMS R186 51_4
XDP_TDI_R R335 51_4
XDP_PREQ# R191 *51_4@NC
XDP_TCK R184 51_4

JTAG MAPPING

XDP_TDI_R R337 0_4 XDP_TDI
XDP_TDO_M R341 *0_4@NC XDP_TDO
R340 0_4
XDP_TRST# R342 51_4
XDP_TDI_M R339 *0_4@NC
XDP_TDO_R R343 0_4

Scan Chain (Default)	STUFF -> R337, R340, R343 NO STUFF -> R341, R339
CPU Only	STUFF -> R337, R341 NO STUFF -> R340, R339, R343
GMCH Only	STUFF -> R339, R343 NO STUFF -> R337, R341, R340

PEG_C_TXN15 C604 0.1U/10V/X5R_4 PEG_TXN15
PEG_C_TXN14 C596 0.1U/10V/X5R_4 PEG_TXN14
PEG_C_TXN13 C593 0.1U/10V/X5R_4 PEG_TXN13
PEG_C_TXN12 C587 0.1U/10V/X5R_4 PEG_TXN12
PEG_C_TXN11 C579 0.1U/10V/X5R_4 PEG_TXN11
PEG_C_TXN10 C577 0.1U/10V/X5R_4 PEG_TXN10
PEG_C_TXN9 C572 0.1U/10V/X5R_4 PEG_TXN9
PEG_C_TXN8 C564 0.1U/10V/X5R_4 PEG_TXN8
PEG_C_TXN7 C560 0.1U/10V/X5R_4 PEG_TXN7
PEG_C_TXN6 C556 0.1U/10V/X5R_4 PEG_TXN6
PEG_C_TXN5 C552 0.1U/10V/X5R_4 PEG_TXN5
PEG_C_TXN4 C543 0.1U/10V/X5R_4 PEG_TXN4
PEG_C_TXN3 C540 0.1U/10V/X5R_4 PEG_TXN3
PEG_C_TXN2 C536 0.1U/10V/X5R_4 PEG_TXN2
PEG_C_TXN1 C526 0.1U/10V/X5R_4 PEG_TXN1
PEG_C_TXN0 C524 0.1U/10V/X5R_4 PEG_TXN0
PEG_TXN[0..15] (16)

PEG_C_TXP15 C598 0.1U/10V/X5R_4 PEG_TXP15
PEG_C_TXP14 C594 0.1U/10V/X5R_4 PEG_TXP14
PEG_C_TXP13 C588 0.1U/10V/X5R_4 PEG_TXP13
PEG_C_TXP12 C580 0.1U/10V/X5R_4 PEG_TXP12
PEG_C_TXP11 C578 0.1U/10V/X5R_4 PEG_TXP11
PEG_C_TXP10 C573 0.1U/10V/X5R_4 PEG_TXP10
PEG_C_TXP9 C568 0.1U/10V/X5R_4 PEG_TXP9
PEG_C_TXP8 C561 0.1U/10V/X5R_4 PEG_TXP8
PEG_C_TXP7 C557 0.1U/10V/X5R_4 PEG_TXP7
PEG_C_TXP6 C553 0.1U/10V/X5R_4 PEG_TXP6
PEG_C_TXP5 C546 0.1U/10V/X5R_4 PEG_TXP5
PEG_C_TXP4 C541 0.1U/10V/X5R_4 PEG_TXP4
PEG_C_TXP3 C537 0.1U/10V/X5R_4 PEG_TXP3
PEG_C_TXP2 C529 0.1U/10V/X5R_4 PEG_TXP2
PEG_C_TXP1 C525 0.1U/10V/X5R_4 PEG_TXP1
PEG_C_TXP0 C523 0.1U/10V/X5R_4 PEG_TXP0
PEG_TXP[0..15] (16)

Processor Pullups

+1.05V_VTT
R199 49.9/F_4
R192 68_4
R193 *68_4@NC
H_CATERR#
H_PROCHOT#
H_CPURST#

(8,49) DELAY_VR_PWRGOOD R205 *0_4@NC SYS_AGENT_PWROK
(11) H_PWRGOOD R206 0_4

Platform REFDES	ERB	CRB
R205	STUFF	NO_STUFF
R206	NO_STUFF	STUFF

Processor Compensation Signals

H_COMP0
H_COMP1
H_COMP2
H_COMP3
R344 49.9/F_4
R195 49.9/F_4
R345 20/F_4
R346 20/F_4

DDR3 Compensation Signals

SM_RCOMP_2
SM_RCOMP_1
SM_RCOMP_0
R355 130/F_4
R354 24.9/F_4
R353 100/F_4
Layout Note: Place these resistors near Processor

PROJECT: GC9A
Quanta Computer Inc.

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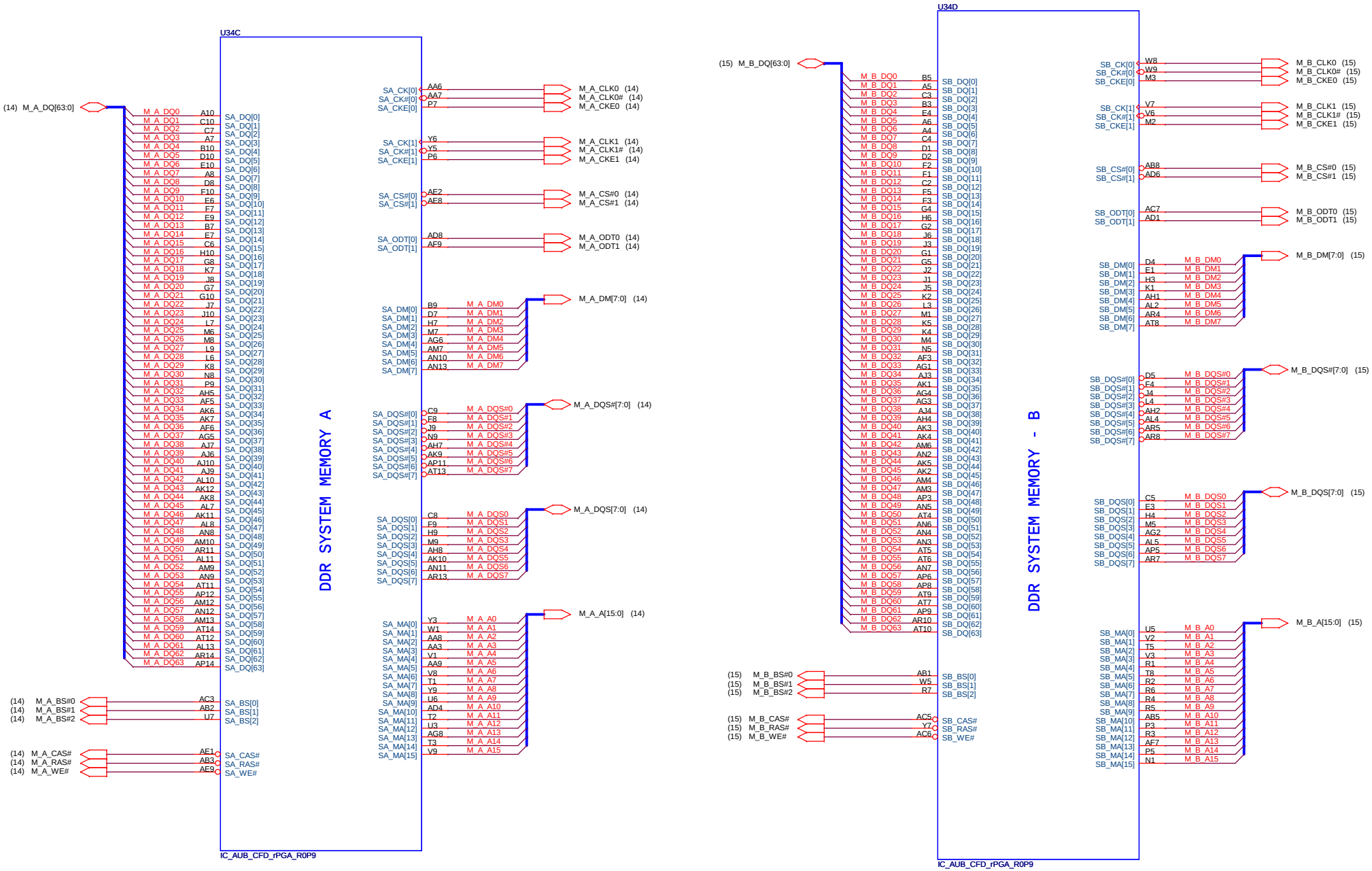
ARRANDALE PROCESSOR (DDR3)

05



PROJECT: GC9A Quanta Computer Inc.		
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(44,49) VCC_CORE
(3,4,8,9,10,11,12,44,47,49) +1.05V_VTT
(4,14,15,44,46,50) 1.5VSUS
(10,12,17,18,21,22,24,44,51) +1.8V

CPU Core Power

AUBURNDALE PROCESSOR (POWER)

U34F

VCC_CORE

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
V35 VCC61
V34 VCC62
V33 VCC63
V32 VCC64
V31 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

1.1V RAIL POWER

VTT0_1 AH14
VTT0_2 AH12
VTT0_3 AH11
VTT0_4 AH10
VTT0_5 J14
VTT0_6 J13
VTT0_7 H14
VTT0_8 H12
VTT0_9 G14
VTT0_10 G13
VTT0_11 G12
VTT0_12 G11
VTT0_13 F14
VTT0_14 F13
VTT0_15 F12
VTT0_16 F11
VTT0_17 E14
VTT0_18 E12
VTT0_19 D14
VTT0_20 D13
VTT0_21 D12
VTT0_22 D11
VTT0_23 C14
VTT0_24 C13
VTT0_25 C12
VTT0_26 C11
VTT0_27 B14
VTT0_28 B12
VTT0_29 A14
VTT0_30 A13
VTT0_31 A12
VTT0_32 A11

+1.05V_VTT

C372 10U/10V/X5R_8
C371 10U/10V/X5R_8
C377 10U/10V/X5R_8
C378 10U/10V/X5R_8
C375 10U/10V/X5R_8
C376 10U/10V/X5R_8
C373 *10U/10V/X5R_8@NC
C374 *10U/10V/X5R_8@NC
C380 10U/10V/X5R_8
C379 22U/6.3V/X5R_8
C208 22U/6.3V/X5R_8
C207 22U/6.3V/X5R_8

CPU CORE SUPPLY

VTT0_33 AF10
VTT0_34 AE10
VTT0_35 AC10
VTT0_36 AB10
VTT0_37 Y10
VTT0_38 W10
VTT0_39 U10
VTT0_40 T10
VTT0_41 J12
VTT0_42 J11
VTT0_43 J16
VTT0_44 J15

+1.05V_VTT

C209 22U/6.3V/X5R_8
C210 22U/6.3V/X5R_8

POWER

CPU VIDS

PSI# AN33 H_PSI# (49)

VID[0] AK35 CPU_VID0 CPU_VID0 (49)
VID[1] AK33 CPU_VID1 CPU_VID1 (49)
VID[2] AK34 CPU_VID2 CPU_VID2 (49)
VID[3] AL35 CPU_VID3 CPU_VID3 (49)
VID[4] AL33 CPU_VID4 CPU_VID4 (49)
VID[5] AM33 CPU_VID5 CPU_VID5 (49)
VID[6] AM35 CPU_VID6 CPU_VID6 (49)
PROC_DPRSLPVR AM34 DPRSLPVR DPRSLPVR (49)

VTT_SELECT G15 H_VTTVID1 TP23

SENSE LINES

ISENSE AN35 IMON (49)

VCC_SENSE AJ34 VCCSENSE (49)
VSS_SENSE AJ35 VSSSENSE (49)

VTT_SENSE B15 VTT_SENSE (47)
VSS_SENSE_VTT A15

VCC_CORE

R168 100_4
R167 100_4

IC_AUB_CFD_rPGA_R0P9

ARRANDALE PROCESSOR (GRAPHICS POWER)

U34G

AT21 VAXG1
AT19 VAXG2
AT18 VAXG3
AT16 VAXG4
AR21 VAXG5
AR19 VAXG6
AR18 VAXG7
AR16 VAXG8
AP21 VAXG9
AP19 VAXG10
AP18 VAXG11
AP16 VAXG12
AN21 VAXG13
AN19 VAXG14
AN18 VAXG15
AN16 VAXG16
AM21 VAXG17
AM19 VAXG18
AM18 VAXG19
AM16 VAXG20
AL21 VAXG21
AL19 VAXG22
AL18 VAXG23
AL16 VAXG24
AK21 VAXG25
AK19 VAXG26
AK18 VAXG27
AK16 VAXG28
AJ21 VAXG29
AJ19 VAXG30
AJ18 VAXG31
AJ16 VAXG32
AH21 VAXG33
AH19 VAXG34
AH18 VAXG35
AH16 VAXG36

GRAPHICS POWER

SENSE LINES

VAXG_SENSE AR22
VSSAXG_SENSE AT22

GRAPHICS VIDS

GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24

GFX_VR_EN AR25
GFX_DPRSLPVR AT25
GFX_IMON AM24

R127 1K_4

DDR3 - 1.5V RAILS

+1.5VCPU

VDDQ1 AJ1
VDDQ2 AF1
VDDQ3 AE7
VDDQ4 AE4
VDDQ5 AC1
VDDQ6 AB7
VDDQ7 AB4
VDDQ8 Y1
VDDQ9 W7
VDDQ10 W4
VDDQ11 U1
VDDQ12 T7
VDDQ13 T4
VDDQ14 P1
VDDQ15 N7
VDDQ16 N4
VDDQ17 L1
VDDQ18 H1

C225 1U/6.3V/X5R_4
C222 1U/6.3V/X5R_4
C223 1U/6.3V/X5R_4
C221 1U/6.3V/X5R_4
C224 1U/6.3V/X5R_4
C240 22U/6.3V/X5R_8
C239 22U/6.3V/X5R_8
C251 *330u_2.5V_7343@NC

PEG & DMI

+1.05V_VTT

C365 22U/6.3V/X5R_8
C194 22U/6.3V/X5R_8

J24 VTT1_45
J23 VTT1_46
H25 VTT1_47

C358 22U/6.3V/X5R_8
C187 22U/6.3V/X5R_8
C356 22U/6.3V/X5R_8
C370 22U/6.3V/X5R_8

K26 VTT1_48
J27 VTT1_49
J26 VTT1_50
J25 VTT1_51
H27 VTT1_52
G28 VTT1_53
G27 VTT1_54
G26 VTT1_55
F26 VTT1_56
E26 VTT1_57
E25 VTT1_58

1.1V

+1.05V_VTT

VTT0_59 P10
VTT0_60 N10
VTT0_61 L10
VTT0_62 K10

C211 10U/6.3V/X5R_6
C218 10U/6.3V/X5R_6

VTT1_63 J22
VTT1_64 J20
VTT1_65 J18
VTT1_66 H21
VTT1_67 H20
VTT1_68 H19

C366 22U/6.3V/X5R_8
C203 22U/6.3V/X5R_8

1.8V

+1.8V

VCCPLL1 L26
VCCPLL2 L27
VCCPLL3 M26

C181 1U/6.3V/X5R_4
C186 1U/6.3V/X5R_4
C178 2.2U/6.3V/X5R_6
C172 4.7U/6.3V/X5R_6
C152 22U/6.3V/X5R_8

IC_AUB_CFD_rPGA_R0P9

+1.05V_VTT

R318 1K_4
R156 1K_4
R319 1K_4
R320 *1K_4@NC
R157 *1K_4@NC
R158 1K_4
R321 *1K_4@NC
R322 1K_4
R323 *1K_4@NC

CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
CPU_VID5
CPU_VID6
DPRSLPVR
H_PSI#

R324 *1K_4@NC
R161 *1K_4@NC
R325 *1K_4@NC
R326 1K_4
R162 1K_4
R163 *1K_4@NC
R327 1K_4
R328 *1K_4@NC
R329 1K_4

VCC_CORE

C359 22U/6.3V/X5R_8
C363 22U/6.3V/X5R_8
C361 22U/6.3V/X5R_8
C364 22U/6.3V/X5R_8
C192 22U/6.3V/X5R_8
C191 22U/6.3V/X5R_8
C189 22U/6.3V/X5R_8

C362 22U/6.3V/X5R_8
C190 22U/6.3V/X5R_8
C188 22U/6.3V/X5R_8
C193 22U/6.3V/X5R_8
C360 22U/6.3V/X5R_8
C146 10U/6.3V/X5R_6
C147 10U/6.3V/X5R_6

C144 10U/6.3V/X5R_6
C174 10U/6.3V/X5R_6
C179 10U/6.3V/X5R_6
C148 10U/6.3V/X5R_6
C145 10U/6.3V/X5R_6
C149 10U/6.3V/X5R_6
C150 10U/6.3V/X5R_6

C185 10U/6.3V/X5R_6
C176 10U/6.3V/X5R_6
C151 10U/6.3V/X5R_6
C184 10U/6.3V/X5R_6
C175 10U/6.3V/X5R_6
C177 10U/6.3V/X5R_6
C173 10U/6.3V/X5R_6

C183 0.1U/10V/X5R_4
C182 0.1U/10V/X5R_4

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Quanta Computer Inc.

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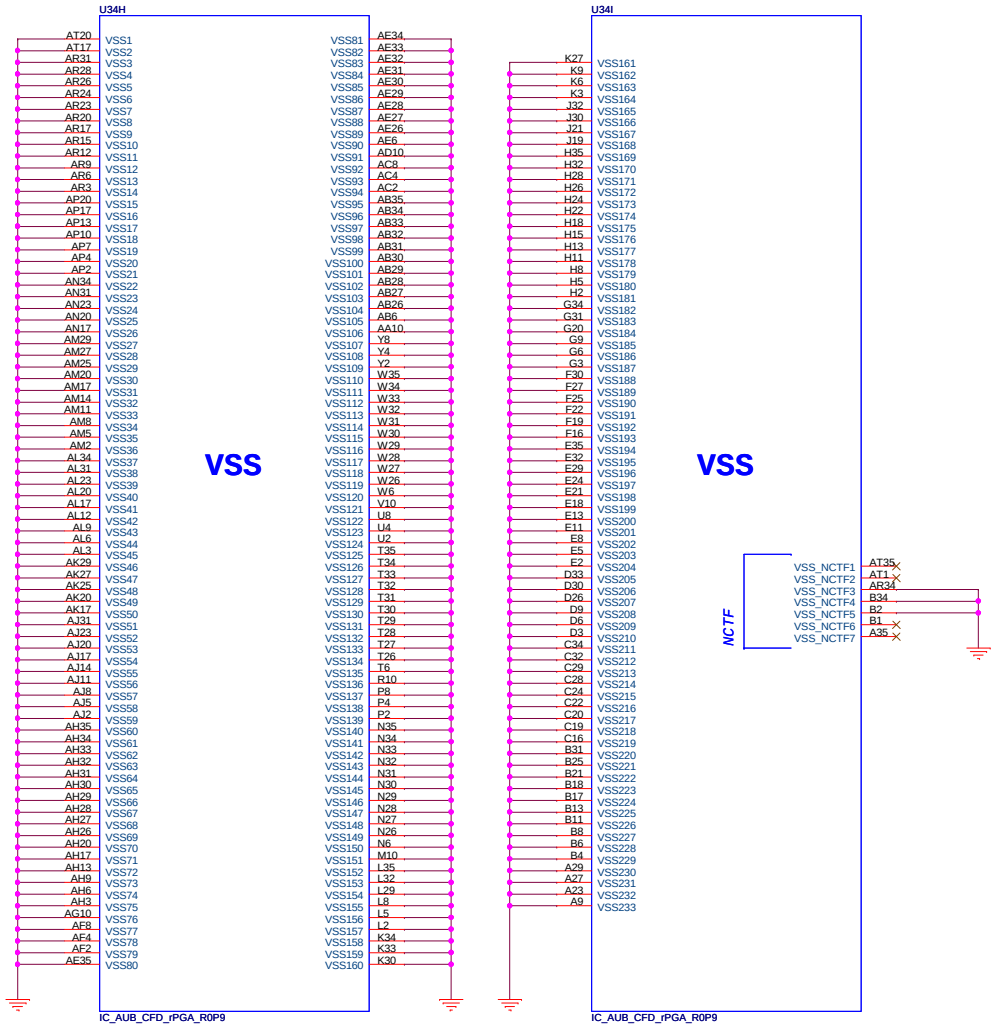
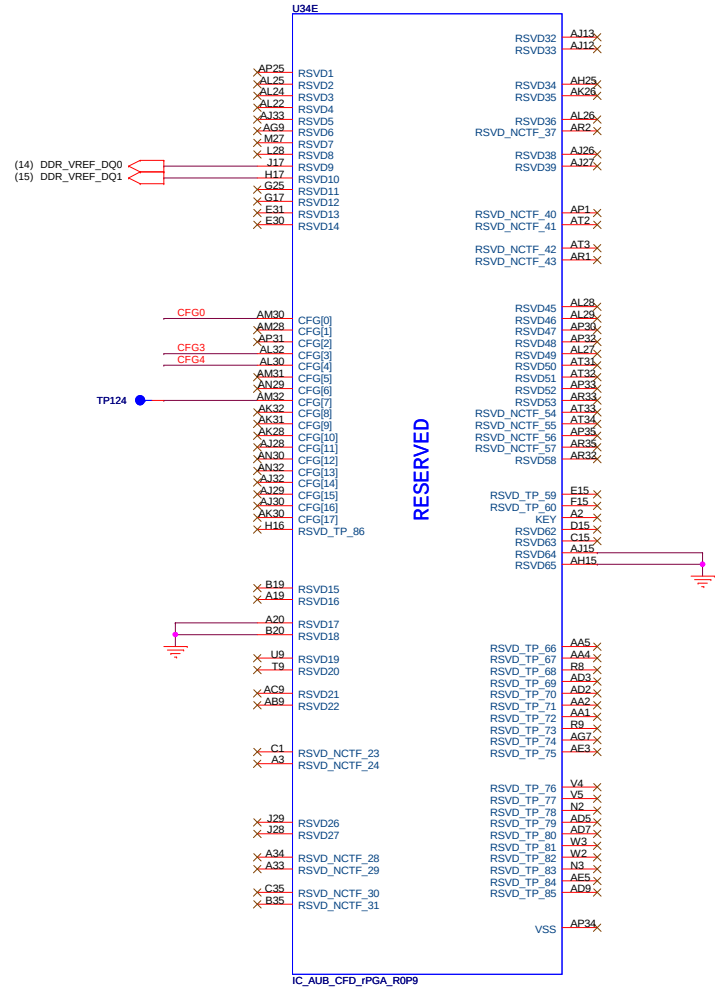
ARRANDALE PROCESSOR (GND)



ARRANDALE PROCESSOR(RESERVED, CFG)



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

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Quanta Computer Inc.

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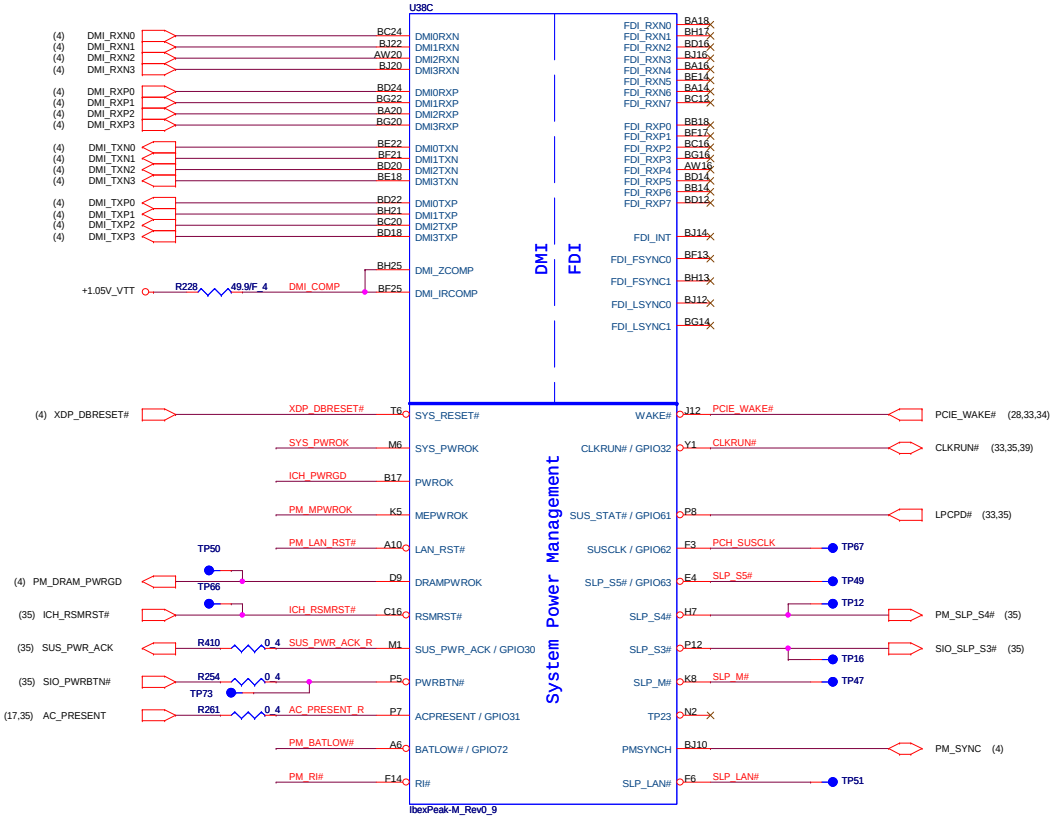
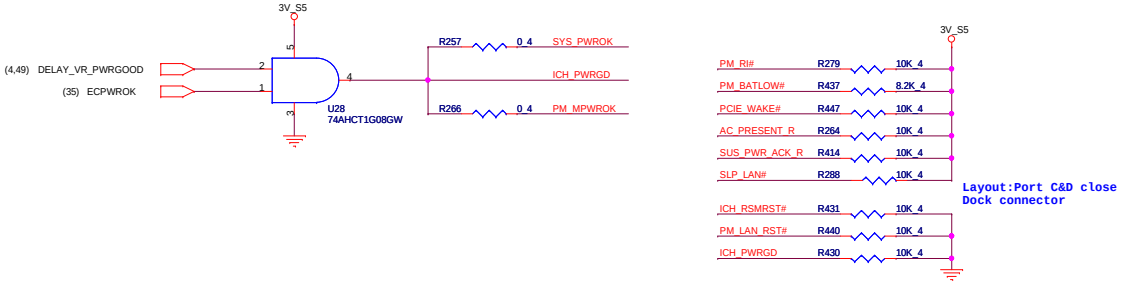
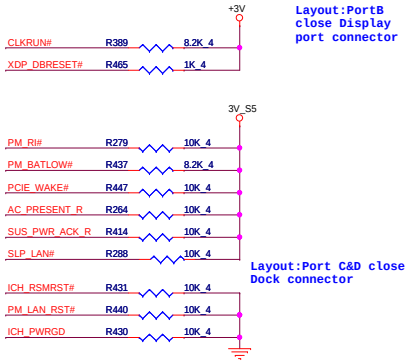
(3,4,6,9,10,11,12,44,47,49) +1.05V_VTT
(4,9,10,11,12,30,33,42,44) 3V_S5
(3,4,9,10,11,12,14,15,17,23,24,25,26,28,29,30,31,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(12,18,21,24,25,26,29,35,37,38,44) +5V

IBEX PEAK-M (DMI,FDI,GPIO)



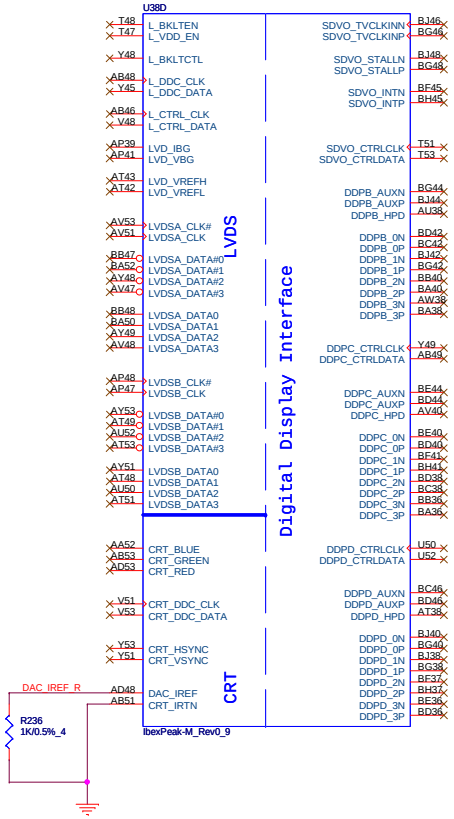




Layout:PortB close Display port connector

Layout:Port C&D close Dock connector

IBEX PEAK-M (LVDS,DDI)



(12,35) +3VRTC
(23,28,31,35,40,41,44,45,48,50) 3VPCU
(3,4,8,10,11,12,14,15,17,23,24,25,26,28,29,30,31,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(4,8,10,11,12,30,33,42,44) 3V_S5
(3,4,6,8,10,11,12,44,47,49) +1.05V_VTT

RTC Circuitry

CMOS Settings	J2
Clear CMOS	1-2
Save CMOS	1-X (Default)

TPM Settings	J3
Clear ME RTC registers	1-2
Save ME RTC registers	1-X (Default)

+3VRTC
3VPCU
D14 RB501V-40
C429 1U/6.3V/X5R_4
+3VRTC_2
D15 RB501V-40
R445 20K/F_4
R446 20K/F_4
C441 1U/6.3V/X5R_4
J3 *SHORT_ PAD1
C440 1U/6.3V/X5R_4
J2 *SHORT_PAD1
R169 1K/F_4
R432 1M/F_4
+3VRTC_1
BT1
RTC BATTERY
C452 15P/50V/NPO_4
C451 15P/50V/NPO_4
Y4 32.768KHZ
R459 10M_4
Cap values depend on Xtal

IBEX PEAK-M (HDA,JTAG,SATA)

U38A

RTC_X1 B13 RTCX1
RTC_X2 D13 RTCX2
RTC_RST# C14 RTCRST#
SRTC_RST# D17 SRTCRST#
SM_INTRUDER# A16 INTRUDER#
+3VRTC R433 330K_4 PCH_INVRMEN A14 INTVRMEN

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

RTC

FWH0 / LAD0 D33 LPC_LAD0 (33,35,39)
FWH1 / LAD1 B33 LPC_LAD1 (33,35,39)
FWH2 / LAD2 C32 LPC_LAD2 (33,35,39)
FWH3 / LAD3 A32 LPC_LAD3 (33,35,39)
FWH4 / LFRAME# C34 LPC_LFRAME# (33,35,39)
LDRQ0# A34 LPC_DRQ#0 LPC_DRQ#0 (33)
LDRQ1# / GPIO23 E34 LCD_BK_OFF LCD_BK_OFF (23)
R275 *10K_4@NC +3V
SERIRQ AB9
R293 10K_4 +3V
IRQ_SERIRQ (33,35,39)

LPC

ACZ_BIT_CLK A30 HDA_BCLK
ACZ_SYNC D29 HDA_SYNC
(26) SPKR P1 SPKR
ACZ_RST# C30 HDA_RST#
(26) ICH_AZ_CODEC_SDIN0 G30 HDA_SDIN0
TP43 F30 HDA_SDIN1
TP46 E32 HDA_SDIN2
TP48 F32 HDA_SDIN3
ACZ_SDOUT B29 HDA_SDO
R272 *1K_4@NC
+3V R291 *1K_4@NC HDA_DOCK_EN# H32 HDA_DOCK_EN# / GPIO33
3V_S5 R259 *10K_4@NC HDA_DOCK_RST# J30 HDA_DOCK_RST# / GPIO13

IHDA

HDA_DOCK_EN# has a weak internal pull-up.
High : the security measures defined in the Flash Descriptor will be in effect (default).
Low : the Flash Descriptor Security will be overridden.

SATA0RXN AK7
SATA0RXP AK6
SATA0TXN AK11 SATA_TXN0_C C270 0.01U/16V/X7R_4 SATA_RX0- (29) SATA_RX0+ (29)
SATA0TXP AK9 SATA_TXP0_C C267 0.01U/16V/X7R_4 SATA_TX0- (29) SATA_TX0+ (29)
SATA HDD
SATA1RXN AH6
SATA1RXP AH5
SATA1TXN AH9 SATA_TXN1_C C271 0.01U/16V/X7R_4 SATA_RX1- (29) SATA_RX1+ (29)
SATA1TXP AH8 SATA_TXP1_C C276 0.01U/16V/X7R_4 SATA_TX1- (29) SATA_TX1+ (29)
SATA ODD
SATA2RXN AF11
SATA2RXP AF9
SATA2TXN AF7
SATA2TXP AF6
SATA3RXN AH3
SATA3RXP AH1
SATA3TXN AF3
SATA3TXP AF1

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

SATA4RXN AD9
SATA4RXP AD8
SATA4TXN AD6 SATA_TXN4_C C296 0.01U/16V/X7R_4 SATA_RX4- (30) SATA_RX4+ (30)
SATA4TXP AD5 SATA_TXP4_C C292 0.01U/16V/X7R_4 SATA_TX4- (30) SATA_TX4+ (30)
E-SATA
SATA5RXN AD3
SATA5RXP AD1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO AF16
SATAICOMPI AF15 SATA_COMP R237 37.4/F_4 +1.05V_VTT
SATALED# T3 R404 10K_4 +3V SATA_LED# (40)
SATA0GP / GPIO21 Y9 SATA0GP R449 10K_4 +3V TP82
SATA1GP / GPIO19 V1 SATA1GP R450 10K_4 +3V TP83

SATA

TP65 PCH_JTAG_TCK M3 JTAG_TCK
TP68 K3 JTAG_TMS
TP54 K1 JTAG_TDI
TP52 J2 JTAG_TDO
TP53 PCH_JTAG_RST# J4 JTAG_RST#

JTAG

(42) SPI_CLK_R BA2 SPI_CLK
(42) SPI_CS0#_R AV3 SPI_CS0#
TP63 SPI_CS1# AY3 SPI_CS1#
(42) SPI_SI_R AY1 SPI_MOSI
(42) SPI_SO AV1 SPI_MISO

SPI

ibexPeak-M_Rev0_9

EC-A-05

(26) ICH_AZ_CODEC_BITCLK R426 33_4 ACZ_BIT_CLK
C427 *10P/50V/COG_4@NC
(26) ICH_AZ_CODEC_SYNC R428 33_4 ACZ_SYNC
(26) ICH_AZ_CODEC_RST# R425 33_4 ACZ_RST#
(26) ICH_AZ_CODEC_SDOUT R427 33_4 ACZ_SDOUT

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R651, R652, R650 & R653 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

No Reboot Strap

+3V
Place near connector
R408 *1K_4@NC SPKR
R268 10K_4 IRQ_SERIRQ

VSUS
PR82 PCH_JTAG_RST# 10K_4
R347 PCH_JTAG_TCK 51_4

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IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

(3,4,8,9,11,12,14,15,17,23,24,25,26,28,29,30,31,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(4,8,9,11,12,30,33,42,44) 3V_S5
(3,4,6,8,9,11,12,44,47,49) +1.05V_VTT
(6,12,17,18,21,22,24,44,51) +1.8V

U38E

PCI: AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31; C/BE0# C/BE1# C/BE2# C/BE3#; PIRQA# PIRQB# PIRQC# PIRQD#; REQ0# REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54; GNT0# GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55; PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5; PCIRST#; SERR# PERR#; IRDY# PAR DEVSEL# FRAME#; PLOCK#; STOP# TRDY#; PME#; PLTRST#; CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4

NVRAM: NV_CE0# NV_CE1# NV_CE2# NV_CE3#; NV_DQS0 NV_DQS1; NV_DQ0 / NV_IO0 … NV_DQ15 / NV_IO15; NV_ALE NV_CLE; NV_RCOMP; NV_RB#; NV_WR#0_RE# NV_WR#1_RE#; NV_WE#_CK0 NV_WE#_CK1

USB: USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBRBIAS# USBRBIAS; OC0# / GPIO59 OC1# / GPIO40 OC2# / GPIO41 OC3# / GPIO42 OC4# / GPIO43 OC5# / GPIO9 OC6# / GPIO10 OC7# / GPIO14

ICH_USBP0- (30) ICH_USBP0+ (30) — USB0
ICH_USBP1- (30) ICH_USBP1+ (30) — USB1
ICH_USBP2- (34) ICH_USBP2+ (34) — Express Card
ICH_USBP3- (23) ICH_USBP3+ (23) — Camera
ICH_USBP4- (33) ICH_USBP4+ (33) — Mini Card (WLAN)
ICH_USBP5- (32) ICH_USBP5+ (32) — Mini Card (WWAN)
ICH_USBP8- (31) ICH_USBP8+ (31) — USB3
ICH_USBP9- (31) ICH_USBP9+ (31) — USB2
ICH_USBP10- (31) ICH_USBP10+ (31) — FINGER PRINTER
ICH_USBP11- (41) ICH_USBP11+ (41) — Dock Usb
ICH_USBP13- (36) ICH_USBP13+ (36) — BLUETOOTH

R231 *32.4/F_4

USB_BIAS R429 22.6/F_4

USB_OC0_1# (30) USB_OC8_9# (31) DRAMRST_CTRL_PCH (4)

IbexPeak-M_Rev0_9

U38B

Card Reader: (31) PCIE_RX1- (31) PCIE_RX1+ (31) PCIE_TX1- (31) PCIE_TX1+ — C465 0.1U/10V/X5R_4 PCIE_TXN1_C; C461 0.1U/10V/X5R_4 PCIE_TXP1_C

MiniWLAN: (33) PCIE_RX2- (33) PCIE_RX2+ (33) PCIE_TX2- (33) PCIE_TX2+ — C262 0.1U/10V/X5R_4 PCIE_TXN2_C; C261 0.1U/10V/X5R_4 PCIE_TXP2_C

LAN: (28) PCIE_RX3-/GLAN_RX- (28) PCIE_RX3+/GLAN_RX+ (28) PCIE_TX3-/GLAN_TX- (28) PCIE_TX3+/GLAN_TX+ — C398 0.1U/10V/X5R_4 PCIE_TXN3_C; C399 0.1U/10V/X5R_4 PCIE_TXP3_C

Express Card: (34) PCIE_RX4- (34) PCIE_RX4+ (34) PCIE_TX4- (34) PCIE_TX4+ — C255 0.1U/10V/X5R_4 PCIE_TXN4_C; C256 0.1U/10V/X5R_4 PCIE_TXP4_C

MiniWWAN: (32) PCIE_RX5- (32) PCIE_RX5+ (32) PCIE_TX5- (32) PCIE_TX5+ — C397 0.1U/10V/X5R_4 PCIE_TXN5_C; C396 0.1U/10V/X5R_4 PCIE_TXP5_C

PCI-E*: PERN1 PERP1 PETN1 PETP1; PERN2 PERP2 PETN2 PETP2; PERN3 PERP3 PETN3 PETP3; PERN4 PERP4 PETN4 PETP4; PERN5 PERP5 PETN5 PETP5; PERN6 PERP6 PETN6 PETP6; PERN7 PERP7 PETN7 PETP7; PERN8 PERP8 PETN8 PETP8

SMBus: SMBALERT# / GPIO11; SMBCLK; SMBDATA; SMLOALERT# / GPIO60; SMLOCLK; SMLODATA; SMLIALERT# / GPIO74; SMLICLK / GPIO58; SMLIDATA / GPIO75

Controller Link: CL_CLK1 TP33; CL_DATA1 TP38; CL_RST1# TP32

PEG: PEG_A_CLKRQ# / GPIO47; CLKOUT_PEG_A_N CLKOUT_PEG_A_P; CLKOUT_DMI_N CLKOUT_DMI_P; CLKOUT_DP_N / CLKOUT_BCLK1_N; CLKOUT_DP_P / CLKOUT_BCLK1_P

From CLK BUFFER: CLKOUT_PCIE0N CLKOUT_PCIE0P; PCIECLKRQ9# / GPIO73; CLKOUT_PCIE1N CLKOUT_PCIE1P; PCIECLKRQ1# / GPIO18; CLKOUT_PCIE2N CLKOUT_PCIE2P; PCIECLKRQ2# / GPIO20; CLKOUT_PCIE3N CLKOUT_PCIE3P; PCIECLKRQ3# / GPIO25; CLKOUT_PCIE4N CLKOUT_PCIE4P; PCIECLKRQ4# / GPIO26; CLKOUT_PCIE5N CLKOUT_PCIE5P; PCIECLKRQ5# / GPIO44; CLKOUT_PEG_B_N CLKOUT_PEG_B_P; PEG_B_CLKRQ# / GPIO56

Clock Flex: CLKOUTFLEX0 / GPIO64; CLKOUTFLEX1 / GPIO65; CLKOUTFLEX2 / GPIO66; CLKOUTFLEX3 / GPIO67

CLK_PCIE_REQ0# P9; CLK_PCIE_REQ1# R397 0_4 U4; MINI1CLK_REQ# R411 0_4 N4; CLK_PCIE_REQ3# R419 0_4 A8; CARD_CLK_REQ# R265 0_4 M9; CLK_PCIE_REQ5# R289 0_4 H8; CLK_PCIE_LAN_REQ# R277 0_4 P13

TP113 TP114 TP115 TP116

MiniWLAN: (33) CLK_PCH_SRC2_N (33) CLK_PCH_SRC2_P (33) MINI1CLK_REQ#

Card Reader: (31) CLK_PCIE_CARD# (31) CLK_PCIE_CARD

Express Card: (34) CLK_PCH_SRC4_N (34) CLK_PCH_SRC4_P (34) CARD_CLK_REQ#

MiniWWAN: (32) CLK_PCH_SRC5_N (32) CLK_PCH_SRC5_P (32) CLK_PCIE_REQ5#

LAN: (28) CLK_PCIE_LOM# (28) CLK_PCIE_LOM (28) CLK_PCIE_LAN_REQ#

SMBALERT# / GPIO11 B9 → SMBALERT#
SMBCLK H14 → ICH_SMBCLK (3)
SMBDATA C8 → ICH_SMBDATA (3)
SMLOALERT# / GPIO60 J14 → SMLOALERT#
SMLOCLK C6 → SMB_CLK_ME0
SMLODATA G8 → SMB_DATA_ME0
SMLIALERT# / GPIO74 M14 → SMLIALERT#
SMLICLK / GPIO58 E10 → SMB_CLK_ME1
SMLIDATA / GPIO75 G12 → SMB_DATA_ME1
CL_CLK1 T13 → CL_CLK1 TP33
CL_DATA1 T11 → CL_DATA1 TP38
CL_RST1# T9 → CL_RST1# TP32
PEG_A_CLKRQ# / GPIO47 H1 → PEGA_CLKREQ#
CLKOUT_PEG_A_N AD43 / CLKOUT_PEG_A_P AD45 → CLK_PCIE_VGA# (16) / CLK_PCIE_VGA (16)
CLKOUT_DMI_N AN4 / CLKOUT_DMI_P AN2 → CLK_PCIE_3GPLL# (4) / CLK_PCIE_3GPLL (4)
CLKOUT_DP_N / CLKOUT_BCLK1_N AT1; CLKOUT_DP_P / CLKOUT_BCLK1_P AT3
CLKIN_DMI_N AW24 / CLKIN_DMI_P BA24 → CLK_BUF_PCIE_3GPLL# (3) / CLK_BUF_PCIE_3GPLL (3)
CLKIN_BCLK_N AP3 / CLKIN_BCLK_P AP1 → CLK_BUF_BCLK_N (3) / CLK_BUF_BCLK_P (3)
CLKIN_DOT_96N F18 / CLKIN_DOT_96P E18 → CLK_BUF_DREFCLK# (3) / CLK_BUF_DREFCLK (3)
CLKIN_SATA_N / CKSSCD_N AH13 / CLKIN_SATA_P / CKSSCD_P AH12 → CLK_BUF_DREFSSCLK# (3) / CLK_BUF_DREFSSCLK (3)
REFCLK14IN P41 → CLK_ICH_14M (3)
CLKIN_PCILOOPBACK J42 → CLK_PCI_FB
XTAL25_IN AH51 / XTAL25_OUT AH53 → XTAL25_IN / XTAL25_OUT
XCLK_RCOMP AF38 → XCLK_RCOMP R235 90.9/F_4 +1.05V_VTT
CLKOUTFLEX0 / GPIO64 T45 → CLK_FLEX0 TP36
CLKOUTFLEX1 / GPIO65 P43 → CLK_FLEX1 TP40
CLKOUTFLEX2 / GPIO66 T42 → CLK_FLEX2 TP37
CLKOUTFLEX3 / GPIO67 N50 → CLK_FLEX3 TP35

IbexPeak-M_Rev0_9

(35) SIO_EXT_WAKE# M7
TP74 D5
(33) CLK_LPC_DEBUG R409 22_4 CLK_LPC_DEBUG_C N52
(39) CLK_LPC_TPM R443 22_4 CLK_LPC_TPM_C P53
(35) CLK_PCI_8512 R263 22_4 CLK_PCI_8512_C P46
CLK_PCI_FB R258 22_4 CLK_PCI_FB_C P51
CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4 P48

(36) BT_DET# M53
TP41 PCI_GNT#0 F48
TP39 PCI_GNT#1 K45
TP42 PCI_GNT#2 F36
GNT3# H53
(41) DOCK_ID0 PCI_PIRQE# B41
(41) DOCK_ID1 PCI_PIRQF# K53
(41) DOCK_ID2 PCI_PIRQG# A36
PCI_PIRQH# A48
PCI_RST_R# K6
PCI_SERR# E44
PCI_PERR# E50
PCI_IRDY# A42
PCI_DEVSEL# H44
PCI_FRAME# F46
PCI_PLOCK# C46
PCI_STOP# D49
PCI_TRDY# D41
C48

PCI_PIRQA# PCI_PIRQB# PCI_PIRQC# PCI_PIRQD# A44
PCI_REQ0# F51
PCI_REQ1# A46
PCI_REQ2# B45
BT_DET# M53

C424 *10P/50V/COG_4@NC CLK_LPC_DEBUG
C325 *10P/50V/COG_4@NC CLK_PCI_8512
FOR EMI

C495 0.047U/10V/X7R_4@NC *TC7SZ32FU U36 PCI_RST_R# → PCI_RST# (16) R373 0_4

Non-iAMT
Add Buffers as needed for Loading and fanout concerns.

C336 0.047U/10V/X7R_4 U29 TC7SZ32FU PCI_PLTRST# → PLTRST# (4,28,31,32,33,34,39,42)

SMBALERT# R434 10K_4; SMLOALERT# R448 10K_4; ICH_SMBCLK R451 2.2K_4; ICH_SMBDATA R435 2.2K_4; SMB_CLK_ME0 R436 2.2K_4; SMB_DATA_ME0 R286 2.2K_4; SMB_CLK_ME1 R282 2.2K_4; SMB_DATA_ME1 R283 2.2K_4; SMLIALERT# R281 10K_4

RP7 10P8R-8.2K: USB_OC8# USB_OC7# USB_OC4# USB_OC5# → USB_OC0# USB_OC1# USB_OC2# USB_OC3#

RP4 10P8R-8.2K: BT_DET# PCI_PIRQB# PCI_PLOCK# PCI_PERR# → PCI_PIRQC# PCI_PIRQA# PCI_SERR# PCI_DEVSEL#

RP10 10P8R-8.2K: PCI_IRDY# PCI_PIRQD# PCI_REQ2# PCI_REQ1# → PCI_STOP# PCI_REQ0# PCI_TRDY# PCI_FRAME#

R421 R415 R424 R420 8.2K_4: PCI_PIRQE# PCI_PIRQF# PCI_PIRQG# PCI_PIRQH#
R413 10K_4 MINI1CLK_REQ#
R401 10K_4 CLK_PCIE_REQ1#

R287 R267 R290 R278 R439 10K_4: CLK_PCIE_REQ0# CARD_CLK_REQ# CLK_PCIE_REQ5# CLK_PCIE_LAN_REQ# CLK_PCIE_REQ3#
R417 10K_4 PEGA_CLKREQ#

R260 *1K_4@NC PCI_GNT#0
R256 *1K_4@NC PCI_GNT#1

Boot BIOS Strap

PCI_GNT0#	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

XTAL25_IN C493 *18P/50V/COG_4; R379 *1M/F_4; Y6 *25MHZ; XTAL25_OUT C492 *18P/50V/COG_4

No stuff XTAL25_IN and XTAL25_OUT circuitry until integrated CG becomes PCH POR.

DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

+1.8V
NV_ALE R390 *1K_4@NC
NV_CLE R386 *1K_4@NC

Danbury Technology Enabled

NV_ALE	High = Enable Low = Disable

GNT3# R416 *1K_4@NC

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SMB_CLK_ME1 → Q18 2N7002 → MB_CLK (19,35)
SMB_DATA_ME1 → Q17 2N7002 → MB_DATA (19,35)

PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	IBEX PEAK-M 3/6	1A

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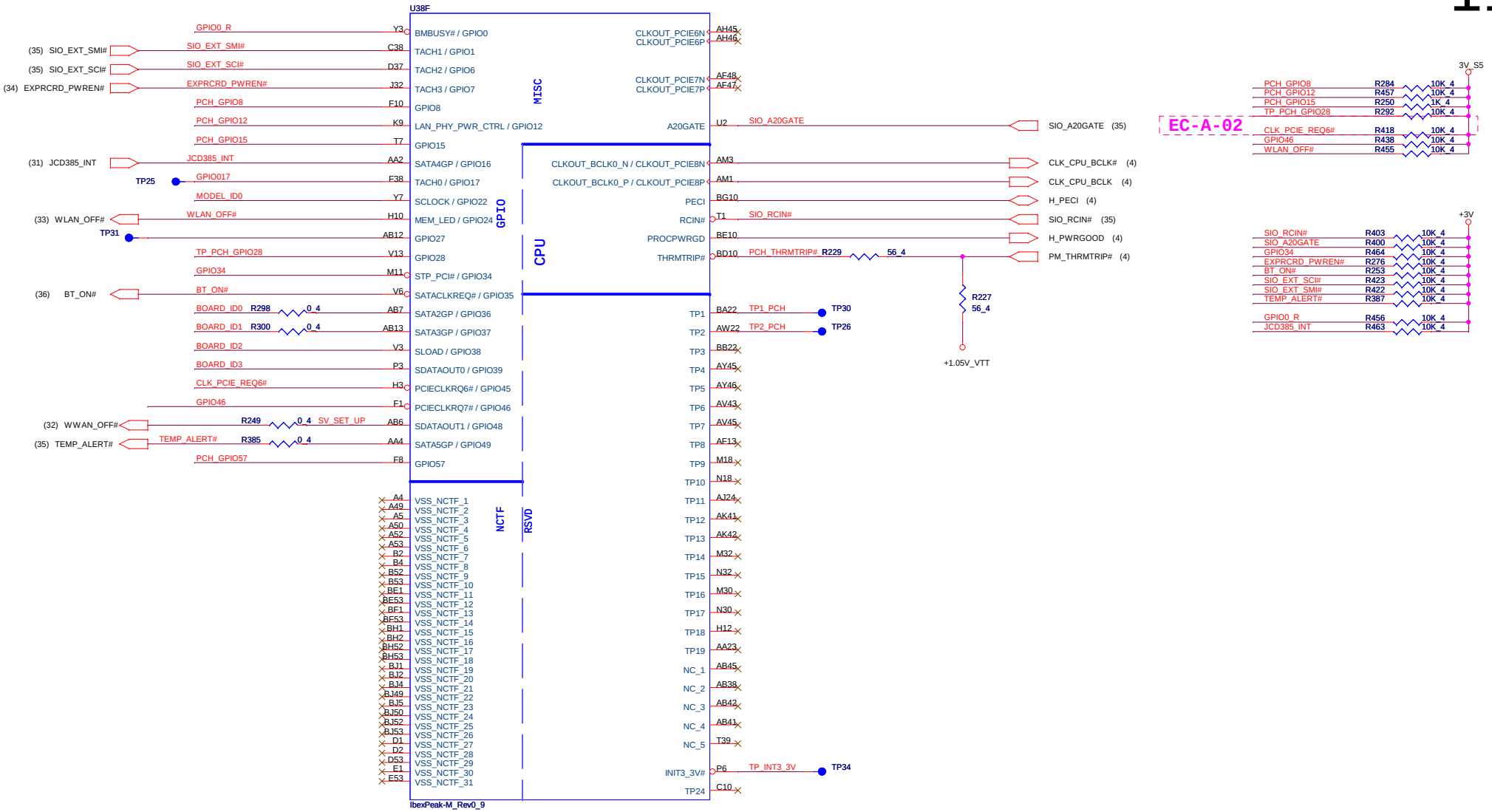
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

(3,4,8,9,10,12,14,15,17,23,24,25,26,28,29,30,31,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(4,8,9,10,12,30,33,42,44) 3V_S5
(3,4,6,8,9,10,12,44,47,49) +1.05V_VTT



EC-A-02

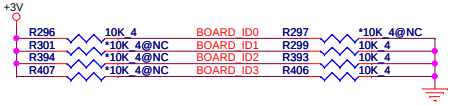
3V_S5

PCH_GPIO8	R284	10K_4
PCH_GPIO12	R457	10K_4
PCH_GPIO15	R250	1K_4
TP_PCH_GPIO28	R292	10K_4
CLK_PCIE_REQ6#	R418	10K_4
GPIO46	R438	10K_4
WLAN_OFF#	R455	10K_4

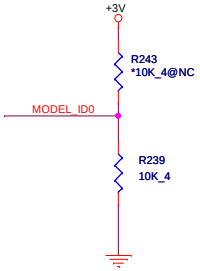
+3V

SIO_RCIN#	R403	10K_4
SIO_A20GATE	R400	10K_4
GPIO34	R464	10K_4
EXPRCRD_PWREN#	R276	10K_4
BT_ON#	R253	10K_4
SIO_EXT_SCI#	R423	10K_4
SIO_EXT_SMI#	R422	10K_4
TEMP_ALERT#	R387	10K_4
GPIO0_R	R456	10K_4
JCD385_INT	R463	10K_4

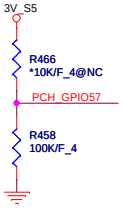
Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO36
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	0	1	1
SOVP	0	1	0	0



Model ID	MODEL_ID0
14"	0
15"	1



TPM physical presence	
PCH_GPIO57	Low: Default



SV_SET_UP	1-X High = Strong (Default)

PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	IBEX PEAK-M 4/6	1A

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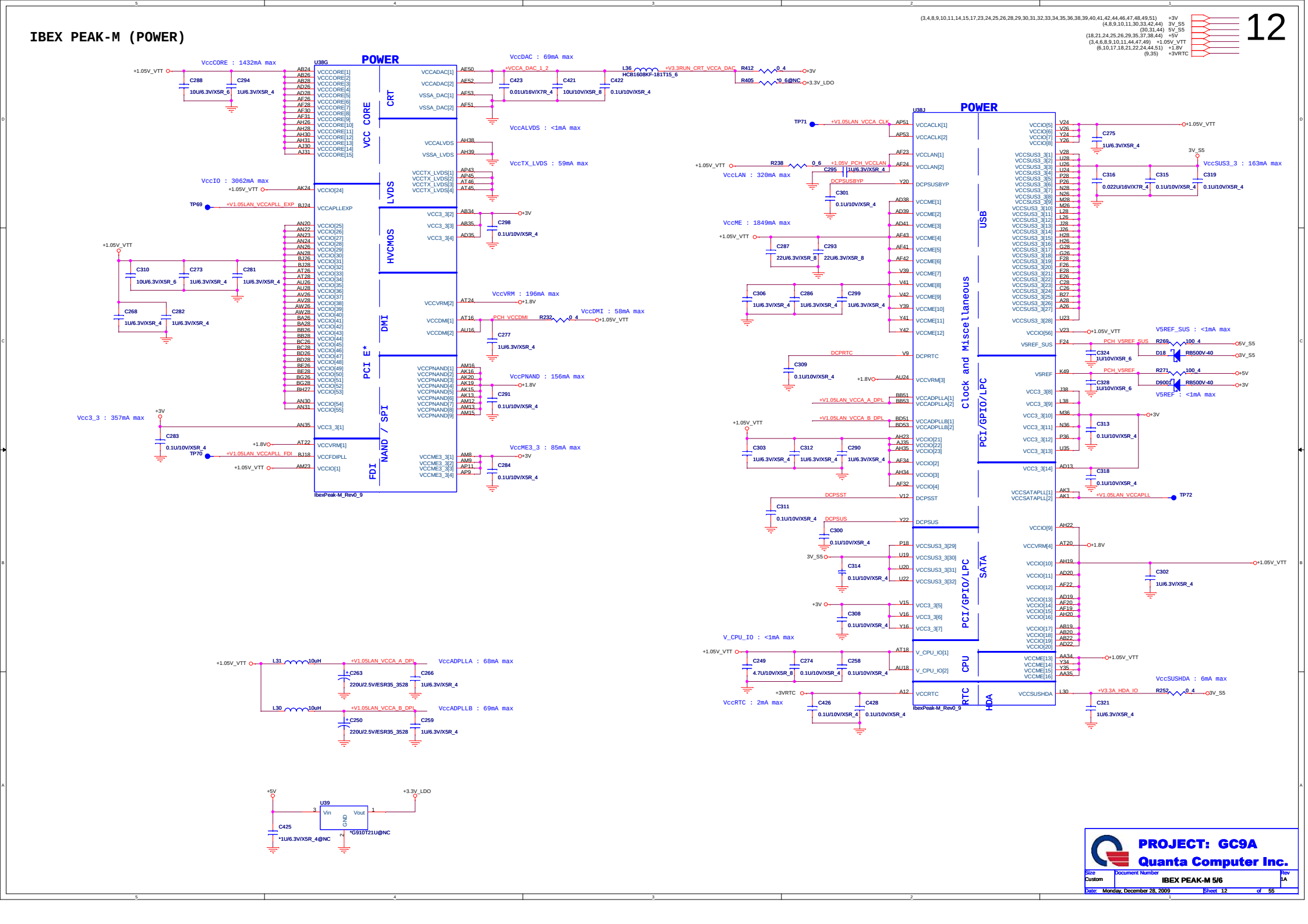
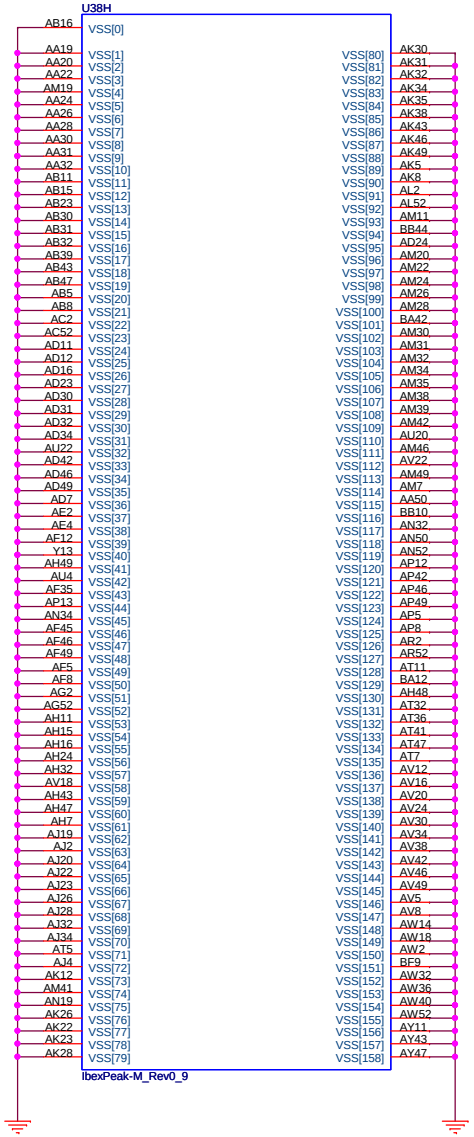
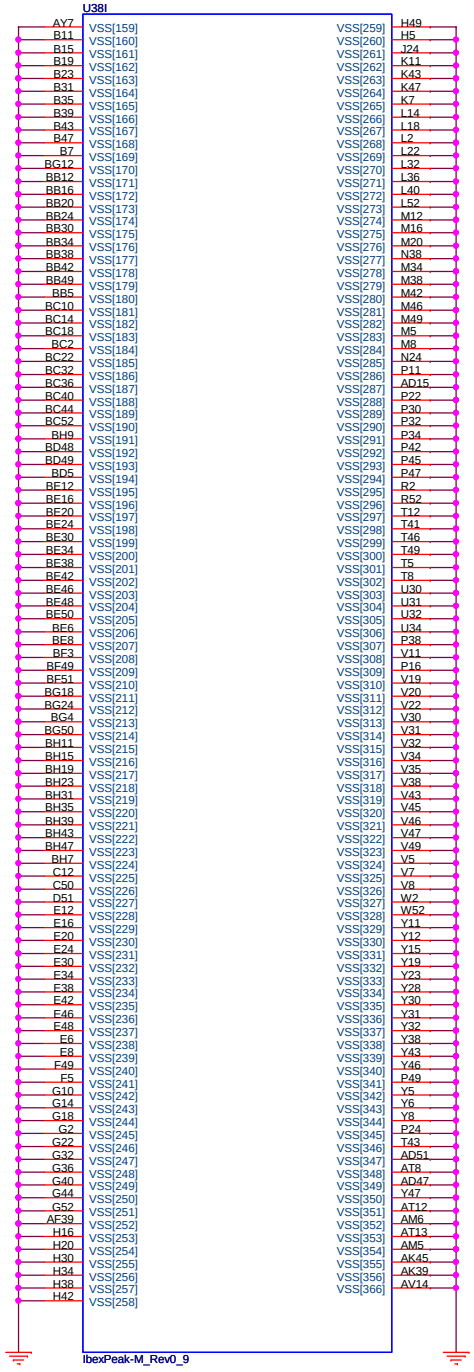
IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)





PROJECT: GC9A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	IBEX PEAK-M 6/6	1A

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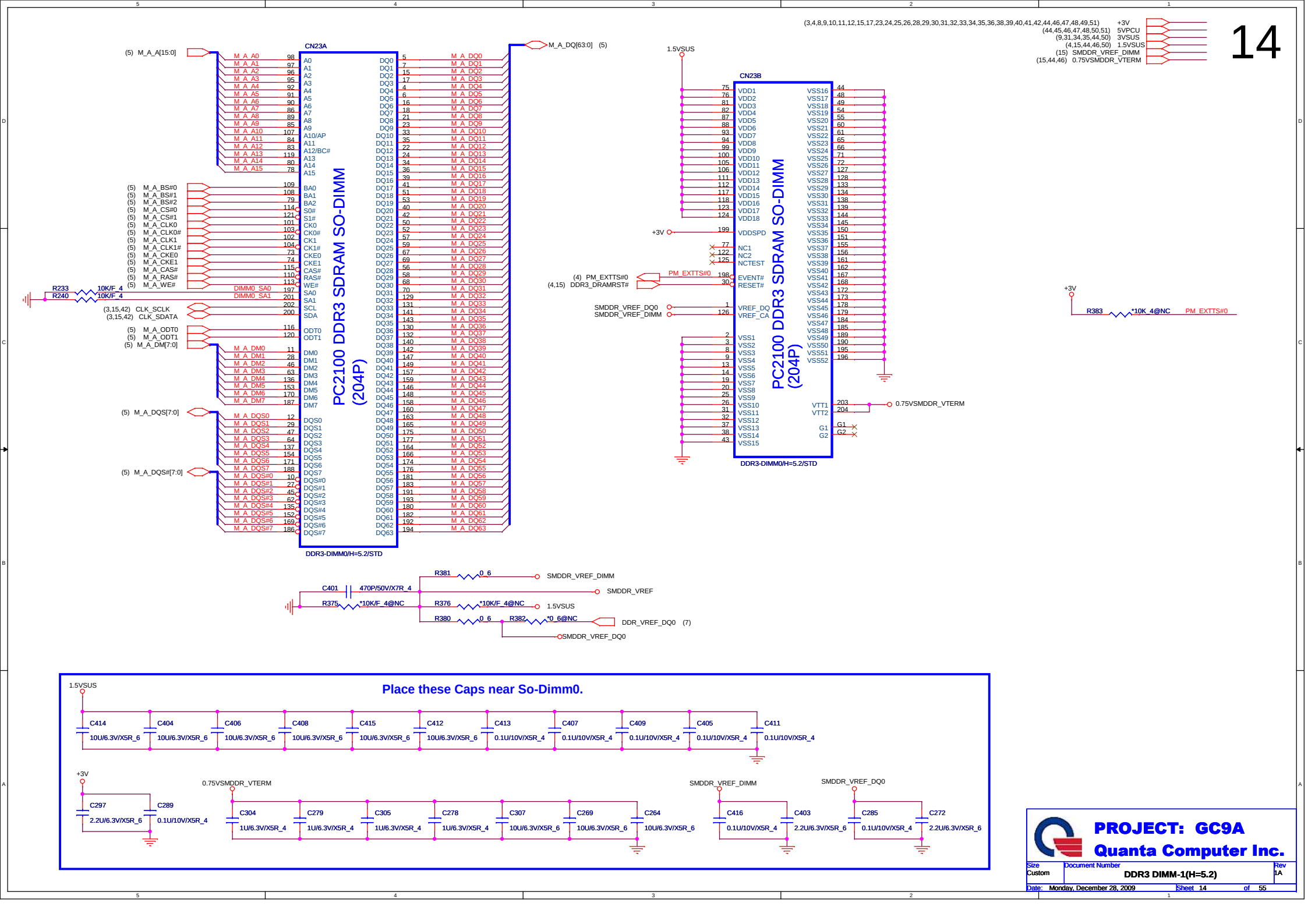

PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1(H=5.2)	1A

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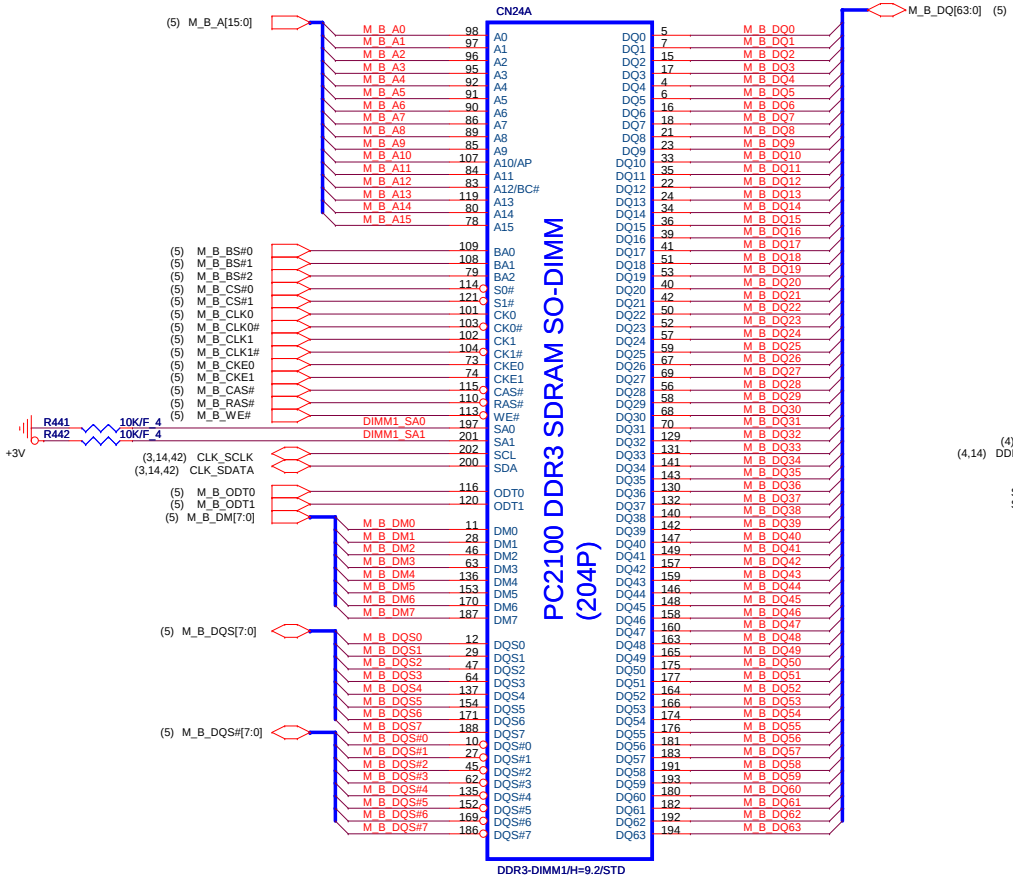
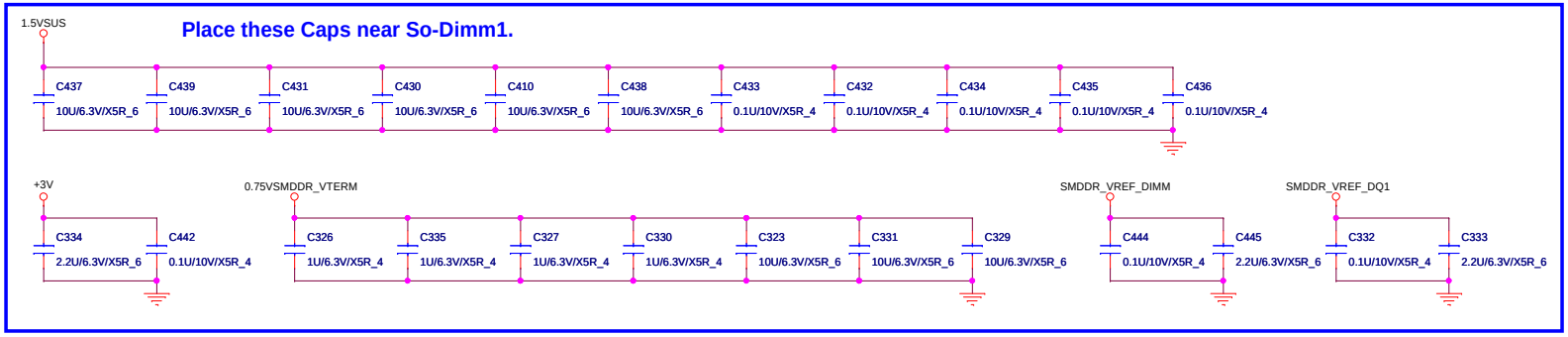
(3,4,8,9,10,11,12,14,17,23,24,25,26,28,29,30,31,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(9,31,34,35,44,50) 3VSUS
(4,14,44,46,50) 1.5VSUS
(14) SMDDR_VREF_DIMM
(14,44,46) 0.75VSMDDR_VTERM



Place these Caps near So-Dimm1.



PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1(H=9.2)	1A
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(4) PEG_TXP[0..15]
(4) PEG_TXN[0..15]

U9003A
PART 1 OF 10

PCI-EXPRESS INTERFACE

PEG_TXP0	AF30	PCIE_RX0P	PCIE_TX0P	AH30	PEG_C_RXP0
PEG_TXN0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PEG_C_RXN0
PEG_TXP1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	PEG_C_RXP1
PEG_TXN1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PEG_C_RXN1
PEG_TXP2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PEG_C_RXP2
PEG_TXN2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PEG_C_RXN2
PEG_TXP3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PEG_C_RXP3
PEG_TXN3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PEG_C_RXN3
PEG_TXP4	AB30	PCIE_RX4P	PCIE_TX4P	AC25	PEG_C_RXP4
PEG_TXN4	AA31	PCIE_RX4N	PCIE_TX4N	AB25	PEG_C_RXN4
PEG_TXP5	AA29	PCIE_RX5P	PCIE_TX5P	Y23	PEG_C_RXP5
PEG_TXN5	Y28	PCIE_RX5N	PCIE_TX5N	Y24	PEG_C_RXN5
PEG_TXP6	Y30	PCIE_RX6P	PCIE_TX6P	AB27	PEG_C_RXP6
PEG_TXN6	W31	PCIE_RX6N	PCIE_TX6N	AB26	PEG_C_RXN6
PEG_TXP7	W29	PCIE_RX7P	PCIE_TX7P	Y27	PEG_C_RXP7
PEG_TXN7	V28	PCIE_RX7N	PCIE_TX7N	Y26	PEG_C_RXN7
PEG_TXP8	V30	PCIE_RX8P	PCIE_TX8P	W24	PEG_C_RXP8
PEG_TXN8	U31	PCIE_RX8N	PCIE_TX8N	W23	PEG_C_RXN8
PEG_TXP9	U29	PCIE_RX9P	PCIE_TX9P	V27	PEG_C_RXP9
PEG_TXN9	T28	PCIE_RX9N	PCIE_TX9N	U26	PEG_C_RXN9
PEG_TXP10	T30	PCIE_RX10P	PCIE_TX10P	U24	PEG_C_RXP10
PEG_TXN10	R31	PCIE_RX10N	PCIE_TX10N	U23	PEG_C_RXN10
PEG_TXP11	R29	PCIE_RX11P	PCIE_TX11P	T26	PEG_C_RXP11
PEG_TXN11	P28	PCIE_RX11N	PCIE_TX11N	T27	PEG_C_RXN11
PEG_TXP12	P30	PCIE_RX12P	PCIE_TX12P	T24	PEG_C_RXP12
PEG_TXN12	N31	PCIE_RX12N	PCIE_TX12N	T23	PEG_C_RXN12
PEG_TXP13	N29	PCIE_RX13P	PCIE_TX13P	P27	PEG_C_RXP13
PEG_TXN13	M28	PCIE_RX13N	PCIE_TX13N	P26	PEG_C_RXN13
PEG_TXP14	M30	PCIE_RX14P	PCIE_TX14P	P24	PEG_C_RXP14
PEG_TXN14	L31	PCIE_RX14N	PCIE_TX14N	P23	PEG_C_RXN14
PEG_TXP15	L29	PCIE_RX15P	PCIE_TX15P	M27	PEG_C_RXP15
PEG_TXN15	K30	PCIE_RX15N	PCIE_TX15N	N26	PEG_C_RXN15

(10) CLK_PCIE_VGA
(10) CLK_PCIE_VGA#

AK30 PCIE_REFCLKP
AK32 PCIE_REFCLKN

(10) PCI_RST#

AL27 PERSTB

PCIE_CALRN AA22 PCIE_CALRN 2K/F_4 R9020
PCIE_CALRP Y22 PCIE_CALRP 1.27K/F_4 R9018

(1.1V)
+1.1V_GFX_PCIE

M92-S2/M92-XT

100 MHz (+/-300 ppm) input frequency,
0-0.7 V single-ended swing.
clock must be provided less than 400ns
after CLKREQ# is asserted

(18,21,22,44,50) +1.1V_GFX_PCIE

PEG_RXP[0..15] (4)
PEG_RXN[0..15] (4)

PEG_C_RXP0	0.1U/10V/X5R_4	C9014	PEG_RXP0
PEG_C_RXP1	0.1U/10V/X5R_4	C9024	PEG_RXP1
PEG_C_RXP2	0.1U/10V/X5R_4	C9031	PEG_RXP2
PEG_C_RXP3	0.1U/10V/X5R_4	C9044	PEG_RXP3
PEG_C_RXP4	0.1U/10V/X5R_4	C9049	PEG_RXP4
PEG_C_RXP5	0.1U/10V/X5R_4	C9060	PEG_RXP5
PEG_C_RXP6	0.1U/10V/X5R_4	C9055	PEG_RXP6
PEG_C_RXP7	0.1U/10V/X5R_4	C9073	PEG_RXP7
PEG_C_RXP8	0.1U/10V/X5R_4	C9072	PEG_RXP8
PEG_C_RXP9	0.1U/10V/X5R_4	C9089	PEG_RXP9
PEG_C_RXP10	0.1U/10V/X5R_4	C9086	PEG_RXP10
PEG_C_RXP11	0.1U/10V/X5R_4	C9108	PEG_RXP11
PEG_C_RXP12	0.1U/10V/X5R_4	C9098	PEG_RXP12
PEG_C_RXP13	0.1U/10V/X5R_4	C9112	PEG_RXP13
PEG_C_RXP14	0.1U/10V/X5R_4	C9124	PEG_RXP14
PEG_C_RXP15	0.1U/10V/X5R_4	C9122	PEG_RXP15

PEG_C_RXN0	0.1U/10V/X5R_4	C9015	PEG_RXN0
PEG_C_RXN1	0.1U/10V/X5R_4	C9027	PEG_RXN1
PEG_C_RXN2	0.1U/10V/X5R_4	C9037	PEG_RXN2
PEG_C_RXN3	0.1U/10V/X5R_4	C9038	PEG_RXN3
PEG_C_RXN4	0.1U/10V/X5R_4	C9053	PEG_RXN4
PEG_C_RXN5	0.1U/10V/X5R_4	C9068	PEG_RXN5
PEG_C_RXN6	0.1U/10V/X5R_4	C9059	PEG_RXN6
PEG_C_RXN7	0.1U/10V/X5R_4	C9080	PEG_RXN7
PEG_C_RXN8	0.1U/10V/X5R_4	C9063	PEG_RXN8
PEG_C_RXN9	0.1U/10V/X5R_4	C9092	PEG_RXN9
PEG_C_RXN10	0.1U/10V/X5R_4	C9081	PEG_RXN10
PEG_C_RXN11	0.1U/10V/X5R_4	C9100	PEG_RXN11
PEG_C_RXN12	0.1U/10V/X5R_4	C9093	PEG_RXN12
PEG_C_RXN13	0.1U/10V/X5R_4	C9109	PEG_RXN13
PEG_C_RXN14	0.1U/10V/X5R_4	C9127	PEG_RXN14
PEG_C_RXN15	0.1U/10V/X5R_4	C9114	PEG_RXN15

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MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0
512MB	1	0	0

Memory Straps	RAM_TYPE _CFG3	RAM_TYPE _CFG2	RAM_TYPE _CFG1	RAM_TYPE _CFG0
800MHz 512MB(64M*16) Samsung K4W1G1646E-HC12	0	0	0	1
800MHz 512MB(64M*16) Hynix H5TQ1G63BFR-12C	0	0	1	0

GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	G NOTE Setting
GPIO0	GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable) 0 : Default. (Driver Controlled Gen2) 1 : Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO_5_AC_BATT 0 : Battery saving mode = 0.0 V 1 : AC (Performance mode) = 3.3 V	1
GPIO6	ATI Internal use only	0
GPIO8	ATI reserved configuration straps.	0
GPIO9	VGA Disable 0 - VGA Controller capacity enabled 1 - The device will not recognized as the system's VGA controller	0
GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
HSYNC VSYNC	AUD[1:0] 00 - No audio function 01 - Audio for DisplayPort and HDMI if adapter is detectd 10 - Audio for DisplayPort only 11 - Audio for both DisplayPort and HDMI	1 1

	SS DISABLE	SS ENABLE
R3079	DE-POP	POP
R3080	POP	DE-POP

Layout Note:
Place 150 ohm termination resistors close to ATI CHIP.

A2VSSQ connect to GND by a via directly

A2VSSQ connect to GND by a via directly

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(16,21,22,44,50) +1.1V_GFX_PCIE
(3,19,20,32,33,34,46) +1.5V
(6,10,12,17,21,22,24,44,51) +1.8V
(17,19,21) +3.3V_DELAY
(21,44,50) +VCC_GFX_CORE
(12,21,24,25,26,29,35,37,38,44) +5V

layout note: close to VDDR1#[1:17]

+1.5V
C9128 1U/6.3V/X5R_4
C9131 1U/6.3V/X5R_4
C9129 1U/6.3V/X5R_4
C9121 1U/6.3V/X5R_4
C9126 0.1U/10V/X5R_4
C9120 0.1U/10V/X5R_4
C9118 0.1U/10V/X5R_4
C9117 0.1U/10V/X5R_4
C9102 0.1U/10V/X5R_4
C9125 1U/6.3V/X5R_4
C9143 1U/6.3V/X5R_4
C9134 1U/6.3V/X5R_4
C9133 1U/6.3V/X5R_4
C9130 1U/6.3V/X5R_4
C9119 1U/6.3V/X5R_4

+1.5V
C9191 10U/6.3V/X5R_6
C9209 10U/6.3V/X5R_6
C9185 10U/6.3V/X5R_6
C9211 10U/6.3V/X5R_6
C9140 10U/6.3V/X5R_6

VDDR1+VDDRHA
0.93 A (RMS) / 1.2 A (peak)

U9003D
PART 4 OF 10
POWER

+1.5V
H13 VDDR1#1
H16 VDDR1#2
H19 VDDR1#3
J10 VDDR1#4
J23 VDDR1#5
J24 VDDR1#6
J9 VDDR1#7
K10 VDDR1#8
K23 VDDR1#9
K24 VDDR1#10
K9 VDDR1#11
L11 VDDR1#12
L12 VDDR1#13
L13 VDDR1#14
L20 VDDR1#15
L21 VDDR1#16
L22 VDDR1#17

110mA
+1.8V
L9004 BLM15BD121SN1D
+VDD_CT
C9006 10U/6.3V/X5R_6
C9067 0.1U/10V/X5R_4
C9066 1U/6.3V/X5R_4
C9065 1U/6.3V/X5R_4
C9013 0.1U/10V/X5R_4
AA20 VDD_CT#1
AA21 VDD_CT#2
AB20 VDD_CT#3
AB21 VDD_CT#4

+3.3V_DELAY
50mA
C9062 1U/6.3V/X5R_4
C9056 1U/6.3V/X5R_4
C9058 0.1U/10V/X5R_4
C9064 0.1U/10V/X5R_4
AA17 VDDR3#1
AA18 VDDR3#2
AB17 VDDR3#3
AB18 VDDR3#4

170mA
+1.8V
C9057 1U/6.3V/X5R_4
C9051 0.1U/10V/X5R_4
C9061 1U/6.3V/X5R_4
C9069 0.1U/10V/X5R_4
AA11 VDDR4#1
AA12 VDDR4#2
Y11 VDDR4#3
Y12 VDDR4#4

+1.5V
L9011 BLM15BD121SN1D
+VDDRH1
C9135 1U/6.3V/X5R_4
C9113 1U/6.3V/X5R_4
U11 VDDR5#1
U12 VDDR5#2
V11 VDDR5#3
V12 VDDR5#4
L17 VDDRHA
L16 VSSRHA

180mA
+BBP
Q9008 SI2301BDS-T1-E3
+1.8V
C9071 1U/6.3V/X5R_4
Q9007 2N7002K-T1-E3
(0.9~1.2V)
+VCC_GFX_CORE
R9025 100K_4
+5V
(17) BB_ENA
R9019 10K_4
Q9003 2N7002

(0.9~1.2V)
+VCC_GFX_CORE
C9090 10U/6.3V/X5R_6
C9078 10U/6.3V/X5R_6
C9091 10U/6.3V/X5R_6

M92-S2/M92-XT

PCIE_VDDR#1 AB23
PCIE_VDDR#2 AC23
PCIE_VDDR#3 AD24
PCIE_VDDR#4 AE24
PCIE_VDDR#5 AE25
PCIE_VDDR#6 AE26
PCIE_VDDR#7 AF25
PCIE_VDDR#8 AG26

(PCIE_VDDC 1.1V @ 1A)
(1.1V)
+1.1V_GFX_PCIE
362mA
+1.8V
C9082 1U/6.3V/X5R_4
C9034 0.1U/10V/X5R_4
C9054 1U/6.3V/X5R_4
C9045 0.01U/25V/X7R_4
C9178 10U/6.3V/X5R_6
C9136 10U/6.3V/X5R_6
C9139 1U/6.3V/X5R_4
C9111 0.1U/10V/X5R_4
C9041 10U/6.3V/X5R_6
C9099 1U/6.3V/X5R_4
C9116 0.1U/10V/X5R_4

(1.1V)
+1.1V_GFX_PCIE
1.4A
C9115 1U/6.3V/X5R_4
C9032 1U/6.3V/X5R_4
C9137 1U/6.3V/X5R_4
C9097 1U/6.3V/X5R_4
C9138 1U/6.3V/X5R_4
C9132 1U/6.3V/X5R_4
C9088 1U/6.3V/X5R_4
C9040 10U/6.3V/X5R_6

PCIE_VDDC#1 L23
PCIE_VDDC#2 L24
PCIE_VDDC#3 L25
PCIE_VDDC#4 L26
PCIE_VDDC#5 M22
PCIE_VDDC#6 N22
PCIE_VDDC#7 N23
PCIE_VDDC#8 N24
PCIE_VDDC#9 R22
PCIE_VDDC#10 T22
PCIE_VDDC#11 U22
PCIE_VDDC#12 V22

10.9 A (RMS) / 11.5 A (peak)
6.6 A (RMS) / 7.3 A (peak)
5.8 A (RMS) / 6.4 A (peak)
(0.9~1.2V)

VDDC#1 AA15
VDDC#2 M11
VDDC#3 M12
VDDC#4 N15
VDDC#5 N17
VDDC#6 R13
VDDC#7 R16
VDDC#8 R18
VDDC#9 R21
VDDC#10 T12
VDDC#11 T15
VDDC#12 T17
VDDC#13 T20
VDDC#14 U13
VDDC#15 U16
VDDC#16 U18
VDDC#17 U21
VDDC#18 V15
VDDC#19 V17
VDDC#20 V20
VDDC#21 V21
VDDC#22 Y13
VDDC#23 Y16
VDDC#24 Y18
VDDC#25 Y21

+VCC_GFX_CORE
+BBP
C9085 0.1U/10V/X5R_4
C9077 1U/6.3V/X5R_4

2A
+VDDCI
(0.9~1.2V)

VDDCI#1 M13
VDDCI#2 M15
VDDCI#3 M16
VDDCI#4 M17
VDDCI#5 M18
VDDCI#6 M20
VDDCI#7 M21
VDDCI#8 N20

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PART 5 OF 10
GND

PCIE_VSS#1 AA27
PCIE_VSS#2 AB24
PCIE_VSS#3 AB32
PCIE_VSS#4 AC24
PCIE_VSS#5 AC26
PCIE_VSS#6 AC27
PCIE_VSS#7 AD25
PCIE_VSS#8 AD32
PCIE_VSS#9 AE27
PCIE_VSS#10 AF32
PCIE_VSS#11 AG27
PCIE_VSS#12 AH32
PCIE_VSS#13 K28
PCIE_VSS#14 K32
PCIE_VSS#15 L27
PCIE_VSS#16 M32
PCIE_VSS#17 N25
PCIE_VSS#18 N27
PCIE_VSS#19 P25
PCIE_VSS#20 P32
PCIE_VSS#21 R27
PCIE_VSS#22 T25
PCIE_VSS#23 T32
PCIE_VSS#24 U25
PCIE_VSS#25 U27
PCIE_VSS#26 V32
PCIE_VSS#27 W25
PCIE_VSS#28 W26
PCIE_VSS#29 W27
PCIE_VSS#30 Y25
PCIE_VSS#31 Y32

GND#1 A3
GND#2 A30
GND#3 AA13
GND#4 AA16
GND#5 AB10
GND#6 AB15
GND#7 AB6
GND#8 AC9
GND#9 AD6
GND#10 AD8
GND#11 AE7
GND#12 AG12
GND#13 AH10
GND#14 AH28
GND#15 B10
GND#16 B12
GND#17 B14
GND#18 B16
GND#19 B18
GND#20 B20
GND#21 B22
GND#22 B24
GND#23 B26
GND#24 B6
GND#25 B8
GND#26 C1
GND#27 C32
GND#28 E28
GND#29 F10
GND#30 F12
GND#31 F14
GND#32 F16

GND#33 F18
GND#34 F2
GND#35 F20
GND#36 F22
GND#37 F24
GND#38 F26
GND#39 F6
GND#40 F8
GND#41 G10
GND#42 G27
GND#43 G31
GND#44 G8
GND#45 H14
GND#46 H17
GND#47 H2
GND#48 H20
GND#49 H6
GND#50 J27
GND#51 J31
GND#52 K11
GND#53 K2
GND#54 K22
GND#55 K6
GND#56 M6
GND#57 N11
GND#58 N12
GND#59 N13
GND#60 N16
GND#61 N18
GND#62 N21
GND#63 P6
GND#64 P9
GND#65 R12
GND#66 R15
GND#67 R17
GND#68 R20
GND#69 T13
GND#70 T16
GND#71 T18
GND#72 T21
GND#73 T6
GND#74 U15
GND#75 U17
GND#76 U20
GND#77 U3
GND#78 U9
GND#79 V13
GND#80 V16
GND#81 V18
GND#82 V6
GND#83 Y10
GND#84 Y15
GND#85 Y17
GND#86 Y20
GND#87 Y6
GND#88 T11
GND#89 R11

VSS_MECH#1 A32
VSS_MECH#2 AM1
VSS_MECH#3 AM32

M92-S2/M92-XT

(0.9~1.2V)
+VCC_GFX_CORE
C9083 1U/6.3V/X5R_4
C9087 1U/6.3V/X5R_4
C9094 1U/6.3V/X5R_4
C9106 1U/6.3V/X5R_4
C9075 1U/6.3V/X5R_4
C9070 1U/6.3V/X5R_4
C9076 1U/6.3V/X5R_4
C9101 1U/6.3V/X5R_4
C9079 1U/6.3V/X5R_4
C9096 1U/6.3V/X5R_4
C9107 1U/6.3V/X5R_4
C9095 1U/6.3V/X5R_4
C9084 1U/6.3V/X5R_4

(0.9~1.2V)
(0.9~1.2V)
+VCC_GFX_CORE
+VDDCI
L9010 BLM18EG221SN1D
C9105 0.1U/10V/X5R_4
C9104 0.1U/10V/X5R_4
C9110 1U/6.3V/X5R_4
C9103 1U/6.3V/X5R_4
C9123 10U/6.3V/X5R_6

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MEMORY INTERFACE

(3,18,20,32,33,34,46) +1.5V
(17,18,21) +3.3V_DELAY

U9003C
PART 3 OF 10
MEMORY INTERFACE
M92-S2/M92-XT

(20) M_QSA#[7..0] — M_QSA#[7..0]
(20) M_QSA[7..0] — M_QSA[7..0]
(20) M_DQMA#[7..0] — M_DQMA#[7..0]
(20) M_MDA[63..0] — M_MDA[63..0]
(20) M_MAA[12..0] — M_MAA[12..0]
(20) BA[2..0] — BA[2..0]

M_MDA	DQA	M_MAA	MAA	M_DQMA#	DQMA	M_QSA	QSA
M_MDA0 K27	DQA_0	M_MAA0 K17	MAA_0	M_DQMA#0 E32	DQMA_0	M_QSA0 H28	QSA_0
M_MDA1 J29	DQA_1	M_MAA1 J20	MAA_1	M_DQMA#1 E30	DQMA_1	M_QSA1 C27	QSA_1
M_MDA2 H30	DQA_2	M_MAA2 H23	MAA_2	M_DQMA#2 A21	DQMA_2	M_QSA2 A23	QSA_2
M_MDA3 H32	DQA_3	M_MAA3 G23	MAA_3	M_DQMA#3 C21	DQMA_3	M_QSA3 E19	QSA_3
M_MDA4 G29	DQA_4	M_MAA4 G24	MAA_4	M_DQMA#4 E13	DQMA_4	M_QSA4 E15	QSA_4
M_MDA5 F28	DQA_5	M_MAA5 H24	MAA_5	M_DQMA#5 D12	DQMA_5	M_QSA5 D10	QSA_5
M_MDA6 F32	DQA_6	M_MAA6 J19	MAA_6	M_DQMA#6 E3	DQMA_6	M_QSA6 D6	QSA_6
M_MDA7 F30	DQA_7	M_MAA7 K19	MAA_7	M_DQMA#7 F4	DQMA_7	M_QSA7 G5	QSA_7
M_MDA8 C30	DQA_8	M_MAA8 J14	MAA_8				
M_MDA9 F27	DQA_9	M_MAA9 K14	MAA_9			M_QSA#0 H27	QSA_0B
M_MDA10 A28	DQA_10	M_MAA10 J11	MAA_10			M_QSA#1 A27	QSA_1B
M_MDA11 C28	DQA_11	M_MAA11 J13	MAA_11			M_QSA#2 C23	QSA_2B
M_MDA12 E27	DQA_12	BA0 J16	MAA_BA0			M_QSA#3 C19	QSA_3B
M_MDA13 G26	DQA_13	BA1 L15	MAA_BA1			M_QSA#4 C15	QSA_4B
M_MDA14 D26	DQA_14	M_MAA12 H11	MAA_12			M_QSA#5 E9	QSA_5B
M_MDA15 F25	DQA_15	BA2 G11	MAA_BA2			M_QSA#6 C5	QSA_6B
M_MDA16 A25	DQA_16					M_QSA#7 H4	QSA_7B
M_MDA17 C25	DQA_17						
M_MDA18 E25	DQA_18						
M_MDA19 D24	DQA_19						
M_MDA20 E23	DQA_20						
M_MDA21 F23	DQA_21						
M_MDA22 D22	DQA_22						
M_MDA23 F21	DQA_23						
M_MDA24 E21	DQA_24						
M_MDA25 D20	DQA_25						
M_MDA26 F19	DQA_26						
M_MDA27 A19	DQA_27						
M_MDA28 D18	DQA_28						
M_MDA29 F17	DQA_29						
M_MDA30 A17	DQA_30						
M_MDA31 C17	DQA_31						
M_MDA32 E17	DQA_32						
M_MDA33 D16	DQA_33						
M_MDA34 F15	DQA_34						
M_MDA35 A15	DQA_35						
M_MDA36 D14	DQA_36						
M_MDA37 F13	DQA_37						
M_MDA38 A13	DQA_38						
M_MDA39 C13	DQA_39						
M_MDA40 E11	DQA_40						
M_MDA41 A11	DQA_41						
M_MDA42 C11	DQA_42						
M_MDA43 F11	DQA_43						
M_MDA44 A9	DQA_44						
M_MDA45 C9	DQA_45						
M_MDA46 F9	DQA_46						
M_MDA47 D8	DQA_47						
M_MDA48 E7	DQA_48						
M_MDA49 A7	DQA_49						
M_MDA50 C7	DQA_50						
M_MDA51 F7	DQA_51						
M_MDA52 A5	DQA_52						
M_MDA53 E5	DQA_53						
M_MDA54 C3	DQA_54						
M_MDA55 E1	DQA_55						
M_MDA56 G7	DQA_56						
M_MDA57 G6	DQA_57						
M_MDA58 G1	DQA_58						
M_MDA59 G3	DQA_59						
M_MDA60 J6	DQA_60						
M_MDA61 J1	DQA_61						
M_MDA62 J3	DQA_62						
M_MDA63 J5	DQA_63						

ODTA0 L18	ODTA0 (20)	
ODTA1 K16	ODTA1 (20)	
CLKA0 H26	CLKA0 (20)	
CLKA1 G9	CLKA1 (20)	
CLKA0B H25	CLKA0# (20)	
CLKA1B H9	CLKA1# (20)	
RASA0B G22	RASA0# (20)	
RASA1B G17	RASA1# (20)	
CASA0B G19	CASA0# (20)	
CASA1B G16	CASA1# (20)	
CSA0B_0 H22	CSA0_0# (20)	
CSA0B_1 J22		
CSA1B_0 G13	CSA1_0# (20)	
CSA1B_1 K13		
CKEA0 K20	CKEA0 (20)	
CKEA1 J17	CKEA1 (20)	
WEA0B G25	WEA0# (20)	
WEA1B H10	WEA1# (20)	
DRAM_RST L10	DRAM_RST# (20)	

WRITE_STROBE_READ_STROBE

MVREFDA K26
MVREFSA J26
CLKTESTA K8
CLKTESTB L7
MEMTEST J8
MEM_CALRP1 K7
NC_MAA_13 G20
NC_MAA_14 G14
NC_MEM_CALRN1 K25
NC_MEM_CALRP0 J25
NC_MEM_CALRN0

DIVIDER RESISTORS	DDR3	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

+1.5V
R9076 100_4
MVREFD_A
R9077 100_4
C9184 0.1U/10V/X5R_4
+1.5V
R9034 100_4
MVREFS_A
R9033 100_4
C9142 0.1U/10V/X5R_4
C9141 0.01U/25V/X7R_4
+1.5V
R9027 4.7K_4
R9026 4.7K_4
R9029 243/F_4
R9031 *4.7K_4@NC
R9030 *4.7K_4@NC
R9032 *4.7K_4@NC
Reserved for furture ASIC

+1.5V
R9079 4.7K_4
C9183 1U/6.3V/X5R_4
R9078 *4.7K_4

THERMAL MONITOR

+3.3V_DELAY
(10,35) MB_CLK
Q9004 2N7002
R9046 4.7K_4
R9047 4.7K_4
Q9000 2N7002
(10,35) MB_DATA
(17) THERMAL_INT#
THERMAL_INT#
U9002
SCLK SDATA ALERT# GND
VDD D+ D- THERM#
ADM1032ARMZ-1
C9021 2200P/50V/X7R_4
C9001 0.1U/10V/X5R_4
VGA_THERMDP (21)
VGA_THERMDN (21)
MB_THERM#
MB_THERM# R9059 *10K_4@NC
THERMAL_INT# R9000 10K_4
+3.3V_DELAY
MB_THERM#
Q9005 2N7002
SYS_SHDN# (38,44,48,49)

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256MB/ 512MB DDR3

(19) M_MDA[63..0] — M_MDA[63..0]
(19) M_MAA[12..0] — M_MAA[12..0]
(19) M_QSA[7..0] — M_QSA[7..0]
(19) M_QSA#[7..0] — M_QSA#[7..0]
(19) M_DQMA#[7..0] — M_DQMA#[7..0]

(3,18,19,32,33,34,46) +1.5V

U9001 VRAM_DDR3 — 96-BALL SDRAM DDR3
U9004 VRAM_DDR3 — 96-BALL SDRAM DDR3
U9005 VRAM_DDR3 — 96-BALL SDRAM DDR3
U9000 VRAM_DDR3 — 96-BALL SDRAM DDR3

Should be 240 Ohms +-1%
R9045 240/F_4
R9080 240/F_4
R9086 240/F_4
R9038 240/F_4

VREFC_VMA1 / VREFD_VMA1 / VREFC_VMA2 / VREFD_VMA2 / VREFC_VMA3 / VREFD_VMA3 / VREFC_VMA4 / VREFD_VMA4
R9043 / R9039 / R9042 / R9082 / R9091 / R9035 / R9037 / R9092 — 4.99K/F_4
R9044 / R9040 / R9081 / R9083 / R9089 / R9041 / R9036 / R9090 — 4.99K/F_4
C9164 / C9146 / C9189 / C9203 / C9200 / C9144 / C9145 / C9201 — 0.1U/10V/X5R_4

close to U3003 AND U3004
C9153 C9197 C9190 C9147 C9216 — 10U/6.3V/X5R_6

close to U3003
C9161 C9162 C9156 C9152 C9148 C9157 C9160 C9155 — 1U/6.3V/X5R_4

close to U3004
C9186 C9193 C9198 C9199 C9192 C9195 C9212 C9202 — 1U/6.3V/X5R_4

close to U3006 AND U3007
C9154 C9149 C9159 C9217 C9215 — 10U/6.3V/X5R_6

close to U3006
C9158 C9151 C9196 C9150 C9165 C9163 C9210 C9207 — 1U/6.3V/X5R_4

close to U3007
C9206 C9213 C9188 C9187 C9194 C9205 C9208 C9214 — 1U/6.3V/X5R_4

CLKA1 / CLKA1# — R9088 56_4 / R9087 56_4 — VMA_CLK1_COMM — C9218 0.01U/16V/X7R_4
CLKA0 / CLKA0# — R9084 56_4 / R9085 56_4 — VMA_CLK0_COMM — C9204 0.01U/16V/X7R_4

MB ASSY' PN	Memory Straps	
31GC5MB0000	800MHz 512MB(64M*16)	AKD5LZGTW00 QuantaBuy
		AKD5LZGTW02 VOL B/S
		QuantaBuy
		VOL B/S
		QuantaBuy
		VOL B/S
		QuantaBuy
		VOL B/S
		QuantaBuy
		VOL B/S
		QuantaBuy
		VOL B/S
		QuantaBuy
		VOL B/S

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(6,10,12,17,18,22,24,44,51) +1.8V
(17,18,19) +3.3V_DELAY
(18,44,50) +VCC_GFX_CORE

U9003J
Part 10 of 10
XTAL / PLL

T9010 — H7 NC_SPV18
J7 SPVSS
+SPV10 H8 SPV10
(17) XTALIN AM28 XTALIN
(17) XTALOUT AK28 XTALOUT
L8 NC_MPV18

DPLL_PVDD AE14 +DPLL_PVDD
DPLL_PVSS AE14
DPLL_VDDC AD14 +DPLL_VDDC
PCIE_PVDD AM30 +PCIE_PVDD

(0.9~1.2V) +VCC_GFX_CORE — L9016 BLM15BD121SN1D
C9182 1U/6.3V/X5R_4
C9180 1U/6.3V/X5R_4
C9179 0.1U/10V/X5R_4
C9181 0.01U/25V/X7R_4

+DPLL_PVDD: L9008 BLM15BD121SN1D — +1.8V 120mA
C9030 0.01U/25V/X7R_4
C9026 0.1U/10V/X5R_4
C9035 10U/6.3V/X5R_6
C9039 10U/6.3V/X5R_6

(1.1V) +1.1V_GFX_PCIE
+DPLL_VDDC: L9012 BLM15BD121SN1D — 150mA
C9176 0.01U/25V/X7R_4
C9167 0.1U/10V/X5R_4
C9166 1U/6.3V/X5R_4
C9169 10U/6.3V/X5R_6

+PCIE_PVDD: L9006 BLM15BD121SN1D — +1.8V 40mA
C9018 1U/6.3V/X5R_4
C9017 0.01U/25V/X7R_4
C9019 0.1U/10V/X5R_4
C9023 10U/6.3V/X5R_6

T9006

Dock DP1 & System DP

U2002 SN74CBT3257CPWR
+5V
C1412 0.1U/10V_4
DPA_AUX1_P 4 C_A
DPA_AUX1_N 7 C_B
DPA_DDCCLK 9 C_C
DPA_DDCDAT 12 C_D
DPC_HPD 1 SE
15 EN#
VCC 16
A0 2
A1 3
B0 5
B1 6
C0 11
C1 10
D0 14
D1 13
GND 8
DPC_AUX_SINK_P_C — C689 0.1U/10V/X5R_4
DPC_AUX_SINK_N_C — C688 0.1U/10V/X5R_4
DPA_AUX_SINK_P (24)
DPC_AUX_SINK_P (41)
DPA_AUX_SINK_N (24)
DPC_AUX_SINK_N (41)
DPA_DDCCLK1 (24)
DPC_DDCCLK2 (41)
DPA_DDCDAT1 (24)
DPC_DDCDAT2 (41)

U9003H
Part 8 of 10
I2C / DDC / AUX

CRT
(25) M92_CRT_DDCCLK — AC1 DDC6CLK
(25) M92_CRT_DDCDAT — AC3 DDC6DATA
R1 SCL
R3 SDA

TMDP / DAC1
AUX1P AD2 DPA_AUX1_P
AUX1N AD4 DPA_AUX1_N
DDC1CLK AE6 DPA_DDCCLK
DDC1DATA AE5 DPA_DDCDAT
AUX2P AD13 DPB_AUX1_P — C687 0.1U/10V/X5R_4 — DPB_AUX_SINK_P (41)
AUX2N AD11 DPB_AUX1_N — C686 0.1U/10V/X5R_4 — DPB_AUX_SINK_N (41)
DDC2CLK AC11 DPB_DDCCLK1 — DPB_DDCCLK1 (41)
DDC2DATA AC13 DPB_DDCDAT1 — DPB_DDCDAT1 (41)

Dock DP0

LVTMDP / DAC2
DDCCLK_AUX5P AE16 M92_LVDS_DDCCLK — M92_LVDS_DDCCLK (23)
DDCDATA_AUX5N AD16 M92_LVDS_DDCDAT — M92_LVDS_DDCDAT (23)
NC_DDCCLK_AUX7P AD20
NC_DDCDATA_AUX7N AC20

LVDS
+3.3V_DELAY
M92_LVDS_DDCCLK — R9064 2.2K_4
M92_LVDS_DDCDAT — R9065 2.2K_4

M92-S2/M92-XT

20mA
+1.8V — L9001 BLM15BD121SN1D
C9003 1U/6.3V/X5R_4
C9009 0.1U/10V/X5R_4
+TSVDD AD17 TSVDD
AC17 TSVSS

U9003I
Part 9 of 10
TSS FDO
TS_FDO R5
DPLUS T4 — VGA_THERMDP (19)
DMINUS T2 — VGA_THERMDN (19)

M92-S2/M92-XT

+3.3V_DELAY
0.1U/10V/X5R_4 C121
Layout: close Dock connector
(17) DPC_HPD_1
U17 TC7SH86FU
DPC_HPD (24,41)
DPA_HPD (24)
R370 150K/F_4

dGPU	detect	no detect
DP(DPA)	DP1	SYS
DP(DPB)	DP0	DP0

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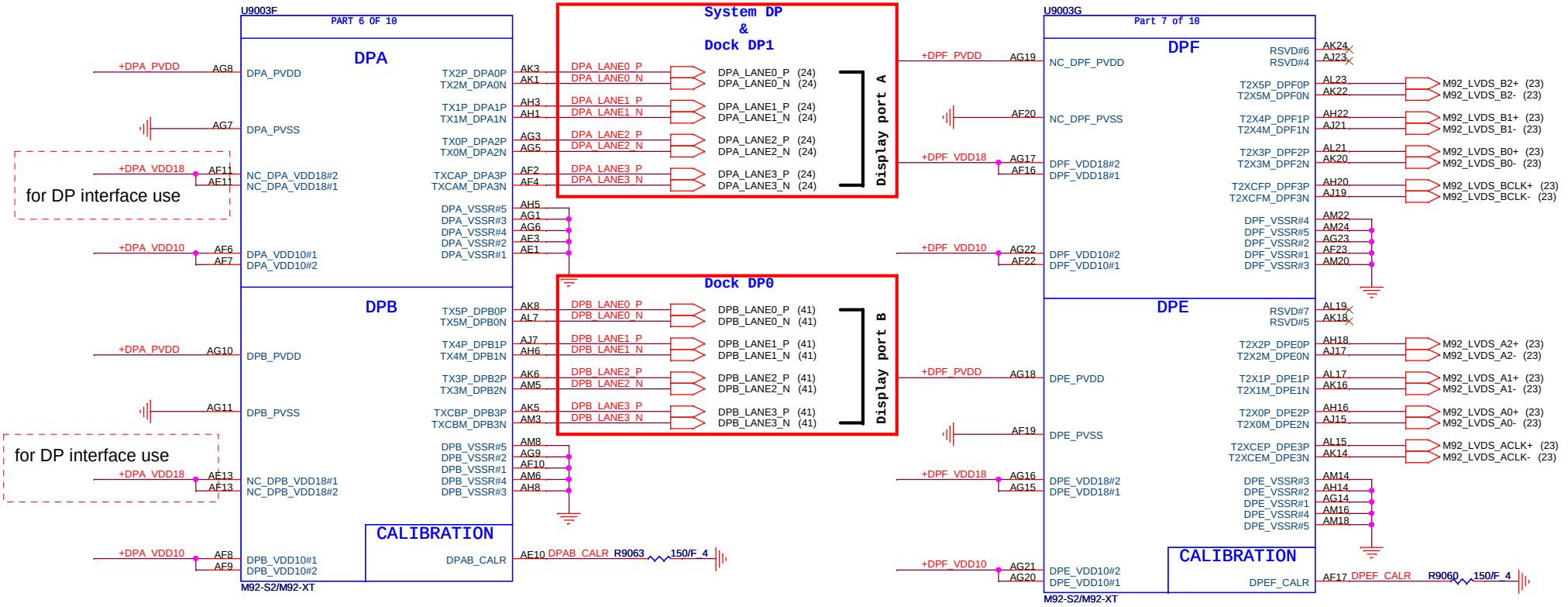
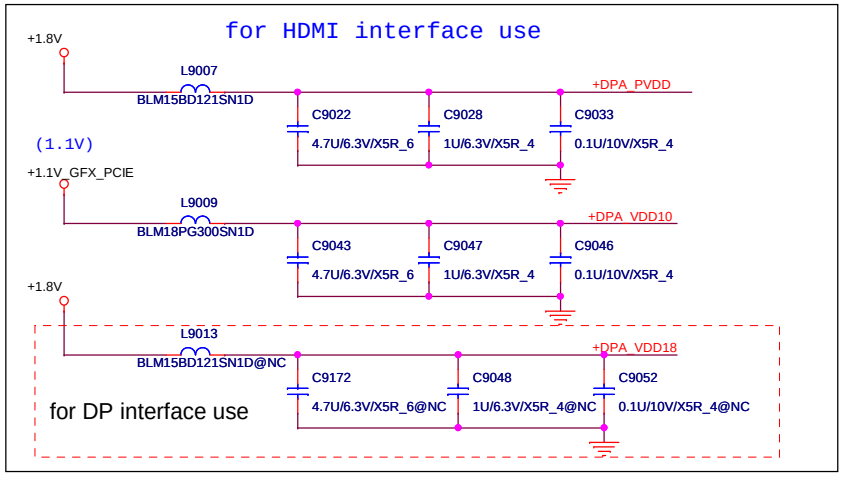
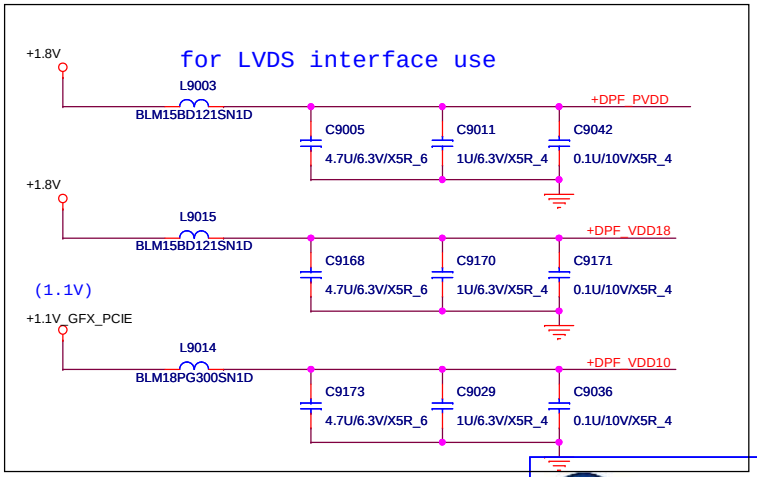
(6,10,12,17,18,21,24,44,51) +1.8V

TMDP(HDMI) INTERFACE

LVDS INTERFACE







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Quanta Computer Inc.

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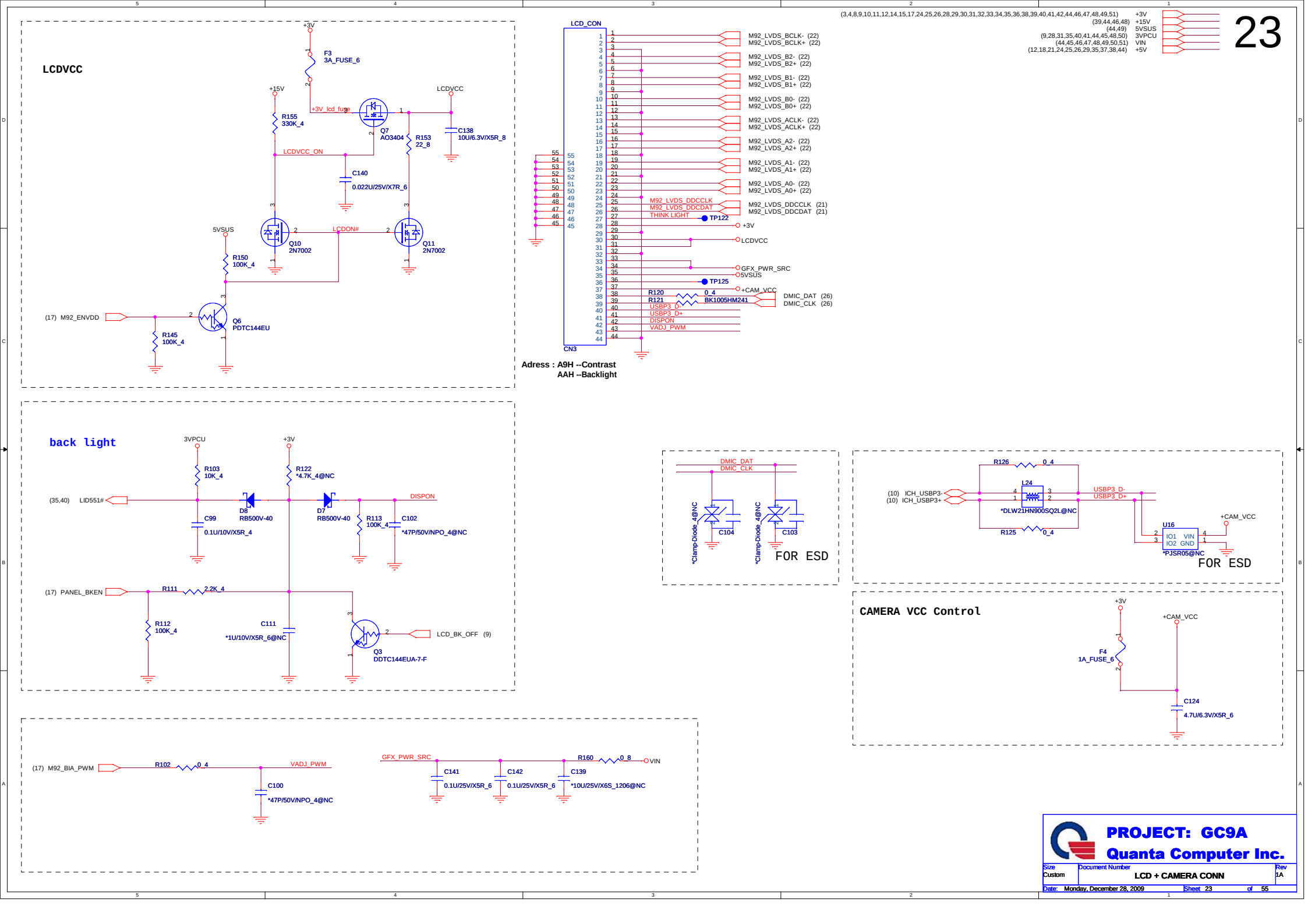

23
LCDVCC
+3V
F3
3A_FUSE_6
+15V
LCDVCC
+3V_lcd_fuse
R155
330K_4
Q7
AO3404
R153
22_8
C138
10U/6.3V/X5R_8
LCDVCC_ON
C140
0.022U/25V/X7R_6
5VSUS
Q10
2N7002
LCDON#
Q11
2N7002
R150
100K_4
(17) M92_ENVDD
Q6
PDTC144EU
R145
100K_4
LCD_CON
CN3
M92_LVDS_BCLK- (22)
M92_LVDS_BCLK+ (22)
M92_LVDS_B2- (22)
M92_LVDS_B2+ (22)
M92_LVDS_B1- (22)
M92_LVDS_B1+ (22)
M92_LVDS_B0- (22)
M92_LVDS_B0+ (22)
M92_LVDS_ACLK- (22)
M92_LVDS_ACLK+ (22)
M92_LVDS_A2- (22)
M92_LVDS_A2+ (22)
M92_LVDS_A1- (22)
M92_LVDS_A1+ (22)
M92_LVDS_A0- (22)
M92_LVDS_A0+ (22)
M92_LVDS_DDCCLK
M92_LVDS_DDCDAT
THINK LIGHT
M92_LVDS_DDCCLK (21)
M92_LVDS_DDCDAT (21)
TP122
+3V
LCDVCC
GFX_PWR_SRC
5VSUS
TP125
+CAM_VCC
R120
0_4
R121
BK1005HM241
USBP3_D-
USBP3_D+
DISPON
VADJ_PWM
DMIC_DAT (26)
DMIC_CLK (26)
Adress : A9H --Contrast
AAH --Backlight
(3,4,8,9,10,11,12,14,15,17,24,25,26,28,29,30,31,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(39,44,46,48) +15V
(44,49) 5VSUS
(9,28,31,35,40,41,44,45,48,50) 3VPCU
(44,45,46,47,48,49,50,51) VIN
(12,18,21,24,25,26,29,35,37,38,44) +5V
back light
3VPCU
+3V
R103
10K_4
R122
*4.7K_4@NC
(35,40) LID551#
D8
RB500V-40
D7
RB500V-40
DISPON
C99
0.1U/10V/X5R_4
R113
100K_4
C102
*47P/50V/NPO_4@NC
(17) PANEL_BKEN
R111
2.2K_4
R112
100K_4
C111
*1U/10V/X5R_6@NC
Q3
DDTC144EUA-7-F
LCD_BK_OFF (9)
DMIC_DAT
DMIC_CLK
*Clamp-Diode_4@NC
C104
*Clamp-Diode_4@NC
C103
FOR ESD
R126
0_4
L24
(10) ICH_USBP3-
(10) ICH_USBP3+
USBP3_D-
USBP3_D+
*DLW21HN900SQ2L@NC
R125
0_4
U16
+CAM_VCC
IO1 VIN
IO2 GND
*PJSR05@NC
FOR ESD
CAMERA VCC Control
+3V
+CAM_VCC
F4
1A_FUSE_6
C124
4.7U/6.3V/X5R_6
(17) M92_BIA_PWM
R102
0_4
VADJ_PWM
C100
*47P/50V/NPO_4@NC
GFX_PWR_SRC
C141
0.1U/25V/X5R_6
C142
0.1U/25V/X5R_6
C139
*10U/25V/X6S_1206@NC
R160
0_8
VIN
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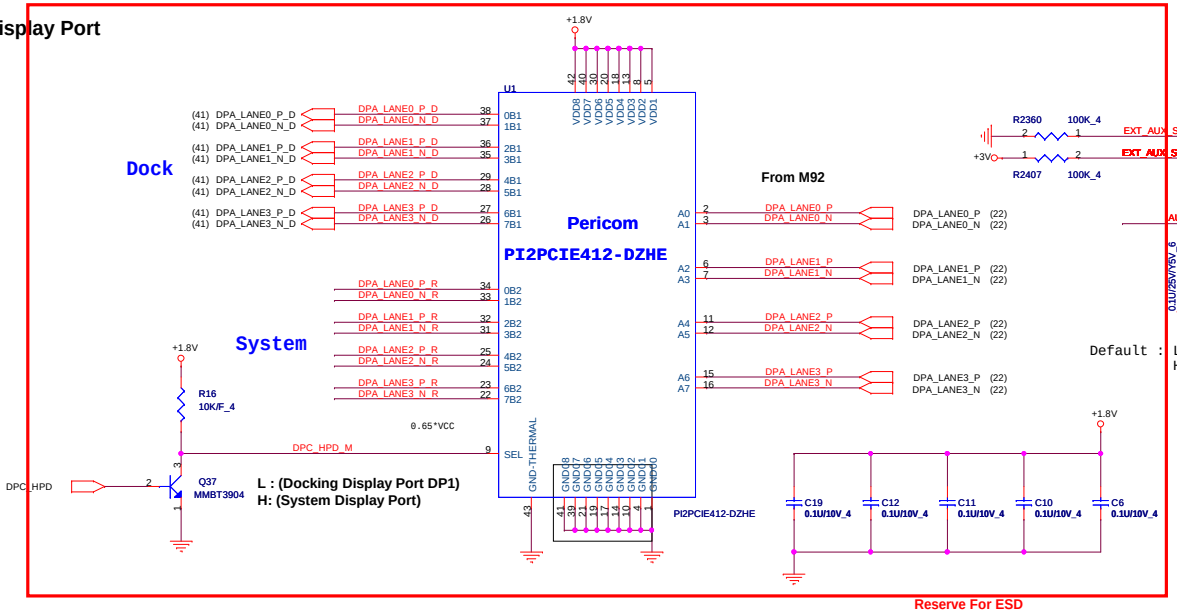
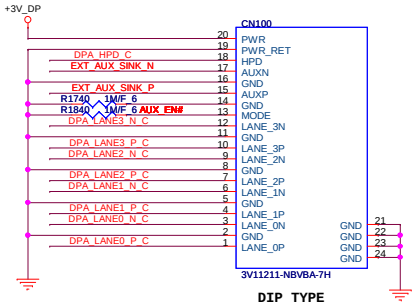
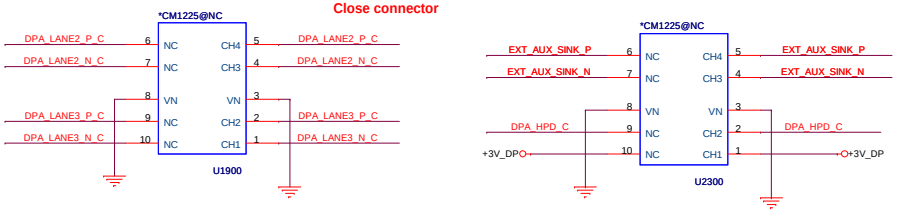
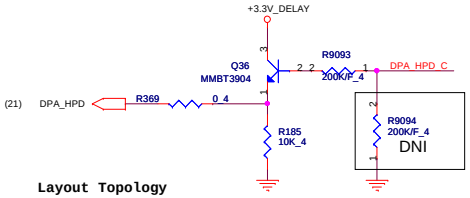
Display Port



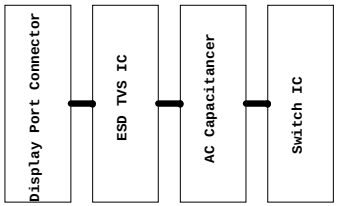


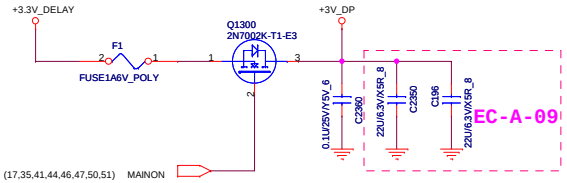
Reserve For ESD
Close connector





Layout Topology





Close to display port connector

Display port sys

DPA_LANE0_N_R	C245	0.1U/10V/X5R_4	DPA_LANE0_N_C
DPA_LANE0_P_R	C244	0.1U/10V/X5R_4	DPA_LANE0_P_C
DPA_LANE1_N_R	C391	0.1U/10V/X5R_4	DPA_LANE1_N_C
DPA_LANE1_P_R	C390	0.1U/10V/X5R_4	DPA_LANE1_P_C
DPA_LANE2_N_R	C247	0.1U/10V/X5R_4	DPA_LANE2_N_C
DPA_LANE2_P_R	C246	0.1U/10V/X5R_4	DPA_LANE2_P_C
DPA_LANE3_N_R	C254	0.1U/10V/X5R_4	DPA_LANE3_N_C
DPA_LANE3_P_R	C253	0.1U/10V/X5R_4	DPA_LANE3_P_C

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(12,18,21,24,26,29,35,37,38,44) +5V
(3,4,8,9,10,11,12,14,15,17,23,24,26,28,29,30,31,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

CRT_VCC
D1 RB500V-40
Layout Note: 40mil
C9 0.1U/10V/X5R_4
+5V
F2 FUSE1A6V_POLY
CRT_VCC_R

CRT_R_CON — L5 BK1608LL680 — CRT_R1
CRT_G_CON — L4 BK1608LL680 — CRT_G1
CRT_B_CON — L3 BK1608LL680 — CRT_B1

R14 150/F_4
R13 150/F_4
R12 150/F_4
C17 5.6P/50V/COG_4
C16 5.6P/50V/COG_4
C15 5.6P/50V/COG_4
C1 5.6P/50V/COG_4
C2 5.6P/50V/COG_4
C3 5.6P/50V/COG_4

TP1
CN17 CRT_CONN

ESD PROTECTION
D25 PJSD05LCTS — CRT_R1
D24 PJSD05LCTS — CRT_G1
D23 PJSD05LCTS — CRT_B1
D21 PJSD05LCTS — CRTVSYNC
D22 PJSD05LCTS — CRTHSYNC
D20 PJSD05LCTS — DDCCLK3
D26 PJSD05LCTS — DDCDAT3
D28 PJSD05LCTS — CRT_VCC_R

+5V
(17) M92_CRT_VSYNC — U31 AHCT1G125DCH — VGAVSYNC_R — R28 10_4 — CRTVSYNC1 (41)
C26 0.1U/10V/X5R_4
(17) M92_CRT_HSYNC — U32 AHCT1G125DCH — VGAHSYNC_R — R15 10_4 — CRTHSYNC1 (41)

Place near U5001,U5002 < 200 mil

CRTVSYNC1 — L1 BLM18AG121SN1D — CRTVSYNC
CRTHSYNC1 — L2 BLM18AG121SN1D — CRTHSYNC
C8 10P/50V/C0G_4
C7 10P/50V/C0G_4

Place near CRT connector < 200 mil

+3.3V_DELAY
CRT_VCC
R8 10K_4
R5 10K_4
R4 2.2K_4
R6 2.2K_4

(21) M92_CRT_DDCCLK — Q21 2N7002K-T1-E3 — DDCCLK2 — R1 0_6 — DDCCLK3 — DDCCLK3 (41)
+3V
(21) M92_CRT_DDCDAT — Q22 2N7002K-T1-E3 — DDCDAT2 — R2 0_6 — DDCDAT3 — DDCDAT3 (41)

C5 *10P/50V/COG_4@NC
C4 *10P/50V/COG_4@NC

+5V
C494 0.1U/10V_4

U40 SN74CBT3257CPWR
(17) M92_CRT_RED — C_A — CRT_R_CON — DOCK_RED (41)
(17) M92_CRT_GRN — C_B — CRT_G_CON — DOCK_GEN (41)
(17) M92_CRT_BLU — C_C — CRT_B_CON — DOCK_BLU (41)
R396 10K_4 — C_D
(41) DOCK_ATTACHED_3V# — SE / EN#
VCC, GND

SEL	FUNCTION(COM)
LOW	IN_x0
HIGH	IN_x1

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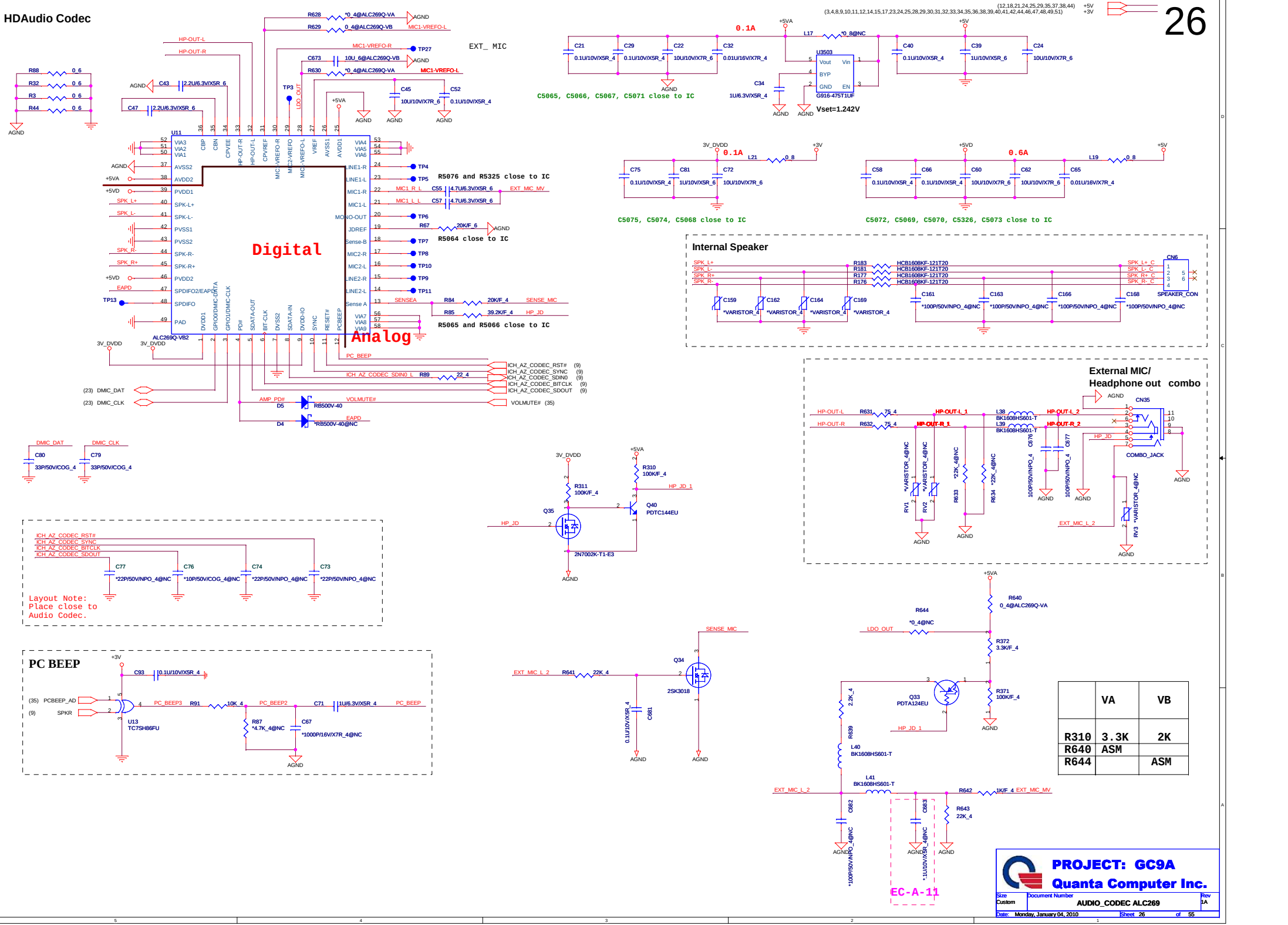
HDAudio Codec



	VA	VB
R310	3.3K	2K
R640	ASM	
R644		ASM

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Custom	AUDIO_CODEC ALC269	1A

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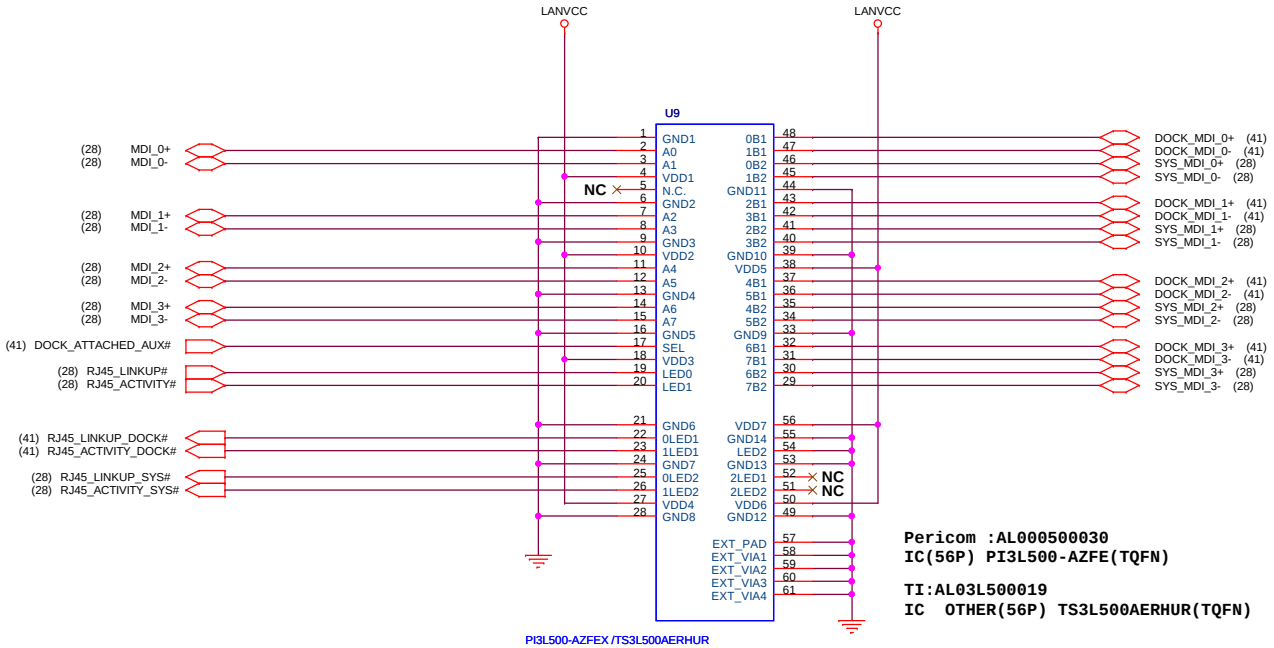
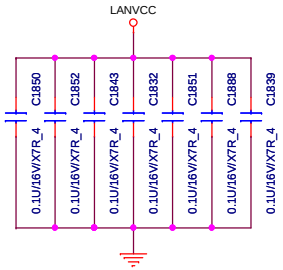


Pericom :AL000500030
IC(56P) PI3L500-AZFE(TQFN)

TI:AL03L500019
IC OTHER(56P) TS3L500AERHUR(TQFN)



PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN SW	1A

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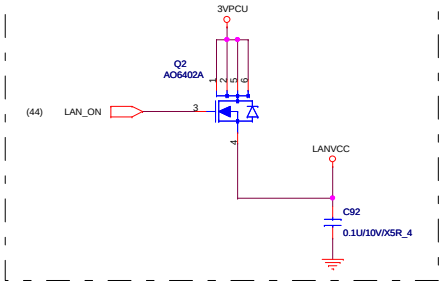
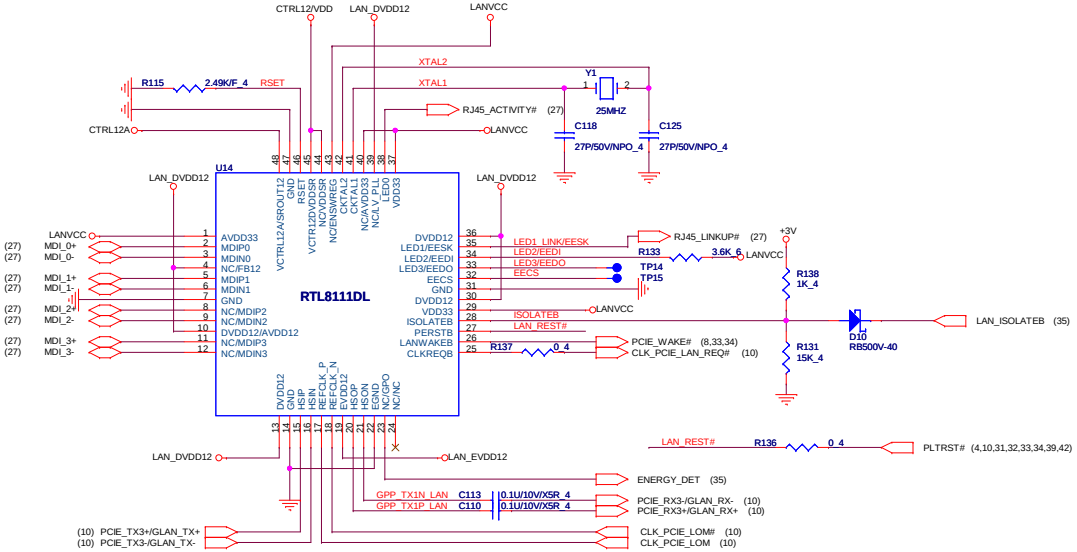
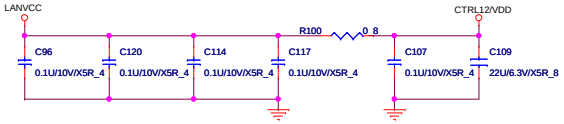
(27,41,44) LANVCC
(3,4,8,9,10,11,12,14,15,17,23,24,25,26,29,30,31,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(9,23,31,35,40,41,44,45,48,50) 3VPCU

LANVCC

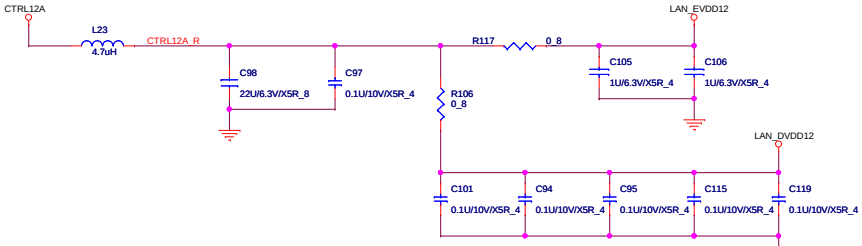






* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.

Place C5113 ,C5094 closed to U5006 pins44,45.



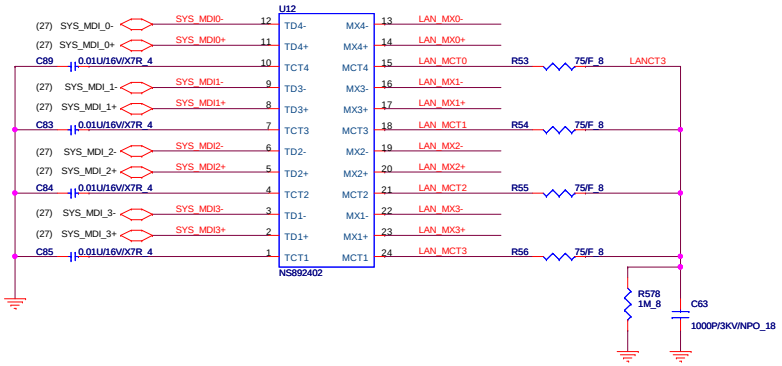
* C5116 and C5273 are for U5006 EVDD12 pin 19.

* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

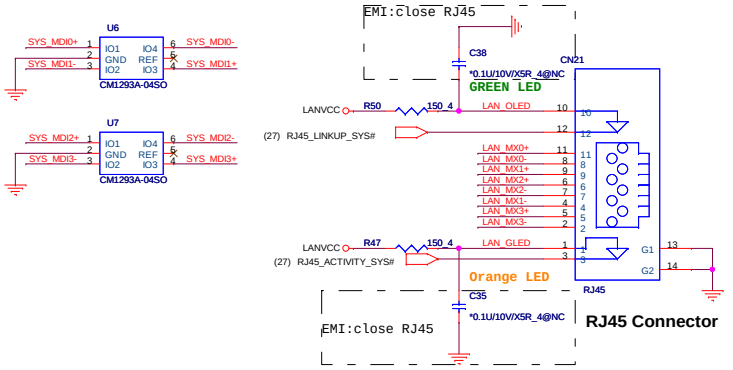
Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.

Layout:All termination signal should have 20 mil trace

Tramsformer



RJ45 Connector



PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111DL	1A
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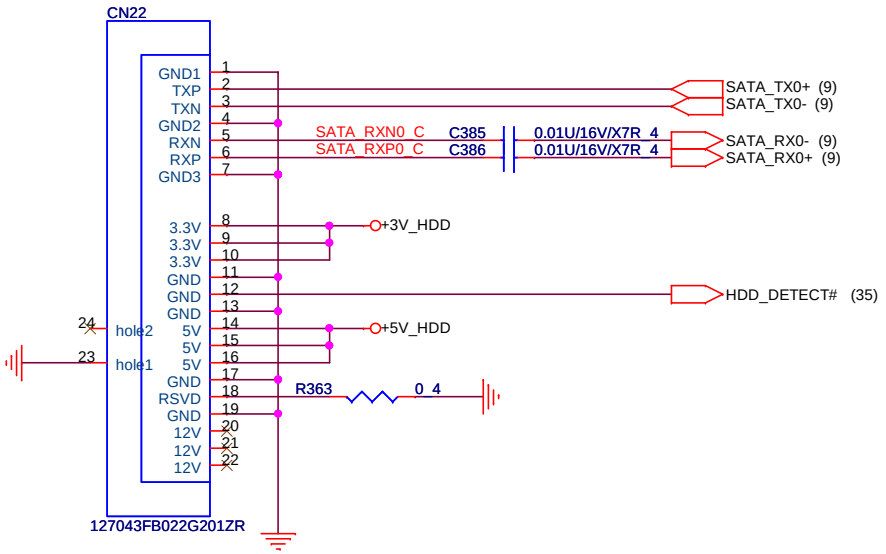
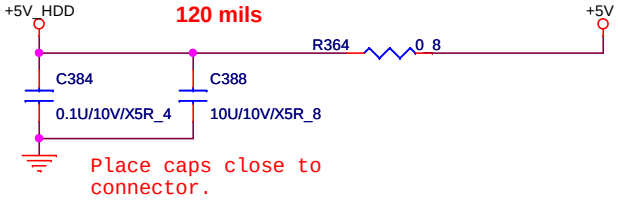
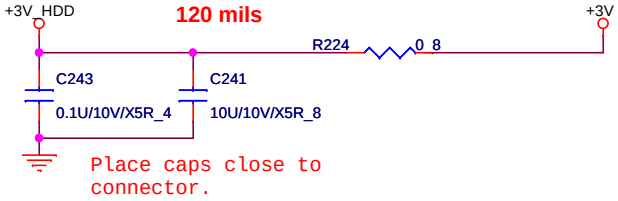
SATA Connector.

(12,18,21,24,25,26,35,37,38,44) +5V
(3,4,8,9,10,11,12,14,15,17,23,24,25,26,28,30,31,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V

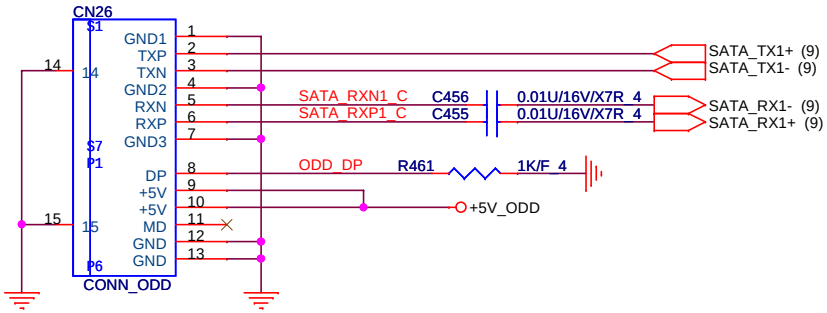
29

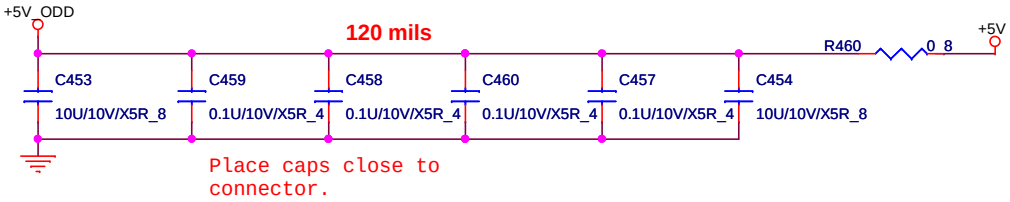






ODD Connector

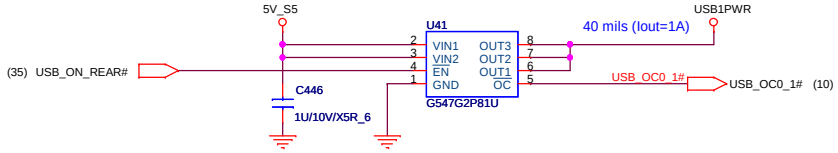




PROJECT: GC9A
Quanta Computer Inc.

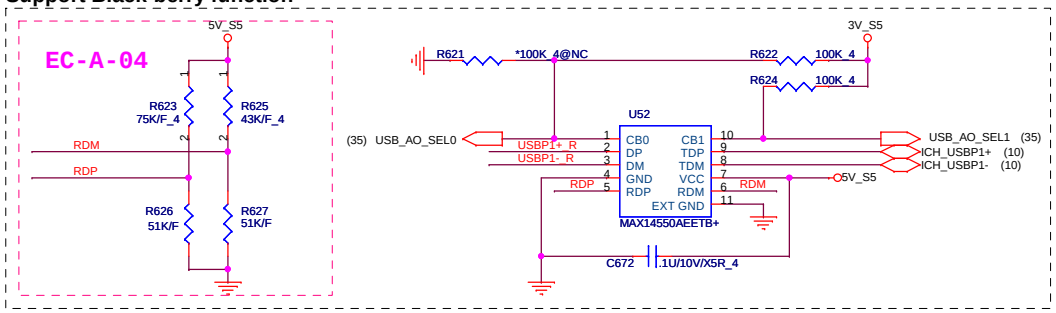
Size	Document Number	Rev
Custom	SATA (HDD&CD_ROM)	1A
Date: Tuesday, January 05, 2010	Sheet 29 of 55	

USBX1

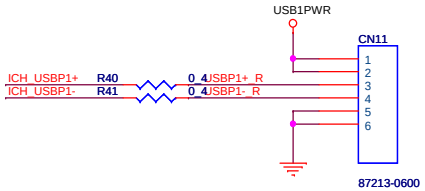


(12,31,44) 5V_S5
(3,4,8,9,10,11,12,14,15,17,23,24,25,26,28,29,31,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V

Support Black-berry function



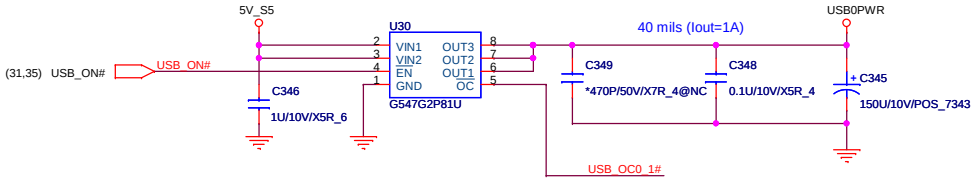
USB X1---> Wire to board conn

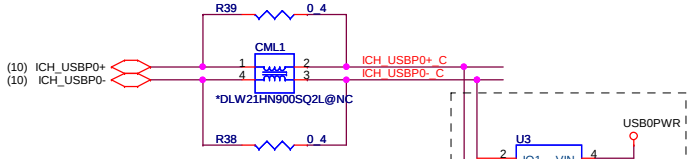


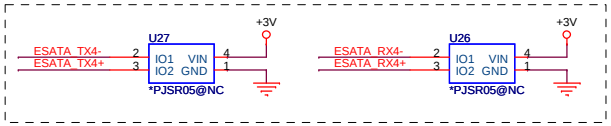
USB 1

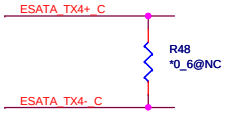
	w/ AOU3	w/o AOU3
R40	NO ASM	ASM
R41	NO ASM	ASM
U52	ASM	NO ASM
R622	ASM	NO ASM
R624	ASM	NO ASM
R626	ASM	NO ASM
C676	ASM	NO ASM

USB + E-SATA

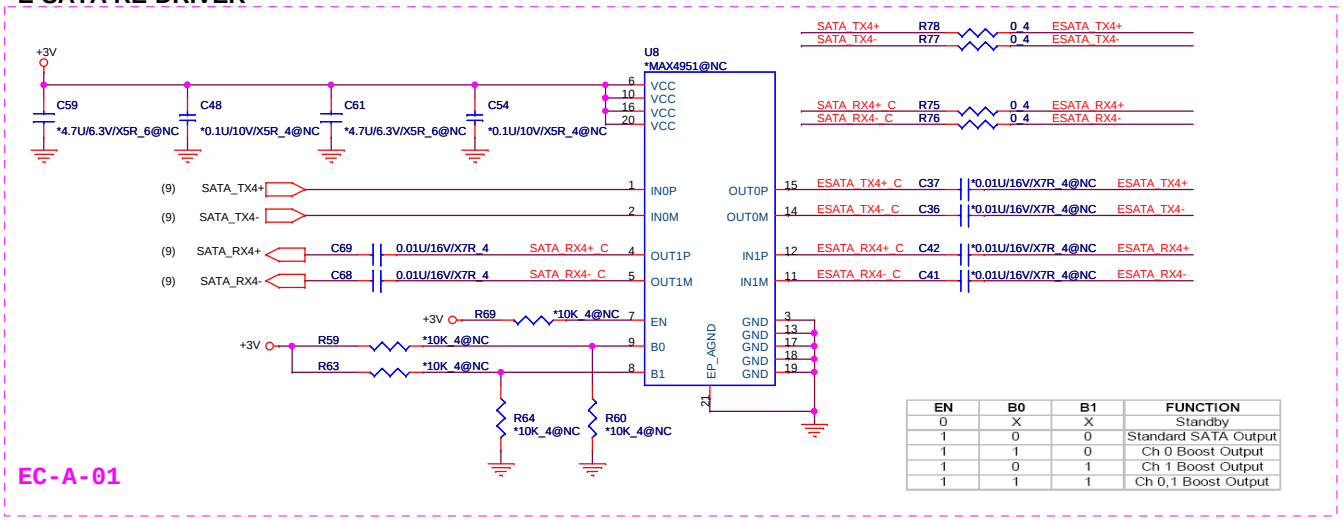








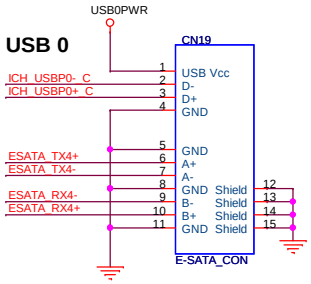
E-SATA RE-DRIVER



EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

EC-A-01

USB 0



PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB X1/USB+ESATA	1A

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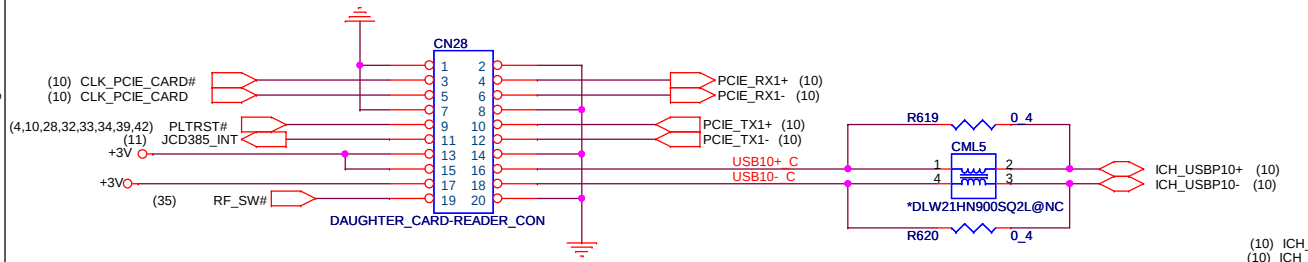
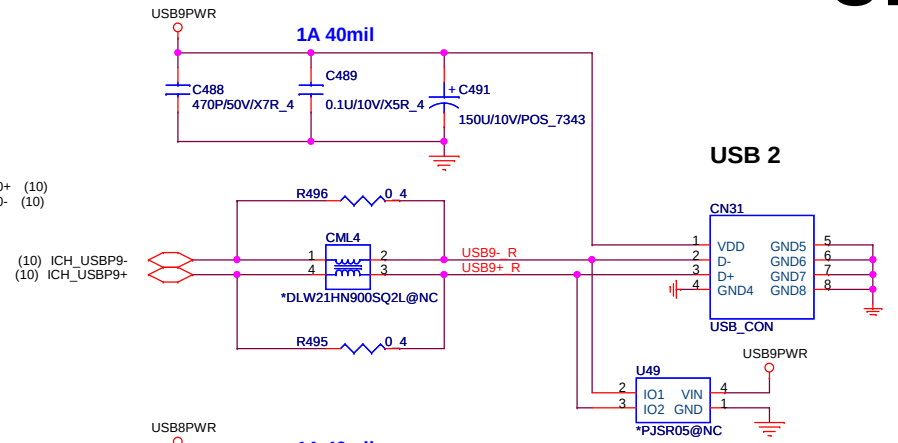
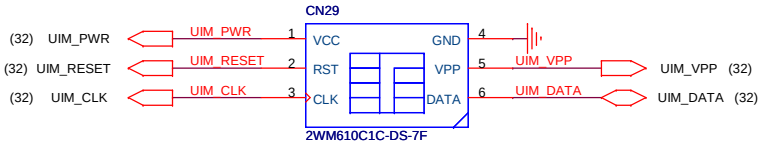
(12,30,44) 5V_S5
(3,4,8,9,10,11,12,14,15,17,23,24,25,26,28,29,30,32,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(9,23,28,35,40,41,44,45,48,50) 3VPCU
(9,34,35,44,50) 3VSUS



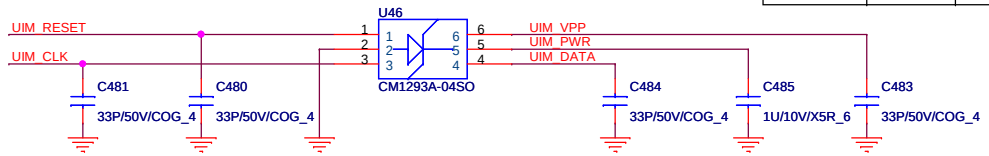


SIM Card CONN

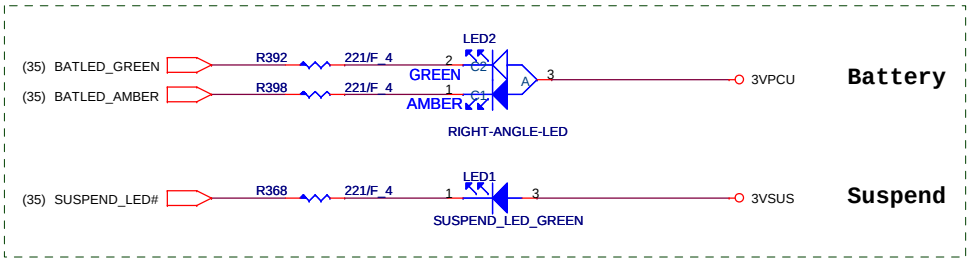


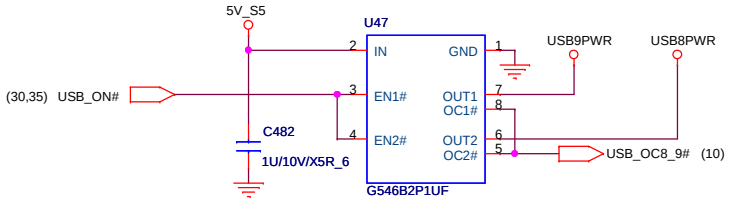
	w/ WWAN	w/o WWAN
CN29	ASM	NO ASM
U46	ASM	NO ASM
C480-C481	ASM	NO ASM
C483-C485	ASM	NO ASM

Layout Note:
UIM_RESET,UIM_CLK,UIM_DATA routting as short as possible



FRONT LEDs





PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB X2/SIM_CARD/LEDs/RF	1A

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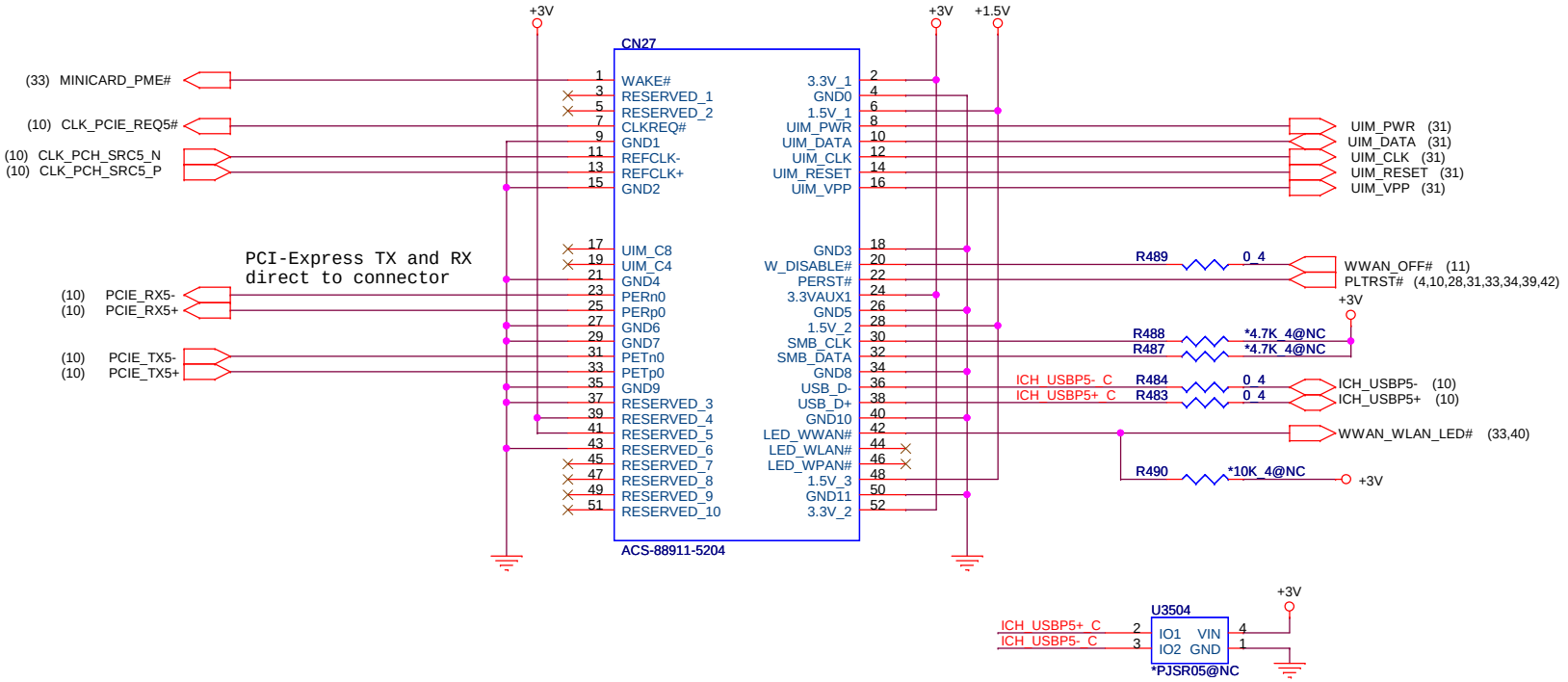
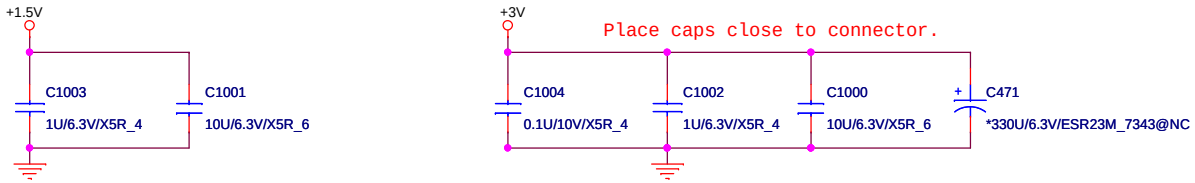
(3,4,8,9,10,11,12,14,15,17,23,24,25,26,28,29,30,31,33,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(3,18,19,20,33,34,46) +1.5V

MiniCard WWAN connector



	w/ WWAN	w/o WWAN
CN27	ASM	NO ASM
R489	ASM	NO ASM
R484	ASM	NO ASM
R483	ASM	NO ASM
C1000~ C1004	ASM	NO ASM



PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-Card (UWB, WWAN)	1A

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MiniCard WLAN/WiMAX connector

(3,4,8,9,10,11,12,14,15,17,23,24,25,26,28,29,30,31,32,34,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(3,18,19,20,32,34,46) +1.5V
(9,23,28,31,35,40,41,44,45,48,50) 3VPCU
(23,44,45,46,47,48,49,50,51) VIN

33

PCI-Express TX and RX direct to connector

CN12

(32) MINICARD_PME#	MINICARD_PME#	1	WAKE#
(36) BBC0EX1		3	RESERVED_1
(36) BBC0EX2		5	RESERVED_2
(10) MINI1CLK_REQ#		7	CLKREQ#
		9	GND1
(10) CLK_PCH_SRC2_N		11	REFCLK-
(10) CLK_PCH_SRC2_P		13	REFCLK+
		15	GND2
	PLTRST# R303 0_4	17	UIM_C8
(10) CLK_LPC_DEBUG	R302 0_4 CLK_DEBUG	19	UIM_C4
		21	GND4
(10) PCIE_RX2-		23	PERn0
(10) PCIE_RX2+		25	PERp0
		27	GND6
		29	GND7
(10) PCIE_TX2-		31	PETn0
(10) PCIE_TX2+		33	PETp0
		35	GND9
		37	RESERVED_3
		39	RESERVED_4
		41	RESERVED_5
		43	RESERVED_6
(8,35) LPCPD#	R305 *0_4@NC LPC_PD#_R	45	RESERVED_7
(9) LPC_DRQ#0	R308 *0_4@NC LPC_LDRQ0#_R	47	RESERVED_8
(9,35,39) IRQ_SERIRQ	R307 *0_4@NC IRQ_SERIRQ_R	49	RESERVED_9
(8,35,39) CLKRUN#	R306 *0_4@NC CLKRUN#_R	51	RESERVED_10

3.3V_1	2		
GND0	4		
1.5V_1	6		
UIM_PWR	8	LPC_LFRAME# (9,35,39)	
UIM_DATA	10	LPC_LAD3 (9,35,39)	
UIM_CLK	12	LPC_LAD2 (9,35,39)	
UIM_RESET	14	LPC_LAD1 (9,35,39)	
UIM_VPP	16	LPC_LAD0 (9,35,39)	
GND3	18		
W_DISABLE#	20	WLAN_OFF_R#	
PERST#	22	PLTRST#	PLTRST# (4,10,28,31,32,34,39,42)
3.3VAUX1	24		+3.3V_WLAN
GND5	26		
1.5V_2	28		
SMB_CLK	30	R479 *4.7K_4@NC	
SMB_DATA	32	R481 *4.7K_4@NC	
GND8	34		
USB_D-	36	ICH_USBP4-_C R486 0_4	ICH_USBP4- (10)
USB_D+	38	ICH_USBP4+_C R485 0_4	ICH_USBP4+ (10)
GND10	40		
LED_WWAN#	42		
LED_WLAN#	44		WWAN_WLAN_LED# (32,40)
LED_WPAN#	46		
1.5V_3	48	R482 *10K_4@NC	+3V
GND11	50		
3.3V_2	52		

ACS-88911-5204

3V_S5
R304 *10K_4@NC
(8,28,34) PCIE_WAKE# — Q19 *PDTC144EU@NC — MINICARD_PME#

WLAN_OFF_R# — D27 RB500V-40 — WLAN_OFF# (11)
R480 *0_4@NC

ICH_USBP4-_C, ICH_USBP4+_C — U45 *PJSR05@NC (IO1 VIN, IO2 GND) — +3.3V_WLAN

+3.3V_WLAN — R478 0_8 — +3V

+1.5V: C1006 1U/6.3V/X5R_4; C463 0.1U/10V/X5R_4; C469 10U/6.3V/X5R_8
+3.3V_WLAN: C467 0.1U/10V/X5R_4; C1007 1U/6.3V/X5R_4; C464 0.1U/10V/X5R_4; C1008 1U/6.3V/X5R_4; C1005 10U/6.3V/X5R_8; C462 *330U/6.3V/ESR23M_7343@NC

Place caps close to connector.

PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-Card (WLAN)	1A

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Express Card

(3,4,8,9,10,11,12,14,15,17,23,24,25,26,28,29,30,31,32,33,35,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(3,18,19,20,32,33,46) +1.5V
(9,31,35,44,50) 3VSUS

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

(10) ICH_USBP2+
(10) ICH_USBP2-
R179 0_4
R178 0_4
L26
*DLW21HN900SQ2L@NC
USBP2_D+
USBP2_D-
U19
IO1 VIN
IO2 GND
*PJSR05@NC
+3.3V_CARD
FOR ESD

+1.5V +3V 3VSUS +3.3V_CARDAUX +3.3V_CARD +1.5V_CARD
U20
AUXIN AUXOUT
3.3VIN_0 3.3VOUT_0
3.3VIN_1 3.3VOUT_1
1.5VIN_0 1.5VOUT_0
1.5VIN_1 1.5VOUT_1
ExpressSwitch
SHDN# PERST#
STBY# CPPE#
SYSRST# CPUSB#
OC#
NC RCLKEN
GND0
G577BSR91U/RT9716AGQW

3VSUS
R172 10K_4 2231_SHDN#
R173 10K_4 2231_STBY#
(4,10,28,31,32,33,39,42) PLTRST#
Q39
2N7002
+3V
CARD_RESET#
EXPRCRD_PWREN#
CPUSB#
R182 *100K_4@NC
R180 *100K_4@NC
TP18
TP17

20090928
avoid current leakage

CN4
GND_1 USB- USB+ CPUSB# RSV_0 RSV_1 SMBCLK SMBDATA +1.5V_0 +1.5V_1 WAKE# +3.3VAUX PERST# +3.3V_1 +3.3V_2 CLKREQ# CPPE# REFCLK- REFCLK+ GND_2 PERn0 PERp0 GND_3 PETn0 PETp0 GND_4 NC1 NC2 NC3 NC4 NC5
48303-0033
JAE PX10FS16PH-26P
USBP2_D-
USBP2_D+
CPUSB#
+3.3V_CARDAUX
R170 10K_4
R171 10K_4
+1.5V_CARD
(8,28,33) PCIE_WAKE#
+3.3V_CARDAUX
CARD_RESET#
+3.3V_CARD
(10) CARD_CLK_REQ#
(11) EXPRCRD_PWREN#
(10) CLK_PCH_SRC4_N
(10) CLK_PCH_SRC4_P
EXPRCRD_PWREN#
(10) PCIE_RX4-
(10) PCIE_RX4+
(10) PCIE_TX4-
(10) PCIE_TX4+
C674 0.047U/25V/X7R_4

+1.5V C170 0.1U/10V/X5R_4 Please the cap near pin 12 & 14(1.5VIN).
+3V C157 0.1U/10V/X5R_4 Please the cap near pin 2 & 4 (3.3VIN).
3VSUS C165 0.1U/10V/X5R_4 Please the cap near pin 17 (AUXIN).
+3.3V_CARDAUX C167 0.1U/10V/X5R_4 Please the cap near pin 15 (AUXOUT).
+3.3V_CARD C160 0.1U/10V/X5R_4 Please the cap near pin 3 & 5 (3.3VOUT).
+1.5V_CARD C171 0.1U/10V/X5R_4 Please the cap near pin 11 & 13(1.5VOUT).

+1.5V_CARD C158 0.1U/10V/X5R_4 C155 0.1U/10V/X5R_4 Please the cap near connector.
+3.3V_CARD C153 0.1U/10V/X5R_4 C156 0.1U/10V/X5R_4 C154 10U/6.3V/X5R_6 Please the cap near connector.

PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Express Card	1A
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(3,4,8,9,10,11,12,14,15,17,23,24,25,26,28,29,30,31,32,33,34,36,38,39,40,41,42,44,46,47,48,49,51) +3V
(9,23,28,31,40,41,44,45,48,50) 3VPCU
(9,12) +3VRTC
(12,18,21,24,25,26,29,37,38,44) +5V

IT8502E

RTC_VCC +3VRTC
R148 0_4
C127 0.1U/10V/X5R_4

IT8512_AVCC L20 10_6 3VPCU
C82 1000P/16V/X7R_4
C90 1U/6.3V/X5R_4
L22 BLM18AG121SN1D
L25 BLM18AG121SN1D 3VPCU
C128 0.1U/10V/X5R_4
(For PLL Power)

Layout Note:
Place all capacitors close to IT8512.

3VPCU
C91 0.1U/10V/X5R_4
C108 0.1U/10V/X5R_4
C116 0.1U/10V/X5R_4
C129 0.1U/10V/X5R_4
C112 0.1U/10V/X5R_4
C126 0.1U/10V/X5R_4

(10) CLK_PCI_8512 CLK_PCI_8512
C131 *15P/50V/NPO_4@NC
EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

+3V 3VPCU RTC_VCC
C134 0.1U/10V/X5R_4

IT8512_VSTBY

TRACK_POINT_RESET
RF_SW#
TRACK_POINT_RESET (37)
RF_SW# (31)
LAN_ISOLATEB (28)
PAD_RESET# PAD_RESET# (37)
ICH_RSMRST# (8)
USB_ON_REAR# (30)
ECPWROK (8)
GSENSOR_TST# (39)
MIC_MUTE_LED# (40)
VRON (44,49)
SPEAKER_MUTE_LED# (40)
MAINON (17,24,41,44,46,47,50,51)
SUSON (44,46)
S5_ON (44)

3VPCU
R109 10K_4
R107 *10K_4@NC
DIS =>R109
UMA=>R107

R99 0_4 CLKRUN# (8,33,39)

+5V
RP1 *10K_8P4R@NC
R97 10K_4
R98 10K_4

(9,33,39) LPC_LAD0
(9,33,39) LPC_LAD1
(9,33,39) LPC_LAD2
(9,33,39) LPC_LAD3
(23,40) LID551#
CLK_PCI_8512
(9,33,39) LPC_LFRAME#
OV_EVENT
(8,33) LPCPD#
(11) SIO_A20GATE
(9,33,39) IRQ_SERIRQ
(11) SIO_EXT_SMI#
(11) SIO_EXT_SCI#
WRST_8512#
(11) SIO_RCIN#
(40) CAPSLED
D9 D13 D11 D12 RB500V-40

LAD0 LAD1 LAD2 LAD3
LPCRST#/WUI4/GPD2
LPCCLK
LFRAME#
LPCPD#/WUI6/GPE6
GA20/GPB5
SERIRQ
ECSMI#/GPD4
ECSCI#/GPD3
WRST#
KBRST#/GPB6
PWUREQ#/GPC7
LPC

SM BUS
SMCLK0/GPB3 MBCLK (45)
SMDAT0/GPB4 MBDATA (45)
SMCLK1/GPC1 MB_CLK (10,19)
SMDAT1/GPC2 MB_DATA (10,19)
SMCLK2/GPF6 AC_PRESENT (8,17)
SMDAT2/GPF7 VOLMUTE# (26)

PS/2
PS2CLK0/GPF0 MSCLK
PS2DAT0/GPF1 MSDATA
PS2CLK1/GPF2 KPCLK
PS2DAT1/GPF3 KPDATA
PS2CLK2/GPF4 TPCLK
PS2DAT2/GPF5 TPDATA
TPCLK (37)
TPDATA (37)

GPIO

(45) D/C#
(44) LAN_POWER
GPC0/CRX
GPB2/CTX
CIR

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

PWM
PWM0/GPA0 PWR_LED# (40)
PWM1/GPA1
PWM2/GPA2 VFAN (38)
PWM3/GPA3 SUSPEND_LED# (31)
PWM4/GPA4 GSENSOR_ON# (39)
PWM5/GPA5 PCBEEP_AD (26)
PWM6/GPA6 ENERGY_DET (28)
PWM7/GPA7 PAD_DETECT# (37)
TACH0/GPD6 FANSIG (38)
TACH1/GPD7 DRAMRST_CTRL_EC (4)
TMR0/WUI2/GPC4 TEMP_ALERT# (11)
TMR1/WUI3/GPC6 HWPG HWPG (4,42,46,47,48,49,50,51)
C691 *1U/10V/X5R_4

WAKE UP
PWRSW/GPE4 NBSWON# NBSWON# (40,41)
RI1#/WUI0/GPD0 SIO_SLP_S3# (8)
RI2#/WUI1/GPD1 ACIN (45)
WUI5/GPE5 CARE_BUTTON# CARE_BUTTON# (40)
RING#/PWRFAIL#/LPCRST#/GPB7 DOCK_ATTACHED_3VPCU# (41)

UART
TXD/GPB1 BATLED_AMBER_LED# BATLED_AMBER (31)
RXD/GPB0 BATLED_GREEN_LED# BATLED_GREEN (31)

A/D D/A
ADC0/GPI0 TEMP_MBAT (45)
ADC1/GPI1 MBATV (45)
ADC2/GPI2 AD_ID (45)
ADC3/GPI3 GSENSOR_Z_R
ADC4/GPI4 GSENSOR_X_R
ADC5/GPI5 GSENSOR_Y_R
ADC6/GPI6 ACDC_ID (41,45)
ADC7/GPI7 PM_SLP_S4# (8)

DAC0/GPJ0 HDD_DETECT# (29)
DAC1/GPJ1 SIO_EXT_WAKE# (10)
DAC2/GPJ2 BL/C# (45)
DAC3/GPJ3 USB_AO_SEL1 (30)
DAC4/GPJ4 DNBSWON_R
DAC5/GPJ5 USB_AO_SEL0 (30)
D6 RB500V-40 SIO_PWRBTN# (8)

CLOCK
CK32KE IT8512_CK32KE
CK32K IT8512_CK32K
Y2 32.768KHZ
C136 15P/50V/NPO_4
C135 15P/50V/NPO_4

FLASH
(8) SUS_PWR_ACK 8512_SCK
(30,31) USB_ON# 8512_SO 8512_SI 8512_SCE#
FLRST#/WUI7/GPG0/TM
FLCLK/SCK
FLAD3/GPG6
FLAD2/SO
FLAD1/SI
FLAD0/SCE#
FLFRAME#/GPG2

KBMX
KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15
MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15
(37,40) MY[0..15]
MX0 MX1 MX2 MX3 MX4 MX5 MX6 MX7
(37,40) MX[0..7]
KSI0/STB# KSI1/AFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7

EC-A-03
R101 100K_4

R609	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

U15 IT8502E

VSS pins: 1, 27, 49, 61, 73, 122, 75, 12
AVSS
C133 *1U/6.3V/X5R_4@NC
C132 0.1U/10V/X5R_4

TP44
Layout Note:
Place this test point on top side
3VPCU R147 470K_4
WRST_8512#
C130 0.1U/10V/X5R_4

3VPCU
MB_CLK R123 4.7K_4
MB_DATA R124 4.7K_4
MBCLK R118 4.7K_4
MBDATA R119 4.7K_4
PAD_RESET# R114 10K_4
BATLED_AMBER_LED# R116 *10K_4@NC
BATLED_GREEN_LED# R110 *10K_4@NC
BL/C# R92 *10K_4@NC
TRACK_POINT_RESET R96 *10K_4@NC
HDD_DETECT# R194 100K_4
DOCK_ATTACHED_3VPCU# R1100 10K_4

+3V
HWPG R130 10K_4

RF ON/OFF SWITCH

3VSUS
R95 100K_4
RF_SW#
C88 0.1U/10V/X5R_4

POWER SWITCH/ CARE BUTTON

EC-A-07

3VPCU R135 10K_4 NBSWON#
C122 0.1U/10V/X5R_4
3VPCU R262 10K_4 CARE_BUTTON#
C382 0.1U/10V/X5R_4

16Mbit (2M Byte), SPI

Winbond	AKE38ZP0N00
SST	AKE28FP0K07
MX	AKE37FP0Z13

3VPCU
R175 10K_4
R187 10K_4
8512_SCE# R188 47_4 8512_SCK1
8512_SCK R189 47_4 8512_SI1
8512_SI R174 15_4 8512_SO1
8512_SO
U21 MX25L1605A
CE# SCK SI SO WP# VDD HOLD# VSS
C180 0.1U/10V/X5R_4

Width = 6mils Spacing = 10 mils

GSENSOR_X_R R94 56K_4 GSENSOR_X (39)
GSENSOR_Y_R R90 56K_4 GSENSOR_Y (39)
GSENSOR_Z_R R93 *56K_4@NC GSENSOR_Z (39)
C87 0.1U/10V/X5R_4
C78 0.1U/10V/X5R_4
C86 *0.1U/10V/X5R_4@NC

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Quanta Computer Inc.

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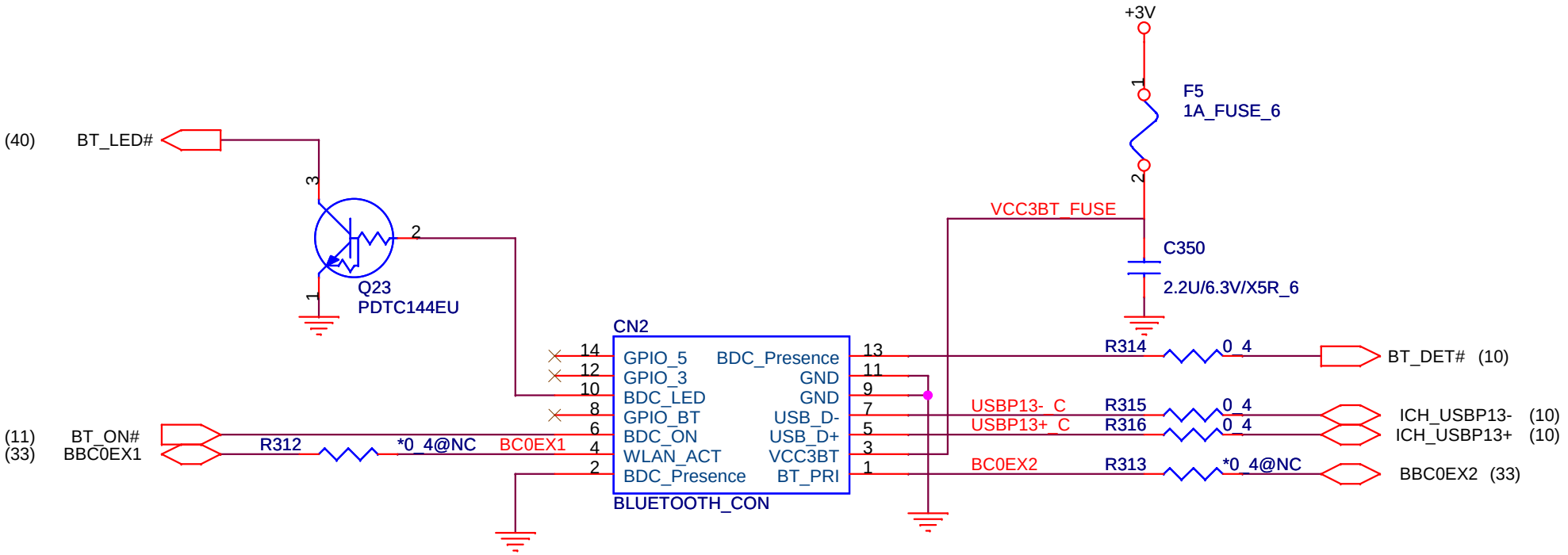
BLUETOOTH

(3,4,8,9,10,11,12,14,15,17,23,24,25,26,28,29,30,31,32,33,34,35,38,39,40,41,42,44,46,47,48,49,51) +3V

36



PROJECT: GC9A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	B/T	1A

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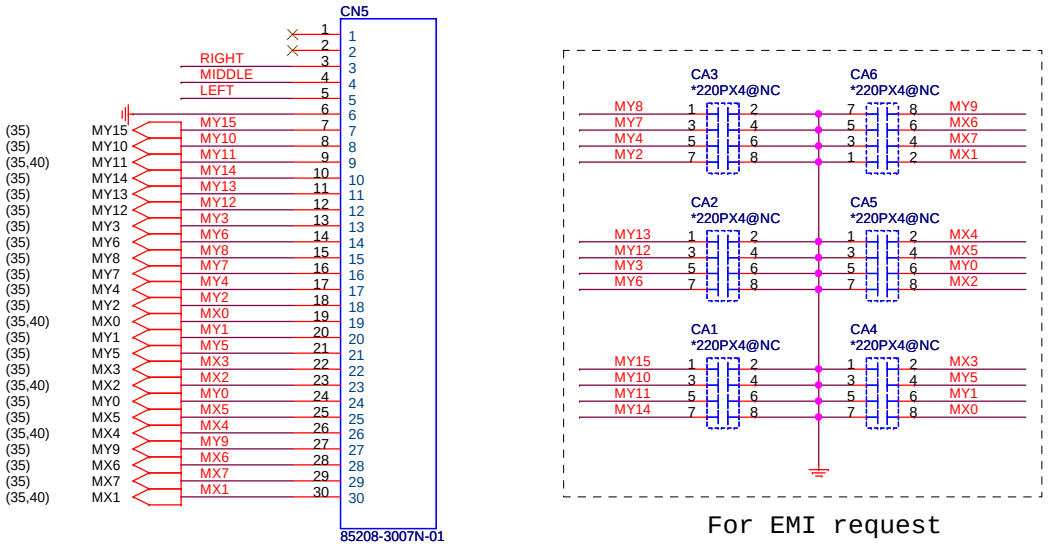
KEYBOARD

KEYBOARD connector

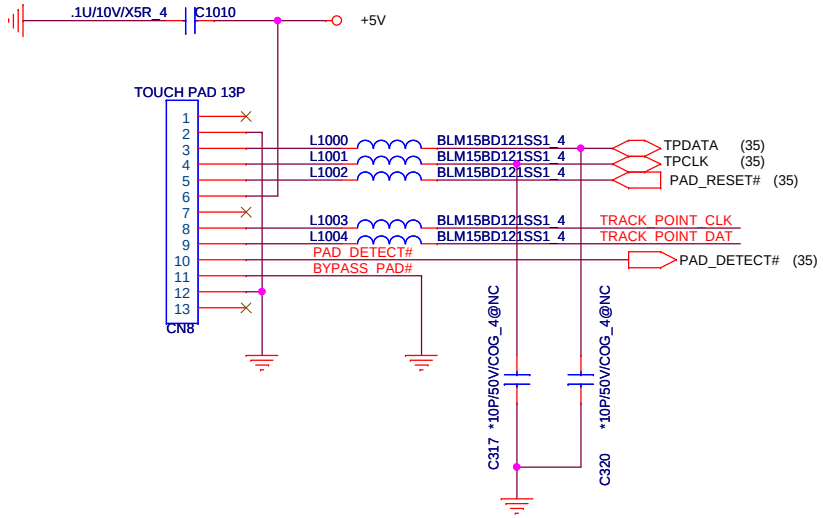


(12,18,21,24,25,26,29,35,38,44) +5V
(9,23,28,31,35,40,41,44,45,48,50) 3VPCU

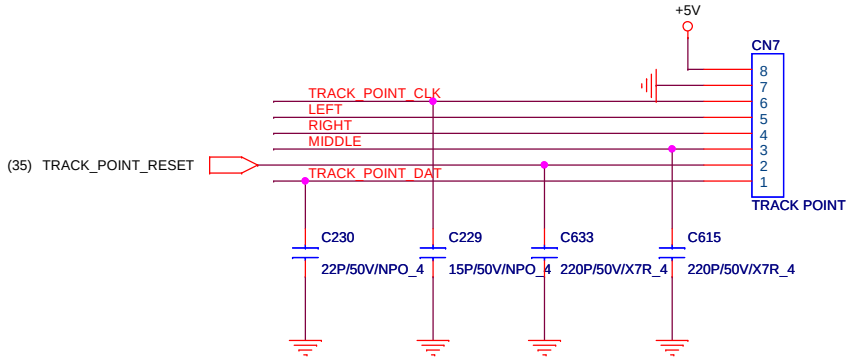
For EMI request

Touch pad

EMI/RF:BEAD NEAR Connector



TRACK POINT



PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	K/B, T/P	1A
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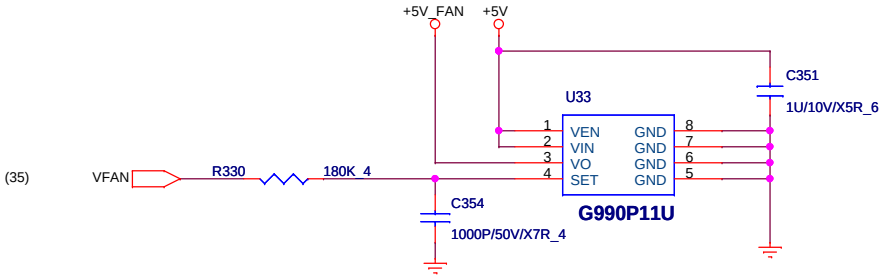
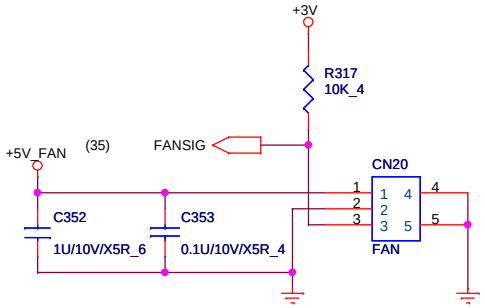
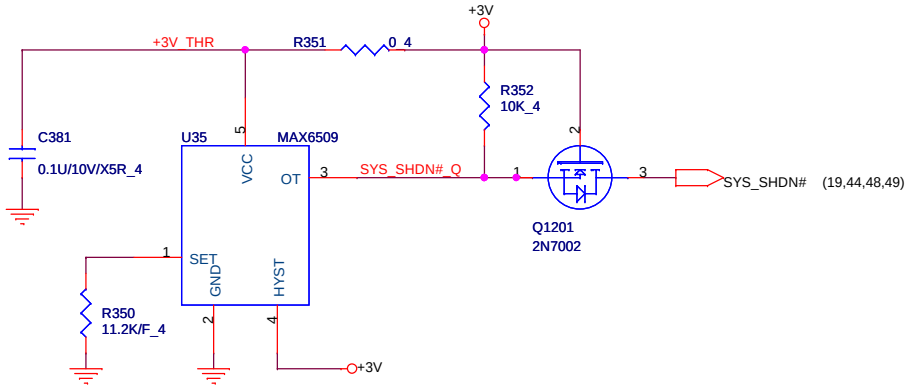
FAN CONTROL

(3,4,8,9,10,11,12,14,15,17,23,24,25,26,28,29,30,31,32,33,34,35,36,39,40,41,42,44,46,47,48,49,51) +3V
(12,18,21,24,25,26,29,35,37,44) +5V







PROJECT: GC9A
Quanta Computer Inc.

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Custom	FAN & THERMAL	1A
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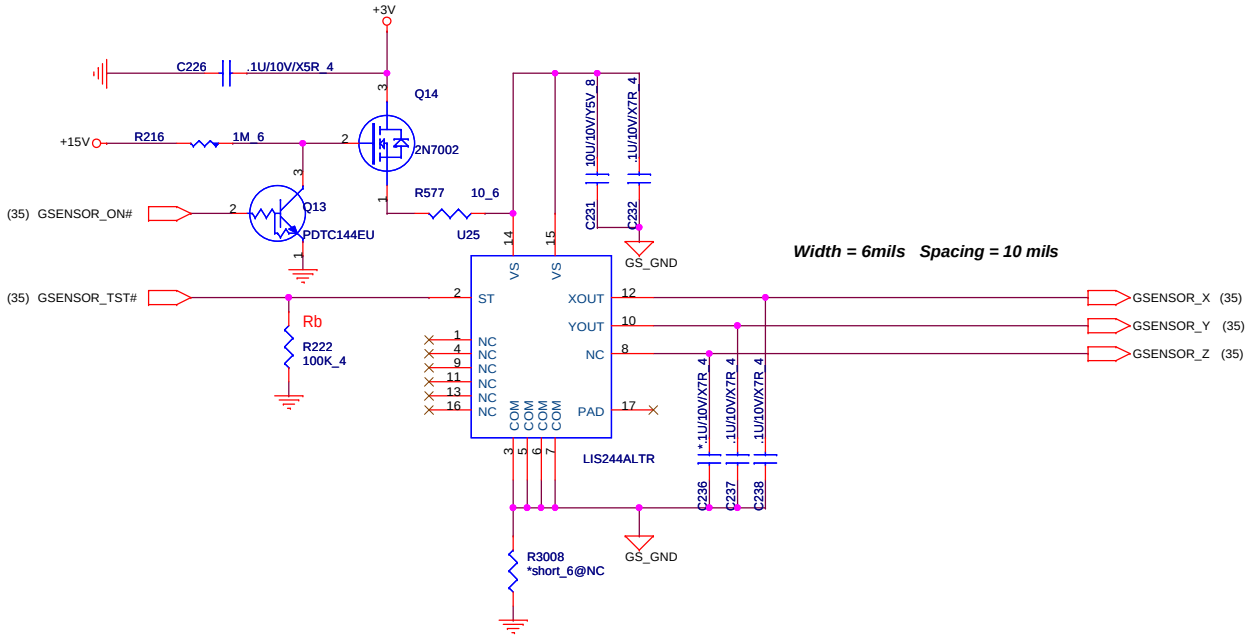
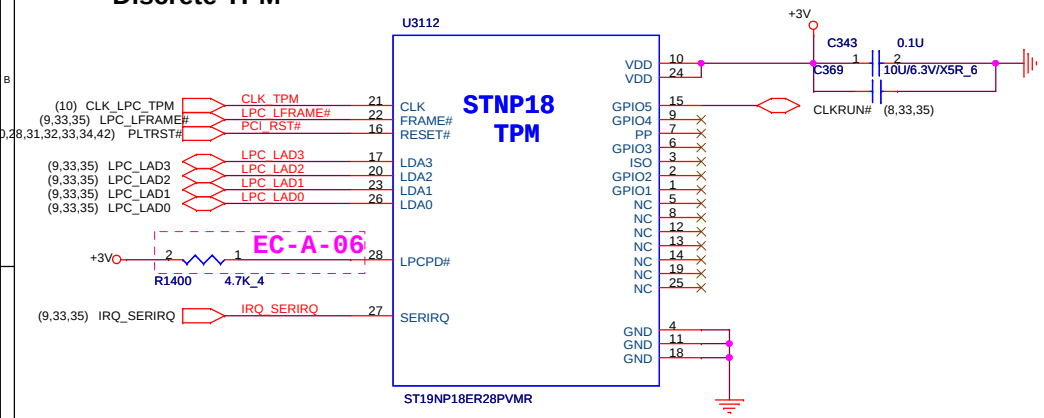
G-SENSOR (2-Axial)



Discrete TPM



supplier P/N:ST19NP18ER28PVMR
Quanta P/N:AL19NP18K13
F/P:tssop28-6_4-65-1_2h

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Quanta Computer Inc.

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Custom	G-SENSOR/Discrete TPM	1A

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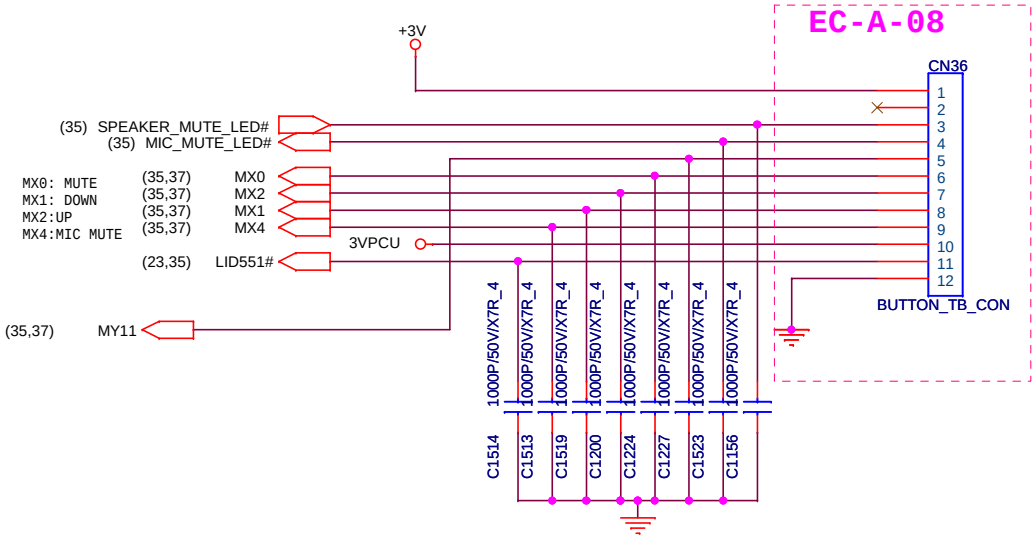
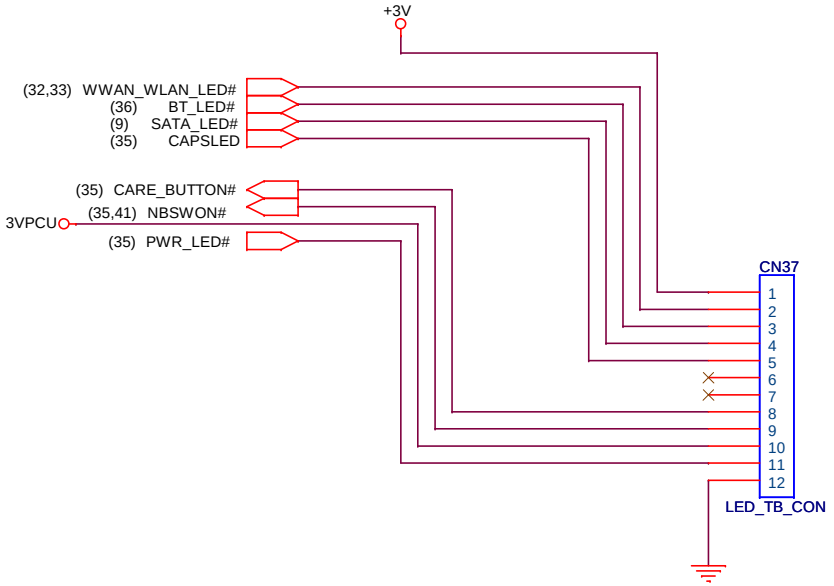
Daughter Boards for LEDs & Ports

FFC TO KBD LEFT SIDE CONNECTOR



FFC TO LED RIGHT SIDE CONNECTOR



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Daughter Boards	1A
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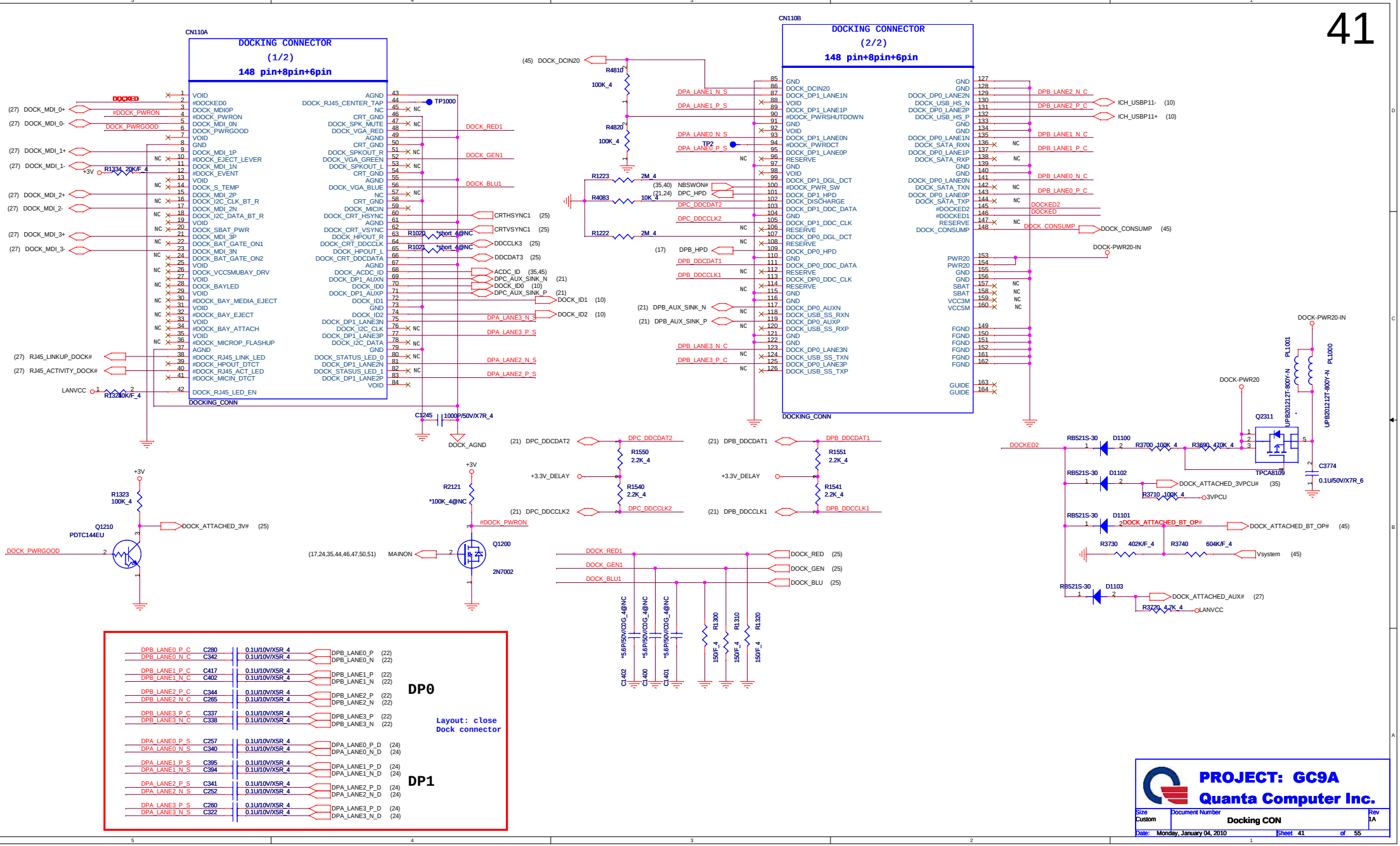
41
CN110A
DOCKING CONNECTOR
(1/2)
148 pin+8pin+6pin
DOCKING_CONN
CN110B
DOCKING CONNECTOR
(2/2)
148 pin+8pin+6pin
DOCKING_CONN
DP0
DP1
Layout: close
Dock connector
PROJECT: GC9A
Quanta Computer Inc.
Size
Custom
Document Number
Docking CON
Rev
1A
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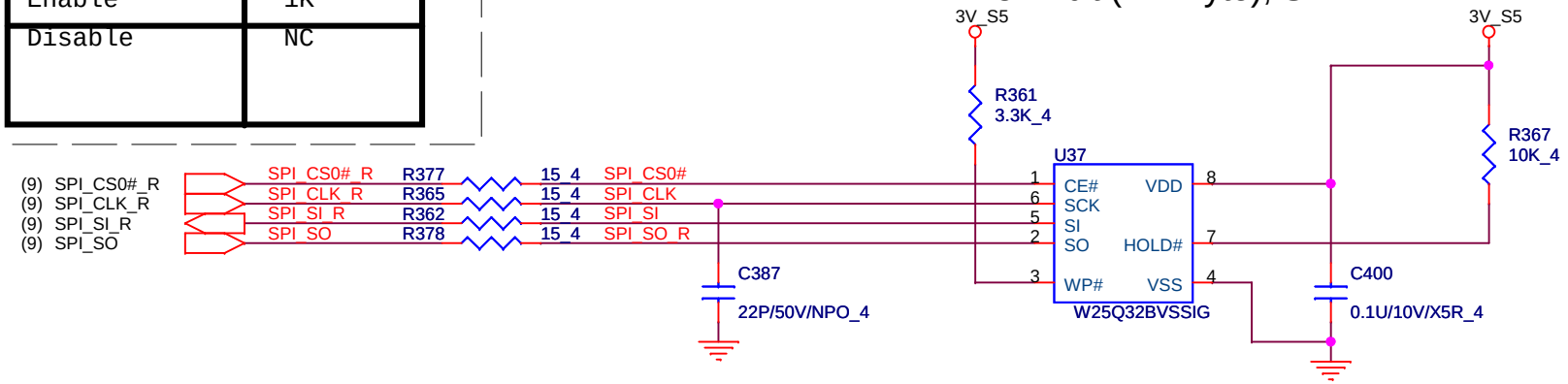
iTPM ENABLE/DISABLE

3V_S5 — R366 *1K_4 — SPI_SI

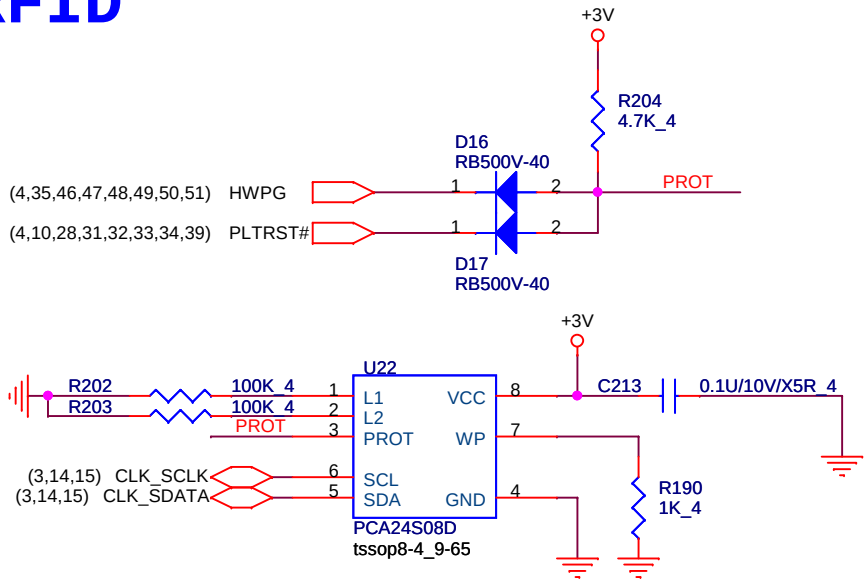
iTPM Function	R366
Enable	1K
Disable	NC

(3,4,8,9,10,11,12,14,15,17,23,24,25,26,28,29,30,31,32,33,34,35,36,38,39,40,41,44,46,47,48,49,51) +3V

For PCH
32Mbit (4M Byte), SPI



RFID



PROJECT: GC9A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	iTPM & RFID EEPROM	1A

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MiniCard WLAN

HOLE13 H-TC197BC142D102P2
HOLE14 H-TC197BC142D102P2
Top side

MiniCard WWAN

HOLE35 H-TC236BC102D64P2
HOLE36 H-TC236BC102D64P2
Bot side

Hole for PCH support

HOLE34 H-TC197BC118D118P2
HOLE33 H-TC197BC118D118P2

Drink Hole

HOLE8 *H-C298D298N

Bluetooth nut

HOLE3 H-TC197D118PT
Top side

Hole for CPU support

HOLE29 *H-C142D142N@NC
HOLE31 *H-C142D142N@NC
HOLE30 *H-C142D142N@NC
HOLE32 *H-C142D142N@NC

VGA nut

HOLE27 H-TC197BC158D122P2
HOLE28 H-TC197BC158D122P2
HOLE26 H-TC197BC158D122P2

Break Hole

HOLE11 *o-gc4@NC

Boundary Hole

HOLE7 *H-TC276BC216D91P2
HOLE4 *H-C276D91P2@NC
HOLE5 *H-C86D86N@NC
HOLE15 *H-TC236BC216D87P2
HOLE10 *H-TC209BC315D209P2
HOLE1 *H-C276D91P2@NC
HOLE9 *H-C276I107D91P2
HOLE17 *H-C276D91P2@NC
HOLE2 *H-C276D91P2@NC

Card Reader Nut

HOLE18 H-TC197BC158D122P2
HOLE37 H-TC197BC158D122P2
Top side

Boundary Hole

HOLE6 *H-TSHAPEBC276D91P2-1@NC
HOLE16 *H-C276D91P2@NC
HOLE25 *H-C276D91P2@NC
HOLE23 *H-C91D91N
HOLE21 *H-C157D91P2
HOLE24 *H-C276D91P2@NC

Boundary Hole (ODD)

HOLE12 *H-C276D91P2@NC

PAD

GP2 *SPAD-SPE1NP
GP3 *SPAD-RE197X217NP
GP1 *RE236X494NP
GP4 *RE270X220NP

HOLE19 O-GC2A-1
HOLE20 O-GC2A-2
HOLE22 *H-TC197BC93D93P2

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Quanta Computer Inc.

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Custom	HOLE & SCREW	1A
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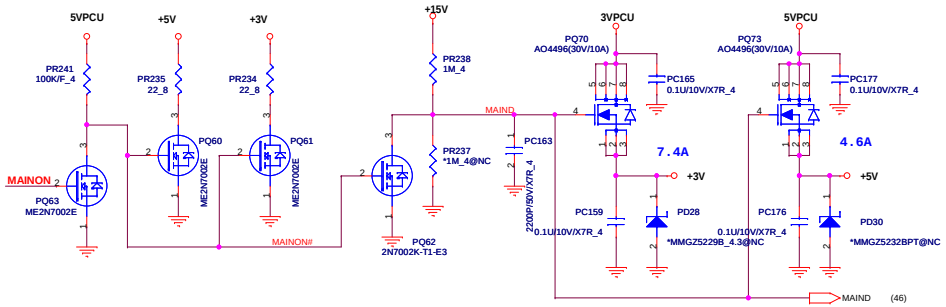
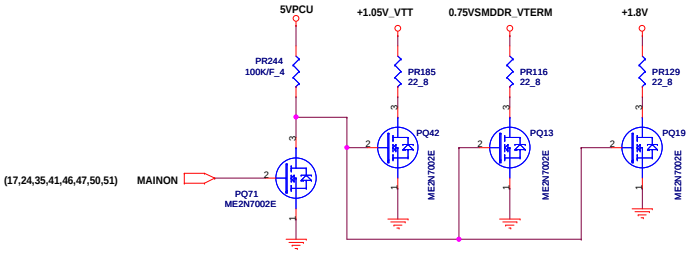
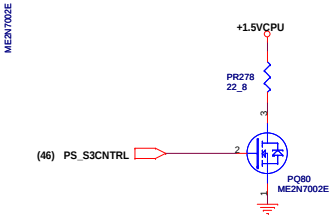
DISCHARGE

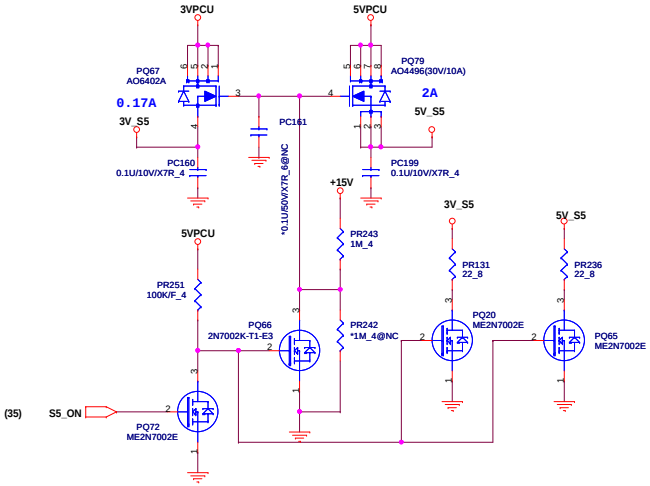
+3.3V, +5V

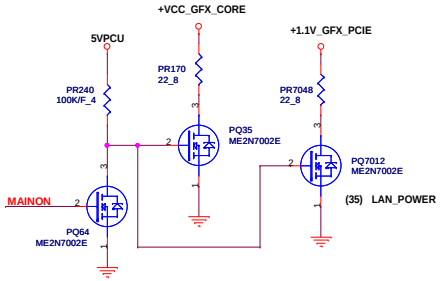




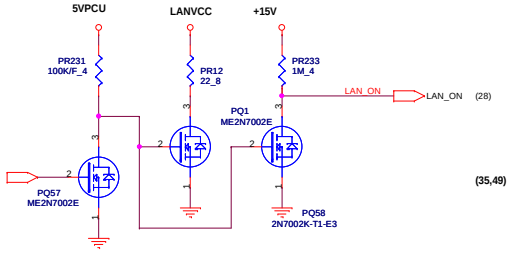


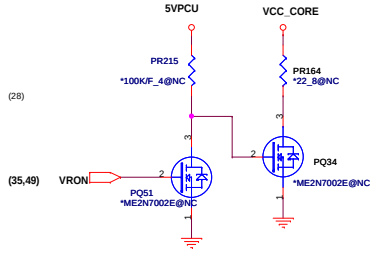
3V_S5, 5V_S5

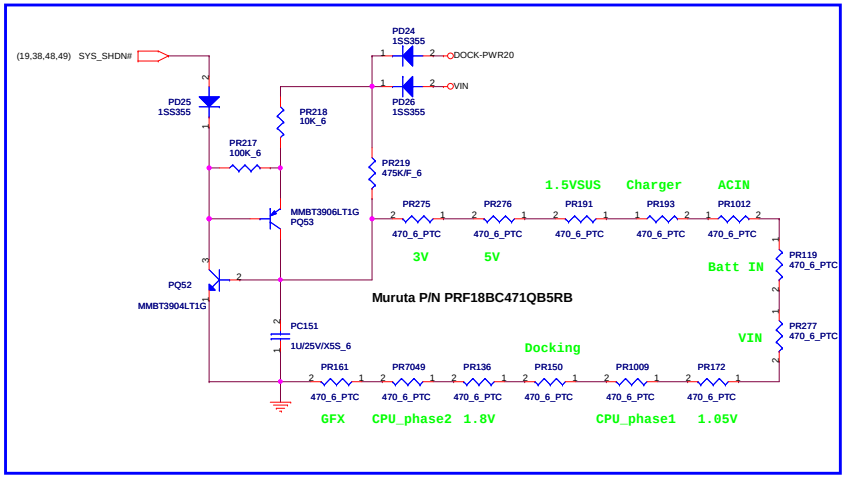




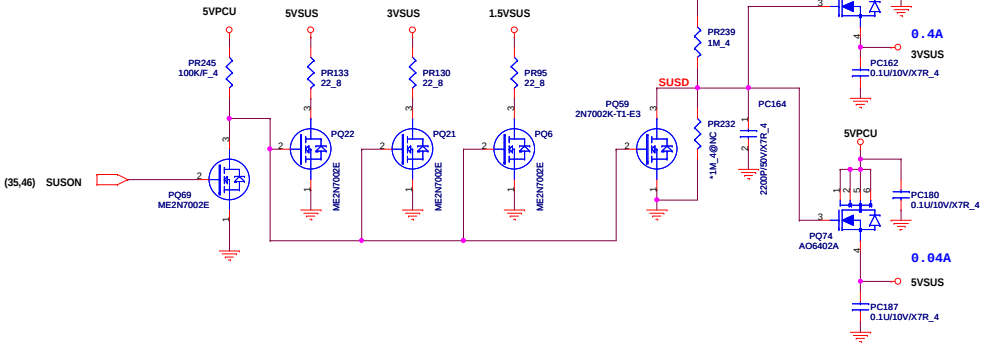
LANVCC

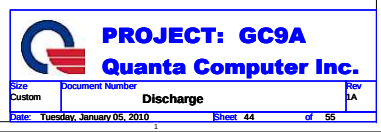


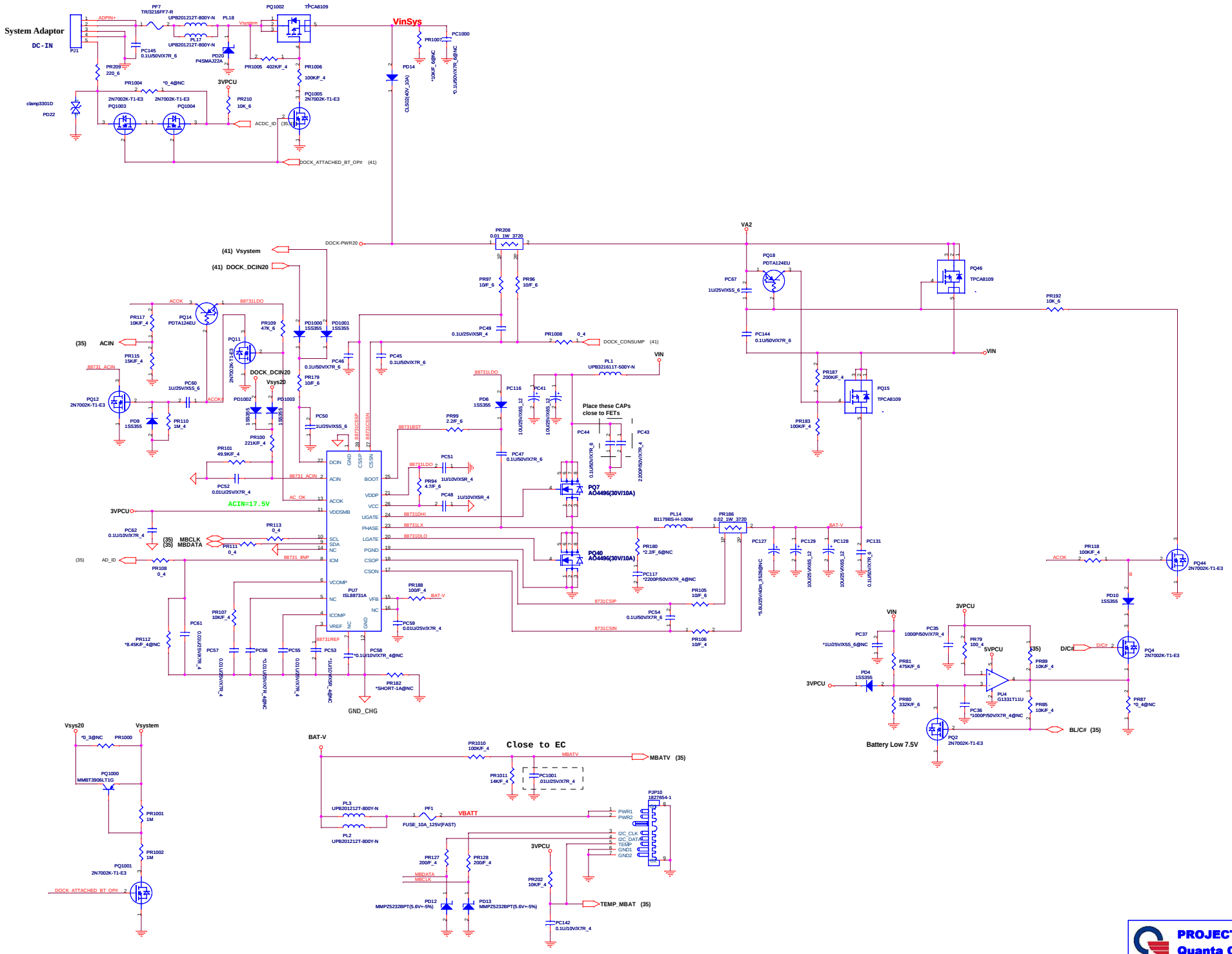


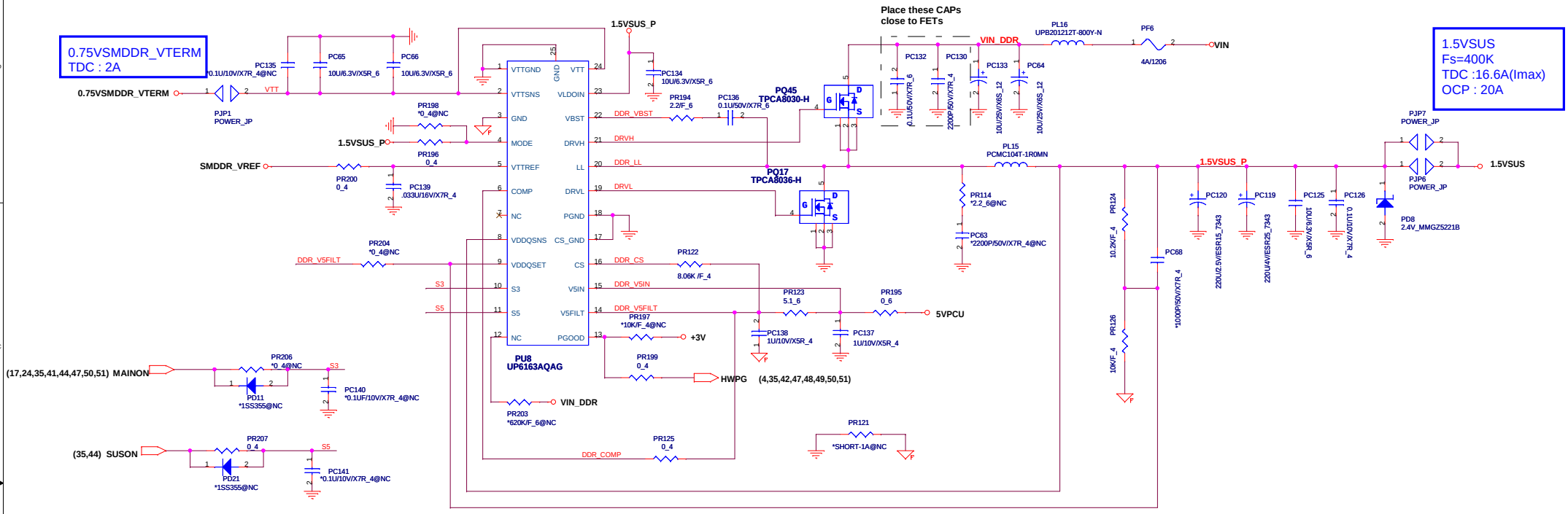


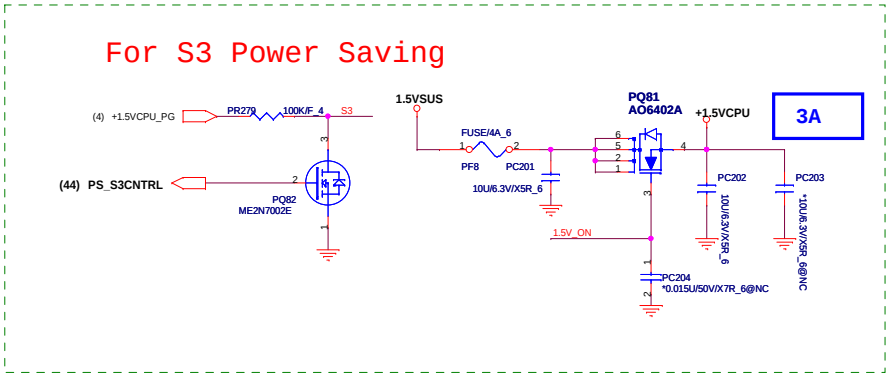
3VSUS, 5VSUS

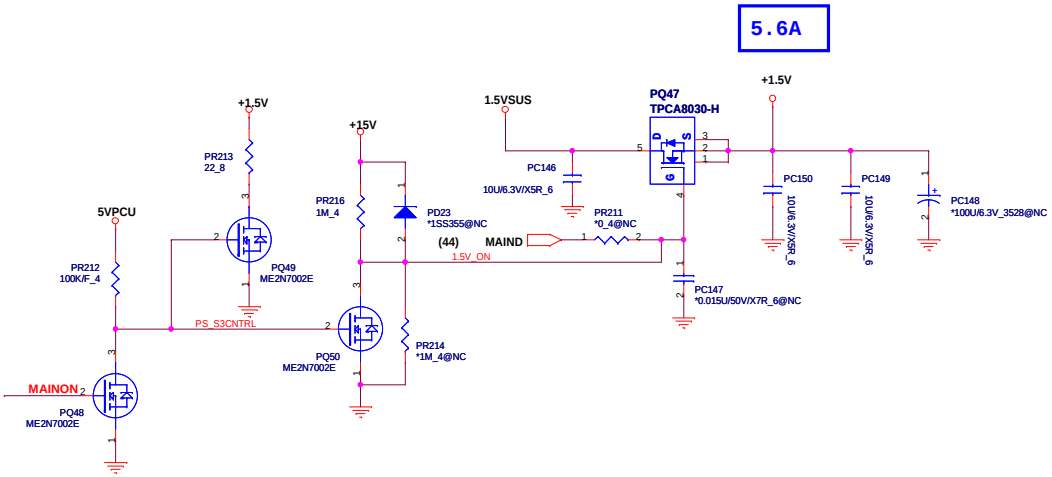





System Adaptor
DC-IN
VinSys
Vsystem
3VPCU
5VPCU
VA2
VIN
Vsys20
DOCK_DCIN20
ACIN=17.5V
Close to EC
Place these CAPs close to FETs
Battery Low 7.5V
GND_CHG
TEMP_MBAT (35)
BL/C# (35)
PROJECT: GC9A
Quanta Computer Inc.
Charger(ISL88731A)
Monday, January 04, 2010
Sheet 45 of 55



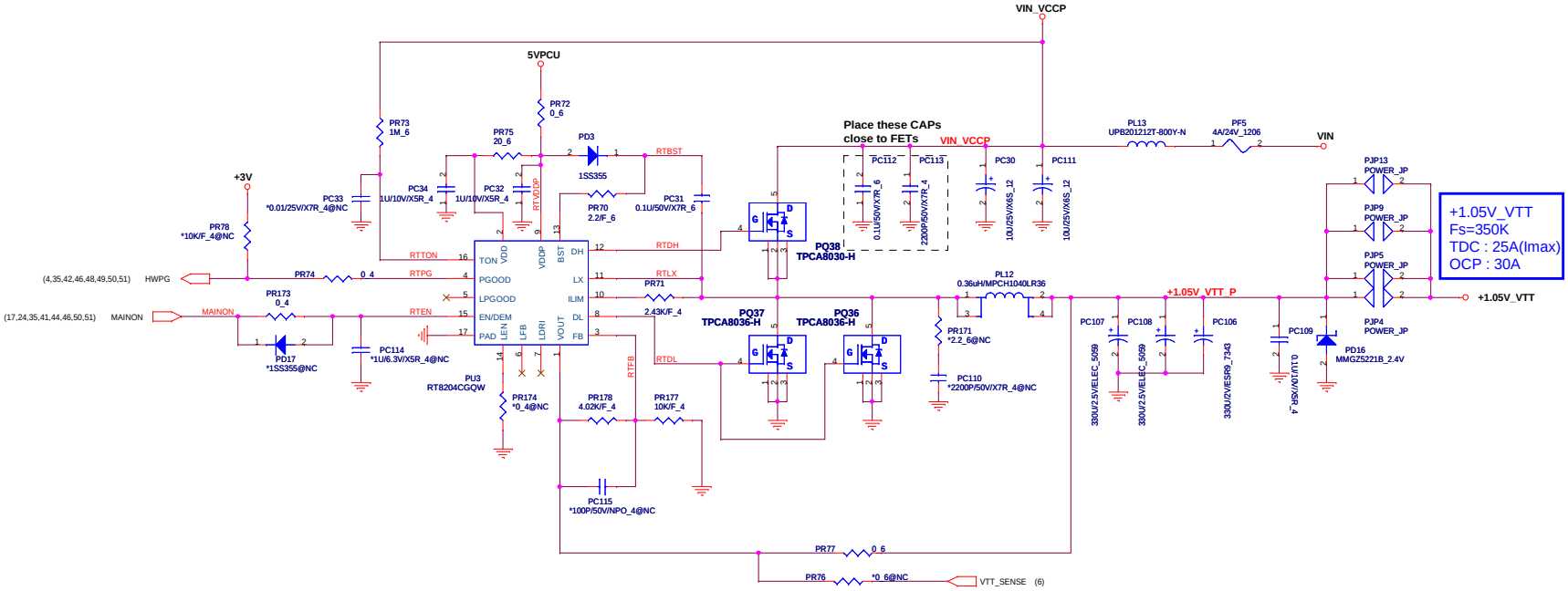




PROJECT: GC9A
Quanta Computer Inc.

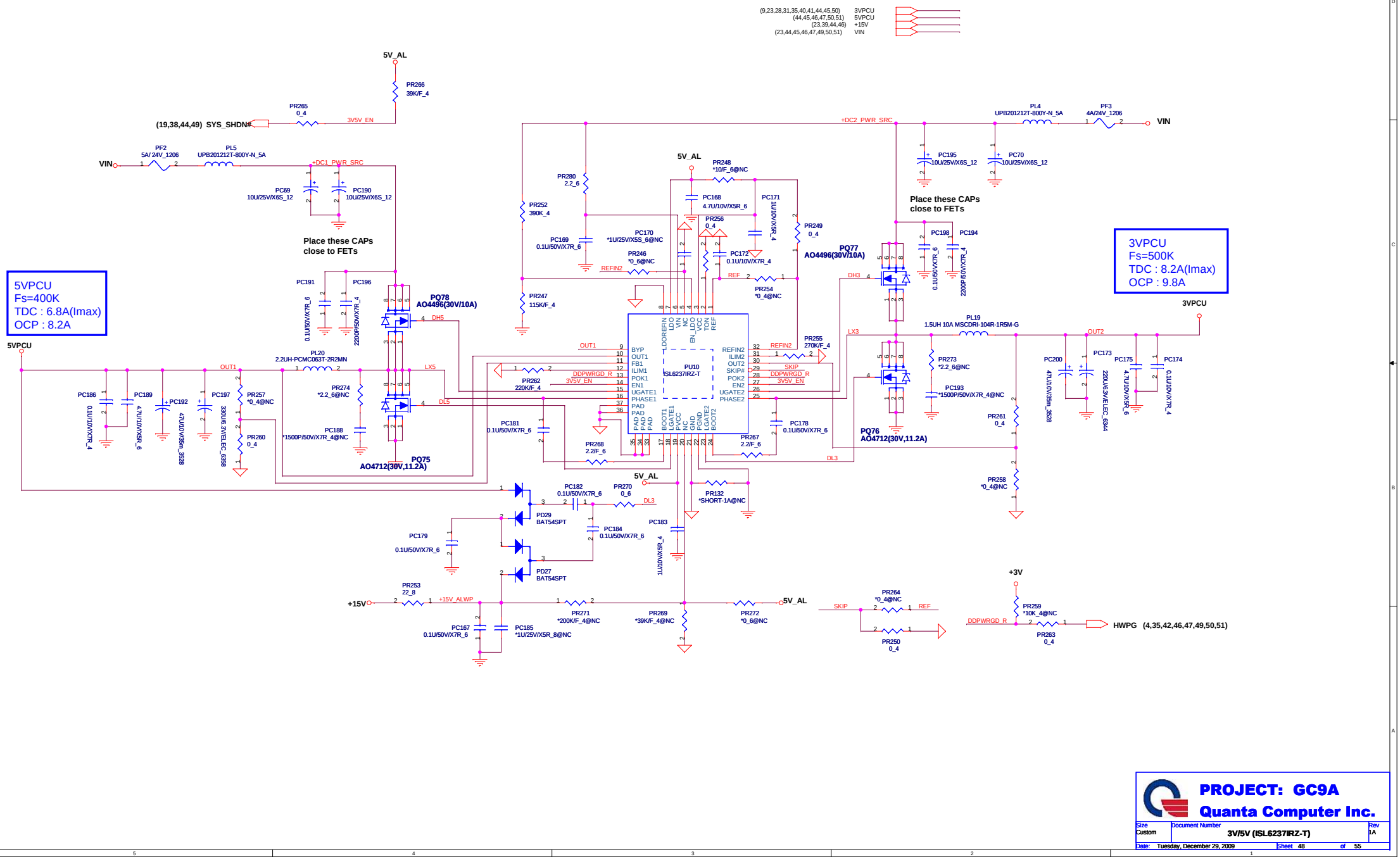
Size	Document Number	Rev
Custom	DDR3/0.75VSMDDR (UP6163AQAG)	1A

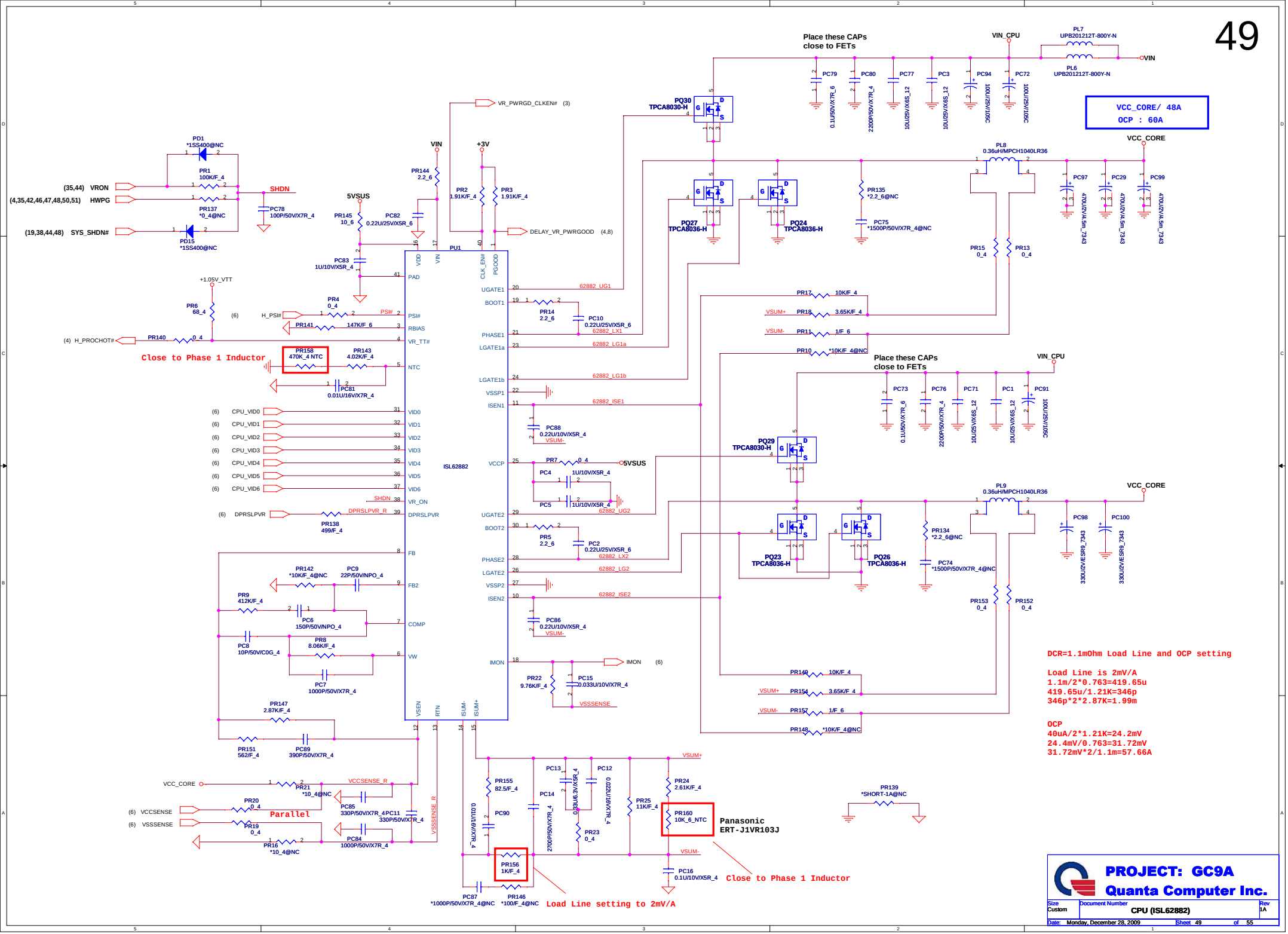
Date: Monday, January 04, 2010 Sheet 46 of 55



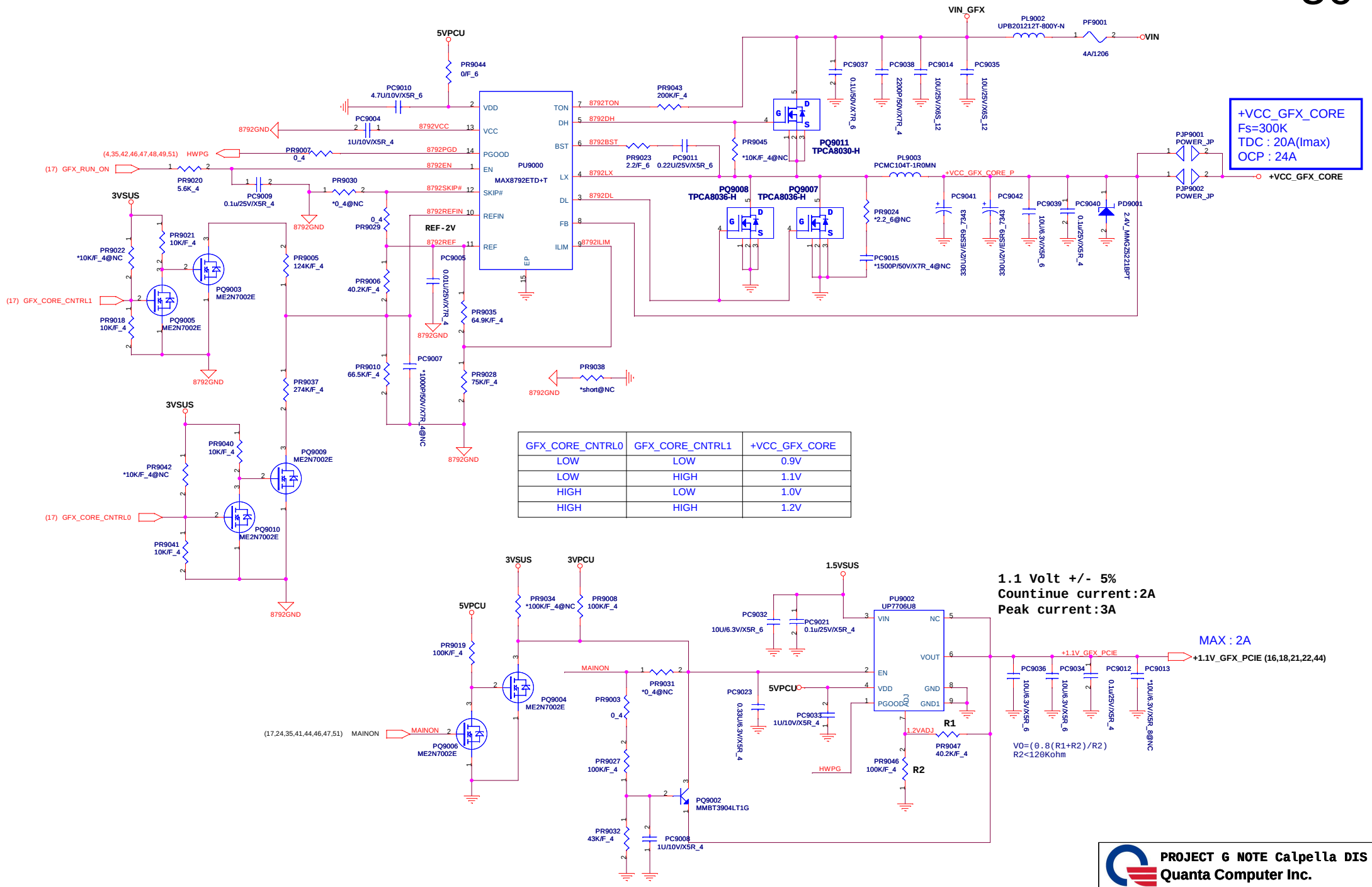
PROJECT: GC9A
Quanta Computer Inc.

Size	Document Number	Rev
C	1.05V_VTT/1.05_PCH (RT8204)	1A
Date: Monday, December 28, 2009	Sheet 47 of 55	


(9,23,28,31,35,40,41,44,45,50) 3VPCU
(44,45,46,47,50,51) 5VPCU
(23,39,44,46) +15V
(23,44,45,46,47,49,50,51) VIN
5V_AL
PR266 39K/F_4
PR265 0_4
(19,38,44,49) SYS_SHDN#
3V5V_EN
VIN
PF2 5A/ 24V_1206
PL5 UPB201212T-800Y-N_5A
+DC1_PWR_SRC
PC69 10U/25V/X6S_12
PC190 10U/25V/X6S_12
Place these CAPs close to FETs
5VPCU
Fs=400K
TDC : 6.8A(Imax)
OCP : 8.2A
PC191 0.1U/50V/X7R_6
PC196 2200P/50V/X7R_4
PQ78 AO4496(30V/10A)
DH5
PL20 2.2UH-PCMC063T-2R2MN
OUT1
LX5
DL5
PC186 0.1U/10V/X7R_4
PC189 4.7U/10V/X5R_6
PC192
PC197 330U/6.3V/ELEC_6558
PR257 *0_4@NC
PR260 0_4
PR274 *2.2_6@NC
PC188 *1500P/50V/X7R_4@NC
PQ75 AO4712(30V,11.2A)
PC181 0.1U/50V/X7R_6
PR268 2.2/F_6
PC182 0.1U/50V/X7R_6
PR270 0_6
DL3
PD29 BAT54SPT
PD27 BAT54SPT
PC179 0.1U/50V/X7R_6
PC184 0.1U/50V/X7R_6
PC183 1U/10V/X5R_4
PR253 22_8
+15V
+15V_ALWP
PC167 0.1U/50V/X7R_6
PC185 *1U/25V/X5R_8@NC
PR271 *200K/F_4@NC
PR269 *39K/F_4@NC
PR272 *0_6@NC
5V_AL
PR132 *SHORT-1A@NC
PR280 2.2_6
PR252 390K_4
PC169 0.1U/50V/X7R_6
PC170 *1U/25V/X5S_6@NC
PR246 *0_6@NC
REFIN2
PR247 115K/F_4
PR248 *10/F_6@NC
PC168 4.7U/10V/X5R_6
PR256 0_4
PC172 0.1U/10V/X7R_4
REF
PR254 *0_4@NC
PC171 10U/10V/X5R_4
PR249 0_4
PU10 ISL6237IRZ-T
LDOREFIN LDO VIN LDO_EN VCC TON REF
BYP OUT1 FB1 ILIM1 POK1 EN1 UGATE1 PHASE1 PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# POK2 EN2 UGATE2 PHASE2
BOOT1 LGATE1 VCC RC GND PGND LGATE2 BOOT2
DDPWRGD_R
PR262 220K/F_4
PR255 270K/F_4
SKIP
PC178 0.1U/50V/X7R_6
PR267 2.2/F_6
PQ77 AO4496(30V/10A)
DH3
PC198 0.1U/50V/X7R_6
PC194 2200P/50V/X7R_4
PQ76 AO4712(30V,11.2A)
LX3
PL19 1.5UH 10A MSCDRI-104R-1R5M-G
PR273 *2.2_6@NC
PC193 *1500P/50V/X7R_4@NC
PR261 0_4
PR258 *0_4@NC
PC195 10U/25V/X6S_12
PC70 10U/25V/X6S_12
PL4 UPB201212T-800Y-N_5A
PF3 4A/24V_1206
+DC2_PWR_SRC
VIN
Place these CAPs close to FETs
3VPCU
Fs=500K
TDC : 8.2A(Imax)
OCP : 9.8A
3VPCU
OUT2
PC200 470U/10V/35m_3528
PC173 220U/6.3V/ELEC_6344
PC175 4.7U/10V/X5R_6
PC174 0.1U/10V/X7R_4
SKIP
PR264 *0_4@NC
REF
PR250 0_4
+3V
PR259 *10K_4@NC
DDPWRGD_R
PR263 0_4
HWPG (4,35,42,46,47,49,50,51)
PROJECT: GC9A
Quanta Computer Inc.
Size Custom
Document Number 3V/5V (ISL6237IRZ-T)
Rev 1A
Date: Tuesday, December 29, 2009
Sheet 48 of 55


Place these CAPs close to FETs
VIN_CPU
VIN
VCC_CORE/ 48A
OCP : 60A
VCC_CORE
Close to Phase 1 Inductor
Parallel
Panasonic ERT-J1VR103J
Load Line setting to 2mV/A
Close to Phase 1 Inductor
ISL62882
DCR=1.1mOhm Load Line and OCP setting
Load Line is 2mV/A
1.1m/2*0.763=419.65u
419.65u/1.21K=346p
346p*2*2.87K=1.99m
OCP
40uA/2*1.21K=24.2mV
24.4mV/0.763=31.72mV
31.72mV*2/1.1m=57.66A
PROJECT: GC9A
Quanta Computer Inc.
CPU (ISL62882)
Monday, December 28, 2009

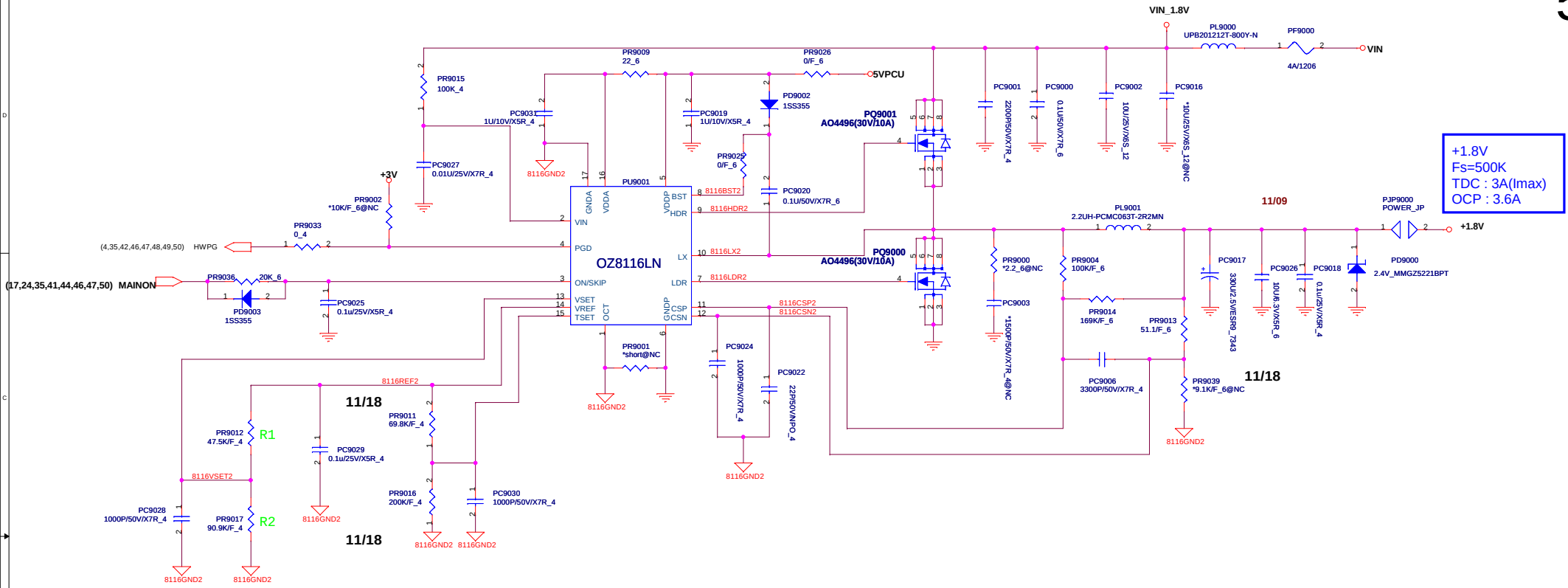
For Descrete M92 VGA Only



GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
LOW	HIGH	1.1V
HIGH	LOW	1.0V
HIGH	HIGH	1.2V

PROJECT G NOTE Calpella DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DIS_GFX_VCC (MAX8792)	1B
Date: Tuesday, December 29, 2009	Sheet 50 of 55	



PROJECT G NOTE Calpella DIS			
Quanta Computer Inc.			
Size: Custom	Document Number: DIS_1.8V_RUN (OZ8116LN)		Rev: 1A
Date: Tuesday, December 29, 2009	Sheet 51 of 55		

Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
1A		DV	Initial release		

Schematic Value Explanation Description :

RESISTOR

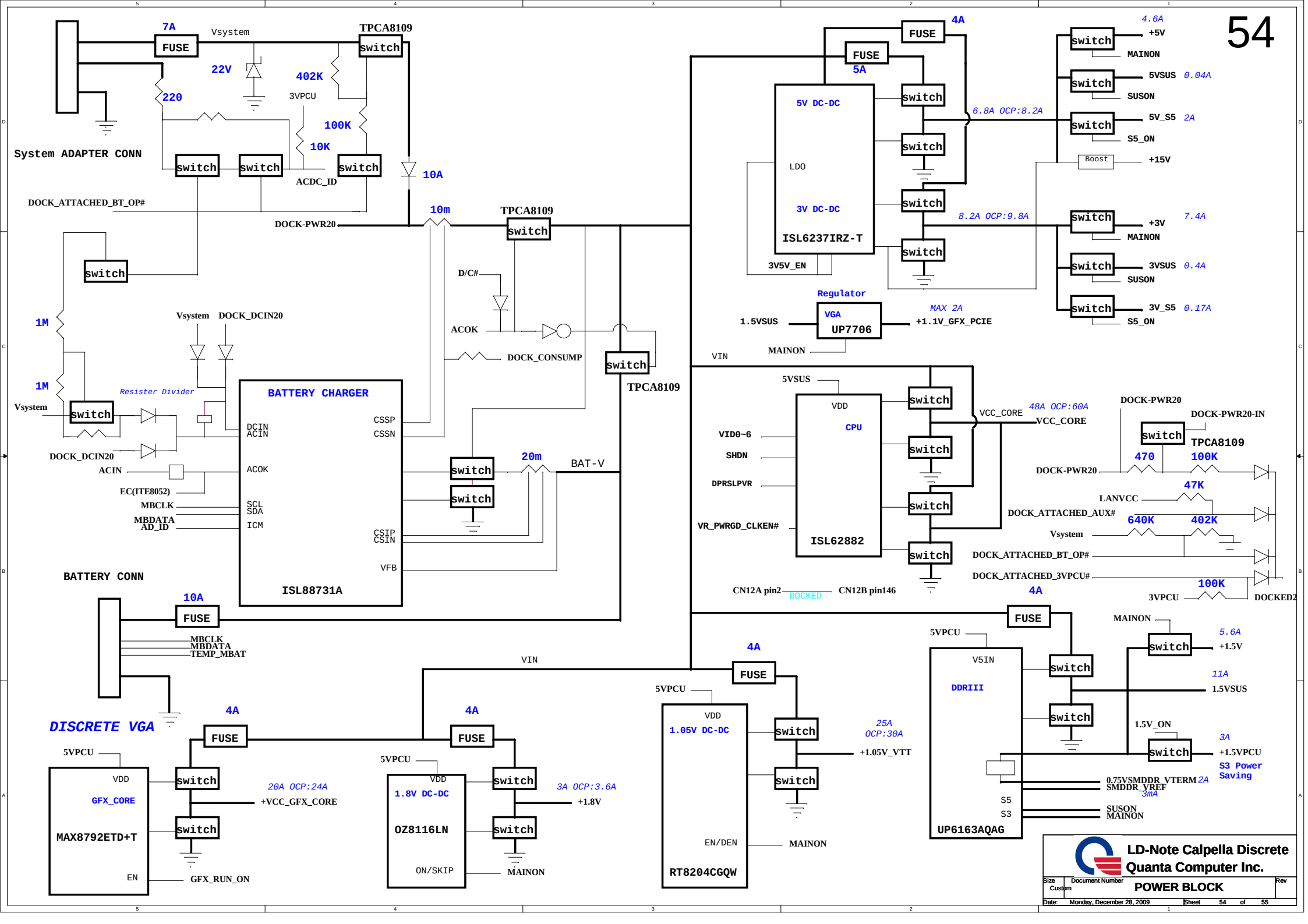
Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP

CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

G NOTE SKU TABLE

Location					



LD-Note Calpella Discrete
Quanta Computer Inc.

Size	Document Number	Rev
Custom	POWER BLOCK	

Date: Monday, December 28, 2009 Sheet 54 of 55

2009

A stage

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-01	30	12/22	R36,R37,R42,R43	Delete R36,R37,R41,R42 (redundant optional resistor) and change connection of E-sata.
EC-A-02	11	12/22	R285	No POP R285 or delete.We have R466 for TPM physical presence
EC-A-03	35	12/22	R101	EC use SPI type
EC-A-04	30	12/22	R623,R625,R626, R627	AUO3 use ext power
EC-A-05	9	12/22	R449,R450	GPIO19,21 should have pull up 10K to +3V due to no internal PU/PD
EC-A-06	39	12/22		Cut LPCPD# signal from TPM#28. due to PCH bug(SUSSTAT# signal chatteringwhen assert)
EC-A-07	35	12/23	R262,C382	Add Pull high for CARE_BUTTON#
EC-A-08	40	12/23	R79,R80,R81, R82,R83,R86, R104,R105,R108	Delete these resistor to save space for layout.
EC-A-09	24	12/28	C2350,C196	Change CAP value per customer request.
EC-A-10	03	12/28	C8222,C8223	Add decoupling cap per RF engineer requested.
EC-A-11	26	12/29	C683	De-pop C683 to prevent efect high frequency of THD+N.

ERROR: syntaxerror
OFFENDING COMMAND: --nostringval--

STACK:

/Title
()
/Subject
(D:20100106114247+08’00’)
/ModDate
()
/Keywords
(PDFCreator Version 0.9.5)
/Creator
(D:20100106114247+08’00’)
/CreationDate
(93121305)
/Author
-mark-