

COMPAL CONFIDENTIAL

MODEL NAME : NAL60  
PCB NO : LA-5691P ( DAA00001K00 )  
BOM P/N : 43178731L01/43178731L02

M10 Lafite  
BGA Arrandale (34 x 28 mm) +  
SFF IBEXPEAK-M

2009-07-07  
REV : 0.1(X00)

@ : Nopop Component

MB Type	BOM P/N	CPU	With BLT	Non BLT	TCM		TPM		BOM CONFIG
			1@	2@	W(3@)	W/O(4@)	W(5@)	W/O(6@)	
BLT EN,TPM EN	43178731L01	SV 2.4G	*			*	*		1@, 4@, 5@
BLT EN,TPM EN	43178731L02	SV 2.0G	*		*			*	1@, 3@, 6@
BLT DIS,TCM EN	43178731L03	LV 1.8G		*		*	*		2@, 4@, 5@

MB PCB	
Part Number	Description
DAA00001K00	PCB QAW LA-5691P REV0 M/B

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Title

Cover Sheet

Size

Document Number

LA-5691P

Rev

0.1

Date

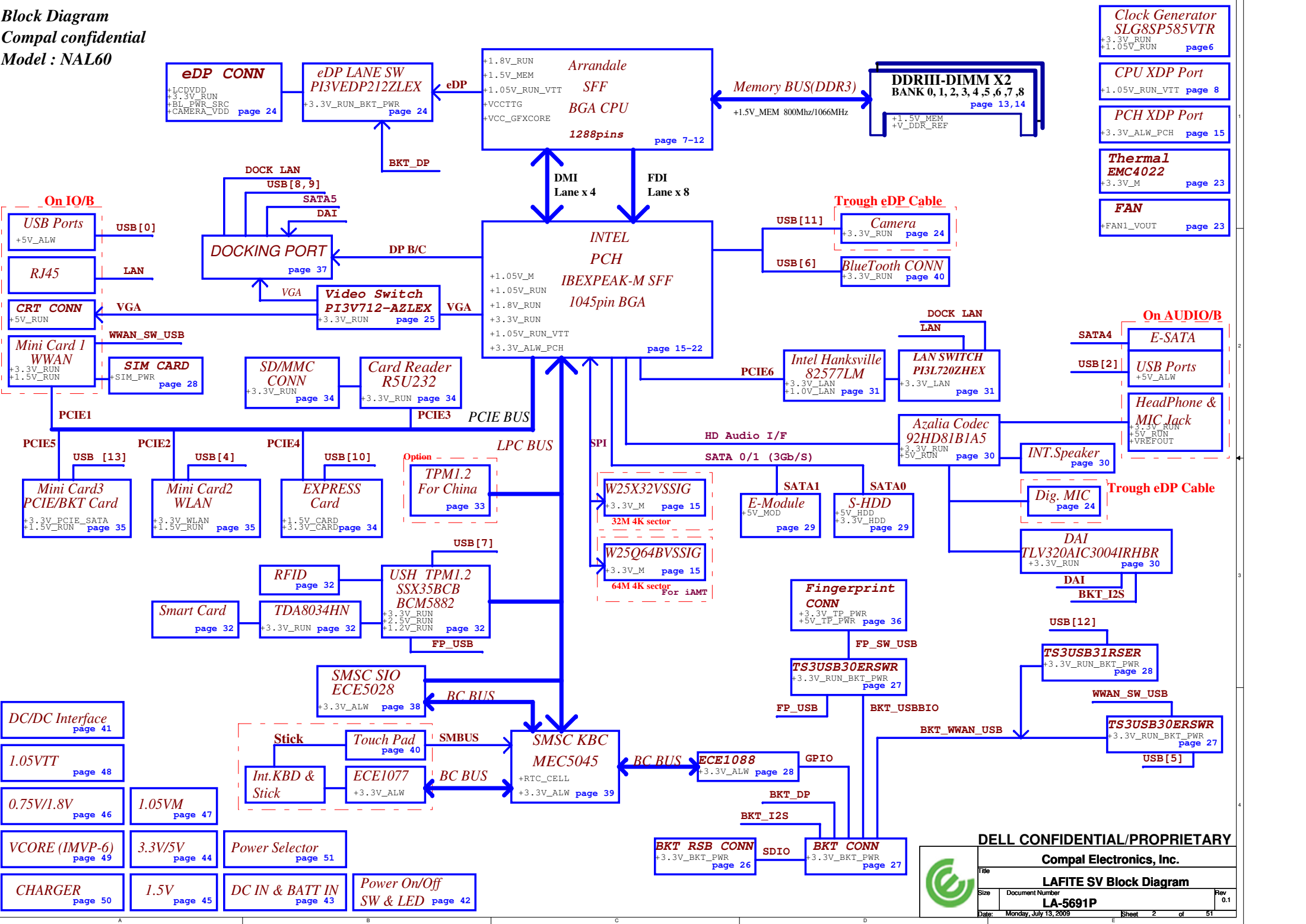
Monday, July 13, 2009

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## POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	ON
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

## PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	USB Port (Ext Right Side)
	1	NA
	2	USB Port (Ext Left Side )
	3	NA
	4	WLAN
	5	WWAN
	6	Bloetooth
	7	USB->BIO
	8	DOCKING
	9	DOCKING
	10	Express Card
	11	Camera
	12	BKT
	13	WPAN/NVMHCI

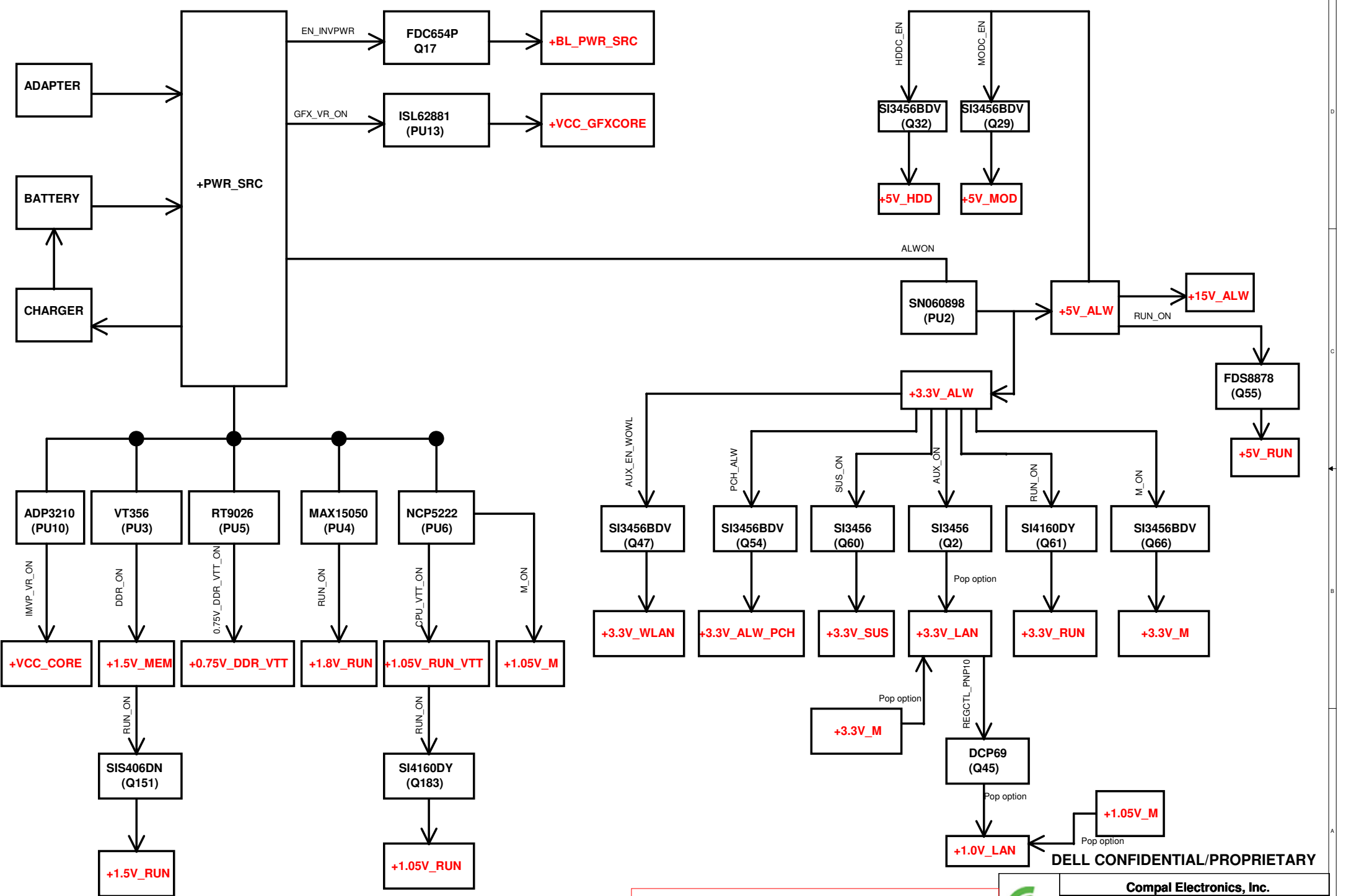
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Card Reader
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 WPAN/NVMHCI
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None

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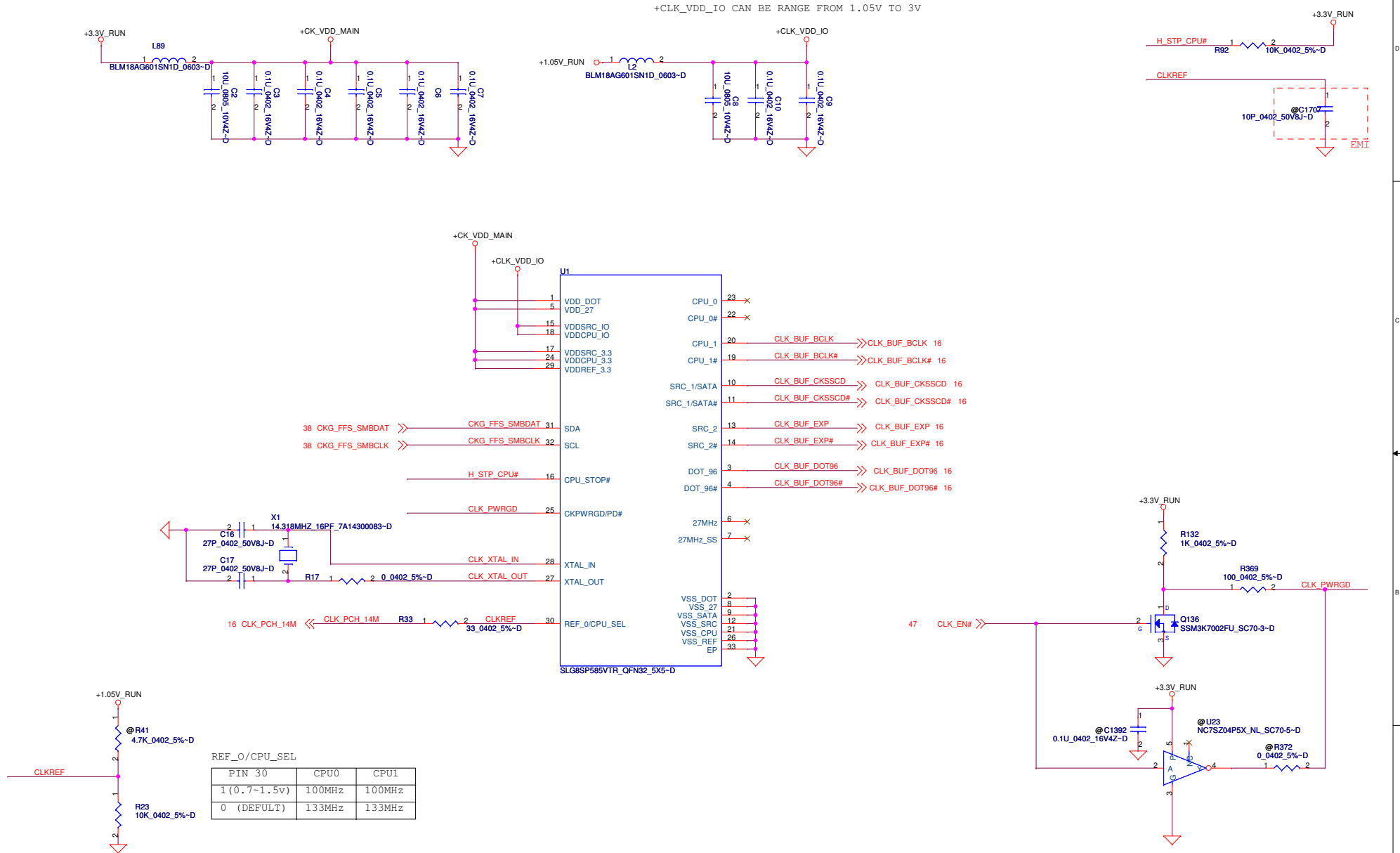
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Title <b>Power Rail</b>		
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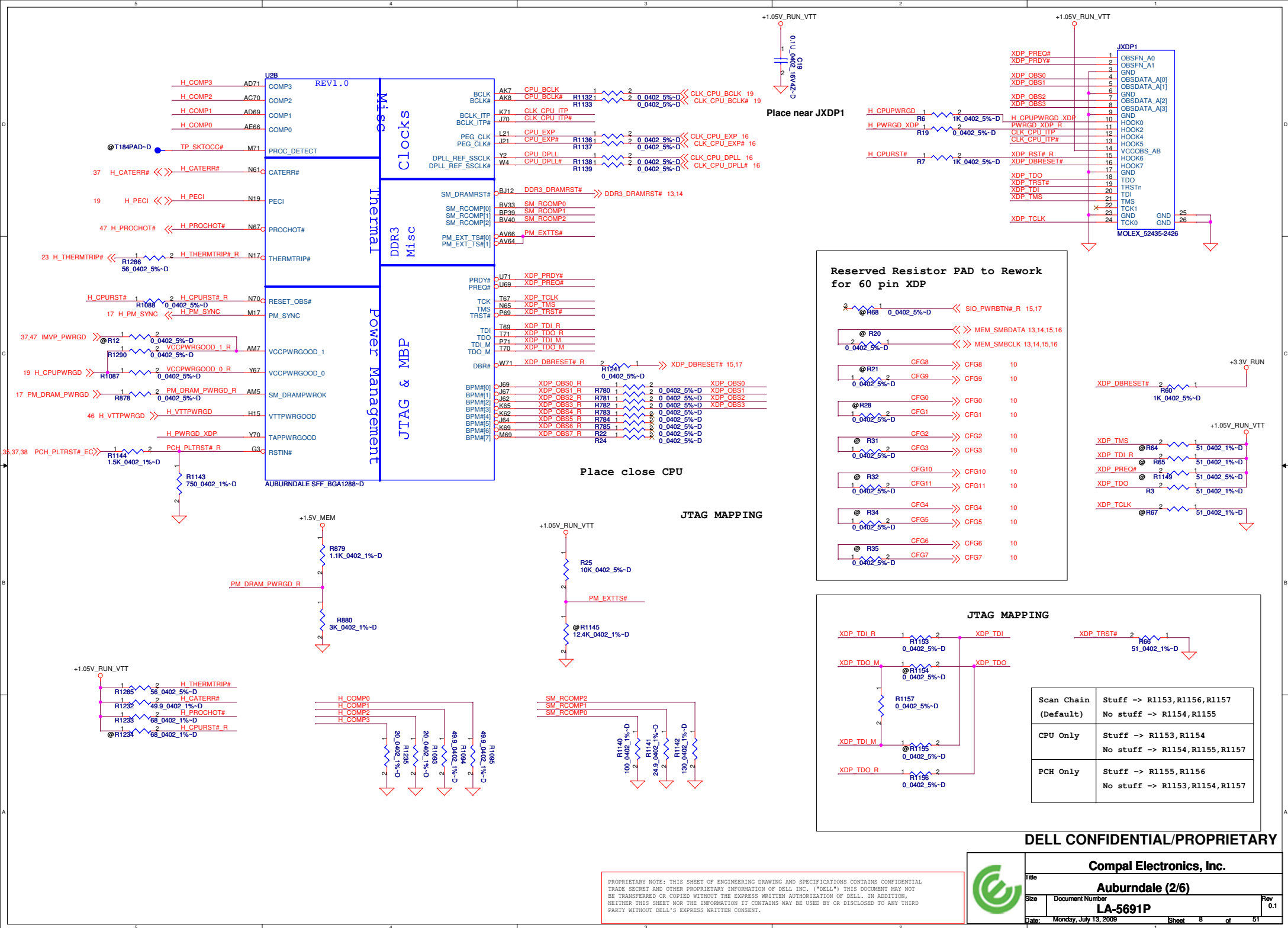


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Title			
Clock Generator			
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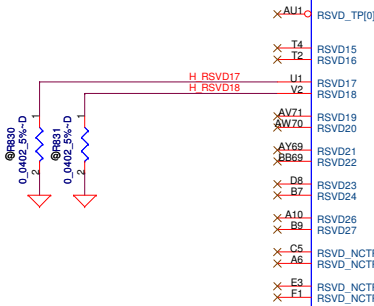








Reserve VIA on PCB



AUBURNDAL SFF\_BGA1288-D

RESERVED

#### Package Daisy Chain:

- 1: BR71 - pkg - BT71- board - BT69 - pkg - BV71 - board - BV69 - pkg - BV68
- 2: A68 - pkg - A69 - board - C69 - pkg - A71 - board - C71 - pkg - E71
- 3: A5 - pkg - C3
- 4: BR1 - pkg - BT1 - board - BV1 - pkg - BT3 - board - BV3 - pkg - BV5

PCI-Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enable

PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Number Reversed 15->0, 14->1 ...

Display Port Presence	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

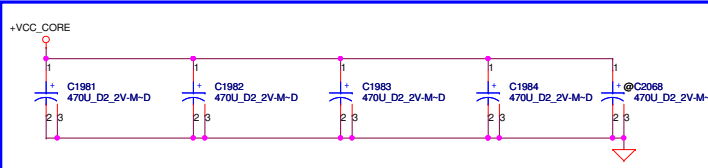
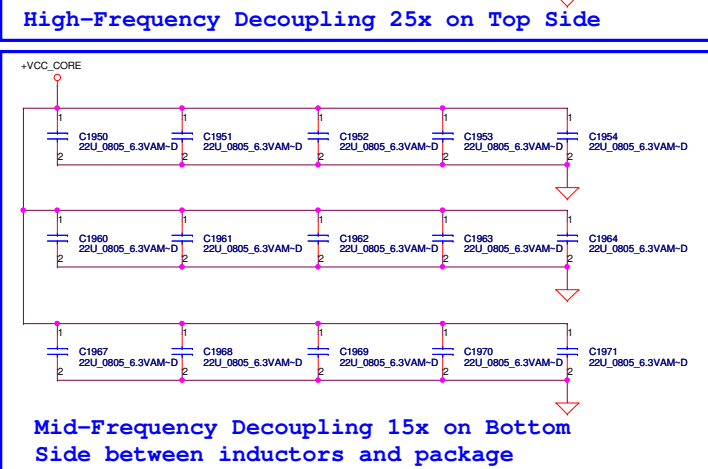
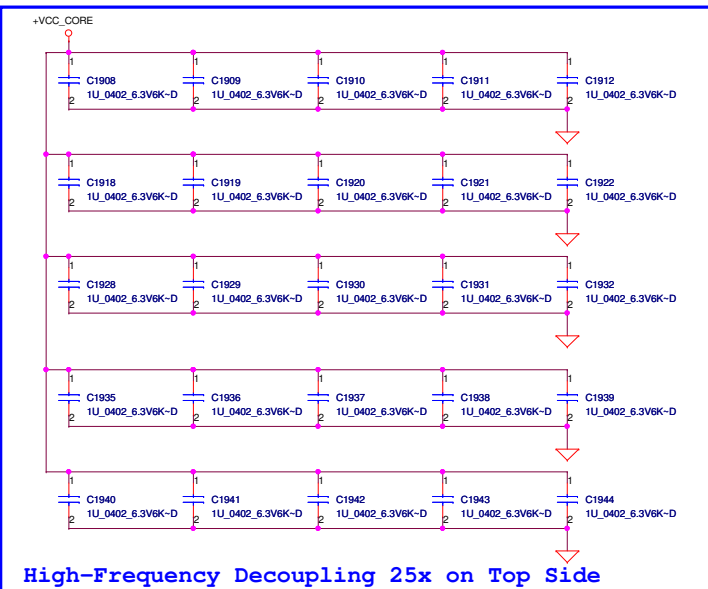
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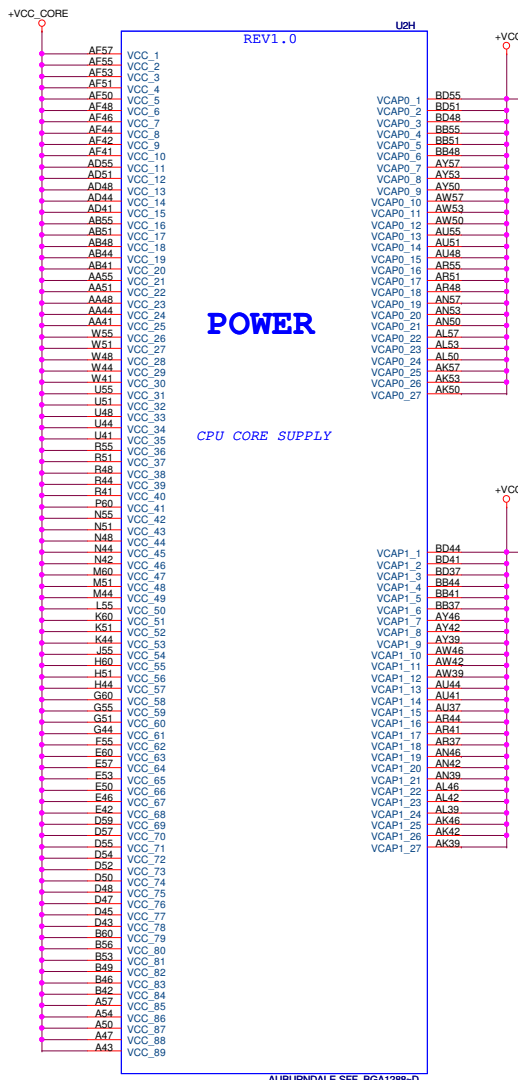
Auburndale (4/6)

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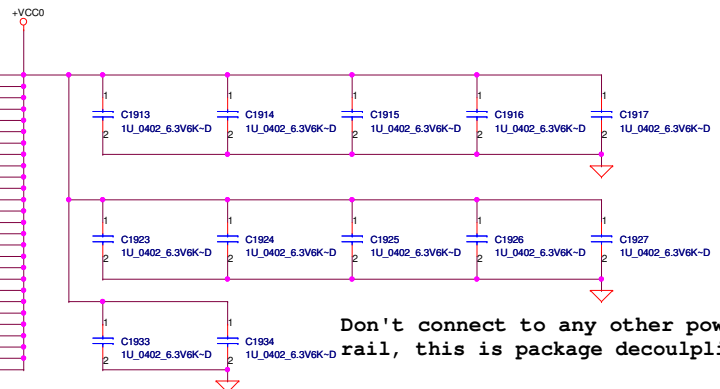
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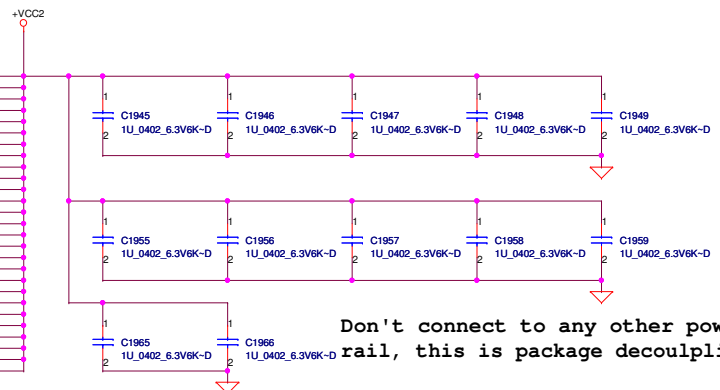
## POWER

CPU CORE SUPPLY

AUBURNDALD SFF\_BGA1288-D



Don't connect to any other power rail, this is package decoupling



Don't connect to any other power rail, this is package decoupling

PROCESSOR Power Rail Table (EDS V1.0)		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VXNG	1.5	22
VccPLL	1.8	1.35
VCORE	0.75	48
VDDR	1.5	3
VTT	1.05	18

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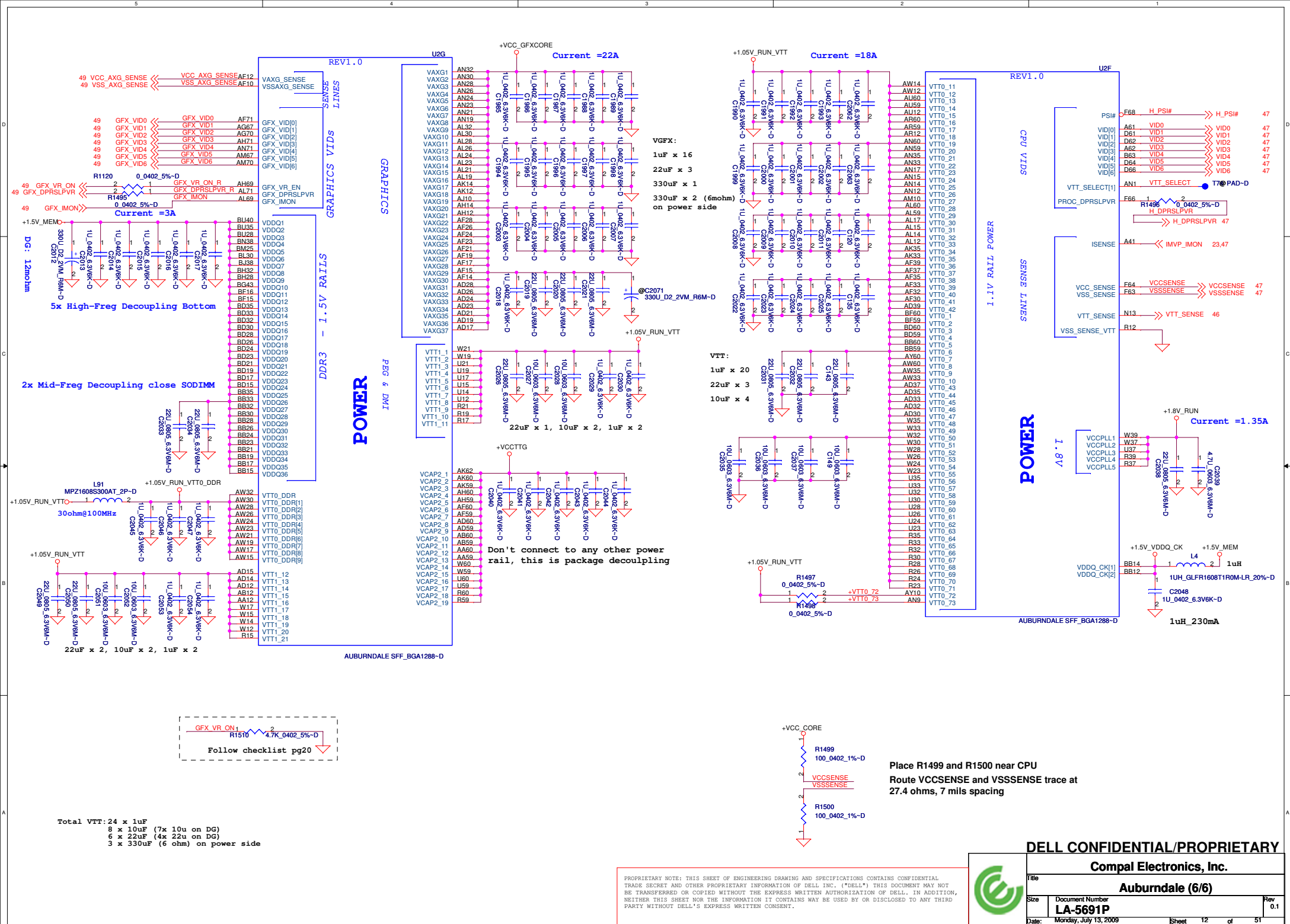
Auburndale (5/6)

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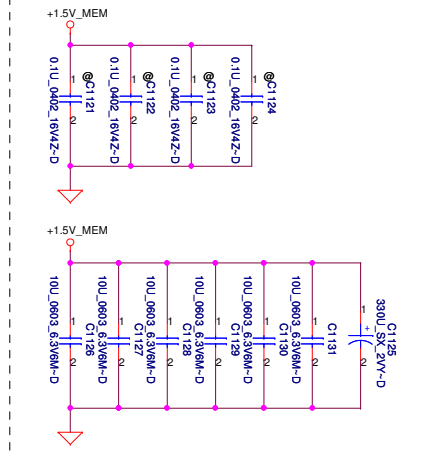
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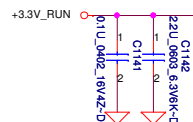
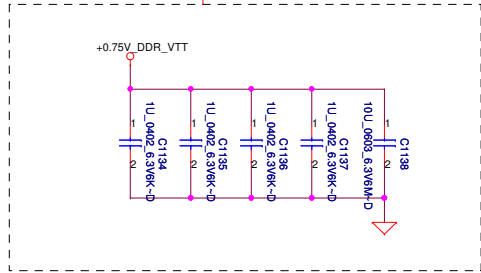
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 9 DDR\_A\_D[0..63] <<>>  
 9 DDR\_A\_DM[0..7] <<>>  
 9 DDR\_A\_DQS[0..7] <<>>  
 9 DDR\_A\_MA[0..15] <<>>

Populate R87 for Intel DDR3  
 VREFDQ multiple methods M1

Layout Note:  
 Place near JDIMMA



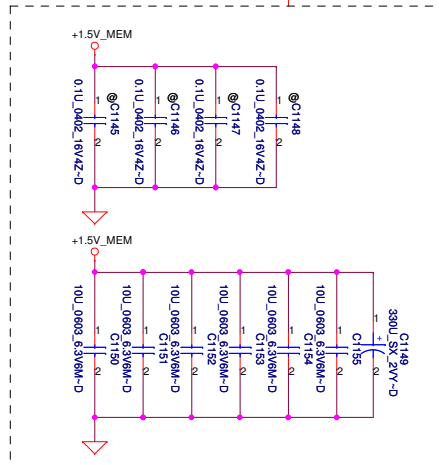
Layout Note:  
 Place near JDIMMA.203,204



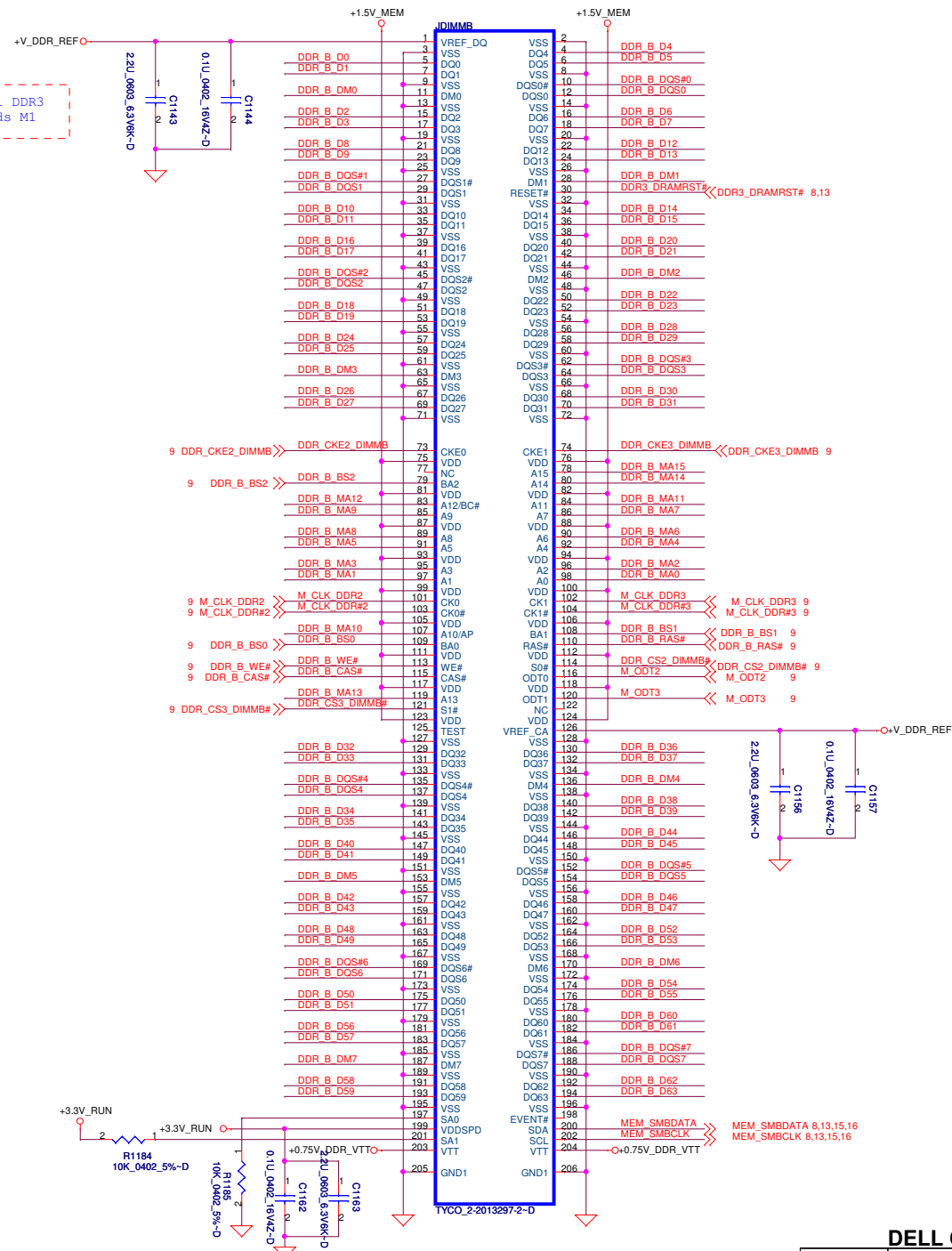
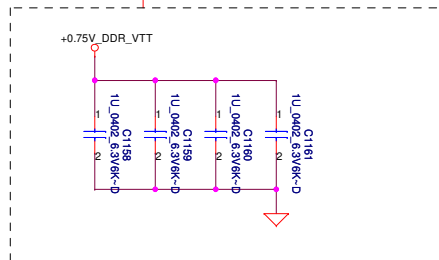
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 9 DDR\_B\_D[0..63] <<>>  
 9 DDR\_B\_DM[0..7] <<>>  
 9 DDR\_B\_DQS#[0..7] <<>>  
 9 DDR\_B\_MA[0..15] <<>>

Populate R88 for Intel DDR3  
 VREFDQ multiple methods M1

Layout Note:  
 Place near JDIMMB



Layout Note:  
 Place near JDIMMB.203,204



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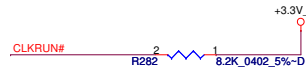
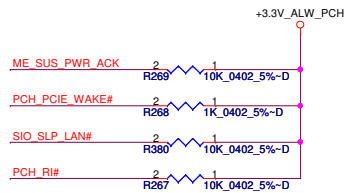
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Title			
DDR3II-SODIMM SLOT2			
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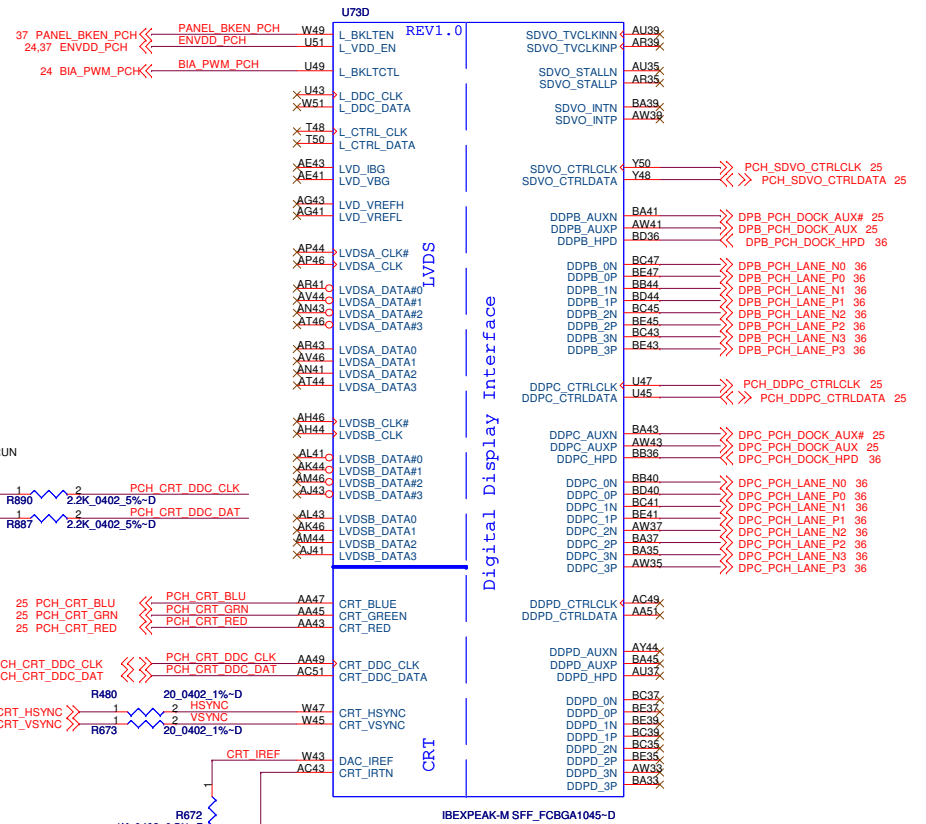
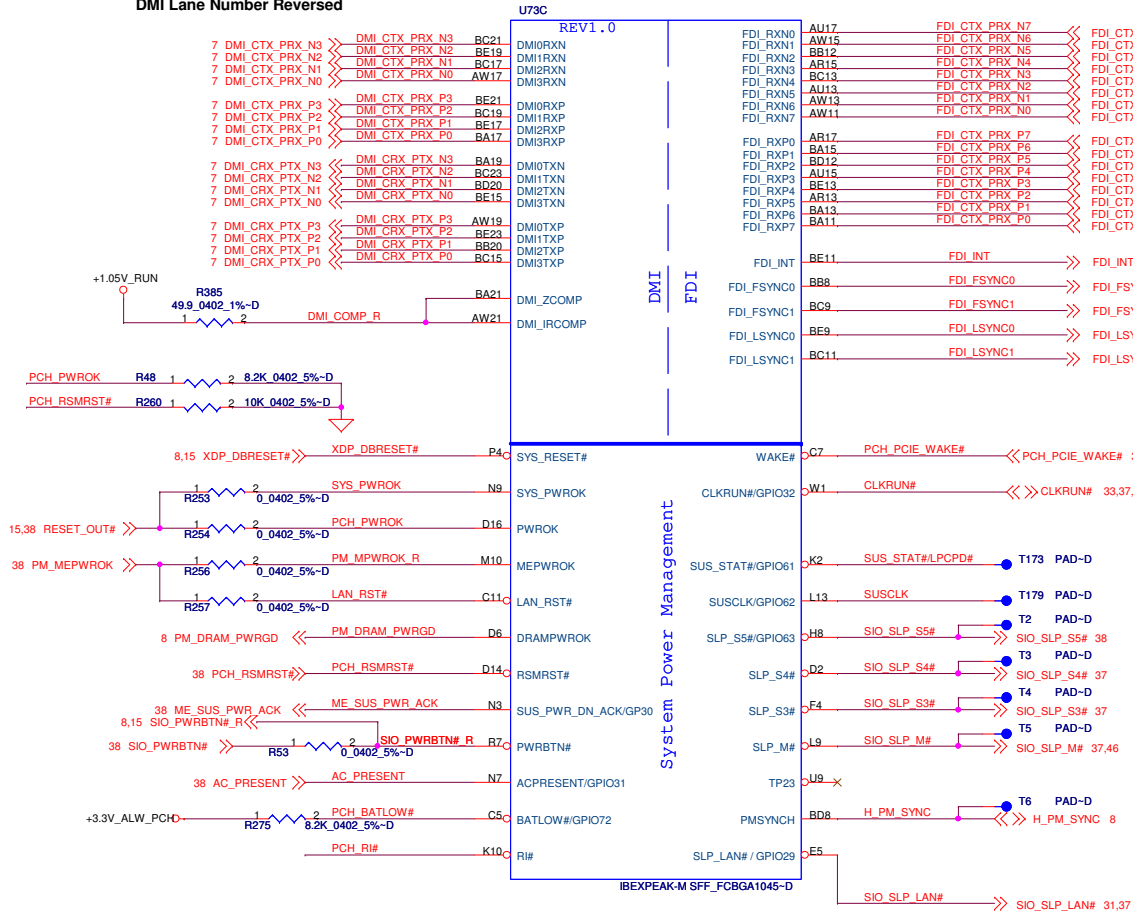






### DMI Lane Number Reversed

### FDI Lane Number Reversed

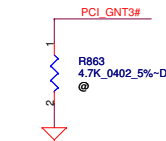
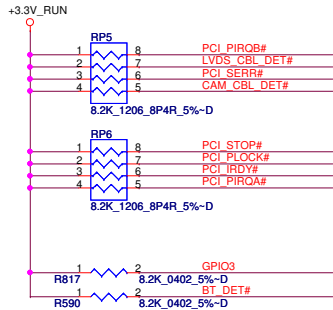
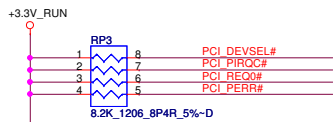


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A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

29,38 HDD\_FALL\_INT1

24 CAM\_CBL\_DET#

35 PCIE\_MCARD3\_DET#

24 LVDS\_CBL\_DET#

24 CAM\_CBL\_DET#

FFS\_PCH\_INT

PCH\_PCIRST#

PCI\_SERR#

PCI\_PERR#

PCI\_IRDY#

PCI\_DEVSEL#

PCI\_FRAME#

PCI\_PLOCK#

PCI\_STOP#

PCI\_TRDY#

PME#

PLTRST#

CLK\_PIO59

CLK\_PIO40

CLK\_PIO41

CLK\_PIO42

CLK\_PIO43

CLK\_PIO44

CLK\_PIO45

CLK\_PIO46

CLK\_PIO47

CLK\_PIO48

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CLK\_PIO223

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CLK\_PIO225

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CLK\_PIO254

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CLK\_PIO256

CLK\_PIO257

CLK\_PIO258

CLK\_PIO259

CLK\_PIO260

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CLK\_PIO262

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CLK\_PIO273

CLK\_PIO274

CLK\_PIO275

CLK\_PIO276

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CLK\_PIO284

CLK\_PIO285

CLK\_PIO286

CLK\_PIO287

CLK\_PIO288

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CLK\_PIO293

CLK\_PIO294

CLK\_PIO295

CLK\_PIO296

CLK\_PIO297

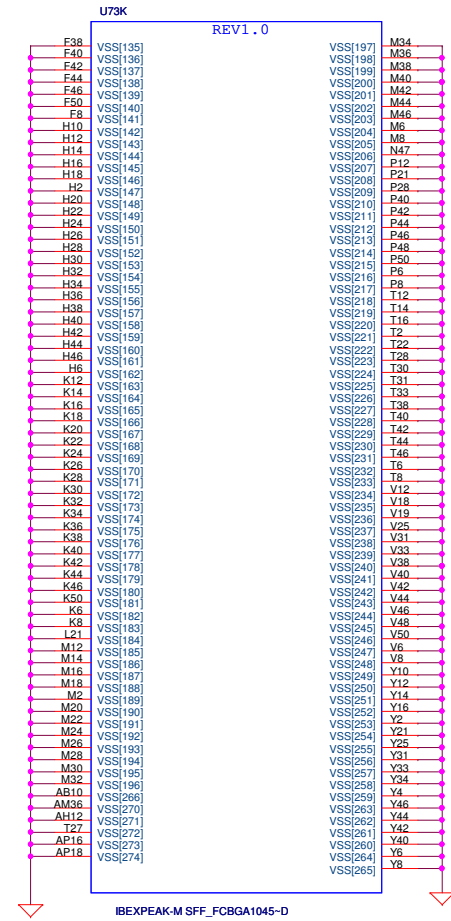
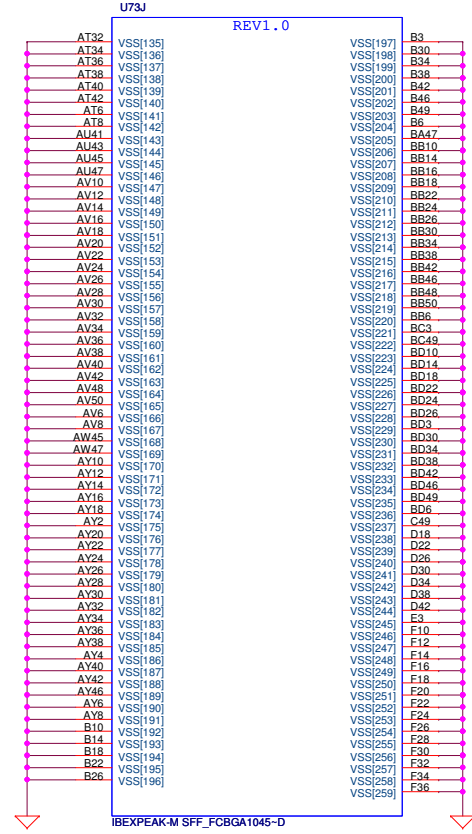
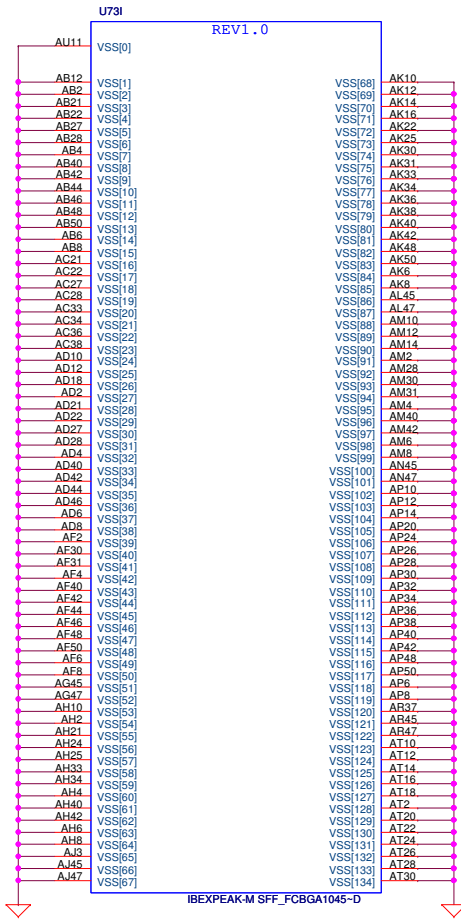
CLK\_PIO298

CLK\_PIO299



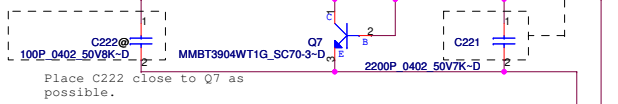
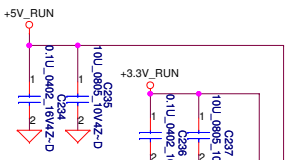
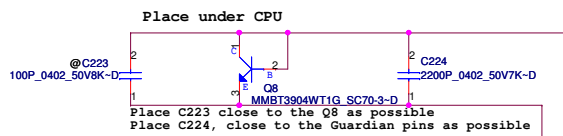
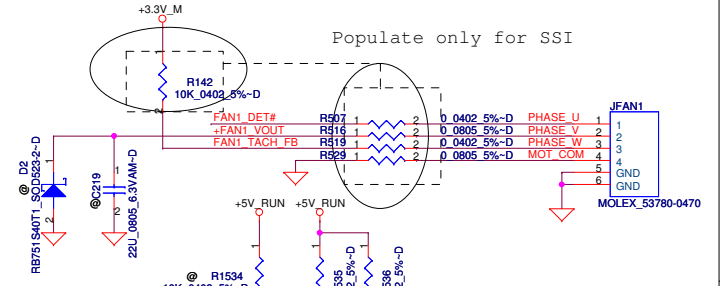
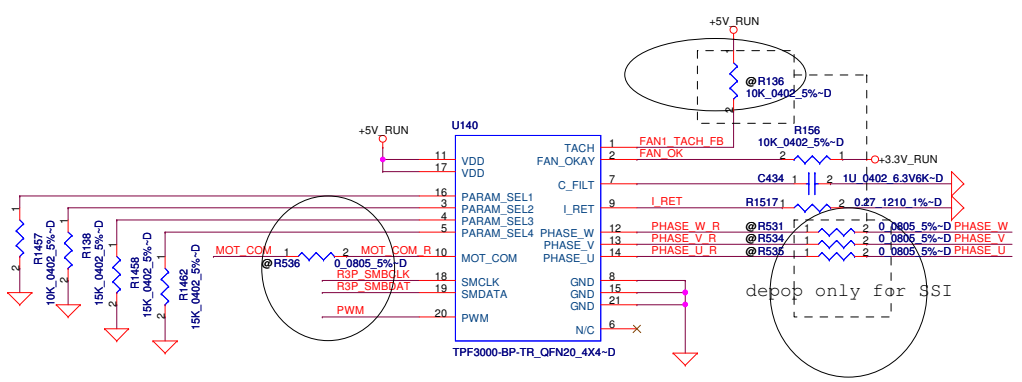
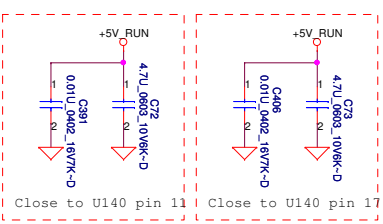






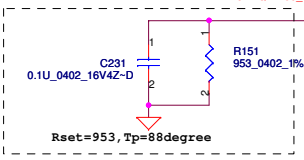
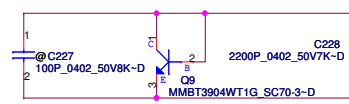
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PCH (8/8)			
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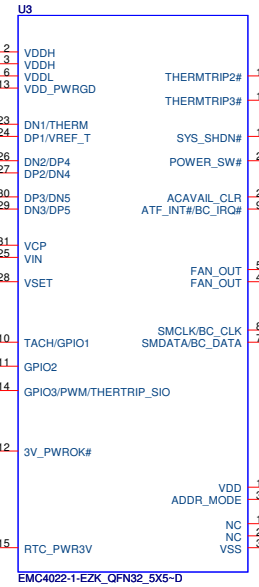
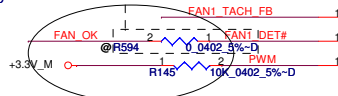


Q9 Place near DIMM

Place C227 close to Q9



Depop for M09 Fan Solution

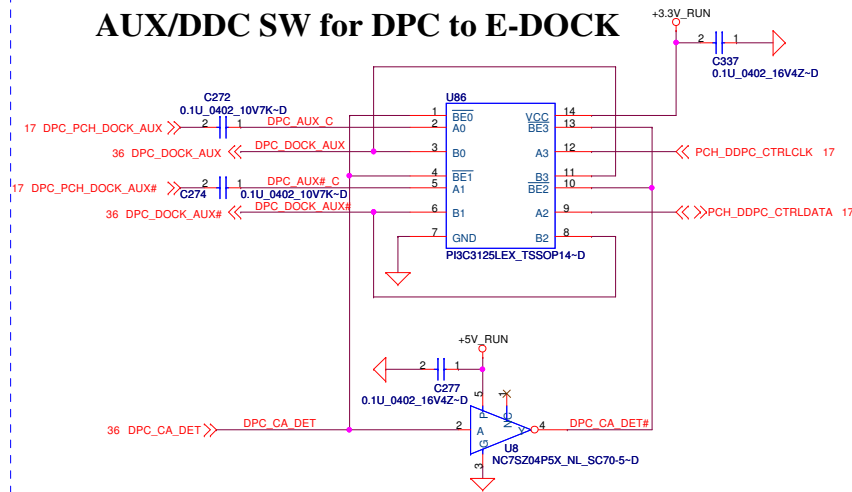




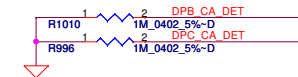
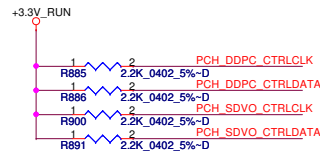
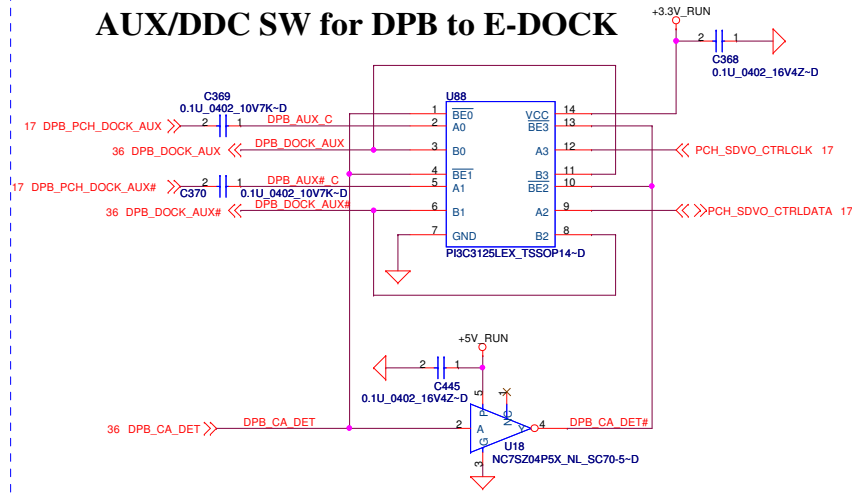




## AUX/DDC SW for DPC to E-DOCK



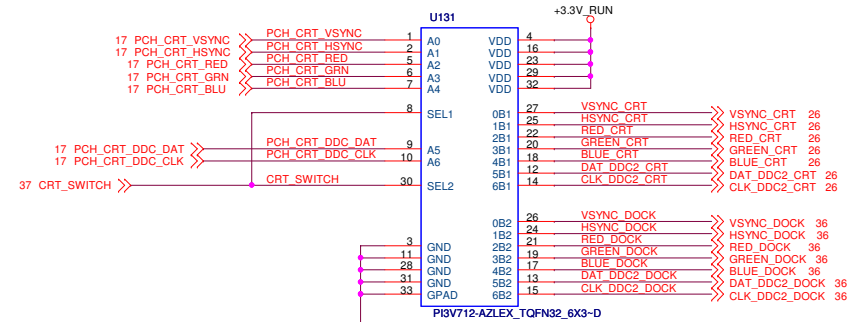
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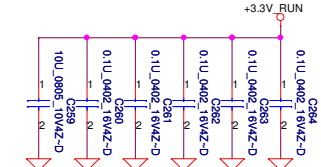
Intel WW18 Strapping option

Intel WW18 Strapping option

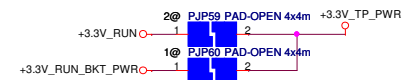
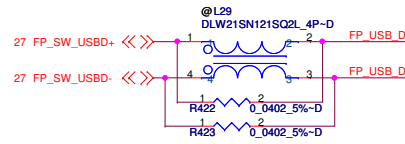
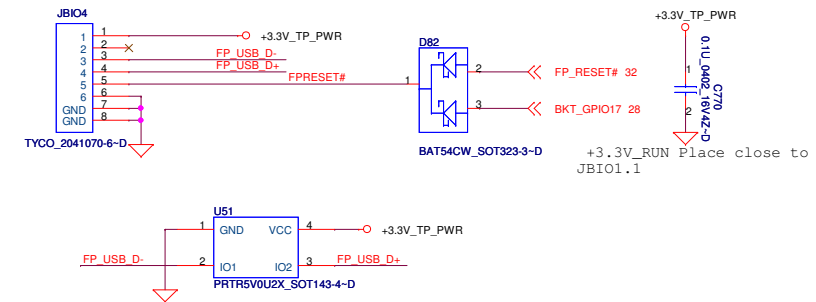
## VGA SW for MB/DOCK



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



## Fingerprint CONN.



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Title			
DPC DPD SW for DOCK			
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Three circuit diagrams are shown, each representing a different power supply pin:

- +VREFOUT:** A capacitor labeled C2055 is connected between the +VREFOUT pin (terminal 1) and ground (terminal 2). The capacitor value is 0.1u\_0402\_16V4Z-D.
- +5V\_RUN:** A capacitor labeled C2056 is connected between the +5V\_RUN pin (terminal 1) and ground (terminal 2). The capacitor value is 0.1u\_0402\_16V4Z-D.
- +5V\_ALW:** A capacitor labeled C2057 is connected between the +5V\_ALW pin (terminal 1) and ground (terminal 2). The capacitor value is 0.1u\_0402\_16V4Z-D.

Pinout diagram for the Molex 48210-3011-D connector. The diagram shows the connection between the connector pins and the board signals. The connector has 30 pins, numbered 1 to 30. The board signals are listed on the left and right sides of the diagram. The connections are as follows:

Connector Pin	Board Signal
1	ESATA_USB_PWR_EN#
2	EXT_MONO_MIC
3	USB_OC1#
4	AUD_HP_OUT_L
5	AUD_HP_OUT_R
6	AUD_MIC_SWITCH
7	AUD_HP_NB_SENSE
8	AUD_NB_MUTE
9	ESATA_PTX_DRX_N4_C
10	AUD_NB_MUTE
11	ESATA_PTX_DRX_P4_C
12	AUD_NB_MUTE
13	ESATA_PTX_DRX_N4_C
14	AUD_NB_MUTE
15	ESATA_PTX_DRX_P4_C
16	AUD_NB_MUTE
17	ESATA_PTX_DRX_N4_C
18	AUD_NB_MUTE
19	ESATA_PTX_DRX_P4_C
20	AUD_NB_MUTE
21	ESATA_PTX_DRX_N4_C
22	AUD_NB_MUTE
23	ESATA_PTX_DRX_P4_C
24	AUD_NB_MUTE
25	ESATA_PTX_DRX_N4_C
26	AUD_NB_MUTE
27	ESATA_PTX_DRX_P4_C
28	AUD_NB_MUTE
29	ESATA_PTX_DRX_N4_C
30	AUD_NB_MUTE

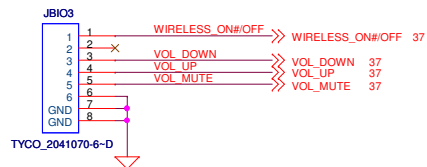
Additional board signals shown on the left:

- 18 USBP2+
- 18 USBP2-
- 18 +V5\_RUN
- 18 +V5\_ALW

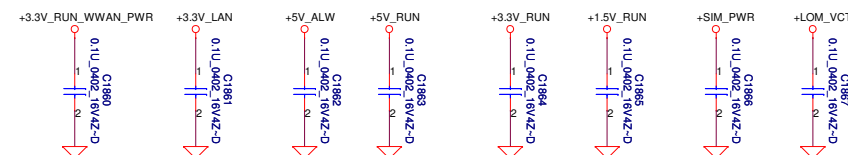
The connector is labeled MOLEX\_48210-3011-D.

[illegible]

Change to 6 pins connector



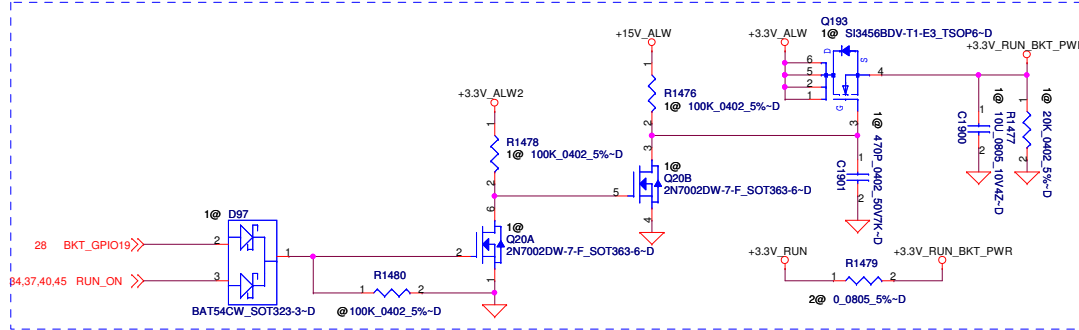
Pin	Internal Signal	External Connection
1	DETECT_GND	
2	CLK_PCIE_MINI#1	CLK_PCIE_MINI#1 16
3	MINICLK_REQ#	CLK_PCIE_MINI#1 16
4	UIM_CLK_REQ#	
5	UIM_CLK	
6	UIM_DATA	
7	UIM_RESET	
8	UIM_VPP	
9	PCIE_PRX_WANTX_N1	PCIE_PRX_WANTX_N1 16
10	PCIE_PRX_WANTX_P1	PCIE_PRX_WANTX_P1 16
11	PCIE_PTX_WANRX_N1_C	PCIE_PTX_WANRX_N1_C 16
12	PCIE_PTX_WANRX_P1_C	PCIE_PTX_WANRX_P1_C 16
13	WWAN_SW_USBD-	
14	WWAN_SW_USBD+	
15	SW_LAN_TX0+	SW_LAN_TX0+ 31
16	SW_LAN_TX0-	SW_LAN_TX0- 31
17	SW_LAN_TX1+	SW_LAN_TX1+ 31
18	SW_LAN_TX1-	SW_LAN_TX1- 31
19	SW_LAN_TX2+	SW_LAN_TX2+ 31
20	SW_LAN_TX2-	SW_LAN_TX2- 31
21	SW_LAN_TX3+	SW_LAN_TX3+ 31
22	SW_LAN_TX3-	SW_LAN_TX3- 31
23	RED_CRT	RED_CRT 25
24	GREEN_CRT	GREEN_CRT 25
25	BLUE_CRT	BLUE_CRT 25
26	HSYNC_CRT	HSYNC_CRT 25
27	VSNC_CRT	VSNC_CRT 25
28	DAT_DDC2_CRT	DAT_DDC2_CRT 25
29	CLK_DDC2_CRT	CLK_DDC2_CRT 25
30	USBP0+	USBP0+ 18
31	USBP0-	USBP0- 18
32	IO_LOOP	IO_LOOP 19
33		
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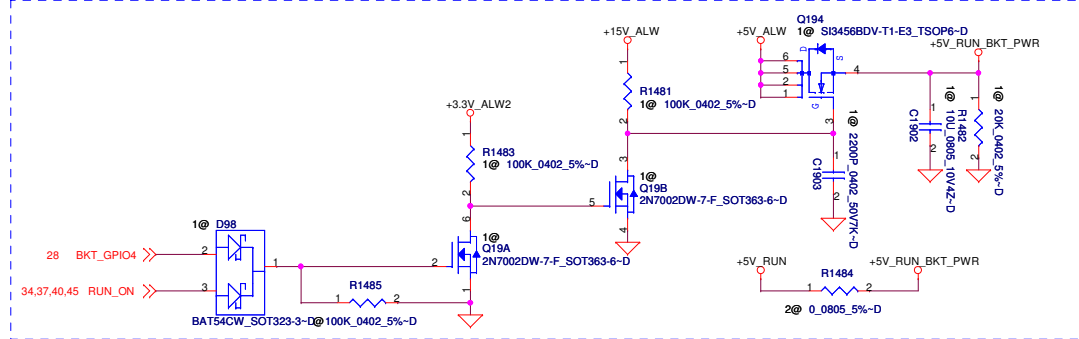
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<b>COMPAL ELECTRONICS, INC.</b>			
<b>Display port</b>			
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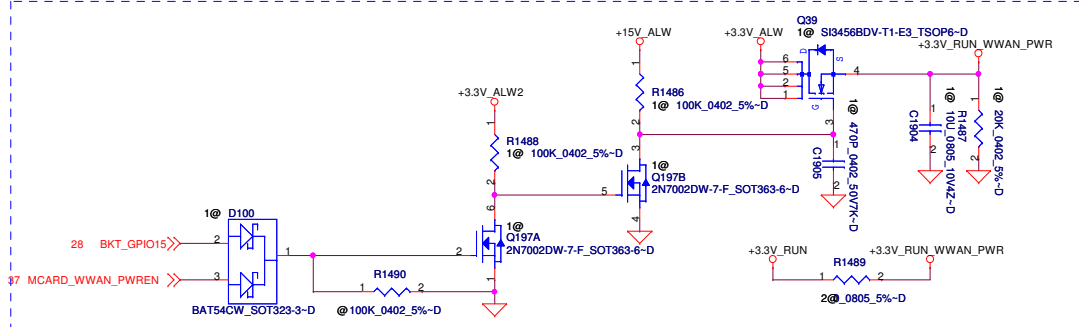
### +3.3V\_RUN\_BKT\_PWR Source



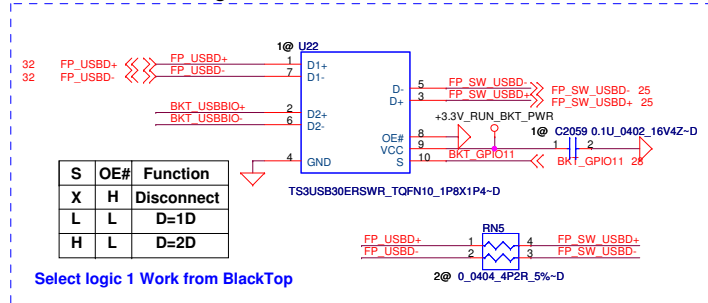
### +5V\_RUN\_BKT\_PWR Source, for Touch Pad and Audio Amplifier



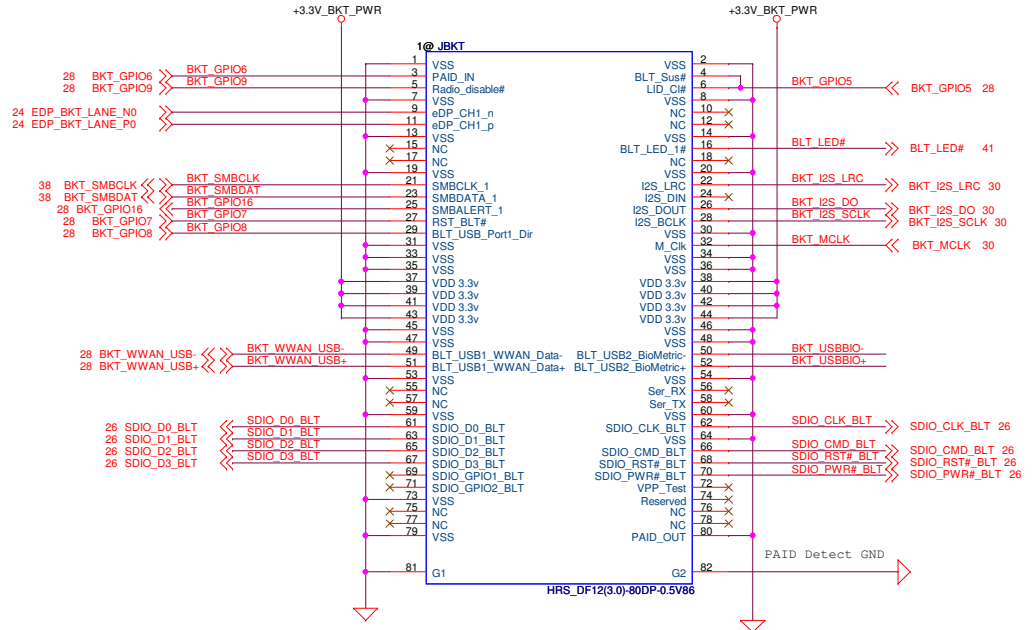
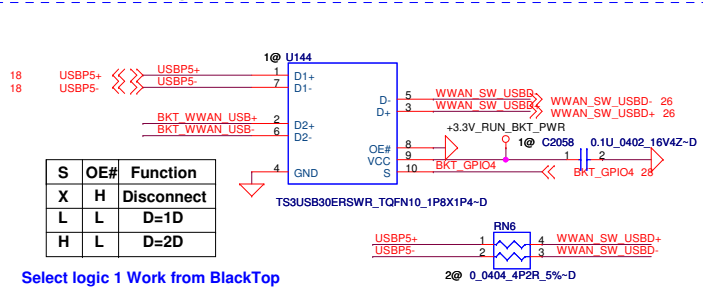
### +3.3V\_RUN\_WWAN\_PWR Source, for WWAN



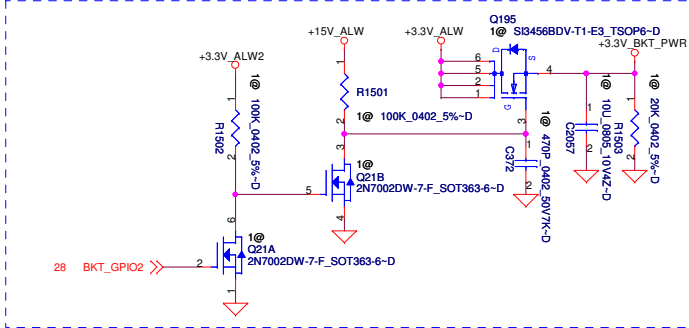
### For Biometric USB signals isolation



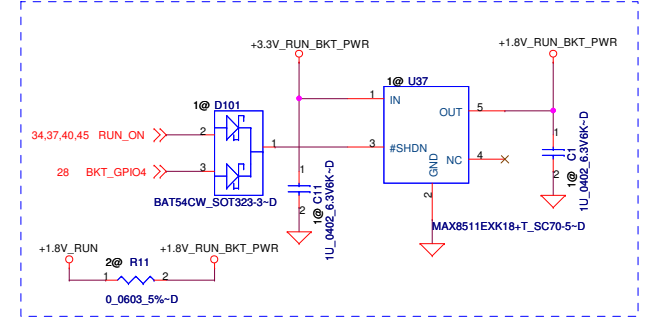
### For WWAN USB signals isolation



### Enable BlackTop POWER



### For Audio I2S



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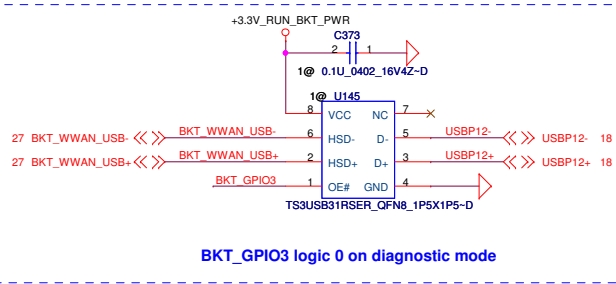


BlackTop POWER and CONN			
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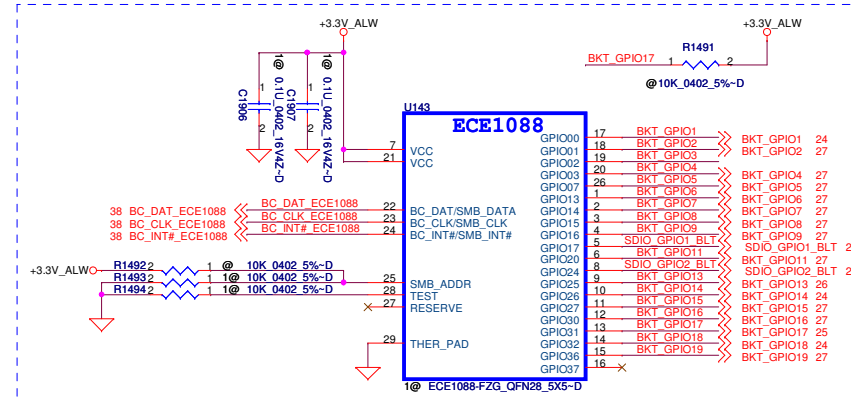
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## GPIO Expander for BlackTop

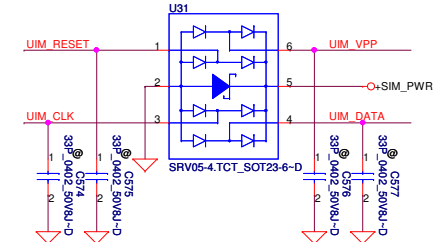
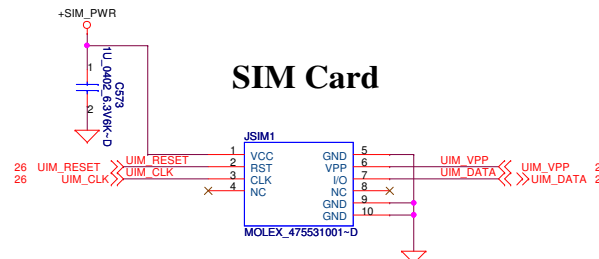
Add BlackTop to PCH interface by USB signal when diagnostic mode



- BKT\_GPIO1 → For eDP signals switch
- BKT\_GPIO2 → For BKT power switch
- BKT\_GPIO3 → For TP power switch&USB signal switch
- BKT\_GPIO4 → For AMP/TP power source&USB signal switch
- BKT\_GPIO5 → For LID\_Closed
- BKT\_GPIO6 → For PAD\_Out
- BKT\_GPIO7 → For BKT Reset
- BKT\_GPIO8 → For USB\_SEL\_BLK
- BKT\_GPIO9 → For Radio\_OFF
- BKT\_GPIO11 → Biometric mux switch
- BKT\_GPIO12 → For WLAN antenna mux control
- BKT\_GPIO13 → RSB\_DET#
- BKT\_GPIO14 → For Inverter Power
- BKT\_GPIO15 → For WWAN Power
- BKT\_GPIO16 → For SMBALERT
- BKT\_GPIO17 → For Biometric reset signal
- BKT\_GPIO18 → For LVDS Power switch
- BKT\_GPIO19 → For TP Power



## SIM Card



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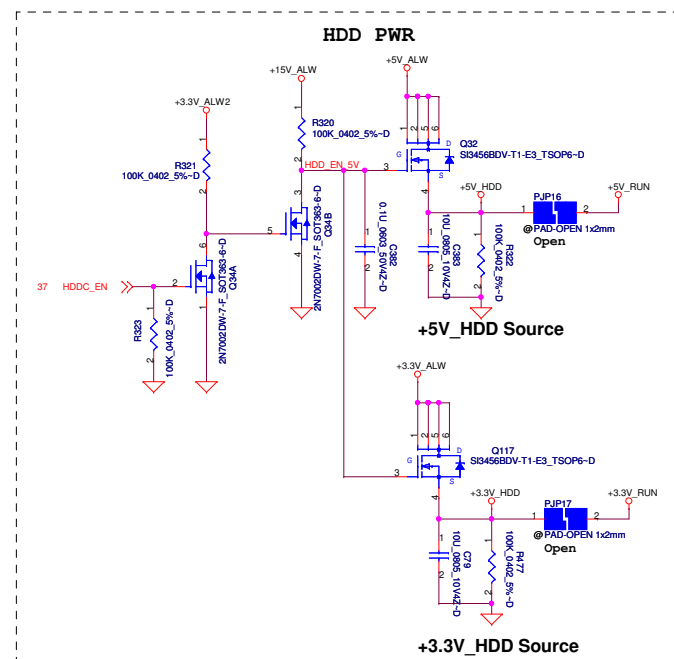
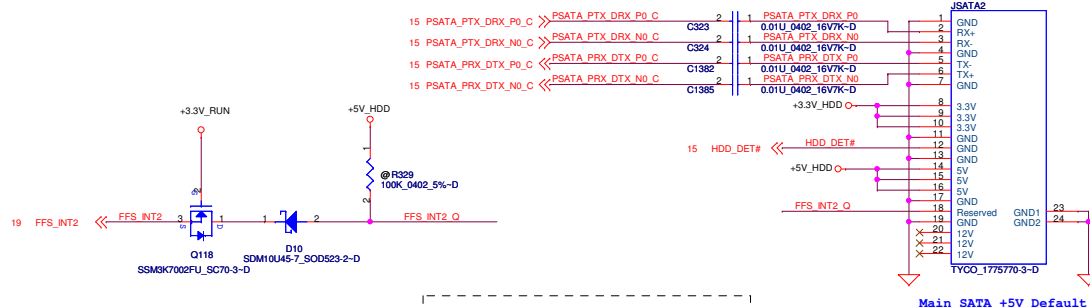
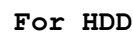
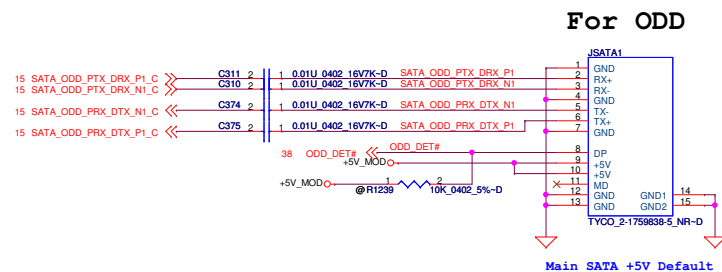
Compal Electronics, Inc.

Title: Braidwood/ SATA repeater & PCIE SATA SW

Size: Document Number: LA-5691P

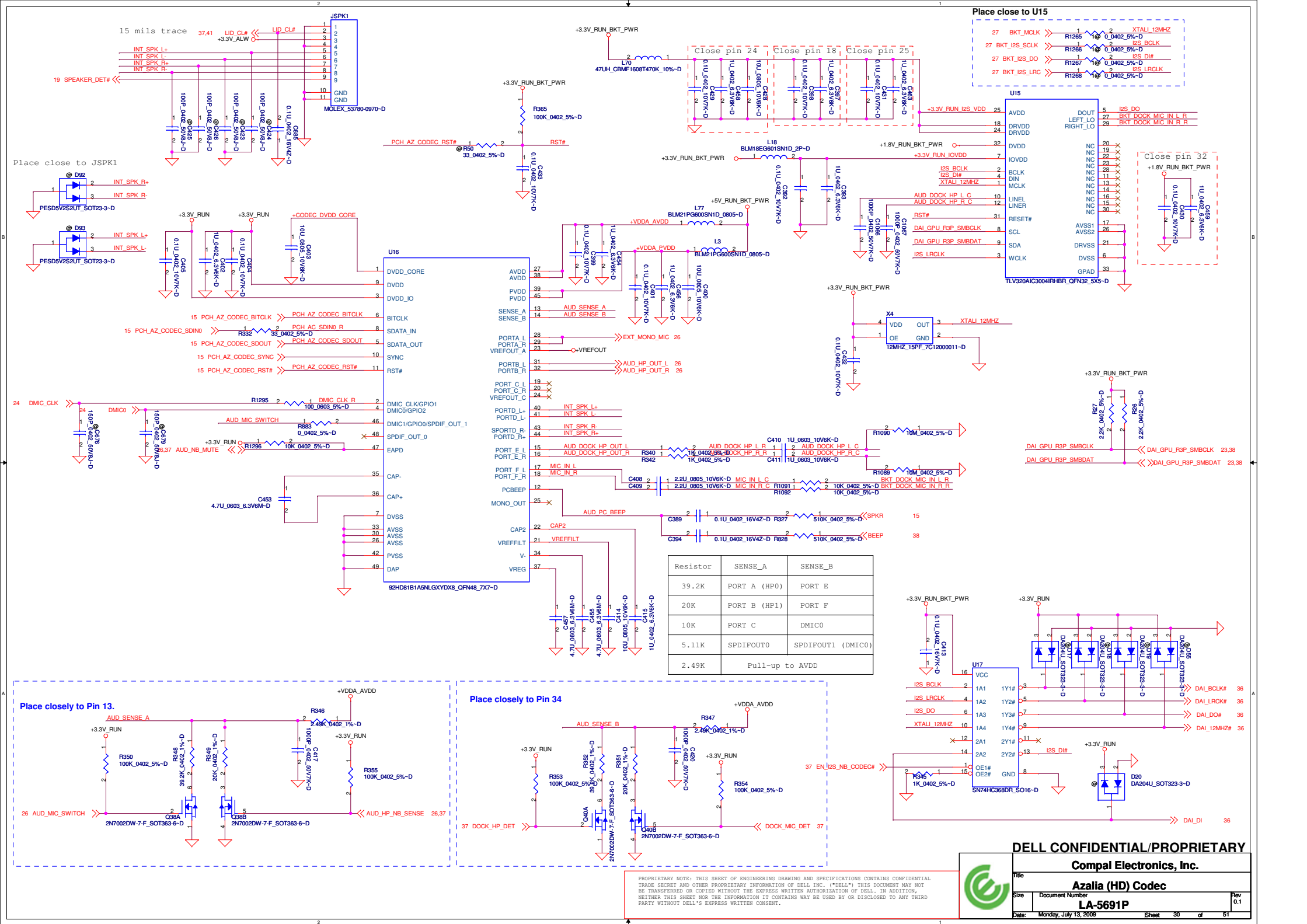
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Title			
<b>ODD/HDD CONNECTOR</b>			
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USH BCM5882 and China TPM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 3@	POP	@	@
SIO 5028 ->SP_TPM_LPC_EN	PU R841	@	POP	@
	PD R483	POP	@	@
	PU R788	@	@	@
PCH GPIO38 ->TPM_ID1	PU R787	@	@	POP
	PD R339	POP	POP	@
PCH GPIO38 ->TPM_ID0	PU R273	POP	POP	@
	PD R922	@	@	POP

LOW:Power Down Mode  
High:Working Mode

### China TPM

TCM Vender	POP
ZTE	R1026, R1023, C23, C1174
Jetway	C1175, R910

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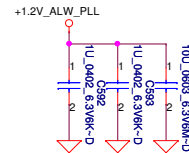
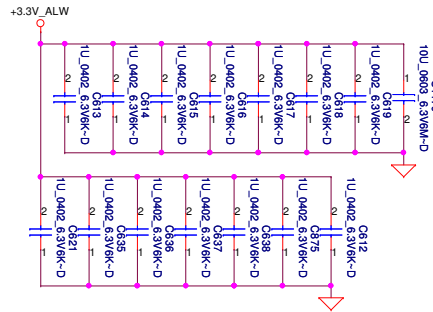
USH BCM5882 (2/2)

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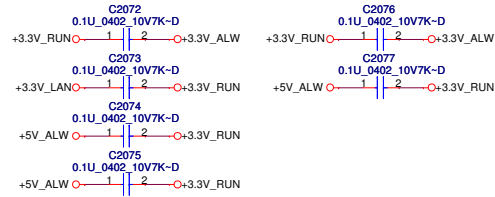


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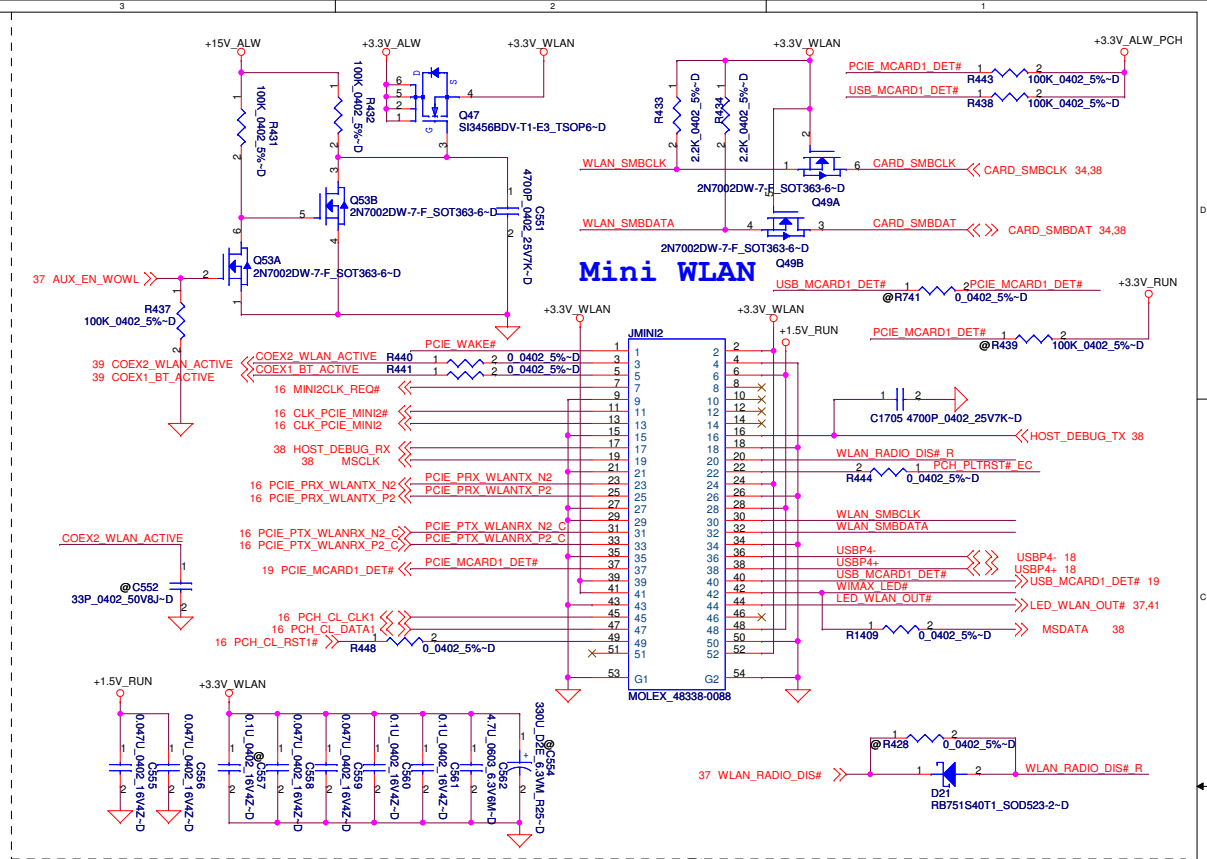




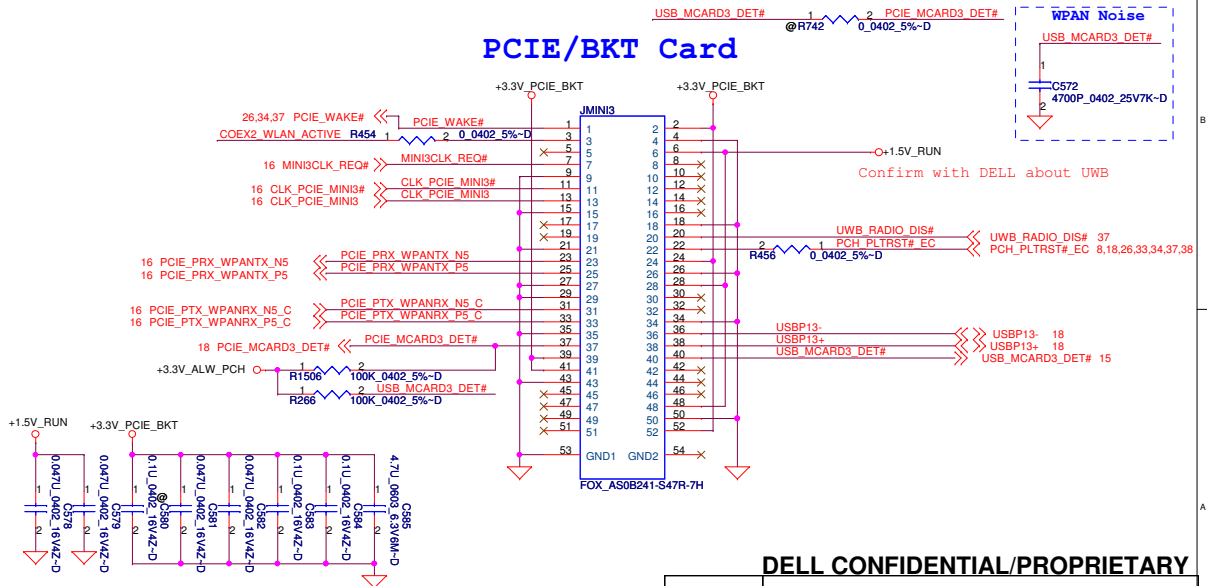
### Stitching caps for MDI



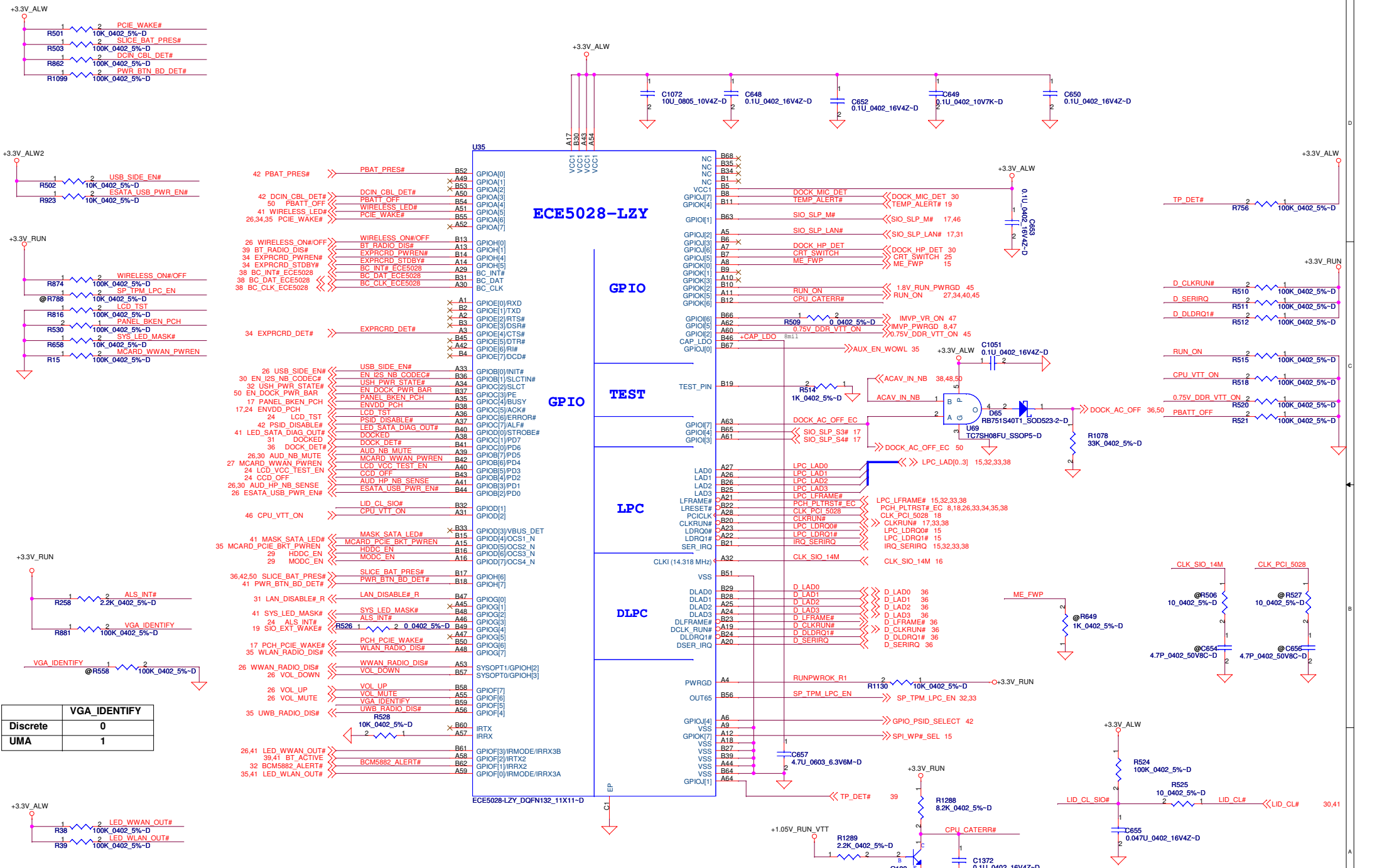
### Stitching caps for PCIe6



### PCIE/BKT Card





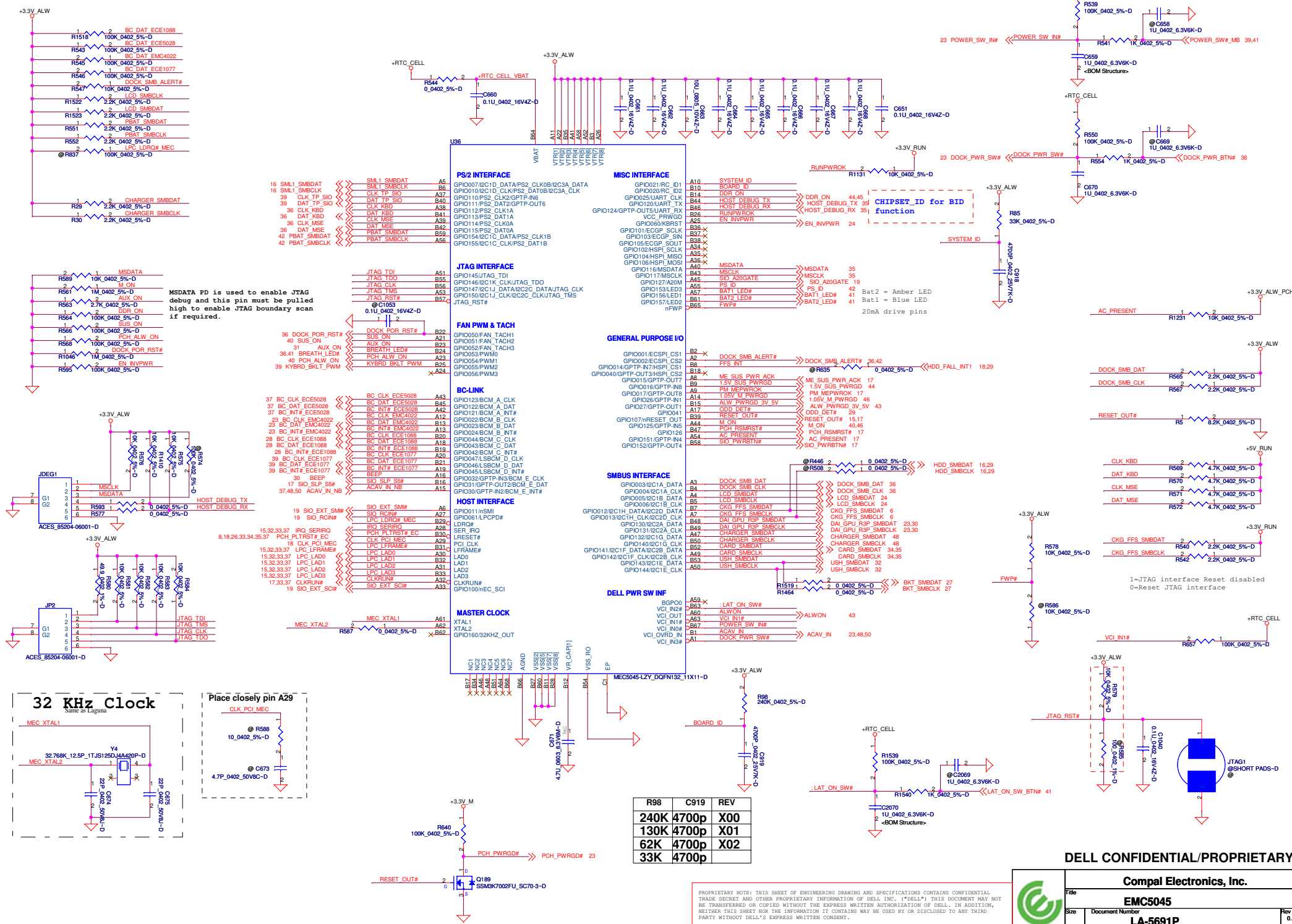


	VGA_IDENTIFY
Discrete	0
UMA	1

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Compal Electronics, Inc.			
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# Touch Pad

The schematic diagram illustrates the Touch Pad circuit. It features a +5V\_ALW supply connected to a network of resistors R613 and R614 (4.7k\_0402 5%-D). The circuit includes four capacitors C680, C681, C682, and C683 (10p\_0402 50V/6J-D) and two inductors L41 and L42 (BLM18AG601SN1D\_0603-D). The circuit is connected to TP\_DATA, TP\_CLK, DAT\_TP\_SIO, and CLK\_TP\_SIO signals, which are then connected to DAT\_TP\_SIO 38 and CLK\_TP\_SIO 38 pins.

38 BC\_DAT ECE1077

38 BC\_CLK ECE1077

38 BC\_INT# ECE1077

+3.3V\_ALW

TP\_CLK

TP\_DATA

+5V\_TP\_PWR

+5V\_ALW

+3.3V\_TP\_PWR

38 KYBRD\_BKLT\_PWM

37 TP\_DET#

KYBRD\_BKLT\_PWM

TP\_DET#

J1P1

1 1

2 2

3 3

4 4

5 5

6 6

7 7

8 8

9 9

10 10

11 11

12 12

13 13

14 14

15 15

16 16

17 G1

18 G2

HRS\_FH12-16S-0P5SH(55)-D

+5V\_TP\_PWR

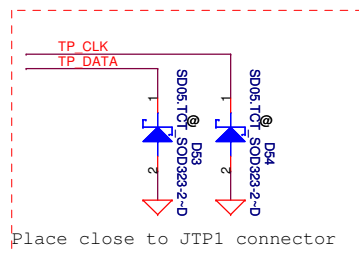
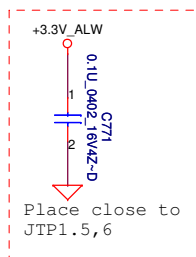
0.1uF 0402.16V4Z-D

Q678

+5V\_ALW

0.1uF 0402.16V4Z-D

C1413



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[illegible]

38,41 POWER\_SW#\_MB <<POWER\_SW# MB

@C684  
100P\_0402\_50V8J-D

@PWRSW1  
SHORT PADS-D  
Place on Top

@PWRSW2  
SHORT PADS-D  
Place on Bottom

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

Part Number	Description
DC02000CS0L	H-CONN SET ZGX MB-MDC

Part Number	Description
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LC 14 WXGA+(-1ch)

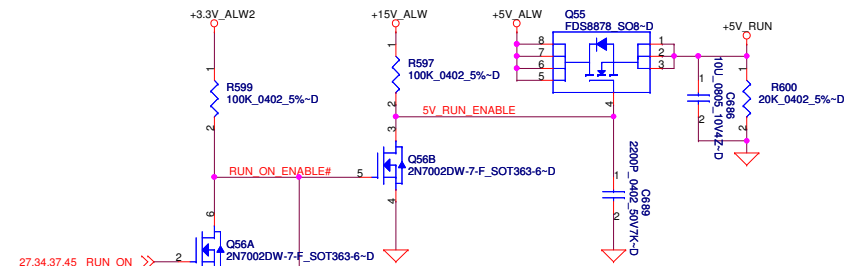
Part Number	Description
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+(-2ch)

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

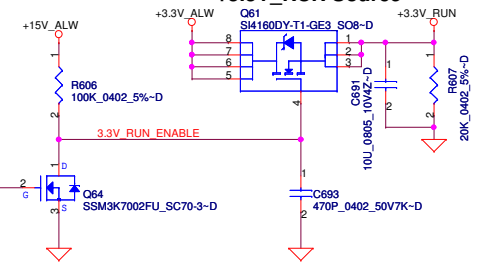


Title			
Touch PAD/Int KB/LID			
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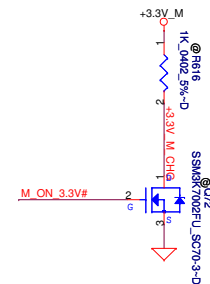
### +5V<sub>RUN</sub> Source



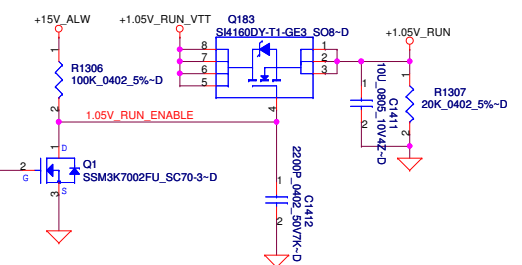
### +3.3V\_RUN Source



### +1.5V\_RUN Source

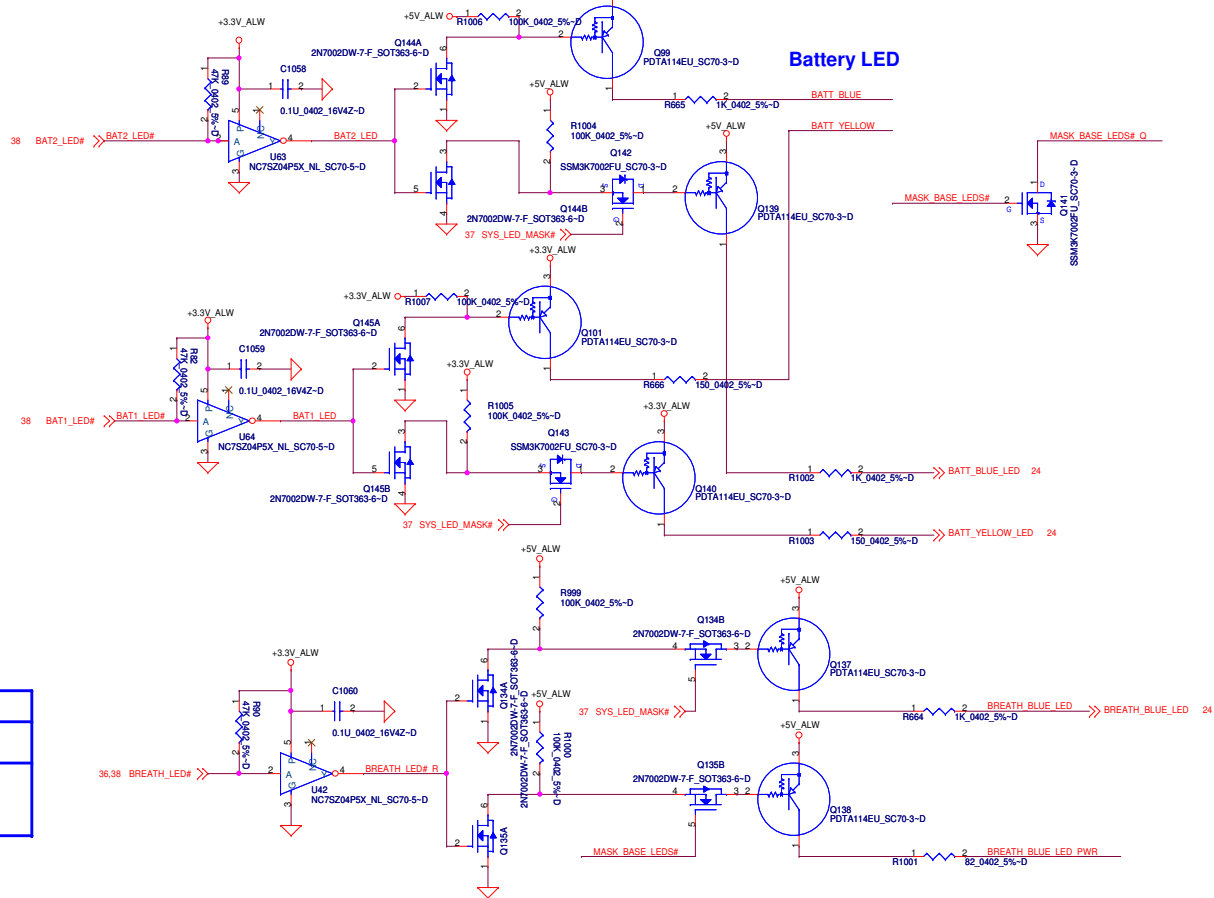
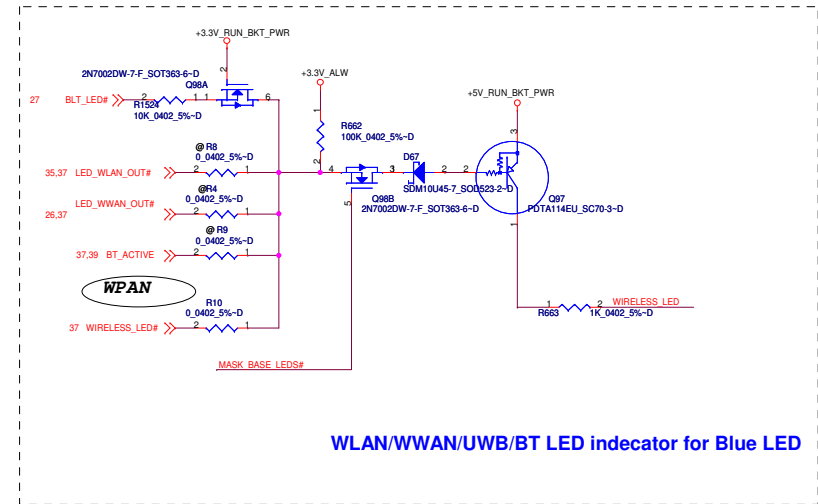
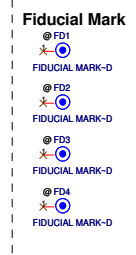
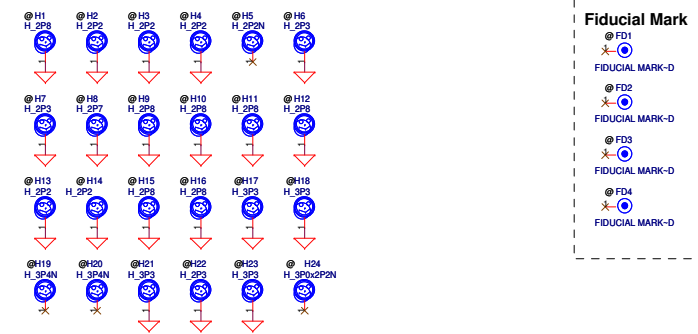
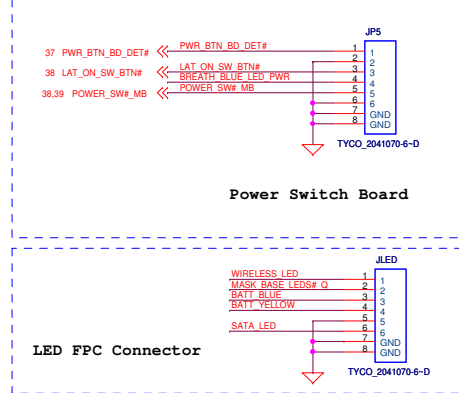
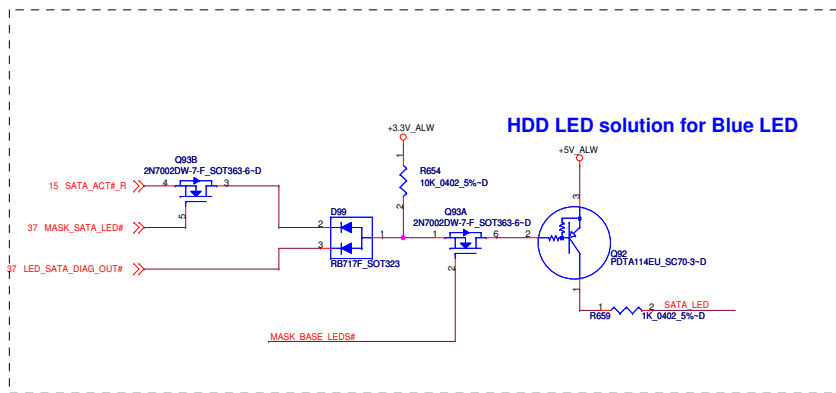


### +1.05V\_RUN Source

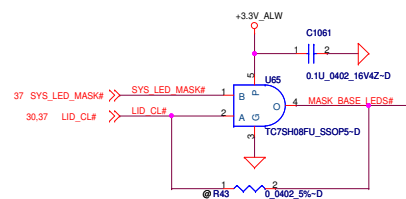


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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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**PAD and Standoff**

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+3.3V\_ALWP/ +5V\_ALWP/ +5V\_ALW2 / +15V\_ALWP/ +3.3V\_RTC\_LDO

5 Volt +/-5%  
Thermal Design Current:4.854A  
Peak Current:6.935A  
OCP\_MIN:8.322A


3.3 Volt +/-5%  
Thermal Design Current: 3.133A  
Peak current: 4.475A  
OCP\_MIN:5.37A

VOUT2=5V  
L=2.8uF  
Fsw=400KHz  
D=0.256  
Input Ripple Current= $TDC * (D * (1-D))^{0.5} = 3.641A$   
Output Ripple Current= $(19-5) * 0.263/3u/400K = 3.32A$   
Output Ripple Voltage= $3.32 * 25m = 83mV$

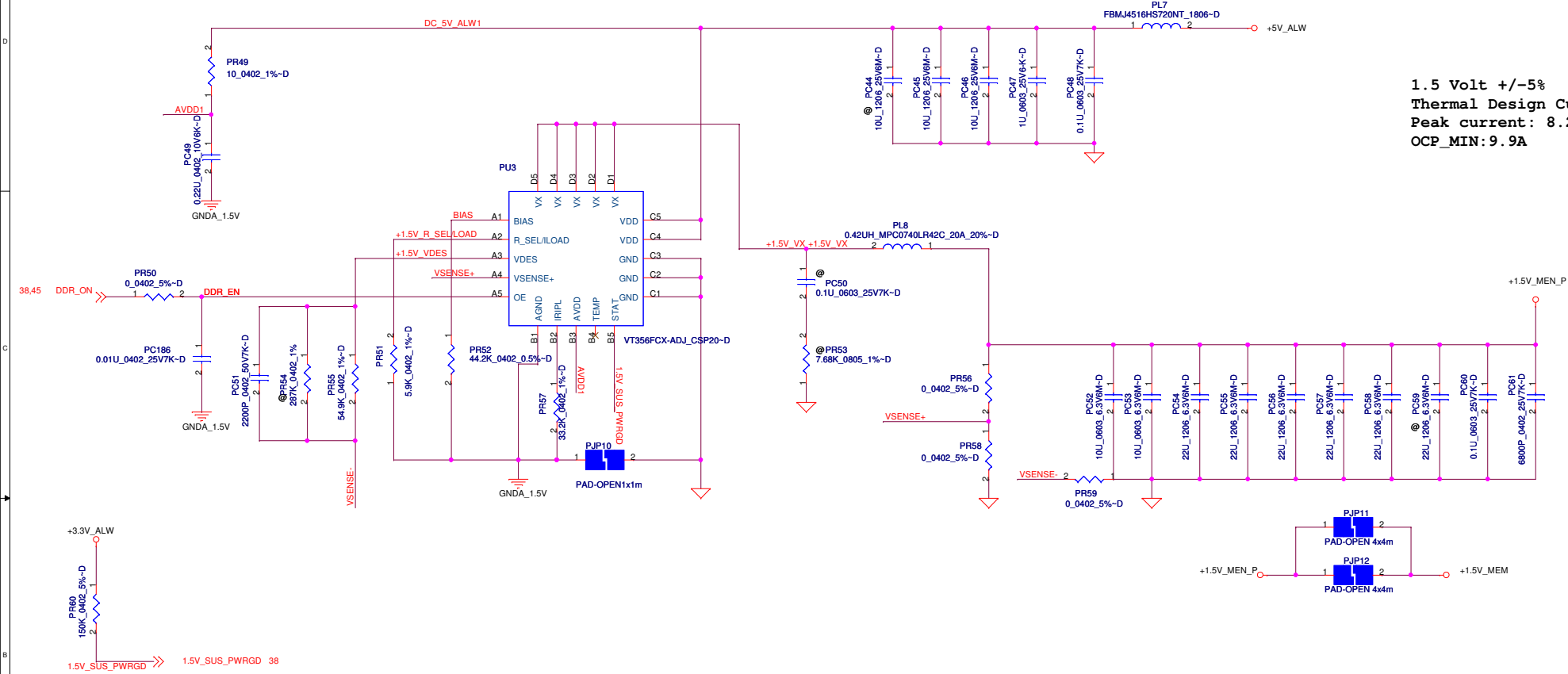
VOUT2=3.3V  
L=2.8uF  
Fsw=300KHz  
D=0.169  
Input Ripple Current= $TDC * (D * (1-D))^{0.5} = 2.051A$   
Output ripple current= $(19-3.3) * 0.173/3u/300K = 3.264A$   
Output ripple Voltage= $3.264 * 25 = 81.6mV$

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		DC/DC +3V/ +5V	
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# +1.5V\_MEN\_P (VT356)



1.5 Volt +/-5%  
Thermal Design Current: 5.775A  
Peak current: 8.25A  
OCP\_MIN: 9.9A

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Title  
+1.5V\_MEM

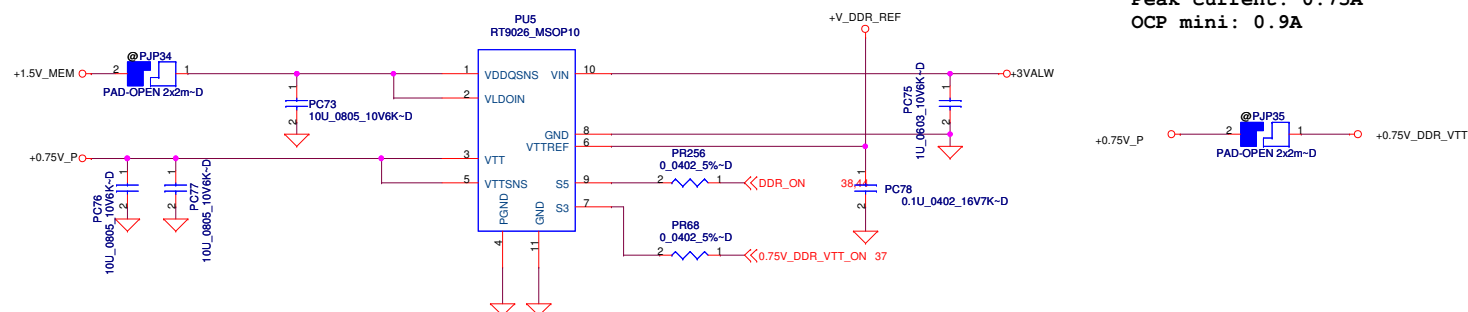
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1.8 Volt +/-5%  
Thermal Design Current: 0.894A  
Peak current: 1.277A  
OCP\_min:1.532A



0.75Volt +/-5%  
Thermal Design Current: 0.525A  
Peak current: 0.75A  
OCP mini: 0.9A



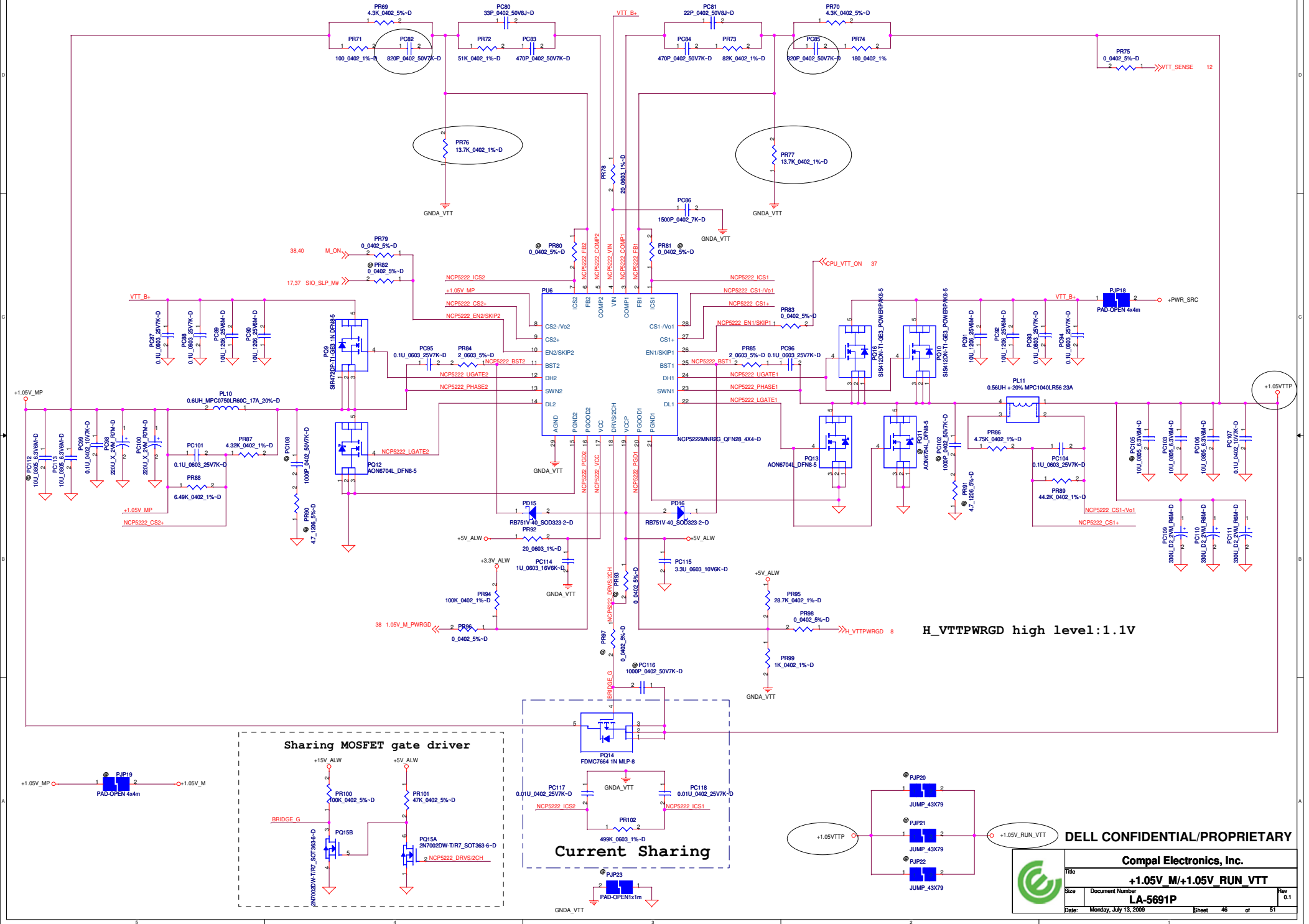
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Title			
<b>+1.8V RUN/+0.75V DDR VT</b>			
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1.05 Volt +/-5%  
Thermal Design Current: 15.9A  
Peak current: 22.7A













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