MODEL NAME : ZAVA1/ZAVC1
PCB NO : DA80011D000 LA-B015P-R1.0

Compal Confidential

Schematic Document

Intel BoardWell ULT
ZAVA1/ZAVC1
DIS AMD 25W/M2+DDR3x8

2014-10-17 **Rev: 1.0**

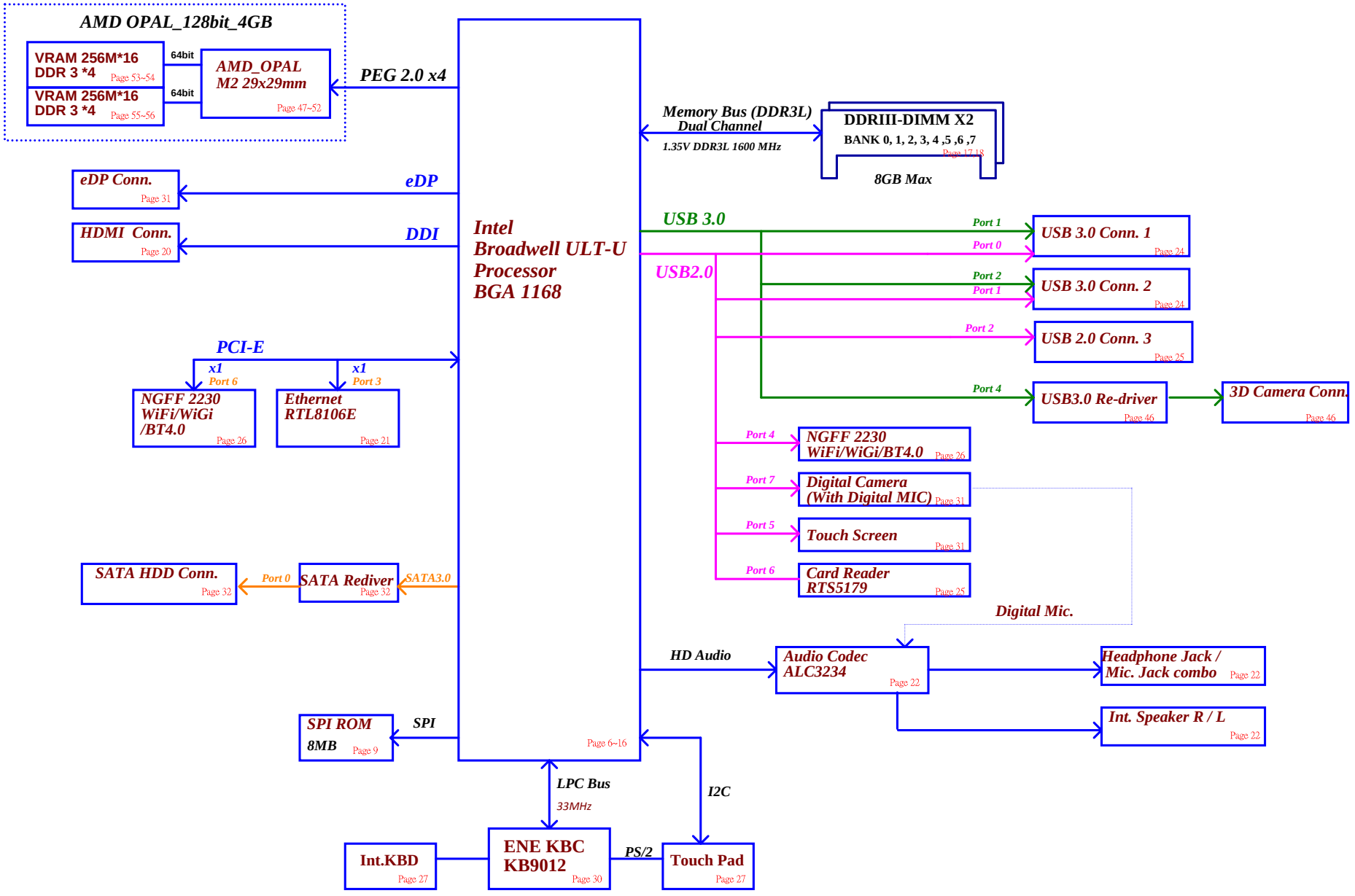
Security Classification	Compal Secret Data		
Issued Date	2014/10/17	Deciphered Date	2018/04/30

Compal Electronics, Inc.

Title: *Cover Page*

Size: Document Number: *LA-B015P* Rev: 1.0

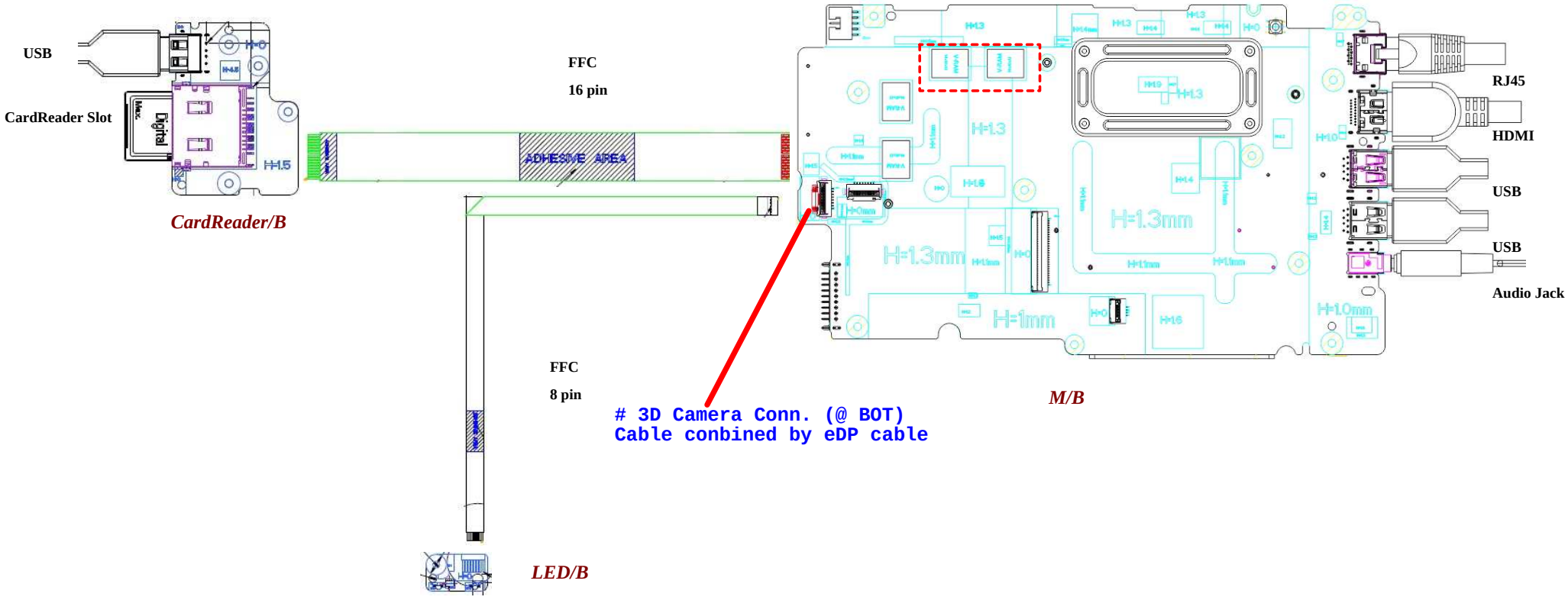
Date: Friday, October 17, 2014 Sheet 1 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/10/17	Deciphered Date	2018/04/30

Compal Electronics, Inc.			
Title: Block Diagram			
Size	Document Number: LA-B015P		Rev: 1.0
Date: Friday, October 17, 2014	Sheet 2 of 56		

Compal Confidential
File Name : LA-B015P



Security Classification	Compal Secret Data		
Issued Date	2014/10/17	Deciphered Date	2018/04/30

Compal Electronics, Inc.			
Title	MB/DB Drawing		
Size	Document Number	LA-B015P	Rev 1.0
Date:	Friday, October 17, 2014	Sheet 3 of 56	

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	VGA	DIMM	XDP	Thermal Sensor	FFS
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012			V			V	
SMBCLK SMBDATA	ULT				V			V
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

Link

Symbol Note :

: means Digital Ground

: means Analog Ground

HSW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)	DIS(OPAL)
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

BDW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)	DIS(OPAL)
0	1.0_3D CAM			
1		1.0_3D CAM		
2			1.0_3D CAM	
3	SSI(BDW)			
4		SSI(BDW)		
5			SSI(BDW)	
6	PT(BDW) SSI_3D CAM			
7		PT(BDW) SSI_3D CAM		
8			PT(BDW) SSI_3D CAM	
9	ST(BDW) PT_3D CAM			
10		ST(BDW) PT_3D CAM		
11			ST(BDW) PT_3D CAM	
12	1.0(BDW) ST_3D CAM			
13		1.0(BDW) ST_3D CAM		
14			1.0(BDW) ST_3D CAM	
15				SSI
16				PT
17				ST
18				1.0

CLOCK SIGNAL (Diff. 100MHz)	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

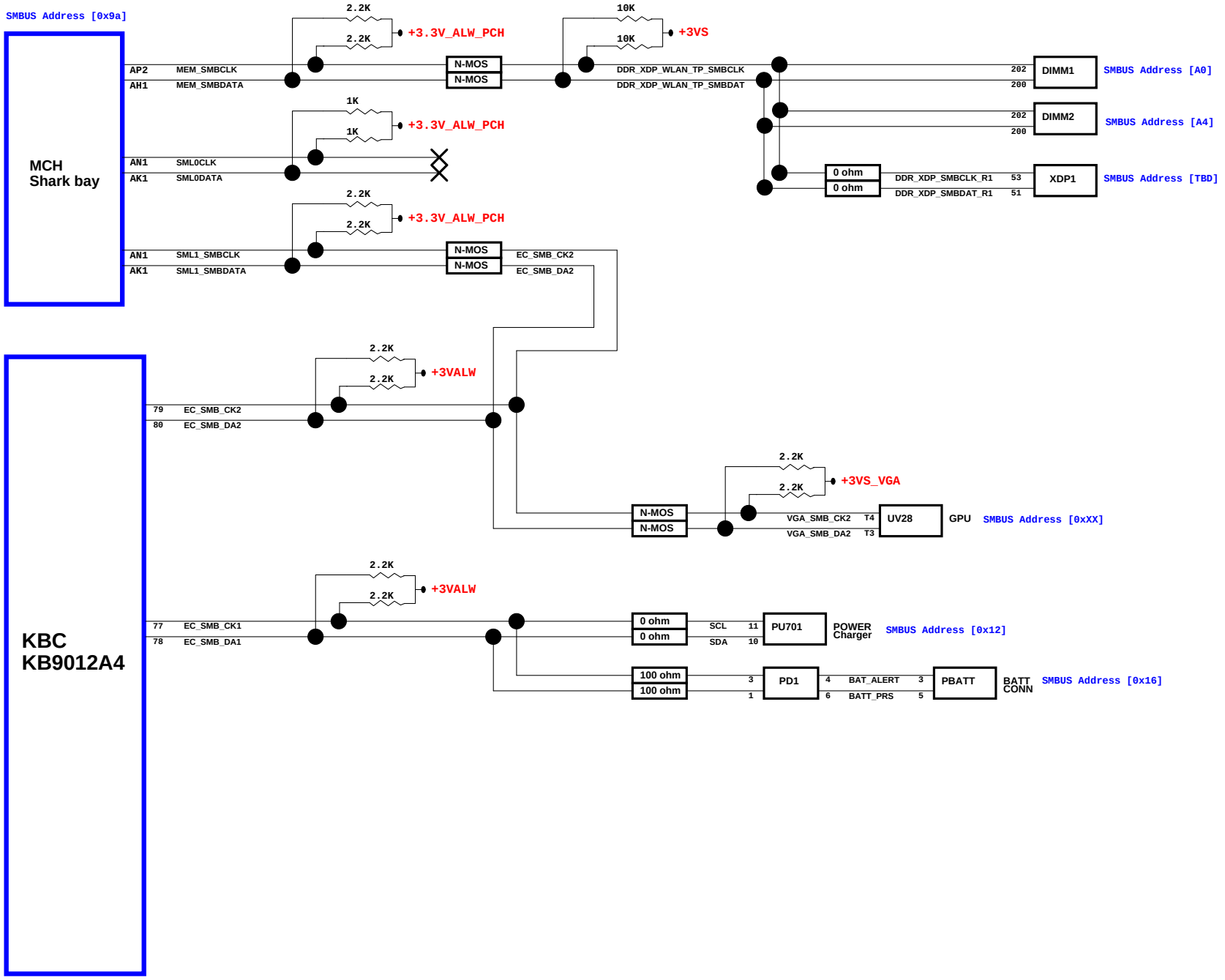
ULT		
	USB3.0	
	Port1	USB connector 1
	Port2	USB connector 2
	Port3	
	Port4	3D Camera
	USB2.0	
	Port0	USB connector 1
	Port1	USB connector 2
	Port2	USB connector 3 (D/B)
	Port3	
	Port4	MINI Card (WLAN)
	Port5	Touch Screen Panel
	Port6	Card Reader
	Port7	Camera
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	10/100 LAN
	Lane 4	MINI Card (WLAN)
	Lane 5	PEG (AMD JET/TOBAZ)
	Lane 6	
	SATA	
	SATA0	HDD
	SATA1	
	SATA2	
	SATA3	

Compal Electronics, Inc.

Title: ID Table / Function Map

Size | Document Number: LA-B015P | Rev: 1.0

Date: Friday, October 17, 2014 | Sheet 4 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/10/17	Deciphered Date	2018/04/30

Compal Electronics, Inc.

Title: **SMBus/I2C Connection Map**

Size: Document Number: **LA-B015P** Rev: 1.0

Date: Friday, October 17, 2014 Sheet 5 of 56

BDW_Pre-QS for DVT2 BDW_QS for DVT2

i3 CPU

i5 CPU

UC1 I5_1.2G@

CL8065801674128 QG21 C0 1.2G

SA00007OS0L

i7 CPU

UC1 I7_1.2G@

CL8065801675027 QG22 C0 1.2G

SA00007OT0L

i3 CPU

i5 CPU

UC1 I5_2.2G@

FH8065801620204 QH3G F0 2.2G

SA00008990L

i7 CPU

UC1 I7_2.4G@

FH8065801620004 QH3E F0 2.4G

SA000089A0L

BDW (ES2) CPU for 3D / 4G

UC1 1.8G1600@

CL8065801703601 QGH9 D0 1.8G

SA00007U90L

UC1 1.6G1600@

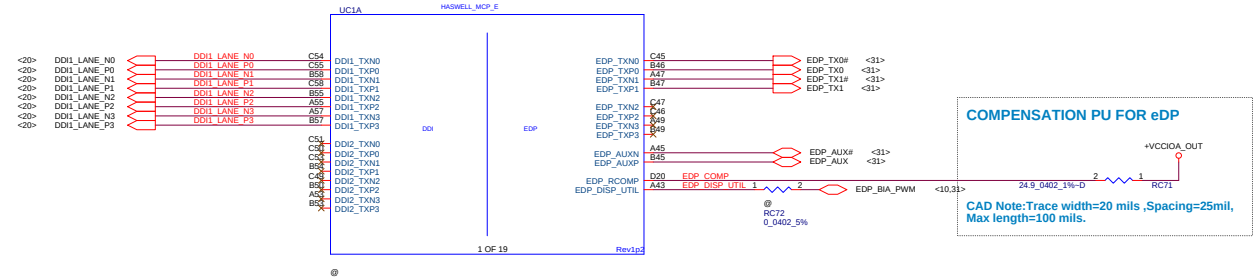
CL8065801703603 QGHB D0 1.6G

SA00007UH0L

UC1 1.6G1333@

CL8065801703602 QGHA D0 1.6G

SA00007UG0L



COMPENSATION PU FOR eDP

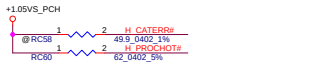
+VCCIOA_OUT

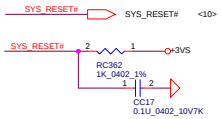
24.9_0402_1%~D

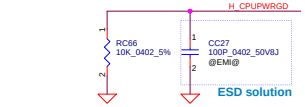
RC71

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

RC72 0_0402_5%







CAD Note:
Avoid stub in the PWRGD path while placing resistors RC115

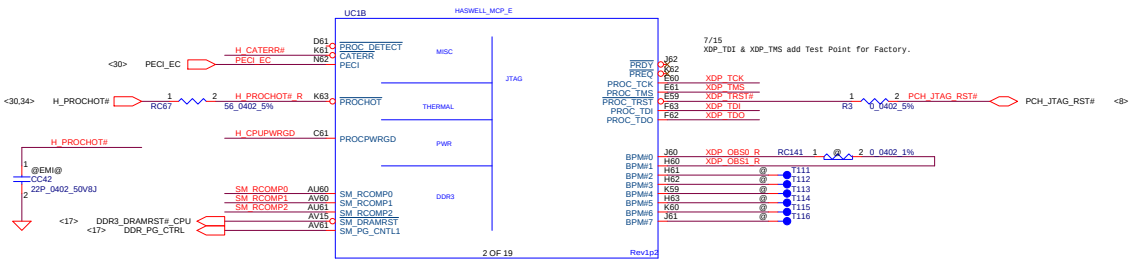
DDR3 COMPENSATION SIGNALS

200_0402_1% RC68 SM_RCOMP0

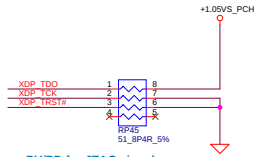
120_0402_1% RC69 SM_RCOMP1

100_0402_1% RC70 SM_RCOMP2

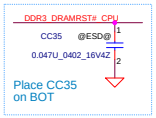
CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil



7/15
XDP_TDI & XDP_TMS add Test Point for Factory.



PU/PD for JTAG signals



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Title	MCP(1,2/19) eDP,XDP,MISC		
Size	Document Number		Rev
	LA-B015P		0.1
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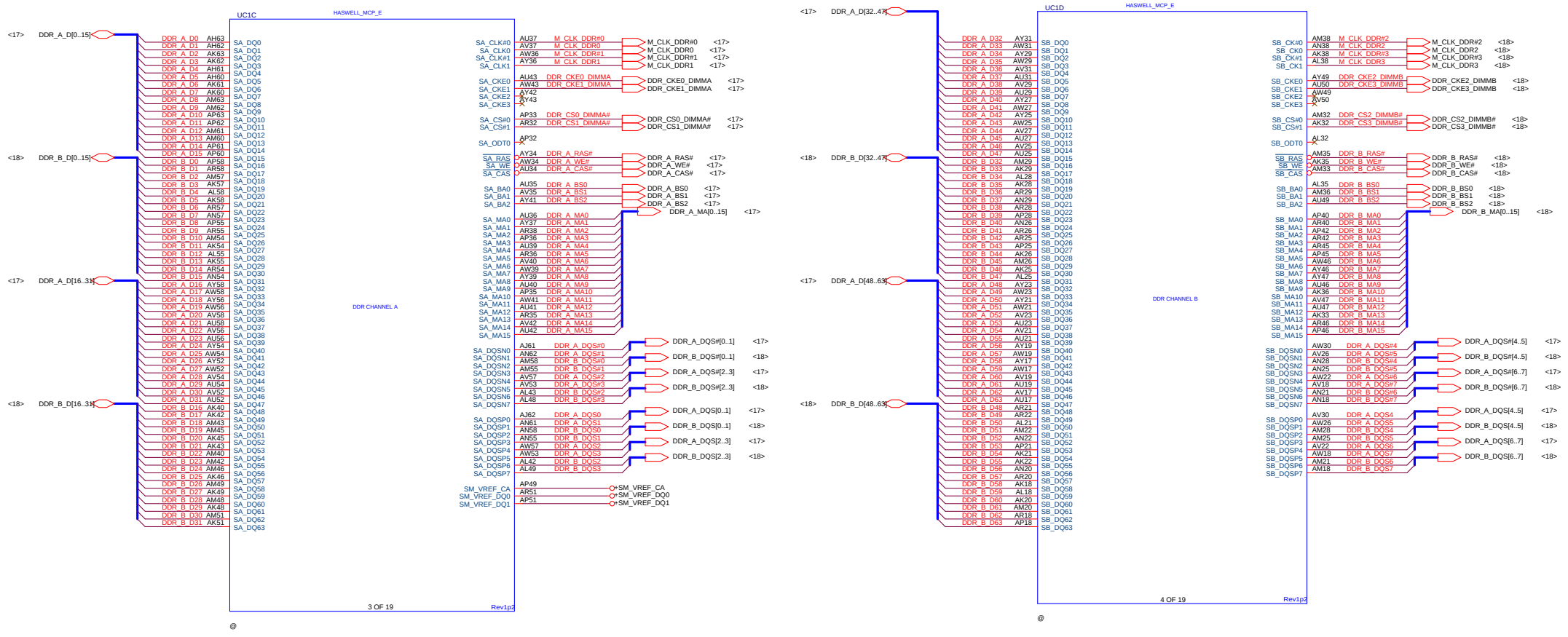
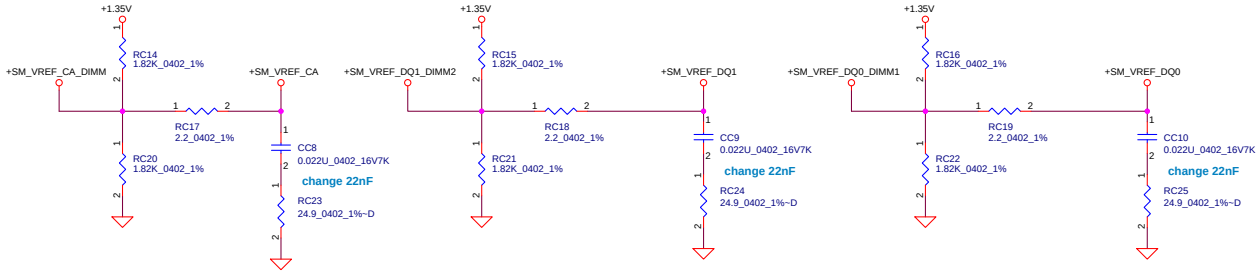
Interleaved Memory





confirm by intel request PDG P141

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title: MCP(3,4/19) DDR3
				Size: Document Number: LA-B015P Rev: 0.1
				Date: Wednesday, September 10, 2014 Sheet 7 of 56

RTC Battery

+RTCBATT
+CHGRTC
RC10 1K_0402_5%
W=20mils
W=20mils
DC1 BAT54CW_SOT323-3
+RTCVCC
W=20mils
CC26 1U_0603_10V6K

+RTCVCC — JP14 @ JUMP_43X39
+CHGRTC — JP12 @ JUMP_43X39 — +3VLP

For GCLK

<19> PCH_RTCX1 — PCH_RTCX1

+RTCVCC
RC1 330K_0402_1%
PCH_INTVRMEN
RC2 330K_0402_1%

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

+3VS
@RC3 PCH_AZ_SDOUT 1K_0402_5%

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED

CC1 XTAL@ 15P_0402_50V8J — PCH_RTCX1
XTAL@ YC1 32.768KHZ_12.5PF_Q13FC1350000
XTAL@ RC4 10M_0402_5%
CC2 XTAL@ 15P_0402_50V8J — PCH_RTCX2
+RTCVCC — RC7 1M_0402_5% — INTRUDER#
RC5 20K_0402_5% — PCH_INTVRMEN
RC6 20K_0402_5% — SRTCRST#
CC3 1U_0402_6.3V6K — PCH_RTCRST#
@ CMOS1 SHORT PADS~D
CC4 1U_0402_6.3V6K

UC1E HASWELL_MCP_E

RTCX1	AW5	RTC
RTCX2	AY5	
INTRUDER	AU6	
INTVRMEN	AV7	
SRTCRST	AV6	
RTCRST	AU7	
HDA_BCLK/I2S0_SCLK	AW8	AUDIO
HDA_SYNC/I2S0_SFRM	AV11	
HDA_RST/I2S_MCLK	AU8	
HDA_SDI0/I2S0_RXD	AY10	
HDA_SDI1/I2S1_RXD	AU12	
HDA_SDO/I2S0_TXD	AU11	
HDA_DOCK_EN/I2S1_TXD	AW10	
HDA_DOCK_RST/I2S1_SFRM	AV12	
I2S1_SCLK	AY8	
PCH_TRST	AE62	JTAG
PCH_TCK	AE62	
PCH_TDI	AD61	
PCH_TDO	AE61	
PCH_TMS	AD62	
RSVD	AL11	
RSVD	AC2	
RSVD	AE63	
JTAGX	AV2	
RSVD		

5 OF 19 Rev1p2

SATA_RN0/PERN6_L3 — J5 — SATA_PRX_DTX_N0_C <32>
SATA_RP0/PERP6_L3 — H5 — SATA_PRX_DTX_P0_C <32>
SATA_TN0/PETN6_L3 — B15 — SATA_PTX_DRX_N0_C <32>
SATA_TP0/PETP6_L3 — A15 — SATA_PTX_DRX_P0_C <32>
SATA HDD
SATA_RN1/PERN6_L2 — J8
SATA_RP1/PERP6_L2 — D8
SATA_TN1/PETN6_L2 — A17
SATA_TP1/PETP6_L2 — B17
SATA_RN2/PERN6_L1 — J6
SATA_RP2/PERP6_L1 — D6
SATA_TN2/PETN6_L1 — B14
SATA_TP2/PETP6_L1 — C15
SATA_RN3/PERN6_L0 — F5
SATA_RP3/PERP6_L0 — E5
SATA_TN3/PETN6_L0 — C17
SATA_TP3/PETP6_L0 — D17
SATA0GP/GPIO34 — V1 — EC_SMI# <30>
SATA1GP/GPIO35 — U1 — PCH_GPIO35 — ODD_DETECT#
SATA2GP/GPIO36 — V6 — ODD_DETECT#
SATA3GP/GPIO37 — AC1 — PCH_GPIO37
SATA_IREF — A12 — SATA_IREF — RC126 1 @ 2 0_0603_1% — +1.05VS_ASATA3PLL
RSVD — L11
RSVD — K10
SATA_RCOMP — C12 — SATA_RCOMP — RC131 1 2 3.01K_0402_1%
SATALED — U3 — SATA_ACT# — SATA_ACT# <25>

PCH Rx side need use strap pin to update PCIE +/-
+3VS — RC107 10K_0402_5% — EC_SMI#

SATA Impedance Compensation
within 500 mils
CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.
reference FFRD sch 0.5

CMOS place near DIMM

<22> PCH_AZ_CODEC_SDIN0
<30> ME_EN — RC8 1K_0402_5% — PCH_AZ_SDOUT

<6> PCH_JTAG_RST# — PCH_JTAG_RST# AU62, PCH_JTAG_TCK AE62, PCH_JTAG_TDI AD61, PCH_JTAG_TDO AE61, PCH_JTAG_TMS AD62

7/15
PCH_JTAG_TCK add Test Point for Factory.

RTC discharge by EC

SRTCRST#
PCH_RTCRST#
@ DMN66D0LDW-7_SOT363-6 QC2B
@ DMN66D0LDW-7_SOT363-6 QC2A
<30> RTC_DIS
@ RC368 100K_0402_5%

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

HDA for Codec

<22> PCH_AZ_CODEC_SDOUT — EMI@ R2356 1 2 33_0402_5% — PCH_AZ_SDOUT
<22> PCH_AZ_CODEC_SYNC — EMI@ R2357 1 2 33_0402_5% — PCH_AZ_SYNC
<22> PCH_AZ_CODEC_RST# — EMI@ R2358 1 2 33_0402_5% — PCH_AZ_RST#
<22> PCH_AZ_CODEC_BITCLK — EMI@ R2359 1 2 33_0402_5% — PCH_AZ_BITCLK
1 @EMI@ CC5 27P_0402_50V8J 2

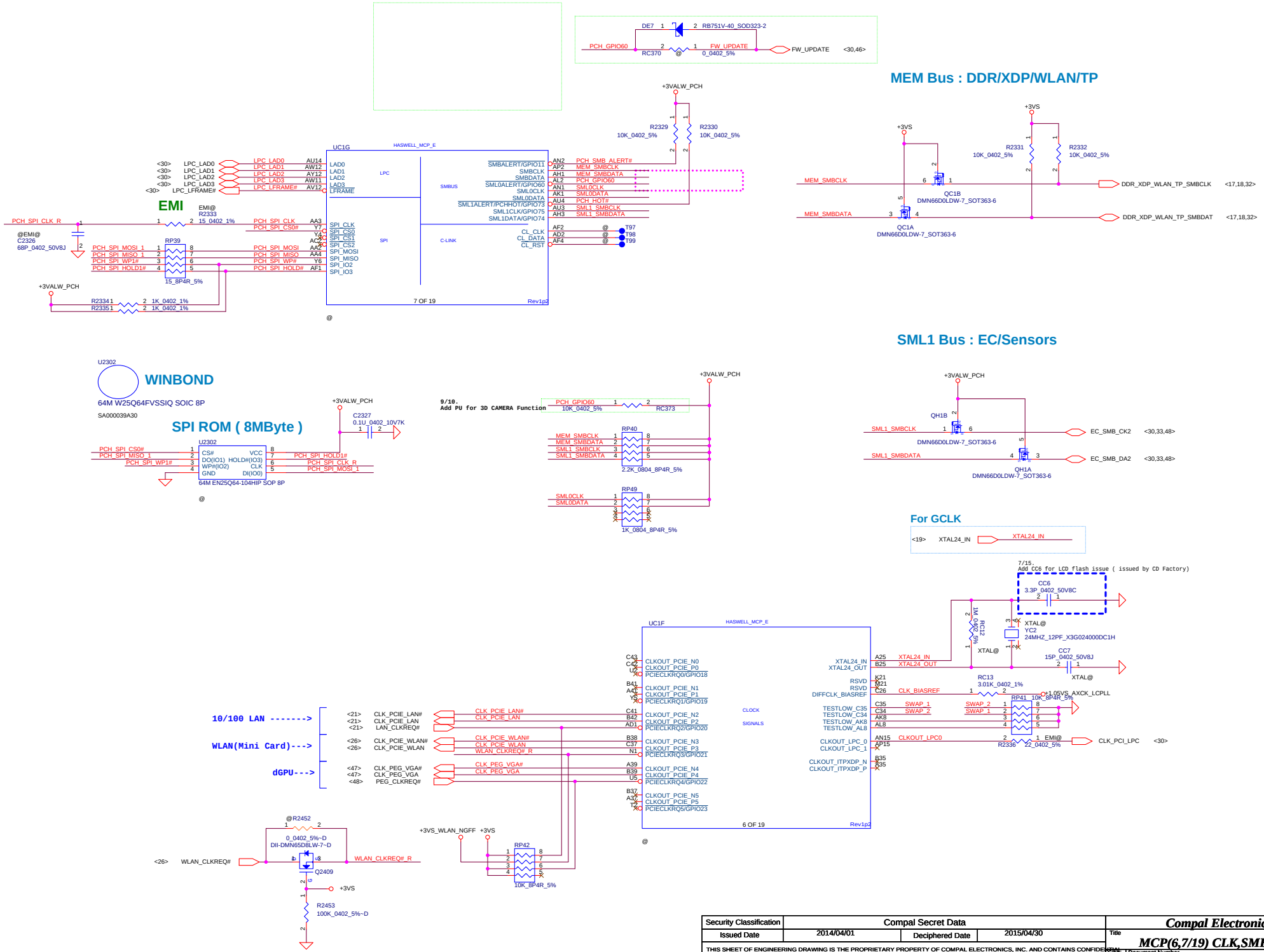
EMI depop location

+3VS
ODD_DETECT# 1 8
PCH_GPIO35 2 7
PCH_GPIO37 3 6
4 5
RP37 10K_8P4R_5%

+1.05VS_PCH
PCH_JTAG_TDI 1 8
PCH_JTAG_TDO 2 7
PCH_JTAG_TMS 3 6
4 5
RP48 51_8P4R_5%

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.
Title: MCP(5/19) RTC,SATA,HDA,JTAG
Size: C
Document Number: LA-B015P
Rev: 0.1
Date: Wednesday, September 10, 2014
Sheet 8 of 56



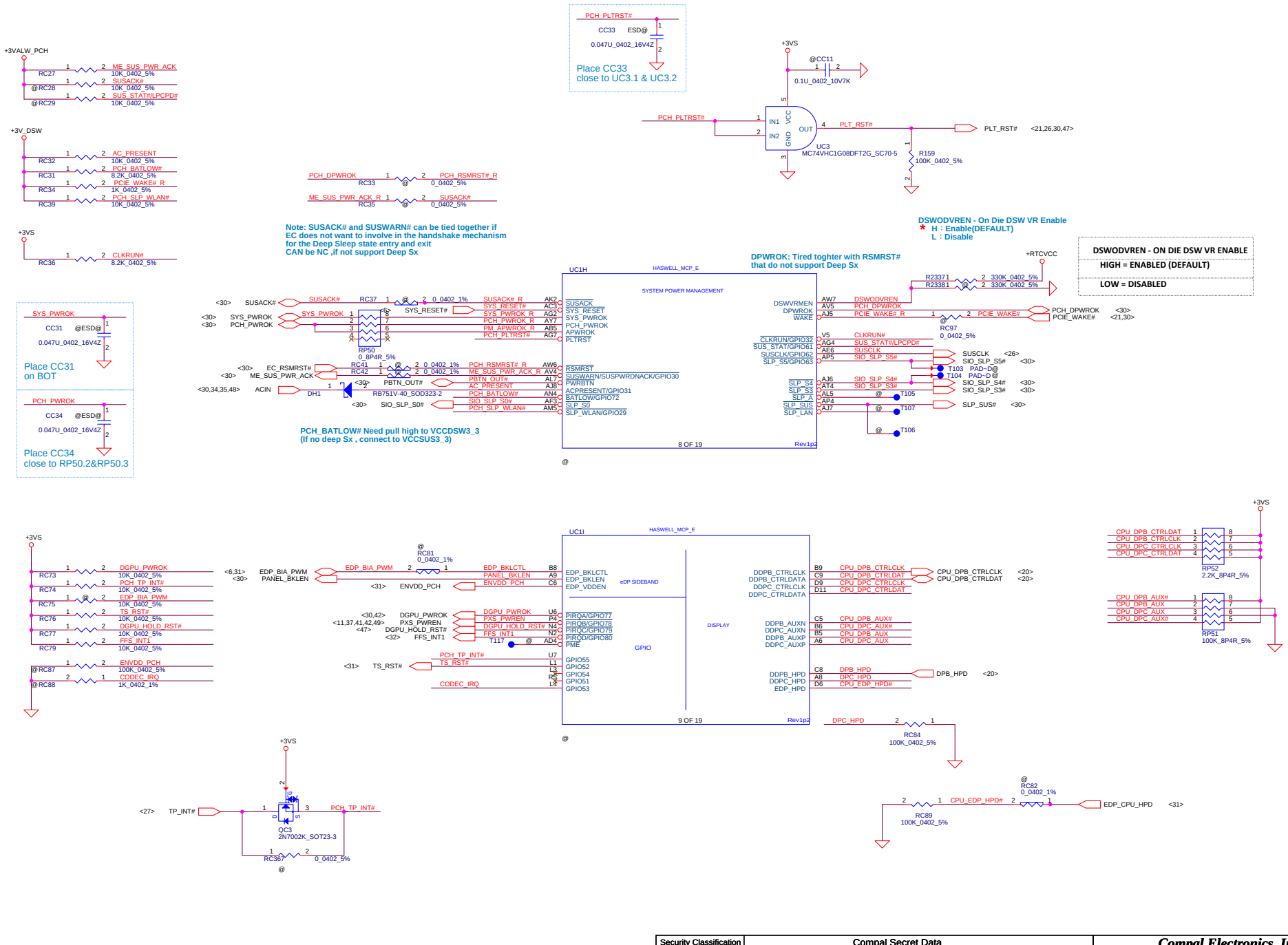
Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **MCP(6,7/19) CLK,SMB,SPI,LPC**

Size: A3 | Document Number: **LA-B015P** | Rev: 0.1

Date: Tuesday, September 16, 2014 | Sheet 9 of 56



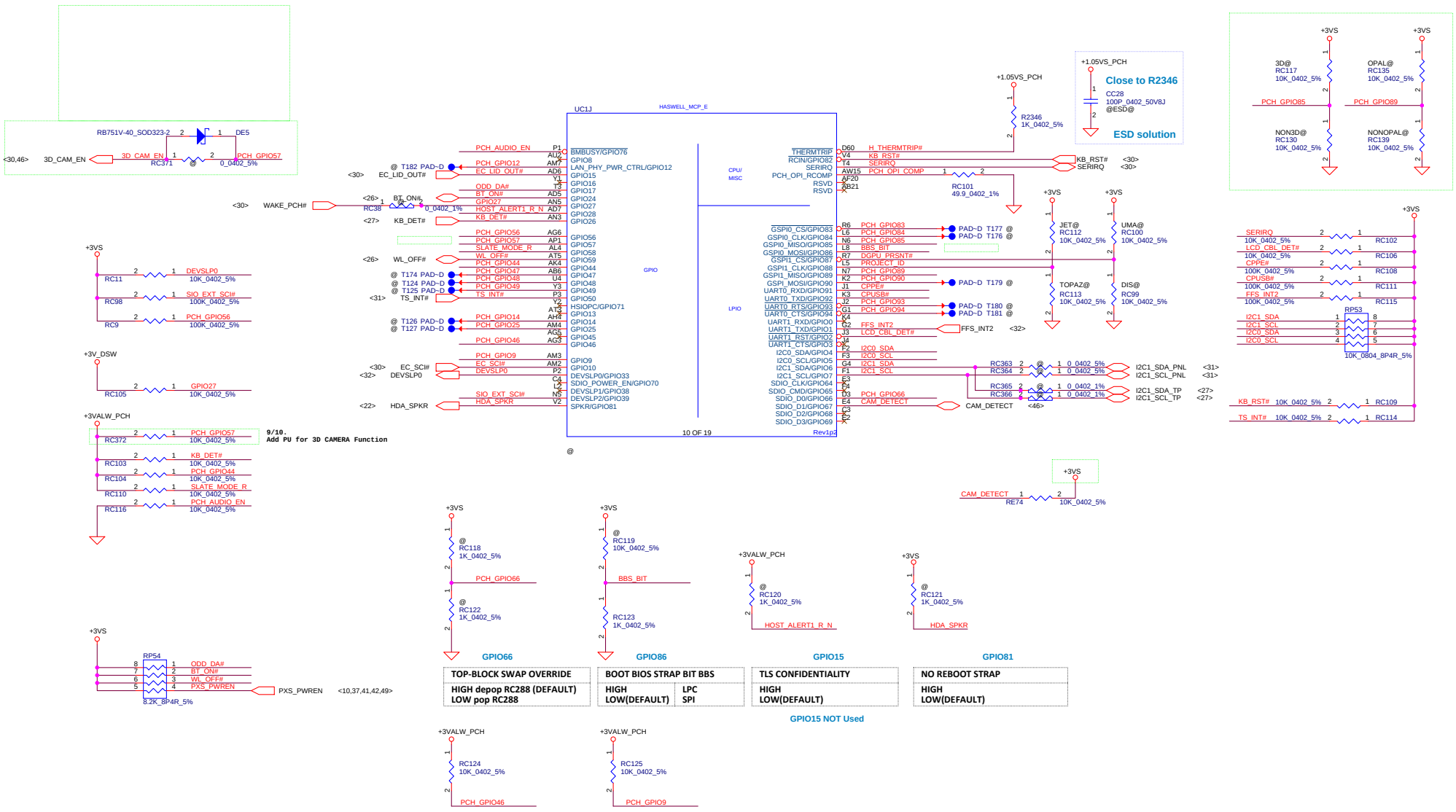
Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **MCP(8,9/19) DDI,EDP,GPIO**

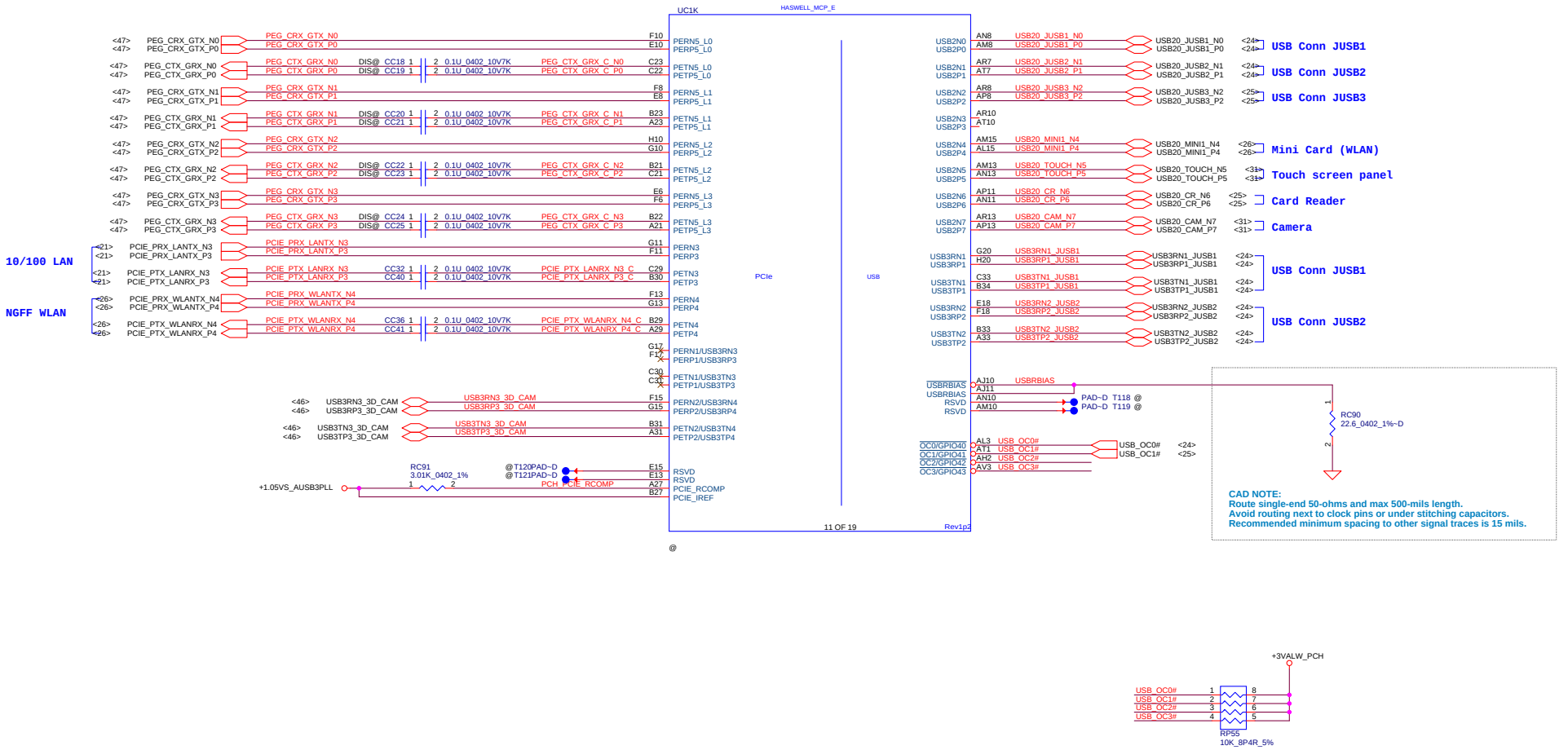
Size: Document Number: **LA-B015P** Rev: 0.1

Date: Wednesday, September 10, 2014 Sheet 10 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.	
Title	MCP(10/19) GPIO,LPIO,MISC
Size	Document Number: LA-B015P
Rev	0.1
Date:	Tuesday, September 16, 2014
Sheet	11 of 56



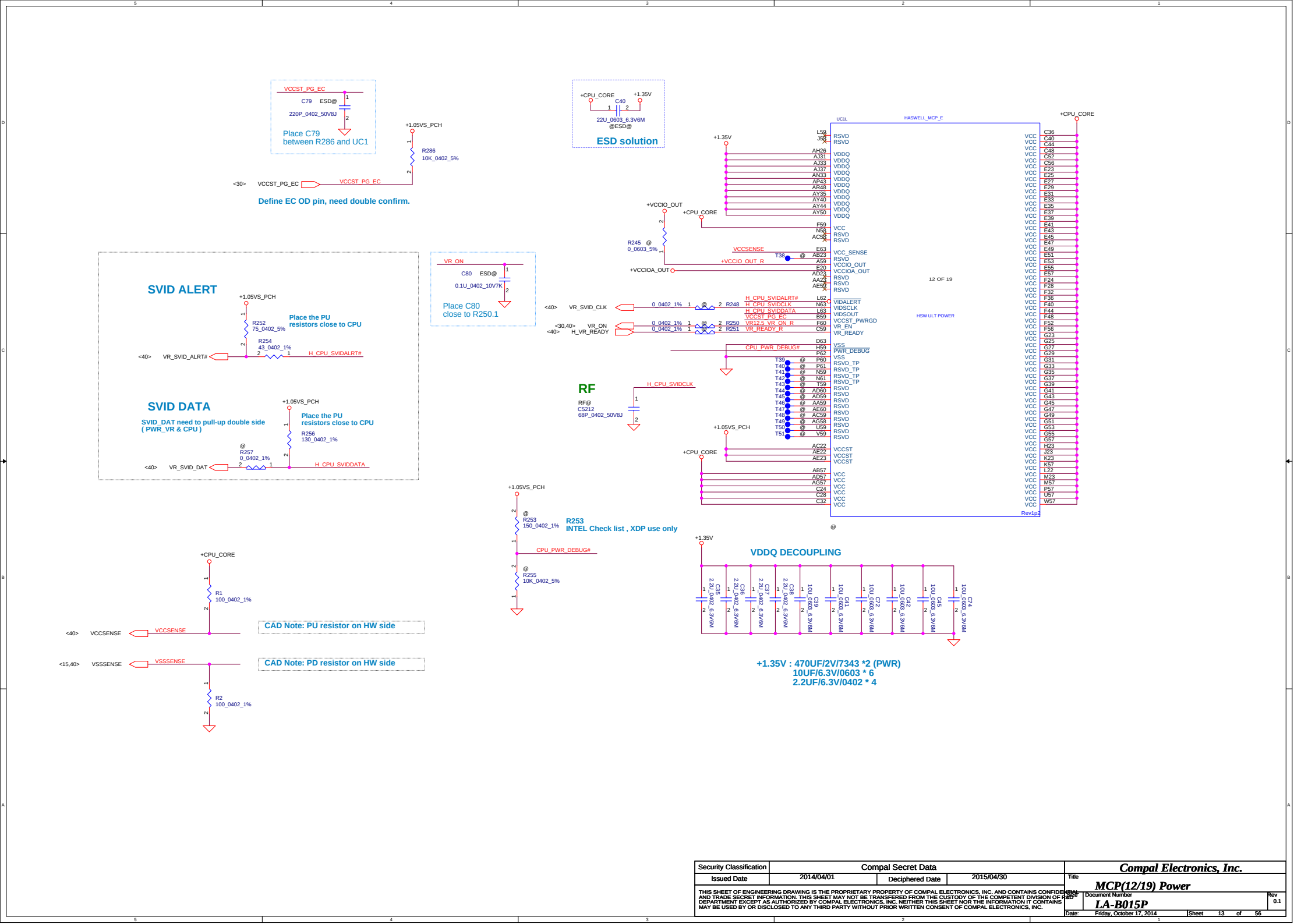
Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **MCP(11/19) PCIE,USB**

Size: A3 | Document Number: **LA-B015P** | Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 12 of 56



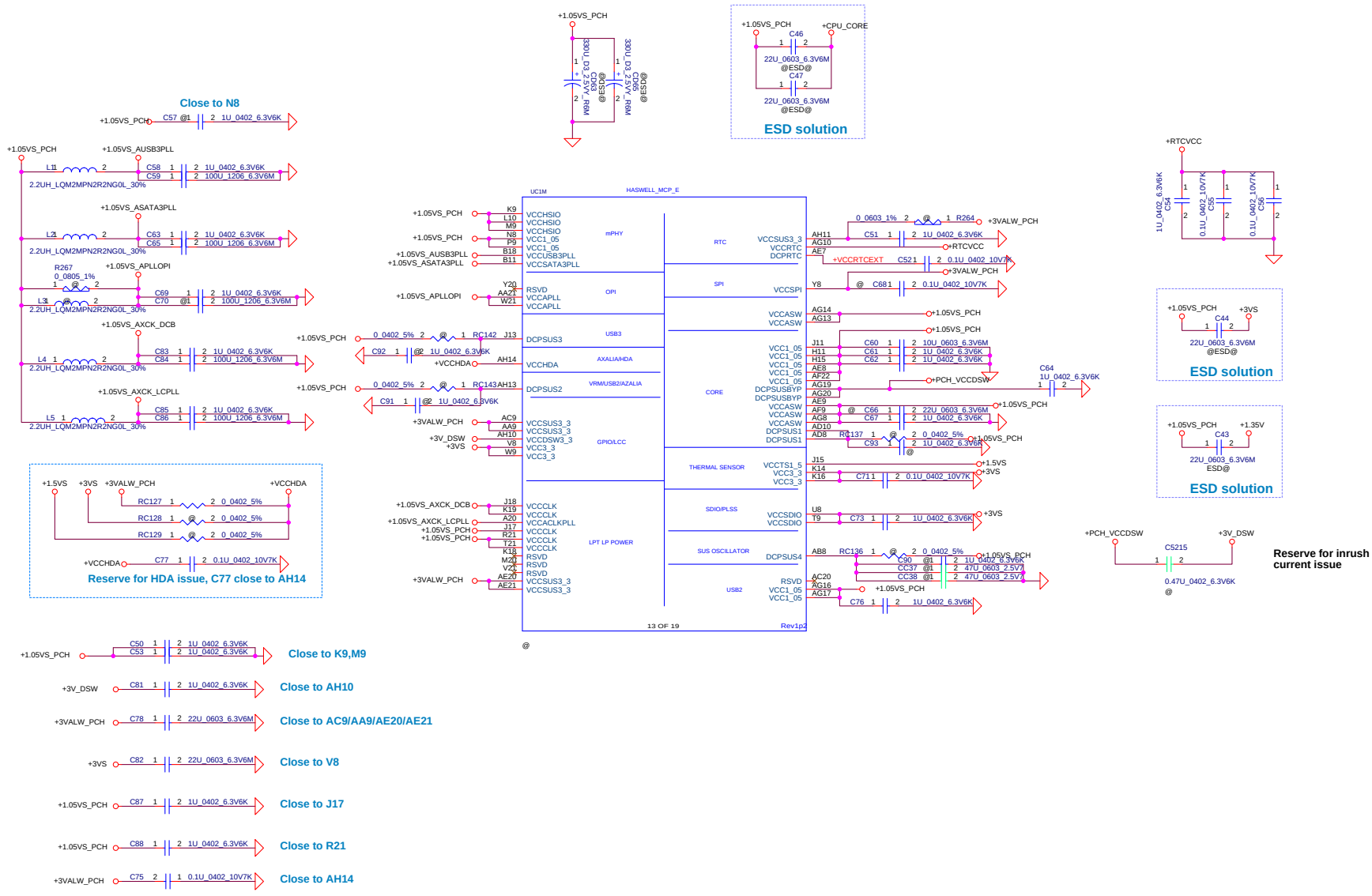
Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **MCP(12/19) Power**

Size: A3 | Document Number: **LA-B015P** | Rev: 0.1

Date: Friday, October 17, 2014 | Sheet 13 of 56



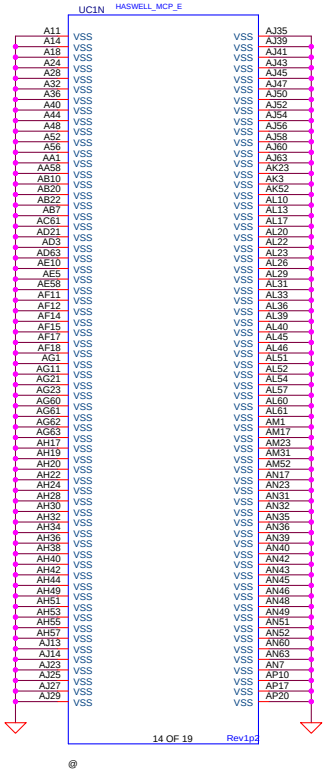
Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

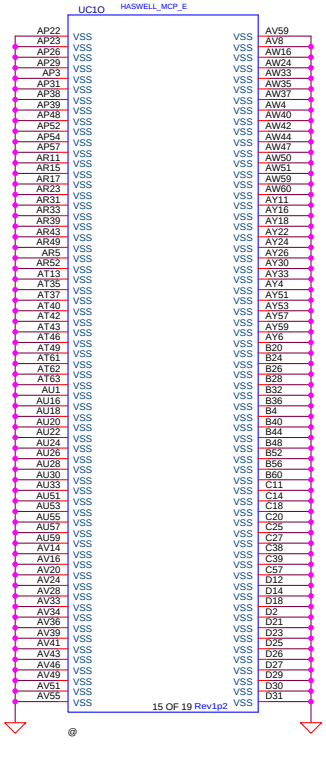
Compal Electronics, Inc.

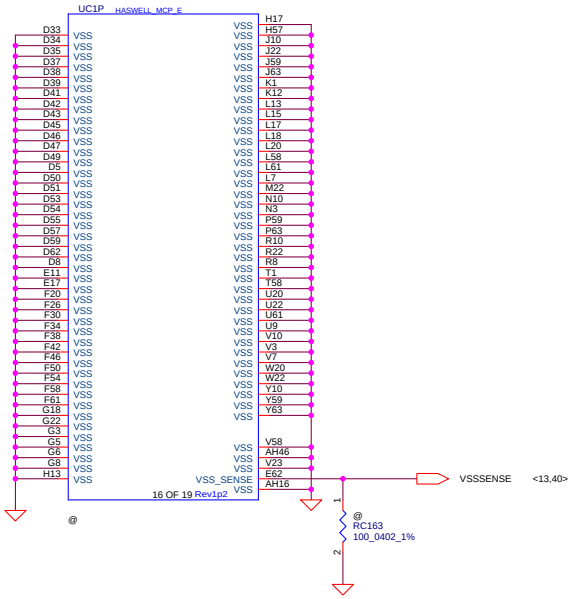
Title: **MCP(13/19) Power**

Size: A3 | Document Number: **LA-B015P** | Rev: 0.1

Date: Friday, October 17, 2014 | Sheet 14 of 56







CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

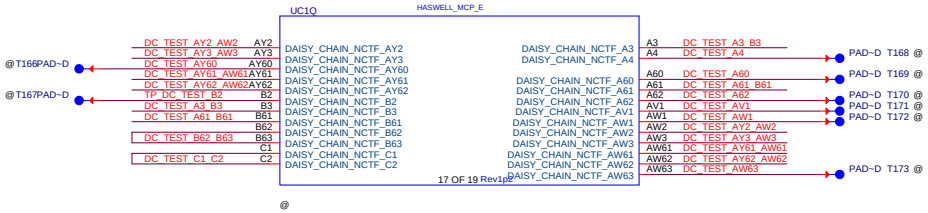
Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

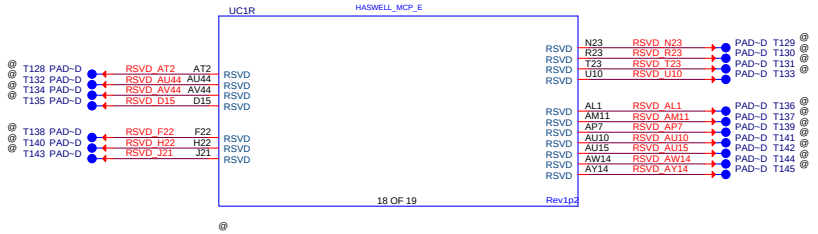
Compal Electronics, Inc.

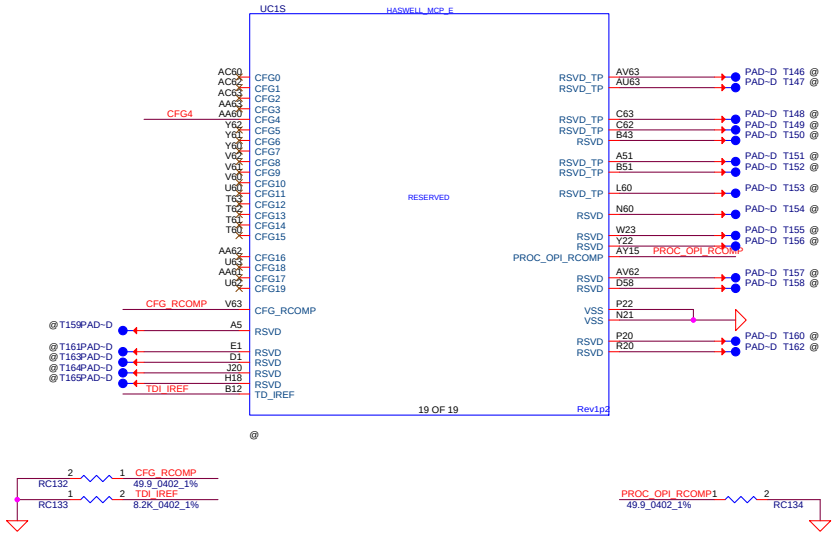
Title: MCP(14,15,16/19) VSS

Size: A3 | Document Number: LA-B015P | Rev: 0.1

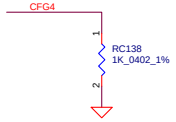
Date: Wednesday, September 10, 2014 | Sheet 15 of 56







CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: MCP(17,18,19/19) CFG,RSVD

Size: A3 | Document Number: LA-B015P | Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 16 of 56

H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM1

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMM1.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

DDR3L SODIMM ODT GENERATION

Place CC31 between QD2 and R2349

ESD solution

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: DDRIII DIMMA

Size: C | Document Number: LA-B015P | Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 17 of 56

H=4mm

2-3A to 1 DIMMs/channel

Populate RD4, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

<7> DDR_B_DQS#[0..7]
<7> DDR_B_D[0..63]
<7> DDR_B_DQS[0..7]
<7> DDR_B_MA[0..15]

Layout Note: Place near JDIMM2

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMM2.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

JDIMM2
BELLW_80011-1021
CONN@

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

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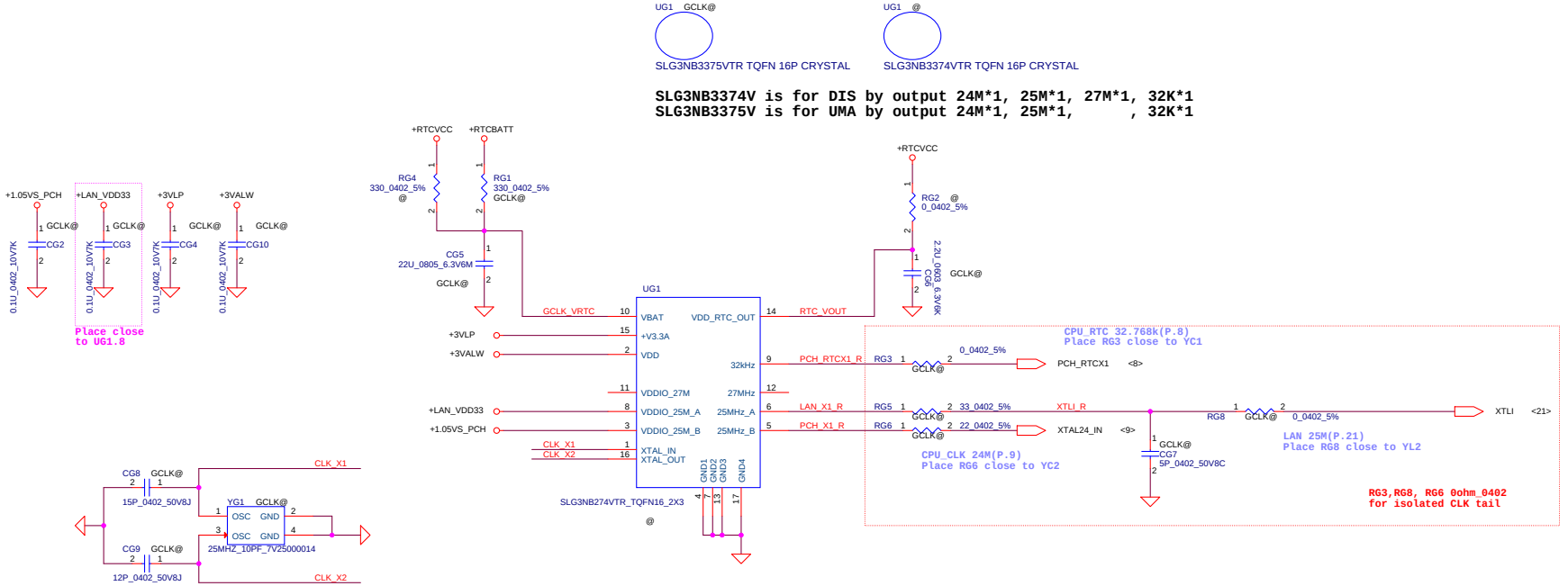
Compal Electronics, Inc.

Title: DDRIII DIMMB
Size: C
Document Number: LA-B015P
Rev: 0.1
Date: Wednesday, September 10, 2014
Sheet 18 of 56



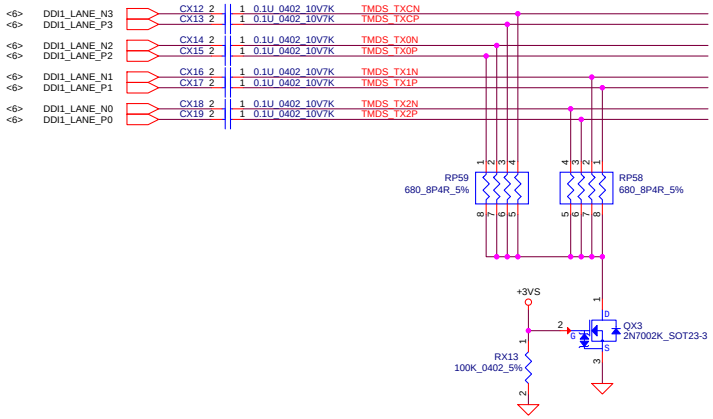
Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

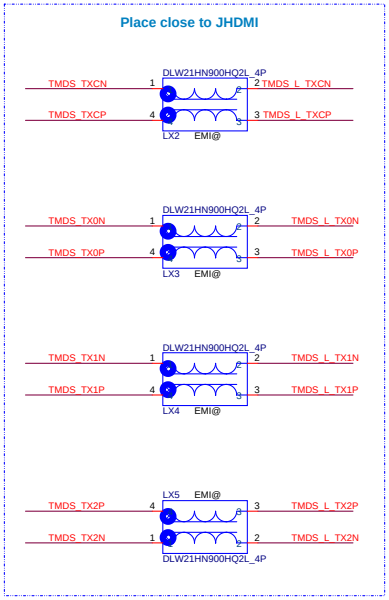
Compal Electronics, Inc.

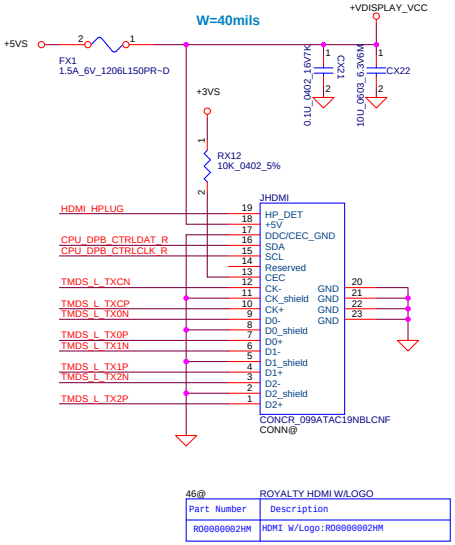
Title: **Green CLK**

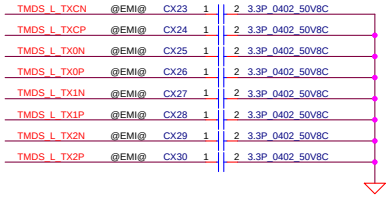
Size: C | Document Number: **LA-B015P** | Rev: 0.1

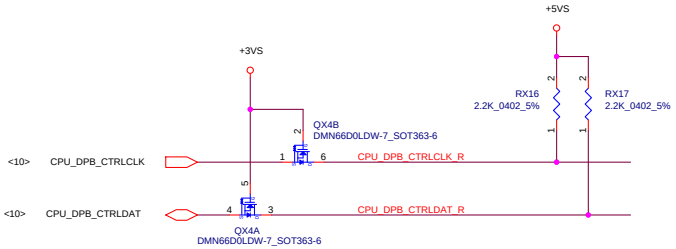
Date: Wednesday, September 10, 2014 | Sheet 19 of 56

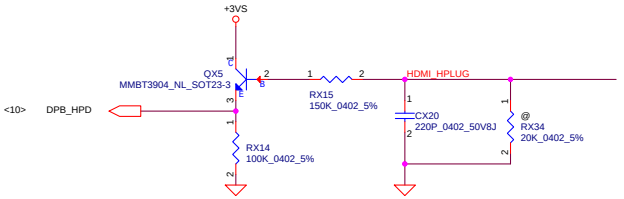












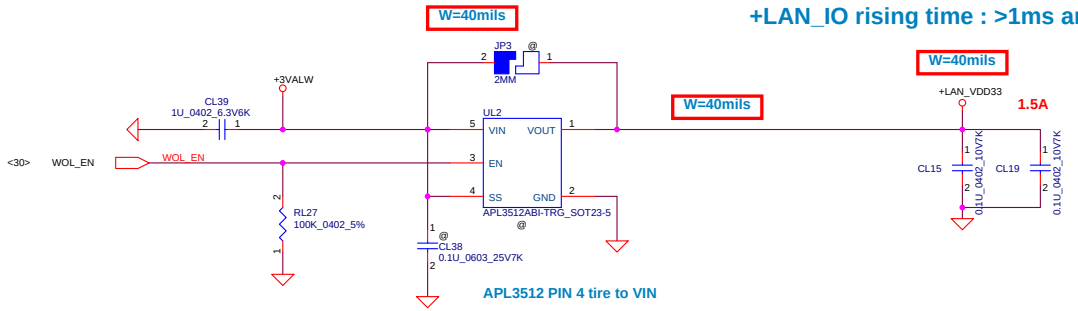
Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

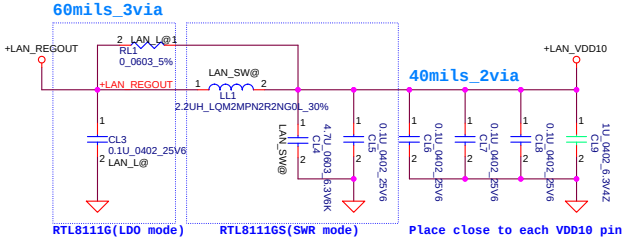
Title: HDMI

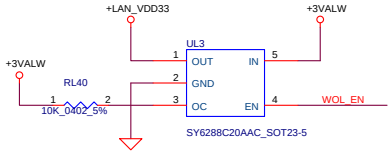
Size: C | Document Number: LA-B015P | Rev: 0.1

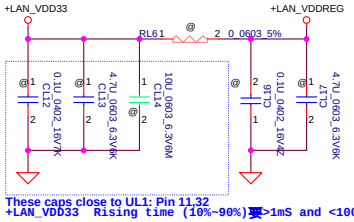
Date: Tuesday, September 16, 2014 | Sheet 20 of 56

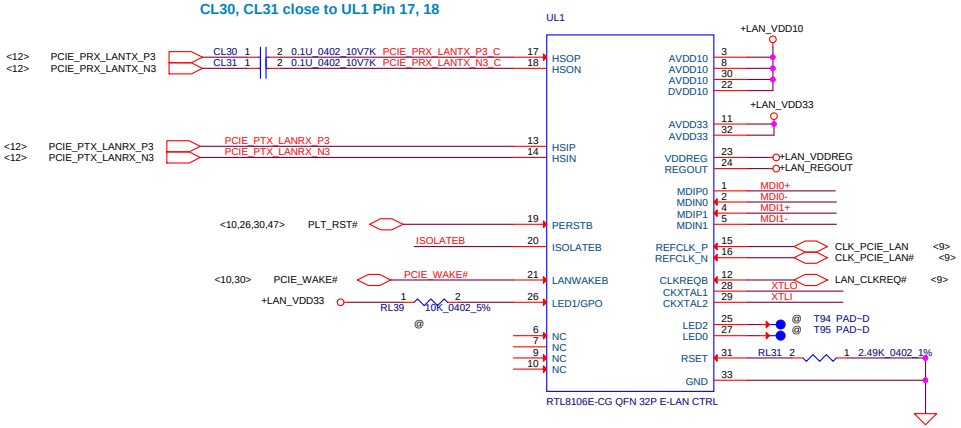


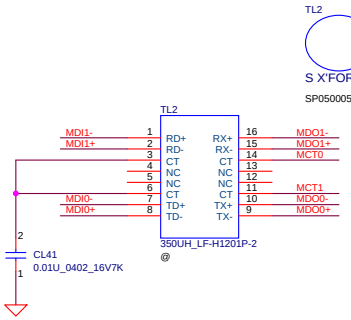
+LAN_IO rising time : >1ms and <100ms

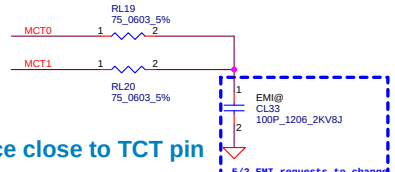


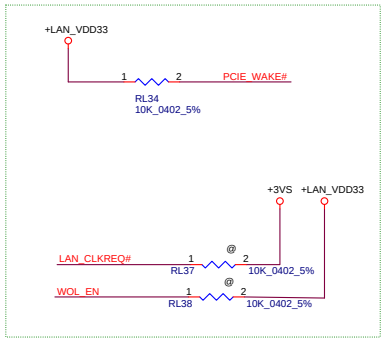


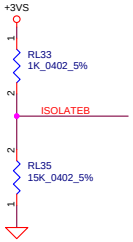


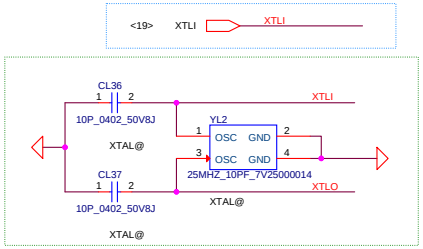


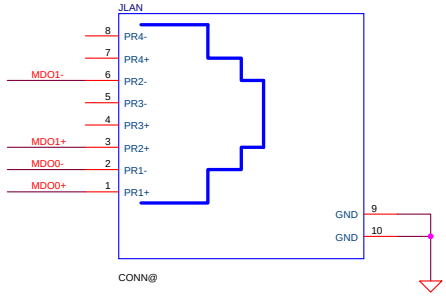












Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: 10/100 LAN

Size: Custom | Document Number: LA-B015P | Rev: 0.1

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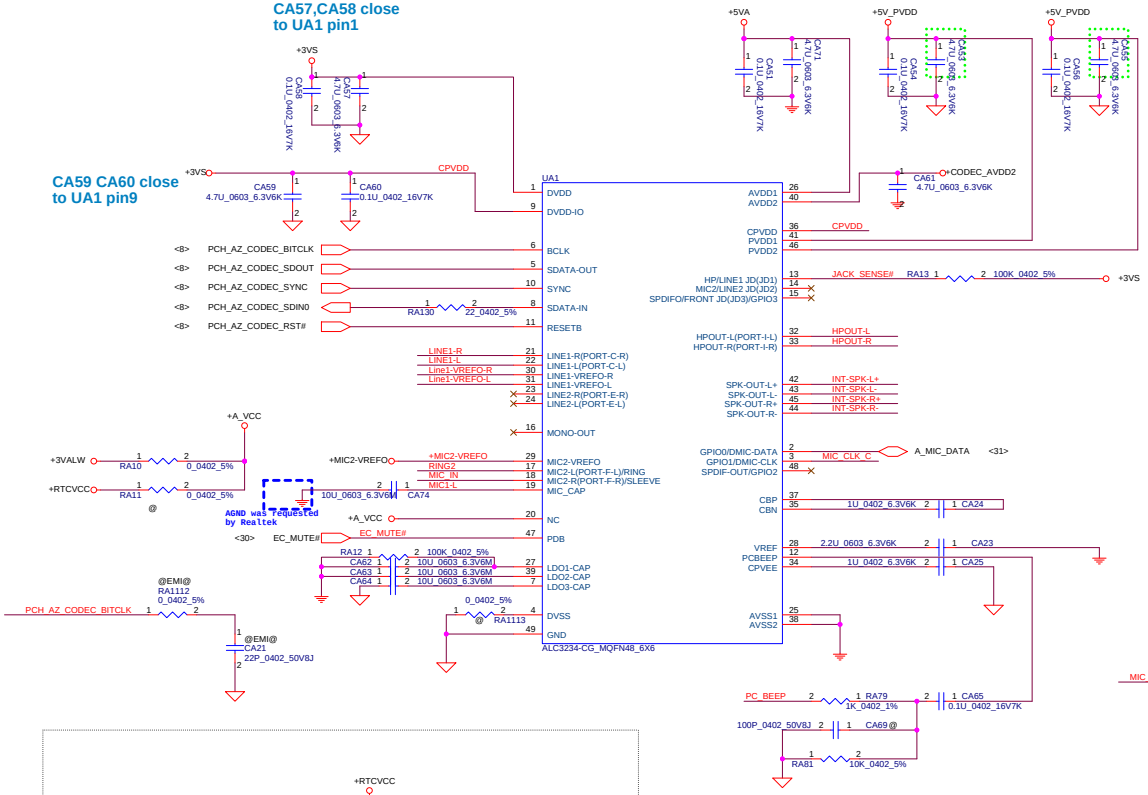
CA71, CA51 place close to Pin 26

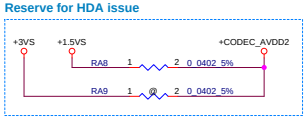
CA53, CA55 change Value from 10U_0603_6.3V6M~D to 4.7U_0603_6.3V6K

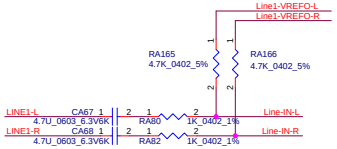
CA57,CA58 close to UA1 pin1

CA59 CA60 close to UA1 pin9

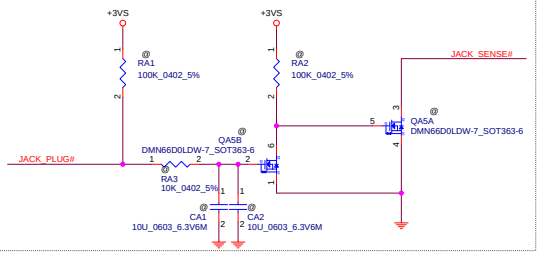


Reserve for HDA issue

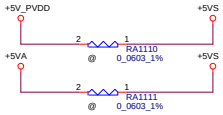


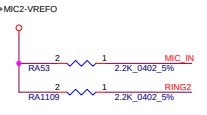


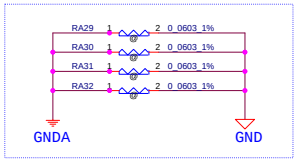
JACK_PLUG Delay circutis



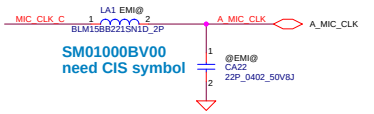
Reserve for cancel Delay circutis



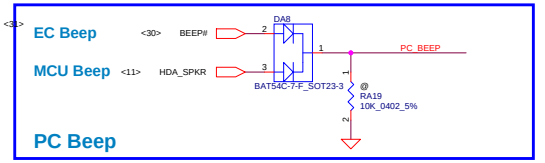


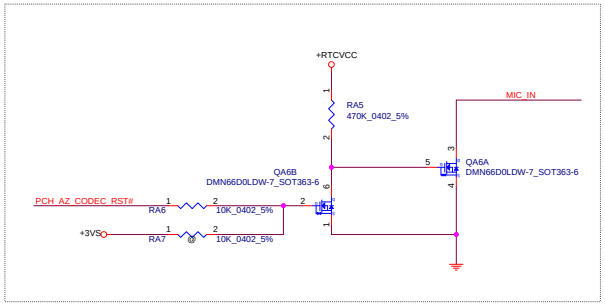


Place on the moat between GND & GNDA.



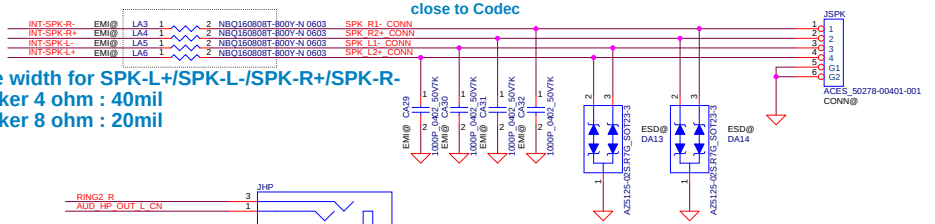
SM01000BV00 need CIS symbol





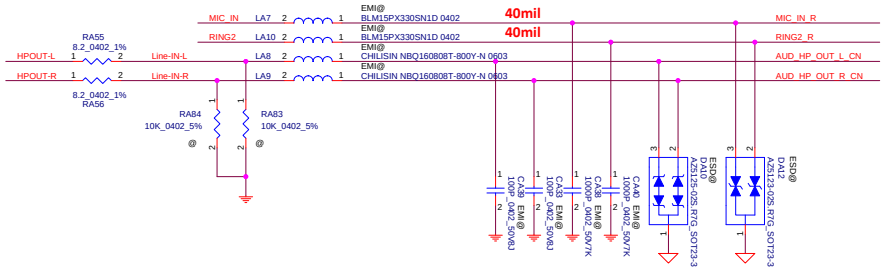
Close to UA1 Pin11,13,14,16

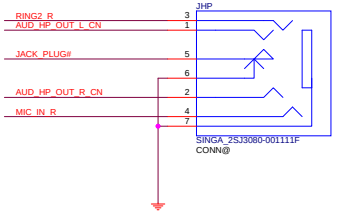
close to Codec



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

iPhone and Nokia type Combo Jack





Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: Audio Codec ALC3234

Document Number: LA-B015P

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Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **Reserved Page**

Size: | Document Number: **LA-B015P** | Rev: 0.1

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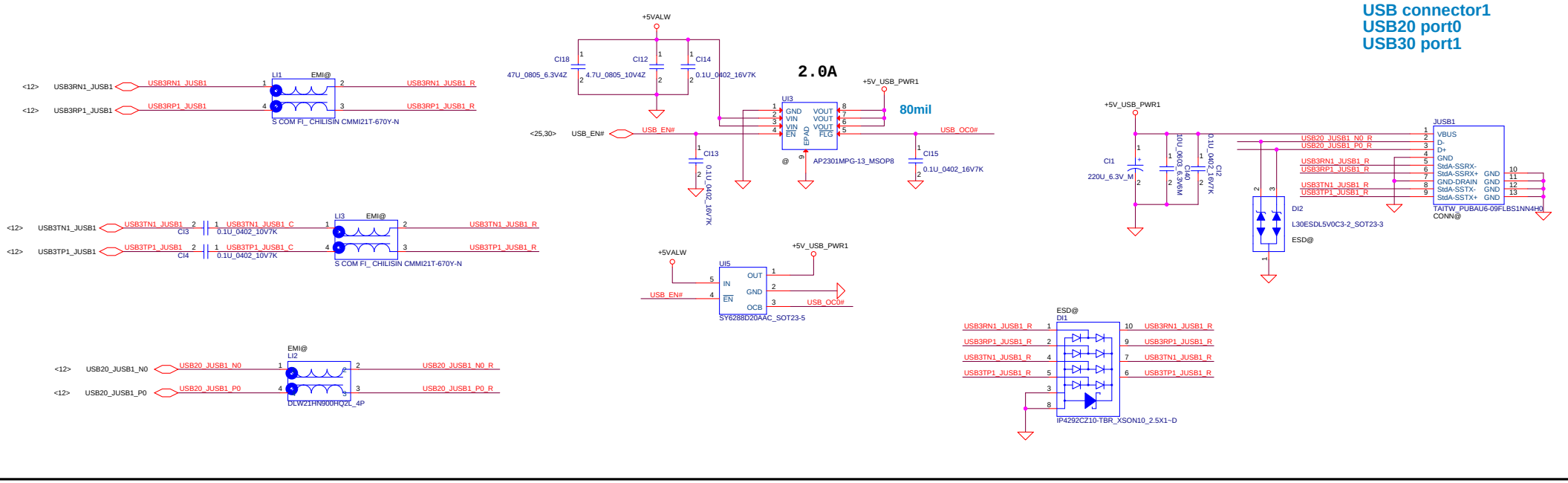
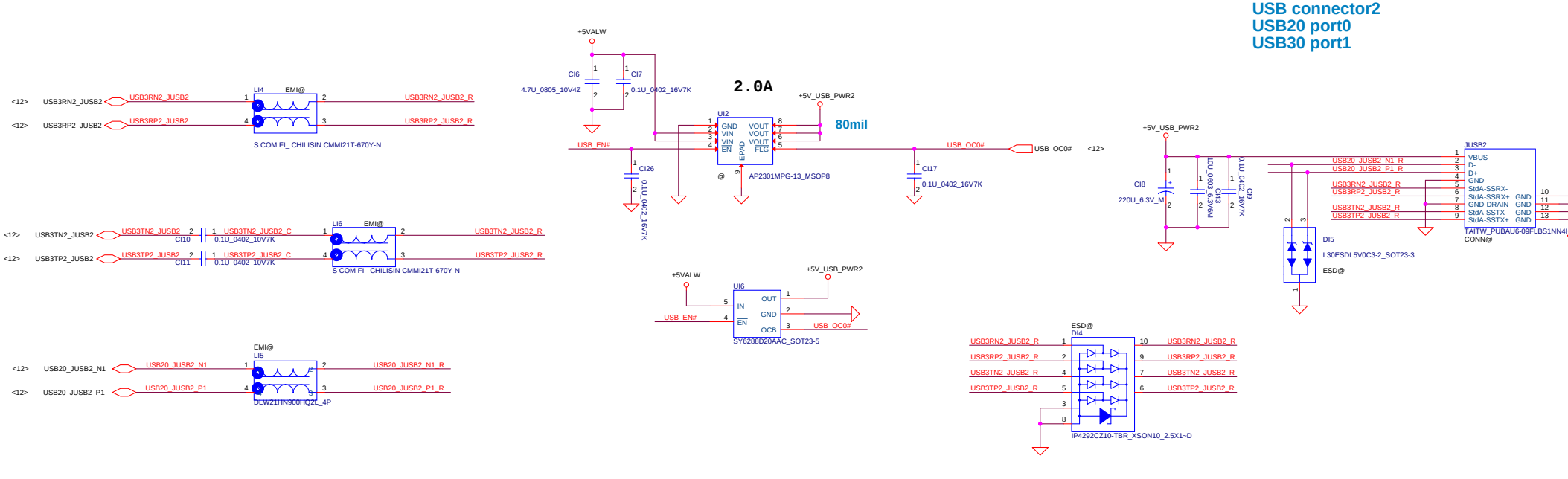




Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

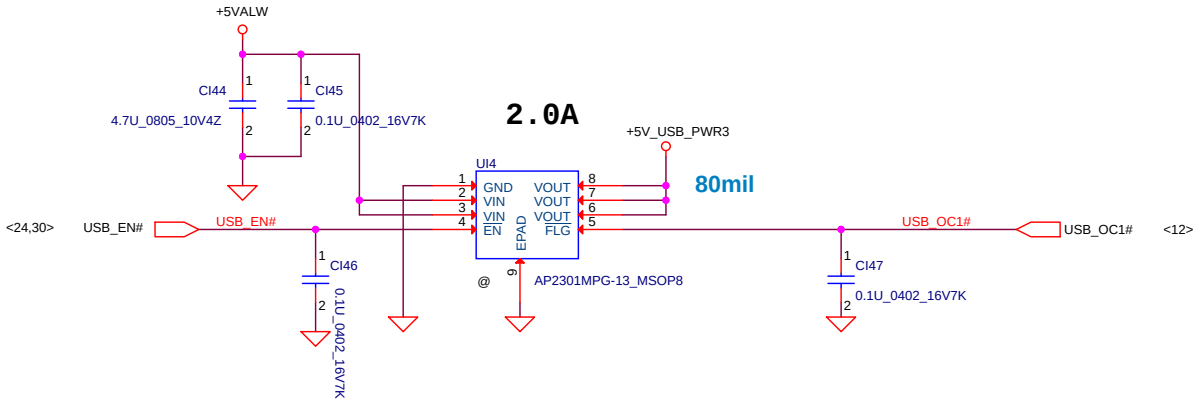
Compal Electronics, Inc.

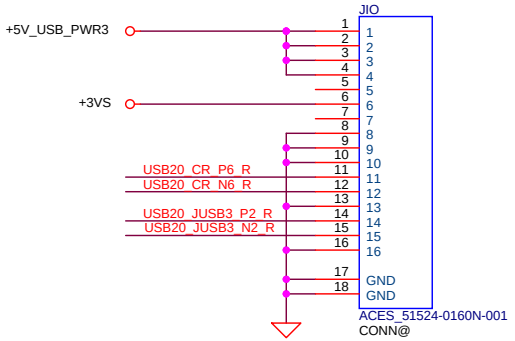
Title: **USB3.0**

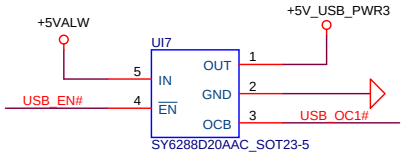
Size: C | Document Number: **LA-B015P** | Rev: 0.1

Date: Tuesday, September 16, 2014 | Sheet 24 of 56

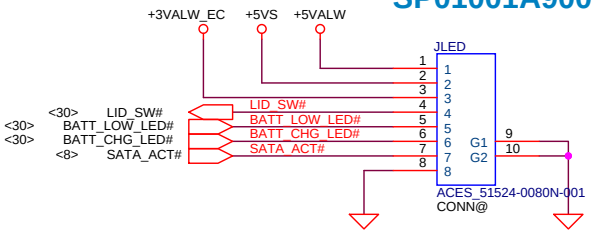
IO to MB CONN
Substitute:SP01001FS00

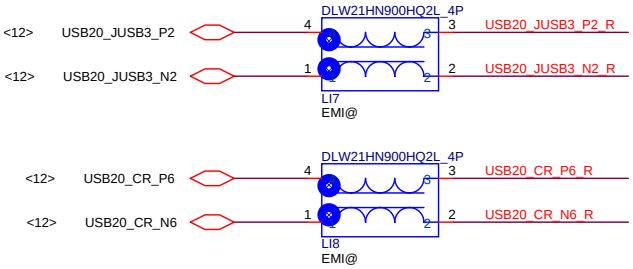






LED/B TO M/B
SP01001A900





Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

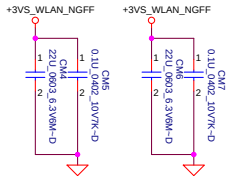
Title: *IO/B, LED/B*

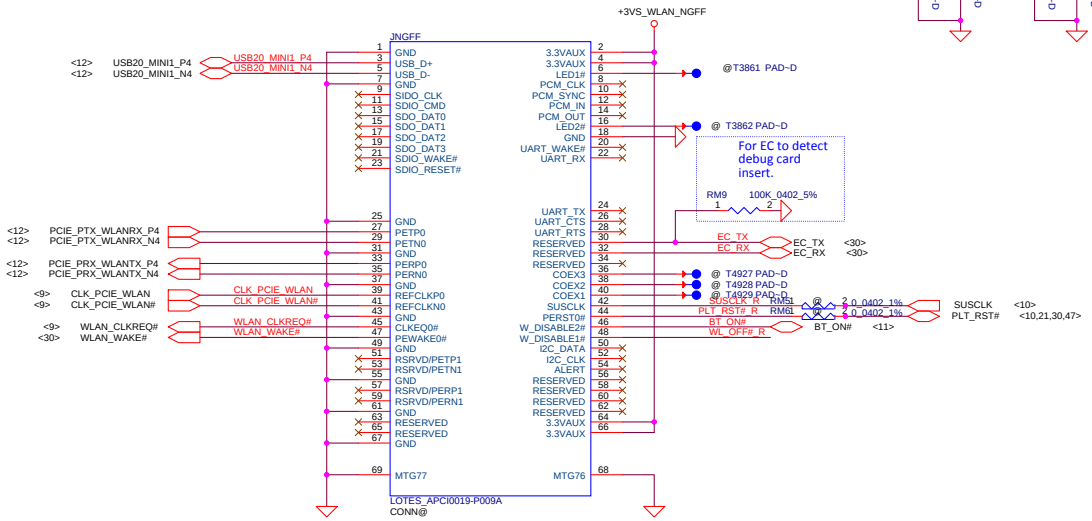
Size: B | Document Number: *LA-B015P* | Rev: 0.1

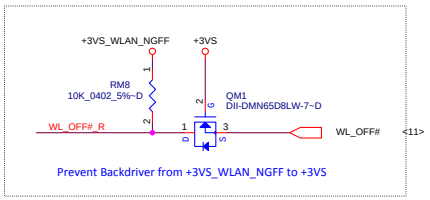
Date: Tuesday, September 16, 2014 | Sheet 25 of 56

NGFF WL Con (E Key)

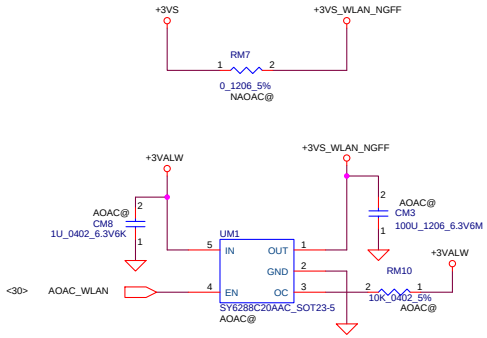
closed to pin 2, 4 closed to pin 64, 66







+3VALW TO +3VS_WLAN_NGFF



Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: NGFF WLAN

Size: A3 | Document Number: LA-B015P | Rev: 0.1

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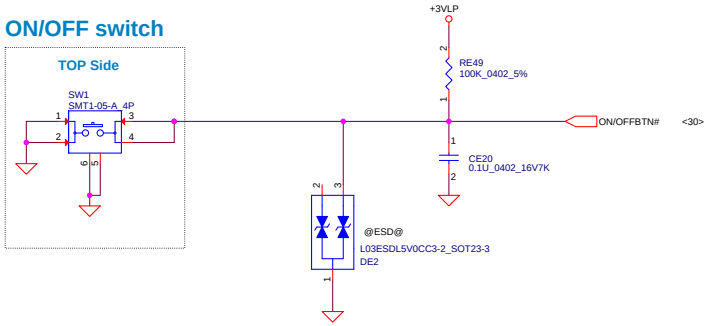
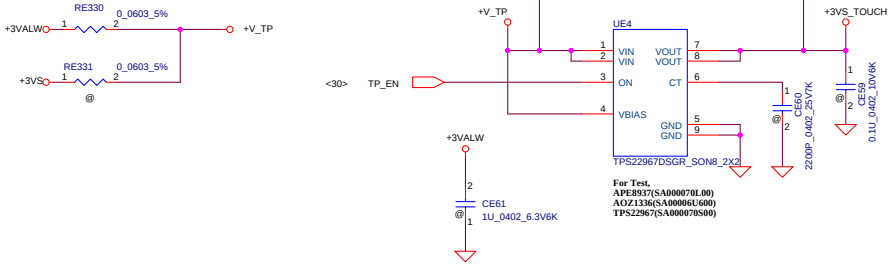
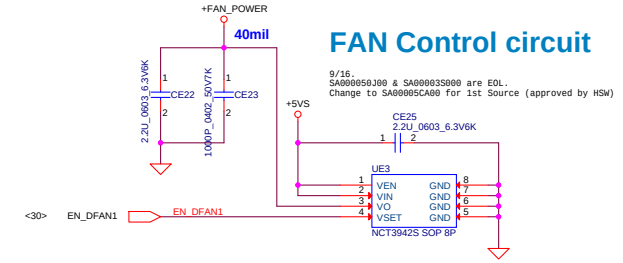
Power ON Circuit

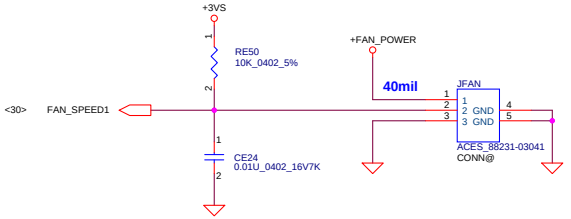
ON/OFF switch



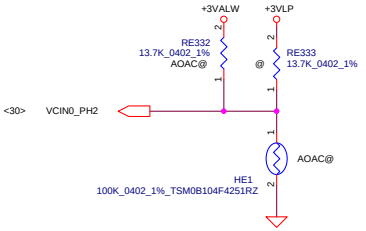


FAN Control circuit

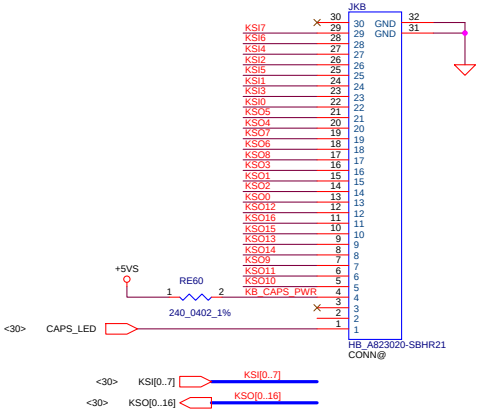




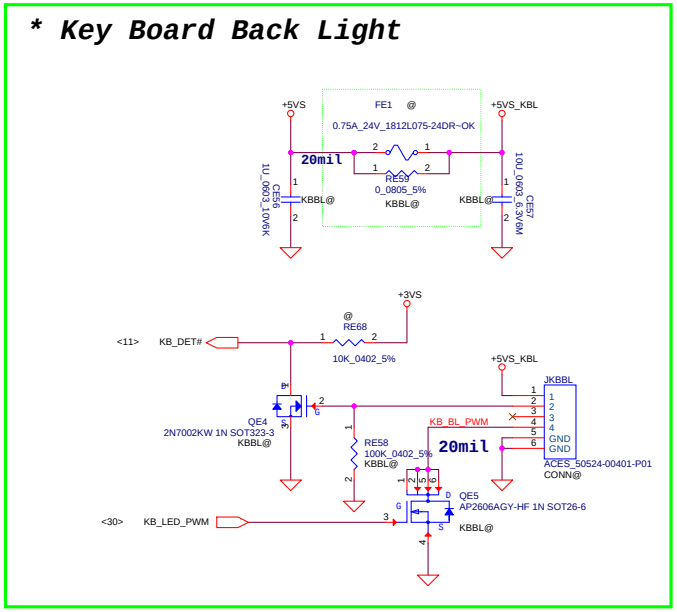
HE1 place around FAN area.



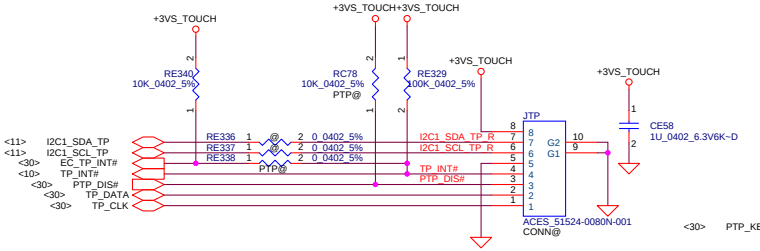
INT_KBD Connector



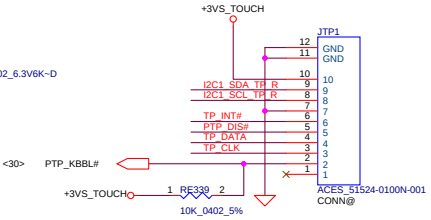
* Key Board Back Light

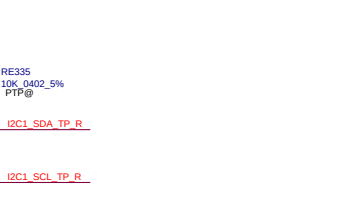


Touch pad



PTP





Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: FAN / TP / PWR SW / KBBL

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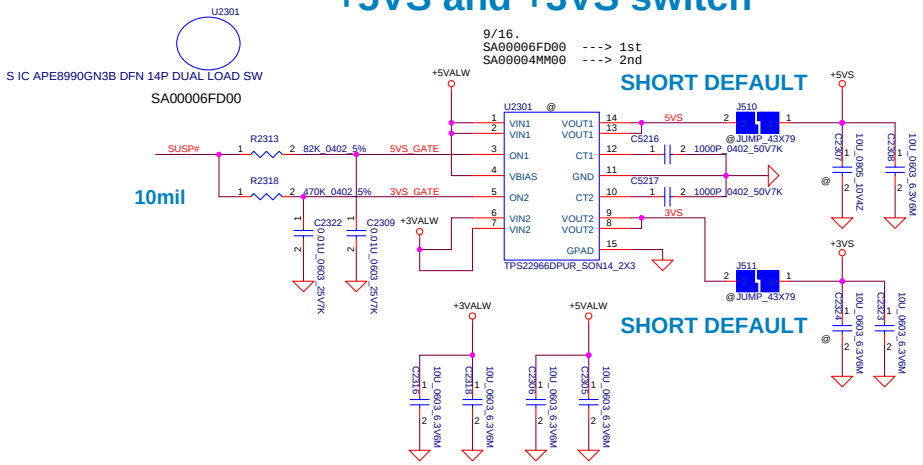
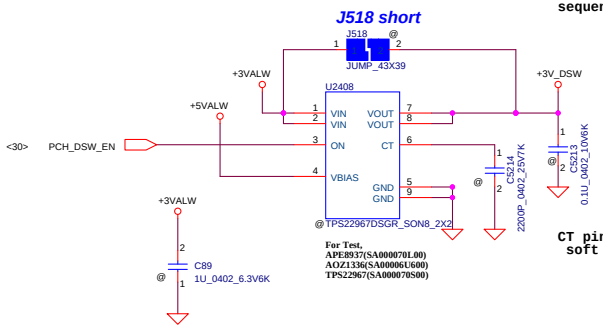
+5VS and +3VS switch



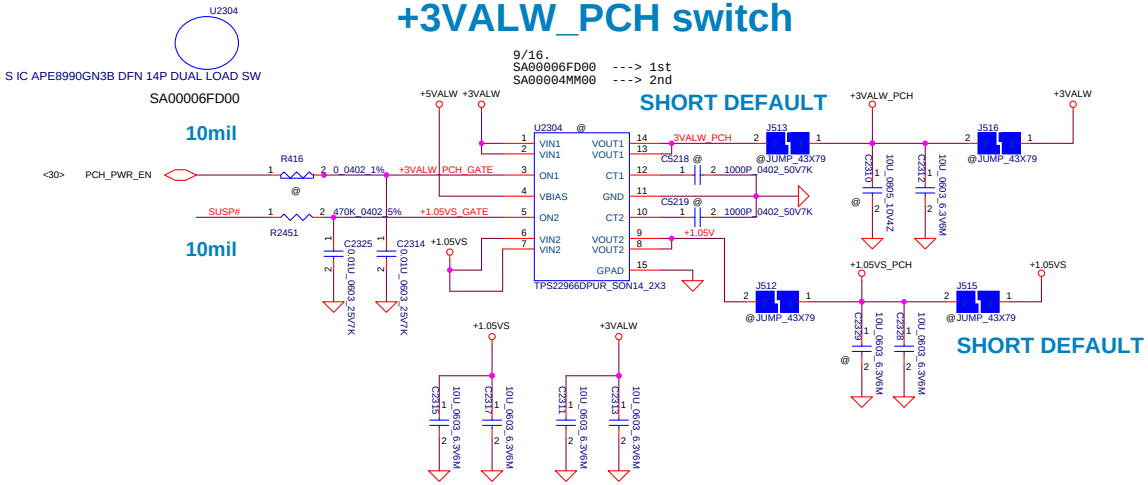
+3VALW TO +3V_DSW

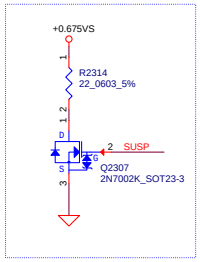


+3V_DSW have soft start sequence: +3V_DSW stable > +3VALW_PCH > 0ms

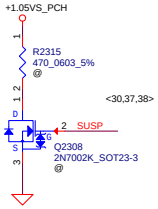
CT pin use 2200pf for soft start tuning

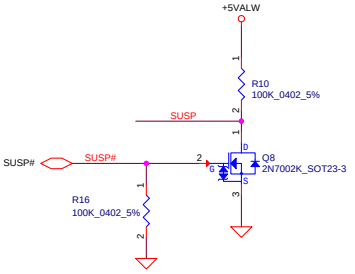
+3VALW_PCH switch





For Intel S3 Power Reduction





Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **DC/DC Interface**

Size: C | Document Number: **LA-B015P** | Rev: 0.1

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Screw Hole

ZZZ

PCB 13G LA-B015P REV0 M/B

DA80011D000

H1 H_2P8N @
H20 H_2P8N @
H21 H_2P8N @
H22 H_2P8X3P3N @
H23 H_2P8X4P8N @

H2 H_2P8 @
H3 H_2P8 @
H4 H_2P8 @
H5 H_2P8 @
H6 H_2P8 @
H7 H_2P8 @
H8 H_2P8 @
H9 H_2P8 @

H10 Delete.
Layout informed PCB vendor to do PTH solution.
(Function is same as beofre.)

H11 H_2P8 @
H12 H_2P8 @

H13 H_3P6 @
H14 H_3P6 @
H15 H_3P6 @
H16 H_3P6 @

CPU bracket

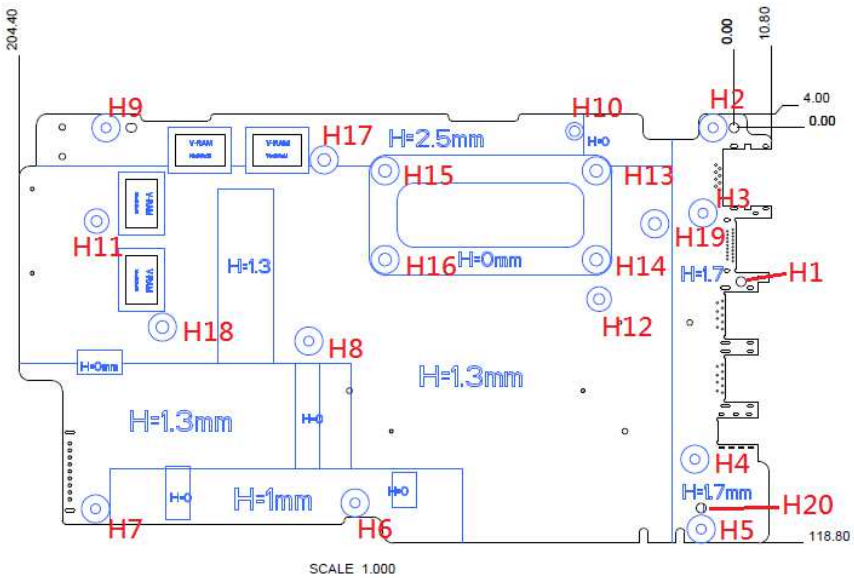
H17 H_3P3 @
H18 H_3P3 @

VGA stand-off

H19 H_3P3 @

NGFF stand-off

FD1 @FIDUCAL
FD2 @FIDUCIAL
FD3 @FIDUCAL
FD4 @FIDUCIAL



SCALE 1.000

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **Screw Hole**

Size | Document Number: **LA-B015P** | Rev: 0.1

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SD034120280	12K_0402_1%
SD034270280	27K_0402_1%
SD034430280	43K_0402_1%
SD034560280	56K_0402_1%
SD034750280	75K_0402_1%
SD034100380	100K_0402_1%
SD034130380	130K_0402_1%
SD034160380	160K_0402_1%
SD034200380	200K_0402_1%
SD028430380	430K_0402_1%
SD034150280	15K_0402_1%
SD034330280	33K_0402_1%
SD028200280	20K_0402_1%

Board ID

Place CC30 close to RC51.1

PWM Output

AD Input

DA Output

PS2 Interface

Int. K/B Matrix

SPI Device Interface

SPI Flash ROM

GPIO

SM Bus

GPO

GPI

Reserve for ESD

Please close to EC

Reserve for abnormal shutdown

Place CE34 between DE1 and RE12

Place CE35 between DE1 and UE1

Place DE1 close to UE1

Place CE30,CE31,CE32 close to UE1

20mil

KB9012A3 change to KB9012A4 SA00004OB30

ME_FWP PCH has internal 20K PD. (suspend power rail)

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

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Compal Electronics, Inc.

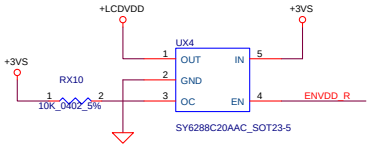
Title: EC ENE-KB9012

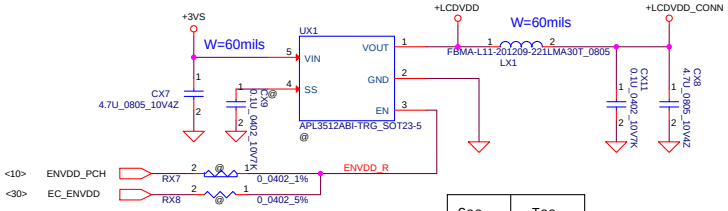
Size: Document Number: LA-B015P

Rev: 0.1

Date: Friday, October 17, 2014 Sheet 30 of 56

LCD PWR CTRL

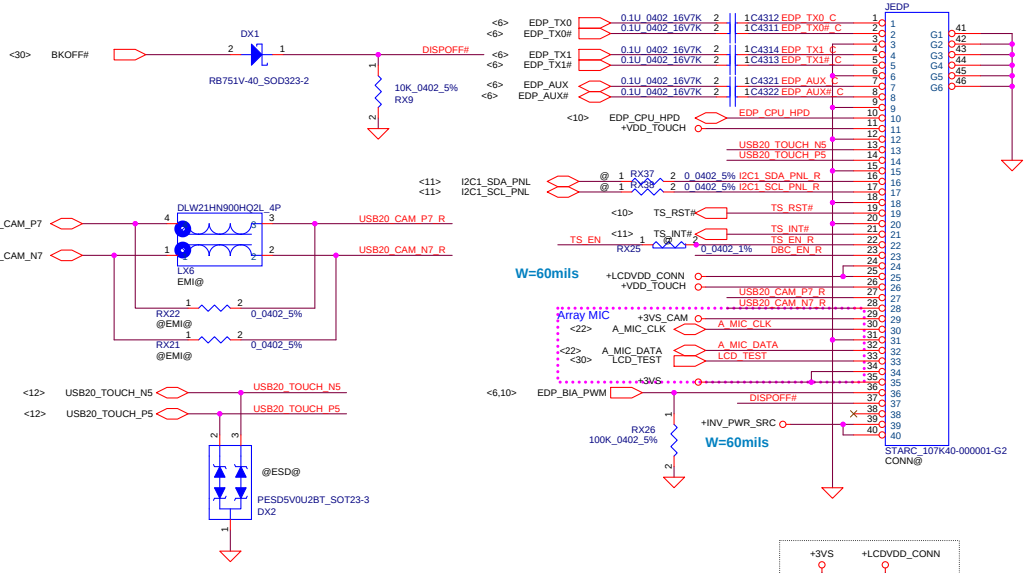


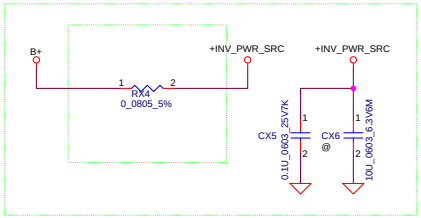


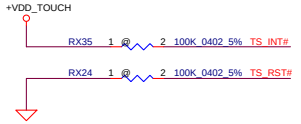
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

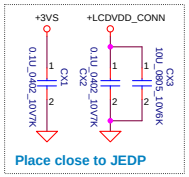
SS table

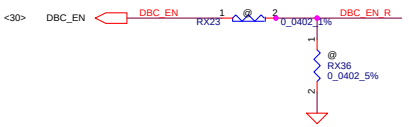
eDP Connector



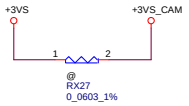




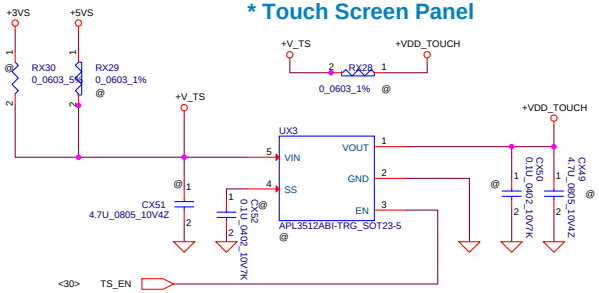


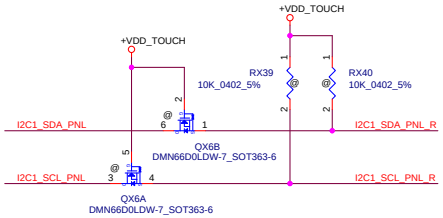


Webcam PWR CTRL



* Touch Screen Panel





Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: eDP / webcam / TouchScreen

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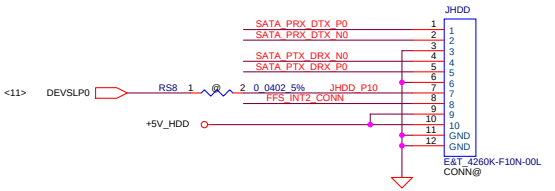
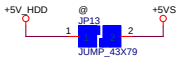
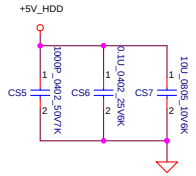
SATA HDD Connector

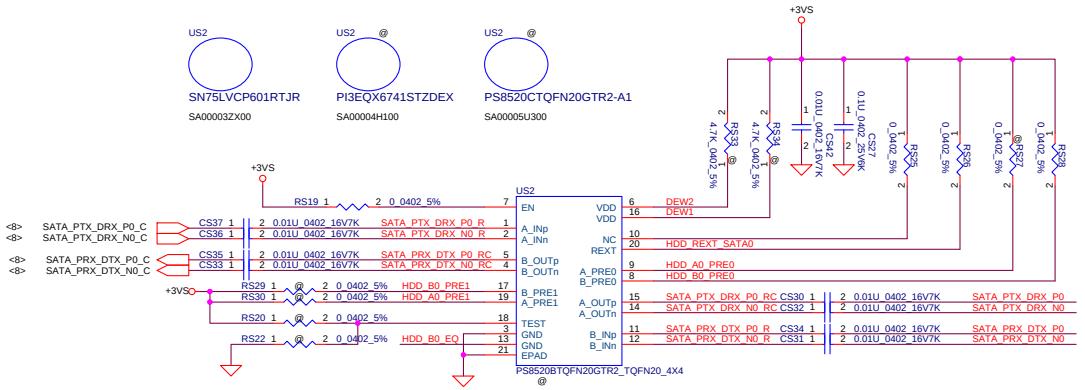


+5V_HDD Source

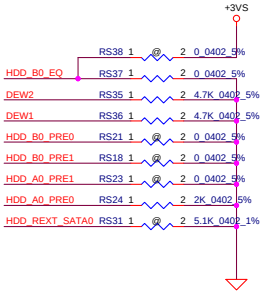


SHORT DEFAULT

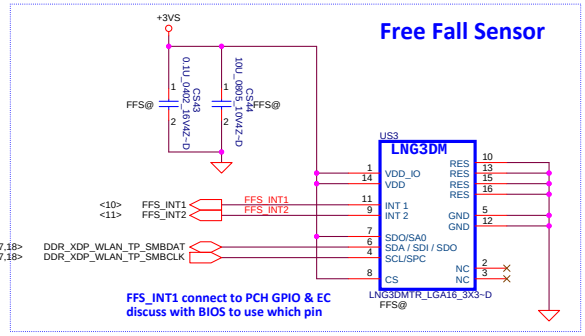


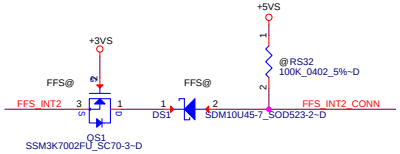


	US2	RS35	RS36	RS18	RS22	RS23	RS24	RS28
TI	SA00003ZX00	4.7K	4.7K	NC	NC	NC	2K	V
PARADE	SA00007TU00	7.5K	NC	V	V	V	NC	NC



Free Fall Sensor





Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

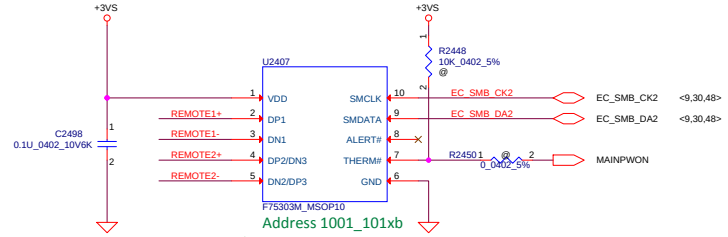
Compal Electronics, Inc.

Title: HDD / Free Fall Sensor

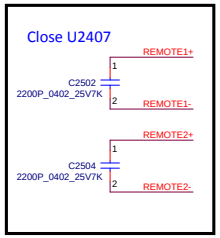
Size: C | Document Number: LA-B015P | Rev: 0.1

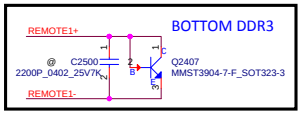
Date: Wednesday, September 10, 2014 | Sheet 32 of 56

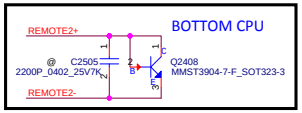
Fintek thermal sensor
placed near by TOP DDR3



2nd source
SA000029210-->EMC1403-2-AIZL-TR







REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **Thermal Sensor**

Size: | Document Number: **LA-B015P** | Rev: 0.1

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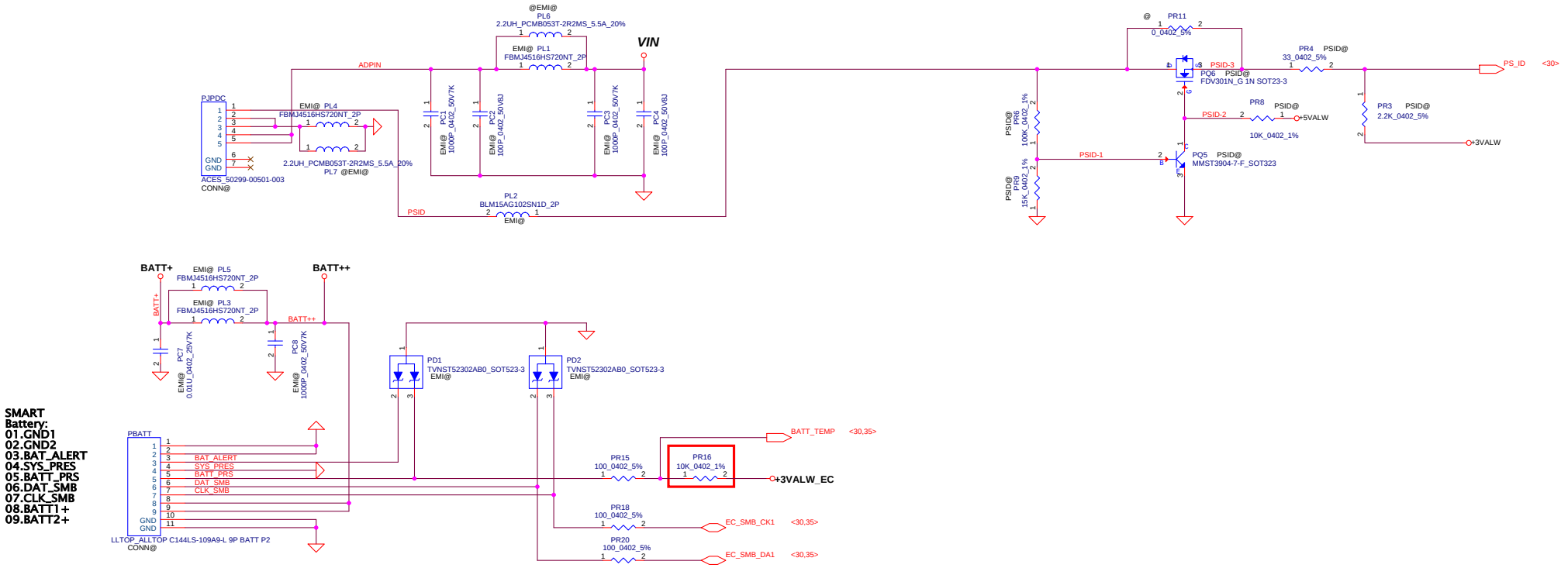
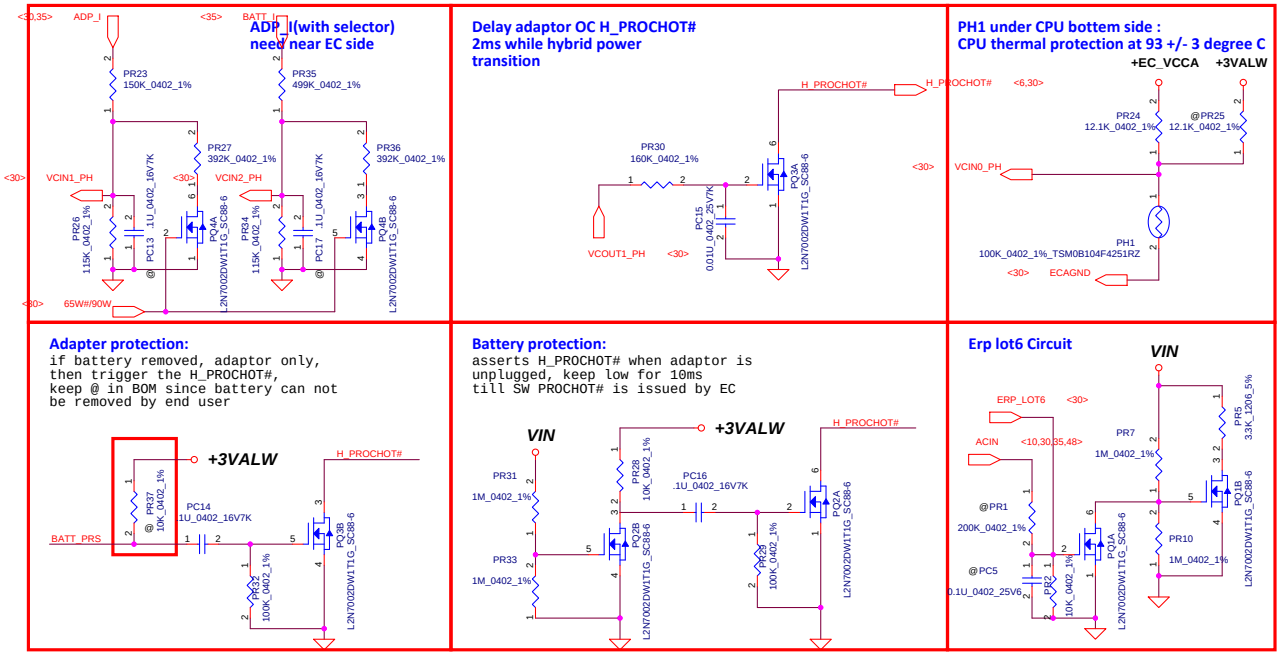
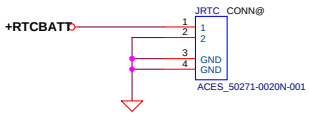


Other component (37.1)





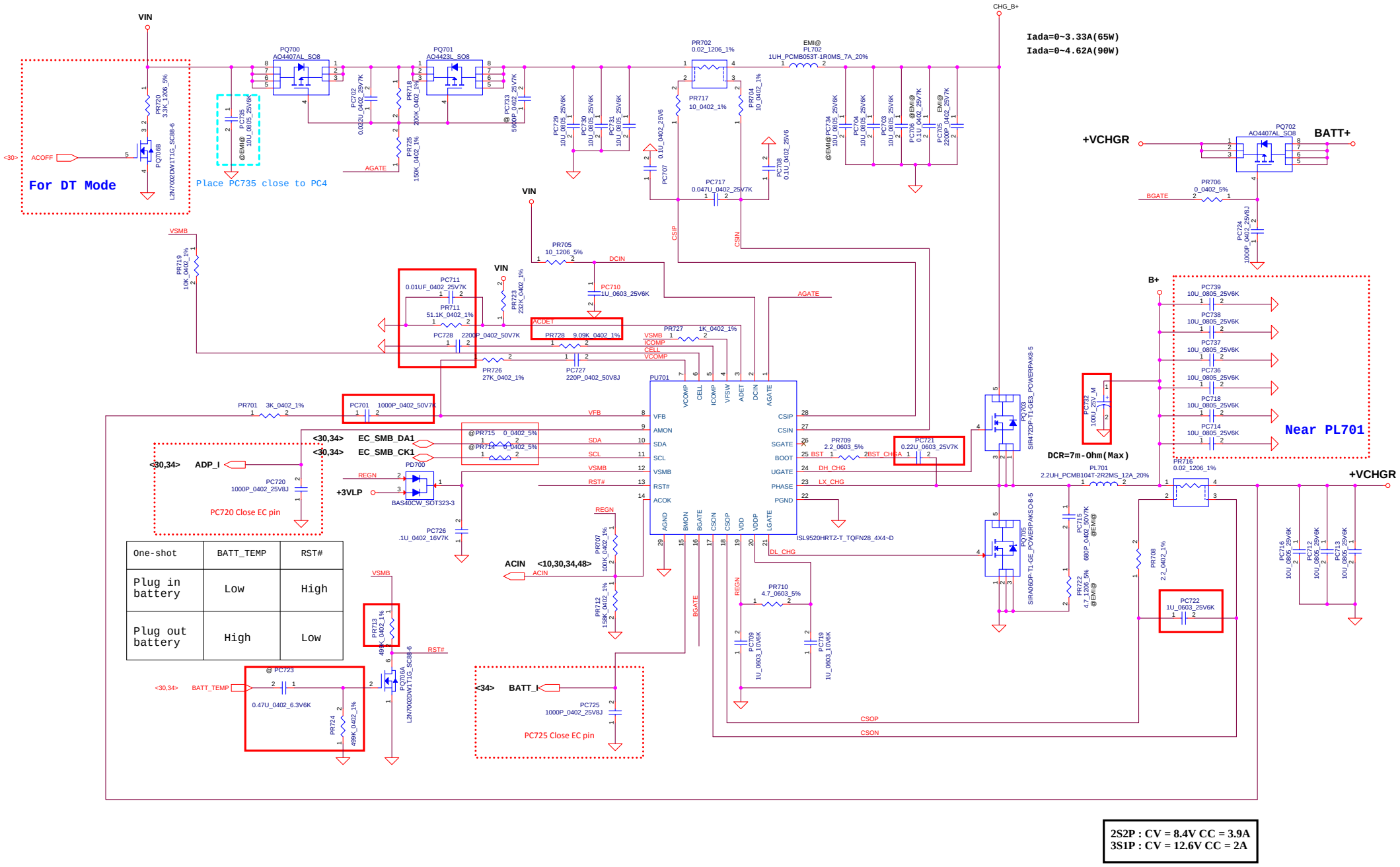
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: PWR_DCIN/BATT CONN/OTP

Size: Document Number: LA-B012P Rev: 1.0

Date: Wednesday, September 10, 2014 Sheet 34 of 56



One-shot	BATT_TEMP	RST#
Plug in battery	Low	High
Plug out battery	High	Low

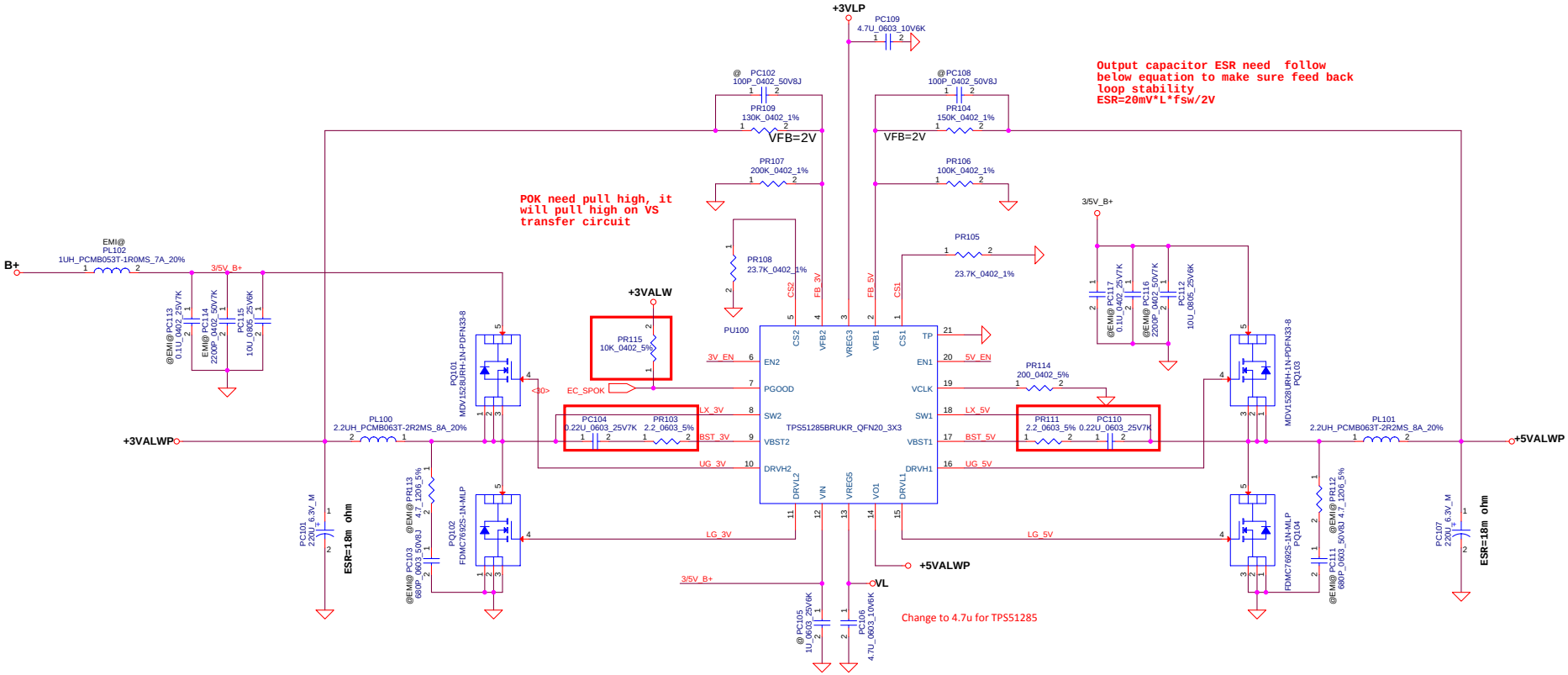
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: PWR_CHARGER

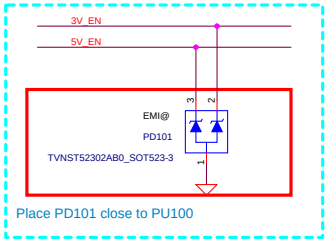
Size: A3 | Document Number: LA-B012P | Rev: 1.0

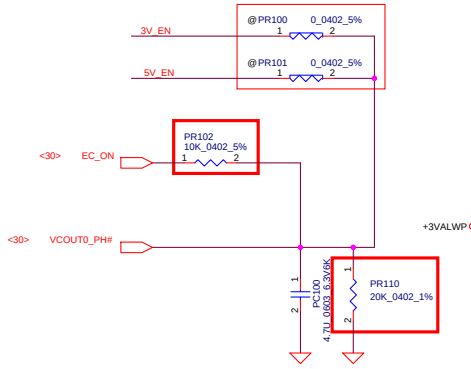
Date: Wednesday, September 10, 2014 | Sheet 35 of 56



3VALWP
TDC 5.95A
Peak Current 8.5A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm





5VALWP
TDC 5.96A
Peak Current 8.51A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm

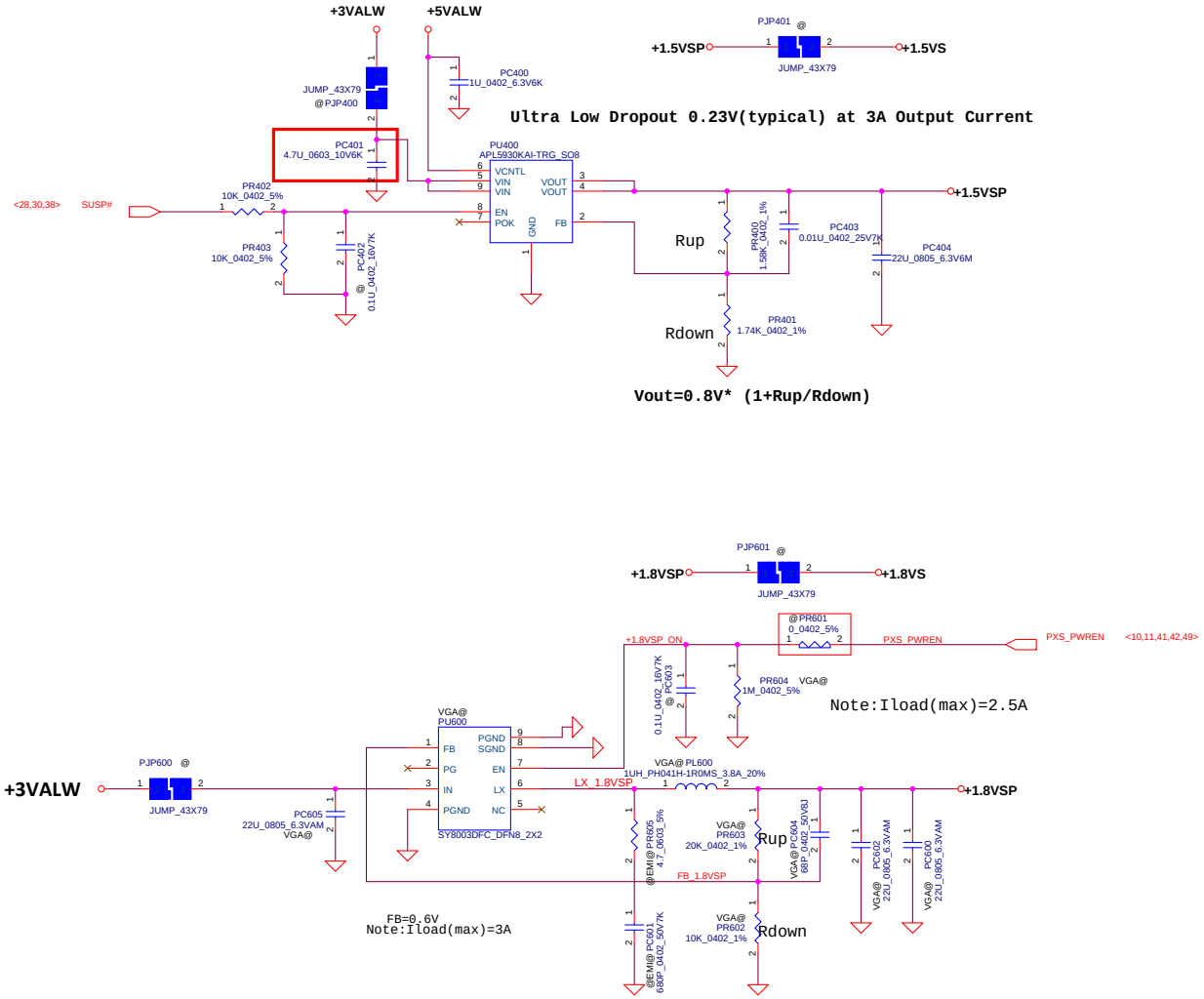
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: **PWR_3.3VALWP/5VALWP**

Size: C | Document Number: **LA-B012P** | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 36 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

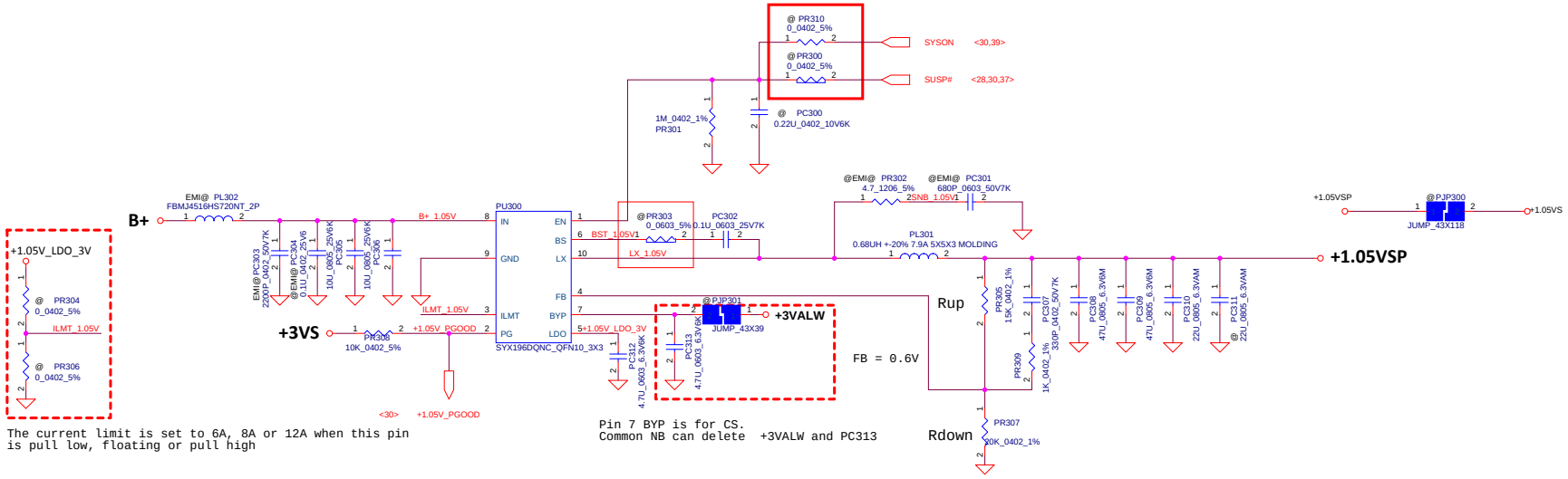
Compal Electronics, Inc.

Title: PWR_1.5VSP / 1.8VSP

Size: C | Document Number: LA-B012P | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 37 of 56

EN pin don't floating
If have pull down resistor at HW side, pls delete PR301



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC313

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=1.05V

+1.05VSP
TDC 5A
Peak Current 6.6A
OCP current 8A

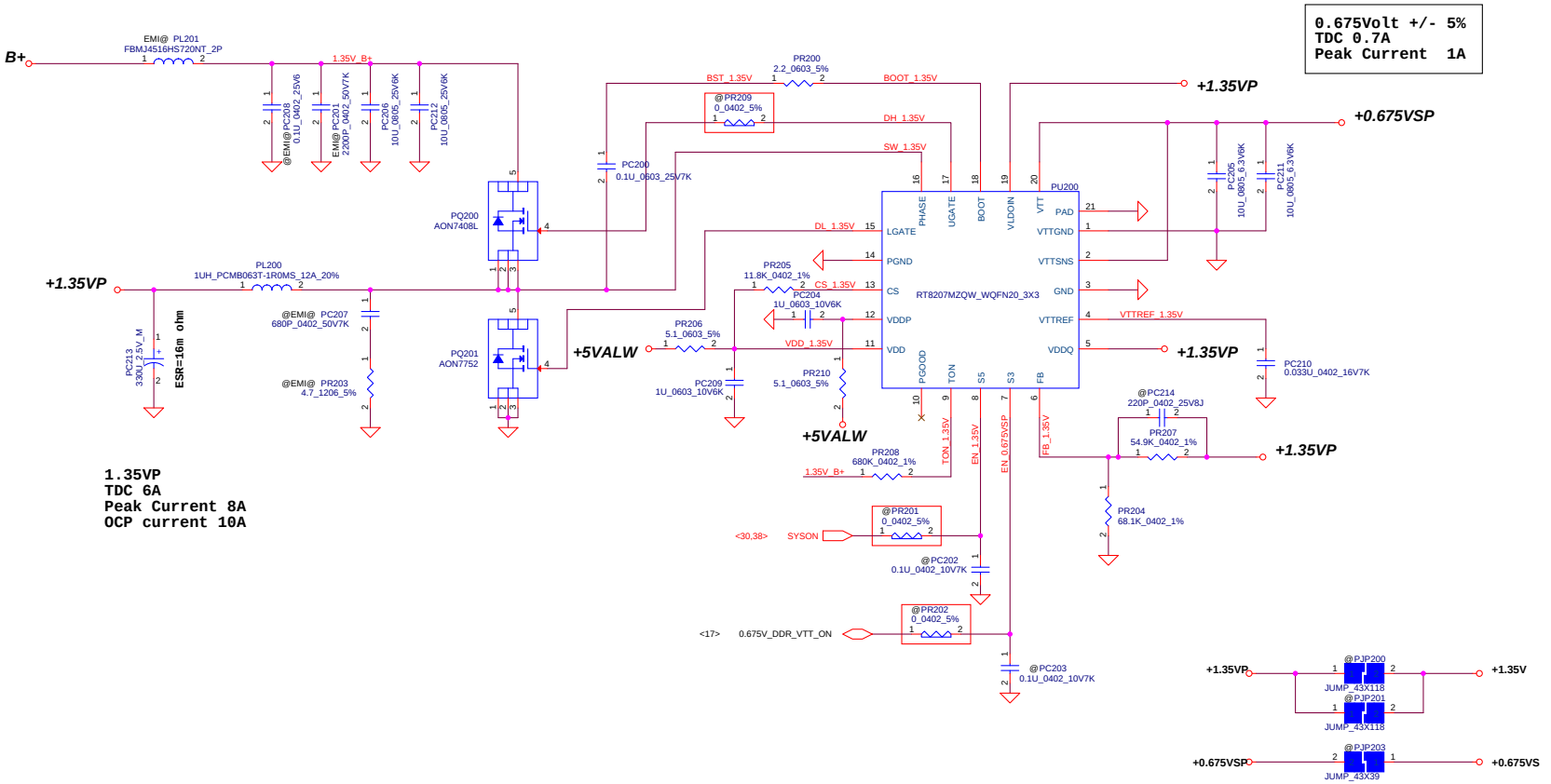
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: PWR_+VCCIO

Size: C | Document Number: LA-B012P | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 38 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: PWR_+1.35VP/0.675VSP

Size: A3 | Document Number: LA-B012P | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 39 of 56

EMI Part (47.1)

B+

CPU_CORE
TDC 10A/14A(PL2)@15W CPU
Peak Current 32A@15W CPU
OCP current 40A@15w
Choke DCR 1.1m-Ohm(Max)
Load line -2mV/A

DCR=0.66m-Ohm +/-7%

Check are there a pair 100Ω
at HW side and close to CPU.

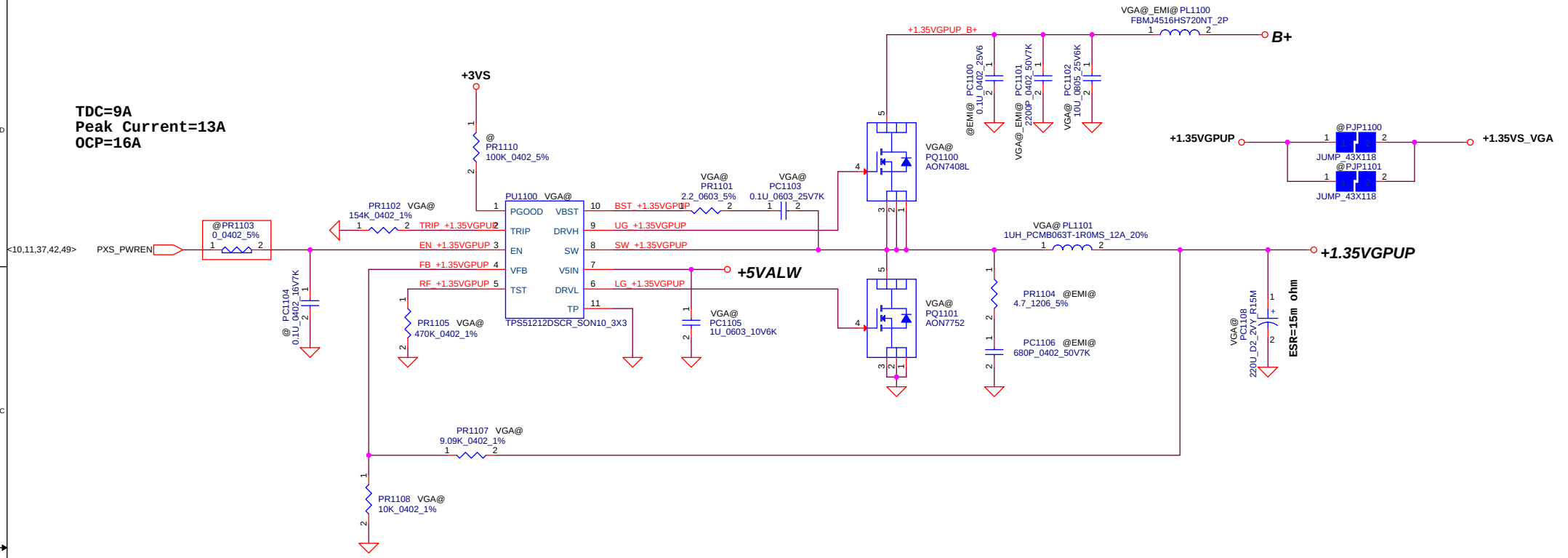
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: PWR_VCORE

Size: B | Document Number: LA-B012P | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 40 of 56



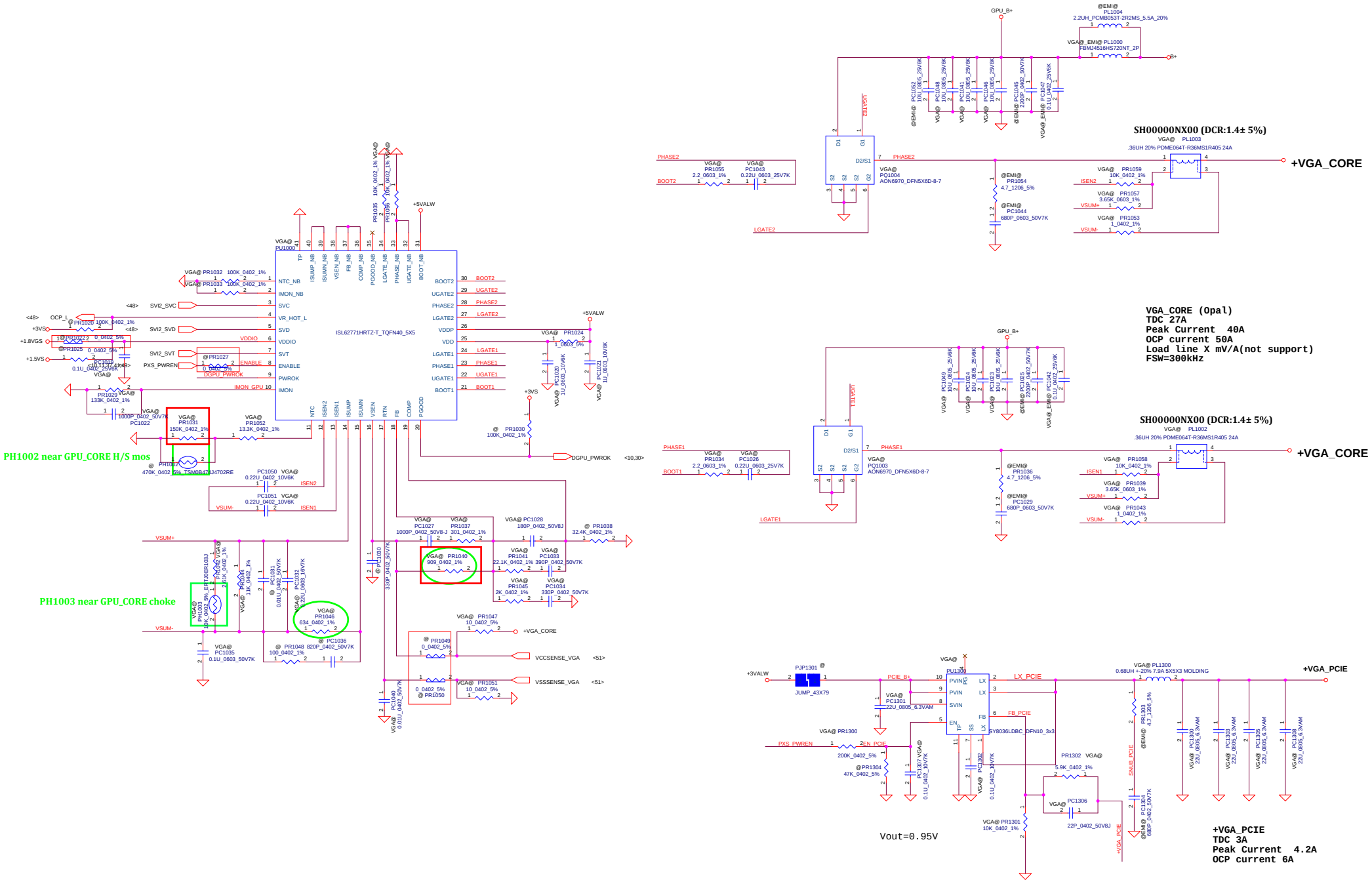
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: **PWR_+1.35VGPU**

Size: | Document Number: **LA-B012P** | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 41 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

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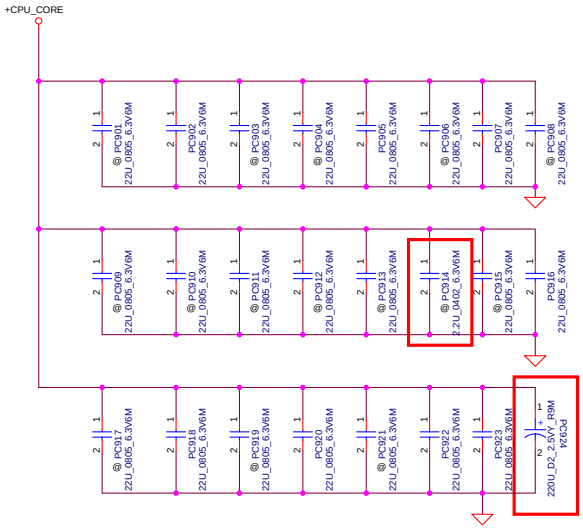
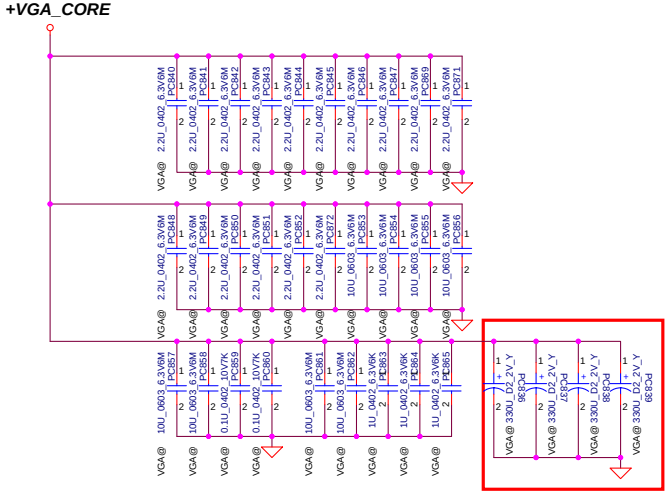
Compal Electronics, Inc.			
Title	PWR_VGA_CORE/PCIE		
Size: Custom	Document Number: LA-B012P		Rev: 1.0
Date: Wednesday, September 10, 2014	Sheet 42 of 56		





Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

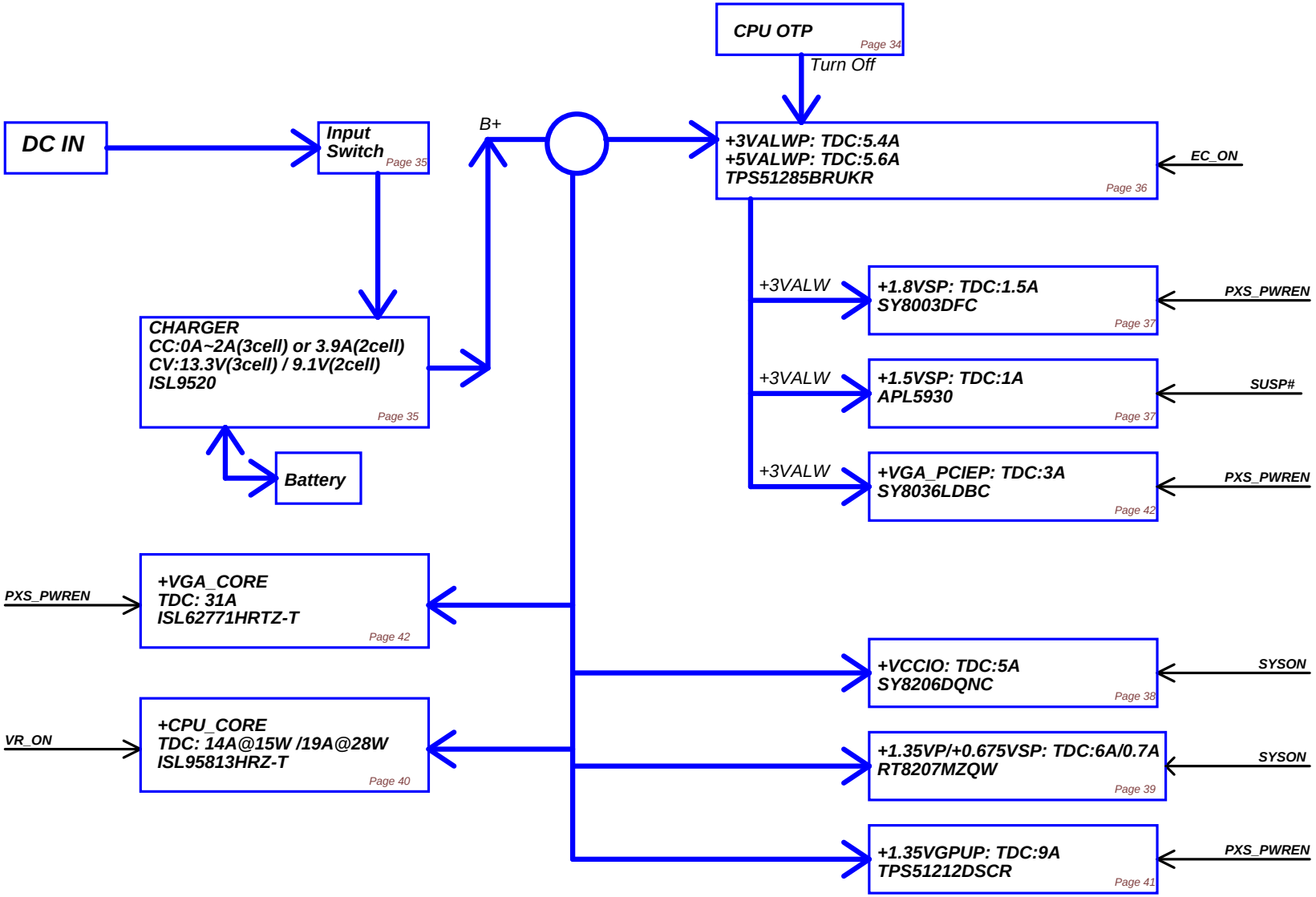
Compal Electronics, Inc.

Title: **PWR_PROCESSOR DECOUPLING**

Size: C | Document Number: **LA-B012P** | Rev: 1.0

Date: Wednesday, September 10, 2014 | Sheet 43 of 56

Power block



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.			
Title: PWR_POWER BLOCK DIAGRAM			
Size:	Document Number: LA-B012P		Rev: 1.0
Date: Wednesday, September 10, 2014	Sheet 44 of 56		

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	DCIN/BATT CONN/OTP	13/10/24	Morris	design change	change PR16 from 100K to 10K add PR37 10K	0.2
2	45	CHARGER	13/10/24	Morris	design change	change PC711 from 1000pF to 0.01uF change PR711 from 49.9K to 51.1K change PR713 from 10K to 499K change PR724 from 100K to 499K change PC721 from 0.047u to 0.22u change PC722 from 0.1u to 1u add PC732 100u	0.2
3	46	3.3VALWP/5VALWP	13/10/24	Morris	design change for solve can't root issue	change PC104 from 0.1u to 0.22u change PC110 from 0.1u to 0.22u change PR102 from 2.2K to 10K add PR110 20K	0.2
4	50	VCORE	13/10/24	Morris	adjust CPU parameter	change PR507(15W@) from 90.9K to 169K change PR519 from 1.91K to 10K change PR521 from 95.3K to 97.6K change PR539 from 8.06K to 909 change PC515,PC516 from SF000005100 to SF000004M00 change PL502 from SH00000NM00 to SH00000PQ00 change PR535(15W@) from 340 to 210 change PR537 from 1.27K to 1.37K change PR535(28W@) from 432 to 261 change PR507(28W@) from 113K to 205K change PR551 from 2.61K to 5.23K add PC522 82pF add PR533 0-ohm	0.2
6	52	VGA_CORE/PCIE	13/10/24	Morris	design change from vendor change LL	change PR1040 from 1.24K to 825	0.2
7	53	PROCESSOR DECOUPLING	13/10/24	Morris	adjust CPU parameter	change PC924 from SGA20331E10 to SGA00009800 remove PC901,PC903,PC904,PC906,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC917,PC919,PC921	0.2
8	45	CHARGER	13/10/28	Morris	design change for plug out battery shut down issue	change PC723 from 0.01uF to 0.47uF change PR728 from 0 to 9.09K change PC728 from 4700pF to 2200pF change PC701 from 220pF to 1000pF	0.2
9	46	3.3VALWP/5VALWP	13/12/12	Morris	design change from EE request	add PR115 10K-ohm	0.3
10	50	VCORE	13/12/12	Morris	design change from Intel recommend	change PR519 from 10K to 1.5K	0.3
11	48	+VCCIO	13/12/13	Morris	design change from EE request	delete PR310 and add PR300 0-ohm	0.3
12	50	VCORE	14/01/20	Morris	adjust CPU parameter	change PR507(15W@) from 169K to 90.9K change PR507(28W@) from 205K to 113K	1.0
13	53	PROCESSOR DECOUPLING	14/02/13	Morris	design change from thermal request	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0
14	50	VCORE	14/03/03	Morris	design change for VGA thermal issue	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0

Vendor	PS8713B	TI	Spec				schematic netname	3Vs		GND	
1	VDD	VCC	Same								
2	B_EQ0	EQ1	**LL:** 9.5dB (default)	**LH:** 13dB	**HL:** 4.5dB	**HH:** 7.7 dB	USB3_EQ1_P0	RI23	@	RI32	@
3	DE0	DE1	LL: 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_DE1_P0	RI26	@	RI35	@
4	EQ1	OS1	**LL:** 9.5dB	**LH:** 13dB	**HL:** 4.5dB	**HH:** 7.7 dB	USB3_OS1_P0	RI22	@	RI40	@
5	PD#	EN_RXD	it can be left open				USB3_ERD_P0	RI44	@	RI48	@
6	B_DE1	GND	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_P0_PIN6	RI53	@	RI49	@
7	REXT	NC		4.99K						RI56	4.99K
8	B_Inn	RX1-	Same								
9	B_Inp	RX1+	Same								
10	GND	GND	Same								
11	A_OUTn	TX2-	Same								
12	A_OUTp	TX2+	Same								
13	VDD	VCC	Same								
14	TST/NC	CM	4.7K ohm resistor for perfomance adjustment				USB3_CM_P0	RI42	@	RI46	@
15	A_EQ1	OS2	LL: 9.5 dB (default)	**LH:** 13 dB			USB3_OS2_P0	RI19	@	RI87	@
16	A_DE0	DE2	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_DE2_P0	RI20	@	RI31	@
17	A_EQ0	EQ2	LL: 9.5 dB (default)	**LH:** 13 dB			USB3_EQ2_P0	RI21	@	RI36	@
18	A_DE1	GND	**LL:** 3.5dB (default)	**LH:** no DE	**HL:** 2.7dB	**HH:** 5 dB	USB3_P0_PIN18	RI52	@	RI50	@
19	A_Inp	RX2+	Same								
20	A_Inn	RX2-	Same								
21	GND	GND	Same								
22	B_OUTp	TX1+	Same								
23	B_OUTn	TX1-	Same								
24	I2C_EN	NC	this pin canbe NC or connected to GND				NC			RI57	@

<11,30>

+3VS

RI53 1 @ 2 3.3K_0402_5% USB3_P0_PIN6
RI52 1 @ 2 3.3K_0402_5% USB3_P0_PIN18
RI421 2 4.7K_0402_5%~D USB3_CM_P0
RI441 @ 2 4.7K_0402_5%~D USB3_ERD_P0
RI191 @ 2 4.7K_0402_5%~D USB3_OS2_P0
RI201 @ 2 4.7K_0402_5%~D USB3_DE2_P0
RI211 @ 2 4.7K_0402_5%~D USB3_EQ2_P0
RI221 @ 2 4.7K_0402_5%~D USB3_OS1_P0
RI261 @ 2 4.7K_0402_5%~D USB3_DE1_P0
RI231 @ 2 4.7K_0402_5%~D USB3_EQ1_P0

RI871 @ 2 4.7K_0402_5%~D USB3_OS2_P0
RI311 @ 2 4.7K_0402_5%~D USB3_DE2_P0
RI361 @ 2 4.7K_0402_5%~D USB3_EQ2_P0
RI401 @ 2 4.7K_0402_5%~D USB3_OS1_P0
RI351 @ 2 4.7K_0402_5%~D USB3_DE1_P0
RI321 @ 2 4.7K_0402_5%~D USB3_EQ1_P0
RI461 @ 2 4.7K_0402_5%~D USB3_CM_P0
RI481 @ 2 4.7K_0402_5%~D USB3_ERD_P0
RI49 1 @ 2 0_0402_5%~D USB3_P0_PIN6
RI50 1 @ 2 0_0402_5%~D USB3_P0_PIN18

+3VS
CI23 0.01U_0402_16V7K~D
CI20 .1U_0402_16V7K~D

UI8 PS8713BTQFN24GTR2-A0_TQFN24_4X4

1	VCC		7	RI56 1	2 3.3K_0402_1%		
13	VCC	NC	24	@RI57 1	2 0_0402_5%~D		
			20	USB3RN3_R_C			
11	TX2-	RX2-	19	USB3RP3_R_C			
12	TX2+	RX2+					
15	USB3_OS2_P0						
16	USB3_DE2_P0	OS2					
17	USB3_EQ2_P0	DE2 EN_RXD	5	USB3_ERD_P0			
		EQ2 CM	14	USB3_CM_P0			
8	RX1-	TX1-	23	USB3TN3_RC CI21 1	2 0.1U_0402_10V6K~D	USB3TN3_R_C	
9	RX1+	TX1+	22	USB3TP3_RC CI24 1	2 0.1U_0402_10V6K~D	USB3TP3_R_C	
4	USB3_OS1_P0						
3	USB3_DE1_P0	OS1					
2	USB3_EQ1_P0	DE1 GND	6	USB3_P0_PIN6			
		EQ1 GND	10				
		GND	18	USB3_P0_PIN18			
25	PGND	GND	21				

<12> USB3RN3_3D_CAM — USB3RN3 CI22 1 2 0.1U_0402_10V6K~D USB3RN3_L
<12> USB3RP3_3D_CAM — USB3RP3 CI19 1 2 0.1U_0402_10V6K~D USB3RP3_L
<12> USB3TN3_3D_CAM — USB3TN3 CI16 1 2 0.1U_0402_10V6K~D USB3TN3_L
<12> USB3TP3_3D_CAM — USB3TP3 CI5 1 2 0.1U_0402_10V6K~D USB3TP3_L

@RI3 1 2 0_0402_5%~D
USB3RN3_R_C 2 EMI@ LI10 1 USB3RN3_R
USB3RP3_R_C 3 4 USB3RP3_R
S COM FI_ CHILISIN CMMI21T-670Y-N
@RI4 1 2 0_0402_5%~D

@RI5 1 2 0_0402_5%~D
USB3TN3_R_C 2 EMI@ LI9 1 USB3TN3_R
USB3TP3_R_C 3 4 USB3TP3_R
S COM FI_ CHILISIN CMMI21T-670Y-N
@RI6 1 2 0_0402_5%~D

+5VALW
C94 1U_0402_6.3V6K
+5VALW
+5VALW
+5VALW

+3VALW TO +5V_3DCAM

J521 open

J521 @ JUMP_43X39

U2409 TPS22967DSGR_SON8_2X2

1	VIN	VOUT	7
2	VIN	VOUT	8
3	ON	CT	6
4	VBIAS	GND	5
		GND	9

+5V_CAM
C5220 2200P_0402_25V7K
C5221 0.1U_0402_10V6K

3D_CAM_EN
RI90 100K_0402_5%~D

For Test,
APE8937(SA000070L00)
AOZ1336(SA00006U600)
TPS22967(SA000070S00)

CT pin use 2200pf for soft start tuning

+3VALW_PCH +3VS
RI55 10K_0402_5% FW_UPDATE
RI89 @ 10K_0402_5%

+3VALW_PCH +3VS
RI54 10K_0402_5% 3D_CAM_EN
RI88 @ 10K_0402_5%

<11> CAM_DETECT
<9,30> FW_UPDATE

RI58 0_0402_5%~D CAM_DETECT FW_UPDATE DETECT
RI91 100K_0402_5%~D @ +5V_CAM

JCAM3D ACES_50463-0104A-001

1			1
2	USB3RN3_R		2
3	USB3RP3_R		3
4			4
5	USB3TN3_R		5
6	USB3TP3_R		6
7	DETECT		7
8			8
9			9
10			10
11	GND		11
12	GND		12

DI3 @ESD@ S DIO(BR) TVWDF1004AD0 DFN ESD

USB3TN3_R	1	10	USB3TN3_R
USB3TP3_R	2	9	USB3TP3_R
USB3RN3_R	4	7	USB3RN3_R
USB3RP3_R	5	6	USB3RP3_R
	3		
	8		

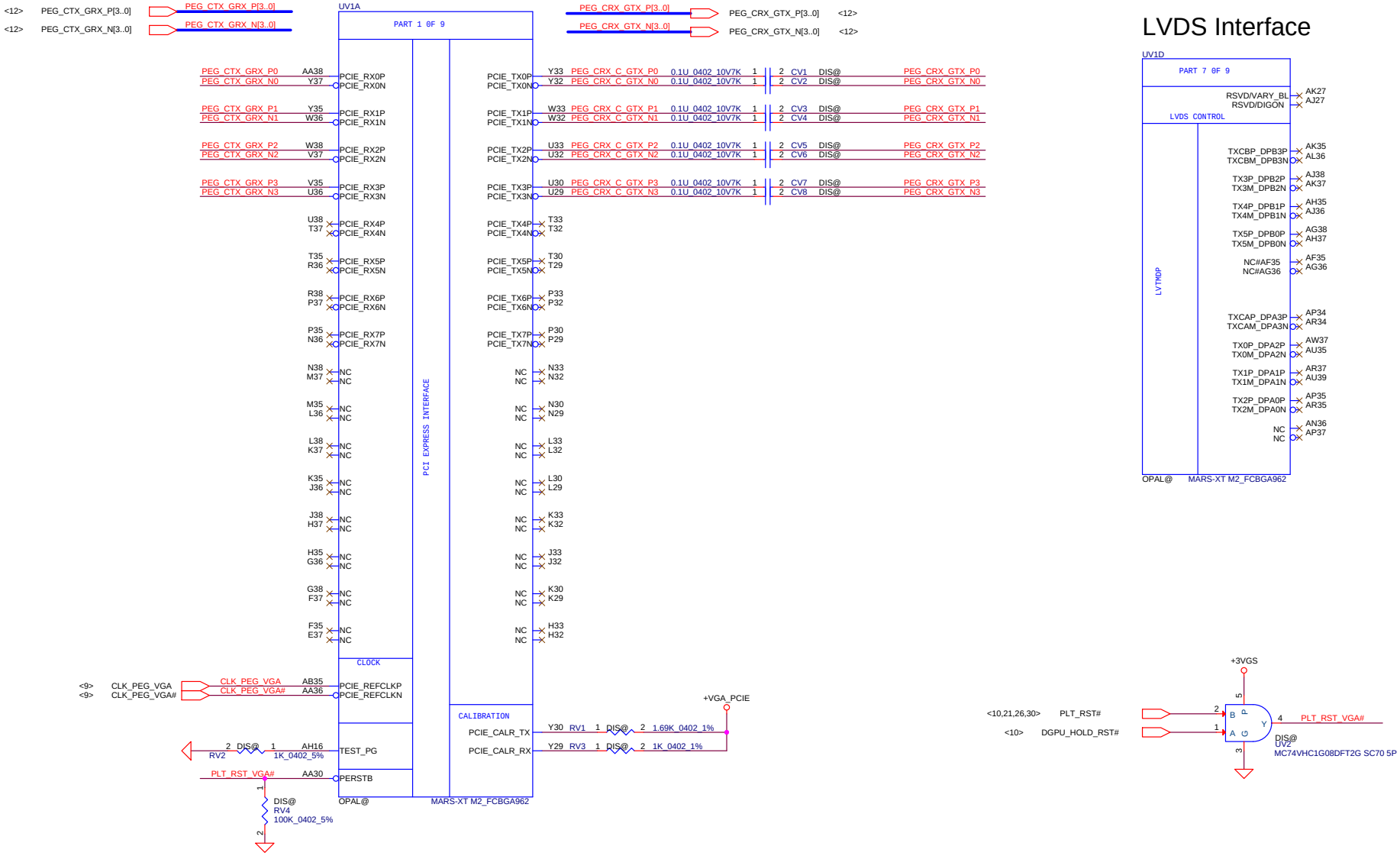
Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

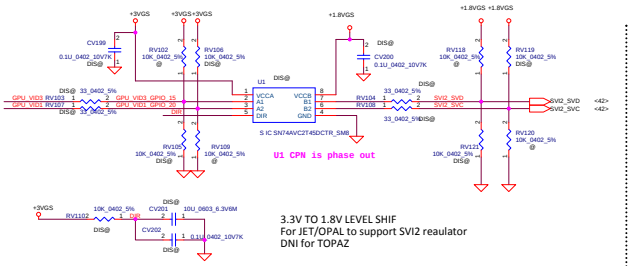
Title: **3D CAMERA**

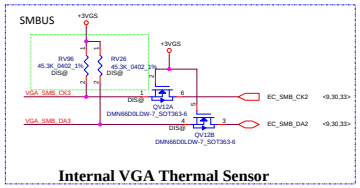
Size: Document Number: **LA-B015P** Rev: 0.1

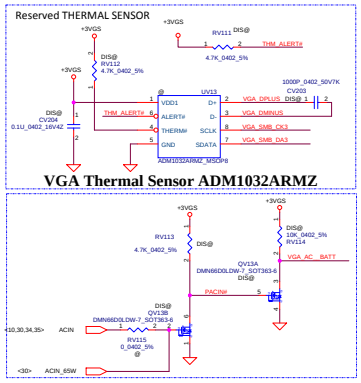
Date: Wednesday, October 22, 2014 Sheet 46 of 56

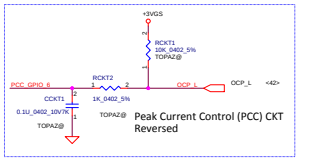


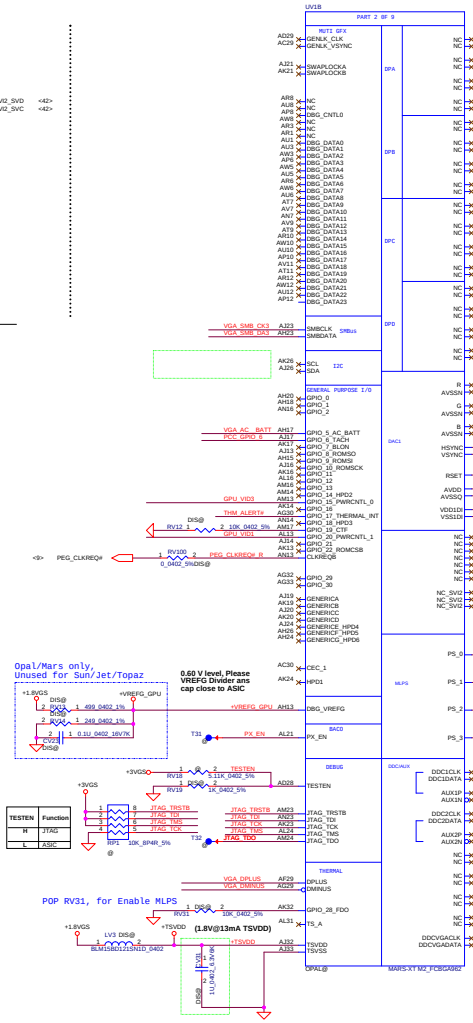
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/04/01	Deciphered Date 2015/04/30	Title: AMD_OPAL-XT_M2_PCIE/LVDS
			Size: Custom; Document Number: LA-B015P; Rev: 0.1
			Date: Wednesday, September 10, 2014; Sheet 47 of 56











TESTEN	Function
H	JTAG
L	ASIC

TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

(1.8V@70mA AVDD)

(1.8V@117mA VDD1DI)

VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

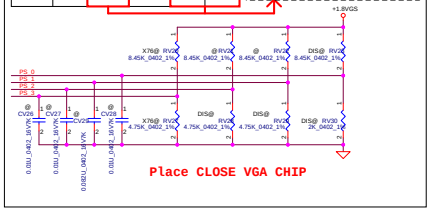
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	PCIE Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	0
BIF_GEN3_EN_A	PS_1[1]	PCIE Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select if PS_2[3]=0, defines memory aperture size if PS_2[3]=1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV010 (Chingis) 101 - 1Mbit Pm25LV020 (Chingis)	000
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	0
AUD[1] AUD[0]	NA NA	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It isthe responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	Reserved for future ASIC	1
		NOTE:ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[3:1]	1 1	001	NC	8.45K	2K
PS_1[5:1]	11	0 0 0	NC	NC	4.75K
PS_2[5:1]	11	0 0 0	NC	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to memory table



Bits [3:1] Memory ID	P/N	Vendor	vendor part number	Size	RV20	RV27
111	SA000076P0L	SAMSUNG	K4W4G1646D-BC1A	4GB	**4.75K**	**NC**
(default) 000	SA00006E80L	HYNIX	H5TC4G63AFR-11C	4GB	**NC**	**4.75K**
001	SA000077K0L	Micron	MT41J256M16HA-093G:E	4GB	**8.45K**	**2K**

MLPS implementation:

- ★Place MLPS circuit components as close to ASIC as possible
- ★Total DC resistance of trace between PS pin and C should be less than 2 ohm
- ★Total DC resistance of trace between C and ground should be less than 2 ohm
- ★Trace capacitance should be less than 100pf.
- ★Resistors should be of +-1% tolerance

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Issued Date	2014/04/01	Deciphered Date	2015/04/30

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Title	AMD_OPAL-XT_M2_Main_MSIC		
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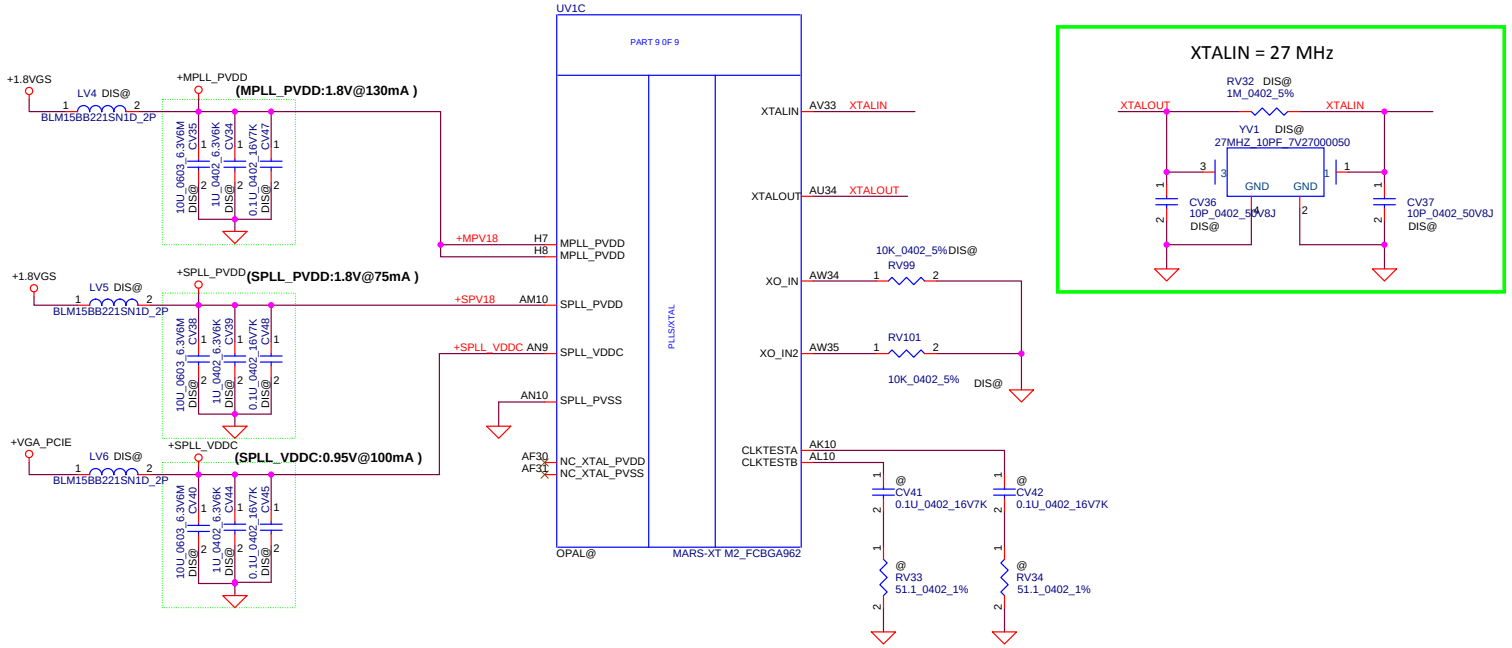
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

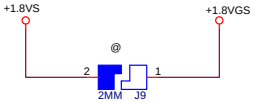
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



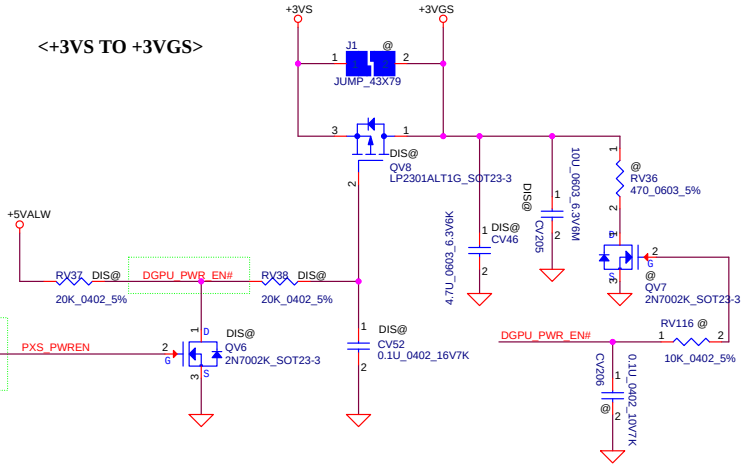
+1.35VS_VGA TO +1.35V_MEM_GFX

SHORT DEFAULT

+1.8VS TO +1.8VGS



SHORT DEFAULT



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Title: AMD_OPAL-XT_M2_BACO POWER

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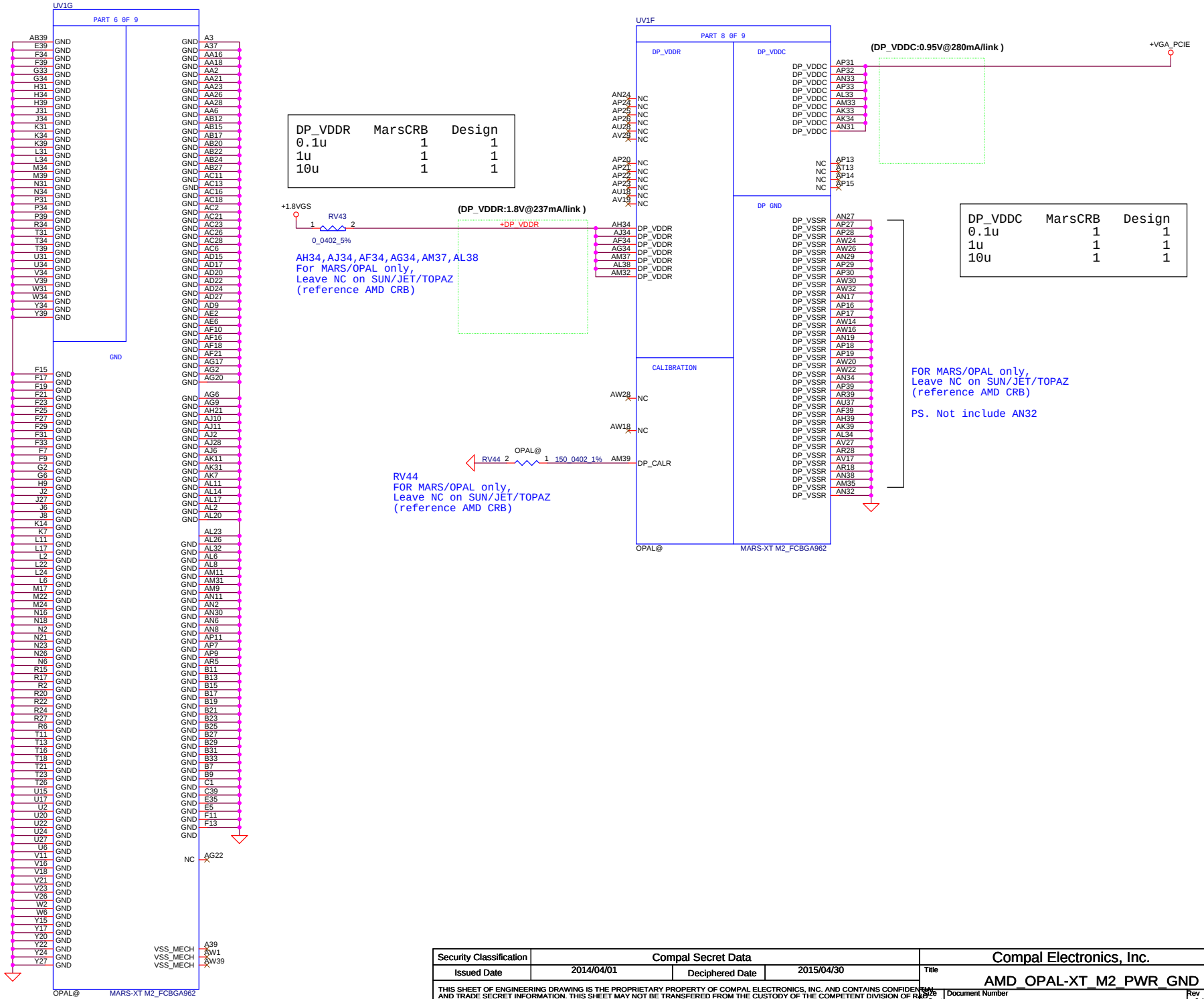

DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

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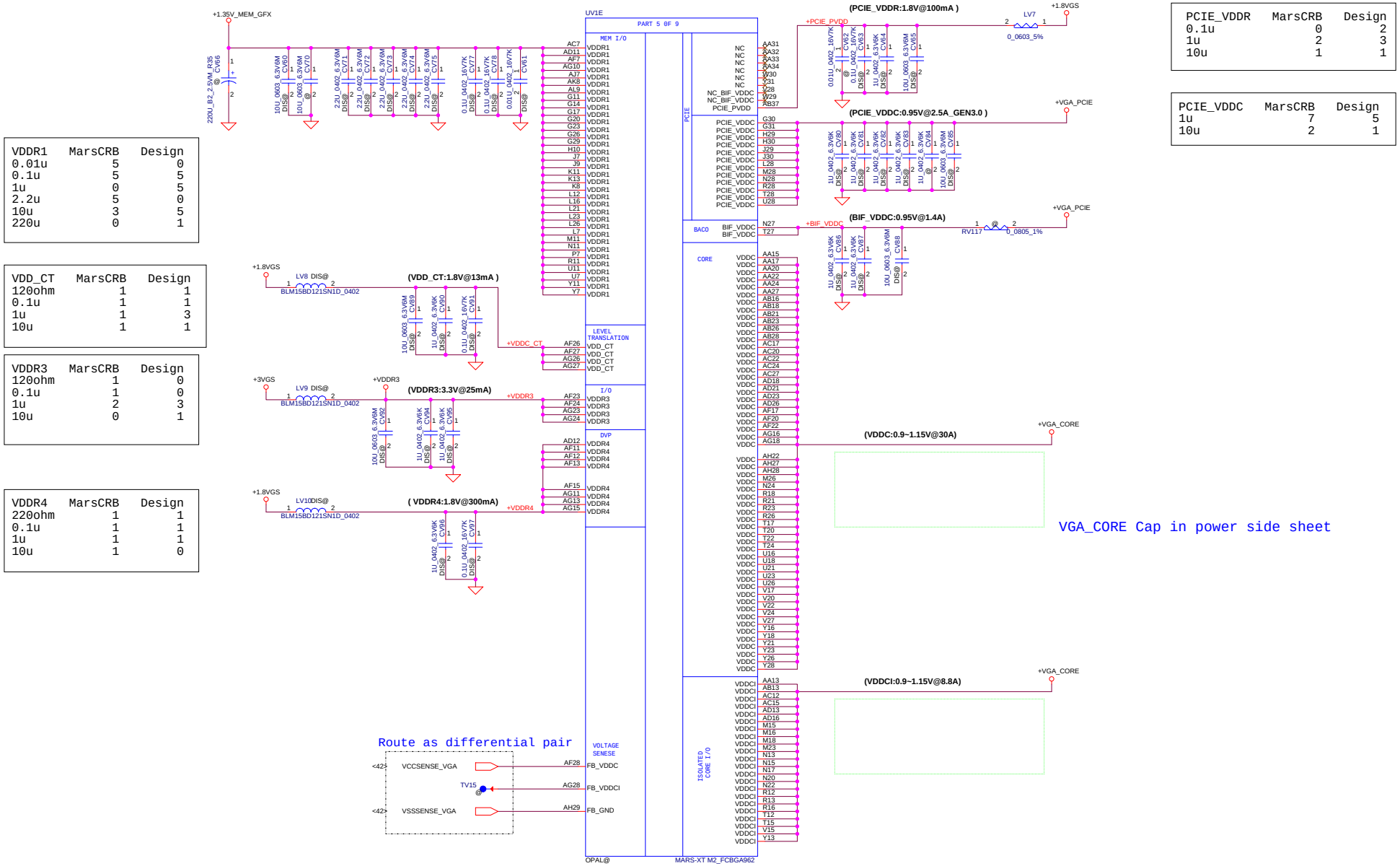
Title: AMD_OPAL-XT_M2_PWR_GND

Size: Custom | Document Number: LA-B015P | Rev: 0.1

Date: Wednesday, September 10, 2014 | Sheet 50 of 56



VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

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Title: AMD_OPAL-XT_M2_Power

Size	Document Number	Rev
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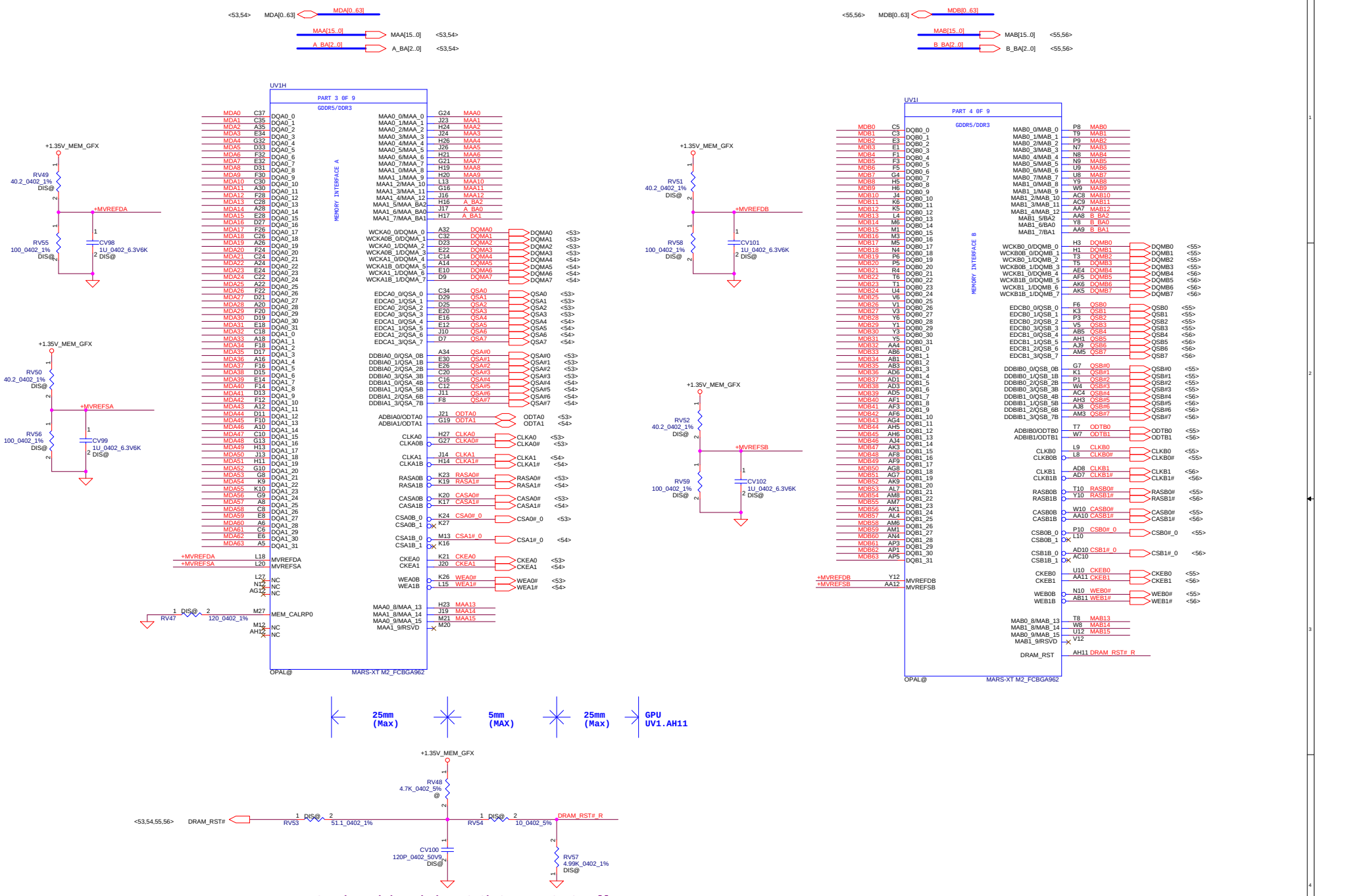
Date: Wednesday, September 10, 2014 Sheet 51 of 56



DRAM_RST# is a daisy-chain net that connects to all VRAM

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

Ball to RV57 < 1"
CV100 to RV57 < 200 mil
CV100 to RV53 < 1"

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Title: AMD_OPAL-XT_M2_MEM IF

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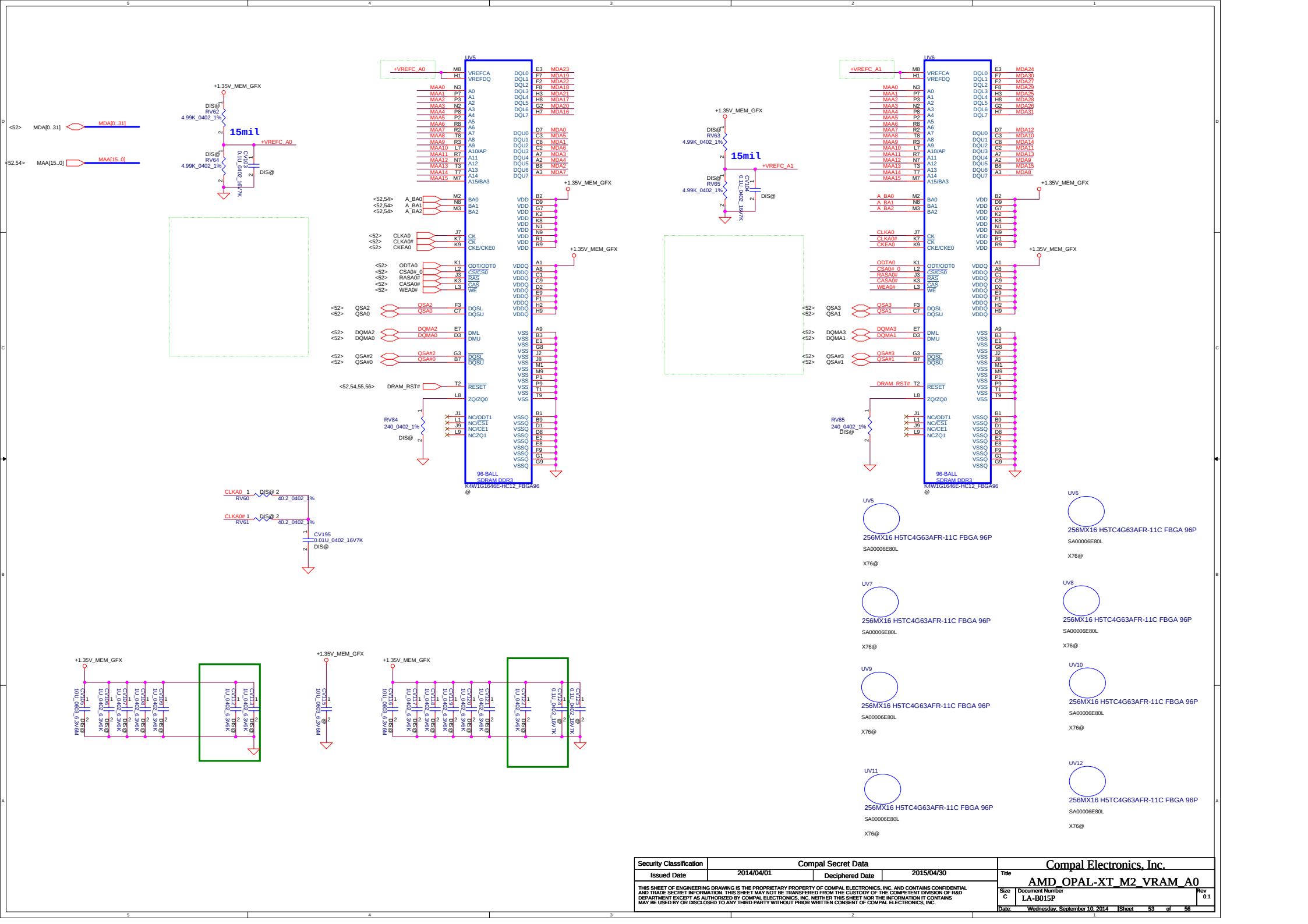
UV5
UV6
+1.35V_MEM_GFX
+VREFC_A0
+VREFC_A1
15mil
96-BALL SDRAM DDR3
K4W1G1646E-HC12_FBGA96
256MX16 H5TC4G63AFR-11C FBGA 96P
SA00006E80L
X76@
UV7
UV8
UV9
UV10
UV11
UV12
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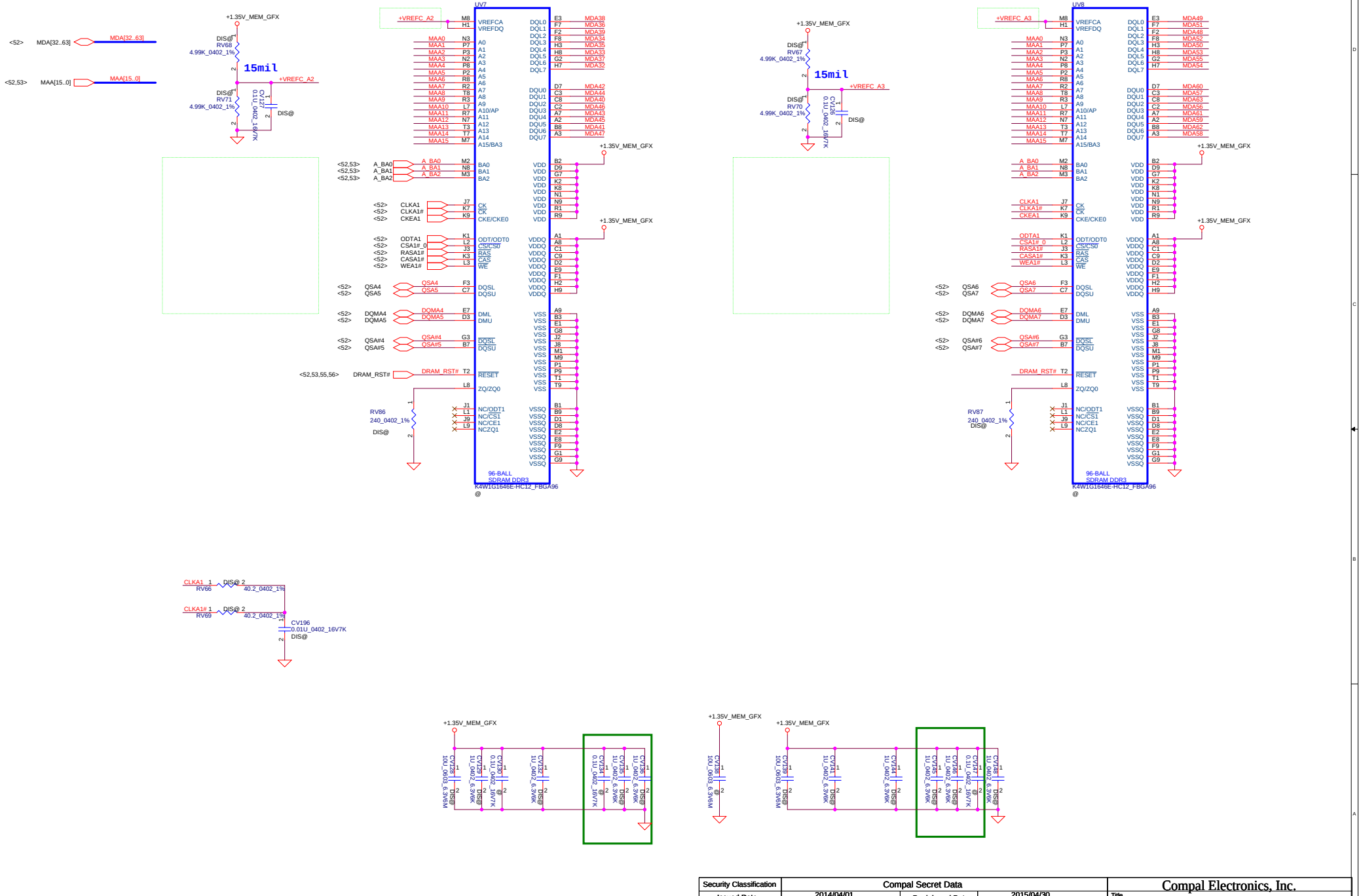
Document Number LA-B015P
Rev 0.1
Date: Wednesday, September 10, 2014
Sheet 53 of 56



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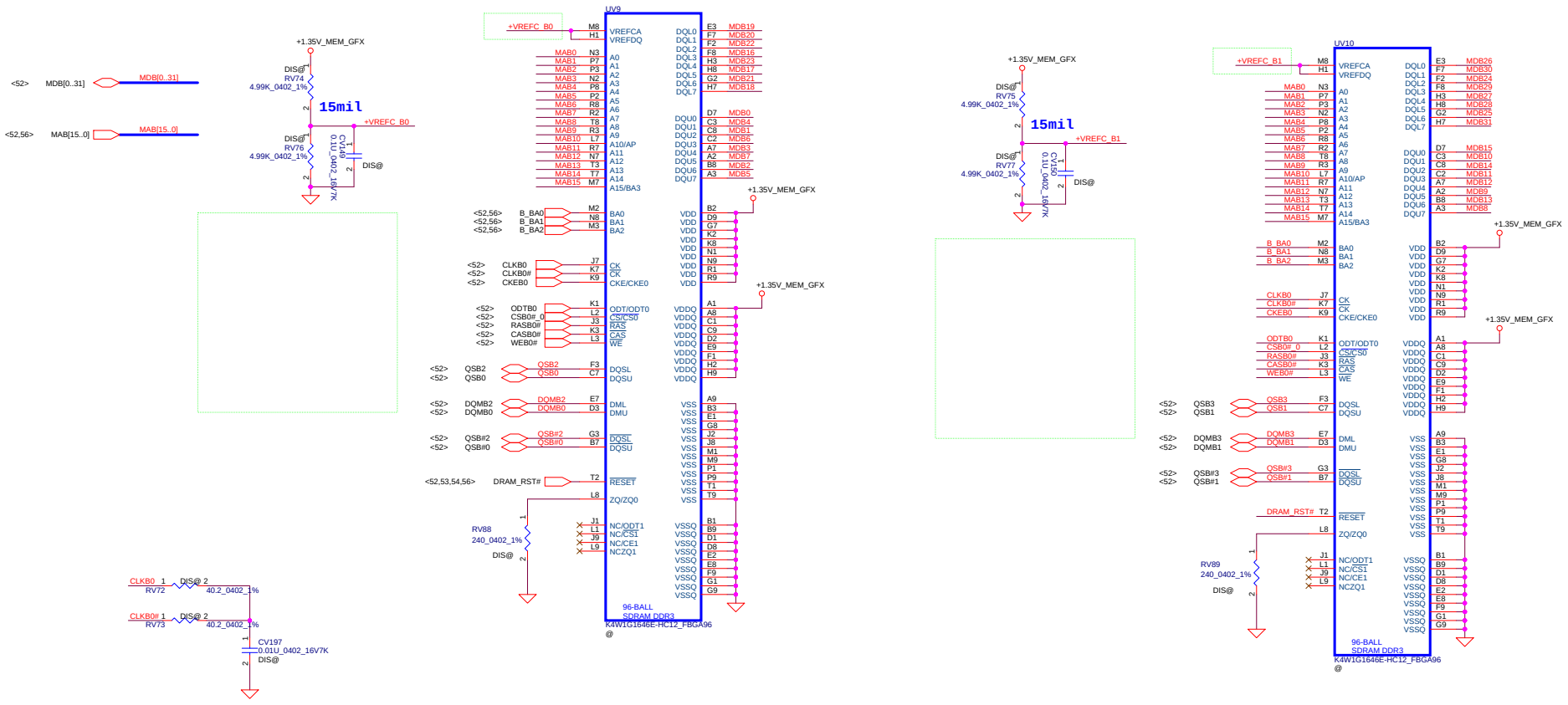

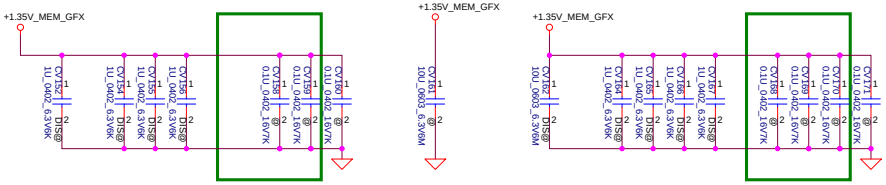

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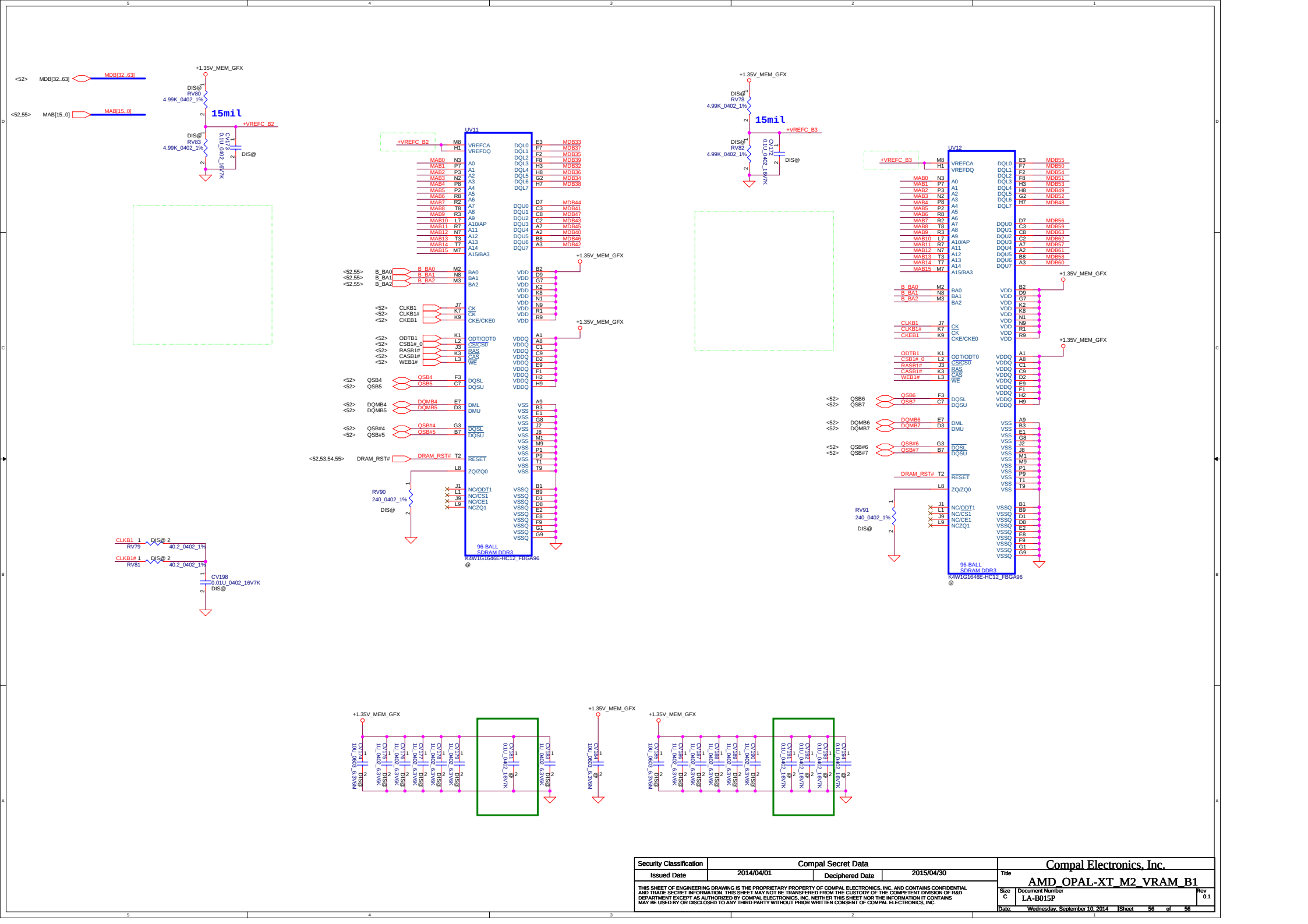

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