

Hades_HBS 860M SV

Schematics Document

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緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Cover Page

Hades_HBS 860M

SE

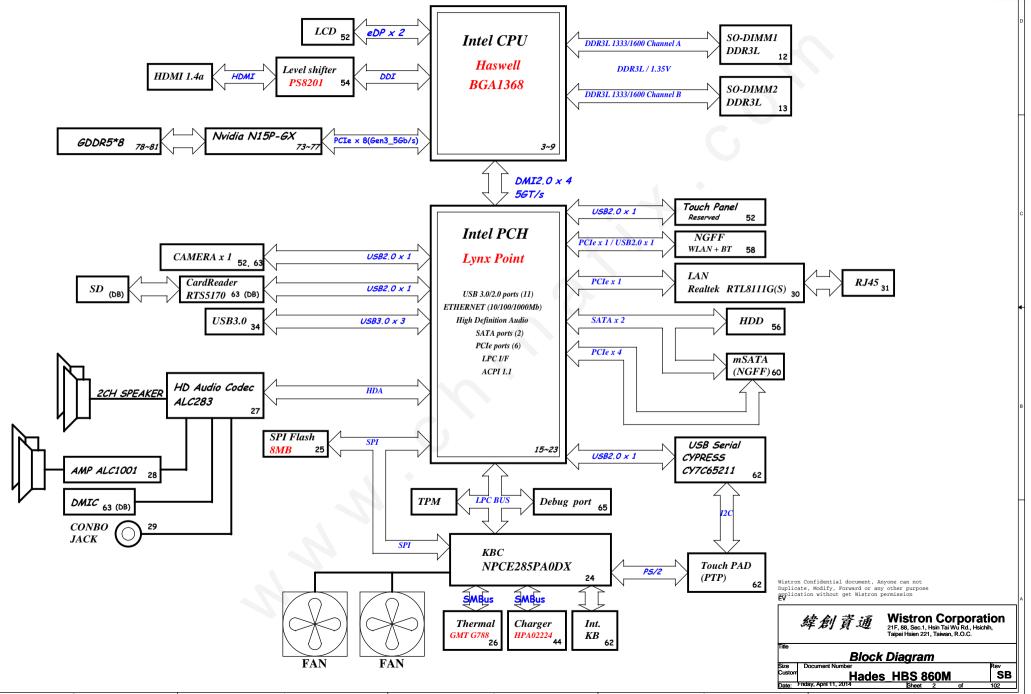
Hades_HBS Board Block Diagram

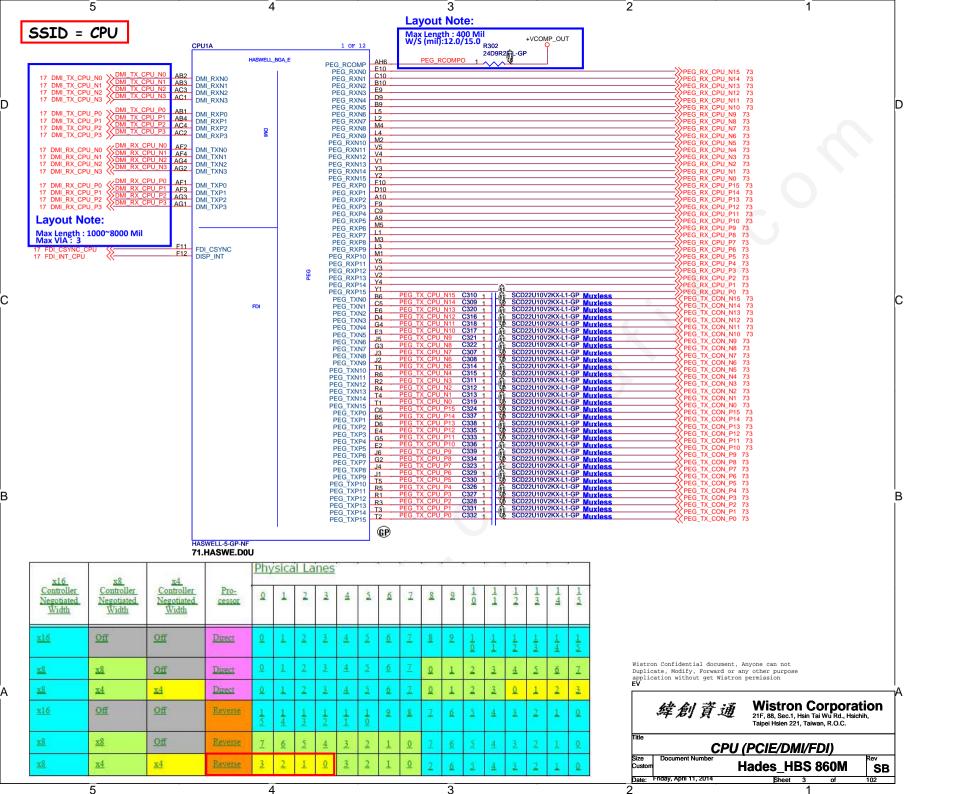
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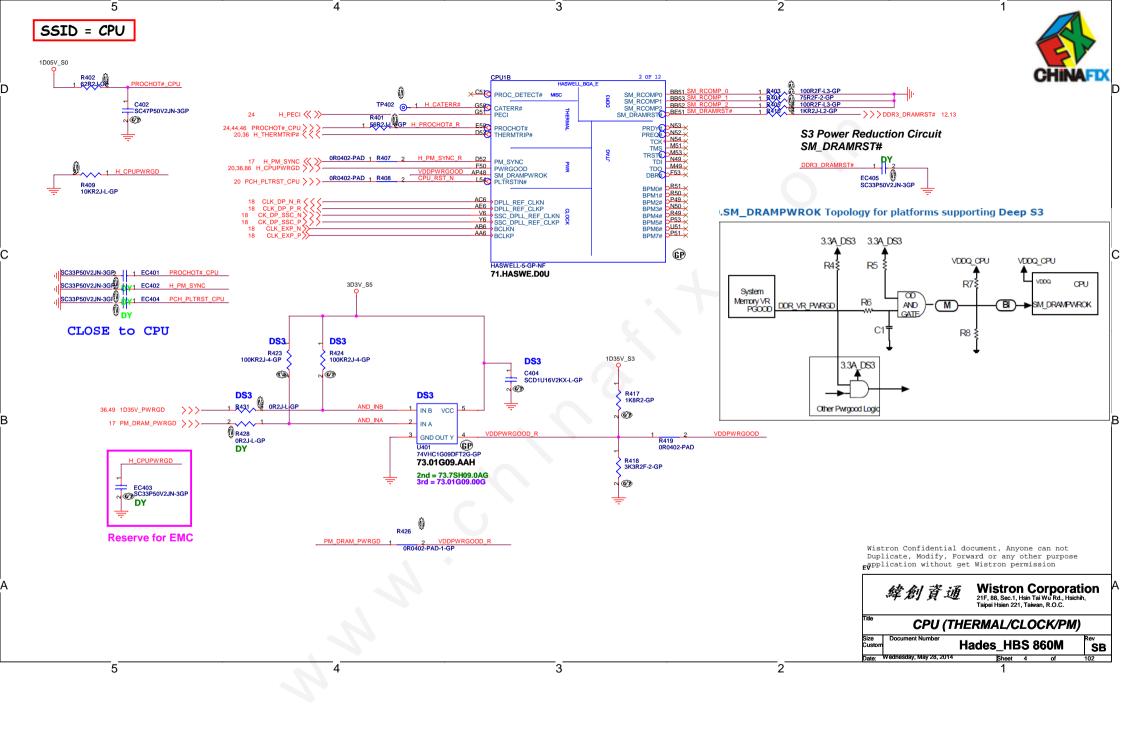
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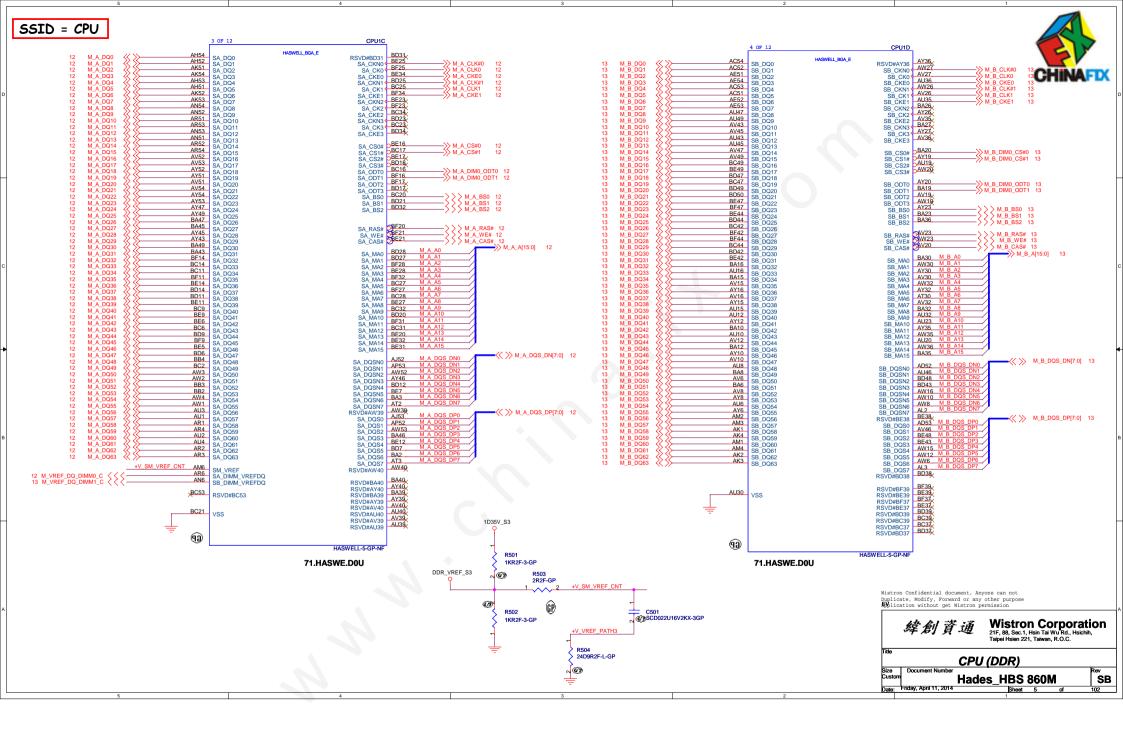
 Revision
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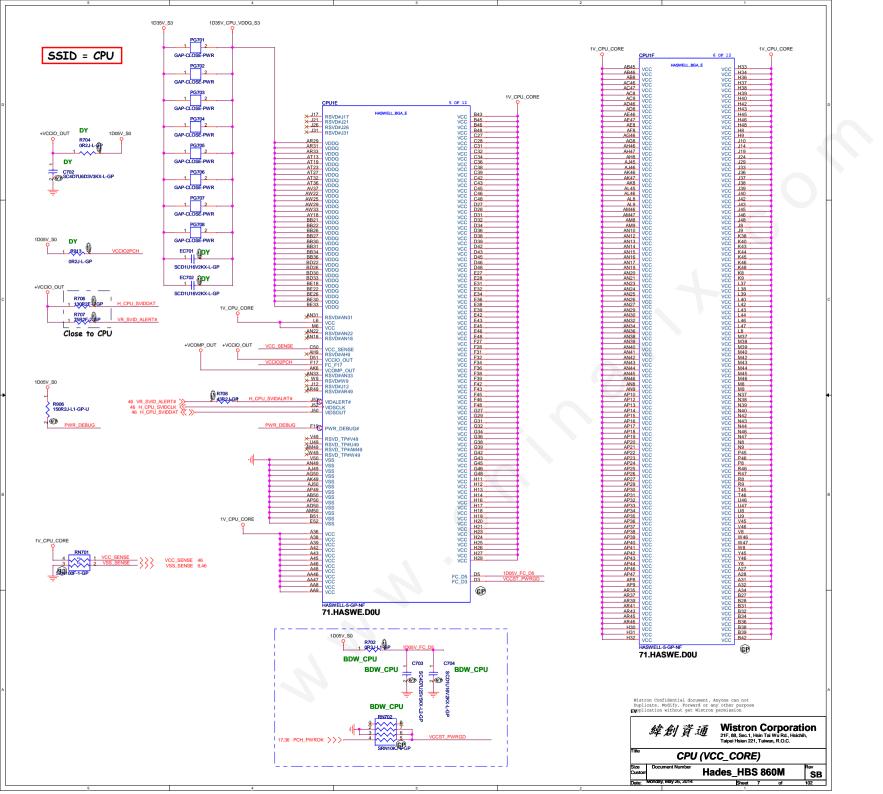






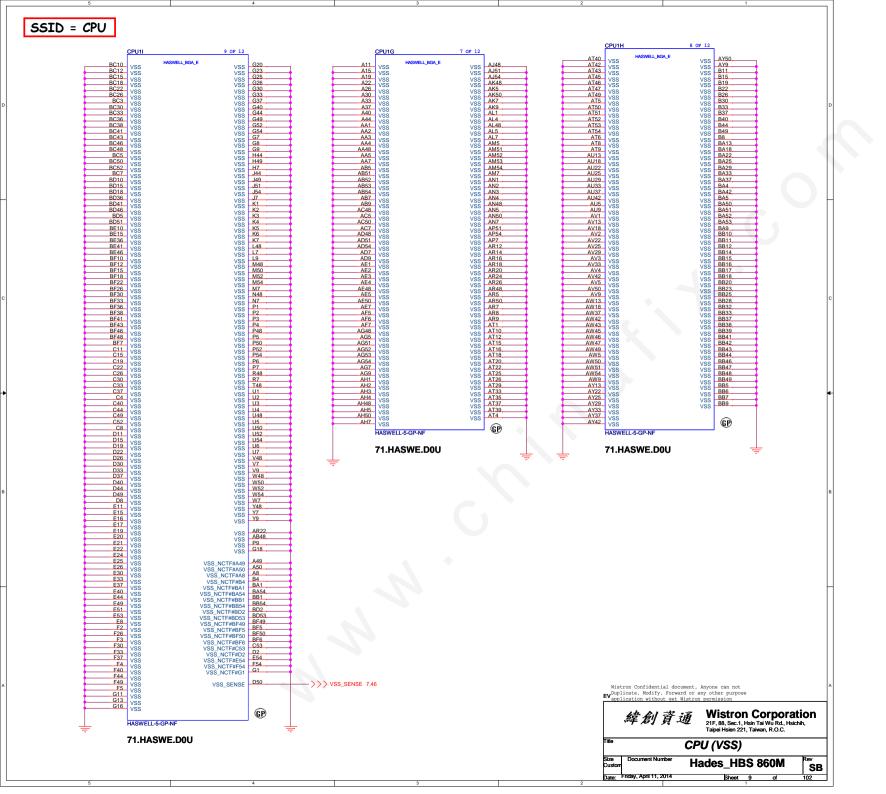
SSID = CPU 1V CPU CORE CPU1K 11 OF 12 12 OF 12 HASWELL_BGA_E RSVD_TP#F1 NCTF TEST PIN: A3,A53,B2,B54,,C1,BE1, RSVD_TP#BE4 RSVD_TP#BD3 BD3 BE54.BF2.BF53 DAISY CHAIN NCTF A × F6 RSVD_TP#F6 RSVD_TP#G6 TP606 1.0 DAISY CHAIN NCTF BF51 BF52 ×G21 ×G24 F21 DAISY_CHAIN_NCTF_BF52 TP602 Y51 V RSVD_TP#G21 DAISY_CHAIN_NCTF_A51 R601 49D9R2FiL1-GP H_CPU_TESTLO_F2 A52 DAISY_CHAIN_NCTF_A52 RSVD_TP#G24 TESTLO_F21 CFG19 V52 × G19 F51 VSS VSS DAISY_CHAIN_NCTF_C2 DAISY_CHAIN_NCTF_C3 F52 RSVD#B50 RSVD#AH49 RSVD#AU27 RSVD#AU27 RSVD#AU27 RSVD#B04 RSVD#B04 RSVD#B64 RSVD#B64 RSVD#F8 C54 NCTF_B54_C54 NCTF_B3_A3 B3 DAISY CHAIN NCTF B3 DAISY CHAIN NCTF C54 TP607 × L52 × L53 RSVD_TP#L52 RSVD_TP#L53 DAISY_CHAIN_NCTF_D1 NCTF A52 B5 DAISY CHAIN NCTF B52 TP608 DAISY_CHAIN_NCTF_B53 DAISY_CHAIN_NCTF_D54 × L51 RSVD_TP#L51 DAISY CHAIN NCTF#A3 ↑ R605 2 49D9R2FtL1-GP H_CPU_TESTLO_F20 × F20 DAISY_CHAIN_NCTF#A3 A53 DAISY_CHAIN_NCTF#A53 B2 DAISY_CHAIN_NCTF#B2 B2 RSVD_TP#F24 RSVD_TP#F25 TP603 TP604 BC1 DAISY CHAIN NOTE BC1 - DAISY_CHAIN_NCTF_BC1 DAISY_CHAIN_NCTF#B54
- DAISY_CHAIN_NCTF_BC54 DAISY_CHAIN_NCTF#B54
- DAISY_CHAIN_NCTF#B51 DAISY_CHAIN_NCTF#B61
- DAISY_CHAIN_NCTF#B61
- DAISY_CHAIN_NCTF#B654 TESTLO_F20 BD1 AG49 AD49 AC49 RSVD#F16 F16 × CEGO BE54 CFG1 NCTF_BE54_BD54 BD54 BF2 DAISY_CHAIN_NCTF_BD54 DAISY_CHAIN_NCTF#BF2
DAISY_CHAIN_NCTF#BF53 AF49 BF53 CFG3 Y50 AB49 BE2 BE3 BE2
BE3
DAISY_CHAIN_NCTF_BE2
DAISY_CHAIN_NCTF_BE3
DAISY_CHAIN_NCTF_BE52
DAISY_CHAIN_NCTF_BE53 CFG5 RSVD#AN35 RSVD#AN37 RSVD#AF9 RSVD#AE9 V51 RSVD_TP#G12 G12 X RSVD_TP#G10 G10 X W51 × Y49 Y54 H54 VSS × Y53 × W53 × U53 × V54 × R53 × R52 CFG9 VSS H53 BF3 DAISY_CHAIN_NCTF_BF3 DAISY_CHAIN_NCTF_BF4 RSVD#AE9 RSVD#G14 RSVD#G17 RSVD#AD45 RSVD#AG45 CFG11 H52 CFG13 VSS RSVD#AG45 N51 × G53 × H50 × RSVD#N51 CFG15 (GP) RSVD#G53 × L50 × L49 RSVD#L50 RSVD#H50 RSVD#L49 RSVD#E5 HASWELL-5-GP-NF (GP) HASWELL-5-GP-NF 71.HASWE.D0U 71.HASWE.D0U PEG Static Lane Reversal eDP Enable 1: Normal Operation; Lane # 1:Disable CFG2 CFG4 0:Lane Reversed CFG2 CFG4 R602 1KR2J-L2-GP R604 1KR2J-L2-GP PCIE Port Bifurcation Straps CFG[6:5] 11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission $\mathbf{E}^{\mathbf{V}}$ CFG9 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. Rens R609 DY 1KR2J-L2-GP DY 1KR2J-L2-GP KR2J-L2-GP 1KR2J-L2-GP DY DY (E) **(** (**@** (C) CPU (CFG) Hades HBS 860M SB



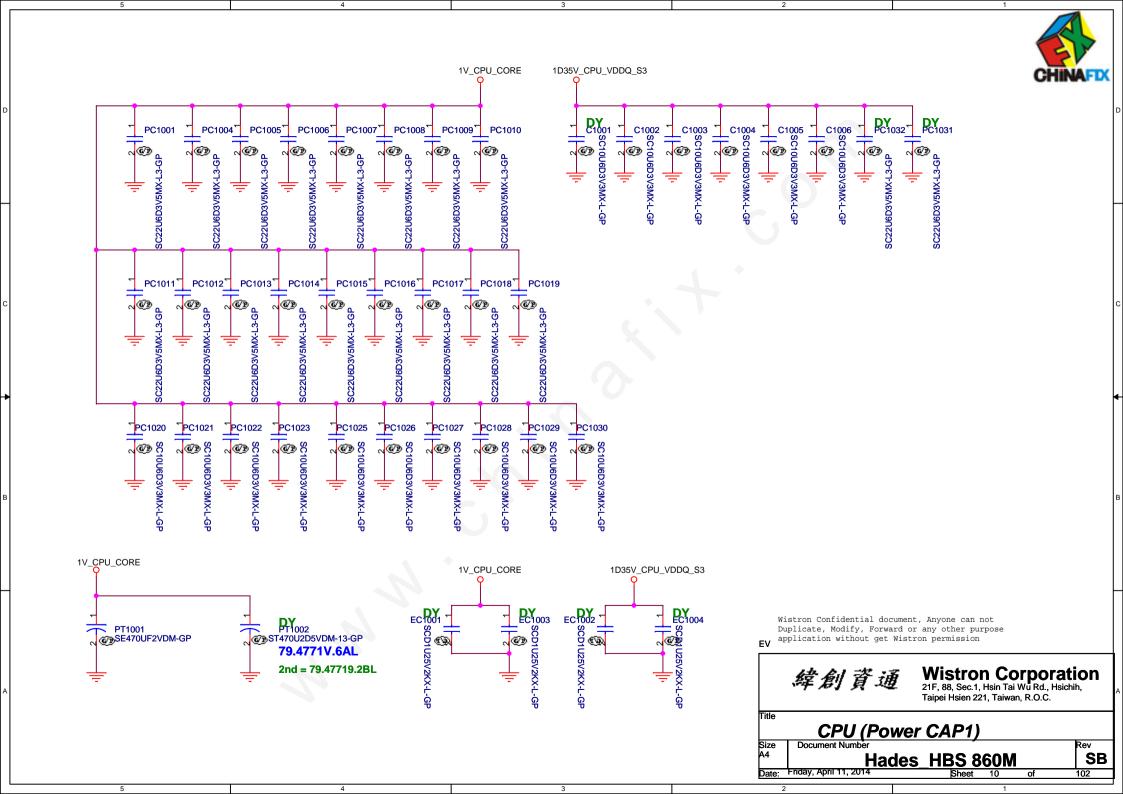


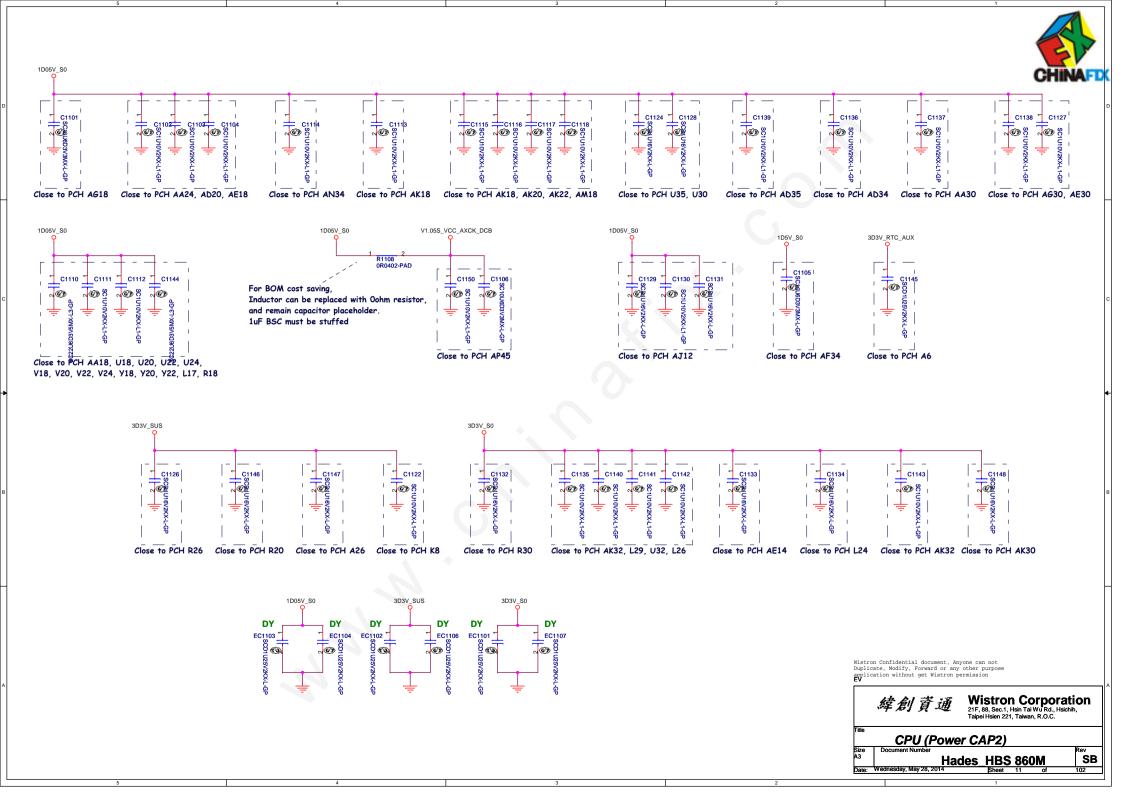


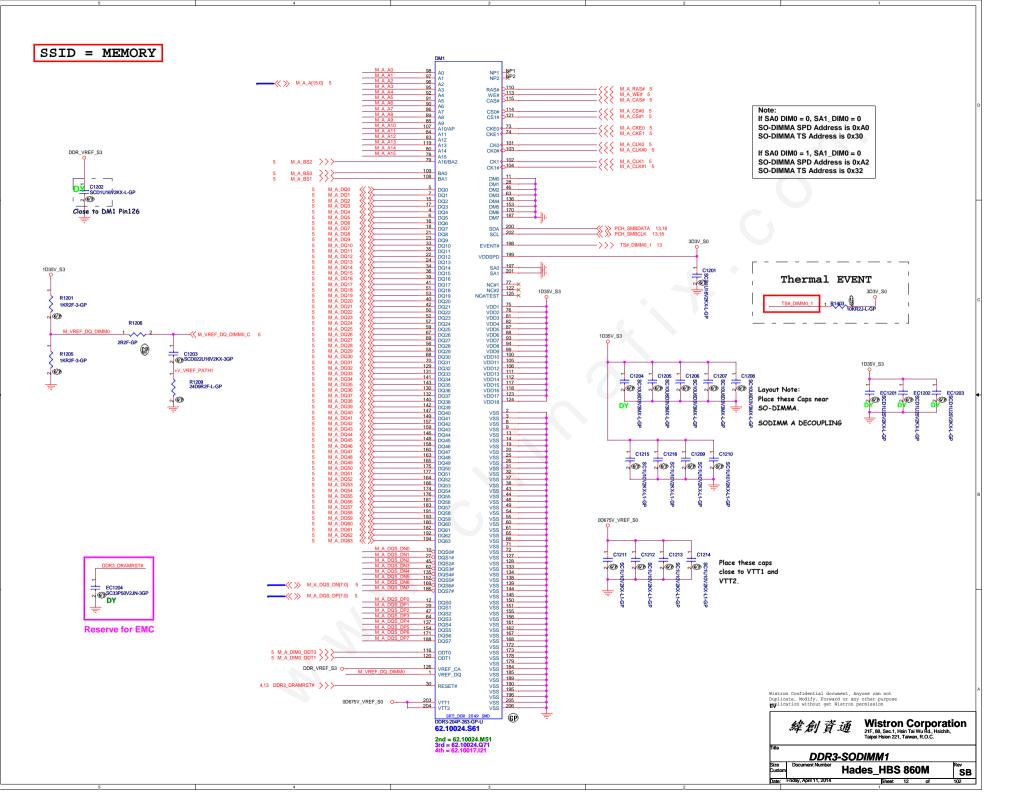
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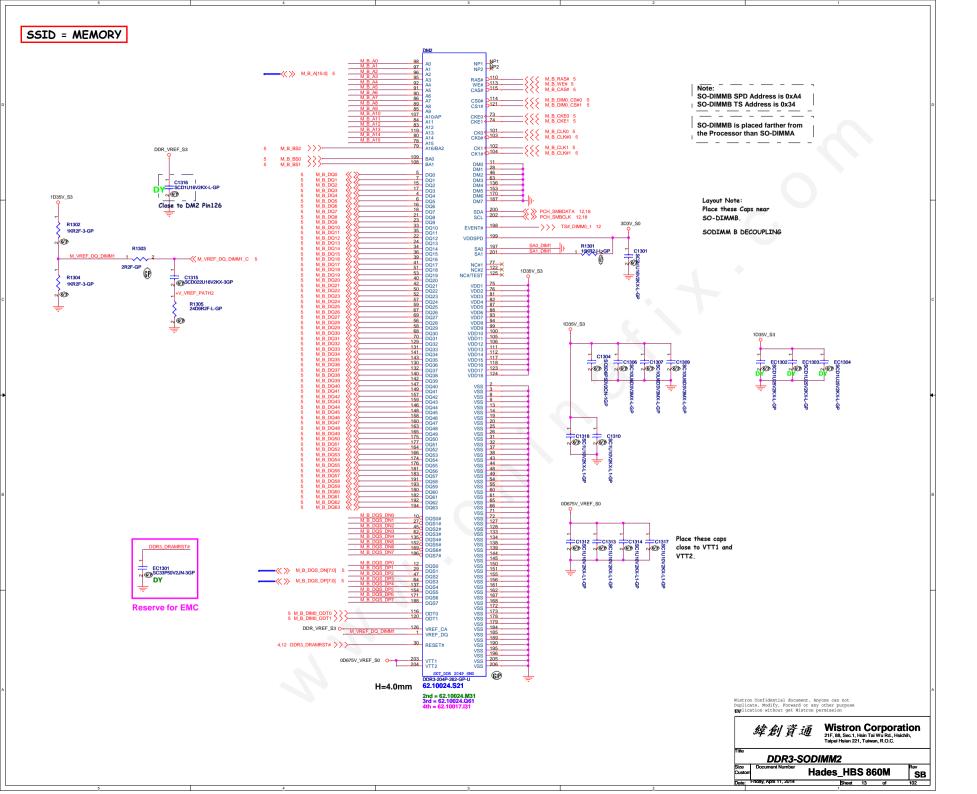






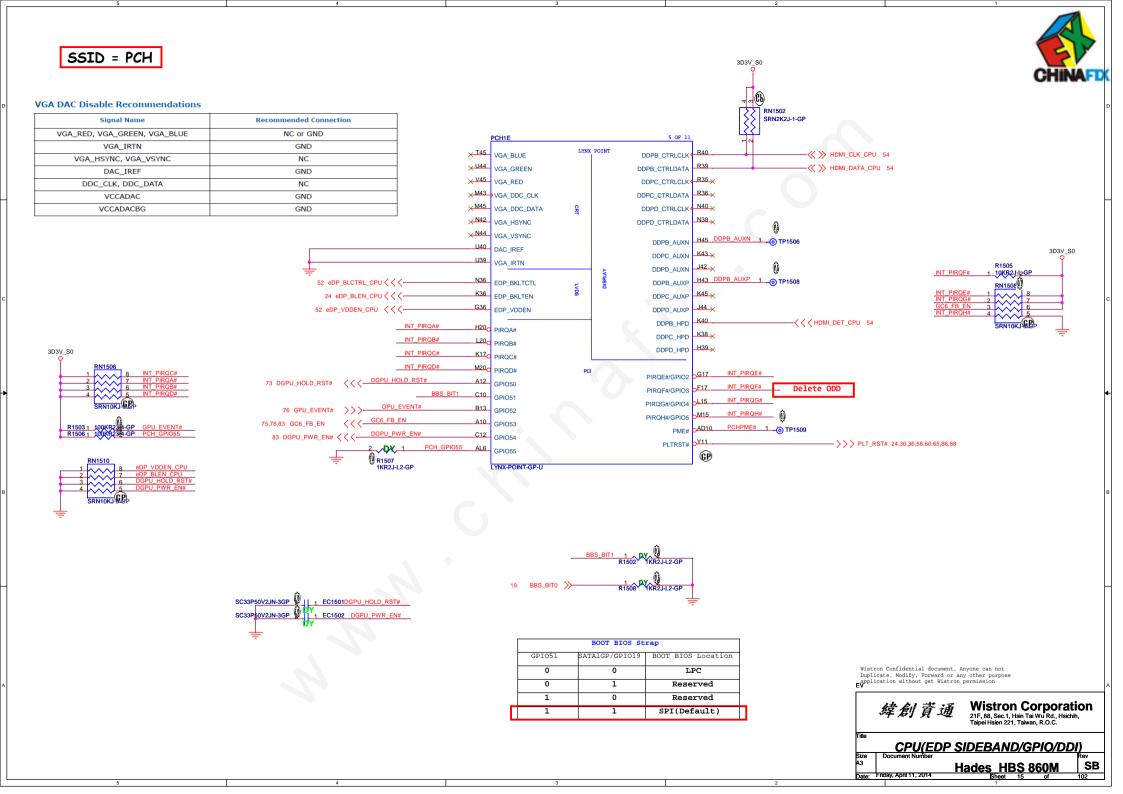


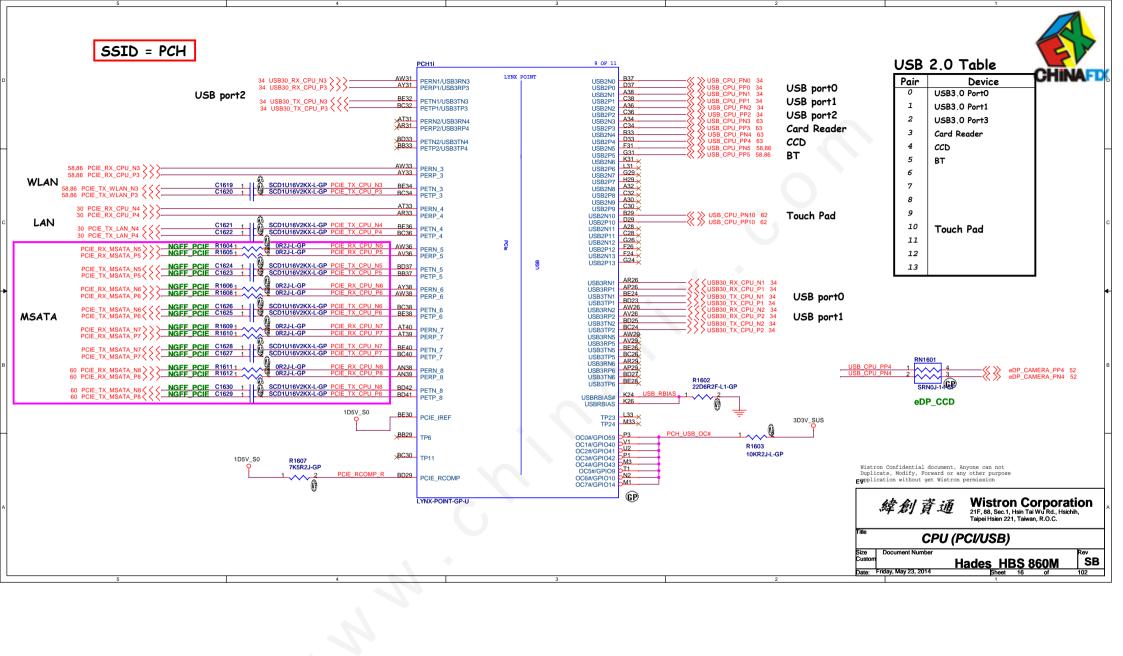


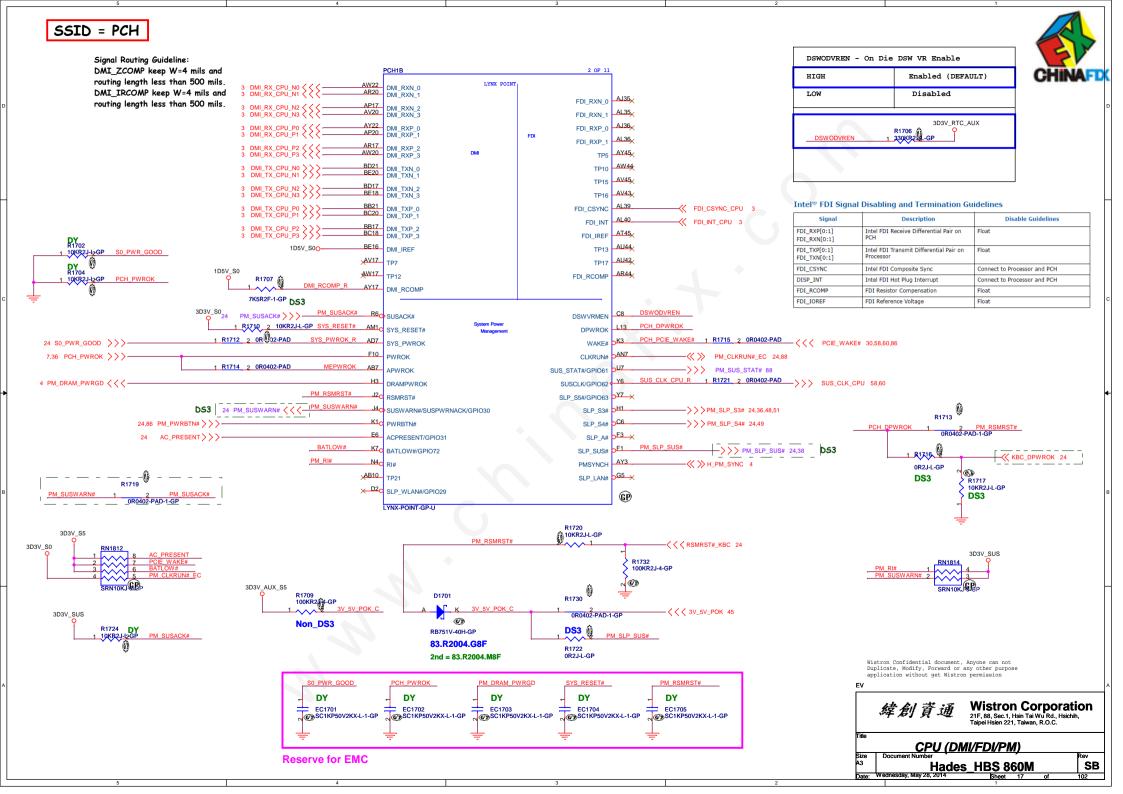


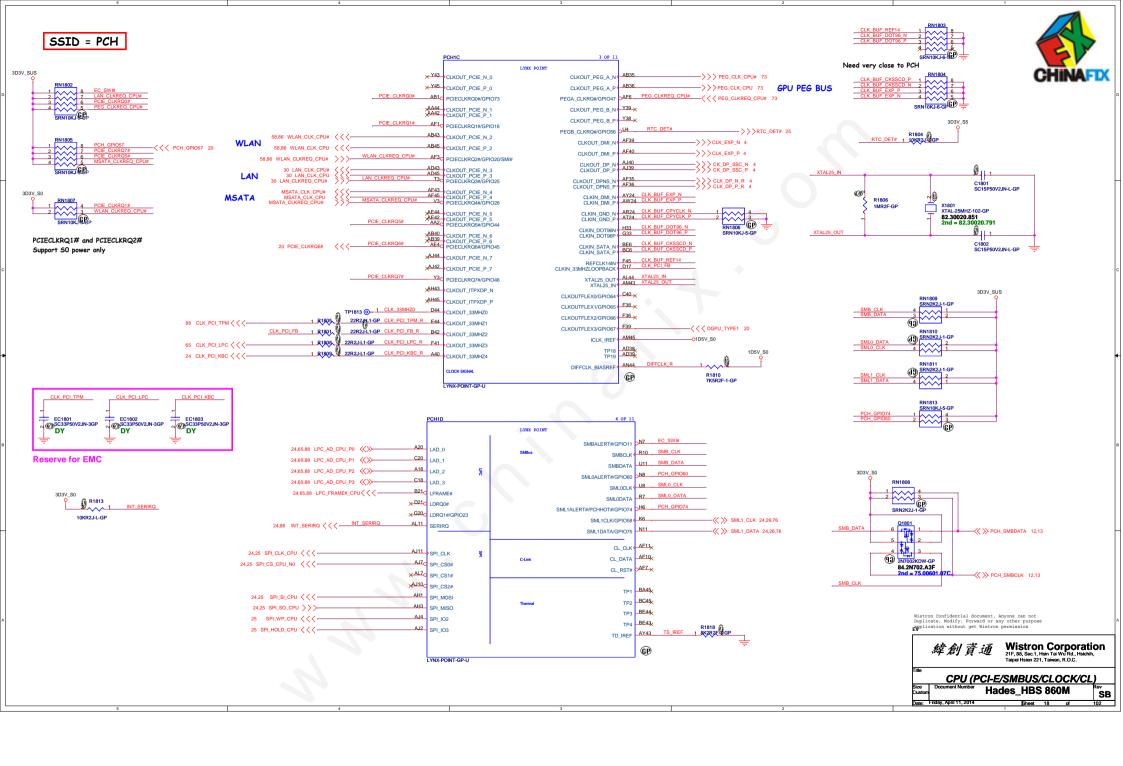


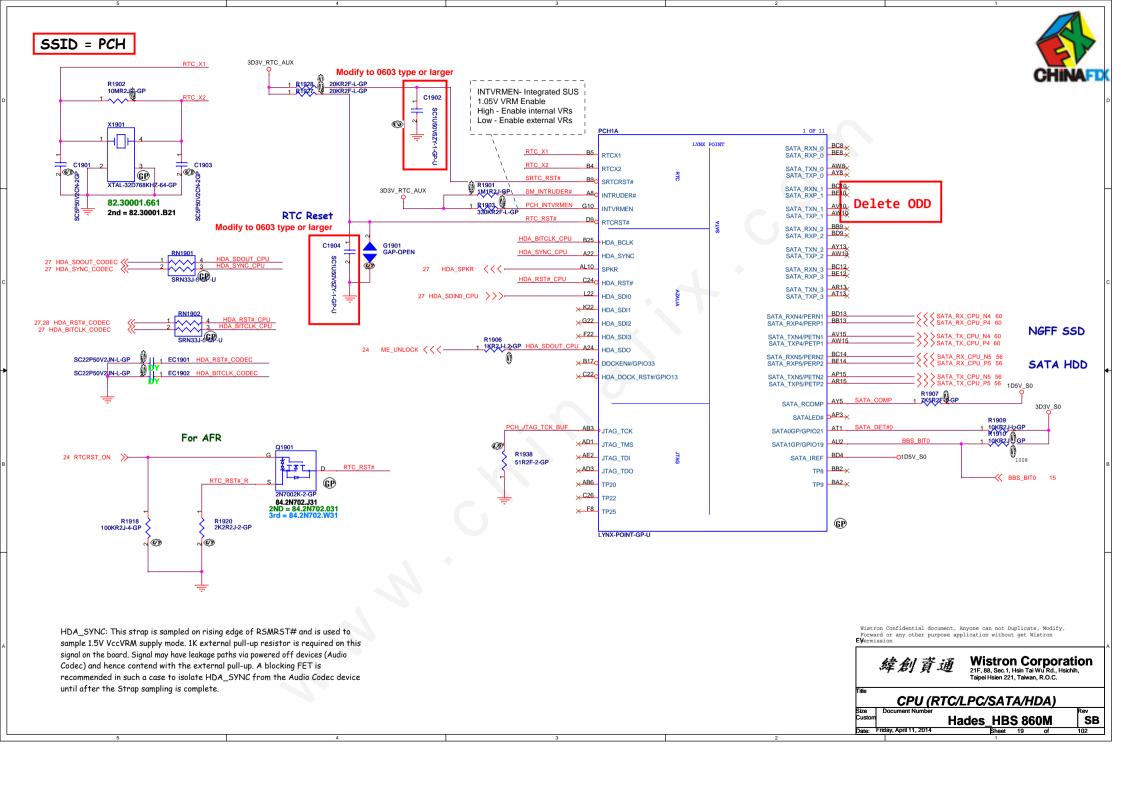


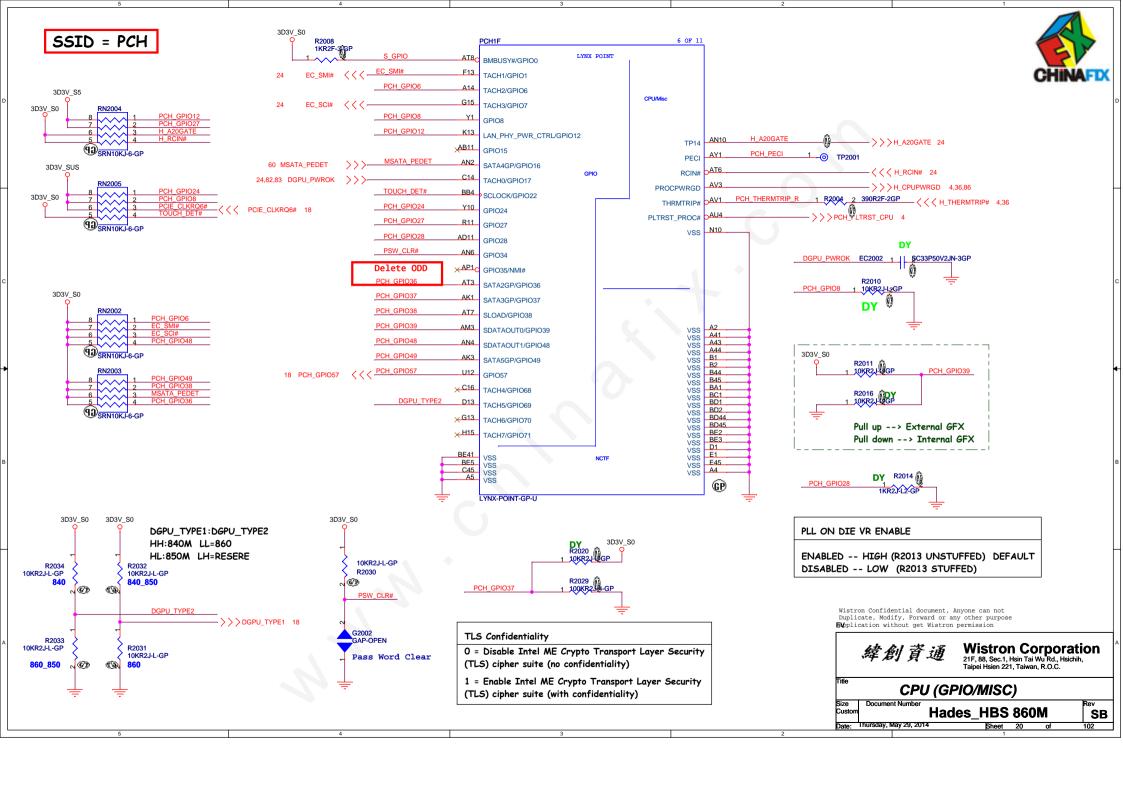




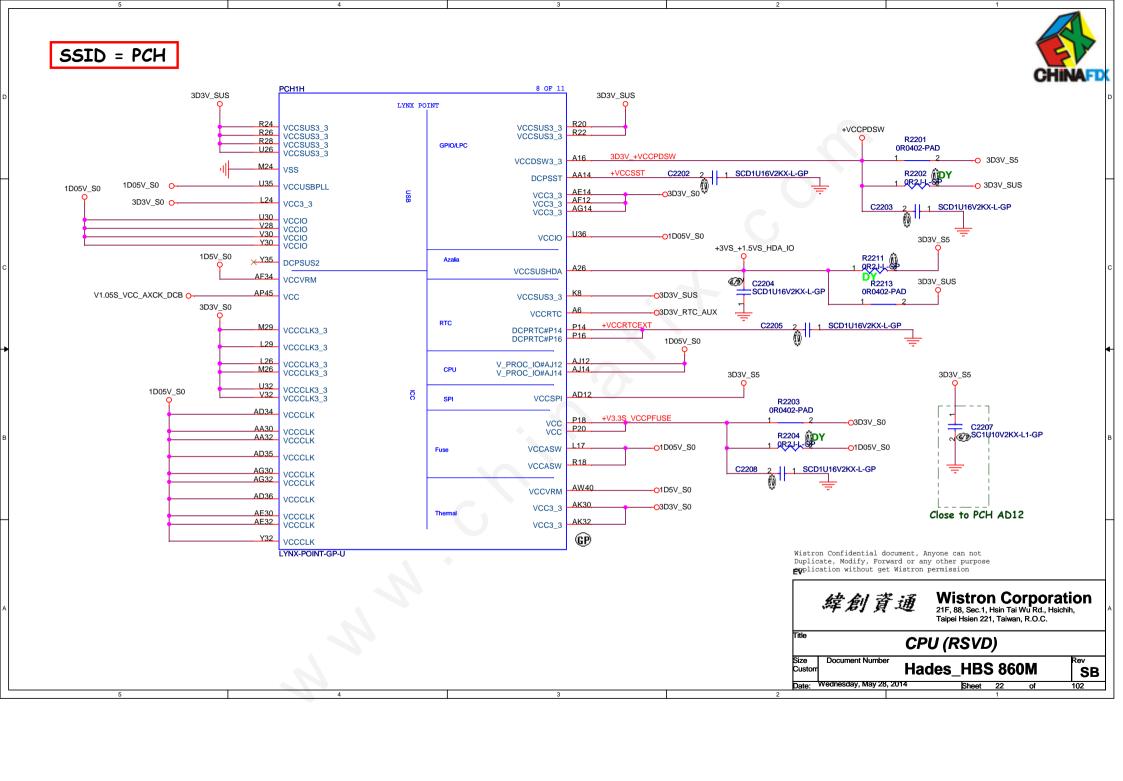






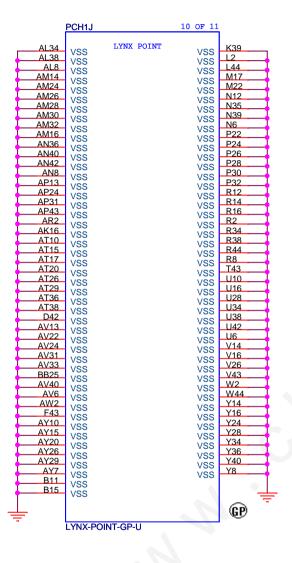


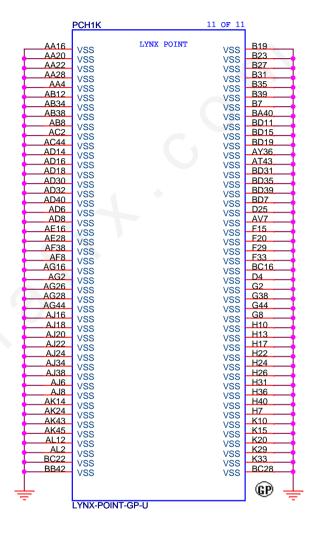
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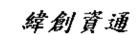
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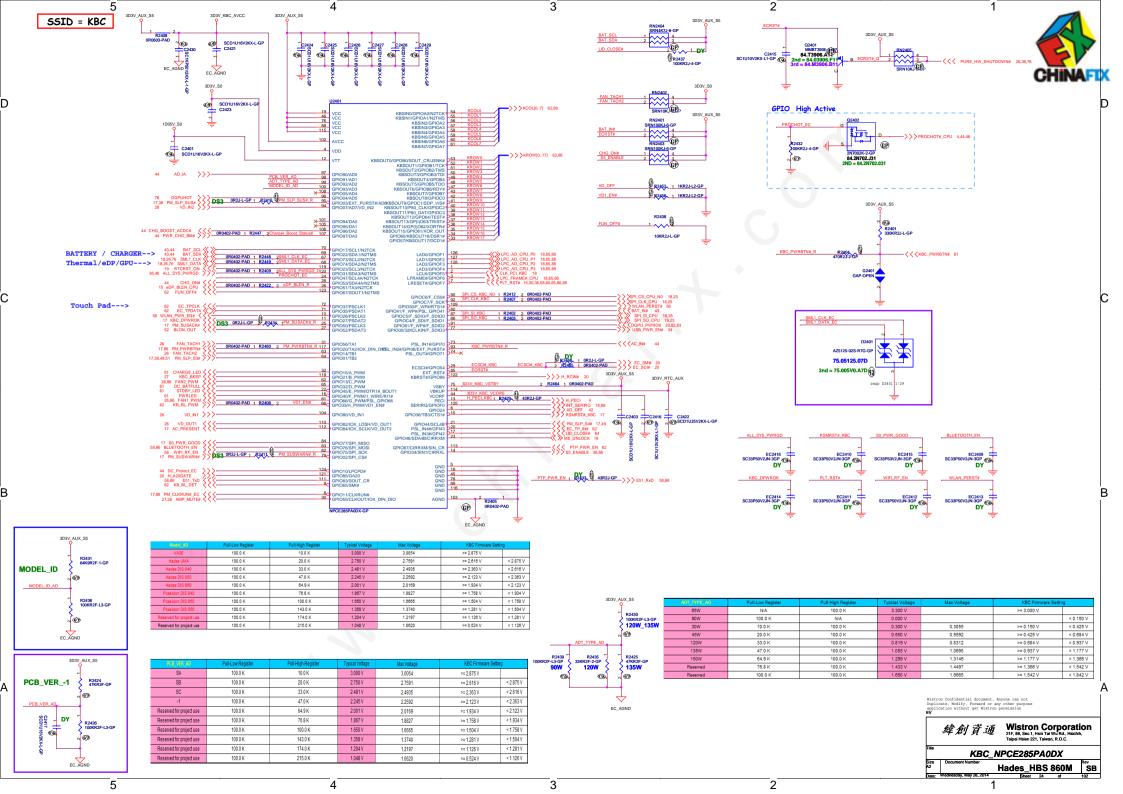
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

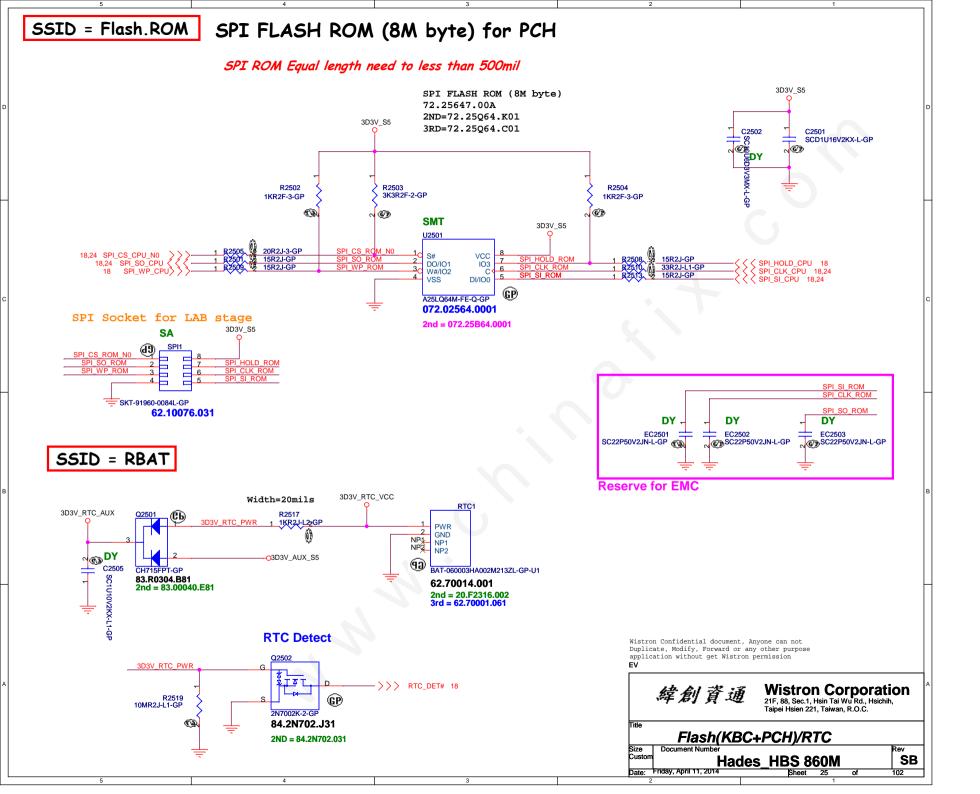
Taipei Hsien 221, Taiwan, R.O.C.

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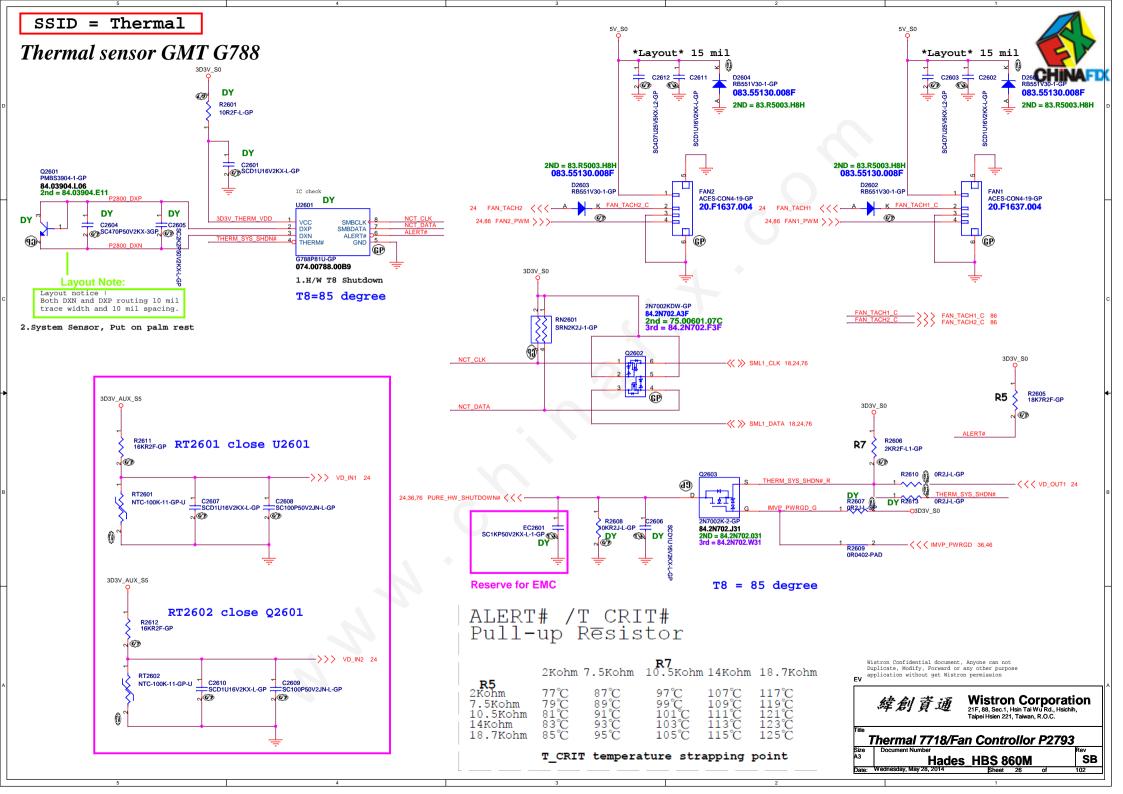
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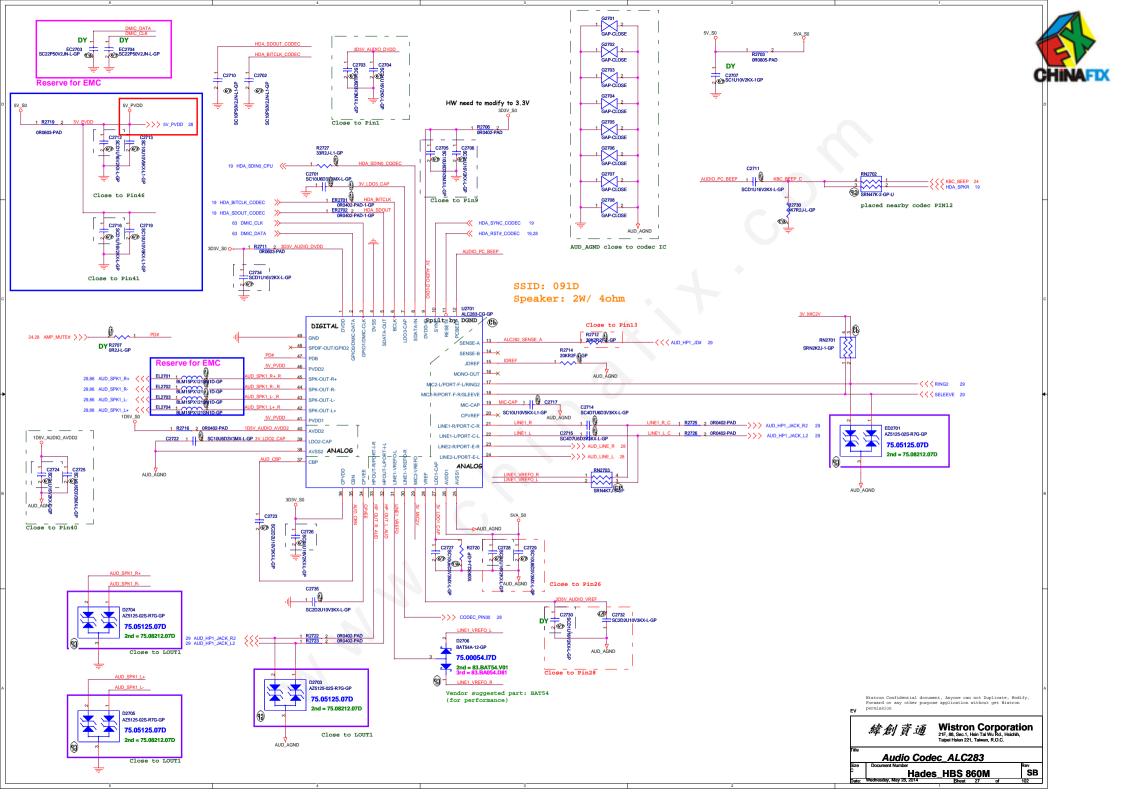
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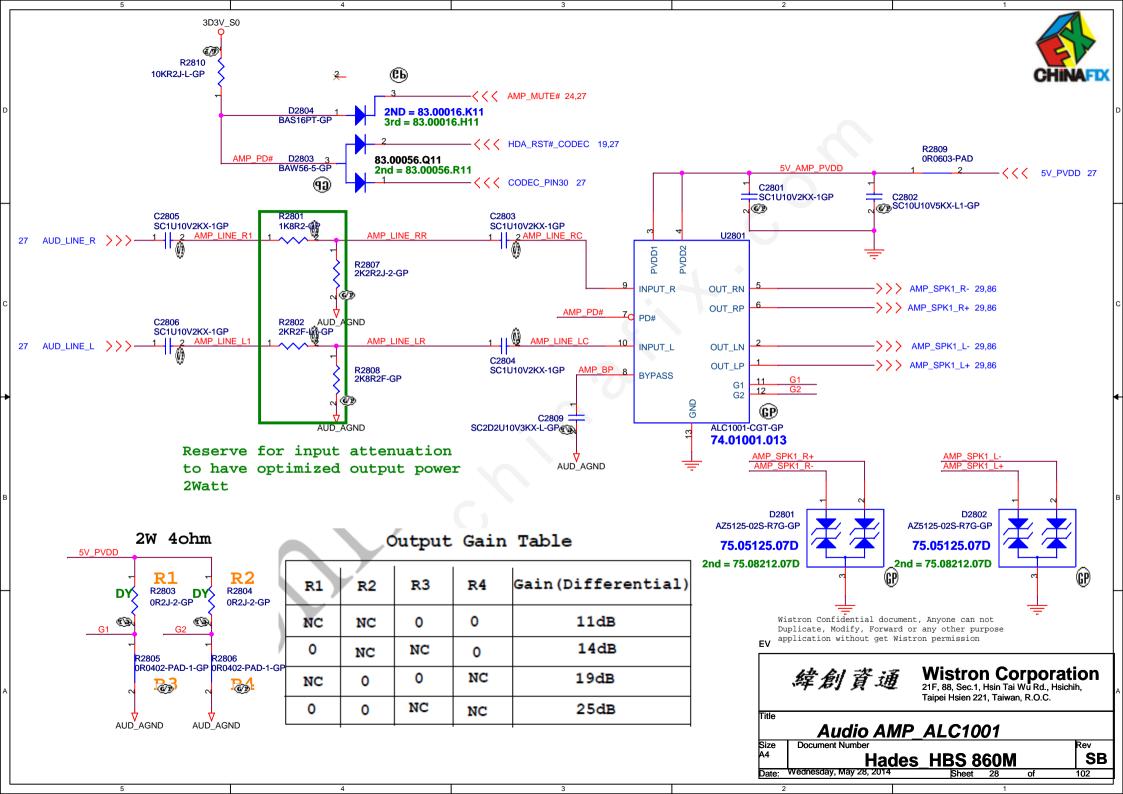


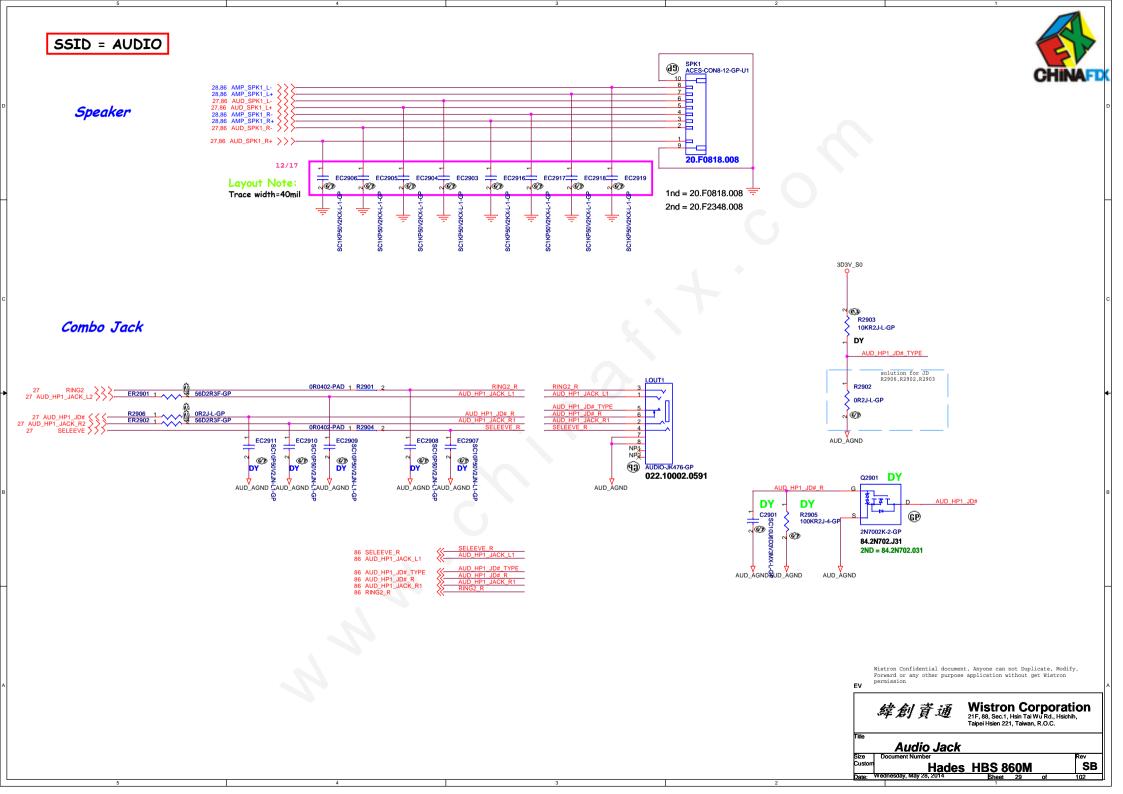




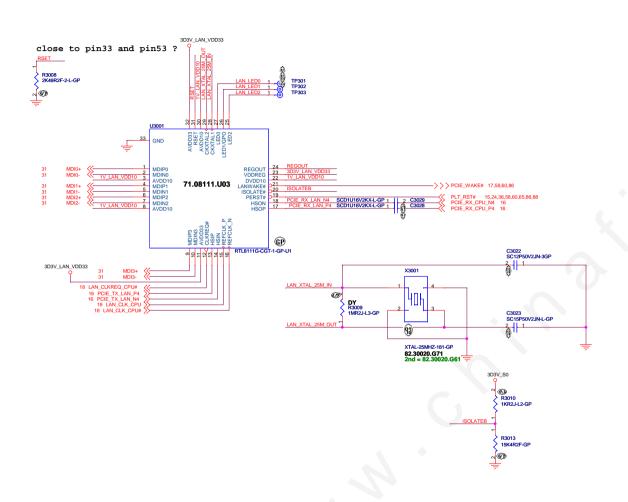


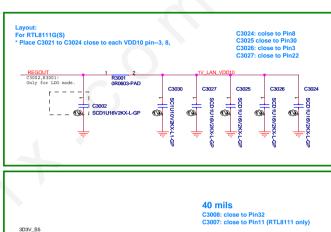


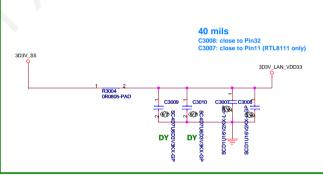






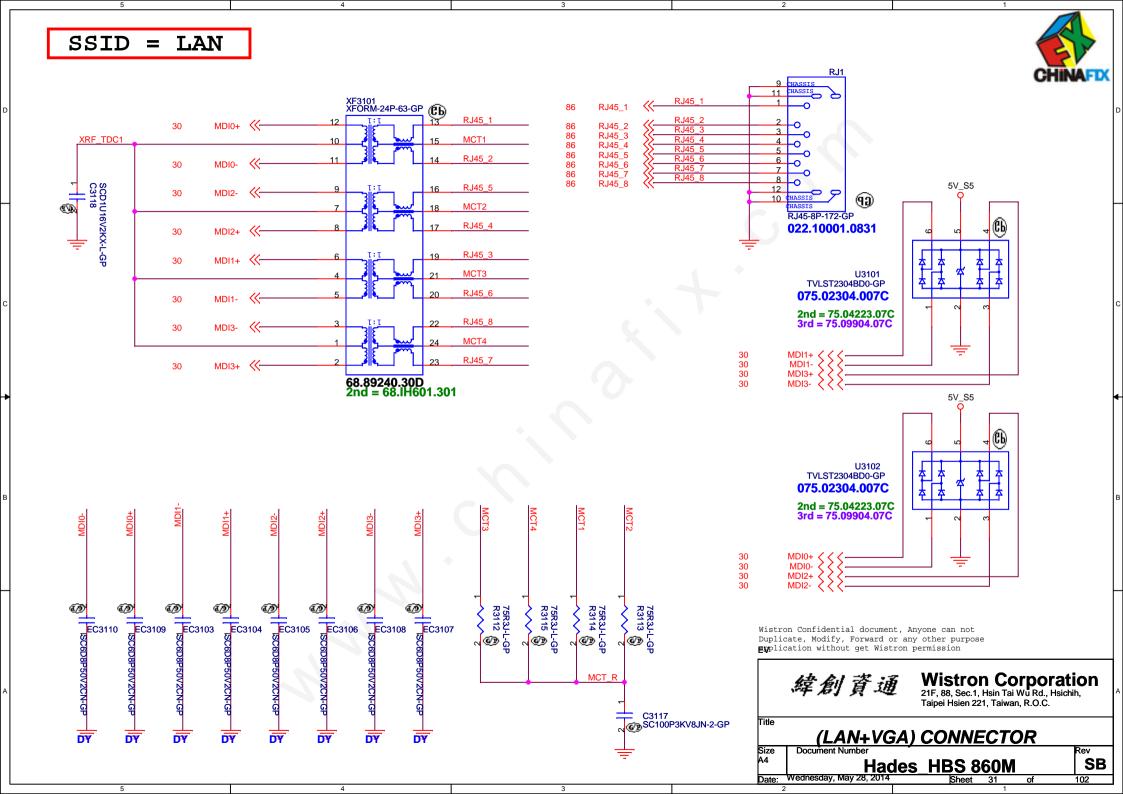


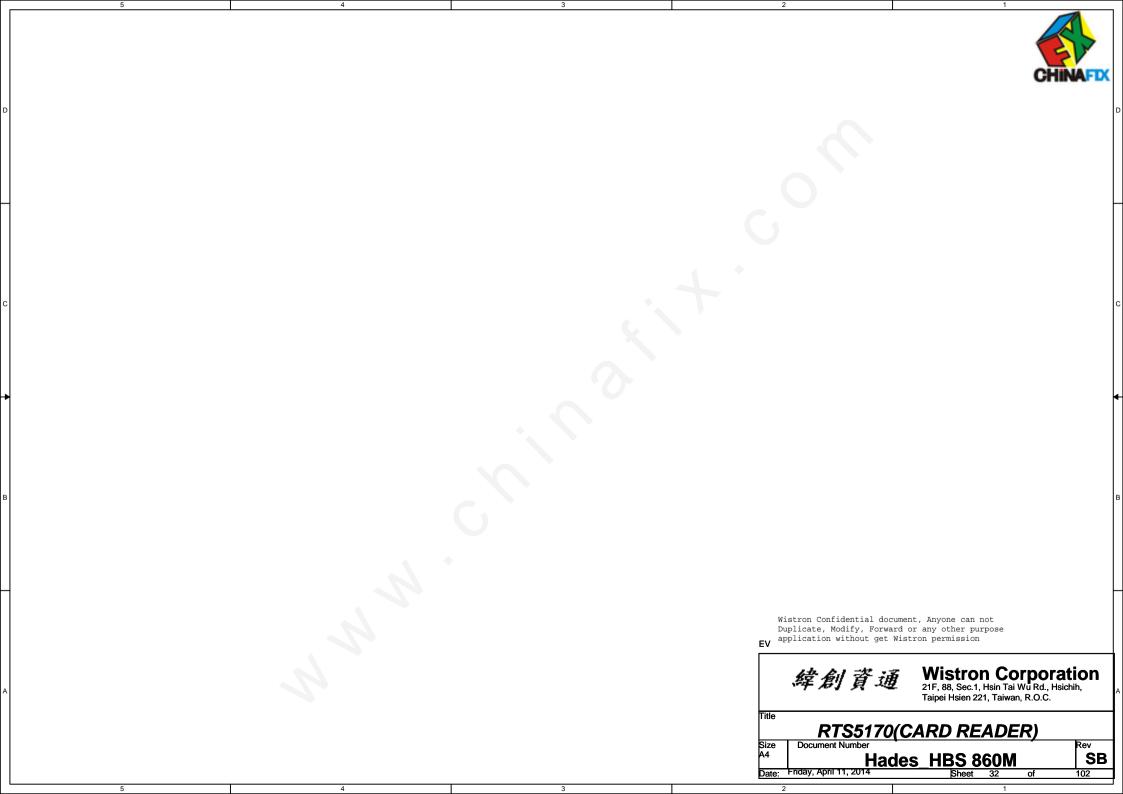


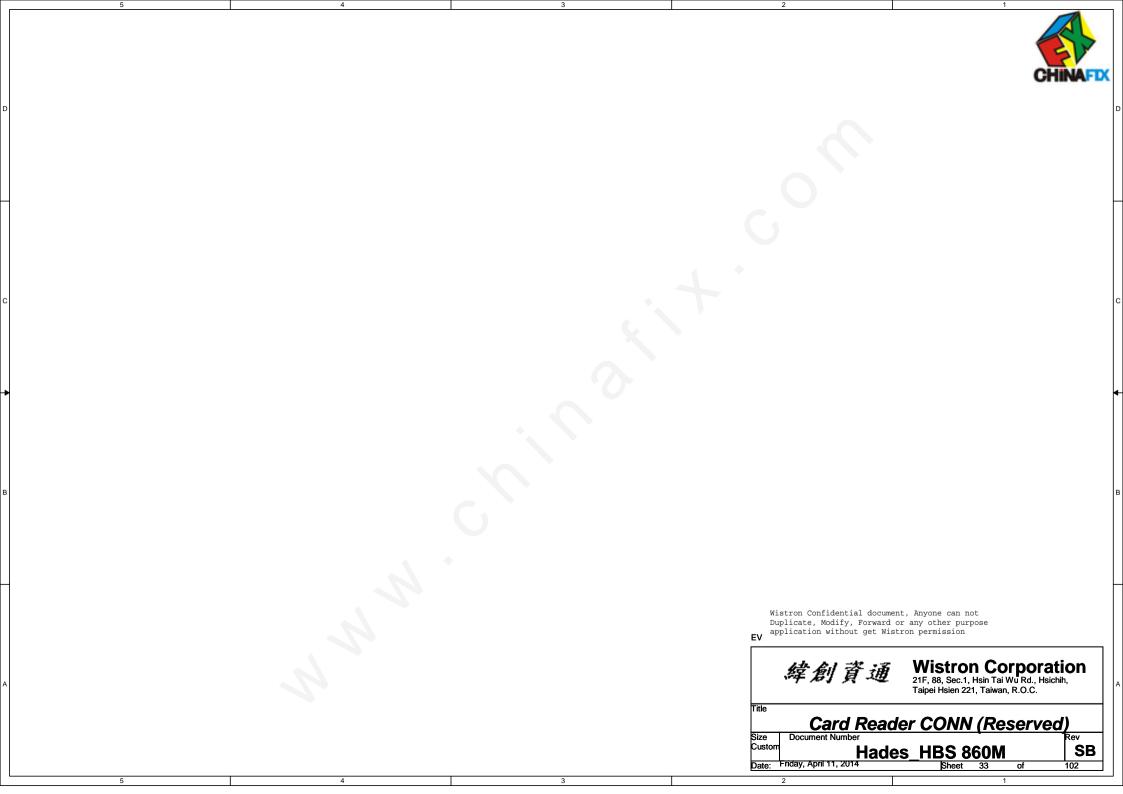


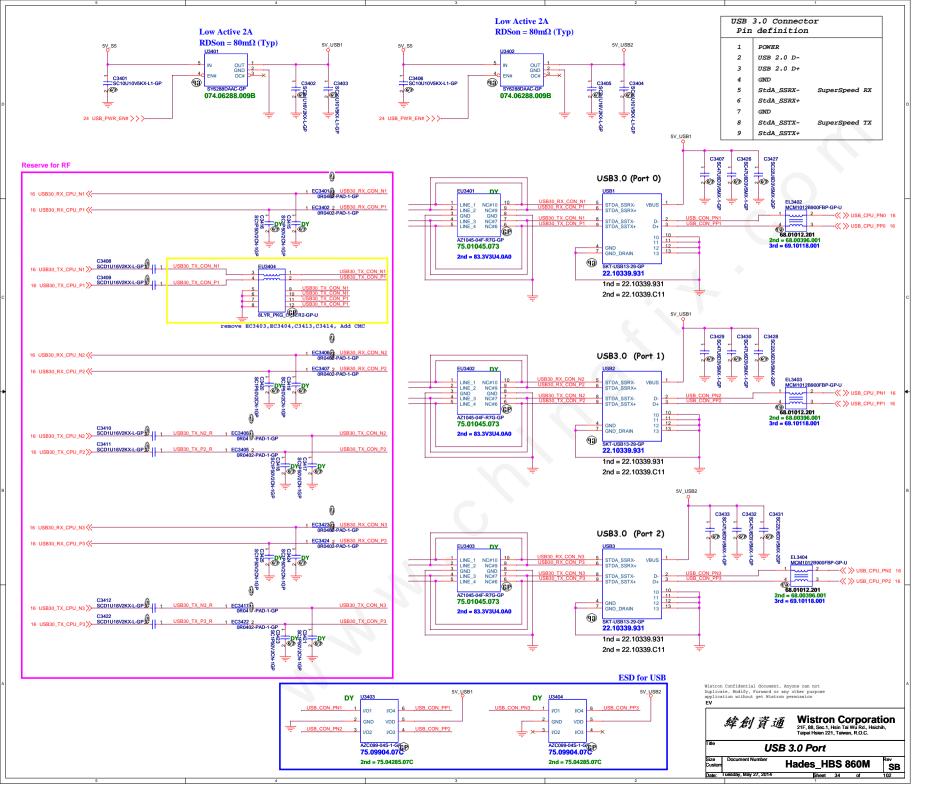
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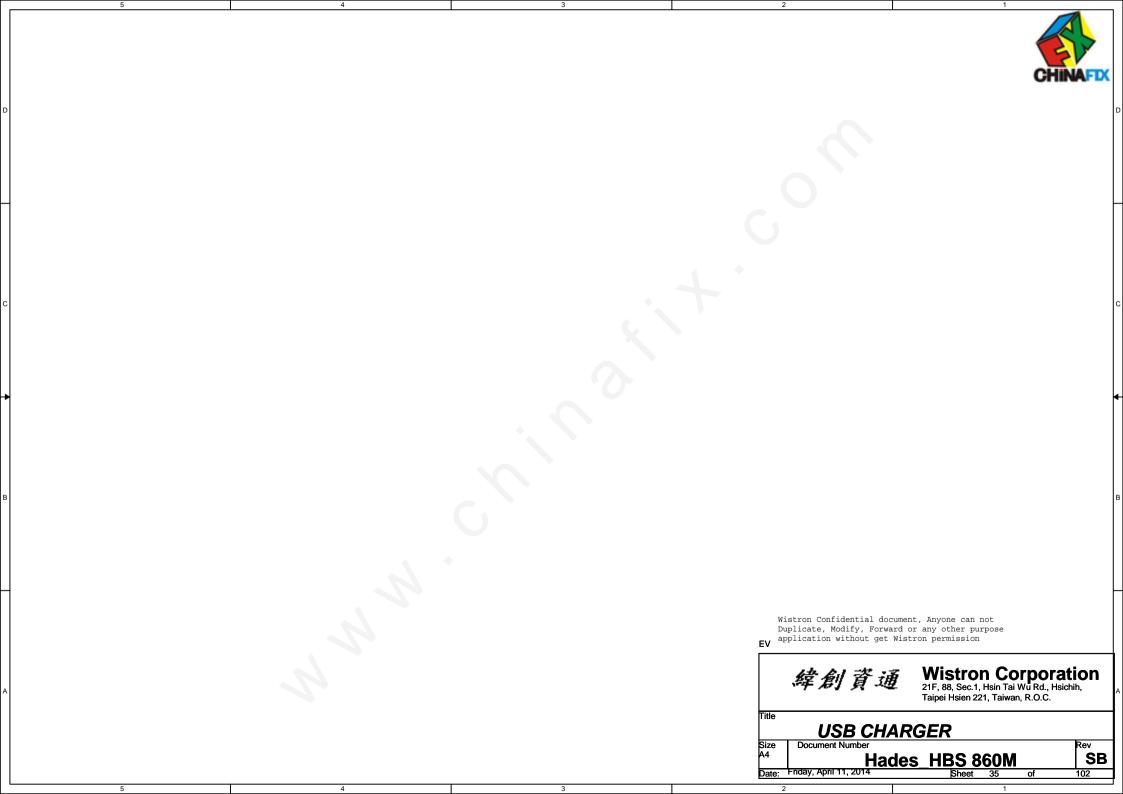






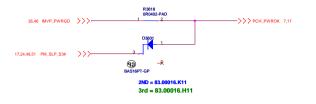


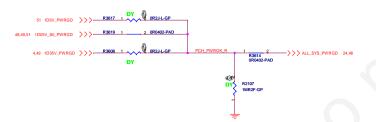




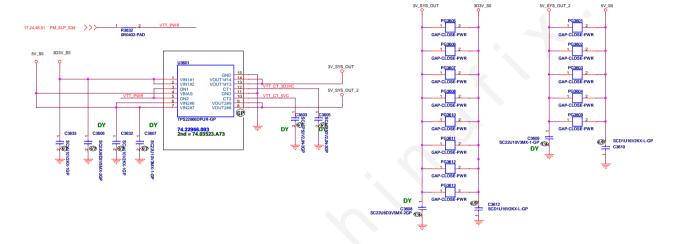
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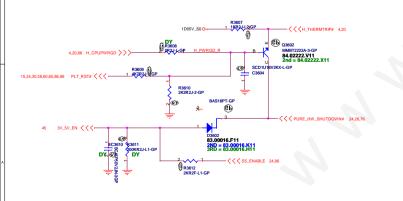




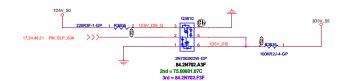


ANNIE Run Power



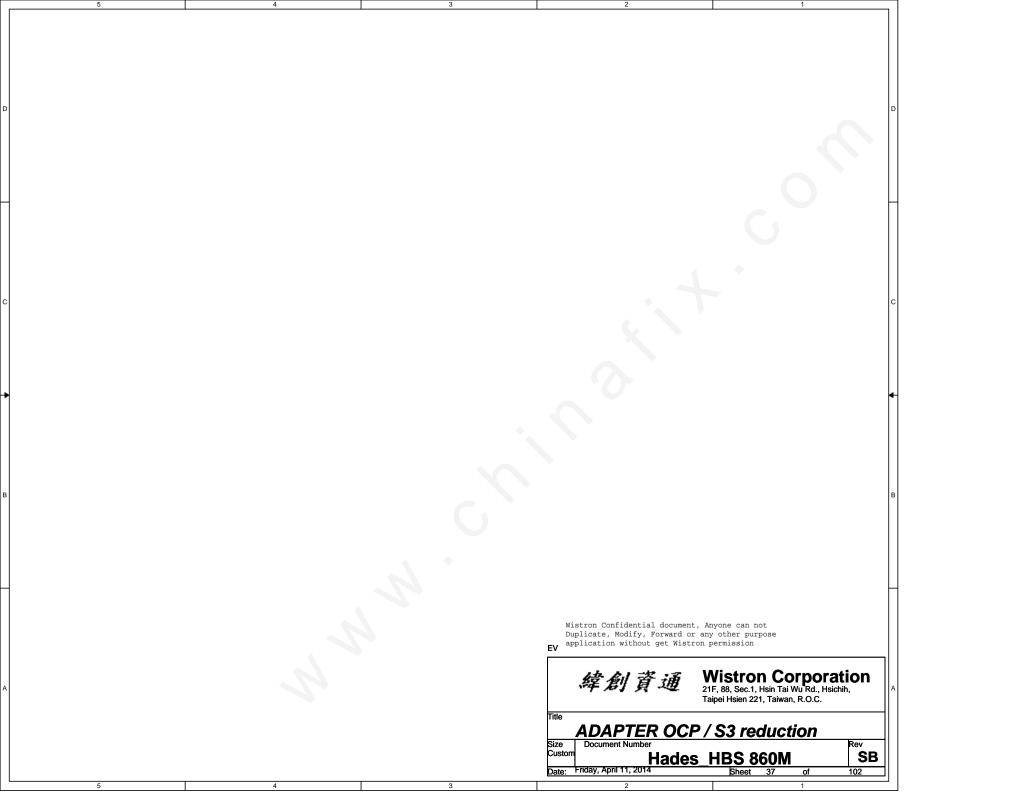


Discharge Circuit



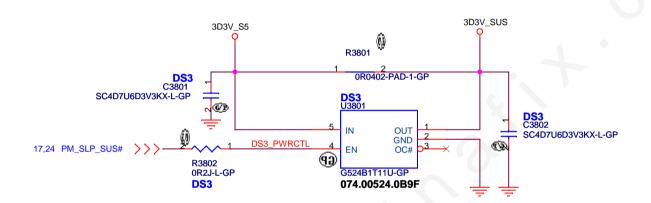
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Power Plane Enable & SEQUENCE





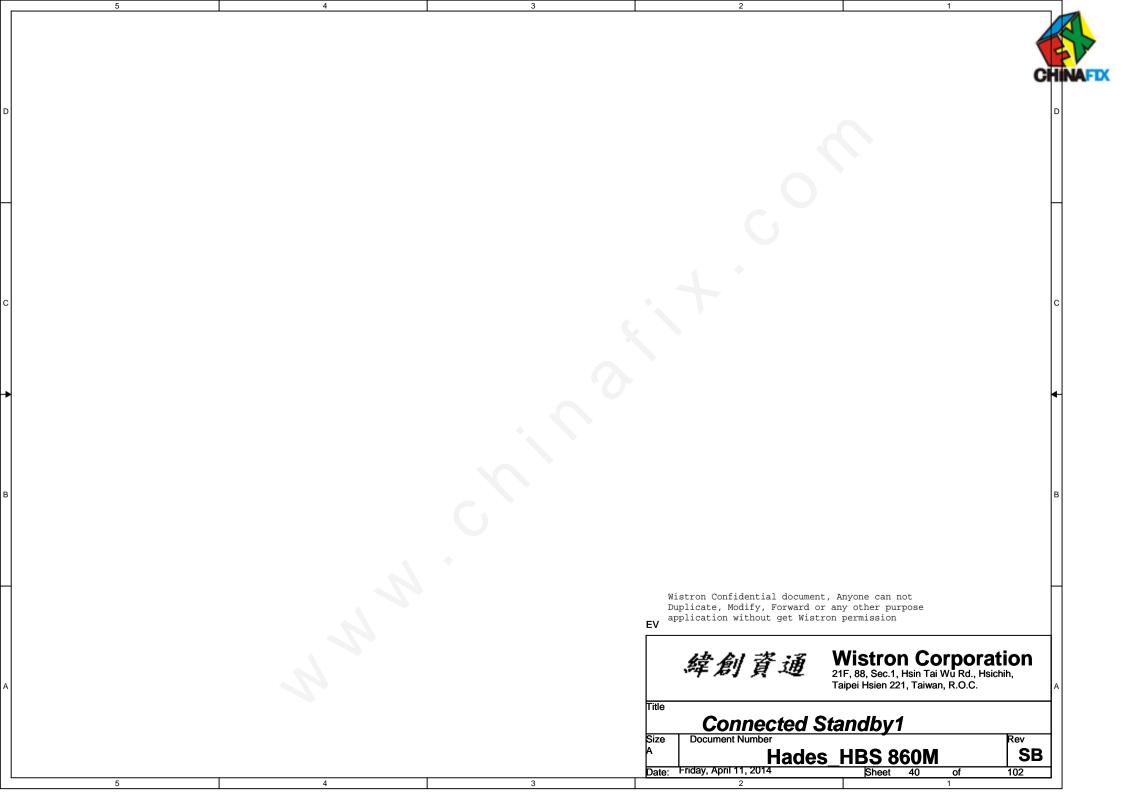


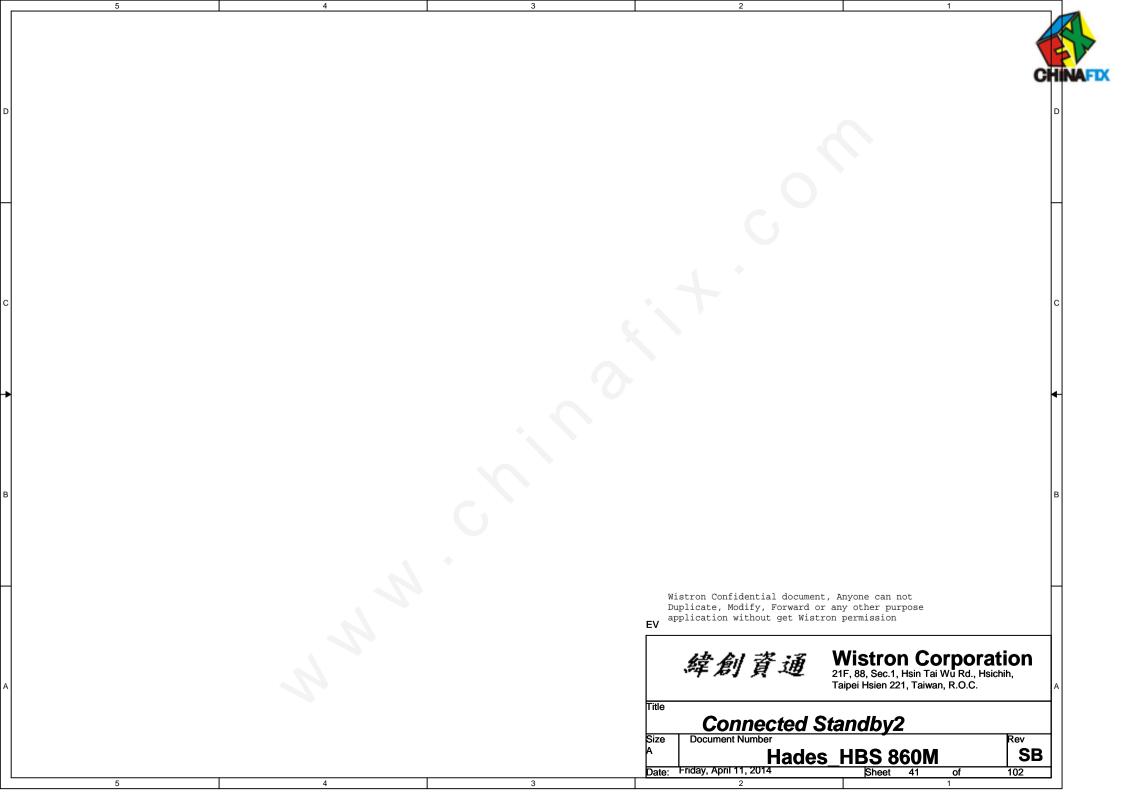


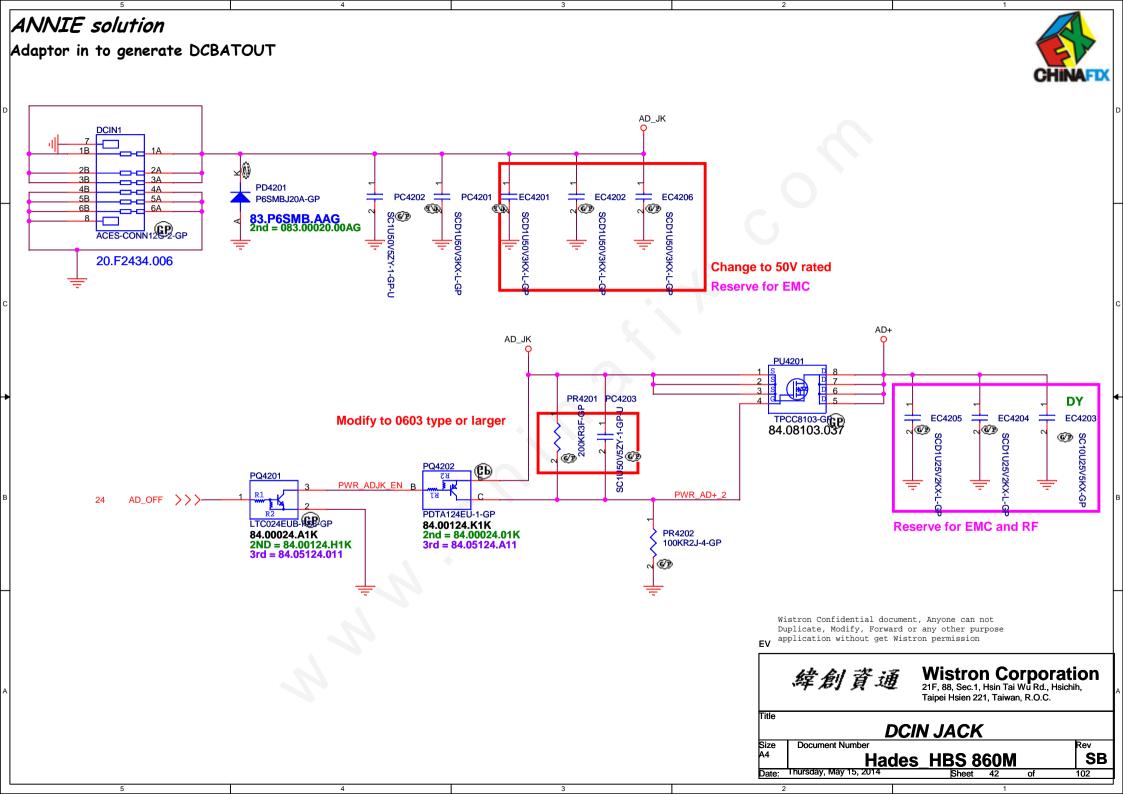
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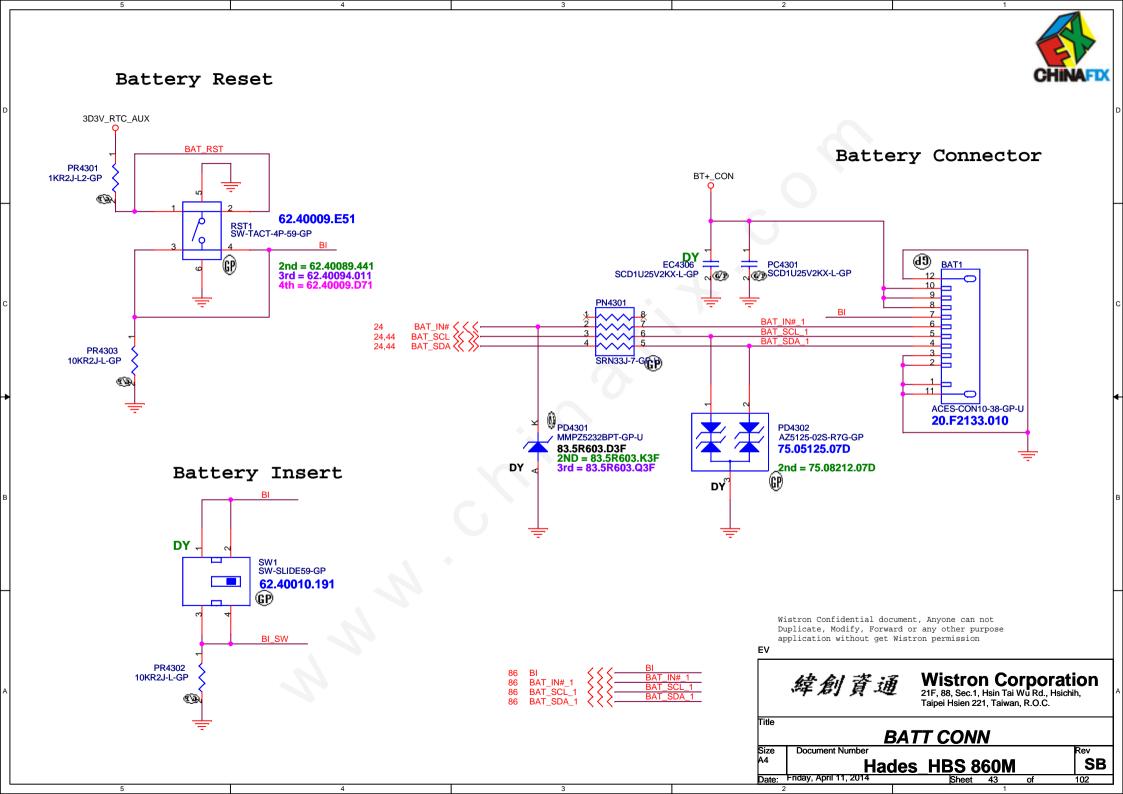
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Date:	Thursday, May 22, 2014	Sheet	38	of	102

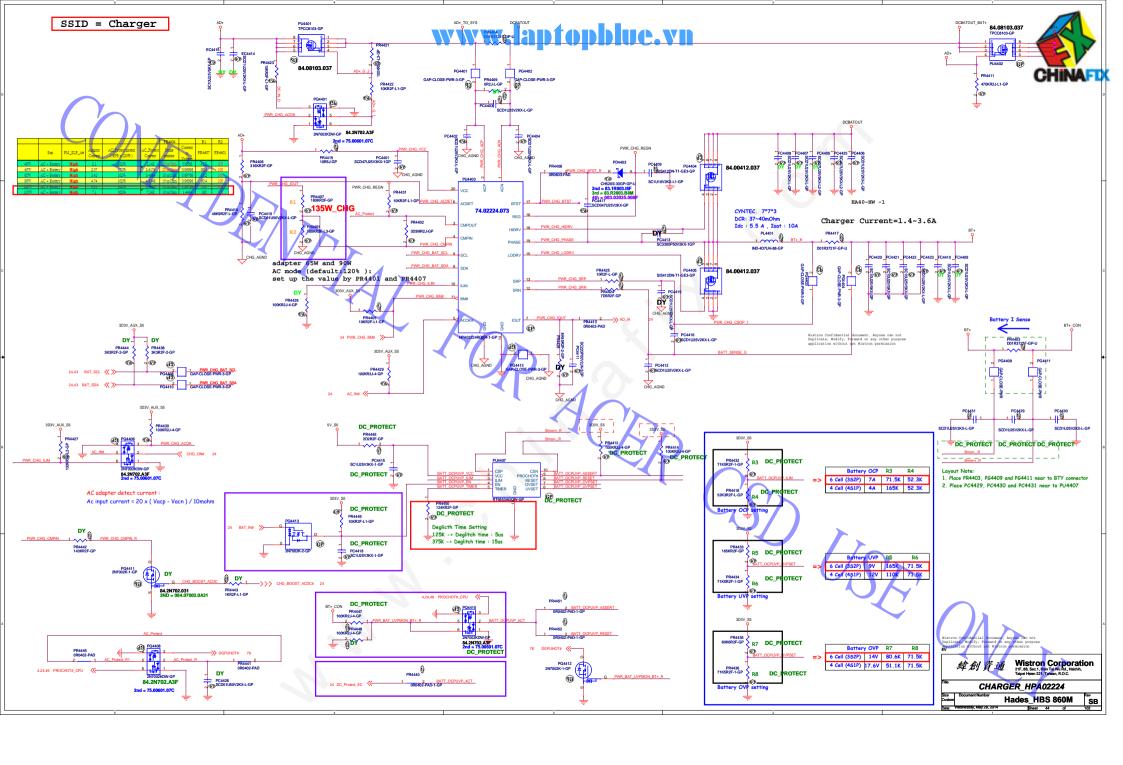
Power Sequence Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. 1D05_M SB 102



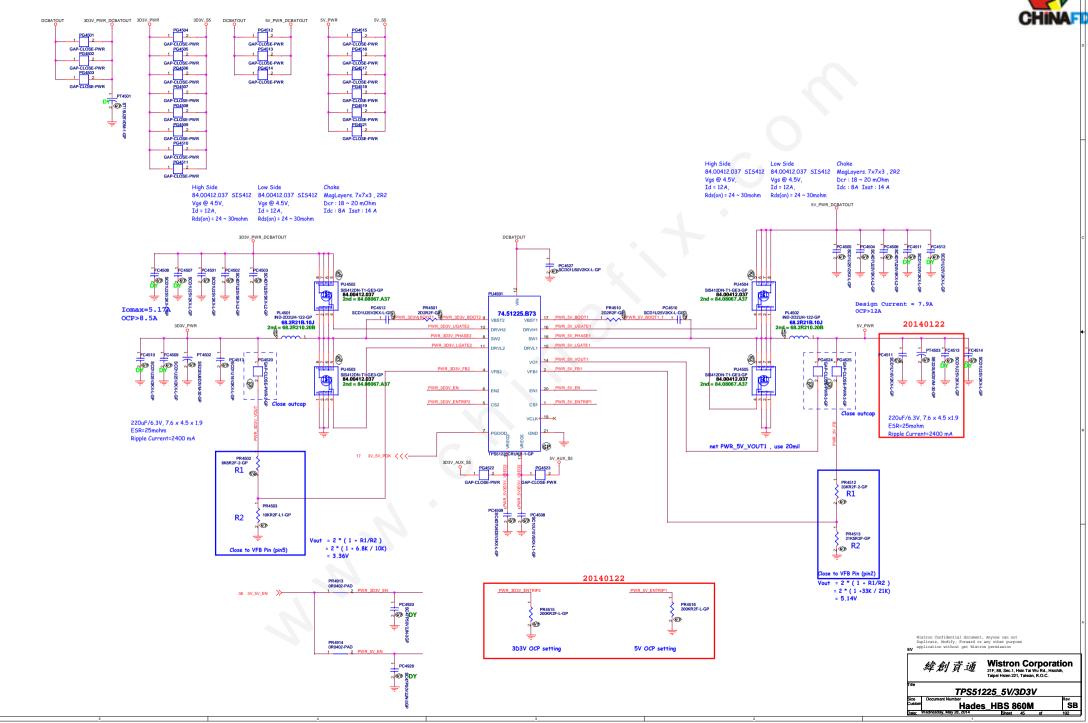


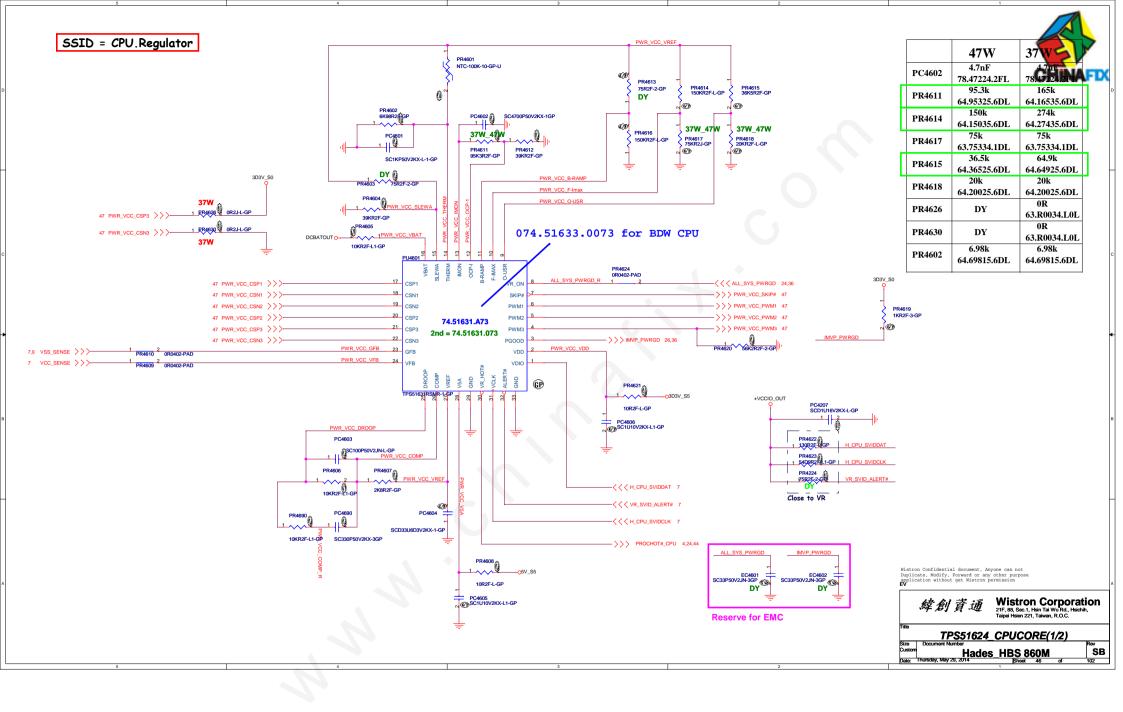


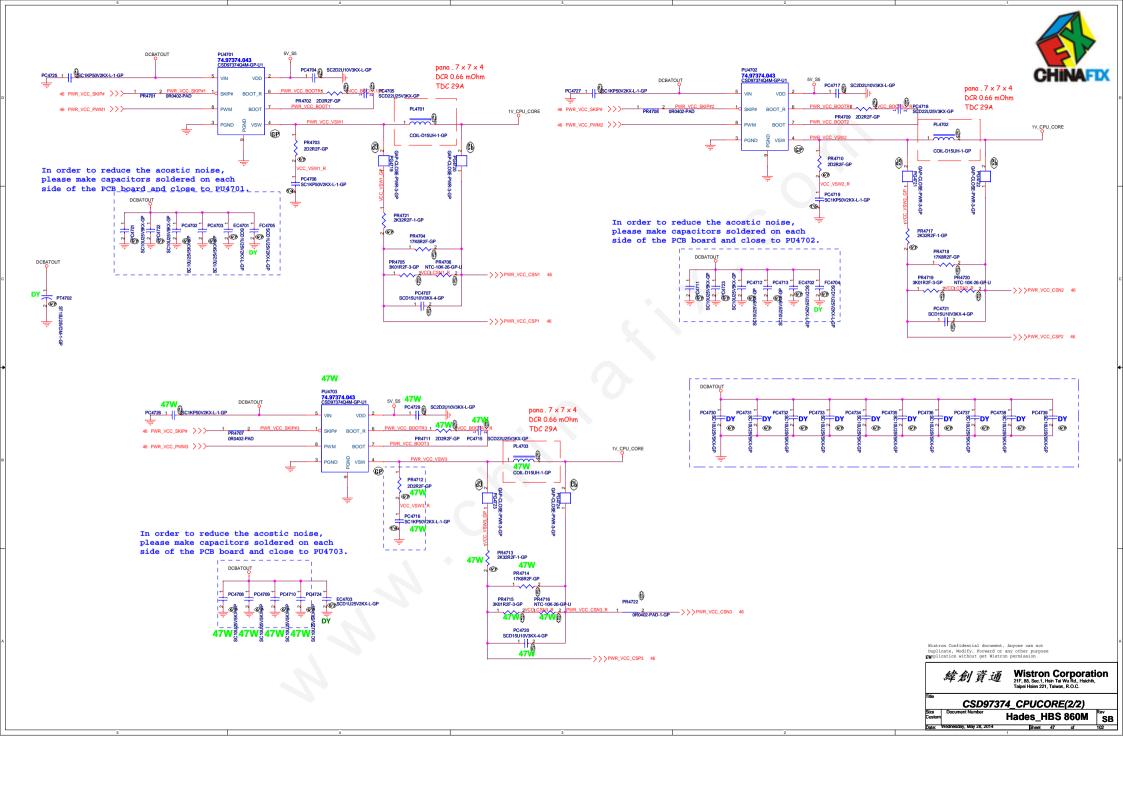


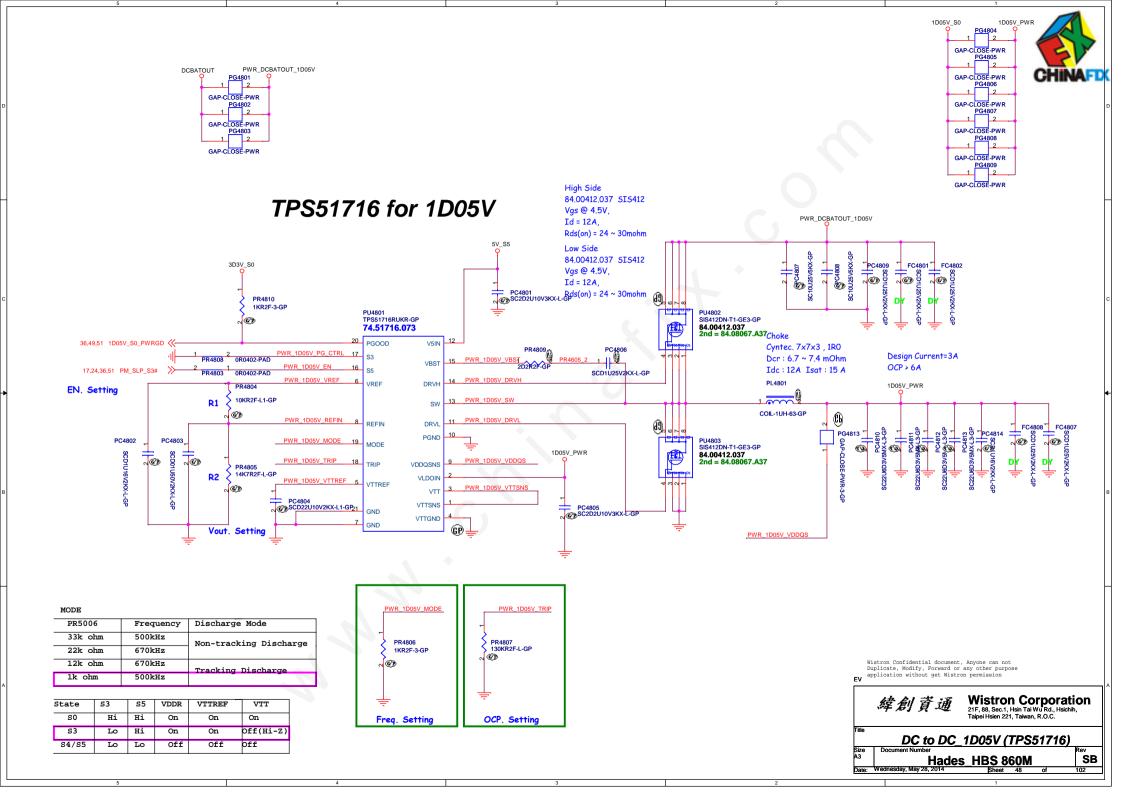


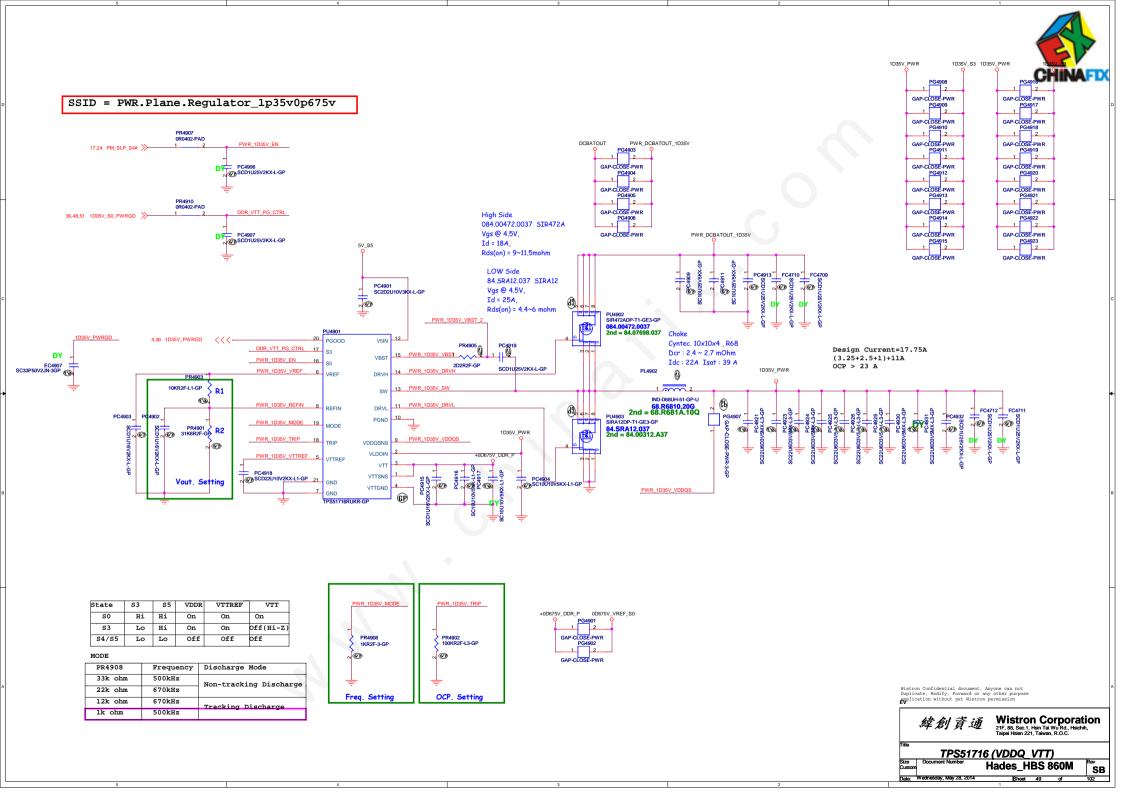


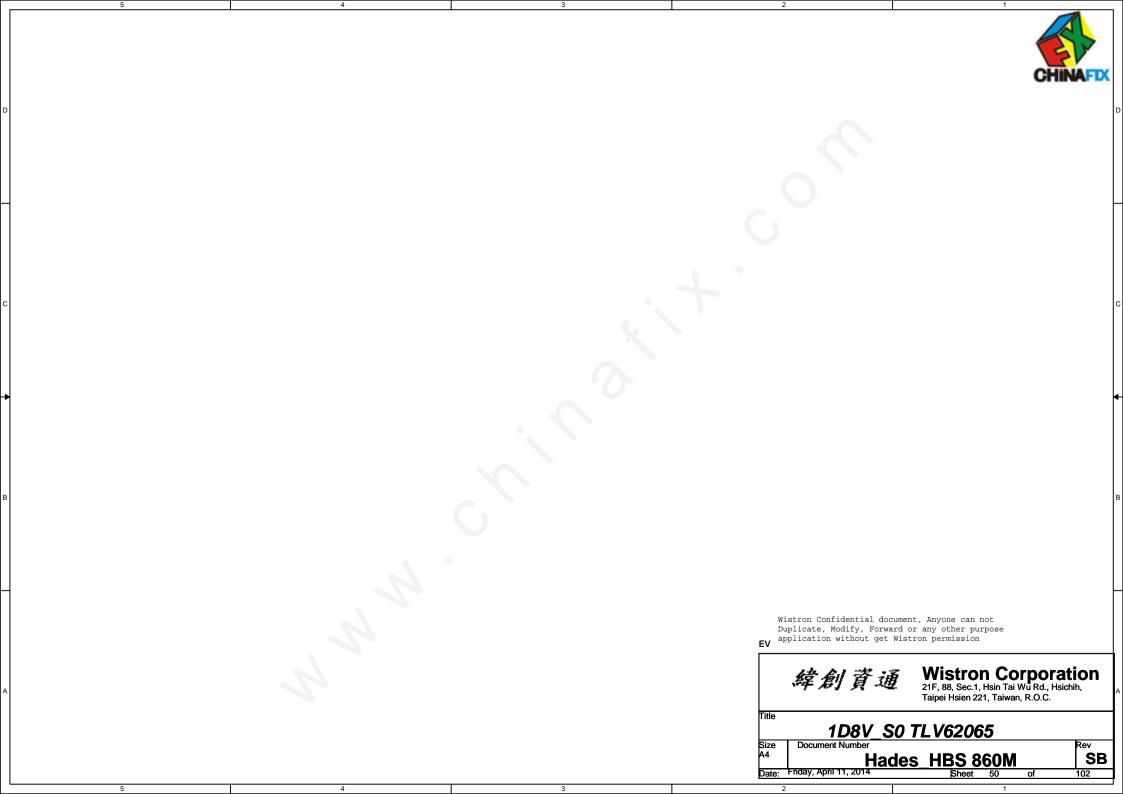




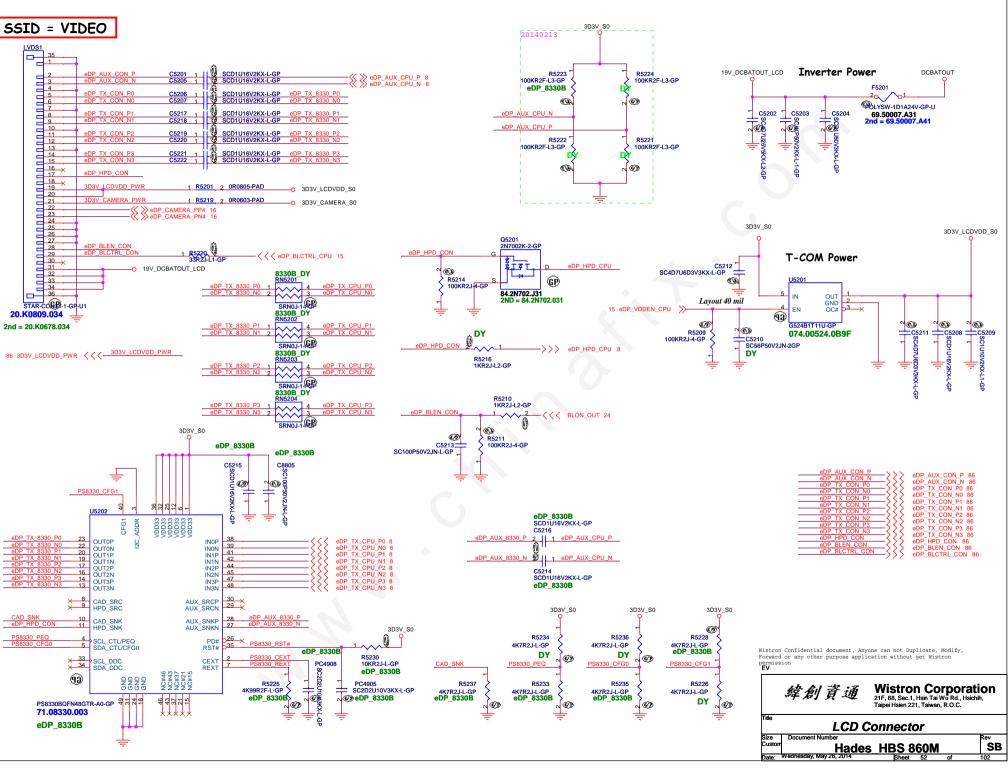




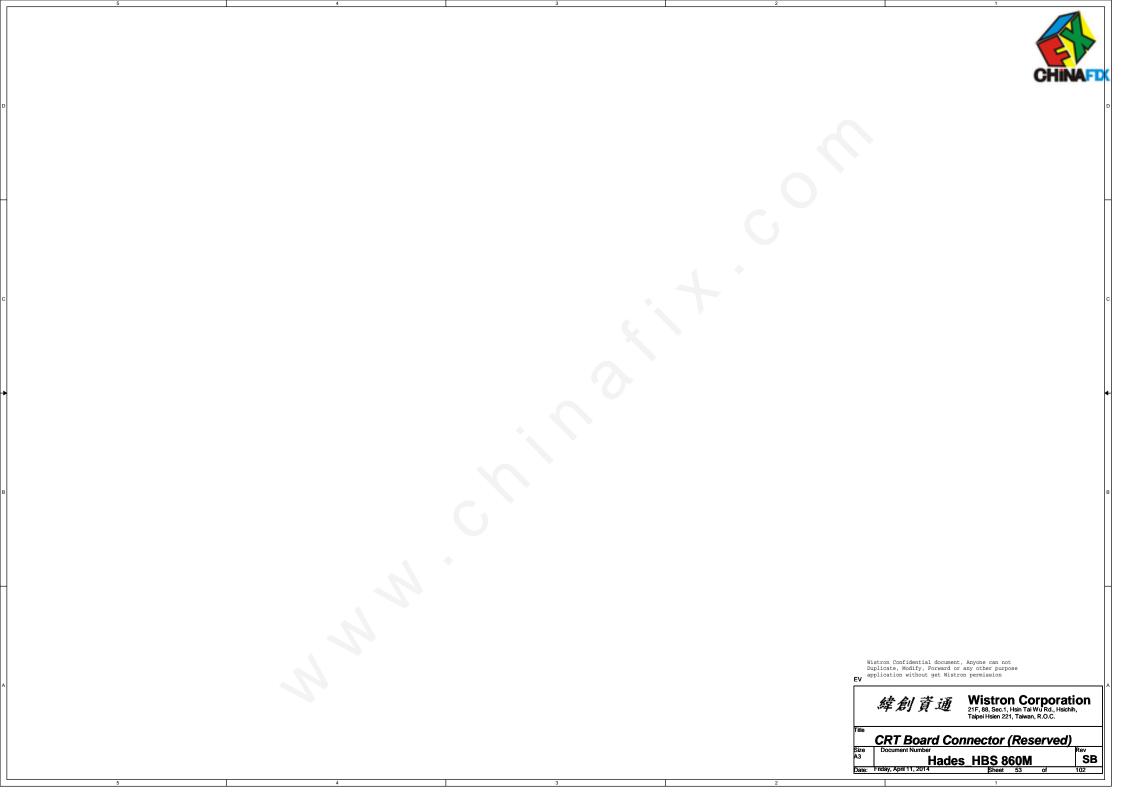




S-1339D15 for 1D5V_S0 Enable=1.0V Disable=0.25V 3D3V_S5 3D3V_PVDD_PWR_1D5V GAP-CLOSE-PWR PC5104 PC5104 SC1U10V2KX-L1-GP 1D5V PWR 1D5V S0 Iomax=360mA PU5103 PG5103 36,48,49 1D05V_S0_PWRGD >>> VIN VOUT VSS PWR 1D5V S0 EN GAP-CLOSE-PWR 17,24,36,48 PM SLP S3# ON/OFF NC#4 1D5V_PWR_EN PC5106 SC1U10V2KX-L1-GP PR5107 100KR2J-4-GP PC5105 💯 S-1339D15-M5001-GP SC22P50V2JN-L-GP DY 74.01339.B3F 2nd = 74.09198.B7F 3D3V_S5 3D3V_S5 PR5104 47KR2J-L2-GP PR5105 DY 1KR2F-3-GP Q5101 2N7002K-2-GP 1D5V_S0 1D5V PWORK# PR5103 TAT 1D5V_PWRGD 36 84.03904.L06 2nd = 84.03904.E11 DY Q5102 84.2N702.J31 DY PMBS3904-1-GP 2ND = 84.2N702.031 PC5107 SC22P50V2JN-L-GP Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose puplication without get Wistron permission Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. 緯創資通 1D5V_S0 SYW232 Document Number Size Rev Custon Hades HBS 860M SB

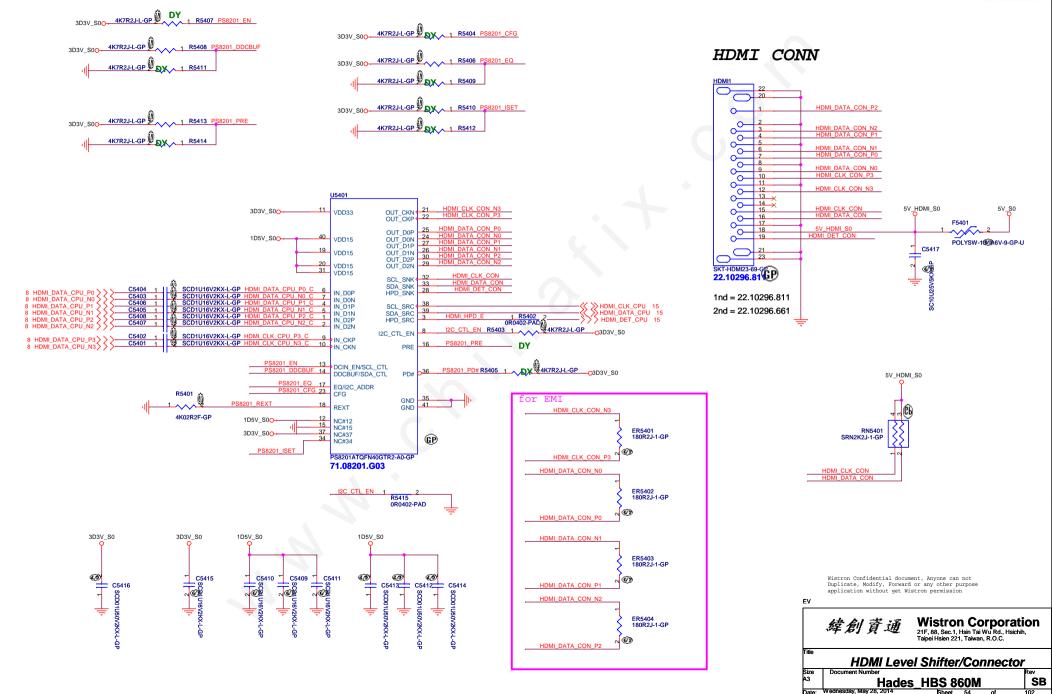


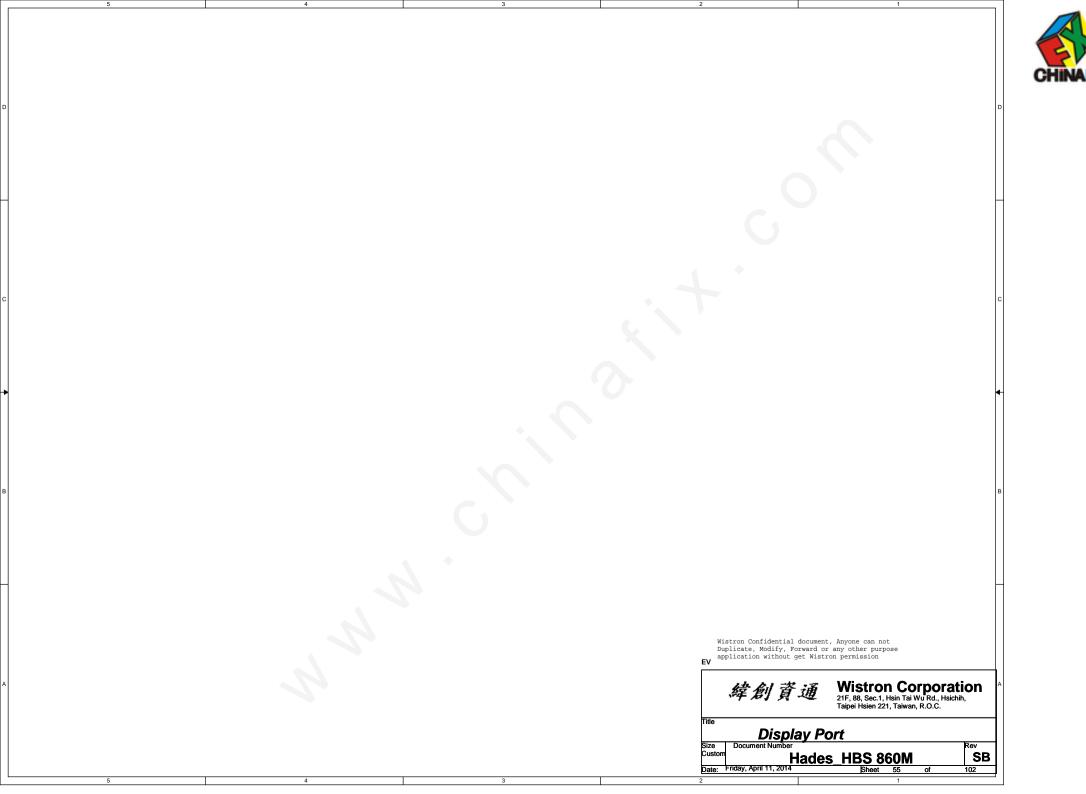




ssid = video HDMI Level Shifter & CONNECTOR



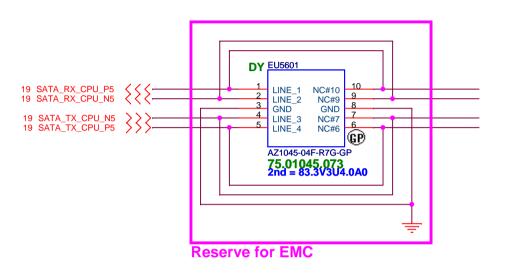


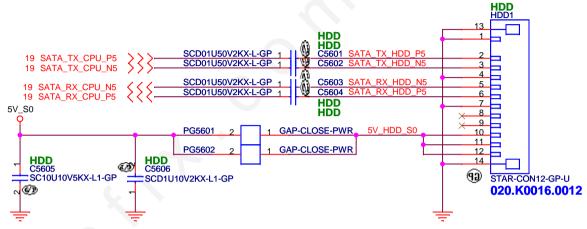


SSID = SATA



SATA HDD Connector

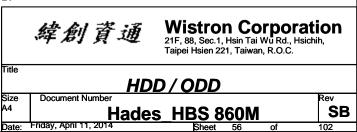


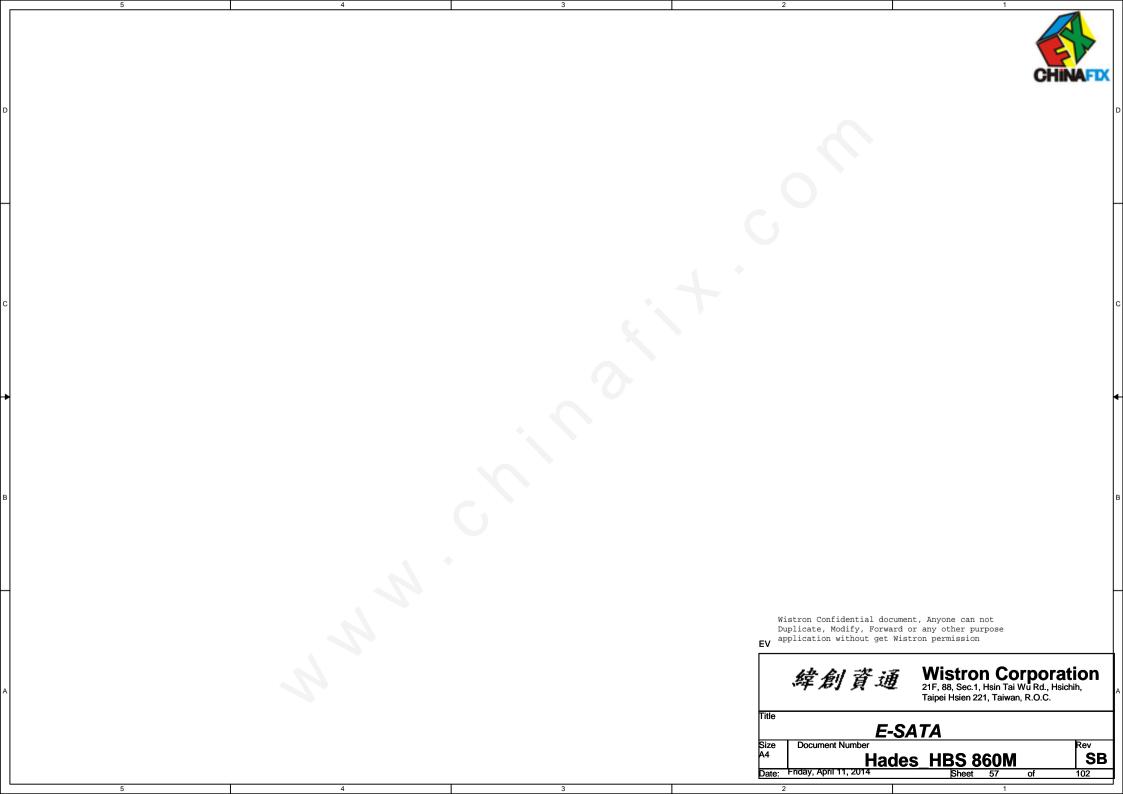


AC coupling caps near connector < 100 mils

SATA ODD Connector

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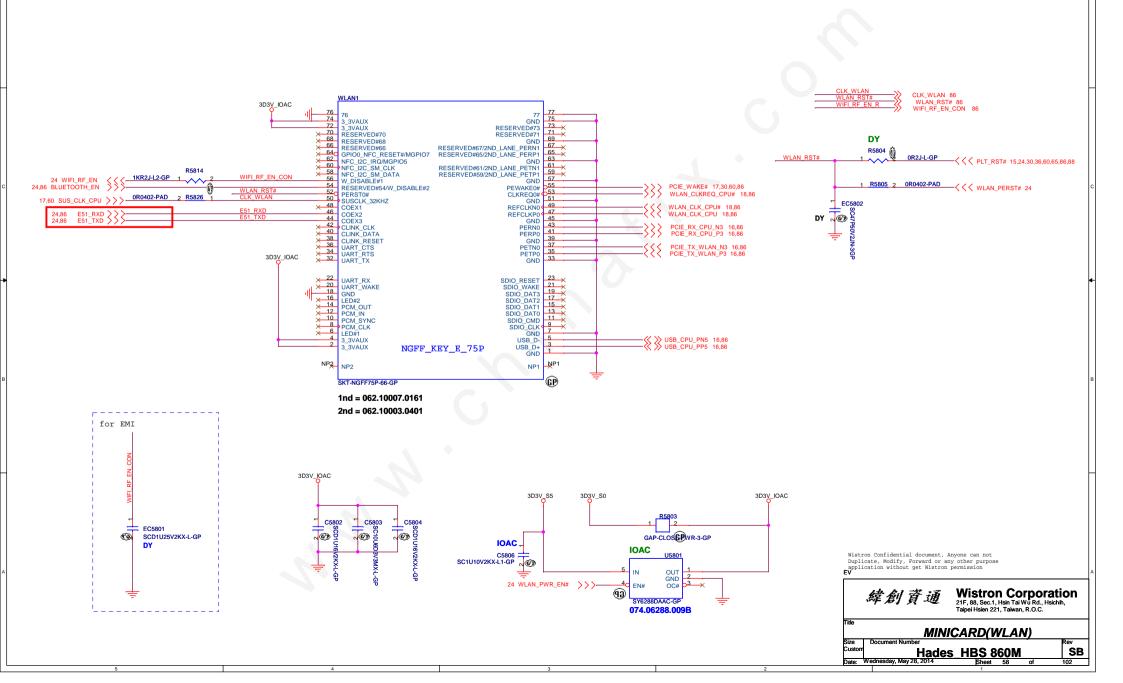




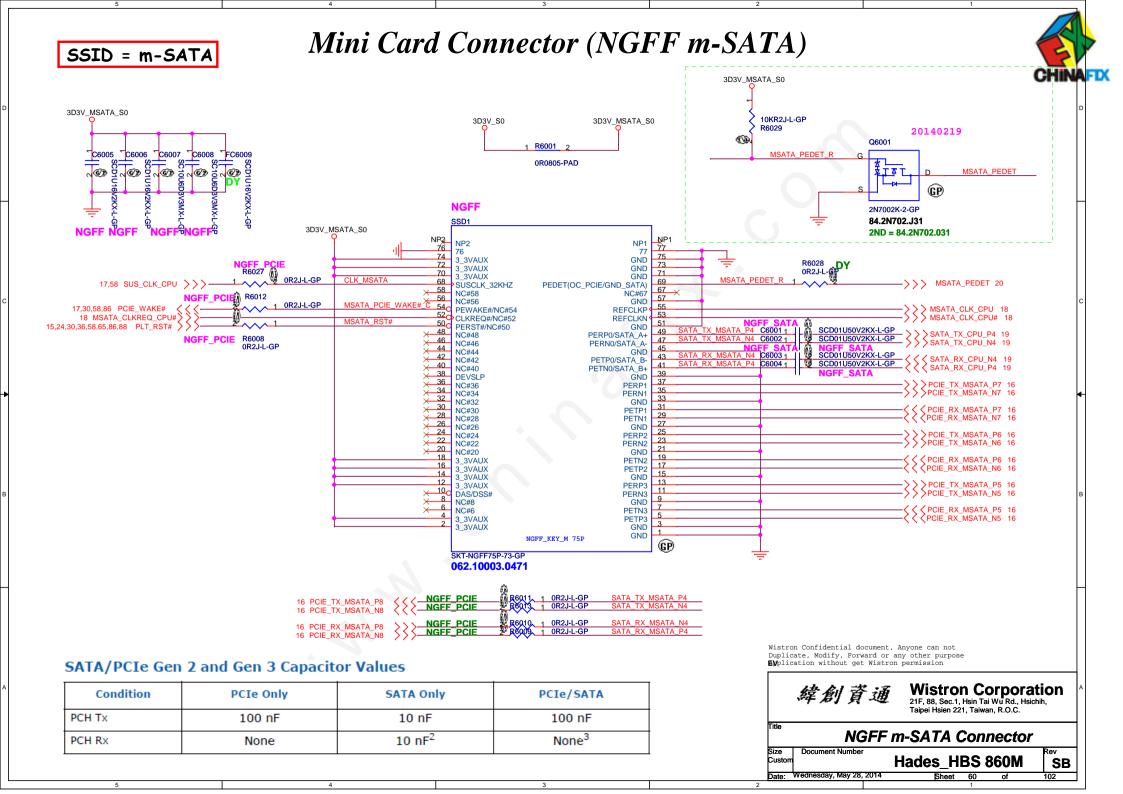
SSID = Wireless

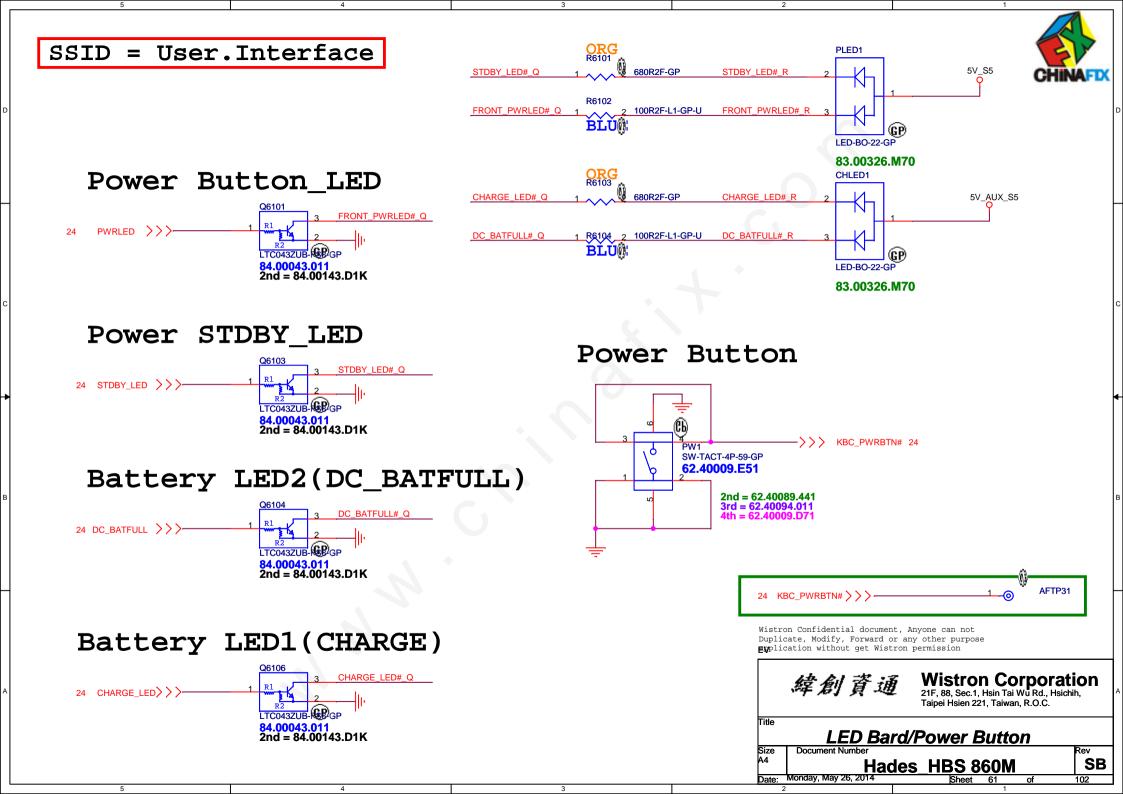
NGFF Connector (802.11a/b/g/n)

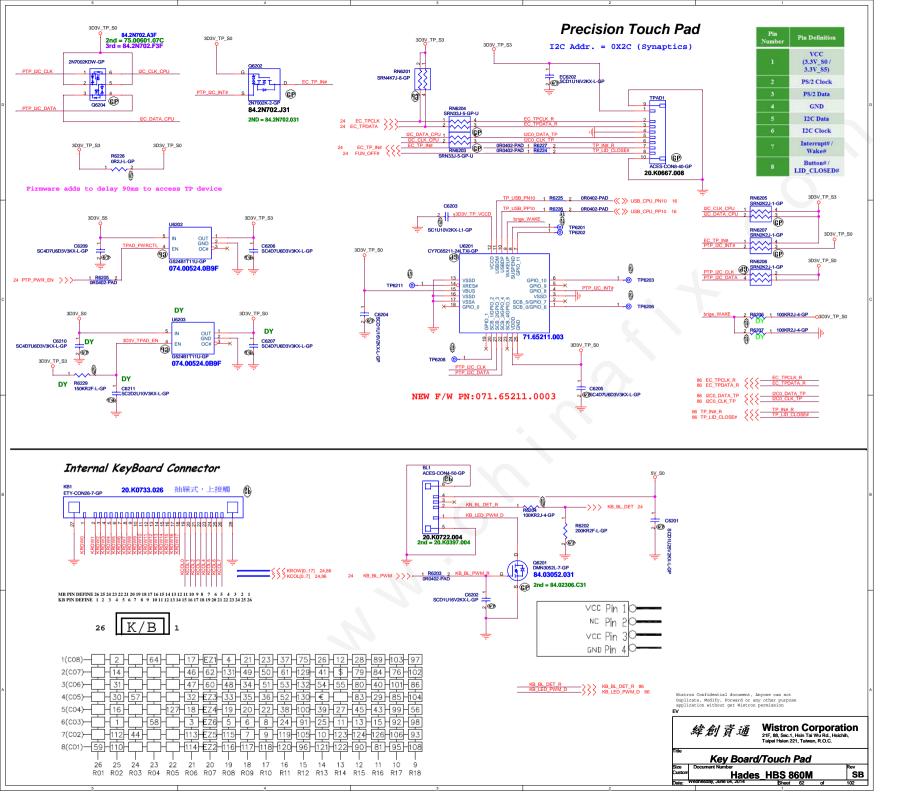




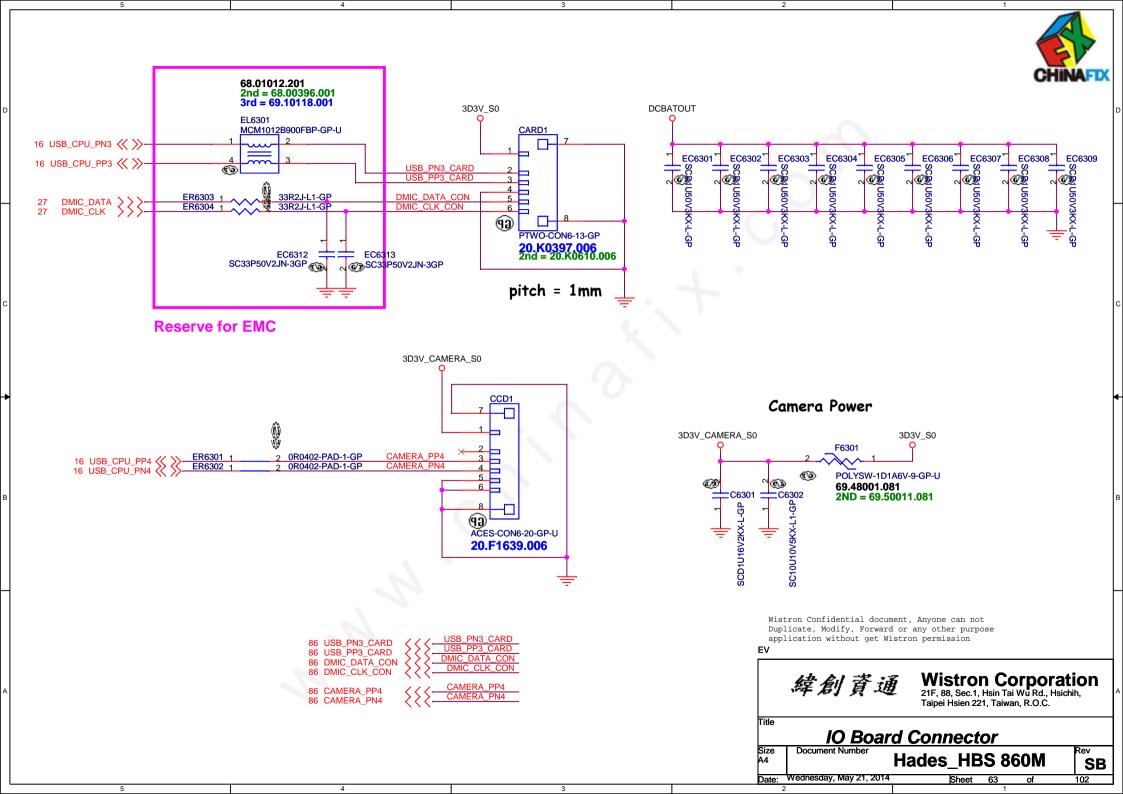
SSID = Wireless Mini Card Connector(mSATA) Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. 緯創資通 **WWAN CONN** Document Number Rev Hades HBS 860M Sheet 59 SB

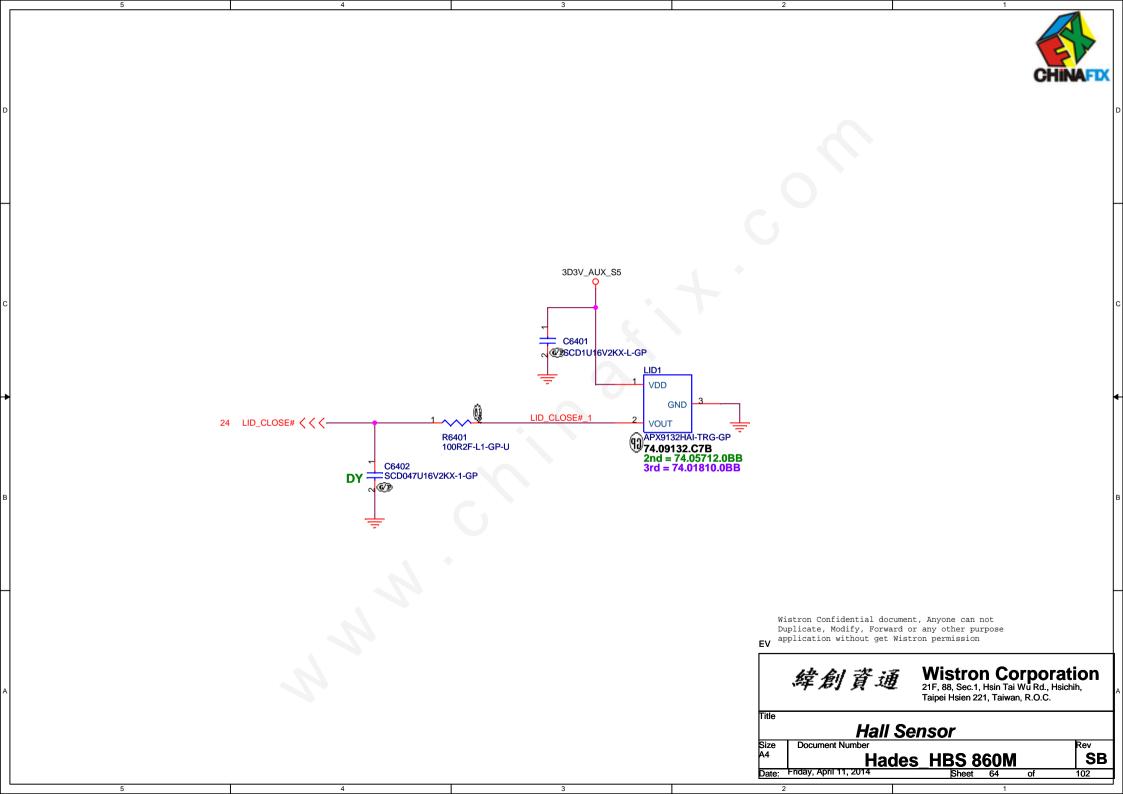


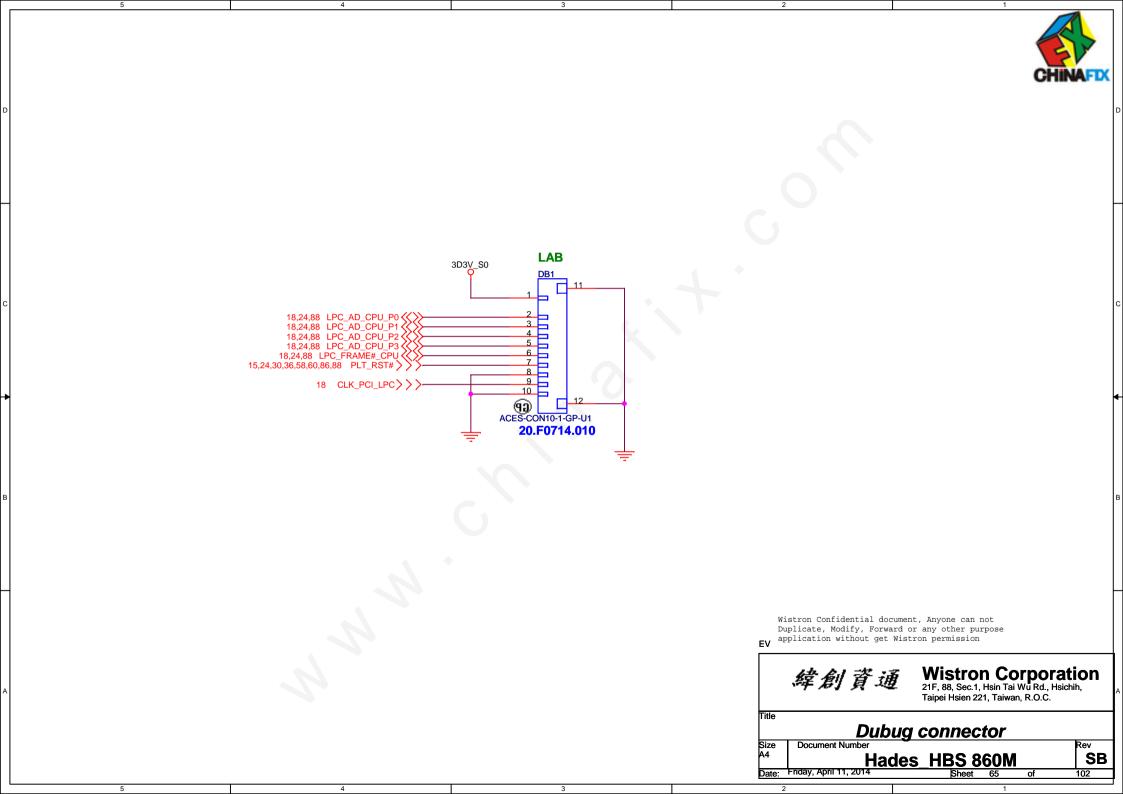








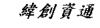






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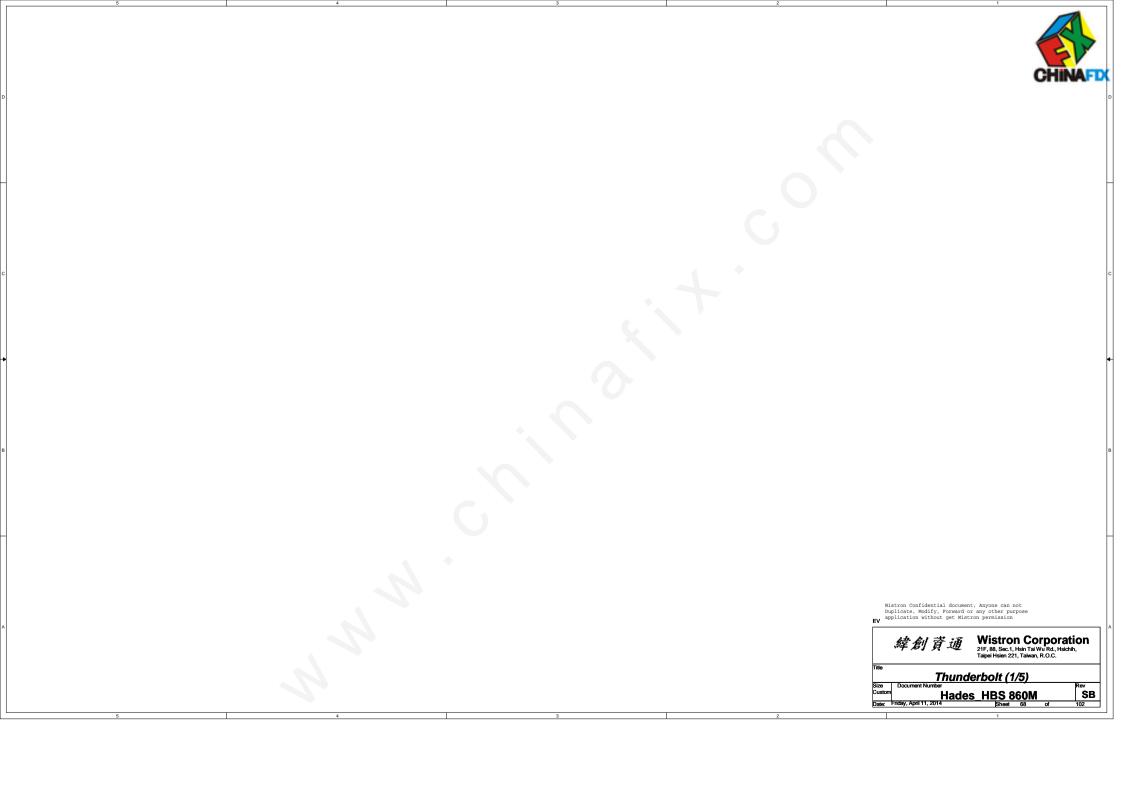
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SENSOR HUB

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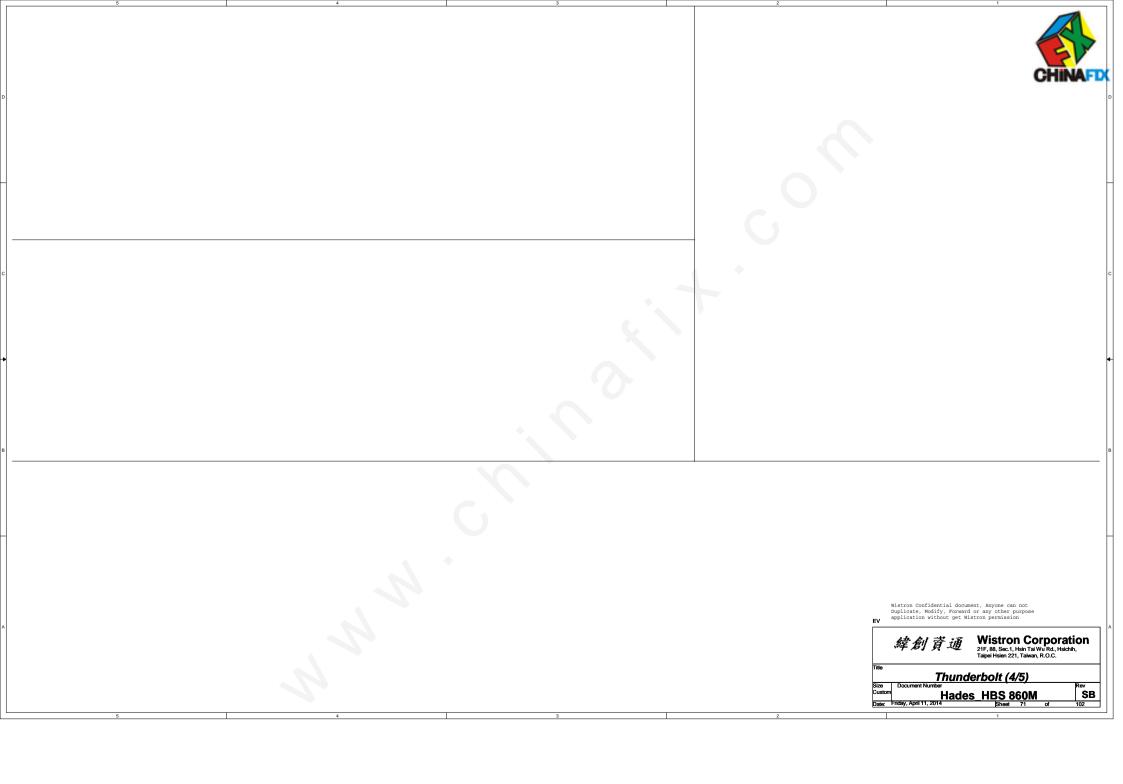
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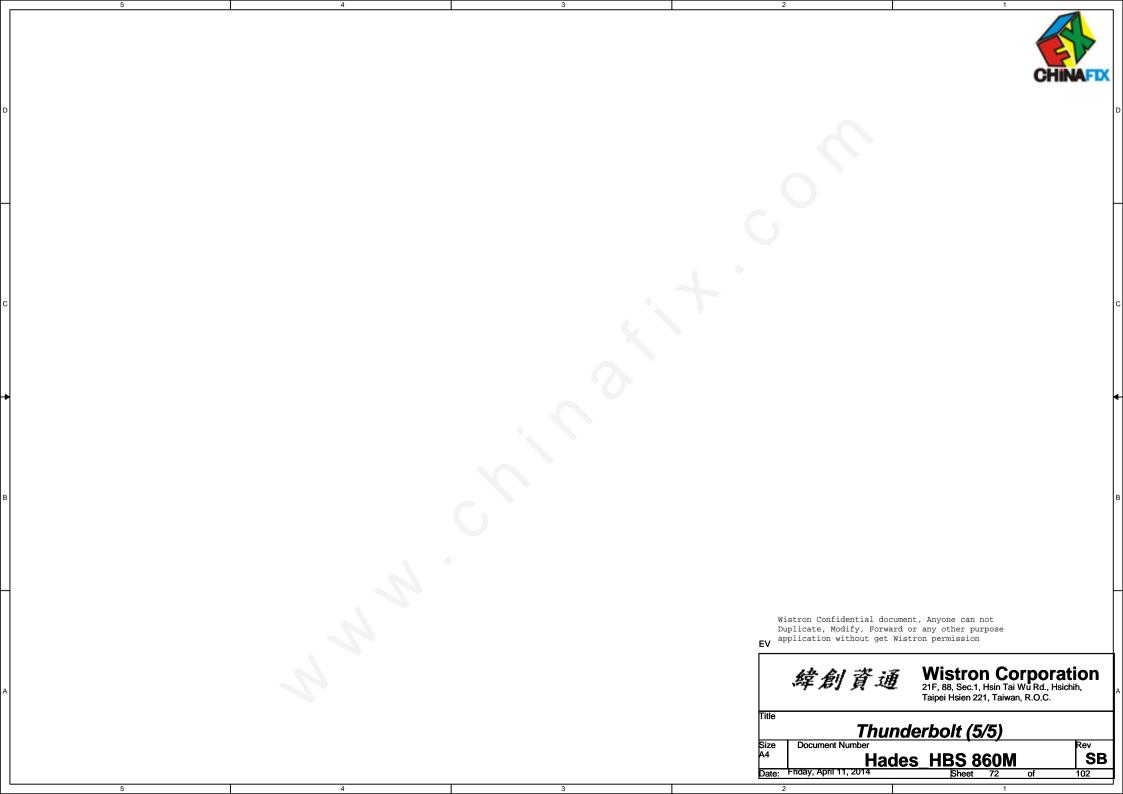
- no via, trace, under the sensor (keep out area around 2mm) Free Fall Sensor - stay away from the screw hole or metal shield soldering joints - design PCB pad based on our sensor LGA pad size (add 0.1mm) - solder stencil opening to 90% of the PCB pad size - mount the sensor near the center of mass of the NB as possible as you can Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission SDO="H"; address="3Ah" *SDO="L"; address="38h" Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, 緯創資通 Taipei Hsien 221, Taiwan, R.O.C. *CS="H"; mode="I2C" CS="L"; mode="SPI" G Sensor Document Number Rev SB Hades HBS 860M

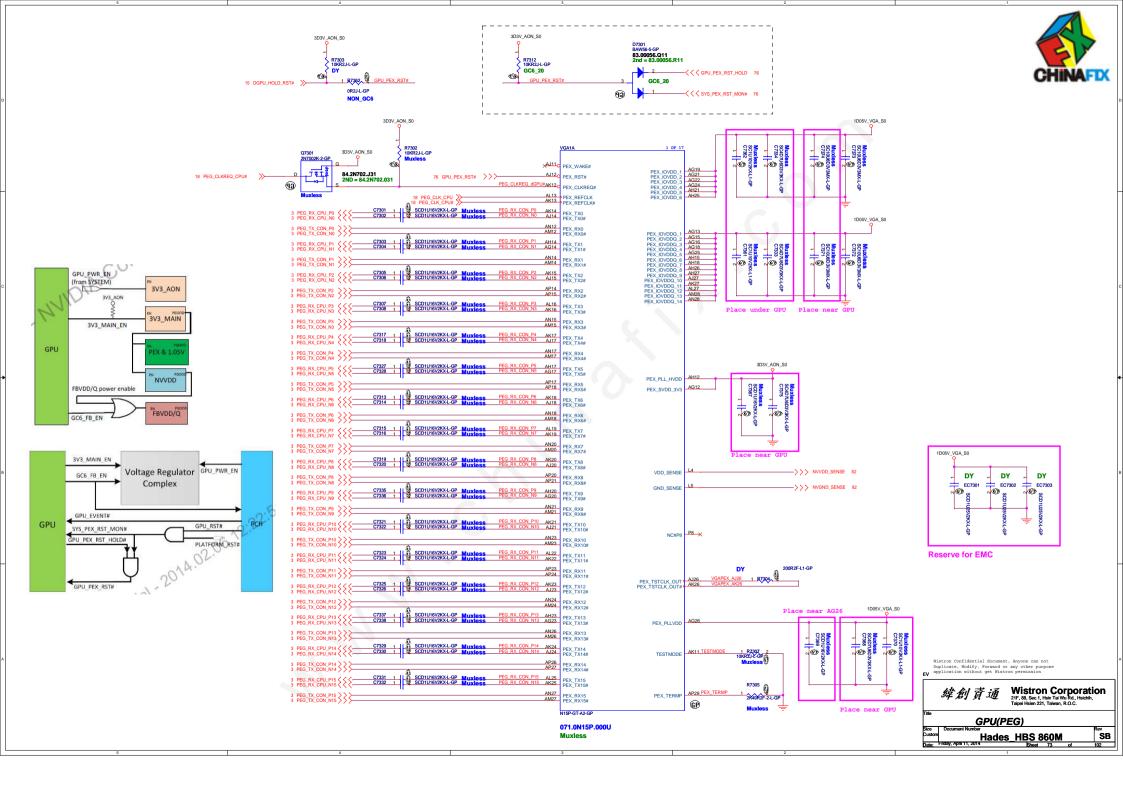


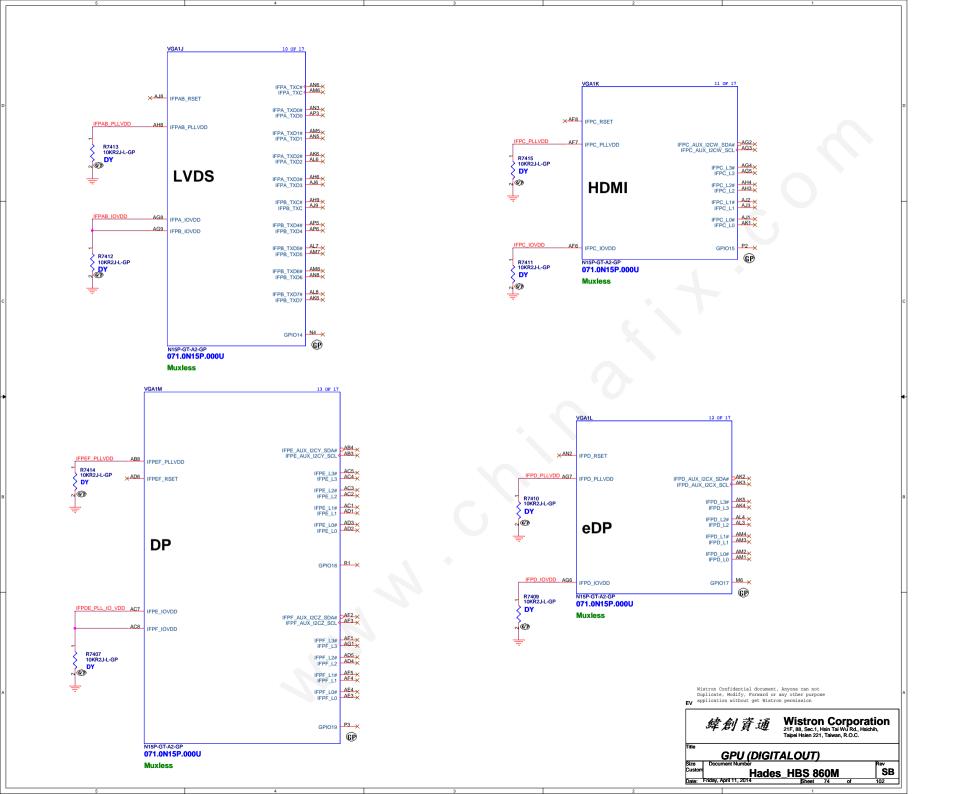




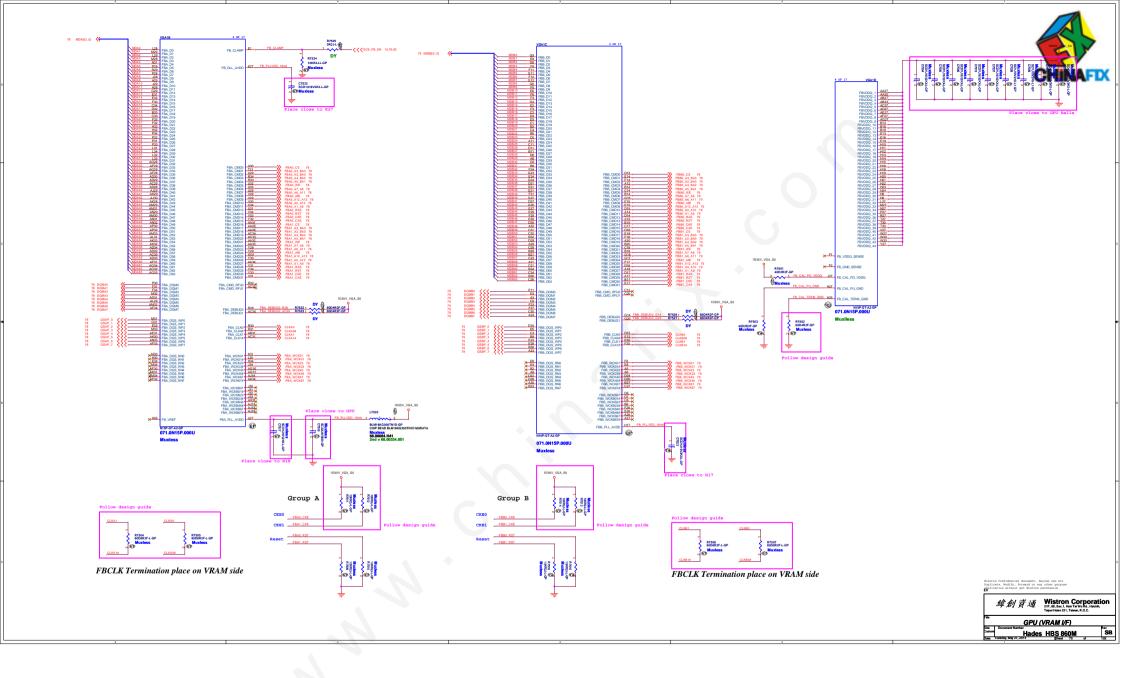


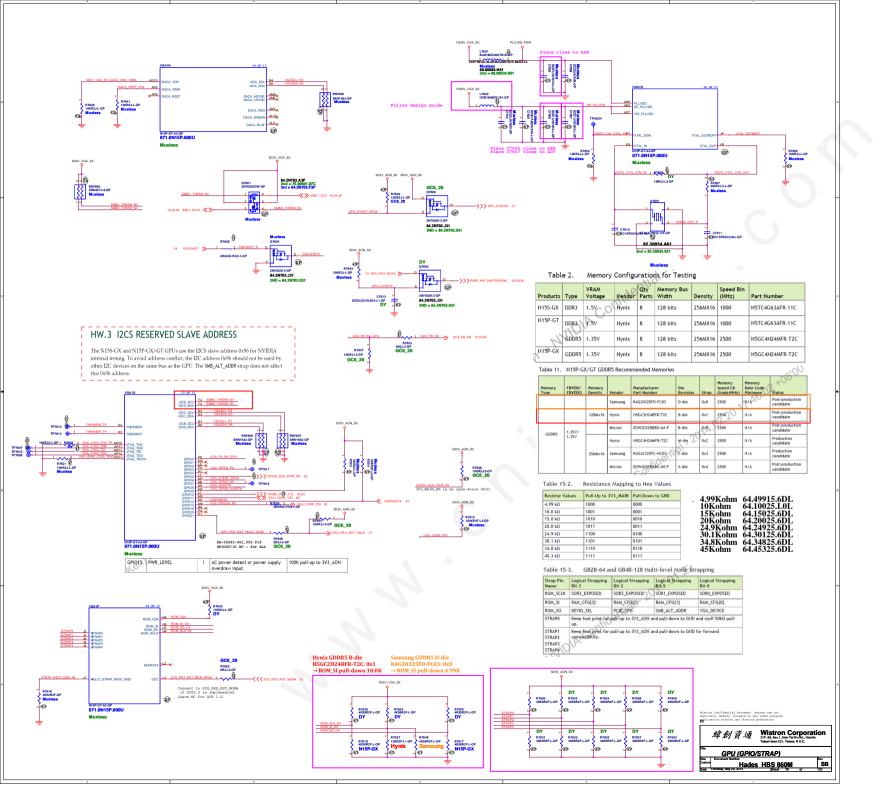




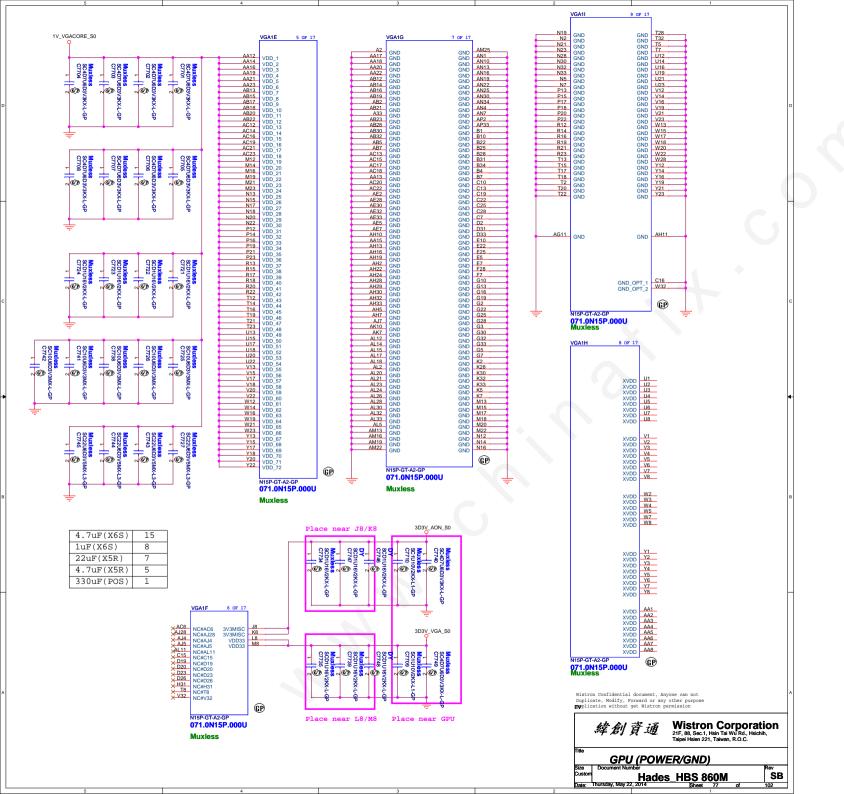










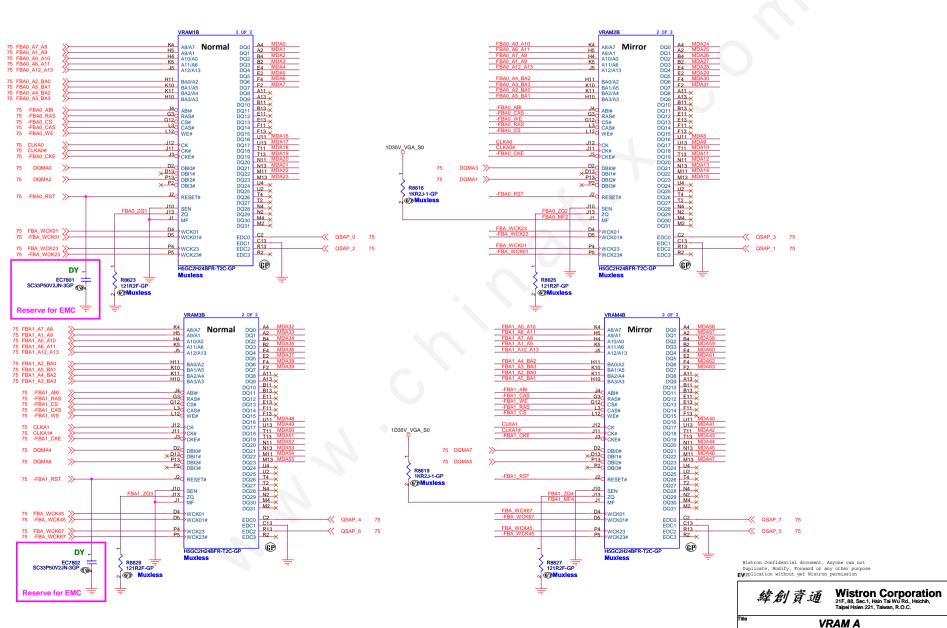




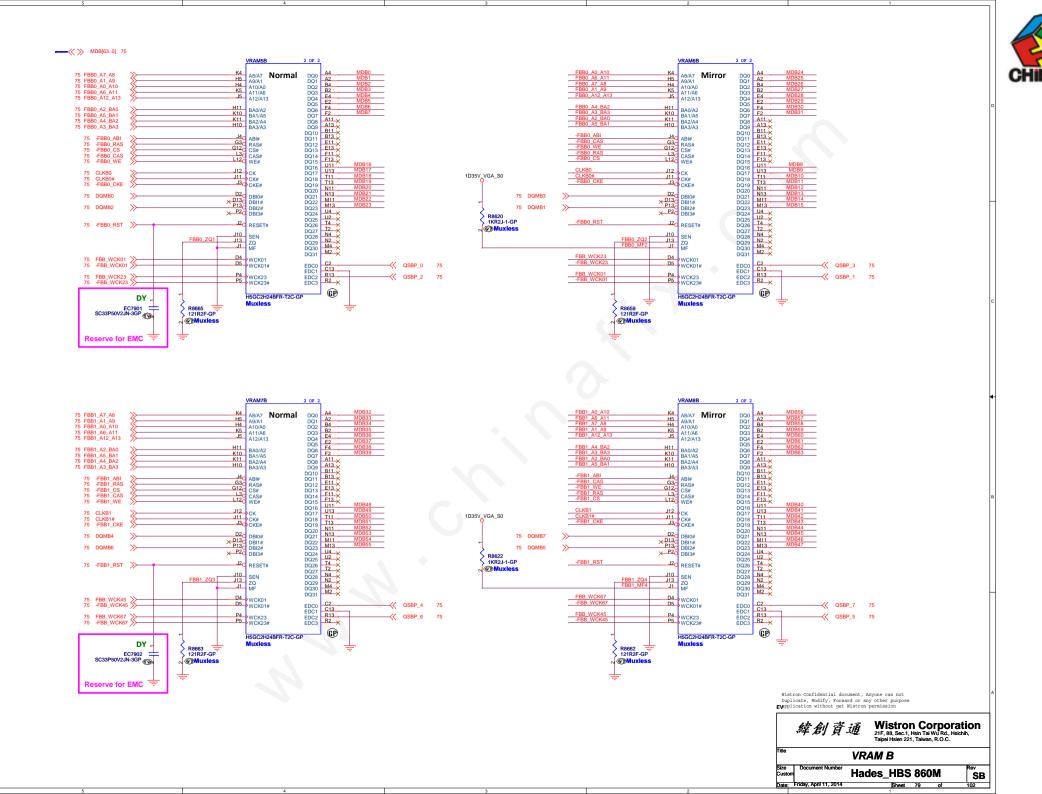
GDDR5 VIDEO MEMORY 72.05224.A0U SAMSUNG 4GBITS **HYNIX 2GBITS** SAMSUNG 2GBITS **HYNIX 4GBITS** (64Mx32) (64Mx32) (128Mx32) (128Mx32) U91 U92 U93 U94 H5GC4H24MFR K4G41325FC-HC03 H5GQ2H24AFR-T2C K4G20325FD-FC04 U95 U96 U97 U98 (tentative) (tentative) LOGIC FB CMD mapping Mode H -N15P-GX GDDR5 VRAM2B

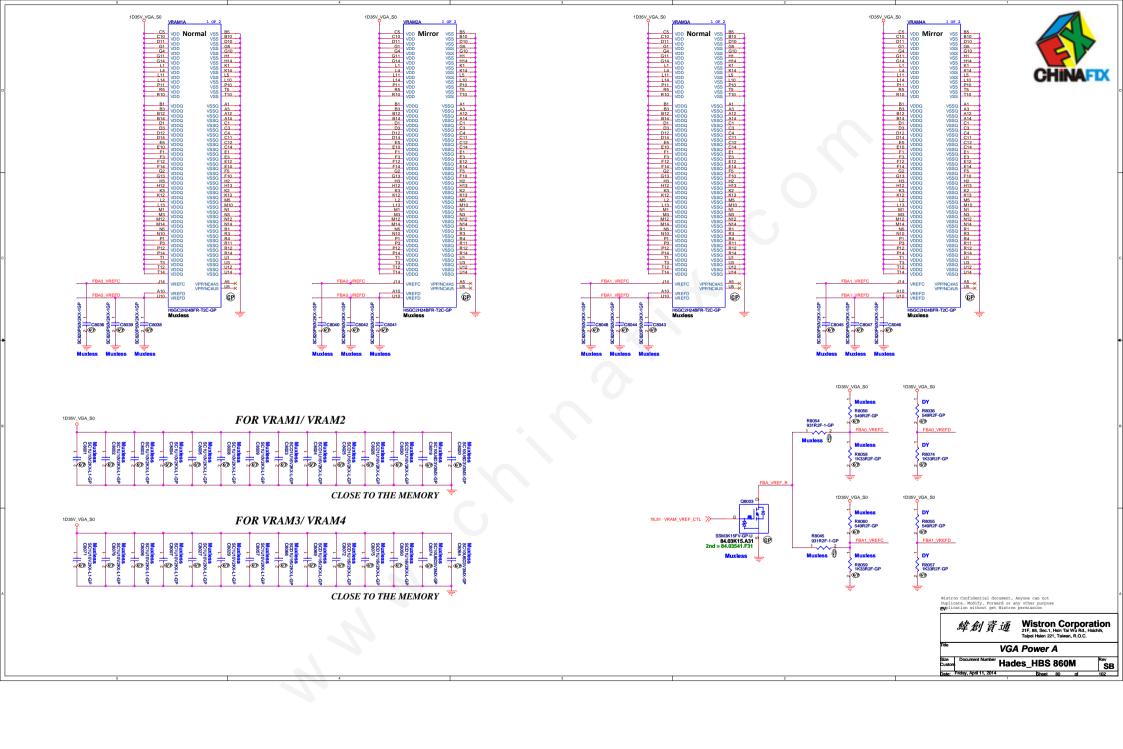
Hades_HBS 860M

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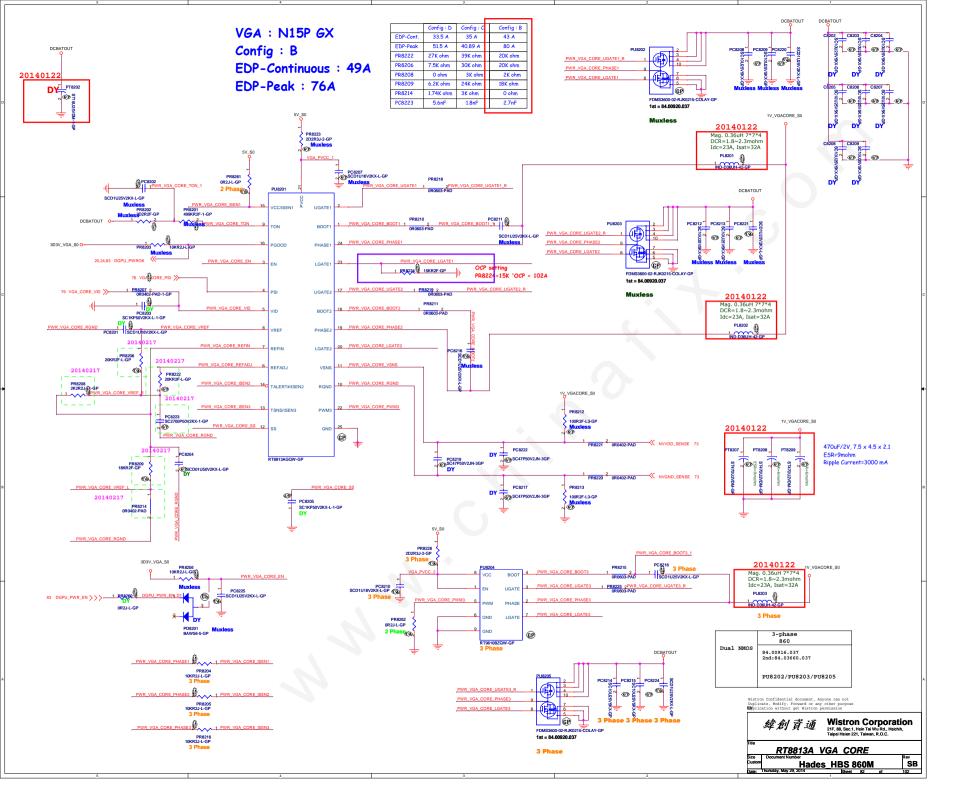


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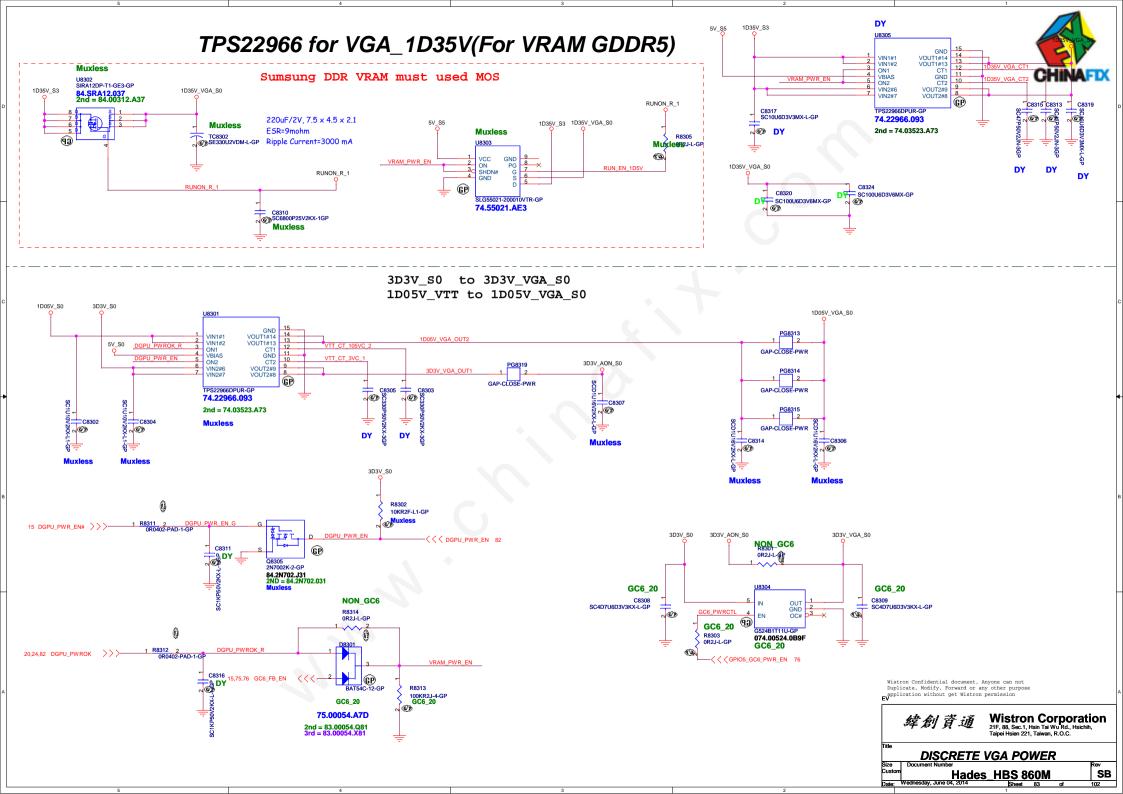


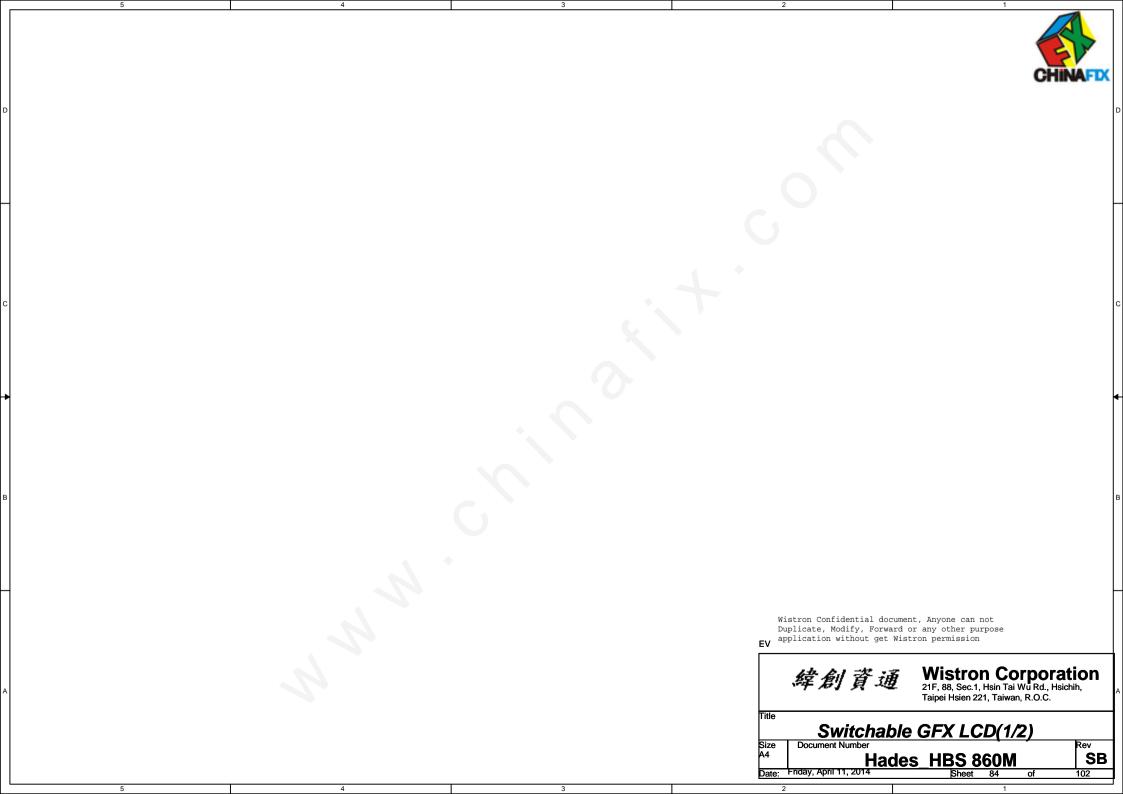


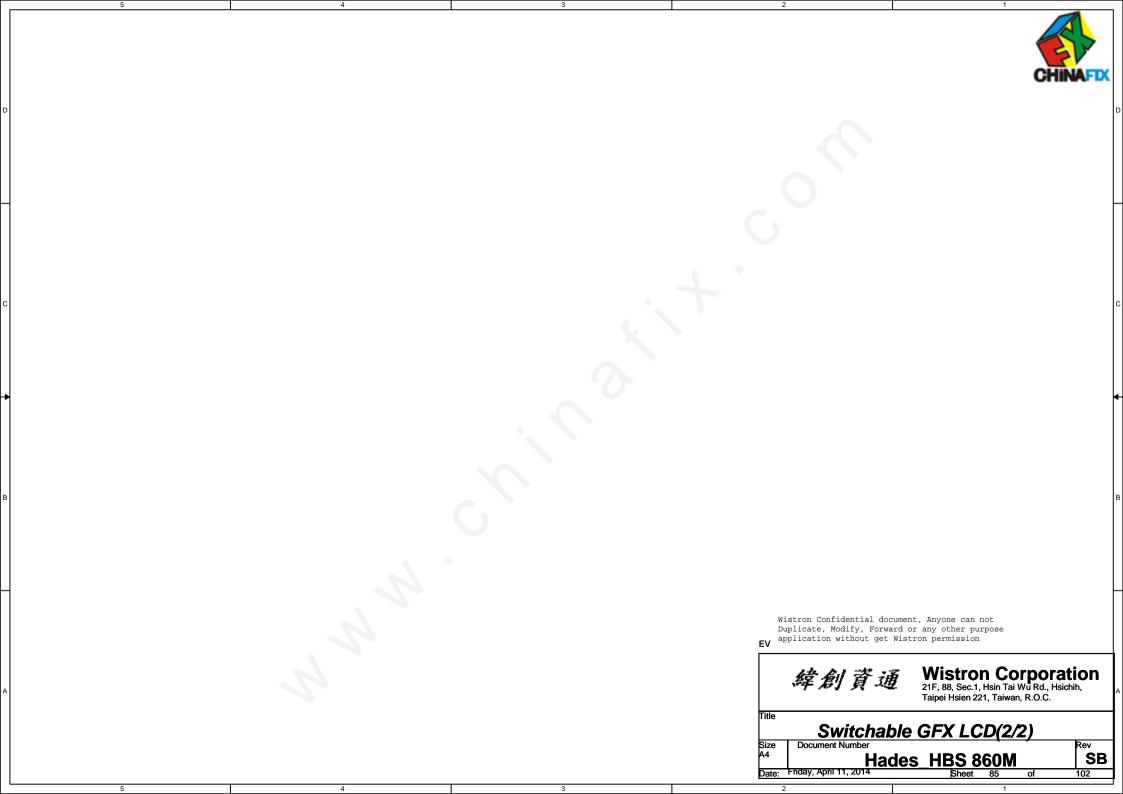


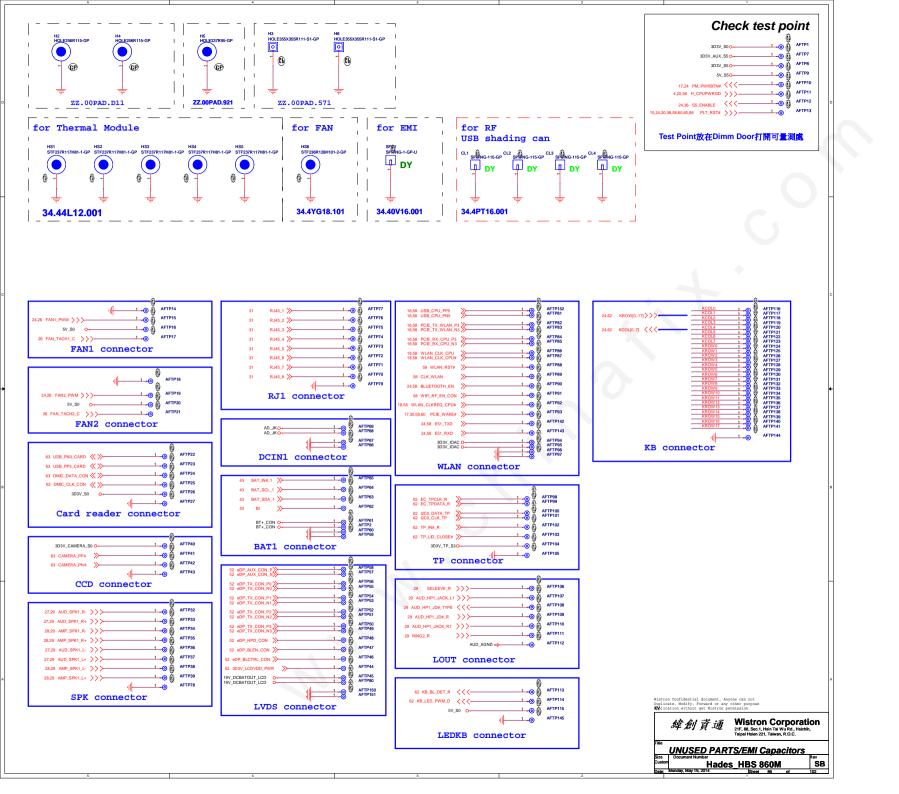






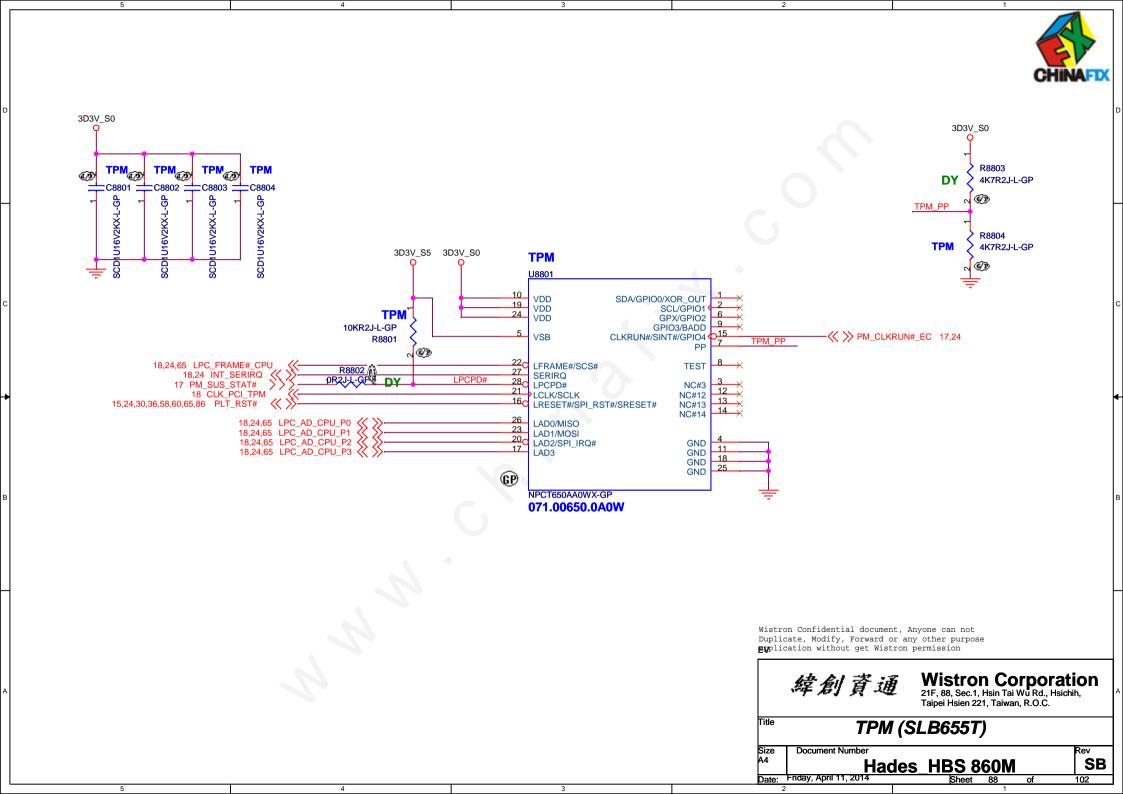


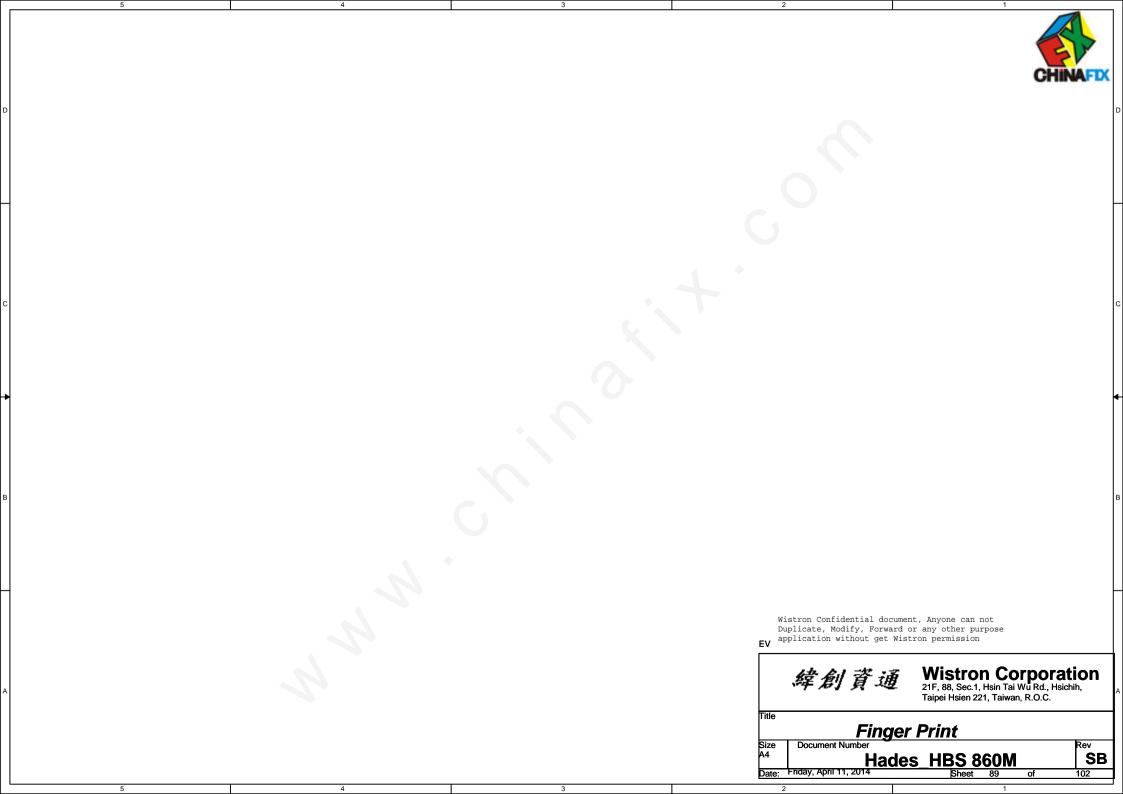


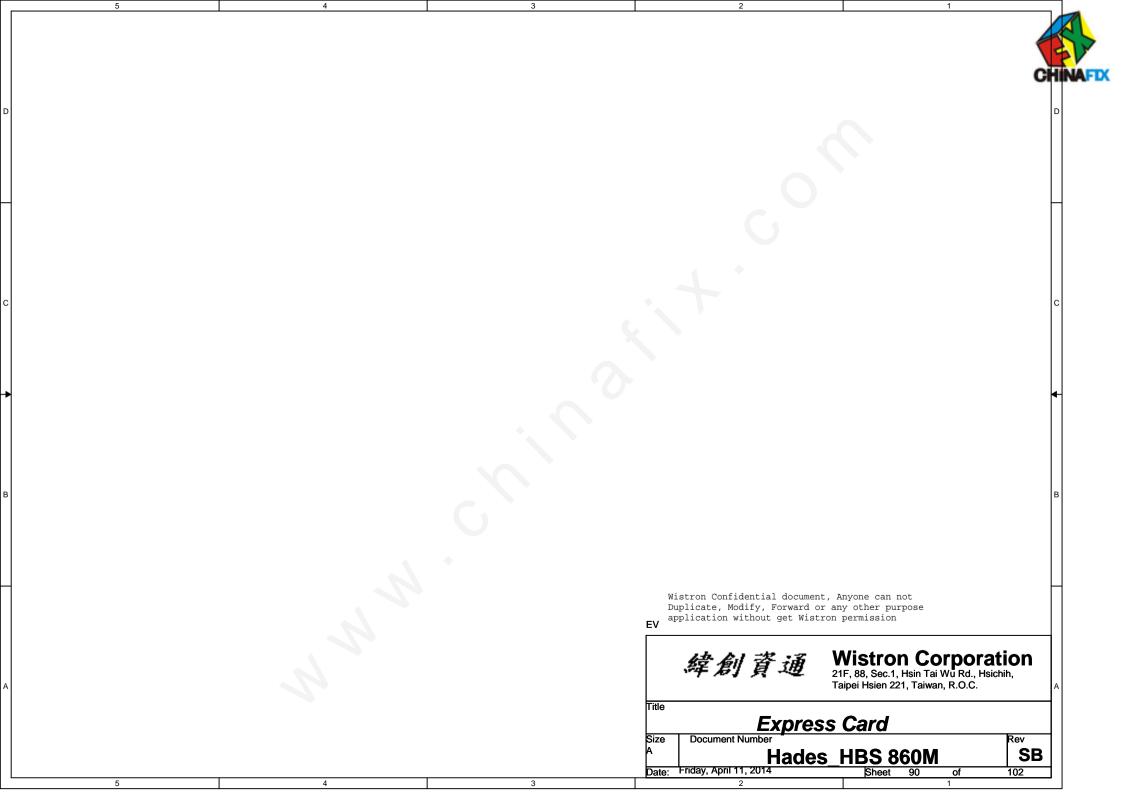


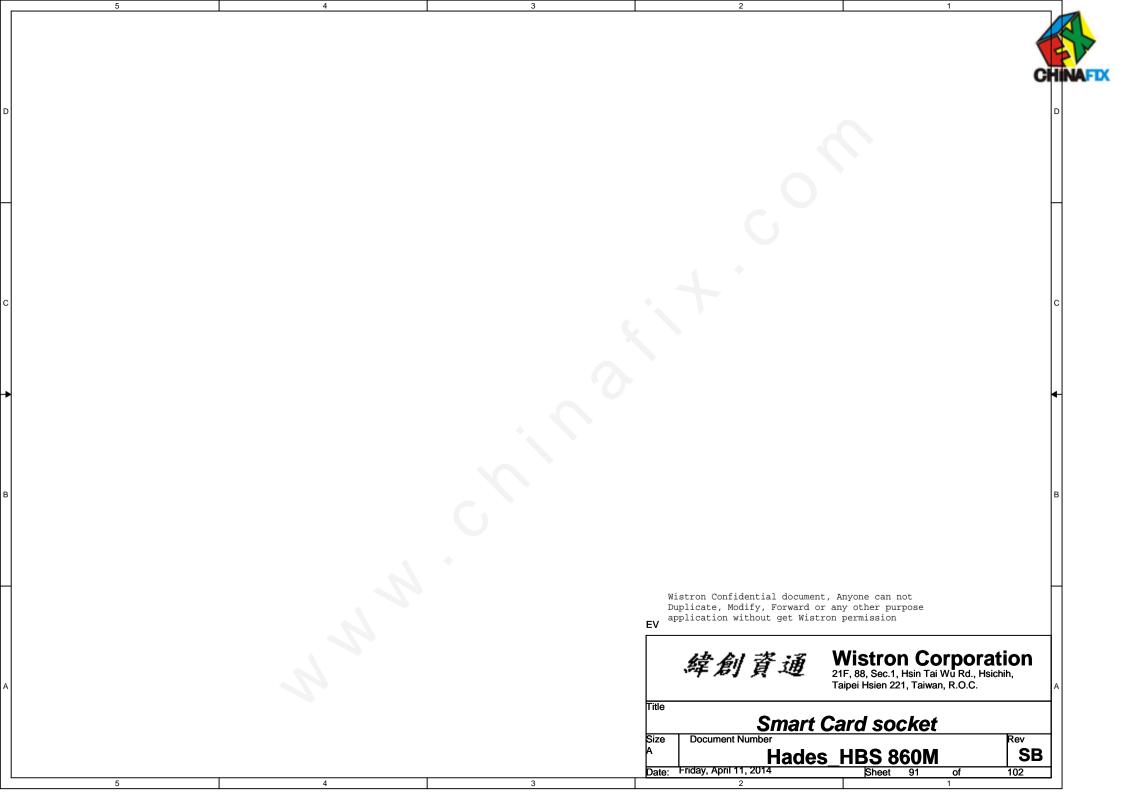


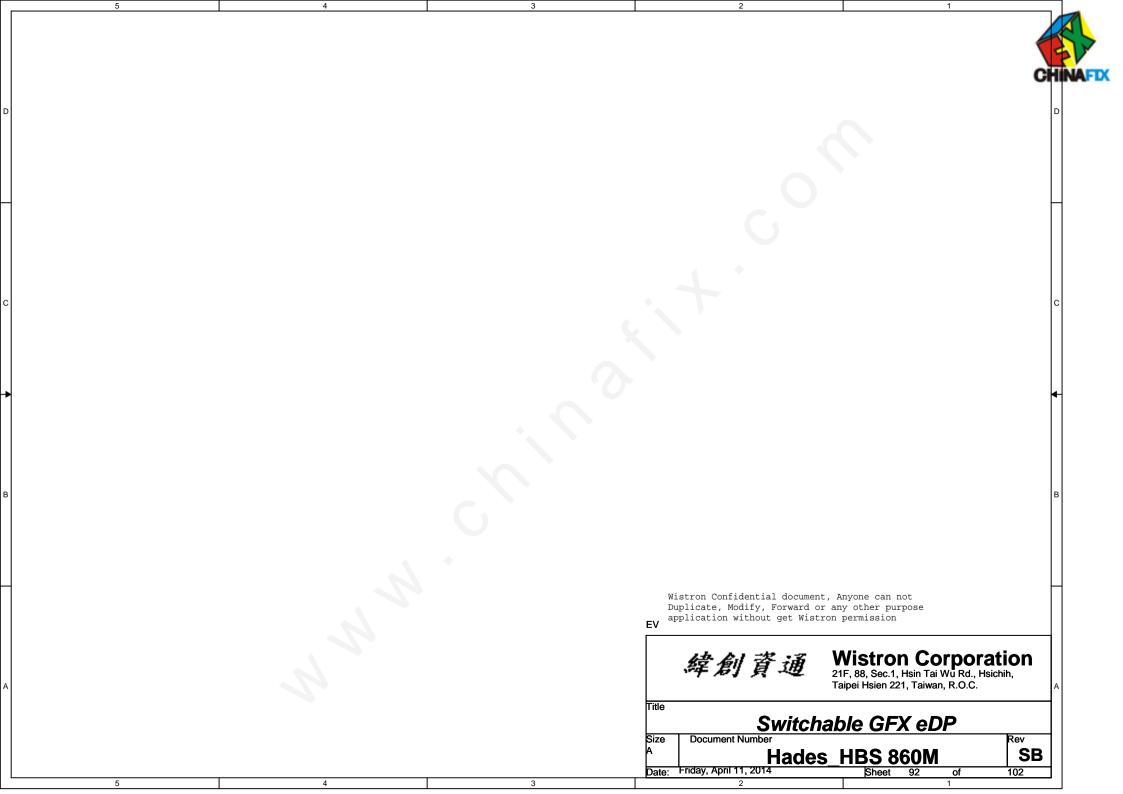
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Date: Friday, April 11, 2014 Sheet 87

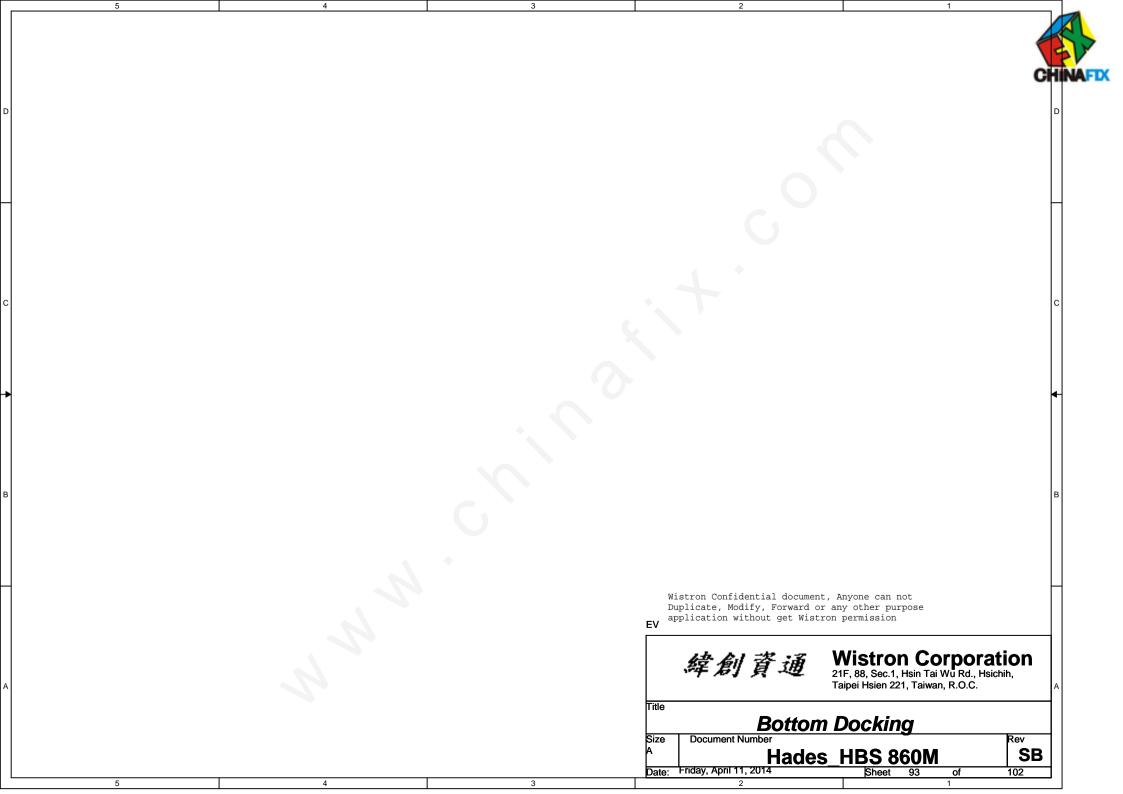


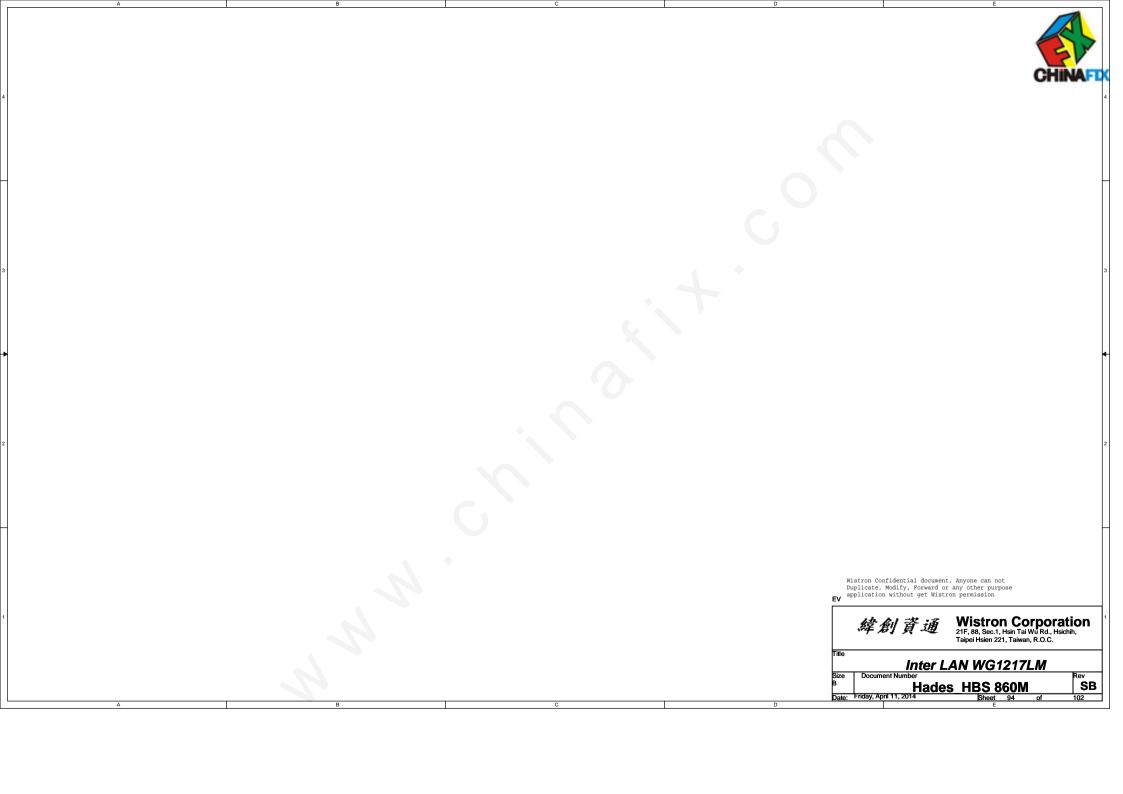


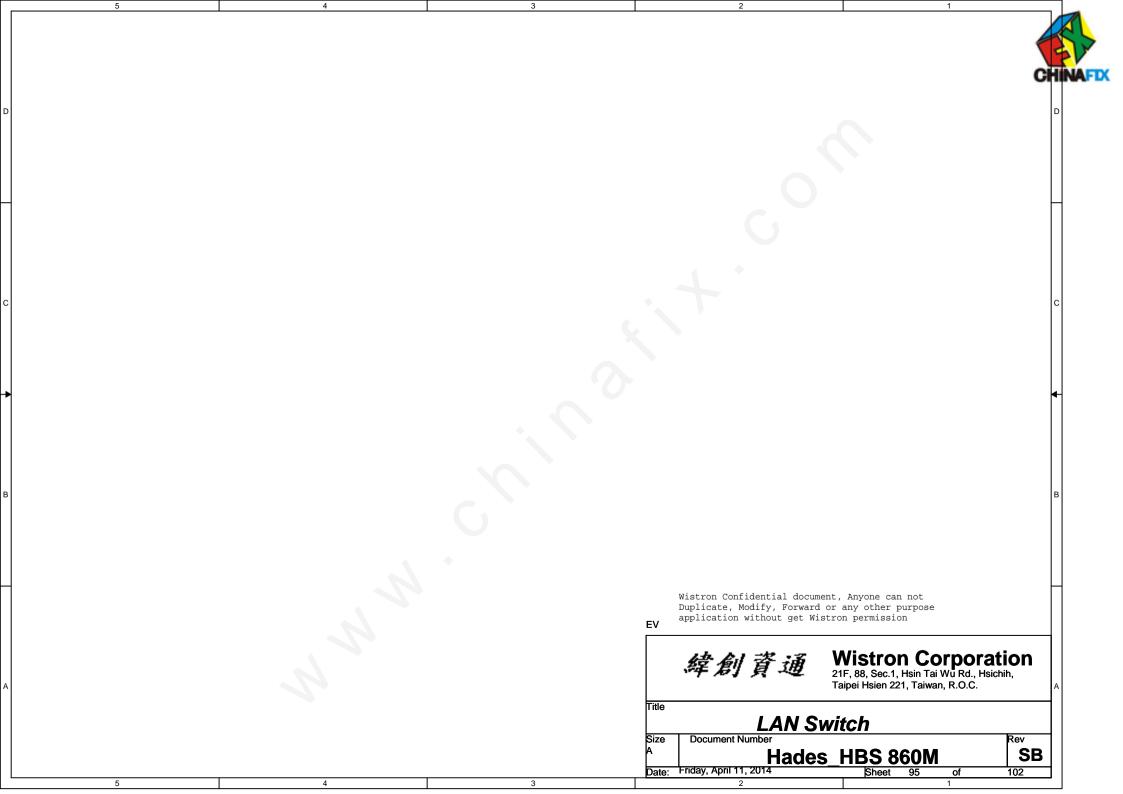














Pin	XDP Signal Name	Target Signal	1/0	Device	Pin	XDP Signal Name	Target Signal	1/0	Device
1	OBSFN_A0	Open	1/0		2	OBSFN_A1	Open	1/0	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	1/0		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	1/0		8	OBSDATA_A[3]	Open	1/0	
9	GND	GND	NA		10	HOOK01	RSMRST#	I	System
11	HOOK1	BP_PWRGD_ RST#1	0	System	12	ноок2	Open	NA	
13	ноокз	Open	NA		14	HOOK41	1.05V core	NA	1
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	1	System
17	HOOK6	RSMRST#1	0	System	18	HOOK7	DBR#1	0	System
19	GND	GND	NA		20	TDO	JTAG_TDO	1	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	0	PCH
23	TMS	JTAG_TMS	0	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	0	PCH

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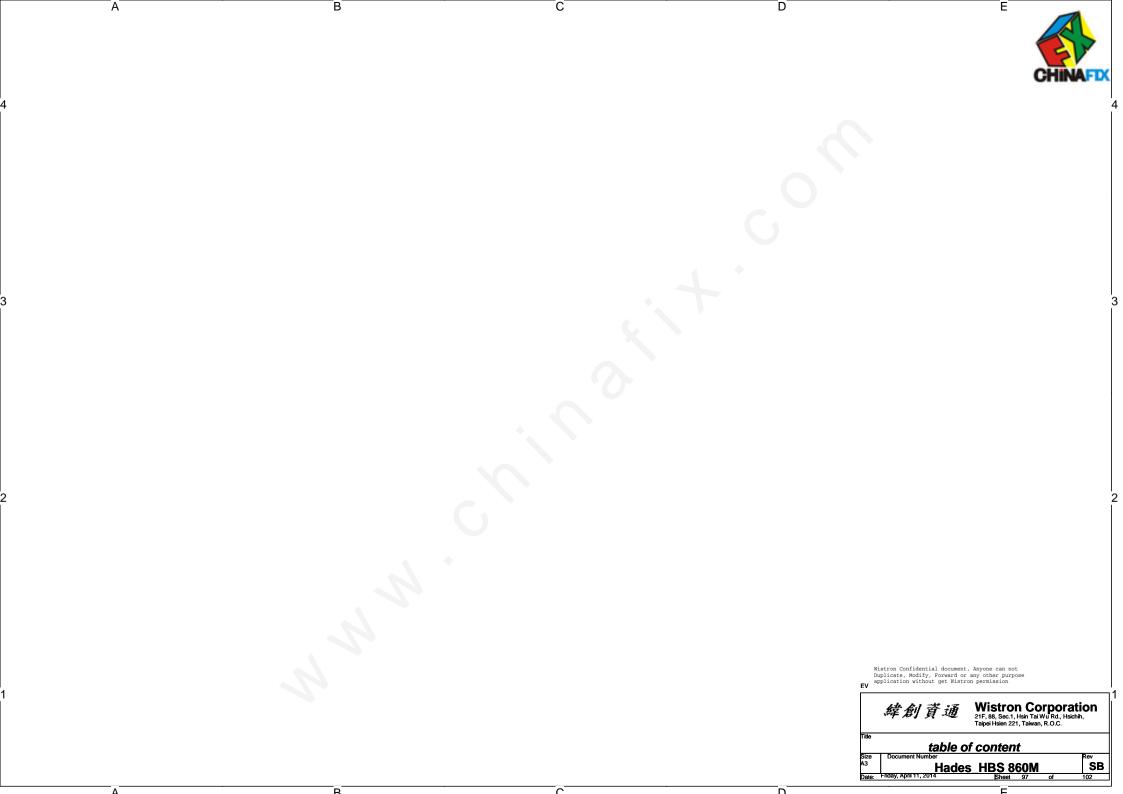
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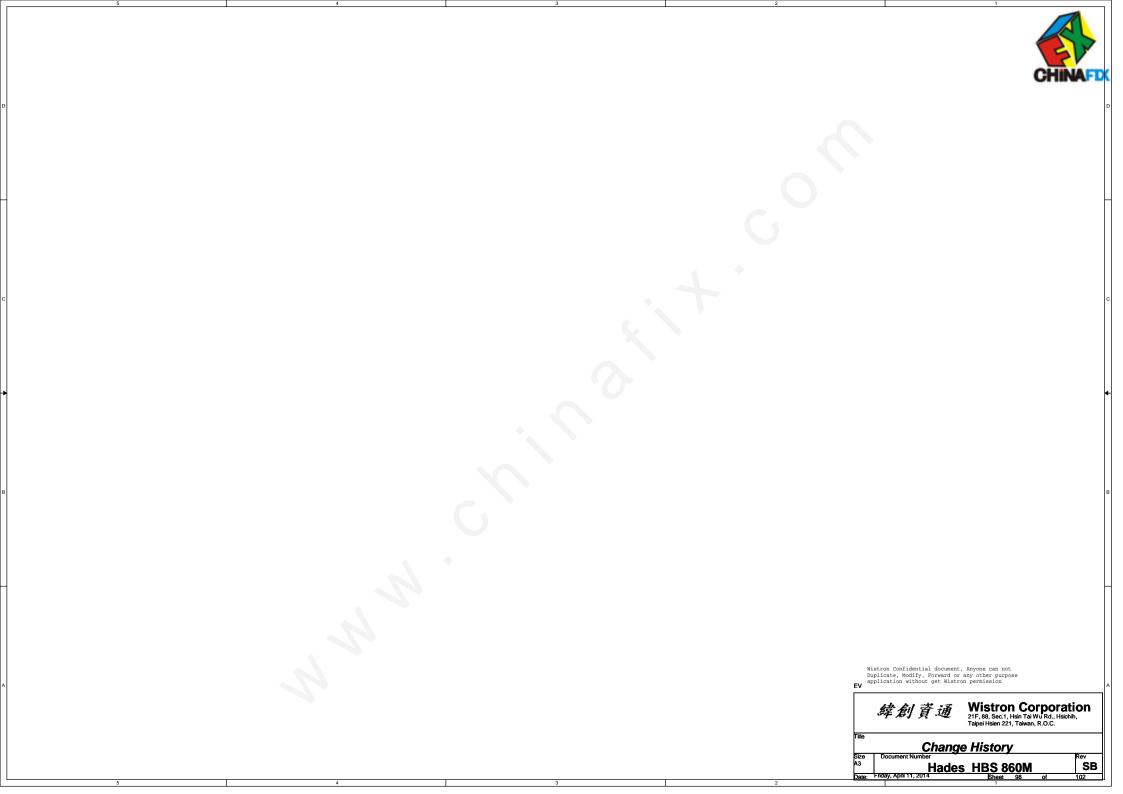
PCH_XDP

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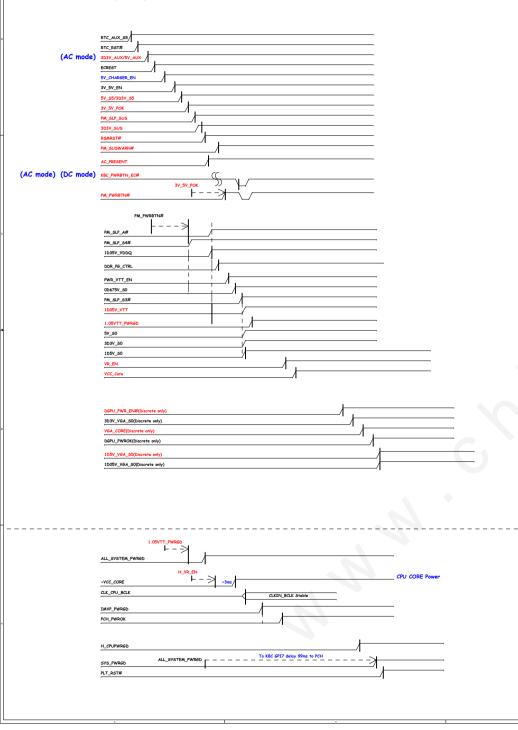
SB

Rev





Intel-Power Up Sequence



SHARK BAY POWER UP SEQUENCE DIAGRAM



