1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,D1

8/8/12

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9216	1	SCHEM,MLB,D1	SCH	CRITICAL	
820-3462	1	PCBF,MLB(NEW),D1	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Thu Aug 9 12:34:09 2012

DRAWING TITLE: SCHEM,MLB,D1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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U1000
INTEL CPU
2.X GHz
IVY BRIDGE 2C-35W
PG 9-15

DDR3-1333/1600MHZ

U3100-U3170
Mem
PG 28

U2900-U2970
Mem
PG 27

J2500
XDP CONN
PG 23

INTEL
PANTHER POINT-MPCH
U1800
PG 16-21

GPIO PG 19
FDI PG 17
DMI PG 17
RTC PG 16
CLK BUFFER PG 16
MISC PG 19
SPI PG 16
SATA PG 16
LPC PG 16
PWR CTRL PG 17
LVDS OUT
RGB OUT
DP OUT
DVI OUT
TMDS OUT
PG 17
eDP OUT PG 17
PCI PG 18
HDMI PG 17
JTAG PG 16
PEG PG 16
USB (UP TO 14 DEVICES) PG 18
USB 3 PG 18
SMBUS PG 16
PCI-E (UP TO 8 LINES) PG 16
HDA PG 16

U2600
SYSTEM CLOCK
PG 24

U4510
SATA REDRIVER
PG 36
1.05V/6GHZ.

J4500
SATA CONN HDD
PG 36

U6100
SPI Boot ROM
PG 49

J6900, J6950
DC/BATT
PG 55

POWER SUPPLY
PG 56-65

U5550,U5570
TEMP SENSOR
PG 47

U5920,U5940
Motion Sensor/GYRO
PG 48

U5340,U5350,U5360,U5370,U5400,U5410,Q5480
Q5490
POWER SENSE
PG 42, 43

J5650,J5660
FAN CONN AND CONTROL
PG 45

U4900
SMC
PG 38
I2C SMS ADC Fan Ser Prt

SPI

J5100
LPC+SPI Conn
Port80,serial
PG 40

J9400
DP/TBT PORT CONN
PG 68,69
PortA
PortB

U9420
MUX
PG 68

U9620
MUX
PG 69

U3600
TBT Host
CIO
PCIe x4
CIO
PG 32,33

DP

J9000
eDP CONN
PG 66

J4410
RIO CONN HDMI
PG 35

J4410
RIO CONN Bluetooth
PG 35

U5701
TP/KB PSOC
PG 46

J5700, J5713
TRACKPAD/ KEYBOARD
PG 46

J3502
CAMERA
PG 31

U4900
SMC
PG 38

U2700
USB HUB
PG 25

U2760
USB MUX
PG 25
EHCI
XHCI

J4410
RIO CONN USB 3
PG 35

J4600
EXTERNAL A USB 3
PG37

From PCH

J2550
PCH XDP CONN
PG 23

J4410
RIO CONN Airport/SD Card
PG 35

U6201
AUDIO Codec
PG 50
EXTMIC LINEIN HPOUT SPDIF MICIN LINEOUT

U6750
MIC BIAS
PG53

U6610,U6620
U6630,U6640
SPEAKER AMPs
PG 52

J6701
PG 53
J5815
PG 47
J6802
J6803
PG 54
AUDIO CONNs

SYNC_MASTER=MASTER
SYNC_DATE=02/15/2013

PAGE TITLE
System Block Diagram

Apple Inc.

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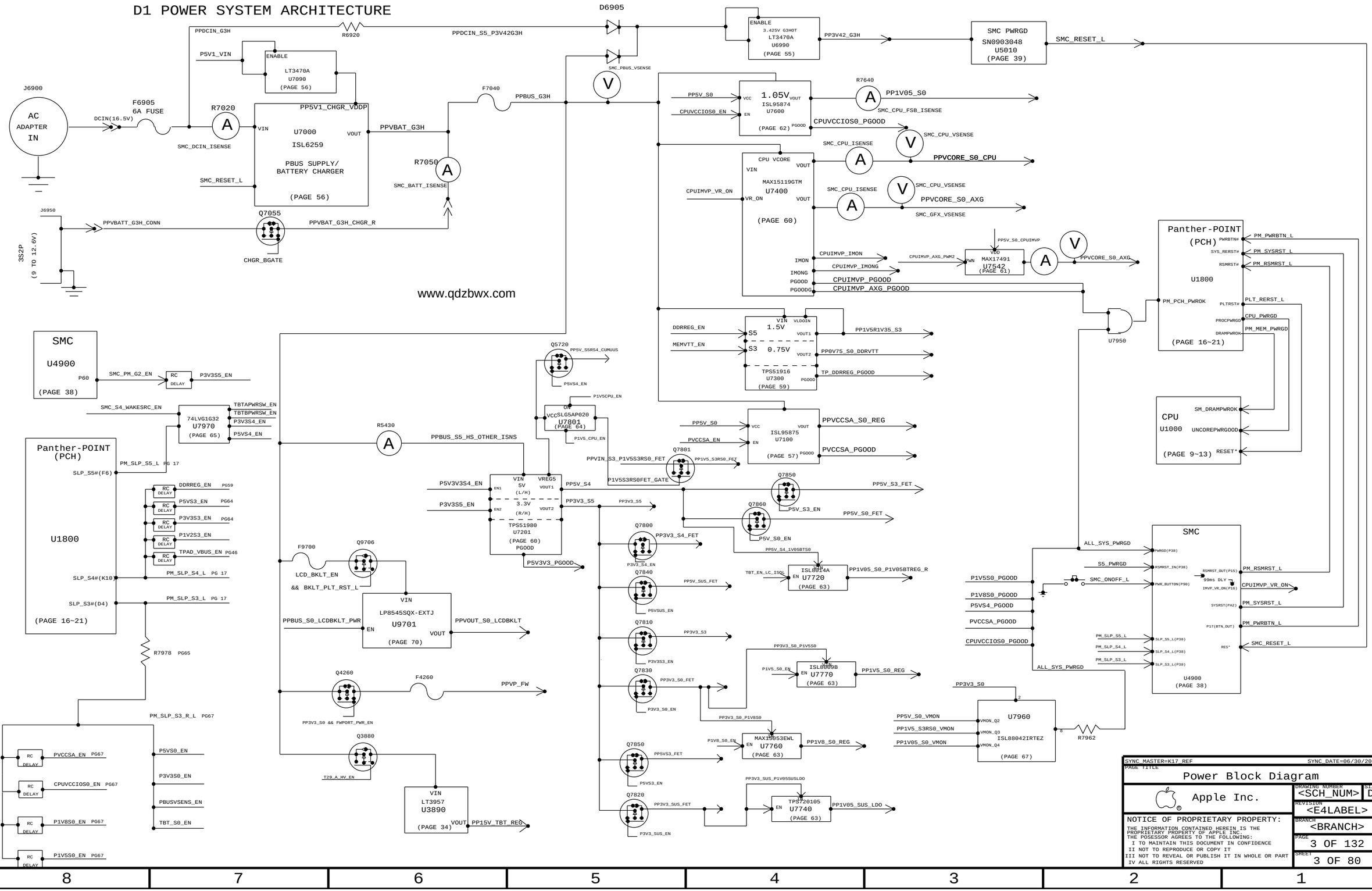
D1 POWER SYSTEM ARCHITECTURE



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PAGE TITLE: Power Block Diagram	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
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SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Revision History

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-4094	DEV BOM,MLB,D1	D1_DEVEL:PVB
607-9189	CMN PTS,PCBA,MLB,D1	D1_COMMON
639-3288	PCBA,2.5G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:DWP2,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3289	PCBA,2.9G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:DWNY,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3290	PCBA,2.5G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:DWP0,RAM_6G_HYNIX_CH0_1600_S
639-3291	PCBA,2.9G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:DWNW,RAM_6G_HYNIX_CH0_1600_S
639-3694	PCBA,2.5G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F16P,RAM_4G_SAMSUNG_35NM_1600_S
639-3695	PCBA,2.9G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F16M,RAM_4G_SAMSUNG_35NM_1600_S
639-3696	PCBA,2.9G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F16N,RAM_4G_HYNIX_1600_S
639-3697	PCBA,2.5G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F16V,RAM_4G_HYNIX_1600_S
639-3773	PCBA,2.5G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F26M,RAM_6G_ELPIDA_CH0_1600_S
639-3772	PCBA,2.9G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F26J,RAM_6G_ELPIDA_CH0_1600_S
639-3770	PCBA,2.5G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F26L,RAM_4G_ELPIDA_1600_S
639-3771	PCBA,2.9G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F26H,RAM_4G_ELPIDA_1600_S
639-3849	PCBA,2.5G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F2WT,RAM_6G_MICRON_CH0_1600_S
639-3848	PCBA,2.9G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F2WR,RAM_6G_MICRON_CH0_1600_S
639-3873	PCBA,2.6G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33H,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3874	PCBA,2.8G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33P,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3875	PCBA,2.6G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33L,RAM_6G_HYNIX_CH0_1600_S
639-3876	PCBA,2.8G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F339,RAM_6G_HYNIX_CH0_1600_S
639-3881	PCBA,2.6G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33G,RAM_4G_SAMSUNG_35NM_1600_S
639-3882	PCBA,2.8G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33C,RAM_4G_SAMSUNG_35NM_1600_S
639-3884	PCBA,2.8G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F337,RAM_4G_HYNIX_1600_S
639-3883	PCBA,2.6G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33D,RAM_4G_HYNIX_1600_S
639-3877	PCBA,2.6G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33Q,RAM_6G_ELPIDA_CH0_1600_S
639-3878	PCBA,2.8G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F338,RAM_6G_ELPIDA_CH0_1600_S
639-3885	PCBA,2.6G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33J,RAM_4G_ELPIDA_1600_S
639-3886	PCBA,2.8G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33N,RAM_4G_ELPIDA_1600_S
639-3879	PCBA,2.6G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33M,RAM_6G_MICRON_CH0_1600_S
639-3880	PCBA,2.8G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F336,RAM_6G_MICRON_CH0_1600_S
639-3846	PCBA,2.5G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F2WV,RAM_4G_MICRON_1600_S
639-3847	PCBA,2.9G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F2WQ,RAM_4G_MICRON_1600_S
639-3887	PCBA,2.6G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33K,RAM_4G_MICRON_1600_S
639-3888	PCBA,2.8G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33F,RAM_4G_MICRON_1600_S

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DV7Q]	CRITICAL	EEEE:DV7Q
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWNY]	CRITICAL	EEEE:DWNY
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWNW]	CRITICAL	EEEE:DWNW
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWP0]	CRITICAL	EEEE:DWP0
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWP2]	CRITICAL	EEEE:DWP2
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16M]	CRITICAL	EEEE:F16M
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16N]	CRITICAL	EEEE:F16N
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16P]	CRITICAL	EEEE:F16P
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16V]	CRITICAL	EEEE:F16V
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26H]	CRITICAL	EEEE:F26H
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26J]	CRITICAL	EEEE:F26J
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26L]	CRITICAL	EEEE:F26L
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26M]	CRITICAL	EEEE:F26M
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WQ]	CRITICAL	EEEE:F2WQ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WR]	CRITICAL	EEEE:F2WR
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WT]	CRITICAL	EEEE:F2WT
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WV]	CRITICAL	EEEE:F2WV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F336]	CRITICAL	EEEE:F336
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F337]	CRITICAL	EEEE:F337
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F338]	CRITICAL	EEEE:F338
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F339]	CRITICAL	EEEE:F339
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33C]	CRITICAL	EEEE:F33C
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33D]	CRITICAL	EEEE:F33D
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33F]	CRITICAL	EEEE:F33F
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33G]	CRITICAL	EEEE:F33G
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33H]	CRITICAL	EEEE:F33H
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33J]	CRITICAL	EEEE:F33J
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33K]	CRITICAL	EEEE:F33K
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33L]	CRITICAL	EEEE:F33L
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33M]	CRITICAL	EEEE:F33M
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33N]	CRITICAL	EEEE:F33N
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33P]	CRITICAL	EEEE:F33P
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33Q]	CRITICAL	EEEE:F33Q

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0364	128S0264		ALL	Kemet alt to Sanyo
128S0303	128S0353		ALL	Panasonic alt to Sanyo
376S0953	376S0958		ALL	RENESAS ALT TO FAIRCHILD
128S0311	128S0329		ALL	NEC ALT TO SANYO
353S3237	353S2192		ALL	TI ALT TO INTERSIL
376S0977	376S0859		ALL	Diodes alt to Toshiba
138S0722	138S0691		ALL	Multi alt to Samsung
197S0487	197S0485		ALL	Epson alt to TXC
197S0484	197S0485		ALL	NDK alt to TXC
197S0479	197S0486		ALL	Epson alt to TXC
197S0478	197S0486		ALL	NDK alt to TXC
197S0481	197S0480		ALL	Epson alt to NDK
376S0972	376S0612		ALL	ROHM alt to Toshiba
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S1017	376S0612		ALL	ROHM alt to Toshiba
138S0624	138S0677		ALL	Murata alt to Taiyo Yuden
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
152S1703	152S1701		ALL	Sumida alt to Cyntec
371S0730	371S0490		ALL	Diodes alt to NXP
138S0725	138S0724		ALL	Samsung alt to Murata
138S0727	138S0709		ALL	Samsung alt to Murata
376S1080	376S0820		ALL	Diodes alt to ON Semi
372S0186	372S0185		ALL	NXP alt to Diodes
128S0363	128S0296		ALL	NEC alt to Sanyo
376S0903	376S0796		ALL	Fairchild alt to Siliconix
740S0144	740S0118		ALL	Littlefuse alt to Polytronic
152S1539	152S1598		ALL	Cyntec alt to Toko
152S1645	152S0461		ALL	Cyntec alt to Vishay
155S0667	155S0583		ALL	MAG LAYERS ALT TO MURATA
103S0305	103S0266		ALL	Yageo alt to Cyntec
112S0274	112S0254		ALL	Yageo alt to Cyntec
376S1113	376S1110		ALL	Diodes to AOS
155S0588	155S0367		ALL	murata ALT TO MURATA

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4181	1	IVB,QBP0,ES2,KB,2.3,35W,2+2,1.0,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.3G_ES2
337S4182	1	IVB,QBP0,ES2,KB,2.6,35W,2+2,1.05,4M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.6G_ES2
337S4292	1	IVB,Q4CT,Q5,L1,2.5,35W,2+2,1.1,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.5G_Q5
337S4300	1	IVB,QC36,Q5,L1,2.6,35W,2+2,1.2,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.6G_Q5
337S4302	1	IVB,QC34,Q5,L1,2.8,35W,2+2,1.2,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.8G_Q5
337S4294	1	IVB,QC4M,Q5,L1,2.9,35W,2+2,1.25,4M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.9G_Q5
337S4264	1	IVB,S R0N0,PRQ,L1,2.5,35W,2+2,1.1,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.5G
337S4338	1	IVB,S R0MY,PRQ,L1,2.6,35W,2+2,1.2,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.6G
337S4339	1	IVB,S R0MU,PRQ,L1,2.8,35W,2+2,1.2,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.8G
337S4265	1	IVB,S R0MU,PRQ,L1,2.9,35W,2+2,1.25,4M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.9G
337S4180	1	IC,PCH,PPT-MB SFF,ES2,B0	U1800	CRITICAL	PCH_ES2
337S4235	1	IC,PCH,PPT-MB SFF,P-Q5,C0	U1800	CRITICAL	PCH_C0
337S4283	1	IC,PCH,PPT-MB SFF,PRQ,C1	U1800	CRITICAL	PCH_C1
338S1113	1	IC,TBT,CR-4C,B1,FRQ,288FCBGA,12X12MM	U3600	CRITICAL	TBTRTR:B1
333S0623	16	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78FBGA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	2G_SAMSUNG_35NM_1600_S
333S0622	16	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78FBGA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	2G_HYNIX_1600_S
333S0628	16	IC,SDRAM,DDR3-1600,256MX8,78FBGA,D-DIE,ELPIDA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	2G_ELPIDA_1600_S
333S0649	16	IC,SDRAM,DDR3-1600,256MX8,78FBGA,MICRON	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	2G_MICRON_1600_S
333S0625	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,HYNIX	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_HYNIX_1600_S
333S0629	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,D-DIE,ELPIDA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_ELPIDA_1600_S
333S0624	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,D35,SAMSUNG	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_SAMSUNG_35NM_1600_S
333S0623	8	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78FBGA	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_SAMSUNG_35NM_CH0_1600_S
333S0624	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,D35,SAMSUNG	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070	CRITICAL	6G_SAMSUNG_35NM_CH0_1600_S
333S0622	8	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78FBGA	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_HYNIX_CH0_1600_S
333S0625	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,HYNIX	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070	CRITICAL	6G_HYNIX_CH0_1600_S
333S0628	8	IC,SDRAM,DDR3-1600,256MX8,78FBGA,D-DIE,ELPIDA	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_ELPIDA_CH0_1600_S
333S0629	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,D-DIE,ELPIDA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070	CRITICAL	6G_ELPIDA_CH0_1600_S
333S0660	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,MICRON	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_MICRON_1600_S
333S0649	8	IC,SDRAM,DDR3-1600,256MX8,78FBGA,MICRON	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_MICRON_CH0_1600_S
333S0660	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,MICRON	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070	CRITICAL	6G_MICRON_CH0_1600_S

D1 BOM GROUPS

BOM GROUP	BOM OPTIONS
D1_COMMON	ALTERNATE,COMMON,D1_COMMON1,D1_COMMON2,D1_PROGPARTS,D1_PVB
D1_COMMON1	CPUMEM:S0,SMC_DEBUG_YES,TBTBST:Y,TBTRTR:B1,TBTHV:P15V,HUB_2NONREM,USBHUB:2512B,AXG_PHASE2,TBTISNS:YES
D1_COMMON2	EDP:YES,PPDDR:1V35,LPCPLUS_CONN:YES,LPCPLUS_R:YES,CAPS:INT,BTPWR:S4,SKIP_5V3V3:AUDIBLE,TPAD_5V_LDO:S5,SMS
D1_PVB	LOADISNS:NO,LCDBKLT:PROD,KBDBKLT:PROD
D1_PROGPARTS	SMC_PROG:PVB,TBTROM:PROG,BOOTROM_PROG:PVB,TPAD_PSOC:PROG
D1_BLANK	
D1_DEVEL:ENG	ALTERNATE,IVB_PPT_XDP,LOADISNS:YES,S0PGOOD_ISL,DDRVREF_DAC,VREFDQ:M1_M3,VREFCA:LDO_DAC
D1_DEVEL:PVB	ALTERNATE,IVB_PPT_XDP,VREFDQ:M1_M3,VREFCA:LDO
IVB_PPT_XDP	XDP,XDP_CONN,XDP_CPU:BPM,XDP_PCH

DDR3 SPD STRAPPINGS

BOM GROUP	BOM OPTIONS
RAM_4G_HYNIX_1600_S	4G_HYNIX_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_2G_ELPIDA_1600_S	2G_ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_4G_SAMSUNG_28NM_1600_S	4G_SAMSUNG_28NM_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_2G_MICRON_1600_S	2G_MICRON_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_ELPIDA_1600_S	4G_ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_4G_SAMSUNG_35NM_1600_S	4G_SAMSUNG_35NM_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_6G_SAMSUNG_35NM_CH0_1600_S	6G_SAMSUNG_35NM_CH0_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM_4G_MICRON_1600_S	4G_MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM_6G_MICRON_CH0_1600_S	6G_MICRON_CH0_1600_S,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_6G_ELPIDA_CH0_1600_S	6G_ELPIDA_CH0_1600_S,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_6G_SAMSUNG_28NM_CH0_1600_S	6G_SAMSUNG_28NM_CH0_1600_S,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_6G_HYNIX_CH0_1600_S	6G_HYNIX_CH0_1600_S,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_2G_SAMSUNG_1600_S	2G_SAMSUNG_35NM_1600_S,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_2G_HYNIX_1600_S	2G_HYNIX_1600_S,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0642	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_SAMSUNG_28NM_1600_S
333S0623	8	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78FBGA	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_SAMSUNG_28NM_CH0_1600_S
333S0642	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070	CRITICAL	6G_SAMSUNG_28NM_CH0_1600_S

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-1533	1	STDOFF,BMU,TOPSIDE,D1,SM	J6950_63	CRITICAL	
860-1530	1	STDOFF-1.9D2.93H-TH-0.85-1.2	J6950_64	CRITICAL	
860-1529	1	STDOFF-1.80D1.53H-SM	J6950_65	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	
946-4350	1	D1 MLB LOCTITE UV GLUE 190024/S 0.24G	EDGE_BOND	CRITICAL	

DEVELOPMENT/BASE BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-4094	1	D1 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9189	1	D1 MLB BASE BOM	BASE	CRITICAL	BASE_BOM

SMC

341S3528	1	IC,SMC12,PROTO1,D1	U4900	CRITICAL	SMC_PROG:PROTO
341S3404	1	IC,SMC,DEVELOPMENT-P1B,D1	U4900	CRITICAL	SMC_PROG:P1B
341S3405	1	IC,SMC,DEVELOPMENT-FSB,D1	U4900	CRITICAL	SMC_PROG:FSB
341S3406	1	IC,SMC,DEVELOPMENT-PVB,D1	U4900	CRITICAL	SMC_PROG:PVB

EFI ROM

341S3571	1	IC,EF,ROM,PROTO1,D1	U6100	CRITICAL	BOOTROM_PROG:PROTO
341S3603	1	IC,EFI,ROM,P1B, D1	U6100	CRITICAL	BOOTROM_PROG:P1B
341S3636	1	IC,EFI,ROM,P1B2, D1	U6100	CRITICAL	BOOTROM_PROG:P1B2
341S3650	1	IC,EFI,ROM,FSB, D1	U6100	CRITICAL	BOOTROM_PROG:FSB
341SXXXX	1	IC,EFI,ROM,FSB2, D1	U6100	CRITICAL	BOOTROM_PROG:FSB2
341S3667	1	IC,EFI,ROM,PVB, D1	U6100	CRITICAL	BOOTROM_PROG:PVB

Programmables - All builds

335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Macronix	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Numonyx	U6100	CRITICAL	BOOTROM_BLANK
341S3670	1	IC,TP PSOC,V224,PVB,D1	U5701	CRITICAL	TPAD_PSOC:PROG
337S2983	1	IC,TP PSOC,QFN,BLANK	U5701	CRITICAL	TPAD_PSOC:BLANK
341S3668	1	IC,EEPROM,CR,V14.1,D1 PVB	U3690	CRITICAL	TBTROM:PROG
335S0865	1	IC,EEPROM,SERIAL,8KB,S3C	U3690	CRITICAL	TBTROM:BLANK
338S1098	1	IC,SMC12-A3,LX4FS1AH58BC1GA3	U4900	CRITICAL	SMC_BLANK
998-3919	1	SOCKET, SMC12	J4900	CRITICAL	SMC_SOCKET

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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BOM Configuration

Apple Inc.

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Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST
- PP5V_S0 — 7 8 — 3 TPs per Fan
- FAN_LT_PWM — 46
- FAN_LT_TACH — 46

J5660 (RIGHT FAN CONN)
- FAN_RT_PWM — 46
- FAN_RT_TACH — 46
- GND — 5 TPs per Fan

J3502 (ALS/CAMERA CONN)
- SMBUS_SMC_2_S3_SDA — 7 39 42 77
- SMBUS_SMC_2_S3_SCL — 7 39 42 77
- PP5V_S3_ALSCAMERA_F — 7 32

J4400 (RIO CABLE CONN)
- PP3V3_S4 — 7 8
- PP3V3_S3 — 7 8
- PP3V3_WLAN_F — 7 36 40 80
- PP5V_S4 — 8
- PP1V5_S0 — 8

J4410 (RIO FLEX CONN)
- USB_EXTB_OC_L — 24 36
- HDMI_IG_DDC_CLK — 9 36
- HDMI_IG_DDC_DATA — 9 36
- HDMI_HPD_L — 36 40
- PM_SLP_S3_L — 7 18 27 36 39 66
- PM_SLP_S4_L — 18 27 36 38 39 66
- AP_CLKREQ_Q_L — 7 36
- ENET_RESET_L — 25
- ENET_CLKREQ_L — 17 36
- SD_PWR_EN — 9 36
- SCONN_STATE_CHANGE_SMC — 25 40
- PCIE_WAKE_L — 7 18 36
- AP_CLKREQ_Q_L — 7 36
- AP_RESET_CONN_L — 7 36
- WIFI_EVENT_L — 36 39 40
- USB_EXTB_P — 26 36 74
- USB_EXTB_N — 26 36 74
- USB_BT_CONN_P — 9 36 74
- USB_BT_CONN_N — 9 36 74

- AP_RESET_CONN_L — 7 36
- SMBUS_PCH_CLK — 17 42 75
- SMBUS_PCH_DATA — 17 42 75

- SMBUS_SMC_1_S0_SCL — 39 42 77
- SMBUS_SMC_1_S0_SDA — 39 42 77

J5815 (KBD BACKLIGHT CONN)
- PP_KBD_BOOST_VOUT — 48
- KBDLED_CATHODE1 — 48
- KBDLED_CATHODE2 — 48
- SMC_KBDLED_PRESENT_L — 48

J6950 (MAIN BATT CONN)
- PPVBAT_G3H_CONN — 66 67
- SMBUS_SMC_5_G3_SCL — 39 42
- SMBUS_SMC_5_G3_SDA — 39 42
- SYS_DETECT_L_R

- SYSDET1
- SYSDET_3_4 — 56

J6801 (2 MIC CONN)
- CON_DMIC_PWR — 55
- CON_DMIC_SDA1 — 55
- CON_DMIC_CLK — 55

- PCH_VSS_NCTF<19> — 7
- PCH_VSS_NCTF<19> — 7

J4600 (LEFT USB CONN)
- PP5V_S3_LTUSB_A_F — 38
- USB_LT1_N — 38 74
- USB_LT1_P — 38 74

FUNC_TEST
- GND
- GND
- GND — 6 TPs

U1000 CHARZ TPS

PCIE_TBT_D2R_P<0>	75 33 9	P2MM SM	PP0700
PCIE_TBT_D2R_N<0>	75 33 9	P2MM SM	PP0701
DMI_S2N_P<0>	46	P2MM SM	PP0702
DMI_S2N_N<0>	46	P2MM SM	PP0703
DMI_CLK100M_CPU_P	1	P2MM SM	PP0721
DMI_CLK100M_CPU_N	1	P2MM SM	PP0722

U1800 CHARZ TPS

DMI_N2S_P<0>	72 18 16	P2MM SM	PP0704
DMI_N2S_N<0>	72 18 16	P2MM SM	PP0705
FDI_DATA_P<0>	18	P2MM SM	PP0706
FDI_DATA_N<0>	18	P2MM SM	PP0707
FDI_DATA_P<4>	18	P2MM SM	PP0708
FDI_DATA_N<4>	18	P2MM SM	PP0709
PCIE_AP_D2R_P	17	P2MM SM	PP0710
PCIE_AP_D2R_N	17	P2MM SM	PP0711
PCIE_ENET_D2R_P	17	P2MM SM	PP0712
PCIE_ENET_D2R_N	17	P2MM SM	PP0713
PCIE_CLK100M_TBT_P	1	P2MM SM	PP0723
PCIE_CLK100M_TBT_N	1	P2MM SM	PP0724

U4900 CHARZ TPS

LPC_AD<0>	1	P2MM SM	PP0714
LPC_AD<1>	1	P2MM SM	PP0715
LPC_AD<2>	1	P2MM SM	PP0716
LPC_AD<3>	1	P2MM SM	PP0717
LPC_FRAME_L	1	P2MM SM	PP0718
LPC_CLK33M_SMC	1	P2MM SM	PP0719
AUD_DMIC_SDA1	55 51	P2MM SM	PP0720

J6701 (AUDIO JACK CONN)
- AUD_CONN_SLEEVE — 54
- AUD_CONN_MIC_XW — 54
- AUD_CONN_SLEEVE_XW — 54
- AUD_CONN_HP_LEFT — 54
- AUD_CONN_TIPDET_INV — 54
- PP3V3_S0 — 7 8 78
- AUD_SPDIF_OUT_JACK — 51 54
- AUD_CONN_HP_RIGHT — 54
- AUD_CONN_TYPEDET — 54
- AUD_CONN_MIC — 54

J6802 (AUDIO LEFT SPEAKER CONN)
- SPKRCONN_L_OUT_P — 53 55 78
- SPKRCONN_L_OUT_N — 53 55 78
- SPKRCONN_L_ID — 51 55
- SPKRCONN_SL_OUT_P — 53 55 78
- SPKRCONN_SL_OUT_N — 53 55 78

J6803 (AUDIO RIGHT SPEAKER CONN)
- SPKRCONN_R_OUT_P — 53 55 78
- SPKRCONN_R_OUT_N — 53 55 78
- SPKRCONN_R_ID — 51 55
- SPKRCONN_SR_OUT_P — 53 55 78
- SPKRCONN_SR_OUT_N — 53 55 78
- GND — 53 55 78

J9000 (EDP CONN)
- PP5VR3V3_SW_LCD — 67
- PPVOUT_S0_LCDBKLT — 67 71 80 — 2 TP needed
- LED_RETURN_6 — 7 67 71
- LED_RETURN_5 — 7 67 71
- LED_RETURN_4 — 7 67 71
- LED_RETURN_3 — 7 67 71
- LED_RETURN_2 — 7 67 71
- LED_RETURN_1 — 67 71
- LCD_HPD_CONN — 67
- DP_INT_AUX_P — 67 79
- DP_INT_AUX_N — 67 79

J3401 & J3402 (AIRPORT/BT/CAMERA CONN)
- PCIE_CLK100M_AP_CONN_P — 36 78
- PCIE_CLK100M_AP_CONN_N — 36 78
- AP_CLKREQ_Q_L — 7 36
- PCIE_WAKE_L — 7 18 36
- AP_RESET_CONN_L — 7 36
- PP3V3_WLAN_F — 7 36 40 80
- PP5V_S3_ALSCAMERA_F — 7 32
- SMBUS_SMC_2_S3_SDA — 7 39 42 77
- SMBUS_SMC_2_S3_SCL — 7 39 42 77
- USB_CAMERA_CONN_P — 32 74
- USB_CAMERA_CONN_N — 32 74

J5713 (KEY BOARD CONN)
- PP3V3_S4 — 7 8
- PP3V42_G3H — 7 8
- WS_KBD1 — 47
- WS_KBD2 — 47
- WS_KBD3 — 47
- WS_KBD4 — 47
- WS_KBD5 — 47
- WS_KBD6 — 47
- WS_KBD7 — 47
- WS_KBD8 — 47
- WS_KBD9 — 47
- WS_KBD10 — 47
- WS_KBD11 — 47
- WS_KBD12 — 47
- WS_KBD13 — 47
- WS_KBD14 — 47
- WS_KBD15_CAP — 47
- WS_KBD16_NUM — 47
- WS_KBD17 — 47
- WS_KBD18 — 47
- WS_KBD19 — 47
- WS_KBD20 — 47
- WS_KBD21 — 47
- WS_KBD22 — 47
- WS_KBD23 — 47
- WS_KBD_ONOFF_L — 47
- WS_LEFT_SHIFT_KBD — 47
- WS_LEFT_OPTION_KBD — 47
- WS_CONTROL_KBD — 47

J5700 (IPD FLEX CONN)
- PP3V3_S4 — 7 8
- Z2_CS_L — 47
- Z2_MOSI — 47
- Z2_MISO — 47
- Z2_SCLK — 47
- Z2_HOST_INTN — 47
- PP5V_S4_CUMULUS — 47
- Z2_CLKIN — 47
- SMBUS_SMC_2_S3_SCL — 7 39 42 77
- SMBUS_SMC_2_S3_SDA — 7 39 42 77
- PSOC_SCLK — 47
- PSOC_MOSI — 47
- PSOC_MISO — 47
- PICKB_L — 47
- PSOC_F_CS_L — 47
- Z2_KEY_ACT_L — 47

J6900 (DC POWER CONN)
- TDM_ONEWIRE_MPM
- ADAPTER_SENSE — 56
- PP18V5_DCIN_FUSE — 56
- GND

J4500 (SSD/HDD FLEX CONN)
- PP3V3_S0_SSD_FLT — 37
- SMC_OOB1_TX_L — 37 39 40
- SMC_OOB1_RX_L — 37 39 40
- PP5V_S0_HDD_FLT — 37
- GND

FUNC_TEST
- BKLT_EN — 71
- LCD_BKLT_PWM — 9 71
- PM_CLKRUN_L — 7 18 39 41
- PM_SYSRST_L — 18 25 39
- SMC_ONOFF_L — 39 40 47

J5100 (LPC + SPI CONN)
- PP3V42_G3H — 7 8
- PP5V_S0 — 7 8
- LPC_CLK33M_LPCPLUS — 25 41 75
- LPC_AD<0> — 7 17 39 41 75
- LPC_AD<2> — 7 17 39 41 75
- LPC_AD<1> — 7 17 39 41 75
- LPC_AD<3> — 7 17 39 41 75
- SPI_ALT_MOSI — 41
- LPCPLUS_GPIO — 20 41
- LPCPLUS_RESET_L — 25 41
- SMC_TDO — 39 40 41
- TP_SMC_TRST_L — 41
- TP_SMC_MD1 — 41
- SMC_TX_L — 39 40 41
- SPI_ALT_MISO — 41
- LPC_FRAME_L — 7 17 39 41 75
- SPIROM_USE_MLB — 20 41 50
- PM_CLKRUN_L — 7 18 39 41
- SPI_ALT_CLK — 41
- SPI_ALT_CS_L — 41
- LPC_SERIRQ — 17 39 41
- LPC_PWRDWN_L — 18 25 39 41
- SMC_TDI — 39 40 41
- SMC_TCK — 39 40 41
- SMC_RESET_L — 39 40 41 57
- SMC_ROMBOOT — 40 41
- SMC_RX_L — 39 40 41
- SMC_TMS — 39 40 41

POWER RAILS

FUNC_TEST
- PM_SLP_S3_L — 7 18 27 36 39 66
- PP0V75_S0_DDRVTT — 8
- PP1V05_S0 — 8

- LED_RETURN_2 — 7 67 71
- LED_RETURN_3 — 7 67 71
- LED_RETURN_4 — 7 67 71
- LED_RETURN_5 — 7 67 71
- LED_RETURN_6 — 7 67 71
- GND — 4 TPs

- PP3V3_S0 — 7 8 78
- PP3V3_S3 — 7 8
- PP3V3_S5 — 8 78
- PP3V3_S5_AVREF_SMC — 39 40
- PP3V42_G3H — 7 8
- PP5V_S0 — 7 8
- PP5V_S3 — 8
- PP5V_S5 — 8
- PPBUS_G3H — 8
- PPDCIN_G3H — 8
- PPVCORE_S0_CPU — 8
- PPVTTDDR_S3 — 8

- DMI_S2N_P<3..1> — 18 18 72 — TRUE
- DMI_S2N_N<3..1> — 18 18 72 — TRUE
- DMI_N2S_P<3..1> — 18 18 72 — TRUE
- DMI_N2S_N<3..1> — 18 18 72 — TRUE

- TBTBPWRSW_ISET_V3P3 — 70 — TRUE
- TBTBPWRSW_ISET_S0_R — 70
- TBTBPWRSW_ISET_S3 — 70 — TRUE
- TBTAPWRSW_ISET_V3P3 — 69 — TRUE
- TBTAPWRSW_ISET_S0 — 69 — TRUE
- TBTAPWRSW_ISET_S3 — 69 — TRUE
- TBTAPWRSW_ISET_S3_R — 69 — TRUE

- TBT_A_R2D_C_P<1..0> — 33 69 76 — TRUE
- TBT_A_R2D_C_N<1..0> — 33 69 76 — TRUE
- TBT_A_R2D_P<1..0> — 69 76 — TRUE
- TBT_A_R2D_N<1..0> — 69 76 — TRUE
- TBT_A_D2R_C_P<1> — 69 76 — TRUE
- TBT_A_D2R_C_N<1> — 69 76 — TRUE
- TBT_A_D2R_C_P<0> — 69 76 — TRUE
- TBT_A_D2R_C_N<0> — 69 76 — TRUE
- TBT_A_D2R_P<1> — 33 69 76 — TRUE
- TBT_A_D2R_N<1> — 33 69 76 — TRUE
- TBT_A_D2R_P<0> — 33 69 76 — TRUE
- TBT_A_D2R_N<0> — 33 69 76 — TRUE
- TBT_B_R2D_C_P<1..0> — 33 70 76 — TRUE
- TBT_B_R2D_C_N<1..0> — 33 70 76 — TRUE
- TBT_B_R2D_P<1..0> — 70 76 — TRUE
- TBT_B_R2D_N<1..0> — 70 76 — TRUE
- TBT_B_D2R_C_P<0> — 70 76 — TRUE
- TBT_B_D2R_C_N<0> — 70 76 — TRUE
- TBT_B_D2R_C_P<1> — 70 76 — TRUE
- TBT_B_D2R_C_N<1> — 70 76 — TRUE
- TBT_B_D2R_P<0> — 33 70 76 — TRUE
- TBT_B_D2R_N<0> — 33 70 76 — TRUE
- TBT_B_D2R_P<1> — 33 70 76 — TRUE
- TBT_B_D2R_N<1> — 33 70 76 — TRUE

- PCIE_AP_D2R_P — 7 17 36 75
- PCIE_AP_D2R_N — 7 17 36 75
- PCIE_AP_R2D_P — 36 75
- PCIE_AP_R2D_N — 36 75

ICT Test Points

CPU NO_TESTs

TP_TBT_MONDC0	TRUE MAKE_BASE=TRUE	NC_TBT_MONDC0
TP_TBT_MONDC1	TRUE MAKE_BASE=TRUE	NC_TBT_MONDC1
TP_TBT_PCIE_RESET0_L	TRUE MAKE_BASE=TRUE	NC_TBT_PCIE_RESET0_L
TP_TBT_PCIE_RESET1_L	TRUE MAKE_BASE=TRUE	NC_TBT_PCIE_RESET1_L
TP_TBT_PCIE_RESET2_L	TRUE MAKE_BASE=TRUE	NC_TBT_PCIE_RESET2_L
TP_TBT_PCIE_RESET3_L	TRUE MAKE_BASE=TRUE	NC_TBT_PCIE_RESET3_L
TP_TBT_XTAL25OUT	TRUE MAKE_BASE=TRUE	NC_TBT_XTAL25OUT

TP_DP_TBTSRC_ML_CP<3>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<3>
TP_DP_TBTSRC_ML_CN<3>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<3>
TP_DP_TBTSRC_ML_CP<2>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<2>
TP_DP_TBTSRC_ML_CN<2>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<2>
TP_DP_TBTSRC_ML_CP<1>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<1>
TP_DP_TBTSRC_ML_CN<1>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<1>
TP_DP_TBTSRC_ML_CP<0>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<0>
TP_DP_TBTSRC_ML_CN<0>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<0>
TP_DP_TBTSRC_AUXCH_CP	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_AUXCH_CP
TP_DP_TBTSRC_AUXCH_CN	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_AUXCH_CN

TP_SPI_CS1_L	TRUE MAKE_BASE=TRUE	NC_SPI_CS1_L
TP_PCH_GPIO8	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO8
TP_PCH_STRP_BBS1	TRUE MAKE_BASE=TRUE	NC_PCH_STRP_BBS1
TP_PCH_STRP_ESI_L	TRUE MAKE_BASE=TRUE	NC_PCH_STRP_ESI_L
TP_PCH_TP23	TRUE MAKE_BASE=TRUE	NC_PCH_TP23
TP_PCI_CLK33M_OUT2	TRUE MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT2
TP_PCIE_CLK100M_PEGAN	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEGAN
TP_PCIE_CLK100M_PEGAP	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEGAP
TP_PM_SLP_A_L	TRUE MAKE_BASE=TRUE	NC_PM_SLP_A_L
TP_PPVOUT_PCH_DCPSUSBYP	TRUE MAKE_BASE=TRUE	NC_PPVOUT_PCH_DCPSUSBYP
TP_SMC_MPM5_LED_PWR	TRUE MAKE_BASE=TRUE	NC_SMC_MPM5_LED_PWR
TP_SMC_MPM5_LED_CHG	TRUE MAKE_BASE=TRUE	NC_SMC_MPM5_LED_CHG
TP_SMS_INT2	TRUE MAKE_BASE=TRUE	NC_SMS_INT2

- PCIE_TBT_R2D_C_P<3..0> — TRUE — 9 33 75
- PCIE_TBT_R2D_C_N<3..0> — TRUE — 9 33 75
- PCIE_TBT_R2D_P<3..0> — TRUE — 33 75
- PCIE_TBT_R2D_N<3..0> — TRUE — 33 75
- PCIE_TBT_D2R_P<3..1> — TRUE — 9 33 75
- PCIE_TBT_D2R_N<3..1> — TRUE — 9 33 75
- PCIE_TBT_D2R_C_P<3..1> — TRUE — 33 75
- PCIE_TBT_D2R_C_N<3..1> — TRUE — 33 75

- MEM_A_DQ<0> — 12 28 73 — TRUE
- MEM_A_DQ<12..2> — TRUE — 12 28 73
- MEM_A_DQ<19..14> — TRUE — 12 28 73
- MEM_A_DQ<24..21> — TRUE — 12 28 73
- MEM_A_DQ<32..26> — TRUE — 12 28 73
- MEM_A_DQ<42..34> — TRUE — 12 28 73
- MEM_A_DQ<54..44> — TRUE — 12 28 73
- MEM_A_DQ<56> — TRUE — 12 28 73
- MEM_A_DQ<63..58> — TRUE — 12 28 73
- MEM_B_DQ<2..0> — TRUE — 12 29 73
- MEM_B_DQ<13..4> — TRUE — 12 29 73
- MEM_B_DQ<19..15> — TRUE — 12 29 73
- MEM_B_DQ<25..21> — TRUE — 12 29 73
- MEM_B_DQ<35..27> — TRUE — 12 29 73
- MEM_B_DQ<40..37> — TRUE — 12 29 73
- MEM_B_DQ<47..42> — TRUE — 12 29 73
- MEM_B_DQ<57..49> — TRUE — 12 29 73
- MEM_B_DQ<63..59> — TRUE — 12 29 73
- NC_MEM_EVENT_L — TRUE — 40

- HDMI_IG_CLK_C_P — TRUE — 9 36 78
- HDMI_IG_CLK_C_N — TRUE — 9 36 78
- HDMI_IG_DATA_C_P<2..0> — TRUE — 9 36 78
- HDMI_IG_DATA_C_N<2..0> — TRUE — 9 36 78

- PCIE_CLK100M_ENET_P — 7 17 36 75
- PCIE_CLK100M_ENET_N — 7 17 36 75
- USB3_EXTB_TX_C_P — 36 79
- USB3_EXTB_TX_C_N — 36 79

TP_XDP_PCH_HOOK4	TRUE	NC_XDP_PCH_HOOK4
TP_XDP_PCH_HOOK5	TRUE	NC_XDP_PCH_HOOK5
TP_XDP_PCH_OBSFN_B<0>	TRUE	NC_XDP_PCH_OBSFN_B<0>
TP_XDP_PCH_OBSFN_B<1>	TRUE	NC_XDP_PCH_OBSFN_B<1>
TP_XDP_PCH_OBSFN_A<0>	TRUE	NC_XDP_PCH_OBSFN_A<0>
TP_XDP_PCH_OBSFN_A<1>	TRUE	NC_XDP_PCH_OBSFN_A<1>
TP_XDP_PCH_OBSFN_D<0>	TRUE	NC_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_D<1>	TRUE	NC_XDP_PCH_OBSFN_D<1>
TP_XDP_PCH_TRST_L	TRUE	NC_XDP_PCH_TRST_L

TP_1V05_S0_PCH_VCCAPLLEXP	TRUE	NC_1V05_S0_PCH_VCCAPLLEXP
TP_AUD_CODEC_MICBIAS	TRUE	NC_AUD_CODEC_MICBIAS
TP_AUD_MIC_INRP	TRUE	NC_AUD_MIC_INRP
TP_AUD_MIC_INRN	TRUE	NC_AUD_MIC_INRN
AUD_SPDIF_IN	TRUE	AUD_SPDIF_IN
TP_BKL_FAULT	TRUE	NC_BKL_FAULT
TP_LPC_DREQ0_L	TRUE	NC_LPC_DREQ0_L

S2 CAMERA PCIE SIGNALS

NC_PCIE_CAMERA_D2RP	MAKE_BASE=TRUE	PCIE_EXCARD_D2R_N
NC_PCIE_CAMERA_D2RN	TRUE MAKE_BASE=TRUE	PCIE_EXCARD_D2R_P
NC_PCIE_CAMERA_R2D_CN	TRUE MAKE_BASE=TRUE	PCIE_EXCARD_R2D_C_N
NC_PCIE_CAMERA_R2D_CP	TRUE MAKE_BASE=TRUE	PCIE_EXCARD_R2D_C_P
NC_PCIE_CLK100M_CAMERAN	TRUE MAKE_BASE=TRUE	PCIE_CLK100M_EXCARD_N — 7 17 75
NC_PCIE_CLK100M_CAMERAP	TRUE MAKE_BASE=TRUE	PCIE_CLK100M_EXCARD_P — 7 17 75

NO_TEST NC NO_TESTs

	TRUE MAKE_BASE=TRUE	NC_PCIE_5_D2RN — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_5_D2RP — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_5_R2D_CN — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_5_R2D_CP — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_6_D2RN — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_6_D2RP — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_6_R2D_CN — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_6_R2D_CP — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_7_D2RN — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_7_D2RP — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_7_R2D_CN — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_7_R2D_CP — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_8_D2RN — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_8_D2RP — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_8_R2D_CN — 17
	TRUE MAKE_BASE=TRUE	NC_PCIE_8_R2D_CP — 17

TP_PCIE_CLK100M_PE4N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N — 17
TP_PCIE_CLK100M_PE4P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P — 17
TP_PCIE_CLK100M_PEBN	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN — 17
TP_PCIE_CLK100M_PEBP	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP — 17

TP_SATA_C_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_C_D2RN — 17
TP_SATA_C_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_C_D2RP — 17
TP_SATA_C_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_C_R2D_CN — 17
TP_SATA_C_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_C_R2D_CP — 17
TP_SATA_D_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_D_D2RN — 17
TP_SATA_D_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_D_D2RP — 17
TP_SATA_D_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_D_R2D_CN — 17
TP_SATA_D_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_D_R2D_CP — 17
TP_SATA_E_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_E_D2RN — 17
TP_SATA_E_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_E_D2RP — 17
TP_SATA_E_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_E_R2D_CN — 17
TP_SATA_E_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_E_R2D_CP — 17
TP_SATA_F_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_F_D2RN — 17
TP_SATA_F_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_F_D2RP — 17
TP_SATA_F_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_F_R2D_CN — 17
TP_SATA_F_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_F_R2D_CP — 17

TP_CRT_IG_BLUE	TRUE	NC_CRT_IG_BLUE — 18
TP_CRT_IG_GREEN	TRUE	NC_CRT_IG_GREEN — 18
TP_CRT_IG_RED	TRUE	NC_CRT_IG_RED — 18
TP_CRT_IG_DDC_CLK	TRUE	NC_CRT_IG_DDC_CLK — 18
TP_CRT_IG_DDC_DATA	TRUE	NC_CRT_IG_DDC_DATA — 18
TP_CRT_IG_HSYNC	TRUE	NC_CRT_IG_HSYNC — 18
TP_CRT_IG_VSYNC	TRUE	NC_CRT_IG_VSYNC — 18
TP_HDA_SDIN1	TRUE	NC_HDA_SDIN1 — 17
TP_HDA_SDIN2	TRUE	NC_HDA_SDIN2 — 17
TP_HDA_SDIN3	TRUE	NC_HDA_SDIN3 — 17

TP_SDVO_TVCLKINN	TRUE	NC_SDVO_TVCLKINN — 18
TP_SDVO_TVCLKINP	TRUE	NC_SDVO_TVCLKINP — 18
TP_SDVO_STALLN	TRUE	NC_SDVO_STALLN — 18
TP_SDVO_STALLP	TRUE	NC_SDVO_STALLP — 18
TP_SDVO_INTN	TRUE	NC_SDVO_INTN — 18
TP_SDVO_INTP	TRUE	NC_SDVO_INTP — 18
TP_PCI_PME_L	TRUE	NC_PCI_PME_L — 19
TP_PCI_CLK33M_OUT3	TRUE	NC_PCI_CLK33M_OUT3 — 19
	TRUE MAKE_BASE=TRUE	NC_ISNS_LCDBKLTN — 80
	TRUE MAKE_BASE=TRUE	NC_ISNS_LCDBKLTP — 80
	TRUE MAKE_BASE=TRUE	NC_ISNS_WLANN — 80
	TRUE MAKE_BASE=TRUE	NC_ISNS_WLANP — 80
	TRUE MAKE_BASE=TRUE	NC_ISNS_LCD_PANELN — 67 80
	TRUE MAKE_BASE=TRUE	NC_ISNS_LCD_PANELP — 67 80

PCH ALIASES

NC_LPC_DREQ0_L	TRUE	TP_LPC_DREQ0_L — 7 17
NC_LPC_DREQ1_L	TRUE	TP_LPC_DREQ1_L
TP_CLINK_CLK	TRUE	NC_CLINK_CLK — 17
TP_CLINK_DATA	TRUE	NC_CLINK_DATA — 17
TP_CLINK_RESET_L	TRUE	NC_CLINK_RESET_L — 17

- PCIE_ENET_R2D_C_P — TRUE
- PCIE_ENET_R2D_C_N — TRUE

- PCIE_AP_R2D_C_P — TRUE
- PCIE_AP_R2D_C_N — TRUE
- PCIE_AP_D2R_P — TRUE
- PCIE_AP_D2R_N — TRUE

- PCIE_AP_D2R_PI_P — TRUE
- PCIE_AP_D2R_PI_N — TRUE
- PCIE_AP_R2D_PI_P — TRUE
- PCIE_AP_R2D_PI_N — TRUE

- PCIE_CLK100M_PCH_P — TRUE
- PCIE_CLK100M_PCH_N — TRUE
- PCIE_CLK100M_TBT_P — TRUE
- PCIE_CLK100M_TBT_N — TRUE

- PCH_CLK100M_SATA_P — TRUE

- PCH_CLK33M_PCIIN — TRUE

- PCIE_CLK100M_SSD_P — TRUE
- PCIE_CLK100M_SSD_N — TRUE
- PEG_CLK100M_P — TRUE
- PEG_CLK100M_N — TRUE
- PCIE_CLK100M_ENET_P — TRUE
- PCIE_CLK100M_ENET_N — TRUE
- PCIE_CLK100M_AP_P — TRUE
- PCIE_CLK100M_AP_N — TRUE
- PCIE_CLK100M_FW_P — TRUE
- PCIE_CLK100M_FW_N — TRUE
- PCIE_CLK100M_EXCARD_P — TRUE
- PCIE_CLK100M_EXCARD_N — TRUE

- SATA_HDD_R2D_RDRIN_P — TRUE
- SATA_HDD_R2D_RDRIN_N — TRUE
- SATA_HDD_D2R_RDROUT_P — TRUE
- SATA_HDD_D2R_RDROUT_N — TRUE
- SATA_HDD_D2R_RDRIN_P — TRUE
- SATA_HDD_D2R_RDRIN_N — TRUE
- SATA_HDD_R2D_RDROUT_P — TRUE
- SATA_HDD_R2D_RDROUT_N — TRUE
- SATA_HDD_D2R_RC_P — TRUE
- SATA_HDD_D2R_RC_N — TRUE
- SATA_HDD_R2D_RC_N — TRUE
- SATA_HDD_R2D_RC_P — TRUE

- SATA_HDD_R2D_C_P — TRUE
- SATA_HDD_R2D_C_N — TRUE
- SATA_HDD_D2R_P — TRUE
- SATA_HDD_D2R_N — TRUE

- SATA_SSDRHDD_D2R_P — TRUE
- SATA_SSDRHDD_D2R_N — TRUE
- SATA_SSDRHDD_R2D_P — TRUE
- SATA_SSDRHDD_R2D_N — TRUE

- USB3_EXTA_RX_F_P — TRUE
- USB3_EXTA_RX_F_N — TRUE
- USB3_EXTA_RX_P — TRUE
- USB3_EXTA_RX_N — TRUE

- USB3_EXTA_TX_C_P — TRUE
- USB3_EXTA_TX_C_N — TRUE
- USB3_EXTA_TX_N — TRUE
- USB3_EXTA_RX_N — TRUE

- USB3_EXTB_RX_RC_P — TRUE
- USB3_EXTB_RX_RC_N — TRUE
- USB3_EXTB_RX_P — TRUE
- USB3_EXTB_RX_N — TRUE

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Functional / ICT Test

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

C

B

A

G3H Rails

=PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPBUS_S0_LCDBKLT
=PPVIN_S5_HS_OTHER_ISNS_R
=PPVIN_S5_HS_COMPUTING_ISNS_R
=PPVIN_SW_TBTBST
=PPBUS_S0_VSENSE
=PPBUS_G3H_T25_R

=PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_CPUIMVP
=PPVIN_S3_DDRREG
=PPVIN_S0_CPUVCCIOS0
=PPVIN_S0_CPUAXG
=PPVIN_S0_VCCSAS0

=PPVIN_S5_HS_OTHER_ISNS
PPVIN_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE
=PPVIN_S5_P5VP3V3

=PP18V5_DCIN_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 mm VOLTAGE=18.5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PPDCIN_S5_CHGR

=PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP3V3_S5_LPCPLUS
=PP3V3_S5_SMC
=PP3V42_G3H_CHGR
=PP3V42_G3H_ONEWIREPROT
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_SMBUS_SMC_5
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_TPAD
=PPVIN_S5_SMCVREF
=PPVBAT_G3_SYSCLK

=PP3V42_G3H_BMU
=PP3V42_G3H_AUDIO
=PP3V42_G3H_TDM
=PP3V42_S3_HALL

For PCH RTC Power

=PPVRTC_G3_OUT
PPVRTC_G3H
MIN_LINE_WIDTH=0.3 mm VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PPVRTC_G3_PCH

5V Rails

=PP5V_S5_LDO
PP5V_S5
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.1 mm MAKE_BASE=TRUE
=PP5V_S5_P1V5S3RS0FET
=PP5V_S5_P5VSUSFET
=PP5V_S5_TPAD

=PP5V_SUS_FET
PP5V_SUS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP5V_SUS_PCH

=PP5V_S4_REG
PP5V_S4
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP5V_S0_LCD
=PP5V_S3_LTUSB
=PP5V_S4_P5VS0FET
=PP5V_S4_P5VS3FET
=PP5V_S4_AUDIO
=PP5V_S4_RIO
=PP5V_S4_P1V05TBTS0
=PP5V_S4_TPAD

=PP5V_S3_FET
PP5V_S3
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP5V_S3_ISNS
=PP5V_S3_ALSCAMERA
=PP5V_S3_DDRREG
=PP5V_S3_DEBUG_ADC_AVDD
=PP5V_S3_DEBUG_ADC_DVDD
=PP5V_S3_DEBUG_ISNS
=PP5V_S3_MEMRESET

=PP5V_S0_FET
PP5V_S0
MIN_LINE_WIDTH=0.4 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP5V_S0_AUDIO_XW
=PP5V_S0_AUDIO
=PP5V_S0_BKL
=PP5V_S0_CPUIMVP
=PP5V_S0_CPUVCCIOS0
=PP5V_S0_FAN_LT
=PP5V_S0_FAN_RT
=PP5V_S0_KBDLED
=PP5V_S0_LPCPLUS
=PP5V_S0_PCH
=PP5V_S0_HDD
=PP5V_S0_RMC
=PP5V_S0_VCCSAS0
=PP5V_S0_VMON

3.3V Rails

=PP3V3_S4_FET
PP3V3_S4
MIN_LINE_WIDTH=0.6 mm VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1 mm MAKE_BASE=TRUE
=PP3V3_S4_TBT
=PP3V3_S4_RIO
=PP3V3_S4_TPAD
=PP3V3_S4_SMC
=PP3V3_S4_BT

=PP3V3_SUS_FET
PP3V3_SUS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP3V3_SUS_P1V05SUSLDO
=PP3V3_SUS_PCH
=PP3V3_SUS_PCH_VCCSUS
=PP3V3_SUS_PCH_VCCSUS_GPIO
=PP3V3_SUS_ROM
=PP3V3_SUS_PCH_GPIO
=PP3V3_SUS_PCH_VCCSUS_USB
=PP3V3_SUS_PCH_VCC_SPI
=PP3V3_SUS_CNTRL
=PP3V3_SUS_SMC

=PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S0_P3V3S0FET
=PP3V3_S3_P3V3S3FET
=PP3V3_S4_TBTAPWRSW
=PP3V3_S4_TBTBPWRSW
=PP3V3_S4_P3V3S4FET
=PP3V3_S5_CPU_VCCDDR
=PP3V3_S5_P3V3SUSFET
=PP3V3_S5_PCH
=PP3V3_S5_PCHPWRGD
=PP3V3_S5_PCH_GPIO
=PP3V3_S5_PCH_VCCDSW
=PP3V3_S5_PWRCTL
=PP3V3_S5_SMCBATLOW
=PP3V3_S5_SYSCLK
=PP3V3_S5_VMON
=PP3V3_S5_XDP
=PP3V3_S5_P1V5S0

=PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.58MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.28MM MAKE_BASE=TRUE
=PP3V3_S3_ISNS
=PP3V3_S3_MEMRESET
=PP3V3_S3_PCH_GPIO
=PP3V3_S3_RIO
=PP3V3_S3_SMBUS_SMC_2_S3
=PP3V3_S3_SMBUS_SMC_3
=PP3V3_S3_USBMUX
=PP3V3_S3_USB_HUB
=PP3V3_S3_USB_RESET
=PP3V3_S3_VREFMRGN
=PP3V3_S3_WLAN
=PP3V3_S3_GYRO
=PP3V3_S3_SMS
=PP3V3_S3_SDBUF
=PP3V3_S3_CAMERA
=PP3V3_S3_P1V2S3
=PP3V3_S3_P1V8S3
=PP3V3_S3_BT

=PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.075 mm MAKE_BASE=TRUE
=PP3V3_S0_AUDIO
=PP3V3_S0_AUDIO_DIG
=PP3V3_S0_BKL_VDDIO
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_P1V5S0
=PP3V3_S0_P1V8S0
=PP3V3_S0_BKLI2C
=PP3V3_S0_DDCMUX
=PP3V3_S0_FAN_LT
=PP3V3_S0_FAN_RT
=PP3V3_S0_GPUTHMSNS
=PP3V3_S0_HS_ISNS
=PP3V3_S0_IMVPISNS
=PP3V3_S0_ISNS
=PP3V3_S0_CPU_VCCIO_SEL
=PP3V3_S0_LCD
=PP3V3_S0_P3V3TBTFET
=PP3V3_S0_PCH
=PP3V3_S0_PCH_GPIO
=PP3V3_S0_PCH_VCC3_3_CLK
=PP3V3_S0_PCH_VCC3_3_GPIO
=PP3V3_S0_PCH_VCC3_3_HVCMOS
=PP3V3_S0_PCH_VCC3_3_PCI
=PP3V3_S0_PCH_VCC3_3_SATA
=PP3V3_S0_PCH_VCCADAC
=PP3V3_S0_PCH_VCC3_3
=PP3V3_S0_PWRCTL
=PP3V3_S0_RSTBUF
=PP3V3_S0_SATAMUX
=PP3V3_S0_SB_PM
=PP3V3_S0_SMBUS_PCH
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_1_S0
=PP3V3_S0_SSD
=PP3V3_S0_SYSCLK
=PP3V3_S0_TBTI2C
=PP3V3_S0_TBTPWRCTL
=PP3V3_S0_HDMI
=PP3V3_S0_TPAD
=PP3V3_S0_VMON
=PP3V3_S0_XDP
=PP3V3_S0_DDR3THMSNS
=PP3V3_S0_SPKRTHMSNS
=PP3V3_S0_HS_COMPUTING_ISNS
=PP3V3_S0_HS_OTHER_ISNS
=PP3V3_S0_PCH_STRAPS

1.8V/1.5V/1.2V/1.05V Rails

=PP1V8_S0_REG
2A max supply
PP1V8_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8R1V5_S0_PCH_VCCVRM
=PP1V8_S0_AUDIO
=PP1V8_S0_CPU_VCCPLL
=PP1V8_S0_PCH_VCC_DFTERM
=PPVDDIO_S0_SBCLK

=PP1V8_S0_CPU_VCCPLL_R
PP1V8_S0_CPU_VCCPLL_R
MIN_LINE_WIDTH=0.5 MM VOLTAGE=1.8V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

=PPDDR_S3_REG
PP1V5R1V35_S3
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.35V
MAKE_BASE=TRUE
=PPDDR_S3_MEMVREF
=PPVIN_S3_P1V5S3RS0_FET
=PPVIN_S0_DDRREG_LDO
=PPVIN_S3_MEM_ISNS_R

=PPVIN_S3_MEM_ISNS
PP1V5R1V35_MEM
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.35V
MAKE_BASE=TRUE
=PP1V5R1V35_S3_MEM_A
=PP1V5R1V35_S3_MEM_B
=PP1V5_S3_MEMRESET

=PP1V5_S3RS0_FET
PP1V5_S3RS0_CPUDDR
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3RS0_VMON
=PP1V5R1V35_S3_CPU_VCCDDR

=PP1V5_S0_REG
PP1V5_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_AUDIO
=PP3V3R1V5_S0_PCH_VCCSUSHDA
=PP1V5_S0_RDRVR

=PPVTT_S3_DDR_BUF
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.675V
MAKE_BASE=TRUE

=PPVTT_S0_DDR_LDO
PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.675V
MAKE_BASE=TRUE
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
=PPVTT_S0_VTTCLAMP

=PP1V05_SUS_LDO
PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_SUS_PCH_JTAG

=PPCPUVCCIO_S0_REG
PP1V05_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU_VCCIO
=PPVCCIO_S0_XDP
=PPVCCIO_S0_CPUIMVP
=PPVCCIO_S0_SMC
=PP1V05_S0_VMON
=PP1V05_S0_RMC
=PP1V05_S0_PCH_VCCIO_PLLPCIE
=PP1V05_S0_PCH_VCCADPLL
=PP1V05_S0_PCH_VCCIO
=PP1V05_S0_PCH_VCCIO_PCIE
=PP1V05_S0_PCH_VCCIO_SATA
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCIO_USB
=PP1V05_S0_PCH_VCC_CORE
=PP1V05_S0_PCH_VCCASW
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCDIFFCLK
=PP1V05_S0_PCH
=PP1V05_S0_PCH_VCCSSC
=PP1V05_S0_PCH_V_PROC_IO
=PP1V05_S0_PCH_VCCIO_PLLUSB
=PP1V05_S0_PCH_VCC_DMI
=PP1V05_S0_PCH_VCCIO_PLLFDI
=PP1V05_S0_PCH_VCCDMI_FDI

=PPBUS_G3H_T25
PPBUS_G3H_T25_PWR
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 MM VOLTAGE=12.8V

Backlight Rails

=PPBUS_SW_BKL
PPBUS_SW_BKL
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 MM VOLTAGE=12.6V
PPBUS_S0_LCDBKLT_PWR

=PP18V5_DCIN_ISOL
PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.3 MM VOLTAGE=18.5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPDCIN_S5_CHGR_ISOL
=PPDCIN_S5_VSENSE

TBT Rails (off when no cable)

=PPVIN_SW_TBTBST
PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

=PP15V_TBT_REG
PP15V_TBT
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=15V
MAKE_BASE=TRUE
=PPHV_SW_TBTAPWRSW
=PPHV_SW_TBTBPWRSW

=PP3V3_TBTLC_FET
PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_TBT_PCH_GPIO
=PP3V3_TBTLC_RTR
=PPVDDIO_TBT_CLK
=PP3V3_TBT_PCH_GPIO

=PP1V05_S0_P1V05TBTREG_R
PP1V05_S0_P1V05TBTREG_R
MIN_LINE_WIDTH=0.4 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

=PP1V05_S0_P1V05TBTREG
PP1V05_S0_P1V05TBTREG
MIN_LINE_WIDTH=0.4 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V05_TBTLC_RTR
=PP1V05_TBTLC

=PP1V05_TBTCIO_FET
PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_TBTCIO_RTR

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.25 MM VOLTAGE=1.25V
=PPVCORE_S0_CPU

=PPVCORE_S0_AXG_REG
PPVCORE_S0_AXG
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
=PPVCORE_S0_CPU_VCCAXG

=PP1V5_S3_CPU_VCCDQ
PP1V5_S3_CPU_VCCDQ
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V

=PP1V05_S0_CPU_VCCPQE
PP1V05_S0_CPU_VCCPQE
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

=PPVCCSA_S0_REG
PPVCCSA_S0_REG
MIN_LINE_WIDTH=0.6 MM VOLTAGE=0.9V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPVCCSA_S0_CPU

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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Power Aliases

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Frame Holes

ZT0940
4P5R2P3-3P5B

ZT0960
4P5R2P3-3P5B

Bosses for limiting deflection

SH0910
2.8OD1.2ID-2.25H-SM-D1
APN:860-1557

SH0911
2.8OD1.2ID-2.25H-SM-D1

SH0912
2.8OD1.2ID-2.25H-SM-D1

SH0913
2.8OD1.2ID-2.25H-SM-D1

SH0950
SM
SHLD-D1-USB

SH0951
SM
SHLD-D1-MLB-T29

D1 THERMAL MODULE STANDOFF (860-1439)

SH0920
STDOFF-4.50D2.15H-SM

SH0921
STDOFF-4.50D2.15H-SM

SH0926
STDOFF-4.50D2.15H-SM

SH0927
STDOFF-4.50D2.15H-SM

D1 BMU MODULE STANDOFFS

SH0928
STDOFF-4.50D1.73H-SM
APN: 860-1490

SH0963
STDOFF-4.50D2.33H-SM

SH0963 is BMU standoff with flange. 860-1534

TH0900 for upper TBT can gnd slot

TH0903 for lower TBT can gnd slot

TH0904,5 for USB can gnd slot

FAN BOSSES (4X 860-1327)

SH0922
STDOFF-4.50D1.8H-SM

SH0923
STDOFF-4.50D1.8H-SM

SH0924
STDOFF-4.50D1.8H-SM

SH0925
STDOFF-4.50D1.8H-SM

D1 POGO PINS (870-2451)

SH0932
POGO-2.30D-5.5H-SM-LOW-FORCE

SH0933
POGO-2.30D-4.1H-SM-LOW-FORCE

SH0934
POGO-2.30D-5.5H-SM-LOW-FORCE

SH0935
POGO-2.30D-5.5H-SM-LOW-FORCE

SH0936
POGO-2.30D-5.5H-SM-LOW-FORCE

SH0937
POGO-2.30D-5.5H-SM-LOW-FORCE

D1 ELIPTICAL SLOT HOLES

ZT0930
TH-NSP
SL-3.9X2.3-4.2x2.6

ZT0920
TH-NSP
SL-2.8X1.8-3.1x2.1

ZT0931
TH-NSP
SL-3.9X2.3-4.2x2.6

TH0900
TH-NSP
SL-1.1X0.5-1.4x0.8

TH0903
TH-NSP
SL-1.1X0.5-1.4x0.8
APN:862-0118

TH0904
TH-NSP
SL-1.1X0.45-1.4x0.75
APN:998-3975

TH0905
TH-NSP
SL-1.1X0.45-1.4x0.75

MLB_RAMCFG3
MLB_RAMCFG2
MLB_RAMCFG1
MLB_RAMCFG0
RAMCFG0:L R0910 1K 5% 1/20W MF 0201
RAMCFG1:L R0911 1K 5% 1/20W MF 0201
RAMCFG2:L R0912 1K 5% 1/20W MF 0201
RAMCFG3:L R0913 1K 5% 1/20W MF 0201

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Digital Ground

eDP signals

DP_INT_AUX_C_P — TP_EDP_AUX_P
DP_INT_AUX_C_N — TP_EDP_AUX_N
DP_INT_ML_C_P<3..0> — TP_EDP_TX_P<3..0>
DP_INT_ML_C_N<3..0> — TP_EDP_TX_N<3..0>

LCD_BKLT_PWM — LVDS_IG_BKL_PWM
LCD_BKLT_EN — LVDS_IG_BKL_ON
LCD_PWR_EN — LVDS_IG_PANEL_PWR

CR SFF DG v1p0 Table 3-56 mapping for HDMI

HDMI_IG_CLK_C_P — TP_DP_IG_B_MLP<3>
HDMI_IG_CLK_C_N — TP_DP_IG_B_MLN<3>
HDMI_IG_DATA_C_P<2..0> — TP_DP_IG_B_MLP<0..2>
HDMI_IG_DATA_C_N<2..0> — TP_DP_IG_B_MLN<0..2>
HDMI_IG_DDC_CLK — DPA_IG_DDC_CLK
HDMI_IG_DDC_DATA — DPA_IG_DDC_DATA
HDMI_HPD — DPA_IG_HPD

DP_TBTSNK0_AUXCH_C_P — DPB_IG_AUX_CH_P
DP_TBTSNK0_AUXCH_C_N — DPB_IG_AUX_CH_N
DP_TBTSNK0_ML_C_P<3..0> — TP_DP_IG_C_MLP<3..0>
DP_TBTSNK0_ML_C_N<3..0> — TP_DP_IG_C_MLN<3..0>
DP_TBTSNK0_DDC_CLK — DPB_IG_DDC_CLK
DP_TBTSNK0_DDC_DATA — DPB_IG_DDC_DATA
DP_TBTSNK0_HPD — DPB_IG_HPD

DP_TBTSNK1_AUXCH_C_P — TP_DP_IG_D_AUXP
DP_TBTSNK1_AUXCH_C_N — TP_DP_IG_D_AUXN
DP_TBTSNK1_ML_C_P<3..0> — TP_DP_IG_D_MLP<3..0>
DP_TBTSNK1_ML_C_N<3..0> — TP_DP_IG_D_MLN<3..0>
DP_TBTSNK1_DDC_CLK — TP_DP_IG_D_CTRL_CLK
DP_TBTSNK1_DDC_DATA — TP_DP_IG_D_CTRL_DATA
DP_TBTSNK1_HPD — TP_DP_IG_D_HPD

NC_PCH_GPIO64_CLKOUTFLEX0 — TP_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1 — TP_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2 — TP_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3 — TP_PCH_GPIO67_CLKOUTFLEX3

=PP5V_S0_AUDIO_XW
XW0902 SM PP5V_S0_AUDIO_AMP_L
XW0903 SM PP5V_S0_AUDIO_AMP_R
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

CPU signals

MEMVTT_EN — =DDRVTT_EN

T29 Signals Through PEG

PCIE_TBT_D2R_P<3..0> — =PEG_D2R_P<11..8>
PCIE_TBT_D2R_N<3..0> — =PEG_D2R_N<11..8>
PCIE_TBT_R2D_C_P<3..0> — =PEG_R2D_C_P<11..8>
PCIE_TBT_R2D_C_N<3..0> — =PEG_R2D_C_N<11..8>

SD_PWR_EN_PCH — ENET_LOW_PWR_PCH
SD_PWR_EN — ENET_LOW_PWR
TP_FW_PWR_EN — FW_PWR_EN

Unused PEG signals

NC_PEG_D2RP<15..12> — =PEG_D2R_P<15..12>
NC_PEG_D2RN<15..12> — =PEG_D2R_N<15..12>
NC_PEG_R2D_CP<15..12> — =PEG_R2D_C_P<15..12>
NC_PEG_R2D_CN<15..12> — =PEG_R2D_C_N<15..12>

Unused GPU signals

NC_PEG_D2RP<7..0> — =PEG_D2R_P<7..0>
NC_PEG_D2RN<7..0> — =PEG_D2R_N<7..0>
NC_PEG_R2D_CP<7..0> — =PEG_R2D_C_P<7..0>
NC_PEG_R2D_CN<7..0> — =PEG_R2D_C_N<7..0>

NC_DPA_IG_AUX_CHP — DPA_IG_AUX_CH_P
NC_DPA_IG_AUX_CHN — DPA_IG_AUX_CH_N

NC_PEG_CLK100MN — PEG_CLK100M_N
NC_PEG_CLK100MP — PEG_CLK100M_P

UNUSED USB SIGNALS

NC_USB3_EXTC_TXP — USB3_EXTC_TX_P
NC_USB3_EXTC_TXN — USB3_EXTC_TX_N
NC_USB3_EXTC_RXP — USB3_EXTC_RX_P
NC_USB3_EXTC_RXN — USB3_EXTC_RX_N
NC_USB_EXTCP — USB_EXTC_P
NC_USB_EXTCN — USB_EXTC_N
NC_USB3_EXTD_TXP — USB3_EXTD_TX_P
NC_USB3_EXTD_TXN — USB3_EXTD_TX_N
NC_USB3_EXTD_RXP — USB3_EXTD_RX_P
NC_USB3_EXTD_RXN — USB3_EXTD_RX_N
NC_USB_EXTD_EHCIP — USB_EXTD_EHCI_P
NC_USB_EXTD_EHCIN — USB_EXTD_EHCI_N
NC_USB_4N — TP_USB_4N
NC_USB_4P — TP_USB_4P
NC_USB_SDN — TP_USB_SDN
NC_USB_SDP — TP_USB_SDP
NC_USB_WLANN — TP_USB_WLANN
NC_USB_WLANP — TP_USB_WLANP
NC_USB_BT_HSN — TP_USB_BT_HSN
NC_USB_BT_HSP — TP_USB_BT_HSP
NC_USB_12N — TP_USB_12N
NC_USB_12P — TP_USB_12P
NC_USB_13N — TP_USB_13N
NC_USB_13P — TP_USB_13P

USB SIGNALS

USB_BT_P — USBHUB_DN1_P
USB_BT_N — USBHUB_DN1_N
USB_TPAD_P — USBHUB_DN2_P
USB_TPAD_N — USBHUB_DN2_N
USB_SMC_P — USBHUB_DN3_P
USB_SMC_N — USBHUB_DN3_N
PU_USBHUB_DN4_P — USBHUB_DN4_P
PU_USBHUB_DN4_N — USBHUB_DN4_N

NC_CPU_THERMDN — CPU_THERMD_N
NC_CPU_THERMDP — CPU_THERMD_P
NC_LCD_FSS — LCD_FSS

NC_PCIE_CLK100M_SSDN — PCIE_CLK100M_SSD_N
NC_PCIE_CLK100M_SSDP — PCIE_CLK100M_SSD_P
NC_PCIE_CLK100M_FWN — PCIE_CLK100M_FW_N
NC_PCIE_CLK100M_FWP — PCIE_CLK100M_FW_P

NC_PCIE_FW_D2RN — PCIE_FW_D2R_N
NC_PCIE_FW_D2RP — PCIE_FW_D2R_P
NC_PCIE_FW_R2D_CN — PCIE_FW_R2D_C_N
NC_PCIE_FW_R2D_CP — PCIE_FW_R2D_C_P

Unused SATA ODD Signals

NC_SATA_ODD_D2RN — SATA_ODD_D2R_N
NC_SATA_ODD_D2RP — SATA_ODD_D2R_P
NC_SATA_ODD_R2D_CN — SATA_ODD_R2D_C_N
NC_SATA_ODD_R2D_CP — SATA_ODD_R2D_C_P

Unused Memory Signals

NC_MEM_A_CLKP<1> — MEM_A_CLK_P<1>
NC_MEM_A_CLKN<1> — MEM_A_CLK_N<1>
NC_MEM_B_CLKP<1> — MEM_B_CLK_P<1>
NC_MEM_B_CLKN<1> — MEM_B_CLK_N<1>

=PP3V3_S0_PWRCTL
R0991 10K 5% 1/20W MF 0201
Unused PGOOD signal
CPUIMVP_AXG_PGOOD

TP_P1V5S3RS0_RAMP_DONE — P1V5S3RS0_RAMP_DONE
TP_DDRREG_PGOOD — DDRREG_PGOOD

SYNC_MASTER=D1_MLB_TEST	SYNC_DATE=01/27/2012
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NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.

OMIT_TABLE
CRITICAL

U1000
IVY-BRIDGE
2C-35W
BGA
(1 OF 9)

DMI_RX_0* M2
DMI_RX_1* P6
DMI_RX_2* P1
DMI_RX_3* P10
DMI_RX_0 N3
DMI_RX_1 P7
DMI_RX_2 P3
DMI_RX_3 P11
DMI_TX_0* K1
DMI_TX_1* M8
DMI_TX_2* N4
DMI_TX_3* R2
DMI_TX_0 K3
DMI_TX_1 M7
DMI_TX_2 P4
DMI_TX_3 T3

DMI

FDI_DATA_N<0> U7
FDI_DATA_N<1> W11
FDI_DATA_N<2> W1
FDI_DATA_N<3> AA6
FDI_DATA_N<4> W6
FDI_DATA_N<5> V4
FDI_DATA_N<6> Y2
FDI_DATA_N<7> AC9
FDI_DATA_P<0> U6
FDI_DATA_P<1> W10
FDI_DATA_P<2> W3
FDI_DATA_P<3> AA7
FDI_DATA_P<4> W7
FDI_DATA_P<5> T4
FDI_DATA_P<6> AA3
FDI_DATA_P<7> AC8
FDI_FSYNC<0> AA11
FDI_FSYNC<1> AC12
FDI_INT U11
FDI_LSYNC<0> AA10
FDI_LSYNC<1> AG8
CPU_EDP_COMP AD2
AF3

FDI0_TX_0* FDI0_TX_1* FDI0_TX_2* FDI0_TX_3*
FDI1_TX_0* FDI1_TX_1* FDI1_TX_2* FDI1_TX_3*
FDI0_TX_0 FDI0_TX_1 FDI0_TX_2 FDI0_TX_3
FDI1_TX_0 FDI1_TX_1 FDI1_TX_2 FDI1_TX_3
FDI0_FSYNC FDI1_FSYNC FDI_INT FDI0_LSYNC FDI1_LSYNC

INTEL FLEXIBLE DISPLAY INTERFACE SIGNALS

EDP_ICOMPO EDP_COMPIO EDP_HPD EDP_AUX* EDP_AUX EDP_TX_0* EDP_TX_1* EDP_TX_2* EDP_TX_3* EDP_TX_0 EDP_TX_1 EDP_TX_2 EDP_TX_3

EMBEDDED DISPLAY PORT

PCI EXPRESS BASED INTERFACE SIGNALS

=PP1V05_S0_CPU_VCCIO

R1030 24.9 1% 1/16W MF-LF 402 PLACE_NEAR=U1000.AF3:12.7MM

OMIT_TABLE
R1031 10K 1% 1/16W MF-LF 402 PLACE_NEAR=U1000.AG11:12.7MM

EDP_HPD_L

TP_EDP_AUX_N AG4
TP_EDP_AUX_P AF4
TP_EDP_TX_N<0> AC3
TP_EDP_TX_N<1> AC4
TP_EDP_TX_N<2> AE11
TP_EDP_TX_N<3> AE7
TP_EDP_TX_P<0> AC1
TP_EDP_TX_P<1> AA4
TP_EDP_TX_P<2> AE10
TP_EDP_TX_P<3> AE6

Q1031
DMN5L06TK
SOT523
SYM_VER_1

LCD_HPD

EDP:YES

PEG_ICOMPI G3
PEG_ICOMPO G1
PEG_RCOMPO G4

R1010 24.9 1% 1/16W MF-LF 402 PLACE_NEAR=U1000.G3:12.7MM
CPU_PEG_COMP =PP1V05_S0_CPU_VCCIO

PEG_RX_0* H22 =PEG_D2R_N<0>
PEG_RX_1* J21 =PEG_D2R_N<1>
PEG_RX_2* B22 =PEG_D2R_N<2>
PEG_RX_3* D21 =PEG_D2R_N<3>
PEG_RX_4* A19 =PEG_D2R_N<4>
PEG_RX_5* D17 =PEG_D2R_N<5>
PEG_RX_6* B14 =PEG_D2R_N<6>
PEG_RX_7* D13 =PEG_D2R_N<7>
PEG_RX_8* A11 =PEG_D2R_N<8>
PEG_RX_9* B10 =PEG_D2R_N<9>
PEG_RX_10* G8 =PEG_D2R_N<10>
PEG_RX_11* A8 =PEG_D2R_N<11>
PEG_RX_12* B6 =PEG_D2R_N<12>
PEG_RX_13* H8 =PEG_D2R_N<13>
PEG_RX_14* E5 =PEG_D2R_N<14>
PEG_RX_15* K7 =PEG_D2R_N<15>

PEG_RX_0 K22 =PEG_D2R_P<0>
PEG_RX_1 K19 =PEG_D2R_P<1>
PEG_RX_2 C21 =PEG_D2R_P<2>
PEG_RX_3 D19 =PEG_D2R_P<3>
PEG_RX_4 C19 =PEG_D2R_P<4>
PEG_RX_5 D16 =PEG_D2R_P<5>
PEG_RX_6 C13 =PEG_D2R_P<6>
PEG_RX_7 D12 =PEG_D2R_P<7>
PEG_RX_8 C11 =PEG_D2R_P<8>
PEG_RX_9 C9 =PEG_D2R_P<9>
PEG_RX_10 F8 =PEG_D2R_P<10>
PEG_RX_11 C8 =PEG_D2R_P<11>
PEG_RX_12 C5 =PEG_D2R_P<12>
PEG_RX_13 H6 =PEG_D2R_P<13>
PEG_RX_14 F6 =PEG_D2R_P<14>
PEG_RX_15 K6 =PEG_D2R_P<15>

PEG_TX_0* G22 =PEG_R2D_C_N<0>
PEG_TX_1* C23 =PEG_R2D_C_N<1>
PEG_TX_2* D23 =PEG_R2D_C_N<2>
PEG_TX_3* F21 =PEG_R2D_C_N<3>
PEG_TX_4* H19 =PEG_R2D_C_N<4>
PEG_TX_5* C17 =PEG_R2D_C_N<5>
PEG_TX_6* K15 =PEG_R2D_C_N<6>
PEG_TX_7* F17 =PEG_R2D_C_N<7>
PEG_TX_8* F14 =PEG_R2D_C_N<8>
PEG_TX_9* A15 =PEG_R2D_C_N<9>
PEG_TX_10* J14 =PEG_R2D_C_N<10>
PEG_TX_11* H13 =PEG_R2D_C_N<11>
PEG_TX_12* M10 =PEG_R2D_C_N<12>
PEG_TX_13* F10 =PEG_R2D_C_N<13>
PEG_TX_14* D9 =PEG_R2D_C_N<14>
PEG_TX_15* J4 =PEG_R2D_C_N<15>

PEG_TX_0 F22 =PEG_R2D_C_P<0>
PEG_TX_1 A23 =PEG_R2D_C_P<1>
PEG_TX_2 D24 =PEG_R2D_C_P<2>
PEG_TX_3 E21 =PEG_R2D_C_P<3>
PEG_TX_4 G19 =PEG_R2D_C_P<4>
PEG_TX_5 B18 =PEG_R2D_C_P<5>
PEG_TX_6 K17 =PEG_R2D_C_P<6>
PEG_TX_7 G17 =PEG_R2D_C_P<7>
PEG_TX_8 E14 =PEG_R2D_C_P<8>
PEG_TX_9 C15 =PEG_R2D_C_P<9>
PEG_TX_10 K13 =PEG_R2D_C_P<10>
PEG_TX_11 G13 =PEG_R2D_C_P<11>
PEG_TX_12 K10 =PEG_R2D_C_P<12>
PEG_TX_13 G10 =PEG_R2D_C_P<13>
PEG_TX_14 D8 =PEG_R2D_C_P<14>
PEG_TX_15 K4 =PEG_R2D_C_P<15>

PLACE_NEAR=U1000.H43:50.8MM
PLACE_SIDE=TOP
=PPVCORE_S0_CPU

=PPVCORE_S0_CPU_VCCAXG

R1064 49.9 1% 1/16W MF-LF 402 NOSTUFF
R1070 49.9 1% 1/16W MF-LF 402 NOSTUFF
PLACE_NEAR=U1000.H45:50.8MM
PLACE_SIDE=TOP

CPU_VCC_VALSENSE_P H43 VCC_VAL_SENSE
CPU_VCC_VALSENSE_N K43 VSS_VAL_SENSE
Note. VOLTAGE=1.25V
Note. VOLTAGE=0V

CPU_AXG_VALSENSE_P H45 VAXG_VAL_SENSE
CPU_AXG_VALSENSE_N K45 VSSAXG_VAL_SENSE
Note. VOLTAGE=1.05V
Note. VOLTAGE=0V

TP_CPU_VCC_DIE_SENSE F48 VCC_DIE_SENSE

R1065 49.9 1% 1/16W MF-LF 402 NOSTUFF
R1071 49.9 1% 1/16W MF-LF 402 NOSTUFF
PLACE_NEAR=U1000.K45:50.8MM
PLACE_SIDE=TOP

CPU_THERMD_P H48 RSVD_6
CPU_THERMD_N K48 RSVD_7

NOTE: Intel does not recommend to use this alnalog sense due to accuracy concern.

PLACE_NEAR=U1000.K43:50.8MM
PLACE_SIDE=TOP

NOTE: Intel validation sense lines per doc 439028 rev1.0 HR_PPDG sections 6.2.1 and 6.3.1.

CPU_CFG<0> B50 CFG_0
CPU_CFG<1> C51 CFG_1
CPU_CFG<2> B54 CFG_2
CPU_CFG<3> D53 CFG_3
CPU_CFG<4> A51 CFG_4
CPU_CFG<5> C53 CFG_5
CPU_CFG<6> C55 CFG_6
CPU_CFG<7> H49 CFG_7
CPU_CFG<8> A55 CFG_8
CPU_CFG<9> H51 CFG_9
CPU_CFG<10> K49 CFG_10
CPU_CFG<11> K53 CFG_11
CPU_CFG<12> F53 CFG_12
CPU_CFG<13> G53 CFG_13
CPU_CFG<14> L51 CFG_14
CPU_CFG<15> F51 CFG_15
CPU_CFG<16> D52 CFG_16
CPU_CFG<17> L53 CFG_17

OMIT_TABLE
CRITICAL

U1000
BGA
(5 OF 9)
RESERVED
IVY-BRIDGE
2C-35W

MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V

SA_DIMM_VREFDQ BE7 PPCPU_MEM_VREFDQ_A
SB_DIMM_VREFDQ BG7 PPCPU_MEM_VREFDQ_B

RSVD_30 N42 NC
RSVD_31 L42 NC
RSVD_32 L43 NC
RSVD_33 L44 NC
RSVD_34 M13 NC
RSVD_35 M14 NC
RSVD_36 U13 NC
RSVD_37 W13 NC
RSVD_38 P13 NC
RSVD_39 AT49 NC
RSVD_40 K20 NC
RSVD_41 AH2 NC
RSVD_42 AG13 NC
RSVD_43 AM13 NC
RSVD_44 AM14 NC
RSVD_45 N50 NC

RSVD_23 BE22
RSVD_24 BG26
RSVD_25 BE26
RSVD_26 BE23
RSVD_27 BE24

DC_TEST_A4 A4 TP_CPU_DC_TEST_A4
DC_TEST_C4 C4 CPU_DC_TEST_C4_D3
DC_TEST_D3 D3
DC_TEST_D1 D1 TP_CPU_DC_TEST_D1
DC_TEST_A58 A58 TP_CPU_DC_TEST_A58
DC_TEST_A59 A59 CPU_DC_TEST_C59_A59
DC_TEST_C59 C59
DC_TEST_A61 A61 CPU_DC_TEST_C61_A61
DC_TEST_C61 C61
DC_TEST_D61 D61 TP_CPU_DC_TEST_D61
DC_TEST_BD61 BD61 TP_CPU_DC_TEST_BD61
DC_TEST_BE61 BE61 CPU_DC_TEST_BE59_BE61
DC_TEST_BE59 BE59
DC_TEST_BG61 BG61 CPU_DC_TEST_BG59_BG61
DC_TEST_BG59 BG59
DC_TEST_BG58 BG58 TP_CPU_DC_TEST_BG58
DC_TEST_BG4 BG4 TP_CPU_DC_TEST_BG4
DC_TEST_BG3 BG3 CPU_DC_TEST_C4_BE3_BG3
DC_TEST_BE3 BE3
DC_TEST_BG1 BG1 CPU_DC_TEST_C4_BE1_BG1
DC_TEST_BE1 BE1
DC_TEST_BD1 BD1 TP_CPU_DC_TEST_BD1

CPU_CFG<7> CPU_CFG<6> CPU_CFG<5> CPU_CFG<4> CPU_CFG<2>

R1042 1K NOSTUFF
R1044 1K EDP:YES
R1045 1K
R1046 1K NOSTUFF
R1047 1K NOSTUFF

CPU_CFG<16> CPU_CFG<3> CPU_CFG<1> CPU_CFG<0>

R1040 1K NOSTUFF
R1041 1K NOSTUFF
R1043 1K NOSTUFF
R1049 1K NOSTUFF

These can be Placed close to J2500 and Only for debug access

FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0066	1	RES,MTL FILM,1/16W,1K,0402,SMD,LF	R1031		EDP:YES
116S0090	1	RES,MTL FILM,1/16W,10K,0402,SMD,LF	R1031		EDP:NO

Intel Doc 460452 ChiefRiver Platform design guild rev1.0 section 2.2.12 recommendation.

NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active High signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kohm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2011

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

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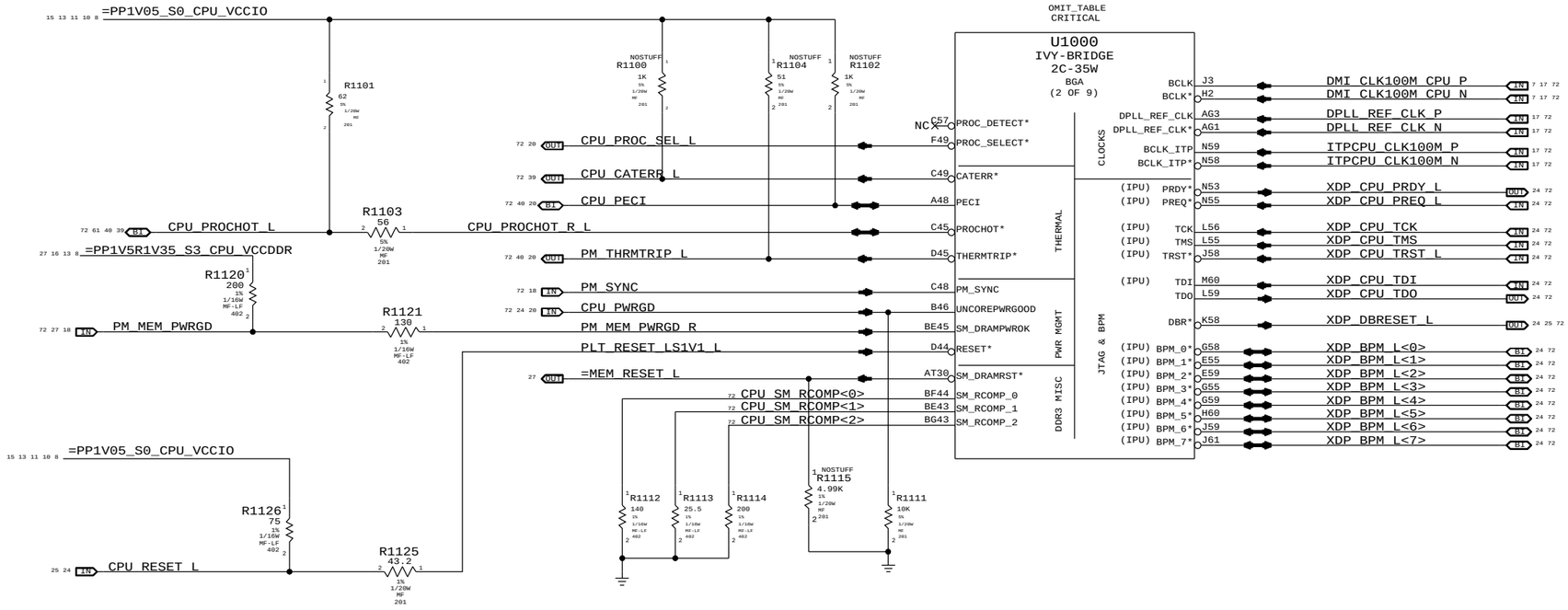

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PAGE TITLE

CPU CLOCK/MISC/JTAG

Apple Inc.

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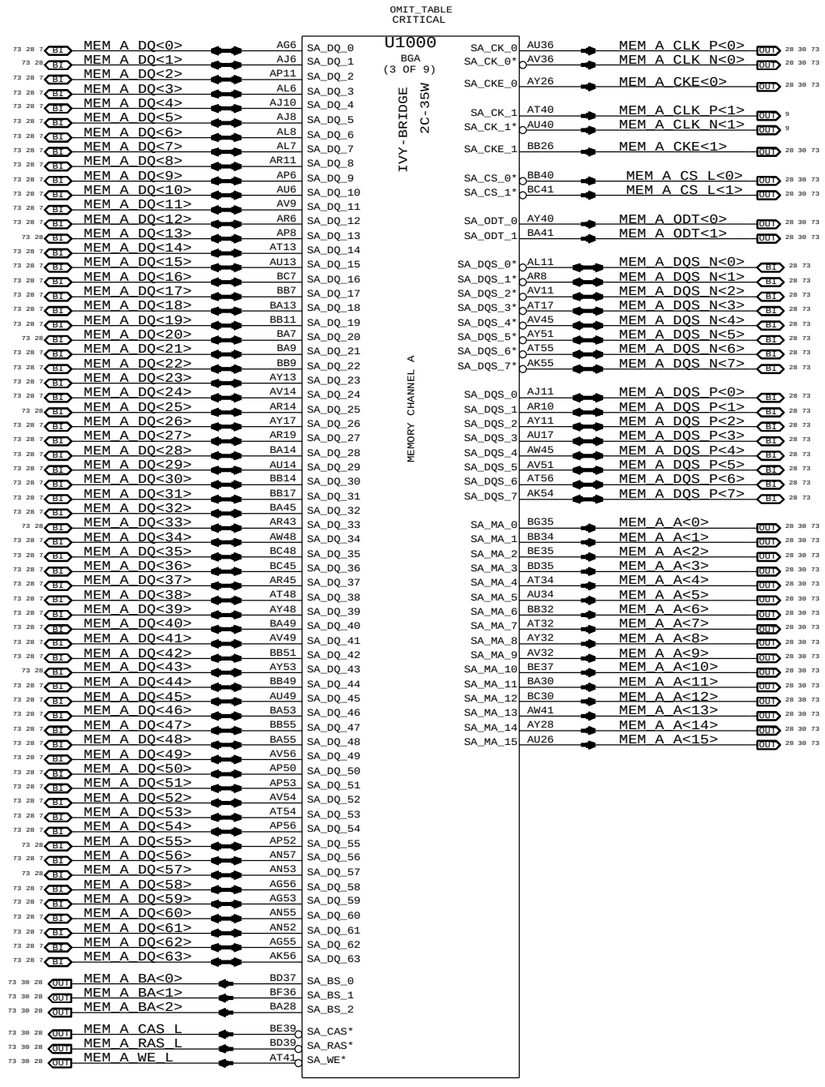

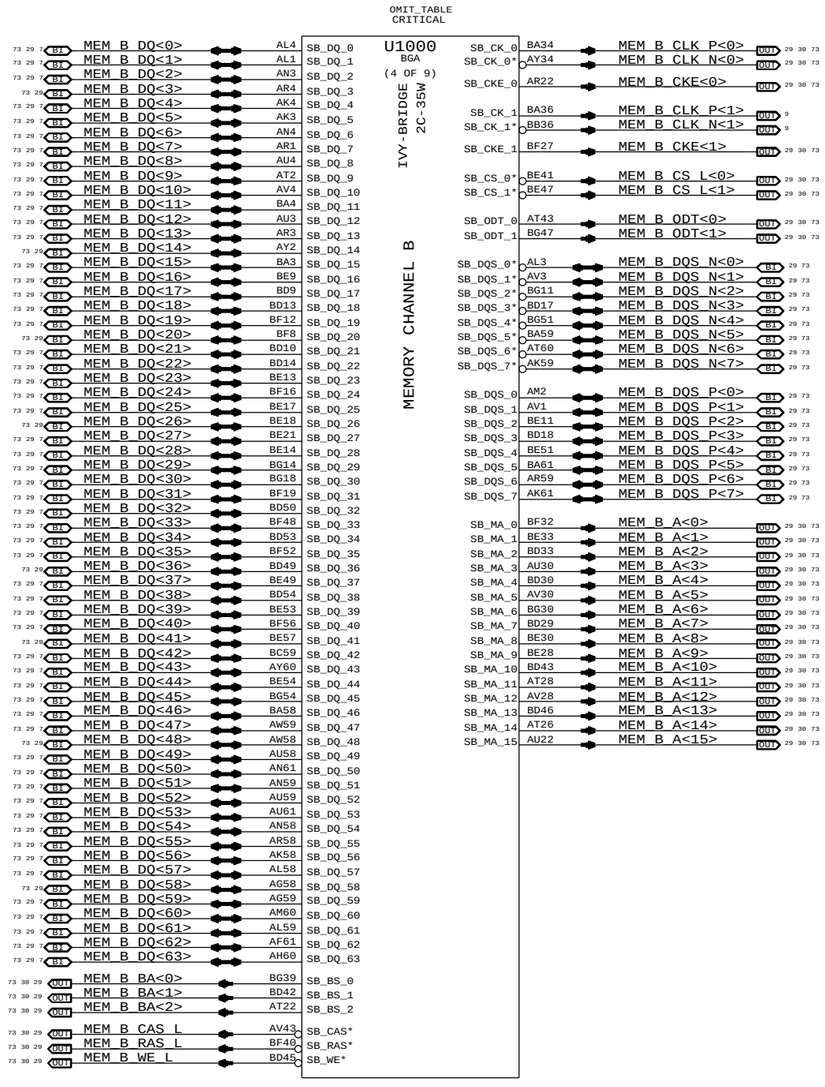

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PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

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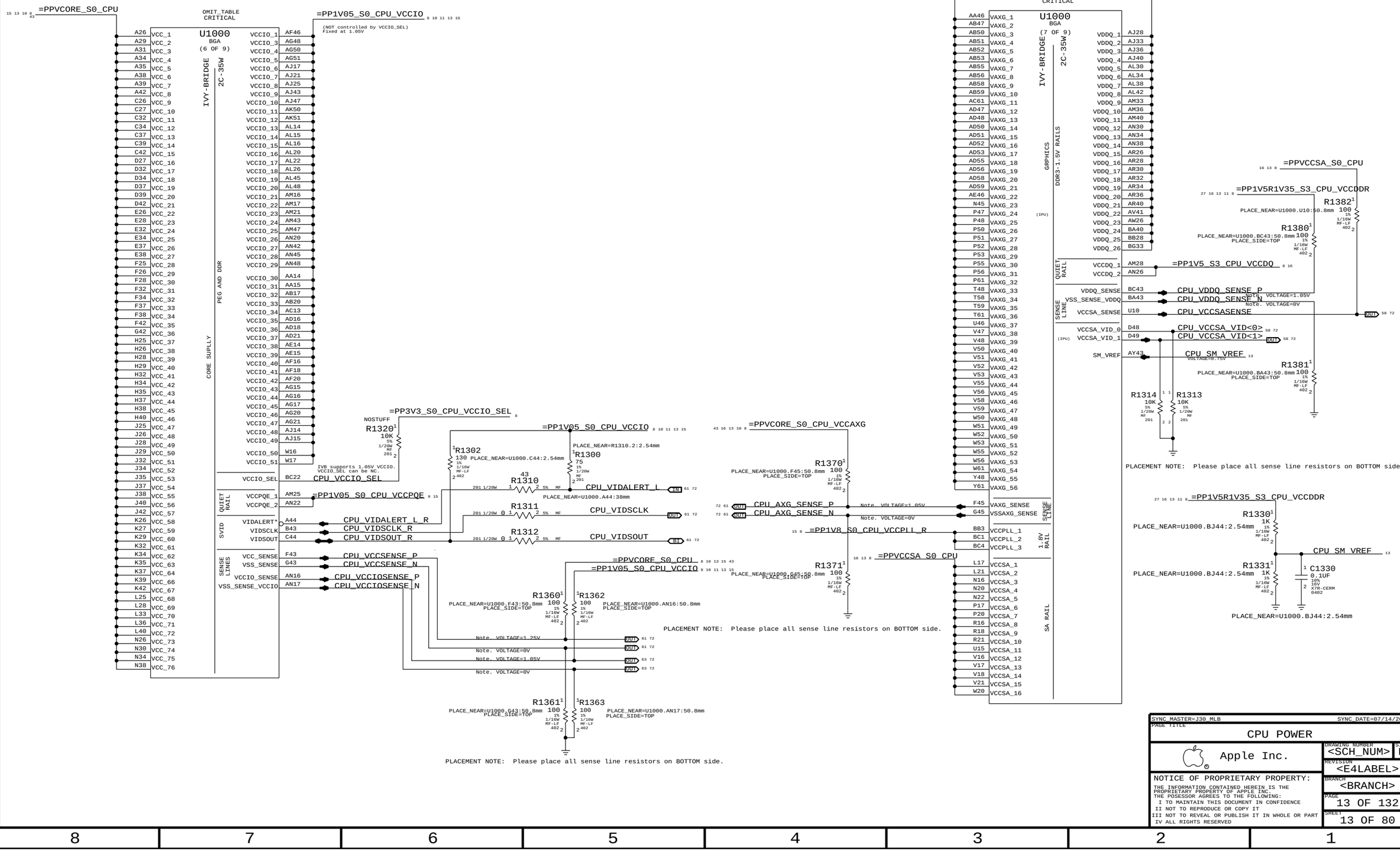

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Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
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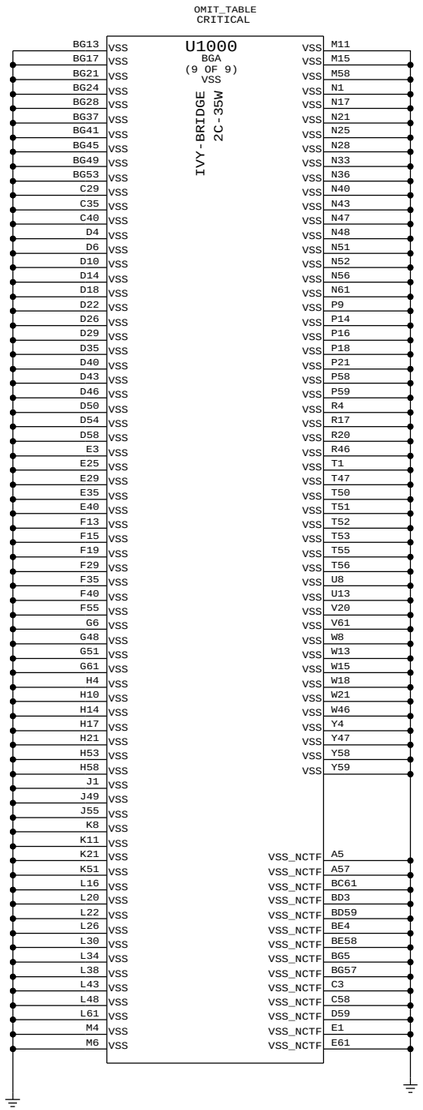

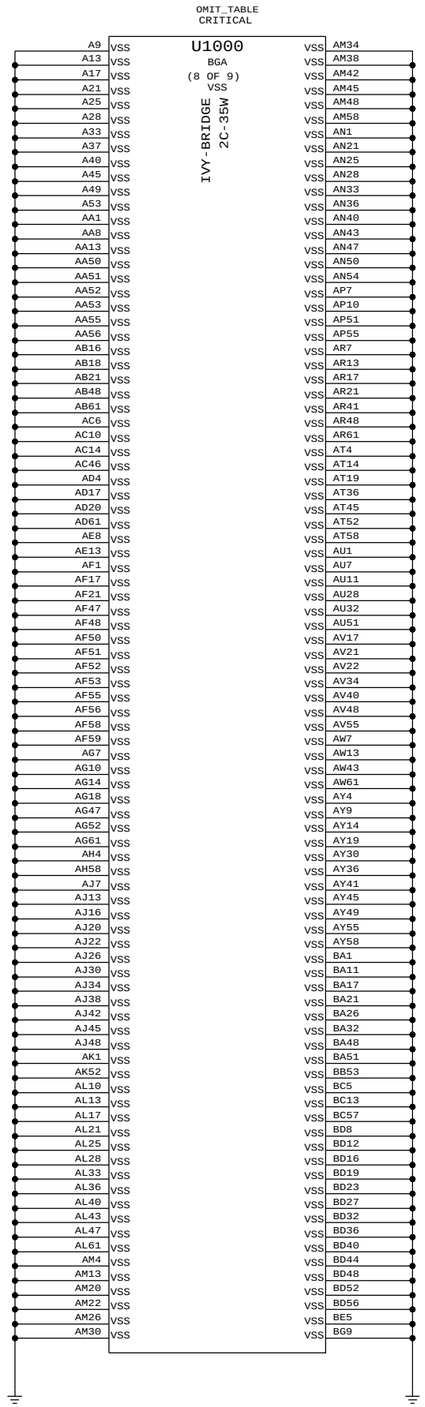

SYNC MASTER=J30_MLB SYNC DATE=07/14/2013

PAGE TITLE

CPU GROUNDS

Apple Inc.

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All INTEL recommendations from Intel doc #458544 Chief River Platform Power Design Guide v0p9

CPU VCORE DECOUPLING

Intel recommendation (Table 7-2): Option 2: 35x 2.2uF, 12x 22uF, 4x 470uF, or Option 3: 35x 2.2uF, 6x 22uF, 6x 330 uF

43 13 10 8 =PPVCORE_S0_CPU

CRITICAL: C1600 C1604 C1606 C1607 C1608 C1609 C1610 C1612 C1613 C1615 C1617 C1623 C1624
CRITICAL: C1625 C1627 C1628 C1631 C1632 C1635 C1637 C1638 C1639 C1640 C1641 C1642 C1643 C1644 C1645 C1647 C1648
CRITICAL: C1650 C1651 C1652 C1653 C1654

2.2UF 20% 6.3V CERM 402-2

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

CRITICAL: C1646 C168F C16A0
CRITICAL: C1655 C1656 C1657 C1658 C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C166A C166B C166C C166D C166E C166F C165A C165B C1667 C1674

20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1667-C1679):
Place close to U1000 on bottom side.

CRITICAL: C16A1 C16A2 C16A3
CRITICAL: C1675 C1668 C1669 C1670 C1671 C1672 C1673 C1649 C164A C1676 C1677 C1678 C1679 C165C C165D C165E C165F C164E C164B C164C C164D C164F

20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

C1680 C1681 C1682 C1683: 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C168D: 270UF 20% 2V TANT CASE-B2-SM
C168E: 270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Table 7-7): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

13 11 10 8 =PP1V05_S0_CPU_VCCIO

C1684 C1685 C1686 C1687 C1688 C1689 C1690 C1691 C1692 C1693 C1694 C1695 C1696
C1697 C1698 C1699 C169A C169B C169C C169D C169E C169F C161A C161B C161C C161D

1UF 10% 10V X5R-CERM 0402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C161E C161F C162A C162B C162C C162D C162E C167A C167B C167C

10UF 20% 6.3V CERM-X5R 0402-1

C167D C167E C168A C168B: 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603 — =PP1V05_S0_CPU_VCCPQE — 8 13

C167F: 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (table 7-5): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

8 =PP1V8_S0_CPU_VCCPLL — R1600 0 5% 1/10W MF-LF 402 — =PP1V8_S0_CPU_VCCPLL_R — 8 13

PLACE_NEAR=U1000.AK61:5mm PLACE_NEAR=U1000.AK61:5mm
PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA
PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

C160X C160Y: 1UF 10% 10V X5R 402
C160Z: 270UF 20% 2V TANT CASE-B2-SM
C168C: 270UF 20% 2V TANT CASE-B2-SM

CPU VCCPLL Low pass filter

SYNC_MASTER=MASTER SYNC_DATE=MASTER
PAGE TITLE: CPU DECOUPLING-I

Apple Inc.

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VAXG DECOUPLING

Intel recommendation (Table 7-4) for GT2 3.9mOhm LL: 11x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

43 13 10 8 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL C1700 1UF 10% 10V X5R-CERM 0402
CRITICAL C1701 1UF 10% 10V X5R-CERM 0402
CRITICAL C1702 1UF 10% 10V X5R-CERM 0402
CRITICAL C1703 1UF 10% 10V X5R-CERM 0402
CRITICAL C1704 1UF 10% 10V X5R-CERM 0402
CRITICAL C1705 1UF 10% 10V X5R-CERM 0402
CRITICAL C1706 1UF 10% 10V X5R-CERM 0402
CRITICAL C1707 1UF 10% 10V X5R-CERM 0402
CRITICAL C1708 1UF 10% 10V X5R-CERM 0402
CRITICAL C1709 1UF 10% 10V X5R-CERM 0402
CRITICAL C1710 1UF 10% 10V X5R-CERM 0402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL C1711 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1712 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1713 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1714 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1715 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL C1717 20UF 20% 2V X6T-CERM 0402
CRITICAL C1718 20UF 20% 2V X6T-CERM 0402
CRITICAL C1719 20UF 20% 2V X6T-CERM 0402
CRITICAL C1720 20UF 20% 2V X6T-CERM 0402
CRITICAL C1721 20UF 20% 2V X6T-CERM 0402
CRITICAL C1722 20UF 20% 2V X6T-CERM 0402
NO STUFF C1725 20UF 20% 2V X6T-CERM 0402
NO STUFF C1726 20UF 20% 2V X6T-CERM 0402
NO STUFF C1727 20UF 20% 2V X6T-CERM 0402
NO STUFF C1728 20UF 20% 2V X6T-CERM 0402
NO STUFF C1729 20UF 20% 2V X6T-CERM 0402
NO STUFF C172A 20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1723-C1724):

Place near inductors on bottom side.

C1723 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C1724 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Table 7-11): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

27 13 11 8 =PP1V5R1V35_S3_CPU_VCCDDR

Place on bottom side of U1000

C1738 1UF 10% 10V X5R-CERM 0402
C1739 1UF 10% 10V X5R-CERM 0402
C1740 1UF 10% 10V X5R-CERM 0402
C1741 1UF 10% 10V X5R-CERM 0402
C1742 1UF 10% 10V X5R-CERM 0402
C1743 1UF 10% 10V X5R-CERM 0402
C1744 1UF 10% 10V X5R-CERM 0402
C1745 1UF 10% 10V X5R-CERM 0402
C1746 1UF 10% 10V X5R-CERM 0402
C1747 1UF 10% 10V X5R-CERM 0402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V CERM-X5R 0402-1
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V CERM-X5R 0402-1
C1755 10UF 20% 6.3V CERM-X5R 0402-1

C1756 270UF 20% 2V TANT CASE-B2-SM
C1770 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W MF 0603

=PP1V5_S3_CPU_VCCDQ 8 13

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Table 7-9): 5x 1uf, 5x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

13 8 =PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 1UF 10% 10V X5R-CERM 0402
C1759 1UF 10% 10V X5R-CERM 0402
C1760 1UF 10% 10V X5R-CERM 0402
C1761 1UF 10% 10V X5R-CERM 0402
C1762 1UF 10% 10V X5R-CERM 0402

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

C1768 270UF 20% 2V TANT CASE-B2-SM
C1769 270UF 20% 2V TANT CASE-B2-SM

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: CPU DECOUPLING-II

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DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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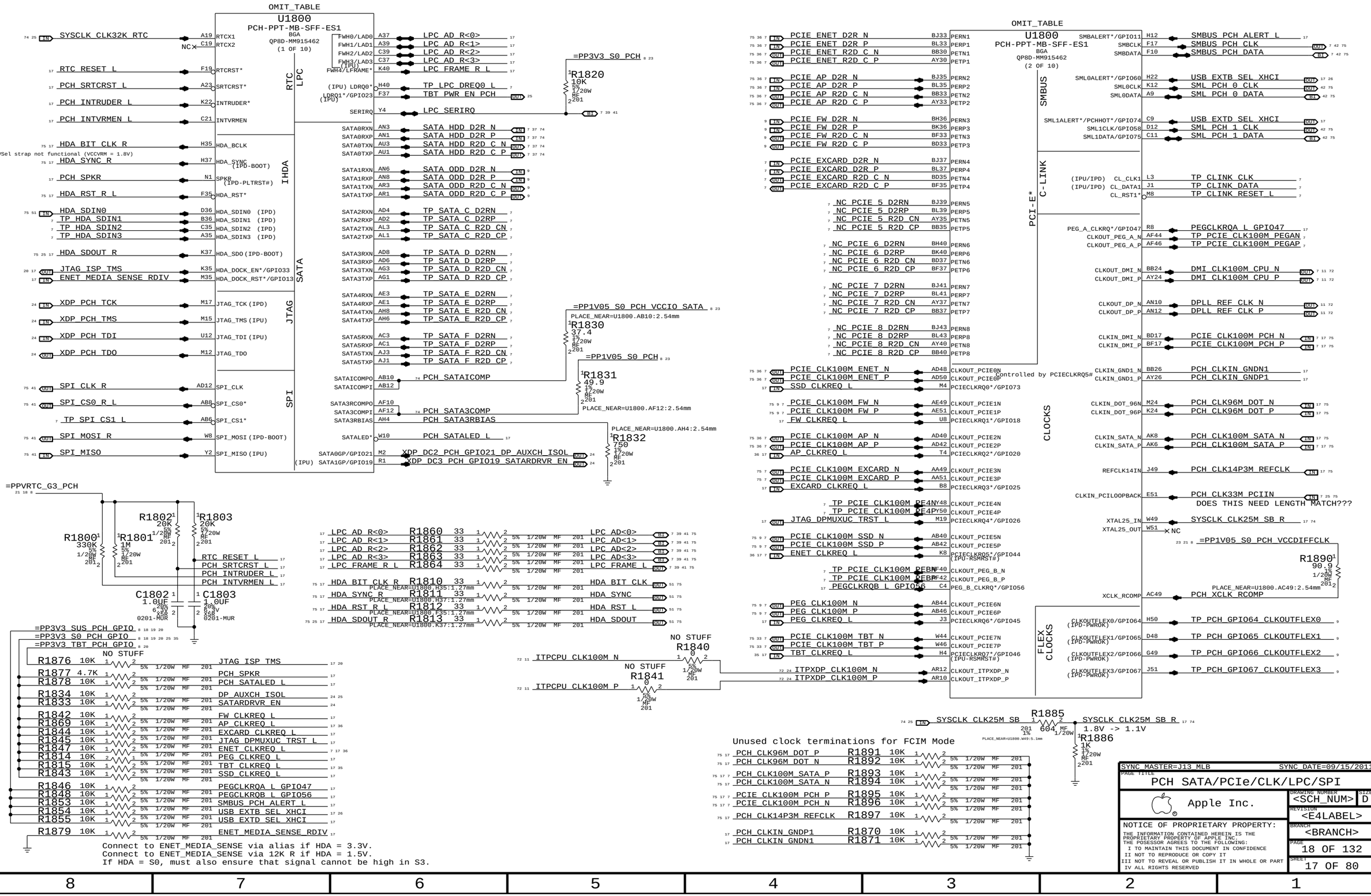
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(1 OF 10)
RTC
LPC
IHDA
SATA
JTAG
SPI
SYSCLK CLK32K RTC
RTC RESET L
PCH SRTCRST L
PCH INTRUDER L
PCH INTVRMEN L
HDA BIT CLK R
HDA SYNC R
PCH SPKR
HDA RST R L
HDA SDIN0
TP HDA SDIN1
TP HDA SDIN2
TP HDA SDIN3
HDA SDOUT R
JTAG ISP TMS
ENET MEDIA SENSE RDIV
XDP PCH TCK
XDP PCH TMS
XDP PCH TDI
XDP PCH TDO
SPI CLK R
SPI CS0 R L
TP SPI CS1 L
SPI MOSI R
SPI MISO
LPC AD R<0>
LPC AD R<1>
LPC AD R<2>
LPC AD R<3>
LPC FRAME R L
TP LPC DREQ0 L
TBT PWR EN PCH
LPC SERIRQ
=PP3V3 S0 PCH
SATA HDD D2R N
SATA HDD D2R P
SATA HDD R2D C N
SATA HDD R2D C P
SATA ODD D2R N
SATA ODD D2R P
SATA ODD R2D C N
SATA ODD R2D C P
TP SATA C D2RN
TP SATA C D2RP
TP SATA C R2D CN
TP SATA C R2D CP
TP SATA D D2RN
TP SATA D D2RP
TP SATA D R2D CN
TP SATA D R2D CP
TP SATA E D2RN
TP SATA E D2RP
TP SATA E R2D CN
TP SATA E R2D CP
TP SATA F D2RN
TP SATA F D2RP
TP SATA F R2D CN
TP SATA F R2D CP
=PP1V05 S0 PCH VCCIO SATA
PLACE_NEAR=U1800.AB10:2.54mm
R1830 37.4 1% 1/20W MF 201
=PP1V05 S0 PCH
R1831 49.9 1% 1/20W MF 201
PCH SATAICOMP
PCH SATA3COMP
PCH SATA3RBIAS
PLACE_NEAR=U1800.AF12:2.54mm
PLACE_NEAR=U1800.AH4:2.54mm
R1832 750 1% 1/20W MF 201
PCH SATALED L
XDP DC2 PCH GPIO21 DP AUXCH ISOL
XDP DC3 PCH GPIO19 SATARDRVR EN
=PPVRTC_G3_PCH
R1800 330K 5% 1/20W MF 201
R1801 1M 5% 1/20W MF 201
R1802 20K 5% 1/20W MF 201
R1803 20K 5% 1/20W MF 201
C1802 1.0UF 20% 6.3V X5R 0201-MUR
C1803 1.0UF 20% 6.3V X5R 0201-MUR
RTC RESET L
PCH SRTCRST L
PCH INTRUDER L
PCH INTVRMEN L
R1860 33 5% 1/20W MF 201
R1861 33 5% 1/20W MF 201
R1862 33 5% 1/20W MF 201
R1863 33 5% 1/20W MF 201
R1864 33 5% 1/20W MF 201
R1810 33 5% 1/20W MF 201
PLACE_NEAR=U1800.H35:1.27mm
R1811 33 5% 1/20W MF 201
PLACE_NEAR=U1800.H37:1.27mm
R1812 33 5% 1/20W MF 201
PLACE_NEAR=U1800.F35:1.27mm
R1813 33 5% 1/20W MF 201
PLACE_NEAR=U1800.K37:1.27mm
HDA BIT CLK
HDA SYNC
HDA RST L
HDA SDOUT
=PP3V3 SUS PCH GPIO
=PP3V3 S0 PCH GPIO
=PP3V3 TBT PCH GPIO
NO STUFF
R1876 10K JTAG ISP TMS
R1877 4.7K PCH SPKR
R1878 10K PCH SATALED L
R1834 10K DP AUXCH ISOL
R1833 10K SATARDRVR EN
R1842 10K FW CLKREQ L
R1869 10K AP CLKREQ L
R1844 10K EXCARD CLKREQ L
R1845 10K JTAG DPMUXUC TRST L
R1847 10K ENET CLKREQ L
R1814 10K PEG CLKREQ L
R1815 10K TBT CLKREQ L
R1843 10K SSD CLKREQ L
R1846 10K PEGCLKRQA L GPIO47
R1848 10K PEGCLKRQB L GPIO56
R1853 10K SMBUS PCH ALERT L
R1854 10K USB EXTB SEL XHCI
R1855 10K USB EXTD SEL XHCI
R1879 10K ENET MEDIA SENSE RDIV
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
ITPCPU CLK100M N
ITPCPU CLK100M P
NO STUFF
R1840 0 5% 1/20W MF 201
NO STUFF
R1841 0 5% 1/20W MF 201
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(2 OF 10)
SMBUS
C-LINK
PCI-E*
CLOCKS
FLEX CLOCKS
PCIE ENET D2R N
PCIE ENET D2R P
PCIE ENET R2D C N
PCIE ENET R2D C P
PCIE AP D2R N
PCIE AP D2R P
PCIE AP R2D C N
PCIE AP R2D C P
PCIE FW D2R N
PCIE FW D2R P
PCIE FW R2D C N
PCIE FW R2D C P
PCIE EXCARD D2R N
PCIE EXCARD D2R P
PCIE EXCARD R2D C N
PCIE EXCARD R2D C P
NC PCIE 5 D2RN
NC PCIE 5 D2RP
NC PCIE 5 R2D CN
NC PCIE 5 R2D CP
NC PCIE 6 D2RN
NC PCIE 6 D2RP
NC PCIE 6 R2D CN
NC PCIE 6 R2D CP
NC PCIE 7 D2RN
NC PCIE 7 D2RP
NC PCIE 7 R2D CN
NC PCIE 7 R2D CP
NC PCIE 8 D2RN
NC PCIE 8 D2RP
NC PCIE 8 R2D CN
NC PCIE 8 R2D CP
PCIE CLK100M ENET N
PCIE CLK100M ENET P
SSD CLKREQ L
PCIE CLK100M FW N
PCIE CLK100M FW P
FW CLKREQ L
PCIE CLK100M AP N
PCIE CLK100M AP P
AP CLKREQ L
PCIE CLK100M EXCARD N
PCIE CLK100M EXCARD P
EXCARD CLKREQ L
TP PCIE CLK100M PE4N
TP PCIE CLK100M PE4P
JTAG DPMUXUC TRST L
PCIE CLK100M SSD N
PCIE CLK100M SSD P
ENET CLKREQ L
TP PCIE CLK100M PE8N
TP PCIE CLK100M PE8P
PEGCLKRQB L GPIO56
PEG CLK100M N
PEG CLK100M P
PEG CLKREQ L
PCIE CLK100M TBT N
PCIE CLK100M TBT P
TBT CLKREQ L
ITPXDP CLK100M N
ITPXDP CLK100M P
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
(IPU/IPD) CL_CLK1
(IPU/IPD) CL_DATA1
CL_RST1*
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64 (IPD-PWROK)
CLKOUTFLEX1/GPIO65 (IPD-PWROK)
CLKOUTFLEX2/GPIO66 (IPD-PWROK)
CLKOUTFLEX3/GPIO67 (IPD-PWROK)
SMBUS PCH ALERT L
SMBUS PCH CLK
SMBUS PCH DATA
USB EXTB SEL XHCI
SML PCH 0 CLK
SML PCH 0 DATA
USB EXTD SEL XHCI
SML PCH 1 CLK
SML PCH 1 DATA
TP CLINK CLK
TP CLINK DATA
TP CLINK RESET L
PEGCLKRQA L GPIO47
TP PCIE CLK100M PEGAN
TP PCIE CLK100M PEGAP
DMI CLK100M CPU N
DMI CLK100M CPU P
DPLL REF CLK N
DPLL REF CLK P
PCIE CLK100M PCH N
PCIE CLK100M PCH P
PCH CLKIN GNDN1
PCH CLKIN GNDP1
PCH CLK96M DOT N
PCH CLK96M DOT P
PCH CLK100M SATA N
PCH CLK100M SATA P
PCH CLK14P3M REFCLK
PCH CLK33M PCIIN
DOES THIS NEED LENGTH MATCH???
SYSCLK CLK25M SB R
=PP1V05 S0 PCH VCCDIFFCLK
R1890 90.9 1% 1/20W MF 201
PLACE_NEAR=U1800.AC49:2.54mm
PCH XCLK RCOMP
TP PCH GPIO64 CLKOUTFLEX0
TP PCH GPIO65 CLKOUTFLEX1
TP PCH GPIO66 CLKOUTFLEX2
TP PCH GPIO67 CLKOUTFLEX3
CLKOUT_PCIE0N
CLKOUT_PCIE0P
PCIECLKRQ0*/GPIO73
controlled by PCIECLKRQ5#
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1*/GPIO18
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3*/GPIO25
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4*/GPIO26
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ*/GPIO56
CLKOUT_PCIE6N
CLKOUT_PCIE6P
PCIECLKRQ6*/GPIO45
CLKOUT_PCIE7N
CLKOUT_PCIE7P
PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
SYSCLK CLK25M SB
R1885 604 1% 1/20W MF 201
PLACE_NEAR=U1800.W49:5.1mm
SYSCLK CLK25M SB R
1.8V -> 1.1V
R1886 1K 1% 1/20W MF 201
Unused clock terminations for FCIM Mode
R1891 10K PCH CLK96M DOT P
R1892 10K PCH CLK96M DOT N
R1893 10K PCH CLK100M SATA P
R1894 10K PCH CLK100M SATA N
R1895 10K PCIE CLK100M PCH P
R1896 10K PCIE CLK100M PCH N
R1897 10K PCH CLK14P3M REFCLK
R1870 10K PCH CLKIN GNDP1
R1871 10K PCH CLKIN GNDN1
SYNC_MASTER=J13_MLB
SYNC_DATE=09/15/2011
PAGE TITLE
PCH SATA/PCIe/CLK/LPC/SPI
Apple Inc.
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SIZE D
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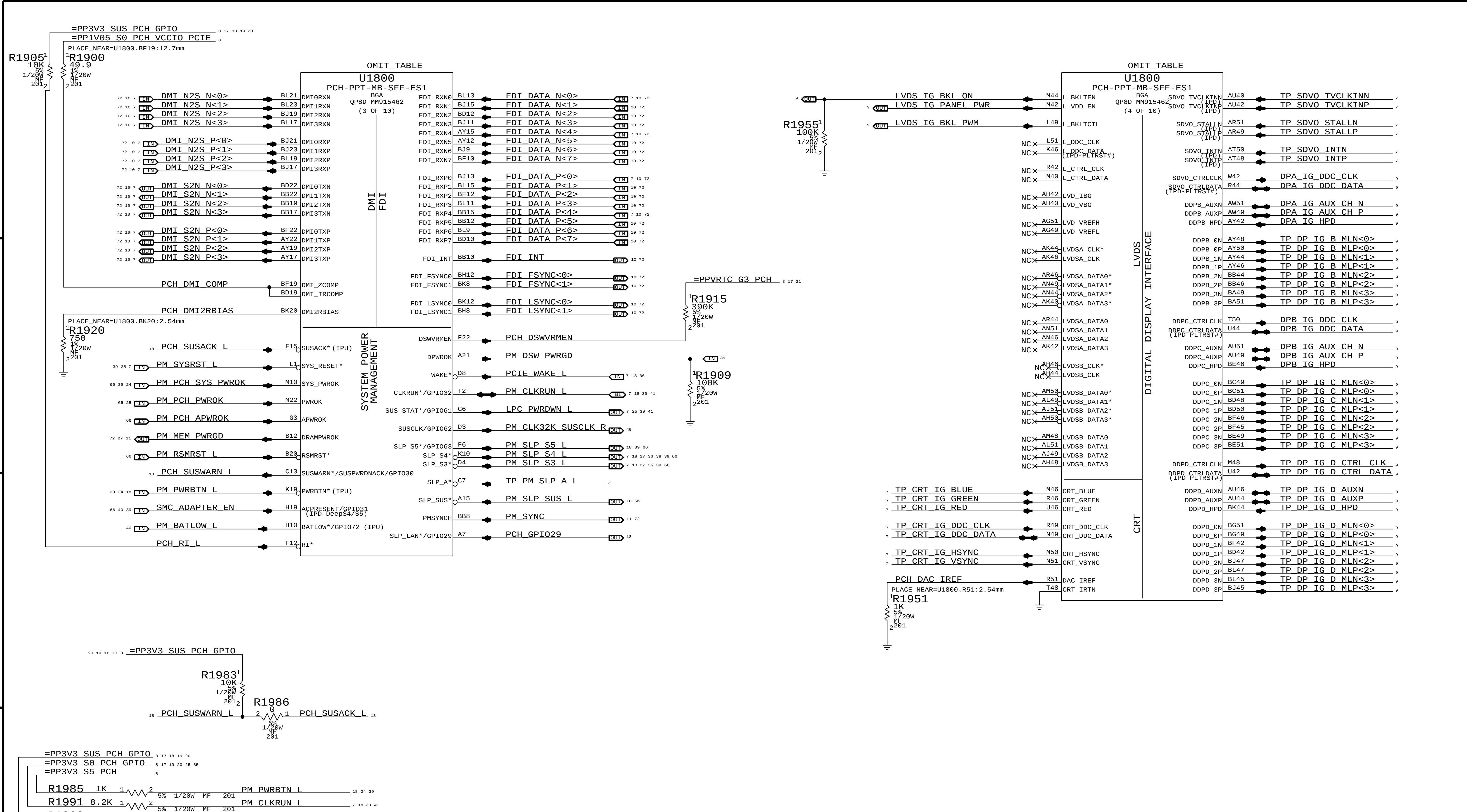

=PP3V3_SUS_PCH_GPIO
=PP1V05_S0_PCH_VCCIO_PCIE
PLACE_NEAR=U1800.BF19:12.7mm
R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
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DMI_N2S_N<0>
DMI_N2S_N<1>
DMI_N2S_N<2>
DMI_N2S_N<3>
DMI_N2S_P<0>
DMI_N2S_P<1>
DMI_N2S_P<2>
DMI_N2S_P<3>
DMI_S2N_N<0>
DMI_S2N_N<1>
DMI_S2N_N<2>
DMI_S2N_N<3>
DMI_S2N_P<0>
DMI_S2N_P<1>
DMI_S2N_P<2>
DMI_S2N_P<3>
PCH_DMI_COMP
PCH_DMI2RBIAS
PLACE_NEAR=U1800.BK20:2.54mm
R1920 750 1% 1/20W MF 201
DMI
FDI
FDI_DATA_N<0>
FDI_DATA_N<1>
FDI_DATA_N<2>
FDI_DATA_N<3>
FDI_DATA_N<4>
FDI_DATA_N<5>
FDI_DATA_N<6>
FDI_DATA_N<7>
FDI_DATA_P<0>
FDI_DATA_P<1>
FDI_DATA_P<2>
FDI_DATA_P<3>
FDI_DATA_P<4>
FDI_DATA_P<5>
FDI_DATA_P<6>
FDI_DATA_P<7>
FDI_INT
FDI_FSYNC<0>
FDI_FSYNC<1>
FDI_LSYNC<0>
FDI_LSYNC<1>
=PPVRTC_G3_PCH
R1915 390K 5% 1/20W MF 201
SYSTEM POWER MANAGEMENT
PCH_SUSACK_L
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PM_PCH_APWROK
PM_MEM_PWRGD
PM_RSMRST_L
PCH_SUSWARN_L
PM_PWRBTN_L
SMC_ADAPTER_EN
PM_BATLOW_L
PCH_RI_L
PCH_DSWVRMEN
PM_DSW_PWRGD
R1909 100K 5% 1/20W MF 201
PCIE_WAKE_L
PM_CLKRUN_L
LPC_PWRDWN_L
PM_CLK32K_SUSCLK_R
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PM_SLP_A_L
PM_SLP_SUS_L
PM_SYNC
PCH_GPIO29
R1983 10K 5% 1/20W MF 201
R1986 0 5% 1/20W MF 201
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
=PP3V3_S5_PCH
R1985 1K 5% 1/20W MF 201 PM_PWRBTN_L
R1991 8.2K 5% 1/20W MF 201 PM_CLKRUN_L
R1982 10K 5% 1/20W MF 201 PCH_GPIO29
R1925 1K 5% 1/20W MF 201 PCIE_WAKE_L
R1924 100K 5% 1/20W MF 201 PM_SLP_S3_L
R1921 100K 5% 1/20W MF 201 PM_SLP_S4_L
R1922 100K 5% 1/20W MF 201 PM_SLP_S5_L
R1923 100K 5% 1/20W MF 201 PM_SLP_SUS_L
LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR
LVDS_IG_BKL_PWM
R1955 100K 5% 1/20W MF 201
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
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LVDS
DIGITAL DISPLAY INTERFACE
CRT
TP_CRT_IG_BLUE
TP_CRT_IG_GREEN
TP_CRT_IG_RED
TP_CRT_IG_DDC_CLK
TP_CRT_IG_DDC_DATA
TP_CRT_IG_HSYNC
TP_CRT_IG_VSYNC
PCH_DAC_IREF
PLACE_NEAR=U1800.R51:2.54mm
R1951 1K 5% 1/20W MF 201
TP_SDVO_TVCLKINN
TP_SDVO_TVCLKINP
TP_SDVO_STALLN
TP_SDVO_STALLP
TP_SDVO_INTN
TP_SDVO_INTP
DPA_IG_DDC_CLK
DPA_IG_DDC_DATA
DPA_IG_AUX_CH_N
DPA_IG_AUX_CH_P
DPA_IG_HPD
TP_DP_IG_B_MLN<0>
TP_DP_IG_B_MLP<0>
TP_DP_IG_B_MLN<1>
TP_DP_IG_B_MLP<1>
TP_DP_IG_B_MLN<2>
TP_DP_IG_B_MLP<2>
TP_DP_IG_B_MLN<3>
TP_DP_IG_B_MLP<3>
DPB_IG_DDC_CLK
DPB_IG_DDC_DATA
DPB_IG_AUX_CH_N
DPB_IG_AUX_CH_P
DPB_IG_HPD
TP_DP_IG_C_MLN<0>
TP_DP_IG_C_MLP<0>
TP_DP_IG_C_MLN<1>
TP_DP_IG_C_MLP<1>
TP_DP_IG_C_MLN<2>
TP_DP_IG_C_MLP<2>
TP_DP_IG_C_MLN<3>
TP_DP_IG_C_MLP<3>
TP_DP_IG_D_CTRL_CLK
TP_DP_IG_D_CTRL_DATA
TP_DP_IG_D_AUXN
TP_DP_IG_D_AUXP
TP_DP_IG_D_HPD
TP_DP_IG_D_MLN<0>
TP_DP_IG_D_MLP<0>
TP_DP_IG_D_MLN<1>
TP_DP_IG_D_MLP<1>
TP_DP_IG_D_MLN<2>
TP_DP_IG_D_MLP<2>
TP_DP_IG_D_MLN<3>
TP_DP_IG_D_MLP<3>

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PAGE TITLE

PCH DMI/FDI/PM/Graphics

Apple Inc.

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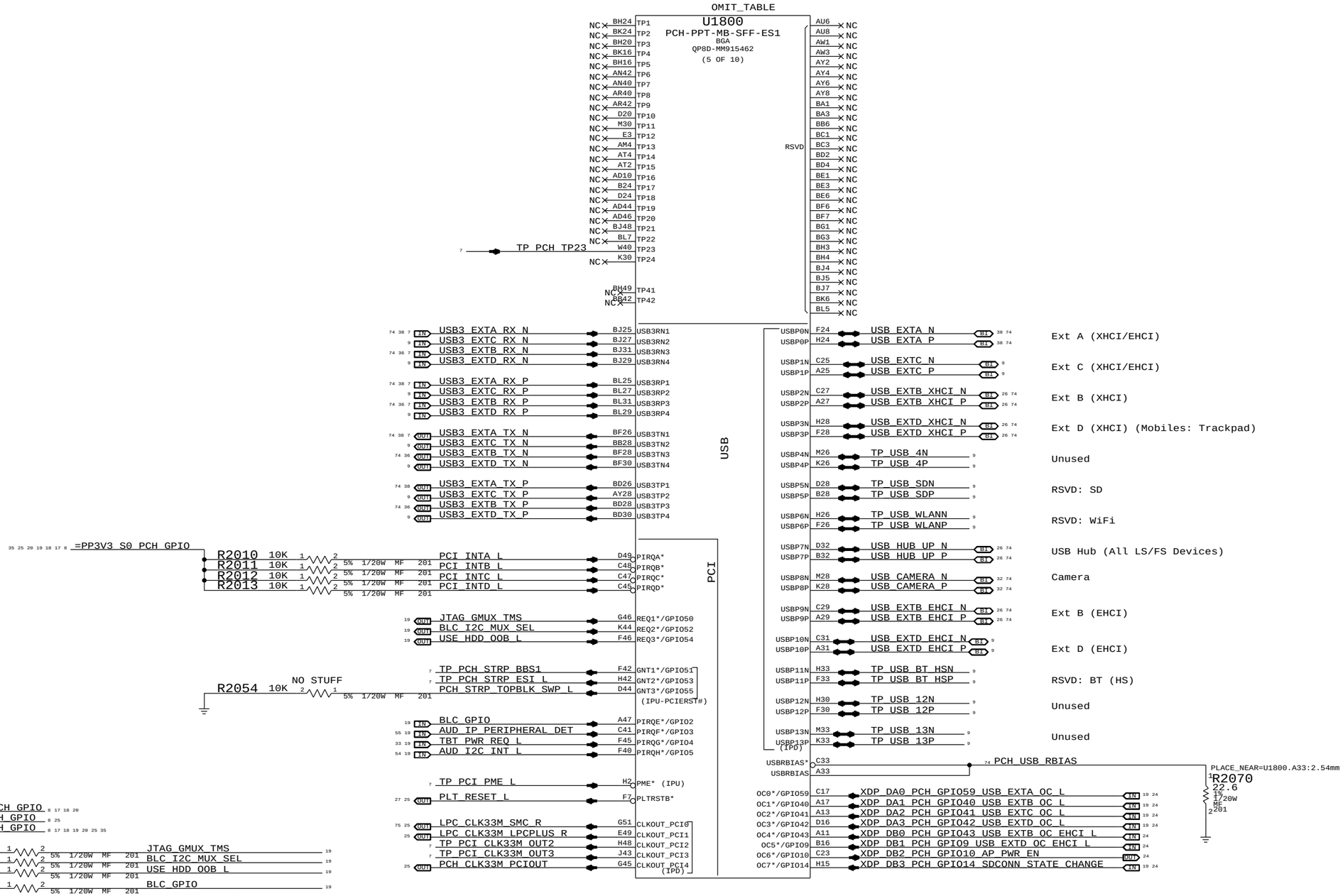

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PAGE TITLE	PCH PCI/USB/TP/RSVD
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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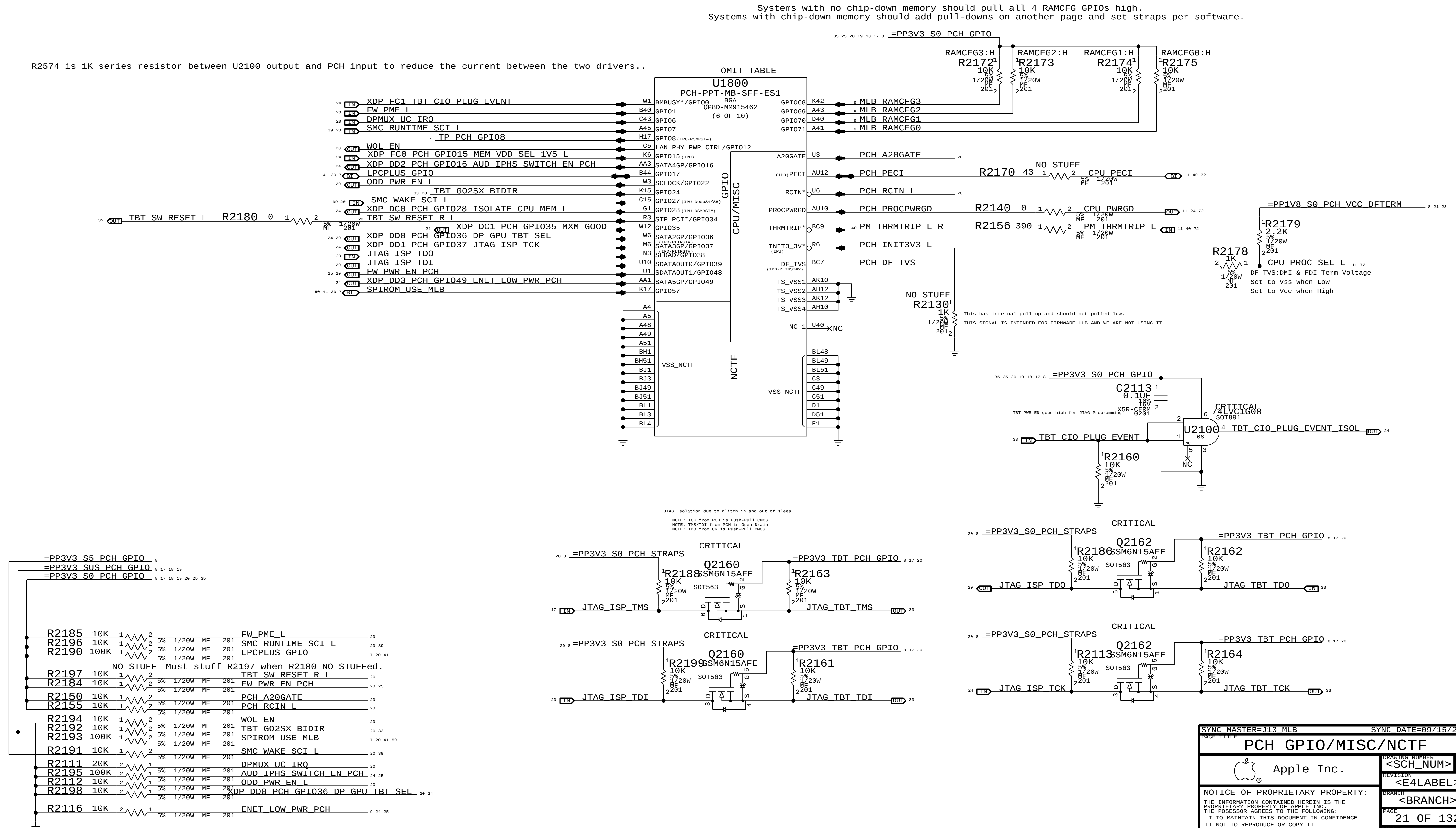
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H



Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.
R2574 is 1K series resistor between U2100 output and PCH input to reduce the current between the two drivers..
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(6 OF 10)
GPIO
CPU/MISC
NCTF
VSS_NCTF
=PP3V3_S0_PCH_GPIO
RAMCFG3:H R2172 10K
RAMCFG2:H R2173 10K
RAMCFG1:H R2174 10K
RAMCFG0:H R2175 10K
MLB_RAMCFG3
MLB_RAMCFG2
MLB_RAMCFG1
MLB_RAMCFG0
XDP_FC1_TBT_CIO_PLUG_EVENT
FW_PME_L
DPMUX_UC_IRQ
SMC_RUNTIME_SCI_L
TP_PCH_GPIO8
WOL_EN
XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
LPCPLUS_GPIO
ODD_PWR_EN_L
TBT_GO2SX_BIDIR
SMC_WAKE_SCI_L
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L
TBT_SW_RESET_R_L
XDP_DC1_PCH_GPIO35_MXM_GOOD
XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK
JTAG_ISP_TDO
JTAG_ISP_TDI
FW_PWR_EN_PCH
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH
SPIROM_USE_MLB
TBT_SW_RESET_L R2180 0
PCH_A20GATE
PCH_PECI
NO STUFF R2170 43 CPU_PECI
PCH_RCIN_L
PCH_PROCPWRGD R2140 0 CPU_PWRGD
PM_THRMTRIP_L_R R2156 390 PM_THRMTRIP_L
PCH_INIT3V3_L
PCH_DF_TVS
NO STUFF R2130 1K
This has internal pull up and should not pulled low.
THIS SIGNAL IS INTENDED FOR FIRMWARE HUB AND WE ARE NOT USING IT.
=PP1V8_S0_PCH_VCC_DFTERM
R2179 2.2K
R2178 1K
CPU_PROC_SEL_L
DF_TVS:DMI & FDI Term Voltage
Set to Vss when Low
Set to Vcc when High
=PP3V3_S0_PCH_GPIO
C2113 0.1UF
CRITICAL
74LVC1G08
SOT891
U2100
TBT_PWR_EN goes high for JTAG Programming
TBT_CIO_PLUG_EVENT
TBT_CIO_PLUG_EVENT_ISOL
R2160 10K
JTAG Isolation due to glitch in and out of sleep
NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TMS/TDI from PCH is Open Drain
NOTE: TDO from CR is Push-Pull CMOS
CRITICAL
=PP3V3_S0_PCH_STRAPS
=PP3V3_TBT_PCH_GPIO
Q2160 SSM6N15AFE SOT563
R2188 10K
R2163 10K
JTAG_ISP_TMS
JTAG_TBT_TMS
R2199 10K
R2161 10K
JTAG_ISP_TDI
JTAG_TBT_TDI
Q2162 SSM6N15AFE SOT563
R2186 10K
R2162 10K
JTAG_ISP_TDO
JTAG_TBT_TDO
R2113 10K
R2164 10K
JTAG_ISP_TCK
JTAG_TBT_TCK
=PP3V3_S5_PCH_GPIO
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
R2185 10K FW_PME_L
R2196 10K SMC_RUNTIME_SCI_L
R2190 100K LPCPLUS_GPIO
NO STUFF Must stuff R2197 when R2180 NO STUFFed.
R2197 10K TBT_SW_RESET_R_L
R2184 10K FW_PWR_EN_PCH
R2150 10K PCH_A20GATE
R2155 10K PCH_RCIN_L
R2194 10K WOL_EN
R2192 10K TBT_GO2SX_BIDIR
R2193 100K SPIROM_USE_MLB
R2191 10K SMC_WAKE_SCI_L
R2111 20K DPMUX_UC_IRQ
R2195 100K AUD_IPHS_SWITCH_EN_PCH
R2112 10K ODD_PWR_EN_L
R2198 10K XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
R2116 10K ENET_LOW_PWR_PCH

SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE

PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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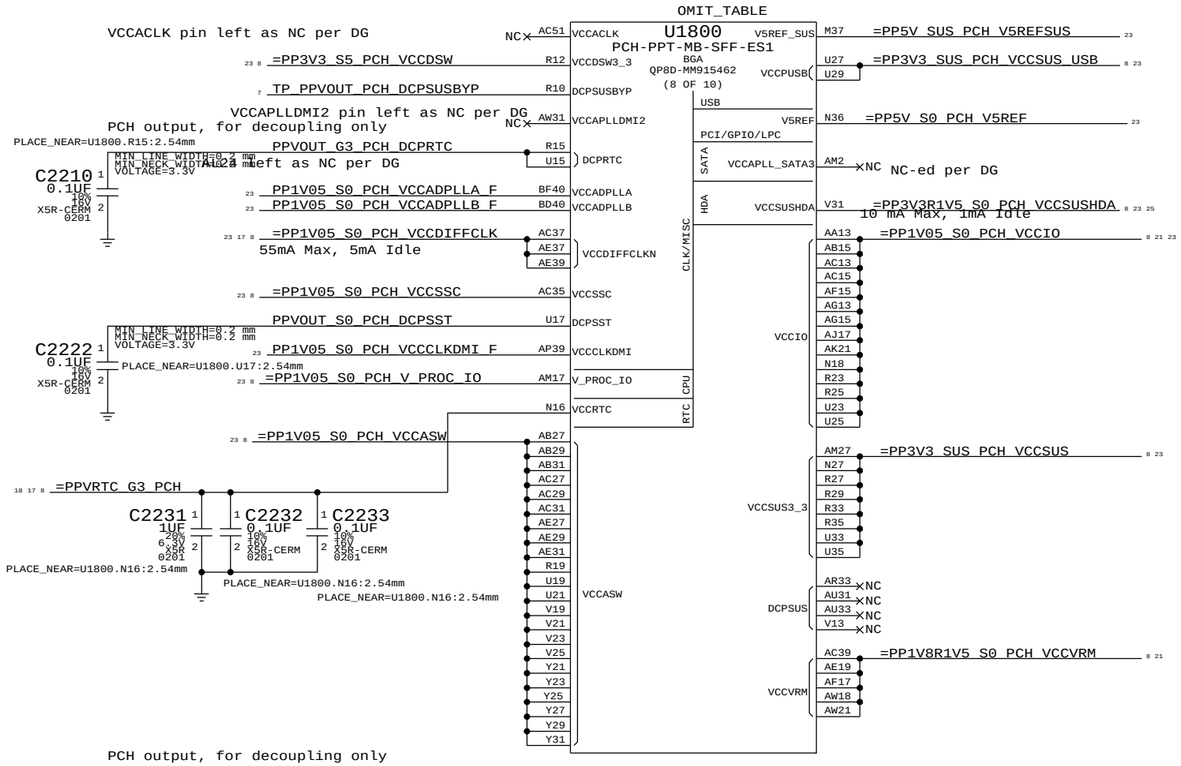

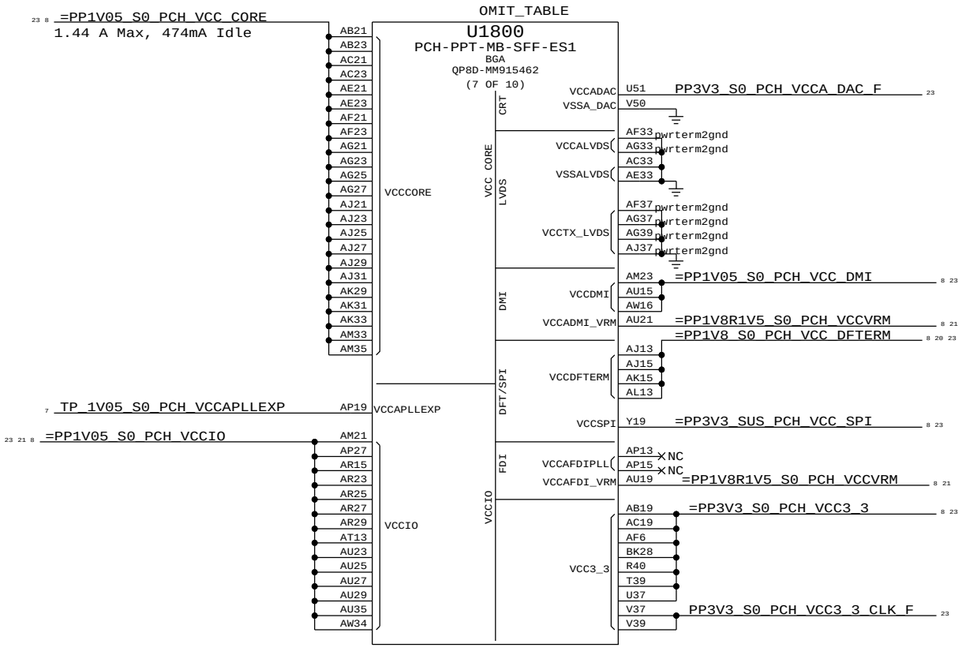

SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE: PCH POWER

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(9 OF 10)

AA7			AP2
AA9			AP4
AA11			AP7
AA39			AP9
AA41			AP11
AA43			AP17
AA45			AP21
AB2			AP23
AB4			AP25
AB17			AP29
AB25			AP31
AB33			AP33
AB35			AP35
AB37			AP37
AB48			AP41
AB50			AP43
AC7			AP45
AC9			AP48
AC11			AP50
AC17			AR6
AC25			AR8
AC41			AR17
AC43			AR19
AC45			AR21
AE7			AR31
AE9			AR35
AE11			AR37
AE13			AT7
AE15			AT9
AE17			AT11
AE25			AT39
AE35			AT41
AE41			AT43
AE43			AT45
AE45			AU17
AF2			AU37
AF4			AV2
AF8			AV4
AF19			AV48
AF25			AV50
AF27			AW7
AF29	VSS	VSS	AW9
AF31			AW11
AF35			AW13
AF48			AW23
AF50			AW25
AG7			AW27
AG9			AW29
AG11			AW36
AG17			AW39
AG19			AW41
AG29			AW43
AG31			AW45
AG35			AY10
AG41			B6
AG43			B10
AG45			B14
AH2			B18
AJ7			B22
AJ9			B26
AJ11			B30
AJ19			B34
AJ33			B38
AJ35			B42
AJ39			B46
AJ41			BA7
AJ43			BA9
AJ45			BA11
AK2			BA13
AK4			BA16
AK17			BA18
AK19			BA21
AK23			BA23
AK25			BA25
AK27			BA27
AK35			BA29
AK37			BA31
AK48			BA34
AK50			BA36
AL7			BA39
AL9			BA41
AL11			BA43
AL39			BA45
AL41			BB2
AL43			BB4
AL45			BB48
AM15			BB50
AM19			BC11
AM25			BC13
AM29			BC16
AM31			BC18
AM37			BC21

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(10 OF 10)

BC23			G39
BC25			G41
BC27			G43
BC29			J7
BC31			J9
BC34			J11
BC36			J13
BC39			J16
BC41			J18
BC43			J21
BC45			J23
BD15			J25
BD24			J27
BE7			J29
BE9			J31
BE11			J34
BE13			J36
BE16			J39
BE18			J41
BE21			J45
BE23			K2
BE25			K4
BE27			K48
BE29			K50
BE31			L7
BE34			L9
BE36			L11
BE39			L13
BE41			L16
BE43			L18
BE45			L21
BF2			L23
BF4			L25
BF15			L27
BF24			L29
BF48			L31
BF50			L34
BH6			L36
BH10			L39
BH14	VSS	VSS	L41
BH18			L43
BH22			L45
BH26			N7
BH28			N9
BH30			N11
BH32			N13
BH34			N21
BH38			N23
BH42			N25
BH44			N29
BH46			N31
BH48			N34
BK10			N39
BK14			N41
BK18			N43
BK22			N45
BK26			P2
BK30			P4
BK32			P48
BK34			P50
BK38			R17
BK42			R21
BK46			R31
D6			R37
D10			T7
D14			T9
D18			T11
D22			T13
D26			T41
D30			T43
D34			T45
D38			U31
D42			U49
D46			V2
F2			V4
F4			V7
F48			V9
F50			V11
G7			V15
G9			V17
G11			V27
G13			V29
G16			V33
G18			V35
G21			V41
G23			V43
G25			V45
G27			V48
G29			Y15
G31			Y17
G34			Y33
G36			Y35
			Y37

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Apple Inc.

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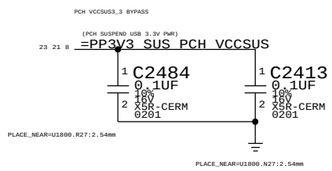

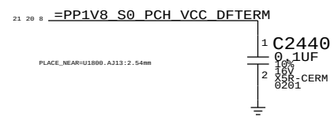

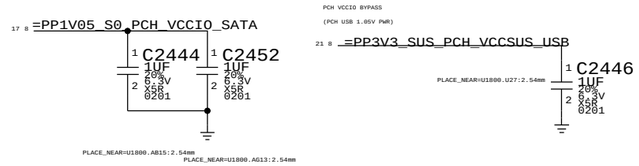

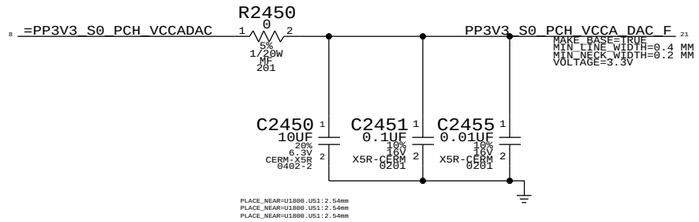

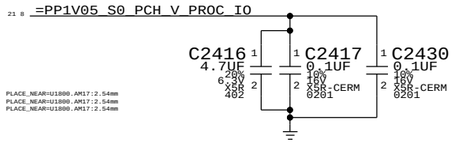

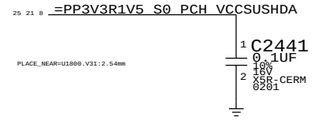

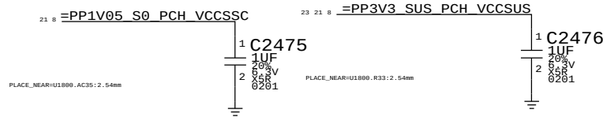

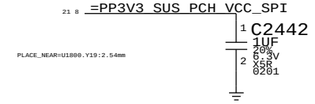

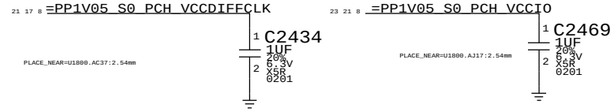

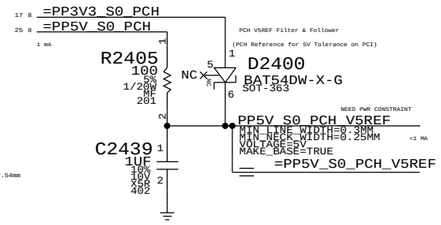

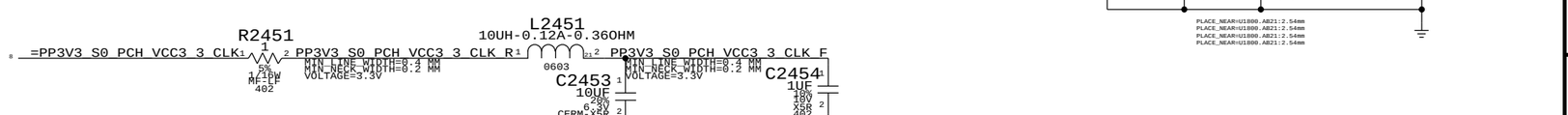

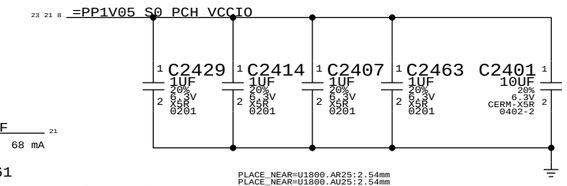

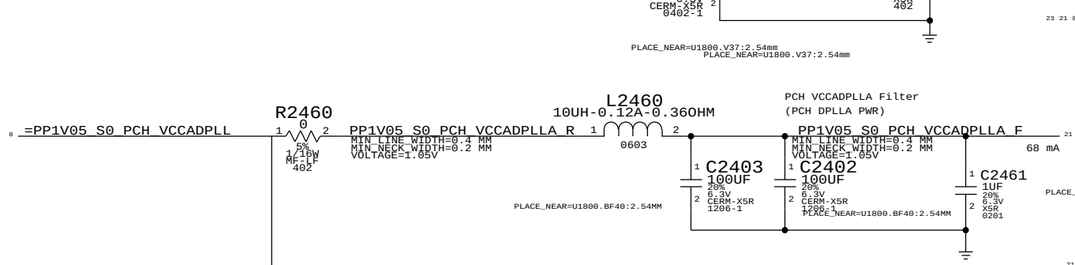

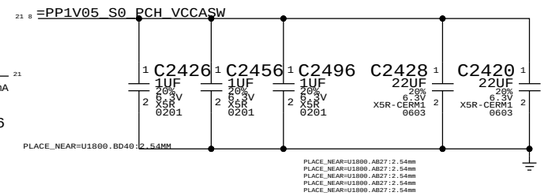

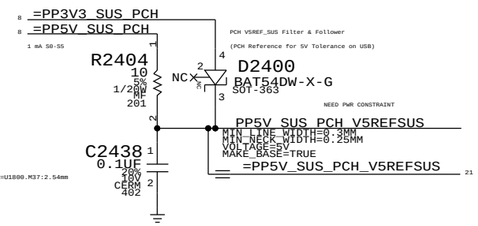

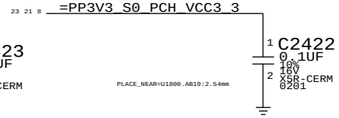

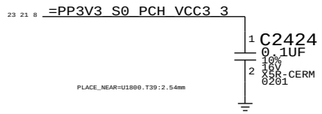

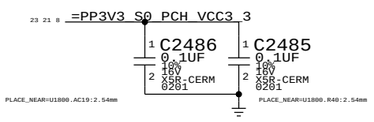

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Apple Inc.

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CPU Micro2-XDP

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

CRITICAL
XDP_CONN
J2500
DF40RC-60DP-0.4V
M-ST-SM1

518S0847

(R2560-R2563)
XDP_CPU:BPM

XDP_BPM_L<4>	R2560	0	
XDP_BPM_L<5>	R2561	0	
XDP_BPM_L<6>	R2562	0	
XDP_BPM_L<7>	R2563	0	

(R2564-R2567)
XDP_CPU:CFG

CPU_CFG<12>	R2564	0	
CPU_CFG<13>	R2565	0	
CPU_CFG<14>	R2566	0	
CPU_CFG<15>	R2567	0	

CPU_PWRGD	R2500	1K	PLACE_NEAR=U1000.C60:2.54mm
PM_PWRBTN_L	R2502	0	PLACE_NEAR=U4900.P17:2.54mm
CPU_CFG<0>	R2501	1K	PLACE_NEAR=U1000.B57:2.54mm
PM_PCH_SYS_PWROK	R2504	330	

XDP_CPU_PREQ_L	OBSEN_A0	
XDP_CPU_PRDY_L	OBSEN_A1	
XDP_BPM_L<0>	OBSDATA_A0	
XDP_BPM_L<1>	OBSDATA_A1	
XDP_BPM_L<2>	OBSDATA_A2	
XDP_BPM_L<3>	OBSDATA_A3	
CPU_CFG<10>	OBSEN_B0	
CPU_CFG<11>	OBSEN_B1	
XDP_OBSDATA_B<0>	OBSDATA_B0	
XDP_OBSDATA_B<1>	OBSDATA_B1	
XDP_OBSDATA_B<2>	OBSDATA_B2	
XDP_OBSDATA_B<3>	OBSDATA_B3	
XDP_CPU_PWRGD	PWRGD/HOOK0	
XDP_CPU_PWRBTN_L	HOOK1	
XDP_CPU_CFG<0>	VCC_OBS_AB / HOOK2	
XDP_VR_READY	HOOK3	
=SMBUS_XDP_SDA	SDA	
=SMBUS_XDP_SCL	SCL	
XDP_CPU_TCK	TCK1 / TCK0	

OBSEN_C0	CPU_CFG<16>	
OBSEN_C1	CPU_CFG<17>	
OBSDATA_C0	CPU_CFG<0>	
OBSDATA_C1	CPU_CFG<1>	
OBSDATA_C2	CPU_CFG<2>	
OBSDATA_C3	CPU_CFG<3>	
OBSEN_D0	CPU_CFG<8>	
OBSEN_D1	CPU_CFG<9>	
OBSDATA_D0	CPU_CFG<4>	
OBSDATA_D1	CPU_CFG<5>	
OBSDATA_D2	CPU_CFG<6>	
OBSDATA_D3	CPU_CFG<7>	
ITPCLK/HOOK4	XDP_CPU_CLK100M_P	
ITPCLK#/HOOK5	XDP_CPU_CLK100M_N	
VCC_OBS_CD		
RESET#/HOOK6	XDP_CPURST_L	
DBR#/HOOK7	XDP_DBRESET_L	
TDO	XDP_CPU_TDO	
TRSTn	XDP_CPU_TRST_L	
TDI	XDP_CPU_TDI	
TMS	XDP_CPU_TMS	
XDP_PRESENT#		

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_CPU_TDO	R2510	51	PLACE_NEAR=J2500.52:2.54mm
XDP_CPU_TDI	R2511	51	PLACE_NEAR=U1000.K61:2.54mm
XDP_CPU_TMS	R2512	51	PLACE_NEAR=U1000.H59:2.54mm
XDP_CPU_TCK	R2513	51	PLACE_NEAR=U1000.J58:2.54mm
XDP_CPU_TRST_L	R2514	51	PLACE_NEAR=U1000.H63:2.54mm

R2515	0	ITPXDP_CLK100M_P	PLACE_NEAR=R1841.1:2.54mm
R2516	0	ITPXDP_CLK100M_N	PLACE_NEAR=R1840.1:2.54mm
R2505	1K	CPU_RESET_L	PLACE_NEAR=U1000.G3:2.54mm

=PPVCCIO_S0_XDP
=PP3V3_S0_XDP NO STUFF R2540 1K 5% 1/16W MF-LF 402
C2500 0.1UF 10% 10V X7R-CERM 0402
C2501 0.1UF 10% 10V X7R-CERM 0402
R2581 1K 1/20W 5% MF 201
R2580 1K 1/20W 5% MF 201

XDP SIGNALS

(R2520-R2537)

XDP_DA0_USB_EXTA_OC_L	R2520	33	
XDP_DA1_USB_EXTB_OC_L	R2521	33	
XDP_DA2_USB_EXTC_OC_L	R2522	33	
XDP_DA3_USB_EXTD_OC_L	R2523	33	
XDP_DB0_USB_EXTB_OC_EHCI_L	R2524	33	
XDP_DB1_USB_EXTD_OC_EHCI_L	R2525	33	
XDP_DB2_AP_PWR_EN	R2526	33	
XDP_DB3_SDCONN_STATE_CHANGE	R2527	33	
XDP_FC0_MEM_VDD_SEL_1V5_L	R2528	33	
XDP_FC1	R2529	33	
XDP_DC0_ISOLATE_CPU_MEM_L	R2530	33	
XDP_DC1_MXM_GOOD	R2531	33	
XDP_DC2_DP_AUXCH_ISOL	R2532	33	
XDP_DC3_SATARDRVR_EN	R2533	33	
XDP_DD0_DP_GPU_TBT_SEL	R2534	33	
XDP_DD1_JTAG_ISP_TCK	R2535	33	
XDP_DD2_AUD_IPHS_SWITCH_EN	R2536	33	
XDP_DD3_ENET_LOW_PWR	R2537	33	

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	
XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L	
XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L	
XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI	
XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L	
XDP_DB2_PCH_GPIO10_AP_PWR_EN	
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	
XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L	
XDP_FC1_TBT_CIO_PLUG_EVENT	
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	
XDP_DC1_PCH_GPIO35_MXM_GOOD	
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	
XDP_DC3_PCH_GPIO19_SATARDRVR_EN	
XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL	
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	R2590	0	USB_EXTA_OC_L
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2591	0	USB_EXTB_OC_L
XDP_DB2_PCH_GPIO10_AP_PWR_EN	R2596	0	AP_PWR_EN
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	R2597	0	SDCONN_STATE_CHANGE
XDP_DC3_PCH_GPIO19_SATARDRVR_EN	R2573	0	SATARDRVR_EN
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	R2570	0	ISOLATE_CPU_MEM_L
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	R2572	0	DP_AUXCH_ISOL
XDP_FC1_TBT_CIO_PLUG_EVENT	R2574	1K	TBT_CIO_PLUG_EVENT_ISOL

Non-XDP Signals

PPDDR:1V5

XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L	R2595	0	MEM_VDD_SEL_1V5_L
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	R2575	0	JTAG_ISP_TCK
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	R2576	0	AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	R2577	0	ENET_LOW_PWR_PCH

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

PCH Micro2-XDP

CRITICAL
XDP_CONN
J2550
DF40RC-60DP-0.4V
M-ST-SM1

518S0847

=PP3V3_S5_XDP
C2580 0.1UF 10% 10V X7R-CERM 0402
C2581 0.1UF 10% 10V X7R-CERM 0402

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

TP_XDP_PCH_OBSFN_A<0>	OBSEN_A0	
TP_XDP_PCH_OBSFN_A<1>	OBSEN_A1	
XDP_DA0_USB_EXTA_OC_L	OBSDATA_A0	
XDP_DA1_USB_EXTB_OC_L	OBSDATA_A1	
XDP_DA2_USB_EXTC_OC_L	OBSDATA_A2	
XDP_DA3_USB_EXTD_OC_L	OBSDATA_A3	
TP_XDP_PCH_OBSFN_B<0>	OBSEN_B0	
TP_XDP_PCH_OBSFN_B<1>	OBSEN_B1	
XDP_DB0_USB_EXTB_OC_EHCI_L	OBSDATA_B0	
XDP_DB1_USB_EXTD_OC_EHCI_L	OBSDATA_B1	
XDP_DB2_AP_PWR_EN	OBSDATA_B2	
XDP_DB3_SDCONN_STATE_CHANGE	OBSDATA_B3	
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	
XDP_PCH_PWRBTN_L	HOOK1	
TP_XDPPCH_HOOK2	VCC_OBS_AB / HOOK2	
TP_XDPPCH_HOOK3	HOOK3	
=SMBUS_XDP_SDA	SDA	
=SMBUS_XDP_SCL	SCL	
XDP_PCH_TCK	TCK1 / TCK0	

OBSEN_C0	XDP_FC0_MEM_VDD_SEL_1V5_L	
OBSEN_C1	XDP_FC1	
OBSDATA_C0	XDP_DC0_ISOLATE_CPU_MEM_L	
OBSDATA_C1	XDP_DC1_MXM_GOOD	
OBSDATA_C2	XDP_DC2_DP_AUXCH_ISOL	
OBSDATA_C3	XDP_DC3_SATARDRVR_EN	
OBSEN_D0	TP_XDP_PCH_OBSFN_D<0>	
OBSEN_D1	TP_XDP_PCH_OBSFN_D<1>	
OBSDATA_D0	XDP_DD0_DP_GPU_TBT_SEL	
OBSDATA_D1	XDP_DD1_JTAG_ISP_TCK	
OBSDATA_D2	XDP_DD2_AUD_IPHS_SWITCH_EN	
OBSDATA_D3	XDP_DD3_ENET_LOW_PWR	
ITPCLK/HOOK4	TP_XDP_PCH_HOOK4	
ITPCLK#/HOOK5	TP_XDP_PCH_HOOK5	
VCC_OBS_CD		
RESET#/HOOK6	XDPPCH_PLTRST_L	
DBR#/HOOK7	XDP_DBRESET_L	
TDO	XDP_PCH_TDO	
TRSTn	TP_XDP_PCH_TRST_L	
TDI	XDP_PCH_TDI	
TMS	XDP_PCH_TMS	
XDP_PRESENT#		

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_PCH_TDO	R2550	51	PLACE_NEAR=J2550.52:2.54mm
XDP_PCH_TDI	R2551	51	PLACE_NEAR=U1800.K5:2.54mm
XDP_PCH_TMS	R2552	51	PLACE_NEAR=U1800.H7:2.54mm
XDP_PCH_TCK	R2556	51	PLACE_NEAR=U1800.J3:2.54mm

ALL_SYS_PWRGD	R2584	1K	PLACE_NEAR=J2550.39:2.54mm
PM_PWRBTN_L	R2585	0	PLACE_NEAR=U4900.P17:2.54mm

1K series R on PCH Support Page

=PP1V05_SUS_PCH_JTAG

SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2011

PAGE TITLE: CPU & PCH XDP

Apple Inc.

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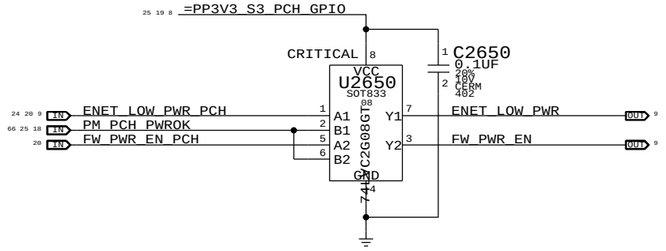
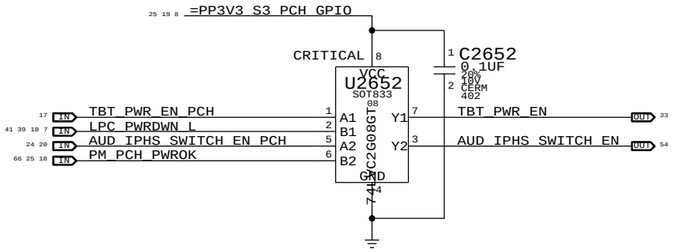
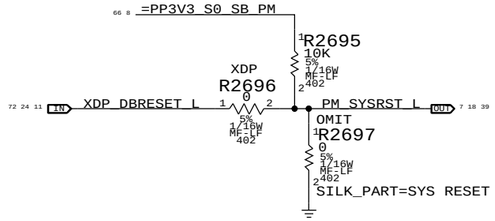
GPIO Glitch Prevention

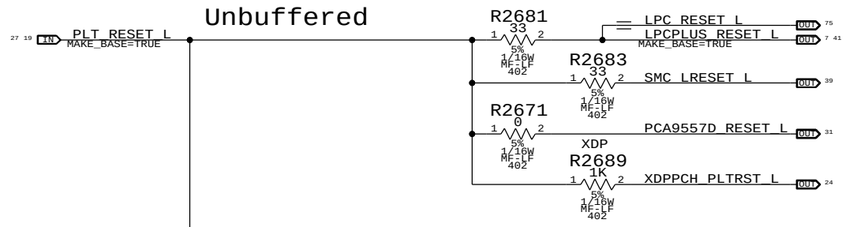




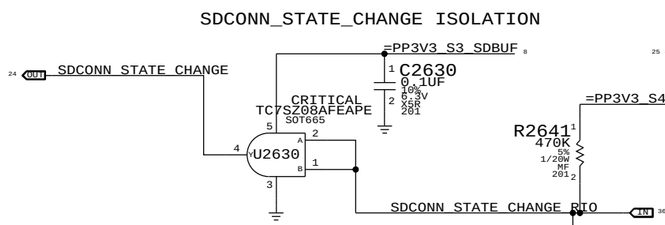
PCH Reset Button

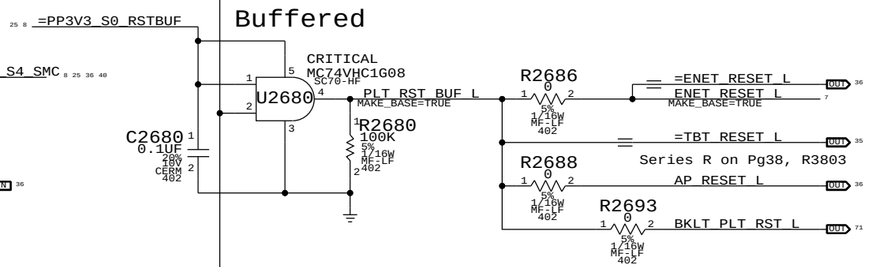


Platform Reset Connections

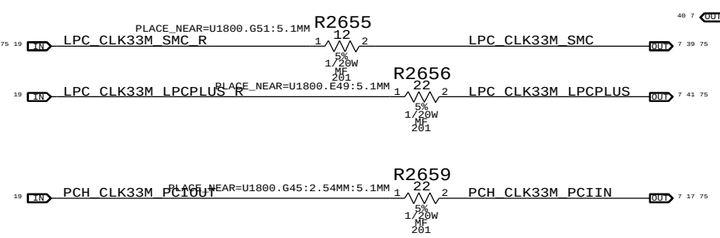


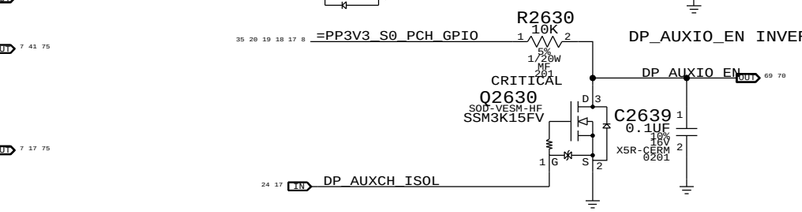
SDCONN_STATE_CHANGE ISOLATION

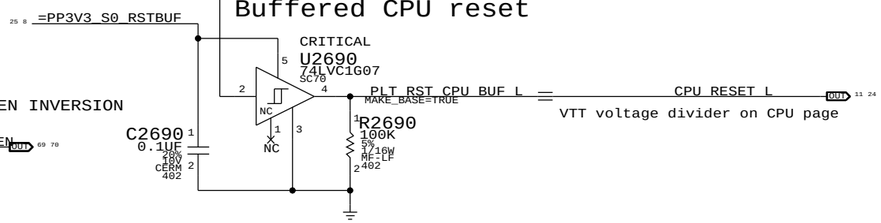




33 MHz Clock Series Termination



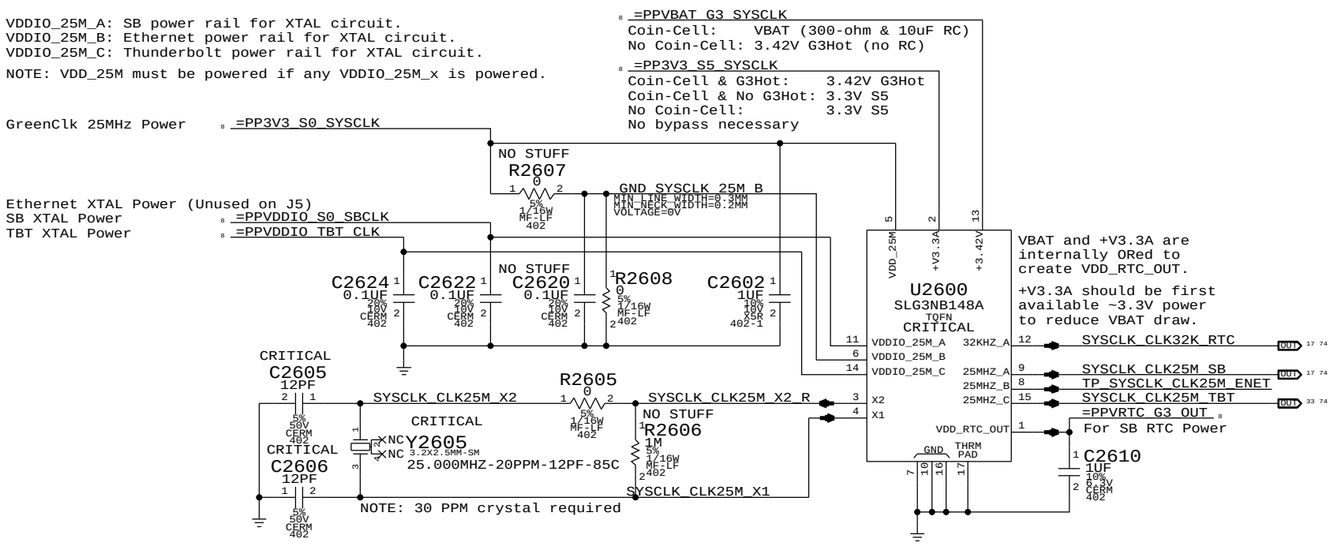




System RTC Power Source & 32kHz / 25MHz Clock Generator

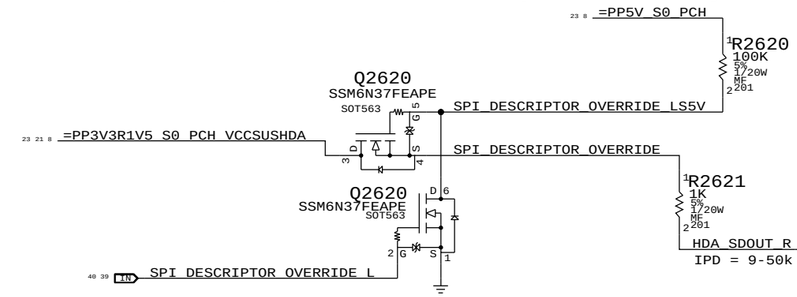
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC_MASTER=MASTER	SYNC_DATE=MASTER
PAGE TITLE	Chipset Support
Apple Inc.	DRAWING NUMBER <SCH_NUM> / SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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USB MUX FOR LS/FS INTERNAL DEVICES

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

NON_REM 1 :	NON_REM 0	STRAP PIN CFG
0	0	ALL PORTS ARE REMOVABLE
0	1	PORT 1 IS NON REMOVABLE
1	0	PORT 1&2 ARE NON REMOVABLE
1	1	PORT 1&2&3 ARE NON REMOVABLE

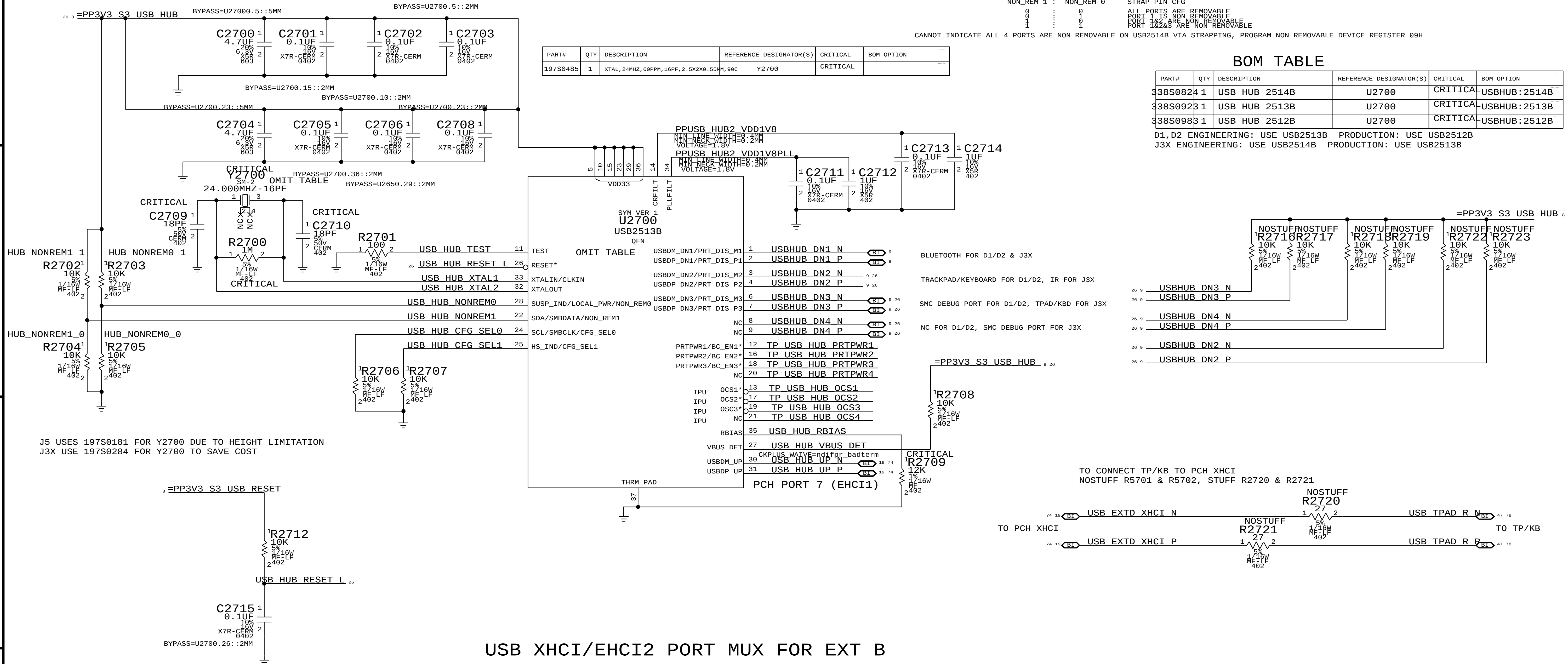
CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STRAPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0485	1	XTAL,24MHZ,60PPM,16PF,2.5X2X0.55MM,90C	Y2700	CRITICAL	

BOM TABLE

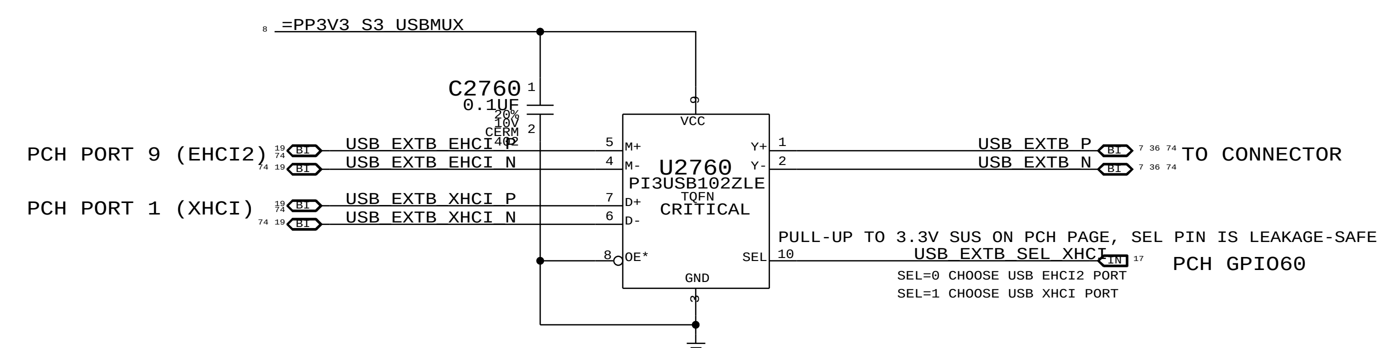
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB:2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB:2513B
338S0988	1	USB HUB 2512B	U2700	CRITICAL	USBHUB:2512B

D1,D2 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



=PP3V3_S3_USB_HUB
BYPASS=U27000.5::5MM
BYPASS=U2700.5::2MM
C2700 4.7UF 20% 6.3V X5R 603
C2701 0.1UF 10% 16V X7R-CERM 0402
C2702 0.1UF 10% 16V X7R-CERM 0402
C2703 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U2700.15::2MM
BYPASS=U2700.10::2MM
BYPASS=U2700.23::5MM
BYPASS=U2700.23::2MM
C2704 4.7UF 20% 6.3V X5R 603
C2705 0.1UF 10% 16V X7R-CERM 0402
C2706 0.1UF 10% 16V X7R-CERM 0402
C2708 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U2700.36::2MM
BYPASS=U2650.29::2MM
CRITICAL
Y2700 SM-2
OMIT_TABLE
24.000MHZ-16PF
C2709 18PF 5% 50V CERM 402
C2710 18PF 5% 50V CERM 402
R2700 1M 5% 1/16W MF-LF 402
R2701 100 5% 1/16W MF-LF 402
PPUSB_HUB2_VDD1V8
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.8V
PPUSB_HUB2_VDD1V8PLL
C2711 0.1UF 10% 16V X7R-CERM 0402
C2712 1UF 10% 16V X5R 402
C2713 0.1UF 10% 16V X7R-CERM 0402
C2714 1UF 10% 16V X5R 402
SYM VER 1
U2700
USB2513B
QFN
OMIT_TABLE
VDD33
CRFILT
PLLFILT
TEST
RESET*
XTALIN/CLKIN
XTALOUT
SUSP_IND/LOCAL_PWR/NON_REM0
SDA/SMBDATA/NON_REM1
SCL/SMBCLK/CFG_SEL0
HS_IND/CFG_SEL1
USB_HUB_TEST
USB_HUB_RESET_L
USB_HUB_XTAL1
USB_HUB_XTAL2
USB_HUB_NONREM0
USB_HUB_NONREM1
USB_HUB_CFG_SEL0
USB_HUB_CFG_SEL1
HUB_NONREM1_1
HUB_NONREM0_1
R2702 10K 5% 1/16W MF-LF 402
R2703 10K 5% 1/16W MF-LF 402
HUB_NONREM1_0
HUB_NONREM0_0
R2704 10K 5% 1/16W MF-LF 402
R2705 10K 5% 1/16W MF-LF 402
R2706 10K 5% 1/16W MF-LF 402
R2707 10K 5% 1/16W MF-LF 402
USBDM_DN1/PRT_DIS_M1
USBDP_DN1/PRT_DIS_P1
USBDM_DN2/PRT_DIS_M2
USBDP_DN2/PRT_DIS_P2
USBDM_DN3/PRT_DIS_M3
USBDP_DN3/PRT_DIS_P3
USBHUB_DN1_N
USBHUB_DN1_P
USBHUB_DN2_N
USBHUB_DN2_P
USBHUB_DN3_N
USBHUB_DN3_P
USBHUB_DN4_N
USBHUB_DN4_P
BLUETOOTH FOR D1/D2 & J3X
TRACKPAD/KEYBOARD FOR D1/D2, IR FOR J3X
SMC DEBUG PORT FOR D1/D2, TPAD/KBD FOR J3X
NC FOR D1/D2, SMC DEBUG PORT FOR J3X
PRTPWR1/BC_EN1*
PRTPWR2/BC_EN2*
PRTPWR3/BC_EN3*
TP_USB_HUB_PRTPWR1
TP_USB_HUB_PRTPWR2
TP_USB_HUB_PRTPWR3
TP_USB_HUB_PRTPWR4
OCS1*
OCS2*
OSC3*
IPU
TP_USB_HUB_OCS1
TP_USB_HUB_OCS2
TP_USB_HUB_OCS3
TP_USB_HUB_OCS4
RBIAS
USB_HUB_RBIAS
VBUS_DET
USB_HUB_VBUS_DET
CKPLUS_WAIVE=ndifpr_badterm
USBDM_UP
USBDP_UP
USB_HUB_UP_N
USB_HUB_UP_P
PCH PORT 7 (EHCI1)
THRM_PAD
=PP3V3_S3_USB_HUB
R2708 10K 5% 1/16W MF-LF 402
CRITICAL
R2709 12K 1% 1/16W MF 402
NOSTUFF
R2716 10K 5% 1/16W MF-LF 402
R2717 10K 5% 1/16W MF-LF 402
R2718 10K 5% 1/16W MF-LF 402
R2719 10K 5% 1/16W MF-LF 402
R2722 10K 5% 1/16W MF-LF 402
R2723 10K 5% 1/16W MF-LF 402
J5 USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
J3X USE 197S0284 FOR Y2700 TO SAVE COST
=PP3V3_S3_USB_RESET
R2712 10K 5% 1/16W MF-LF 402
USB_HUB_RESET_L
C2715 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U2700.26::2MM
TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R5701 & R5702, STUFF R2720 & R2721
TO PCH XHCI
USB_EXTD_XHCI_N
USB_EXTD_XHCI_P
NOSTUFF
R2720 27 5% 1/16W MF-LF 402
R2721 27 5% 1/16W MF-LF 402
USB_TPAD_R_N
USB_TPAD_R_P
TO TP/KB

USB XHCI/EHCI2 PORT MUX FOR EXT B



PULL-UP TO 3.3V SUS ON PCH PAGE, SEL PIN IS LEAKAGE-SAFE
SEL=0 CHOOSE USB EHCI2 PORT
SEL=1 CHOOSE USB XHCI PORT

SYNC_MASTER=J5_AMD SYNC_DATE=08/17/2011

PAGE TITLE: USB HUB & MUX

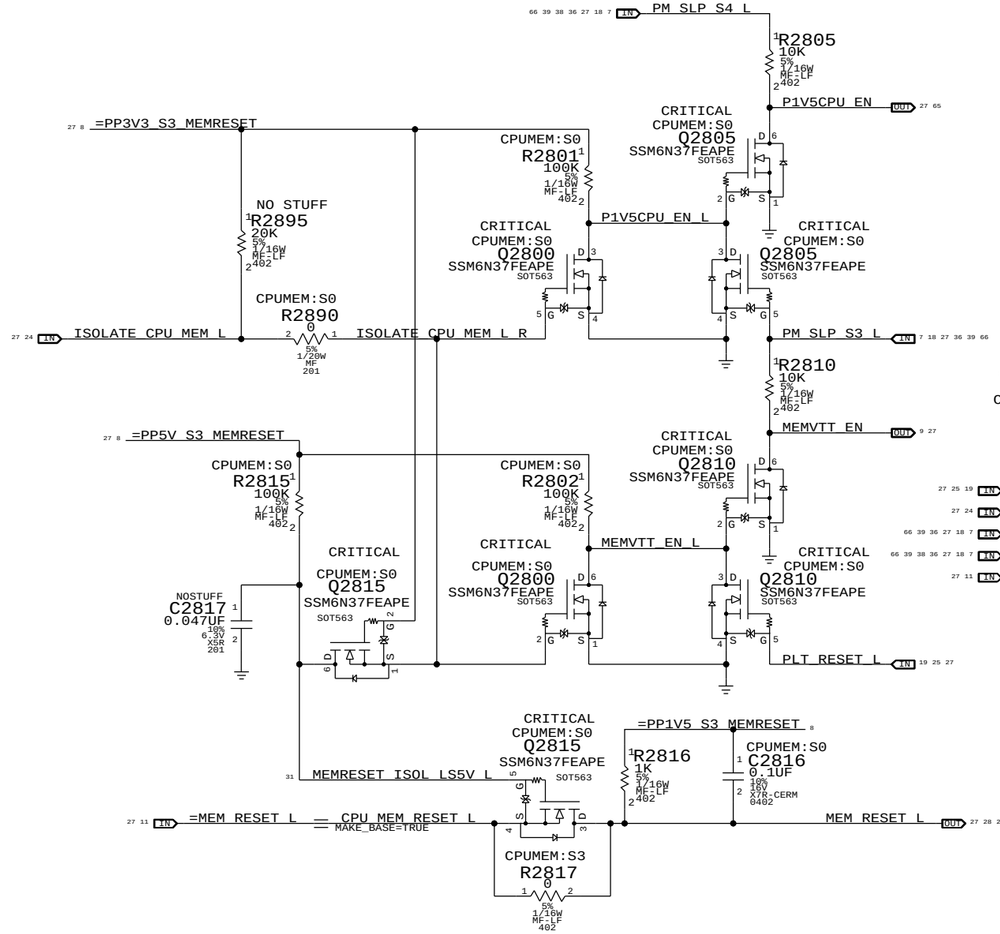
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>

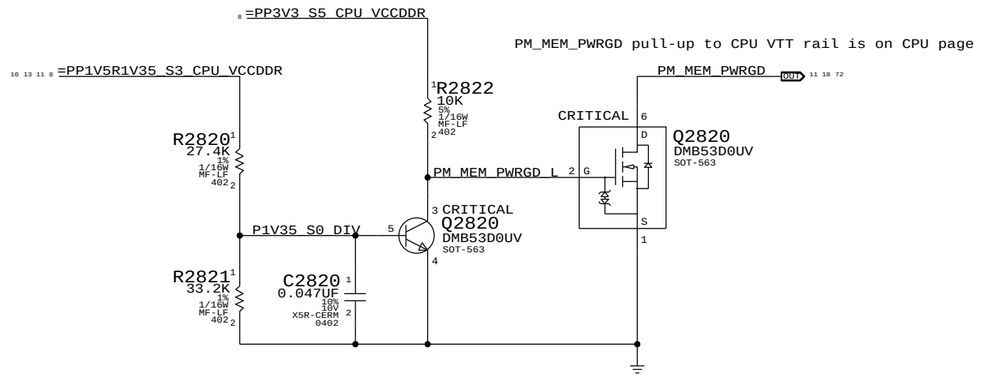
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

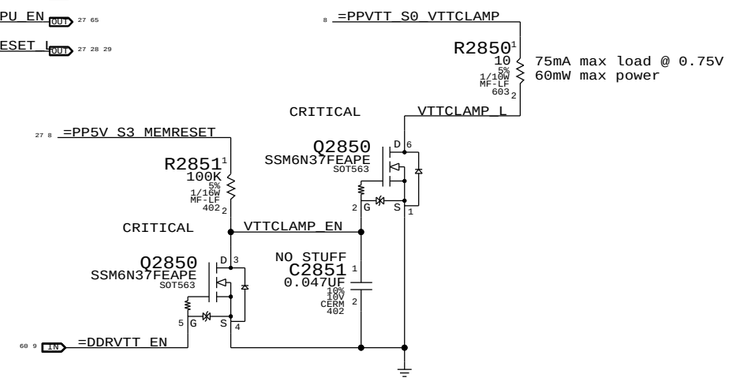


1V35 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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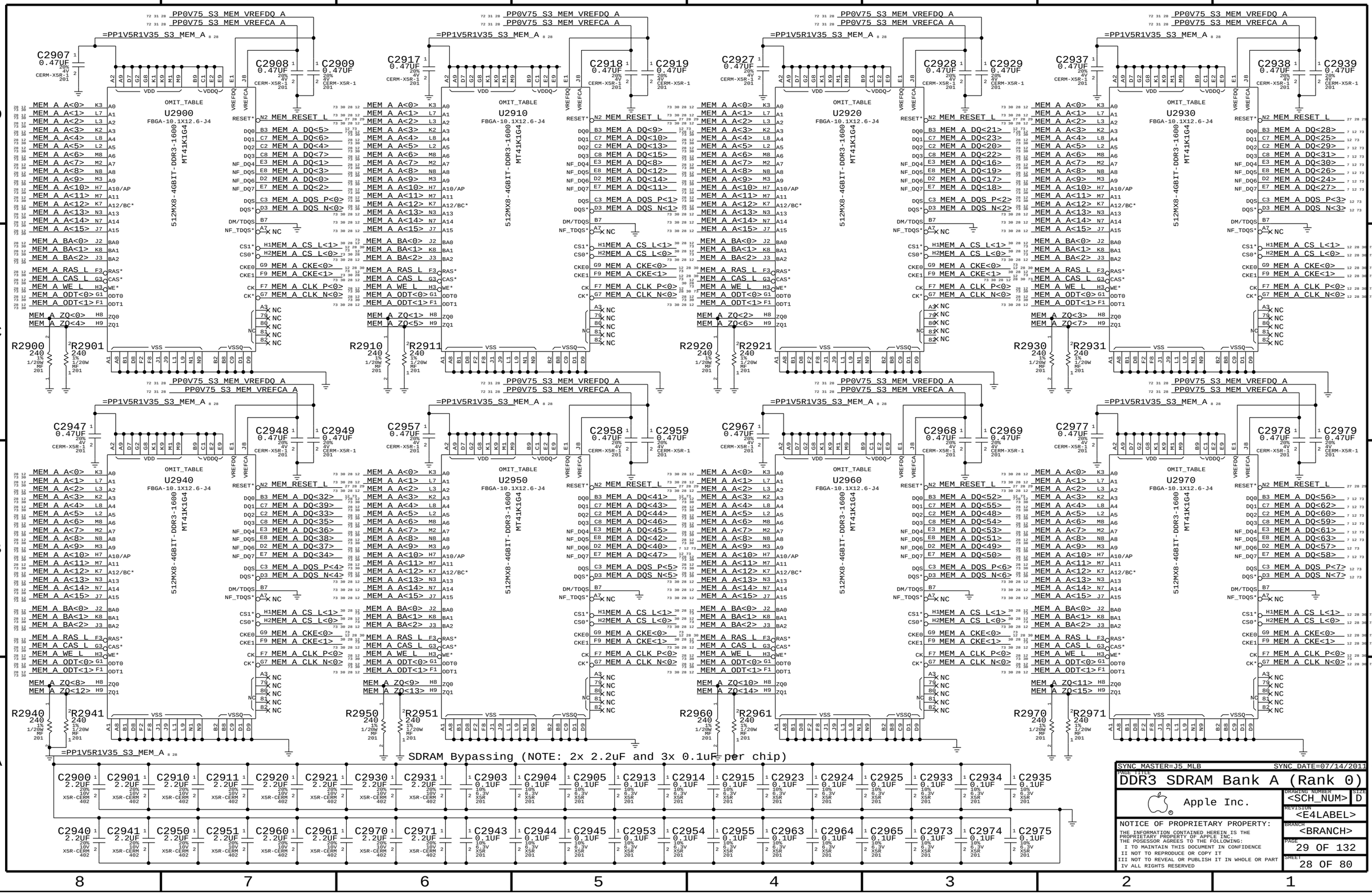
U2900
U2910
U2920
U2930
U2940
U2950
U2960
U2970
FBGA-10.1X12.6-J4
512MX8-4GBIT-DDR3-1600
MT41K1G4
OMIT_TABLE
=PP1V5R1V35_S3_MEM_A
PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA_A
MEM_RESET_L
MEM_A_CS_L<1>
MEM_A_CS_L<0>
MEM_A_CKE<0>
MEM_A_CKE<1>
MEM_A_CLK_P<0>
MEM_A_CLK_N<0>
MEM_A_RAS_L
MEM_A_CAS_L
MEM_A_WE_L
MEM_A_ODT<0>
MEM_A_ODT<1>
SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
SYNC_MASTER=J5_MLB
SYNC_DATE=07/14/2011
PAGE TITLE
DDR3 SDRAM Bank A (Rank 0)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
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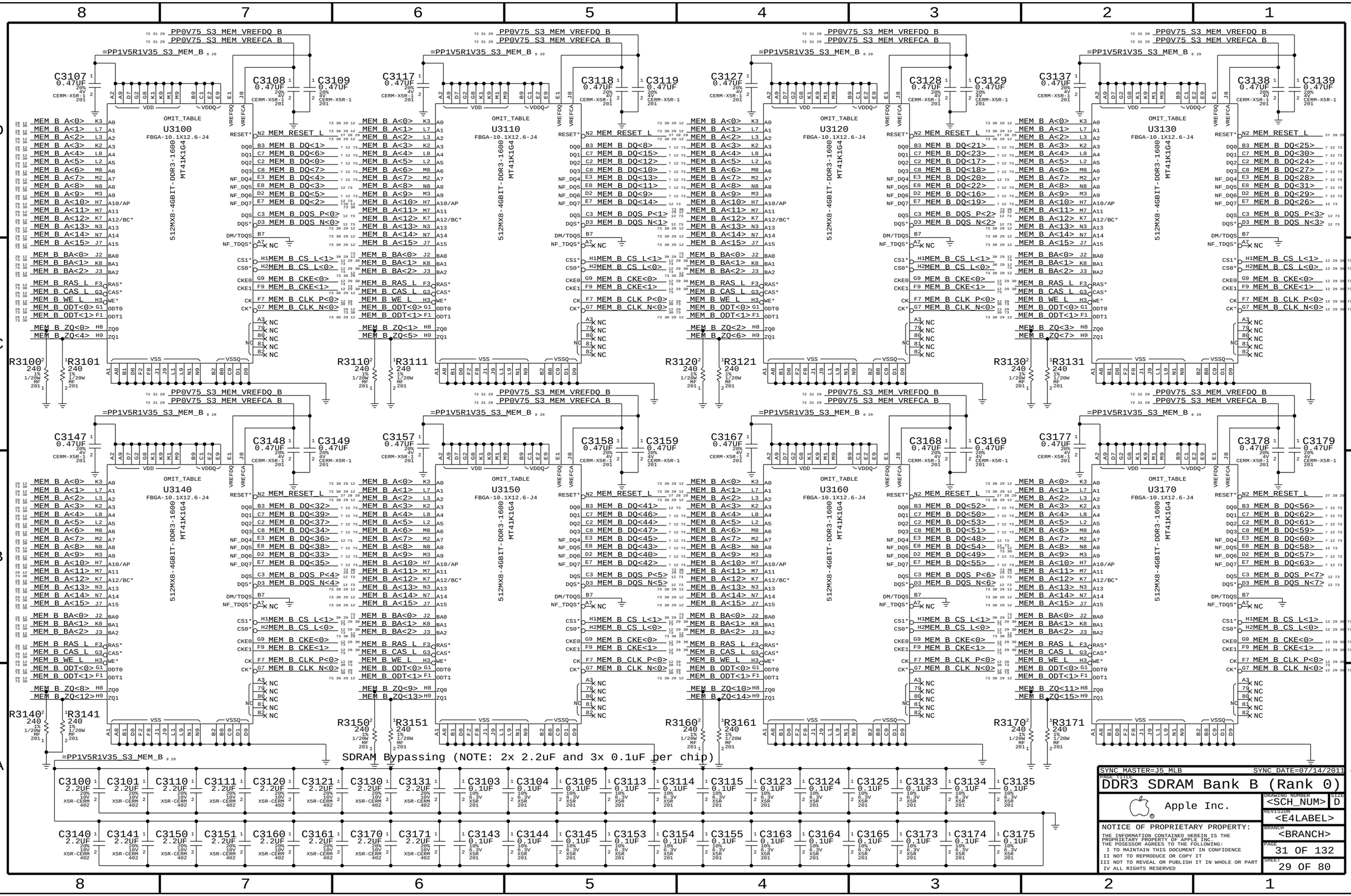
U3100
U3110
U3120
U3130
U3140
U3150
U3160
U3170
FBGA-10.1X12.6-J4
512MX8-4GBIT-DDR3-1600
MT41K1G4
OMIT_TABLE
PP0V75_S3_MEM_VREFDQ_B
PP0V75_S3_MEM_VREFCA_B
=PP1V5R1V35_S3_MEM_B
MEM_RESET_L
SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
SYNC_MASTER=J5_MLB
SYNC_DATE=07/14/2011
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DDR3 SDRAM Bank B (Rank 0)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
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REVISION
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JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

=PP0V75_S0_MEM_VTT_A

MEM_A_A<3>	RP3305	36	1	8	5% 1/32W 4X0201
MEM_A_CKE<1>	RP3301	36	4	5	5% 1/32W 4X0201
MEM_A_BA<2>	RP3302	36	2	7	5% 1/32W 4X0201
MEM_A_A<14>	RP3306	36	2	7	5% 1/32W 4X0201
MEM_A_A<2>	RP3303	36	1	8	5% 1/32W 4X0201
MEM_A_A<12>	RP3302	36	1	8	5% 1/32W 4X0201
MEM_A_ODT<0>	RP3301	36	2	7	5% 1/32W 4X0201
MEM_A_BA<0>	RP3305	36	2	7	5% 1/32W 4X0201
MEM_A_A<1>	RP3303	36	2	7	5% 1/32W 4X0201
MEM_A_A<7>	RP3307	36	3	6	5% 1/32W 4X0201
MEM_A_A<8>	RP3306	36	1	8	5% 1/32W 4X0201
MEM_A_CS_L<1>	RP3305	36	3	6	5% 1/32W 4X0201
MEM_A_A<11>	RP3306	36	4	5	5% 1/32W 4X0201
MEM_A_BA<1>	RP3302	36	3	6	5% 1/32W 4X0201
MEM_A_CKE<0>	RP3304	36	3	6	5% 1/32W 4X0201
MEM_A_A<0>	RP3303	36	4	5	5% 1/32W 4X0201
MEM_A_A<10>	RP3304	36	1	8	5% 1/32W 4X0201
MEM_A_A<9>	RP3307	36	2	7	5% 1/32W 4X0201
MEM_A_WE_L	RP3302	36	4	5	5% 1/32W 4X0201
MEM_A_A<4>	RP3303	36	3	6	5% 1/32W 4X0201
MEM_A_A<5>	RP3307	36	1	8	5% 1/32W 4X0201
MEM_A_A<15>	RP3305	36	4	5	5% 1/32W 4X0201
MEM_A_A<13>	RP3307	36	4	5	5% 1/32W 4X0201
MEM_A_CAS_L	RP3304	36	2	7	5% 1/32W 4X0201
MEM_A_CS_L<0>	RP3304	36	4	5	5% 1/32W 4X0201
MEM_A_RAS_L	RP3301	36	3	6	5% 1/32W 4X0201
MEM_A_ODT<1>	RP3301	36	1	8	5% 1/32W 4X0201
MEM_A_A<6>	RP3306	36	3	6	5% 1/32W 4X0201

C3300 0.47UF 20% 4V CERM-X5R-1 201
C3302 0.47UF 20% 4V CERM-X5R-1 201
C3303 0.47UF 20% 4V CERM-X5R-1 201
C3304 0.47UF 20% 4V CERM-X5R-1 201
C3305 0.47UF 20% 4V CERM-X5R-1 201
C3306 0.47UF 20% 4V CERM-X5R-1 201
C3307 0.47UF 20% 4V CERM-X5R-1 201
C3308 0.47UF 20% 4V CERM-X5R-1 201
C3310 0.47UF 20% 4V CERM-X5R-1 201

=PP0V75_S0_MEM_VTT_B

MEM_B_WE_L	RP3322	36	2	7	5% 1/32W 4X0201
MEM_B_A<13>	RP3325	36	1	8	5% 1/32W 4X0201
MEM_B_CKE<1>	RP3328	36	1	8	5% 1/32W 4X0201
MEM_B_A<12>	RP3325	36	2	7	5% 1/32W 4X0201
MEM_B_ODT<1>	RP3328	36	2	7	5% 1/32W 4X0201
MEM_B_A<0>	RP3325	36	3	6	5% 1/32W 4X0201
MEM_B_CS_L<1>	RP3320	36	2	7	5% 1/32W 4X0201
MEM_B_BA<0>	RP3326	36	4	5	5% 1/32W 4X0201
MEM_B_A<6>	RP3330	36	2	7	5% 1/32W 4X0201
MEM_B_ODT<0>	RP3320	36	3	6	5% 1/32W 4X0201
MEM_B_A<4>	RP3330	36	1	8	5% 1/32W 4X0201
MEM_B_A<5>	RP3330	36	3	6	5% 1/32W 4X0201
MEM_B_BA<1>	RP3324	36	4	5	5% 1/32W 4X0201
MEM_B_A<9>	RP3326	36	2	7	5% 1/32W 4X0201
MEM_B_A<8>	RP3324	36	1	8	5% 1/32W 4X0201
MEM_B_A<3>	RP3326	36	3	6	5% 1/32W 4X0201
MEM_B_A<10>	RP3322	36	3	6	5% 1/32W 4X0201
MEM_B_A<7>	RP3326	36	1	8	5% 1/32W 4X0201
MEM_B_A<1>	RP3330	36	4	5	5% 1/32W 4X0201
MEM_B_A<14>	RP3324	36	3	6	5% 1/32W 4X0201
MEM_B_A<11>	RP3324	36	2	7	5% 1/32W 4X0201
MEM_B_A<2>	RP3325	36	4	5	5% 1/32W 4X0201
MEM_B_BA<2>	RP3320	36	4	5	5% 1/32W 4X0201
MEM_B_CS_L<0>	RP3320	36	1	8	5% 1/32W 4X0201
MEM_B_RAS_L	RP3322	36	1	8	5% 1/32W 4X0201
MEM_B_CAS_L	RP3328	36	4	5	5% 1/32W 4X0201
MEM_B_CKE<0>	RP3328	36	3	6	5% 1/32W 4X0201
MEM_B_A<15>	RP3322	36	4	5	5% 1/32W 4X0201

C3320 0.47UF 20% 4V CERM-X5R-1 201
C3322 0.47UF 20% 4V CERM-X5R-1 201
C3323 0.47UF 20% 4V CERM-X5R-1 201
C3324 0.47UF 20% 4V CERM-X5R-1 201
C3325 0.47UF 20% 4V CERM-X5R-1 201
C3326 0.47UF 20% 4V CERM-X5R-1 201
C3327 0.47UF 20% 4V CERM-X5R-1 201
C3328 0.47UF 20% 4V CERM-X5R-1 201
C3330 0.47UF 20% 4V CERM-X5R-1 201

MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

MEM_A_CLK_N<0> — R3350 30 5% 1/20W MF 201 — MEM_A_CLK0_TERM_R — C3351 0.1UF 10% 6.3V X5R 201
C3350 3.3PF 5% 25V CERM 201 (PLACE_NEAR=U2900.F7:3.2mm)
MEM_A_CLK_P<0> — R3351 30 5% 1/20W MF 201

MEM_B_CLK_N<0> — R3360 30 5% 1/20W MF 201 — MEM_B_CLK0_TERM_R — C3361 0.1UF 10% 6.3V X5R 201
C3360 3.3PF 5% 25V CERM 201 (PLACE_NEAR=U3170.F7:3.2mm)
MEM_B_CLK_P<0> — R3361 30 5% 1/20W MF 201

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: DDR3 Termination

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs Apple margining circuit.
- VREFDQ:LDO - LDO outputs sent to DQ inputs.
- VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
- VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
- VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
- VREFCA:LDO - LDO outputs sent to CA inputs.
- VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

10mA max load

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE: DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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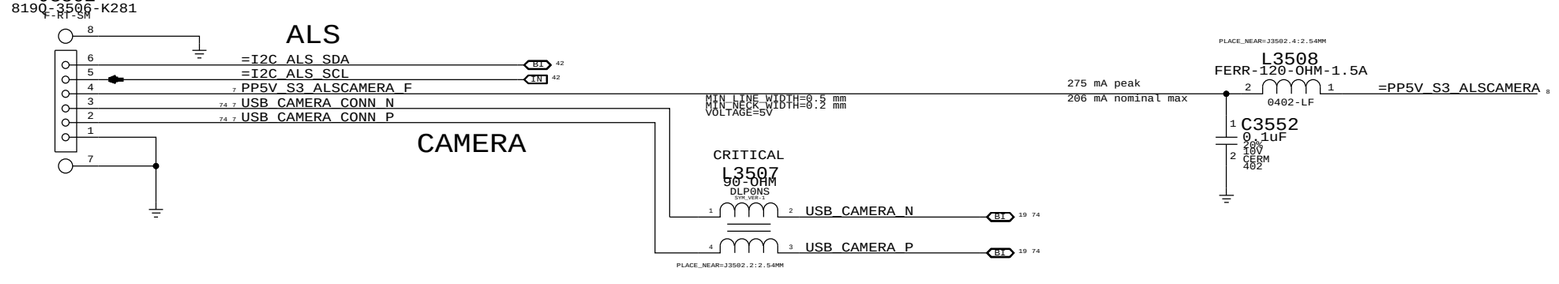
518S0767

CRITICAL
J3502
819Q-3506-K281
F-RT-SM



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
ALS/CAMERA CONNECTOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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CRITICAL
OMIT_TABLE
U3600
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)
PCIE GEN2
RECEIVE
TRANSMIT
MISC
EEPROM
JTAG/TEST PORT
DISPLAYPORT
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
PORT0
PORT1
PORT2
PORT3
PORTS
CLOCKS
PCIE RESET
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
SNK0 AC Coupling
SNK1 AC Coupling
For unused port, pull CONFIG1, CONFIG2, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=J5_MLB_KEPLER
SYNC_DATE=11/14/2011
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
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33 OF 80
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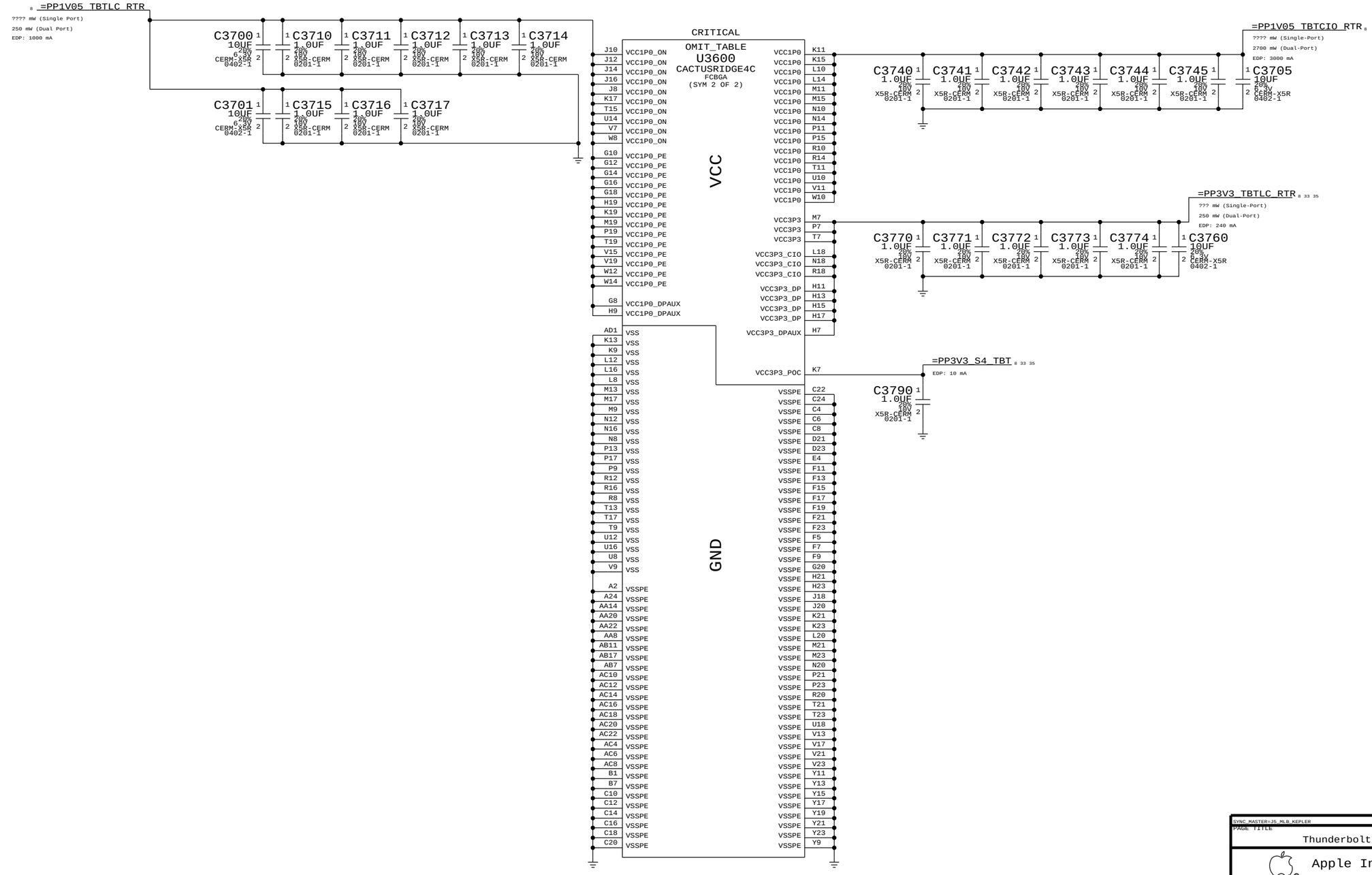

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2011

PAGE TITLE

Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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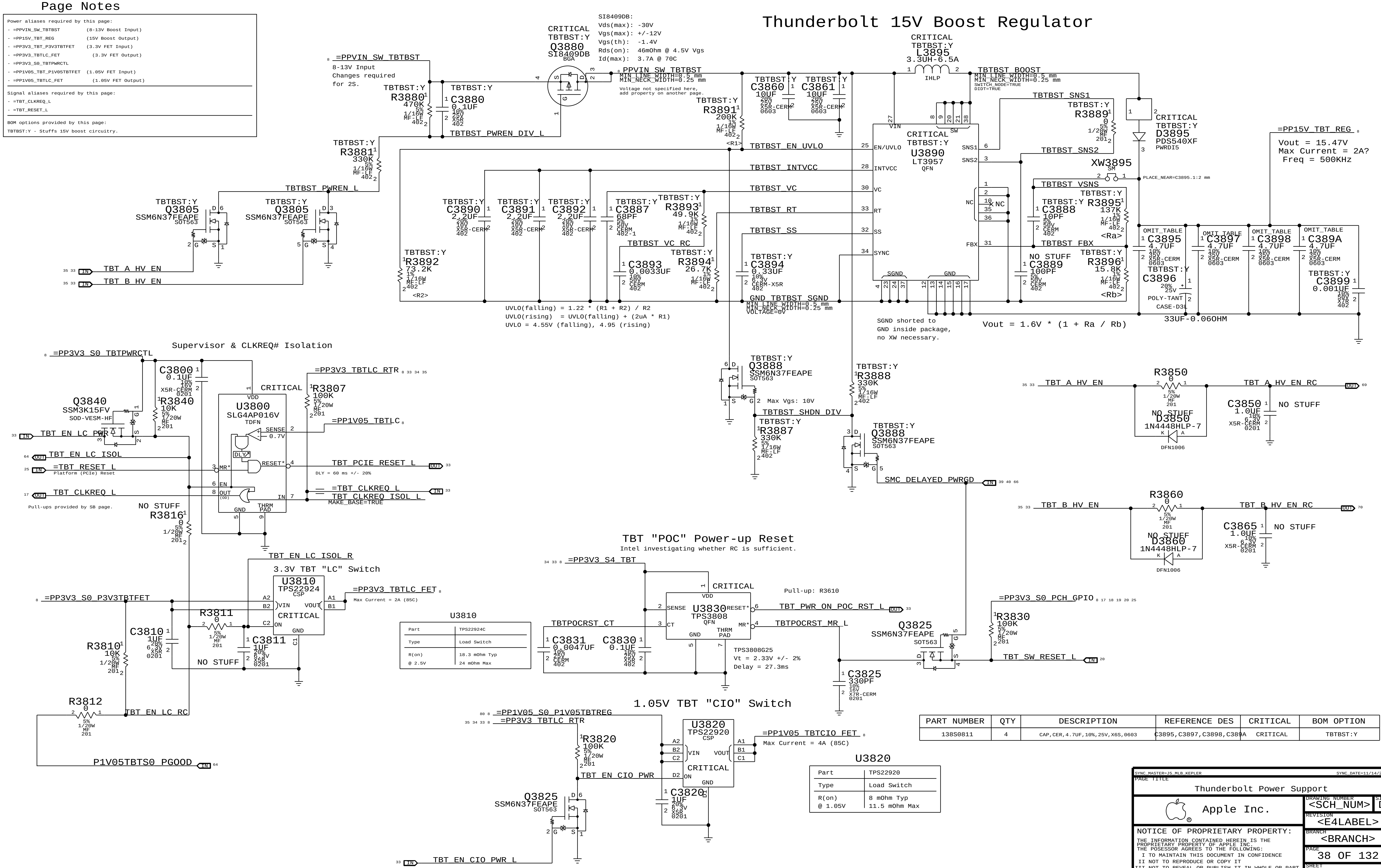
Thunderbolt 15V Boost Regulator

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBTLC_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBTLC_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.



SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C
=PPVIN_SW_TBTBST
8-13V Input
Changes required for 2S.
CRITICAL TBTBST:Y Q3880 SI8409DB BGA
PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.
CRITICAL TBTBST:Y L3895 3.3UH-6.5A IHLP
TBTBST_BOOST
SWITCH_NODE=TRUE
DIDT=TRUE
TBTBST_PWREN_DIV_L
TBTBST_PWREN_L
TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
TBTBST_SNS1
TBTBST_SNS2
TBTBST_VSNS
TBTBST_FBX
CRITICAL TBTBST:Y U3890 LT3957 QFN
CRITICAL TBTBST:Y D3895 PDS540XF PWRDI5
XW3895 SM
PLACE_NEAR=C3895.1:2 mm
=PP15V_TBT_REG
Vout = 15.47V
Max Current = 2A?
Freq = 500KHz
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)
SGND shorted to GND inside package, no XW necessary.
Vout = 1.6V * (1 + Ra / Rb)
33UF-0.060OHM
OMIT_TABLE C3895 C3897 C3898 C389A 4.7UF 10% 35V X5R-CERM 0603
TBTBST:Y C3896 20% 25V POLY-TANT CASE-D3L
TBTBST:Y C3899 0.001UF
TBT_A_HV_EN
TBT_B_HV_EN
Q3805 SSM6N37FEAPE SOT563
Supervisor & CLKREQ# Isolation
=PP3V3_S0_TBTPWRCTL
Q3840 SSM3K15FV SOD-VESM-HF
C3800 0.1UF
R3840 10K
CRITICAL U3800 SLG4AP016V TDFN
=PP3V3_TBTLC_RTR
R3807 100K
=PP1V05_TBTLC
TBT_EN_LC_PWR
TBT_EN_LC_ISOL
=TBT_RESET_L
Platform (PCIe) Reset
TBT_PCIE_RESET_L
DLY = 60 ms +/- 20%
TBT_CLKREQ_L
=TBT_CLKREQ_L
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE
Pull-ups provided by SB page.
NO STUFF R3816 0
TBTBST:Y Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
R3888 330K
R3887 330K
TBTBST_SHDN_DIV
SMC_DELAYED_PWRGD
R3850 0
TBT_A_HV_EN_RC
C3850 1.0UF NO STUFF
NO STUFF D3850 1N4448HLP-7 DFN1006
R3860 0
TBT_B_HV_EN_RC
C3865 1.0UF NO STUFF
NO STUFF D3860 1N4448HLP-7 DFN1006
TBT "POC" Power-up Reset
Intel investigating whether RC is sufficient.
=PP3V3_S4_TBT
CRITICAL U3830 TPS3808 QFN
Pull-up: R3610
TBT_PWR_ON_POC_RST_L
TBTPOCRST_CT
TBTPOCRST_MR_L
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms
C3831 0.0047UF
C3830 0.1UF
C3825 330PF
Q3825 SSM6N37FEAPE SOT563
=PP3V3_S0_PCH_GPIO
R3830 100K
TBT_SW_RESET_L
TBT_EN_LC_ISOL_R
3.3V TBT "LC" Switch
U3810 TPS22924 CSP CRITICAL
=PP3V3_S0_P3V3TBTFET
=PP3V3_TBTLC_FET
Max Current = 2A (85C)
R3810 10K
C3810 1UF
R3811 0
C3811 1UF NO STUFF
R3812 0
TBT_EN_LC_RC
P1V05TBTS0_PGOOD
1.05V TBT "CIO" Switch
=PP1V05_S0_P1V05TBTREG
=PP3V3_TBTLC_RTR
R3820 100K
U3820 TPS22920 CSP CRITICAL
=PP1V05_TBTCIO_FET
Max Current = 4A (85C)
TBT_EN_CIO_PWR
C3820 1UF
Q3825 SSM6N37FEAPE SOT563
TBT_EN_CIO_PWR_L

U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	4	CAP,CER,4.7UF,10%,25V,X6S,0603	C3895,C3897,C3898,C389A	CRITICAL	TBTBST:Y

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2011

PAGE TITLE: Thunderbolt Power Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L4470,L4471,L4473,L4474		

3V S3 WLAN FET

DEBUG CURRENT SENSE RD135 connects to PP3V3_WLAN_F

AIRPORT

Max Current = 2A (85C)

U4450
TPS22924
CSP
CRITICAL

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

RIO FLEX CONNECTOR

CRITICAL

J4410
DF40CG3.0-70DS-0.4V
F-ST-SM

*NOTE: This connector is shielded 70P Hirose Receptacle.

516S1058

Note: This receptacle mates with the plug with APN 998-4708.

RIO POWER CONNECTOR

CRITICAL
J4400
504050-0691
M-RT-SM

518s0862

Supervisor & CLKFREG # Isolation

Delay = 130 ms +/- 20%

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

SIGNAL_MODEL=MOJO_MUX

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: RIO CONNECTORS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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' C4518 & C4517 Placement Note:
' It is critical that these two should be near
' to U1800 pin AM1 and AM3.

D2R Passive DeEmphasis

VALUE: 0.0 DB

R4506 0 5% 1/20W MF 201 NOSTUFF
C4515 5.0PF 0201 +/-0.1PF C0G 25V NOSTUFF
R4507 0 5% 1/20W MF 201

SATA_SSDRHDD_D2R_P → SATA_HDD_D2R_RC_P → C4518 0.01UF 10%16V X7R-CERM 0402 → SATA_HDD_D2R_P (OUT)
SATA_SSDRHDD_D2R_N → SATA_HDD_D2R_RC_N → C4517 0.01UF 10%16V X7R-CERM 0402 → SATA_HDD_D2R_N (OUT)

PLACE_NEAR=U1800.AM1:5MM
PLACE_NEAR=U1800.AM3:5MM
GND_VOID=TRUE

R4508 0 5% 1/20W MF 201 NOSTUFF
C4521 15PF 5% 25V NP0 0201 NOSTUFF
R4510 0 5% 1/20W MF 201

SATA_SSDRHDD_R2D_N → SATA_HDD_R2D_RC_N → C4522 0.01UF 10%16V X7R-CERM 0402 → SATA_HDD_R2D_C_N (IN)

C4524 15PF 5% 25V NP0 0201

SATA_SSDRHDD_R2D_P → SATA_HDD_R2D_RC_P → C4525 0.01UF 10%16V X7R-CERM 0402 → SATA_HDD_R2D_C_P (IN)

R2D Passive DeEmphasis

VALUE: 0.0 DB

516S1035 (recpt)

CRITICAL
J4500
DF40CG1.5-48DS-0.4V
F-ST-SM

PP3V3_S0_SSD_FLT
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V

PLACE_NEAR=J4500.9:3MM
CRITICAL
L4500
FERR-70-OHM-4A
0603

PLACE_NEAR=L4500.1:2MM
C4501 0.1UF 20% 16V CERM 402

PP3V3_S0_SSD_R
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=3.3V

C4502 0.1UF 20% 16V CERM 402
PLACE_NEAR=L4500.2:2MM

CRITICAL
R4530
0.001
1% 1W MF 0612

=PP3V3_S0_SSD
ISNS_SSD_P (OUT)
ISNS_SSD_N (OUT)

SATA_SSDRHDD_D2R_P
SATA_SSDRHDD_D2R_N
SMC_OOB1_TX_I (IN)
SMC_OOB1_RX_L (OUT)
SATA_SSDRHDD_R2D_P
SATA_SSDRHDD_R2D_N

SATA GUMSTICK2 CONNECTOR

PP5V_S0_HDD_FLT
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

L4510
FERR-70-OHM-4A
0603
CRITICAL
PLACE_NEAR=J4500.39:3MM

=PP5V_S0_HDD

C4510 0.1UF 20% 16V CERM 402
PLACE_NEAR=L4510.1:2MM

C4511 0.1UF 20% 16V CERM 402
PLACE_NEAR=L4510.2:2MM

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: SSD/HDD Connectors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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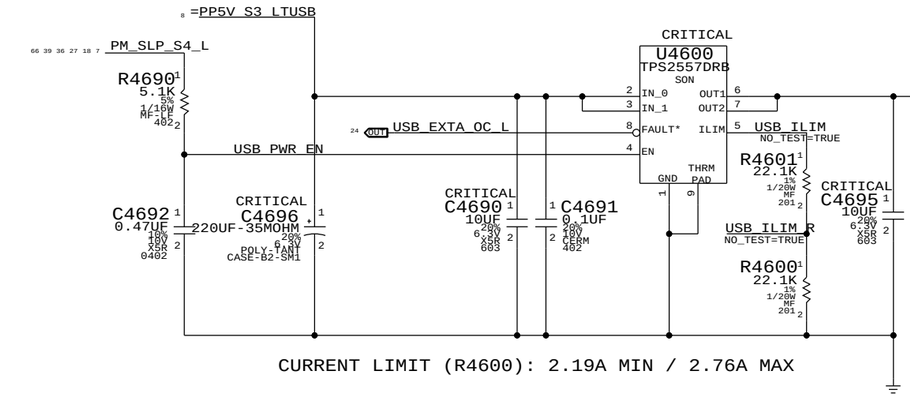
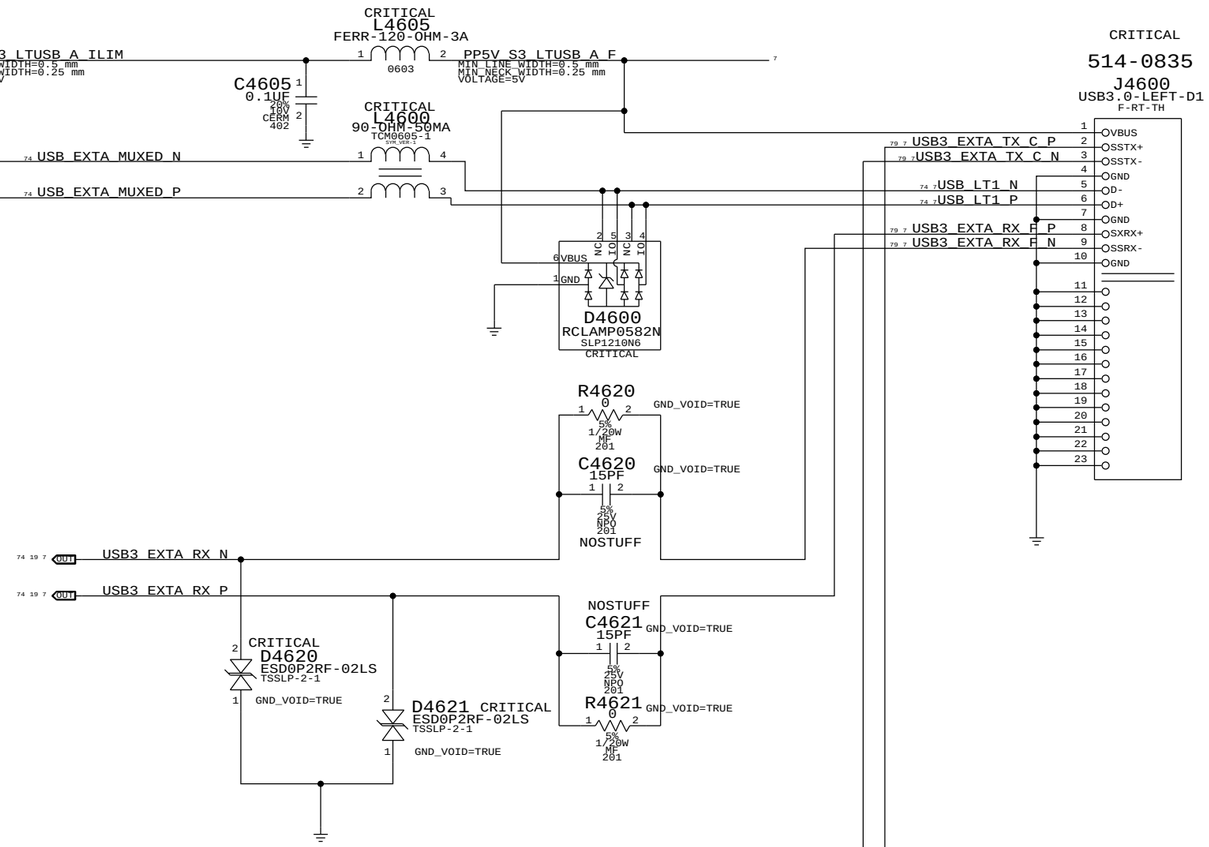
USB Port Power Switch

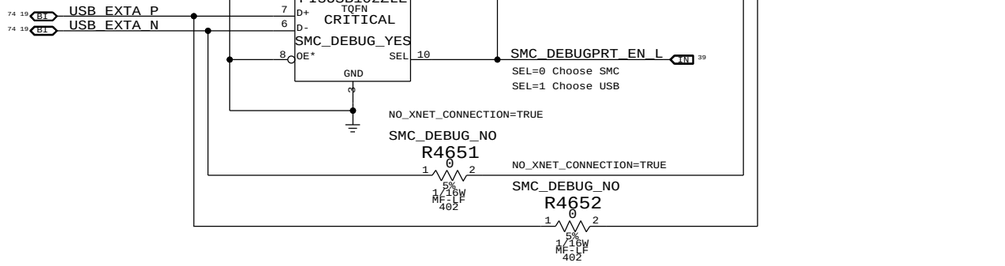


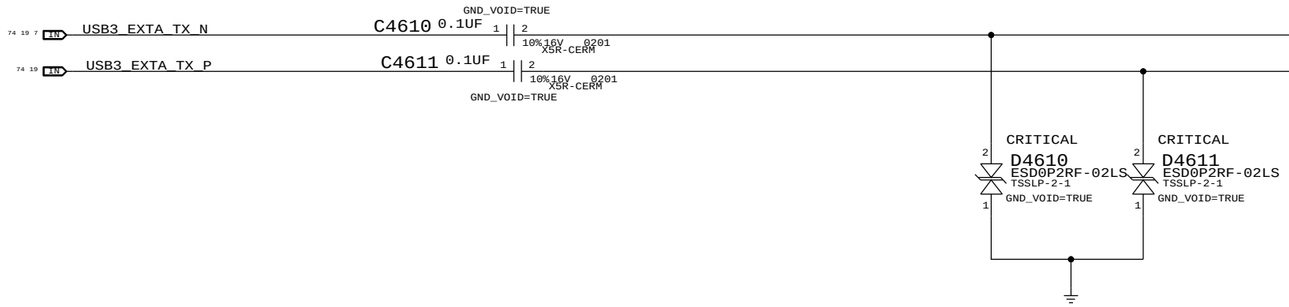
CURRENT LIMIT (R4600): 2.19A MIN / 2.76A MAX

Left USB Port A



USB/SMC Debug Mux





SYNC_MASTER=J5_AMD SYNC_DATE=08/24/2011

PAGE TITLE: USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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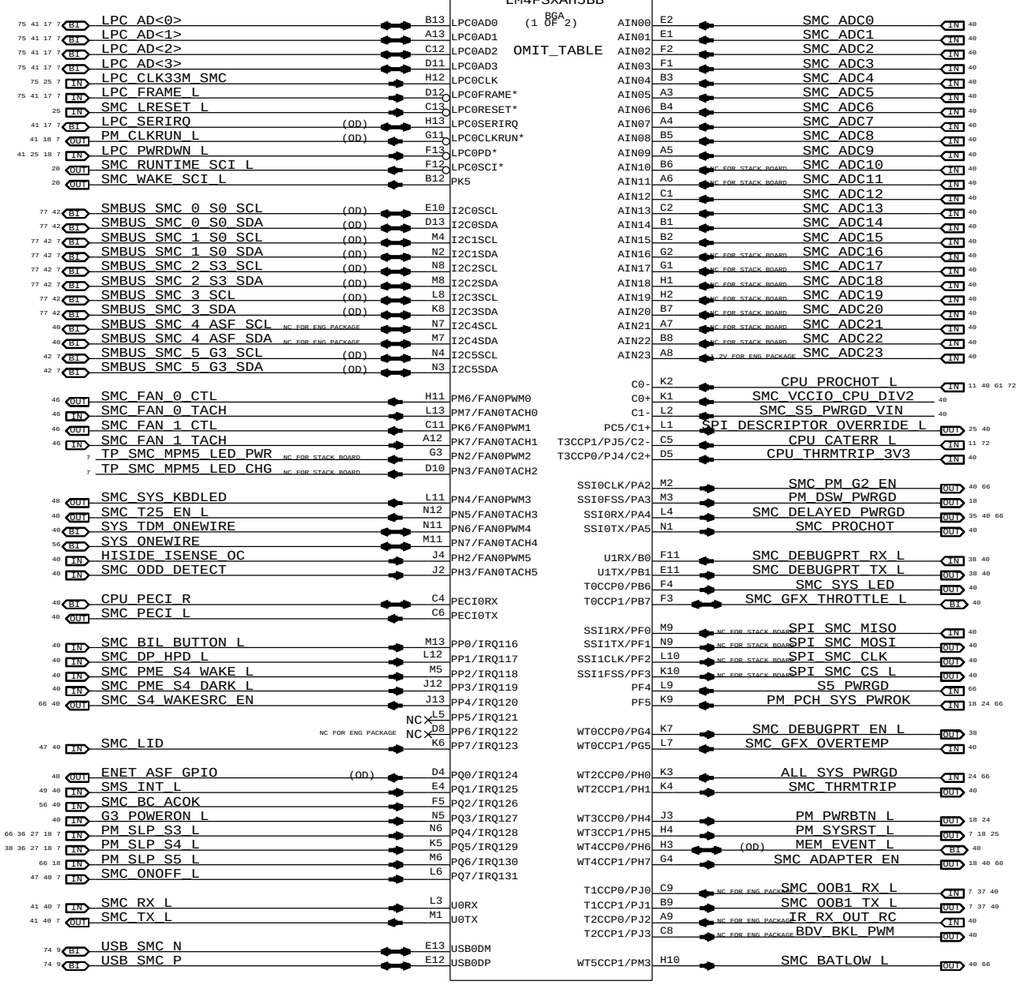
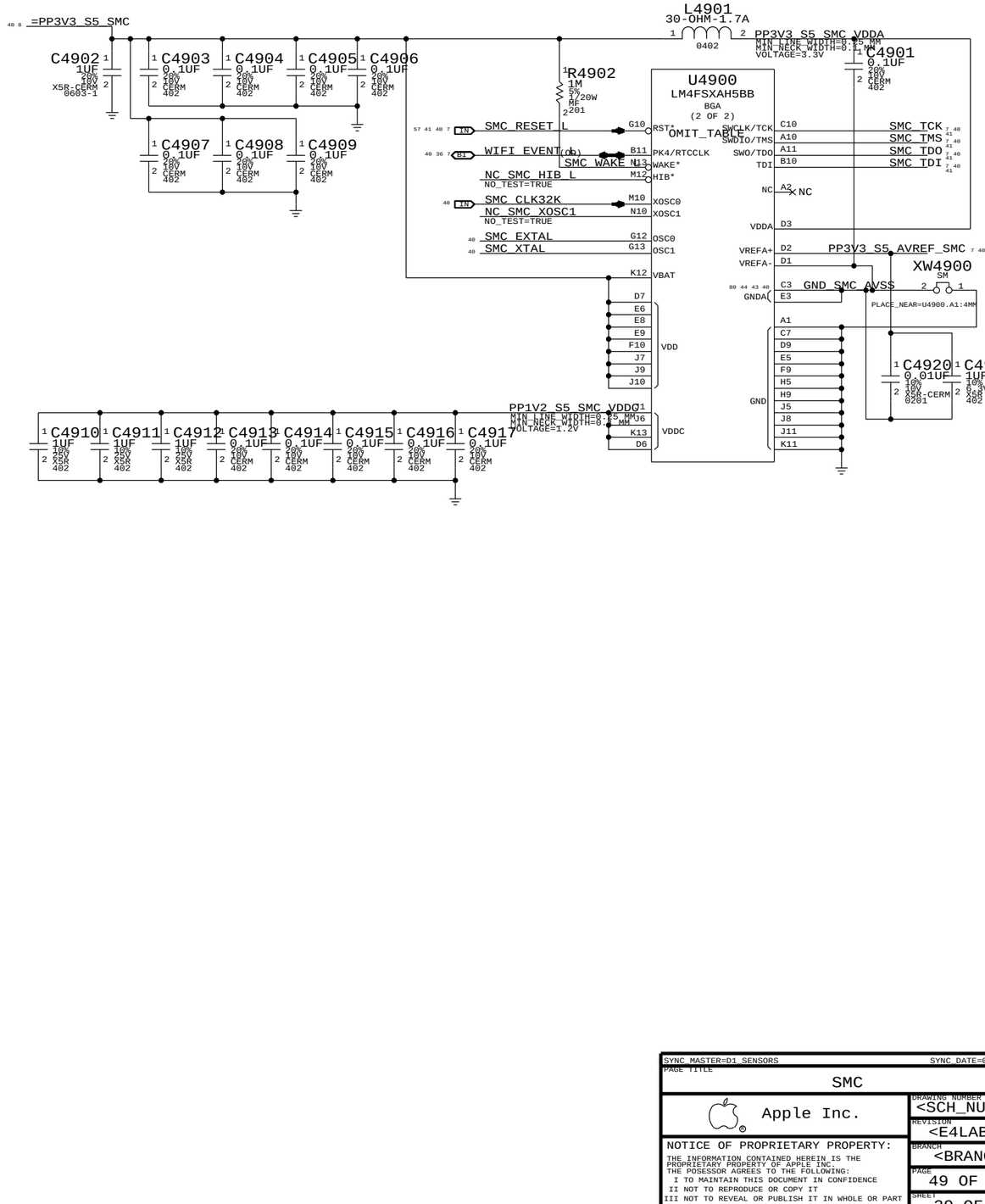
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 49 OF 132
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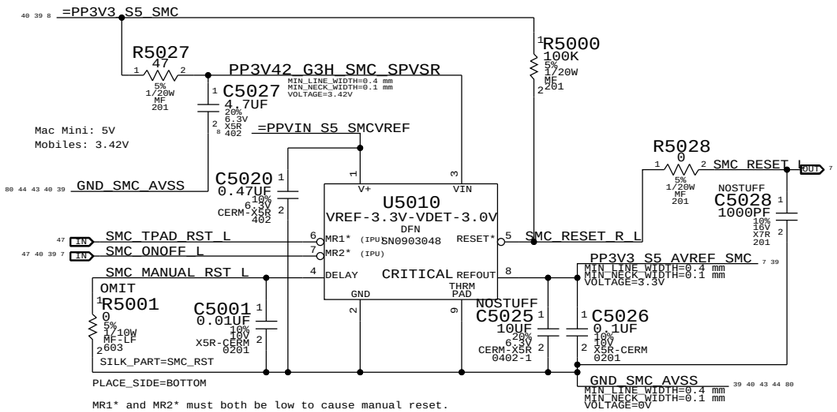
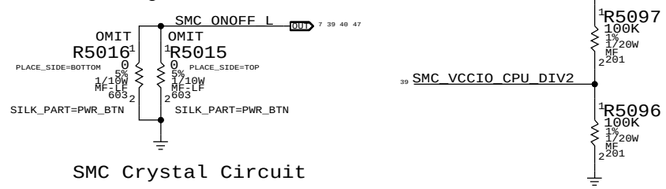
SMC Reset "Button", Supervisor & AVREF Supply



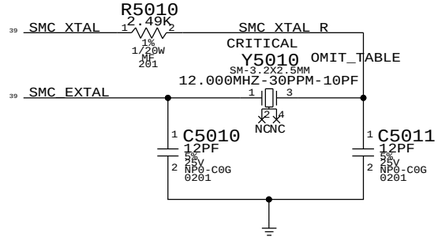
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



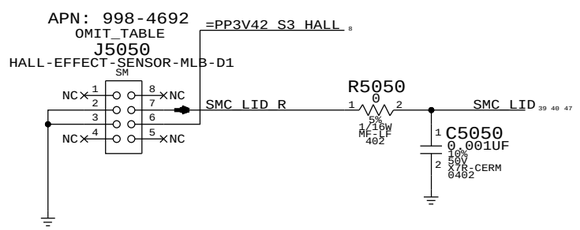
SMC Crystal Circuit



SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0486	1	XTAL,12MHZ,30PPM,10PF,3.2X2.5X0.7MM,90C	Y5010	CRITICAL	

Hall Effect pads



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-9320	1	SUBASSY,PCBA HALL EFFECT,J4	J5050	CRITICAL	

639-3261 (J4 Hall effect board) reports to 607-9320

Debug Power "Buttons"

SMC Crystal Circuit

SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0486	1	XTAL,12MHZ,30PPM,10PF,3.2X2.5X0.7MM,90C	Y5010	CRITICAL	

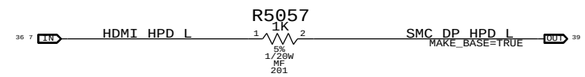
Hall Effect pads

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-9320	1	SUBASSY,PCBA HALL EFFECT,J4	J5050	CRITICAL	

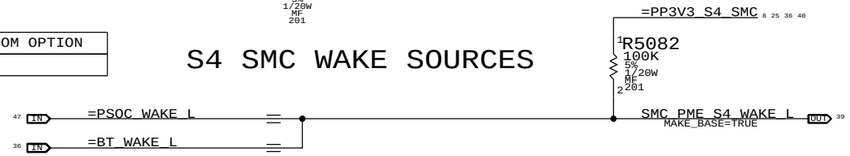
639-3261 (J4 Hall effect board) reports to 607-9320

=CHGR_ACOK	SMC_BC_ACOK		
HISIDE_ISENSE_OC	NC_HISIDE_ISENSE_OC		
SMC_ADC0	SMC_CPU_VSENSE		
SMC_ADC1	SMC_CPU_ISENSE		
SMC_ADC2	NC_SMC_GPU_HI_ISENSE		
SMC_ADC3	SMC_DCIN_VSENSE		
SMC_ADC4	SMC_DCIN_ISENSE		
SMC_ADC5	SMC_PBUS_VSENSE		
SMC_ADC6	SMC_SSD_ISENSE		
SMC_ADC7	SMC_BMON_ISENSE		
SMC_ADC8	SMC_CPU_HI_ISENSE		
SMC_ADC9	SMC_OTHER_HI_ISENSE		
SMC_ADC10	SMC_MEM_ISENSE		
SMC_ADC11	SMC_VCCIO_ISENSE		
SMC_ADC12	SMC_AXG_VSENSE		
SMC_ADC13	SMC_CPU_SA_ISENSE		
SMC_ADC14	SMC_CPU_SA_VSENSE		
SMC_ADC15	SMC_LCD_PANEL_ISENSE		
SMC_ADC16	SMC_LCDBKLT_VSENSE		
SMC_ADC17	SMC_LCDBKLT_ISENSE		
SMC_ADC18	SMC_AXG_ISENSE		
SMC_ADC19	NC_SMC_GPU_P1V35_ISENSE		
SMC_ADC20	NC_SMC_T25_ISENSE		
SMC_ADC21	NC_SMC_PCH_CORE_ISENSE		
SMC_ADC22	SMC_X29_ISENSE		
SMC_ADC23	SMC_TBT_ISENSE		
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL		
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA		
BDV_BKL_PWM	NC_BDV_BKL_PWM		
SMC_PME_S4_DARK_L	SDCONN_STATE_CHANGE_SMC		
	=TBT_WAKE_L		

HDMI HPD ESD PROTECTION

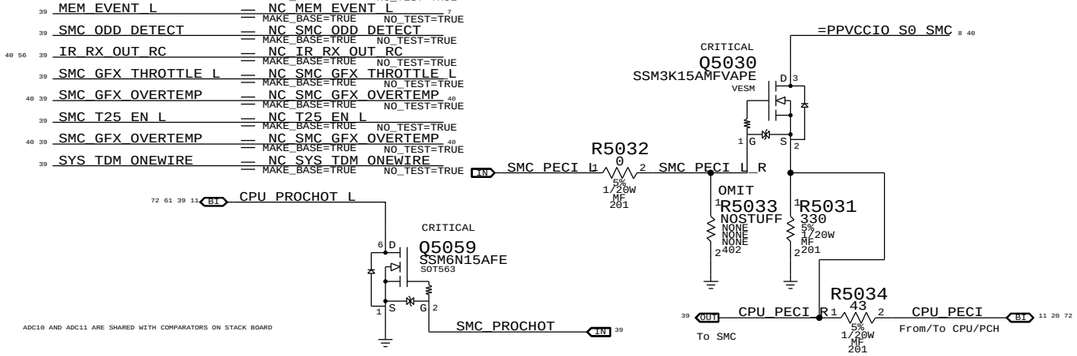


S4 SMC WAKE SOURCES



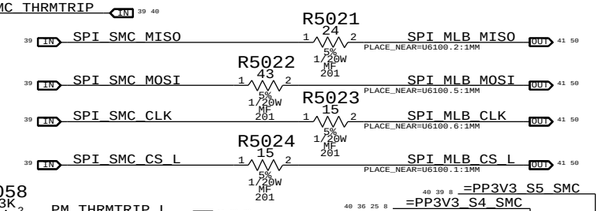
ENET_ASF_GPIO	NC_ENET_ASF_GPIO	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_SYS_LED	NC_SMC_SYS_LED	MAKE_BASE=TRUE	NO_TEST=TRUE
MEM_EVENT_L	NC_MEM_EVENT_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_ODD_DETECT	NC_SMC_ODD_DETECT	MAKE_BASE=TRUE	NO_TEST=TRUE
IR_RX_OUT_RC	NC_IR_RX_OUT_RC	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_T25_EN_L	NC_T25_EN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE	NO_TEST=TRUE
SYS_TDM_ONEWIRE	NC_SYS_TDM_ONEWIRE	MAKE_BASE=TRUE	NO_TEST=TRUE

SMC12 PECI SUPPORT

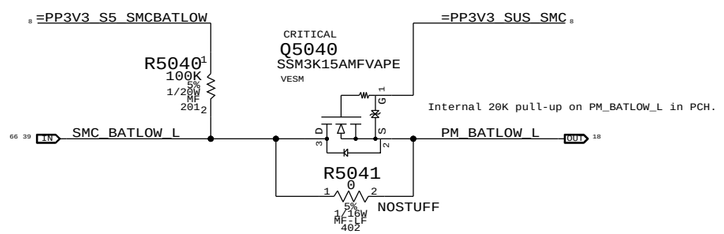


SMC12 SPI SUPPORT

SERIES RESISTORS ARE NO STUFFED UNTIL THE TOPOLOGY OF 2 SPI MASTERS IS VERIFIED



BATLOW# ISOLATION



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE

SMC Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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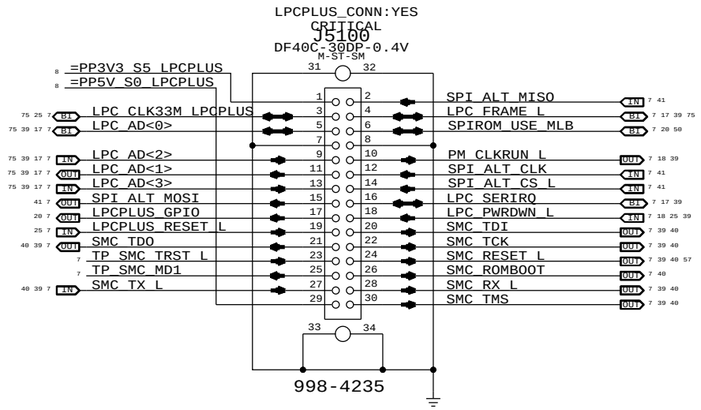
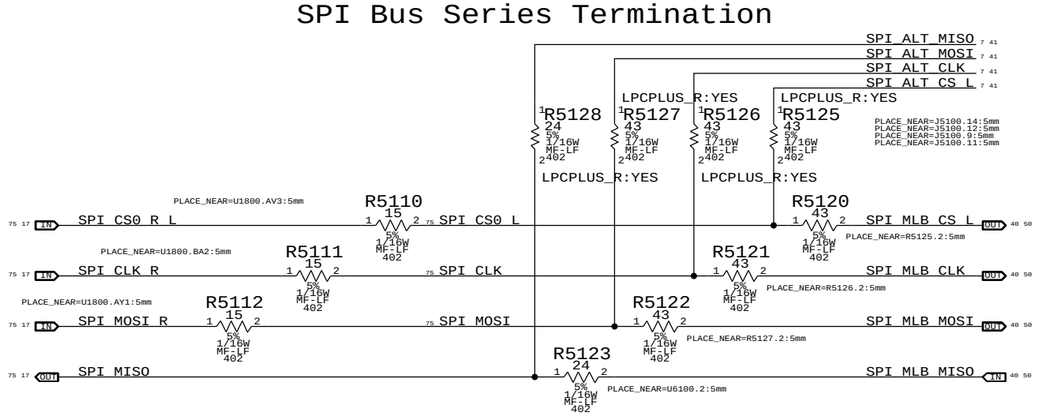
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE

LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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PCH SMBus "0" Connections

=PP3V3_S0_SMBUS_PCH

Panther Point
U1800
(MASTER)
SMBUS_PCH_CLK (MAKE_BASE=TRUE)
SMBUS_PCH_DATA (MAKE_BASE=TRUE)

R5200 1K 5% 1/20W MF 201
R5201 1K 5% 1/20W MF 201

TBT
U3600
(WRITE: 0XX READ: 0XX)
=I2C_TBTRTR_SCL
=I2C_TBTRTR_SDA

VRef DACs
U3300
(Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA

AUDIO
U6411
(WRITE: 0X34 READ: 0X35)

Margin Control
U3301
(Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA

AUDIO
U6410
(WRITE: 0X32 READ: 0X33)

MIKEY
U6751
(WRITE: 0X72 READ: 0X73)
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA

AUDIO
U6400
(WRITE: 0XE0 READ: 0XE1)

XDP Connectors
J2500 & J2550
(MASTER)
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA

AUDIO
U6750
(WRITE: 0X76 READ: 0X77)

HDMI Redriver (on RIO)
J4410
(WRITE: 0xCC READ: 0xCD)
=I2C_HDMIRDRV_SCL
=I2C_HDMIRDRV_SDA

LED BACKLIGHT
U9700
(WRITE: 0X58 READ: 0X59)
=I2C_BKL_1_SCL
=I2C_BKL_1_SDA

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

SMC
U4900
(MASTER)
SMB_0_S0_CLK
SMB_0_S0_DATA

R5250 4.7K 5% 1/20W MF 201
R5251 4.7K 5% 1/20W MF 201

SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)
=SMBUS_GPUTHMSNS_SCL
=SMBUS_GPUTHMSNS_SDA

SMC "2" SMBUS CONNECTIONS

NOTE: SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_2_S3

SMC
U4900
(MASTER)
SMB_2_S3_CLK
SMB_2_S3_DATA

R5270 1K 5% 1/20W MF 201
R5271 1K 5% 1/20W MF 201

SMBUS_SMC_2_S3_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_2_S3_SDA (MAKE_BASE=TRUE)

Trackpad
J5800
(Write: 0x90 Read: 0x91)
=I2C_TPAD_SCL
=I2C_TPAD_SDA

ALS
J3502
(Write: 0x72 Read: 0x73)
=I2C_ALS_SCL
=I2C_ALS_SDA

SMS
U5920
(WRITE: 0X30/31 READ: 0X32/33)
=I2C_SMC_SMS_SCL
=I2C_SMC_SMS_SDA

GYRO
U5940
(WRITE: 0XD0 READ: 0XD1)
=I2C_SMC_GYRO_SCL
=I2C_SMC_GYRO_SDA

SMC "1" SMBUS CONNECTIONS

=PP3V3_S0_SMBUS_SMC_1_S0

SMC
U4900
(MASTER)
SMB_1_S0_CLK
SMB_1_S0_DATA

R5260 1K 5% 1/20W MF 201
R5261 1K 5% 1/20W MF 201

SMBUS_SMC_1_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_1_S0_SDA (MAKE_BASE=TRUE)

CPU/DDR3/PCH/AIRFLOW TEMP
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)
=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA

PCH "SMLink 1" Connections

Panther Point
U1800
(Write: 0x88 Read: 0x89)
SML_PCH_1_CLK
SML_PCH_1_DATA

SMLink 1 is slave port to access PCH & CPU via PECI.

X29 TEMP
TMP105: U5523
(WRITE: 0X92 READ: 0X93)
=I2C_X29THMSNS_SCL
=I2C_X29THMSNS_SDA

SPKR TEMP
U6420
(WRITE: 0XD8 READ: 0XD9)
U6421
(WRITE: 0X38 READ: 0X39)
=I2C_SPKRTHMSNS_SCL
=I2C_SPKRTHMSNS_SDA

SMC "5" SMBUS CONNECTIONS

=PP3V42_G3H_SMBUS_SMC_5

SMC
U4900
(MASTER)
SMB_5_CLK
SMB_5_DATA

R5280 2.0K 5% 1/20W MF 201
R5281 2.0K 5% 1/20W MF 201

SMBUS_SMC_5_G3_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_5_G3_SDA (MAKE_BASE=TRUE)

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA

Battery
J6955
(See Table)
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA

Battery
Battery Manager - (Write: 0x16 Read: 0x17)

SMC "3" SMBUS CONNECTIONS

=PP3V3_S3_SMBUS_SMC_3

SMC
U4900
(MASTER)
SMB_3_CLK
SMB_3_DATA

DEBUG_ADC
R5290 4.7K 5% 1/20W MF 201
DEBUG_ADC
R5291 4.7K 5% 1/20W MF 201

SMBUS_SMC_3_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_3_SDA (MAKE_BASE=TRUE)

DEBUG SENSOR ADC A
UD000
(Write: 0x10 Read: 0x11)
=I2C_SMC_ADCS_SCL
=I2C_SMC_ADCS_SDA

PCH "SMLink 0" Connections

=PP3V3_S0_SMBUS_PCH

Panther Point
U1800
(MASTER)
SML_PCH_0_CLK (MAKE_BASE=TRUE)
SML_PCH_0_DATA (MAKE_BASE=TRUE)

R5210 8.2K 5% 1/20W MF 201
R5211 8.2K 5% 1/20W MF 201

SYNC_MASTER=MASTER
SYNC_DATE=MASTER
PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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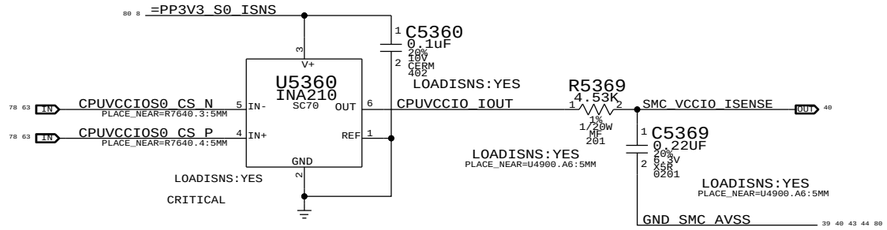
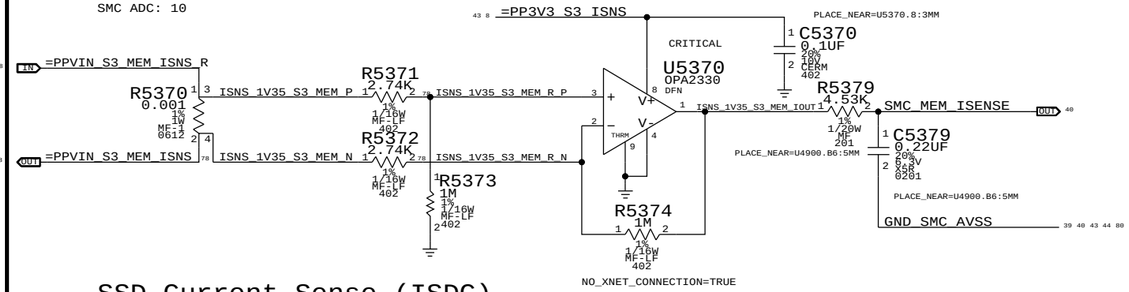
CPU/PCH VCCIO & TBT 1.05V Load Side Current Sense (IC1C)

Gain: 200x, EDP: 20 A
Rsense: 0.001 (R7640)
V across Rsense: 15 mV
SMC ADC: 11



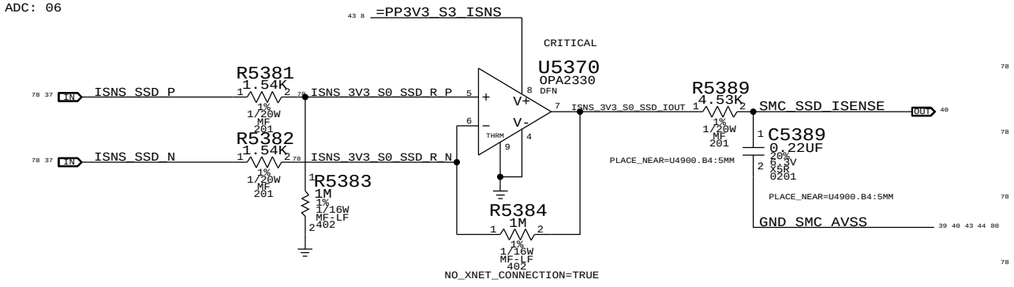
DDR 1.35V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
SMC ADC: 10



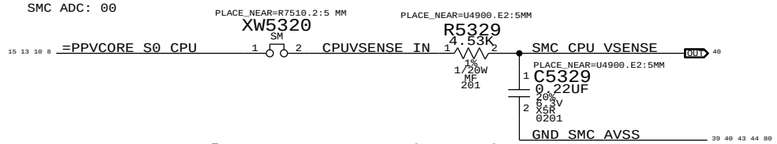
SSD Current Sense (ISDC)

Gain: 649.35x, EDP: 5 A (16.5 W)
Rsense: 0.001 (R5370)
V across Rsense: 5 mV
SMC ADC: 06



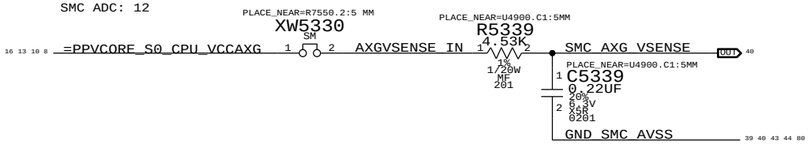
CPU Core Voltage Sense (VC0C)

Gain: 1x
SMC ADC: 00



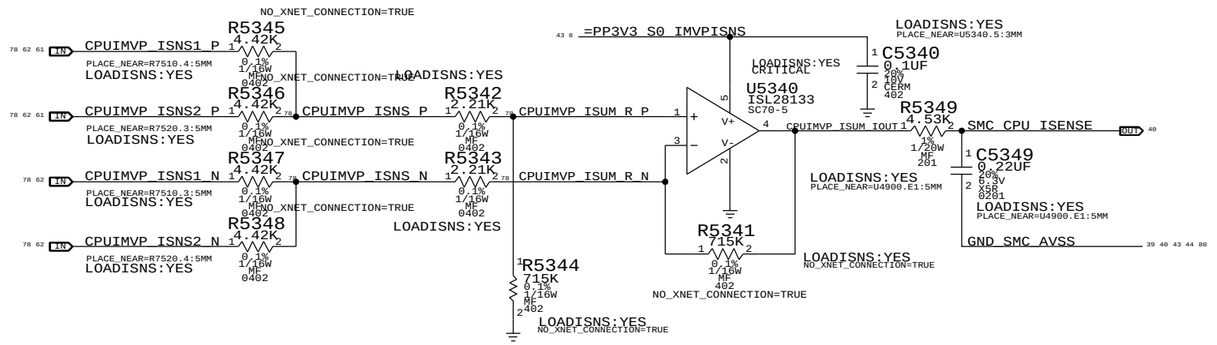
AXG Core Voltage Sense (VN0C)

Gain: 1x
SMC ADC: 12



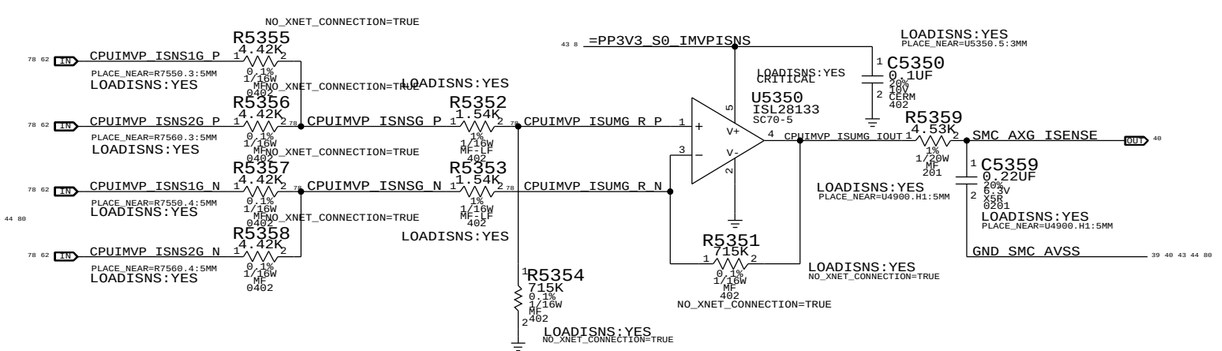
CPU Core Load Side Current Sense (IC0C)

Gain: 161.7x, EDP: 53 A
Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375
V across Rsense: 19.8 mV
SMC ADC: 01



AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375
V across Rsense: 17.25 mV
SMC ADC: 18



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE
Power Sensor: Load Side

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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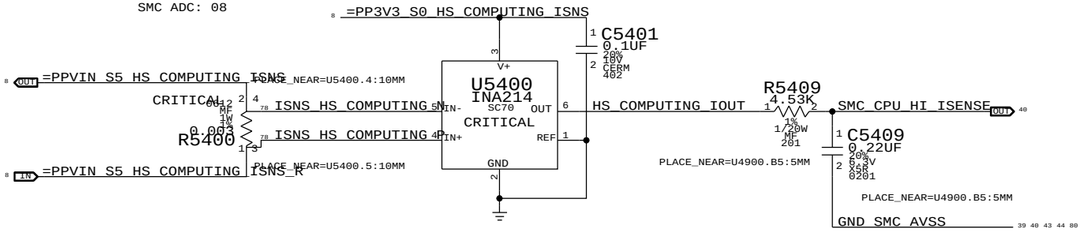
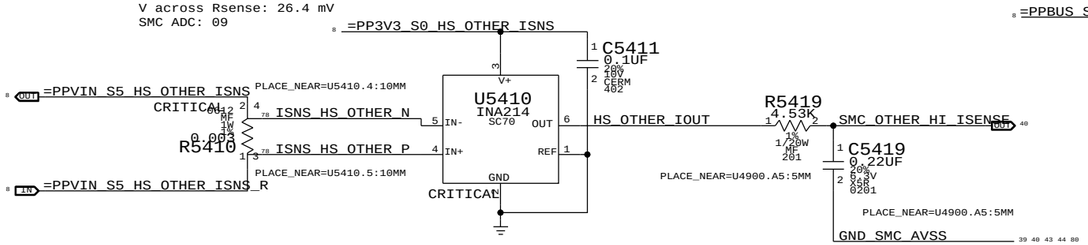
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
Rsense: 0.003 (R5400)
V across Rsense: 52.2 mV
SMC ADC: 08



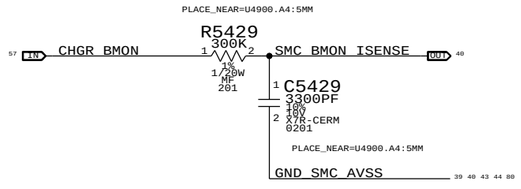
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
Rsense: 0.003 (R5410)
V across Rsense: 26.4 mV
SMC ADC: 09



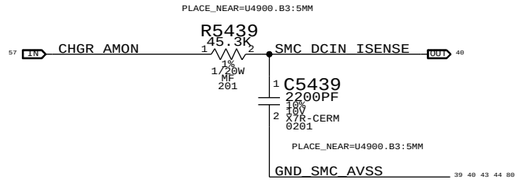
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x, EDP: 6.6 A
Rsense: 0.010 (R7050)
SMC ADC: 07



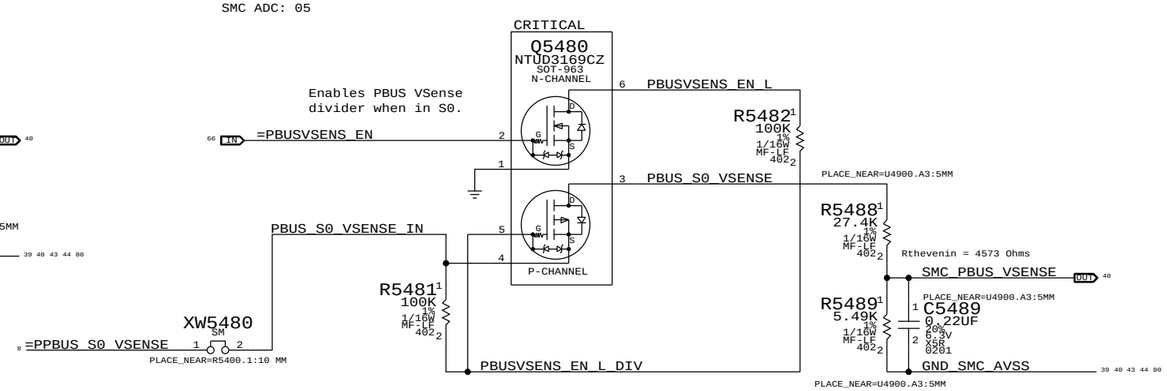
DC-In (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7020)
SMC ADC: 04



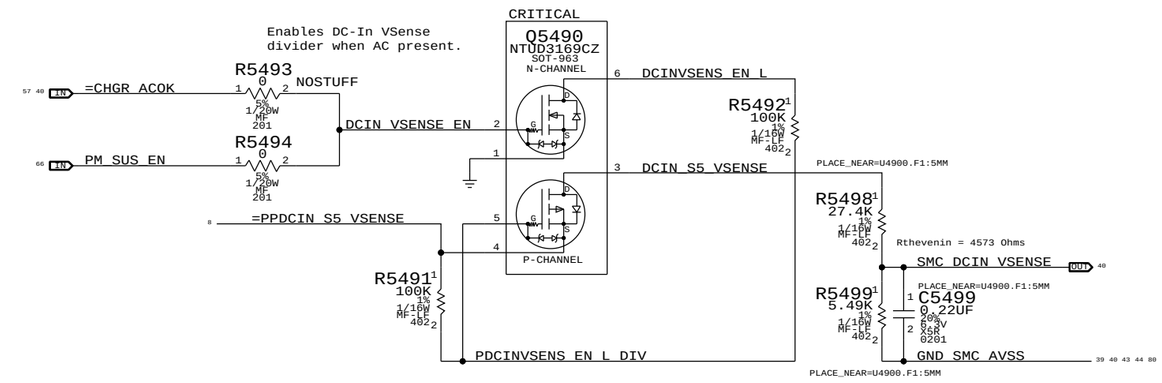
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
SMC ADC: 05



DC In Voltage Sense & Enable (VD0R)

Gain: 0.167x
SMC ADC: 03



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE
Power Sensor: High Side

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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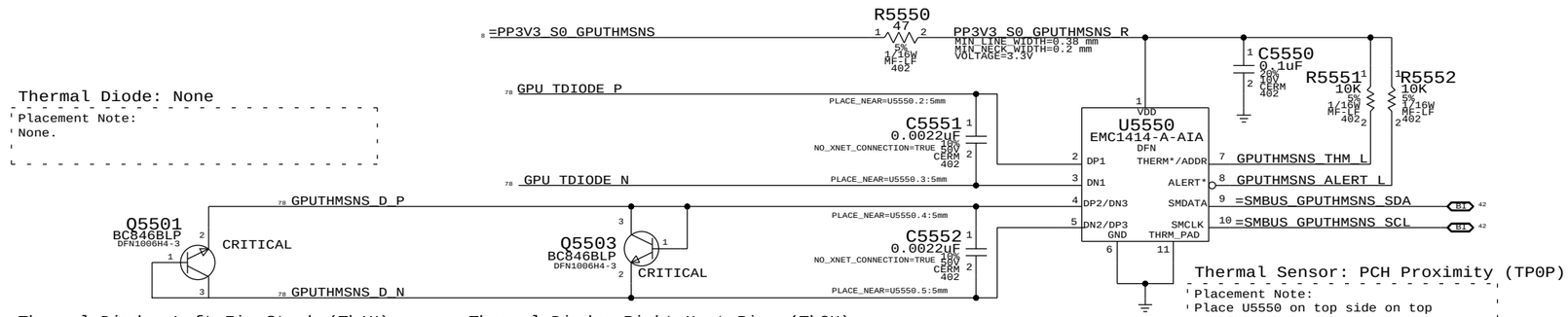
SHEET 44 OF 80

Thermal Sensor A:
PCH Proximity, Left Fin Pipe, Right Fin Stack

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: None

Placement Note:
None.

Thermal Diode: Left Fin Stack (Th1H)

Placement Note:
Place Q5501 on the top side on the corner close to the Left Fin Stack.

Thermal Diode: Right Heat Pipe (Th2H)

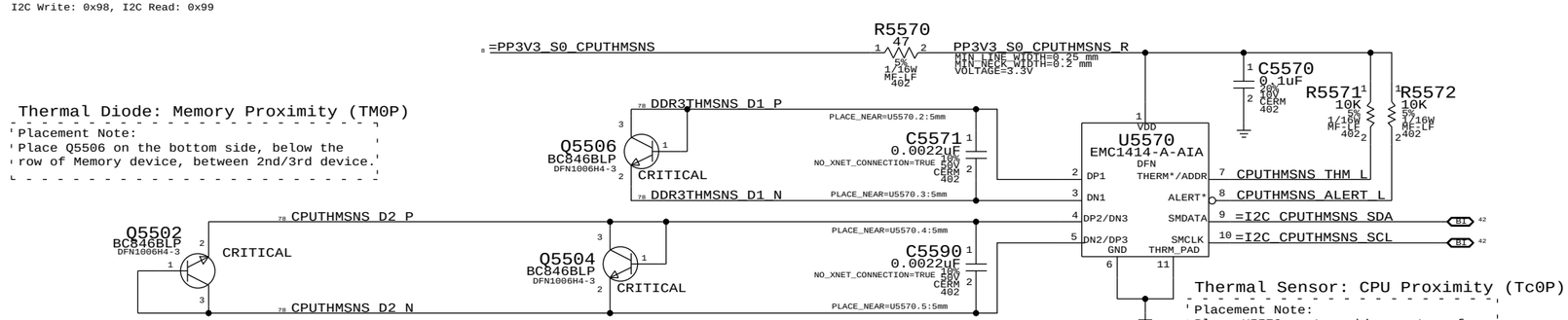
Placement Note:
Place Q5503 under the top side on the corner close to the Right Fin Stack.

Thermal Sensor: PCH Proximity (TP0P)

Placement Note:
Place U5550 on top side on top of PCH.

Thermal Sensor B:
CPU Proximity, Memory Proximity, Airflow

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: Memory Proximity (TM0P)

Placement Note:
Place Q5506 on the bottom side, below the row of Memory device, between 2nd/3rd device.

Thermal Diode: Airflow (TA0P)

Placement Note:
Place Q5502 on the bottom side, below left underneath the left fan well in the neck.

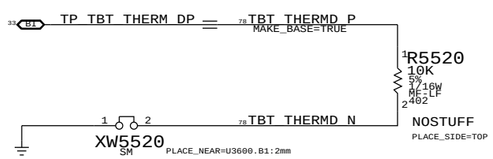
Thermal Diode: Airflow (TA1P)

Placement Note:
Place Q5504 on the either side, near LCD connector and DCIN connector.

Thermal Sensor: CPU Proximity (Tc0P)

Placement Note:
Place U5570 on top side, on top of the CPU.

Thermal Sensor: T29 Die



Note: Use GND pin B1 on U3600 for N leg.

SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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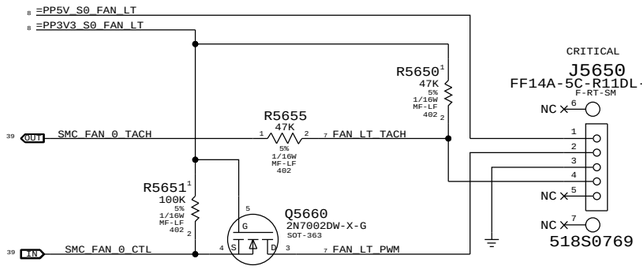
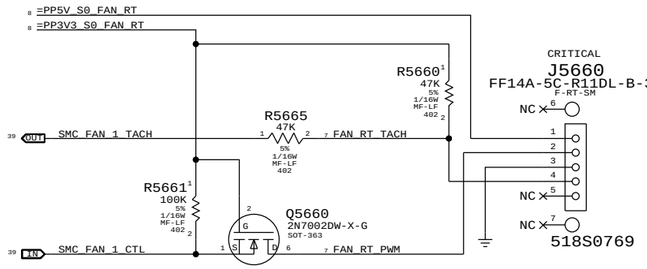
Left Fan



Right Fan



SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE

Fan Connectors

Apple Inc.

DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
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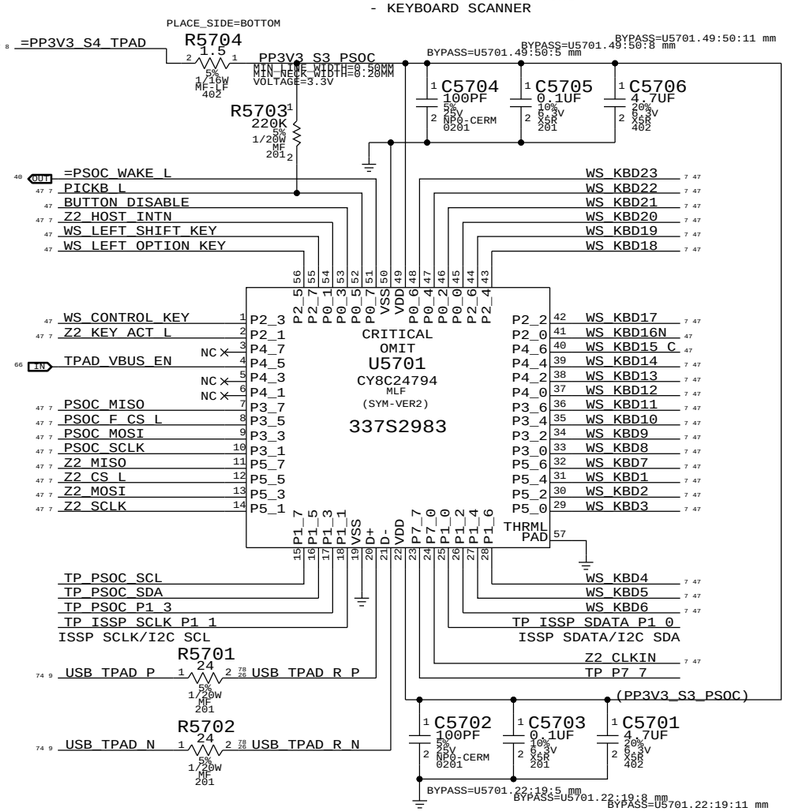
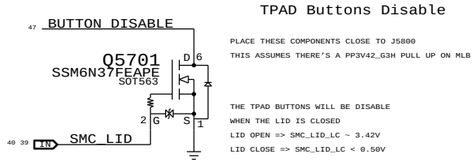
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

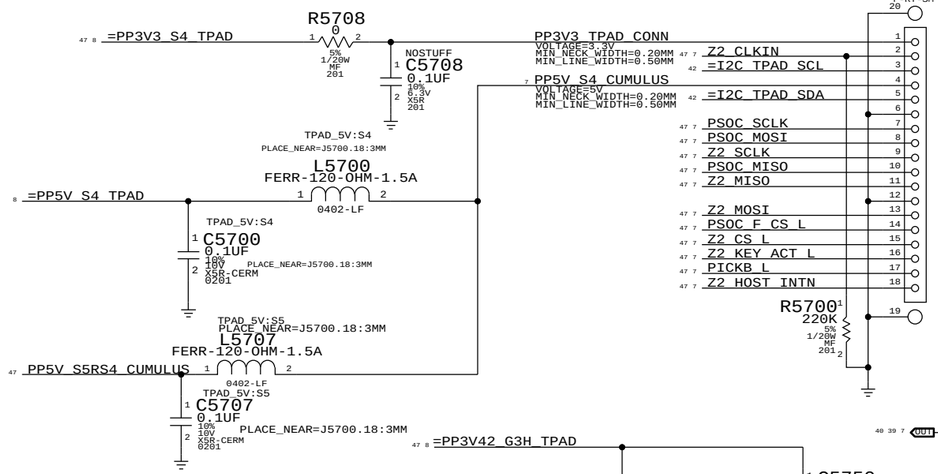


TPAD Buttons Disable

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

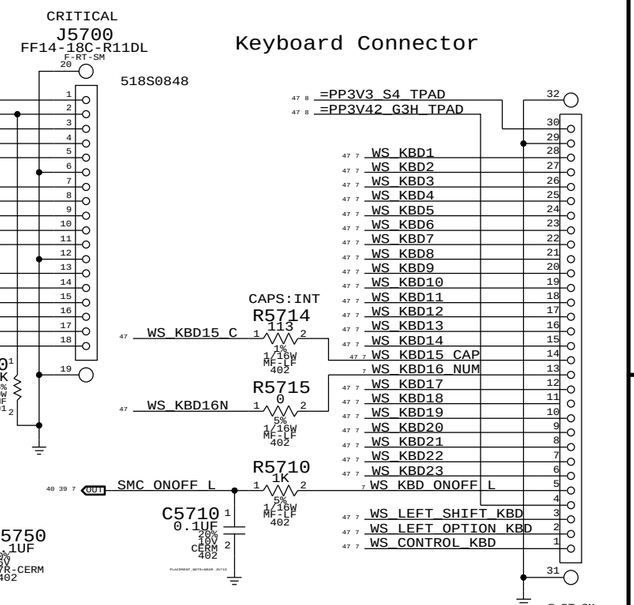
THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

IPD Flex Connector



www.qdzbwx.com

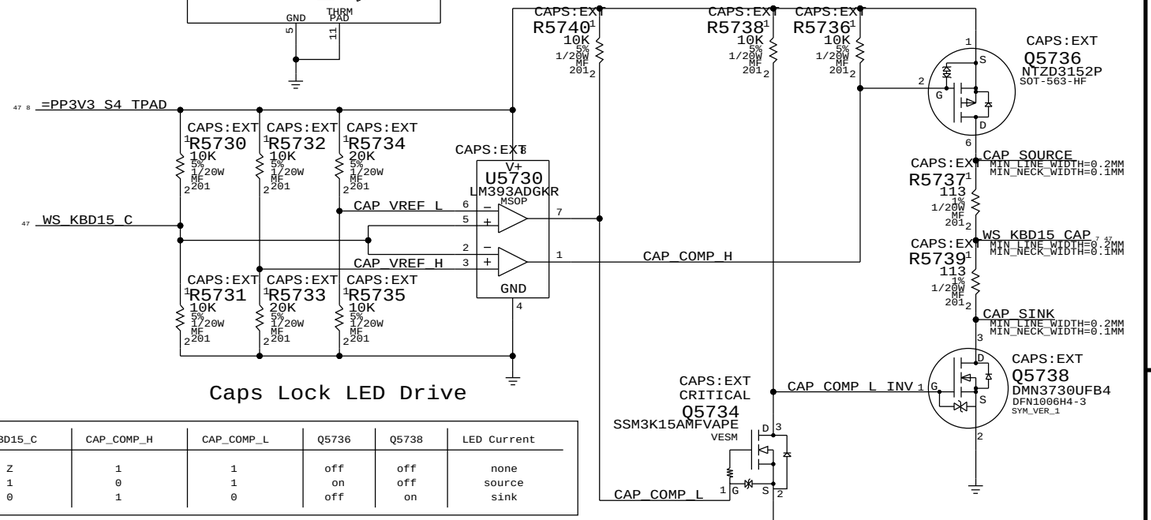
Keyboard Connector



SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with MSP power to isolate when MSP is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

Caps Lock LED Drive

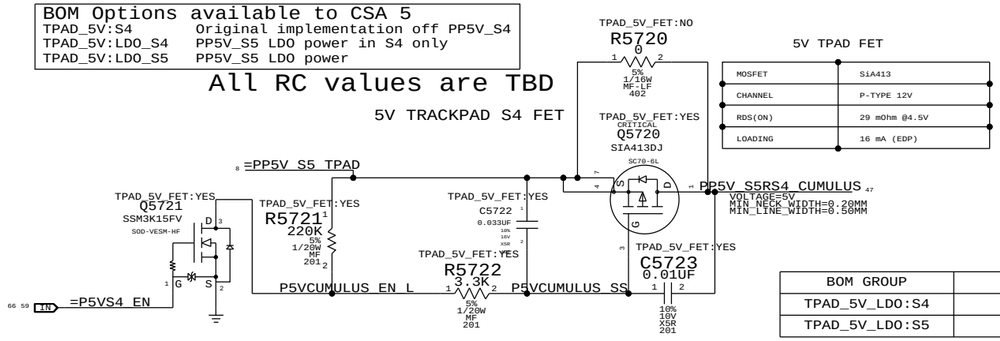


WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink

BOM Options available to CSA 5	
TPAD_5V:S4	Original implementation off PP5V_S4
TPAD_5V:LDO_S4	PP5V_S5 LDO power in S4 only
TPAD_5V:LDO_S5	PP5V_S5 LDO power

All RC values are TBD

5V TRACKPAD S4 FET



5V TPAD FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	16 mA (EDP)

BOM GROUP	BOM OPTIONS
TPAD_5V_LDO:S4	TPAD_5V_FET:YES,TPAD_5V:S5
TPAD_5V_LDO:S5	TPAD_5V_FET:NO,TPAD_5V:S5

SYNC_MASTER=D2_MLB_KEPLER
SYNC_DATE=12/08/2011

PAGE TITLE

KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
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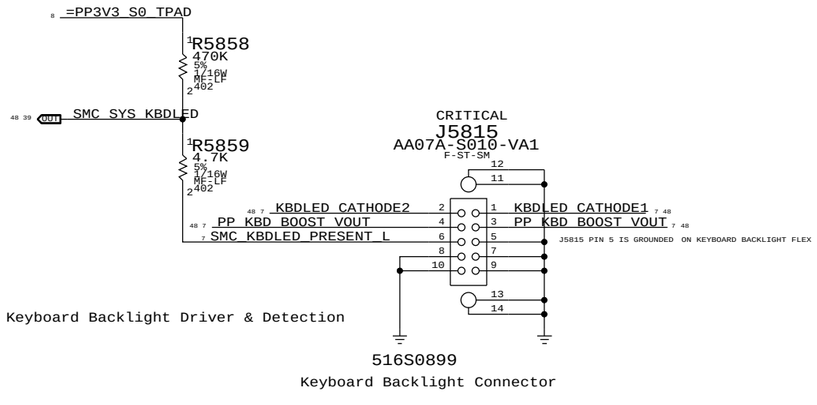


Keyboard Backlight Driver & Detection

To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

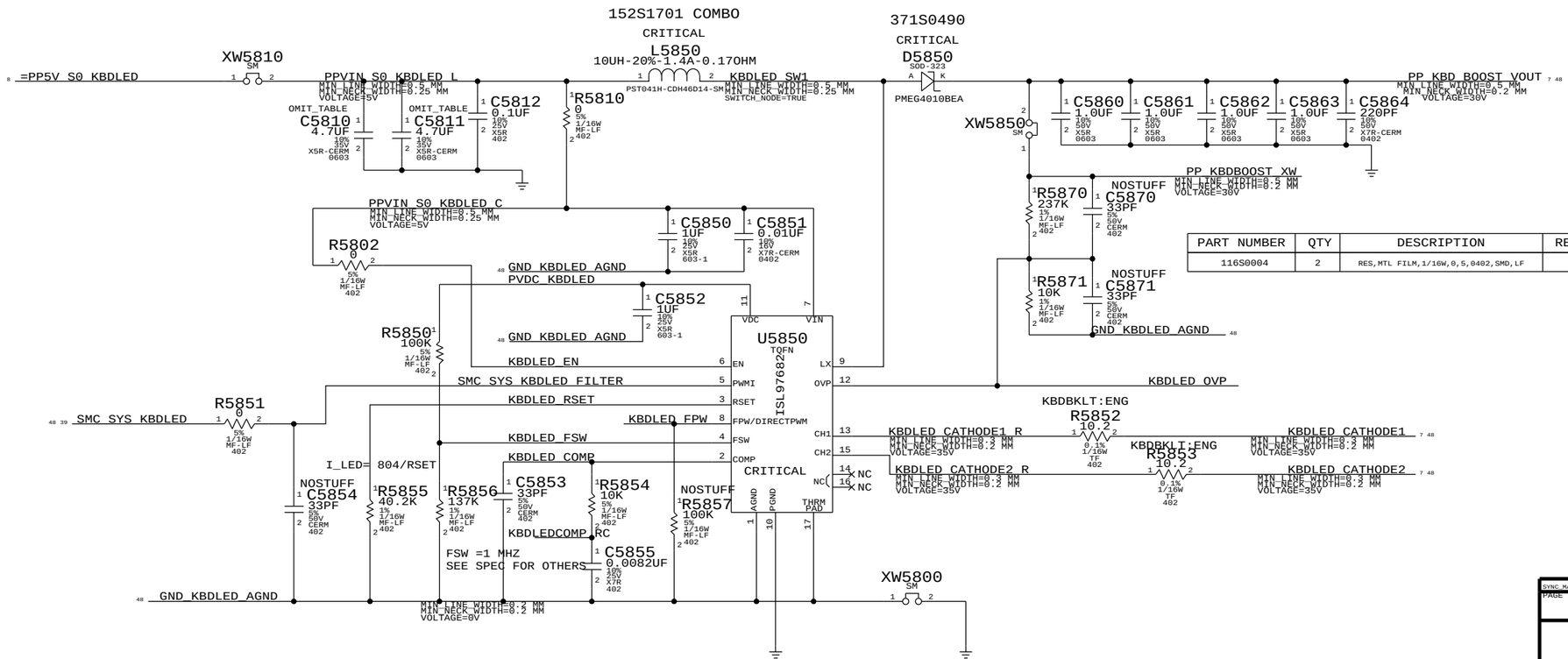
If LOW, keyboard backlight present

If HIGH, keyboard backlight not present

516S0899

Keyboard Backlight Connector

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	2	CAP,CER,4.7UF,10%,25V,X6S,0603	C5810,C5811	CRITICAL	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,1/16W,0,5,0402,SMD,LF	R5852,R5853	CRITICAL	KBDBKLT:PROD

SYNC_MASTER=D2_MLB_KEPLER SYNC_DATE=12/08/2011

PAGE TITLE

KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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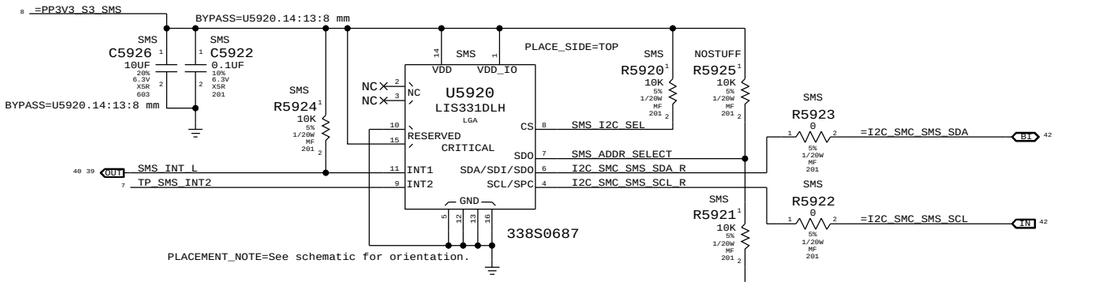

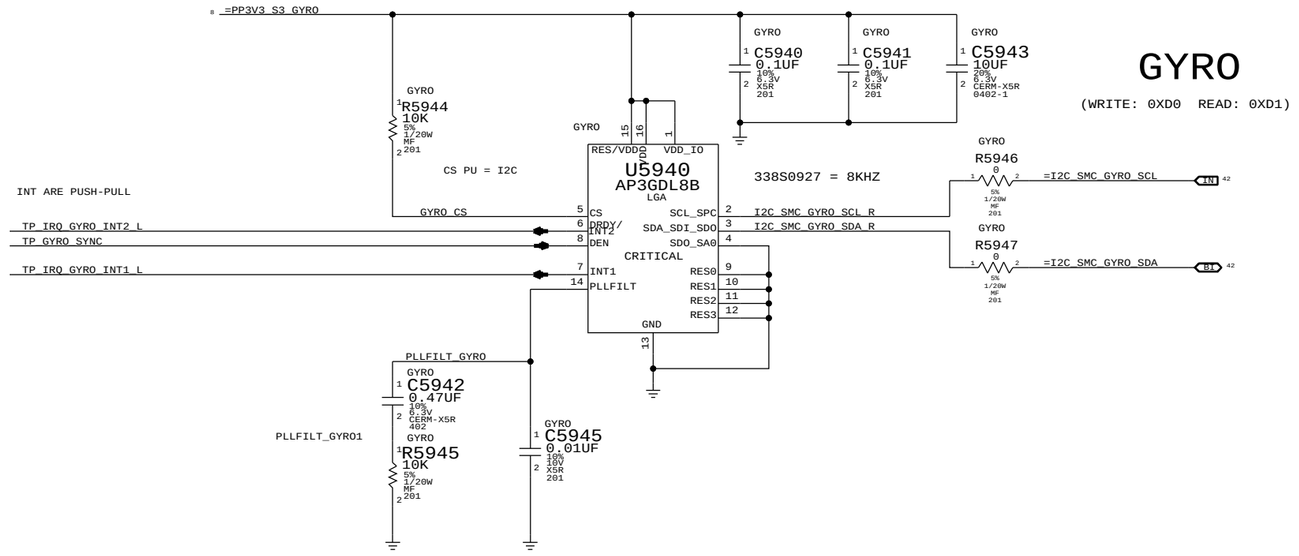

GYRO

(WRITE: 0XD0 READ: 0XD1)

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE: DIGITAL ACCELEROMETER & GYRO

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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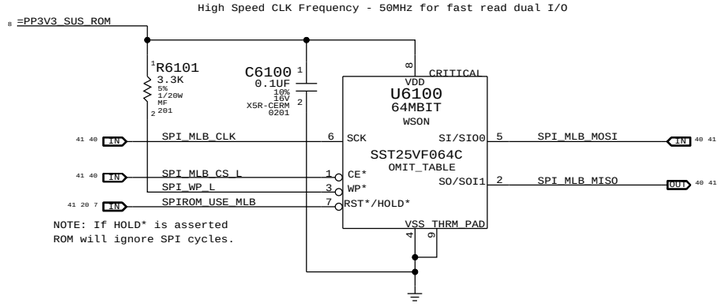
DUAL I/O MODE (MODE 0 & 3) SUPPORTED
High Speed CLK Frequency - 50MHz for fast read dual I/O



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles.

SYNC_MASTER=J13_MLB SYNC_DATE=01/20/2012

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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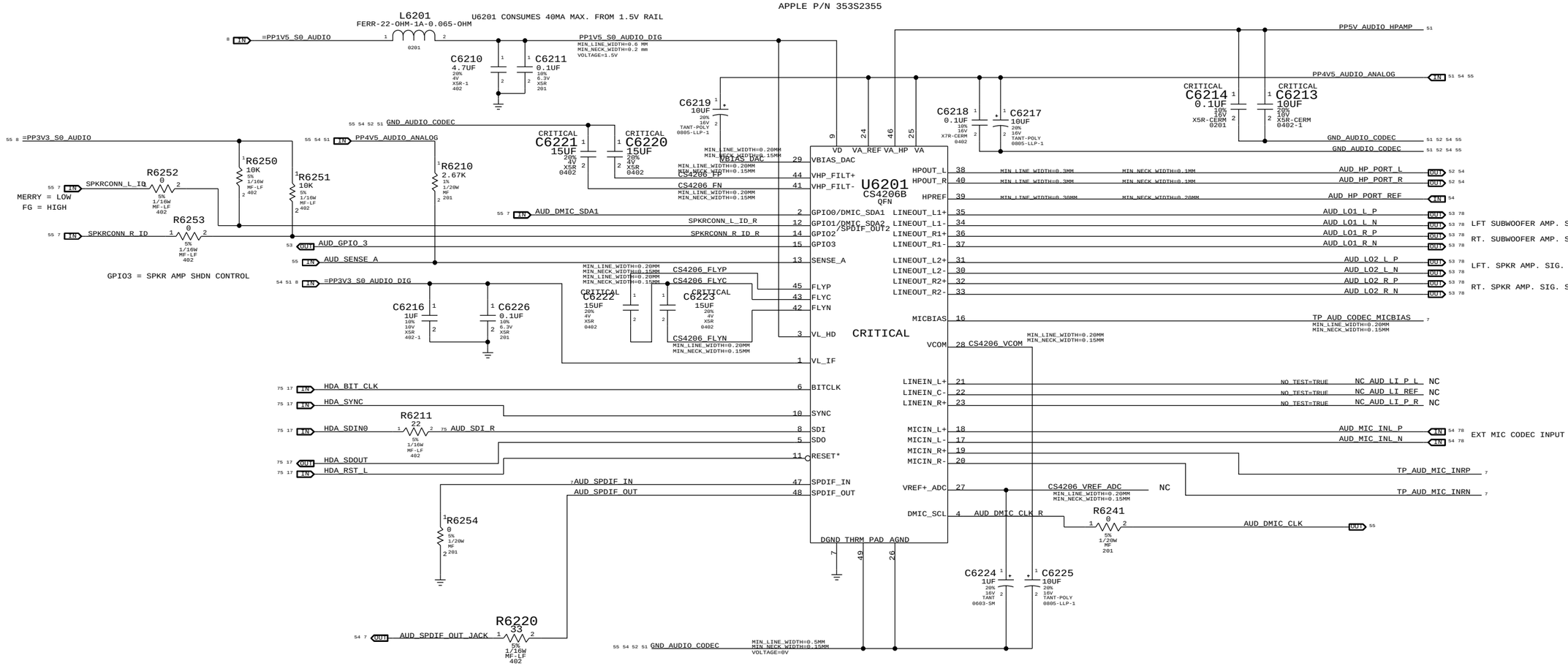
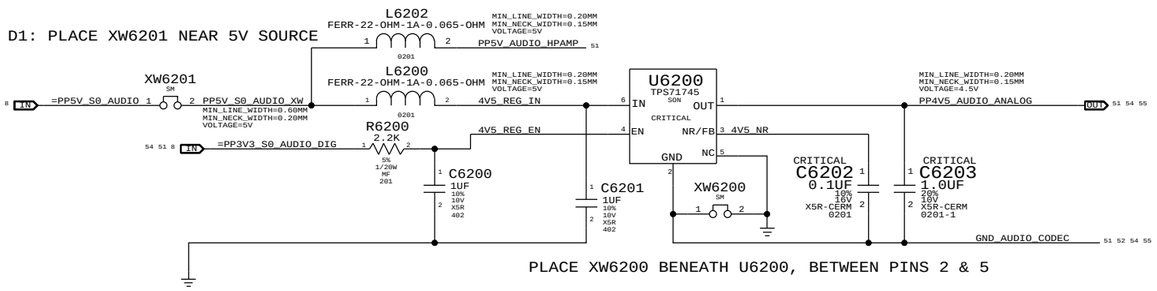
AUDIO CODEC

APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012

PAGE TITLE

AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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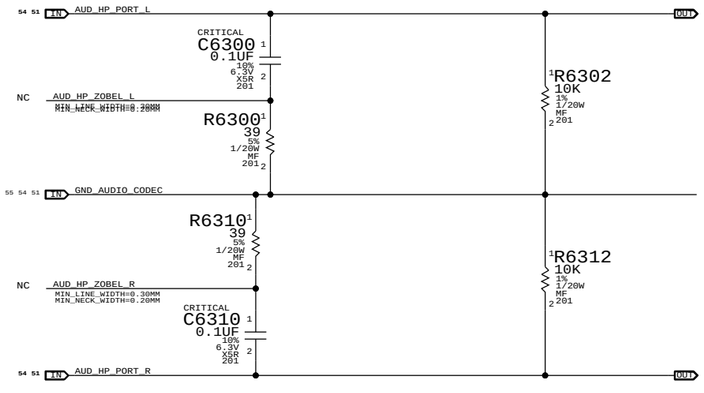
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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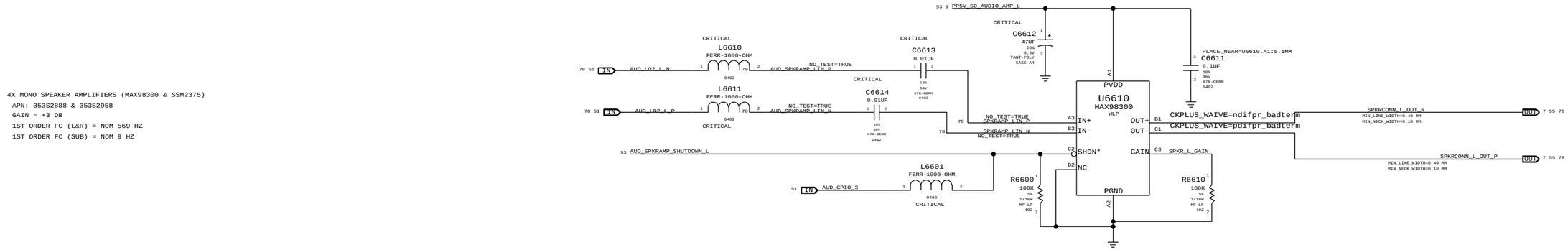
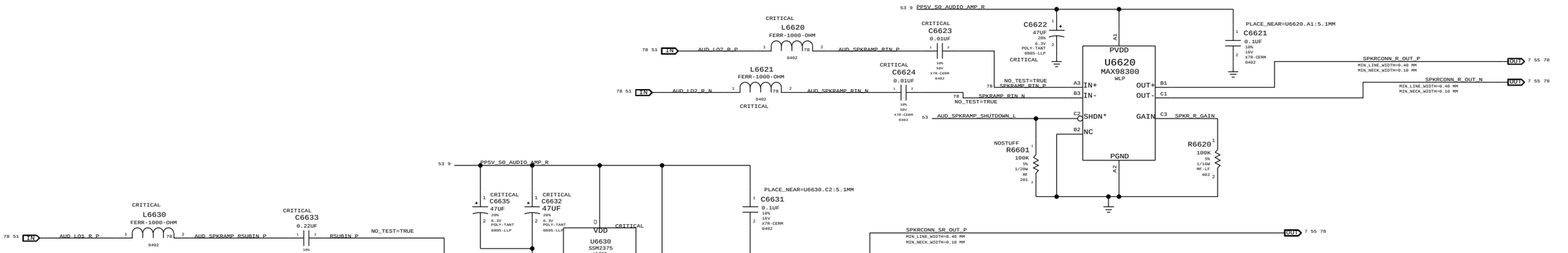
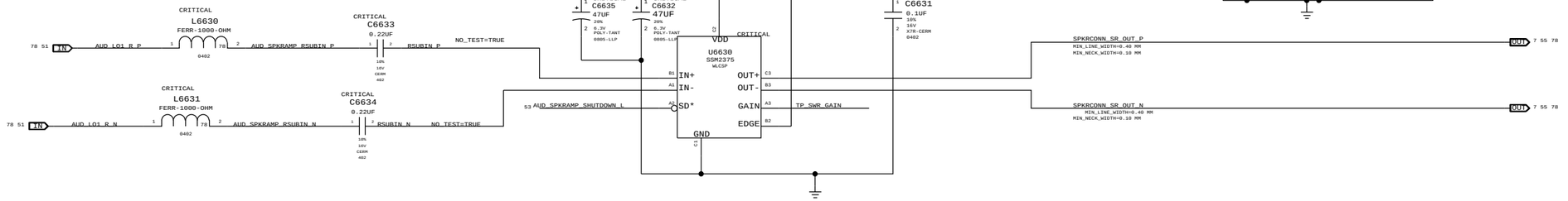
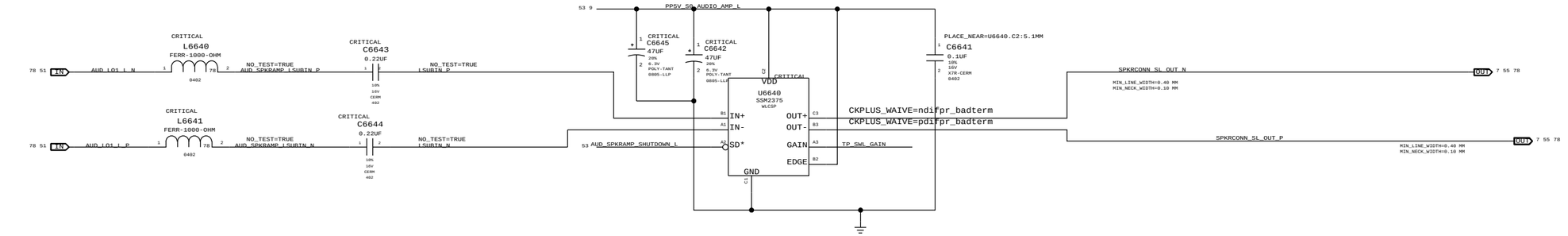
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2013

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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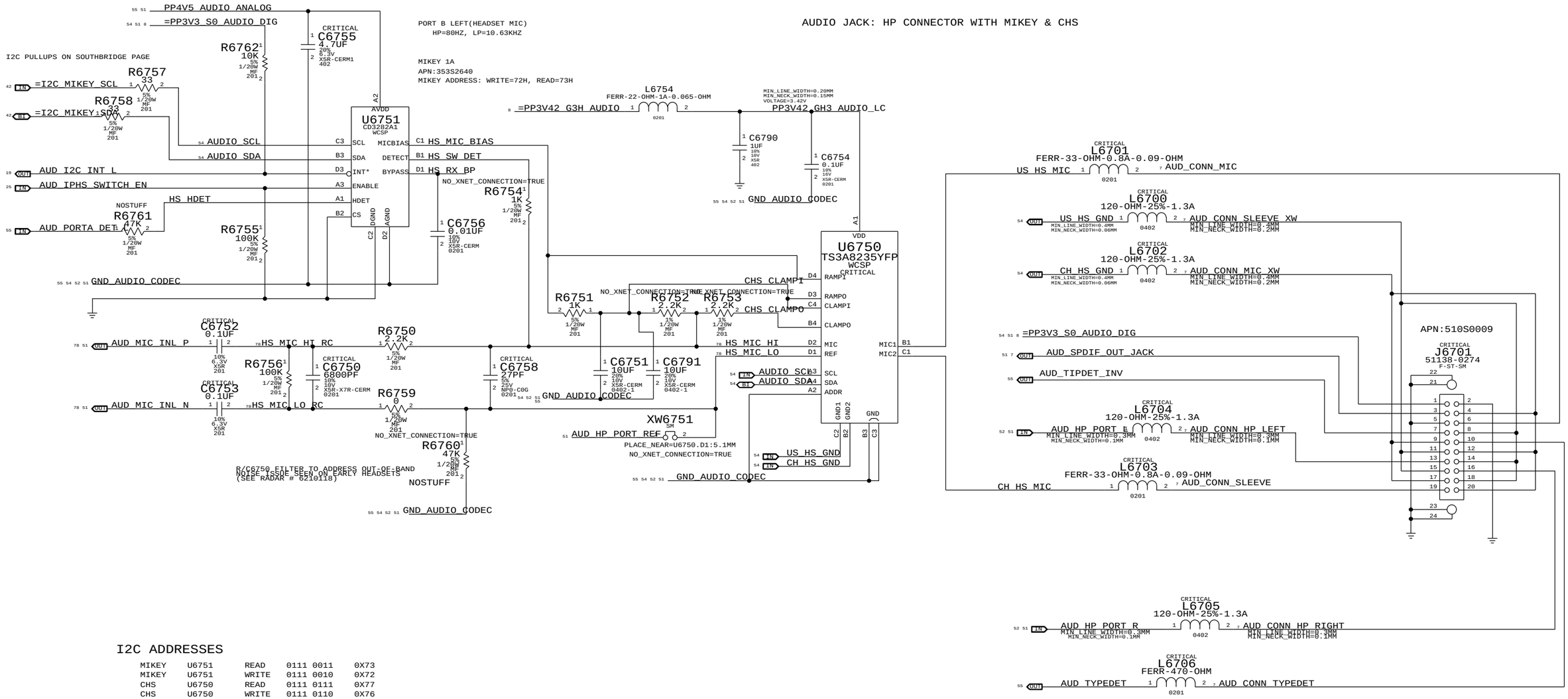
AUDIO JACK: HP CONNECTOR WITH MIKEY & CHS

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=10.63KHZ

MIKEY 1A
APN:353S2640
MIKEY ADDRESS: WRITE=72H, READ=73H

I2C PULLUPS ON SOUTHBRIDGE PAGE



I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012

PAGE TITLE: AUDIO: JACK

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (B)
TWEETERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (A)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
DMIC 1	0X06 (6)	0X0E (0,E)	3V3	N/A
DMIC2	0X05 (5)	0X12 (12,C)	3V3	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

2-MIC CONNECTOR

MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.15MM
VOLTAGE=3.3V

55 51 8 =PP3V3_S0_AUDIO
R6885 0 5% 1/16W MF-LF 402
CON_DMIC_PWR
51 7 OUT AUD_DMIC_SDA1
R6884 0 5% 1/16W MF-LF 402
CON_DMIC_SDA1
51 OUT AUD_DMIC_CLK
R6883 0 5% 1/16W MF-LF 402
CON_DMIC_CLK

CRITICAL
J6801
FF14A-6C-R11DL-B-3H
F-RT-SM
NC 7
NC 8

SPEAKER CONNECTOR

HP=80HZ

APN: 518S0627

CRITICAL
J6802
78171-6006
M-RT-SM

78 53 7 IN SPKRCONN_L_OUT_P
78 53 7 IN SPKRCONN_L_OUT_N
55 51 7 OUT SPKRCONN_L_ID
78 53 7 IN SPKRCONN_SL_OUT_P
78 53 7 IN SPKRCONN_SL_OUT_N

CRITICAL
J6803
78171-6006
M-RT-SM

78 53 7 IN SPKRCONN_R_OUT_P
78 53 7 IN SPKRCONN_R_OUT_N
55 51 7 OUT SPKRCONN_R_ID
78 53 7 IN SPKRCONN_SR_OUT_P
78 53 7 IN SPKRCONN_SR_OUT_N

PORT B DETECT(SPDIF DELEGATE)

55 51 OUT AUD_SENSE_A
R6896 20.0K 1% 1/16W MF-LF 2402
AUD_PORTA_DET_L 54
Q6897 SSM6N15AFE SOT563
55 IN AUD_OUTJACK_INSERT_L

PORT A DETECT (HEADPHONES)

R6895 39.2K 1% 1/16W MF-LF 2402
AUD_PORTB_DET_L NC
Q6897 SSM6N15AFE SOT563

55 54 52 51 GND_AUDIO_CODEC
R6802 100K 5% 1/20W MF 201
AUD_TYPEDET_OD 55

PP4V5_AUDIO_ANALOG
R6801 150K 1% 1/20W MF 201
Q6800 DMC2400UV SOT563 P-CHN
AUD_TYPEDET 54

55 54 51 PP4V5_AUDIO_ANALOG
R6803 100K 5% 1/20W MF 201
AUD_TYPEDET_OD_INV
C6800 0.1UF 10% 6.3V X5R 201
PLACE_NEAR=Q6800.4:5.1MM
Q6800 DMC2400UV SOT563 N-CHN
AUD_TYPEDET_OD IN 55
PP4V5_AUDIO_ANALOG 51 54 55
GND_AUDIO_CODEC 51 52 54 55

55 8 =PP5V_S4_AUDIO
SPEAKERID R6810 100K 1% 1/16W MF-LF 402
SPEAKERID R6811 100K 1% 1/16W MF-LF 402
55 51 7 IN SPKRCONN_L_ID
SPKRCONN_R_ID IN 7 51 55
R6812 100K 1% 1/16W MF-LF 402
R6813 100K 1% 1/16W MF-LF 402

SPEAKERID R6816 100K 1% 1/16W MF-LF 402
55 8 =PP5V_S4_AUDIO
SPEAKERID C6810 0.1UF 10% 6.3V X5R 201
SPEAKERID CRITICAL U6800 MCP6541T SC70-5
MCP6514_POS 3
MCP6514_NEG 4
MCP6514_OUT 1
SPEAKERID L6802 FERR-1000-OHM 0402
SPKR_MATCH_DRV_R 1
SPEAKERID R6820 33 5% 1/16W MF-LF 402
SPKR_MATCH_DRV 2

55 8 =PP5V_S4_AUDIO
SPEAKERID R6814 274K 1% 1/16W MF-LF 402
SPEAKERID R6815 90.9K 1% 1/16W MF-LF 402
SPEAKERID C6811 4.7UF 20% 10V X5R-CERM 0402
SPEAKERID R6817 45.3K 1% 1/16W MF-LF 402

PORT C DETECT(SPEAKER MISMATCH)

55 51 OUT AUD_SENSE_A
SPEAKERID R6894 10K 1% 1/16W MF-LF 402
NC AUD_PORTC_DET_L
SPEAKERID Q6896 SSM6N15AFE SOT563
55 54 52 51 GND_AUDIO_CODEC

55 51 8 =PP3V3_S0_AUDIO
R6867 0 5% 1/16W MF-LF 402
AUD_IP_PERIPHERAL_DET OUT 19
EXTRACTION NOTIFICATION
R6865 47K 5% 1/20W MF 201
R6866 475K 1% 1/20W MF 201
APN:376S0613
AUD_TIPDET_FET1
AUD_OUTJACK_INSERT_L OUT 55
Q6803 SSM6N15AFE SOT563
54 IN AUD_TIPDET_INV
R6892 1.5K 1% 1/10W MF-LF 402
AUD_TIPDET_INV_R
C6860 1UF 10% 25V X5R 402
CRITICAL
L6801 FERR-33-OHM-0.8A-0.09-OHM 0201
AUD_TIPDET_FET2
C6891 1UF 10% 25V X5R 402
55 54 52 51 GND_AUDIO_CODEC

NOM R6892-C6860 FC = 106Hz
SSM6N15FE Vth = 0.8V to 1.5V
SSM6N15FE IGSS = +/-1uA
FLEX-SIDE RPULLDOWN = 100k (TB 49.9k in REV 3)

AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV

Alternate Parts

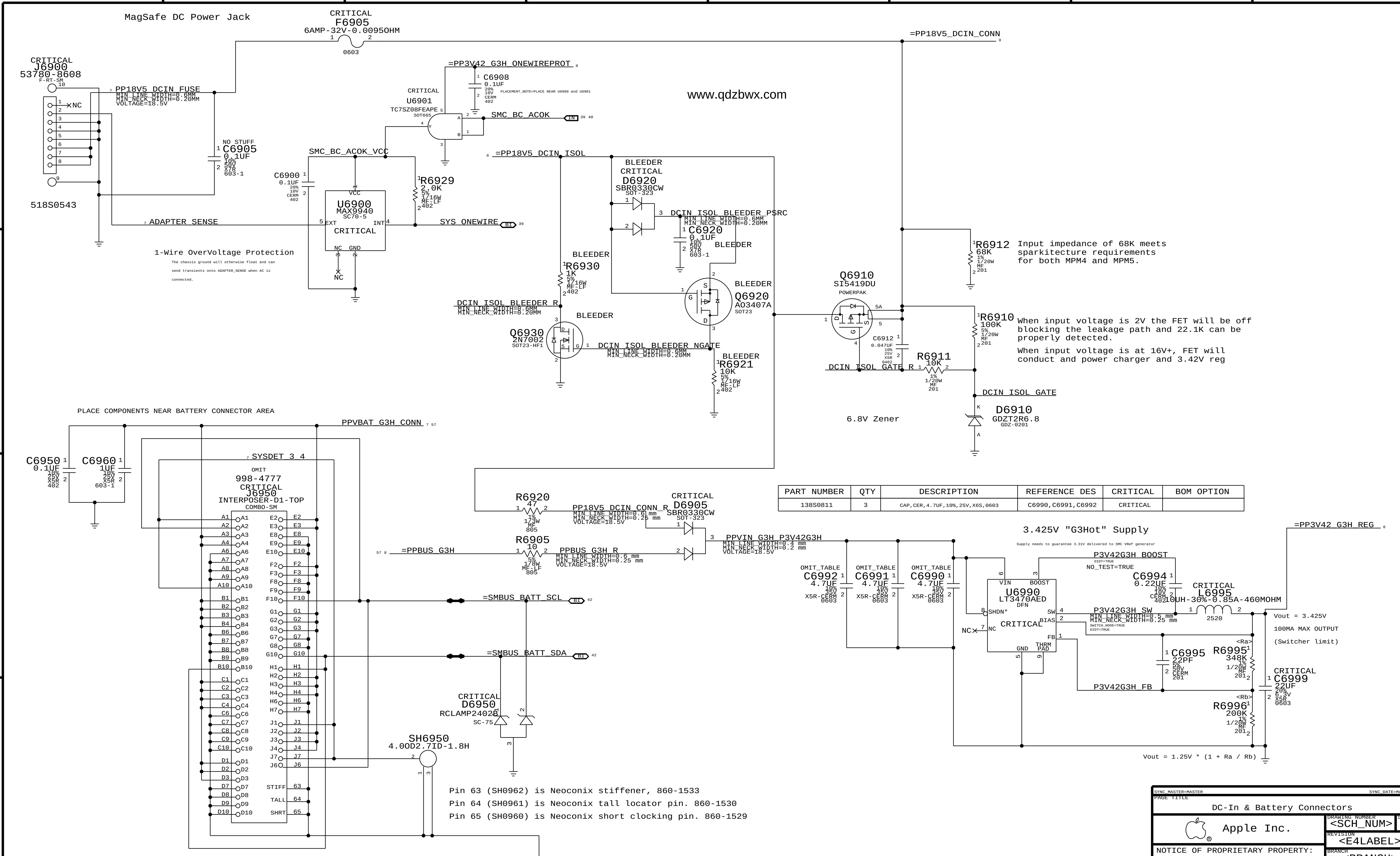
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S3452	353S1286		U6800	MAXIM ALT TO MICROCHIP
376S0975	376S1081		Q6800	TOSHIBA ALT TO DIODES

SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012

PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 68 OF 132
SHEET 55 OF 80


MagSafe DC Power Jack
CRITICAL
F6905
6AMP-32V-0.0095OHM
0603
CRITICAL
J6900
53780-8608
F-RT-SM
PP18V5_DCIN_FUSE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=18.5V
NO_STUFF
C6905
0.1UF
518S0543
=PP18V5_DCIN_CONN
=PP3V42_G3H_ONEWIREPROT
C6908
0.1UF
PLACEMENT_NOTE=PLACE NEAR U6900 and U6901
CRITICAL
U6901
TC7SZ08FEAPE
SOT665
SMC_BC_ACOK
www.qdzbwx.com
SMC_BC_ACOK_VCC
C6900
0.1UF
U6900
MAX9940
SC70-5
CRITICAL
R6929
2.0K
ADAPTER_SENSE
SYS_ONEWIRE
1-Wire OverVoltage Protection
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.
=PP18V5_DCIN_ISOL
BLEEDER
CRITICAL
D6920
SBR0330CW
SOT-323
DCIN_ISOL_BLEEDER_PSRC
C6920
0.1UF
BLEEDER
R6930
1K
BLEEDER
Q6920
AO3407A
SOT23
DCIN_ISOL_BLEEDER_R
BLEEDER
Q6930
2N7002
SOT23-HF1
DCIN_ISOL_BLEEDER_NGATE
BLEEDER
R6921
10K
R6912
68K
Input impedance of 68K meets sparkitecture requirements for both MPM4 and MPM5.
Q6910
SI5419DU
POWERPAK
R6910
100K
When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.
When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg
C6912
0.047UF
R6911
10K
DCIN_ISOL_GATE_R
DCIN_ISOL_GATE
D6910
GDZT2R6.8
GDZ-0201
6.8V Zener
PLACE COMPONENTS NEAR BATTERY CONNECTOR AREA
PPVBAT_G3H_CONN
C6950
0.1UF
C6960
1UF
SYSDET_3_4
OMIT
998-4777
CRITICAL
J6950
INTERPOSER-D1-TOP
COMBO-SM
R6920
47
PP18V5_DCIN_CONN_R
CRITICAL
D6905
SBR0330CW
SOT-323
R6905
10
=PPBUS_G3H
PPBUS_G3H_R
PPVIN_G3H_P3V42G3H
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA
CRITICAL
D6950
RCLAMP2402B
SC-75
SH6950
4.00D2.7ID-1.8H
Pin 63 (SH0962) is Neoconix stiffener, 860-1533
Pin 64 (SH0961) is Neoconix tall locator pin. 860-1530
Pin 65 (SH0960) is Neoconix short clocking pin. 860-1529
3.425V "G3Hot" Supply
Supply needs to guarantee 3.31V delivered to SMC VRef generator
=PP3V42_G3H_REG
OMIT_TABLE
C6992
4.7UF
OMIT_TABLE
C6991
4.7UF
OMIT_TABLE
C6990
4.7UF
P3V42G3H_BOOST
NO_TEST=TRUE
C6994
0.22UF
CRITICAL
L6995
10UH-30%-0.85A-460MOHM
2520
U6990
LT3470AED
DFN
CRITICAL
P3V42G3H_SW
Vout = 3.425V
100MA MAX OUTPUT
(Switcher limit)
C6995
22PF
R6995
348K
CRITICAL
C6999
22UF
P3V42G3H_FB
R6996
200K
Vout = 1.25V * (1 + Ra / Rb)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	3	CAP,CER,4.7UF,10%,25V,X6S,0603	C6990,C6991,C6992	CRITICAL	

SYNC_MASTER=MASTER SYNC_DATE=MASTER

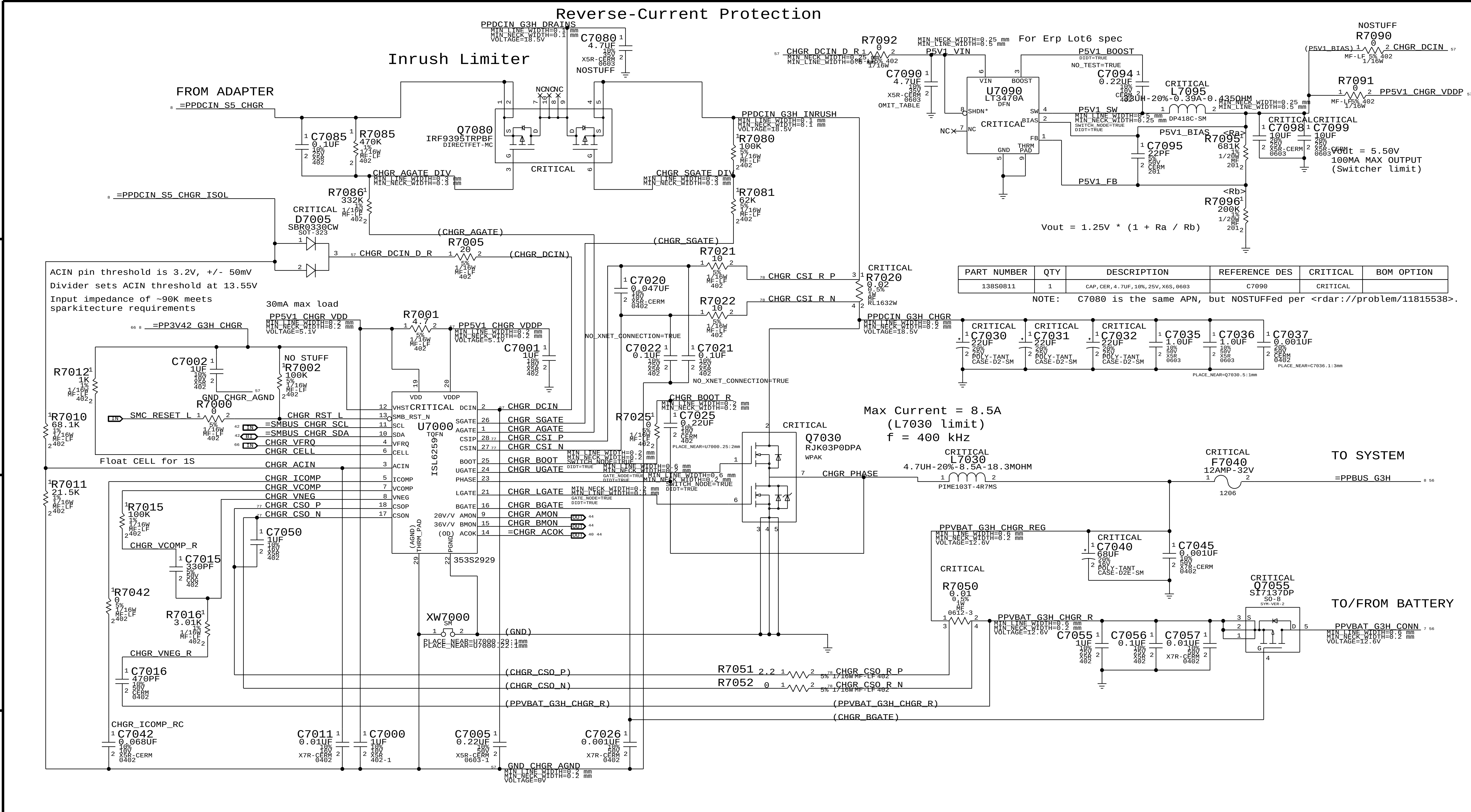
PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X6S,0603	C7090	CRITICAL	

NOTE: C7080 is the same APN, but NOSTUFFed per <rdar://problem/11815538>.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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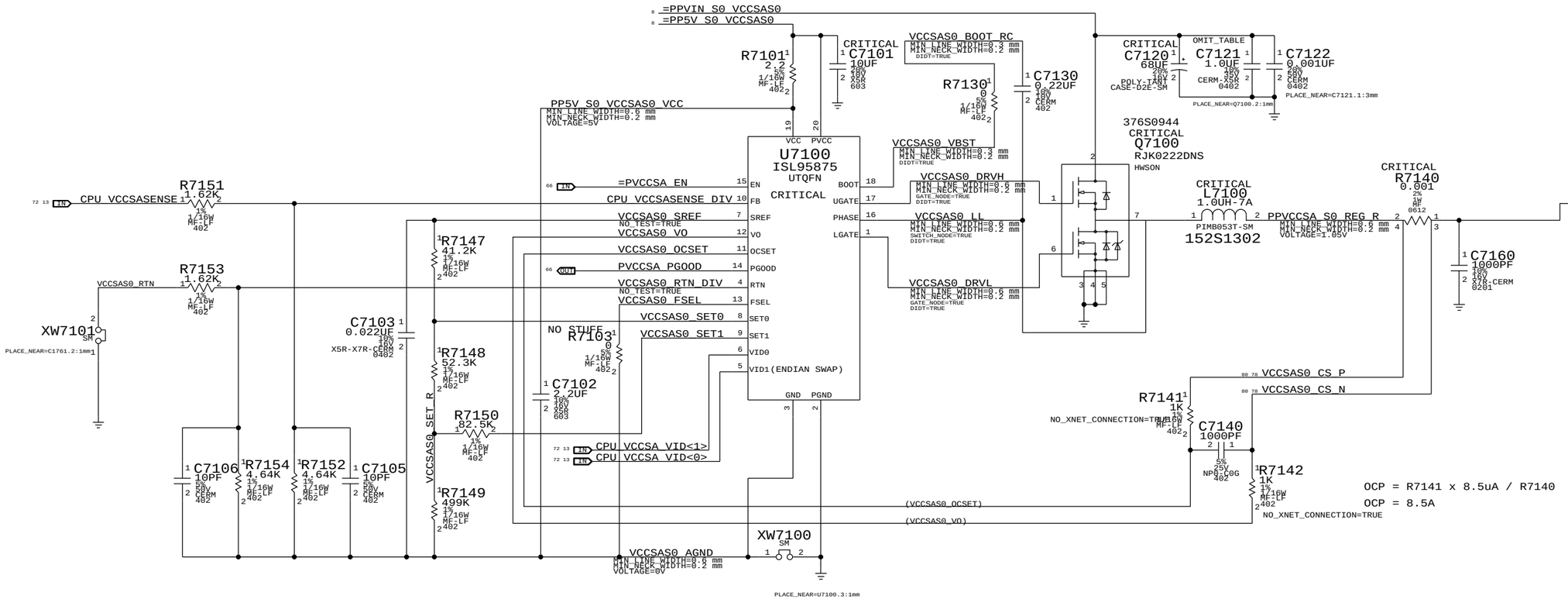
System Agent Power Supply

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7121	CRITICAL	



INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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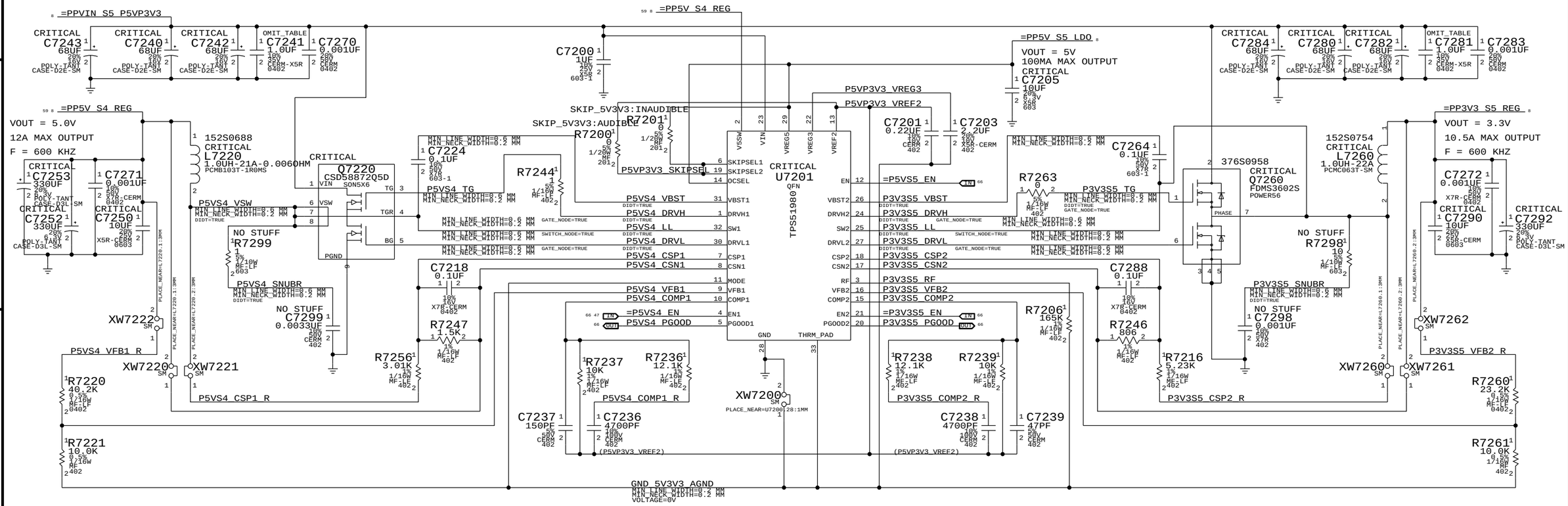
SHEET: 58 OF 80

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7241,C7281	CRITICAL	



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PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 72 OF 132
	SHEET 59 OF 80

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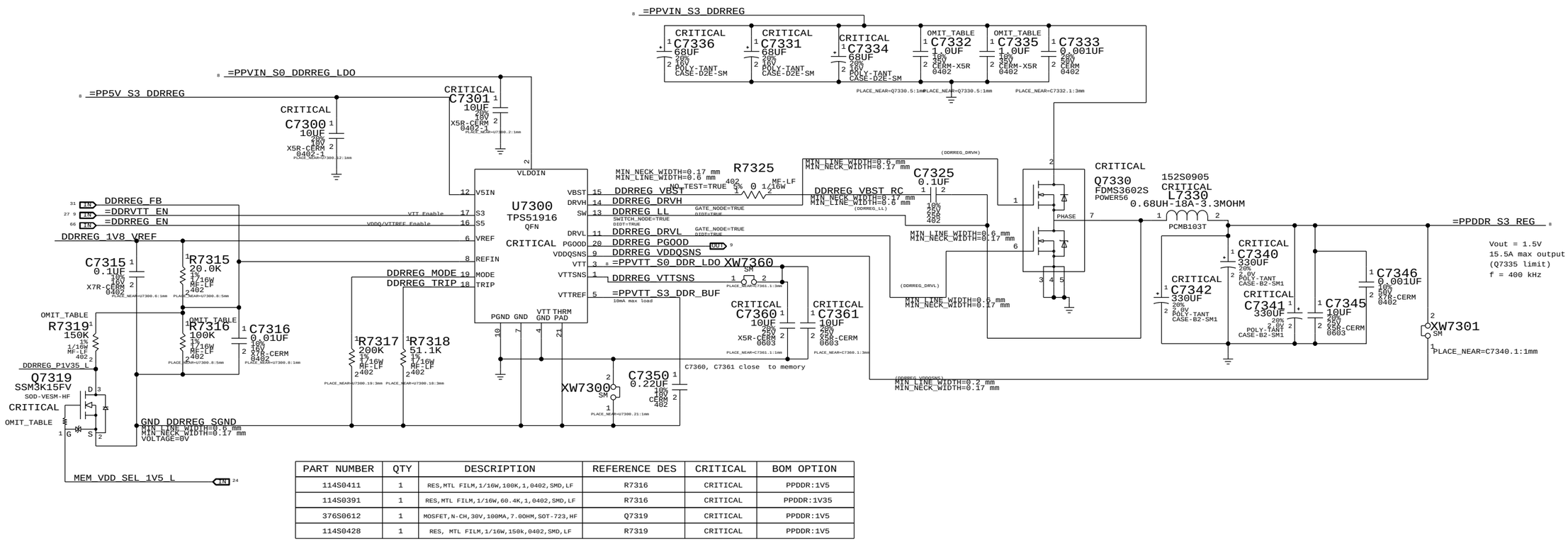
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7332,C7335	CRITICAL	

DDR3 (1V5R1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7316	CRITICAL	PPDDR:1V5
114S0391	1	RES,MTL FILM,1/16W,60.4K,1,0402,SMD,LF	R7316	CRITICAL	PPDDR:1V35
376S0612	1	MOSFET,N-CH,30V,100MA,7.0OHM,SOT-723,HF	Q7319	CRITICAL	PPDDR:1V5
114S0428	1	RES, MTL FILM,1/16W,150k,0402,SMD,LF	R7319	CRITICAL	PPDDR:1V5

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: 1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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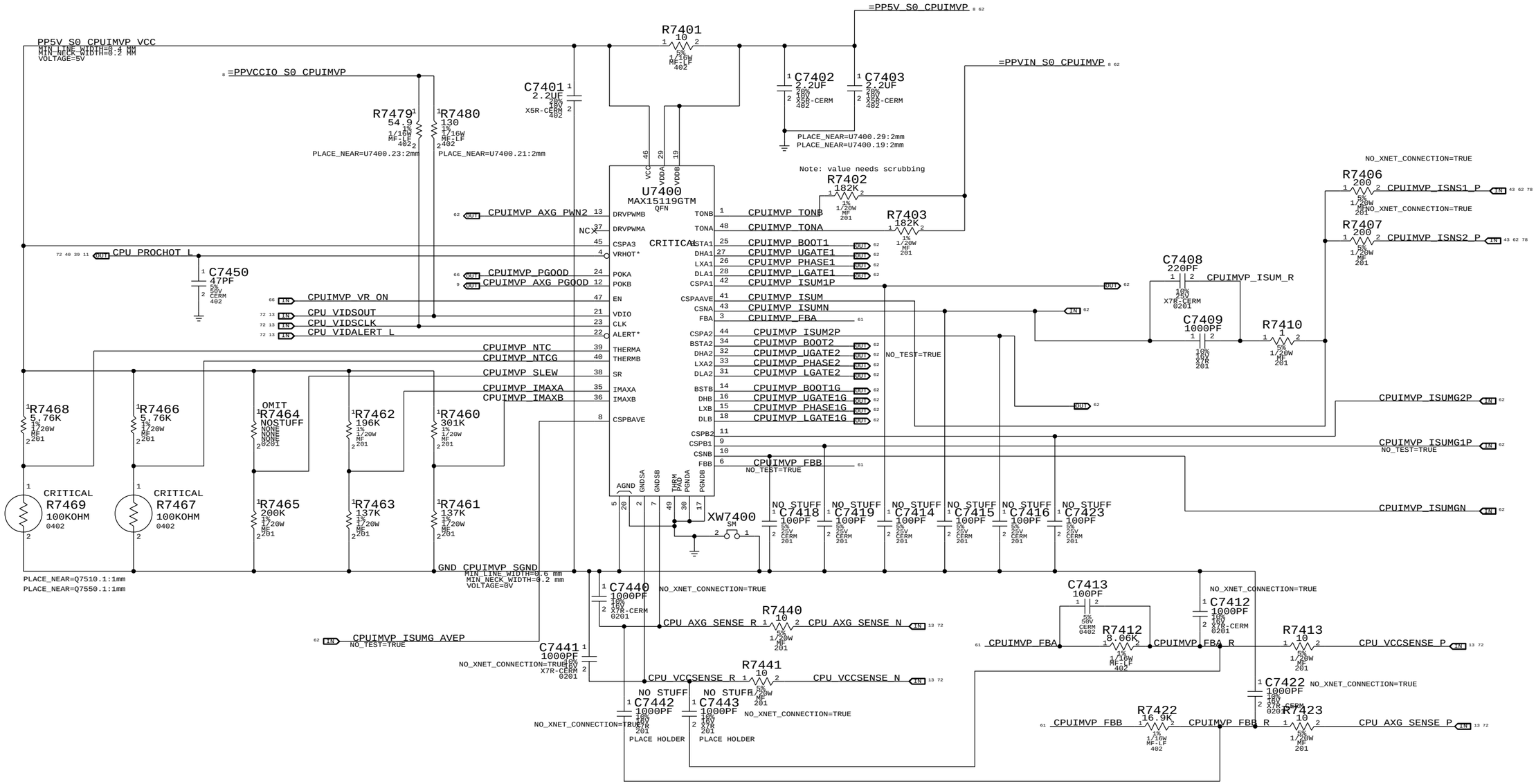

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PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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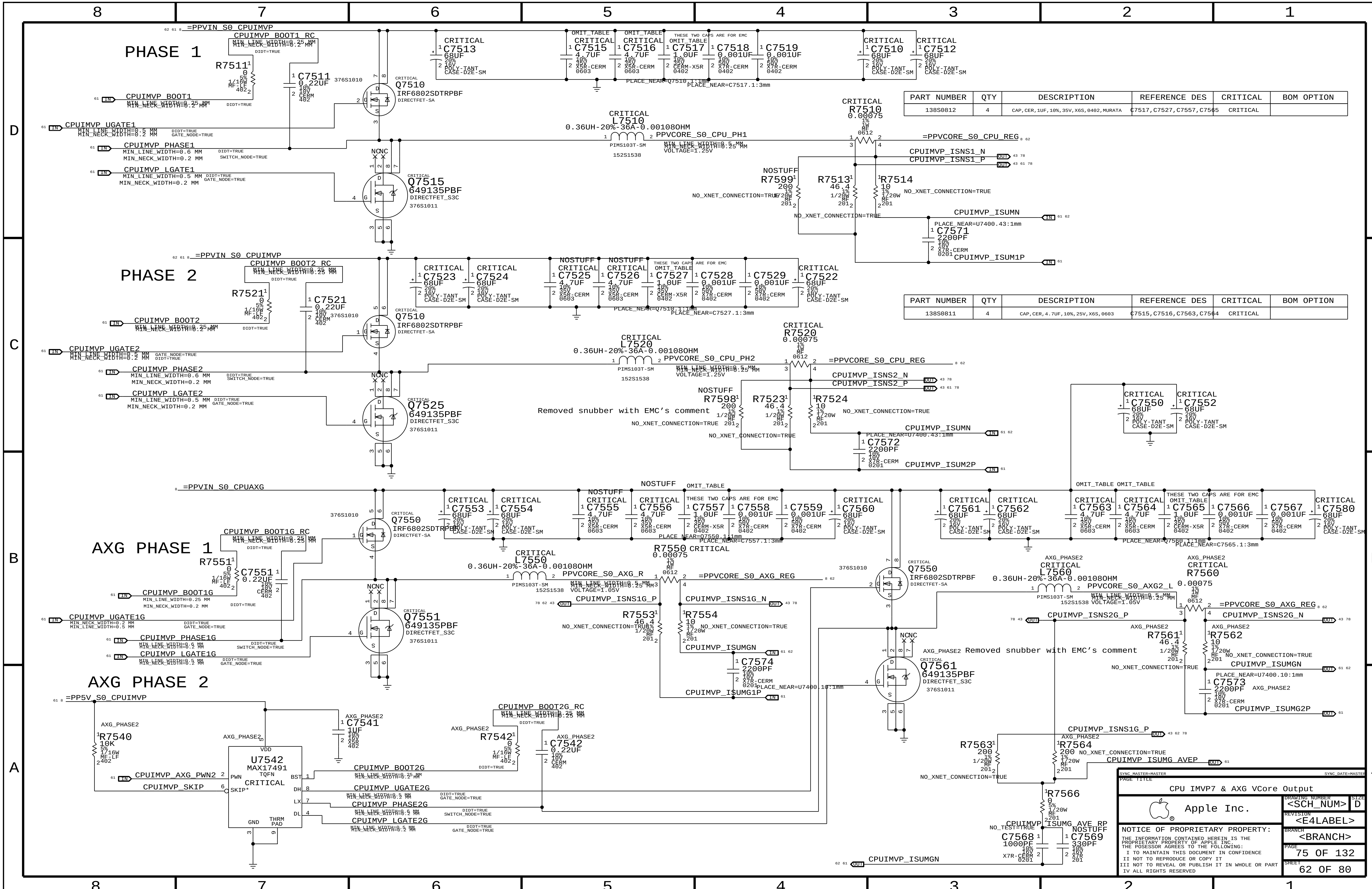


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	4	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7517,C7527,C7557,C7565	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	4	CAP,CER,4.7UF,10%,25V,X6S,0603	C7515,C7516,C7563,C7564	CRITICAL	

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

CPU IMVP7 & AXG VCore Output

Apple Inc.

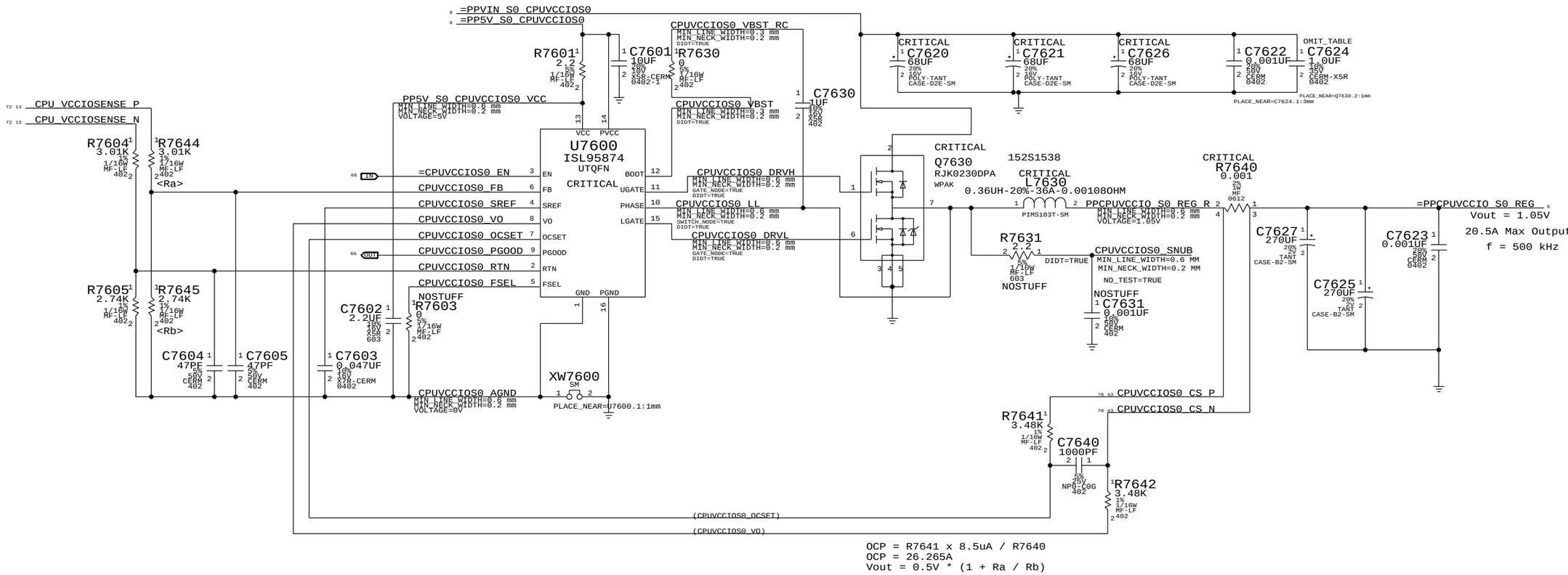
DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

CPU VCCIO (1.05V S0) Regulator

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7624	CRITICAL	



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: CPUVCCIO (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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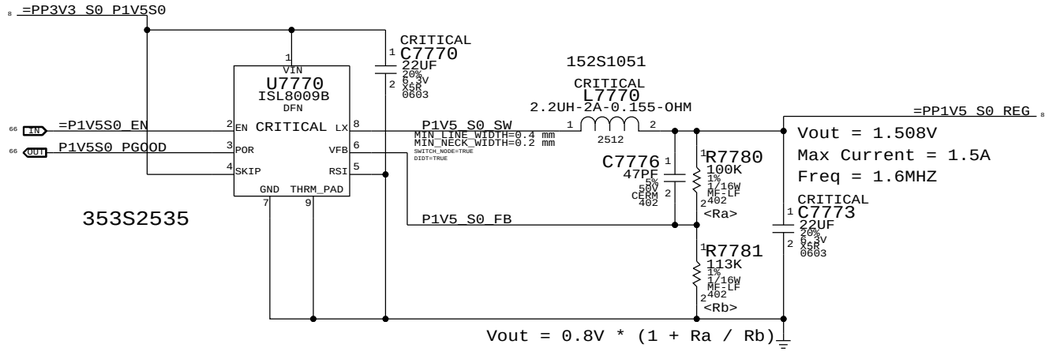
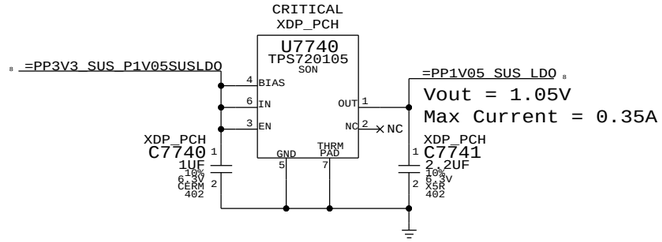
1.5V S0 Switcher



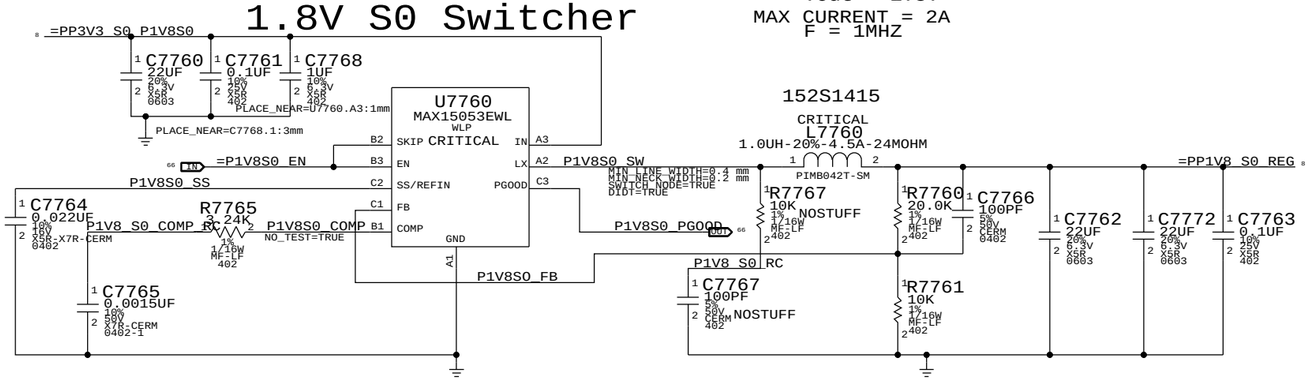
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

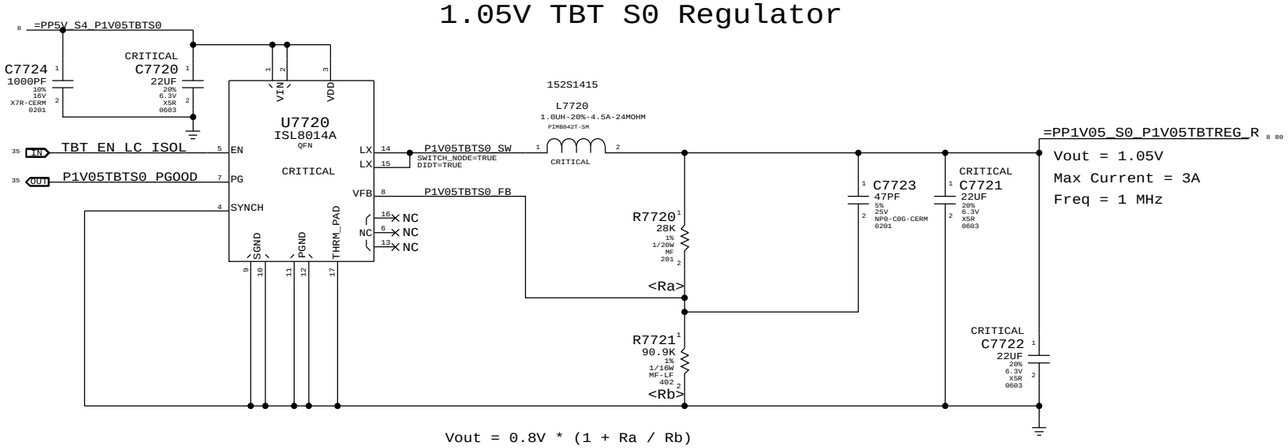


1.8V S0 Switcher

Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



1.05V TBT S0 Regulator



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Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
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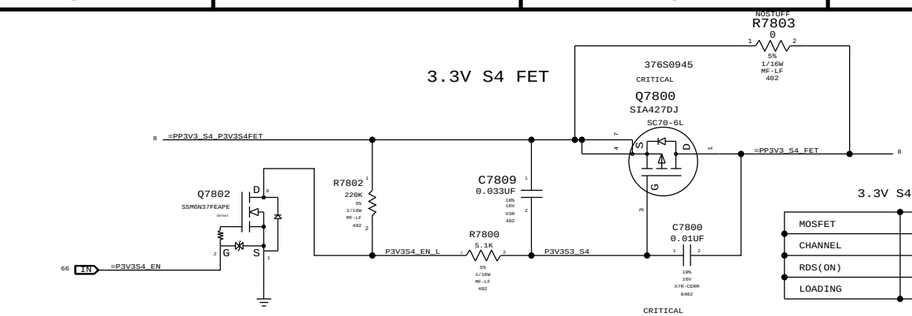
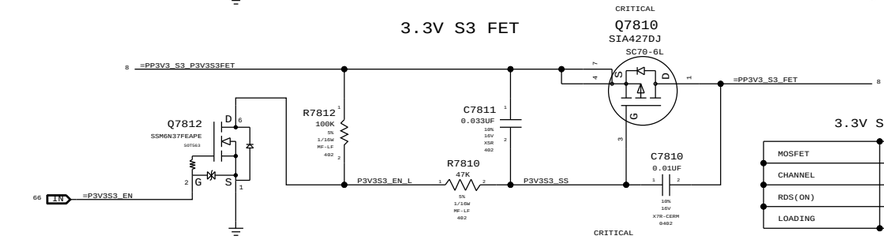
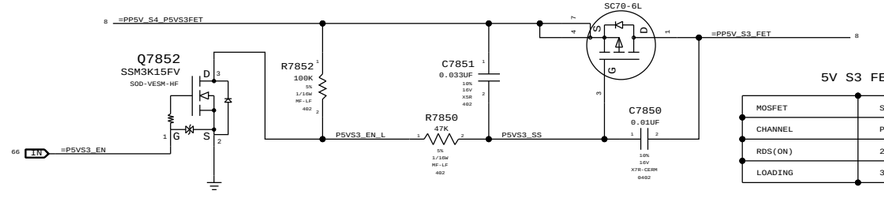
	PAGE: 77 OF 132
	SHEET: 64 OF 80



3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)



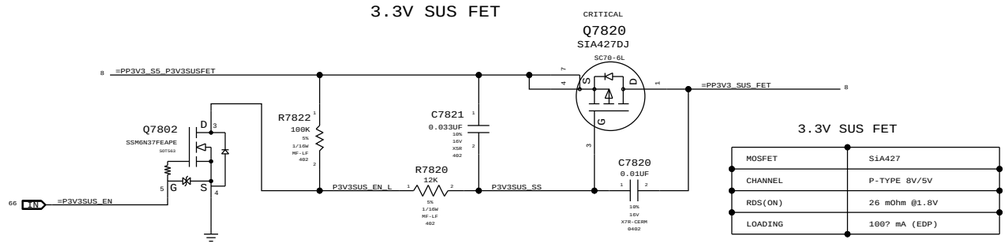
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)



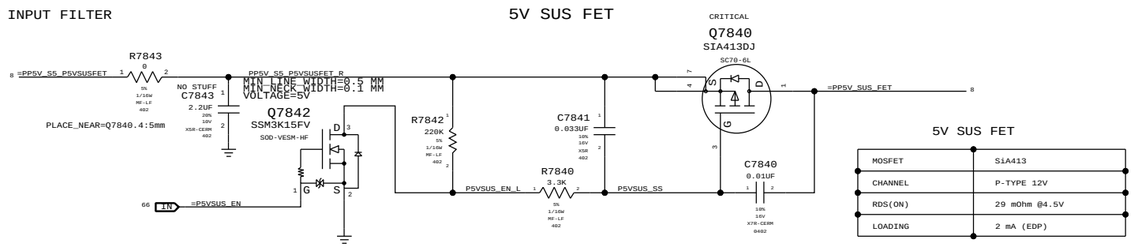
5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

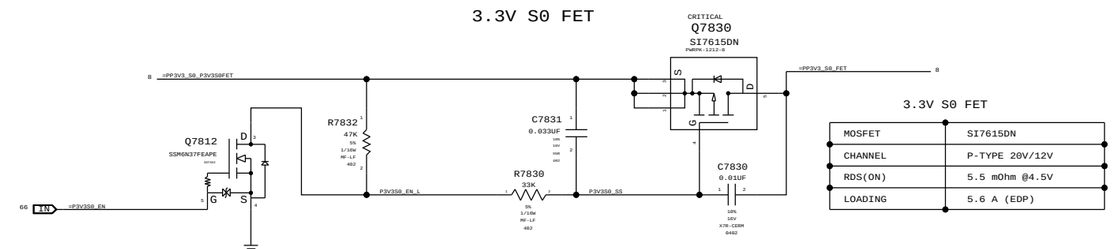
5V_SUS FET INPUT FILTER



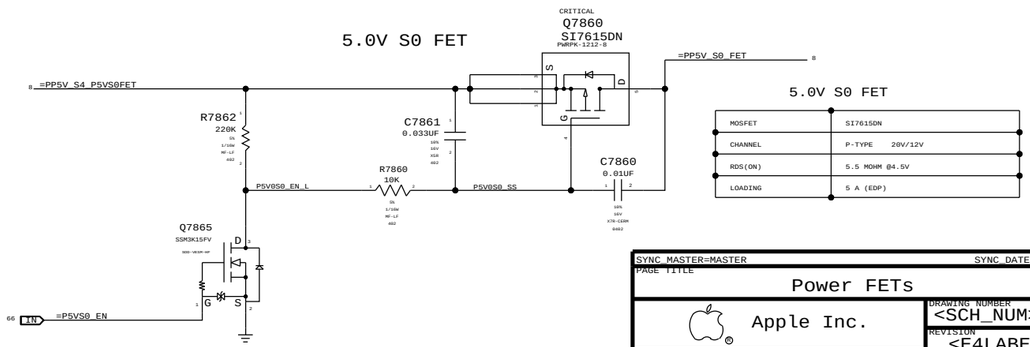
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)



5V SUS FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)



3.3V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	5 A (EDP)

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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S5 Rail Enables & PGOOD

=P5VS5_EN → SMC_PM_G2_EN (MAKE_BASE=TRUE) → R7940 100 5% 1/16W MF-LF 402 → P3V3S5_EN (MAKE_BASE=TRUE) → =P3V3S5_EN
PLACE_NEAR=U7201.21:7mm
C7942 0.0033UF 10% 16V X5R 402 NO STUFF

=PP3V42_G3H_PWRCTL → R7941 100K 5% 1/16W MF-LF 402 → P3V3S5_PGOOD → S5_PWRGD (MAKE_BASE=TRUE)
PLACE_NEAR=U7201.20:7mm
S5_PWRGD (old name RSMRST_PWRGD)-->SMC
SMC-->PM_DSW_PWRGD

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

1.2V, 5V, 3.3V, DDR S3 ENABLE

PM_SLP_S4_L → R7911 5.1K 5% 1/16W MF-LF 402 (PLACE_NEAR=U7300.10:6mm)
PM_SLP_S4_L:100K pull down in PCH page
R7912 0 5% 1/16W MF-LF 402 (PLACE_NEAR=Q7812.2:6mm)
R7913 0 5% 1/16W MF-LF 402 (PLACE_NEAR=Q7842.2:6mm)
R7914 0 5% 1/16W MF-LF 402 (PLACE_NEAR=U4900.K5:6mm)
R7916 3.3K 5% 1/16W MF-LF 402 (PLACE_NEAR=U4900.K5:6mm)
C7910 0.47UF 10% 6.3V X5R 402
NO STUFF C7912 0.47UF 10% 6.3V X5R 402
NO STUFF C7913 0.47UF 10% 6.3V X5R 402
NO STUFF C7914 0.47UF 10% 6.3V X5R 402
NO STUFF C7916 0.47UF 10% 6.3V X5R 402

TPAD_VBUS_EN → 47
P1V2S3_EN
P5VS3_EN → =P5VS3_EN (MAKE_BASE=TRUE) → 65
P3V3S3_EN → =P3V3S3_EN (MAKE_BASE=TRUE) → 65
DDRREG_EN → =DDRREG_EN (MAKE_BASE=TRUE) → 60

3.3V S4 ENABLE

=PP3V3_S5_PWRCTL → C7970 0.1uF 20% 10V X5R 402 (PLACE_NEAR=U7940.1:2.3mm)
PM_SLP_S5_L:100K pull down on PCH page
PM_SLP_S5_L → U7970 74LVC1G32 SOT891 → P5V3V3_S4_EN (MAKE_BASE=TRUE)
SMC_S4_WAKESRC_EN (MAKE_BASE=TRUE)
NOSTUFF R7915 0 5% 1/16W MF-LF 402

=TBTAPWRSW_EN → 69
=TBTBPWRSW_EN → 70
=P3V3S4_EN → 65
=P5VS4_EN → 47 59

CPUVCORE ENABLE

ALL_SYS_PWRGD → R7974 0 5% 1/16W MF-LF 402 (PLACE_NEAR=U7400.7:5mm) → CPUIMVP_VR_ON → 61

3.3V/5.0V Sus ENABLE

=PP3V3_S5_PWRCTL → C7940 0.1uF 20% 10V X5R 402 (PLACE_NEAR=U7940.1:2.3mm)
SMC_BATLOW_L:100K pull up on SMC page
SMC_BATLOW_L → U7940 74AUP1G3208 SOT891
PM_SLP_SUS_L:100K pull down on PCH page
PM_SLP_SUS_L → PM_SUS_EN (MAKE_BASE=TRUE) → =P5VSUS_EN → 65 ; =P3V3SUS_EN → 65
NO STUFF R7917 0 5% 1/16W MF-LF 402

S0 ENABLE

PM_SLP_S3_L → R7978 100 5% 1/16W MF-LF 402
PM_SLP_S3_L:100K pull down in PCH page

(PM_SLP_S3_R_L) → PM_SLP_S3_R_L (MAKE_BASE=TRUE)
R7987 33K 5% 1/16W MF-LF 402 (PLACE_NEAR=U7100.15:6mm)
R7981 20K 5% 1/16W MF-LF 402 (PLACE_NEAR=U7600.3:6mm)
R7985 20K 5% 1/16W MF-LF 402
R7988 10K 5% 1/16W MF-LF 402 (PLACE_NEAR=U7770.3:6mm)
R7986 5.1K 5% 1/16W MF-LF 402 (PLACE_NEAR=U7760.B3:6mm)
C7987 0.47UF 10% 6.3V X5R 402 (PLACE_NEAR=U7100.15:6mm)
C7981 0.47UF 10% 6.3V X5R 402 (PLACE_NEAR=U7600.3:6mm)
C7984 0.47UF 10% 6.3V X5R 402 (PLACE_NEAR=U7770.3:6mm)
C7988 0.47UF 10% 6.3V X5R 402 (PLACE_NEAR=U7770.3:6mm)
C7986 0.47UF 10% 6.3V X5R 402 (PLACE_NEAR=U7760.B3:6mm)

=P5VS0_EN → 65
=P3V3S0_EN → 65
=PBUSVSENS_EN → 44
=TBT_S0_EN → 69 70
P1V8S0_EN → =P1V8S0_EN (MAKE_BASE=TRUE) → 64
P1V5S0_EN → =P1V5S0_EN (MAKE_BASE=TRUE) → 64
P1V05S0_EN (Replaced by TBT_EN_LC_ISOL)
CPUVCCIOS0_EN → =CPUVCCIOS0_EN (MAKE_BASE=TRUE) → 63
PVCCSA_EN → =PVCCSA_EN (MAKE_BASE=TRUE) → 58

CHGR VFRQ Generation

=PP3V42_G3H_CHGR → R7931 100K 5% 1/16W MF-LF 402 → CHGR_VFRQ → 57
Q7931 SSM3K15FV SOD-VESM-HF

VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

S0 Rail PGOOD (BJT Version)

=PP3V3_S0_VMON → R7951 15.0K 1% 1/16W MF-LF 402
=PP3V3_S5_VMON → R7956 150K 1% 1/16W MF-LF 402
R7953 1K 5% 1/16W MF-LF 402 → VMON_3V3_DIV → VMON_Q2_BASE
R7952 7.15K 1% 1/16W MF-LF 402
=PP1V5_S3RS0_VMON → R7954 1K 5% 1/16W MF-LF 402 → VMON_Q3_BASE
R7955 1K 5% 1/16W MF-LF 402 → =PP1V05_S0_VMON → VMON_Q4_BASE
Q7950 ASMCC0179 DFN2015H4-8 (Q1 Q2 Q3 Q4; NC; CRITICAL)
ALL_SYS_PWRGD → S0PGD_C → S0PGD_BJT_GND_R 353S2809
R7957 100 5% 1/16W MF-LF 402

Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

3.3V SUS Detect

=PP3V3_S5_PWRCTL → C7930 0.1uF 20% 10V X5R 402 (PLACE_NEAR=U7930.6:2.3mm)
No stuff C7931, 12ms Min delay time
U7930 Sense input threhold is 3.07V
CRITICAL
=PP3V3_SUS_CNTRL → R7933 100K 5% 1/16W MF-LF 402
=PP3V3_SUS_CNTRL → U7930 TPS3808G33DBVRG4 SOT23-6 (SENSE, VDD, GND, RESET*, MR*) → PM_RSMRST_L (PM_RSMRST_L goes to U1800.C21)
Sus_PGOOD_4CT
C7931 0.001UF 20% 25V X7R 402 NO STUFF

PCH S0 PWRGD

=PP3V3_S5_PCHPWRGD
=PP3V3_S0_SB_PM
R7950 1K 5% 1/16W MF-LF 402
C7950 0.1UF 20% 10V X5R 402
ALL_SYS_PWRGD
CPUIMVP_PGOOD
U7950 74LVC2G08GT SOT833 (PLACE_NEAR=U1800.P12:7mm)
PM_S0_PGOOD
SYS_PWROK_R → R7949 1K 5% 1/16W MF-LF 402 → PM_PCH_SYS_PWROK → 18 24 39
PM_PCH_APWROK → 18
SMC_DELAYED_PWRGD → R7948 0 5% 1/16W MF-LF 402 → PM_PCH_PWROK (MAKE_BASE=TRUE) → 18 25

S0 Rail PGOOD Circuitry (ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

=PP5V_S0_VMON
=PP1V5_S3RS0_VMON
=PP1V05_S0_VMON
=PP3V3_S0_VMON
S0PGOOD_ISL
C7960 0.1UF 20% 10V X5R 402
R7960 10K 1% 1/16W MF-LF 402
R7970 6.04K 1% 1/16W MF-LF 402
R7972 6.04K 1% 1/16W MF-LF 402
R7961 15.0K 1% 1/16W MF-LF 402
R7971 12.4K 1% 1/16W MF-LF 402
R7973 15.0K 1% 1/16W MF-LF 402
P5V_DIV_VMON
P1V5_DIV_VMON
P1V05_VID_VMON
U7960 ISL88042IRTEZ TDFN (VDD, V2MON, V3MON, V4MON, GND, THRM_PAD, RST*, CRITICAL) 353S2310

=PP3V3_S0_PWRCTL → R7967 10K 1% 1/16W MF-LF 402
R7968 100 5% 1/16W MF-LF 402 ← P1V5S0_PGOOD
R7966 100 5% 1/16W MF-LF 402 ← P1V8S0_PGOOD
NO STUFF R7965 100 5% 1/16W MF-LF 402 ← P5VS4_PGOOD
R7969 100 5% 1/16W MF-LF 402 ← CPUVCCIOS0_PGOOD
R7963 100 5% 1/16W MF-LF 402 ← PVCCSA_PGOOD
→ 24 39 66
R7962 330 5% 1/16W MF-LF 402 → ALL_SYS_PWRGD

"WLAN" = ("S3" && "AP_PWR_EN")

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

SMC_ADAPTER_EN → Q7920 SSM6N37FEAPE SOT563 (NO STUFF R7929 0 5% 1/16W MF-LF 402)
AC_EN_L
PM_SLP_S3_L → Q7920 SSM6N37FEAPE SOT563
Q7925 SSM6N15AFE SOT563
PM_WLAN_EN_L
=PP3V3_S3_WLAN → R7926 10K 5% 1/16W MF-LF 402 → PM_WLAN_EN → 36
R7925 10K 5% 1/16W MF-LF 402
Q7925 SSM6N15AFE SOT563
AP_PWR_EN → 19 24 36

SYNC_MASTER=MASTER | SYNC_DATE=MASTER
PAGE TITLE: Power Control 1/ENABLE

Apple Inc.

DRAWING NUMBER	<SCH_NUM>
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BRANCH	<BRANCH>
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LCD PANEL INTERFACE (eDP)

CRITICAL
J9000
20525-130E-01
F-RT-SM

LCD_HPD
DP_INT_AUX_C_P
DP_INT_AUX_C_N
DP_INT_ML_C_P<0>
DP_INT_ML_C_N<0>
DP_INT_ML_C_P<1>
DP_INT_ML_C_N<1>
DP_INT_ML_C_P<2>
DP_INT_ML_C_N<2>
DP_INT_ML_C_P<3>
DP_INT_ML_C_N<3>

R9000 0 5% 1/20W MF 201
C9028 0.1UF 10% 16V X5R-CERM 0201
C9029 0.1UF 10% 16V X5R-CERM 0201
C9020 0.1UF 10% 16V X5R-CERM 0201
C9021 0.1UF 10% 16V X5R-CERM 0201
C9022 0.1UF 10% 16V X5R-CERM 0201
C9023 0.1UF 10% 16V X5R-CERM 0201
C9024 0.1UF 10% 16V X5R-CERM 0201
C9025 0.1UF 10% 16V X5R-CERM 0201
C9026 0.1UF 10% 16V X5R-CERM 0201
C9027 0.1UF 10% 16V X5R-CERM 0201

PPVOUT_S0_LCDBKLT
NC
LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1
LCD_HPD_CONN
LCD_FSS
DP_INT_AUX_P
DP_INT_AUX_N
BEAD_PROBE=TRUE DP_INT_ML_P<0>
BEAD_PROBE=TRUE DP_INT_ML_N<0>
BEAD_PROBE=TRUE DP_INT_ML_P<1>
BEAD_PROBE=TRUE DP_INT_ML_N<1>
BEAD_PROBE=TRUE DP_INT_ML_P<2>
BEAD_PROBE=TRUE DP_INT_ML_N<2>
BEAD_PROBE=TRUE DP_INT_ML_P<3>
BEAD_PROBE=TRUE DP_INT_ML_N<3>

518S0829

LCD Panel Current XW Short

EDP: 1 A, Refdes: XW9020

XW9020 SM
PP5VR3V3_SW_LCD_ISNS
PP5VR3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

CRITICAL
L9000
FERR-220-OHM
0805

PP5VR3V3_SW_LCD

C9001 0.1UF 10% 16V X5R-CERM 0201
C9002 0.1UF 10% 16V X5R-CERM 0201
C9003 1000PF 10% 100V X7R-CERM 0603
C9000 1000PF 10% 100V X7R-CERM 0603

NC_ISNS_LCD_PANELN
NC_ISNS_LCD_PANELP

NO_XNET_CONNECTION=TRUE
BP9000 BEAD-PROBE SM
BP9001 BEAD-PROBE SM
BP9002 BEAD-PROBE SM
BP9003 BEAD-PROBE SM
BP9004 BEAD-PROBE SM
BP9005 BEAD-PROBE SM
BP9006 BEAD-PROBE SM
BP9007 BEAD-PROBE SM

R9011 1M 5% 1/20W MF 201
R9012 1M 5% 1/20W MF 201
R9013 1M 5% 1/20W MF 201
R9014 1M 5% 1/20W MF 201
R9015 1M 5% 1/20W MF 201
R9016 1M 5% 1/20W MF 201
R9017 1M 5% 1/20W MF 201
R9018 1M 5% 1/20W MF 201

LCD_PWR_EN
R9010 1K 5% 1/10W MF 402

CRITICAL
U9000
FPF1009
MFET-2X2-8IN
ON
VIN_1 VIN_2 VOUT_1 VOUT_2 GND THRM PAD

=PP5V_S0_LCD

C9009 0.1UF 10% 16V X7R-CERM 0402
C9011 0.1UF 10% 16V X7R-CERM 0402
C9012 10UF 20% 6.3V X5R 603

LCD Panel HPD & AUX strapping

=PP3V3_S0_LCD
R9003 1M 5% 1/20W MF 201
DP_INT_AUX_N
LCD_HPD_CONN
DP_INT_AUX_P
R9001 1M 5% 1/20W MF 201
R9002 1M 5% 1/20W MF 201

SYNC_MASTER=D1_SENSORS	SYNC_DATE=07/11/2012
PAGE TITLE: eDP Display Connector	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 90 OF 132
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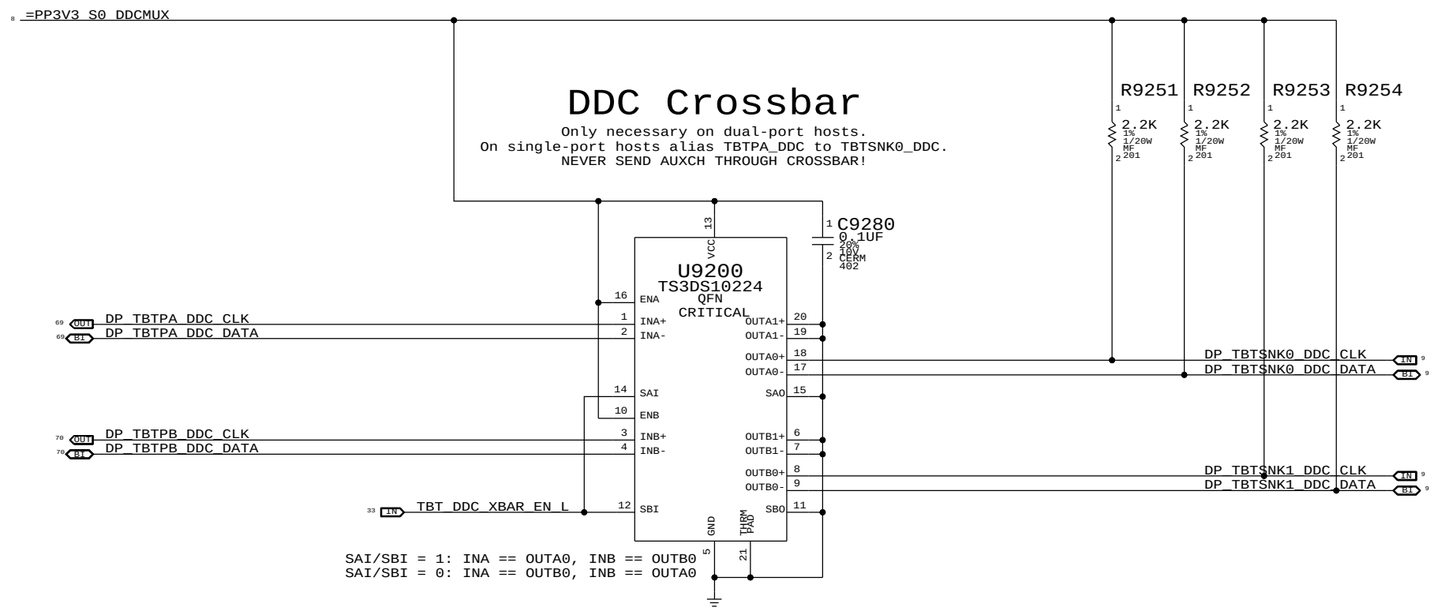

SYNC_MASTER=MASTER	SYNC_DATE=MASTER
PAGE TITLE	DDC Crossbar
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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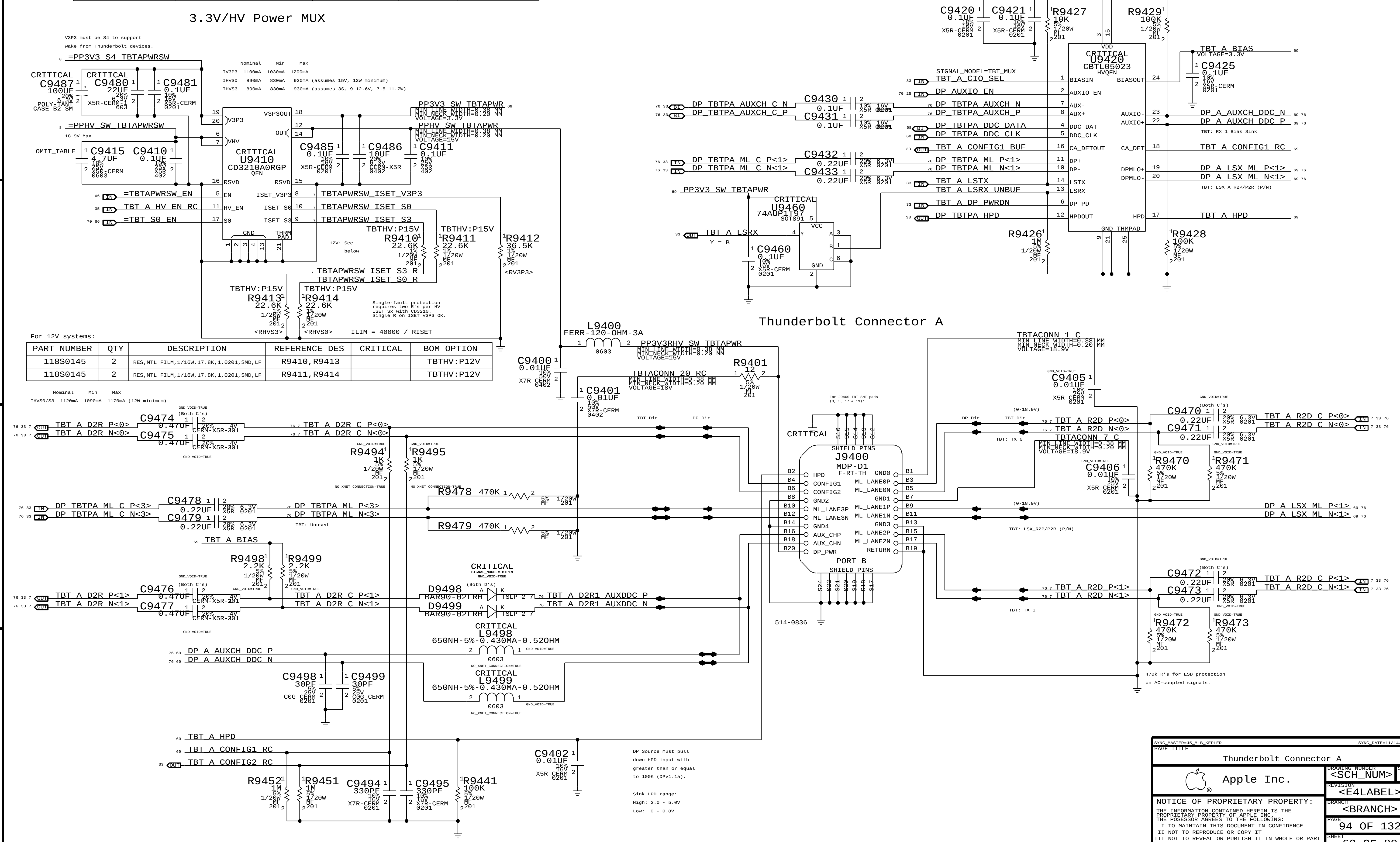
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X5R,0603,MURATA	C9415	CRITICAL	

3.3V/HV Power MUX



For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2011

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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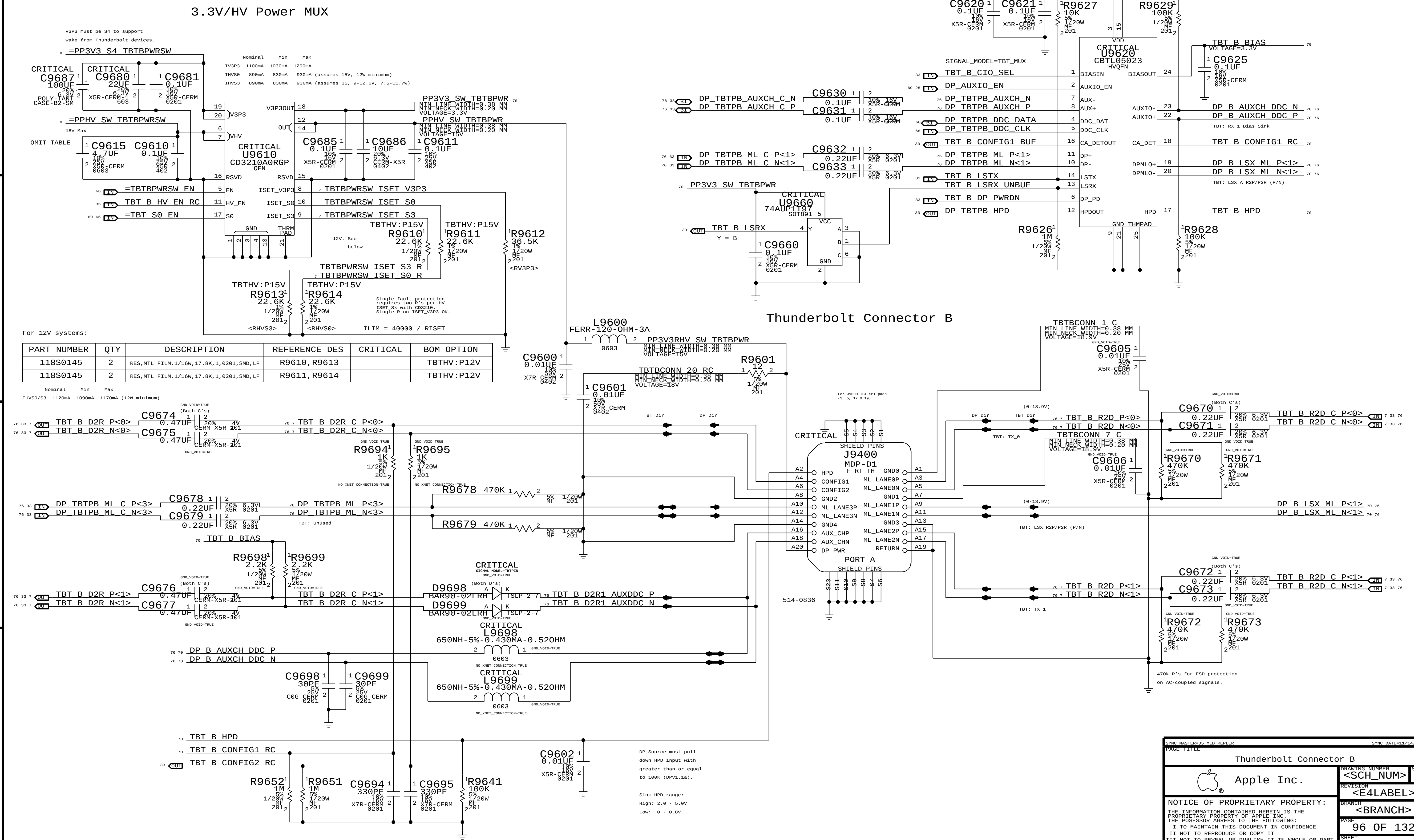
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X5R,0603,MURATA	C9615	CRITICAL	

3.3V/HV Power MUX



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9610,R9613		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9611,R9614		TBTHV:P12V

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2011

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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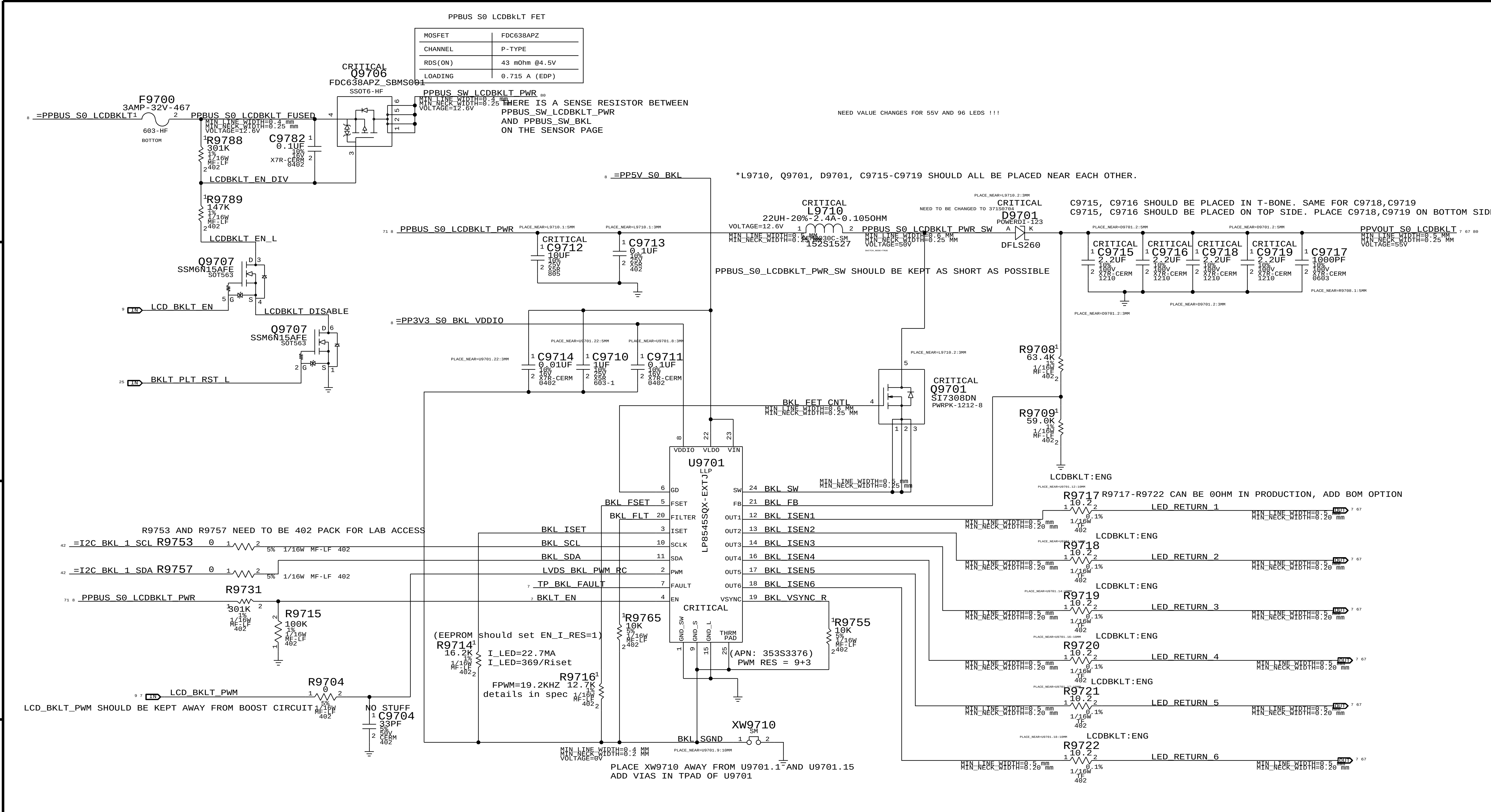

PPBUS S0 LCDBKLT FET
MOSFET FDC638APZ
CHANNEL P-TYPE
RDS(ON) 43 mOhm @4.5V
LOADING 0.715 A (EDP)
CRITICAL Q9706 FDC638APZ_SBMS001 SSOT6-HF
F9700 3AMP-32V-467 603-HF BOTTOM
=PPBUS_S0_LCDBKLT
PPBUS_S0_LCDBKLT_FUSED
PPBUS_SW_LCDBKLT_PWR
THERE IS A SENSE RESISTOR BETWEEN
PPBUS_SW_LCDBKLT_PWR
AND PPBUS_SW_BKL
ON THE SENSOR PAGE
NEED VALUE CHANGES FOR 55V AND 96 LEDS !!!
R9788 301K
C9782 0.1UF
LCDBKLT_EN_DIV
R9789 147K
LCDBKLT_EN_L
Q9707 SSM6N15AFE SOT563
LCD_BKLT_EN
LCDBKLT_DISABLE
BKLT_PLT_RST_L
=PP5V_S0_BKL
*L9710, Q9701, D9701, C9715-C9719 SHOULD ALL BE PLACED NEAR EACH OTHER.
CRITICAL L9710 22UH-20%-2.4A-0.105OHM 152S1527
CRITICAL D9701 POWERDI-123 DFLS260
C9715, C9716 SHOULD BE PLACED IN T-BONE. SAME FOR C9718,C9719
C9715, C9716 SHOULD BE PLACED ON TOP SIDE. PLACE C9718,C9719 ON BOTTOM SIDE
PPBUS_S0_LCDBKLT_PWR
CRITICAL C9712 10UF
C9713 0.1UF
PPBUS_S0_LCDBKLT_PWR_SW
PPVOUT_S0_LCDBKLT
CRITICAL C9715 2.2UF
CRITICAL C9716 2.2UF
CRITICAL C9718 2.2UF
CRITICAL C9719 2.2UF
C9717 1000PF
PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE
=PP3V3_S0_BKL_VDDIO
C9714 0.01UF
C9710 1UF
C9711 0.1UF
CRITICAL Q9701 SI7308DN PWRPK-1212-8
BKL_FET_CNTL
R9708 63.4K
R9709 59.0K
LCDBKLT:ENG
U9701 LP8545SQX-EXTJ LLP CRITICAL
BKL_SW
BKL_FB
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
BKL_VSYNC_R
BKL_FSET
BKL_FLT
BKL_ISET
BKL_SCL
BKL_SDA
LVDS_BKL_PWM_RC
TP_BKL_FAULT
BKL_EN
R9717-R9722 CAN BE 0OHM IN PRODUCTION, ADD BOM OPTION
R9717 10.2
R9718 10.2
R9719 10.2
R9720 10.2
R9721 10.2
R9722 10.2
LED_RETURN_1
LED_RETURN_2
LED_RETURN_3
LED_RETURN_4
LED_RETURN_5
LED_RETURN_6
R9753 AND R9757 NEED TO BE 402 PACK FOR LAB ACCESS
=I2C_BKL_1_SCL R9753 0
=I2C_BKL_1_SDA R9757 0
PPBUS_S0_LCDBKLT_PWR
R9731 301K
R9715 100K
(EEPROM should set EN_I_RES=1)
R9714 16.2K
I_LED=22.7MA
I_LED=369/Riset
R9716 12.7K
FPWM=19.2KHZ
details in spec
R9765 10K
R9755 10K
(APN: 353S3376)
PWM RES = 9+3
LCD_BKLT_PWM
R9704 0
LCD_BKLT_PWM SHOULD BE KEPT AWAY FROM BOOST CIRCUIT
NO STUFF C9704 33PF
XW9710 SM
BKL_SGND
PLACE XW9710 AWAY FROM U9701.1 AND U9701.15
ADD VIAS IN TPAD OF U9701

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	6	RES,MTL FILM,1/16W,0,5,0402,SMD,LF	R9717,R9718,R9719,R9720,R9721,R9722	CRITICAL	LCDBKLT:PROD

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=09/21/2011

PAGE TITLE

LCD Backlight Driver (LP8545)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.1MM	0.1MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	=4X_DIELECTRIC	?
CPU_ITP	*	=4x_DIELECTRIC	?
CPU_VCCSENSE	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=6X_DIELECTRIC	?
CLK_PCIE	*	=5X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	7 10 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	7 10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	7 10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	7 10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	7 10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	7 10 18
FDI_FSYNC	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	10 18
FDI_LSYNC	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	10 18
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	10 18
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	7 11 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	7 11 17
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_COMP	10
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 24
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 17
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 17
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	17 24
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	17 24
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLK_P	11 17
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLK_N	11 17
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 24
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 24
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 24
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 24
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 24
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	11 24
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	11 24
XDP_BDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	11 24 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	11 24
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	11 24
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	11 39
CPU_PROC_SEL_L	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	11 20
CPU_PECI	CPU_50S	CPU_VID	CPU_PECI	11 20 40
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 39 40 61
XDP_CPU_PWRGD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	24
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	11 20 40
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	11 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	11 18 27
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	11 20 24
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	11
	CPU_50S	CPU_VID	CPU_VIDSOUT	13 61
	CPU_50S	CPU_VID	CPU_VIDSCLK	13 61
	CPU_50S	CPU_VID	CPU_VIDALERT_L	13 61
	CPU_55S	CPU_VID	CPU_VCCSA_VID<1..0>	13 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	13 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	13 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	10
CPU_VCCSASENSE	CPU_50S	CPU_AGTL	CPU_VCCSASENSE	13 58
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_A	10 31
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_B	10 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_A	28 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	29 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_A	28 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	29 31
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	24
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	24

SYNC_MASTER=JS_MLB SYNC_DATE=09/13/2012

PAGE TITLE

CPU Constraints

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4X_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3X_DIELECTRIC	?
MEM_CTRL2MEM	*	=3X_DIELECTRIC	?
MEM_CMD2CMD	*	=2X_DIELECTRIC	?
MEM_CMD2MEM	*	=3X_DIELECTRIC	?
MEM_DATA2DATA	*	=2X_DIELECTRIC	?
MEM_DATA2MEM	*	=3X_DIELECTRIC	?
MEM_DQS2MEM	*	=4X_DIELECTRIC	?
MEM_2OTHER	*	=6X_DIELECTRIC	?
MEM_DQBL2BL	*	=4X_DIELECTRIC	?
MEM_DQCH2CH	*	=6X_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_*	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQ_BYTE*	MEM_*	*	MEM_DATA2MEM
MEM_*_DQ_BYTE*	=SAME	*	MEM_DATA2DATA
MEM_A_DQ_BYTE*	MEM_A_DQ_BYTE*	*	MEM_DQBL2BL
MEM_B_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQBL2BL
MEM_A_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQCH2CH

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_*	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	*	*	MEM_2OTHER

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Chief River SFF Platform DG, Rev 0.7 (#460452), Section 2.6.3

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<0>	12 28 30
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<1..0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<1>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<1>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	12 28 30
MEM_A_DQ_BYTE0	MEM_50S	MEM_A_DQ_BYTE0	MEM_A_DQ<7..0>	7 12 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_A_DQ_BYTE1	MEM_A_DQ<15..8>	7 12 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_A_DQ_BYTE2	MEM_A_DQ<23..16>	7 12 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_A_DQ_BYTE3	MEM_A_DQ<31..24>	7 12 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_A_DQ_BYTE4	MEM_A_DQ<39..32>	7 12 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_A_DQ_BYTE5	MEM_A_DQ<47..40>	7 12 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_A_DQ_BYTE6	MEM_A_DQ<55..48>	7 12 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_A_DQ_BYTE7	MEM_A_DQ<63..56>	7 12 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	12 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	12 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	12 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	12 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	12 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	12 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	12 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	12 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	12 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	12 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	12 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	12 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	12 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	12 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	12 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	12 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<0>	12 29 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<1>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<1..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	12 29 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_B_DQ_BYTE0	MEM_B_DQ<7..0>	7 12 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_B_DQ_BYTE1	MEM_B_DQ<15..8>	7 12 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_B_DQ_BYTE2	MEM_B_DQ<23..16>	7 12 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_B_DQ_BYTE3	MEM_B_DQ<31..24>	7 12 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_B_DQ_BYTE4	MEM_B_DQ<39..32>	7 12 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_B_DQ_BYTE5	MEM_B_DQ<47..40>	7 12 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_B_DQ_BYTE6	MEM_B_DQ<55..48>	7 12 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_B_DQ_BYTE7	MEM_B_DQ<63..56>	7 12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	12 29

SYNC_MASTER=J5_MLB SYNC_DATE=09/13/2013

PAGE TITLE: Memory Constraints

Apple Inc.

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Digital Video Signal Constraints

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	*	=5:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
I25 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRIN_P	7
I25 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRIN_N	7
I25 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDROUT_P	7
I25 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDROUT_N	7
I25 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRIN_P	7
I25 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRIN_N	7
I25 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDROUT_N	7
I25 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDROUT_P	7
I26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RC_P	7 37
I26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RC_N	7 37
I26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_N	7 37
I26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_P	7 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	7 17 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_N	7 17 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	7 17 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_N	7 17 37
I232 SATA_HDD_D2R	SATA_90D	SATA	SATA_SSDRHDD_D2R_P	7 37
I233 SATA_HDD_D2R	SATA_90D	SATA	SATA_SSDRHDD_D2R_N	7 37
I234 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSDRHDD_R2D_P	7 37
I235 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSDRHDD_R2D_N	7 37
I33 PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP	17
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP	17
I236 USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_P	19 26
I237 USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_N	19 26
USB_EXTB	USB_85D	USB	USB_EXTB_EHCI_P	19 26
USB_EXTB	USB_85D	USB	USB_EXTB_EHCI_N	19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_P	19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_N	19 26
USB_EXTA	USB_85D	USB	USB_EXTA_P	19 38
USB_EXTA	USB_85D	USB	USB_EXTA_N	19 38
USB_EXTB	USB_85D	USB	USB_EXTB_P	7 26 36
USB_EXTB	USB_85D	USB	USB_EXTB_N	7 26 36
USB_EXTC	USB_85D	USB	USB_EXTD_P	
USB_EXTC	USB_85D	USB	USB_EXTD_N	
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	7 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_N	7 32
USB_BT	USB_85D	USB	USB_BT_P	7 9 36
USB_BT	USB_85D	USB	USB_BT_N	7 9 36
USB_TPAD	USB_85D	USB	USB_TPAD_P	9 47
USB_TPAD	USB_85D	USB	USB_TPAD_N	9 47
USB_SMC	USB_85D	USB	USB_SMC_P	9 39
USB_SMC	USB_85D	USB	USB_SMC_N	9 39
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	19
I238 USB_EXTD	USB_85D	USB	USB_EXTD_XHCI_P	19 26
I239 USB_EXTD	USB_85D	USB	USB_EXTD_XHCI_N	19 26
I245 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	38
I244 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_N	38
I247 USB_CAMERA	USB_85D	USB	USB_CAMERA_P	19 32
I246 USB_CAMERA	USB_85D	USB	USB_CAMERA_N	19 32
I245 USB_EXTA	USB_85D	USB	USB_LT1_P	7 38
I243 USB_EXTA	USB_85D	USB	USB_LT1_N	7 38
I220 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_P	19 36
I221 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_N	19 36
I222 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_P	7 19 36
I223 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_N	7 19 36
I230 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_P	19 38
I229 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_N	7 19 38
I228 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_P	7 19 38
I231 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_N	7 19 38

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
I256 SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	17 25
I255 SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	17 25
I254	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	17
I253 SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	
I252	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
I251 SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT	25 33
I250	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT_R	33

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=09/21/2017

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	7 17 39 41
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	7 17 39 41
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	25
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	7 25 39
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	7 25 41
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	7 17 42
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	7 17 42
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 42
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 42
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SML_PCH_1_CLK	17 42
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SML_PCH_1_DATA	17 42
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 51
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 51
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 51
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 51
	HDA_50S	HDA	AUD_SDI_R	51
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 51
	HDA_50S	HDA	HDA_SDOUT_R	17 25
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 41
	SPI_55S	SPI	SPI_CLK	41
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 41
	SPI_55S	SPI	SPI_MOSI	41
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 41
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 41
	SPI_55S	SPI	SPI_CS0_L	41
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	7 17 36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	7 17 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	7 17 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_N	7 17 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_P	7 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_N	7 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	7 17 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_N	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P	7 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N	7 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P	7 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N	7 36
PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	7 17
PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	7 17
PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_P	7 17 33
PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_N	7 17 33
PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	17
PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	17
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	7 17
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	17
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	17
	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	7 17 25
PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_P	7 9 17
PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_N	7 9 17
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	7 9 17
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	7 9 17
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	7 17 36
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	7 17 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	7 17 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	7 17 36
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	7 9 17
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	7 9 17
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	7 17
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	7 17
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_P<3..0>	7 9 33
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_N<3..0>	7 9 33
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_P<3..0>	7 33
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_N<3..0>	7 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_P<3..0>	7 9 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_N<3..0>	7 9 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_P<3..0>	7 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_N<3..0>	7 33

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2013

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

NOTE: Thunderbolt high-speed nets are NOT directly assigned to TBTDP_*D physical rules.
TABLE_PHYSICAL_ASSIGNMENT symbols must be used to create the assignments.
Proper differential impedance depends on mDP connector used.
For 514-0637: R2D nets (SMT pins) = 80D, D2R nets (TH pins) = 100D

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
HDMI	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMI	TOP,BOTTOM	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_P<1..0>	7 33 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_N<1..0>	7 33 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_P<1..0>	7 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_N<1..0>	7 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3..1:2>	33 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3..1:2>	33 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3..1:2>	69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3..1:2>	69
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	69
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<1>	7 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<1>	7 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<0>	7 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<0>	7 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_P<1>	7 33 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_N<1>	7 33 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_P<0>	7 33 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_N<0>	7 33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	69
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	69
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_P	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_N	69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_P<1..0>	7 33 70
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_N<1..0>	7 33 70
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_P<1..0>	7 70
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_N<1..0>	7 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3..1:2>	33 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3..1:2>	33 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3..1:2>	70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3..1:2>	70
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	70
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<0>	7 70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<0>	7 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<1>	7 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<1>	7 70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_P<0>	7 33 70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_N<0>	7 33 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_P<1>	7 33 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_N<1>	7 33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	70
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	70
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_P	70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_N	70

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	33
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	33
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	33
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	33

Only used on hosts supporting Thunderbolt video-in

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SMBUS_SMC_2_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	7 39 42
SMBUS_SMC_2_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	7 39 42
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	7 39 42
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	7 39 42
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	39 42
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	39 42
SMBUS_SMC_5_SCL	SMB_50S	SMB	SMBUS_SMC_5_SCL	
SMBUS_SMC_5_SDA	SMB_50S	SMB	SMBUS_SMC_5_SDA	
SMBUS_SMC_3_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	39 42
SMBUS_SMC_3_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	39 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_N	57

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_CLK	*	GND_P2MM
GND	MEM_CMD	*	GND_P2MM
GND	MEM_CTRL	*	GND_P2MM
GND	MEM_*_DQ_BYTE*	*	GND_P2MM
GND	MEM_DQS	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB3	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB3	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DDR3 Loaded Segment Constraint Relaxations

Alternate single ended and differential impedances between devices.

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_37S	BGA_MEM	MEM_50S
MEM_40S	BGA_MEM	MEM_50S
MEM_72D	BGA_MEM	MEM_85D

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
1TO1_DIFFPAIR	*	1:1_DIFFPAIR
SENSE_1TO1_55S	*	SENSE_1TO1_55S
THERM_1TO1_55S	*	THERM_1TO1_55S
DIFFPAIR	*	DIFFPAIR

Graphics, SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

D1 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 10
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 10
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	43 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	43 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VDDQ_SENSE_P	13
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VDDQ_SENSE_N	13
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCD_PANEL_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCD_PANEL_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_SSD_P	37 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_SSD_N	37 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_3V3_S0_SSD_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_3V3_S0_SSD_R_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_WLAN_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_WLAN_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_P	80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_N	80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_R_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	58 80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	58 80
HDMI_CLK	HDMI_90D	HDMI	HDMI_IG_CLK_C_P	7 9 36
HDMI_CLK	HDMI_90D	HDMI	HDMI_IG_CLK_C_N	7 9 36
HDMI_DATA	HDMI_90D	HDMI	HDMI_IG_DATA_C_P<2..0>	7 9 36
HDMI_DATA	HDMI_90D	HDMI	HDMI_IG_DATA_C_N<2..0>	7 9 36

D1 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	7 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	7 36
	1TO1_DIFFPAIR		CHGR_CSI_R_P	57
	1TO1_DIFFPAIR		CHGR_CSI_R_N	57
	1TO1_DIFFPAIR		CHGR_CSO_R_P	57
	1TO1_DIFFPAIR		CHGR_CSO_R_N	57
USB_BT	USB_85D	USB	USB_BT_CONN_P	36
USB_BT	USB_85D	USB	USB_BT_CONN_N	36
USB_BT	USB_85D	USB	USB_BT_WAKE_P	36
USB_BT	USB_85D	USB	USB_BT_WAKE_N	36
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	7 53 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_N	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_N	7 53 55 78
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_P	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	43 61 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	43 61 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	43
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	51 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	51 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_HI_RC	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_LO_RC	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_HI	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_LO	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_N	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_N	7 53 55 78
USB_TPAD	USB_85D	USB	USB_TPAD_R_P	26 47
USB_TPAD	USB_85D	USB	USB_TPAD_R_N	26 47
USB_HUB	USB_85D	USB	PU_USBHUB_DN4_P	9
USB_HUB	USB_85D	USB	PU_USBHUB_DN4_N	9
		SB_POWER	PP3V3_S5	7 8
		SB_POWER	PP3V3_S0	7 8
		SB_POWER	PP1V5_S3RS0_CPUDDR	8
		GND	GND	

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D1 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_MEM	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.120 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.079 MM	0.079 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

Stackup-Defined Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP,BOTTOM	0.1 MM	?
1:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.1 MM	?
1:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

J4 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
J4P1 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	9 33
J4P2 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	9 33
J4P3 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	9 33
J4P4 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	9 33
J4P5 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	9 33
J4P6 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	9 33
J4P7 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	9 33
J4P8 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	9 33
J4P72 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	33
J4P73 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	33
J4P74 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	33
J4P75 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	33
J4P76 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	33
J4P77 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	33
J4P78 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	33
J4P79 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	33
J4P62 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	9 67
J4P63 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	9 67
J4P68 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_C_P	9 67
J4P69 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_C_N	9 67
J4P67 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	7 67
J4P66 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	7 67
J4P56 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67
J4P55 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67
J4P54 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	
J4P53 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	
J4P41 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_RC_P	7 36
J4P42 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_RC_N	7 36
J4P43 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_F_P	7 38
J4P44 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_F_N	7 38
J4P45 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_C_P	7 38
J4P46 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_C_N	7 38
J4P47 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
J4P48 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36

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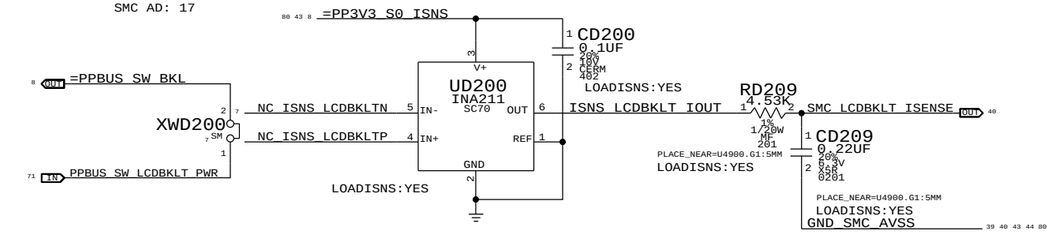
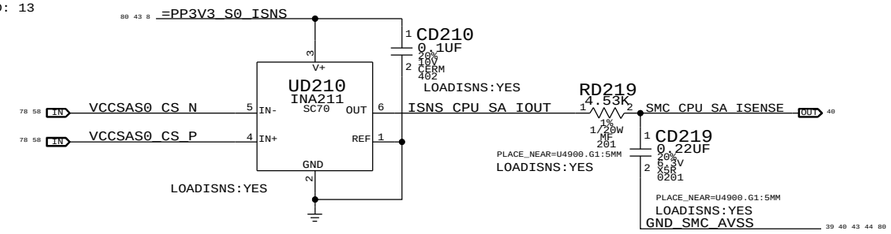
LCD Backlight Current Sense (IBLC)

Gain: 500x. EDP: 0.9 A
Rsense: 0.005 (RD200 / XWD200)
V across Rsense: 4.5 mV
SMC AD: 17



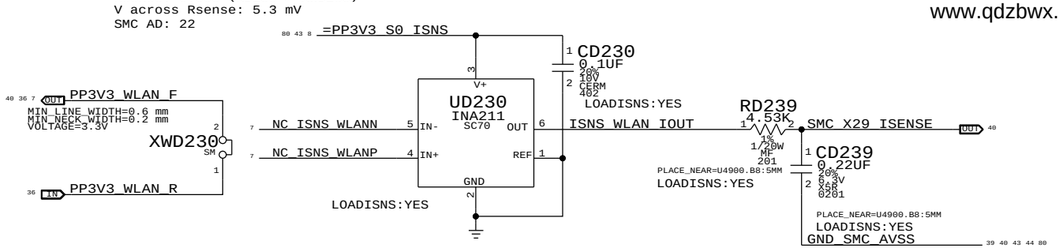
CPU SA Current Sense (IC2C)

Gain: 500x. EDP: 6 A
Rsense: 0.001 (R7140)
V across Rsense: 6 mV
SMC AD: 13



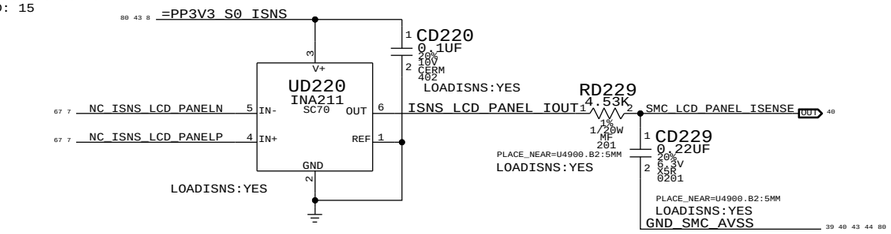
Airport X29 Current Sense (IAPC)

Gain: 500x. EDP: 1.06 A
Rsense: 0.005 (RD230 / XWD230)
V across Rsense: 5.3 mV
SMC AD: 22



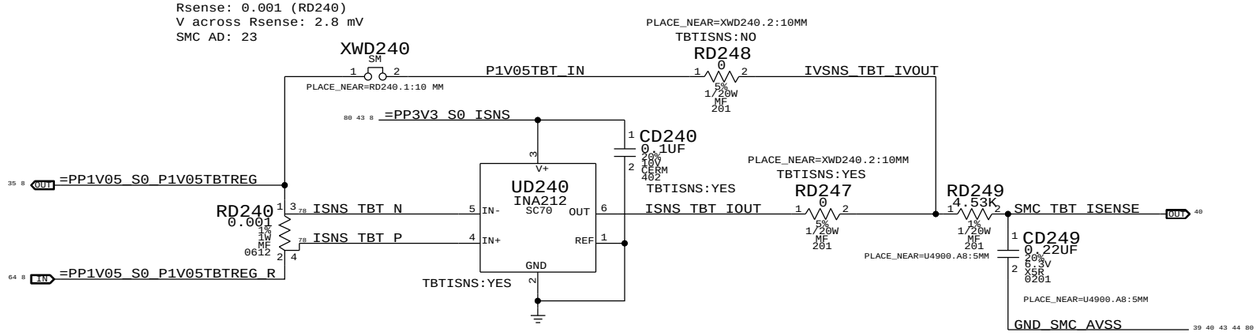
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
Rsense: 0.005 (R9020, XW9020)
V across Rsense: 5 mV
SMC AD: 15



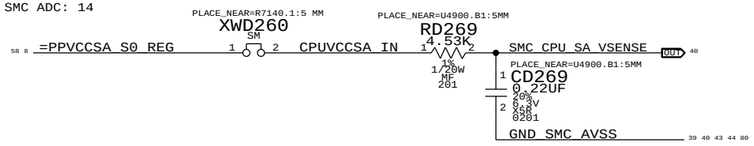
Thunderbolt TBT Current/Voltage Sense (IHSP/VHSP)

Gain: 1000x. EDP: 2.8 A
Rsense: 0.001 (RD240)
V across Rsense: 2.8 mV
SMC AD: 23



CPU SA Voltage Sense (VC2C)

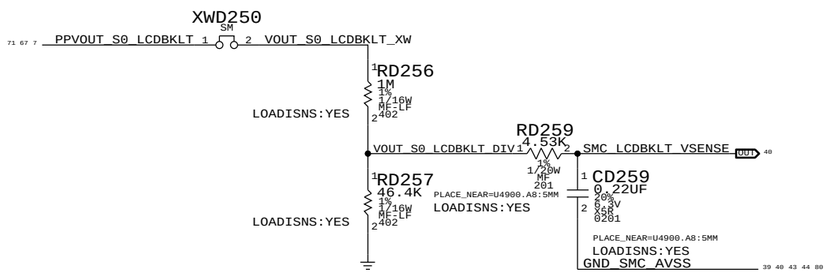
Gain: 1x
SMC ADC: 14



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD209,CD219,CD229		LOADISNS:NO
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD239,CD259		LOADISNS:NO

LCD Backlight Voltage Sense (VBLC)

Gain: 0.04434



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