Z50-HR(S204-SC) Schematics Document
Sandy Bridge
Intel PCH
2011-02-14
REV :-1

N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cover Page***

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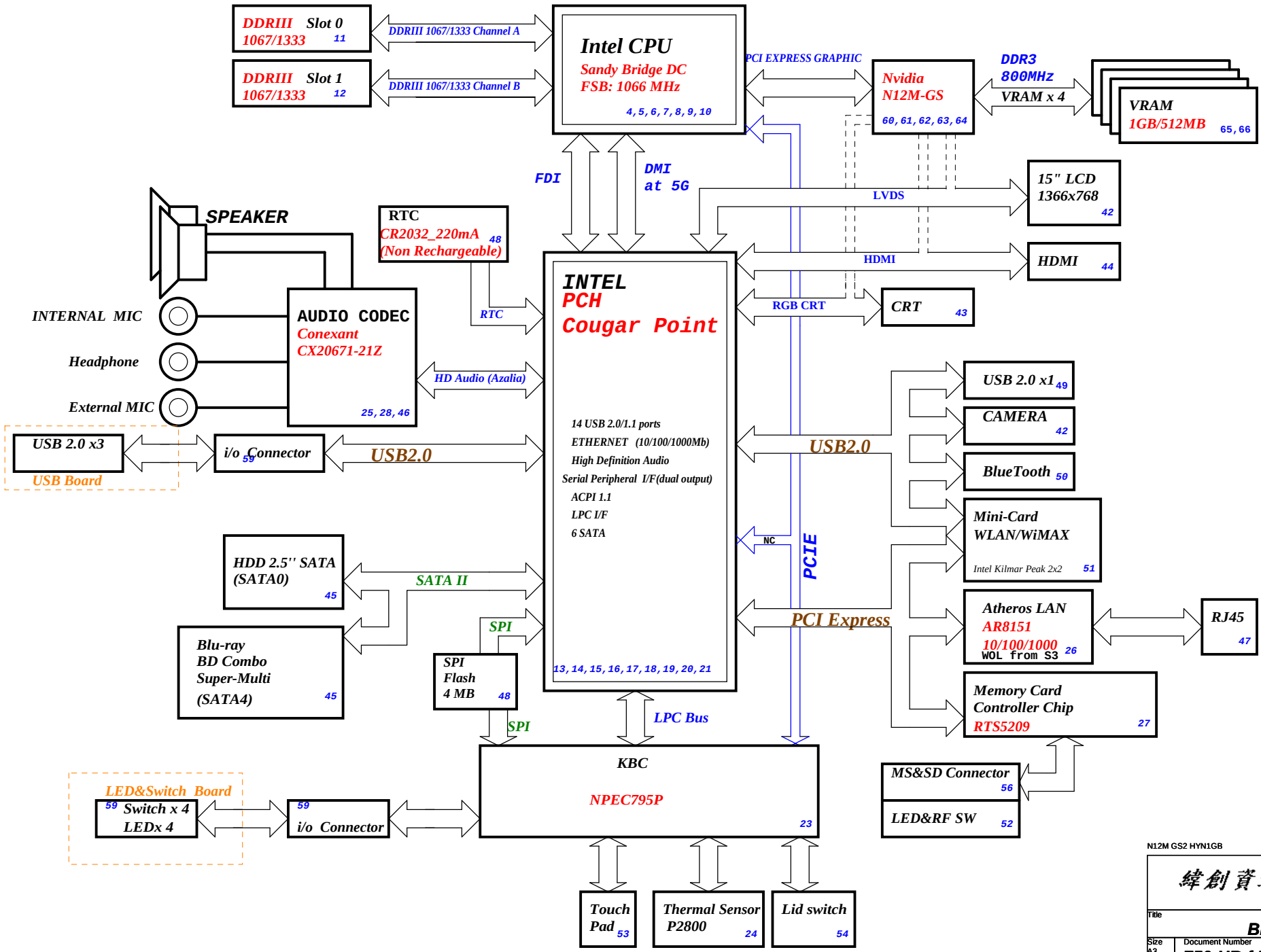
Z50-HR Block Diagram



CPU DC/DC ISL95831 35,36,37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51218D 38	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8223 34	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207 39	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC ISL95831HRTZ 37	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208A 67	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24725 33	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC RT9025 40	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC APL5916KAI-TRL-GP 41	
INPUTS	OUTPUTS
3D3V_S0	0D85V_S0

Switches 29	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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Title: **Block Diagram**

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

PCIE Routing

LANE1	Mini Card1(WLAN)
LANE2	Card Reader
LANE3	N/A
LANE4	GIGA LAN
LANE5	N/A
LANE6	N/A
LANE7	N/A
LANE8	N/A

SATA Table

SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	N/A

USB Table

Pair	Device	
0	USB Ext. port 2	OC#0
1	USB Ext. port 1	OC#1
2	USB Ext. port 4	OC#2
3		
4	USB Ext. port 3	OC#3
5	X	
6	X	
7	X	
8	X	
9	CAMERA	OC#5
10	X	
11	X	
12	Mini Card1 (WLAN)	
13	BLUETOOTH	OC#7

N12M GS2 HYN1GB

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SSID = CPU

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.
Lane reversal does not apply to FDI sideband signals.

If left as no connect, there is no functional impact, but power (~15 mW) may be wasted.

FDI_LSYNC0
FDI_FSYNC0
FDI_LSYNC1
FDI_FSYNC1
FDI_INT

R404 1KR2J-1-GP DIS
RN401 SRN1KJ-4-GP DIS 66.10236.08L

【DG 0.9 P.54】
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

EDP_COMPIO 4mil 24.9R VCCIO
EDP_ICOMPO 12mil

Port	Strap	Enable	Disable
eDP	CFG[4]	Pull down to GND through a 1K ± 5% resistor	No Connect
	EDP_HDP	Pull down to GND through a 1K ± 5% resistor	Pull high to CPU VCCIO through a 10K ± 5% resistor

【DG 0.9 P.32】
PEG_RCOMPO 4mil 24.9R VCCIO
PEG_ICOMPI
PEG_ICOMPO 12mil

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

CPU1A 1 OF 9 SANDY

DMI: DMI_TXN[3:0] DMI_TXP[3:0] DMI_RXN[3:0] DMI_RXP[3:0]
Intel(R) FDI: FDI_TXN[7:0] FDI_TXP[7:0] FDI_FSYNC0 FDI_FSYNC1 FDI_INT FDI_LSYNC0 FDI_LSYNC1
PCI EXPRESS* - GRAPHICS: PEG_RXN[0..15] PEG_RXP[0..15] PEG_TXN[0..15] PEG_TXP[0..15]
eDP: DP_COMP eDP_HPD EDP_COMPIO EDP_ICOMPO EDP_HPD EDP_AUX EDP_AUX# EDP_TX0 EDP_TX1 EDP_TX2 EDP_TX3

R401 1 24D9R2F-L-GP 1D05V_VTT
R402 1 24D9R2F-L-GP 1D05V_VTT
R403 1 10KR2J-3-GP

eDP Disable

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal
close to the processor

C421–C452 DIS SCD22U10V2KX-1GP

ARRAN

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Title: CPU (PCIE/DMI/FDI)
Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1
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SSID = CPU

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

【CHKLST 6.9 P.53 】

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

CPU1B — 2 OF 9 — SANDY

MISC: SNB_IVB#, SKTOCC#
THERMAL: CATERR#, PECI, PROCHOT#, THERMTRIP#
PM_SYNC, UNCOREPWRGOOD, SM_DRAMPWROK, RESET#

CLOCKS: BCLK, BCLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK#
DDR3 MISC: SM_DRAMRST#, SM_RCOMP0, SM_RCOMP1, SM_RCOMP2
JTAG & BPM: PRDY#, PREQ#, TCK, TMS, TRST#, TDI, TDO, DBR#, BPM#0–BPM#7

ARRAN

close to the processor

+V_NVRAM_VCCQ — R517 2K2R2J-2-GP — 14 H_SNB_IVB# — C26 SNB_IVB#

Do Not Stuff TP501 — SKTOCC# R — AN34 SKTOCC#

Do Not Stuff TP502 — H_CATERR# — AL33 CATERR#

18,23 H_PECI — AN33 PECI

close to the processor

23,35 H_PROCHOT# — 1D05V_VTT — R501 62R2J-GP — R516 56R2J-4-GP 63.56034.1DL — H_PROCHOT# R — AL32 PROCHOT#

18,22 H_THERMTRIP# — AN32 THERMTRIP# — 1D05V_VTT — R523 56R2J-4-GP

Connect EC to PROCHOT# through inverting OD buffer.

15 H_PM_SYNC — AM34 PM_SYNC

18,69 H_CPUPWRGD — R504 Do Not Stuff — H_CPUPWRGD_R — AP33 UNCOREPWRGOOD

close to the processor

15,30 PM_DRAM_PWRGD — R503 10KR2J-3-GP — NO_S8 R524 Do Not Stuff — VDDPWRGOOD — V8 SM_DRAMPWROK

1D05V_VTT — NO_S8 R521 Do Not Stuff

30 VDDPWRGOOD

14,22,23,26,27,51,55,60,69 PLT_RST# — R510 1KR2F-2-GP — BUF_CPU_RST# — AR33 RESET# — R509 750R2F-GP

BCLK A28 — CLK_EXP_P 16
BCLK# A27 — CLK_EXP_N 16

DPLL_REF_SSCLK A16 — CLK_DP_P_R — DIS SRN1KJ-7-GP EVT — RN503 — 1D05V_VTT
DPLL_REF_SSCLK# A15 — CLK_DP_N_R

R502 4K99R2F-L-GP

SM_DRAMRST# R8 — SM_DRAMRST# 30

SM_RCOMP0 AK1 — SM_RCOMP_0 R506 140R2F-GP
SM_RCOMP1 A5 — SM_RCOMP_1 R507 25D5R2F-GP
SM_RCOMP2 A4 — SM_RCOMP_2 R508 200R2F-L-GP

Signal Routing Guideline:
SM_RCOMP[0,1] keep W/S=20/20 mils and routing length less than 500 mils.
SM_RCOMP[2] keep W/S=15/20 mils and routing length less than 500 mils.

PRDY# AP29 — XDP_PRDY#
PREQ# AP27 — XDP_PREQ#
TCK AR26 — XDP_TCLK
TMS AR27 — XDP_TMS
TRST# AP30 — XDP_TRST#
TDI AR28 — XDP_TDI
TDO AP26 — XDP_TDO
DBR# AL35 — XDP_DBRESET#

3D3V_S0 — R513 1KR2J-1-GP — EVT

BPM#0 AT28 — XDP_BPM0
BPM#1 AR29 — XDP_BPM1
BPM#2 AR30 — XDP_BPM2
BPM#3 AT30 — XDP_BPM3
BPM#4 AP32 — XDP_BPM4
BPM#5 AR31 — XDP_BPM5
BPM#6 AT31 — XDP_BPM6
BPM#7 AR32 — XDP_BPM7

1D05V_VTT — RN501 DY — XDP_TDI, XDP_TMS, XDP_TCLK — Do Not Stuff

1D05V_VTT — RN502 — XDP_TRST#, XDP_TDO — SRN51J-GP

XDP Test Point

XDP_PRDY#	TP12	Do Not Stuff
XDP_PREQ#	TP13	Do Not Stuff
XDP_BPM0	TP14	Do Not Stuff
XDP_BPM1	TP15	Do Not Stuff
XDP_BPM2	TP18	Do Not Stuff
XDP_BPM3	TP16	Do Not Stuff
XDP_BPM4	TP19	Do Not Stuff
XDP_BPM5	TP20	Do Not Stuff
XDP_BPM6	TP21	Do Not Stuff
XDP_BPM7	TP22	Do Not Stuff

62.10055.321

Buffered reset to CPU

1D05V_VTT — R514 Do Not Stuff DY — 3D3V_S0 — C501 Do Not Stuff DY

U501 (NC#1, A, GND, VCC, Y)
14,22,23,26,27,51,55,60,69 PLT_RST# — BUFO_CPU_RST# — DY R515 Do Not Stuff — BUF_CPU_RST#
DY Do Not Stuff
R512 Do Not Stuff DY

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Title: CPU (THERMAL/CLOCK/PM)

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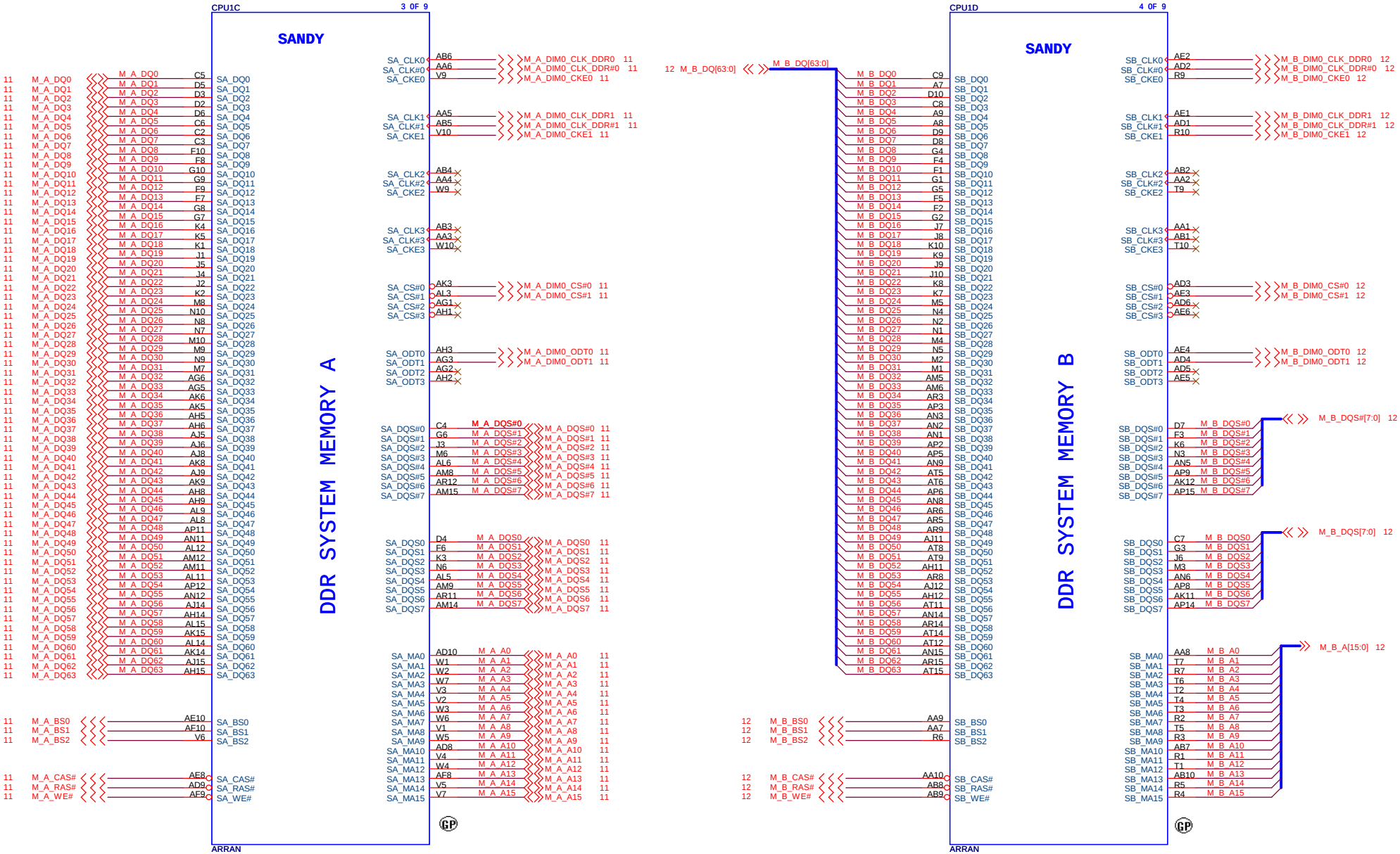
SSID = CPU



N12M GS2 HYN1GB

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Title: CPU (DDR)

Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

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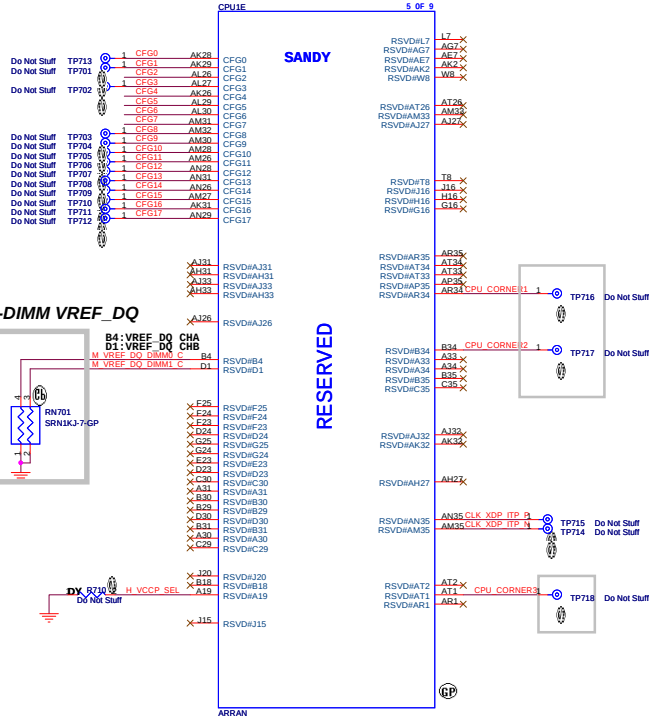
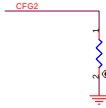
SSID = CPU

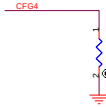


M3 - Processor Generated SO-DIMM VREF_DQ

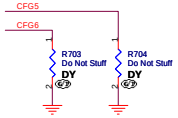
PEG Static Lane Reversal	
CFG[0]	Connect a series 1K ohm resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.



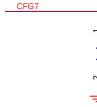
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port Can float on Processor if eDP interface is disabled 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: CPU (RESERVED)

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SSID = CPU

POWER

CPU1F

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SANDY

ARRAN

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

PROCESSOR CORE POWER

VCC_CORE

53A

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 F14 E12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

1D05V_VTT

C805 SC22U6D3V5MX-2GP; C806 SC22U6D3V5MX-2GP; C807 SC22U6D3V5MX-2GP; C808 SC10U6D3V5KX-1GP; C809 SC10U6D3V5KX-1GP; C810 SC22U6D3V5MX-2GP; C838 SC22U6D3V5MX-2GP; C839 SC22U6D3V5MX-2GP; C840 SC22U6D3V5MX-2GP; C841 SC10U6D3V5KX-1GP

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

C812 SC22U6D3V5MX-2GP; C813 SC22U6D3V5MX-2GP; C814 Do Not Stuff; C829 SC10U6D3V5KX-1GP; C830 SC10U6D3V5KX-1GP; C842 SC22U6D3V5MX-2GP; C843 SC10U6D3V5KX-1GP; C844 SC22U6D3V5MX-2GP; C845 SC10U6D3V5KX-1GP

C801 C802 C803 C804 C811 — Do Not Stuff

C820 C819 C818 C817 C815 — Do Not Stuff

C816 C821 C822 C823 C824 SC10U6D3V5KX-1GP; C825 C826 Do Not Stuff; C827 SC10U6D3V5KX-1GP

C837 Do Not Stuff; C836 SC10U6D3V5KX-1GP; C835 Do Not Stuff; C834 SC10U6D3V5KX-1GP; C833 SC10U6D3V5KX-1GP; C832 SC22U6D3V5MX-2GP; C831 SC22U6D3V5MX-2GP; C828 SC10U6D3V5KX-1GP

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 1 43R2J-GP VR_SVID_ALERT# 35
VIDSCLK AJ30 H_CPU_SVIDCLK H_CPU_SVIDCLK 35
VIDSOUT AJ28 H_CPU_SVIDDAT H_CPU_SVIDDAT 35

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V_VTT — H_CPU_SVIDDAT R807 1 130R2F-1-GP

SENSE LINES

1D05V_VTT — R804 10R2F-L-GP

VCC_CORE — R801 10R2F-L-GP

R801,R802 close to CPU

VCC_SENSE AJ35 — VCCSENSE 35
VSS_SENSE AJ34 — VSSSENSE 35

VCCIO_SENSE B10 — VCCIO_SENSE 38
VSSIO_SENSE A10 — VSSIO_SENSE 38

R802 10R2F-L-GP

R805 10R2F-L-GP

ED801 VARISTOR-5V-1-GP; ED802 VARISTOR-5V-1-GP

PVT

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: Z50-HR { Huron River Platform} | Rev: -1

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SSID = CPU

POWER

20110117

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 UMA, C903 UMA, C904 UMA, C905 UMA, C906 UMA — Do Not Stuff

C907 UMA, C908 UMA, C918 DY, C919 DY, C920 UMA — Do Not Stuff

CPU1G — SANDY — GRAPHICS

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17 — VAXG

SENSE LINES

VAXG_SENSE — AK35
VSSAXG_SENSE — AK34

VCC_AXG_SENSE 35
VSS_AXG_SENSE 35

VREF

SM_VREF — AL1 — +V_SM_VREF_CNT

DDR3 -1.5V RAILS

VDDQ: AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

SA RAIL

VCCSA: M27 M26 L26 J26 J25 J24 H26 H25

MISC

VCCSA_SENSE — H23 — VCCSA_SENSE

FC_C22 — C22 — H_FC_C22
VCCSA_VID1 — C24 — VCCSA_SEL — VCCSA_SEL 41

1.8V RAIL

VCCPLL: B6 A6 A2

ARRAN

R906,R907 close to CPU

VCC_GFXCORE

R906 Do Not Stuff UMA — DVT

R907 Do Not Stuff UMA

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

PVT

ED901 VARISTOR-5V-1-GP, ED902 VARISTOR-5V-1-GP

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

1D5V_DDR_S0

PROCESSOR VDDQ: 10A

C909 SC22U6D3V5MX-2GP; C910 SC10U6D3V5KX-1GP; C911 SC10U6D3V5KX-1GP; C912 SC10U6D3V5KX-1GP; C913 SC10U6D3V5KX-1GP; C914 SC10U6D3V5KX-1GP; TC901 Do Not Stuff DY

0D85V_S0

PROCESSOR VCCSA: 6A

C916 SC10U6D3V5KX-1GP; C915 SC10U6D3V5KX-1GP; C917 SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0D85V_S0

R902 10R2J-2-GP — **R902 need be close to pin H23.**

RN901 SRN10KJ-5-GP

H_FC_C22 — TP901 Do Not Stuff
VCCSA_SENSE — TP902 Do Not Stuff

EVT
20100910 Del R904,R905,R901

VCC_GFXCORE

R903 0R3J-0-U-GP DIS

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V_S0

PROCESSOR VCCPLL: 1.2A

C902 DY, C923 DY, C922 DY, C924 SC1U10V2KX-1GP — Do Not Stuff

N12M GS2 HYN1GB

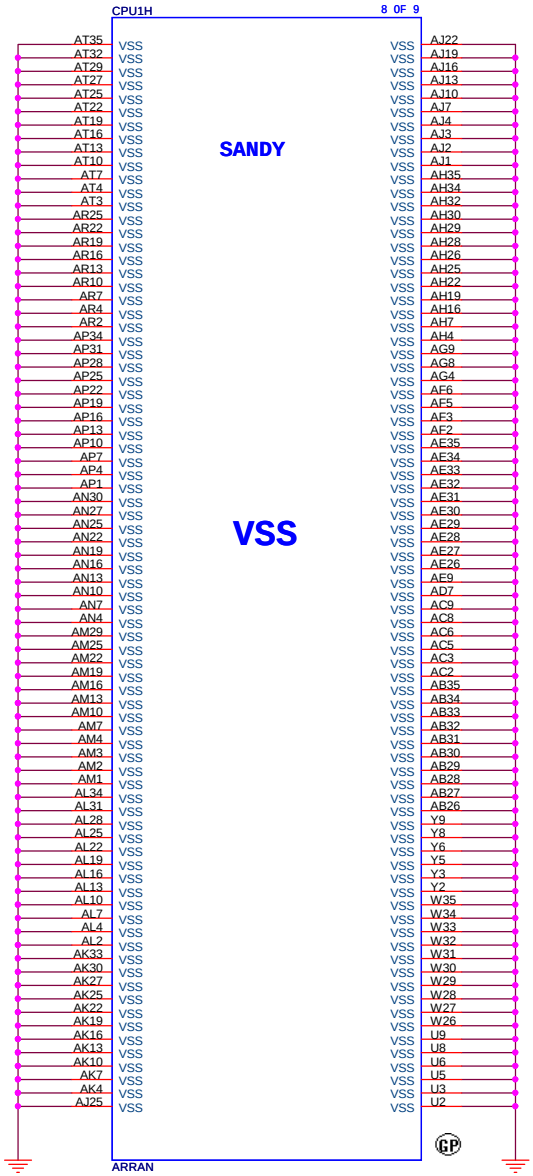
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

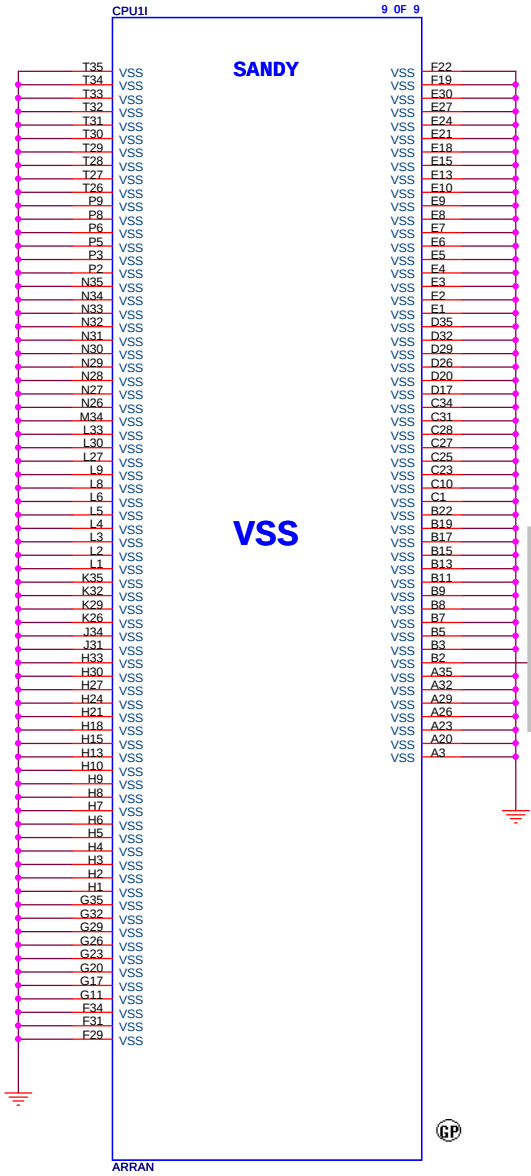
Title: CPU (VCC_GFXCORE)

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 9 of 74

SSID = CPU





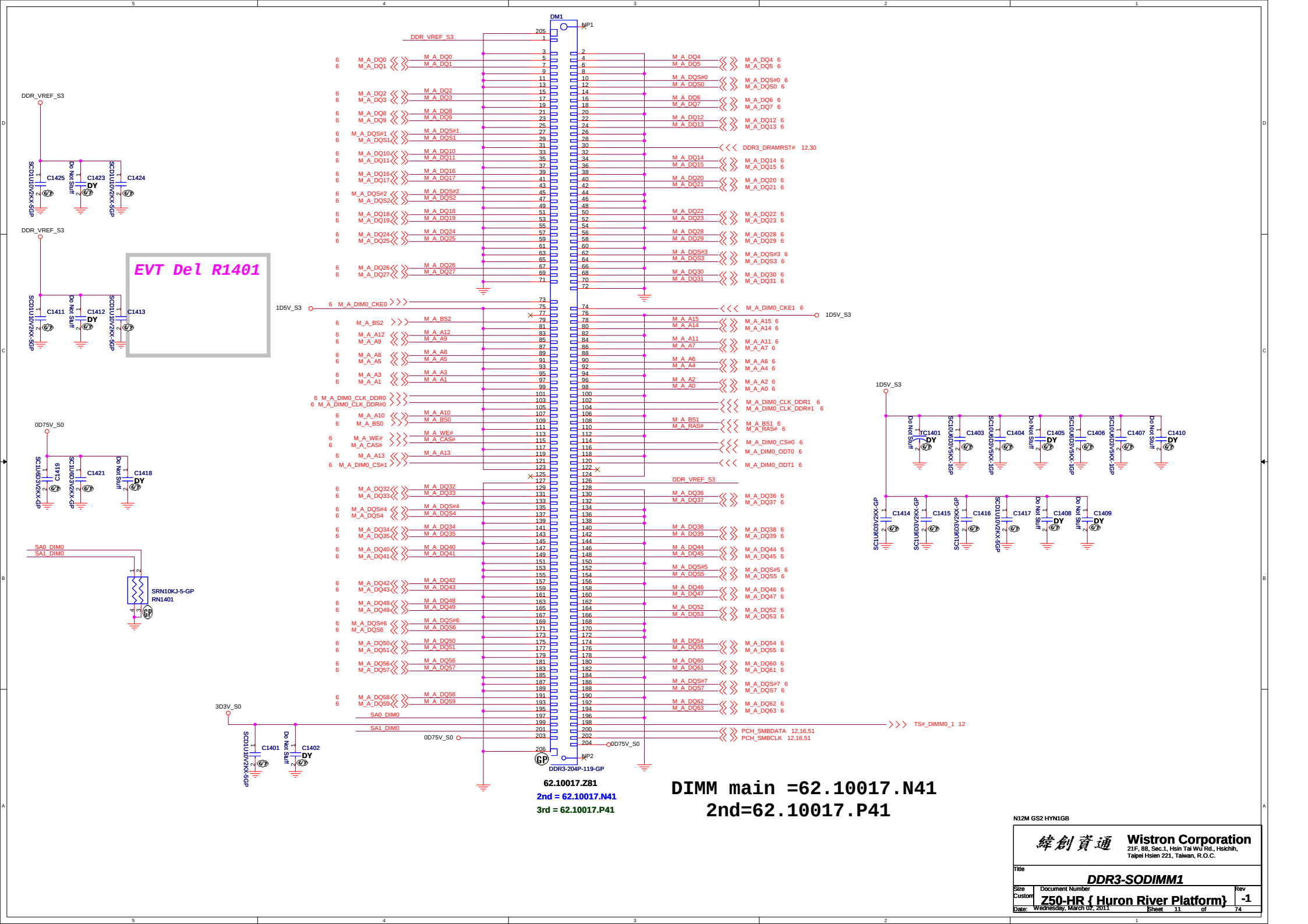
N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

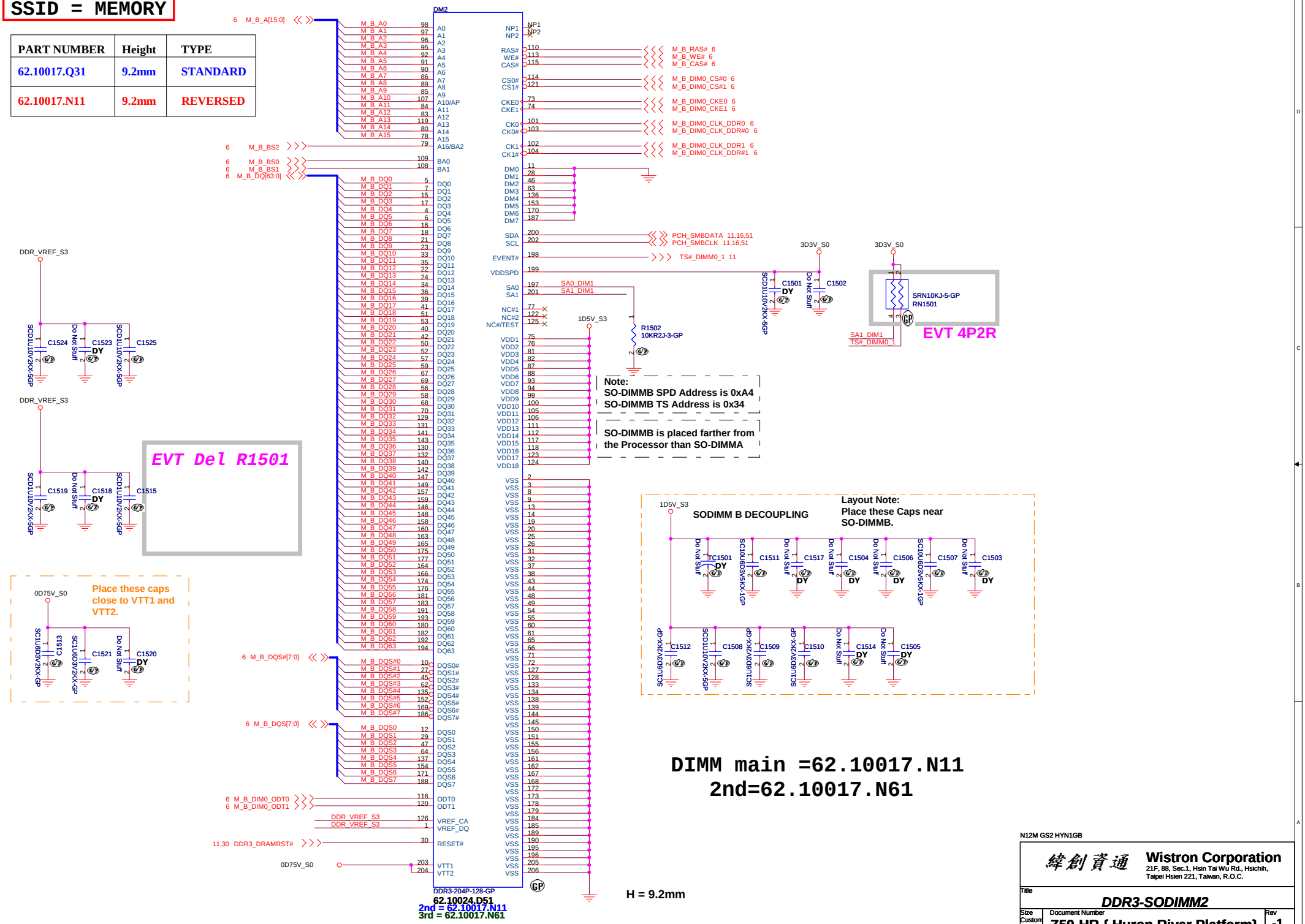
Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

Date: Wednesday, March 02, 2011 Sheet 10 of 74


DM1
DDR3-204P-119-GP
DDR_VREF_S3
M_A_DQ0
M_A_DQ1
M_A_DQ2
M_A_DQ3
M_A_DQ8
M_A_DQ9
M_A_DQS#1
M_A_DQS1
M_A_DQ10
M_A_DQ11
M_A_DQ16
M_A_DQ17
M_A_DQS#2
M_A_DQS2
M_A_DQ18
M_A_DQ19
M_A_DQ24
M_A_DQ25
M_A_DQ26
M_A_DQ27
M_A_DQ4
M_A_DQ5
M_A_DQS#0
M_A_DQS0
M_A_DQ6
M_A_DQ7
M_A_DQ12
M_A_DQ13
DDR3_DRAMRST# 12,30
M_A_DQ14
M_A_DQ15
M_A_DQ20
M_A_DQ21
M_A_DQ22
M_A_DQ23
M_A_DQ28
M_A_DQ29
M_A_DQS#3
M_A_DQS3
M_A_DQ30
M_A_DQ31
1D5V_S3
M_A_DIM0_CKE0
M_A_DIM0_CKE1 6
M_A_BS2
M_A_A12
M_A_A9
M_A_A8
M_A_A5
M_A_A3
M_A_A1
M_A_A15
M_A_A14
M_A_A11
M_A_A7
M_A_A6
M_A_A4
M_A_A2
M_A_A0
M_A_DIM0_CLK_DDR0
M_A_DIM0_CLK_DDR#0
M_A_DIM0_CLK_DDR1 6
M_A_DIM0_CLK_DDR#1 6
M_A_A10
M_A_BS0
M_A_BS1
M_A_RAS#
M_A_WE#
M_A_CAS#
M_A_DIM0_CS#0
M_A_DIM0_ODT0
M_A_A13
M_A_DIM0_CS#1
M_A_DIM0_ODT1
M_A_DQ32
M_A_DQ33
M_A_DQS#4
M_A_DQS4
M_A_DQ34
M_A_DQ35
M_A_DQ40
M_A_DQ41
M_A_DQ36
M_A_DQ37
M_A_DQ38
M_A_DQ39
M_A_DQ44
M_A_DQ45
M_A_DQS#5
M_A_DQS5
M_A_DQ42
M_A_DQ43
M_A_DQ48
M_A_DQ49
M_A_DQ46
M_A_DQ47
M_A_DQ52
M_A_DQ53
M_A_DQS#6
M_A_DQS6
M_A_DQ50
M_A_DQ51
M_A_DQ56
M_A_DQ57
M_A_DQ54
M_A_DQ55
M_A_DQ60
M_A_DQ61
M_A_DQS#7
M_A_DQS7
M_A_DQ58
M_A_DQ59
M_A_DQ62
M_A_DQ63
3D3V_S0
SA0_DIM0
SA1_DIM0
0D75V_S0
TS#_DIMM0_1 12
PCH_SMBDATA 12,16,51
PCH_SMBCLK 12,16,51
NP1
NP2
C1401
C1402
C1403
C1404
C1405
C1406
C1407
C1408
C1409
C1410
C1411
C1412
C1413
C1414
C1415
C1416
C1417
C1418
C1419
C1421
C1423
C1424
C1425
TC1401
SRN10KJ-5-GP
RN1401
Do Not Stuff
DY
EVT Del R1401
62.10017.Z81
2nd = 62.10017.N41
3rd = 62.10017.P41
DIMM main =62.10017.N41
2nd=62.10017.P41
N12M GS2 HYN1GB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR3-SODIMM1
Size
Custom
Document Number
Z50-HR { Huron River Platform}
Rev
-1
Date: Wednesday, March 02, 2011
Sheet 11 of 74

SSID = MEMORY

PART NUMBER	Height	TYPE
62.10017.Q31	9.2mm	STANDARD
62.10017.N11	9.2mm	REVERSED



DIMM main =62.10017.N11
2nd=62.10017.N61

H = 9.2mm

N12M GS2 HYN1GB

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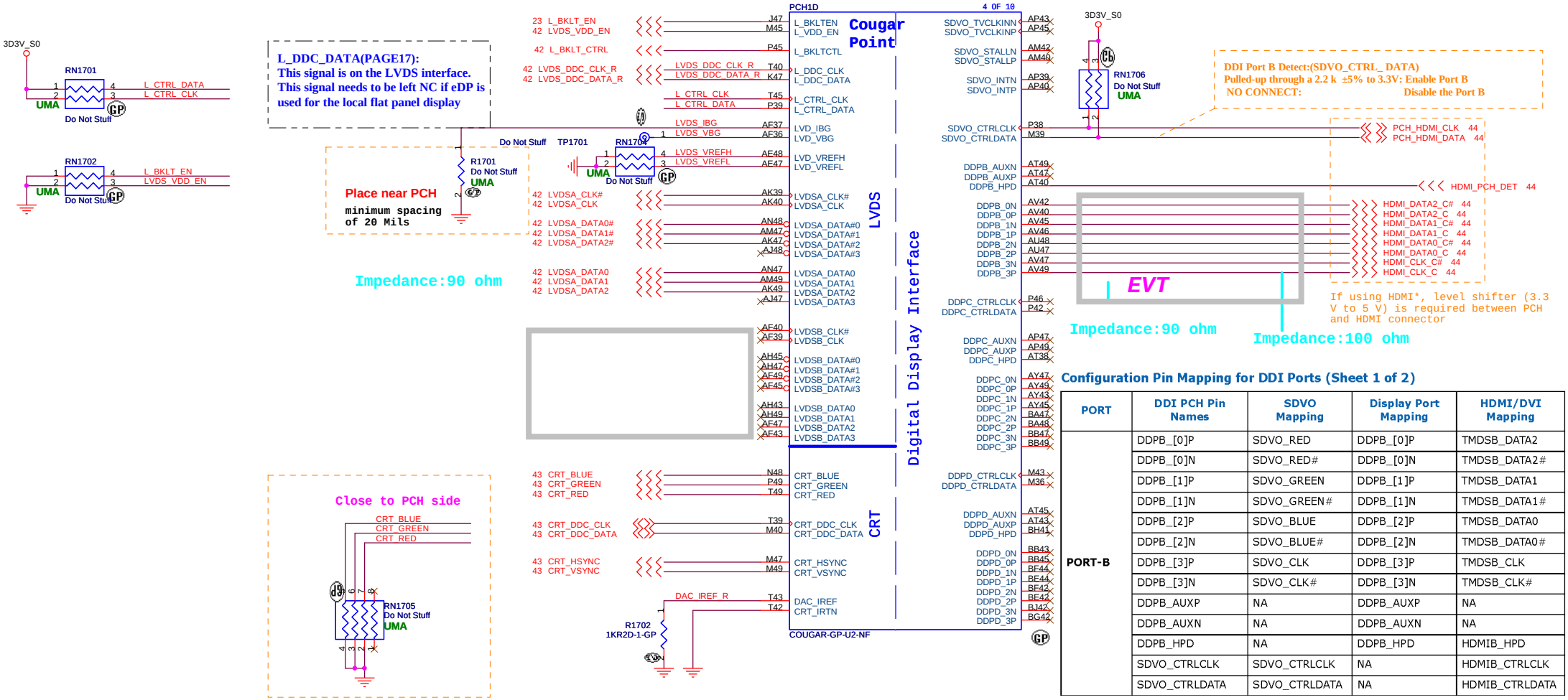
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: Custom | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 12 of 74

CHANGE TO 71.0HM65.00U



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

N12M GS2 HYN1GB

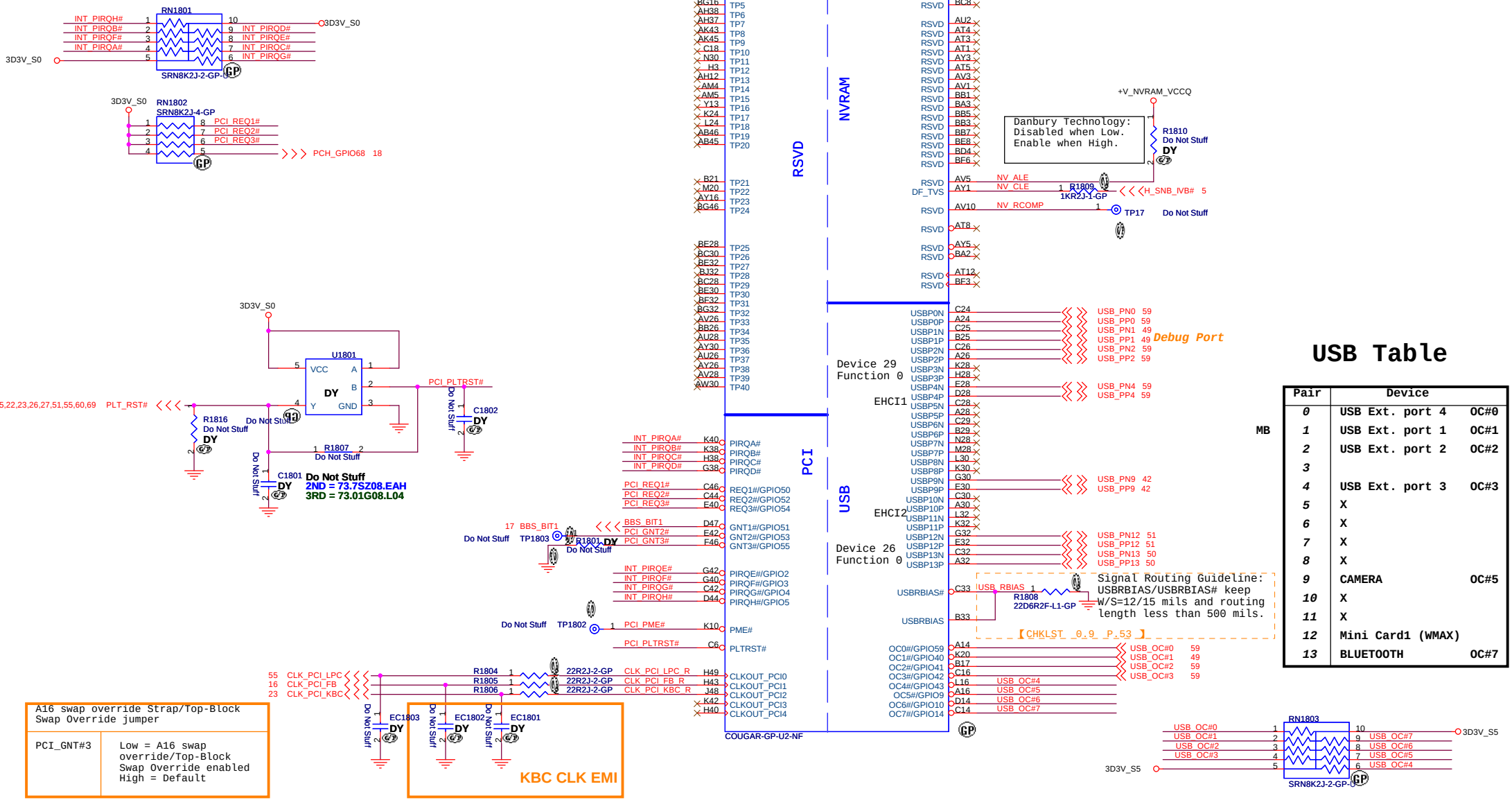
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 13 of 74

SSID = PCH



USB Table

MB

Pair	Device	
0	USB Ext. port 4	OC#0
1	USB Ext. port 1	OC#1
2	USB Ext. port 2	OC#2
3		
4	USB Ext. port 3	OC#3
5	X	
6	X	
7	X	
8	X	
9	CAMERA	OC#5
10	X	
11	X	
12	Mini Card1 (WMAX)	
13	BLUETOOTH	OC#7

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

N12M GS2 HYN1GB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 14 of 74

SSID = PCH

For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

PCH1C — 3 OF 10 — Cougar Point

DMI: DMI_RXN[3:0], DMI_RXP[3:0], DMI_TXN[3:0], DMI_TXP[3:0]
FDI: FDI_TXN[7:0], FDI_TXP[7:0], FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

1D05V_VTT
R1904 1 49D9R2F-GP DMI_COMP_R
R1907 1 750R2F-GP RBIAS_CPY

System Power Management:
SUS_PWR_ACK, R1902 Do Not Stuff, SUSACK#
3D3V_S0, R1905 10KR2J-3-GP, SYS_RESET#
29 SYS_PWROK, DY R1921 Do Not Stuff, DY R1923 Do Not Stuff
PVT
22,23,29,35,44 S0_PWR_GOOD, R1911 1KR2J-1-GP, R1910 10KR2J-3-GP, PWROK
29,35,41 PWR_VCCSA_PWRGD, DY R1906 Do Not Stuff, R1903 Do Not Stuff, MEPWROK
5,30 PM_DRAM_PWRGD
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms
PM_RSMRST#
23 SUS_PWR_ACK
23,69 PM_PWRBTN#
23,63 AC_PRESENT
R1908 100KR2J-1-GP PM_RSMRST#
16 BATLOW#
PM_RI#
VccASW Suspend 1D05_VTT
OD Output
internal pull-up

DSWVRMEN, DSWODVREN
DPWROK, PCH_DPWROK, R1927 Do Not Stuff, PM_RSMRST#
WAKE#, PCIE_WAKE# 26,51
CLKRUN#/GPIO32, PM_CLKRUN# 23
SUS_STAT#/GPIO61, PM_SUS_STAT#, TP1901 Do Not Stuff
SUSCLK/GPIO62, SUS_CLK, R1913 Do Not Stuff, PCH_SUSCLK_KBC 23
SLP_S5#/GPIO63, PM_SLP_S5#, TP1902 Do Not Stuff
SLP_S4#, SLP_S4#_R, R1914 Do Not Stuff, PM_SLP_S4# 23,29,39
SLP_S3#, SLP_S3#_R, R1915 Do Not Stuff, PM_SLP_S3# 23,29,30,40,45,67
SLP_A#, PM_SLP_A#, TP1903 Do Not Stuff
SLP_SUS#, PM_SLP_SUS#, TP1904 Do Not Stuff
PMSYNCH, H_PM_SYNC, H_PM_SYNC 5
SLP_LAN#/GPIO29, PM_SLP_LAN#, TP1905 Do Not Stuff

SUSWARN#/SUSPWRDNACK/GPIO30
PWROK
BATLOW#/GPIO72
RSMRST#
ACPRESENT/GPIO31

COUGAR-GP-U2-NF

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5
R1917 330KR2J-1-GP
DSWODVREN
DY R1918 Do Not Stuff

Deep S4/S5 Supported | Deep S4/S5 **Not** Supported
VccDSW3_3
DPWROK
VccSUS3_3
RSMRST#

PVT
3D3V_S5
SUS_PWR_ACK, R1925 Do Not Stuff DY
RN1901 SRN10KJ-6-GP
AC_PRESENT
PCIE_WAKE#
PM_RI#
PM_PWRBTN#, R1922 Do Not Stuff DY
PM_SLP_LAN#, R1920 10KR2J-3-GP
EVT
3D3V_S0
PM_CLKRUN#, R1919 8K2R2J-3-GP

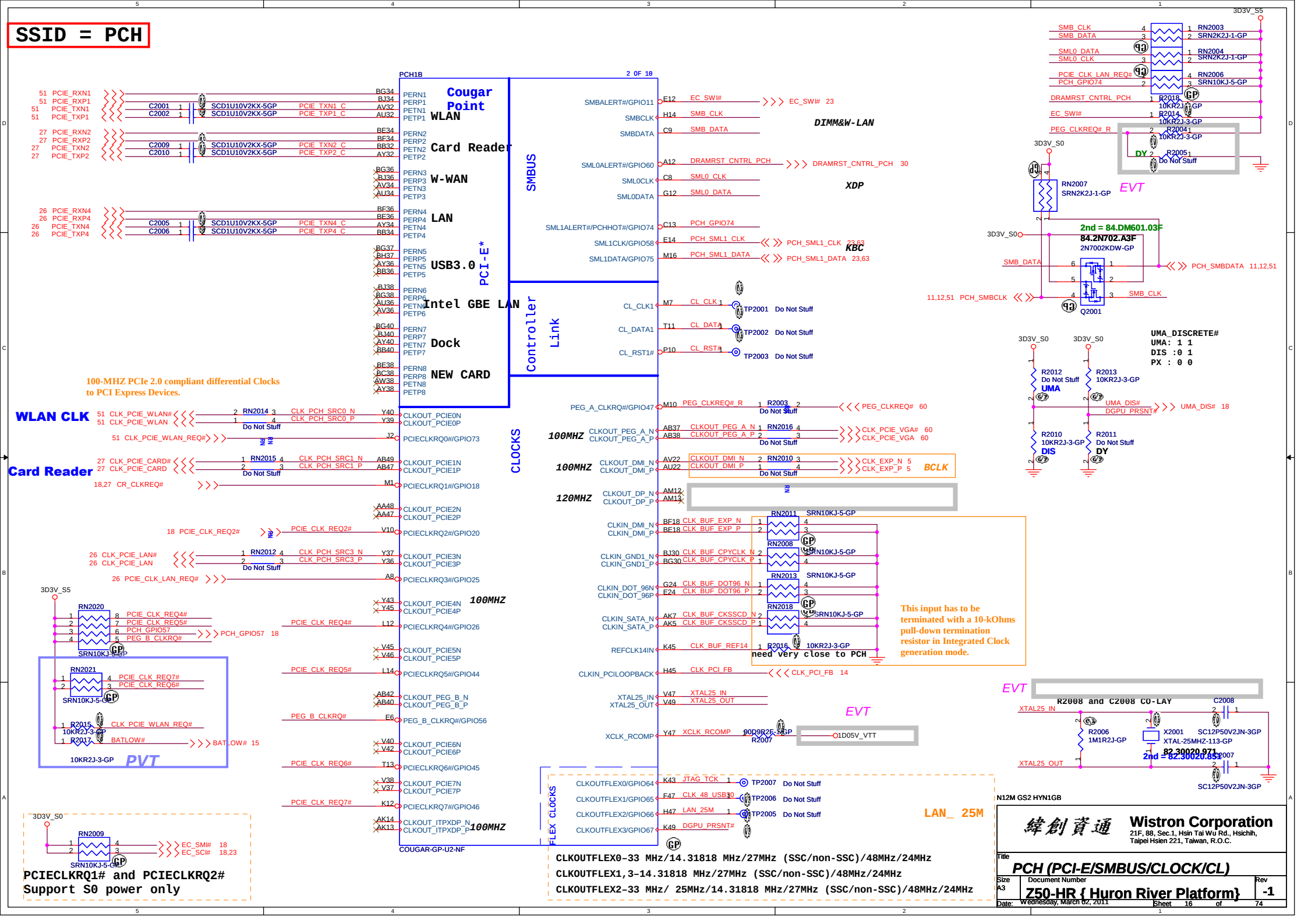
PVT
PWROK, Q1904 DY, S0_PWR_GOOD, G680_RST#
5V_AUX_S5, C1901 SCD1U10V2KX-5GP
U1901 G680LT1UF-GP 74.00680.A7F
VCC, RESET#/RESET, HTH, GND, LTH
DCBATOUT
R1929 820KR2F-GP
R1930 15KR2F-GP
R1931 165KR2F-GP
3D3V_AUX_S5
R1909 100KR2J-1-GP
R1916 10KR2J-3-GP
Q1901 2N7002KDW-GP 84.2N702.A3F 2nd = 84.DM601.03F
3V_5V_POK#
R1912 1KR2J-1-GP
3V_5V_POK 34
RSMRST#_KBC 23
PM_RSMRST#
PWROK, R1924 0R2J-2-GP
D1901 BAS70-05-7-F-GP 83.BAS70.C11
G680_RST#
22 G680_RST#

N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**
Size: A3 | Document Number: **Z50-HR { Huron River Platform}** | Rev: -1
Date: Wednesday, March 02, 2011 | Sheet 15 of 74

SSID = PCH



N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 16 of 74

SSID = PCH

Intruder Detect: 【EDS 1.0 P.195】

This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.

Functional Strap Definitions

【EDS 1.0 P.89】

RTC_X1 — R2101 10MR2J-L-GP — RTC_X2

X2101 X-32D768KHZ-34GPU

C2101 SC5D06P50V2CN-1GP

C2102 SC5D6P50V2CN-1GP

82.30001.661

2ND = 82.30001.B21

GPIO33

Pull-down with 1K is recommended for manufacturing environment.
There is an internal pull-up of 20 k for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.

1. HDA_SDO and HDA_BCLK must be length matched to within 500 mils
2. HDA_DOCK_EN#length matched of 500 mils with HDA_BCLK.

【EDS 1.0 P.92】

EVT

+3VS_HDA_IO — R2103 1KR2J-1-GP — HDA_SYNC

R2124 33R2J-2-GP

25 CODEC_SYNC

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used tosample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform. co-operate with R2310

On-Die PLL Voltage Regulator Voltage Select	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

NO REBOOT STRAP 【EDS 1.0 P.89】

Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature)

3D3V_S0 — DY R2106 Do Not Stuff — HDA_SPKR

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

Flash Descriptor Security Override/ ME Debug Mode	
HDA_SDOUT	Low = Default High = Enable 【EDS 1.0 P.92】

+3VS_HDA_IO — DY R2107 Do Not Stuff — HDA_SDOUT

RTC_AUX_S5 — R2115 20KR2F-L-GP — R2116 20KR2F-L-GP — C2103 SC1U6D3V2KX-GP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided

C2104 SC1U6D3V2KX-GP — G2101 DY Do Not Stuff

RTC_AUX_S5 — R2104 1M1R2J-GP — R2105 330KR2F-L-GP

INTVRMEN- Integrated SUS 【EDS 1.0 P.90】
1.05V VRM Enable
High - Enable internal 1.05 V regulators.
Low - Enable external 1.05 V regulators.
NOTE: This signal should always be pulled high

LPC_AD0_PCH — C2105 SC22P50V2JN-4GP
LPC_AD1_PCH — C2107 SC22P50V2JN-4GP
LPC_AD2_PCH — C2108 SC22P50V2JN-4GP
LPC_AD3_PCH — C2109 SC22P50V2JN-4GP
LPC_FRAME#_PCH — C2110 DY Do Not Stuff

PVT

PCH_SPI_CS0# — EC2104 DY Do Not Stuff

PCH1A 1 OF 10

Cougar Point

RTC: RTCX1 A20 — RTC_X1; RTCX2 C20 — RTC_X2; RTCRST# D20 — RTC_RST#; SRTCRST# G22 — SRTC_RST#; INTRUDER# K22 — SM_INTRUDER#; INTVRMEN C17 — PCH_INTVRMEN

LPC: FWH0/LAD0 C38 — LPC_AD0_PCH; FWH1/LAD1 A38 — LPC_AD1_PCH; FWH2/LAD2 B37 — LPC_AD2_PCH; FWH3/LAD3 C37 — LPC_AD3_PCH; FWH4/LFRAME# D36 — LPC_FRAME# PCH; LDRQ0# E36; LDRQ1#/GPIO23 K36 — internal pull Up; SERIRQ V5 — INT_SERIRQ 23

PVT

LPC_AD[0..3] — R2127 47R2J-2-GP LPC_AD0; R2128 47R2J-2-GP LPC_AD1; R2129 47R2J-2-GP LPC_AD2; R2130 47R2J-2-GP LPC_AD3 — LPC_AD[0..3] 23,55

R2126 0R2J-2-GP — LPC_FRAME# 23,55

SATA 6G: SATA0RXN AM3 — SATA_RXN0 45; SATA0RXP AM1 — SATA_RXP0 45; SATA0TXN AP7 — SATA_TXN0 45; SATA0TXP AP5 — SATA_TXP0 45

HDD1

SATA1RXN AM10; SATA1RXP AM8; SATA1TXN AP11; SATA1TXP AP10

INT_SERIRQ — R2111 10KR2J-3-GP — 3D3V_S0

SATA2RXN AD7; SATA2RXP AD5; SATA2TXN AH5; SATA2TXP AH4

SATA3RXN AB8; SATA3RXP AB10; SATA3TXN AF3; SATA3TXP AF1

SATA: SATA4RXN Y7 — SATA_RXN4 45; SATA4RXP Y5 — SATA_RXP4 45; SATA4TXN AD3 — SATA_TXN4 45; SATA4TXP AD1 — SATA_TXP4 45

ODD

SATA5RXN Y3; SATA5RXP Y1; SATA5TXN AB3; SATA5TXP AB1

SATAICOMPO Y11; SATAICOMPI Y10 — SATA_COMP R2112 37D4R2F-GP — 1D05V_VTT

Place the resistor within 500 mils of the PCH — *pull-up to VCCIO*

SATA3RCOMPO AB12; SATA3COMPI AB13 — SATA3_COMP R2113 49D9R2F-GP — 1D05V_VTT

SATA3RBIAS AH1 — RBIAS_SATA3 R2114 750R2F-GP

The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to10 k) to Vcc3_3.

SATALED# P3 — SATA_LED# 52

SATA0GP/GPIO21 V14 — SATA_DET#0

SATA1GP/GPIO19 P1 — BBS_BIT0

internal pull-up

RN2103 SRN10KJ-5-GP — SATA_LED# — SATA_DET#0 — 3D3V_S0

HDA_BITCLK N34 — HDA_BCLK — 24MHz

HDA_SYNC L34 — 48 kHz fixed rate — internal pull down

SPKR T10 — internal pull down — 25 HDA_SPKR

HDA_RST# K34

IHDA: HDA_SDIN0 E34 — 25 HDA_SDIN0; HDA_SDIN1 G34; HDA_SDIN2 C34; HDA_SDIN3 A34 — Can be left NO CONNECT if not used (internal pull-down resistors that are always enabled). — internal pull down

HDA_SDO A36 — HDA_SDOUT — internal pull down

HDA_DOCK_EN#/GPIO33 C36 — internal pull UP

HDA_DOCK_RST#/GPIO13 N32 — This can be left unconnected when not in use. — defaults GPIO13

JTAG: JTAG_TCK J3 — PCH_JTAG_TCK_BUF — Do Not Stuff TP2101; JTAG_TMS H7 — PCH_JTAG_TMS — Do Not Stuff TP2102; JTAG_TDI K5 — PCH_JTAG_TDI — Do Not Stuff TP2103; JTAG_TDO H1 — PCH_JTAG_TDO — Do Not Stuff TP2104

SPI: SPI_CLK T3 — PCH_SPI_CLK — R2108 33R2J-2-GP — 23,48 SPI_CLK_R; SPI_CS0# Y14 — PCH_SPI_CS0# — R2109 33R2J-2-GP — 23,48 SPI_CS0#_R; SPI_CS1# T1; SPI_MOSI V4 — PCH_SPI_SI — R2110 33R2J-2-GP — 23,48 SPI_SI_R; SPI_MISO U3 — 23,48 SPI_SO_R

COUGAR-GP-U2-NF

23 ME_UNLOCK — R2107 1KR2J-1-GP Do Not Stuff — TP2105 — PCH_GPIO33

25 CODEC_SDOUT — R2125 33R2J-2-GP — HDA_SDOUT

25,28 HDA_CODEC_RST# — HDA_RST#

25 HDA_CODEC_BITCLK — HDA_BITCLK

RN2102 SRN33J-5-GP-U

DY R2122 Do Not Stuff — BBS_BIT1 — BBS_BIT1 14

DY R2123 Do Not Stuff — BBS_BIT0

1-k to 2.2-k pulldown

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

EVT

PCH_JTAG_TCK_BUF — R2121 4K7R2J-2-GP

N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size: A3 | Document Number: **Z50-HR { Huron River Platform}** | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 17 of 74

SSID = PCH

[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G

Note:
For PCH debug with XDP, need to NO STUFF R2218

EVT

PCH1F 6 OF 10

Cougar Point

GPIO | CPU/MISC | NCTF

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

DY 1 R2205 PCH_GPIO27 Do Not Stuff 【CKLIST P.66】

Deep Sleep	
GPIO27	HIGH (R2019 DY)- ENABLED [DEFAULT] LOW (R2019) - DISABLED

GPIO27 has a weak[20K] internal pull up.
If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

DY 1 R2212 PLL_ODVR_EN Do Not Stuff

The On-Die PLL voltage regulator
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED) If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail.

If not used Can be NC

If not used, 8.2 to 10-kΩ pull-up to VccSuS3_3 (+V3.3A) OR pull-down to GND

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

This signal has a weak internal pull-up.
Note: The internal pull-up is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled low. Leave as "No Connect".

DVT 20101029

Core power :3D3V_S0
Core power :3D3V_S0

EVT

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.
This signal has a weak internal pull-down.
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

This signal has a weak internal pull-down.
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.

PVT

N12M GS2 HYN1GB

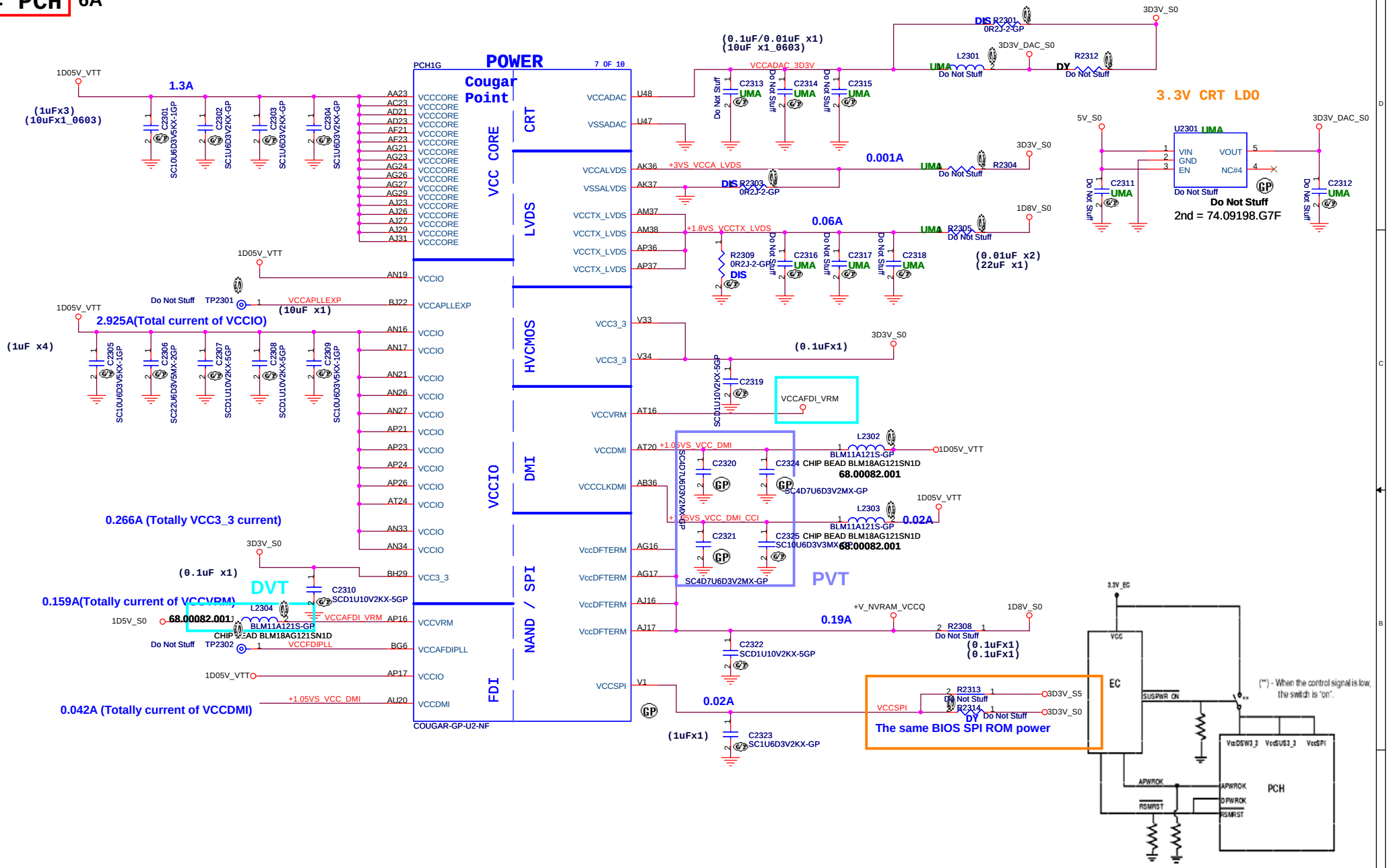
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 18 of 74

SSID = PCH 6A



N12M GS2 HYN1GB

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (POWER1)		
Size: A3	Document Number: Z50-HR { Huron River Platform}	Rev: -1
Date: Wednesday, March 02, 2011	Sheet 19 of 74	

SSID = PCH

POWER

Cougar Point

PCH1J

10 OF 10

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

COUGAR-GP-U2-NF

0.002A

0.097A (Totally current of VCCSUS3_3)

0.001A

1.01A (Total current of VCCASW)

0.16A (Totally current of VCCVRM

0.08A (1uFx1) (220uFx1)

0.08A (1uFx1) (220uFx1)

0.055A

0.095A

0.001A

0.001A

6uA

EVT

DVT

LOW POWER MODE close the PCH

This rail needs to be connected to the +V3.3A power-rail or +V1.5A power-rail.
Note: On CRB, +V3.3A power-rail is used as default (V3.3A_1.5A_HDA_IO).
Also a 0.1-µF capacitor is required close the PCH ball.

N12M GS2 HYN1GB

緯創資通 Wistron Corporation
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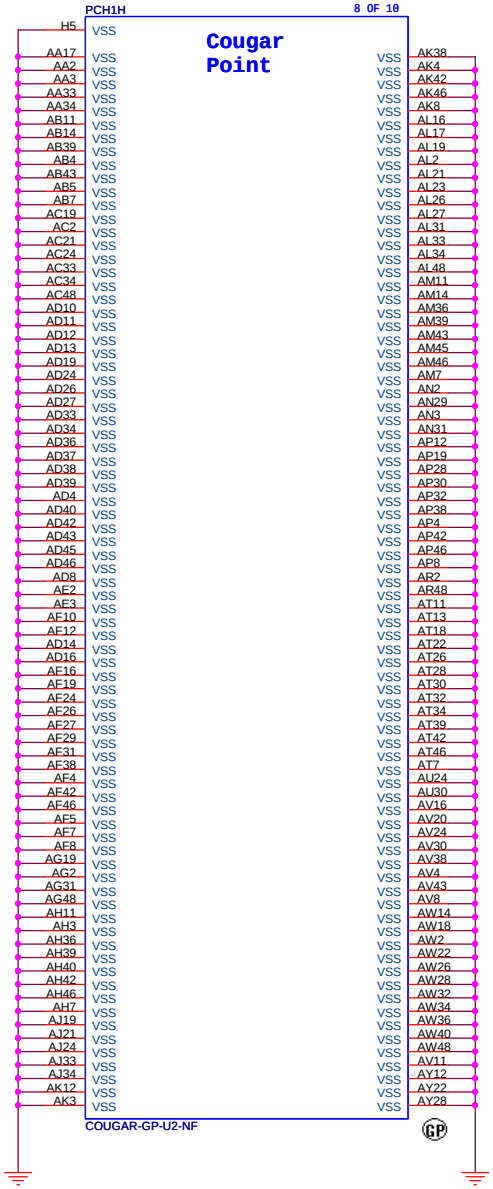
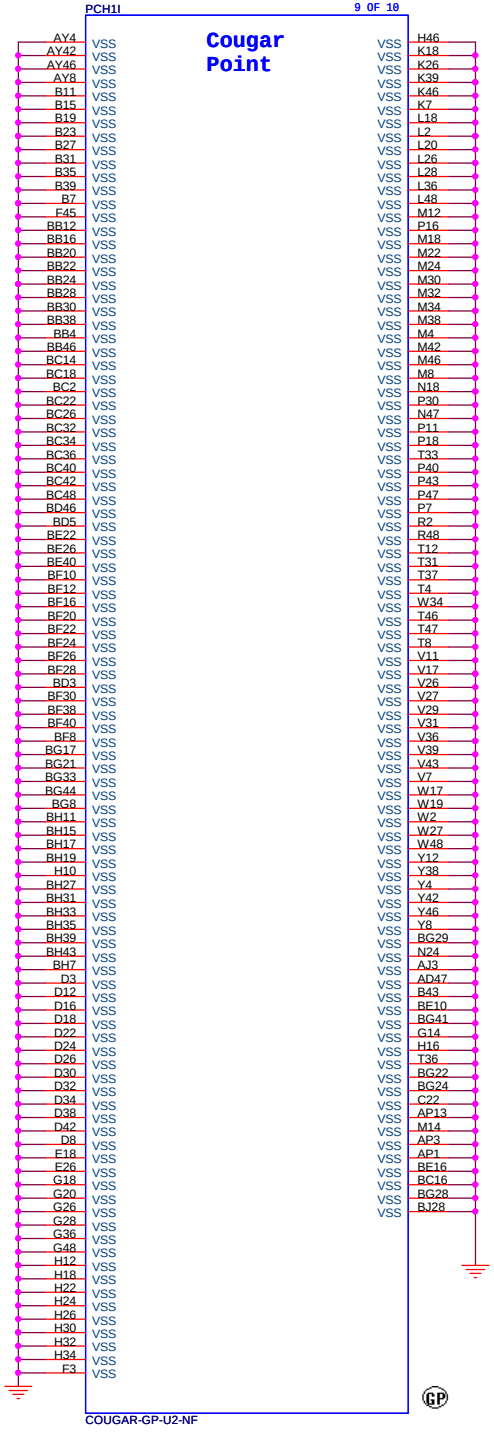
Title: PCH (POWER2)

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 20 of 74

SSID = PCH





N12M GS2 HYN1GB

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

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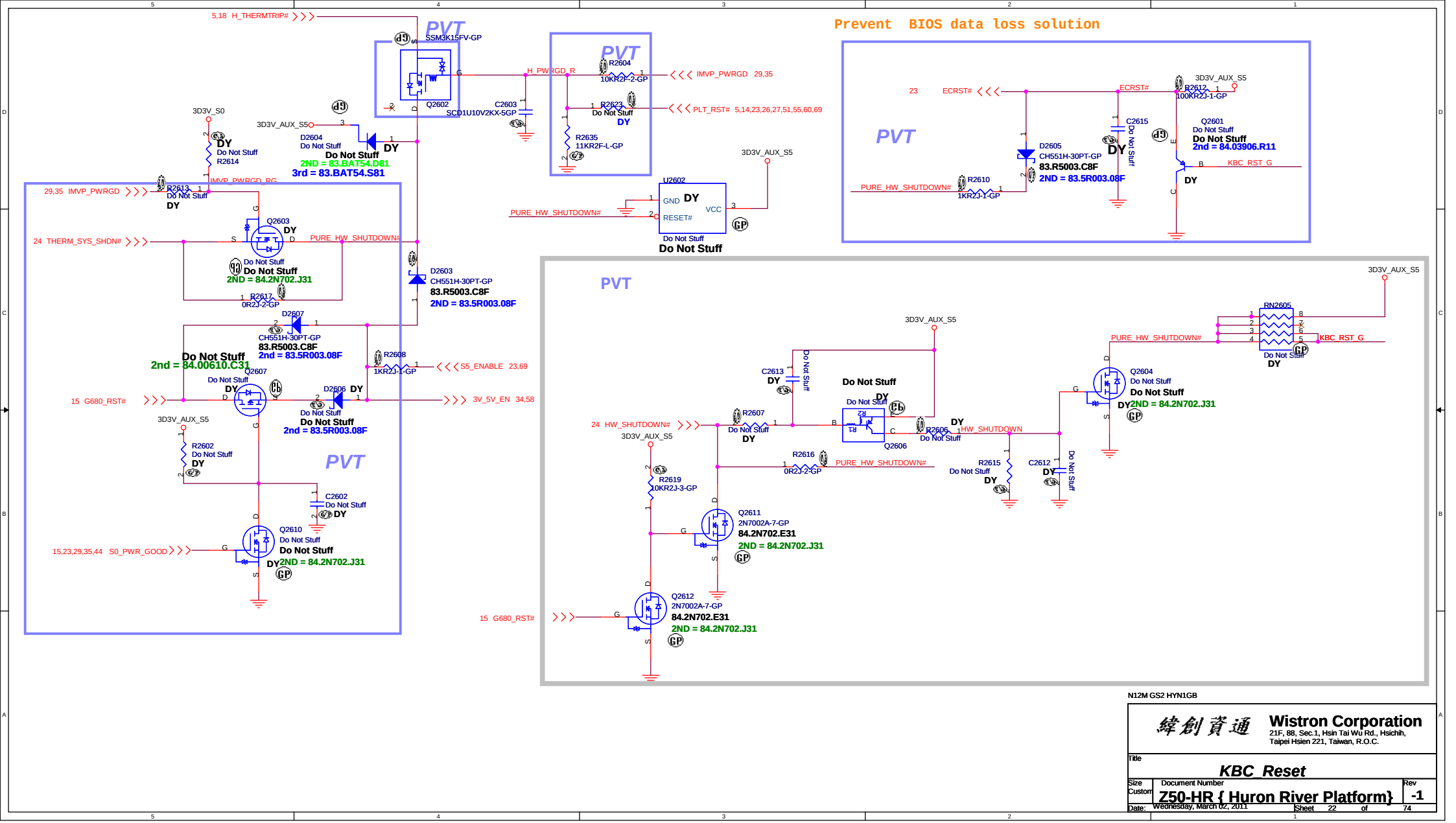
Prevent BIOS data loss solution
PVT
5,18 H_THERMTRIP#
SSM3K15FV-GP
Q2602
H_PWRGD_R
R2604
10KR2F-2-GP
IMVP_PWRGD 29,35
C2603
SCD1U10V2KX-5GP
R2623
Do Not Stuff
DY
PLT_RST# 5,14,23,26,27,51,55,60,69
R2635
11KR2F-L-GP
3D3V_S0
3D3V_AUX_S5
D2604
Do Not Stuff
2ND = 83.BAT54.D81
3rd = 83.BAT54.S81
R2614
IMVP_PWRGD_RG
29,35 IMVP_PWRGD
R2613
Do Not Stuff
U2602
GND
RESET#
VCC
PURE_HW_SHUTDOWN#
Do Not Stuff
23 ECRST#
ECRST#
R2612
100KR2J-1-GP
C2615
Do Not Stuff
Q2601
Do Not Stuff
2nd = 84.03906.R11
KBC_RST_G
D2605
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.5R003.08F
R2610
1KR2J-1-GP
Q2603
24 THERM_SYS_SHDN#
PURE_HW_SHUTDOWN#
2ND = 84.2N702.J31
R2617
0R2J-2-GP
D2603
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.5R003.08F
D2607
CH551H-30PT-GP
83.R5003.C8F
2nd = 83.5R003.08F
R2608
1KR2J-1-GP
S5_ENABLE 23,69
2nd = 84.00610.C31
Q2607
15 G680_RST#
D2606
3V_5V_EN 34,58
R2602
Do Not Stuff
C2602
Do Not Stuff
Q2610
15,23,29,35,44 S0_PWR_GOOD
2ND = 84.2N702.J31
3D3V_AUX_S5
C2613
Do Not Stuff
24 HW_SHUTDOWN#
R2607
R2606
HW_SHUTDOWN
Q2606
R2616
PURE_HW_SHUTDOWN#
R2619
10KR2J-3-GP
Q2611
2N7002A-7-GP
84.2N702.E31
2ND = 84.2N702.J31
Q2612
2N7002A-7-GP
84.2N702.E31
2ND = 84.2N702.J31
15 G680_RST#
R2615
C2612
RN2605
PURE_HW_SHUTDOWN#
KBC_RST_G
Q2604
Do Not Stuff
2ND = 84.2N702.J31
N12M GS2 HYN1GB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
KBC_Reset
Size
Custom
Document Number
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Date: Wednesday, March 02, 2011
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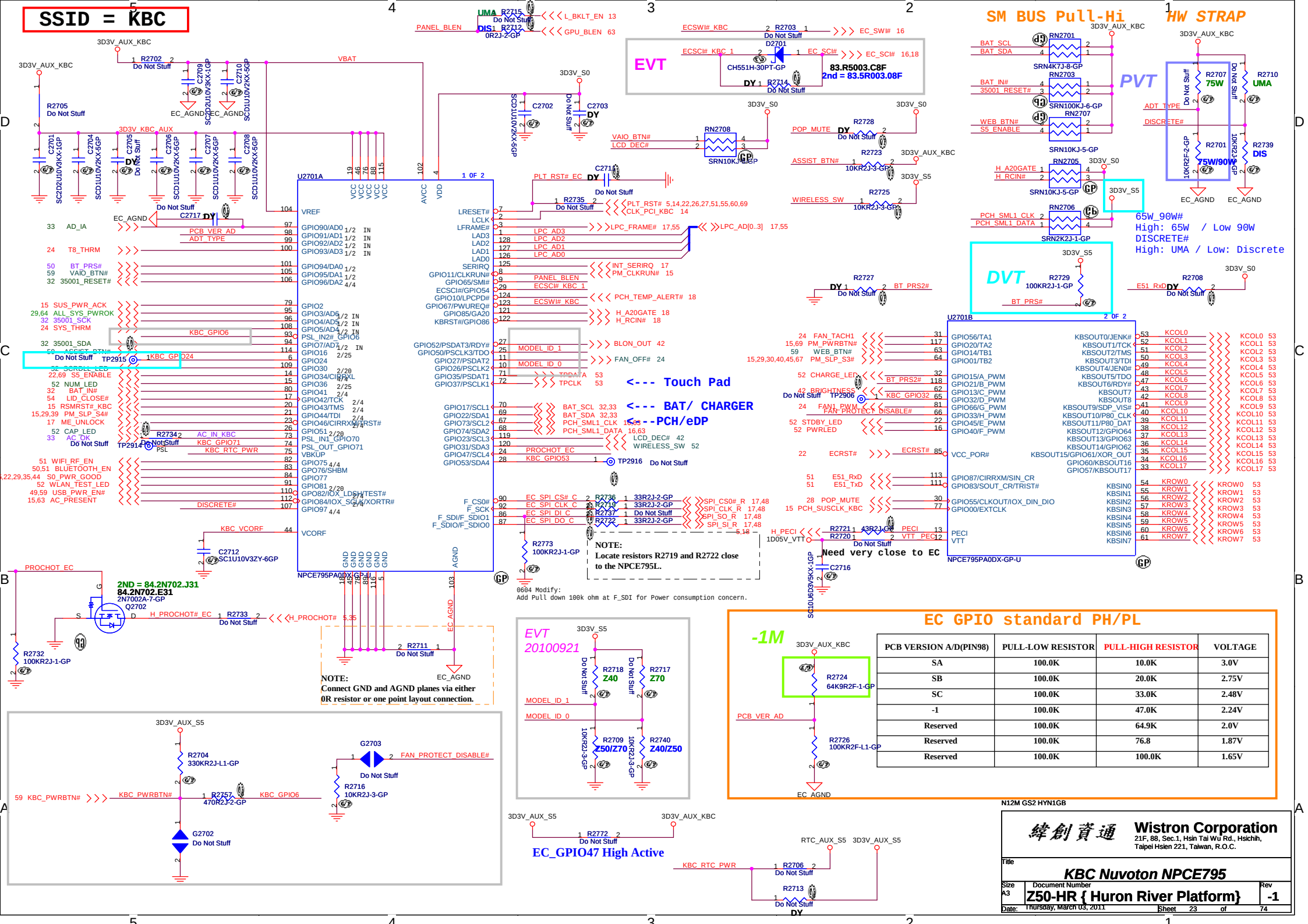
SSID = KBC



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

N12M GS2 HYN1GB

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Title: KBC Nuvoton NPCE795

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Thursday, March 03, 2011 | Sheet 23 of 74

SSID = Thermal

Thermal sensor P2800

Layout 15 mil

ps. FAN1 POWER TRACE WIDTH ~15 MIL

PVT

DVT

EVT
Q9306 NO DY

Max current is 235mA;
Stopped is ~10mA

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

2.System Sensor, Put on palm rest

1.H/W T8 Shutdown

EVT
U2801

Close to CPU

Close to MS Card Connector

Close to GPU

Close to Battery Connector

Close to HDD Connector

PWM FAN
PIN1 PWM
PIN2 GND
PIN3 FG
PIN4 VCC

ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

N12M GS2 HYN1GB

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Title: Thermal P2800
Size: A3
Document Number: Z50-HR { Huron River Platform}
Rev: -1
Date: Wednesday, March 02, 2011
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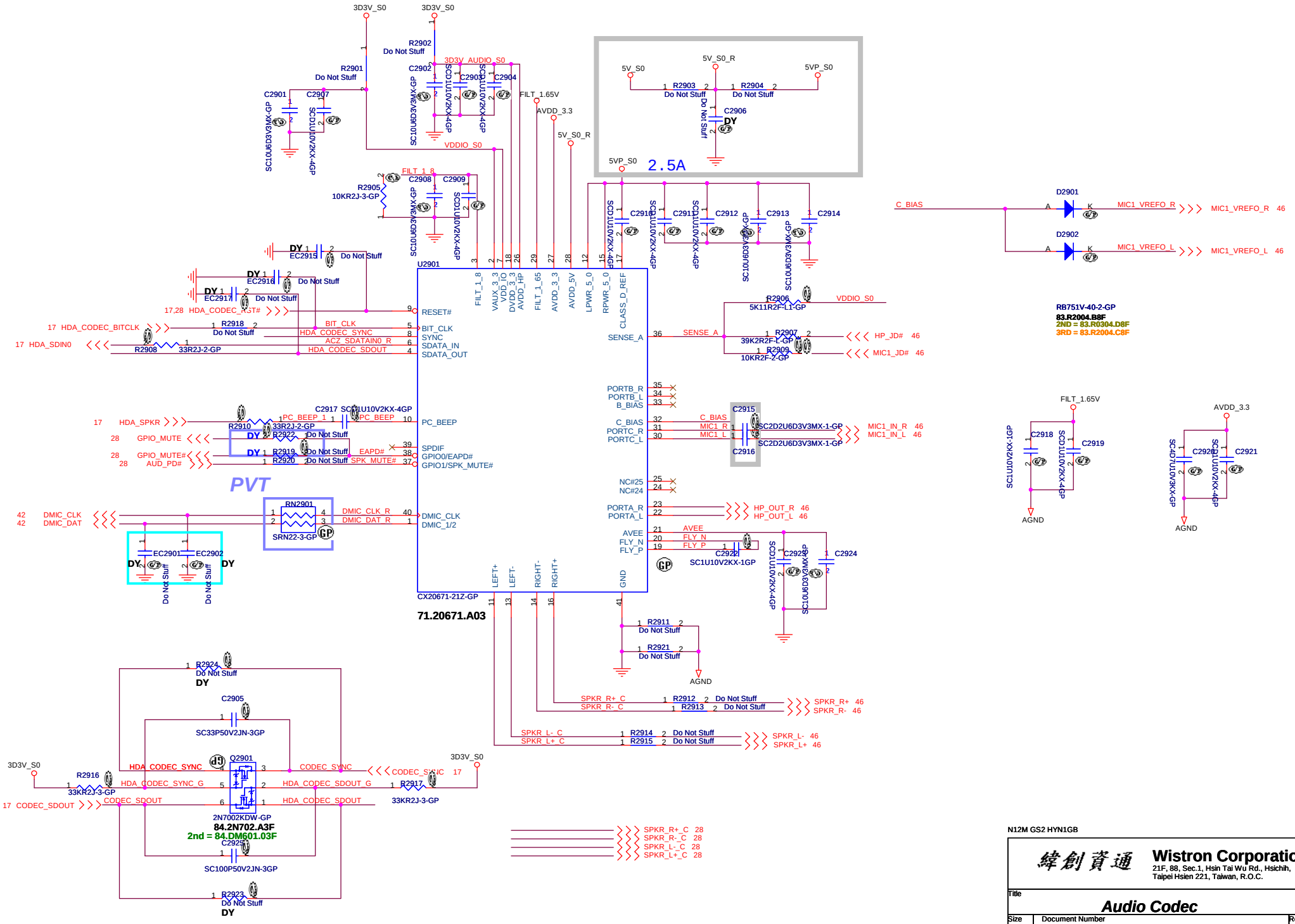
3D3V_S0
3D3V_S0
R2902
Do Not Stuff
3D3V_AUDIO_S0
R2901
Do Not Stuff
C2901
C2907
C2902
C2903
C2904
SC10U6D3V3MX-GP
SC1U10V2KX-4GP
SC10U6D3V3KX-GP
FILT_1.65V
AVDD_3.3
5V_S0_R
VDDIO_S0
5V_S0
5V_S0_R
5VP_S0
R2903
R2904
C2906
DY
2.5A
5VP_S0
FILT_1_8
C2908
C2909
R2905
10KR2J-3-GP
C2910
C2911
C2912
C2913
C2914
SC1U10V2KX-4GP
SC10U6D3V3MX-GP
DY
EC2915
Do Not Stuff
DY
EC2916
Do Not Stuff
DY
EC2917
Do Not Stuff
17,28 HDA_CODEC_RST#
U2901
FILT_1_8
VAUX_3_3
VDD_IO
DVDD_3_3
AVDD_HP
FILT_1_65
AVDD_3_3
AVDD_5V
LPWR_5_0
RPWR_5_0
CLASS_D_REF
RESET#
17 HDA_CODEC_BITCLK
R2918
Do Not Stuff
BIT_CLK
HDA_CODEC_SYNC
ACZ_SDATAIN0_R
HDA_CODEC_SDOUT
17 HDA_SDIN0
R2908
33R2J-2-GP
BIT_CLK
SYNC
SDATA_IN
SDATA_OUT
SENSE_A
36
SENSE_A
R2906
5K11R2F-L1-GP
R2907
39K2R2F-L-GP
R2909
10KR2F-2-GP
HP_JD# 46
MIC1_JD# 46
RB751V-40-2-GP
83.R2004.B8F
2ND = 83.R0304.D8F
3RD = 83.R2004.C8F
C_BIAS
D2901
D2902
MIC1_VREFO_R
MIC1_VREFO_L
MIC1_VREFO_R 46
MIC1_VREFO_L 46
C2917 SC1U10V2KX-4GP
17 HDA_SPKR
R2910
33R2J-2-GP
PC_BEEP_1
PC_BEEP
PC_BEEP
28 GPIO_MUTE
DY
R2922
Do Not Stuff
28 GPIO_MUTE#
28 AUD_PD#
DY
R2919
Do Not Stuff
R2920
Do Not Stuff
EAPD#
SPK_MUTE#
SPDIF
GPIO0/EAPD#
GPIO1/SPK_MUTE#
PVT
PORTB_R
PORTB_L
B_BIAS
C_BIAS
PORTC_R
PORTC_L
C2915
C2916
SC2D2U6D3V3MX-1-GP
MIC1_R
MIC1_L
MIC1_IN_R 46
MIC1_IN_L 46
FILT_1.65V
AVDD_3.3
C2918
C2919
C2920
C2921
SC1U10V2KX-4GP
SC4D7U10V3KX-GP
AGND
NC#25
NC#24
PORTA_R
PORTA_L
HP_OUT_R 46
HP_OUT_L 46
RN2901
42 DMIC_CLK
42 DMIC_DAT
DMIC_CLK_R
DMIC_DAT_R
SRN22-3-GP
DMIC_CLK
DMIC_1/2
AVEE
FLY_N
FLY_P
C2922
SC1U10V2KX-1GP
C2923
C2924
SC1U10V2KX-4GP
SC10U6D3V3MX-GP
EC2901
EC2902
DY
Do Not Stuff
Do Not Stuff
DY
LEFT+
LEFT-
RIGHT-
RIGHT+
GND
CX20671-21Z-GP
71.20671.A03
R2911
Do Not Stuff
R2921
Do Not Stuff
AGND
R2924
Do Not Stuff
DY
C2905
SC33P50V2JN-3GP
SPKR_R+_C
SPKR_R-_C
R2912
R2913
Do Not Stuff
SPKR_R+ 46
SPKR_R- 46
SPKR_L-_C
SPKR_L+_C
R2914
R2915
Do Not Stuff
SPKR_L- 46
SPKR_L+ 46
3D3V_S0
R2916
33KR2J-3-GP
HDA_CODEC_SYNC
HDA_CODEC_SYNC_G
CODEC_SDOUT
Q2901
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
HDA_CODEC_SYNC
HDA_CODEC_SDOUT_G
HDA_CODEC_SDOUT
CODEC_SYNC
CODEC_SDOUT
17
R2917
33KR2J-3-GP
3D3V_S0
C2925
SC100P50V2JN-3GP
R2923
Do Not Stuff
DY
SPKR_R+_C 28
SPKR_R-_C 28
SPKR_L-_C 28
SPKR_L+_C 28
N12M GS2 HYN1GB
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio Codec
Size
A3
Document Number
Z50-HR { Huron River Platform}
Rev
-1
Date: Wednesday, March 02, 2011
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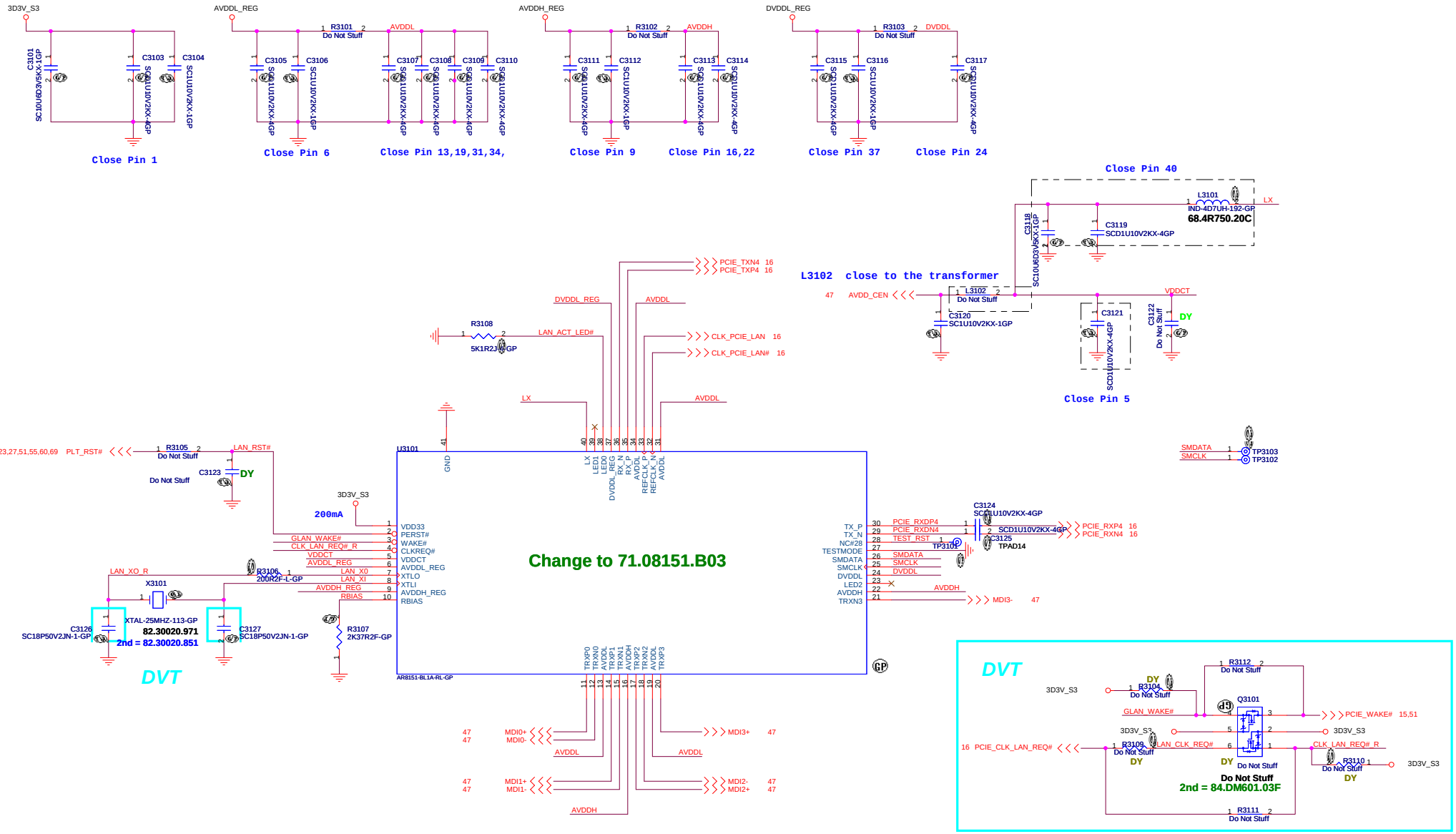


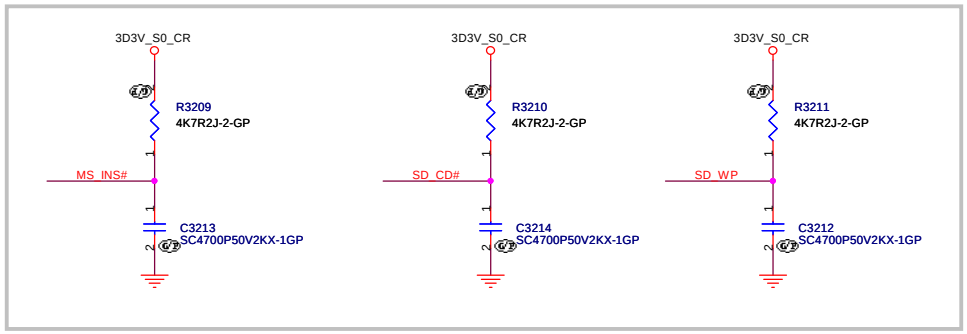
N12M GS2 HYN1GB

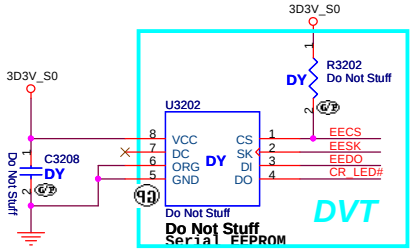
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

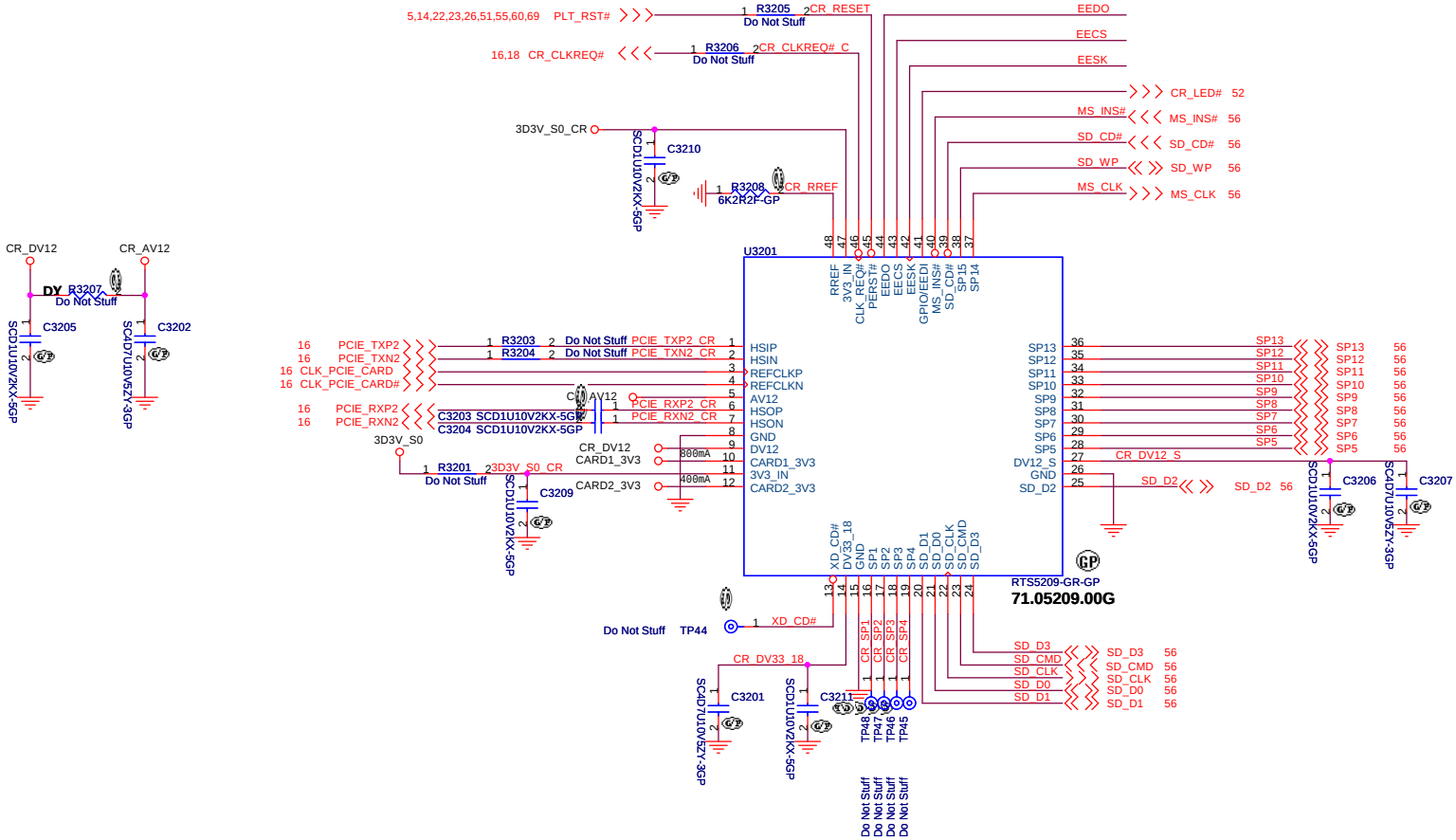
Title: Atheros 8151

Size: Custom | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 26 of 74







N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5209 (CARD READER)***

Size	Document Number	Rev
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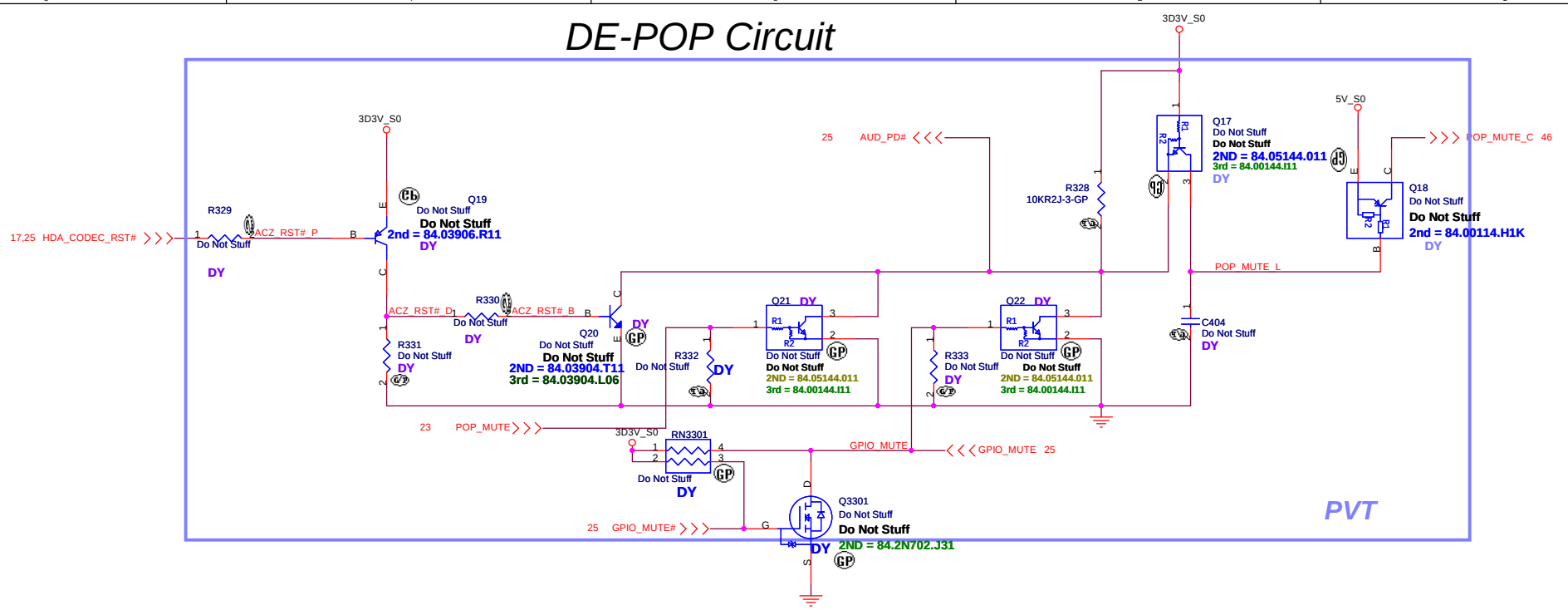
DE-POP Circuit



EVT
NO PGND

25 SPKR_L+_C
DY R334
Do Not Stuff
SPKR_L+_C_R
C405
DY
C406
DY
R335
Do Not Stuff
DY
Q23
Do Not Stuff
Do Not Stuff
2ND = 84.02222.X11
Q24
Do Not Stuff
Do Not Stuff
2ND = 84.02222.X11
25 SPKR_L-_C
DY R337
Do Not Stuff
SPKR_L-_C_R
C408
DY

25 SPKR_R+_C
DY R340
Do Not Stuff
SPKR_R+_C_R
C410
DY
C411
DY
R342
DY
Do Not Stuff
Q26
Do Not Stuff
Do Not Stuff
2ND = 84.02222.X11
Q27
Do Not Stuff
Do Not Stuff
2ND = 84.02222.X11
25 SPKR_R-_C
DY R343
Do Not Stuff
SPKR_R-_C_R
C412
DY

5V_S0_R
5V_S0_R
C407
DY
Do Not Stuff
U29
DY
Do Not Stuff
5V_S0_R_1
Q25
Do Not Stuff
Do Not Stuff
2nd = 84.03906.R11
DY
R336
Do Not Stuff
DY
R338
DY
Do Not Stuff
C409
DY
R339
DY
Do Not Stuff
5VP_S0_1
5VP_S0
5VP_S0
R341
DY
Do Not Stuff
5VP_S0_Q1

N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Audio DE-POP Circuit*

Size	Document Number	Rev
	Z50-HR { Huron River Platform}	-1

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Power Sequence

EVT
DEL U3608

ALL_SYS_PWROK 23,64
PWR_VCCSA_PWRGD 15,35,41
R3604 Do Not Stuff

22,35 IMVP_PWRGD
R3615 Do Not Stuff
SYS_PWROK
DY
15,22,23,35,44 S0_PWR_GOOD
R3602 Do Not Stuff
S0_PWR_GOOD
D3604
CH551H-30PT-GP
SYS_PWROK 15
15,23,30,40,45,67 PM_SLP_S3#
R3605 Do Not Stuff
83.R5003.C8F
2nd = 83.5R003.08F
C3615
DY
R3614
CRB : 1K
Do Not Stuff

Run Power

PVT
84.S0610.B31
2nd = 84.00610.C31
DCBATOUT
Q3604
NDS0610-NL-GP
R3619 0R2J-2-GP
R3622 10KR2J-3-GP
RUN_ENABLE
R3618 330KR2J-L1-GP
Z_12V_G3
R3617 100KR2J-1-GP
Z_12V_G3_R
R3620 10KR2J-3-GP
Z_12V_D4
C3606 SCD22U25V3KX-GP
C3607 Do Not Stuff
DY
D3602
MMPZ5239BPT-GP
2ND = 83.9R103.F3F
83.9R103.D3F
5V_S0
5V_S5
U3604
R3623 0R2J-2-GP
AO4468-GP
84.04468.037
2ND = 84.08882.037
PVT
3D3V_S0
3D3V_S5
U3607
R3624 0R2J-2-GP
AO4468-GP
84.04468.037
2ND = 84.08882.037
1D5V_S0
1D5V_S3
U3605
R3627 0R2J-2-GP
AO4468-GP
84.04468.037
2ND = 84.08882.037
SCD01U50V2KX-1GP
C3614
1D5V_DDR_S0
R3631 Do Not Stuff
R3625 Do Not Stuff
R3612 10KR2J-3-GP
5V_S5
15,23,30,40,45,67 PM_SLP_S3#
PS_S3CNTRL
Q3605
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
PM_SLP_S3# 15,23,30,40,45,67
Q3603
2N7002A-7-GP
84.2N702.E31
2ND = 84.2N702.J31
20101112
DVT
2nd = 84.DM601.03F
PS_S3CNTRL PS_S3CNTRL 30,39,67

1D5V_S0
MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

S3 Power

DCBATOUT
R3603 330KR2J-L1-GP
3D3V_S3
3D3V_S5
U3601
S3_ON
R3628 0R2J-2-GP
AO4468-GP
84.04468.037
2ND = 84.08882.037
PVT
D3603
MMPZ5239BPT-GP
2ND = 83.9R103.F3F
83.9R103.D3F
0R2J-2-GP
R3626
5V_S5
R3607 100KR2J-1-GP
15,23,39 PM_SLP_S4#
R3606 Do Not Stuff
PM_SLP_S4# 1
S3_ON1
PM_SLP_S4
Q3601
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
C3601 SCD1U16V2KX-3GP
DVT
3D3V_S3
DY
R3608 Do Not Stuff
3D3V_S3_DIS_D
DY
Q3606
Do Not Stuff
Do Not Stuff
2ND = 84.2N702.J31
PM_SLP_S4

N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

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Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

All VREF traces should be 20 mils wide and 20 mils spacing to other signals/planes.

M1 :Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref to channel A SO-DIMM0 and B SO-DIMM1 connectors. This is the default stuffing option.

【DG 0.9 P.87】

DDR_VREF_S3 — R3708 0R0603-PAD — +V_SM_VREF

DY R3707 Do Not Stuff

Q3708 2N7002A-7-GP 84.2N702.E31 2ND = 84.2N702.J31

R3705 100KR2J-1-GP

+V_SM_VREF_CNT 9

PM_SLP_S3# 15,23,29,40,45,67

EVT

3D3V_S5

R3727 Do Not Stuff DY

PS_S3CNTRL → PS_S3CNTRL 29,39,67

Q3713 2ND = 84.2N702.J31 Do Not Stuff Do Not Stuff DY

15,23,29,40,45,67 PM_SLP_S3#

DVT

5V_S5 R3722 10KR2J-3-GP

3D3V_S0 R3726 10KR2J-3-GP

1.5V_RUN_CPU_EN#

1D5V_DDR_S0 R3723 3K3R2J-3-GP

EVT

38,41,68 1.05VTT_PWRGD — DY R3711 Do Not Stuff

39 0D75V_EN

15,23,29,40,45,67 PM_SLP_S3# — R3724 Do Not Stuff DY

C3707 SCD1U10V2KX-5GP

Q3712 2N7002A-7-GP 84.2N702.E31 2ND = 84.2N702.J31

Q3707 CH3904GP-GP-U 84.03904.X11 2ND = 84.03904.T11 3rd = 84.03904.L06

R3725 4K7R2J-2-GP

S3 Power Reduction Circuit

Close to DIMM

S3 Power Reduction Circuit RamPower discharge

0D75V_S0 — R3703 22R2J-2-GP — 0D75V_S0_DIS — Q3701 2N7002A-7-GP 84.2N702.E31 2ND = 84.2N702.J31 — PS_S3CNTRL

1D5V_DDR_S0 — R3704 220R2J-L2-GP — 1D5V_DDR_S0_DIS — Q3702 2N7002A-7-GP 84.2N702.E31 2ND = 84.2N702.J31 — PS_S3CNTRL

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

【DG 0.9 P.107】

1D5V_S3 — R3706 1KR2J-1-GP

DY R3709 Do Not Stuff

5 SM_DRAMRST#

EVT

16 DRAMRST_CNTRL_PCH

Q3703 2N7002A-7-GP 84.2N702.E31 2ND = 84.2N702.J31

C3703 SCD047U16V2KX-1-GP

SM_DRAMRST# D — R3718 1KR2J-1-GP — DDR3_DRAMRST# 11,12

C3702 SC100P50V2JN-3GP

S3 Power Reduction Circuit
SM_DRAMRST#

Signal Routing Guideline:
1. Maximal trace length from R_iso to any DRAM (on the SO DIMM) is 6".
2. FET's Ron must be lower than 6 Ohms and pad capacitance lower than 30pF.

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

3D3V_S0 3D3V_S5 1D5V_S0

EVT

DY R3715 Do Not Stuff — R3713 200R2F-L-GP

R3702 200R2F-L-GP

U3702 74AHC1G09GW-GP 73.01G09.0AB 2ND = 73.01G09.AAH

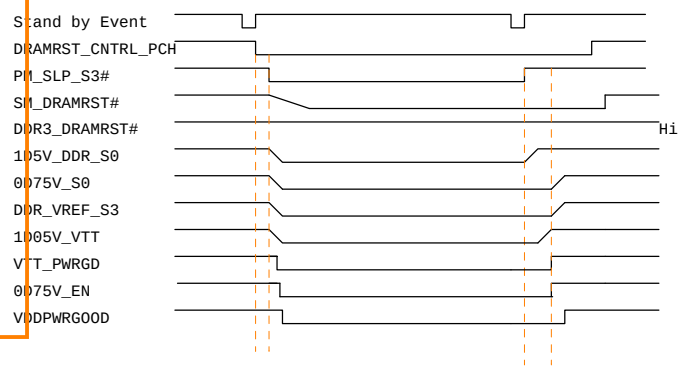
5,15 PM_DRAM_PWRGD

38,39,40 RUNPWROK — R3701 Do Not Stuff — 0D75V_EN_1

C3701 DY Do Not Stuff

VDDPWRGOOD_R — R3710 130R2F-1-GP — VDDPWRGOOD 5

R3712 Do Not Stuff DY



N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: S3 reduction

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

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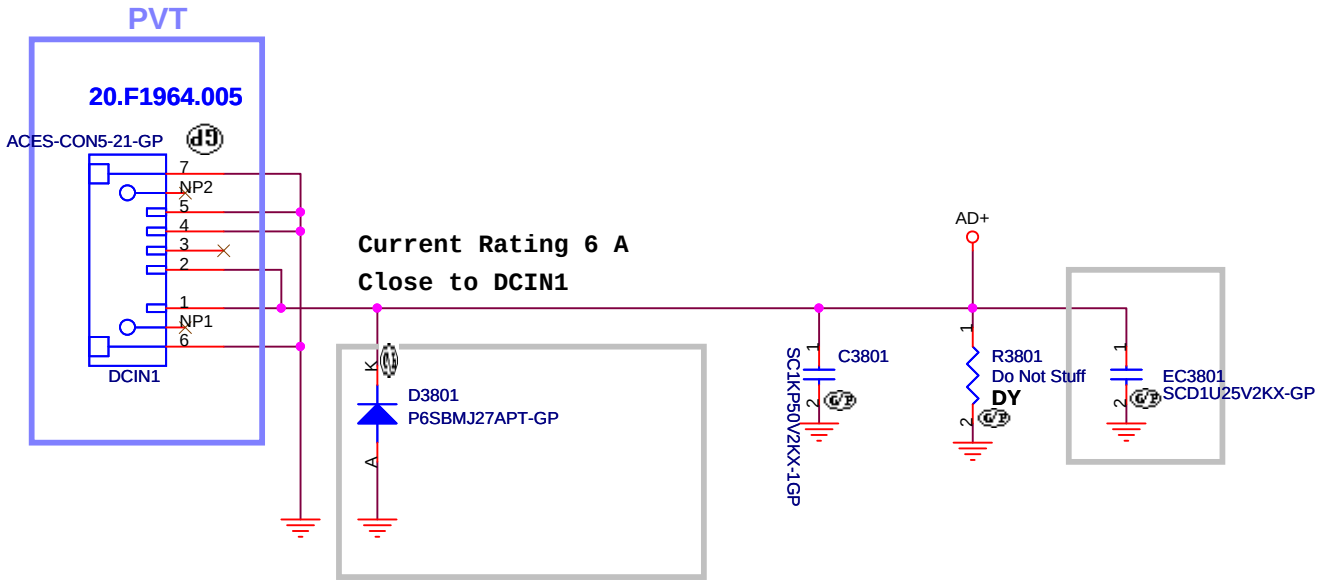
Adaptor in to generate DCBATOUT



N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DCIN JACK***

Size	Document Number	Rev
A4	Z50-HR { Huron River Platform}	-1

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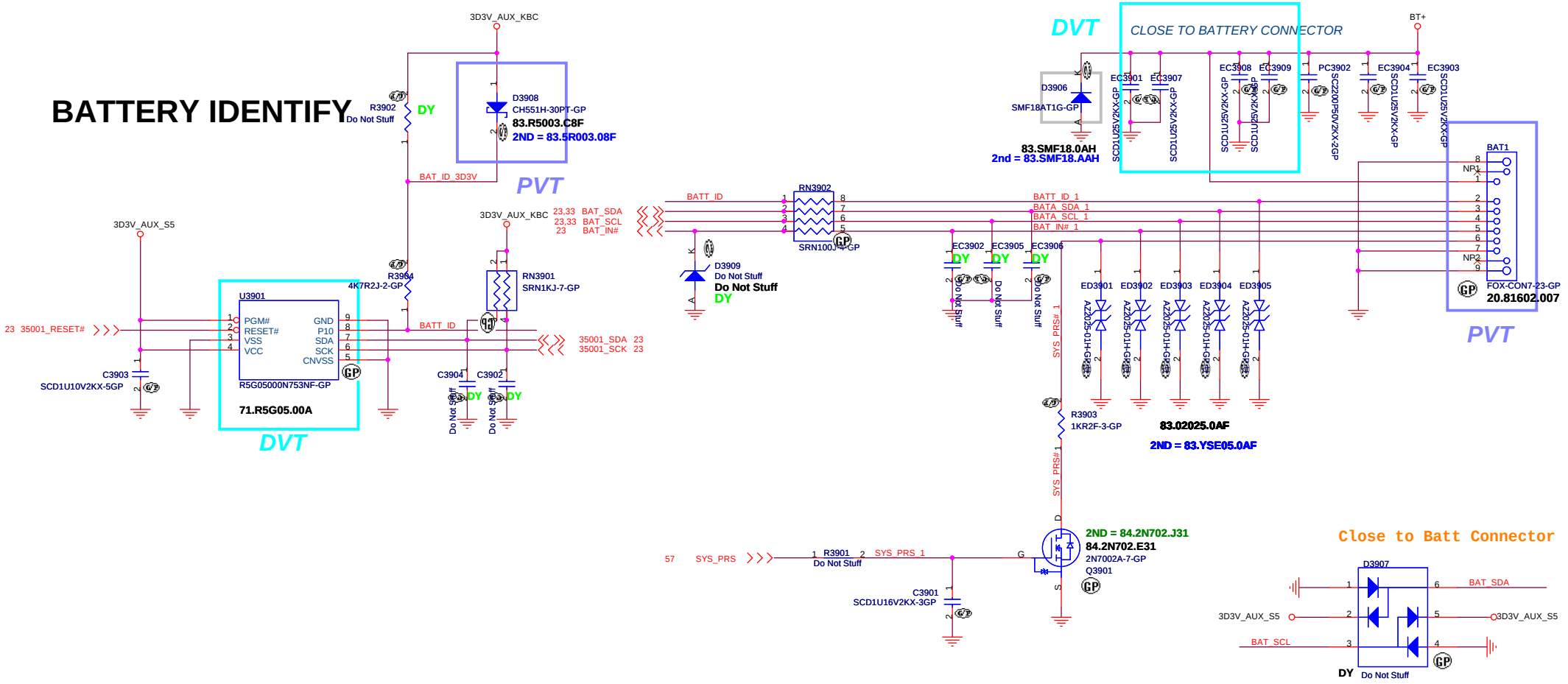
BATTERY IDENTIFY



N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

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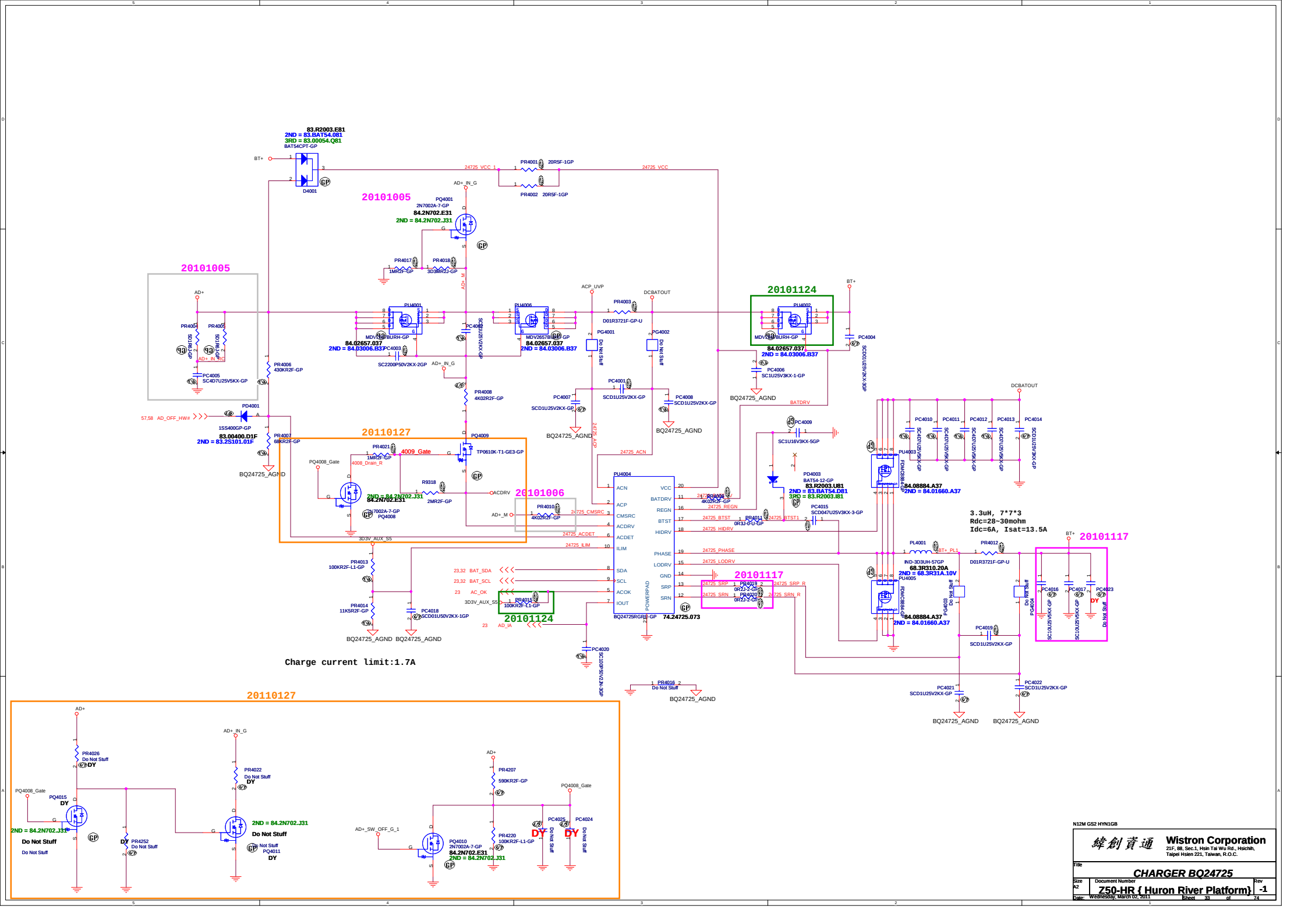
83.R2003.E81
2ND = 83.BAT54.081
3RD = 83.00054.Q81
BAT54CPT-GP
D4001
20101005
PQ4001
2N7002A-7-GP
84.2N702.E31
2ND = 84.2N702.J31
PR4001 20R5F-1GP
PR4002 20R5F-1GP
PR4017 1MR2F-GP
PR4018 3D3MR2J-GP
PR4006 430KR2F-GP
PR4008 4K02R2F-GP
PD4001
1SS400GP-GP
83.00400.D1F
2ND = 83.2S101.01F
PR4007 68KR2F-GP
BQ24725_AGND
20110127
PR4021 1MR2F-GP
4009_Gate
TP0610K-T1-GE3-GP
PQ4009
PQ4008_Gate
4008_Drain_R
PQ4008
R9318 2MR2F-GP
ACDRV
20101006
PR4010 4K02R2F-GP
PU4004
ACN
ACP
CMSRC
ACDRV
ACDET
ILIM
SDA
SCL
ACOK
IOUT
VCC
BATDRV
REGN
BTST
HIDRV
PHASE
LODRV
GND
SRP
SRN
POWERPAD
BQ24725RGRR-GP
74.24725.073
PR4013 100KR2F-L1-GP
PR4014 11K5R2F-GP
PC4018 SCD01U50V2KX-1GP
PR4016 100KR2F-L1-GP
20101124
PC4020 SC0D0F50V2KX-3GP
PR4016 Do Not Stuff
PU4001
PU4006
MDV2657B/BURH-GP
84.02657.037
2ND = 84.03006.B37
PC4002 SC1U25V3KX-GP
PC4003 SC2200P50V2KX-2GP
PR4003 D01R3721F-GP-U
PG4001 Do Not Stuff
PG4002 Do Not Stuff
PC4001 SCD1U25V2KX-GP
PC4007 SCD1U25V2KX-GP
PC4008 SCD1U25V2KX-GP
20101124
PU4002
PC4004 SC0D0U50V2KX-3GP
PC4006 SC1U25V3KX-1GP
BQ24725_AGND
BATDRV
PC4009 SC1U16V3KX-5GP
PD4003 BAT54-12-GP
83.R2003.U81
2ND = 83.BAT54.D81
3RD = 83.R2003.I81
PC4015 SCD047U25V3KX-3-GP
PR4011 0R3J-0-U-GP
PU4003
FDMC8884-GP
84.08884.A37
2ND = 84.01660.A37
PC4010 SC4D7U25V5KX-GP
PC4011 SC4D7U25V5KX-GP
PC4012 SC4D7U25V5KX-GP
PC4013 SC4D7U25V5KX-GP
PC4014 SC0D1U25V3KX-GP
DCBATOUT
3.3uH, 7*7*3
Rdc=28~30mohm
Idc=6A, Isat=13.5A
20101117
PL4001
IND-3D3UH-57GP
68.3R310.20A
2ND = 68.3R31A.10V
PR4012 D01R3721F-GP-U
PC4016 SC1U25V5KX-GP
PC4017 SC1U25V5KX-GP
PC4023 DY
PC4019 SCD1U25V2KX-GP
PC4021 SCD1U25V2KX-GP
PC4022 SCD1U25V2KX-GP
Charge current limit:1.7A
20110127
PR4026 Do Not Stuff DY
PQ4015 DY
PR4252 Do Not Stuff
PR4022 Do Not Stuff DY
2ND = 84.2N702.J31
Do Not Stuff
Not Stuff
PQ4011 DY
PR4207 590KR2F-GP
PR4220 100KR2F-L1-GP
PQ4010 2N7002A-7-GP
84.2N702.E31
2ND = 84.2N702.J31
PC4025 DY Do Not Stuff
PC4024 DY Do Not Stuff
N12M GS2 HYN1GB
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER BQ24725
Size A2
Document Number
Z50-HR { Huron River Platform}
Rev -1
Date: Wednesday, March 02, 2011
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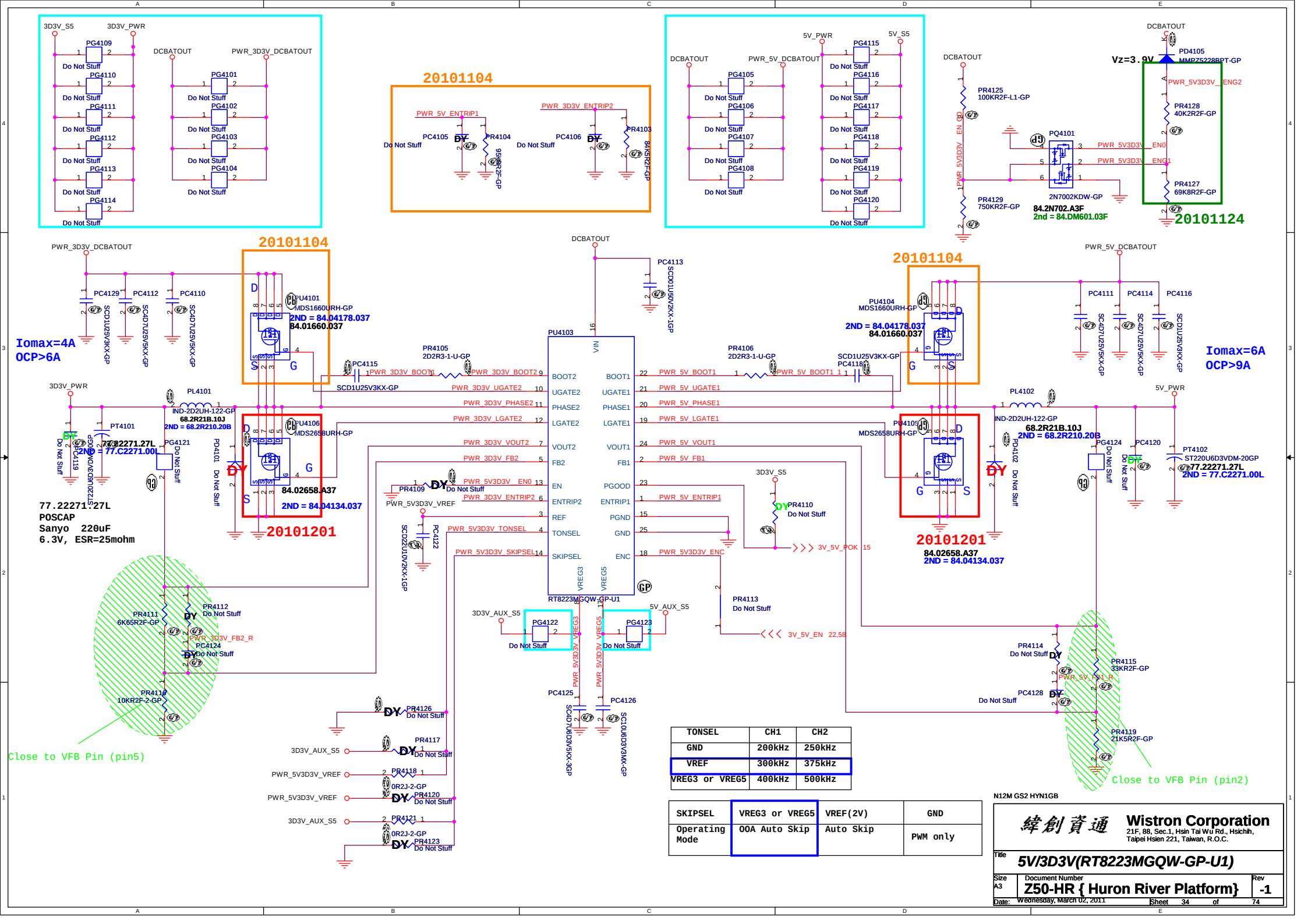


TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

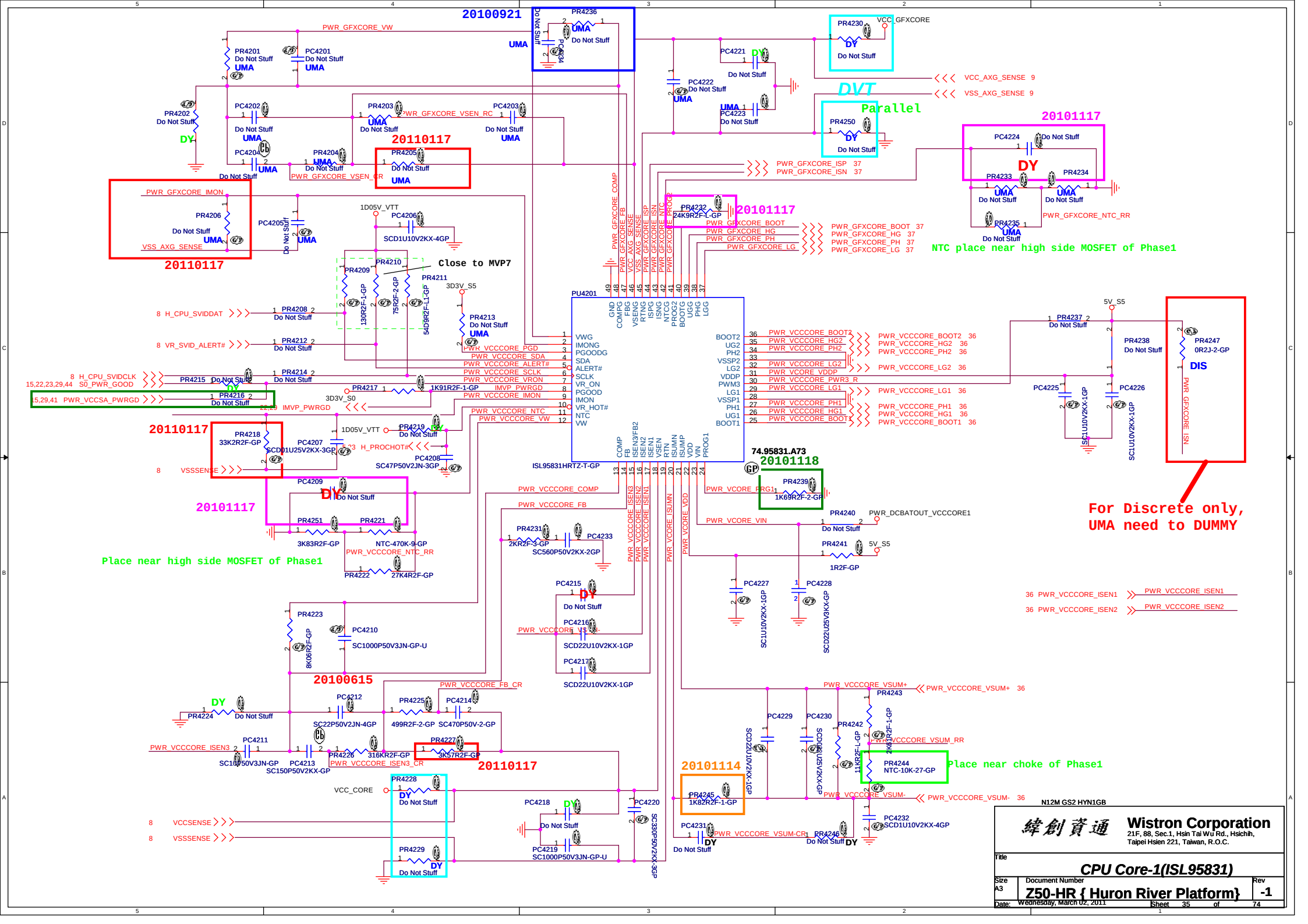
N12M GS2 HYN1GB

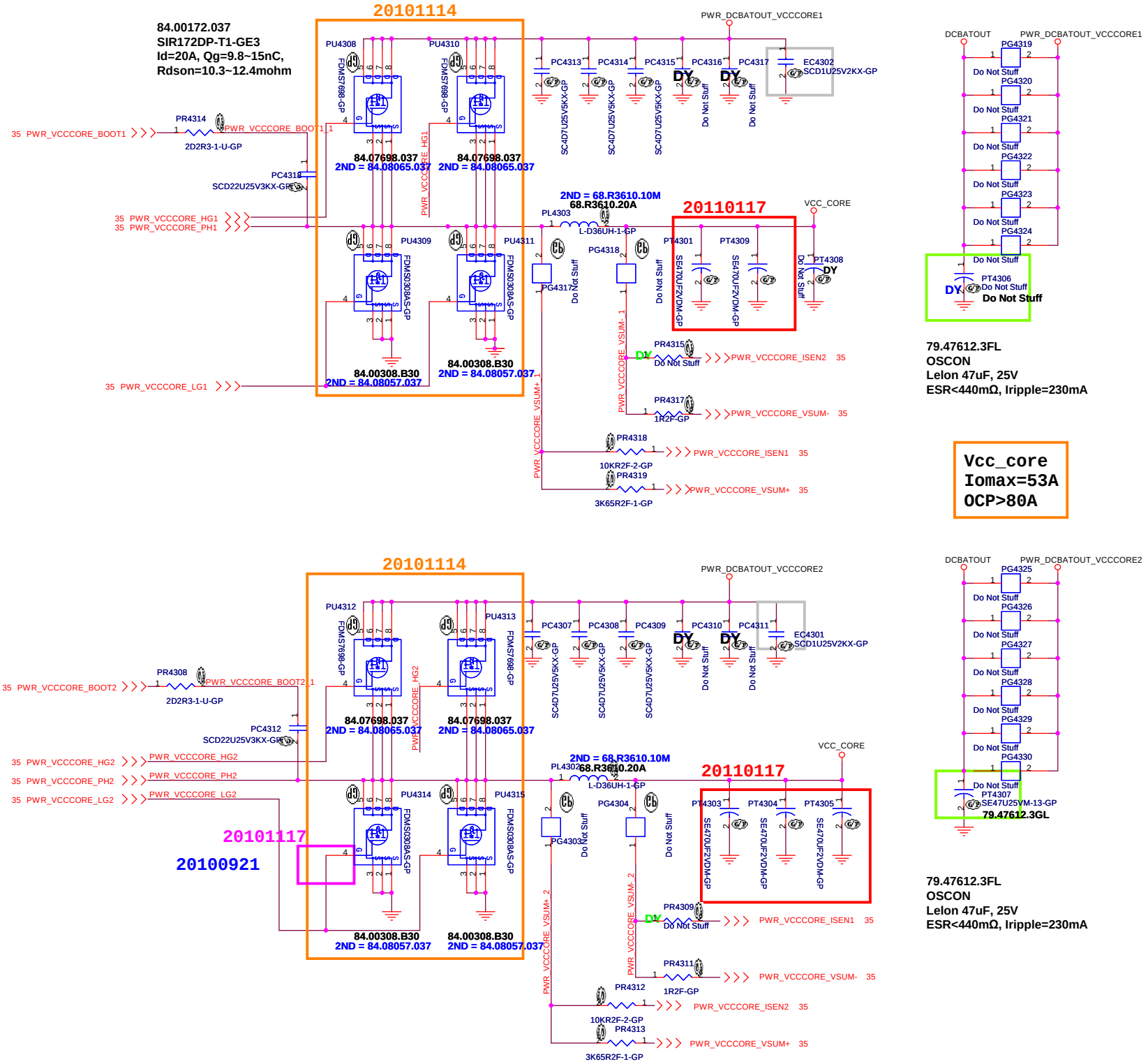
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

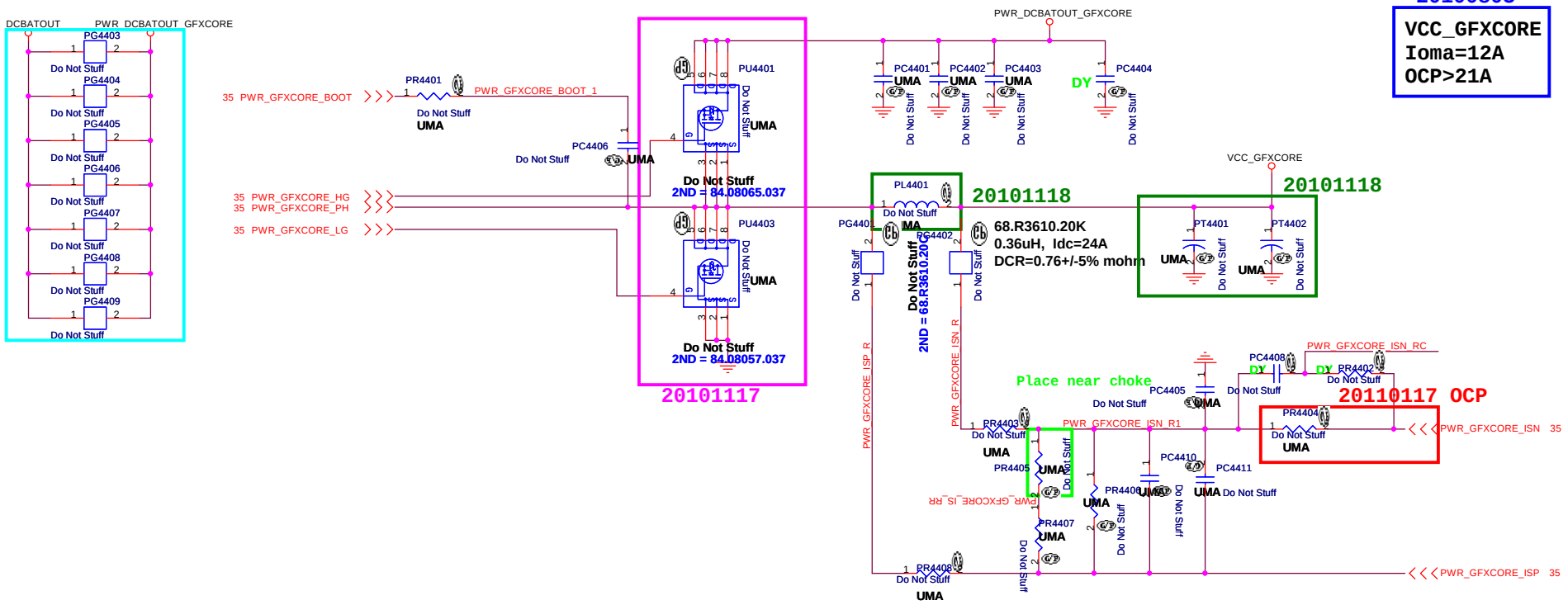
Title: 5V/3D3V(RT8223MGQW-GP-U1)

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 34 of 74


20100921
PU4201
ISL95831HRTZ-T-GP
74.95831.A73
20101118
20101117
20110117
20100615
20101114
DVT
Parallel
DY
UMA
Do Not Stuff
Close to MVP7
NTC place near high side MOSFET of Phase1
Place near high side MOSFET of Phase1
Place near choke of Phase1
For Discrete only,
UMA need to DUMMY
PWR_GFXCORE_VW
PWR_GFXCORE_IMON
VSS_AXG_SENSE
PWR_GFXCORE_VSEN_RC
PWR_GFXCORE_VSEN_CR
PWR_GFXCORE_ISP
PWR_GFXCORE_ISN
PWR_GFXCORE_NTC_RR
PWR_GFXCORE_BOOT
PWR_GFXCORE_HG
PWR_GFXCORE_PH
PWR_GFXCORE_LG
VCC_AXG_SENSE
VSS_AXG_SENSE
1D05V_VTT
3D3V_S5
5V_S5
3D3V_S0
PWR_VCCCORE_PGD
PWR_VCCCORE_SDA
PWR_VCCCORE_ALERT#
PWR_VCCCORE_SCLK
PWR_VCCCORE_VRON
PWR_VCCCORE_IMON
PWR_VCCCORE_NTC
PWR_VCCCORE_VW
IMVP_PWRGD
H_PROCHOT#
PWR_VCCCORE_COMP
PWR_VCCCORE_FB
PWR_VCCCORE_FB_CR
PWR_VCCCORE_ISEN3
PWR_VCCCORE_ISEN3_CR
PWR_VCCCORE_ISEN2
PWR_VCCCORE_ISEN1
PWR_VCCCORE_ISUMN
PWR_VCCCORE_VDD
PWR_VCCCORE_VSUM+
PWR_VCCCORE_VSUM_RR
PWR_VCCCORE_VSUM-
PWR_VCCCORE_VSUM-CR
PWR_VCCCORE_NTC_RR
PWR_VCCCORE_BOOT2
PWR_VCCCORE_HG2
PWR_VCCCORE_PH2
PWR_VCCCORE_LG2
PWR_VCORE_VDDP
PWR_VCCCORE_PWR3_R
PWR_VCCCORE_LG1
PWR_VCCCORE_PH1
PWR_VCCCORE_HG1
PWR_VCCCORE_BOOT1
PWR_VCORE_PRG1
PWR_VCORE_VIN
PWR_DCBATOUT_VCCCORE1
VCC_CORE
VCCSENSE
VSSSENSE
H_CPU_SVIDDAT
H_CPU_SVIDCLK
VR_SVID_ALERT#
S0_PWR_GOOD
PWR_VCCSA_PWRGD
VSSSENSE
PR4201 Do Not Stuff UMA
PC4201 Do Not Stuff UMA
PR4202 Do Not Stuff DY
PC4202 Do Not Stuff UMA
PR4203 UMA Do Not Stuff
PC4203 Do Not Stuff UMA
PC4204 Do Not Stuff UMA
PR4204 UMA Do Not Stuff
PR4205 Do Not Stuff UMA
PR4206 Do Not Stuff UMA
PC4205 Do Not Stuff UMA
PC4206 SCD1U10V2KX-4GP
PR4209 130R2F-1-GP
PR4210 75R2F-2-GP
PR4211 5409R2F-L1-GP
PR4208 Do Not Stuff
PR4212 Do Not Stuff
PR4213 Do Not Stuff UMA
PR4214 Do Not Stuff
PR4215 Do Not Stuff DY
PR4216 Do Not Stuff
PR4217 1K91R2F-1-GP
PR4218 33K2R2F-GP
PC4207 SCD01U25V2KX-3GP
PC4208 SC47P50V2JN-3GP
PR4219 Do Not Stuff DY
PC4209 Do Not Stuff DY
PR4251 3K83R2F-GP
PR4221 NTC-470K-9-GP
PR4222 27K4R2F-GP
PR4223 8K06R2F-GP
PC4210 SC1000P50V3JN-GP-U
PR4224 Do Not Stuff DY
PC4212 SC22P50V2JN-4GP
PR4225 499R2F-2-GP
PC4214 SC470P50V-2-GP
PC4211 SC100P50V3JN-GP
PC4213 SC150P50V2KX-GP
PR4226 316KR2F-GP
PR4227 3K57R2F-GP
PR4228 Do Not Stuff DY
PR4229 Do Not Stuff DY
PC4218 Do Not Stuff DY
PC4219 SC1000P50V3JN-GP-U
PC4220 SC330P50V2KX-3GP
PR4231 2K2R2F-3-GP
PC4233 SC560P50V2KX-2GP
PC4215 Do Not Stuff DY
PC4216 SCD22U10V2KX-1GP
PC4217 SCD22U10V2KX-1GP
PR4232 24K9R2F-L-GP
PR4230 Do Not Stuff DY
PC4221 Do Not Stuff DY
PC4222 Do Not Stuff UMA
PR4223 Do Not Stuff UMA
PR4250 Do Not Stuff DY
PC4224 Do Not Stuff
PR4233 UMA Do Not Stuff
PR4234 UMA Do Not Stuff
PR4235 UMA Do Not Stuff
PR4237 Do Not Stuff
PR4238 Do Not Stuff
PR4247 0R2J-2-GP DIS
PC4225 SC1U10V2KX-1GP
PC4226 SC1U10V2KX-1GP
PR4239 1K69R2F-2-GP
PR4240 Do Not Stuff
PR4241 1R2F-GP
PC4227 SC1U10V2KX-1GP
PC4228 SCD22U25V3KX-GP
PR4243 2K49R2F-1-GP
PR4242 11K2R2F-L-GP
PR4244 NTC-10K-27-GP
PC4229 SCD22U10V2KX-1GP
PC4230 SCD22U25V2KX-GP
PR4245 1K82R2F-1-GP
PR4246 Do Not Stuff DY
PC4231 DY Do Not Stuff
PC4232 SCD1U10V2KX-4GP
N12M GS2 HYN1GB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Core-1(ISL95831)
Size A3
Document Number
Z50-HR { Huron River Platform}
Rev -1
Date: Wednesday, March 02, 2011
Sheet 35 of 74


84.00172.037
SIR172DP-T1-GE3
Id=20A, Qg=9.8~15nC,
Rdson=10.3~12.4mohm
20101114
PWR_DCBATOUT_VCCCORE1
PU4308
PU4310
PC4313
PC4314
PC4315
PC4316
PC4317
EC4302
SCD1U25V2KX-GP
PR4314
2D2R3-1-U-GP
35 PWR_VCCCORE_BOOT1
PWR_VCCCORE_BOOT1_1
PC4318
SCD22U25V3KX-GP
PWR_VCCCORE_HG1
84.07698.037
2ND = 84.08065.037
35 PWR_VCCCORE_HG1
35 PWR_VCCCORE_PH1
2ND = 68.R3610.10M
68.R3610.20A
20110117
VCC_CORE
PL4303
L-D36UH-1-GP
PU4309
PU4311
PG4317
PG4318
PT4301
PT4309
PT4308
SE470UF2VDM-GP
PR4315
PWR_VCCCORE_ISEN2 35
PR4317
1R2F-GP
PWR_VCCCORE_VSUM- 35
PWR_VCCCORE_VSUM- 1
PWR_VCCCORE_VSUM+ 1
PR4318
10KR2F-2-GP
PWR_VCCCORE_ISEN1 35
PR4319
3K65R2F-1-GP
PWR_VCCCORE_VSUM+ 35
84.00308.B30
2ND = 84.08057.037
35 PWR_VCCCORE_LG1
DCBATOUT
PWR_DCBATOUT_VCCCORE1
PG4319
PG4320
PG4321
PG4322
PG4323
PG4324
PT4306
Do Not Stuff
79.47612.3FL
OSCON
Lelon 47uF, 25V
ESR<440mΩ, Iripple=230mA
Vcc_core
Iomax=53A
OCP>80A
20101114
PWR_DCBATOUT_VCCCORE2
PU4312
PU4313
PC4307
PC4308
PC4309
PC4310
PC4311
EC4301
PR4308
2D2R3-1-U-GP
35 PWR_VCCCORE_BOOT2
PWR_VCCCORE_BOOT2_1
PC4312
SCD22U25V3KX-GP
PWR_VCCCORE_HG2
35 PWR_VCCCORE_HG2
35 PWR_VCCCORE_PH2
35 PWR_VCCCORE_LG2
2ND = 68.R3610.10M
68.R3610.20A
20110117
VCC_CORE
PL4302
L-D36UH-1-GP
PU4314
PU4315
PG4303
PG4304
PT4303
PT4304
PT4305
SE470UF2VDM-GP
PR4309
PWR_VCCCORE_ISEN1 35
PR4311
1R2F-GP
PWR_VCCCORE_VSUM- 35
PWR_VCCCORE_VSUM- 2
PR4312
10KR2F-2-GP
PWR_VCCCORE_ISEN2 35
PR4313
3K65R2F-1-GP
PWR_VCCCORE_VSUM+ 35
20101117
20100921
84.00308.B30
2ND = 84.08057.037
DCBATOUT
PWR_DCBATOUT_VCCCORE2
PG4325
PG4326
PG4327
PG4328
PG4329
PG4330
PT4307
SE47U25VM-13-GP
79.47612.3GL
79.47612.3FL
OSCON
Lelon 47uF, 25V
ESR<440mΩ, Iripple=230mA
N12M GS2 HYN1GB
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Core-2(ISL95831)
Size
A3
Document Number
Z50-HR { Huron River Platform}
Rev
-1
Date: Wednesday, March 02, 2011
Sheet 36 of 74



N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU Core-3(ISL95831)***

Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

Date: Wednesday, March 02, 2011 Sheet 37 of 74

TPS51218D for 1D05V

DCBATOUT PWR_DCBATOUT_1D05V
PG4501 Do Not Stuff
PG4502 Do Not Stuff
PG4503 Do Not Stuff
PG4504 Do Not Stuff
PT4501 SE47U25VM-13-GP
79.47612.3GL

79.47612.3FL
OSCON
Lelon 47uF, 25V
ESR<440mΩ, Iripple=230mA

1D05V_VTT 1D05V_PWR 1D05V_VTT
PG4513 PG4505 PG4514 PG4506 PG4515 PG4507 PG4516 PG4508 PG4517 PG4509 PG4518 PG4510 PG4519 PG4511 PG4520 PG4512
Do Not Stuff

1D05V_VTT
PT4504 SE330U2VDM-L-GP
79.33719.L01
2ND = 77.C3371.051

Freq=360KHz

20101114
PWR_DCBATOUT_1D05V
PU4502 FDMS7698-GP
84.07698.037
2ND = 84.08065.037
PU4503 FDMS0312S-GP
84.00312.037
2ND = 84.08059.037
PC4504 SC4D7U25V5KX-GP
PC4506 SC4D7U25V5KX-GP
PC4507 DY Do Not Stuff
PC4511 SCD1U25V3KX-GP

20101114
Iomax=14A
OCP>21A

20101114
PL4501 IND-D88UH-10-GP
68.R8810.10G
2ND = 68.R8810.201

1D05V_PWR
79.33719.L01
PC4508 DY Do Not Stuff
PT4502 SE330U2VDM-L-GP
PT4503 DY Do Not Stuff
PC4509 DY Do Not Stuff
2ND = 77.C3371.051

79.33719.L01
Panasonic cap 330uF
2V, ESR=9mohm

PR4516 10KR2J-3-GP
3D3V_S0
20101124
PR4504 93K1R2F-L-GP
64.93125.6DL
2ND = 64.68025.6DL
30,41,68 1.05VTT_PWRGD
30,39,40 RUNPWROK
PR4512 Do Not Stuff
PC4505 SC1KP50V2KX-1GP
PR4503 470KR2F-GP

PU4501 TPS51218DSCR-GP-U1
PGOOD TRIP EN VFB RF GND VBST DRVH SW V5IN DRVL
PWR_1D05V_IMAX
PWR_1D05V_EN
PWR_1D05V_VFB
PWR_1D05V_CCM
PWR_1D05V_BOOT
PWR_1D05V_UGATE
PWR_1D05V_PHASE
PWR_1D05V_LGATE
5V_S5

PR4505 2D2R3-1-U-GP
PC4503 SCD1U25V3KX-GP
PWR_1D05V_BOOT_R

VTT_SENSE_L
PR4507 10KR2F-2-GP
PWR_1D05V_VFB
PR4508 20KR2F-L-GP
VSS_SENSE_L
PR4509 DY Do Not Stuff

PVT

Vout=0.704*(1+R1/R2)

VTT_SENSE_L
PR4510 Do Not Stuff
PC4510 SC1000P50V3JN-GP-U
VCCIO_SENSE 8
VSS_SENSE_L
PR4511 Do Not Stuff
VSSIO_SENSE 8
ED4501 VARISTOR-5V-1-GP
ED4502 VARISTOR-5V-1-GP

PVT

N12M GS2 HYN1GB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1D05V(TPS51218D)
Size: A3
Document Number: Z50-HR { Huron River Platform}
Rev: -1
Date: Wednesday, March 02, 2011
Sheet 38 of 74

SSID = PWR.Plane.Regulator_1p5v0p75v

RT8207 for 1D5V and 0D75V

79.47612.3FL
OSCON
Lelon 47uF, 25V
ESR<440mΩ, Iripple=230mA

Close to pin23

Close to pin23

Iomax=1A
OCP>1.5A

Close to output cap pin1, not inside of the output cap

+0.75VS
Iomax: 1.2A

Close to PIN9

20101124

20101114

20101125

Mag. 1.0uH 10*10*4
DCR=2.9~3.3mohm
Idc=18A, Isat=36A

Iomax=12A
OCP>20A
PVT

79.33719.L01
Panasonic cap 330uF
2V, ESR=9mohm

DVT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

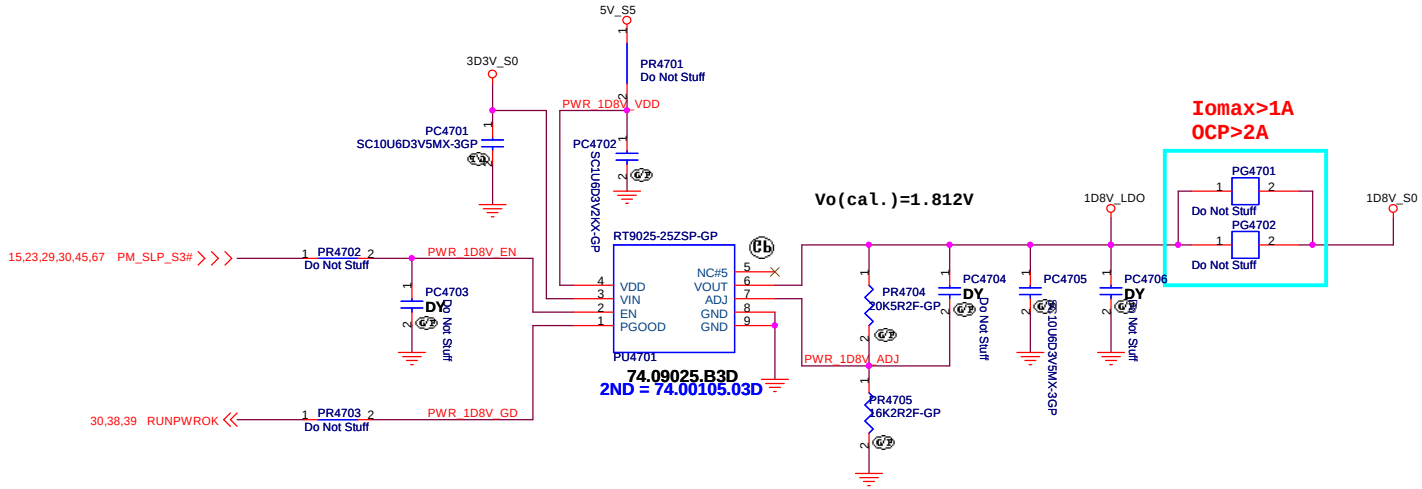
Title: RT8207

Size: Custom | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 39 of 74

SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



N12M GS2 HYN1GB

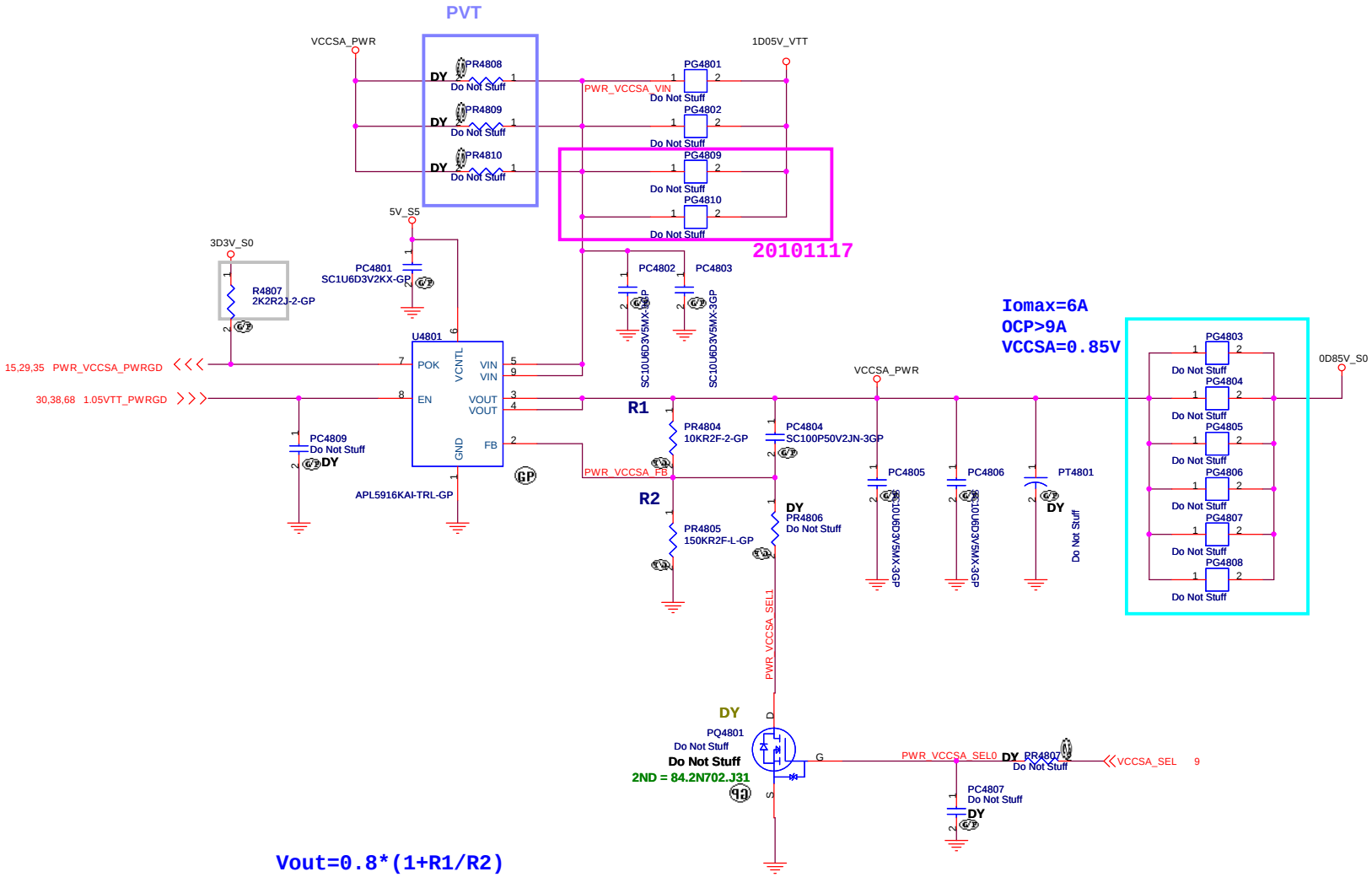
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LDO_1D8V(RT9025)*

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 40 of 74

APL5916 for VCCSA



VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO_VCCSA(APL5916)

Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

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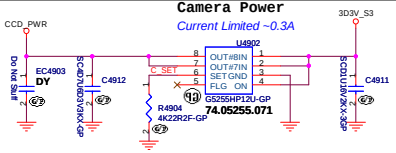
SSID = VIDEO

LVDS CONNECTOR

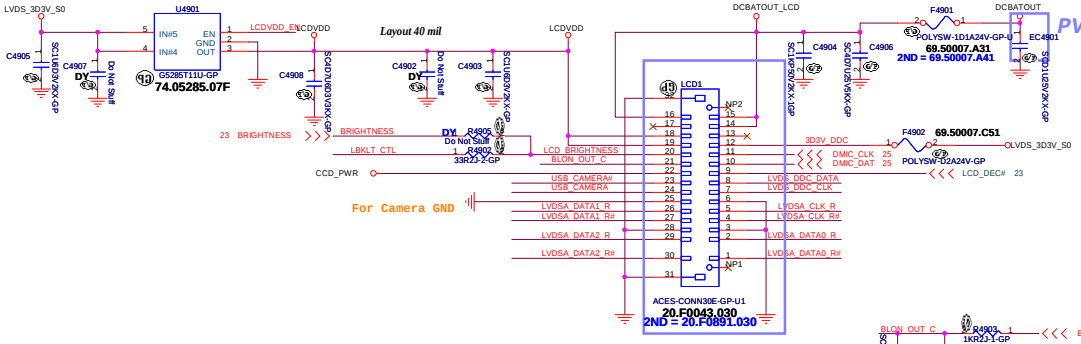
Impedance:90ohm

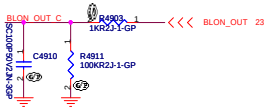
Camera Power

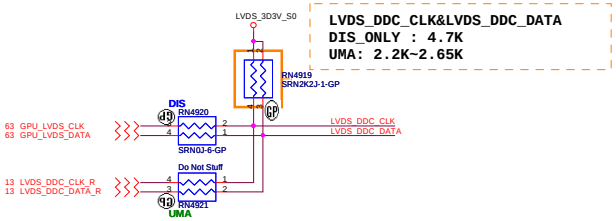
Current Limited ~0.3A

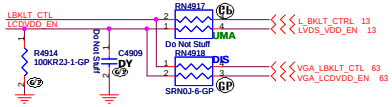


Power En



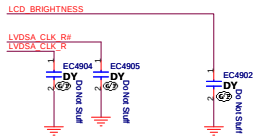




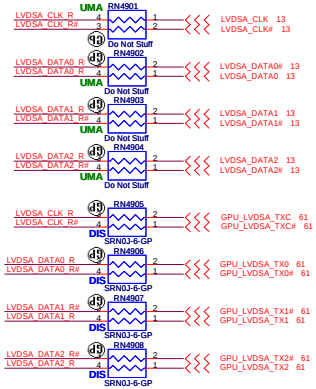


For EMI request

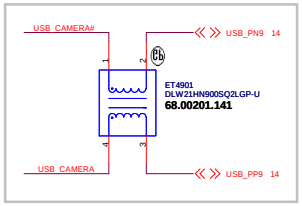
Close to LVDS connector



LVDS Channel A



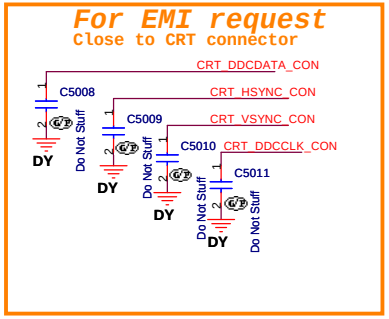
LVDS Channel B

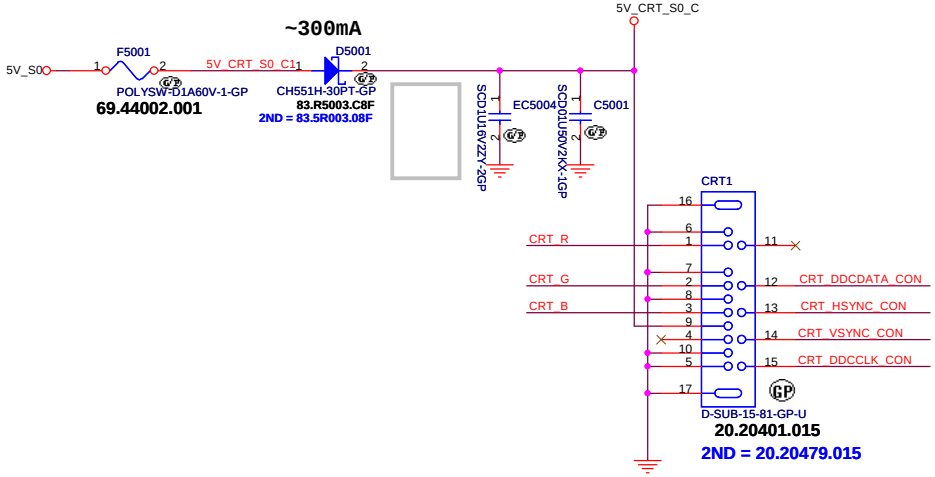


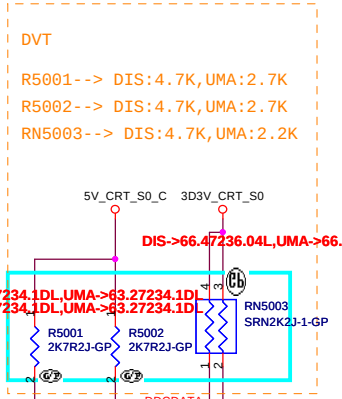
N12M GS2 HYN1GB

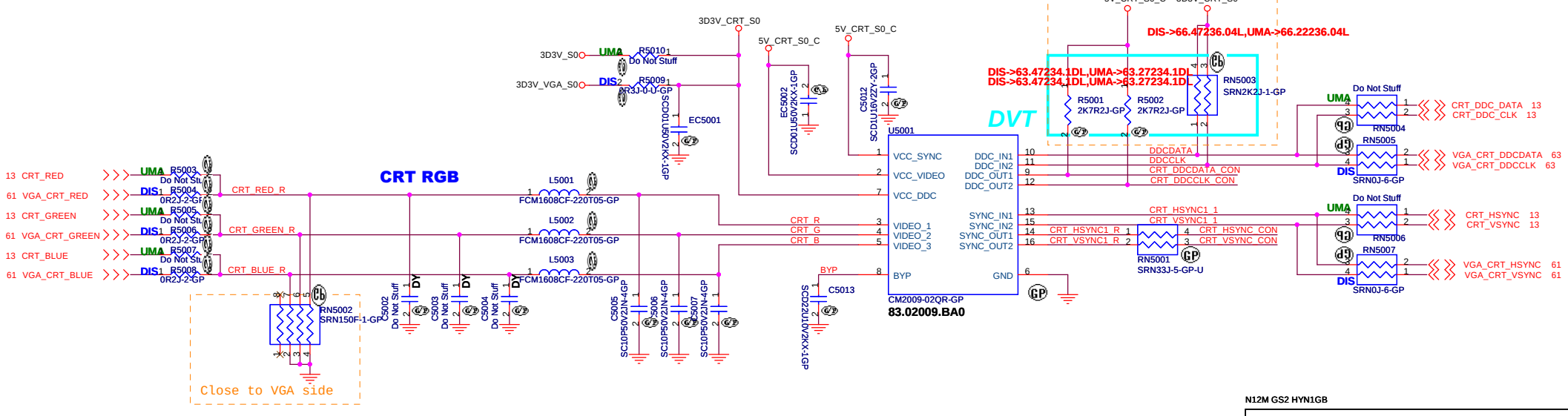
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD Connector		
Size: A2	Document Number: Z50-HR { Huron River Platform}	Rev: -1
Date: Wednesday, March 02, 2011	Sheet 42 of 74	

CRT I/F & CONNECTOR









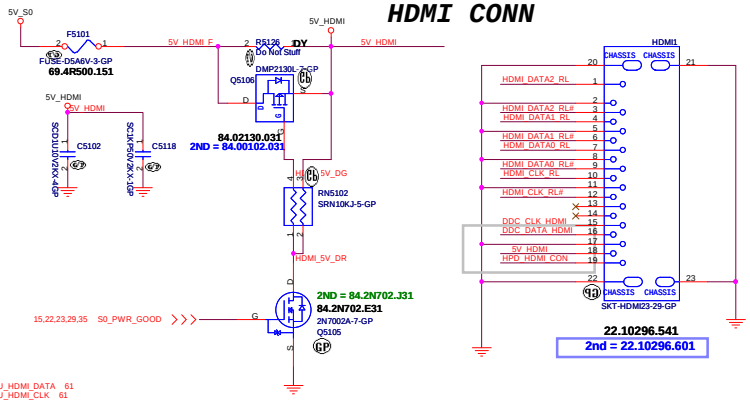
N12M GS2 HYN1GB

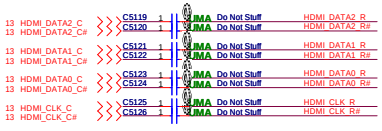
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CRT Connector	
Size A3	Document Number: Z50-HR { Huron River Platform}	Rev: -1
Date: Friday, March 18, 2011	Sheet 43 of 74	

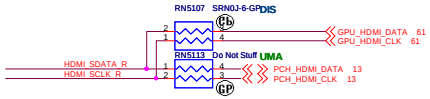
SSID = VIDEO

HDMI Level Shifter& CONNECTOR

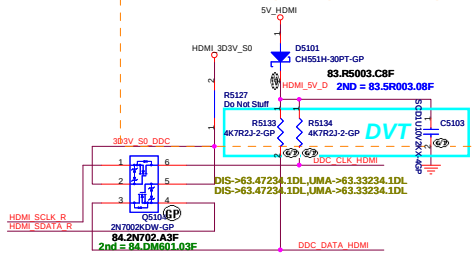
HDMI CONN

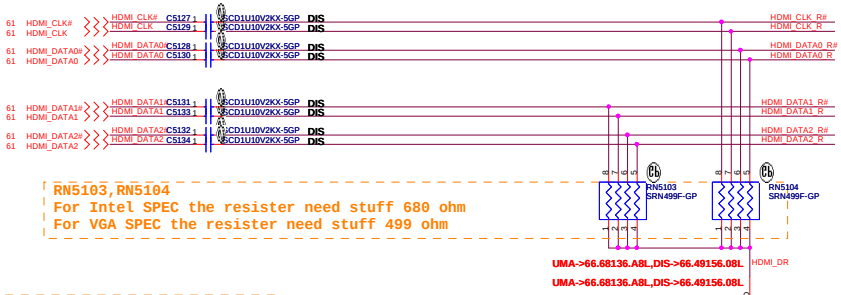


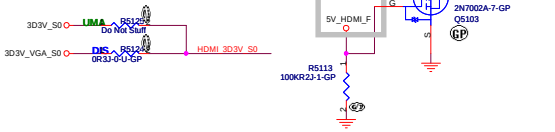


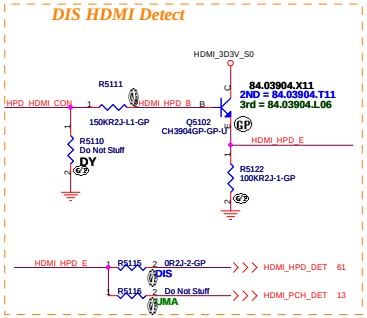


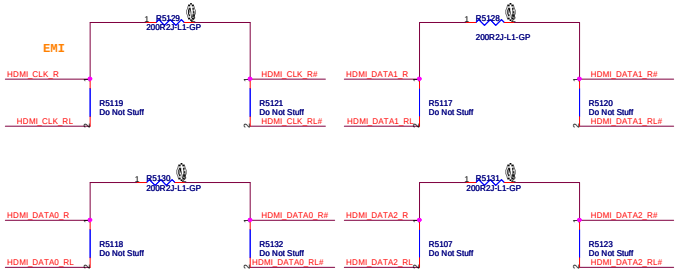
DVT
R5133 DIS 4.7K pull up ,UMA 3.3K pull up
R5134 DIS 4.7K pull up ,UMA 3,3K pull up











N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

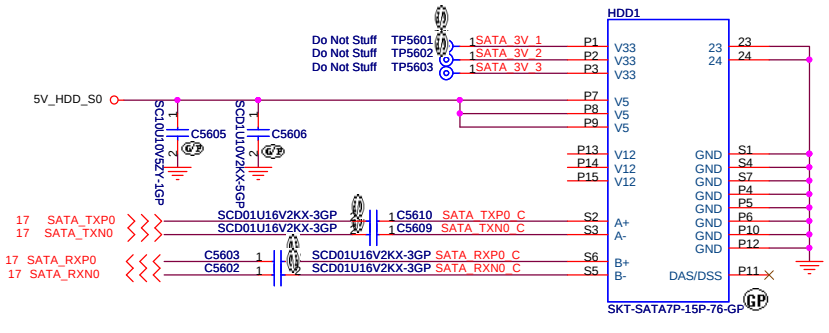
Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A2	Z50-HR { Huron River Platform}	-1

Date: Wednesday, March 02, 2011 Sheet 44 of 74

SSID = SATA

SATA HDD Connector

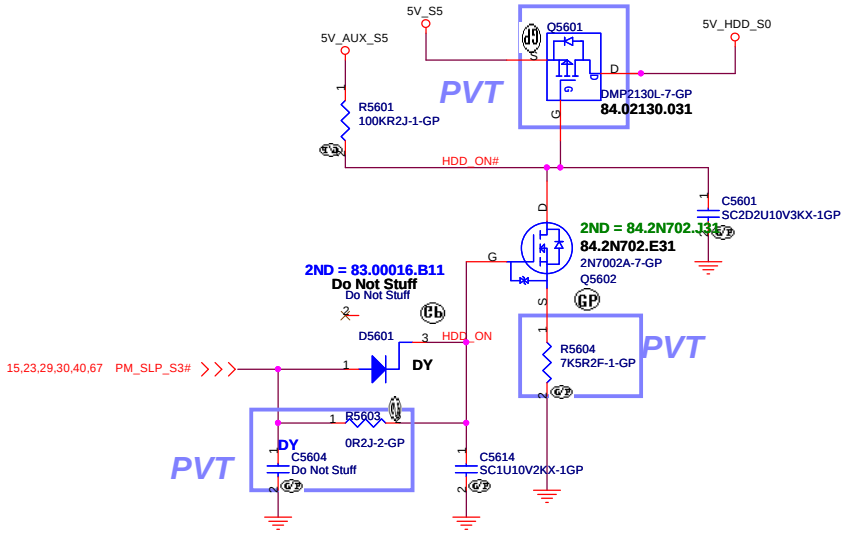


22.10300.C51

2ND = 20.81599.022

PVT

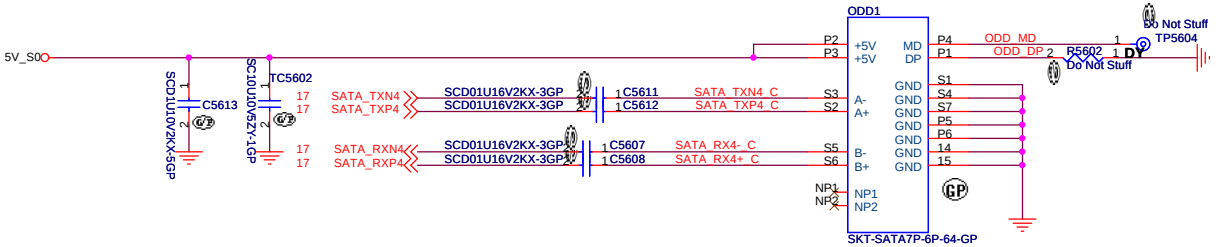
Delay HDD power



Delay HDD power off timing for 400ms after SATA controller shut down. Control the C5601 and R5601 to finally tune delay timing between 500ms and 400ms.

ODD Connector

SATA_RX- and SATA_RX+ Trace Length match within 20 mil



22.10300.C41

2nd = 22.10300.D11

PVT

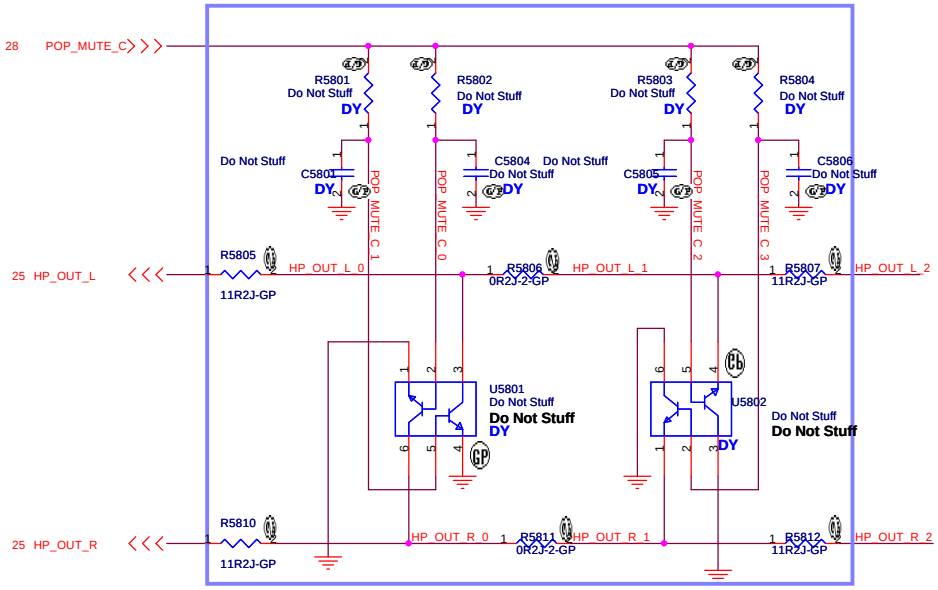
N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

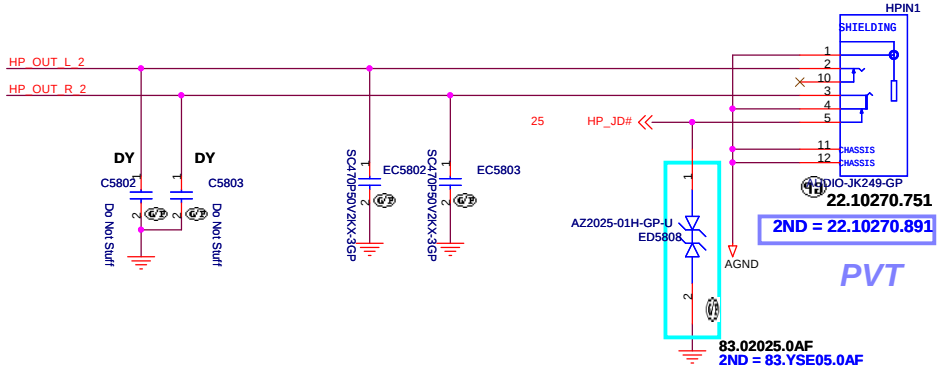
Title: HDD/ODD

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

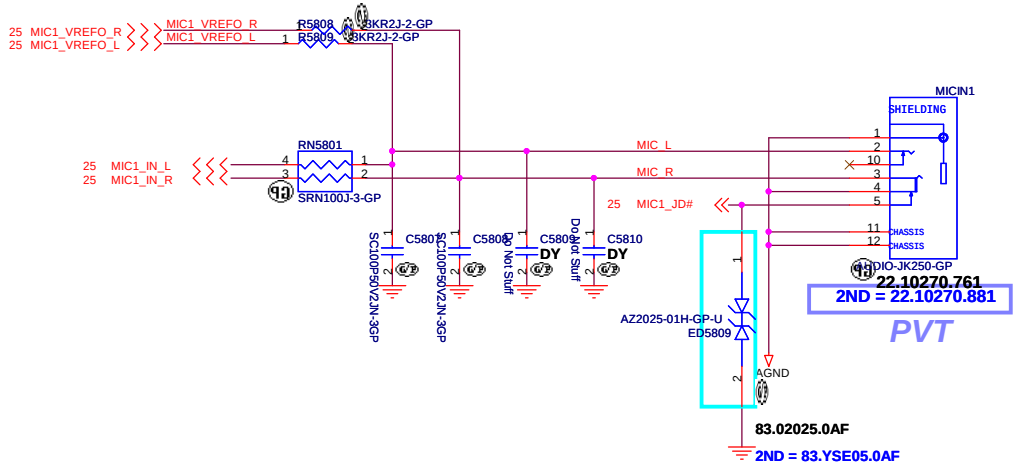
Date: Wednesday, March 02, 2011 | Sheet 45 of 74

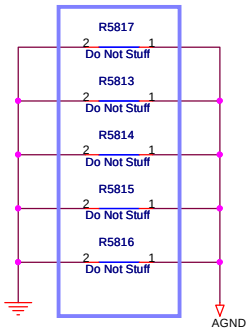


PVT

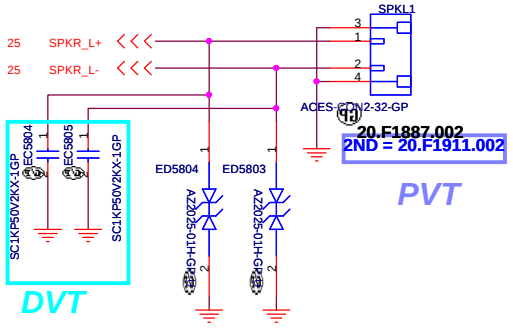


DVT





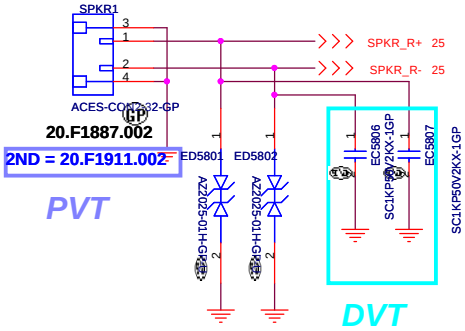
PVT



DVT

83.02025.0AF

2ND = 83.YSE05.0AF



PVT

DVT

83.02025.0AF

2ND = 83.YSE05.0AF

N12M GS2 HYN1GB

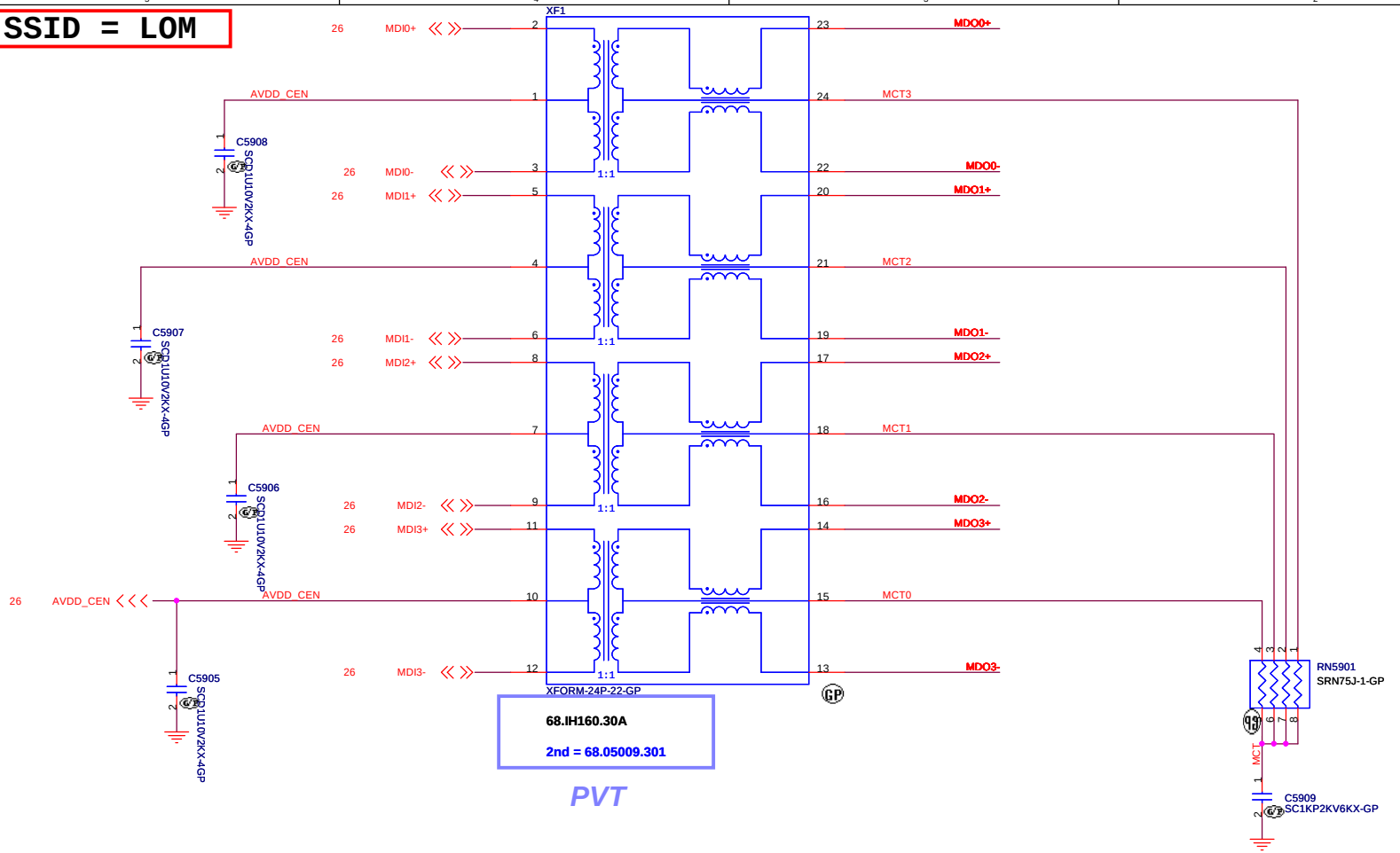
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

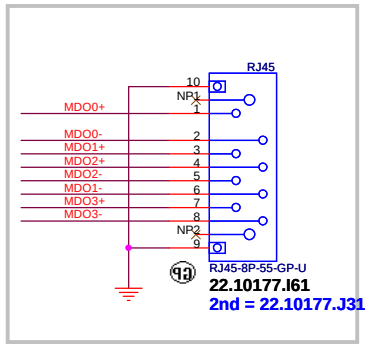
Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

Date: Wednesday, March 02, 2011 Sheet 46 of 74

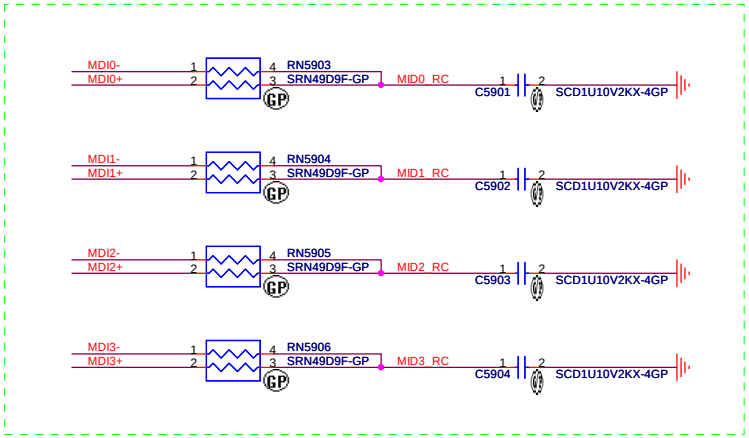
SSID = LOM



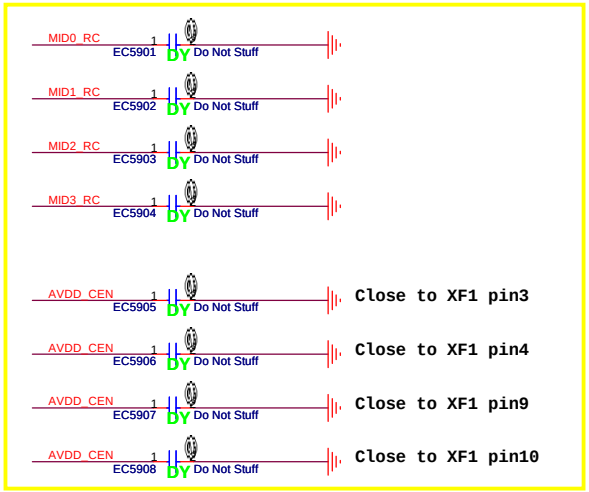
PVT



Close to LAN AR8151



EMI



N12M GS2 HYN1GB

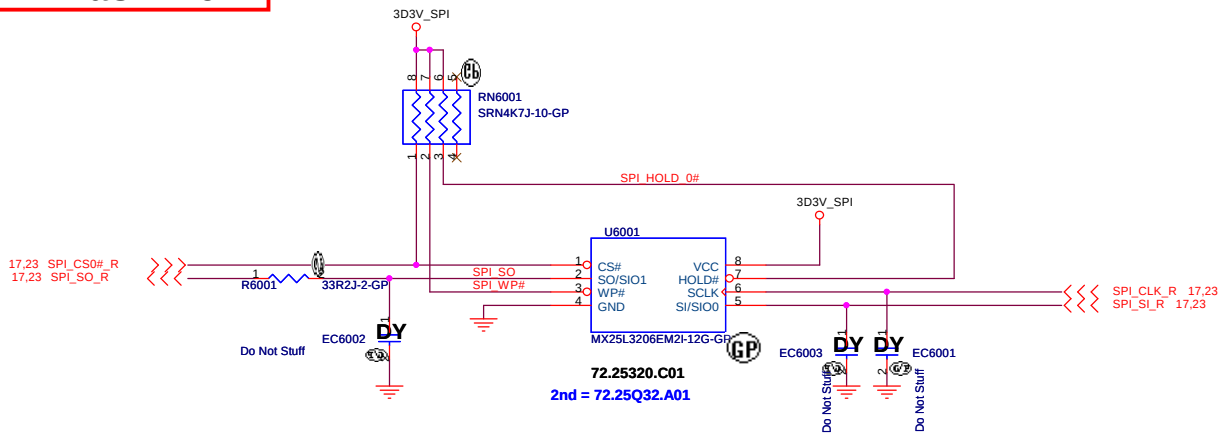
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

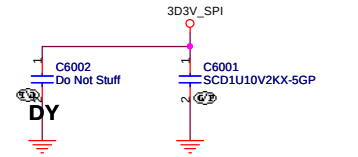
Title: **LAN CONNECTOR**

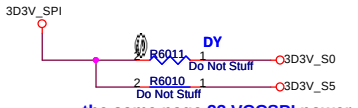
Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

Date: Wednesday, March 02, 2011 Sheet 47 of 74

SSID = Flash.ROM



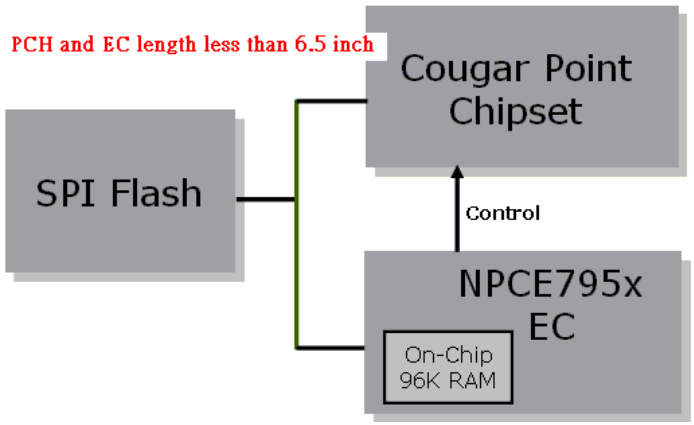


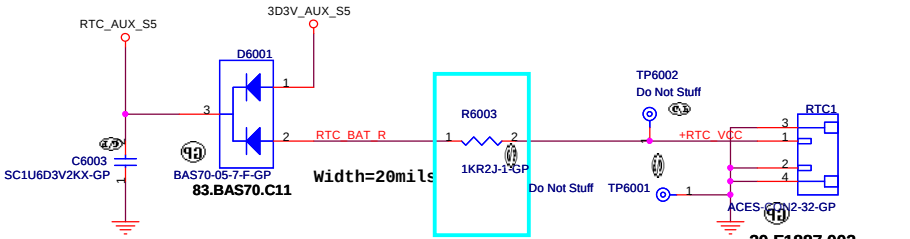


the same page 23 VCCSPI power

SYSTEM SPI ROM
Socket : 62.10089.001

SPI ROM Equal length need to less than 500mil



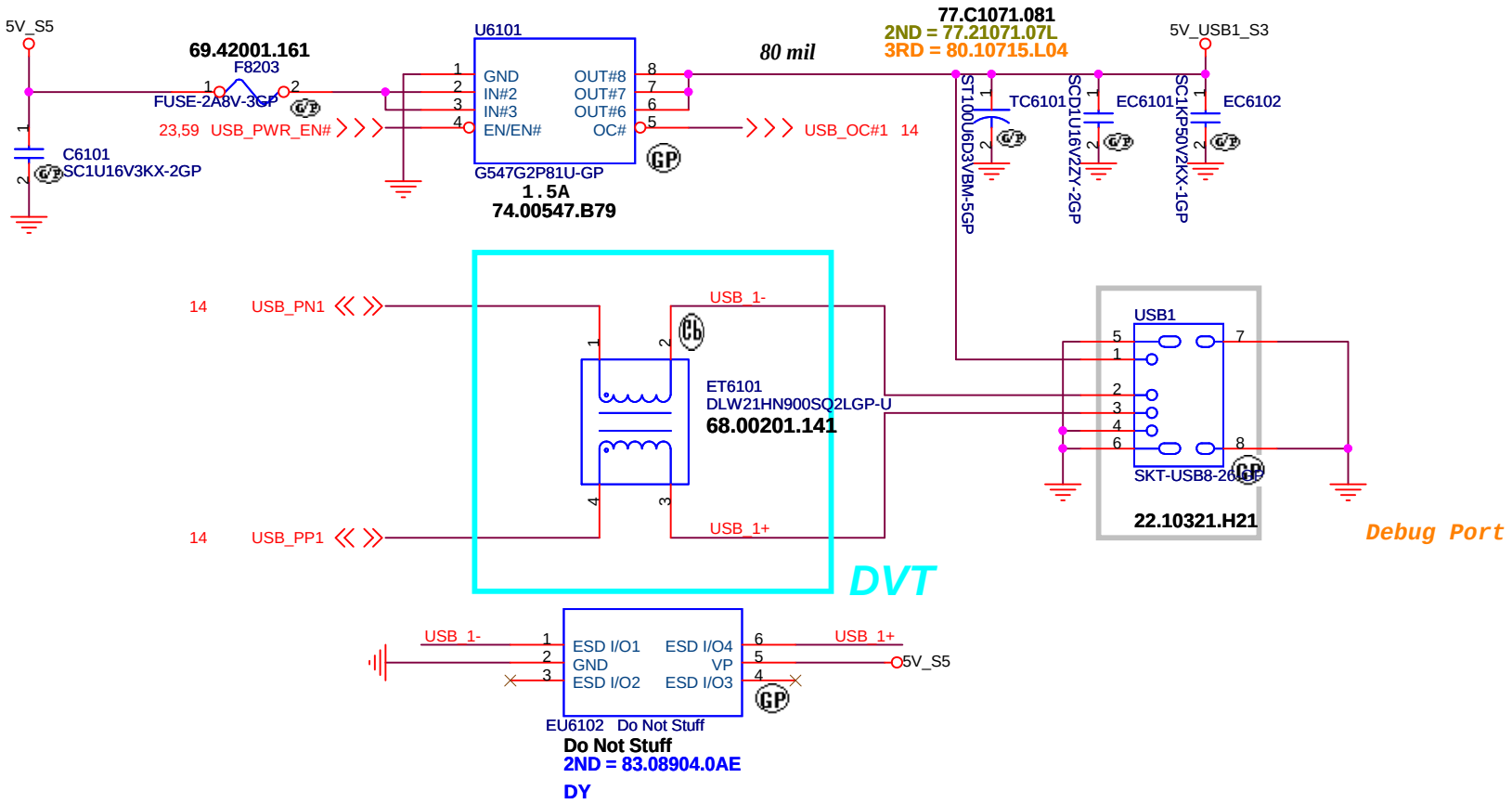


PVT

N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Flash(KBC+PCH)/RTC CONN***	
Size A3	Document Number **Z50-HR { Huron River Platform}**	Rev -1
Date: Wednesday, March 02, 2011	Sheet 48 of 74	



N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

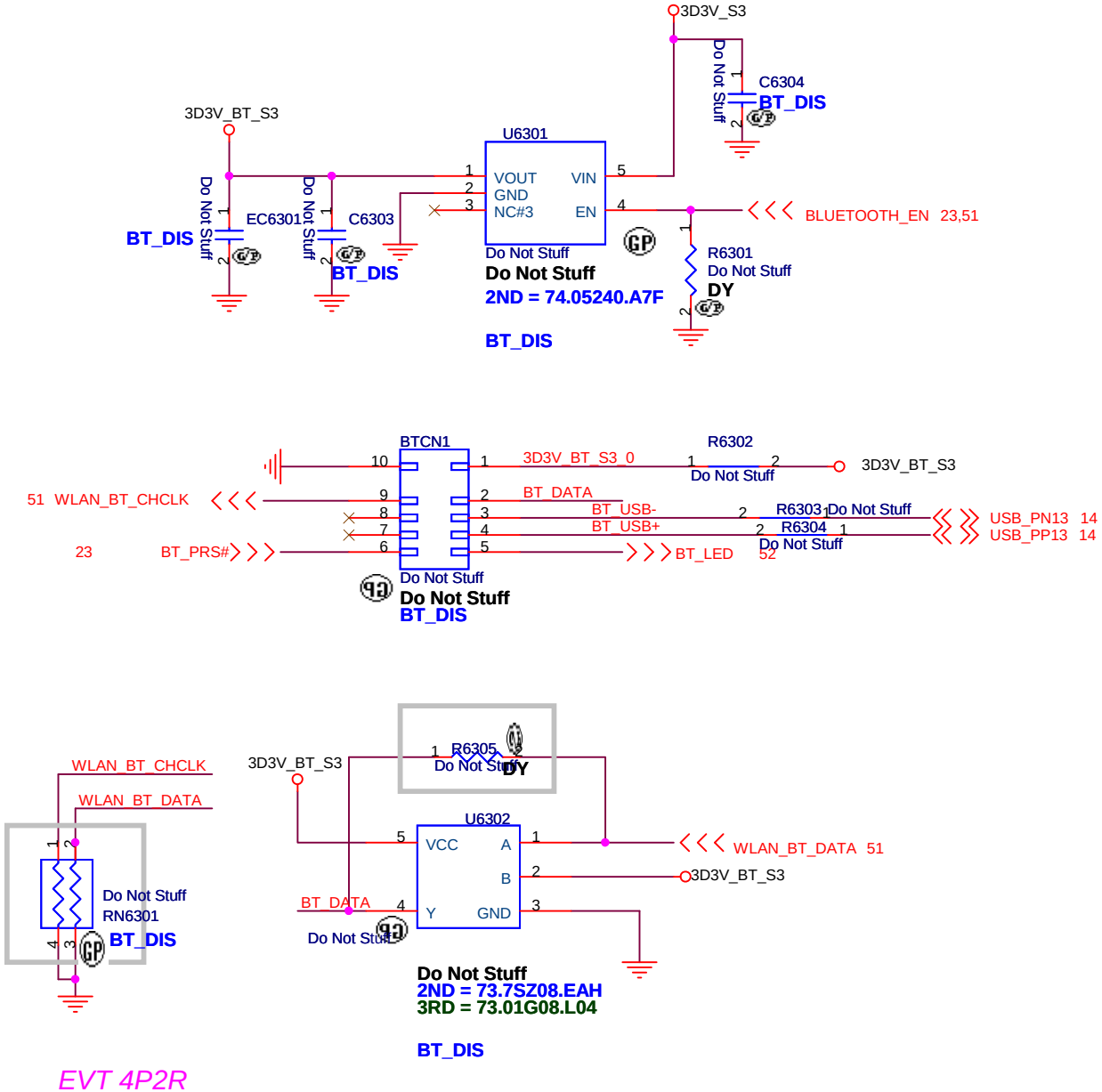
Size	Document Number	Rev
A4	Z50-HR { Huron River Platform}	-1

Date: Wednesday, March 02, 2011 Sheet 49 of 74

Bluetooth

SSID = User.Interface

Bluetooth Module conn.



EVT 4P2R

N12M GS2 HYN1GB

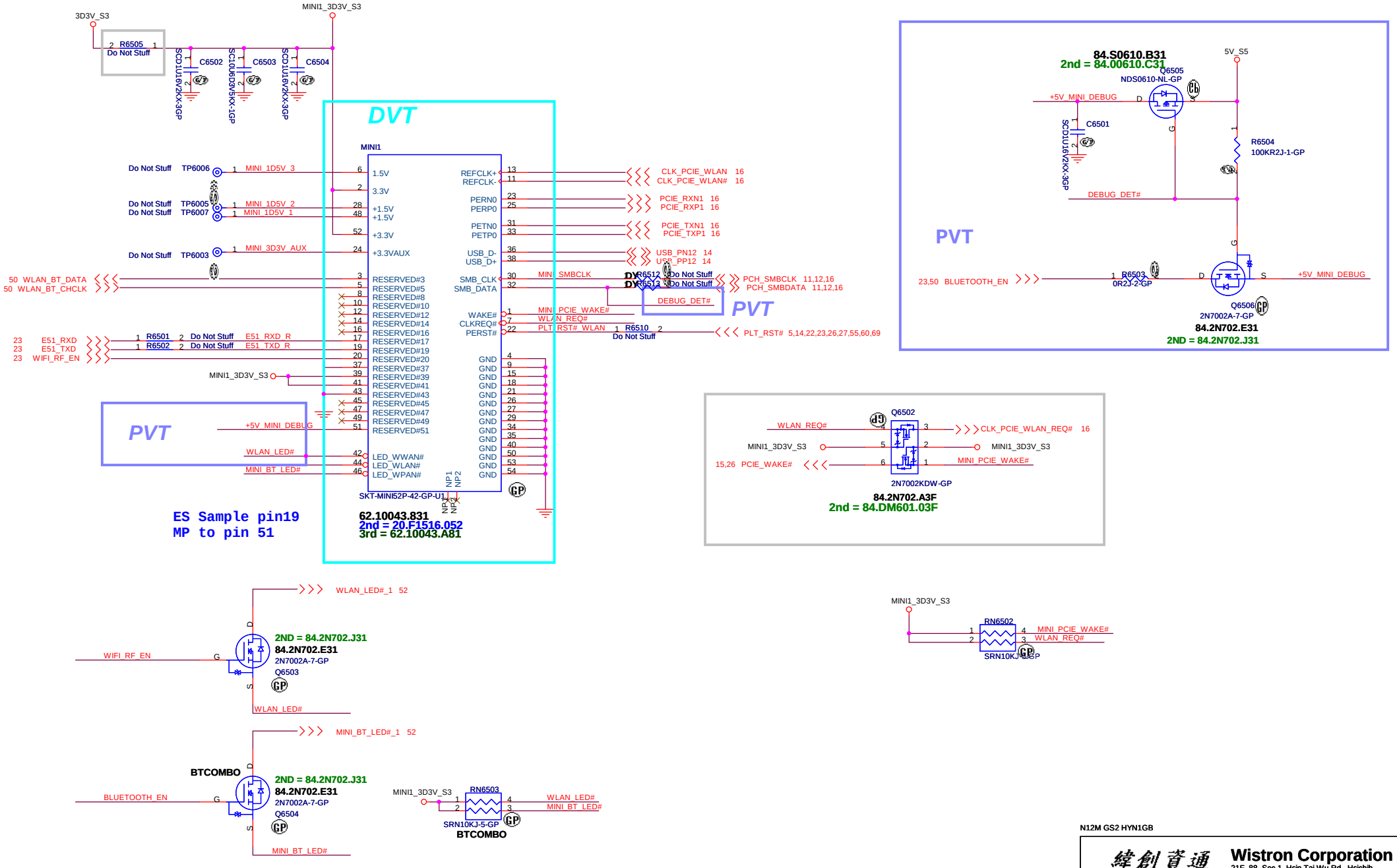
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A4	Z50-HR { Huron River Platform}	-1

Date: Wednesday, March 02, 2011 Sheet 50 of 74

SSID = Wireless Mini Card Connector(802.11a/b/g/n)



N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

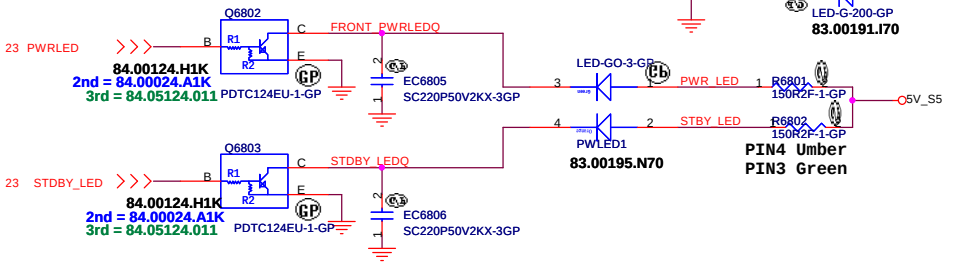
Title: MINICARD(WLAN&WMAX)

Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

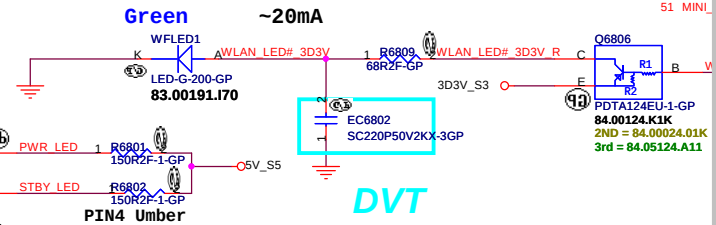
Date: Wednesday, March 02, 2011 Sheet 51 of 74

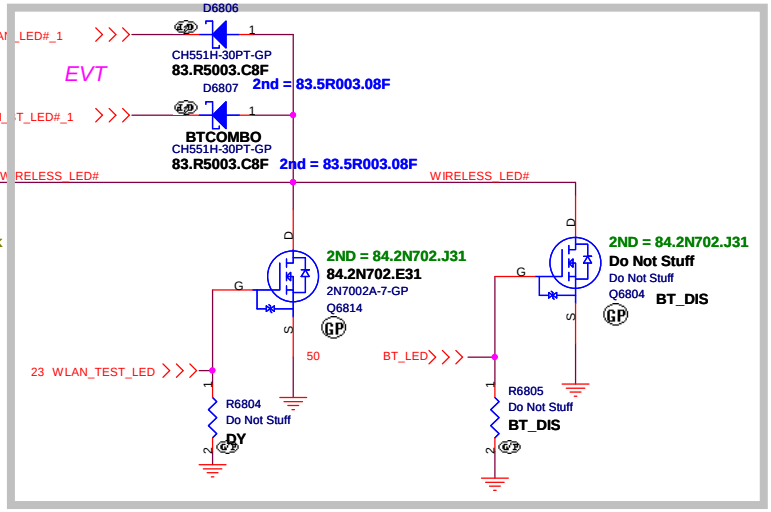
SSID = User.Interface

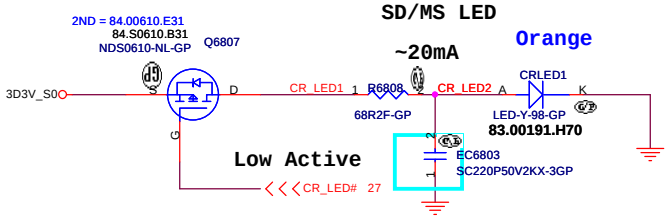
Power button LED
Power STDBY_LED



WLAN_LED



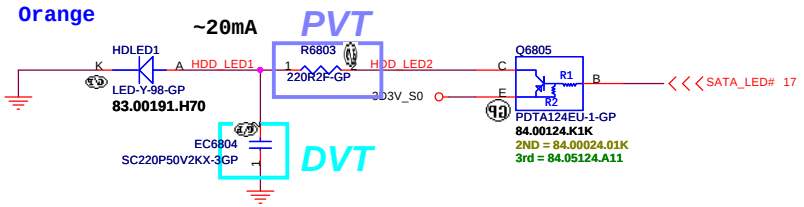




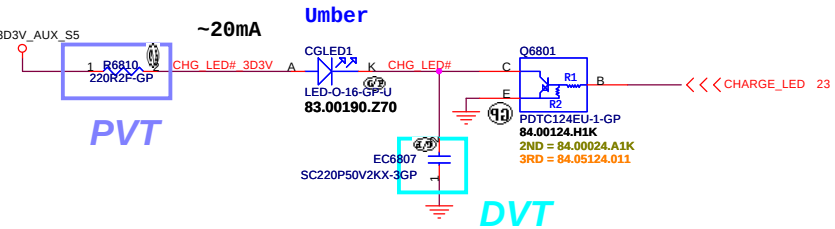
Common wireless SW(mechanical)	ON							
WLAN SW(software)	ON	OFF	ON	OFF	ON	OFF	ON	OFF
WWAN SW(software)	ON	ON	OFF	OFF	ON	ON	OFF	OFF
Bluetooth SW(software)	ON	ON	ON	ON	OFF	OFF	OFF	OFF
LED	TURN ON							OFF

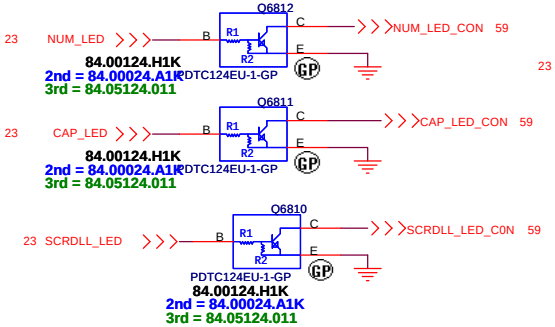
active	High	Low
WWAN(W_DISABLE#)	ON	OFF
WLAN(WLAN_LED#)	OFF	ON
Bluetooth(BT_LED)	ON	OFF

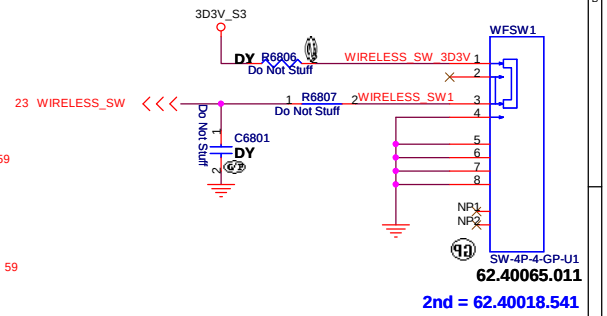
SATA HDD LED



Battery LED1(CHARGE)







N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

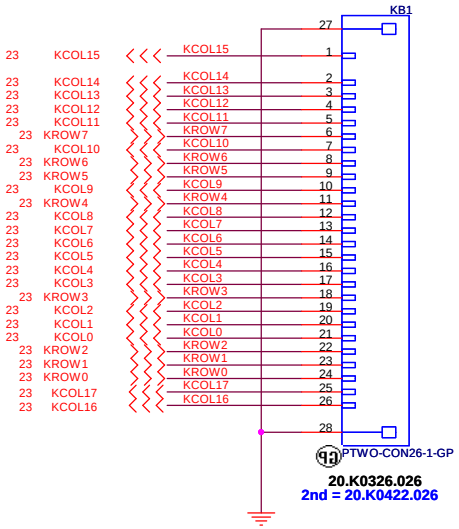
Title: LED /Wireless Switch

Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

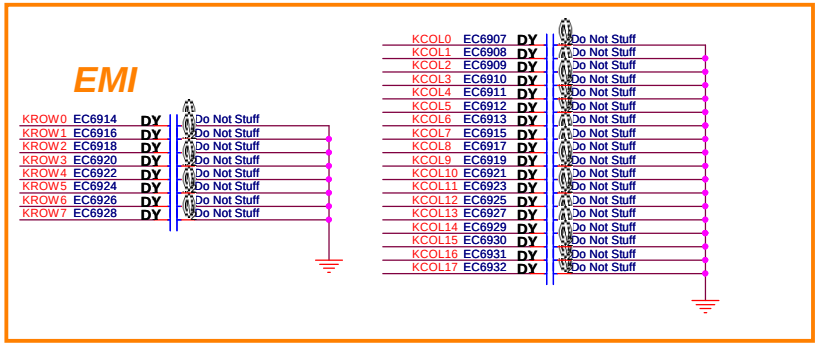
Date: Wednesday, March 02, 2011 Sheet 52 of 74

SSID = KBC

Internal KeyBoard Connector

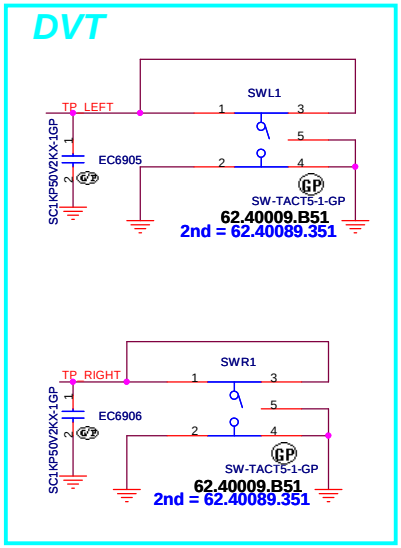


EMI

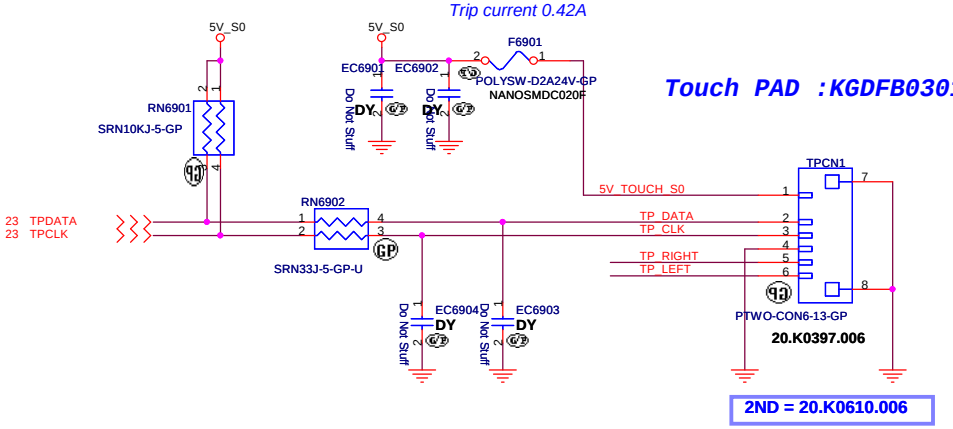


TOUCH PAD

DVT

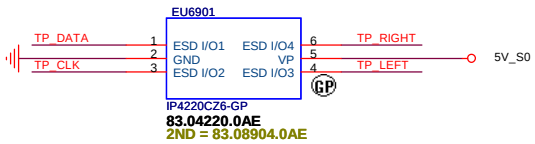


Current rating 0.2A
Trip current 0.42A



Touch PAD :KGDFB0301A

PVT



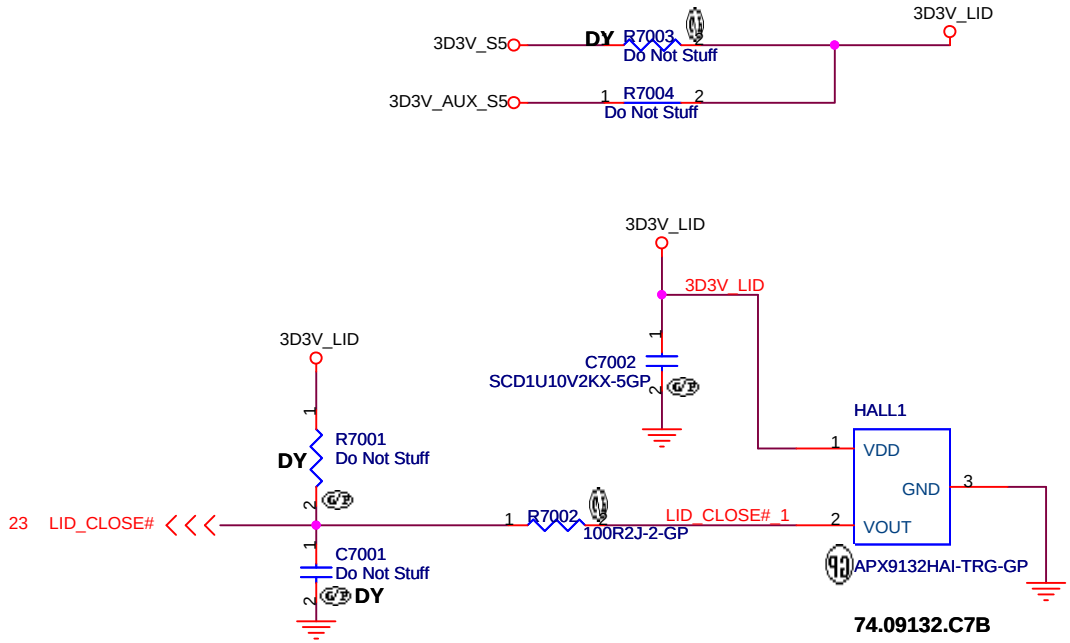
N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

Date: Wednesday, March 02, 2011 Sheet 53 of 74



N12M GS2 HYN1GB

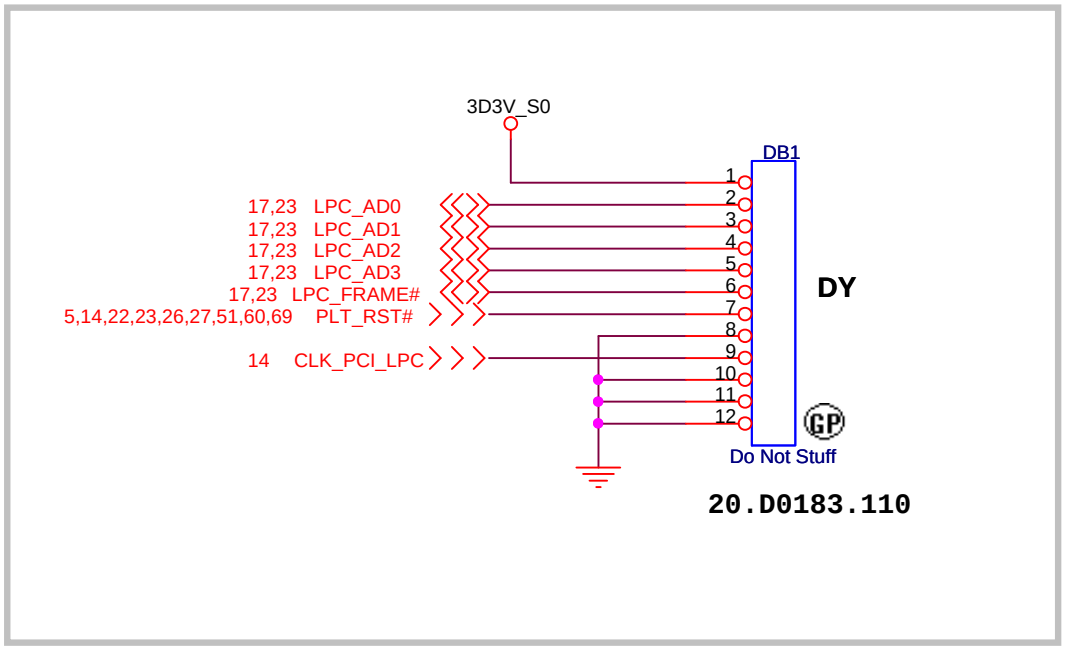
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	**Z50-HR { Huron River Platform}**	**-1**

Date: Wednesday, March 02, 2011 Sheet 54 of 74

EVT



N12M GS2 HYN1GB

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

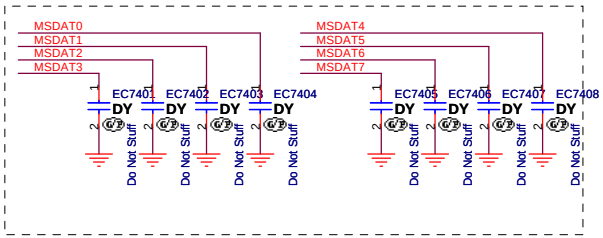
Dubug connector

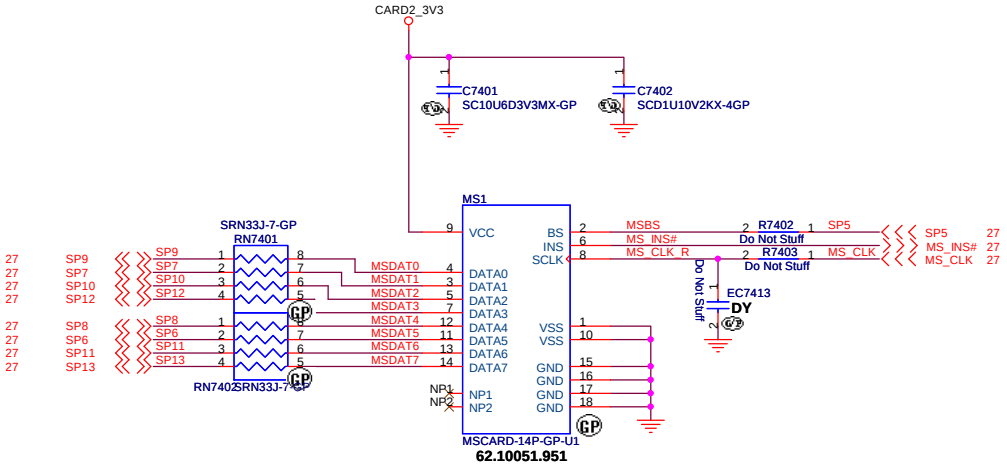
Size	Document Number	Rev
A	Z50-HR { Huron River Platform}	-1

Date: Wednesday, March 02, 2011 Sheet 55 of 74

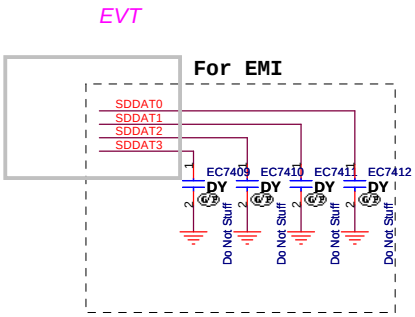
SSID = SDIO

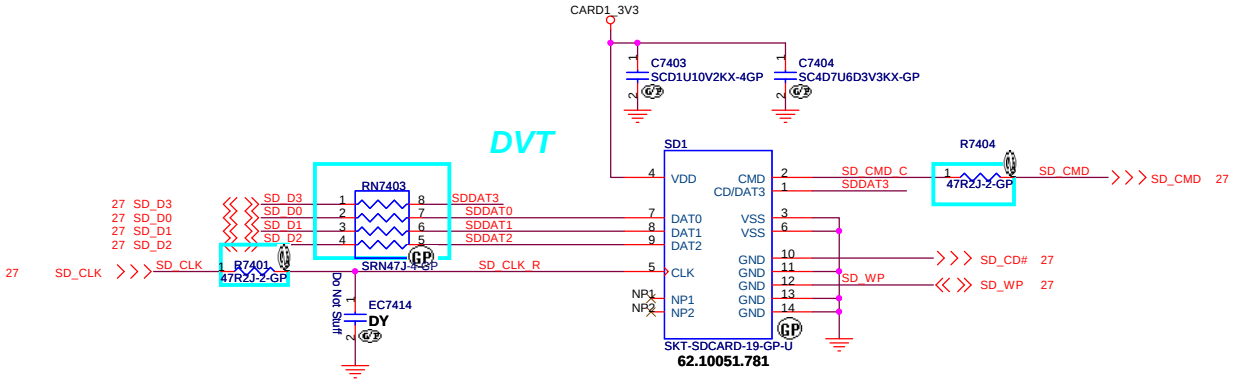
SD/MS Card Reader





MS CONN.





SD CARD CONN.

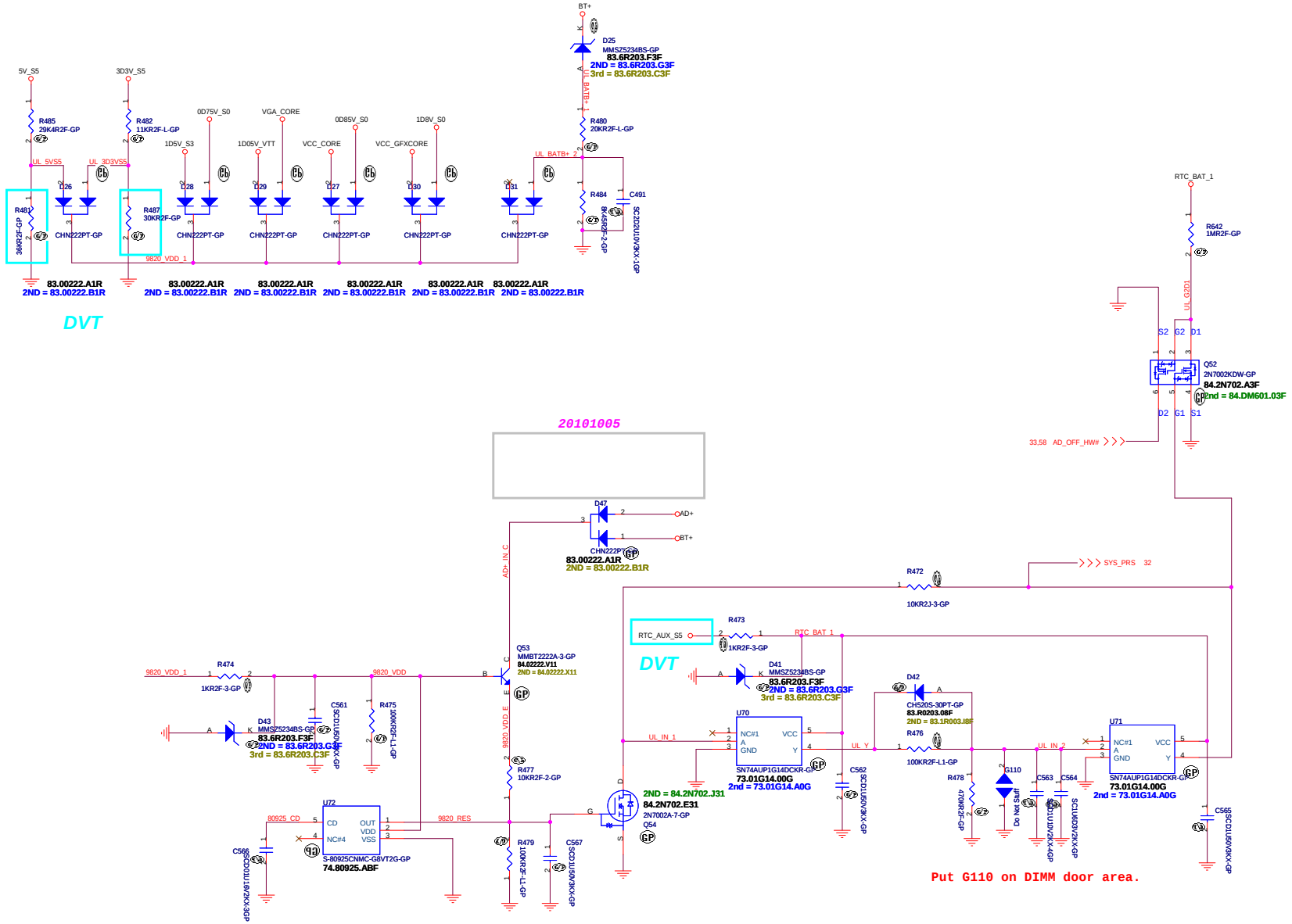
N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CARD Reader CONN***

Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

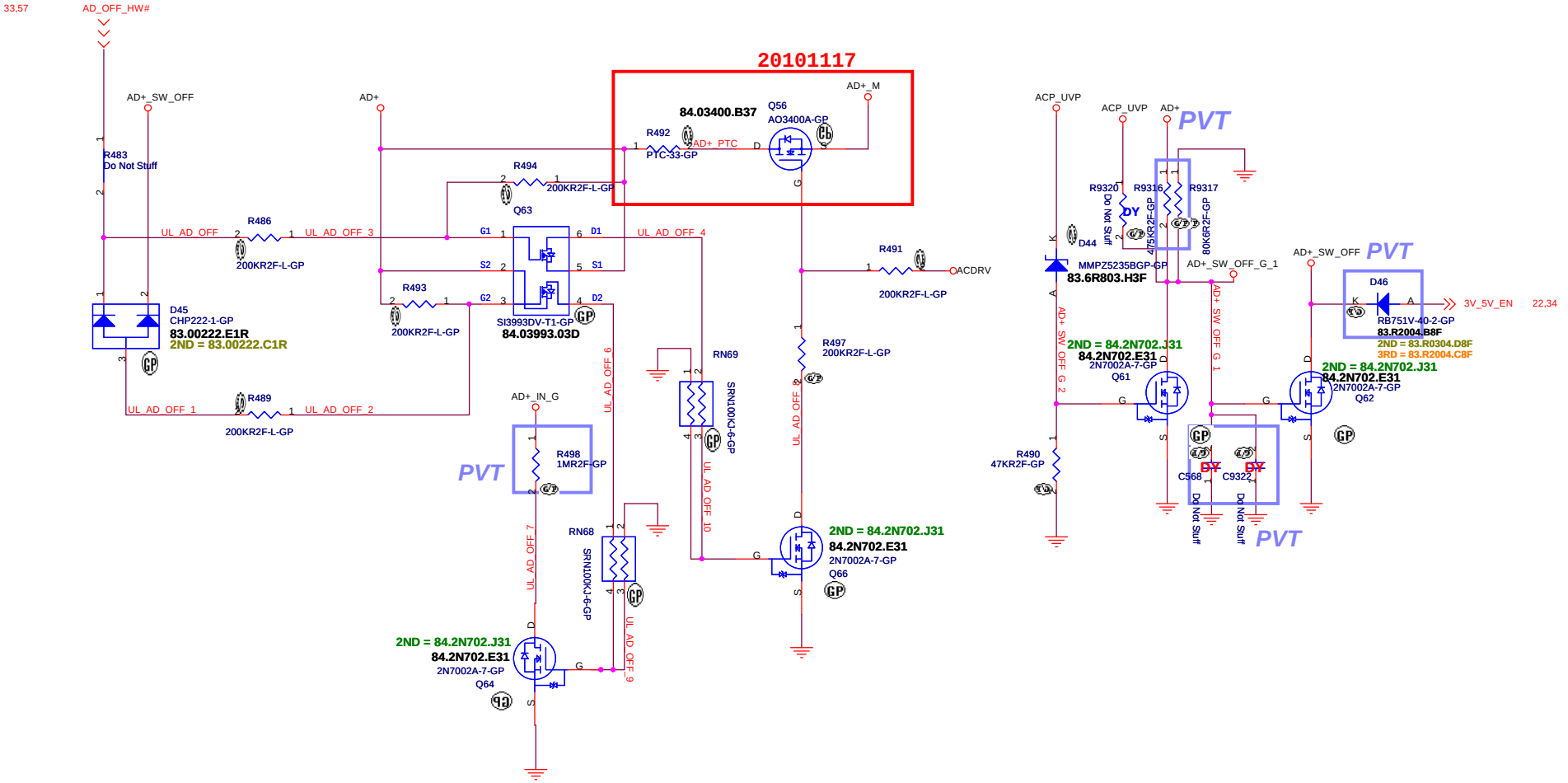
Date: Wednesday, March 02, 2011 Sheet 56 of 74



N12M GS2 HYN1GB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***UL_CIRCUIT***	
Size C	Document Number **Z50-HR { Huron River Platform}**	Rev -1
Date: Friday, March 18, 2011	Sheet 57 of 74	

SSID = UVP Protect Rev :0714

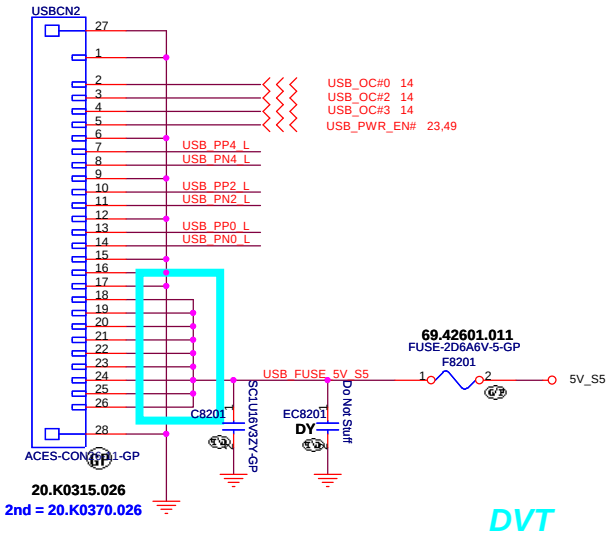


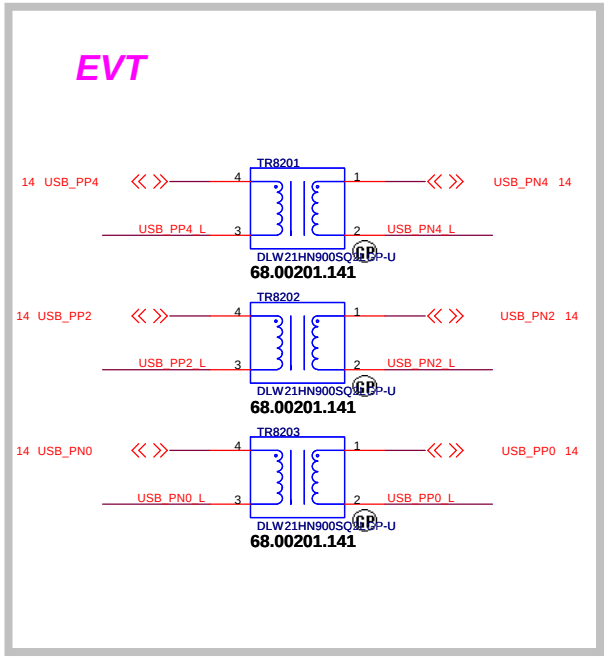
N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

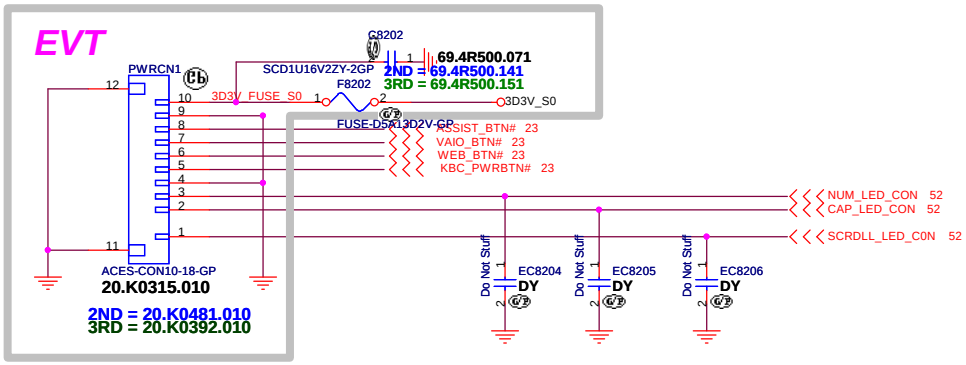
Title: ***UVP***		
Size: A3	Document Number: **Z50-HR { Huron River Platform}**	Rev: -1
Date: Wednesday, March 02, 2011	Sheet 58 of 74	

USB BTB CONN





LED BTB CONN



N12M GS2 HYN1GB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	Z50-HR { Huron River Platform}	-1

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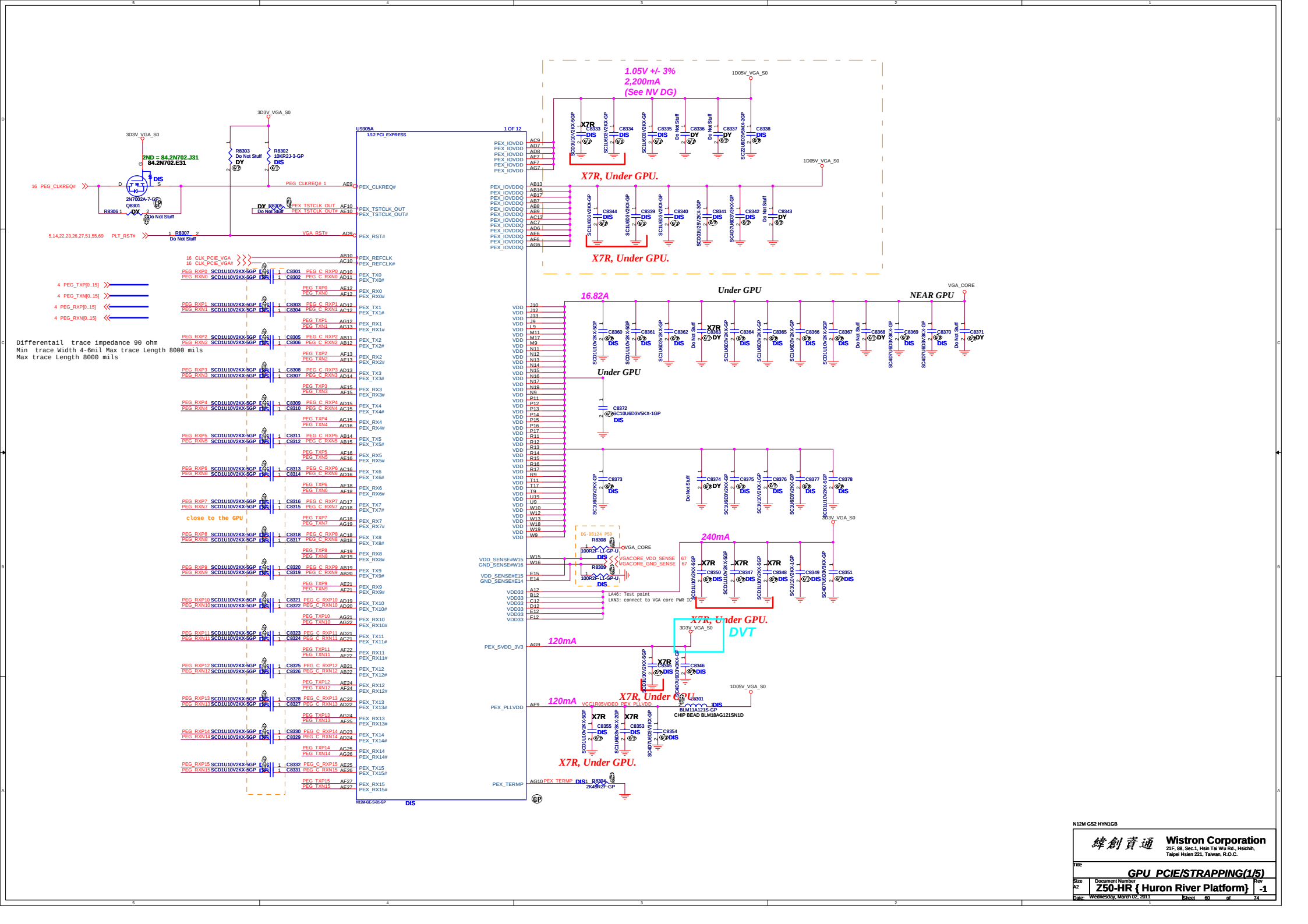
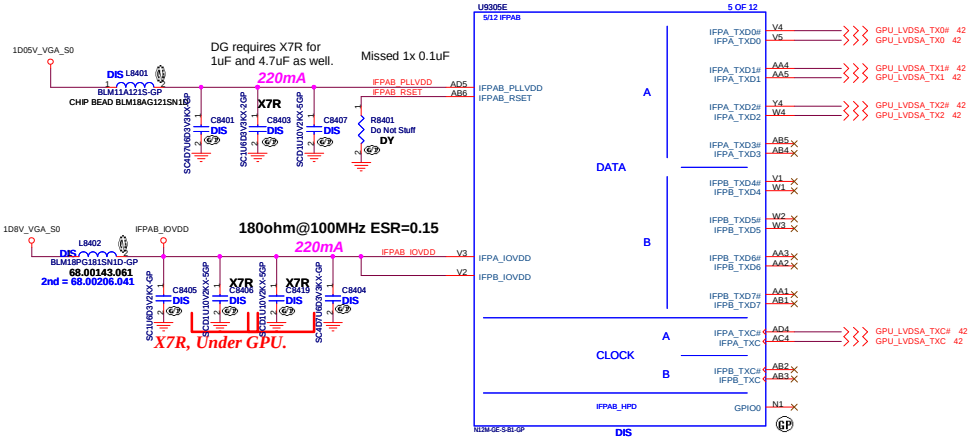
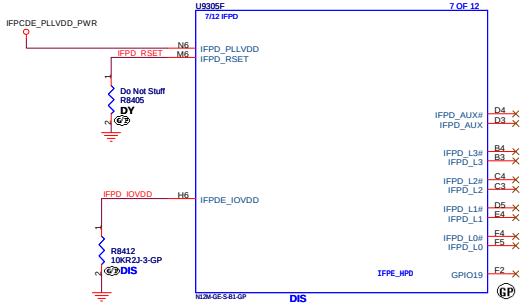
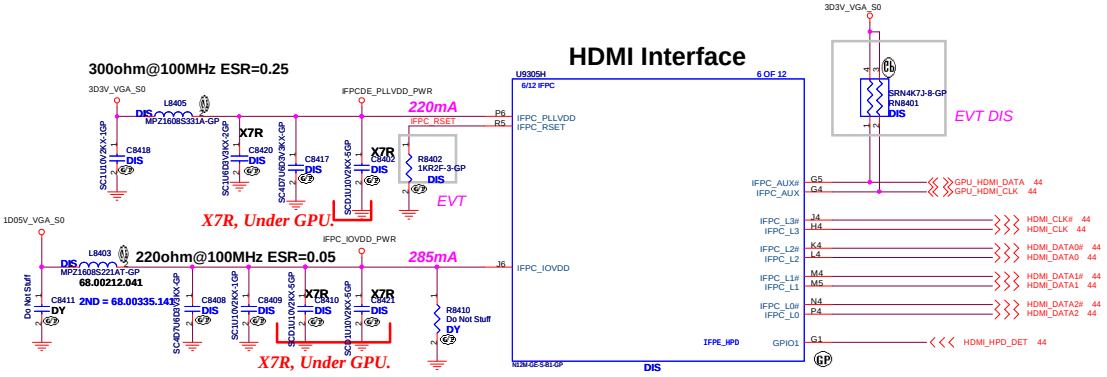

1.05V +/- 3%
2,200mA
(See NV DG)
X7R, Under GPU.
Under GPU
NEAR GPU
16.82A
240mA
120mA
DVT
close to the GPU
Differentail trace impedance 90 ohm
Min trace Width 4-6mil Max trace Length 8000 mils
Max trace Length 8000 mils
2ND = 84.2N702.J31
84.2N702.E31
U9305A
1/2 PCI_EXPRESS
1 OF 12
N12M-GES-81-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GPU_PCIE/STRAPPING(1/5)
Z50-HR { Huron River Platform}
-1
Wednesday, March 02, 2011
Sheet 60 of 74

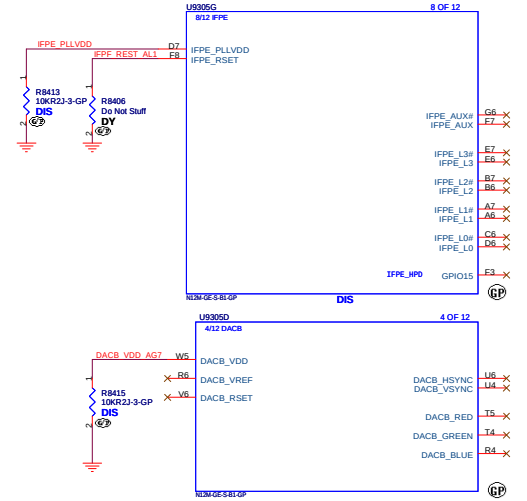
LVDS Interface



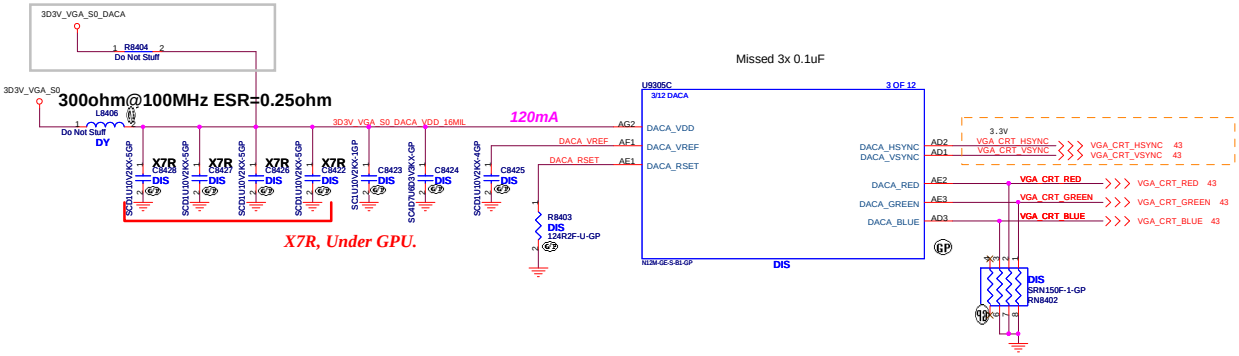


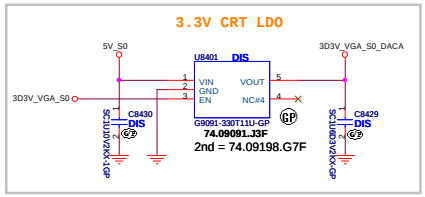
HDMI Interface





I2CA=>CRT, I2CC=>LVDS.





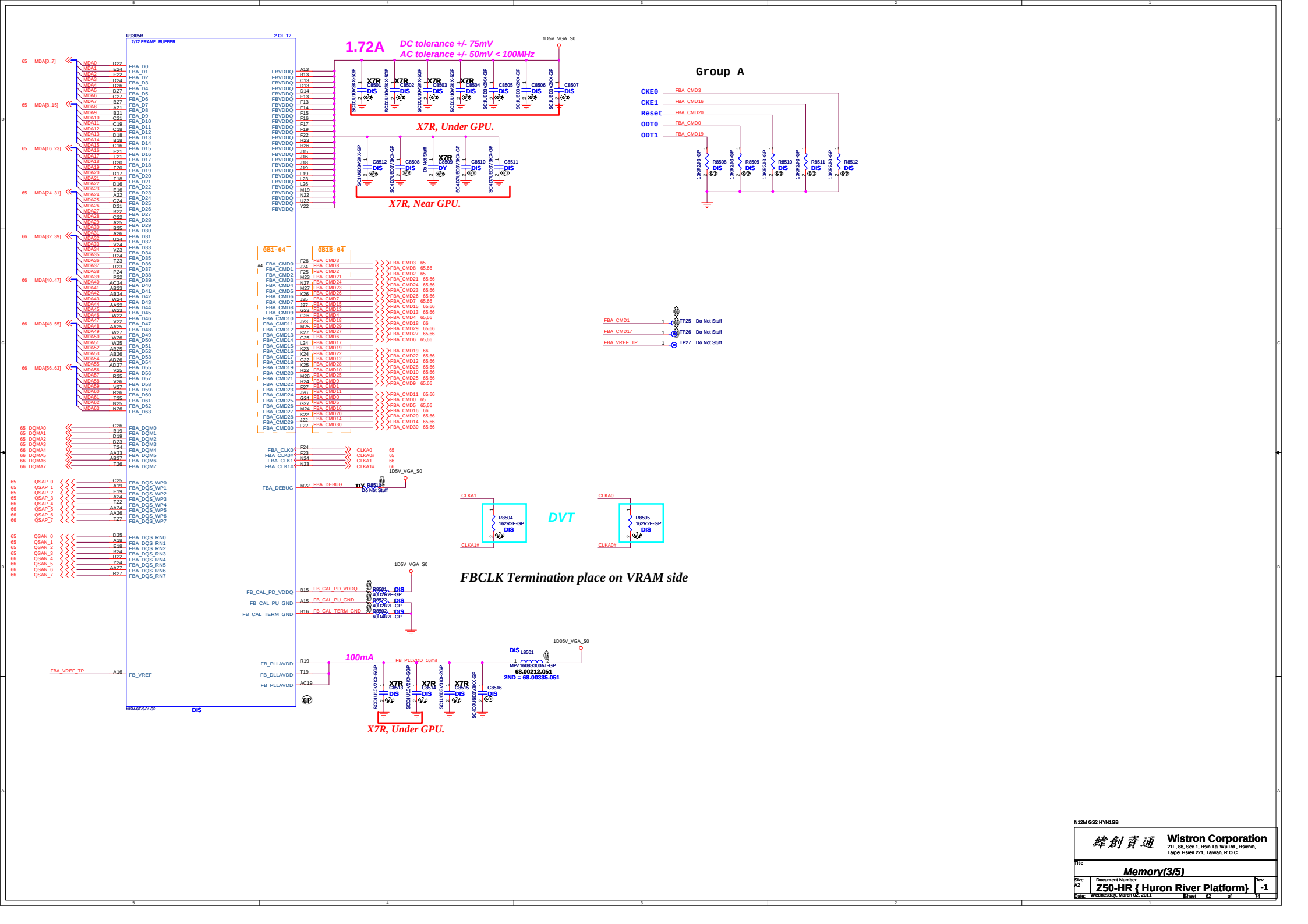
N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU HDMI/LVDS/CRT(2/5)

Size: A2 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

Date: Wednesday, March 02, 2011 | Sheet 61 of 74



N12M GS2 HYN1GB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Memory(3/5)

Size: A2 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

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STRAP0

USER[0]=1
USER[1]=1
USER[2]=1
USER[3]=1

User[3:0]	Type	Resolution	Sync	Notes
0000	XGA	1024 x 768	-/-	
0001	XGA	1024 x 768	+/+	
0010	SXGA	1280 x 1024	-/+	
0011	SXGA+	1400 x 1050	-/-	
0100	UXGA	1600 x 1200	+/+	
0101	QXGA	2048 x 1536	+/+	Reduced Blanking
0110	SXGA+	1400 x 1050	-/-	
0111	SVGA	800 x 600	+/+	
1000 - 1100	-	-	-	Customer defined (Default)[1]
1111	-	-	-	EDID is used

STRAP1

3GIO_PADCFG[0]=0
3GIO_PADCFG[1]=1
3GIO_PADCFG[2]=1
3GIO_PADCFG[3]=0

3GIO_PADCFG[3:0]		Notes
0000-0101	RESERVED	
0110	Notebook	Notebook Default
0111,...1110	RESERVED	
1111	RESERVED	

STRAP2

PCI_DEVID[0]=1
PCI_DEVID[1]=0
PCI_DEVID[2]=0
PCI_DEVID[3]=0

DVT
R8629 STRAP2_N12P-GV need 4.99K pull down
N12M-GS need 25K pull down

N12P-GV->64.49915.6DL,N12M-GS->30025.6DL

Multi-Level Strapping

DVT

20101112

SAM512M->20K,1G->45K;HYN512M->15K,1G->35K

DVT

Resistor Values	Pull-up to VDD	Pull-down to GND
5 kΩ	1000	0000
10 kΩ	1001	0001
15 kΩ	1010	0010
20 kΩ	1011	0011
25 kΩ	1100	0100
30 kΩ	1101	0101
35 kΩ	1110	0110
45 kΩ	1111	0111

HY1G(512MVRAM)
HY2G(16VRAM)

GPU_ROM_SI

for 1Gbit Hynix VRAM	for 2Gbit Hynix VRAM	for 1Gbit Samsung VRAM	for 2Gbit Samsung VRAM
RAM_CFG[0]=0	RAM_CFG[0]=0	RAM_CFG[0]=1	RAM_CFG[0]=1
RAM_CFG[1]=1	RAM_CFG[1]=1	RAM_CFG[1]=1	RAM_CFG[1]=1
RAM_CFG[2]=0	RAM_CFG[2]=1	RAM_CFG[2]=0	RAM_CFG[2]=1
RAM_CFG[3]=0	RAM_CFG[3]=0	RAM_CFG[3]=0	RAM_CFG[3]=0

GPU_ROM_SO

VGA_DEVICE =1 (low bit)
SMB_ALT_ADDR =0
FB_0_BAR_SIZE =0
XCLK_417 =0 (High bit)

GPU_ROM_SCLK

PEX_PLL_EN_TERM =0
SLOT_CLK_CFG =1
SUB_VENDOR =0
PCI_DEVID[4] =1

it's the last bit of F from 0x0DF1

VIDEO MEMORY TABLE

	HYNIX 128Mx16 0110	SAMSUNG 128Mx16 0111	HYNIX 64Mx16 0010	Samsung 64Mx16 0011
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

NVIDIA TABLE

	N12P-Q1 ES DEV ID: 0x0DFE	N12P-Q1 QS DEV ID: 0x0DFA	N12P-Q3 DEV ID: 0x0DDA
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	15Kohm 64.15025.6DL

Physical Strapping Pin	GPU Package	Power Rail	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	GB1-64	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
	GB1b-64		PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	GB1-64	VDD33	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
	GB1b-64		RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	GB1-64	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
	GB1b-64		FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	GB1-64	VDD33	USER[3]	USER[2]	USER[1]	USER[0]
	GB1b-64		USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	GB1-64	VDD33	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
	GB1b-64		3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	GB1-64	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	GB1b-64		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	GB1b-64	VDD33	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	GB1b-64	VDD33	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

Mode	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND	Strapping Resistor for other STRAP pins
Binary Production Strapping	40.2 kΩ, 1% to GND	NC	10 kΩ, 5%
Multi-level Strapping	40.2 kΩ, 1% to GND	40.2 kΩ, 1% to GND	Refer to section12.1

GPIO TABLE

GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	NVGEM_HOTPLUG_DETECT
GPIO1	IN	N/A	IFPC_HOTPLUG_DETECT(HDMI)
GPIO2	OUT	HIGH	PANEL BACKLIGHT PWM
GPIO3	OUT	HIGH	PANEL POWER ENABLE
GPIO4	OUT	HIGH	PANEL BACKLIGHT ENABLE
GPIO5	OUT	HIGH	NVVDD ALV0(GPU VID0)
GPIO6	OUT	HIGH	NVVDD ALV1(GPU VID1)
GPIO7	OUT	HIGH	FBVDD VID0(GPU VID2)
GPIO8	IN/OUT	LOW	OVERTEMP(Thermal Catastrophic Overtemp)
GPIO9	OUT	LOW	ALERT(Thermal Alert)
GPIO10	OUT	HIGH	Memory VREF switch
GPIO11	IN	HIGH	NOT USED
GPIO12	IN	N/A	AC_DETECT
GPIO13	OUT	LOW	Load STEP DOWN
GPIO14	OUT	HIGH	Load STEP UP
GPIO15	IN	N/A	IFPE_HOTPLUG DETECT
GPIO16	OUT	HIGH	FAN_PWM_OUT
GPIO17	IN	N/A	FAN_TACH_IN
GPIO18	OUT	HIGH	SRVC_HDR
GPIO19	IN	N/A	IFPD_HOTPLUG DETECT
GPIO20	OUT	LOW	3D Vision
GPIO21	IN	N/A	Reserved

HARMORY 27MHz
12P 30PPM
HSX530G

N12M GS2 HYN1GB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_GPIO/MIC(4/5)

Size: A2 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

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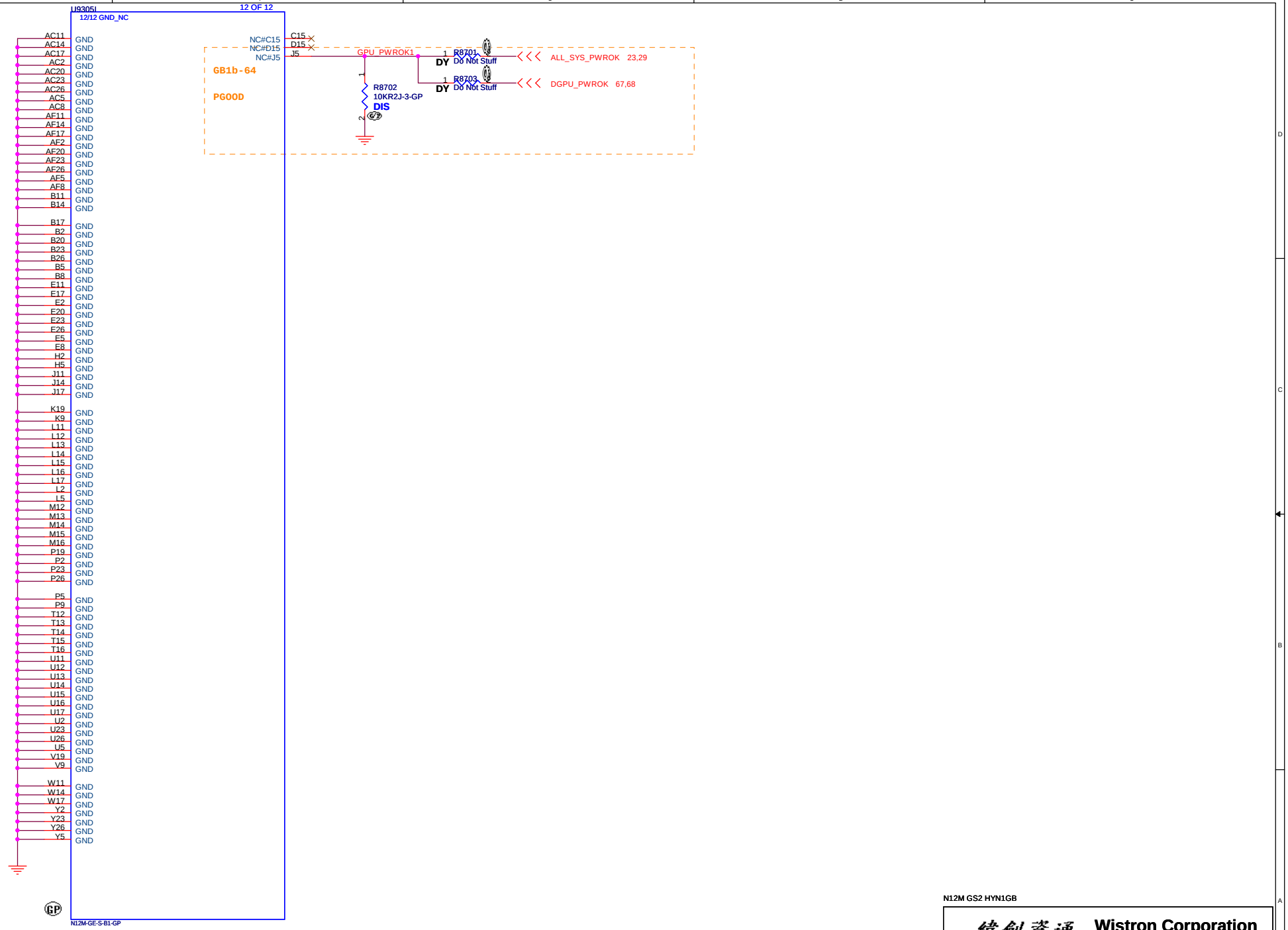

N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU_GND(5/5)***

Size	Document Number	Rev
A3	**Z50-HR { Huron River Platform}**	-1

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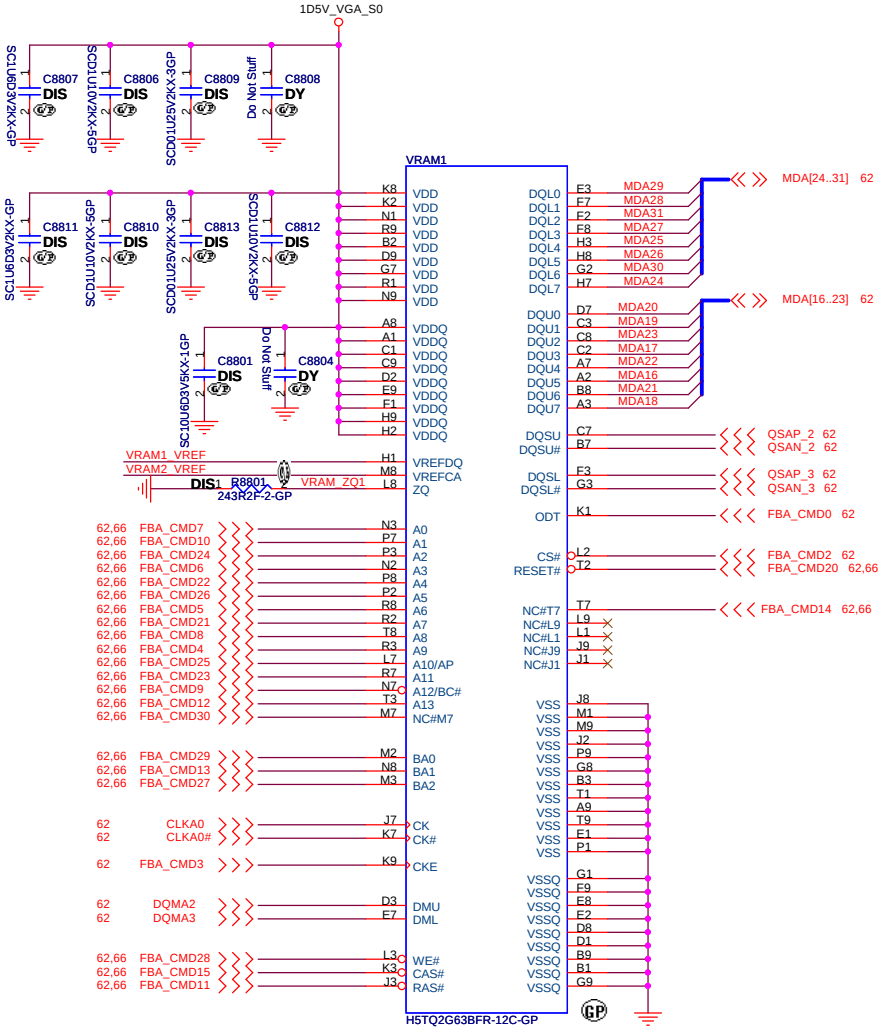
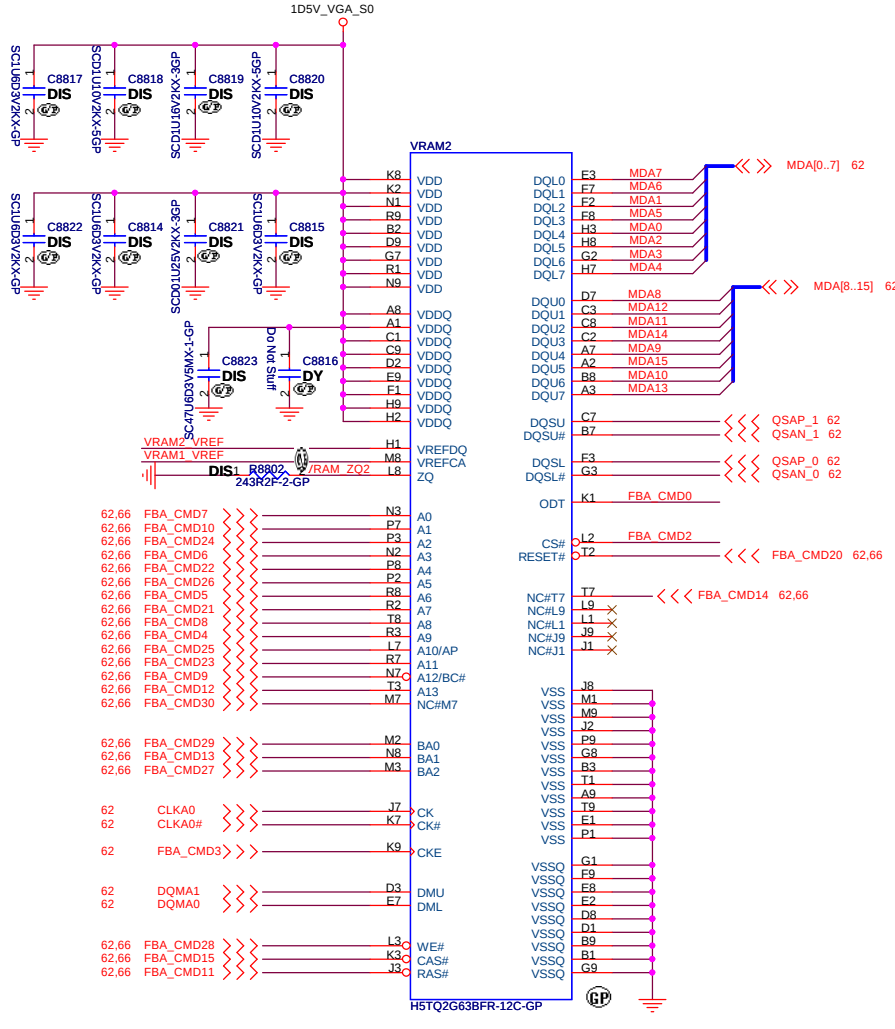


VRAM

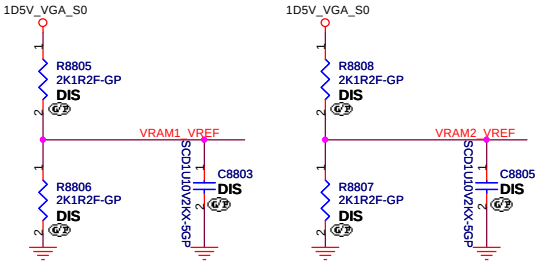
72.52G63.A0U



VRAM

72.52G63.A0U

72.41646.Q0U	K4W1G1646G-BC11	Samsung 1Gb
72.42164.D0U	K4W2G1646C-HC11	Samsung 2Gb
72.51G63.H0U	H5TQ1G63DFR-11C	Hynix 1Gb
72.52G63.A0U	H5TQ2G63BFR-11C	Hynix 2Gb



N12M GS2 HYN1GB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM1,2 (1/2)***

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

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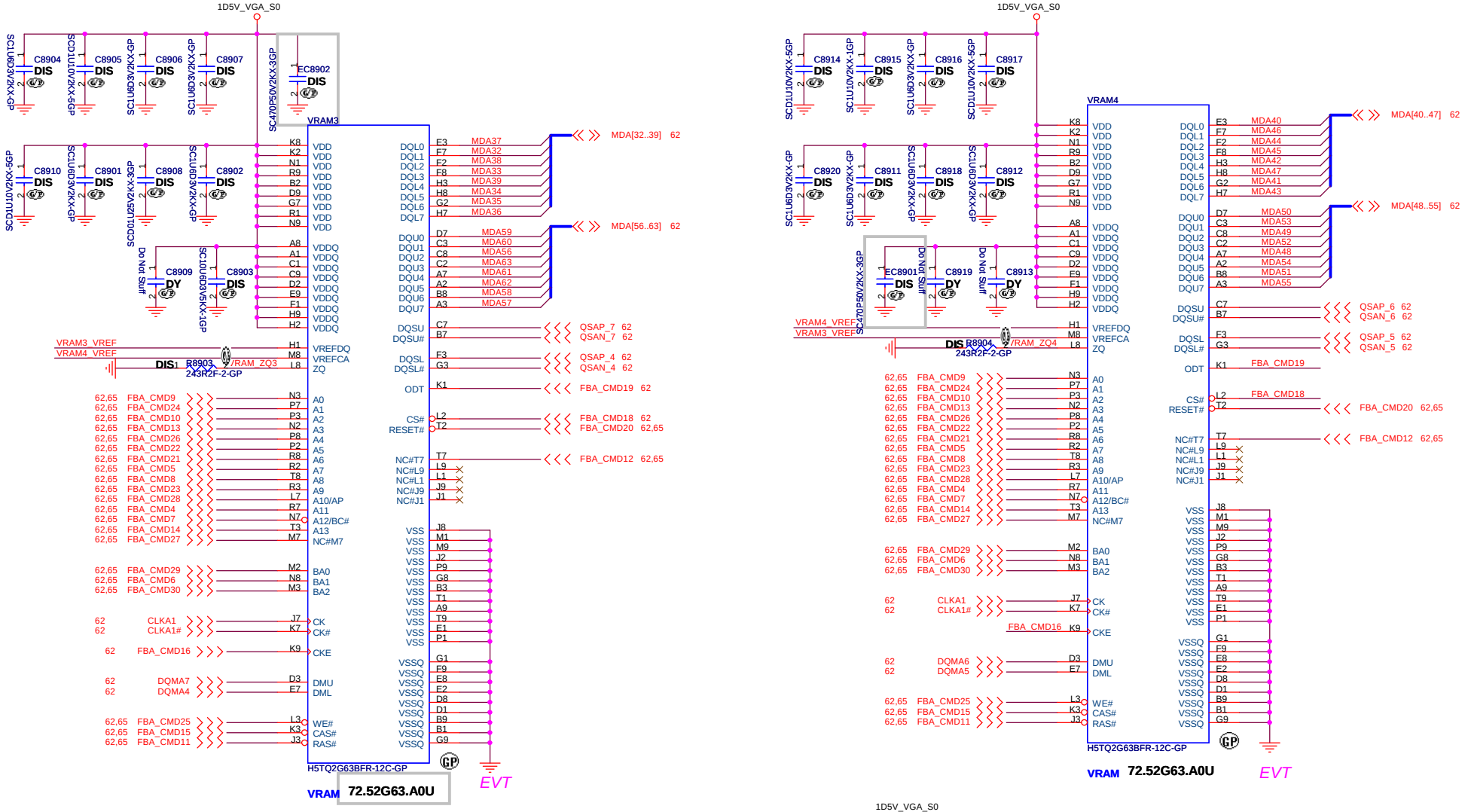

72.41646.Q0U	K4W1G1646G-BC11	Samsung 1Gb
72.42164.D0U	K4W2G1646C-HC11	Samsung 2Gb
72.51G63.H0U	H5TQ1G63DFR-11C	Hynix 1Gb
72.52G63.A0U	H5TQ2G63BFR-11C	Hynix 2Gb

N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/2)

Size: A3 | Document Number: Z50-HR { Huron River Platform} | Rev: -1

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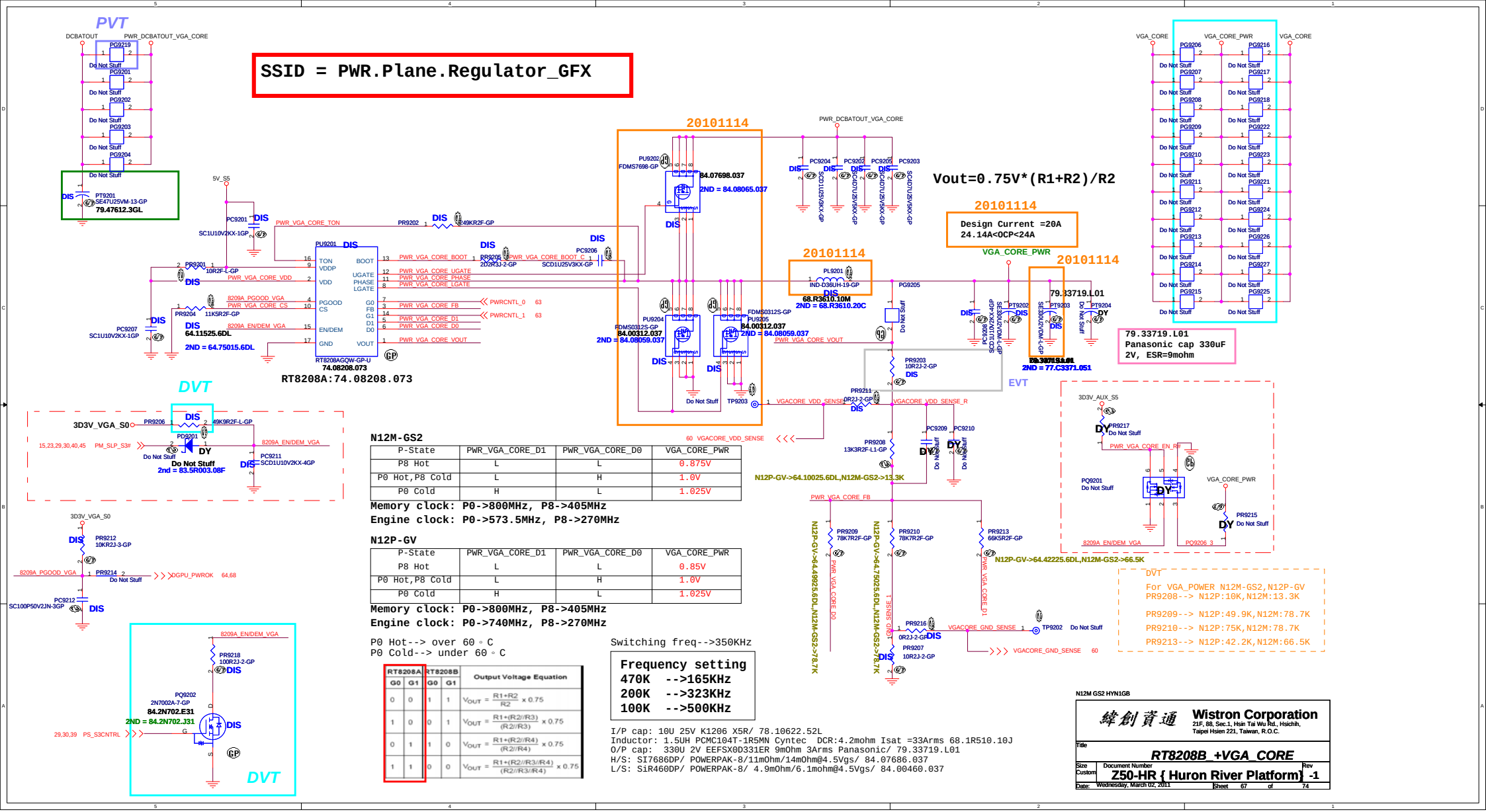
PVT
SSID = PWR.Plane.Regulator_GFX
Vout=0.75V*(R1+R2)/R2
20101114
Design Current =20A
24.14A<OCP<24A
VGA_CORE_PWR
79.33719.L01
Panasonic cap 330uF
2V, ESR=9mohm
RT8208A:74.08208.073
DVT
EVT
N12M-GS2
P-State | PWR_VGA_CORE_D1 | PWR_VGA_CORE_D0 | VGA_CORE_PWR
P8 Hot | L | L | 0.875V
P0 Hot,P8 Cold | L | H | 1.0V
P0 Cold | H | L | 1.025V
Memory clock: P0->800MHz, P8->405MHz
Engine clock: P0->573.5MHz, P8->270MHz
N12P-GV
P-State | PWR_VGA_CORE_D1 | PWR_VGA_CORE_D0 | VGA_CORE_PWR
P8 Hot | L | L | 0.85V
P0 Hot,P8 Cold | L | H | 1.0V
P0 Cold | H | L | 1.025V
Memory clock: P0->800MHz, P8->405MHz
Engine clock: P0->740MHz, P8->270MHz
P0 Hot--> over 60 ◦ C
P0 Cold--> under 60 ◦ C
Switching freq-->350KHz
Frequency setting
470K --> 165KHz
200K --> 323KHz
100K --> 500KHz
RT8208A | RT8208B | Output Voltage Equation
G0 G1 | G0 G1
0 0 | 1 1 | VOUT = (R1+R2)/R2 x 0.75
1 0 | 0 1 | VOUT = (R1+(R2//R3)/(R2//R3)) x 0.75
0 1 | 1 0 | VOUT = (R1+(R2//R4)/(R2//R4)) x 0.75
1 1 | 0 0 | VOUT = (R1+(R2//R3//R4)/(R2//R3//R4)) x 0.75
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
DVT
For VGA_POWER N12M-GS2,N12P-GV
PR9208--> N12P:10K,N12M:13.3K
PR9209--> N12P:49.9K,N12M:78.7K
PR9210--> N12P:75K,N12M:78.7K
PR9213--> N12P:42.2K,N12M:66.5K
N12M GS2 HYN1GB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8208B_+VGA_CORE
Size Custom
Document Number
Z50-HR { Huron River Platform} -1
Rev
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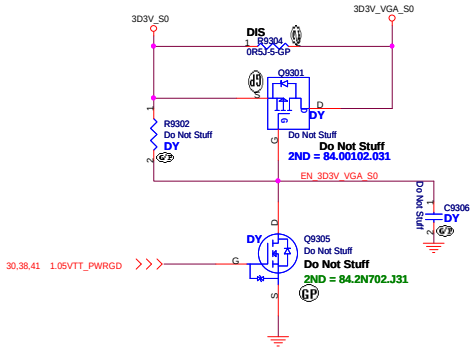
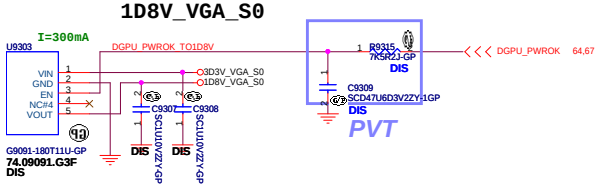
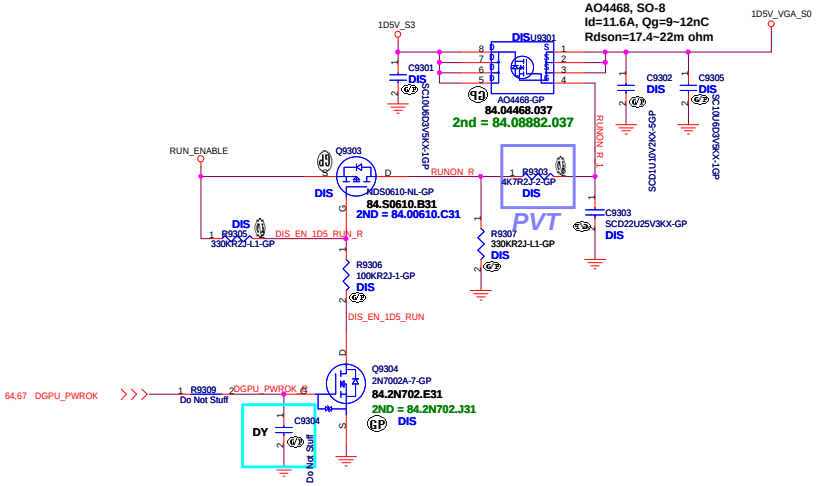
3D3V_VGA_S0



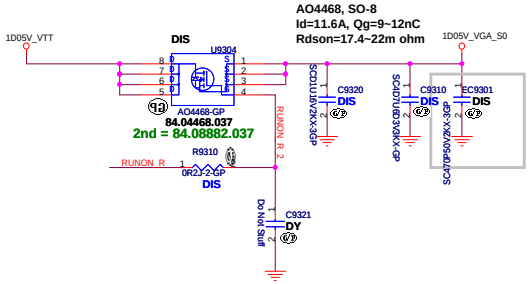
1D8V_VGA_S0



1D5V_VGA_S0



1D05V_VGA_S0



N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DISCRETE VGA POWER**

Size	Document Number	Rev
C	Z50-HR { Huron River Platform}	-1

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H1 Do Not Stuff
H2 Do Not Stuff
H4 Do Not Stuff
H3 Do Not Stuff
H5 Do Not Stuff
H8 Do Not Stuff
H7 Do Not Stuff
H10 Do Not Stuff
H9 Do Not Stuff
H12 Do Not Stuff
H11 Do Not Stuff
H13 Do Not Stuff
H15 Do Not Stuff
H17 Do Not Stuff

TPSPR1
SPRING-57-GP
34.42T14.002

SPR1
Do Not Stuff
DY
Do Not Stuff

PVT

GPU Thermal module hole
HGPU1 STF237R128H42-1-GP
HGPU2 STF237R128H42-1-GP

stand off
HMIN1 STF256R117H119-GP
HMIN2 STF256R117H119-GP
DVT

HPCH1 STF237R128H42-1-GP
HPCH2 STF237R128H42-1-GP
34.4GD01.001
34.4GD01.001

DCBATOUT
EC9701 EC9702 EC9703 EC9704 EC9705 EC9706 EC9707
EC9715 EC9716 EC9717 EC9718 EC9719 EC9720
SCD1U25V2KX-GP

DCBATOUT
EC9722 EC9723 EC9725 EC9726
SCD1U25V2KX-GP

DCBATOUT
EC9728
SCD1U25V2KX-GP

1D5V_S3
EC9733 EC9734 EC9735 EC9736 EC9737
SCD1U25V2KX-GP

1D5V_S3
EC9738 EC9739 EC9740
SCD1U25V2KX-GP

DVT

-1M

DCBATOUT
TC9702 TC9705 DIS TC9707
SE47U25VM-13-GP
79.47612.3GL 79.47612.3GL
DY Do Not Stuff
Do Not Stuff

DVT

TPAD1 Do Not Stuff
TPAD2 Do Not Stuff
TPAD3 Do Not Stuff
Do Not Stuff Do Not Stuff Do Not Stuff
CPU Thermal module hole

change footprint

1D05V_VTT
EC9729 EC9730 EC9731 EC9732
DY Do Not Stuff

VCC_GFXCORE
EC9711 EC9712
DY Do Not Stuff

VCC_CORE
EC9713 EC9714
DY Do Not Stuff

Check test point

3D3V_S0 AFTP1
3D3V_AUX_S5 AFTP7
3D3V_S5 AFTP8
5V_S5 AFTP9
15,23 PM_PWRBTN# AFTP10
5,18 H_CPUPWRGD AFTP11
22,23 S5_ENABLE AFTP12
5,14,22,23,26,27,51,55,60 PLT_RST# AFTP13

N12M GS2 HYN1GB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: Z50-HR { Huron River Platform}
Rev: -1
Date: Wednesday, March 02, 2011
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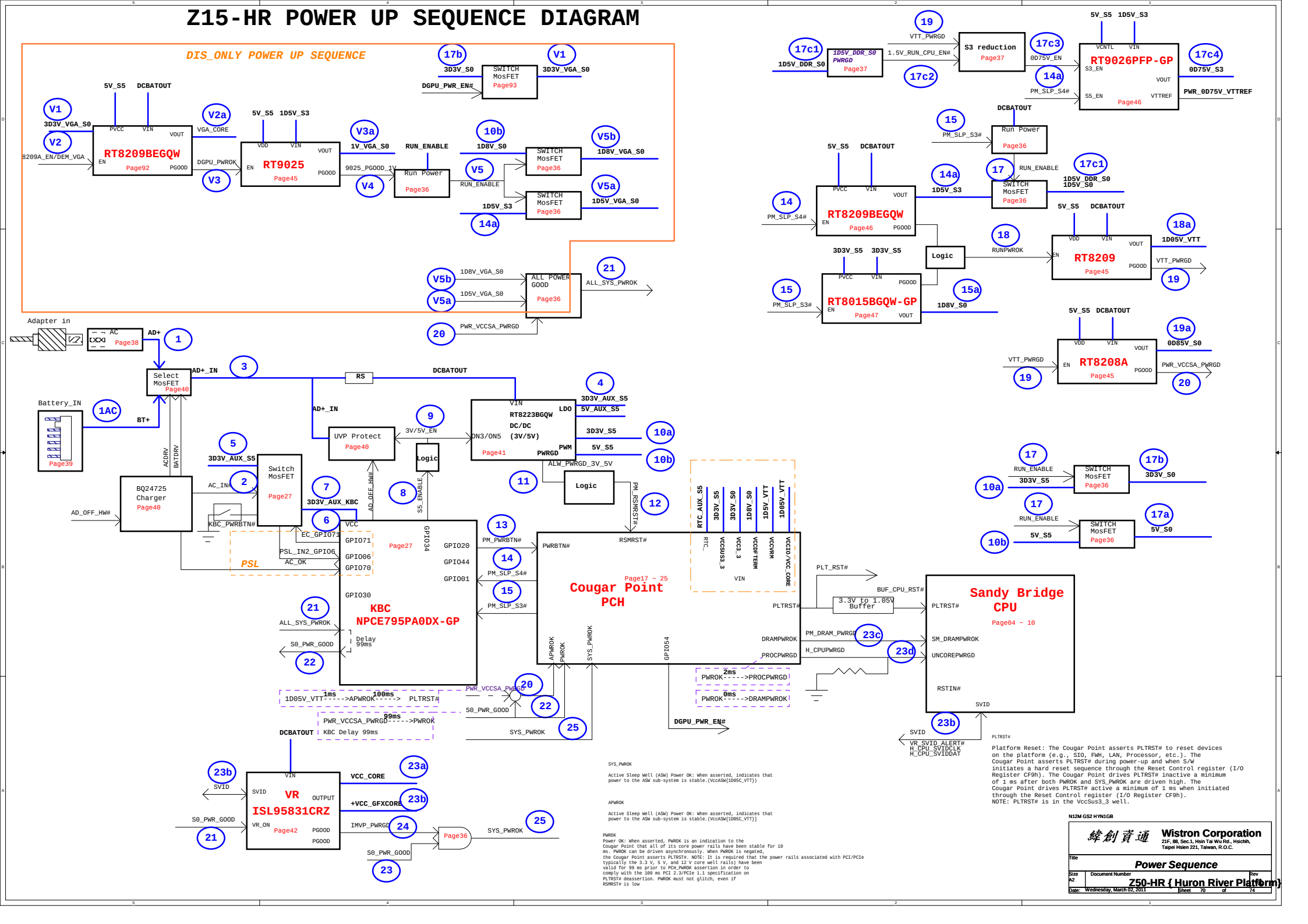
Z15-HR POWER UP SEQUENCE DIAGRAM



SYS_PWROK

Active Sleep Well (ASW) Power OK: When asserted, indicates that power to the ASW sub-system is stable.(VccASW[1D05C_VTT])

APWROK

Active Sleep Well (ASW) Power OK: When asserted, indicates that power to the ASW sub-system is stable.(VccASW[1D05C_VTT])

PWROK

Power OK: When asserted, PWROK is an indication to the Cougar Point that all of its core power rails have been stable for 10 ms. PWROK can be driven asynchronously. When PWROK is negated, the Cougar Point asserts PLTRST#. NOTE: It is required that the power rails associated with PCI/PCIe typically the 3.3 V, 5 V, and 12 V core well rails) have been valid for 99 ms prior to PCH_PWROK assertion in order to comply with the 100 ms PCI 2.3/PCIe 1.1 specification on PLTRST# deassertion. PWROK must not glitch, even if RSMRST# is low

PLTRST#

Platform Reset: The Cougar Point asserts PLTRST# to reset devices on the platform (e.g., SIO, FWH, LAN, Processor, etc.). The Cougar Point asserts PLTRST# during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O Register CF9h). The Cougar Point drives PLTRST# inactive a minimum of 1 ms after both PWROK and SYS_PWROK are driven high. The Cougar Point drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O Register CF9h).
NOTE: PLTRST# is in the VccSus3_3 well.

N12M GS2 HYN1GB

緯創資通 Wistron Corporation
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Title: Power Sequence

Size: A2 | Document Number: Z50-HR { Huron River Platform} | Rev: 0

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Reversion History

EVT

(2010/09/28)

P.5 CPU (THERMAL/CLOCK/PM)	DUMMY RN501 pull high 1D05V_VTT for intel bebug use
P.7 CPU (RESERVED)	Delete R706~R709 for no M3 function
P.9 CPU (VCC_GFXCORE)	Delete R904,R905,R901 , because R902 has pull low
P.13 PCH (LVDS/CRT/DDI)	Delete LVBS B channel for Z70
P.14 PCH (PCI/USB/NVRAM)	Reserved EC1803 for EMI
P.15 PCH (DM I/FDI/PM)	1.DUMMY R1922 ,internal already pull high,2 Del R1925 for intel debug.
P.16 PCH (PCI-E/SMBUS/CLOCK/CL)	1.Delete RN2017 for no display port,2 R2005 dummy, R2004 mount for PEG_CLKREQ# need pull high
P.17 PCH (SPI/RTC/LPC/SATA/IHDA)	DEL R2115~R2120,for intel JTAG no use
P.18 PCH (GPIO/CPU)	Add PCH_GPIO22 for VRAM Frequency 800MHZ ro 900MHZ
P.22 KBC_Reset	Add VEDS_VEVS_Thermal_System_Protection_Rev1.0.0
P.23 KBC Nuvoton NPCE795	1.ADD GPIO:FAN_PROTECT_DISABLE#, 2.ADD MODEL_ID for Z40,Z50 model, 3.ADD R2757 for vendor suggest , 4.R2724 CHANGE TO 20K for SB Ver. 5.ADD BT_PRS2# for BT present.
P.24 Thermal P2800	1.CHANGE FAN PIN DEFINE,2.MOUNT D2802 for Vbemf(back emf), 3.U2802~U2806 pin4 connector to pin5 pull high follow Thermal_System_Protection_Rev1.0.0
P.21 Audio Codec_CX20671-21Z	CHANGE Codec to CX20671
P.22 Atheros 8151	CHANGE LAN to Atheros 8151
P.27 RTS5209 (CARD READER)	DUMMY R3202 for use external EEPROM
P.28 Audio DE-POP Circuit	Add Q3301,R333 for CODEC multi-function
P.29 Power Plane Enable	Change r3626 to 20k for 3D3V_S3 Leakage
P.30 S3 reduction	1.Del R577 for double pull low,2.Change Q3708_G net to PM_SLP_S3# for Sequence 3.DUMMY R3724 mount Q3712,R3726,R3722,R3723,Q3707,C3706 for 0D75_EN timing.
P.32 BATT CONN	1.ADD D3906 for battery Protection,2.MOUNT D3901~D3905 for EMI
P.34 CPU Core-1(ISL95831)	1.ADD PR4231,PC4233,PR4236,PC4234,MOUNT PR4221,PR4222,PR4420 ,Intel spec update for feedback compensate. 2.mount PR4221,PR4222,PR4420,PR4233~PR4235 for sensor MOS temperature.
P.42 [LCD Connector]	Change LCD1 to 30pin and pin define
P.42 [LCD Connector]	Add TR4901 for EMI
P.44 [HDMI Level Shifter/Conn]	F5101 change to 69.4R500.151 POLYSWITCH
P.45 [HDD/ODD]	Change R5601 to 147K for delay timing
P.46 [Audio Jack]	Add SPKR1 small board move to MB
P.46 [Audio Jack]	R5808 and R5809 change to 3.0K for Conexant FAE suggestion
P.47 [LAN Connector]	XF1 change to 68.89246.301 common part
P.51 [MINICARD]	Add WLAN/BT COMBO function
P.52 [LED Board/Power Button]	1.PWRLED1 change to 83.00195.N70 for green color
P.52 [LED Board/Power Button]	Add WLAN/BT COMBO LED signal pin
P.52 [LED Board/Power Button]	Delete Q86 and Q85 for function board no PWR/STDBY LED
P.52 [Key Board/Touch Pad]	Add EC6905 and EC6906 for EMI
P.55 [Debug connector]	Add DB1 for SW debug
P.58 [UVP Protect]	Change net from UL_AD_OFF_4 to UL_AD_OFF_41 net name wrong
P.58 [UVP Protect]	RN67 separate to R7816 1Mohm and R7817 80Kohm for change shutdown voltage detect
P.58 [UVP Protect]	Add C7801 10UF/25V for change shutdown voltage detect
P.59 [IO Board Connector]	USBCN2 change to 26pin for USB board add G709 thermal sensor
P.59 [IO Board Connector]	Add F8201, F8202 and F8203 POLYSWITCH for comtmer request
P.59 [IO Board Connector]	Add TR8201, TR8202 and TR8203 for EMI
P.59 [IO Board Connector]	PWRCN1 change to 10pin for function board no SPKR1 and PWR/STDBY LED
P.61 [GPU HDMI/LVDS/CRT(2/5)]	Add LDO 3D3V_VGA_S0_DACA power for INCREASE POWER
P.61 [GPU HDMI/LVDS/CRT(2/5)]	Mount R8402 BOM error becouse HDMI no display
P.63 [GPU_GPIO/MIC(4/5)]	R8630 change to 45K for N12P-GV Device ID 0x107F
P.63 [GPU_GPIO/MIC(4/5)]	R8627 change to 45K for Samsung VRAM 2Gbit size
P.67 [RT8208B_+VGA_CORE]	Add PU9205 low-side mosfet for N12P-GV NVVDD 20.02A
P.69 [UNUSED PARTS/EMI Capacitors]	Add TPSPR1 for EMI
P.69 [UNUSED PARTS/EMI Capacitors]	Mount EC9740 for EMI

(2010/09/29)

P.15 PCH (DMI/FDI/PM)	Add U1901, D1901, D1902, C1901, R1929~R1931 for RSMRST#, PWROK must be "Low" earlier than PCH power down.
P.22 KBC_Reset	D2603 change to 83.R5003.C8F
P.60 [RTC Connector]	D6001 change to 83.BAS70.011 for customer request
P.11(DDR3-SODIMM1)	Del R1401 for use DDR_VREF_S3 POWER
P.12 (DDR3-SODIMM2)	Del R1501 for use DDR_VREF_S3 POWER
P.31 DCIN JACK	Change D3801(TVS) for surge voltage

(2010/09/30)

P.29 Power Plane Enable	Add D3603 for protect FET AO4468
P.25 Audio Codec_CX20671-21Z	Add C2905, C2925 and R2923(DY), R2924(DY) for vendor request
P.67 [RT8208B_+VGA_CORE]	PR9203 change to 10R, PR9208 change to 15K for VGA_CORE keep 0.9V
P.68 [DISCRETE VGA POWER]	R9302 change to 20K for 1D05V_VTT enbale timing

(2010/10/01)

P.20 [PCH (POWER2)]	D2401, D2402 change to 83.R2004.B8F for common part
P.22 [KBC_Reset]	Q2602 change to 84.02222.V11, Q2601 change to 84.C3906.A11 for common part
P.24 Thermal P8200	Q2801 change to 84.03904.X11 for common part
P.25 Audio Codec_CX20671-21Z	D2901, D2902 change to 83.R2004.B8F for common part
P.28 Audio DE-POP Circuit	Q19 change to 84.C3906.A11, Q20 change to 84.03904.X11 Q18 change to 84.09114.A11, Q25 change to 84.C3906.A11 for common part
P.30 S3 reduction	Q3707 change to 84.03904.X11, U3702 change to 73.01G09.0AB for common part
P.32 BATT CONN	D3908 change to 83.00016.F11 for common part
P.48 Flash(KBC+PCH)	U6001 change to 72.25320.C01 for common part
P.50 BLUETOOTH	U6301 change to 74.07534.A7F, U6302 change to 73.01G08.EHG for common part
P.63 [GPU_GPIO/MIC(4/5)]	X8601 change to 82.30034.641 for common part

(2010/10/04)

P.15 PCH (DMI/FDI/PM)	Mount R1920, GPIO pin need to Pull Hi for PCH GPIO multi-function
P.27 RTS5209 (CARD READER)	Add R3209~R3211,C3212~C3214 for customer request
P.29 Power Plane Enable	D3604 change to schottky for customer request
P.33 CHARGER BQ24725	PD4002 change to 83.10004.08M for common part
P.51 [MINICARD]	Change R6505 to 0805 size for meet PCIE MINI card max power spec
P.30 S3 reduction	Mount R3704,Q3702 for Huron River S3 reduction Desing Guide

(2010/10/05)

P.7 CPU (RESERVED)	ADD corner test point for CPU
P.18 PCH (GPIO/CPU)	ADD corner test point for PCH
P.33 CHARGER BQ24725	ADD PU4006,PR4017,PR4018,PQ4001
P.57 [UVP Protect]	ADD PU4006,PR4017,PR4018,PQ4001
P.58 [UVP Protect]	(Q56 pin D connect to AD+) (R9316 pin 1 connect to AD+) add R9320 and DUMMY it. (Part number 64.10045.6DL) connect R9320 pin 1 to ACP_UVP. change C568 to the part number 78.10620.51L add C9322 component (part number 78.10620.51L)
P.44 [HDMI Level Shifter/Conn]	HDMI CONN pin17 connect to GND
P.67 [RT8208B_+VGA_CORE]	PR9208 change to 17.8k
P.63 [GPU_GPIO/MIC(4/5)]	P8603 change to 15k
P.63 [GPU_GPIO/MIC(4/5)]	R8617 DUMMY, R8625 PU 10K for vendor suggest

(2010/10/07)

P.49 USB Power SW	Add F6101 POLYSWISH 2A for USB power
P.17 PCH /P.24	Change net name from "+3VS_+1.5VS_HDA_IO" to "+3VS_HDA_IO"
P.44 [HDMI Level Shifter/Conn]	Del HDMI Level Shifter

(2010/10/14)

P.18 PCH (GPIO/CPU)	R2204 BOM change to 390ohm for intel spec

N12M GS2 HYN1GB

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Reversion History

DVT

(2010/11/16~2010/11/17)

P17--C2101, C2102 change to 6pF
Reason: Crystal vendor suggestion (32.768K)
Possible Risk: Rework OK

P17--Add R2126 ~ R2130 and C2105~C2110.
Reason: Reserver for LPC debug by EC VEVS
Possible Risk:

P18--DUMMY R2204
Reason: For customer request THERMTRIP# Shutdown Policy
Possible Risk: Rework OK

P22--R2604 stuff to IMVP_PWRGD, Q2602 change to 2N7002
Reason: For customer request THERMTRIP# Shutdown Policy
Possible Risk: Rework OK

P23--BT_PRS# add R2729 pull-up to 3D3V_S5
Reason: The VEVS request BT_PRS# signal be high when Module is not present so we add it.
Possible Risk:We already rework to finish BT VEVS report.

P23-- R2724 change to 33K
Reason: For SC version
Possible Risk:

P23--PCH_SML1_CLK,PCH_SML1_DATA Change power source to 3D3V_S5
Reason: If PH 3D3V_AUX_S5. When DC mode will cause leakage Problem
Possible Risk: Rework OK.

P24-- Add C2803=0.1uF
Reason: 5V has drop when fan power on so add a cap for soft start
Possible Risk: Rework OK.

P25--Stuff EC2901,EC2902
Reason:FOR EMI request
Possible Risk:

P25--DUMMY R2919 ,stuff R2922
Reason: "codec verb table" set mute functio is high active so we change it..
Possible Risk: Rework OK.

P26--DUMMY Q3101 R3104,R3110,ADD R3112,R3111
Reason:LAN_CLK_REQ# and PCIE_WAKE# no leakage on S3.
Possible Risk: Rework OK.

P26--Change C3126, C3127 to 18pF
Reason: Crystal vendor suggestion (25MHz for LAN)
Possible Risk: Rework OK.

P27--Dummy U3202, mount R3202
Reason: Use card reader IC internal EFUSE
Possible Risk: Rework OK

P29--R3626 change to 0ohm
Reason:First we use resistor to do voltage divider for protecting U3601 (let gate voltage < spec) but it is not safty so we add Zener diode D3603 to protect U3601.So Voltage divider do not need.
Possible Risk: Rework OK.

P29--Add Q3606, R3608 (DY)
Reason: Reserve 3D3V_S3 discharge circuit
Possible Risk: Rework OK

P30--DUMMY R3714,Q3704
Reason:When enter S3, DDR_VREF_S3 still have power. So it cannot do discharge when enter S3.
Possible Risk:

P30--DUMMY R3727,Q3713 ,replace PM_SLP_S3 net by PS_S3CNTRL .
Reason:PS_S3CNTRL control S3 discharge can instead of R3612,Q3603
Possible Risk:

P30--R3722 change to 10k,R3723 change to 3.3k,C3706 change to 4.7kohm, stuff C3707.
Reason:for S3 resume issue and sequence timing(ID 0547)
Possible Risk:Rework OK.

P32--add EC3901.EC3907,EC3908,EC3909
Reason:for EMI request
Possible Risk:

P43--R5001, R5002, RN5003 change to 4.7K for DIS SKU
R5001, R5002=2.7K, RN5003=2.2K for UMA SKU
Reason: For CRT DDC signal VEVS report
Possible Risk: Rework OK

P44-- R5133,R5134 change 3.3K for UMA sku, 4.7K for DIS SKU
Reason: For HDMI DDC signal VEVS report
Possible Risk: Rework OK

P45--R5601 change to 100k,R5603 change to 220k,C5614,C5604 change to 1u
Reason:for delay HDD power off timing
Possible Risk:Rework OK

P46--R5805,R5806,R5807,R5810,R5811,R5812 change to 11ohm.
Reason:For VEVS audio full scale output votage(FSOV) report
Possible Risk:Rework OK.

P46--Add EC5804,EC5805,EC5806,EC5807,ED5808,ED5809
Reason:for EMI request (ED is mean diode)
Possible Risk:

P49--Add TR6101
Reason:for EMI request
Possible Risk:Rework OK and USB eye diagram pass.

P56--Add SD DATA, CLK, CMD 47 ohm damping(RN7403,R7401,R7404)
Reason:For cardreader VEVS report overshoot and undershoot
Possible Risk: Rework OK.

P57--RTC_PWR change to RTC_AUX_S5 power
Reason: Unplug AC will auto shut down after Remove RTC battery
Possible Risk: Rework OK

P59--Change USB BD FFC CONN pin define
Reason:del G709 on USB BD then add one usb power and ground pin for USB voltage drop issue. (ID 0583)
Possible Risk:

P62--R8504, R8505 change to 162ohm
Reason: NV FAE suggestion
Possible Risk:

P63--Change GPU GPIO strap pin R8626 to 4.99K, R8619 to 10K, R8629 to 4.99K for N12P-GV, R8629 to 25K for N12M-GS2, Dummy R8630 Dummy R8632, mount R8633=35K
Reason: NV FAE suggestion for GPU HW strap pin
Possible Risk:

P63--R8607 change to 470ohm
Reason: Crystal vendor suggestion (27MHz)
Possible Risk:Rework OK

P63--R8639 change to15K ohm
Reason: Resolve ID 0617 no HDMI audio output
Possible Risk:Rework OK

P67--Change PR9206 to 49.9K; add PR9218,PQ9202 for VGA_CORE discharge circuit.
Reason:For GPU VEVS Sequence Issue (ID 01019)
Possible Risk: Rework ok.

P68--Change R9303 to 0ohm ,R9315 to 2.2K, C9309 to 1uF; Dummy C9304
Reason:For GPU VEVS Sequence Issue (ID 01019)
Possible Risk: Rework ok.

P69--add DCBATOUT and 1D5V_S3 POWER plane capacitance
Reason:For EMI request
Possible Risk:

(2010/11/22)

P18--Delete R2220, R2221
Reason: Only use 900MHz VRAM frequence
Possible Risk: Rework OK

P22--Add Q2610,Q2607,D2606,R2608,R2602,C2602
Reason: For UVP circuit Simplification and Verification by 3V_5V_EN
Possible Risk: Rework OK

P44--add C5103 0.1uF.
Reason: Resolve HDMI DDC/CEC Capacitance fail (Issue ID 1106)
Possible Risk: Rework OK

P69--Add SPR1
Reason: For EMI request
Possible Risk:

(2010/11/24)

P17--Add C2105,C2107 ~ C2110
Reason: Reserver for LPC debug by EC VEVS
Possible Risk:

P19--Add C2324,C2325,L2302,L2303,L2304
Reason: Improve DMI eye diagram
Possible Risk: Under Verify (ZM and ZG-I different)

P48--DelR6004,R6003 change to 1k
Reason: customer request,do not need "RCT_PWR"net
Possible Risk: Rework OK

P60--PEX_SVDD_3V3 power rail from 1.05V change to 3.3V
Reason: NV FAE suggution for N12M-GS2/N12P-GV GPU
Possible Risk:

(2010/11/25)

P9--R906, R907 change to 10ohm
Reason: Customer requirement
Possible Risk:

P24-- Add F2801
Reason: 0.5A POLYSWITCH for FAN by Customer requirement
Possible Risk:

P35--Dummy PR4230, PR4250, PR4228, PR4229
Reason: Customer requirement
Possible Risk:

(2010/11/26)

P32--Change U3901 to R5G05000N753NF
Reason: Battery authentication IC package is shrunk and renamed as R5G05000N753NF.
Possible Risk:

(2010/11/29)

P58--dummy R9320
Reason: customer request
Possible Risk:

P58--R8629 change to 30k for N12M
Reason: N12M GPU change new device ID
Possible Risk:

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(POWER modify)

P8--R801, R802 change to 10ohm, reserve R804, R805=10ohm
Reason: Vendor suggation
Possible Risk:

P33--Add PR4019, PR4020
Reason: Vendor TI suggestion reserve
Possible Risk:

P33--PU4001, PU4002, PU4006 change to 84.02657.037
Reason: Low Rds(on), decrease consumption
Possible Risk:

P34--Change PU4101 PU4106 PU4104 PU4105
Reason: Material shortage issue
Possible Risk:

P34--PR4104 change to 95.3K, PR4103 change to 84.5K
Reason: OCP modify
Possible Risk:

P35--Change PR4205 to 2.26K, PR4227 to 3.74K
Reason: Load line
Possible Risk:

P35--Change PR4206 to 21.5K, PC4205 to 0.01uF, PR4218 to 36K
PC4207 to 0.01uF
Reason: Vendor Intersil suggestion for Imon=2.7V
Possible Risk:

P35--Dummy PC4224, PC4209
Reason: FAE suggestion for delay issue
Possible Risk:

P35--Change PR4239 to 1.69K
Reason: For Intel spec increase efficiency
Possible Risk:

P36--Delete PU4308, PU4311,PU4312, PU4314
change PL4303, PL4302 to 68.R3610.10X
Reason: Thermal issue, use low DCR
Possible Risk:

P36--Change PU4308~ PU4315
Reason: Material shortage issue
Possible Risk:

P37--Change PU4401 to 84.07698.037, PU4403 to 84.00308.B03
PL4401 to 68.R3610.10M
Reason: Material shortage issue
Possible Risk:

P37--Change PR4404 to 536ohm
Reason: OCP modify
Possible Risk:

P37--Change PC4405 TO 10K
Reason: Transient
Possible Risk:

P38--Change PR4504 to 93.1K
Reason: OCP modify
Possible Risk:

P38--Change PU4502 to 84.07698.037, PU4503 to 84.00312.037
Reason: Material shortage issue
Possible Risk:

P38--Change PL4501 to 68.R8810.10G
Reason: Increase ripple
Possible Risk:

P39--Change PR4603 to 32.4K
Reason: OCP modify
Possible Risk:

P39--Change PU4602 to 84.07698.037, PU4603 to 84.00312.037
Reason: Material shortage issue
Possible Risk:

P41--Add PG4810, PG4809
Reason: Increase input current
Possible Risk:

P67--Change PU9202, PU9304, PU9205 PL9201
Reason: Material shortage issue
Possible Risk:

P67--Mount PTC9203
Reason: Decrease output ripple
Possible Risk:

P58--Dummy D46
Reason: For UVP circuit by Customer requirement
Possible Risk:

P58--Add Q57
Reason: Prevent battery only, voltage through body diode return back
to adaptor, induce unknow risk
Possible Risk:

P67--Add PG9218~PG9220, PG9222~PG9224
Reason: Increase input current
Possible Risk:

P67--PR9208=13.3k, PR9210=78.7k, PR9209=78.7k, PR9213=66.5K for N12M-GS2
PR9208=10k, PR9210=75k, PR9209=49.9k,PR9213=42.2K for N12P-GV
Reason: Tune GPU P-State voltage
Possible Risk:

(ME Connector change)

1. Mini Card CONN: (MINI1)
Issue: The ANT cable's tube might
has risk to overlap with Low-case's shielding

Action: Changed the CONN height from 8.0 to 5.3mm

2. RTC & SPK & Fan CONN: (RTC1,SPKL1,SPKR1,FAN1)
Issue: Follow Sandra's request to
change the terminal with Gold plating

Action: change the CONN's terminal from Tin to Gold terminal

3. ODD & HDD CONN: (ODD1,HDD1)
Issue: Follow WKS's request to change
from SMT to DIP type for prevent Empty solder,
Floating solder Excess solder

Action: Changed the CONN from SMT to DIP type

4. TP Switch: (SWL1,SWR1)
Issue: Issue: Follow WKS's request to change
new Switch for prevent Empty solder,
Floating solder and Excess solder ect.

Action: Changed new switch.

5. WLA: (MINI1)
Issue: Issue: cost too high
Action: Changed size the same new connector.

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PVT

(2010/10/28~2011/01/05)

P63_ Dummy RN8606
Reason: for double pull high
Possible Risk: Rework ok

P30_ Delete R3714,Q3704(Q00008)
Reason:customer request delete S3 error circuit
Possible Risk: Rework ok

P32_change D3908 to Schottky diode(Q-00009)
Reason:customer request
Possible Risk: Rework ok

P58_UVP R9316 change to 475K
Reason: customer request
Possible Risk: Rework ok

(2011/01/11~01/18)

P8_Add R805,R804(Q00002)
Reason: customer request
Possible Risk: Rework ok

P15_G680 reset_change D1901 to schottky diode(Q00003)
Reason: customer request
Possible Risk: Rework ok

P15_ Delete R1928
Reason: Customer request for DeepSleep issue
Possible Risk: Rework ok

P20_ Delete R2415
Reason: Customer request for DeepSleep issue
Possible Risk: Rework ok

P22_ R2604 change to 10.5K, R2635 change to 8.87K, Q2602 change to transistor 84.02222.V11, R2612 change to 100K, Mount R2616
Dummy Q2607, R2602, C2602, Q2610, R2607, C2613, Q2606, R2606, R2615, C2612, Q2604, RN2605, Q2601, R2613, Q2603,
Add R2619, Q2611, Q2612, D2605, R2611,R2617(Q00004)
Reason: Customer request
Possible Risk: Rework OK

P8, 9, 37_ Add ED801, ED802, ED901, ED902, ED4501, ED4502 Varistor
Reason: EMI request for ESD protect
Possible Risk: Rework OK

P24_ U2801 power plane change to 3D3V_AUX_S5
Dummy R2809, (Q-00035)
Reason: Customer request for Thermal Sensor P2800 Issue
Possible Risk: Rework OK

P24_ R2811&R2812 change to 29.4K, R2810 change to 44.2K
R2824 change to 33.2K, R2833 change to 36.5K(Q-00006)
Reason: Thermal request for G709 temperature protect
Possible Risk: Rework OK

P37_ Mount PR4510, PR4511,PC4510
Reason: Customer request for VCCIO sense function (Q00013)
Possible Risk: Rework OK

P42_ Change LCD1 connector and pin define
Reason: Fool-proof is not good (ME)
Possible Risk:

P44_ Delete U5102~U5105
Reason: Manufactory request can not co-lay
Possible Risk:

P50_ R6803, R6810 change to 220 ohm
Reason: Adjust LED brightness
Possible Risk: Rework OK

P51_ Delete D6501, R6517, R6516; Add Q6505, Q6506, R6504,R6503
Reason: Manufactory request can direct use debug card
Possible Risk: Rework OK

P58_ Mount D46 schottky diode(Q00033)
Reason: Customer request
Possible Risk: Rework OK

P68_ R9303 change to 4.7K, R9315 change to 7.5K
C9309 cgange to 0.47uF
Reason: For VEVS report GPU sequence timing
Possible Risk: Rework OK

(2011/01/17~01/25)

P32_ Change BAT1 connector to 20.81602.007
Reason: Solve hitting L-case or battery shutdown issue (ME)
Possible Risk:

P58_ D46 change to Schottky diode 83.R2004.B8F(Q00033)
Reason: Customer request
Possible Risk: Rework OK

P33, 58_Delete Q57, Add PR4021~PR4023, PQ4008, PQ4009, PQ4011
Reason: Provide DCBATOUT short surge current (power team)
Possible Risk: Rework OK

P9_C901, C903, C904, C905 and C906 change to 22uF
Reason: For GFX power ripple
Possible Risk: Rework OK

P23_R2707 change to 47K
Reason: For UMA 75W setting
Possible Risk:

P23_R2724 change to 47K
Reason: For -1 version
Possible Risk:

P17_R2127~R2130 change to 47 ohm,R2130 change to 0 ohm
C2105, C2107, C2108, C2109 change to 22pF
Reason: For VEVS LPC report
Possible Risk:

P15_ D1901 change to dual schottky , dummy Q1904,
R1911 change to 1K, R1910 change to 10K ,add R1924(Q00003)
Reason: Customer request
Possible Risk: Rework OK

P29_R3619 change to 0 ohm, add R3622=10K
R3623, R3624, R3627, R3628=0 ohm, Dummy C3614
Reason: Customer request
Possible Risk: Rework OK

P25,P28 , 46_Dummy R2922 ,Q17~Q22, R329 R331 , R330, R333,C404, R5801~R5804, C5801, C5804, C5805, C5806, U5801, U5802(Q00042)
Reason: Customer request for External De-pop Circuit Eliminating Trial (Q00043)
Possible Risk: Rework OK

P22_ Q2602 change to FET MOS
Reason: Customer request
Possible Risk: Rework OK

P33_ PR4404 change to 715
Reason: For VCC_GFXCORE OCP protect (power team)
Possible Risk:

P36_ PT4301,PT4303,PT4304,PT4305,PT4309, Dummy PT4308
Reason: For CPU transient (power team)
Possible Risk:

P35_ PR4227 change to 3.57K
Reason: For CPU load line (power team)
Possible Risk:

P35_ PR4218 change to 33.2K
Reason: For CPU Imon setting (power team)
Possible Risk:

P37_PR4404 change to 715 ohm
Reason: For 3/5V OCP protect (power team)
Possible Risk: Rework OK

P35_PR4205 change to 2.74K
Reason: For CPU load line (power team)
Possible Risk: Rework OK

P35_PR4206 change to 17.8K
Reason: For CPU Imon setting (power team)
Possible Risk: Rework OK

P45_Dummy C5604 ,R5603 change
to 0 ohm,add R5604_7.5 ohm ,change Q5601(Q00011)
Reason: Customer request
Possible Risk: Rework OK

(2011/01/17~01/26)

P22_ R2635 change to 11K
Reason: Customer request
Possible Risk: Rework OK

P39_ PR4603 change to 16.2K
Reason: For 1.5V OCP protect (power team)
Possible Risk: Rework OK

P38_ PR4504 change to 93.1K
Reason: For 1.05V OCP protect (power team)
Possible Risk: Rework OK

P42_ Add EC4901
Reason:LDC connector DCBATOUT (EMI team)
Possible Risk: Rework OK

P58_ Add R496,R505,R499,C569,R495,R500,R518,R511
Reason:UVP protect(Customer request)
Possible Risk:

(2011/01/27)

P15_ DUMMY R1925(SUSPWRDNACK)
Reason:intel HR schematic check list
Possible Risk:Rework OK

P15_ Q1904 change to 84.03k15.A31
Reason:Low VGS
Possible Risk:Rework OK

P58_ Del R496,R505,R499,C569,R495,R500,R518,R511
Dummy:C568, C9322 and D46
Reason:UVP protect(Customer request)
Possible Risk:

P33_ add PC4025,PC4024,PR4207,PR4220,PQ4010,PR4552,PR4026,PQ4015
Reason:UVP protect(Customer request)
Possible Risk:

(2011/01/31)

P38_ Dummy PR4509,PR4506
Reason:For 1.05v VCCIO_SENSE ,dummy 1.05v is better
Possible Risk:Rework OK

(2011/02/08)

P41_ Add PR4808, PR4809, PR4810(DUMMY)
Reason: for intel released
new spec of Celeron and Pentium CPU VCCSA_PWR
Possible Risk:

(2011/02/09)

Add Aluminum Solid Capacitors 2ND source
Reason: Material shortage issue
Possible Risk:

P58_ Add D46
Reason:
Possible Risk:

(2011/02/11)

P25_ Change RN2901 to 22 ohm
Reason: DMIC VEVS report
Possible Risk:

(2011/02/14)

P69_DUMMY SPR1
Reason: factory damage issue
Possible Risk:

P40_change PU4701 new version
Reason: old will EOL
Possible Risk:

P58_ ADD D46,R498 change to 1M ohm
Reason:UVP protect
Possible Risk:Rework ok

P33_ DUMMY PR4026,PQ4015,PR4252,PR4022,PQ4011
Reason:UVP protect
Possible Risk:Rework ok

P25_ Delete EC2901 and EC2902
Reason: For D-MIC record sound quietly
Possible Risk: Rework OK

Reversion History

-1M

(2011/03/02)

P23_R2724 change to 64.9K
Reason: For -1M version
Possible Risk:

MATSUKI capacitance 47U/ 25V change to NCC
Reason:MATSUKI test failure issue
Possible Risk:

N12M GS2 HYN1GB

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Title: **Change History**

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