LCD-1

IVY Bridge (rPGA989)

Intel PCH (Panther Point)

DY:No stuff
SWG:SWG SKU

PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.

BOM1

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Title: *Cover Page*

Size	Document Number	Rev
A3	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 1 of 102

LCD-1 Discrete Block Diagram

Project Code: 91.4SE01.001
PCB(Raw Card): 11248

PCB Layer Stackup

L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOTTOM

NVIDIA N13PNS1 GB4-128 83,84,85,86,87

PCIe 16X Gen2

Intel CPU Ivy Bridge 4~10

CPU XDP 11

PCH XDP 26

Channel A DDR3 1600/1333

UNBUFFERED DDR3 SODIMM Normal Socket Primary 15

204-PIN DDR3 SODIMM

Channel B DDR3 1600/1333

UNBUFFERED DDR3 SODIMM Normal Socket Primary 14

VRAM PortA DDR3 2Gbx4 88,89

VRAM PortB DDR3 2Gbx4 90,91

FDI x4

DMI x4

Intel Panther Point 17~25

USB 3.0 (4 ports)
USB 2.0 (14 ports)
AC97 2.3/Azalia Interface
Serial ATA 150MB/s
ACPI 2.0
LPC I/F
PCI Rev 2.3
PCI Express
INT. RTC

SATA HDD
SATA HDD CONN 56
SATA Port 0

SATA ODD
SATA ODD CONN 56
SATA Port 1

DOCKING CONN 94
SATA Port 4

2CH SPEAKER 58

AUDIO COMBO Jack

AUDIO CODEC ALC3202 29
HD AUDIO

MEDIA CARD READER
REALTEK RTS5229
Socket P/N:62.10051.A51

82

PCI Express 1

USB 3.0 CONN 62
USB 2.0 CONN 61
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USB 2.0 CH0
USB 2.0 CH1,9

High Speed BUS to Docking 94
USB 3.0 port 3
USB 2.0 CH2,8

14" HD/HD+ LCD 49
Dual Link LVDS

CRT Port 50
CRT SELECTION 50
RGB CRT

mini DP connector 52
Display Port

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Display Port

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CH11
USB 2.0

SPI FLASH 60
SPI

USB 2.0 CH12
PCI Express 2
Mini PCI-E WLAN Card 65

USB 2.0 CH3
SATA Port 2
Mini PCI-E WWAN/mSATA 66
SIM 66

USB 2.0 CH5
PCI Express 3
82
Express Card

PCI Express 4
REALTEK GLAN RTL8111F 31
GBE Switch PI3L500AZFEX 31

CH9
USB 2.0 CH4,13
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CAMERA
RJ45
USB Conn AOU4

LPC Bus / 33MHz

KBC NPCE885G 27
CH10

LPC Debug Board Conn 71
TPM 77

G-Sensor 79
Touch Pad Finger Print 69
Int. KB 69
Thermal 28
FAN 28

PWR Load SW 36,37,97
AC Adapter 38
BATT 39
RTC 60
RFID 80
Docking Connector 94

Battery Charger BQ24707 40
INPUTS | OUTPUTS
AD+ | BT+

System DC/DC TPS51123RGER 41
DCBATOUT | 5V_S5, 3D3V_S5

CPU DC/DC ISL95838HRTZ 42,43
DCBATOUT | VCC_CORE

1D05V_VTT TPS51219RTER 45
DCBATOUT | 1D05V_VTT

1D5V_S3/DDR3_REF 0D75V_S0 TPS51216RUKR 46
DCBATOUT | 0D75V_S0, 1D5V_PWR, DDR3_VREF

1D8V_S0 TPS51311RGTR 47
3D3V_S5 | 1D8V_S0

VCCSA TPS51461RGER 48
5V_S5 | VCCSA

VGA_CORE ISL62882CHRTZ 92
DCBATOUT | VGA_CORE

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Title: Block Diagram
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PCH Strapping

Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

PCIe Routing

LANE1	Card Reader
LANE2	Mini Card1(WLAN)
LANE3	Express Card
LANE4	GBE LAN
LANE5	X
LANE6	X
LANE7	X
LANE8	X

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1D0V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

USB Table

Pair	Device
0	USB3.0 port 0
1	USB2.0 port 1
2	USB3.0 Docking
3	WWAN
4	USB2.0 port (AUO4)
5	New Card
6	X
7	X
8	USB2.0 Docking
9	USB2.0 port 2
10	FPR
11	BLUETOOTH
12	WLAN
13	Camera

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

SATA Table

SATA Pair	SATA Device
0	HDD
1	ODD
2	mSATA
3	N/A
4	Docking
5	N/A

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Title: Table of Content

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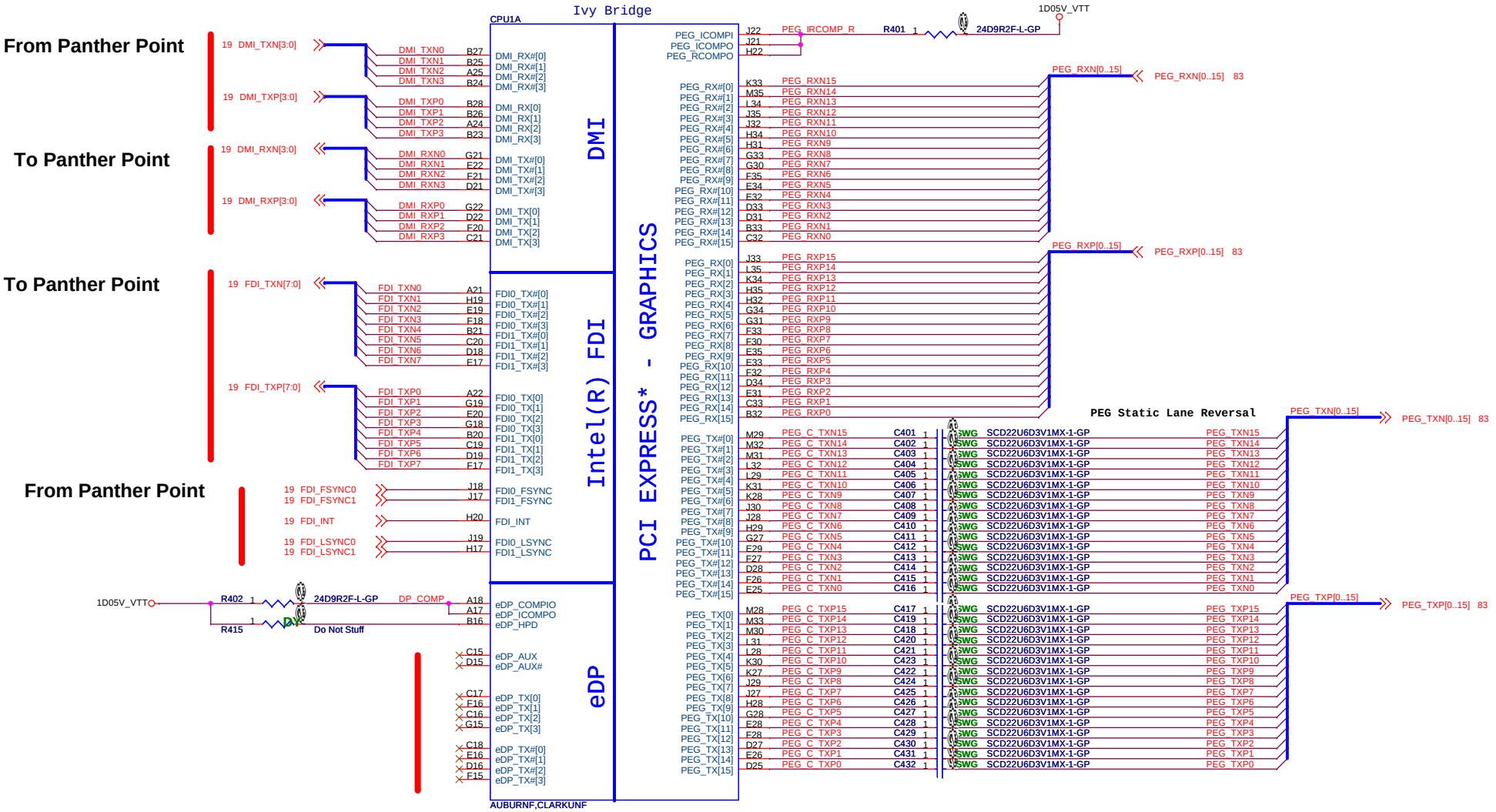
SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
A3	CD1 DIS	SC

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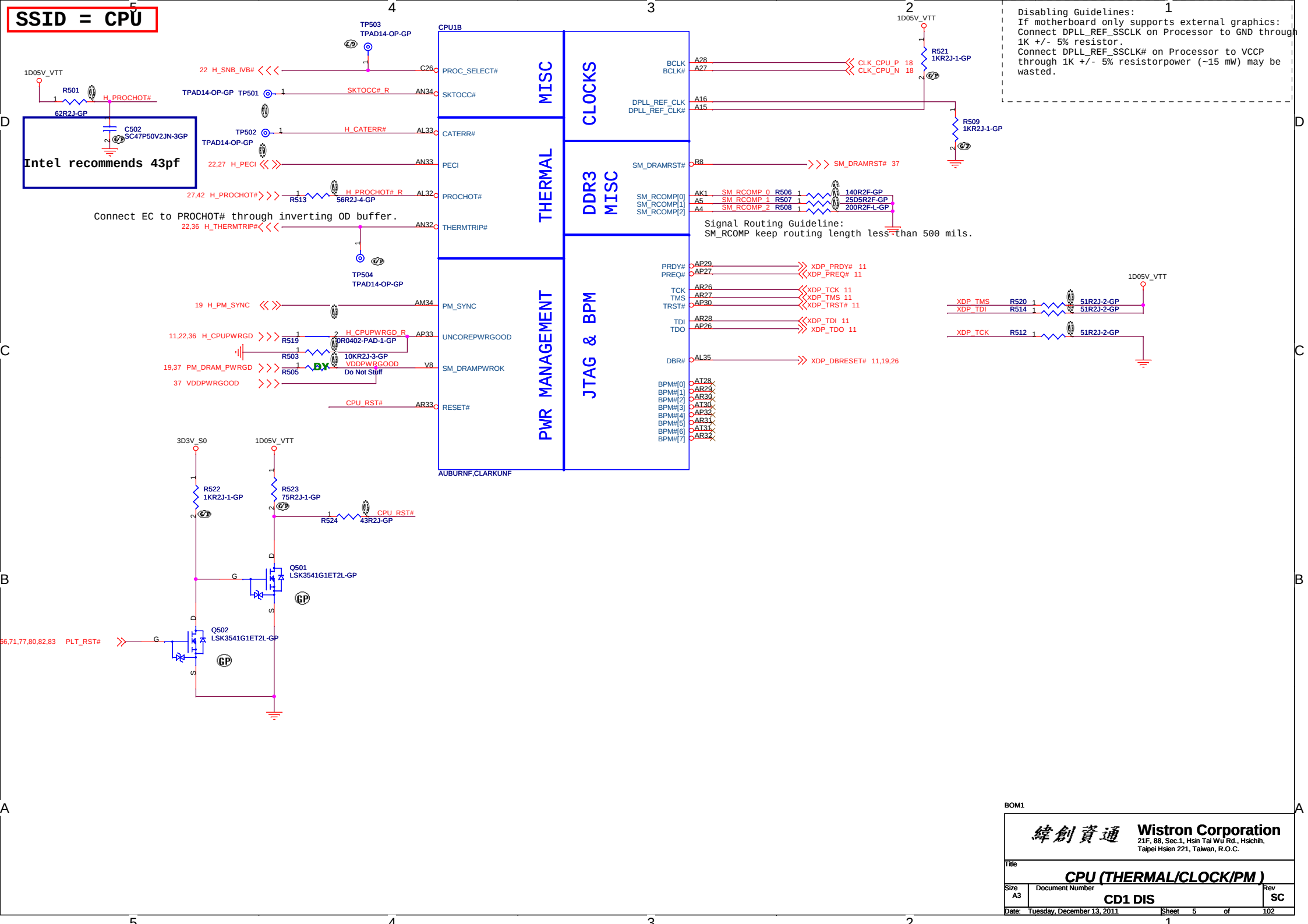
SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.



BOM1

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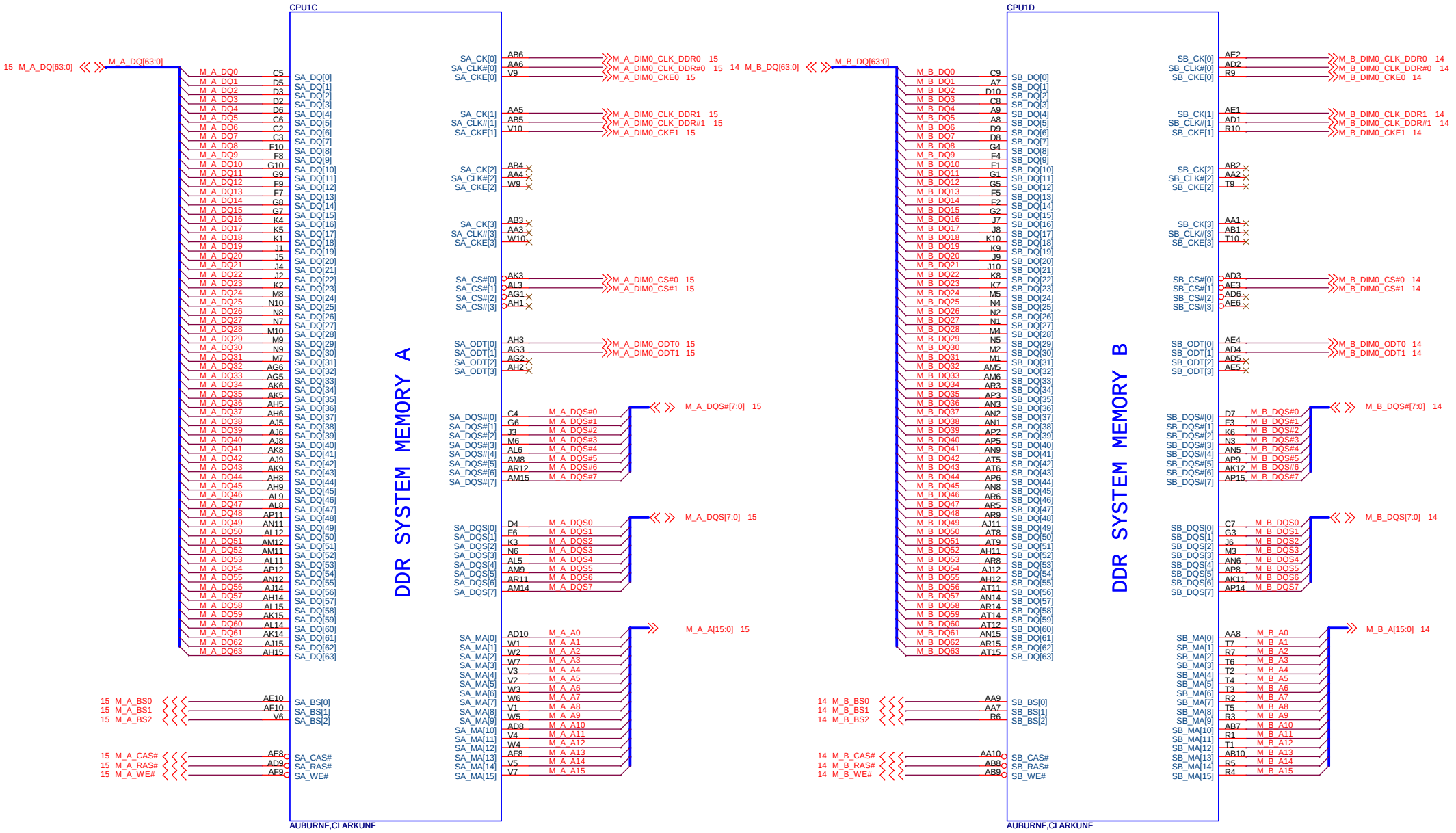
Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A3	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 5 of 102

SSID = CPU



BOM1

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Title		
	CPU (DDR)	
Size: A3	Document Number: **CD1 DIS**	Rev: SC
Date: Tuesday, December 13, 2011	Sheet 6 of 102	

SSID = CPU

CFG2 — R702 1KR2J-1-GP

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

VCC_GFXCORE — R376 Do Not Stuff DY — VAXG_SENSE
VCC_CORE — R377 Do Not Stuff DY — VCC_SENSE
VSSAXG_SENSE — R708 49D9R2F-GP
VSS_SENSE — R309 49D9R2F-GP

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG7 — R705 Do Not Stuff DY

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CPU1E

TPAD14-OP-GP TP715 — 11 CFG0 — AK28 CFG[0]
TPAD14-OP-GP TP717 — CFG2 — AL26 CFG[1]
TPAD14-OP-GP TP719 — CFG3 — AL27 CFG[2]
TPAD14-OP-GP TP716 — CFG4 — AK26 CFG[3]
TPAD14-OP-GP TP718 — CFG5 — AL29 CFG[4]
TPAD14-OP-GP TP720 — CFG6 — AL30 CFG[5]
TPAD14-OP-GP TP721 — CFG7 — AM31 CFG[6]
AM32 CFG[7]
AM30 CFG[8]
AM28 CFG[9]
AM26 CFG[10]
AN28 CFG[11]
AN31 CFG[12]
AN26 CFG[13]
AM27 CFG[14]
TPAD14-OP-GP TP722 — AK31 CFG[15]
AN29 CFG[16]
CFG[17]

CFG

VAXG_SENSE — AJ31 VAXG_VAL_SENSE
VSSAXG_SENSE — AH31 VSSAXG_VAL_SENSE
VCC_SENSE — AJ33 VCC_VAL_SENSE
VSS_SENSE — AH33 VSS_VAL_SENSE

AJ26 RSVD5

F25 RSVD8
F24 RSVD9
F23 RSVD10
D24 RSVD11
G25 RSVD12
G24 RSVD13
E23 RSVD14
D23 RSVD15
C30 RSVD16
A31 RSVD17
B30 RSVD18
B29 RSVD19
D30 RSVD20
B31 RSVD21
A30 RSVD22
C29 RSVD23

J20 RSVD24
B18 RSVD25

J15 RSVD27

RESERVED

VCC_DIE_SENSE — AH27
VSS_DIE_SENSE — AH26

RSVD28 L7
RSVD29 AG7
RSVD30 AE7
RSVD31 AK2
RSVD32 W8
RSVD33 AT26
RSVD34 AM33
RSVD35 AJ27

RSVD37 T8
RSVD38 J16
RSVD39 H16
RSVD40 G16

RSVD_NCTF41 AR35 — CPU_NCTF5 — TP705 TPAD14-OP-GP
RSVD_NCTF42 AT34 — CPU_NCTF6 — TP706 TPAD14-OP-GP
RSVD_NCTF43 AT33
RSVD_NCTF44 AP35
RSVD_NCTF45 AR34

RSVD_NCTF46 B34
RSVD_NCTF47 A33
RSVD_NCTF48 A34 — CPU_NCTF7 — TP707 TPAD14-OP-GP
RSVD_NCTF49 B35 — CPU_NCTF4 — TP704 TPAD14-OP-GP
RSVD_NCTF50 C35

RSVD51 AJ32
RSVD52 AK32

BCLK_ITP AN35 — TP713 — TP713 TPAD14-OP-GP
BCLK_ITP# AM35 — TP714 — TP714 TPAD14-OP-GP

RSVD_NCTF56 AT2 — CPU_NCTF3 — TP703 TPAD14-OP-GP
RSVD_NCTF57 AT1 — CPU_NCTF2 — TP702 TPAD14-OP-GP
RSVD_NCTF58 AR1

KEY B1 — CPU_NCTF1 — TP701 TPAD14-OP-GP

AUBURNF,CLARKUNF

BOM1

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Title: CPU (RESERVED)
Size: A3 | Document Number: CD1 DIS | Rev: SC
Date: Tuesday, December 13, 2011 | Sheet 7 of 102

POWER

CPU1F

VCC_CORE

VCC CORE:53A

8 x 22 uF at Top Socket Cavity

C849 SC22U6D3V5MX-2GP
C851 SC22U6D3V5MX-2GP
C850 SC22U6D3V5MX-2GP
C828 SC22U6D3V5MX-2GP
C836 SC22U6D3V5MX-2GP
C846 SC22U6D3V5MX-2GP
C847 SC22U6D3V5MX-2GP
C848 SC22U6D3V5MX-2GP

8 x 22 uF at Top Socket Edge

C855 SC22U6D3V5MX-2GP
C857 SC22U6D3V5MX-2GP
C856 SC22U6D3V5MX-2GP
C852 SC22U6D3V5MX-2GP
C859 SC22U6D3V5MX-2GP
C853 SC22U6D3V5MX-2GP
C854 SC22U6D3V5MX-2GP
C858 SC22U6D3V5MX-2GP

5 x 10 uF at Bottom Socket Cavity

C864 SC10U6D3V5KX-1GP
C862 SC10U6D3V5KX-1GP
C863 SC10U6D3V5KX-1GP
C861 SC10U6D3V5KX-1GP
C860 SC10U6D3V5KX-1GP

5 x 10 uF at Bottom Socket Cavity

C869 SC10U6D3V5KX-1GP
C868 SC10U6D3V5KX-1GP
C867 SC10U6D3V5KX-1GP
C866 SC10U6D3V5KX-1GP
C865 SC10U6D3V5KX-1GP

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

AUBURNF,CLARKUNF

VCCIO:8.5A

1D05V_VTT

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 Y10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J13
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

C870 C871 C872 C874 C875 SC22U6D3V5MX-2GP

C881 C882 C883 C884 C885 Do Not Stuff

C886 ST330U2D5V6M-1-GP

C878 C879 C873 C877 C876 C880 SC22U6D3V5MX-2GP

DY

VCCIO Output Decoupling Recommendation:
3 x 330 uF, 6mΩ
5 x 22 uF & 5 x 0805(no-stuff) MB Bottom Socket Cavity
7 x 22 uF & 2 x 0805(no-stuff) MB Top Socket Catity

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V_VTT
H_CPU_SVIDDAT R804 130R2F-1-GP

R807 75R2J-1-GP 1D05V_VTT

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 43R2J-GP
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

VR_SVID_ALERT# 42
H_CPU_SVIDCLK 42
H_CPU_SVIDDAT 42

1D05V_VTT
R805 10R2F-L-GP
VCCIO_SENSE
VSSIO_SENSE
R806 10R2F-L-GP

VCC_CORE
R801 100R2F-L1-GP-U

VCC_SENSE AJ35
VSS_SENSE AJ34

VCCSENSE 42
VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10
VSS_SENSE_VCCIO A10

VCCIO_SENSE 45
VSSIO_SENSE 45

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size: Custom | Document Number: CD1 DIS | Rev: SC

Date: Tuesday, December 13, 2011 | Sheet 8 of 102

Ivy Bridge POWER

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

11/28 Wistron ORB change to 100ohm (64.10005.6DL), need verify

CPU1G

VCC_GFXCORE

2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge

2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

SC22U6D3V5MX-2GP

GRAPHICS

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

SENSE LINES

VAXG_SENSE
VSSAXG_SENSE
AK35
AK34
VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

VREF

SM_VREF
AL1
SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
B4
D1
DDR_WR_VREF01 12
DDR_WR_VREF02 12

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

1D5V_S0
R1214 1KR2F-3-GP
R1215 1KR2F-3-GP
C1203 Do Not Stuff DY
C1204 Do Not Stuff DY

VCC_GFXCORE
VCC_AXG_SENSE
VSS_AXG_SENSE
R906 10R2F-L-GP
R907 10R2F-L-GP

VDDQ Output Decoupling Recommendation:
1 x 330 uF, 6mΩ
6 x 10 uF (0805)

DDR3 -1.5V RAILS

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15
AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

1D5V_VDDQ
SC10U6D3V5KX-1GP
PTC902 ST330U2D5VBM-1-GP

VDDQ:12A

PR901 PD01RL0816F-L-GP
1D5V_S0
C934 C933 C932 C925 SC22U10V2KX-5GP

NEC, 330uF, 2.5V
ESR=6mΩ
Iripple=4.563A

7/19 Wire to GND

SA RAIL

VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8
M27 M26 L26 J26 J25 J24 H26 H25

VCCSA

VCCA:6A

SC10U6D3V5KX-1GP
PTC903 ST330U2D5VBM-1-GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF, 6mΩ
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

NEC, 330uF, 2.5V, B2
ESR=9mΩ
Iripple=3.073A

MISC

VCCSA_SENSE
H23
VCCSA_SENSE 48

VCCSA_VID[0]
VCCSA_VID[1]
C22
C24
VCCSA_SEL0 48
VCCSA_SEL1 48

RN901 SRN1KJ-7-GP

VCCIO_SEL
A19
R723 DY Do Not Stuff
VCCIO_SEL 45

9/2 VCCIO_SEL

define 1D05V_VTT power voltage whether 1.00V(IB) or 1.05V(SB)		
Part	Logic-Low [IVY-ES1]	Logic High [SandyBridge]
PR4505	DY	ASM
PR4525	(DY)	DY
PR4511	(DY)	DY
PR4518	ASM	ASM
R8765	ASM	DY

9/1 IVY Bridge ES1: remove PR4505
Sandy Bridge: remove R8765 (SDV)

R8765 DY Do Not Stuff

1.8V RAIL

AUBURNF,CLARKUNF

1D8V_S0

VCCPLL:1.5A

VCCPLL1 VCCPLL2 VCCPLL3
B6 A6 A2

C905 SC10U6D3V5KX-1GP
C903 C904 SC1U6D3V3KX-2GP
PTC901 ST330U2D5VBM-1-GP

NEC, 330uF, 2.5V, B2
ESR=9mΩ
Iripple=3.073A

VCCPLL Output Decoupling Recommendation:
1 x 330 uF, 6mΩ
2 x 1 uF (0402)
1 x 10 uF (0805)

BOM1

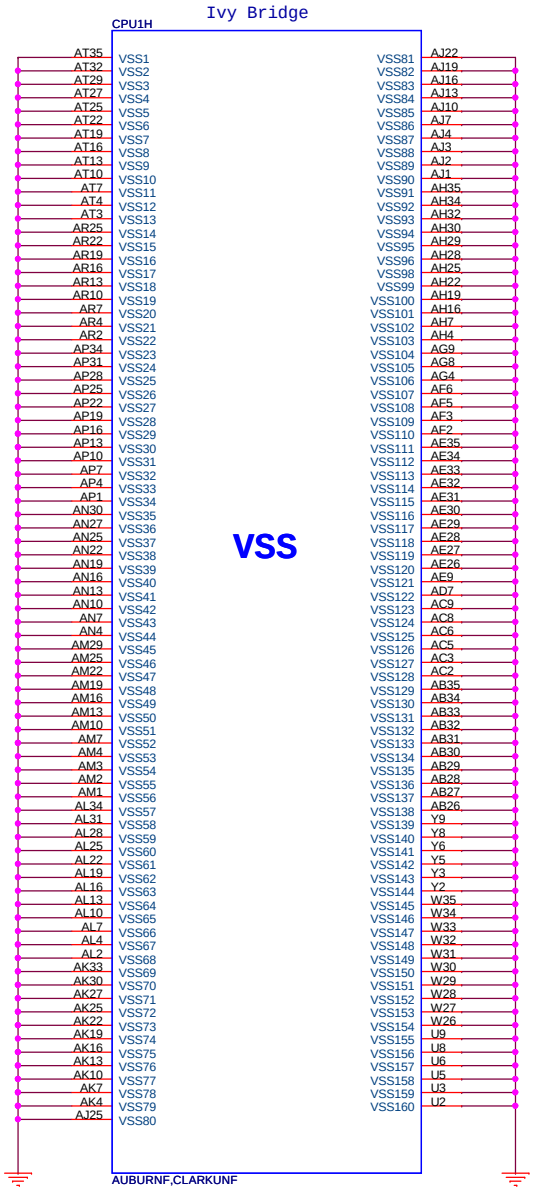
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

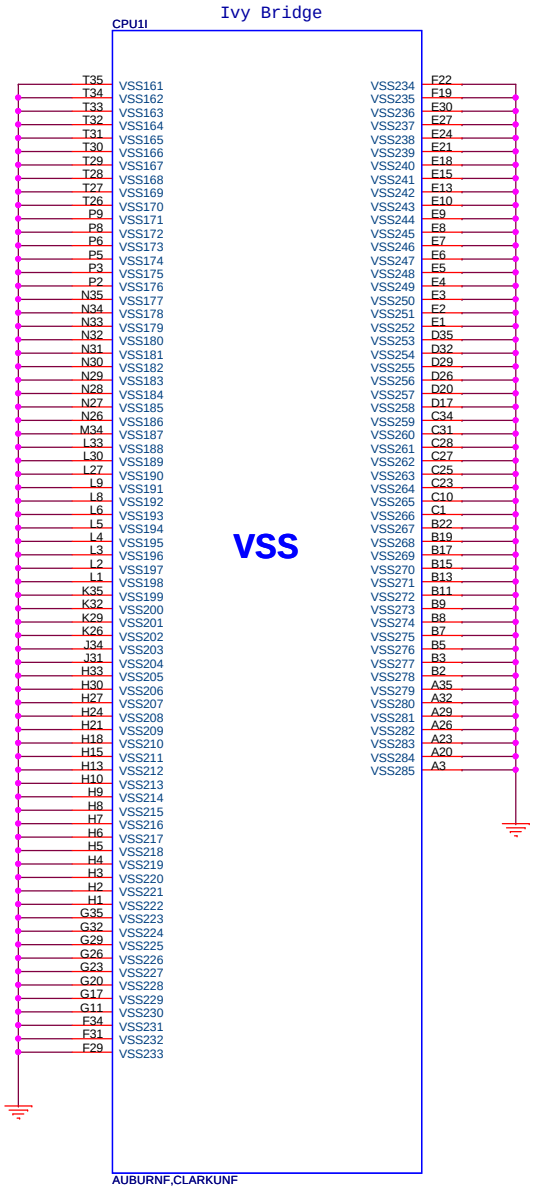
Title: CPU (VCC_GFXCORE)

Size: A3 | Document Number: CD1 DIS | Rev: SC

Date: Tuesday, December 13, 2011 | Sheet 9 of 102

SSID = CPU





BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 10 of 102

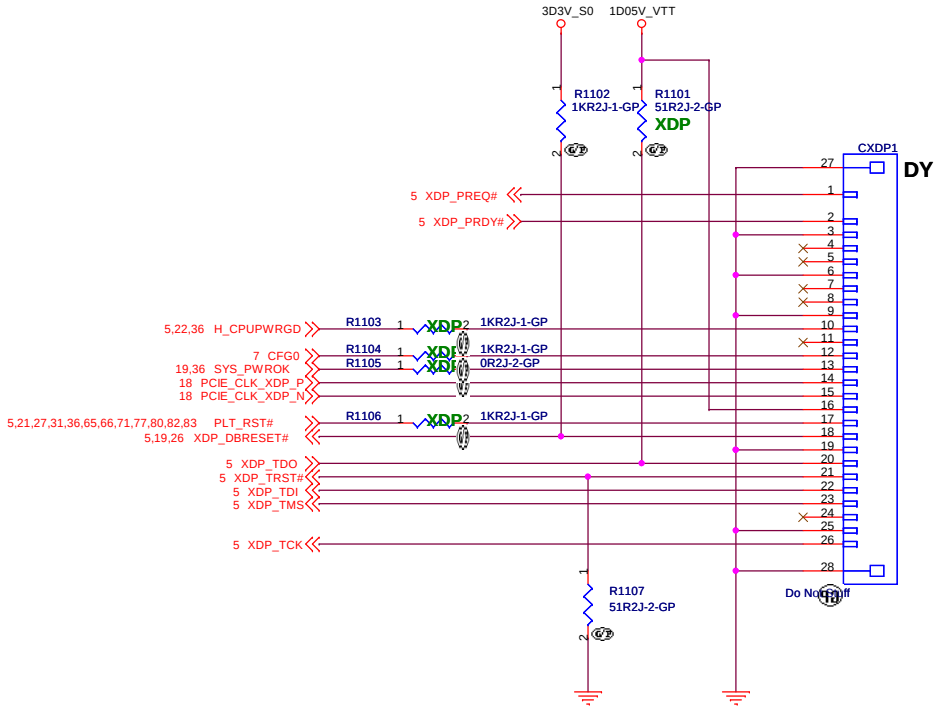
In production, All of parts should be not moounted except of pulldown 51 ohm on TRSTn and Pullup DBR#.

SIGNAL	REF DES	ENABLE	DISABLE
TDO	R1101	ASM	NOASM
TRST#	R1107	ASM	ASM
DBRESET#	R1102	ASM	ASM
PLT_RST#	R1106	ASM	NOASM
CFG0	R1104	ASM	NOASM
CPUPWRGD	R1103	ASM	NOASM
SYS_PWROK	R1105	ASM	NOASM
	CXDP1	ASM	NOASM

LOGIC

9/2 CPU_XDP

Part	Enable	Disable
R1101	ASM	DY
R1107	ASM	ASM
R1102	ASM	ASM
R1106	ASM	DY
R1104	ASM	DY
R1103	ASM	DY
R1105	ASM	DY
CXDP1	ASM	DY



CPU XDP SFF 26pin IF
Pin 1 OBSFN_A0 (PREQ#, I/O)
Pin 2 OBSFN_A1 (PRDY#, I/O)
Pin 3 GND
Pin 4 OBSDATA_A0 (Open, I/O)
Pin 5 OBSDATA_A1 (Open, I/O)
Pin 6 GND
Pin 7 OBSDATA_A2 (Open, I/O)
Pin 8 OBSDATA_A3 (Open, I/O)
Pin 9 GND
Pin 10 HOOK0 (PWRGD, In)
Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
Pin 12 HOOK2 (CFG0, Out)
Pin 13 HOOK3 (vr_READYSYS_PWROK,Out)
Pin 14 HOOK4 (BCLK, In)
Pin 15 HOOK5 (BCLK#, In)
Pin 16 VCCOBS_AB (VCCP Voltage of CPU, In)
Pin 17 HOOK6 (RESET#, Out)
Pin 18 HOOK7 (DBR#, Out)
Pin 19 GND
Pin 20 TDO, In
Pin 21 TRST#, Out
Pin 22 TDI, Out
Pin 23 TMS, Out
Pin 24 TCK1 (Open)
Pin 25 GND
Pin 26 TCK0 ,Out

BOM1

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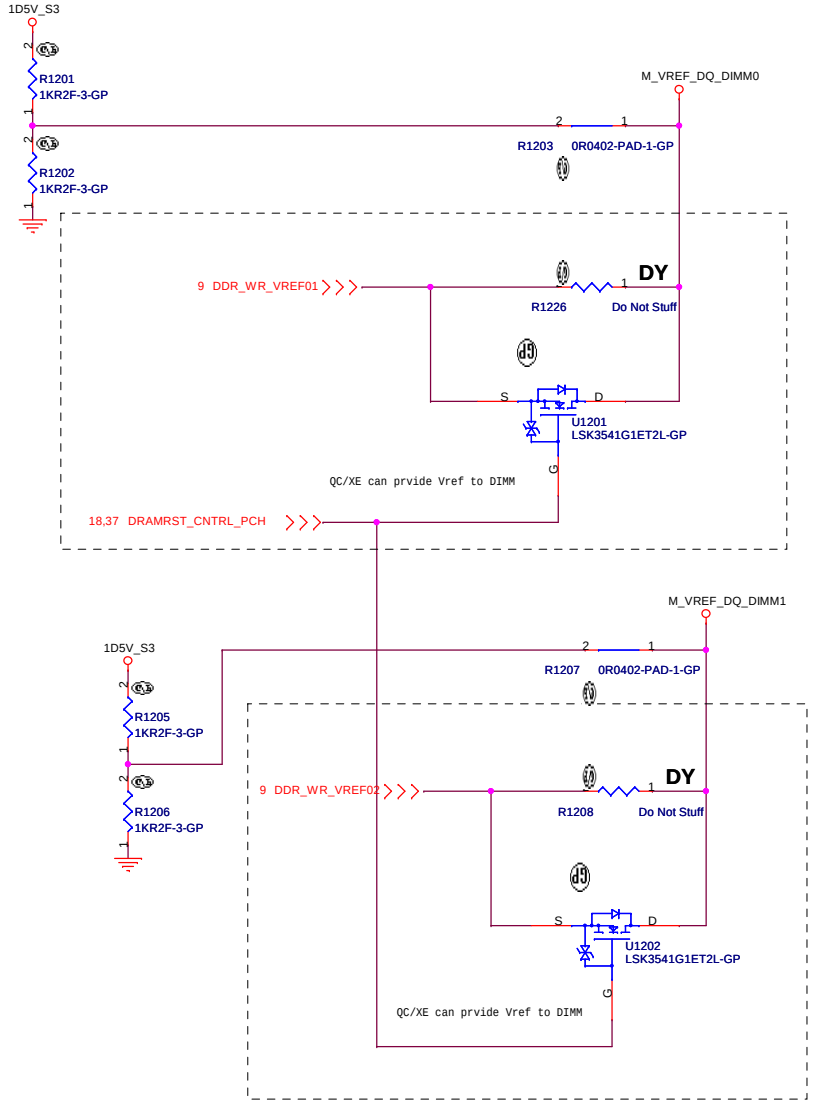
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU XDP

Size	Document Number	Rev
A3	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 11 of 102

VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation



BOM1

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Title: *M3*		
Size: A3	Document Number: CD1 DIS	Rev: SC
Date: Tuesday, December 13, 2011	Sheet 12 of 102	

(Blanking)

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 13 of 102

SSID = MEMORY

20101231

DM2

DDR3-204P-144-GP-U1

H =4mm

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

Thermal EVENT

20110209

SODIMM B DECOUPLING

Layout Note:
Place these Caps near SO-DIMMB.

Decoupling cap
1x330uF
6x10uF

Place these caps close to VTT1 and VTT2.

RF

PART NUMBER	Height	TYPE
62.10017.S51	4mm	REVERSED
		REVERSED
		REVERSED
		REVERSED

1110 X02 Modify:
DM2 1st change to 62.10017.P61; 2nd change to 62.10017.N41 on ST stage from ME updated connector list.

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3 SO-DIMM2

Size: Custom | Document Number: CD1 DIS | Rev: SC

Date: Tuesday, December 13, 2011 | Sheet 14 of 102

SSID = MEMORY

20101231

DM1

DDR3-204P-138-GP

62.10024.F31

H =7.0mm

Place these caps close to VTT1 and VTT2.

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

20110209

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMA.

Decoupling cap
1x330uF
6x10uF

PART NUMBER	Height	TYPE
62.10017.K91	7.0mm	REVERSED
		REVERSED
		REVERSED
		REVERSED

1110 X02 Modify:
DM1 1st change to 62.10017.Q41; 2nd change to 62.10017.N11 on ST stage from ME updated connector list.

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3 SO-DIMM1

Size: Custom | Document Number: CD1 DIS | Rev: SC

Date: Tuesday, December 13, 2011 | Sheet 15 of 102

(Blanking)

BOM1

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 16 of 102

SSID = PCH

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Notes:
ME_UNLOCK (HDA_SDO) connect to EC.
Make sure EC drive this pin "low" all the time.

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

NO REBOOT STRAP

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

HDD
ODD
mSATA
DOCKING
Place to near connector

Wistron Corporation	緯創資通
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Title: PCH : HDA/JTAG/SATA
Size: A3 | Document Number: CD1 DIS | Rev: SC
Date: Tuesday, December 13, 2011 | Sheet 17 of 102

SSID = PCH

If PCIE port 1 is disabled, it will cause all PCIE port disabled

9/25 add

PCH1B — 2 OF 10

Card Reader — WLAN — NEW CARD — LAN — PCI-E* — SMBUS — Controller Link — CLOCKS — FLEX CLOCKS

Card Reader CLK — RN1807 SRN0J-6-GP

WLAN CLK — RN1808 SRN0J-6-GP

EXC CLK — RN1815 SRN0J-6-GP

LAN CLK — RN1811 SRN0J-6-GP

RN1801 SRN10KJ-5-GP

RN1814 SRN10KJ-5-GP

RN1816 SRN10KJ-5-GP

PCIECLKRQ1# and PCIECLKRQ2# Support S0 power only

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

84.2N702.J31
2nd = 84.2N702.031

84.2N702.A3F
2nd = 84.DM601.03F

82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.C61

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH : PCIE/SMBUS/CLK**

Size: A3 | Document Number: CD1 DIS | Rev: SC

Date: Tuesday, December 13, 2011 | Sheet 18 of 102

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

SSID = PCH

For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

PCH1C — PANTHER-GP-NF — 3 OF 10

DMI: DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN, DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP, DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN, DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP

FDI: FDI_RXN0–7, FDI_RXP0–7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

System Power Management: DSWVRMEN, DPWROK, WAKE#, CLKRUN#/GPIO32, SUS_STAT#/GPIO61, SUSCLK/GPIO62, SLP_S5#/GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN#/GPIO29, SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT/GPIO31, BATLOW#/GPIO72, RI#

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

PCH_WAKE#
CRB : 1K
CHKLIST: 10K

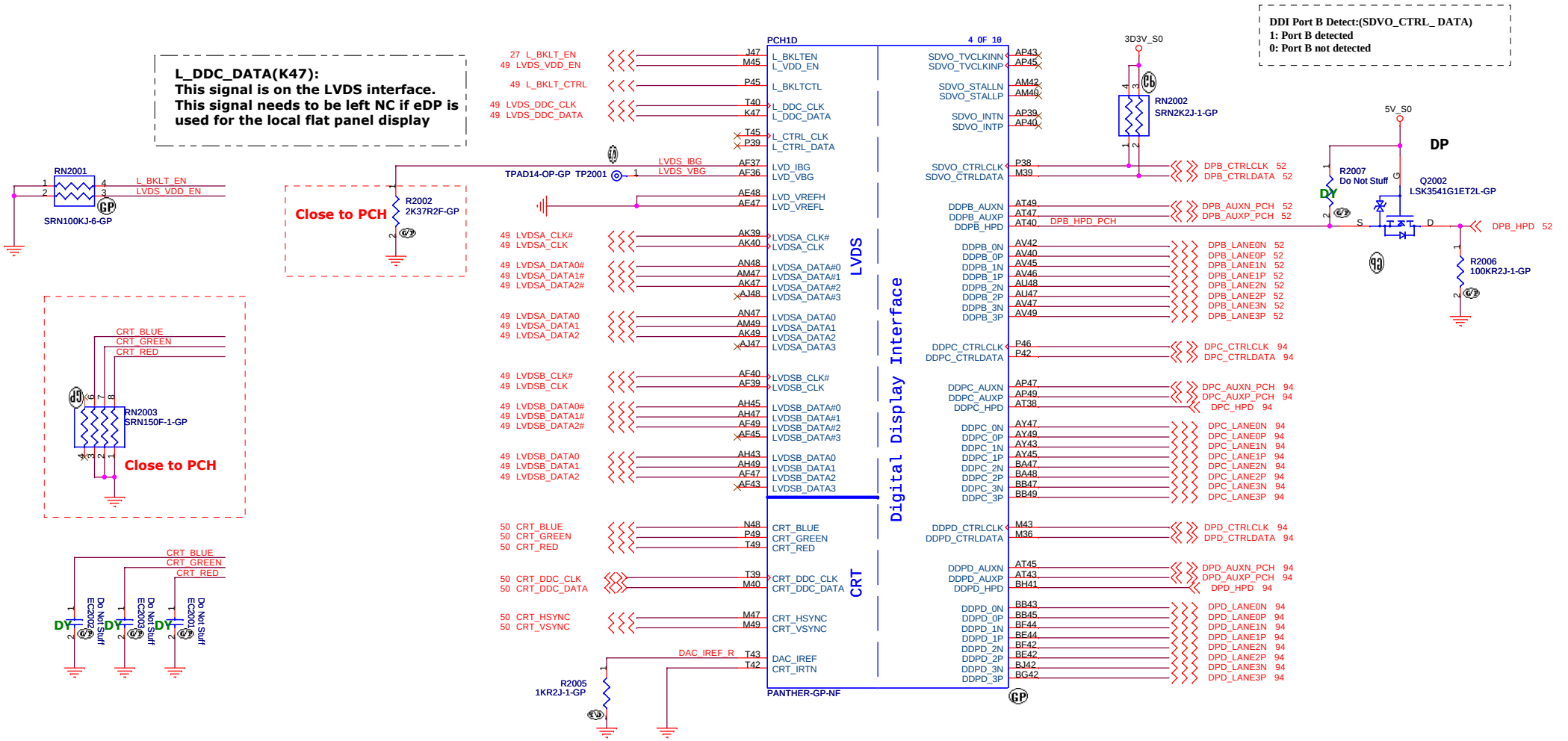
RN1901 SRN10KJ-8-GP

Q1901 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : DMI/FDI/PM
Size: A3 | Document Number: CD1 DIS | Rev: SC
Date: Tuesday, December 13, 2011 | Sheet 19 of 102



PORT	DDI PCH Pin Names	SDVO Mapping	DisplayPort Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

Digital Display Ports Enable and Disable Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
LVDS	L_DDC_DATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port B	SDVO_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

NOTE: LVDS and eDP on processor can not be enabled at the same time.

BOM1

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Title: **PCH : LVDS/CRT/DDI**

Size	Document Number	Rev
A3	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 20 of 102

SSID = PCH

For PPT USB3.0 feature

Utilize Port 9 for USB debug

USB Table

Pair	Device
0	USB3.0 port 0
1	USB2.0 port 1
2	USB3.0 Docking
3	WWAN
4	USB2.0 port (AU04)
5	New Card
6	X
7	X
8	USB2.0 Docking
9	USB2.0 port 2
10	FPR
11	BLUETOOTH
12	WLAN
13	Camera

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

GPIO51 and GPIO19 Internal PU

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : PCI/USB/NVRAM/RSVD

Size: A3 | Document Number: CD1 DIS | Rev: SC

Date: Tuesday, December 13, 2011 | Sheet 21 of 102

Note:
For PCH debug with XDP, need to NO STUFF R2218

PCH1F 6 OF 10

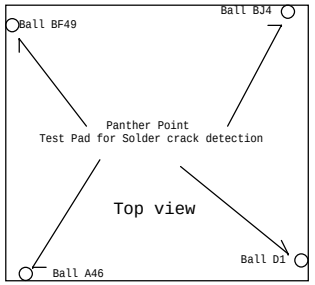
BOM Control

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

Model_ID	
PH	14"
PL	15"

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.



Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

NCTF TEST PIN:
A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49, BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48, D1, D49, E1, E49, F1, F49

PANTHER-GP-NF

BOM1

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Title: PCH : GPIO/NTCF/MISC

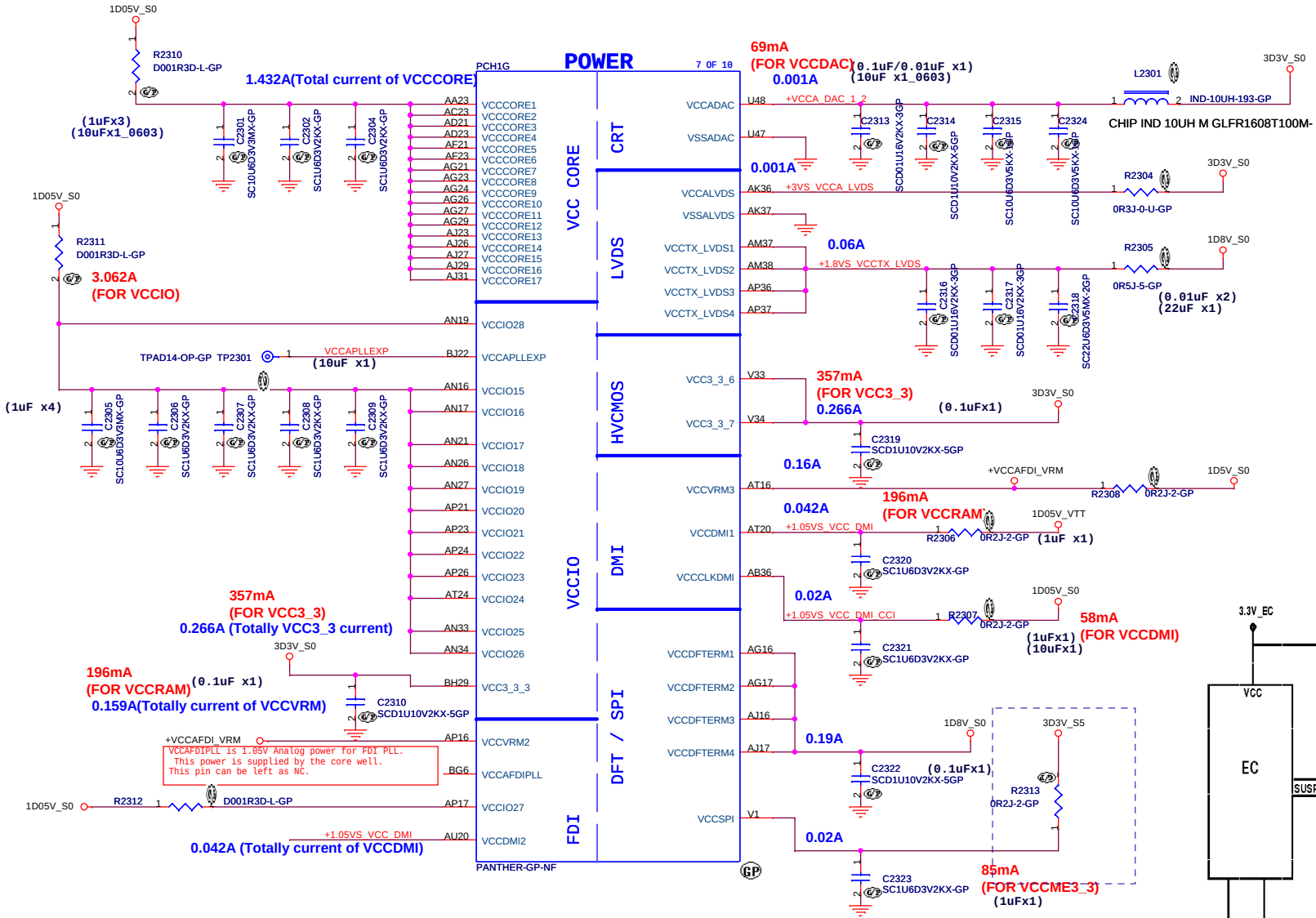
Size: A3 | Document Number: CD1 DIS | Rev: SC

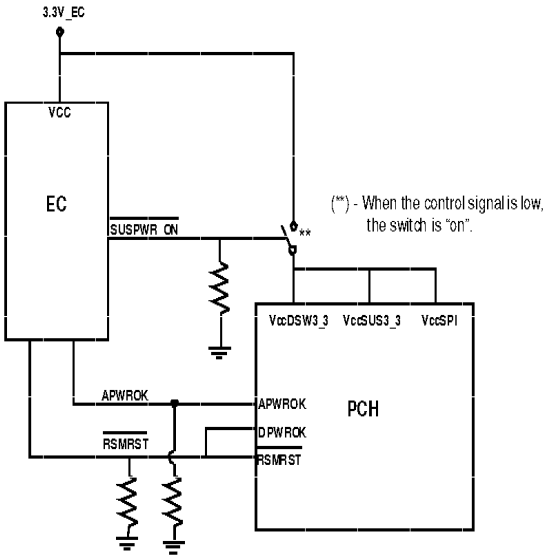
Date: Tuesday, December 13, 2011 | Sheet 22 of 102

SSID = PCH 6A

Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture





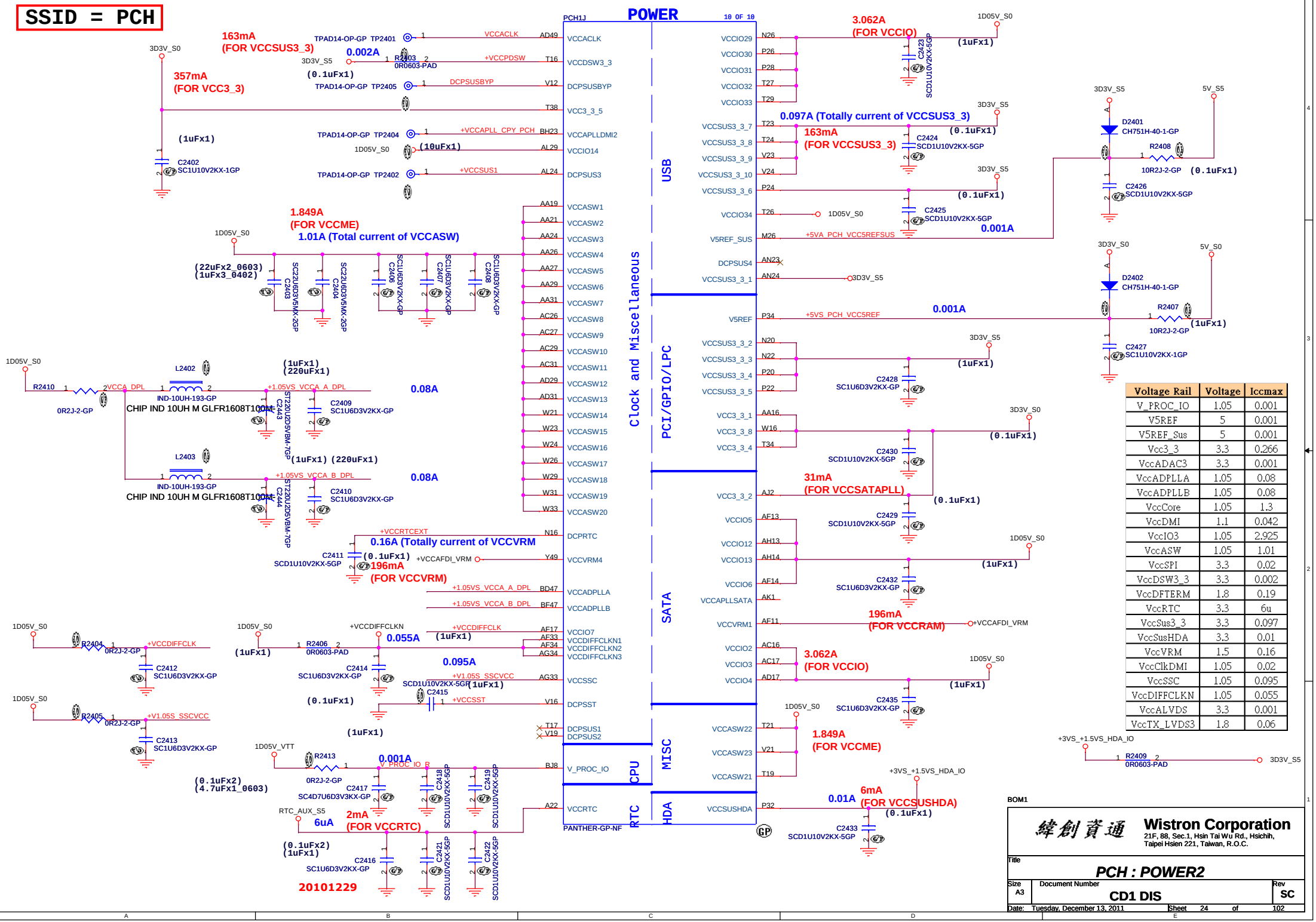
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH : POWER1**

Size	Document Number	Rev
A3	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 23 of 102

SSID = PCH



Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

BOM1

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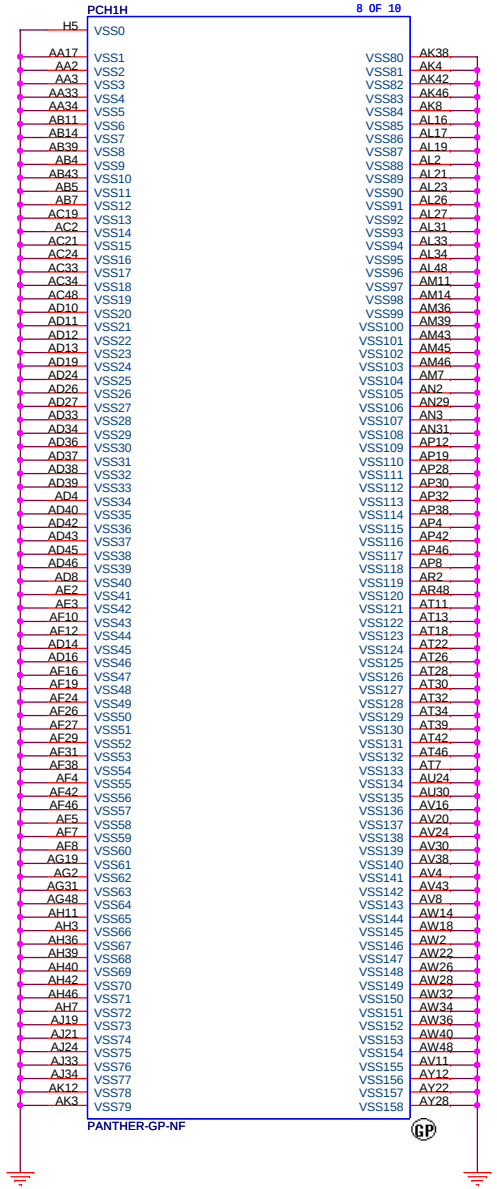
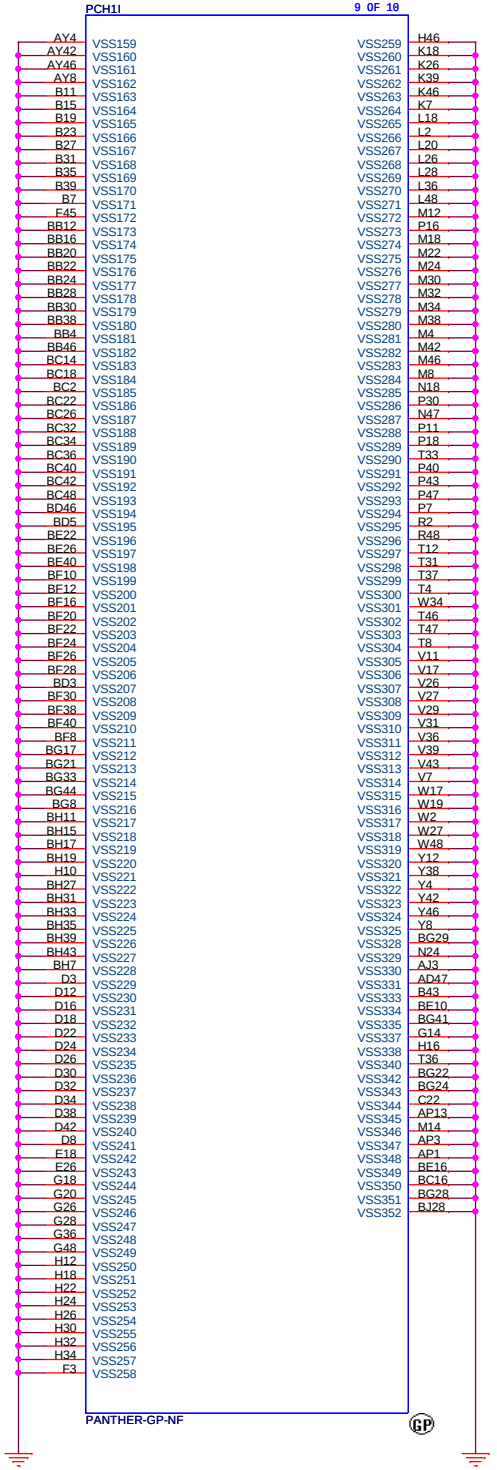
Title: PCH : POWER2

Size: A3 | Document Number: CD1 DIS | Rev: SC

Date: Tuesday, December 13, 2011 | Sheet 24 of 102

SSID = PCH





BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH : VSS***

Size	Document Number	Rev
A3	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 25 of 102

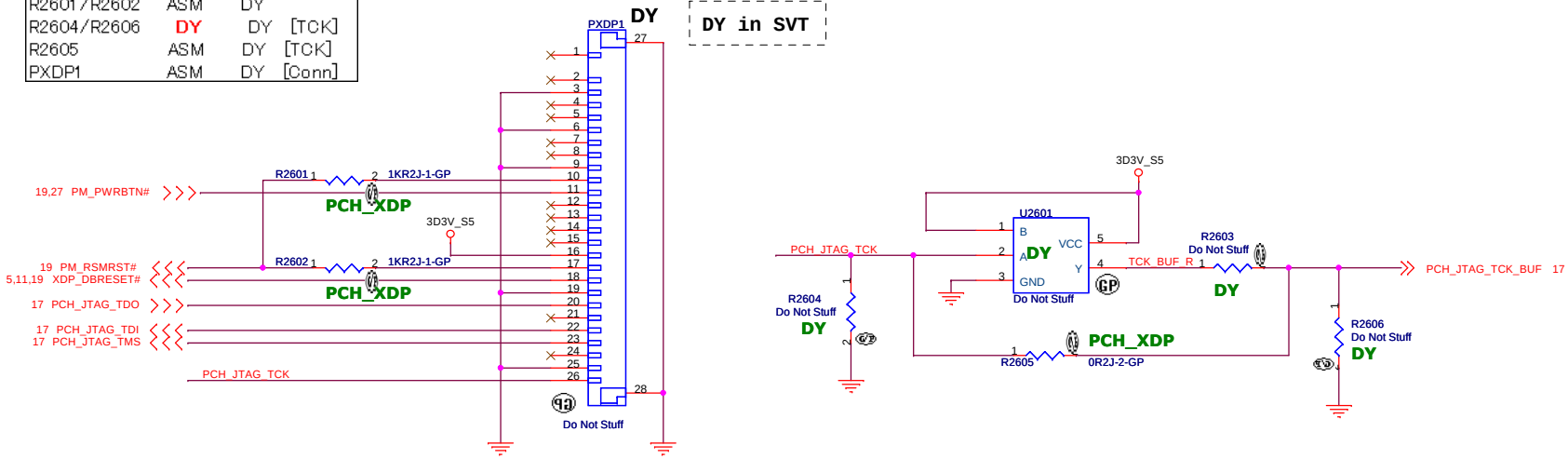
9/2 PCH_XDP

Part	Enable	Disable
R1726/R1730	ASM	ASM [TMS]
R1727/R1731	ASM	ASM [TDI]
R1728/R1732	ASM	DY [TDO]
R1729	ASM	DY [TCK]
R2601/R2602	ASM	DY
R2604/R2606	DY	DY [TCK]
R2605	ASM	DY [TCK]
PXDP1	ASM	DY [Conn]

PCH XDP

DY

DY in SVT



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_XDP

Size	Document Number	Rev
A3	CD1 DIS	SC

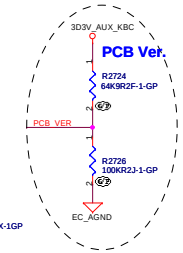
Date: Tuesday, December 13, 2011 Sheet 26 of 102

SSID = KBC

PCB Version A/D (PIN 98)		Pull-Low Resistor R2726	Pull-High Resistor (3D3V_AUX_KBC) R2724	Voltage
SA	14"	100K	10K	3.0V
	15"		20K	2.75V
SB	14"	100K	33K	2.48V
	15"		47K	2.24V
SC	14"	100K	64.9K	2.0V
	15"		76.8K	1.87V
1	14"	100K	100K	1.65V
	15"		143K	1.36V

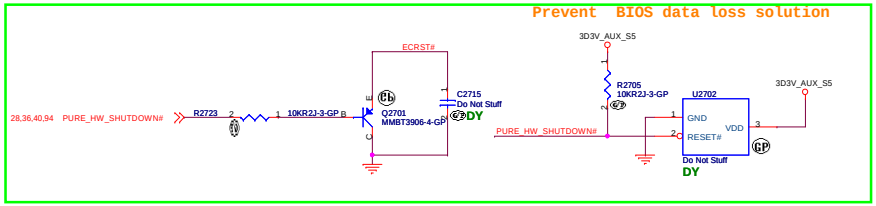
PCB Version A/D (PIN 98)		Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_KBC)	Voltage
Reserved	14"	100K	174K	1.2V
	15"		215K	1.04V
Reserved	14"			
	15"			
Reserved	14"			
	15"			
Reserved	14"			
	15"			

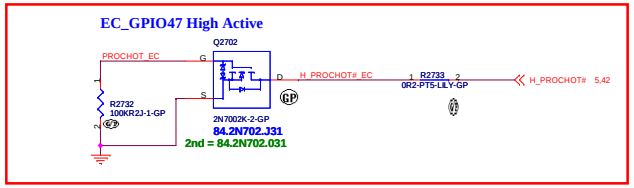
PCB Ver.

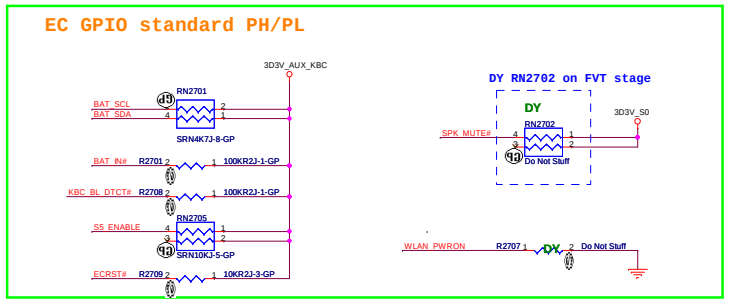


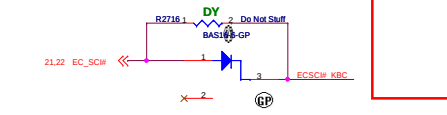
NOTE:
PWM Signal :
1. If unused, select altrnative GPIO function and enable internal pull-down.
2. Please measure and make sure that the rise time of VCC_POR is less than 10us.

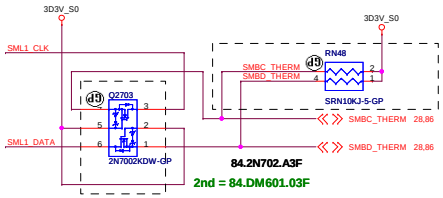
NOTE:
Please be aware that the SPI interface trace length between PCH and EC should not exceed 6500mils,. The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

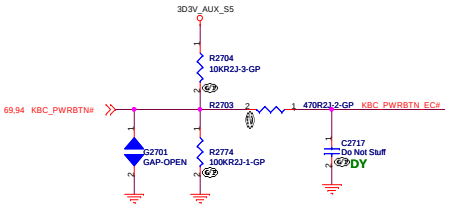












ASM for ISSC function ECR105692

12/09 change

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795

Size	Document Number	Rev
A2	CD1 DIS	SC

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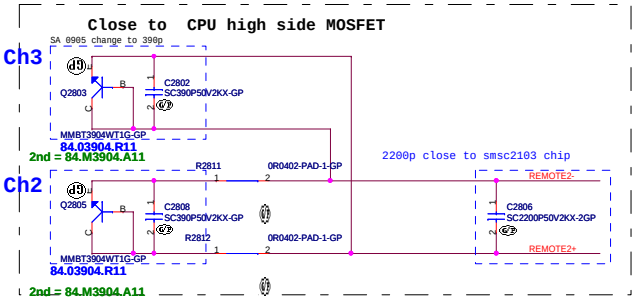
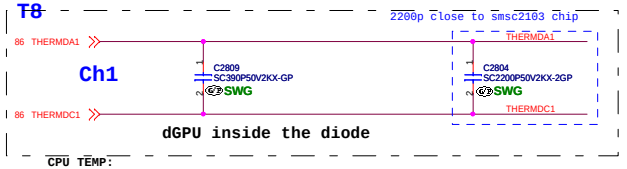
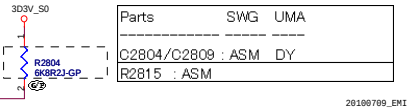
SSID = Thermal

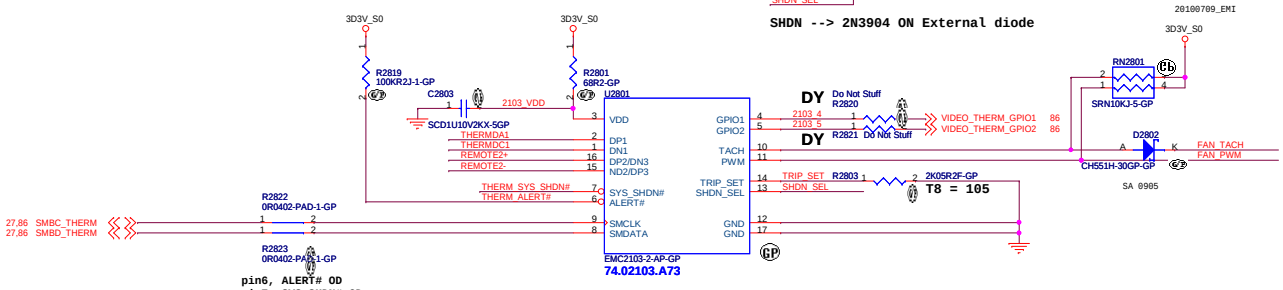
Thermal sensor

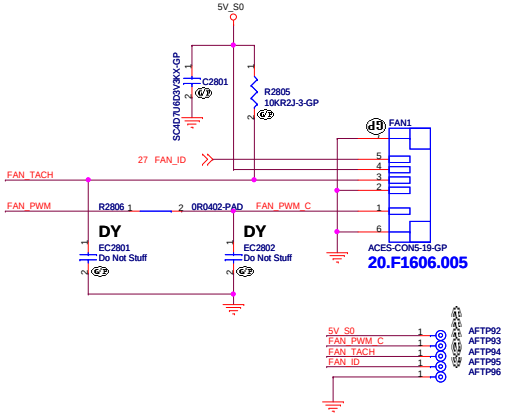




9/2 Thermal Fun.		
Parts	SWG	UMA
C2804/C2809 : ASM		DY
R2815 : ASM		







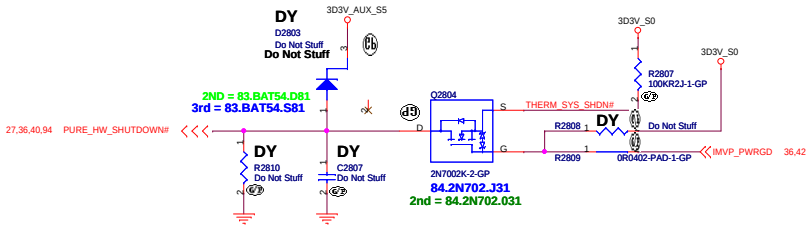
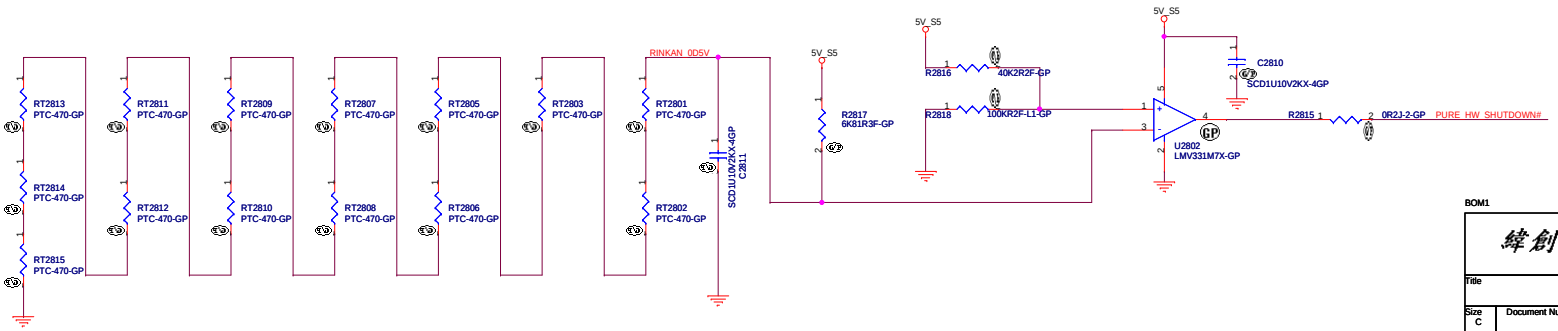


Table 28.1- General Purpose Transistors multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ON	MMBT3904WT1G	N/A	84.03904.R11
PANJIT	MMBT3904W	N/A	84.M3904.A11



BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal/FAN*

Size	Document Number	Rev
C	CD1 DIS	SC

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9/26 change to S0

All Power Line(VDD,AVDD,PVDD,REF etc) must wide trace [20mil]

6-10 mil trace recommend

All audio analog signal must trace with min 10mil width

SPKR trace width 40 mils---4ohm speaker recommend 40,mil, required 20mil.as min

Close to Pin 47.

PLACE NEAR CODEC

PLACE NEAR CODEC

Place under or under ALC3202

Layout Note: place R9500 and R9501 near dock conn

U2901

Analog

Digital

ALC3202-GR-GP

USE SHAPE

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

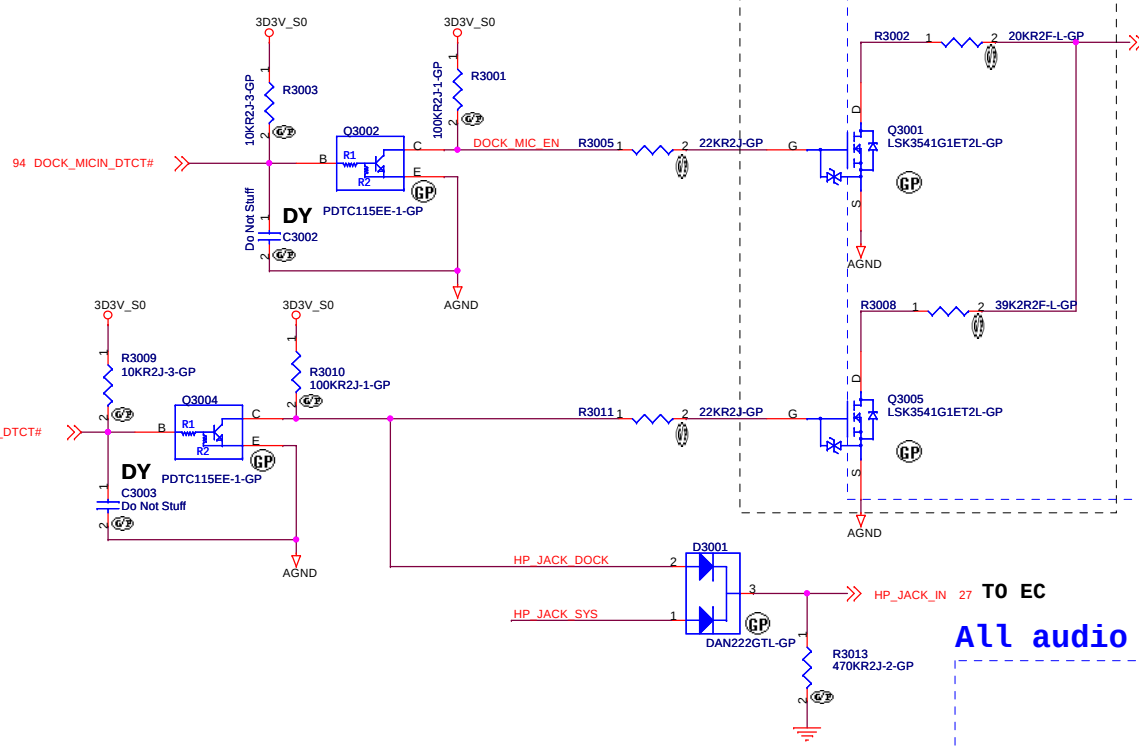
Title: Audio Codec ALC3202

Size: A2 | Document Number: CD1 DIS | Rev: SC

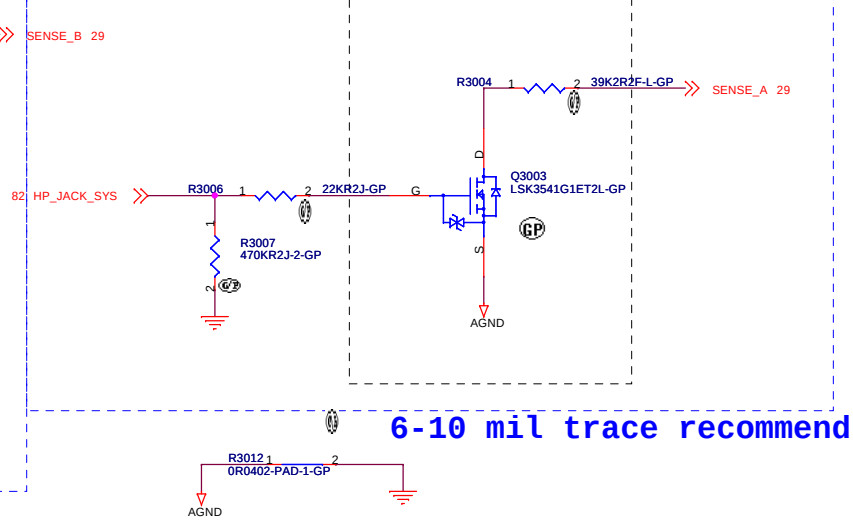
Date: Tuesday, December 13, 2011 | Sheet 29 of 102

6-10 mil trace recommend

CLOSE TO CODEC

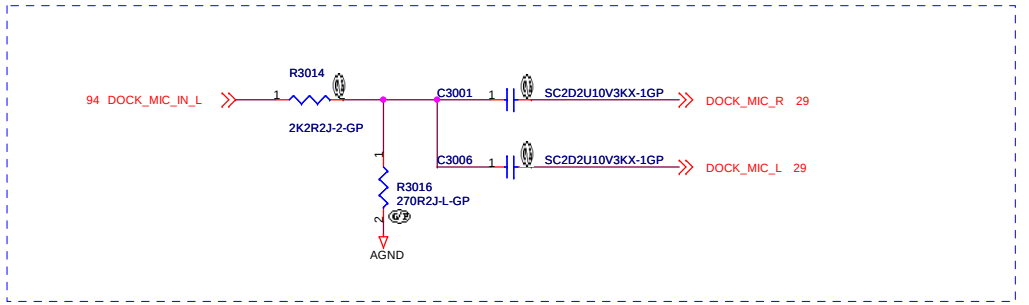


CLOSE TO CODEC

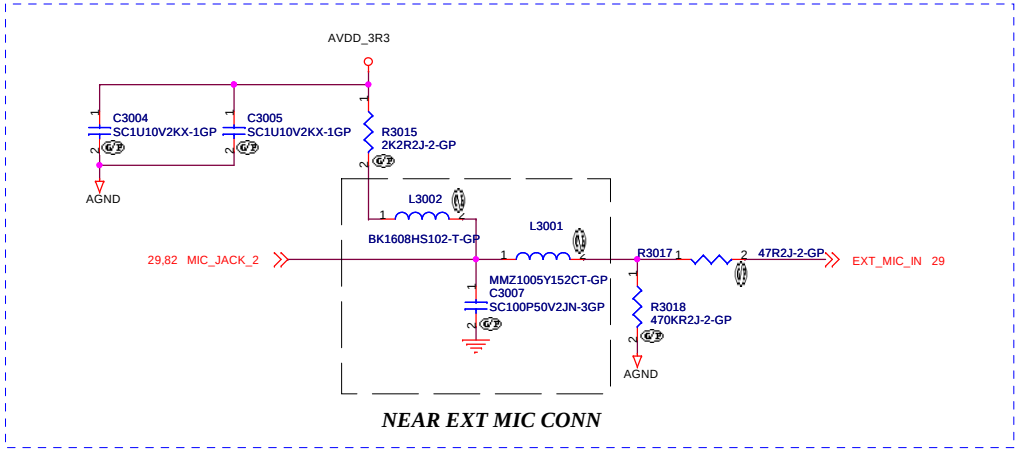


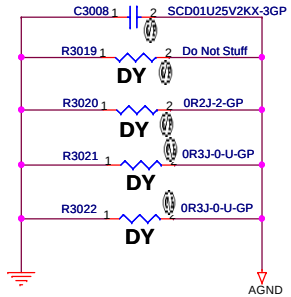
6-10 mil trace recommend

All audio analog signal must trace with min 10mil width



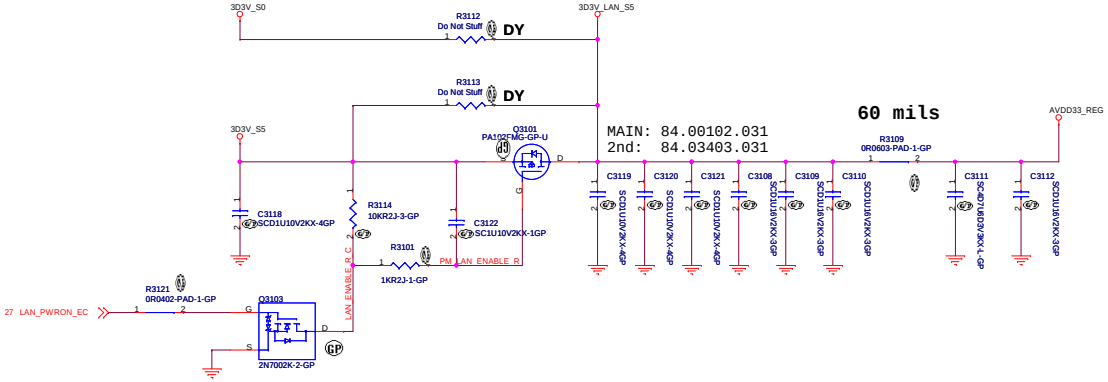
All audio analog signal must trace with min 10mil width

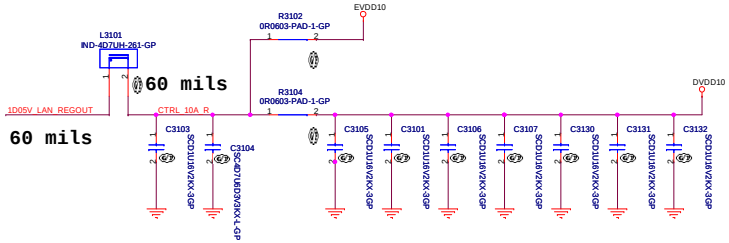




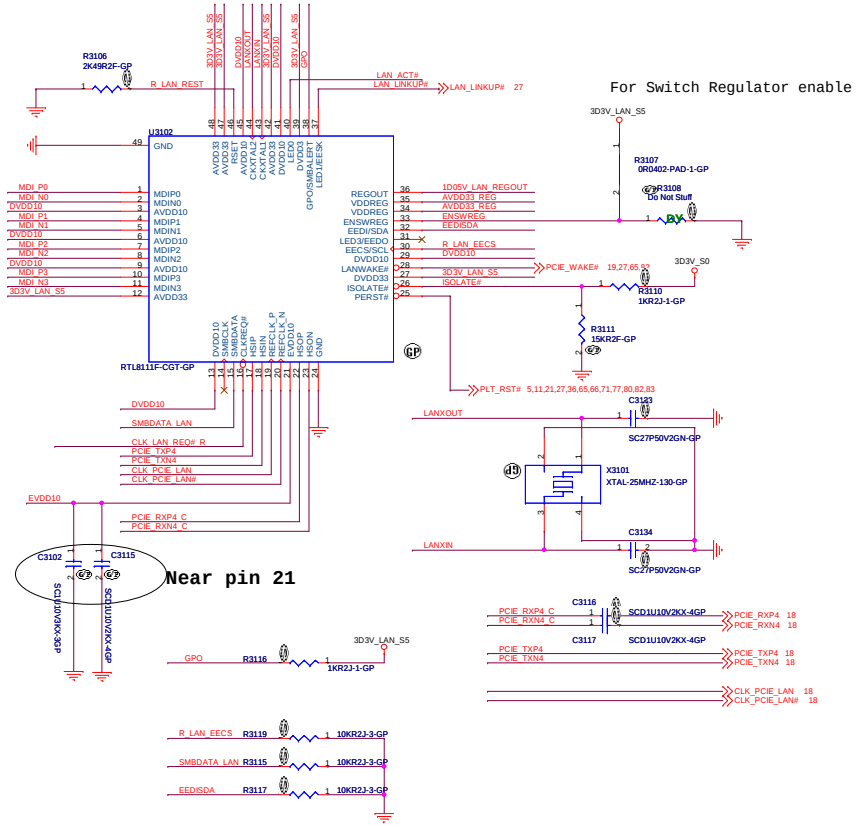
BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Speaker Conn		
Size: A3	Document Number: CD1 DIS	Rev: SC
Date: Tuesday, December 13, 2011	Sheet 30 of 102	

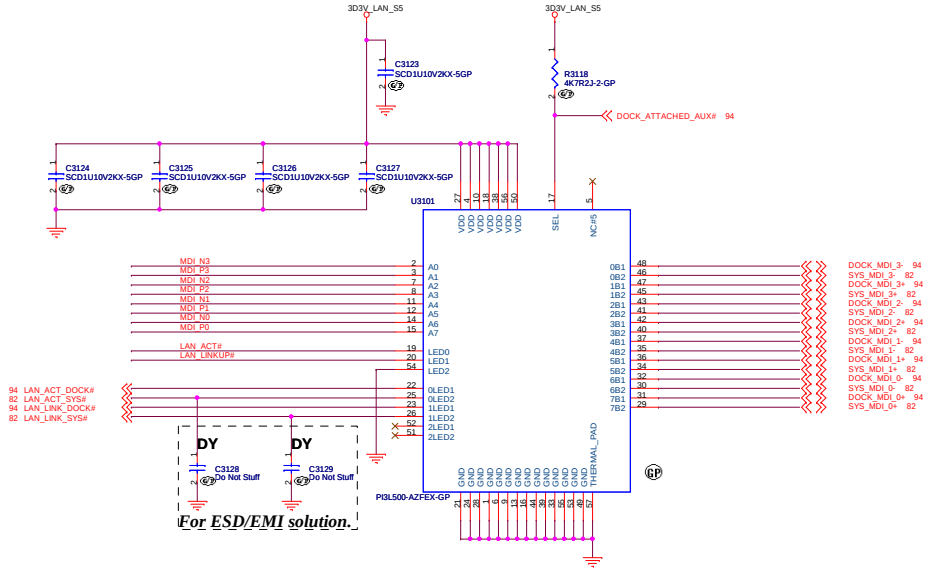




LAN CHIP



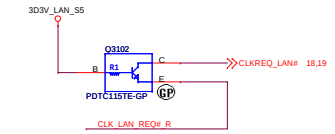
For Switch Regulator enable



For ESD/EMI solution.

[Source Cadidate]				
1st	Pericom	PI3L500AZFEX	73.3L500.003	41R0539AA
2nd	TI	TS3L500AERHUR	73.3L500.A0V	41R0539BA
3th	ONSEMI	NS3L500MTTWG	73.03500.003	

Isolate between PCH S5-Power and LAN Power(3D3V_LAN_S5) leakage.



BOM1

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Title: **LOM_RTL8111F**

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BOM1

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Title: *Reserved*

Size	Document Number	Rev
A3	CD1 DIS	SC

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BOM1

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Title: ***Reserved***

Size	Document Number	Rev
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BOM1

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Title: ***Reserved***

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BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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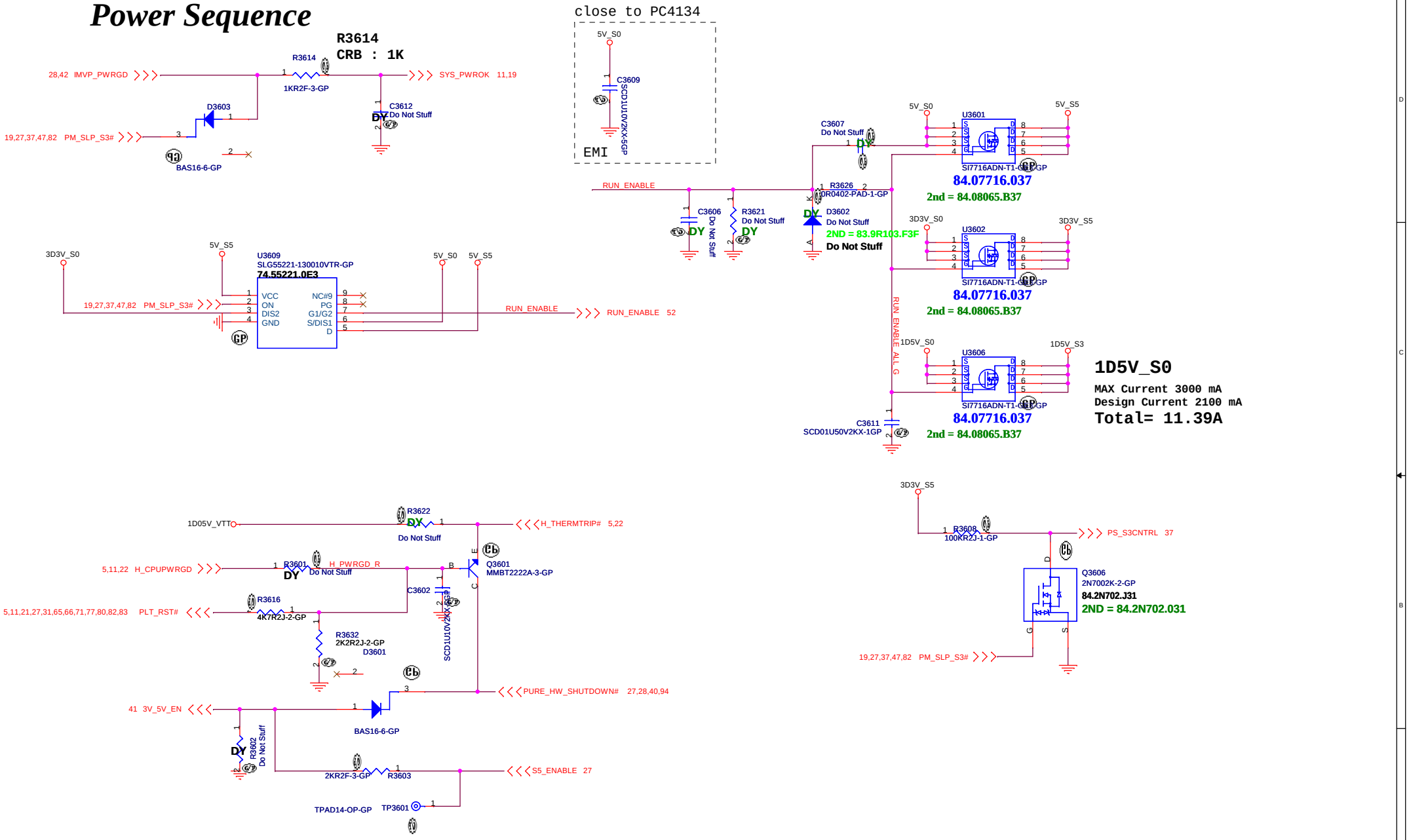
Power Sequence



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size	Document Number	Rev
A3	CD1 DIS	SC

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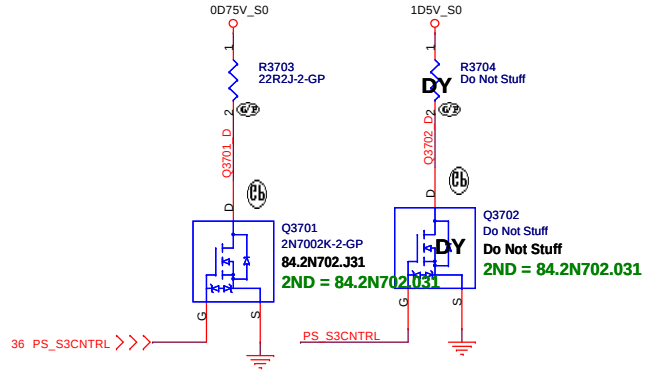
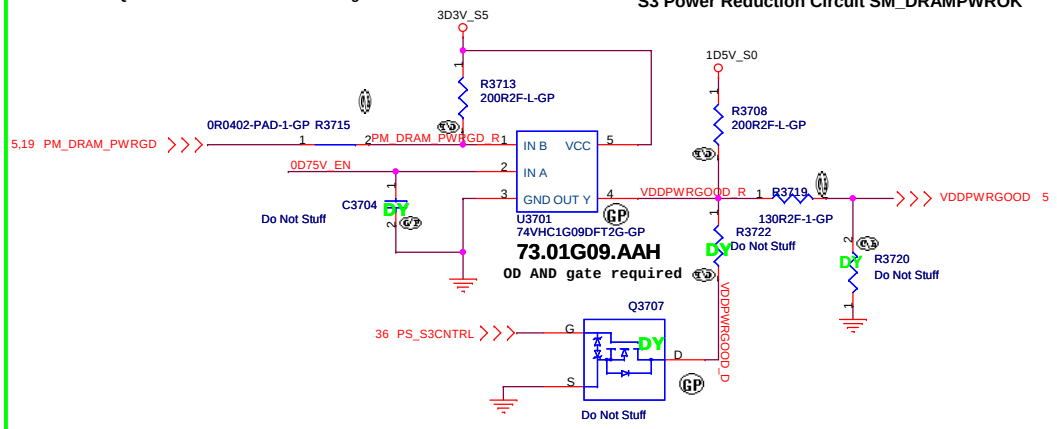
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

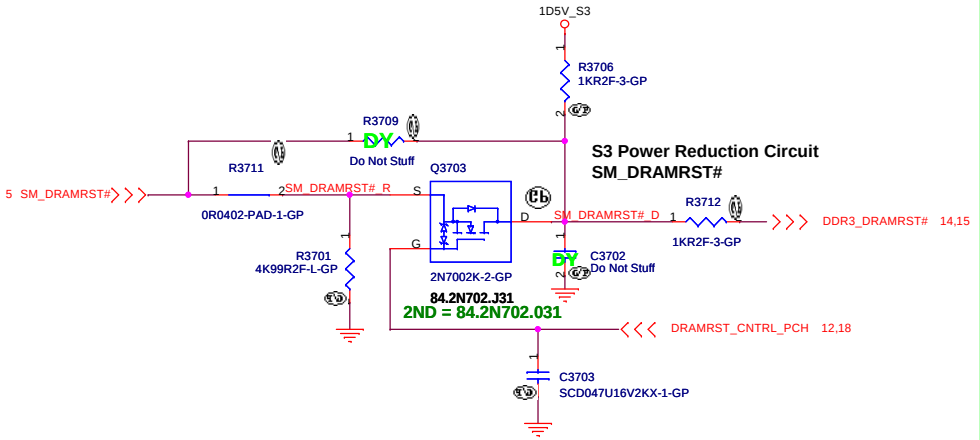


SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

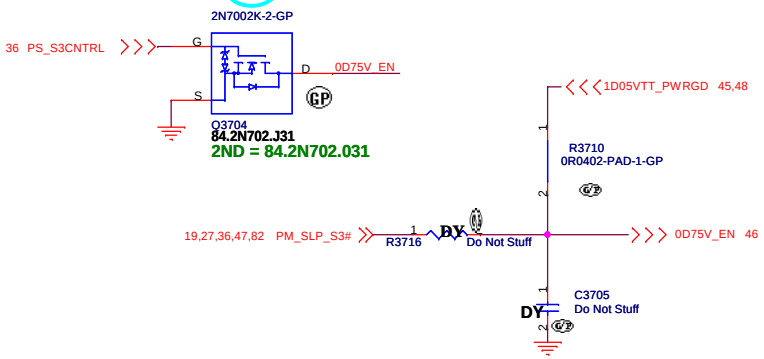
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMRST#



5 S3 Power Reduction



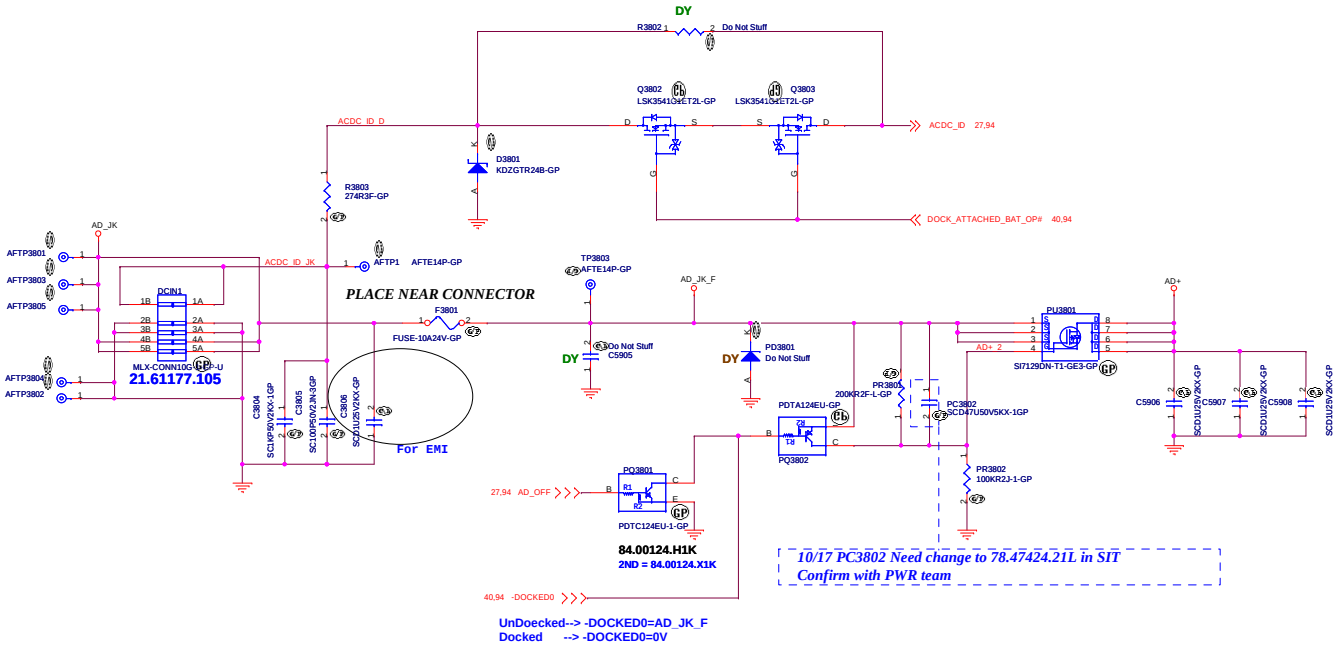
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

Size	Document Number	Rev
A3	CD1 DIS	SC

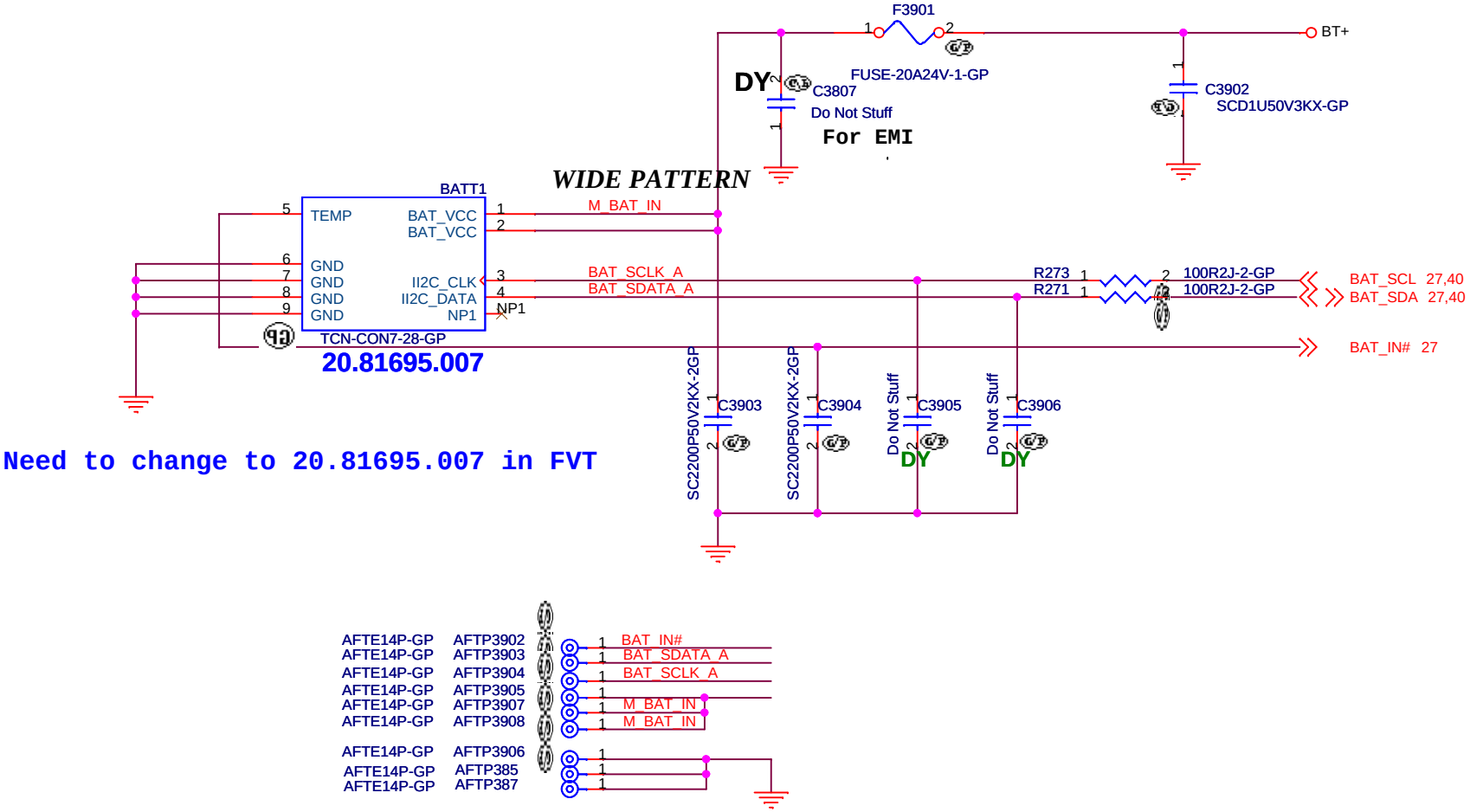
Date: Tuesday, December 13, 2011 Sheet 37 of 102



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DCIN JACK		
Size: A2	Document Number: CD1 DIS	Rev: SC
Date: Tuesday, December 13, 2011	Sheet 38 of 102	

BATT Connecter



Need to change to 20.81695.007 in FVT

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BATT CONN***

Size	Document Number	Rev
A4	CD1 DIS	SC

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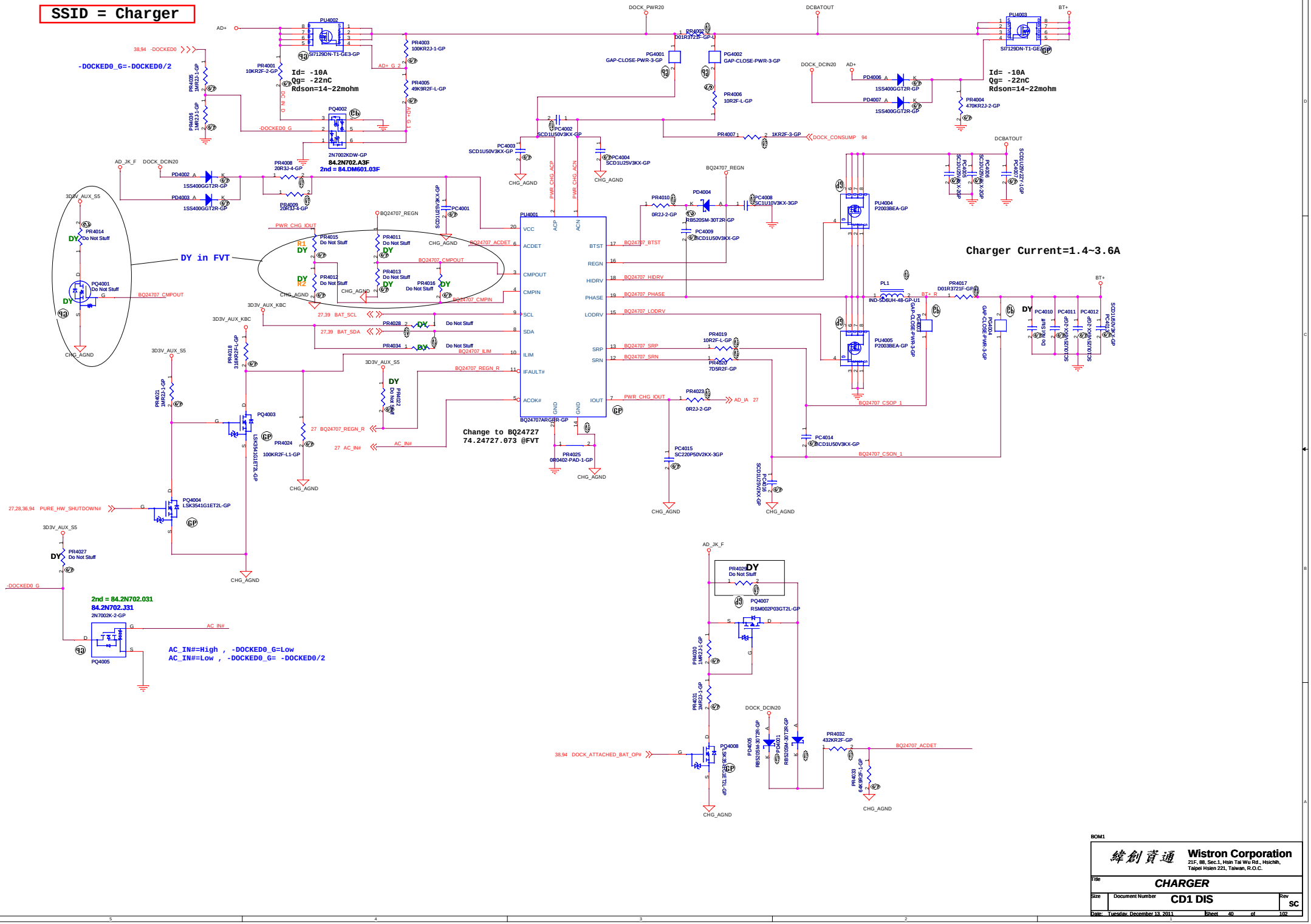
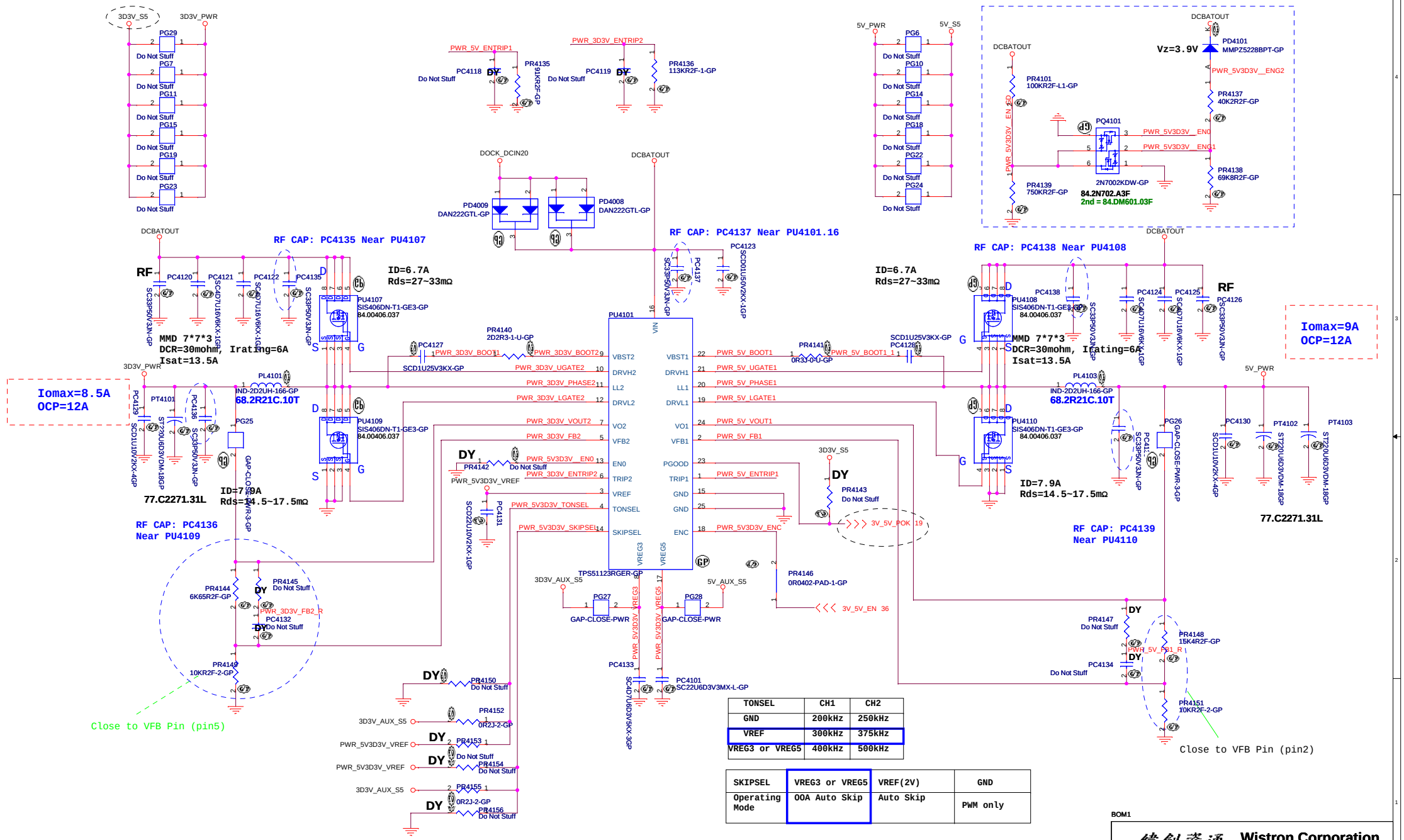
SSID = Charger



Confirm PWR for PQ4101 circuit Fun. (FVT Stage)



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

BOM1

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Title: TPS51123_5V/3D3V

Size: Custom | Document Number: CD1 DIS | Rev: SC

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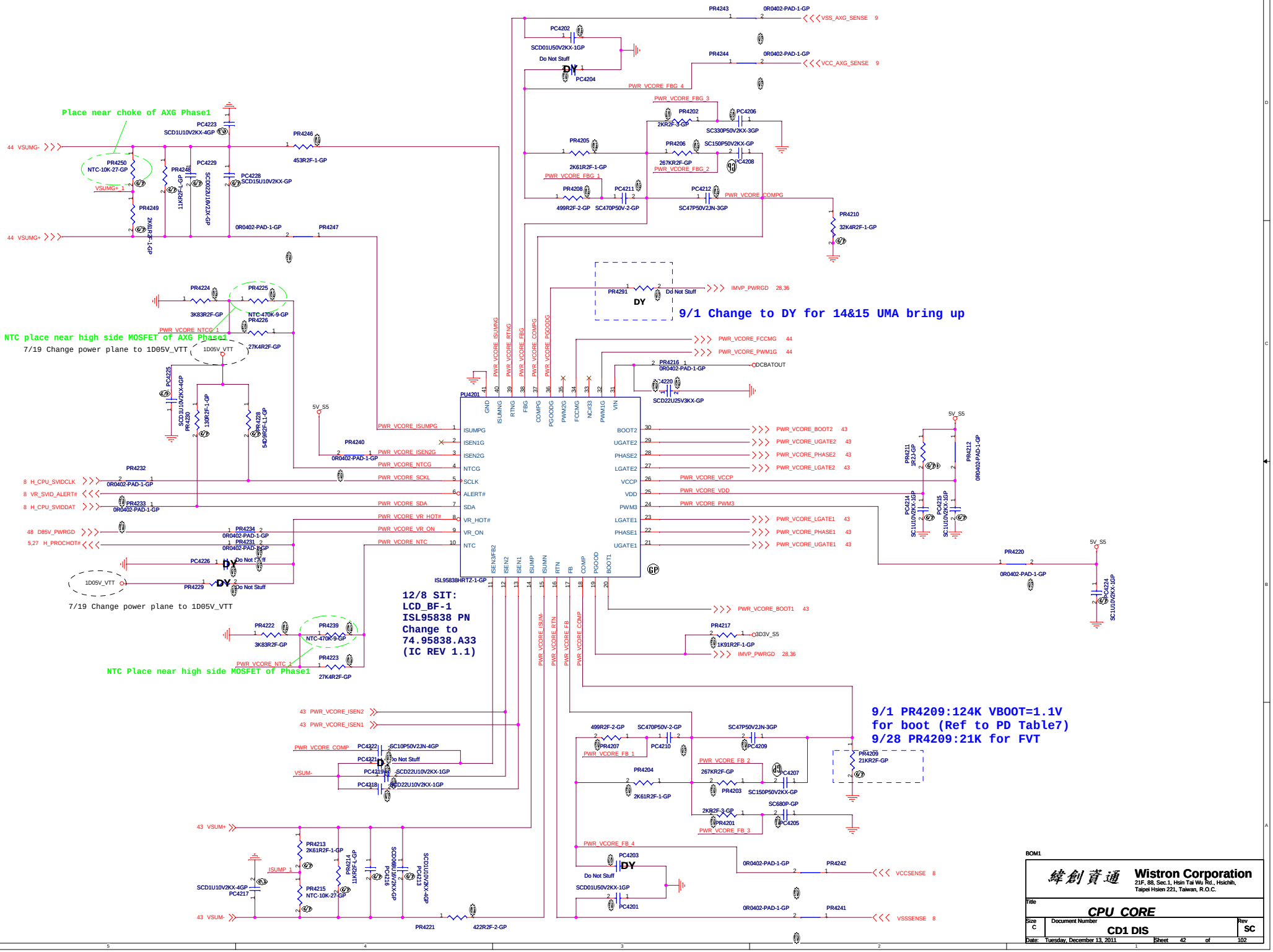
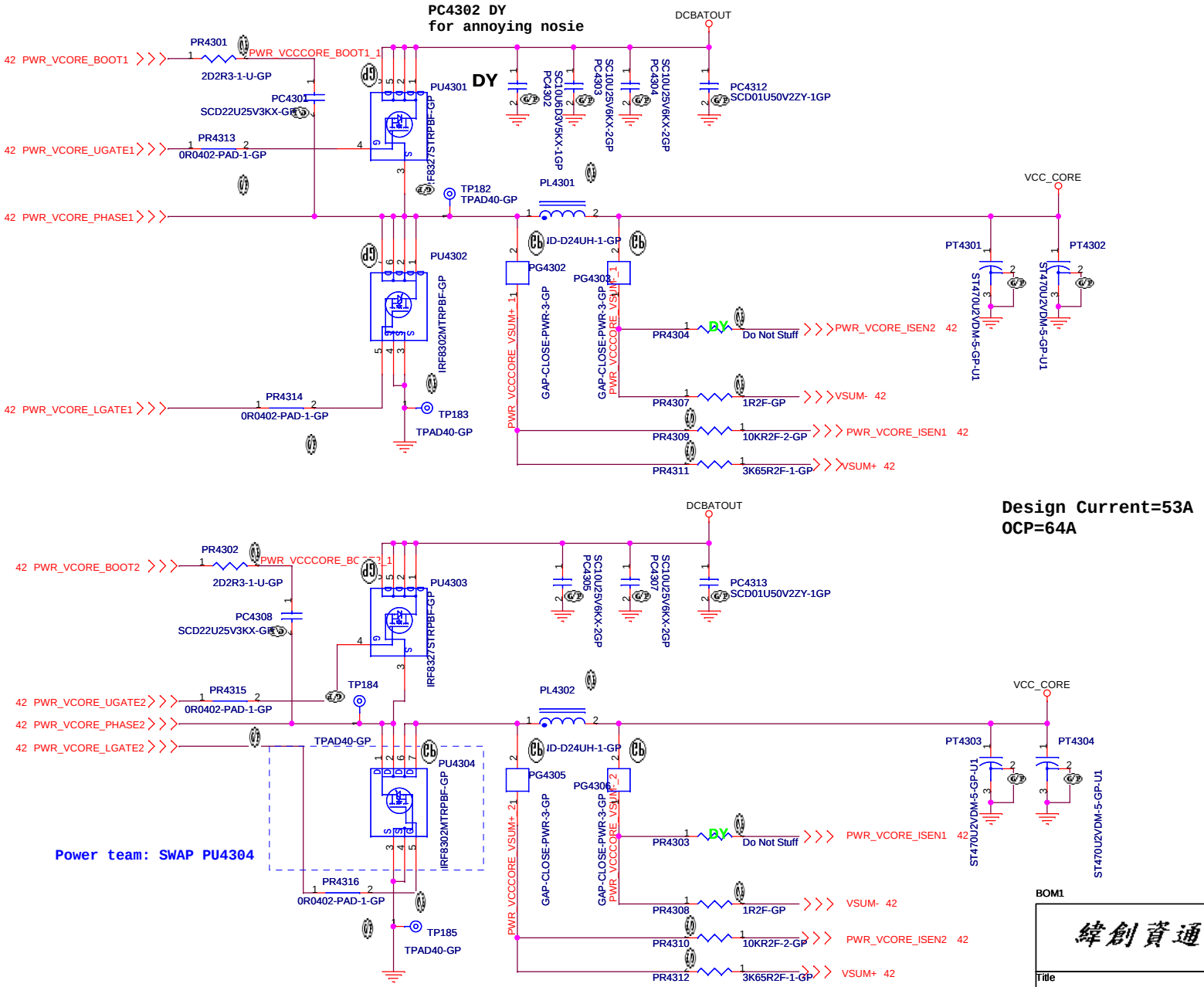

Place near choke of AXG Phase1
NTC place near high side MOSFET of AXG Phase1
7/19 Change power plane to 1D05V_VTT
7/19 Change power plane to 1D05V_VTT
NTC Place near high side MOSFET of Phase1
9/1 Change to DY for 14&15 UMA bring up
12/8 SIT:
LCD_BF-1
ISL95838 PN
Change to
74.95838.A33
(IC REV 1.1)
9/1 PR4209:124K VBOOT=1.1V
for boot (Ref to PD Table7)
9/28 PR4209:21K for FVT
PU4201
ISL95838HRTZ-1-GP
Do Not Stuff
DY
BOM1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU_CORE
Size C
Document Number
CD1 DIS
Rev SC
Date: Tuesday, December 13, 2011
Sheet 42 of 102



BOM1

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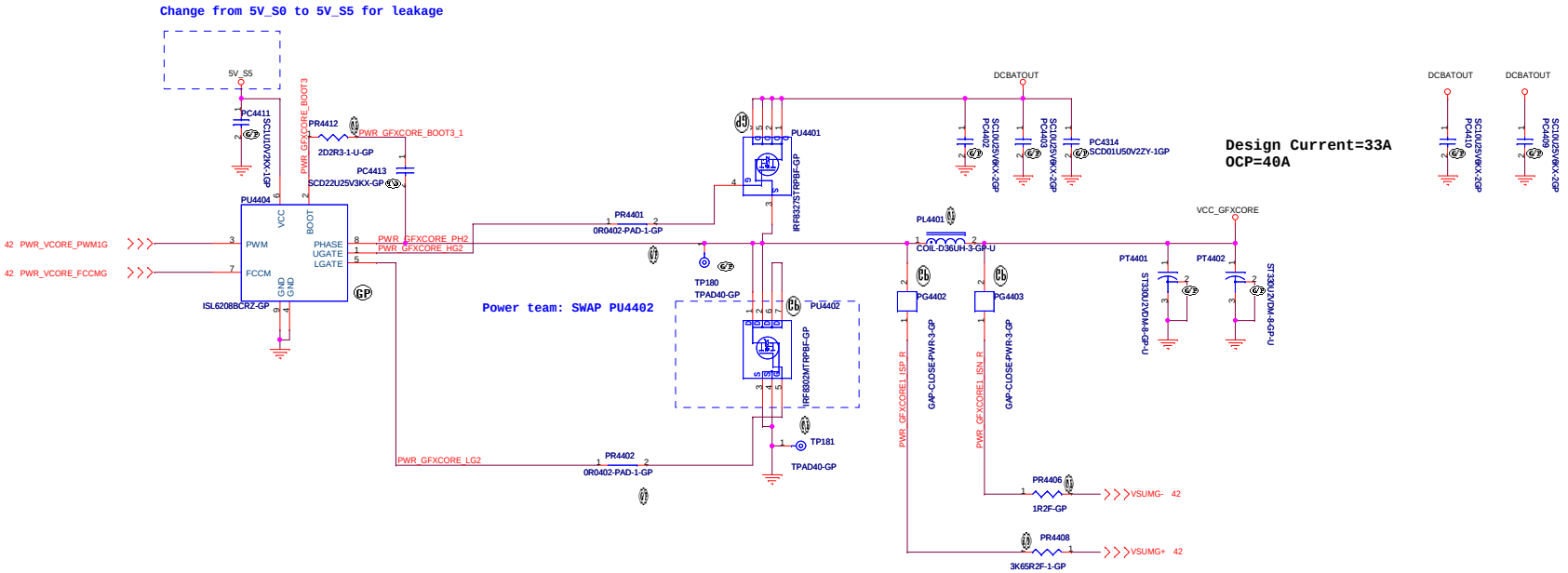
Title: **CPU CORE**

Size	Document Number	Rev
B	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 43 of 102

SSID = AXG.Regulator



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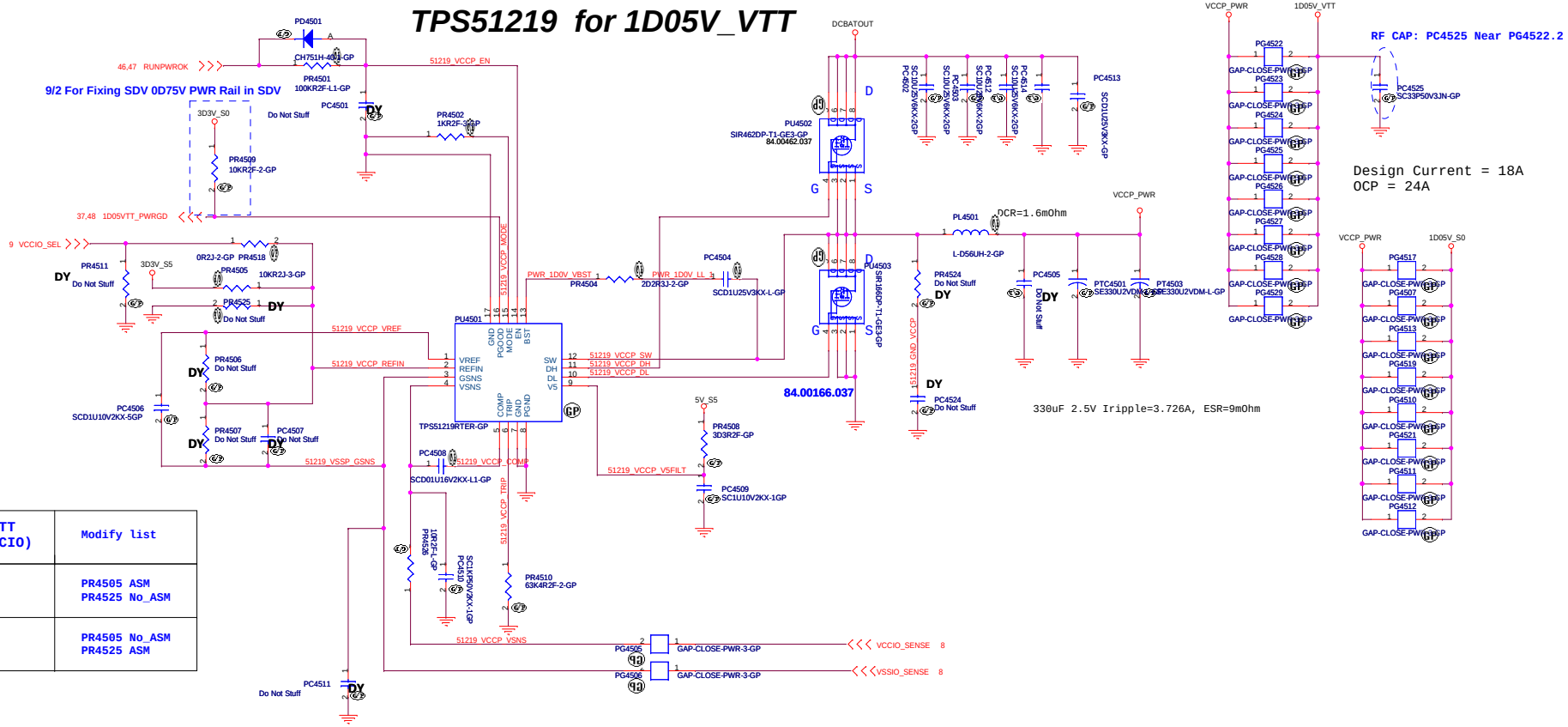
Title: CPU_CORE

Size	Document Number	Rev
C	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 44 of 102

TPS51219 for 1D05V_VTT



1D05V_VTT (CPU VCCIO)	Modify list
1.05V	PR4505 ASM PR4525 No_ASM
1.0V	PR4505 No_ASM PR4525 ASM

BOM1

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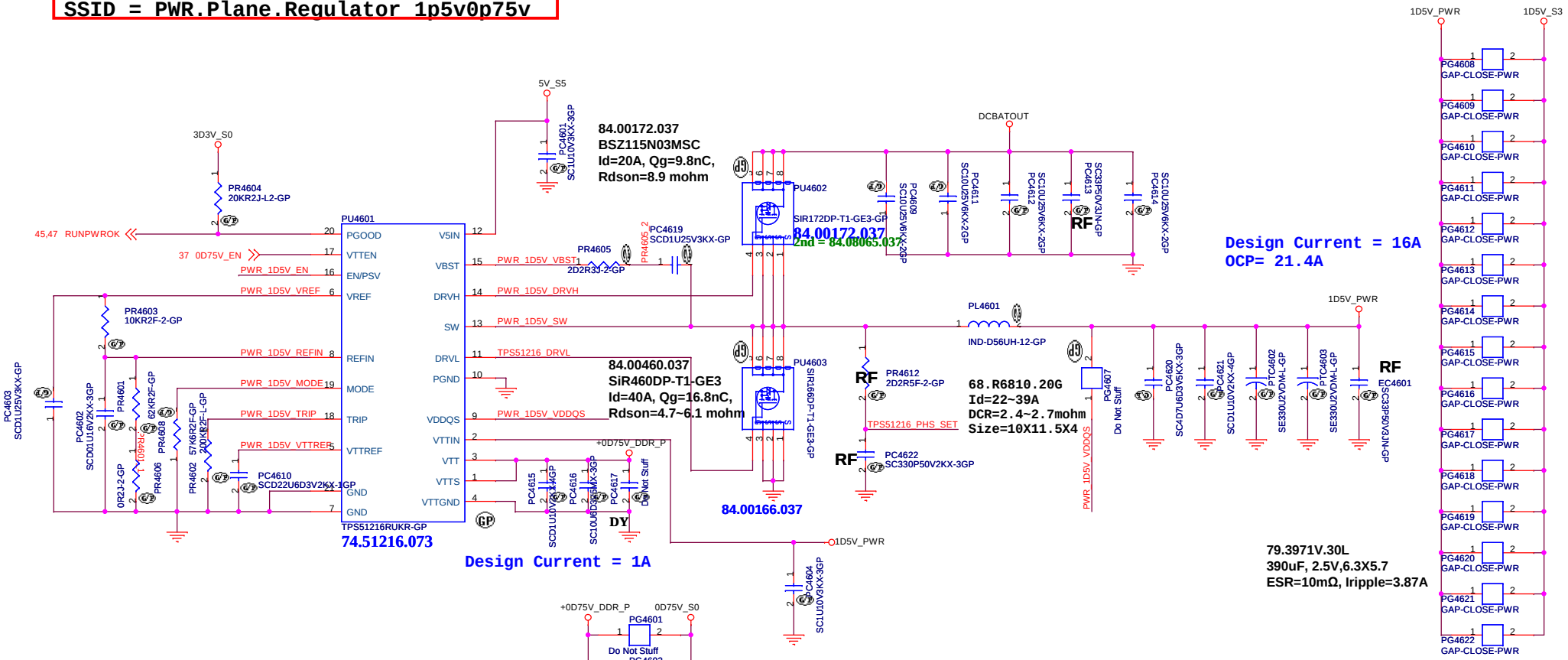
Title: TPS51219_1D05V

Size | Document Number | Rev: SC

Date: Tuesday, December 13, 2011 | Sheet 45 of 102

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR5003	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

BOM1

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Title: ***TPS51216_1D5V&0D75V***

Size	Document Number	Rev
A3	CD1 DIS	SC

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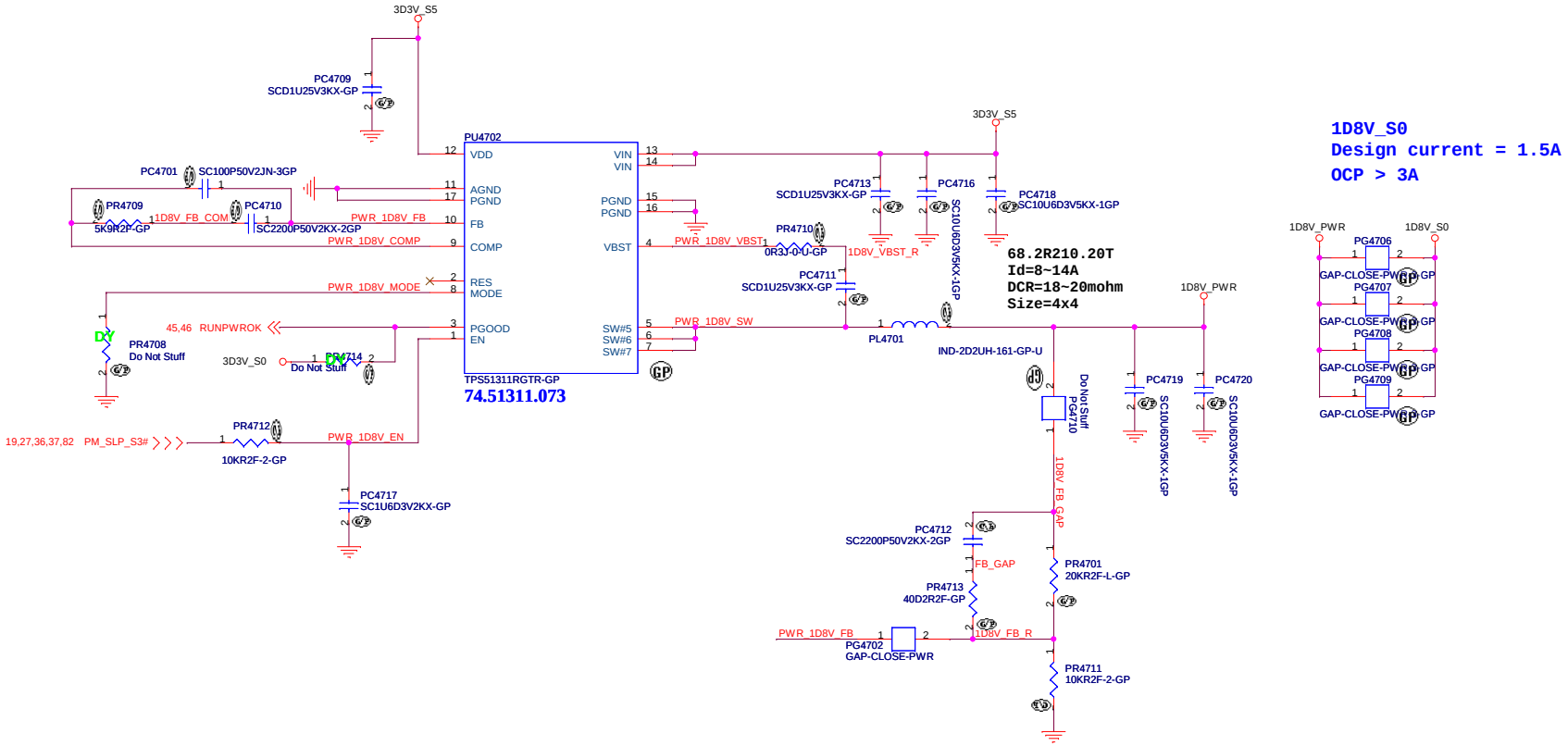
TPS51311 for 1D8V_S0



1D8V_S0
Design current = 1.5A
OCP > 3A

BOM1

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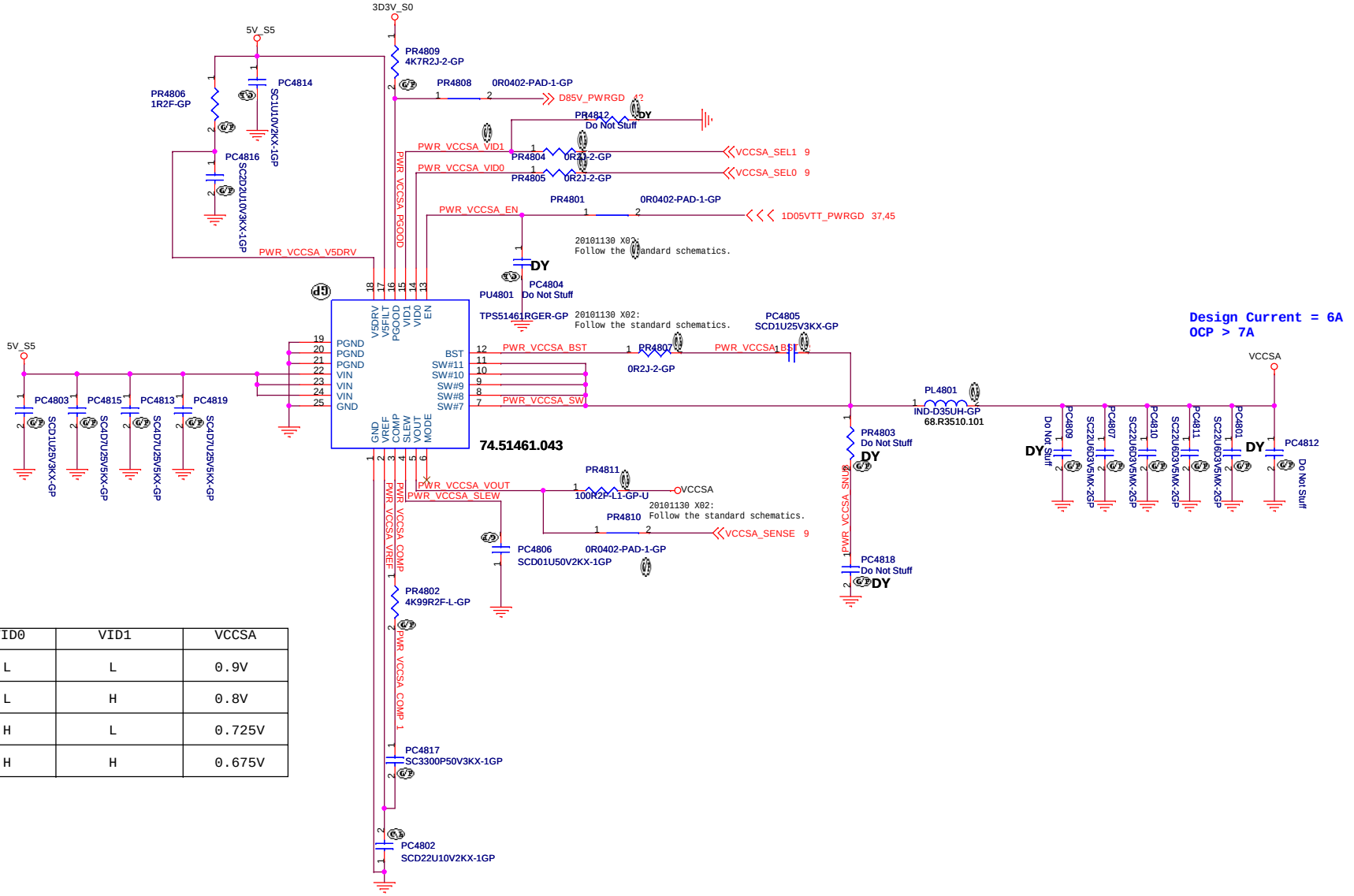
Title: *PWM_1D8V_RT8015B*		
Size	Document Number: **CD1 DIS**	Rev: SC
Date: Tuesday, December 13, 2011	Sheet 47 of 102	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

BOM1

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Title: VCCSA_TPS51461

Size | Document Number | Rev: SC

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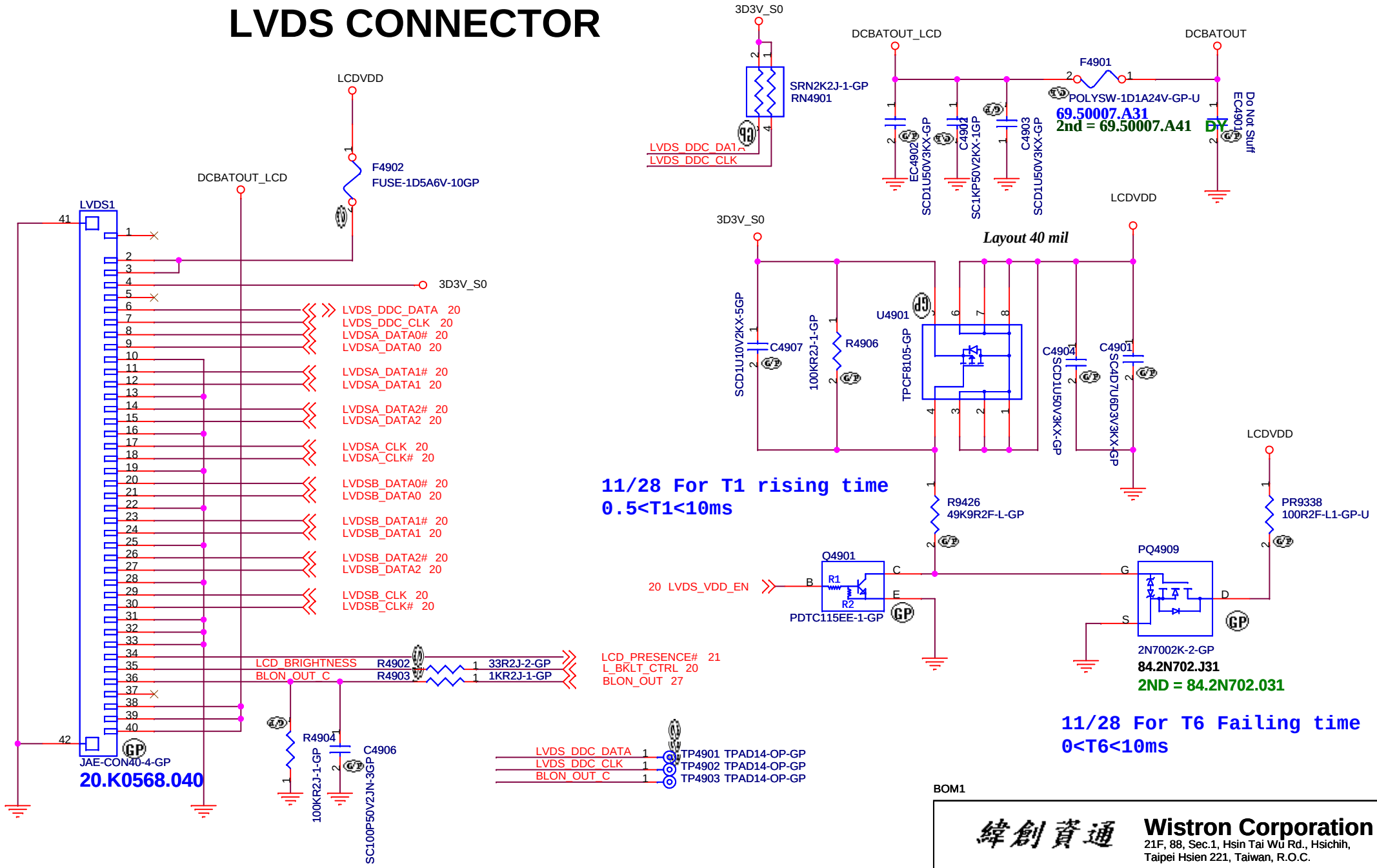
LVDS CONNECTOR



BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LCD Connector***	
Size A4	Document Number **CD1 DIS**	Rev **SC**
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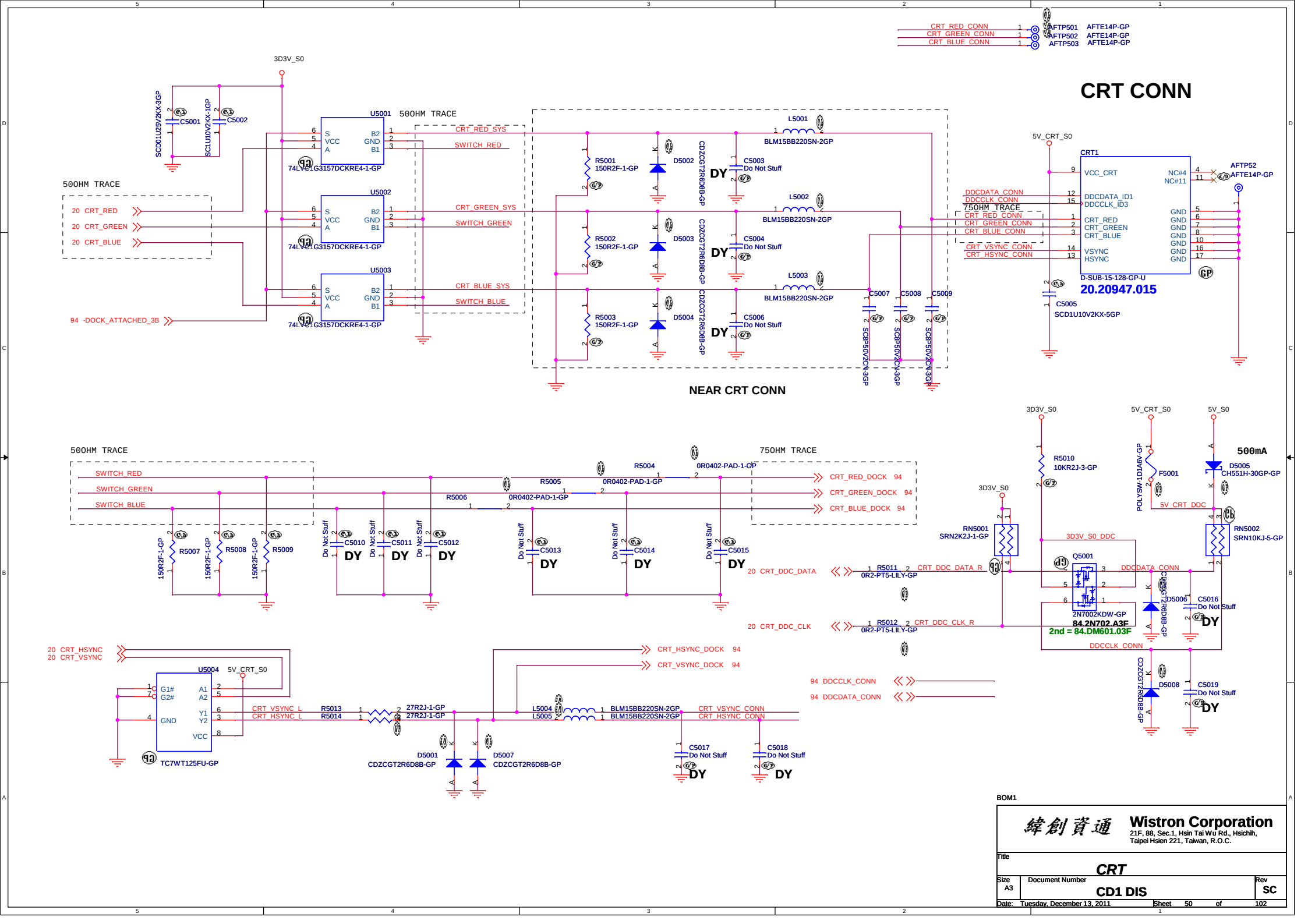
CRT CONN



BOM1

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Title	***CRT***	
Size A3	Document Number **CD1 DIS**	Rev **SC**
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BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	CD1 DIS	SC

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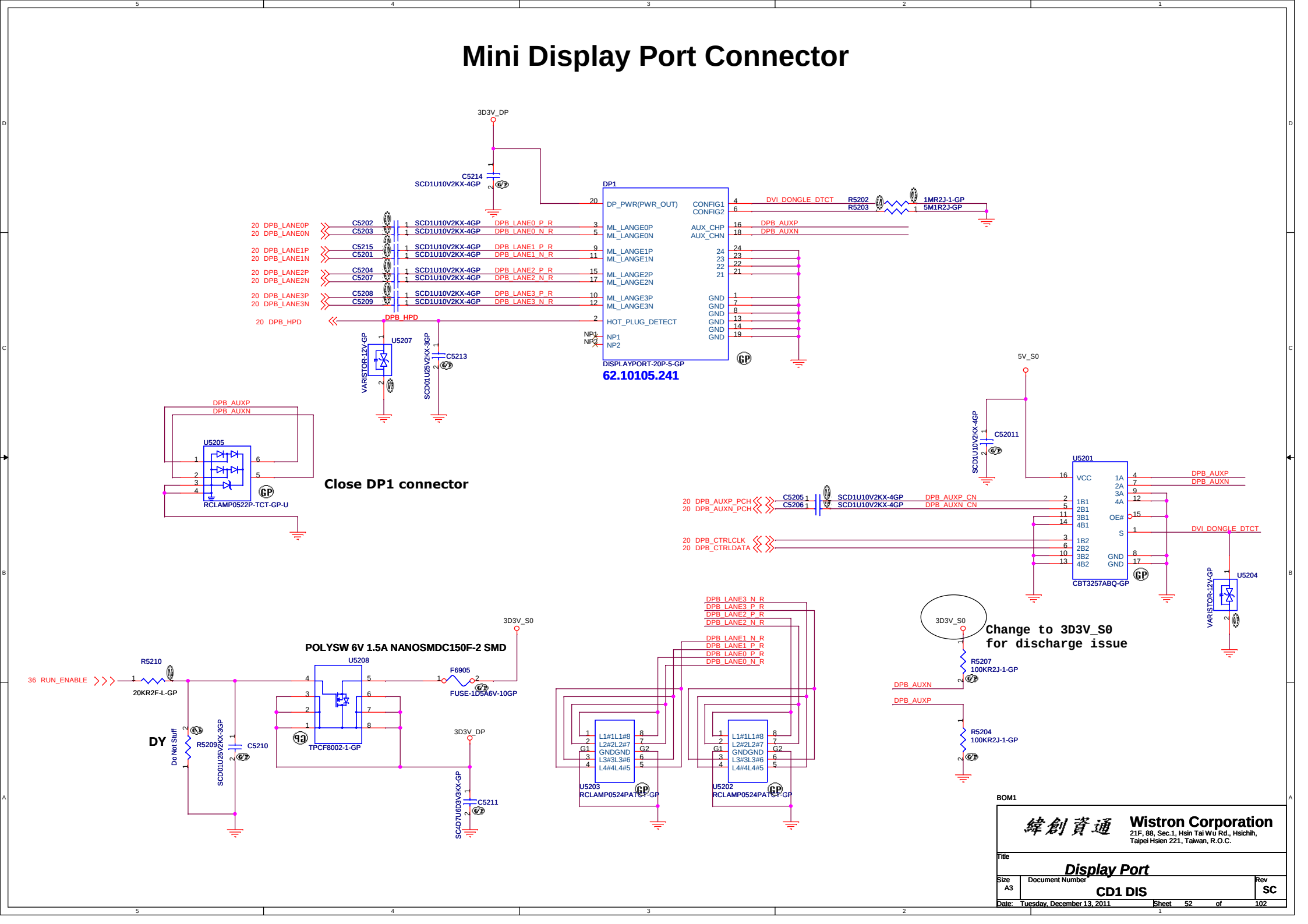
Mini Display Port Connector



BOM1

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Title: ***Display Port***		
Size: A3	Document Number: **CD1 DIS**	Rev: SC
Date: Tuesday, December 13, 2011	Sheet 52 of 102	

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BOM1

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

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BOM1

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Title: ***Reserved***

Size	Document Number	Rev
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BOM1

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Title: ***Reserved***

Size	Document Number	Rev
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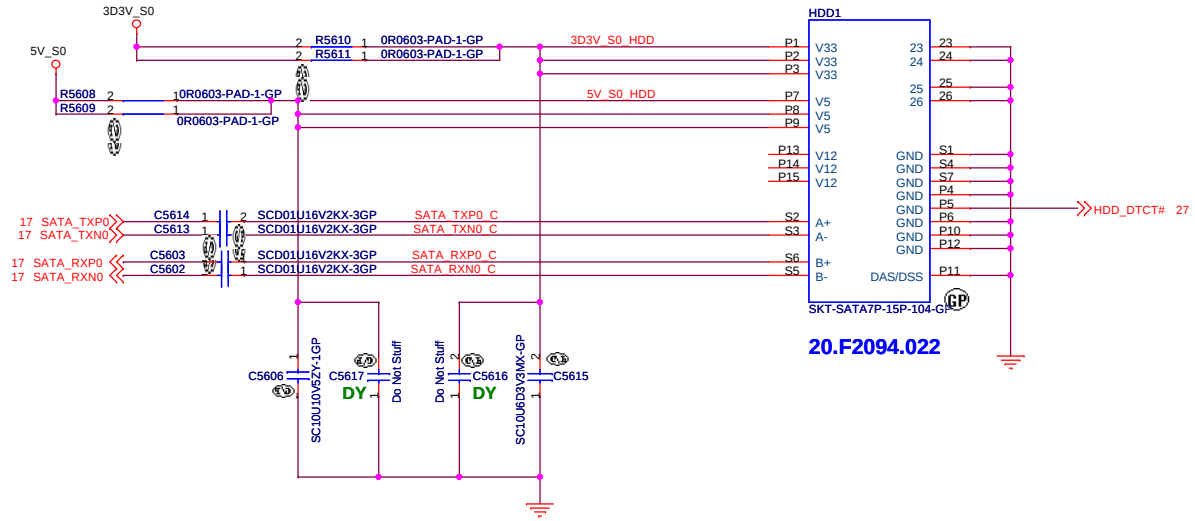
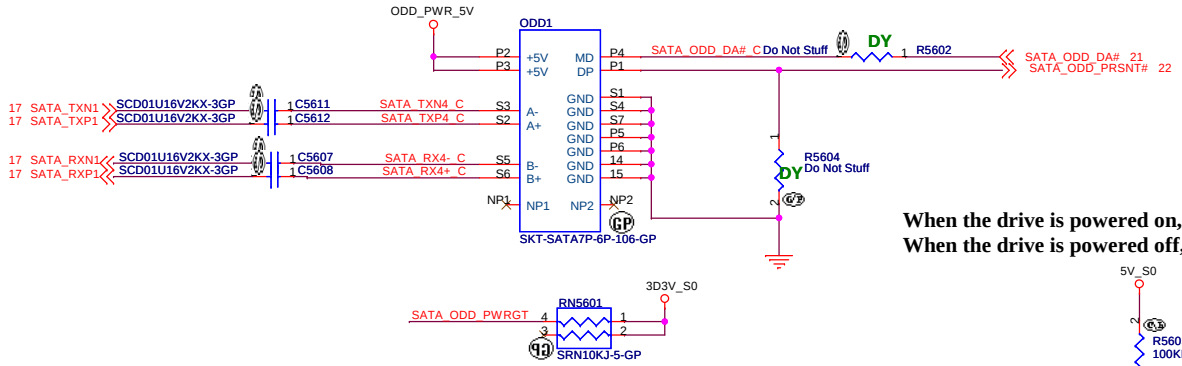
SATA HDD Connector

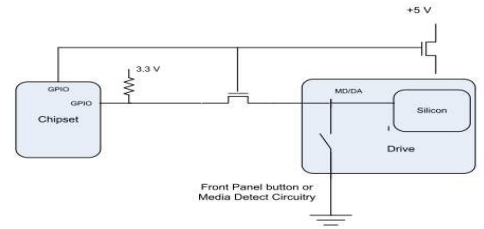


ODD Connector

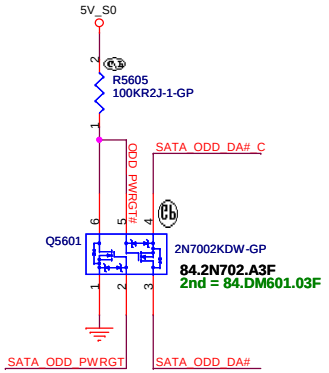
SATA_RX- and SATA_RX+ Trace Length match within 20 mil



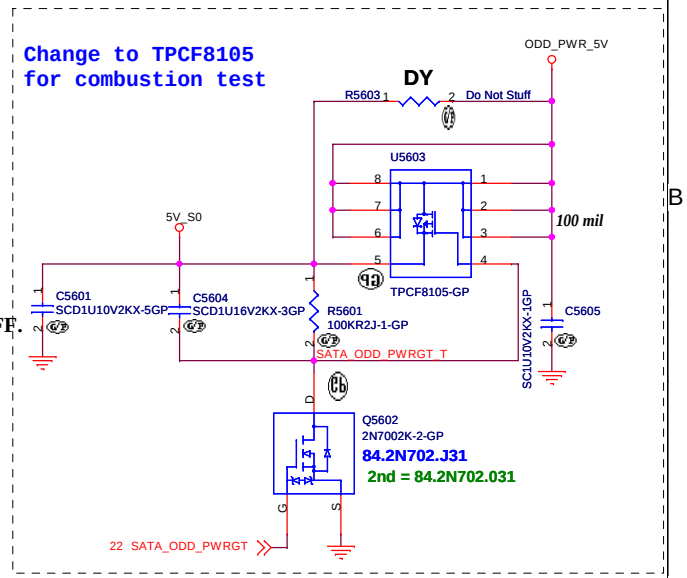
SUPPORT ZERO SATA ODD



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



SATA Zero Power ODD



BOM1

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Title: **HDD/ODD**

Size	Document Number	Rev
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BOM1

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Title: ***RESERVED***

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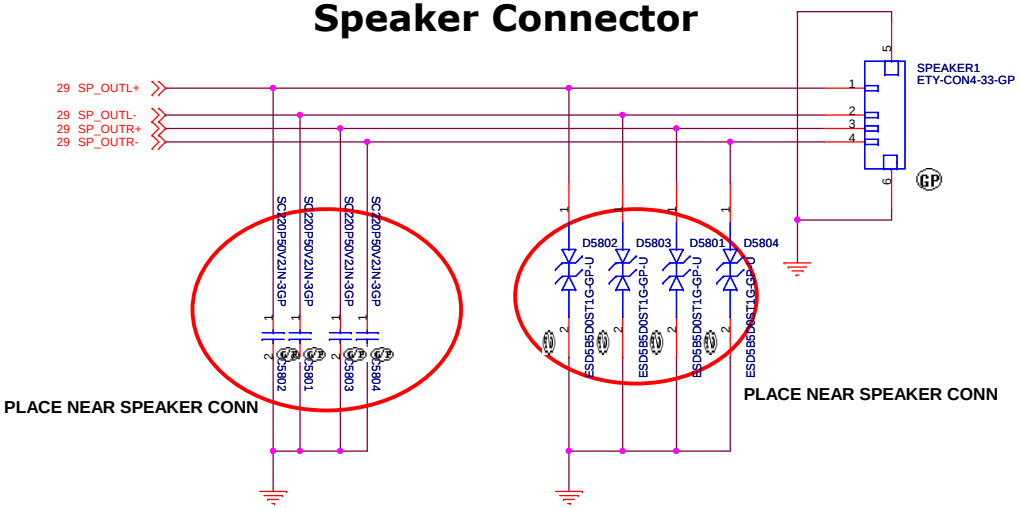
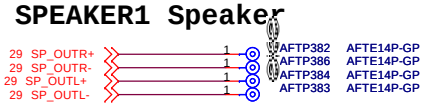
Speaker Connector



Near SPEAKER1 Speaker



BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SPEAKER CONN***

Size	Document Number	Rev
A3	CD1 DIS	SC

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BOM1

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Title: ***Reserved***

Size	Document Number	Rev
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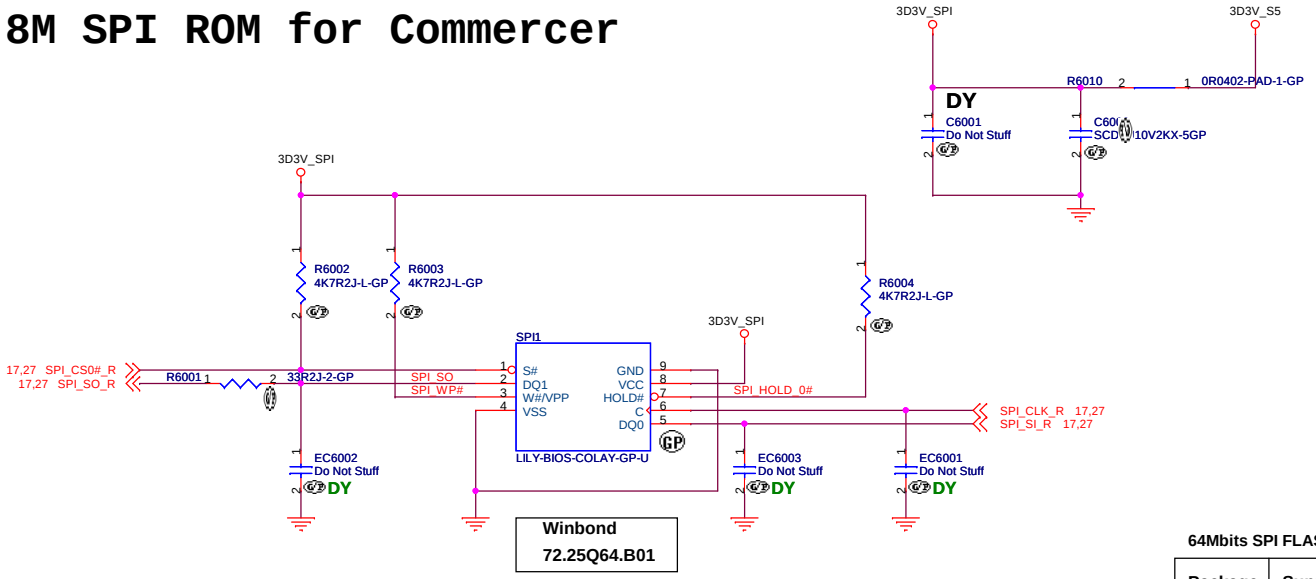
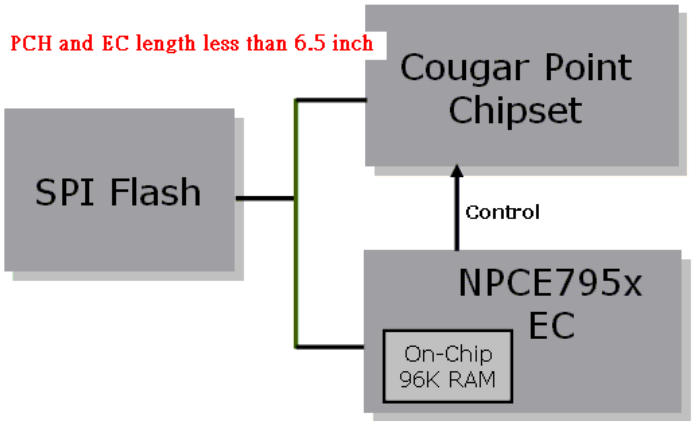
SSID = Flash.ROM

8M SPI ROM for Commercer



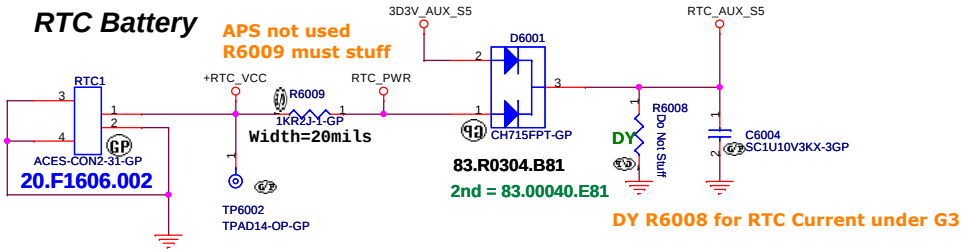
Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

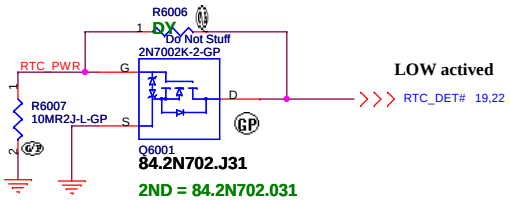


64Mbits SPI FLASH (SPI1):

Package	Supplier	Vendor P/N	Wistron P/N
SO8	Macronix	MX25L6406EM2I-12G	72.25640.D01
	Winbond	W25Q64CVSSIG	72.25Q64.B01
	Numonyx	N25Q064A13ESE40F	72.25Q64.D01

SSID = RBATT





BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

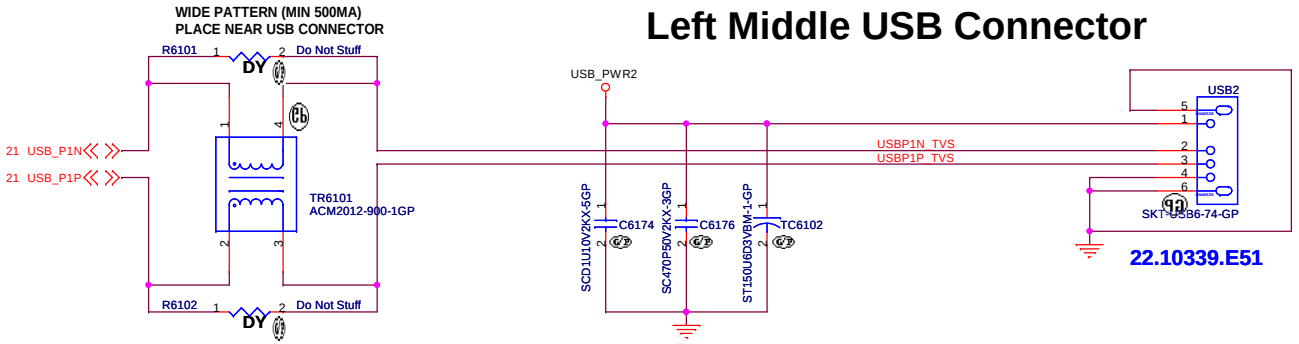
Title: *Flash/RTC*

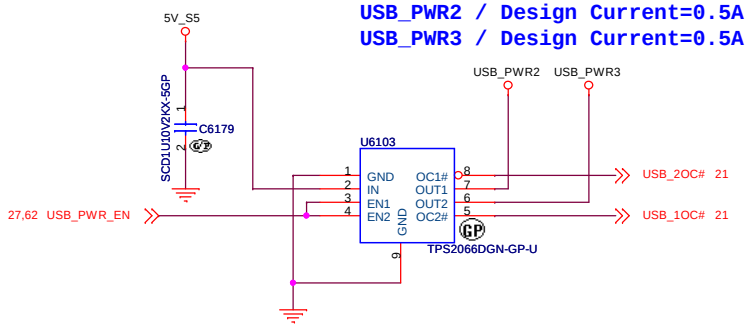
Size: A3 | Document Number: CD1 DIS | Rev: SC

Date: Tuesday, December 13, 2011 | Sheet 60 of 102

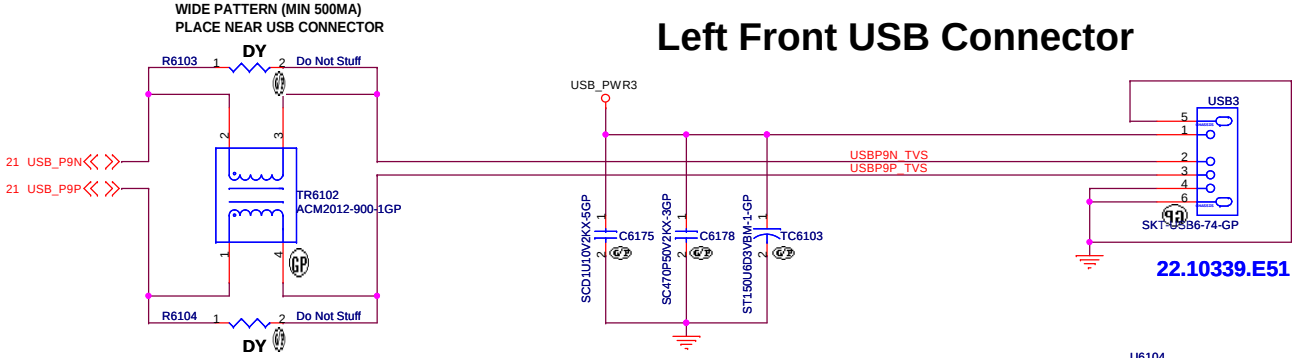
SSID = USB

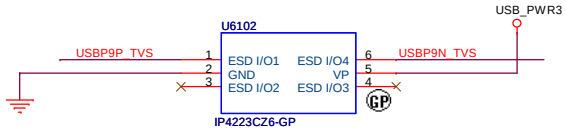
Left Middle USB Connector

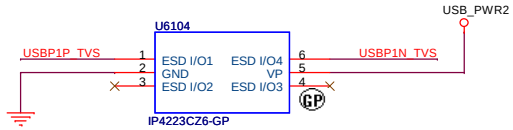




Left Front USB Connector







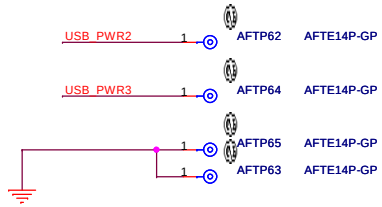


Table 61.1- USB2.0 PWR SW multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
TI	TPS2066DGN	41R0511AA	74.02066.A71
TI	TPS2066DGN-1	N/A	74.02066.B71

Table 61.2- 150U 6.3V POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NEC-TOKIN	TEPSLB20J157M	N/A	77.C1571.09L
SANYO	6TPE150MAZB	N/A	77.21571.111
HPC	TNCB0J157MTRZTF	N/A	80.15715.12L

Table 61.3- ESD protection

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	IP4223CZ6	N/A	83.42236.0AE
AOS	AOZ8904CIL	N/A	83.08904.0AE
AMC	AZC099-04S	N/A	83.09904.AAE

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A3	CD1 DIS	SC

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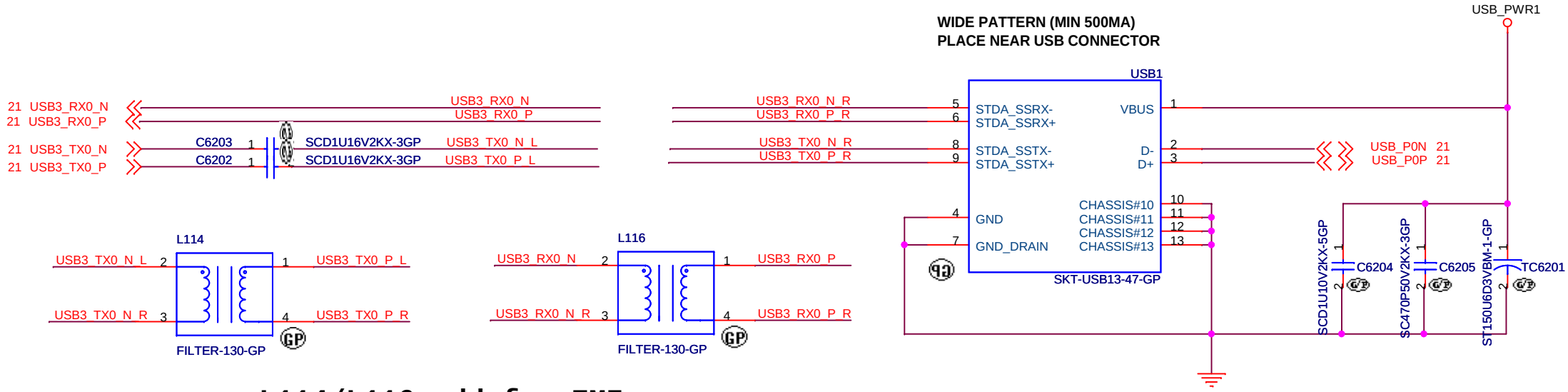
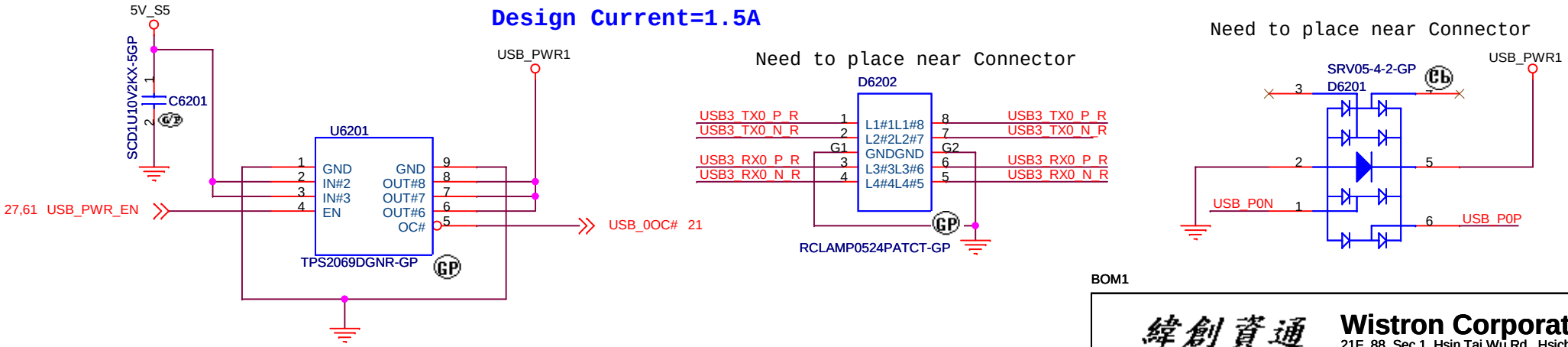
Left Rear USB Connector



L114/L116 add for EMI



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***USB3.0***	
Size A4	Document Number **CD1 DIS**	Rev **SC**
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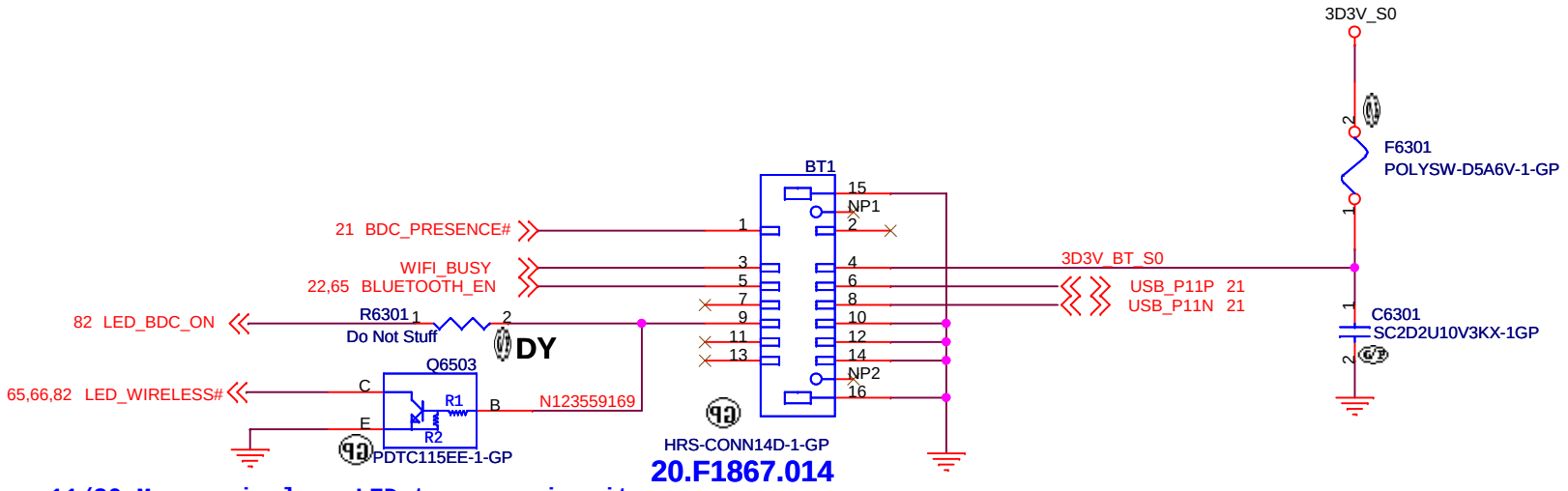
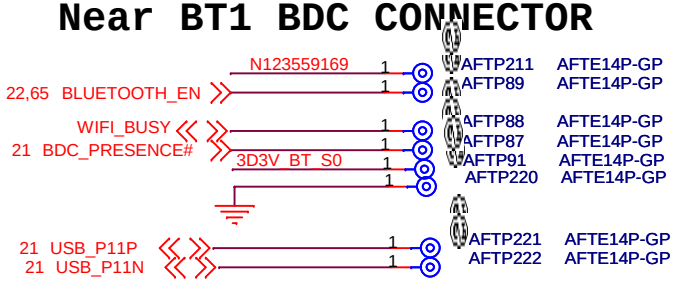
Bluetooth Module conn.



11/30 Merge wireless LED turn on circuits for Windoes8 requirement

Near BT1 BDC CONNECTOR



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A4	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 63 of 102

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Finger Print Conn***

Size	Document Number	Rev
A3	CD1 DIS	SC

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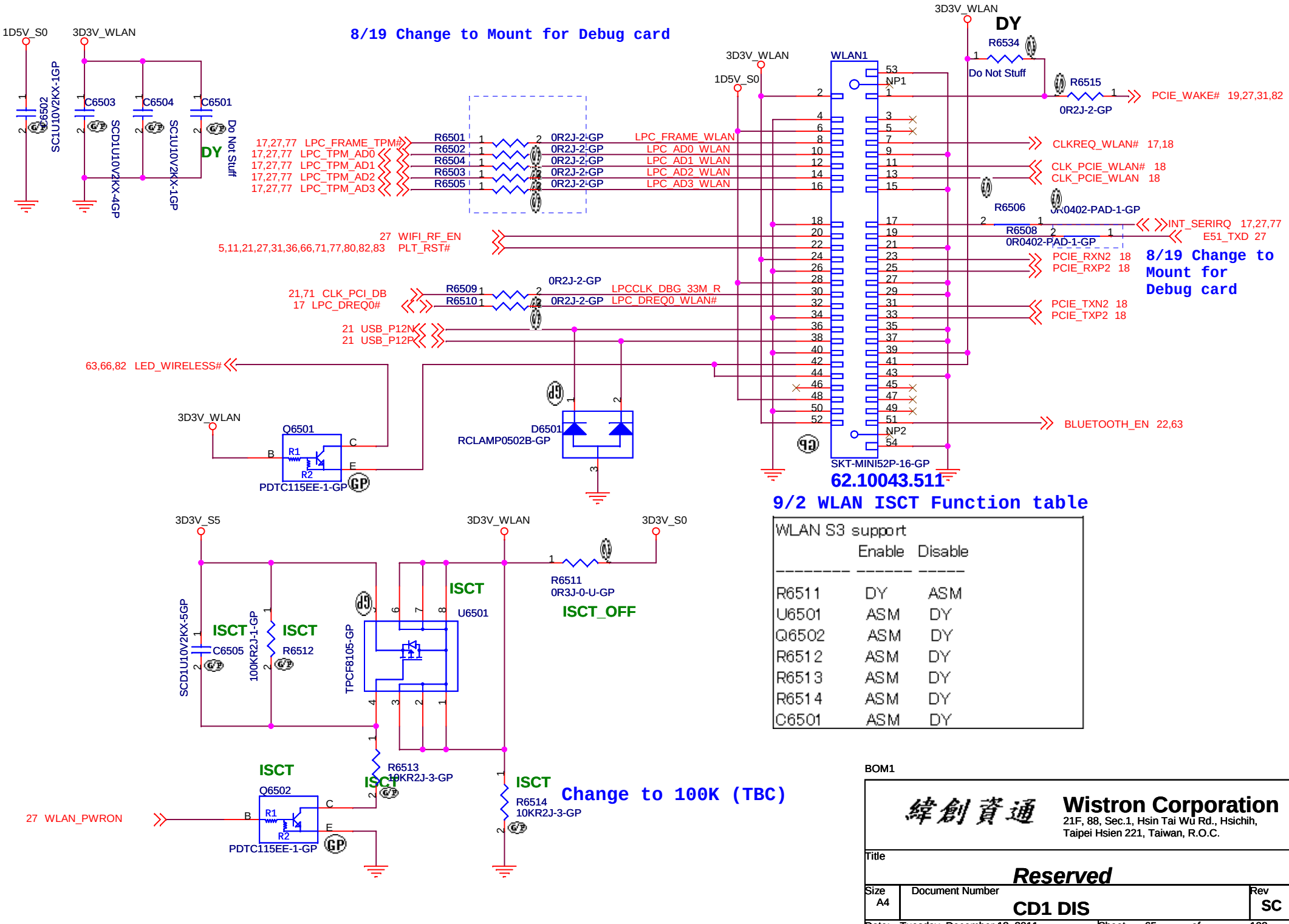


WLAN S3 support	Enable	Disable
R6511	DY	ASM
U6501	ASM	DY
Q6502	ASM	DY
R6512	ASM	DY
R6513	ASM	DY
R6514	ASM	DY
C6501	ASM	DY

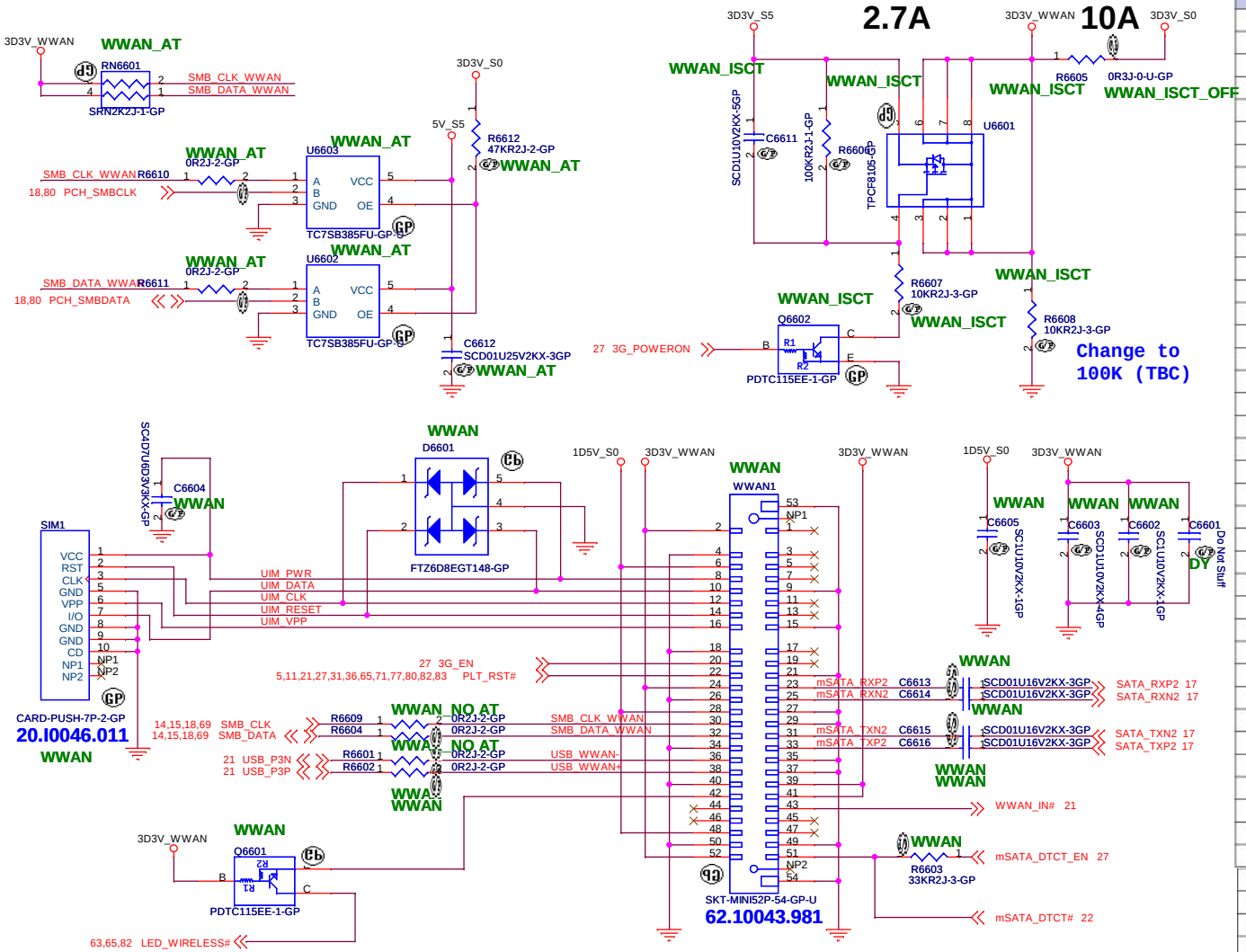
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 65 of 102



Pin	Function	Definition
P1	Reserved	No Connect
P2	+3.3 V	3.3 V Source
P3	Reserved	No Connect
P4	GND	Return Current Path
P5	Reserved	No Connect
P6	+1.5 V	1.5 V Source
P7	Reserved	No Connect
P8	Reserved	No Connect
P9	GND	Return Current Path
P10	Reserved	No Connect
P11	Reserved	No Connect
P12	Reserved	No Connect
P13	Reserved	No Connect
P14	Reserved	No Connect
P15	GND	Return Current Path
P16	Reserved	No Connect
P17	Reserved	No Connect
P18	GND	Return Current Path
P19	Reserved	No Connect
P20	Reserved	No Connect
P21	GND	Return Current Path
P22	Reserved	No Connect
P23	+B	Host Receiver Differential Signal Pair
P24	+3.3 V	3.3 V Source
P25	-B	Host Receiver Differential Signal Pair
P26	GND	Return Current Path
P27	GND	Return Current Path
P28	+1.5 V	1.5 V Source
P29	GND	Return Current Path
P30	Two Wire Interface	Two Wire Interface Clock[2]
P31	-A	Host Transmitter Differential Signal Pair
P32	Two Wire Interface	Two Wire Interface Data[2]
P33	+A	Host Transmitter Differential Signal Pair
P34	GND	Return Current Path
P35	GND	Return Current Path
P36	Reserved	No Connect
P37	GND	Return Current Path
P38	Reserved	No Connect
P39	+3.3 V	3.3 V Source
P40	GND	Return Current Path
P41	+3.3 V	3.3 V Source
P42	Reserved	No Connect
P43	Reserved	No Connect
P44	Reserved	No Connect
P45	Vendor	Vendor Specific / Manufacturing Pin[3]
P46	Reserved	No Connect
P47	Vendor	Vendor Specific / Manufacturing Pin[3]
P48	+1.5 V	1.5 V Source
P49	DA/DSS	Device Activity Signal / Disable Staggered Spin-up
P50	GND	Return Current Path
P51	Presence Detection	Shall be pulled to GND by device[1]
P52	+3.3 V	3.3 V Source

WWAN ASM/NON ASM

WWAN	YES	NO
WWAN1	ASM	No_ASM
SIM1	ASM	No_ASM
C6604	ASM	No_ASM
C6602	ASM	No_ASM
C6603	ASM	No_ASM

LOGIC

WWAN ISCT Funtion

Location	Disable 3G_PWRON	Enable 3G_PWRON
R6605	ASM	No_ASM
R6606	No_ASM	ASM
R6607	No_ASM	ASM
R6608	No_ASM	ASM
C6611	No_ASM	ASM
U6601	No_ASM	ASM
Q6602	No_ASM	ASM

LOGIC

Anti Theft Function

Location	AT No suport	AT suport
R6604	ASM	No_ASM
R6609	ASM	ASM
R6610	No_ASM	ASM
R6611	No_ASM	ASM
U6602	No_ASM	ASM
U6603	No_ASM	ASM
RN6601	No_ASM	ASM
R6612	No_ASM	ASM

LOGIC

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***WWAN/mSATA***

Size	Document Number	Rev
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BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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5 4 3 2 1

D

C

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B

A

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LED Bard/Power Button

Size	Document Number	Rev
A4	**CD1 DIS**	**SC**

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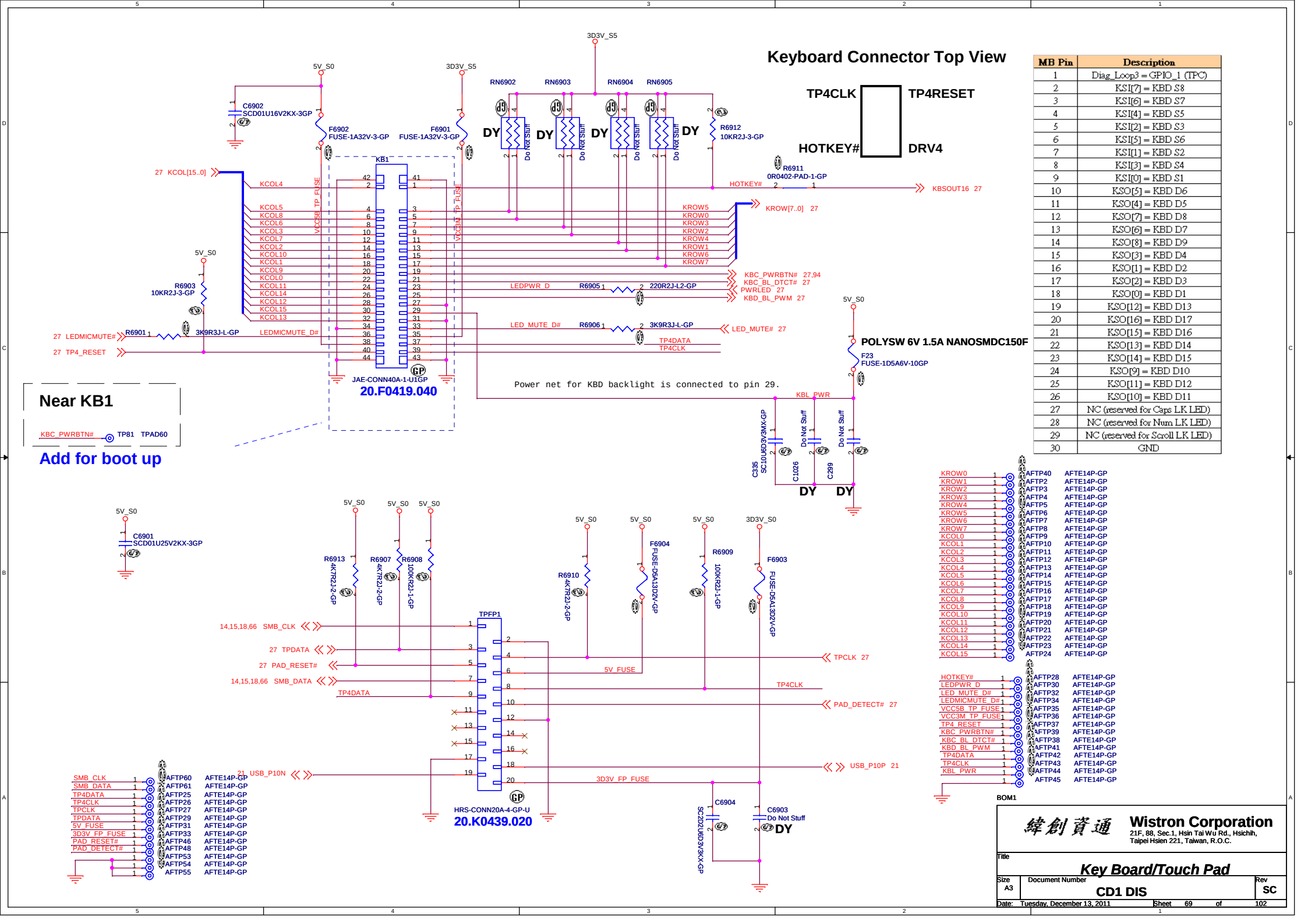

MB Pin	Description
1	Diag_Loop3 = GPIO_1 (TPC)
2	KSI[7] = KBD S8
3	KSI[6] = KBD S7
4	KSI[4] = KBD S5
5	KSI[2] = KBD S3
6	KSI[5] = KBD S6
7	KSI[1] = KBD S2
8	KSI[3] = KBD S4
9	KSI[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[7] = KBD D8
13	KSO[6] = KBD D7
14	KSO[8] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[12] = KBD D13
20	KSO[16] = KBD D17
21	KSO[15] = KBD D16
22	KSO[13] = KBD D14
23	KSO[14] = KBD D15
24	KSO[9] = KBD D10
25	KSO[11] = KBD D12
26	KSO[10] = KBD D11
27	NC (reserved for Caps LK LED)
28	NC (reserved for Num LK LED)
29	NC (reserved for Scroll LK LED)
30	GND

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Key Board/Touch Pad	
Size: A3	Document Number: CD1 DIS
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(Blanking)

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	CD1 DIS	SC

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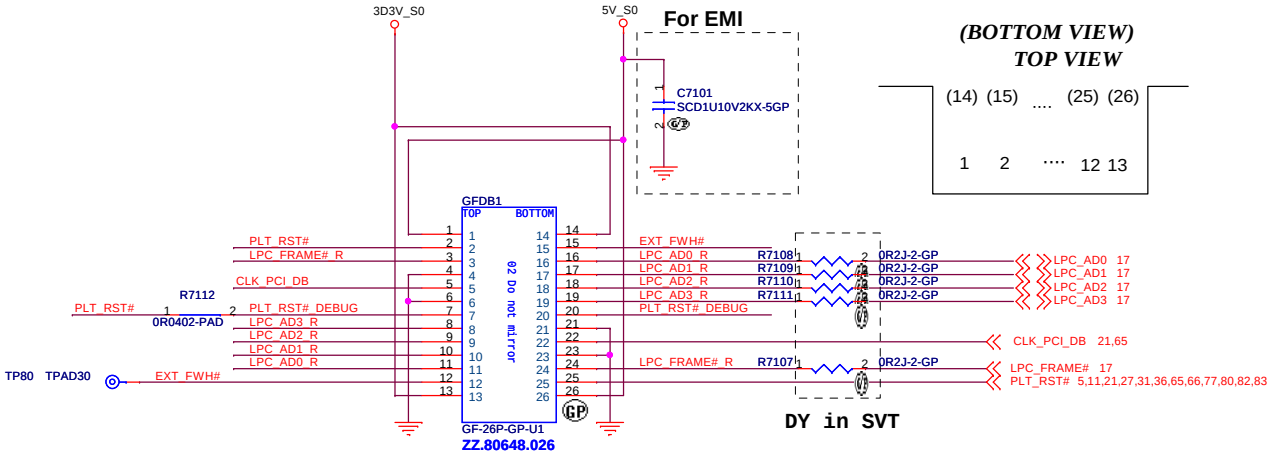
Golden Finger for Debug Board



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Dubug connector		
Size: A3	Document Number: CD1 DIS	Rev: SC
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BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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20.I0129.001

PIN	TYPE	FUNCTION	RTS5138 NET
P1	SD	SD-CD	SP6
P2	SD	SD-WP	SP1
P3	SD	SD-DAT1	SP3
P4	SD	SD-DAT0	SP4
P5	MMC_PLUS	MMC-DATA7	SP5
P6	MemoryStick	MS-GND	GND
P7	SD	SD-GND	GND
P8	MMC_PLUS	MMC-DATA6	SP7
P9	MemoryStick	MS-BS	SP14
P10	SD	SD-CLK	SP8
P11	MemoryStick	MS-DATA1	SP12
P12	MemoryStick	MS-DATA0	SP9
P13	SD	SD-VCC	3D3V_CARD_S0
P14	MemoryStick	MS-DATA2	SP8
P15	SD	SD-GND	GND
P16	MemoryStick	MS-INS	SP2
P17	MMC_PLUS	MMC-DATA5	SP9
P18	MemoryStick	MS-DATA3	SP5
P19	SD	SD-CMD	SP10
P20	MemoryStick	MS-SCLK	SP1
P21	MMC_PLUS	MMC-DATA4	SP11
P22	MemoryStick	MS-VCC	3D3V_CARD_S0
P23	SD	SD-DATA3	SP12
P24	MemoryStick	MS-GND	GND
P25	SD	SD-DAT2	SP13
P26	SD	SD-WP COM /SDIO GND	GND
P27	SD	SD-CD COM /SDIO GND	GND
#1	XD	XD-CD	XD_CD#
#2	XD	XD-R/B	SP1
#3	XD	XD-RE	SP2
#4	XD	XD-CE	SP3
#5	XD	XD-CLE	SP4
#6	XD	XD-ALE	SP5
#7	XD	XD-WE	SP6
#8	XD	XD-WP-IN	SP7
#9	XD	XD-GND	GND
#10	XD	XD-D0	SP8
#11	XD	XD-D1	SP9
#12	XD	XD-D2	SP10
#13	XD	XD-D3	SP11
#14	XD	XD-D4	SP12
#15	XD	XD-D5	SP13
#16	XD	XD-D6	SP14
#17	XD	XD-D7	XD-D7
#18	XD	XD-VCC	3D3V_CARD_S0
#19	XD	XD-GND	GND

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SD/XD/MS/MMC Card CONN***

Size: A3 | Document Number: **CD1 DIS** | Rev: SC

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BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Express Card***

Size	Document Number	Rev
A4	CD1 DIS	SC

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BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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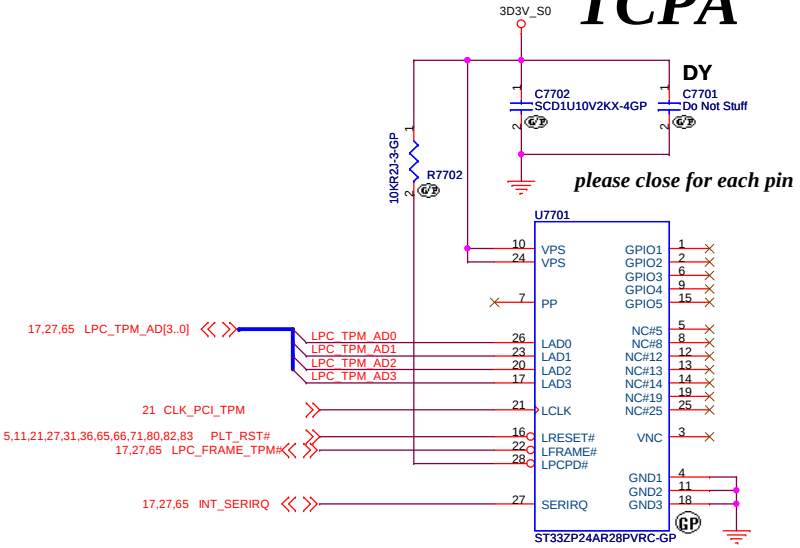
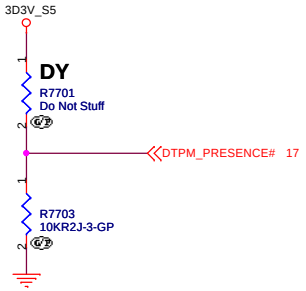
	NO TPM	ST Micro ST19NP18ER28PVMK
U39	NO_ASM	ASM
C379	NO_ASM	ASM
C9203	NO_ASM	NO_ASM
R149	NO_ASM	ASM
R212	ASM	NO_ASM
R270	NO_ASM	ASM

LOGIC

TCPA



71.03324.C0W



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPM**

Size: A3 | Document Number: **CD1 DIS** | Rev: SC

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BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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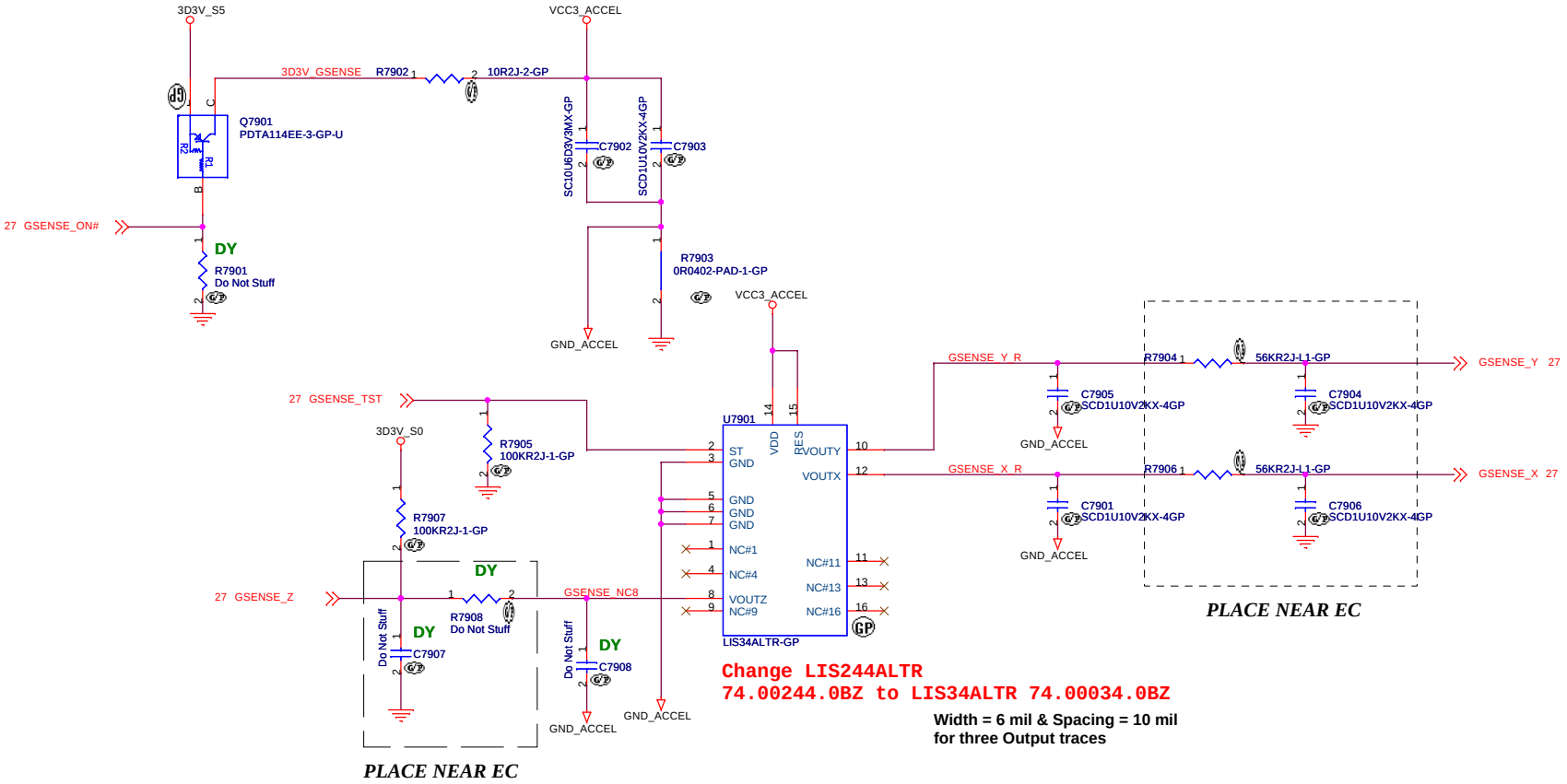

Change LIS244ALTR 74.00244.0BZ to LIS34ALTR 74.00034.0BZ

Width = 6 mil & Spacing = 10 mil for three Output traces

	LIS244AL LIS34AL	NO ACC.
R401	NO-ASM	ASM
R957	ASM	ASM
U65	ASM	NO-ASM
Q105	ASM	NO-ASM
R885	10-OHM	NO-ASM
C829	ASM	NO-ASM
C969	ASM	NO-ASM
C830	ASM	NO-ASM
C847	ASM	NO-ASM
R970	56K	NO-ASM
C956	ASM	NO-ASM
R969	56K	NO-ASM
C938	ASM	NO-ASM
C704	NO-ASM	NO-ASM
R344	NO-ASM	NO-ASM
C703	NO-ASM	NO-ASM
R125	ASM	ASM

Table

	Supplier	Vendo P/N	WISTRON P/N
1	ST	LIS34ALTR	74.00034.0BZ 41R0828AA
2	Kionix	KXTC8-2850	74.KXTC8.0BZ

Layout Comment :

(1) Place C586, C588, Q17, R415, R417, C584, C585, R420 close to U34.

(2) Avoid routing under DCDC switching area.

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size: A3 | Document Number: CD1 DIS | Rev: SC

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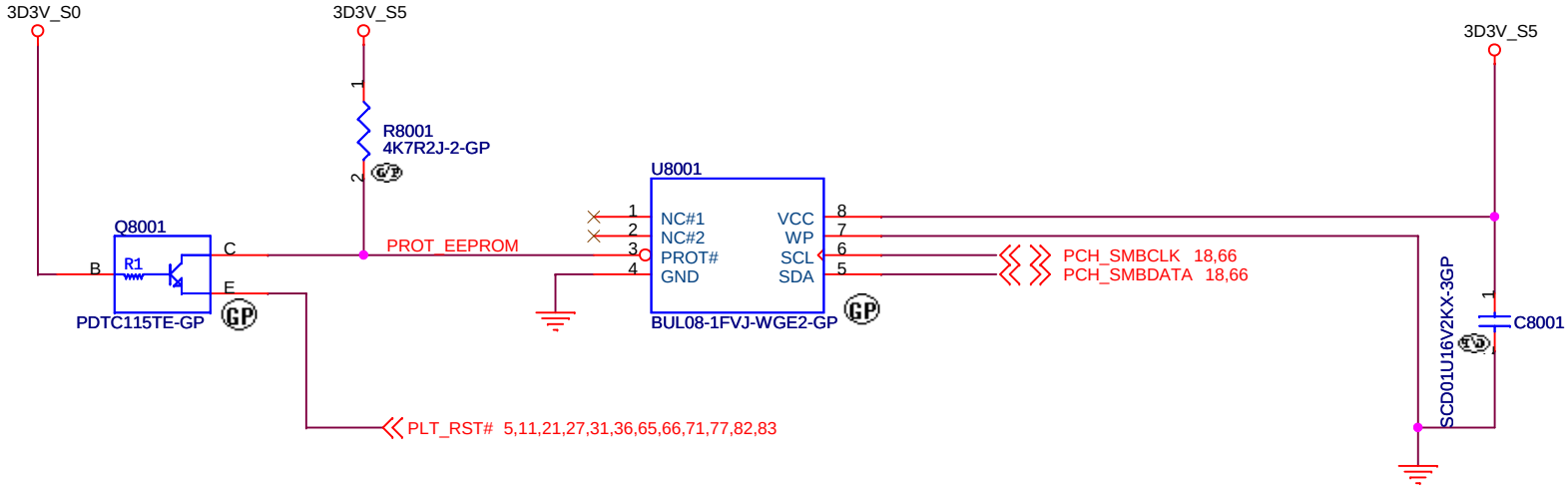

Supplier	Description	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	72.BUL08.A0Q
NXP	PCA24S08ADP	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	72.26C08.00R

BOM1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RFID***

Size	Document Number	Rev
A4	CD1 DIS	SC

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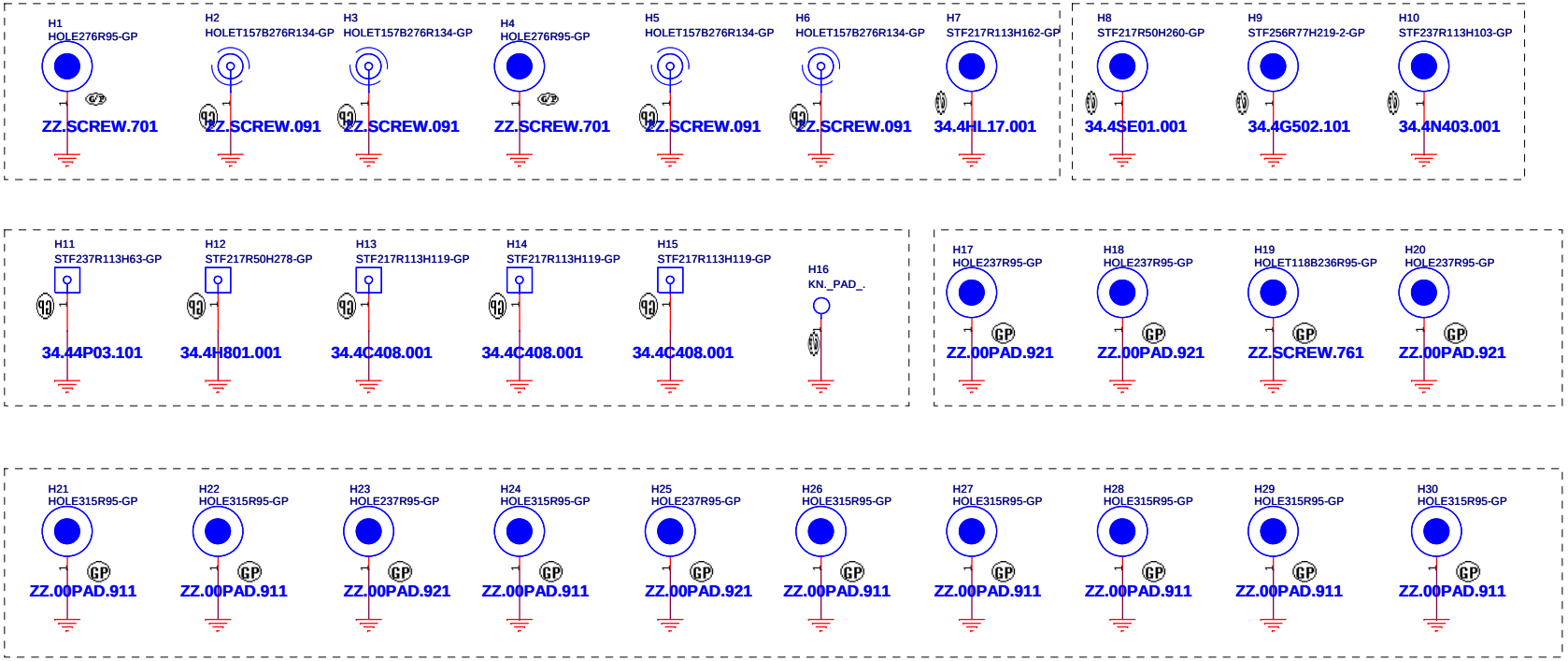

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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Reserve for
ISSC function
ECR105692

RJ45/A0U4/LED IF

9/27 modified

3D3V_AUX_KBC 3D3V_S5

R2718 Do Not Stuff

DY R2731 0R2J-2-GP

3D3V_LAN_S5 3D3V_S0 5V_S5 3D3V_S5

RJBD1

FOX-CONN40D-3-GP-U

20.F1400.040

31 LAN_ACT_SYS#
31 SYS_MDI_0+
31 SYS_MDI_0-
31 SYS_MDI_1+
31 SYS_MDI_1-
31 SYS_MDI_2+
31 SYS_MDI_2-
31 SYS_MDI_3+
31 SYS_MDI_3-
31 LAN_LINK_SYS#
21 USB_P4P
21 USB_P4N
27 USB_AO_SEL
27 USB_PWR_EN2
21 USB_4OC#
N115596552

LED_BDC_ON 63
DRIVE_LED# 17
MIC_DATA 29
MIC_CLK 29
USB_P13P 21
USB_P13N 21
LEDSUS# 27
LEDFUEL0# 27
LED_WIRELESS# 63,65,66
LEDFUEL1# 27
MIC_DET# 22
LID_CLOSE# 27

C8206 C8202 C8201 C8203 C8204 C8205 — Do Not Stuff — DY

LED IF COLOR

LEDFUEL0#	Orange
LEDFUEL1#	Green

27 LID_CLOSE#
17 DRIVE_LED#
27 LEDFUEL0#
27 LEDFUEL1#
31 LAN_ACT_SYS#
31 LAN_LINK_SYS#
27 USB_AO_SEL
27 USB_PWR_EN2
21 USB_4OC#
63 LED_BDC_ON
29 MIC_CLK
29 MIC_DATA
22 MIC_DET#
27 LEDSUS#
63,65,66 LED_WIRELESS#
3D3V_S5
5V_S5
3D3V_S0
3D3V_LAN_S5
3D3V_S5
3D3V_AUX_KBC

AFTP74 AFTP83 AFTP47 AFTP51 AFTP84 AFTP85 AFTP86 AFTP97 AFTP98 AFTP99 AFTP100 AFTP75 AFTP102 AFTP49 AFTP56 AFTP105 AFTP106 AFTP103 AFTP104 AFTP107 AFTP108 AFTP101 — AFTE14P-GP

AUDIO JACK/MEDIA CARDREADER

3D3V_S0

MCBD1

ACES-CONN33C-3-GP-U

18 PCIE_RXN1
18 PCIE_RXP1
18 CLK_PCIE_MCC#
18 CLK_PCIE_MCC
18 PCIE_TXN1
18 PCIE_TXP1
18 CLKREQ_MCC#
5,11,21,27,31,36,65,66,71,77,80,83 PLT_RST#

MIC_JACK_2 29,30
HP_L_JACK 29
HP_R_JACK 29
HP_JACK_SYS 30

AGND

change symbol

18 CLKREQ_MCC#
5,11,21,27,31,36,65,66,71,77,80,83 PLT_RST#
29,30 MIC_JACK_2
29 HP_L_JACK
29 HP_R_JACK
30 HP_JACK_SYS
3D3V_S0
AGND

AFTP76 AFTP110 AFTP50 AFTP57 AFTP113 AFTP114 AFTP111 AFTP112 AFTP115 — AFTE14P-GP

EXPRESS CARD

AFTE14P-GP AFTP78 N115596552
AFTE14P-GP AFTP77 PLT_RST# 5,11,21,27,31,36,65,66,71,77,80,83
AFTE14P-GP AFTP116 PCIE_WAKE# 19,27,31,65
AFTE14P-GP AFTP59 PM_SLP_S3# 19,27,36,37,47
AFTE14P-GP AFTP58 EXC_PWR_SHDN#
AFTE14P-GP AFTP118 CLKREQ_NEW# 18,22
AFTE14P-GP AFTP117 3D3V_S0
AFTE14P-GP AFTP119 3D3V_S5
AFTE14P-GP AFTP120 1D5V_S0
AFTE14P-GP AFTP121

EXPBD1

3D3V_S0 1.3A
3D3V_S5 275mA
1D5V_S0 650mA

USB_P5N 21
USB_P5P 21
CLK_PCIE_NEW# 18
CLK_PCIE_NEW 18
PCIE_RXN3 18
PCIE_RXP3 18
PCIE_TXN3 18
PCIE_TXP3 18

5,11,21,27,31,36,65,66,71,77,80,83 PLT_RST#
19,27,31,65 PCIE_WAKE#
19,27,36,37,47 PM_SLP_S3#
EXC_PWR_SHDN#
18,22 CLKREQ_NEW#

19,27,46 PM_SLP_S4# — R8202 — DY — Do Not Stuff
27 EXC_PWR_SHDN_R# — R8203 0R0402-PAD-1-GP

FOX-CONN30D-GP

20.F2065.030

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: CD1 DIS | Rev: SC

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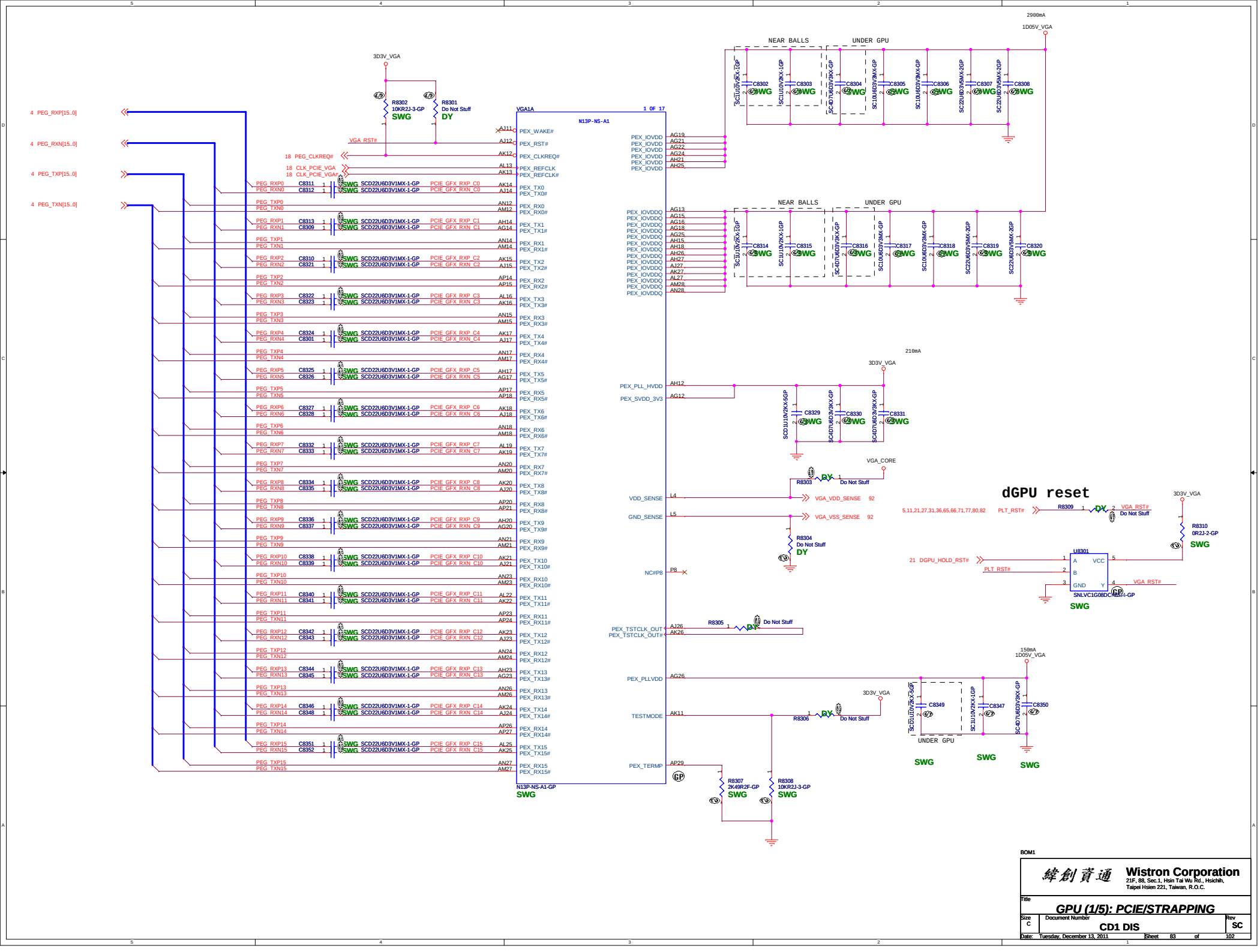

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (1/5): PCIE/STRAPPING

Size	Document Number	Rev
C	CD1 DIS	SC

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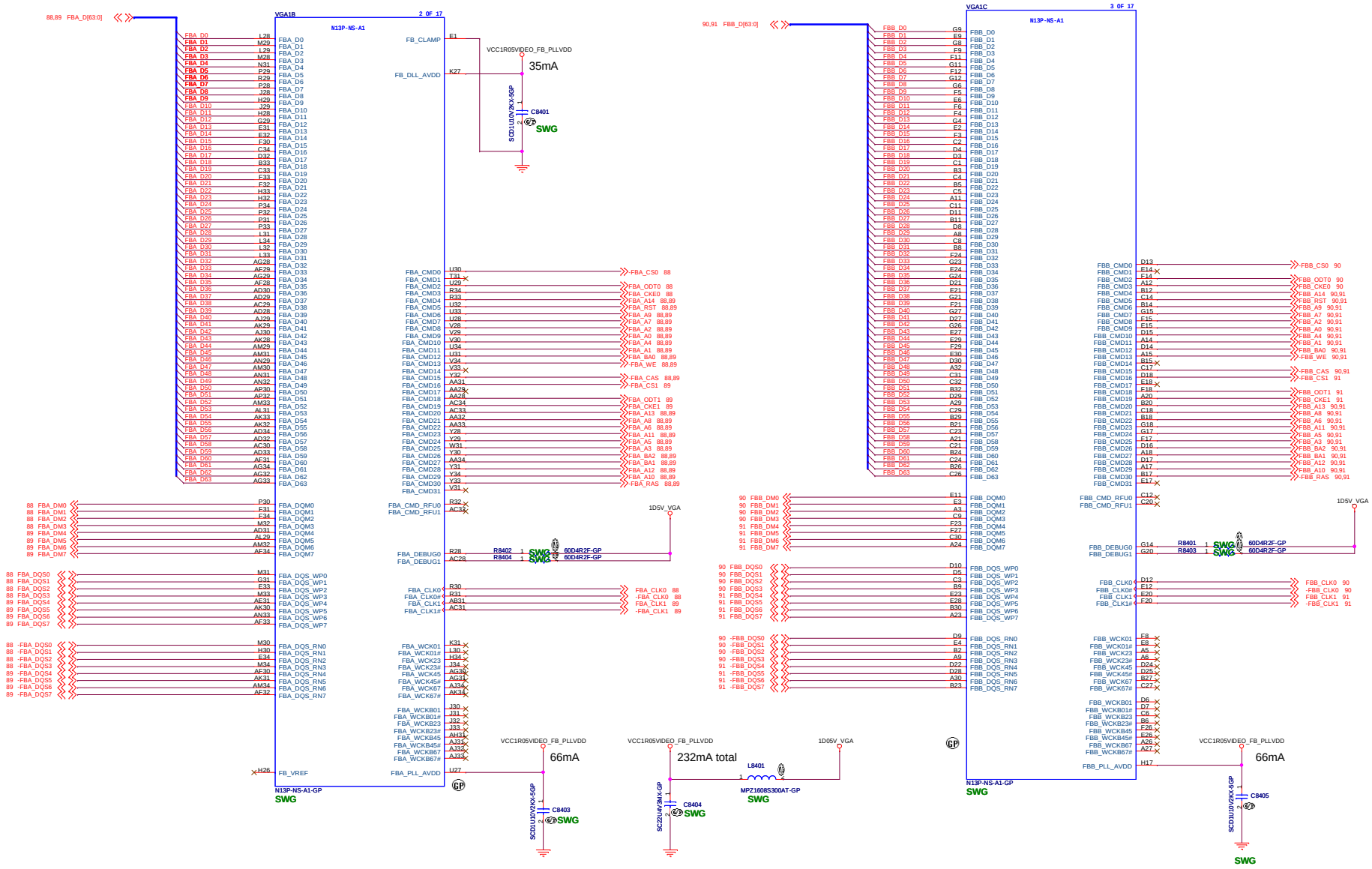
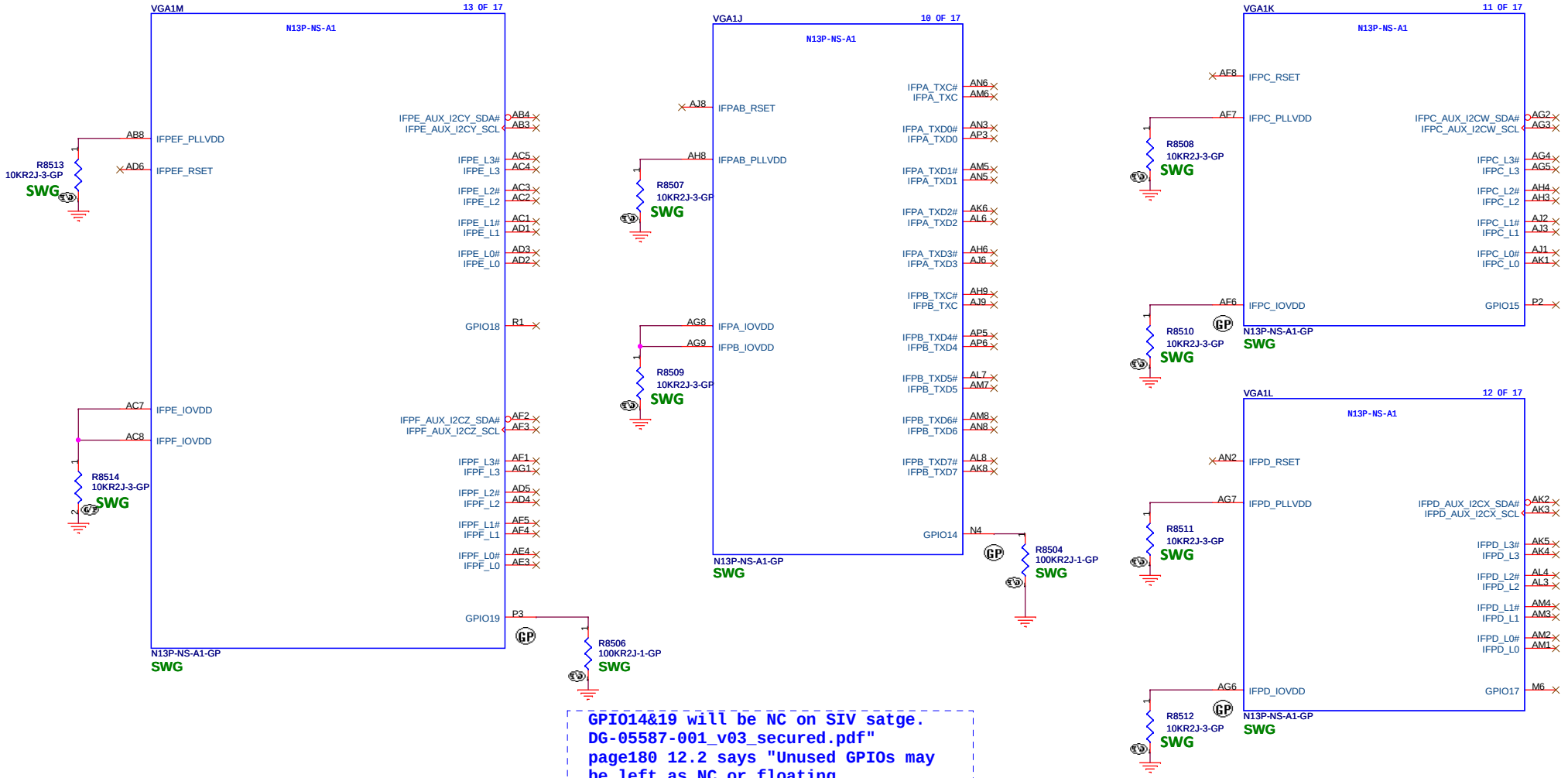


BOM1

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: GPU (2/5): Memory		
Size: A2	Document Number: CD1 DIS	Rev: SC
Date: Tuesday, December 13, 2011	Sheet 84 of 102	



GPIO14&19 will be NC on SIV satge.
DG-05587-001_v03_secured.pdf"
page180 12.2 says "Unused GPIOs may
be left as NC or floating

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (3/5): DP/LVDS/CRT/GPIO

Size	Document Number	Rev
A3	CD1 DIS	SC

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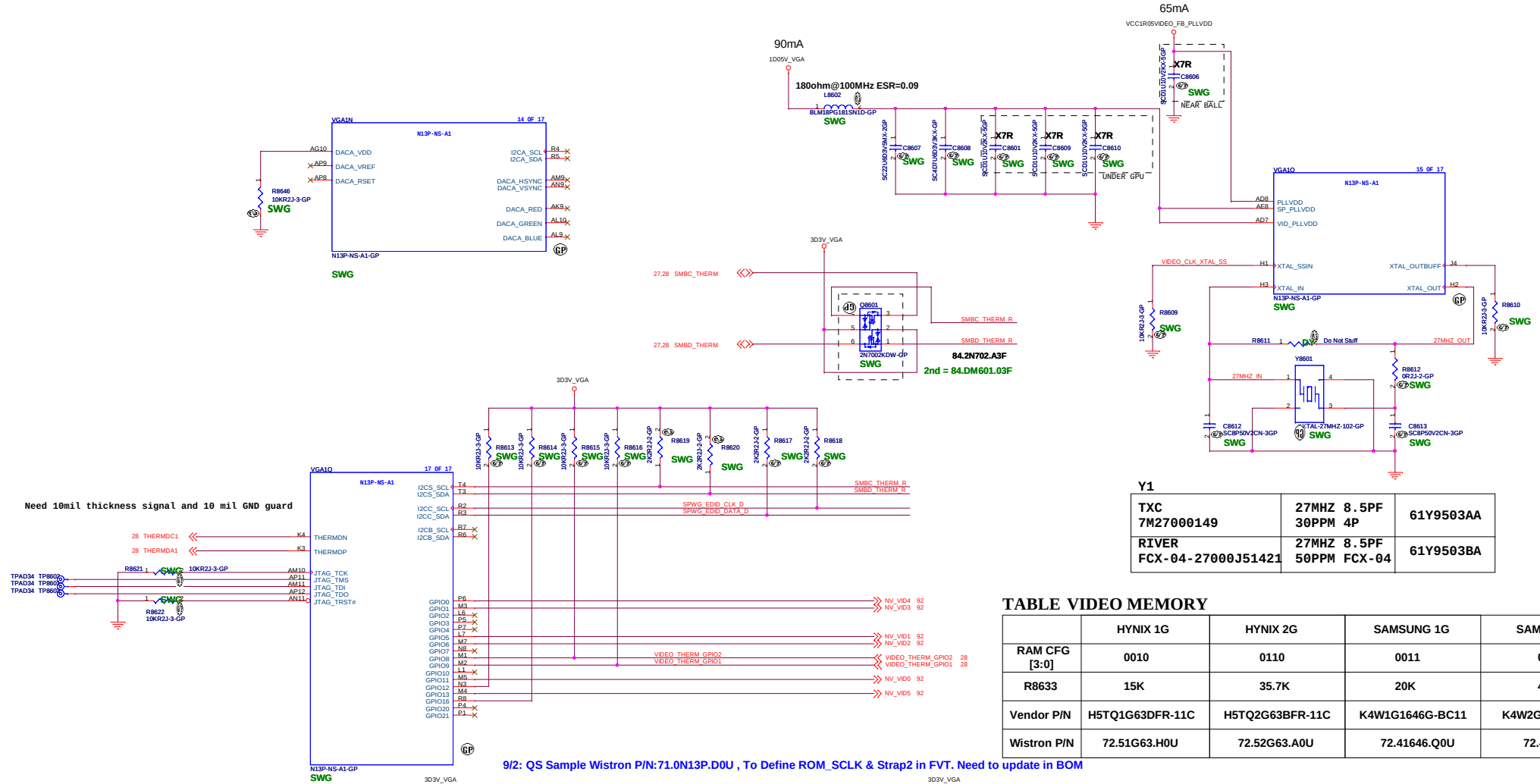


Y1

TXC 7M27000149	27MHZ 8.5PF 30PPM 4P	61Y9503AA
RIVER FCX-04-27000J51421	27MHZ 8.5PF 50PPM FCX-04	61Y9503BA

TABLE VIDEO MEMORY

	HYNIX 1G	HYNIX 2G	SAMSUNG 1G	SAMSUNG 2G
RAM CFG [3:0]	0010	0110	0011	0111
R8633	15K	35.7K	20K	45.3K
Vendor P/N	H5TQ1G63DFR-11C	H5TQ2G63BFR-11C	K4W1G1646G-BC11	K4W2G1646C-HC11
Wistron P/N	72.51G63.H0U	72.52G63.A0U	72.41646.Q0U	72.42164.D0U

N13P-ES4-A1	Setting	ROM_SCLK	Strap2
	0x0DEF	0010	1111
		15Kohm pull-down	45Kohm pull-up

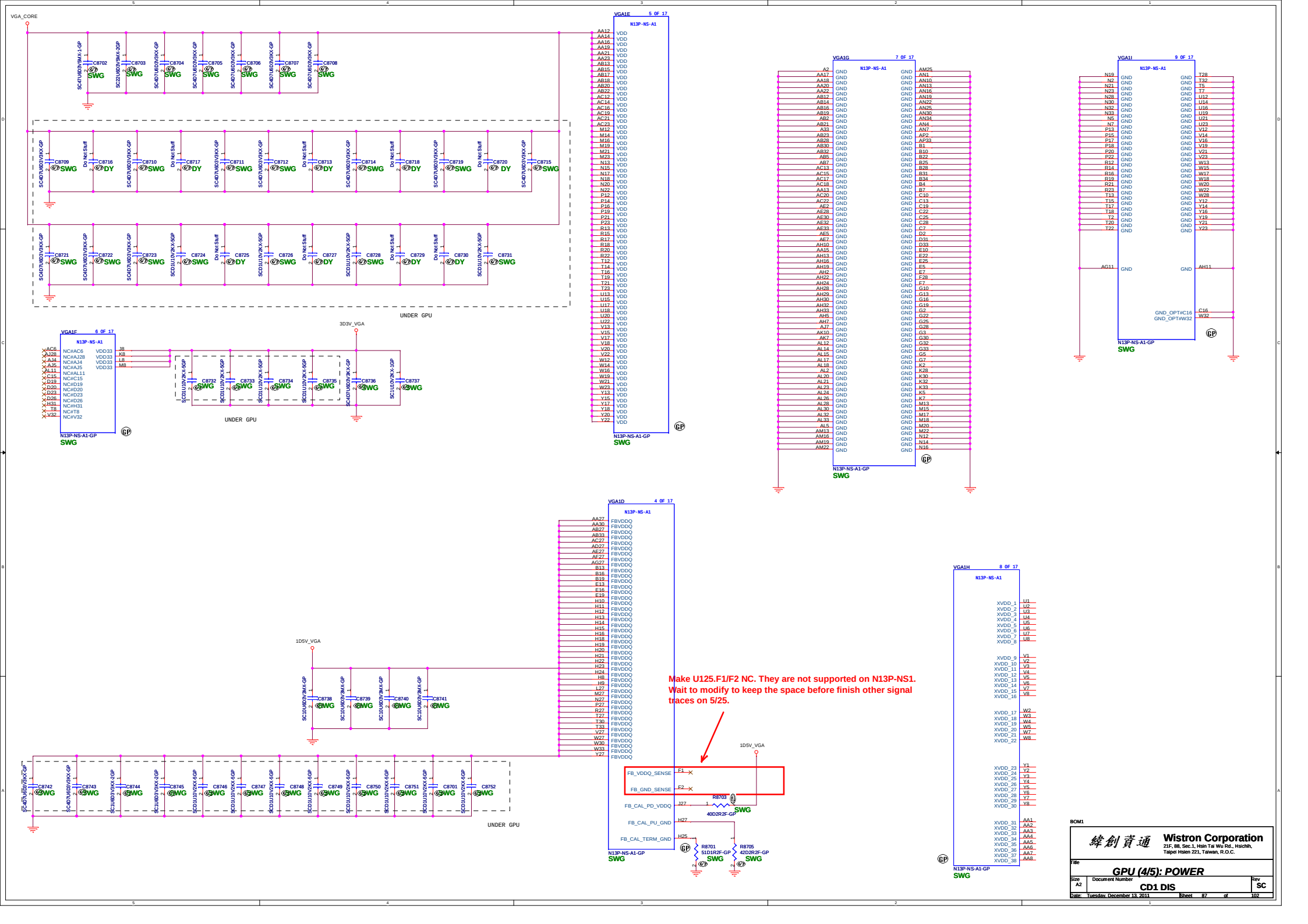
BOM1

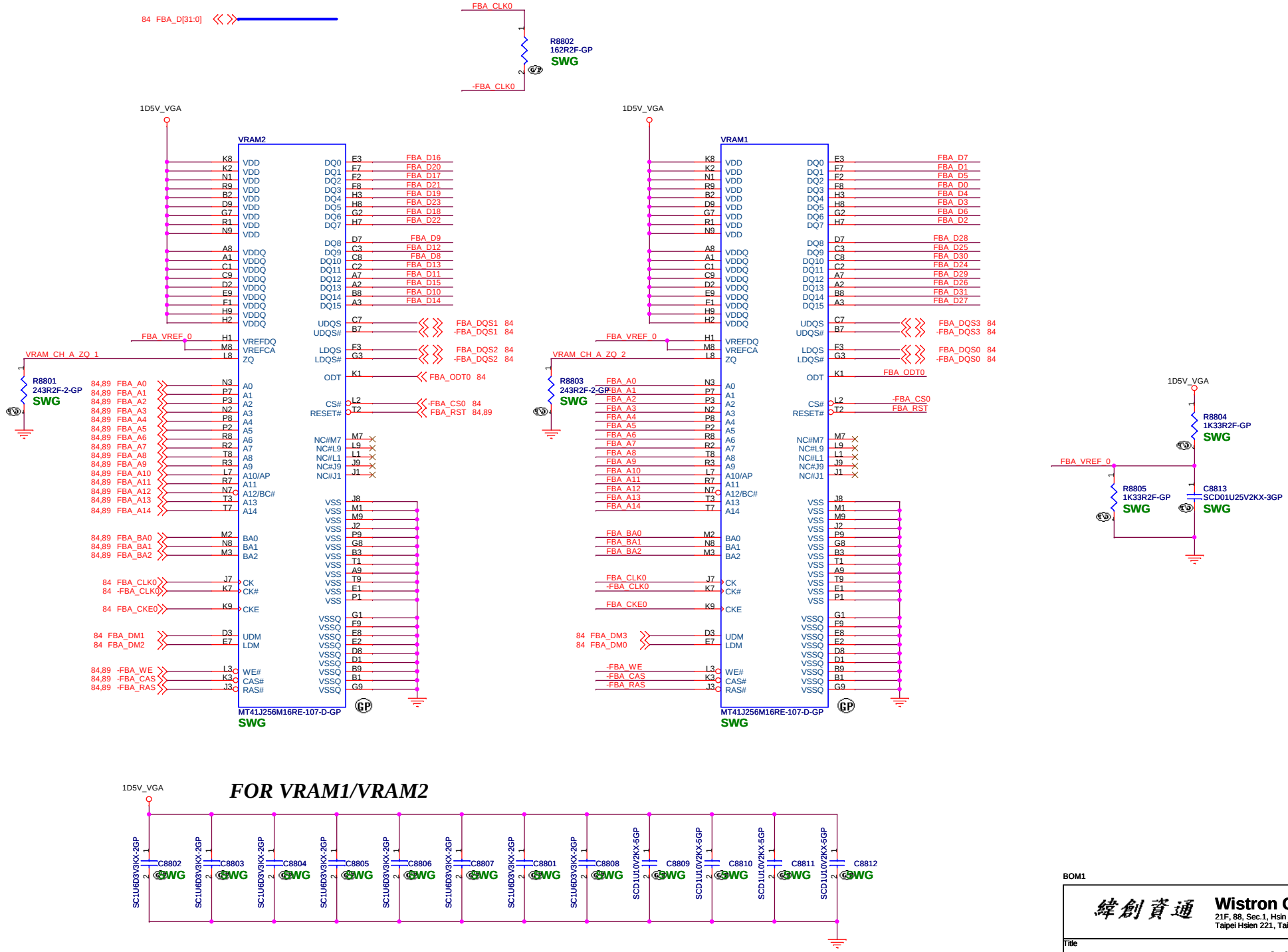
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (5/5): DPPWR/GND

Size: A2 | Document Number: CD1 DIS | Rev: SC

Date: Tuesday, December 13, 2011 | Sheet 86 of 102


VGA_CORE
VGA1E 5 OF 17
N13P-NS-A1
N13P-NS-A1-GP
SWG
UNDER GPU
VGA1F 6 OF 17
3D3V_VGA
VGA1G 7 OF 17
VGA1I 9 OF 17
VGA1D 4 OF 17
1D5V_VGA
VGA1H 8 OF 17
Make U125.F1/F2 NC. They are not supported on N13P-NS1.
Wait to modify to keep the space before finish other signal
traces on 5/25.
FB_VDDQ_SENSE
FB_GND_SENSE
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
R8703 40D2R2F-GP
R8701 51D1R2F-GP
R8705 42D2R2F-GP
BOM1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU (4/5): POWER
Size A2
Document Number
CD1 DIS
Rev SC
Date: Tuesday, December 13, 2011
Sheet 87 of 102



BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
A3	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 88 of 102

84 FBA_D[63:32]

FBA_CLK1 — R8902 162R2F-GP SWG — -FBA_CLK1

1D5V_VGA

VRAM3

VRAM_CH_A_ZQ_3 — R8903 243R2F-2-GP SWG

FBA_VREF_1

84,88 FBA_A0	FBA_A0	N3	A0
84,88 FBA_A1	FBA_A1	P7	A1
84,88 FBA_A2	FBA_A2	P3	A2
84,88 FBA_A3	FBA_A3	N2	A3
84,88 FBA_A4	FBA_A4	P8	A4
84,88 FBA_A5	FBA_A5	P2	A5
84,88 FBA_A6	FBA_A6	R8	A6
84,88 FBA_A7	FBA_A7	R2	A7
84,88 FBA_A8	FBA_A8	T8	A8
84,88 FBA_A9	FBA_A9	R3	A9
84,88 FBA_A10	FBA_A10	L7	A10/AP
84,88 FBA_A11	FBA_A11	R7	A11
84,88 FBA_A12	FBA_A12	N7	A12/BC#
84,88 FBA_A13	FBA_A13	T3	A13
84,88 FBA_A14		T7	A14
84,88 FBA_BA0	FBA_BA0	M2	BA0
84,88 FBA_BA1	FBA_BA1	N8	BA1
84,88 FBA_BA2	FBA_BA2	M3	BA2
84 FBA_CLK1		J7	CK
84 -FBA_CLK1		K7	CK#
84 FBA_CKE1		K9	CKE
84 FBA_DM4		D3	UDM
84 FBA_DM7		E7	LDM
84,88 -FBA_WE	-FBA_WE	L3	WE#
84,88 -FBA_CAS	-FBA_CAS	K3	CAS#
84,88 -FBA_RAS	-FBA_RAS	J3	RAS#

DQ0	E3	FBA_D58
DQ1	E7	FBA_D61
DQ2	F2	FBA_D57
DQ3	F8	FBA_D62
DQ4	H3	FBA_D56
DQ5	H8	FBA_D60
DQ6	G2	FBA_D59
DQ7	H7	FBA_D63
DQ8	D7	FBA_D33
DQ9	C3	FBA_D37
DQ10	C8	FBA_D34
DQ11	C2	FBA_D38
DQ12	A7	FBA_D35
DQ13	A2	FBA_D36
DQ14	B8	FBA_D32
DQ15	A3	FBA_D39
UDQS	C7	FBA_DQS4 84
UDQS#	B7	-FBA_DQS4 84
LDQS	F3	FBA_DQS7 84
LDQS#	G3	-FBA_DQS7 84
ODT	K1	FBA_ODT1 84
CS#	L2	-FBA_CS1 84
RESET#	T2	FBA_RST 84,88

NC#M7 M7, NC#L9 L9, NC#L1 L1, NC#J9 J9, NC#J1 J1

VSS: J8, M1, M9, J2, P9, G8, B3, T1, A9, T9, E1, P1

VSSQ: G1, F9, E8, E2, D8, D1, B9, B1, G9

MT41J256M16RE-107-D-GP SWG

VRAM4

1D5V_VGA

VRAM_CH_A_ZQ_4 — R8901 243R2F-2-GP SWG

FBA_VREF_1

FBA_A0		N3	A0
FBA_A1		P7	A1
FBA_A2		P3	A2
FBA_A3		N2	A3
FBA_A4		P8	A4
FBA_A5		P2	A5
FBA_A6		R8	A6
FBA_A7		R2	A7
FBA_A8		T8	A8
FBA_A9		R3	A9
FBA_A10		L7	A10/AP
FBA_A11		R7	A11
FBA_A12		N7	A12/BC#
FBA_A13		T3	A13
FBA_A14		T7	A14
FBA_BA0		M2	BA0
FBA_BA1		N8	BA1
FBA_BA2		M3	BA2
FBA_CLK1		J7	CK
-FBA_CLK1		K7	CK#
FBA_CKE1		K9	CKE
84 FBA_DM6		D3	UDM
84 FBA_DM5		E7	LDM
-FBA_WE		L3	WE#
-FBA_CAS		K3	CAS#
-FBA_RAS		J3	RAS#

DQ0	E3	FBA_D47
DQ1	F7	FBA_D42
DQ2	F2	FBA_D44
DQ3	F8	FBA_D41
DQ4	H3	FBA_D45
DQ5	H8	FBA_D40
DQ6	G2	FBA_D46
DQ7	H7	FBA_D43
DQ8	D7	FBA_D52
DQ9	C3	FBA_D51
DQ10	C8	FBA_D54
DQ11	C2	FBA_D48
DQ12	A7	FBA_D53
DQ13	A2	FBA_D50
DQ14	B8	FBA_D55
DQ15	A3	FBA_D49
UDQS	C7	FBA_DQS6 84
UDQS#	B7	-FBA_DQS6 84
LDQS	F3	FBA_DQS5 84
LDQS#	G3	-FBA_DQS5 84
ODT	K1	FBA_ODT1
CS#	L2	-FBA_CS1
RESET#	T2	FBA_RST

NC#M7 M7, NC#L9 L9, NC#L1 L1, NC#J9 J9, NC#J1 J1

VSS: J8, M1, M9, J2, P9, G8, B3, T1, A9, T9, E1, P1

VSSQ: G1, F9, E8, E2, D8, D1, B9, B1, G9

MT41J256M16RE-107-D-GP SWG

1D5V_VGA — R8904 1K33R2F-GP SWG

FBA_VREF_1 — R8905 1K33R2F-GP SWG — C8913 SCD01U25V2KX-3GP SWG

1D5V_VGA

FOR VRAM3/VRAM4

C8902	SC1U6D3V3KX-2GP	SWG
C8903	SC1U6D3V3KX-2GP	SWG
C8901	SC1U6D3V3KX-2GP	SWG
C8904	SC1U6D3V3KX-2GP	SWG
C8905	SC1U6D3V3KX-2GP	SWG
C8906	SC1U6D3V3KX-2GP	SWG
C8907	SC1U6D3V3KX-2GP	SWG
C8908	SC1U6D3V3KX-2GP	SWG
C8909	SCD1U10V2KX-5GP	SWG
C8910	SCD1U10V2KX-5GP	SWG
C8911	SCD1U10V2KX-5GP	SWG
C8912	SCD1U10V2KX-5GP	SWG

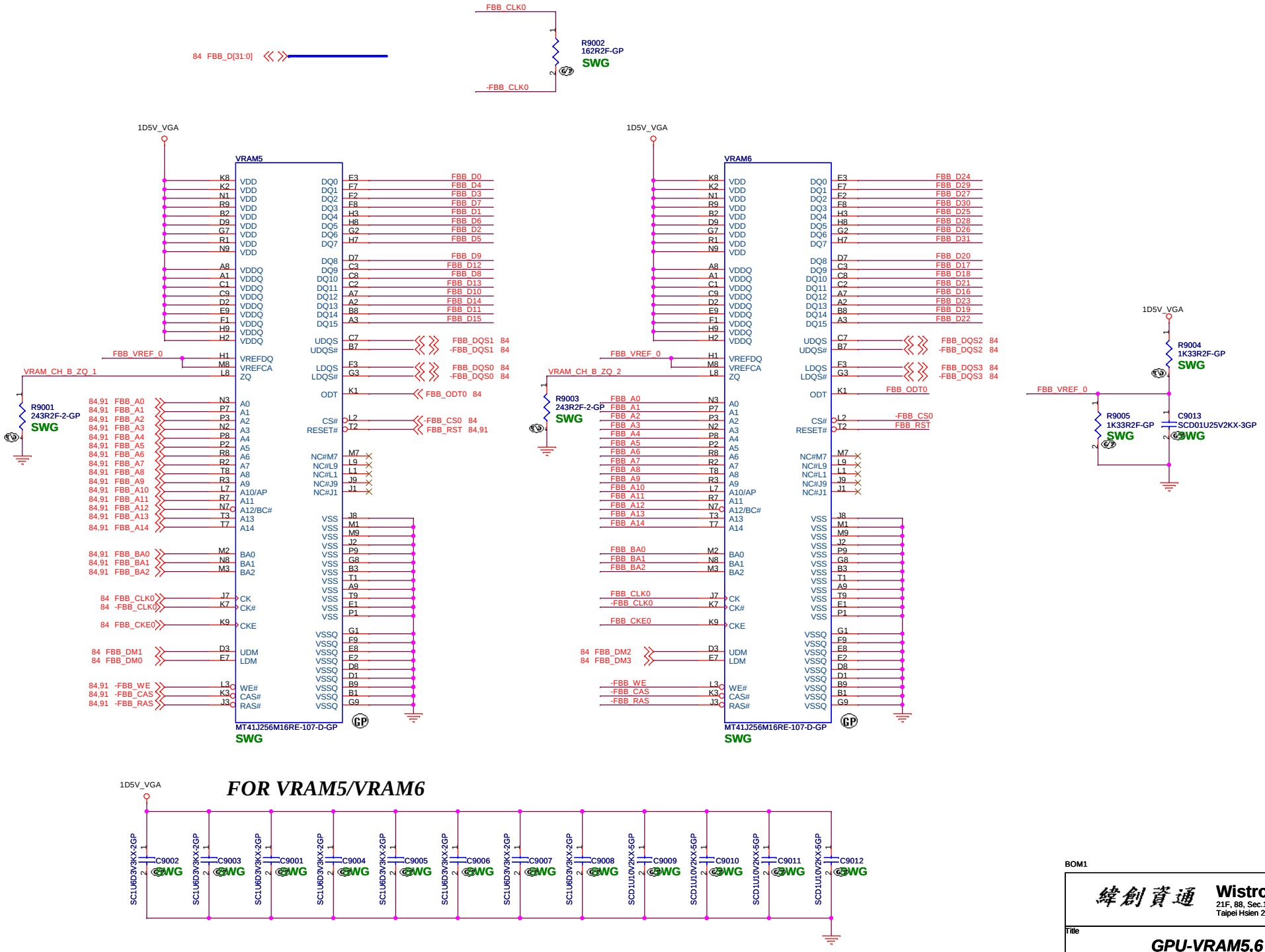
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A3	CD1 DIS	SC

Date: Tuesday, December 13, 2011 Sheet 89 of 102



BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A3	CD1 DIS	SC

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84 FBB_D[63:32]

FBB_CLK1
R9101
162R2F-GP
SWG
-FBB_CLK1

1D5V_VGA

VRAM8

FBB_VREF_1
VRAM_CH_B_ZQ_3
R9102
243R2F-2-GP
SWG

MT41J256M16RE-107-D-GP
SWG

1D5V_VGA

VRAM7

FBB_VREF_1
VRAM_CH_B_ZQ_4
R9103
243R2F-2-GP
SWG

MT41J256M16RE-107-D-GP
SWG

1D5V_VGA
R9104
1K33R2F-GP
SWG
FBB_VREF_1
R9105
1K33R2F-GP
SWG
C9113
SCD01U25V2KX-3GP
SWG

1D5V_VGA

FOR VRAM7/VRAM8

C9102 C9103 C9104 C9105 C9106 C9107 C9108 C9109 C9110 C9101 C9111 C9112
SC1U6D3V3KX-2GP
SCD1U10V2KX-5GP
SWG

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A3	CD1 DIS	SC

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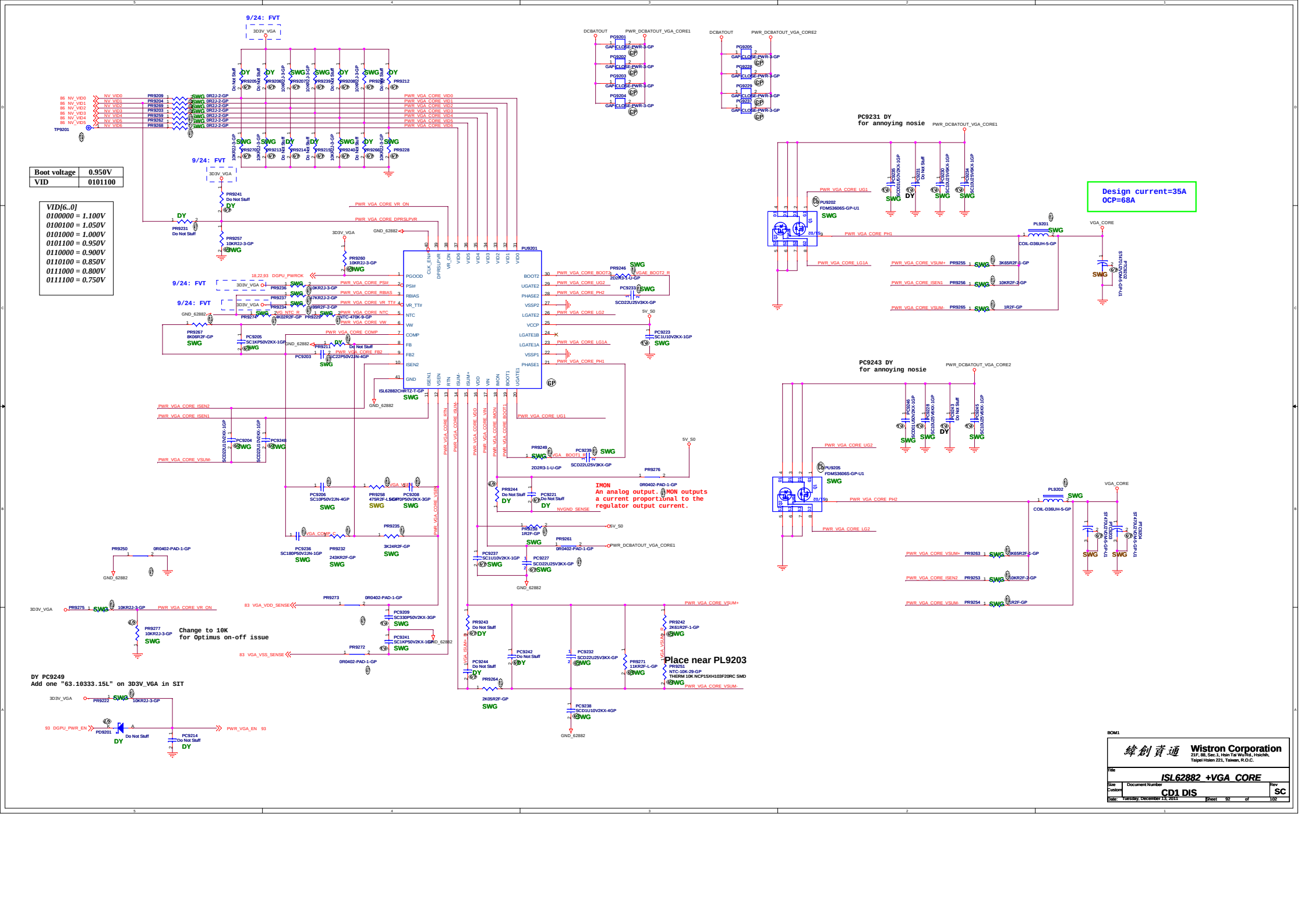
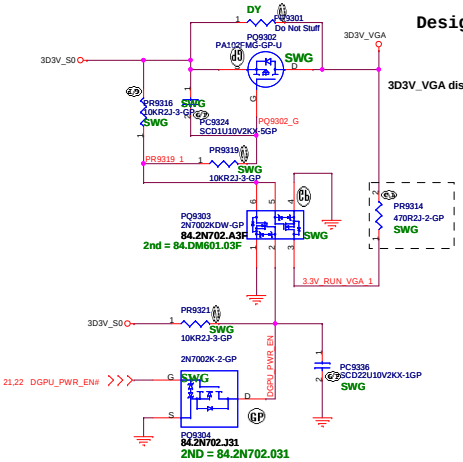

9/24: FVT
3D3V_VGA
Boot voltage 0.950V
VID 0101100
VID[6..0]
0100000 = 1.100V
0100100 = 1.050V
0101000 = 1.000V
0101100 = 0.950V
0110000 = 0.900V
0110100 = 0.850V
0111000 = 0.800V
0111100 = 0.750V
PU9201
ISL62882CHRTZ-T-GP
PWR_VGA_CORE_VID0
PWR_VGA_CORE_VID1
PWR_VGA_CORE_VID2
PWR_VGA_CORE_VID3
PWR_VGA_CORE_VID4
PWR_VGA_CORE_VID5
PWR_VGA_CORE_VID6
PWR_VGA_CORE_VR_ON
PWR_VGA_CORE_DPRSLPVR
PWR_VGA_CORE_PSI#
PWR_VGA_CORE_RBIAS
PWR_VGA_CORE_VR_TT#
PWR_VGA_CORE_NTC
PWR_VGA_CORE_VW
PWR_VGA_CORE_COMP
PWR_VGA_CORE_FB2
PWR_VGA_CORE_ISEN2
PWR_VGA_CORE_ISEN1
PWR_VGA_CORE_VSUM-
PWR_VGA_CORE_VSUM+
PWR_VGA_CORE_UG1
PWR_VGA_CORE_LG1A
PWR_VGA_CORE_PH1
PWR_VGA_CORE_UG2
PWR_VGA_CORE_LG2
PWR_VGA_CORE_PH2
PWR_VGA_CORE_BOOT2
VGAE_BOOT2_R
VGA_BOOT1_R
VGA_VSEN
VGA_COMP
VGA_ISUM+
VGA_ISUM-
NVGND_SENSE
5V_S0
DCBATOUT
PWR_DCBATOUT_VGA_CORE1
PWR_DCBATOUT_VGA_CORE2
PG9201
PG9202
PG9203
PG9204
PG9205
PG9228
PG9229
PG9230
PG9231
GAP-CLOSE-PWR-3-GP
PC9231 DY
for annoying nosie
PU9202
FDMS3606S-GP-U1
PL9201
COIL-D36UH-5-GP
VGA_CORE
PC9243 DY
for annoying nosie
PU9205
PL9202
Design current=35A
OCP=68A
IMON
An analog output. IMON outputs
a current proportional to the
regulator output current.
Change to 10K
for Optimus on-off issue
Place near PL9203
DY PC9249
Add one "63.10333.15L" on 3D3V_VGA in SIT
BOM1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL62882 +VGA_CORE
CD1 DIS
SC
Tuesday, December 13, 2011
92
102

3D3V_S0 to 3D3V_VGA_S0 Transfer

12/8 SIT PQ9302

Design current = 330mA

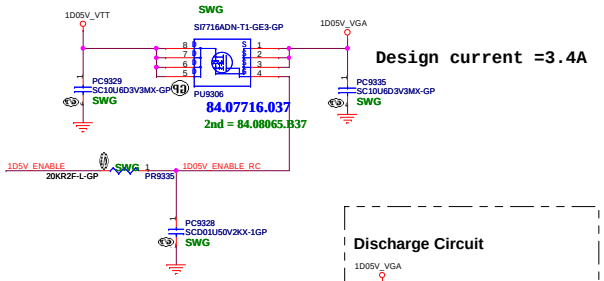


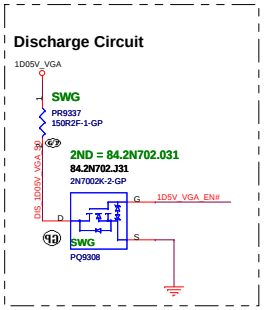
1D05V_VGA

9/27 Modify for 1D05VGA power sequence issue

1D5V_S3 to 1D5V_VGA_S0 trace need increase to avoid 1D5V_VGA_S0 DROP Voltage.

Design current =3.4A





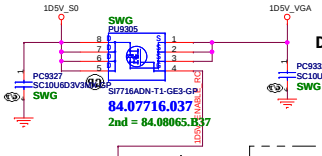
1D5V_VGA

change low Rds(on) MOSFET

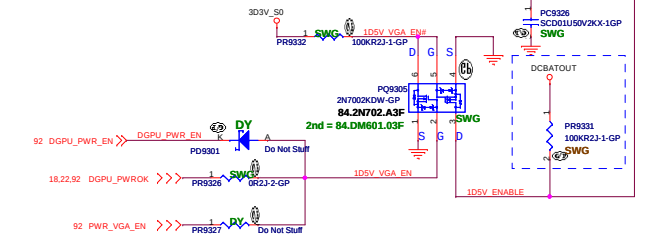
AO4468, SO-8
Id=16A, Qg=9~12nC
Rdson=17.4~22m ohm

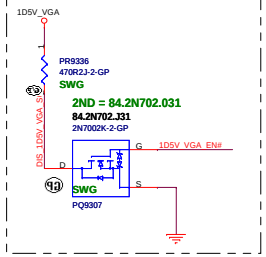
1D5V_S0 to 1D5V_VGA trace need increase to avoid 1D5V_VGA DROP Voltage.

Design current =6.27A (dGPU=4.23A,VRAM=2.24A)



Park_Madison_Does_Not_Support_BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence





9/2 PR9331.1 For Fixing RUN_ENABLE Gate Voltage Fail in SDV

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size	Document Number	Rev
A2	CD1 DIS	SC

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9/29 Modified

9/7: Need to confirm -DOCK_ATTACHED_3B before FVT

Confirm if we need it??

For Lizzie DVI issue

DOCK1

JAE-CONN148-6R-1-GP

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Dock Connector

Size: A2 | Document Number: CD1 DIS | Rev: SC

Date: Tuesday, December 13, 2011 | Sheet 94 of 102

BOM1

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPIO Extender

Size	Document Number	Rev
A4	**CD1 DIS**	SC

Date: Tuesday, December 13, 2011 Sheet 95 of 102

(Blanking)

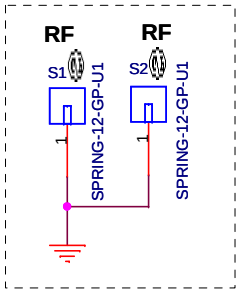
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

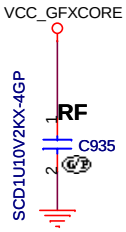
Title: ***Reserved***

Size	Document Number	Rev
A3	CD1 DIS	SC

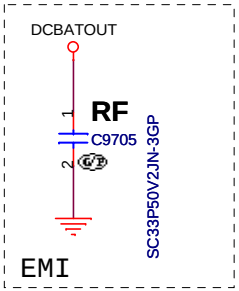
Date: Tuesday, December 13, 2011 Sheet 96 of 102

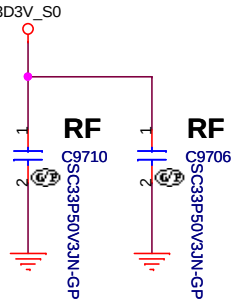


Only for BF UMA (11270) layout



close to PU4502

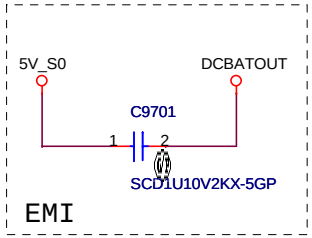




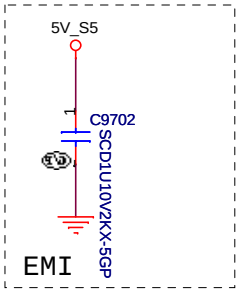
12/6 RF Solution Table:

Location		CD DIS	CD UMA	BF UMA
C1427	33PF	No_ASM	No_ASM	ASM
EC4601	33PF	ASM	ASM	No_ASM
PC4126	33PF	ASM	ASM	No_ASM
PC4120	33PF	ASM	ASM	No_ASM
PC4613	33PF	ASM	ASM	No_ASM
C9705	33PF	ASM	ASM	No_ASM
PC4622	330PF	ASM	ASM	No_ASM
PR4612	2.2ohm	ASM	ASM	No_ASM
C9710 C9706	33PF	No_ASM	No_ASM	ASM
C935	0.1uF	No_ASM	No_ASM	ASM
S1 S2	Spring	No_ASM	No_ASM	ASM

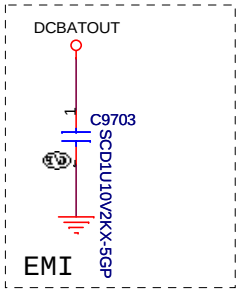
close to PC4134



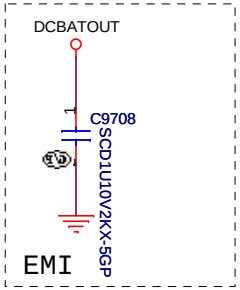
close to U3601



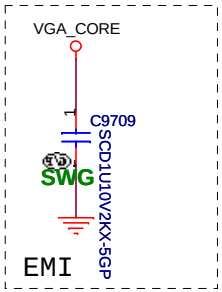
close to PR4004

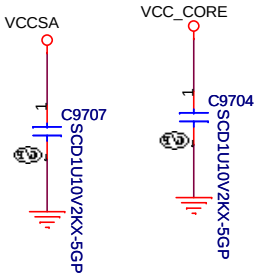


close to PR9209



close to R9101





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Title: ***EMI Capacitors***

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Schematic Change List

Date	Page number	Description	Remark
2011/07/12	28	Add U2802,R28015~R2818,C2810~C2811,RT2801~RT2814 for Thermister protection function.	
	22	Change R2211 to ASM.	
	49	Change LVDS connector reference to LVDS1 and pin1,5,37 NC.	
	66	Add R6610~R6612,C6612,U6602,U6603 for SMbus alternative path (Intel Anti-sheft 3.0)	
	17	Add intersheet connection for LPC_AD[3:0] and LPC_FRAME#.	
	45,....	Change power rail name VCCP_CPU to 1D05V_VTT, Delete PR4514 (for iAMT),Change 1D05V_LAN to 1D05V_S0.	
	69	Change net TP4CLKPAD to TP4CLK, net TP4DATAPAD to TP4DATA.	
	42	Remove PR4227,PR4229 because of double pull-up.	
	41	Change net I244143961 to 5V_S5.	
	27	Change pull-up power of FAN_ID to 3D3V_S0.	
2011/07/13	27	Reserve test pads TP2709,TP2710 for net KCOL16,KCOL17.	
	2	Remove Media card reader block right side.	
	28,86	Delete Q2801,Q2802,C2805,R2813,R2814,wire themal sensor channel1 to dGPU inside	
	52	Change DP net name to DPC to DPB of connector side.	
	92	Remove U9204,U9207 and output cap because of space reason.	
	93	Remove 1D8V_VGA_S0 power rail.Change 1V_VGA_S0 to 1D05V_VGA_PLL Add power for 1D05V_VGA_S0 power rail.	
	86,92,93	Change 3D3V_VGA_S0 to 3D3V_VGA.	
	93	Change 1D5V_VGA_S0 to 1D5V_VGA.	
	40,94	Change net -PWRSHUTDOWN to PURE_HW_SHUTDOWN#.	
	61	Change U6102.5 connecting to 5V_S5.	
2011/07/14	93	Remove LDE RD3552 and the 1D05V_VGA_PLL. Change net 1D05V_VGA_PLL to 1D05V_VGA.	
	83~87	Connect GPU core power named as "VGA_CORE", Connect 1D05V power named as"1D05V_VGA".	
	8	Remove R801 and PTC803 because of layout space reason.	
	46	Add PTC4603 (330UF BULK CAP).	
	45	Remove PTC4502 because of layout space reason.	
	42~44	Change CPU core power controller to ISL95838 because of layout requirement.	
2011/07/15	21,31	Reserve R3120,R3121 to select LAN power control by EC or PCH,change PCH GPIO14 as LAN_PWERON_PCH.	
	29	Add 10uF hook and DY on signal MIC_GPI.	
	27	Change EC pin16 from CAPSLOCK_LED# to PCIE_WAKE#.	
	28	Change Thermistor comparator power from VCC5M to 5V_S5.	
	85	Removed power supply to IFPx modules and add R8507~R8514 to pull down.	
	86	Removed power supply to DAC modules and add R8646 to pull down.let DAC I/O pins NC.	
	93	Add PC9336 0.22uF for DGPU power sequence adjustment.	
	84	Connect pin FB_CLAMP to GND, let pin FB_VREF NC.	
2011/07/16	28,86	Add pull up resistor R2819 net on net THERM_ALERT#.	
	69	Change TPFP1 type, remove pins for POA function.	
	86	Remove R8623~R8625.	
2011/07/17	18	Remove R1825 because of double pull down.	
2011/07/18	49	Change U4901 from GMT part to TI22922.	
	27	Change U2702 from GMT part to TPS3809,Remove R2710,R2713,R2718,R2724,R2726,R2741.	
	28,86	Connect GPU GPIO9 signal VIDEO_THERM_ALERT# to thermal sensor ALERT pin.	
	69	Update TPFP1 pin assignment.	
2011/07/19	45	Remove PR4517, Cahnge net 1.05VTT_PWRGD to 1D05VTT_PWRGD.	
	66	Change U6602,U6603 pin1 to SMB_DATA_WWAN,SMB_CLK_WWAN.	
	21,63,82	Change BLUETOOH LED control from PCH to BLUETOOTH, Add R2108 as pull up of REQ2#.	
	5	Remove R511,R516 because of duplication.	
	26	Move R2602 from XDP_DBRESET# to PM_RSMRST#, and correct connection of PXDP1 pin 10,17,18.	
	18,22,27	Correct EC_SCI#,EC_SMI#,EC_SWI connection,leave only EC_SCI# from PCH to EC.	
	14,15	Add C1423,C1424,C1425,C1426,C1503,C1504,C1517,C1522 for VREF CA,VREF DQ power. Add 10uF caps C1427,C1523,C1524 on 0D75V_S0.	
	66	Add C6613,C6614,C6615,C6616 for mSATA.	
	18	Change RN1802 as pull up SMB_CLK_PCH/SMBDATA_PCH	
	56	Remove connection of SATA_ODD_DA# and RN2102.	
2011/07/19	9	C934 pin2 change to GND	
	42	PR4230 pin1 and PR4229 pin1 change to 1D05V_VTT	
	13	Del 3D3V_PCIE_AOAC PWR Plane	
	66	Change RN6601 pin1,2 net name to SMB_CLK_WWAN and SMB_DATA_WWAN	
	69	Del RN6901	
	77	Cut U7701 pin15	
	82	RJBD1 pin34 change to LED_BDC_ON	
	93	Change net name to 1D05V_VGA_EN	
2011/07/20	17	PCH_JTAG_TDI keep PU to follow LKN4	
	93	PR9335 pin2 change to 1D5V_ENABLE,R9326 change to SWG,R9327 change to DY to adjust GPU power up sequence.	
	43,44	Add PC4312, PC4313, PC4314 for EMI	

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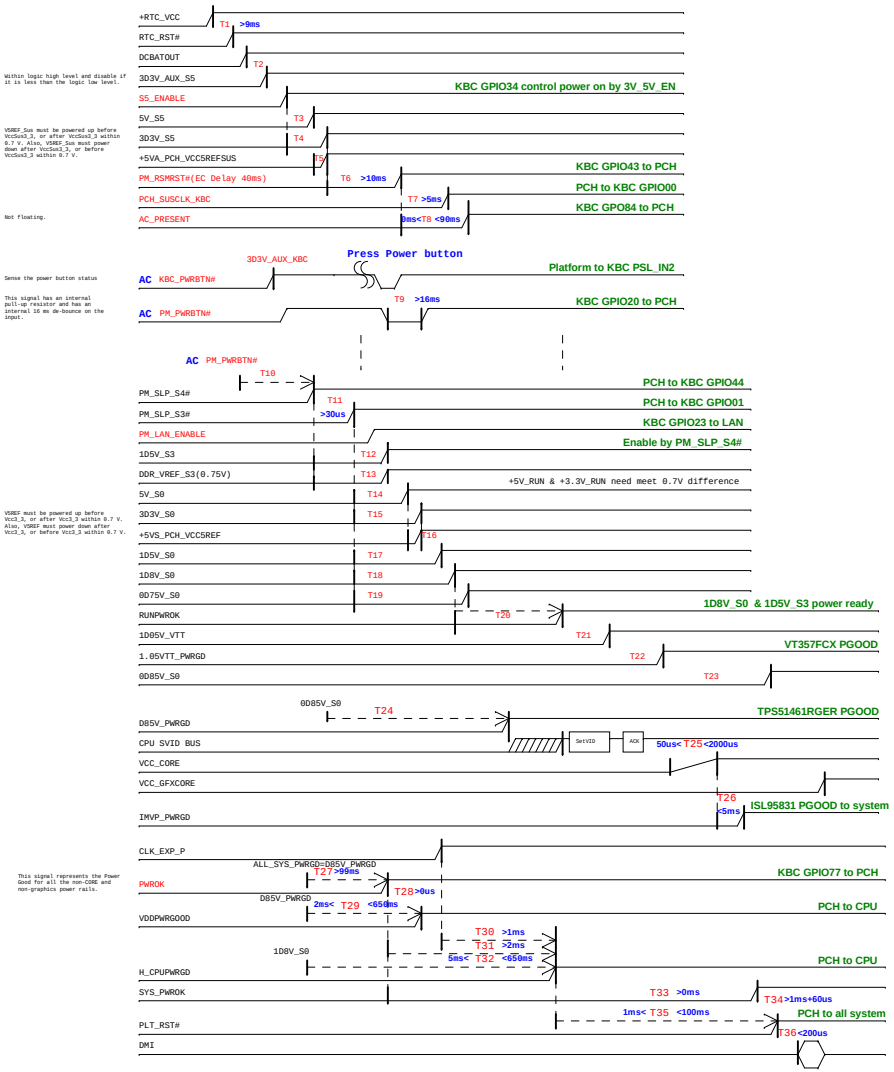
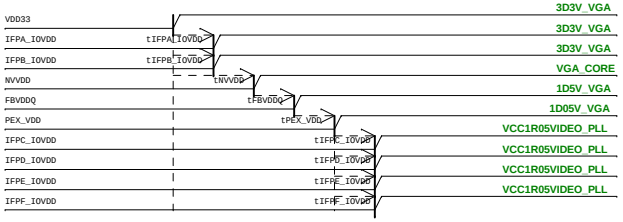
Chief River Platform Power Sequence

(AC mode)

red word: KBC GPIO

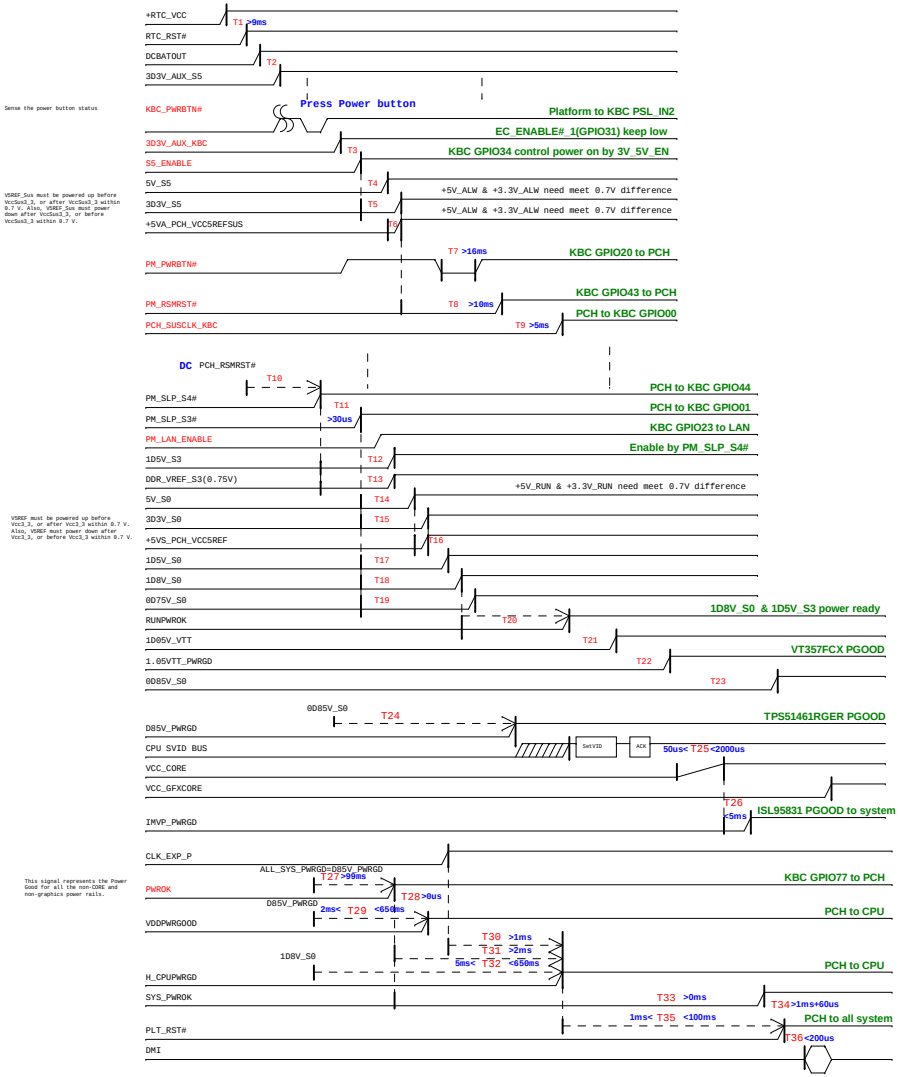


NVIDIA



(DC mode)

red word: KBC GPIO



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Title: Power Sequence		
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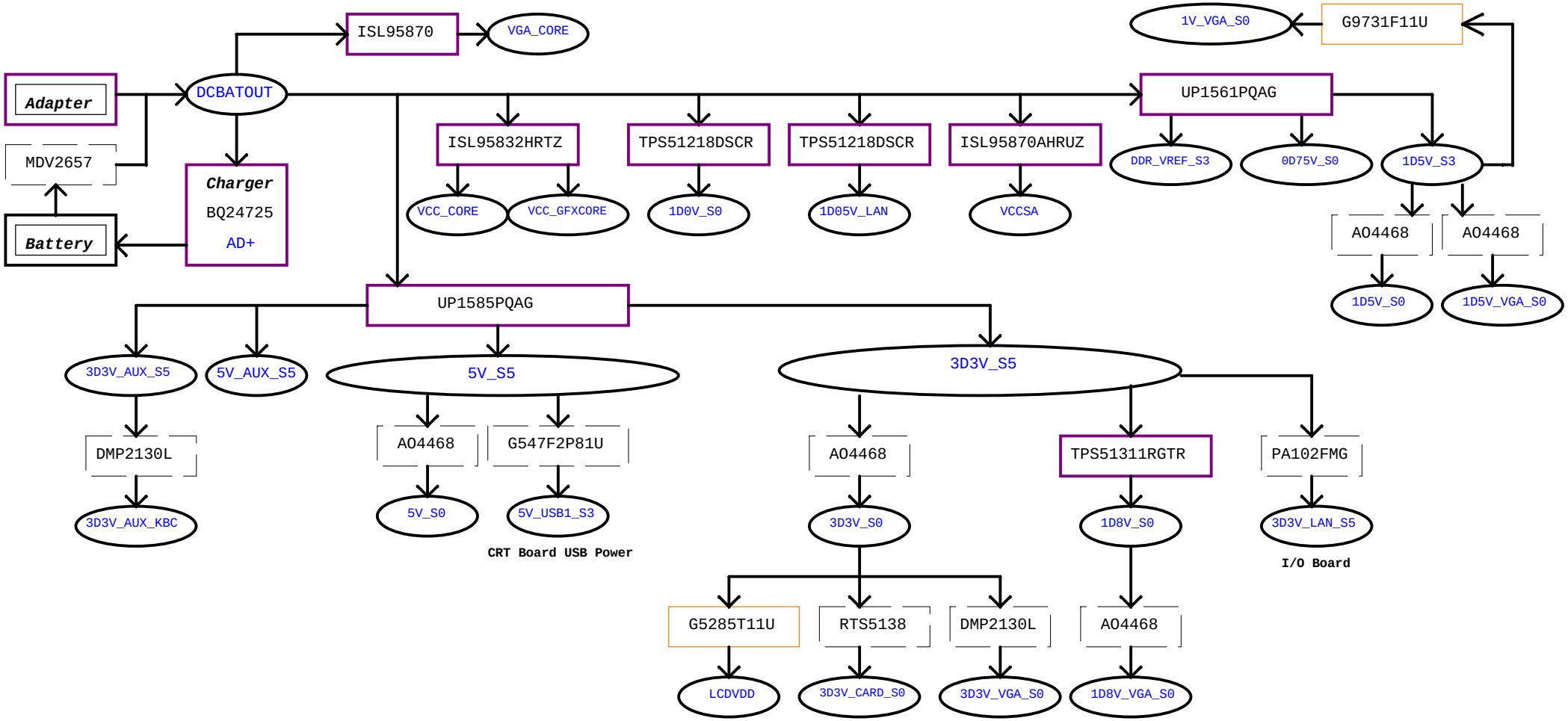

Power Shape

Regulator	LDO	Switch

BOM1

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Title: ***Power Block Diagram***

Size	Document Number	Rev
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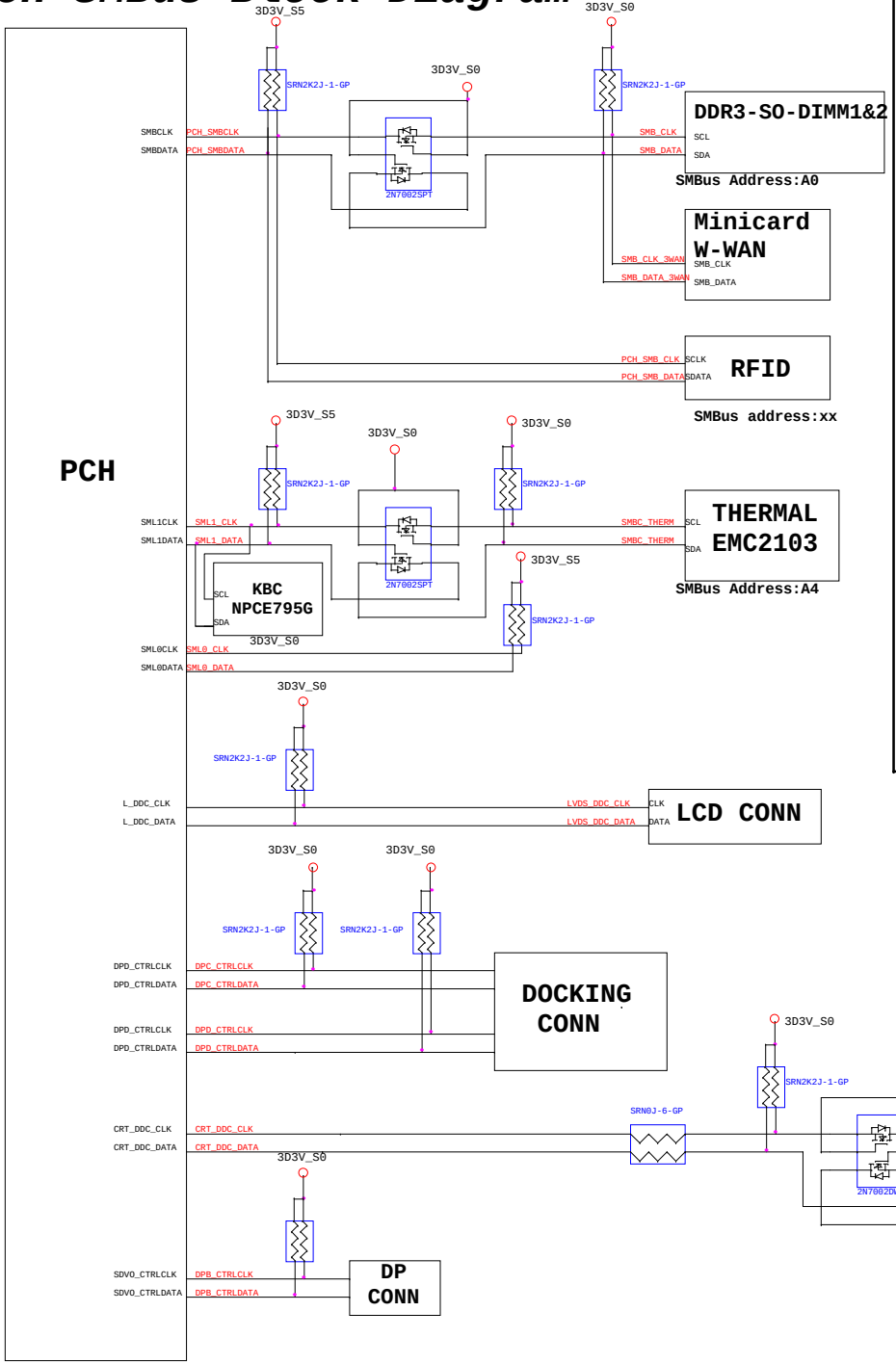
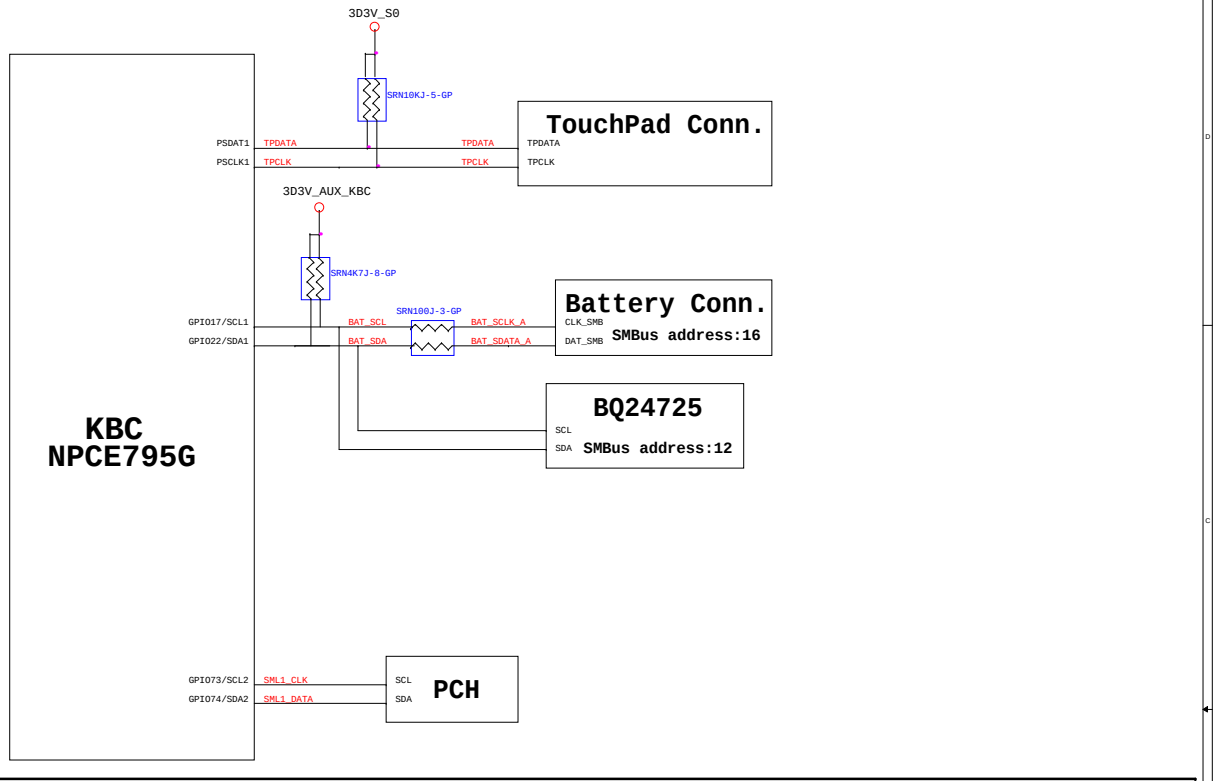
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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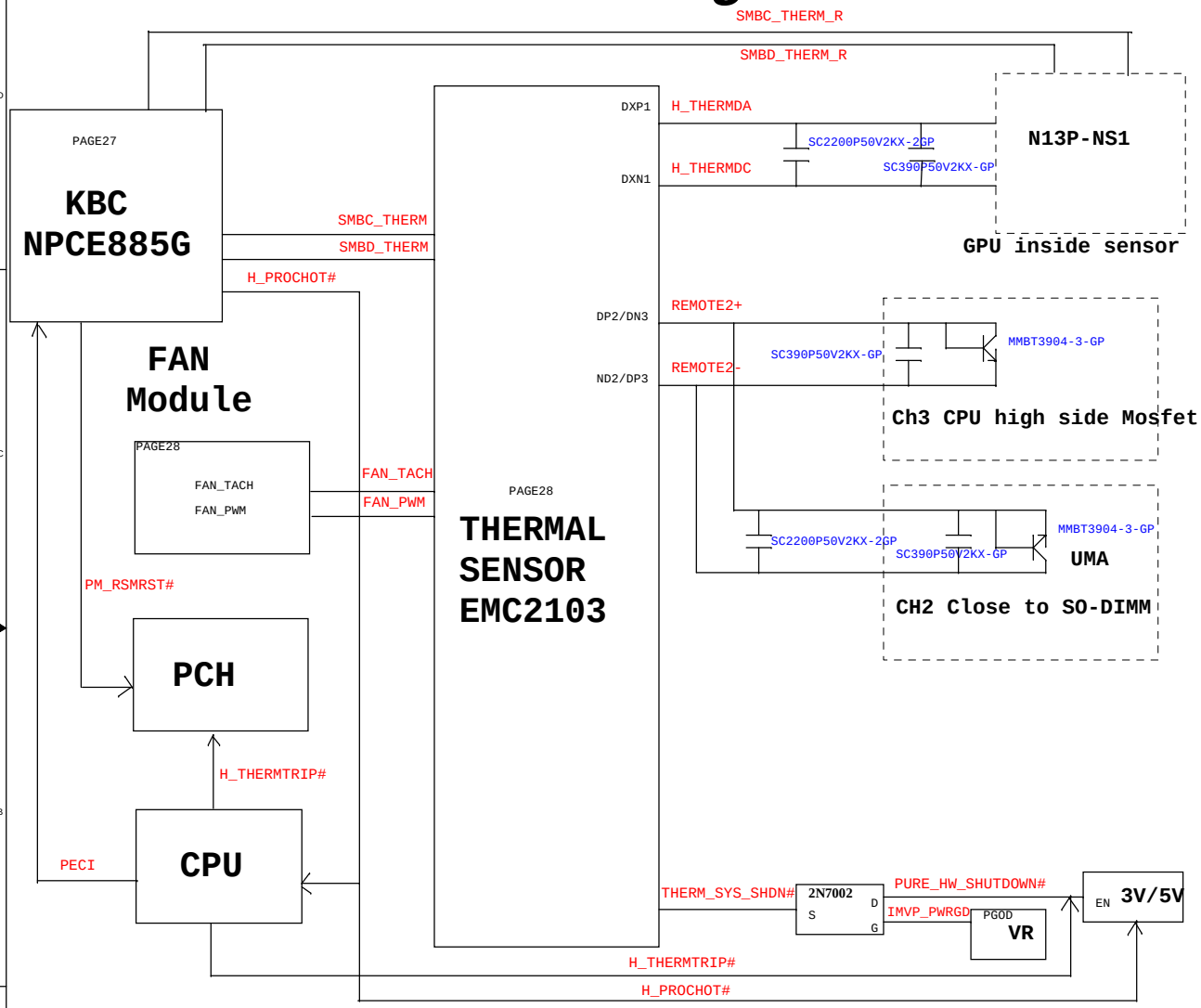
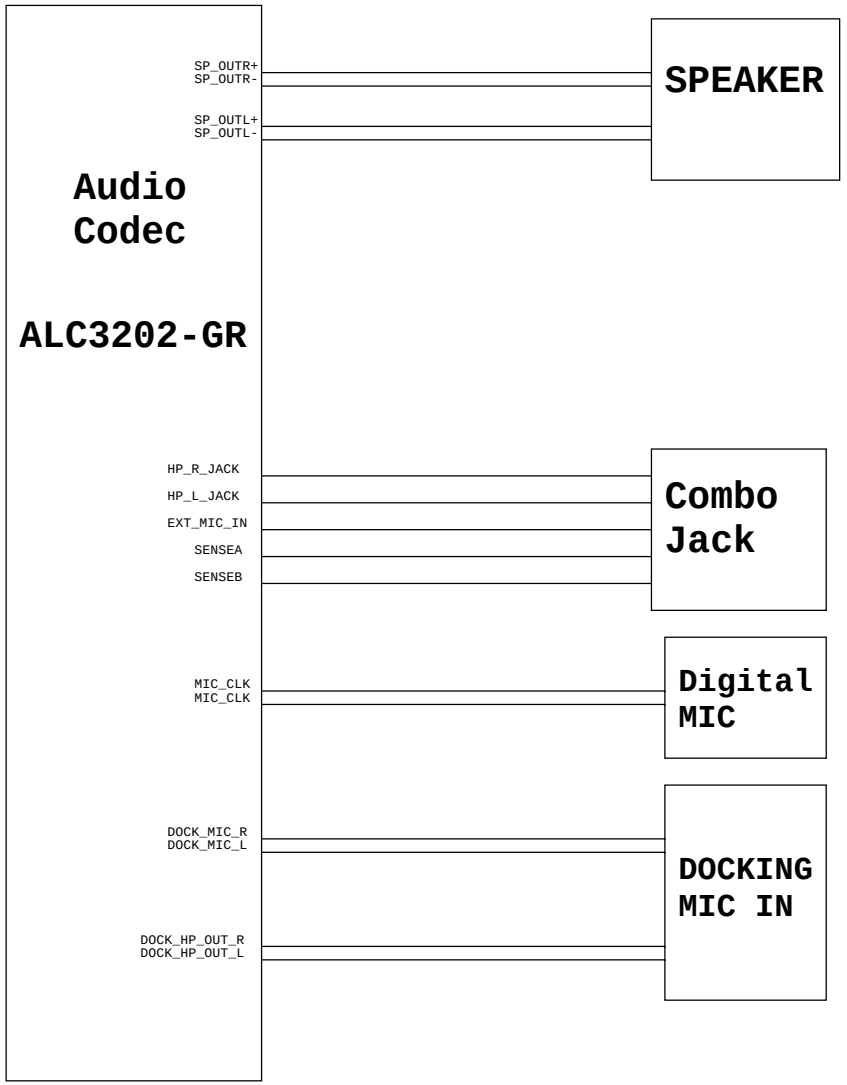
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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