VIQY1

(Y510)

NM_A032 Rev1.0 Schematic

Intel Haswell Processor with DDRIII + Lynx point PCH
nVIDIA N14P GT + 2nd VGA N14P GT

2013-03-19 Rev1.0

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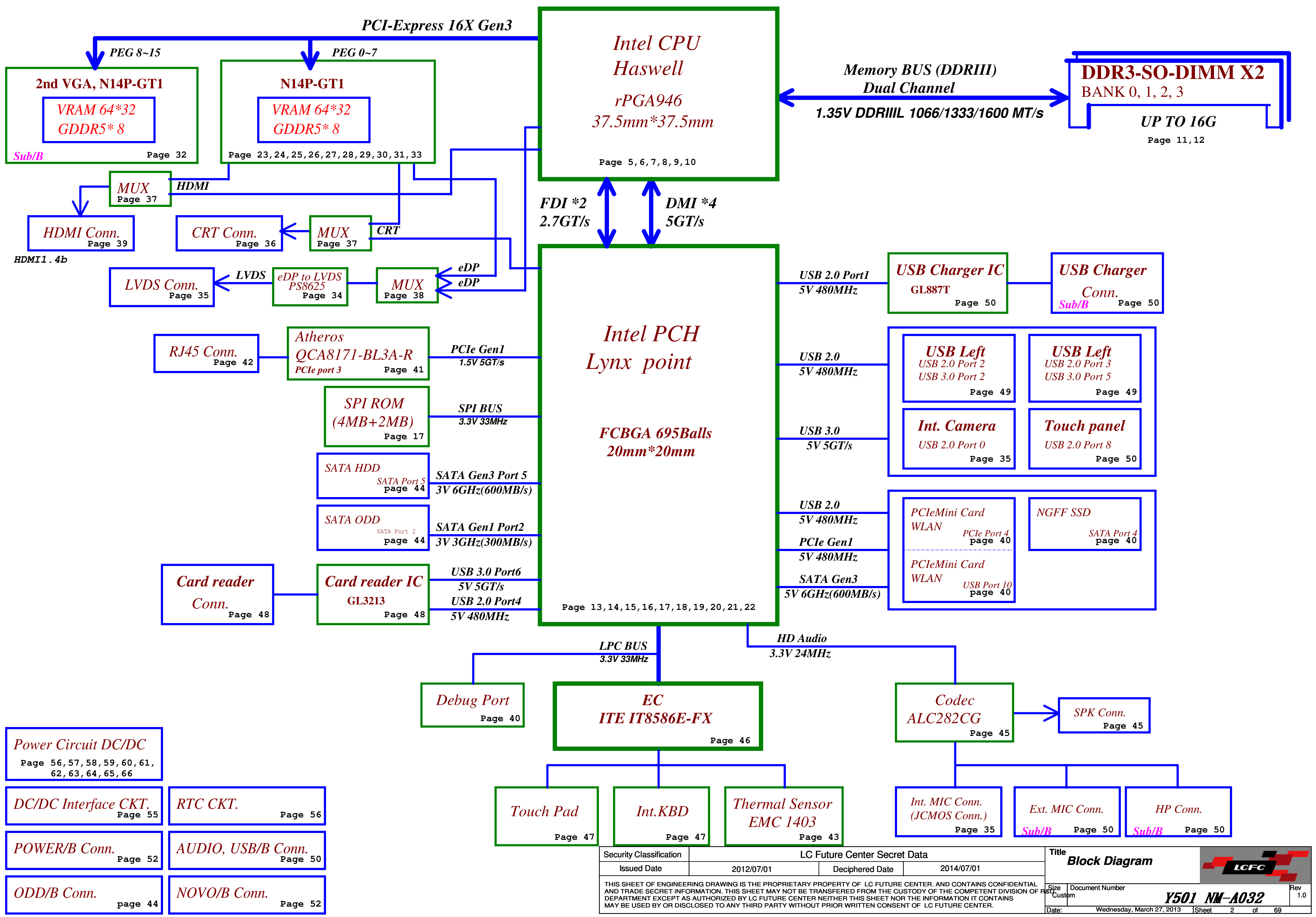
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title **Cover Page**

LCFC

Size Custom
Document Number **Y510 NM-A032**
Rev 1.0

Date: Wednesday, March 27, 2013



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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
Block Diagram

LCFC

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0		Port	4 External USB Port
EHCI1	XHCI		0	Camera
			1	USB Port (Right Side)
		2	2	USB Port (Left Side)
		5	3	USB Port (Left Side)
		6	4	Card Reader
			5	
			6	
			7	
EHCI2			8	Touch panel
			9	
			10	Mini Card(WLAN)
			11	
			12	
			13	

BOM Structure Table

BOM Structure	BTO Item
GT@	NV GT750M
GT1@	NV GT755M
CMOS@	CMOS Camera part
SURGE@	QCA8171 LAN surge part
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
@	Unpop
DS3@	Deep S3 support part
daul@	Support daul channel panel function
887T@	GENESYS 887T USB charger solution
887@	GENESYS 887 USB charger solution
TI@	TI USB charger solution
EDP@	Support EDP panel function
SLI@	For SLI function part
47W@	For 47W CPU part
37W@	For 37W CPU part

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
SMB_CLK_S3 SMB_DATA_S3	PCH +3VS	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIE PORT LIST

Port	Device
1	
2	
3	
4	LAN
5	WLAN
6	
7	
8	

Address

EC SM Bus1 address

Device	
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

ZZZ1
DAZ0SF00100

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Title **Notes List**

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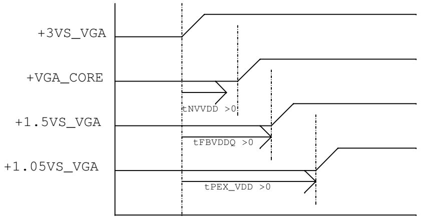
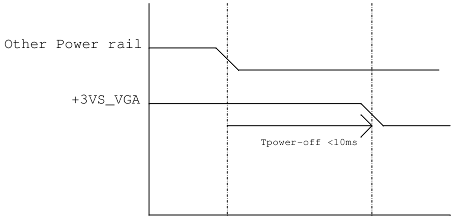
Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N14Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	IN	-	FB_CLAMP_MON
GPIO1	OUT	-	NA
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	NA
GPIO6	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO7	OUT	-	NA
GPIO8	OUT	-	OVERT#
GPIO9	OUT	-	VGA_ALERT#
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	NVVDD PWM_VID
GPIO12	IN	-	AC Power Detect Input (10K pull High)
GPIO13	OUT	-	DPRSLPVR_VGA
GPIO14	OUT	-	NA
GPIO15	IN	-	NA
GPIO16	OUT	-	NA
GPIO17	IN	-	VGA_EDP_HPD
GPIO18	IN	-	DGPU_HDMI_HPD
GPIO19	IN	-	NA



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GT (28nm)	0x0FCD

	setting	I2C Slave addrees ID
SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
	1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N14P-GT 28nm	PU 10K	PD 15K	PU 45K	PD 5K	PD 25K	PU 5K	PD 45K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU		N14P-GT	N14P-GT1	
FB Memory (GDDR5)		ROM_SI	ROM_SI	
Samsung 3000MHz	K4G20325FD-FC03			
	64Mx32		PD 30K	
Hynix 3000MHz	H5GQ2H24AFR-R0C			
	64Mx32		PD 25K	
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24AFR-T2C			
	64Mx32	PD 25K		

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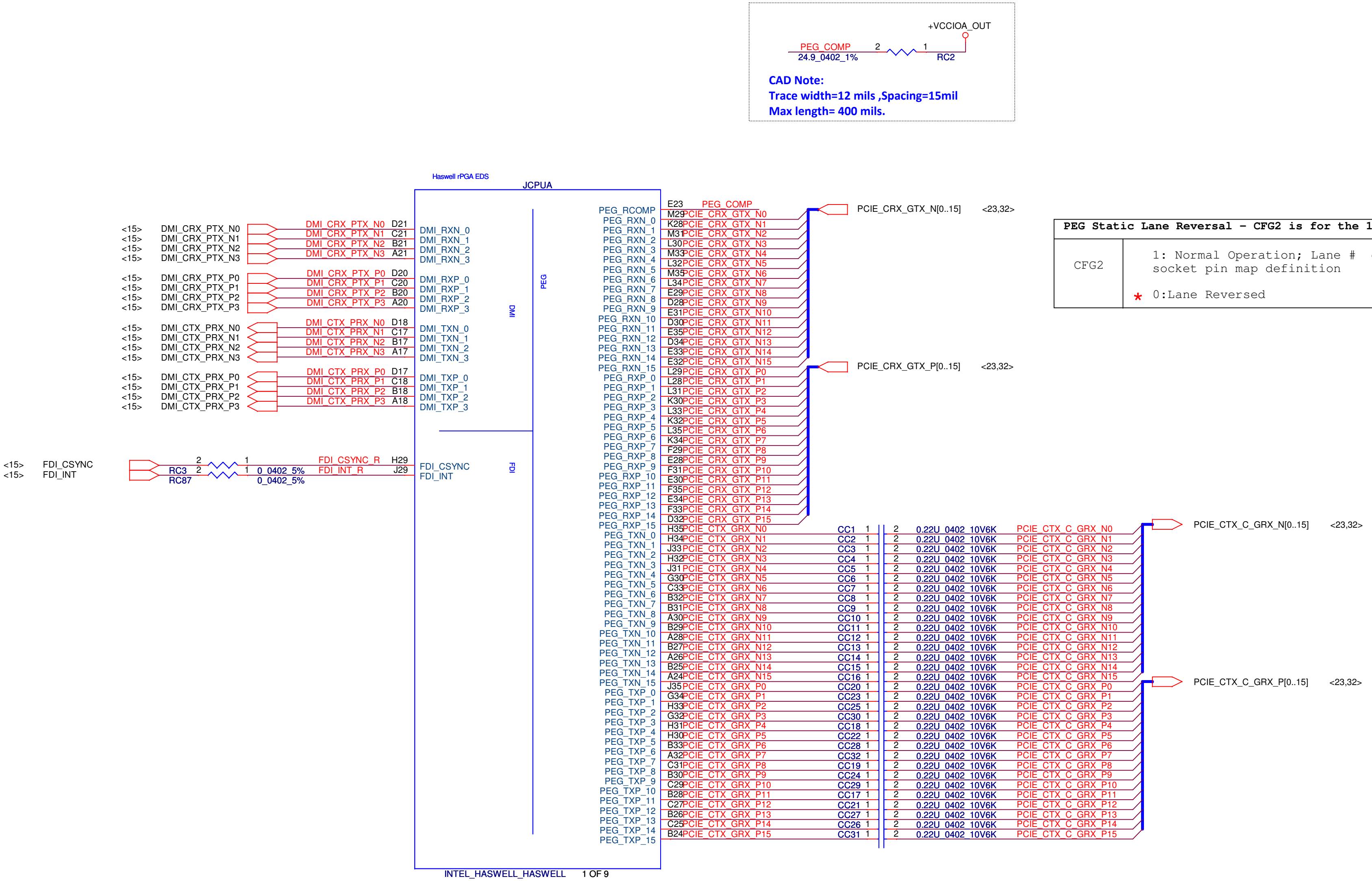
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Haswell rPGA EDS
JCPUA
DMI
PEG
FDI
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<15> DMI_CTX_PRX_P2 DMI_CTX_PRX_P2 B18 DMI_TXP_2
<15> DMI_CTX_PRX_P3 DMI_CTX_PRX_P3 A18 DMI_TXP_3
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<15> FDI_INT RC87 2 1 0_0402_5% FDI_INT_R J29 FDI_INT
PEG_RCOMP E23 PEG_COMP
PEG_RXN_0 M29 PCIE_CRX_GTX_N0
PEG_RXN_1 K28 PCIE_CRX_GTX_N1
PEG_RXN_2 M31 PCIE_CRX_GTX_N2
PEG_RXN_3 L30 PCIE_CRX_GTX_N3
PEG_RXN_4 M33 PCIE_CRX_GTX_N4
PEG_RXN_5 L32 PCIE_CRX_GTX_N5
PEG_RXN_6 M35 PCIE_CRX_GTX_N6
PEG_RXN_7 L34 PCIE_CRX_GTX_N7
PEG_RXN_8 E29 PCIE_CRX_GTX_N8
PEG_RXN_9 D28 PCIE_CRX_GTX_N9
PEG_RXN_10 E31 PCIE_CRX_GTX_N10
PEG_RXN_11 D30 PCIE_CRX_GTX_N11
PEG_RXN_12 E35 PCIE_CRX_GTX_N12
PEG_RXN_13 D34 PCIE_CRX_GTX_N13
PEG_RXN_14 E33 PCIE_CRX_GTX_N14
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PEG_RXP_5 K32 PCIE_CRX_GTX_P5
PEG_RXP_6 L35 PCIE_CRX_GTX_P6
PEG_RXP_7 K34 PCIE_CRX_GTX_P7
PEG_RXP_8 F29 PCIE_CRX_GTX_P8
PEG_RXP_9 E28 PCIE_CRX_GTX_P9
PEG_RXP_10 F31 PCIE_CRX_GTX_P10
PEG_RXP_11 E30 PCIE_CRX_GTX_P11
PEG_RXP_12 F35 PCIE_CRX_GTX_P12
PEG_RXP_13 E34 PCIE_CRX_GTX_P13
PEG_RXP_14 F33 PCIE_CRX_GTX_P14
PEG_RXP_15 D32 PCIE_CRX_GTX_P15
PCIE_CRX_GTX_P[0..15] <23,32>
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PEG_TXN_3 H32 PCIE_CTX_GRX_N3 CC4 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N3
PEG_TXN_4 J31 PCIE_CTX_GRX_N4 CC5 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N4
PEG_TXN_5 G30 PCIE_CTX_GRX_N5 CC6 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N5
PEG_TXN_6 C33 PCIE_CTX_GRX_N6 CC7 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N6
PEG_TXN_7 B32 PCIE_CTX_GRX_N7 CC8 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N7
PEG_TXN_8 B31 PCIE_CTX_GRX_N8 CC9 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N8
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PCIE_CTX_C_GRX_P[0..15] <23,32>
INTEL_HASWELL_HASWELL 1 OF 9

CAD Note:
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

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CPU (1/7) DMI, FDI, PEG

LCFC

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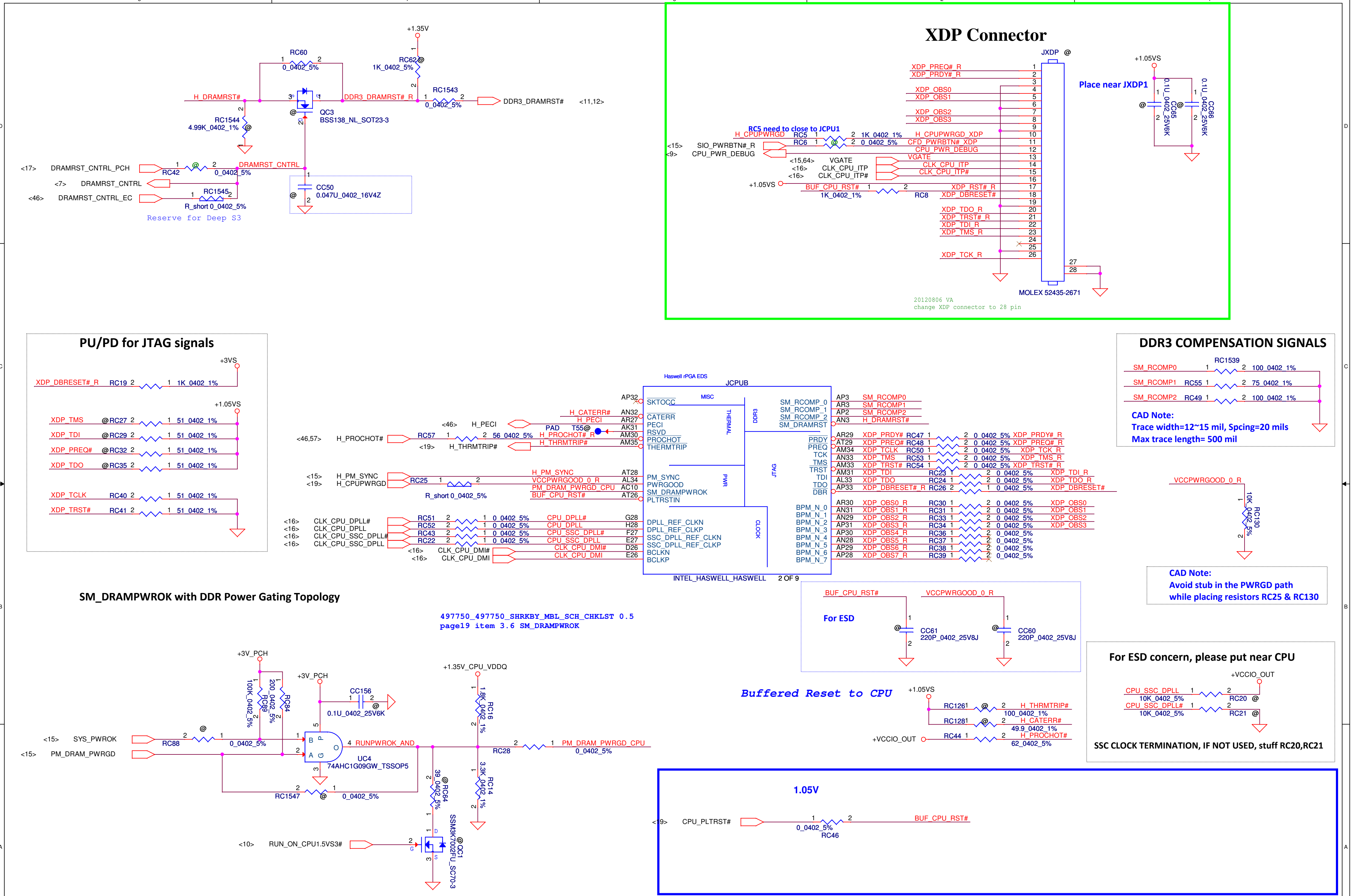
XDP Connector
JXDP @
+1.05VS
Place near JXDP1
CC65 0.1U_0402_25V6K
CC66 0.1U_0402_25V6K
XDP_PREQ#_R
XDP_PRDY#_R
XDP_OBS0
XDP_OBS1
XDP_OBS2
XDP_OBS3
RC5 need to close to JCPU1
H_CPUPWRGD
RC5 1K_0402_1%
RC6 0_0402_5%
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BUF_CPU_RST#
RC8 1K_0402_1%
XDP_RST#_R
XDP_DBRESET#_R
XDP_TDO_R
XDP_TRST#_R
XDP_TDI_R
XDP_TMS_R
XDP_TCK_R
MOLEX 52435-2671
20120806 VA
change XDP connector to 28 pin
+1.35V
RC60 0_0402_5%
RC62 @ 1K_0402_5%
H_DRAMRST#
QC3 BSS138_NL_SOT23-3
DDR3_DRAMRST#_R
RC1543 0_0402_5%
DDR3_DRAMRST# <11,12>
RC1544 4.99K_0402_1% @
<17> DRAMRST_CNTRL_PCH
RC42 0_0402_5%
DRAMRST_CNTRL
<7> DRAMRST_CNTRL
<46> DRAMRST_CNTRL_EC
RC1545 R_short 0_0402_5%
CC50 0.047U_0402_16V4Z
Reserve for Deep S3
PU/PD for JTAG signals
+3VS
XDP_DBRESET#_R RC19 1K_0402_1%
+1.05VS
XDP_TMS @RC27 51_0402_1%
XDP_TDI @RC29 51_0402_1%
XDP_PREQ# @RC32 51_0402_1%
XDP_TDO @RC35 51_0402_1%
XDP_TCLK RC40 51_0402_1%
XDP_TRST# RC41 51_0402_1%
Haswell rPGA EDS
JCPUB
MISC THERMAL DDR3 JTAG PWR CLOCK
SKTOCC CATERR PECI RSVD PROCHOT THERMTRIP
PM_SYNC PWRGOOD SM_DRAMPWROK PLTRSTIN
DPLL_REF_CLKN DPLL_REF_CLKP SSC_DPLL_REF_CLKN SSC_DPLL_REF_CLKP BCLKN BCLKP
SM_RCOMP_0 SM_RCOMP_1 SM_RCOMP_2 SM_DRAMRST
PRDY PREQ TCK TMS TRST TDI TDO DBR
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INTEL_HASWELL_HASWELL 2 OF 9
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XDP_TMS RC53 0_0402_5% XDP_TMS_R
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XDP_TDI RC23 0_0402_5% XDP_TDI_R
XDP_TDO RC24 0_0402_5% XDP_TDO_R
XDP_DBRESET#_R RC26 0_0402_5% XDP_DBRESET#
XDP_OBS0_R RC30 0_0402_5% XDP_OBS0
XDP_OBS1_R RC31 0_0402_5% XDP_OBS1
XDP_OBS2_R RC33 0_0402_5% XDP_OBS2
XDP_OBS3_R RC34 0_0402_5% XDP_OBS3
XDP_OBS4_R RC36 0_0402_5%
XDP_OBS5_R RC37 0_0402_5%
XDP_OBS6_R RC38 0_0402_5%
XDP_OBS7_R RC39 0_0402_5%
DDR3 COMPENSATION SIGNALS
SM_RCOMP0 RC1539 100_0402_1%
SM_RCOMP1 RC55 75_0402_1%
SM_RCOMP2 RC49 100_0402_1%
VCCPWRGOOD_0_R RC130 10K_0402_5%
BUF_CPU_RST# VCCPWRGOOD_0_R
For ESD
CC61 220P_0402_25V8J
CC60 220P_0402_25V8J
SM_DRAMPWROK with DDR Power Gating Topology
497750_497750_SHRKBY_MBL_SCH_CHKLST 0.5
page19 item 3.6 SM_DRAMPWROK
+3V_PCH
RC89 100K_0402_5%
RC84 200_0402_5%
CC156 0.1U_0402_25V6K
<15> SYS_PWROK RC88 0_0402_5%
<15> PM_DRAM_PWRGD
UC4 74AHC1G09GW_TSSOP5
RUNPWROK_AND
RC1547 @ 0_0402_5%
+1.35V_CPU_VDDQ
RC16 1.8K_0402_1%
RC28 0_0402_5% PM_DRAM_PWRGD_CPU
RC14 3.3K_0402_1%
RC64 39_0402_5%
<10> RUN_ON_CPU1.5VS3#
QC1 @ SSM3K7002FU_SC70-3
Buffered Reset to CPU
+1.05VS
RC1261 @ 100_0402_1% H_THRMTRIP#
RC1281 @ 49.9_0402_1% H_CATERR#
+VCCIO_OUT RC44 62_0402_5% H_PROCHOT#
For ESD concern, please put near CPU
+VCCIO_OUT
CPU_SSC_DPLL RC20 @ 10K_0402_5%
CPU_SSC_DPLL# RC21 @ 10K_0402_5%
SSC CLOCK TERMINATION, IF NOT USED, stuff RC20,RC21
1.05V
<9> CPU_PLTRST# RC46 0_0402_5% BUF_CPU_RST#

CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC25 & RC130

Security Classification	LC Future Center Secret Data			Title
Issued Date	2012/07/01	Deciphered Date	2014/07/01	CPU (2/7) PM, XDP, CLK

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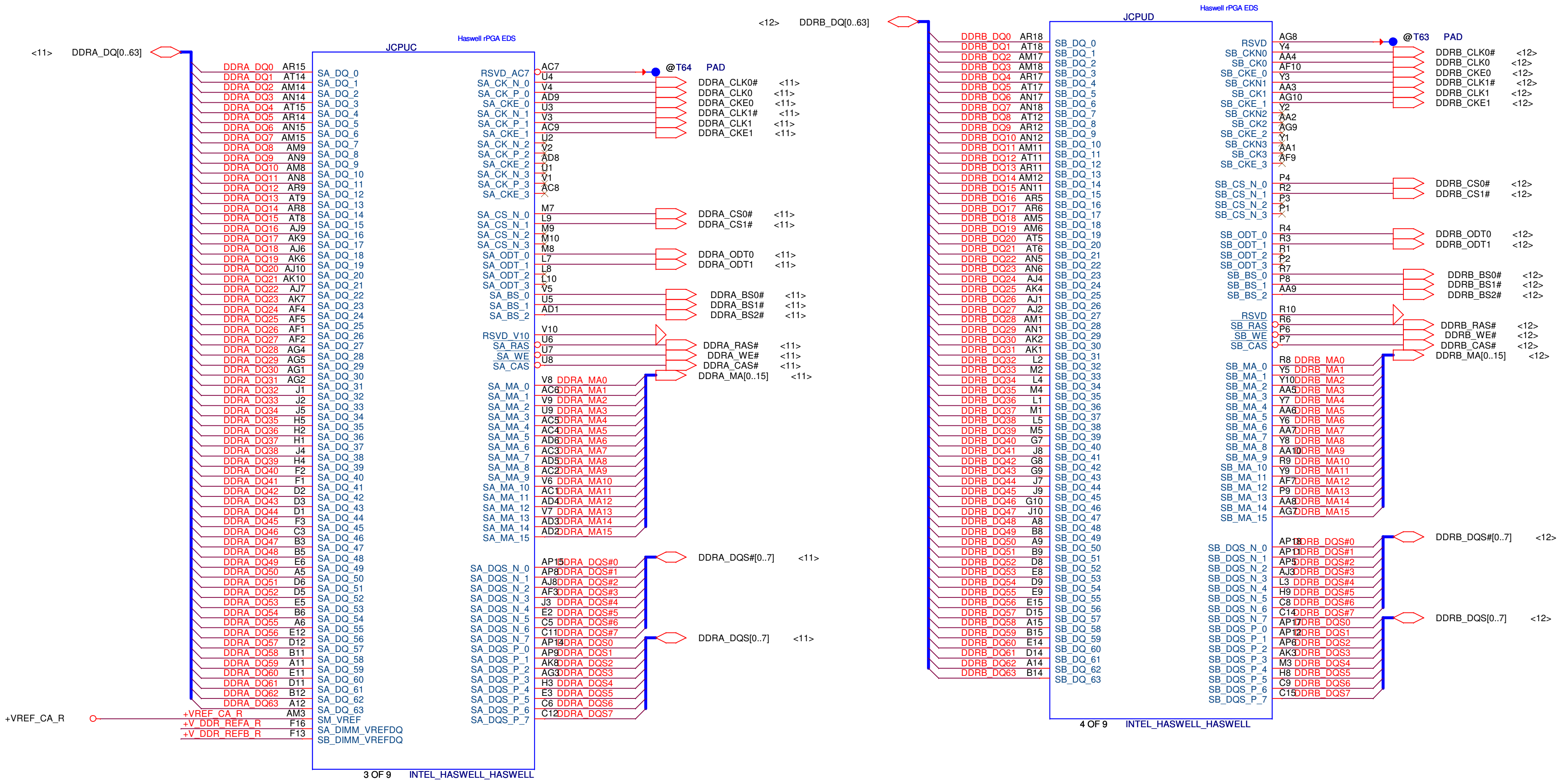
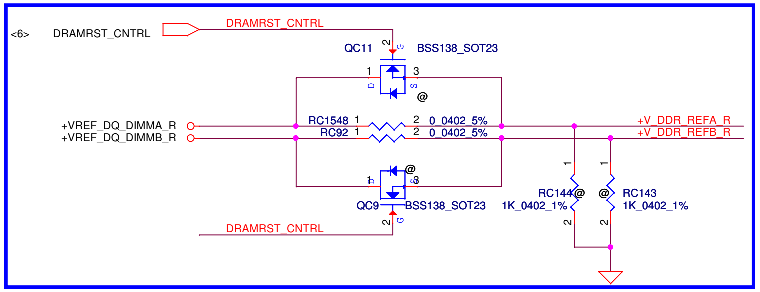
Size	Document Number	Rev
Custom	Y501 NM-A032	1.0

Date: Wednesday, March 27, 2013 Sheet 6 of 69





6/8: Add M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

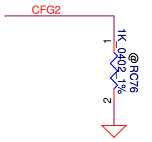
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
CPU (3/7) DDRIII

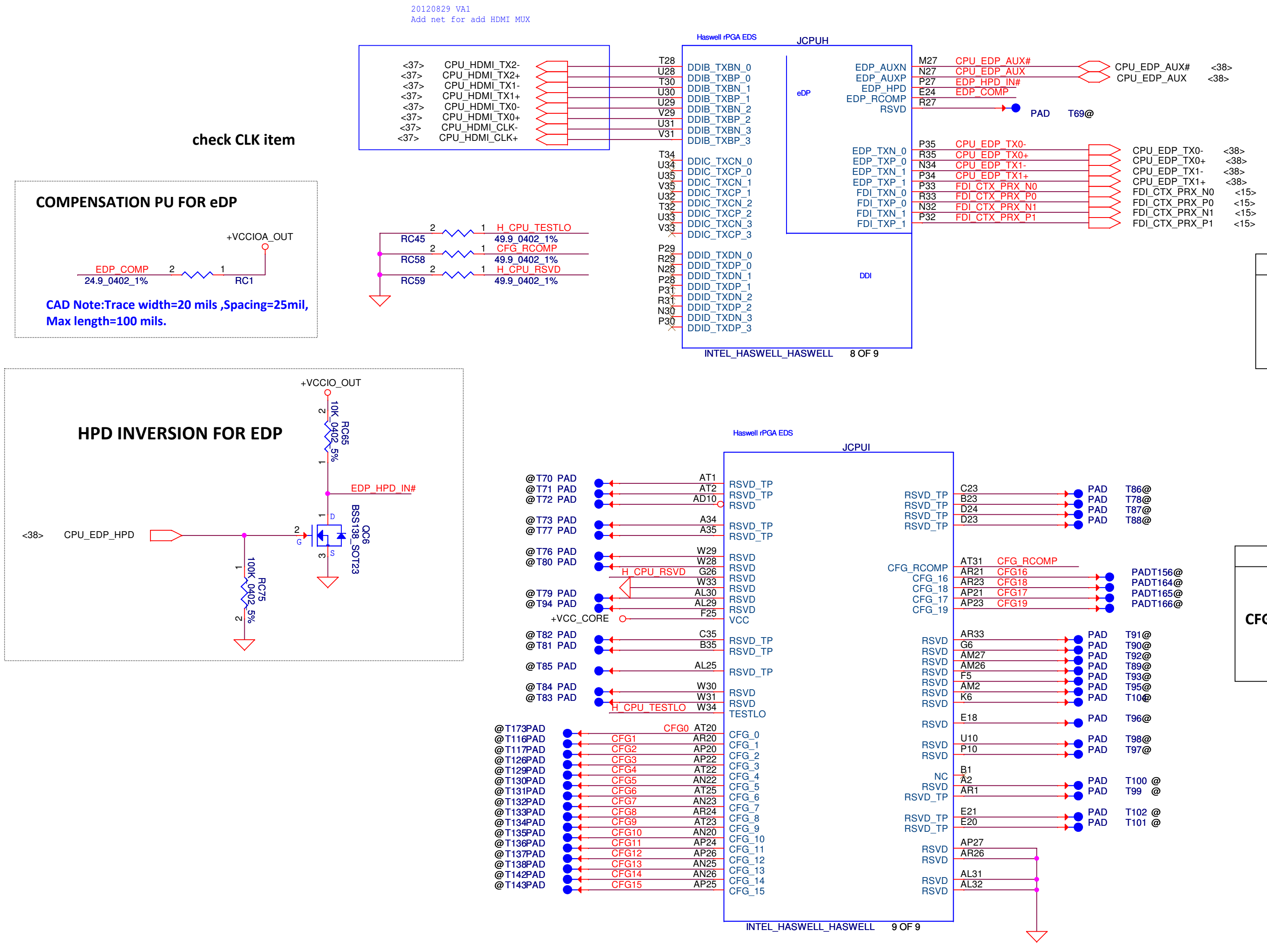
LCFC

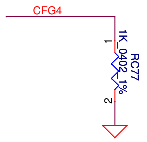
Size: Custom
Document Number: Y501 NM-A032
Rev: 1.0
Date: Wednesday, March 27, 2013

CFG STRAPS for CPU

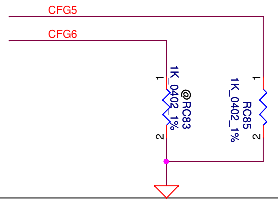


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

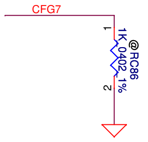




Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled * 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
CPU (4/7) RSVD,CFG

Size: Custom
Document Number: Y501 NM-A032
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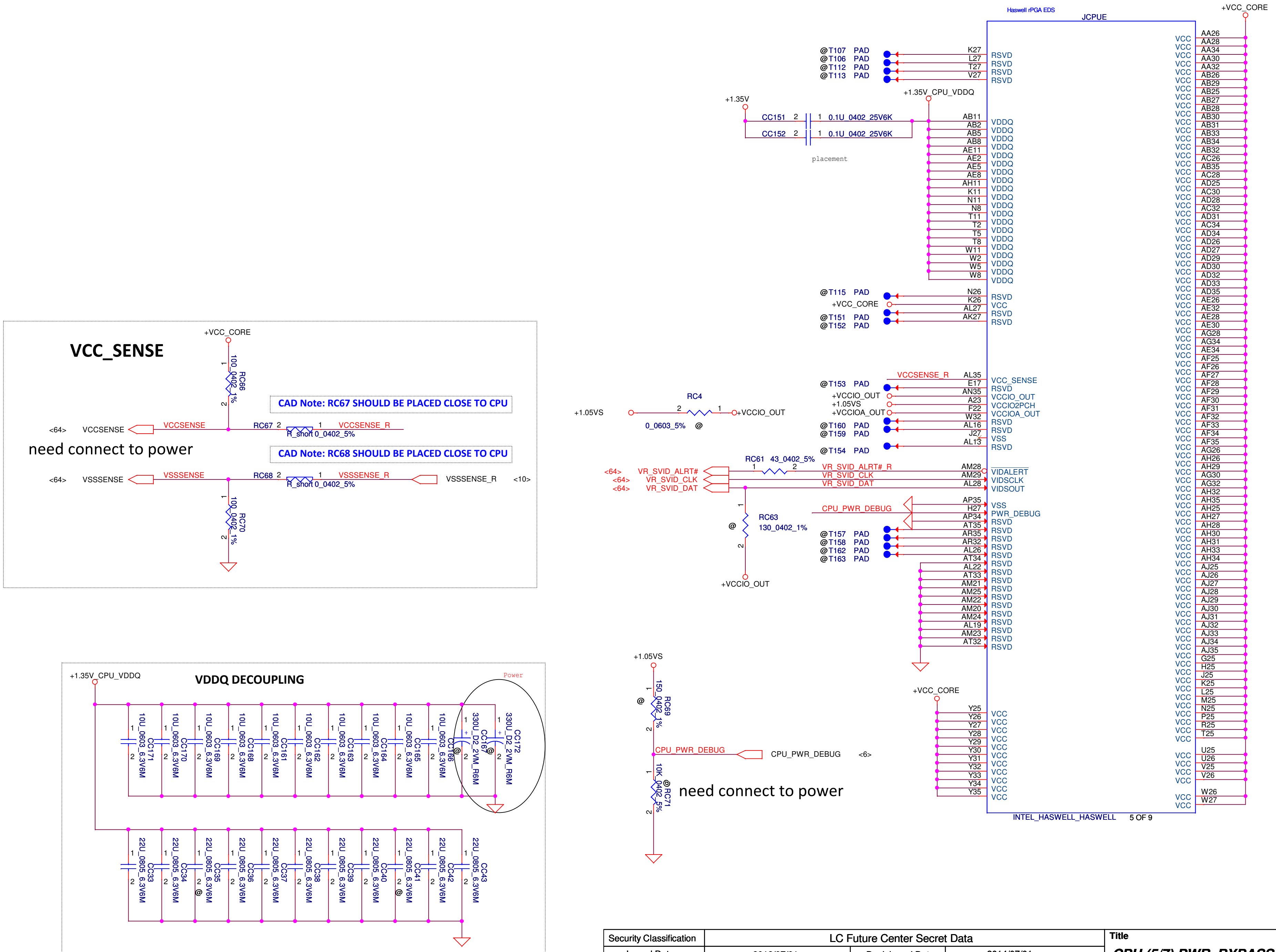
Date: Wednesday, March 27, 2013
Sheet 8 of 69



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Title

CPU (5/7) PWR, BYPASS

LCFC

Size: Custom
Document Number: Y501 NM-A032
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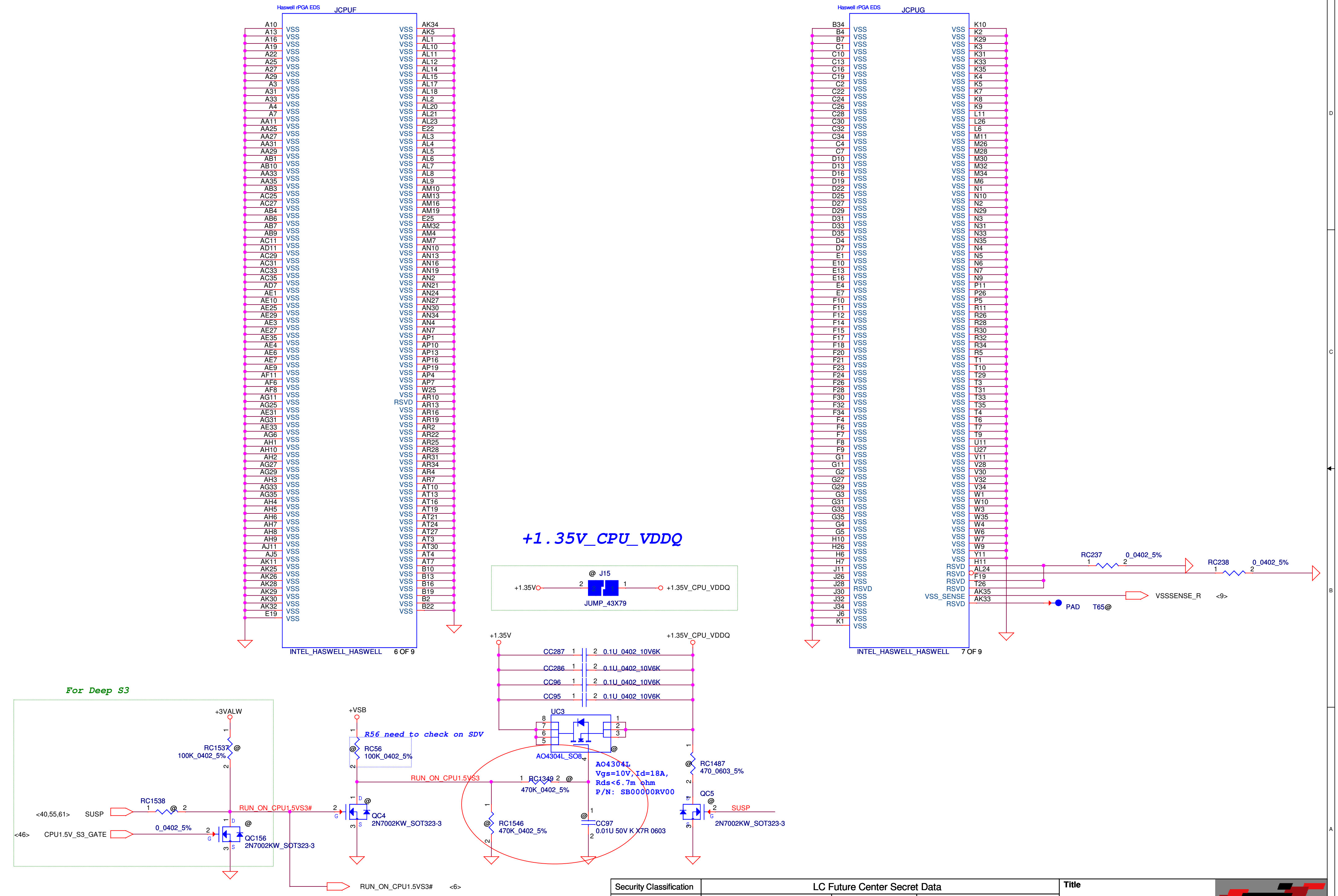
Date: Wednesday, March 27, 2013
Sheet 9 of 69


Haswell rPGA EDS
JCPUF
A10 A13 A16 A19 A22 A25 A27 A29 A3 A31 A33 A4 A7 AA11 AA25 AA27 AA31 AA29 AB1 AB10 AA33 AA35 AB3 AC25 AC27 AB4 AB6 AB7 AB9 AC11 AD11 AC29 AC31 AC33 AC35 AD7 AE1 AE10 AE25 AE29 AE3 AE27 AE35 AE4 AE6 AE7 AE9 AF11 AF6 AF8 AG11 AG25 AE31 AG31 AE33 AG6 AH1 AH10 AH2 AG27 AG29 AH3 AG33 AG35 AH4 AH5 AH6 AH7 AH8 AH9 AJ11 AJ5 AK11 AK25 AK26 AK28 AK29 AK30 AK32 E19
VSS
AK34 AK5 AL1 AL10 AL11 AL12 AL14 AL15 AL17 AL18 AL2 AL20 AL21 AL23 E22 AL3 AL4 AL5 AL6 AL7 AL8 AL9 AM10 AM13 AM16 AM19 E25 AM32 AM4 AM7 AN10 AN13 AN16 AN19 AN2 AN21 AN24 AN27 AN30 AN34 AN4 AN7 AP1 AP10 AP13 AP16 AP19 AP4 AP7 W25 AR10 AR13 AR16 AR19 AR2 AR22 AR25 AR28 AR31 AR34 AR4 AR7 AT10 AT13 AT16 AT19 AT21 AT24 AT27 AT3 AT30 AT4 AT7 B10 B13 B16 B19 B2 B22
RSVD
INTEL_HASWELL_HASWELL
6 OF 9
Haswell rPGA EDS
JCPUG
B34 B4 B7 C1 C10 C13 C16 C19 C2 C22 C24 C26 C28 C30 C32 C34 C4 C7 D10 D13 D16 D19 D22 D25 D27 D29 D31 D33 D35 D4 D7 E1 E10 E13 E16 E4 E7 F10 F11 F12 F14 F15 F17 F18 F20 F21 F23 F24 F26 F28 F30 F32 F34 F4 F6 F7 F8 F9 G1 G11 G2 G27 G29 G3 G31 G33 G35 G4 G5 H10 H26 H6 H7 J11 J26 J28 J30 J32 J34 J6 K1
K10 K2 K29 K3 K31 K33 K35 K4 K5 K7 K8 K9 L11 L26 L6 M11 M26 M28 M30 M32 M34 M6 N1 N10 N2 N29 N3 N31 N33 N35 N4 N5 N6 N7 N9 P11 P26 P5 R11 R26 R28 R30 R32 R34 R5 T1 T10 T29 T3 T31 T33 T35 T4 T6 T7 T9 U11 U27 V11 V28 V30 V32 V34 W1 W10 W3 W35 W4 W6 W7 W9 Y11 H11 AL24 F19 T26 AK35 AK33
RSVD
VSS_SENSE
INTEL_HASWELL_HASWELL
7 OF 9
RC237
1
2
0_0402_5%
RC238
1
2
0_0402_5%
VSSSENSE_R
<9>
PAD
T65@
+1.35V_CPU_VDDQ
@ J15
+1.35V
2
1
+1.35V_CPU_VDDQ
JUMP_43X79
+1.35V
+1.35V_CPU_VDDQ
CC287 1 2 0.1U_0402_10V6K
CC286 1 2 0.1U_0402_10V6K
CC96 1 2 0.1U_0402_10V6K
CC95 1 2 0.1U_0402_10V6K
UC3
8 7 6 5
1 2 3
4
AO4304L_SO8
@
AO4304L
Vgs=10V,Id=18A,
Rds<6.7m ohm
P/N: SB00000RV00
RC1487
470_0603_5%
@
QC5
2N7002KW_SOT323-3
SUSP
For Deep S3
+3VALW
RC1537
100K_0402_5%
@
RC1538
1 @ 2
<40,55,61>
SUSP
RUN_ON_CPU1.5VS3#
<46>
CPU1.5V_S3_GATE
0_0402_5%
QC156
2N7002KW_SOT323-3
+VSB
R56 need to check on SDV
RC56
100K_0402_5%
@
RUN_ON_CPU1.5VS3
QC4
2N7002KW_SOT323-3
1 RC1349 2 @
470K_0402_5%
RC1546
470K_0402_5%
@
CC97
0.01U 50V K X7R 0603
@
RUN_ON_CPU1.5VS3#
<6>

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Title
CPU (6/7) PWR

LCFC

Size Custom
Document Number **Y501 NM-A032**
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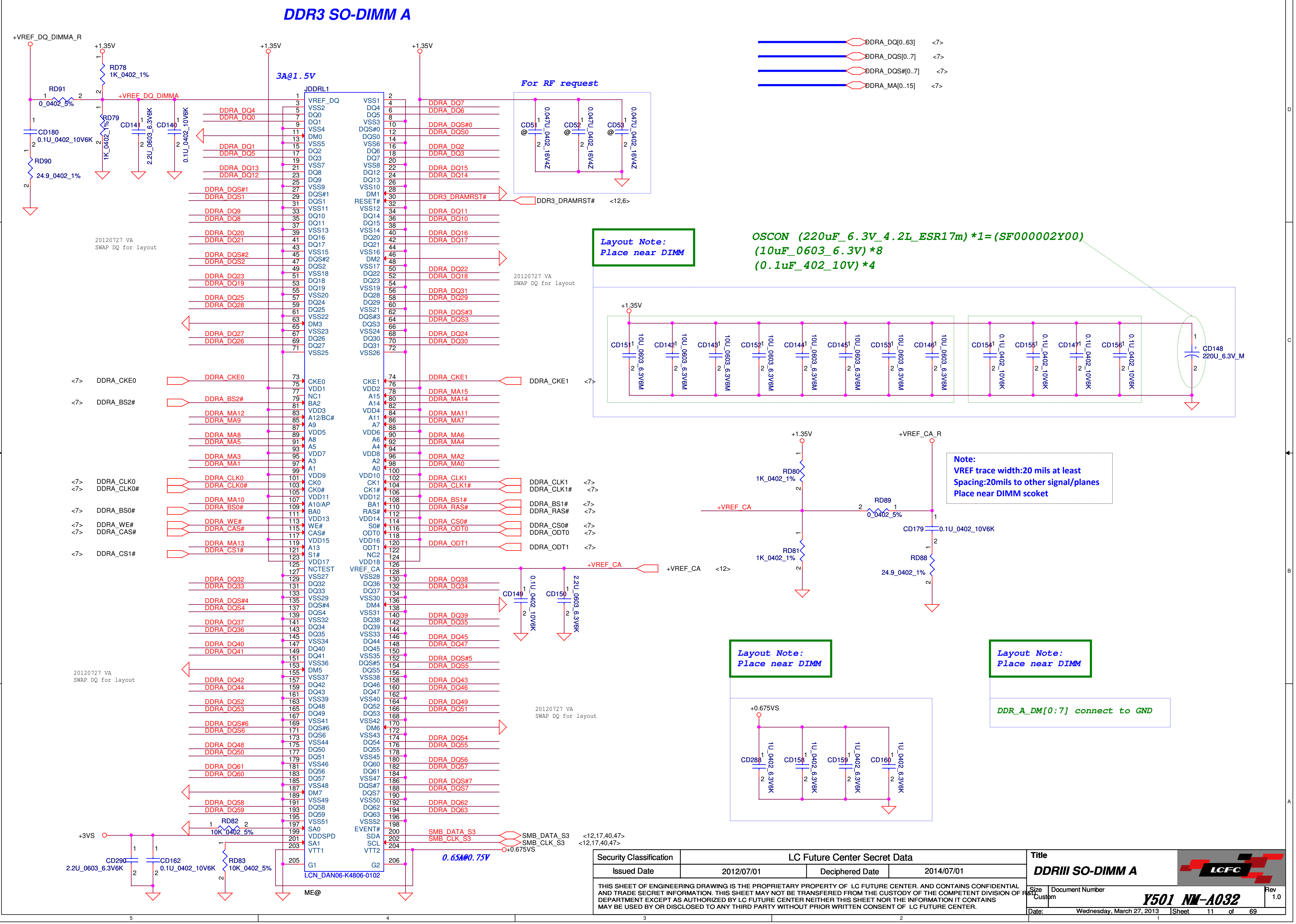
DDR3 SO-DIMM A



Layout Note:
Place near DIMM

*OSCON (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)*
*(10uF_0603_6.3V)*8*
*(0.1uF_402_10V)*4*

Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM scoket

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

DDR_A_DM[0:7] connect to GND

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Title
DDRIII SO-DIMM A

Size: Custom
Document Number: Y501 NM-A032
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Date: Wednesday, March 27, 2013
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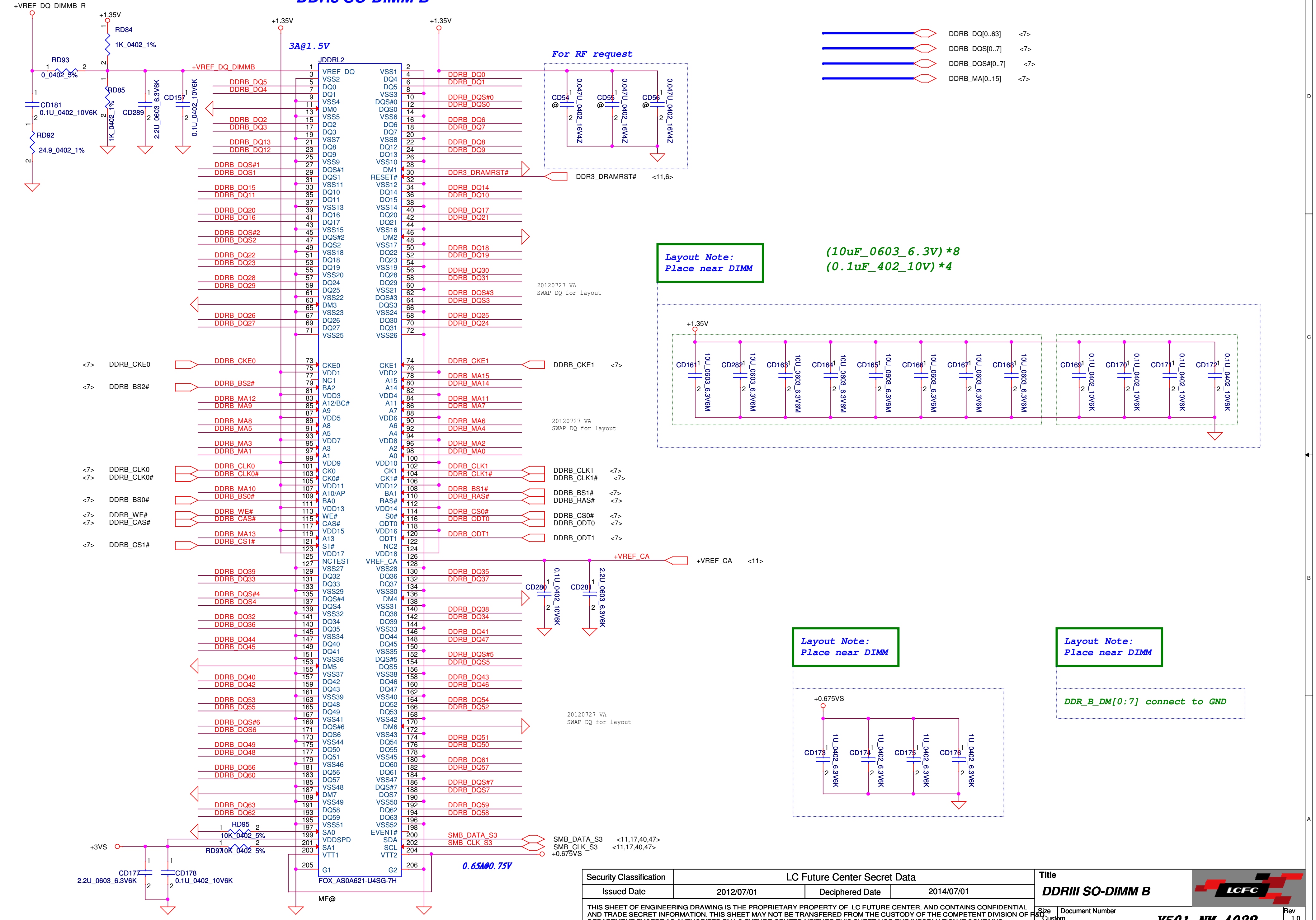
DDR3 SO-DIMM B



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
DDRIII SO-DIMM B

LCFC

Size: Custom
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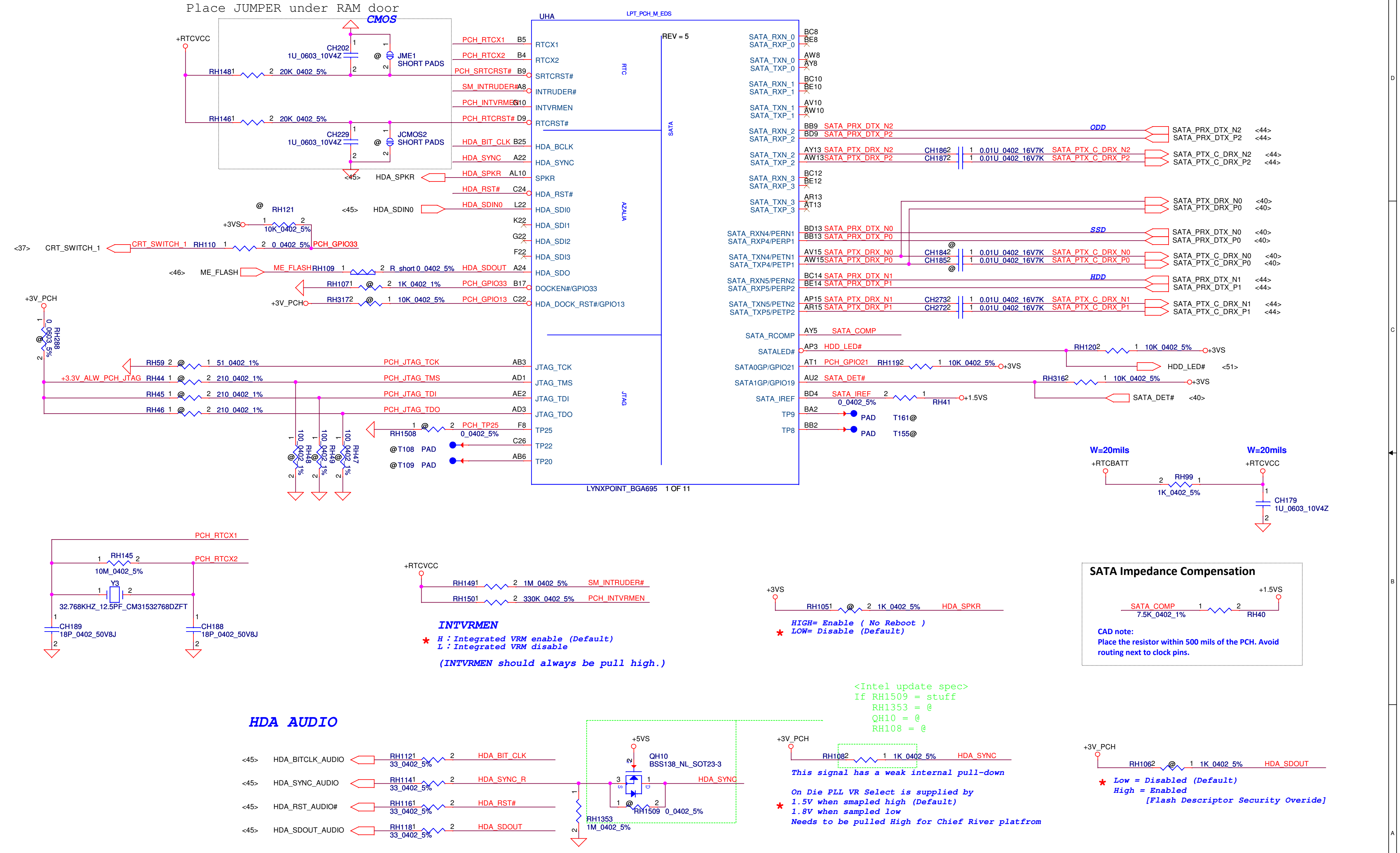
Place JUMPER under RAM door



CMOS
+RTCVCC
CH202 1U_0603_10V4Z
JME1 SHORT PADS
RH148 20K_0402_5%
RH146 20K_0402_5%
CH229 1U_0603_10V4Z
JCMOS2 SHORT PADS
UHA
LPT_PCH_M_EDS
REV = 5
PCH_RTCX1 B5 RTCX1
PCH_RTCX2 B4 RTCX2
PCH_SRTCRST# B9 SRTCRST#
SM_INTRUDER# A8 INTRUDER#
PCH_INTVRMEN C10 INTVRMEN
PCH_RTCRST# D9 RTCRST#
RTC
PCH_HDA_BIT_CLK B25 HDA_BCLK
HDA_SYNC A22 HDA_SYNC
HDA_SPKR AL10 SPKR
HDA_RST# C24 HDA_RST#
HDA_SDIN0 L22 HDA_SDI0
K22 HDA_SDI1
G22 HDA_SDI2
F22 HDA_SDI3
HDA_SDOUT A24 HDA_SDO
PCH_GPIO33 B17 DOCKEN#/GPIO33
PCH_GPIO13 C22 HDA_DOCK_RST#/GPIO13
AZALIA
<45> HDA_SPKR
<45> HDA_SDIN0
RH121
+3VS RH121 10K_0402_5%
<37> CRT_SWITCH_1 RH110 0_0402_5% PCH_GPIO33
<46> ME_FLASH RH109 R_short 0_0402_5%
RH107 1K_0402_1%
+3V_PCH RH317 10K_0402_5%
+3V_PCH
RH288 0_0603_5%
RH59 51_0402_1% PCH_JTAG_TCK AB3 JTAG_TCK
+3.3V_ALW_PCH_JTAG RH44 210_0402_1% PCH_JTAG_TMS AD1 JTAG_TMS
RH45 210_0402_1% PCH_JTAG_TDI AE2 JTAG_TDI
RH46 210_0402_1% PCH_JTAG_TDO AD3 JTAG_TDO
JTAG
RH48 100_0402_1%
RH49 100_0402_1%
RH47 100_0402_1%
RH1508 0_0402_5% PCH_TP25 F8 TP25
@T108 PAD C26 TP22
@T109 PAD AB6 TP20
LYNXPOINT_BGA695 1 OF 11
SATA
SATA_RXN_0 SATA_RXP_0 BC8 BE8
SATA_TXN_0 SATA_TXP_0 AW8 AY8
SATA_RXN_1 SATA_RXP_1 BC10 BE10
SATA_TXN_1 SATA_TXP_1 AV10 AW10
SATA_RXN_2 SATA_RXP_2 BB9 BD9 SATA_PRX_DTX_N2 SATA_PRX_DTX_P2
ODD
SATA_PRX_DTX_N2 <44>
SATA_PRX_DTX_P2 <44>
SATA_TXN_2 SATA_TXP_2 AY13 AW13 SATA_PTX_DRX_N2 SATA_PTX_DRX_P2
CH186 CH187 0.01U_0402_16V7K
SATA_PTX_C_DRX_N2 <44>
SATA_PTX_C_DRX_P2 <44>
SATA_RXN_3 SATA_RXP_3 BC12 BE12
SATA_TXN_3 SATA_TXP_3 AR13 AT13
SATA_PTX_DRX_N0 <40>
SATA_PTX_DRX_P0 <40>
SATA_RXN4/PERN1 SATA_RXP4/PERP1 BD13 BB13 SATA_PRX_DTX_N0 SATA_PRX_DTX_P0
SSD
SATA_PRX_DTX_N0 <40>
SATA_PRX_DTX_P0 <40>
SATA_TXN4/PETN1 SATA_TXP4/PETP1 AV15 AW15 SATA_PTX_DRX_N0 SATA_PTX_DRX_P0
CH184 CH185 0.01U_0402_16V7K
SATA_PTX_C_DRX_N0 <40>
SATA_PTX_C_DRX_P0 <40>
SATA_RXN5/PERN2 SATA_RXP5/PERP2 BC14 BE14 SATA_PRX_DTX_N1 SATA_PRX_DTX_P1
HDD
SATA_PRX_DTX_N1 <44>
SATA_PRX_DTX_P1 <44>
SATA_TXN5/PETN2 SATA_TXP5/PETP2 AP15 AR15 SATA_PTX_DRX_N1 SATA_PTX_DRX_P1
CH273 CH272 0.01U_0402_16V7K
SATA_PTX_C_DRX_N1 <44>
SATA_PTX_C_DRX_P1 <44>
SATA_RCOMP AY5 SATA_COMP
SATALED# AP3 HDD_LED#
RH120 10K_0402_5% +3VS
HDD_LED# <51>
SATA0GP/GPIO21 AT1 PCH_GPIO21 RH119 10K_0402_5% +3VS
SATA1GP/GPIO19 AU2 SATA_DET# RH316 10K_0402_5% +3VS
SATA_DET# <40>
SATA_IREF BD4 SATA_IREF 0_0402_5% RH41 +1.5VS
TP9 BA2 PAD T161@
TP8 BB2 PAD T155@
W=20mils
+RTCBATT
RH99 1K_0402_5%
W=20mils
+RTCVCC
CH179 1U_0603_10V4Z
PCH_RTCX1
RH145 10M_0402_5%
PCH_RTCX2
Y3
32.768KHZ_12.5PF_CM31532768DZFT
CH189 18P_0402_50V8J
CH188 18P_0402_50V8J
+RTCVCC
RH149 1M_0402_5% SM_INTRUDER#
RH150 330K_0402_5% PCH_INTVRMEN
+3VS
RH105 1K_0402_5% HDA_SPKR
+1.5VS
SATA_COMP 7.5K_0402_1% RH40
<45> HDA_BITCLK_AUDIO RH112 33_0402_5% HDA_BIT_CLK
<45> HDA_SYNC_AUDIO RH114 33_0402_5% HDA_SYNC_R
<45> HDA_RST_AUDIO# RH116 33_0402_5% HDA_RST#
<45> HDA_SDOUT_AUDIO RH118 33_0402_5% HDA_SDOUT
+5VS
QH10 BSS138_NL_SOT23-3
HDA_SYNC
RH1509 0_0402_5%
RH1353 1M_0402_5%
+3V_PCH
RH108 1K_0402_5% HDA_SYNC
+3V_PCH
RH106 1K_0402_5% HDA_SDOUT

INTVRMEN

* H : Integrated VRM enable (Default)
L : Integrated VRM disable

(INTVRMEN should always be pull high.)

* HIGH= Enable (No Reboot)
LOW= Disable (Default)

SATA Impedance Compensation

CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

<Intel update spec>
If RH1509 = stuff
RH1353 = @
QH10 = @
RH108 = @

HDA AUDIO

This signal has a weak internal pull-down

* On Die PLL VR Select is supplied by
1.5V when smapled high (Default)
1.8V when sampled low
Needs to be pulled High for Chief River platfrom

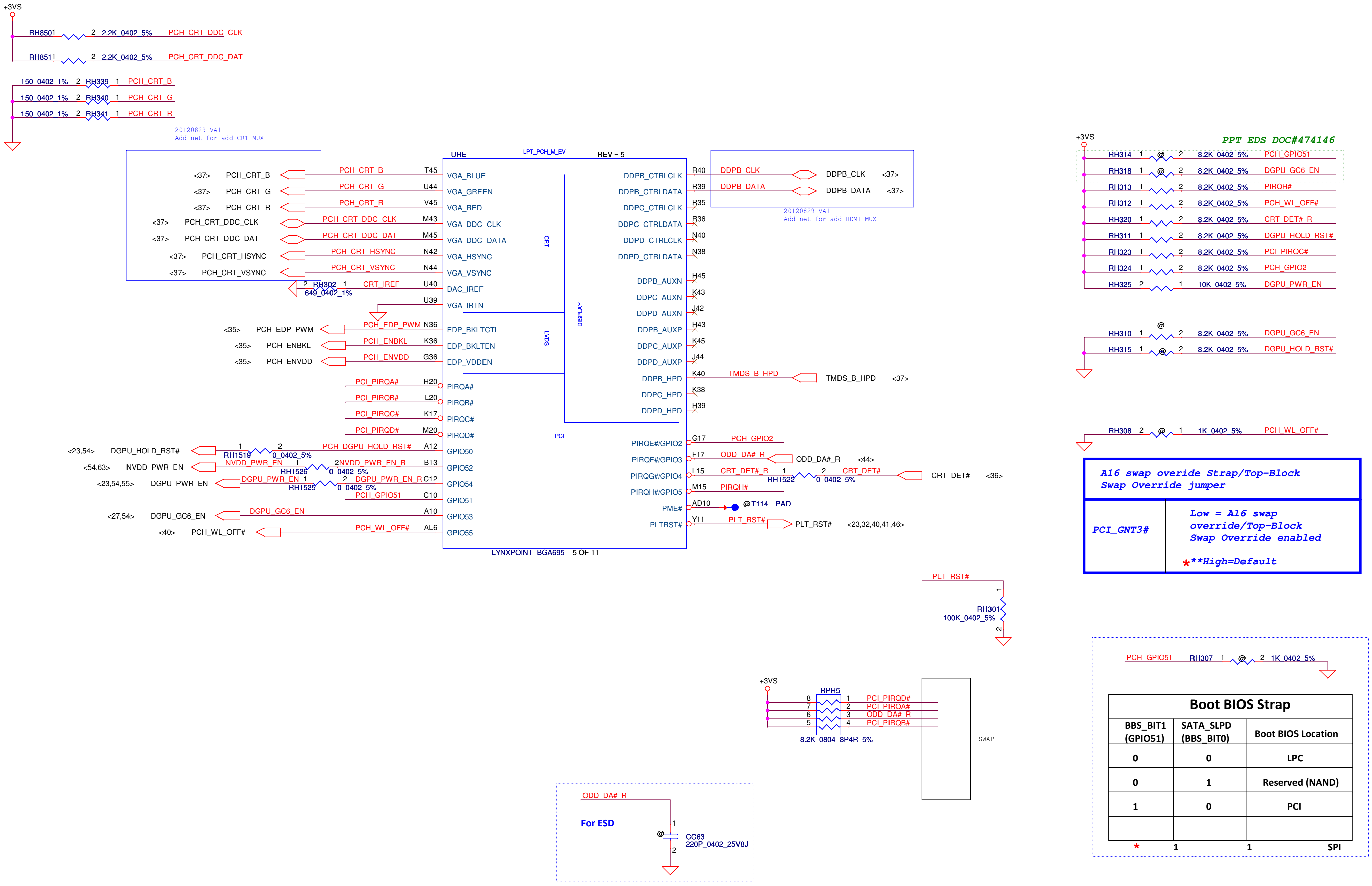
* Low = Disabled (Default)
High = Enabled
[Flash Descriptor Security Overide]

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
PCH (1/9) SATA,HDA,SPI, LPC

LCFC

Size: Custom
Document Number: Y501 NM-A032
Rev: 1.0
Date: Wednesday, March 27, 2013


+3VS
RH8501 2 2.2K_0402_5% PCH_CRT_DDC_CLK
RH8511 2 2.2K_0402_5% PCH_CRT_DDC_DAT
150_0402_1% 2 RH339 1 PCH_CRT_B
150_0402_1% 2 RH340 1 PCH_CRT_G
150_0402_1% 2 RH341 1 PCH_CRT_R
20120829 VA1
Add net for add CRT MUX
UHE
LPT_PCH_M_EV
REV = 5
<37> PCH_CRT_B
<37> PCH_CRT_G
<37> PCH_CRT_R
<37> PCH_CRT_DDC_CLK
<37> PCH_CRT_DDC_DAT
<37> PCH_CRT_HSYNC
<37> PCH_CRT_VSYNC
PCH_CRT_B T45 VGA_BLUE
PCH_CRT_G U44 VGA_GREEN
PCH_CRT_R V45 VGA_RED
PCH_CRT_DDC_CLK M43 VGA_DDC_CLK
PCH_CRT_DDC_DAT M45 VGA_DDC_DATA
PCH_CRT_HSYNC N42 VGA_HSYNC
PCH_CRT_VSYNC N44 VGA_VSYNC
2 RH302 1 CRT_IREF U40 DAC_IREF
649_0402_1%
U39 VGA_IRTN
CRT
<35> PCH_EDP_PWM PCH_EDP_PWM N36 EDP_BKLTCTL
<35> PCH_ENBKL PCH_ENBKL K36 EDP_BKLTEN
<35> PCH_ENVDD PCH_ENVDD G36 EDP_VDDEN
LVDS
DISPLAY
PCI_PIRQA# H20 PIRQA#
PCI_PIRQB# L20 PIRQB#
PCI_PIRQC# K17 PIRQC#
PCI_PIRQD# M20 PIRQD#
PCI
<23,54> DGPU_HOLD_RST# 1 RH1519 2 0_0402_5% PCH_DGPU_HOLD_RST# A12 GPIO50
<54,63> NVDD_PWR_EN NVDD_PWR_EN 1 RH1526 2 NVDD_PWR_EN_R 0_0402_5% B13 GPIO52
<23,54,55> DGPU_PWR_EN DGPU_PWR_EN 1 RH1525 2 DGPU_PWR_EN_R 0_0402_5% C12 GPIO54
PCH_GPIO51 C10 GPIO51
<27,54> DGPU_GC6_EN DGPU_GC6_EN A10 GPIO53
<40> PCH_WL_OFF# PCH_WL_OFF# AL6 GPIO55
LYNXPOINT_BGA695 5 OF 11
DDPB_CTRLCLK R40 DDPB_CLK DDPB_CLK <37>
DDPB_CTRLDATA R39 DDPB_DATA DDPB_DATA <37>
DDPC_CTRLCLK R35
DDPC_CTRLDATA R36
DDPD_CTRLCLK N40
DDPD_CTRLDATA N38
20120829 VA1
Add net for add HDMI MUX
DDPB_AUXN H45
DDPC_AUXN K43
DDPD_AUXN J42
DDPB_AUXP H43
DDPC_AUXP K45
DDPD_AUXP J44
DDPB_HPD K40 TMDS_B_HPD TMDS_B_HPD <37>
DDPC_HPD K38
DDPD_HPD H39
PIRQE#/GPIO2 G17 PCH_GPIO2
PIRQF#/GPIO3 F17 ODD_DA#_R ODD_DA#_R <44>
PIRQG#/GPIO4 L15 CRT_DET#_R 1 RH1522 2 0_0402_5% CRT_DET# CRT_DET# <36>
PIRQH#/GPIO5 M15 PIRQH#
PME# AD10 @T114 PAD
PLTRST# Y11 PLT_RST# PLT_RST# <23,32,40,41,46>
+3VS
PPT EDS DOC#474146
RH314 1 @ 2 8.2K_0402_5% PCH_GPIO51
RH318 1 @ 2 8.2K_0402_5% DGPU_GC6_EN
RH313 1 2 8.2K_0402_5% PIRQH#
RH312 1 2 8.2K_0402_5% PCH_WL_OFF#
RH320 1 2 8.2K_0402_5% CRT_DET#_R
RH311 1 2 8.2K_0402_5% DGPU_HOLD_RST#
RH323 1 2 8.2K_0402_5% PCI_PIRQC#
RH324 1 2 8.2K_0402_5% PCH_GPIO2
RH325 2 1 10K_0402_5% DGPU_PWR_EN
RH310 1 @ 2 8.2K_0402_5% DGPU_GC6_EN
RH315 1 @ 2 8.2K_0402_5% DGPU_HOLD_RST#
RH308 2 @ 1 1K_0402_5% PCH_WL_OFF#
PLT_RST#
1 RH301 100K_0402_5% 2
+3VS
RPH5
8 1 PCI_PIRQD#
7 2 PCI_PIRQA#
6 3 ODD_DA#_R
5 4 PCI_PIRQB#
8.2K_0804_8P4R_5%
SWAP
ODD_DA#_R
For ESD
1 @ CC63 220P_0402_25V8J 2
PCH_GPIO51 RH307 1 @ 2 1K_0402_5%

A16 swap overide Strap/Top-Block
Swap Override jumper

PCI_GNT3#	***Low = A16 swap override/Top-Block Swap Override enabled*** ★*****High=Default***

Boot BIOS Strap

BBS_BIT1 (GPIO51)	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
★ 1	1	SPI

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Title
PCH (2/9) PCIE, SMBUS, CLK
LCFC
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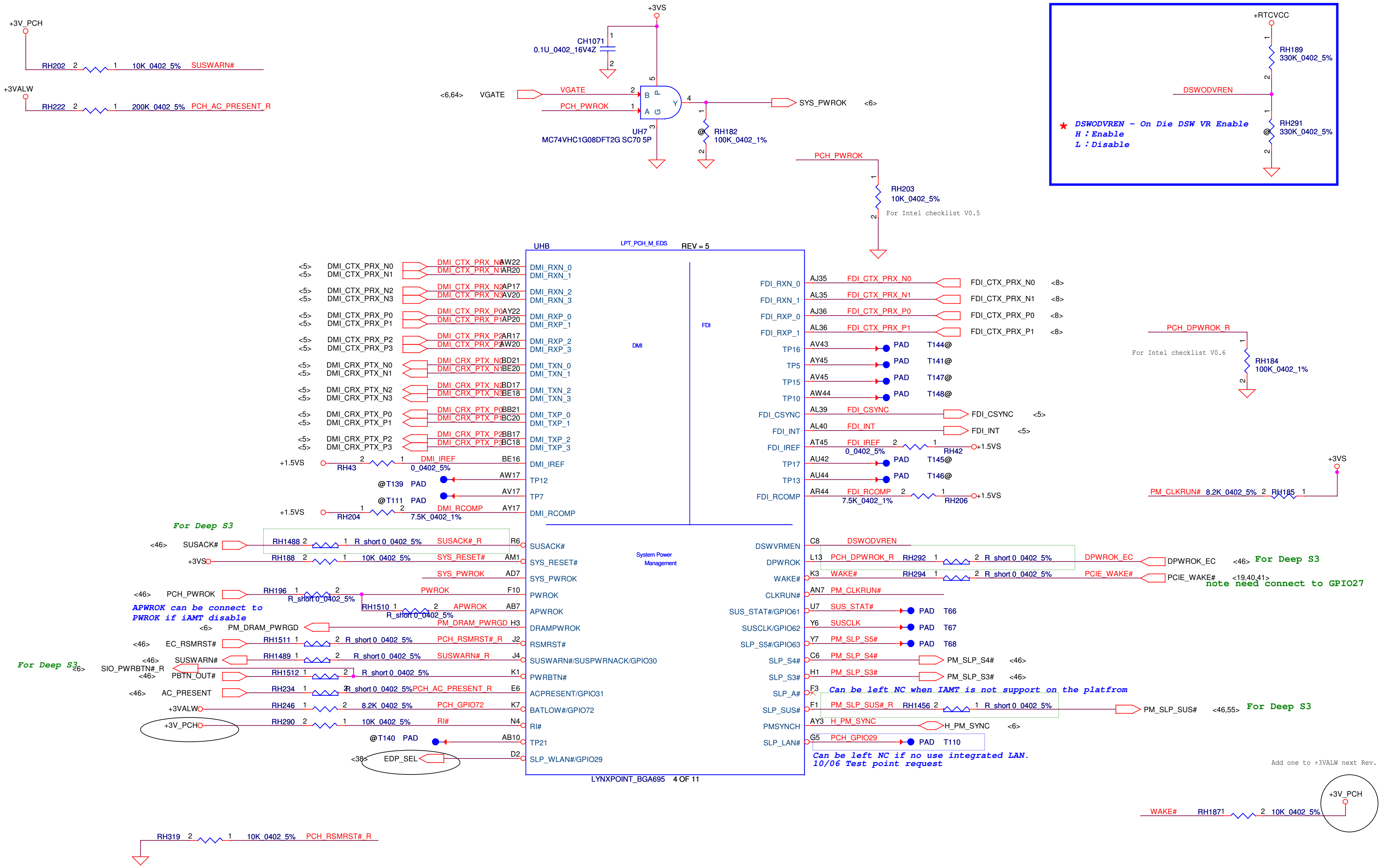
Date: Wednesday, March 27, 2013


+3V_PCH
RH202 2 1 10K_0402_5% SUSWARN#
+3VALW
RH222 2 1 200K_0402_5% PCH_AC_PRESENT_R
+3VS
CH1071 0.1U_0402_16V4Z
<6,64> VGATE
VGATE
PCH_PWROK
UH7 MC74VHC1G08DFT2G SC70 5P
SYS_PWROK <6>
@ RH182 100K_0402_1%
PCH_PWROK
RH203 10K_0402_5%
For Intel checklist V0.5
+RTCVCC
RH189 330K_0402_5%
DSWODVREN
@ RH291 330K_0402_5%
★ DSWODVREN - On Die DSW VR Enable
H : Enable
L : Disable
UHB LPT_PCH_M_EDS REV = 5
DMI
FDI
System Power Management
<5> DMI_CTX_PRX_N0 AW22 DMI_RXN_0
<5> DMI_CTX_PRX_N1 AR20 DMI_RXN_1
<5> DMI_CTX_PRX_N2 AP17 DMI_RXN_2
<5> DMI_CTX_PRX_N3 AV20 DMI_RXN_3
<5> DMI_CTX_PRX_P0 AY22 DMI_RXP_0
<5> DMI_CTX_PRX_P1 AP20 DMI_RXP_1
<5> DMI_CTX_PRX_P2 AR17 DMI_RXP_2
<5> DMI_CTX_PRX_P3 AW20 DMI_RXP_3
<5> DMI_CRX_PTX_N0 BD21 DMI_TXN_0
<5> DMI_CRX_PTX_N1 BE20 DMI_TXN_1
<5> DMI_CRX_PTX_N2 BD17 DMI_TXN_2
<5> DMI_CRX_PTX_N3 BE18 DMI_TXN_3
<5> DMI_CRX_PTX_P0 BB21 DMI_TXP_0
<5> DMI_CRX_PTX_P1 BC20 DMI_TXP_1
<5> DMI_CRX_PTX_P2 BB17 DMI_TXP_2
<5> DMI_CRX_PTX_P3 BC18 DMI_TXP_3
+1.5VS RH43 0_0402_5% DMI_IREF BE16 DMI_IREF
@T139 PAD AW17 TP12
@T111 PAD AV17 TP7
+1.5VS RH204 7.5K_0402_1% DMI_RCOMP AY17 DMI_RCOMP
FDI_RXN_0 AJ35 FDI_CTX_PRX_N0 FDI_CTX_PRX_N0 <8>
FDI_RXN_1 AL35 FDI_CTX_PRX_N1 FDI_CTX_PRX_N1 <8>
FDI_RXP_0 AJ36 FDI_CTX_PRX_P0 FDI_CTX_PRX_P0 <8>
FDI_RXP_1 AL36 FDI_CTX_PRX_P1 FDI_CTX_PRX_P1 <8>
TP16 AV43 PAD T144@
TP5 AY45 PAD T141@
TP15 AV45 PAD T147@
TP10 AW44 PAD T148@
FDI_CSYNC AL39 FDI_CSYNC FDI_CSYNC <5>
FDI_INT AL40 FDI_INT FDI_INT <5>
FDI_IREF AT45 FDI_IREF 0_0402_5% RH42 +1.5VS
TP17 AU42 PAD T145@
TP13 AU44 PAD T146@
FDI_RCOMP AR44 FDI_RCOMP 7.5K_0402_1% RH206 +1.5VS
PCH_DPWROK_R
For Intel checklist V0.6
RH184 100K_0402_1%
+3VS
PM_CLKRUN# 8.2K_0402_5% RH185
For Deep S3
<46> SUSACK# RH1488 R_short 0_0402_5% SUSACK#_R R6 SUSACK#
+3VS RH188 10K_0402_5% SYS_RESET# AM1 SYS_RESET#
SYS_PWROK AD7 SYS_PWROK
<46> PCH_PWROK RH196 R_short 0_0402_5% PWROK F10 PWROK
RH1510 R_short 0_0402_5% APWROK AB7 APWROK
APWROK can be connect to PWROK if iAMT disable
<6> PM_DRAM_PWRGD PM_DRAM_PWRGD H3 DRAMPWROK
<46> EC_RSMRST# RH1511 R_short 0_0402_5% PCH_RSMRST#_R J2 RSMRST#
<46> SUSWARN# RH1489 R_short 0_0402_5% SUSWARN#_R J4 SUSWARN#/SUSPWRNACK/GPIO30
For Deep S3 <6> SIO_PWRBTN#_R
<46> PBTN_OUT# RH1512 R_short 0_0402_5% K1 PWRBTN#
<46> AC_PRESENT RH234 R_short 0_0402_5% PCH_AC_PRESENT_R E6 ACPRESENT/GPIO31
+3VALW RH246 8.2K_0402_5% PCH_GPIO72 K7 BATLOW#/GPIO72
+3V_PCH RH290 10K_0402_5% RI# N4 RI#
@T140 PAD AB10 TP21
<38> EDP_SEL D2 SLP_WLAN#/GPIO29
DSWVRMEN C8 DSWODVREN
DPWROK L13 PCH_DPWROK_R RH292 R_short 0_0402_5% DPWROK_EC DPWROK_EC <46> For Deep S3
WAKE# K3 WAKE# RH294 R_short 0_0402_5% PCIE_WAKE# PCIE_WAKE# <19,40,41>
note need connect to GPIO27
CLKRUN# AN7 PM_CLKRUN#
SUS_STAT#/GPIO61 U7 SUS_STAT# PAD T66
SUSCLK/GPIO62 Y6 SUSCLK PAD T67
SLP_S5#/GPIO63 Y7 PM_SLP_S5# PAD T68
SLP_S4# C6 PM_SLP_S4# PM_SLP_S4# <46>
SLP_S3# H1 PM_SLP_S3# PM_SLP_S3# <46>
SLP_A# F3 Can be left NC when IAMT is not support on the platfrom
SLP_SUS# F1 PM_SLP_SUS#_R RH1456 R_short 0_0402_5% PM_SLP_SUS# <46,55> For Deep S3
PMSYNCH AY3 H_PM_SYNC H_PM_SYNC <6>
SLP_LAN# G5 PCH_GPIO29 PAD T110
Can be left NC if no use integrated LAN.
10/06 Test point request
LYNXPOINT_BGA695 4 OF 11
Add one to +3VALW next Rev.
+3V_PCH
WAKE# RH1871 10K_0402_5%
RH319 10K_0402_5% PCH_RSMRST#_R

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PCH (3/9) PCIE, SMBUS, CLK

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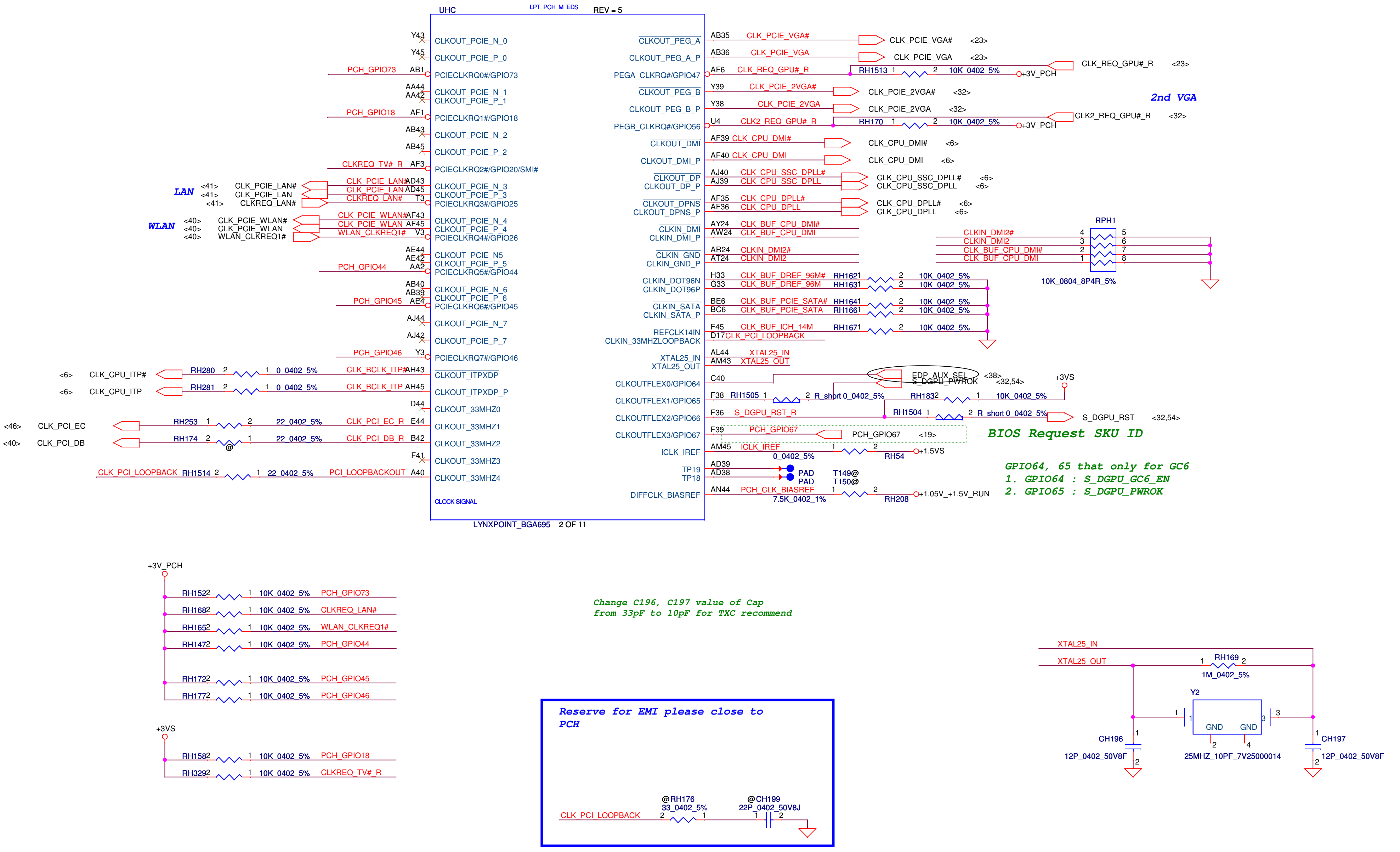
UHC
LPT_PCH_M_EDS
REV = 5
Y43 CLKOUT_PCIE_N_0
Y45 CLKOUT_PCIE_P_0
PCH_GPIO73 AB1 PCIECLKRQ0#/GPIO73
AA44 CLKOUT_PCIE_N_1
AA42 CLKOUT_PCIE_P_1
PCH_GPIO18 AF1 PCIECLKRQ1#/GPIO18
AB43 CLKOUT_PCIE_N_2
AB45 CLKOUT_PCIE_P_2
CLKREQ_TV#_R AF3 PCIECLKRQ2#/GPIO20/SMI#
LAN
<41> CLK_PCIE_LAN# CLK_PCIE_LAN# AD43 CLKOUT_PCIE_N_3
<41> CLK_PCIE_LAN CLK_PCIE_LAN AD45 CLKOUT_PCIE_P_3
<41> CLKREQ_LAN# CLKREQ_LAN# T3 PCIECLKRQ3#/GPIO25
WLAN
<40> CLK_PCIE_WLAN# CLK_PCIE_WLAN# AF43 CLKOUT_PCIE_N_4
<40> CLK_PCIE_WLAN CLK_PCIE_WLAN AF45 CLKOUT_PCIE_P_4
<40> WLAN_CLKREQ1# WLAN_CLKREQ1# V3 PCIECLKRQ4#/GPIO26
AE44 CLKOUT_PCIE_N5
AE42 CLKOUT_PCIE_P_5
PCH_GPIO44 AA2 PCIECLKRQ5#/GPIO44
AB40 CLKOUT_PCIE_N_6
AB39 CLKOUT_PCIE_P_6
PCH_GPIO45 AE4 PCIECLKRQ6#/GPIO45
AJ44 CLKOUT_PCIE_N_7
AJ42 CLKOUT_PCIE_P_7
PCH_GPIO46 Y3 PCIECLKRQ7#/GPIO46
<6> CLK_CPU_ITP# RH280 2 1 0_0402_5% CLK_BCLK_ITP# AH43 CLKOUT_ITPXDP
<6> CLK_CPU_ITP RH281 2 1 0_0402_5% CLK_BCLK_ITP AH45 CLKOUT_ITPXDP_P
D44 CLKOUT_33MHZ0
<46> CLK_PCI_EC RH253 1 2 22_0402_5% CLK_PCI_EC_R E44 CLKOUT_33MHZ1
<40> CLK_PCI_DB RH174 2 1 22_0402_5% CLK_PCI_DB_R B42 CLKOUT_33MHZ2
@
F41 CLKOUT_33MHZ3
CLK_PCI_LOOPBACK RH1514 2 1 22_0402_5% PCI_LOOPBACKOUT A40 CLKOUT_33MHZ4
CLOCK SIGNAL
LYNXPOINT_BGA695 2 OF 11
CLKOUT_PEG_A AB35 CLK_PCIE_VGA# CLK_PCIE_VGA# <23>
CLKOUT_PEG_A_P AB36 CLK_PCIE_VGA CLK_PCIE_VGA <23>
PEGA_CLKRQ#/GPIO47 AF6 CLK_REQ_GPU#_R RH1513 1 2 10K_0402_5% +3V_PCH CLK_REQ_GPU#_R <23>
CLKOUT_PEG_B Y39 CLK_PCIE_2VGA# CLK_PCIE_2VGA# <32>
CLKOUT_PEG_B_P Y38 CLK_PCIE_2VGA CLK_PCIE_2VGA <32>
2nd VGA
PEGB_CLKRQ#/GPIO56 U4 CLK2_REQ_GPU#_R RH170 1 2 10K_0402_5% +3V_PCH CLK2_REQ_GPU#_R <32>
CLKOUT_DMI AF39 CLK_CPU_DMI# CLK_CPU_DMI# <6>
CLKOUT_DMI_P AF40 CLK_CPU_DMI CLK_CPU_DMI <6>
CLKOUT_DP AJ40 CLK_CPU_SSC_DPLL# CLK_CPU_SSC_DPLL# <6>
CLKOUT_DP_P AJ39 CLK_CPU_SSC_DPLL CLK_CPU_SSC_DPLL <6>
CLKOUT_DPNS AF35 CLK_CPU_DPLL# CLK_CPU_DPLL# <6>
CLKOUT_DPNS_P AF36 CLK_CPU_DPLL CLK_CPU_DPLL <6>
CLKIN_DMI AY24 CLK_BUF_CPU_DMI#
CLKIN_DMI_P AW24 CLK_BUF_CPU_DMI
CLKIN_GND AR24 CLKIN_DMI2#
CLKIN_GND_P AT24 CLKIN_DMI2
RPH1
CLKIN_DMI2# 4 5
CLKIN_DMI2 3 6
CLK_BUF_CPU_DMI# 2 7
CLK_BUF_CPU_DMI 1 8
10K_0804_8P4R_5%
CLKIN_DOT96N H33 CLK_BUF_DREF_96M# RH162 1 2 10K_0402_5%
CLKIN_DOT96P G33 CLK_BUF_DREF_96M RH163 1 2 10K_0402_5%
CLKIN_SATA BE6 CLK_BUF_PCIE_SATA# RH164 1 2 10K_0402_5%
CLKIN_SATA_P BC6 CLK_BUF_PCIE_SATA RH166 1 2 10K_0402_5%
REFCLK14IN F45 CLK_BUF_ICH_14M RH167 1 2 10K_0402_5%
CLKIN_33MHZLOOPBACK D17 CLK_PCI_LOOPBACK
XTAL25_IN AL44 XTAL25_IN
XTAL25_OUT AM43 XTAL25_OUT
CLKOUTFLEX0/GPIO64 C40 EDP_AUX_SEL S_DGPU_PWROK <38> <32,54>
+3VS
CLKOUTFLEX1/GPIO65 F38 RH1505 1 2 R_short 0_0402_5% RH183 2 1 10K_0402_5%
CLKOUTFLEX2/GPIO66 F36 S_DGPU_RST_R RH1504 1 2 R_short 0_0402_5% S_DGPU_RST <32,54>
CLKOUTFLEX3/GPIO67 F39 PCH_GPIO67 PCH_GPIO67 <19>
BIOS Request SKU ID
ICLK_IREF AM45 ICLK_IREF 1 2 0_0402_5% RH54 +1.5VS
TP19 AD39 PAD T149@
TP18 AD38 PAD T150@
DIFFCLK_BIASREF AN44 PCH_CLK_BIASREF 1 2 7.5K_0402_1% RH208 +1.05V_+1.5V_RUN
GPIO64, 65 that only for GC6
1. GPIO64 : S_DGPU_GC6_EN
2. GPIO65 : S_DGPU_PWROK
+3V_PCH
RH152 2 1 10K_0402_5% PCH_GPIO73
RH168 2 1 10K_0402_5% CLKREQ_LAN#
RH165 2 1 10K_0402_5% WLAN_CLKREQ1#
RH147 2 1 10K_0402_5% PCH_GPIO44
RH172 2 1 10K_0402_5% PCH_GPIO45
RH177 2 1 10K_0402_5% PCH_GPIO46
+3VS
RH158 2 1 10K_0402_5% PCH_GPIO18
RH329 2 1 10K_0402_5% CLKREQ_TV#_R
Change C196, C197 value of Cap
from 33pF to 10pF for TXC recommend
Reserve for EMI please close to
PCH
CLK_PCI_LOOPBACK
@RH176
33_0402_5%
2 1
@CH199
22P_0402_50V8J
1 2
XTAL25_IN
XTAL25_OUT
RH169
1 2
1M_0402_5%
Y2
1 1 GND GND 3 3
2 4
25MHZ_10PF_7V25000014
CH196
1 2
12P_0402_50V8F
CH197
1 2
12P_0402_50V8F

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Title
PCH (3/9) DMI, FDI, PM

LCFC

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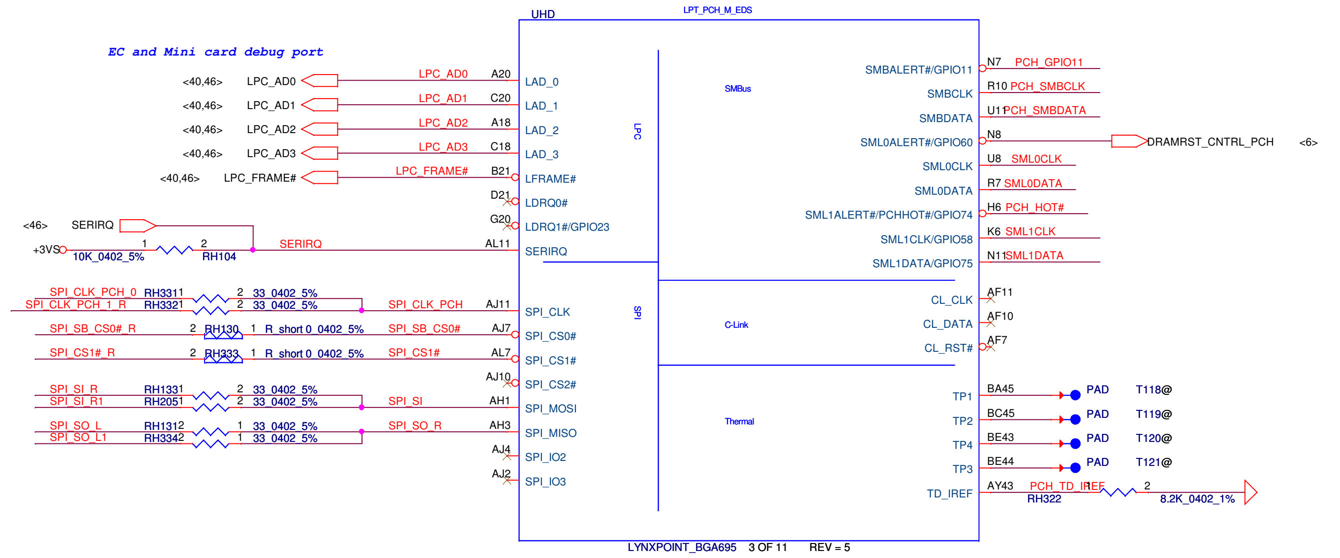
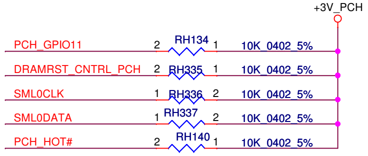
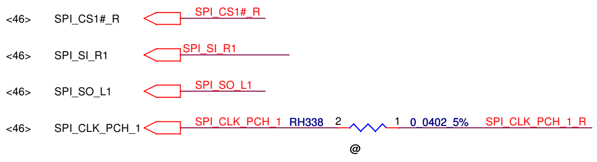
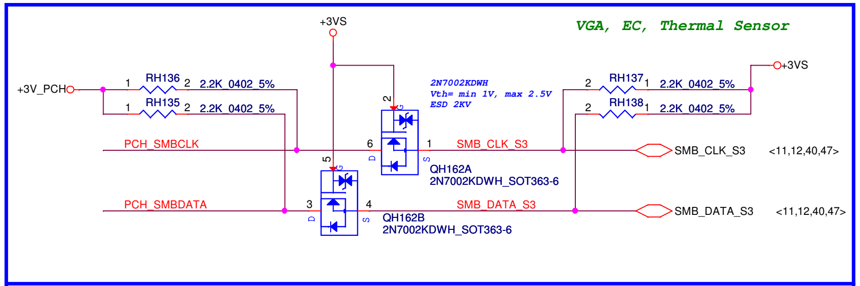
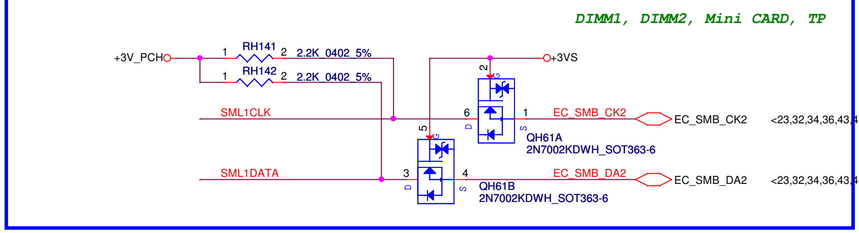
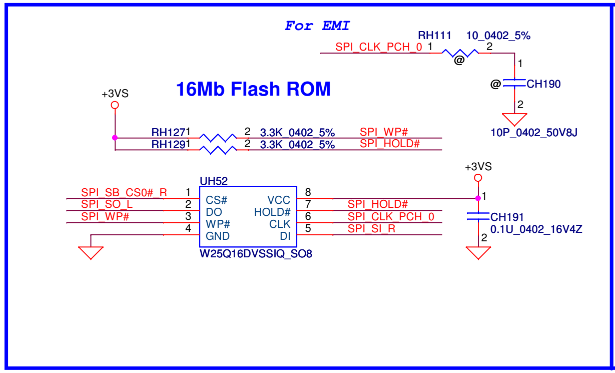

EC and Mini card debug port
UHD
LPT_PCH_M_EDS
<40,46> LPC_AD0 LPC_AD0 A20 LAD_0
<40,46> LPC_AD1 LPC_AD1 C20 LAD_1
<40,46> LPC_AD2 LPC_AD2 A18 LAD_2
<40,46> LPC_AD3 LPC_AD3 C18 LAD_3
<40,46> LPC_FRAME# LPC_FRAME# B21 LFRAME#
D21 LDRQ0#
G20 LDRQ1#/GPIO23
<46> SERIRQ
+3VS 1 2 10K_0402_5% RH104 SERIRQ AL11 SERIRQ
LPC
SPI_CLK_PCH_0 RH3311 2 33_0402_5%
SPI_CLK_PCH_1_R RH3321 2 33_0402_5% SPI_CLK_PCH AJ11 SPI_CLK
SPI_SB_CS0#_R 2 RH130 1 R_short 0_0402_5% SPI_SB_CS0# AJ7 SPI_CS0#
SPI_CS1#_R 2 RH333 1 R_short 0_0402_5% SPI_CS1# AL7 SPI_CS1#
AJ10 SPI_CS2#
SPI_SI_R RH1331 2 33_0402_5%
SPI_SI_R1 RH2051 2 33_0402_5% SPI_SI AH1 SPI_MOSI
SPI_SO_L RH1312 1 33_0402_5%
SPI_SO_L1 RH3342 1 33_0402_5% SPI_SO_R AH3 SPI_MISO
AJ4 SPI_IO2
AJ2 SPI_IO3
SPI
SMBus
C-Link
Thermal
SMBALERT#/GPIO11 N7 PCH_GPIO11
SMBCLK R10 PCH_SMBCLK
SMBDATA U11 PCH_SMBDATA
SML0ALERT#/GPIO60 N8 DRAMRST_CNTRL_PCH <6>
SML0CLK U8 SML0CLK
SML0DATA R7 SML0DATA
SML1ALERT#/PCHHOT#/GPIO74 H6 PCH_HOT#
SML1CLK/GPIO58 K6 SML1CLK
SML1DATA/GPIO75 N11 SML1DATA
CL_CLK AF11
CL_DATA AF10
CL_RST# AF7
TP1 BA45 PAD T118@
TP2 BC45 PAD T119@
TP4 BE43 PAD T120@
TP3 BE44 PAD T121@
TD_IREF AY43 PCH_TD_IREF 1 2 RH322 8.2K_0402_1%
LYNXPOINT_BGA695 3 OF 11 REV = 5

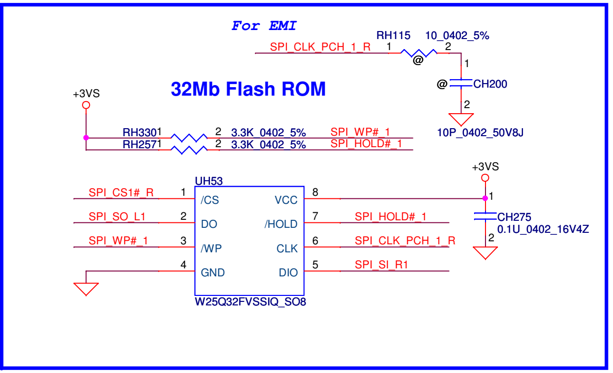

+3V_PCH
PCH_GPIO11 2 RH134 1 10K_0402_5%
DRAMRST_CNTRL_PCH 2 RH335 1 10K_0402_5%
SML0CLK 1 RH336 2 10K_0402_5%
SML0DATA 1 RH337 2 10K_0402_5%
PCH_HOT# 2 RH140 1 10K_0402_5%


<46> SPI_CS1#_R SPI_CS1#_R
<46> SPI_SI_R1 SPI_SI_R1
<46> SPI_SO_L1 SPI_SO_L1
<46> SPI_CLK_PCH_1 SPI_CLK_PCH_1 RH338 2 1 0_0402_5% SPI_CLK_PCH_1_R
@




DIMM1, DIMM2, Mini CARD, TP
+3V_PCH 1 RH141 2 2.2K_0402_5%
1 RH142 2 2.2K_0402_5%
+3VS
SML1CLK 6 1 EC_SMB_CK2 EC_SMB_CK2 <23,32,34,36,43,46>
QH61A 2N7002KDWH_SOT363-6
SML1DATA 3 4 EC_SMB_DA2 EC_SMB_DA2 <23,32,34,36,43,46>
QH61B 2N7002KDWH_SOT363-6


For EMI
RH111 10_0402_5%
SPI_CLK_PCH_0 1 2 @
CH190 @ 10P_0402_50V8J
16Mb Flash ROM
+3VS
RH1271 2 3.3K_0402_5% SPI_WP#
RH1291 2 3.3K_0402_5% SPI_HOLD#
+3VS
UH52
SPI_SB_CS0#_R 1 CS# VCC 8
SPI_SO_L 2 DO HOLD# 7 SPI_HOLD#
SPI_WP# 3 WP# CLK 6 SPI_CLK_PCH_0
4 GND DI 5 SPI_SI_R
W25Q16DVSSIQ_SO8
CH191 0.1U_0402_16V4Z



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Title
PCH (4/9) LVDS, CRT,DP,HDMI

LCFC

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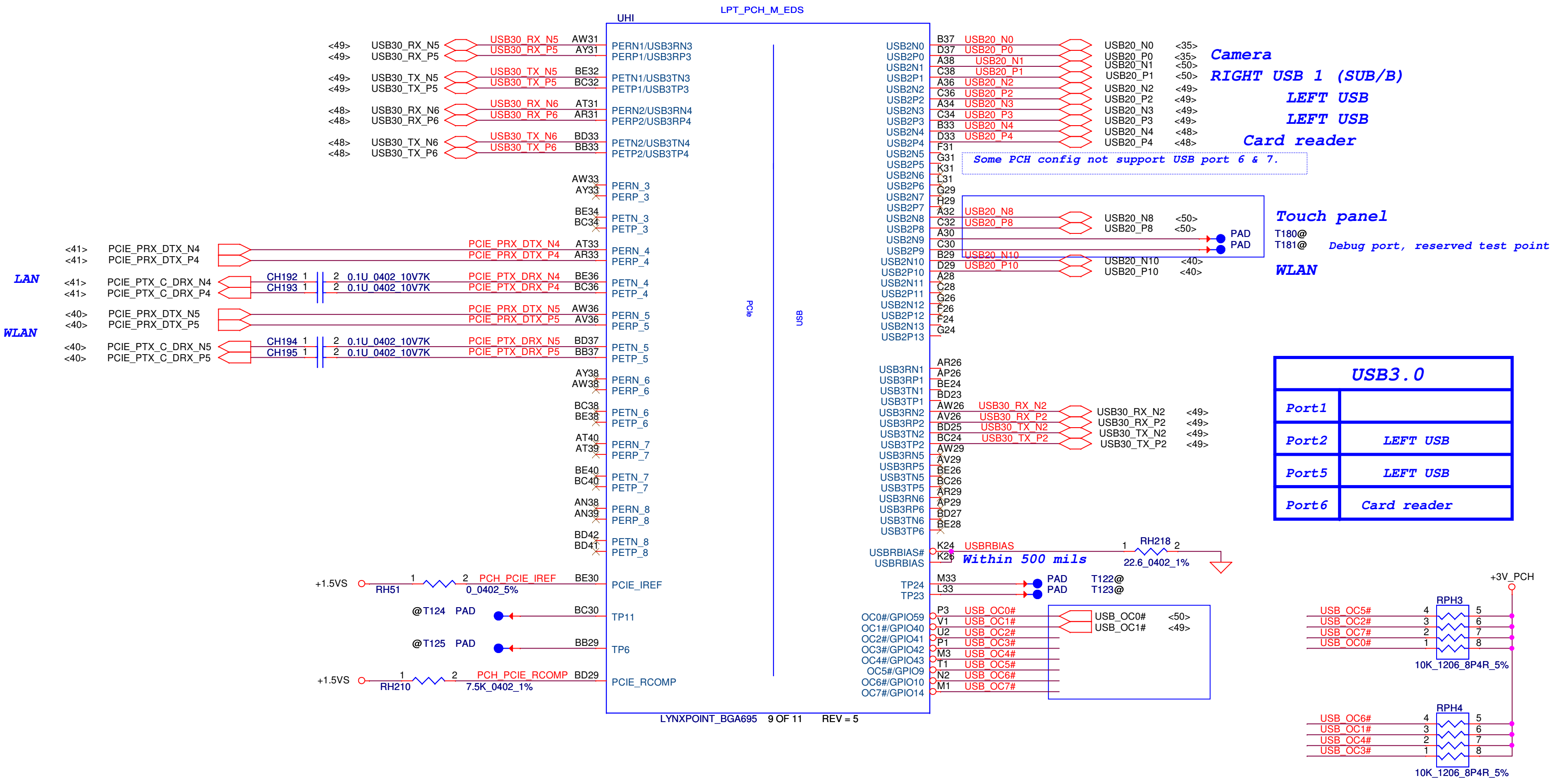

LPT_PCH_M_EDS
UHI
USB30_RX_N5 AW31 PERN1/USB3RN3
USB30_RX_P5 AY31 PERP1/USB3RP3
USB30_TX_N5 BE32 PETN1/USB3TN3
USB30_TX_P5 BC32 PETP1/USB3TP3
USB30_RX_N6 AT31 PERN2/USB3RN4
USB30_RX_P6 AR31 PERP2/USB3RP4
USB30_TX_N6 BD33 PETN2/USB3TN4
USB30_TX_P6 BB33 PETP2/USB3TP4
<49> USB30_RX_N5
<49> USB30_RX_P5
<49> USB30_TX_N5
<49> USB30_TX_P5
<48> USB30_RX_N6
<48> USB30_RX_P6
<48> USB30_TX_N6
<48> USB30_TX_P6
AW33 PERN_3
AY33 PERP_3
BE34 PETN_3
BC34 PETP_3
<41> PCIE_PRX_DTX_N4 AT33 PERN_4
<41> PCIE_PRX_DTX_P4 AR33 PERP_4
LAN
<41> PCIE_PTX_C_DRX_N4 CH192 0.1U_0402_10V7K PCIE_PTX_DRX_N4 BE36 PETN_4
<41> PCIE_PTX_C_DRX_P4 CH193 0.1U_0402_10V7K PCIE_PTX_DRX_P4 BC36 PETP_4
<40> PCIE_PRX_DTX_N5 AW36 PERN_5
<40> PCIE_PRX_DTX_P5 AV36 PERP_5
WLAN
<40> PCIE_PTX_C_DRX_N5 CH194 0.1U_0402_10V7K PCIE_PTX_DRX_N5 BD37 PETN_5
<40> PCIE_PTX_C_DRX_P5 CH195 0.1U_0402_10V7K PCIE_PTX_DRX_P5 BB37 PETP_5
AY38 PERN_6
AW38 PERP_6
BC38 PETN_6
BE38 PETP_6
AT40 PERN_7
AT39 PERP_7
BE40 PETN_7
BC40 PETP_7
AN38 PERN_8
AN39 PERP_8
BD42 PETN_8
BD41 PETP_8
+1.5VS RH51 0_0402_5% PCH_PCIE_IREF BE30 PCIE_IREF
@T124 PAD BC30 TP11
@T125 PAD BB29 TP6
+1.5VS RH210 7.5K_0402_1% PCH_PCIE_RCOMP BD29 PCIE_RCOMP
PCIe
USB
USB2N0 B37 USB20_N0 USB20_N0 <35>
USB2P0 D37 USB20_P0 USB20_P0 <35>
Camera
USB2N1 A38 USB20_N1 USB20_N1 <50>
USB2P1 C38 USB20_P1 USB20_P1 <50>
RIGHT USB 1 (SUB/B)
USB2N2 A36 USB20_N2 USB20_N2 <49>
USB2P2 C36 USB20_P2 USB20_P2 <49>
LEFT USB
USB2N3 A34 USB20_N3 USB20_N3 <49>
USB2P3 C34 USB20_P3 USB20_P3 <49>
LEFT USB
USB2N4 B33 USB20_N4 USB20_N4 <48>
USB2P4 D33 USB20_P4 USB20_P4 <48>
Card reader
USB2N5 F31
USB2P5 G31
USB2N6 K31
USB2P6 L31
USB2N7 G29
USB2P7 H29
Some PCH config not support USB port 6 & 7.
USB2N8 A32 USB20_N8 USB20_N8 <50>
USB2P8 C32 USB20_P8 USB20_P8 <50>
Touch panel
USB2N9 A30 PAD T180@
USB2P9 C30 PAD T181@
Debug port, reserved test point
USB2N10 B29 USB20_N10 USB20_N10 <40>
USB2P10 D29 USB20_P10 USB20_P10 <40>
WLAN
USB2N11 A28
USB2P11 C28
USB2N12 G26
USB2P12 F26
USB2N13 F24
USB2P13 G24
USB3RN1 AR26
USB3RP1 AP26
USB3TN1 BE24
USB3TP1 BD23
USB3RN2 AW26 USB30_RX_N2 USB30_RX_N2 <49>
USB3RP2 AV26 USB30_RX_P2 USB30_RX_P2 <49>
USB3TN2 BD25 USB30_TX_N2 USB30_TX_N2 <49>
USB3TP2 BC24 USB30_TX_P2 USB30_TX_P2 <49>
USB3RN5 AW29
USB3RP5 AV29
USB3TN5 BE26
USB3TP5 BC26
USB3RN6 AR29
USB3RP6 AP29
USB3TN6 BD27
USB3TP6 BE28
USBRBIAS# K24 USBRBIAS RH218 22.6_0402_1%
USBRBIAS K26
Within 500 mils
TP24 M33 PAD T122@
TP23 L33 PAD T123@
OC0#/GPIO59 P3 USB_OC0# USB_OC0# <50>
OC1#/GPIO40 V1 USB_OC1# USB_OC1# <49>
OC2#/GPIO41 U2 USB_OC2#
OC3#/GPIO42 P1 USB_OC3#
OC4#/GPIO43 M3 USB_OC4#
OC5#/GPIO9 T1 USB_OC5#
OC6#/GPIO10 N2 USB_OC6#
OC7#/GPIO14 M1 USB_OC7#
LYNXPOINT_BGA695 9 OF 11 REV = 5
USB3.0
Port1
Port2 LEFT USB
Port5 LEFT USB
Port6 Card reader
+3V_PCH
RPH3
USB_OC5# 4 5
USB_OC2# 3 6
USB_OC7# 2 7
USB_OC0# 1 8
10K_1206_8P4R_5%
RPH4
USB_OC6# 4 5
USB_OC1# 3 6
USB_OC4# 2 7
USB_OC3# 1 8
10K_1206_8P4R_5%

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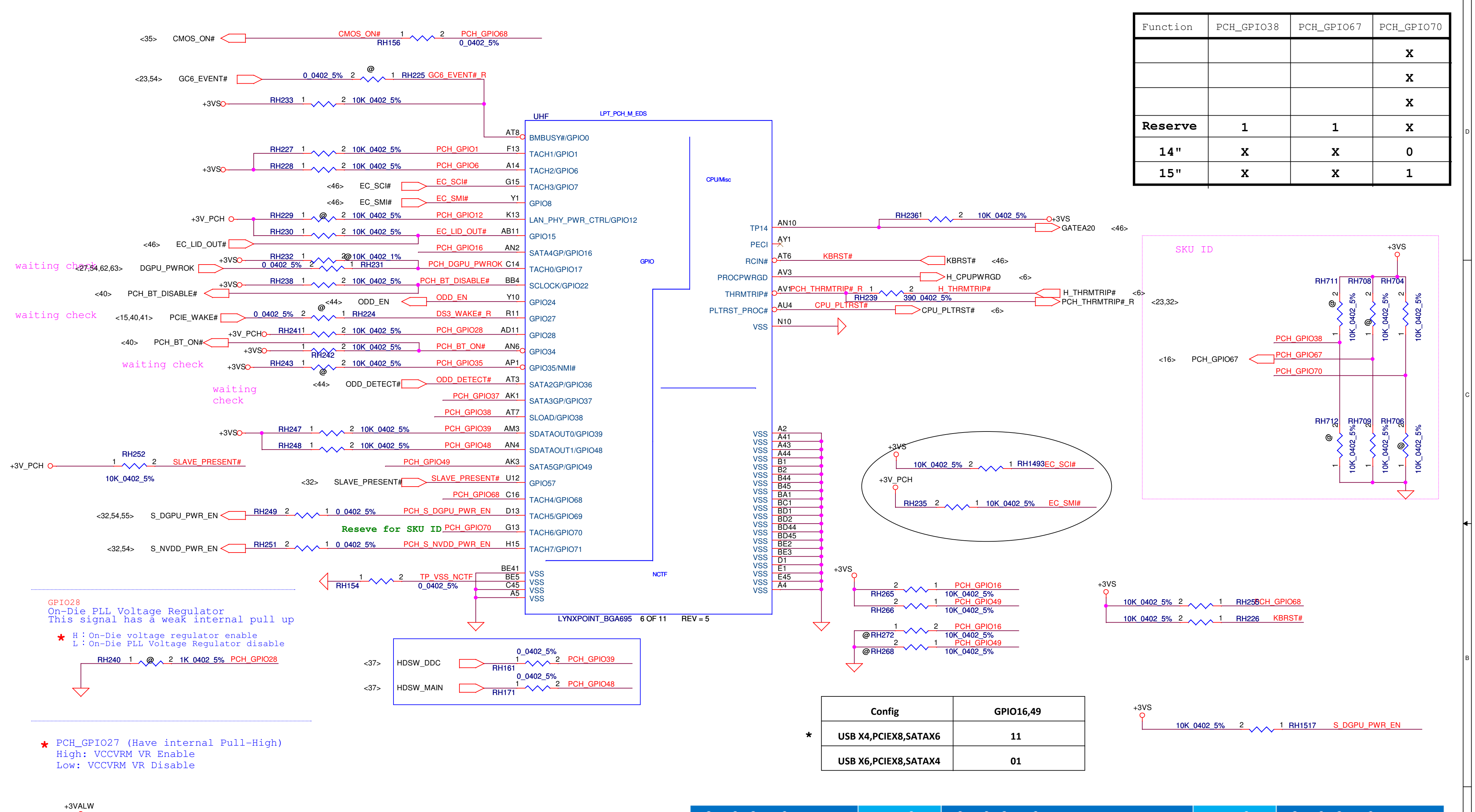
Title
PCH (5/9) PCI, USB

LCFC

Size	Document Number	Rev
Custom	Y501 NM-A032	1.0

Date: Wednesday, March 27, 2013 Sheet 18 of 69



<35> CMOS_ON#
CMOS_ON# RH156 PCH_GPIO68 0_0402_5%
<23,54> GC6_EVENT#
0_0402_5% RH225 GC6_EVENT#_R
+3VS RH233 10K_0402_5%
UHF
LPT_PCH_M_EDS
BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
GPIO24
GPIO27
GPIO28
GPIO34
GPIO35/NMI#
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57
TACH4/GPIO68
TACH5/GPIO69
TACH6/GPIO70
TACH7/GPIO71
GPIO
CPU/Misc
NCTF
TP14
PECI
RCIN#
PROCPWRGD
THRMTRIP#
PLTRST_PROC#
VSS
LYNXPOINT_BGA695 6 OF 11 REV = 5
RH227 10K_0402_5% PCH_GPIO1
RH228 10K_0402_5% PCH_GPIO6
<46> EC_SCI#
<46> EC_SMI#
+3V_PCH RH229 10K_0402_5% PCH_GPIO12
RH230 10K_0402_5% EC_LID_OUT#
<46> EC_LID_OUT#
PCH_GPIO16
waiting check
<27,54,62,63> DGPU_PWROK
RH232 10K_0402_1% RH231 0_0402_5% PCH_DGPU_PWROK
RH238 10K_0402_5% PCH_BT_DISABLE#
<40> PCH_BT_DISABLE#
<44> ODD_EN
waiting check
<15,40,41> PCIE_WAKE#
0_0402_5% RH224 DS3_WAKE#_R
RH2411 10K_0402_5% PCH_GPIO28
<40> PCH_BT_ON#
RH242 10K_0402_5% PCH_BT_ON#
waiting check
RH243 10K_0402_5% PCH_GPIO35
<44> ODD_DETECT#
waiting check
PCH_GPIO37
PCH_GPIO38
RH247 10K_0402_5% PCH_GPIO39
RH248 10K_0402_5% PCH_GPIO48
+3V_PCH RH252 10K_0402_5% SLAVE_PRESENT#
PCH_GPIO49
<32> SLAVE_PRESENT#
PCH_GPIO68
<32,54,55> S_DGPU_PWR_EN
RH249 0_0402_5% PCH_S_DGPU_PWR_EN
Reserve for SKU ID
PCH_GPIO70
<32,54> S_NVDD_PWR_EN
RH251 0_0402_5% PCH_S_NVDD_PWR_EN
RH154 0_0402_5% TP_VSS_NCTF
RH2361 10K_0402_5% +3VS
GATEA20 <46>
KBRST# <46>
H_CPUPWRGD <6>
PCH_THRMTRIP#_R RH239 390_0402_5% H_THRMTRIP#
H_THRMTRIP# <6>
PCH_THRMTRIP#_R <23,32>
CPU_PLTRST# <6>
SKU ID
RH711 RH708 RH704 10K_0402_5%
PCH_GPIO38
<16> PCH_GPIO67
PCH_GPIO70
RH712 RH709 RH706 10K_0402_5%
+3VS 10K_0402_5% RH1493 EC_SCI#
+3V_PCH RH235 10K_0402_5% EC_SMI#
RH265 10K_0402_5% PCH_GPIO16
RH266 10K_0402_5% PCH_GPIO49
RH272 10K_0402_5% PCH_GPIO16
RH268 10K_0402_5% PCH_GPIO49
+3VS 10K_0402_5% RH255 PCH_GPIO68
10K_0402_5% RH226 KBRST#
<37> HDSW_DDC RH161 0_0402_5% PCH_GPIO39
<37> HDSW_MAIN RH171 0_0402_5% PCH_GPIO48
RH240 1K_0402_5% PCH_GPIO28
+3VS 10K_0402_5% RH1517 S_DGPU_PWR_EN

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
			X
			X
			X
Reserve	1	1	X
14"	X	X	0
15"	X	X	1

	Config	GPIO16,49
*	USB X4,PCIEX8,SATAX6	11
	USB X6,PCIEX8,SATAX4	01

+3VALW RH207 DS3@ 10K_0402_5% DS3_WAKE#_R

+3VS 200K_0402_5% RH250 ODD_DETECT#

RH259 10K_0402_5% PCH_GPIO37

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1 (00) USB3 3 (01)	PCIE 2 (00) USB3 4 (01)	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4 (00) PCIE 1 (01)	SATA 5 (00) PCIE 2 (01)	SATA 0	SATA 1	SATA 2	SATA 3

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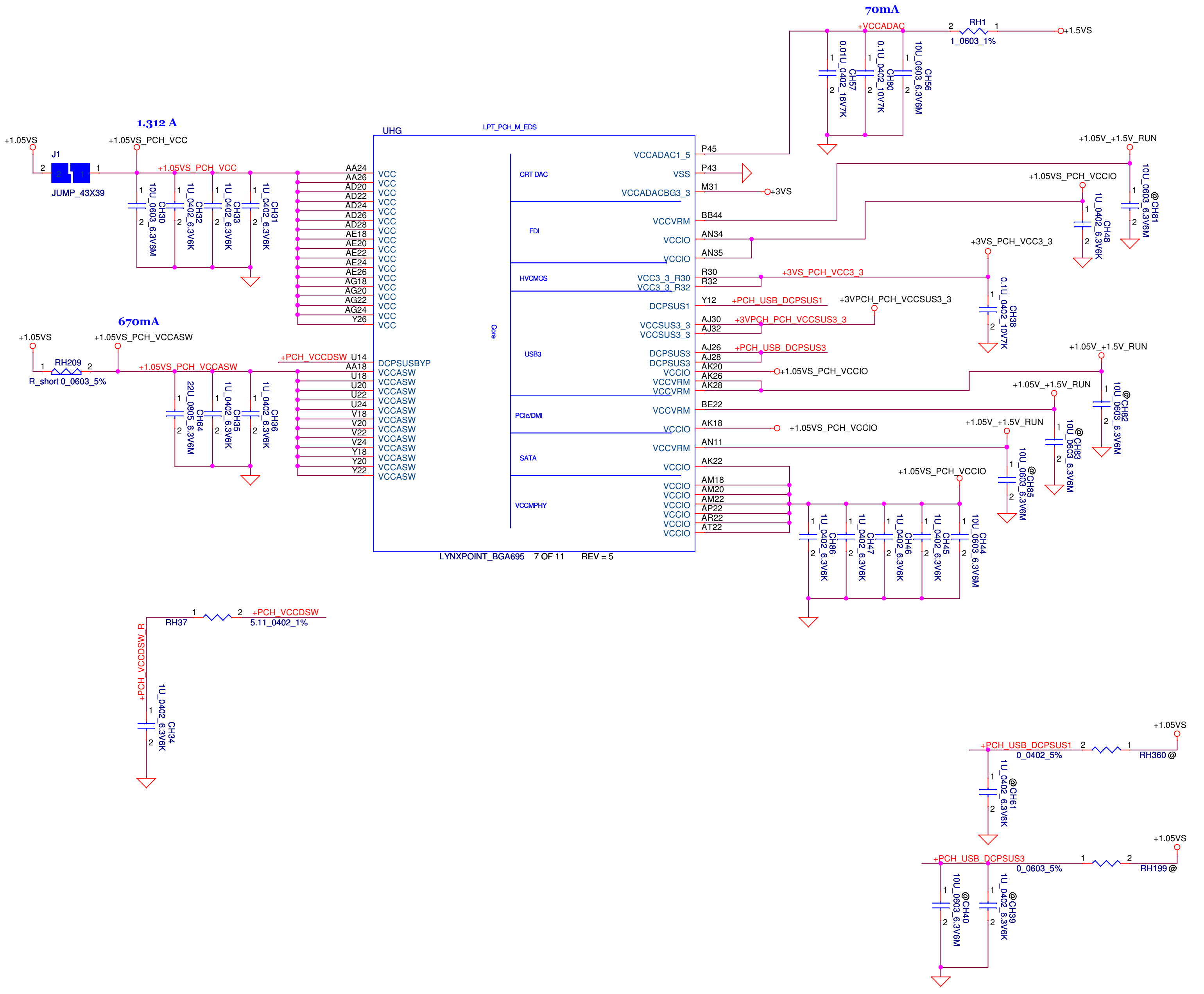
Title
PCH (6/9) GPIO, CPU, MISC

Size Custom
Document Number Y501 NM-A032
Rev 1.0
Date: Wednesday, March 27, 2013 Sheet 19 of 69



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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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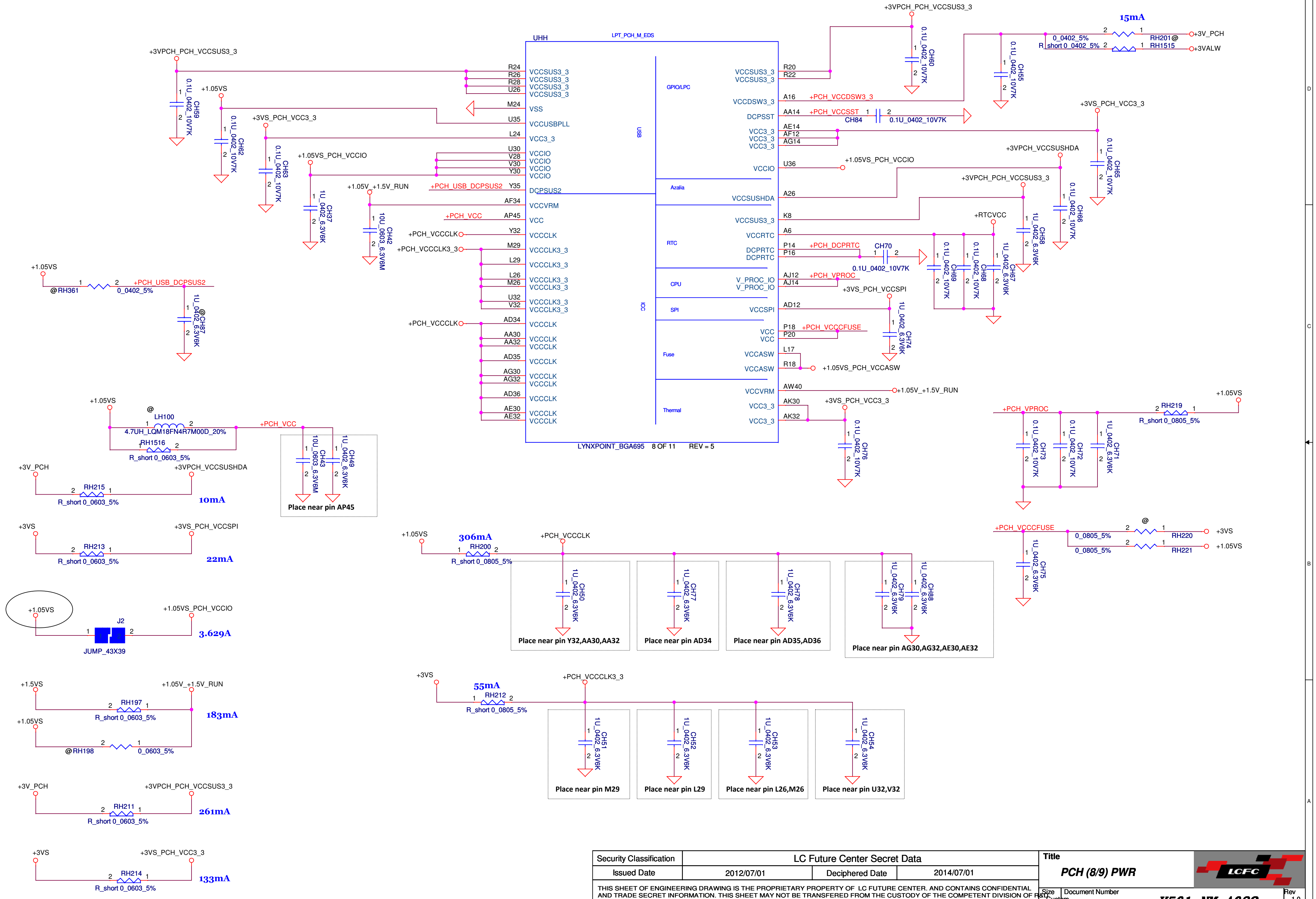
Title
PCH (7/9) PWR

LCFC

Size	Document Number	Rev
Custom	Y501 NM-A032	1.0

Date: Wednesday, March 27, 2013 Sheet 20 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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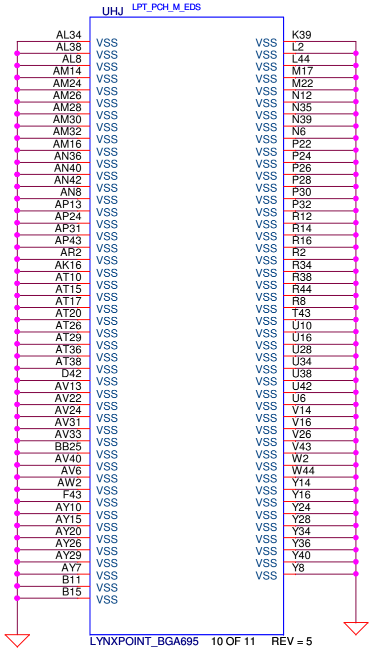
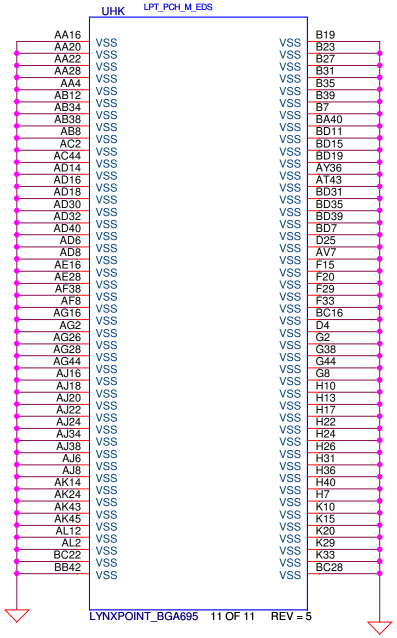
Title
PCH (8/9) PWR

LCFC

Size: Custom
Document Number: **Y501 NM-A032**
Rev: 1.0

Date: Wednesday, March 27, 2013 Sheet 21 of 69





Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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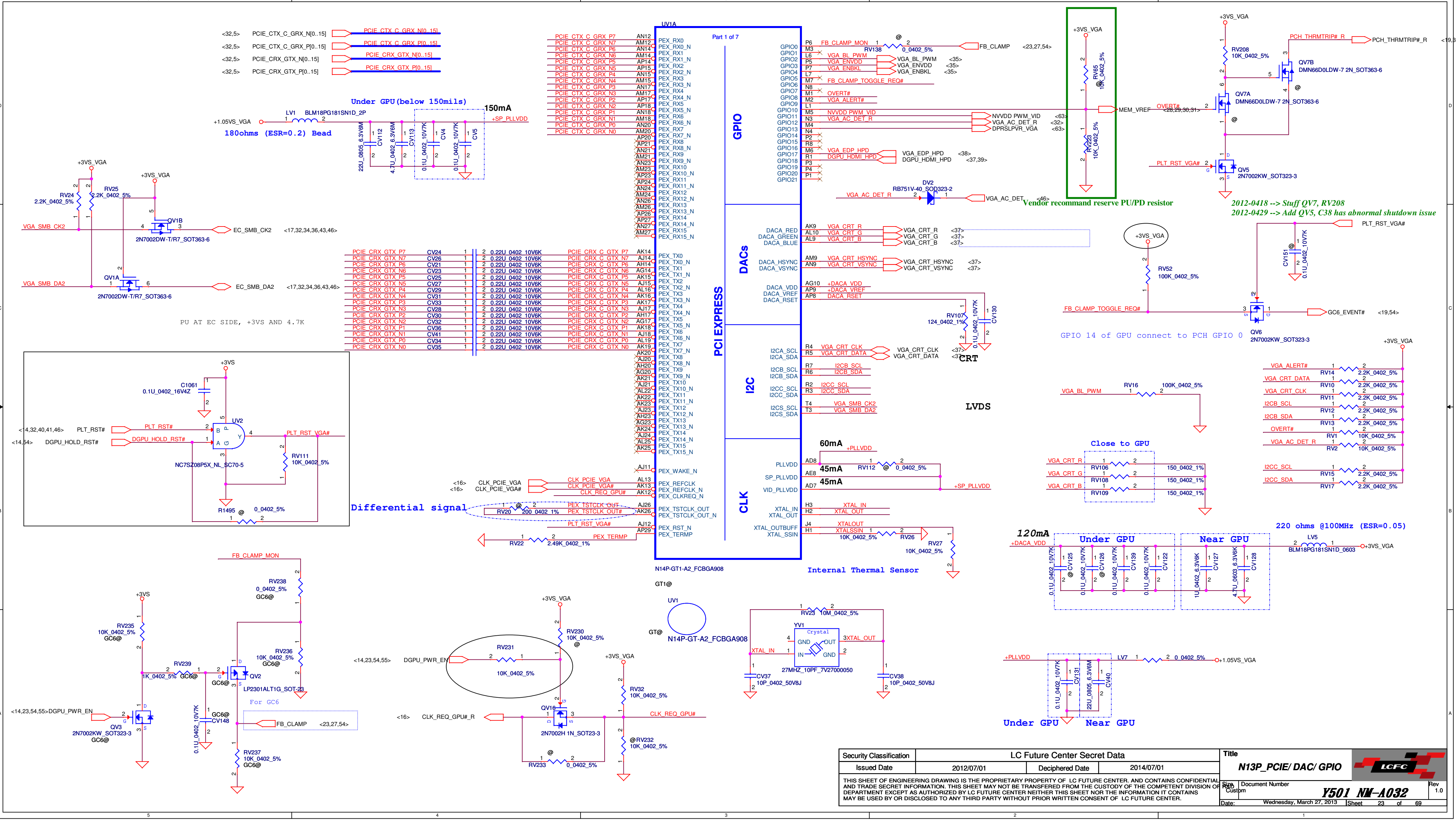
Title
PCH (9/9) VSS

LCFC

Size	Document Number	Rev
Custom	Y501 NM-A032	1.0

Date: Wednesday, March 27, 2013 Sheet 22 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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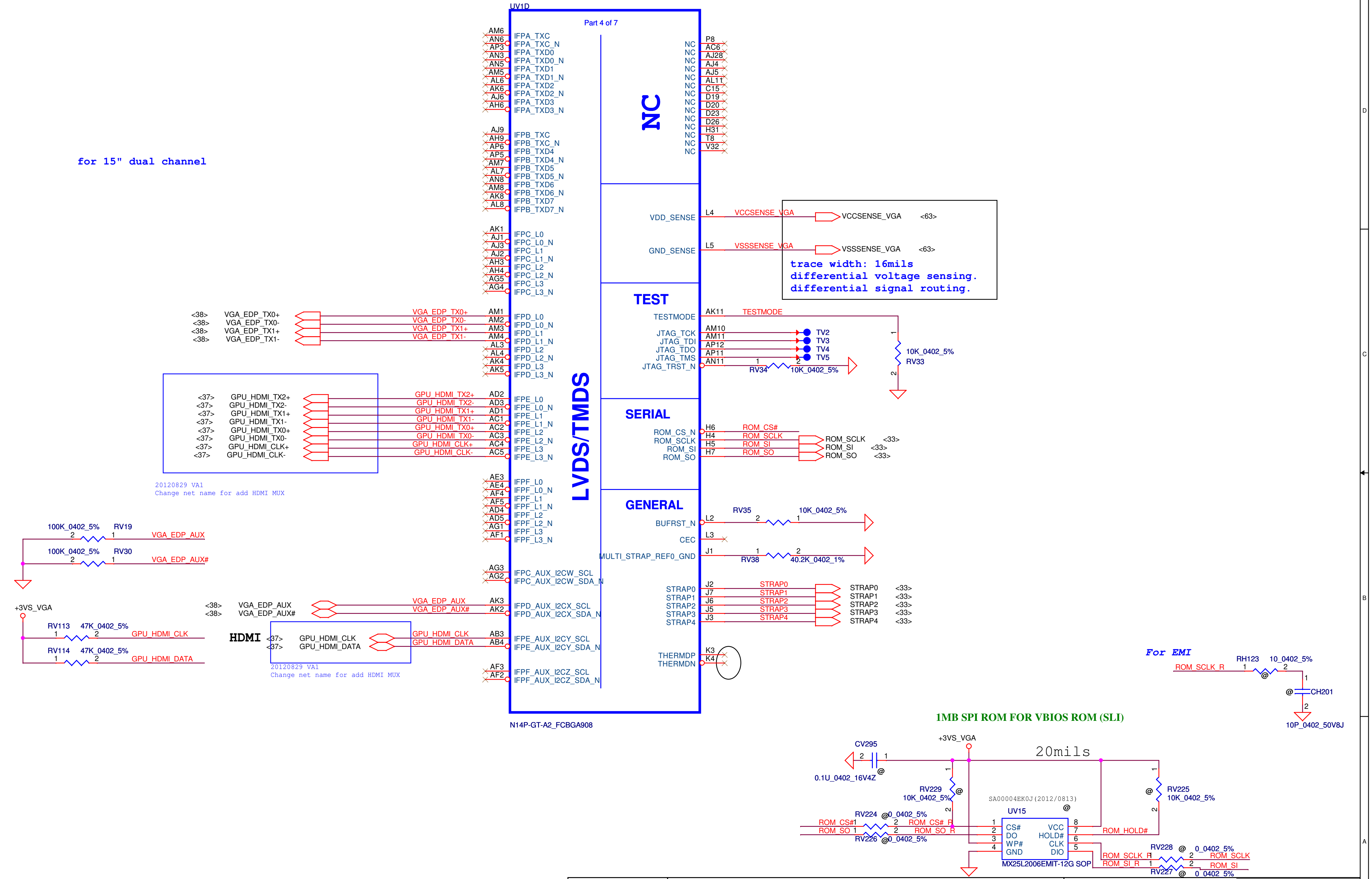
Title
N13P_PCIE/ DAC/ GPIO

Size Custom | Document Number Y501 NM-A032 | Rev 1.0

Date: Wednesday, March 27, 2013 | Sheet 23 of 69



for 15" dual channel

trace width: 16mils
differential voltage sensing.
differential signal routing.

20120829 VA1
Change net name for add HDMI MUX

20120829 VA1
Change net name for add HDMI MUX

For EMI

1MB SPI ROM FOR VBIOS ROM (SLI)

20mils

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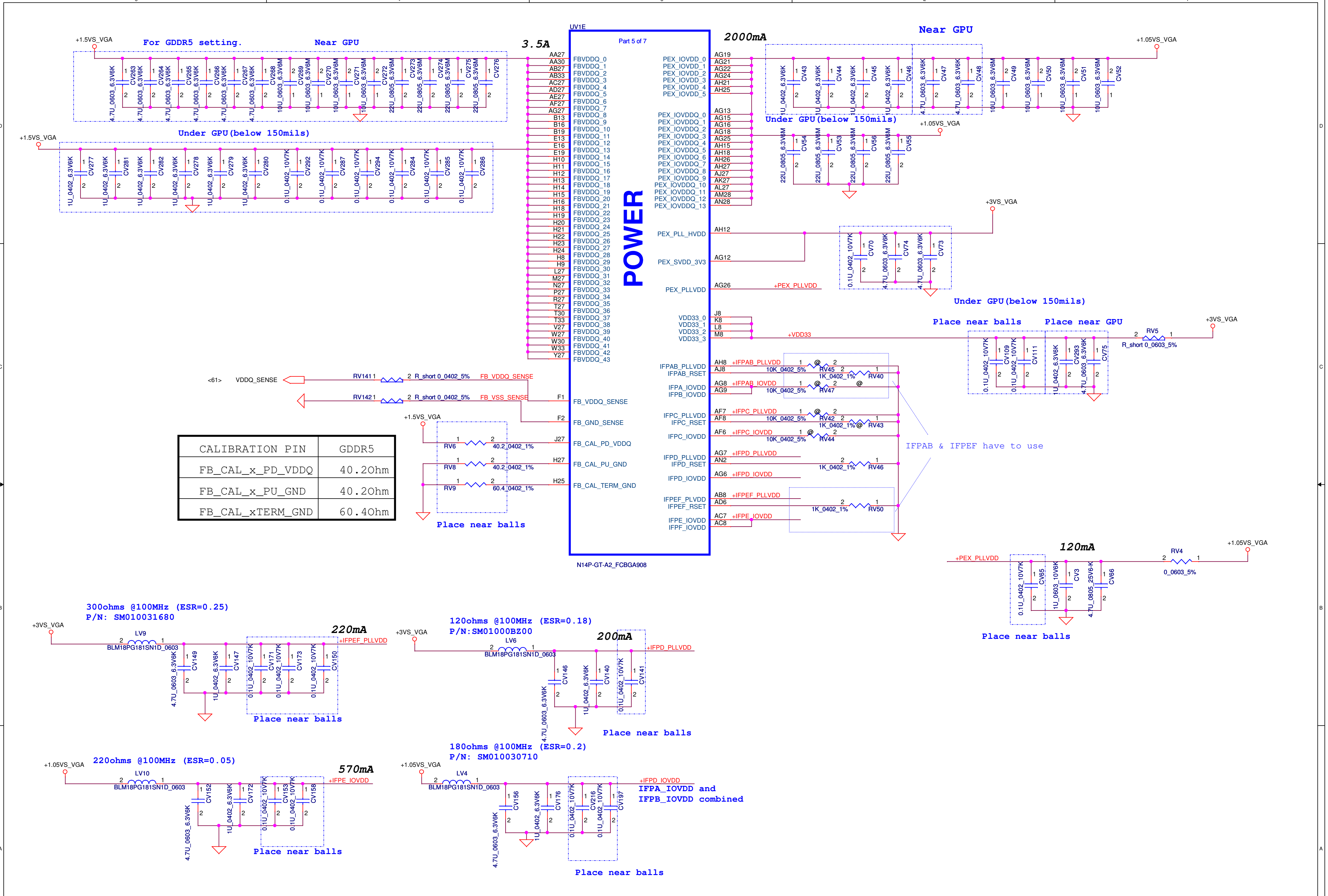
Title
N13P_LVDS/ HDMI/ THERM

LCFC

Size	Document Number	Rev
Custom	Y501 NM-A032	1.0

Date: Wednesday, March 27, 2013 Sheet 24 of 69



CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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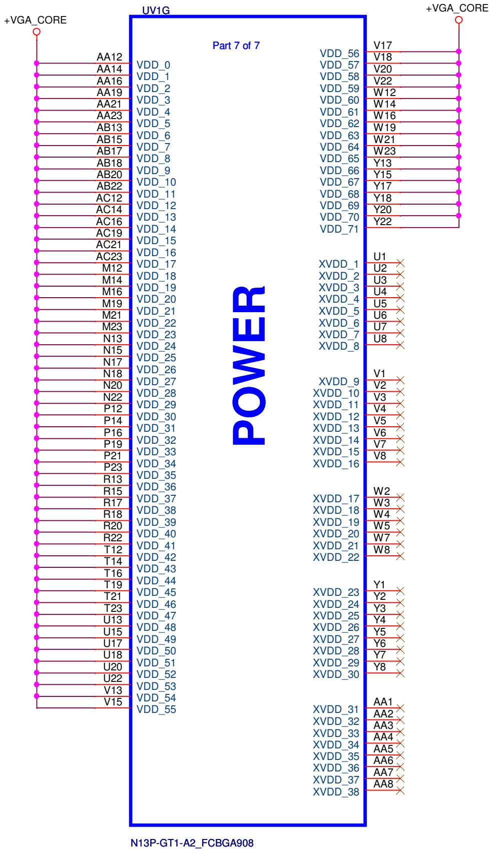
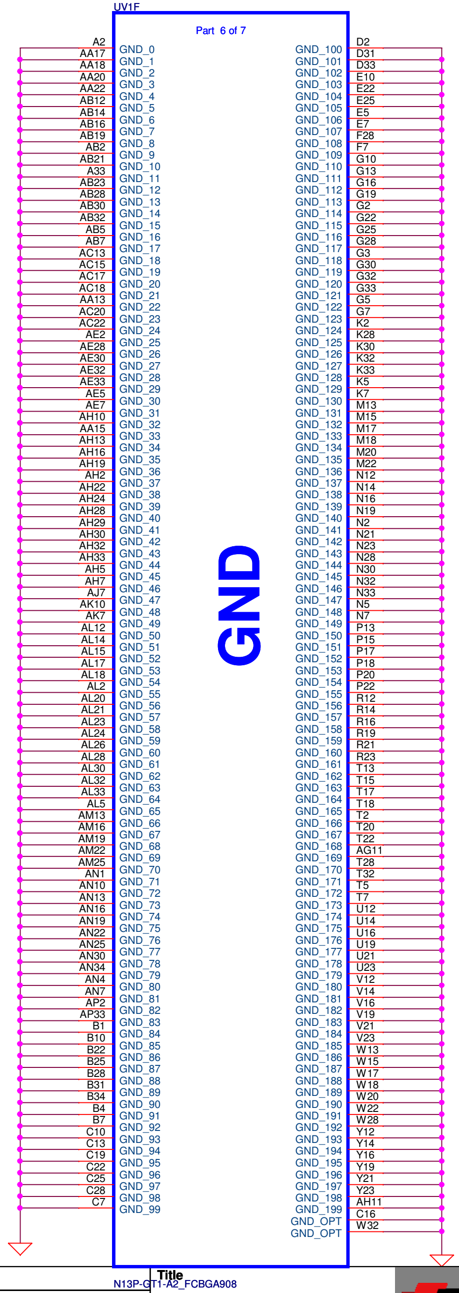
Title
N13P_Power

Size Custom
Document Number Y501 NM-A032
Rev 1.0

Date: Wednesday, March 27, 2013 Sheet 25 of 69





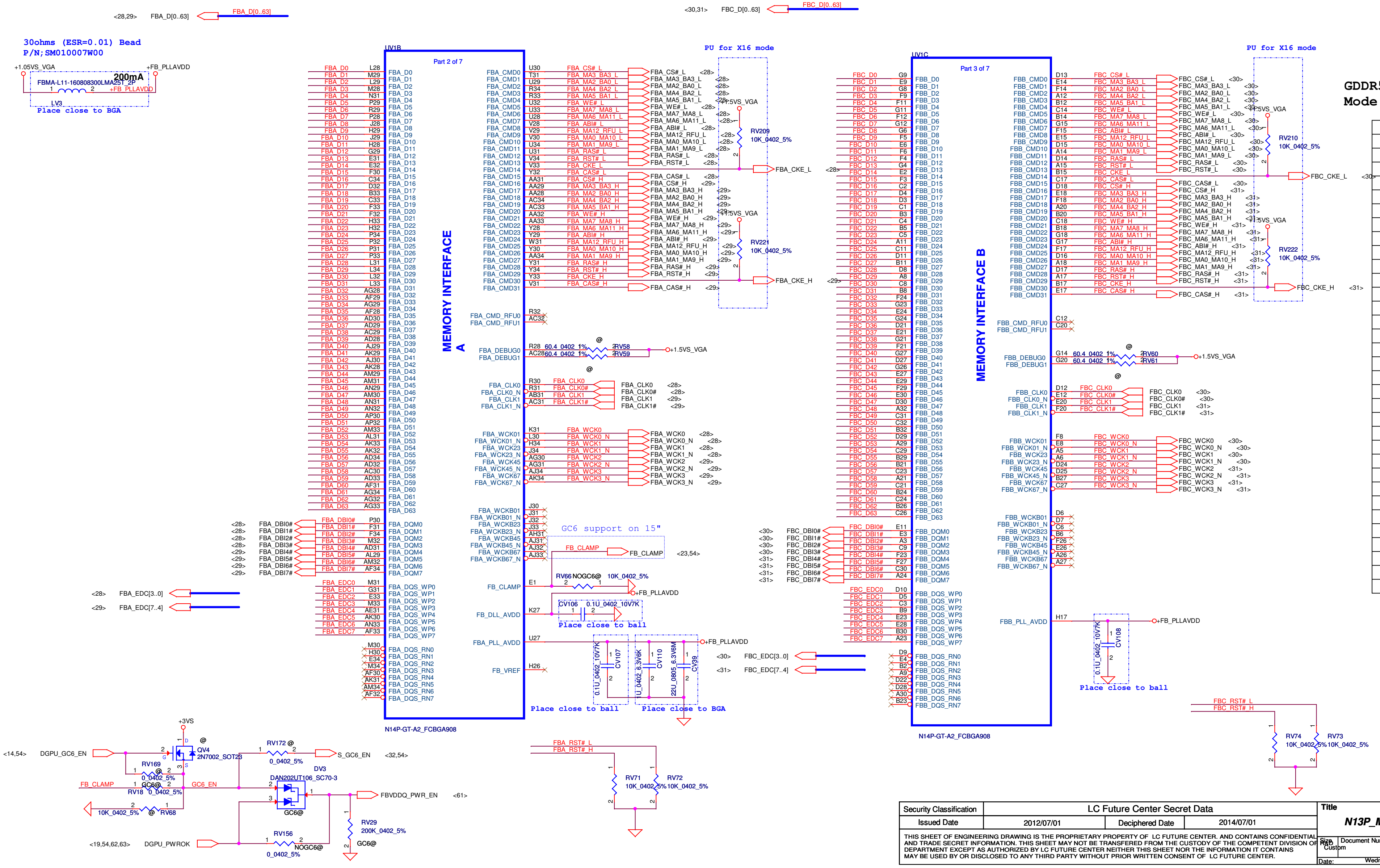
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_+VGA CORE, GND

LCFC

Size	Document Number	Rev
Custom	Y501 NM-A032	1.0

Date: Wednesday, March 27, 2013



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_MEM Interface

LCFC

Size: Custom
Document Number: Y501 NM-A032
Rev: 1.0
Date: Wednesday, March 27, 2013
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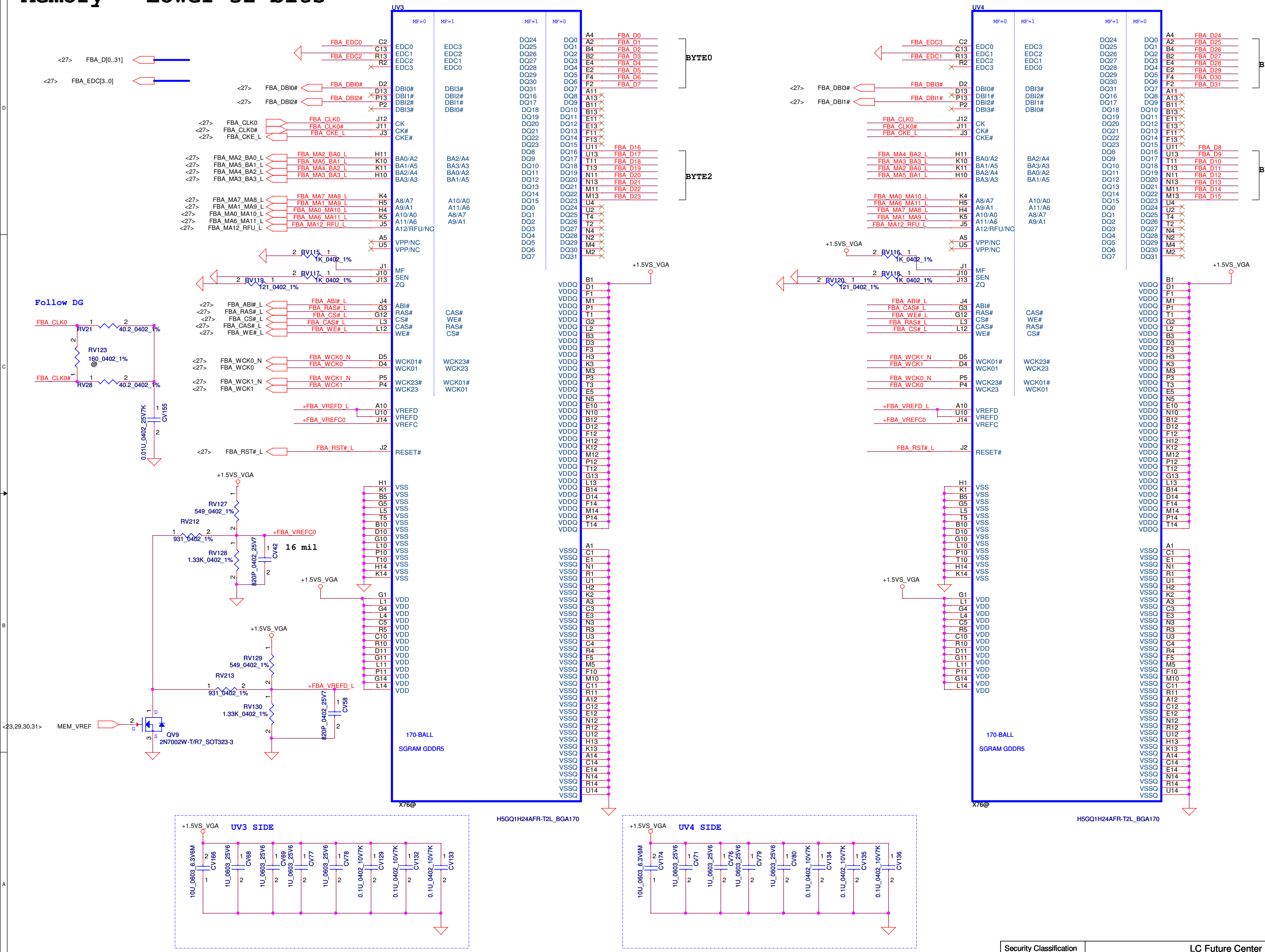
Memory - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

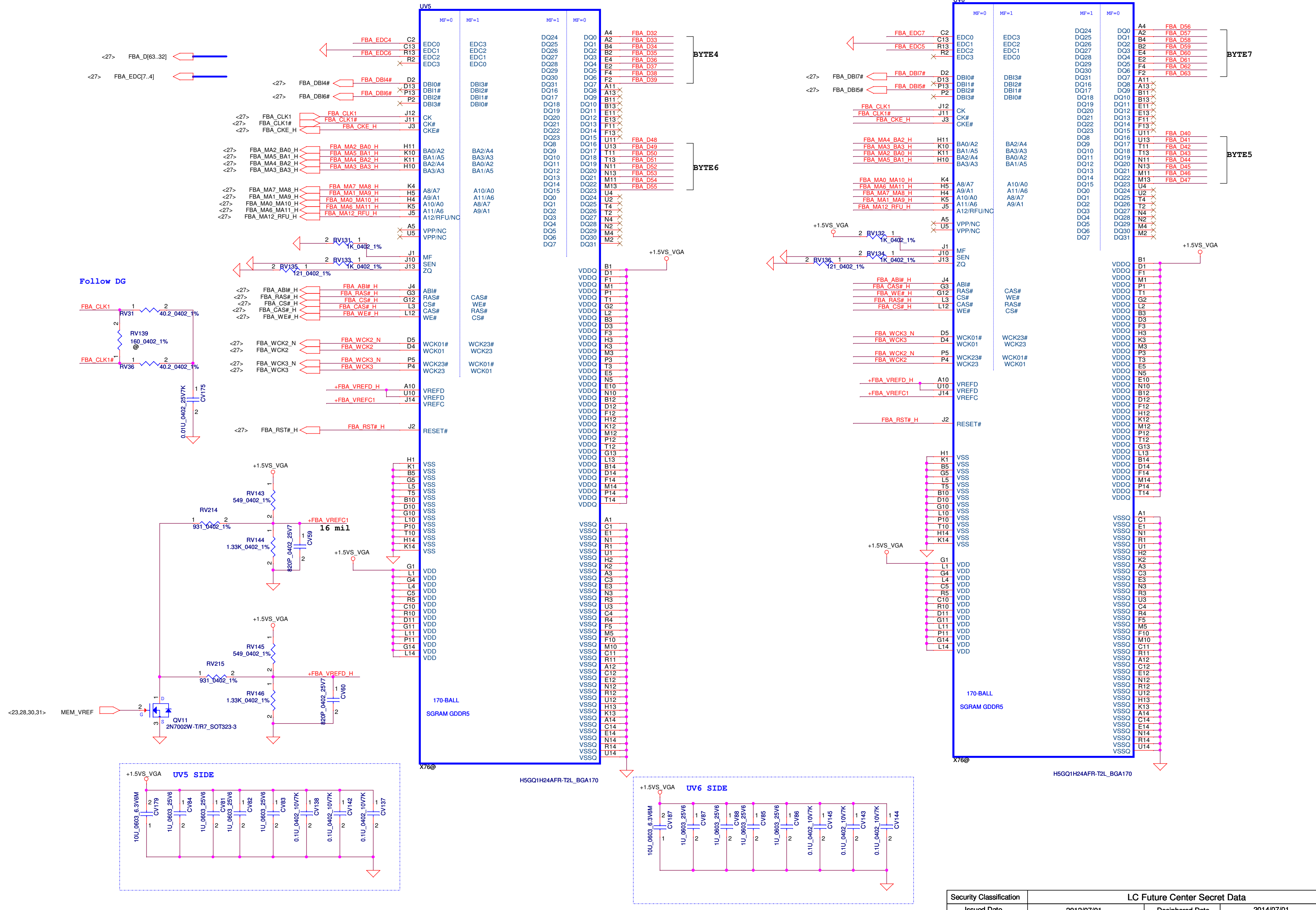
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_GDDR5_A Lower
LCFC

Size	Document Number	Rev
Custom	Y501 NM-A032	1.0

Date: Wednesday, March 27, 2013
Sheet 28 of 69

Memory - Upper 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_GDDR5_A Upper

Size	Document Number	Rev
Custom	Y501 NM-A032	1.0

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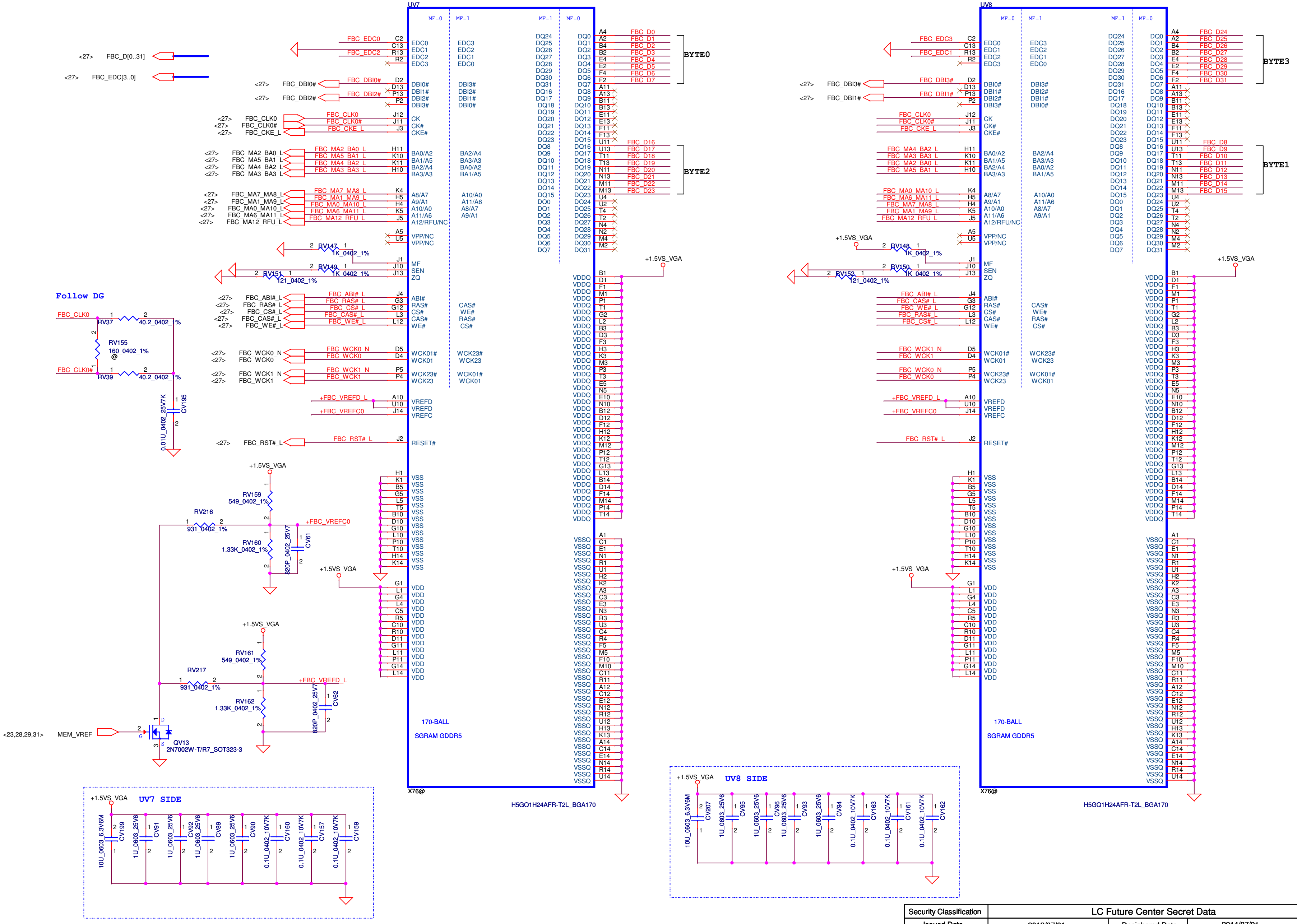
Memory Partition C - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

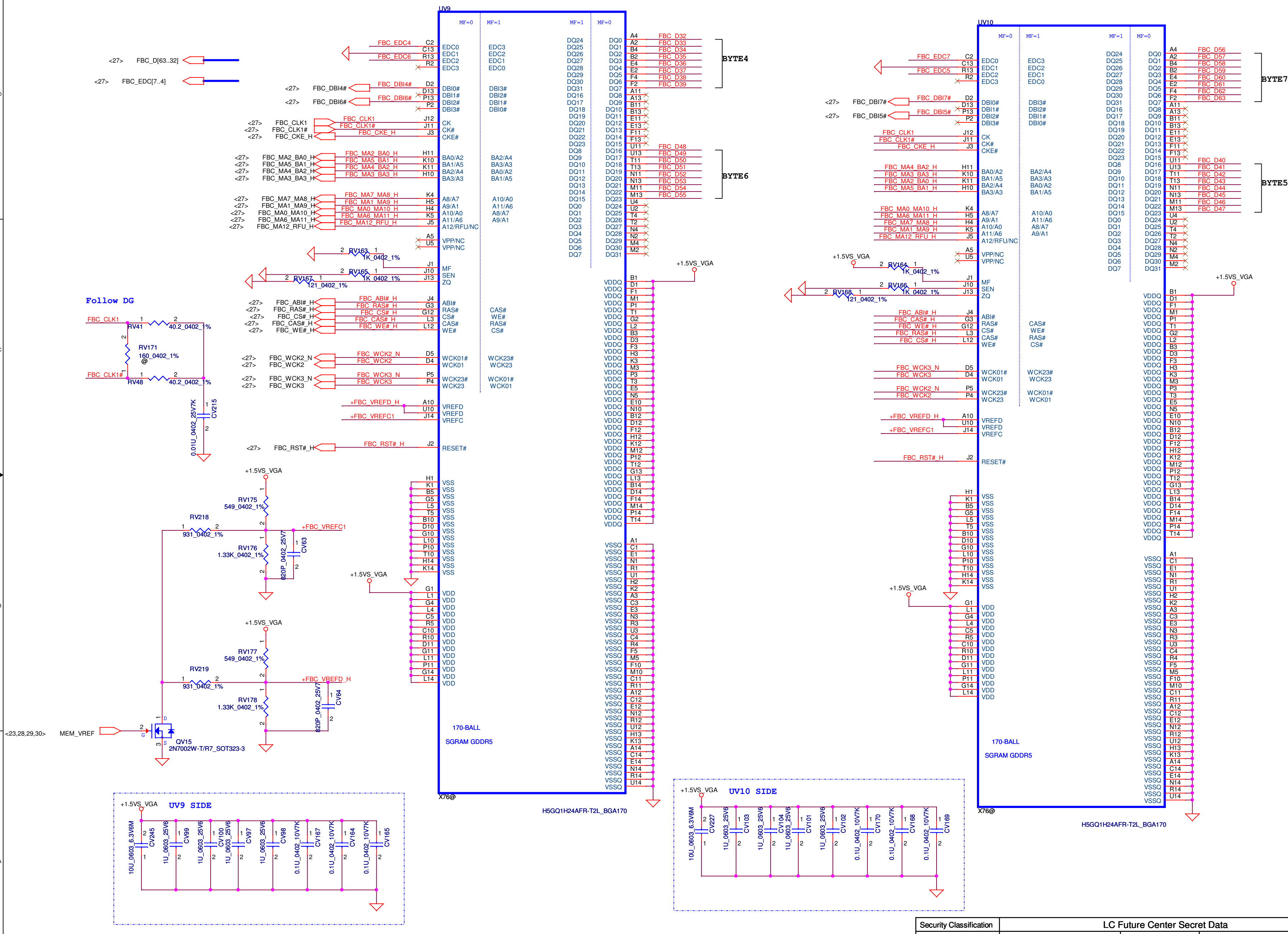
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_GDDR5_C Lower

LCFC

Size: Custom
Document Number: Y501 NM-A032
Rev: 1.0
Date: Wednesday, March 27, 2013

Memory Partition C - Upper 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_GDDR5_C Upper
LCFC
Size: Custom
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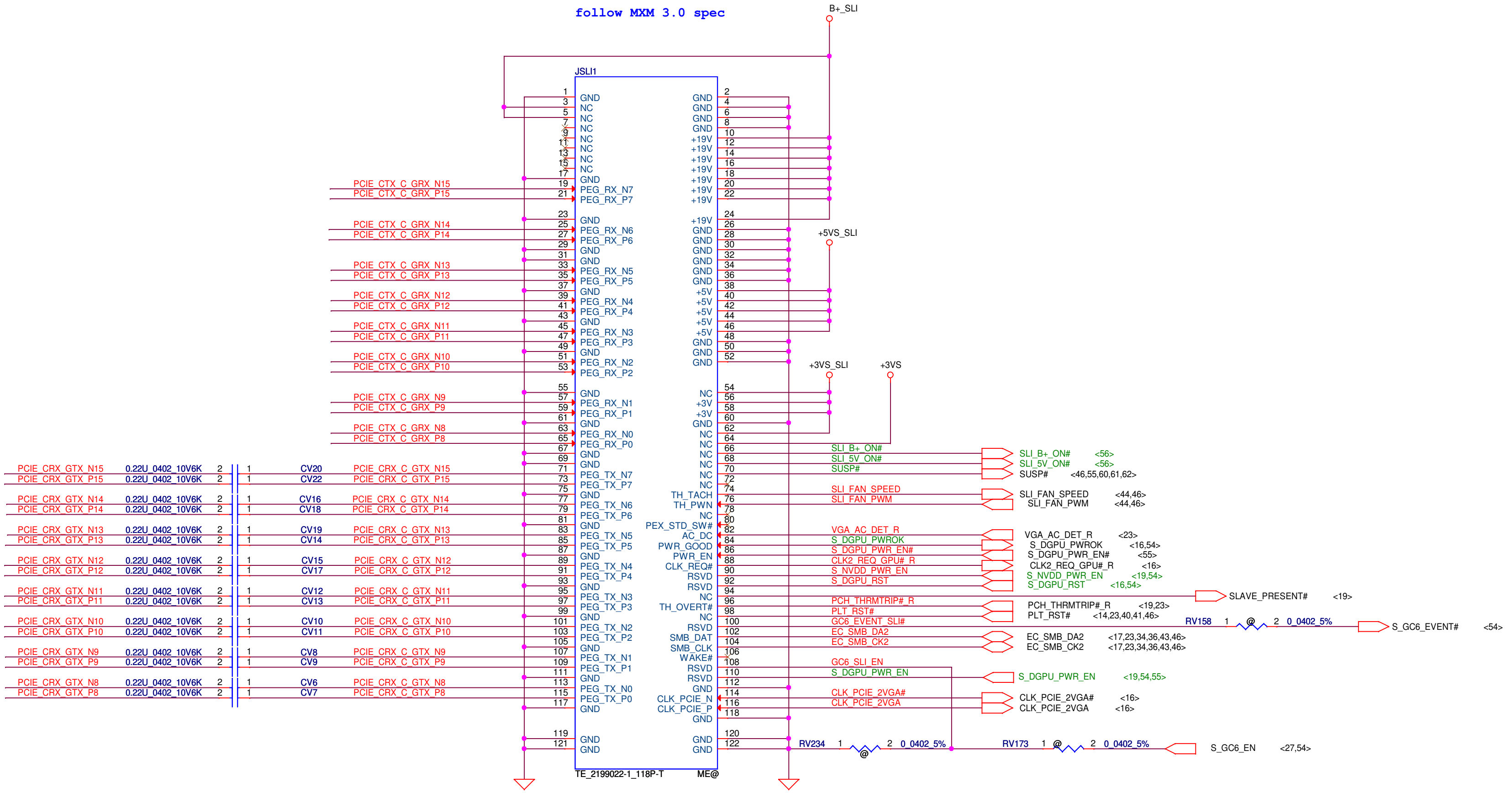
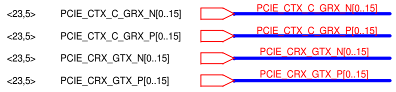
Date: Wednesday, March 27, 2013

follow MXM 3.0 spec



11/11 for 2nd VGA fan
need to notic EC


<23,5> PCIE_CTX_C_GRX_N[0..15]
PCIE_CTX_C_GRX_N[0..15]
<23,5> PCIE_CTX_C_GRX_P[0..15]
PCIE_CTX_C_GRX_P[0..15]
<23,5> PCIE_CRX_GTX_N[0..15]
PCIE_CRX_GTX_N[0..15]
<23,5> PCIE_CRX_GTX_P[0..15]
PCIE_CRX_GTX_P[0..15]

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
VGA MXM

LCFC

Size: Custom
Document Number: Y501 NM-A032
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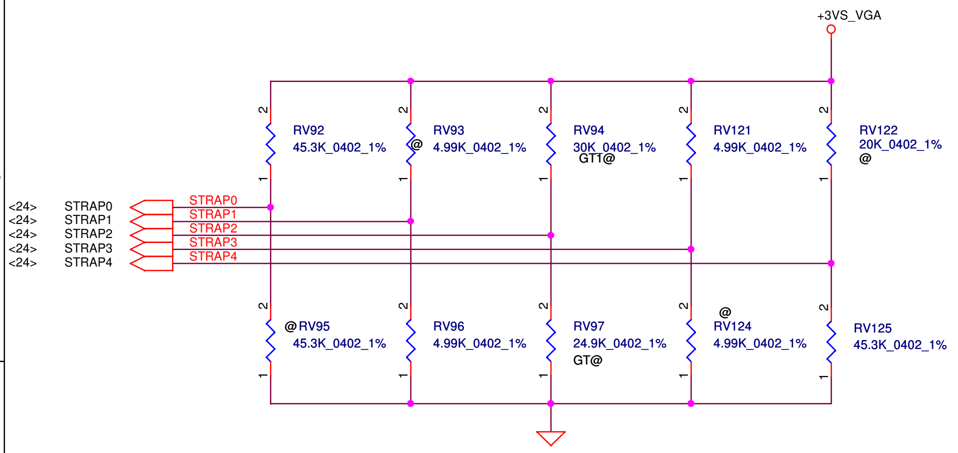

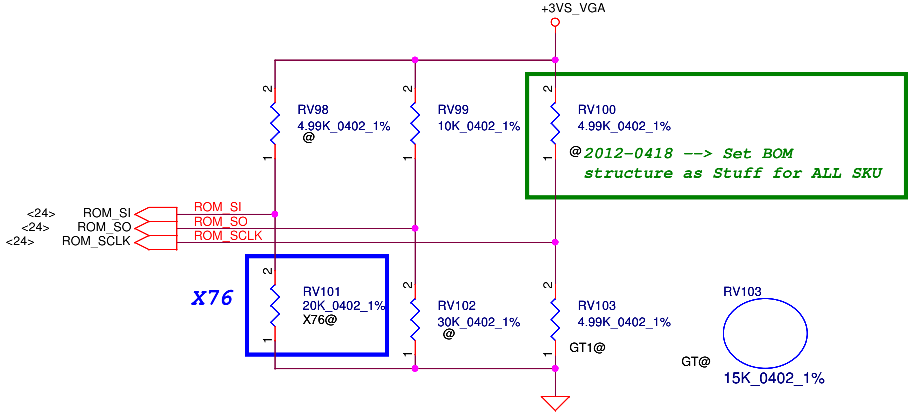

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0000	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

X76

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GT1 28nm	Samsung	K4G20325FD-FC04 2G 64Mx32	PD 30K	PU 10K	PD 15K (ROM not present) PD 35K (ROM present)	PU 45K	PD 5K	PD 25K	PU 5K	PD 45K
		K4G10325FG-HC04 1G 32Mx32	PD 45K							
	Hynix	~~H5GQ2H24MFR-T2C 2G 64Mx32~~ EOL	~~PD 25K~~							
		H5GQ1H24BFR-T2C 1G 32Mx32	PD 20K							
		H5GQ2H24AFR-T2C 2G 64Mx32	PD 25K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01 (2G 64Mx32)	SA00005B70J
	X76409JVL51 (1G 32Mx16)	SA00003RS0J
Hynix	X76409JVL02 (2G 64Mx32)	SA00004GD0J EOL
	X76409JVL02 (2G 64Mx32)	SA00004GD1J
	X76409JVL52 (1G 32Mx16)	SA00003WL1J

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Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
N13P_MISC

LCFC

Size: Custom
Document Number: Y501 NM-A032
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Date: Wednesday, March 27, 2013
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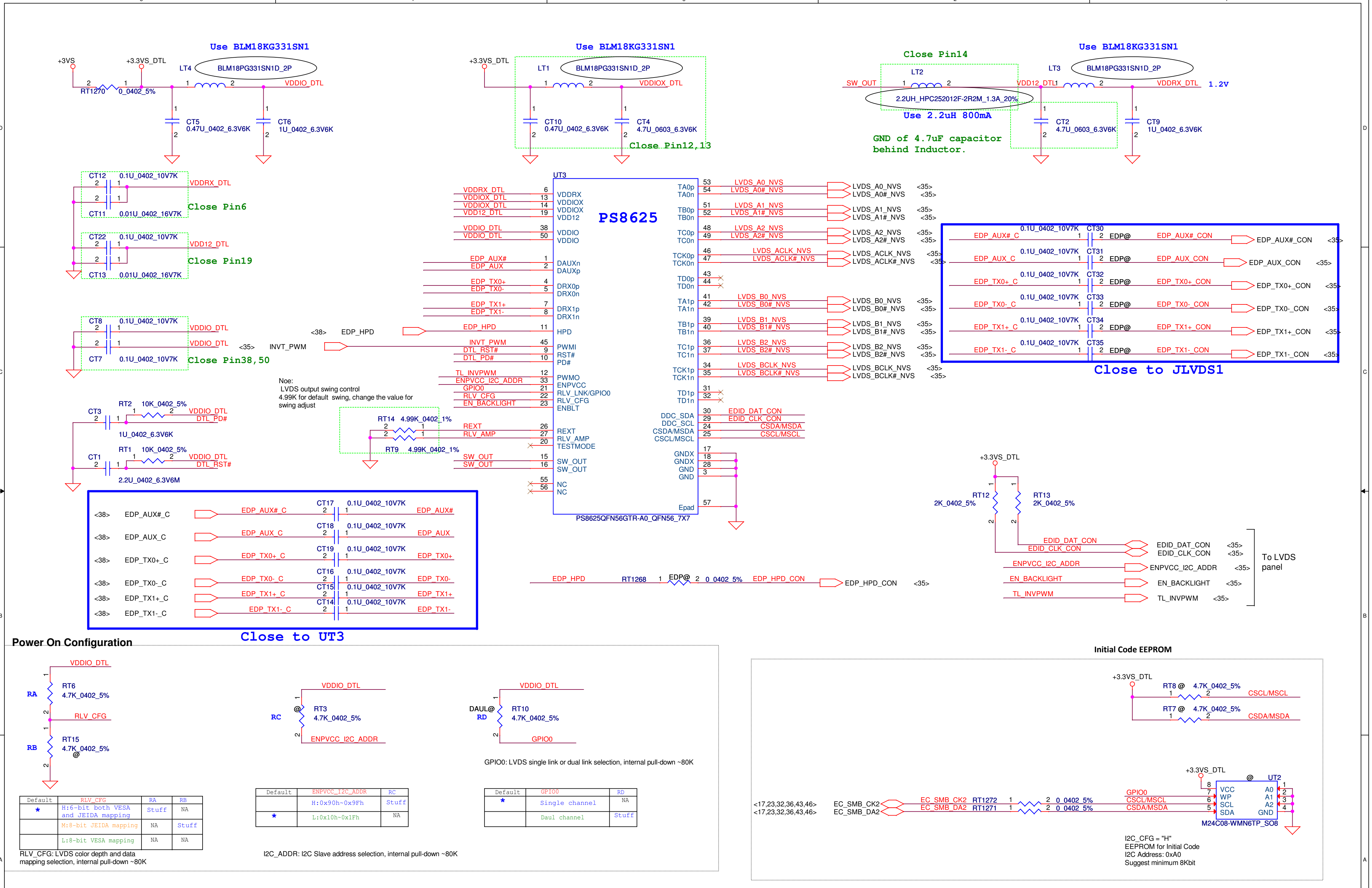

Default	RLV_CFG	RA	RB
*	H:6-bit both VESA and JEIDA mapping	Stuff	NA
	M:8-bit JEIDA mapping	NA	Stuff
	L:8-bit VESA mapping	NA	NA

RLV_CFG: LVDS color depth and data mapping selection, internal pull-down ~80K

Default	ENPVCC_I2C_ADDR	RC
	H:0x90h~0x9Fh	Stuff
*	L:0x10h~0x1Fh	NA

I2C_ADDR: I2C Slave address selection, internal pull-down ~80K

Default	GPIO0	RD
*	Single channel	NA
	Daul channel	Stuff

GPIO0: LVDS single link or dual link selection, internal pull-down ~80K

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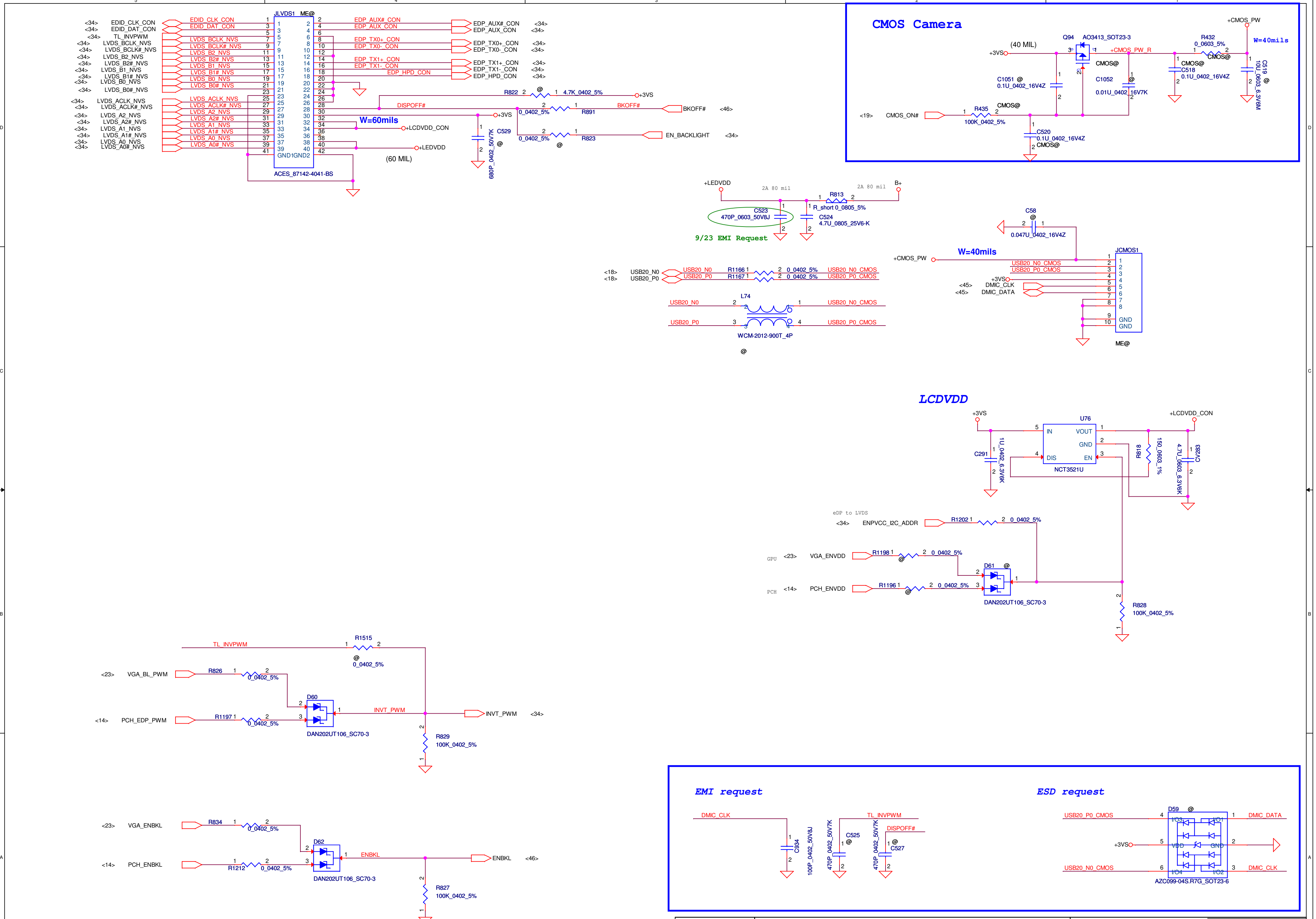
Title
LVDS/ CMOS/ USB-ReDriver

LCFC

Size: Custom
Document Number: Y501 NM-A032
Rev: 1.0
Date: Wednesday, March 27, 2013



LVDS LOAD SWITCH

1.9mS Typical Rise time ,Rds_on 80m ohm

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Title
LVDS/ CMOS/ USB-ReDriver

LCFC

Size: Custom
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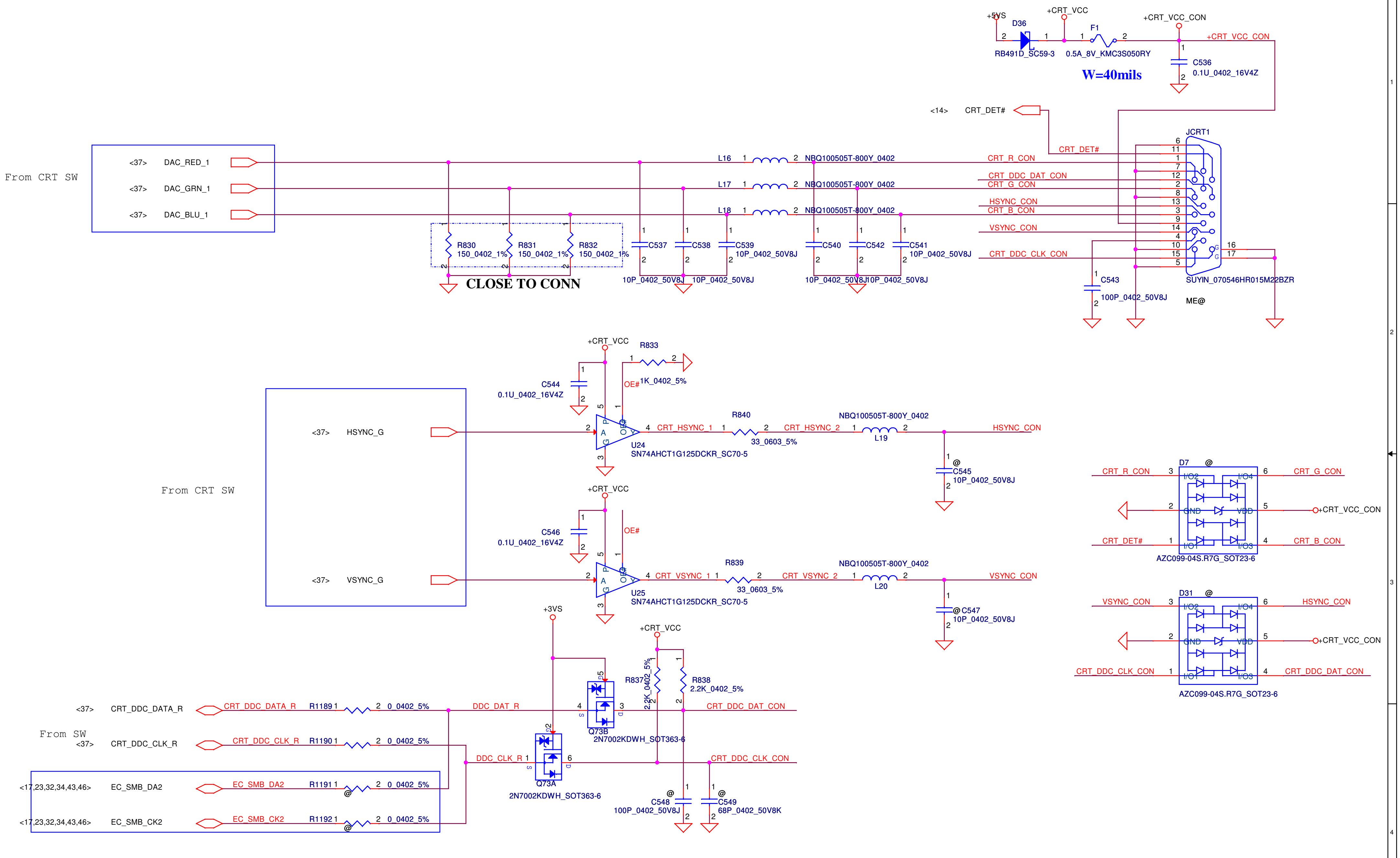
CRT Connector



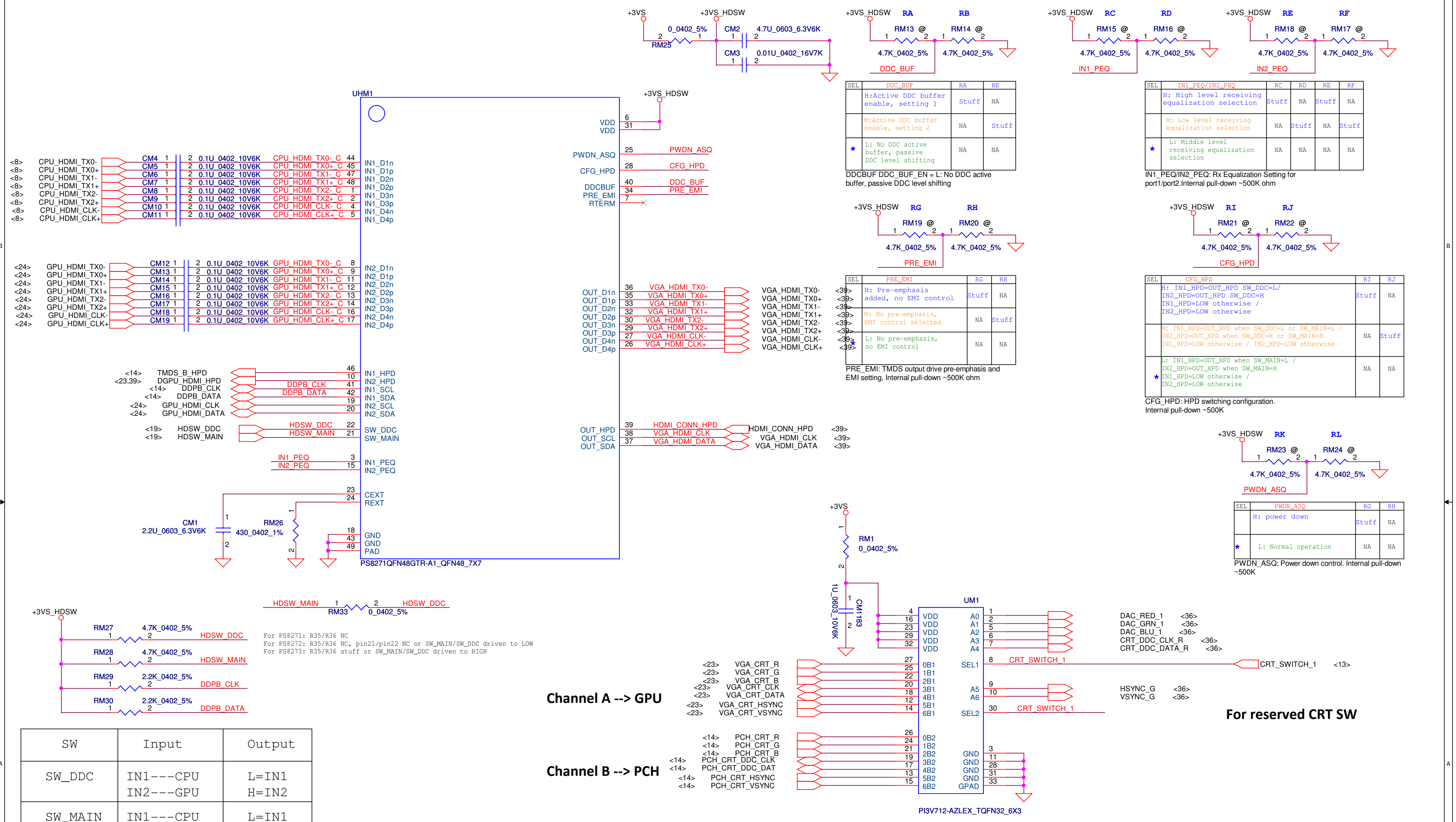
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
CRT Connector

LCFC

Size	Document Number	Rev
Custom	Y501 NM-A032	1.0

Date: Wednesday, March 27, 2013 Sheet 36 of 69



SEL	DDC_BUF	RA	RB
	H:Active DDC buffer enable, setting 1	Stuff	NA
	M:Active DDC buffer enable, setting 2	NA	Stuff
*	L: No DDC active buffer, passive DDC level shifting	NA	NA

DDCBUF DDC_BUF_EN = L: No DDC active buffer, passive DDC level shifting

SEL	IN1_PEQ/IN2_PEQ	RC	RD	RE	RF
	H: High level receiving equalization selection	Stuff	NA	Stuff	NA
	M: Low level receiving equalization selection	NA	Stuff	NA	Stuff
*	L: Middle level receiving equalization selection	NA	NA	NA	NA

IN1_PEQ/IN2_PEQ: Rx Equalization Setting for port1/port2.Internal pull-down ~500K ohm

SEL	PRE_EMI	RG	RH
	H: Pre-emphasis added, no EMI control	Stuff	NA
	M: No pre-emphasis, EMI control selected	NA	Stuff
*	L: No pre-emphasis, no EMI control	NA	NA

PRE_EMI: TMDS output drive pre-emphasis and EMI setting, Internal pull-down ~500K ohm

SEL	CFG_HPD	RI	RJ
	H: IN1_HPD=OUT_HPD SW_DDC=L / IN2_HPD=OUT_HPD SW_DDC=H IN1_HPD=LOW otherwise / IN2_HPD=LOW otherwise	Stuff	NA
	M: IN1_HPD=OUT_HPD when SW_DDC=L or SW_MAIN=L / IN2_HPD=OUT_HPD when SW_DDC=H or SW_MAIN=H IN1_HPD=LOW otherwise / IN2_HPD=LOW otherwise	NA	Stuff
*	L: IN1_HPD=OUT_HPD when SW_MAIN=L / IN2_HPD=OUT_HPD when SW_MAIN=H IN1_HPD=LOW otherwise / IN2_HPD=LOW otherwise	NA	NA

CFG_HPD: HPD switching configuration.
Internal pull-down ~500K

SEL	PWDN_ASQ	RG	RH
	H: power down	Stuff	NA
*	L: Normal operation	NA	NA

PWDN_ASQ: Power down control. Internal pull-down ~500K

SW	Input	Output

SW_DDC	IN1---CPU
	IN2---GPU
		L=IN1
		H=IN2

SW_MAIN	IN1---CPU
	IN2---GPU
		L=IN1
		H=IN2

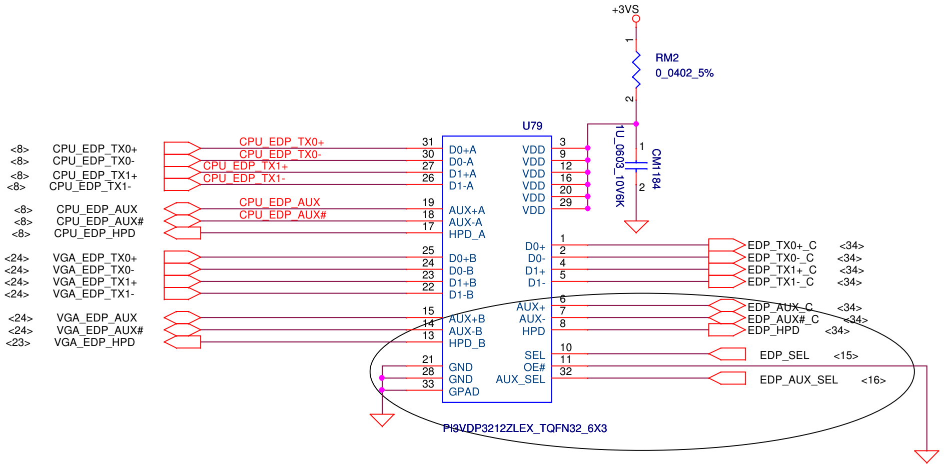
Input SELx	Input/Output An	Function
L	nB1--GPU	An=nB1
H	nB2---PCH	An=nB2

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
HDMI and CRT SW

LCFC

Size: Custom
Document Number: Y501 NM-A032
Rev: 1.0
Date: Wednesday, March 27, 2013



OE#	SEL	AUX_SEL	FUNCTION
L	L	L	PORT A
L	L	H	PORT A-HS, PORT B-HPD/AUX
L	H	L	PORT B-HS, PORT A-HPD/AUX
L	H	H	PORT B
H	X	X	IC POWER DOWN

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
LVDS/ CMOS/ USB-ReDriver
LCFC
Size Custom
Document Number **Y501 NM-A032**
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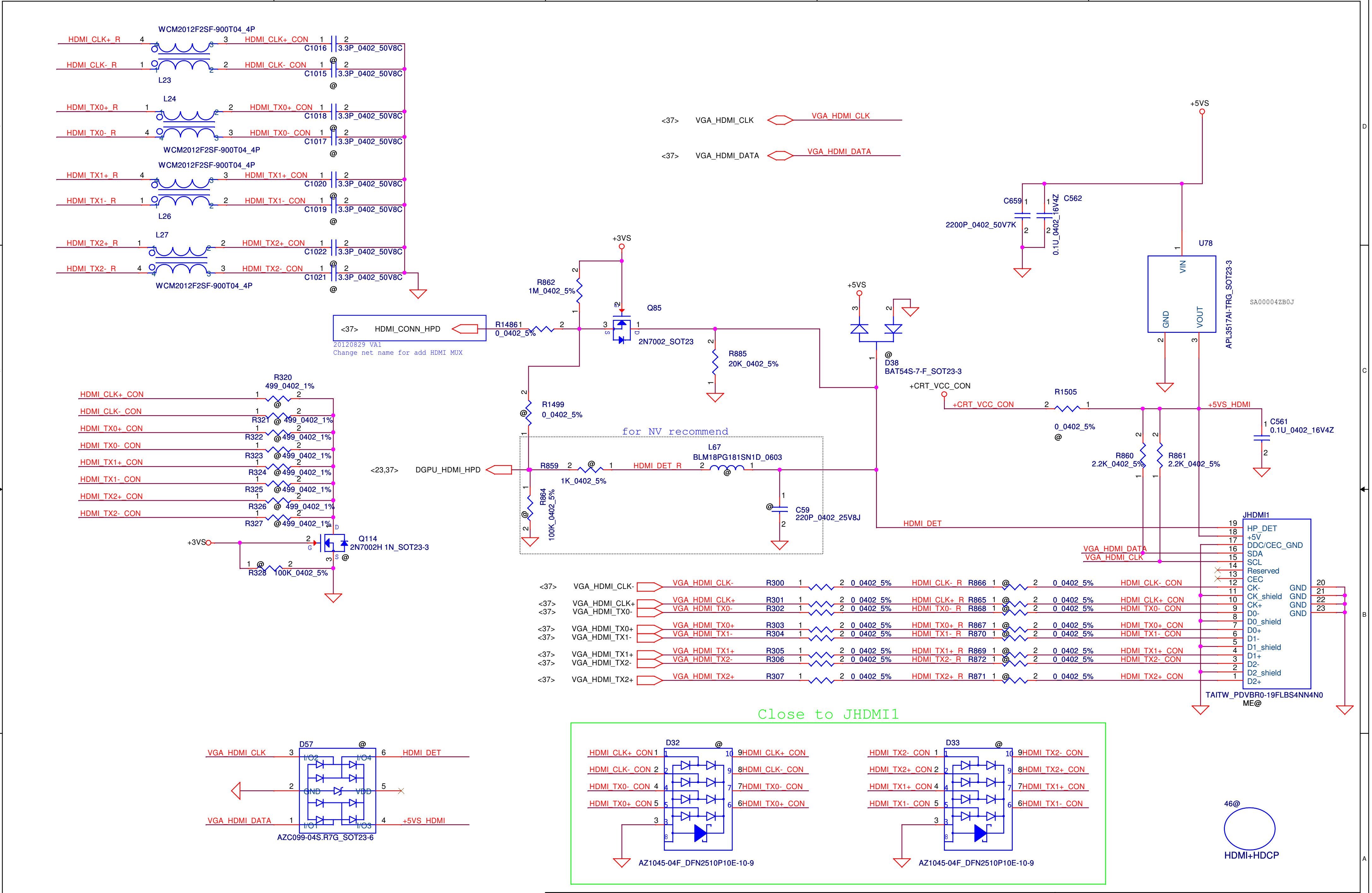

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Title
HDMI_CONN

LCFC

Size: Custom
Document Number: **Y501 NM-A032**
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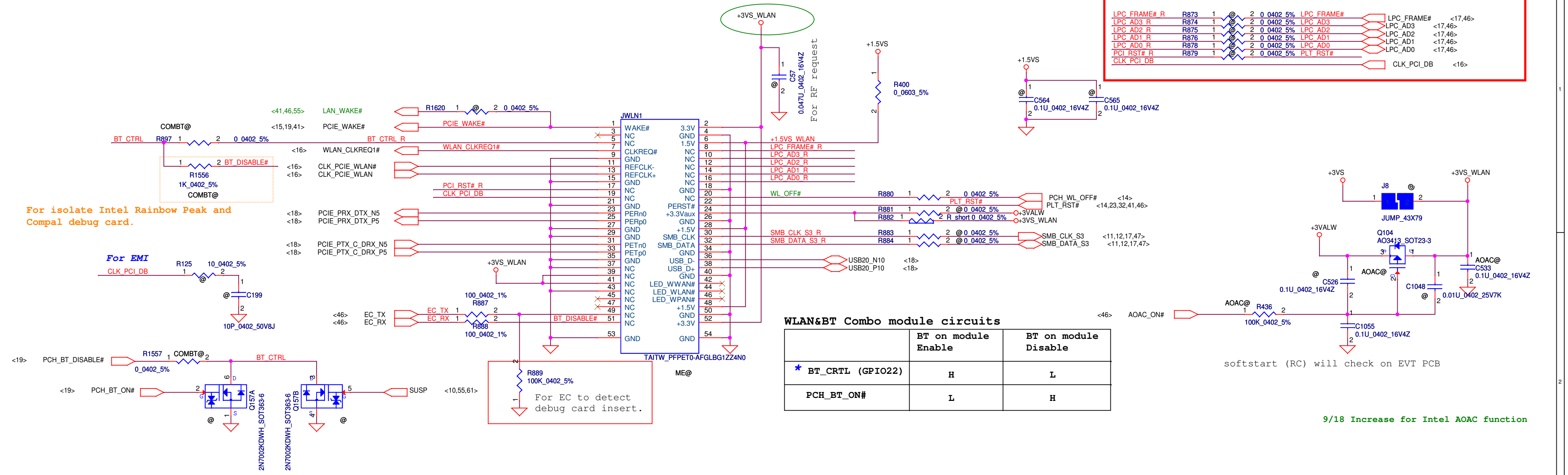
Mini-Express Card(WLAN/WiMAX)


+3VS_WLAN
C57 0.047U_0402_16V4Z
+1.5VS
R400 0_0603_5%
+1.5VS
C564 0.1U_0402_16V4Z
C565 0.1U_0402_16V4Z
LPC_FRAME#_R R873 0_0402_5% LPC_FRAME# <17,46>
LPC_AD3_R R874 0_0402_5% LPC_AD3 <17,46>
LPC_AD2_R R875 0_0402_5% LPC_AD2 <17,46>
LPC_AD1_R R876 0_0402_5% LPC_AD1 <17,46>
LPC_AD0_R R878 0_0402_5% LPC_AD0 <17,46>
PCI_RST#_R R879 0_0402_5% PLT_RST#
CLK_PCI_DB CLK_PCI_DB <16>
<41,46,55> LAN_WAKE# R1620 0_0402_5%
<15,19,41> PCIE_WAKE#
COMBT@
BT_CTRL R897 0_0402_5% BT_CTRL_R
<16> WLAN_CLKREQ1#
R1556 1K_0402_5% BT_DISABLE#
COMBT@
<16> CLK_PCIE_WLAN#
<16> CLK_PCIE_WLAN
PCI_RST#_R
CLK_PCI_DB
<18> PCIE_PRX_DTX_N5
<18> PCIE_PRX_DTX_P5
<18> PCIE_PTX_C_DRX_N5
<18> PCIE_PTX_C_DRX_P5
JWLN1
WAKE# NC NC CLKREQ# GND REFCLK- REFCLK+ GND NC NC GND PERn0 PERp0 GND GND PETn0 PETp0 GND NC NC NC NC NC NC NC NC NC GND
3.3V GND 1.5V NC NC NC NC NC GND NC PERST# +3.3Vaux GND +1.5V SMB_CLK SMB_DATA GND USB_D- USB_D+ GND LED_WWAN# LED_WLAN# LED_WPAN# +1.5V GND +3.3V GND
TAITW_PFPET0-AFGLBG1ZZ4N0
ME@
+1.5VS_WLAN
LPC_FRAME#_R LPC_AD3_R LPC_AD2_R LPC_AD1_R LPC_AD0_R
WL_OFF# R880 0_0402_5% PCH_WL_OFF# <14>
PLT_RST# PLT_RST# <14,23,32,41,46>
R881 0_0402_5% +3VALW
R882 R_short 0_0402_5% +3VS_WLAN
SMB_CLK_S3_R R883 0_0402_5% SMB_CLK_S3 <11,12,17,47>
SMB_DATA_S3_R R884 0_0402_5% SMB_DATA_S3 <11,12,17,47>
USB20_N10 <18>
USB20_P10 <18>
For EMI
CLK_PCI_DB R125 10_0402_5%
C199 10P_0402_50V8J
+3VS_WLAN
100_0402_1% R887
<46> EC_TX
<46> EC_RX
R888 100_0402_1%
BT_DISABLE#
<19> PCH_BT_DISABLE# R1557 0_0402_5% COMBT@ BT_CTRL
<19> PCH_BT_ON#
Q157A 2N7002KDWH_SOT363-6
Q157B 2N7002KDWH_SOT363-6
SUSP <10,55,61>
R889 100K_0402_5%
+3VS J8 JUMP_43X79 +3VS_WLAN
+3VALW
Q104 AO3413_SOT23-3
AOAC@
C526 0.1U_0402_16V4Z
C533 0.1U_0402_16V4Z
C1048 0.01U_0402_25V7K
<46> AOAC_ON# R436 100K_0402_5%
C1055 0.1U_0402_16V4Z

9/18 JP1 Pin2,24,52 contact to +3VS_WLAN for AOAC function

For RF request

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

For isolate Intel Rainbow Peak and Compal debug card.

For EC to detect debug card insert.

softstart (RC) will check on EVT PCB

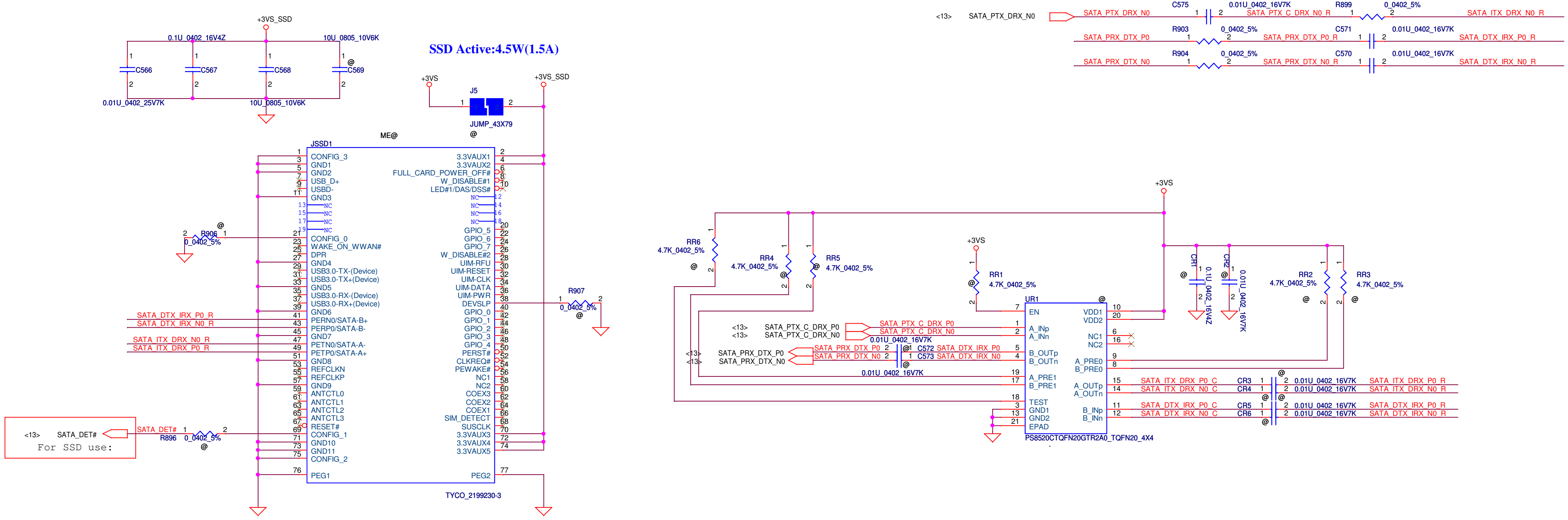
9/18 Increase for Intel AOAC function

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
* BT_CRTL (GPIO22)	H	L
PCH_BT_ON#	L	H

NGFF(SSD)

SSD Active:4.5W(1.5A)


+3VS_SSD
C566 C567 C568 C569
0.1U_0402_16V4Z 10U_0805_10V6K
0.01U_0402_25V7K 10U_0805_10V6K
+3VS J5 JUMP_43X79 +3VS_SSD
ME@
JSSD1
CONFIG_3 GND1 GND2 USB_D+ USBD- GND3 CONFIG_0 WAKE_ON_WWAN# DPR GND4 USB3.0-TX-(Device) USB3.0-TX+(Device) GND5 USB3.0-RX-(Device) USB3.0-RX+(Device) GND6 PERN0/SATA-B+ PERP0/SATA-B- GND7 PETN0/SATA-A- PETP0/SATA-A+ GND8 REFCLKN REFCLKP GND9 ANTCTL0 ANTCTL1 ANTCTL2 ANTCTL3 RESET# CONFIG_1 GND10 GND11 CONFIG_2 PEG1
3.3VAUX1 3.3VAUX2 FULL_CARD_POWER_OFF# W_DISABLE#1 LED#1/DAS/DSS# GPIO_5 GPIO_6 GPIO_7 W_DISABLE#2 UIM-RFU UIM-RESET UIM-CLK UIM-DATA UIM-PWR DEVSLP GPIO_0 GPIO_1 GPIO_2 GPIO_3 GPIO_4 PERST# CLKREQ# PEWAKE# NC1 NC2 COEX3 COEX2 COEX1 SIM_DETECT SUSCLK 3.3VAUX3 3.3VAUX4 3.3VAUX5 PEG2
TYCO_2199230-3
R906 0_0402_5%
R907 0_0402_5%
SATA_DTX_IRX_P0_R SATA_DTX_IRX_N0_R SATA_ITX_DRX_N0_R SATA_ITX_DRX_P0_R
<13> SATA_DET# SATA_DET# R896 0_0402_5%
<13> SATA_PTX_DRX_P0 SATA_PTX_DRX_P0 C574 0.01U_0402_16V7K SATA_PTX_C_DRX_P0_R R898 0_0402_5% SATA_ITX_DRX_P0_R
<13> SATA_PTX_DRX_N0 SATA_PTX_DRX_N0 C575 0.01U_0402_16V7K SATA_PTX_C_DRX_N0_R R899 0_0402_5% SATA_ITX_DRX_N0_R
SATA_PRX_DTX_P0 R903 0_0402_5% SATA_PRX_DTX_P0_R C571 0.01U_0402_16V7K SATA_DTX_IRX_P0_R
SATA_PRX_DTX_N0 R904 0_0402_5% SATA_PRX_DTX_N0_R C570 0.01U_0402_16V7K SATA_DTX_IRX_N0_R
+3VS
RR6 4.7K_0402_5% RR4 4.7K_0402_5% RR5 4.7K_0402_5%
RR1 4.7K_0402_5% RR2 4.7K_0402_5% RR3 4.7K_0402_5%
CR1 CR2 0.1U_0402_16V4Z 0.01U_0402_16V7K
UR1 EN A_INp A_INn B_OUTp B_OUTn A_PRE1 B_PRE1 TEST GND1 GND2 EPAD VDD1 VDD2 NC1 NC2 A_PRE0 B_PRE0 A_OUTp A_OUTn B_INp B_INn
PS8520CTQFN20GTR2A0_TQFN20_4X4
<13> SATA_PTX_C_DRX_P0 <13> SATA_PTX_C_DRX_N0
<13> SATA_PRX_DTX_P0 <13> SATA_PRX_DTX_N0
C572 C573 0.01U_0402_16V7K
CR3 CR4 CR5 CR6 0.01U_0402_16V7K
SATA_ITX_DRX_P0_C SATA_ITX_DRX_N0_C SATA_DTX_IRX_P0_C SATA_DTX_IRX_N0_C

For SSD use:

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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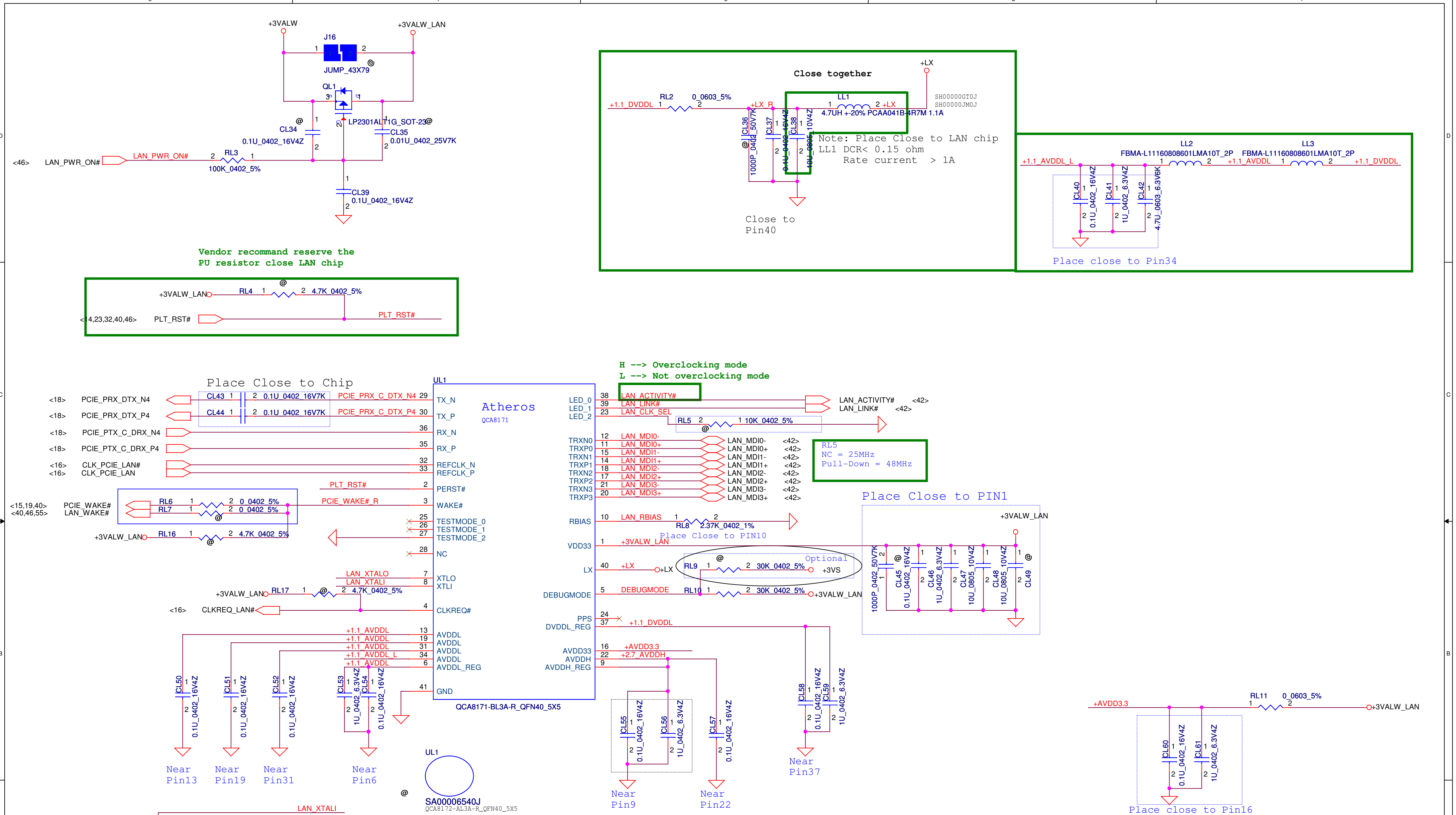
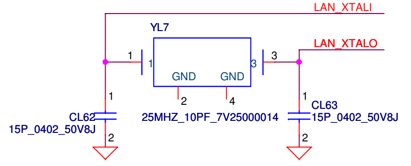
Title: **Mini-Card**

LCFC

Size	Document Number	Rev
C	Y501 NM-A032	1.0

Date: Wednesday, March 27, 2013 Sheet 40 of 69



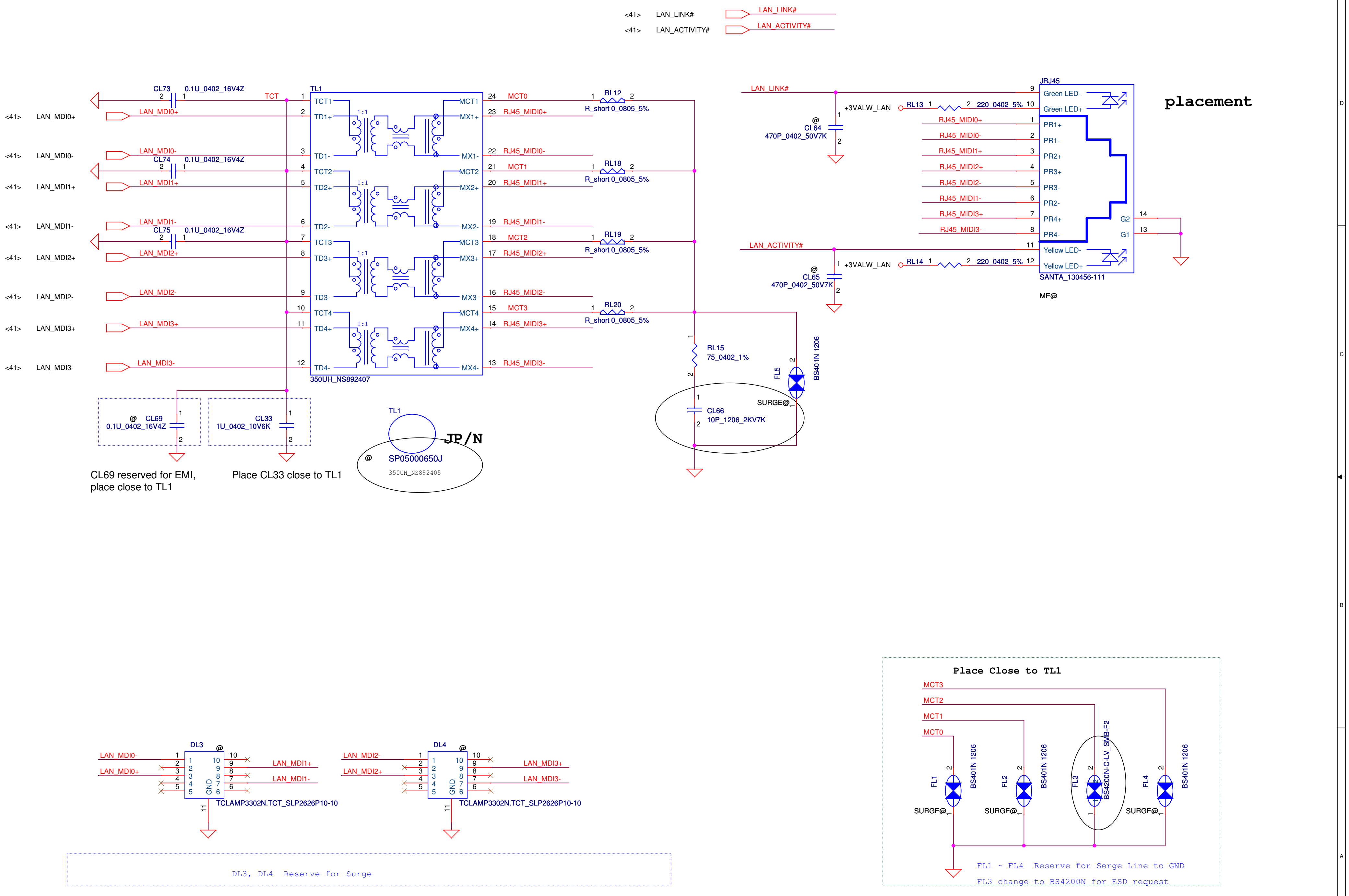


QCA8171/72 Pin defination difference.

	Pin17	Pin18	Pin19	Pin20	Pin21
QCA8171	LAN_MDI2+	LAN_MDI2-	+1.1_AVDDL	LAN_MDI3+	LAN_MDI3-
QCA8172	NC	NC	NC	NC	NC

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
LAN_QCA8171
LCFC
Size Custom
Document Number Y501 NM-A032
Rev 1.0
Date: Wednesday, March 27, 2013
Sheet 41 of 69



placement

JP/N

CL69 reserved for EMI,
place close to TL1

Place CL33 close to TL1

Place Close to TL1

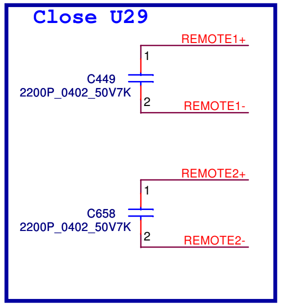
FL1 ~ FL4 Reserve for Serge Line to GND
FL3 change to BS4200N for ESD request

DL3, DL4 Reserve for Surge

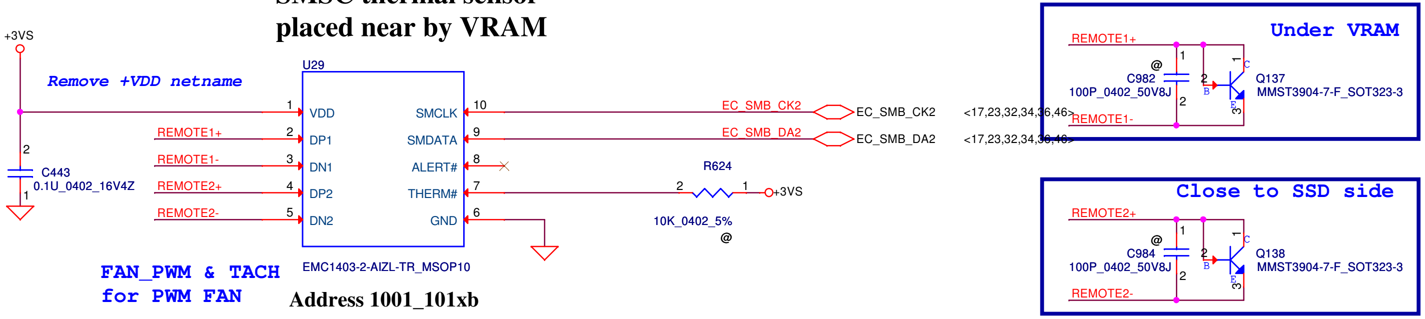
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
LAN Transformer

Size: Custom
Document Number: Y501 NM-A032
Rev: 1.0
Date: Wednesday, March 27, 2013



SMSC thermal sensor placed near by VRAM



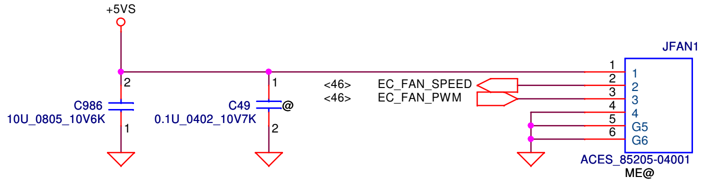
FAN_PWM & TACH
for PWM FAN

Address 1001_101xb

internal pull up 1.2K to 1.5V
R for initial thermal
shutdown temp

REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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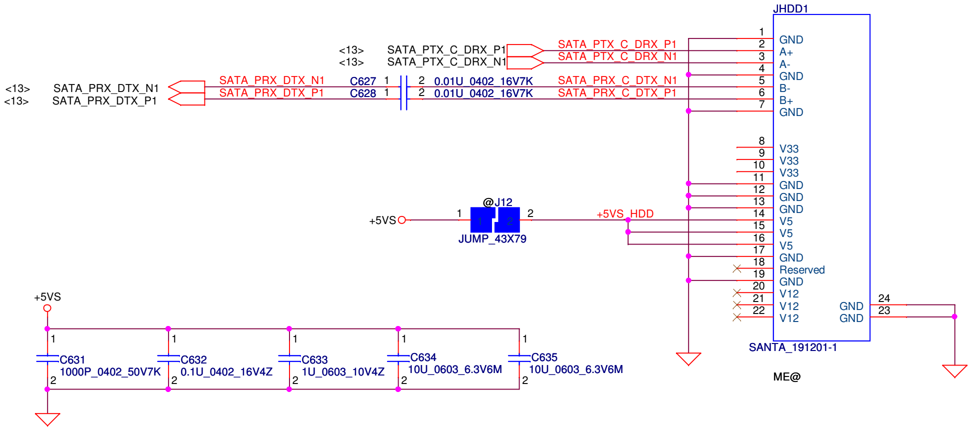
Title
VGA Thermal sensor/FAN CONN

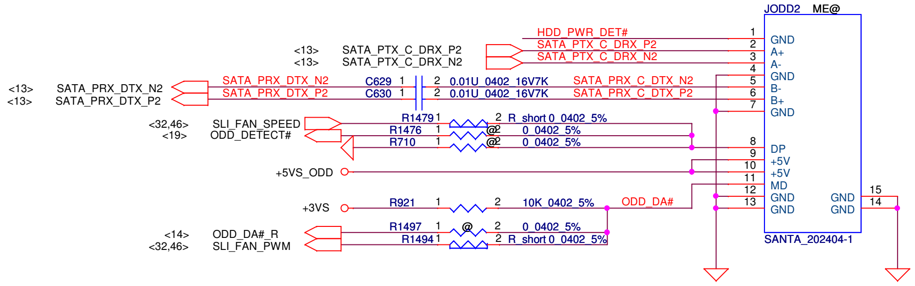
LCFC

Size: Custom
Document Number: *Y501 NM-A032*
Rev: 1.0
Date: Wednesday, March 27, 2013
Sheet 43 of 69

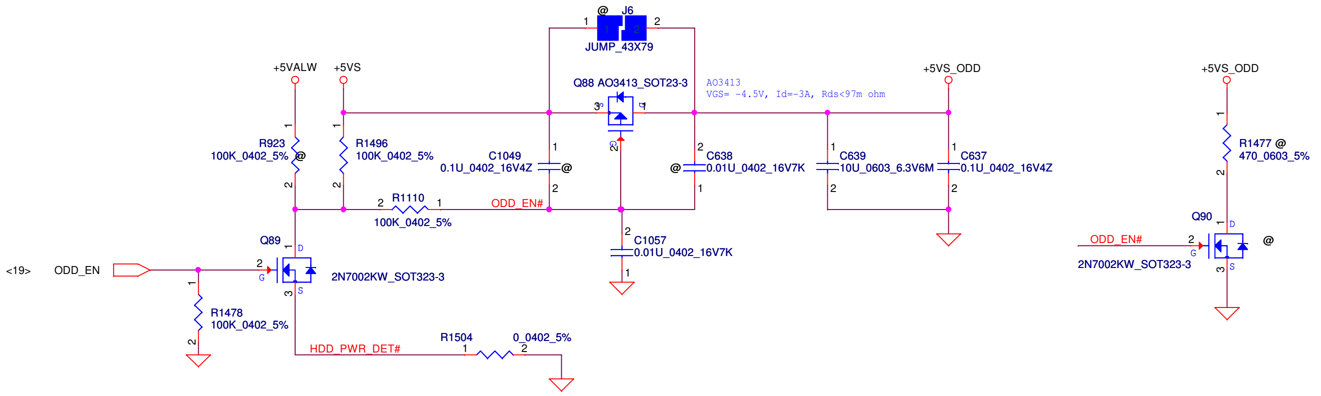
SATA HDD Conn.



SATA ODD Conn.



ODD Power Control



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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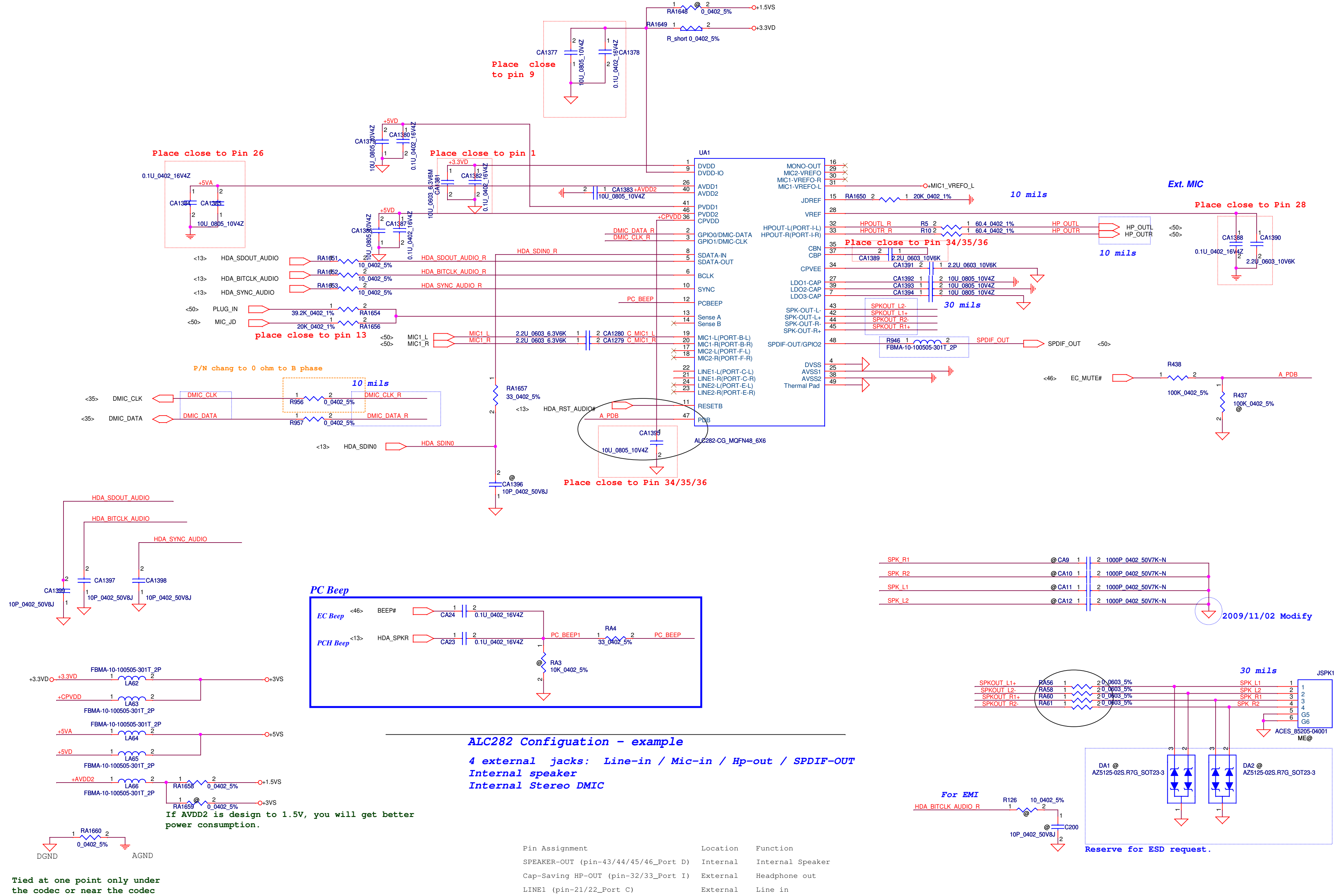
Title
HDD/ODD CONN

Size: Custom
Document Number: Y501 NM-A032
Rev: 1.0
Date: Wednesday, March 27, 2013
Sheet 44 of 69



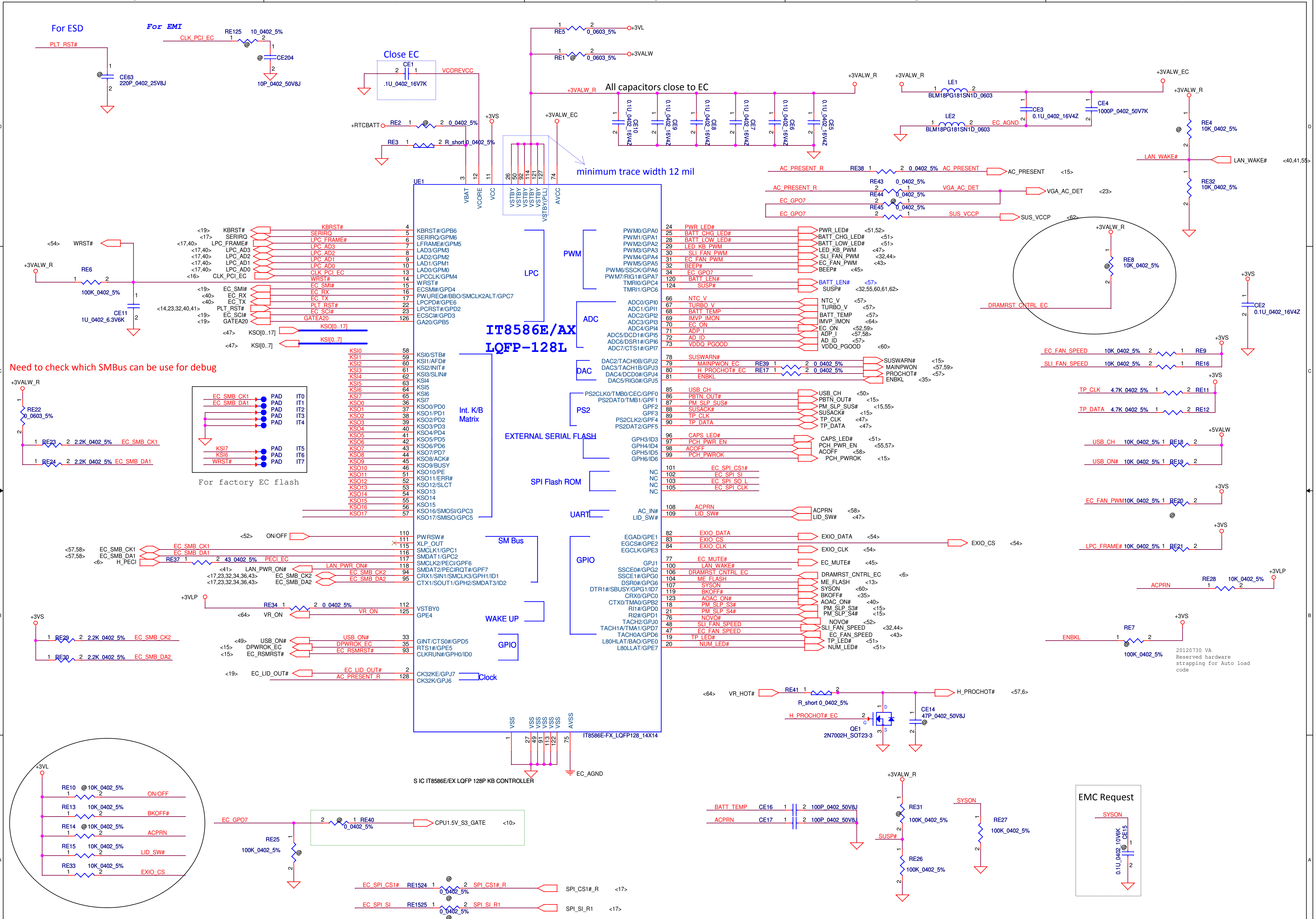
ALC282 Configuation – example

4 external jacks: Line-in / Mic-in / Hp-out / SPDIF-OUT
Internal speaker
Internal Stereo DMIC

Pin Assignment	Location	Function
SPEAKER-OUT (pin-43/44/45/46_Port D)	Internal	Internal Speaker
Cap-Saving HP-OUT (pin-32/33_Port I)	External	Headphone out
LINE1 (pin-21/22_Port C)	External	Line in
MIC1 (pin-19/20_Port B)	External	Mic in
MONO-OUT (pin-16)	NC	
MIC2 (pin-17/18_Port F)	NC	
DMIC1/2 (pin-2/3)	Internal	Internal Mic (Digital MIC)

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

Title
Audio Codec
LCFC
Size C
Document Number Y501 NM-A032
Rev 1.0
Date: Wednesday, March 27, 2013


For ESD
For EMI
PLT_RST#
CE63 220P_0402_25V8J
CLK_PCI_EC
RE125 10_0402_5%
CE204 10P_0402_50V8J
Close EC
CE1 .1U_0402_16V7K
VCOREVCC
RE5 0_0603_5% +3VL
RE1 0_0603_5% +3VALW
+3VALW_R
All capacitors close to EC
CE10 CE9 CE8 CE7 CE6 CE5 0.1U_0402_16V4Z
LE1 BLM18PG181SN1D_0603
LE2 BLM18PG181SN1D_0603
CE3 0.1U_0402_16V4Z
CE4 1000P_0402_50V7K
EC_AGND
+3VALW_EC
RE4 10K_0402_5%
LAN_WAKE#
LAN_WAKE# <40,41,55>
+RTCBATT
RE2 0_0402_5%
RE3 R_short 0_0402_5%
+3VS
minimum trace width 12 mil
AC_PRESENT_R
RE38 0_0402_5%
AC_PRESENT <15>
RE43 0_0402_5%
RE44 0_0402_5%
VGA_AC_DET <23>
EC_GPO7
RE45 0_0402_5%
SUS_VCCP <62>
RE32 10K_0402_5%
UE1
VBAT VCORE VCC VSTBY VSTBY VSTBY VSTBY VSTBY VSTBY(PLL) AVCC
IT8586E/AX
LQFP-128L
LPC
PWM
ADC
DAC
PS2
Int. K/B Matrix
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
SM Bus
GPIO
WAKE UP
Clock
KBRST#/GPB6 SERIRQ/GPM6 LFRAME#/GPM5 LAD3/GPM3 LAD2/GPM2 LAD1/GPM1 LAD0/GPM0 LPCCLK/GPM4 WRST# ECSMI#/GPD4 PWUREQ#/BBO/SMCLK2ALT/GPC7 LPCPD#/GPE6 LPCRST#/GPD2 ECSCI#/GPD3 GA20/GPB5
KSI0/STB# KSI1/AFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7 KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15 KSO16/SMOSI/GPC3 KSO17/SMISO/GPC5
PWRSW# XLP_OUT SMCLK1/GPC1 SMDAT1/GPC2 SMCLK2/PECI/GPF6 SMDAT2/PECIRQT#/GPF7 CRX1/SIN1/SMCLK3/GPH1/ID1 CTX1/SOUT1/GPH2/SMDAT3/ID2
VSTBY0 GPE4
GINT/CTS0#/GPD5 RTS1#/GPE5 CLKRUN#/GPH0/ID0
CK32KE/GPJ7 CK32K/GPJ6
PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/SSCK/GPA6 PWM7/RIG1#/GPA7 TMRI0/GPC4 TMRI1/GPC6
ADC0/GPI0 ADC1/GPI1 ADC2/GPI2 ADC3/GPI3 ADC4/GPI4 ADC5/DCD1#/GPI5 ADC6/DSR1#/GPI6 ADC7/CTS1#/GPI7
DAC2/TACH0B/GPJ2 DAC3/TACH1B/GPJ3 DAC4/DCD0#/GPJ4 DAC5/RIG0#/GPJ5
PS2CLK0/TMB0/CEC/GPF0 PS2DAT0/TMB1/GPF1 GPF2 GPF3 PS2CLK2/GPF4 PS2DAT2/GPF5
GPH3/ID3 GPH4/ID4 GPH5/ID5 GPH6/ID6
NC NC NC NC
AC_IN# LID_SW#
EGAD/GPE1 EGCS#/GPE2 EGCLK/GPE3 GPJ1 SSCE0#/GPG2 SSCE1#/GPG0 DSR0#/GPG6 DTR1#/SBUSY/GPG1/ID7 CRX0/GPC0 CTX0/TMA0/GPB2 RI1#/GPD0 RI2#/GPD1 TACH2/GPJ0 TACH1A/TMA1/GPD7 TACH0A/GPD6 L80HLAT/BAO/GPE0 L80LLAT/GPE7
VSS VSS VSS VSS VSS VSS AVSS
IT8586E-FX_LQFP128_14X14
S IC IT8586E/EX LQFP 128P KB CONTROLLER
EC_AGND
KBRST# SERIRQ LPC_FRAME# LPC_AD3 LPC_AD2 LPC_AD1 LPC_AD0 CLK_PCI_EC WRST# EC_SMI# EC_RX EC_TX PLT_RST# EC_SCI# GATEA20
<54> WRST#
+3VALW_R RE6 100K_0402_5%
CE11 1U_0402_6.3V6K
KSO[0..17] KSI[0..7]
Need to check which SMBus can be use for debug
RE22 0_0603_5%
RE23 2.2K_0402_5% EC_SMB_CK1
RE24 2.2K_0402_5% EC_SMB_DA1
EC_SMB_CK1 EC_SMB_DA1 PAD IT0 IT1 IT2 IT3 IT4
KSI7 KSI6 WRST# PAD IT5 IT6 IT7
For factory EC flash
<52> ON/OFF
<57,58> EC_SMB_CK1 <57,58> EC_SMB_DA1 <6> H_PECI
RE37 43_0402_5% PECI_EC
<41> LAN_PWR_ON#
EC_SMB_CK2 EC_SMB_DA2
+3VLP RE34 0_0402_5% VR_ON
+3VS RE29 2.2K_0402_5% EC_SMB_CK2
RE30 2.2K_0402_5% EC_SMB_DA2
<49> USB_ON# <15> DPWROK_EC <15> EC_RSMRST#
<19> EC_LID_OUT# AC_PRESENT_R
PWR_LED# BATT_CHG_LED# BATT_LOW_LED# LED_KB_PWM SLI_FAN_PWM EC_FAN_PWM BEEP# EC_GPO7 BATT_LEN# SUSP#
NTC_V TURBO_V BATT_TEMP IMVP_IMON EC_ON ADP_I AD_ID VDDQ_PGOOD
SUSWARN# MAINPWON_EC H_PROCHOT#_EC ENBKL
RE39 0_0402_5% RE17 0_0402_5%
SUSWARN# <15> MAINPWON <57,59> PROCHOT# <57> ENBKL <35>
USB_CH PBTN_OUT# PM_SLP_SUS# SUSACK# TP_CLK TP_DATA
CAPS_LED# PCH_PWR_EN ACOFF PCH_PWROK
EC_SPI_CS1# EC_SPI_SI EC_SPI_SO_L EC_SPI_CLK
ACPRN LID_SW#
EXIO_DATA EXIO_CS EXIO_CLK EC_MUTE# LAN_WAKE# DRAMRST_CNTRL_EC ME_FLASH SYSON BKOFF# AOAC_ON# PM_SLP_S3# PM_SLP_S4# NOVO# SLI_FAN_SPEED EC_FAN_SPEED TP_LED# NUM_LED#
+3VALW_R RE8 10K_0402_5%
DRAMRST_CNTRL_EC
CE2 0.1U_0402_16V4Z
EC_FAN_SPEED 10K_0402_5% RE9
SLI_FAN_SPEED 10K_0402_5% RE16
TP_CLK 4.7K_0402_5% RE11
TP_DATA 4.7K_0402_5% RE12
+5VALW
USB_CH 10K_0402_5% RE18
USB_ON# 10K_0402_5% RE19
EC_FAN_PWM 10K_0402_5% RE20
LPC_FRAME# 10K_0402_5% RE21
+3VLP RE28 10K_0402_5% ACPRN
ENBKL RE7 100K_0402_5%
20120730 VA Reserved hardware strapping for Auto load code
<64> VR_HOT#
RE41 R_short 0_0402_5%
H_PROCHOT# <57,6>
H_PROCHOT#_EC
QE1 2N7002H_SOT23-3
CE14 47P_0402_50V8J
+3VL
RE10 10K_0402_5% ON/OFF
RE13 10K_0402_5% BKOFF#
RE14 10K_0402_5% ACPRN
RE15 10K_0402_5% LID_SW#
RE33 10K_0402_5% EXIO_CS
EC_GPO7 RE40 0_0402_5% CPU1.5V_S3_GATE <10>
RE25 100K_0402_5%
BATT_TEMP CE16 100P_0402_50V8J
ACPRN CE17 100P_0402_50V8J
+3VALW_R RE31 100K_0402_5%
SUSP#
RE26 100K_0402_5%
SYSON RE27 100K_0402_5%
EMC Request
SYSON CE15 0.1U_0402_10V6K
EC_SPI_CS1# RE1524 0_0402_5% SPI_CS1#_R SPI_CS1#_R <17>
EC_SPI_SI RE1525 0_0402_5% SPI_SI_R1 SPI_SI_R1 <17>
EC_SPI_SO_L RE1526 0_0402_5% SPI_SO_L1 SPI_SO_L1 <17>
EC_SPI_CLK RE1527 0_0402_5% SPI_CLK_PCH_1 SPI_CLK_PCH_1 <17>
5 4 3 2 1
D C B A

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Issued Date	2012/05/02	Deciphered Date	2012/5/02

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Title
EC ITE8586LQFP

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Size C
Document Number **Y501 NM-A032**
Rev 1.0

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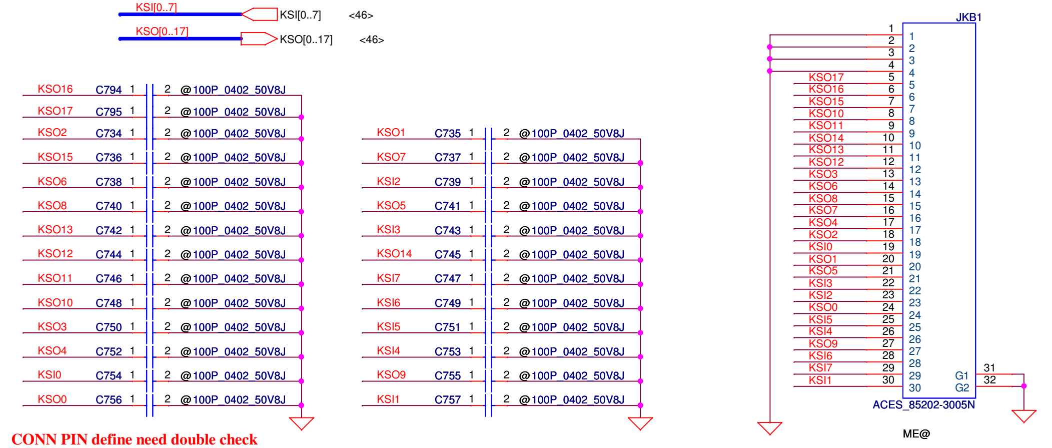
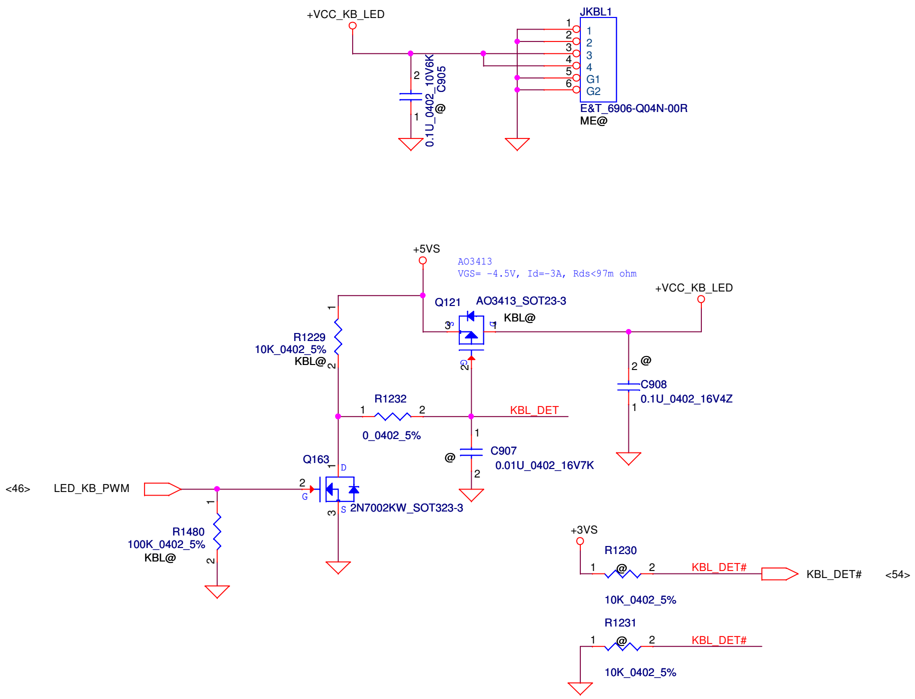
15" INT_KBD Conn.

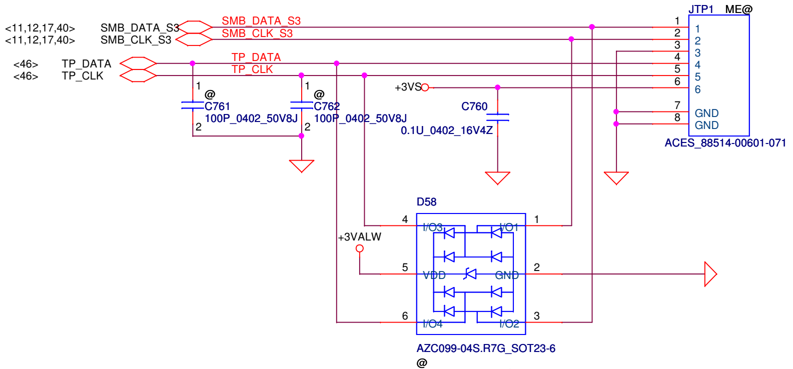

KSI[0..7]
KSI[0..7] <46>
KSO[0..17]
KSO[0..17] <46>
KSO16 C794 @100P_0402_50V8J
KSO17 C795 @100P_0402_50V8J
KSO2 C734 @100P_0402_50V8J
KSO15 C736 @100P_0402_50V8J
KSO6 C738 @100P_0402_50V8J
KSO8 C740 @100P_0402_50V8J
KSO13 C742 @100P_0402_50V8J
KSO12 C744 @100P_0402_50V8J
KSO11 C746 @100P_0402_50V8J
KSO10 C748 @100P_0402_50V8J
KSO3 C750 @100P_0402_50V8J
KSO4 C752 @100P_0402_50V8J
KSI0 C754 @100P_0402_50V8J
KSO0 C756 @100P_0402_50V8J
KSO1 C735 @100P_0402_50V8J
KSO7 C737 @100P_0402_50V8J
KSI2 C739 @100P_0402_50V8J
KSO5 C741 @100P_0402_50V8J
KSI3 C743 @100P_0402_50V8J
KSO14 C745 @100P_0402_50V8J
KSI7 C747 @100P_0402_50V8J
KSI6 C749 @100P_0402_50V8J
KSI5 C751 @100P_0402_50V8J
KSI4 C753 @100P_0402_50V8J
KSO9 C755 @100P_0402_50V8J
KSI1 C757 @100P_0402_50V8J
JKB1
KSO17 KSO16 KSO15 KSO10 KSO11 KSO14 KSO13 KSO12 KSO3 KSO6 KSO8 KSO7 KSO4 KSO2 KSI0 KSO1 KSO5 KSI3 KSI2 KSO0 KSI5 KSI4 KSO9 KSI6 KSI7 KSI1
G1 G2 31 32
ACES_85202-3005N
ME@

CONN PIN define need double check

KB Lighting CONN.4pin

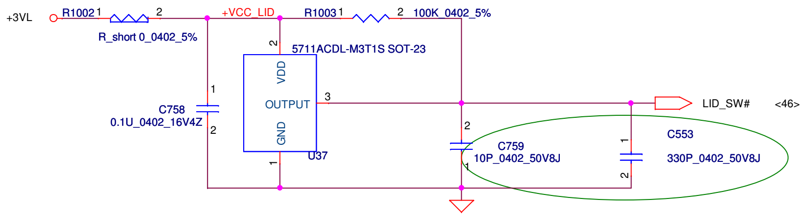


To TP/B Conn.



For ESD request

Lid Switch



For ESD Request

Security Classification	LC Future Center Secret Data			Title
Issued Date	2012/07/01	Deciphered Date	2014/07/01	KB/ KB-LIGHT/ LID IC

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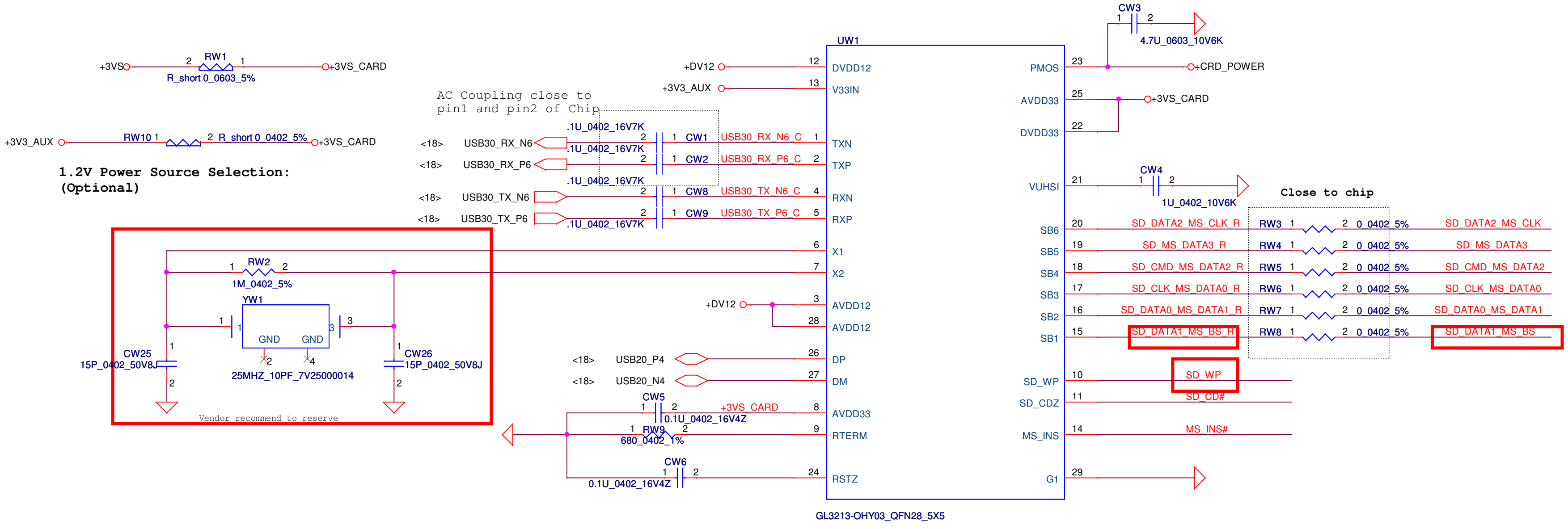
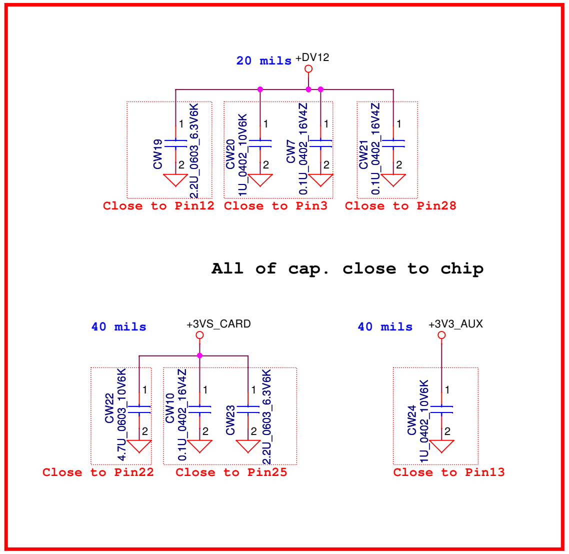
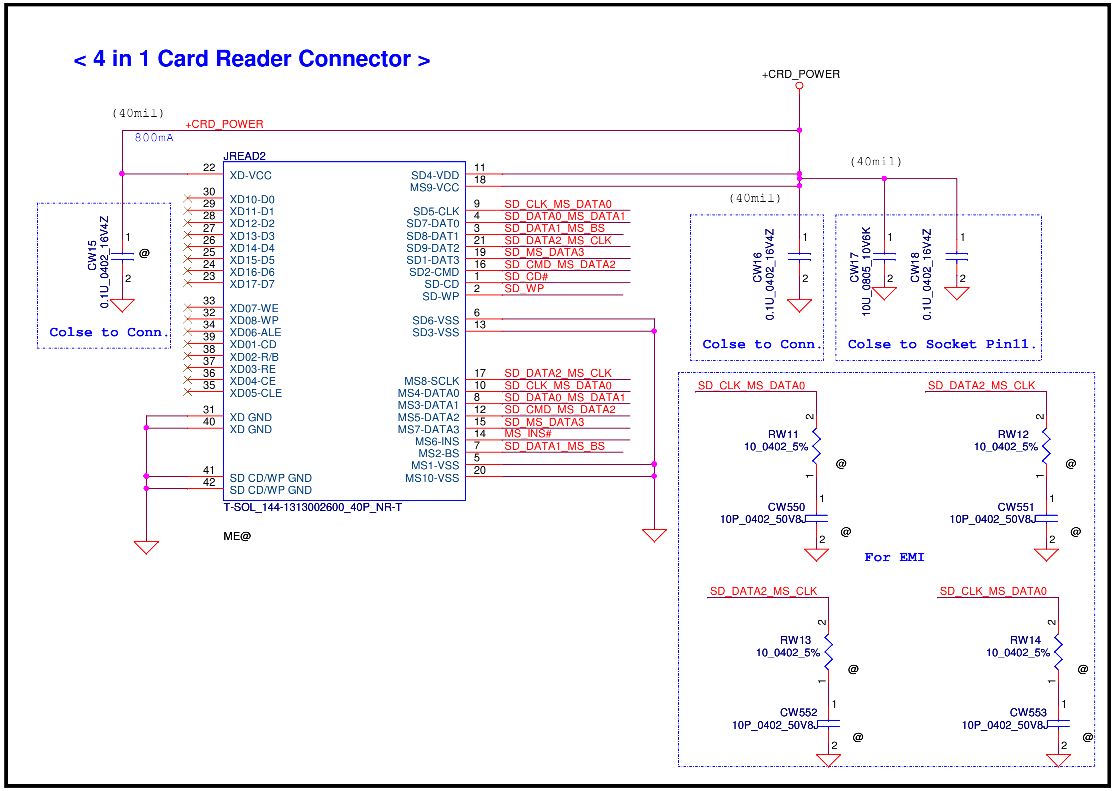
Date:	Wednesday, March 27, 2013	Sheet 47 of 69







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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
Card reader GL3213

LCFC

Size	Document Number	Rev
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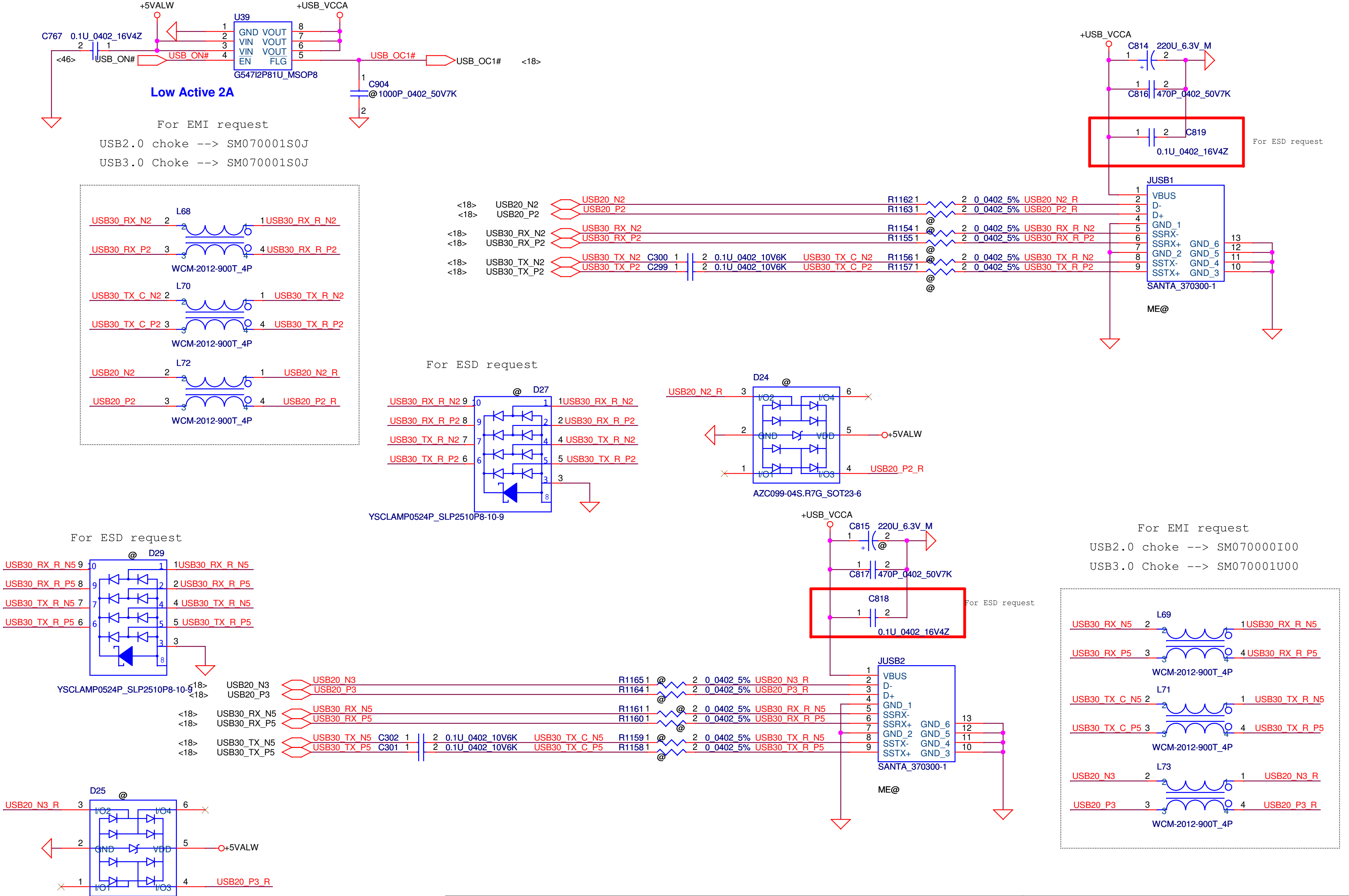
LEFT SIDE USB3.0 PORT X1



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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
USB 3.0 PORT (LEFT)

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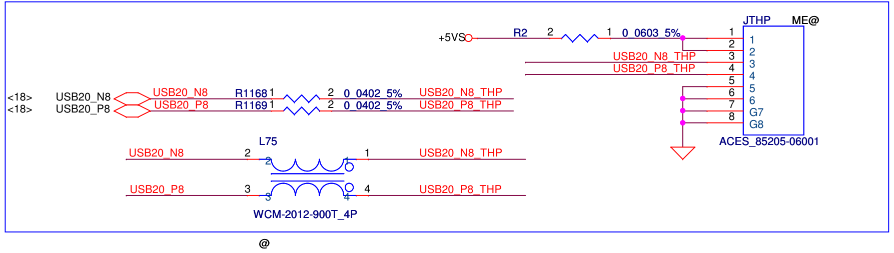
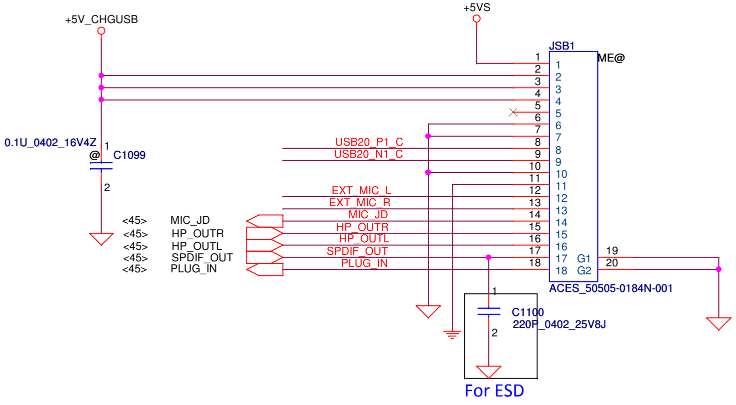
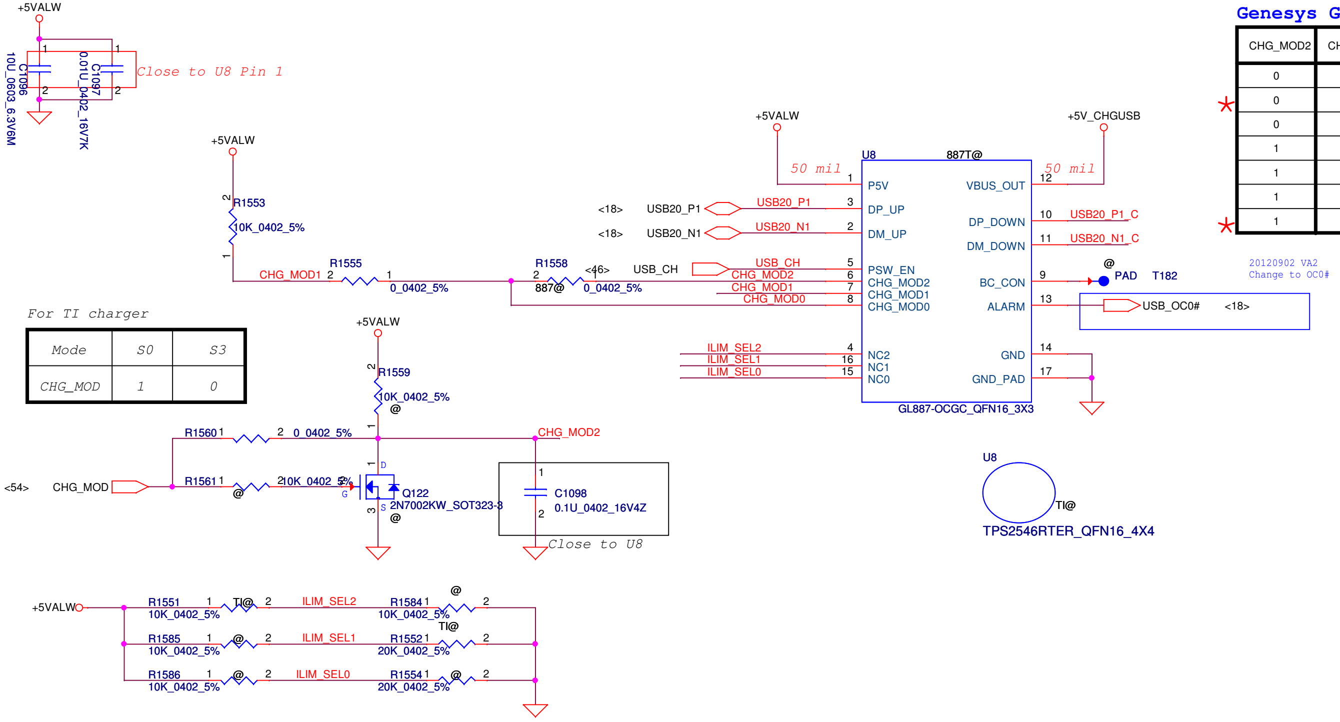
Touch panel





Sleep & Charge
Right side USB Charger Port (USB_Port5, near JMIC1)



For TI charger

Mode	*S0*	*S3*
CHG_MOD	*1*	*0*

Genesys GL887

	CHG_MOD2	CHG_MOD1	CHG_MOD0	Charge Mode
	0	0	0	Charge Disable
*	0	1	0	CDP mode
	0	1	1	DCP mode
	1	0	0	Apple 1A mode
	1	0	1	Apple 2A mode
	1	1	0	Auto mode (DCP and Apple 1A)
*	1	1	1	Auto mode (DCP and Apple 2A)

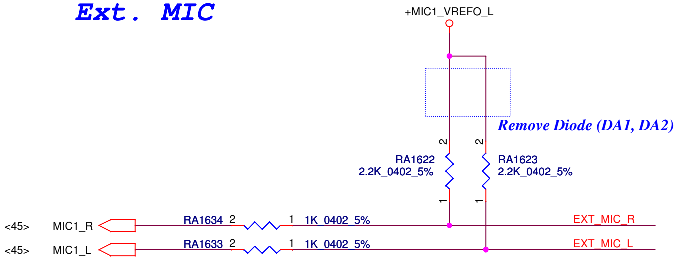
Genesys GL887T

	CHG_MOD2	CHG_MOD1	CHG_MOD0	Charge Mode
	0	0	0	Power down mode
	0	0	1	Auto 2A mode without wake up function
	X	1	0	BC1.2 SDP mode
*	0	1	1	Auto 2A mode with wake up function
	1	0	0	BC1.2 DCP mode
	1	0	1	Apple 2A mode
*	1	1	1	BC1.2 CDP mode with Smart CDP

TI TPS2543

	CHG_MOD2	CHG_MOD1	CHG_MOD0	ILIM_SEL2	MODE
	0	0	0	X	**DCH** OUT held low /Data lines disconnected
*	1	1	1	1	**CDP** Data connected and Load detect active
	1	1	1	0	**SDP2** Data connected
	1	1	0	X	**SDP1** Data connected
	0	1	0	X	**SDP1** Data connected
	1	0	0	X	**DCP_Short** Stay in DCP BC1.2 Charging mode
	1	0	1	X	**DCP_Divider** Stay in DCP Divider1 Charging mode
*	0	1	1	X	**DCP_Auto** Data disconnected and Load detect active
	0	0	1	X	**DCP_Auto** Data disconnected and Load detect active

Ext. MIC



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Title
AUDIO-B CONN/ USB CHARGER
LCFC
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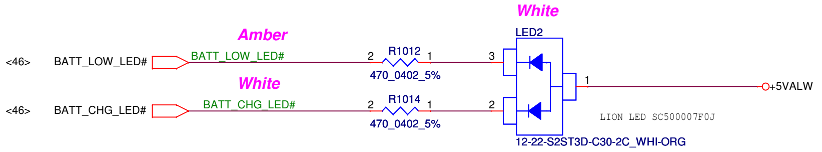
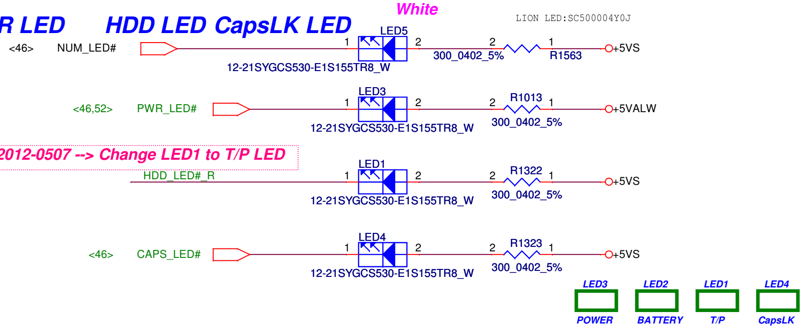
Date: Wednesday, March 27, 2013

BATT CHARGE/LOW LED

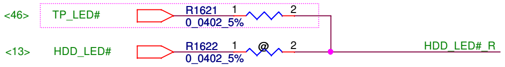


PWR LED

HDD LED CapsLK LED



TouchPad_LED



Screw Hole

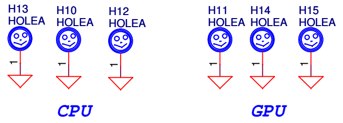
CPU and GPU: H_3P8X 6

MIN PCIE: H_3P3 X 1

C: H_3P8X 3

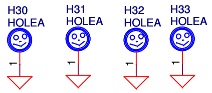
B: H_3P8X 3

E: H_3P3X 1



ME: H_8P0 X 8; H_3P3X 1; H_4P0X3P0N X 2; H_2P0X 1

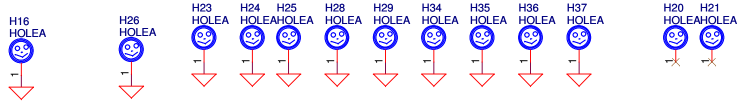
A: H_2P8X 8



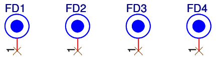
H_3P0X9

E: H_3P3X 3

H_2P8X4P0NX1



PCB Fedical Mark PAD



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Title
LED

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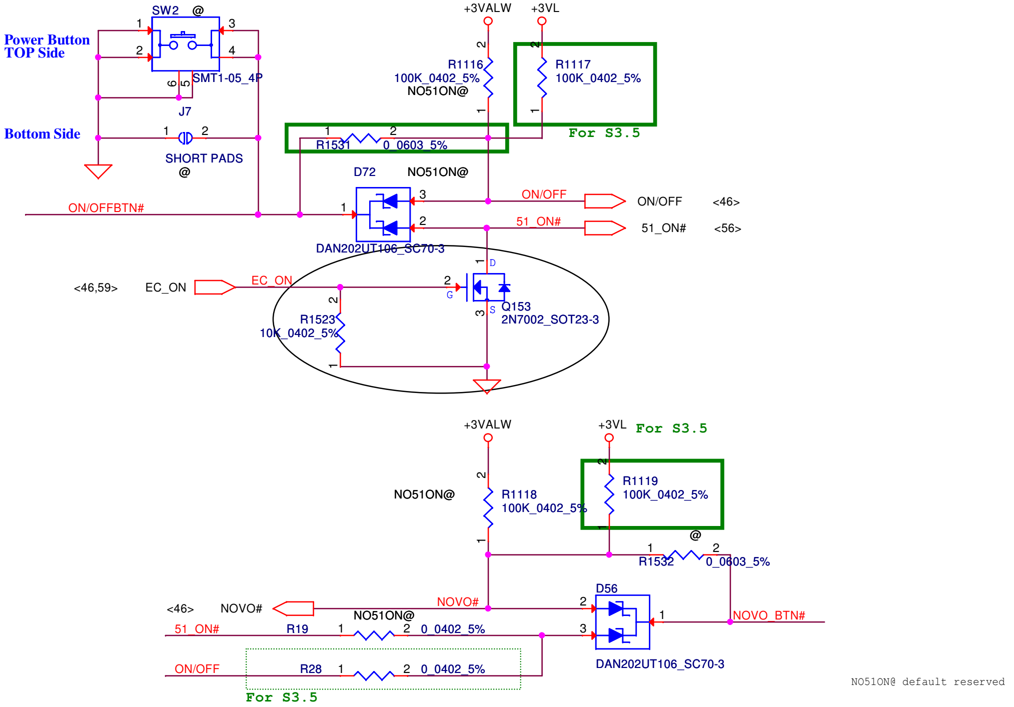
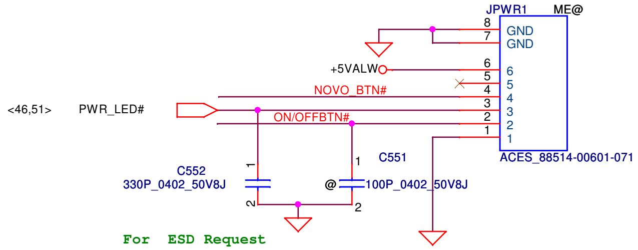
ON/OFF switch



Power Button/B link
to Function/B Conn. 10pin



EMI REQUEST 1ST = SCA00000E00

2ST = SCA00000R00

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
ONOFF SW/ PWR-B CONN/ ISPD

Size	Document Number	Rev
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Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Title

NVSR

Size	Document Number	Rev
C	***Y501 NM-A032***	1.0

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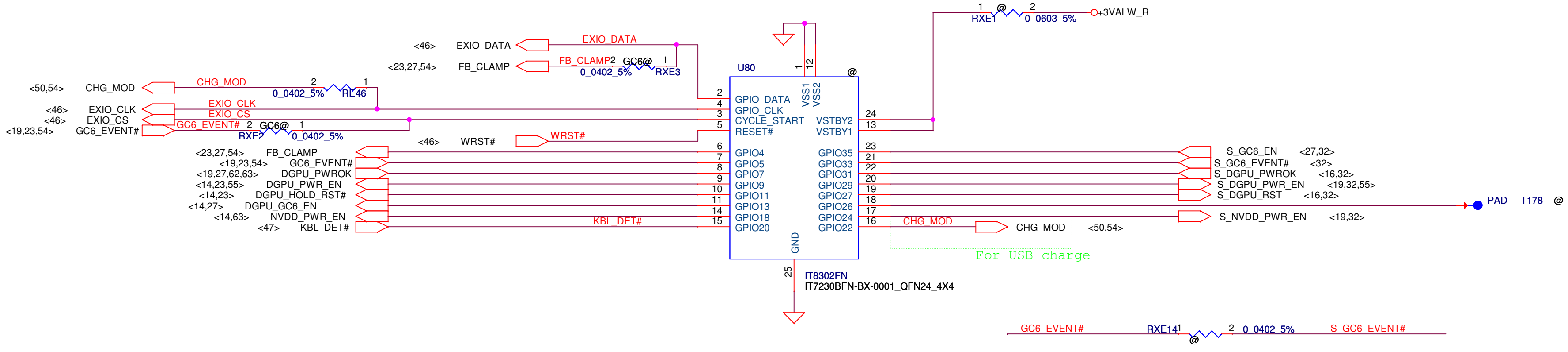

SLI_FB_Clamp
FB_clamp_req
GPU_PWR_GOOD
GPU_PWR_EN
PEX REST
DGPU_HOLD_RST#

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
EX IO

LCFC

Size: Custom
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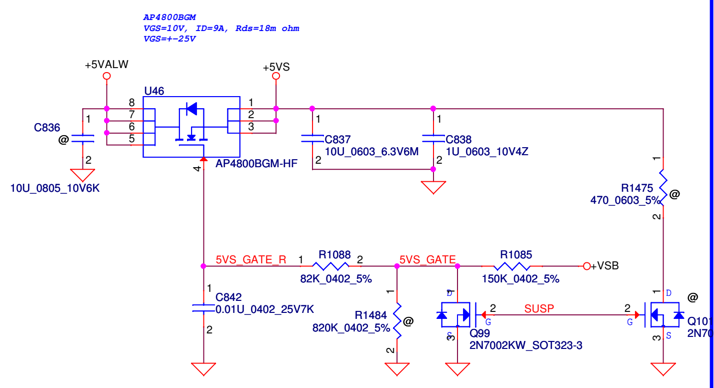
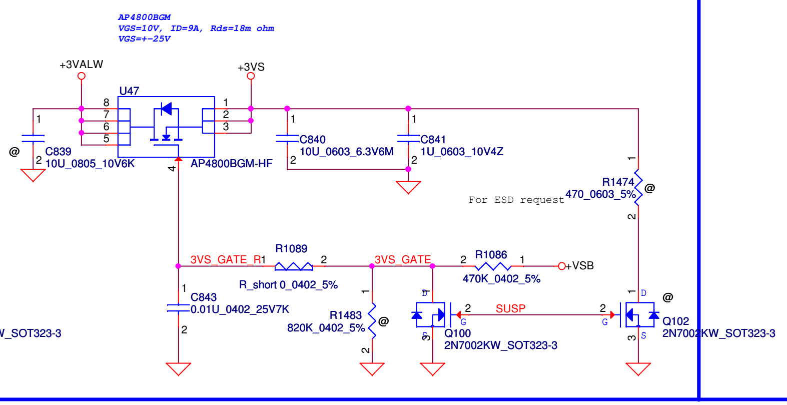
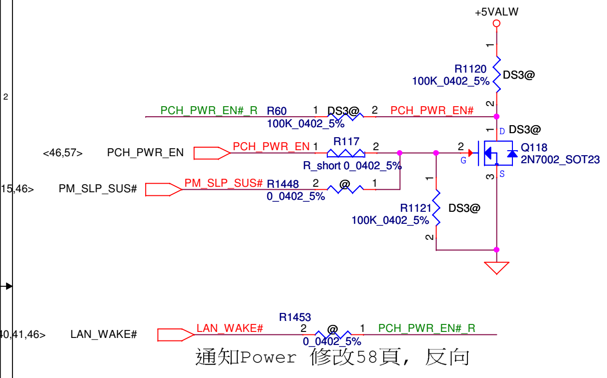
+5VALW to +5VS



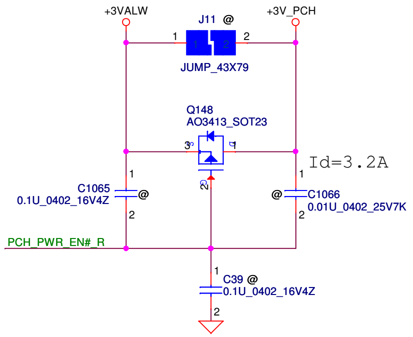
+3VALW to +3VS

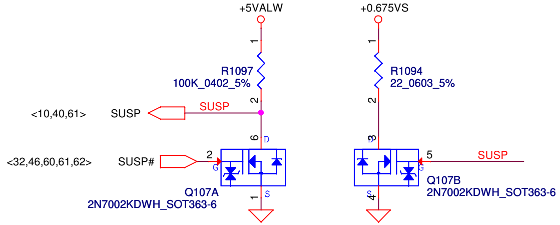


+3VALW to +3V_PCH

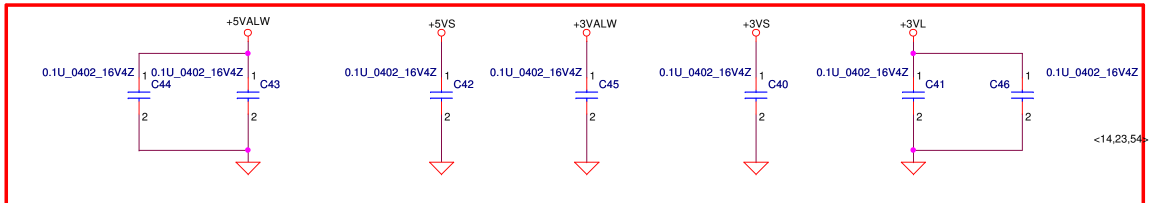


通知Power 修改58頁, 反向



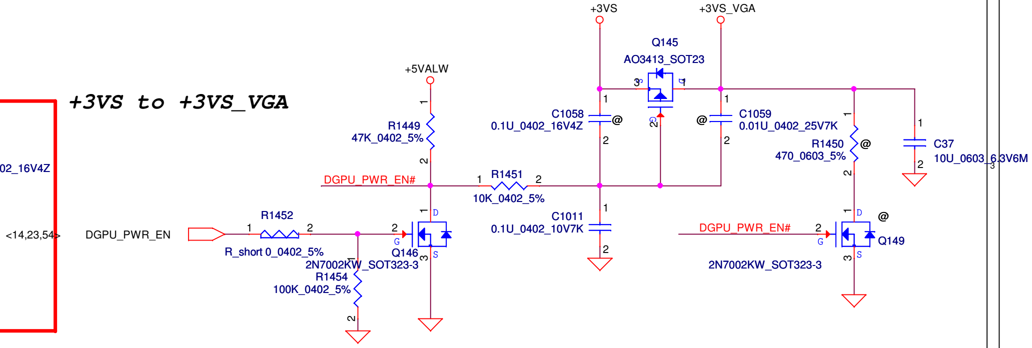


For Intel S3 Power Reduction.



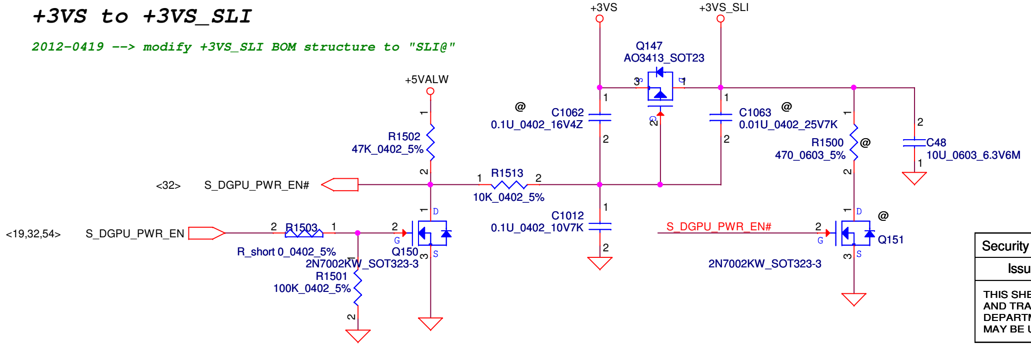
For ESD request

+3VS to +3VS_VGA



+3VS to +3VS_SLI

2012-0419 ---> modify +3VS_SLI BOM structure to "SLI@"



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Title
DC V TO VS INTERFACE

LCFC

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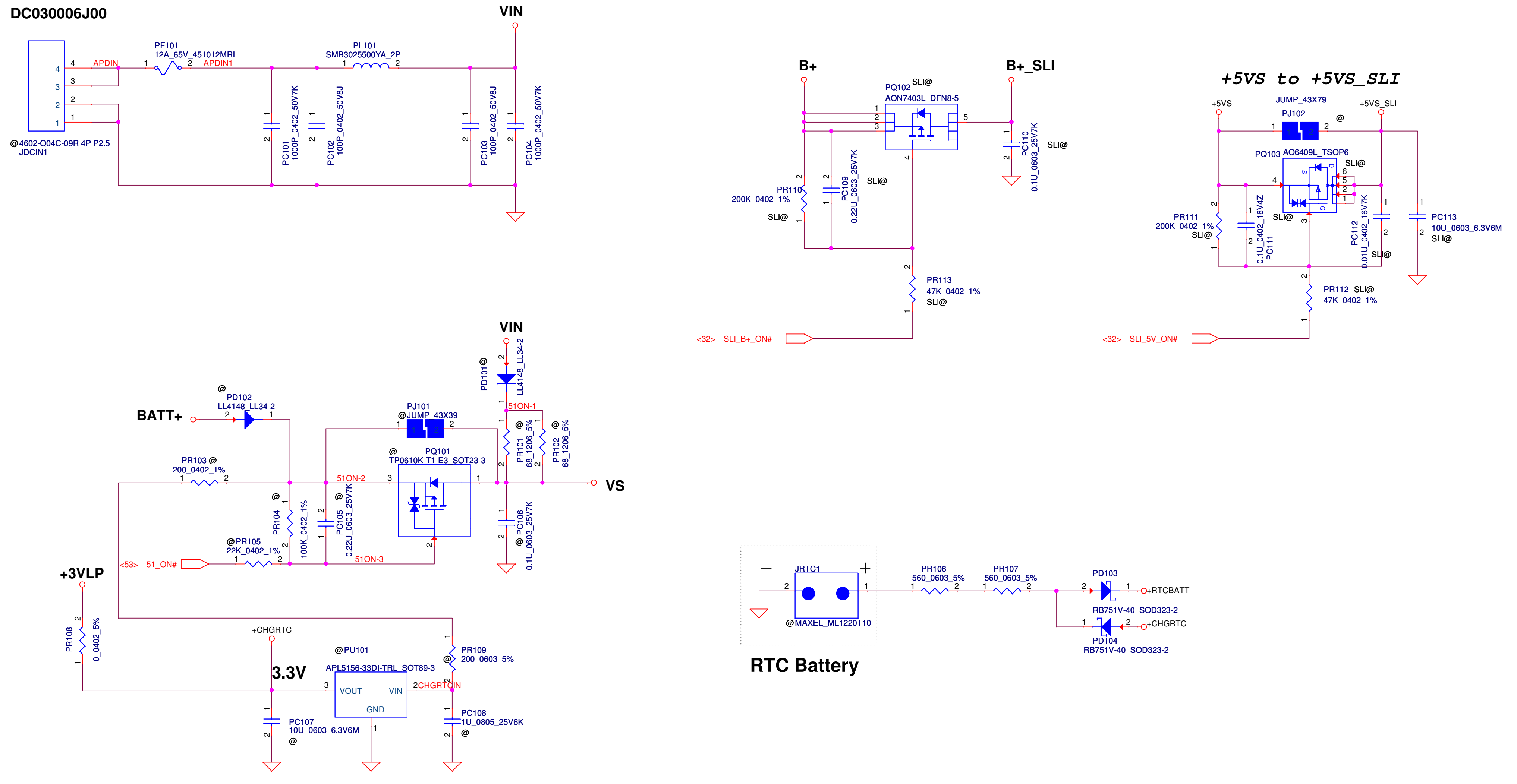

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Title
Vin Detector

LCFC

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Custom	*Y510 NM-A032*	1.0

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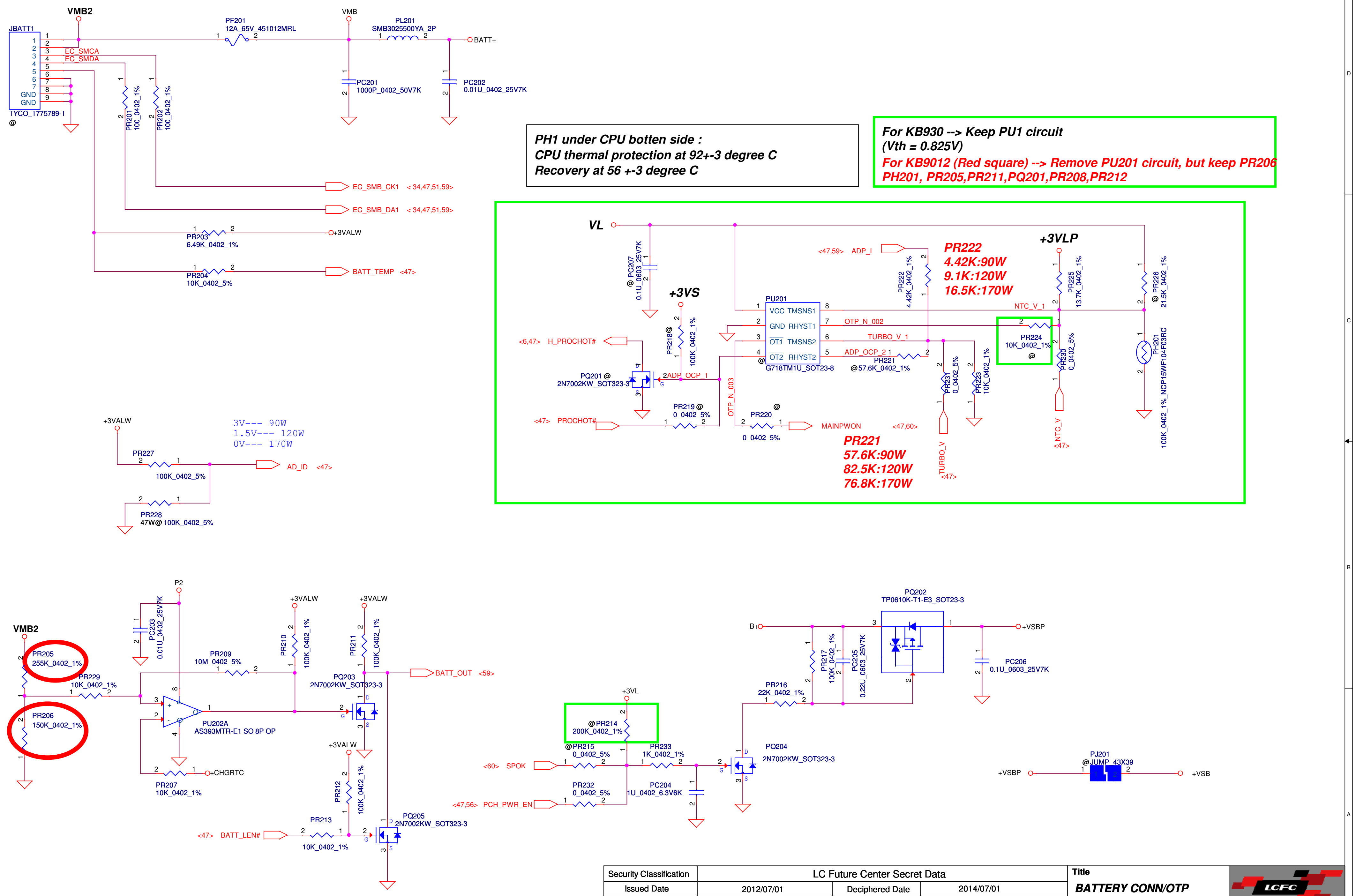

PH1 under CPU botten side :
CPU thermal protection at 92+-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205,PR211,PQ201,PR208,PR212

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
BATTERY CONN/OTP

LCFC

Size: Custom
Document Number: Y510 NM-A032
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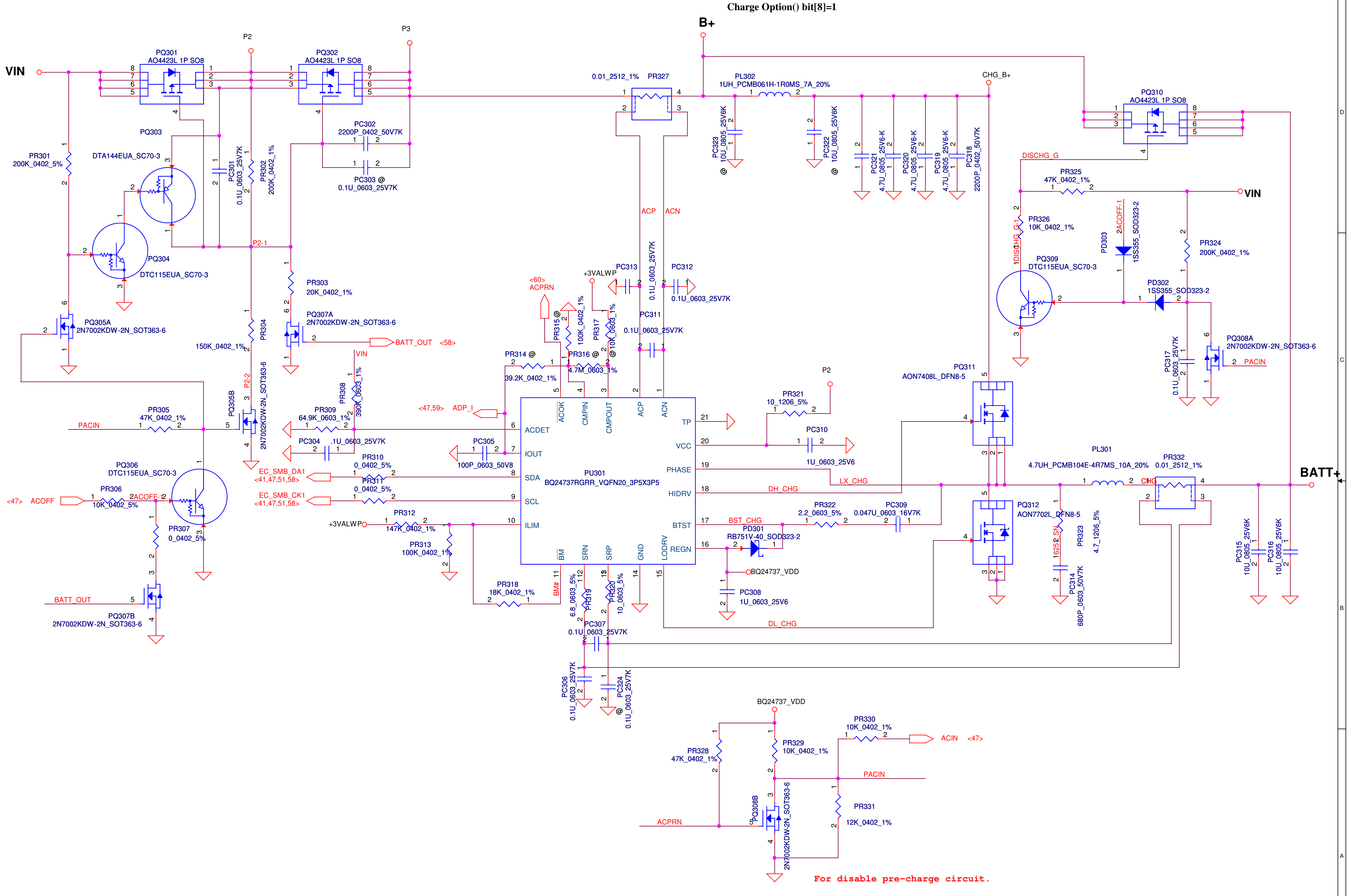

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
CHARGER

LCFC

Size Custom	Document Number Y510 NM-A032	Rev 1.0
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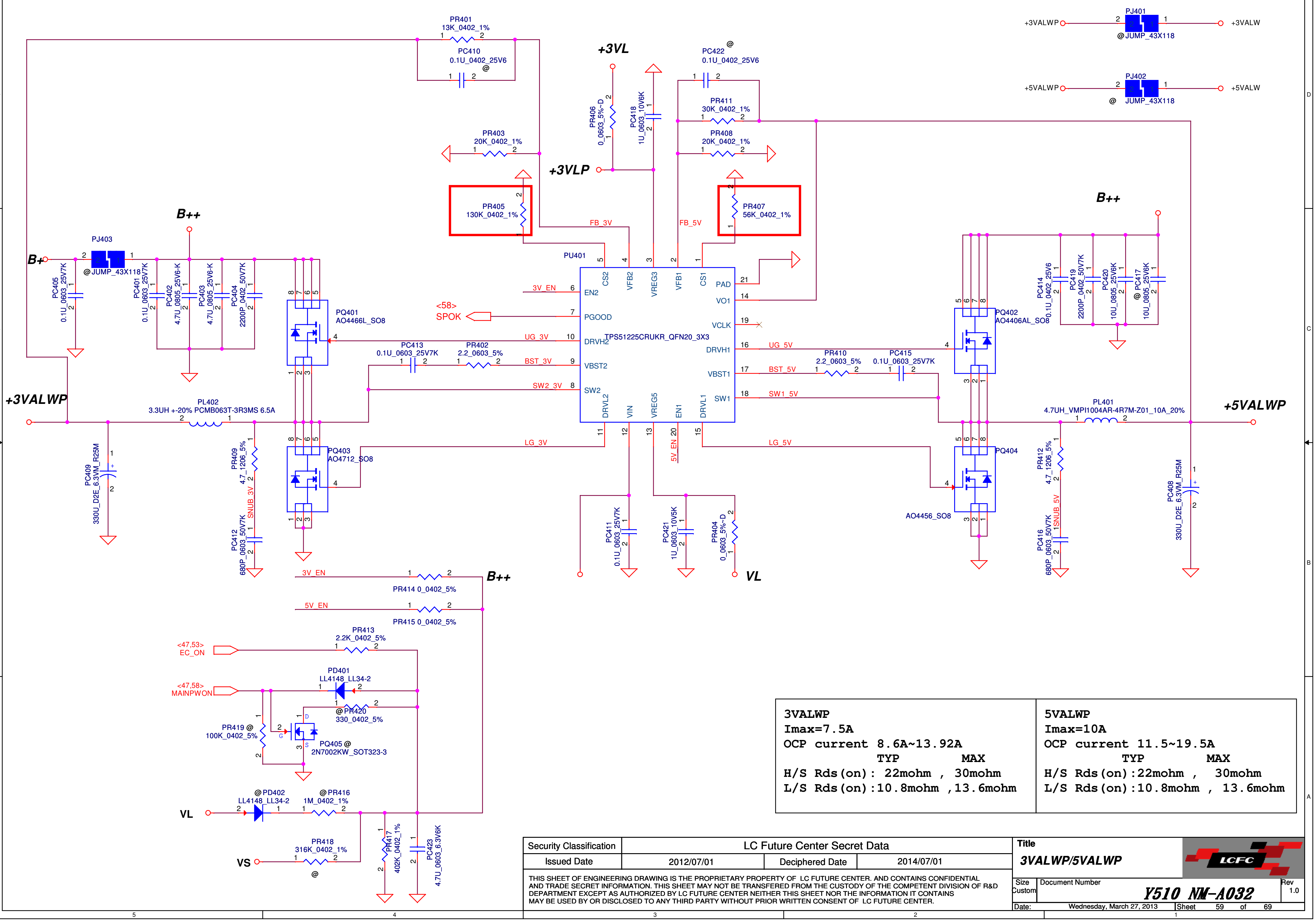

3VALWP
Imax=7.5A
OCP current 8.6A~13.92A

	TYP	MAX
H/S Rds(on):	22mohm	30mohm
L/S Rds(on):	10.8mohm	13.6mohm

5VALWP
Imax=10A
OCP current 11.5~19.5A

	TYP	MAX
H/S Rds(on):	22mohm	30mohm
L/S Rds(on):	10.8mohm	13.6mohm

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
3VALWP/5VALWP
LCFC
Size Custom
Document Number Y510 NM-A032
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Date: Wednesday, March 27, 2013
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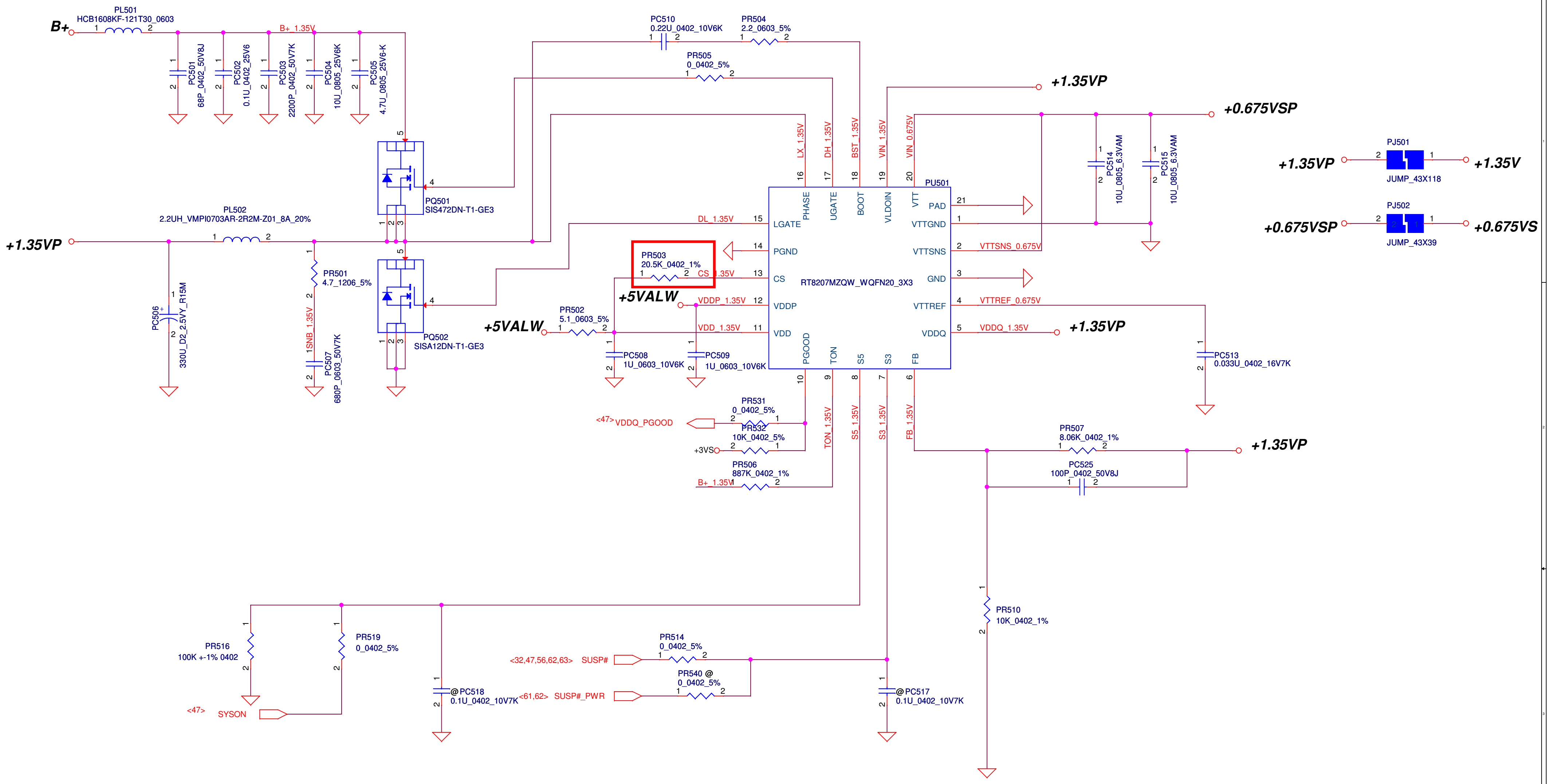

Security Classification	LC Future Center Secret Data		
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Title
1.35VP/0.675VSP

Size Custom
Document Number **Y510 NM-A032**
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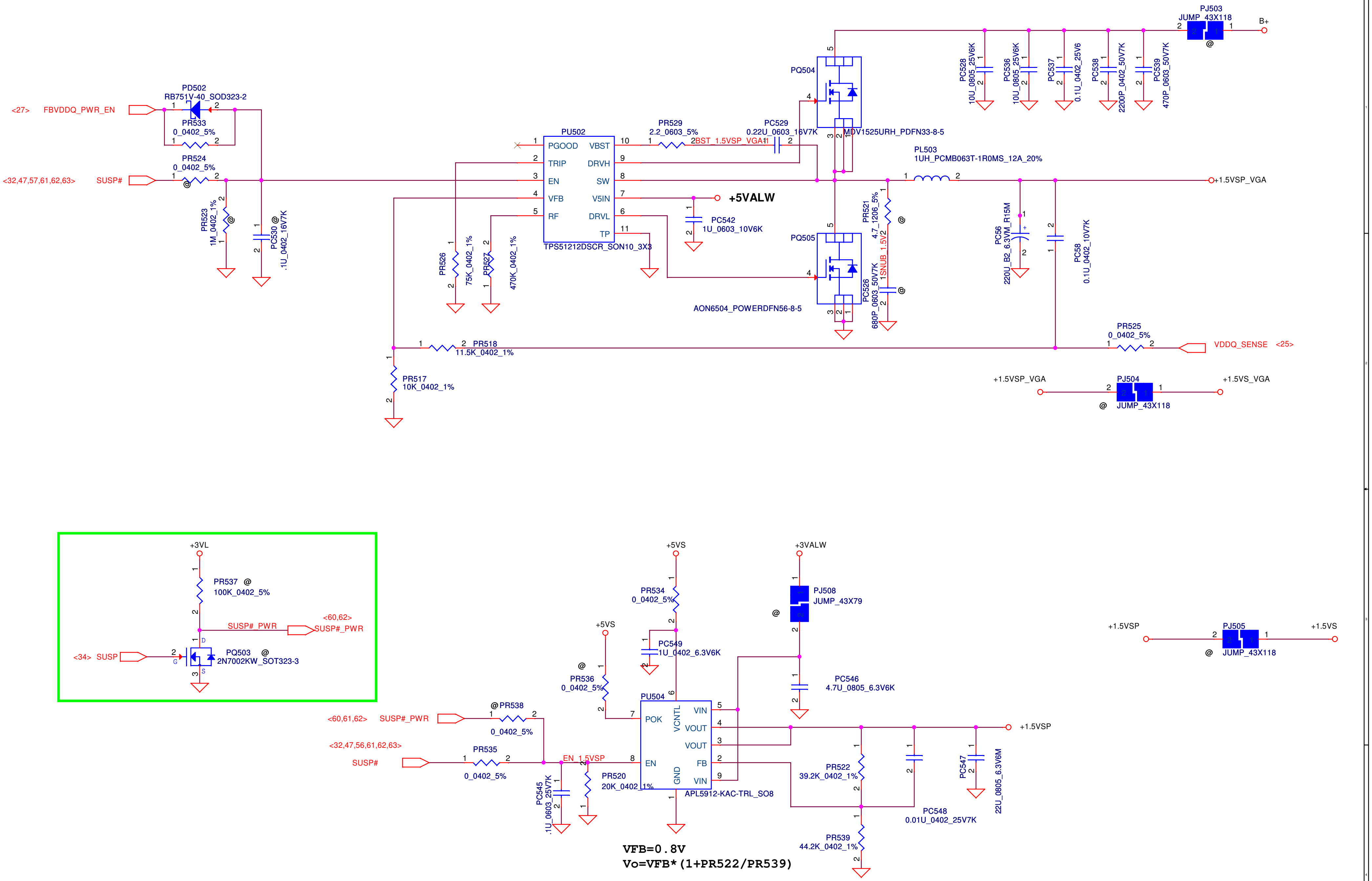

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
+1.5VS_VGA/+1.5VS

LCFC

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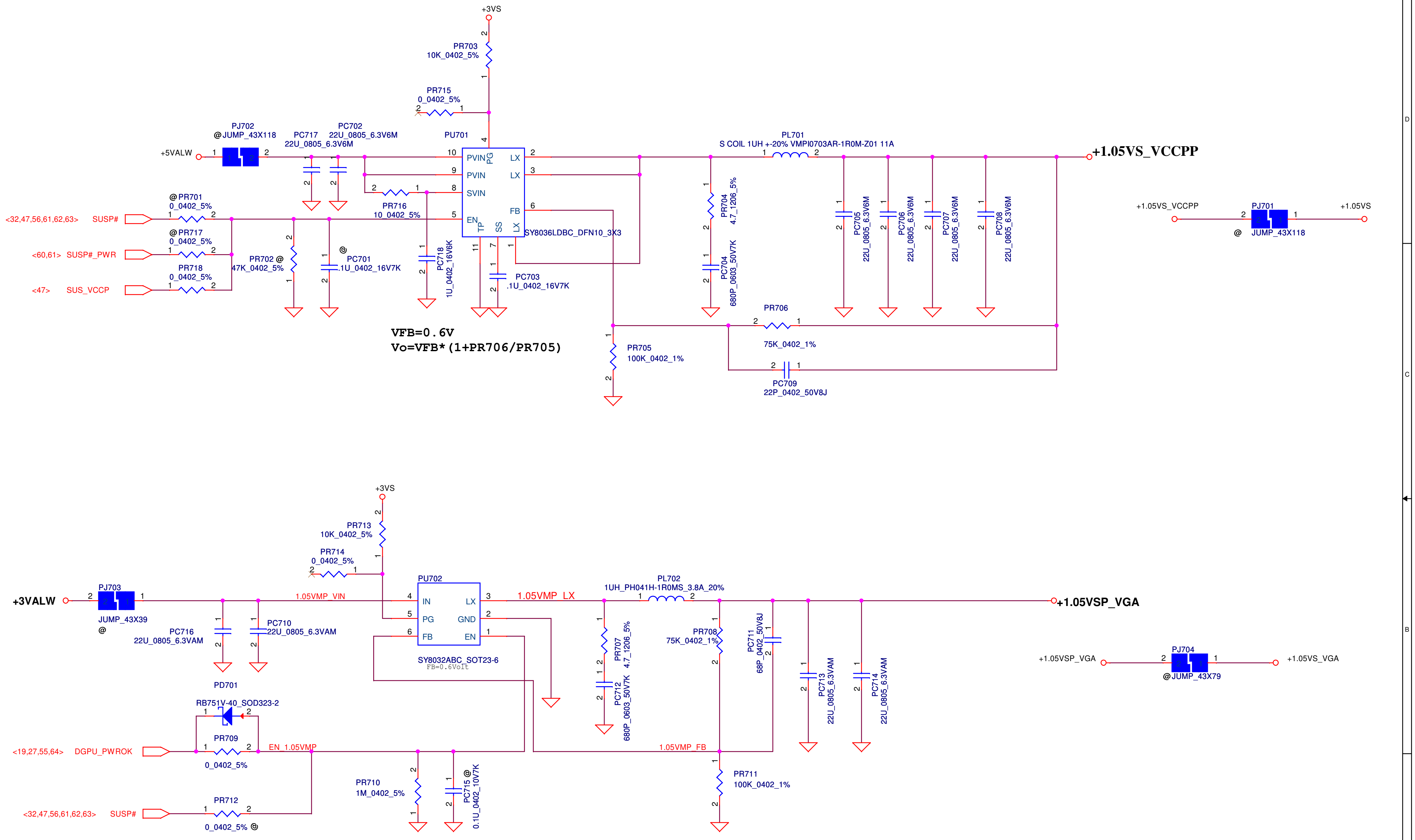

VFB=0.6V
Vo=VFB*(1+PR706/PR705)

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
+1.05VS/+1.05VS_VGA

LCFC

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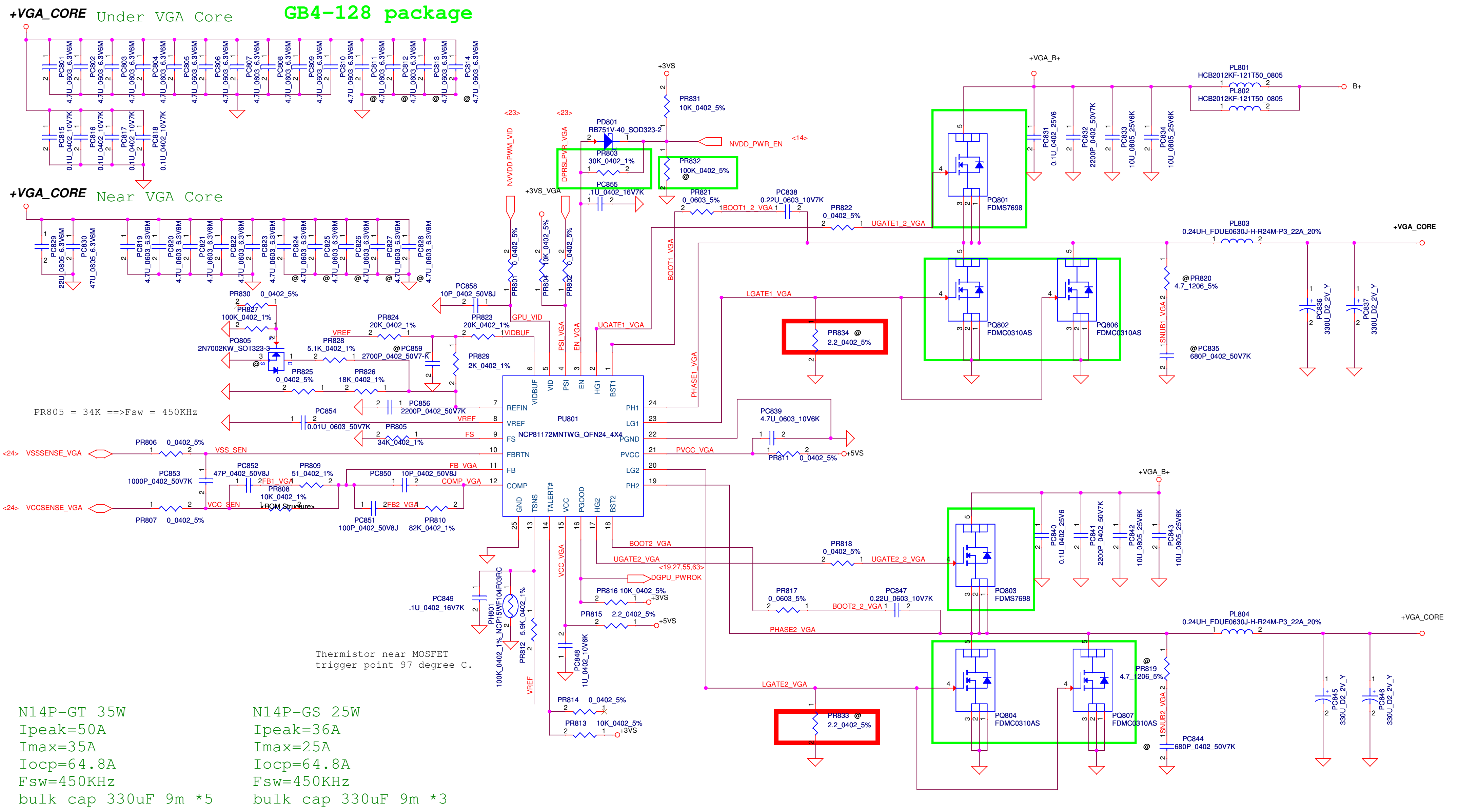

PR805 = 34K ==>Fsw = 450KHz

Thermistor near MOSFET
trigger point 97 degree C.

N14P-GT 35W
Ipeak=50A
Imax=35A
Iocp=64.8A
Fsw=450KHz
bulk cap 330uF 9m *5

N14P-GS 25W
Ipeak=36A
Imax=25A
Iocp=64.8A
Fsw=450KHz
bulk cap 330uF 9m *3

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Title
VGA_CORE

LCFC

Size	Document Number	Rev
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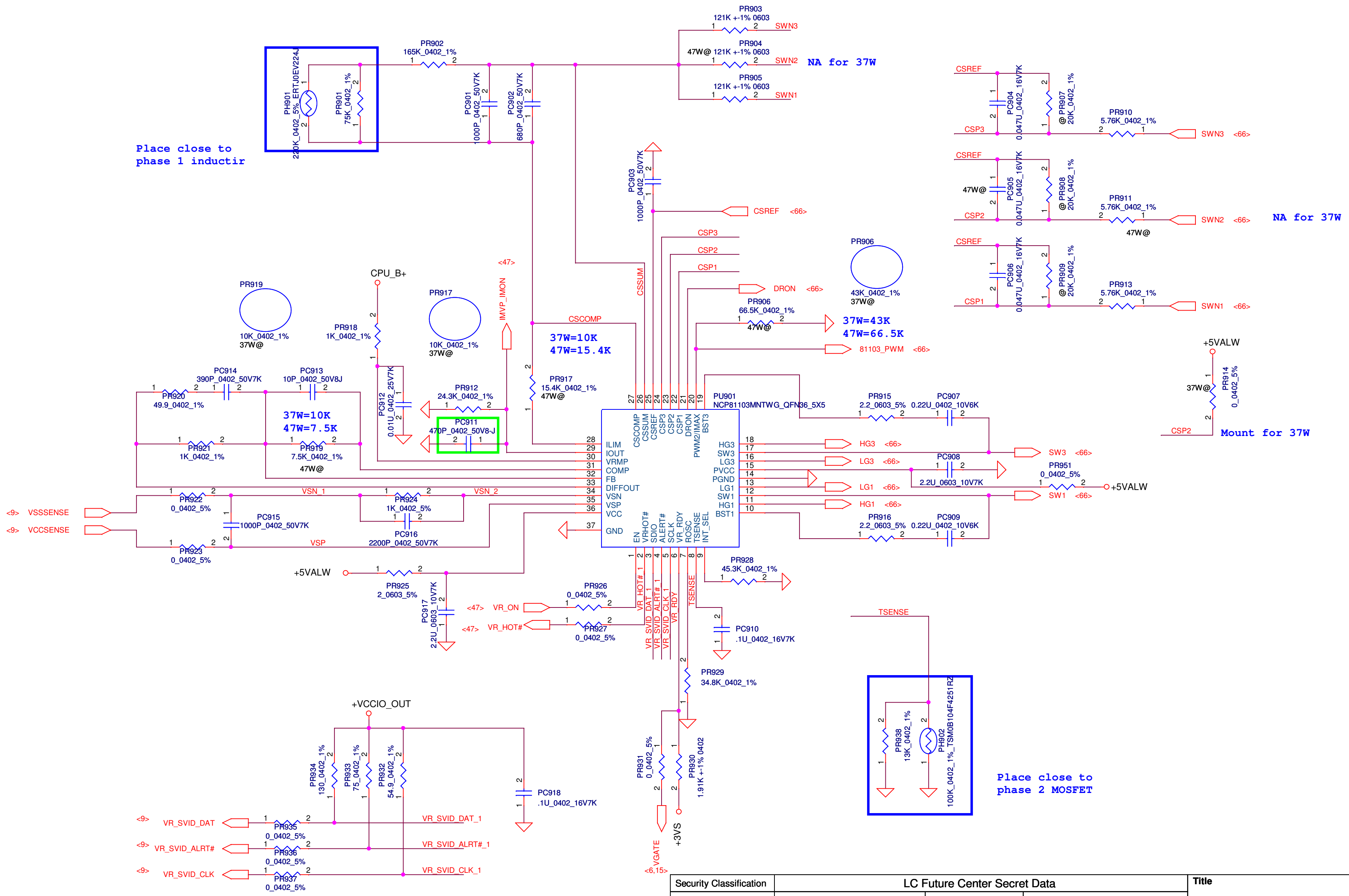


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title

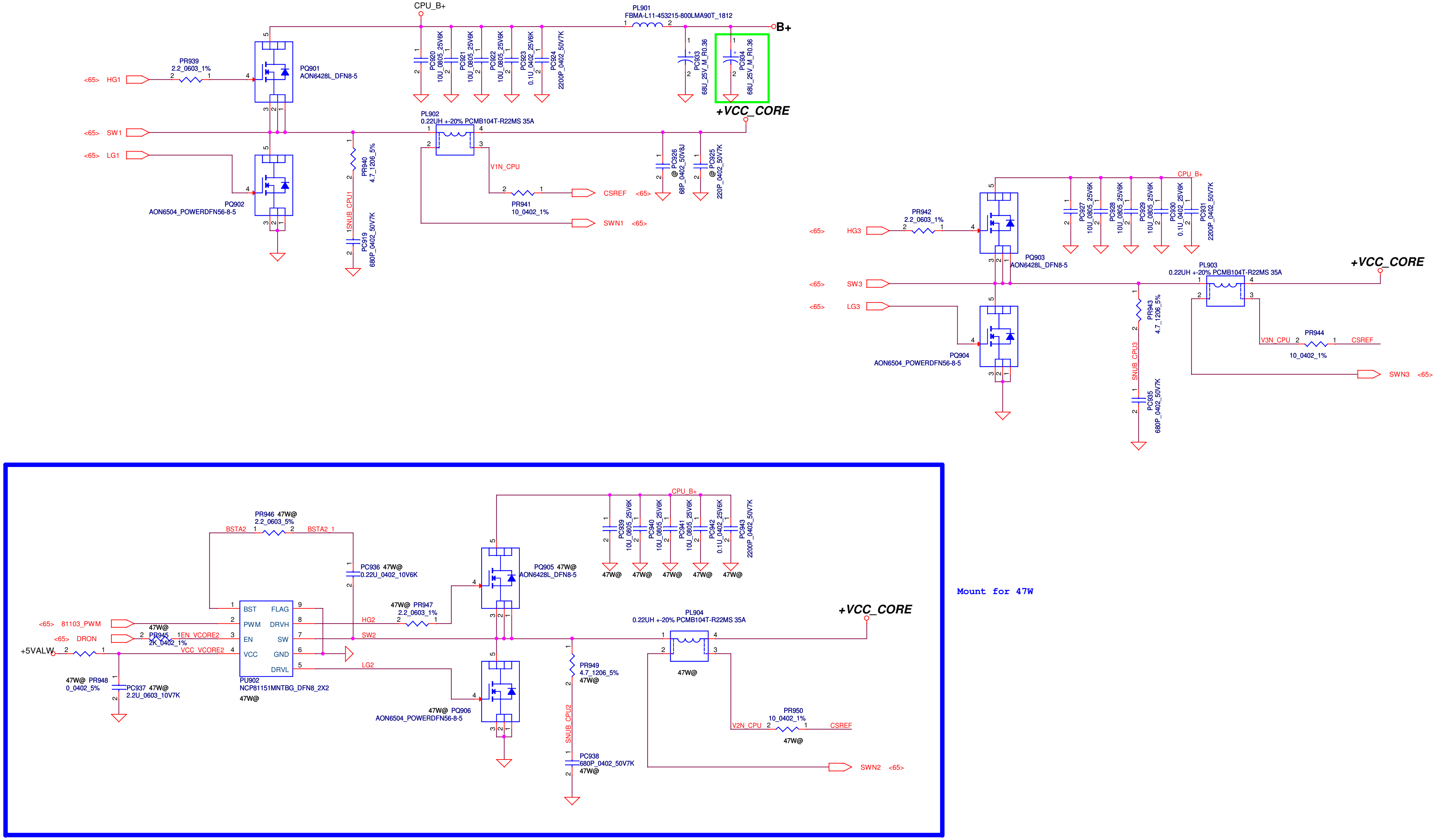
CPU_CORE

Size Custom

Document Number **Y510 NM-A032**

Rev 1.0

Date: Wednesday, March 27, 2013



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title
CPU_CORE

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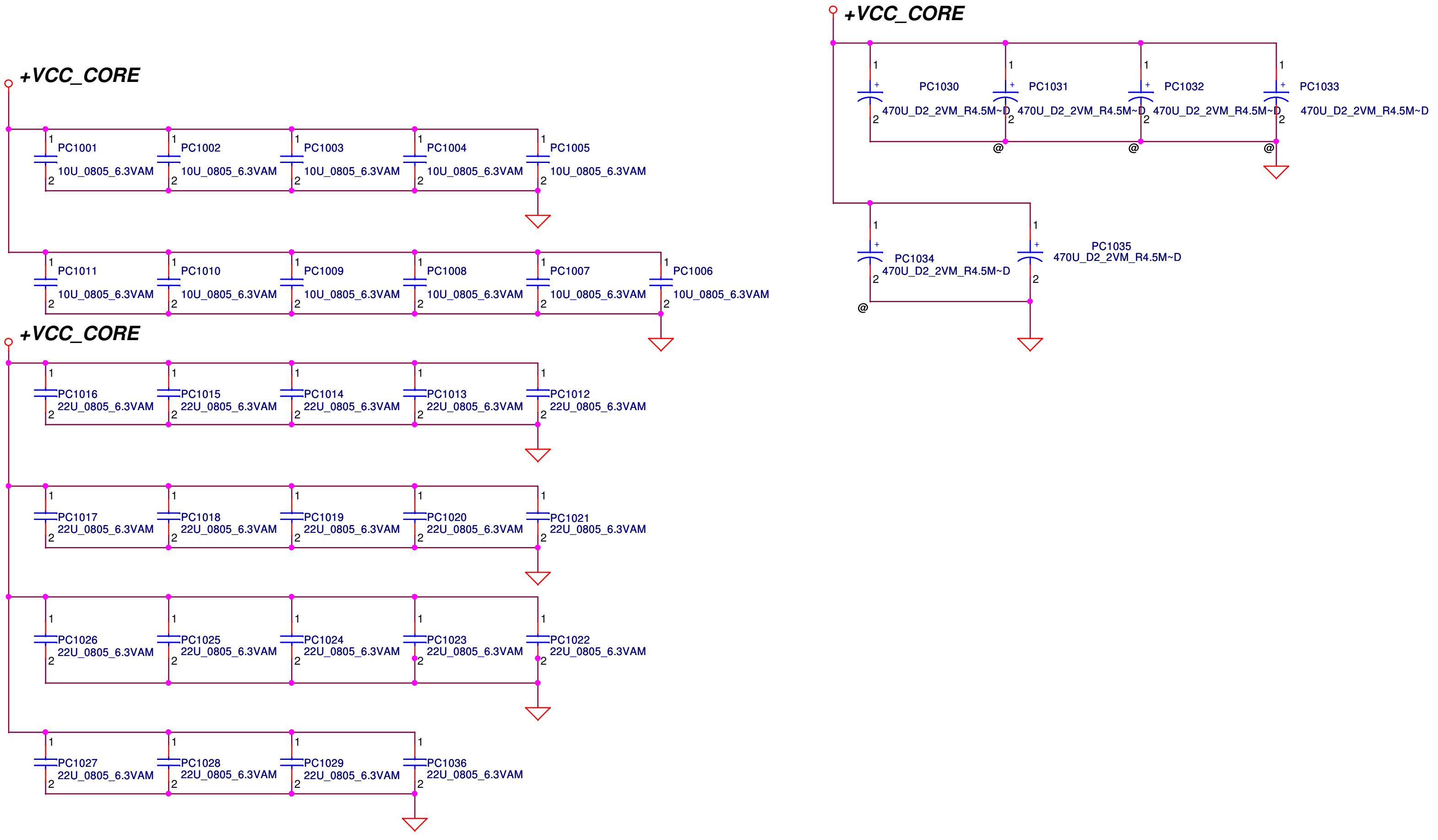
Based on PDDG rev 0.7 Table 5-1.

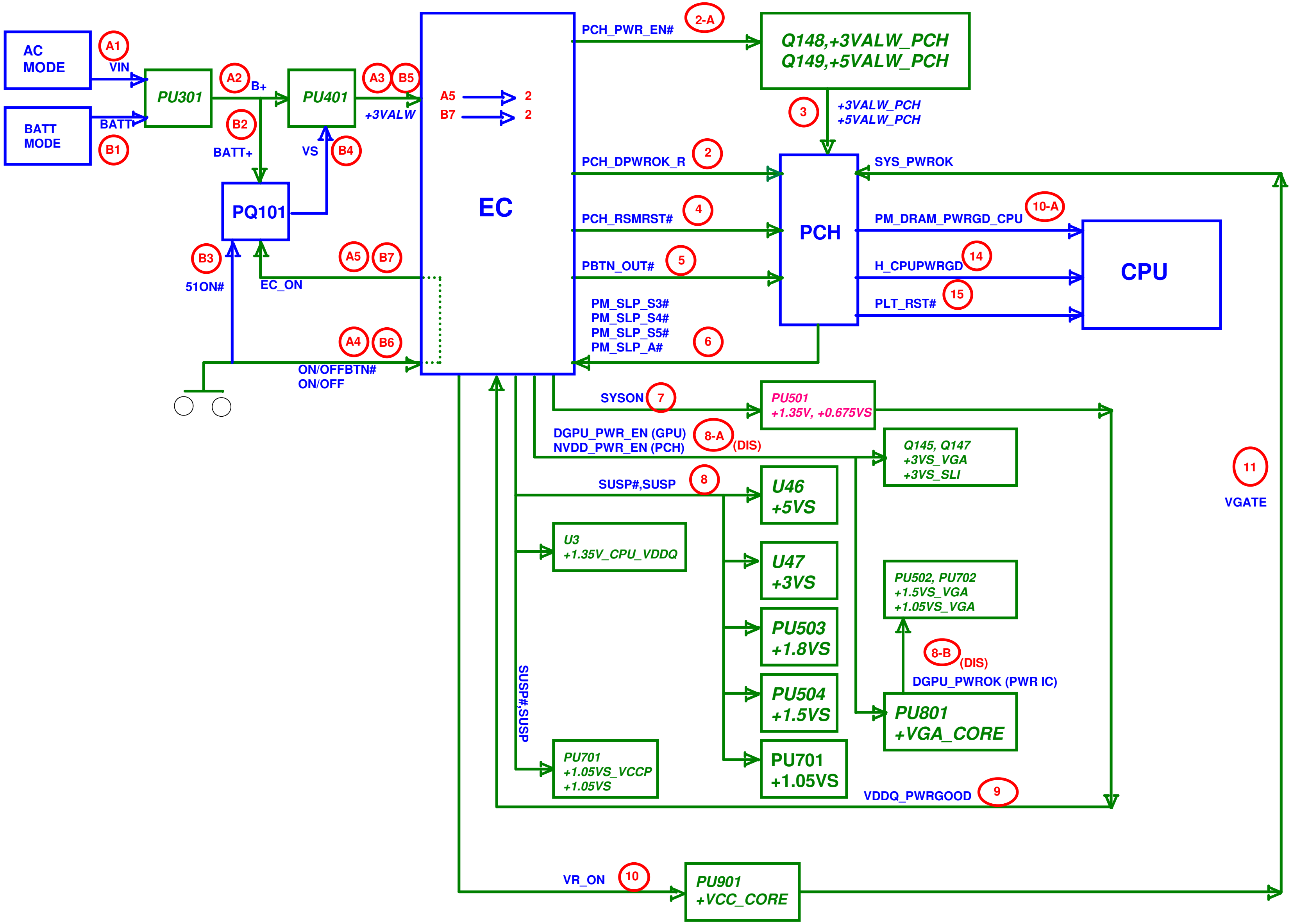


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
PROCESSOR DECOUPLING

Size	Document Number	Rev
Custom	Y510 NM-A032	1.0

Date: Wednesday, March 27, 2013



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
Power Sequence

LCFC

Size | Document Number
Y510 NM-A032
Rev 1.0

Date: Wednesday, March 27, 2013

HW PIR (Product Improve Record)

QIQY5 LA-8691P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2012/03/09

NO	DATE	PAGE		MODIFICATION LIST	PURPOSE
01)	03/14	10	R64	Change R64 BOM structure from "@" to "DS3@"	For Deep S3 Function

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
HW PIR

LCFC

Size	Document Number	Rev
	Y510 NM-A032	1.0

Date: Wednesday, March 27, 2013

Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1					
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Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title
PWR PIR

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