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ZAWBA/ZAWBB
DIS M/B Schematics Document
AMD Beema SOC with DDR3L

AMD Jet LE

2014-03-03

LA-B291P

REV：1.0

For DFB Only

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Issued Date	2014/03/03	Deciphered Date 2015/03/03	Title: Cover Page

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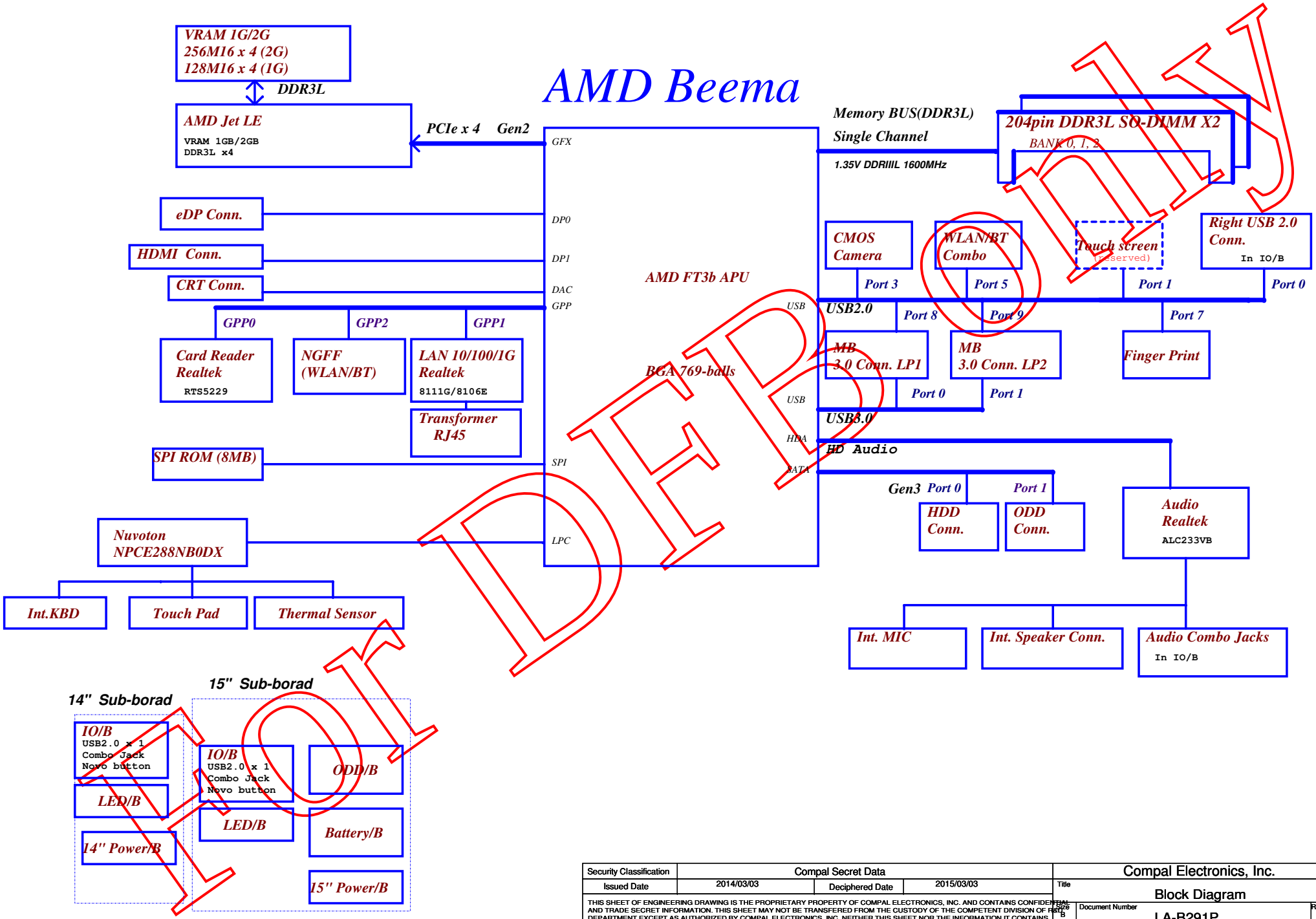
AMD Beema



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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.35V	1.35V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+3VGS	3.3V switched power rail for VGA	ON	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	ON	OFF	OFF
+1.35VGS	1.35V switched power rail for VGA	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+0.675VS	0.675V switched power rail for DDR terminator	ON	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	MP
1	PVT
2	DVT
3	EVT
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
R1562	100K +/- 5%

Board ID	R1564	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

USB OC MAPPING

OC#	USB Port	
0	USB20 port0	
1	USB20 port1,2,8,9	USB30 port0,1
2		
3		

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1	288N +3VALW	X	V +3VALW	X	X	X	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	288N +3VS	V +3VS	X	X	X	X	V +3VS	X	V +3VS	X

APU PCIE PORT LIST

Port	Device
0	Card Reader
1	LAN
2	WLAN
3	

BOM Structure Table

BOM Structure	BTO Item
45@	for HDMI Logo
14@	for 14" componect
15@	for 15" componect
B5@	15W 2.4GHz BGA APU
B4@	15W 1.8GHz BGA APU
B3@	15W 1.5GHz BGA APU
B2@	10W 1.5GHz BGA APU
B1@	10W 1.35GHz BGA APU
UMA@	UMA part
PX@	Common VGA circuit
JET@	Jet LE GPU
TOPAZ@	Topaz XT GPU
CMOS@	CMOS Camera part
HDMI@	HDMI part
8106ELDO@	Realtek RTL8106E with LDO mode
8106ESW@	Realtek RTL8106E with SWR mode
8111GLDO@	Realtek RTL8111G with LDO mode
8111GSW@	Realtek RTL8111G with SWR mode
TS@	Touch Screen
ZODD@	Zero Power ODD part
NOZODD@	Non-Zero Power ODD part
CHG@	USB Charger function
NOCHG@	Non-USB Charger function
FHD@	Full HD Panel
DR@	VRAM Dual Rank
SR@	VRAM Single Rank
USB2@	USB 2.0
USB3@	USB 3.0
233VB@	Realtek ALC233-VB Audio IC
ME@	ME part
EMIP@	EMI pop component
EMIU@	EMI Un pop component
ESDP@	ESD pop component
ESDU@	ESD Un pop component
GIGAEMIP@	EMI Un pop for LAN GIGA function
@	Unpop

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
Thermal Sensor	1001 101X b	9AH
SB-TSI (APU)	1001 100X b	98H
VGA Internal Thermal	1000 001X b	82H

APU SM Bus address

Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H
DDR DIMM2	1010 001Xb	A2H

USB Port Table

USB 2.0	USB 3.0		Port	3 External USB Port
			0	Touch Screen
			1	RIGHT USB
			2	
			3	Camera
			4	
			5	WLAN/BT Combo
			6	
			7	Finger Print
	XHCI	0	8	LEFT USB3.0
		1	9	LEFT USB3.0

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Jet LE VRAM STRAP

		X76@ Vendor UV5, UV6, UV7, UV8	ID	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV21	R_pd RV24
1GBytes	ZZZ09 JH1G@	Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	0	0	0	0	NC	4.75K
1GBytes	ZZZ10 JM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	0	0	1	8.45K	2K
1GBytes	ZZZ11 JS1G@	Samsung 2048Mbits SA000068U40 128Mx16 K4W2G1646Q-BC1A	2	0	1	0	4.53K	2K
2GBytes	ZZZ12 JH2G@	Hynix 4096Mbits SA00006E800 256Mx16 H5TC4G63AFR-11C	3	0	1	1	6.98K	4.99K
2GBytes	ZZZ13 JS2G@	Samsung 4096Mbits SA000076P00 256Mx16 K4W4G1646D-BC1A	4	1	0	0	4.53K	4.99K
2GBytes	ZZZ14 JM2G@	Micron 4096Mbits SA000077K00 256Mx16 MT41J256M16HA-093G:E	5	1	0	1	3.24K	5.62K
2GBytes	ZZZ08 JM2G2@	Micron 4096Mbits SA000065D00 256Mx16 MT41K256M16HA-107G:E	6	1	1	0	3.4K	10K
1GBytes	ZZZ16 JM1G2@	Micron 2048Mbits SA00005XB00 128Mx16 MT41K128M16JT-107G:K	7	1	1	1	4.75K	NC

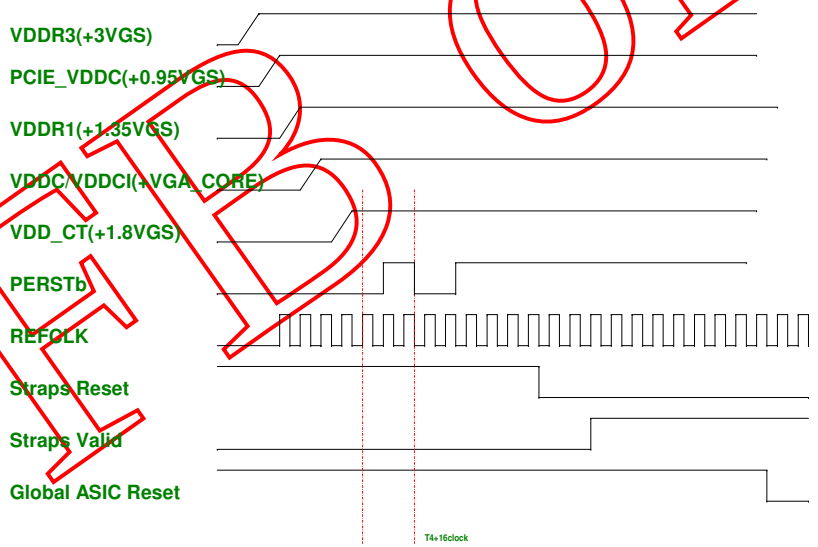
R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Power-Up/Down Sequence

"Jet" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- It is recommended that the 3.3-V rail ramp up frist.
- It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2ms from the start of VDDC ramping up.
- The power rails that are shared with other components on the system should be gated for the dGPU so that when dGPU is powered down (for example AMD PowerXpressTM idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≦ 50mV/us)
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



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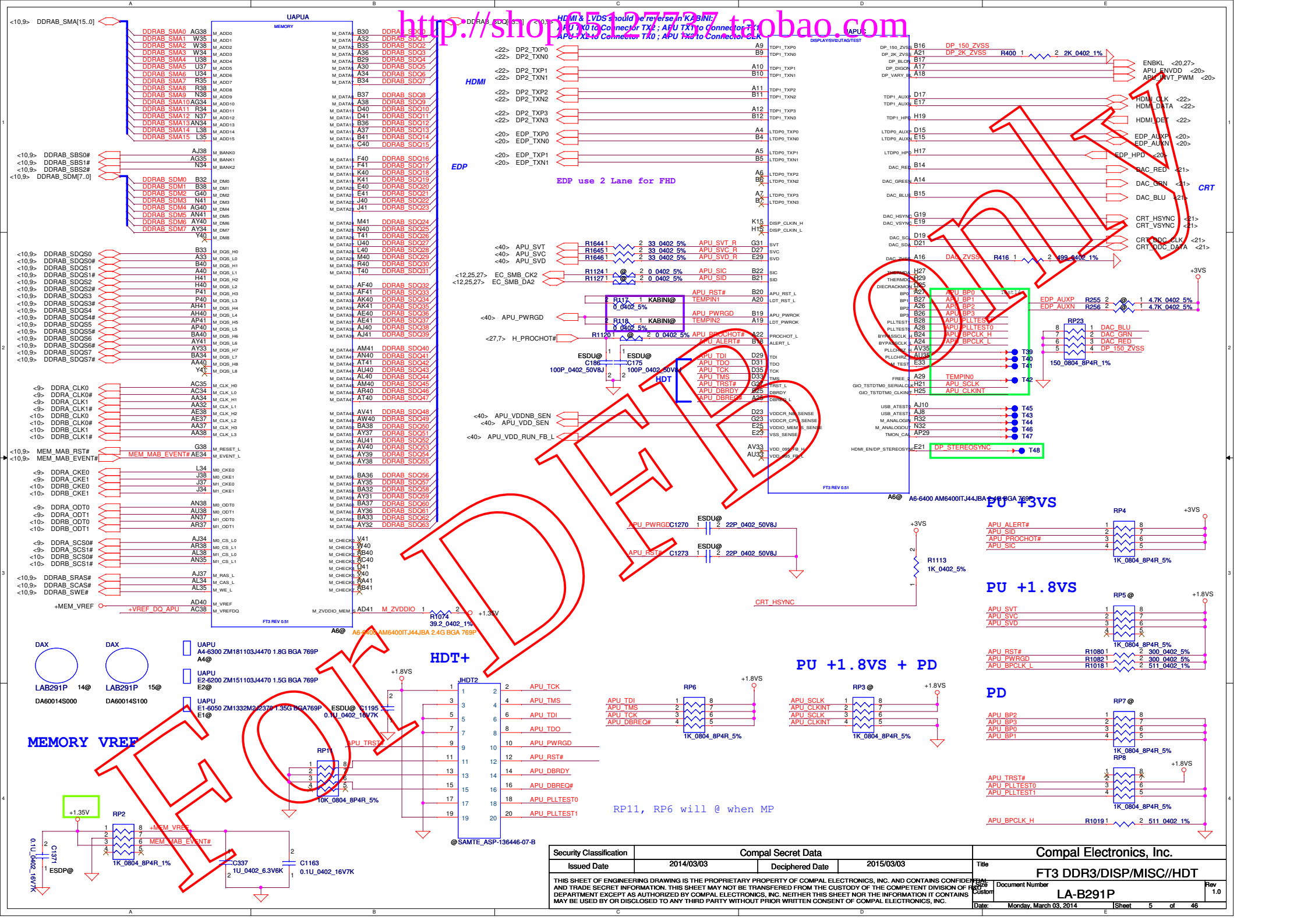

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Title: FT3 DDR3/DISP/MISC//HDT

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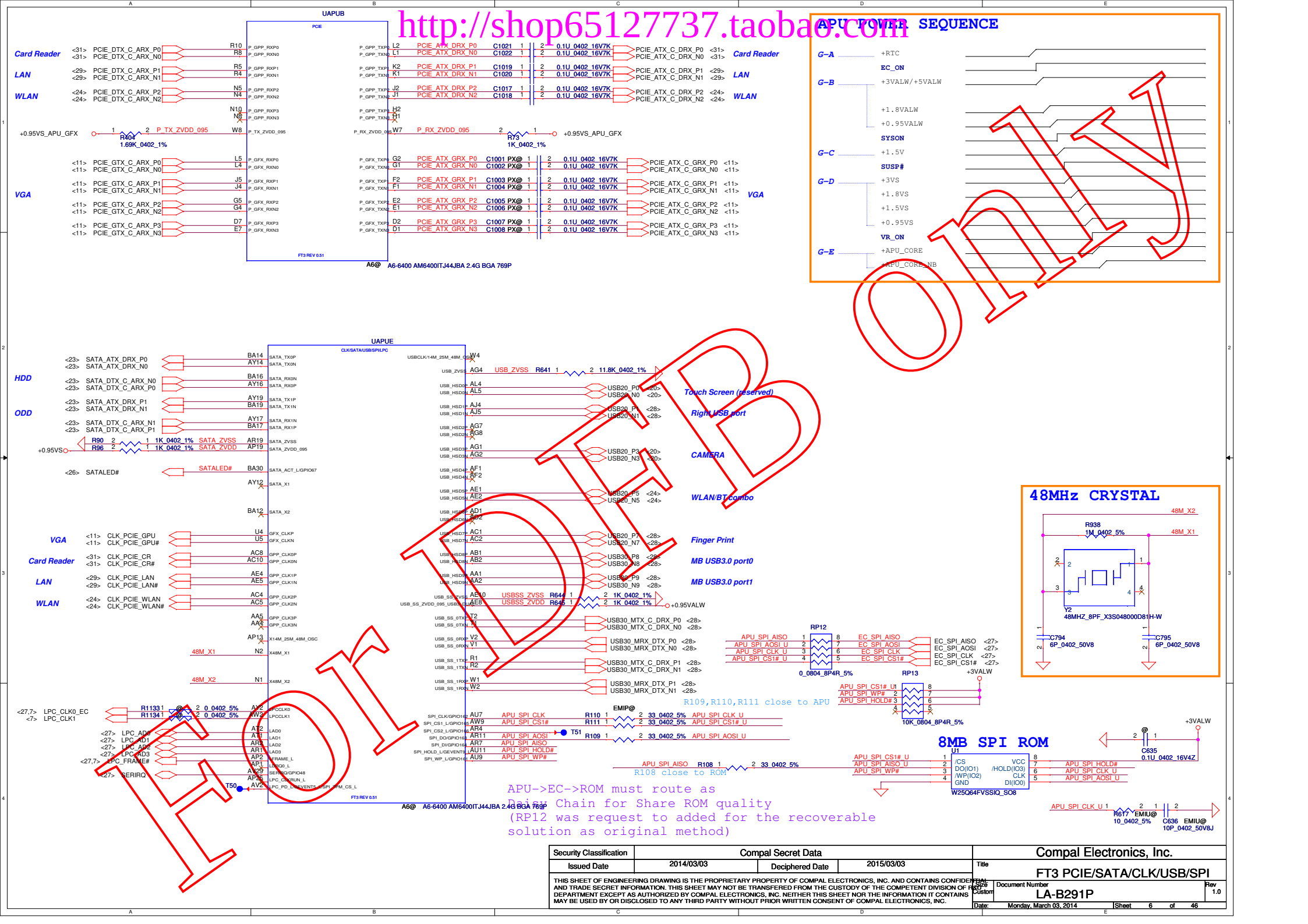

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Compal Electronics, Inc.			
Title	FT3 PCIE/SATA/CLK/USB/SPI		
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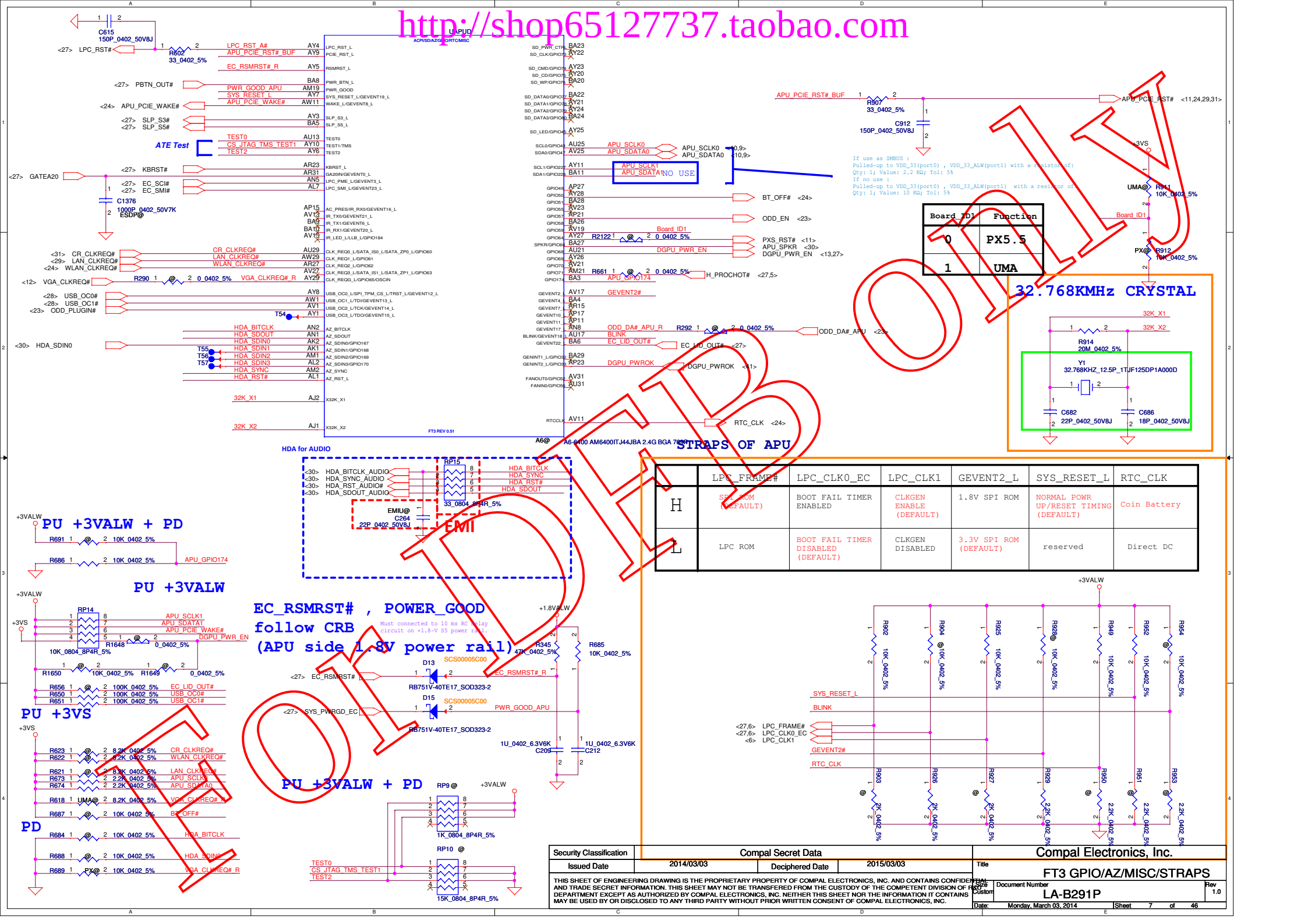

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	SYS_RESET_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)	Coin Battery
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	reserved	Direct DC

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CORE POWER OF APU

+APU_CORE — VDDCR_CPU

C1179 1U_0402_6.3V6K, C1180 1U_0402_6.3V6K, C1181 1U_0402_6.3V6K, C1182 1U_0402_6.3V6K, C1183 1U_0402_6.3V6K, C1184 1U_0402_6.3V6K, C1185 1U_0402_6.3V6K, C1187 1U_0402_6.3V6K, C1188 1U_0402_6.3V6K, C1189 1U_0402_6.3V6K, C1190 180P_0402_50V8J @

RTC OF APU

VDDBT_RTC_G

+RTCBATT_R — W=20mils — R93 1 — 2 10K_0402_5%

C1365 0.22U_0402_10V6K

CLRP1 @ SHORT PADS — Need OPEN

for Clear CMOS

+RTCBATT需過LDO轉1.5V, 20130930 added

+RTCBATT — U102 (Vout / GND / Vin) — AP2138N-1.5TRG1_SOT23-3

C811 0.1U_0603_25V7K

+RTCBATT_3V — C810 680P_0603_50VK

Need use+3.3V transfer to +1.5V LDO to APU side for Boema

INTEGRATED GPU POWER OF APU

+APU_CORE_NB — VDDCR_NB

C1200 1U_0402_6.3V6K, C1201 1U_0402_6.3V6K, C1202 1U_0402_6.3V6K, C1192 1U_0402_6.3V6K, C1191 1U_0402_6.3V6K, C1193 1U_0402_6.3V6K, C1194 1U_0402_6.3V6K, C1197 180P_0402_50V8J

+3VALW/+3VS OF APU

+3VS — C1249 1U_0402_6.3V6K, C1257 180P_0402_50V8J

+3VALW_APU — R582 @ 1 — 2 0_0603_5%

+3VALW — C1252 1U_0402_6.3V6K, C1253 1U_0402_6.3V6K

VDD_33 — VDD_33_ALW

VDDIO_AZ_ALW
(Could be S0 or S5 power rail)

+1.35V — VDDIO_MEM_S — PLANE SPLIT

C924 10U_0603_6.3V6M, C925 10U_0603_6.3V6M, C949 10U_0603_6.3V6M, C823 0.1U_0402_16V7K, C825 0.1U_0402_16V7K, C827 0.1U_0402_16V7K, C828 0.1U_0402_16V7K, C829 0.1U_0402_16V7K, C830 0.1U_0402_16V7K, C831 0.1U_0402_16V7K, C832 0.1U_0402_16V7K, C1211 180P_0402_50V8J, C1210 180P_0402_50V8J, C1208 180P_0402_50V8J, C1207 180P_0402_50V8J, C1230 180P_0402_50V8J, C1231 180P_0402_50V8J, C1258 180P_0402_50V8J, C1259 180P_0402_50V8J, C1372 0.1U_0402_16V7K ESD@, C1373 0.1U_0402_16V7K ESD@

+1.5VS — C1161 @ 4.7U_0603_6.3V6K, C1255 1U_0402_6.3V6K, C1254 1U_0402_6.3V6K, C1255 1U_0402_6.3V6K, C1232 180P_0402_50V8J

+0.95VALW/+0.95VS OF APU

VDD_095_GFX

+0.95VS — VDD_095 — L22 FBMA-L11-201209-121LMA50T_0805

C935 10U_0603_6.3V6M, C934 10U_0603_6.3V6M, C1198 1U_0402_6.3V6K, C1199 1U_0402_6.3V6K, C1205 1U_0402_6.3V6K, C1204 1U_0402_6.3V6K, C1206 1U_0402_6.3V6K, C1250 1U_0402_6.3V6K, C1213 180P_0402_50V8J

+0.95VS_APU_GFX — C938 10U_0603_6.3V6M, C1203 1U_0402_6.3V6K

+0.95VALW — C937 10U_0603_6.3V6M, C938 10U_0603_6.3V6M, C1216 1U_0402_6.3V6K, C1214 1U_0402_6.3V6K, C1221 1U_0402_6.3V6K, C1218 180P_0402_50V8J

+0.95VALW — C1220 1U_0402_6.3V6K, C1217 1U_0402_6.3V6K, C1219 1U_0402_6.3V6K, C1222 1U_0402_6.3V6K

VDD_095_USB3_DUAL — VDD_095_ALW

+1.8VALW/+1.8VS OF APU

VDD_18

+1.8VS — C933 10U_0603_6.3V6M, C1236 1U_0402_6.3V6K, C1237 1U_0402_6.3V6K, C1238 1U_0402_6.3V6K, C1239 1U_0402_6.3V6K, C1240 1U_0402_6.3V6K, C1223 180P_0402_50V8J

+1.8VALW — C1160 4.7U_0603_6.3V6K, C1244 1U_0402_6.3V6K, C1250 1U_0402_6.3V6K, C1246 1U_0402_6.3V6K, C1245 1U_0402_6.3V6K, C1245 180P_0402_50V8J

VDD_18_ALW

UAPUF

POWER

+1.35V — VDDIO_MEM_S_1 J35, VDDIO_MEM_S_2 L32, VDDIO_MEM_S_3 L37, VDDIO_MEM_S_4 N35, VDDIO_MEM_S_5 R31, VDDIO_MEM_S_6 R37, VDDIO_MEM_S_7 U32, VDDIO_MEM_S_8 U35, VDDIO_MEM_S_9 W31, VDDIO_MEM_S_10 W32, VDDIO_MEM_S_11 AA31, VDDIO_MEM_S_12 AA35, VDDIO_MEM_S_13 AC32, VDDIO_MEM_S_14 AC37, VDDIO_MEM_S_15 AE31, VDDIO_MEM_S_16 AE35, VDDIO_MEM_S_17 AG32, VDDIO_MEM_S_18 AG37, VDDIO_MEM_S_19 AJ35, VDDIO_MEM_S_20 AJ32, VDDIO_MEM_S_21 AL37, VDDIO_MEM_S_22 AR35, VDDIO_MEM_S_23

+APU_CORE — VDDCR_CPU_1 L21, VDDCR_CPU_2 L23, VDDCR_CPU_3 L25, VDDCR_CPU_4 L27, VDDCR_CPU_5 L29, VDDCR_CPU_6 N21, VDDCR_CPU_7 N23, VDDCR_CPU_8 N27, VDDCR_CPU_9 R21, VDDCR_CPU_10 R23, VDDCR_CPU_11 R27, VDDCR_CPU_12 U21, VDDCR_CPU_13 U23, VDDCR_CPU_14 U27, VDDCR_CPU_15 W21, VDDCR_CPU_16 W23, VDDCR_CPU_17 W27, VDDCR_CPU_18 AA21, VDDCR_CPU_19 AA23, VDDCR_CPU_20 AA27, VDDCR_CPU_21 AC21, VDDCR_CPU_22 AC23, VDDCR_CPU_23 AC27, VDDCR_CPU_24 AE21, VDDCR_CPU_25 AE23, VDDCR_CPU_26 AE27

+APU_CORE_NB — VDDCR_NB_1 L13, VDDCR_NB_2 L17, VDDCR_NB_3 N11, VDDCR_NB_4 N13, VDDCR_NB_5 N17, VDDCR_NB_6 R11, VDDCR_NB_7 R13, VDDCR_NB_8 R17, VDDCR_NB_9 U13, VDDCR_NB_10 U17, VDDCR_NB_11 W13, VDDCR_NB_12 W17, VDDCR_NB_13 AA13, VDDCR_NB_14 AA17, VDDCR_NB_15 AC13, VDDCR_NB_16 AC17, VDDCR_NB_17 AE15, VDDCR_NB_18 AE17, VDDCR_NB_19 AE19, VDDCR_NB_20 AG17, VDDCR_NB_21 AG21

+1.5VS — VDDIO_AZ_ALW_1 AL10, VDDIO_AZ_ALW_2 AL11

+1.8VALW — VDD_18_ALW_1 B1, VDD_18_ALW_2 B2

+1.8VS — VDD_18_1 A2, VDD_18_2 A3, VDD_18_3 B3, VDD_18_4 C3

+3VALW_APU — VDD_33_ALW_1 AL13, VDD_33_ALW_2 AM13

+3VS — VDD_33_1 AM15, VDD_33_2 AM17

+0.95VALW — VDD_095_USB3_DUAL_1 AR5, VDD_095_USB3_DUAL_2 AU4, VDD_095_USB3_DUAL_3 AV7, VDD_095_USB3_DUAL_4 AW5

+0.95VS — VDD_095_1 AG23, VDD_095_2 AG27, VDD_095_3 AJ21, VDD_095_4 AJ27, VDD_095_5 AL21, VDD_095_6 AL23, VDD_095_7 AL27, VDD_095_8 AM23, VDD_095_9 AM25

+0.95VALW — VDD_095_ALW_1 AE11, VDD_095_ALW_2 AE13, VDD_095_ALW_3 AJ11, VDD_095_ALW_4 AJ13

+0.95VS_APU_GFX — VDD_095_GFX_1 U10, VDD_095_GFX_2 W10, VDD_095_GFX_3 AA10

+RTCBATT_R — VDDBT_RTC_G AN4

FT3 REV 0.51

A6@ A6-6400 AM6400ITJ44JBA 2.4G BGA 769P

UAPUG

GND

VSS_1 A8, VSS_2 A13, VSS_3 A23, VSS_4 A31, VSS_5 A35, VSS_6 A39, VSS_7 B8, VSS_8 B13, VSS_9 B23, VSS_10 B31, VSS_11 B39, VSS_12 C1, VSS_13 C2, VSS_14 C5, VSS_15 C7, VSS_16 C9, VSS_17 C11, VSS_18 C13, VSS_19 C15, VSS_20 C19, VSS_21 C21, VSS_22 C23, VSS_23 C25, VSS_24 C27, VSS_25 C29, VSS_26 C31, VSS_27 C33, VSS_28 C35, VSS_29 C37, VSS_30 C39, VSS_31 C41, VSS_32 D9, VSS_33 D11, VSS_34 D13, VSS_35 E3, VSS_36 E4, VSS_37 E9, VSS_38 E11, VSS_39 E13, VSS_40 E27, VSS_41 E31, VSS_42 E35, VSS_43 E38, VSS_44 E39, VSS_45 G3, VSS_46 G7, VSS_47 G11, VSS_48 G13, VSS_49 G15, VSS_50 G17, VSS_51 G21, VSS_52 G25, VSS_53 G29, VSS_54 G35, VSS_55 G37, VSS_56 G39, VSS_57 G41, VSS_58 H11, VSS_59 H13, VSS_60 H23, VSS_61 H31, VSS_62 J3, VSS_63 J7, VSS_64 J8, VSS_65 J39, VSS_66 K11, VSS_67 K13, VSS_68 K17, VSS_69 K19, VSS_70 K21, VSS_71 K23, VSS_72 K25, VSS_73 K27, VSS_74 K29, VSS_75 K31, VSS_76 L3, VSS_77 L7, VSS_78 L8, VSS_79 L10, VSS_80 L11, VSS_81 L15, VSS_82 L19, VSS_83 L31, VSS_84 L39, VSS_85 L41, VSS_86 M1, VSS_87 M2, VSS_88 N7, VSS_89 N15, VSS_90 N19, VSS_91 N25, VSS_92 N29, VSS_93 N31, VSS_94 N39, VSS_95 P1, VSS_96 P2, VSS_97 R3, VSS_98 R7, VSS_99 R15, VSS_100 R19, VSS_101 R25, VSS_102 R29, VSS_103 R39, VSS_104 R41, VSS_105 U1, VSS_106 U2, VSS_107 U3, VSS_108 U7, VSS_109 U8, VSS_110 U11, VSS_111 U15, VSS_112 U19, VSS_113 U25, VSS_114 U29, VSS_115 U31, VSS_116 U39, VSS_117 W3, VSS_118 W5, VSS_119 W11, VSS_120 W15, VSS_121 W19, VSS_122 W25, VSS_123 W29, VSS_124 W39, VSS_125 W41, VSS_126 Y1, VSS_127 Y2, VSS_128 AA3, VSS_129 AA7, VSS_130 AA8, VSS_131 AA11, VSS_132 AA15, VSS_133 AA19, VSS_134 AA25, VSS_135 AA29, VSS_136 AA39, VSS_137 AC3, VSS_138 AC7, VSS_139 AC11, VSS_140 AC15, VSS_141 AC19, VSS_142 AC25, VSS_143 AC29, VSS_144 AC31, VSS_145 AC39, VSS_146 AC41, VSS_147 AE3, VSS_148 AE7, VSS_149 AE25, VSS_150 AE29, VSS_151 AE32, VSS_152 AE39, VSS_153 AG3, VSS_154 AG5, VSS_155 AG10, VSS_156 AG11, VSS_157 AG13, VSS_158 AG15, VSS_159 AG19, VSS_160 AG25, VSS_161 AG29, VSS_162 AG31, VSS_163 AG39, VSS_164 AG41, VSS_165 AH1, VSS_166 AH2, VSS_167 AJ3, VSS_168 AJ7, VSS_169 AJ15, VSS_170 AJ17, VSS_171 AJ19, VSS_172 AJ23, VSS_173 AJ25, VSS_174 AJ29, VSS_175 AJ31, VSS_176 AJ32, VSS_177 AJ39, VSS_178 AL3, VSS_179 AL8, VSS_180 AL15, VSS_181 AL17, VSS_182 AL19, VSS_183 AL25, VSS_184 AL29, VSS_185 AL39, VSS_186 AL41, VSS_187 AM11, VSS_188 AM27, VSS_189 AM31, VSS_190 AN3, VSS_191 AN7, VSS_192 AN39, VSS_193 AP31, VSS_194 AR3, VSS_195 AR13, VSS_196 AR17, VSS_197 AR21, VSS_198 AR25, VSS_199 AR29, VSS_200 AR39, VSS_201 AR41, VSS_202 AU1, VSS_203 AU2, VSS_204 AU3, VSS_205 AU15, VSS_206 AU19, VSS_207 AU23, VSS_208 AU27, VSS_209 AU39, VSS_210 AV9, VSS_211 AW3, VSS_212 AW7, VSS_213 AW13, VSS_214 AW15, VSS_215 AW17, VSS_216 AW19, VSS_217 AW21, VSS_218 AW23, VSS_219 AW25, VSS_220 AW27, VSS_221 AW31, VSS_222 AW33, VSS_223 AW35, VSS_224 AW37, VSS_225 AW39, VSS_226 AW41, VSS_227 AY3, VSS_228 AY15, VSS_229 AY18, VSS_230 AY30, VSS_231 BA2, VSS_232 BA7, VSS_233 BA13, VSS_234 BA15, VSS_235 BA18, VSS_236 BA21, VSS_237 BA25, VSS_238 BA31, VSS_239 BA35, VSS_240 BA39, VSS_241 A15, VSS_242 AL31, VSSBG_DAC AM29, VBUFF, PSEN

FT3 REV 0.51

A6@ A6-6400 AM6400ITJ44JBA 2.4G BGA 769P

UAPUH

GND

VSS_187 AL39, VSS_188 AL41, VSS_189 AM11, VSS_190 AM27, VSS_191 AM31, VSS_192 AN3, VSS_193 AN7, VSS_194 AN39, VSS_195 AP31, VSS_196 AR3, VSS_197 AR13, VSS_198 AR17, VSS_199 AR21, VSS_200 AR25, VSS_201 AR29, VSS_202 AR39, VSS_203 AR41, VSS_204 AU1, VSS_205 AU2, VSS_206 AU3, VSS_207 AU15, VSS_208 AU19, VSS_209 AU23, VSS_210 AU27, VSS_211 AU39, VSS_212 AV9, VSS_213 AW3, VSS_214 AW7, VSS_215 AW13, VSS_216 AW15, VSS_217 AW17, VSS_218 AW19, VSS_219 AW21, VSS_220 AW23, VSS_221 AW25, VSS_222 AW27, VSS_223 AW31, VSS_224 AW33, VSS_225 AW35, VSS_226 AW37, VSS_227 AW39, VSS_228 AW41, VSS_229 AY13, VSS_230 AY15, VSS_231 AY18, VSS_232 AY30, VSS_233 BA2, VSS_234 BA7, VSS_235 BA13, VSS_236 BA15, VSS_237 BA18, VSS_238 BA21, VSS_239 BA25, VSS_240 BA31, VSS_241 BA35, VSS_242 BA39, VSS_243 A15, VSS_244 AL31, VSS_245 AM29

FT3 REV 0.51

A6@ A6-6400 AM6400ITJ44JBA 2.4G BGA 769P

TEMPINRETUNE — R131 KABINI@ 2 — 0_0402_5%

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Issued Date	2014/03/03	Deciphered Date 2015/03/05	Title: FT3 PWR/GND

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Date: Monday, March 03, 2014	Sheet 8 of 46		

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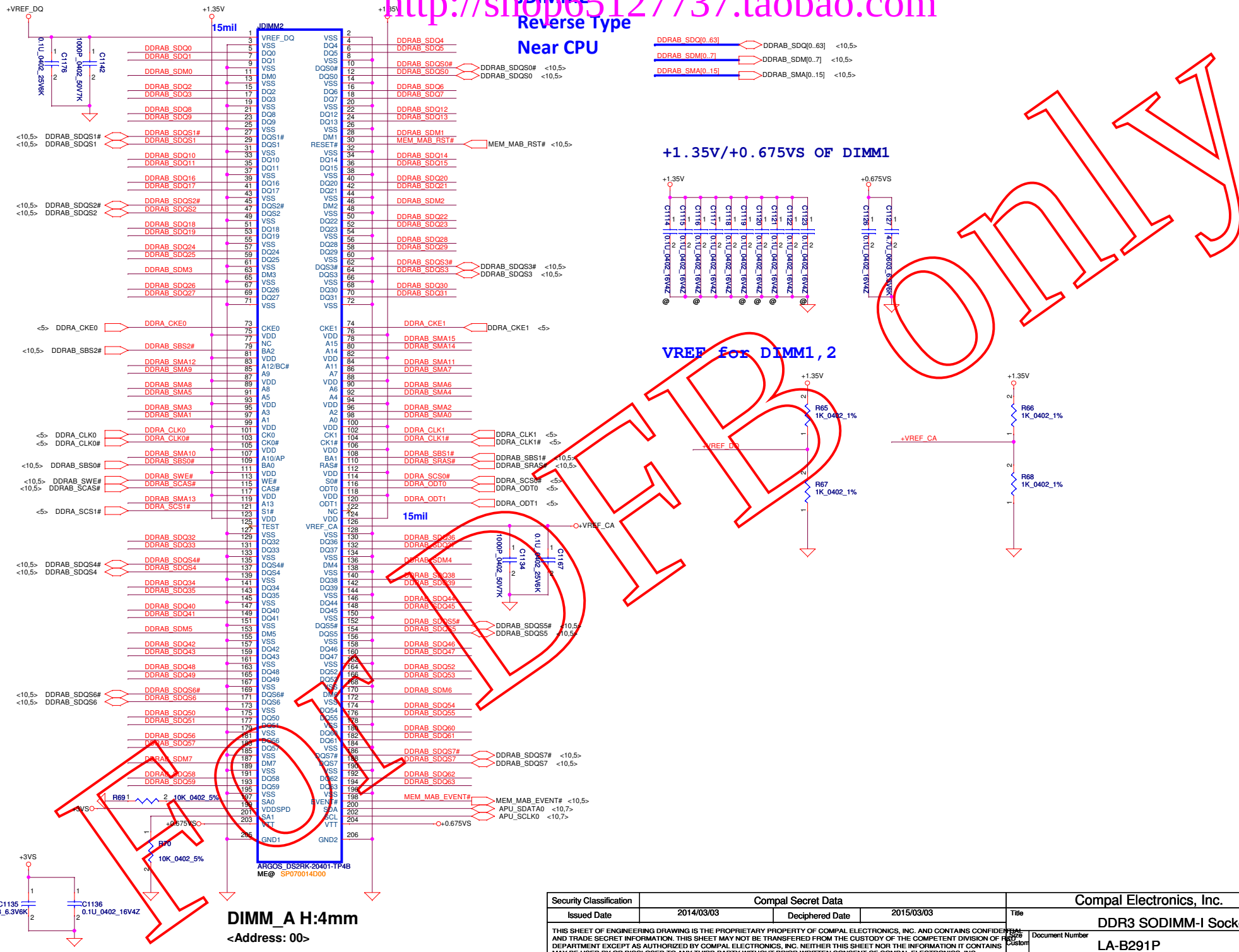

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date 2015/03/05	Title: DDR3 SODIMM-I Socket
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			Date: Monday, March 03, 2014; Sheet 9 of 46

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JDIMM1

Standard Type

Near User

15mil

+VREF_DQ

+1.35V

0.1U_0402_25V6K C1177

1000P_0402_50V7K C1143

JDIMM1

1	VREF_DQ	VSS	2				
3	VSS	DQ4	4	DDRAB_SDQ4			
5	DQ0	DQ5	6	DDRAB_SDQ5			
7	DQ1	VSS	8				
9	VSS	DQS0#	10	DDRAB_SDQS0#	DDRAB_SDQS0#	<5,9>	
11	DM0	DQS0	12	DDRAB_SDQS0	DDRAB_SDQS0	<5,9>	
13	VSS	VSS	14				
15	DQ2	DQ6	16	DDRAB_SDQ6			
17	DQ3	DQ7	18	DDRAB_SDQ7			
19	VSS	VSS	20				
21	DQ8	DQ12	22	DDRAB_SDQ12			
23	DQ9	DQ13	24	DDRAB_SDQ13			
25	VSS	VSS	26				
27	DQS1#	DM1	28	DDRAB_SDM1			
29	DQS1	RESET#	30	MEM_MAB_RST#	MEM_MAB_RST#	<5,9>	
31	VSS	VSS	32				
33	DQ10	DQ14	34	DDRAB_SDQ14			
35	DQ11	DQ15	36	DDRAB_SDQ15			
37	VSS	VSS	38				
39	DQ16	DQ20	40	DDRAB_SDQ20			
41	DQ17	DQ21	42	DDRAB_SDQ21			
43	VSS	VSS	44				
45	DQS2#	DM2	46	DDRAB_SDM2			
47	DQS2	VSS	48				
49	VSS	DQ22	50	DDRAB_SDQ22			
51	DQ18	DQ23	52	DDRAB_SDQ23			
53	DQ19	VSS	54				
55	VSS	DQ28	56	DDRAB_SDQ28			
57	DQ24	DQ29	58	DDRAB_SDQ29			
59	DQ25	VSS	60				
61	VSS	DQS3#	62	DDRAB_SDQS3#	DDRAB_SDQS3#	<5,9>	
63	DM3	DQS3	64	DDRAB_SDQS3	DDRAB_SDQS3	<5,9>	
65	VSS	VSS	66				
67	DQ26	DQ30	68	DDRAB_SDQ30			
69	DQ27	DQ31	70	DDRAB_SDQ31			
71	VSS	VSS	72				
73	CKE0	CKE1	74	DDRB_CKE1	DDRB_CKE1	<5>	
75	VDD	VDD	76				
77	NC	A15	78	DDRAB_SMA15			
79	BA2	A14	80	DDRAB_SMA14			
81	VDD	VDD	82				
83	A12/BC#	A11	84	DDRAB_SMA11			
85	A9	A7	86	DDRAB_SMA7			
87	VDD	VDD	88				
89	A8	A6	90	DDRAB_SMA6			
91	A5	A4	92	DDRAB_SMA4			
93	VDD	VDD	94				
95	A3	A2	96	DDRAB_SMA2			
97	A1	A0	98	DDRAB_SMA0			
99	VDD	VDD	100				
101	CK0	CK1	102	DDRB_CLK1	DDRB_CLK1	<5>	
103	CK0#	CK1#	104	DDRB_CLK1#	DDRB_CLK1#	<5>	
105	VDD	VDD	106				
107	A10/AP	BA1	108	DDRAB_SBS1#	DDRAB_SBS1#	<5,9>	
109	BA0	RAS#	110	DDRAB_SRAS#	DDRAB_SRAS#	<5,9>	
111	VDD	VDD	112				
113	WE#	S0#	114	DDRB_SCS0#	DDRB_SCS0#	<5>	
115	CAS#	ODT0	116	DDRB_ODT0	DDRB_ODT0	<5>	
117	VDD	VDD	118				
119	A13	ODT1	120	DDRB_ODT1	DDRB_ODT1	<5>	
121	S1#	NC	122				
123	VDD	VDD	124				
125	TEST	VREF_CA	126				
127	VSS	VSS	128				
129	DQ32	DQ36	130	DDRAB_SDQ36			
131	DQ33	DQ37	132	DDRAB_SDQ37			
133	VSS	VSS	134				
135	DQS4#	DM4	136	DDRAB_SDM4			
137	DQS4	VSS	138				
139	VSS	DQ38	140	DDRAB_SDQ38			
141	DQ34	DQ39	142	DDRAB_SDQ39			
143	DQ35	VSS	144				
145	VSS	DQ44	146	DDRAB_SDQ44			
147	DQ40	DQ45	148	DDRAB_SDQ45			
149	DQ41	VSS	150				
151	VSS	DQS5#	152	DDRAB_SDQS5#	DDRAB_SDQS5#	<5,9>	
153	DM5	DQS5	154	DDRAB_SDQS5	DDRAB_SDQS5	<5,9>	
155	VSS	VSS	156				
157	DQ42	DQ46	158	DDRAB_SDQ46			
159	DQ43	DQ47	160	DDRAB_SDQ47			
161	VSS	VSS	162				
163	DQ48	DQ52	164	DDRAB_SDQ52			
165	DQ49	DQ53	166	DDRAB_SDQ53			
167	VSS	VSS	168				
169	DQS6#	DM6	170	DDRAB_SDM6			
171	DQS6	VSS	172				
173	VSS	DQ54	174	DDRAB_SDQ54			
175	DQ50	DQ55	176	DDRAB_SDQ55			
177	DQ51	VSS	178				
179	VSS	DQ60	180	DDRAB_SDQ60			
181	DQ56	DQ61	182	DDRAB_SDQ61			
183	DQ57	VSS	184				
185	VSS	DQS7#	186	DDRAB_SDQS7#	DDRAB_SDQS7#	<5,9>	
187	DM7	DQS7	188	DDRAB_SDQS7	DDRAB_SDQS7	<5,9>	
189	VSS	VSS	190				
191	DQ58	DQ62	192	DDRAB_SDQ62			
193	DQ59	DQ63	194	DDRAB_SDQ63			
195	VSS	VSS	196				
197	SA0	EVENT#	198	MEM_MAB_EVENT#	MEM_MAB_EVENT#	<5,9>	
199	VDDSPD	SDA	200	APU_SDATA0	APU_SDATA0	<7,9>	
201	SA1	SCL	202	APU_SCLK0	APU_SCLK0	<7,9>	
203	VTT	VTT	204	+0.675VS			
205	GND1	GND2	206				
207	BOSS1	BOSS2	208				

ARGOS_DS2SK-20401-TP4B

ME@

SP070014E00

15mil

VREF_CA

0.1U_0402_25V6K C1139

1000P_0402_50V7K C1124

R71 10K_0402_5%

+3VS

R72 10K_0402_5%

+0.675VS

DDRAB_SDQ[0..63] → DDRAB_SDQ[0..63] <5,9>

DDRAB_SDM[0..7] → DDRAB_SDM[0..7] <5,9>

DDRAB_SMA[0..15] → DDRAB_SMA[0..15] <5,9>

+1.35V/+0.675VS OF DIMM2

+1.35V

C1133 0.1U_0402_16V4Z @

C1155 0.1U_0402_16V4Z

C1132 0.1U_0402_16V4Z @

C1162 0.1U_0402_16V4Z

C1165 0.1U_0402_16V4Z @

C1168 0.1U_0402_16V4Z

C1169 0.1U_0402_16V4Z @

C1170 0.1U_0402_16V4Z

C1171 0.1U_0402_16V4Z @

C1172 0.1U_0402_16V4Z @

+0.675VS

C1175 0.1U_0402_16V4Z

C1158 4.7U_0603_6.3V6K

+1.35V

C250 330U_D3_2.5VY_R6M @

FOLDED ONLY

DIMM_B H:4mm

<Address: 10>

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Compal Electronics, Inc.

Title: DDR3 SODIMM-II Socket

Size	Document Number	Rev
Custom	LA-B291P	1.0

Date: Monday, March 03, 2014 Sheet 10 of 46

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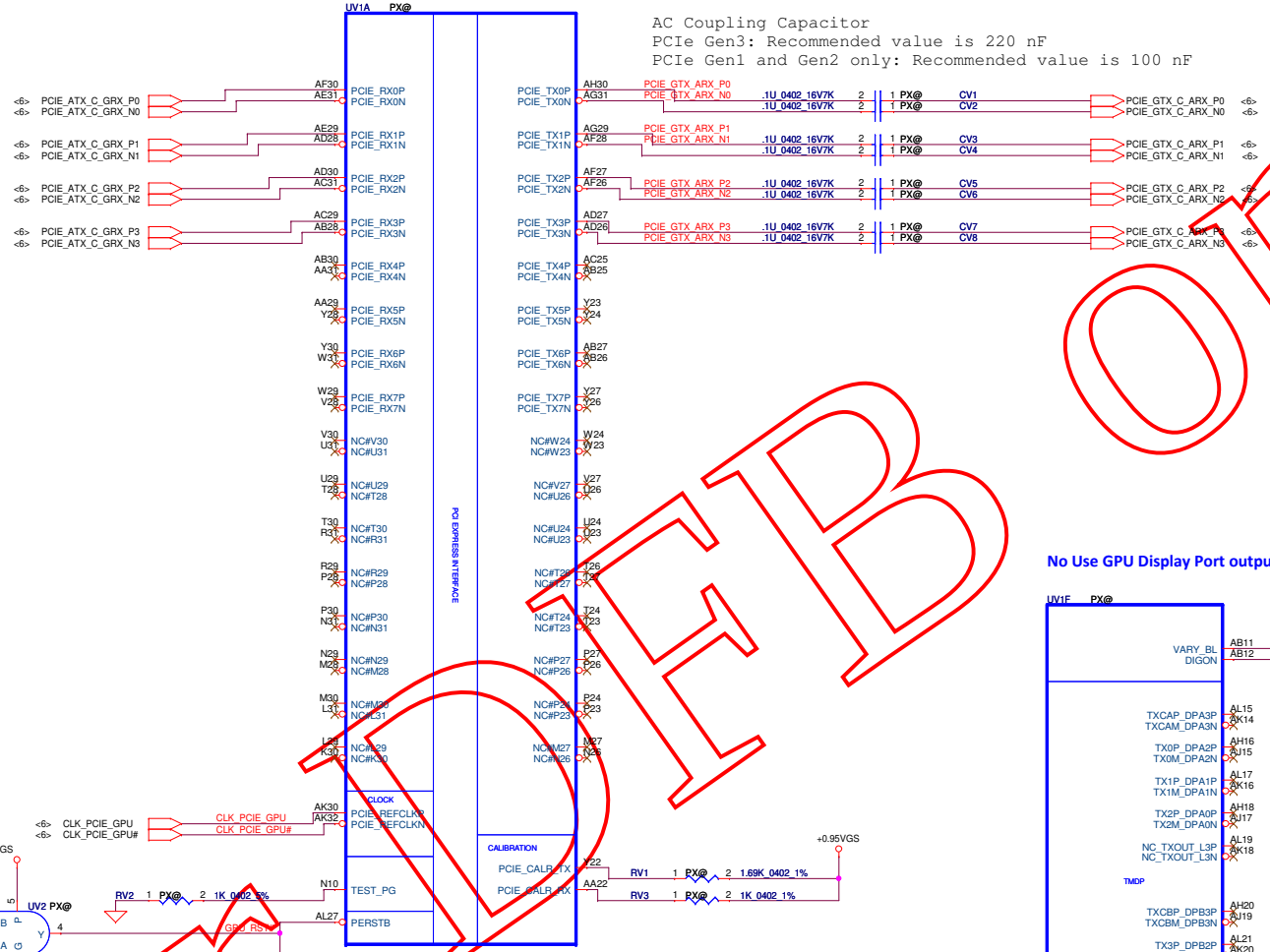
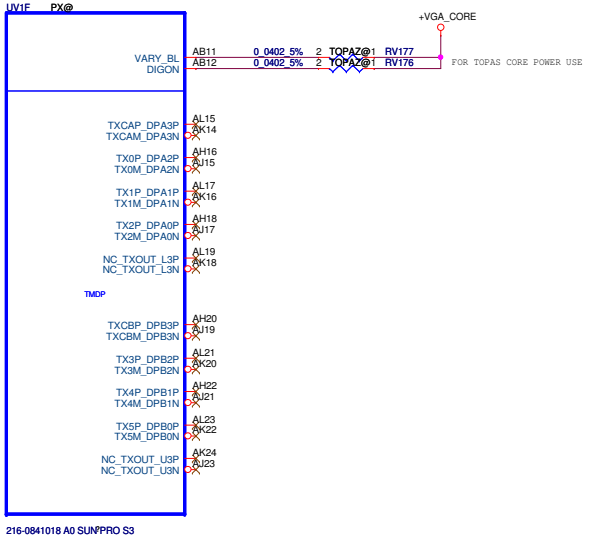
AC Coupling Capacitor
PCIe Gen3: Recommended value is 220 nF
PCIe Gen1 and Gen2 only: Recommended value is 100 nF



No Use GPU Display Port outpud



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Compal Electronics, Inc.

Title: JET/TOPAL(1/5)_PCIE/DP

Size: Custom | Document Number: LA-B291P | Rev: 1.0

Date: Monday, March 03, 2014 | Sheet 11 of 46

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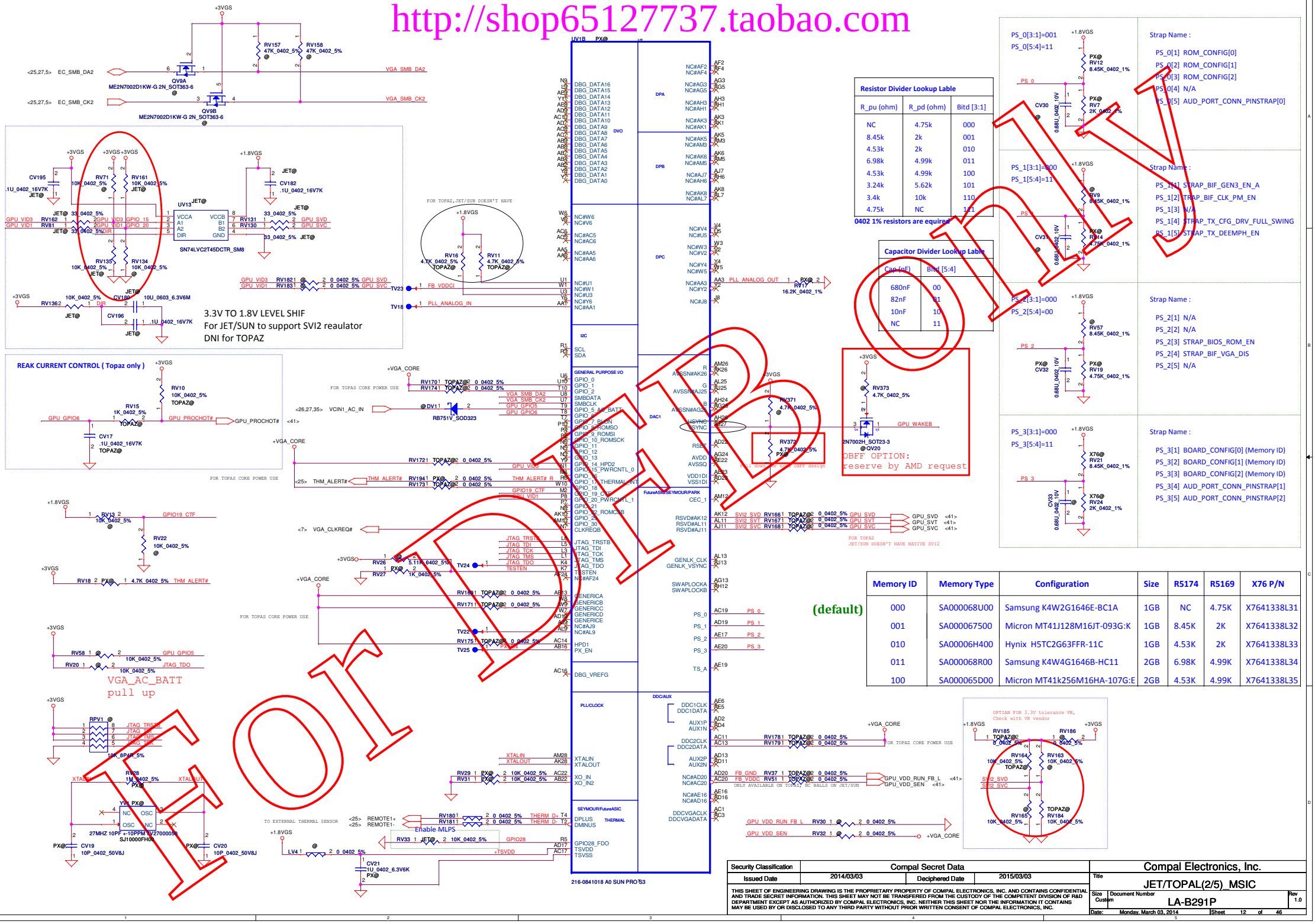

Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

Memory ID	Memory Type	Configuration	Size	R5174	R5169	X76 P/N
000	SA000068U00	Samsung K4W2G1646E-BC1A	1GB	NC	4.75K	X7641338L31
001	SA000067500	Micron MT41J128M16JT-093G:K	1GB	8.45K	2K	X7641338L32
010	SA00006H400	Hynix H5TC2G63FFR-11C	1GB	4.53K	2K	X7641338L33
011	SA000068R00	Samsung K4W4G1646B-HC11	2GB	6.98K	4.99K	X7641338L34
100	SA000065D00	Micron MT41k256M16HA-107G:E	2GB	4.53K	4.99K	X7641338L35

(default)

FOR QUOTE ONLY

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	JET/TOPAL(2/5)_MSIC
Size: Custom	Document Number: LA-B291P
Rev	1.0
Date: Monday, March 03, 2014	Sheet 12 of 46

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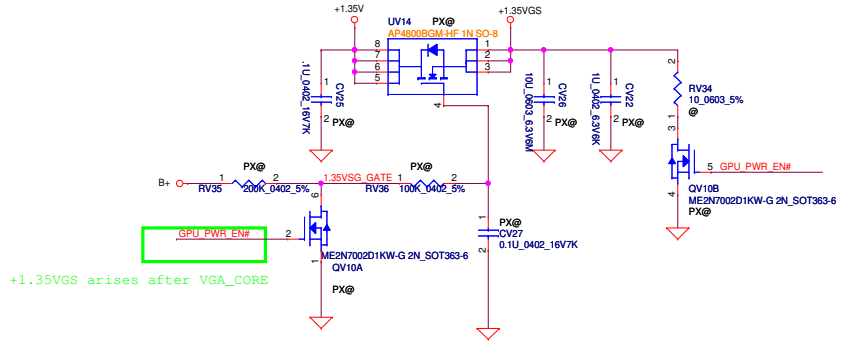
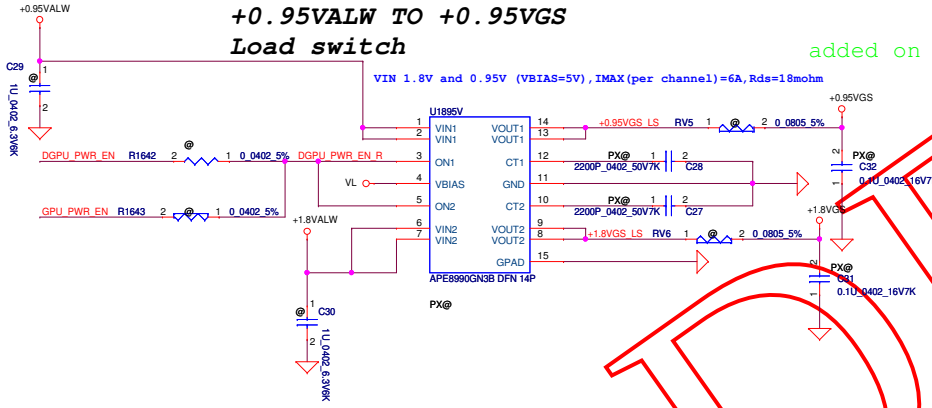
+1.35VS to +1.35VGS

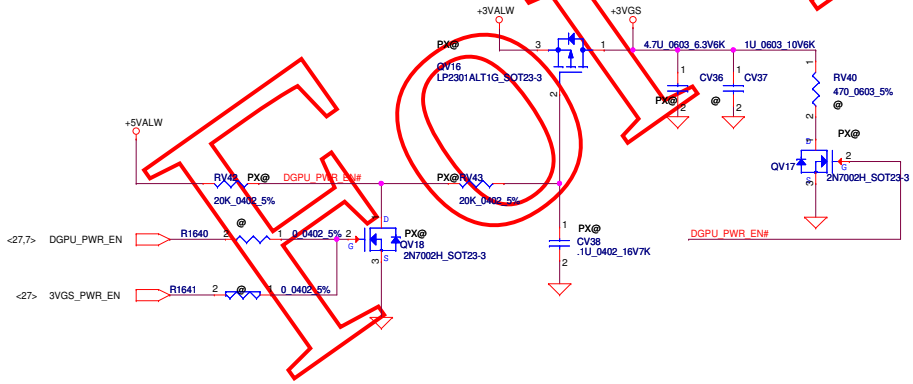


+1.8VALW TO +1.8VGS
+0.95VALW TO +0.95VGS
Load switch

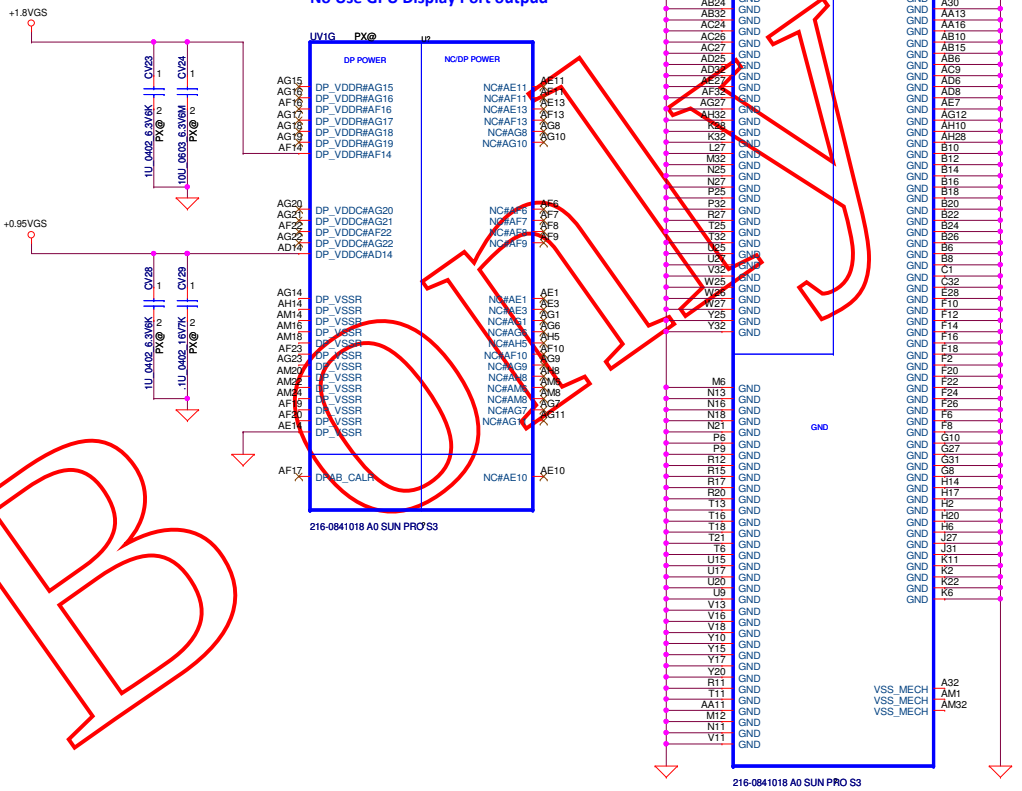
added on 9/28

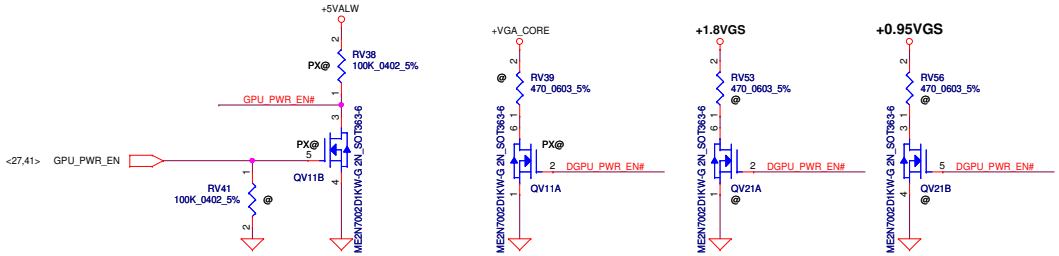


+3VS to +3VS_VGA



No Use GPU Display Port outpud





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Compal Electronics, Inc.

Title: JET/TOPAL(3/5)_PWR/GND

Size: Custom | Document Number: LA-B291P | Rev: 1.0

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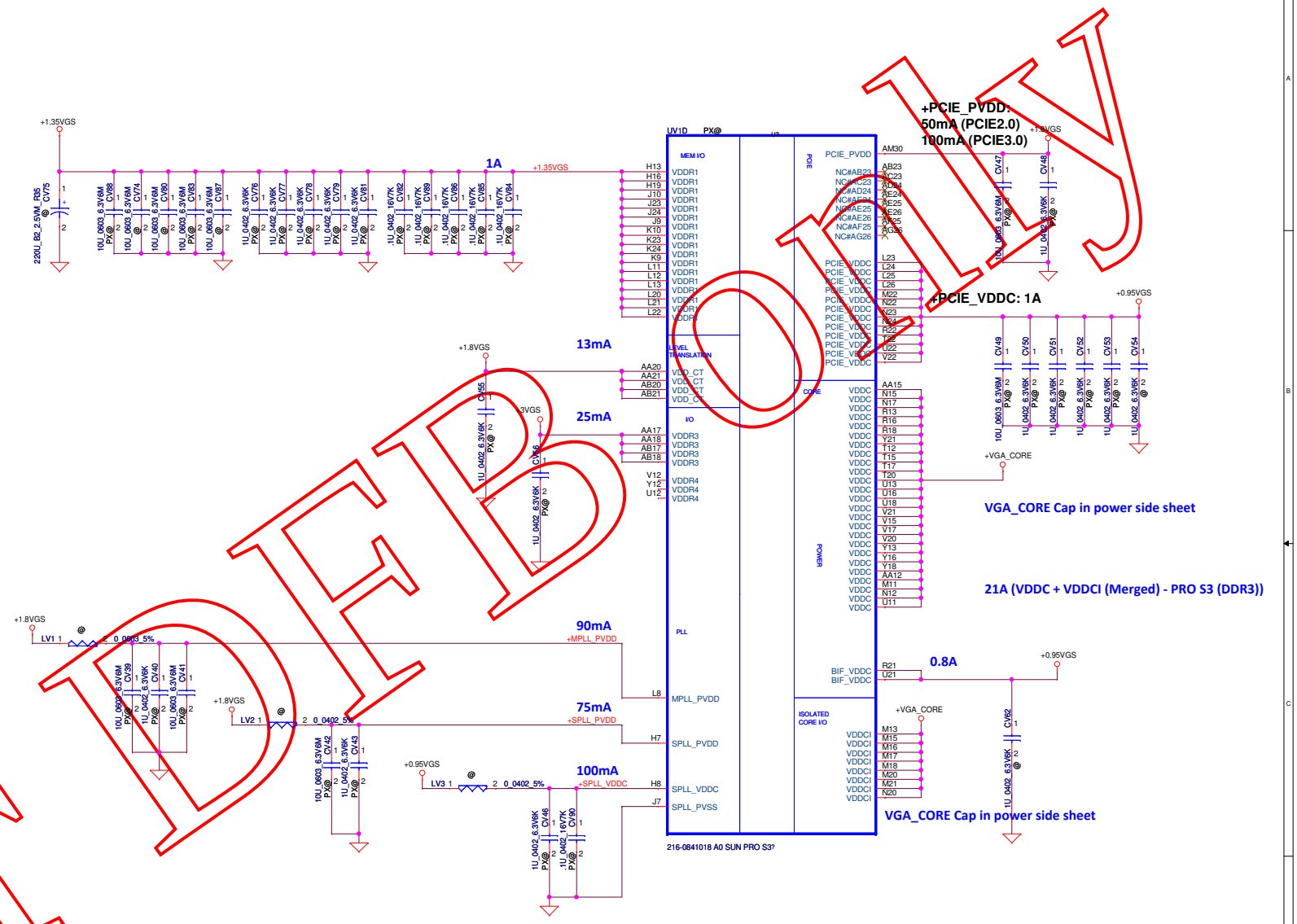
+VGA_CORE		10uF	2.2uF	1uF	0.1uF
VDDC	TBD	7	16	4	3
VDDCI	3.5A				

+0.95VGS		10uF	1uF	0.1uF
PCIE_VDDC	1A	1	5(1@)	0
BIF_VDDC	0.8A	0	1(1@)	0
SPLL_VDDC	100mA	0	1	1

+1.35VGS		10uF	1uF	0.1uF	0.01uF
VDDR1	1.5A	5(3@)	5	5	0

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	0
MPLL_PVDD	130mA	2	1	0
SPLL_PVDD	75mA	0	1	0
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	0	1	0
+TSVDD	13mA	0	1	0
+DP_VDDR		1	1	0
+DP_VDDC		0	1	1

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	1	0



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Issued Date	2014/03/03	Deciphered Date	2015/03/03

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Compal Electronics, Inc.

Title: JET/TOPAL(4/5)_PWR

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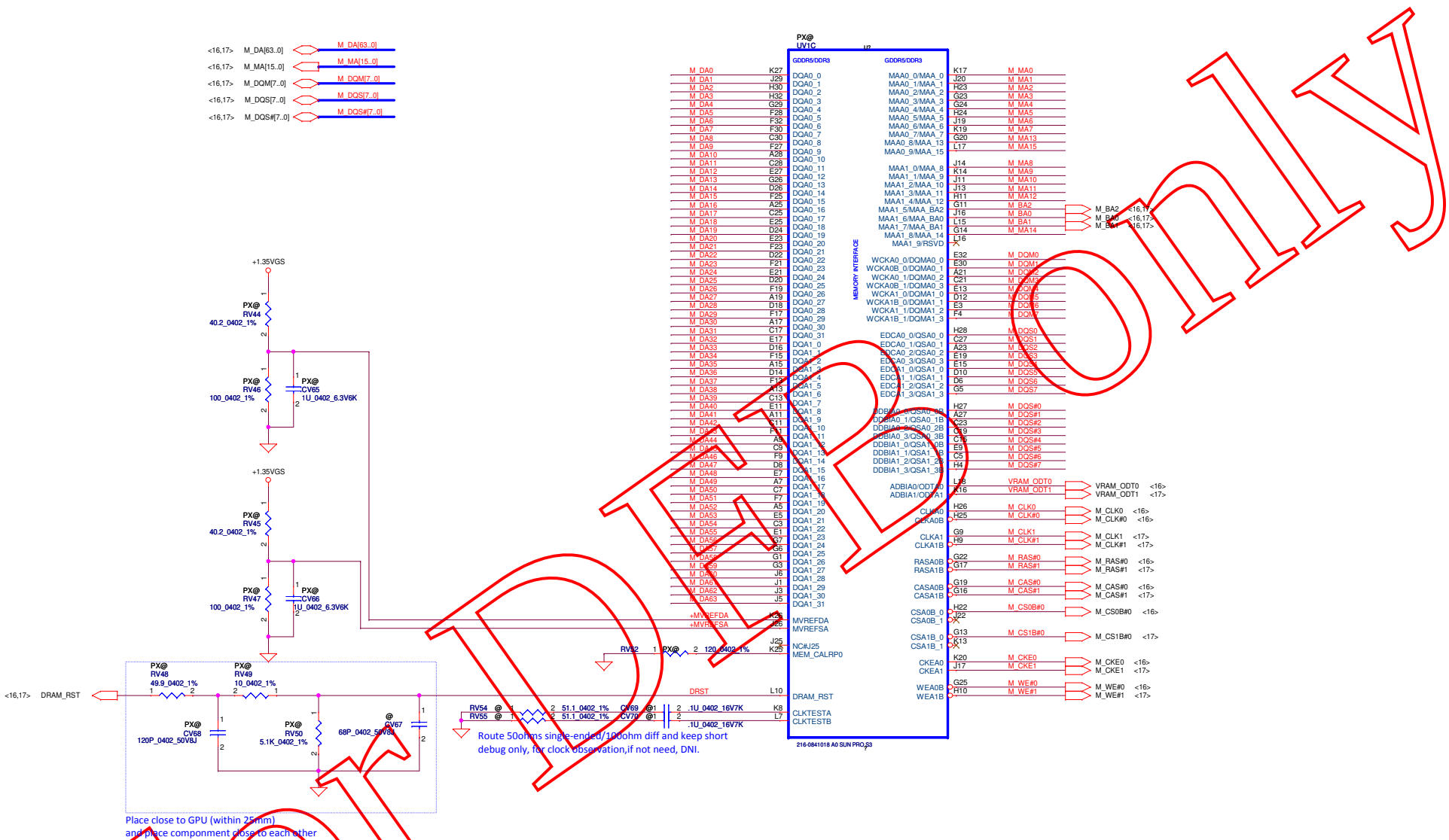

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Compal Electronics, Inc.

Title: JET/TOPAL(5/5)_MEM

Size	Document Number	Rev
Custom	LA-B291P	1.0

Date: Monday, March 03, 2014 Sheet 15 of 46

DDR3L Memory Channel Rank 0:A0

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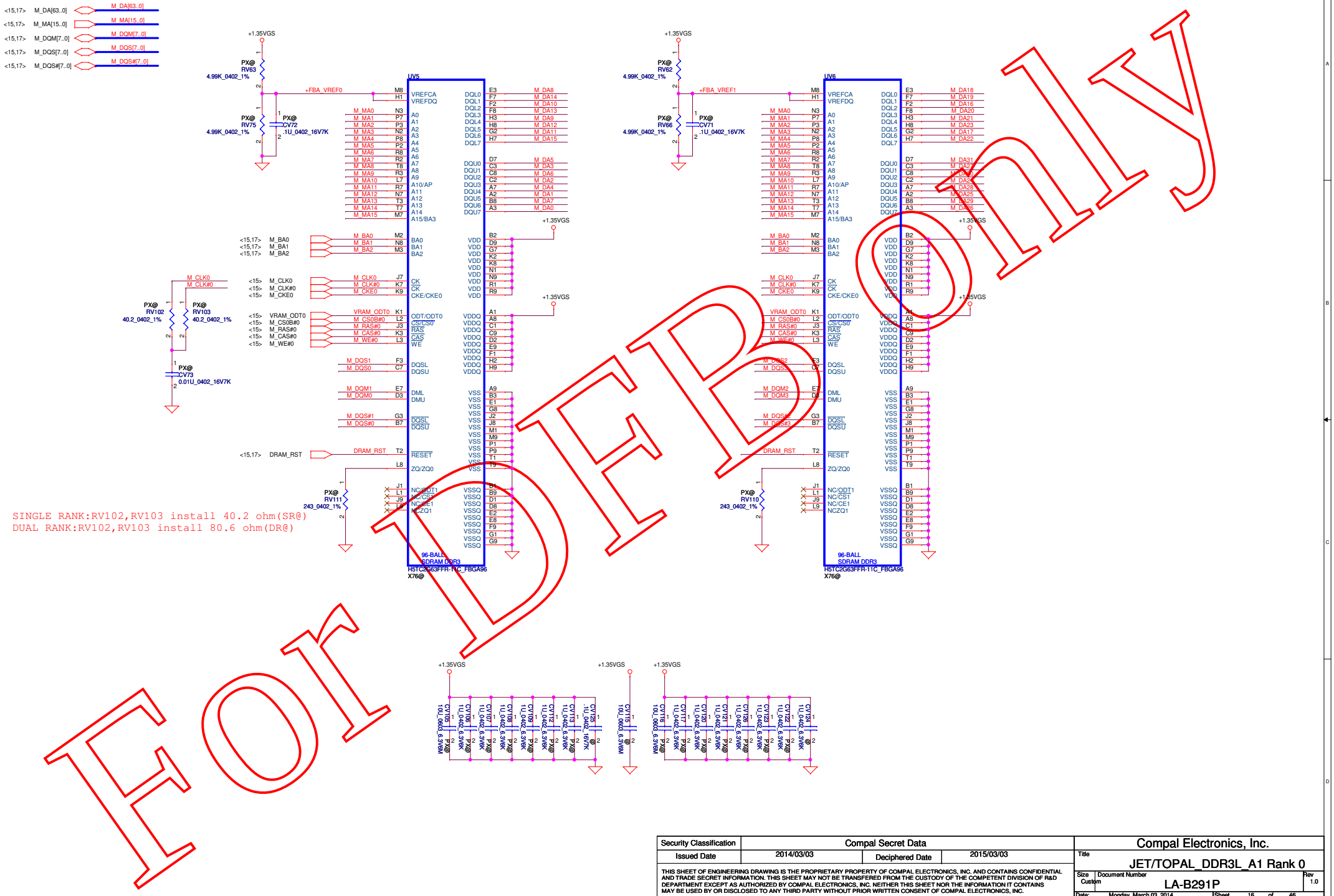

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Compal Electronics, Inc.	
Title	JET/TOPAL_DDR3L_A1 Rank 0
Size: Custom	Document Number: LA-B291P
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Date: Monday, March 03, 2014	Sheet 16 of 46

DDR3L Memory Channel Rank 0:A1

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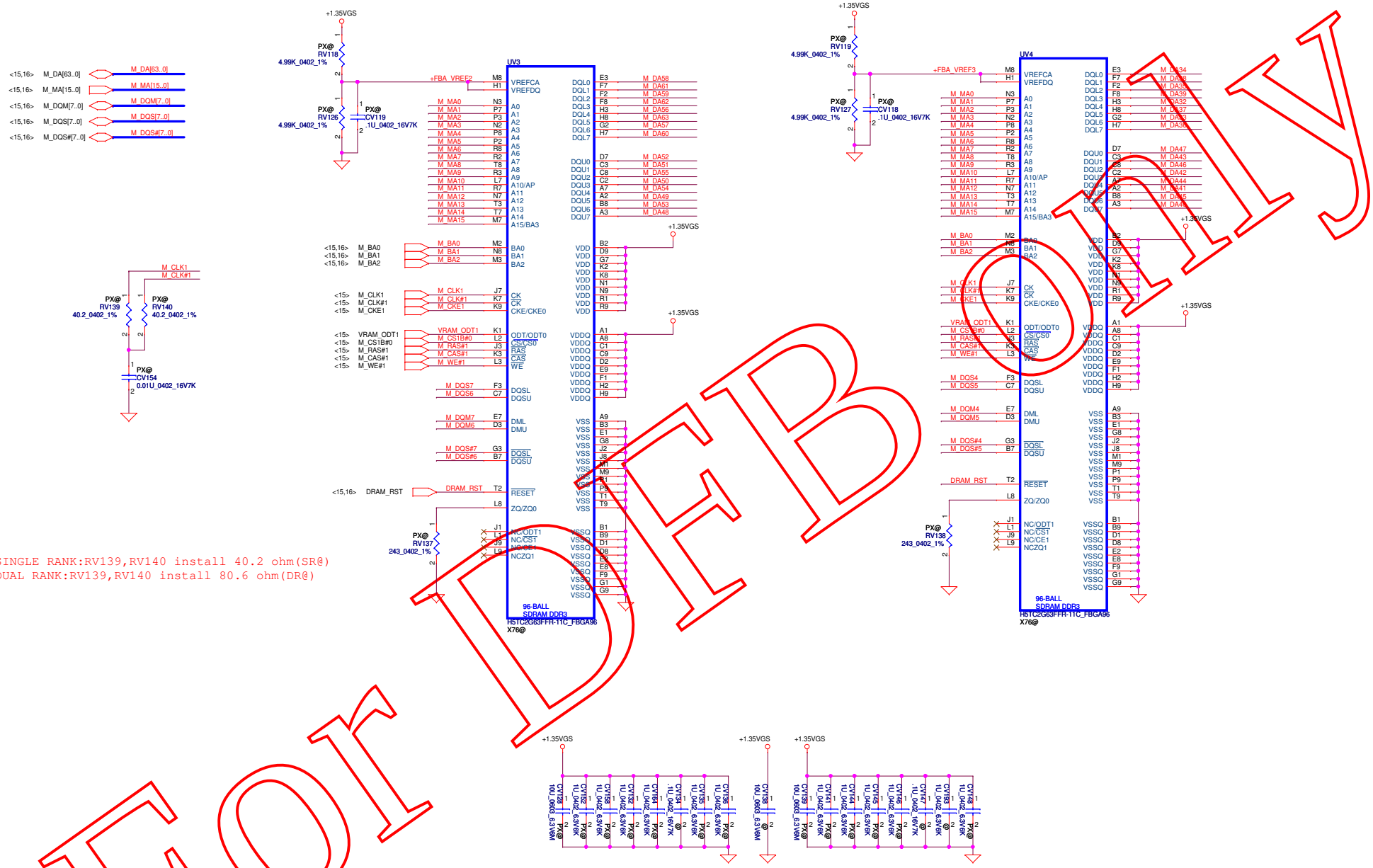

SINGLE RANK:RV139,RV140 install 40.2 ohm(SR@)
DUAL RANK:RV139,RV140 install 80.6 ohm(DR@)

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Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

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Compal Electronics, Inc.

Title: JET/TOPAL_DDR3L_A2 Rank 0

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Size: A	Document Number: LA-B291P	Rev: 1.0
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Title: Reserved		
Size: A	Document Number: LA-B291P	Rev: 1.0
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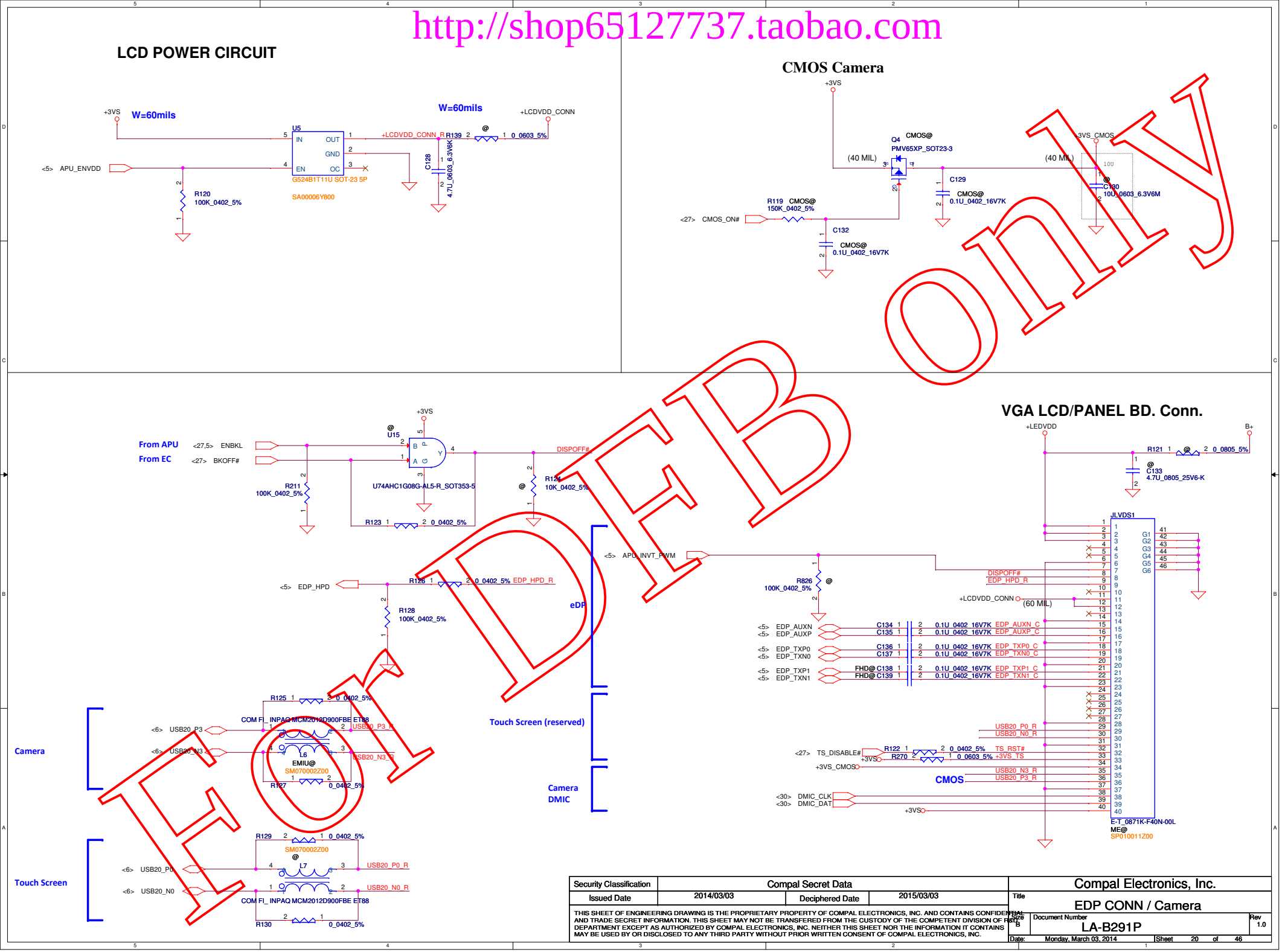

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Issued Date	2014/03/03	Deciphered Date	2015/03/03

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Compal Electronics, Inc.

Title: EDP CONN / Camera

Size: B | Document Number: LA-B291P | Rev: 1.0

Date: Monday, March 03, 2014 | Sheet 20 of 46

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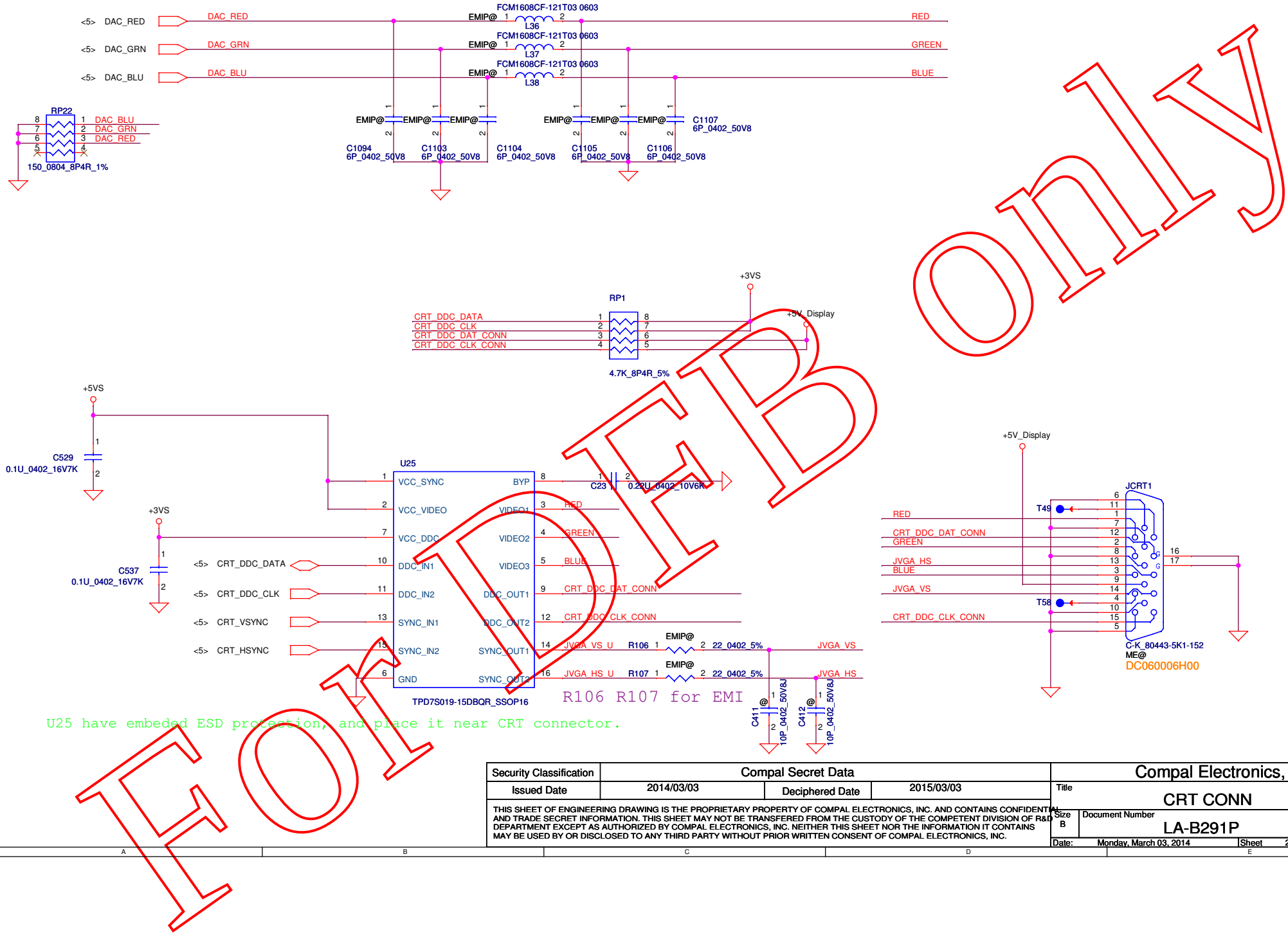

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Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

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Compal Electronics, Inc.

Title: CRT CONN

Size	Document Number	Rev
B	LA-B291P	1.0

Date: Monday, March 03, 2014 Sheet 21 of 46

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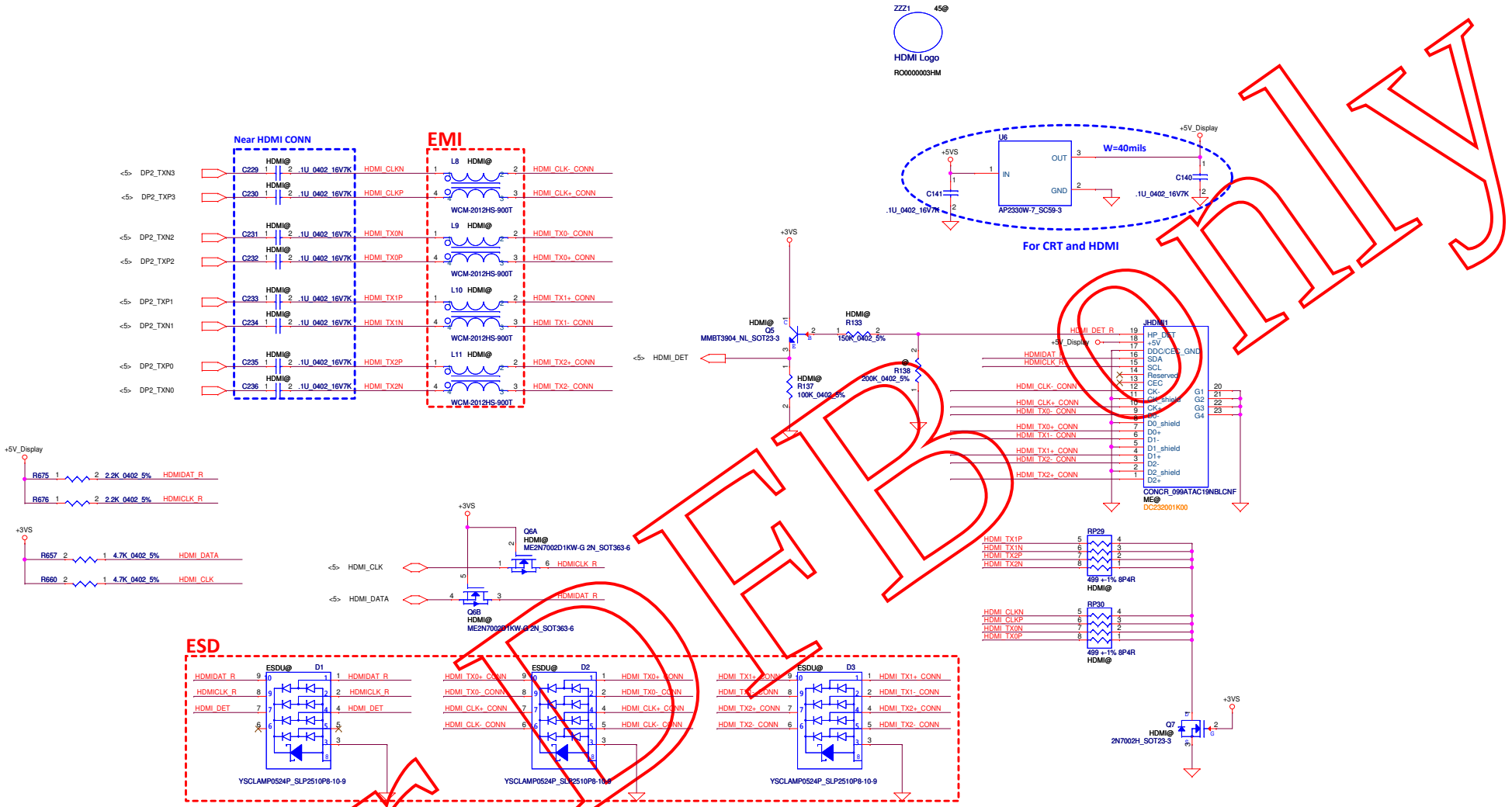

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03
Title	HDMI CONN		
Size C	Document Number LA-B291P		Rev 1.0
Date: Monday, March 03, 2014	Sheet 22 of 46		

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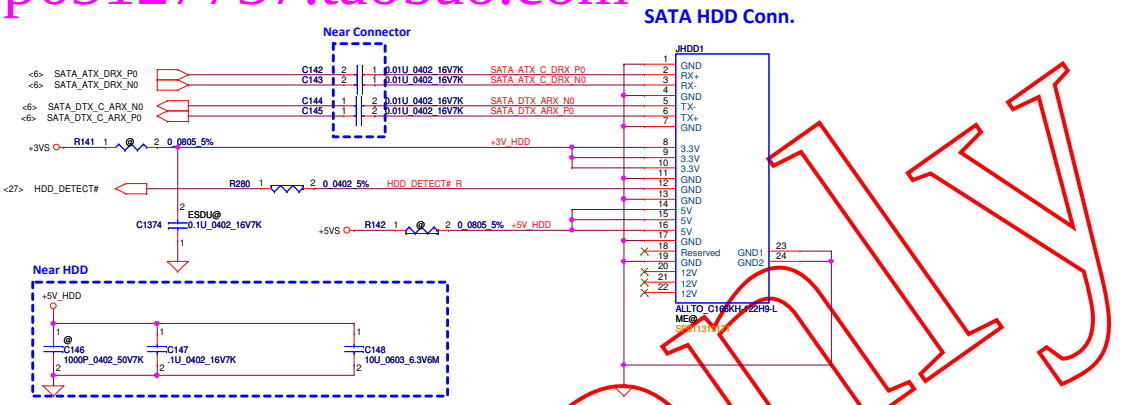
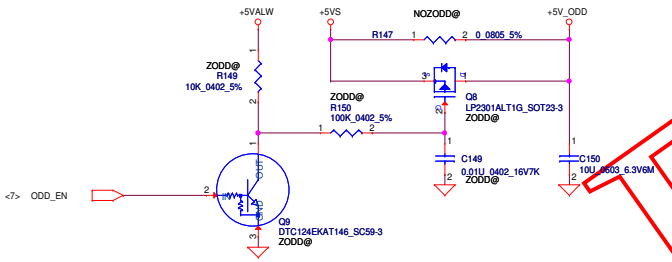
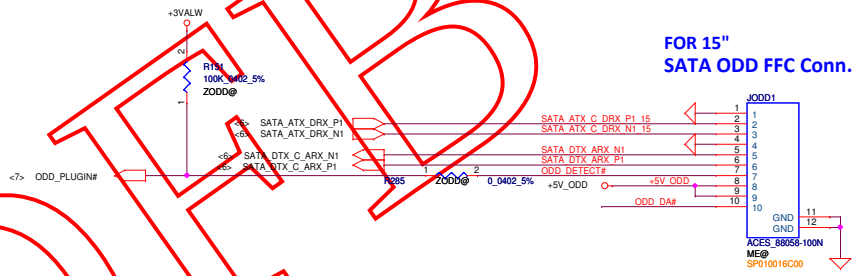
HDD

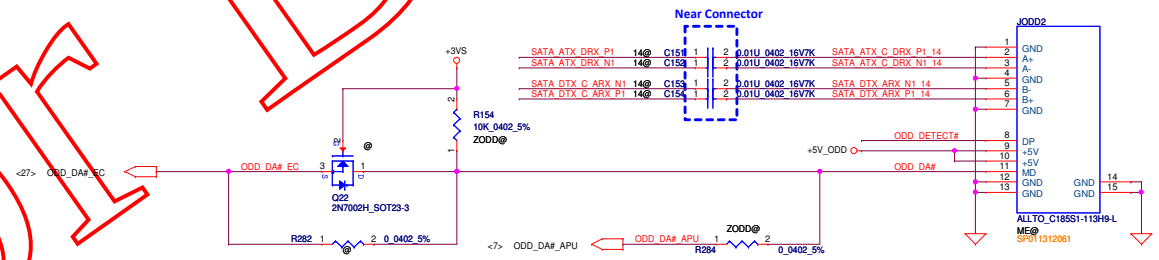


ODD

ODD Power Control







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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03
Title	HDD/ODD		
Size C	Document Number LA-B291P		Rev 1.0
Date: Monday, March 03, 2014	Sheet 23 of 46		

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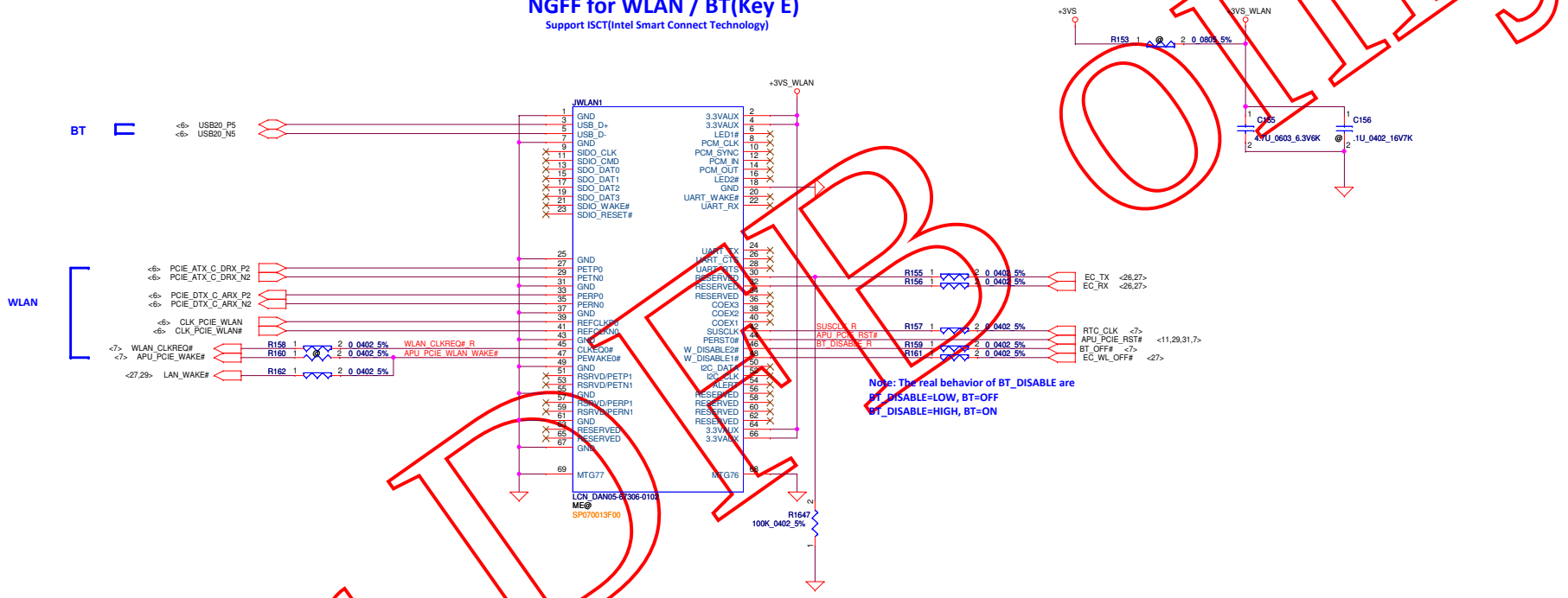
NGFF for WLAN / BT(Key E)

Support ISCT(Intel Smart Connect Technology)



For DTB Only

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03
Title	NGFF WLAN/BT		
Size C	Document Number LA-B291P		Rev 1.0
Date: Monday, March 03, 2014	Sheet 24 of 46		

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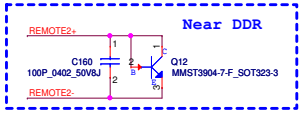
3 Channel



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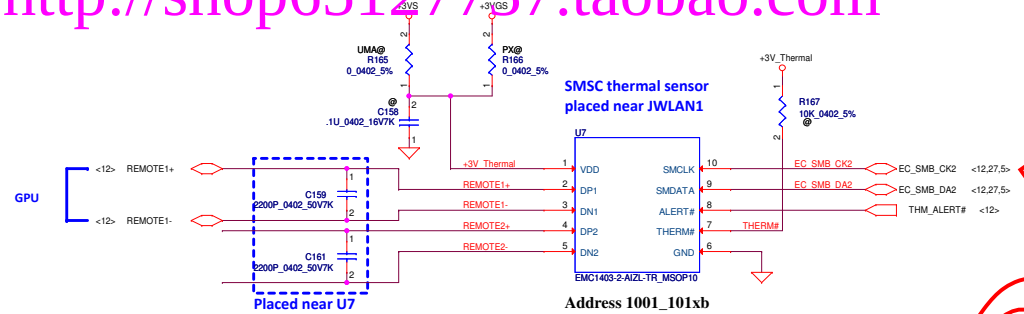
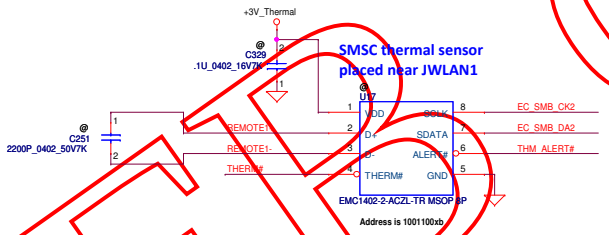
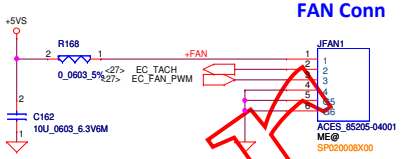
Trace length:<8"

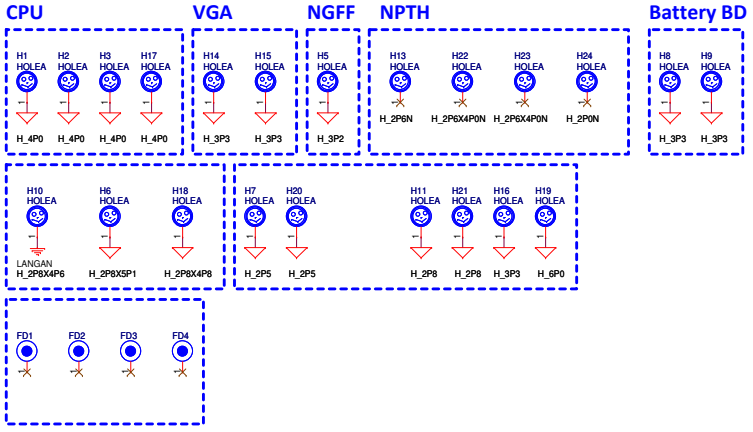


2 Channel



FAN Conn





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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03
Title	EMC1403-2/FAN/Screw Hole		
Size C	Document Number LA-B291P		Rev 1.0
Date: Monday, March 03, 2014	Sheet 25 of 46		

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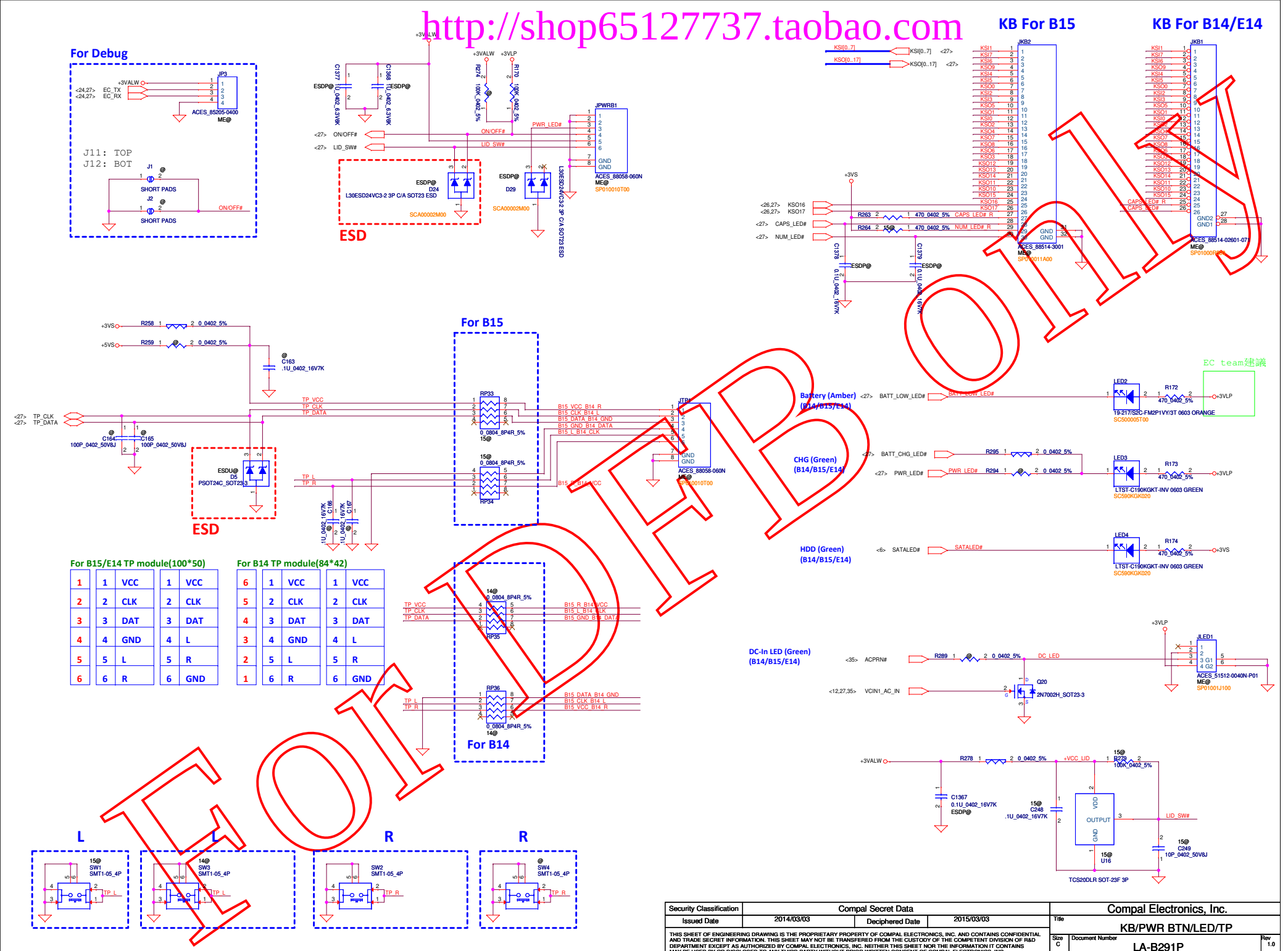

1	1	VCC	1	VCC	
2	2	CLK	2	CLK	
3	3	DAT	3	DAT	
4	4	GND	4	L	
5	5	L	5	R	
6	6	R	6	GND	

6	1	VCC	1	VCC	
5	2	CLK	2	CLK	
4	3	DAT	3	DAT	
3	4	GND	4	L	
2	5	L	5	R	
1	6	R	6	GND	

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Issued Date	2014/03/03	Deciphered Date	2015/03/03

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Compal Electronics, Inc.			
Title	KB/PWR BTN/LED/TP		
Size C	Document Number LA-B291P		Rev 1.0
Date: Monday, March 03, 2014	Sheet 26 of 46		

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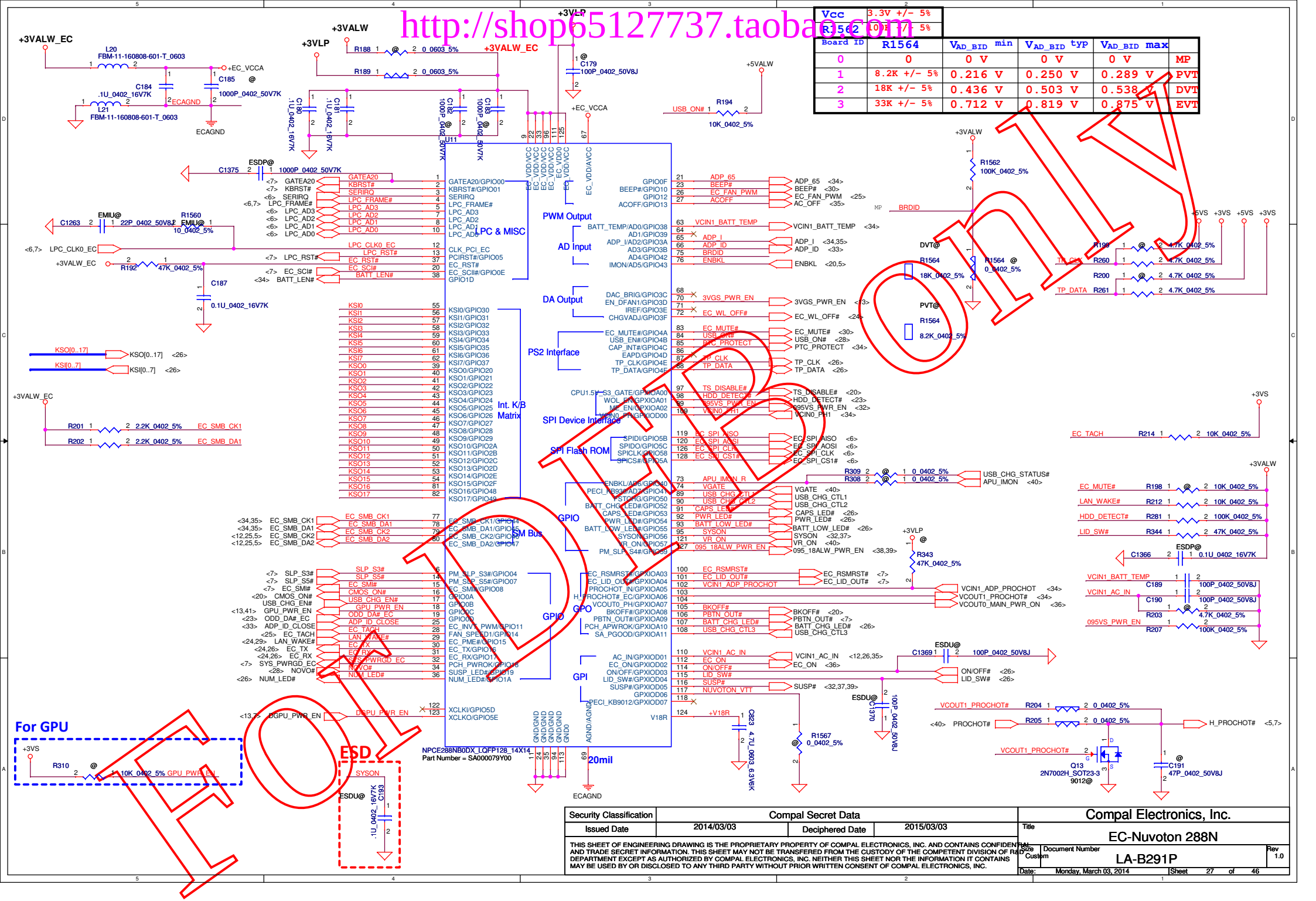
Vcc	3.3V +/- 5%
R1562	100K +/- 5%

Board ID	R1564	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT



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Compal Electronics, Inc.

Title: EC-Nuvoton 288N

Size: Custom | Document Number: LA-B291P | Rev: 1.0

Date: Monday, March 03, 2014 | Sheet 27 of 46

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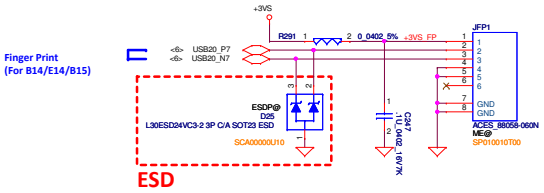
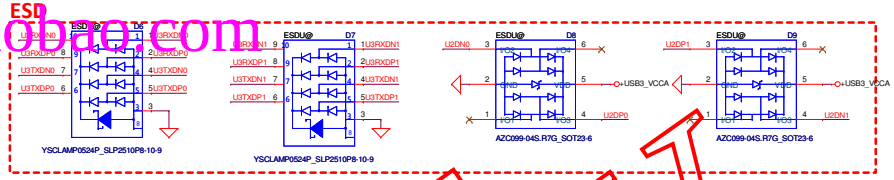
Finger Print

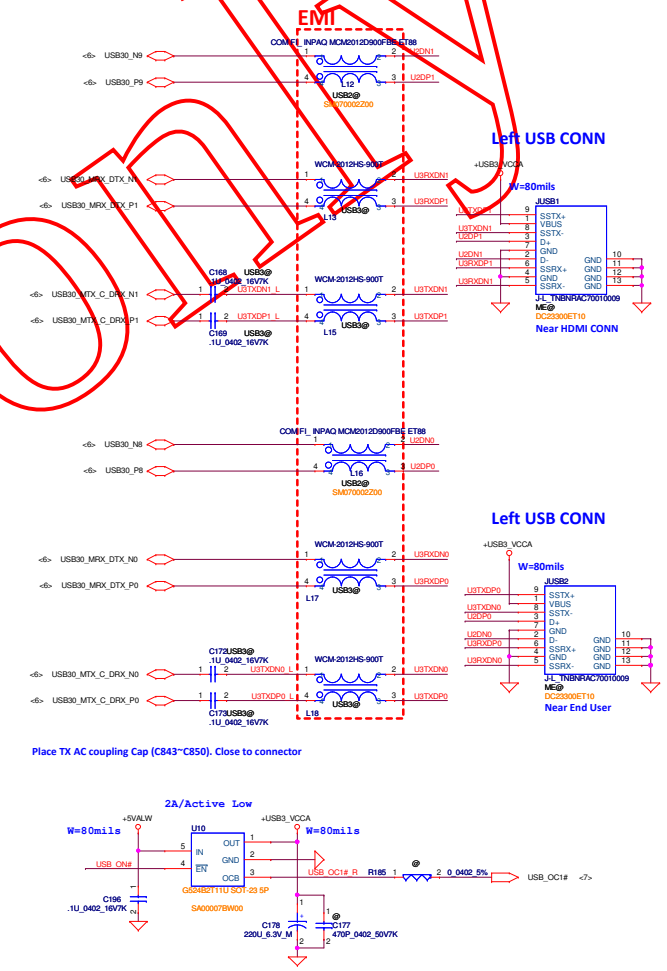


ESD

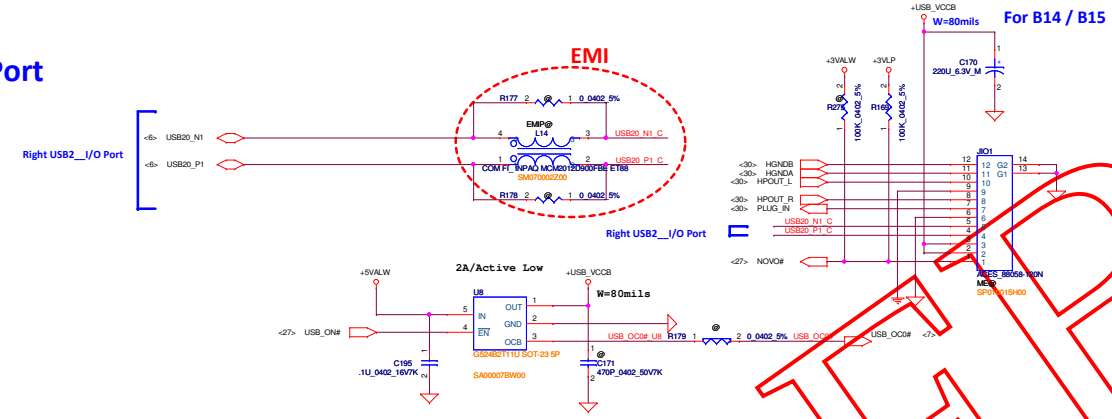


ESD protection needs to be placed near connector side

USB3.0_Port



USB2.0_Port



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Issued Date	2014/03/03	Deciphered Date	2015/03/03
			Title: USB Port/FP
			Size: Custom; Document Number: LA-B291P; Rev: 1.0
			Date: Monday, March 03, 2014; Sheet 28 of 46

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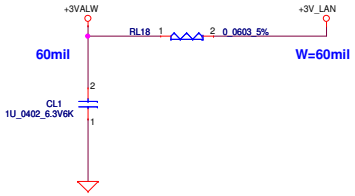
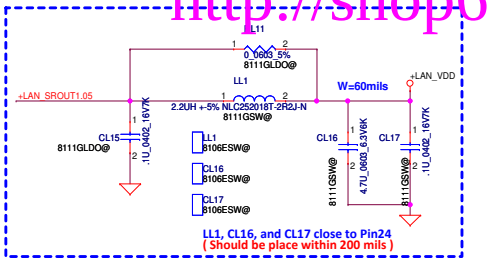
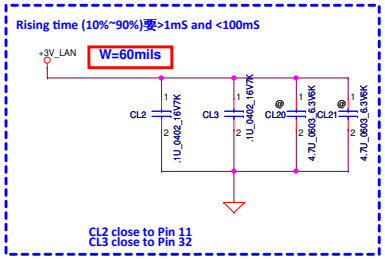
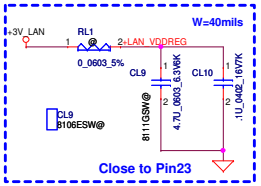


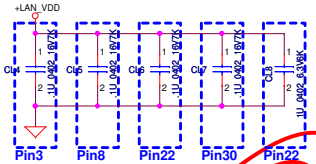


		1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
SA00005V700	RTL8111G	LDO	X	X	X	O	O
	~~RTL8111G~~	~~External~~	~~X~~	~~X~~	~~X~~	~~X~~	~~O~~
	RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
SA00006Y00	RTL8106E	LDO	X	X	X	X	X

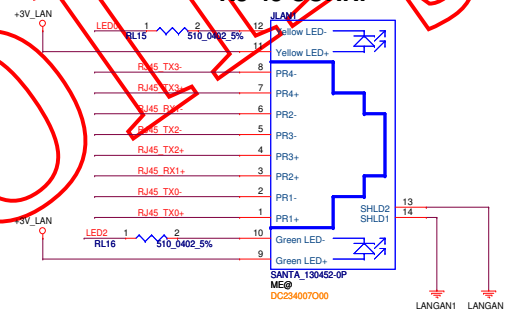
Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.







RJ-45 CONN.



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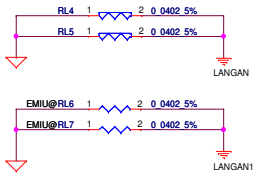

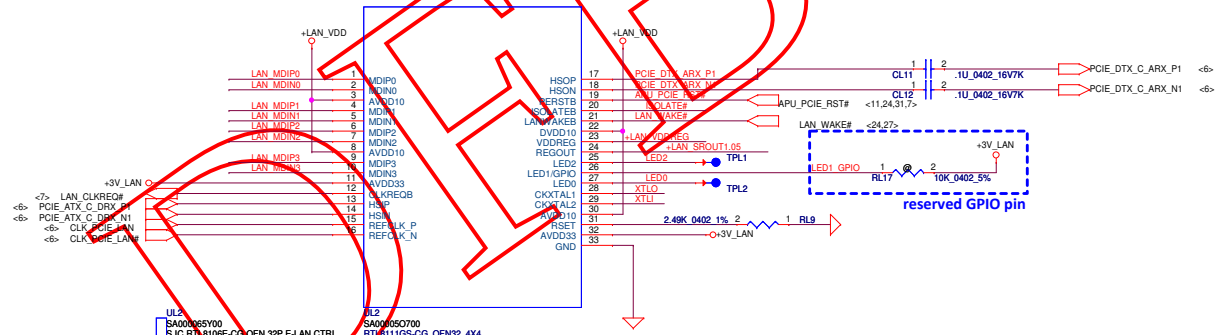

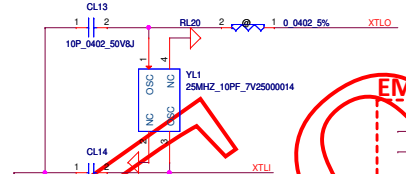

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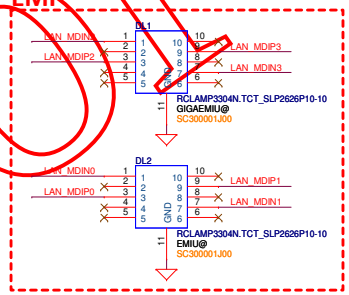

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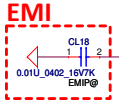

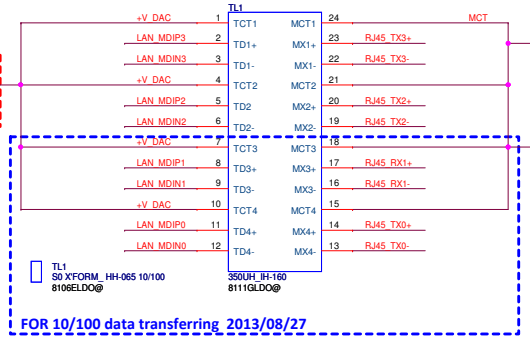

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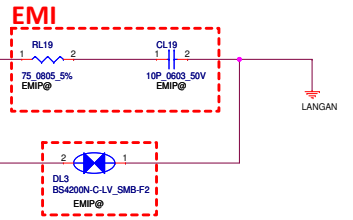

EMI

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Title	LAN_RTL8111G/RTL8106E		
Size C	Document Number LA-B291P		Rev 1.0
Date: Monday, March 03, 2014		Sheet 29 of 46	

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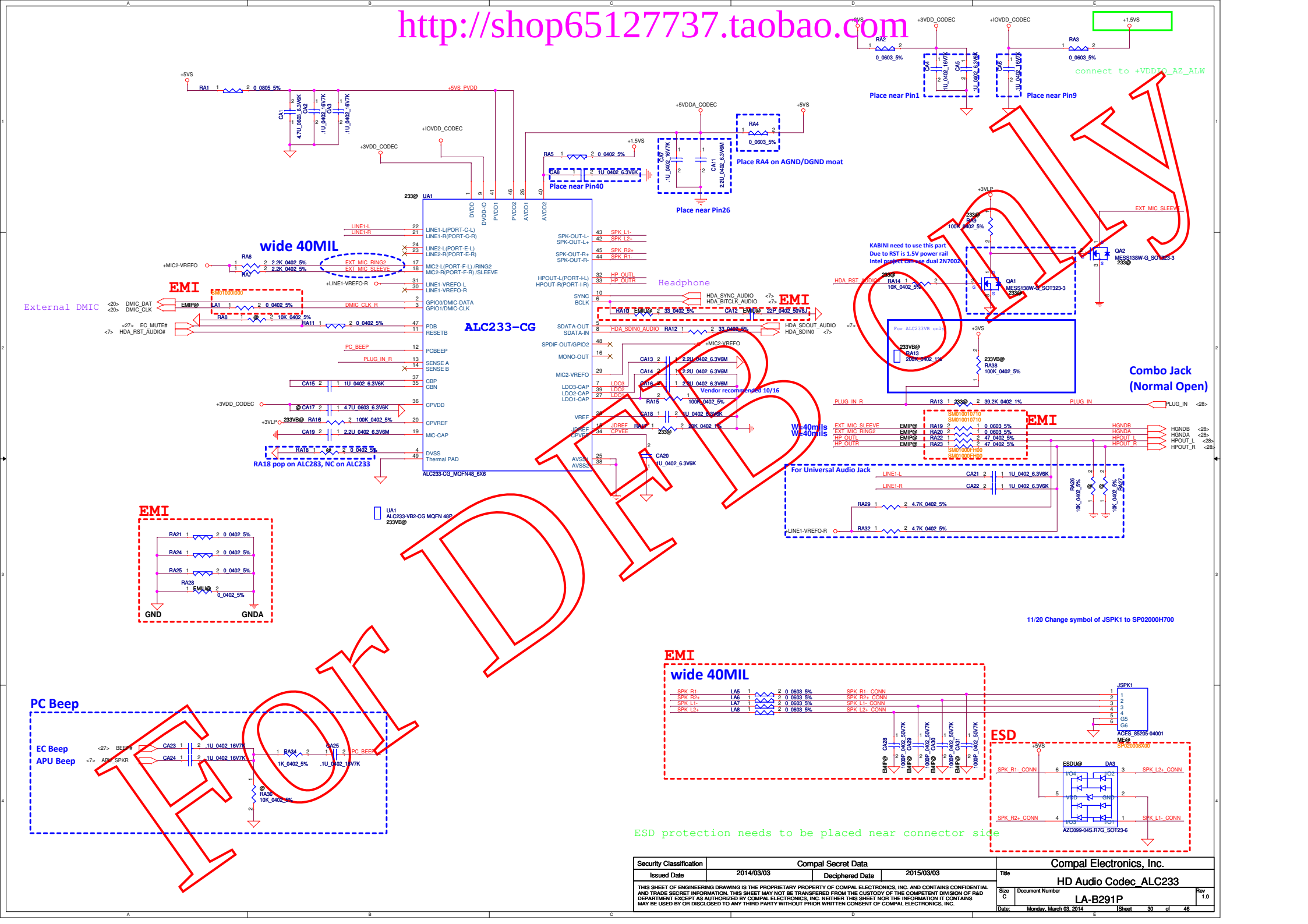

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Issued Date	2014/03/03	Deciphered Date	2015/03/03

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Compal Electronics, Inc.	
Title	HD Audio Codec_ALC233
Size: C	Document Number: LA-B291P
Rev: 1.0	
Date: Monday, March 03, 2014	Sheet 30 of 46

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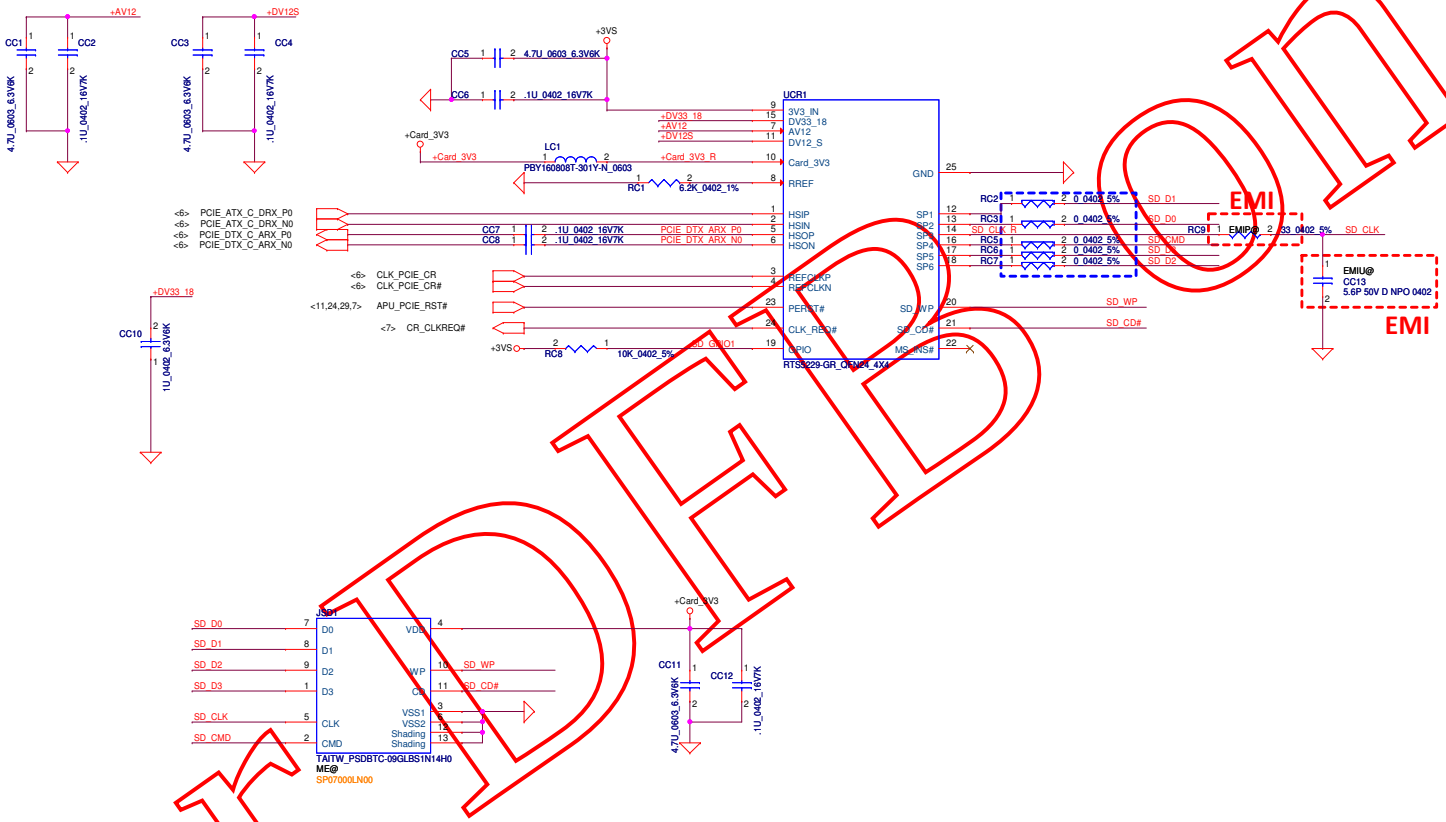

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Title	Card Reader RTS5229		
Size C	Document Number LA-B291P		Rev 1.0
Date: Monday, March 03, 2014		Sheet 31 of 46	

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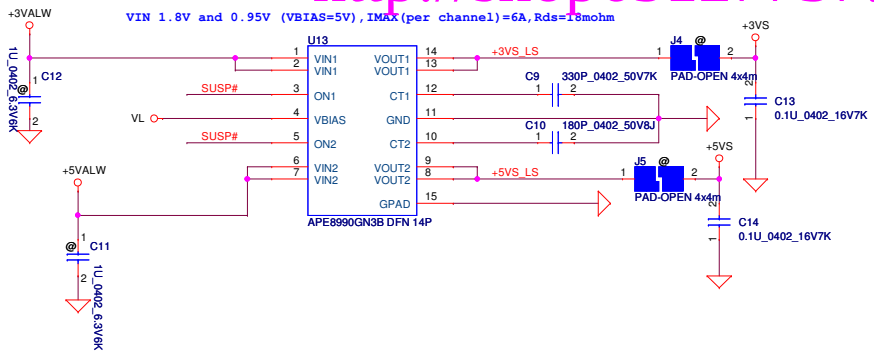
+5VALW TO +5VS
+3VALW TO +3VS
Load switch

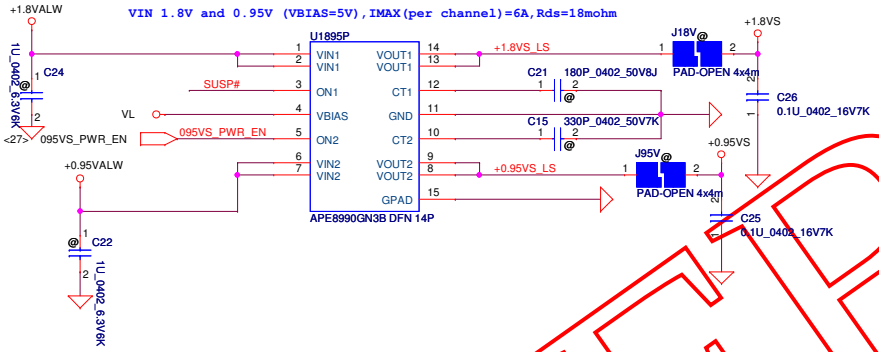
VIN 5V and 3.3V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm

VIN 1.8V and 0.95V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm

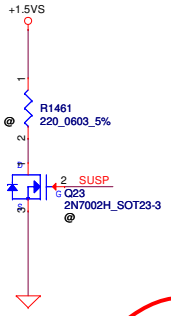


+1.8VALW TO +1.8VS
+0.95VALW TO +0.95VS
Load switch

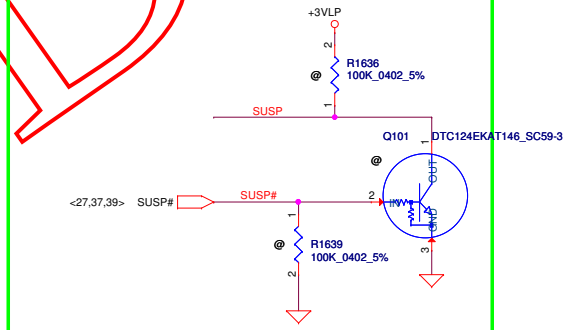
VIN 1.8V and 0.95V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm

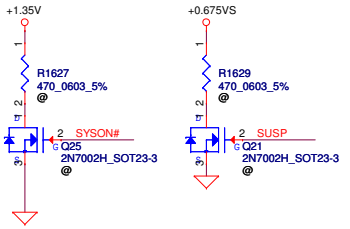


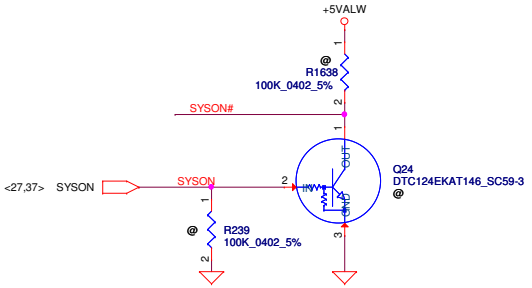
+1.5VS discharge circuit only for Beema
only 1.5VS from PWR



only for Beema







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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date 2015/03/05	Title: DC Interface
Size: B	Document Number: LA-B291P		Rev: 1.0
Date: Monday, March 03, 2014	Sheet 32 of 46		

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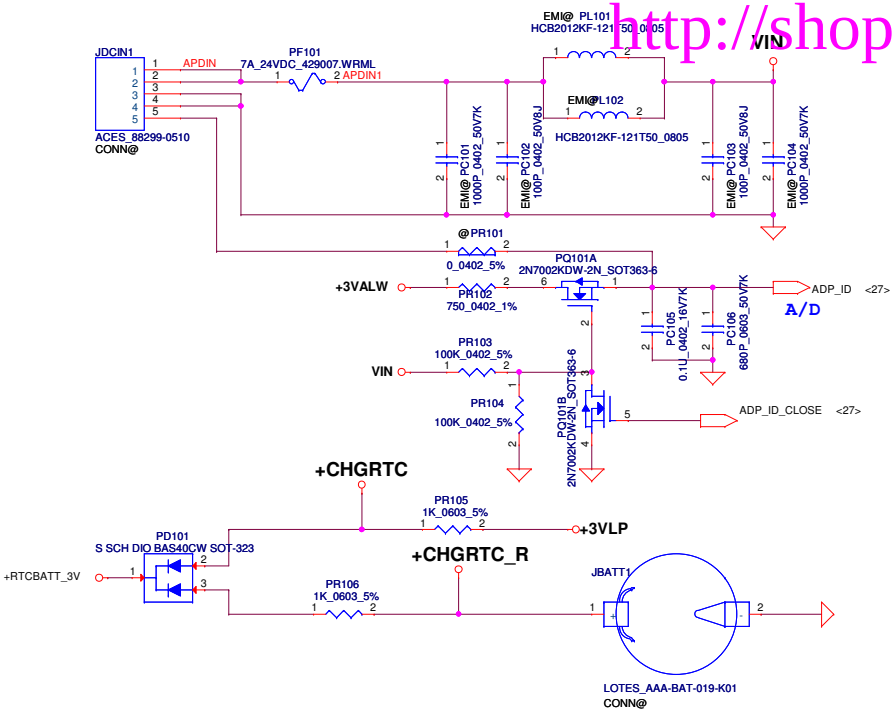

ADP_ID		
AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

RTC Battery

For DFB only

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03
			Title: Power Map
			Size: Custom; Document Number: LA-B291P; Rev: 1.0
			Date: Monday, March 03, 2014; Sheet 33 of 46

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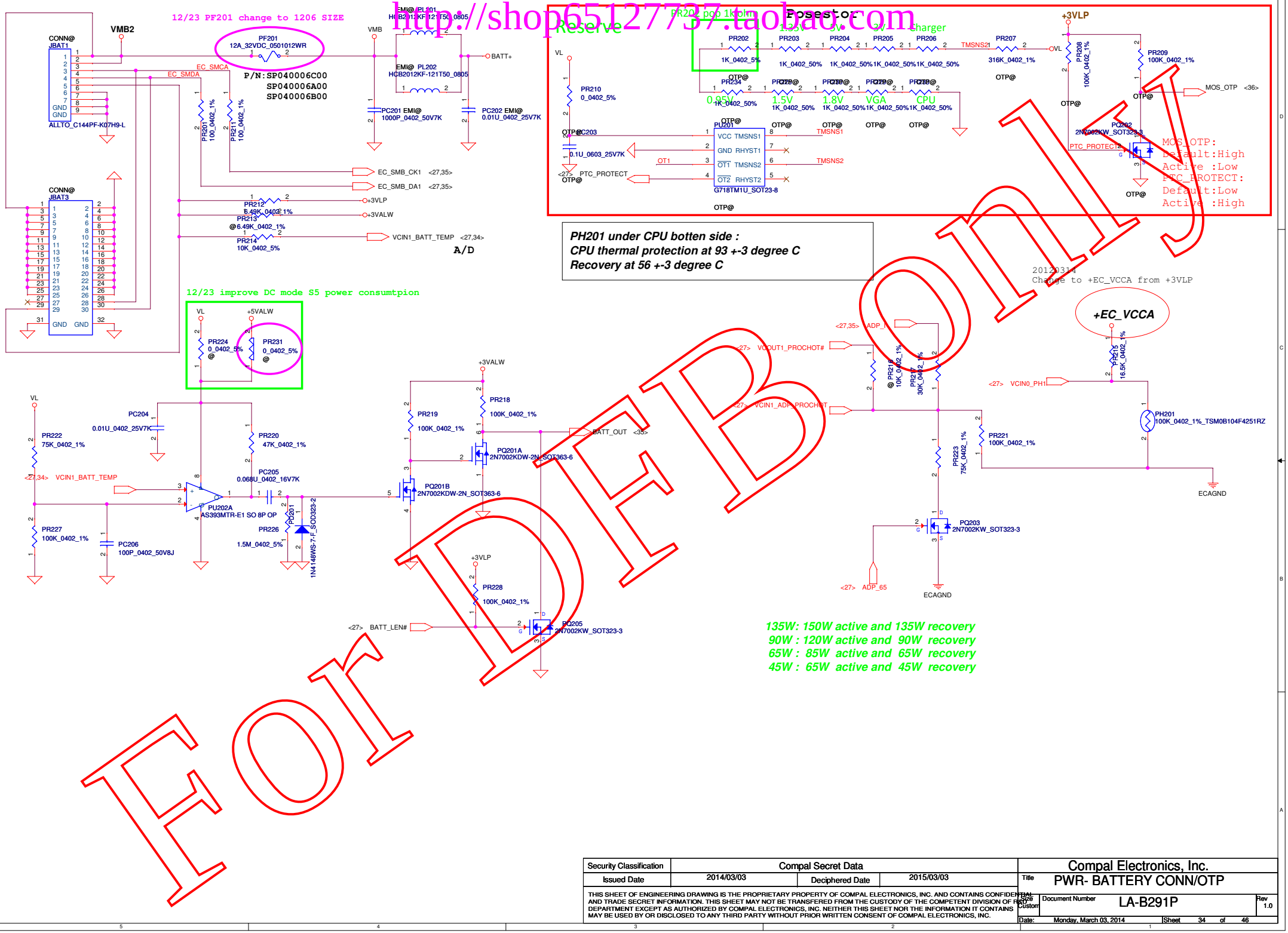

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Issued Date	2014/03/03	Deciphered Date	2015/03/03

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Compal Electronics, Inc.			
Title	PWR- BATTERY CONN/OTP		
Size: Custom	Document Number: LA-B291P		Rev: 1.0
Date: Monday, March 03, 2014	Sheet 34 of 46		

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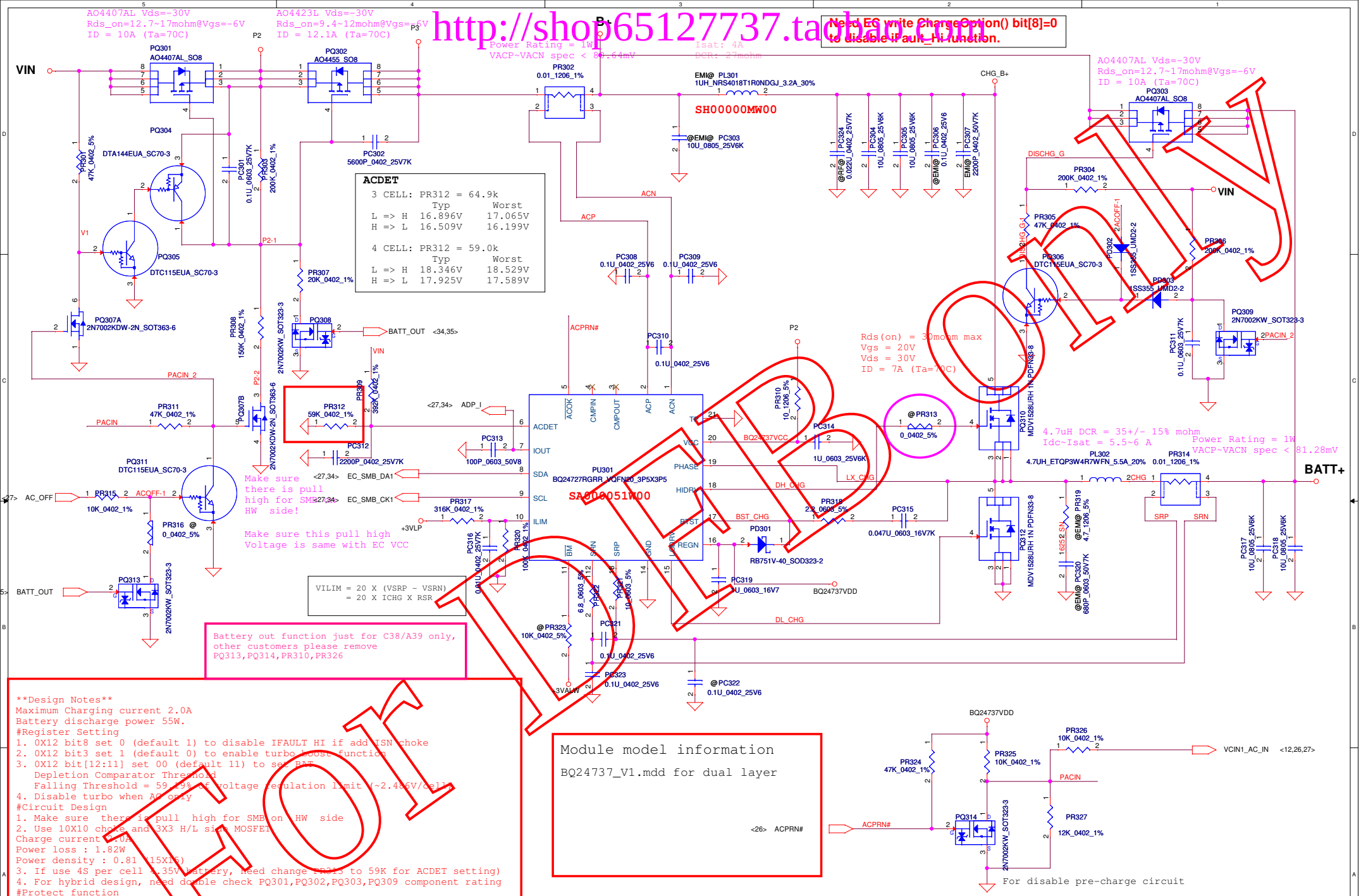

Design Notes
Maximum Charging current 2.0A
Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
2. 0X12 bit3 set 1 (default 0) to enable turbo boost function
3. 0X12 bit[12:11] set 00 (default 11) to set BAT
Depletion Comparator Threshold
Falling Threshold = 59.19% of voltage regulation limit (~2.486V/cell)
4. Disable turbo when AC only
#Circuit Design
1. Make sure there is pull high for SMB on HW side
2. Use 10X10 choke and 3X3 H/L side MOSFET
Charge current 2.0A
Power loss : 1.82W
Power density : 0.81 (15X15)
3. If use 4S per cell 4.35V battery, need change PR313 to 59K for ACDET setting)
4. For hybrid design, need double check PQ301,PQ302,PQ303,PQ309 component rating
#Protect function
1. ACOVP : ACDET voltage > 3.15V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 104%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 135mV (default)

Module model information
BQ24737_V1.mdd for dual layer

For TEST Only

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title: PWR- CHARGER BQ24727
				Size: Document Number: LA-B291P — Rev: 1.0
				Date: Monday, March 03, 2014 — Sheet 35 of 46

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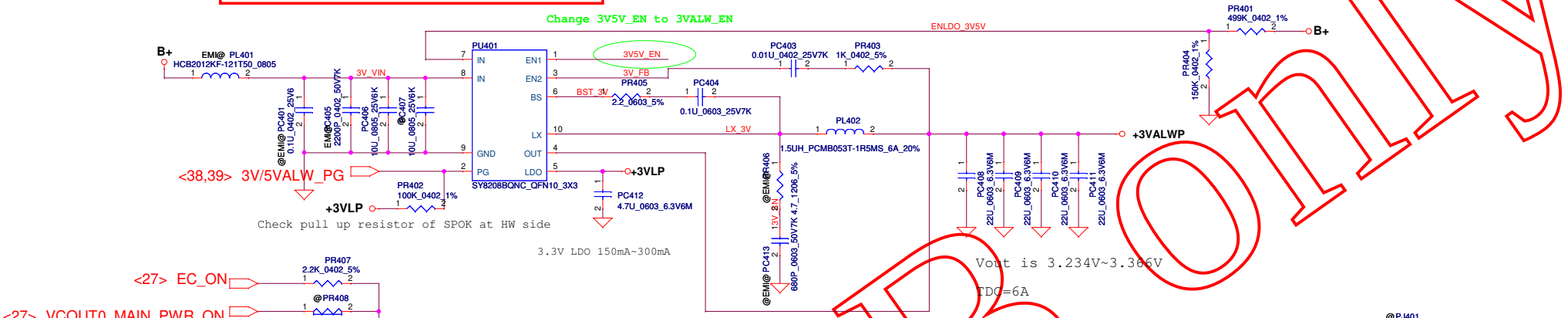
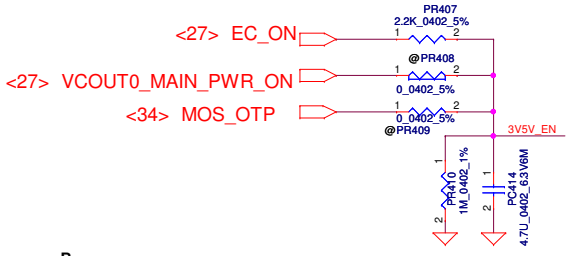
Module model information

SY8208B_V2.mdd

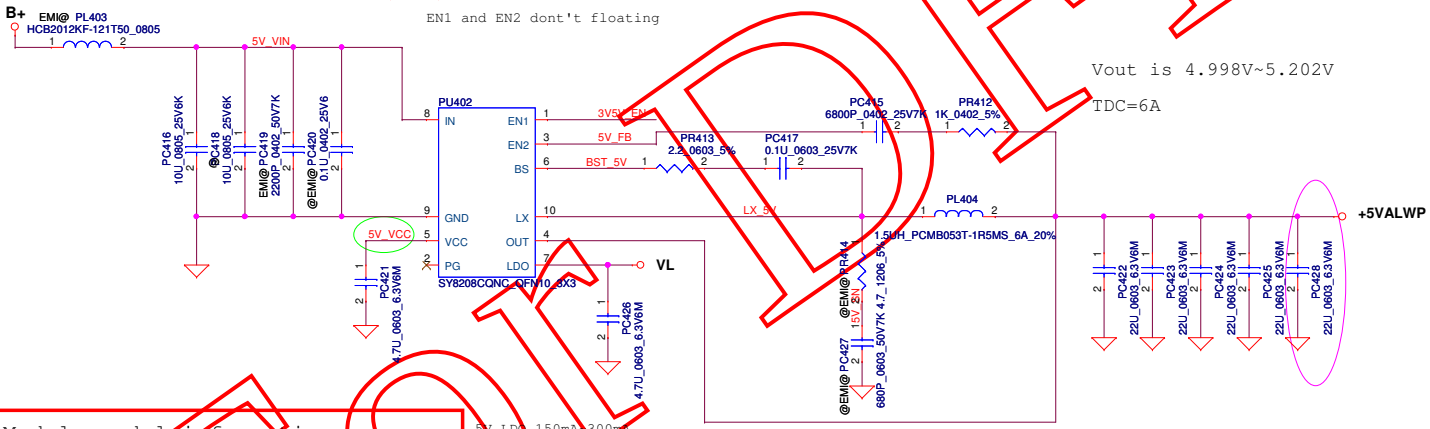
EN1 and EN2 dont't floating

Change 3V5V_EN to 3VALW_EN





EN1 and EN2 dont't floating



Module model information

SY8208C_V2.mdd

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03
Title	PWR- 3VALW/5VALW-SY8208B/C		
Size	Custom	Document Number	LA-B291P
Rev	1.0		
Date:	Monday, March 03, 2014	Sheet	36 of 46

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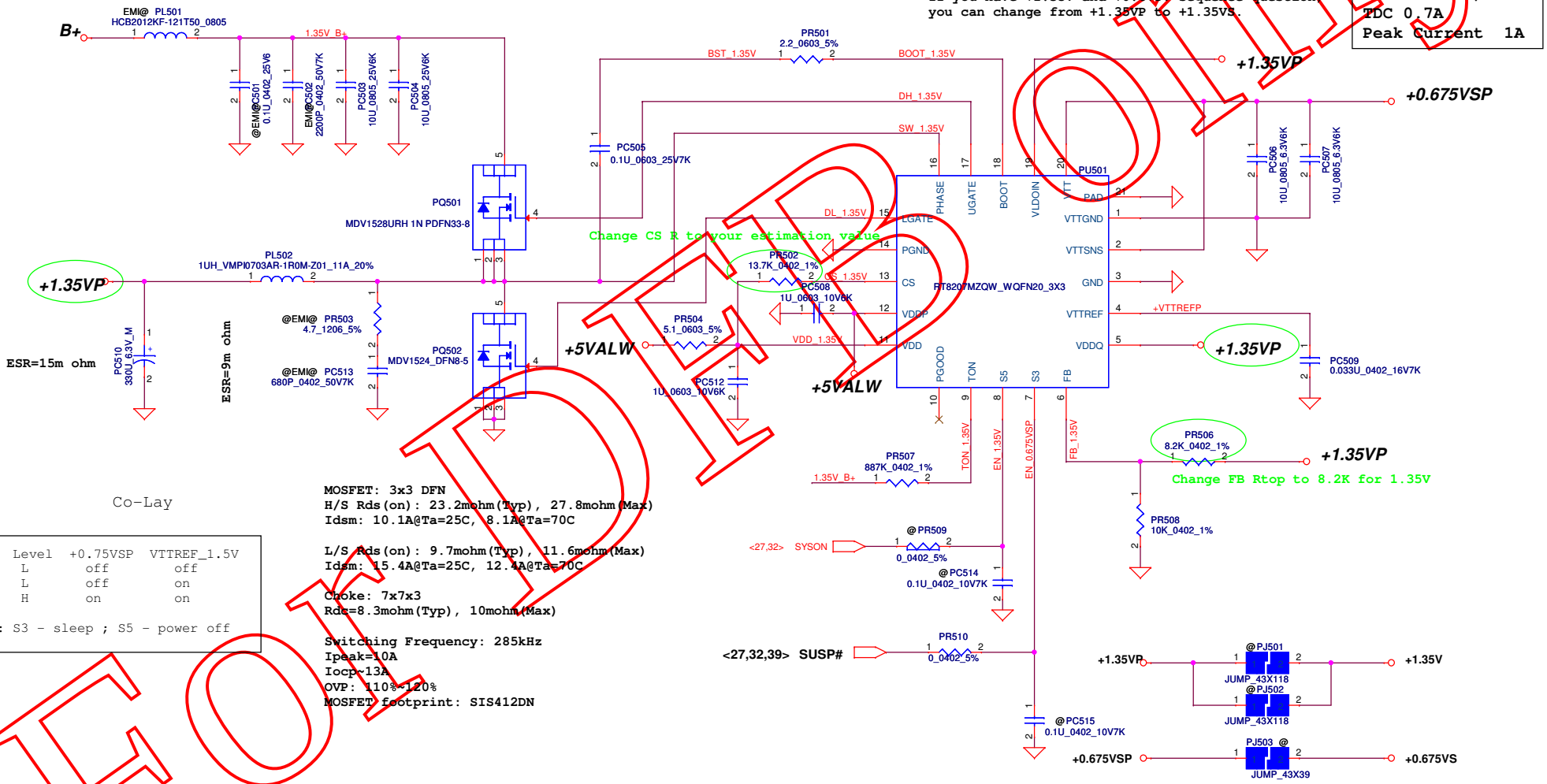
Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



Co-Lay

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 23.2mohm(Typ), 27.8mohm(Max)
Idsm: 10.1A@Ta=25C, 8.1A@Ta=70C

L/S Rds(on): 9.7mohm(Typ), 11.6mohm(Max)
Idsm: 15.4A@Ta=25C, 12.4A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
MOSFET footprint: SIS412DN

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Compal Electronics, Inc.

Title: PWR-+1.35VP/ +0.675VS

Size: Custom | Document Number: LA-B291P | Rev: 1.0

Date: Monday, March 03, 2014 | Sheet 37 of 46

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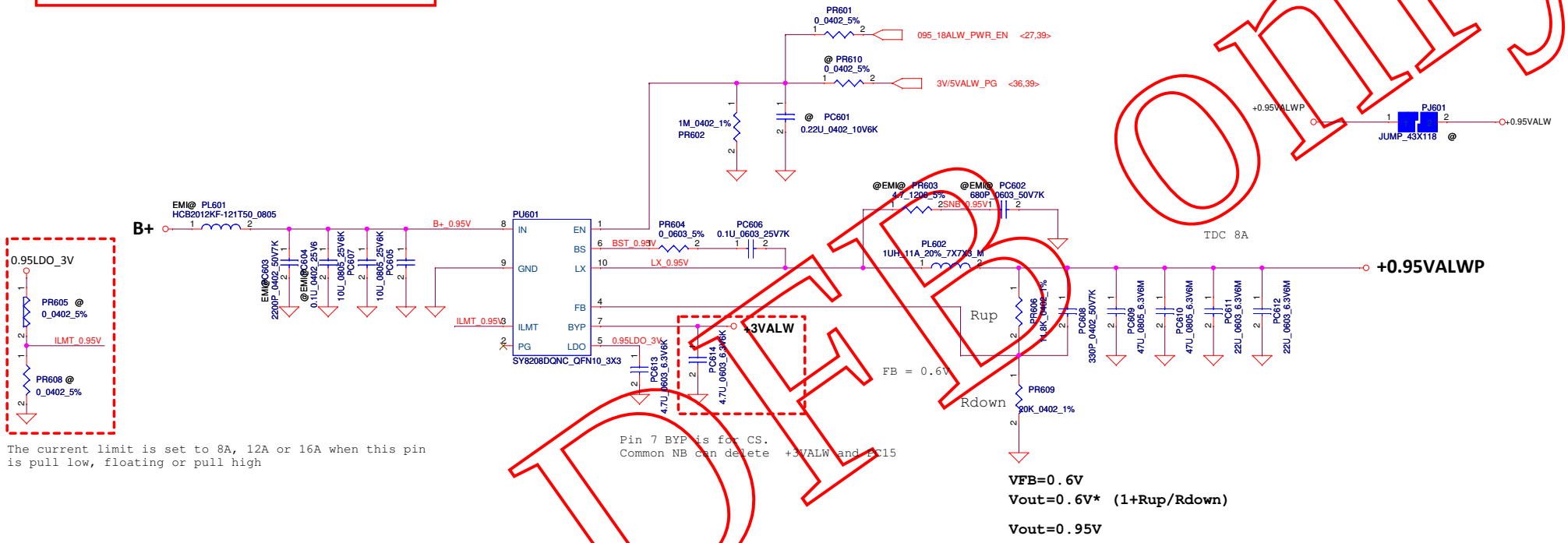
Module model information

SY8208D_V2.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

Vout=0.95V

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Compal Electronics, Inc.			
Title	PWR- +0.95VALW		
Size: Custom	Document Number: LA-B291P		Rev: 1.0
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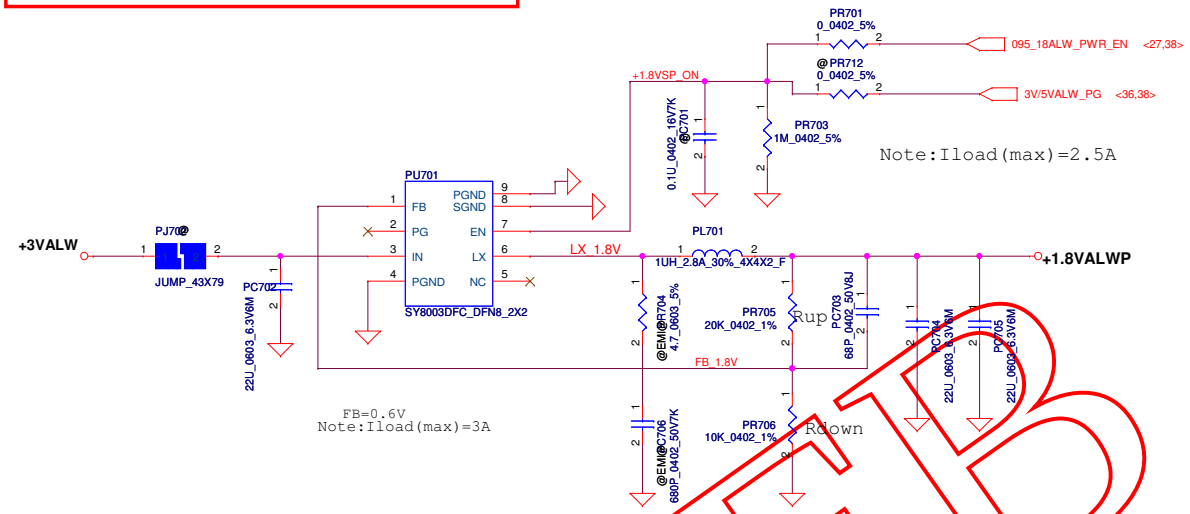
Module model information

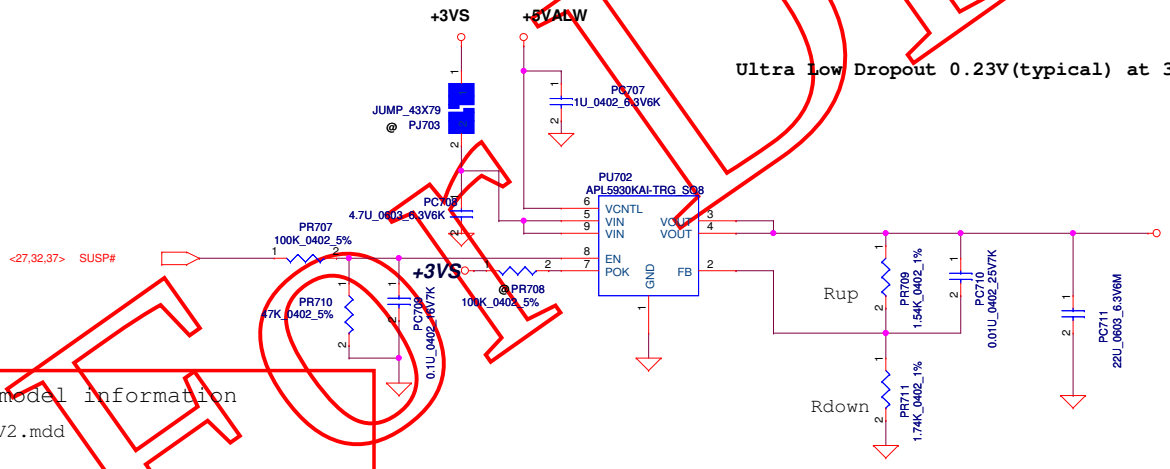
SY8003_V2.mdd

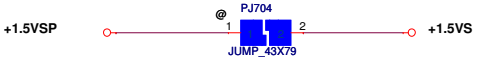


Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Ultra Low Dropout 0.23V(typical) at 3A Output Current





Vout=0.8V* (1+Rup/Rdown)

Module model information

APL5930_V2.mdd

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Title	PWR- +1.8VALW/ +1.5VS		
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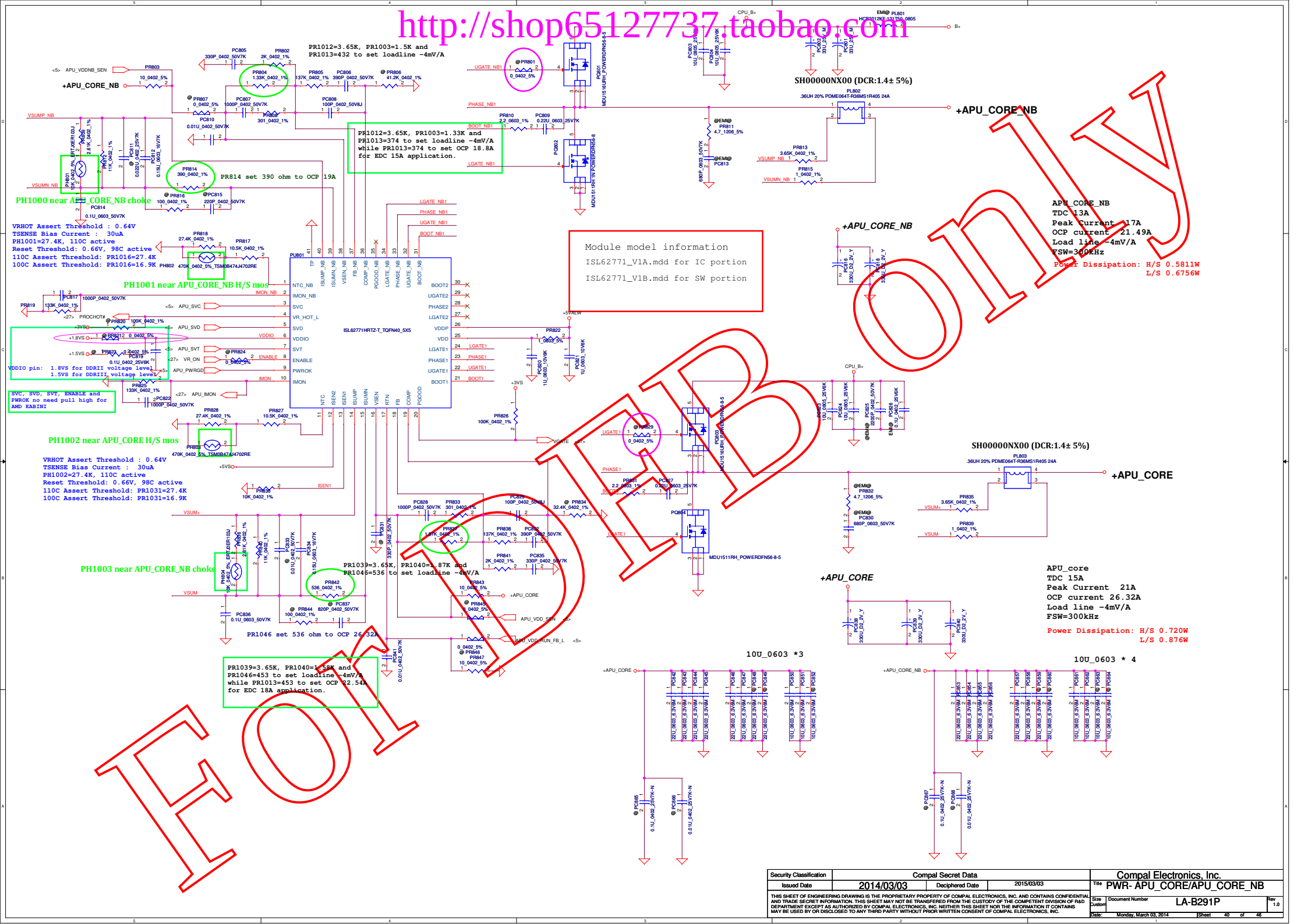

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Module model information

ISL62771_V1A.mdd for IC portion

ISL62771_V1B.mdd for SW portion

+VGA_CORE
AMD JET LE
TDC 20A
EDC 30A

VRHOT Assert Threshold : 0.64V
TSENSE Bias Current : 30uA
PH1001=27.4K, 110C active
Reset Threshold: 0.66V, 98C active
110C Assert Threshold: PR1016=27.4K
100C Assert Threshold: PR1016=16.9K

SVC, SVD, SVT, ENABLE and PWROK no need pull high for AMD KABINI

VRHOT Assert Threshold : 0.64V
TSENSE Bias Current : 30uA
PH1002=27.4K, 110C active
Reset Threshold: 0.66V, 98C active
110C Assert Threshold: PR1031=27.4K
100C Assert Threshold: PR1031=16.9K

Fsw=400K Hz

25W

15W

GPU 15W setting

PR931=536 ohm, PR924=1K ohm, PC925=0.1uF,
PR944 =0 ohm, PR920=10K ohm,
PC961 @, PC962 @, PR938 @ and PR939 @
while PR931=536 ohm to set OCP for GPU 15W application.

SH00000NX00 (DCR:1.4± 5%)

1/7 change to H=6 CAP_SF000002000

Power Dissipation: H/S 0.720W
L/S 0.876W

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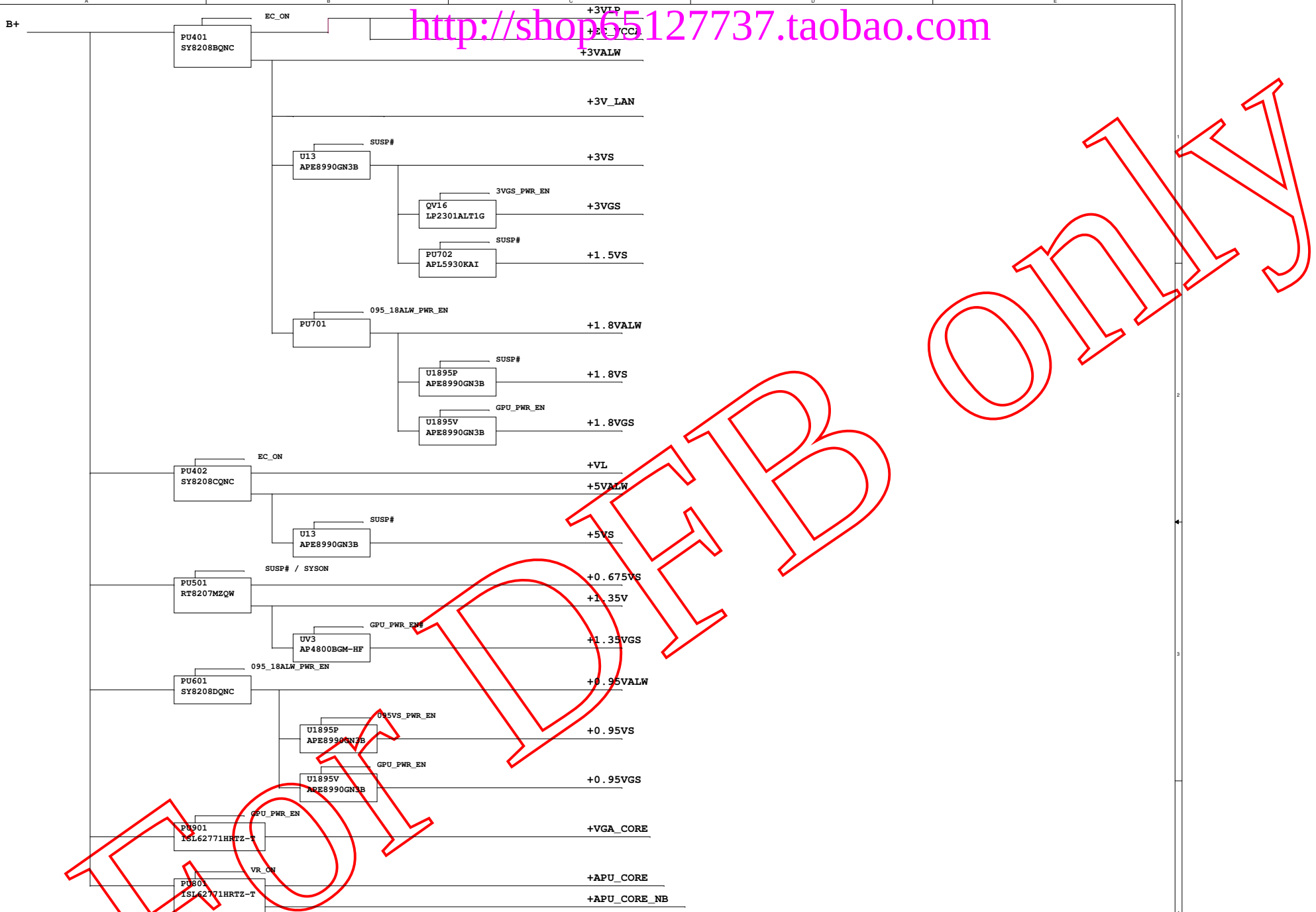

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Compal Electronics, Inc.

Title: PWR DCIN / RTC Battery

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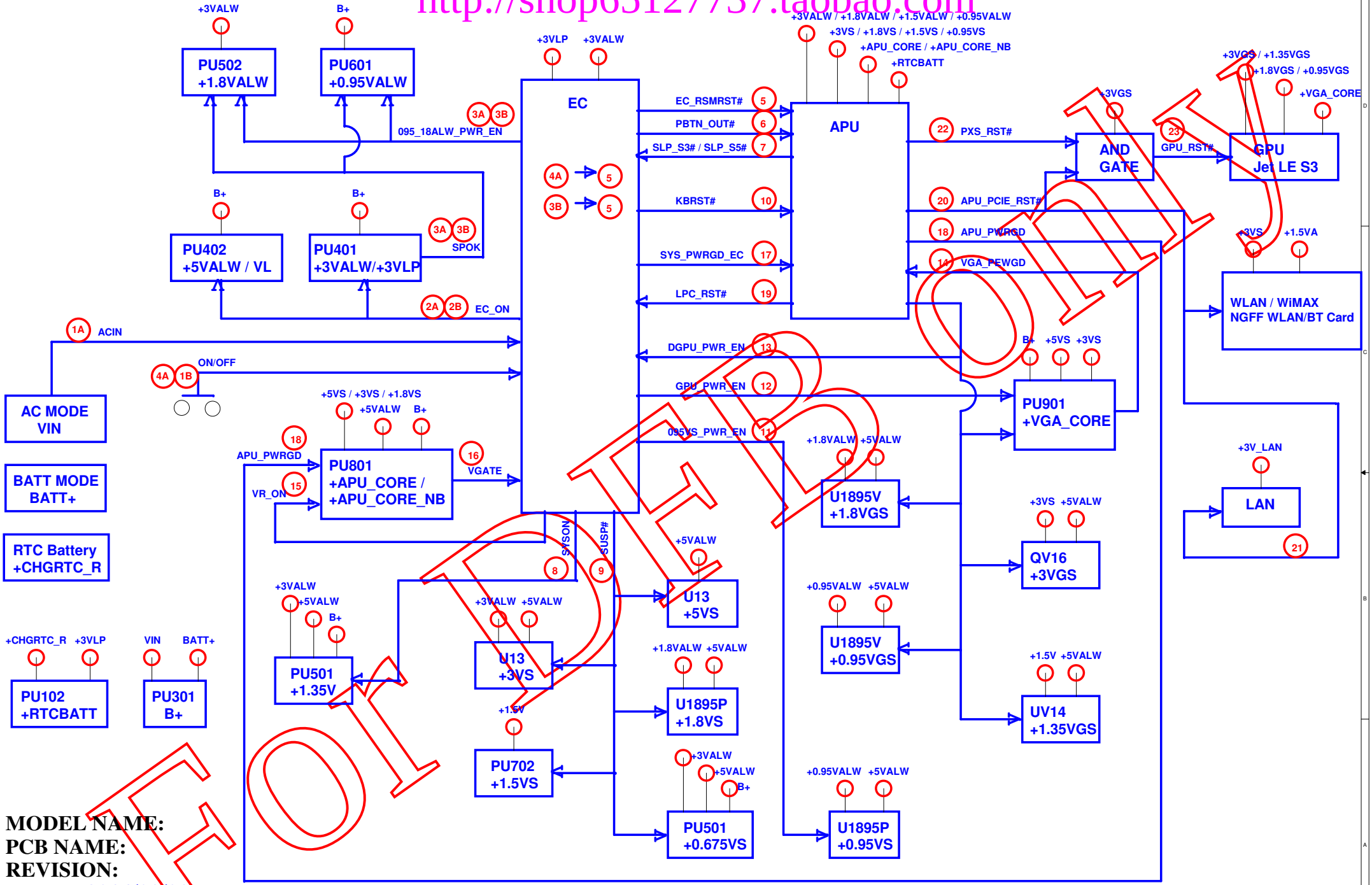

FOR QUIET

MODEL NAME:
PCB NAME:
REVISION:
DATE: *2014/03/03*

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Compal Electronics, Inc.

Title: Power Sequence Block

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