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Compal Confidential

Model Name :
File Name : LA-8671P

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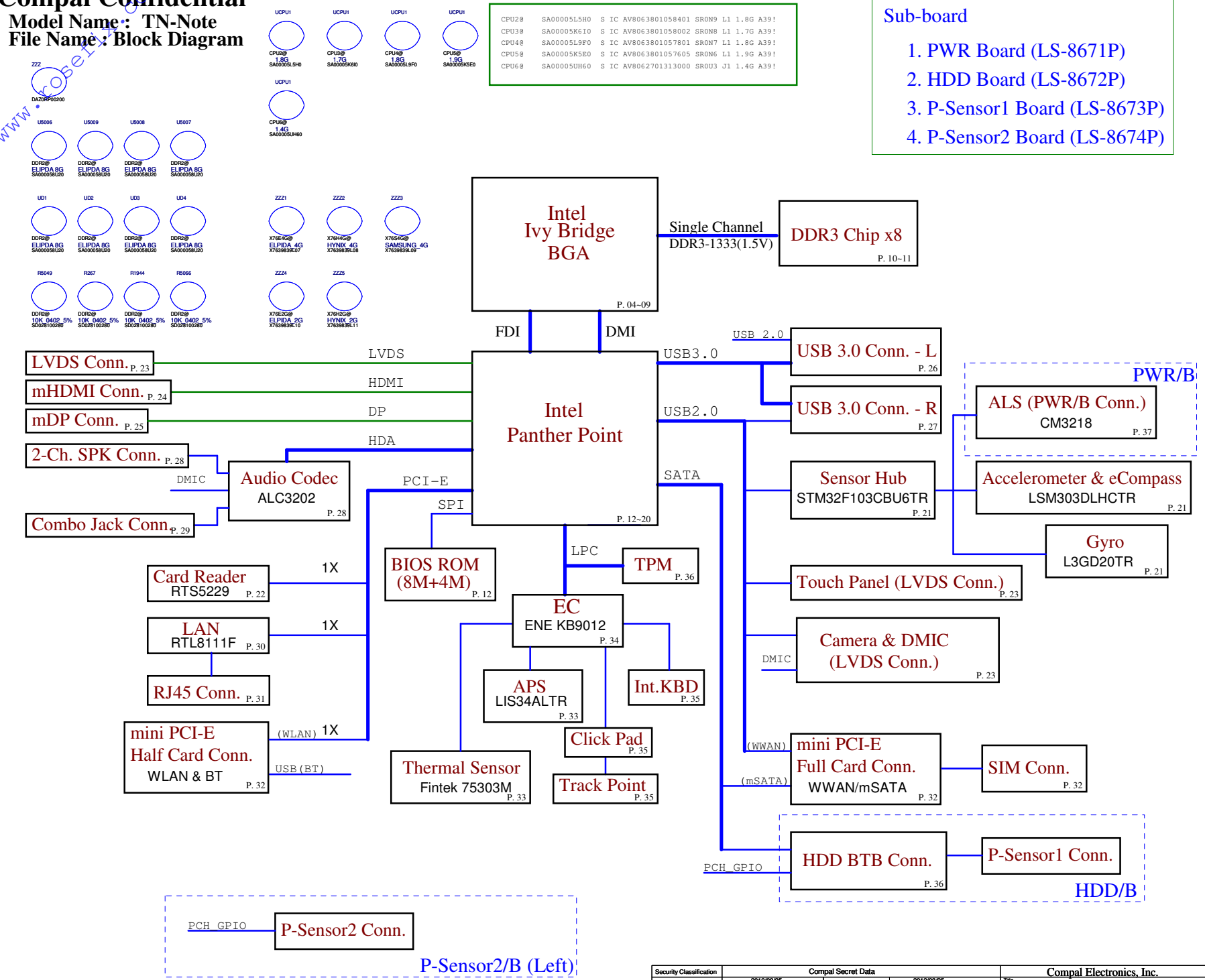
TN-Note Schematic Document

2012-07-27

REV:1.0_0727A

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Issued Date		2010/08/25	Deciphered Date	2012/08/25	
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Compal Confidential
Model Name: TN-Note
File Name: Block Diagram



- Sub-board
1. PWR Board (LS-8671P)
 2. HDD Board (LS-8672P)
 3. P-Sensor1 Board (LS-8673P)
 4. P-Sensor2 Board (LS-8674P)

CPU28	SA00005L5H0	S IC	AV8063801058401	SR0N9	L1	1.8G	A39!
CPU38	SA00005K610	S IC	AV8063801058002	SR0N8	L1	1.7G	A39!
CPU48	SA00005L9F0	S IC	AV8063801057801	SR0N7	L1	1.8G	A39!
CPU58	SA00005K5E0	S IC	AV8063801057605	SR0N6	L1	1.9G	A39!
CPU68	SA00005UH60	S IC	AV8062701313000	SR0U3	J1	1.4G	A39!

Voltage Rails

Power plane	State	+B	+5VALW +3VALW	+1.5V	+3VM +1.05VM	+5VS +3VS +1.8VS +1.5VS +1.05VS +VCC_GFXCORE_AXG +CPU_CORE +VCCSA +0.75VS
S0		○	○	○	○	○
S3		○	○	○	○	×
M3		○	○	○	○	×
S4/S5 - AC		○	○	×	×	×
S4/S5 - BATT ONLY		○	×	×	×	×
S4/S5 - NO AC & BATT		×	×	×	×	×

BOM Structure

	SDV	FVT	SIT	SVT	SOVP
@ : No Stuff					
ME@ : ME components					
CPUx@ : CPU SKU	V	V	V	V	
DDRx@ : RAM SKU	V	V	V	V	
SBA@ : SBA	V	V	V	V	
NOSBA@ : NO SBA					
ID4@ : Intel Deep S4	V				
AOAC@ : AOAC	V	V	V	V	
TPM@ : TPM		V	V	V	
Short@ : 0ohm short pad					

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS
Full ON		H	H	H	ON	ON	ON
S3 (Suspend to RAM)		L	H	H	ON	ON	OFF
S4 (Suspend to Disk)		L	L	H	ON	OFF	OFF
S5 (Soft OFF)		L	L	L	ON	OFF	OFF

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	16H	Thermal sensor	1001-101xb	9AH
Charger	0001-0010b	12H	PCH (SML1DATA / GPIO75)	1001-0110 b	96H

EC SM Bus2 address

SM Bus Controller

Device	Address	HEX
Security Rom	1010-100xb	A8 H
DDR DIMM0	1010-000xb	A0 H

SM Bus Controller 0

Device	Address	HEX
No-use	No-use	No-use

Sensor HUB

Device	Address	HEX
ALS	0100-100xb	48h
APS	0011-001xb	32h
Gyroscope	0110-101xb	6Ah
e-Compass	0011-110xb	3Ch

BOARD ID Table

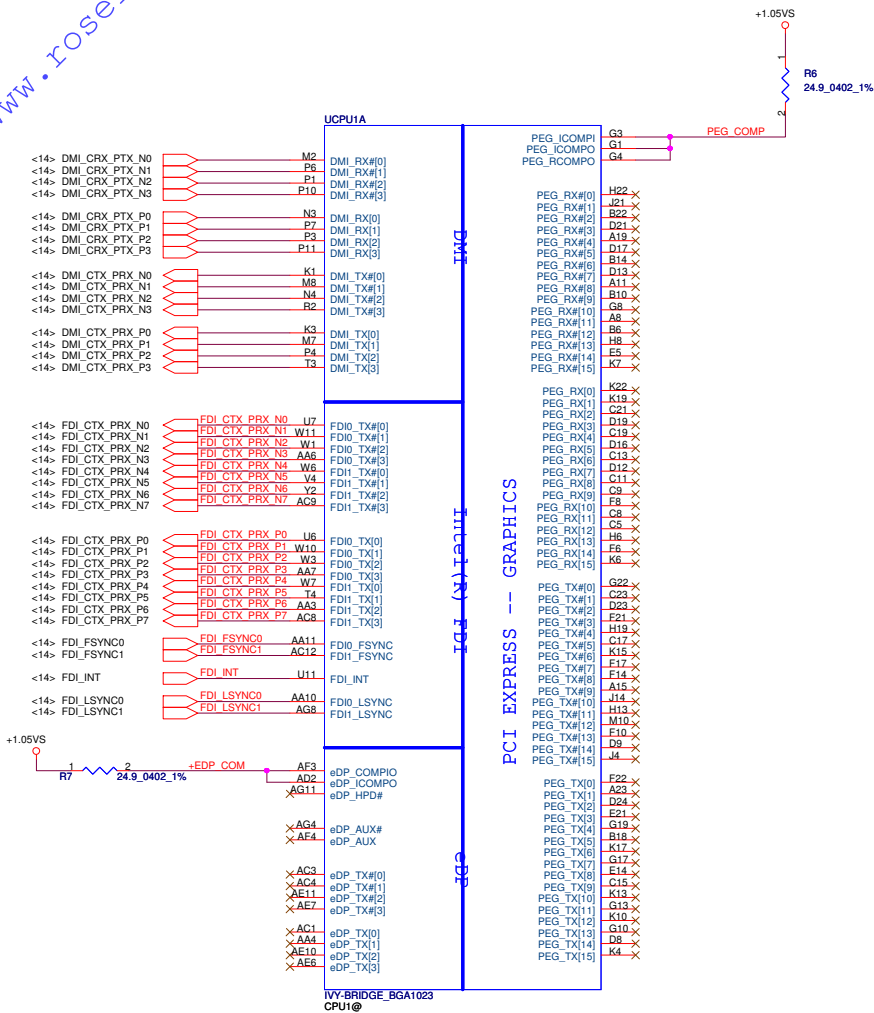
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

USB3.0	USB2.0	NOTE
1	0	
2	1 *	USB3.0/2.0 Conn
3	2	USB3.0/2.0 Conn
4	3	
	4	Sensor Hub
	5	USB Camera
	6	×
	7	×
	8	Touch Panel
	9 *	WWAN
	10	WLAN
	11	Finger Printer**
	12	
	13	Bluetooth**

* Debug Port

** Not Use

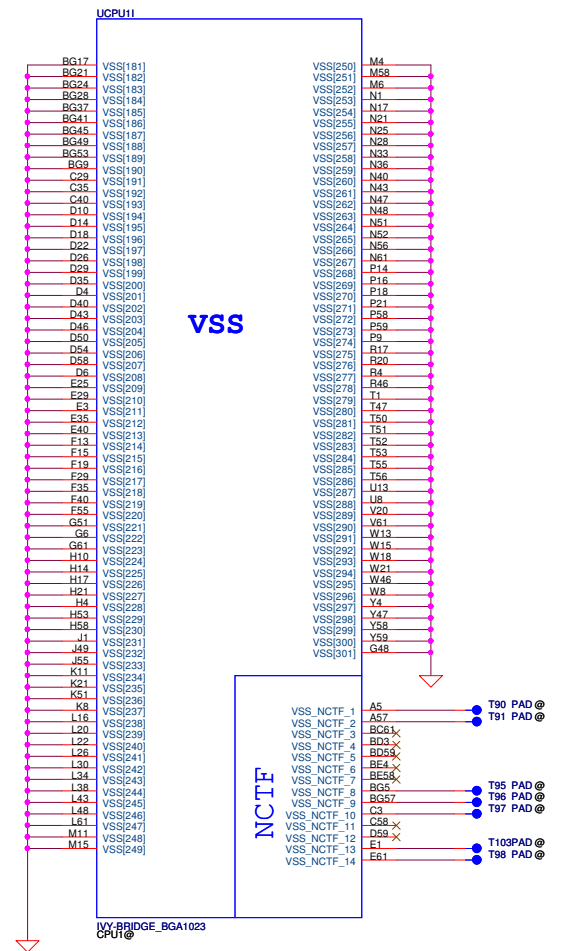
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Issued Date	2011/05/16	Deciphered Date	2013/05/16	Title	Cover Sheet	
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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

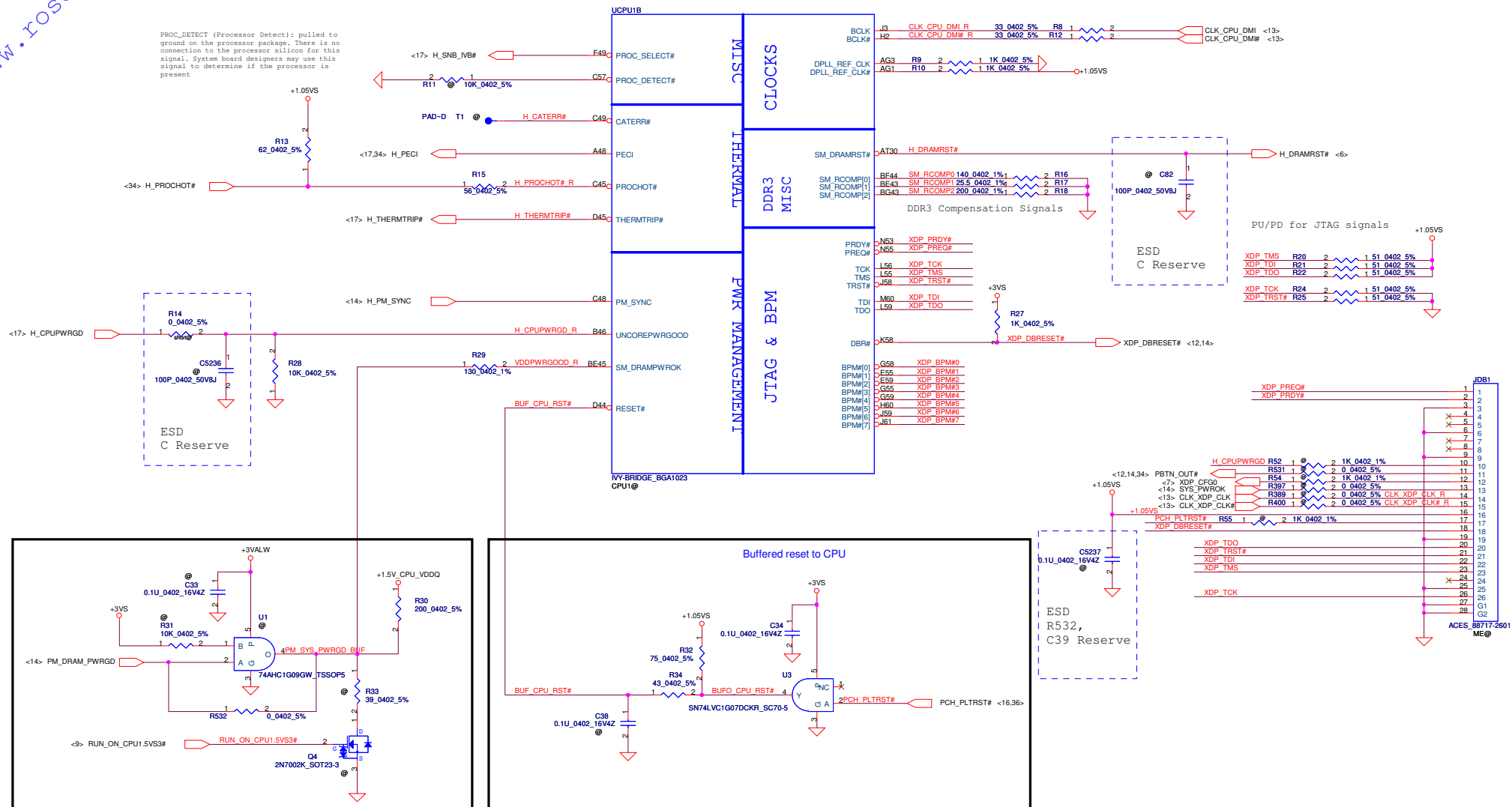
PEG Static Lane Reversal - CFG2 is for the 16x

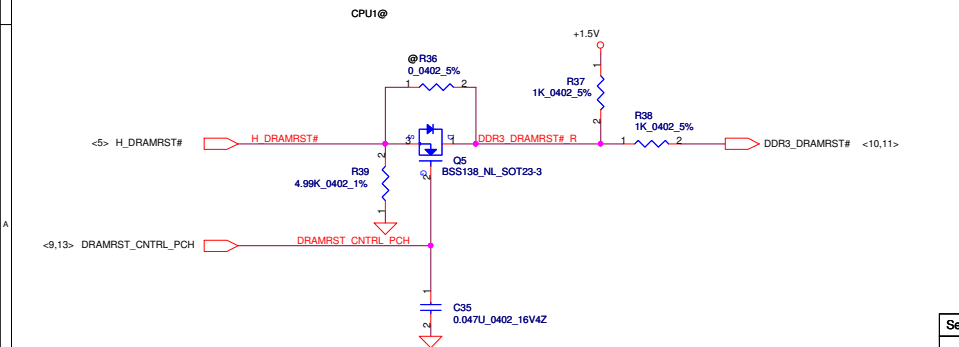
CFG2	★ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
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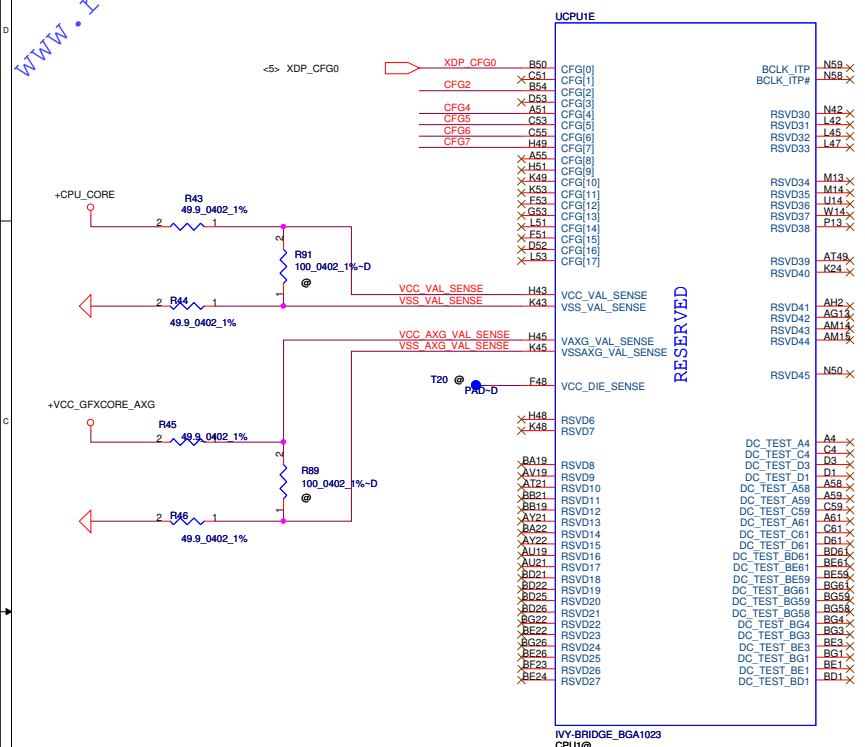
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PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.

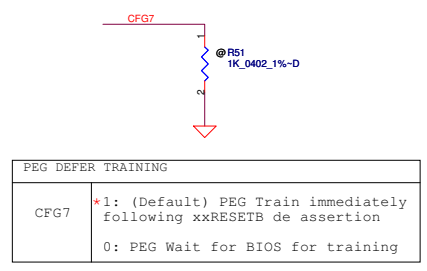
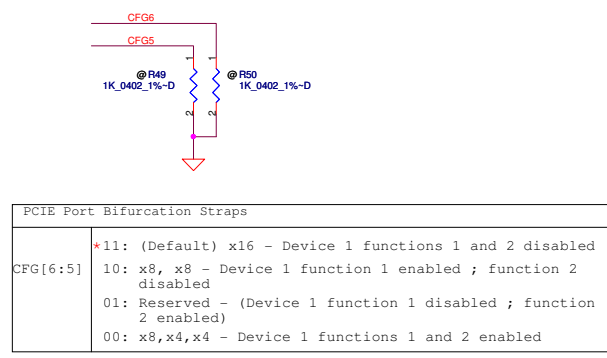
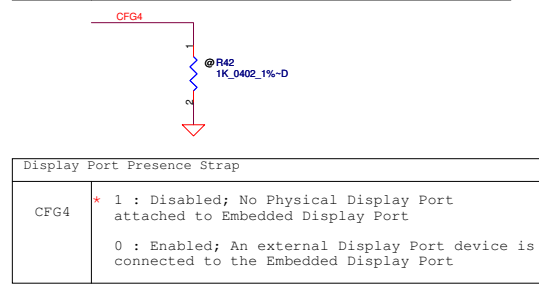
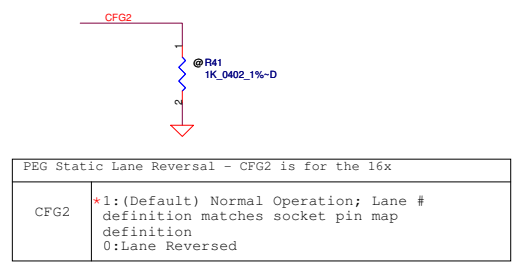


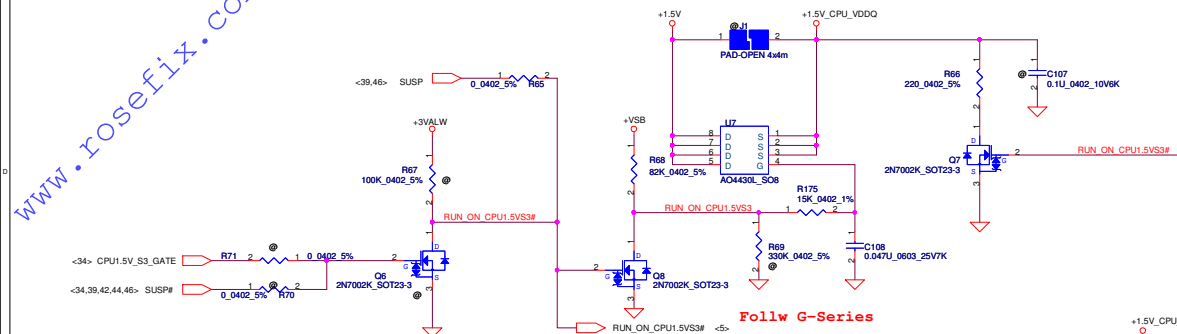


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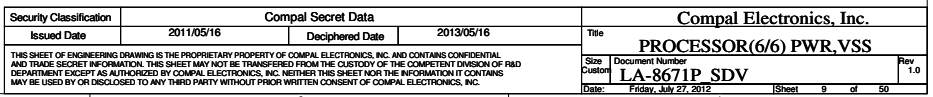


CFG Straps for Processor

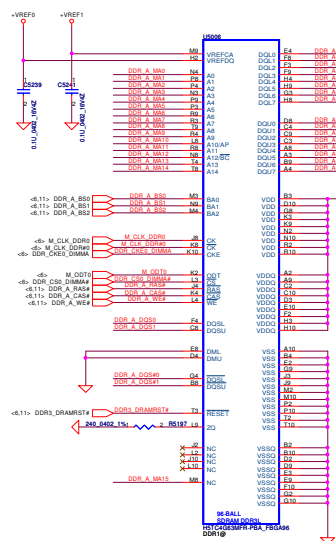




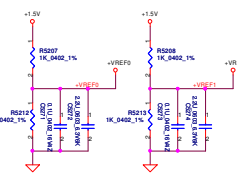
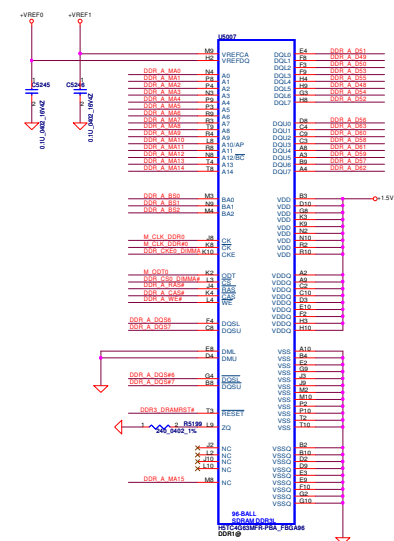
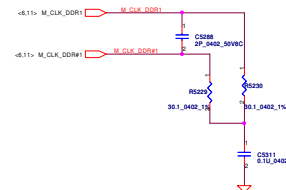
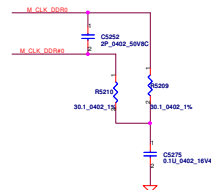
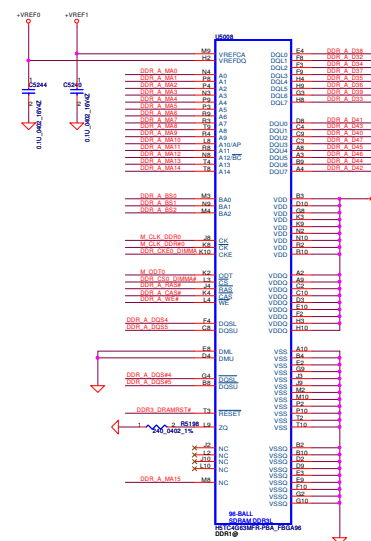
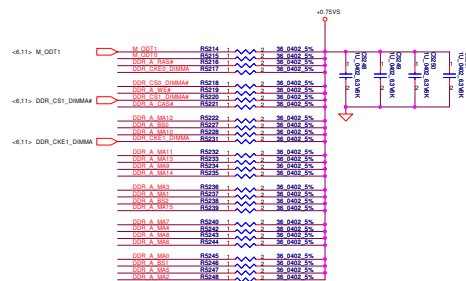
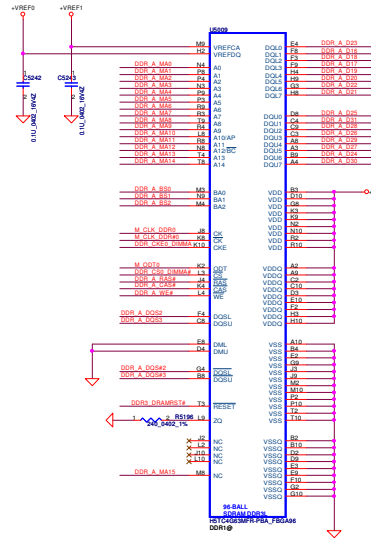
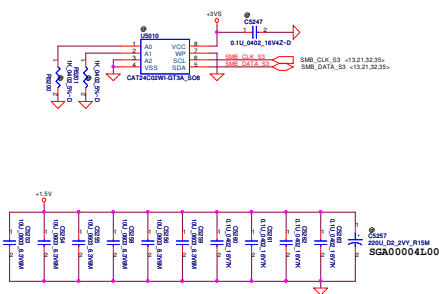
POWER



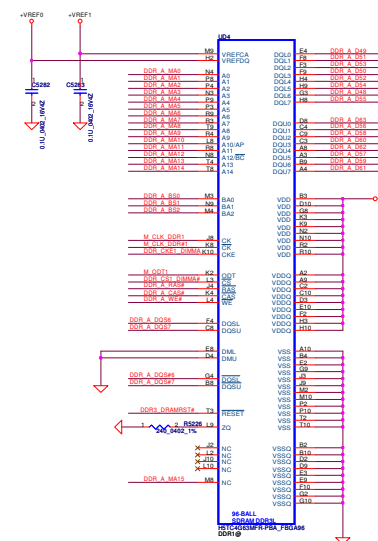
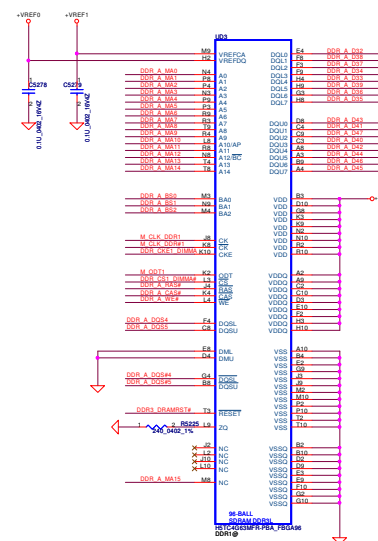
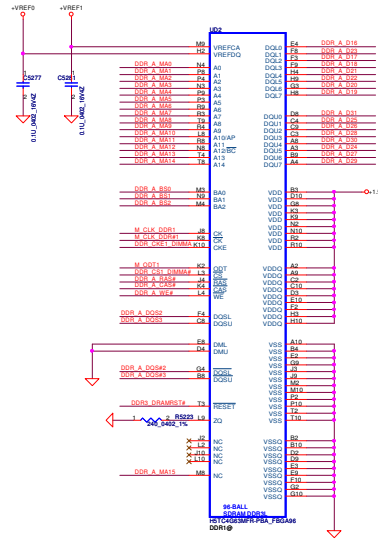
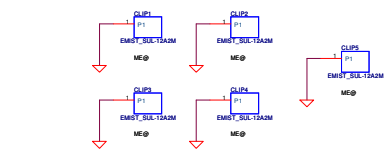
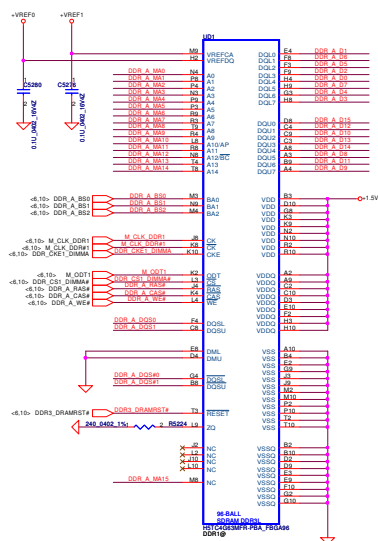
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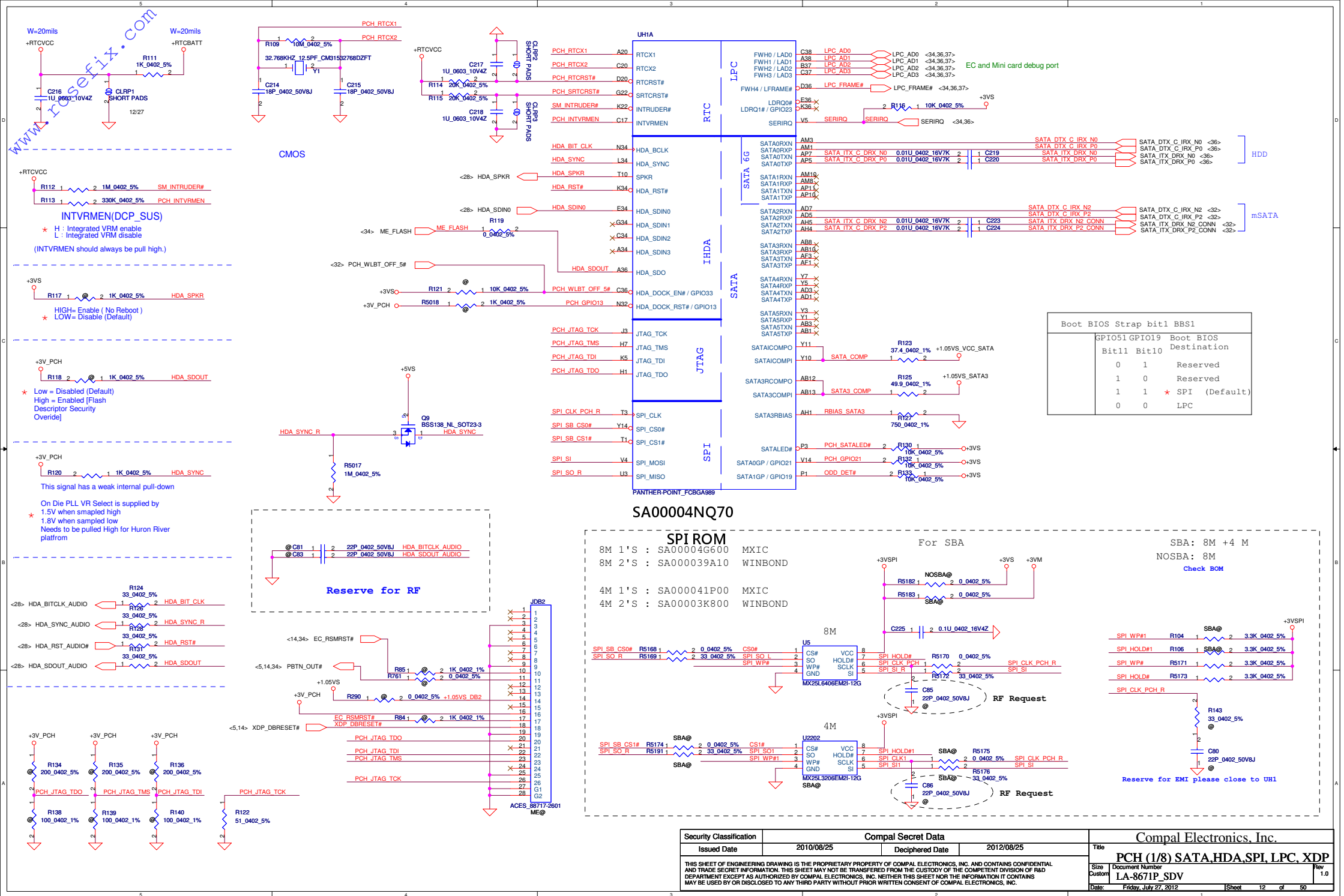


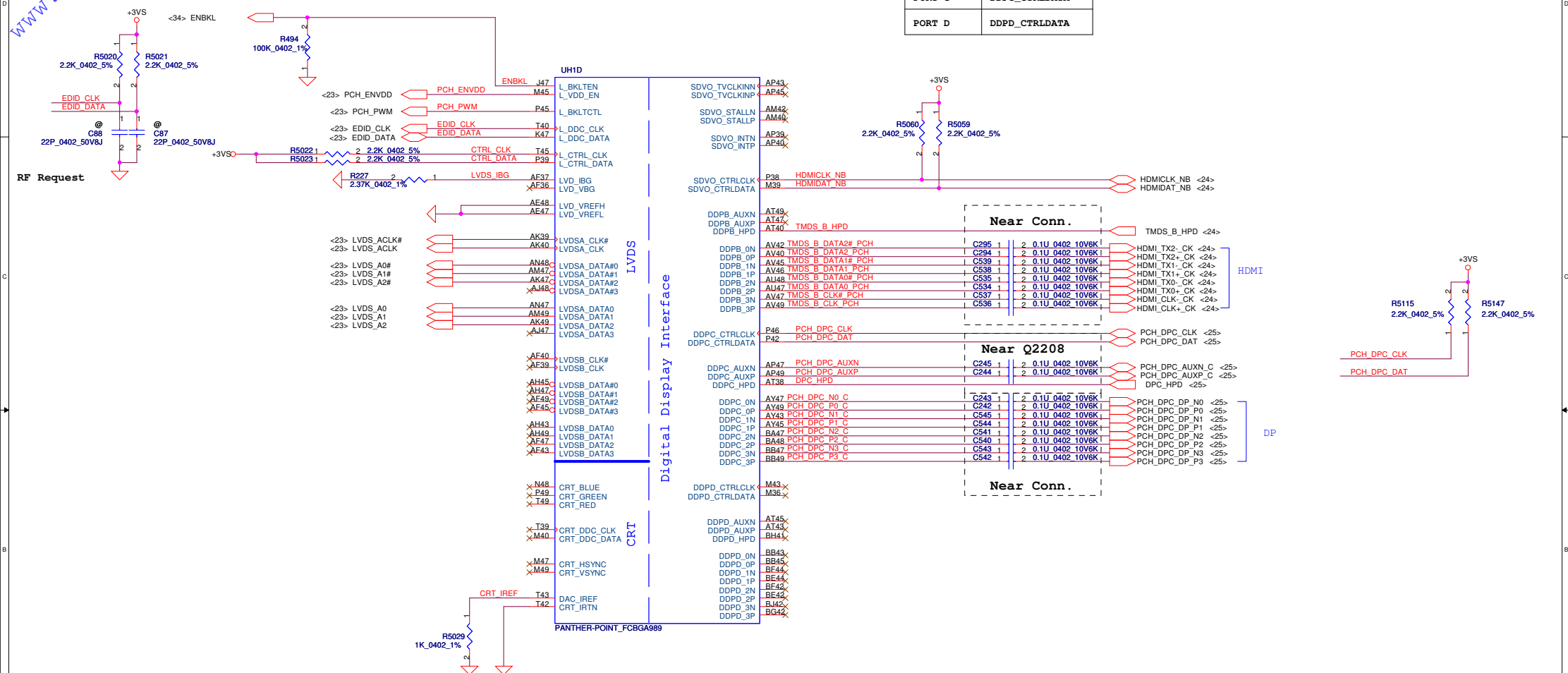
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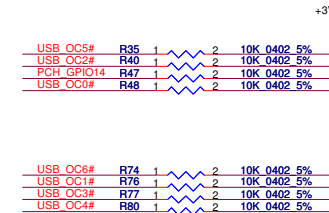
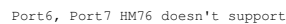
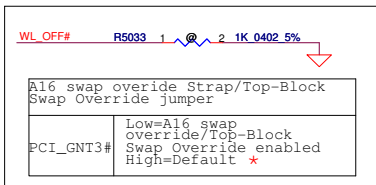


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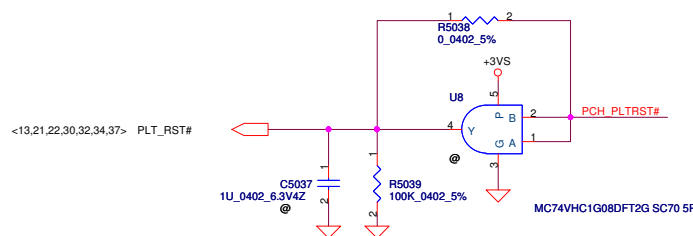
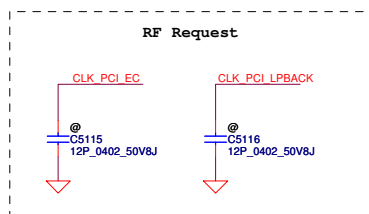




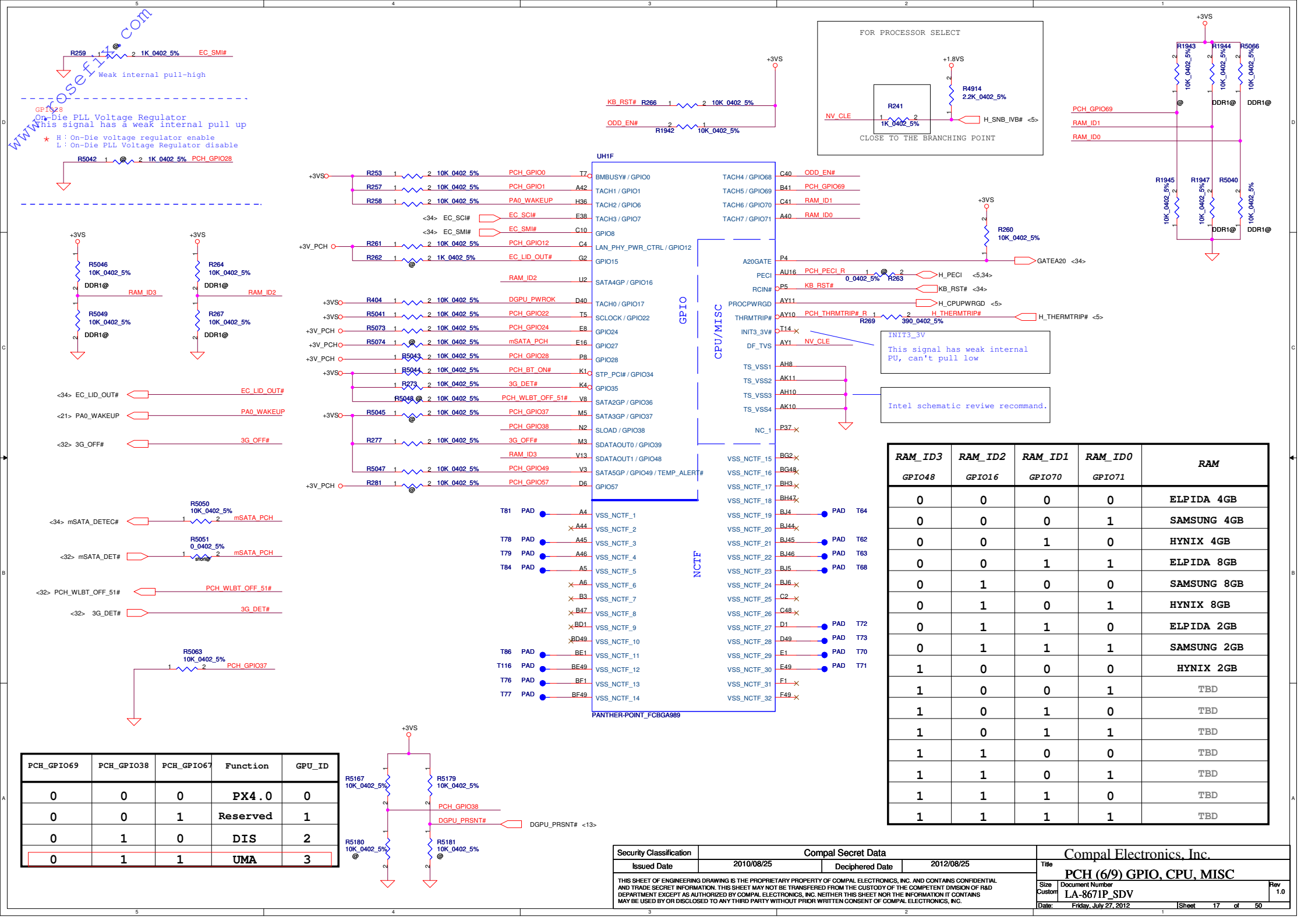
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3	2	USB3.0/2.0 Conn
4	3	
	4	Sensor Hub
	5	USB Camera
	6	X
	7	X
	8	Touch Panel
	9 *	WWAN
	10	WLAN
	11	Finger Printer**
	12	
	13	Bluetooth**

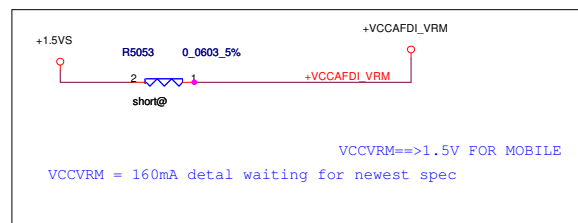
* Debug Port

**** Not Use**

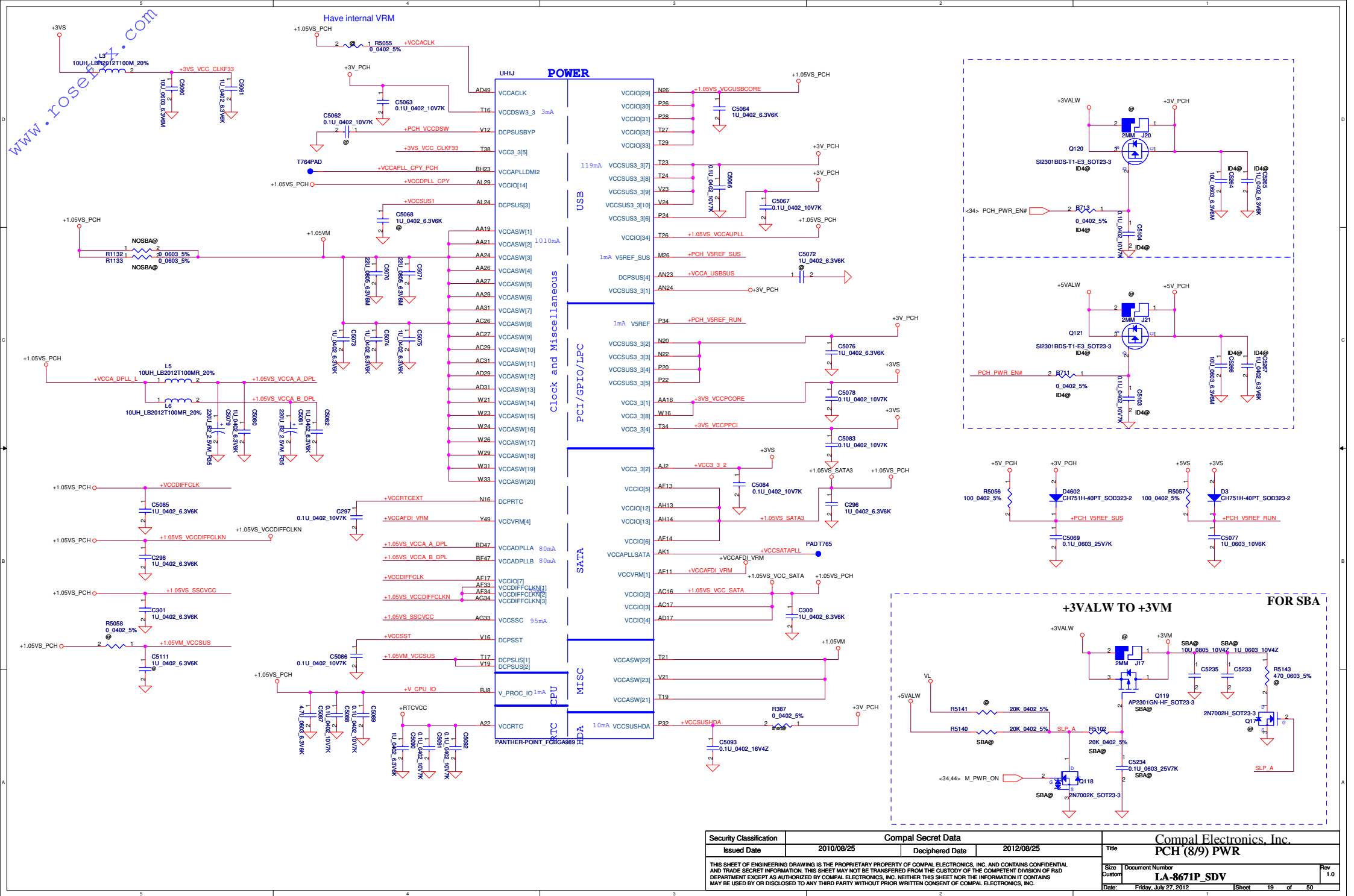


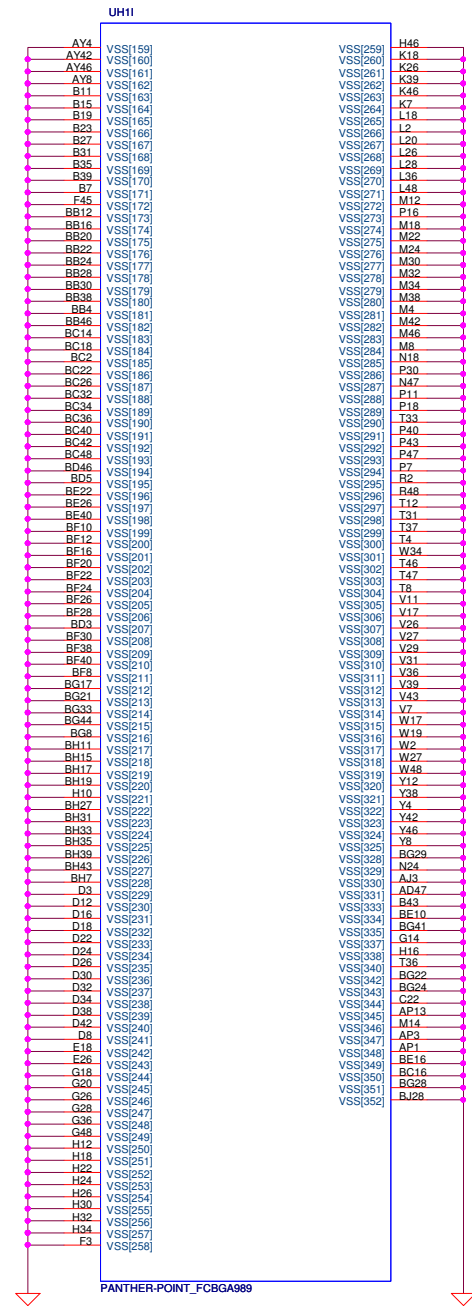
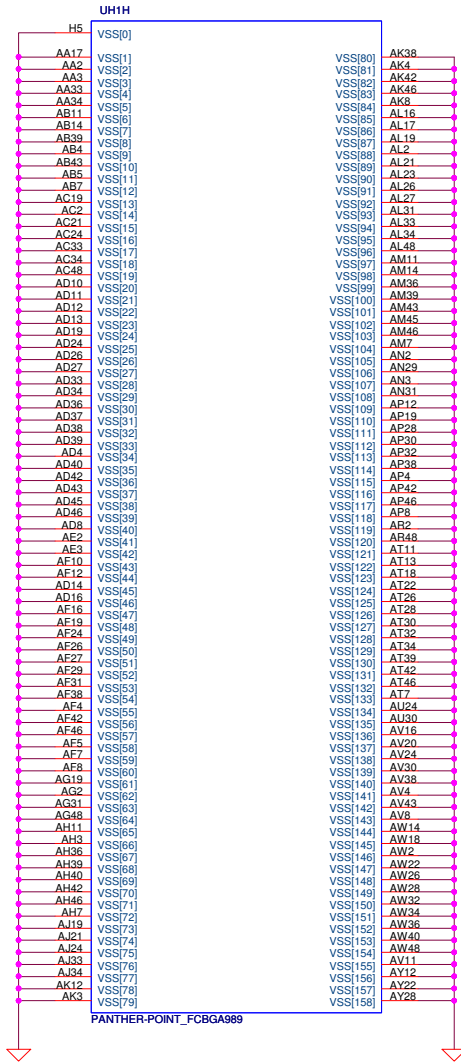
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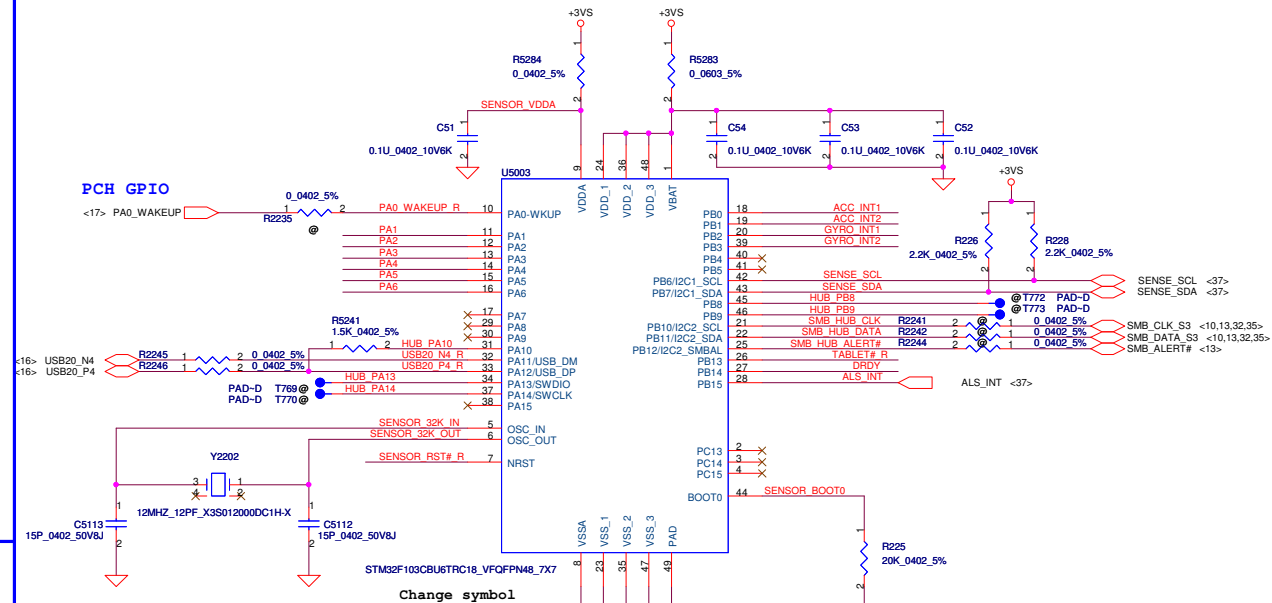
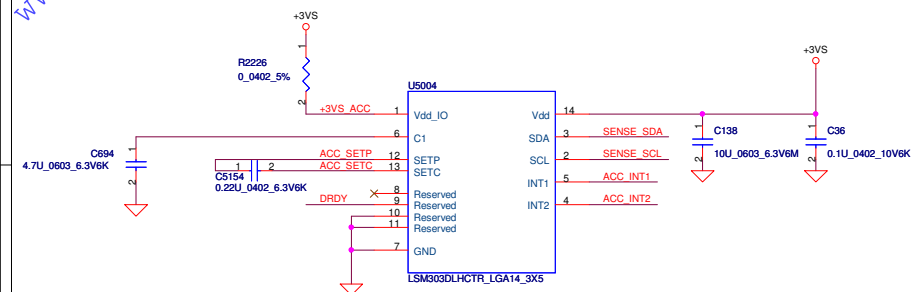


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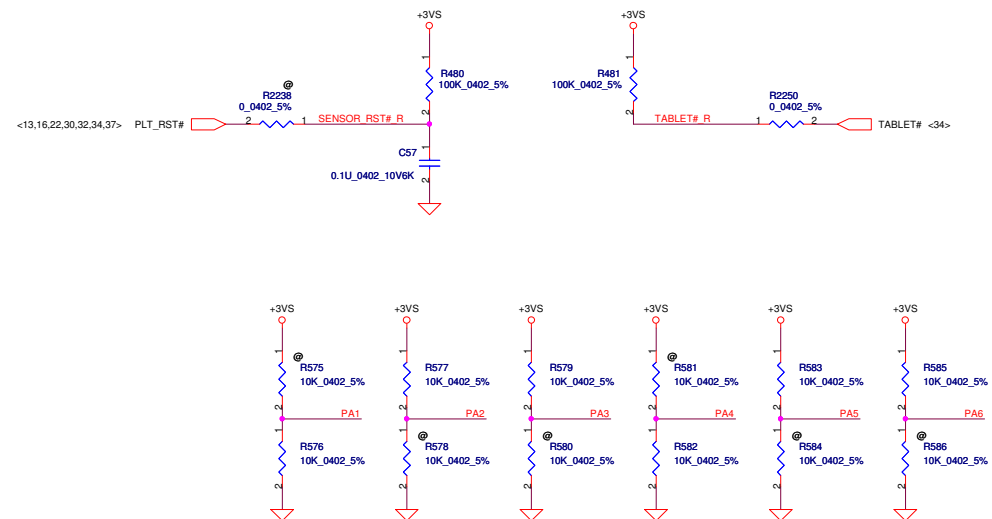
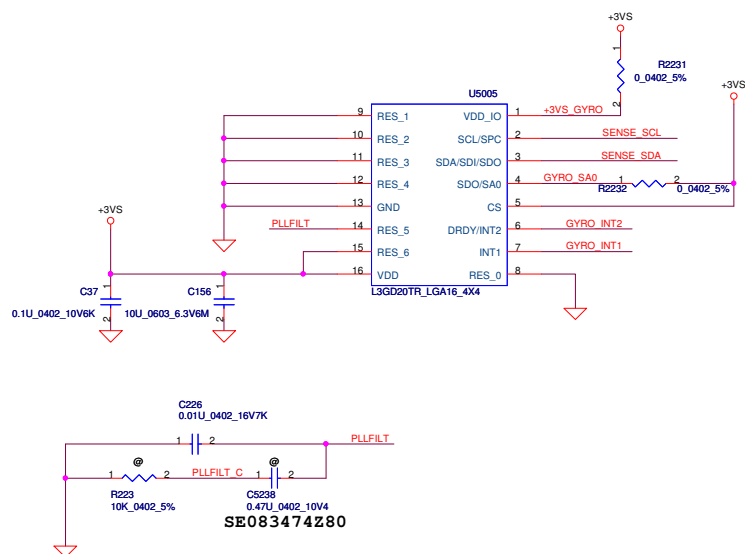


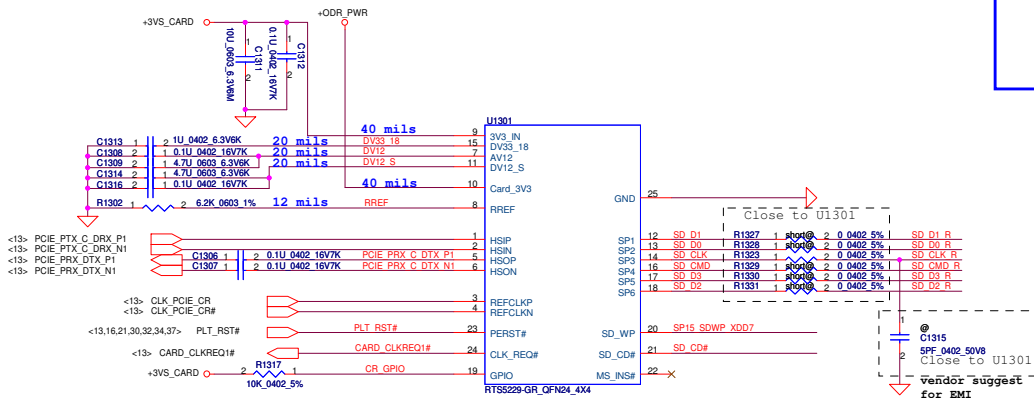
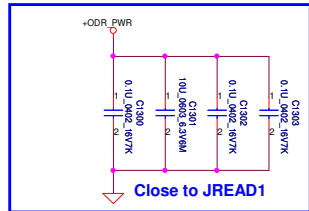
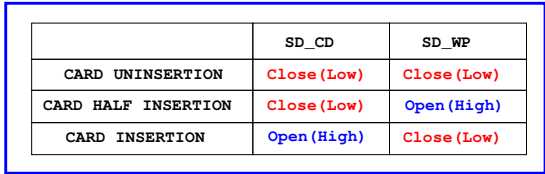


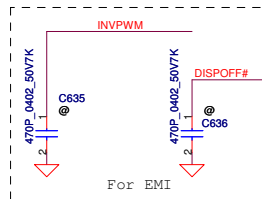
Sensor Hub



Gyro

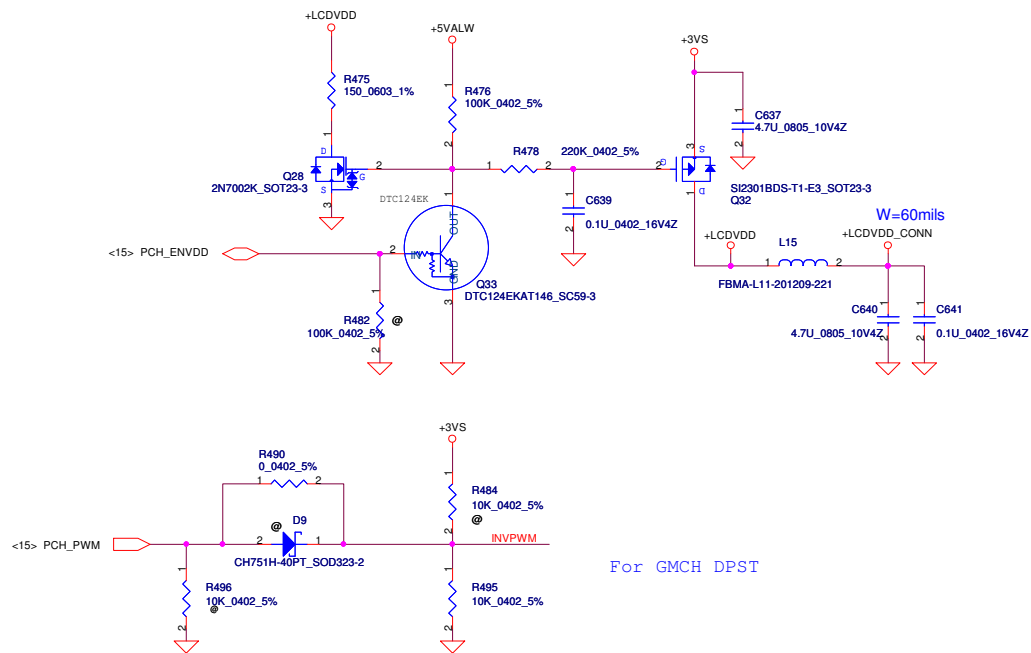






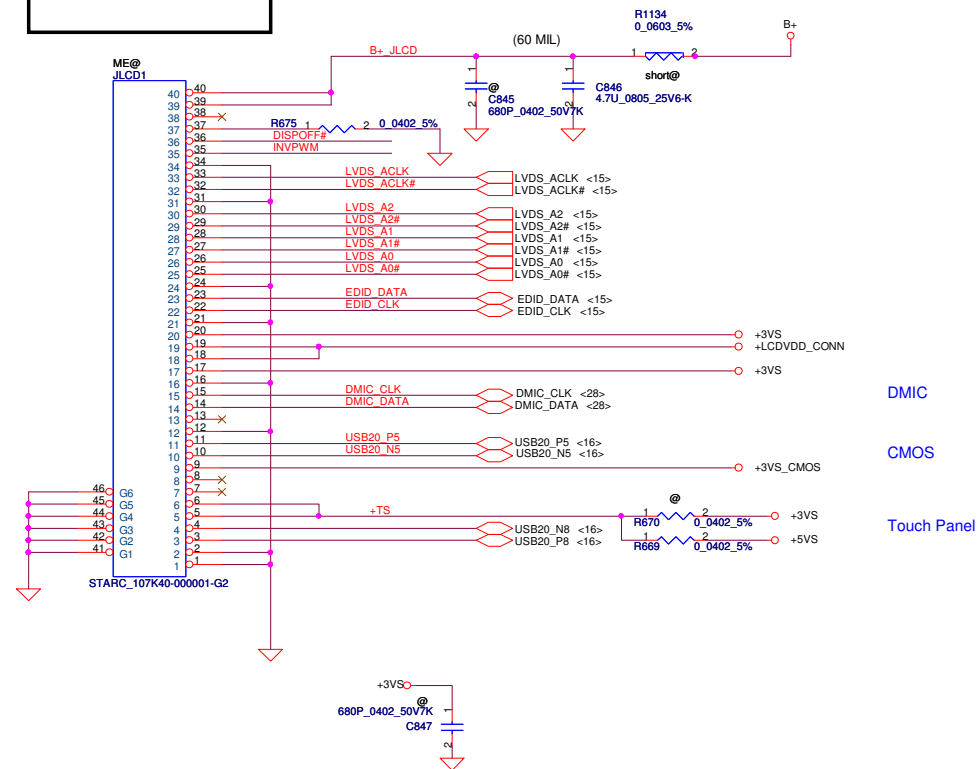
W=60mils

LCD POWER CIRCUIT

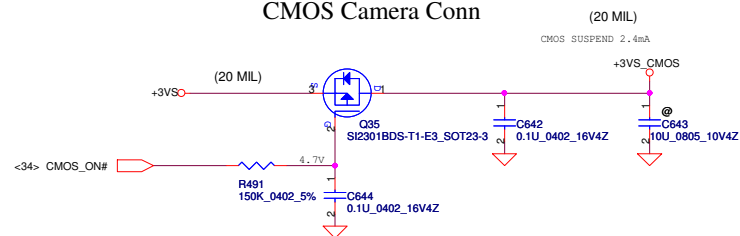


For GMCH DPST

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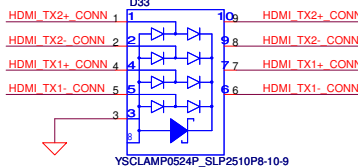
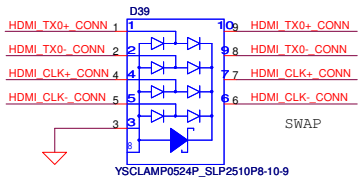
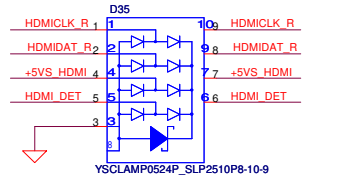
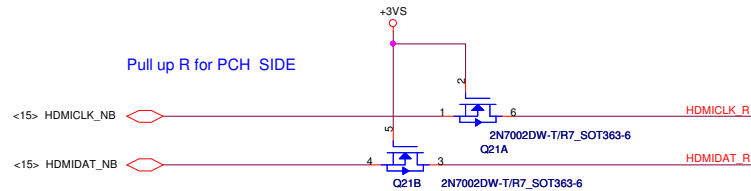
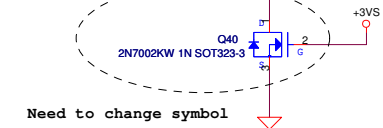
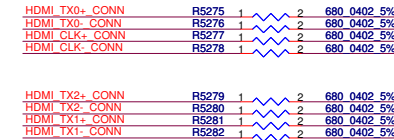
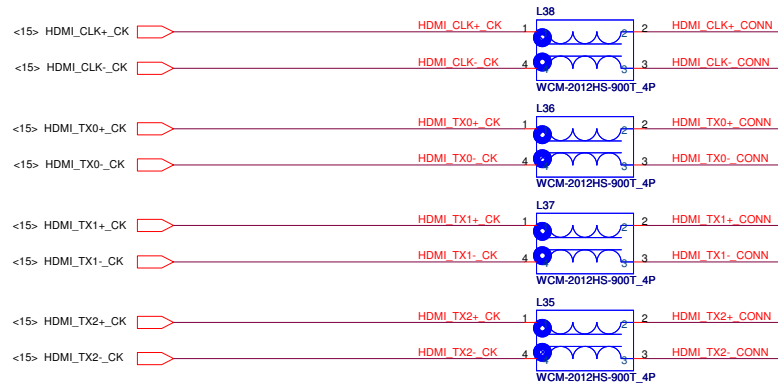


CMOS Camera Conn

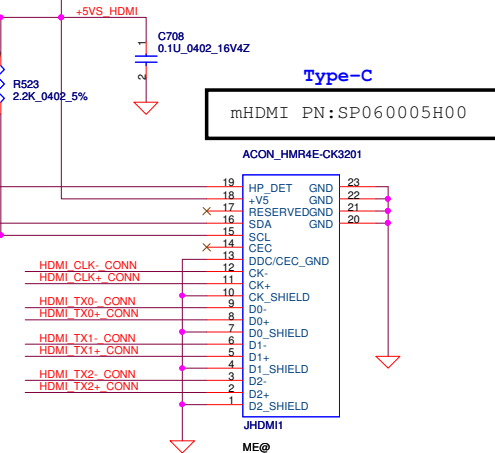
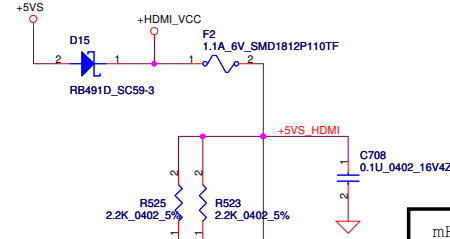
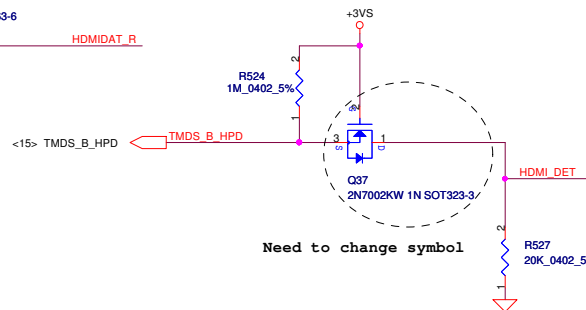


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Date: Friday, July 27, 2012		Sheet 23 of 50			

PN:SM070001S00x 4

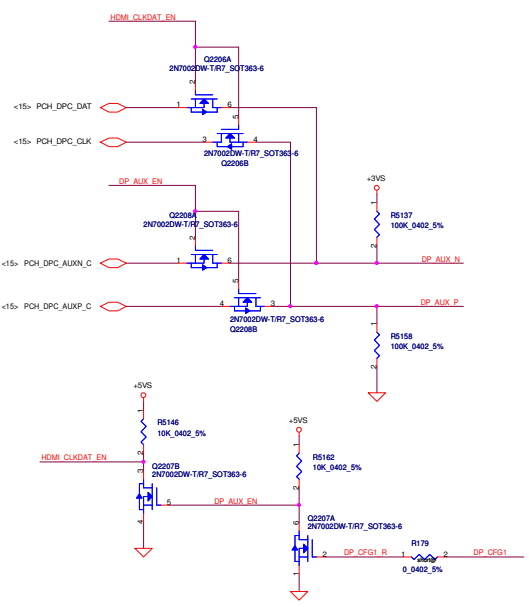
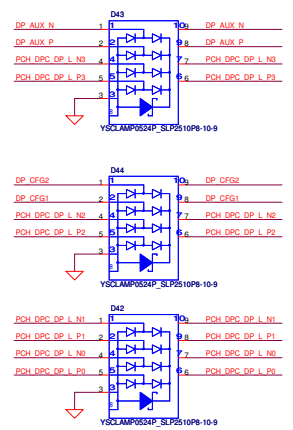
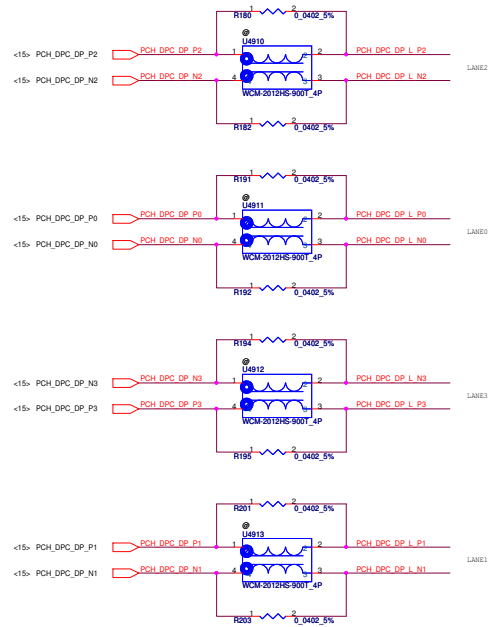


1'SPN: SC300001Y00
2'SPN: SC300002800



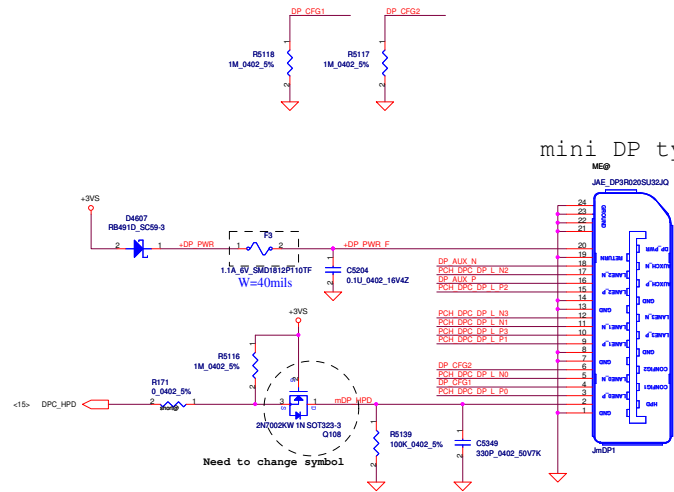
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/08/25	Deciphered Date	2012/08/25	Mini-HDMI	
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				Document Number	1.0
				LA-8671P SDV	
				Date	Friday, July 27, 2012
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Close to JmDP1



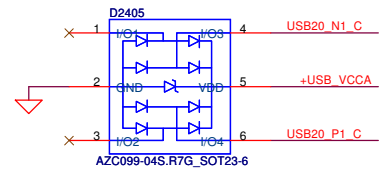
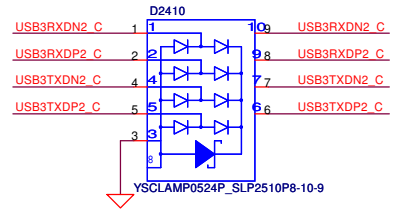
TBT, HDMI, DP mode table

HPD	CFG1	CFG2	LSRX	Mode
1	0	0	X	DP
1	1	X	X	HDMI
0	0	1	1	TBT



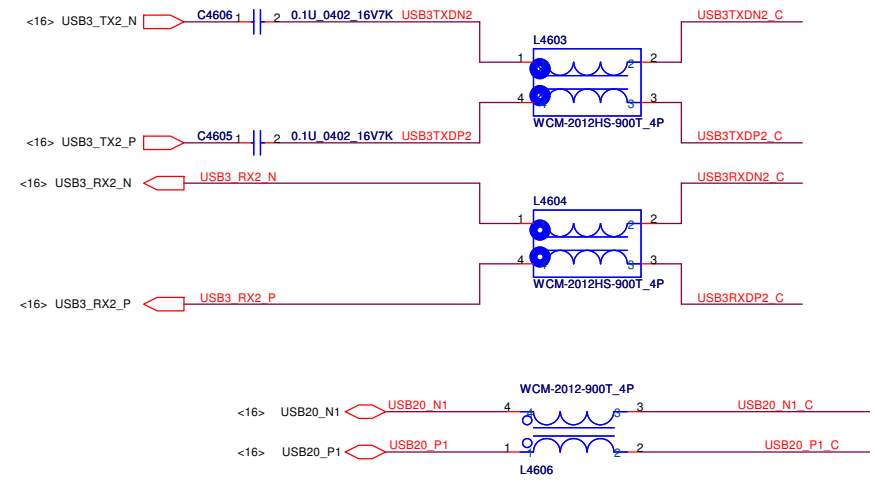
mini DP type

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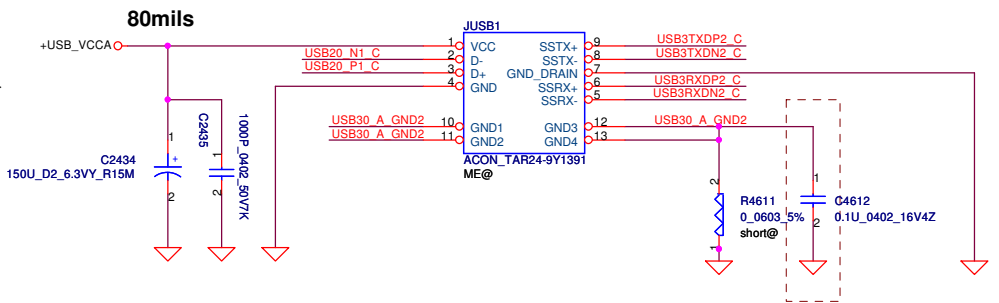
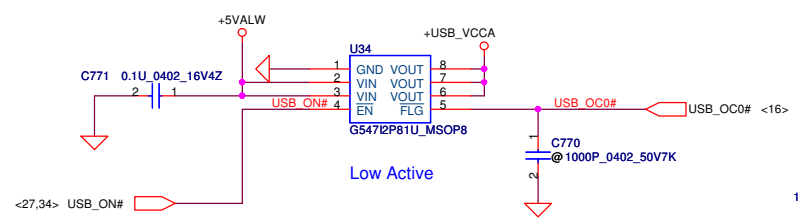


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2'S PN: SC300002E00

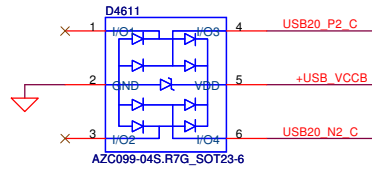
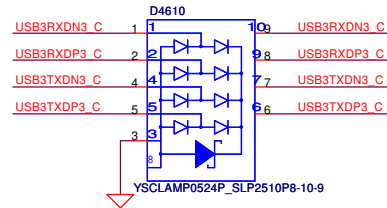
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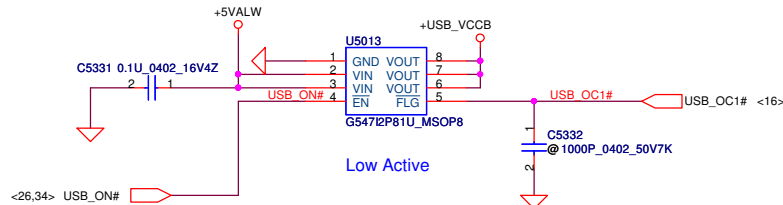
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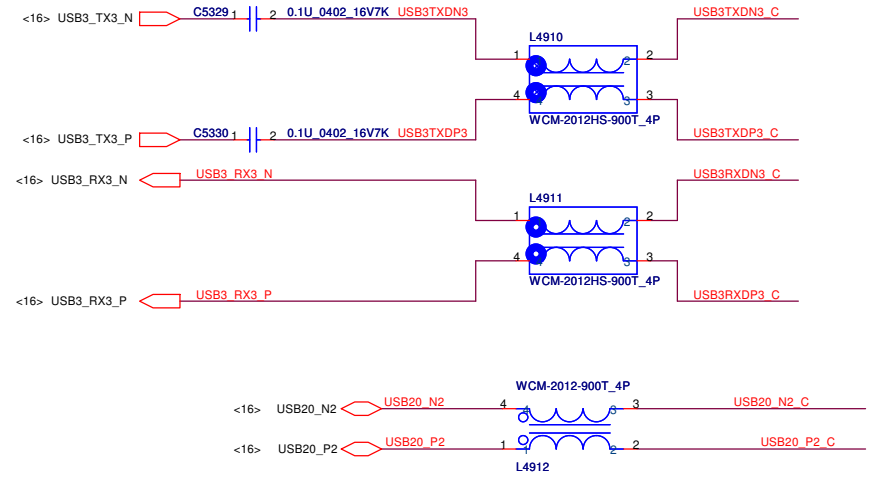
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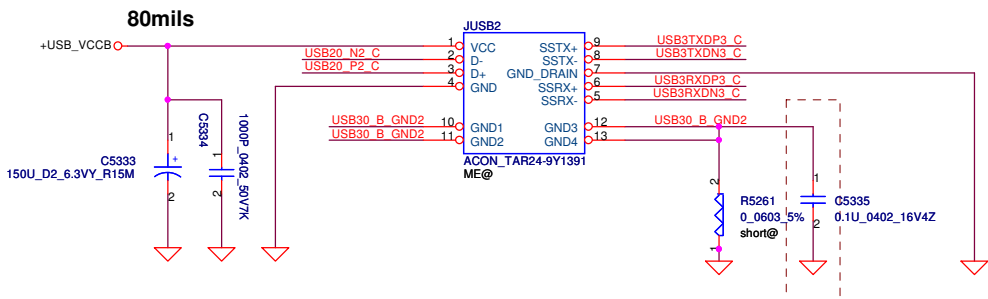
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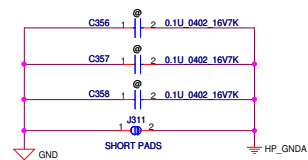
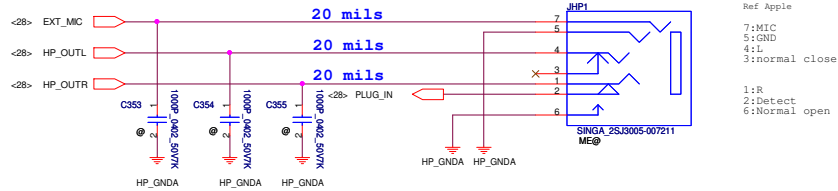
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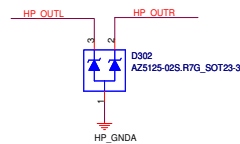
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Issued Date		2011/05/16		Deciphered Date		2013/05/16		Title					
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								Size		Document Number		Rev	
								Custom		LA-8671P_SDV		1.0	
								Date:		Friday, July 27, 2012		Sheet 27 of 50	

PN:DC230008E00

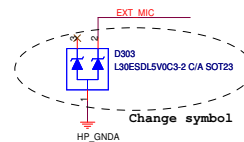
Choose normal-open type!



GND

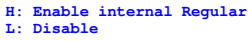


PN: SCA00001I00

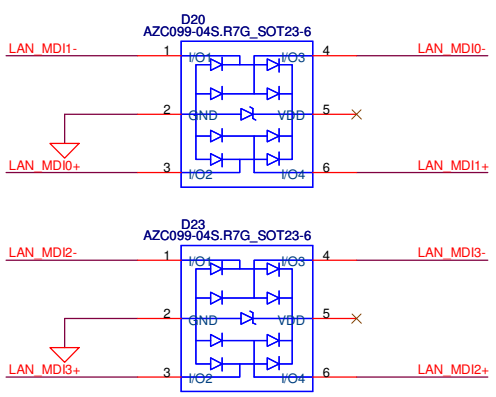
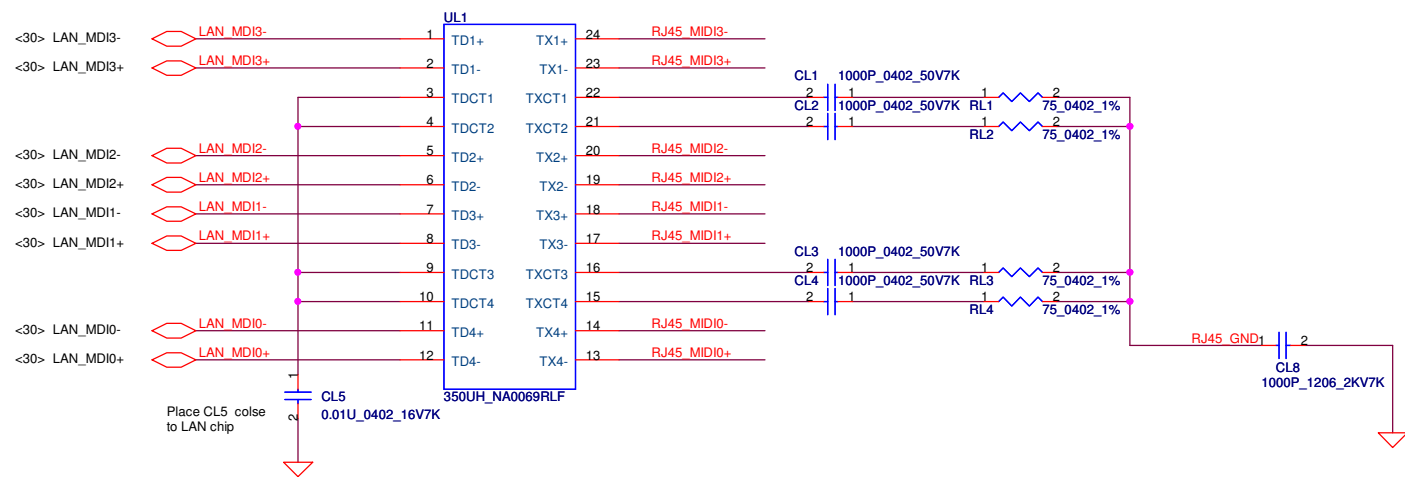


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				Date:	Friday, July 27, 2012
				Sheet	29 of 50
				Rev	1.0



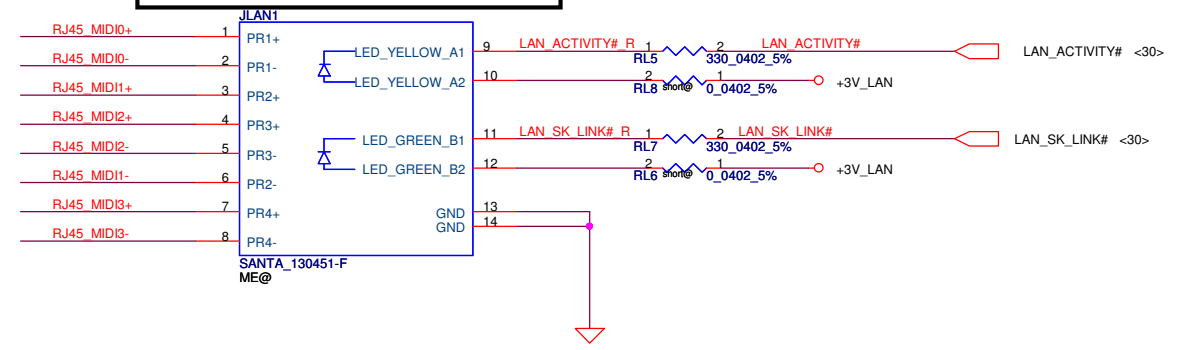
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Issued Date	2010/08/25		Deciphered Date	2012/08/25		Title	
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				Size	Document Number	Rev	
				Custor	LA-8671P_SDV	1.0	
				Date:	Friday, July 27, 2012	Sheet 30 of 50	



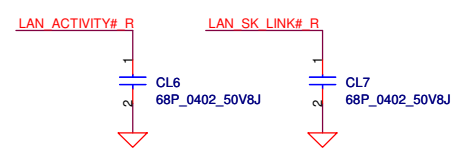
D20/D23
1'S PN:SC300001G00
2'S PN:SC300002E00

DC234005300
LAN Conn.

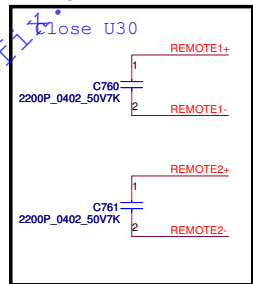
RL5,RL7 Vendor recommend 510 ohm



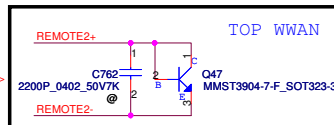
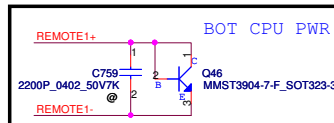
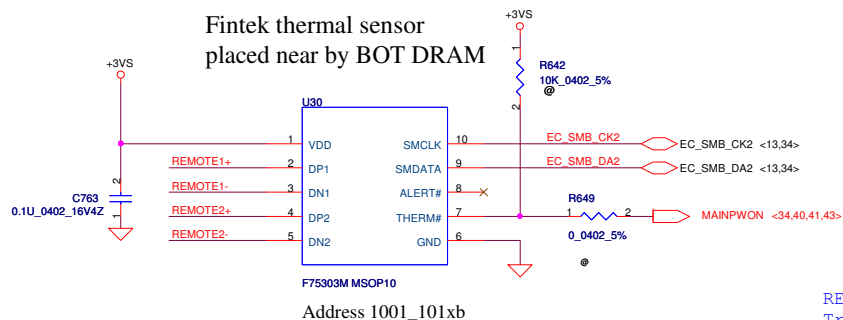
For EMI's request



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Size Custom		Document Number		Rev	
		LA-8671P_SDV		1.0	
Date: Friday, July 27, 2012		Sheet		31 of 50	

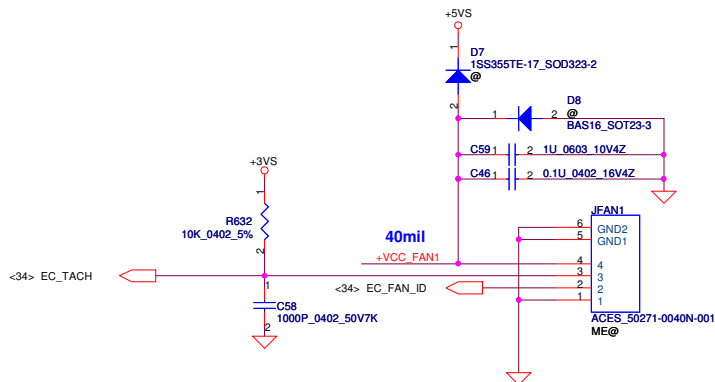
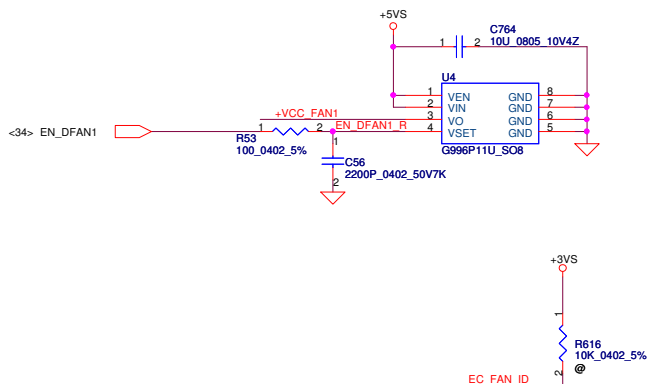


Fintek thermal sensor
placed near by BOT DRAM



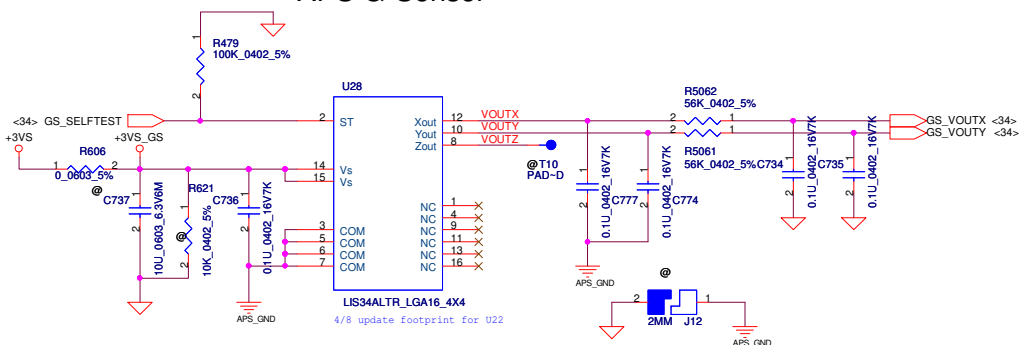
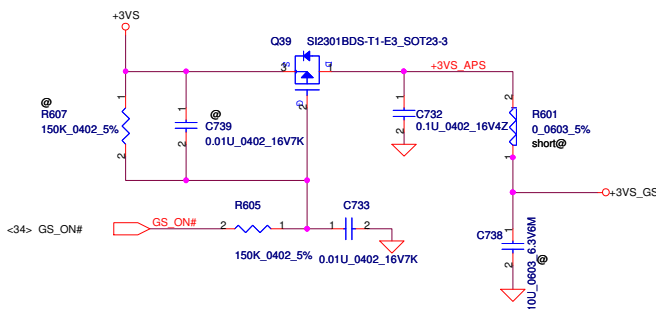
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN +5VS DROOP



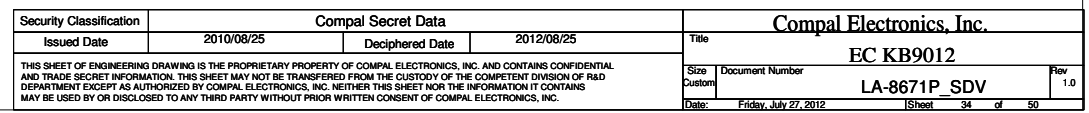
SP02000TS00

APS G-Sensor

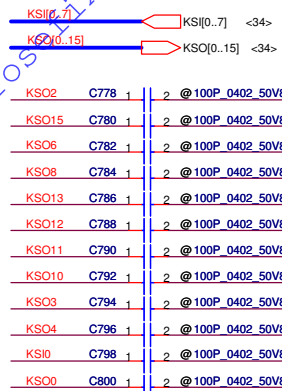


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Issued Date			2010/08/25			Title		
			Deciphered Date			FintekF57303_ Thermal sensor/FAN		
						Size		
						Document Number		
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						Date: Friday, July 27, 2012		
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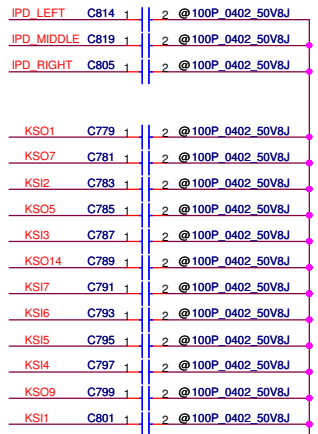
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INT_KBD Conn.



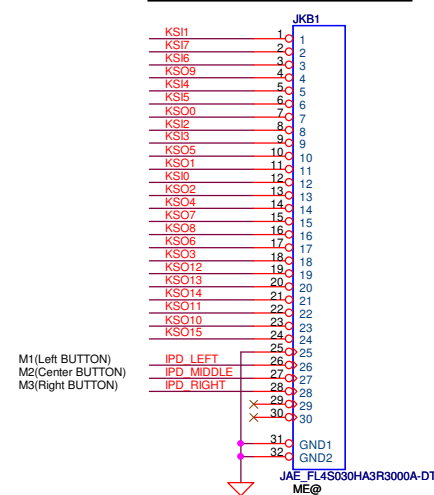
CONN PIN define need double check



Reserve for ESD.

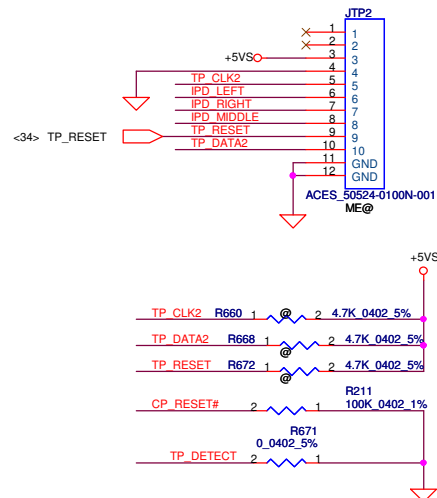
INT_KBD Conn.

PN:SP01000YH00



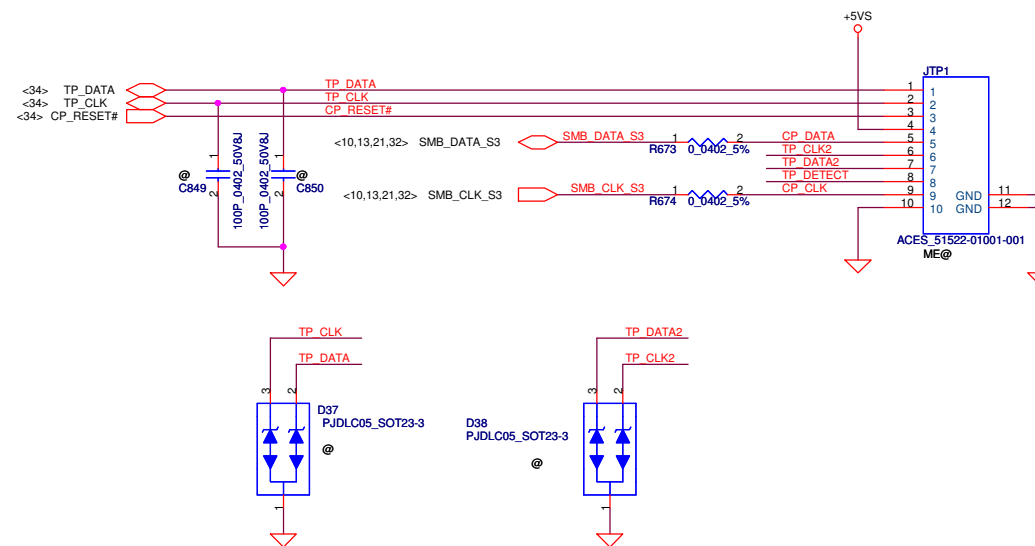
Track point

PN:SP01001CH00



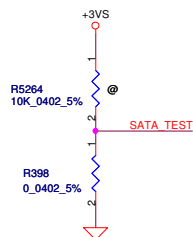
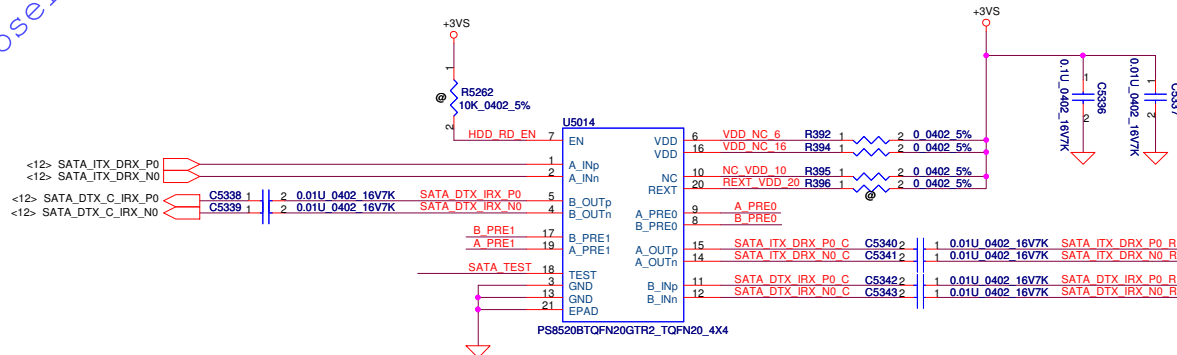
Click pad 10PIN

SP01001AL00

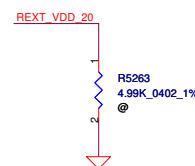


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				LA-8671P_SDV	
				Date: Friday, July 27, 2012	Rev 1.0
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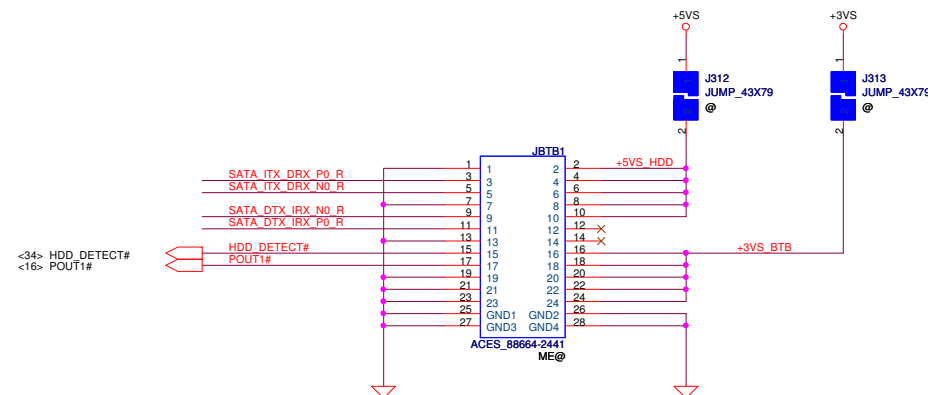
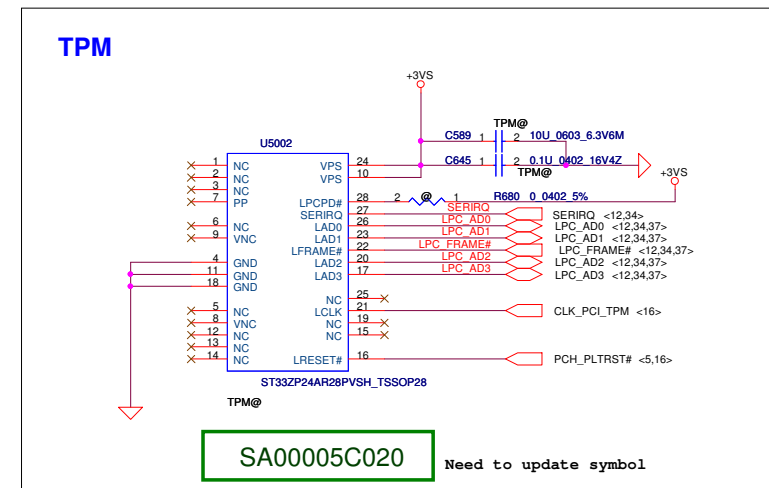


	TEST (Internal Low)
Normal Mode (Default)	LOW
Test Mode	HIGH

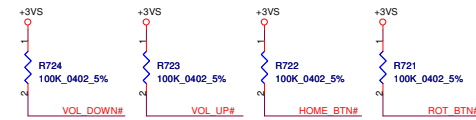
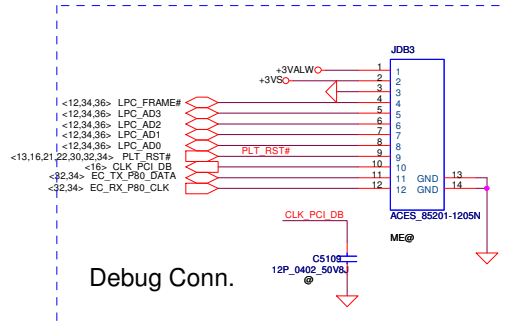
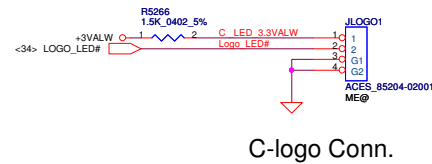
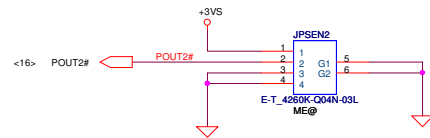
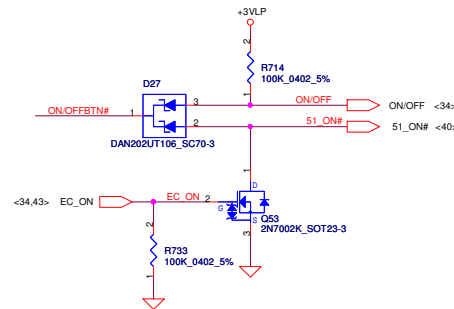
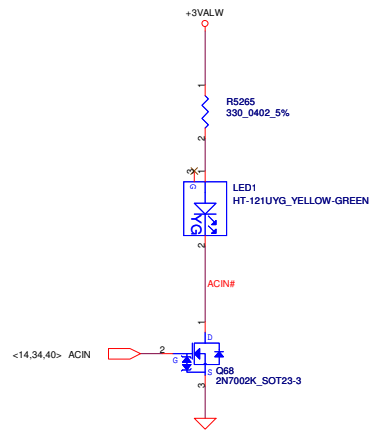


Remove pull-low

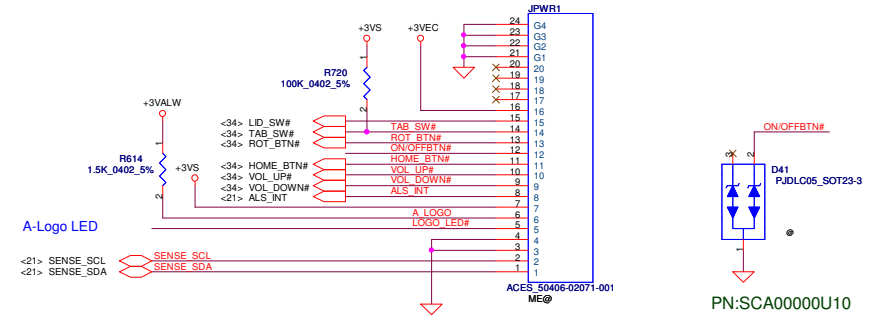
	A_PRE1/B_PRE1 (Internal pull Low)	A_PRE0/B_PRE0 (Internal pull Low)
0dB, no pre-emphasis	Low	Low
1.5dB pre-emphasis is selected	Low	High
2.5dB pre-emphasis is selected	High	Low
3.5dB pre-emphasis is selected	High	High



AC-IN LED (Color : Green)

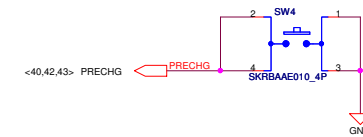


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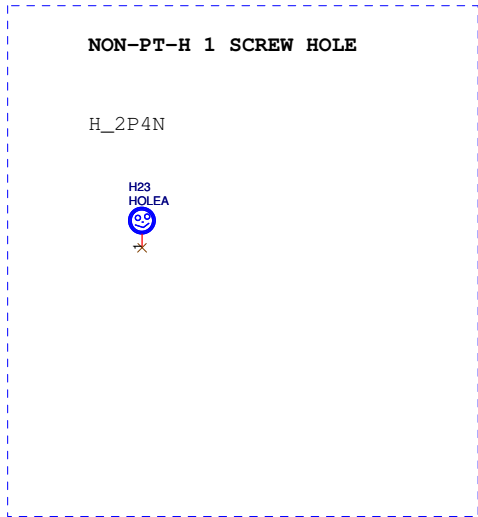
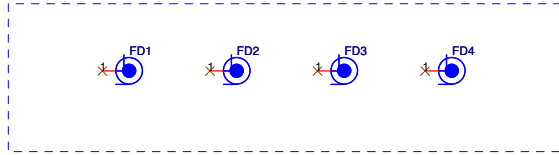
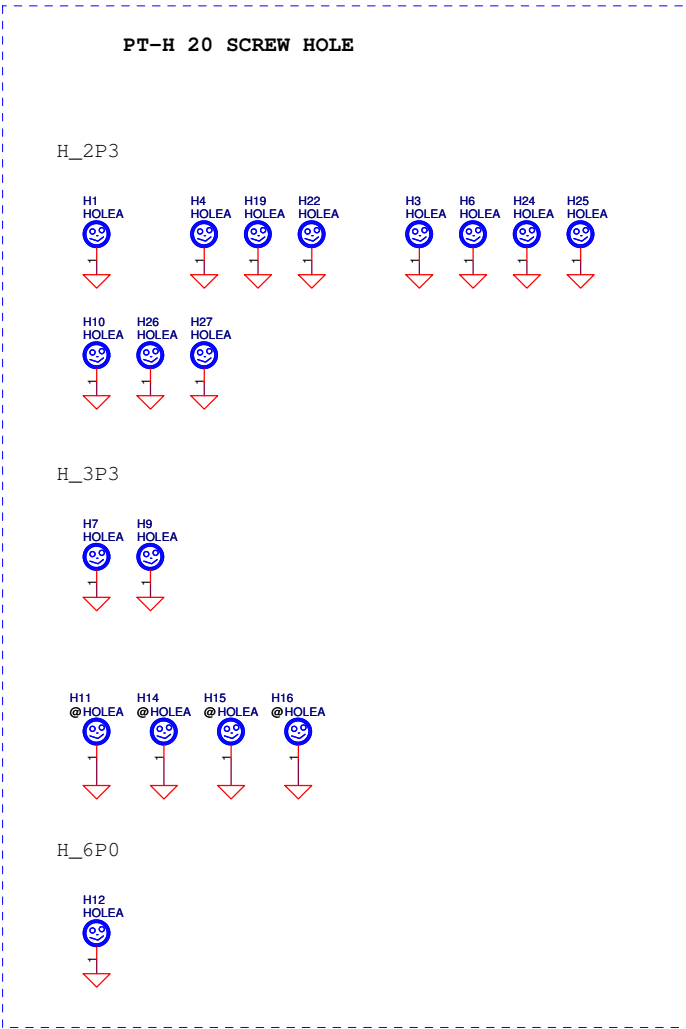
Power Board connector

BOTTOM SIDE
SN111005800 by ME drawing

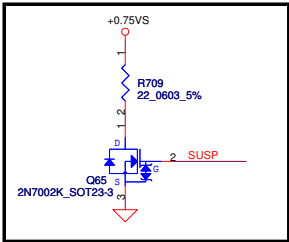
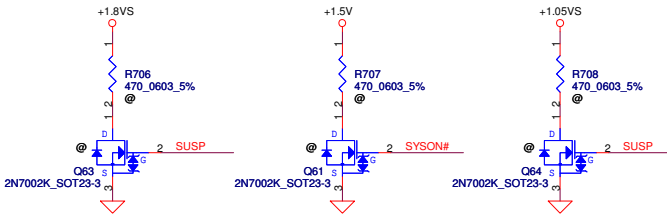
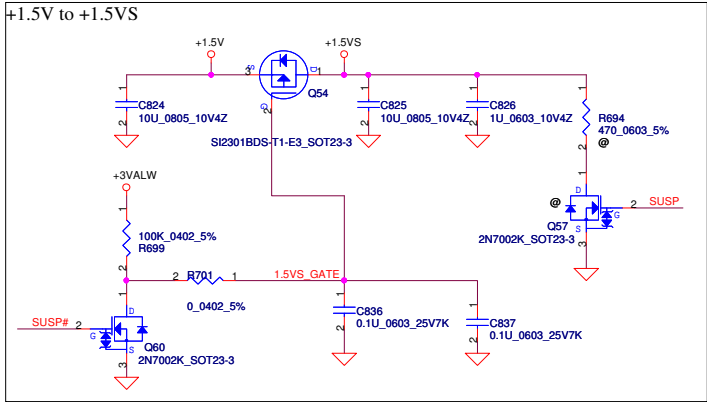
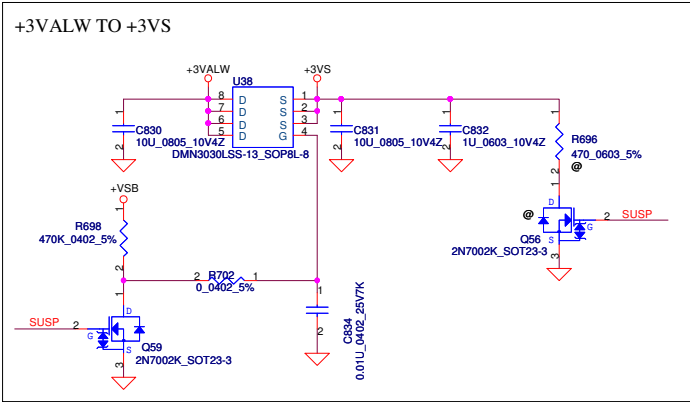
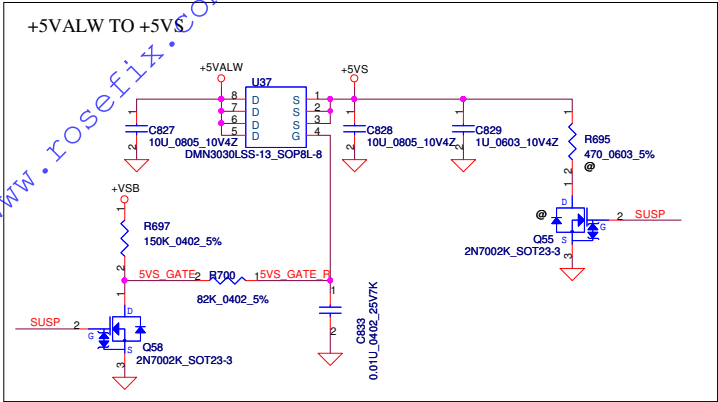


For Power Reset

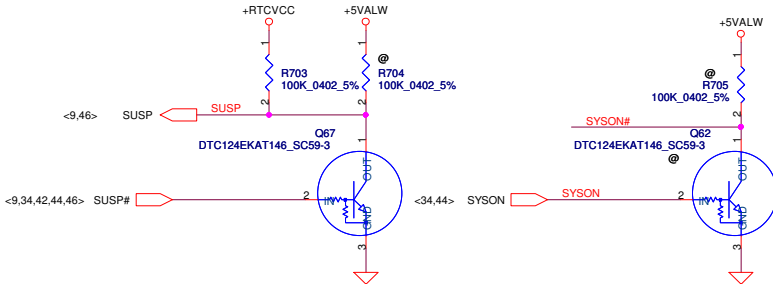
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For Intel S3 Power Reduction.

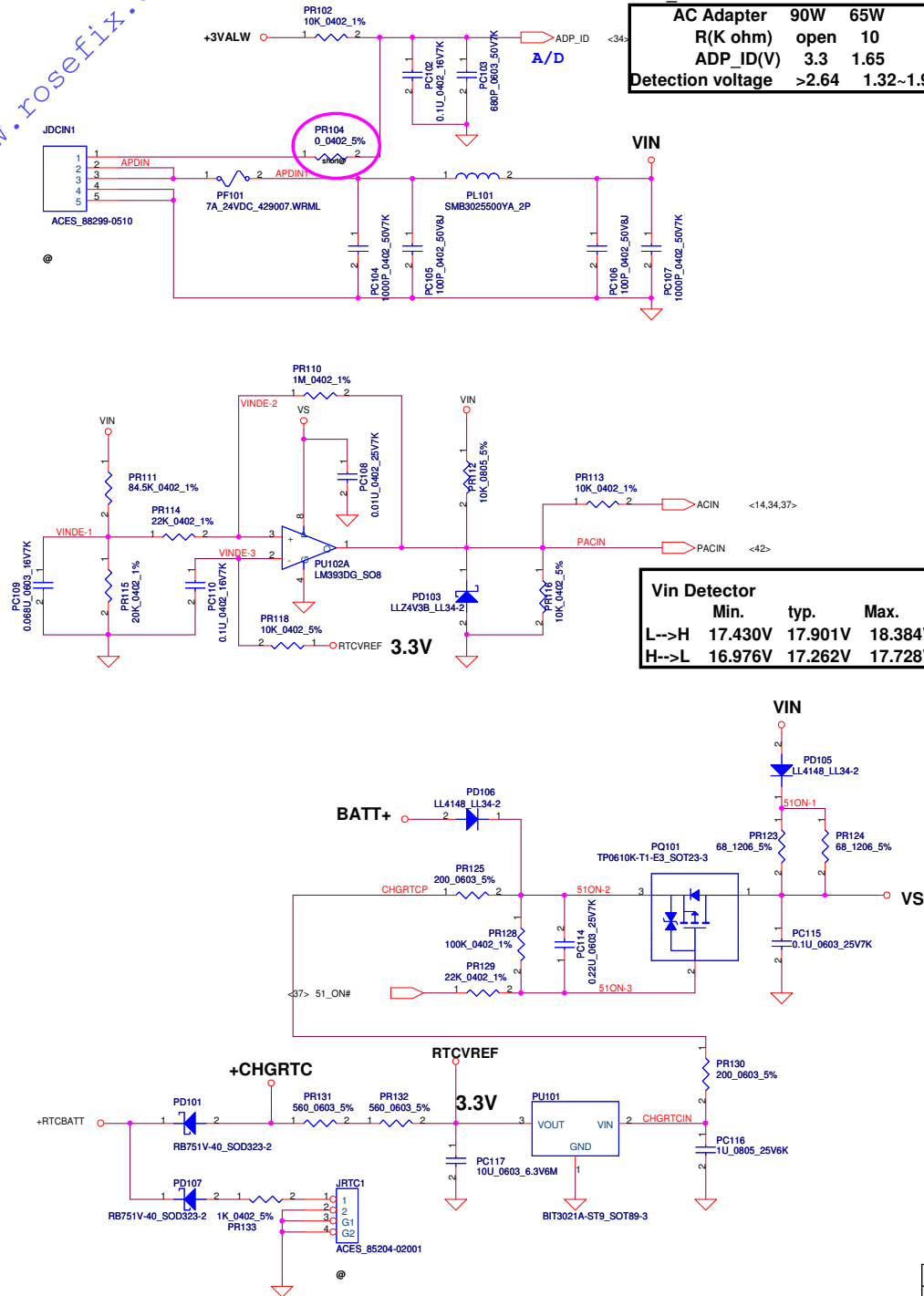


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Size		Document Number		Rev	
Custom		LA-8671P_SDV		1.0	
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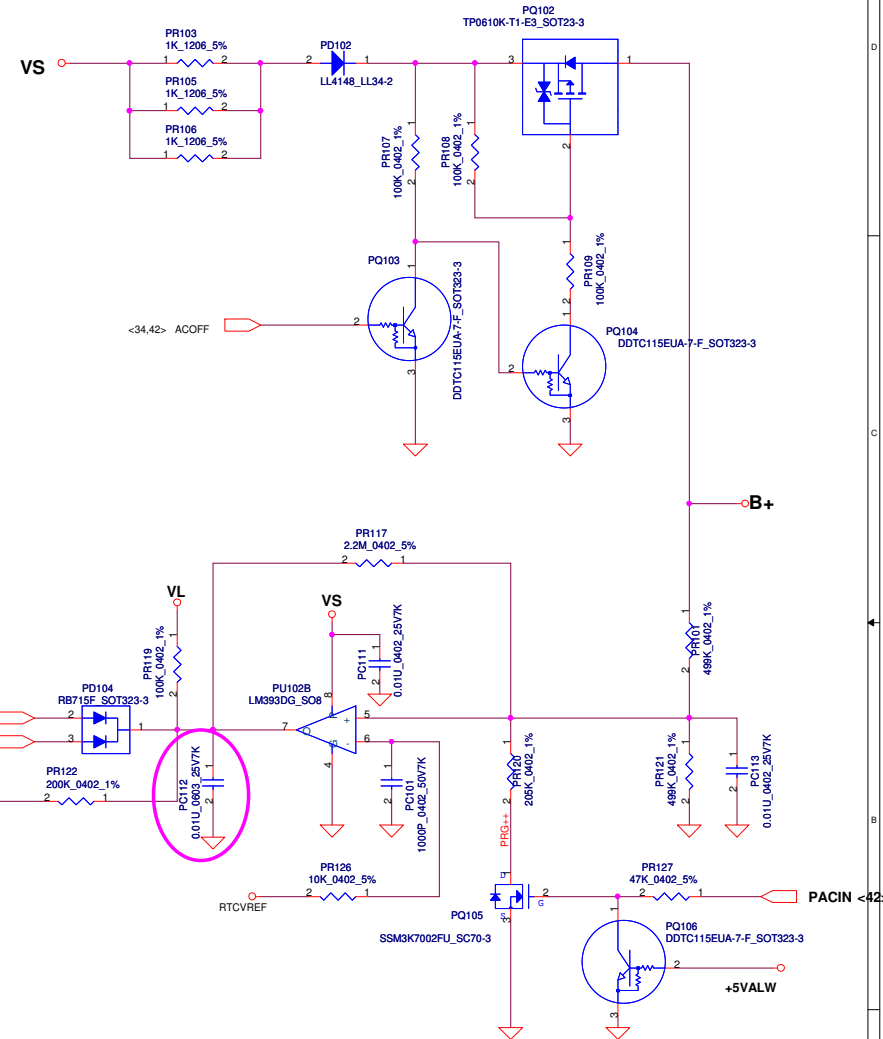
ADP_ID

AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

Precharge detector 15.97V/14.84V FOR ADAPTOR



Vin Detector	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

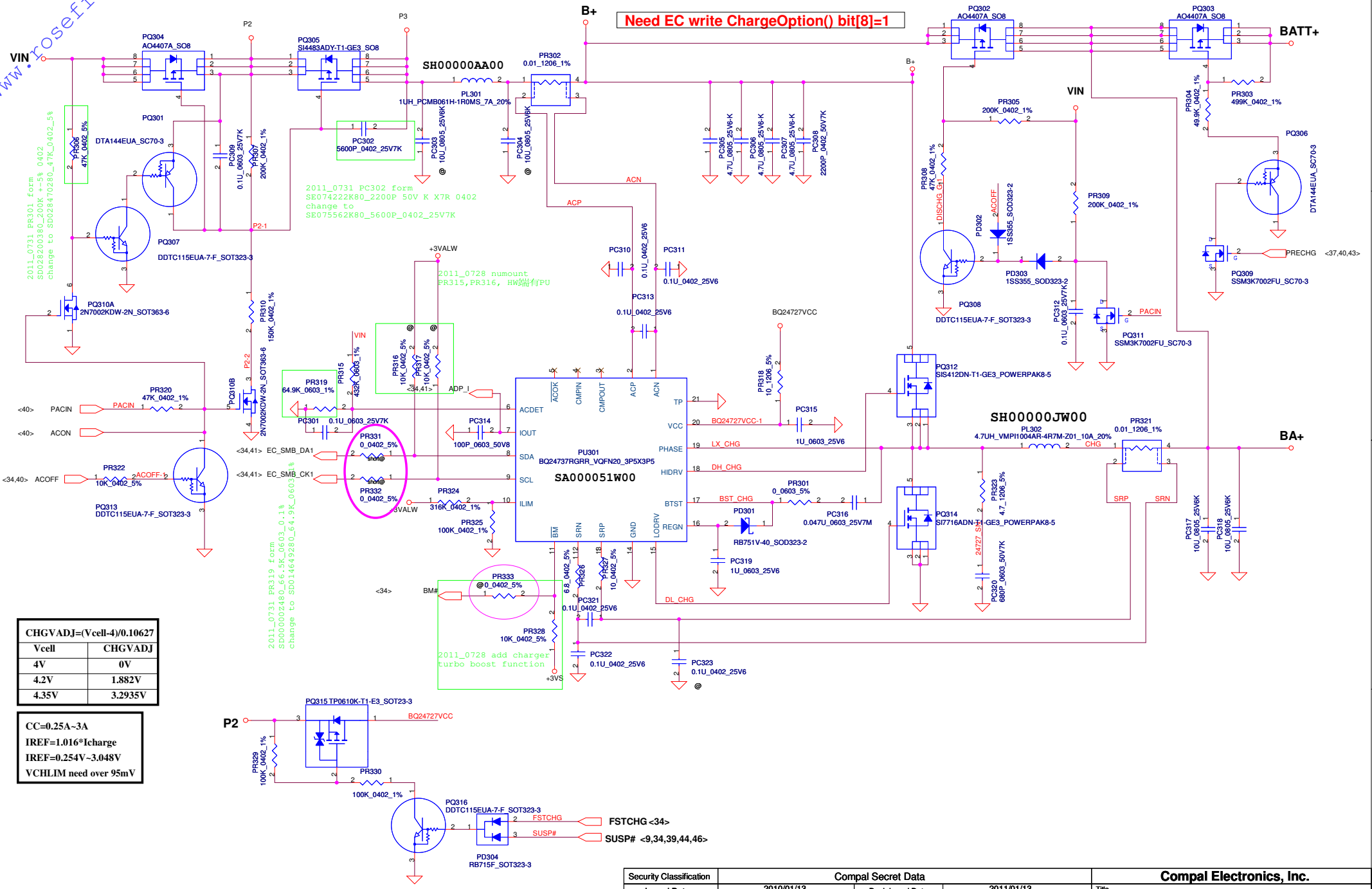
Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



**For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212**



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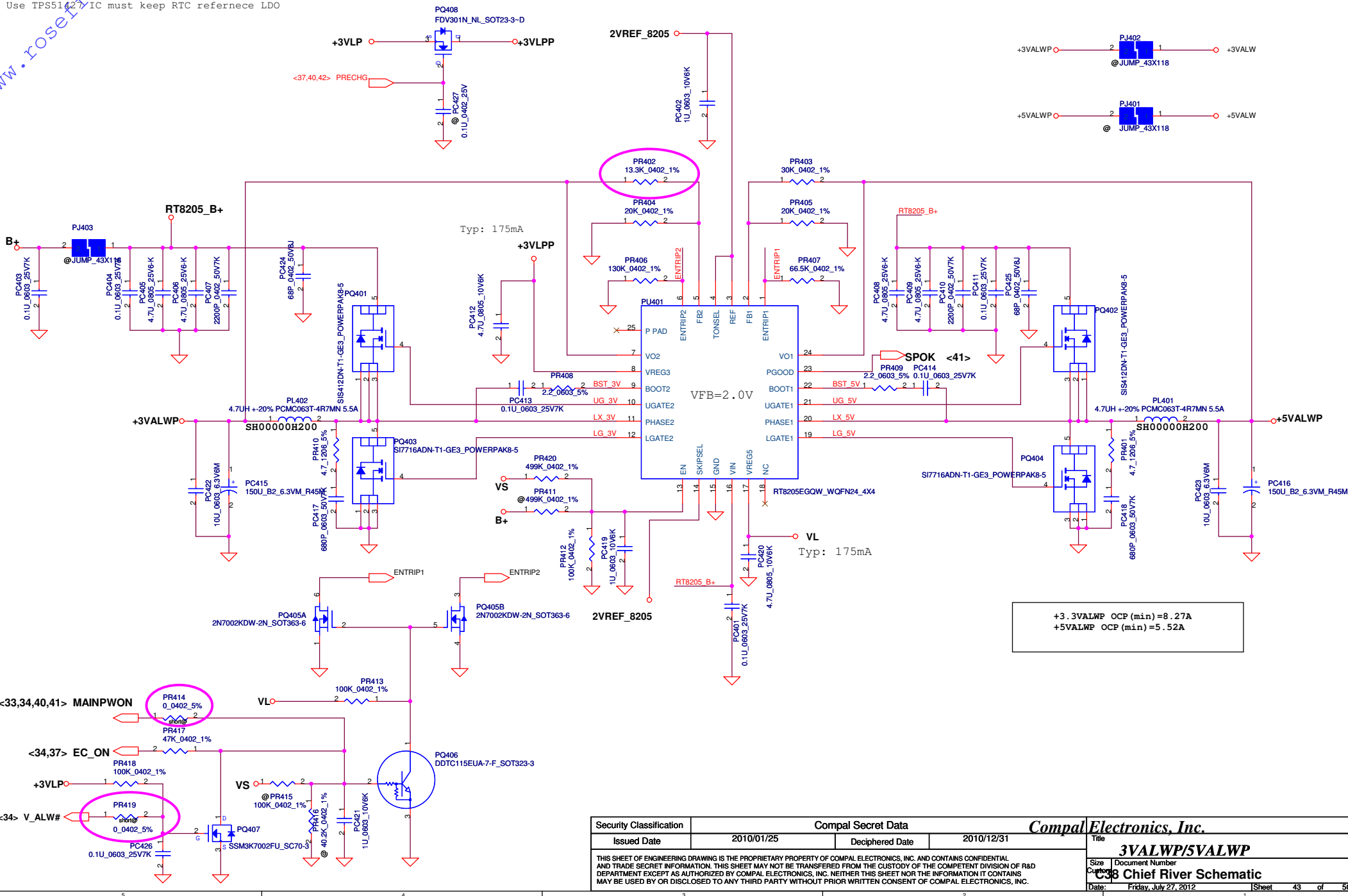


Need EC write ChargeOption() bit[8]=1

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A
 IREF=1.016*Icharge
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

Note:
 Use TPS51125 IC can remove RTC reference LDO
 Use TPS51425 IC must keep RTC reference LDO



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				C38	Chief River Schematic
				Date:	Friday, July 27, 2012
				Sheet	43 of 50
				Rev	0.4

<34,39> SYSON

2011_0801 JP504 form
43x118 change to 43x79

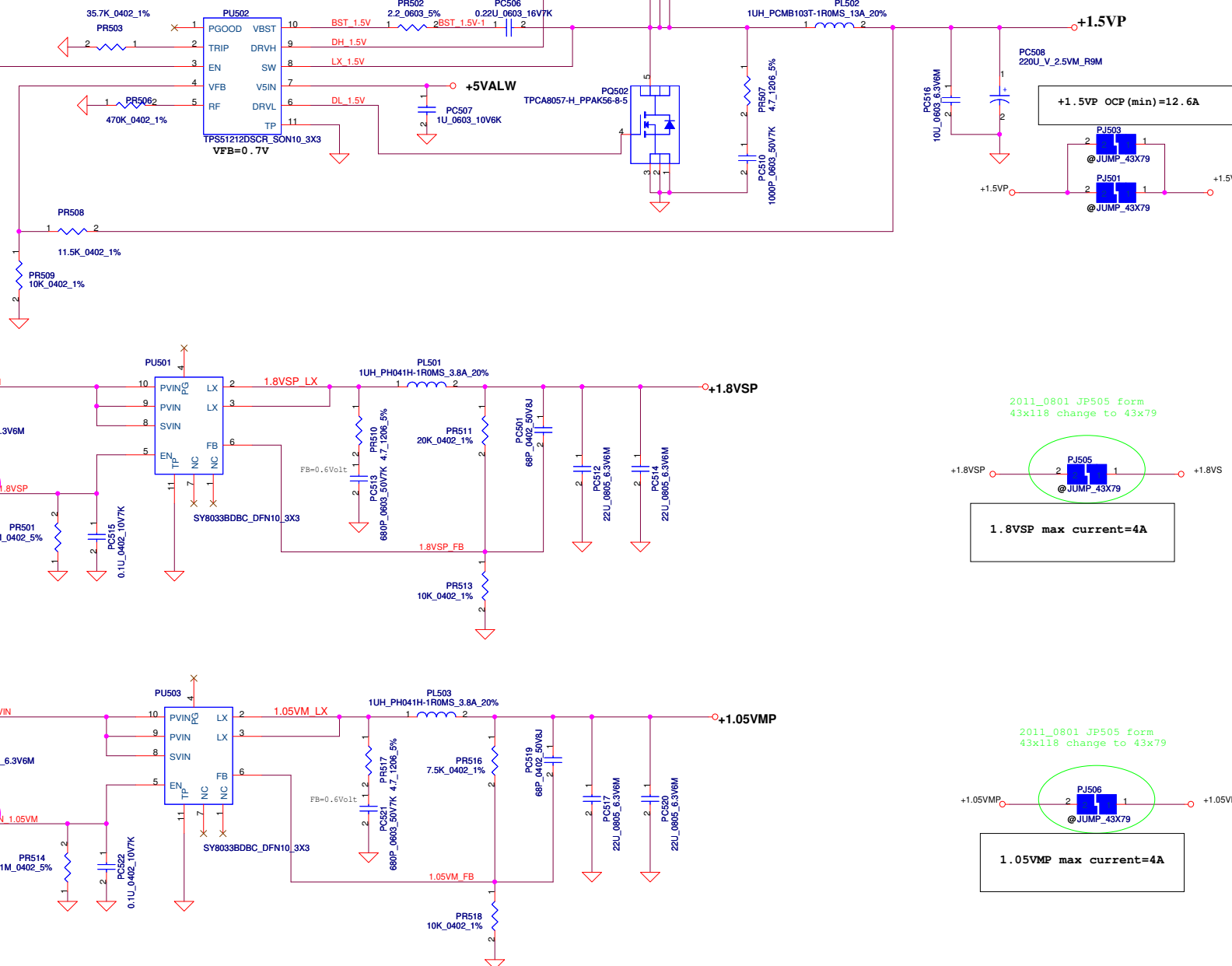
+5VALW

<9,34,39,42,46> SUSP#

2011_0801 JP504 form
43x118 change to 43x79

+5VALW

<19,34> M_PWR_ON



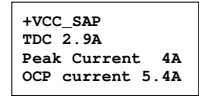
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				C38 Chief River Schematic	0.4
Date: Friday, July 27, 2012		Sheet		44	of 50

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vid [0]
0
0
1
1

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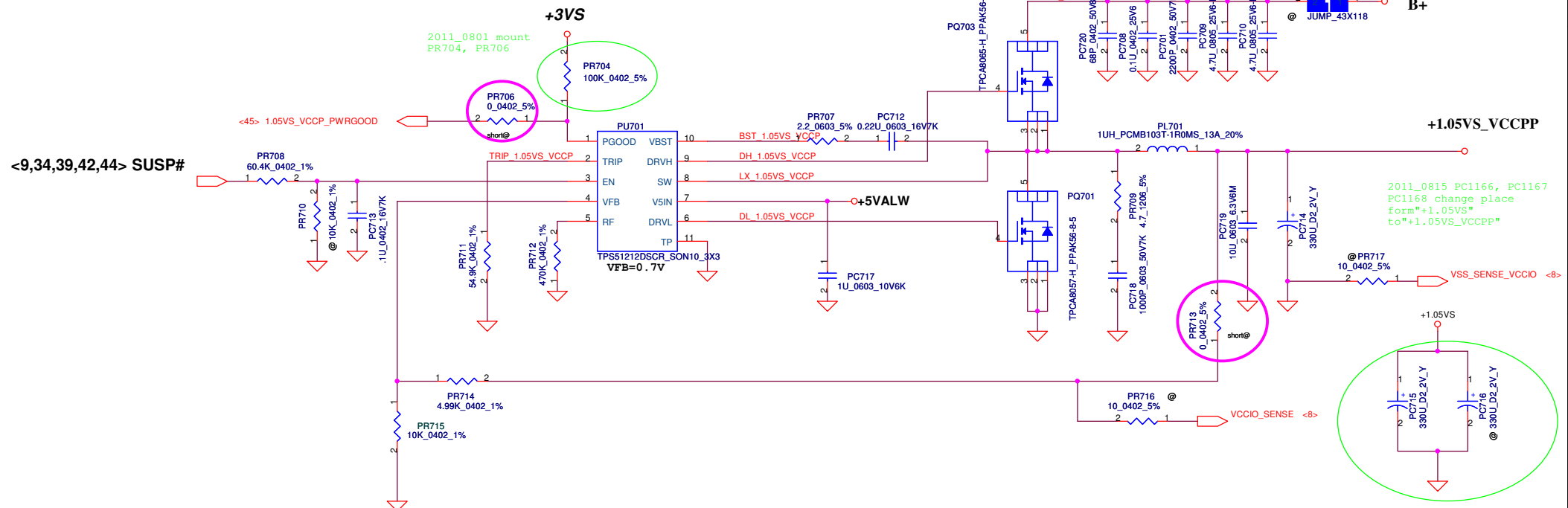
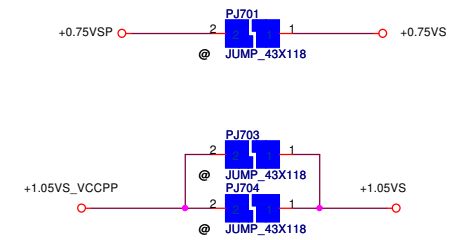
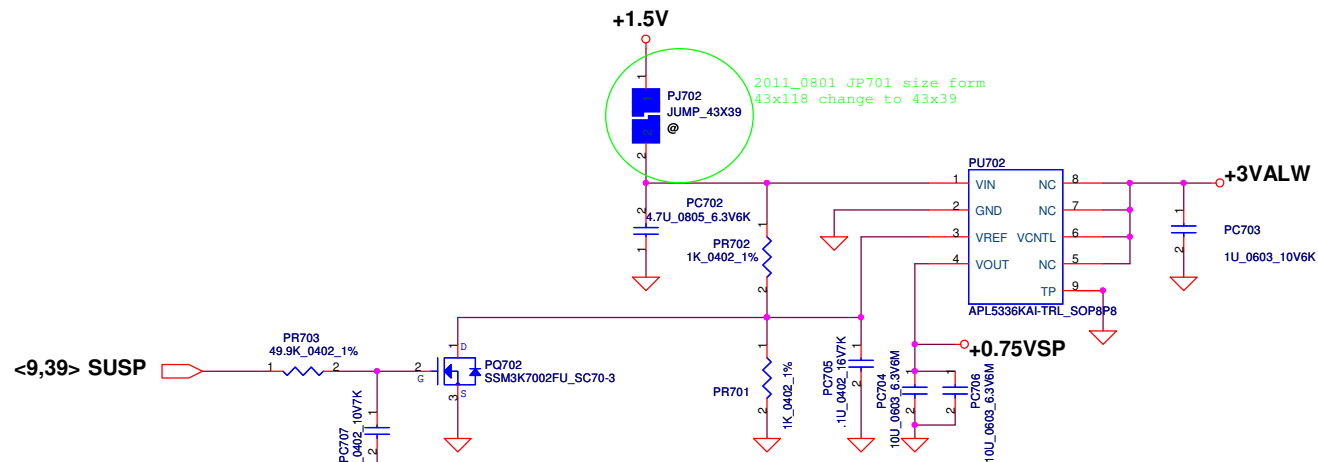
output voltage

BVALW

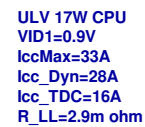
**The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.**

+VCCSAP  **+VCCSA**

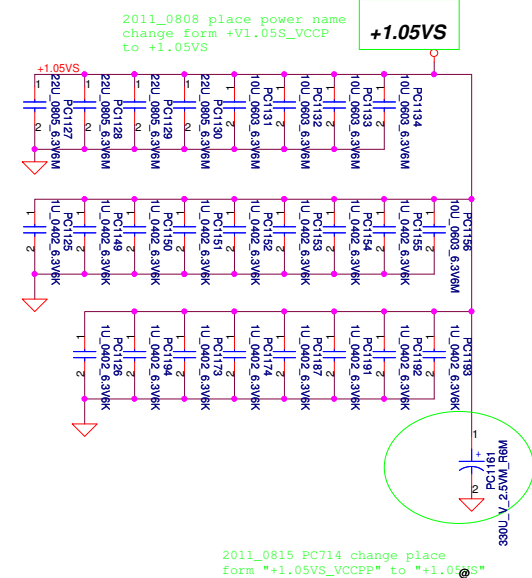
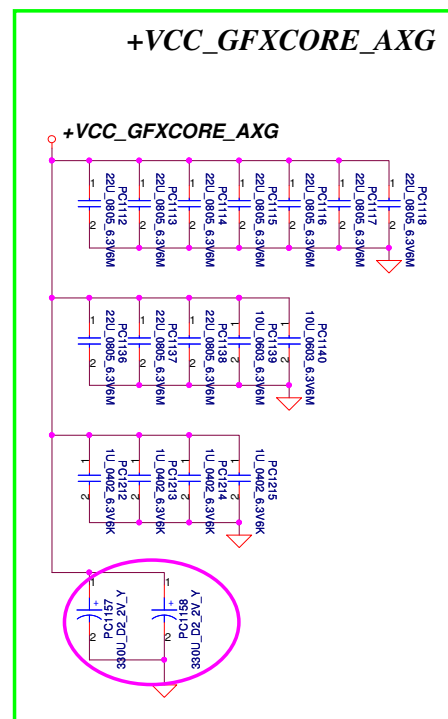
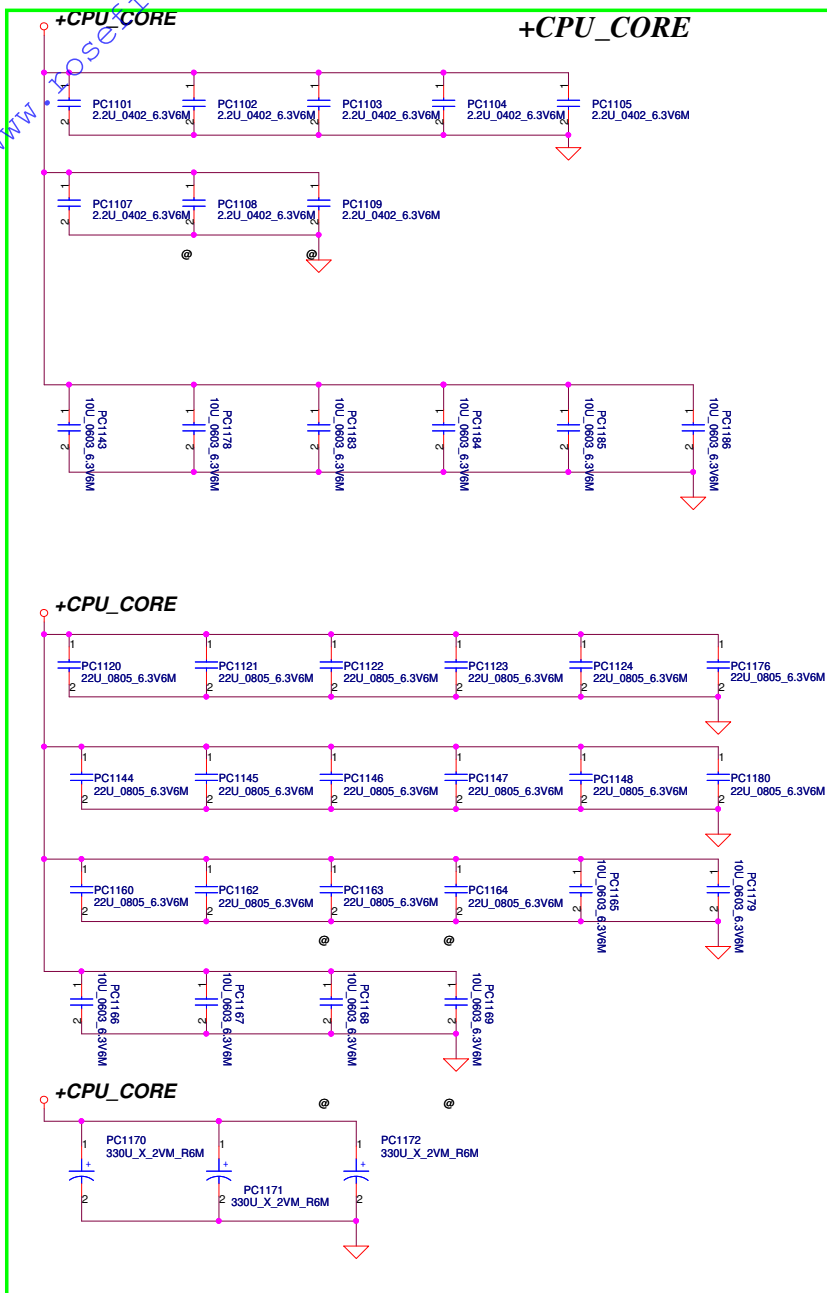
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2011_0801 del +V1.05S_VCCPP circuit
```



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Issued Date		2009/12/01		Title PWR-CPU CORE	
		Deciphered Date		2010/12/31	
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				Date Friday, July 27, 2012	Rev 0.4
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Issued Date	2008/09/15	Deciphered Date	2009/09/15	Title	
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				Document Number	
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Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	NCP6132A update SPEC	P47	Remove PR916, PR945	2012/06/05	
2	Thermal verfy PH1 setting point	P41	Change PR208 value to 18.2K	2012/06/08	
3	ME demand : Keyboard assembly issue	P44	Change PL401, PL402 to High=2.4mm (SH000000H200)	2012/06/08	
4	Noise is PASS, Don't need 33u CAP	P48	Remove PC1023, PC1024	2012/06/08	
5					
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				C38 Chief River Schematic	
Date: Friday, July 27, 2012		Sheet 50 of 50		Rev 0.4	