Berry DG15 Discrete/UMA Schematics Document

Arrandale

Intel PCH

2009-10-12

REV : X00

DY :None Installed
UMA:UMA platform installed
DIS:DIS platform installed
Madisan:gDDR3 1GB platform installed
Colay :Manual modify BOM

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*

Size: A3 | Document Number: *Berry* | Rev: *X00*

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Berry Block Diagram (Discrete/UMA co-lay)

1.Madison-LP; 1GB (64Mx16b*8)
2.Park-XT;512MB (64Mx16b*4)
(1 and 2 co-lay)

##OnMainBoard

VRAM 1GB/512MB 85,86,87,88

DDR3 800MHz

Project code : 91.4HH01.001
PCB P/N : 48.4HH01.0SA
Revision : 09909-SA

Clock Generator SLG8SP585 7

AMD Graphic
Madison-LP / Park-XT (Discrete only)
80,81,82,83,84

PCIe x 16 (Discrete only)

Intel CPU
Arrandale
8,9,10,11,12,13,14

DDRIII 800/1066 Channel A
DDRIII 800/1066 Channel B

DDRIII 800/1066 Slot 0 18
DDRIII 800/1066 Slot 1 19

FDIx4x2 (UMA only)
DMIx4

Discreet/UMA Co-lay

HDMI 57
LCD 54
HDMI Level shifter 57
LVDS(Dual Channel)
RGB CRT

Intel PCH HM57
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24,25,26,27,28

PCIE x 3
SATA x 1
USB 2.0 x 4

I/O Board Connector 76

PCIE x 1 USB x 1
PCIE x 1

Mini-Card 802.11a/b/g
10/100 NIC Realtek RTL8103T
RJ45 CONN

SATAx1 / USB2.0x1
ESATA/USB Combo

PCIE x 1,USB x 1
Mini-Card WWAN
SIM

USB 2.0 x 1
Right Side: USB x 1

CRT
Left Side: USB x 2
CRT Board 77

Bluetooth 73
CAMERA 54
USB2.0 x 4

USB 2.0 x 1
CardReader Realtek RTS5138 78
SD/MMC+/MS/ MS Pro/xD

AZALIA

Internal Analog MIC
HP1
MIC IN
2CH SPEAKER

Azalia CODEC IDT 92HD79B1 30

SPI
Flash ROM 4MB 62

LPC Bus
LPC debug port 70

SATA x 2
HDD 59
ODD 59

KBC
NUVOTON NPCE781BA0DX 37

SPI
SMBus

Flash ROM 256kB 62
Touch PAD 68
Int. KB 68
Thermal Main:G7922 Sec.EMC2102 39
Fan 58

CPU DC/DC ISL62883 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC RT8205B 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW

SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE

VGA RT8208B 89	
INPUTS	OUTPUTS
+PWR_SRC	+VGA_CORE

TI CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_RUN_VGA

SYSTEM DC/DC APL5930 90	
INPUTS	OUTPUTS
+1.5V_SUS	+1.0V_RUN_VGA

Switches	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Bottom

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Title: Block Diagram
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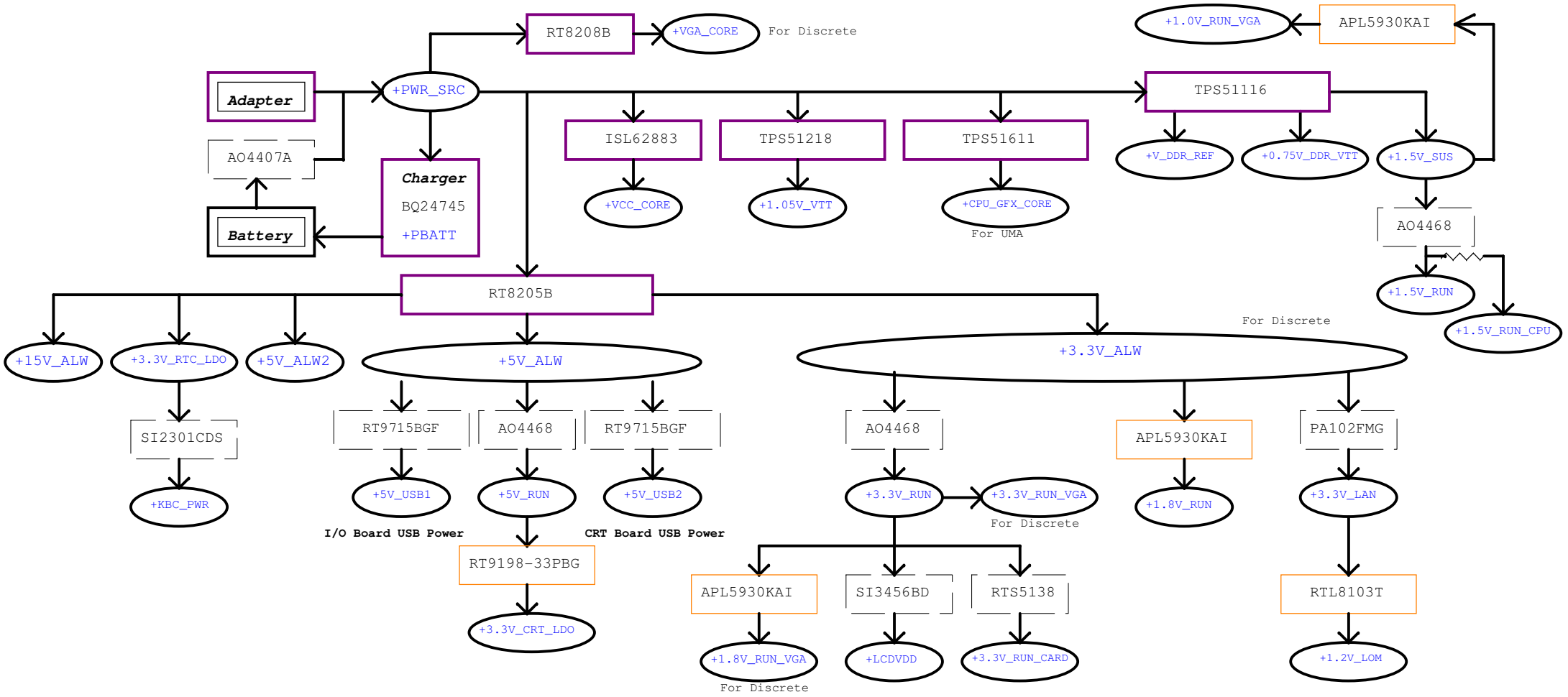

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Title: Power Block Diagram

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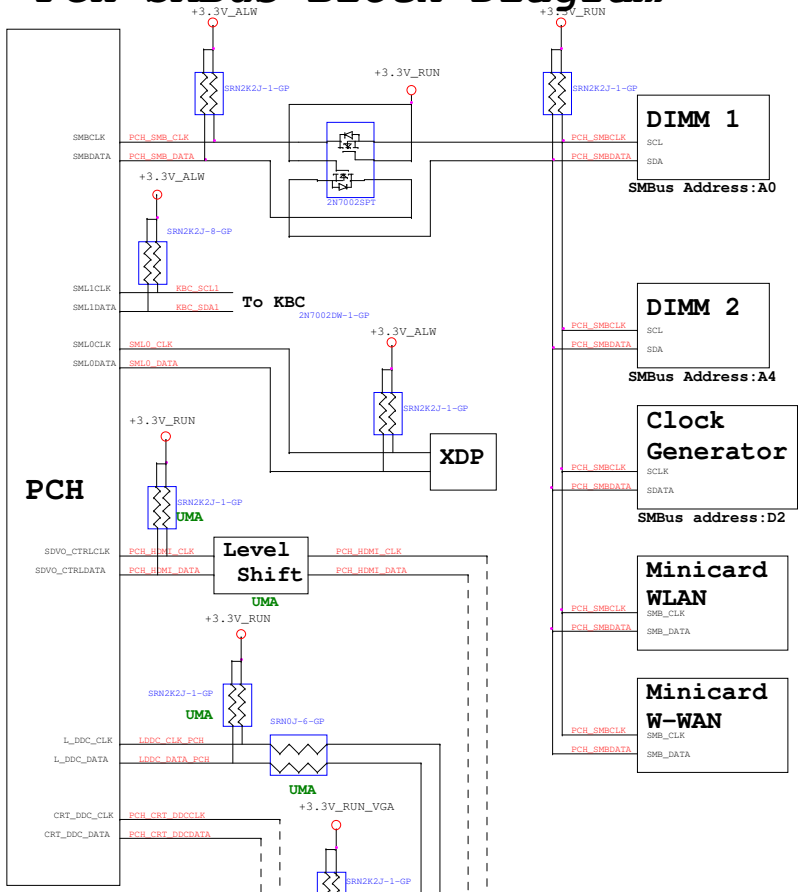
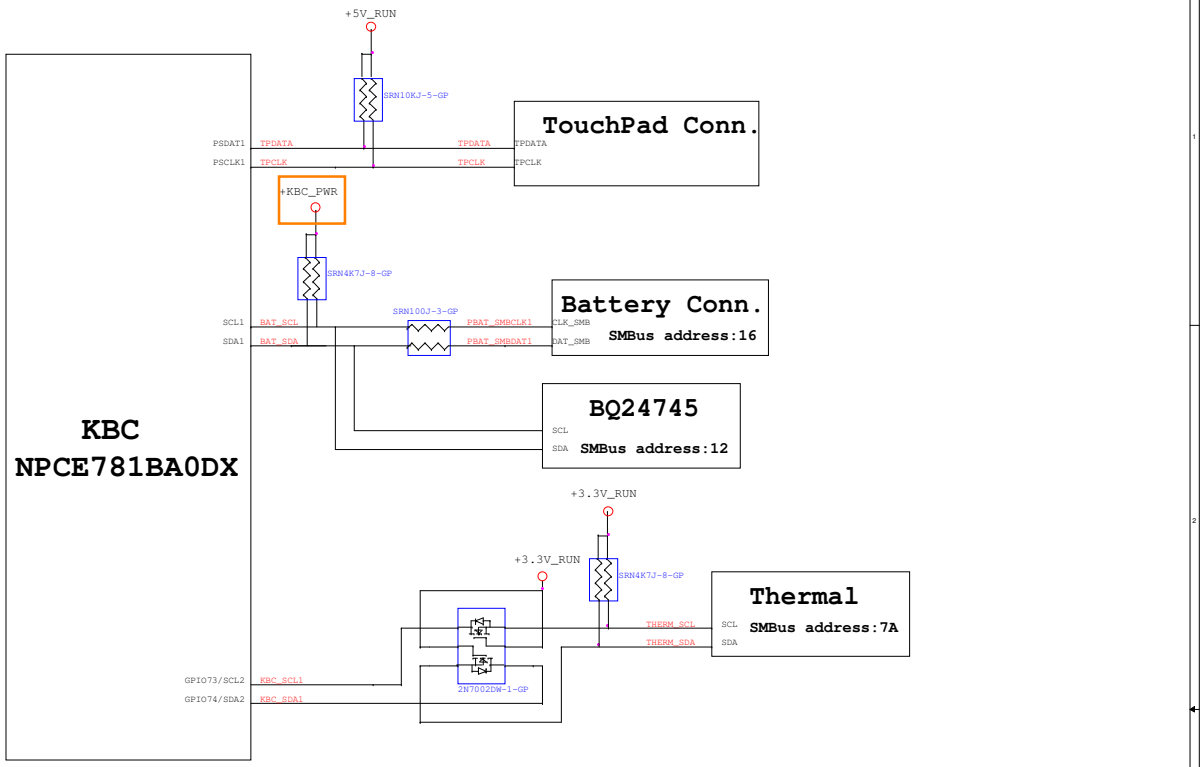
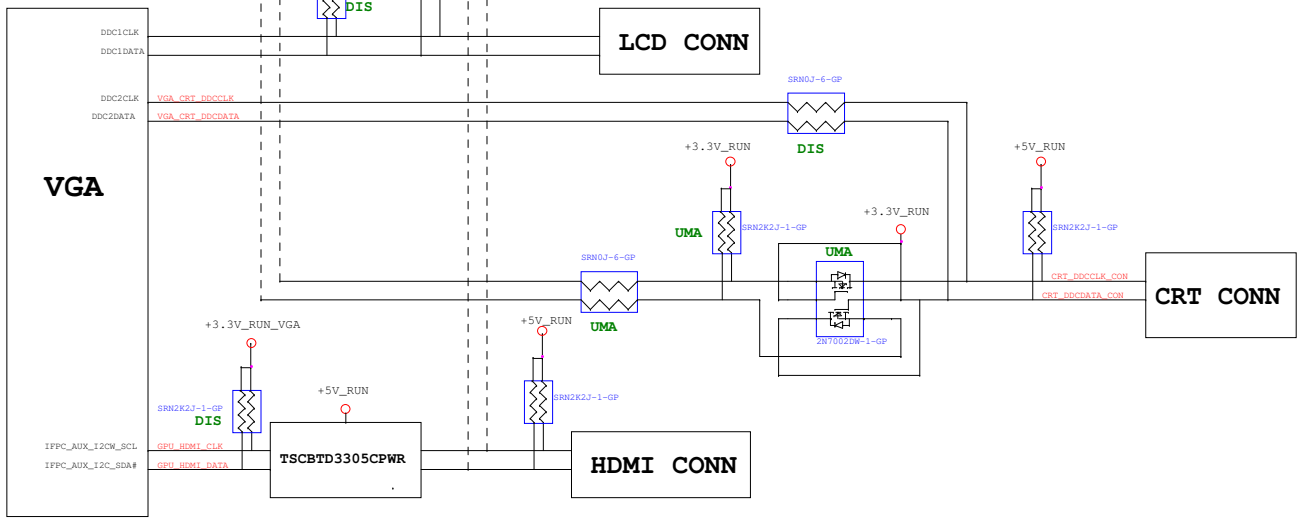
PCH SMBus Block Diagram



KBC SMBus Block Diagram





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Title: SMBUS Block Diagram

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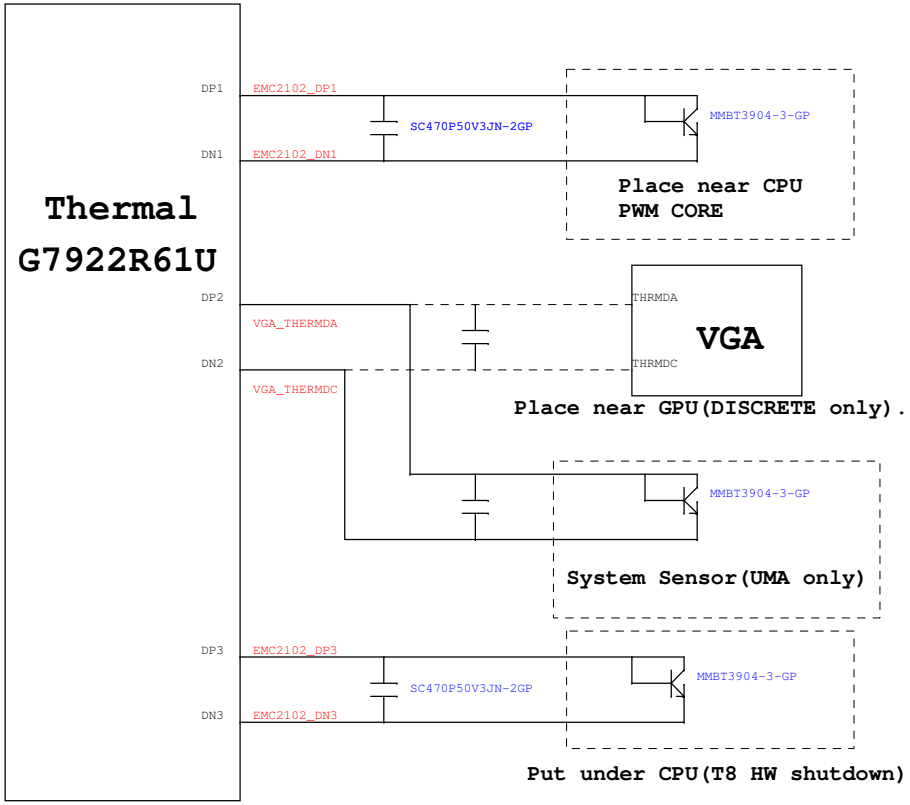
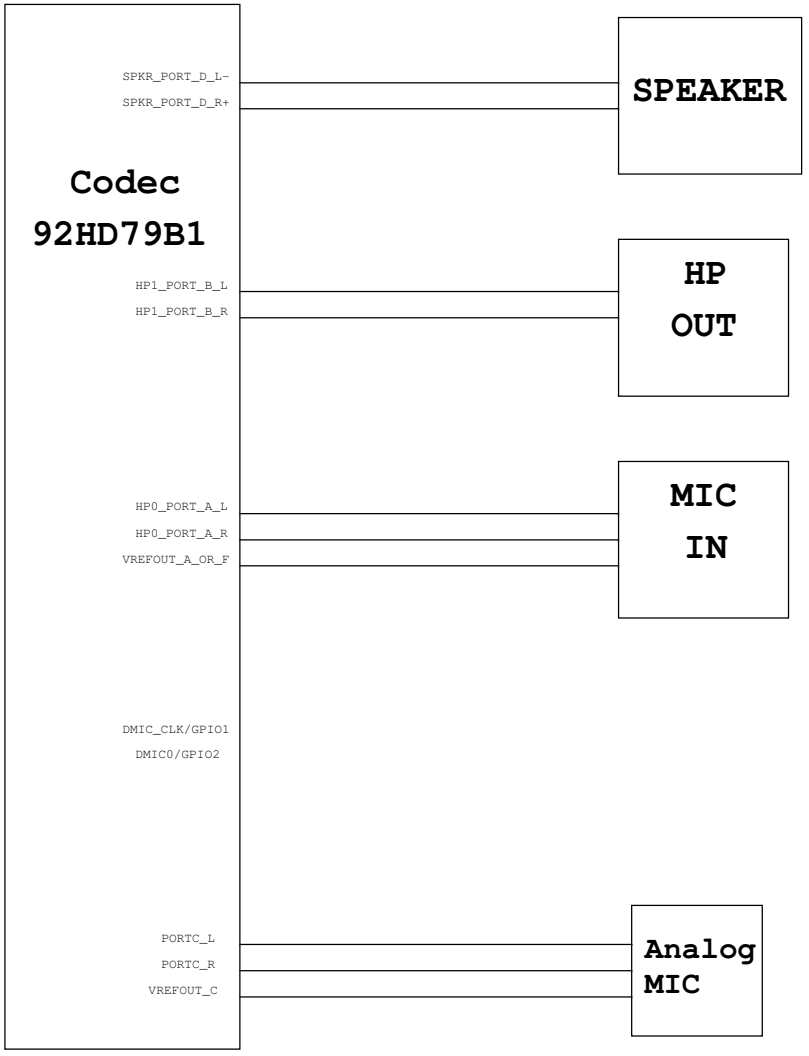
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#/GPIO51	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** – Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCIE Routing

LANE1	RESERVED
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	W-WAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	H55/HM55 no support
LANE8	H55/HM55 no support

USB Table

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	RESERVED
4	CARD READER
5	BLUETOOTH
6	HM55 no support
7	HM55 no support
8	USB1 (I/O Board)
9	USB0 (I/O Board ESATA)
10	RESERVED
11	W-WAN (I/O Board)
12	RESERVED
13	CAMERA

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	HM55 no support
3	HM55 no support
4	ESATA
5	RESERVED

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Title: Table of Content

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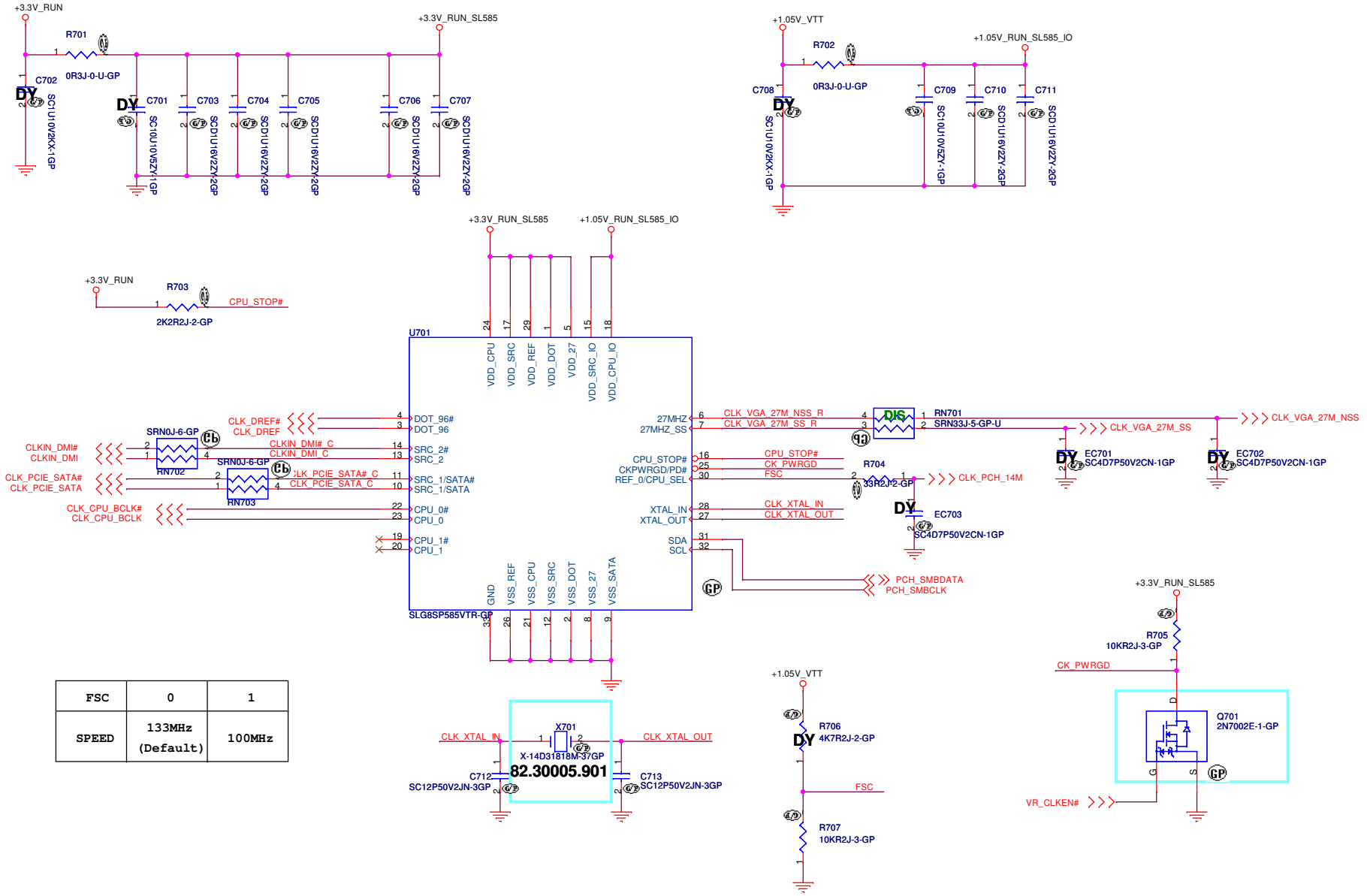
SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator SLG8SP585

Size | Document Number: Berry | Rev: X00

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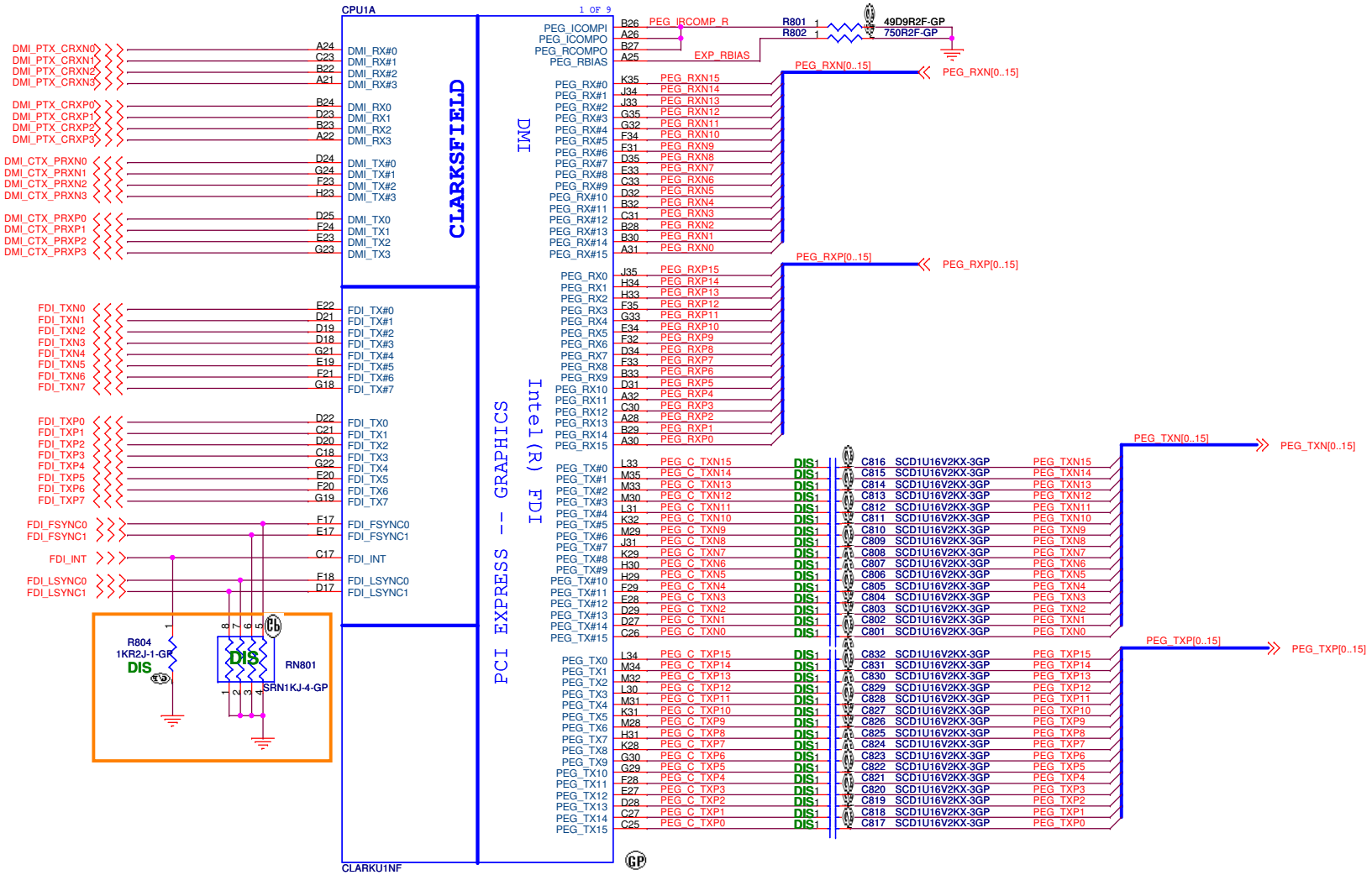
SSID = CPU



62.10055.341

SEC. 62.10053.561

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Title: **CPU (PCIE/DMI/FDI)**

Size	Document Number	Rev
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SSID = CPU

Processor Pullups

+1.05V_VTT
R901 49D9R2F-GP H_CATERR#
R907 68R2-GP H_PROCHOT#
R906 68R2-GP H_CPURST#
DY

Processor Compensation Signals

R902 20R2F-GP H_COMP3
R903 20R2F-GP H_COMP2
R904 49D9R2F-GP H_COMP1
R905 49D9R2F-GP H_COMP0
TPAD14-GP TP901 SKTOCC# R

CPU1B (CLARKSFIELD)

2 OF 9

COMP3	AT23
COMP2	AT24
COMP1	G16
COMP0	AT26
SKTOCC#	AH24
CATERR#	AK14
PECI	AT15
PROCHOT#	AN26
THERMTRIP#	AK15
RESET_OBS#	AP26
PM_SYNC	AL15
VCCPWRGOOD_1	AN14
VCCPWRGOOD_0	AN27
SM_DRAMPWROK	AK13
VTTPWRGOOD	AM15
TAPPWRGOOD	AM26
RSTIN#	AL14

MISC THERMAL SKTOCC
DDR3 MISC
JTAG & BPM
PWR MANAGEMENT

CLARKU1NF

H_PECI
H_PROCHOT#
H_THERMTRIP#
H_CPURST#
H_PM_SYNC
H_PWRGD R910 0R2J-2-GP VCCPWRGOOD
PM_DRAM_PWRGD R912 0R2J-2-GP VDDPWRGOOD_R
H_VTTPWRGD
H_PWRGD_XDP
PLT_RST# R917 1K54R2F-GP PLT_RST# R R918 750R2F-GP

BCLK	A16 BCLK_CPU_C_P
BCLK#	B16 BCLK_CPU_C_N
BCLK_ITP	AR30 BCLK_ITP_P
BCLK_ITP#	AT30 BCLK_ITP_N
PEG_CLK	E16 CLK_EXP_C_P
PEG_CLK#	D16 CLK_EXP_C_N
DPLL_REF_SSCLK	A18
DPLL_REF_SSCLK#	A17
SM_DRAMRST#	F6 SM_DRAMRST#
SM_RCOMP0	AL1 SM_RCOMP_0
SM_RCOMP1	AM1 SM_RCOMP_1
SM_RCOMP2	AN1 SM_RCOMP_2
PM_EXT_TS#0	AN15 PM_EXTTS#0_C
PM_EXT_TS#1	AP15 PM_EXTTS#1_C
PRDY#	AT28 XDP_PRDY#
PREQ#	AP27 XDP_PREQ#
TCK	AN28 XDP_TCLK
TMS	AP28 XDP_TMS
TRST#	AT27 XDP_TRST#
TDI	AT29 XDP_TDI_R
TDO	AR27 XDP_TDO_R
TDI_M	AP29 XDP_TDI_M
TDO_M	AP29 XDP_TDO_M
DBR#	AN25 H_DBR# R
BPM#0	AJ22 XDP_OBS0
BPM#1	AK22 XDP_OBS1
BPM#2	AK24 XDP_OBS2
BPM#3	AJ24 XDP_OBS3
BPM#4	AJ25 XDP_OBS4
BPM#5	AH22 XDP_OBS5
BPM#6	AK23 XDP_OBS6
BPM#7	AH23 XDP_OBS7

RN901 SRN0J-6-GP BCLK_CPU_P BCLK_CPU_N
RN902 SRN0J-6-GP CLK_EXP_P CLK_EXP_N
RN903 SRN10KJ-5-GP
RN904 SRN0J-6-GP PM_EXTTS#0 PM_EXTTS#1

Q901 BSS138-7F-GP
S3_RST_GATE# +1.5V_SUS R908 1KR2J-1-GP DDR3_DRAMRST# R909 0R2J-2-GP

DDR3 Compensation Signals

SM_RCOMP_0 R913 100R2F-L1-GP-U
SM_RCOMP_1 R914 24D9R2F-L-GP
SM_RCOMP_2 R916 130R2F-1-GP

R911 0R2J-2-GP XDP_DBRESET#

+1.5V_RUN_CPU R915 1KR2J-1-GP DY
SM_DRAMRST# R921 100KR2J-1-GP DY

+1.05V_VTT
XDP_TMS R919 51R2J-2-GP DY
XDP_TDI_R R920 51R2J-2-GP DY
XDP_PREQ# R922 51R2J-2-GP DY
XDP_TCLK R923 51R2J-2-GP DY

For EMI

XDP_RST# R
VCCPWRGOOD
VDDPWRGOOD_R
H_VTTPWRGD
PLT_RST# R
XDP_DBRESET#
EC906 EC905 EC904 EC903 EC902 EC901 DY
SCD1U16V2KX-3GP

For S3 Reduction

+3.3V_RUN
U901 NL17SZ08DFT2G-GP
1.5CPU_1.05VTT_PWRGD
VTT_PWRGD_C
R927 1K54R2F-GP DY
VDDPWRGOOD_R
R930 750R2F-GP DY

+1.5V_SUS +1.5V_RUN_CPU
R924 1K1R2F-GP DY R925 1K1R2F-GP
VDDPWRGOOD_R
R926 3KR2F-GP

+1.05V_VTT
H_PWRGD R935 1KR2J-1-GP DY
PM_PWRBTN#_R R937 0R2J-2-GP DY
H_PWRGD_XDP R938 0R2J-2-GP DY
C902 SCD1U16V2KX-3GP DY
SML0_DATA SML0_CLK
H_CPUPWRGD_XDP PM_PWRBTN#_XDP PCIE_CLK_XDP_P

XDP1 STC-CONN60A-GP-U1 DY

XDP_PREQ# XDP_PRDY#
XDP_OBS0 XDP_OBS1
XDP_OBS2 XDP_OBS3
XDP_OBS4 XDP_OBS5
XDP_OBS6 XDP_OBS7
XDP_TCLK

BCLK_ITP_P BCLK_ITP_N
XDP_RST# R R939 1KR2J-1-GP DY
H_CPURST# XDP_DBRESET# XDP_TDO XDP_TRST# XDP_TDI XDP_TMS

+1.05V_VTT
C901 SCD1U16V2KX-3GP DY
R936 51R2J-2-GP
XDP_RST# R R940 0R2J-2-GP DY PLT_RST#

XDP_TDI_R R928 0R2J-2-GP XDP_TDI
XDP_TDO_M R929 0R2J-2-GP XDP_TDO
R931 0R2J-2-GP
XDP_TDI_M R933 0R2J-2-GP
XDP_TDO_R R934 0R2J-2-GP
XDP_TRST# R932 51R2J-2-GP

JTAG MAPPING

Scan Chain (Default)	Stuff --> R928, R931, R934 No Stuff --> R929, R933
CPU Only	Stuff --> R928, R929 No Stuff --> R931, R934, R933
GMCH Only	Stuff --> R933, R934 No Stuff --> R928, R929, R931

<Core Design>

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Title: CPU (THERMAL/CLOCK/PM)
Size | Document Number: Berry | Rev: X00
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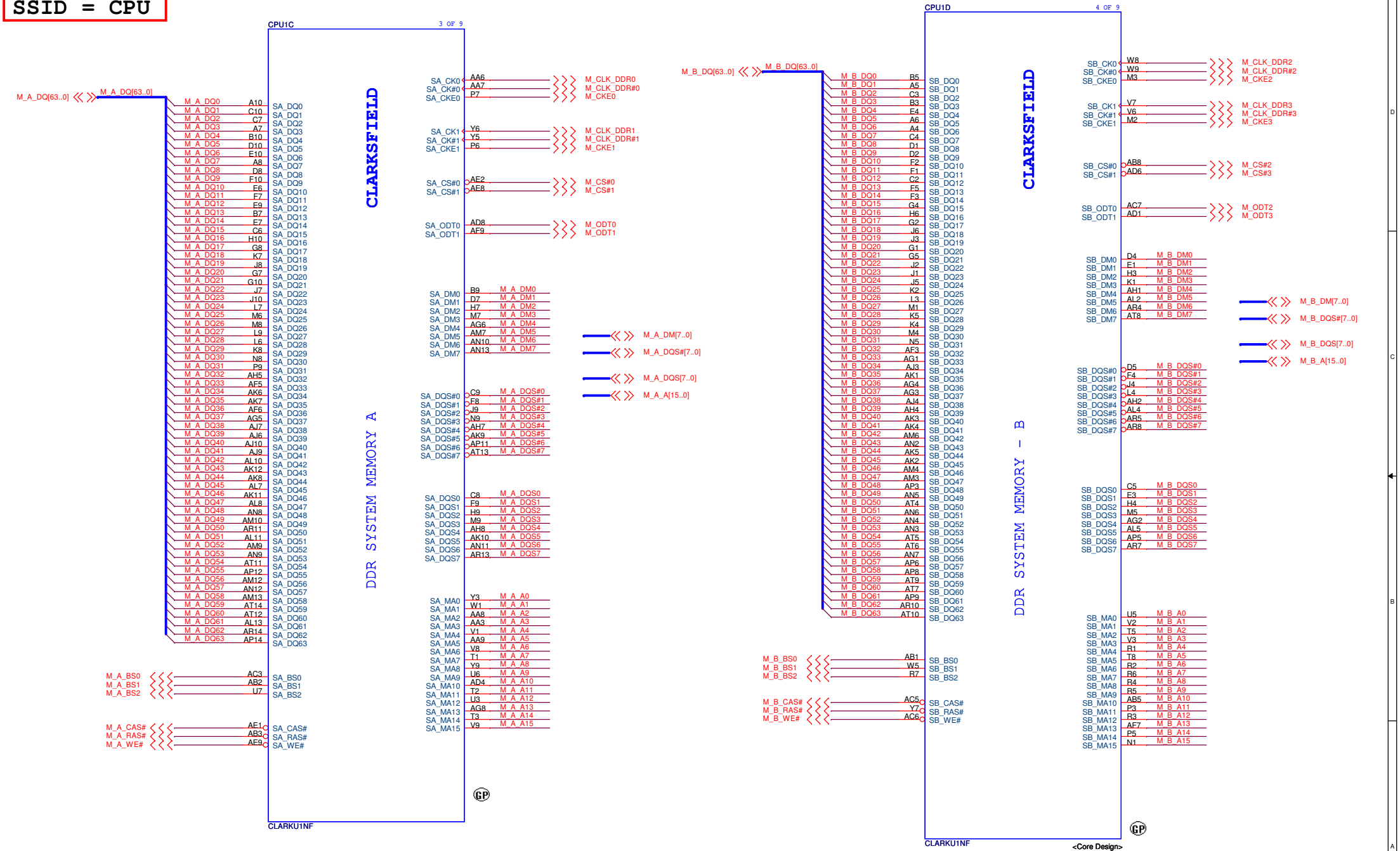
SSID = CPU



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Title	CPU (DDR)	
Size	Document Number: Berry	Rev: X00
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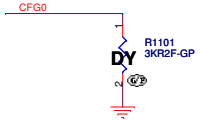
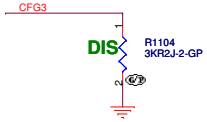
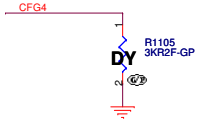
SSID = CPU



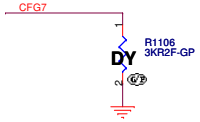
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



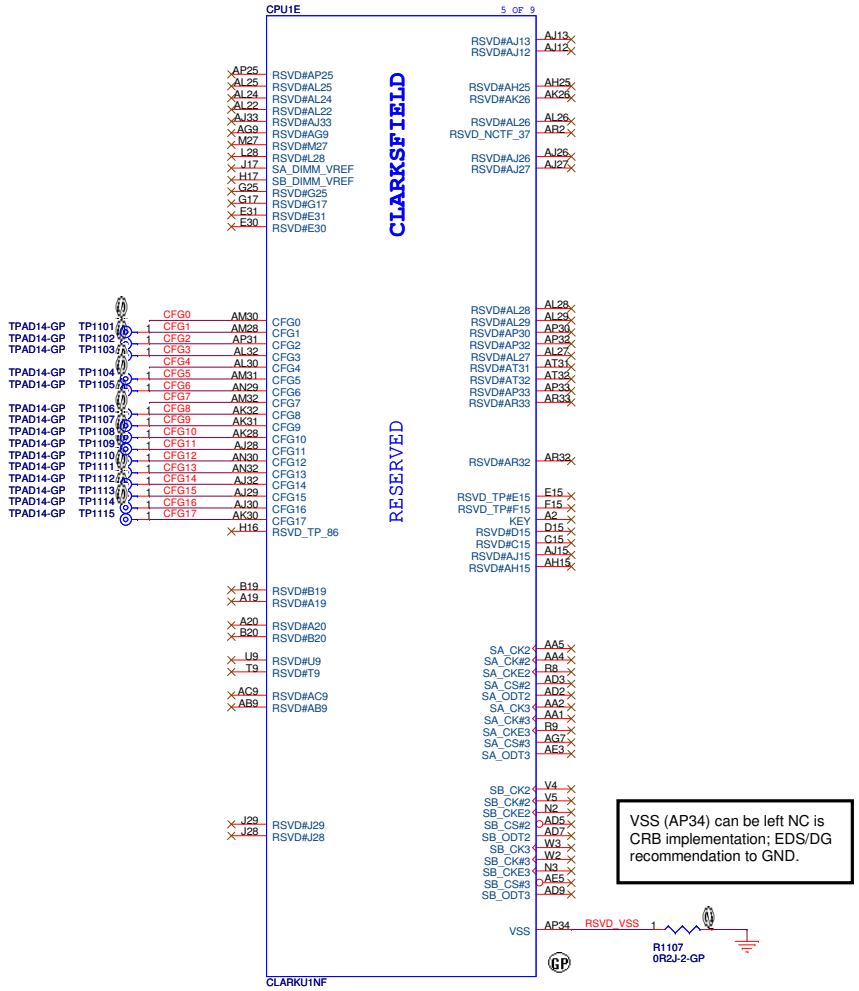
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

<Core Design>

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Title		
	CPU (RESERVED)	
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SSID = CPU

PROCESSOR CORE POWER

48A

+VCC_CORE

CPU1F

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CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

CLARKU1NF

+1.05V_VTT

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

<Core Design>

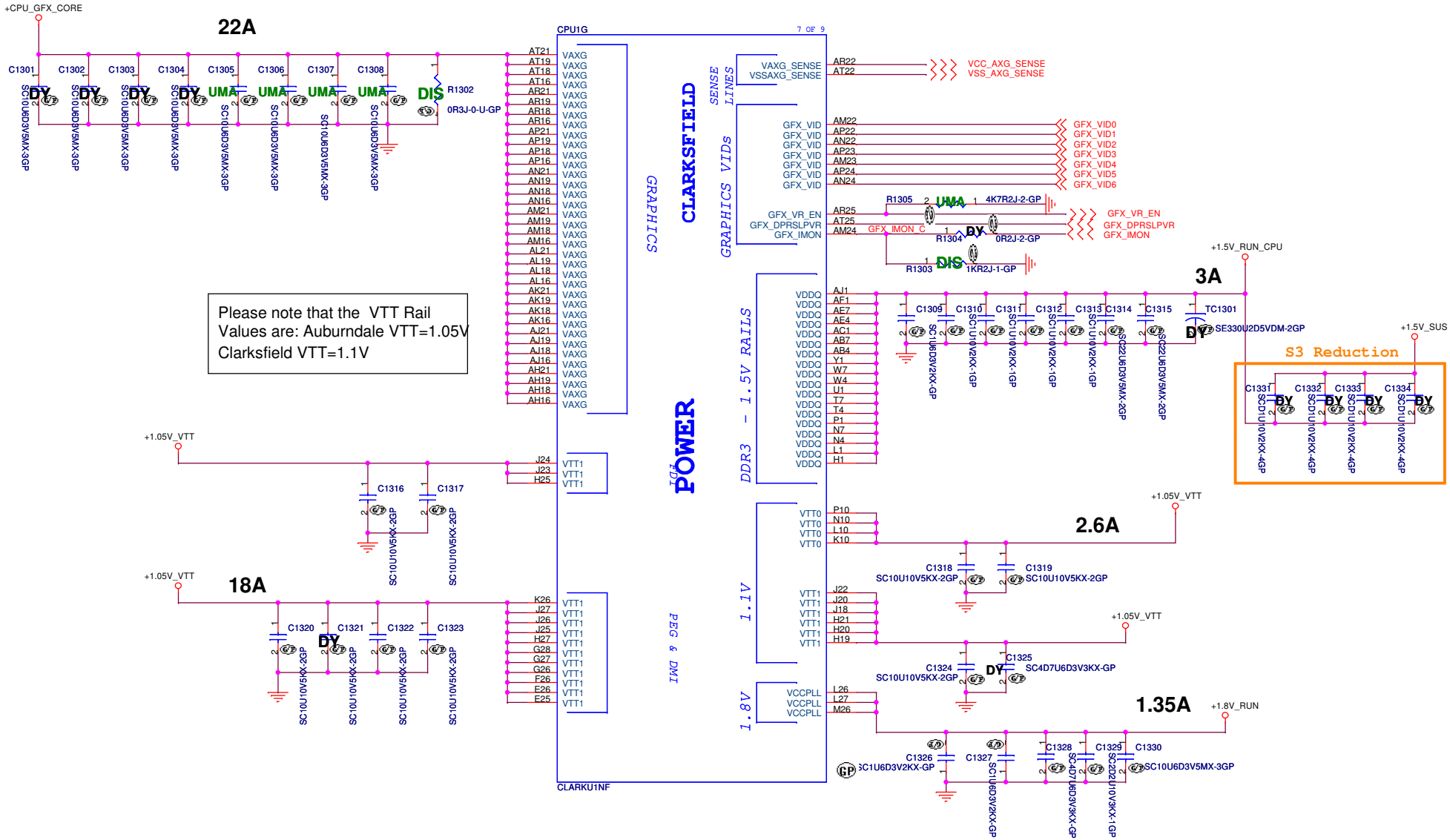
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size | Document Number: Berry | Rev: X00

Date: Thursday, October 22, 2009 | Sheet 12 of 92

SSID = CPU

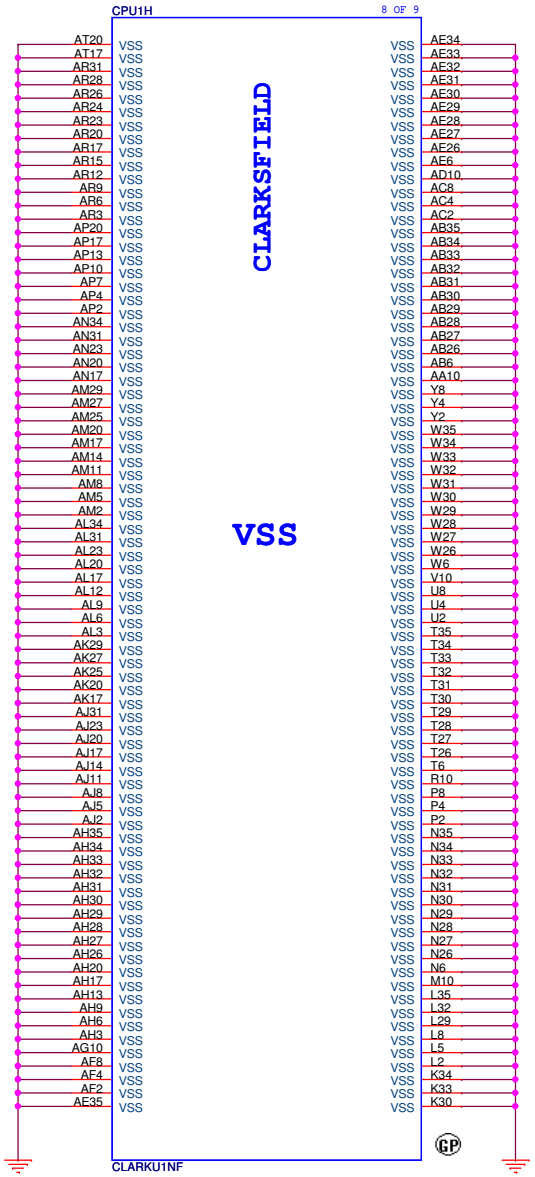


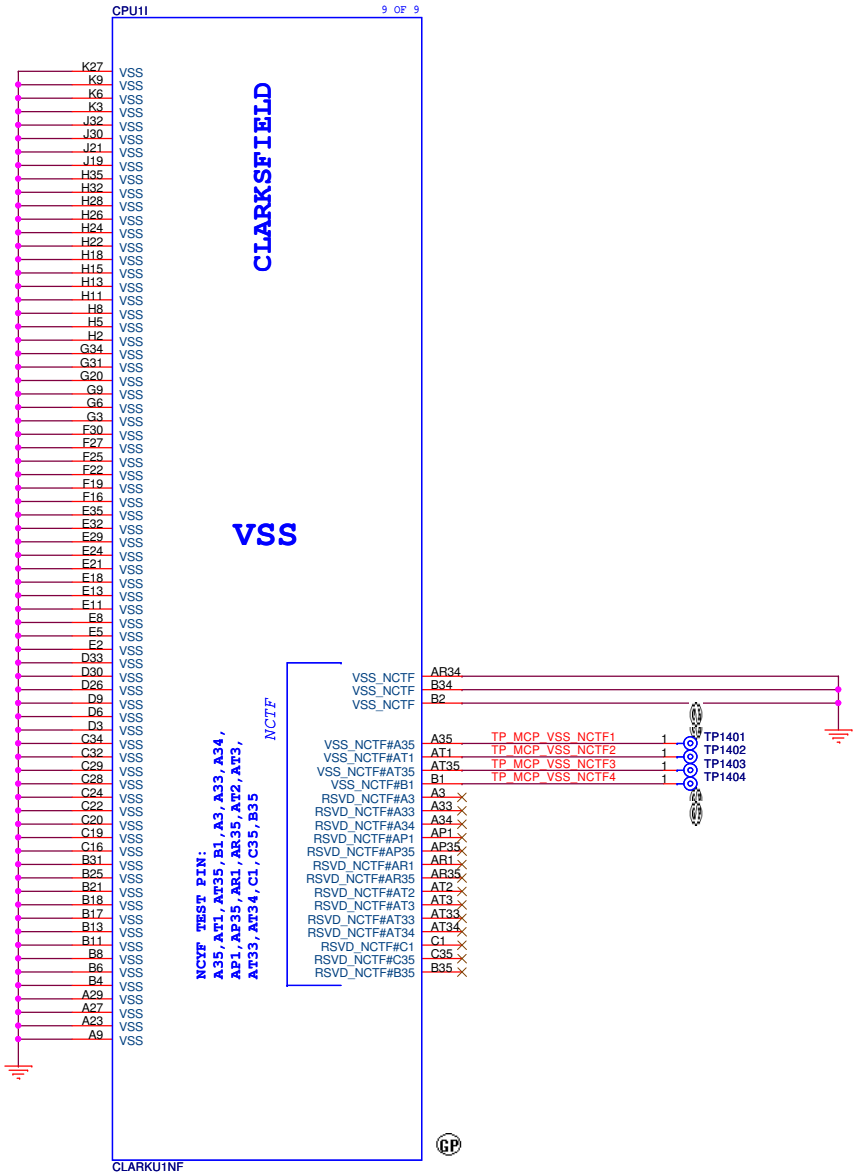
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU (VCC_GFXCORE)		
Size	Document Number: Berry	Rev: X00
Date: Thursday, October 22, 2009	Sheet 13 of 92	

SSID = CPU





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VSS)	
Size	Document Number: Berry	Rev: X00
Date: Wednesday, October 14, 2009	Sheet 14 of 92	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*X00*

Date: Wednesday, October 14, 2009 Sheet 15 of 92

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*X00*

Date: Wednesday, October 14, 2009 Sheet 16 of 92

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*X00*

Date: Wednesday, October 14, 2009 Sheet 17 of 92

SSID = MEMORY

DM1

DDR3-204P-47-GP

H =4mm

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMA.

Place these caps close to VTT1 and VTT2.

2 S3 Power Reduction

84.2N702.D31

62.10017.P31

SEC. 62.10017.P11

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size | Document Number: Berry | Rev: X00

Date: Thursday, October 22, 2009 | Sheet 18 of 92

SSID = MEMORY

DM2

DDR3-204P-55-GP

H = 8mm

62.10017.Q31

SEC. 62.10017.N71

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM B DECOUPLING

Layout Note:
Place these Caps near
SO-DIMMB.

Place these caps
close to VTT1 and
VTT2.

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from
the Processor than SO-DIMMA

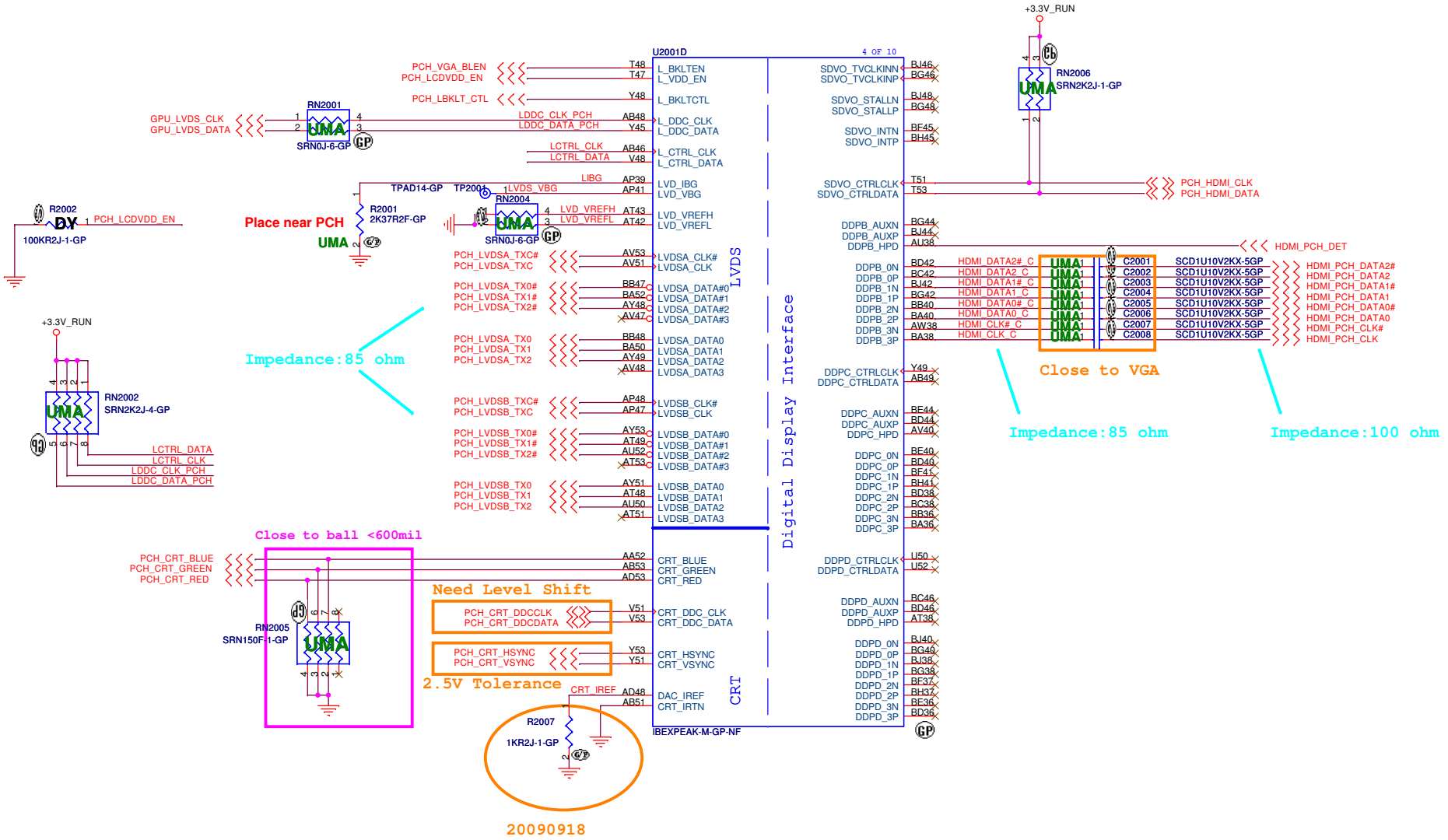
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size | Document Number: Berry | Rev: X00

Date: Thursday, October 22, 2009 | Sheet 19 of 92



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
	Berry	X00

Date: Thursday, October 22, 2009 Sheet 20 of 92

SSID = PCH

RN2101 SRN8K2J-2-GP-U
PCI_TRDY# 1 — PCI_FRAME# 10 +3.3V_RUN
PCI_DEVSEL# 2 — PCI_REQ2# 9
INT_PIRQA# 3 — INT_PIRQD# 8
PCI_IRDY# 4 — PCI_SERR# 7
+3.3V_RUN 5 — 6

RN2103 SRN8K2J-2-GP-U
INT_PIRQH# 1 — PCI_REQ1# 10 +3.3V_RUN
INT_PIRQB# 2 — PCI_PLOCK# 9
INT_PIRQF# 3 — PCI_PERR# 8
PCI_REQ3# 4 — PCI_REQ0# 7
+3.3V_RUN 5 — 6

RN2102 SRN8K2J-4-GP
+3.3V_RUN 1 — PCI_STOP# 8
2 — INT_PIRQE# 7
3 — INT_PIRQC# 6
4 — INT_PIRQG# 5

BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

RN2104 SRN8K2J-2-GP-U
USB_OC#2_3 1 — USB_OC#12_13 10 +3.3V_ALW
SMC_WAKE_SCI#_R 2 — USB_OC#8_9 9
USB_OC#6_7 3 — USB_OC#10_11 8
USB_OC#0_1 4 — USB_OC#4_5 7
+3.3V_ALW 5 — 6

R2105 4K7R2J-2-GP
PCI_GNT3# — 1 — DY

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

+3.3V_RUN — U2101 NL17SZ08DFT2G-GP (VCC, Y, A, GND, DY) — PCI_PLTRST#
PLT_RST# — R2101 0R2J-2-GP — C2101 SC220P50V2KX-3GP

PCLK_FWH — R2107 22R2J-2-GP — PCLK_FWH_R
CLK_PCI_FB — R2108 22R2J-2-GP — CLK_PCI_FB_R
PCLK_KBC — R2109 22R2J-2-GP — PCLK_KBC_R
EC2101 SC4D7P50V2CN-1GP

KBC CLK EMI

U2001E IBEXPEAK-M-GP-NF (5 OF 10)

PCI:
AD0 H40, AD1 N34, AD2 C44, AD3 A38, AD4 C36, AD5 J34, AD6 A40, AD7 D45, AD8 E36, AD9 H48, AD10 E40, AD11 C40, AD12 M48, AD13 M45, AD14 F53, AD15 M40, AD16 M43, AD17 J36, AD18 K48, AD19 F40, AD20 C42, AD21 K46, AD22 M51, AD23 J52, AD24 K51, AD25 L34, AD26 F42, AD27 J40, AD28 G46, AD29 F44, AD30 M47, AD31 H36
C/BE0# J50, C/BE1# G42, C/BE2# H47, C/BE3# G34
PIRQA# G38, PIRQB# H51, PIRQC# B37, PIRQD# A44
REQ0# F51, REQ1#/GPIO50 A46, REQ2#/GPIO52 B45, REQ3#/GPIO54 M53
GNT0# F48, GNT1#/GPIO51 K45, GNT2#/GPIO53 F36, GNT3#/GPIO55 H53
PIRQE#/GPIO2 B41, PIRQF#/GPIO3 K53, PIRQG#/GPIO4 A36, PIRQH#/GPIO5 A48
PCIRST# K6
SERR# E44, PERR# E50
IRDY# A42, PAR H44, DEVSEL# F46, FRAME# C46
PLOCK# D49
STOP# D41, TRDY# C48
PME# M7
PLTRST# D5
CLKOUT_PCI0 N52, CLKOUT_PCI1 P53, CLKOUT_PCI2 P46, CLKOUT_PCI3 P51, CLKOUT_PCI4 P48

NVRAM:
NV_CE#0 AY9, NV_CE#1 BD1, NV_CE#2 AP15, NV_CE#3 BD8
NV_DQS0 AV9, NV_DQS1 BG8
NV_DQ0/NV_IO0 AP7, NV_DQ1/NV_IO1 AP6, NV_DQ2/NV_IO2 AT6, NV_DQ3/NV_IO3 AT9, NV_DQ4/NV_IO4 BB1, NV_DQ5/NV_IO5 AV6, NV_DQ6/NV_IO6 BB3, NV_DQ7/NV_IO7 BA4, NV_DQ8/NV_IO8 BE4, NV_DQ9/NV_IO9 BB6, NV_DQ10/NV_IO10 BD6, NV_DQ11/NV_IO11 BB7, NV_DQ12/NV_IO12 BC8, NV_DQ13/NV_IO13 BJ8, NV_DQ14/NV_IO14 BJ6, NV_DQ15/NV_IO15 BG6
NV_ALE BD3, NV_CLE AY6
NV_RCOMP AU2
NV_RB# AV7
NV_WR#0_RE# AY8, NV_WR#1_RE# AY5
NV_WE#_CK0 AV11, NV_WE#_CK1 BF5

USB:
USBP0N H18, USBP0P J18, USBP1N A18, USBP1P C18, USBP2N N20, USBP2P P20, USBP3N J20, USBP3P L20, USBP4N F20, USBP4P G20, USBP5N A20, USBP5P C20, USBP6N M22, USBP6P N22, USBP7N B21, USBP7P D21, USBP8N H22, USBP8P J22, USBP9N F22, USBP9P F22, USBP10N A22, USBP10P C22, USBP11N G24, USBP11P H24, USBP12N L24, USBP12P M24, USBP13N A24, USBP13P C24
USBRBIAS# B25, USBRBIAS D25
OC0#/GPIO59 N16, OC1#/GPIO40 J16, OC2#/GPIO41 F16, OC3#/GPIO42 L16, OC4#/GPIO43 E14, OC5#/GPIO9 G16, OC6#/GPIO10 F12, OC7#/GPIO14 T15

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

+V_NVRAM_VCCQ — R2102 KR2J-1-GP — NV_CLE
+V_NVRAM_VCCQ — R2103 KR2J-1-GP — NV_ALE

Danbury Technology:
Disabled when Low.
Enable when High.

NV_ALE — NV_CLE — NV_RCOMP — TP2105 TPAD14-GP

USBP0N — USB_PN0, USBP0P — USB_PP0, USBP1N — USB_PN1, USBP1P — USB_PP1, USBP2N — USB_PN2, USBP2P — USB_PP2
USBP4N — USB_PN4, USBP4P — USB_PP4, USBP5N — USB_PN5, USBP5P — USB_PP5
USBP8N — USB_PN8, USBP8P — USB_PP8, USBP9N — USB_PN9, USBP9P — USB_PP9
USBP11N — USB_PN11, USBP11P — USB_PP11
USBP13N — USB_PN13, USBP13P — USB_PP13

USB_RBIAS_PN — R2106 22D6R2F-L1-GP

OC0#/GPIO59 — USB_OC#0_1 — USB_OC#0_1
OC1#/GPIO40 — USB_OC#2_3
OC2#/GPIO41 — USB_OC#4_5
OC3#/GPIO42 — USB_OC#6_7
OC4#/GPIO43 — USB_OC#8_9 — USB_OC#8_9
OC5#/GPIO9 — USB_OC#10_11
OC6#/GPIO10 — USB_OC#12_13
OC7#/GPIO14 — SMC_WAKE_SCI#_R

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	X
4	CARD READER
5	BLUETOOTH
6	X
7	X
8	USB1 (I/O Board)
9	ESATA (I/O Board COMBO)
10	X
11	W-WAN (I/O Board)
12	X
13	CAMERA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: Document Number: Berry — Rev: X00
Date: Thursday, October 22, 2009 — Sheet 21 of 92

SSID = PCH

U2001C

3 OF 10

DMI

FDI

System Power Management

iBEXPEAK-M-GP-NF

depend on Layout

Option to " Disable " clkrun.
Pulling it down will keep the clks running.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)

Size | Document Number: Berry | Rev: X00

Date: Thursday, October 22, 2009 | Sheet 22 of 92

SSID = PCH

U2001B — 2 OF 10 — IBEXPEAK-M-GP-NF

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

WLAN
LAN
W-WAN

PCI-E*
SMBus
PEG
From CLK BUFFER
Clock Flex

DIS uses 0ohm 63.R0034.1DL
UMA uses 18pF 78.18034.1FL

For EMI

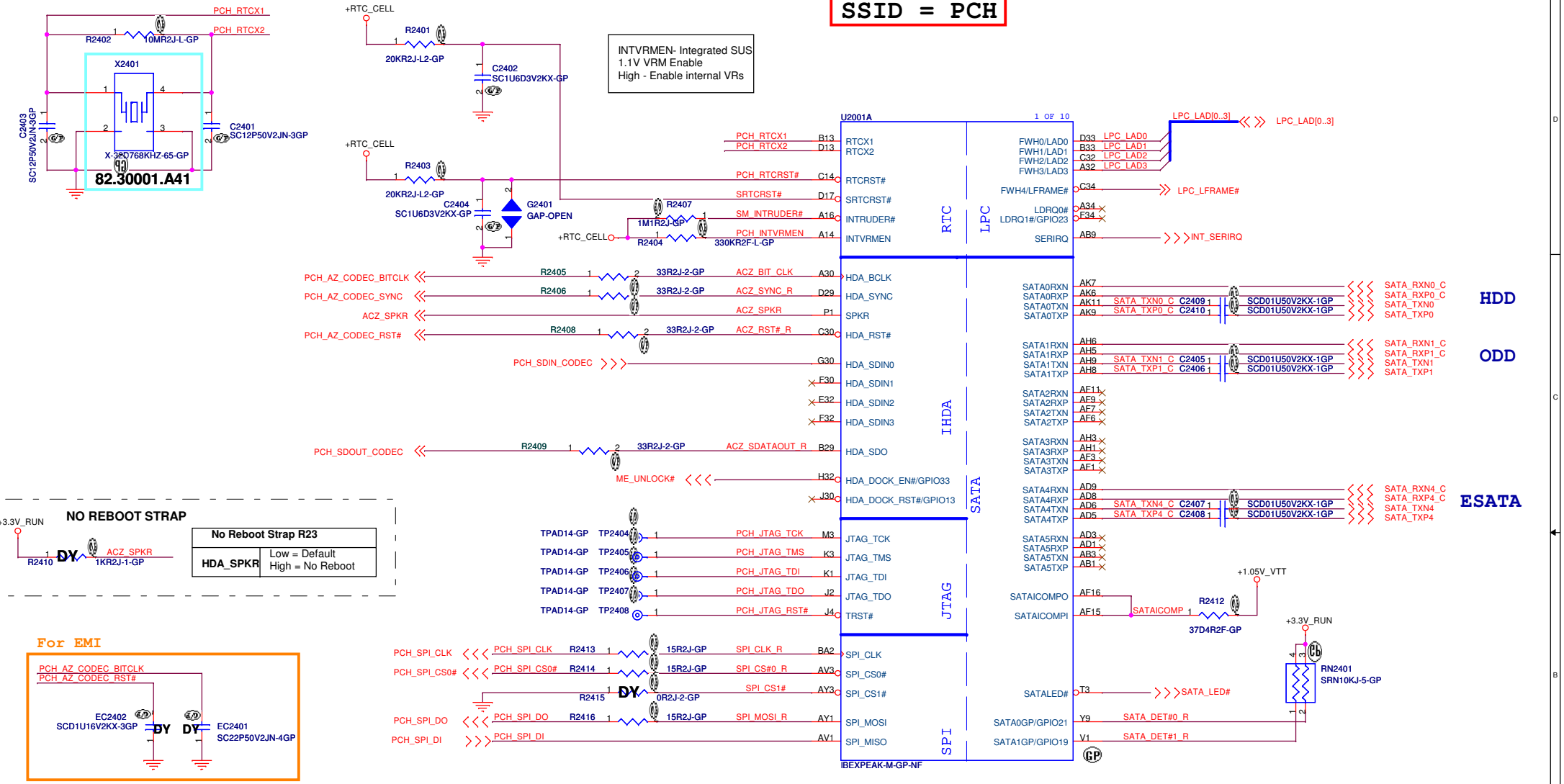
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)
Size:
Document Number: Berry
Rev: X00
Date: Thursday, October 22, 2009
Sheet 23 of 92

SSID = PCH

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs



NO REBOOT STRAP

+3.3V_RUN — R2410 DY 1KR2J-1-GP — ACZ_SPKR

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

For EMI

PCH_AZ_CODEC_BITCLK
PCH_AZ_CODEC_RST#
EC2402 SCD1U16V2KX-3GP DY
EC2401 SC22P50V2JN-4GP DY

<Core Design>

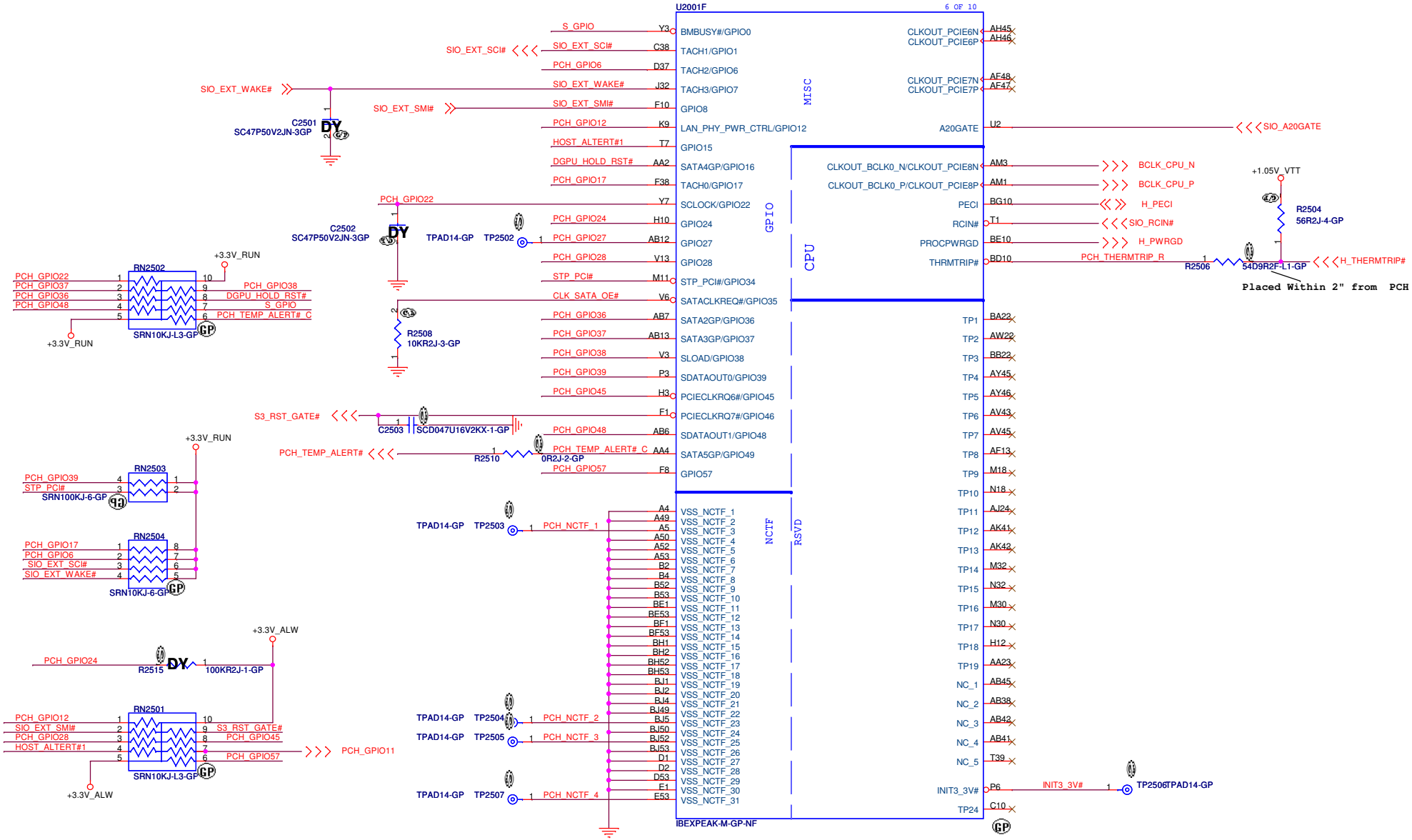
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
	Berry	X00

Date: Thursday, October 22, 2009 Sheet 24 of 92

SSID = PCH

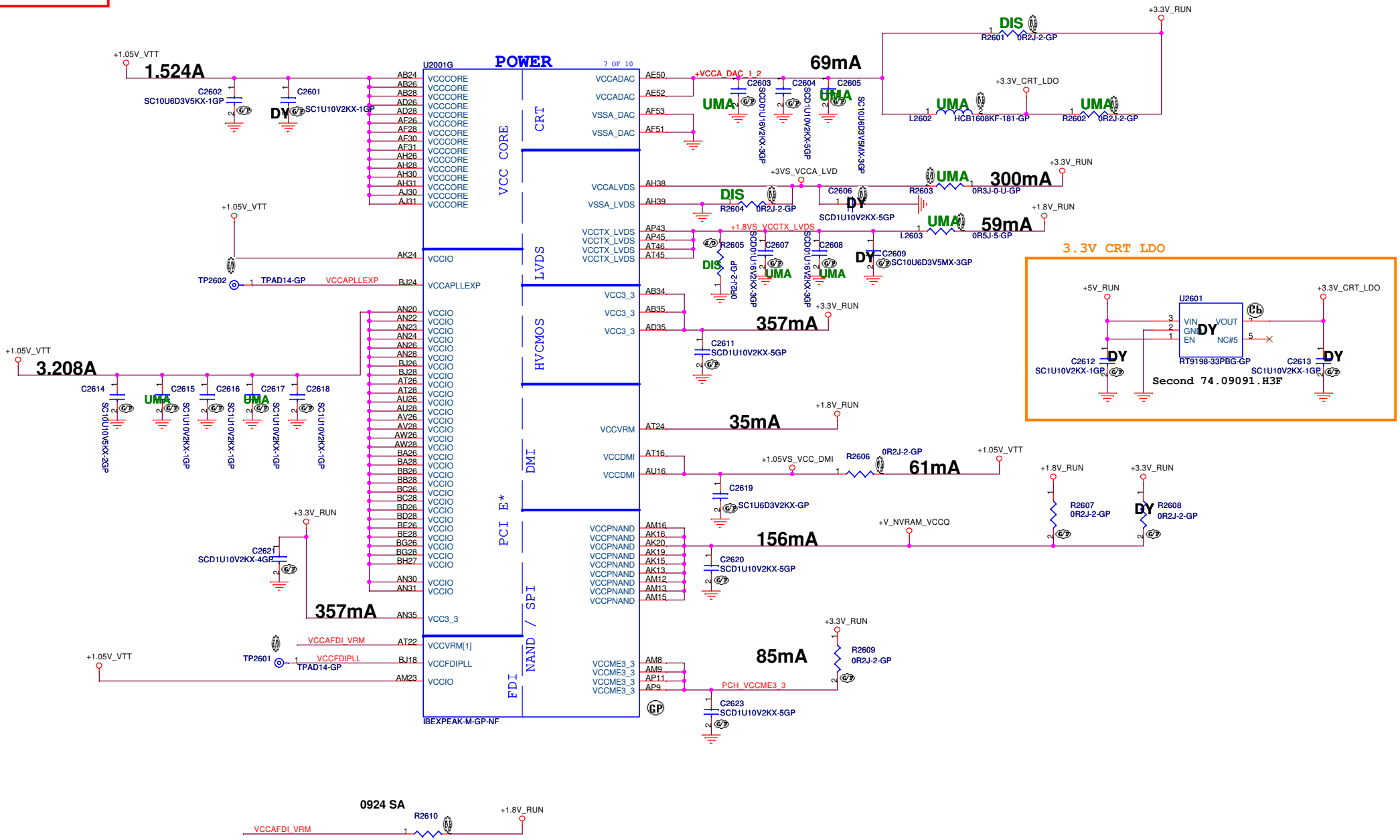


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (GPIO/CPU)	
Size	Document Number: Berry	Rev: X00
Date: Thursday, October 22, 2009	Sheet 25 of 92	

SSID = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size | Document Number: Berry | Rev: X00

Date: Thursday, October 22, 2009 | Sheet 26 of 92

SSID = PCH

U2001J POWER 10 OF 10

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | CPU | RTC | HDA

TP2701 VCCACLK TPAD14-GP

AP51 VCCACLK
AP53 VCCACLK

AF23 VCCLAN
AF24 VCCLAN

DCPSUSBYP Y20 DCPSUSBYP
C2703 SCD1U10V2KX-4GP

AD38 VCCME
AD39 VCCME
AD41 VCCME
AF43 VCCME
AF41 VCCME
AF42 VCCME
V39 VCCME
V41 VCCME
V42 VCCME
Y39 VCCME
Y41 VCCME
Y42 VCCME

+1.05V_VTT
1.998A
C2707 SC10U10V5KX-2GP
C2704 DY SC10U6D3V5MX-3GP
C2708 SC1U10V2KX-1GP
C2710 SC1U10V2KX-1GP DY

+1.05V_VTT
L2702 IND-10UH-218-GP
+1.05VS_VCCA_A_DPL
C2711 DY SC10U6D3V5MX-3GP
C2712 SC1U10V2KX-1GP

L2703 IND-10UH-218-GP
+1.05VS_VCCA_B_DPL
C2716 DY SC10U6D3V5MX-3GP
C2717 SC1U10V2KX-1GP

+VCCRTCEXT V9 DCPRTC
C2714 SCD1U10V2KX-4GP
+1.8V_RUN
AU24 VCCVRM

72mA +1.05VS_VCCA_A_DPL
BB51 VCCADPLLA
BB53 VCCADPLLA

73mA +1.05VS_VCCA_B_DPL
BD51 VCCADPLLB
BD53 VCCADPLLB

+1.05V_VTT
AH23 VCCIO
AJ35 VCCIO
AH35 VCCIO
C2720 SC1U10V2KX-1GP
C2721 SC1U10V2KX-1GP
C2722 SC1U10V2KX-1GP
AF34 VCCIO
AH34 VCCIO
AF32 VCCIO

V12 DCPSST
+VCCSST
C2725 SCD1U10V2KX-4GP

+1.05VALW_INT_VCCSUS Y22 DCPSUS
C2726 SCD1U10V2KX-4GP

+3.3V_ALW
163mA
P18 VCCSUS3_3
U19 VCCSUS3_3
U20 VCCSUS3_3
U22 VCCSUS3_3
C2728 SCD1U10V2KX-4GP

+3.3V_RUN
V15 VCC3_3
V16 VCC3_3
Y16 VCC3_3
C2729 SCD1U10V2KX-4GP

+1.05V_VTT
1mA
AT18 V_CPU_IO
AU18 V_CPU_IO
C2730 SC10U6D3V5KX-1GP
C2731 SCD1U16V2KX-3GP
C2732 SCD1U16V2KX-3GP

+RTC_CELL
2mA
A12 VCCRTC
C2734 SCD1U10V2KX-4GP
C2735 SCD1U10V2KX-4GP

IBEXPEAK-M-GP-NF

VCCIO V24
VCCIO V26
VCCIO Y24
VCCIO Y26
+1.05V_VTT
C2705 DY SC1U10V2KX-1GP

VCCSUS3_3 V28
VCCSUS3_3 U28
VCCSUS3_3 U26
VCCSUS3_3 U24
VCCSUS3_3 P28
VCCSUS3_3 P26
VCCSUS3_3 N28
VCCSUS3_3 N26
VCCSUS3_3 M28
VCCSUS3_3 M26
VCCSUS3_3 L28
VCCSUS3_3 L26
VCCSUS3_3 J28
VCCSUS3_3 J26
VCCSUS3_3 H28
VCCSUS3_3 H26
VCCSUS3_3 G28
VCCSUS3_3 G26
VCCSUS3_3 F28
VCCSUS3_3 F26
VCCSUS3_3 E28
VCCSUS3_3 E26
VCCSUS3_3 C28
VCCSUS3_3 C26
VCCSUS3_3 B27
VCCSUS3_3 A28
VCCSUS3_3 A26
+3.3V_ALW
C2706 SCD1U10V2KX-4GP

VCCSUS3_3 U23
+3.3V_ALW
C2709 SCD1U10V2KX-4GP

VCCIO V23
+1.05V_VTT

V5REF_SUS F24 +5VALW_PCH_VCC5REFSUS
+3.3V_ALW
D2701 CH751H-40PT-GP
R2702 10R2J-2-GP
+5V_ALW

change 1uF
C2713 SC1U10V2KX-1GP
DG update 1.62

V5REF K49 +5VS_PCH_VCC5REF
D2702 CH751H-40PT-GP
+3.3V_RUN
R2701 10R2J-2-GP
+5V_RUN
C2715 SC1U10V2KX-1GP

VCC3_3 J38
VCC3_3 L38
VCC3_3 M36
VCC3_3 N36
VCC3_3 P36
VCC3_3 U35
+3.3V_RUN
C2718 SCD1U10V2KX-4GP

VCC3_3 AD13
C2719 SCD1U10V2KX-4GP
+3.3V_RUN

VCCSATAPLL AK3
VCCSATAPLL AK1
VCCSATAPLL TPAD14-GP TP2702

VCCIO AH22
+1.05V_VTT
C2727 SC1U10V2KX-1GP

VCCVRM AT20
+1.8V_RUN

VCCIO AH19
VCCIO AD20
VCCIO AF22
VCCIO AD19
VCCIO AF20
VCCIO AE19
VCCIO AH20
VCCIO AB19
VCCIO AB20
VCCIO AB22
VCCIO AD22

VCCME AA34
VCCME Y34
VCCME Y35
VCCME AA35
+1.05V_VTT
6mA

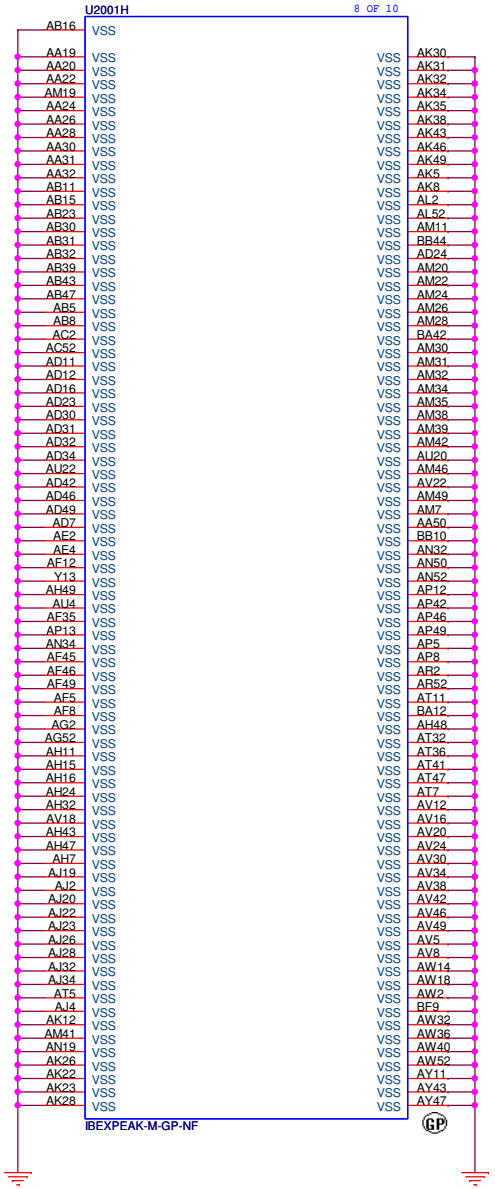
VCCSUSHDA L30 +VCCSUSHDA
R2703 0R2J-2-GP
+3.3V_ALW
C2733 SC1U10V2KX-1GP

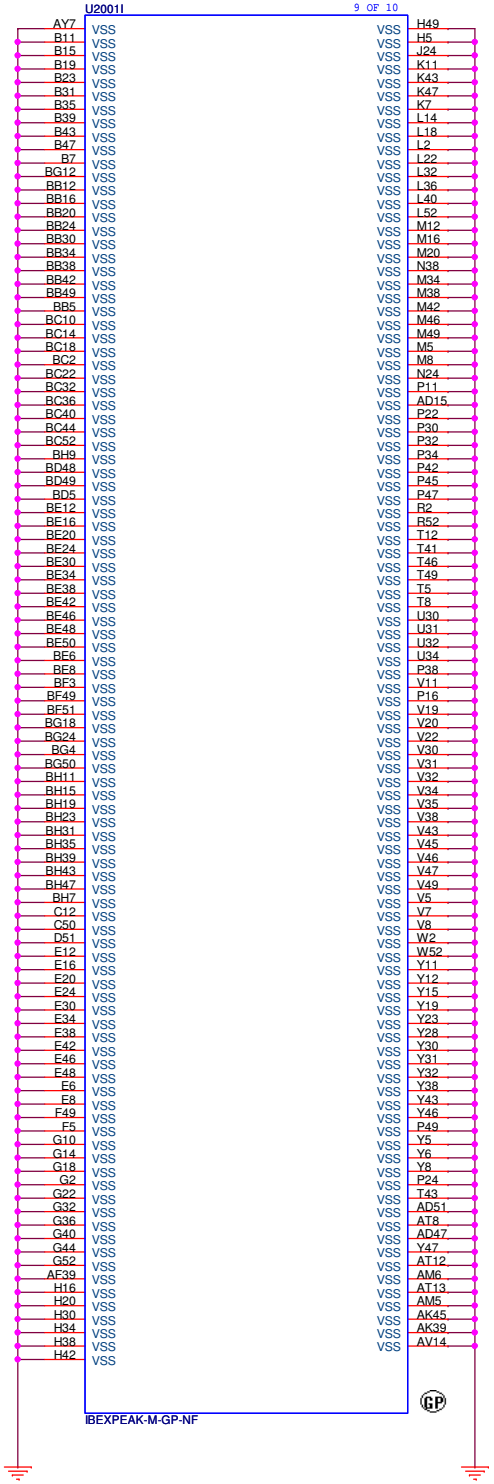
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER2)
Size: Document Number: Berry Rev: X00
Date: Thursday, October 22, 2009 Sheet 27 of 92

SSID = PCH





<Core Design>

Wistron Corporation
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Title	PCH (VSS)	
Size	Document Number: Berry	Rev: X00
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<Core Design>

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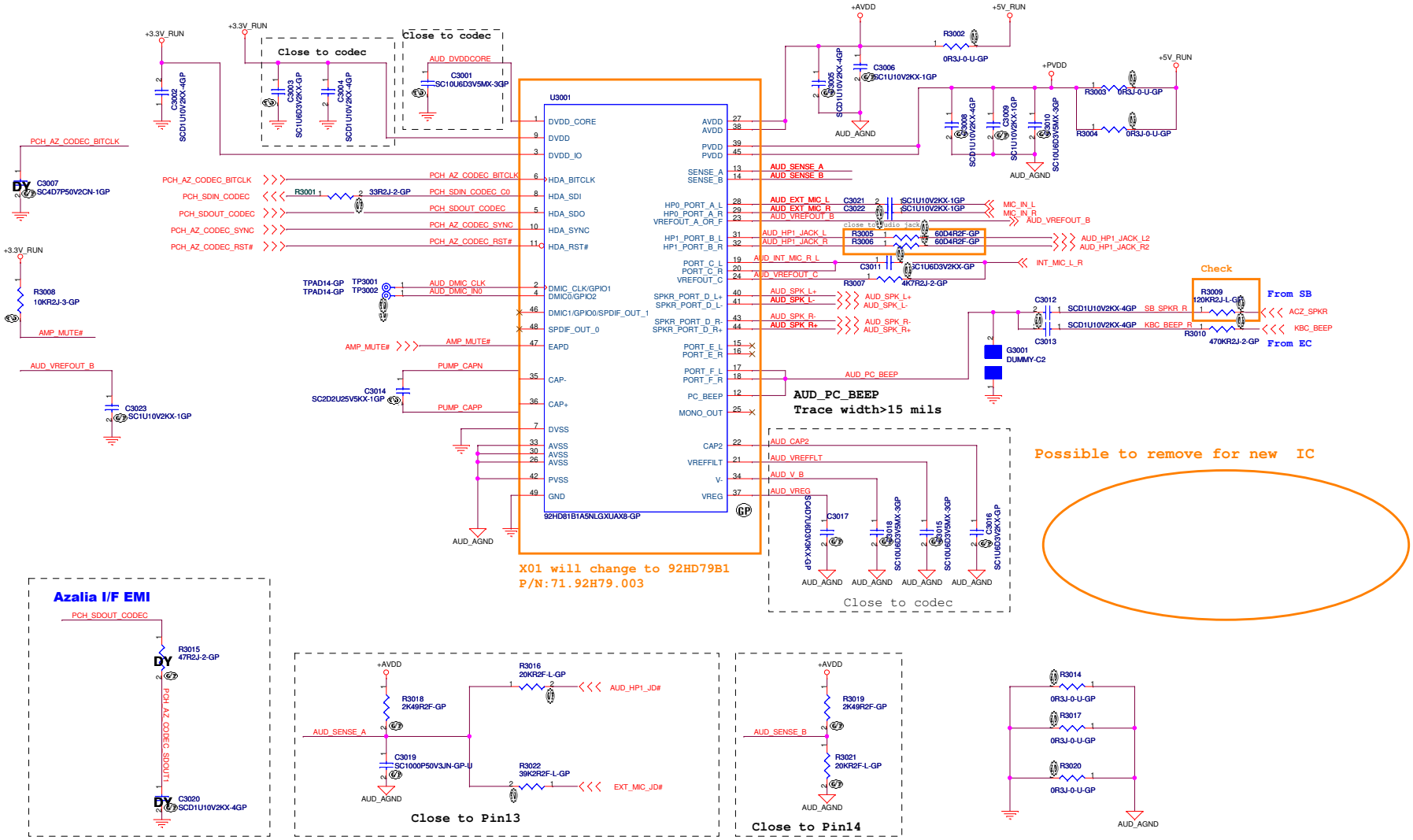
Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*X00*

Date: Wednesday, October 14, 2009 Sheet 29 of 92

SSID = AUDIO



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD81B1

Size: Custom | Document Number: Berry | Rev: X00

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *X00*

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<Core Design>

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Title

Reserved

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<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*X00*

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<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*X00*

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *X00*

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<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*X00*

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10 mW solution remove

CAP close to VCC-GND pin pair

SSID = KBC

20090702 Update 10mW circuit

PH for Discrete
Internal PL for UMA

For 512MB/1GB VRAM option

X01 change location

Vendor recomment FW can do it

Vendor recomment can remove

For EMI

MB VERSION ID

	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
X02	0	1	0
A00	0	1	1

VGA STRAP option

	GPIO24	GPIO5
UMA	0	0
Madisan	1	1
Park	1	0
Reserved	0	1

<Core Design>

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Title: KBC Nuvoton NPCE781BA0DX

Size: A2 | Document Number: Berry | Rev: X00

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<Core Design>

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Title

Reserved

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SSID = Thermal

1. Place near CPU PWM CORE and PCH.

Layout notice :
Both DN1 and DP1 routing 10 mil
trace width and 10 mil spacing.

C3905 must be near Q3901

near EMC2102

2. System Sensor(UMA Only)

Layout notice :
Both DN2 and DP2 routing 10 mil
trace width and 10 mil spacing.

Reserved DISCRETE

3.VGA Sensor(DISCRETE Only)

Layout notice :
Both VGA_THERMDA and VGA_THERMDC routing
10 mil trace width and 10 mil spacing.

C3907 must be near Q3902

4.HW T8 sensor

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

Main G7922R61U for GMT P/N:74.07922.0B3
SEC. EMC2102 for SMSC P/N:74.02102.A73

TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)

T8 shutdown is set 88 deg-C.

32K suspend clock output

84.2N702.D31

<Core Design>

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Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: Berry | Rev: X00

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<Core Design>

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Title: *Reserved*

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<Core Design>

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Title: *Reserved*

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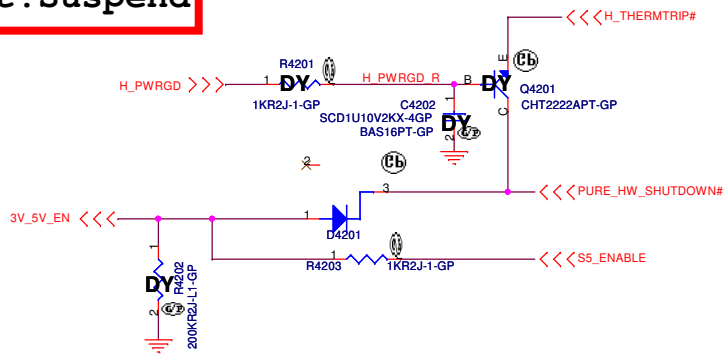
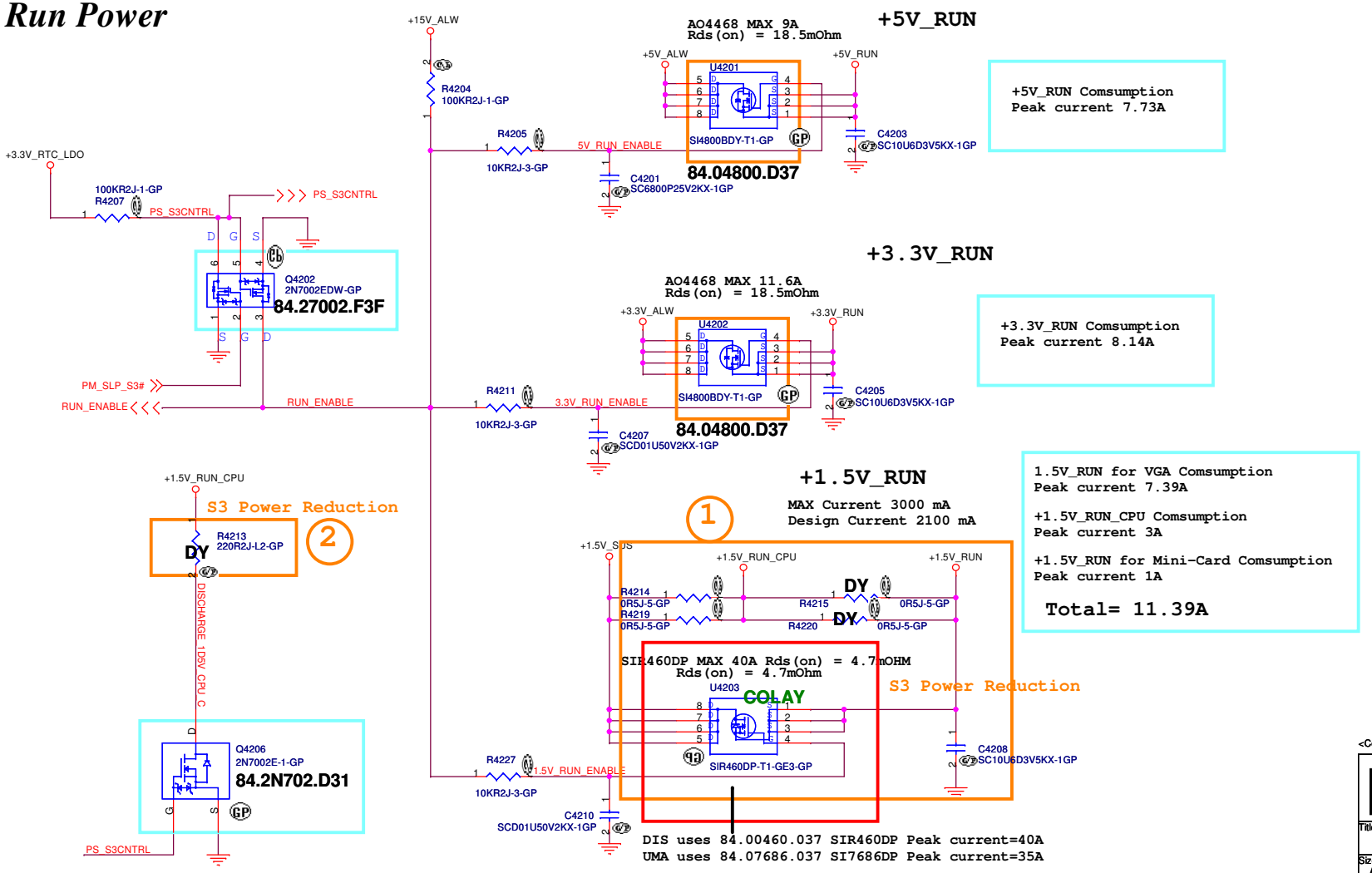
SSID = Reset.Suspend



Run Power



<Core Design>

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Title: Power Plane Enable

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Date: Thursday, October 22, 2009 Sheet 42 of 92

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<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
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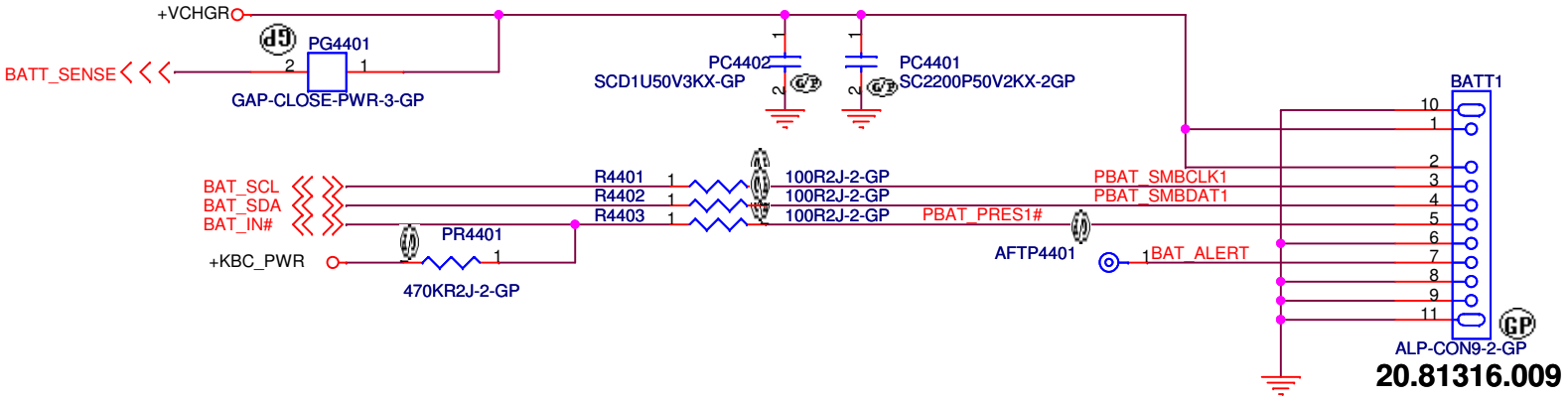
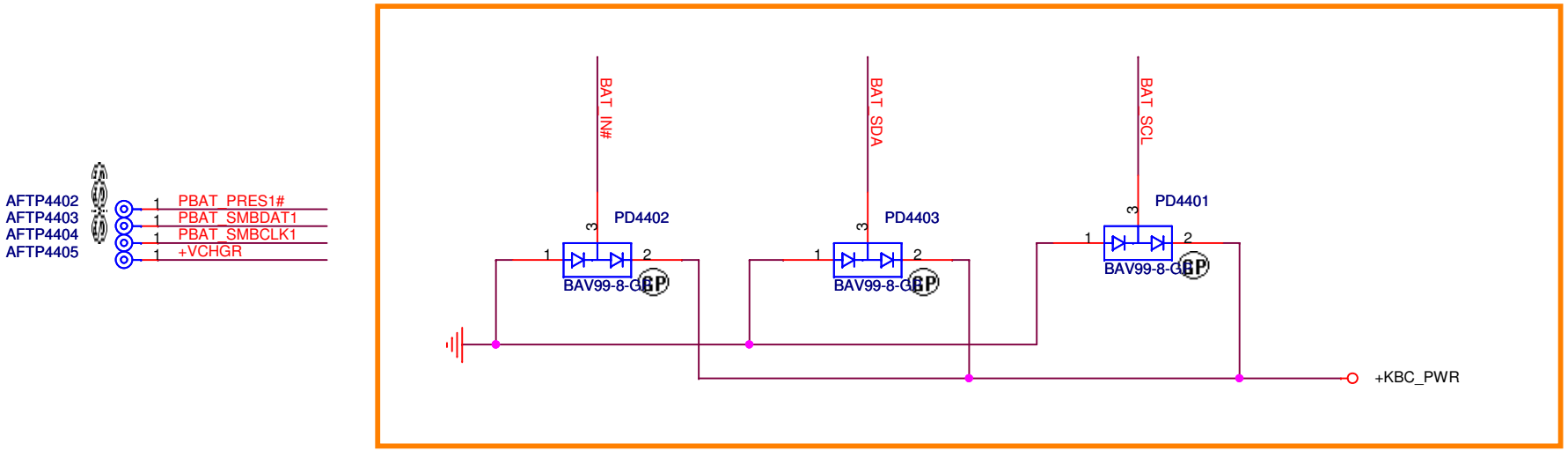
Date: Wednesday, October 14, 2009 Sheet 43 of 92

Batt Connecter



For actual location, need to be swap all pin

Close to Batt Connector



<Core Design>

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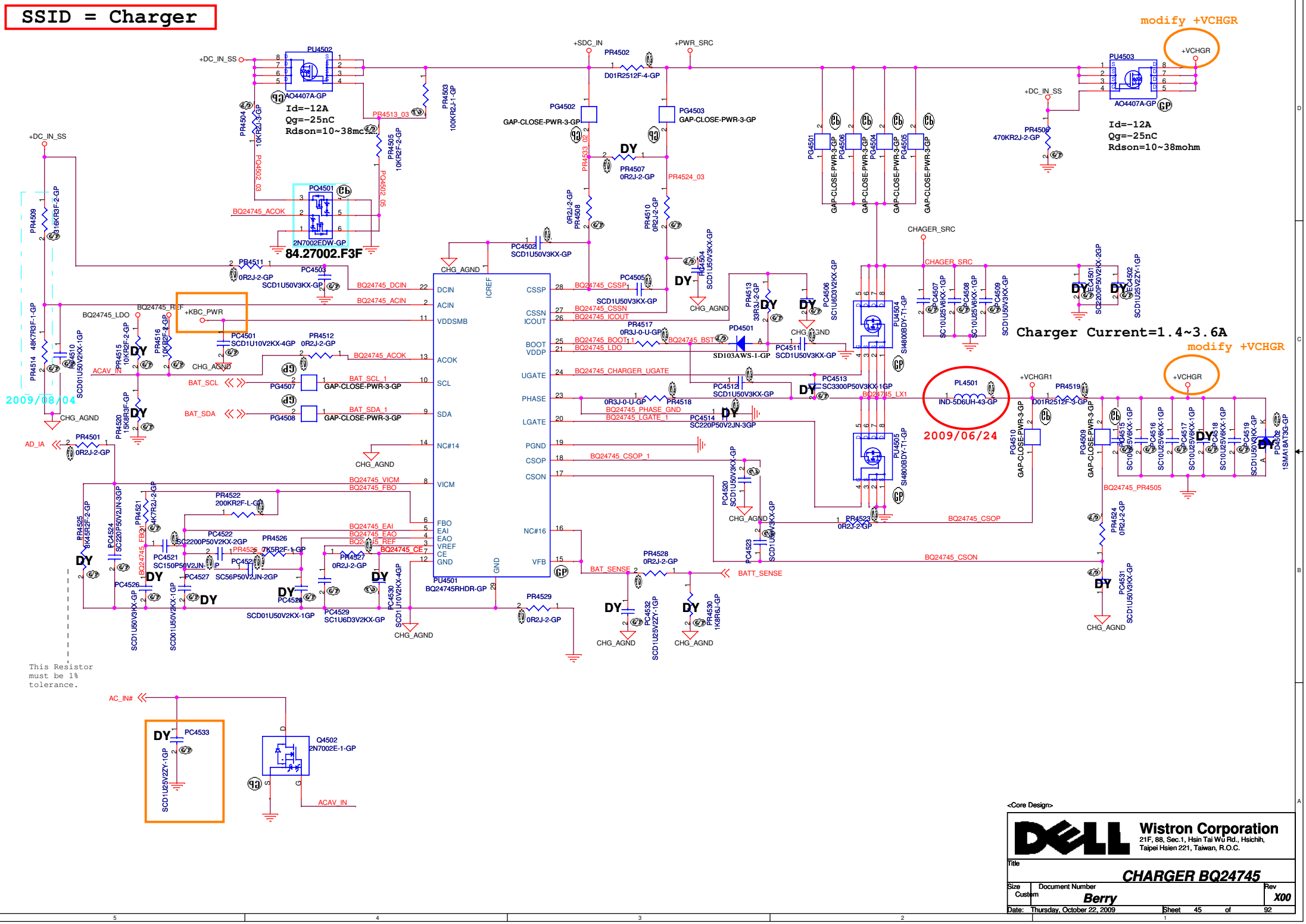
Title: **BATT CONN**

Size	Document Number	Rev
A4	Berry	X00

Date: Thursday, October 22, 2009 Sheet 44 of 92

SSID = Charger



<Core Design>

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Title: CHARGER BQ24745

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Custom	Berry	X00

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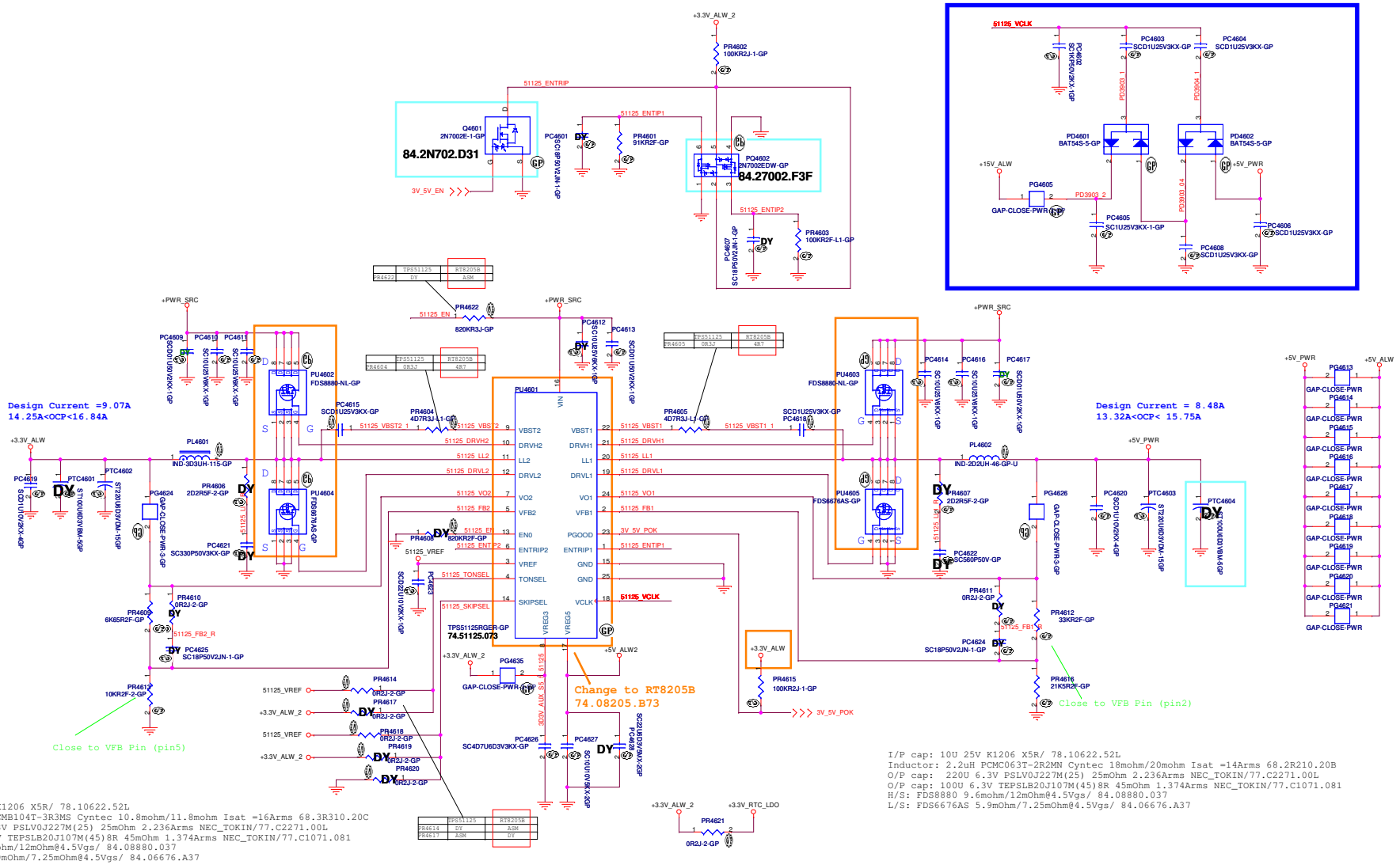

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 10.8mohm/11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37

TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

Bom

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Title: RT8205B_5V/3D3V

Size	Document Number	Rev
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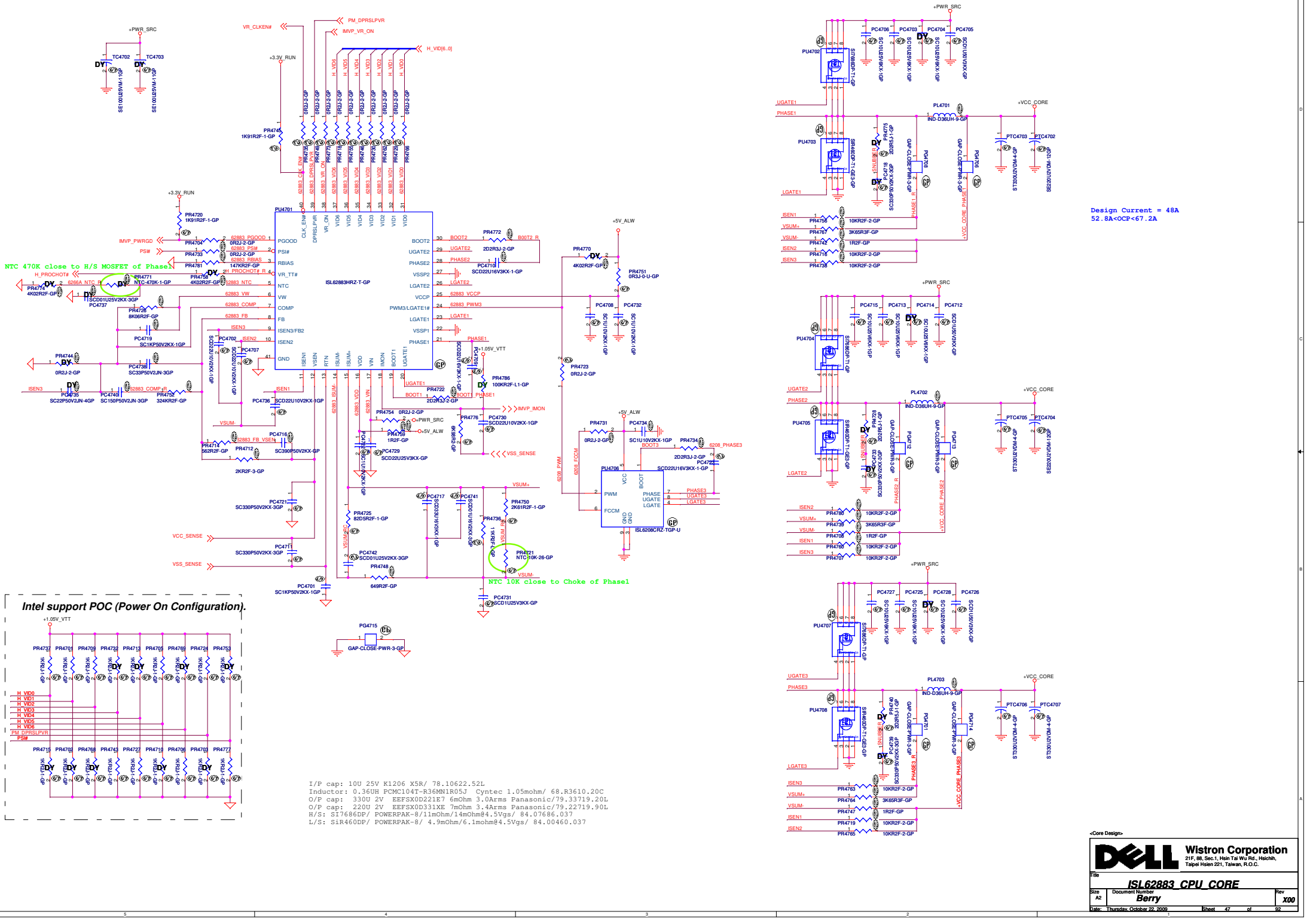

<Core Design>

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Title: ISL62883_CPU_CORE

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<Core Design>

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Title: *Reserved*

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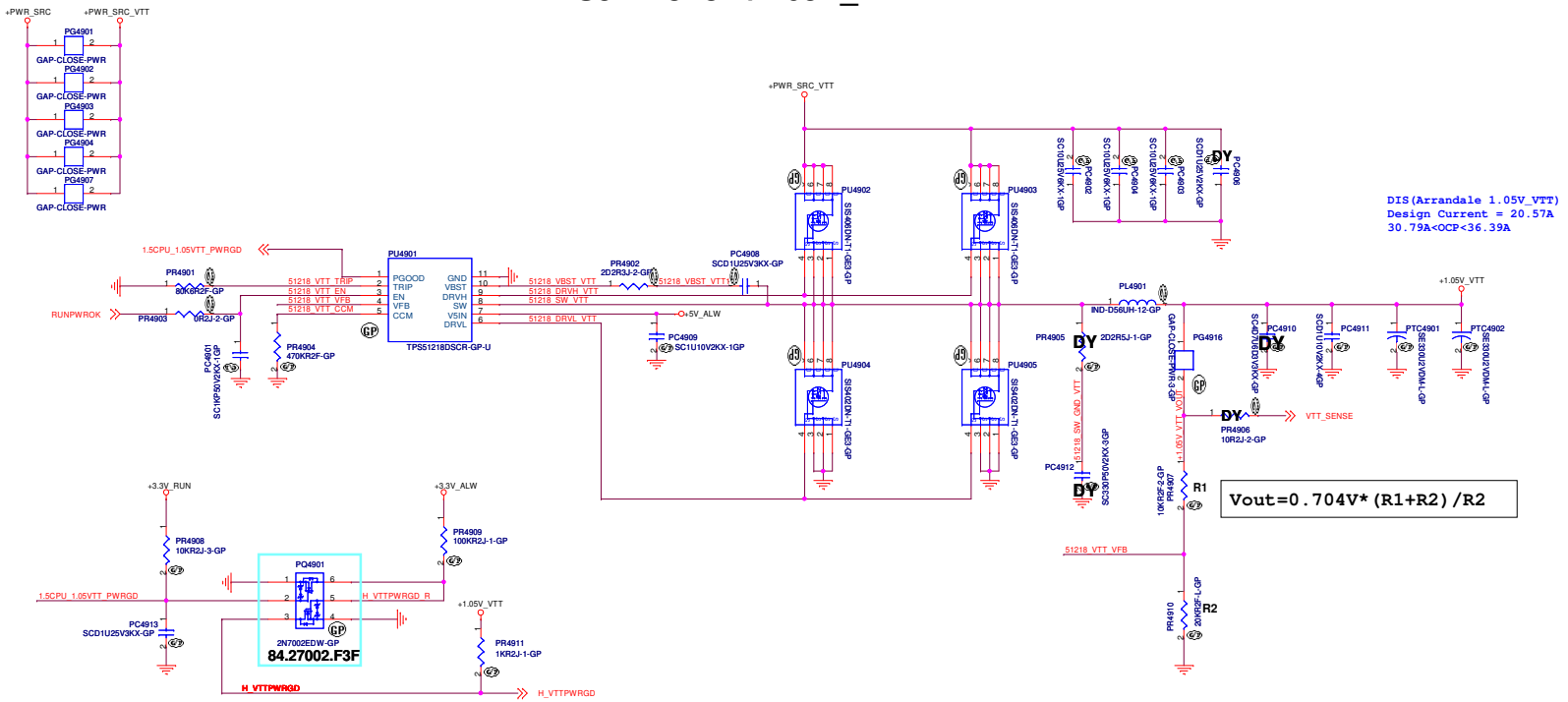
TPS51218 for +1.05V_VTT



DIS(Arrandale 1.05V_VTT)
Design Current = 20.57A
30.79A<OCP<36.39A

Vout=0.704V*(R1+R2)/R2

Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

<Core Design>

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Title: TPS51218 +1.05V_VTT

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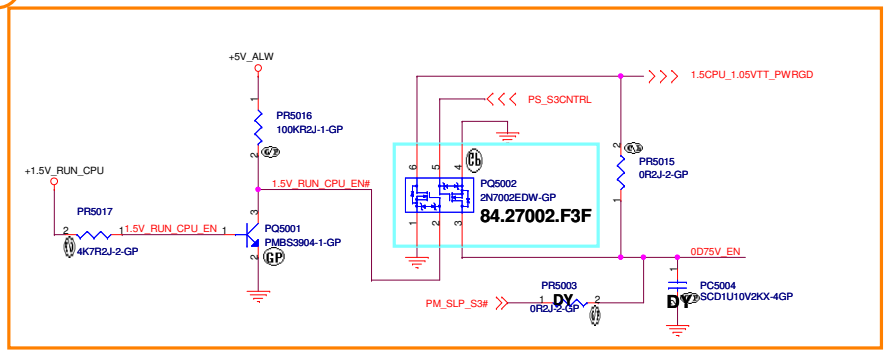
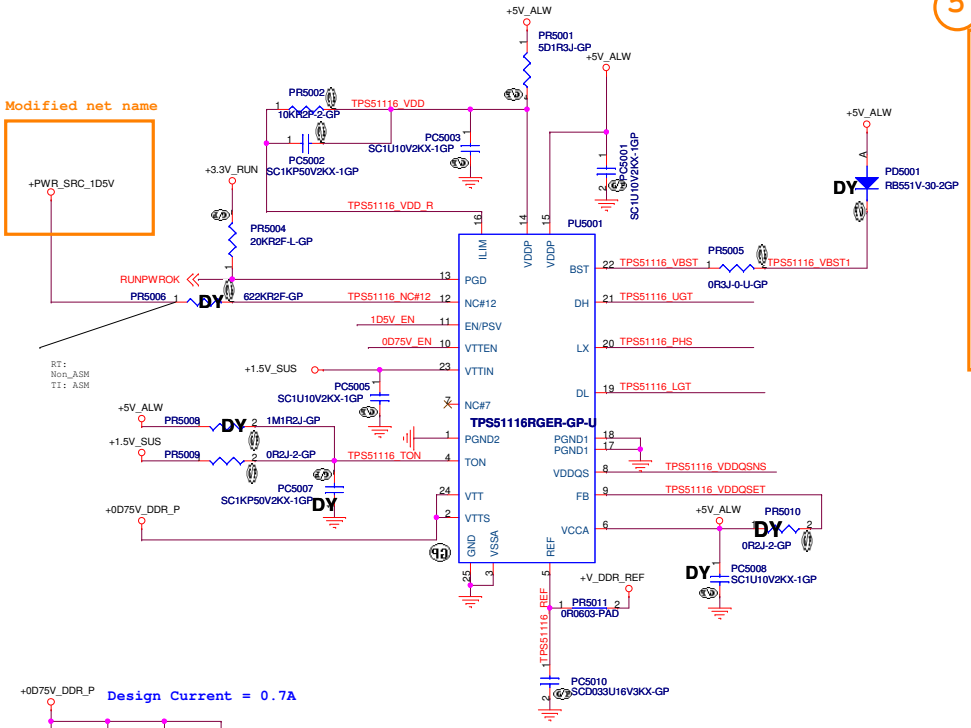
SSID = PWR.Plane.Regulator_1p5v0p75v

Modified net name

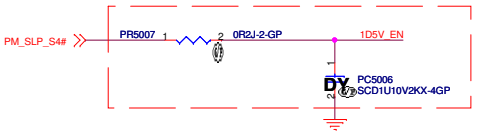
+PWR_SRC_1D5V

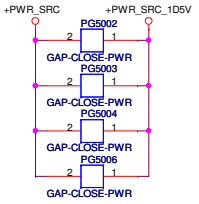
5 S3 Power Reduction



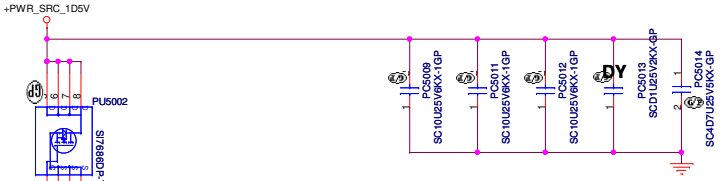


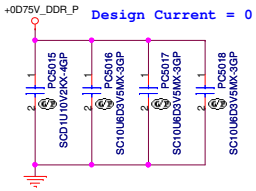
RT: Non_ASM
TI: ASM



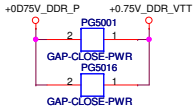


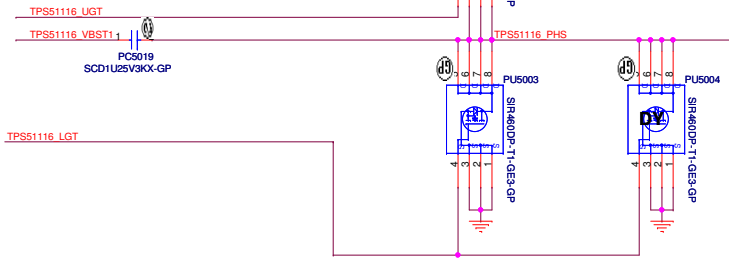
Design Current = 14.45A
22.71A<OCP< 26.84A

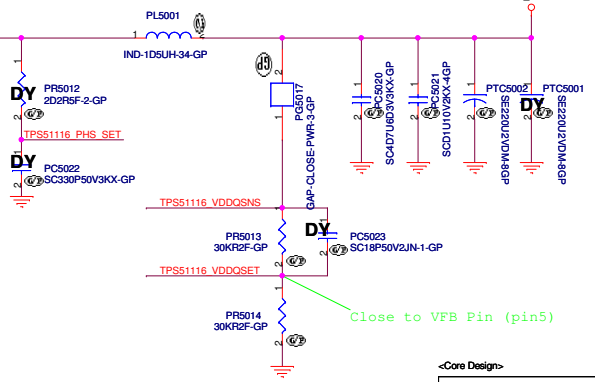




Design Current = 0.7A







State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

<Core Design>

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Title: TPS51116_+1.5V_SUS

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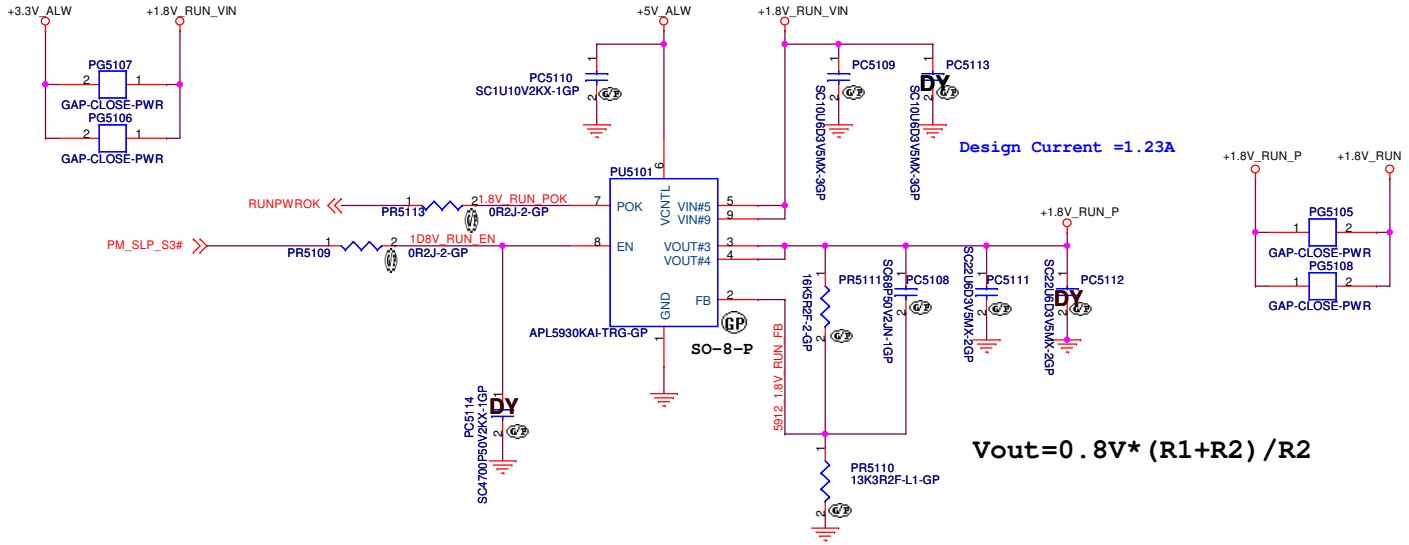
SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



<Core Design>

Wistron Corporation
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Title	APL5930 +1.8V RUN	
Size: A3	Document Number: Berry	Rev: X00
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<Core Design>

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Title: *Reserved*

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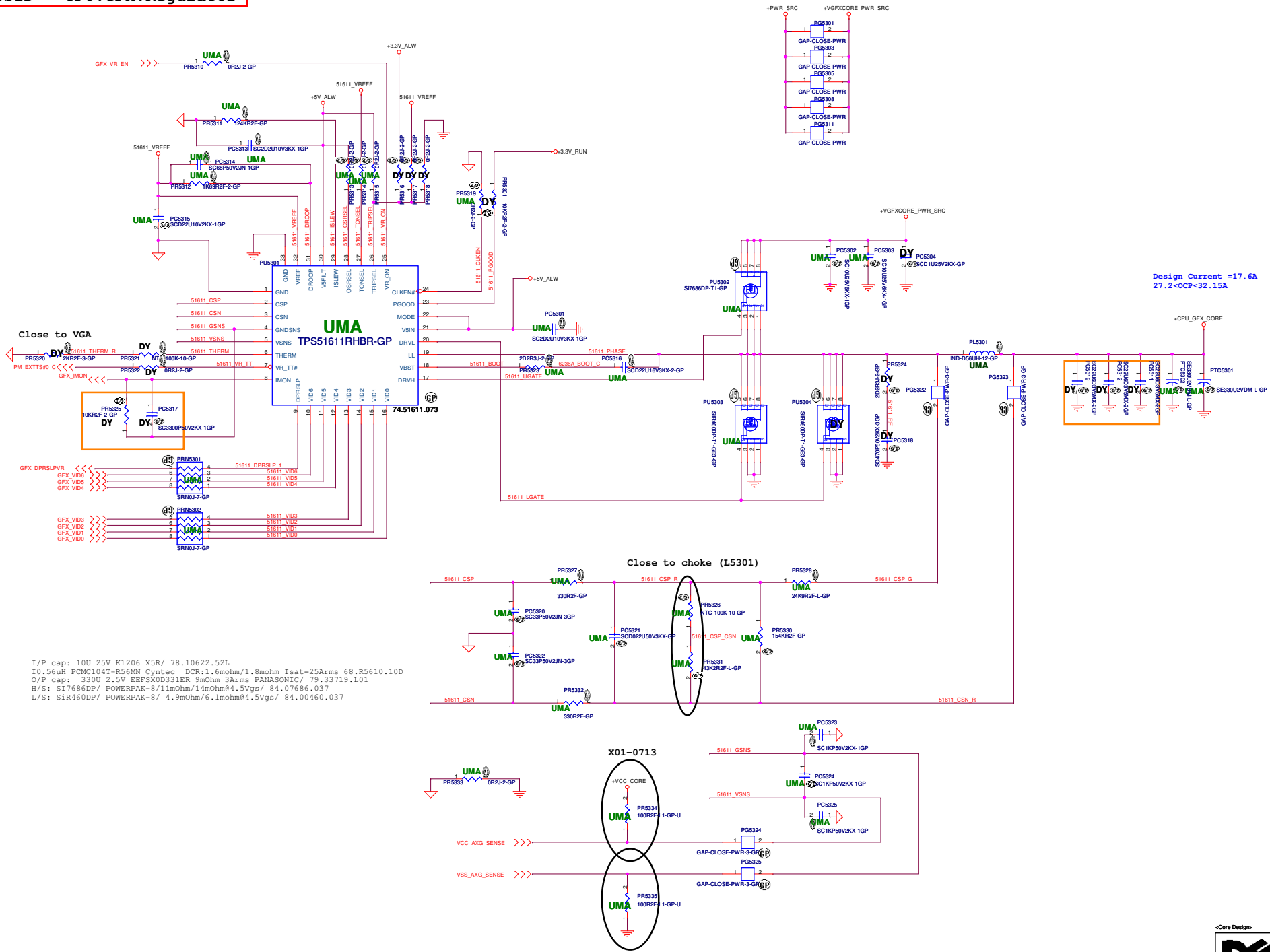
SSID = CPU.GFX.Regulator



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51611_+GFX_CORE(UMA)

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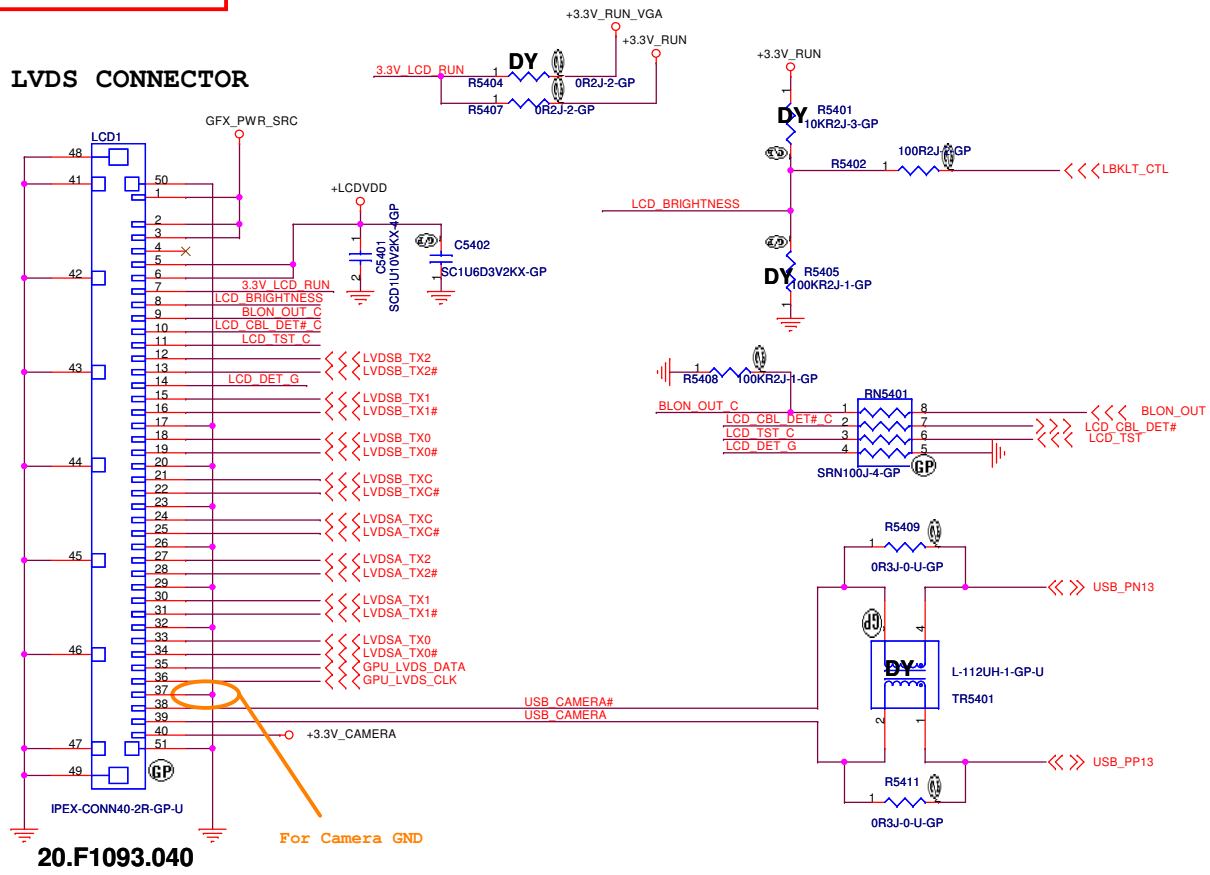
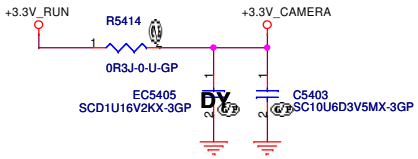
SSID = VIDEO

LVDS CONNECTOR

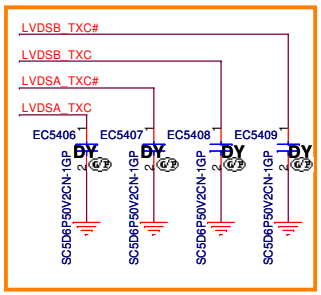


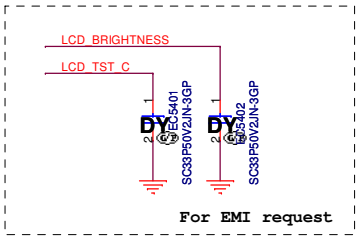
20.F1093.040

Camera Power



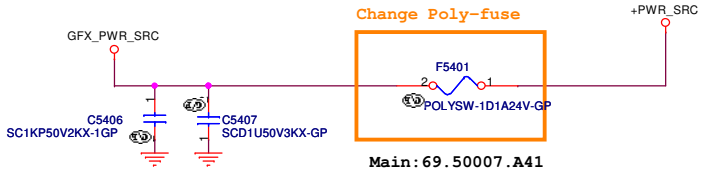
Close to LVDS connector





SSID = Inverter

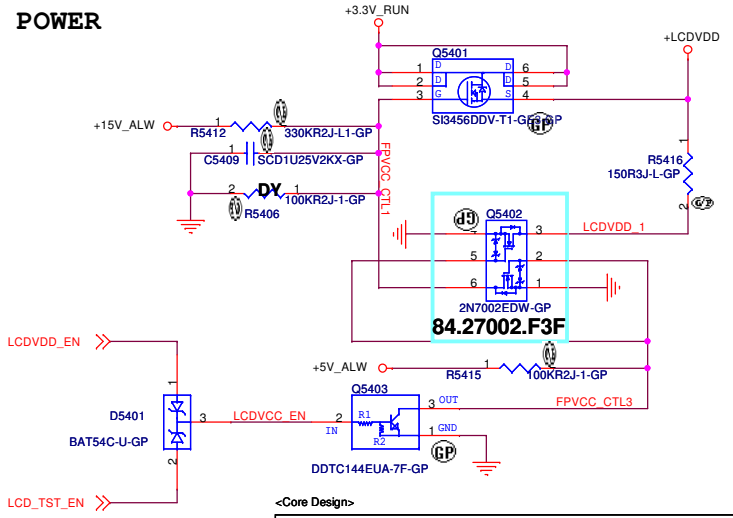
INVERTER POWER



Main:69.50007.A41
Second:69.50007.A31

SSID = VIDEO

LCD POWER



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD/Inverter Connector	
Size: A3	Document Number: Berry	Rev: X00
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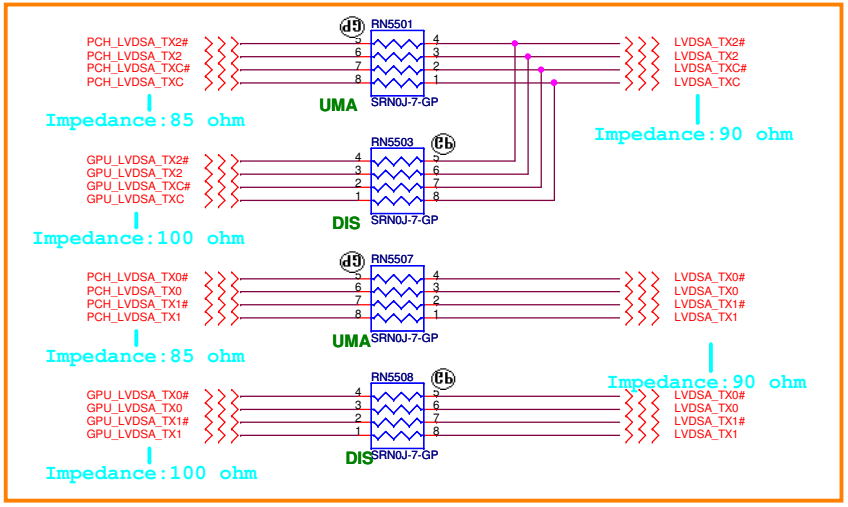
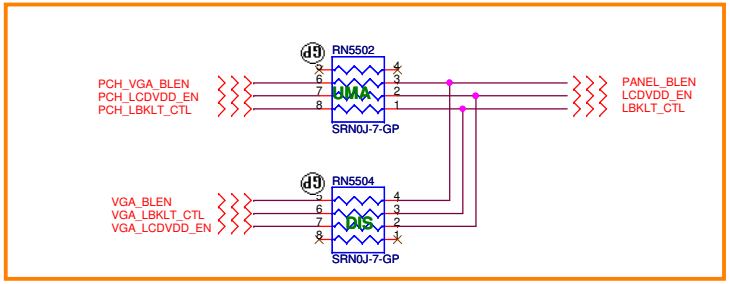
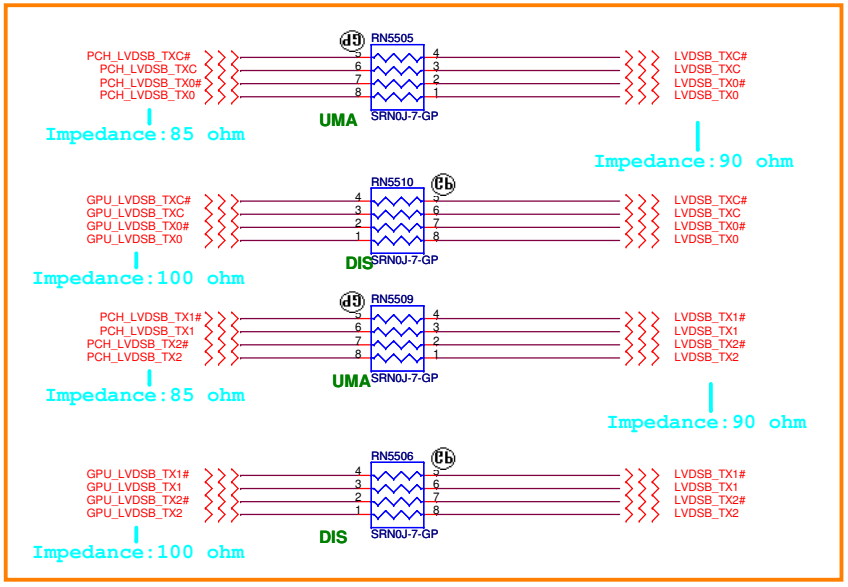
LVDS Channel A



Panel BL brightness/Power En/BL En



LVDS Channel B



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LVDS Switch	
Size	Document Number: Berry	Rev: X00
Date: Thursday, October 22, 2009	Sheet 55 of 92	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size	Document Number	Rev
A3	*Berry*	*X00*

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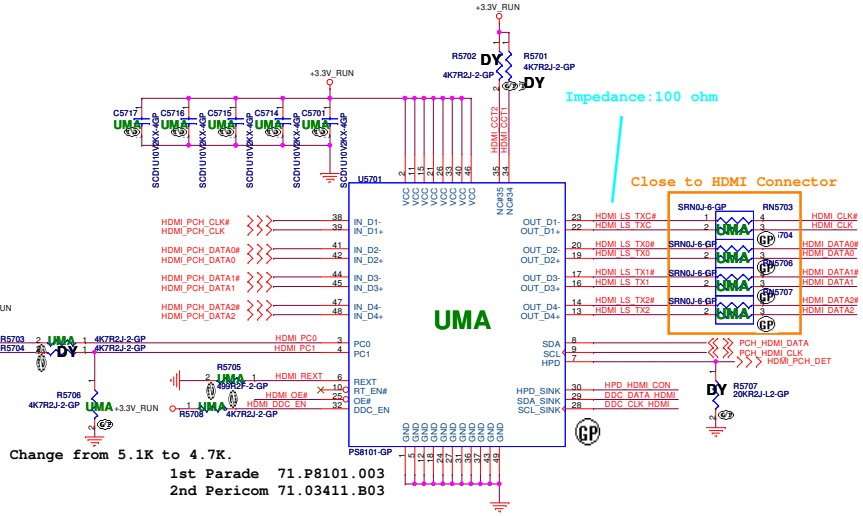
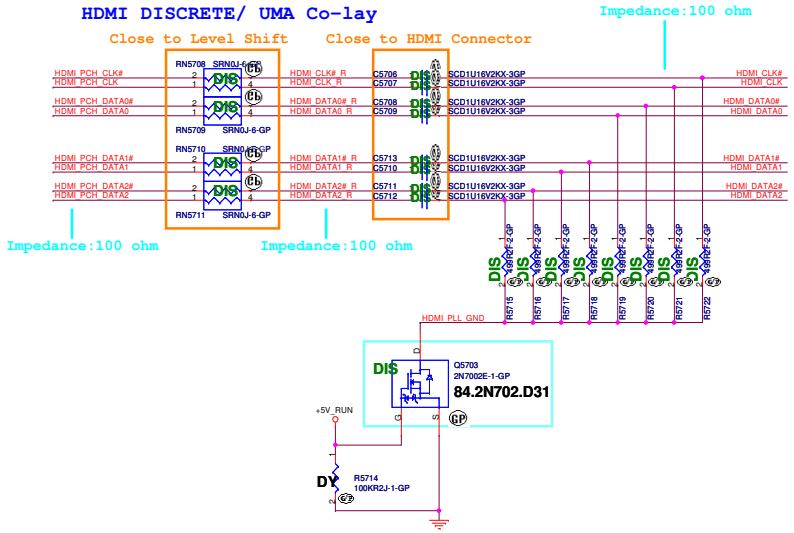
SSID = VIDEO

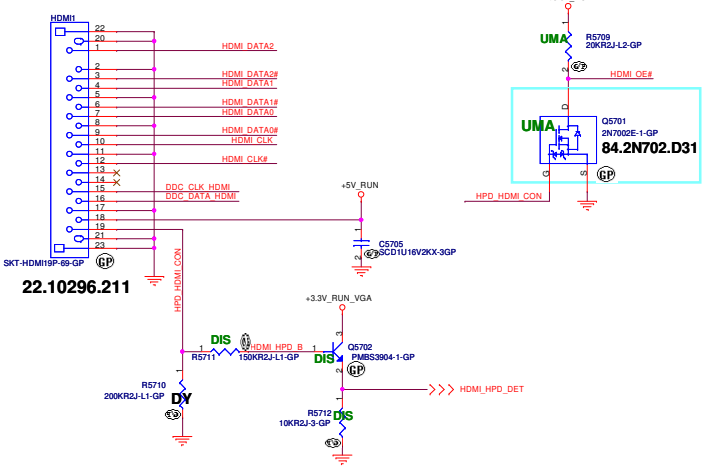
HDMI Level Shifter & CONNECTOR



HDMI DISCRETE/ UMA Co-lay



HDMI CONN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

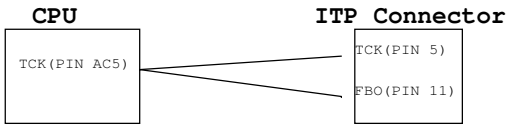
Size: A2 | Document Number: Berry | Rev: X00

Date: Thursday, October 22, 2009 | Sheet 57 of 92

SSID = User.Interface

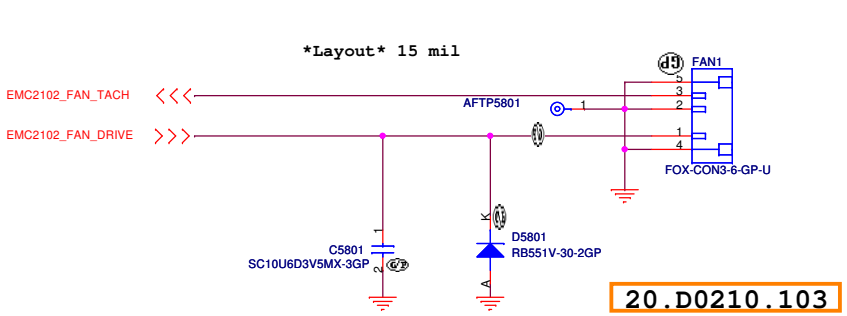
ITP Connector

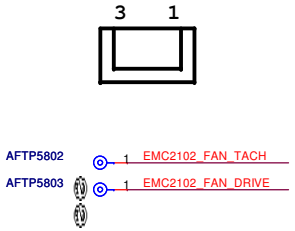
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



SSID = Thermal

Fan Connector





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

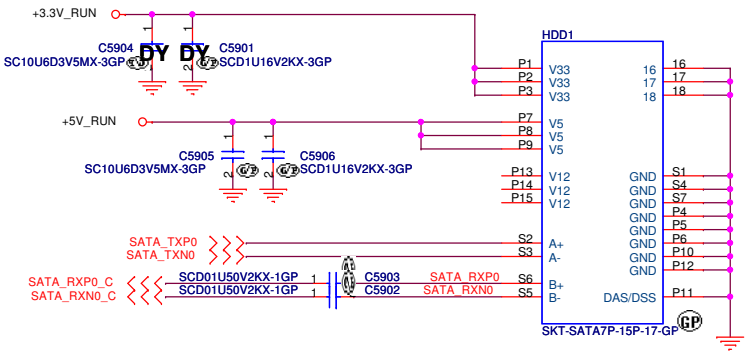
Title: ITP/Fan Connector

Size: A3 | Document Number: Berry | Rev: X00

Date: Thursday, October 22, 2009 | Sheet 58 of 92

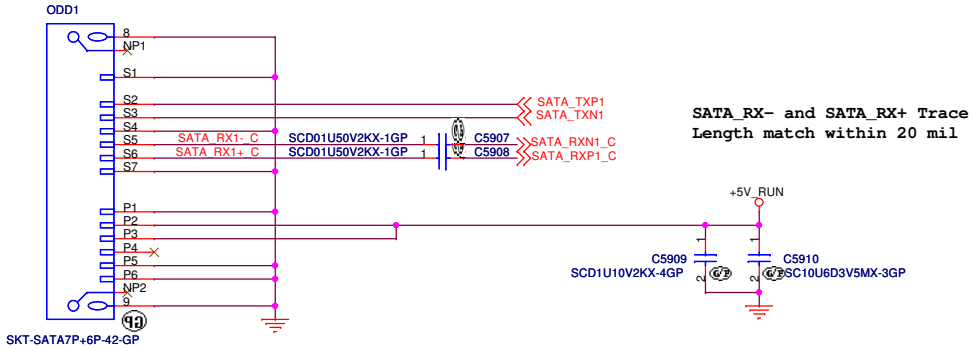
SSID = SATA

SATA HDD Connector



62.10065.C71

ODD Connector



SATA_RX- and SATA_RX+ Trace Length match within 20 mil

62.10065.581

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
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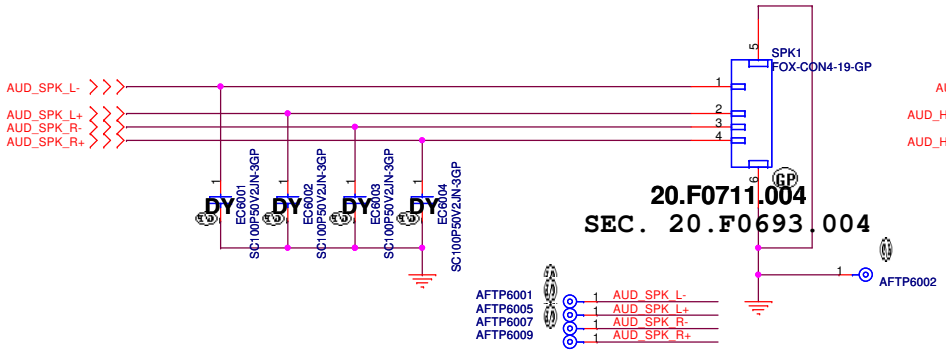
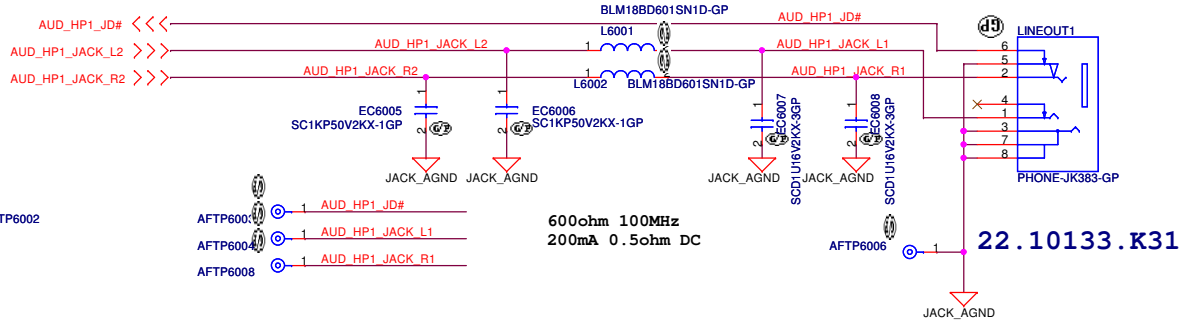
SSID = AUDIO

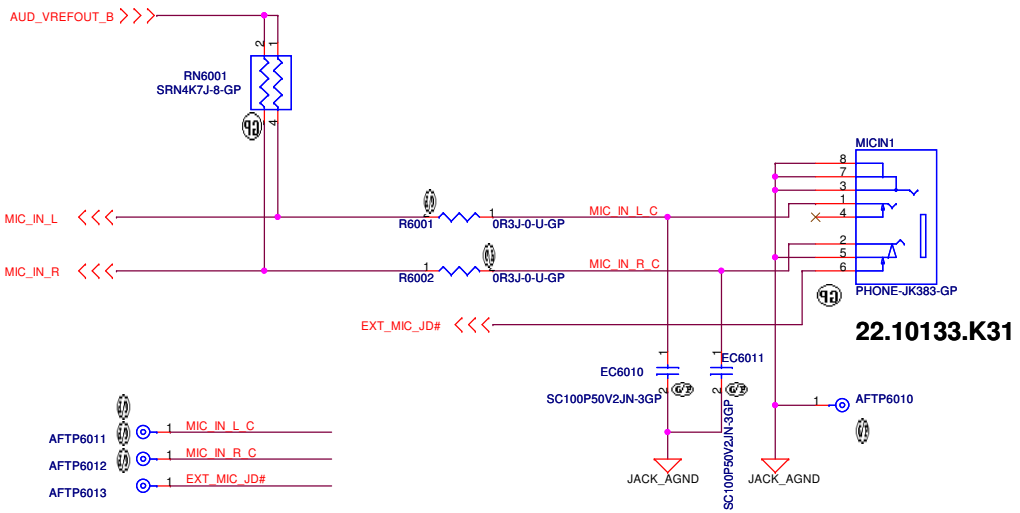
Speaker Connector



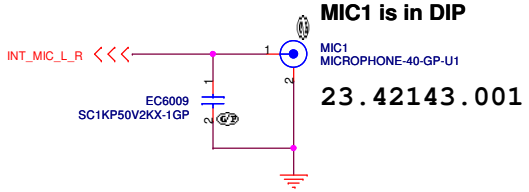
LINE1 OUT

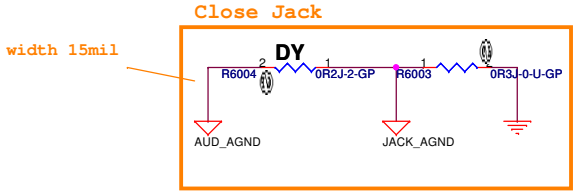


MIC IN



Internal Microphone





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack		
Size: A3	Document Number: Berry	Rev: X00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

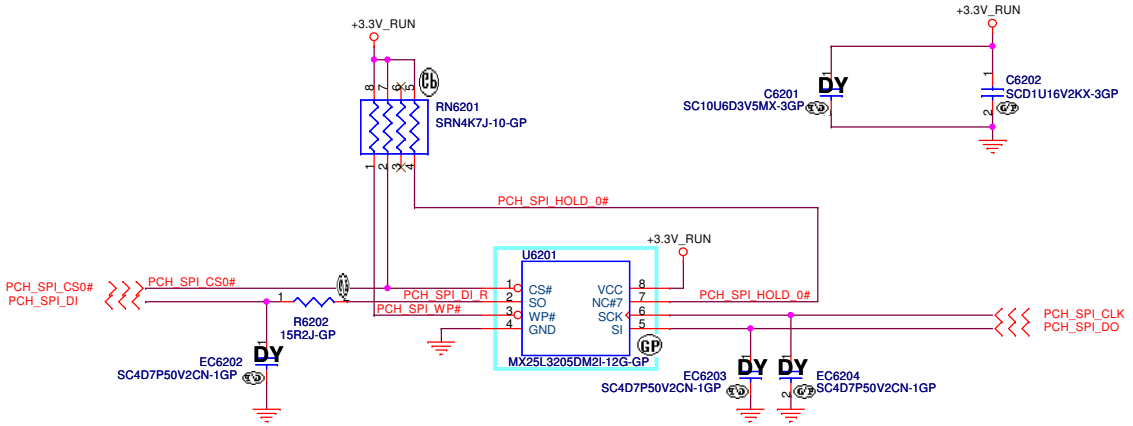
Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*X00*

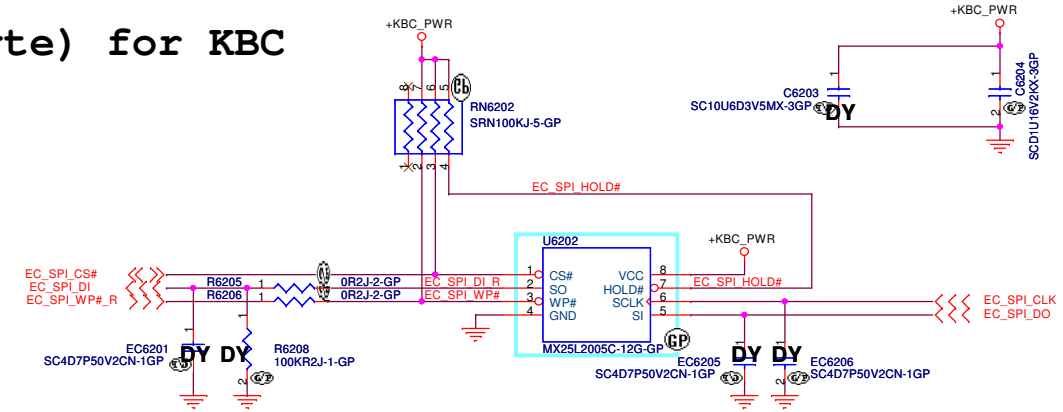
Date: Wednesday, October 14, 2009 Sheet 61 of 92

SSID = Flash.ROM

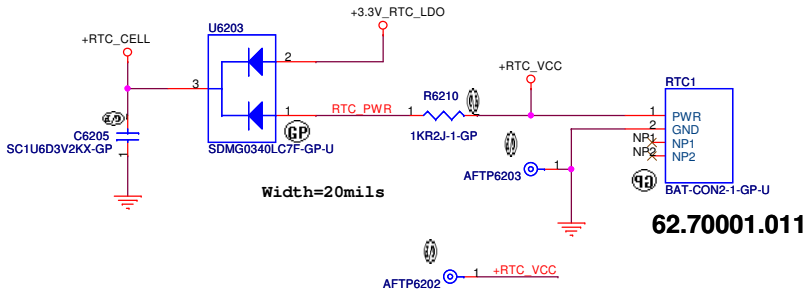
SPI FLASH ROM (4M byte) for PCH



SPI FLASH ROM (256K byte) for KBC



SSID = RBATT



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Flash/RTC	
Size: A3	Document Number: Berry	Rev: X00
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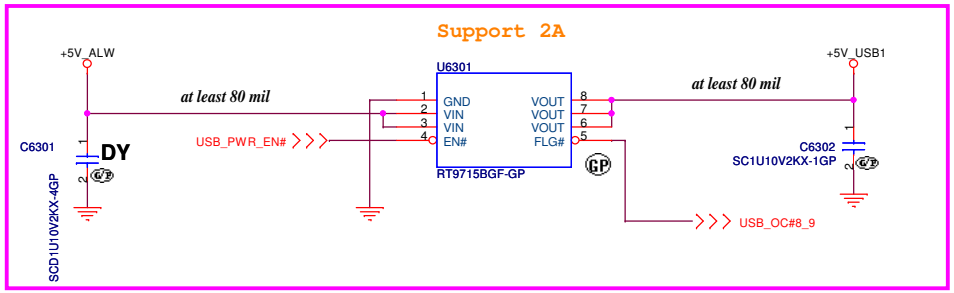
SSID = USB

IO Board USB Power

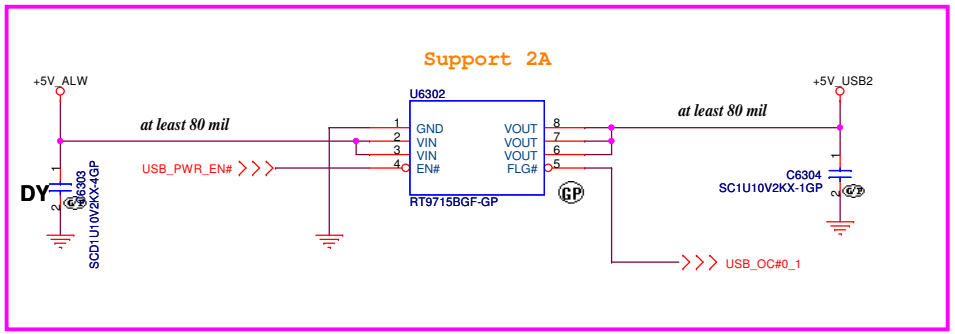
Close to I/O connector

Main RT9715BGF P/N:74.09715.B79
SEC G547F2P81U P/N: 74.00547.A79



CRT Board USB Power

Close to CRT Board connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB Power SW	
Size	Document Number: Berry	Rev: X00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

Size	Document Number	Rev
A4	***Berry***	***X00***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size	Document Number	Rev
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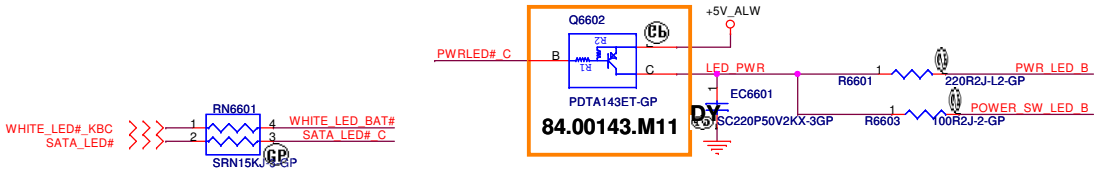
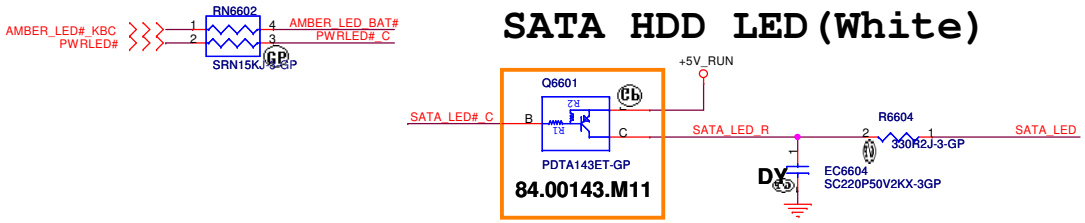
SSID = User.Interface

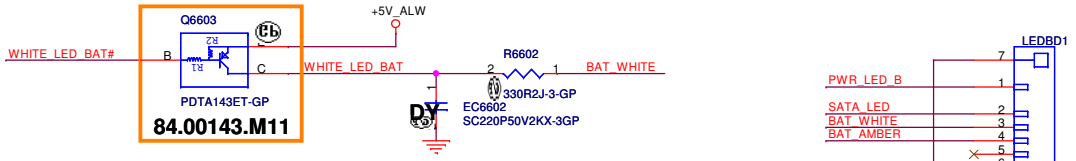
Power LED(White)



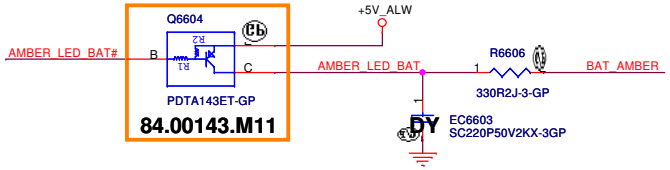
SATA HDD LED(White)



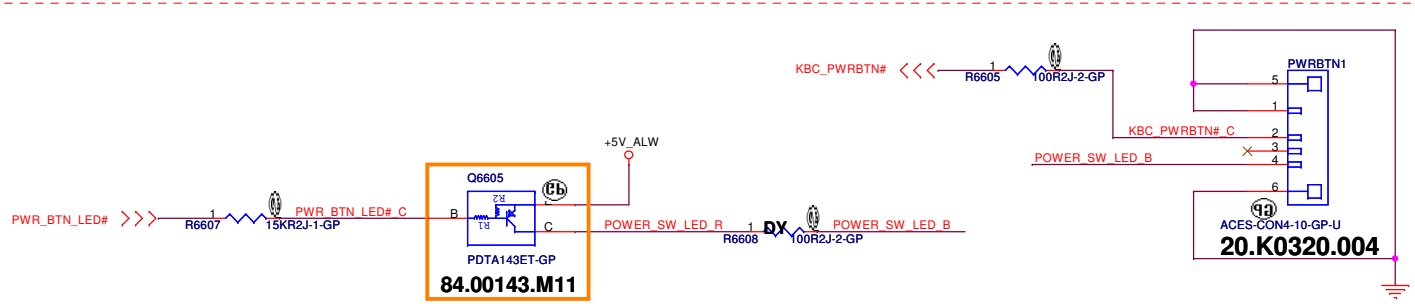
Battery LED1(White)



Battery LED2(Amber)



Power button LED(White)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
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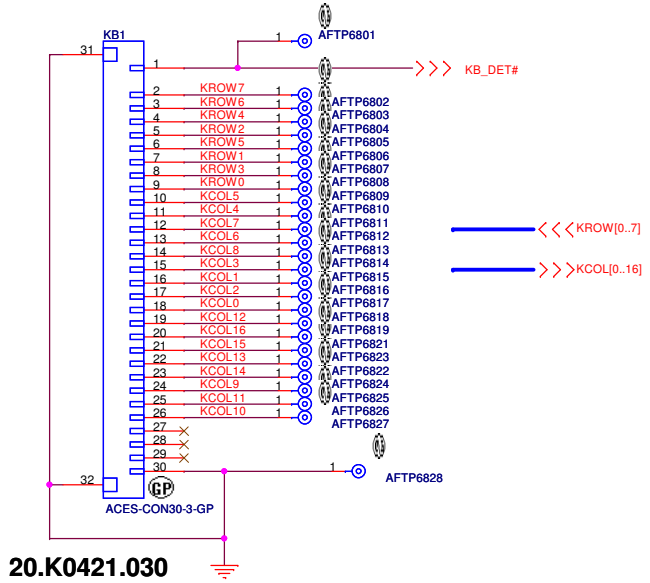
SSID = KBC

Internal KeyBoard Connector

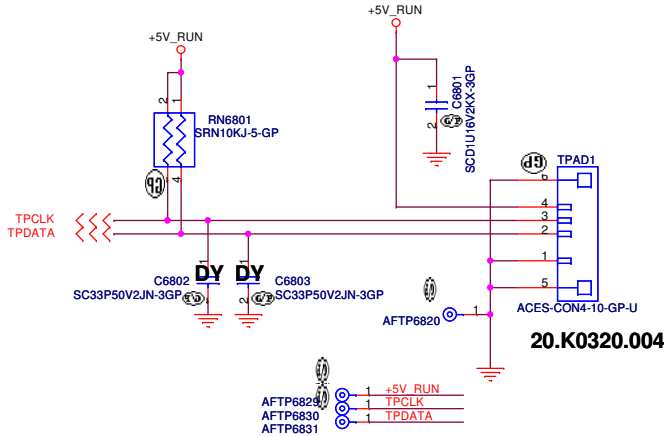


20.K0421.030

Sec. 20.K0259.030

SSID = Touch.Pad

TouchPad Connector



20.K0320.004

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Key Board/Touch Pad	
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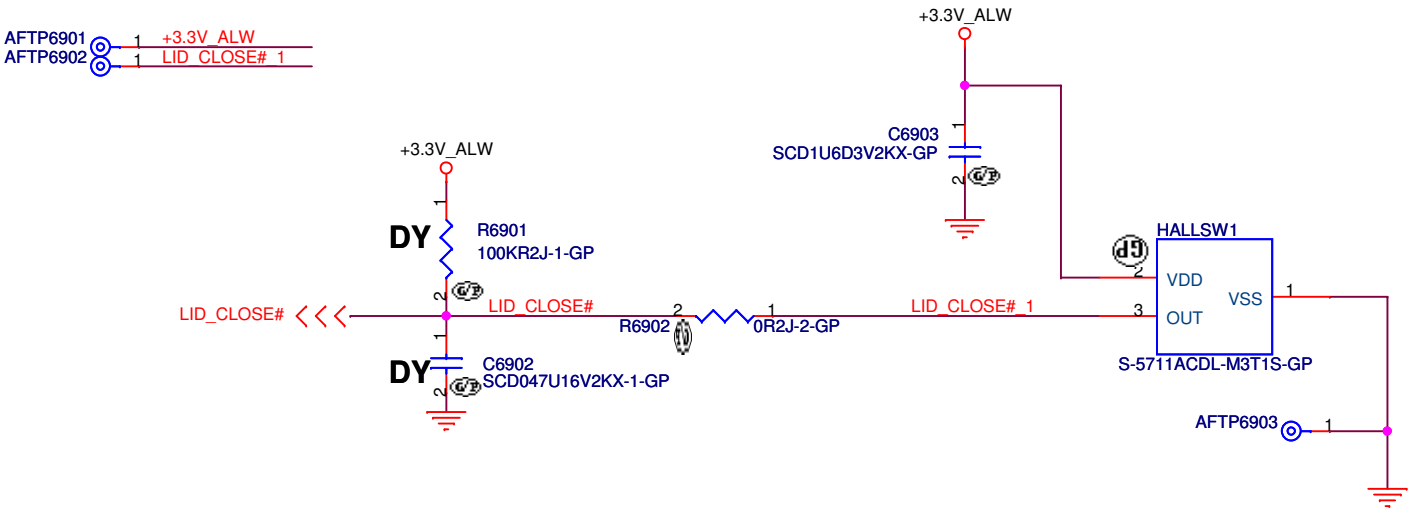

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

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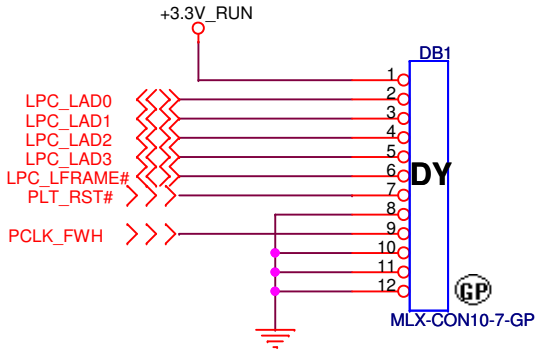

20.D0183.110

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
A4	***Berry***	***X00***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size: A3 | Document Number: Berry | Rev: X00

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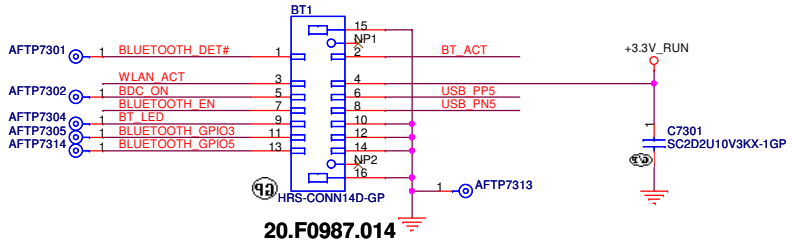
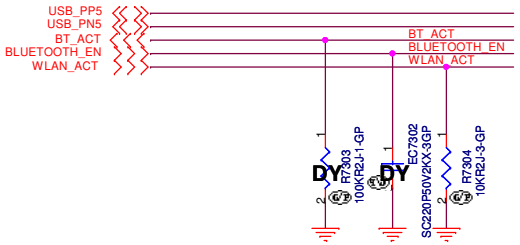
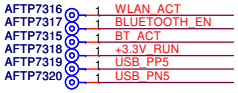
SSID = User.Interface

Bluetooth Module conn.



20.F0987.014





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth

Size: A3 | Document Number: Berry | Rev: X00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

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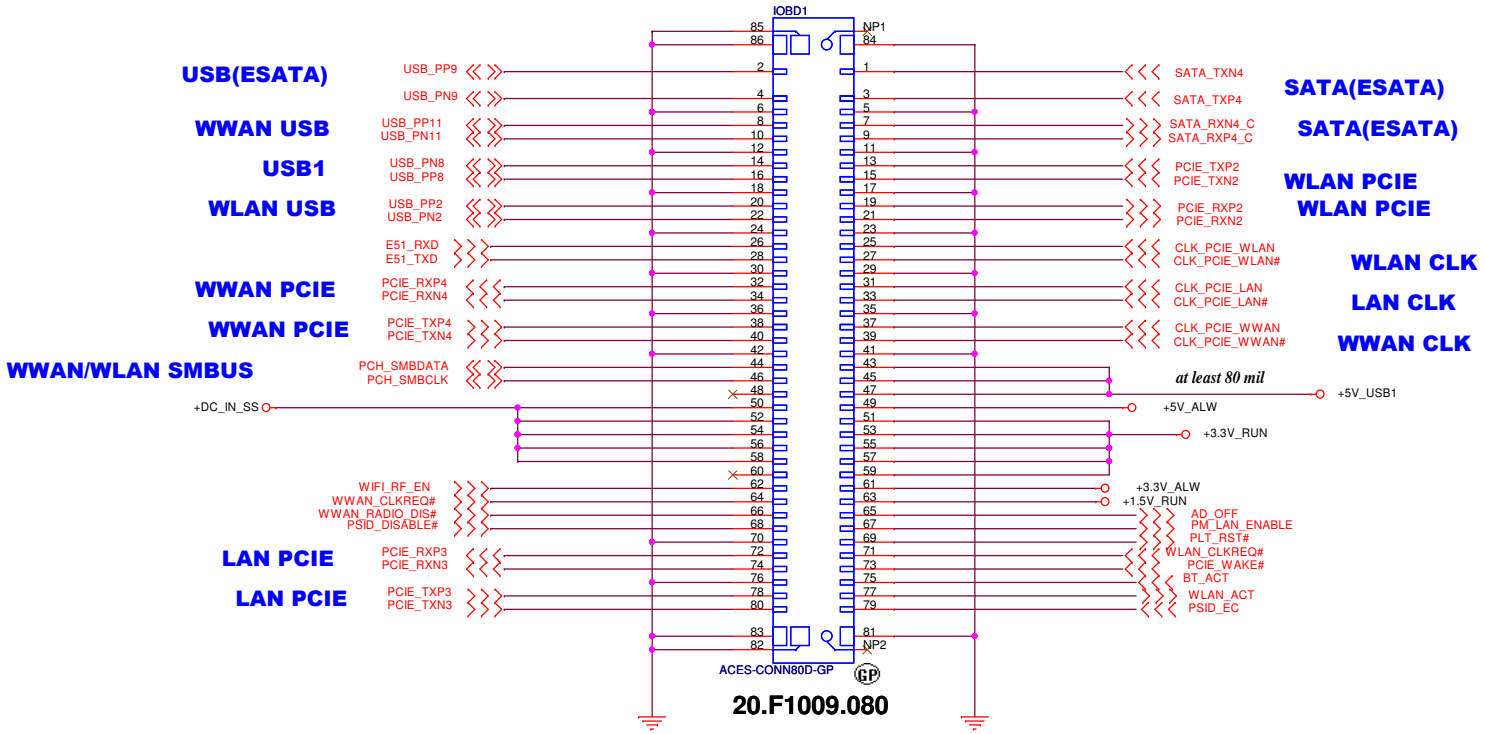
IO Board CONN 80 pin



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *IO Board Connector*

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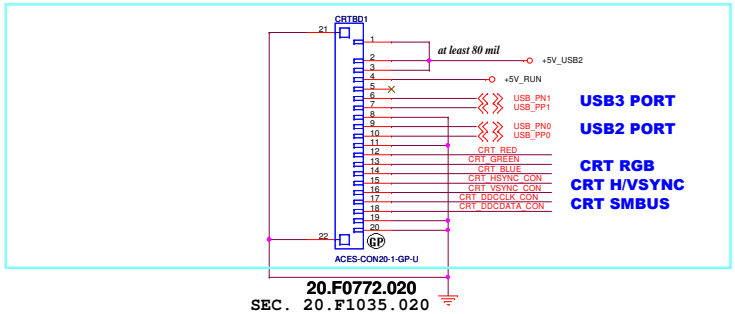
CRT Board Connector



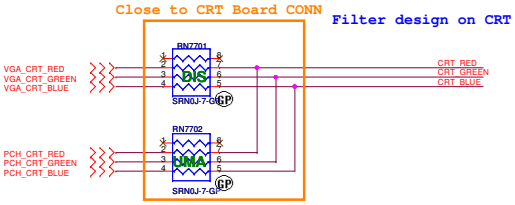
20.F0772.020

SEC. 20.F1035.020

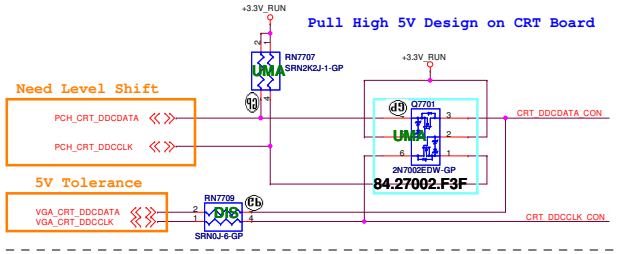
CRT RGB

Close to CRT Board CONN

Filter design on CRT Board

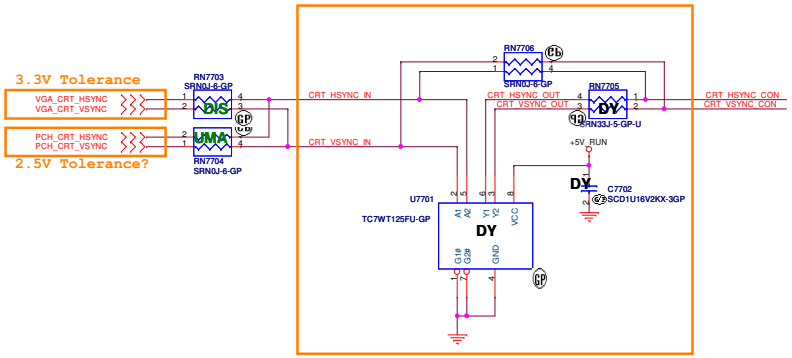


CRT DDCDATA & DDCCLK level shift



CRT Hsync & Vsync level shift

Close to CRT Board CONN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

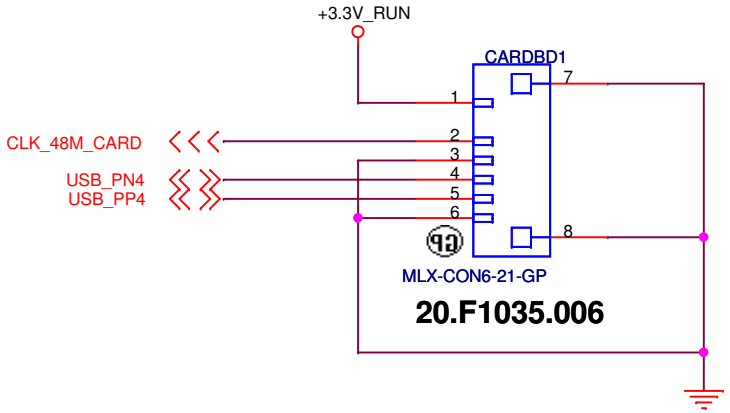
Title: CRT Board Connector

Size: A2 | Document Number: Berry | Rev: X00

Date: Thursday, October 22, 2009 | Sheet 77 of 92

SSID = SDIO

Card Reader connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN		
Size: A4	Document Number: Berry	Rev: X00
Date: Thursday, October 22, 2009	Sheet 78 of 92	

H1
HTE95BE95R29-R-5-GP

H2
HTE95BE95R29-R-5-GP

H3
HTE95BE95R29-R-5-GP

H4
HTE95BE95R29-R-5-GP

H5
HTE95BE95R29-R-5-GP

H6
HTE95BE95R29-R-5-GP

H7
HTE95BE95R29-R-5-GP

H8
HTE95BE95R29-R-5-GP

H9
HTE95BE95R29-R-5-GP

H10
HOLE335R115-GP

CPU Thermal module hole

HTML1
HOLE197R166-GP

HTML2
HOLE197R166-GP

HTML3
HOLE197R166-GP

DY DY DY

GPU Thermal module hole

HGPU1
STF237R117H83-1-GP

stand off

HBT1
STF237R115H123-GP

EMI Reserve

+PWR_SRC

EC7901 EC7902 EC7904 EC7903 EC7905 EC7907 EC7909

DY DY DY DY DY DY DY

SCD1U25V2KX-GP

+VGFXCORE_PWR_SRC

EC7906

DY

SCD1U25V2KX-GP

+PWR_SRC_VTT

EC7911

DY

SCD1U25V2KX-GP

+PWR_SRC_1D5V

EC7916

DY

SCD1U25V2KX-GP

EMI Reserve

SPR1

SPRING-58-GP

DY

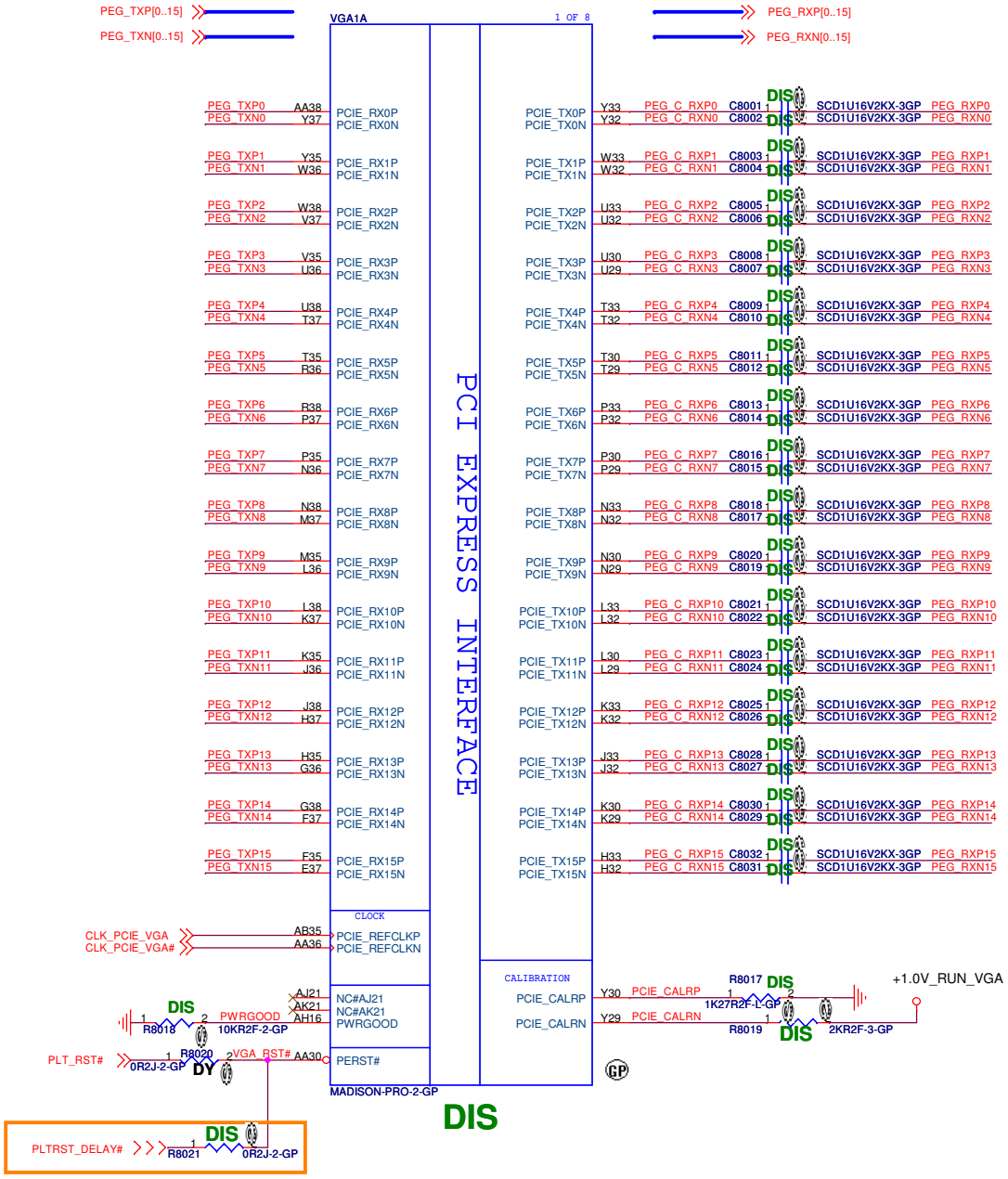
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS/EMI Capacitors***

Size	Document Number	Rev
A4	*Berry*	*X00*

Date: Thursday, October 22, 2009 Sheet 79 of 92



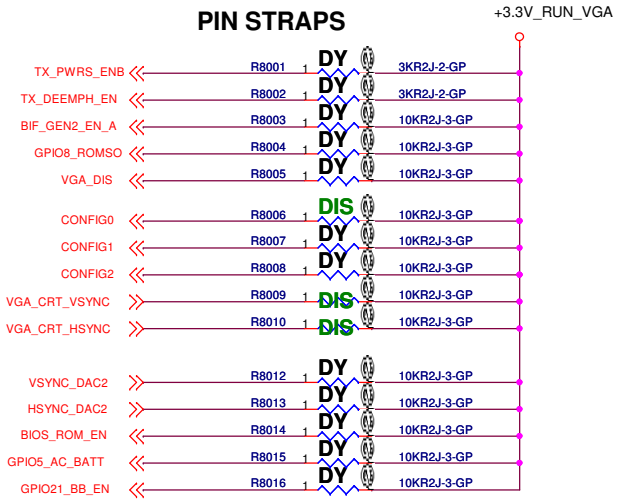
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS



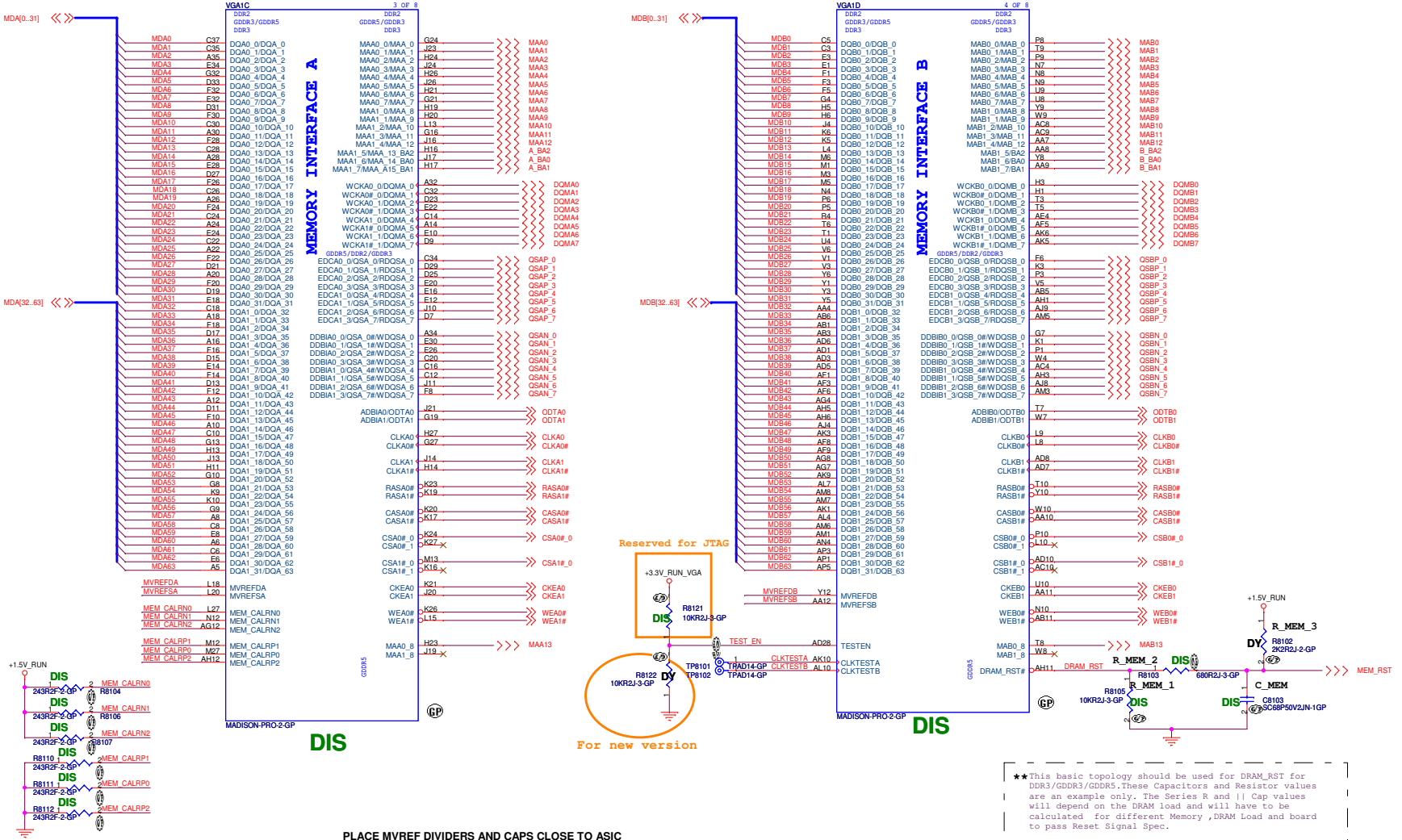
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size	Document Number	Rev
A3	Berry	X00

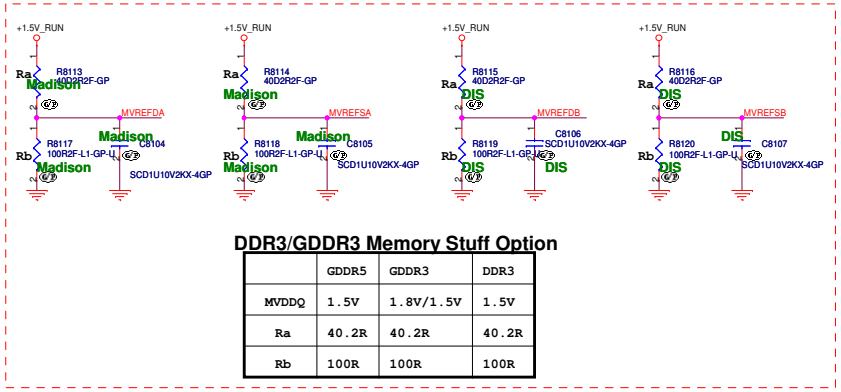
Date: Thursday, October 22, 2009 Sheet 80 of 92



**This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	0R/Short	680R
R_MEM_3	DNI	DNI
C_MEM	2.2nF	68pF

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size	Document Number	Rev
C	Berry	X00

Date: Thursday, October 22, 2009 Sheet 81 of 92

LVDS Interface

MEMORY ID Table

DVPDATA[0:3]	Description
1000	DDR3 Samsung-K4W1G1646E-HC12 (800MHz)
0000	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz)

DVPDATA[0:3] Default:Pull down

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode
TESTEN	"1" (PU)	"1" (PU)
JTAG_TRST#	"0" (PD)	"1" (PU)
JTAG_TCK	CLK	"1" (PU)
JTAG_TMS	"1" (PU)	"1" (PU)

MEM_ID Control

I2C Bus for LVDS

Straps

For new version

For new version no 27M

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

DDC1 channel for CRT

DDC2 channel for HDMI

DDC1/DDC2/DDC6 have 5V-tolerant

+3.3V tolerant

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

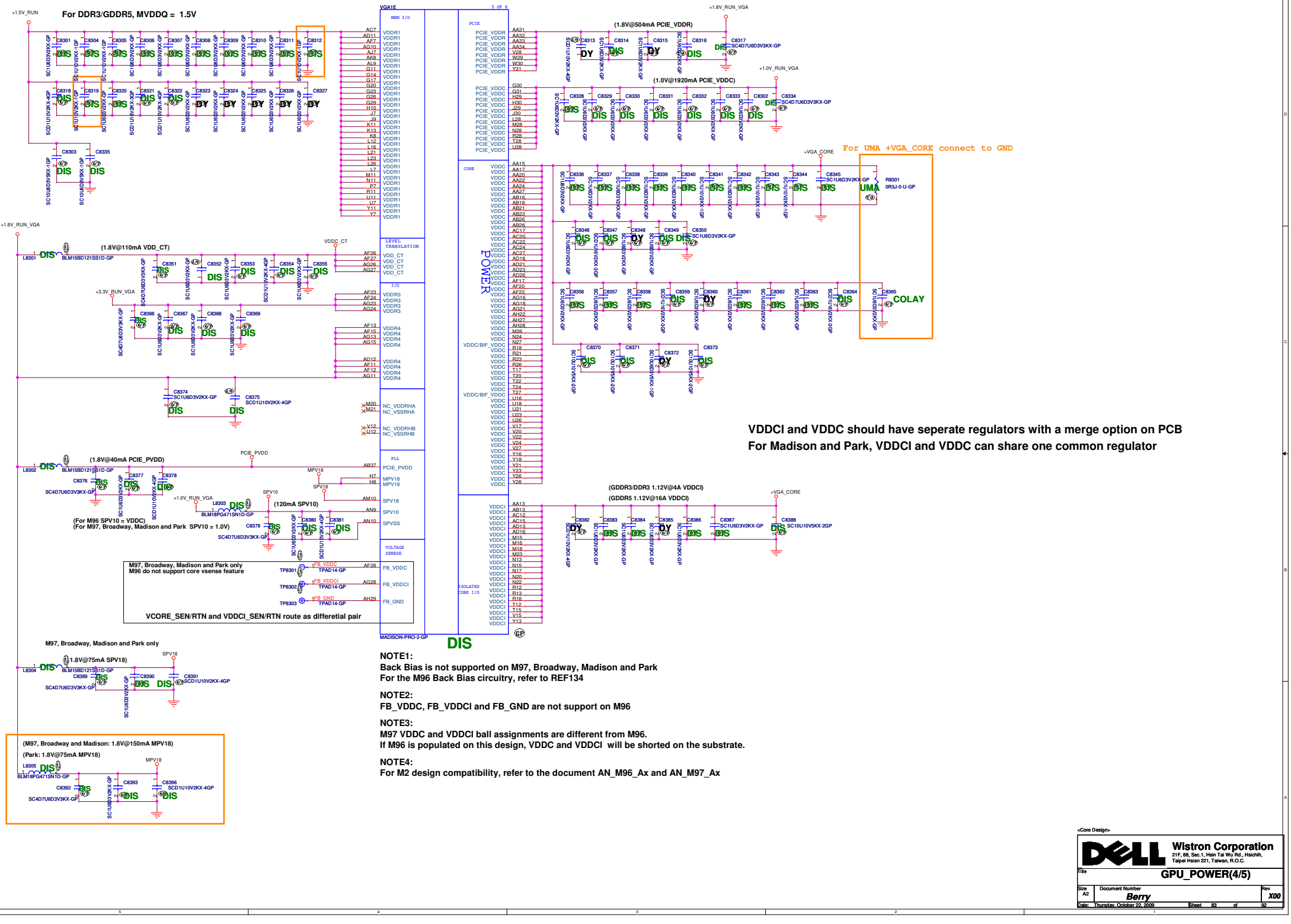
<Core Design>

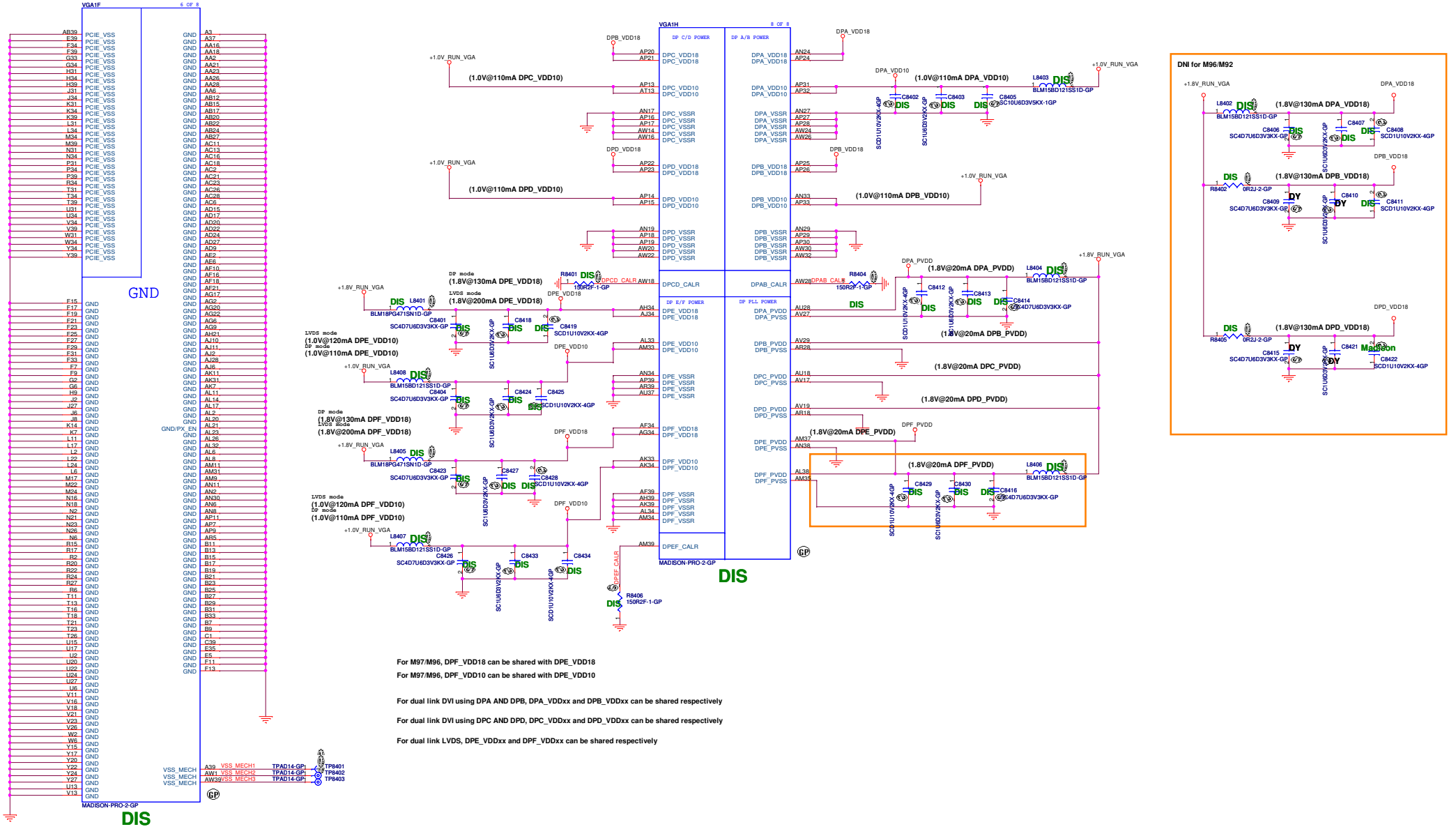
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

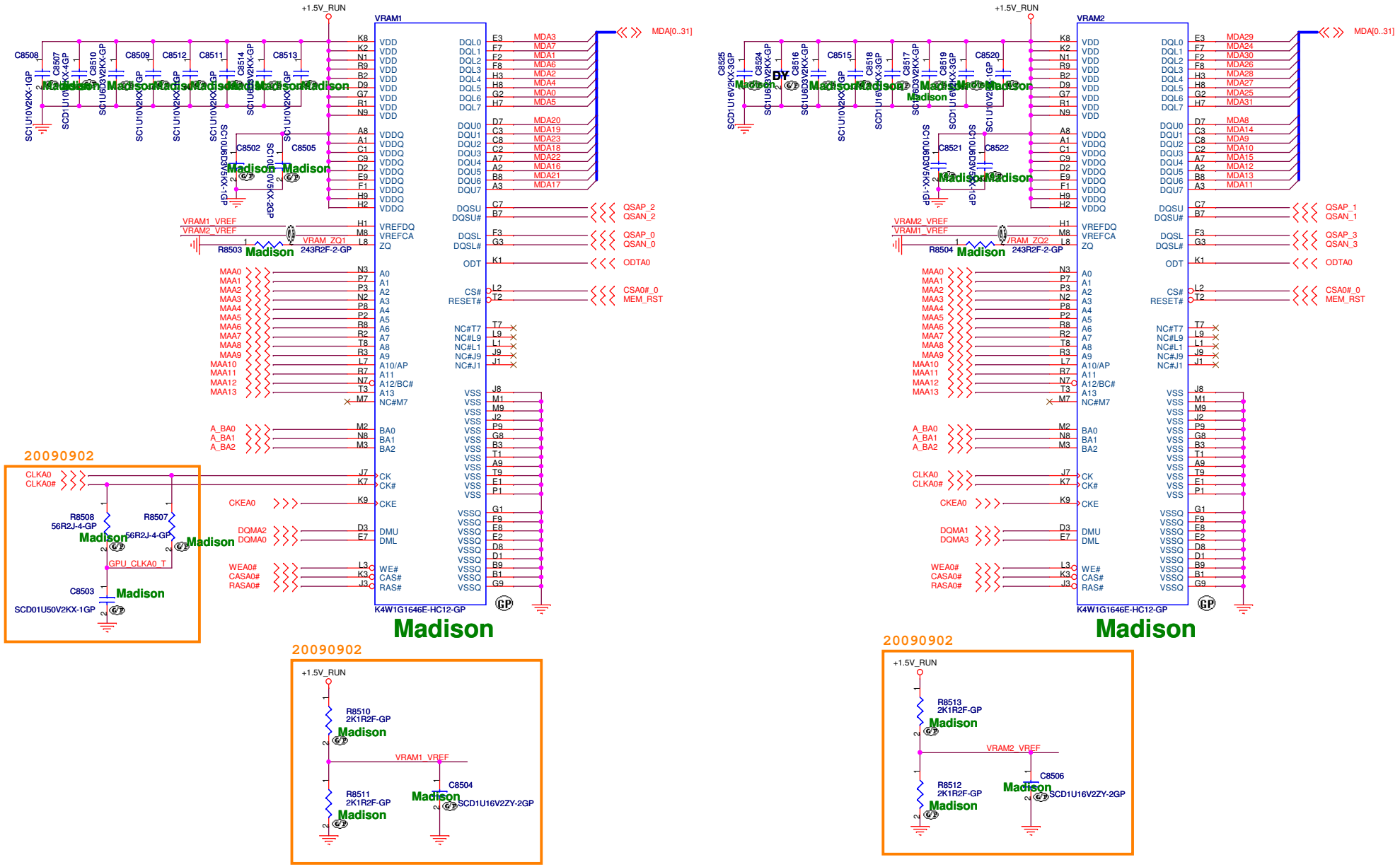
Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: Berry | Rev: X00

Date: Thursday, October 22, 2009 | Sheet 82 of 92


For DDR3/GDDR5, MVDDQ = 1.5V
VGA1E
MADISON-PRO-2-GP
POWER
DIS
For UMA +VGA_CORE connect to GND
UMA
COLAY
VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator
(1.8V@504mA PCIE_VDDR)
(1.0V@1920mA PCIE_VDDC)
(1.8V@110mA VDD_CT)
(1.8V@40mA PCIE_PVDD)
(120mA SPV10)
(For M96 SPV10 = VDDC)
(For M97, Broadway, Madison and Park SPV10 = 1.0V)
M97, Broadway, Madison and Park only
M96 do not support core vsense feature
VCORE_SEN/RTN and VDDCI_SEN/RTN route as differetial pair
(GDDR3/DDR3 1.12V@4A VDDCI)
(GDDR5 1.12V@16A VDDCI)
M97, Broadway, Madison and Park only
(1.8V@75mA SPV18)
(M97, Broadway and Madison: 1.8V@150mA MPV18)
(Park: 1.8V@75mA MPV18)
NOTE1:
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134
NOTE2:
FB_VDDC, FB_VDDCI and FB_GND are not support on M96
NOTE3:
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.
NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU_POWER(4/5)
Size A2
Document Number Berry
Rev X00
Date: Thursday, October 22, 2009
Sheet 83 of 92


VGA1F
6 OF 8
GND
MADISON-PRO-2-GP
DIS
VGA1H
8 OF 8
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
(1.0V@110mA DPC_VDD10)
(1.0V@110mA DPA_VDD10)
(1.0V@110mA DPD_VDD10)
(1.0V@110mA DPB_VDD10)
(1.8V@130mA DPE_VDD18)
(1.8V@200mA DPE_VDD18)
(1.0V@120mA DPE_VDD10)
(1.0V@110mA DPE_VDD10)
(1.8V@130mA DPF_VDD18)
(1.8V@200mA DPF_VDD18)
(1.0V@120mA DPF_VDD10)
(1.0V@110mA DPF_VDD10)
(1.8V@20mA DPA_PVDD)
(1.8V@20mA DPB_PVDD)
(1.8V@20mA DPC_PVDD)
(1.8V@20mA DPD_PVDD)
(1.8V@20mA DPE_PVDD)
(1.8V@20mA DPF_PVDD)
DNI for M96/M92
(1.8V@130mA DPA_VDD18)
(1.8V@130mA DPB_VDD18)
(1.8V@130mA DPD_VDD18)
For M97/M96, DPF_VDD18 can be shared with DPE_VDD18
For M97/M96, DPF_VDD10 can be shared with DPE_VDD10
For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively
For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively
For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU_DPPWR/GND(5/5)
Size
A2
Document Number
Berry
Rev
X00
Date: Tuesday, October 20, 2009
Sheet 84 of 92



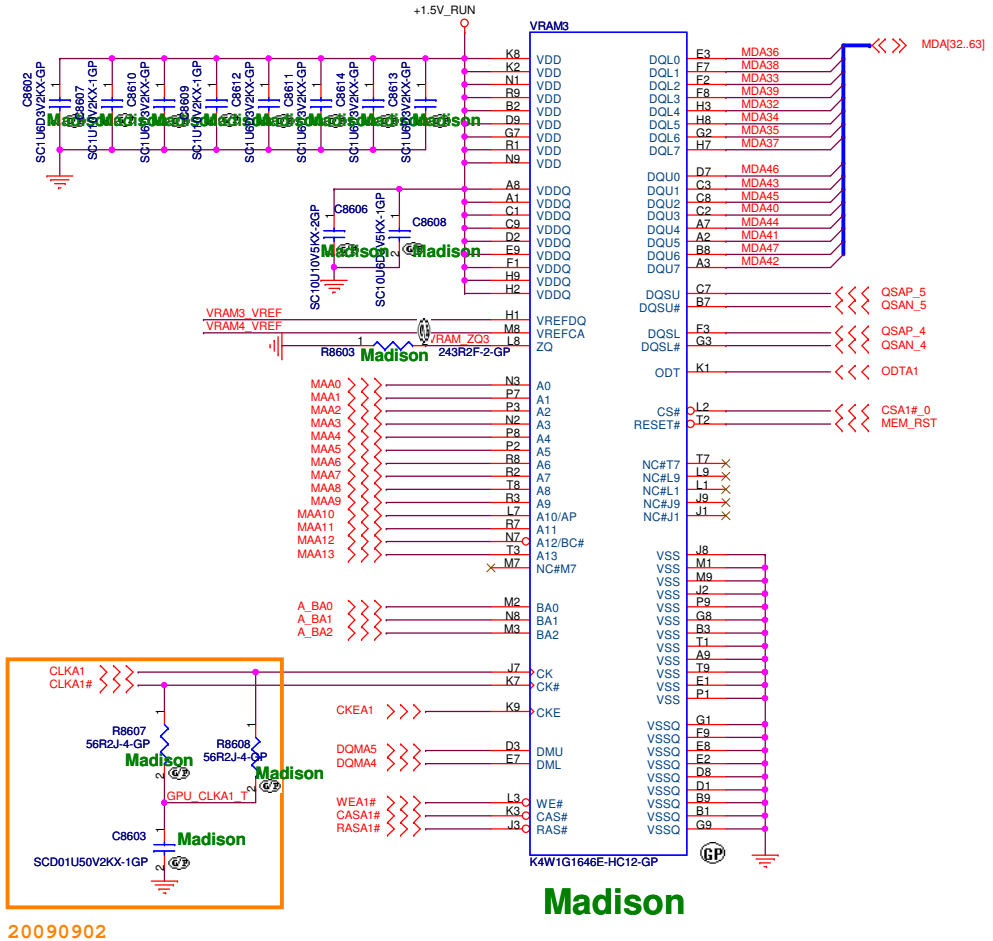
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

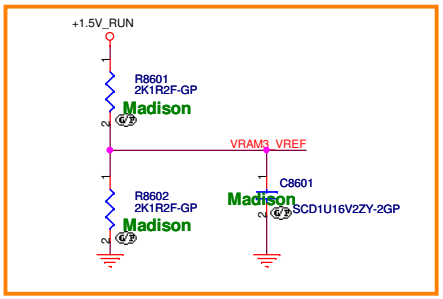
Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
Custom	Berry	X00

Date: Thursday, October 22, 2009 Sheet 85 of 92



20090902



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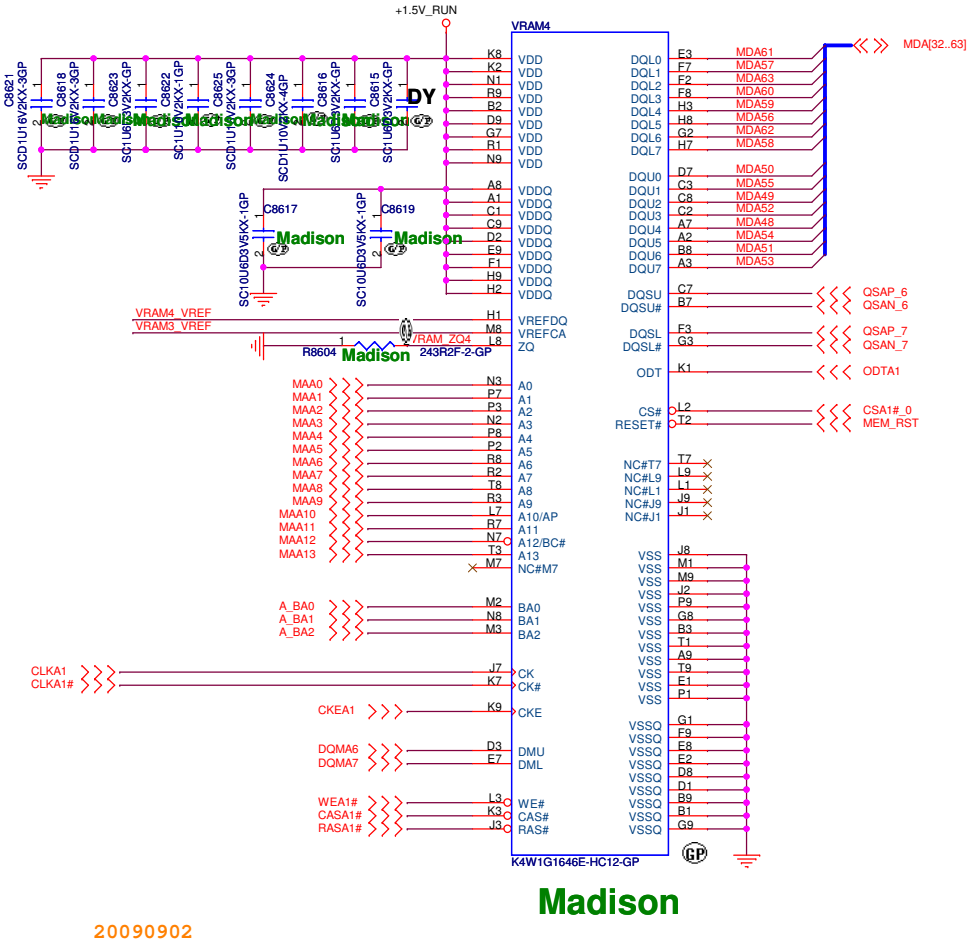

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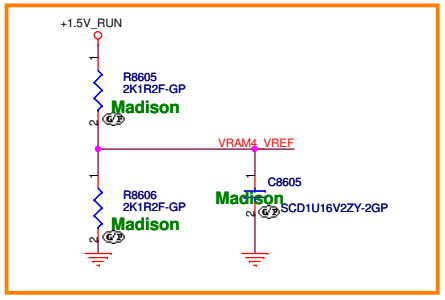


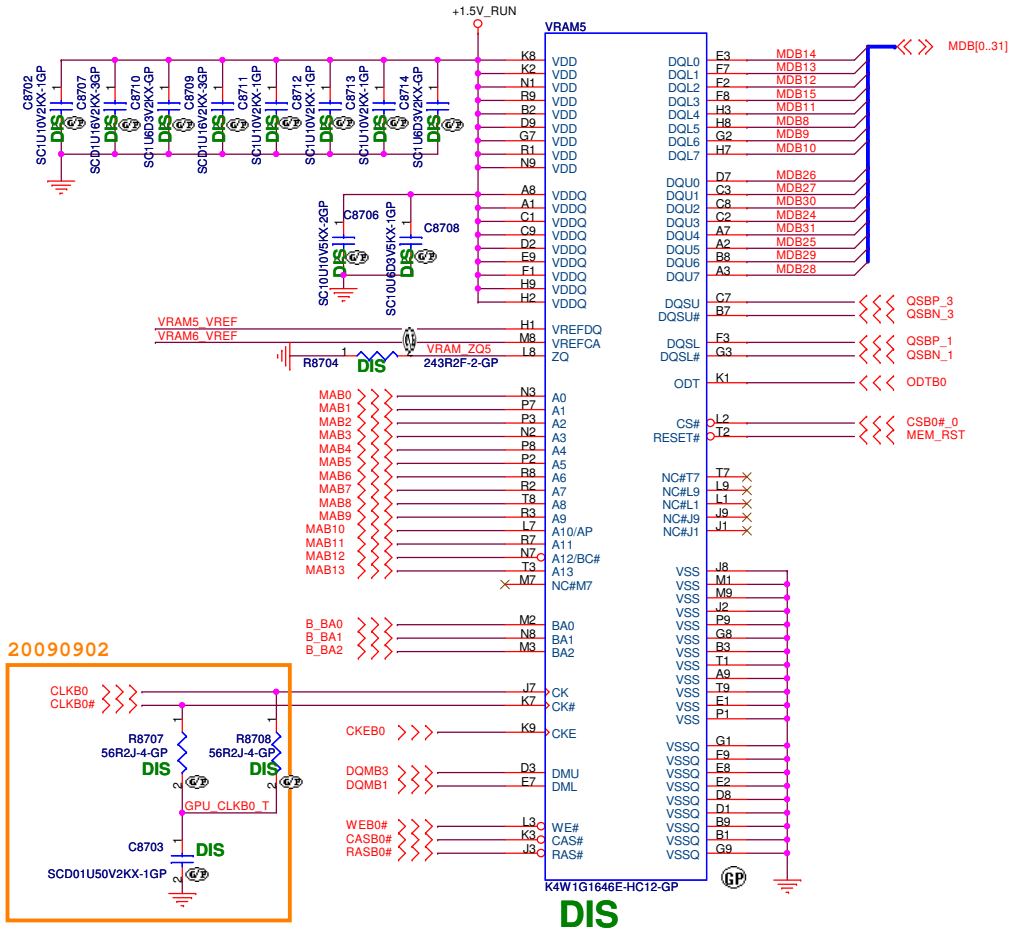
<Core Design>

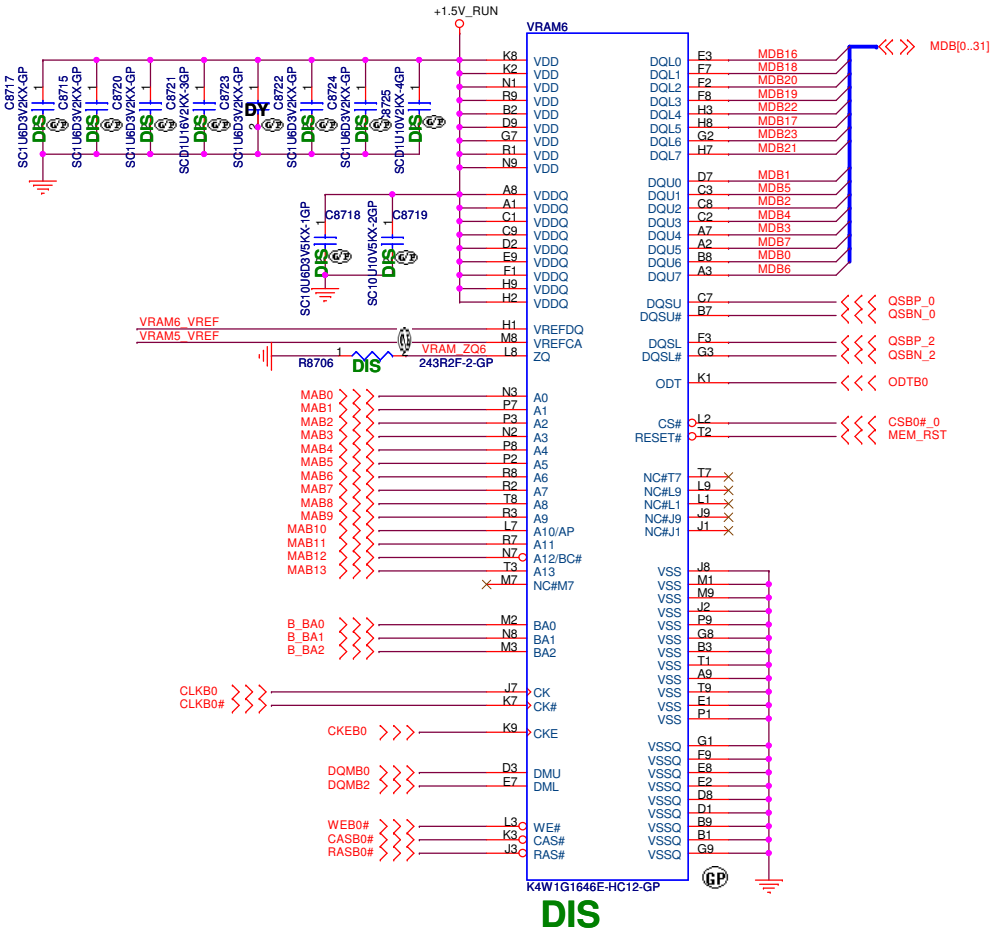
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

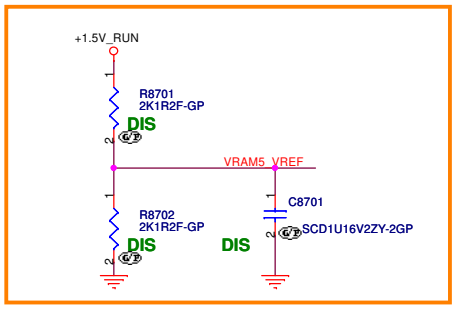
Title: GPU-VRAM3,4 (2/4)

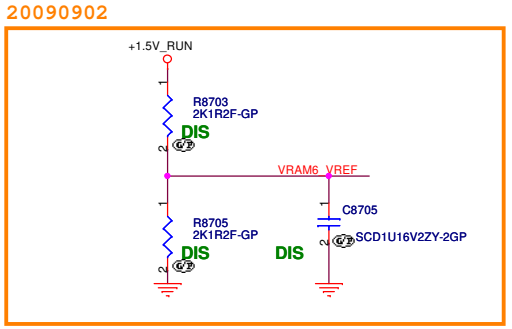
Size	Document Number	Rev
Custom	Berry	X00

Date: Thursday, October 22, 2009 Sheet 86 of 92









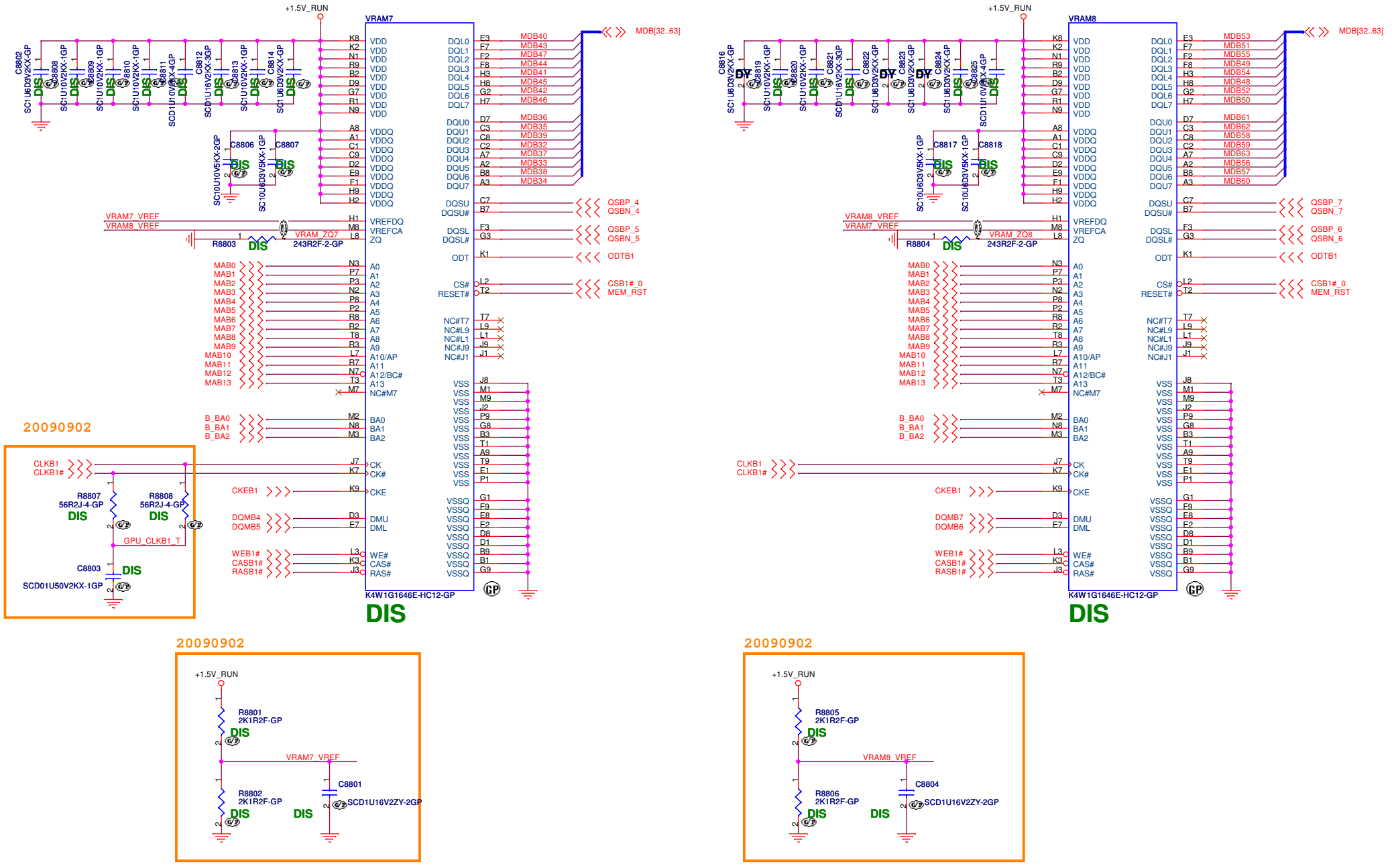
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size: A3 | Document Number: Berry | Rev: X00

Date: Thursday, October 22, 2009 | Sheet 87 of 92



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

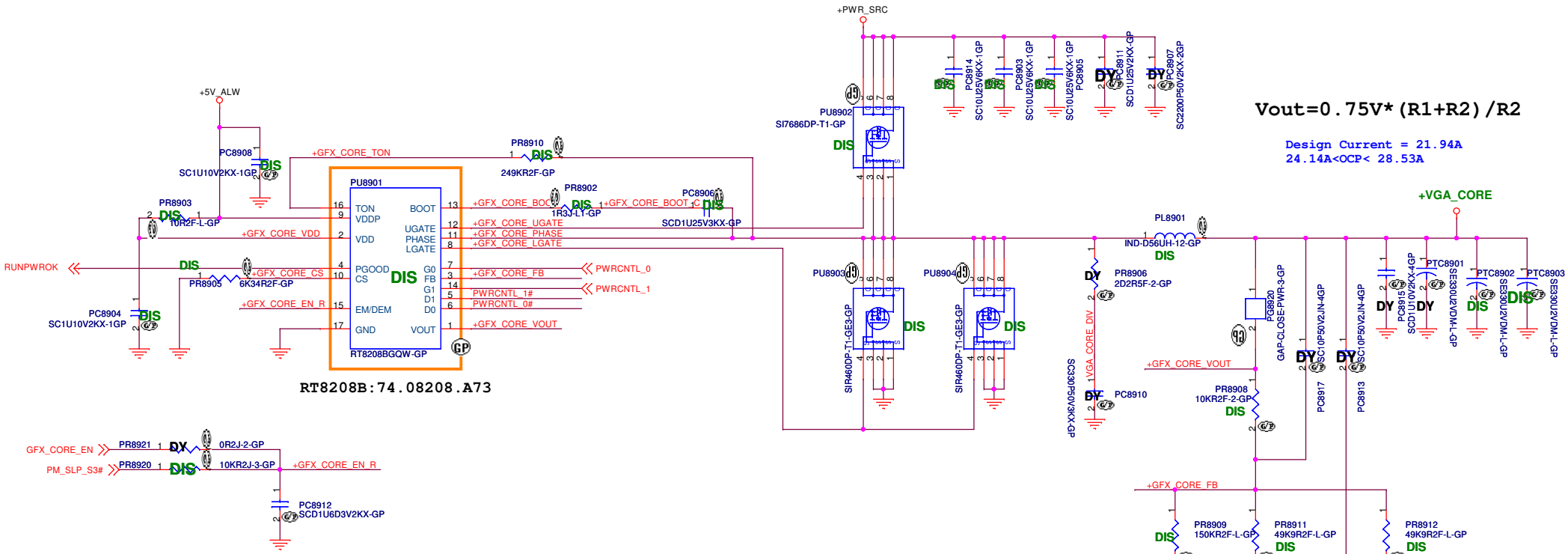
Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A3	Berry	X00

Date: Thursday, October 22, 2009 Sheet 88 of 92

SSID = Video.PWR.Regulator

RT8208BGQW for +VGA_CORE



PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.1V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

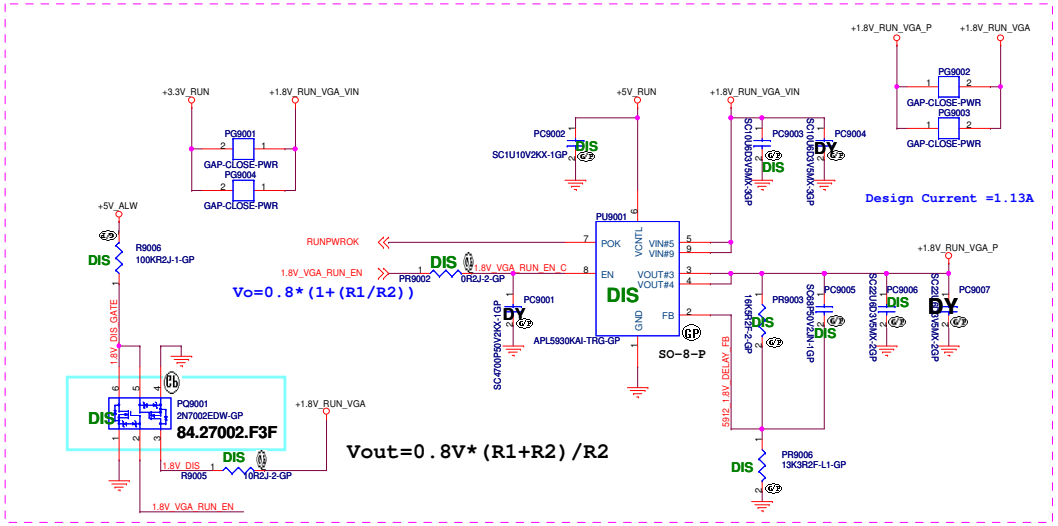
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_+VGA_CORE

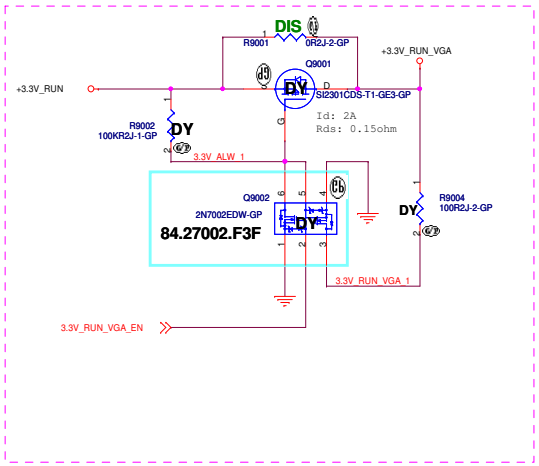
Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: X00

Date: Thursday, October 22, 2009 | Sheet 89 of 92

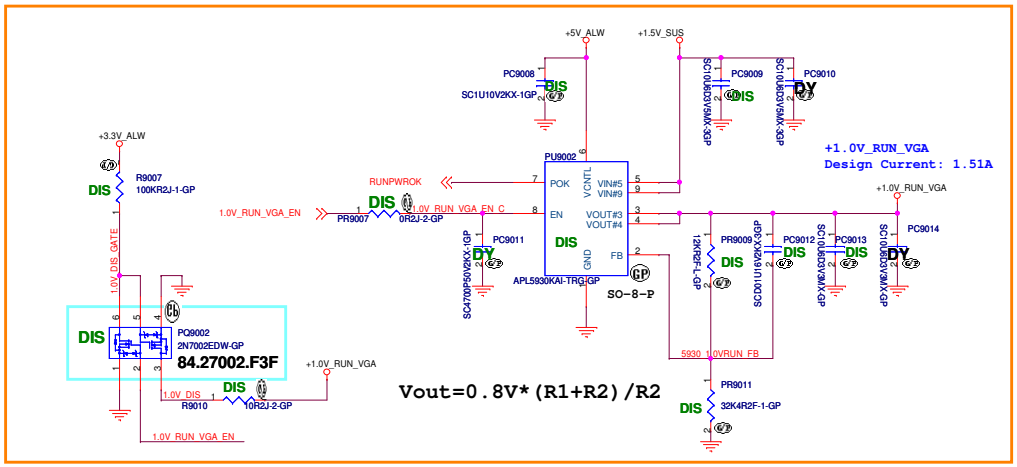
APL5930 for +1.8V_RUN_VGA



+3.3V_RUN_VGA



APL5930KAI for +1.0V_RUN_VGA



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

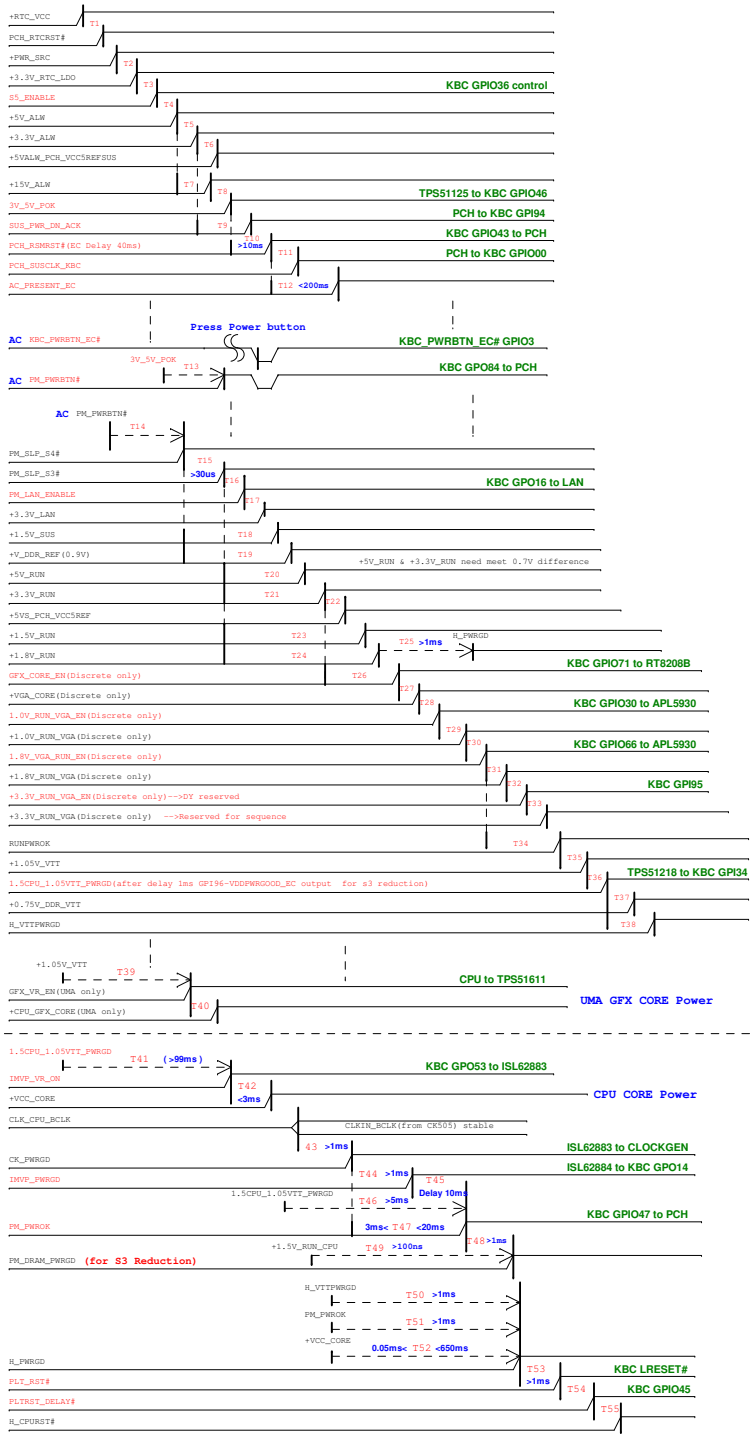
Size	Document Number	Rev
C	Berry	X00

Date: Thursday, October 22, 2009 Sheet 90 of 92

D15 Intel-Power Up Sequence

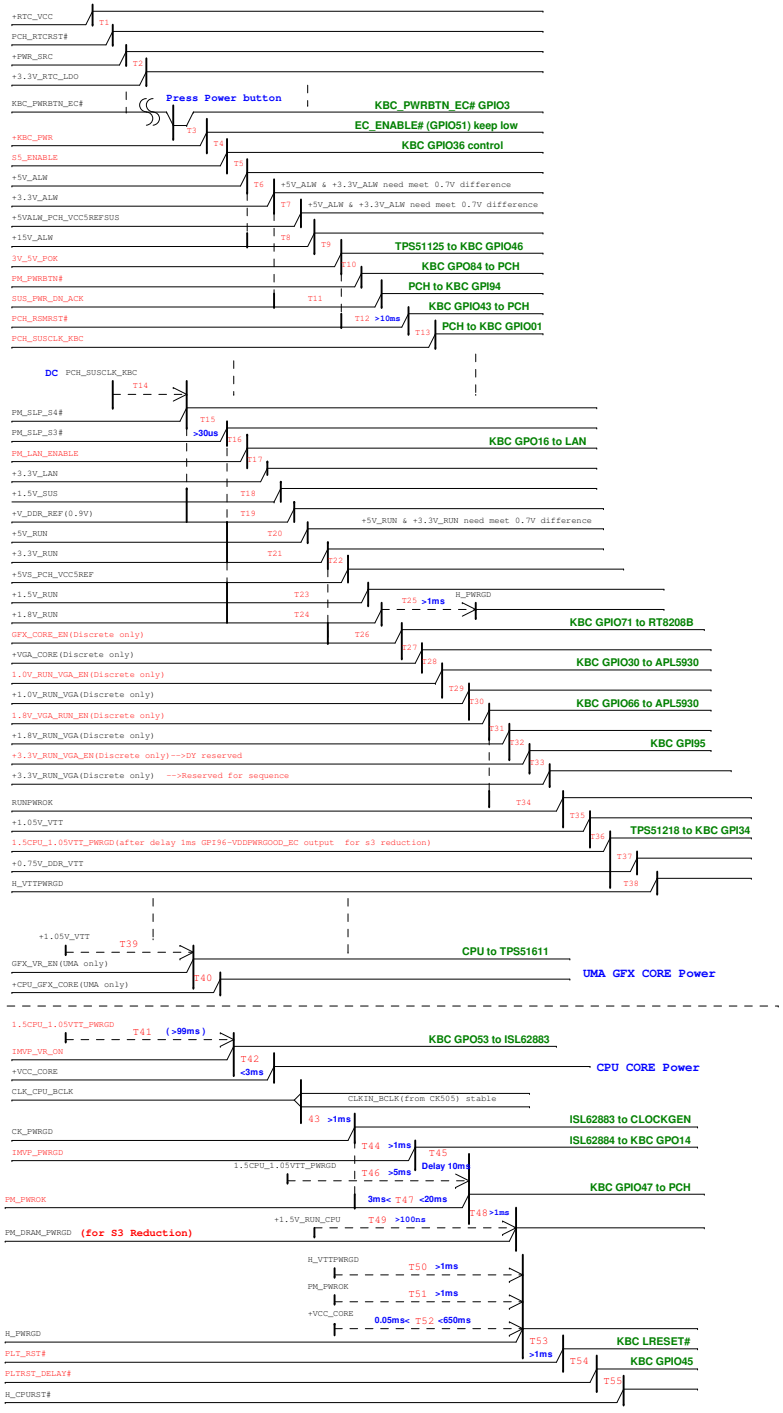
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size: A1 | Document Number: Berry | Rev: X00

Date: Tuesday, October 28, 2008 | Sheet 51 of 56

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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