1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-02-15

SCHEM,MLB_KEPLER_2PHASE,J31

FRB & RISK RAMP 02/15/12

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9585	1	SCHEM,MLB_KEPLER_2PHASE,J31	SCH	CRITICAL	
820-3330	1	PCBF,MLB_KEPLER_2PHASE,J31	PCB	CRITICAL	

DRAWING ABBREV=DRAWING TITLE=MLB

LAST_MODIFIED=Wed Feb 15 20:30:03 2012

DRAWING TITLE: SCHEM,MLB_KEPLER,J31

Apple Inc.

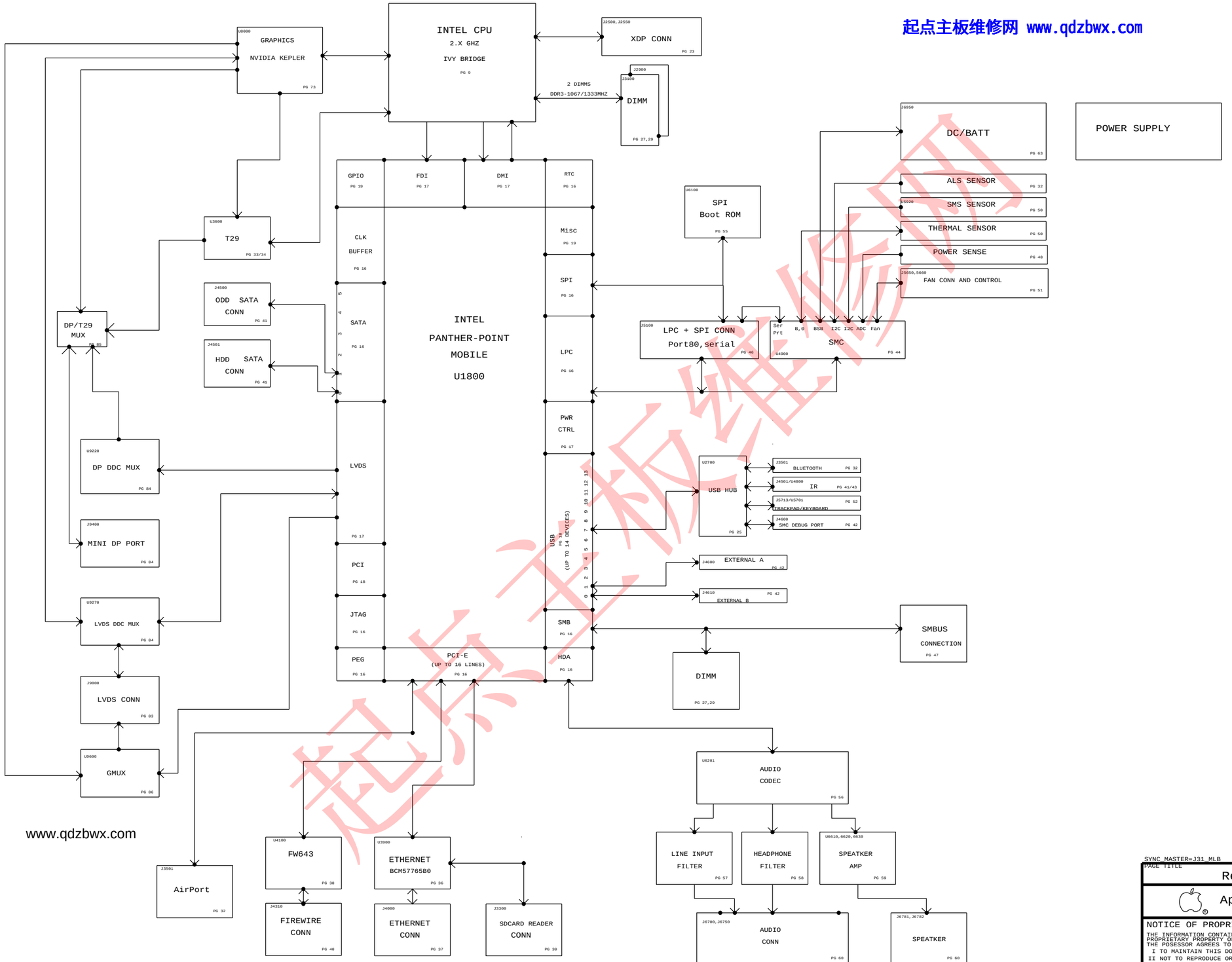
DRAWING NUMBER: 051-9585 | SIZE: D

REVISION: 3.0.0

BRANCH:

PAGE: 1 OF 132

SHEET: 1 OF 105



SYNC_MASTER=J31_MLB SYNC_DATE=04/19/2011

PAGE TITLE

Revision History

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

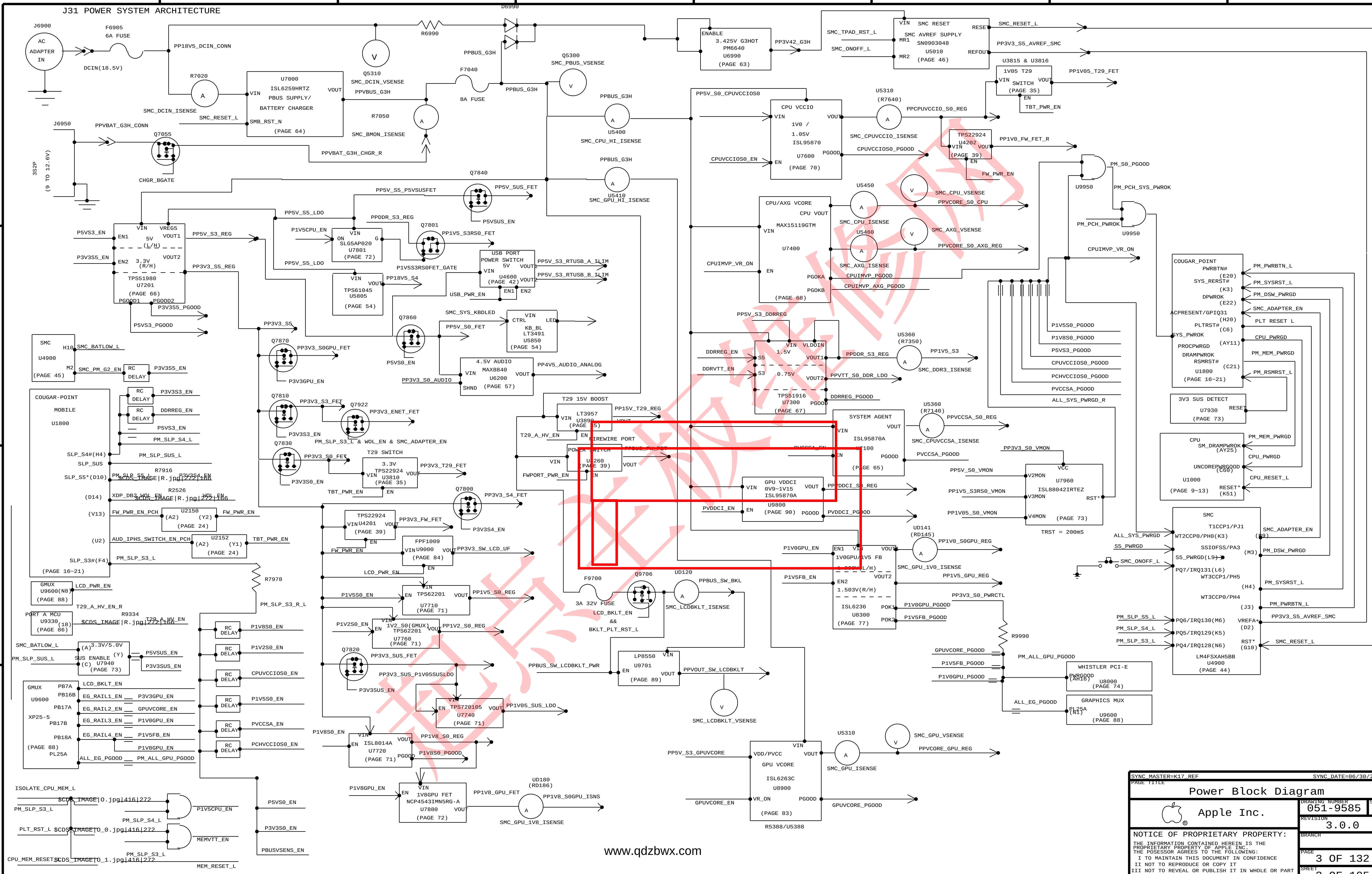
REVISION 3.0.0

BRANCH

PAGE 2 OF 132

SHEET 2 OF 105

J31 POWER SYSTEM ARCHITECTURE



SYNC_MASTER=K17_REF	SYNC_DATE=06/30/2009
PAGE TITLE	Power Block Diagram
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 3 OF 132
	SHEET 3 OF 105

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Revision History

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 4 OF 132

SHEET 4 OF 105

BOM VARIANTS - FSB

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3860	PCBA,MLB_2P,FSB,2.3,FOX,512_HYN,REN,J31,F327	J31_CMNPTS,SODIMM:FOXCONN,CPU:2_3GHZ,FB_512_HYNIX,FET:REN,DEVEL_BOM,GPUDEC:EXP,EEEE:F327
639-3861	PCBA,MLB_2P,FSB,2.3,MOL,512_SAM,FAIR,J31,F32C	J31_CMNPTS,SODIMM:MOLEX,CPU:2_3GHZ,FB_512_SAMSUNG,FET:FAIR,DEVEL_BOM,GPUDEC:EXP,EEEE:F32C
639-3862	PCBA,MLB_2P,FSB,2.6,MOL,1G_HY,FAIR,J31,F325	J31_CMNPTS,SODIMM:MOLEX,CPU:2_6GHZ,FB_1G_HYNIX_A_DIE,FET:FAIR,DEVEL_BOM,GPUDEC:EXP,EEEE:F325
639-3863	PCBA,MLB_2P,FSB,2.6,FOX,1G_SAM,REN,J31,F324	J31_CMNPTS,SODIMM:FOXCONN,CPU:2_6GHZ,FB_1G_SAMSUNG,FET:REN,DEVEL_BOM,GPUDEC:EXP,EEEE:F324
639-3864	PCBA,MLB_2P,FSB,2.7,FOX,1G_HY,REN,J31,F328	J31_CMNPTS,SODIMM:FOXCONN,CPU:2_7GHZ,FB_1G_HYNIX_A_DIE,FET:REN,DEVEL_BOM,GPUDEC:EXP,EEEE:F328
639-3865	PCBA,MLB_2P,FSB,2.7,MOL,1G_SAM,FAIR,J31,F329	J31_CMNPTS,SODIMM:MOLEX,CPU:2_7GHZ,FB_1G_SAMSUNG,FET:FAIR,DEVEL_BOM,GPUDEC:EXP,EEEE:F329
607-9557	CMN PTS,PCBA,MLB_KEPLER,J31	J31_COMMON
085-4620	J31 MLB_KEP_2P DEVELOPMENT BOM	J31_DEVEL:PVT

SUB BOMS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-4620	1	J31 MLB_KEP_2P DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9557	1	CMN PTS,PCBA,MLB_KEP_2P,J31	CMNPTS	CRITICAL	J31_CMNPTS

BOM GROUPS

BOM GROUP	BOM OPTIONS
J31_COMMON	ALTERNATE,COMMON,J31_COMMON1,J31_COMMON2,J31_PROGPARTS,J31_PROGPARTS1,UVGLUE_J31,J31_PVT
J31_COMMON1	CPUMEM_S0,RAMCFG_SLOT,USBHUB2513B,HUB_3NONREM,SMC_PACKAGE:PROD,MOJO:YES,TBTHV:P15V,SKIP_5V3V3:AUDIBLE
J31_COMMON2	BTPWR:S4,TPAD:Z2,T29:YES,TBTBST:Y,SDRV_PD,SDRVI2C:MCU,T29_DP_HPD:ALL_OR,LPCPLUS_R:YES,MEM_VDD_SEL:GPIO15,GPU:2P
J31_PROGPARTS	GMUX_PROG,IR_PROG,TPAD_PROG:FSB,ENETROM_PROG:FSB,T29ROM:PROG,T29MCU:PROG
J31_PROGPARTS1	SMC_PROG:RR,BOOTROM_PROG:FSB
J31_PVT	VREF:PROD,XDP,XDP_CPU:BPM,BKLT:PROD,LOADISNS:NO,XWLOADISNS:NO
J31_DEVEL:ENG	DDRVREF_DAC,VREF:ENG_M3,IVB_PPT_XDP,GMUX_JTAG_CONN,LPCPLUS_CONN:YES,BKLT:ENG,S0PGOOD_ISL,CPURIPPLE_ENG,LOADISNS:YES,XWLOADISNS:YES,DEBUG_ADC
J31_DEVEL:FSB	DDRVREF_DAC,VREF:ENG_M3,IVB_PPT_XDP,LPCPLUS_CONN:YES,BKLT:PROD,S0PGOOD_ISL,LOADISNS:YES,XWLOADISNS:NO
J31_DEVEL:PVT	LPCPLUS_CONN:YES,XDP_CONN_CPU
IVB_PPT_XDP	XDP,XDP_CONN_PCH,XDP_CONN_CPU,XDP_CPU:BPM,XDP_PCH

BOM GROUP	BOM OPTIONS
VREF:PROD	VREFDQ:M1_M3,VREFCA:LDO
VREF:ENG_M3	VREFDQ:M1_M3,VREFCA:LDO_DAC
VREF:ENG_LDO	VREFDQ:M1_DAC,VREFCA:LDO_DAC

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4266	1	IC,CPU,IVB,S,RBMP,PRQ,E1,2.3,45W,4+2,1.2,GM,BGA	U1000	CRITICAL	CPU:2_3GHZ
337S4267	1	IC,CPU,IVB,S,RBMM,PRQ,E1,2.6,45W,4+2,1.25,GM,BGA	U1000	CRITICAL	CPU:2_6GHZ
337S4268	1	IC,CPU,IVB,S,RBMK,PRQ,E1,2.7,45W,4+2,1.25,GM,BGA	U1000	CRITICAL	CPU:2_7GHZ
337S4269	1	IC,PCH,PPT,C1,SL3BC,PRQ,BGB28MM77	U1800	CRITICAL	
337S4239	1	IC,GPU,NV GK107-GTX-QS-A2	U8000	CRITICAL	
338S1072	1	IC,ASSP,LIGHTRIDGE,PRQ,S LJJY,FCBGA,15X15MM,C1	U3600	CRITICAL	T29:YES
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
353S3055	1	IC,PI3VED9212,X2 DISPLAYPORT 2:1 MUX,QFN	U9390	CRITICAL	
333S0619	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,G-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_512_SAMSUNG
333S0620	4	IC,SDRAM,GDDR5,32MX32,1.5GHz,VEGA 44NM,B-DIE	U8400,U8450,U8500,U8550	CRITICAL	FB_512_HYNIX
333S0631	4	IC,SGRAM,GDDR5,64MX32,5GBPS,D-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_SAMSUNG
333S0630	4	IC,SGRAM,GDDR5,64MX32,5GBPS,A-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX_A_DIE
333S0609	4	IC,SGRAM,GDDR5,64MX32,4.2GBPS,M-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX_M_DIE
725-1479	1	MLB LOCTITE UV EB CPU,PCH,T29,GPU,K91	UV_GLUE_,J31	CRITICAL	UVGLUE_J31
516S0806	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,FOXCONN	J3100	CRITICAL	SODIMM:FOXCONN
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:FOXCONN
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:MOLEX
516-0245	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,MOLEX	J2900	CRITICAL	SODIMM:MOLEX
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:HYBRID
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:HYBRID
376S0964	2	RJK0225	Q7330,Q8360	CRITICAL	FET:REN
376S0965	2	RJK0225	Q7335,Q8361	CRITICAL	FET:REN
376S0979	2	FDMC8225	Q7330,Q8360	CRITICAL	FET:FAIR
376S0874	2	FDMC8202S	Q7335,Q8361	CRITICAL	FET:FAIR
376S0826	1	FET,N-CH,30V,3.6MOHM,LF,HF,RJK0332DPB	Q7630	CRITICAL	FET:REN
376S0617	1	FET,N-CH,30V,30A,6.7MOHM,RJK0305DPB	Q7635	CRITICAL	FET:REN
376S0917	1	FET,N-CH,30V,3.6MOHM,LF,HF,FDMS8333S	Q7630	CRITICAL	FET:FAIR
376S1018	1	FET,N-CH,30V,14A,13MOHM,FDMS8349	Q7635	CRITICAL	FET:FAIR

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F327]	CRITICAL	EEEE:F327
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F32C]	CRITICAL	EEEE:F32C
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F325]	CRITICAL	EEEE:F325
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F324]	CRITICAL	EEEE:F324
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F328]	CRITICAL	EEEE:F328
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F329]	CRITICAL	EEEE:F329

Alternate Parts

(Alternate) (Primary)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
353S2805	353S2603		ALL	Fairchild wafer option
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
353S3085	353S1658		ALL	ST Micro alt to LT
376S0972	376S0612		ALL	RDHM alt to Toshiba N-FET
376S0855	376S0613		ALL	SSHMA alt to Toshiba dual N-FET
138S0676	138S0691		ALL	Murata alt to Samsung cap
138S0652	138S0648		ALL	Samsung / Murata alt for Taiyo Yuden
138S0681	138S0638		ALL	Taiyo Yuden alt for Samsung
152S0685	152S0796		ALL	Delta/Vishay/TDK alt for Cyntec
376S0977	376S0859		ALL	Diodes alt for Rohm
353S2592	353S3199		ALL	anon semi semi semi nxp mc in n/mach rm mm mc
335S0550	335S0777		ALL	add 4M Byte as alternative to 2M
371S0709	371S0652		ALL	NXP alternate for pin diodes
138S0671	138S0673		ALL	Taiyo Yuden alt for Murata 10 uF caps
514-0788	514-0671		ALL	Acon (with Tolmar) alt to Acon
155S0578	155S0367		ALL	Taps Yuden alt to Murata inductors
138S0681	138S0638		ALL	Taps Yuden alt to Samsung caps.
138S0671	138S0673		ALL	Taps Yuden alt to Murata caps.
155S0625	155S0559		ALL	Murata alt to TDK cm mode filter
376S0777	376S0761		ALL	ABB alternate to Fairchild
157S0084	157S0055		ALL	TDK alternate for ethernet transformer
353S3312	353S3055		ALL	NXP alternate to Percom SP Mux
376S0958	376S0953		ALL	For Q7350, Fairchild alt to Ren.
376S1053	376S0604		ALL	Radar 10567726
371S0713	371S0558		ALL	Radar 10562580
128S0311	128S0329		ALL	Radar 10357464
127S0134	127S0111		ALL	Radar 10360888
127S0127	127S0090		ALL	Radar 10360328
197S0431	197S0432		ALL	RADAR 10670230
197S0434	197S0343		ALL	RADAR 10739227
197S0435	197S0343		ALL	RADAR 10739227

Programmables - All Builds

PSOC

341S3099	1	IC,TP PSOC,K9x,DVT,PVT,J31	U5701	CRITICAL	TPAD_PROG:PROTO0
341S3351	1	IC,TP PSOC,PROTO1,J31	U5701	CRITICAL	TPAD_PROG:PROTO1
341S3227	1	IC,TP PSOC,PROTO2,PROTO3-ZZ,J31	U5701	CRITICAL	TPAD_PROG:PROTO3
341S3489	1	IC,TP PSOC,PIB,J31	U5701	CRITICAL	TPAD_PROG:PIB
341S3522	1	IC,TP PSOC,FSB,J31	U5701	CRITICAL	TPAD_PROG:FSB

341S2830	1	IC,CPLD,LATTICE,GMUX,K91/K91F,J31	U9600	CRITICAL	GMUX_PROG
336S0042	1	IC,PLD,LATTICE,LFXP2-5E-5,132 BALL CSBGA	U9600	CRITICAL	GMUX_BLANK
341S2384	1	IR,ENCORE II,CYYC63833-LFXC	U4800	CRITICAL	IR_PROG
341S3430	1	IC,T29 EEPROM,LR,J30/J31	U3690	CRITICAL	T29ROM:PROG
335S0777	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	T29ROM:BLANK
341S3365	1	IC,PROGRMD,LPC1112A,T29 PORT MCU,PVT,HVQFN25,J31	U9330	CRITICAL	T29MCU:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
335S0852	1	IC,GPUROM,J31,BLANK	U8701	CRITICAL	GPUROM:BLANK

ETHERNET ROM

335S0663	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENETROM_BLANK
341S3096	1	IC,ENET ROM,1MBIT,DVT,PVT,K90I/K91x,J31	U3990	CRITICAL	ENETROM_PROG:PROTO3
341S3492	1	IC,PRGRMD,ENET,SPI ROM,FSB,J30/J31	U3990	CRITICAL	ENETROM_PROG:FSB

SMC

338S0895	1	IC,SMC,MSB/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S3258	1	IC,SMC,DEVELOPMENT-PROTO0,J31	U4900	CRITICAL	SMC_PROG:PROTO0
341S3294	1	IC,SMC,DEVELOPMENT-PROTO1,J31	U4900	CRITICAL	SMC_PROG:PROTO1
341S3401	1	IC,EXTERNAL,PROTO2,PROTO3,J31	U4900	CRITICAL	SMC_PROG:PROTO3
341S3481	1	IC,SMC,EXTERNAL,PIB,V2.1A83,A3,J31	U4900	CRITICAL	SMC_PROG:A3_PIB
341S3296	1	IC,SMC,EXTERNAL,FSB,V2.1A143,J31	U4900	CRITICAL	SMC_PROG:FSB
341S3297	1	IC,SMC,EXTERNAL,RISKRAMP,J31	U4900	CRITICAL	SMC_PROG:RR

EFI ROM

335S0740	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341S3257	1	IC,EFI,ROM,PROTO0, J31	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S3344	1	IC,EFI,ROM,PROTO1, J31	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3419	1	IC,EFI,ROM,PROTO2,J31	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S3454	1	IC,EFI,ROM,PROTO3,J31	U6100	CRITICAL	BOOTROM_PROG:PROTO3
341S3510	1	IC,EFI,ROM,POST-PIB,J31	U6100	CRITICAL	BOOTROM_PROG:PIB2
341S3476	1	IC,EFI,ROM,FSB,J31	U6100	CRITICAL	BOOTROM_PROG:FSB

PD Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
452-1708	2	SCR,M1.6X0.35X6.0,D4,HO.3,BLK,M97	SODIMM_SCREW1,SODIMM_SCREW2	CRITICAL	
452-1708	2	SCR,M1.6X0.35X6.0,D4,HO.3,BLK,M97	SODIMM_SCREW3,SODIMM_SCREW4	CRITICAL	
725-1607	1	INSULATOR,GPU,J31	GPU_INSULATOR	CRITICAL	

SYNC_MASTER=K17_REF SYNC_DATE=05/28/2009

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 5 OF 132

SHEET 5 OF 105

Functional Test Points

J5650 (LEFT FAN CONN)
FUNC_TEST
PP5V_S0 6 7
FAN_LT_PWM 52
FAN_LT_TACH 52
GND

J5660 (RIGHT FAN CONN)
PP5V_S0 6 7
FAN_RT_PWM 52
FAN_RT_TACH 52
GND

J6780 (MIC CONN)
BI_MIC_N 62 63 101
BI_MIC_SHIELD 62 63
BI_MIC_P 62 63 101
GND
2 TPs

J5100
GND
6 TPs
PP5V_S0 6 7
PP3V42_G3H 6 7

J6781 & J6782 (SPEAKERS CONN)
SPKRCONN_L_OUT_P 61 62 101
SPKRCONN_L_OUT_N 61 62 101
SPKRCONN_R_OUT_P 61 62 101
SPKRCONN_R_OUT_N 61 62 101
SPKRCONN_S_OUT_P 61 62 101
SPKRCONN_S_OUT_N 61 62 101
GND
4 TPs

J9000 (LVDS CONN)
PP3V3_SW_LCD 85
PP3V3_S0 6 7 101
PPVOUT_S0_LCDBKLT 8 85 104
2 TP needed
3 TP needed
LVDS_DDC_CLK 85 86
LVDS_DDC_DATA 85 86
LVDS_CONN_A_DATA_P<0> 85 86 100
LVDS_CONN_A_DATA_N<0> 85 86 100
LVDS_CONN_A_DATA_P<1> 85 86 100
LVDS_CONN_A_DATA_N<1> 85 86 100
LVDS_CONN_A_DATA_P<2> 85 86 100
LVDS_CONN_A_DATA_N<2> 85 86 100
LVDS_CONN_A_CLK_F_P 85 100
LVDS_CONN_A_CLK_F_N 85 100
LVDS_CONN_B_DATA_P<0> 85 86 100
LVDS_CONN_B_DATA_N<0> 85 86 100
LVDS_CONN_B_DATA_P<1> 85 86 100
LVDS_CONN_B_DATA_N<1> 85 86 100
LVDS_CONN_B_DATA_P<2> 85 86 100
LVDS_CONN_B_DATA_N<2> 85 86 100
LVDS_CONN_B_CLK_F_P 85 100
LVDS_CONN_B_CLK_F_N 85 100
LED_RETURN_1 85 90
LED_RETURN_2 85 90
LED_RETURN_3 85 90
LED_RETURN_4 85 90
LED_RETURN_5 85 90
LED_RETURN_6 85 90
GND
8 TPs

J4500 (SATA ODD CONN)
PP5V_SW_ODD 41
4 TPs
SMC_ODD_DETECT 41 45
SATA_ODD_D2R_C_P 41 95
SATA_ODD_D2R_C_N 41 95
SATA_ODD_R2D_P 41 95
SATA_ODD_R2D_N 41 95
GND
7 TPs

J4501 (SATA HDD CONN)
PP5V_S0_HDD_FLT 41
4 TPs
SATA_HDD_R2D_P 41 95
SATA_HDD_R2D_N 41 95
SATA_HDD_D2R_C_N 41 95
SATA_HDD_D2R_C_P 41 95
GND
8 TPs

IR_RX_OUT 6 41 44
PP5V_S3_IR_R 6 41
SSD_OOBD2R_L 41
SSD_OOBR2D_L 41

J5815 (KBD BACKLIGHT CONN)
KBDLED_ANODE 54
2 TPs
SMC_KDBLED_PRESENT_L 54
GND

J3501 & J3502 (AIRPORT/BT/CAMERA CONN)
PCIE_AP_R2D_P 32 96
PCIE_AP_R2D_N 32 96
PCIE_CLK100M_AP_CONN_P 32 101
PCIE_CLK100M_AP_CONN_N 32 101
AP_CLKREQ_O_L 32
PCIE_WAKE_L 17 24 32
WIFI_EVENT_L 32 45 46
AP_RESET_CONN_L 32
PP3V3_WLAN 32
6 TPs
PP5V_S3_ALSCAMERA_F 32
SMBUS_SMC_2_S3_SDA 6 45 48 99
SMBUS_SMC_2_S3_SCL 6 45 48 99
USB_CAMERA_CONN_P 32 95
USB_CAMERA_CONN_N 32 95
GND
10 TPs

PP3V3_S3R54_BT_F 32
USB_BT_CONN_P 32 95
USB_BT_CONN_N 32 95

J6950 (BAT CONN)
SYS_DETECT_L 6 64

J5800 (IPD FLEX CONN)
PP18V5_Z2 54
PP3V3_S4 6 7
PP5V_S5_CUMULUS 54
Z2_HOST_INTN 53 54
Z2_MOSI 53 54
Z2_CS_L 53 54
Z2_DEBUG3 53 54
Z2_MISO 53 54
Z2_BOOST_EN 54
Z2_SCLK 53 54
Z2_CLKIN 53 54
Z2_KEY_ACT_L 53 54
Z2_RESET 53 54
PSOC_F_CS_L 53 54
PICKB_L 53 54
PSOC_MOSI 53 54
PSOC_MISO 53 54
SMBUS_SMC_2_S3_SCL 6 45 48 99
SMBUS_SMC_2_S3_SDA 6 45 48 99
GND
2 TPs needed

J6900 (DC POWER CONN)
ADAPTER_SENSE 64
PP18V5_DCIN_FUSE 64
2 TPs
GND
2 TPs

J6950 (MAIN BATT CONN)
PPVBAT_G3H_CONN 64 65
3 TPs
SMBUS_SMC_5_G3_SCL 6 45 48 99
SMBUS_SMC_5_G3_SDA 6 45 48 99
SYS_DETECT_L 6 64
GND
7 TPs

J6955 (BAT LED CONN)
PP3V42_G3H 6
3 TPs
SMBUS_SMC_5_G3_SDA 6 45 48 99
SMBUS_SMC_5_G3_SCL 6 45 48 99
SMC_BIL_BUTTON_L 45 46 64
SMC_LID_R 6 64
GND
7 TPs

J5713 (KEY BOARD CONN)
PP3V3_S4 6 7
PP3V42_G3H 6 7
WS_KBD1 53
WS_KBD2 53
WS_KBD3 53
WS_KBD4 53
WS_KBD5 53
WS_KBD6 53
WS_KBD7 53
WS_KBD8 53
WS_KBD9 53
WS_KBD10 53
WS_KBD11 53
WS_KBD12 53
WS_KBD13 53
WS_KBD14 53
WS_KBD15_CAP 53
WS_KBD16_NUM 53
WS_KBD17 53
WS_KBD18 53
WS_KBD19 53
WS_KBD20 53
WS_KBD21 53
WS_KBD22 53
WS_KBD23 53
WS_KBD_ONOFF_L 53
WS_LEFT_SHIFT_KBD 53
WS_LEFT_OPTION_KBD 53
WS_CONTROL_KBD 53
GND

J6950 (BIL CABLE CONN)
PP5V_S3_IR_R 6 41
SMC_LID_R 6 64
IR_RX_OUT 6 41 44
SYS_LED_ANODE 41 46
GND

POWER RAILS
FUNC_TEST
PM_SLP_S3_L 17 26 45 74
PP0V75_S0_DDRVTT 7
PP1V05_S0 7
PP1V05_S0GPU 7
PP1V0_FW_FWPHY 7
PP1V2_ENET 7
PP1V2_S0 7
PP1V5_S3 7
PP1V8_S0 7
PP3V3_ENET 7
PP3V3_FW_FWPHY 7
PP3V3_S0 6 7 101
PP3V3_S3 7
PP3V3_S5 7 101
PP3V3_S5_AVREF_SMC 45 46
PP3V42_G3H 6 7
PP5V_S0 6 7
PP5V_S3 7
PPBUS_G3H 7
PPDCIN_G3H 7
PPVCORE_GPU 7
PPVCORE_S0_CPU 7
PPVP_FW 7
PPVTTDDR_S3 7

FUNC_TEST
BKLT_EN 90
ISSP_SCLK_P1_1 8
ISSP_SDATA_P1_0 8
LCD_BKLT_PWM 89 90
LPCPLUS_GPIO 19 47
LPCPLUS_RESET_L 24 47
LPC_AD<0..3> 16 45 47 89 96
LPC_CLK33M_LPCPLUS 24 47 96
LPC_FRAME_L 16 45 47 89 96
LPC_PWRDWN_L 17 45 47
LPC_SERIRQ 16 45 47
PM_CLKRUN_L 17 45 47
PM_SYSRST_L 17 24 45
SMC_ONOFF_L 45 46 53
SMC_RESET_L 45 46 47 65
SMC_RX_L 45 46 47
SMC_TCK 45 46 47
SMC_TDI 45 46 47
SMC_TDO 45 46 47
SMC_TMS 45 46 47
SMC_ROMBOOT 46 47
SMC_TX_L 45 46 47
SPIROM_USE_MLB 19 47 56
SPI_ALT_CLK 47
SPI_ALT_CS_L 47
SPI_ALT_MISO 47
SPI_ALT_MOSI 47
SYS_LED_ANODE_R 41

NO_TEST=TRUE
TBT_R2D_C_P<1..0>
TBT_R2D_C_N<1..0>

TBTDPA_ML_P<3..0>
TBTDPA_ML_N<3..0>
DP_TBTSNK0_AUXCH_C_P 33 81 98
DP_TBTSNK0_AUXCH_C_N 33 81 98
DP_TBTSNK0_AUXCH_P 33 98
DP_TBTSNK0_AUXCH_N 33 98
DP_TBTSNK0_ML_C_P<3..0> 33 81 98
DP_TBTSNK0_ML_C_N<3..0> 33 81 98
DP_TBTSNK0_ML_P<3..0> 33 98
DP_TBTSNK0_ML_N<3..0> 33 98
DP_TBTSNK1_AUXCH_C_P 33 81 98
DP_TBTSNK1_AUXCH_C_N 33 81 98
DP_TBTSNK1_AUXCH_P 33 98
DP_TBTSNK1_AUXCH_N 33 98
DP_TBTSNK1_ML_C_P<3..0> 33 81 98
DP_TBTSNK1_ML_C_N<3..0> 33 81 98
DP_TBTSNK1_ML_P<3..0> 33 98
DP_TBTSNK1_ML_N<3..0> 33 98
TP_DP_TBTSRC_AUXCH_CN 6 33
TP_DP_TBTSRC_AUXCH_CP 6 33
DP_TBTSRC_ML_C_P<3..0> 6 33
DP_TBTSRC_ML_C_N<3..0> 6 33
DP_SDRVA_ML_C_P<0> 87 98
DP_SDRVA_ML_C_N<0> 87 98
DP_SDRVA_ML_C_P<2> 87 98
DP_SDRVA_ML_C_N<2> 87 98
DP_SDRVA_ML_P<0> 87 98
DP_SDRVA_ML_N<0> 87 98
DP_SDRVA_ML_P<2> 87 98
DP_SDRVA_ML_N<2> 87 98
TP_TBT_PCIE_RESET0_L 6 33
TP_TBT_PCIE_RESET1_L 6 33
TP_TBT_PCIE_RESET2_L 6 33
TP_TBT_PCIE_RESET3_L 6 33
PEG_D2R_C_P<7..0> 75 93
PEG_D2R_C_N<7..0> 75 93
PEG_R2D_P<7..0> 75 92 93
PEG_R2D_N<7..0> 75 92 93

NC NO_TESTS
NO_TEST
TP_FW643_SCIFCLK 38
TP_FW643_SCIFDAIN 38
TP_FW643_SCIFDOUT 38
TP_FW643_SCIFRC 38
TP_FW643_SDA 38
TP_FW643_SE 38
TP_FW643_SM 38
TP_FW643_CE 38
TP_FW643_FW620_L 38
TP_FW643_JASI_EN 38
DMI_S2N_N<1> 25 74
DMI_S2N_P<1> 25 74
FDI_DATA_N<1> 9 17 93
FDI_DATA_P<1> 9 17 93
FDI_FSYNC<1..0> 9 17 93
FDI_LSYNC<1..0> 9 17 93
FDI_INT 9 17 93
FDI_DATA_N<7..4> 9 17 93
FDI_DATA_P<7..4> 9 17 93

TP_FW643_VAUX_ENABLE 38
TP_FW643_VBUF 38
TP_FW643_TCK 38
TP_FW643_TDO 38
TP_FW643_TMS 38
TP_SMC_P10
TP_P7_7 53
TP_PSOC_SCL 53
TP_PSOC_SDA 53
TP_SMC_P24
DC_TEST_BH1_BG2 12
DC_TEST_BH3_BJ2 12
TP_USB_HUB1_OCS1
TP_USB_HUB1_PRTPWR1
TP_USB_HUB2_OCS1
TP_USB_HUB2_PRTPWR1
TP_DC_TEST_A62 12
TP_DC_TEST_D65 12

ICT Test Points

CPU NO_TESTs
NO_TEST
TP_CPU_RSVD<65..62> NC_TP_CPU_RSVD<65..62>
TP_CPU_RSVD<58..45> NC_TP_CPU_RSVD<58..45>
TP_CPU_RSVD<43..32> NC_TP_CPU_RSVD<43..32>
TP_CPU_RSVD<27..26> NC_TP_CPU_RSVD<27..26>
TP_CPU_RSVD<24..15> NC_TP_CPU_RSVD<24..15>
TP_CPU_RSVD<2..1> NC_TP_CPU_RSVD<2..1>
TP_CPU_RSVD_NCTF<8..5> NC_TP_CPU_RSVD_NCTF<8..5>

NC NO_TESTS
NO_TEST
17 TP_CRT_IG_BLUE NC_CRT_IG_BLUE
17 TP_CRT_IG_GREEN NC_CRT_IG_GREEN
17 TP_CRT_IG_RED NC_CRT_IG_RED
17 TP_CRT_IG_DDC_CLK NC_CRT_IG_DDC_CLK
17 TP_CRT_IG_DDC_DATA NC_CRT_IG_DDC_DATA
17 TP_CRT_IG_HSYNC NC_CRT_IG_HSYNC
17 TP_CRT_IG_VSYNC NC_CRT_IG_VSYNC
17 TP_LVDS_IG_CTRL_CLK NC_LVDS_IG_CTRL_CLK
17 TP_LVDS_IG_CTRL_DATA NC_LVDS_IG_CTRL_DATA
17 TP_PCH_LVDS_VBG NC_PCH_LVDS_VBG

16 TP_HDA_SDIN1 NC_HDA_SDIN1
16 TP_HDA_SDIN2 NC_HDA_SDIN2
16 TP_HDA_SDIN3 NC_HDA_SDIN3
33 6 TP_DP_TBTSRC_AUXCH_CP TP_DP_TBTSRC_AUXCH_CP 6 33
33 6 TP_DP_TBTSRC_AUXCH_CN TP_DP_TBTSRC_AUXCH_CN 6 33
33 6 TBT_PCIE_RESET0_L NC_TBT_PCIE_RESET0_L
33 6 TP_TBT_PCIE_RESET1_L NC_TBT_PCIE_RESET1_L
33 6 TBT_PCIE_RESET2_L NC_TBT_PCIE_RESET2_L
33 6 TP_TBT_PCIE_RESET3_L NC_TBT_PCIE_RESET3_L
33 TP_TBT_MONDC0 NC_TBT_MONDC0
33 TP_TBT_MONDC1 NC_TBT_MONDC1
33 TP_TBT_MONOBSP NC_TBT_MONOBSP
33 TP_TBT_MONOBSN NC_TBT_MONOBSN
33 6 TP_DP_TBTSRC_ML_CP<0..3> NC_DP_TBTSRC_ML_CP<0..3>
33 6 TP_DP_TBTSRC_ML_CN<0..3> NC_DP_TBTSRC_ML_CN<0..3>

NO_TEST
TP_AUD_GPIO_2
TP_AUD_GPIO_1
TP_AUD_LDO1_N
TP_AUD_LDO1_P
TP_BKL_FAULT 90
TP_SPI_DESCRIPTOR_OVERRIDE_L
TP_XDPPCH_HOOK2 23
TP_XDPPCH_HOOK3 23
TP_GMUX_PL68 89
CPUIMVP_BOOT1 6 69 70
CPUIMVP_BOOT2 6 69 70
CPUIMVP_UGATE2 6 69 70
TP_LVDS_S0_PCH_VCCAPLLEXP 20

TP_PCI_PME_L NC_PCI_PME_L
TP_PCI_CLK33M_OUT3 NC_PCI_CLK33M_OUT3
16 TP_PCIE_CLK100M_PE4N NC_PCIE_CLK100M_PE4N
16 TP_PCIE_CLK100M_PE4P NC_PCIE_CLK100M_PE4P
16 TP_PCIE_CLK100M_PE5N NC_PCIE_CLK100M_PE5N
16 TP_PCIE_CLK100M_PE5P NC_PCIE_CLK100M_PE5P
TP_PCIE_CLK100M_PE6N NC_PCIE_CLK100M_PE6N
TP_PCIE_CLK100M_PE6P NC_PCIE_CLK100M_PE6P
TP_PCIE_CLK100M_PE7N NC_PCIE_CLK100M_PE7N
TP_PCIE_CLK100M_PE7P NC_PCIE_CLK100M_PE7P
53 TP_PSOC_P1_3 NC_PSOC_P1_3
TP_SATA_B_D2RN NC_SATA_B_D2RN
TP_SATA_B_D2RP NC_SATA_B_D2RP
TP_SATA_B_R2D_CN NC_SATA_B_R2D_CN
TP_SATA_B_R2D_CP NC_SATA_B_R2D_CP
16 TP_SATA_D_D2RN NC_SATA_D_D2RN
16 TP_SATA_D_D2RP NC_SATA_D_D2RP
16 TP_SATA_D_R2D_CN NC_SATA_D_R2D_CN
16 TP_SATA_D_R2D_CP NC_SATA_D_R2D_CP
16 TP_SATA_E_D2RN NC_SATA_E_D2RN
16 TP_SATA_E_D2RP NC_SATA_E_D2RP
16 TP_SATA_E_R2D_CN NC_SATA_E_R2D_CN
16 TP_SATA_E_R2D_CP NC_SATA_E_R2D_CP
16 TP_SATA_F_D2RN NC_SATA_F_D2RN
16 TP_SATA_F_D2RP NC_SATA_F_D2RP
16 TP_SATA_F_R2D_CN NC_SATA_F_R2D_CN
16 TP_SATA_F_R2D_CP NC_SATA_F_R2D_CP
16 TP_SMC_P41 NC_SMC_P41

PCH ALIASES
NC_LPC_DREQ0_L TP_LPC_DREQ0_L 16
16 TP_CLINK_CLK NC_CLINK_CLK
16 TP_CLINK_DATA NC_CLINK_DATA
16 TP_CLINK_RESET_L NC_CLINK_RESET_L
16 TP_PCIE_CLK100M_PEBN NC_PCIE_CLK100M_PEBN
16 TP_PCIE_CLK100M_PEBP NC_PCIE_CLK100M_PEBP

NO_TEST
NC NO_TESTS
NC_SMC_FAN_3_TACH
NC_SMC_FAN_3_CTL
NC_SMC_FAN_2_TACH
NC_SMC_FAN_2_CTL
NC_FW2_TPBP 40
NC_FW2_TPBN 40
NC_FW2_TPBIAS 40
NC_FW2_TPAP 40
NC_FW2_TPAN 40
NC_FW0_TPBP 40
NC_FW0_TPBN 40
NC_FW0_TPAP 40
NC_ESTARLDO_EN
NC_ALS_GAIN

38 TP_FW643_AVREG NC_FW643_AVREG
39 TP_FW643_TDI NC_FW643_TDI
TP_DP_IG_C_HPD NC_DP_IG_C_HPD
TP_DP_IG_C_CTRL_CLK NC_DP_IG_C_CTRL_CLK
TP_DP_IG_C_CTRL_DATA NC_DP_IG_C_CTRL_DATA
17 TP_DP_IG_C_MLP<3..0> NC_DP_IG_C_MLP<3..0>
17 TP_DP_IG_C_MLN<3..0> NC_DP_IG_C_MLN<3..0>
TP_DP_IG_C_AUXP NC_DP_IG_C_AUXP
TP_DP_IG_C_AUXN NC_DP_IG_C_AUXN
17 TP_DP_IG_D_HPD NC_DP_IG_D_HPD
17 TP_DP_IG_D_CTRL_CLK NC_DP_IG_D_CTRL_CLK
17 TP_DP_IG_D_CTRL_DATA NC_DP_IG_D_CTRL_DATA
17 TP_DP_IG_D_MLP<3..0> NC_DP_IG_D_MLP<3..0>
17 TP_DP_IG_D_MLN<3..0> NC_DP_IG_D_MLN<3..0>
17 TP_DP_IG_D_AUXP NC_DP_IG_D_AUXP
17 TP_DP_IG_D_AUXN NC_DP_IG_D_AUXN
17 TP_SDVO_TVCLKINN NC_SDVO_TVCLKINN
17 TP_SDVO_TVCLKINP NC_SDVO_TVCLKINP
17 TP_SDVO_STALLN NC_SDVO_STALLN
17 TP_SDVO_STALLP NC_SDVO_STALLP
17 TP_SDVO_INTN NC_SDVO_INTN
17 TP_SDVO_INTP NC_SDVO_INTP
TP_GPU_BUFRST_L NC_GPU_BUFRST_L
TP_GPU_GSTATE<0> NC_GPU_GSTATE<0>
TP_GPU_GSTATE<1> NC_GPU_GSTATE<1>
TP_GPU_MIOA_D<9..0> NC_GPU_MIOA_D<9..0>
TP_GPU_MIOA_DE NC_GPU_MIOA_DE

9 TP_LVDS_IG_B_CLKN NC_LVDS_IG_B_CLKN
9 TP_LVDS_IG_B_CLKP NC_LVDS_IG_B_CLKP
9 TP_LVDS_IG_BKL_PWM NC_LVDS_IG_BKL_PWM

MEM_A_BA<2..0> 11 27 94
MEM_A_CKE<1..0> 11 27 94
MEM_A_CLK_N<1..0> 11 27 94
MEM_A_CLK_P<1..0> 11 27 94
MEM_A_CS_L<1..0> 11 27 94
MEM_A_ODT<1..0> 11 27 94
MEM_A_SA<1..0> 27
MEM_A_DQ<63..0> 11 28
MEM_A_DQS_N<7..0> 11 28 94
MEM_A_DQS_P<7..0> 11 28 94
FB_A0_DQ<31..0> 77 79 100
FB_A0_A<8..0> 77 79 100
FB_A0_ABI_L 77 79 100
FB_A0_EDC<3..0> 77 79 100
FB_A0_WCLK_N<1..0> 77 79 100
FB_A0_WCLK_P<1..0> 77 79 100
FB_A0_DBI_L<3..0> 77 79 100
FB_A1_DQ<31..0> 77 79 100
FB_A1_A<8..0> 77 79 100
FB_A1_ABI_L 77 79 100
FB_A1_EDC<3..0> 77 79 100
FB_A1_WCLK_N<1..0> 77 79 100
FB_A1_WCLK_P<1..0> 77 79 100
FB_A1_DBI_L<3..0> 77 79 100
MEM_A_A<15..0> 11 27 94
MEM_A_CAS_L 11 27 94
MEM_A_RAS_L 11 27 94
MEM_A_WE_L 11 27 94
MEM_B_A<15..0> 11 29 94
MEM_B_CAS_L 11 29 94
MEM_B_RAS_L 11 29 94
MEM_B_WE_L 11 29 94

MEM_B_BA<2..0> 11 29 94
MEM_B_CKE<1..0> 11 29 94
MEM_B_CLK_N<1..0> 11 29 94
MEM_B_CLK_P<1..0> 11 29 94
MEM_B_CS_L<1..0> 11 29 94
MEM_B_ODT<1..0> 11 29 94
MEM_B_SA<1..0> 29
MEM_B_DQ<63..0> 11 28
MEM_B_DQS_N<7..0> 11 28 94
MEM_B_DQS_P<7..0> 11 28 94
FB_B0_DQ<31..0> 77 80 100
FB_B0_A<8..0> 77 80 100
FB_B0_ABI_L 77 80 100
FB_B0_EDC<3..0> 77 80 100
FB_B0_WCLK_N<1..0> 77 80 100
FB_B0_WCLK_P<1..0> 77 80 100
FB_B0_DBI_L<3..0> 77 80 100
FB_B1_DQ<31..0> 77 80 100
FB_B1_A<8..0> 77 80 100
FB_B1_ABI_L 77 80 100
FB_B1_EDC<3..0> 77 80 100
FB_B1_WCLK_N<1..0> 77 80 100
FB_B1_WCLK_P<1..0> 77 80 100
FB_B1_DBI_L<3..0> 77 80 100

NO_TEST=TRUE
CHGR_BOOT
CHGR_ICOMP_RC
CHGR_LGATE
CHGR_PHASE
CHGR_UGATE
CHGR_VCOMP
CPU_VCCSASENSE_DIV
CPUIMVP_AXG1_SNUB
CPUIMVP_AXG2_SNUB
CPUIMVP_BOOT1
CPUIMVP_BOOT1_RC
CPUIMVP_BOOT1G
CPUIMVP_BOOT1G_R
CPUIMVP_LGATE1
CPUIMVP_LGATE1G
CPUIMVP_LGATE2
CPUIMVP_LGATE2G
CPUIMVP_LGATE3
CPUIMVP_PH1_SNUB
CPUIMVP_PH2_SNUB
CPUIMVP_PH3_SNUB
CPUIMVP_PHASE1
CPUIMVP_PHASE1G
CPUIMVP_PHASE2
CPUIMVP_PHASE2G
CPUIMVP_PHASE3
CPUIMVP_SKIP
CPUIMVP_SLEW
CPUIMVP_TONA
CPUIMVP_TONB
CPUIMVP_VSW1
CPUIMVP_VSW2
CPUVCCIOS0_BOOT_RC
CPUVCCIOS0_DRVH
CPUVCCIOS0_DRVL
CPUVCCIOS0_FB
CPUVCCIOS0_LL
CPUVCCIOS0_OCSET
CPUVCCIOS0_RTN
CPUVCCIOS0_VBST
DC_TEST_B3_C2
DDRREG_DRVH
DDRREG_DRVL
DDRREG_FB
DDRREG_LL
P3V3S5_VBST
P3V42G3H_SW
P5VS3_CSP1_R
P5VS3_DRVH
P5VS3_DRVL
P5VS3_LL
P5VS3_SNUBR
P5VS3_TG
P5VS3_VBST
P5VS3_VFB1
PCHVCCIOS0_BOOT_RC
PCHVCCIOS0_DRVH
PCHVCCIOS0_DRVL
PCHVCCIOS0_FB
PCHVCCIOS0_LL
PCHVCCIOS0_OCSET
PCHVCCIOS0_VBST
PPVCORE_S0_CPU_PH1_L
PPVCORE_S0_CPU_PH2_L
PPVCORE_S0_CPU_PH3_L
VCCSASO_B00T_RC
VCCSASO_DRVL
VCCSASO_LL
VCCSASO_VBST

CPUIMVP_BOOT2
CPUIMVP_BOOT2_RC
CPUIMVP_BOOT2G
CPUIMVP_BOOT2G_RC
CPUIMVP_BOOT3
CPUIMVP_BOOT3_RC

CPUIMVP_UGATE1
CPUIMVP_UGATE1G
CPUIMVP_UGATE2
CPUIMVP_UGATE2G
CPUIMVP_UGATE3

DDRREG_TRIP
GFXIMVP_LGATE
GFXIMVP_LL_RC
GFXIMVP_PHASE
GFXIMVP_PHASE_L
GFXIMVP_UGATE
GFXIMVP_UGATE_R
GFXIMVP_VBST
GFXIMVP_VBST_R
GPUFB_BOOT_RC
GPUFB_DRVH
GPUFB_DRVL
GPUFB_LL
GPUFB_VBST
P1V05_GPU_DRVL
P1V05_GPU_DRVH
P1V05_GPU_LL
P1V05_GPU_VBST
P1V05_GPU_BOOT_RC
P1V8S0_FB
P1V8S0_SW
P3V3S5_CSP2_R
P3V3S5_DRVH
P3V3S5_DRVL
P3V3S5_LL
P3V3S5_SNUBR
P3V3S5_VFB2
P3V3S5_VBST
P3V42G3H_SW
P5VS3_CSP1_R
P5VS3_DRVH
P5VS3_DRVL
P5VS3_LL
P5VS3_SNUBR
P5VS3_VBST
P5VS3_VFB1
P5VS3G3H_BOOST
P5VS3G3H_SW

DMI_S2N_N<3>
DMI_S2N_P<3>
DMI_S2N_N<1..0>
DMI_S2N_P<1..0>
DMI_N2S_N<2..1>
DMI_N2S_P<3..1>

USB3_EXTB_RX_N
USB3_EXTB_RX_P
USB3_EXTB_RX_F_N
USB3_EXTB_RX_F_P
USB3_EXTB_TX_N
USB3_EXTB_TX_C_N
USB3_EXTB_TX_F_N
USB3_EXTB_TX_P
USB3_EXTB_TX_C_P
USB3_EXTB_TX_F_P

USB3_EXTA_RX_N
USB3_EXTA_RX_P
USB3_EXTA_RX_F_N
USB3_EXTA_RX_F_P
USB3_EXTA_TX_N
USB3_EXTA_TX_C_N
USB3_EXTA_TX_F_N
USB3_EXTA_TX_P
USB3_EXTA_TX_C_P
USB3_EXTA_TX_F_P

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010
PAGE TITLE
Functional / ICT Test
Apple Inc.
DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 7 OF 132
SHEET 6 OF 105

G3H Rails

=PPBUS_G3H → PPBUS_G3H (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.8V, MAKE_BASE=TRUE)
- =PPBUS_S0_LCDBKLT 90
- =PPBUS_S5_FWPWRSW 39
- =PPVIN_S5_HS_OTHER_ISNS_R 50
- =PPVIN_S5_HS_COMPUTING_ISNS_R 50
- =PPVIN_S5_HS_GPU_ISNS_R 50
- =PPBUS_S0_VSENSE 49
- =PPBUS_SW_TBTBST 8 35

=PPVIN_S5_HS_COMPUTING_ISNS → PPVIN_S5_HS_COMPUTING_ISNS (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.8V, MAKE_BASE=TRUE)
- =PPVIN_S0_CPUIMVP 69 70
- =PPVIN_S3_DDRREG 68
- =PPVIN_S0_CPUVCCIOS0 71
- =PPVIN_S0_CPUAXG 70
- =PPVIN_S0_VCCSAS0 66
- =PPVIN_S0_PCHVCCIOS0

=PPVIN_S5_HS_GPU_ISNS → PPVIN_S5_HS_GPU_ISNS (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.8V, MAKE_BASE=TRUE)
- =PPVIN_S0GPU_P1V5 78
- =PPVIN_S0_GFXIMVP 84
- =PPVIN_S0GPU_P1V05 78

=PPVIN_S5_HS_OTHER_ISNS → PPVIN_S5_HS_OTHER_ISNS (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.8V, MAKE_BASE=TRUE)
- =PPVIN_S5_P5VP3V3 67

=PP18V5_DCIN_CONN → PPDCIN_G3H (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=18.5V, MAKE_BASE=TRUE)
- =PPDCIN_S5_CHGR 65
- =PPDCIN_S5_VSENSE 49

=PP3V42_G3H_REG → PP3V42_G3H (MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.42V, MAKE_BASE=TRUE)
- =PP3V3_S5_LPCPLUS 47
- =PP3V3_S5_SMC 45 46 82
- =PP3V42_G3H_BIL 64
- =PP3V42_G3H_CHGR 65 74
- =PP3V42_G3H_ONEWIREPROT 64
- =PP3V42_G3H_PWRCTL 74
- =PP3V42_G3H_SMBUS_SMC_5 48
- =PP3V42_G3H_SMCUSBMUX 42
- =PP3V42_G3H_TPAD 53
- =PPVIN_S5_SMCVREF 46
- =PPVBAT_G3_SYSCLK 24
- =PP3V42_G3H_AUDIO 59

For PCH RTC Power

=PPVRTC_G3_OUT → PPVRTC_G3H (MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.42V, MAKE_BASE=TRUE)
- =PPVRTC_G3_PCH 16 17 20

5V Rails

=PP5V_S5_LDO → PP5V_S5 (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V, MAKE_BASE=TRUE)
- =PP5V_S5_P1V5S3RS0FET 73
- =PP5V_S5_P5VSUSFET 73
- =PP5V_S5_TPAD 54
- =PP5V_S5_ISNS

=PP5V_SUS_FET → PP5V_SUS (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V, MAKE_BASE=TRUE)
- =PP5V_SUS_PCH 22

=PP5V_S3_REG → PP5V_S3 (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V, MAKE_BASE=TRUE)
- =PP5V_S3_ALSCAMERA 32
- =PP5V_S3_DDRREG 68
- =PP5V_S5_DEBUG_ADC_AVDD 104
- =PP5V_S5_DEBUG_ADC_DVDD 104
- =PP5V_S3_AUDIO
- =PP5V_S3_IR 41 44
- =PP5V_S3_MEMRESET 26
- =PP5V_S3_ODD 41
- =PP5V_S3_P5VS0FET 73
- =PP5V_S3_USB 42
- =PP5V_S3_SYSLED 46
- =PP5V_S3_P5VS0SW
- =PP5V_S3_P3V3S0SW
- =PP5V_S3_GFXIMVP 84

=PP5V_S0_FET → PP5V_S0 (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V, MAKE_BASE=TRUE)
- =PP5V_S0_ISNS 103
- =PP5V_S0_BKL 90
- =PP5V_S0_CPUIMVP 69 70
- =PP5V_S0_CPUVCCIOS0 71
- =PP5V_S0_FAN_LT 52
- =PP5V_S0_FAN_RT 52
- =PP5V_S0_VCCSAS0 66
- =PP5V_S0_VMON 74
- =PP5V_S0_HDD 41
- =PP5V_S0_KBDLED 54
- =PP5V_S0_LPCPLUS 47
- =PP5V_S0_PCH 22 24
- =PP5V_S0GPU_P1V05 78
- =PP5V_S0_AUDIO_XW 8
- =PP5V_S0_RMC 105
- =PP5V_S0GPU_P1V5 78

3.3V Rails

=PP3V3_S4_FET → PP3V3_S4 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE, VOLTAGE=3.3V)
- =PP3V3_S4_SD_HPD 30
- =PP3V3_S4_BT 32
- =PP3V3_S4_TPAD 53 54
- =PP3V3_S4_SMC 46

=PP3V3_SUS_FET → PP3V3_SUS (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE, VOLTAGE=3.3V)
- =PP3V3_SUS_P1V05SUSLDO 72
- =PP3V3_SUS_PCH_VCCSUS 20 22
- =PP3V3_SUS_PCH_VCCSUS_GPIO 20 22
- =PP3V3_SUS_PCH_GPIO 16 17 18 19
- =PP3V3_SUS_PCH_VCCSUS_USB 20 22
- =PP3V3_SUS_CNTRL 74
- =PP3V3_SUS_SMC 46
- =PP3V3_SUS_ROM 56
- =PP3V3_SUS_PCH_VCC_SPI 20 22

=PP3V3_S5_REG → PP3V3_S5 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- =PP3V3_GPU_P3V3GPUFET 73
- =PP3V3_S0_P3V3S0FET 73
- =PP3V3_S3_P3V3S3FET 73
- =PP3V3_S4_P3V3S4FET 73
- =PP3V3_S5_SYSCLK 24
- =PP3V3_S5_LCD 85
- =PP3V3_FW_P3V3FWFET 39
- =PP3V3_S5_P1V2P1V8 72
- =PP3V3_S5_PCH 17
- =PP3V3_S5_PCHPWRGD 92
- =PP3V3_S5_PCH_GPIO 19
- =PP3V3_S5_CPU_VCCDDR 26
- =PP3V3_S5_MEMVDDSEL
- =PP3V3_S5_PCH_VCCDSW 20 22
- =PP3V3_S5_VMON 74
- =PP3V3_S5_XDP 23
- =PP3V3_S5_P3V3SUSFET 73
- =PP3V3_S5_PWRCTL 74
- =PP3V3_S5_P1V5S0 72
- =PP3V3_S5_SMCBATLOW 46
- =PP3V3_S4_TBTAPWRSW 88

=PP3V3_S3_FET → PP3V3_S3_FET (MIN_LINE_WIDTH=0.50MM, MIN_NECK_WIDTH=0.20MM, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- =PP3V3_S3_ISNS_R 104

=PP3V3_S3_ISNS → PP3V3_S3 (MIN_LINE_WIDTH=0.50MM, MIN_NECK_WIDTH=0.20MM, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- =PP3V3_S3_BT 104 103 49 7
- =PP3V3_S3_GMUX 89
- =PP3V3_S3_MEMRESET 26
- =PP3V3_S3_P3V3ENETFET 74
- =PP3V3_S3_SMBUS_SMC_2_S3 48
- =PP3V3_S3_SMBUS_SMC_3 48
- =PP3V3_S3_SMS 55
- =PP3V3_S3_USB_HUB 25
- =PP3V3_S3_USB_RESET 25
- =PP3V3_S3_VREFMRGN 31
- =PP3V3_S3_WLAN 32
- =PP3V3_S3_ISNS 7 49 103 104
- =PP3V3_S3_PCH_GPIO 18 24
- =PP3V3_S3_USBMUX 25
- =PP3V3_S3_SDBUF 24

=PP3V3_S0_FET → PP3V3_S0 (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.075 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- =PP3V3_S0_XDP 23
- =PP3V3_S0_ENETPHY 36
- =PP3V3_S0_AUDIO 57 62 63
- =PP3V3_S0_BKL_VDDIO 90
- =PP3V3_S0_DPSDRVA 87
- =PP3V3_S0_HS_ISNS
- =PP3V3_S0_CPUTHMSNS 51
- =PP3V3_S0_DDC_LCD 85
- =PP3V3_S0_ISNS 49 50 103 104
- =PP3V3_S0_TBTPWRCTL 35
- =PP3V3_S0_DPMUX 86
- =PP3V3_S0_FAN_LT 52
- =PP3V3_S0_FAN_RT 52
- =PP3V3_S0_FWPWRCTL 39
- =PP3V3_S0_FWLATEVG 39 40
- =PP3V3_S0_CPU_VCCIO_SEL 12
- =PP3V3_S0_GMUX 86 89
- =PP3V3_S0_P3V3TBTFET 35
- =PP3V3_S0_GPUTHMSNS 51
- =PP3V3_S0_LVDSDDCMUX 86
- =PP3V3_S0_ODD 41
- =PP3V3_S0_PCH 16 22
- =PP3V3_S0_PCH_GPIO 16 17 18 19 30
- =PP3V3_S0_PCH_VCC3_3_CLK 22
- =PP3V3_S0_PCH_VCC3_3_GPIO 20 22
- =PP3V3_S0_PCH_VCC3_3_HVCMOS 20 22
- =PP3V3_S0_PCH_VCC3_3_PCI 20 22
- =PP3V3_S0_PCH_VCC3_3_SATA 20 22
- =PP3V3_S0_PCH_VCCADAC 22
- =PP3V3_S0_PCH_VCCA_LVDS 20
- =PP3V3_S0_PWRCTL 74 92
- =PP3V3_S0_RSTBUF 24
- =PP3V3_S0_SB_PM 24 92
- =PP3V3_S0_SDCARD 30
- =PP3V3_S0_SMBUS_PCH 48
- =PP3V3_S0_SMBUS_SMC_0_S0 48
- =PP3V3_S0_SMBUS_SMC_1_S0 48
- =PP3V3_S0_SMC 41
- =PP3V3_S0_TPAD 54
- =PP3V3_S0_VMON 74
- =PPSPD_S0_MEM_A 27
- =PPSPD_S0_MEM_B 29
- =PP3V3_S0_HDD 41
- =PP3V3_S0_P1V8GPUFET 73
- =PP3V3_S0_IMVPISNS 50
- =PP3V3_S0_T29I2C 48
- =PP3V3_S0_TBT_HPD_GPU

T29 Rails

=PP3V3_TBT_FET → PP3V3_TBT (MIN_LINE_WIDTH=0.4 MM, VOLTAGE=3.3V, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE)
- =PP3V3_T29_PCH_GPIO 16 19
- =PPVDDIO_T29_CLK 24
- =PP3V3_TBT_RTR 33 34 35
- =PP3V3_T29_JTAG 89

=PP1V05_TBT_FET → PP1V05_TBT (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE)
- =PP1V05_TBT_RTR_R 104

=PP15V_TBT_REG → PP15V_TBT (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=15V, MAKE_BASE=TRUE)
- =PPHV_SW_TBTAPWRSW 88

1.8V/1.5V/1.2V/1.05V Rails

=PP1V8_S0_REG → PP1V8_S0 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE)
2A max supply
- =PP1V8_S0_GMUX 89
- =PP1V8_S0_GPUFET 73
- =PP1V8_S0_PCH_VCCTX_LVDS 22
- =PP1V8_S0_PCH_VCC_DFTERM 19 20 22
- =PP1V8_S0_CPU_VCCPLL 14
- =PP1V8R1V5_S0_PCH_VCCVRM 20
- =PPVDDIO_S0_SBCLK 24

=PP1V8_S0_CPU_VCCPLL_R → PP1V8_S0_CPU_VCCPLL_R (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.8V, MAKE_BASE=TRUE)

=PPDDR_S3_REG → PP1V5_S3_REG (MIN_LINE_WIDTH=0.8 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE)
- =PP1V5_S3_ISNS_R 103

=PP1V5_S3_ISNS → PP1V5_S3 (MIN_LINE_WIDTH=0.8 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE)
- =PP1V5_S3_DDR_ISNS_R 49
- =PPVIN_S3_P1V5S3RS0_FET 73

=PP1V5_S3RS0_FET → PP1V5_S3RS0 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE)
- =PP1V5_S3_CPU_VCCDDR 10 13 15 26

=PP1V5_S3_DDR_ISNS → PP1V5_S3_DDR (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE)
- =PP1V5_S3_MEMRESET 26
- =PP1V5_S3_MEM_A 27
- =PP1V5_S3_MEM_B 29
- =PPVIN_S0_DDRREG_LDO 68
- =PPDDR_S3_MEMVREF 31

=PP1V5_S0_REG → PP1V5_S0 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE)
- =PP1V5_S0_RDRVR 41
- =PP1V5_S0_AUDIO 57
- =PP3V3R1V5_S0_PCH_VCCSUSHDA 20 22 24
- =PP1V5_S0_VMON 74

=PPVTT_S3_DDR_BUF → PPVTTDDR_S3 (MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0.75V, MAKE_BASE=TRUE)

=PPVTT_S0_DDR_LDO → PP0V75_S0_DDRVTT (MIN_LINE_WIDTH=2 mm, MIN_NECK_WIDTH=0.17 mm, VOLTAGE=0.75V, MAKE_BASE=TRUE)
- =PP0V75_S0_MEM_VTT_A 27
- =PP0V75_S0_MEM_VTT_B 29
- =PPVTT_S0_VTTCLAMP 26

=PP1V2_S0_REG → PP1V2_S0 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.2V, MAKE_BASE=TRUE)
- =PP1V2_S0_GMUX 89

=PP1V05_SUS_LDO → PP1V05_SUS (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE)
- =PP1V05_SUS_PCH_JTAG 23

=PPCPUVCCIO_S0_REG → PP1V05_S0 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE)
- =PP1V05_S0_CPU_VCCIO 9 10 12 13 14
- =PPVCCIO_S0_XDP 23
- =PPVCCIO_S0_CPUIMVP 69
- =PPVCCIO_S0_SMC 46
- =PP1V05_S0_RMC 105
- =PP1V05_S0_FWPWRCTL 39
- =PP1V05_FW_P1V0FWFET 39
- =PP1V05_S0_VMON 74
- =PP1V05_S0_P1V05TBTFET 35
- =PP1V05_S0_PCH_VCCIO_PLLPCIE 20
- =PP1V05_S0_PCH_VCCADPLL 22
- =PP1V05_S0_PCH_VCCIO 20 22
- =PP1V05_S0_PCH_VCCIO_PCIE 17
- =PP1V05_S0_PCH_VCCIO_SATA 16 20 22
- =PP1V05_S0_PCH_VCCIO_CLK 7 20 22
- =PP1V05_S0_PCH_VCCIO_USB 20 22
- =PP1V05_S0_PCH_VCC_CORE 20 22
- =PP1V05_S0_PCH_VCCASW 20 22
- =PP1V05_S0_PCH_VCCIO_CLK 7 20 22
- =PP1V05_S0_PCH_VCCDIFFCLK 16 20 22
- =PP1V05_S0_PCH 16 22
- =PP1V05_S0_PCH_VCCSSC 20 22
- =PP1V05_S0_PCH_V_PROC_IO 20 22
- =PP1V05_S0_PCH_VCCIO_PLLUSB 20
- =PP1V05_S0_PCH_VCC_DMI 20 22
- =PP1V05_S0_PCH_VCCIO_PLLEDI 20
- =PP1V05_S0_PCH_VCCDMI_FDI 20
- =PPPCHVCCIO_S0_REG 91

Backlight Rails

=PPBUS_SW_BKL → PPBUS_SW_BKL (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, MAKE_BASE=TRUE, VOLTAGE=12.8V)

=PP3V3_ENET_FET → PP3V3_ENET (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- =PP3V3_ENET_PHY 24 36 72
- =PPVDDIO_ENET_CLK 24
- =PP3V3_ENET_SYSCLK 24

ENET Rails

=PP1V2_S3_ENET_PHY → PP1V2_ENET (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.2V, MAKE_BASE=TRUE)
- =PP1V2_ENET_PHY 36

TBT Rails

=PP1V05_TBT_RTR → PP1V05_TBT_RTR (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE)

PPVIN_SW_TBTBST 35 (VOLTAGE=12.8V)

"GPU" Rails

=PP3V3_S0GPU_FET → PP3V3_S0GPU_FET (MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.10MM, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- =PP3V3_S0GPU_ISNS_R 104

=PP3V3_S0GPU_ISNS → PP3V3_S0GPU (MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.10MM, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- =PP3V3_GPU_IFPX_PLLVDD 81
- =PP3V3_GPU_LVDS_DDC 86
- =PP3V3_S0_GFX3V3BIAS 84
- =PP3V3_GPU_VDD33 75 81 82 83
- =PP3V3_GPU_OSC

=PP1V8_GPU_FET → PP1V8_S0GPU (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.15 MM, VOLTAGE=1.8V, MAKE_BASE=TRUE)
- =PP1V8_GPU_IFPAB_IOVDD 81

=PP1V5R1V35_GPU_REG → PPGPUFB_S0 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE)
- =PP1V35_GPU_FBVDDQ 76 79 80
- =PP1V35_GPU_S0_FB 77

=PP1V05_S0GPU_REG → PP1V05_S0GPU (MIN_LINE_WIDTH=0.9 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE)
- =PP1V05_GPU_IFPAB_PLLVDD 81
- =PP1V05_GPU_IFPCD_IOVDD 81
- =PP1V05_GPU_IFPEF_IOVDD 81
- =PP1V05_GPU_PEX_IOVDD 77 83
- =PP1V05_GPU_PEX_PLLVDD 81 83

=PPVCORE_S0_GFX_REG → PPVCORE_GPU (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.0V, MAKE_BASE=TRUE)
- =PPVCORE_GPU 76 83
- =PPVCORE_GPU_REG 49

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG → PPVCORE_S0_CPU (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, MAKE_BASE=TRUE, VOLTAGE=1.25V)
- =PPVCORE_S0_CPU 12 14 49 105

=PPVCORE_S0_AXG_REG → PPVCORE_S0_AXG (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE, VOLTAGE=1.05V)
- =PPVCORE_S0_CPU_VCCAXG 12 13 15

=PP1V5_S3_CPU_VCCDQ → PP1V5_S3_CPU_VCCDQ (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE, VOLTAGE=1.5V)

=PP1V05_S0_CPU_VCCPQE → PP1V05_S0_CPU_VCCPQE (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE)

=PPVCCSA_S0_REG → PPVCCSA_S0_REG (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0.9V, MAKE_BASE=TRUE)
- =PPVCCSA_S0_CPU 12 15

FireWire Rails

=PPBUS_FW_FET → PPVP_FW (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=12.8V, MAKE_BASE=TRUE)
- =PPVP_FW_PORT1 40
- =PPVP_FW_PHY_CPS_FET 40

=PP3V3_FW_FET → PP3V3_FW_FWPHY (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- =PP3V3_FW_FWPHY 38 39 40

=PP1V0_FW_FET_R → PP1V0_FW_FWPHY (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.0V, MAKE_BASE=TRUE)
- =PP1V0_FW_FWPHY 38 39

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SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 8 OF 132
SHEET: 7 OF 105

Thermal Module Holes

ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0985 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0986 STDOFF-4.50D.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND_BATT_CHGND
ZT0940 3R2P5 — GND_CHASSIS_LVDS
ZT0950 TH — GND_CHASSIS_FAN
SL-3.1X2.7-6CIR-NSP
ZT0960 3R2P5 — GND_CHASSIS_SATA
ZT0990 3R2P5 — GND_CHASSIS_BATTCONN

Tall EMI pogo pins

SH0930 POGO-2.00D-3.5H-K86-K87
SH0931 POGO-2.00D-3.5H-K86-K87 NOSTUFF
SH0902 POGO-2.00D-3.5H-K86-K87
SH0903 POGO-2.00D-3.5H-K86-K87
SH0904 POGO-2.00D-3.5H-K86-K87
SH0936 POGO-2.00D-3.5H-K86-K87 NOSTUFF
SH0914 1.4DIA-SHORT-SILVER-K99 — GND_CHASSIS_AUDIO_JACK 62

NOSTUFF SH0932 POGO-2.00D-3.5H-K86-K87
SH0933 POGO-2.00D-3.5H-K86-K87 NOSTUFF
SH0900 POGO-2.00D-3.5H-K86-K87
SH0916 POGO-2.00D-3.5H-K86-K87
SH0937 POGO-2.00D-3.5H-K86-K87 NOSTUFF
SH0938 POGO-2.00D-3.5H-K86-K87 NOSTUFF

Short (IO Row) EMI pogo pins

SH0910 1.4DIA-SHORT-SILVER-K99
SH0912 1.4DIA-SHORT-SILVER-K99
SH0901 1.4DIA-SHORT-SILVER-K99
SH0911 1.4DIA-SHORT-SILVER-K99
SH0913 1.4DIA-SHORT-SILVER-K99
SH0917 1.4DIA-SHORT-SILVER-K99
SH0918 1.4DIA-SHORT-SILVER-K99

Fan Holes

ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH

Left Speaker Holes

ZT0934 STDOFF-4.00D3.0H-TH
ZT0935 STDOFF-4.00D3.0H-TH
NOSTUFF
SH0934 POGO-2.00D-3.5H-K86-K87
SH0935 POGO-2.00D-3.5H-K86-K87 NOSTUFF

Keyboard / IPD Conn Protect

ZT0952 4.00D1.85H-M1.6X0.35
ZT0953 4.00D1.85H-M1.6X0.35

R0921 51 5% 1/20W MF 201 — T29_A_BIAS_R — TBT_A_BIAS0P — C0901 0.01UF 10% 10V XSR 201
R0922 51 5% 1/20W MF 201 — T29_A_BIAS_R — TBT_A_BIAS0N — C0902 0.01UF 10% 10V XSR 201
R0923 51 5% 1/20W MF 201 — T29_A_BIAS_R — TBT_A_BIAS2P — C0903 0.01UF 10% 10V XSR 201
R0924 51 5% 1/20W MF 201 — T29_A_BIAS_R — TBT_A_BIAS2N — C0904 0.01UF 10% 10V XSR 201

R9490 51 5% 1/20W MF 201 — T29_A_BIAS — =TBT_A_BIAS — C9490 0.1UF 10% 6.3V XSR 201 — T29_A_BIAS_R VOLTAGE=3.3V
PLACE_NEAR=C9490.1:2 mm

DPLL_REF_CLK_P 10 — DPLL_REF_CLK 93
R0941 1K 5% 1/16W MF-LF 402 — DPLL_REF_CLK_N 10 — DPLL_REF_CLKN
R0940 1K 5% 1/16W MF-LF 402 — =PP1V05_S0_CPU_VCCPQE 14 12
Unused eDP CLK

TBTBST:N
=PPVIN_SW_TBTBST 35 7 — R0950 0 5% 1/8W MF-LF 805 — =PP15V_TBT_REG 7 35

T29 / GMUX JTAG Signals

JTAG_ISP_TCK 23 19 — JTAG_GMUX_TCK — JTAG_TBT_TCK 33
JTAG_ISP_TDI 89 19 — JTAG_TBT_TDI 19 33
JTAG_ISP_TDO 89 19 — JTAG_TBT_TDO 33
TBT_LSOE<3> 33 — T29_LSEO_LSOE3 NO_TEST=TRUE — TBT_LSEO<3> 33
TBT_LSOE<2> 33 — T29_LSEO_LSOE2 — TBT_LSEO<2> 33

GMUX ALIASES

GMUX_INT 89 — DPMUX_UC_IRQ 19
PM_ALL_GPU_PGOOD 92 — ALL_EG_PGOOD 89
TP_LVDS_MUX_SEL_EG — LVDS_MUX_SEL_EG 89
EG_RESET_L 89 — GPU_RESET_L 75 82
LVDS_IG_BKL_ON 17 — IG_BKLT_EN 89
LVDS_IG_PANEL_PWR 17 — IG_LCD_PWR_EN 89
PPVOUT_S0_LCDBKLT 104 85 6 — PPVOUT_SW_LCDBKLT 90

PEX_CLKREQ_L — EG_CLKREQ_IN_L 82 89
PEG_CLKREQ_L 16 — EG_CLKREQ_OUT_L 89
PM_ENET_EN — =P1V2ENET_EN

Unused eDP signals

DP_INT_IG_ML_P<3..0> 93 9 — NC_DP_INT_IG_MLP<3..0>
DP_INT_IG_ML_N<3..0> 93 9 — NC_DP_INT_IG_MLN<3..0>
DP_INT_IG_AUX_P 93 9 — NC_DP_INT_IG_AUXP
DP_INT_IG_AUX_N 93 9 — NC_DP_INT_IG_AUXN
DP_INT_IG_HPD 9 — NC_DP_INT_IG_HPD

FW_PLUG_DET_L — FW_PME_L 19 39
FW643_WAKE_L 39 — =FW_PME_L 38 39
TP_SMC_EXCARD_PWR_EN — SMC_EXCARD_PWR_EN

PCIE_EXCARD_D2R_N 16 — NC_PCIE_EXCARD_D2RN
PCIE_EXCARD_D2R_P 16 — NC_PCIE_EXCARD_D2RP
PCIE_EXCARD_R2D_C_N 16 — NC_PCIE_EXCARD_R2D_CN
PCIE_EXCARD_R2D_C_P 16 — NC_PCIE_EXCARD_R2D_CP
PCIE_CLK100M_EXCARD_N 96 16 — NC_PCIE_CLK100M_EXCARDN
PCIE_CLK100M_EXCARD_P 96 16 — NC_PCIE_CLK100M_EXCARDP

TP_PEG_B_CLKRQ_L_GPIO56 — NC_PEG_B_CLKRQ_L_GPIO56
TP_PCIECLKRQ4_L_GPIO26 — NC_PCIECLKRQ4_L_GPIO26
TP_ISSP_SCLK_P1_1 53 — ISSP_SCLK_P1_1 6
TP_ISSP_SDATA_P1_0 53 — ISSP_SDATA_P1_0 6
TP_GMUX_PT20A 89
TP_GMUX_PT20B 89
TP_GMUX_PT32A 89
TP_GMUX_PT32B 89
=PP1V05_S0M_PCH_VCC_LAN

TP_PCH_CLKOUT_DPN 16 — NC_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP 16 — NC_PCH_CLKOUT_DPP
TP_PCH_GPIO64_CLKOUTFLEX0 16 — NC_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1 16 — NC_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2 16 — NC_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3 16 — NC_PCH_GPIO67_CLKOUTFLEX3

NC_FSB_CLK133M_PCHP — FSB_CLK133M_PCH_P
NC_FSB_CLK133M_PCHN — FSB_CLK133M_PCH_N
NC_LT_GAIN_TP — LT_GAIN_TP
NC_RT_GAIN_TP — RT_GAIN_TP
NC_SW_GAIN_TP — SW_GAIN_TP

LCD_BKLT_EN 90 89 — R0901 4.7K 5% 1/16W MF-LF 402

=PP5V_S0_AUDIO_XW 7 — XW0901 SM — PP5V_S0_AUDIO — =PP5V_S0_AUDIO 57
XW0902 SM — PP5V_S0_AUDIO_AMP_L 61 — MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.30MM VOLTAGE=5V
XW0903 SM — PP5V_S0_AUDIO_AMP_R 61 — MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.30MM VOLTAGE=5V

USB Signals

NC_USB_EXTD_EHCIN — USB_EXTD_EHCI_N 18
NC_USB_EXTD_EHCIP — USB_EXTD_EHCI_P 18
NC_USB3_EXTC_RXN — USB3_EXTC_RX_N 18
NC_USB3_EXTC_RXP — USB3_EXTC_RX_P 18
NC_USB3_EXTC_TXN — USB3_EXTC_TX_N 18
NC_USB3_EXTC_TXP — USB3_EXTC_TX_P 18

Unused PEG signals

NC_PEG_D2RP<15..12> — =PEG_D2R_P<15..12> 9
NC_PEG_D2RN<15..12> — =PEG_D2R_N<15..12> 9
NC_PEG_R2D_CP<15..12> — =PEG_R2D_C_P<15..12> 9
NC_PEG_R2D_CN<15..12> — =PEG_R2D_C_N<15..12> 9

T29 Signals Through PEG

PCIE_TBT_D2R_P<3..0> 96 33 — =PEG_D2R_P<11..8> 9
PCIE_TBT_D2R_N<3..0> 96 33 — =PEG_D2R_N<11..8> 9
PCIE_TBT_R2D_C_P<3..0> 96 33 — =PEG_R2D_C_P<11..8> 9
PCIE_TBT_R2D_C_N<3..0> 96 33 — =PEG_R2D_C_N<11..8> 9

GPU signals

PEG_D2R_P<7..0> 93 75 — =PEG_D2R_P<7..0> 9
PEG_D2R_N<7..0> 93 75 — =PEG_D2R_N<7..0> 9
PEG_R2D_C_P<7..0> 93 75 — =PEG_R2D_C_P<7..0> 9
PEG_R2D_C_N<7..0> 93 75 — =PEG_R2D_C_N<7..0> 9

Unused T29 Ports

TBT_D2R_P<3..2> 98 33 — NC_T29_D2RP<3..2>
TBT_D2R_N<3..2> 98 33 — NC_T29_D2RN<3..2>
TBT_R2D_C_P<3..2> 98 33 — NC_T29_R2D_CP<3..2>
TBT_R2D_C_N<3..2> 98 33 — NC_T29_R2D_CN<3..2>

CPU signals

MEMVTT_EN 26 — =DDRVTT_EN 26 68

DP_EG_AUXCH_N — DP_EG_AUX_CH_N 81 86 100
DP_EG_AUXCH_P — DP_EG_AUX_CH_P 81 86 100
NC_DPB_EG_AUX_CHN — DPB_EG_AUX_CH_N
NC_DPB_EG_AUX_CHP — DPB_EG_AUX_CH_P
NC_DPB_EG_DDC_CLK — DPB_EG_DDC_CLK
NC_DPB_EG_DDC_DATA — DPB_EG_DDC_DATA
NC_DPB_EG_MLN<3..0> — DPB_EG_ML_N<3..0>
NC_DPB_EG_MLP<3..0> — DPB_EG_ML_P<3..0>

R0926 51 5% 1/20W MF 201 — T29_A_BIAS_R — TBT_A_BIAS1P — C0906 0.01UF 10% 10V XSR 201
R0927 51 5% 1/20W MF 201 — T29_A_BIAS_R — TBT_A_BIAS1N — C0907 0.01UF 10% 10V XSR 201

PLACE_NEAR=C9361.1:2 mm
R9363 51 5% 1/20W MF 201 — DP_A_BIAS2
DP_A_BIAS — =DP_A_BIAS
R9362 51 5% 1/20W MF 201 — DP_A_BIAS0
PLACE_NEAR=C9361.1:2 mm
C0905 0.01UF 10% 10V XSR 201
C0908 0.01UF 10% 10V XSR 201

NC_DP_IG_MLP<3..0> — TP_DP_IG_B_MLP<3..0> 17
NC_DP_IG_MLN<3..0> — TP_DP_IG_B_MLN<3..0> 17
DP_IG_AUX_CH_P 95 86 — DPA_IG_AUX_CH_P 17
DP_IG_AUX_CH_N 95 86 — DPA_IG_AUX_CH_N 17
DP_IG_DDC_CLK 86 — DPA_IG_DDC_CLK 17
DP_IG_DDC_DATA 86 — DPA_IG_DDC_DATA 17
DP_IG_HPD 86 — DPA_IG_HPD 17

GND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.095 mm
VOLTAGE=0V
Digital Ground

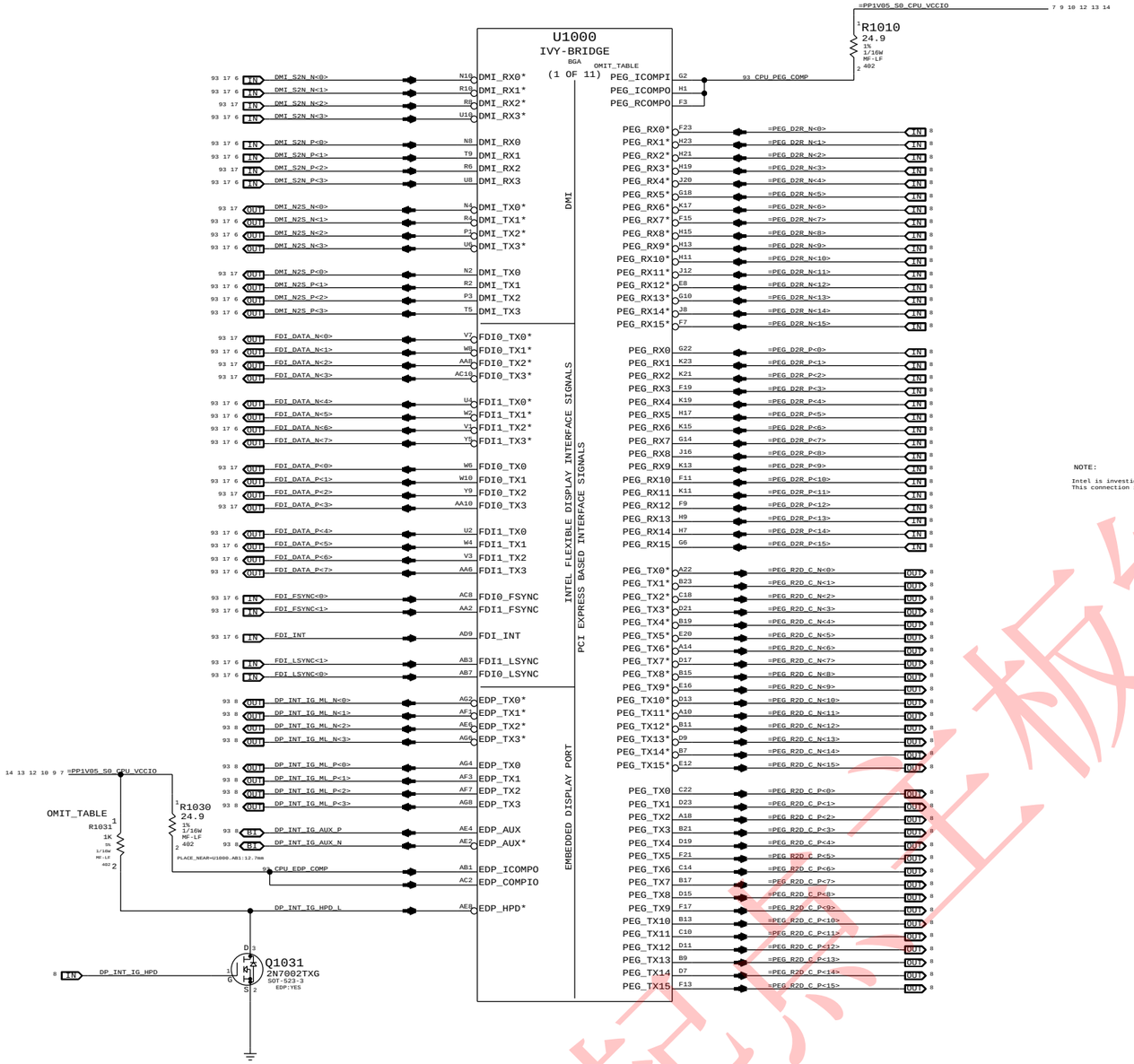
USB_BT_N 95 32 — USBHUB_DN1_N 25
USB_BT_P 95 32 — USBHUB_DN1_P 25
USB_TPAD_N 95 53 — USBHUB_DN3_N 25
USB_TPAD_P 95 53 — USBHUB_DN3_P 25
USB_IR_N 95 44 — USBHUB_DN2_N 25
USB_IR_P 95 44 — USBHUB_DN2_P 25
USB_SMC_N 95 — USBHUB_DN4_N 25
USB_SMC_P 95 — USBHUB_DN4_P 25
NC_ADC_CH6 — ADC_CH6 104
NC_ADC_CH7 — ADC_CH7 104
TP_LVDS_IG_B_CLKP 6 — LVDS_IG_B_CLK_P 17
TP_LVDS_IG_B_CLKN 6 — LVDS_IG_B_CLK_N 17
TP_LVDS_IG_BKL_PWM 6 — LVDS_IG_BKL_PWM 17
NC_GPU_XTALOUT — GPU_XTALOUT
NC_LVDS_IG_A_DATAP<3> — LVDS_IG_A_DATA_P<3> 17 95
NC_LVDS_IG_A_DATAN<3> — LVDS_IG_A_DATA_N<3> 17 95
NC_LVDS_IG_B_DATAP<3> — LVDS_IG_B_DATA_P<3> 17
NC_LVDS_IG_B_DATAN<3> — LVDS_IG_B_DATA_N<3> 17

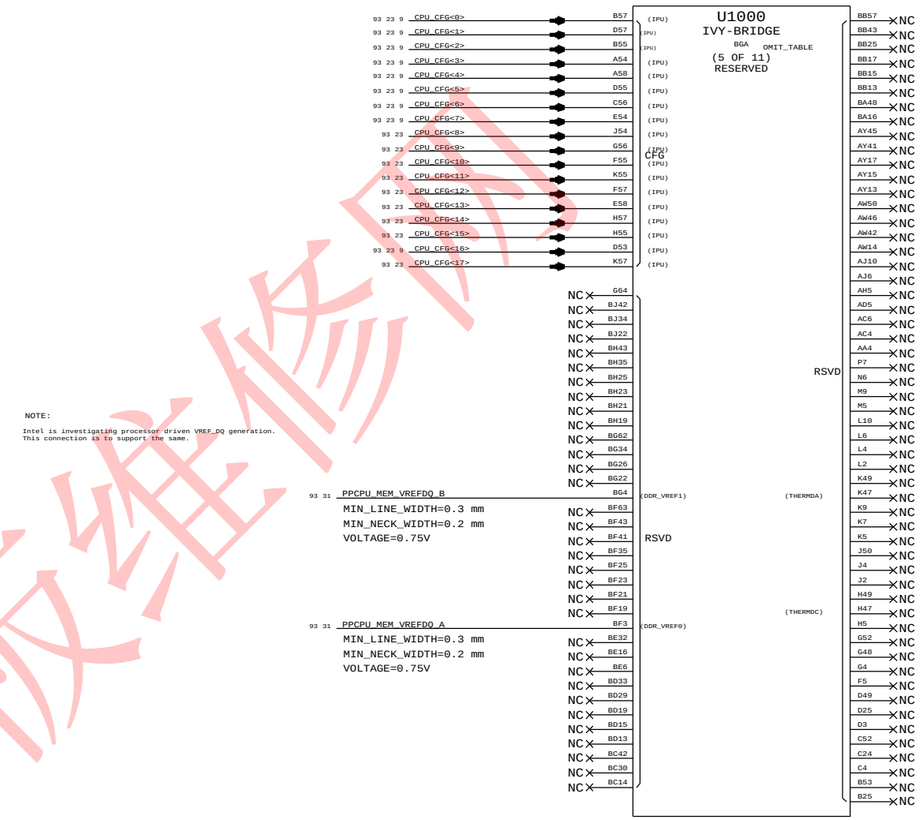
NC_USB_EXTCN — USB_EXTC_N 18 95
NC_USB_EXTCP — USB_EXTC_P 18 95
NC_USB3_EXTD_RXN — USB3_EXTD_RX_N 18
NC_USB3_EXTD_RXP — USB3_EXTD_RX_P 18
NC_USB3_EXTD_TXN — USB3_EXTD_TX_N 18
NC_USB3_EXTD_TXP — USB3_EXTD_TX_P 18

TALL POGO PINS for BT NF

SH0939 POGO-2.00D-3.5H-K86-K87
SH0941 POGO-2.00D-3.5H-K86-K87
SH0940 POGO-2.00D-3.5H-K86-K87
SH0942 POGO-2.00D-3.5H-K86-K87

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010
PAGE TITLE: Signal Aliases
Apple Inc.
DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 9 OF 132
SHEET 8 OF 105





NOTE:

Intel is investigating processor driven VREF_DQ generation.
This connection is to support the same.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0066	1	RES,MTL FILM,1/16W,1K,0402,SMD,LF	R1031		EDP:YES
116S0090	1	RES,MTL FILM,1/16W,10K,0402,SMD,LF	R1031		EDP:NO

CPU_CFG<4> should be pulled down to enable EDP

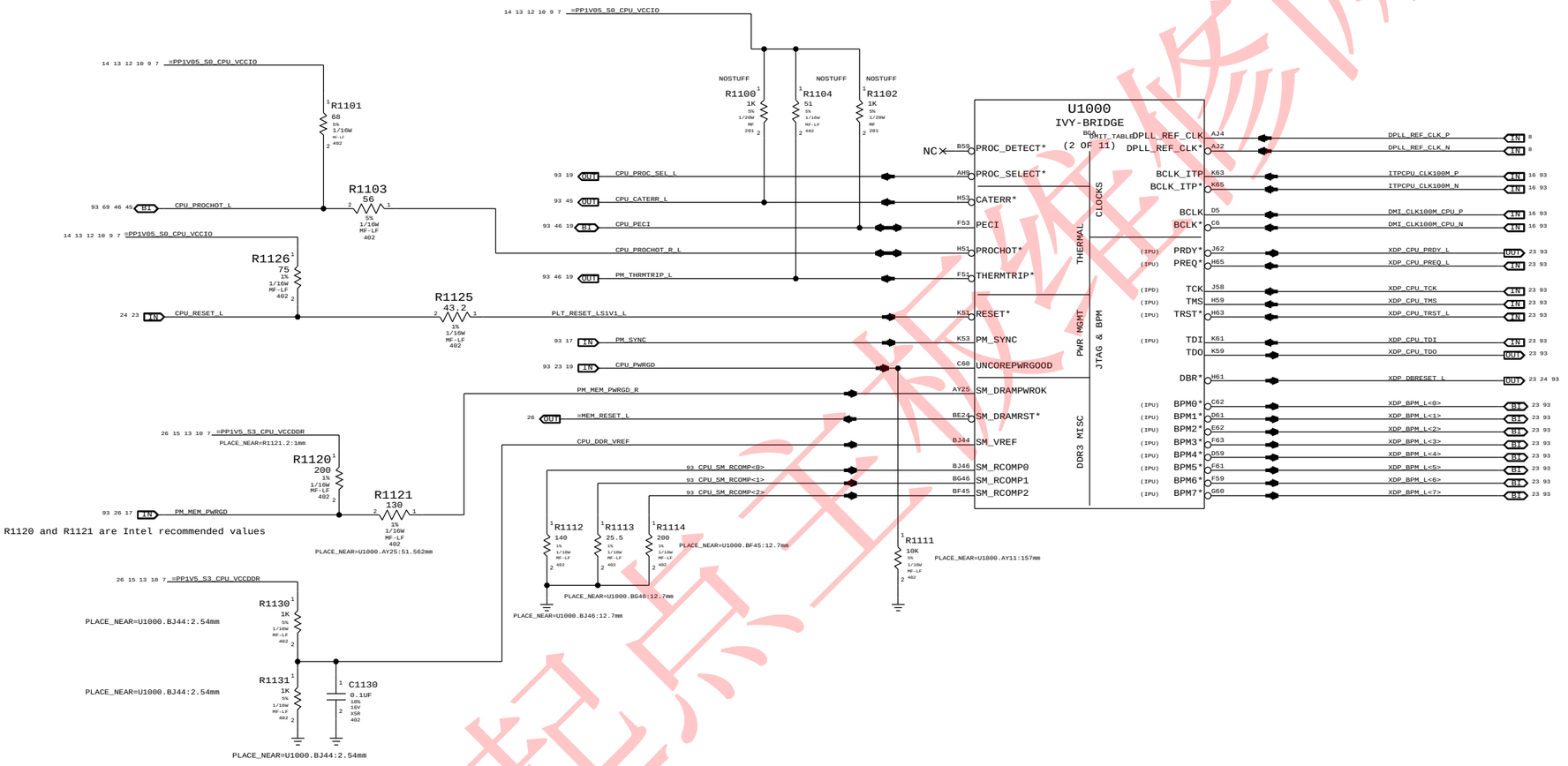
These can be Placed close to J2500 and Only for debug access

CFG [7] :PEG DEFER TRAINING — 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION — 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE — 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL — 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL — 1 = NORMAL OPERATION 0 = LANES REVERSED

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

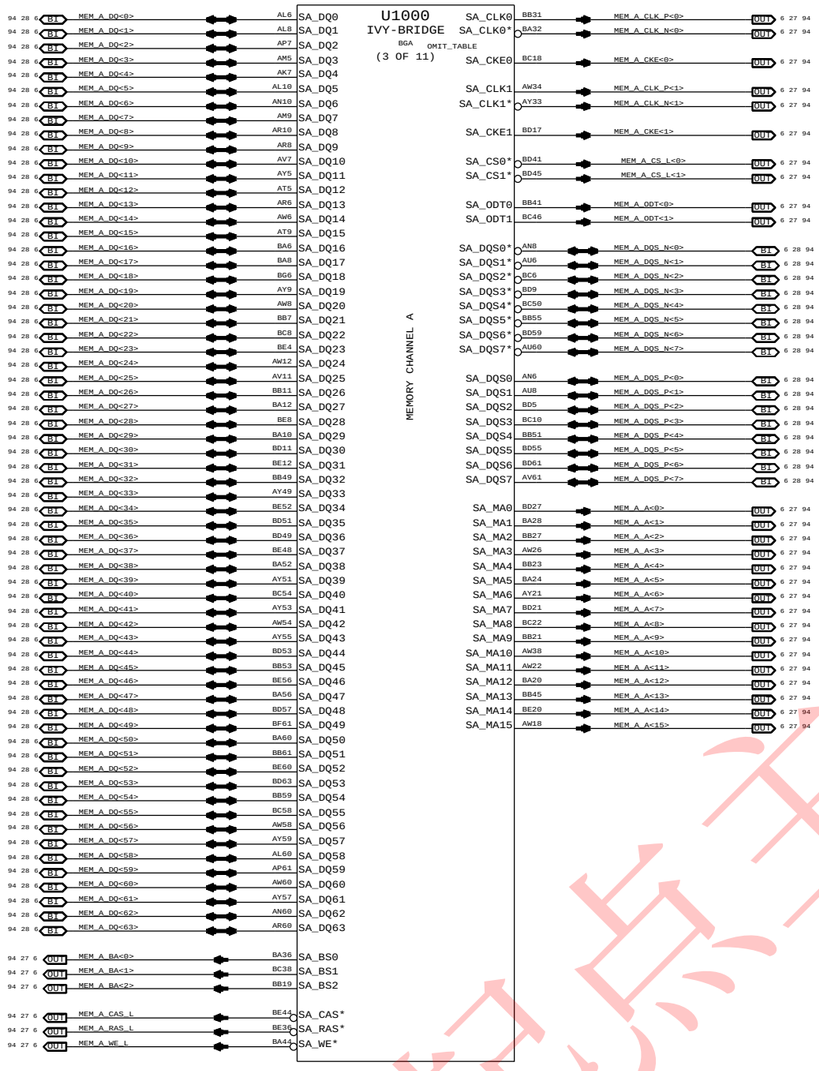
DRAWING NUMBER: 051-9585
SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 10 OF 132
SHEET: 9 OF 105

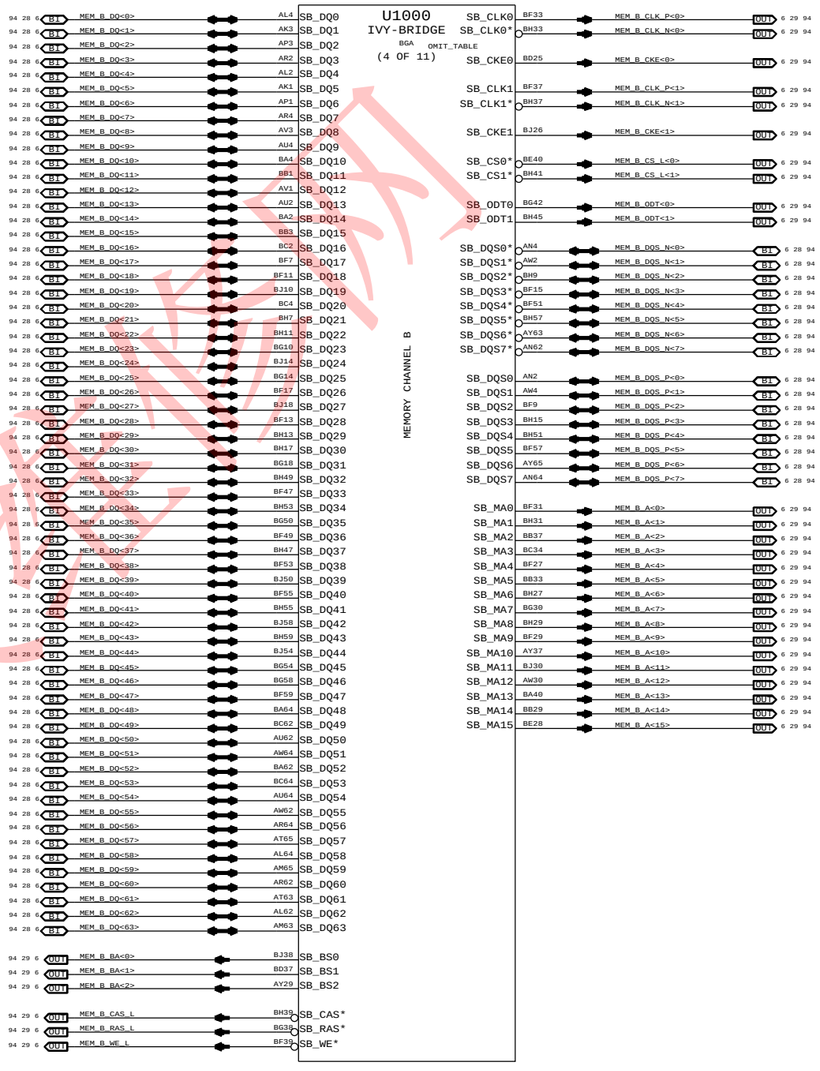


PAGE TITLE
CPU CLOCK/MISC/JTAG

Apple Inc.

DRAWING NUMBER 051-9585
SIZE D
REVISION 3.0.0
BRANCH
PAGE 11 OF 132
SHEET 10 OF 105



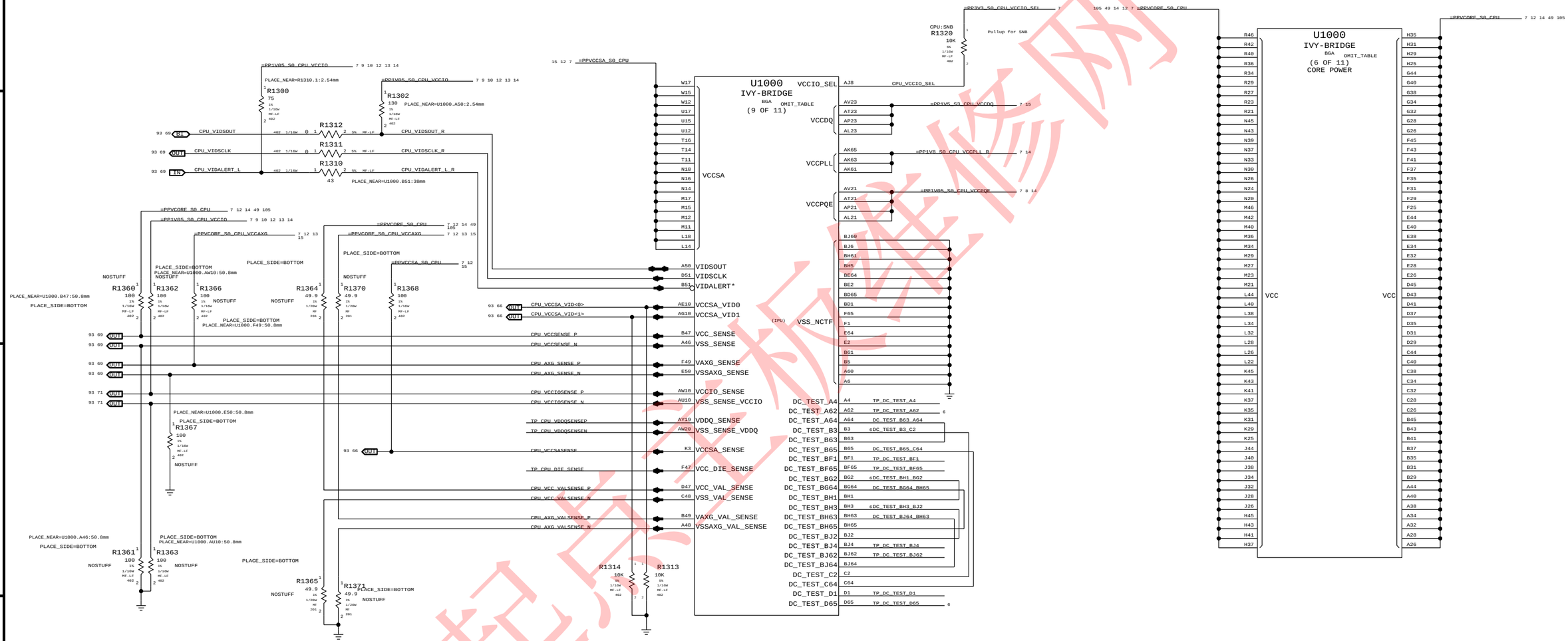


SYNC DATE=06/15/2016

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 12 OF 132
SHEET 11 OF 105



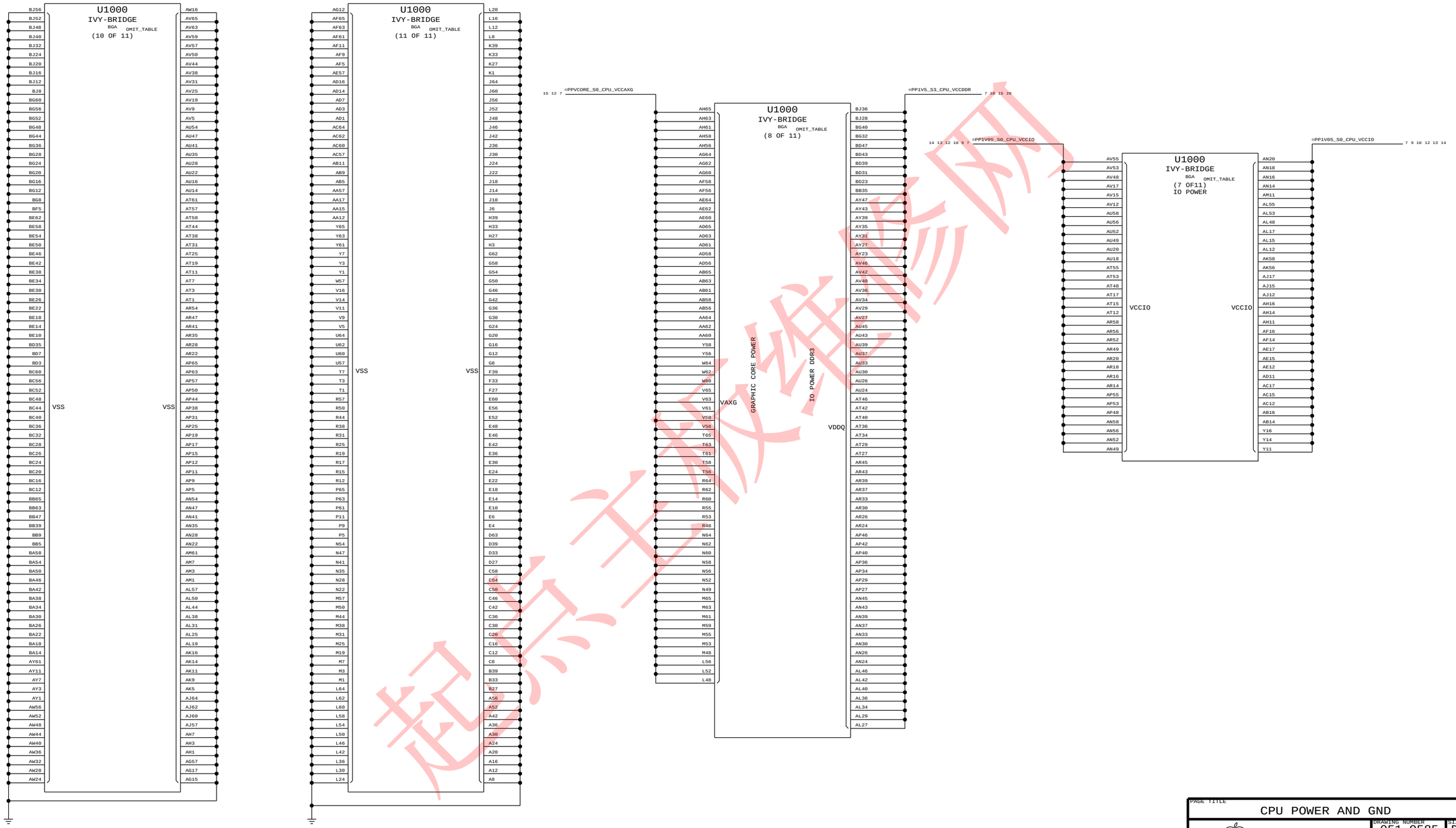
NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

SYNC_MASTER=K92_MLB SYNC_DATE=08/03/2010

PAGE TITLE: CPU POWER

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 13 OF 132
SHEET: 12 OF 105



PAGE TITLE
CPU POWER AND GND

Apple Inc.

DRAWING NUMBER 051-9585
SIZE D
REVISION 3.0.0
BRANCH
PAGE 14 OF 132
SHEET 13 OF 105

CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 8x 1uF 0402 (NOSTUFF)
Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

105 49 12 7 =PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 10% 10V X5R 402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 6.3V X5R 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 6.3V X5R 0201

PLACEMENT_NOTE (C1620-C1623):
Place near U1000 on bottom side

CRITICAL C1620 C1621 C1622 C1623
10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side. Place near inductors on bottom side.

CRITICAL C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
22UF 20% 6.3V X5R-CERM1 0603

NOSTUFF C16D0 C16D1 C16D2 C16D3 C16D4 C16D5
22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

NOSTUFF C1640 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CRITICAL C1641 C1642 C1643 C1644
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

13 12 10 9 7 =PP1V05_S0_CPU_VCCIO

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
1UF 10% 10V X5R 402

C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

CRITICAL C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 6.3V X5R 603

Place near inductors on bottom side

CRITICAL C1682 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

CRITICAL C1683 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

CRITICAL

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603

=PP1V05_S0_CPU_VCCPQE 7 8 12

C1684 1UF 10% 10V X5R 402

CPU VCCPLL DECOUPLING

7 =PP1V8_S0_CPU_VCCPLL

R1600 0 5% 1/10W MF-LF 402

=PP1V8_S0_CPU_VCCPLL_R 7 12

C1685 1UF 10% 10V X5R 402

C1686 1UF 10% 10V X5R 402

CRITICAL C1687 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA

PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

PLACE_NEAR=U1000.AK61:5 mm

CPU VCCPLL Low pass filter

SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2016

PAGE TITLE: CPU DECOUPLING-I

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 16 OF 132
SHEET: 14 OF 105

VAXG DECOUPLING

Intel recommendation: 2x 470uF 4mOhm, 2x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 8x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

13 12 7 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 1UF 10% 10V X5R 402
C1701 1UF 10% 10V X5R 402
C1702 1UF 10% 10V X5R 402
C1703 1UF 10% 10V X5R 402
C1704 1UF 10% 10V X5R 402
C1705 1UF 10% 10V X5R 402
C1706 1UF 10% 10V X5R 402
C1707 1UF 10% 10V X5R 402
C1708 1UF 10% 10V X5R 402
NOSTUFF C1709 1UF 10% 10V X5R 402
NOSTUFF C1710 1UF 10% 10V X5R 402
NOSTUFF C1711 1UF 10% 10V X5R 402
NOSTUFF C1712 1UF 10% 10V X5R 402
NOSTUFF C1713 1UF 10% 10V X5R 402
NOSTUFF C1714 1UF 10% 10V X5R 402
NOSTUFF C1715 1UF 10% 10V X5R 402
NOSTUFF C1716 1UF 10% 10V X5R 402
NOSTUFF C1717 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 10UF 20% 6.3V CERM-X5R 0402-1
C1719 10UF 20% 6.3V CERM-X5R 0402-1
C1720 10UF 20% 6.3V CERM-X5R 0402-1
C1721 10UF 20% 6.3V CERM-X5R 0402-1
C1722 10UF 20% 6.3V CERM-X5R 0402-1
C1723 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1724 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1725 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 22UF 20% 6.3V X5R-CERM1 0603
C1727 22UF 20% 6.3V X5R-CERM1 0603
C1728 22UF 20% 6.3V X5R-CERM1 0603
C1729 22UF 20% 6.3V X5R-CERM1 0603
C1730 22UF 20% 6.3V X5R-CERM1 0603
C1731 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1732 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1733 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1734-C1735):

CRITICAL C1734 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
CRITICAL C1735 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
NOSTUFF CRITICAL C1737 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

26 13 10 7 =PP1V5_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):
Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V X5R 603
C1749 10UF 20% 6.3V X5R 603
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V X5R 603
C1752 10UF 20% 6.3V X5R 603
C1753 10UF 20% 6.3V X5R 603
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V X5R 603

Place near inductors on bottom side

C1756 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700 0.010 1% 1/4W MF 0603
=PP1V5_S3_CPU_VCCDQ 7 12
C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 3x 10uF 0603, 3x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

12 7 =PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):
Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V X5R 603
C1764 10UF 20% 6.3V X5R 603
C1765 10UF 20% 6.3V X5R 603
C1766 10UF 20% 6.3V X5R 603
C1767 10UF 20% 6.3V X5R 603

C1768 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2016

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 17 OF 132
SHEET 15 OF 105

OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (1 OF 10)

RTC: RTCX1, RTCX2, RTCRST*, SRTCRST*, INTRUDER*, INTVRMEN

LPC: FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME*, (IPU) LDRQ0*, (IPU) LDRQ1*/GPIO23, SERIRQ

IHDA: HDA_BCLK, HDA_SYNC (IPD-BOOT), SPKR (IPD-PLTRST#), HDA_RST*, HDA_SDIN0 (IPD), HDA_SDIN1 (IPD), HDA_SDIN2 (IPD), HDA_SDIN3 (IPD), HDA_SDO (IPD-BOOT), HDA_DOCK_EN*/GPIO33, HDA_DOCK_RST*/GPIO13

SATA: SATA0RXN, SATA0RXP, SATA0TXN, SATA0TXP, SATA1RXN, SATA1RXP, SATA1TXN, SATA1TXP, SATA2RXN, SATA2RXP, SATA2TXN, SATA2TXP, SATA3RXN, SATA3RXP, SATA3TXN, SATA3TXP, SATA4RXN, SATA4RXP, SATA4TXN, SATA4TXP, SATA5RXN, SATA5RXP, SATA5TXN, SATA5TXP, SATAICOMPO, SATAICOMPI, SATA3RCOMPO, SATA3COMPI, SATA3RBIAS, SATALED*, SATA0GP/GPIO21, SATA1GP/GPIO19 (IPU)

JTAG: JTAG_TCK (IPD), JTAG_TMS (IPU), JTAG_TDI (IPU), JTAG_TDO

SPI: SPI_CLK, SPI_CS0*, SPI_CS1*, SPI_MOSI (IPD-BOOT), SPI_MISO (IPU)

NCX

=PP3V3_S0_PCH — R1820 10K 5% 1/20W MF 201

=PP1V05_S0_PCH_VCCIO_SATA — PLACE_NEAR=U1800.Y11:2.54mm — R1830 37.4 1% 1/20W MF 201

=PP1V05_S0_PCH — R1831 49.9 1% 1/20W MF 201 — PLACE_NEAR=U1800.AB12:2.54mm

PCH_SATAICOMP

PCH_SATA3COMP

PCH_SATA3RBIAS — PLACE_NEAR=U1800.AH1:2.54mm — R1832 750 5% 1/20W MF 201

PCH_SATALED_L

XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL

XDP_DC3_PCH_GPIO19_SATARDRVR_EN

=PPVRTC_G3_PCH — R1800 330K 5% 1/20W MF 201 — R1801 1M 5% 1/20W MF 201 — R1802 20K 5% 1/20W MF 201 — R1803 20K 5% 1/20W MF 201

RTC_RESET_L, PCH_SRTCRST_L, PCH_INTRUDER_L, PCH_INTVRMEN_L

C1802 1UF 10% 10V X5R 402 — C1803 1UF 10% 10V X5R 402

R1860 33 — LPC_AD_R<0> — LPC_AD<0>
R1861 33 — LPC_AD_R<1> — LPC_AD<1>
R1862 33 — LPC_AD_R<2> — LPC_AD<2>
R1863 33 — LPC_AD_R<3> — LPC_AD<3>
R1864 33 — LPC_FRAME_R_L — LPC_FRAME_L

R1810 33 — HDA_BIT_CLK_R — HDA_BIT_CLK — PLACE_NEAR=U1800.N34:1.27mm
R1811 33 — HDA_SYNC_R — HDA_SYNC — PLACE_NEAR=U1800.L34:1.27mm
R1812 33 — HDA_RST_R_L — HDA_RST_L — PLACE_NEAR=U1800.K34:1.27mm
R1813 33 — HDA_SDOUT_R — HDA_SDOUT — PLACE_NEAR=U1800.A36:1.27mm

ITPCPU_CLK100M_N — NO STUFF R1840 0 5% 1/20W MF 201
ITPCPU_CLK100M_P — NO STUFF R1841 0 5% 1/20W MF 201

R1880 10K — GPU:2P — PEGCLKRQB_L_GPIO56

=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
=PP3V3_T29_PCH_GPIO

R1876 10K — JTAG_TBT_TMS
R1877 4.7K — PCH_SPKR
R1878 10K — PCH_SATALED_L
R1834 10K — DP_AUXCH_ISOL
R1833 10K — SATARDRVR_EN
R1842 10K — FW_CLKREQ_L
R1869 10K — AP_CLKREQ_L
R1844 10K — EXCARD_CLKREQ_L
R1845 10K — JTAG_DPMUXUC_TRST_L
R1847 10K — ENET_CLKREQ_L
R1814 10K — PEG_CLKREQ_L
R1815 10K — TBT_CLKREQ_L
R1843 10K — PCIECLKRQ0_L_GPIO73
R1846 10K — PEGCLKRQA_L_GPIO47
R1848 10K — PEGCLKRQB_L_GPIO56
R1853 10K — PCH_GPIO11
R1854 10K — USB_EXTB_SEL_XHCI
R1855 10K — USB_EXTD_SEL_XHCI
R1879 10K — ENET_MEDIA_SENSE_RDIV

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (2 OF 10)

PCI-E*: PERN1, PERP1, PETN1, PETP1, PERN2, PERP2, PETN2, PETP2, PERN3, PERP3, PETN3, PETP3, PERN4, PERP4, PETN4, PETP4, PERN5, PERP5, PETN5, PETP5, PERN6, PERP6, PETN6, PETP6, PERN7, PERP7, PETN7, PETP7, PERN8, PERP8, PETN8, PETP8

C-LINK: CL_CLK1, CL_DATA1, CL_RST1*

CLOCKS: CLKOUT_PCIE0N, CLKOUT_PCIE0P, PCIECLKRQ0*/GPIO73, CLKOUT_PCIE1N, CLKOUT_PCIE1P, PCIECLKRQ1*/GPIO18, CLKOUT_PCIE2N, CLKOUT_PCIE2P, PCIECLKRQ2*/GPIO20, CLKOUT_PCIE3N, CLKOUT_PCIE3P, PCIECLKRQ3*/GPIO25, CLKOUT_PCIE4N, CLKOUT_PCIE4P, PCIECLKRQ4*/GPIO26, CLKOUT_PCIE5N, CLKOUT_PCIE5P, PCIECLKRQ5*/GPIO44 (IPU-RSMRST#), CLKOUT_PEG_B_N, CLKOUT_PEG_B_P, PEG_B_CLKRQ*/GPIO56, CLKOUT_PCIE6N, CLKOUT_PCIE6P, PCIECLKRQ6*/GPIO45, CLKOUT_PCIE7N, CLKOUT_PCIE7P, PCIECLKRQ7*/GPIO46 (IPU-RSMRST#), CLKOUT_ITPXDP_N, CLKOUT_ITPXDP_P

SMBUS: SMBALERT*/GPIO11, SMBCLK, SMBDATA, SML0ALERT*/GPIO60, SML0CLK, SML0DATA, SML1ALERT*/PCHHOT*/GPIO74, SML1CLK/GPIO58, SML1DATA/GPIO75

FLEX CLOCKS: CLKOUTFLEX0/GPIO64 (IPD-PWROK), CLKOUTFLEX1/GPIO65 (IPD-PWROK), CLKOUTFLEX2/GPIO66 (IPD-PWROK), CLKOUTFLEX3/GPIO67 (IPD-PWROK)

Controlled by PCIECLKRQ5#

PCH_GPIO11, SMBUS_PCH_CLK, SMBUS_PCH_DATA, USB_EXTB_SEL_XHCI, SML_PCH_0_CLK, SML_PCH_0_DATA, USB_EXTD_SEL_XHCI, SML_PCH_1_CLK, SML_PCH_1_DATA, TP_CLINK_CLK, TP_CLINK_DATA, TP_CLINK_RESET_L, PEGCLKRQA_L_GPIO47, TP_PCIE_CLK100M_PEGAN, TP_PCIE_CLK100M_PEGAP, DMI_CLK100M_CPU_N, DMI_CLK100M_CPU_P, TP_PCH_CLKOUT_DPN, TP_PCH_CLKOUT_DPP, PCIE_CLK100M_PCH_N, PCIE_CLK100M_PCH_P, PCH_CLKIN_GNDN1, PCH_CLKIN_GNDP1, PCH_CLK96M_DOT_N, PCH_CLK96M_DOT_P, PCH_CLK100M_SATA_N, PCH_CLK100M_SATA_P, PCH_CLK14P3M_REFCLK, PCH_CLK33M_PCIIN, SYSCLK_CLK25M_SB_R, PCH_XCLK_RCOMP, TP_PCH_GPIO64_CLKOUTFLEX0, TP_PCH_GPIO65_CLKOUTFLEX1, TP_PCH_GPIO66_CLKOUTFLEX2, TP_PCH_GPIO67_CLKOUTFLEX3

DOES THIS NEED LENGTH MATCH???

=PP1V05_S0_PCH_VCCDIFFCLK — R1890 90.9 1% 1/20W MF 201 — PLACE_NEAR=U1800.Y47:2.54mm

SYSCLK_CLK25M_SB — R1872 604 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_SB_R — 1.8V -> 1.1V — R1873 1K 1% 1/20W MF 201

Unused clock terminations for FCIM Mode

PCH_CLK96M_DOT_P — R1891 10K
PCH_CLK96M_DOT_N — R1892 10K
PCH_CLK100M_SATA_P — R1893 10K
PCH_CLK100M_SATA_N — R1894 10K
PCIE_CLK100M_PCH_P — R1895 10K
PCIE_CLK100M_PCH_N — R1896 10K
PCH_CLK14P3M_REFCLK — R1897 10K
PCH_CLKIN_GNDP1 — R1870 10K
PCH_CLKIN_GNDN1 — R1871 10K

SYNC_MASTER=J31_ANNE	SYNC_DATE=06/02/2011
PAGE TITLE: PCH SATA/PCIe/CLK/LPC/SPI	
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 18 OF 132
	SHEET 16 OF 105

=PP3V3_SUS_PCH_GPIO 7 16 17 18 19
=PP1V05_S0_PCH_VCCIO_PCIE 7
PLACE_NEAR=U1800.BJ24:12.7mm
R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201

OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (3 OF 10)

DMI:
- DMI_N2S_N<0> BC24 DMI0RXN
- DMI_N2S_N<1> BE20 DMI1RXN
- DMI_N2S_N<2> BG18 DMI2RXN
- DMI_N2S_N<3> BG20 DMI3RXN
- DMI_N2S_P<0> BE24 DMI0RXP
- DMI_N2S_P<1> BC20 DMI1RXP
- DMI_N2S_P<2> BJ18 DMI2RXP
- DMI_N2S_P<3> BJ20 DMI3RXP
- DMI_S2N_N<0> AW24 DMI0TXN
- DMI_S2N_N<1> AW20 DMI1TXN
- DMI_S2N_N<2> BB18 DMI2TXN
- DMI_S2N_N<3> AV18 DMI3TXN
- DMI_S2N_P<0> AY24 DMI0TXP
- DMI_S2N_P<1> AY20 DMI1TXP
- DMI_S2N_P<2> AY18 DMI2TXP
- DMI_S2N_P<3> AU18 DMI3TXP
- PCH_DMI_COMP BJ24 DMI_ZCOMP; BG25 DMI_IRCOMP
- PCH_DMI2RBIAS BH21 DMI2RBIAS

FDI:
- FDI_RXN0 BJ14 ← FDI_DATA_N<0>
- FDI_RXN1 AY14 ← FDI_DATA_N<1>
- FDI_RXN2 BE14 ← FDI_DATA_N<2>
- FDI_RXN3 BH13 ← FDI_DATA_N<3>
- FDI_RXN4 BC12 ← FDI_DATA_N<4>
- FDI_RXN5 BJ12 ← FDI_DATA_N<5>
- FDI_RXN6 BG10 ← FDI_DATA_N<6>
- FDI_RXN7 BG9 ← FDI_DATA_N<7>
- FDI_RXP0 BG14 ← FDI_DATA_P<0>
- FDI_RXP1 BB14 ← FDI_DATA_P<1>
- FDI_RXP2 BF14 ← FDI_DATA_P<2>
- FDI_RXP3 BG13 ← FDI_DATA_P<3>
- FDI_RXP4 BE12 ← FDI_DATA_P<4>
- FDI_RXP5 BG12 ← FDI_DATA_P<5>
- FDI_RXP6 BJ10 ← FDI_DATA_P<6>
- FDI_RXP7 BH9 ← FDI_DATA_P<7>
- FDI_INT AW16 → FDI_INT
- FDI_FSYNC0 AV12 → FDI_FSYNC<0>
- FDI_FSYNC1 BC10 → FDI_FSYNC<1>
- FDI_LSYNC0 AV14 → FDI_LSYNC<0>
- FDI_LSYNC1 BB10 → FDI_LSYNC<1>

SYSTEM POWER MANAGEMENT:
- DSWVRMEN A18 ← PCH_DSWVRMEN
- DPWROK E22 ← PM_DSW_PWRGD
- WAKE* B9 ← PCIE_WAKE_L
- CLKRUN*/GPIO32 N3 ↔ PM_CLKRUN_L
- SUS_STAT*/GPIO61 G8 → LPC_PWRDWN_L
- SUSCLK/GPIO62 N14 → PM_CLK32K_SUSCLK_R
- SLP_S5*/GPIO63 D10 → PM_SLP_S5_L
- SLP_S4* H4 → PM_SLP_S4_L
- SLP_S3* F4 → PM_SLP_S3_L
- SLP_A* G10 → TP_PM_SLP_A_L
- SLP_SUS* G16 → PM_SLP_SUS_L
- PMSYNCH AP14 → PM_SYNC
- SLP_LAN*/GPIO29 K14 → MEM_VDD_SEL_1V5_L

PCH_SUSACK_L 17 → C12 SUSACK* (IPU)
PM_SYSRST_L 45 24 6 → K3 SYS_RESET*
PM_SYS_PWROK 92 45 23 → P12 SYS_PWROK
PM_PCH_PWROK 92 24 → L22 PWROK
PM_PCH_APWROK 92 → L10 APWROK
PM_MEM_PWRGD 93 26 10 → B13 DRAMPWROK
PM_RSMRST_L 74 → C21 RSMRST*
PCH_SUSWARN_L 17 → K16 SUSWARN*/SUSPWRDNACK/GPIO30
PM_PWRBTN_L 45 23 17 → E20 PWRBTN* (IPU)
SMC_ADAPTER_EN 74 46 45 → H20 ACPRESENT/GPIO31 (IPD-DeepS4/S5)
PM_BATLOW_L 46 → E10 BATLOW*/GPIO72 (IPU)
PCH_RI_L → A10 RI*

PLACE_NEAR=U1800.BH21:2.54mm
R1920 750 1% 1/20W MF 201

=PPVRTC_G3_PCH 7 16 20
R1915 390K 5% 1/20W MF 201
R1909 100K 5% 1/20W MF 201 → IN 45

OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (4 OF 10)

LVDS:
- LVDS_IG_BKL_ON 17 8 → J47 L_BKLTEN
- LVDS_IG_PANEL_PWR 17 8 → M45 L_VDD_EN
- LVDS_IG_BKL_PWM 8 → P45 L_BKLTCTL
- LVDS_IG_DDC_CLK 86 → T40 L_DDC_CLK
- LVDS_IG_DDC_DATA 86 → K47 L_DDC_DATA (IPD-PLTRST#)
- TP_LVDS_IG_CTRL_CLK 6 → T45 L_CTRL_CLK
- TP_LVDS_IG_CTRL_DATA 6 → P39 L_CTRL_DATA
- PCH_LVDS_IBG → AF37 LVD_IBG
- PCH_LVDS_VBG 6 → AF36 LVD_VBG
- AE48 LVD_VREFH
- AE47 LVD_VREFL
- LVDS_IG_A_CLK_N 95 89 → AK39 LVDSA_CLK*
- LVDS_IG_A_CLK_P 95 89 → AK40 LVDSA_CLK
- LVDS_IG_A_DATA_N<0> 95 89 → AN48 LVDSA_DATA0*
- LVDS_IG_A_DATA_N<1> 95 89 → AM47 LVDSA_DATA1*
- LVDS_IG_A_DATA_N<2> 95 89 → AK47 LVDSA_DATA2*
- LVDS_IG_A_DATA_N<3> 95 8 → AJ48 LVDSA_DATA3*
- LVDS_IG_A_DATA_P<0> 95 89 → AN47 LVDSA_DATA0
- LVDS_IG_A_DATA_P<1> 95 89 → AM49 LVDSA_DATA1
- LVDS_IG_A_DATA_P<2> 95 89 → AK49 LVDSA_DATA2
- LVDS_IG_A_DATA_P<3> 95 8 → AJ47 LVDSA_DATA3
- LVDS_IG_B_CLK_N 8 → AF40 LVDSB_CLK*
- LVDS_IG_B_CLK_P 8 → AF39 LVDSB_CLK
- LVDS_IG_B_DATA_N<0> 95 89 → AH45 LVDSB_DATA0*
- LVDS_IG_B_DATA_N<1> 95 89 → AH47 LVDSB_DATA1*
- LVDS_IG_B_DATA_N<2> 95 89 → AF48 LVDSB_DATA2*
- LVDS_IG_B_DATA_N<3> 8 → AF45 LVDSB_DATA3*
- LVDS_IG_B_DATA_P<0> 95 89 → AH43 LVDSB_DATA0
- LVDS_IG_B_DATA_P<1> 95 89 → AH49 LVDSB_DATA1
- LVDS_IG_B_DATA_P<2> 95 89 → AF47 LVDSB_DATA2
- LVDS_IG_B_DATA_P<3> 8 → AF43 LVDSB_DATA3

CRT:
- TP_CRT_IG_BLUE 6 → N48 CRT_BLUE
- TP_CRT_IG_GREEN 6 → P49 CRT_GREEN
- TP_CRT_IG_RED → T49 CRT_RED
- TP_CRT_IG_DDC_CLK 6 → T39 CRT_DDC_CLK
- TP_CRT_IG_DDC_DATA 6 → M40 CRT_DDC_DATA
- TP_CRT_IG_HSYNC 6 → M47 CRT_HSYNC
- TP_CRT_IG_VSYNC 6 → M49 CRT_VSYNC
- PCH_DAC_IREF → T43 DAC_IREF
- T42 CRT_IRTN

PLACE_NEAR=U1800.AF37:2.54mm
R1950 2.37K 1% 1/20W MF 201
PLACE_NEAR=U1800.T43:2.54mm
R1951 1K 5% 1/20W MF 201

DIGITAL DISPLAY INTERFACE:
- SDVO_TVCLKINN (IPD) AP43 ← TP_SDVO_TVCLKINN
- SDVO_TVCLKINP (IPD) AP45 ← TP_SDVO_TVCLKINP
- SDVO_STALLN (IPD) AM42 ← TP_SDVO_STALLN
- SDVO_STALLP (IPD) AM40 ← TP_SDVO_STALLP
- SDVO_INTN (IPD) AP39 ← TP_SDVO_INTN
- SDVO_INTP (IPD) AP40 ← TP_SDVO_INTP
- SDVO_CTRLCLK P38 → DPA_IG_DDC_CLK
- SDVO_CTRLDATA (IPD-PLTRST#) M39 ↔ DPA_IG_DDC_DATA
- DDPB_AUXN AT49 ↔ DPA_IG_AUX_CH_N
- DDPB_AUXP AT47 ↔ DPA_IG_AUX_CH_P
- DDPB_HPD AT40 → DPA_IG_HPD
- DDPB_0N AV42 → TP_DP_IG_B_MLN<0>
- DDPB_0P AV40 → TP_DP_IG_B_MLP<0>
- DDPB_1N AV45 → TP_DP_IG_B_MLN<1>
- DDPB_1P AV46 → TP_DP_IG_B_MLP<1>
- DDPB_2N AU48 → TP_DP_IG_B_MLN<2>
- DDPB_2P AU47 → TP_DP_IG_B_MLP<2>
- DDPB_3N AV47 → TP_DP_IG_B_MLN<3>
- DDPB_3P AV49 → TP_DP_IG_B_MLP<3>
- DDPC_CTRLCLK P46 → DPB_IG_DDC_CLK
- DDPC_CTRLDATA (IPD-PLTRST#) P42 ↔ DPB_IG_DDC_DATA
- DDPC_AUXN AP47 ↔ DPB_IG_AUX_CH_N
- DDPC_AUXP AP49 ↔ DPB_IG_AUX_CH_P
- DDPC_HPD AT38 → DPB_IG_HPD
- DDPC_0N AY47 → TP_DP_IG_C_MLN<0>
- DDPC_0P AY49 → TP_DP_IG_C_MLP<0>
- DDPC_1N AY43 → TP_DP_IG_C_MLN<1>
- DDPC_1P AY45 → TP_DP_IG_C_MLP<1>
- DDPC_2N BA47 → TP_DP_IG_C_MLN<2>
- DDPC_2P BA48 → TP_DP_IG_C_MLP<2>
- DDPC_3N BB47 → TP_DP_IG_C_MLN<3>
- DDPC_3P BB49 → TP_DP_IG_C_MLP<3>
- DDPD_CTRLCLK M43 → TP_DP_IG_D_CTRL_CLK
- DDPD_CTRLDATA (IPD-PLTRST#) M36 → TP_DP_IG_D_CTRL_DATA
- DDPD_AUXN AT45 → TP_DP_IG_D_AUXN
- DDPD_AUXP AT43 → TP_DP_IG_D_AUXP
- DDPD_HPD BH41 → TP_DP_IG_D_HPD
- DDPD_0N BB43 → TP_DP_IG_D_MLN<0>
- DDPD_0P BB45 → TP_DP_IG_D_MLP<0>
- DDPD_1N BF44 → TP_DP_IG_D_MLN<1>
- DDPD_1P BE44 → TP_DP_IG_D_MLP<1>
- DDPD_2N BF42 → TP_DP_IG_D_MLN<2>
- DDPD_2P BE42 → TP_DP_IG_D_MLP<2>
- DDPD_3N BJ42 → TP_DP_IG_D_MLN<3>
- DDPD_3P BG42 → TP_DP_IG_D_MLP<3>

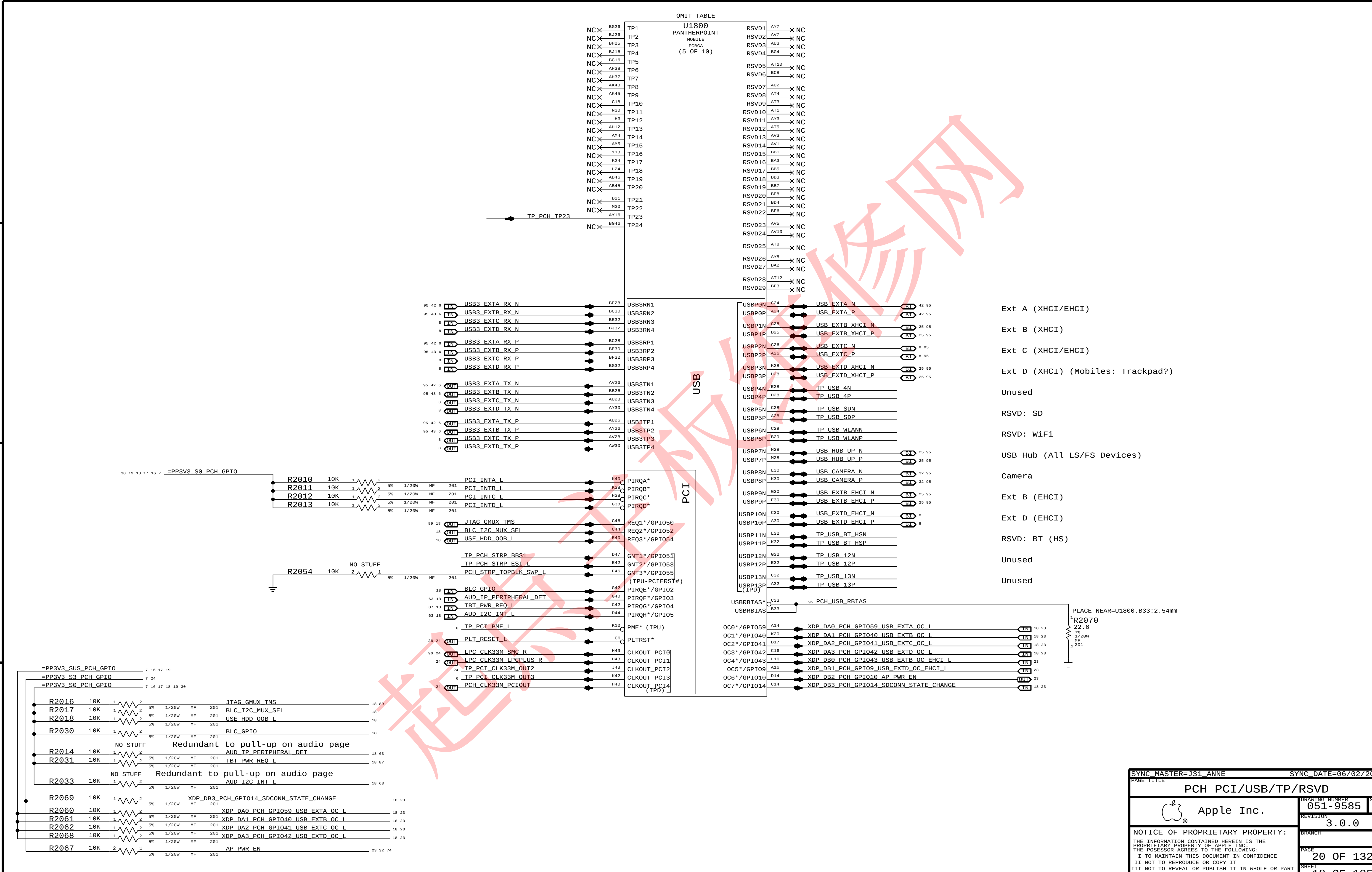
19 18 17 16 7 =PP3V3_SUS_PCH_GPIO
R1983 10K 5% 1/20W MF 201
R1986 0 5% 1/20W MF 201
17 PCH_SUSWARN_L — PCH_SUSACK_L 17

=PP3V3_SUS_PCH_GPIO 7 16 17 18 19
=PP3V3_S0_PCH_GPIO 7 16 18 19 30
=PP3V3_S5_PCH 7

R1985 1K 5% 1/20W MF 201 — PM_PWRBTN_L 17 23 45
R1991 8.2K 5% 1/20W MF 201 — PM_CLKRUN_L 6 17 45 47
R1982 10K 5% 1/20W MF 201 — MEM_VDD_SEL_1V5_L 17
R1925 1K 5% 1/20W MF 201 MAKE_BASE=TRUE — PCIE_WAKE_L 6 17 24 32 — =TBT_WAKE_L → IN 87

R1924 100K 5% 1/20W MF 201 — PM_SLP_S3_L 6 17 26 45 74
R1921 100K 5% 1/20W MF 201 — PM_SLP_S4_L 17 26 32 45 74
R1922 100K 5% 1/20W MF 201 — PM_SLP_S5_L 17 45 74
R1923 100K 5% 1/20W MF 201 — PM_SLP_SUS_L 17 74
R1981 100K 5% 1/20W MF 201 — LVDS_IG_BKL_ON 8 17
R1984 100K 5% 1/20W MF 201 — LVDS_IG_PANEL_PWR 8 17

SYNC_MASTER=J5_MLB SYNC_DATE=05/26/2011
PAGE TITLE: PCH DMI/FDI/PM/Graphics
Apple Inc.
DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 19 OF 132
SHEET 17 OF 105



SYNC_MASTER=J31_ANNE SYNC_DATE=06/02/2011

PAGE TITLE

PCH PCI/USB/TP/RSVD

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

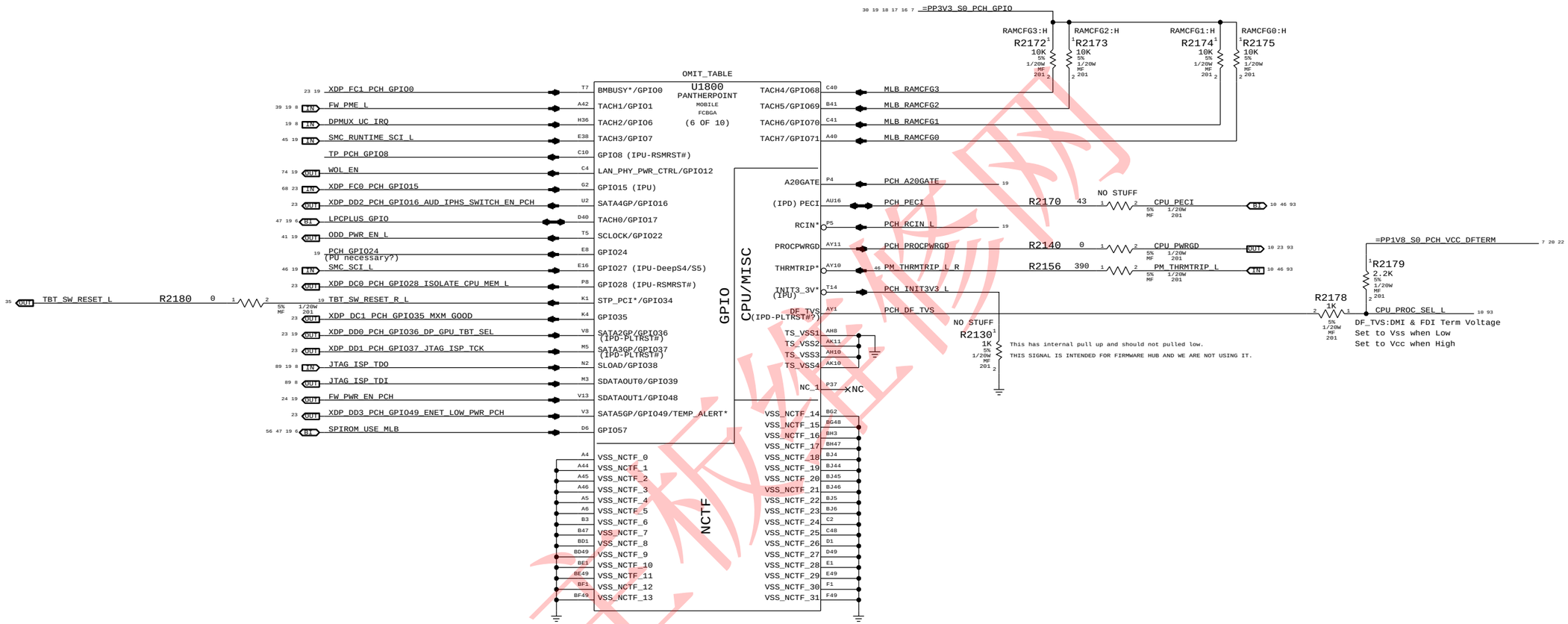
REVISION: 3.0.0

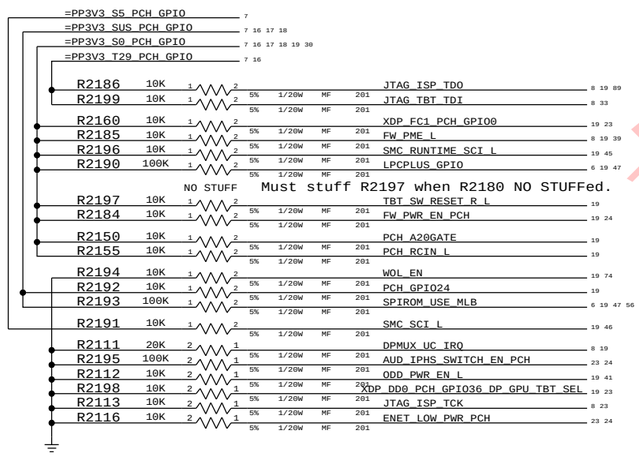
BRANCH

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.

Systems with chip-down memory should add pull-downs on another page and set straps per software.





SYNC_MASTER=J31_ANNE	SYNC_DATE=06/02/2011
PAGE TITLE	PCH GPIO/MISC/NCTF
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 21 OF 132
	SHEET 19 OF 105

VCCACLK pin left as NC per DG

VCCAPLLDMI2 pin left as NC per DG

AL24 left as NC per DG

PCH output, for decoupling only

PLACE_NEAR=U1800.N16:2.54mm

55mA Max, 5mA Idle

NC-ed per DG

OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (8 OF 10)

USB

CLK/MISC

PCI/GPIO/LPC

SATA

MISC

CPU

HDA

RTC

DCPSUS_4_USB NC-ed per DG

VCCAPLLSATA pin left as NC per DG

10 mA Max, 1mA Idle

1.44 A Max, 474mA Idle

OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (7 OF 10)

VCC CORE

CRT

LVDS

HVCMOS

VCCIO

DMI

FDI

DFT/SPI

VCCAFDIPLL pin left as NC per DG

SYNC_MASTER=J5_MLB SYNC_DATE=03/21/2011

PAGE TITLE

PCH POWER

Apple Inc.

DRAWING NUMBER 051-9585

SIZE D

REVISION 3.0.0

BRANCH

PAGE 22 OF 132

SHEET 20 OF 105

OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
FCBGA
(9 OF 10)
VSS

H5	VSS	VSS	AK38
AA17	VSS	VSS	AK4
AA2	VSS	VSS	AK42
AA3	VSS	VSS	AK46
AA33	VSS	VSS	AK8
AA34	VSS	VSS	AL16
AB11	VSS	VSS	AL17
AB14	VSS	VSS	AL19
AB39	VSS	VSS	AL2
AB4	VSS	VSS	AL21
AB43	VSS	VSS	AL23
AB5	VSS	VSS	AL26
AB7	VSS	VSS	AL27
AC19	VSS	VSS	AL31
AC2	VSS	VSS	AL33
AC21	VSS	VSS	AL34
AC24	VSS	VSS	AL48
AC33	VSS	VSS	AM11
AC34	VSS	VSS	AM14
AC48	VSS	VSS	AM36
AD10	VSS	VSS	AM39
AD11	VSS	VSS	AM43
AD12	VSS	VSS	AM45
AD13	VSS	VSS	AM46
AD19	VSS	VSS	AM7
AD24	VSS	VSS	AN2
AD26	VSS	VSS	AN29
AD27	VSS	VSS	AN3
AD33	VSS	VSS	AN31
AD34	VSS	VSS	AP12
AD36	VSS	VSS	AP19
AD37	VSS	VSS	AP28
AD38	VSS	VSS	AP30
AD39	VSS	VSS	AP32
AD4	VSS	VSS	AP38
AD40	VSS	VSS	AP4
AD42	VSS	VSS	AP42
AD43	VSS	VSS	AP46
AD45	VSS	VSS	AP8
AD46	VSS	VSS	AR2
AD8	VSS	VSS	AR48
AE2	VSS	VSS	AT11
AE3	VSS	VSS	AT13
AF10	VSS	VSS	AT18
AF12	VSS	VSS	AT22
AD14	VSS	VSS	AT26
AD16	VSS	VSS	AT28
AF16	VSS	VSS	AT30
AF19	VSS	VSS	AT32
AF24	VSS	VSS	AT34
AF26	VSS	VSS	AT39
AF27	VSS	VSS	AT42
AF29	VSS	VSS	AT46
AF31	VSS	VSS	AT7
AF38	VSS	VSS	AU24
AF4	VSS	VSS	AU30
AF42	VSS	VSS	AV11
AF46	VSS	VSS	AV16
AF5	VSS	VSS	AV20
AF7	VSS	VSS	AV24
AF8	VSS	VSS	AV30
AG19	VSS	VSS	AV38
AG2	VSS	VSS	AV4
AG31	VSS	VSS	AV43
AG48	VSS	VSS	AV8
AH11	VSS	VSS	AW14
AH3	VSS	VSS	AW18
AH36	VSS	VSS	AW2
AH39	VSS	VSS	AW22
AH40	VSS	VSS	AW26
AH42	VSS	VSS	AW28
AH46	VSS	VSS	AW32
AH7	VSS	VSS	AW34
AJ19	VSS	VSS	AW36
AJ21	VSS	VSS	AW40
AJ24	VSS	VSS	AW48
AJ33	VSS	VSS	AY12
AJ34	VSS	VSS	AY22
AK12	VSS	VSS	AY28
AK3	VSS		

OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
FCBGA
(10 OF 10)
VSS

AY4	VSS	VSS	H46
AY42	VSS	VSS	K18
AY46	VSS	VSS	K26
AY8	VSS	VSS	K39
B11	VSS	VSS	K46
B15	VSS	VSS	K7
B19	VSS	VSS	L18
B23	VSS	VSS	L2
B27	VSS	VSS	L20
B31	VSS	VSS	L26
B35	VSS	VSS	L28
B39	VSS	VSS	L36
B7	VSS	VSS	L48
F45	VSS	VSS	M12
BB12	VSS	VSS	P16
BB16	VSS	VSS	M18
BB20	VSS	VSS	M22
BB22	VSS	VSS	M24
BB24	VSS	VSS	M30
BB28	VSS	VSS	M32
BB30	VSS	VSS	M34
BB38	VSS	VSS	M38
BB4	VSS	VSS	M4
BB46	VSS	VSS	M42
BC14	VSS	VSS	M46
BC18	VSS	VSS	M8
BC2	VSS	VSS	N18
BC22	VSS	VSS	P30
BC26	VSS	VSS	N47
BC32	VSS	VSS	P11
BC34	VSS	VSS	P18
BC36	VSS	VSS	T33
BC40	VSS	VSS	P40
BC42	VSS	VSS	P43
BC48	VSS	VSS	P47
BD46	VSS	VSS	P7
BD5	VSS	VSS	R2
BE22	VSS	VSS	R48
BE26	VSS	VSS	T12
BE40	VSS	VSS	T31
BF10	VSS	VSS	T37
BF12	VSS	VSS	T4
BF16	VSS	VSS	W34
BF20	VSS	VSS	T46
BF22	VSS	VSS	T47
BF24	VSS	VSS	T8
BF26	VSS	VSS	V11
BF28	VSS	VSS	V17
BD3	VSS	VSS	V26
BF30	VSS	VSS	V27
BF38	VSS	VSS	V29
BF40	VSS	VSS	V31
BF8	VSS	VSS	V36
BG17	VSS	VSS	V39
BG21	VSS	VSS	V43
BG33	VSS	VSS	V7
BG44	VSS	VSS	W17
BG8	VSS	VSS	W19
BH11	VSS	VSS	W2
BH15	VSS	VSS	W27
BH17	VSS	VSS	W48
BH19	VSS	VSS	Y12
H10	VSS	VSS	Y38
BH27	VSS	VSS	Y4
BH31	VSS	VSS	Y42
BH33	VSS	VSS	Y46
BH35	VSS	VSS	Y8
BH39	VSS		
BH43	VSS		
BH7	VSS	VSS	BG29
D3	VSS	VSS	N24
D12	VSS	VSS	AJ3
D16	VSS	VSS	AD47
D18	VSS		
D22	VSS	VSS	B43
D24	VSS	VSS	BE10
D26	VSS	VSS	BG41
D30	VSS		
D32	VSS	VSS	G14
D34	VSS	VSS	H16
D38	VSS		
D42	VSS	VSS	T36
D8	VSS		
E18	VSS	VSS	BG22
E26	VSS	VSS	BG24
G18	VSS	VSS	C22
G20	VSS	VSS	AP13
G26	VSS	VSS	M14
G28	VSS	VSS	AP3
G36	VSS	VSS	AP1
G48	VSS	VSS	BE16
H12	VSS	VSS	BC16
H18	VSS	VSS	BG28
H22	VSS	VSS	BJ28
H24	VSS		
H26	VSS		
H30	VSS		
H32	VSS		
H34	VSS		
F3	VSS		

SYNC_MASTER=J5_MLB SYNC_DATE=03/21/2011

PAGE TITLE

PCH GROUNDS

Apple Inc.

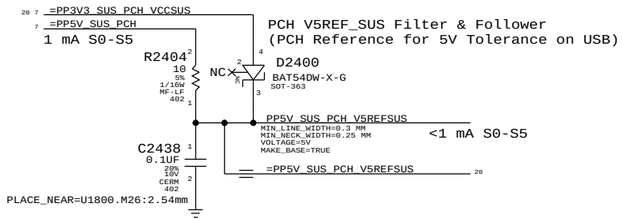
DRAWING NUMBER 051-9585 SIZE D

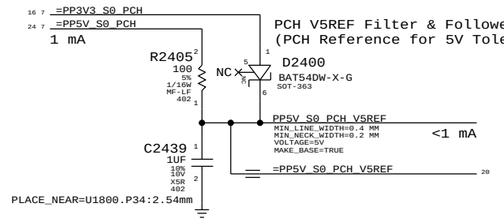
REVISION 3.0.0

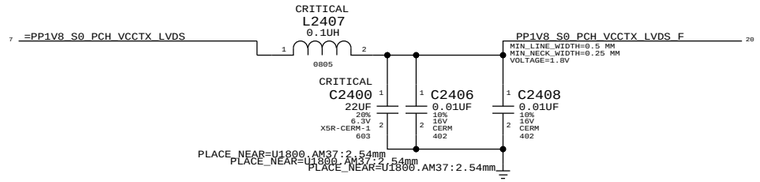
BRANCH

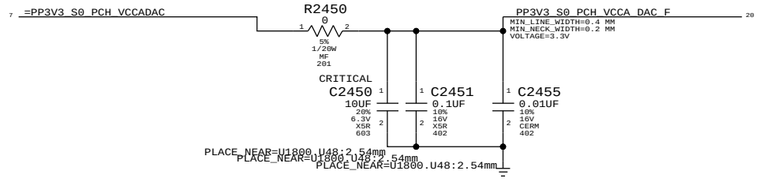
PAGE 23 OF 132

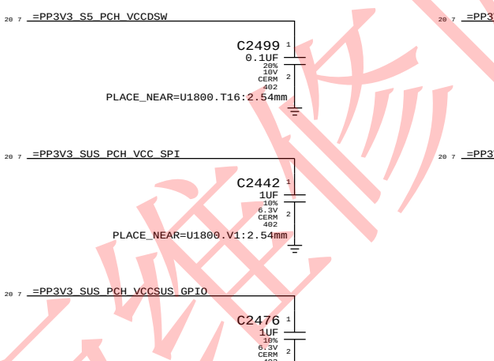
SHEET 21 OF 105

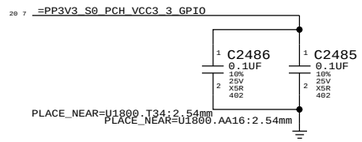


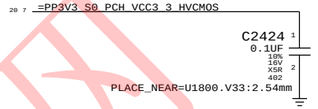


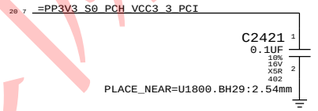


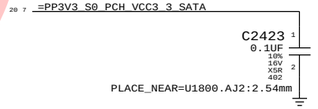


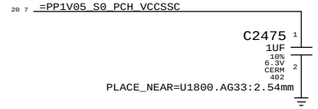


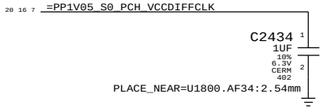


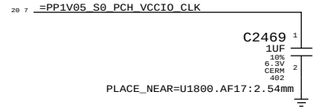


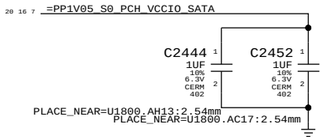


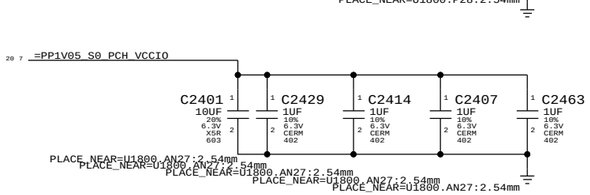


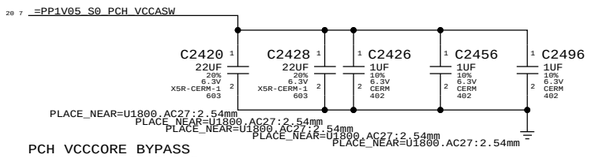


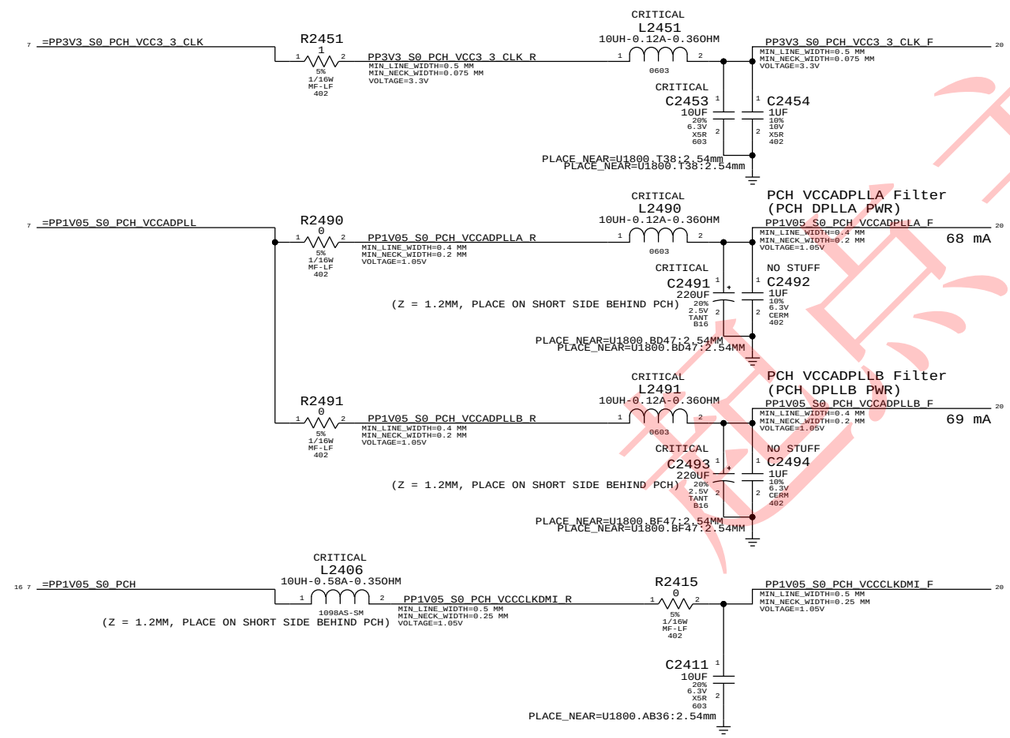


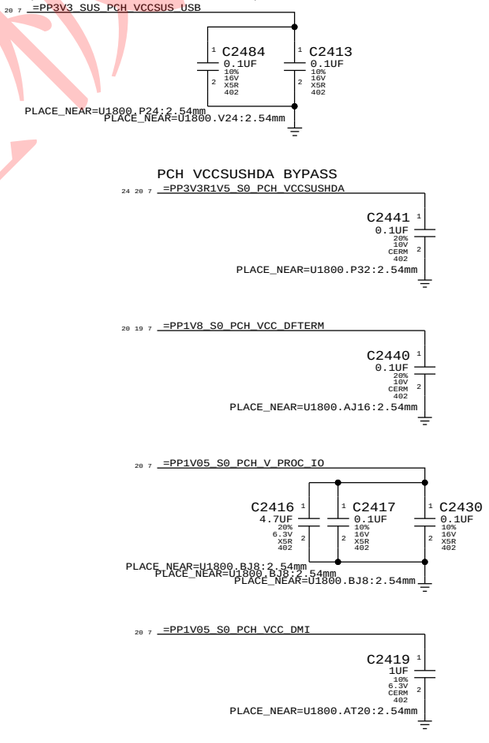












PCH VCCIO BYPASS

PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)

SYNC_MASTER=J5_MLB	SYNC_DATE=05/26/2011
PAGE TITLE	PCH DECOUPLING
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 24 OF 132
	SHEET 22 OF 105

CPU Micro2-XDP

CRITICAL
XDP_CONN_CPU
J2500
DF40RC-60DP-0.4V
M-ST-SM

23 7 =PPVCCIO_S0_XDP

7 =PP3V3_S0_XDP
NO STUFF
R2540 1K 5% 1/16W MF-LF 402

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

93 10 BI XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<16> IN 9 93
93 10 IN XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<17> IN 9 93
93 10 IN XDP_BPM_L<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<0> IN 9 23 93
93 10 IN XDP_BPM_L<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<1> IN 9 93
93 10 IN XDP_BPM_L<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<2> IN 9 93
93 10 IN XDP_BPM_L<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<3> IN 9 93
93 9 IN CPU_CFG<10>	OBSEN_B0	OBSEN_D0	CPU_CFG<8> IN 9 93
93 9 IN CPU_CFG<11>	OBSEN_B1	OBSEN_D1	CPU_CFG<9> IN 9 93
XDP_OBSDATA_B<0>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<4> IN 9 93
XDP_OBSDATA_B<1>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<5> IN 9 93
XDP_OBSDATA_B<2>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<6> IN 9 93
XDP_OBSDATA_B<3>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<7> IN 9 93
93 XDP_CPU_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	93 XDP_CPU_CLK100M_P
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	93 XDP_CPU_CLK100M_N
	VCC_OBS_AB	VCC_OBS_CD	
XDP_CPU_CFG<0>	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_VR_READY	HOOK3	DBR#/HOOK7	XDP_DBRESET_L OUT 10 23 24 93
		NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page	
48 23 BI =SMBUS_XDP_SDA	SDA	TDO	XDP_CPU_TDO IN 10 23 93
48 23 IN =SMBUS_XDP_SCL	SCL	TRSTn	XDP_CPU_TRST_L OUT 10 23 93
	TCK1	TDI	XDP_CPU_TDI OUT 10 23 93
93 23 10 OUT XDP_CPU_TCK	TCK0	TMS	XDP_CPU_TMS OUT 10 23 93
	NC	XDP_PRESENT#	

XDP C2500 0.1uF 10% 16V X5R 402 — XDP C2501 0.1uF 10% 16V X5R 402

998-2516

(R2560-R2563)
XDP_CPU:BPM

93 10 IN XDP_BPM_L<4>	R2560	0	5% 1/20W MF 201
93 10 IN XDP_BPM_L<5>	R2561	0	5% 1/20W MF 201
93 10 IN XDP_BPM_L<6>	R2562	0	5% 1/20W MF 201
93 10 IN XDP_BPM_L<7>	R2563	0	5% 1/20W MF 201

(R2564-R2567)
XDP_CPU:CFG

93 9 IN CPU_CFG<12>	R2564	0	5% 1/20W MF 201
93 9 IN CPU_CFG<13>	R2565	0	5% 1/20W MF 201
93 9 IN CPU_CFG<14>	R2566	0	5% 1/20W MF 201
93 9 IN CPU_CFG<15>	R2567	0	5% 1/20W MF 201

93 19 10 IN CPU_PWRGD	R2500	1K	XDP PLACE_NEAR=U1000.C60:2.54mm 5% 1/20W MF 201
45 23 17 OUT PM_PWRBTN_L	R2502	0	XDP PLACE_NEAR=U4900.P17:2.54mm 5% 1/20W MF 201
93 23 9 OUT CPU_CFG<0>	R2501	1K	XDP PLACE_NEAR=U1000.B57:2.54mm 5% 1/20W MF 201
92 45 17 OUT PM_PCH_SYS_PWROK	R2504	330	XDP 5% 1/20W MF 201

93 23 10 XDP_CPU_TDO	R2510	51	XDP PLACE_NEAR=J2500.52:2.54mm 5% 1/20W MF 201
93 23 10 XDP_CPU_TDI	R2511	51	XDP PLACE_NEAR=U1000.K61:2.54mm 5% 1/20W MF 201
93 23 10 XDP_CPU_TMS	R2512	51	XDP PLACE_NEAR=U1000.H59:2.54mm 5% 1/20W MF 201
93 23 10 XDP_CPU_TCK	R2513	51	XDP PLACE_NEAR=U1000.J58:2.54mm 5% 1/20W MF 201
93 23 10 XDP_CPU_TRST_L	R2514	51	XDP PLACE_NEAR=U1000.H63:2.54mm 5% 1/20W MF 201

R2515	0	XDP PLACE_NEAR=R1841.1:2.54mm ITPXDP_CLK100M_P 5% 1/20W MF 201	IN 16 93
R2516	0	XDP PLACE_NEAR=R1840.1:2.54mm ITPXDP_CLK100M_N 5% 1/20W MF 201	IN 16 93
R2505	1K	XDP PLACE_NEAR=U1000.G3:2.54mm CPU_RESET_L 5% 1/20W MF 201	IN 10 24

XDP SIGNALS

(R2520-R2537)
XDP

23 OUT XDP_DA0_USB_EXTA_OC_L	R2520	33	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	IN 18 23
23 OUT XDP_DA1_USB_EXTB_OC_L	R2521	33	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	IN 18 23
23 OUT XDP_DA2_USB_EXTC_OC_L	R2522	33	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L	IN 18
23 OUT XDP_DA3_USB_EXTD_OC_L	R2523	33	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L	IN 18 23
23 OUT XDP_DB0_USB_EXTB_OC_EHCI_L	R2524	33	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L	IN 18 23
23 OUT XDP_DB1_USB_EXTD_OC_EHCI_L	R2525	33	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L	IN 18 23
23 IN XDP_DB2_AP_PWR_EN	R2526	33	XDP_DB2_PCH_GPIO10_AP_PWR_EN	OUT 18 23
23 OUT XDP_DB3_SDCONN_STATE_CHANGE	R2527	33	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	IN 18 23
23 OUT XDP_FC0	R2528	33	XDP_FC0_PCH_GPIO15	IN 19 68
23 OUT XDP_FC1	R2529	33	XDP_FC1_PCH_GPIO0	IN 19
23 IN XDP_DC0_ISOLATE_CPU_MEM_L	R2530	33	XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	OUT 19 23
23 IN XDP_DC1_MXM_GOOD	R2531	33	XDP_DC1_PCH_GPIO35_MXM_GOOD	OUT 19
23 IN XDP_DC2_DP_AUXCH_ISOL	R2532	33	XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	OUT 16 23
23 IN XDP_DC3_SATARDRVR_EN	R2533	33	XDP_DC3_PCH_GPIO19_SATARDRVR_EN	OUT 16 23
23 IN XDP_DD0_DP_GPU_TBT_SEL	R2534	33	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL	OUT 19
23 IN XDP_DD1_JTAG_ISP_TCK	R2535	33	XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	OUT 19 23
23 IN XDP_DD2_AUD_IPHS_SWITCH_EN	R2536	33	XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	OUT 19 23
23 IN XDP_DD3_ENET_LOW_PWR	R2537	33	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	OUT 19 23

PCH SIGNALS

23 18 OUT XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	R2590	0	USB_EXTA_OC_L IN 42
23 18 OUT XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2591	0	USB_EXTB_OC_L IN 42
23 18 IN XDP_DB2_PCH_GPIO10_AP_PWR_EN	R2596	0	AP_PWR_EN OUT 18 32 74
23 18 OUT XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	R2597	0	SDCONN_STATE_CHANGE IN 24
23 16 IN XDP_DC3_PCH_GPIO19_SATARDRVR_EN	R2573	0	SATARDRVR_EN OUT 16 41
23 19 OUT XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	R2570	0	ISOLATE_CPU_MEM_L OUT 26
23 16 IN XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	R2572	0	DP_AUXCH_ISOL OUT 16 87

Non-XDP Signals

23 19 OUT XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	R2575	0	JTAG_ISP_TCK OUT 8 19
23 19 OUT XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	R2576	0	AUD_IPHS_SWITCH_EN_PCH OUT 19 24
23 19 OUT XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	R2577	0	ENET_LOW_PWR_PCH OUT 19 24

PCH Micro2-XDP

CRITICAL
XDP_CONN_PCH
J2550
DF40RC-60DP-0.4V
M-ST-SM

=PP3V3_S5_XDP 7

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

	TP_XDP_PCH_OBSFN_A<0>	OBSEN_A0	OBSEN_C0	XDP_FC0	23
	TP_XDP_PCH_OBSFN_A<1>	OBSEN_A1	OBSEN_C1	XDP_FC1	23
23 XDP_DA0_USB_EXTA_OC_L		OBSDATA_A0	OBSDATA_C0	XDP_DC0_ISOLATE_CPU_MEM_L	23
23 XDP_DA1_USB_EXTB_OC_L		OBSDATA_A1	OBSDATA_C1	XDP_DC1_MXM_GOOD	23
23 XDP_DA2_USB_EXTC_OC_L		OBSDATA_A2	OBSDATA_C2	XDP_DC2_DP_AUXCH_ISOL	23
23 XDP_DA3_USB_EXTD_OC_L		OBSDATA_A3	OBSDATA_C3	XDP_DC3_SATARDRVR_EN	23
	TP_XDP_PCH_OBSFN_B<0>	OBSEN_B0	OBSEN_D0	TP_XDP_PCH_OBSFN_D<0>	
	TP_XDP_PCH_OBSFN_B<1>	OBSEN_B1	OBSEN_D1	TP_XDP_PCH_OBSFN_D<1>	
23 XDP_DB0_USB_EXTB_OC_EHCI_L		OBSDATA_B0	OBSDATA_D0	XDP_DD0_DP_GPU_TBT_SEL	23
23 XDP_DB1_USB_EXTD_OC_EHCI_L		OBSDATA_B1	OBSDATA_D1	XDP_DD1_JTAG_ISP_TCK	23
23 XDP_DB2_AP_PWR_EN		OBSDATA_B2	OBSDATA_D2	XDP_DD2_AUD_IPHS_SWITCH_EN	23
23 XDP_DB3_SDCONN_STATE_CHANGE		OBSDATA_B3	OBSDATA_D3	XDP_DD3_ENET_LOW_PWR	23
92 89 74 45 IN ALL_SYS_PWRGD		PWRGD/HOOK0	ITPCLK/HOOK4	TP_XDP_PCH_HOOK4	
XDP_PCH_PWRBTN_L		HOOK1	ITPCLK#/HOOK5	TP_XDP_PCH_HOOK5	
		VCC_OBS_AB	VCC_OBS_CD		
6 TP_XDPPCH_HOOK2		HOOK2	RESET#/HOOK6	XDPPCH_PLTRST_L	IN 24
6 TP_XDPPCH_HOOK3		HOOK3	DBR#/HOOK7	XDP_DBRESET_L	OUT 10 23 24 93
			NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page		
48 23 BI =SMBUS_XDP_SDA		SDA	TDO	XDP_PCH_TDO	IN 16 23
48 23 IN =SMBUS_XDP_SCL		SCL	TRSTn	TP_XDP_PCH_TRST_L	
		TCK1	TDI	XDP_PCH_TDI	OUT 16 23
23 16 OUT XDP_PCH_TCK		TCK0	TMS	XDP_PCH_TMS	OUT 16 23
		NC	XDP_PRESENT#		

XDP C2580 0.1uF 10% 16V X5R 402 — XDP C2581 0.1uF 10% 16V X5R 402

998-2516

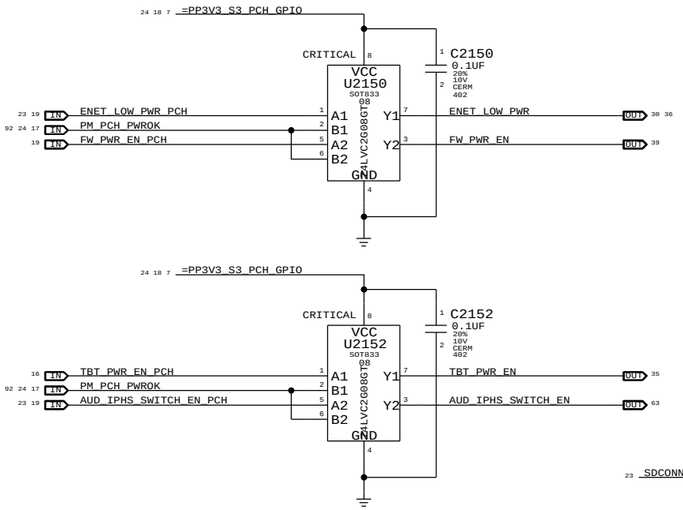
1K series R on PCH Support Page

23 18 XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2580	1K	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L 18 23
23 18 XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L	R2581	1K	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L 18 23

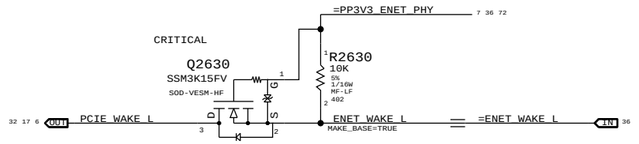
23 16 XDP_PCH_TDO	R2550	51	XDP PLACE_NEAR=J2550.52:2.54mm 5% 1/20W MF 201	7 =PP1V05_SUS_PCH_JTAG		
23 16 XDP_PCH_TDI	R2551	51	XDP PLACE_NEAR=U1800.K5:2.54mm 5% 1/20W MF 201			
23 16 XDP_PCH_TMS	R2552	51	XDP PLACE_NEAR=U1800.H7:2.54mm 5% 1/20W MF 201			
23 16 XDP_PCH_TCK	R2556	51	XDP PLACE_NEAR=U1800.J3:2.54mm 5% 1/20W MF 201			

SYNC_MASTER=J31_ANNE	SYNC_DATE=06/09/2011
PAGE TITLE	CPU & PCH XDP
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 25 OF 132
	SHEET 23 OF 105

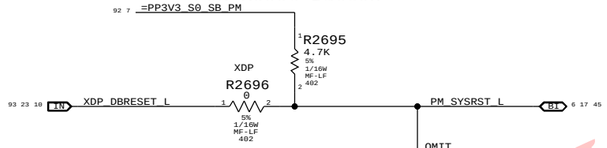
GPIO Glitch Prevention



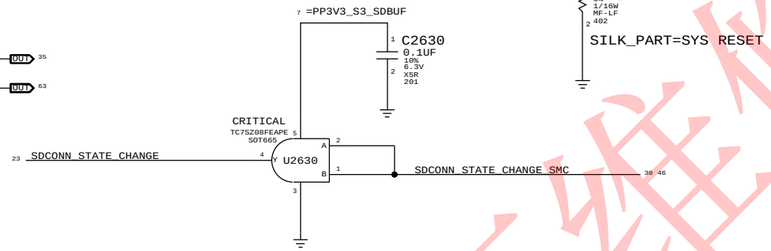
Ethernet WAKE# Isolation



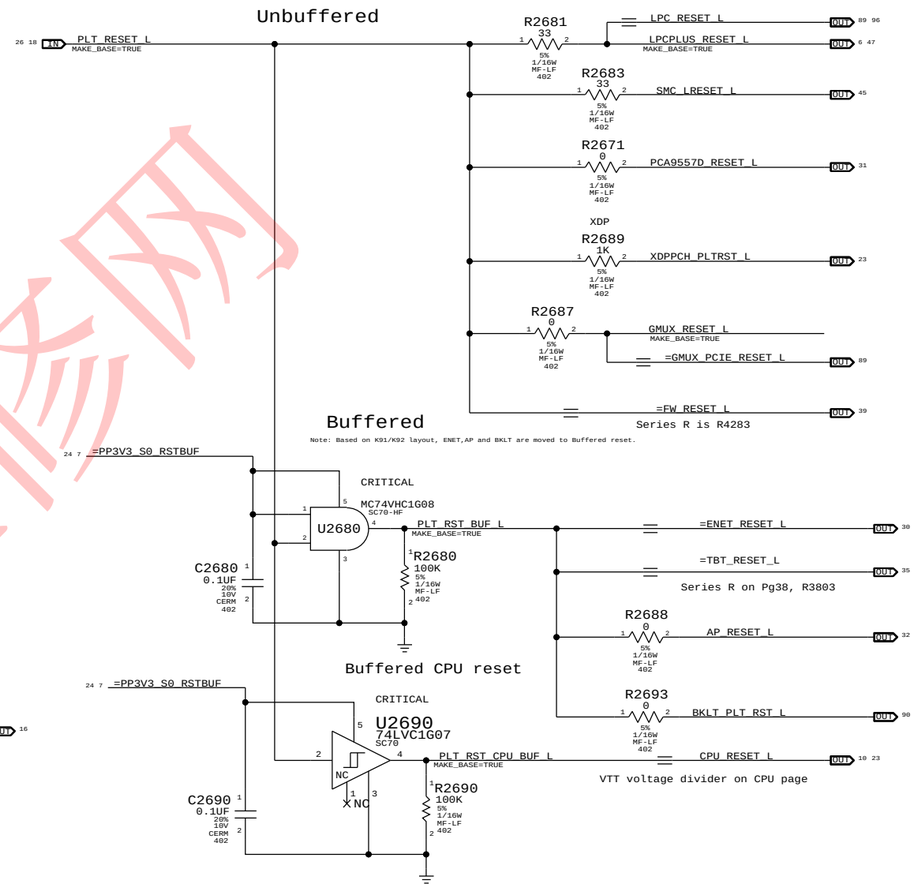
PCH Reset Button



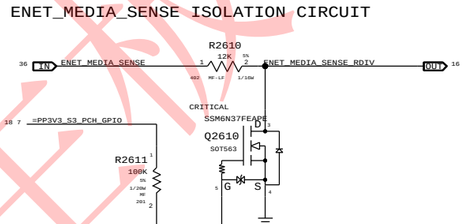
SDCONN_STATE_CHANGE



Platform Reset Connections



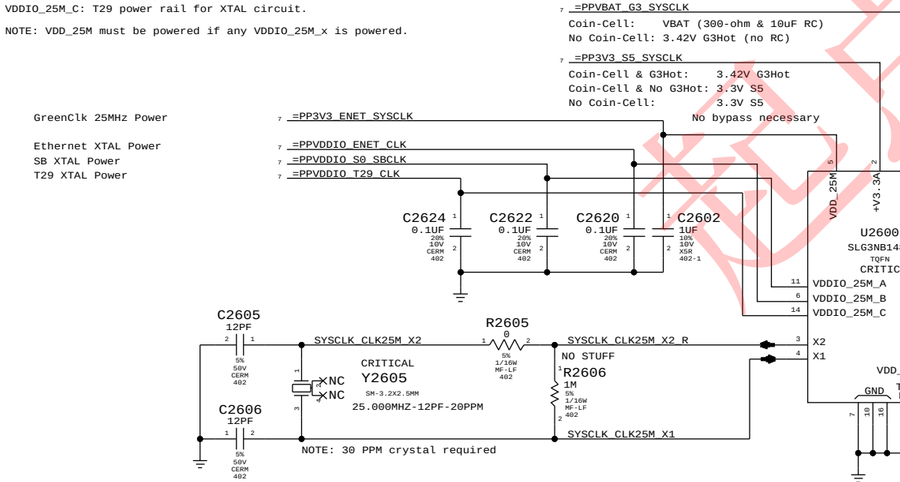
ENET_MEDIA_SENSE_ISOLATION_CIRCUIT



System RTC Power Source & 32kHz / 25MHz Clock Generator

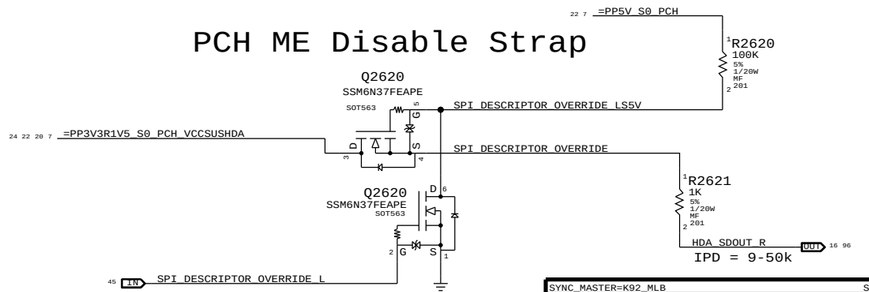
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC_MASTER=K92_MLB	SYNC_DATE=07/06/2010
PAGE TITLE	Chipset Support
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D · REVISION 3.0.0 · BRANCH · PAGE 26 OF 132 · SHEET 24 OF 105

USB MUX FOR LS/FS INTERNAL DEVICES

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

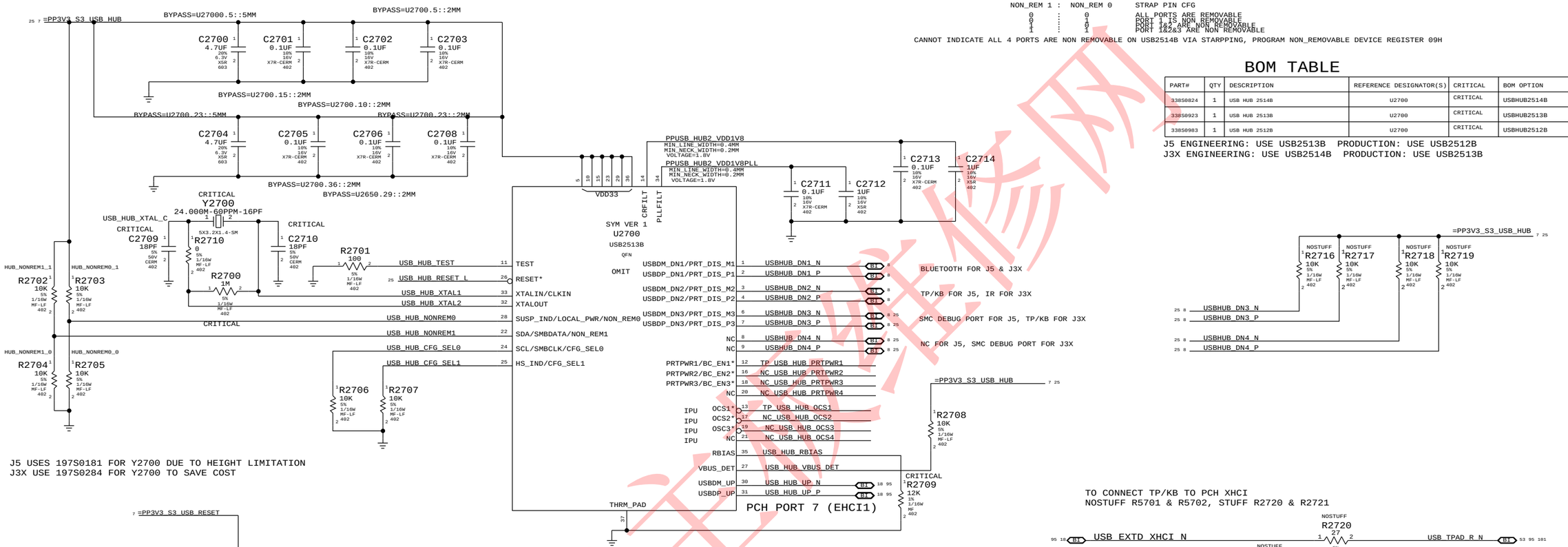
NON_REM 1	NON_REM 0	STRAP PIN CFG
0	0	ALL PORTS ARE REMOVABLE
0	1	PORT 1 IS NON REMOVABLE
1	0	PORT 2&3 ARE NON REMOVABLE
1	1	PORT 1&2&3 ARE NON REMOVABLE

CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STARPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

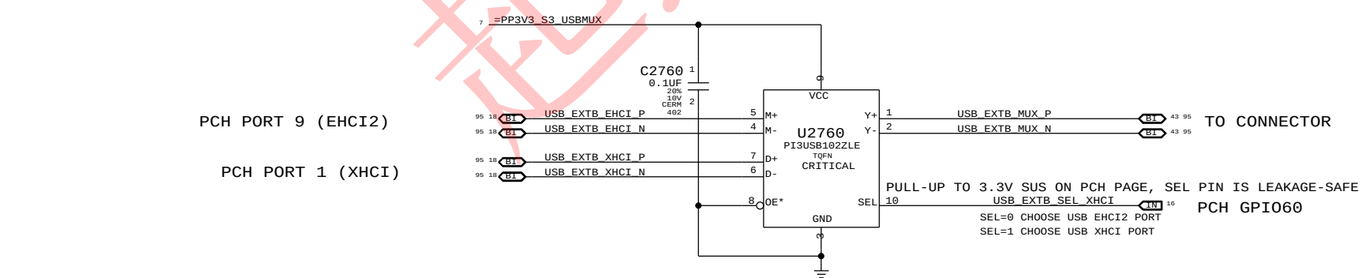
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB2512B

J5 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



USB XHCI/EHCI2 PORT MUX FOR EXT B

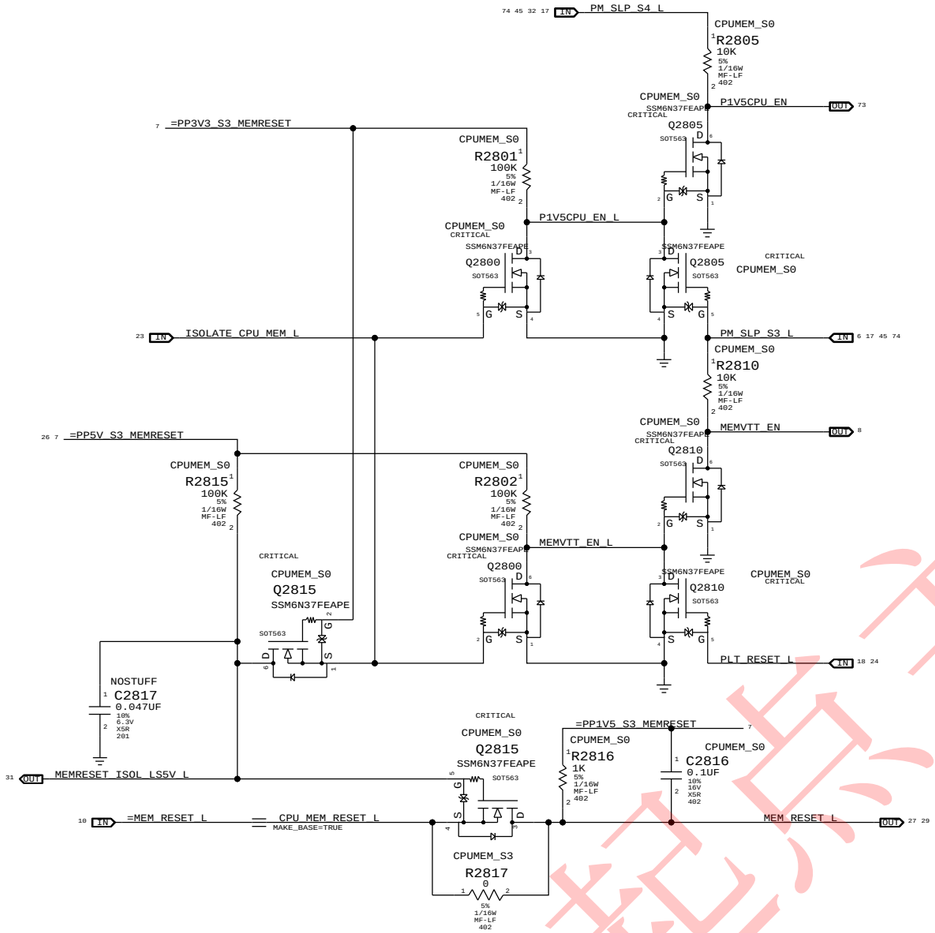


SYNC_MASTER=J31_LINDA	SYNC_DATE=09/16/2011
PAGE TITLE	USB HUB & MUX
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 27 OF 132
	SHEET 25 OF 105

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

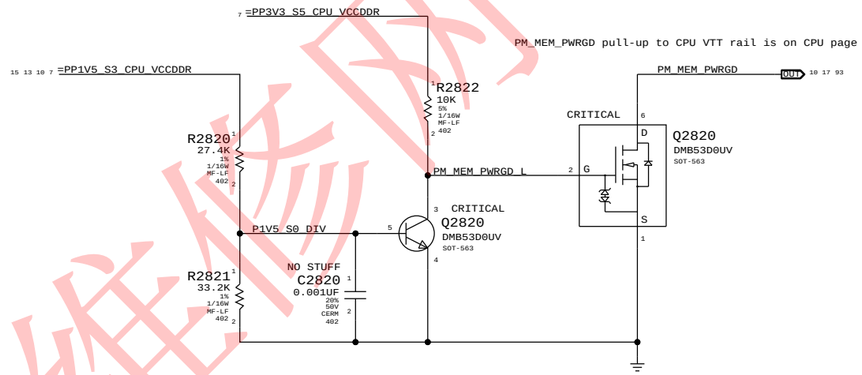


	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

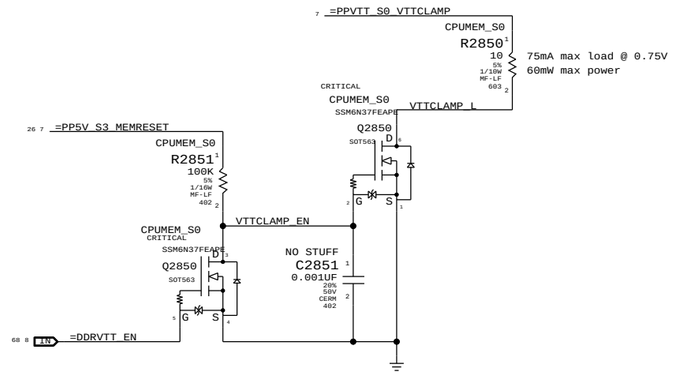
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=K18_MLB	SYNC_DATE=04/27/2010
PAGE TITLE	CPU Memory S3 Support
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 28 OF 132
	SHEET 26 OF 105

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

7 =PP1V5_S3_MEM_A

C2900 10UF 20% 6.3V X5R 603
C2901 10UF 20% 6.3V X5R 603
PLACE_NEAR=J2900.75:2.54mm

C2910 C2911 C2912 C2913 C2914 C2915 C2916 C2917 C2918 C2919 C2920 C2921 C2922 C2923
0.1UF 20% 10V CERM 402
PLACE_NEAR=J2900.75:2.54mm

93 31 PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

OMIT_TABLE

J2900 F-RT-THB
DDR3_SODIMM-DUAL-K6 (SYMBOL 2 OF 2)

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204

KEY

NC ×
×NC

J2900 F-RT-THB
DDR3_SODIMM-DUAL-K6 (SYMBOL 1 OF 2)

1	VREFDQ	VSS	2
3	VSS	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS	8
9	VSS	DQS0*	10
11	DM0	DQS0	12
13	VSS	VSS	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS	VSS	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS	VSS	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS	VSS	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS	VSS	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS	VSS	44
45	DQS2*	DM2	46
47	DQS2	VSS	48
49	VSS	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS	54
55	VSS	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS	60
61	VSS	DQS3*	62
63	DM3	DQS3	64
65	VSS	VSS	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS	VSS	72

KEY

CRITICAL

See CSA05 BOM table

PP0V75_S3_MEM_VREFCA_A 31 93

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

"Factory" (top) slot

=PPSPD_S0_MEM_A

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

6 MEM_A_SA<0>
6 MEM_A_SA<1>

516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

=PP0V75_S0_MEM_VTT_A 7

C2950 C2951 C2952 C2953
1UF 10% 10V X5R 402

SYNC_MASTER=K92_SUMA	SYNC_DATE=06/23/2010
PAGE TITLE	DDR3 SO-DIMM Connector A
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 29 OF 132
	SHEET 27 OF 105

CPU CHANNEL A DQS 0 -> DIMM A DQS 0

94 11 6 MEM_A_DQS_N<0> MAKE_BASE=TRUE =MEM_A_DQS_N<0> 27
94 11 6 MEM_A_DQS_P<0> MAKE_BASE=TRUE =MEM_A_DQS_P<0> 27

94 11 6 MEM_A_DQ<7> MAKE_BASE=TRUE =MEM_A_DQ<3> 27
94 11 6 MEM_A_DQ<6> MAKE_BASE=TRUE =MEM_A_DQ<6> 27
94 11 6 MEM_A_DQ<5> MAKE_BASE=TRUE =MEM_A_DQ<5> 27
94 11 6 MEM_A_DQ<4> MAKE_BASE=TRUE =MEM_A_DQ<4> 27
94 11 6 MEM_A_DQ<3> MAKE_BASE=TRUE =MEM_A_DQ<7> 27
94 11 6 MEM_A_DQ<2> MAKE_BASE=TRUE =MEM_A_DQ<0> 27
94 11 6 MEM_A_DQ<1> MAKE_BASE=TRUE =MEM_A_DQ<1> 27
94 11 6 MEM_A_DQ<0> MAKE_BASE=TRUE =MEM_A_DQ<2> 27

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

94 11 6 MEM_A_DQS_N<1> MAKE_BASE=TRUE =MEM_A_DQS_N<1> 27
94 11 6 MEM_A_DQS_P<1> MAKE_BASE=TRUE =MEM_A_DQS_P<1> 27

94 11 6 MEM_A_DQ<15> MAKE_BASE=TRUE =MEM_A_DQ<15> 27
94 11 6 MEM_A_DQ<14> MAKE_BASE=TRUE =MEM_A_DQ<14> 27
94 11 6 MEM_A_DQ<13> MAKE_BASE=TRUE =MEM_A_DQ<12> 27
94 11 6 MEM_A_DQ<12> MAKE_BASE=TRUE =MEM_A_DQ<13> 27
94 11 6 MEM_A_DQ<11> MAKE_BASE=TRUE =MEM_A_DQ<10> 27
94 11 6 MEM_A_DQ<10> MAKE_BASE=TRUE =MEM_A_DQ<11> 27
94 11 6 MEM_A_DQ<9> MAKE_BASE=TRUE =MEM_A_DQ<9> 27
94 11 6 MEM_A_DQ<8> MAKE_BASE=TRUE =MEM_A_DQ<8> 27

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

94 11 6 MEM_A_DQS_N<2> MAKE_BASE=TRUE =MEM_A_DQS_N<2> 27
94 11 6 MEM_A_DQS_P<2> MAKE_BASE=TRUE =MEM_A_DQS_P<2> 27

94 11 6 MEM_A_DQ<23> MAKE_BASE=TRUE =MEM_A_DQ<23> 27
94 11 6 MEM_A_DQ<22> MAKE_BASE=TRUE =MEM_A_DQ<22> 27
94 11 6 MEM_A_DQ<21> MAKE_BASE=TRUE =MEM_A_DQ<17> 27
94 11 6 MEM_A_DQ<20> MAKE_BASE=TRUE =MEM_A_DQ<20> 27
94 11 6 MEM_A_DQ<19> MAKE_BASE=TRUE =MEM_A_DQ<19> 27
94 11 6 MEM_A_DQ<18> MAKE_BASE=TRUE =MEM_A_DQ<18> 27
94 11 6 MEM_A_DQ<17> MAKE_BASE=TRUE =MEM_A_DQ<16> 27
94 11 6 MEM_A_DQ<16> MAKE_BASE=TRUE =MEM_A_DQ<21> 27

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

94 11 6 MEM_A_DQS_N<3> MAKE_BASE=TRUE =MEM_A_DQS_N<3> 27
94 11 6 MEM_A_DQS_P<3> MAKE_BASE=TRUE =MEM_A_DQS_P<3> 27

94 11 6 MEM_A_DQ<31> MAKE_BASE=TRUE =MEM_A_DQ<31> 27
94 11 6 MEM_A_DQ<30> MAKE_BASE=TRUE =MEM_A_DQ<30> 27
94 11 6 MEM_A_DQ<29> MAKE_BASE=TRUE =MEM_A_DQ<29> 27
94 11 6 MEM_A_DQ<28> MAKE_BASE=TRUE =MEM_A_DQ<28> 27
94 11 6 MEM_A_DQ<27> MAKE_BASE=TRUE =MEM_A_DQ<27> 27
94 11 6 MEM_A_DQ<26> MAKE_BASE=TRUE =MEM_A_DQ<26> 27
94 11 6 MEM_A_DQ<25> MAKE_BASE=TRUE =MEM_A_DQ<25> 27
94 11 6 MEM_A_DQ<24> MAKE_BASE=TRUE =MEM_A_DQ<24> 27

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

94 11 6 MEM_A_DQS_N<4> MAKE_BASE=TRUE =MEM_A_DQS_N<4> 27
94 11 6 MEM_A_DQS_P<4> MAKE_BASE=TRUE =MEM_A_DQS_P<4> 27

94 11 6 MEM_A_DQ<39> MAKE_BASE=TRUE =MEM_A_DQ<38> 27
94 11 6 MEM_A_DQ<38> MAKE_BASE=TRUE =MEM_A_DQ<37> 27
94 11 6 MEM_A_DQ<37> MAKE_BASE=TRUE =MEM_A_DQ<39> 27
94 11 6 MEM_A_DQ<36> MAKE_BASE=TRUE =MEM_A_DQ<33> 27
94 11 6 MEM_A_DQ<35> MAKE_BASE=TRUE =MEM_A_DQ<35> 27
94 11 6 MEM_A_DQ<34> MAKE_BASE=TRUE =MEM_A_DQ<34> 27
94 11 6 MEM_A_DQ<33> MAKE_BASE=TRUE =MEM_A_DQ<32> 27
94 11 6 MEM_A_DQ<32> MAKE_BASE=TRUE =MEM_A_DQ<36> 27

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

94 11 6 MEM_A_DQS_N<5> MAKE_BASE=TRUE =MEM_A_DQS_N<5> 27
94 11 6 MEM_A_DQS_P<5> MAKE_BASE=TRUE =MEM_A_DQS_P<5> 27

94 11 6 MEM_A_DQ<47> MAKE_BASE=TRUE =MEM_A_DQ<47> 27
94 11 6 MEM_A_DQ<46> MAKE_BASE=TRUE =MEM_A_DQ<41> 27
94 11 6 MEM_A_DQ<45> MAKE_BASE=TRUE =MEM_A_DQ<43> 27
94 11 6 MEM_A_DQ<44> MAKE_BASE=TRUE =MEM_A_DQ<44> 27
94 11 6 MEM_A_DQ<43> MAKE_BASE=TRUE =MEM_A_DQ<40> 27
94 11 6 MEM_A_DQ<42> MAKE_BASE=TRUE =MEM_A_DQ<46> 27
94 11 6 MEM_A_DQ<41> MAKE_BASE=TRUE =MEM_A_DQ<42> 27
94 11 6 MEM_A_DQ<40> MAKE_BASE=TRUE =MEM_A_DQ<45> 27

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

94 11 6 MEM_A_DQS_N<6> MAKE_BASE=TRUE =MEM_A_DQS_N<6> 27
94 11 6 MEM_A_DQS_P<6> MAKE_BASE=TRUE =MEM_A_DQS_P<6> 27

94 11 6 MEM_A_DQ<55> MAKE_BASE=TRUE =MEM_A_DQ<49> 27
94 11 6 MEM_A_DQ<54> MAKE_BASE=TRUE =MEM_A_DQ<54> 27
94 11 6 MEM_A_DQ<53> MAKE_BASE=TRUE =MEM_A_DQ<55> 27
94 11 6 MEM_A_DQ<52> MAKE_BASE=TRUE =MEM_A_DQ<52> 27
94 11 6 MEM_A_DQ<51> MAKE_BASE=TRUE =MEM_A_DQ<51> 27
94 11 6 MEM_A_DQ<50> MAKE_BASE=TRUE =MEM_A_DQ<50> 27
94 11 6 MEM_A_DQ<49> MAKE_BASE=TRUE =MEM_A_DQ<53> 27
94 11 6 MEM_A_DQ<48> MAKE_BASE=TRUE =MEM_A_DQ<48> 27

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

94 11 6 MEM_A_DQS_N<7> MAKE_BASE=TRUE =MEM_A_DQS_N<7> 27
94 11 6 MEM_A_DQS_P<7> MAKE_BASE=TRUE =MEM_A_DQS_P<7> 27

94 11 6 MEM_A_DQ<63> MAKE_BASE=TRUE =MEM_A_DQ<59> 27
94 11 6 MEM_A_DQ<62> MAKE_BASE=TRUE =MEM_A_DQ<58> 27
94 11 6 MEM_A_DQ<61> MAKE_BASE=TRUE =MEM_A_DQ<56> 27
94 11 6 MEM_A_DQ<60> MAKE_BASE=TRUE =MEM_A_DQ<61> 27
94 11 6 MEM_A_DQ<59> MAKE_BASE=TRUE =MEM_A_DQ<63> 27
94 11 6 MEM_A_DQ<58> MAKE_BASE=TRUE =MEM_A_DQ<62> 27
94 11 6 MEM_A_DQ<57> MAKE_BASE=TRUE =MEM_A_DQ<57> 27
94 11 6 MEM_A_DQ<56> MAKE_BASE=TRUE =MEM_A_DQ<60> 27

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

94 11 6 MEM_B_DQS_N<0> MAKE_BASE=TRUE =MEM_B_DQS_N<0> 29
94 11 6 MEM_B_DQS_P<0> MAKE_BASE=TRUE =MEM_B_DQS_P<0> 29

94 11 6 MEM_B_DQ<7> MAKE_BASE=TRUE =MEM_B_DQ<6> 29
94 11 6 MEM_B_DQ<6> MAKE_BASE=TRUE =MEM_B_DQ<3> 29
94 11 6 MEM_B_DQ<5> MAKE_BASE=TRUE =MEM_B_DQ<5> 29
94 11 6 MEM_B_DQ<4> MAKE_BASE=TRUE =MEM_B_DQ<4> 29
94 11 6 MEM_B_DQ<3> MAKE_BASE=TRUE =MEM_B_DQ<1> 29
94 11 6 MEM_B_DQ<2> MAKE_BASE=TRUE =MEM_B_DQ<7> 29
94 11 6 MEM_B_DQ<1> MAKE_BASE=TRUE =MEM_B_DQ<2> 29
94 11 6 MEM_B_DQ<0> MAKE_BASE=TRUE =MEM_B_DQ<0> 29

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

94 11 6 MEM_B_DQS_N<1> MAKE_BASE=TRUE =MEM_B_DQS_N<1> 29
94 11 6 MEM_B_DQS_P<1> MAKE_BASE=TRUE =MEM_B_DQS_P<1> 29

94 11 6 MEM_B_DQ<15> MAKE_BASE=TRUE =MEM_B_DQ<15> 29
94 11 6 MEM_B_DQ<14> MAKE_BASE=TRUE =MEM_B_DQ<14> 29
94 11 6 MEM_B_DQ<13> MAKE_BASE=TRUE =MEM_B_DQ<13> 29
94 11 6 MEM_B_DQ<12> MAKE_BASE=TRUE =MEM_B_DQ<12> 29
94 11 6 MEM_B_DQ<11> MAKE_BASE=TRUE =MEM_B_DQ<11> 29
94 11 6 MEM_B_DQ<10> MAKE_BASE=TRUE =MEM_B_DQ<10> 29
94 11 6 MEM_B_DQ<9> MAKE_BASE=TRUE =MEM_B_DQ<9> 29
94 11 6 MEM_B_DQ<8> MAKE_BASE=TRUE =MEM_B_DQ<8> 29

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

94 11 6 MEM_B_DQS_N<2> MAKE_BASE=TRUE =MEM_B_DQS_N<2> 29
94 11 6 MEM_B_DQS_P<2> MAKE_BASE=TRUE =MEM_B_DQS_P<2> 29

94 11 6 MEM_B_DQ<23> MAKE_BASE=TRUE =MEM_B_DQ<23> 29
94 11 6 MEM_B_DQ<22> MAKE_BASE=TRUE =MEM_B_DQ<22> 29
94 11 6 MEM_B_DQ<21> MAKE_BASE=TRUE =MEM_B_DQ<21> 29
94 11 6 MEM_B_DQ<20> MAKE_BASE=TRUE =MEM_B_DQ<20> 29
94 11 6 MEM_B_DQ<19> MAKE_BASE=TRUE =MEM_B_DQ<19> 29
94 11 6 MEM_B_DQ<18> MAKE_BASE=TRUE =MEM_B_DQ<18> 29
94 11 6 MEM_B_DQ<17> MAKE_BASE=TRUE =MEM_B_DQ<17> 29
94 11 6 MEM_B_DQ<16> MAKE_BASE=TRUE =MEM_B_DQ<16> 29

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

94 11 6 MEM_B_DQS_N<3> MAKE_BASE=TRUE =MEM_B_DQS_N<3> 29
94 11 6 MEM_B_DQS_P<3> MAKE_BASE=TRUE =MEM_B_DQS_P<3> 29

94 11 6 MEM_B_DQ<31> MAKE_BASE=TRUE =MEM_B_DQ<31> 29
94 11 6 MEM_B_DQ<30> MAKE_BASE=TRUE =MEM_B_DQ<30> 29
94 11 6 MEM_B_DQ<29> MAKE_BASE=TRUE =MEM_B_DQ<29> 29
94 11 6 MEM_B_DQ<28> MAKE_BASE=TRUE =MEM_B_DQ<28> 29
94 11 6 MEM_B_DQ<27> MAKE_BASE=TRUE =MEM_B_DQ<27> 29
94 11 6 MEM_B_DQ<26> MAKE_BASE=TRUE =MEM_B_DQ<26> 29
94 11 6 MEM_B_DQ<25> MAKE_BASE=TRUE =MEM_B_DQ<25> 29
94 11 6 MEM_B_DQ<24> MAKE_BASE=TRUE =MEM_B_DQ<24> 29

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

94 11 6 MEM_B_DQS_N<4> MAKE_BASE=TRUE =MEM_B_DQS_N<4> 29
94 11 6 MEM_B_DQS_P<4> MAKE_BASE=TRUE =MEM_B_DQS_P<4> 29

94 11 6 MEM_B_DQ<39> MAKE_BASE=TRUE =MEM_B_DQ<39> 29
94 11 6 MEM_B_DQ<38> MAKE_BASE=TRUE =MEM_B_DQ<38> 29
94 11 6 MEM_B_DQ<37> MAKE_BASE=TRUE =MEM_B_DQ<37> 29
94 11 6 MEM_B_DQ<36> MAKE_BASE=TRUE =MEM_B_DQ<36> 29
94 11 6 MEM_B_DQ<35> MAKE_BASE=TRUE =MEM_B_DQ<35> 29
94 11 6 MEM_B_DQ<34> MAKE_BASE=TRUE =MEM_B_DQ<34> 29
94 11 6 MEM_B_DQ<33> MAKE_BASE=TRUE =MEM_B_DQ<33> 29
94 11 6 MEM_B_DQ<32> MAKE_BASE=TRUE =MEM_B_DQ<32> 29

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

94 11 6 MEM_B_DQS_N<5> MAKE_BASE=TRUE =MEM_B_DQS_N<5> 29
94 11 6 MEM_B_DQS_P<5> MAKE_BASE=TRUE =MEM_B_DQS_P<5> 29

94 11 6 MEM_B_DQ<47> MAKE_BASE=TRUE =MEM_B_DQ<47> 29
94 11 6 MEM_B_DQ<46> MAKE_BASE=TRUE =MEM_B_DQ<46> 29
94 11 6 MEM_B_DQ<45> MAKE_BASE=TRUE =MEM_B_DQ<45> 29
94 11 6 MEM_B_DQ<44> MAKE_BASE=TRUE =MEM_B_DQ<44> 29
94 11 6 MEM_B_DQ<43> MAKE_BASE=TRUE =MEM_B_DQ<43> 29
94 11 6 MEM_B_DQ<42> MAKE_BASE=TRUE =MEM_B_DQ<42> 29
94 11 6 MEM_B_DQ<41> MAKE_BASE=TRUE =MEM_B_DQ<41> 29
94 11 6 MEM_B_DQ<40> MAKE_BASE=TRUE =MEM_B_DQ<40> 29

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

94 11 6 MEM_B_DQS_N<6> MAKE_BASE=TRUE =MEM_B_DQS_N<6> 29
94 11 6 MEM_B_DQS_P<6> MAKE_BASE=TRUE =MEM_B_DQS_P<6> 29

94 11 6 MEM_B_DQ<55> MAKE_BASE=TRUE =MEM_B_DQ<55> 29
94 11 6 MEM_B_DQ<54> MAKE_BASE=TRUE =MEM_B_DQ<54> 29
94 11 6 MEM_B_DQ<53> MAKE_BASE=TRUE =MEM_B_DQ<53> 29
94 11 6 MEM_B_DQ<52> MAKE_BASE=TRUE =MEM_B_DQ<52> 29
94 11 6 MEM_B_DQ<51> MAKE_BASE=TRUE =MEM_B_DQ<51> 29
94 11 6 MEM_B_DQ<50> MAKE_BASE=TRUE =MEM_B_DQ<50> 29
94 11 6 MEM_B_DQ<49> MAKE_BASE=TRUE =MEM_B_DQ<49> 29
94 11 6 MEM_B_DQ<48> MAKE_BASE=TRUE =MEM_B_DQ<48> 29

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

94 11 6 MEM_B_DQS_N<7> MAKE_BASE=TRUE =MEM_B_DQS_N<7> 29
94 11 6 MEM_B_DQS_P<7> MAKE_BASE=TRUE =MEM_B_DQS_P<7> 29

94 11 6 MEM_B_DQ<63> MAKE_BASE=TRUE =MEM_B_DQ<63> 29
94 11 6 MEM_B_DQ<62> MAKE_BASE=TRUE =MEM_B_DQ<62> 29
94 11 6 MEM_B_DQ<61> MAKE_BASE=TRUE =MEM_B_DQ<61> 29
94 11 6 MEM_B_DQ<60> MAKE_BASE=TRUE =MEM_B_DQ<60> 29
94 11 6 MEM_B_DQ<59> MAKE_BASE=TRUE =MEM_B_DQ<59> 29
94 11 6 MEM_B_DQ<58> MAKE_BASE=TRUE =MEM_B_DQ<58> 29
94 11 6 MEM_B_DQ<57> MAKE_BASE=TRUE =MEM_B_DQ<57> 29
94 11 6 MEM_B_DQ<56> MAKE_BASE=TRUE =MEM_B_DQ<56> 29

SYNC_MASTER=K92_SUMA SYNC_DATE=05/10/2010

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 30 OF 132

SHEET 28 OF 105

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

7 =PP1V5_S3_MEM_B

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
PLACE_NEAR=J3100.75:2.54mm

C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402
PLACE_NEAR=J3100.75:2.54mm

93 31 PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

OMIT_TABLE

J3100 F-RT-BGA6 DDR3-SODIMM (2 OF 2)

94 11 6 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 6 11 94
	NC	75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_A<15>	IN 6 11 94
94 11 6 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 6 11 94
		81	VDD	VDD	82		
94 11 6 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 6 11 94
94 11 6 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 6 11 94
		87	VDD	VDD	88		
94 11 6 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 6 11 94
94 11 6 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 6 11 94
		93	VDD	VDD	94		
94 11 6 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 6 11 94
94 11 6 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 6 11 94
		99	VDD	VDD	100		
94 11 6 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 6 11 94
94 11 6 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 6 11 94
		105	VDD	VDD	106		
94 11 6 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 6 11 94
94 11 6 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 6 11 94
		111	VDD	VDD	112		
94 11 6 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 6 11 94
94 11 6 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 6 11 94
		117	VDD	VDD	118		
94 11 6 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 6 11 94
94 11 6 IN	MEM_B_CS_L<1>	121	S1*	NC	122	NC	
		123	VDD	VDD	124		
NC		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
28 BI	MEM_B_DQ<32>	129	DQ32	DQ36	130	MEM_B_DQ<36>	BI 28
28 BI	MEM_B_DQ<33>	131	DQ33	DQ37	132	MEM_B_DQ<37>	BI 28
		133	VSS	VSS	134		
28 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136		
28 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_B_DQ<38>	BI 28
28 BI	MEM_B_DQ<34>	141	DQ34	DQ39	142	MEM_B_DQ<39>	BI 28
28 BI	MEM_B_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_B_DQ<44>	BI 28
28 BI	MEM_B_DQ<40>	147	DQ40	DQ45	148	MEM_B_DQ<45>	BI 28
28 BI	MEM_B_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_B_DQS_N<5>	BI 28
		153	DM5	DQS5	154	MEM_B_DQS_P<5>	BI 28
		155	VSS	VSS	156		
28 BI	MEM_B_DQ<42>	157	DQ42	DQ46	158	MEM_B_DQ<46>	BI 28
28 BI	MEM_B_DQ<43>	159	DQ43	DQ47	160	MEM_B_DQ<47>	BI 28
		161	VSS	VSS	162		
28 BI	MEM_B_DQ<48>	163	DQ48	DQ52	164	MEM_B_DQ<52>	BI 28
28 BI	MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<53>	BI 28
		167	VSS	VSS	168		
28 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170		
28 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_B_DQ<54>	BI 28
28 BI	MEM_B_DQ<50>	175	DQ50	DQ55	176	MEM_B_DQ<55>	BI 28
28 BI	MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_B_DQ<60>	BI 28
28 BI	MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<61>	BI 28
28 BI	MEM_B_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_B_DQS_N<7>	BI 28
		187	DM7	DQS7	188	MEM_B_DQS_P<7>	BI 28
		189	VSS	VSS	190		
28 BI	MEM_B_DQ<58>	191	DQ58	DQ62	192	MEM_B_DQ<62>	BI 28
28 BI	MEM_B_DQ<59>	193	DQ59	DQ63	194	MEM_B_DQ<63>	BI 28
		195	VSS	VSS	196		
6 MEM_B_SA<0>		197	SA0	EVENT*	198	MEM_EVENT_L	OUT 27 45 46
		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA	BI 48
6 MEM_B_SA<1>		201	SA1	SCL	202	=I2C_SODIMMB_SCL	IN 48
		203	VTT	VTT	204	=PP0V75_S0_MEM_VTT_B	7
			MTG PINS				
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

516S0806

SPD ADDR=0xA4(WR)/0xA5(RD)

7 =PPSPD_S0_MEM_B

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

C3150 1UF 10% 10V X5R 402
C3151 1UF 10% 10V X5R 402
C3152 1UF 10% 10V X5R 402
C3153 1UF 10% 10V X5R 402

PP0V75_S3_MEM_VREFCA_B 31 93

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

OMIT_TABLE

J3100 F-RT-BGA6 DDR3-SODIMM (1 OF 2) CRITICAL

		1	VREFDQ	VSS	2		
		3	VSS	DQ4	4	MEM_B_DQ<4>	BI 28
28 BI	MEM_B_DQ<0>	5	DQ0	DQ5	6	MEM_B_DQ<5>	BI 28
28 BI	MEM_B_DQ<1>	7	DQ1	VSS	8		
		9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 28
		11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 28
		13	VSS	VSS	14		
28 BI	MEM_B_DQ<2>	15	DQ2	DQ6	16	MEM_B_DQ<6>	BI 28
28 BI	MEM_B_DQ<3>	17	DQ3	DQ7	18	MEM_B_DQ<7>	BI 28
		19	VSS	VSS	20		
28 BI	MEM_B_DQ<8>	21	DQ8	DQ12	22	MEM_B_DQ<12>	BI 28
28 BI	MEM_B_DQ<9>	23	DQ9	DQ13	24	MEM_B_DQ<13>	BI 28
		25	VSS	VSS	26		
28 BI	MEM_B_DQS_N<1>	27	DQS1*	DM1	28		
28 BI	MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 26 27
		31	VSS	VSS	32		
28 BI	MEM_B_DQ<10>	33	DQ10	DQ14	34	MEM_B_DQ<14>	BI 28
28 BI	MEM_B_DQ<11>	35	DQ11	DQ15	36	MEM_B_DQ<15>	BI 28
		37	VSS	VSS	38		
28 BI	MEM_B_DQ<16>	39	DQ16	DQ20	40	MEM_B_DQ<20>	BI 28
28 BI	MEM_B_DQ<17>	41	DQ17	DQ21	42	MEM_B_DQ<21>	BI 28
		43	VSS	VSS	44		
28 BI	MEM_B_DQS_N<2>	45	DQS2*	DM2	46		
28 BI	MEM_B_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_B_DQ<22>	BI 28
28 BI	MEM_B_DQ<18>	51	DQ18	DQ23	52	MEM_B_DQ<23>	BI 28
28 BI	MEM_B_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_B_DQ<28>	BI 28
28 BI	MEM_B_DQ<24>	57	DQ24	DQ29	58	MEM_B_DQ<29>	BI 28
28 BI	MEM_B_DQ<25>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_B_DQS_N<3>	BI 28
		63	DM3	DQS3	64	MEM_B_DQS_P<3>	BI 28
		65	VSS	VSS	66		
28 BI	MEM_B_DQ<26>	67	DQ26	DQ30	68	MEM_B_DQ<30>	BI 28
28 BI	MEM_B_DQ<27>	69	DQ27	DQ31	70	MEM_B_DQ<31>	BI 28
		71	VSS	VSS	72		

516S0806

"Expansion" (bottom) slot

SYNC_MASTER=K92_SUMA SYNC_DATE=06/23/2010

PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 31 OF 132
SHEET: 29 OF 105

SD Card Connector

SDCONN_CLK
SDCONN_CMD
SDCONN_DATA<0>
SDCONN_DATA<1>
SDCONN_DATA<2>
SDCONN_DATA<3>
SDCONN_DATA<4>
SDCONN_DATA<5>
SDCONN_DATA<6>
SDCONN_DATA<7>
SDCONN_CARDDETECT_L

R3379 33 5% 1/16W MF-LF 402 — SDCONN_CLK_R
R3361 33 5% 1/16W MF-LF 402 — SDCONN_CMD_R
R3371 33 5% 1/16W MF-LF 402 — SDCONN_R_DATA<0>
R3372 33 5% 1/16W MF-LF 402 — SDCONN_R_DATA<1>
R3373 33 5% 1/16W MF-LF 402 — SDCONN_R_DATA<2>
R3374 33 5% 1/16W MF-LF 402 — SDCONN_R_DATA<3>
R3375 33 5% 1/16W MF-LF 402 — SDCONN_R_DATA<4>
R3376 33 5% 1/16W MF-LF 402 — SDCONN_R_DATA<5>
R3377 33 5% 1/16W MF-LF 402 — SDCONN_R_DATA<6>
R3378 33 5% 1/16W MF-LF 402 — SDCONN_R_DATA<7>

SDCONN_WP
=PP3V3_S0_SW_SD_PWR

CRITICAL
L3300
47NH-1.3OHM
0402
SDCONN_CLK_R_L

516-0225
CRITICAL
J3300
SD-CARD-K19-K24
F-RT-TH

3	VSS
6	VSS
5	CLK
2	CMD
7	DAT0
8	DAT1
9	DAT2
1	CD/DAT3
10	DAT4
11	DAT5
12	DAT6
13	DAT7
14	CARD_DETECT_SW
15	CARD_DETECT_GND
16	WRITE_PROTECT_SW
4	VDD
17	SHLD_PIN
18	SHLD_PIN
19	SHLD_PIN
20	SHLD_PIN

SD Not Inserted, CARD_DETECT is OPEN.
CAESAR-IV Card Detect is programmable, but a Silicon bug makes the active high case unusable.

NOSTUFF C3373 10PF 5% 25V CER 0201
NOSTUFF C3375 10PF 5% 25V CER 0201
NOSTUFF C3377 10PF 5% 25V CER 0201
NOSTUFF C3379 10PF 5% 25V CER 0201
NOSTUFF C3381 10PF 5% 25V CER 0201
NOSTUFF C3371 22PF 5% 50V CERM 402
NOSTUFF C3370 15PF 5% 50V CERM 402
NOSTUFF C3372 10PF 5% 25V CER 0201
NOSTUFF C3374 10PF 5% 25V CER 0201
NOSTUFF C3376 10PF 5% 25V CER 0201
NOSTUFF C3378 10PF 5% 25V CER 0201
NOSTUFF C3380 10PF 5% 25V CER 0201

Place near attr for series resistors:
PLACE_NEAR=U3900.21:5MM
PLACE_NEAR=U3900.26:5MM
PLACE_NEAR=U3900.25:5MM
PLACE_NEAR=U3900.24:5MM
PLACE_NEAR=U3900.23:5MM
PLACE_NEAR=U3900.22:5MM
PLACE_NEAR=U3900.52:5MM
PLACE_NEAR=U3900.53:5MM
PLACE_NEAR=U3900.54:5MM
PLACE_NEAR=U3900.55:5MM

SD Detect & Reset Logic

SDCONN_DETECT Debounce, Inversion, Detect-Changed PCH GPIO Latch Circuit
Converts SDCONN from active-low level signal to active-high pulses.

=PP3V3_S4_SD_HPD
C3310 1UF 10% 10V X5R 402-1

R3311 and R3310 mutually exclusive to control effect of =ENET_RESET_L on DET_CHANGED# logic.

CRITICAL
U3311
SLG4AP026V
TDFN
VDD
LOW_PWR
RST_IN*
RST LOGIC
RST_OUT*
DET_IN (IPU)
DLY
DET_CHNGD*
DET_OUT
DET_LVL
GND
THRM PAD

ENET_LOW_PWR
=ENET_RESET_L
SDCONN_CARDDETECT_L
SLG_ENET_RESET_IN_L
SD_DET_LVL_L
DET_CH_EN*
SD_DET_CH_EN_L
SDCONN_STATE_CHANGE_SMC
SDCONN_DETECT_L
SLG_ENET_RESET_OUT_L

R3315 10K 5% 1/16W MF-LF 402
R3314 0 5% 1/16W MF-LF 402 — ENET_RESET_L
R3311 0 5% 1/16W MF-LF 402
R3310 10K 5% 1/16W MF-LF 402 NOSTUFF
R3316 10K 5% 1/16W MF-LF 402
R3317 10K 5% 1/16W MF-LF 402
R3312 0 5% 1/16W MF-LF 402 NOSTUFF

-> From PCH GPI0
-> From SD Conn (Low active)
-> To SMC & to Isolation Circuit (then to PCH GPIO) (Low active pulse signal)
-> To ENET Chip

Must STUFF R3312 and NOSTUFF R3314 when R3311 is NOT STUFFED.
R3314 and R3312 mutually exclusive to bypass reset logic

DLY block is 20ms nominal
When ENET_LOW_PWR deasserts, RST_OUT# deasserts for >80ms, then asserts for 10ms regardless ofmove RST_IN# state.
Otherwise RST_OUT# follows RST_IN#

SD Card 3.3V Overcurrent Protection

TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.

CRITICAL
U3300
TPS2065-1
DGN
IN0
IN1
EN
OUT0
OUT1
OUT2
OC*
THRM GND PAD
353S3004

=PP3V3_S0_SDCARD
ENET_CR_PWREN

CRITICAL C3300 10UF 20% 6.3V X5R 603
C3301 0.1UF 10% 16V X7R-CERM 402
CRITICAL C3302 10UF 20% 6.3V X5R 603
C3303 0.1UF 10% 16V X7R-CERM 402
NOSTUFF R3300 47K 5% 1/16W MF-LF 402
R3301 10K 5% 1/16W MF-LF 402
R3302 0 5% 1/16W MF-LF 402

=PP3V3_S0_SW_SD_PWR
PP3V3_S0_SW_SD_PWR
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
=PP3V3_S0_PCH_GPIO
SDCONN_OC_L_R
SDCONN_OC_L

SYNC_MASTER=J31_YONAS	SYNC_DATE=10/25/2011
PAGE TITLE	SD Card Connector
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 33 OF 132
	SHEET 30 OF 105

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

=PP3V3_S3_VREFMRGN

OMIT R3418 SHORT — PP3V3_S3_VREFMRGN_DAC — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V

DDRVREF_DAC C3400 2.2UF 20% 6.3V CERM 402-LF

DDRVREF_DAC C3401 0.1UF 20% 10V CERM 402

CRITICAL DDRVREF_DAC U3400 DAC5574 (MSOP, VDD, GND, SCL, SDA, A0, A1, VOUTA, VOUTB, VOUTC, VOUTD)

=I2C_VREFDACS_SCL (IN) — =I2C_VREFDACS_SDA (BI)

Addr=0x98(WR)/0x99(RD)

VREFMRGN_SODIMMA_DQ
VREFMRGN_SODIMMB_DQ
VREFMRGN_SODIMMS_CA
VREFMRGN_MEMVREG_FBVREF

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

OMIT R3419 SHORT — PP3V3_S3_VREFMRGN_CTRL — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V

DDRVREF_DAC C3402 0.1UF 20% 10V CERM 402

CRITICAL DDRVREF_DAC U3401 PCA9557 QFN (OD) (VCC, GND, THRM PAD, A0, A1, A2, SCL, SDA, RESET*, P0–P7)

Addr=0x30(WR)/0x31(RD)

=I2C_PCA9557D_SCL (IN) — =I2C_PCA9557D_SDA (BI)

VREFMRGN_DQ_SODIMMA_EN
VREFMRGN_DQ_SODIMMB_EN
VREFMRGN_CA_SODIMMA_EN
VREFMRGN_CA_SODIMMB_EN
VREFMRGN_MEMVREG_EN
VREFMRGN_FRAMEBUF_EN

PCA9557D_RESET_L (IN)

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

=PPDDR_S3_MEMVREF

CRITICAL Q3420 SSM6N15FEAPE SOT563 — MEMRESET_ISOL_LS5V_L — PPCPU_MEM_VREFDQ_A

DDRVREF_DAC C3420 0.1UF 10% 16V X5R 402 — PLACE_NEAR=Q3420.6:2mm — VREFDQ:M1_M3

R3421 1K 1% 1/16W MF-LF 402 — PLACE_NEAR=Q3420.6:1mm — VREFDQ:M1_M3

PP0V75_S3_MEM_VREFDQ_A (27 31 93)

R3422 1K 1% 1/16W MF-LF 402 — VREFDQ:M1_M3 — PLACE_NEAR=R3421.2:1mm

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

=PPDDR_S3_MEMVREF

CRITICAL Q3420 SSM6N15FEAPE SOT563 — MEMRESET_ISOL_LS5V_L — PPCPU_MEM_VREFDQ_B

DDRVREF_DAC C3440 0.1UF 10% 16V X5R 402 — PLACE_NEAR=Q3420.3:2mm — VREFDQ:M1_M3

R3441 1K 1% 1/16W MF-LF 402 — PLACE_NEAR=Q3420.3:1mm — VREFDQ:M1_M3

PP0V75_S3_MEM_VREFDQ_B (29 31 93)

R3442 1K 1% 1/16W MF-LF 402 — VREFDQ:M1_M3 — PLACE_NEAR=R3441.2:1mm

DDRVREF_DAC C3403 0.1UF 20% 10V CERM 402

CRITICAL DDRVREF_DAC U3402 MAX4253 UCSP — VREFMRGN_DQ_SODIMMA_BUF

=PPVTT_S3_DDR_BUF (68) — 10mA max load

VREFDQ:LDO_DAC R3403 200 1% 1/16W MF-LF 402 — PLACE_NEAR=J2900.1:2.54mm

PP0V75_S3_MEM_VREFDQ_A (27 31 93) — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0.75V

VREFDQ:LDO_DAC R3404 133 1% 1/16W MF-LF 402 — PLACE_NEAR=R3403.2:1mm

DDRVREF_DAC R3401 100K 5% 1/16W MF-LF 402

CRITICAL DDRVREF_DAC U3402 MAX4253 UCSP — VREFMRGN_DQ_SODIMMB_BUF

VREFDQ:LDO_DAC R3405 200 1% 1/16W MF-LF 402 — PLACE_NEAR=J3100.1:2.54mm

PP0V75_S3_MEM_VREFDQ_B (29 31 93) — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0.75V

VREFDQ:LDO_DAC R3406 133 1% 1/16W MF-LF 402 — PLACE_NEAR=R3405.2:1mm

DDRVREF_DAC R3402 100K 5% 1/16W MF-LF 402

DDRVREF_DAC C3404 0.1UF 20% 10V CERM 402

CRITICAL DDRVREF_DAC U3403 MAX4253 UCSP — VREFMRGN_CA_SODIMMA_BUF

VREFCA:LDO_DAC R3409 200 1% 1/16W MF-LF 402 — PLACE_NEAR=J2900.126:2.54mm

PP0V75_S3_MEM_VREFCA_A (27 93) — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0.75V

VREFCA:LDO_DAC R3410 133 1% 1/16W MF-LF 402 — PLACE_NEAR=R3409.2:1mm

DDRVREF_DAC R3407 100K 5% 1/16W MF-LF 402

CRITICAL DDRVREF_DAC U3403 MAX4253 UCSP — VREFMRGN_CA_SODIMMB_BUF

VREFCA:LDO_DAC R3411 200 1% 1/16W MF-LF 402 — PLACE_NEAR=J3100.126:2.54mm

PP0V75_S3_MEM_VREFCA_B (29 93) — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0.75V

VREFCA:LDO_DAC R3412 133 1% 1/16W MF-LF 402 — PLACE_NEAR=R3411.2:1mm

DDRVREF_DAC R3408 100K 5% 1/16W MF-LF 402

DDRVREF_DAC C3405 0.1UF 20% 10V CERM 402

CRITICAL DDRVREF_DAC U3404 MAX4253 UCSP — VREFMRGN_MEMVREG_BUF

DDRVREF_DAC R3414 33.2K 1% 1/16W MF-LF 402 — DDRREG_FB (OUT 6 68)

CRITICAL

DDRVREF_DAC R3416 0 5% 1/16W MF-LF 402 — VREFMRGN_MEMVREG_FBVREF_R

DDRVREF_DAC R3413 100K 5% 1/16W MF-LF 402

CRITICAL DDRVREF_DAC U3404 MAX4253 UCSP — VREFMRGN_FRAMEBUF_BUF

DDRVREF_DAC R3417 0 5% 1/16W MF-LF 402 — VREFMRGN_FRAMEBUF_BUF_R

DDRVREF_DAC R3415 100K 5% 1/16W MF-LF 402

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=J31_ANNE SYNC_DATE=06/09/2011

PAGE TITLE: DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 34 OF 132
SHEET: 31 OF 105

AIRPORT

C3531 0.1UF 10% 16V X5R-CERM 0201 — PLACE_NEAR=J3501.15:2.54mm
C3530 0.1UF 10% 16V X5R-CERM 0201 — PLACE_NEAR=J3501.17:2.54mm
PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N

R3510 0 5% 1/20W MF 201
R3511 0 5% 1/20W MF 201
PCIE_AP_D2R_P
PCIE_AP_D2R_N

WIFI_EVENT_L

516S0582
CRITICAL
J3501
500913-0302
F-ST-SM

96 PCIE_AP_R2D_P
96 PCIE_AP_R2D_N
96 PCIE_AP_D2R_R_P
96 PCIE_AP_D2R_R_N
101 PCIE_CLK100M_AP_CONN_P
101 PCIE_CLK100M_AP_CONN_N

CRITICAL
L3501
330-OHM-80MA
DLP11S
SYM_VER-1
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N
PLACE_NEAR=J3501.11:2.54mm

AP_TEMP_SMB_SCL_PD
AP_TEMP_SMB_SDA_PD
R3520 51 5% 1/16W MF-LF 402
R3521 51 5% 1/16W MF-LF 402

29 PP3V3_S3RS4_BT_F
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.5 mm
C3532 0.01UF 10% 16V CERM 402
L3505 BTPWR:S4
FERR-120-OHM-1.5A
0402-LF
PLACE_NEAR=J3501.27:2.54mm
=PP3V3_S4_BT 7 32

BLUETOOTH

NOSTUFF R3517 15K 1% 1/20W MF 201
BTPWR:S3 R3518 0 5% 1/20W MF 201
NOSTUFF R3515 15K 1% 1/20W MF 201
NOSTUFF R3516 15K 1% 1/20W MF 201
95 USB_BT_CONN_P
95 USB_BT_CONN_N

U3510
PI3USB102ZLE
TQFN
CRITICAL
VCC
SEL
GND
Y+ Y- M+ M- D+ D- OE*

=PP3V3_S4_BT 7 32
C3510 0.1UF 10% 6.3V X5R 201
USB_BT_WAKEP
USB_BT_N BI 8 95
USB_BT_P BI 8 95

BTPWR:S4 R3514 15K 1% 1/20W MF 201
USB_BT_WAKEN
BTPWR:S4 R3512 15K 1% 1/20W MF 201
NOSTUFF R3513 15K 1% 1/20W MF 201

BTPWR:S4
CRITICAL
Q3510
SSM3K15AMFVAPE
=BT_WAKE_L OUT 46

BTPWR:S4 R3519 0 5% 1/20W MF 201
74 45 26 17 PM_SLP_S4_L IN
BTMUX_SEL
NOSTUFF C3511 0.01UF 10% 10V X5R 201

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

Supervisor & CLKFREG # ISolation

Delay = 60 ms +/- 20%

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

CRITICAL
Q3550
DMP2018LFK
DFN2563-6

15550367
L3504
FERR-120-OHM-3A
0603
45 6 PP3V3_WLAN
MIN_NECK_WIDTH=0.4 mm
MIN_LINE_WIDTH=1 mm
PP3V3_WLAN_F 32
C3522 0.1uF 20% 10V CERM 402 — PLACE_NEAR=J3501.29:2.54MM
C3521 0.1uF 20% 10V CERM 402 — PLACE_NEAR=J3501.29:2.54MM

XW3552 SM
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
PP3V3_WLAN_R

C3550 0.1UF 10% 16V X5R 402-1
P3V3WLAN_SS
C3551 0.033UF 10% 16V X5R 402
R3550 33K 5% 1/10W MF-LF 402
R3551 10K 5% 1/16W MF-LF 402
PM_WLAN_EN_L IN 74
=PP3V3_S3_WLAN 7 32

PP3V3_WLAN_F 32
=PP3V3_S3_WLAN 7 32
R3553 100K 1% 1/16W MF-LF 402
R3554 232K 1% 1/16W MF-LF 402
P3V3WLAN_VMON
R3555 100K 1% 1/16W MF-LF 402

CRITICAL
U3540
SLG4AP016V
TDFN
VDD SENSE 0.7V RESET* MR* EN IN OUT (OD) THRM PAD GND
DLY
C3540 0.1uF 20% 10V CERM 402

AP_RESET_L IN 24
AP_PWR_EN IN 18 23 74
AP_CLKREQ_L OUT 16

PCIE_WAKE_L OUT 6 17 24
6 AP_RESET_CONN_L
6 AP_CLKREQ_Q_L

518S0815
CRITICAL
J3502
8190-3506-K281
F-RT-SMT

6 PP5V_S3_ALSCAMERA_F
=I2C_ALS_SCL IN 48
=I2C_ALS_SDA BI 48
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
95 USB_CAMERA_CONN_P
95 USB_CAMERA_CONN_N

ALS CAMERA

275 mA peak
206 mA nominal max

CRITICAL
L3507
90-OHM
DLP8NS
SYM_VER-1
USB_CAMERA_P BI 18 95
USB_CAMERA_N BI 18 95
PLACE_NEAR=J3502.2:2.54MM

PLACE_NEAR=J3502.6:2.54MM
L3508
FERR-120-OHM-1.5A
0402-LF
=PP5V_S3_ALSCAMERA 7
C3552 0.1uF 20% 10V CERM 402

SYNC_MASTER=J30_MLB SYNC_DATE=11/11/2013
PAGE TITLE
X19/ALS/CAMERA CONNECTOR
Apple Inc.
DRAWING NUMBER 051-9585
SIZE D
REVISION 3.0.0
BRANCH
PAGE 35 OF 132
SHEET 32 OF 105

CRITICAL
OMIT_TABLE
U3600
T29
FCBGA
(SYM 1 OF 2)

PCIE GEN2

RECEIVE

PCIE_TBT_R2D_C_P<0>	C3600 0.1UF	PCIE_TBT_R2D_P<0>	PER_0_P
PCIE_TBT_R2D_C_N<0>	C3601 0.1UF	PCIE_TBT_R2D_N<0>	PER_0_N
PCIE_TBT_R2D_C_P<1>	C3602 0.1UF	PCIE_TBT_R2D_P<1>	PER_1_P
PCIE_TBT_R2D_C_N<1>	C3603 0.1UF	PCIE_TBT_R2D_N<1>	PER_1_N
PCIE_TBT_R2D_C_P<2>	C3604 0.1UF	PCIE_TBT_R2D_P<2>	PER_2_P
PCIE_TBT_R2D_C_N<2>	C3605 0.1UF	PCIE_TBT_R2D_N<2>	PER_2_N
PCIE_TBT_R2D_C_P<3>	C3606 0.1UF	PCIE_TBT_R2D_P<3>	PER_3_P
PCIE_TBT_R2D_C_N<3>	C3607 0.1UF	PCIE_TBT_R2D_N<3>	PER_3_N

TRANSMIT

PET_0_P	PCIE_TBT_D2R_C_P<0>	C3640 0.1UF	PCIE_TBT_D2R_P<0>
PET_0_N	PCIE_TBT_D2R_C_N<0>	C3641 0.1UF	PCIE_TBT_D2R_N<0>
PET_1_P	PCIE_TBT_D2R_C_P<1>	C3642 0.1UF	PCIE_TBT_D2R_P<1>
PET_1_N	PCIE_TBT_D2R_C_N<1>	C3643 0.1UF	PCIE_TBT_D2R_N<1>
PET_2_P	PCIE_TBT_D2R_C_P<2>	C3644 0.1UF	PCIE_TBT_D2R_P<2>
PET_2_N	PCIE_TBT_D2R_C_N<2>	C3645 0.1UF	PCIE_TBT_D2R_N<2>
PET_3_P	PCIE_TBT_D2R_C_P<3>	C3646 0.1UF	PCIE_TBT_D2R_P<3>
PET_3_N	PCIE_TBT_D2R_C_N<3>	C3647 0.1UF	PCIE_TBT_D2R_N<3>

TP_TBT_MONDC0	B21	MONDC0
TP_TBT_MONDC1	A20	MONDC1
		DEBUG: For monitoring current/voltage
TP_TBT_MONOBSP	K17	MONOBSP
TP_TBT_MONOBSN	M17	MONOBSN
		DEBUG: For monitoring clock

WAKE* F1 TBT_PCIE_WAKE_L — R3651 10K 5% 1/16W MF-LF 402 — =PP3V3_TBT_RTR
PERST* E6 TBT_RESET_L
RSENSE E14 TBT_RSENSE — R3655 1K 1% 1/16W MF-LF 402
RBIAS E16 TBT_RBIAS

MISC

POWER ON RESET

Not used in host mode.

PCIE_RST_0* K1	TP_TBT_PCIE_RESET0_L
PCIE_RST_1* J2	TP_TBT_PCIE_RESET1_L
PCIE_RST_2* K3	TP_TBT_PCIE_RESET2_L
PCIE_RST_3* J4	TP_TBT_PCIE_RESET3_L

JTAG

TDI T3	JTAG_TBT_TDI
TMS R4	JTAG_TBT_TMS
TCK R2	JTAG_TBT_TCK
TDO T1	JTAG_TBT_TDO

CLOCKS

REFCLK_100_IN_P H17	PCIE_CLK100M_TBT_P
REFCLK_100_IN_N G16	PCIE_CLK100M_TBT_N
XTAL_25_IN P17	SYSCLK_CLK25M_TBT_R — R3695 806 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_TBT
XTAL_25_OUT R16	TP_TBT_XTAL25OUT
TMU_CLK_OUT U2	TBT_TMU_CLK_OUT
TMU_CLK_IN E2	TBT_TMU_CLK_IN

=PP3V3_TBT_RTR — R3698 10K 5% 1/16W MF-LF 402 — R3696 1K 5% 1/16W MF-LF 402
NO STUFF R3699 10K 5% 1/16W MF-LF 402

=PP3V3_TBT_RTR — R3690 3.3K 5% 1/16W MF-LF 402 — R3691 3.3K 5% 1/16W MF-LF 402 — C3690 1UF 10% 6.3V CERM 402 — R3692 3.3K 5% 1/16W MF-LF 402 — R3623 10K 5% 1/16W MF-LF 402 — R3622 10K 5% 1/16W MF-LF 402 — R3621 10K 5% 1/16W MF-LF 402 — R3693 3.3K 5% 1/16W MF-LF 402

CRITICAL
OMIT_TABLE
U3690
M95320-RMB6TG
MLP

TBT_SPI_MOSI	D	
TBT_SPI_CLK	C	
TBT_SPI_CS_L	S_L	
TBTROM_WP_L	W_L	
TBTROM_HOLD_L	HOLD_L	
	Q	TBT_SPI_MISO
	VCC	
	VSS	
	THM PAD	

=TBT_CLKREQ_L
TBT_GPIO<1>
TBT_GPIO<2>
TBT_RSVD

CLK REQUEST

EEPROM

TBT_SPI_MOSI	EE_DI
TBT_SPI_MISO	EE_DO
TBT_SPI_CS_L	EE_CS*
TBT_SPI_CLK	EE_CLK

TP_TBT_THERM_DP	THERM_DP
	Use B1 GND ball for THERM_DN
TBT_TEST_EN	TEST_EN
TP_TBT_TEST_POINT_0	TEST_POINT_0
TP_TBT_TEST_POINT_1	TEST_POINT_1
TP_TBT_TEST_POINT_2	TEST_POINT_2
TBT_TEST_POINT_3	TEST_POINT_3

TEST PORT

R3625 0 5% 1/16W MF-LF 402
R3629 0 5% 1/16W MF-LF 402

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C3620 0.1uF	DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_C_N<0>	C3621 0.1uF	DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_ML_C_P<1>	C3622 0.1uF	DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_C_N<1>	C3623 0.1uF	DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_C_P<2>	C3624 0.1uF	DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_C_N<2>	C3625 0.1uF	DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_C_P<3>	C3626 0.1uF	DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_C_N<3>	C3627 0.1uF	DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_AUXCH_C_P	C3628 0.1uF	DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_C_N	C3629 0.1uF	DP_TBTSNK0_AUXCH_N

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C3630 0.1uF	DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_C_N<0>	C3631 0.1uF	DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_ML_C_P<1>	C3632 0.1uF	DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_C_N<1>	C3633 0.1uF	DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_C_P<2>	C3634 0.1uF	DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_C_N<2>	C3635 0.1uF	DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_C_P<3>	C3636 0.1uF	DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_C_N<3>	C3637 0.1uF	DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_AUXCH_C_P	C3638 0.1uF	DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_C_N	C3639 0.1uF	DP_TBTSNK1_AUXCH_N

DP_TBTSNK0_ML_P<3>	AA4	DPSNK0_ML_LANE_3P
DP_TBTSNK0_ML_N<3>	Y3	DPSNK0_ML_LANE_3N
DP_TBTSNK0_ML_P<2>	AA6	DPSNK0_ML_LANE_2P
DP_TBTSNK0_ML_N<2>	Y5	DPSNK0_ML_LANE_2N
DP_TBTSNK0_ML_P<1>	AA8	DPSNK0_ML_LANE_1P
DP_TBTSNK0_ML_N<1>	Y7	DPSNK0_ML_LANE_1N
DP_TBTSNK0_ML_P<0>	AA10	DPSNK0_ML_LANE_0P
DP_TBTSNK0_ML_N<0>	Y9	DPSNK0_ML_LANE_0N
DP_TBTSNK0_AUXCH_P	V1	DPSNK0_AUX_CHP
DP_TBTSNK0_AUXCH_N	W2	DPSNK0_AUX_CHN
DP_TBTSNK0_HPD	V5	DPSNK0_HOT_PLUG_DET

SINK PORT 0

DP_TBTSNK1_ML_P<3>	V9	DPSNK1_ML_LANE_3P
DP_TBTSNK1_ML_N<3>	U8	DPSNK1_ML_LANE_3N
DP_TBTSNK1_ML_P<2>	V11	DPSNK1_ML_LANE_2P
DP_TBTSNK1_ML_N<2>	U10	DPSNK1_ML_LANE_2N
DP_TBTSNK1_ML_P<1>	V13	DPSNK1_ML_LANE_1P
DP_TBTSNK1_ML_N<1>	U12	DPSNK1_ML_LANE_1N
DP_TBTSNK1_ML_P<0>	V15	DPSNK1_ML_LANE_0P
DP_TBTSNK1_ML_N<0>	U14	DPSNK1_ML_LANE_0N
DP_TBTSNK1_AUXCH_P	V7	DPSNK1_AUX_CHP
DP_TBTSNK1_AUXCH_N	U6	DPSNK1_AUX_CHN
DP_TBTSNK1_HPD	U4	DPSNK1_HOT_PLUG_DET

SINK PORT 1

R3630 100K 5% 1/16W MF-LF 402
R3631 100K 5% 1/16W MF-LF 402

DISPLAY

SOURCE PORT 0

DPSRC0_ML_LANE_3P	AA18 TP_DP_TBTSRC_ML_CP<3>
DPSRC0_ML_LANE_3N	Y17 TP_DP_TBTSRC_ML_CN<3>
DPSRC0_ML_LANE_2P	AA16 TP_DP_TBTSRC_ML_CP<2>
DPSRC0_ML_LANE_2N	Y15 TP_DP_TBTSRC_ML_CN<2>
DPSRC0_ML_LANE_1P	AA14 TP_DP_TBTSRC_ML_CP<1>
DPSRC0_ML_LANE_1N	Y13 TP_DP_TBTSRC_ML_CN<1>
DPSRC0_ML_LANE_0P	AA12 TP_DP_TBTSRC_ML_CP<0>
DPSRC0_ML_LANE_0N	Y11 TP_DP_TBTSRC_ML_CN<0>
DPSRC0_AUX_CHP	W16 TP_DP_TBTSRC_AUXCH_CP
DPSRC0_AUX_CHN	U16 TP_DP_TBTSRC_AUXCH_CN
DPSRC0_HOT_PLUG_DET	V3 DP_TBTSRC_HPD

DP_ATEST	Y19 TBT_DP_ATEST
DP_RES_0	Y21
DP_RES_1	AA20 TBT_DP_RES

100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm
C3685 100PF 5% 50V CERM 402
C3686 0.01UF 10% 16V CERM 402
R3685 14.0K 1% 1/16W MF-LF 402
R3632 100K 5% 1/10W MF-LF 402

PORTS

TBT_R2D_C_P<0>	A6	PRT0_T29T_P
TBT_R2D_C_N<0>	A4	PRT0_T29T_N
TBT_D2R_P<0>	C4	PRT0_T29R_P
TBT_D2R_N<0>	C2	PRT0_T29R_N
TBT_LSEO<0>	J6	T29_0_LSEO
TBT_LSOE<0>	K5	T29_0_LSOE

PORT0

TBT_R2D_C_P<1>	A10	PRT1_T29T_P
TBT_R2D_C_N<1>	A8	PRT1_T29T_N
TBT_D2R_P<1>	C8	PRT1_T29R_P
TBT_D2R_N<1>	C6	PRT1_T29R_N
TBT_LSEO<1>	G8	T29_1_LSEO
TBT_LSOE<1>	H5	T29_1_LSOE

PORT1

I2C_TBT_SDA	F3	T29_SDA
I2C_TBT_SCL	F5	T29_SCL

PORT2

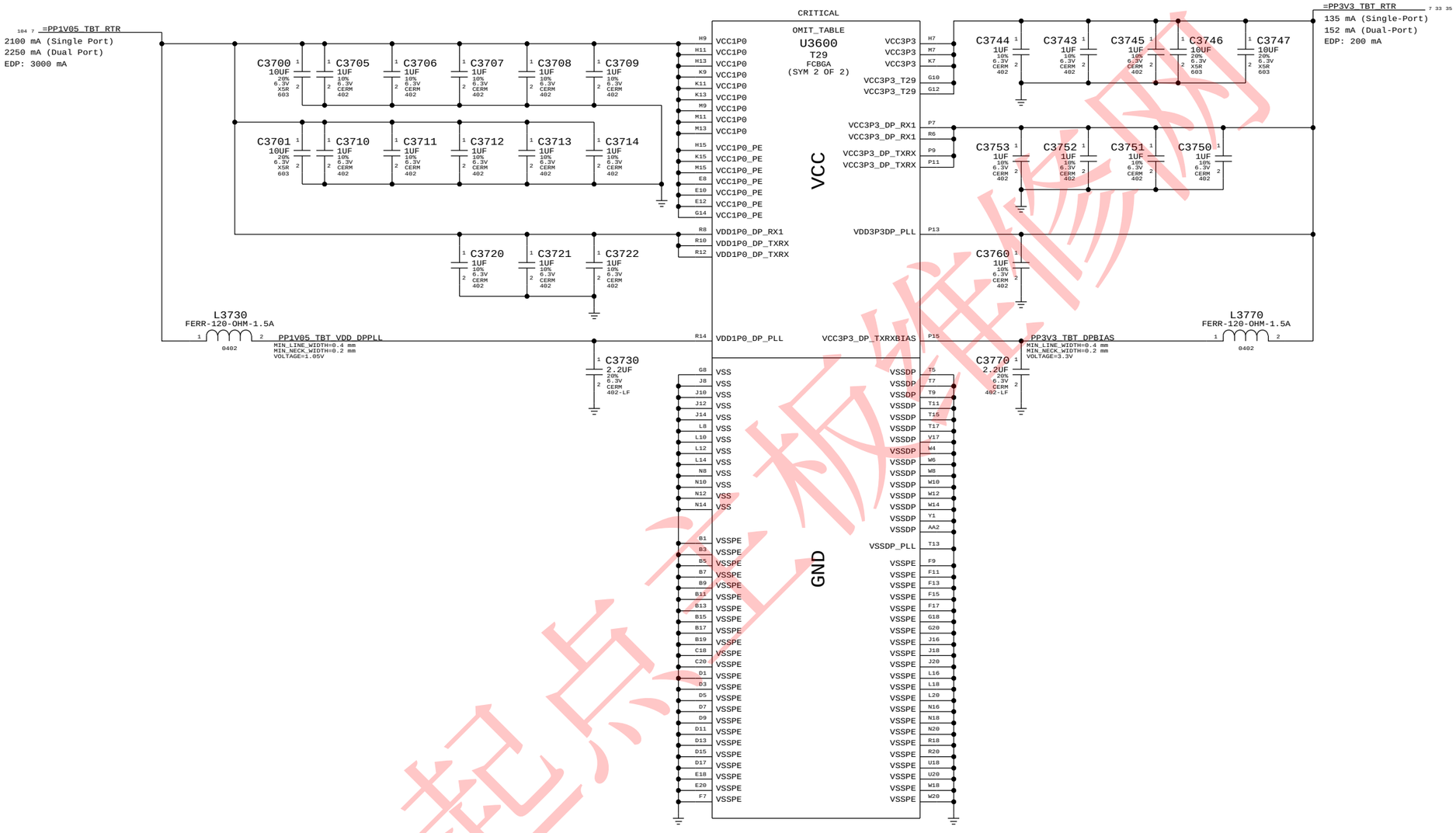
PRT2_T29T_P	A14 TBT_R2D_C_P<2>
PRT2_T29T_N	A12 TBT_R2D_C_N<2>
PRT2_T29R_P	C12 TBT_D2R_P<2>
PRT2_T29R_N	C10 TBT_D2R_N<2>
T29_2_LSEO	G4 TBT_LSEO<2>
T29_2_LSOE	H3 TBT_LSOE<2>

PORT3

PRT3_T29T_P	A18 TBT_R2D_C_P<3>
PRT3_T29T_N	A16 TBT_R2D_C_N<3>
PRT3_T29R_P	C16 TBT_D2R_P<3>
PRT3_T29R_N	C14 TBT_D2R_N<3>
T29_3_LSEO	G2 TBT_LSEO<3>
T29_3_LSOE	H1 TBT_LSOE<3>

NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).

SYNC_MASTER=T29_REF SYNC_DATE=06/14/2011
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 36 OF 132
SHEET 33 OF 105



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_REF SYNC_DATE=06/14/2011

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH:

PAGE: 37 OF 132

SHEET: 34 OF 105

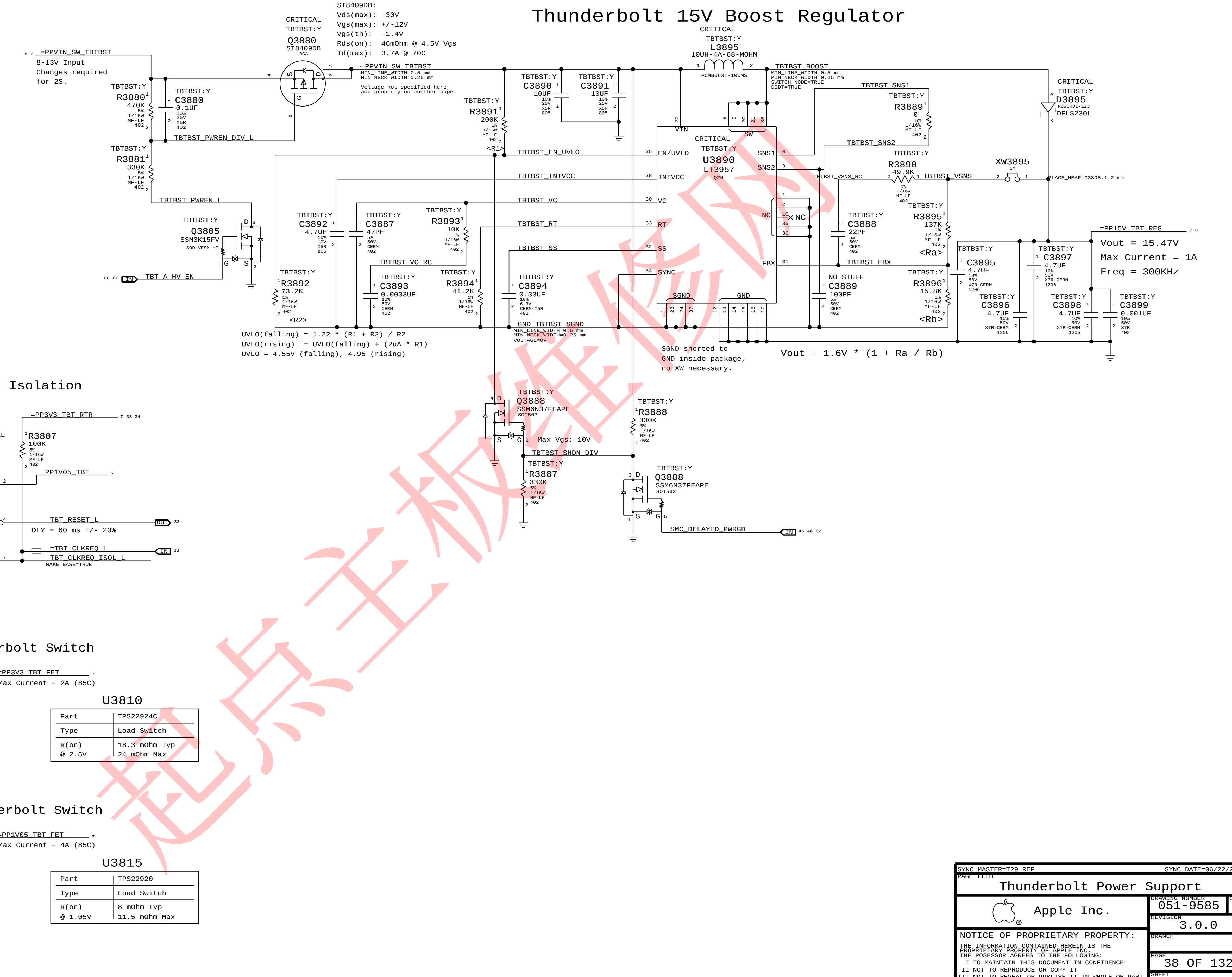
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_S0_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_S0_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

Thunderbolt 15V Boost Regulator



SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C
CRITICAL TBTBST:Y Q3880 SI8409DB
=PPVIN_SW_TBTBST
8-13V Input
Changes required for 2S.
PPVIN_SW_TBTBST
Voltage not specified here, add property on another page.
R3880 470K
C3880 0.1UF
TBTBST_PWREN_DIV_L
R3881 330K
TBTBST_PWREN_L
Q3805 SSM3K15FV
TBT_A_HV_EN
CRITICAL TBTBST:Y L3895 10UH-4A-68-MOHM
TBTBST_BOOST
C3890 10UF
C3891 10UF
R3891 200K
TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
CRITICAL TBTBST:Y U3890 LT3957
VIN
SW
EN/UVLO
INTVCC
VC
RT
SS
SYNC
SNS1
SNS2
FBX
SGND
GND
NC
TBTBST_SNS1
TBTBST_SNS2
R3889 0
R3890 49.9K
TBTBST_VSNS
XW3895
CRITICAL TBTBST:Y D3895 DFLS230L
C3892 4.7UF
C3887 47PF
R3893 10K
C3888 22PF
R3895 137K <Ra>
TBTBST_VC_RC
R3892 73.2K <R2>
C3893 0.0033UF
R3894 41.2K
C3894 0.33UF
NO STUFF C3889 100PF
R3896 15.8K <Rb>
TBTBST_FBX
C3895 4.7UF
C3896 4.7UF
C3897 4.7UF
C3898 4.7UF
C3899 0.001UF
=PP15V_TBT_REG
Vout = 15.47V
Max Current = 1A
Freq = 300KHz
GND_TBTBST_SGND
UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)
SGND shorted to GND inside package, no XW necessary.
Vout = 1.6V * (1 + Ra / Rb)
TBTBST:Y Q3888 SSM6N37FEAPE
Max Vgs: 10V
TBTBST:Y R3888 330K
TBTBST_SHDN_DIV
TBTBST:Y R3887 330K
SMC_DELAYED_PWRGD
Supervisor & CLKREQ# Isolation
=PP3V3_S0_TBTPWRCTL
C3800 0.1UF
CRITICAL U3800 SLG4AP016V
=PP3V3_TBT_RTR
R3807 100K
PP1V05_TBT
Platform (PCIe) Reset
=TBT_RESET_L
R3803 10K
Open-Drain GPIO
TBT_SW_RESET_L
TBT_RESET_L
DLY = 60 ms +/- 20%
TBT_PWR_EN
TBT_CLKREQ_L
=TBT_CLKREQ_L
TBT_CLKREQ_ISOL_L
Pull-ups provided by SB page.
3.3V Thunderbolt Switch
U3810 TPS22924
=PP3V3_S0_P3V3TBTFET
=PP3V3_TBT_FET
Max Current = 2A (85C)
C3810 1UF
R3816 0
TBT_PWR_EN_RC
1.05V Thunderbolt Switch
U3815 TPS22920
=PP1V05_S0_P1V05TBTFET
=PP1V05_TBT_FET
Max Current = 4A (85C)
C3815 1UF
NO STUFF C3816 1UF

U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

U3815

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=T29_REF SYNC_DATE=06/22/2011

PAGE TITLE: Thunderbolt Power Support

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH

BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

72 36 24 7 =PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
36 =PP3V3R1V8_ENET_LR_OUT

CRITICAL L3900 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_XTALVDDH — C3900 0.1UF 10% 16V X7R-CERM 402
CRITICAL L3905 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_BIASVDDH — C3905 0.1UF 10% 16V X7R-CERM 402
CRITICAL L3910 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_AVDDH — R3910 4.7K 5% 1/16W MF-LF 402 — C3910 0.1UF 10% 16V X7R-CERM 402 — C3911 0.1UF 10% 16V X7R-CERM 402
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

ENET_SR_LX 72
ENET_SR_VFB 72

Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY 7
???mA (1000base-T, Caesar V)

CRITICAL L3920 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_AVDDL — C3921 0.1UF 10% 16V X7R-CERM 402 — C3920 4.7UF 10% 6.3V X5R-CERM 603
CRITICAL L3925 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_PCIEPLL — C3926 0.1UF 10% 16V X7R-CERM 402 — C3925 4.7UF 10% 6.3V X5R-CERM 603
CRITICAL L3930 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_GPHYPLL — C3931 0.1UF 10% 16V X7R-CERM 402 — C3930 4.7UF 10% 6.3V X5R-CERM 603
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V

C3936 0.1UF 10% 16V X7R-CERM 402
CRITICAL C3935 10UF 10% 6.3V X5R 805

AVDDH BIASVDDH XTALVDDH VDDO SR_VDD SR_VDDP SR_LX SR_VFB AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

=PP3V3R1V8_ENET_LR_OUT 36
PP3V3R1V8_ENET_LR_OUT_REG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.8V
C3970 4.7UF 10% 6.3V X5R-CERM 603
C3971 0.1UF 10% 16V X7R-CERM 402
C3972 0.1UF 10% 16V X7R-CERM 402

7 =PP3V3_S0_ENETPHY
R3942 1K 5% 1/16W MF-LF 402 — Current Limiting Resistor

C3950 0.1uF 10% 16V X5R 402
C3951 0.1uF 10% 16V X5R 402
C3955 0.1uF 10% 16V X5R 402
C3956 0.1uF 10% 16V X5R 402
R3943 0 5% 1/16W MF-LF 402

96 16 OUT PCIE_ENET_D2R_N
96 16 OUT PCIE_ENET_D2R_P
96 16 IN PCIE_ENET_R2D_C_P
96 16 IN PCIE_ENET_R2D_C_N
24 OUT =ENET_WAKE_L (See note)

ENET_VMAIN_PRSNT — VMAIN_PRSNT (IPD) 58
96 PCIE_ENET_D2R_C_N — PCIE_TXD_N 27
96 PCIE_ENET_D2R_C_P — PCIE_TXD_P 28
96 PCIE_ENET_R2D_P — PCIE_RXD_P 33
96 PCIE_ENET_R2D_N — PCIE_RXD_N 34
96 16 IN PCIE_CLK100M_ENET_P — PCIE_REFCLK_P 31
96 16 IN PCIE_CLK100M_ENET_N — PCIE_REFCLK_N 30
97 30 IN ENET_RESET_L — PERST* (IPD) 11
16 OUT ENET_CLKREQ_L — CLKREQ* (OD) 12
ENET_WAKE_R_L — WAKE* (OD) 3
30 24 IN ENET_LOW_PWR — LOW_PWR (IPD) 4
BCM57765_SMB_CLK — SMB_CLK 6
BCM57765_SMB_DATA — SMB_DATA (IPD) 10
36 BCM57765_SCLK — SCLK_SPD1000LED* 66
36 BCM57765_MISO — SI/EEDATA 64
36 BCM57765_MOSI — SO_LINKLED* 65
36 BCM57765_CS_L — CS*/EECLK 63
(IPU)
TP_BCM57765_SPD100LED_L — SPD100LED*/SERIAL_DO (OD) 2
TP_BCM57765_TRAFFICLED_L — TRAFFICLED*/SERIAL_DI (OD) 67
24 IN SYSCLK_CLK25M_ENET — XTALI 18
NC — XTALO 19
BCM57765_RDAC — RDAC 38
R3965 1.24K 1% 1/16W MF-LF 402

U3900
BCM57765B0
QFN-8X8

THRM_PAD 69

GPIO_0/CR_ACT_LED* (IPD) — NC 5
GPIO_1/LR_OUT — 8
GPIO_2/MEDIA_SENSE — ENET_MEDIA_SENSE 9 OUT 24
(IPx) SD_DETECT* — SDCONN_DETECT_L 1 IN 30
CR_CMD (IPU) — SDCONN_CMD 26 IN 30 97
CR_CLK — SDCONN_CLK 21 OUT 30 97
CR_DATA0 — SDCONN_DATA<0> 25 B4 30 97
CR_DATA1 — SDCONN_DATA<1> 24 B3 30 97
CR_DATA2 — SDCONN_DATA<2> 23 B2 30 97
CR_DATA3 — SDCONN_DATA<3> 22 B1 30 97
CR_DATA4 — SDCONN_DATA<4> 52 B4 30 97
CR_DATA5 — SDCONN_DATA<5> 53 B3 30 97
CR_DATA6 — SDCONN_DATA<6> 54 B2 30 97
CR_DATA7 — SDCONN_DATA<7> 55 B1 30 97
(IPU)

MS_INS* — TP_CE_L_MS_INS_L 59
CR_LED*/CR_BUS_PWR (IPU) — ENET_CR_PWREN 60 OUT 30
CR_WP* — SDCONN_WP 57 IN 30
SR_DISABLE — BDM57765_SR_DISABLE 68

TRD0_P — ENET_MDI_P<0> 40 B4 37 97
TRD0_N — ENET_MDI_N<0> 41 B3 37 97
TRD1_P — ENET_MDI_P<1> 44 B2 37 97
TRD1_N — ENET_MDI_N<1> 43 B1 37 97
TRD2_P — ENET_MDI_P<2> 46 B4 37 97
TRD2_N — ENET_MDI_N<2> 47 B3 37 97
TRD3_P — ENET_MDI_P<3> 50 B2 37 97
TRD3_N — ENET_MDI_N<3> 49 B1 37 97

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

BCM57765 supports both active-levels for WP.

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

R3980 1K 5% 1/16W MF-LF 402

SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)

72 36 24 7 =PP3V3_ENET_PHY
C3990 0.1UF 10% 16V X7R-CERM 402
U3990 AT45DB011D SOIC-BS1
VCC SCK SI CS* SO WP* RESET* GND
OMIT
36 BCM57765_SCLK
36 BCM57765_CS_L
BCM57765_MOSI 36
BCM57765_MISO 36
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

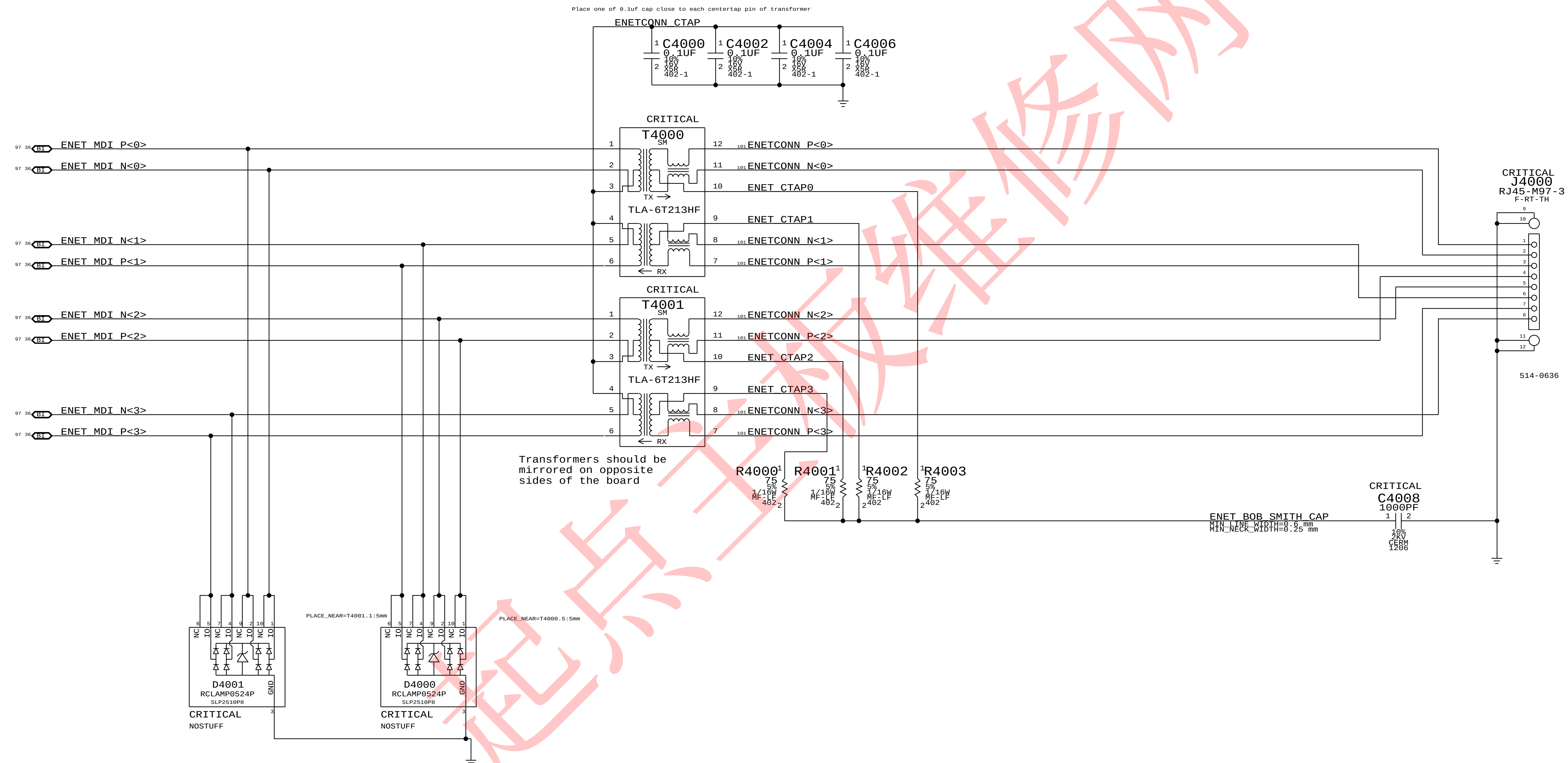
SYNC_MASTER=K91_ERIC SYNC_DATE=10/11/2010
PAGE TITLE
ETHERNET PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 39 OF 132
SHEET 36 OF 105

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K91_TRINHNI SYNC_DATE=05/26/2010

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH

=PP1V0_FW_FWPHY
135 mA
R4100 0 5% 1/10W MF-LF 402
PP1V0_FW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
L4110 120-OHM-0.3A-EMI 0402-LF
PP1V0_FW_FWPHY_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V

25 mA PCIe SerDes
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402

110 mA Digital Core
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402

7 mA I/O
C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402
=PP3V3_FW_FWPHY
138 mA

114 mA FireWire PHY
C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402
PP3V3_FW_FWPHY_VDDA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
L4130 120-OHM-0.3A-EMI 0402-LF

17 mA PCIe SerDes
C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402
PP3V3_FW_FWPHY_VP25
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
L4135 120-OHM-0.3A-EMI 0402-LF

0 mA VReg PWR
C4141 0.1UF 20% 10V CERM 402
C4140 1UF 10% 6.3V CERM 402

VDD10 VDD33 VDDH VP VP25 VREG_PWR

OMIT CRITICAL
U4100 FW643 BGA

NC ATBUSB
NC ATBUSH
NC ATBUSN

=FW_PHY_DS0 DS0 (IPD) NT-19
=FW_PHY_DS1 DS1 (IPD) NT-20
=FW_PHY_DS2 DS2 (IPD) NT-21

FW_P0_TPA_N TPA0N
FW_P0_TPA_P TPA0P
FW_P1_TPA_N TPA1N
FW_P1_TPA_P TPA1P
FW_P2_TPA_N TPA2N
FW_P2_TPA_P TPA2P
FW_P0_TPB_N TPB0N
FW_P0_TPB_P TPB0P
FW_P1_TPB_N TPB1N
FW_P1_TPB_P TPB1P
FW_P2_TPB_N TPB2N
FW_P2_TPB_P TPB2P

FW_P0_TPBIAS TPBIAS0
FW_P1_TPBIAS TPBIAS1
FW_P2_TPBIAS TPBIAS2

FW643_R0 R0
FW643_TPCPS TPCPS

TP_FW643_NAND_TREE NAND_TREE NT-OUT
FW643_REXT REXT
FW_CLK24P576M_XO_R XO
FW_CLK24P576M_XI XI NT-9

NOTE: NT-xx notes show NAND tree order.

TP_FW643_SE SE (IPD)
TP_FW643_SM SM (IPD)
TP_FW643_MODE_A MODE_A (IPD) NT-18
TP_FW643_CE CE (IPD)
TP_FW643_FW620_L FW620* (IPU)
TP_FW643_JASI_EN JASI_EN (IPD) NT-11
TP_FW643_AVREG AVREG
TP_FW643_VBUF VBUF
FW643_PU_RST_L FW_RESET* (IPU) NT-8
TP_FW643_OCR10_CTL OCR_CTL_V10
OCR_CTL_V12 (Reserved)

VSS VREG_VSS

PCI EXPRESS PHY
PCIE_RXD0N PCIE_FW_R2D_N
PCIE_RXD0P PCIE_FW_R2D_P
PCIE_TXD0N PCIE_FW_D2R_C_N
PCIE_TXD0P PCIE_FW_D2R_C_P
REFCLKN PCIE_CLK100M_FW_N
REFCLKP PCIE_CLK100M_FW_P

C4170 0.1UF 20% 16V X5R 402-1 PLACE_NEAR=U1800.AV34:2.54mm PCIE_FW_R2D_C_N
C4171 0.1UF 20% 16V X5R 402-1 PLACE_NEAR=U1800.AU34:2.54mm PCIE_FW_R2D_C_P
C4175 0.1UF 20% 16V X5R 402-1 PLACE_NEAR=U1800.BG36:2.54mm PCIE_FW_D2R_N
C4176 0.1UF 20% 16V X5R 402-1 PLACE_NEAR=U1800.BJ36:2.54mm PCIE_FW_D2R_P

TEST CONTROLLER
TCK TP_FW643_TCK
TDI TP_FW643_TDI
TDO TP_FW643_TDO
TMS TP_FW643_TMS
TRST* FW643_TRST_L

1394 PHY

POWER MANAGEMENT
WAKE* =FW_PME_L
REGCLT FW643_REGCTL
VAUX_DETECT FW643_VAUX_DETECT
VAUX_DISABLE TP_FW643_VAUX_ENABLE
CLKREQN =FW_CLKREQ_L

=PP3V3_FW_FWPHY
FW643_LDO
R4165 10K 5% 1/10W MF-LF 402
R4166 10K 5% 1/10W MF-LF 402
R4164 10K 5% 1/10W MF-LF 402

SCIF
SCIFCLK TP_FW643_SCIFCLK
SCIFDAIN TP_FW643_SCIFDAIN
SCIFDOUT TP_FW643_SCIFDOUT
SCIFMC TP_FW643_SCIFMC

SERIAL EEPROM CONTROLLER
SCL FW643_SCL
SDA TP_FW643_SDA

CHIP RESET
PERST* FW_RESET_L
R4163 10K 5% 1/10W MF-LF 402

=PPVP_FW_PHY_CPS
R4160 200K 1% 1/16W MF-LF 402
PLACE_NEAR=U4100.B10:2mm

C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO
CRITICAL
Y4150 24.576MHZ SM-3.2X2.5MM
NC
NC
R4150 412 1% 1/16W MF-LF 402

R4161 2.94K 1% 1/16W MF-LF 402
R4170 191 1% 1/16W MF-LF 402

R4162 470K 5% 1/16W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402

MISCELLANEOUS

SYNC MASTER=K18_MLB	SYNC DATE=04/27/2010
PAGE TITLE	FireWire LLC/PHY (FW643)
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 41 OF 132
	SHEET 38 OF 105

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

FireWire Port Power Switch

=PPBUS_S5_FWPWRSW

Q4262 provides for fast-off of Q4260 in S0 (Late-VG detection)

R4262 10K 5% 1/16W MF-LF 402
R4263 10 5% 1/16W MF-LF 402
FWPORT_FASTOFF_L_DIV
FWPORT_FASTOFF_L
Q4262 BSS8402DW SOT-363 (SYM-VER2) CRITICAL
=PP3V3_S0_FWLATEVG
FWPORT_PWR_EN

R4260 300K 5% 1/16W MF-LF 402
FWPORT_PWREN_L_DIV
C4260 0.1UF 10% 25V X5R 402
Q4260 FDC638P_G SM CRITICAL
PPBUS_FW_FWPWRSW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

F4260 1.1A-24V MINISMDC110H24 CRITICAL
PPBUS_FW_FWPWRSW_D
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

D4260 SBR3U30P1 PWRDI123 CRITICAL
=PPBUS_FW_FET

R4261 470K 5% 1/16W MF-LF 402
FWPORT_PWREN_L
Q4261 SSM3K15FV SOD-VESM-HF CRITICAL
NO STUFF
C4261 0.1UF 10% 25V X5R 402

Supervisor & CLKREQ# Isolation

=PP3V3_S0_FWPWRCTL
=PP3V3_FW_FWPHY

C4290 0.1UF 10% 25V X5R 402
U4290 SLG4AP016V TDFN CRITICAL
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
GND
THRM PAD
R4290 100K 5% 1/16W MF-LF 402
=PP1V0_FW_FWPHY

=FW_RESET_L
R4283 10K 5% 1/16W MF-LF 402
FW_RESET_R_L
FW_RESET_L
DLY = 60 ms +/- 20%

FW_PWR_EN
FW_CLKREQ_L
Pull-up provided by another page.
=FW_CLKREQ_L
FW_CLKREQ_PHY_L
MAKE_BASE=TRUE

FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.

=PP1V05_S0_FWPWRCTL
R4275 1K 5% 1/16W MF-LF 402
FW_PWR_EN_L
FW_PWR_EN
Q4275 DMB53D0UV SOT-563 CRITICAL

R4270 330K 5% 1/16W MF-LF 402
Q4270 BC847CDXV6TXG SOT563 CRITICAL
FWDET_MIRROR
FW_P1_TPBIAS_R
R4272 1K 5% 1/16W MF-LF 402
PLACE_NEAR=C4360.1:2 mm
FW_P1_TPBIAS

R4271 56K 5% 1/16W MF-LF 402
FW_5KPD_DET_RC
Q4270 BC847CDXV6TXG SOT563 CRITICAL
FWDET_EMIT
R4273 12K 5% 1/16W MF-LF 402

FW_5KPD_DET_L
MAKE_BASE=TRUE
Q4275 DMB53D0UV SOT-563 CRITICAL
C4270 0.1UF 10% 16V X5R 402

FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

=PP3V3_FW_FWPHY
R4277 10K 5% 1/16W MF-LF 402
R4276 100K 5% 1/16W MF-LF 402
FW_WAKE
Q4276 DMB53D0UV SOT-563 CRITICAL
NO STUFF
C4276 0.1UF 10% 16V X5R 402

=FW_PME_L
FW643_WAKE_L
MAKE_BASE=TRUE
Q4276 DMB53D0UV SOT-563 CRITICAL

Dual-purpose output:
1) 5K Pull-down Detect when FW_PWR_EN is low.
2) FW643 WAKE# (PME#) when PHY is powered.
Pull-up provided on another page.
FW_PME_L

3.3V FW Switch

=PP3V3_FW_P3V3FWFET
U4201 TPS22924 CSP CRITICAL
VIN VOUT ON GND
C4201 1UF 10% 6.3V CERM 402
=PP3V3_FW_FET
Max Current = 1.7A (85C)

U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch

=PP1V05_FW_P1V0FWFET
U4202 TPS22924 CSP CRITICAL
VIN VOUT ON GND
C4202 1UF 10% 6.3V CERM 402
PP1V05_FW_FET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
R4202 0.549 1% 1/16W MF 402
=PP1V0_FW_FET_R

LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

SYNC_MASTER=K91_MLB SYNC_DATE=06/17/2011

PAGE TITLE: FireWire Port & PHY Power

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 42 OF 132
SHEET 39 OF 105

Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

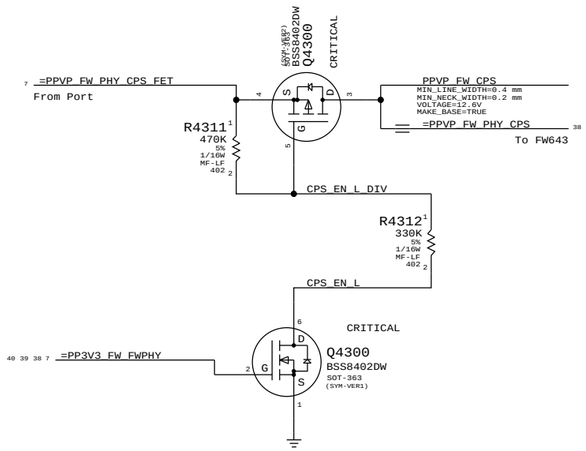
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

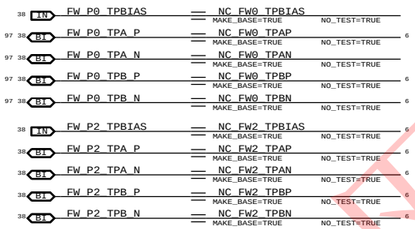
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



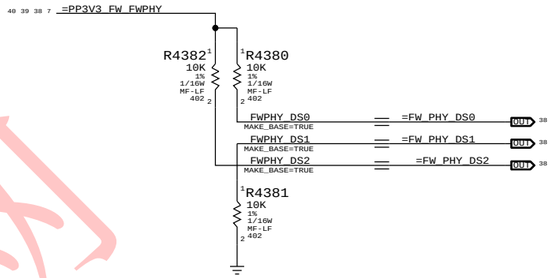
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



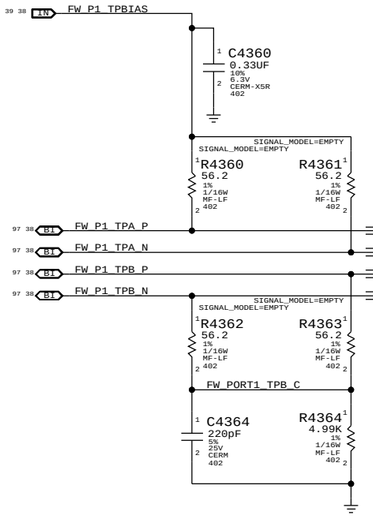
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

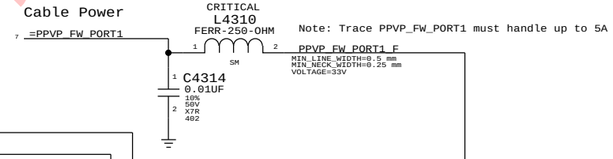


Termination

Place close to FireWire PHY

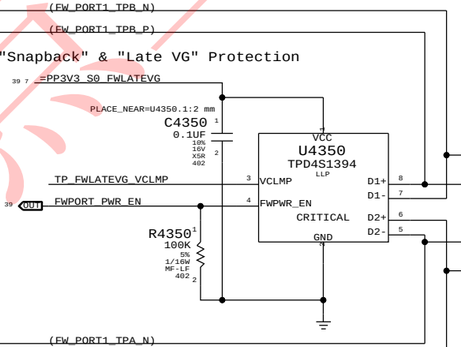


Cable Power



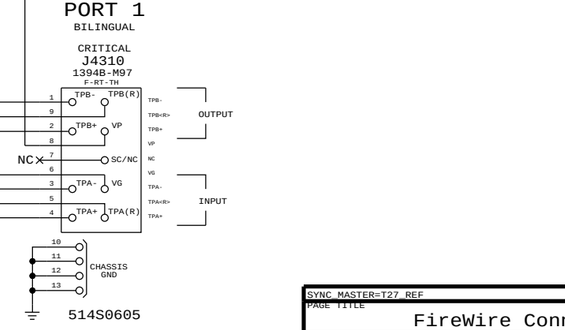
Note: Trace PPVP_FW_PORT1 must handle up to 5A

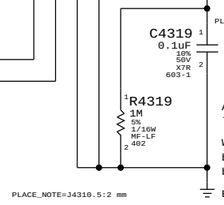
"Snapback" & "Late VG" Protection



PORT 1

BILINGUAL





AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

SYNC_MASTER=T27_REF SYNC_DATE=06/10/2010

PAGE TITLE: FireWire Connector

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 43 OF 132
SHEET: 40 OF 105

ODD Power Control

Note: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

=PP5V_S3_ODD
R4596 100K 5% 1/16W MF-LF 402
C4595 0.068UF 10% 10V CERM 402
Q4590 DMP2018LFK DFN2563-6 CRITICAL
PP5V_SW_ODD
C4596 0.01UF 10% 16V CERM 402
ODD_PWR_EN_LS5V_L
R4595 100K 5% 1/16W MF-LF 402
ODD_PWR_SS
=PP3V3_S0_ODD
R4597 100K 5% 1/16W MF-LF 402
Q4596 SSM6N37FEAPE SOT563
ODD_PWR_EN
Q4596 SSM6N37FEAPE SOT563
IN ODD_PWR_EN_L

SATA ODD Connector

J4500 54722-0164 F-ST-SM CRITICAL 516S0616
SATA_ODD_R2D_P → C4521 0.01UF → SATA_ODD_R2D_C_P
SATA_ODD_R2D_N → C4520 0.01UF → SATA_ODD_R2D_C_N
SATA_ODD_D2R_C_N → C4526 0.01UF → SATA_ODD_D2R_N
SATA_ODD_D2R_C_P → C4525 0.01UF → SATA_ODD_D2R_P
=PP3V3_S0_ODD
R4590 33K 5% 1/16W MF-LF 402
OUT SMC_ODD_DETECT
Note: Indicates disc presence.

SATA HDD Connector (Gen3)

PP5V_S0_HDD_FLT
L4500 FERR-70-OHM-4A 0603 CRITICAL
PP5V_S0_HDD_R
CRITICAL R4599 0.001 1% 1W MF-1 0612
=PP5V_S0_HDD
ISNS_HDD_P
ISNS_HDD_N
C4501 0.1UF 20% 10V CERM 402
C4502 0.1UF 20% 10V CERM 402
=PP3V3_S0_HDD
R4538 100K 5% 1/16W MF-LF 402
NOSTUFF C4537 100UF 20% 16V X5R-CERM 1206
NOSTUFF C4538 100UF 20% 16V X5R-CERM 1206
SSD_OOBR2D_L → R4537 453 1% 1/16W MF-LF 402 → SMC_SSD_OOBR2D_L
SSD_OOBD2R_L → L4539 FERR-220-OHM 0402 → SSD_OOBD2R_FTL_L
SYS_LED_ANODE_R → R4531 4.7 5% 1/16W MF-LF 402 → SYS_LED_ANODE
C4531 0.001UF 10% 50V CERM 402
IR_RX_OUT
=PP5V_S3_IR
R4532 0 5% 1/16W MF-LF 402
PP5V_S3_IR_R
C4532 0.1UF 10% 16V X7R-CERM 402
J4501 54722-0224 F-ST-SM 516S0687 CRITICAL
GND_VOID

D2R Passive DeEmphasis

VALUE: 4.5 DB

SATA_HDD_D2R_C_P → R4536 68.1 → C4536 5.0PF → SATA_HDD_D2R_RC_P → C4516 0.01UF → SATA_HDD_D2R_RDRIN_P
SATA_HDD_D2R_C_N → C4535 5.0PF → R4535 68.1 → SATA_HDD_D2R_RC_N → C4515 0.01UF → SATA_HDD_D2R_RDRIN_N

R2D Passive DeEmphasis

VALUE: 3.0 DB

SATA_HDD_R2D_N → R4534 41.2 → C4534 15PF → SATA_HDD_R2D_RC_N → C4511 0.01UF → SATA_HDD_R2D_RDROUT_N
SATA_HDD_R2D_P → C4533 15PF → R4533 41.2 → SATA_HDD_R2D_RC_P → C4510 0.01UF → SATA_HDD_R2D_RDROUT_P

SATA OOB Comparator

Notes:
OOBD2R was OOB_TEMP, from SSD, to SMC
OOBR2D was TEMP_CTL, from SMC, to SSD

=PP3V3_S0_SMC
=PP1V5_S0_RDRVR
R4581 100K 5% 1/16W MF-LF 402
R4583 49.9K 1% 1/16W MF-LF 402
C4580 0.1UF 20% 10V CERM 402
R4585 1K 5% 1/16W MF-LF 402
SSD_OOB1V0REF
U4580 LMV331 SC70-5
SSD_OOBD2R_FTL_L
R4582 3.3K 5% 1/16W MF-LF 402
SSD_OOBD2R_R_L
R4584 100K 5% 1/16W MF-LF 402
C4584 0.1UF 20% 10V CERM 402
SMC_SSD_OOBD2R_R_L
R4586 0 5% 1/16W MF-LF 402
SMC_SSD_OOBD2R_L

SATA Redriver

Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

=PP1V5_S0_RDRVR
R4513 4.7K 5% 1/16W MF-LF 402
NO STUFF R4515 4.7K 5% 1/16W MF-LF 402
SATARDRVR_I2C_ADDR0
SATARDRVR_I2C_ADDR1

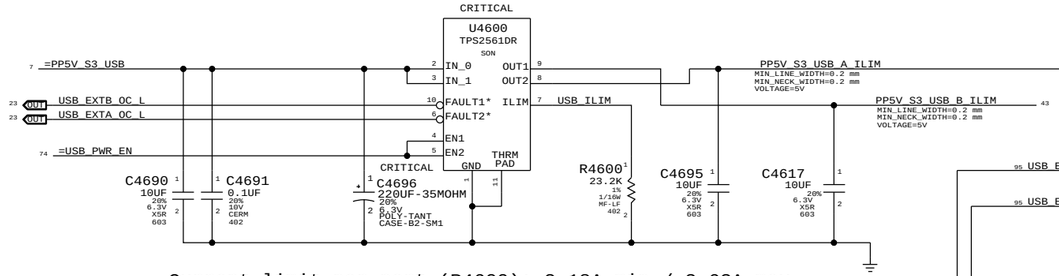
=PP1V5_S0_RDRVR
R4510 4.7K 5% 1/16W MF-LF 402
NOSTUFF
C4514 0.1UF 20% 16V CERM 402
C4519 0.01UF 20% 10V CERM 402
C4518 & C4517 Placement Note:
It is critical that these two should be near to U1800 pin AM1 and AM3.

U4510 PS8521A TQFN 338S0907 CRITICAL
A_INP A_INN B_OUTN B_OUTP EN B_PRE0/I2C_ADDR0 APRE0/I2C_ADDR1 I2C_EN* TEST
A_OUTP A_OUTN B_INN B_INP REXT A_PRE1/SCL_CTL B_PRE1/SDA_CTL
GND THRM PAD
SATARDRVR_EN
SATARDRVR_I2C_ADDR0
SATARDRVR_I2C_ADDR1
SATARDRVR_I2C_EN_L
SATARDRVR_TEST
SATARDRVR_REXT
=SATARDRVR_I2C_SCL
=SATARDRVR_I2C_SDA
R4511 0 5% 1/16W MF-LF 402
R4512 3.74K 1% 1/16W MF-LF 402

SATA_HDD_D2R_RDROUT_P → C4518 0.01UF → SATA_HDD_D2R_P
SATA_HDD_D2R_RDROUT_N → C4517 0.01UF → SATA_HDD_D2R_N
SATA_HDD_R2D_RDRIN_N → C4513 0.01UF → SATA_HDD_R2D_C_N
SATA_HDD_R2D_RDRIN_P → C4512 0.01UF → SATA_HDD_R2D_C_P

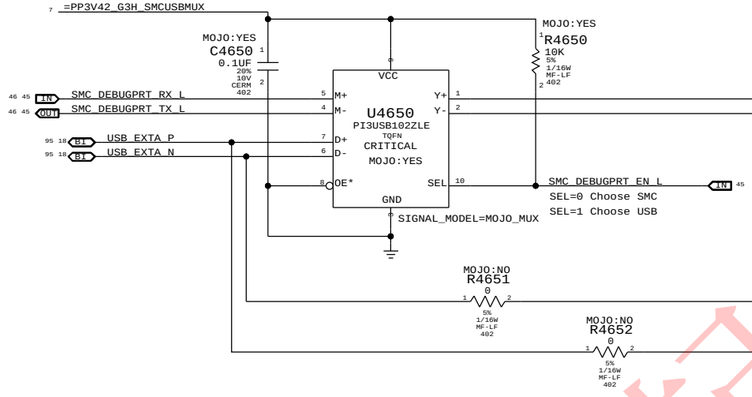
SYNC_MASTER=J31_YONAS SYNC_DATE=11/17/2011
PAGE TITLE: SATA Redriver/Conn, IR, SIL
Apple Inc.
DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 45 OF 132
SHEET 41 OF 105

USB Port Power Switch

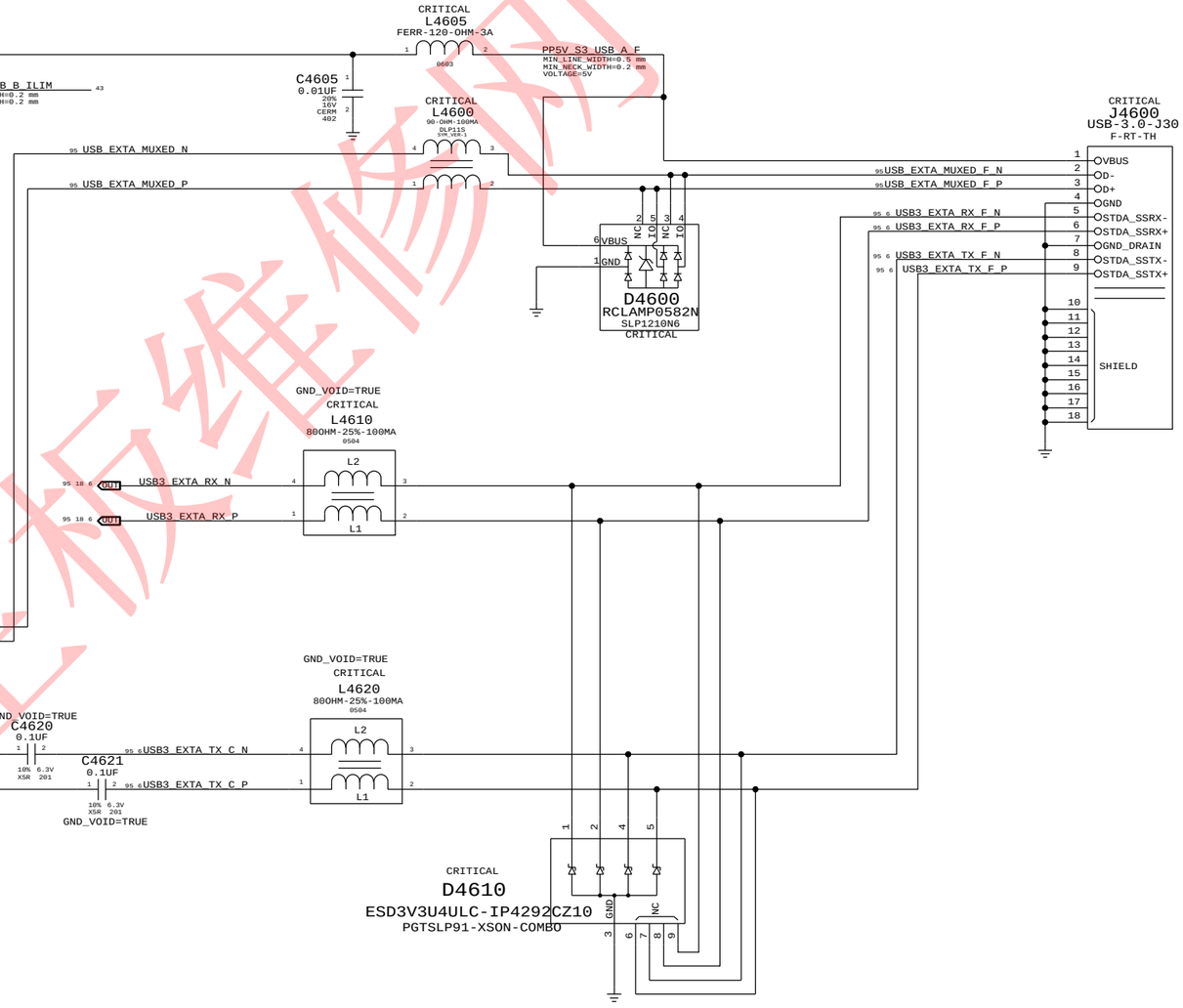


Current limit per port (R4600): 2.18A min / 2.63A max

Mojo SMC Debug Mux



USB Port A (Front Port)



SYNC_MASTER=J31_LINDA SYNC_DATE=09/21/2011

PAGE TITLE: External A USB3 Connector

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

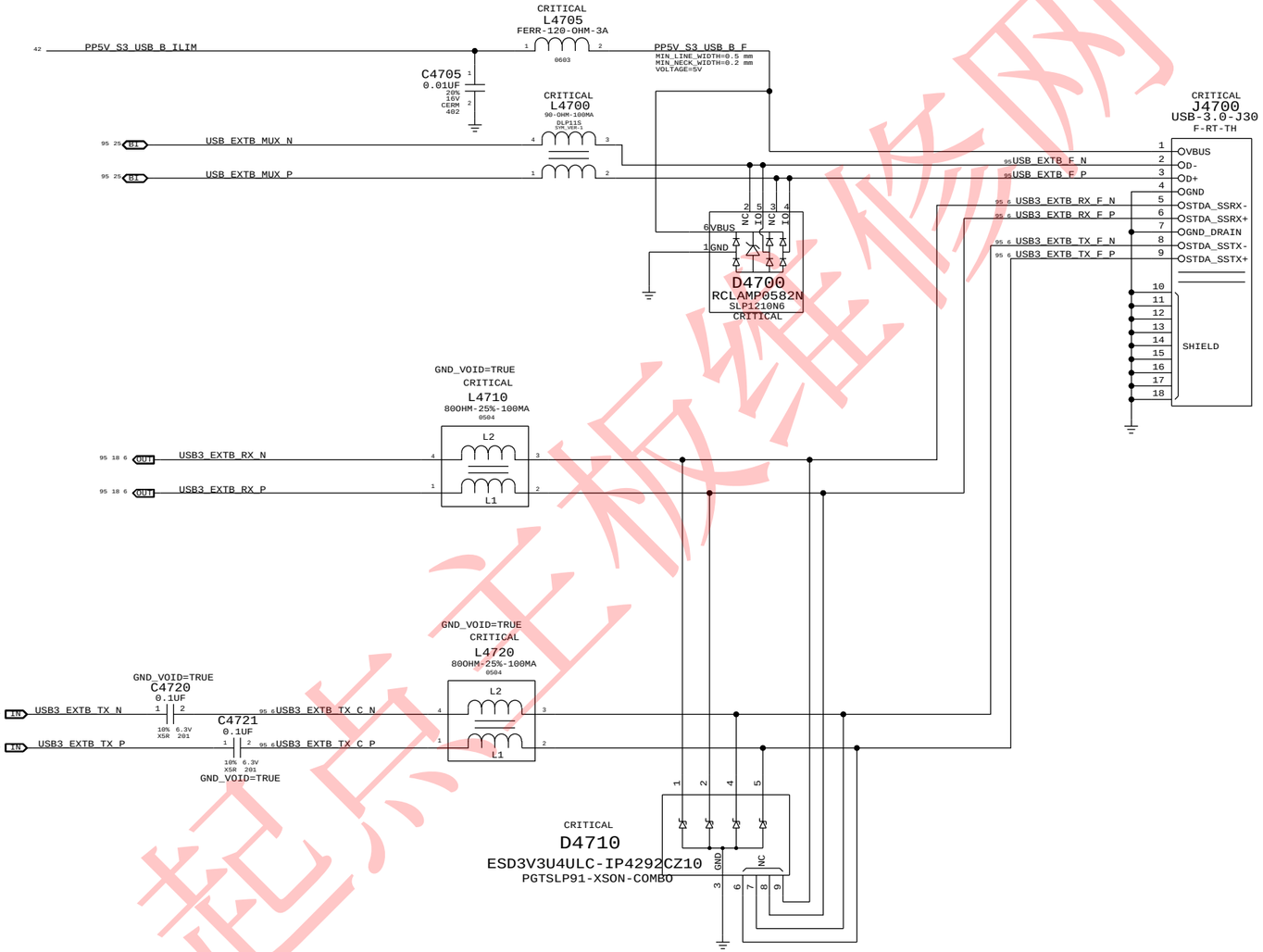
REVISION: 3.0.0

BRANCH:

PAGE: 46 OF 132

SHEET: 42 OF 105

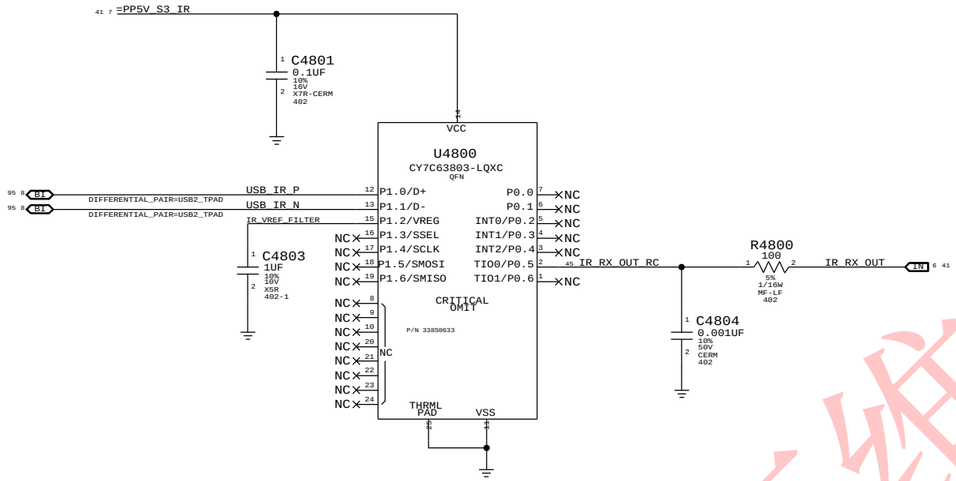
USB Port B (Back Port)



NOTE: Swapped pin4 and 5, pin6 and 7 for layout.

SYNC_MASTER=J30_MLB	SYNC_DATE=08/04/2011
PAGE TITLE	External B USB3 Connector
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 47 OF 132
	SHEET 43 OF 105

IR SUPPORT

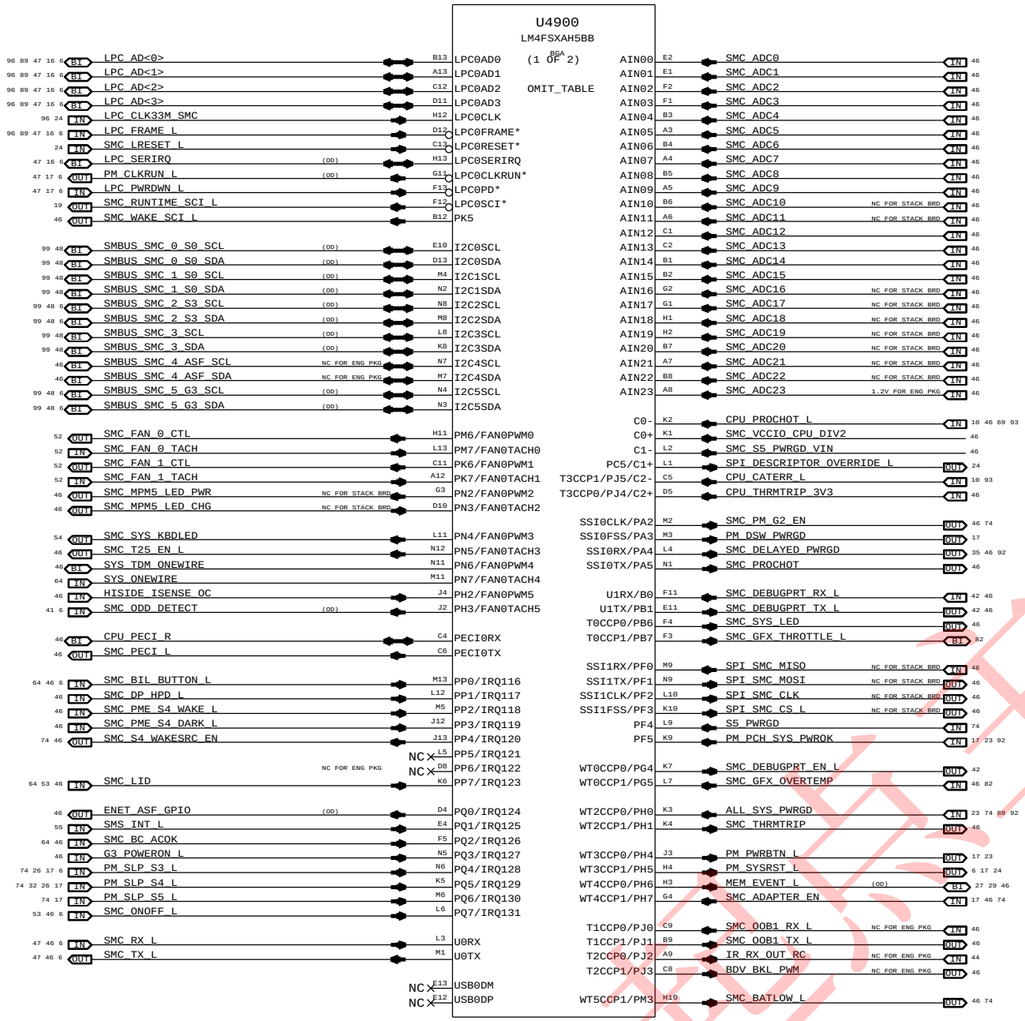


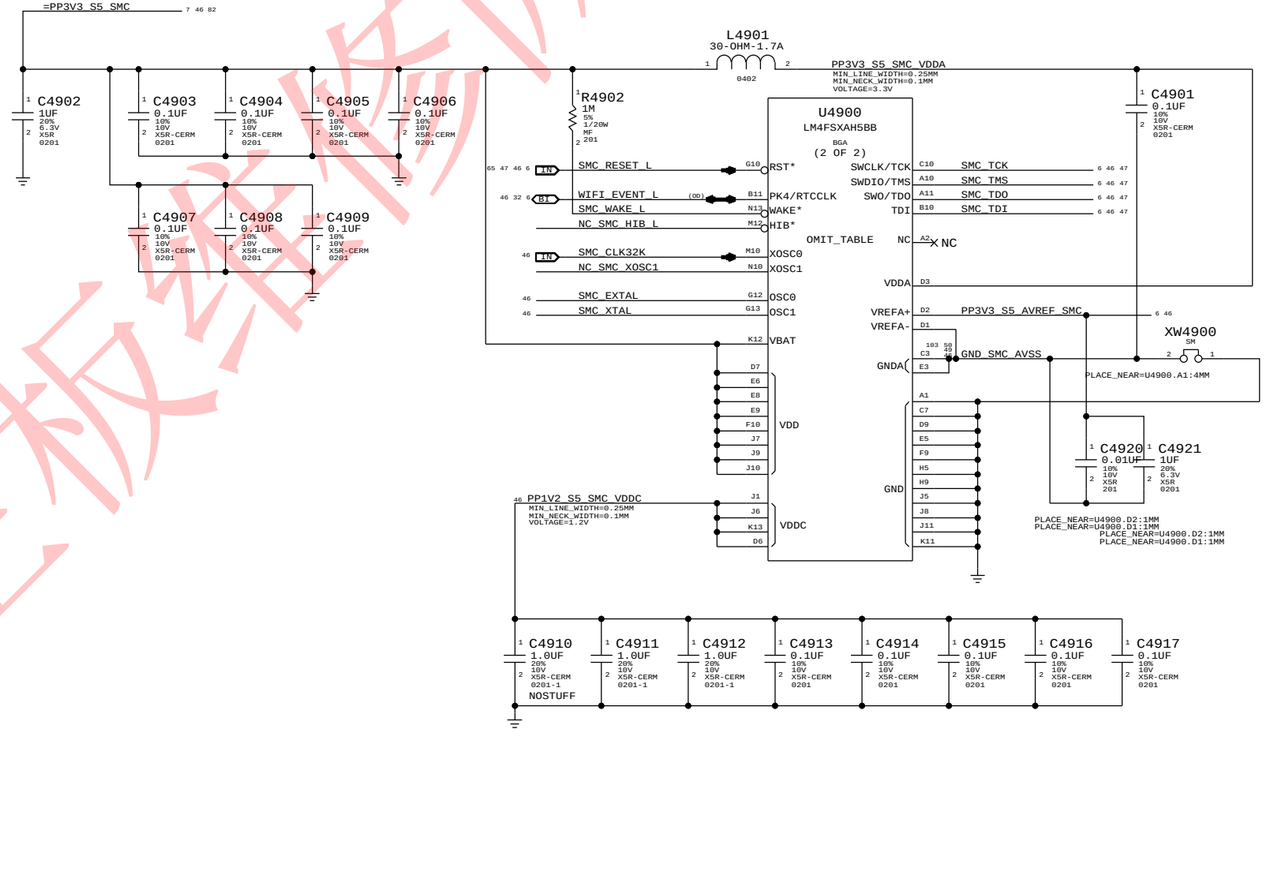
SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE
Front Flex Support

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 48 OF 132
SHEET 44 OF 105





NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

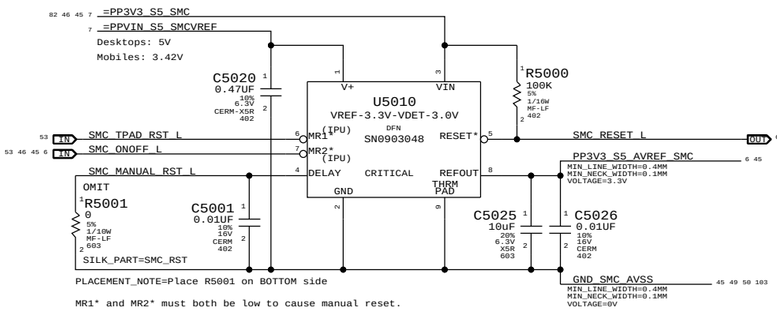
SYNC_MASTER=J31_YONAS SYNC_DATE=12/19/2013

PAGE TITLE: SMC

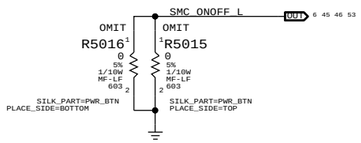
Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 49 OF 132
SHEET: 45 OF 105

SMC Reset "Button", Supervisor & AVREF Supply



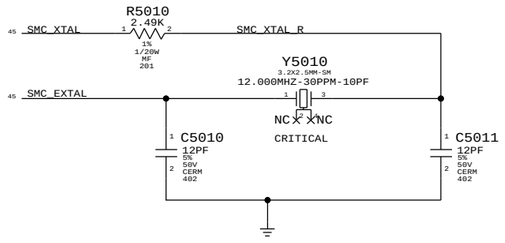
Debug Power "Buttons"



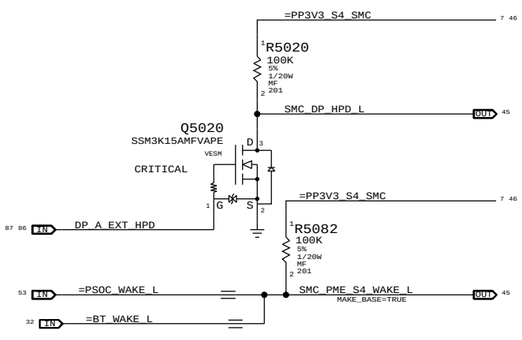
Note:
ADC10 and ADC11 are
share with comparators
on Stack Board.

SMC Crystal Circuit

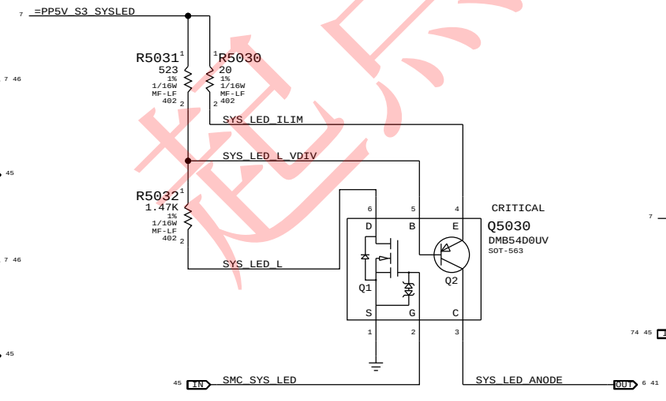
SMC USB Clock require 12 MHz.



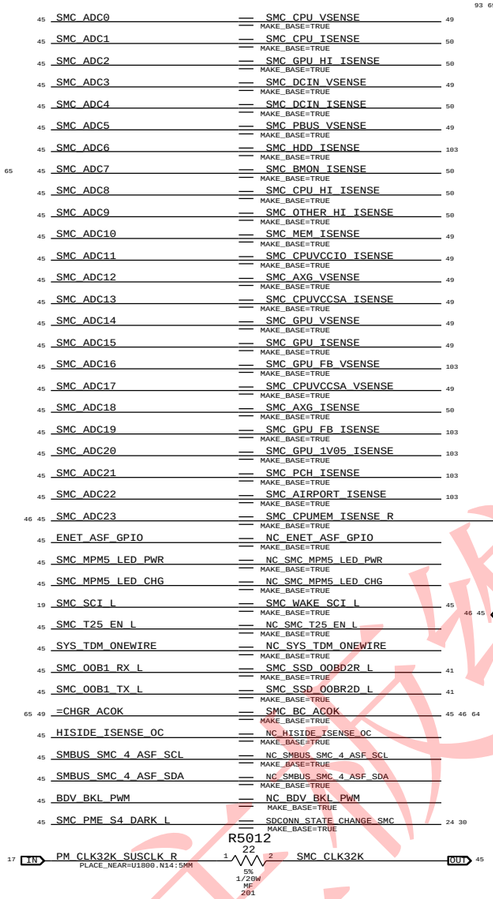
S4 HPD SMC Wake Source



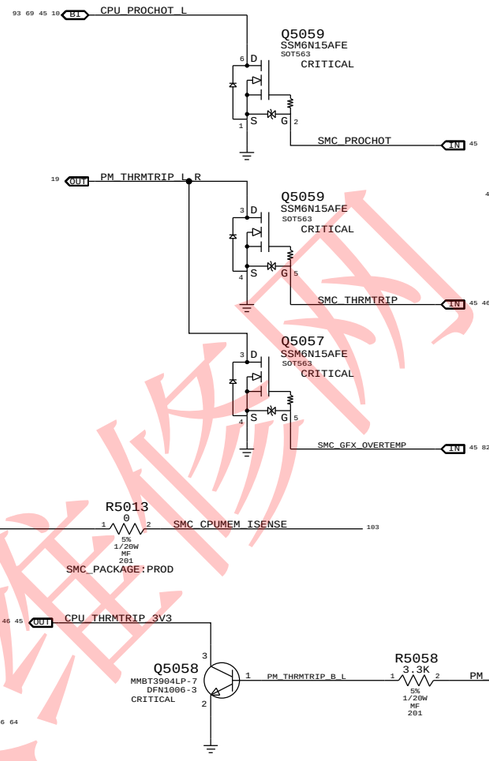
System (Sleep) LED Circuit



SMC Signal Connections



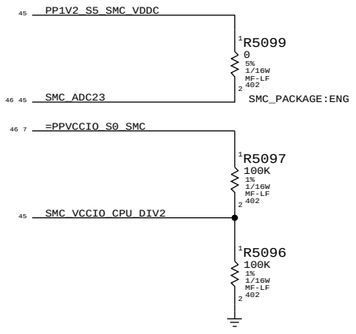
CPU_PROCHOT_L / PM_THRMTRIP_L_R



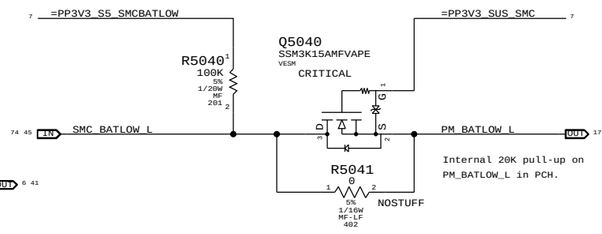
R5013 / CPU_THRMTRIP_3V3

SCM12 Eng Pkg Support

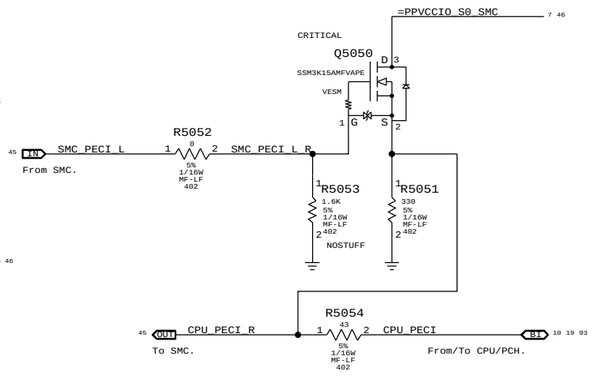
Eng Package requires 1.2V ON SMC_ADC23 pin.



BATLOW# Isolation

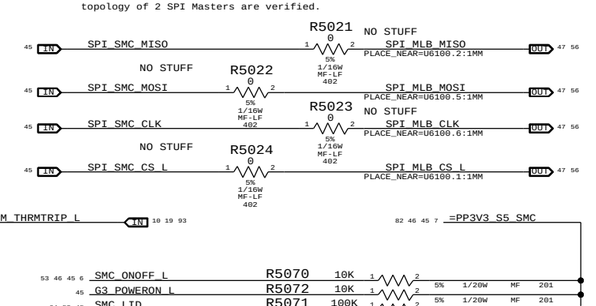


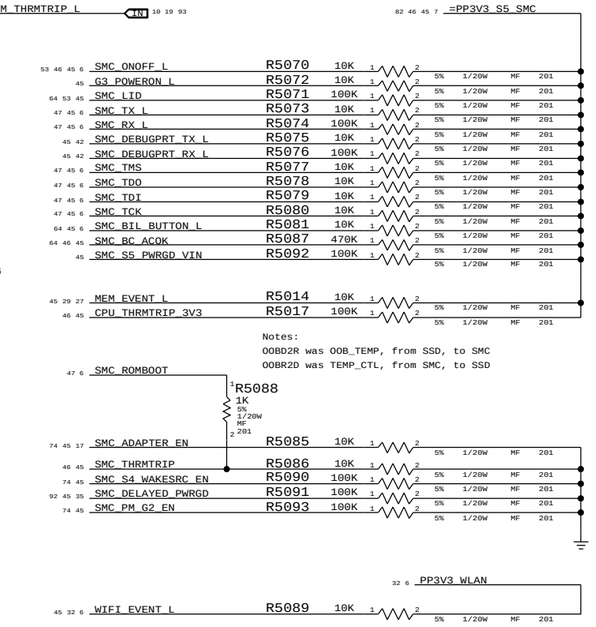
SMC12 PECI Support



SMC12 SPI Support

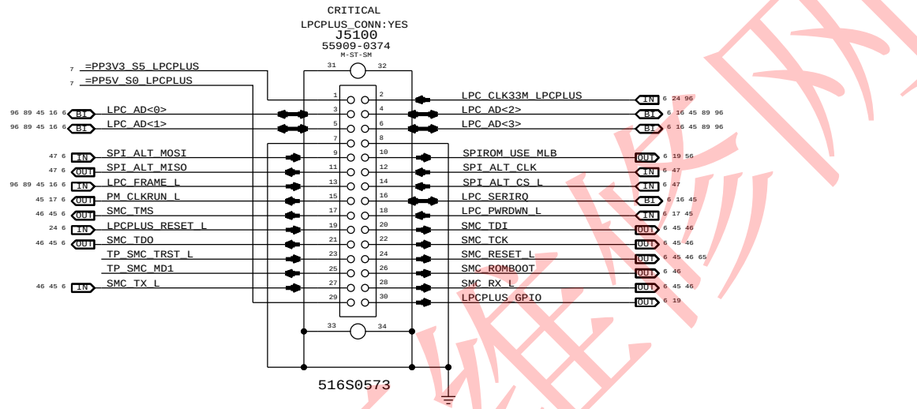
Series resistors are no stuffed until the
topology of 2 SPI Masters are verified.



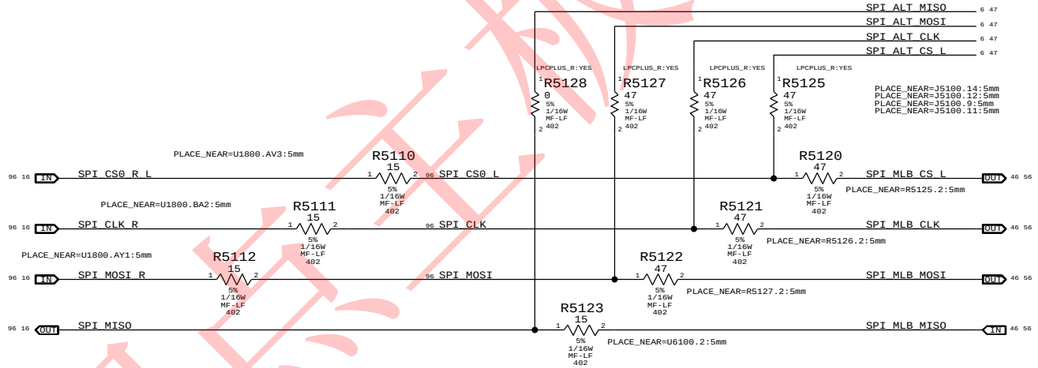


SYNC_MASTER=J31_YONAS	SYNC_DATE=01/19/2012
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-9585
	SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 50 OF 132
	SHEET 46 OF 105

LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=J5_MLB	SYNC_DATE=05/26/2011
PAGE TITLE	LPC+SPI Debug Connector
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 51 OF 132
	SHEET 47 OF 105

PCH SMBus "0" Connections

=PP3V3_S0_SMBUS_PCH

Panther Point U1800 (MASTER)
- SMBUS_PCH_CLK (MAKE_BASE=TRUE)
- SMBUS_PCH_DATA (MAKE_BASE=TRUE)

R5200 1K 5% 1/16W MF-LF 402 — R5201 1K 5% 1/16W MF-LF 402

SO-DIMM "A" J2900 (Write: 0xA0 Read: 0xA1)
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

VRef DACs U3300 (Write: 0x98 Read: 0x99)
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA

SO-DIMM "B" J3100 (Write: 0xA4 Read: 0xA5)
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

Margin Control U3301 (Write: 0x30 Read: 0x31)
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

SATA Redriver U4510 (Write: 0xB6 Read: 0xB7)
- =SATARDRVR_I2C_SCL
- =SATARDRVR_I2C_SDA

LED BACKLIGHT U9701 (WRITE: 0x58 READ: 0x59)
- =I2C_BKL_1_SCL
- =I2C_BKL_1_SDA

XDP Connectors J2500 & J2550 (MASTER)
- =SMBUS_XDP_SCL
- =SMBUS_XDP_SDA

Mikey U6880 (Write: 0x72 Read: 0x73)
- =I2C_MIKEY_SCL
- =I2C_MIKEY_SDA

SDRVI2C:SB
R5236 0 5% 1/20W MF 201
R5237 0 5% 1/20W MF 201

DP SDRV "A" U9310 (Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL (MAKE_BASE=TRUE) → =I2C_DPSDRVA_SCL
- I2C_DPSDRVA_SDA (MAKE_BASE=TRUE) → =I2C_DPSDRVA_SDA

PCH "SMLink 0" Connections

=PP3V3_S0_SMBUS_PCH

Panther Point U1800 (MASTER)
- SML_PCH_0_CLK (MAKE_BASE=TRUE)
- SML_PCH_0_DATA (MAKE_BASE=TRUE)

R5210 8.2K 5% 1/16W MF-LF 402 — R5211 8.2K 5% 1/16W MF-LF 402

PCH "SMLink 1" Connections

=PP3V3_S0_SMBUS_PCH

Panther Point U1800 (Write: 0x88 Read: 0x89)
- SML_PCH_1_CLK (MAKE_BASE=TRUE)
- SML_PCH_1_DATA (MAKE_BASE=TRUE)

NO STUFF R5220 8.2K 5% 1/16W MF-LF 402 — NO STUFF R5221 8.2K 5% 1/16W MF-LF 402

R5223 0 5% 1/16W MF-LF 402

R5222 0 5% 1/16W MF-LF 402

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

SMC U4900 (MASTER)
- SMB_0_S0_CLK → SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
- SMB_0_S0_DATA → SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

R5250 4.7K 5% 1/16W MF-LF 402 — R5251 4.7K 5% 1/16W MF-LF 402

GPU Temp (Ext) EMC1414-A: U5550 (Write: 0x98 Read: 0x99)
- =I2C_GPUTHMSNS_SCL
- =I2C_GPUTHMSNS_SDA

GPU Temp (Int) KEPLER: U8000 (Write: 0x82 Read: 0x83)
- GPU_SMB_CLK_R
- GPU_SMB_DAT_R

SMC "2" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_2_S3

SMC U4900 (MASTER)
- SMB_2_S3_CLK → SMBUS_SMC_2_S3_SCL (MAKE_BASE=TRUE)
- SMB_2_S3_DATA → SMBUS_SMC_2_S3_SDA (MAKE_BASE=TRUE)

R5270 1K 5% 1/16W MF-LF 402 — R5271 1K 5% 1/16W MF-LF 402

Trackpad J5800 (Write: 0x90 Read: 0x91)
- =I2C_TPAD_SCL
- =I2C_TPAD_SDA

J3401 ALS (Write: 0x72 Read: 0x73) Lid Angle Detect (Write: 0x32 Read: 0x33)
- =I2C_ALS_SCL
- =I2C_ALS_SDA

Digital SMS LIS331DLH: U5920 (Write: 0x30 Read: 0x31)
- =I2C_SMC_SMS_SCL
- =I2C_SMC_SMS_SDA

SMC "1" SMBus Connections

=PP3V3_S0_SMBUS_SMC_1_S0

SMC U4900 (MASTER)
- SMB_1_S0_CLK → SMBUS_SMC_1_S0_SCL (MAKE_BASE=TRUE)
- SMB_1_S0_DATA → SMBUS_SMC_1_S0_SDA (MAKE_BASE=TRUE)

R5260 4.7K 5% 1/16W MF-LF 402 — R5261 4.7K 5% 1/16W MF-LF 402

CPU Temp EMC1414-A: U5570 (Write: 0x98 Read: 0x99)
- =I2C_CPUTHMSNS_SCL
- =I2C_CPUTHMSNS_SDA

T29 Temp EMC1412-A: U5520 (Write: 0x90 Read: 0x91)
- =I2C_T29THMSNS_SCL
- =I2C_T29THMSNS_SDA

SMC "5" SMBus Connections

=PP3V42_G3H_SMBUS_SMC_5

SMC U4900 (MASTER)
- SMB_5_CLK → SMBUS_SMC_5_G3_SCL (MAKE_BASE=TRUE)
- SMB_5_DATA → SMBUS_SMC_5_G3_SDA (MAKE_BASE=TRUE)

R5280 2.0K 5% 1/16W MF-LF 402 — R5281 2.0K 5% 1/16W MF-LF 402

Battery Charger ISL6258 - U7000 (Write: 0x12 Read: 0x13)
- =SMBUS_CHGR_SCL
- =SMBUS_CHGR_SDA

Battery J6955 (See Table)
- =SMBUS_BATT_SCL
- =SMBUS_BATT_SDA

Battery
Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x92 Read: 0x93)

SMC "3" SMBus Connections

=PP3V3_S3_SMBUS_SMC_3

SMC U4900 (MASTER)
- SMB_3_CLK → SMBUS_SMC_3_SCL (MAKE_BASE=TRUE)
- SMB_3_DATA → SMBUS_SMC_3_SDA (MAKE_BASE=TRUE)

R5290 4.7K 5% 1/16W MF-LF 402 — R5291 4.7K 5% 1/16W MF-LF 402

Sensor ADC A U5930 (Write: 0x10 Read: 0x11)
- =I2C_SMC_ADCS_SCL
- =I2C_SMC_ADCS_SDA

T29 SMBus Connections

=PP3V3_S0_T29I2C

T29 IC U3600 (MASTER)
- I2C_TBT_SCL (MAKE_BASE=TRUE)
- I2C_TBT_SDA (MAKE_BASE=TRUE)

R5230 4.7K 5% 1/16W MF-LF 402 — R5231 4.7K 5% 1/16W MF-LF 402

T29 Port A MCU J9330 (Write: 0x26 Read: 0x27)
- =I2C_TBTAMCU_SCL
- =I2C_TBTAMCU_SDA

SDRVI2C:MCU
R5234 0 5% 1/20W MF 201
R5235 0 5% 1/20W MF 201

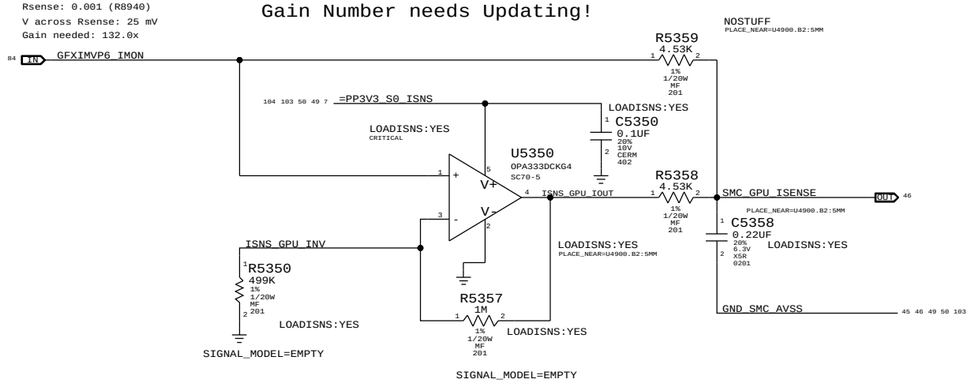
DP SDRV "A" U9310 (Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL (MAKE_BASE=TRUE) → =I2C_DPSDRVA_SCL
- I2C_DPSDRVA_SDA (MAKE_BASE=TRUE) → =I2C_DPSDRVA_SDA

SYNC_MASTER=K18_MLB	SYNC_DATE=04/27/2010
PAGE TITLE	SMBus Connections
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 52 OF 132
	SHEET 48 OF 105

GPU Core Load Side Current Sense (IG0C)

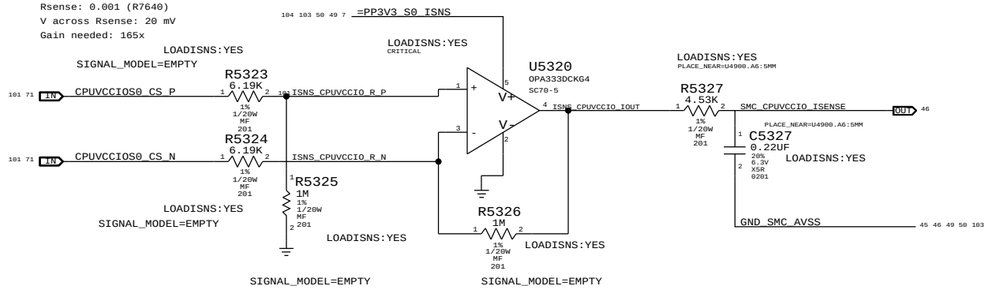
Gain: 130.2x, EDP: 25 A
Rsense: 0.001 (R8940)
V across Rsense: 25 mV
Gain needed: 132.0x

Gain Number needs Updating!



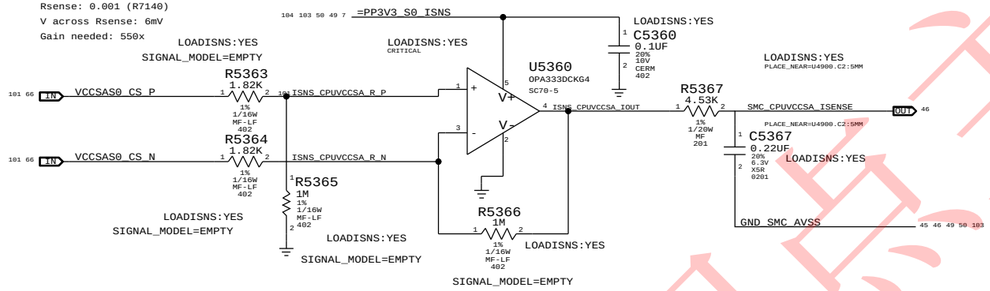
CPU VCCIO 1.05V Load Side Current Sense (IC1C)

Gain: 161.5x, EDP: 20 A
Rsense: 0.001 (R7640)
V across Rsense: 20 mV
Gain needed: 165x



CPU VCCSA Load Side Current Sense (IC2C)

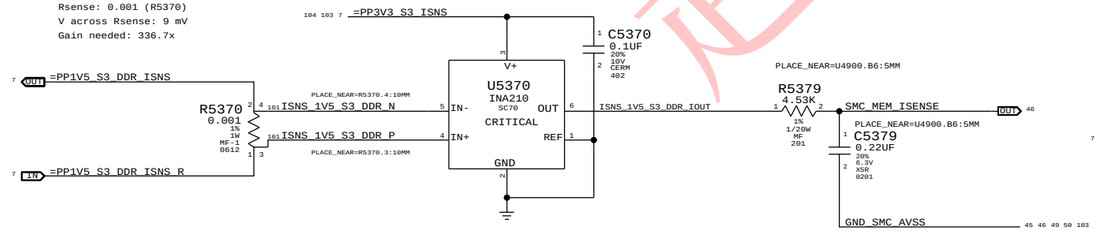
Gain: 549x, EDP: 6A
Rsense: 0.001 (R7140)
V across Rsense: 6mV
Gain needed: 550x



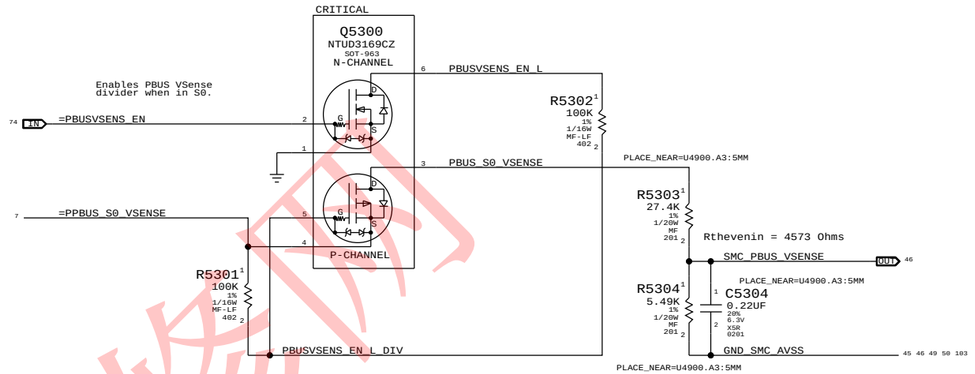
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,100K,201	C5358,C5327,C5367		LOADISNS:NO

DDR 1.5V S3 (Memory) Current Sense (IM0C)

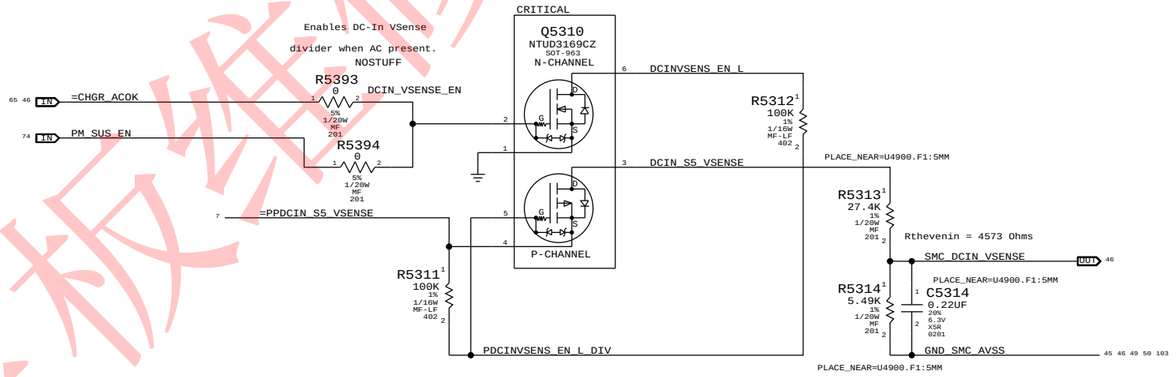
Gain: 200x, EDP: 9A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
Gain needed: 336.7x



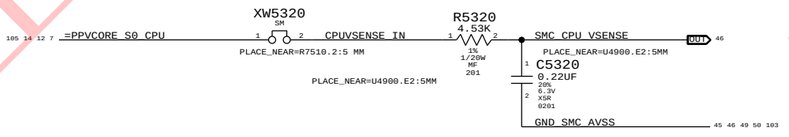
PBUS Voltage Sense & Enable (VP0R)



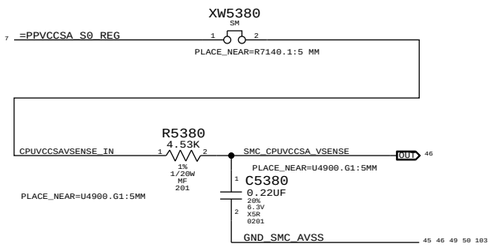
DC-In Voltage Sense & Enable (VD0R)



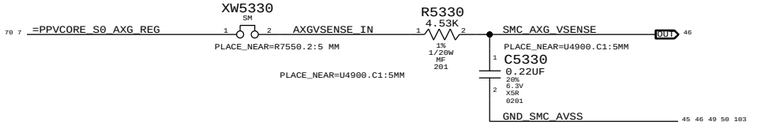
CPU Core Voltage Sense (VC0C)



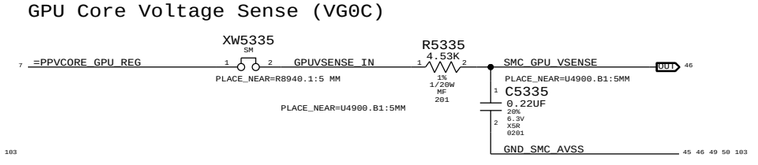
CPU VCCSA Voltage Sense (VC2C)



AXG Core Voltage Sense (VN0C)



GPU Core Voltage Sense (VG0C)



SYNC_MASTER=J31_YONAS SYNC_DATE=01/19/2012

PAGE TITLE

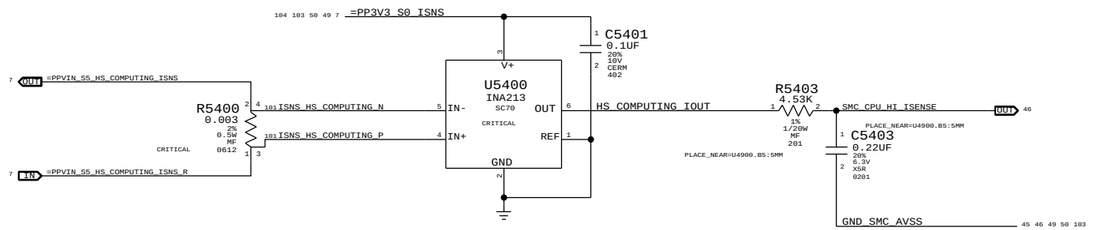
Power Sensors: Load Side

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 53 OF 132
SHEET 49 OF 105

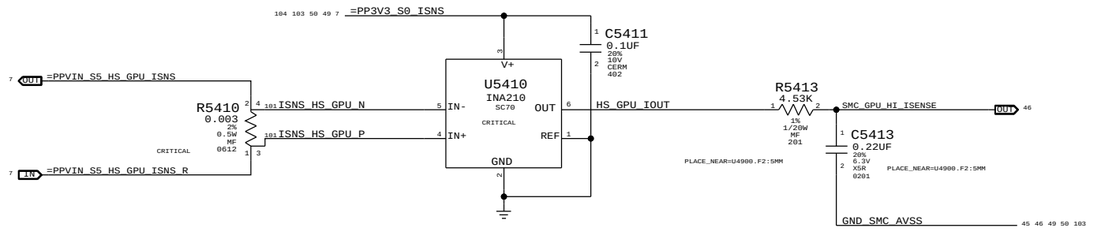
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 22.8 A
Rsense: 0.003 (R5400)
V across Rsense: 68.4 mV
Gain needed: 48.25x



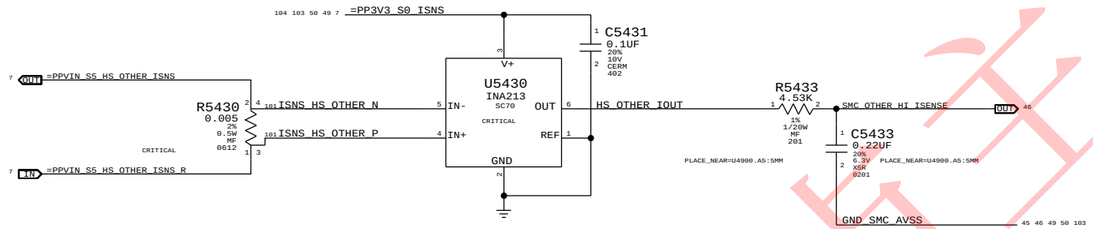
GPU High Side Current Sense (IG0R)

Gain: 200x, EDP: 5.2 A (Kepler)
Rsense: 0.003 (R5410)
V across Rsense: 15.6 mV
Gain needed: 211.54x (Kepler)



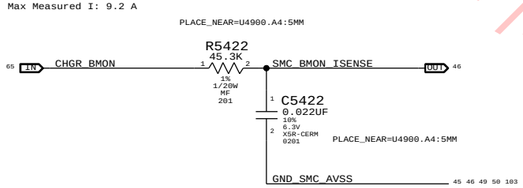
OTHER High Side Current Sense (IO0R)

Gain: 50x, EDP: 10.3 A
Rsense: 0.005 (R5440)
V across Rsense: 51.5 mV
Gain needed: 64.1x



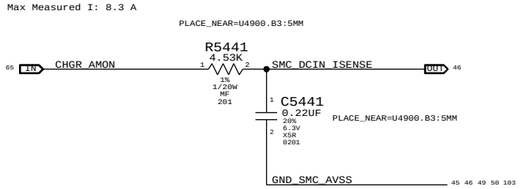
Charger (BMON Prod) Current Sense (IPBR)

Charger Gain: 36x
Rsense: 0.010 (R7050)
Max Measured I: 9.2 A



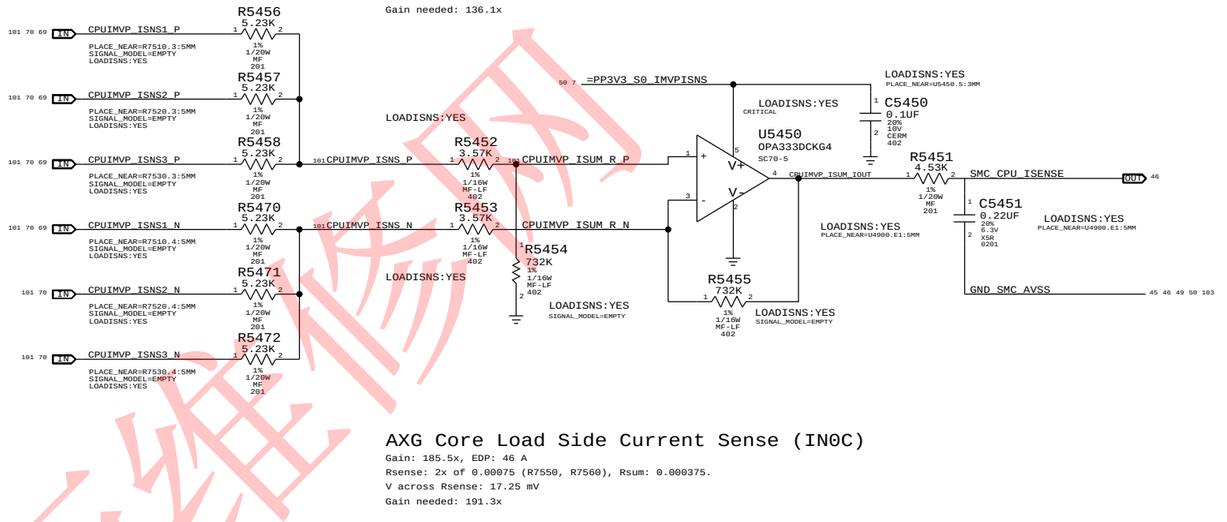
DC-In (AMON) Current Sense (ID0R)

Charger Gain: 20x
Rsense: 0.020 (R7020)
Max Measured I: 8.3 A



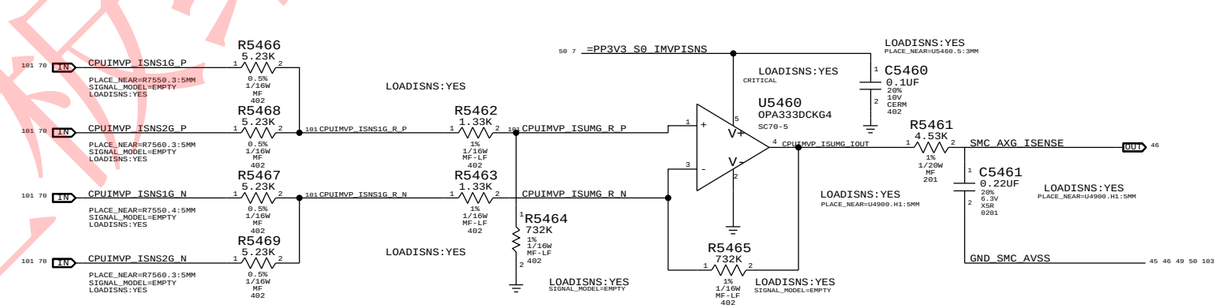
CPU Core Load Side Current Sense (IC0C)

Gain: 136.1x, EDP: 97 A
Rsense: 3x of 0.00075 (R7510, R7520. R7530), Rsum: 0.00025.
V across Rsense: 24.25 mV
Gain needed: 136.1x



AXG Core Load Side Current Sense (IN0C)

Gain: 185.5x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375.
V across Rsense: 17.25 mV
Gain needed: 191.3x



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,100K,201	C5451,C5461		LOADISNS:NO

SYNC_MASTER=J31_YONAS SYNC_DATE=10/25/2011

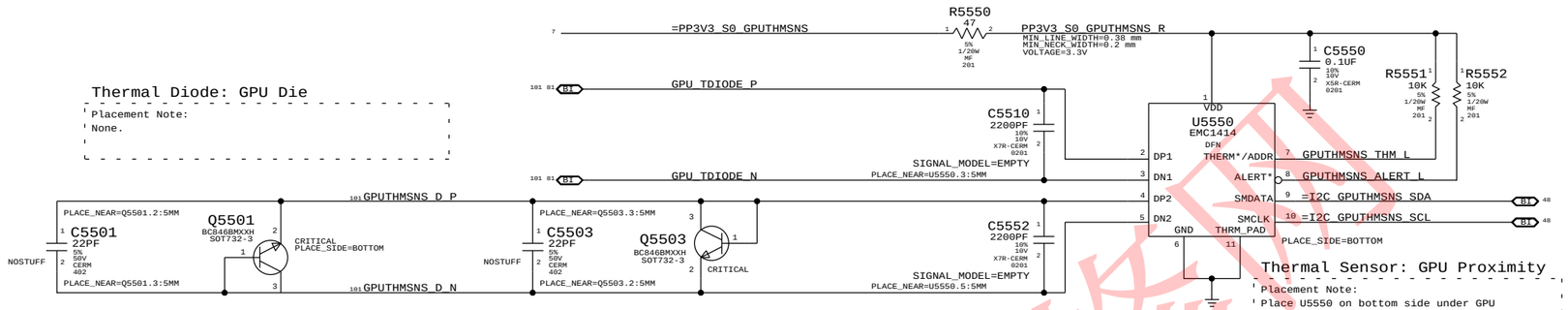
PAGE TITLE
Power Sensors: High Side, CPU, AXG

Apple Inc.

DRAWING NUMBER 051-9585
SIZE D
REVISION 3.0.0
BRANCH
PAGE 54 OF 132
SHEET 50 OF 105

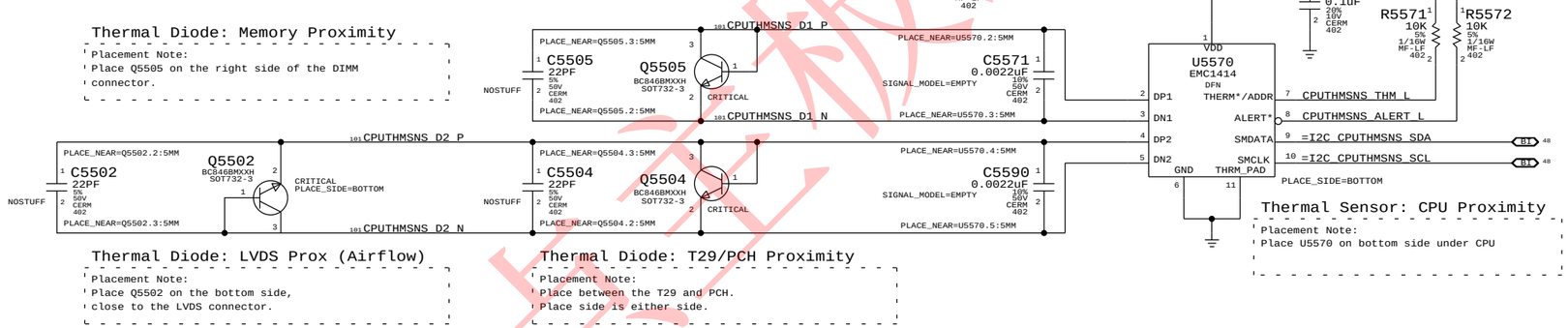
Thermal Sensor A:
GPU Proximity, GPU Die, Left Heat Pipe, Right Fin Stack

I2C Write: 0x98, I2C Read: 0x99

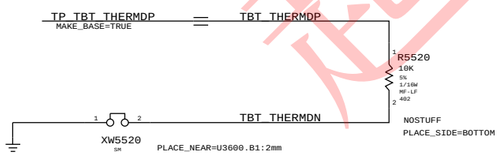


Thermal Sensor B:
CPU Proximity, Memory Proximity, T29/PCH Proximity, LVDS Proximity (Airflow)

I2C Write: 0x98, I2C Read: 0x99



Thermal Sensor: T29 Die



Note: Use GND pin B1 on U3600 for N leg.

SYNC_MASTER=J31_YONAS SYNC_DATE=09/08/2011

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

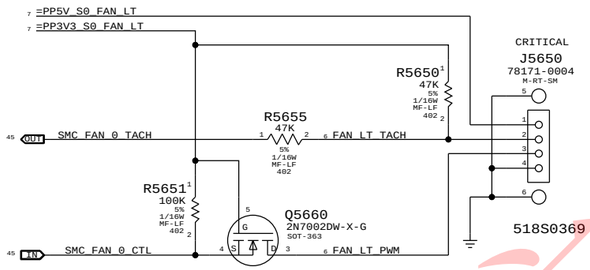
REVISION: 3.0.0

BRANCH:

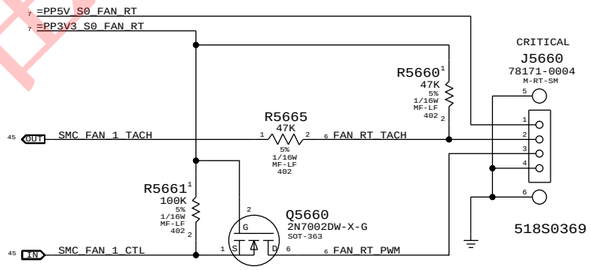
PAGE: 55 OF 132

SHEET: 51 OF 105

Left Fan



Right Fan



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

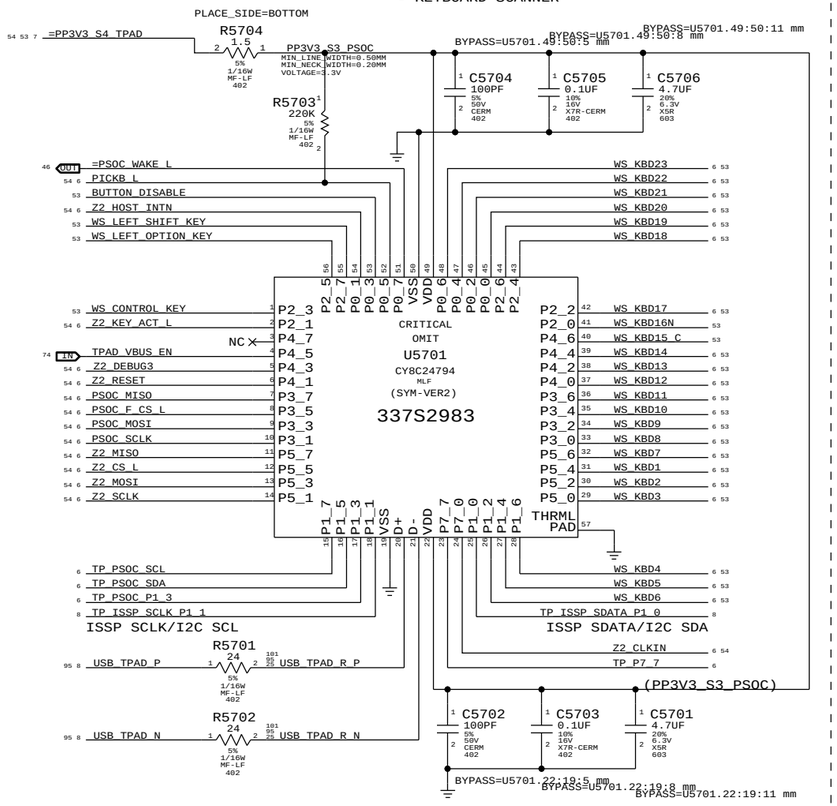
BRANCH:

PAGE: 56 OF 132

SHEET: 52 OF 105

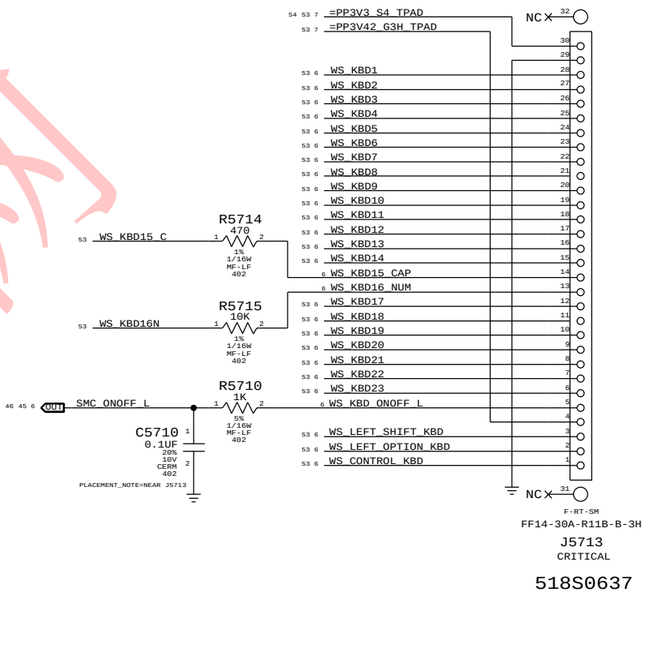
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA 80UA	2.55 KOHM	0.0255 V 0.204 V	0.255E-6 W 16.32E-6 W
3V3 LDO	VDD VOUT	60MA (MAX) 60MA (MAX)	10 OHM 0.2 OHM	0.6 V 0.012 V	36E-3 W 0.72E-3 W
PSOC	VDD	8MA (TYP) 14MA (MAX)	1.5 OHM	0.012 V 0.021 V	96E-6 W 294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

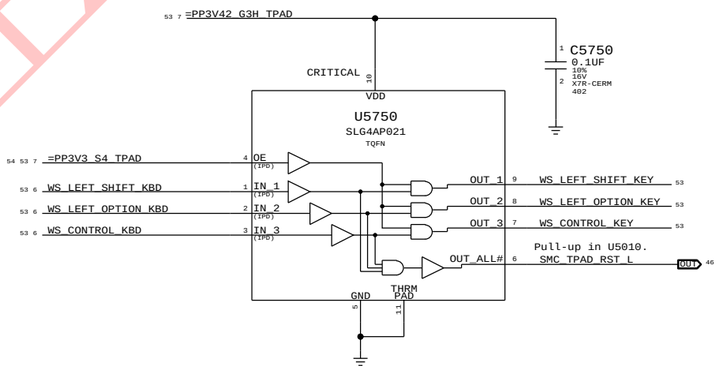
Keyboard Connector



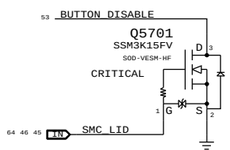
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

Keys ANDed with MSP power to isolate when MSP is not powered. No IPD on OE input pin PP3V3_S4 (symbol error).



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

SYNC_MASTER=J30_MLB SYNC_DATE=06/10/2011

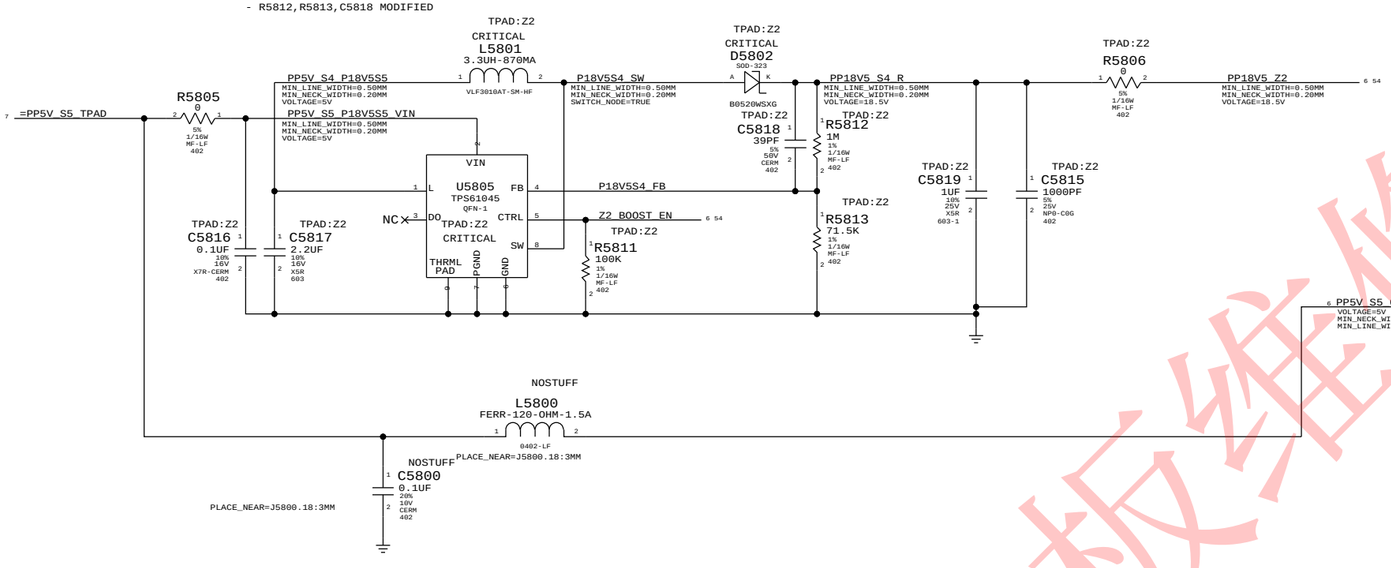
PAGE TITLE: WELLSPRING 1

Apple Inc.

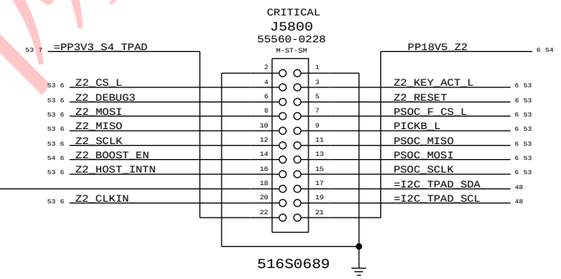
DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 57 OF 132
SHEET: 53 OF 105

BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED

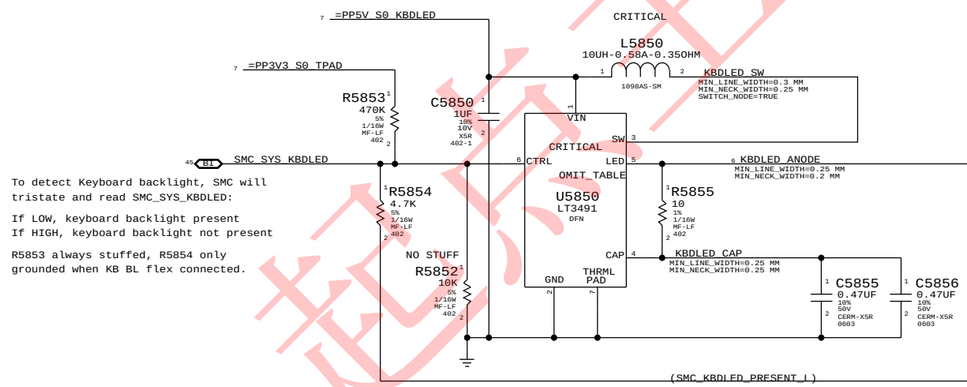


IPD Flex Connector



PIN 21 IS NC ON CUMULUS FLEX
PIN 18 IS NC ON Z2 FLEX

Keyboard Backlight Driver & Detection

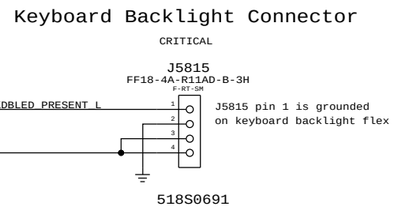


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

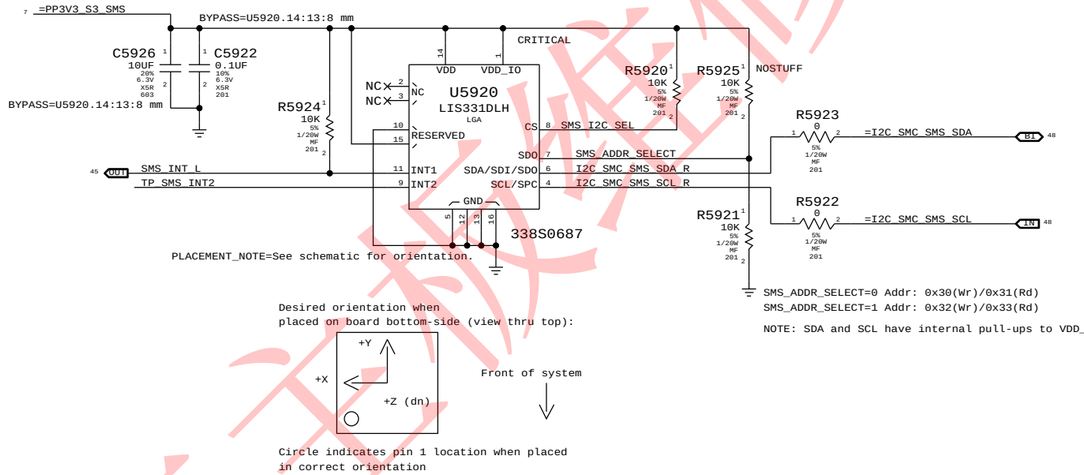
R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3085	1	IC,STLABJ,1-STRING LED DRIVER,2X2DFN-6	U5850	CRITICAL	

起点主板维修网 www.qdzbwx.com



SYNC_MASTER=J31_YONAS SYNC_DATE=08/11/2011

PAGE TITLE: Digital Accelerometer

Apple Inc.

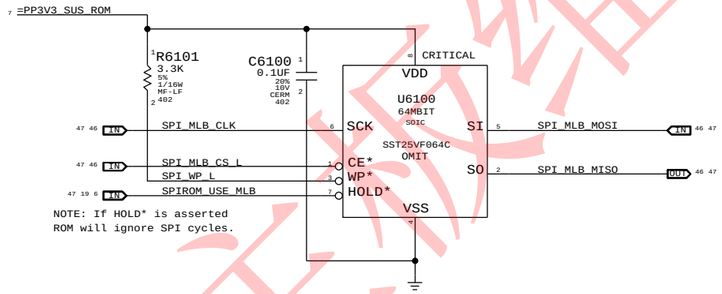
DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH:

PAGE: 59 OF 132

SHEET: 55 OF 105



SYNC_MASTER=K91_BEN SYNC_DATE=06/08/2010

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

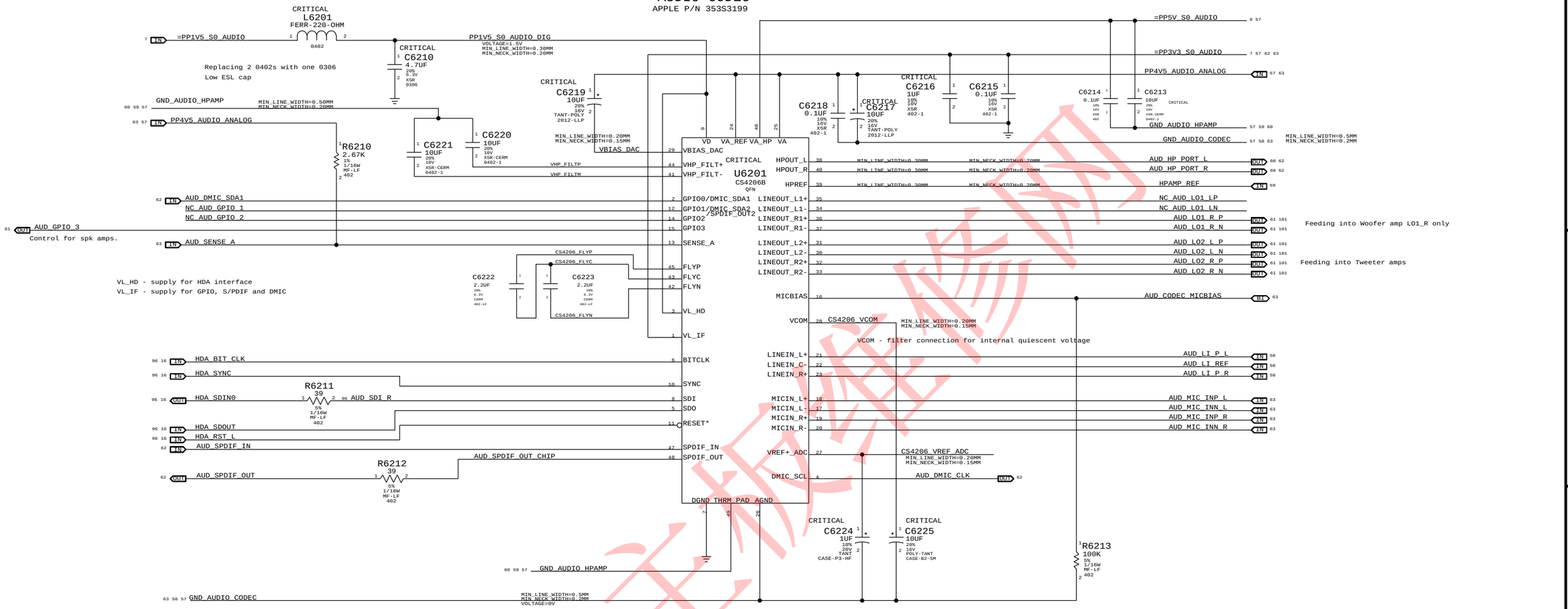
BRANCH

PAGE 61 OF 132

SHEET 56 OF 105

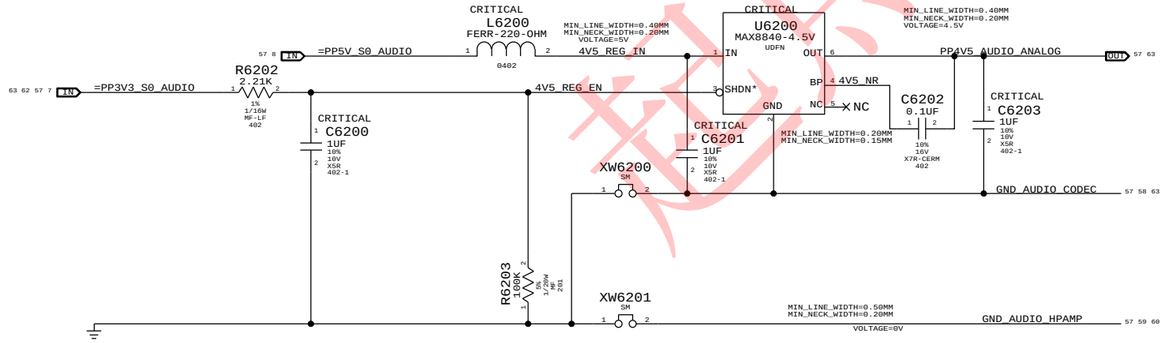
AUDIO CODEC

APPLE P/N 353S3199



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2234



NOTES ON CODEC usage

Hpamp of Codec enabled
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=J31_AUDIO SYNC_DATE=10/26/2011

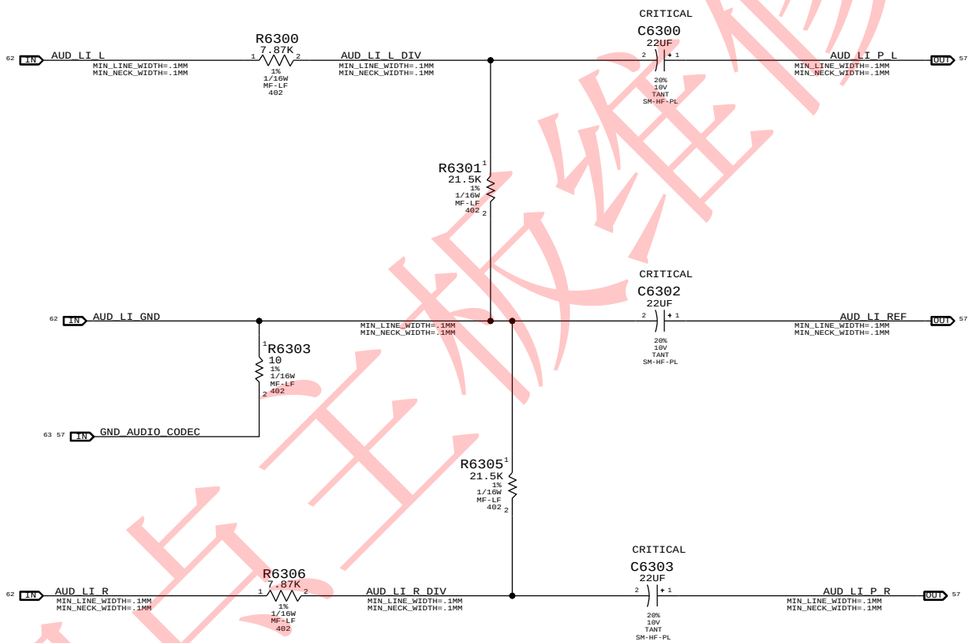
PAGE TITLE: AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 62 OF 132
SHEET 57 OF 105

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 0.36 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



SYNC_MASTER=J31_AUDIO SYNC_DATE=10/26/2011

PAGE TITLE
AUDIO: LINE INPUT FILTER

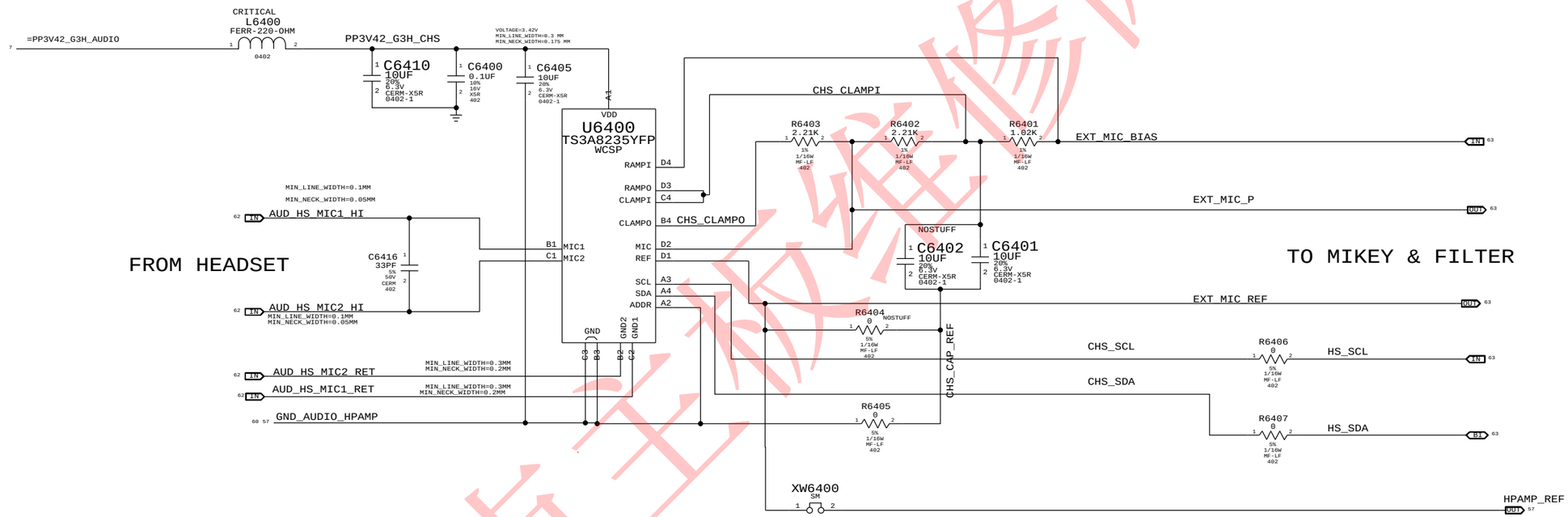
Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 63 OF 132
SHEET 58 OF 105

EXTERNAL (HEADSET) MIC INPUT CIRCUITRY

APN: 353S3066 as of JUly 2011

U6400 should get VDD from battery. Should be powered all the time.



I2C ADDRESSES: CHS uses SMBus 0 connections

CHS	U6400	READ	0111	0111	0x77
CHS	U6400	WRITE	0111	0110	0x76

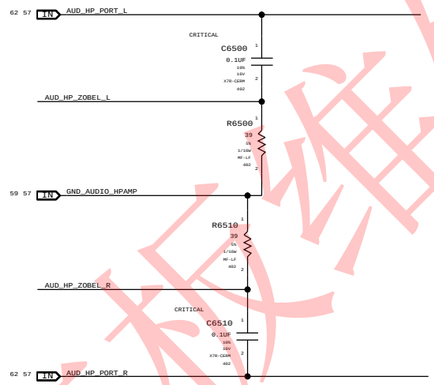
SYNC_MASTER=J31_AUDIO SYNC_DATE=10/26/2011

PAGE TITLE
AUDIO: DETECT/MIC BIAS

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 64 OF 132
SHEET 59 OF 105

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=J31_AUDIO SYNC_DATE=10/26/2011

3X MONO SPEAKER AMPLIFIERS (SSM2375)

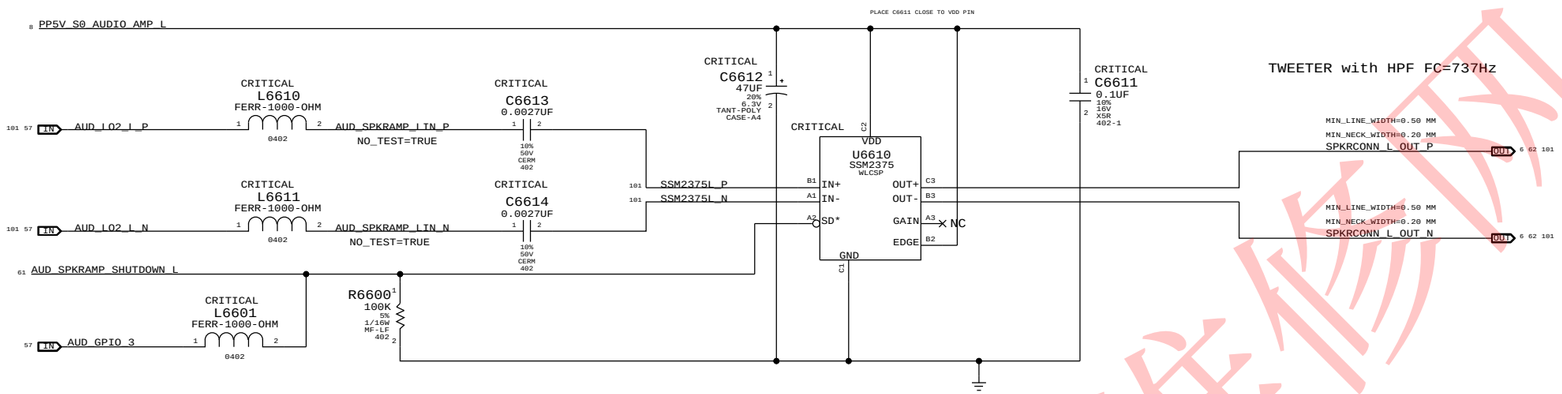
APN: 353S2958 as of July 2011

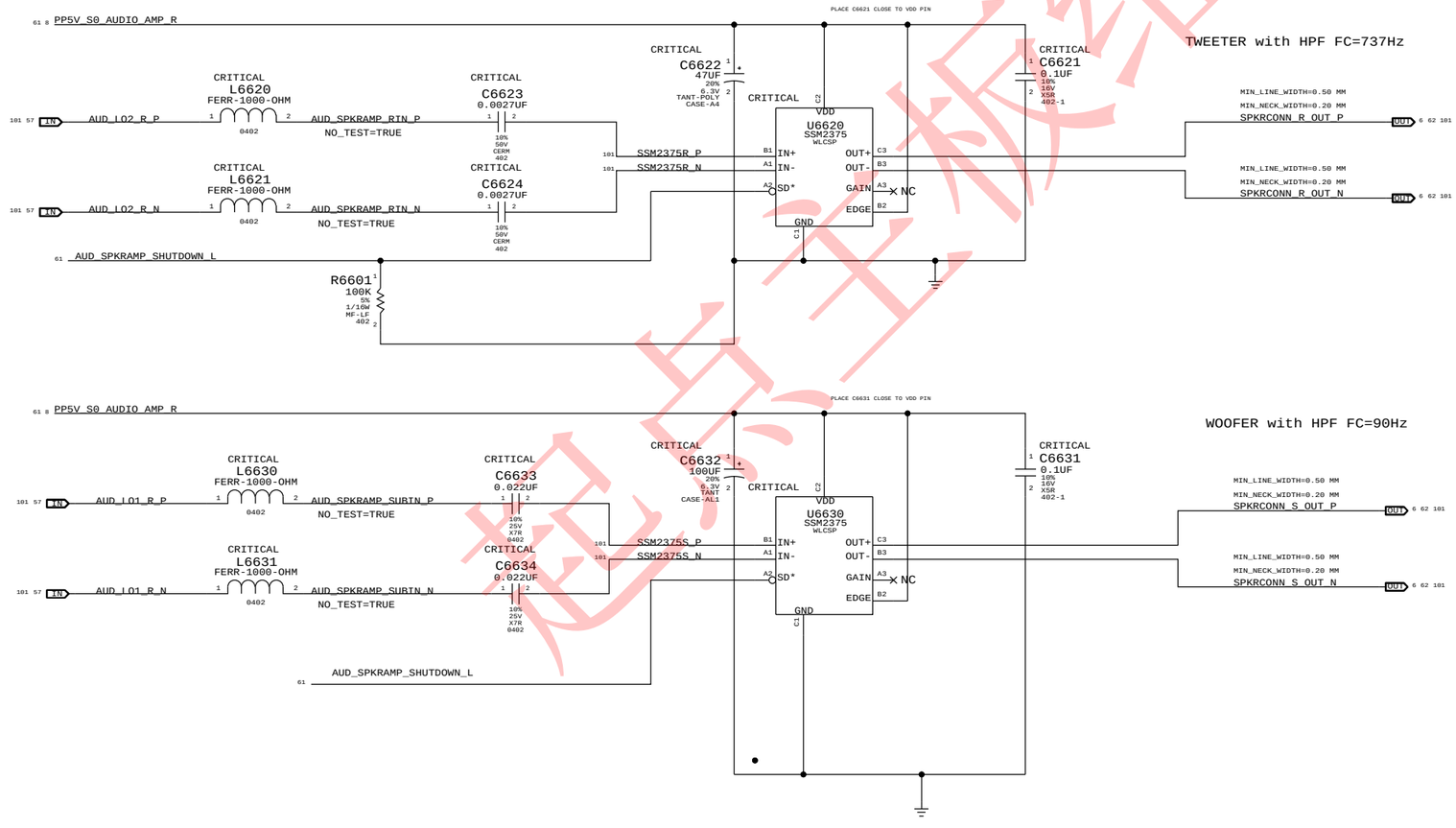
GAIN = +3 DB Rin=80k irrespective of gain

1ST ORDER FC (L&R) = ~737 HZ

1ST ORDER FC (SUB) = ~90 HZ

Gain Pin	Gain dB
Connect to VDD	6
Connect to VDD through 47k	12
Not connected	3
Connect to GND through 47k	9
Connect to GND	0





SYNC_MASTER=J31_AUDIO SYNC_DATE=10/26/2011

PAGE TITLE

AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 66 OF 132

SHEET 61 OF 105

AUDIO JACK 1 LO/HP JACK, SPDIF TX

APN: 514-0671

J6700 SPDIF-TXRX-K24 F-RT-TH

MIC, DETECT, SWITCH, LEFT, RIGHT, GND — AUDIO

A - VIN, B - VCC, C - GND — OPERATING VOLTAGE 3.3 POF

SHELL, SHIELD PINS

C6700 0.1UF 10% 16V X5R 402-1

C6701 2.2UF 20% 6.3V CERM 402-LF

AUD_CONNJ1_TIPDET

AUD_CONNJ1_USMIC

AUD_CONNJ1_USGND_DET

AUD_CONNJ1_LEFT

AUD_CONNJ1_RIGHT

AUD_CONNJ1_USGND

MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM

MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM

Place XW on/near Jack pin

XW6700

L6703 FERR-1000-OHM CRITICAL 0402 — AUD_HS_MIC1_UNFILT → AUD_HS_MIC1_HI

L6707 FERR-120-OHM-2.0A CRITICAL 0402 — AUD_HS_MIC2_RET

L6702 FERR-1000-OHM CRITICAL 0402 — AUD_HS_MIC2_UNFILT → AUD_HS_MIC2_HI

Place XW on/near Jack pin

XW6704

L6708 FERR-120-OHM-2.0A CRITICAL 0402 — AUD_HS_MIC1_RET

L6704 FERR-120-OHM-2.0A CRITICAL 0402 — AUD_HP_PORT_R

L6706 FERR-120-OHM-2.0A CRITICAL 0402 — AUD_HP_PORT_L

R6700 10K 5% 1/16W MF-LF 402

L6705 FERR-1000-OHM CRITICAL 0402 — AUD_J1_TIPDET_R

AUD_J1_SLEEVEDET_R

DZ6703 6.8V-100PF 402

DZ6704 6.8V-100PF 402

DZ6706 6.8V-100PF 402

DZ6701 6.8V-100PF 402

DZ6700 ESDALC5-1BM2 SOD882

C6705 100PF 5% 50V CERM 402

MIN_LINE_WIDTH=0.50 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V

GND_CHASSIS_AUDIO_JACK

XW6701 SM

XW6702 SM

GND PATCH

R6701 0 5% 1/16W MF-LF 402

GND_CHASSIS_AUDIO_JACK

APN: 514-0635

J6750 AUDIO-RCVR-M97 F-RT-TH5

DETECT_FOR_PLUG_TYPE, SWITCH, LEFT, RIGHT, GROUND — AUDIO

A - VDD, B - GND, C - VOUT — OPERATING VOLTAGE 3.3 POF

SHELL, SHIELD PINS

C6750 1UF 10% 10V X5R 402-1

R6749 4.7 5% 1/16W MF-LF 402 — AUD_J2_OPT_OUT → AUD_SPDIF_IN

AUD_CONNJ2_TIPDET

AUD_CONNJ2_RING

AUD_CONNJ2_TIP

AUD_CONNJ2_SLEEVE

MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM

L6754 FERR-1000-OHM CRITICAL 0402 — AUD_LI_R

L6756 FERR-1000-OHM CRITICAL 0402 — AUD_LI_L

L6758 600-OHM-300MA CRITICAL 0402-1 — AUD_LI_GND

L6752 FERR-1000-OHM CRITICAL 0402 — AUD_J2_TIPDET_R

DZ6757 ESDALC5-1BM2 SOD882

DZ6758 ESDALC5-1BM2 SOD882

DZ6756 6.8V-100PF 402

DZ6754 6.8V-100PF 402

C6756 100PF 5% 50V CERM 402

GND_CHASSIS_AUDIO_JACK

AUDIO JACK 2 LINE IN JACK, SPDIF RX

MIC CONNECTOR

J6780 78171-0003 M-RT-SM CRITICAL

BI_MIC_N, BI_MIC_SHIELD, BI_MIC_P

L6783 600-OHM-300MA DIGI_MIC CRITICAL 0402 — AUD_DMIC_CLK → CON_DMIC_CLK

L6784 600-OHM-300MA DIGI_MIC CRITICAL 0402 — AUD_DMIC_SDA1 → CON_DMIC_SDA

L6785 600-OHM-300MA DIGI_MIC CRITICAL 0402 — =PP3V3_S0_AUDIO → CON_DMIC_PWR

J6783 78171-0004 M-RT-SM DIGI_MIC CRITICAL

SPEAKER CONNECTOR APN: 518S0519

J6781 78171-0002 M-RT-SM CRITICAL

SPKRCONN_L_OUT_P, SPKRCONN_L_OUT_N

SPEAKER CONNECTOR APN: 518S0521

J6782 78171-0004 M-RT-SM CRITICAL

SPKRCONN_S_OUT_P, SPKRCONN_S_OUT_N, SPKRCONN_R_OUT_P, SPKRCONN_R_OUT_N

SYNC_MASTER=J31_AUDIO SYNC_DATE=10/26/2011

PAGE TITLE: AUDIO: JACKS

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 67 OF 132

SHEET 62 OF 105

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	NA	0X09 (Jack Detect A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (Jack detect B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (Jack detect C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

I2C addresses: Mikey uses SMBus 0

MIKEY	U6880	READ	0111	0011	0x73
MIKEY	U6880	WRITE	0111	0010	0x72

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ

PORT A DETECT (HEADPHONES)

PORT B DETECT(SPDIF DELEGATE)

PORT B RIGHT(BUILT-IN MIC)

PORT C DETECT (LINE-IN)

Place this next to Charleston

Place this next to the connector

EXTRACTION NOTIFICATION
Voltage level shifting from 5V to 3.3V

APN:376S0975

APN:376S1017

APN:376S0612

CSP MIKEY
APN:353S2640

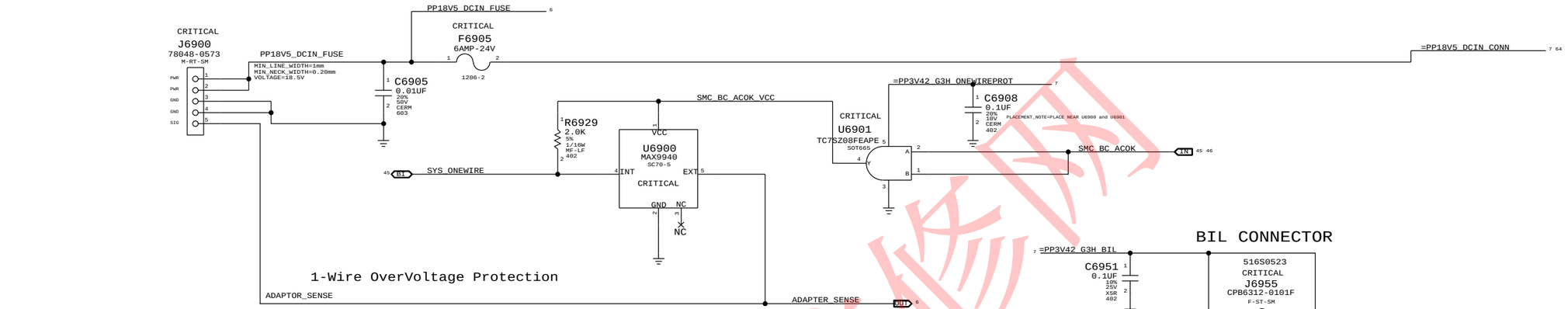
SYNC MASTER=J31_AUDIO
SYNC_DATE=10/26/2011

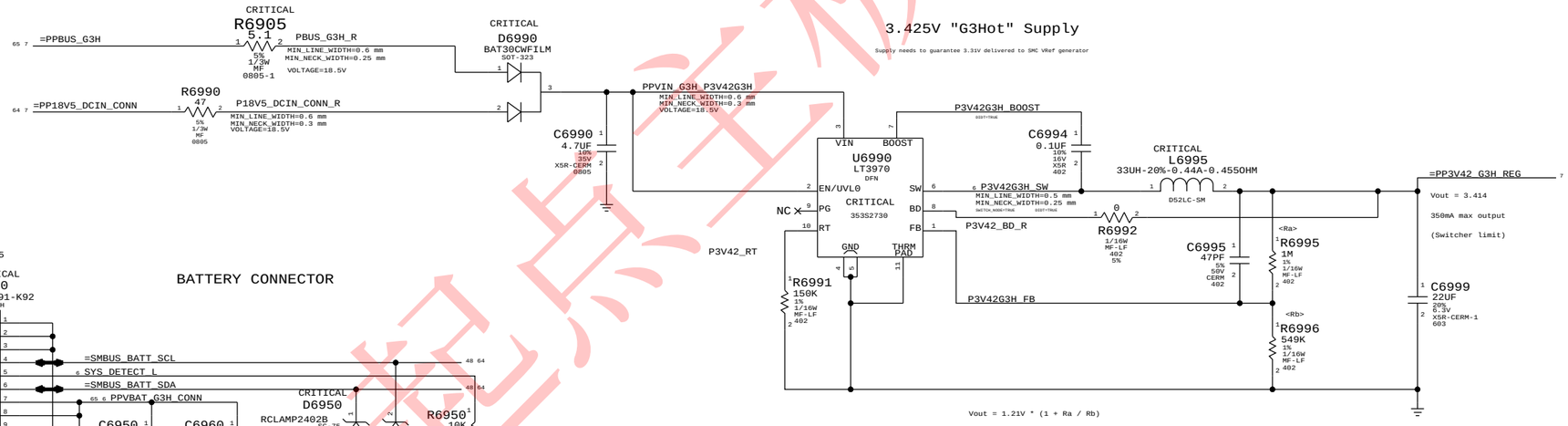
PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

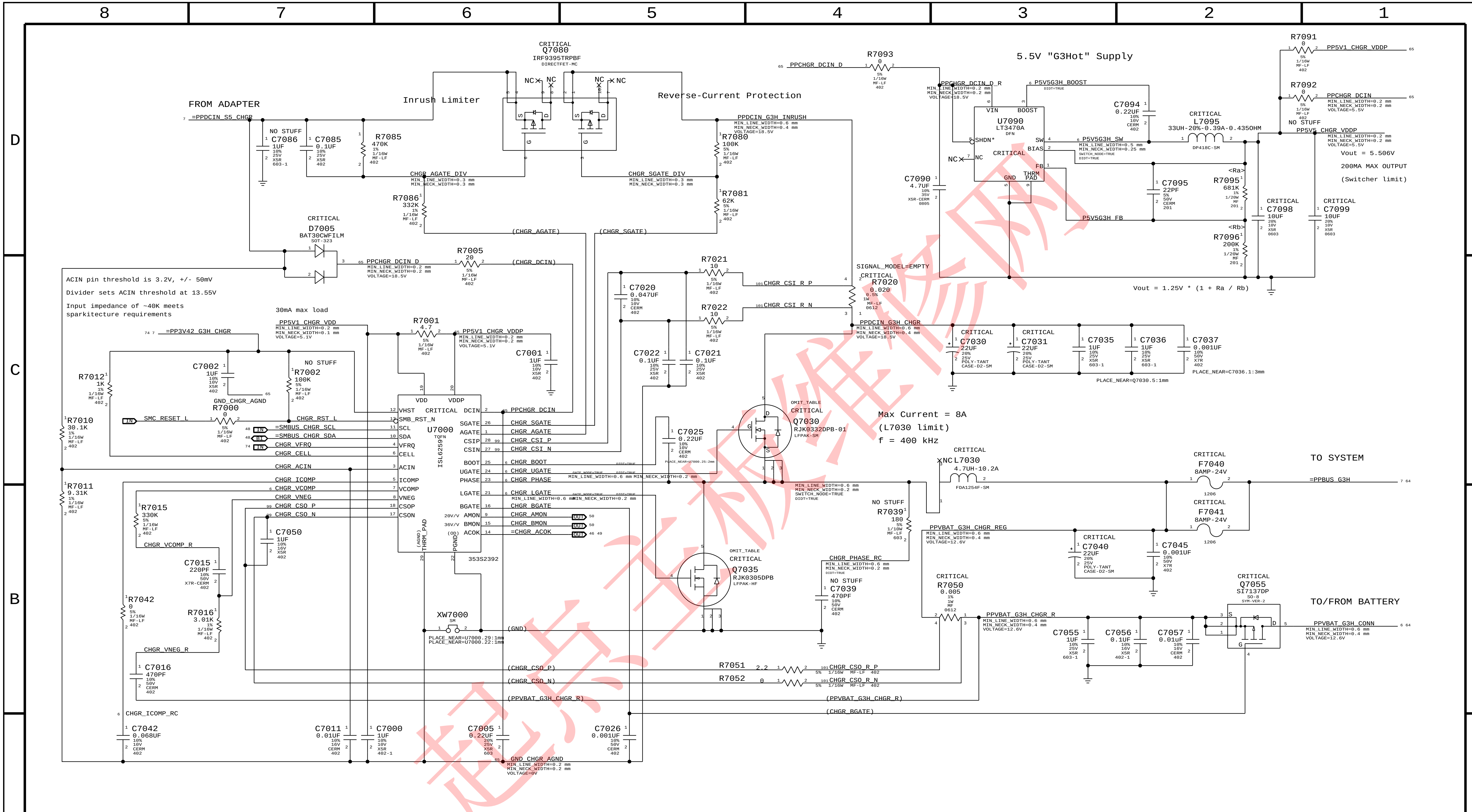
DRAWING NUMBER 051-9585
SIZE D
REVISION 3.0.0
BRANCH
PAGE 68 OF 132
SHEET 63 OF 105

MagSafe DC Power Jack





SYNC_MASTER=J31_JACK	SYNC_DATE=09/02/2011
PAGE TITLE	DC-In & Battery Connectors
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 69 OF 132
	SHEET 64 OF 105



SYNC_MASTER=J31_JACK SYNC_DATE=11/14/2011

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

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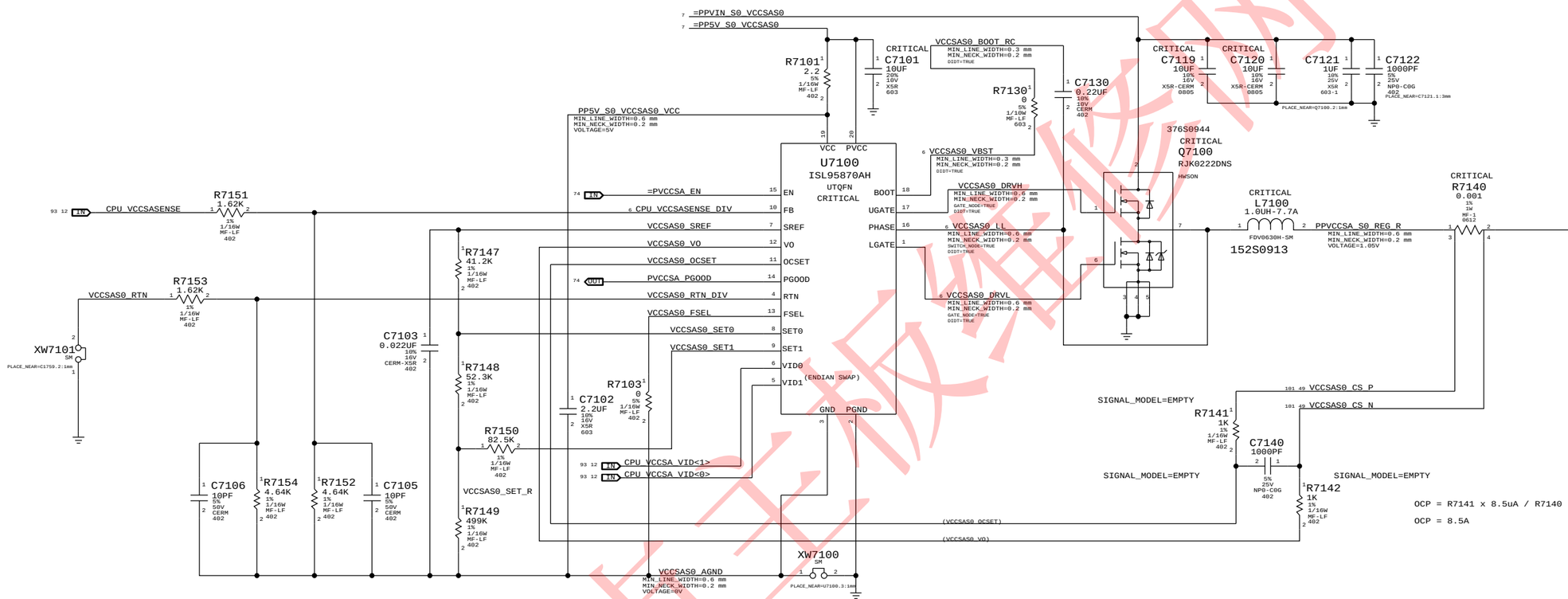


INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC_MASTER=J31_JACK SYNC_DATE=09/14/2011

PAGE TITLE: System Agent Supply

Apple Inc.

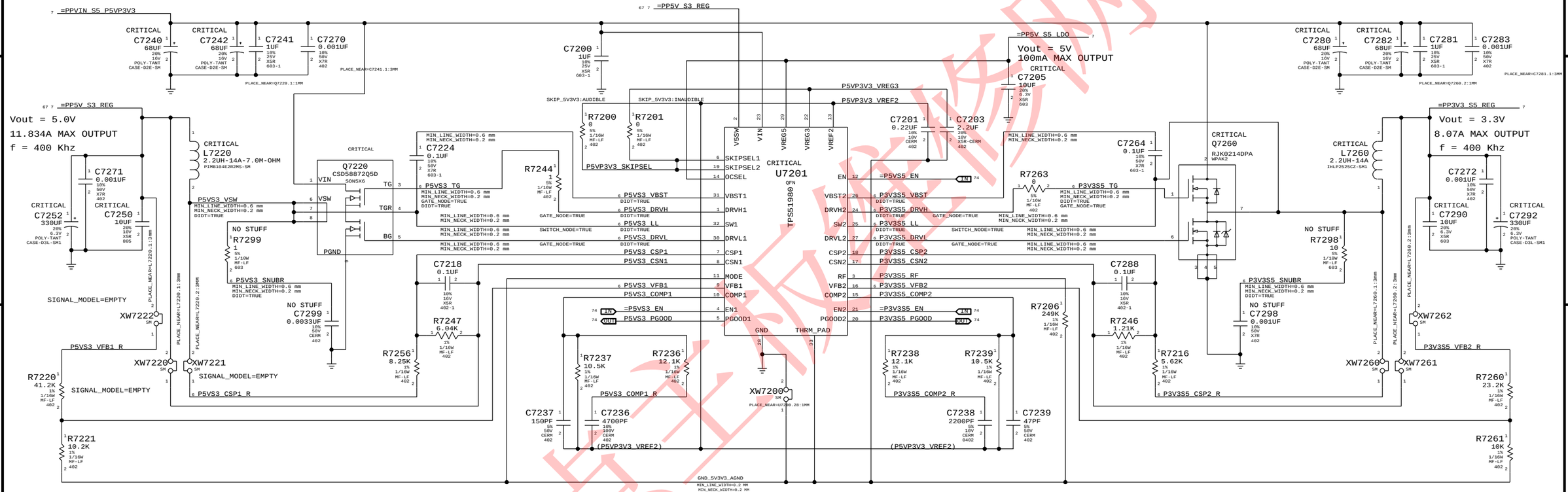
DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

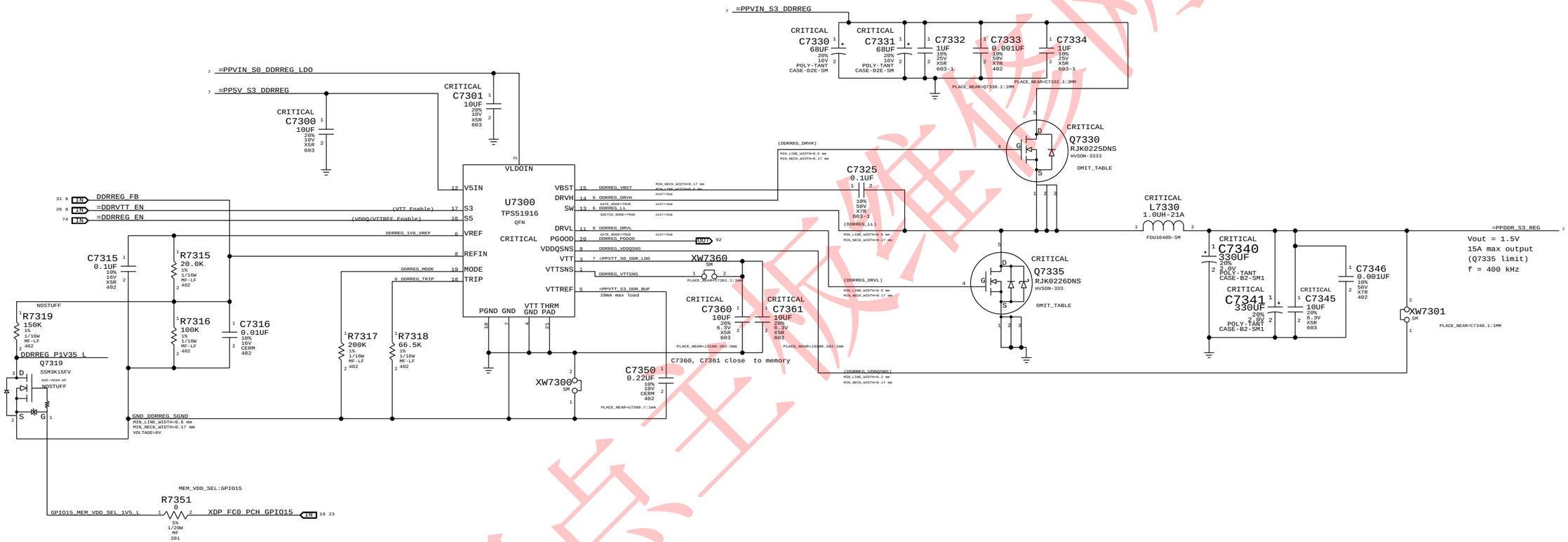
BRANCH:

PAGE: 71 OF 132

SHEET: 66 OF 105



SYNC_MASTER=J31_JACK	SYNC_DATE=11/09/2011
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 72 OF 132
	SHEET 67 OF 105



SYNC_MASTER=J31_JACK SYNC_DATE=07/07/2011

PAGE TITLE

1.5V DDR3 Supply

Apple Inc.

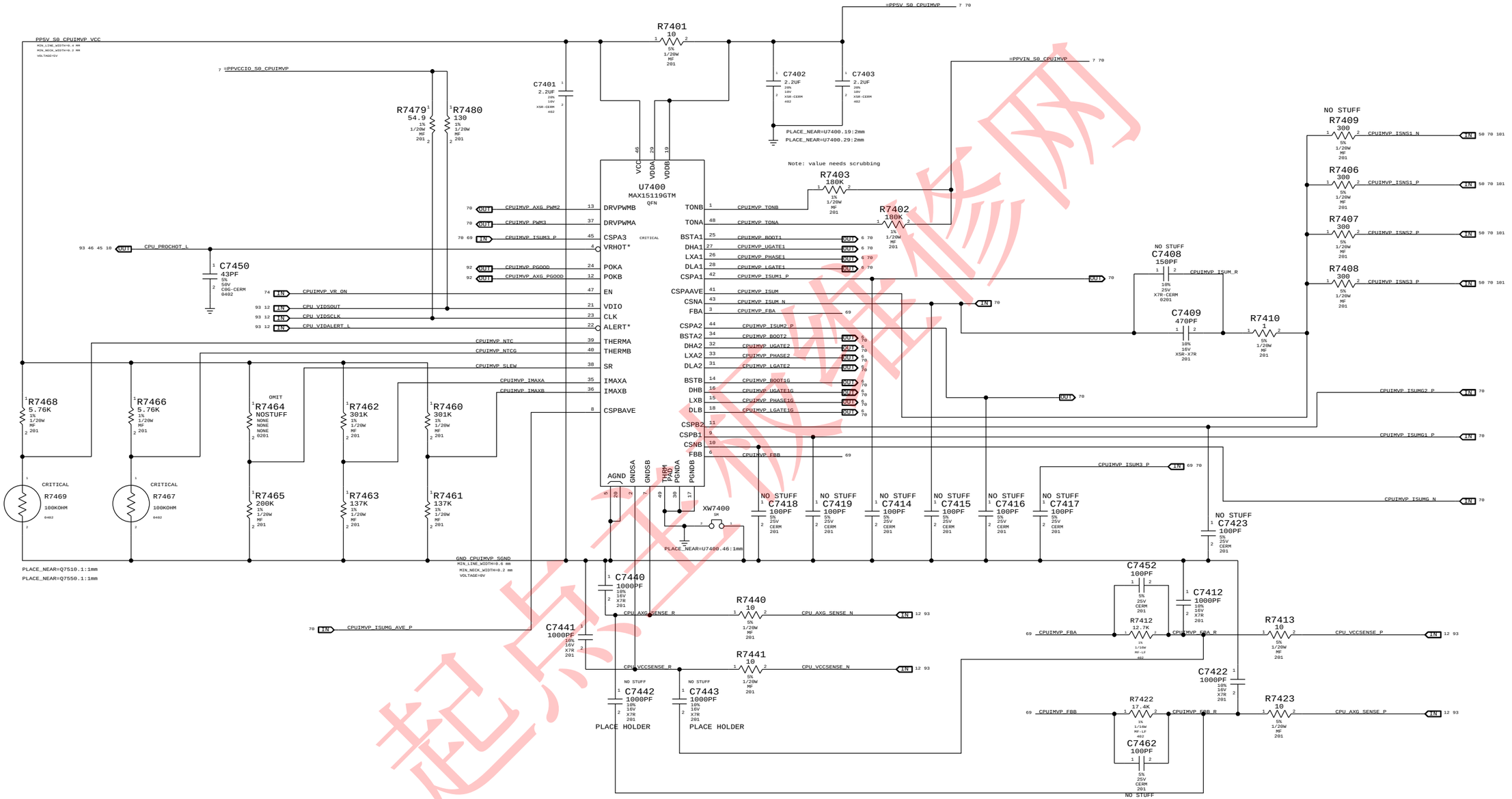
DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 73 OF 132

SHEET 68 OF 105



SYNC_MASTER=J31_JACK	SYNC_DATE=11/11/2013
PAGE TITLE	CPU IMVP7 & AXG VCore Regulator
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 74 OF 132
	SHEET 69 OF 105

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PHASE 1

PHASE 2

PHASE 3

AXG PHASE 1

AXG PHASE 2

Additonal Input Bulk Caps

CPU IMVP7 & AXG VCore Output

Apple Inc.

SYNC_MASTER=J31_JACK SYNC_DATE=11/11/2013

PAGE TITLE

DRAWING NUMBER 051-9585 SIZE D

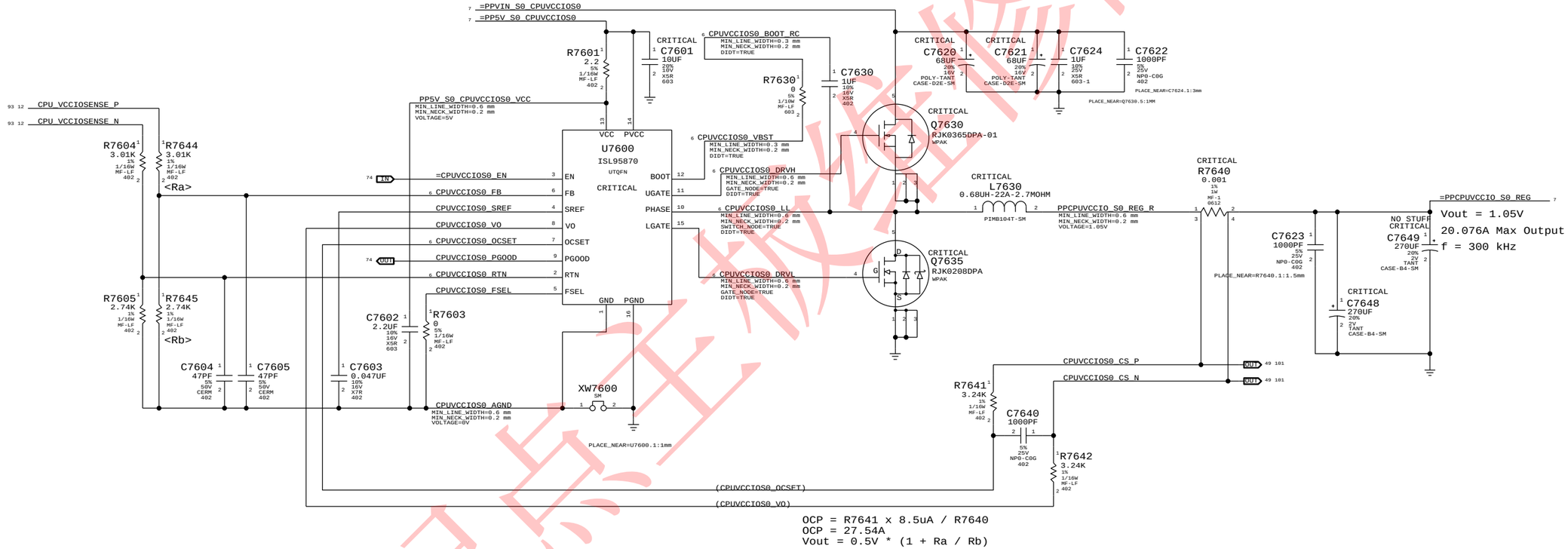
REVISION 3.0.0

BRANCH

PAGE 75 OF 132

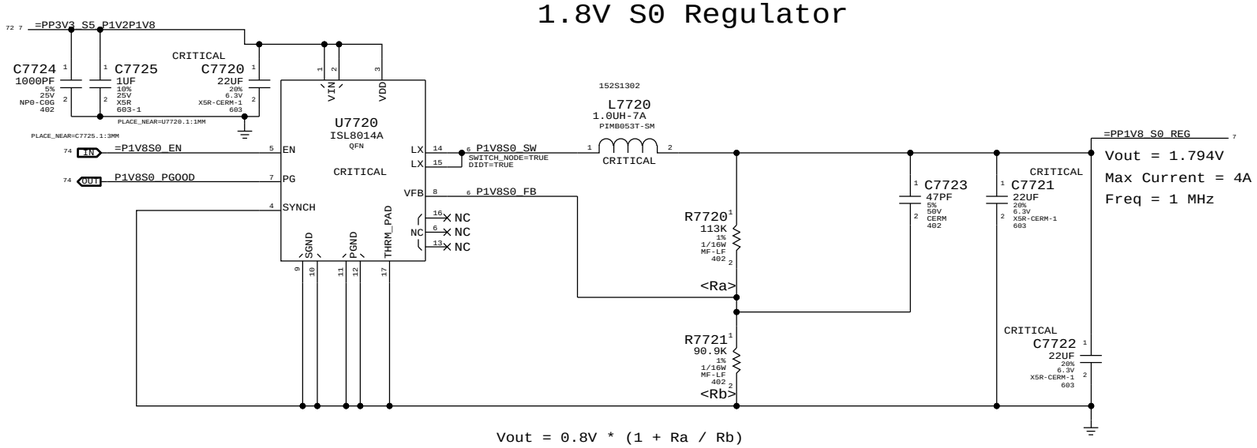
SHEET 70 OF 105

CPU VCCIO REGULATOR



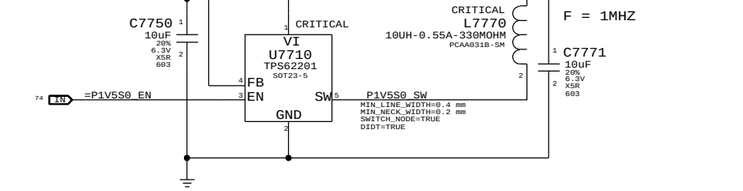
SYNC_MASTER=J31_JACK	SYNC_DATE=09/19/2011
PAGE TITLE	CPU VCCIO (1V0R1V05 S0) POWER SUPPLY
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 76 OF 132
	SHEET 71 OF 105

1.8V S0 Regulator

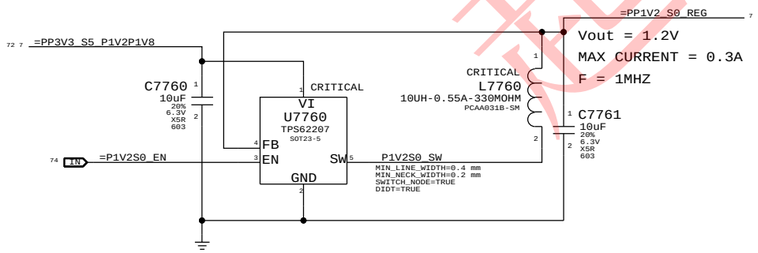


Vout = 0.8V * (1 + Ra / Rb)

1.5V S0 Regulator

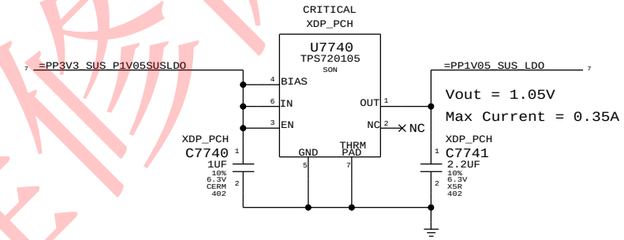


1.2V S0 (GMUX) Regulator

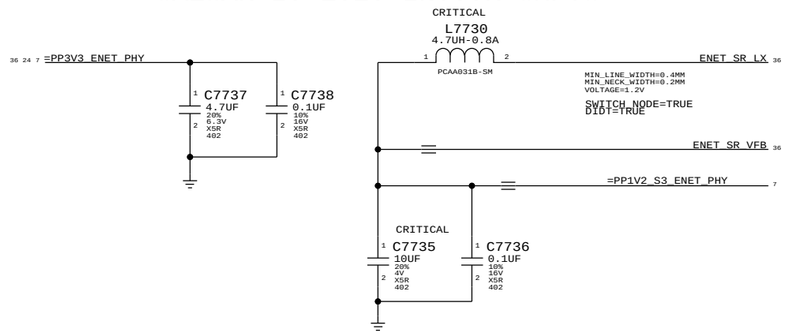


1.05V SUS LDO

Cougar Point-M requires JTAG pull-ups to be powered at 1.05V in Sus.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.



CAESAR IV 1.2V INT.VR CMPTS



SYNC_MASTER=J31_JACK SYNC_DATE=06/10/2011

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

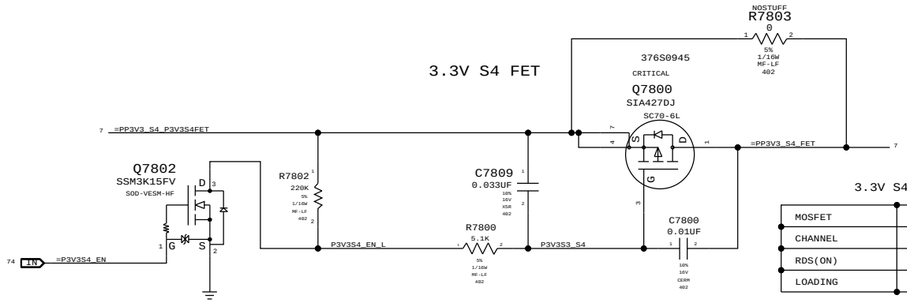
REVISION: 3.0.0

BRANCH:

PAGE: 77 OF 132

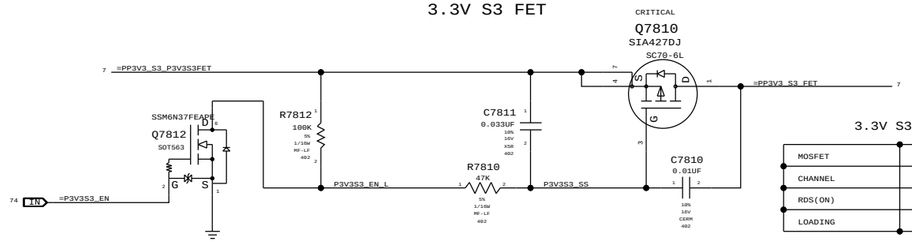
SHEET: 72 OF 105

3.3V S4 FET



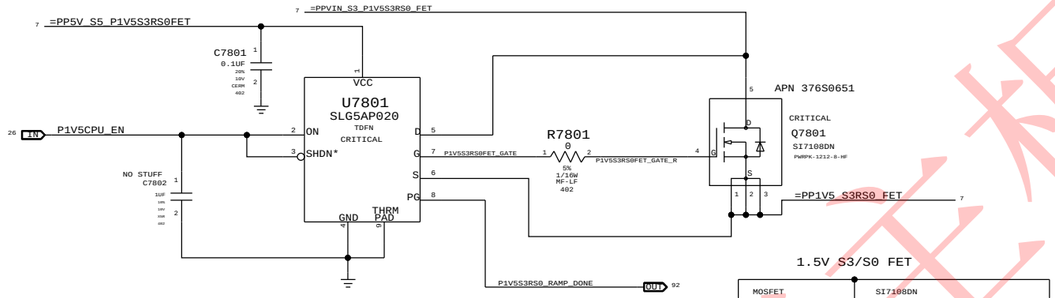
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET



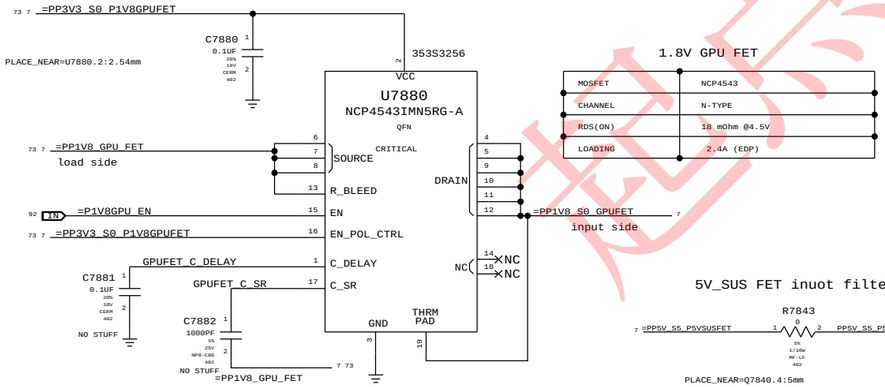
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET



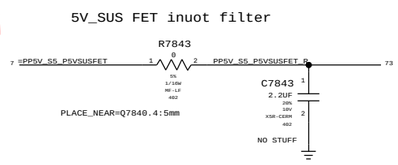
1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

1.8V GPU FET



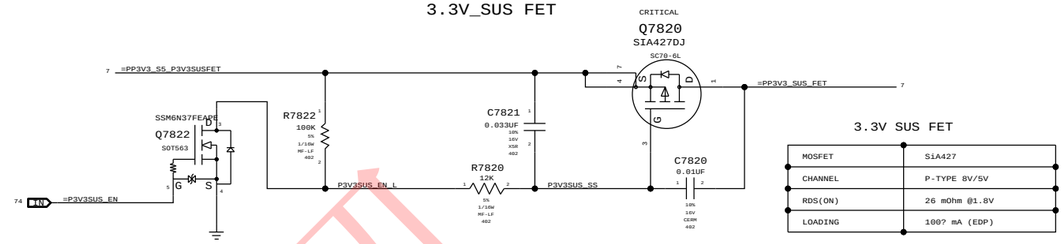
1.8V GPU FET	
MOSFET	NCP4543
CHANNEL	N-TYPE
RDS(ON)	18 mOhm @4.5V
LOADING	2.4A (EDP)

5V_SUS FET inuot filter



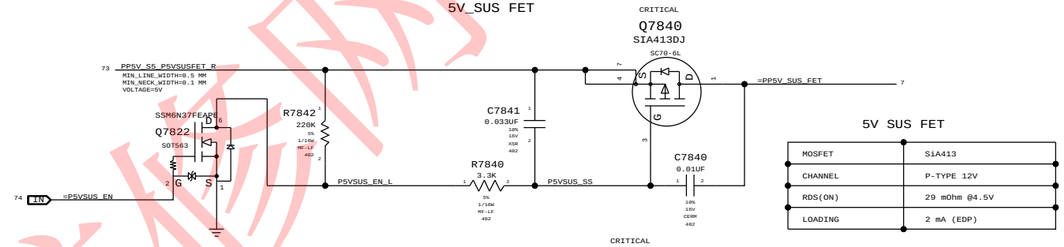
U7880 default Turn on delay EN--> on is 200~650us.

3.3V_SUS FET



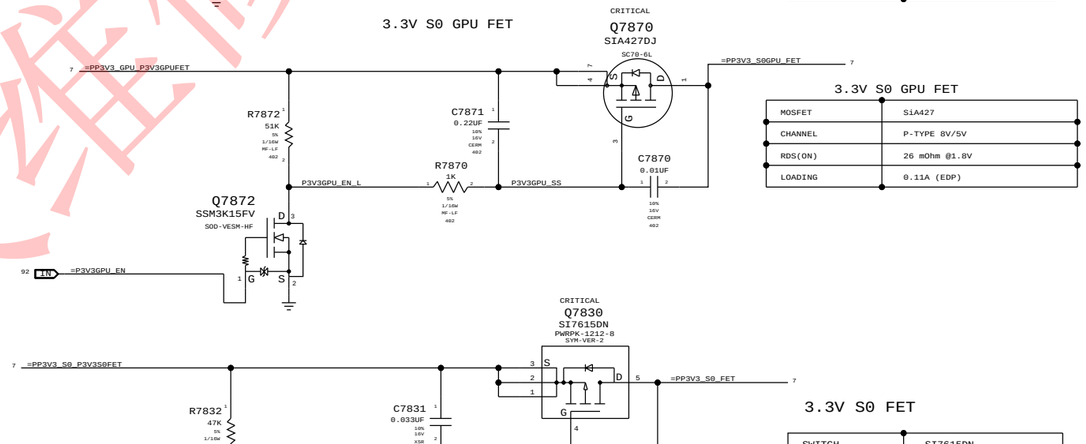
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



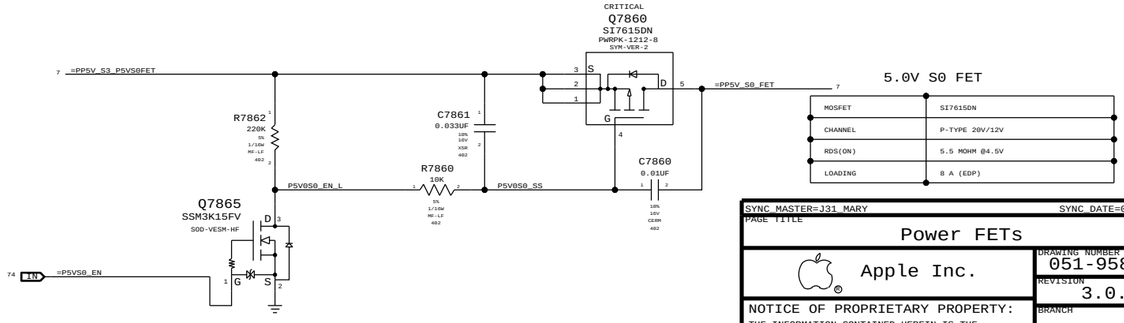
5V SUS FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

3.3V S0 GPU FET



3.3V S0 GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

3.3V S0 FET	
SWITCH	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	8 A (EDP)

SYNC MASTER=J31_MARY SYNC_DATE=05/05/2011

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

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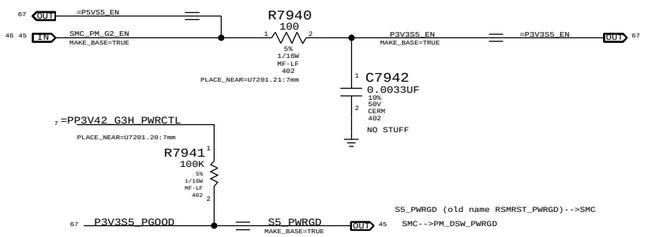
PAGE 78 OF 132

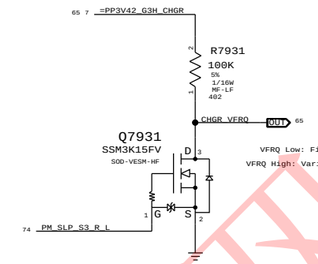
SHEET 73 OF 105

S5 Rail Enables & PGOOD

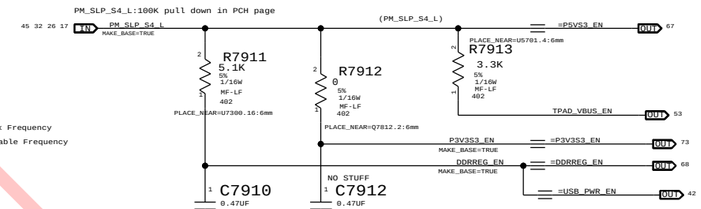


State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

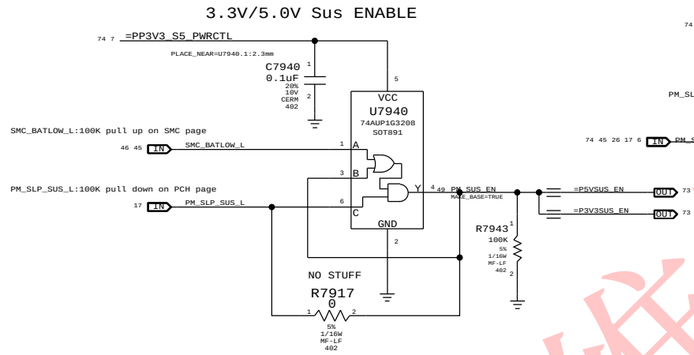
CHGR VFRQ Generation



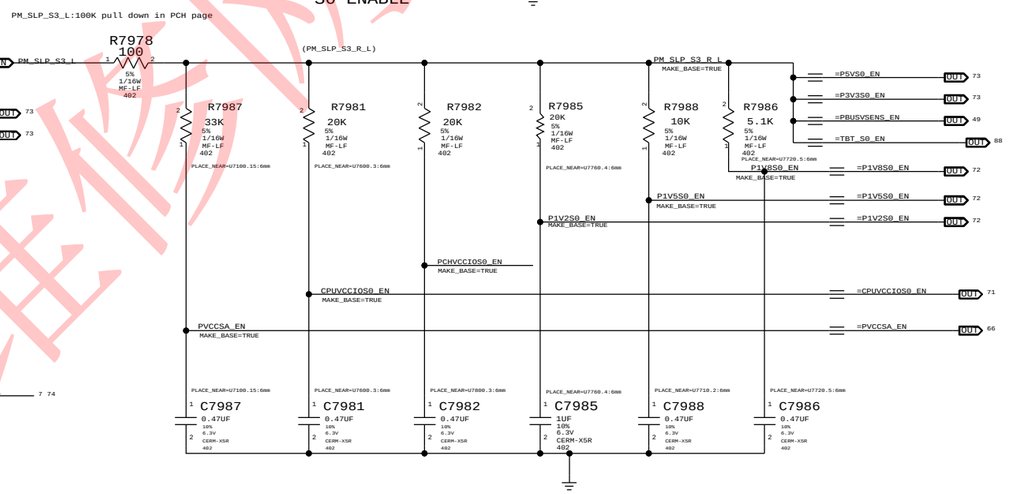
3.3V,5V S3 ENABLE



3.3V/5.0V Sus ENABLE

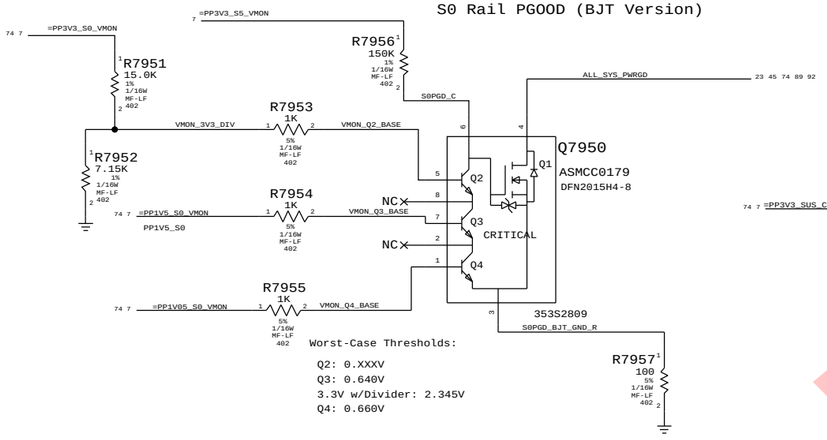


S0 ENABLE

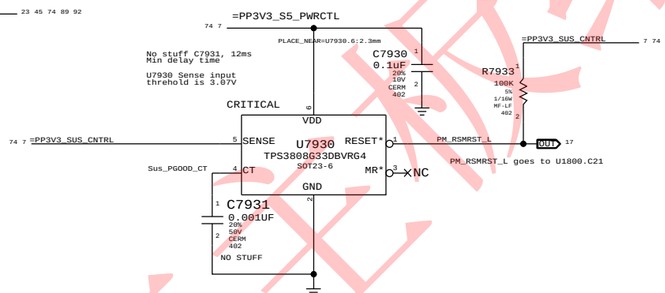


CPUVCORE ENABLE

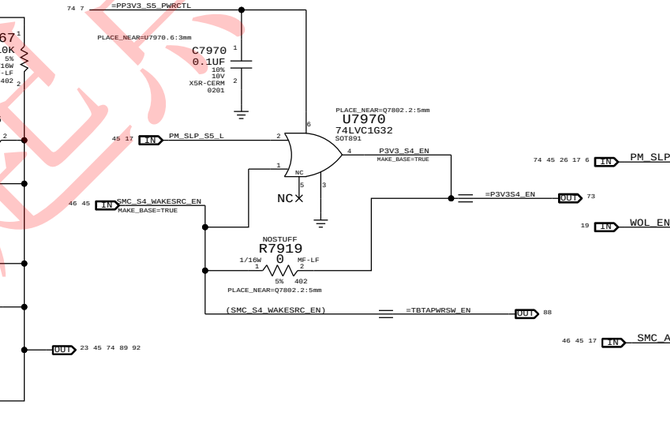
S0 Rail PGOOD (BJT Version)



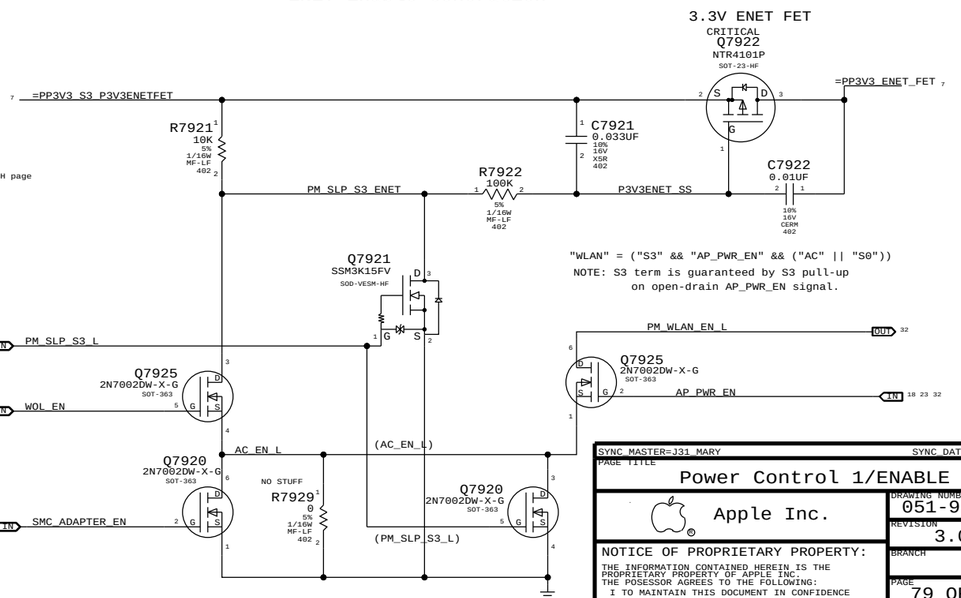
3.3V SUS Detect



3.3V/5.0V S4 ENABLE



ENET Enable Generation



SYNC_MASTER=J31_MARY	SYNC_DATE=06/06/2013
PAGE TITLE	Power Control 1/ENABLE
Apple Inc.	DRAWING NUMBER 051-9585
	SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 79 OF 132
	SHEET 74 OF 105

Page Notes

Power aliases required by this page:
- +PP3V3_GPU_VDD33

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

93 8	IN	PEG_R2D_C_P<0>	C8020	0.22UF	PEG_R2D_P<0>	6 75 92 93
93 8	IN	PEG_R2D_C_N<0>	C8021	0.22UF	PEG_R2D_N<0>	6 75 92 93
93 8	IN	PEG_R2D_C_P<1>	C8022	0.22UF	PEG_R2D_P<1>	6 75 93
93 8	IN	PEG_R2D_C_N<1>	C8023	0.22UF	PEG_R2D_N<1>	6 75 93
93 8	IN	PEG_R2D_C_P<2>	C8024	0.22UF	PEG_R2D_P<2>	6 75 93
93 8	IN	PEG_R2D_C_N<2>	C8025	0.22UF	PEG_R2D_N<2>	6 75 93
93 8	IN	PEG_R2D_C_P<3>	C8026	0.22UF	PEG_R2D_P<3>	6 75 92 93
93 8	IN	PEG_R2D_C_N<3>	C8027	0.22UF	PEG_R2D_N<3>	6 75 92 93
93 8	IN	PEG_R2D_C_P<4>	C8028	0.22UF	PEG_R2D_P<4>	6 75 93
93 8	IN	PEG_R2D_C_N<4>	C8029	0.22UF	PEG_R2D_N<4>	6 75 93
93 8	IN	PEG_R2D_C_P<5>	C8030	0.22UF	PEG_R2D_P<5>	6 75 92 93
93 8	IN	PEG_R2D_C_N<5>	C8031	0.22UF	PEG_R2D_N<5>	6 75 92 93
93 8	IN	PEG_R2D_C_P<6>	C8032	0.22UF	PEG_R2D_P<6>	6 75 93
93 8	IN	PEG_R2D_C_N<6>	C8033	0.22UF	PEG_R2D_N<6>	6 75 93
93 8	IN	PEG_R2D_C_P<7>	C8034	0.22UF	PEG_R2D_P<7>	6 75 92 93
93 8	IN	PEG_R2D_C_N<7>	C8035	0.22UF	PEG_R2D_N<7>	6 75 92 93

Note: Removed GND voids from AC caps for layout (J31).

93 75 6		PEG_D2R_C_P<0>	C8055	0.22UF	PEG_D2R_P<0>	OUT 8 93
93 75 6		PEG_D2R_C_N<0>	C8056	0.22UF	PEG_D2R_N<0>	OUT 8 93
93 75 6		PEG_D2R_C_P<1>	C8057	0.22UF	PEG_D2R_P<1>	OUT 8 93
93 75 6		PEG_D2R_C_N<1>	C8058	0.22UF	PEG_D2R_N<1>	OUT 8 93
93 75 6		PEG_D2R_C_P<2>	C8059	0.22UF	PEG_D2R_P<2>	OUT 8 93
93 75 6		PEG_D2R_C_N<2>	C8060	0.22UF	PEG_D2R_N<2>	OUT 8 93
93 75 6		PEG_D2R_C_P<3>	C8061	0.22UF	PEG_D2R_P<3>	OUT 8 93
93 75 6		PEG_D2R_C_N<3>	C8062	0.22UF	PEG_D2R_N<3>	OUT 8 93
93 75 6		PEG_D2R_C_P<4>	C8063	0.22UF	PEG_D2R_P<4>	OUT 8 93
93 75 6		PEG_D2R_C_N<4>	C8064	0.22UF	PEG_D2R_N<4>	OUT 8 93
93 75 6		PEG_D2R_C_P<5>	C8065	0.22UF	PEG_D2R_P<5>	OUT 8 93
93 75 6		PEG_D2R_C_N<5>	C8066	0.22UF	PEG_D2R_N<5>	OUT 8 93
93 75 6		PEG_D2R_C_P<6>	C8067	0.22UF	PEG_D2R_P<6>	OUT 8 93
93 75 6		PEG_D2R_C_N<6>	C8068	0.22UF	PEG_D2R_N<6>	OUT 8 93
93 75 6		PEG_D2R_C_P<7>	C8069	0.22UF	PEG_D2R_P<7>	OUT 8 93
93 75 6		PEG_D2R_C_N<7>	C8070	0.22UF	PEG_D2R_N<7>	OUT 8 93

OMIT_TABLE

U8000
NV-GK107
BGA
(1 OF 10)

93 92 75 6	PEG_R2D_P<0>	AN12	PEX_RX0	PEX_TX0	AK14	PEG_D2R_C_P<0>	6 75 93
93 92 75 6	PEG_R2D_N<0>	AM12	PEX_RX0*	PEX_TX0*	AJ14	PEG_D2R_C_N<0>	6 75 93
93 75 6	PEG_R2D_P<1>	AN14	PEX_RX1	PEX_TX1	AH14	PEG_D2R_C_P<1>	6 75 93
93 75 6	PEG_R2D_N<1>	AM14	PEX_RX1*	PEX_TX1*	AG14	PEG_D2R_C_N<1>	6 75 93
93 92 75 6	PEG_R2D_P<2>	AP14	PEX_RX2	PEX_TX2	AK15	PEG_D2R_C_P<2>	6 75 93
93 92 75 6	PEG_R2D_N<2>	AP15	PEX_RX2*	PEX_TX2*	AJ15	PEG_D2R_C_N<2>	6 75 93
93 92 75 6	PEG_R2D_P<3>	AN15	PEX_RX3	PEX_TX3	AL16	PEG_D2R_C_P<3>	6 75 93
93 92 75 6	PEG_R2D_N<3>	AM15	PEX_RX3*	PEX_TX3*	AK16	PEG_D2R_C_N<3>	6 75 93
93 75 6	PEG_R2D_P<4>	AN17	PEX_RX4	PEX_TX4	AK17	PEG_D2R_C_P<4>	6 75 93
93 75 6	PEG_R2D_N<4>	AM17	PEX_RX4*	PEX_TX4*	AJ17	PEG_D2R_C_N<4>	6 75 93
93 92 75 6	PEG_R2D_P<5>	AP17	PEX_RX5	PEX_TX5	AH17	PEG_D2R_C_P<5>	6 75 93
93 92 75 6	PEG_R2D_N<5>	AP18	PEX_RX5*	PEX_TX5*	AG17	PEG_D2R_C_N<5>	6 75 93
93 75 6	PEG_R2D_P<6>	AN18	PEX_RX6	PEX_TX6	AK18	PEG_D2R_C_P<6>	6 75 93
93 75 6	PEG_R2D_N<6>	AM18	PEX_RX6*	PEX_TX6*	AJ18	PEG_D2R_C_N<6>	6 75 93
93 92 75 6	PEG_R2D_P<7>	AN20	PEX_RX7	PEX_TX7	AL19	PEG_D2R_C_P<7>	6 75 93
93 92 75 6	PEG_R2D_N<7>	AM20	PEX_RX7*	PEX_TX7*	AK19	PEG_D2R_C_N<7>	6 75 93
NC		AP20	PEX_RX8	PEX_TX8	AK20	NC	
NC		AP21	PEX_RX8*	PEX_TX8*	AJ20	NC	
NC		AN21	PEX_RX9	PEX_TX9	AH20	NC	
NC		AM21	PEX_RX9*	PEX_TX9*	AG20	NC	
NC		AN23	PEX_RX10	PEX_TX10	AK21	NC	
NC		AM23	PEX_RX10*	PEX_TX10*	AJ21	NC	
NC		AP23	PEX_RX11	PEX_TX11	AL22	NC	
NC		AP24	PEX_RX11*	PEX_TX11*	AK22	NC	
NC		AN24	PEX_RX12	PEX_TX12	AK23	NC	
NC		AM24	PEX_RX12*	PEX_TX12*	AJ23	NC	
NC		AN26	PEX_RX13	PEX_TX13	AH23	NC	
NC		AM26	PEX_RX13*	PEX_TX13*	AG23	NC	
NC		AP26	PEX_RX14	PEX_TX14	AK24	NC	
NC		AP27	PEX_RX14*	PEX_TX14*	AJ24	NC	
NC		AN27	PEX_RX15	PEX_TX15	AL25	NC	
NC		AM27	PEX_RX15*	PEX_TX15*	AK25	NC	
96 16	IN PEG_CLK100M_P	AL13	PEX_REFCLK	PEX_TSTCLK_OUT	AJ26	96 PEX_TSTCLK_O_P	
96 16	IN PEG_CLK100M_N	AK13	PEX_REFCLK*	PEX_TSTCLK_OUT*	AK26	96 PEX_TSTCLK_O_N	
82 8	IN GPU_RESET_L	AJ12	PEX_RST*	PEX_TERMP	AP29	GPU_PEX_TERMP	
82 75	OUT PEX_CLKREQ_L_R	AK12	PEX_CLKREQ*	PEX_SVDD_3V3	AG12	PP3V3_GPU_PEX_PLL_HVDD 83	
NC		AJ11	PEX_WAKE*				

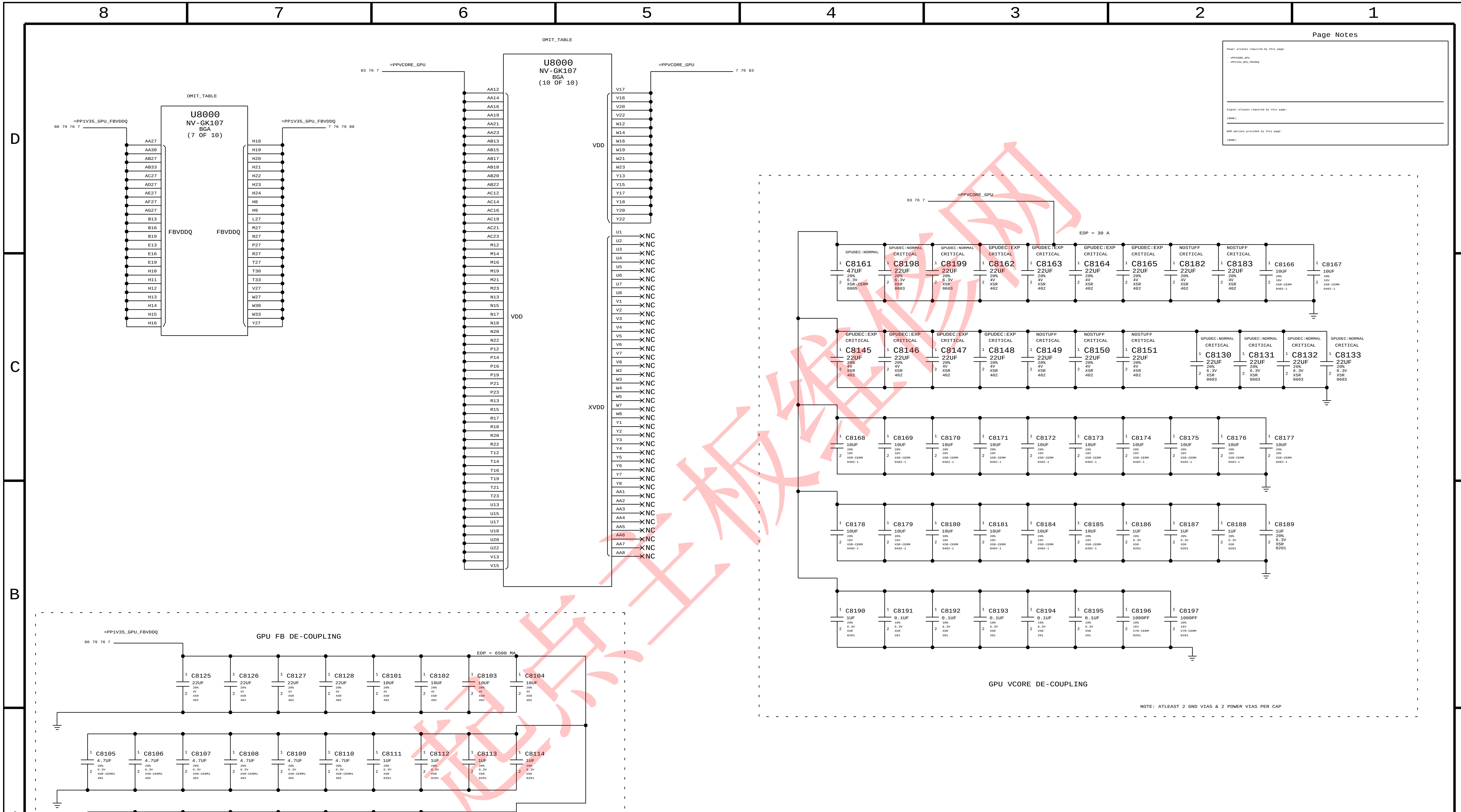
R8000 0 MF 5% 1/20W 201 (GPU_RESET_L – GPU_RESET_R_L)

=PP3V3_GPU_VDD33 (83 82 81 7) — R8001 10K 1% 1/20W MF 201 — PEX_CLKREQ_L_R (82 75)

NOSTUFF R8002 200 1% 1/20W MF 201

R8005 2.49K 1% 1/20W MF 201

SYNC_MASTER=J31_SREE	SYNC_DATE=10/25/2013
PAGE TITLE	KEPLER PCI-E
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 80 OF 132
	SHEET 75 OF 105



SYNC_MASTER=D2_MLB_2P SYNC_DATE=01/18/2012

PAGE TITLE

KEPLER CORE/FB POWER

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 81 OF 132

SHEET 76 OF 105

NOTE:GDDR5 MODE H MAPPING

OMIT_TABLE

U8000
NV-GK107
BGA
(3 OF 10)
MEM INTERFACE A

FBA_D0 L28
FBA_D1 M29
FBA_D2 L29
FBA_D3 M28
FBA_D4 N31
FBA_D5 P29
FBA_D6 R29
FBA_D7 P28
FBA_D8 J28
FBA_D9 H29
FBA_D10 J29
FBA_D11 H28
FBA_D12 G29
FBA_D13 E31
FBA_D14 E32
FBA_D15 F30
FBA_D16 C34
FBA_D17 D32
FBA_D18 B33
FBA_D19 C33
FBA_D20 F33
FBA_D21 F32
FBA_D22 H33
FBA_D23 H32
FBA_D24 P34
FBA_D25 P32
FBA_D26 P31
FBA_D27 P33
FBA_D28 L31
FBA_D29 L34
FBA_D30 L32
FBA_D31 L33
FBA_D32 AG28
FBA_D33 AF29
FBA_D34 AG29
FBA_D35 AF28
FBA_D36 AD30
FBA_D37 AD29
FBA_D38 AC29
FBA_D39 AD28
FBA_D40 AJ29
FBA_D41 AK29
FBA_D42 AJ30
FBA_D43 AK28
FBA_D44 AM29
FBA_D45 AM31
FBA_D46 AN29
FBA_D47 AM30
FBA_D48 AN31
FBA_D49 AN32
FBA_D50 AP30
FBA_D51 AP32
FBA_D52 AM33
FBA_D53 AL31
FBA_D54 AK33
FBA_D55 AK32
FBA_D56 AD34
FBA_D57 AD32
FBA_D58 AC30
FBA_D59 AD33
FBA_D60 AF31
FBA_D61 AG34
FBA_D62 AG32
FBA_D63 AG33

FBA_WCK01 K31
FBA_WCK01* L30
FBA_WCK23 H34
FBA_WCK23* J34
FBA_WCK45 AG30
FBA_WCK45* AG31
FBA_WCK67 AJ34
FBA_WCK67* AK34
FBA_WCKB01 J30
FBA_WCKB01* J31
FBA_WCKB23 J32
FBA_WCKB23* J33
FBA_WCKB45 AH31
FBA_WCKB45* AJ31
FBA_WCKB67 AJ32
FBA_WCKB67* AJ33

FBA_CMD0 U30
FBA_CMD1 T31
FBA_CMD2 U29
FBA_CMD3 R34
FBA_CMD4 R33
FBA_CMD5 U32
FBA_CMD6 U33
FBA_CMD7 U28
FBA_CMD8 V28
FBA_CMD9 V29
FBA_CMD10 V30
FBA_CMD11 U34
FBA_CMD12 U31
FBA_CMD13 V34
FBA_CMD14 V33
FBA_CMD15 Y32
FBA_CMD16 AA31
FBA_CMD17 AA29
FBA_CMD18 AA28
FBA_CMD19 AC34
FBA_CMD20 AC33
FBA_CMD21 AA32
FBA_CMD22 AA33
FBA_CMD23 Y28
FBA_CMD24 Y29
FBA_CMD25 W31
FBA_CMD26 Y30
FBA_CMD27 AA34
FBA_CMD28 Y31
FBA_CMD29 Y34
FBA_CMD30 Y33
FBA_CMD31 V31

FBA_CLK0 R30
FBA_CLK0* R31
FBA_CLK1 AB31
FBA_CLK1* AC31

FBA_DQM0 P30
FBA_DQM1 F31
FBA_DQM2 F34
FBA_DQM3 M32
FBA_DQM4 AD31
FBA_DQM5 AL29
FBA_DQM6 AM32
FBA_DQM7 AF34

FBA_DQS_RN0 M30 NC
FBA_DQS_RN1 H30 NC
FBA_DQS_RN2 E34 NC
FBA_DQS_RN3 M34 NC
FBA_DQS_RN4 AF30 NC
FBA_DQS_RN5 AK31 NC
FBA_DQS_RN6 AM34 NC
FBA_DQS_RN7 AF32 NC

FBA_DQS_WP0 M31
FBA_DQS_WP1 G31
FBA_DQS_WP2 E33
FBA_DQS_WP3 M33
FBA_DQS_WP4 AE31
FBA_DQS_WP5 AK30
FBA_DQS_WP6 AN33
FBA_DQS_WP7 AF33

FBA_DLL_AVDD K27 PP1V05_GPU_FB_DLL_AVDD 77
FBA_PLL_AVDD U27 PP1V05_GPU_FB_PLL_AVDD 77

FBA_DEBUG R28 GPU_FBA_DEBUG0
FBA_DEBUG AC28 GPU_FBA_DEBUG1

FB_CAL_PD_VDDQ J27 FB_CAL_PD_VDDQ 77
FB_CAL_PU_GND H27 FB_CAL_PU_GND 77
FB_CAL_TERM_GND H25 FB_CAL_TERM_GND
FB_CLAMP E1 FB_CLAMP
FBA_CMD_RFU R32 NC
FBA_CMD_RFU AC32 NC

FB_VDDQ_SENSE F1 GPU_FBVDDQ_SENSE_P 78 101
FB_GND_SENSE F2 GPU_FBVDDQ_SENSE_N 78 101

FB_A0_DBI_L<0> 6 79 100
FB_A0_DBI_L<1> 6 79 100
FB_A0_DBI_L<2> 6 79 100
FB_A0_DBI_L<3> 6 79 100
FB_A1_DBI_L<0> 6 79 100
FB_A1_DBI_L<1> 6 79 100
FB_A1_DBI_L<2> 6 79 100
FB_A1_DBI_L<3> 6 79 100

FB_A0_EDC<0> 6 79 100
FB_A0_EDC<1> 6 79 100
FB_A0_EDC<2> 6 79 100
FB_A0_EDC<3> 6 79 100
FB_A1_EDC<0> 6 79 100
FB_A1_EDC<1> 6 79 100
FB_A1_EDC<2> 6 79 100
FB_A1_EDC<3> 6 79 100

FB_A0_CS_L 79 100
FB_A0_A<3> 6 79 100
FB_A0_A<2> 6 79 100
FB_A0_A<4> 6 79 100
FB_A0_A<5> 6 79 100
FB_A0_WE_L 79 100
FB_A0_A<7> 6 79 100
FB_A0_A<6> 6 79 100
FB_A0_ABI_L 6 79 100
FB_A0_A<8> 6 79 100
FB_A0_A<0> 6 79 100
FB_A0_A<1> 6 79 100
FB_A0_RAS_L 79 100
FB_A0_RESET_L 77 79 100
FB_A0_CKE_L 77 79 100
FB_A1_CS_L 79 100
FB_A1_A<3> 6 79 100
FB_A1_A<2> 6 79 100
FB_A1_A<4> 6 79 100
FB_A1_A<5> 6 79 100
FB_A1_WE_L 79 100
FB_A1_A<7> 6 79 100
FB_A1_A<6> 6 79 100
FB_A1_ABI_L 6 79 100
FB_A1_A<8> 6 79 100
FB_A1_A<0> 6 79 100
FB_A1_A<1> 6 79 100
FB_A1_RAS_L 79 100
FB_A1_RESET_L 77 79 100
FB_A1_CKE_L 77 79 100
FB_A1_CAS_L 79 100
FB_A0_CLK_P 79 100
FB_A0_CLK_N 79 100
FB_A1_CLK_P 79 100
FB_A1_CLK_N 79 100

FB_A0_RESET_L 100 79 77
R8250 10K 1% 1/20W MF 201
FB_A1_RESET_L 100 79 77
R8251 10K 1% 1/20W MF 201

FB_A0_CKE_L 77 79 100
R8252 10K 1% 1/20W MF 201
FB_A1_CKE_L 77 79 100
R8253 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 7 77
NOSTUFF R8258 1.33K 1% 1/20W MF 201 PLACE_NEAR=U8000.H26:8.4MM
FB_VREF 77
NOSTUFF R8259 1.33K 1% 1/20W MF 201 PLACE_NEAR=U8000.H25:8.4MM
NOSTUFF C8260 0.1UF 10% 6.3V X5R 201 PLACE_NEAR=U8000.H26:8.4MM
FB VREF GEN (TEST ONLY)

=PP1V35_GPU_S0_FB 7 77
R8203 60.4 1% 1/20W MF 201
R8202 60.4 1% 1/20W MF 201
R8270 100 5% 1/20W MF 201
R8201 60.4 1% 1/20W MF 201 PLACE_NEAR=U8000.H25:8.4MM
R8261 10K 1% 1/20W MF 201
R8271 100 5% 1/20W MF 201
PLACE CLOSE TO BGA

77 FB_CAL_PU_GND
R8204 40.2 1% 1/20W MF 201 PLACE_NEAR=U8000.H27:8.4MM
=PP1V35_GPU_S0_FB 7 77
R8205 40.2 1% 1/20W MF 201 PLACE_NEAR=U8000.J27:8.4MM
FB_CAL_PD_VDDQ 77

OMIT_TABLE

U8000
NV-GK107
BGA
(4 OF 10)
MEM INTRERFACE B

FBB_D0 G9
FBB_D1 E9
FBB_D2 G8
FBB_D3 F9
FBB_D4 F11
FBB_D5 G11
FBB_D6 F12
FBB_D7 G12
FBB_D8 G6
FBB_D9 F5
FBB_D10 E6
FBB_D11 F6
FBB_D12 F4
FBB_D13 G4
FBB_D14 E2
FBB_D15 F3
FBB_D16 C2
FBB_D17 D4
FBB_D18 D3
FBB_D19 C1
FBB_D20 B3
FBB_D21 C4
FBB_D22 B5
FBB_D23 C5
FBB_D24 A11
FBB_D25 C11
FBB_D26 D11
FBB_D27 B11
FBB_D28 D8
FBB_D29 A8
FBB_D30 C8
FBB_D31 B8
FBB_D32 F24
FBB_D33 G23
FBB_D34 E24
FBB_D35 G24
FBB_D36 D21
FBB_D37 E21
FBB_D38 G21
FBB_D39 F21
FBB_D40 G27
FBB_D41 D27
FBB_D42 G26
FBB_D43 E27
FBB_D44 E29
FBB_D45 F29
FBB_D46 E30
FBB_D47 D30
FBB_D48 A32
FBB_D49 C31
FBB_D50 C32
FBB_D51 B32
FBB_D52 D29
FBB_D53 A29
FBB_D54 C29
FBB_D55 B29
FBB_D56 B21
FBB_D57 C23
FBB_D58 A21
FBB_D59 C21
FBB_D60 B24
FBB_D61 C24
FBB_D62 B26
FBB_D63 C26

FBB_WCK01 F8
FBB_WCK01* E8
FBB_WCK23 A5
FBB_WCK23* A6
FBB_WCK45 D24
FBB_WCK45* D25
FBB_WCK67 B27
FBB_WCK67* C27
FBB_WCKB01 D6
FBB_WCKB01* D7
FBB_WCKB23 C6
FBB_WCKB23* B6
FBB_WCKB45 F26
FBB_WCKB45* E26
FBB_WCKB67 A26
FBB_WCKB67* A27

FBB_CMD0 D13
FBB_CMD1 E14
FBB_CMD2 F14
FBB_CMD3 A12
FBB_CMD4 B12
FBB_CMD5 C14
FBB_CMD6 B14
FBB_CMD7 G15
FBB_CMD8 F15
FBB_CMD9 E15
FBB_CMD10 D15
FBB_CMD11 A14
FBB_CMD12 D14
FBB_CMD13 A15
FBB_CMD14 B15
FBB_CMD15 C17
FBB_CMD16 D18
FBB_CMD17 E18
FBB_CMD18 F18
FBB_CMD19 A20
FBB_CMD20 B20
FBB_CMD21 C18
FBB_CMD22 B18
FBB_CMD23 G18
FBB_CMD24 G17
FBB_CMD25 F17
FBB_CMD26 D16
FBB_CMD27 A18
FBB_CMD28 D17
FBB_CMD29 A17
FBB_CMD30 B17
FBB_CMD31 E17

FBB_CLK0 D12
FBB_CLK0* E12
FBB_CLK1 E20
FBB_CLK1* F20

FBB_DQM0 E11
FBB_DQM1 E3
FBB_DQM2 A3
FBB_DQM3 C9
FBB_DQM4 F23
FBB_DQM5 F27
FBB_DQM6 C30
FBB_DQM7 A24

FBB_DQS_RN0 D9 NC
FBB_DQS_RN1 E4 NC
FBB_DQS_RN2 B2 NC
FBB_DQS_RN3 A9 NC
FBB_DQS_RN4 D22 NC
FBB_DQS_RN5 D28 NC
FBB_DQS_RN6 A30 NC
FBB_DQS_RN7 B23 NC

FBB_DQS_WP0 D10
FBB_DQS_WP1 D5
FBB_DQS_WP2 C3
FBB_DQS_WP3 B9
FBB_DQS_WP4 E23
FBB_DQS_WP5 E28
FBB_DQS_WP6 B30
FBB_DQS_WP7 A23

FBB_PLL_AVDD H17 77 PP1V05_GPU_FB_PLL_AVDD
FBB_DEBUG0 G14 GPU_FBB_DEBUG0 77
FBB_DEBUG1 G20 GPU_FBB_DEBUG1 77
FB_VREF H26 FB_VREF 77
FBB_CMD_RFU0 C12 NC
FBB_CMD_RFU1 C20 NC

FB_B0_DBI_L<0> 6 80 100
FB_B0_DBI_L<1> 6 80 100
FB_B0_DBI_L<2> 6 80 100
FB_B0_DBI_L<3> 6 80 100
FB_B1_DBI_L<0> 6 80 100
FB_B1_DBI_L<1> 6 80 100
FB_B1_DBI_L<2> 6 80 100
FB_B1_DBI_L<3> 6 80 100

FB_B0_EDC<0> 6 80 100
FB_B0_EDC<1> 6 80 100
FB_B0_EDC<2> 6 80 100
FB_B0_EDC<3> 6 80 100
FB_B1_EDC<0> 6 80 100
FB_B1_EDC<1> 6 80 100
FB_B1_EDC<2> 6 80 100
FB_B1_EDC<3> 6 80 100

FB_B0_CS_L 80 100
FB_B0_A<3> 6 80 100
FB_B0_A<2> 6 80 100
FB_B0_A<4> 6 80 100
FB_B0_A<5> 6 80 100
FB_B0_WE_L 80 100
FB_B0_A<7> 6 80 100
FB_B0_A<6> 6 80 100
FB_B0_ABI_L 6 80 100
FB_B0_A<8> 6 80 100
FB_B0_A<0> 6 80 100
FB_B0_A<1> 6 80 100
FB_B0_RAS_L 80 100
FB_B0_RESET_L 77 80 100
FB_B0_CKE_L 77 80 100
FB_B0_CAS_L 80 100
FB_B1_CS_L 80 100
FB_B1_A<3> 6 83 77 80 100
FB_B1_A<2> 80 100
FB_B1_A<4> 6 80 100
FB_B1_A<5> 6 80 100
FB_B1_WE_L 80 100
FB_B1_A<7> 6 80 100
FB_B1_A<6> 6 80 100
FB_B1_ABI_L 6 80 100
FB_B1_A<8> 6 80 100
FB_B1_A<0> 6 80 100
FB_B1_A<1> 6 80 100
FB_B1_RAS_L 80 100
FB_B1_RESET_L 77 80 100
FB_B1_CKE_L 77 80 100
FB_B1_CAS_L 80 100
FB_B0_CLK_P 80 100
FB_B0_CLK_N 80 100
FB_B1_CLK_P 80 100
FB_B1_CLK_N 80 100

=PP1V35_GPU_S0_FB 7 77
R8206 60.4 1% 1/20W MF 201
R8207 60.4 1% 1/20W MF 201
GPU_FBB_DEBUG0 77
GPU_FBB_DEBUG1 77

Page Notes

Power aliases required by this page:
- =PP1V35_GPU_S0_REG
- =PP1V05_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V05_GPU_PEX_IOVDD 7 77 83
L8201 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050HM
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
PP1V05_GPU_FB_PLL_AVDD 77
C8201 22UF 20% 6.3V X5R-CERM2 0603
C8202 1UF 20% 6.3V X5R 0201
C8203 0.1UF 10% 6.3V X5R 201
FB PLL & DLL VDD

=PP1V05_GPU_PEX_IOVDD 7 77 83
L8202 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050HM
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
PP1V05_GPU_FB_DLL_AVDD 77
C8208 22UF 20% 6.3V X5R-CERM2 0603
C8204 1UF 20% 6.3V X5R 0201
C8205 0.1UF 10% 6.3V X5R 201

FB_B0_RESET_L 100 80 77
R8254 10K 1% 1/20W MF 201
FB_B1_RESET_L 100 80 77
R8255 10K 1% 1/20W MF 201
FB_B0_CKE_L 77 80 100
R8256 10K 1% 1/20W MF 201
FB_B1_CKE_L 77 80 100
R8257 10K 1% 1/20W MF 201

MEM VREFC & VREFD SWITCH
FB_SW_LEG 80 79 OUT
CRITICAL
Q8265 SSM3K15FV SOD-VESM-HF
GPU_ALT_VREF IN 82

C8206 1UF 20% 6.3V X5R 0201
C8207 0.1UF 10% 6.3V X5R 201

SYNC_MASTER=J31_SREE SYNC_DATE=10/25/2011
PAGE TITLE: KEPLER FRAME BUFFER I/F
Apple Inc.
DRAWING NUMBER: 051-9585
SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 82 OF 132
SHEET: 77 OF 105

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GPU FB SUPPLY

VOUT = 1.5V / 1.35V

11A MAX OUTPUT

F = 500 KHZ

U8350 ISL95870AH UTQFN CRITICAL

GPIO(16)	VID1	VID0	FBVDD
	0	0	1.5V
	1	0	1.35V

GPU 1V05 SUPPLY

VOUT = 1.05V

5.3A MAX OUTPUT

F = 500 KHZ

U8310 ISL95870 UTQFN CRITICAL

Vout = 0.5V * (1 + Ra / Rb)

PAGE TITLE	1V05 GPU / 1V35 FB POWER SUPPLY
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 83 OF 132
	SHEET 78 OF 105

SYNC_MASTER=J31_JACK SYNC_DATE=11/16/2011

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Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

CK TERMINATION - A0

PLACE_NEAR=U8400.J11:8.4MM

R8401 40.2 1% 1/20W MF 201
R8402 40.2 1% 1/20W MF 201
C8490 0.01UF 10% 10V X5R-CERM 0201

FB_A0_CLK_P, FB_A0_CLK_N, FB_A0_CK_MID

R8400 120 1% 1/20W MF 201
R8404 120 1% 1/20W MF 201
R8403 120 1% 1/20W MF 201

CK TERMINATION - A1

R8451 40.2 1% 1/20W MF 201
R8452 40.2 1% 1/20W MF 201
C8491 0.01UF 10% 10V X5R-CERM 0201

FB_A1_CLK_P, FB_A1_CLK_N, FB_A1_CK_MID

U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT_TABLE

FB_A0_A<2>	H11	BA0/A2	
FB_A0_A<5>	K10	BA1/A5	
FB_A0_A<4>	K11	BA2/A4	
FB_A0_A<3>	H10	BA3/A3	
FB_A0_A<7>	K4	A8/A7	
FB_A0_A<1>	H5	A9/A1	
FB_A0_A<0>	H4	A10/A0	
FB_A0_A<6>	K5	A11/A6	
FB_A0_CKE_L	J3	CKE*	
FB_A0_CLK_P	J12	CK	
FB_A0_CLK_N	J11	CK*	
FB_A0_CS_L	G12	CS*	
FB_A0_WE_L	L12	WE*	
FB_A0_CAS_L	L3	CAS*	
FB_A0_RAS_L	G3	RAS*	
FB_A0_ZQ	J13	ZQ	
FB_A0_MF	J1	MF (MF=0)	
FB_A0_SEN	J10	SEN	
FB_A0_RESET_L	J2	RESET*	
FB_A0_ABI_L	J4	ABI*	
FB_A0_EDC<0>	C2	EDC0	
FB_A0_EDC<1>	C13	EDC1	
FB_A0_EDC<2>	R13	EDC2	
FB_A0_EDC<3>	R2	EDC3	
FB_A0_WCLK_P<0>	D4	WCK01	
FB_A0_WCLK_N<0>	D5	WCK01*	
FB_A0_WCLK_P<1>	P4	WCK23	
FB_A0_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_A0_DBI_L<0>	B1
DBI1*	D13	FB_A0_DBI_L<1>	B1
DBI2*	P13	FB_A0_DBI_L<2>	B1
DBI3*	P2	FB_A0_DBI_L<3>	B1
DQ0	A4	FB_A0_DQ<0>	B1
DQ1	A2	FB_A0_DQ<1>	B1
DQ2	B4	FB_A0_DQ<2>	B1
DQ3	B2	FB_A0_DQ<3>	B1
DQ4	E4	FB_A0_DQ<4>	B1
DQ5	E2	FB_A0_DQ<5>	B1
DQ6	F4	FB_A0_DQ<6>	B1
DQ7	F2	FB_A0_DQ<7>	B1
DQ8	A11	FB_A0_DQ<8>	B1
DQ9	A13	FB_A0_DQ<9>	B1
DQ10	B11	FB_A0_DQ<10>	B1
DQ11	B13	FB_A0_DQ<11>	B1
DQ12	E11	FB_A0_DQ<12>	B1
DQ13	E13	FB_A0_DQ<13>	B1
DQ14	F11	FB_A0_DQ<14>	B1
DQ15	F13	FB_A0_DQ<15>	B1
DQ16	U11	FB_A0_DQ<16>	B1
DQ17	U13	FB_A0_DQ<17>	B1
DQ18	T11	FB_A0_DQ<18>	B1
DQ19	T13	FB_A0_DQ<19>	B1
DQ20	N11	FB_A0_DQ<20>	B1
DQ21	N13	FB_A0_DQ<21>	B1
DQ22	M11	FB_A0_DQ<22>	B1
DQ23	M13	FB_A0_DQ<23>	B1
DQ24	U4	FB_A0_DQ<24>	B1
DQ25	U2	FB_A0_DQ<25>	B1
DQ26	T4	FB_A0_DQ<26>	B1
DQ27	T2	FB_A0_DQ<27>	B1
DQ28	N4	FB_A0_DQ<28>	B1
DQ29	N2	FB_A0_DQ<29>	B1
DQ30	M4	FB_A0_DQ<30>	B1
DQ31	M2	FB_A0_DQ<31>	B1
NC	A5, J5, U5	NC	
		FB_A0_A<8>	IN

U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT_TABLE

VDD, VDDQ, VSS, VSSQ, VREFC, VREFD

=PP1V35_GPU_FBVDDQ

C8400 4.7UF 20% 6.3V X5R 402
C8401 4.7UF 20% 6.3V X5R 402
C8402 4.7UF 20% 6.3V X5R 402
C8403 4.7UF 20% 6.3V X5R 402
C8404 4.7UF 20% 6.3V X5R 402
C8405 4.7UF 20% 6.3V X5R 402
C8406 1UF 20% 6.3V X5R 0201
C8407 1UF 20% 6.3V X5R 0201
C8408 1UF 20% 6.3V X5R 0201
C8409 1UF 20% 6.3V X5R 0201
C8410 1UF 20% 6.3V X5R 0201
C8411 1UF 20% 6.3V X5R 0201
C8412 1UF 20% 6.3V X5R 0201
C8413 1UF 20% 6.3V X5R 0201
C8414 1UF 20% 6.3V X5R 0201
C8415 1UF 20% 6.3V X5R 0201
C8416 0.1UF 10% 6.3V X5R 201
C8417 0.1UF 10% 6.3V X5R 201
C8418 0.1UF 10% 6.3V X5R 201
C8419 0.1UF 10% 6.3V X5R 201
C8420 0.1UF 10% 6.3V X5R 201
C8421 0.1UF 10% 6.3V X5R 201
C8422 0.1UF 10% 6.3V X5R 201
C8423 0.1UF 10% 6.3V X5R 201
C8424 0.1UF 10% 6.3V X5R 201
C8425 0.1UF 10% 6.3V X5R 201

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM

R8430 549 1% 1/20W MF 201
R8431 1.33K 1% 1/20W MF 201
R8434 931 1% 1/20W MF 201
C8431 820PF 10% 25V X7R-CERM 0201
FB_A0_VREFC
FB_SW_LEG

PLACE CLOSE TO U8400

R8432 549 1% 1/20W MF 201
R8433 1.33K 1% 1/20W MF 201
R8435 931 1% 1/20W MF 201
C8432 820PF 10% 25V X7R-CERM 0201
C8433 820PF 10% 25V X7R-CERM 0201
FB_A0_VREFD

U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT_TABLE

FB_A1_A<2>	H11	BA0/A2	
FB_A1_A<5>	K10	BA1/A5	
FB_A1_A<4>	K11	BA2/A4	
FB_A1_A<3>	H10	BA3/A3	
FB_A1_A<7>	K4	A8/A7	
FB_A1_A<1>	H5	A9/A1	
FB_A1_A<0>	H4	A10/A0	
FB_A1_A<6>	K5	A11/A6	
FB_A1_CKE_L	J3	CKE*	
FB_A1_CLK_P	J12	CK	
FB_A1_CLK_N	J11	CK*	
FB_A1_CS_L	G12	CS*	
FB_A1_WE_L	L12	WE*	
FB_A1_CAS_L	L3	CAS*	
FB_A1_RAS_L	G3	RAS*	
FB_A1_ZQ	J13	ZQ	
FB_A1_MF	J1	MF (MF=0)	
FB_A1_SEN	J10	SEN	
FB_A1_RESET_L	J2	RESET*	
FB_A1_ABI_L	J4	ABI*	
FB_A1_EDC<0>	C2	EDC0	
FB_A1_EDC<1>	C13	EDC1	
FB_A1_EDC<2>	R13	EDC2	
FB_A1_EDC<3>	R2	EDC3	
FB_A1_WCLK_P<0>	D4	WCK01	
FB_A1_WCLK_N<0>	D5	WCK01*	
FB_A1_WCLK_P<1>	P4	WCK23	
FB_A1_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_A1_DBI_L<0>	B1
DBI1*	D13	FB_A1_DBI_L<1>	B1
DBI2*	P13	FB_A1_DBI_L<2>	B1
DBI3*	P2	FB_A1_DBI_L<3>	B1
DQ0	A4	FB_A1_DQ<0>	B1
DQ1	A2	FB_A1_DQ<1>	B1
DQ2	B4	FB_A1_DQ<2>	B1
DQ3	B2	FB_A1_DQ<3>	B1
DQ4	E4	FB_A1_DQ<4>	B1
DQ5	E2	FB_A1_DQ<5>	B1
DQ6	F4	FB_A1_DQ<6>	B1
DQ7	F2	FB_A1_DQ<7>	B1
DQ8	A11	FB_A1_DQ<8>	B1
DQ9	A13	FB_A1_DQ<9>	B1
DQ10	B11	FB_A1_DQ<10>	B1
DQ11	B13	FB_A1_DQ<11>	B1
DQ12	E11	FB_A1_DQ<12>	B1
DQ13	E13	FB_A1_DQ<13>	B1
DQ14	F11	FB_A1_DQ<14>	B1
DQ15	F13	FB_A1_DQ<15>	B1
DQ16	U11	FB_A1_DQ<16>	B1
DQ17	U13	FB_A1_DQ<17>	B1
DQ18	T11	FB_A1_DQ<18>	B1
DQ19	T13	FB_A1_DQ<19>	B1
DQ20	N11	FB_A1_DQ<20>	B1
DQ21	N13	FB_A1_DQ<21>	B1
DQ22	M11	FB_A1_DQ<22>	B1
DQ23	M13	FB_A1_DQ<23>	B1
DQ24	U4	FB_A1_DQ<24>	B1
DQ25	U2	FB_A1_DQ<25>	B1
DQ26	T4	FB_A1_DQ<26>	B1
DQ27	T2	FB_A1_DQ<27>	B1
DQ28	N4	FB_A1_DQ<28>	B1
DQ29	N2	FB_A1_DQ<29>	B1
DQ30	M4	FB_A1_DQ<30>	B1
DQ31	M2	FB_A1_DQ<31>	B1
NC	A5, J5, U5	NC	
		FB_A1_A<8>	IN

U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT_TABLE

VDD, VDDQ, VSS, VSSQ, VREFC, VREFD

C8450 4.7UF 20% 6.3V X5R 402
C8451 4.7UF 20% 6.3V X5R 402
C8452 4.7UF 20% 6.3V X5R 402
C8453 4.7UF 20% 6.3V X5R 402
C8454 4.7UF 20% 6.3V X5R 402
C8455 4.7UF 20% 6.3V X5R 402
C8456 1UF 20% 6.3V X5R 0201
C8457 1UF 20% 6.3V X5R 0201
C8458 1UF 20% 6.3V X5R 0201
C8459 1UF 20% 6.3V X5R 0201
C8460 1UF 20% 6.3V X5R 0201
C8461 1UF 20% 6.3V X5R 0201
C8462 1UF 20% 6.3V X5R 0201
C8463 1UF 20% 6.3V X5R 0201
C8464 1UF 20% 6.3V X5R 0201
C8465 1UF 20% 6.3V X5R 0201
C8466 0.1UF 10% 6.3V X5R 201
C8467 0.1UF 10% 6.3V X5R 201
C8468 0.1UF 10% 6.3V X5R 201
C8469 0.1UF 10% 6.3V X5R 201
C8470 0.1UF 10% 6.3V X5R 201
C8471 0.1UF 10% 6.3V X5R 201
C8472 0.1UF 10% 6.3V X5R 201
C8473 0.1UF 10% 6.3V X5R 201
C8474 0.1UF 10% 6.3V X5R 201
C8475 0.1UF 10% 6.3V X5R 201

R8450 120 1% 1/20W MF 201
R8454 120 1% 1/20W MF 201
R8453 120 1% 1/20W MF 201

R8480 549 1% 1/20W MF 201
R8481 1.33K 1% 1/20W MF 201
R8484 931 1% 1/20W MF 201
C8481 820PF 10% 25V X7R-CERM 0201
FB_A1_VREFC
FB_SW_LEG

PLACE CLOSE TO U8450

R8482 549 1% 1/20W MF 201
R8483 1.33K 1% 1/20W MF 201
R8485 931 1% 1/20W MF 201
C8482 820PF 10% 25V X7R-CERM 0201
C8483 820PF 10% 25V X7R-CERM 0201
FB_A1_VREFD

SYNC_MASTER=J31_SREE
SYNC_DATE=10/25/2013

PAGE TITLE: GDDR5 Frame Buffer A

Apple Inc.

DRAWING NUMBER	051-9585
SIZE	D
REVISION	3.0.0
BRANCH	
PAGE	84 OF 132
SHEET	79 OF 105

Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

CK TERMINATION - B0

R8501 40.2 1% 1/20W MF 201 — FB_B0_CLK_P — FBB0_CK_MID

R8502 40.2 1% 1/20W MF 201 — FB_B0_CLK_N — FBB0_CK_MID

C8590 0.01UF 10% 10V X5R-CERM 0201

CK TERMINATION - B1

R8551 40.2 1% 1/20W MF 201 — FB_B1_CLK_P — FBB1_CK_MID

R8552 40.2 1% 1/20W MF 201 — FB_B1_CLK_N — FBB1_CK_MID

C8591 0.01UF 10% 10V X5R-CERM 0201

R8500 120 1% 1/20W MF 201

R8504 120 1% 1/20W MF 201

R8503 120 1% 1/20W MF 201

U8500

32MX32-1.25GHZ-MFL

BGA

H5GQ1H24AFR-T2C

(1 OF 2)

FB_B0_A<2>	H11	BA0/A2	
FB_B0_A<5>	K10	BA1/A5	
FB_B0_A<4>	K11	BA2/A4	
FB_B0_A<3>	H10	BA3/A3	
FB_B0_A<7>	K4	A8/A7	
FB_B0_A<1>	H5	A9/A1	
FB_B0_A<0>	H4	A10/A0	
FB_B0_A<6>	K5	A11/A6	
FB_B0_CKE_L	J3	CKE*	
FB_B0_CLK_P	J12	CK	
FB_B0_CLK_N	J11	CK*	
FB_B0_CS_L	G12	CS*	
FB_B0_WE_L	L12	WE*	
FB_B0_CAS_L	L3	CAS*	
FB_B0_RAS_L	G3	RAS*	
FB_B0_ZQ	J13	ZQ	
FB_B0_MF	J1	MF (MF=0)	
FB_B0_SEN	J10	SEN	
FB_B0_RESET_L	J2	RESET*	
FB_B0_ABI_L	J4	ABI*	
FB_B0_EDC<0>	C2	EDC0	
FB_B0_EDC<1>	C13	EDC1	
FB_B0_EDC<2>	R13	EDC2	
FB_B0_EDC<3>	R2	EDC3	
FB_B0_WCLK_P<0>	D4	WCK01	
FB_B0_WCLK_N<0>	D5	WCK01*	
FB_B0_WCLK_P<1>	P4	WCK23	
FB_B0_WCLK_N<1>	P5	WCK23*	

OMIT_TABLE

DBI0*	D2	FB_B0_DBI_L<0>	
DBI1*	D13	FB_B0_DBI_L<1>	
DBI2*	P13	FB_B0_DBI_L<2>	
DBI3*	P2	FB_B0_DBI_L<3>	
DQ0	A4	FB_B0_DQ<0>	
DQ1	A2	FB_B0_DQ<1>	
DQ2	B4	FB_B0_DQ<2>	
DQ3	B2	FB_B0_DQ<3>	
DQ4	E4	FB_B0_DQ<4>	
DQ5	E2	FB_B0_DQ<5>	
DQ6	F4	FB_B0_DQ<6>	
DQ7	F2	FB_B0_DQ<7>	
DQ8	A11	FB_B0_DQ<8>	
DQ9	A13	FB_B0_DQ<9>	
DQ10	B11	FB_B0_DQ<10>	
DQ11	B13	FB_B0_DQ<11>	
DQ12	E11	FB_B0_DQ<12>	
DQ13	E13	FB_B0_DQ<13>	
DQ14	F11	FB_B0_DQ<14>	
DQ15	F13	FB_B0_DQ<15>	
DQ16	U11	FB_B0_DQ<16>	
DQ17	U13	FB_B0_DQ<17>	
DQ18	T11	FB_B0_DQ<18>	
DQ19	T13	FB_B0_DQ<19>	
DQ20	N11	FB_B0_DQ<20>	
DQ21	N13	FB_B0_DQ<21>	
DQ22	M11	FB_B0_DQ<22>	
DQ23	M13	FB_B0_DQ<23>	
DQ24	U4	FB_B0_DQ<24>	
DQ25	U2	FB_B0_DQ<25>	
DQ26	T4	FB_B0_DQ<26>	
DQ27	T2	FB_B0_DQ<27>	
DQ28	N4	FB_B0_DQ<28>	
DQ29	N2	FB_B0_DQ<29>	
DQ30	M4	FB_B0_DQ<30>	
DQ31	M2	FB_B0_DQ<31>	
NC	A5, J5, U5	NC	
		FB_B0_A<8>	

U8550

32MX32-1.25GHZ-MFL

BGA

H5GQ1H24AFR-T2C

(1 OF 2)

FB_B1_A<2>	H11	BA0/A2	
FB_B1_A<5>	K10	BA1/A5	
FB_B1_A<4>	K11	BA2/A4	
FB_B1_A<3>	H10	BA3/A3	
FB_B1_A<7>	K4	A8/A7	
FB_B1_A<1>	H5	A9/A1	
FB_B1_A<0>	H4	A10/A0	
FB_B1_A<6>	K5	A11/A6	
FB_B1_CKE_L	J3	CKE*	
FB_B1_CLK_P	J12	CK	
FB_B1_CLK_N	J11	CK*	
FB_B1_CS_L	G12	CS*	
FB_B1_WE_L	L12	WE*	
FB_B1_CAS_L	L3	CAS*	
FB_B1_RAS_L	G3	RAS*	
FB_B1_ZQ	J13	ZQ	
FB_B1_MF	J1	MF (MF=0)	
FB_B1_SEN	J10	SEN	
FB_B1_RESET_L	J2	RESET*	
FB_B1_ABI_L	J4	ABI*	
FB_B1_EDC<0>	C2	EDC0	
FB_B1_EDC<1>	C13	EDC1	
FB_B1_EDC<2>	R13	EDC2	
FB_B1_EDC<3>	R2	EDC3	
FB_B1_WCLK_P<0>	D4	WCK01	
FB_B1_WCLK_N<0>	D5	WCK01*	
FB_B1_WCLK_P<1>	P4	WCK23	
FB_B1_WCLK_N<1>	P5	WCK23*	

OMIT_TABLE

DBI0*	D2	FB_B1_DBI_L<0>	
DBI1*	D13	FB_B1_DBI_L<1>	
DBI2*	P13	FB_B1_DBI_L<2>	
DBI3*	P2	FB_B1_DBI_L<3>	
DQ0	A4	FB_B1_DQ<0>	
DQ1	A2	FB_B1_DQ<1>	
DQ2	B4	FB_B1_DQ<2>	
DQ3	B2	FB_B1_DQ<3>	
DQ4	E4	FB_B1_DQ<4>	
DQ5	E2	FB_B1_DQ<5>	
DQ6	F4	FB_B1_DQ<6>	
DQ7	F2	FB_B1_DQ<7>	
DQ8	A11	FB_B1_DQ<8>	
DQ9	A13	FB_B1_DQ<9>	
DQ10	B11	FB_B1_DQ<10>	
DQ11	B13	FB_B1_DQ<11>	
DQ12	E11	FB_B1_DQ<12>	
DQ13	E13	FB_B1_DQ<13>	
DQ14	F11	FB_B1_DQ<14>	
DQ15	F13	FB_B1_DQ<15>	
DQ16	U11	FB_B1_DQ<16>	
DQ17	U13	FB_B1_DQ<17>	
DQ18	T11	FB_B1_DQ<18>	
DQ19	T13	FB_B1_DQ<19>	
DQ20	N11	FB_B1_DQ<20>	
DQ21	N13	FB_B1_DQ<21>	
DQ22	M11	FB_B1_DQ<22>	
DQ23	M13	FB_B1_DQ<23>	
DQ24	U4	FB_B1_DQ<24>	
DQ25	U2	FB_B1_DQ<25>	
DQ26	T4	FB_B1_DQ<26>	
DQ27	T2	FB_B1_DQ<27>	
DQ28	N4	FB_B1_DQ<28>	
DQ29	N2	FB_B1_DQ<29>	
DQ30	M4	FB_B1_DQ<30>	
DQ31	M2	FB_B1_DQ<31>	
NC	A5, J5, U5	NC	
		FB_B1_A<8>	

R8550 120 1% 1/20W MF 201

R8554 120 1% 1/20W MF 201

R8553 120 1% 1/20W MF 201

U8500

32MX32-1.25GHZ-MFL

BGA

H5GQ1H24AFR-T2C

(2 OF 2)

=PP1V35_GPU_FBVDDQ

C8500 4.7UF 20% 6.3V X5R 402

C8501 4.7UF 20% 6.3V X5R 402

C8502 4.7UF 20% 6.3V X5R 402

C8503 4.7UF 20% 6.3V X5R 402

C8504 4.7UF 20% 6.3V X5R 402

C8505 4.7UF 20% 6.3V X5R 402

C8506 1UF 20% 6.3V X5R 0201

C8507 1UF 20% 6.3V X5R 0201

C8508 1UF 20% 6.3V X5R 0201

C8509 1UF 20% 6.3V X5R 0201

C8510 1UF 20% 6.3V X5R 0201

C8511 1UF 20% 6.3V X5R 0201

C8512 1UF 20% 6.3V X5R 0201

C8513 1UF 20% 6.3V X5R 0201

C8514 1UF 20% 6.3V X5R 0201

C8515 1UF 20% 6.3V X5R 0201

C8516 0.1UF 10% 6.3V X5R 201

C8517 0.1UF 10% 6.3V X5R 201

C8518 0.1UF 10% 6.3V X5R 201

C8519 0.1UF 10% 6.3V X5R 201

C8520 0.1UF 10% 6.3V X5R 201

C8521 0.1UF 10% 6.3V X5R 201

C8522 0.1UF 10% 6.3V X5R 201

C8523 0.1UF 10% 6.3V X5R 201

C8524 0.1UF 10% 6.3V X5R 201

C8525 0.1UF 10% 6.3V X5R 201

VDD

VDDQ

VSS

VSSQ

VREFC

VREFD

OMIT_TABLE

PLACE CLOSE TO U8500

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM

R8530 549 1% 1/20W MF 201

R8531 1.33K 1% 1/20W MF 201

R8534 931 1% 1/20W MF 201

C8531 820PF 10% 25V X7R-CERM 0201

R8532 549 1% 1/20W MF 201

R8533 1.33K 1% 1/20W MF 201

R8535 931 1% 1/20W MF 201

C8532 820PF 10% 25V X7R-CERM 0201

C8533 820PF 10% 25V X7R-CERM 0201

FB_SW_LEG

U8550

32MX32-1.25GHZ-MFL

BGA

H5GQ1H24AFR-T2C

(2 OF 2)

=PP1V35_GPU_FBVDDQ

C8550 4.7UF 20% 6.3V X5R 402

C8551 4.7UF 20% 6.3V X5R 402

C8552 4.7UF 20% 6.3V X5R 402

C8553 4.7UF 20% 6.3V X5R 402

C8554 4.7UF 20% 6.3V X5R 402

C8555 4.7UF 20% 6.3V X5R 402

C8556 1UF 20% 6.3V X5R 0201

C8557 1UF 20% 6.3V X5R 0201

C8558 1UF 20% 6.3V X5R 0201

C8559 1UF 20% 6.3V X5R 0201

C8560 1UF 20% 6.3V X5R 0201

C8561 1UF 20% 6.3V X5R 0201

C8562 1UF 20% 6.3V X5R 0201

C8563 1UF 20% 6.3V X5R 0201

C8564 1UF 20% 6.3V X5R 0201

C8565 1UF 20% 6.3V X5R 0201

C8566 0.1UF 10% 6.3V X5R 201

C8567 0.1UF 10% 6.3V X5R 201

C8568 0.1UF 10% 6.3V X5R 201

C8569 0.1UF 10% 6.3V X5R 201

C8570 0.1UF 10% 6.3V X5R 201

C8571 0.1UF 10% 6.3V X5R 201

C8572 0.1UF 10% 6.3V X5R 201

C8573 0.1UF 10% 6.3V X5R 201

C8574 0.1UF 10% 6.3V X5R 201

C8575 0.1UF 10% 6.3V X5R 201

VDD

VDDQ

VSS

VSSQ

VREFC

VREFD

OMIT_TABLE

PLACE CLOSE TO U8550

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM

R8580 549 1% 1/20W MF 201

R8581 1.33K 1% 1/20W MF 201

R8584 931 1% 1/20W MF 201

C8581 820PF 10% 25V X7R-CERM 0201

R8582 549 1% 1/20W MF 201

R8583 1.33K 1% 1/20W MF 201

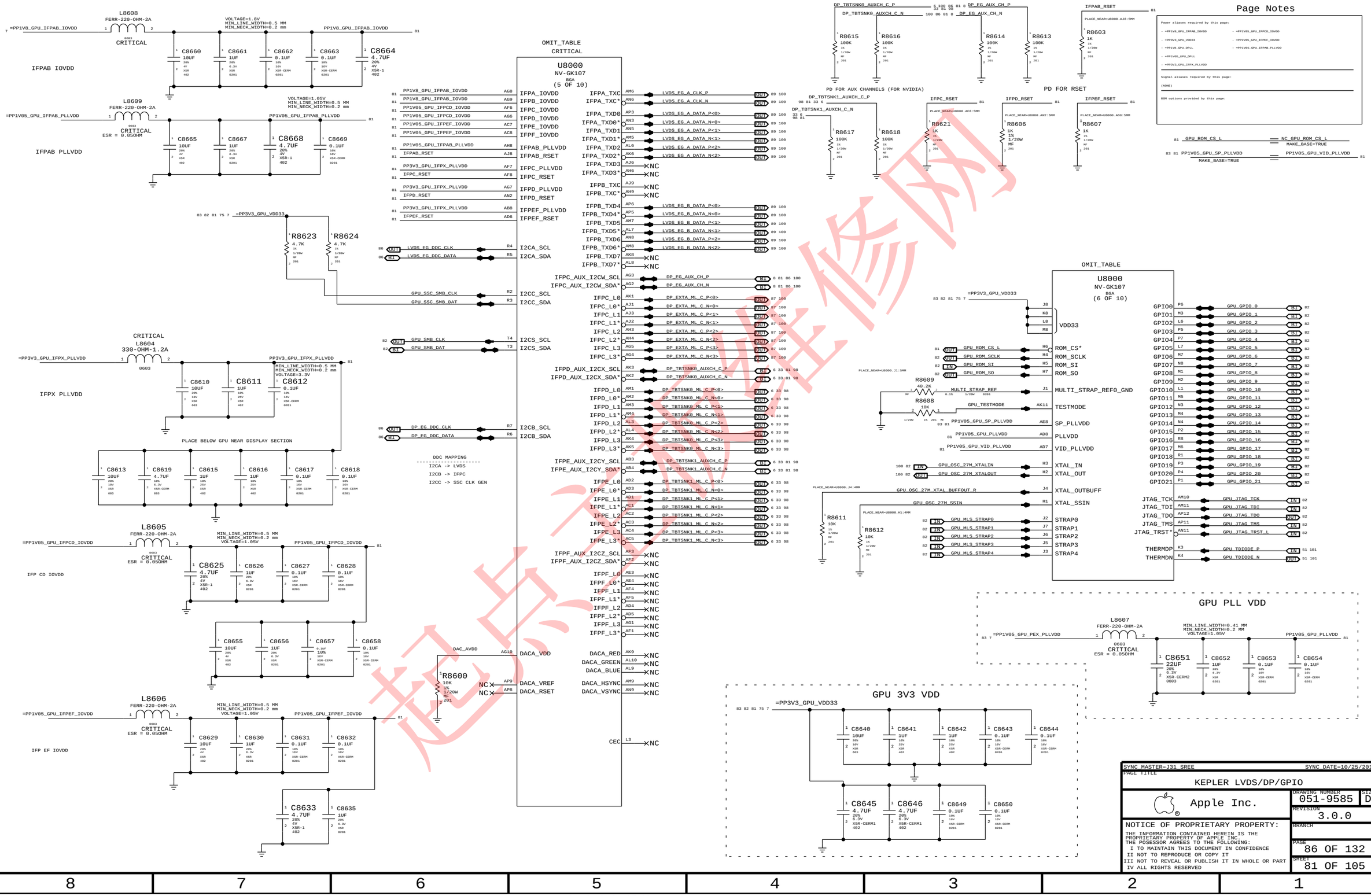
R8585 931 1% 1/20W MF 201

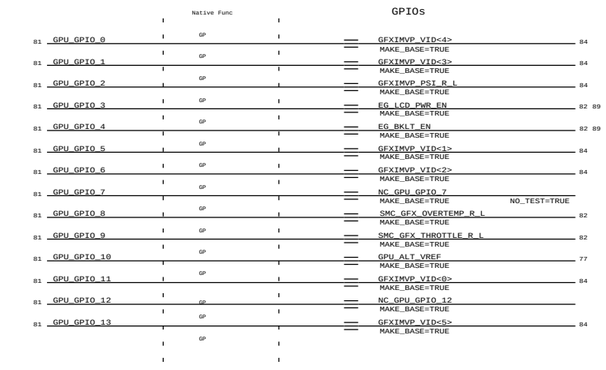
C8582 820PF 10% 25V X7R-CERM 0201

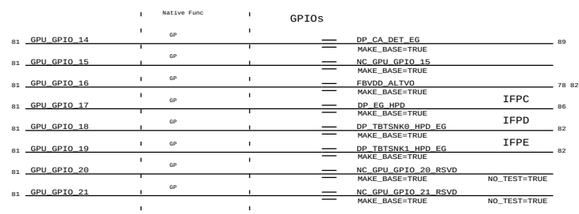
C8583 820PF 10% 25V X7R-CERM 0201

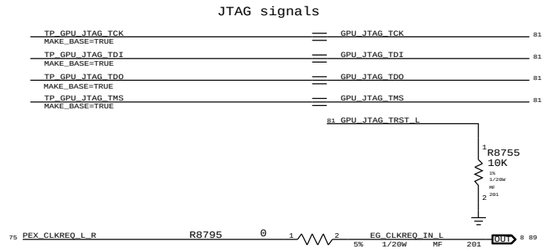
FB_SW_LEG

SYNC_MASTER=J31_SREE	SYNC_DATE=10/25/2013
PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 85 OF 132
	SHEET 80 OF 105









STRAP NOTES:

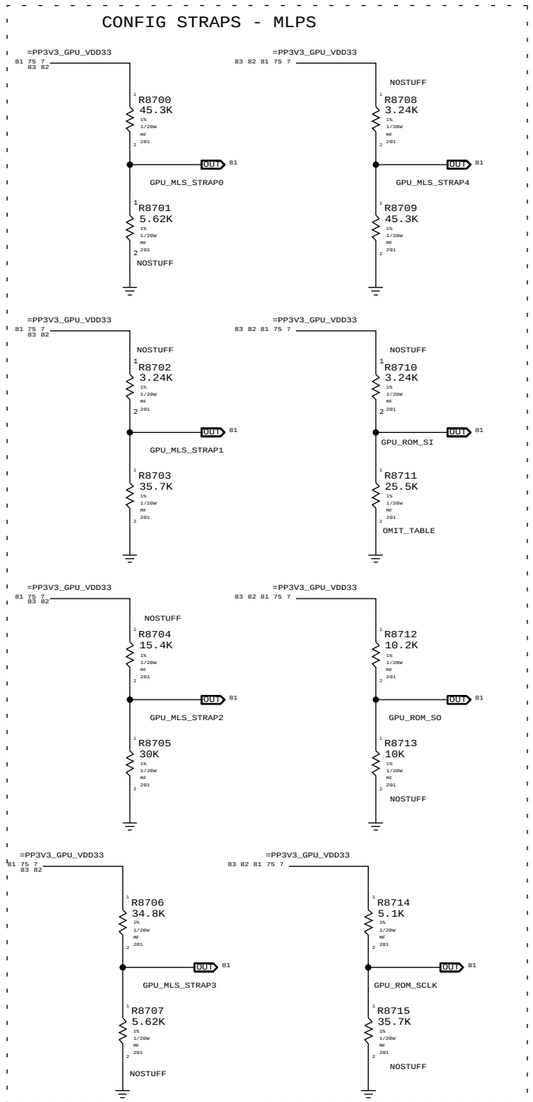
CURRENTLY STUFFED FOR GK107-GTX (R8705)

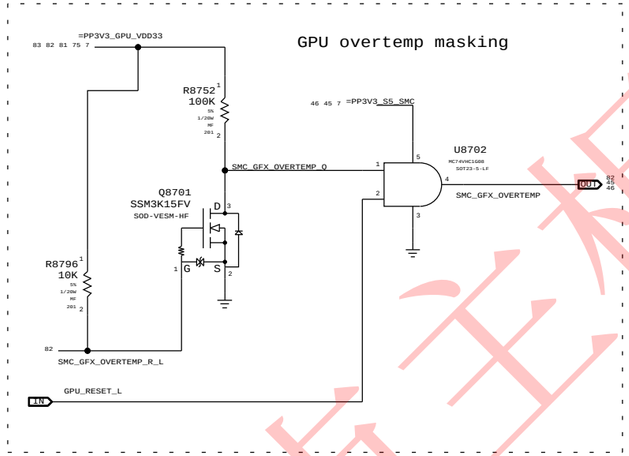
STUFF R8711 = 5KOHM FOR HYNIX 1GB - M die
STUFF R8711 = 10KOHM FOR SAMSUNG 1GB
STUFF R8711 = 15KOHM FOR HYNIX 512MB
STUFF R8711 = 20KOHM FOR SAMSUNG 512MB
STUFF R8711 = 24.9KOHM FOR HYNIX 1GB - A die

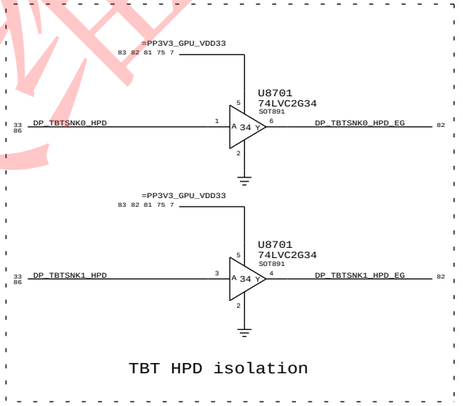
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0019	1	RES, 10.2KOHM, 0201	R8711	CRITICAL	FB_1G_SAMSUNG
118S0414	1	RES, 5.1KOHM, 0201	R8711	CRITICAL	FB_1G_HYNIX_M_DIE
118S0105	1	RES,15KOHM, 0201	R8711	CRITICAL	FB_512_HYNIX
118S0175	1	RES, 20KOHM, 0201	R8711	CRITICAL	FB_512_SAMSUNG
118S0230	1	RES, 24.9KOHM, 0201	R8711	CRITICAL	FB_1G_HYNIX_A_DIE

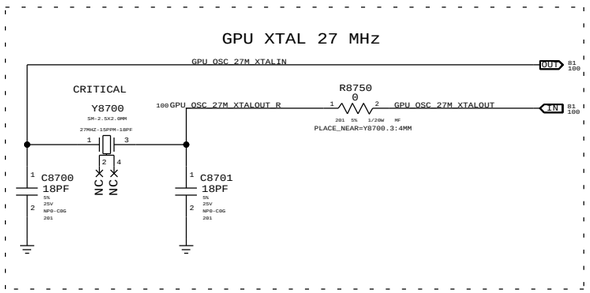
Strap values

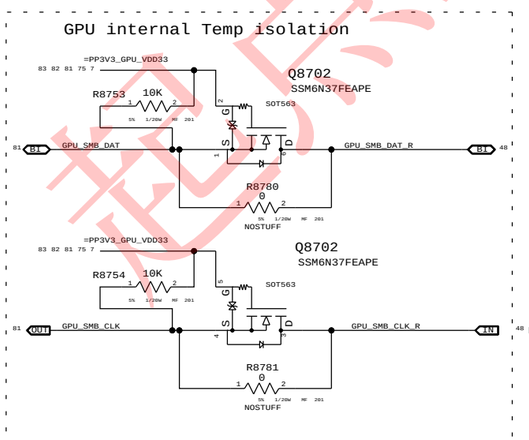
0x01
0x00
0x02
0x03
0x04

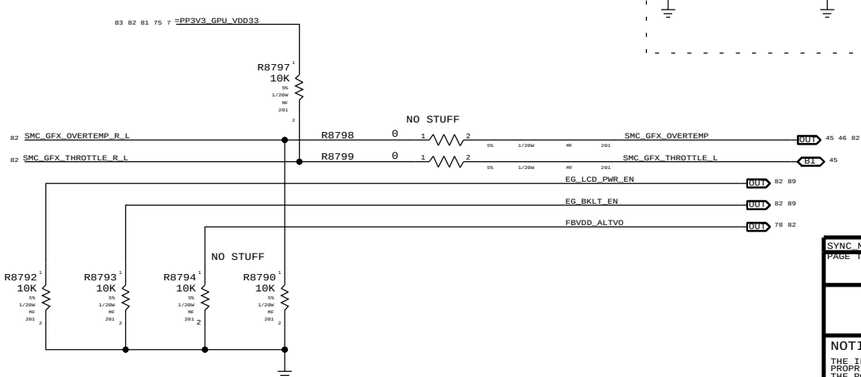












SYNC_MASTER=J31_SREE SYNC_DATE=11/16/2011

PAGE TITLE

KEPLER GPIOS,CLK & STRAPS

Apple Inc.

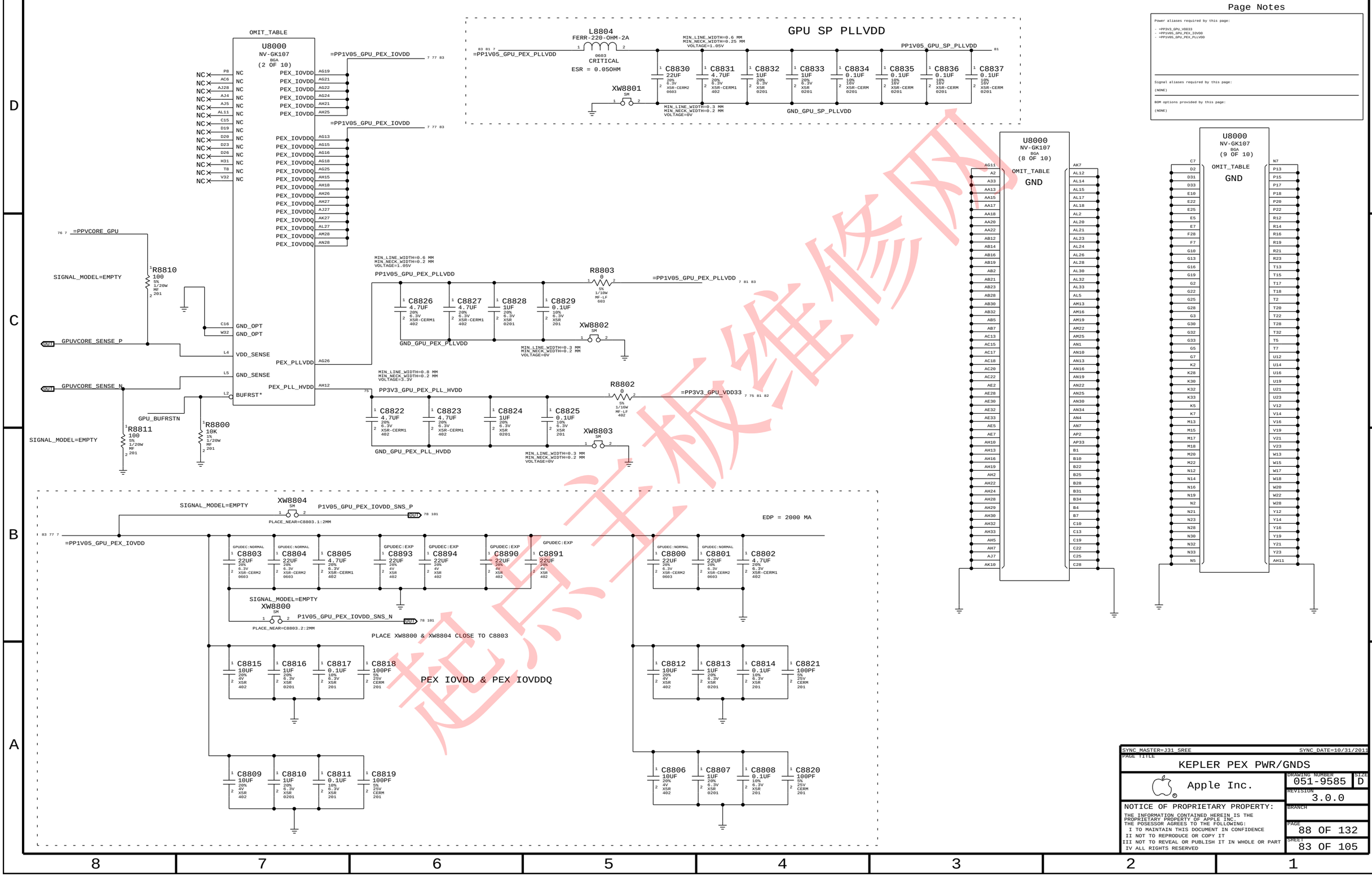
DRAWING NUMBER 051-9585 SIZE D

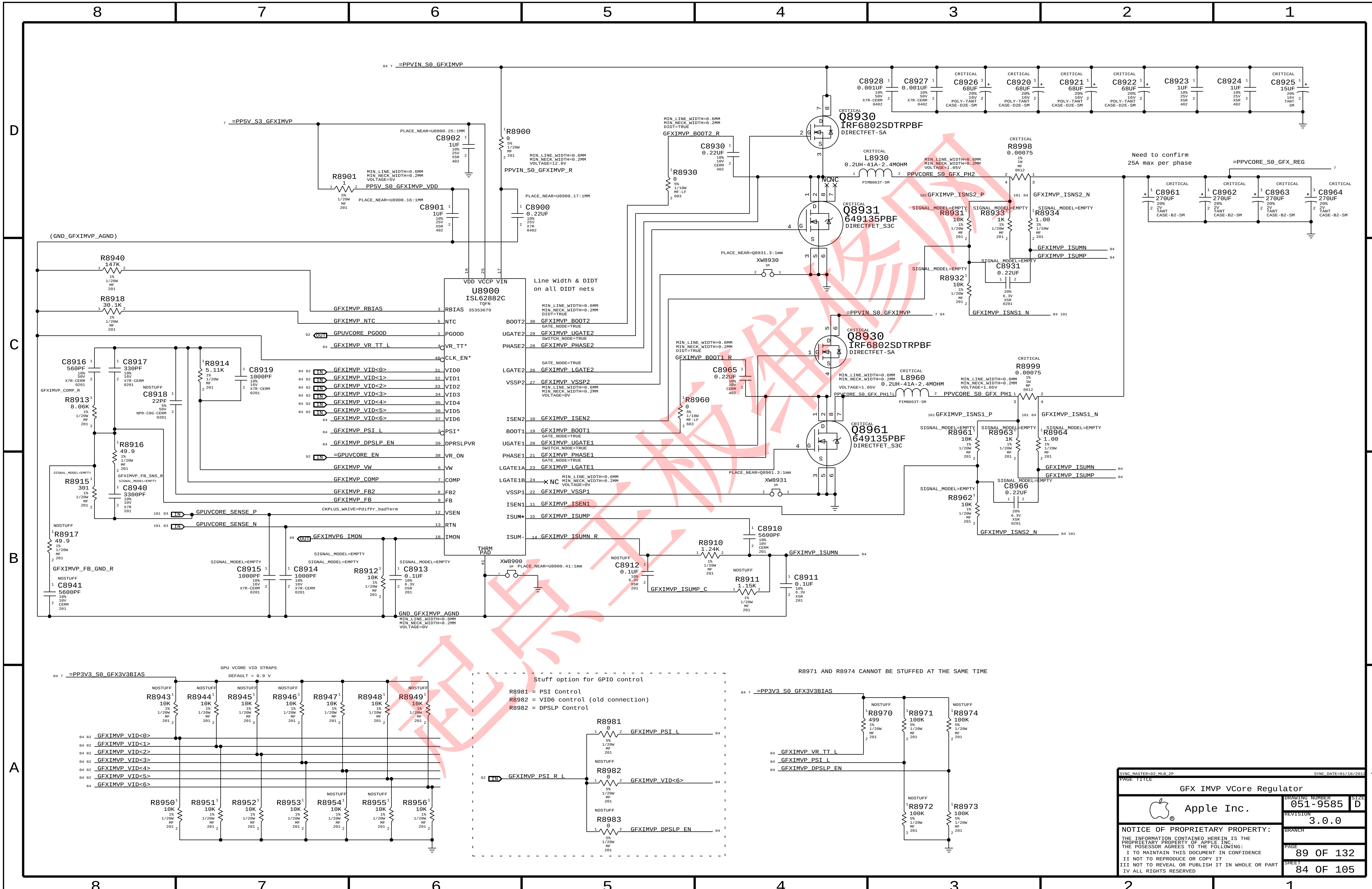
REVISION 3.0.0

BRANCH

PAGE 87 OF 132

SHEET 82 OF 105





GFX IMVP VCore Regulator

Apple Inc.

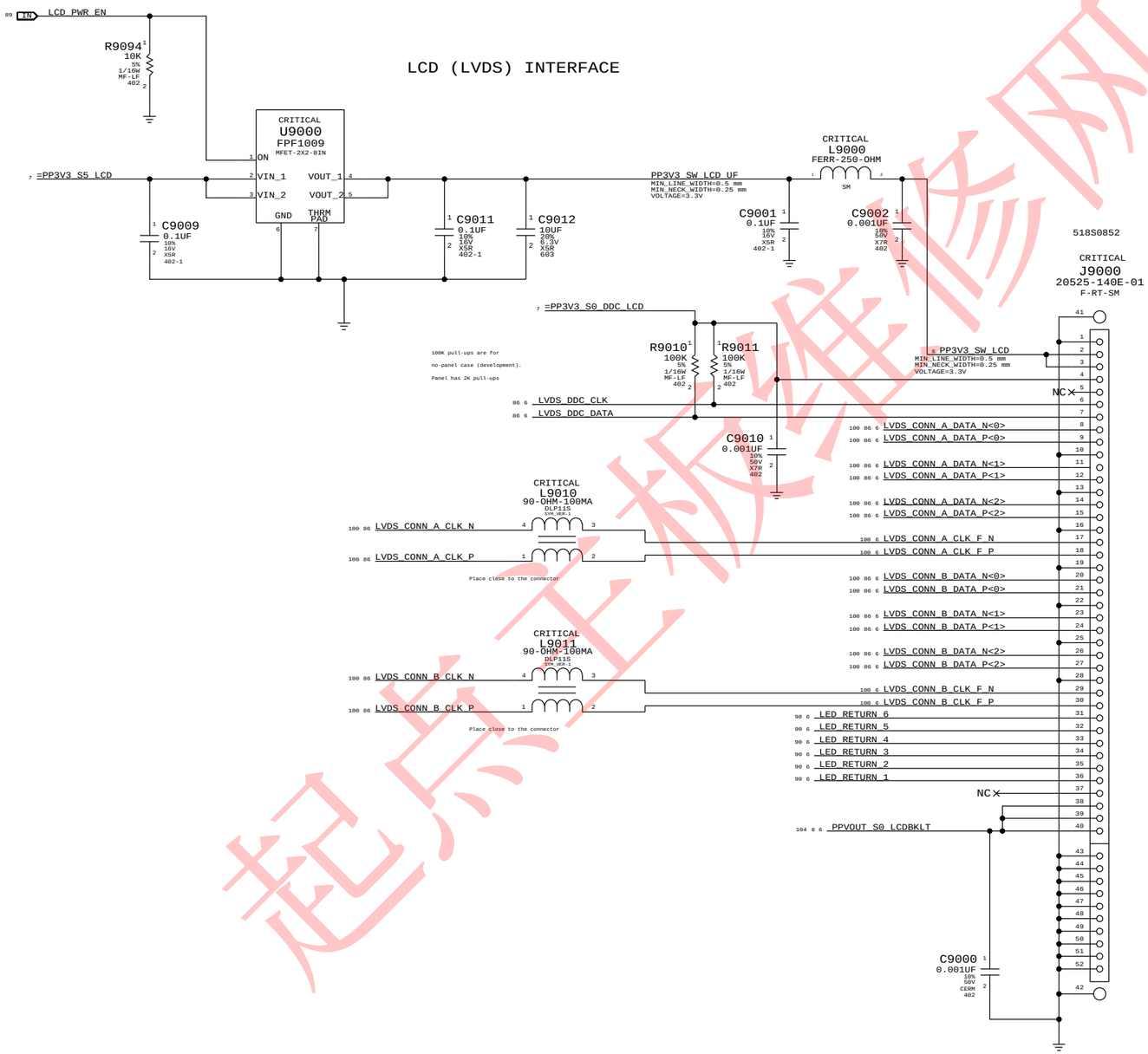
DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

PAGE 89 OF 132

SHEET 84 OF 105

LCD (LVDS) INTERFACE



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

LVDS Display Connector

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 90 OF 132

SHEET 85 OF 105

LVDS Transmitter Termination

All emulated LVDS outputs require this termination

PLACE_NEAR=U9600.A6:7mm
R9220 357 1% 1/20W MF 201
LVDS_A_CLK_P → LVDS_CONN_A_CLK_P

PLACE_NEAR=U9600.A7:7mm
R9222 357 1% 1/20W MF 201
LVDS_A_CLK_N → LVDS_CONN_A_CLK_N

PLACE_NEAR=U9600.A8:7mm
R9225 357 1% 1/20W MF 201
LVDS_A_DATA_P<0> → LVDS_CONN_A_DATA_P<0>

PLACE_NEAR=U9600.B9:7mm
R9227 357 1% 1/20W MF 201
LVDS_A_DATA_N<0> → LVDS_CONN_A_DATA_N<0>

PLACE_NEAR=U9600.A9:7mm
R9230 357 1% 1/20W MF 201
LVDS_A_DATA_P<1> → LVDS_CONN_A_DATA_P<1>

PLACE_NEAR=U9600.C10:7mm
R9232 357 1% 1/20W MF 201
LVDS_A_DATA_N<1> → LVDS_CONN_A_DATA_N<1>

PLACE_NEAR=U9600.B10:7mm
R9235 357 1% 1/20W MF 201
LVDS_A_DATA_P<2> → LVDS_CONN_A_DATA_P<2>

PLACE_NEAR=U9600.A10:7mm
R9237 357 1% 1/20W MF 201
LVDS_A_DATA_N<2> → LVDS_CONN_A_DATA_N<2>

PLACE_NEAR=U9600.C8:7mm
R9240 357 1% 1/20W MF 201
LVDS_B_CLK_P → LVDS_CONN_B_CLK_P

PLACE_NEAR=U9600.C9:7mm
R9242 357 1% 1/20W MF 201
LVDS_B_CLK_N → LVDS_CONN_B_CLK_N

PLACE_NEAR=U9600.A2:7mm
R9245 357 1% 1/20W MF 201
LVDS_B_DATA_P<0> → LVDS_CONN_B_DATA_P<0>

PLACE_NEAR=U9600.A3:7mm
R9247 357 1% 1/20W MF 201
LVDS_B_DATA_N<0> → LVDS_CONN_B_DATA_N<0>

PLACE_NEAR=U9600.A1:7mm
R9250 357 1% 1/20W MF 201
LVDS_B_DATA_P<1> → LVDS_CONN_B_DATA_P<1>

PLACE_NEAR=U9600.B3:7mm
R9252 357 1% 1/20W MF 201
LVDS_B_DATA_N<1> → LVDS_CONN_B_DATA_N<1>

PLACE_NEAR=U9600.C5:7mm
R9255 357 1% 1/20W MF 201
LVDS_B_DATA_P<2> → LVDS_CONN_B_DATA_P<2>

PLACE_NEAR=U9600.A5:7mm
R9257 357 1% 1/20W MF 201
LVDS_B_DATA_N<2> → LVDS_CONN_B_DATA_N<2>

DP AUX, DDC, & HPD muxing to IG/EG

=PP3V3_S0_DPMUX
R9202 10K 5% 1/16W MF-LF 402
C9220 0.1UF 20% 10V CERM 402
C9230 0.1UF 20% 10V CERM 402
VDD
U9220 CBTL03062 BGA

DP_IG_AUX_CH_P	DAUX1+	
DP_IG_AUX_CH_N	DAUX1-	
DP_EG_AUX_CH_P	DAUX2+	CRITICAL
DP_EG_AUX_CH_N	DAUX2-	
DP_IG_DDC_CLK	DDC_CLK1	
DP_IG_DDC_DATA	DDC_DAT1	
DP_EG_DDC_CLK	DDC_CLK2	
DP_EG_DDC_DATA	DDC_DAT2	
DP_IG_HPD	HPD_1	
DP_EG_HPD	HPD_2	
DP_MUX_SEL_EG	GPU_SEL	
DP_MUX_EN	XSD*	

AUX+ ↔ DP_EXTA_AUXCH_C_P
AUX- ↔ DP_EXTA_AUXCH_C_N
DDC_CLK ↔ DP_EXTA_DDC_CLK
DDC_DAT ↔ DP_EXTA_DDC_DATA
HPDIN ← (DP_EXTA_HPD)
GND
R9204 100K 5% 1/16W MF-LF 402
R9205 100K 5% 1/16W MF-LF 402

TBT/DP HOT PLUG IN

T29_DP_HPD:MUX_GMUX
R9206 0 5% 1/16W MF-LF 402
DP_EXTA_HPD
=PP3V3_S0_GMUX
T29_DP_HPD:ALL_OR
C9210 0.1UF 20% 10V CERM 402
CRITICAL
T29_DP_HPD:ALL_OR 74LVC2G32GT SOT833
U9210
DP_TBTSNK0_HPD
DP_TBTSNK1_HPD
TBT_HOTPLUG_DET_OR
T29_DP_HPD:ALL_OR 74LVC2G32GT SOT833
U9210
(DP_EXTA_HPD)
DP_HOTPLUG_DET
T29_DP_HPD:MCU_GMUX
Q9280 SSM3K15FV SOD-VESM-HF
=PP3V3_S0_GMUX
T29_DP_HPD:MCU_GMUX
R9281 100K 5% 1/16W MF-LF 402
DP_A_EXT_HPD

LVDS DDC MUX

=PP3V3_GPU_LVDS_DDC
R9270 20K 5% 1/16W MF-LF 402
R9271 20K 5% 1/16W MF-LF 402
=PP3V3_S0_LVDSDDCMUX
C9270 0.1UF 20% 10V CERM 402
R9272 20K 5% 1/16W MF-LF 402
R9273 20K 5% 1/16W MF-LF 402
VCC
U9270 QFN16
SN74LV4066A

LVDS_DDC_SEL_EG	C1	A1 ↔ LVDS_EG_DDC_CLK
LVDS_DDC_SEL_IG	C2	A2 ↔ LVDS_IG_DDC_CLK
		B2 ↔ LVDS_DDC_CLK
	C3	A3 ↔ LVDS_EG_DDC_DATA
		B3
	C4	A4 ↔ LVDS_IG_DDC_DATA
		B4 ↔ LVDS_DDC_DATA
	GND THRM	

CRITICAL

SYNC_MASTER=K92_MLB SYNC_DATE=11/21/2010
PAGE TITLE: Muxed Graphics Support
Apple Inc.
DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 92 OF 132
SHEET 86 OF 105

TBT A High-Speed Signals

DP_EXTA_ML_C_P<0> C9300 0.1UF DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1UF DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1UF DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1UF DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1UF DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1UF DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1UF DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1UF DP_EXTA_ML_N<3>
(10% 6.3V X5R 201)

DP_EXTA_AUXCH_C_P C9308 0.1uF DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1uF DP_EXTA_AUXCH_N
(10% 16V X5R 402)

R9309 1M (5% MF 1/20W 201) =PP3V3_S0_DPSDRVA
R9308 1M (5% MF 1/20W 201)

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

TBT_A_BIAS0P (VOLTAGE=3.3V) — GND_VOID=TRUE (C9370/C9371)
TBT_D2R_N<0> C9370 0.47UF
TBT_D2R_P<0> C9371 0.47UF
(20% 4V CERM-X5R-1 201)

GND_VOID=TRUE (C9372.1&2)
TBT_R2D_C_N<0> C9372 0.47UF
TBT_R2D_C_P<0> C9373 0.47UF
GND_VOID=TRUE (C9373.1&2)
TBT_A_BIAS0N (VOLTAGE=3.3V)

R9372 1.5K (GND_VOID=TRUE) TBT_R2D_P<0>
R9373 1.5K (GND_VOID=TRUE) TBT_R2D_N<0>
(5% MF 1/20W 201)

TBT signals are P/N-swapped after AC caps to improve layout.

TBT_A_BIAS2P (VOLTAGE=3.3V) — GND_VOID=TRUE (C9380/C9381)
TBT_D2R_N<1> C9380 0.47UF
TBT_D2R_P<1> C9381 0.47UF
GND_VOID=TRUE (C9383.1&2)
TBT_R2D_C_N<1> C9382 0.47UF
TBT_R2D_C_P<1> C9383 0.47UF
GND_VOID=TRUE (C9383.1&2)
TBT_A_BIAS2N (VOLTAGE=3.3V)

R9382 1.5K (GND_VOID=TRUE) TBT_R2D_P<1>
R9383 1.5K (GND_VOID=TRUE) TBT_R2D_N<1>
(5% MF 1/20W 201)

TBT Path Biasing

D9364 BAR90-02LRH (GND_VOID=TRUE (D9364.2))
D9372 BAR90-02LRH
D9373 BAR90-02LRH
D9365 BAR90-02LRH
(TSLP-2-7)
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY

TBT: TX_0
TBT_A_ML_C_P<0> OUT
TBT_A_ML_C_N<0> OUT
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
R9374 1.5K
R9375 1.5K
(5% MF 1/20W 201)

TBT_D2R_C_P<0> TBT_D2R_C_N<0>
TBT_D2R_C_P<1> TBT_D2R_C_N<1>

D9360 BAR90-02LRH (GND_VOID=TRUE (D9360.2))
D9382 BAR90-02LRH
D9383 BAR90-02LRH
D9361 BAR90-02LRH
(TSLP-2-7)
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN
(D9382/D9383)
SIGNAL_MODEL=EMPTY
(D9360/D9361)

TBT: TX_1
TBT_A_ML_C_P<2> OUT
TBT_A_ML_C_N<2> OUT
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
R9384 1.5K
R9385 1.5K
(5% MF 1/20W 201)

DP A Super-Driver

=PP3V3_S0_DPSDRVA
C9310 2.2UF (20% 6.3V CERM 402-LF)
C9311 0.1UF (20% 10V CERM 402)
C9312 0.1UF (20% 10V CERM 402)

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NO STUFF
R9311 1K (5% 1/16W MF-LF 402)
R9310 1K (5% 1/16W MF-LF 402)
R9312 1K (5% 1/16W MF-LF 402)

U9310 PS8301TQFN40GTR-A2 QFN (CRITICAL)

DP_EXTA_ML_P<0>	IN_D0P	OUT_D0P	DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	IN_D0N	OUT_D0N	DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	IN_D1P	OUT_D1P	DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	IN_D1N	OUT_D1N	DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	IN_D2P	OUT_D2P	DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	IN_D2N	OUT_D2N	DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	IN_D3P	OUT_D3P	DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	IN_D3N	OUT_D3N	DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	IN_SCL	AC_AUXP	DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	IN_SDA	AC_AUXN	DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	IN_AUXP	OUT_AUXP_SCL	(DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	IN_AUXN	OUT_AUXN_SDA	(DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	IN_HPD	(IPD) OUT_HPD	DP_SDRVA_HPD
DPSDRVA_I2C_CTL_EN	I2C_CTL_EN (IPU)	CA_DET	DP_A_CA_DET
DPSDRVA_I2C_ADDR0	I2C_ADDR0 (IPD)	CEXT	DPSDRVA_CEXT
DPSDRVA_I2C_ADDR1	I2C_ADDR1 (IPD)		
=I2C_DPSDRVA_SCL	SCL_CTL		
=I2C_DPSDRVA_SDA	SDA_CTL		
DPSDRVA_REXT	REXT		
DP_AUXCH_ISOL	AUXDDC_OFF (IPD)		
DP_A_PWRDWN_R	PD (IPD)		
	GND THMPAD		

PLACE_NEAR=U9310.11:2mm
C9319 2.2UF (20% 6.3V CERM 402-LF)

R9319 value depends on layout. 4.99K is vendor recommendation.

SDRV_PD
R9319 4.99K (1% 1/16W MF-LF 402)
R9318 0 (5% 1/16W MF-LF 402)

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

Port A MCU

DP_A_PWRDWN
=PP3V3_S0_DPSDRVA
See Bill C. for layout-specific guidelines for =DP_A_BIAS.
C9359 0.1UF (10% 16V X5R 402)

CRITICAL U9359 74LVC1G04DBDCK SC70
=DP_A_BIAS
IC supports input high while Vcc = 0V.

=TBT_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#
=TBT_WAKE_L
OMIT R9330 0 (5% 1/16W MF-LF 402)
TBT_A_UC_ADDR

SWCLK
SWDIO
R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

_P3V3_SW_TBTAPWR
Must be 3.3V DP A port power

U9330 LPC1112A HVQFN25 (CRITICAL, OMIT_TABLE)

DP_A_CA_DET	RESET#/PIO0_0	R/PIO1_0/AD1	TBT_A_CONFIG1_RC
TBT_LSEO<0>	PIO0_1/CLKOUT	R/PIO1_1/AD2	TBT_A_CONFIG2_RC
	PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3	TBT_A_HV_EN_R
=I2C_TBTAMCU_SCL	PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4	TBT_A_UC_ADDR
=I2C_TBTAMCU_SDA	PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP	DP_A_EXT_HPD
TBT_A_HPD	PIO0_6/SCK	PIO1_6/RXD	TBT_A_LSX_P2R
=TBT_A_BIAS	PIO0_7/CTS#	PIO1_7/TXD	TBT_A_LSX_R2P
TBT_LSOE<0>	PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0	TBT_LSEO<1>
TBT_LSOE<1>	PIO0_9/MOSI/CT16B0_MAT1		
TBT_PWR_REQ_L	SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)		
	R/PIO0_11/AD0 (OD)	XTALIN	
	VSS THRM PAD		

C9330 0.1UF (20% 10V CERM 402)
C9331 0.1UF (20% 10V CERM 402)
R9335 1K (5% 1/16W MF-LF 402)
R9336 10K (5% 1/16W MF-LF 402)

R9354 30 DP_SDRVA_ML_R_P<0> — C9364 0.22UF (20% 6.3V X5R 0201) — DP_SDRVA_ML_P<0>
R9355 30 DP_SDRVA_ML_R_N<0> — C9365 0.22UF — DP_SDRVA_ML_N<0>
R9350 30 DP_SDRVA_ML_R_P<2> — C9360 0.22UF — DP_SDRVA_ML_P<2>
R9351 30 DP_SDRVA_ML_R_N<2> — C9361 0.22UF — DP_SDRVA_ML_N<2>
(5% MF 1/20W 201)

R9352 270 (5% 1/20W MF 201)
R9353 270 (5% 1/20W MF 201)

C9367 0.1UF DP_SDRVA_ML_P<3>
C9366 0.1UF DP_SDRVA_ML_N<3>
C9363 0.1UF DP_SDRVA_ML_P<1>
C9362 0.1UF DP_SDRVA_ML_N<1>
(10% 6.3V X5R 201)

AUXCH Snoop Port, used by PS8301 during training.
C9369 0.1uF
C9368 0.1uF
(10% 16V X5R 402)

R9392 51 (5% 1/16W MF-LF 402)
R9393 51 (5% 1/16W MF-LF 402)
R9338 10K (5% 1/16W MF-LF 402)
R9334 10K (5% 1/16W MF-LF 402)
TBT_A_HV_EN (OUT 35 88)
I2C Addr: 0x26/0x27 (Wr/Rd)

R9396 1K (5% 1/16W MF-LF 402)
R9397 1K (5% 1/16W MF-LF 402)
DP_A_PWRDWN
=TBT_A_BIAS

R9339 1M (5% 1/16W MF-LF 402)

P2R = Plug to Receptacle
R2P = Receptacle to Plug

DP/TBT A Low-Speed MUX

PP3V3_SW_TBTAPWR
Must be V3P3 output from U9410

C9390 0.1UF (20% 10V CERM 402)
C9391 0.1UF (20% 10V CERM 402)
R9399 100K (5% 1/20W MF 201)

U9390 CBTL04DP081 HVQFN (CRITICAL, OMIT_TABLE)

(DP_SDRVA_ML_N<3>)	DIN1_0+	DOUT_0+	TBT_A_ML_N<3>
(DP_SDRVA_ML_P<3>)	DIN1_0-	DOUT_0-	TBT_A_ML_P<3>
(DP_SDRVA_ML_N<1>)	DIN1_1+	DOUT_1+	TBT_A_ML_N<1>
(DP_SDRVA_ML_P<1>)	DIN1_1-	DOUT_1-	TBT_A_ML_P<1>
DP_SDRVA_AUXCH_P	AUX1+	AUX+	DP_A_EXT_AUXCH_P
DP_SDRVA_AUXCH_N	AUX1-	AUX-	DP_A_EXT_AUXCH_N
(DP_SDRVA_HPD)	HPD_1	HPD_IN	DP_A_EXT_HPD
TBT_A_RSVDN	DIN2_0+		
TBT_A_RSVDP	DIN2_0-		
(TBT_A_LSX_P2R)	DIN2_1+		
(TBT_A_LSX_R2P)	DIN2_1-		
TBT_D2R1_BIASP	AUX2+		
TBT_D2R1_BIASN	AUX2-		
	HPD_2		
DP_A_PWRDWN	GPU_SEL		
=TBT_A_BIAS	AUX_SEL		
	NC		
	THMPAD GND		

R9398 100K (5% 1/20W MF 201)
SIGNAL_MODEL=T29DP_MUX

R9361 1.5K — DP_A_BIAS0 (VOLTAGE=3.3V)
R9360 1.5K
R9365 1.5K — DP_A_BIAS2 (VOLTAGE=3.3V)
R9364 1.5K
(5% MF 1/20W 201)

SYNC_MASTER=J31_WILL	SYNC_DATE=06/20/2013
PAGE TITLE	Thunderbolt MUXing A
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 93 OF 132
	SHEET 87 OF 105

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

=PP3V3_S4_TBTAPWRSW

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S - 9-12.6V, 1W minimum)

CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C9480 22UF 20% 6.3V X5R-CERM-1 603
C9481 0.1UF 20% 10V CERM 402

=PPHV_SW_TBTAPWRSW
20V Max

C9415 4.7UF 10% 25V X5R-CERM 0603
C9410 0.1UF 10% 50V X7R 603-1

U9410 CD3210A0RGP QFN
V3P3 V3P3OUT OUT VHV RSVD RSVD EN ISET_V3P3 HV_EN ISET_S0 S0 ISET_S3 GND THRM PAD

=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN

C9485 0.1UF 20% 10V CERM 402
C9486 10UF 20% 6.3V X5R 603
C9411 0.1UF 10% 50V X7R 603-1

PP3V3_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3

12V: See below

TBTHV:P15V R9410 22.6K 1% 1/16W MF-LF 402 <RHVS3>
TBTHV:P15V R9411 22.6K 1% 1/16W MF-LF 402 <RHVS0>
R9412 36.5K 1% 1/16W MF-LF 402 <RV3P3>

TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R

TBTHV:P15V R9413 22.6K 1% 1/16W MF-LF 402
TBTHV:P15V R9414 22.6K 1% 1/16W MF-LF 402

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0464	1	RES,MTL FILM,1/16W,384K,1,0402,SMD,LF	R9410		TBTHV:P12V
114S0368	1	RES,MTL FILM,1/16W,36.5K,1,0402,SMD,LF	R9411		TBTHV:P12V

	Nominal	Min	Max
IHVS0	1120mA	1090mA	1170mA (12W minimum)
IHVS3	125mA	124mA	126mA (1W minimum)

Thunderbolt Connector A

L9400 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

C9400 0.01UF 10% 50V X7R 402

TBT Dir DP Dir

TBT_D2R_C_P<0>
TBT_D2R_C_N<0>
R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

TBT_A_ML_P<3>
TBT_A_ML_N<3>
Thunderbolt: Unused

TBT_A_BIAS1N VOLTAGE=3.3V
TBT_A_BIAS1P VOLTAGE=3.3V
R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201

TBT_D2R_C_P<1>
TBT_D2R_C_N<1>
D9498 BAR90-02LRH TSLP-2-7 SIGNAL_MODEL=T29PIN
D9499 BAR90-02LRH TSLP-2-7 SIGNAL_MODEL=T29PIN
CRITICAL

CRITICAL L9498 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY
TBT_A_D2R1_AUXCH_P
CRITICAL L9499 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY
TBT_A_D2R1_AUXCH_N

DP_A_EXT_AUXCH_P
DP_A_EXT_AUXCH_N

C9498 30PF 5% 25V C0G-CERM 0201
C9499 30PF 5% 25V C0G-CERM 0201

TBTACONN_20_RC MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18V
R9401 12 5% 1/10W MF-LF 402
C9402 0.01UF 10% 50V X7R 402
C9401 0.01UF 10% 50V X7R 402

R9441 100K 5% 1/10W MF-LF 402

TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC

R9452 1M 5% 1/10W MF-LF 402
R9451 1M 5% 1/10W MF-LF 402
C9494 330PF 10% 50V C0G 402
C9495 330PF 10% 50V C0G 402

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

For J9400 TBT SMT pads (3, 5, 17 & 19):
GND_VOID=TRUE

CRITICAL
J9400 DSPLYPRT-M97-1 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS	
2	HOT_PLUG_DETECT	GND	1
4	CONFIG1	ML_LANE0P	3
6	CONFIG2	ML_LANE0N	5
8	GND	GND	7
10	ML_LANE3P	ML_LANE1P	9
12	ML_LANE3N	ML_LANE1N	11
14	GND	GND	13
16	AUX_CHP	ML_LANE2P	15
18	AUX_CHN	ML_LANE2N	17
20	DP_PWR	RETURN	19
SHIELD PINS			22 21

C9405 0.01UF 10% 50V X7R 402 GND_VOID=TRUE
TBTACONN_1_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V (0-20V)
DP Dir TBT Dir
TBT_A_ML_P<0>
TBT_A_ML_N<0>
TBT: TX_0

C9406 0.01UF 10% 50V X7R 402 GND_VOID=TRUE
TBTACONN_7_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V (0-20V)
TBT_A_ML_P<1>
TBT_A_ML_N<1>
TBT: LSX_R2P/P2R (P/N)

TBT_A_ML_P<2>
TBT_A_ML_N<2>
TBT: TX_1

GND_VOID=TRUE (Both C's)
C9470 0.47UF 20% 4V CERM-XSR-1 201
C9471 0.47UF 20% 4V CERM-XSR-1 201
TBT_A_ML_C_P<0>
TBT_A_ML_C_N<0>
R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201

C9472 0.47UF 20% 4V CERM-XSR-1 201
C9473 0.47UF 20% 4V CERM-XSR-1 201
TBT_A_ML_C_P<2>
TBT_A_ML_C_N<2>
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=T29_REF SYNC_DATE=06/14/2013
PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 94 OF 132
SHEET 88 OF 105

GMUX CPLD

R9600 0 5% 1/10W MF-LF 402 — =PP3V3_S0_GMUX

C9610 0.1UF 10% 6.3V X5R 201
C9621 0.1UF 10% 6.3V X5R 201
C9622 0.1UF 10% 6.3V X5R 201
C9623 0.1UF 10% 6.3V X5R 201
C9624 0.1UF 10% 6.3V X5R 201
C9625 0.1UF 10% 6.3V X5R 201
C9626 0.1UF 10% 6.3V X5R 201
C9627 0.1UF 10% 6.3V X5R 201
C9628 0.1UF 10% 6.3V X5R 201
C9629 0.1UF 10% 6.3V X5R 201

PP3V3_S0_GMUX_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

R9610 0 5% 1/10W MF-LF 402 — =PP1V8_S0_GMUX

C9611 0.1UF 10% 6.3V X5R 201
C9612 0.1UF 10% 6.3V X5R 201
C9613 0.1UF 10% 6.3V X5R 201
C9614 0.1UF 10% 6.3V X5R 201
C9615 0.1UF 10% 6.3V X5R 201
C9616 0.1UF 10% 6.3V X5R 201
C9617 0.1UF 10% 6.3V X5R 201

PP1V8_S0_GMUX_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=1.8V

=PP1V2_S0_GMUX

C9600 4.7UF 20% 4V X5R-1 402
C9604 0.1UF 10% 6.3V X5R 201
C9605 0.1UF 10% 6.3V X5R 201
C9606 0.1UF 10% 6.3V X5R 201
C9607 0.1UF 10% 6.3V X5R 201
C9608 0.1UF 10% 6.3V X5R 201
C9609 0.1UF 10% 6.3V X5R 201

PP3V3_S0_GMUX_ULC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

L9621 FERR-220-OHM 0402
C9631 0.1UF 10% 6.3V X5R 201

PP3V3_S0_GMUX_LRC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

L9620 FERR-220-OHM 0402
C9630 0.1UF 10% 6.3V X5R 201

=PP3V3_S0_GMUX

R9645 10K 1% 1/20W MF 201
R9640 10K 1% 1/20W MF 201

NO STUFF
R9646 10K 1% 1/20W MF 201
R9641 10K 1% 1/20W MF 201

VCC: C4, J3, J13, N11, P8
VCCAUX: C11, J2, J14, M8
VCCIO0: B5
VCCIO1: B7
VCCIO2: A12
VCCIO3: C14
VCCIO4: F13
VCCIO5: M12
VCCIO6: M9
VCCIO7: M3, N5, M1, C3, F2
VCCJ: K12
ULC_VCCPLL: A4
LRC_VCCPLL: P11

OMIT
CRITICAL

U9600
XP25-5
CSBGA

JTAG_GMUX_TCK		K14	TCK	
JTAG_GMUX_TDI		L13	TDI	
JTAG_GMUX_TDO		K13	TDO	
JTAG_GMUX_TMS		L12	TMS	
GMUX_TOE		K2	TOE	
GMUX_CFG0		K1	CFG0	
LCD_BKLT_EN	OUT	P2	PB7A	BANK5
LCD_BKLT_PWM	OUT	N2	PB7B	BANK5
LVDS_DDC_SEL_EG	OUT	P4	PB14A	BANK5
LVDS_DDC_SEL_IG	OUT	N4	PB14B	BANK5
DP_MUX_EN	OUT	N3	PB15A(OD)	BANK5
DP_MUX_SEL_EG	OUT	M4	PB15B	BANK5
EG_RESET_L	OUT	P5	PB16A	BANK5
EG_RAIL1_EN	OUT	M5	PB16B	BANK5
EG_RAIL2_EN	OUT	P6	PB17A	BANK5
EG_RAIL3_EN	OUT	M6	PB17B	BANK5
EG_RAIL4_EN	OUT	P7	PB18A	BANK5
EG_CLKREQ_OUT_L	OUT	M7	PB18B(OD)	BANK5
DP_CA_DET_EG	OUT	N7	PB19A	BANK5
LCD_PWR_EN	OUT	N8	PB19B	BANK5
LPC_AD<0>	BI	P9	PB20A	BANK4
LPC_AD<1>	BI	N9	PB20B	BANK4
LPC_AD<2>	BI	P10	PB26A	BANK4
LPC_AD<3>	BI	M10	PB26B	BANK4
LPC_FRAME_L	BI	P12	PB27A	BANK4
LPC_RESET_L	IN	P13	PB27B	BANK4
LPC_CLK33M_GMUX	IN	N12	PB28A	BANK4
GMUX_INT	OUT	P14	PB28B	BANK4
LVDS_IG_B_DATA_P<2>	IN	B1	PL2A	BANK7
LVDS_IG_B_DATA_N<2>	IN	B2	PL2B	BANK7
GMUX_PL6A		C2	PL6A	BANK7
TP_GMUX_PL6B		D3	PL6B	BANK7
LVDS_IG_A_DATA_P<0>	IN	D1	PL7A	BANK7
LVDS_IG_A_DATA_N<0>	IN	E1	PL7B	BANK7
LVDS_IG_A_DATA_P<1>	IN	D2	PL8A	BANK7
LVDS_IG_A_DATA_N<1>	IN	E3	PL8B	BANK7
LVDS_IG_A_DATA_P<2>	IN	F1	PL9A	BANK7
LVDS_IG_A_DATA_N<2>	IN	G1	PL9B	BANK7
LVDS_IG_B_DATA_P<0>	IN	F3	PL10A	BANK7
LVDS_IG_B_DATA_N<0>	IN	G2	PL10B	BANK7
LVDS_IG_B_DATA_P<1>	IN	H2	PL11A	BANK7
LVDS_IG_B_DATA_N<1>	IN	G3	PL11B	BANK7
LVDS_IG_A_CLK_P	IN	H1	PL12A	BANK7
LVDS_IG_A_CLK_N	IN	H3	PL12B	BANK7
LVDS_MUX_SEL_EG	OUT	L1	PL14A	BANK6
TP_GMUX_PL14B		L3	PL14B	BANK6
=GMUX_PCIE_RESET_L	IN	K3	PL15A	BANK6
TP_GMUX_PL15B		L2	PL15B	BANK6
ALL_EG_PGOOD	IN	N1	PL25A	BANK6
EG_CLKREQ_IN_L	IN	P1	PL25B	BANK6

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

LVDS_B_DATA_P<0>	OUT	A2	PT7A	BANK0
LVDS_B_DATA_N<0>	OUT	A3	PT7B	BANK0
LVDS_B_DATA_P<1>	OUT	A1	PT8A	BANK0
LVDS_B_DATA_N<1>	OUT	B3	PT8B	BANK0
LVDS_B_DATA_P<2>	OUT	C5	PT9A	BANK0
LVDS_B_DATA_N<2>	OUT	A5	PT9B	BANK0
EG_PWRSEQ_EN	IN	B6	PT14A	BANK0
GMUX_DEBUG_RESET_L	IN	C7	PT14B	BANK0
LVDS_A_CLK_P	OUT	A6	PT15A	BANK0
LVDS_A_CLK_N	OUT	A7	PT15B	BANK0
LVDS_B_CLK_P	OUT	C8	PT16A	BANK0
LVDS_B_CLK_N	OUT	C9	PT16B	BANK0
LVDS_A_DATA_P<0>	OUT	A8	PT17A	BANK0
LVDS_A_DATA_N<0>	OUT	B9	PT17B	BANK0
LVDS_A_DATA_P<1>	OUT	A9	PT18A	BANK0
LVDS_A_DATA_N<1>	OUT	C10	PT18B	BANK0
LVDS_A_DATA_P<2>	OUT	B10	PT19A	BANK0
LVDS_A_DATA_N<2>	OUT	A10	PT19B	BANK0
TP_GMUX_PT20A		A11	PT20A	BANK0
TP_GMUX_PT20B		B12	PT20B	BANK1
TP_GMUX_PT32A		B13	PT28A	BANK1
TP_GMUX_PT32B		A13	PT28B	BANK1
DP_A_CA_DET	IN	A14	PR2A	BANK1
DP_HOTPLUG_DET	IN	B14	PR2B	BANK1
LVDS_EG_A_DATA_P<0>	IN	D12	PR6A	BANK2
LVDS_EG_A_DATA_N<0>	IN	D13	PR6B	BANK2
LVDS_EG_A_DATA_P<1>	IN	D14	PR7A	BANK2
LVDS_EG_A_DATA_N<1>	IN	E14	PR7B	BANK2
LVDS_EG_A_DATA_P<2>	IN	E12	PR8A	BANK2
LVDS_EG_A_DATA_N<2>	IN	F12	PR8B	BANK2
LVDS_EG_B_DATA_P<0>	IN	F14	PR9A	BANK2
LVDS_EG_B_DATA_N<0>	IN	G14	PR9B	BANK2
LVDS_EG_B_DATA_P<1>	IN	G12	PR10A	BANK2
LVDS_EG_B_DATA_N<1>	IN	G13	PR10B	BANK2
LVDS_EG_B_DATA_P<2>	IN	H13	PR11A	BANK2
LVDS_EG_B_DATA_N<2>	IN	H12	PR11B	BANK2
LVDS_EG_A_CLK_P	IN	H14	PR12A	BANK2
LVDS_EG_A_CLK_N	IN	J12	PR12B	BANK2
IG_LCD_PWR_EN	IN	L14	PR14A	BANK3
EG_LCD_PWR_EN	IN	M13	PR14B	BANK3
IG_BKLT_EN	IN	N14	PR24A	BANK3
EG_BKLT_EN	IN	N13	PR24B	BANK3

GND: J1, B9, C6, C12, C13, E13, M14, N10, N6, P3, M2, C1, E2, B4, M11
GNDIO0, GNDIO1, GNDIO2, GNDIO3, GNDIO4, GNDIO5, GNDIO6, GNDIO7, ULC_GNDPLL, LRC_GNDPLL

CRITICAL
J9600 1909782 M-RT-SM — GMUX_JTAG_CONN

1	=PP3V3_S0_GMUX	7 86 89
2	JTAG_GMUX_TDO	89
3	JTAG_GMUX_TDI	89
4	JTAG_GMUX_TMS	18 89
5		
6	JTAG_GMUX_TCK	8 89
7		
8		

NO STUFF
R9647 10K 1% 1/20W MF 201

=PP3V3_T29_JTAG — R9605 1K 1% 1/20W MF 201 — T29_JTAG_FET

JTAG_GMUX_TDI → SSM6N37FEAPE Q9605 SOT563 → JTAG_ISP_TDI
JTAG_GMUX_TDO → SSM6N37FEAPE Q9605 SOT563 → JTAG_ISP_TDO

=PP3V3_S3_GMUX — R9676 100K 5% 1/20W MF 201 — GMUX_S3_PD_EN
SSM6N37FEAPE Q9607 SOT563

ALL_SYS_PWRGD

LVDS Receiver Termination

LVDS_IG_A_CLK_P	R9650	100	PLACE_NEAR=U9600.H3:5mm	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>	R9651	100	PLACE_NEAR=U9600.E1:5mm	LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>	R9652	100	PLACE_NEAR=U9600.E3:5mm	LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>	R9653	100	PLACE_NEAR=U9600.G1:5mm	LVDS_IG_A_DATA_N<2>
LVDS_IG_B_DATA_P<0>	R9654	100	PLACE_NEAR=U9600.G2:5mm	LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>	R9655	100	PLACE_NEAR=U9600.G3:5mm	LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>	R9656	100	PLACE_NEAR=U9600.B2:5mm	LVDS_IG_B_DATA_N<2>
LVDS_EG_A_CLK_P	R9660	100	PLACE_NEAR=U9600.J12:5mm	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>	R9661	100	PLACE_NEAR=U9600.D13:5mm	LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>	R9662	100	PLACE_NEAR=U9600.E14:5mm	LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>	R9663	100	PLACE_NEAR=U9600.E12:5mm	LVDS_EG_A_DATA_N<2>
LVDS_EG_B_DATA_P<0>	R9664	100	PLACE_NEAR=U9600.G14:5mm	LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>	R9665	100	PLACE_NEAR=U9600.G13:5mm	LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>	R9666	100	PLACE_NEAR=U9600.H12:5mm	LVDS_EG_B_DATA_N<2>

SIGNAL_MODEL=EMPTY

Required Pullups

=PP3V3_S0_GMUX

EG_PWRSEQ_EN	R9684	1K	5% 1/20W MF 201
JTAG_GMUX_TDI	R9685	10K	5% 1/20W MF 201
JTAG_GMUX_TDO	R9686	10K	5% 1/20W MF 201
GMUX_DEBUG_RESET_L	R9680	1K	5% 1/20W MF 201

NO STUFF
R9679 10K 5% 1/20W MF 201
SILK_PART=GMUX_RST

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K	5% 1/20W MF 201
LVDS_DDC_SEL_IG	R9682	10K	5% 1/20W MF 201
LVDS_DDC_SEL_EG	R9683	10K	5% 1/20W MF 201

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

NO STUFF
EG_RESET_L — R9691 100K 5% 1/20W MF 201
LCD_BKLT_PWM — R9693 100K 5% 1/20W MF 201

EG_RAIL4_EN — R9674 4.7K 5% 1/20W MF 201
EG_RAIL3_EN — R9673 4.7K 5% 1/20W MF 201
EG_RAIL2_EN — R9672 4.7K 5% 1/20W MF 201
EG_RAIL1_EN — R9671 4.7K 5% 1/20W MF 201
LCD_PWR_EN — R9678 4.7K 5% 1/20W MF 201

GMUX_S3_PD_GND

NO STUFF
R9675 0 5% 1/20W MF 201

SSM6N37FEAPE Q9607 SOT563

SYNC_MASTER=K91_MARY SYNC_DATE=08/03/2010

PAGE TITLE: Graphics MUX (GMUX)

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 96 OF 132
SHEET: 89 OF 105

PPBUS S0 LCDBKLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)

F9700 3AMP-32V-467 603-HF BOTTOM

CRITICAL Q9706 FDC638APZ_SBMS001 SSOT6-HF

=PPBUS_S0_LCDBKLT → PPBUS_S0_LCDBKLT_FUSED (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V)

PPBUS_SW_LCDBKLT_PWR (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V) 90 104

THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

R9788 301K 1% 1/16W MF-LF 402 — C9782 0.1UF 10% 16V X5R 402

LCDBKLT_EN_DIV

R9789 147K 1% 1/16W MF-LF 402

LCDBKLT_EN_L

Q9707 SSM6N15AFE SOT563 — LCD_BKLT_EN

LCDBKLT_DISABLE

Q9707 SSM6N15AFE SOT563 — BKLT_PLT_RST_L

*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

=PP5V_S0_BKL

=PPBUS_SW_BKL

CRITICAL L9701 33UH-1.8A-110MOHM 1217AS-2SM

PPBUS_SW_LCDBKLT_PWR_SW (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=40V, SWITCH_NODE=TRUE, DIDT=TRUE)

CRITICAL D9701 SOD-123 RB160M-60G

PPVOUT_SW_LCDBKLT (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=50V)

C9796 220PF 10% 50V X7R-CERM 402 — CRITICAL C9797 10UF 10% 50V X5R 1210-1 — CRITICAL C9799 10UF 10% 50V X5R 1210-1

CRITICAL C9712 10UF 10% 25V X5R 805 — C9713 0.1UF 10% 25V X5R 402

C9710 1UF 10% 25V X5R 603-1 — C9714 0.01UF 10% 16V CERM 402

XW9720 SM

PPVOUT_SW_LCDBKLT_FB VOLTAGE=40V (MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.25 MM)

=PP3V3_S0_BKL_VDDIO

C9711 0.1UF 10% 16V X5R 402

R9755 10K 5% 1/16W MF-LF 402 (MIN_LINE_WIDTH=0.075 mm, MIN_NECK_WIDTH=0.075 mm)

R9741 10K 5% 1/16W MF-LF 402 (MIN_LINE_WIDTH=0.075 mm, MIN_NECK_WIDTH=0.075 mm)

R9753 0 5% 1/16W MF-LF 402

R9757 0 5% 1/16W MF-LF 402

Addr: 0x58(Wr)/0x59(Rd)

=I2C_BKL_1_SCL

=I2C_BKL_1_SDA

PPBUS_SW_LCDBKLT_PWR

R9731 301K 1% 1/16W MF-LF 402 — R9715 100K 1% 1/16W MF-LF 402

R9704 33 5% 1/16W MF-LF 402 — LCD_BKLT_PWM

C9704 33PF 5% 50V C0GM 402

TP_BKL_FAULT PLACE_SIDE=BOTTOM

U9701 25-BUMP-MICRO LP8550

VDDIO	C4	VLDO	D1
VIN	C1	VSYNC	D2
FILTER	C2	ISET	B3
FSET	B4	SCLK	D3
SDA	D4	PWM	A4
EN	A3	FAULT	C3
SW_0	B1	SW_1	B2
FB	A5	OUT1	E5
OUT2	D5	OUT3	C5
OUT4	E3	OUT5	E2
OUT6	E1	GND_S	B5
GND_L	E4	GND_SW	A1
GND_SW	A2		

BKL_VSYNC_R, BKL_FLTR, BKL_ISET, BKL_FSET, BKL_SCL, BKL_SDA, BKL_PWM, BKL_EN

BKL_ISEN1 … BKL_ISEN6

CRITICAL

I_LED=22.7mA

R9716 90.9K 1% 1/16W MF-LF 402 — R9714 16.2K 1% 1/16W MF-LF 402

Fpwm=9.62kHz
see spec for others

I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

GND_BKL_SGND (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V)

XW9710 SM

PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)

BKLT:PROD

R9717 0 5% 1/16W MF-LF 402 — LED_RETURN_1

R9718 0 — LED_RETURN_2

R9719 0 — LED_RETURN_3

R9720 0 — LED_RETURN_4

R9721 0 — LED_RETURN_5

R9722 0 — LED_RETURN_6

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SMR	9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SMR	9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=J31_KIRAN SYNC_DATE=03/21/2011

PAGE TITLE: LCD Backlight Driver

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

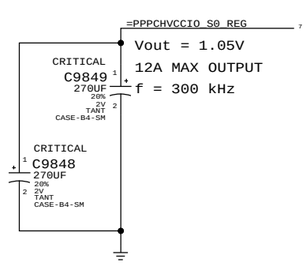
REVISION: 3.0.0

BRANCH:

PAGE: 97 OF 132

SHEET: 90 OF 105

PCH VCCIO (1.05V S0) REGULATOR



SYNC_MASTER=J31_JACK SYNC_DATE=09/16/2011

PAGE TITLE

PCH VCCIO (1.05V) POWER SUPPLY

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 98 OF 132

SHEET 91 OF 105

GPU Rail Sequencing

KEPLER GPU REQUIRES RAILS TO COME
up in the following order:

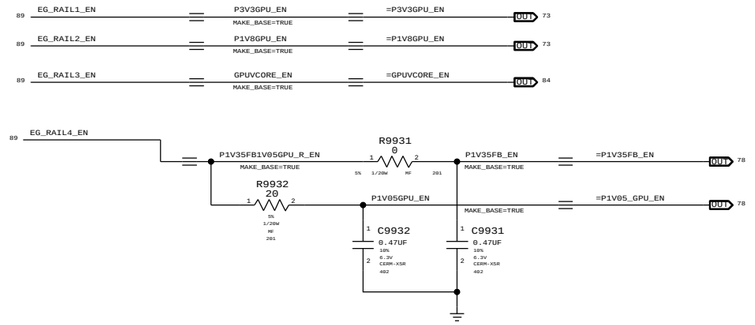
1) GPU_3.3V

2) IFPX IOVDD - 1.8V

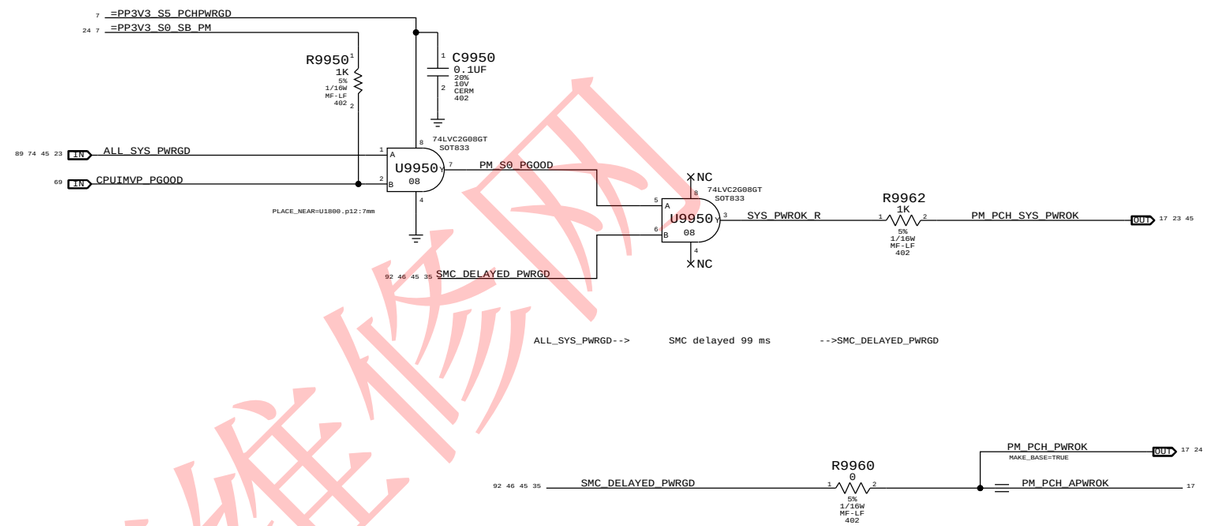
3) GPUVCORE

4) FBVDDQ/GDDR5 1.35V

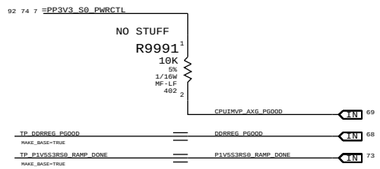
5) PEXVDD/Q OR IFPY IOVDD - 1.05V



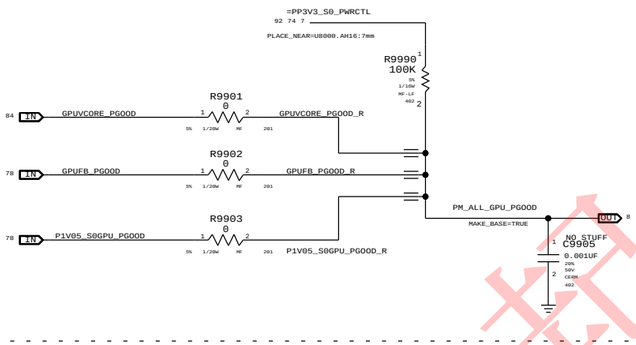
PCH S0 PWRGD



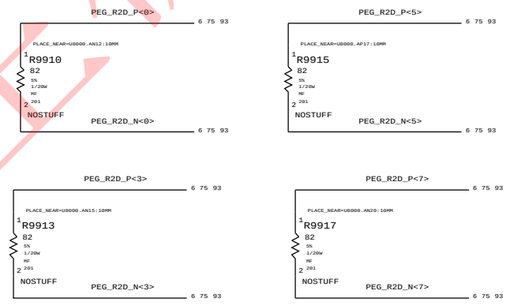
Unused PGOOD signal



EXT GPU PWRGD Pullup



PCIE TEST STRUCTURES (FOR LAB USE)



SYNC_MASTER=J31_SREE SYNC_DATE=09/19/2011

PAGE TITLE

Power Sequencing EG/PCH S0

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 99 OF 132

SHEET 92 OF 105

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	15 MIL	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	15 MIL	?

PEG

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_RXRX	*	=3X_DIELECTRIC	?
PEG_TXTX	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_D2R	PEG_D2R	*	PEG_RXRX
PEG_R2D	PEG_R2D	*	PEG_TXTX
PEG_D2R	PEG_R2D	*	PEG_TXRX

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	6 9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	6 9 17
FDI_FSYNC	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	6 9 17
FDI_LSYNC	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	6 9 17
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	6 9 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
	DP_85D	DISPLAYPORT	DP_INT_IG_ML_P<3:0>	8 9
	DP_85D	DISPLAYPORT	DP_INT_IG_ML_N<3:0>	8 9
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_P	8 9
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_N	8 9
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_COMP	9
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	9 23
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKP	8
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKN	8
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	10 23
XDP_RESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 24
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10 45
CPU_PROC_SEL_L	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	10 19
CPU_PECI	CPU_50S	CPU_VID	CPU_PECI	10 19 46
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 45 46 69
XDP_CPU_PWRGD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	23
PM_THRMTRIP_L	CPU_50S	CPU_BMIL	PM_THRMTRIP_L	10 19 46
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	10
	CPU_50S	CPU_VID	CPU_VIDSOUT	12 69
	CPU_50S	CPU_VID	CPU_VIDSCLK	12 69
	CPU_50S	CPU_VID	CPU_VIDALERT_L	12 69
	CPU_55S	CPU_VID	CPU_VCCSA_VID<1..0>	12 66
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCCSENSE_P	12 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCCSENSE_N	12 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCCIOSENSE_P	12 71
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCCIOSENSE_N	12 71
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_AXG_SENSE_P	12 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_AXG_SENSE_N	12 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCC_VALSENSE_P	12
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCC_VALSENSE_N	12
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_AXG_VALSENSE_P	12
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_AXG_VALSENSE_N	12
CPU_VCCSASENSE	CPU_50S	CPU_AGTL	CPU_VCCSASENSE	12 66
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_A	9 31
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_B	9 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_A	27 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	29 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_A	27 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	29 31
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	PEG_80D	PEG_R2D	PEG_R2D_P<7..0>	6 75 92
	PEG_80D	PEG_R2D	PEG_R2D_N<7..0>	6 75 92
PEG_R2D	PEG_80D	PEG_R2D	PEG_R2D_C_P<7..0>	8 75
	PEG_80D	PEG_R2D	PEG_R2D_C_N<7..0>	8 75
PEG_D2R	PEG_80D	PEG_D2R	PEG_D2R_P<7..0>	8 75
	PEG_80D	PEG_D2R	PEG_D2R_N<7..0>	8 75
	PEG_80D	PEG_D2R	PEG_D2R_C_P<7..0>	6 75
	PEG_80D	PEG_D2R	PEG_D2R_C_N<7..0>	6 75

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

PAGE TITLE: CPU Constraints

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 100 OF 132
SHEET: 93 OF 105

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_*	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_*	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_*	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	*	*	MEM_2OTHER

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 6 11 27
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 6 11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 6 11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0> 6 11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0> 6 11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 6 11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 6 11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 6 11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 6 11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 6 11 27
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 6 11 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 6 11 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 6 11 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 6 11 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 6 11 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 6 11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 6 11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 6 11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 6 11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 6 11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 6 11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 6 11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 6 11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 6 11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 6 11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 6 11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 6 11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 6 11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 6 11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 6 11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 6 11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 6 11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 6 11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 6 11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 6 11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 6 11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0> 6 11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 6 11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0> 6 11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 6 11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 6 11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 6 11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 6 11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 6 11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 6 11 28
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 6 11 28
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 6 11 28
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 6 11 28
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 6 11 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 6 11 28
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 6 11 28
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 6 11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 6 11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 6 11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 6 11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 6 11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 6 11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 6 11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 6 11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 6 11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 6 11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 6 11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 6 11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 6 11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 6 11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 6 11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 6 11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 6 11 28

SYNC_MASTER=K91_MLB SYNC_DATE=06/25/2011

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 101 OF 132
SHEET 94 OF 105

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	1in,3,1in,4,,1in,9,,1in,10	=4:1_SPACING	?
LVDS	1in,3,,1in,4,,1in,9,,1in,10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D_ALT	*	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+

USB 3.0 Interface Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	*	=5:1_SPACING	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P 8 86
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N 8 86
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P 17 89
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N 17 89
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0> 17 89
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0> 17 89
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<3> 8 17
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<3> 8 17
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0> 17 89
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0> 17 89
	SATA_90D_ALT	SATA	SATA_HDD_R2D_C_P 16 41
	SATA_90D_ALT	SATA	SATA_HDD_R2D_C_N 16 41
	SATA_90D_ALT	SATA	SATA_HDD_R2D_RC_P 41
	SATA_90D_ALT	SATA	SATA_HDD_R2D_RC_N 41
1219 SATA_HDD_R2D	SATA_90D_ALT	SATA	SATA_HDD_R2D_P 6 41
1218	SATA_90D_ALT	SATA	SATA_HDD_R2D_N 6 41
SATA_HDD_D2R	SATA_90D_ALT	SATA	SATA_HDD_D2R_P 16 41
	SATA_90D_ALT	SATA	SATA_HDD_D2R_N 16 41
	SATA_90D_ALT	SATA	SATA_HDD_D2R_C_P 6 41
	SATA_90D_ALT	SATA	SATA_HDD_D2R_C_N 6 41
1220	SATA_90D_ALT	SATA	SATA_HDD_D2R_RC_P 41
1219	SATA_90D_ALT	SATA	SATA_HDD_D2R_RC_N 41
1249	SATA_90D_ALT	SATA	SATA_HDD_R2D_RDROUT_P 41
1241	SATA_90D_ALT	SATA	SATA_HDD_R2D_RDROUT_N 41
1246	SATA_90D_ALT	SATA	SATA_HDD_D2R_RDRIN_P 41
1247	SATA_90D_ALT	SATA	SATA_HDD_D2R_RDRIN_N 41
1248	SATA_90D_ALT	SATA	SATA_HDD_D2R_RDROUT_P 41
1240	SATA_90D_ALT	SATA	SATA_HDD_D2R_RDROUT_N 41
1250	SATA_90D_ALT	SATA	SATA_HDD_R2D_RDRIN_P 41
1251	SATA_90D_ALT	SATA	SATA_HDD_R2D_RDRIN_N 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P 16 41
	SATA_90D	SATA	SATA_ODD_R2D_C_N 16 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P 6 41
	SATA_90D	SATA	SATA_ODD_R2D_N 6 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P 16 41
	SATA_90D	SATA	SATA_ODD_D2R_N 16 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_C_P 6 41
	SATA_90D	SATA	SATA_ODD_D2R_C_N 6 41
1243 PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP 16
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP 16
USB_EXTA	USB_85D	USB	USB_EXTA_P 18 42
	USB_85D	USB	USB_EXTA_N 18 42
USB_EXTB_MUX	USB_85D	USB	USB_EXTB_MUX_P 25 43
USB_EXTB_MUX	USB_85D	USB	USB_EXTB_MUX_N 25 43
USB_EXTC	USB_85D	USB	USB_EXTC_P 8 18
	USB_85D	USB	USB_EXTC_N 8 18
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 6 32
	USB_85D	USB	USB_CAMERA_CONN_N 6 32
1223 USB_CAMERA	USB_85D	USB	USB_CAMERA_P 18 32
1223	USB_85D	USB	USB_CAMERA_N 18 32
USB_BT	USB_85D	USB	USB_BT_P 8 32
	USB_85D	USB	USB_BT_N 8 32
1228 USB_BT	USB_85D	USB	USB_BT_CONN_P 6 32
1228	USB_85D	USB	USB_BT_CONN_N 6 32
USB_TPAD	USB_85D	USB	USB_TPAD_P 8 53
	USB_85D	USB	USB_TPAD_N 8 53
1268 USB_TPAD	USB_85D	USB	USB_TPAD_R_P 25 53 101
1269	USB_85D	USB	USB_TPAD_R_N 25 53 101
1273	USB_85D	USB	USB_EXTD_XHCI_P 18 25
1274	USB_85D	USB	USB_EXTD_XHCI_N 18 25
1276	USB_85D	USB	USB_HUB_UP_P 18 25
1277	USB_85D	USB	USB_HUB_UP_N 18 25
USB_IR	USB_85D	USB	USB_IR_P 8 44
	USB_85D	USB	USB_IR_N 8 44
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS 18
1221 USB3_EXT_TX	USB_85D	USB3	USB3_EXTA_TX_P 6 18 42
1220	USB_85D	USB3	USB3_EXTA_TX_N 6 18 42
1222 USB3_EXT_RX	USB_85D	USB3	USB3_EXTA_RX_P 6 18 42
1223	USB_85D	USB3	USB3_EXTA_RX_N 6 18 42
1256 USB3_EXT_TX	USB_85D	USB3	USB3_EXTA_TX_F_P 6 42
1258	USB_85D	USB3	USB3_EXTA_TX_F_N 6 42
1257 USB3_EXT_RX	USB_85D	USB3	USB3_EXTA_RX_F_P 6 42
1259	USB_85D	USB3	USB3_EXTA_RX_F_N 6 42
1260 USB3_EXT_TX	USB_85D	USB3	USB3_EXTA_TX_C_P 6 42
1261	USB_85D	USB3	USB3_EXTA_TX_C_N 6 42
1265 USB3_EXT_TX	USB_85D	USB3	USB3_EXTB_TX_C_P 6 43
1267	USB_85D	USB3	USB3_EXTB_TX_C_N 6 43
1264 USB3_EXT_TX	USB_85D	USB3	USB3_EXTB_TX_F_P 6 43
1265	USB_85D	USB3	USB3_EXTB_TX_F_N 6 43
1262 USB3_EXT_RX	USB_85D	USB3	USB3_EXTB_RX_F_P 6 43
1263	USB_85D	USB3	USB3_EXTB_RX_F_N 6 43
1224 USB3_EXT_TX	USB_85D	USB3	USB3_EXTB_TX_P 6 18 43
1225	USB_85D	USB3	USB3_EXTB_TX_N 6 18 43
1226 USB3_EXT_RX	USB_85D	USB3	USB3_EXTB_RX_P 6 18 43
1227	USB_85D	USB3	USB3_EXTB_RX_N 6 18 43
1230	USB_85D	USB	USB_EXTB_EHCI_P 18 25
1231	USB_85D	USB	USB_EXTB_EHCI_N 18 25
1232	USB_85D	USB	USB_EXTB_XHCI_P 18 25
1233	USB_85D	USB	USB_EXTB_XHCI_N 18 25
1234 USB_EXTB_MUX	USB_85D	USB	USB_EXTB_F_P 43
1235 USB_EXTB_MUX	USB_85D	USB	USB_EXTB_F_N 43
1236 USB_SMC	USB_85D	USB	USB_SMC_N 8
1237 USB_SMC	USB_85D	USB	USB_SMC_P 8
1253 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P 42
1252	USB_85D	USB	USB_EXTA_MUXED_N 42
1254 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_F_P 42
1255	USB_85D	USB	USB_EXTA_MUXED_F_N 42

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

PAGE TITLE: PCH Constraints 1

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH:

PAGE: 102 OF 132

SHEET: 95 OF 105

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	LPC_50S	LPC	LPC_AD<3..0>	6 16 45 47 89
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 45 47 89
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	24 89
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 24
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	24 45
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 24 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 48
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 48
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 48
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 48
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 48
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 57
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 57
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	16 57
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 57
	HDA_50S	HDA	AUD_SDI_R	57
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 57
	HDA_50S	HDA	HDA_SDOUT_R	16 24
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 47
	SPI_55S	SPI	SPI_CLK	47
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 47
	SPI_55S	SPI	SPI_MOSI	47
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 47
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 47
	SPI_55S	SPI	SPI_CS0_L	47
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	36
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 36
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 36
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 36
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	36
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	36
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 32
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 32
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 32
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 32
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	16 32
	PCIE_85D	PCIE	PCIE_AP_D2R_N	16 32
T270	PCIE_85D	PCIE	PCIE_AP_D2R_R_P	32
T269	PCIE_85D	PCIE	PCIE_AP_D2R_R_N	32
	PCIE_85D	PCIE	PCIE_FW_R2D_P	38
	PCIE_85D	PCIE	PCIE_FW_R2D_N	38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 38
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 38
	PCIE_85D	PCIE	PCIE_FW_D2R_N	16 38
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	38
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	38
T253	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
T254	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
T262 PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_P	16 33
T261	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_N	16 33
T255	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
T257	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
T256	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
T259	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
T258	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
T260	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 24
T277 PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEX_TSTCLK_O_P	75
T278	CLK_PCIE_90D	CLK_PCIE	PEX_TSTCLK_O_N	75
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	16 75
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	16 75
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 32
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 38
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	8 16
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	8 16
T263 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_P<3..0>	8 33
T264 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_N<3..0>	8 33
T266 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_P<3..0>	8 33
T265 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_N<3..0>	8 33
T273 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_P<3..0>	33
T274 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_N<3..0>	33
T275 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_P<3..0>	33
T276 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_N<3..0>	33

SYNC_MASTER=J31_YONAS SYNC_DATE=05/05/2013

PAGE TITLE: PCH Constraints 2

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH:

PAGE: 103 OF 132

SHEET: 96 OF 105

CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR	*	=3X_DIELECTRIC	?

SOURCE: Attila Farkas Email - 8/2/10

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
ENET_RESET_L	ENET_50S	ENET_3X	ENET_RESET_L	30 36
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37
I169	ENET_50S	ENET_CR	SDCONN_DATA<7..0>	30 36
I170 CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_CMD	30 36
I171 CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK	30 36
I172	ENET_50S	ENET_CR	SDCONN_CLK_R	30
I173	ENET_50S	ENET_CR	SDCONN_CLK_R_L	30
I174	ENET_50S	ENET_CR	SDCONN_R_DATA<7..0>	30

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
I158 FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	38 40
I159 FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	38 40
I160 FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	38 40
I161 FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	38 40
I162 FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	38 40
I163 FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	38 40
I164 FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	38 40
I165 FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	38 40

Port 2 Not Used

SYNC_MASTER=K91_ERIC SYNC_DATE=08/03/2010

PAGE TITLE: Ethernet/FW Constraints

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH:

PAGE: 104 OF 132

SHEET: 97 OF 105

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C	*	=2x_DIELECTRIC	?

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
TBTDP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius’s Thunderbolt Routing Notes

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_R2D0	TBTDP_80D	TBTDP	TBT_R2D_P<0>	87
TBT_R2D0	TBTDP_80D	TBTDP	TBT_R2D_N<0>	87
TBT_R2D1	TBTDP_80D	TBTDP	TBT_R2D_P<1>	87
TBT_R2D1	TBTDP_80D	TBTDP	TBT_R2D_N<1>	87
TBT_D2R0	TBTDP_100D	TBTDP	TBT_D2R_C_P<0>	87 88
TBT_D2R0	TBTDP_100D	TBTDP	TBT_D2R_C_N<0>	87 88
TBT_D2R1	TBTDP_100D	TBTDP	TBT_D2R_C_P<1>	87 88
TBT_D2R1	TBTDP_100D	TBTDP	TBT_D2R_C_N<1>	87 88
	TBTDP_100D	TBTDP	TBT_A_D2R1_AUXCH_P	88
	TBTDP_100D	TBTDP	TBT_A_D2R1_AUXCH_N	88
	TBTDP_80D	TBTDP	DP_SDRVA_ML_C_P<3..0>	6 87
	TBTDP_80D	TBTDP	DP_SDRVA_ML_C_N<3..0>	6 87
	TBTDP_80D	TBTDP	DP_SDRVA_ML_R_P<3..0>	87
	TBTDP_80D	TBTDP	DP_SDRVA_ML_R_N<3..0>	87
DP_SDRVA_ML_ODD	TBTDP_80D	TBTDP	DP_SDRVA_ML_P<3>	87
DP_SDRVA_ML_ODD	TBTDP_80D	TBTDP	DP_SDRVA_ML_N<3>	87
DP_SDRVA_ML_ODD	TBTDP_80D	TBTDP	DP_SDRVA_ML_P<1>	87
DP_SDRVA_ML_ODD	TBTDP_80D	TBTDP	DP_SDRVA_ML_N<1>	87
DP_SDRVA_ML_EVEN	TBTDP_80D	TBTDP	DP_SDRVA_ML_P<2>	6 87
DP_SDRVA_ML_EVEN	TBTDP_80D	TBTDP	DP_SDRVA_ML_N<2>	6 87
DP_SDRVA_ML_EVEN	TBTDP_80D	TBTDP	DP_SDRVA_ML_P<0>	6 87
DP_SDRVA_ML_EVEN	TBTDP_80D	TBTDP	DP_SDRVA_ML_N<0>	6 87
	TBTDP_80D	TBTDP	DP_SDRVA_AUXCH_P	87
	TBTDP_80D	TBTDP	DP_SDRVA_AUXCH_N	87
	TBTDP_80D	TBTDP	DP_SDRVA_AUXCH_C_P	87
	TBTDP_80D	TBTDP	DP_SDRVA_AUXCH_C_N	87
	TBTDP_80D	TBTDP	TBT_A_ML_P<3..0>	87 88
	TBTDP_80D	TBTDP	TBT_A_ML_N<3..0>	87 88
	TBTDP_80D	TBTDP	TBT_A_ML_C_P<3..0>	87 88
	TBTDP_80D	TBTDP	TBT_A_ML_C_N<3..0>	87 88
	TBTDP_80D	TBTDP	DP_A_EXT_AUXCH_P	87 88
	TBTDP_80D	TBTDP	DP_A_EXT_AUXCH_N	87 88

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	6 33 81
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	6 33 81
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	6 33
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	6 33 81
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	6 33 81
DP_TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	6 33
DP_TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	6 33 81
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	6 33 81
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	6 33
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	6 33 81
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	6 33 81
DP_TBTSNK1_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	6 33
DP_TBTSNK1_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
	TBT_I2C_55S	TBT_I2C	I2C_TBT_SCL	33 48
	TBT_I2C_55S	TBT_I2C	I2C_TBT_SDA	33 48
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	33
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	33
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	33
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	33
	TBTDP_80D	TBTDP	TBT_R2D_C_P<3..0>	6 8 33 87
	TBTDP_80D	TBTDP	TBT_R2D_C_N<3..0>	6 8 33 87
	TBTDP_100D	TBTDP	TBT_D2R_P<3..0>	8 33 87
	TBTDP_100D	TBTDP	TBT_D2R_N<3..0>	8 33 87

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=T29_REF SYNC_DATE=06/14/2011

PAGE TITLE: Thunderbolt Constraints

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH:

PAGE: 105 OF 132

SHEET: 98 OF 105

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	45 48
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	45 48
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	45 48
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	45 48
SMBUS_SMC_2_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	6 45 48
SMBUS_SMC_2_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	6 45 48
SMBUS_SMC_3_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	45 48
SMBUS_SMC_3_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	45 48
SMBUS_SMC_5_G3_SCL	SMB_50S	SMB	SMBUS_SMC_5_G3_SCL	6 45 48
SMBUS_SMC_5_G3_SDA	SMB_50S	SMB	SMBUS_SMC_5_G3_SDA	6 45 48

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	65
	1TO1_DIFFPAIR		CHGR_CSI_N	65
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	65
	1TO1_DIFFPAIR		CHGR_CSO_N	65

SYNC_MASTER=J31_YONAS SYNC_DATE=08/11/2011

PAGE TITLE: SMC Constraints

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH:

PAGE: 106 OF 132

SHEET: 99 OF 105

GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP,BOTTOM	=5x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	77 79
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	77 79
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	77 79
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	77 79
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_A<8..0>	6 77 79
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_A<8..0>	6 77 79
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_ABI_L	6 77 79
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_ABI_L	6 77 79
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_RAS_L	77 79
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_RAS_L	77 79
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CAS_L	77 79
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CAS_L	77 79
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_WE_L	77 79
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_WE_L	77 79
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_CKE_L	77 79
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_CKE_L	77 79
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CS_L	77 79
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CS_L	77 79
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	6 77 79
293 FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	6 77 79
294 FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	6 77 79
295 FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	6 77 79
296 FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	6 77 79
297 FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	6 77 79
298 FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	6 77 79
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	6 77 79
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	6 77 79
299 FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	6 77 79
300 FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	6 77 79
301 FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	6 77 79
302 FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	6 77 79
303 FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	6 77 79
304 FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	6 77 79
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	6 77 79
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>	6 77 79
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>	6 77 79
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>	6 77 79
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>	6 77 79
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>	6 77 79
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>	6 77 79
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>	6 77 79
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>	6 77 79
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	6 77 79
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	6 77 79
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	6 77 79
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	6 77 79
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	6 77 79
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	6 77 79
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	6 77 79
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	6 77 79
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_RESET_L	77 79
1323 FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_RESET_L	77 79

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	77 80
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	77 80
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	77 80
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	77 80
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_A<8..0>	6 77 80
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_A<8..0>	6 77 80
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_ABI_L	6 77 80
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_ABI_L	6 77 80
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_RAS_L	77 80
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_RAS_L	77 80
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CAS_L	77 80
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CAS_L	77 80
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_WE_L	77 80
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_WE_L	77 80
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_CKE_L	77 80
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_CKE_L	77 80
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CS_L	77 80
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CS_L	77 80
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	6 77 80
1305 FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	6 77 80
1306 FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	6 77 80
1307 FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	6 77 80
1310 FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	6 77 80
1309 FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	6 77 80
1308 FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	6 77 80
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	6 77 80
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	6 77 80
1311 FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	6 77 80
1312 FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	6 77 80
1313 FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	6 77 80
1316 FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	6 77 80
1315 FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	6 77 80
1314 FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	6 77 80
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	6 77 80
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	6 77 80
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	6 77 80
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	6 77 80
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	6 77 80
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	6 77 80
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	6 77 80
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	6 77 80
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	6 77 80
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	6 77 80
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	6 77 80
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	6 77 80
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	6 77 80
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	6 77 80
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	6 77 80
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	6 77 80
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	6 77 80
1324 FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_RESET_L	77 80
1325 FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_RESET_L	77 80

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P	86 89
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N	86 89
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>	86 89
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>	86 89
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P	86 89
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N	86 89
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>	86 89
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>	86 89
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P	6 85
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N	6 85
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P	6 85
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N	6 85
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P	85 86
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N	85 86
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>	6 85 86
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>	6 85 86
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P	85 86
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N	85 86
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>	6 85 86
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>	6 85 86

Kepler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
GPU_CLK27M_IN	CLK_SLOW_45S	CLK_SLOW	GPU_OSC_27M_XTALIN	81 82
GPU_CLK27M_OUT	CLK_SLOW_45S	CLK_SLOW	GPU_OSC_27M_XTALOUT	81 82
1326	CLK_SLOW_45S	CLK_SLOW	GPU_OSC_27M_XTALOUT_R	82
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P	81 89
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N	81 89
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>	81 89
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>	81 89
LVDS_EG_A_DATA3	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<3>	
LVDS_EG_A_DATA3	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<3>	
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>	81 89
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>	81 89
LVDS_EG_B_DATA3	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<3>	
LVDS_EG_B_DATA3	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<3>	
DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	81 87
DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	81 87
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	86 87
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	86 87
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_P	8 81 86
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_N	8 81 86
1322	DP_85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	87
1320	DP_85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	87
1321	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_P	87
1318	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_N	87

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

PAGE TITLE
GPU (Kepler) CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 107 OF 132
SHEET 100 OF 105

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

J31 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D1_P	51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D1_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 81
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	51 81
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUVCORE_SENSE_P	83 84
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUVCORE_SENSE_N	83 84
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	49 66
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	49 66
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_DDR_P	49
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_DDR_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIO50_CS_P	49 71
	SENSE_1TO1_55S	SENSE	CPUVCCIO50_CS_N	49 71
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_CS_R_P	
	SENSE_1TO1_55S	SENSE	GFXIMVP6_CS_R_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_CS_P	
	SENSE_1TO1_55S	SENSE	GFXIMVP6_CS_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	103
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	41 103
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	41 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_ISNS2_P	84
	SENSE_1TO1_55S	SENSE	GFXIMVP_ISNS2_N	84
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	101
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	101
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S3_P	101
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S3_N	101
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_ISNS1_P	84
	SENSE_1TO1_55S	SENSE	GFXIMVP_ISNS1_N	84
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S0GPU_P	
	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_P	
	SENSE_1TO1_55S	SENSE	ISNS_TBT_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	50 70
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	50 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_P	50 70
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_N	50 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	50 69 70
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	50 69 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	50 69 70
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	50 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS3_P	50 69 70
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS3_N	50 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	101
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	101
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_P	
	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCORE_RMC_P	105
	SENSE_1TO1_55S	SENSE	CPU_VCORE_RMC_N	105
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S3_P	101
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S3_N	101
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_GPU_R_P	
	SENSE_1TO1_55S	SENSE	ISNS_GPU_R_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPUVCCSA_R_P	49
	SENSE_1TO1_55S	SENSE	ISNS_CPUVCCSA_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPUVCCIO_R_P	49
	SENSE_1TO1_55S	SENSE	ISNS_CPUVCCIO_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S3_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S3_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PPGPUFB_S0_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PPGPUFB_S0_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_P	78 103
	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_N	78 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUFB_CS_P	78 103
	SENSE_1TO1_55S	SENSE	GPUFB_CS_N	78 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_R_P	104
	SENSE_1TO1_55S	SENSE	ISNS_TBT_R_N	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V05_GPU_PEX_IOVDD_SNS_P	78 83
	SENSE_1TO1_55S	SENSE	P1V05_GPU_PEX_IOVDD_SNS_N	78 83
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPU_FBVDDQ_SENSE_P	77 78
	SENSE_1TO1_55S	SENSE	GPU_FBVDDQ_SENSE_N	77 78

J31 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 32
	1TO1_DIFFPAIR		CHGR_CSI_R_P	65
	1TO1_DIFFPAIR		CHGR_CSI_R_N	65
	1TO1_DIFFPAIR		CHGR_CSO_R_P	65
	1TO1_DIFFPAIR		CHGR_CSO_R_N	65
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	BI_MIC_P	6 62 63
	AUDIODIFF	AUDIO	BI_MIC_N	6 62 63
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	
	AUDIODIFF	AUDIO	AUD_LO1_L_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	57 61
	AUDIODIFF	AUDIO	AUD_LO1_R_N	57 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	57 61
	AUDIODIFF	AUDIO	AUD_LO2_L_N	57 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	57 61
	AUDIODIFF	AUDIO	AUD_LO2_R_N	57 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	61
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	61
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_P	61
	AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_N	61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375L_P	61
	AUDIODIFF	AUDIO	SSM2375L_N	61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375R_P	61
	AUDIODIFF	AUDIO	SSM2375R_N	61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375S_P	61
	AUDIODIFF	AUDIO	SSM2375S_N	61
SPK_OUT		AUDIO	SPKRCONN_L_OUT_P	6 61 62
		AUDIO	SPKRCONN_L_OUT_N	6 61 62
SPK_OUT		AUDIO	SPKRCONN_R_OUT_P	6 61 62
		AUDIO	SPKRCONN_R_OUT_N	6 61 62
SPK_OUT		AUDIO	SPKRCONN_S_OUT_P	6 61 62
		AUDIO	SPKRCONN_S_OUT_N	6 61 62
	USB_85D	USB	USB_TPAD_R_P	25 53 95
	USB_85D	USB	USB_TPAD_R_N	25 53 95
		SB_POWER	PP3V3_S5	6 7
		SB_POWER	PP3V3_S0	6 7
		SB_POWER	PP1V5_S3RS0	7
		GND	GND	

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PAGE TITLE

Project Specific Constraints

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 108 OF 132

SHEET 101 OF 105

J31 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.091 MM		0.120 MM	0.080 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.091 MM		0.120 MM	0.080 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?
10X_DIELECTRIC	*	0.700 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF_ALT	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF_ALT	ISL3,ISL4,ISL9,ISL10	Y	0.099 MM	0.099 MM		0.280 MM	0.280 MM
90_OHM_DIFF_ALT	ISL2,ISL11	Y	0.099 MM	0.099 MM		0.280 MM	0.280 MM
90_OHM_DIFF_ALT	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.300 MM	0.300 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: PCB Rule Definitions

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

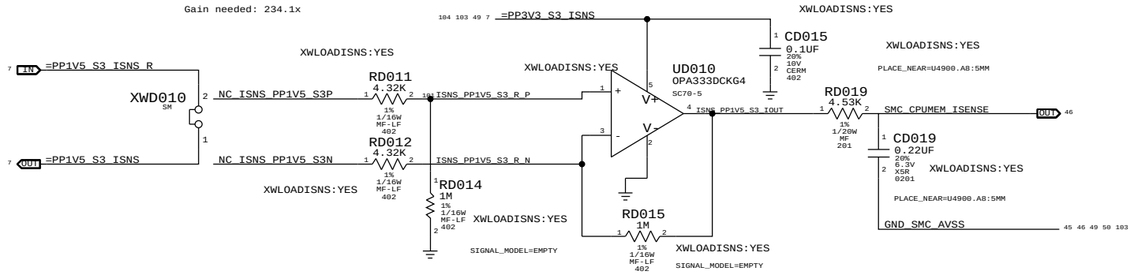
BRANCH:

PAGE: 109 OF 132

SHEET: 102 OF 105

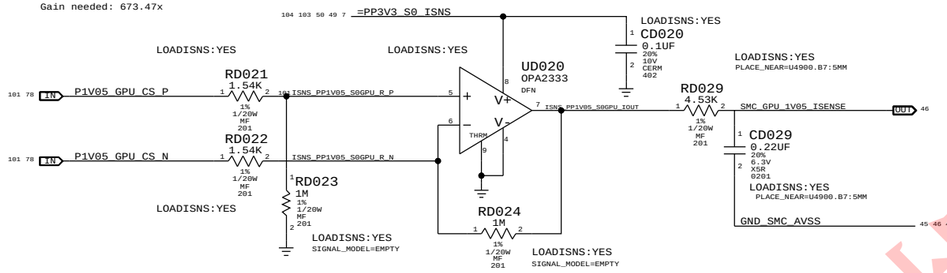
DDR 1.5V S3 (CPU & Memory) Current Sense (IM1C)

Gain: 231.4x, EDP: 14.1 A
Rsense: 0.001 (RD010)
V accross Rsense: 14.1 mV
Gain needed: 234.1x



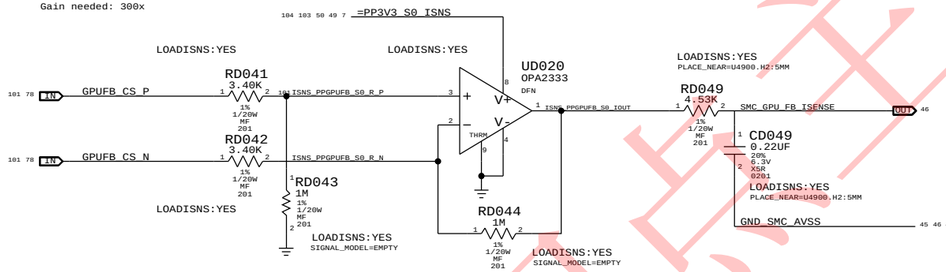
GPU 1.05V Current Sense (IG1C)

Gain: 649.35x, EDP: 4.9 A
Rsense: 0.001 (RD8310)
V accross Rsense: 4.9 mV
Gain needed: 673.47x

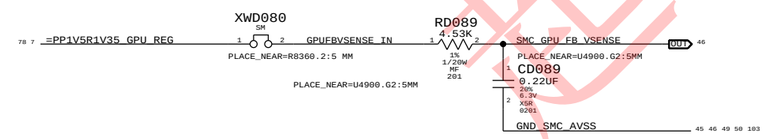


GPU FB (1.35V/1.5V) Current Sense (IG3C)

Gain: 294.12x, EDP: 11 A
Rsense: 0.001 (R8360)
V accross Rsense: 11 mV
Gain needed: 300x

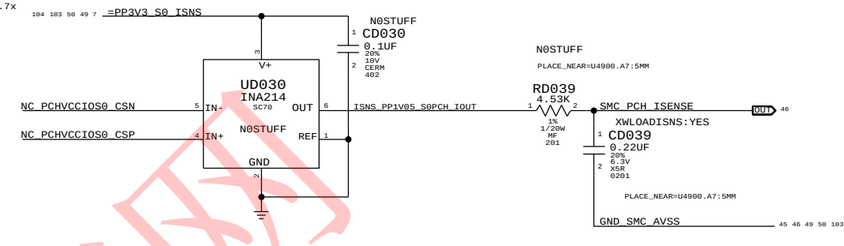


GPU FB (1.35V/1.5V) Voltage Sense (VG3C)



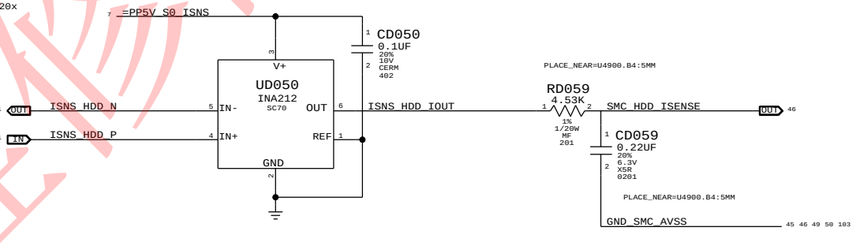
PCH Core (PCH VCCIO) Current Sense (ISBC)

Gain: 100x, EDP: 11.4 A
Rsense: 0.002 (R9840)
V accross Rsense: 22.8 mV
Gain needed: 144.7x



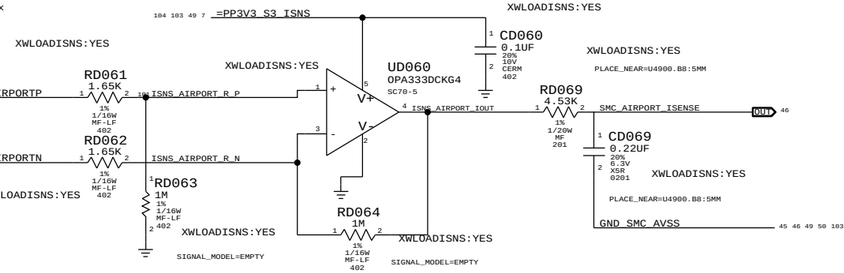
HDD Current Sense (IHDC)

Gain: 1000x, EDP: 2.5 A (12.5 W)
Rsense: 0.001 (R4599)
V accross Rsense: 2.5 mV
Gain needed: 1320x



Airport Current Sense (IAPC)

Gain: 606x, EDP: 1 A
Rsense: 0.005 (R3552)
V accross Rsense: 5 mV
Gain needed: 660x



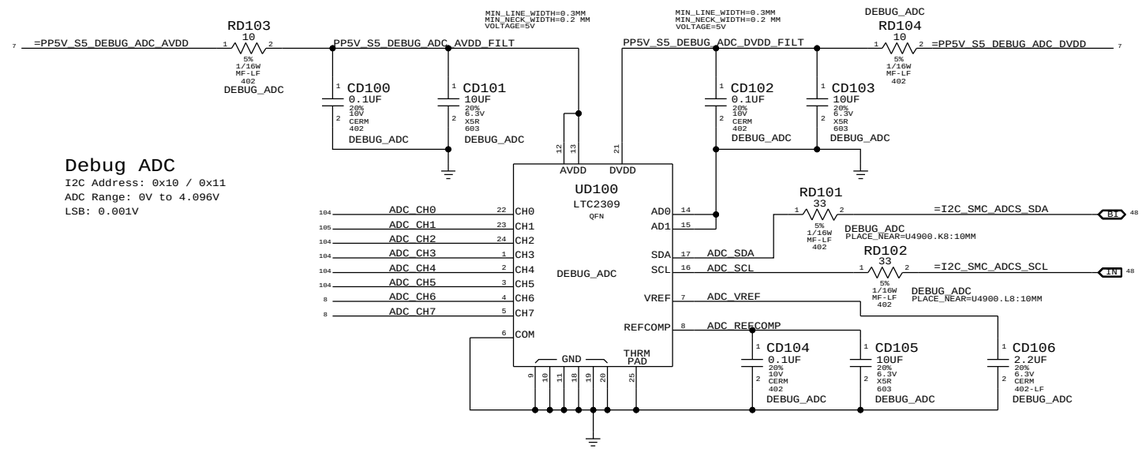
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,100K,201	CD029,CD049		LOADISNS:NO
117S0008	3	RES,100K,201	CD019,CD039,CD069		XWLOADISNS:NO

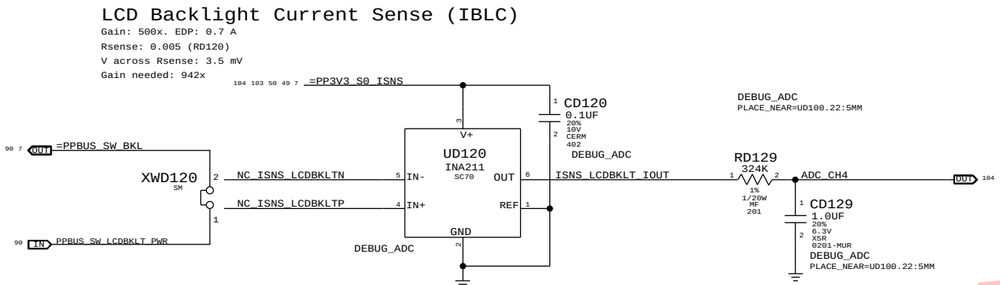
SYNC_MASTER=J31_YONAS SYNC_DATE=09/12/2013

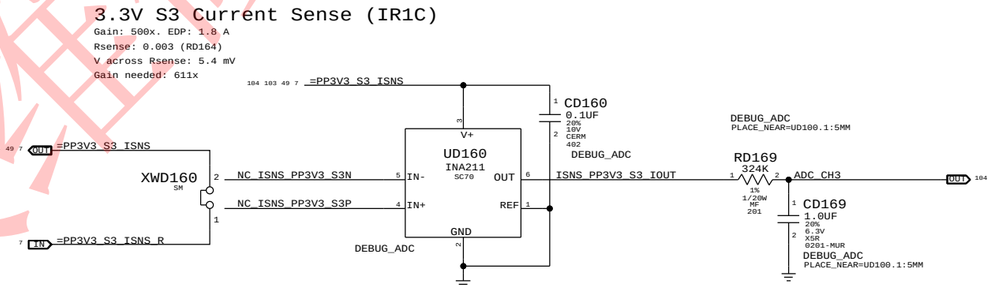
PAGE TITLE: Power Sensors: SMC Extended

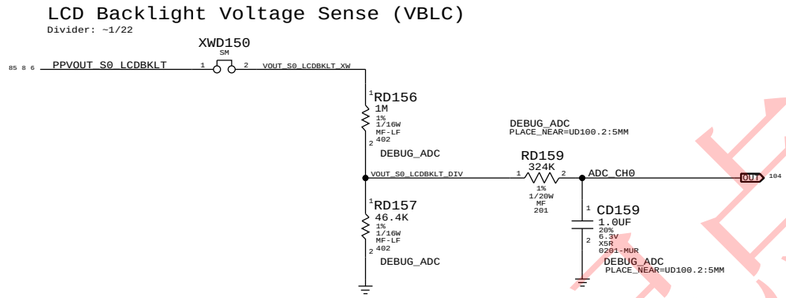
Apple Inc.

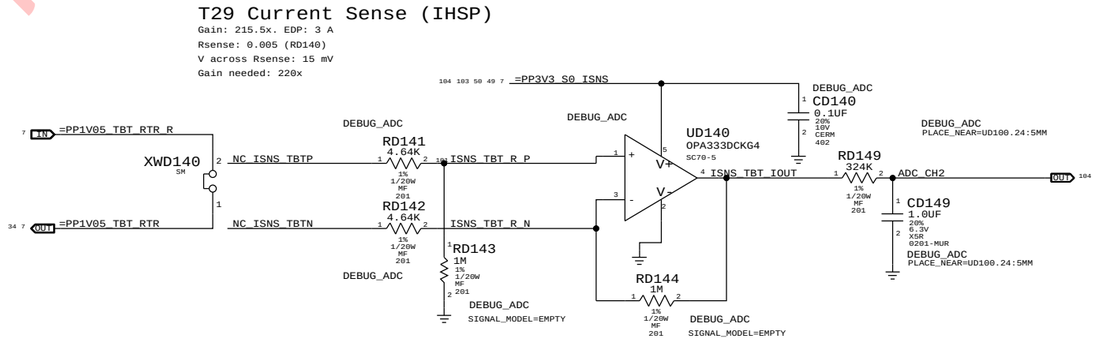
DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 130 OF 132
SHEET: 103 OF 105

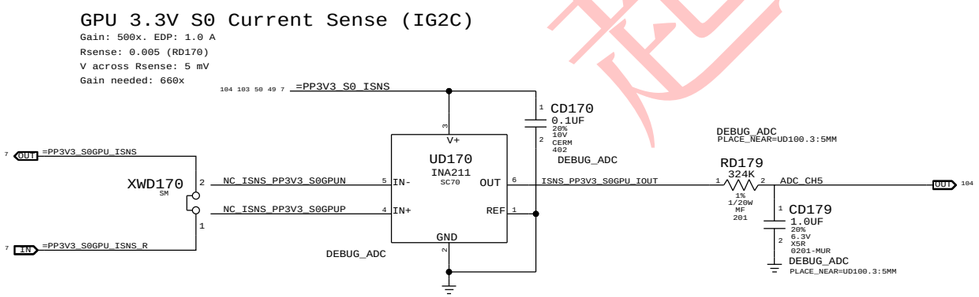






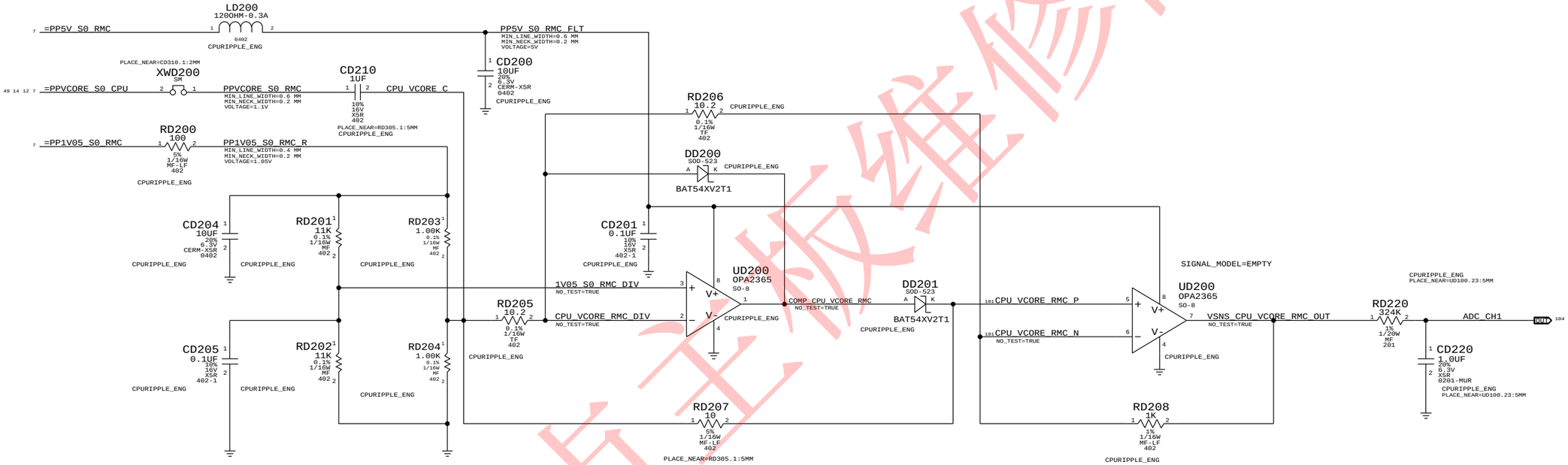






SYNC_MASTER=J31_YONAS	SYNC_DATE=09/12/2013
PAGE TITLE	Power Sensors: Debug ADC
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 131 OF 132
	SHEET 104 OF 105

CPU Rippler Voltage Sense (VCRP)



SYNC_MASTER=J31_YONAS SYNC_DATE=08/24/2011

PAGE TITLE

Power Sensors: CPU Ripple

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 132 OF 132

SHEET 105 OF 105