Latitude3000 Schematic
Haswell-ULT

2013-3-15

REV : X00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

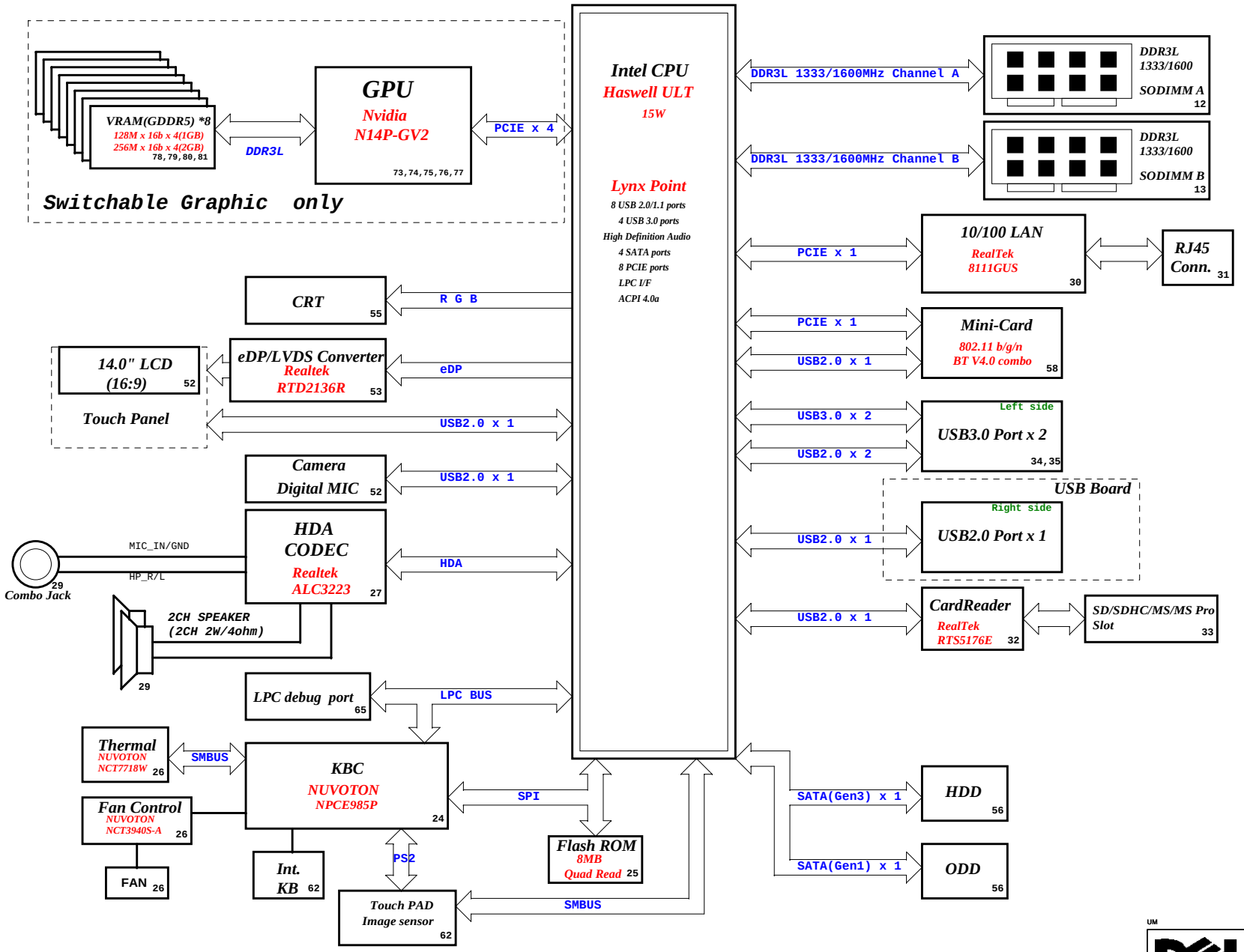
UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet 1 of 104	

Project code: 91.46O01.001
PCB P/N : 13221-SA
Revision: X00

Latitude3000 Block Diagram



CHARGER		
BQ24717		44
INPUTS	OUTPUTS	
AD+ BT+	DCBATOUT	

SYSTEM DC/DC		
TPS51225		45
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5	

CPU Core Power		
ISL95813		46,47
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	

DDR3L SUS		
TPS51216		49
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3 0D65V_S0	

CPU 1.05V		
RT8237		48
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0	

CPU 1D5V_S0		
TLV70215		51
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	

Switches 36 83	
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	0D675V_S0
VCCP_CPU	3D3V_S0
3D3V_S0	1D05V_VGA_S0
	3D3V_VGA_S0
	1D35V_VGA_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size	Document Number	Rev
C	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 2 of 104

(Blanking)

UM

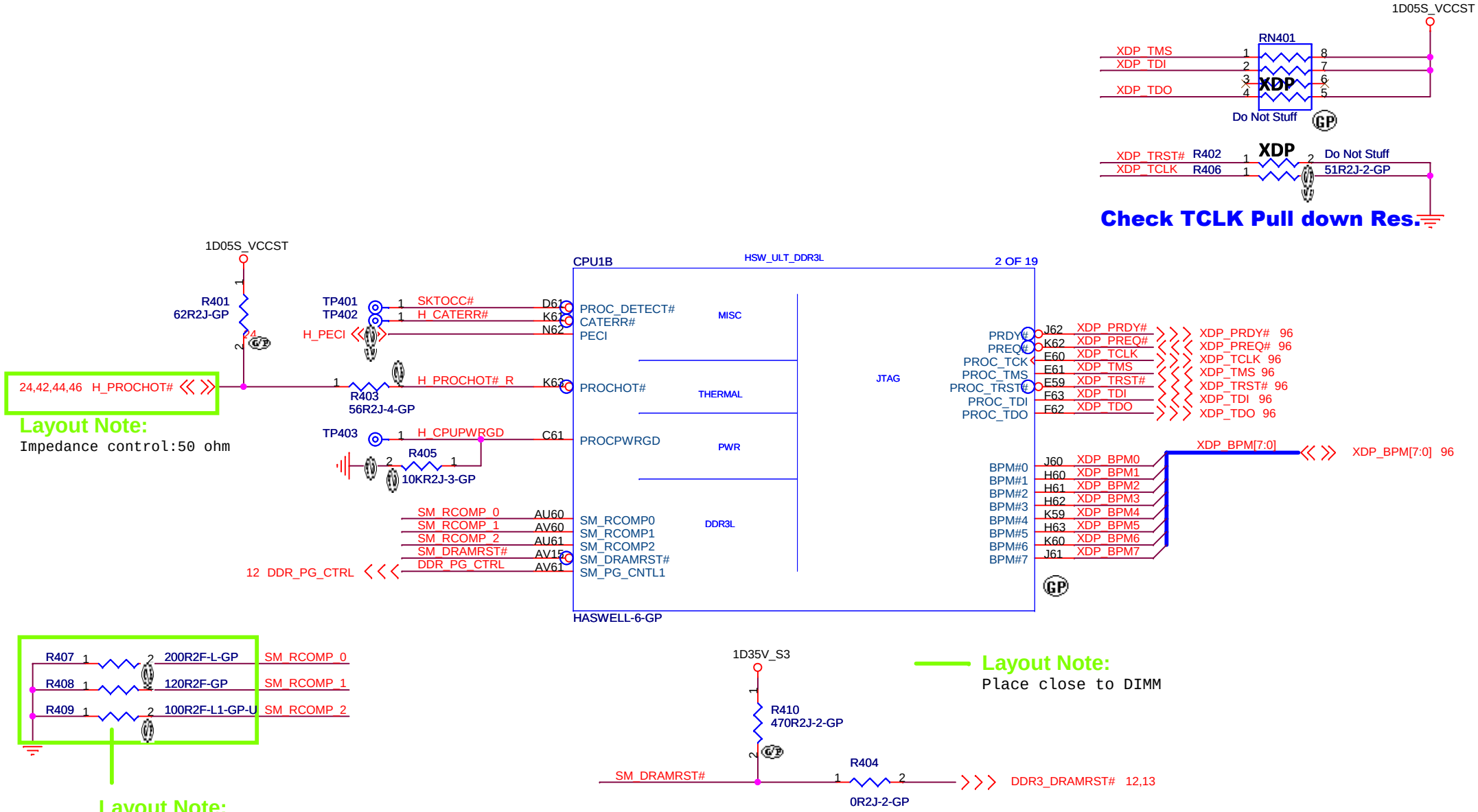
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

SSID = CPU



UM

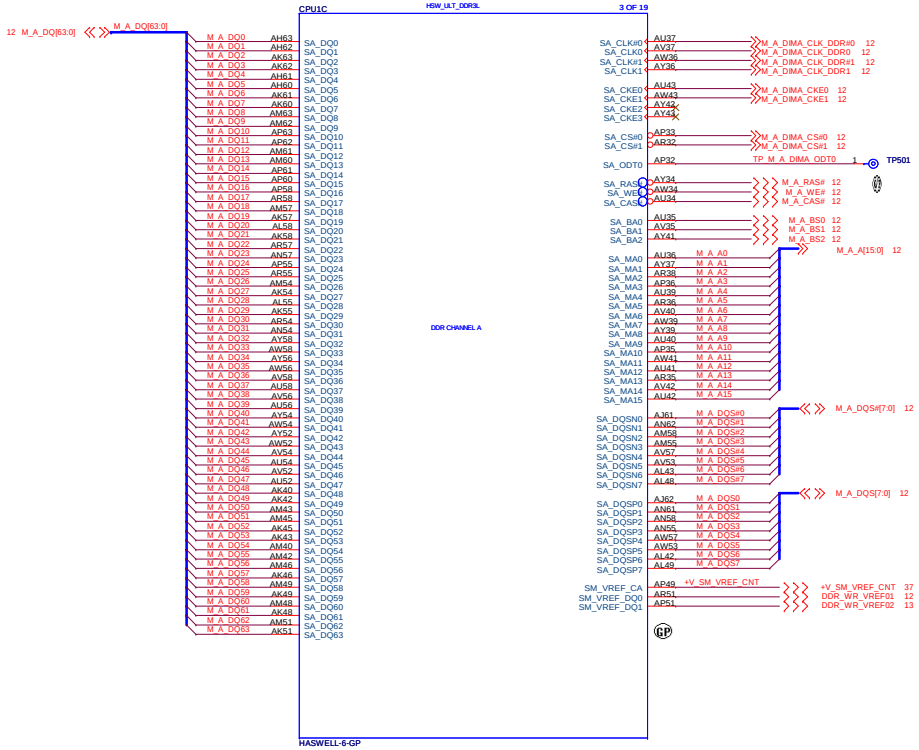
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

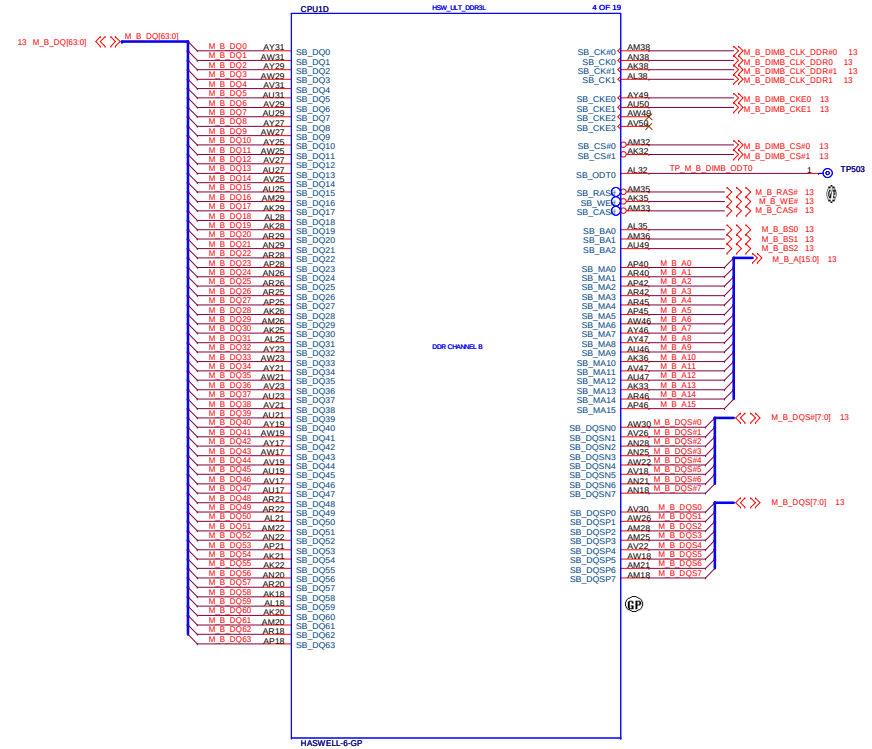
Title: ***CPU (THERMAL/MISC/PM)***

Size	Document Number	Rev
A4	***Latitude300 Haswell***	***X00***

Date: Friday, March 15, 2013 Sheet 4 of 104

SSID = CPU





UM

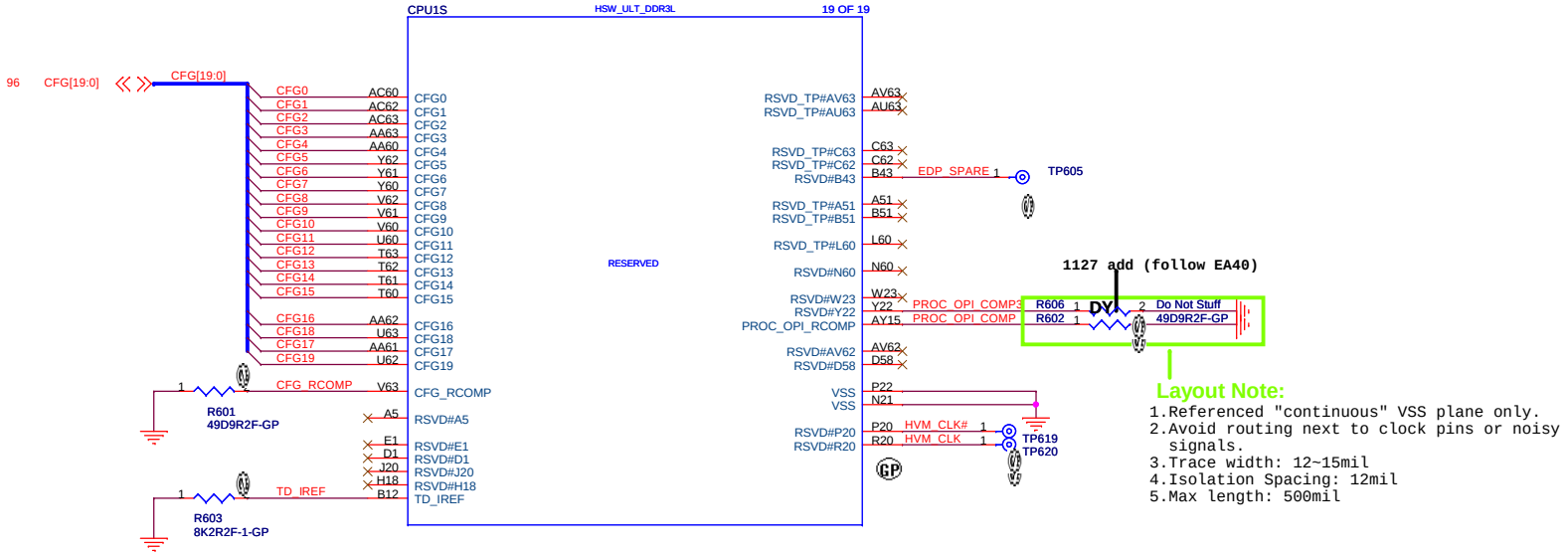
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (DDR)**

Size	Document Number	Rev
A2	Latitude300 Haswell	X00

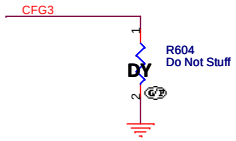
Date: Friday, March 15, 2013 Sheet 5 of 104

SSID = CPU



Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

UM

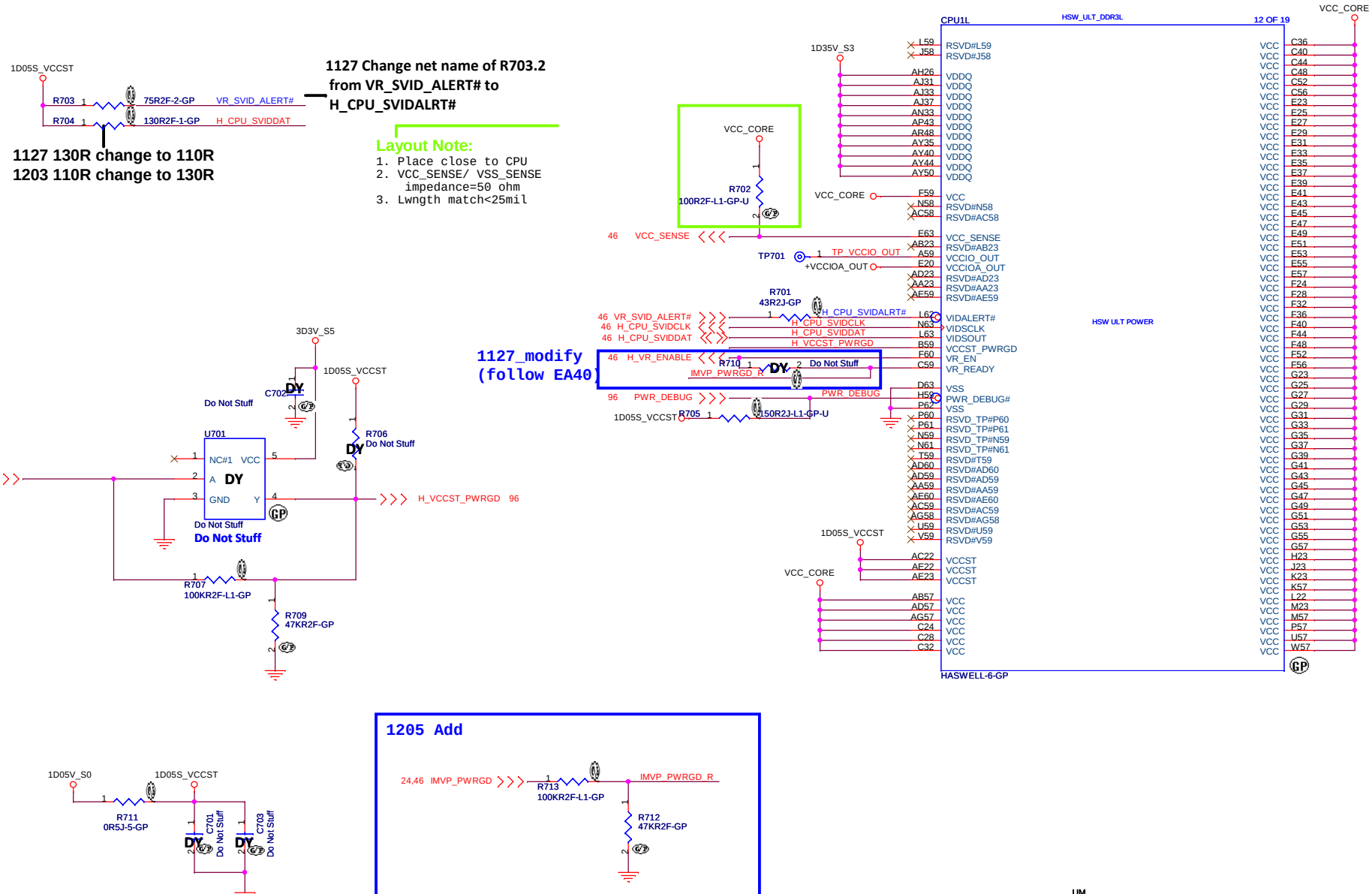
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RESERVED)

Size: A3 | Document Number: Latitude300 Haswell | Rev: X00

Date: Friday, March 15, 2013 | Sheet 6 of 104

SSID = CPU



UM

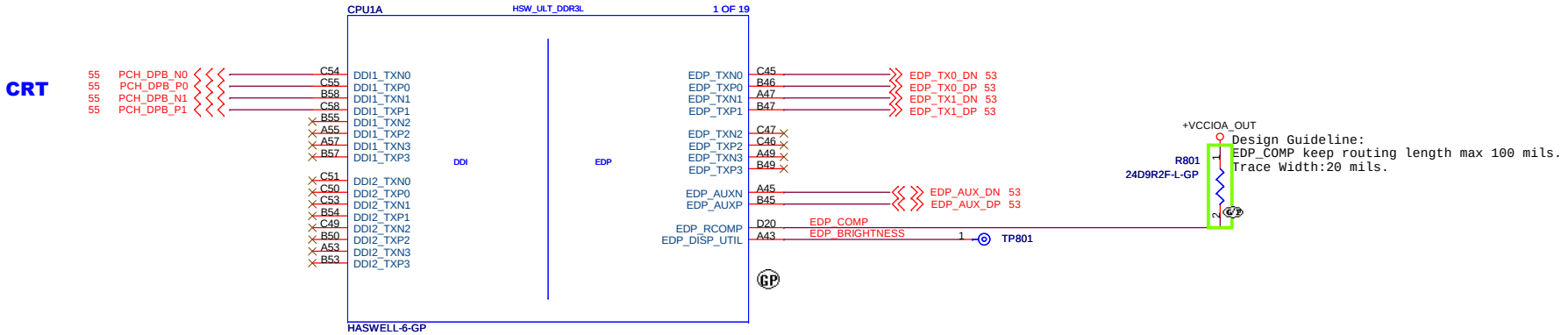
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC CORE)

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 7 of 104

SSID = CPU



UM

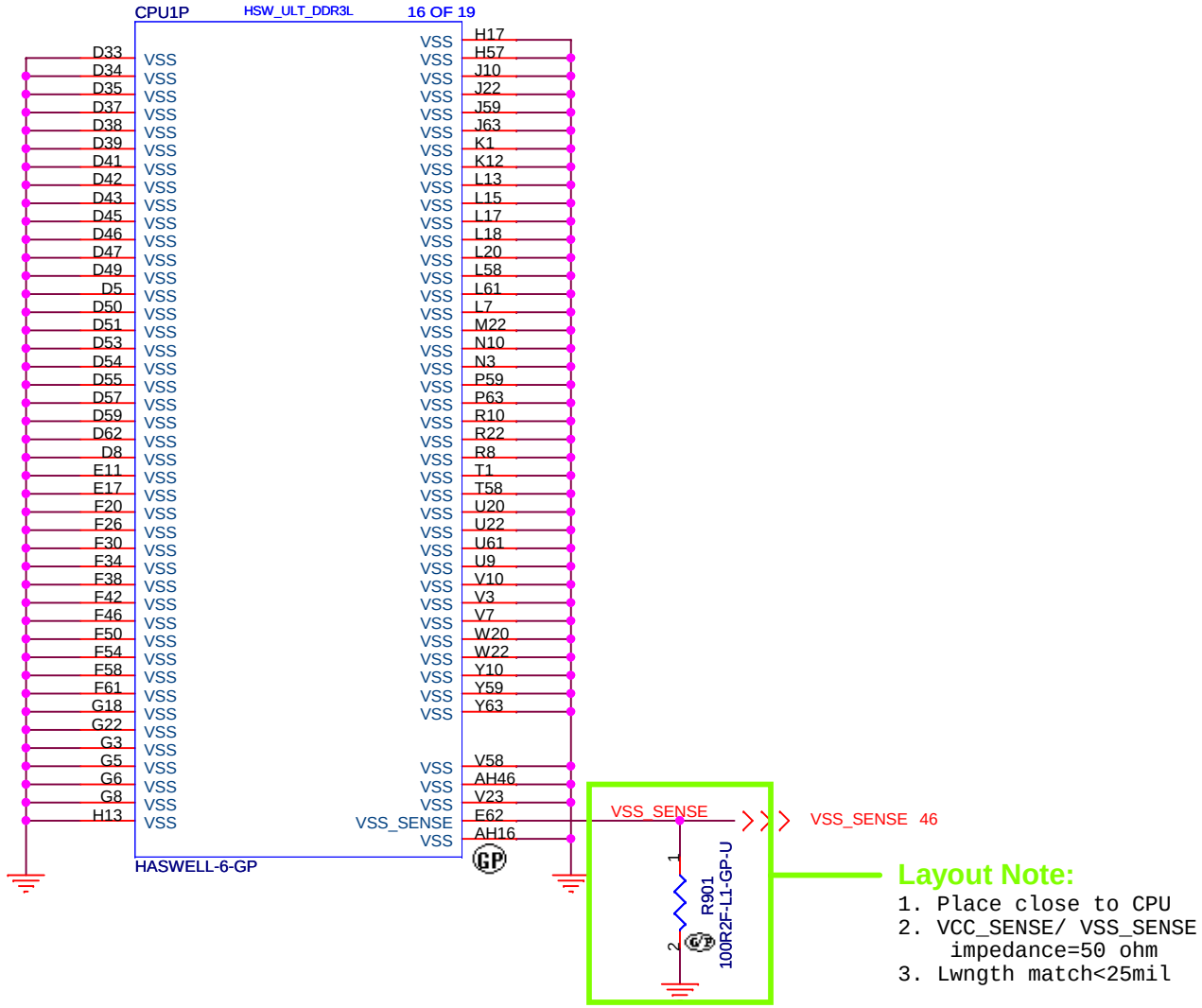
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDI/EDP)

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 8 of 104

SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Lwngth match<25mil

UM

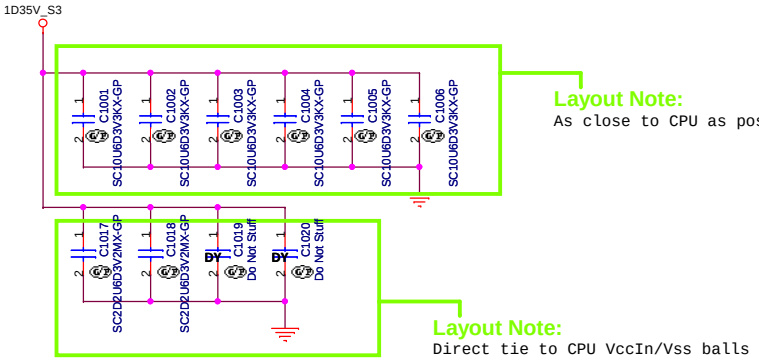
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A4	***Latitude300 Haswell***	***X00***

Date: Friday, March 15, 2013 Sheet 9 of 104

SSID = CPU



Layout Note:
As close to CPU as possible

Layout Note:
Direct tie to CPU VccIn/Vss balls

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

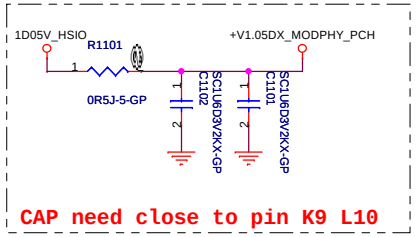
Title: ***Reserved***

Size	Document Number	Rev
A3	***Latitude300 Haswell***	*X00*

Date: Friday, March 15, 2013 Sheet 10 of 104

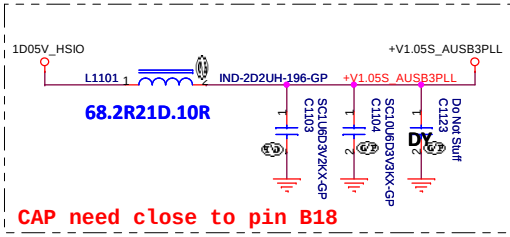
MAX: 1.92A

1.838A



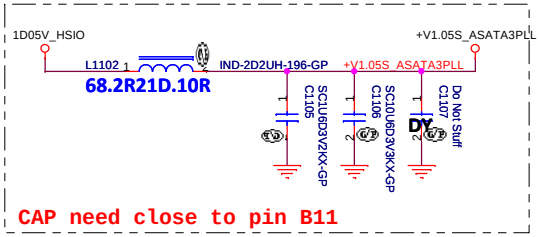
CAP need close to pin K9 L10

41mA



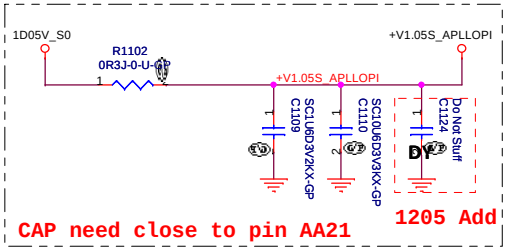
CAP need close to pin B18

42mA



CAP need close to pin B11

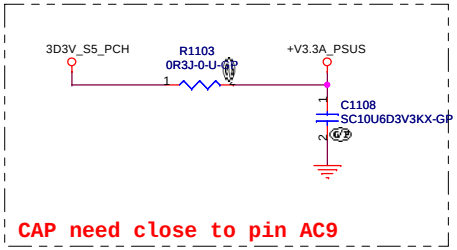
57mA



CAP need close to pin AA21

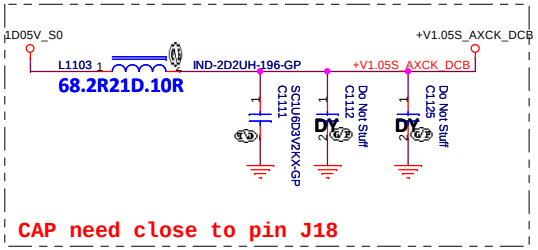
1205 Add

62mA



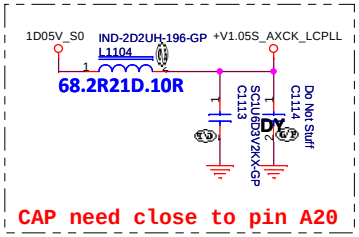
CAP need close to pin AC9

200mA



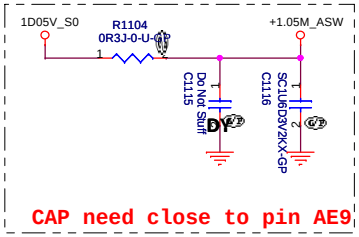
CAP need close to pin J18

31mA



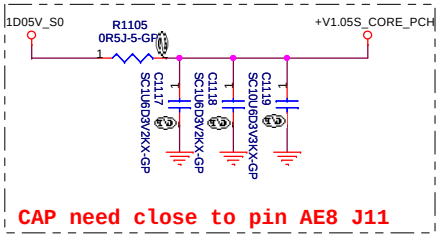
CAP need close to pin A20

658mA



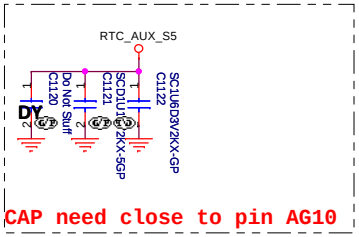
CAP need close to pin AE9

1.632A



CAP need close to pin AE8 J11

1mA



CAP need close to pin AG10

UM

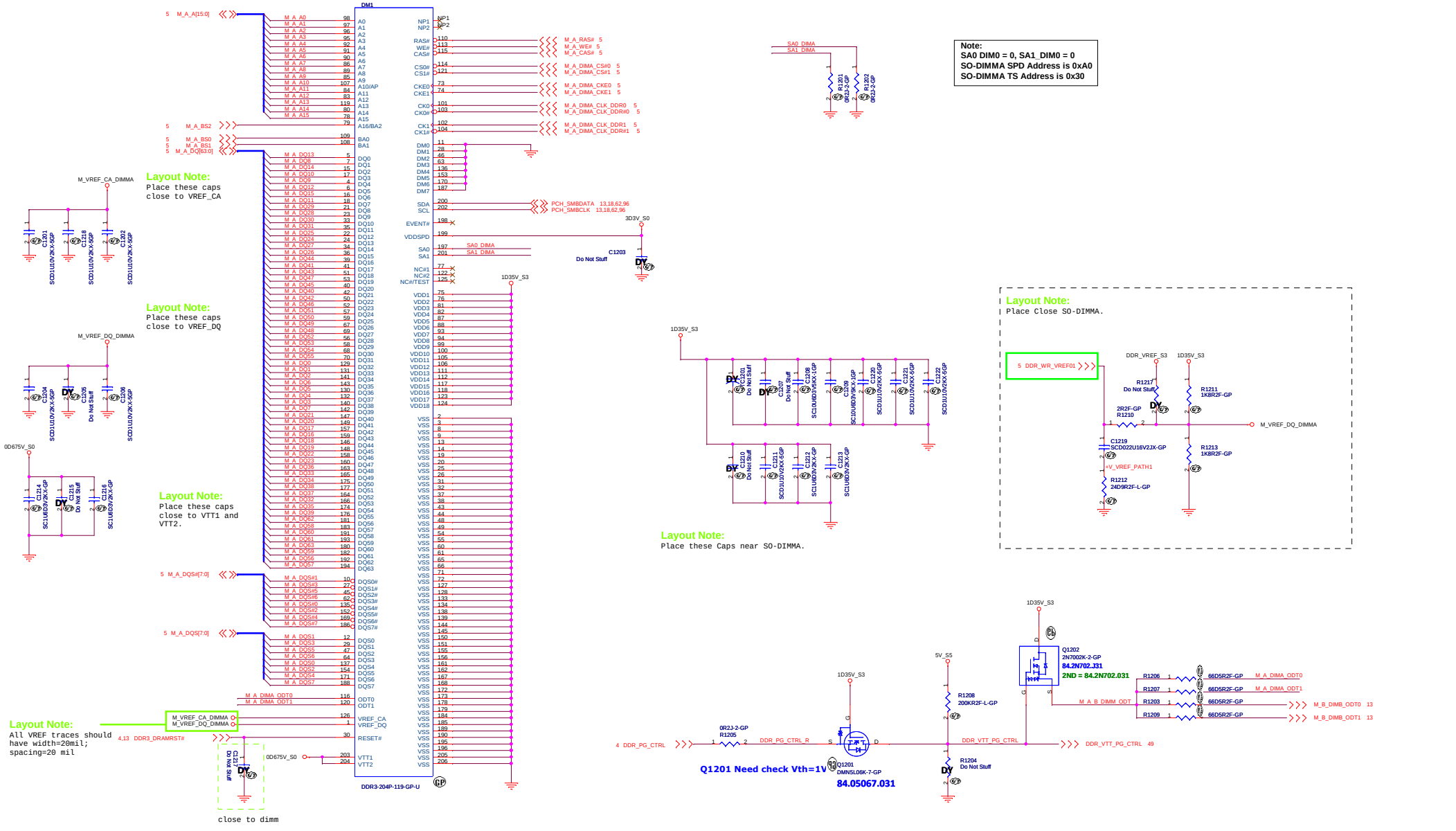
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

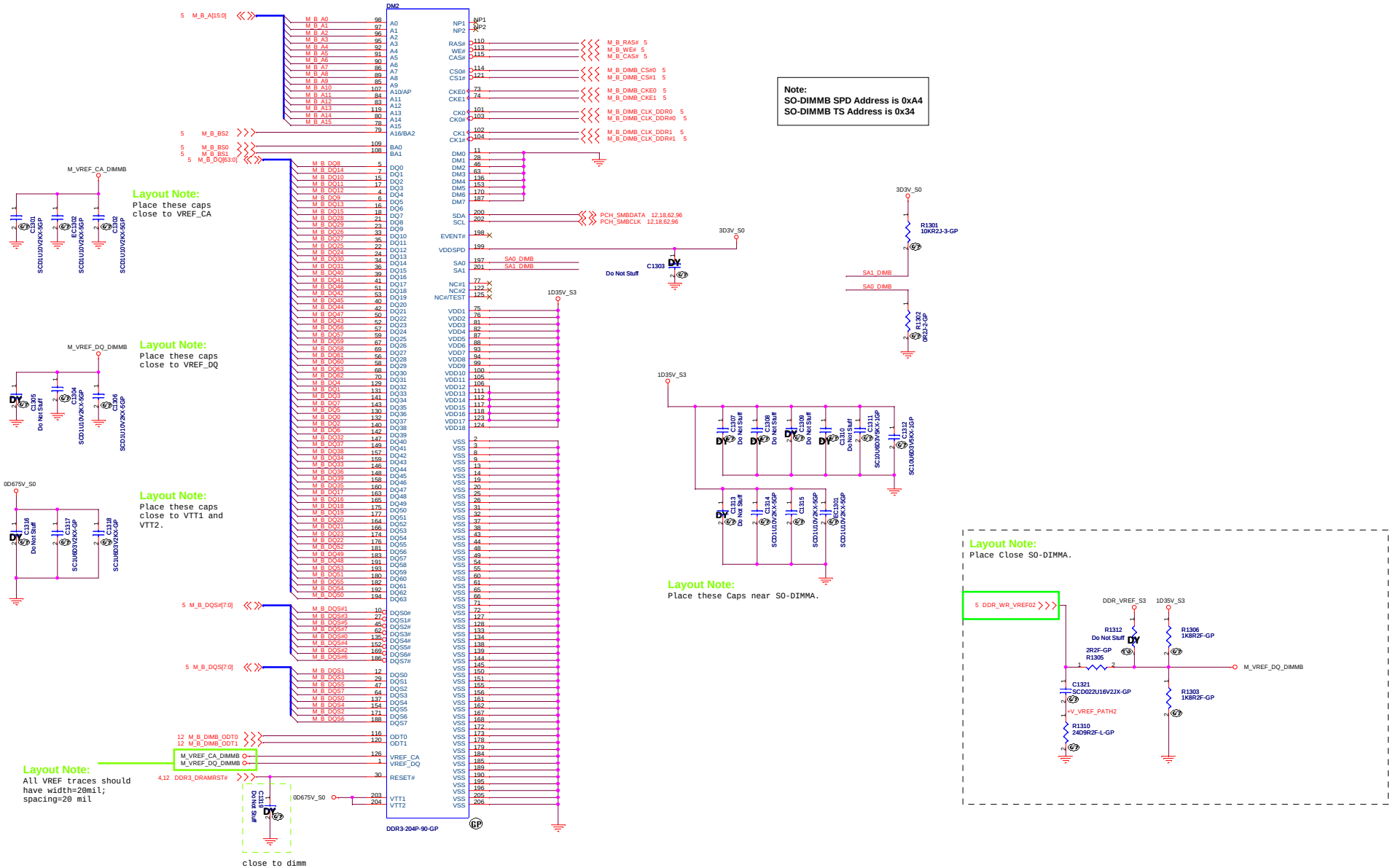
Size	Document Number	Rev
A3	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 11 of 104

SSID = MEMORY


DM1
DDR3-204P-119-GP-U
Layout Note:
Place these caps close to VREF_CA
Layout Note:
Place these caps close to VREF_DQ
Layout Note:
Place these caps close to VTT1 and VTT2.
Layout Note:
All VREF traces should have width=20mil; spacing=20 mil
close to dimm
Note:
SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
Layout Note:
Place these Caps near SO-DIMMA.
Layout Note:
Place Close SO-DIMMA.
Q1202
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
Q1201
DMN5L06K-7-GP
84.05067.031
Q1201 Need check Vth=1V
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
DDR3-SODIMM1
Latitude300 Haswell
X00
Friday, March 15, 2013

SSID = MEMORY



UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A2	*Latitude300 Haswell*	*X00*

Date: Friday, March 15, 2013 Sheet 13 of 104

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

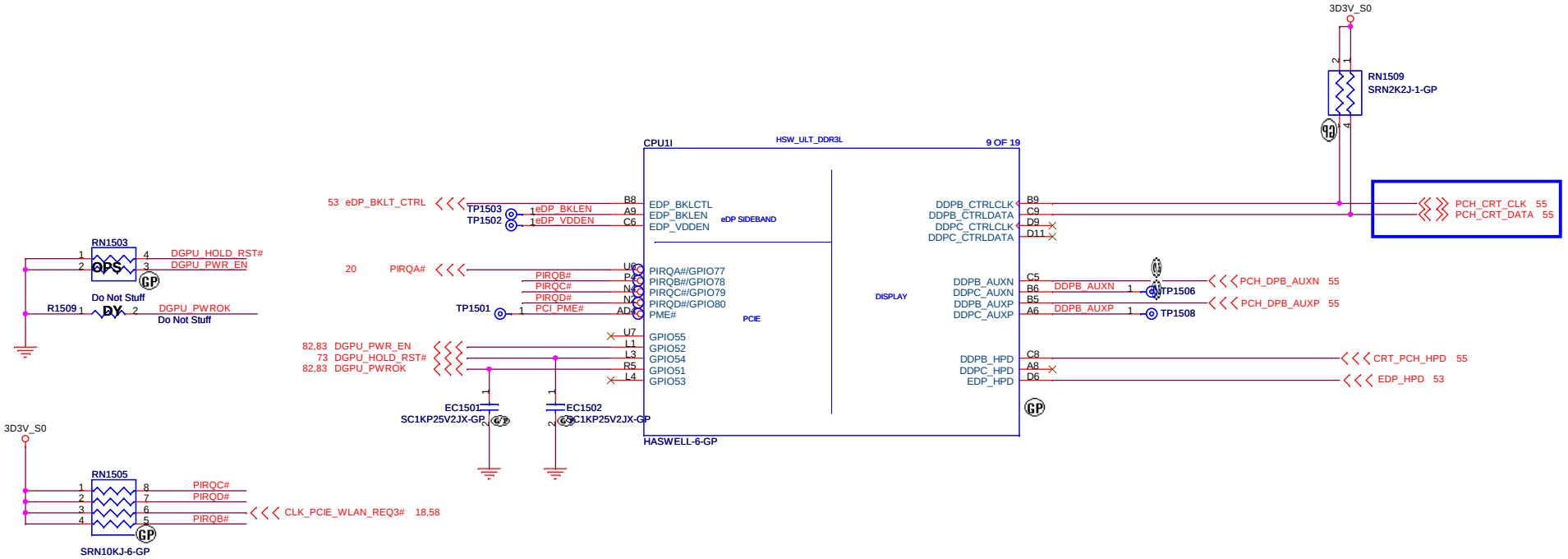
Title

M3

Size	Document Number	Rev
A3	***Latitude300 Haswell***	***X00***

Date: Friday, March 15, 2013 Sheet 14 of 104

SSID = CPU



UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (EDP/GPIO/DDI)

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 15 of 104

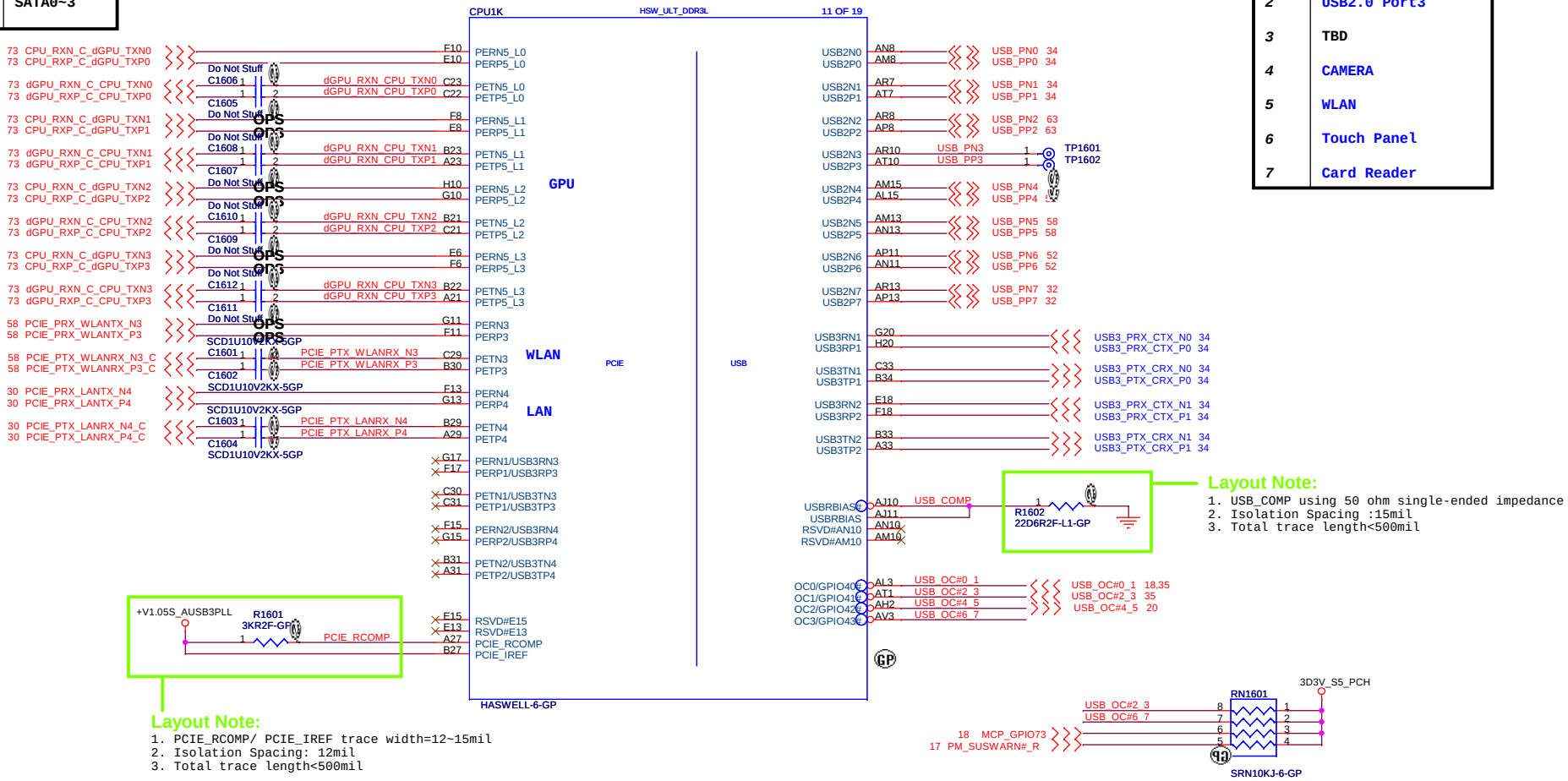
SSID = PCH

PCIE Table

Port	Device	Share BUS
1	TBD	USB3.0_3
2	TBD	USB3.0_4
3	WLAN	
4	LAN	
5(4lane)	GPU	
6(4lane)	TBD	SATA0~3

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2
2	USB2.0 Port3
3	TBD
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

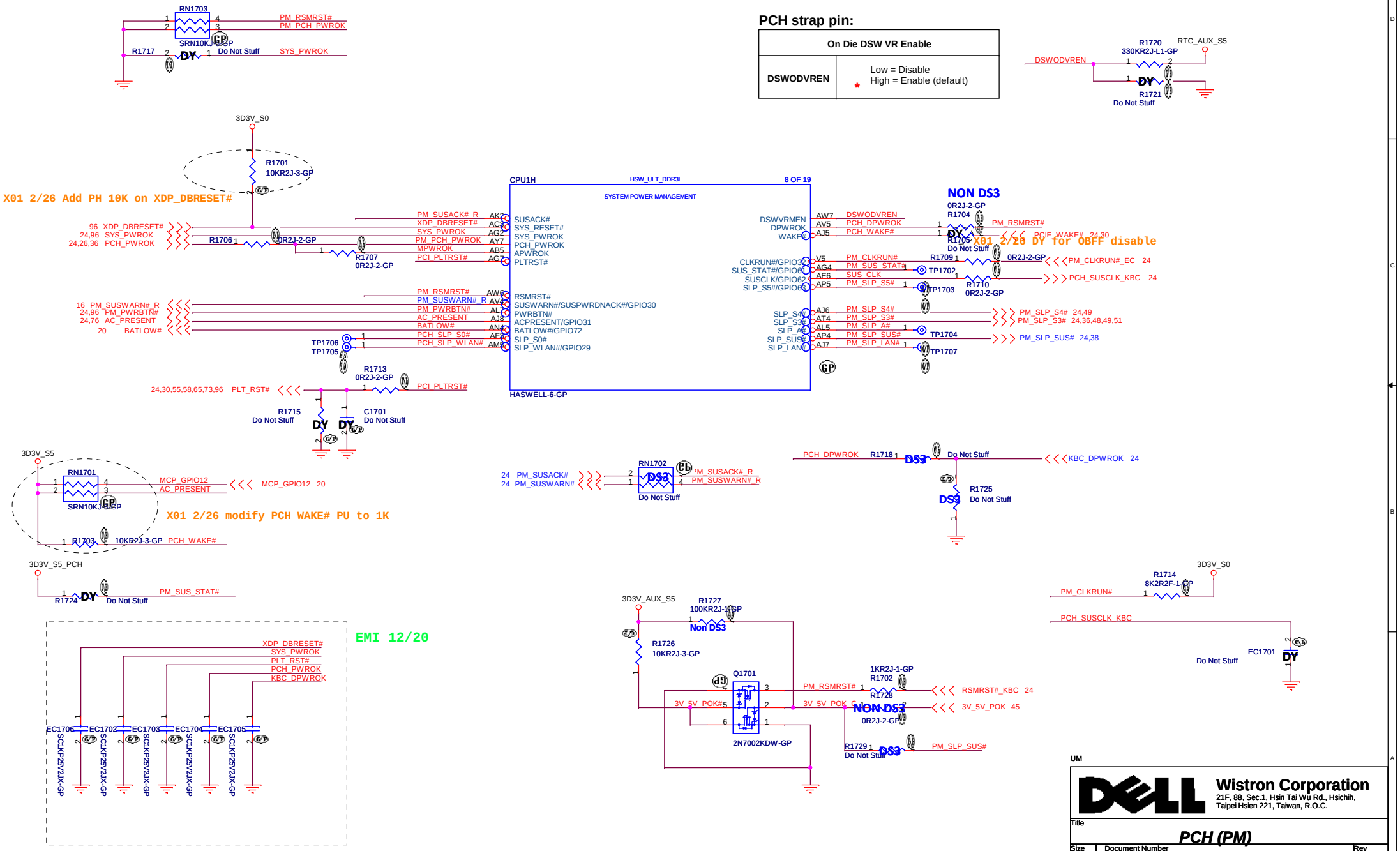


UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

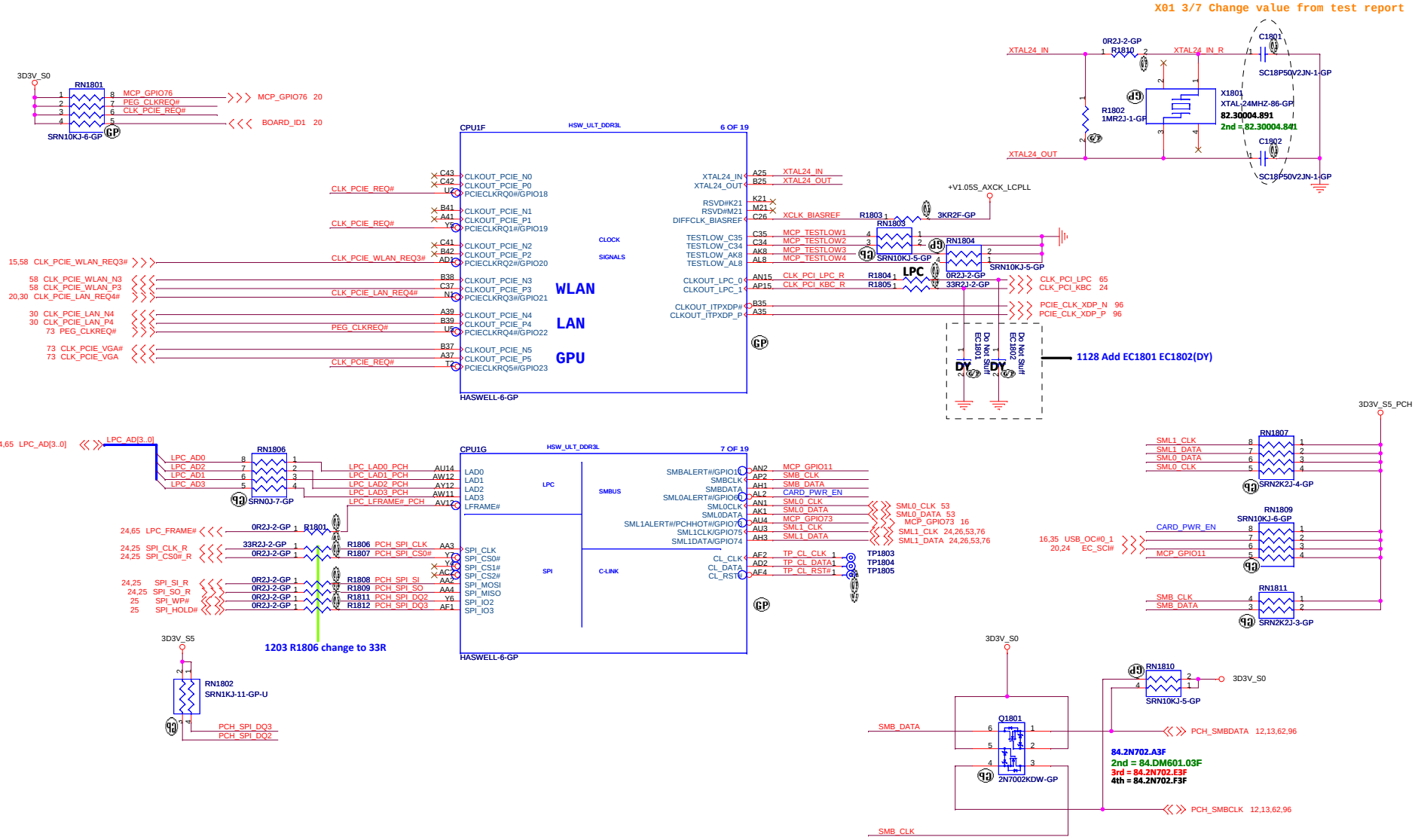
Title: PCH (PCIE/USB)		
Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet 16 of 104	

SSID = PCH


PCH strap pin:
On Die DSW VR Enable
DSWODVREN
Low = Disable
High = Enable (default)
*
X01 2/26 Add PH 10K on XDP_DBRESET#
X01 2/26 DY for OBFF disable
X01 2/26 modify PCH_WAKE# PU to 1K
EMI 12/20
NON DS3
CPU1H
HSW_ULT_DDR3L
8 OF 19
SYSTEM POWER MANAGEMENT
HASWELL-6-GP
RN1703
SRN10KJ-4-GP
R1717
R1720
330KR2J-L1-GP
R1721
RTC_AUX_S5
3D3V_S0
R1701
10KR2J-3-GP
R1706
R1707
0R2J-2-GP
R1704
R1705
R1709
R1710
TP1702
TP1703
TP1704
TP1707
R1713
R1715
C1701
3D3V_S5
RN1701
R1703
PCH_WAKE#
3D3V_S5_PCH
R1724
PM_SUS_STAT#
RN1702
R1718
R1725
KBC_DPWROK
3D3V_AUX_S5
R1727
100KR2J-1-GP
R1726
10KR2J-3-GP
Q1701
2N7002KDW-GP
1KR2J-1-GP
R1702
R1728
R1729
R1714
8K2R2F-1-GP
EC1701
EC1706
EC1702
EC1703
EC1704
EC1705
SC1KP25V2JX-GP
XDP_DBRESET#
SYS_PWROK
PLT_RST#
PCH_PWROK
KBC_DPWROK
PM_RSMRST#
PM_PCH_PWROK
SYS_PWROK
PM_SUSACK# R
XDP_DBRESET#
SYS_PWROK
PM_PCH_PWROK
MPWROK
PCI_PLTRST#
PM_SUSWARN# R
PM_PWRBTN#
AC_PRESENT
BATLOW#
PCH_SLP_S0#
PCH_SLP_WLAN#
SUSACK#
SYS_RESET#
RSMRST#
SUSWARN#/SUSPWRDNACK#/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
SLP_S0#
SLP_WLAN#/GPIO29
APWROK
PLTRST#
DSWVRMEN
DPWROK
WAKE#
DSWODVREN
PCH_DPWROK
PCH_WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK/GPIO62
SLP_S5#/GPIO63
PM_CLKRUN#
PM_SUS_STAT#
SUS_CLK
PM_SLP_S5#
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
SLP_LAN#
PM_SLP_S4#
PM_SLP_S3#
PM_SLP_A#
PM_SLP_SUS#
PM_SLP_LAN#
PLT_RST#
MCP_GPIO12
AC_PRESENT
PM_SUSACK#
PM_SUSWARN#
PCIE_WAKE#
RSMRST#_KBC
3V_5V_POK
3V_5V_POK#
PM_SLP_SUS#
PM_CLKRUN#_EC
PCH_SUSCLK_KBC
PM_SLP_S4#
PM_SLP_S3#
PM_SLP_SUS#
Do Not Stuff
DY
DS3
GP
UM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (PM)
Size
A3
Document Number
Latitude300 Haswell
Rev
X00
Date: Friday, March 15, 2013
Sheet 17 of 104

SSID = PCH

X01 3/7 Change value from test report



UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (CLOCK/SMBUS/CL/LPC/SPI)

Size	Document Number	Rev
Custom	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 18 of 104

SSID = CPU

X01 3/7 Change value from test report

X01 3/7 Change value from test report

82.30001.A41
2nd = 82.30001.841

84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31

1203 R1907 change from 0R to 33R

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

HDD1

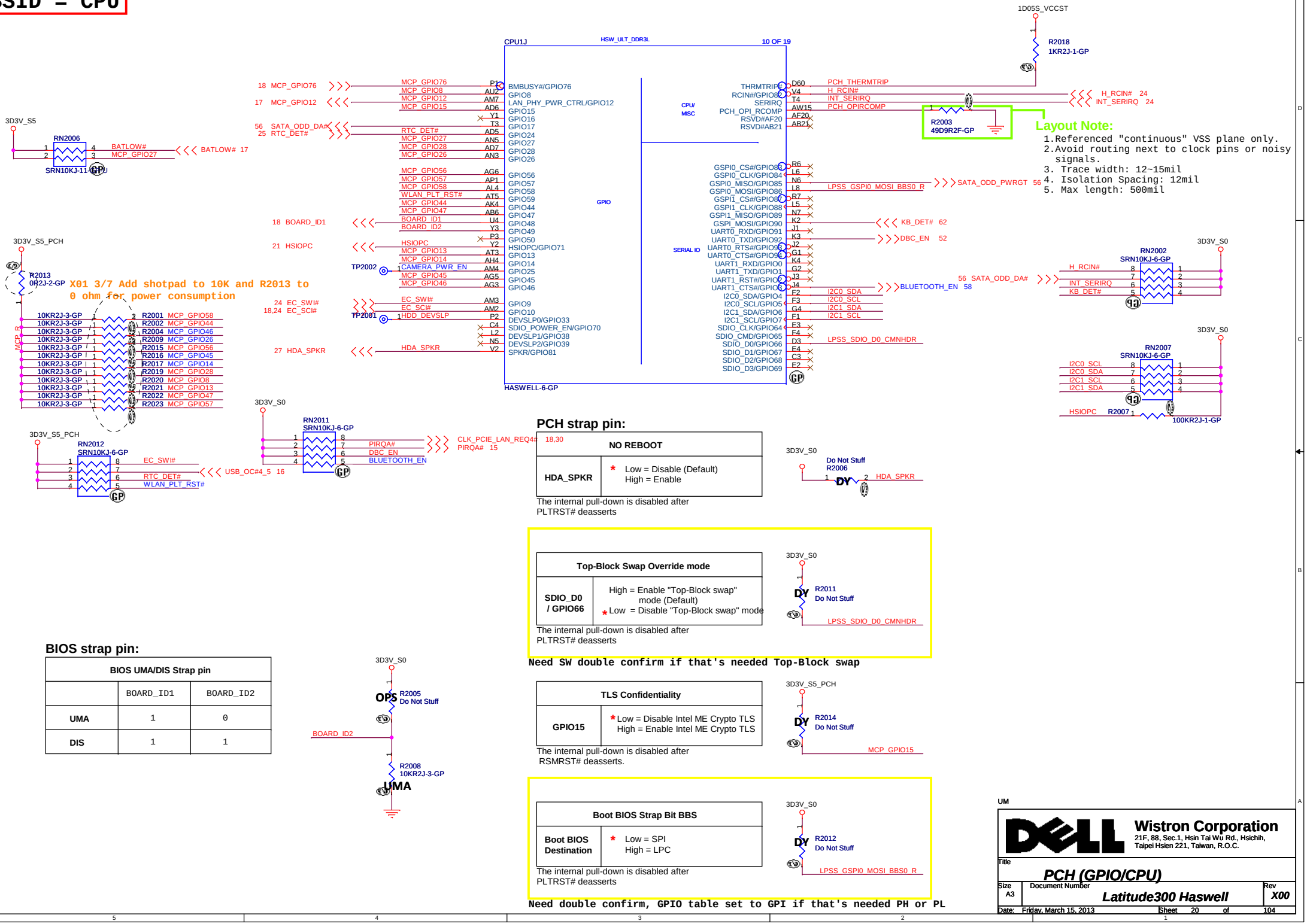
ODD

0114 Change

Layout Note:
4mil trace at break-out and 3 12-15mil trace with <0.2 ohms and length total <= 500mils.

UM			
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: PCH (RTC/SATA/HDA/JTAG)			
Size: A3	Document Number: Latitude300 Haswell		Rev: X00
Date: Friday, March 15, 2013	Sheet 19 of 104		

SSID = CPU



PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Disable (Default) High = Enable

The internal pull-down is disabled after PLTRST# deasserts

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	High = Enable "Top-Block swap" mode (Default) * Low = Disable "Top-Block swap" mode

The internal pull-down is disabled after PLTRST# deasserts

Need SW double confirm if that's needed Top-Block swap

TLS Confidentiality	
GPIO15	* Low = Disable Intel ME Crypto TLS High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts.

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI High = LPC

The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PH or PL

BIOS strap pin:

BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
UMA	1	0
DIS	1	1

UM

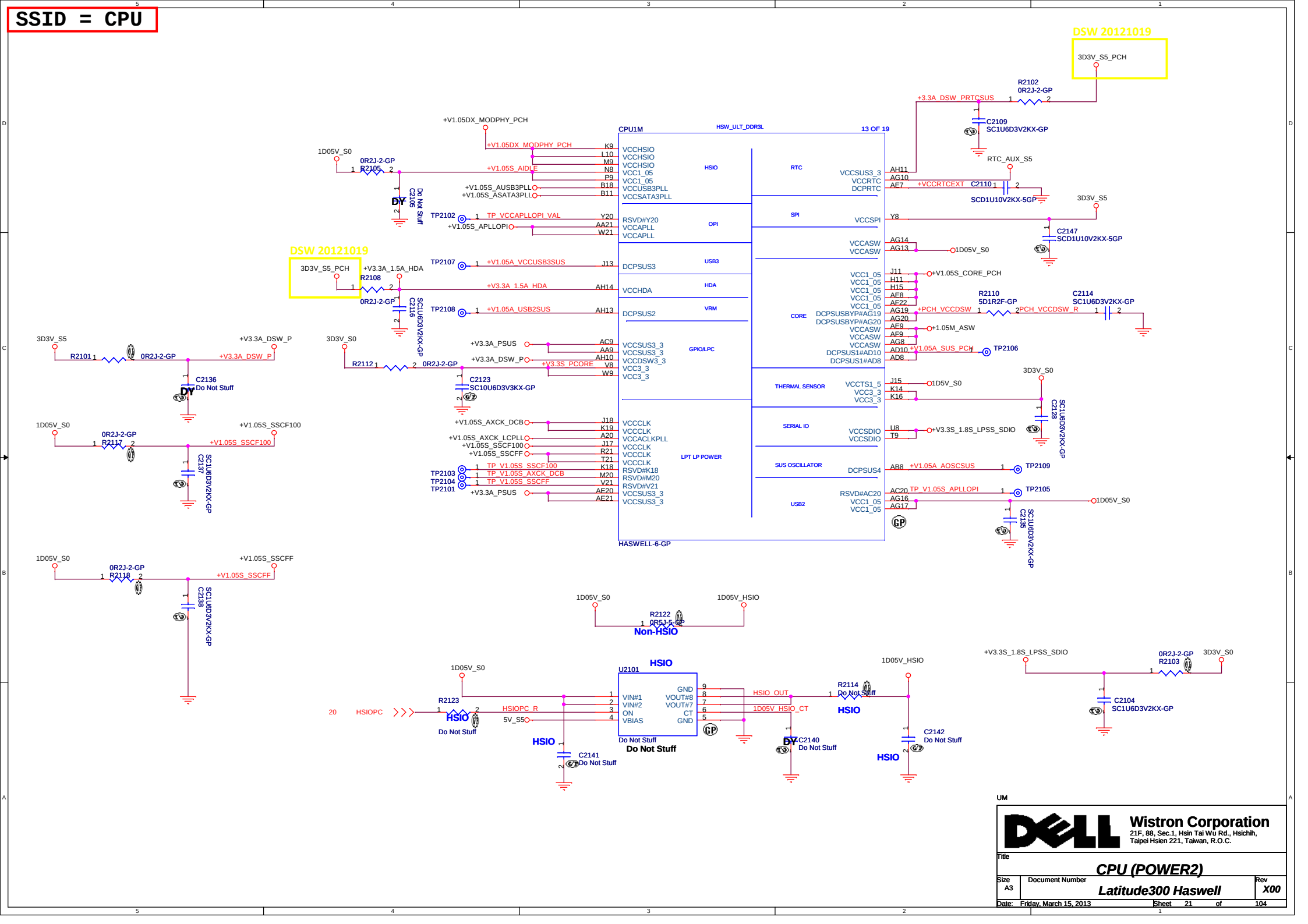
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size: A3 | Document Number: Latitude300 Haswell | Rev: X00

Date: Friday, March 15, 2013 | Sheet 20 of 104

SSID = CPU

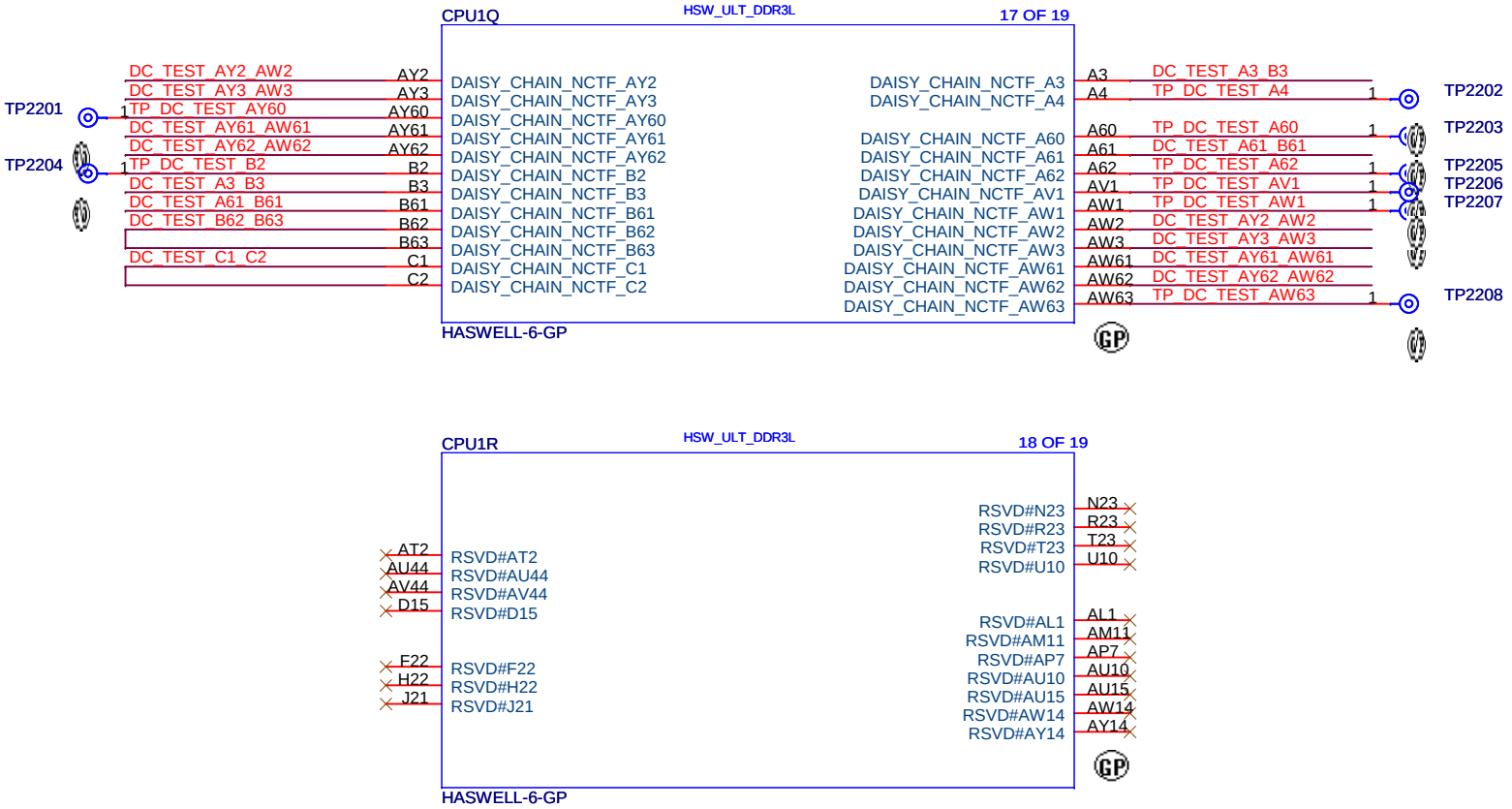


UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (POWER2)	
Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet 21 of 104	

SSID = PCH



UM

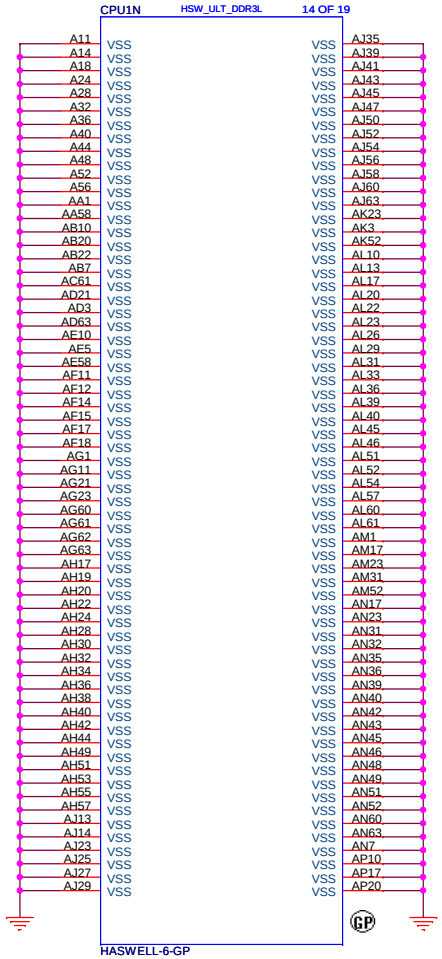
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

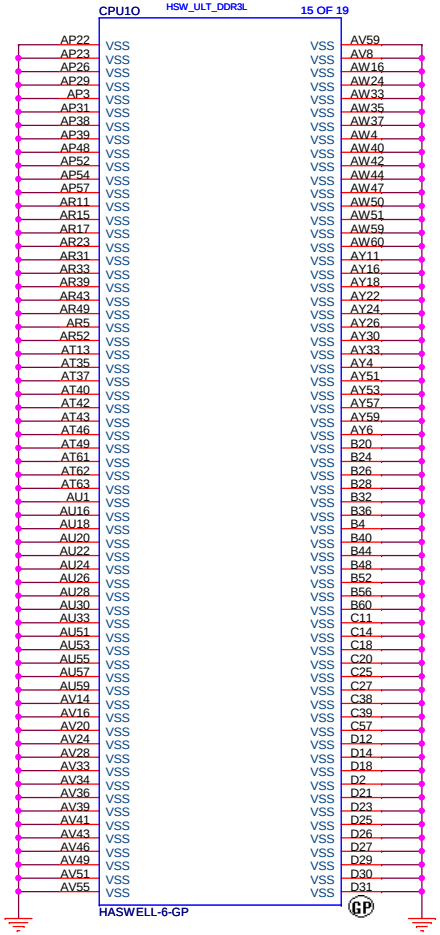
Title: ***(Reserved)***

Size	Document Number	Rev
A4	***Latitude300 Haswell***	***X00***

Date: Friday, March 15, 2013 Sheet 22 of 104

SSID = PCH





UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A3	***Latitude300 Haswell***	***X00***

Date: Friday, March 15, 2013 Sheet 23 of 104

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
UMA	100.0K	10.0K(64.10025.6D1)	3.0V
TBD	100.0K	13.7K(64.13725.6D1)	2.902V
TBD	100.0K	17.8K(64.17825.6D1)	2.801V
TBD	100.0K	22.1K(64.22125.6D1)	2.702V
TBD	100.0K	27.0K(64.27025.6D1)	2.598V
TBD	100.0K	32.4K(64.32425.6D1)	2.492V
TBD	100.0K	37.4K(64.37425.6D1)	2.402V
TBD	100.0K	43.2K(64.43225.6D1)	2.304V
DIS	100.0K	49.9K(64.49925.6D1)	2.201V
N14M-GE	100.0K	57.6K(64.57625.6D1)	2.093V
N14P-GV2	100.0K	64.9K(64.64925.6D1)	2.001V
TBD	100.0K	73.2K(64.73225.6D1)	1.905V
TBD	100.0K	82.5K(64.82525.6D1)	1.808V
TBD	100.0K	93.1K(64.93125.6D1)	1.709V
TBD	100.0K	107K(64.10735.6D1)	1.594V
TBD	100.0K	120K(64.12035.6D1)	1.499V
TBD	100.0K	137K(64.13735.6D1)	1.392V
TBD	100.0K	154K(64.15435.6D1)	1.298V
TBD	100.0K	200K(64.20035.6D1)	1.099V
TBD	100.0K	232K(64.23236.6D1)	0.994V

Layout Note:
Need very close to EC

X01 3/5 move WPAN_LED# from GPIO85 to GPIO93

Don't PD

ALL_SYS_PWRGD assert,
delay 10ms; PCH_PWROK assert.

ALL_SYS_PWRGD de-assert,
delay 100ms; SYS_PWROK assert.

LVDS backlight Control from PS8625

eDP backlight Control from Travis
Travis request response time < 1ms

71.00985.C0G

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC
C2422 PDG is 47p

Layout Note:
Connect GND and AGND planes via either
0R resistor or connect directly.

Power Switch Logic(PSL)

0111 Add

EC_GPIO47 High Active

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

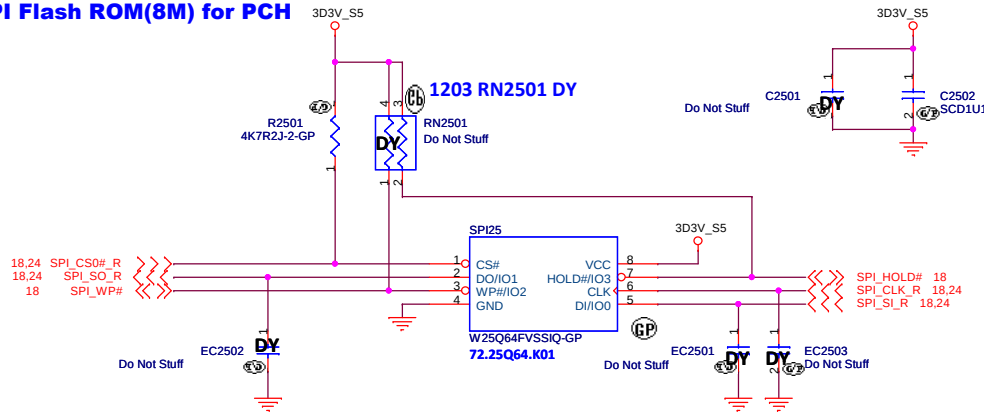
Title: KBC Nuvoton NPCE885

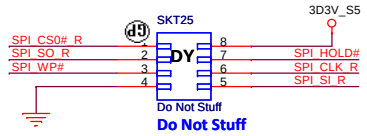
Size: A2 | Document Number: Latitude300 Haswell | Rev: X00

Date: Friday, March 15, 2013 | Sheet 24 of 104

SSID = Flash.ROM

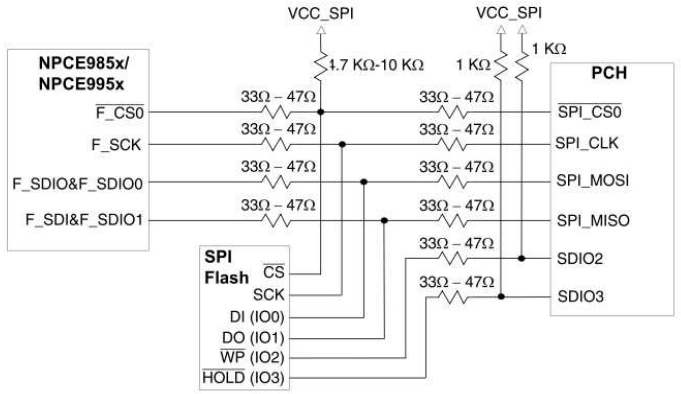
SPI Flash ROM(8M) for PCH





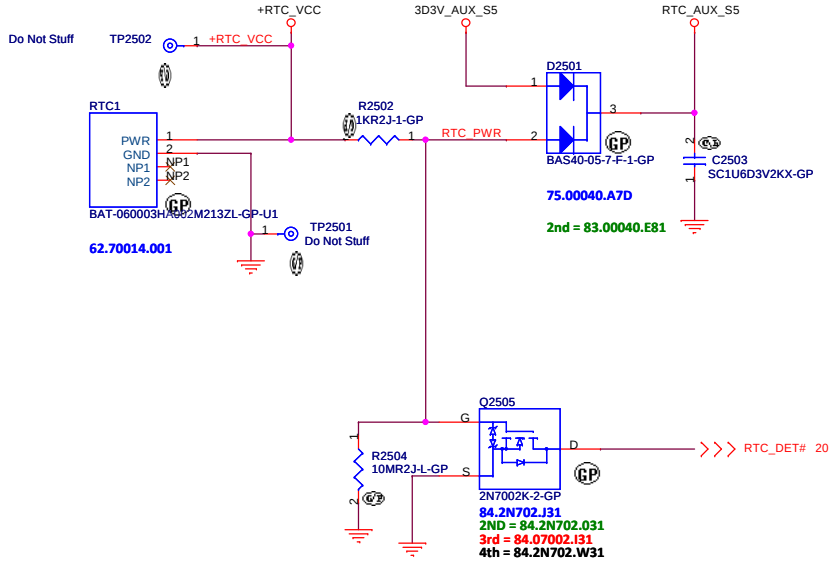
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25Q64.F01	O	O
72.25Q64.D01	O	O

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT



UM

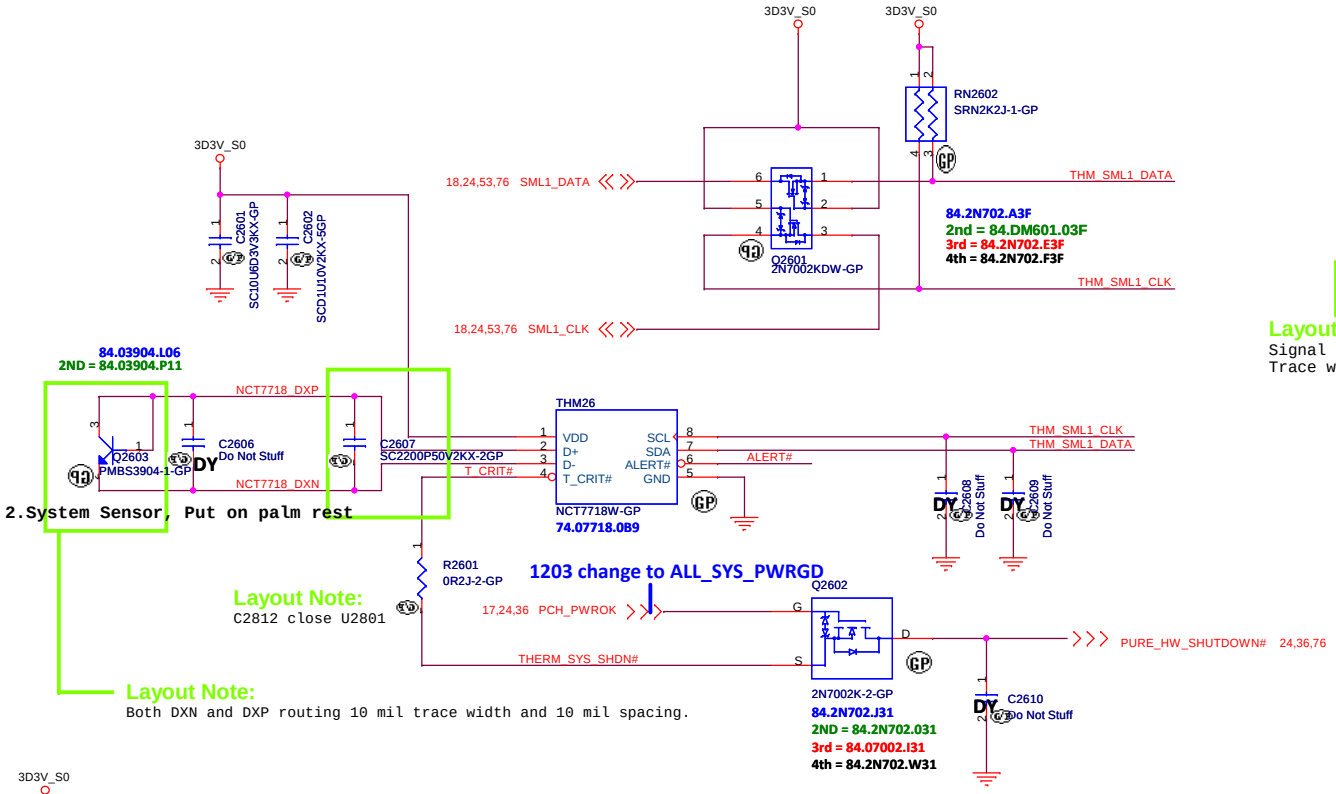
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

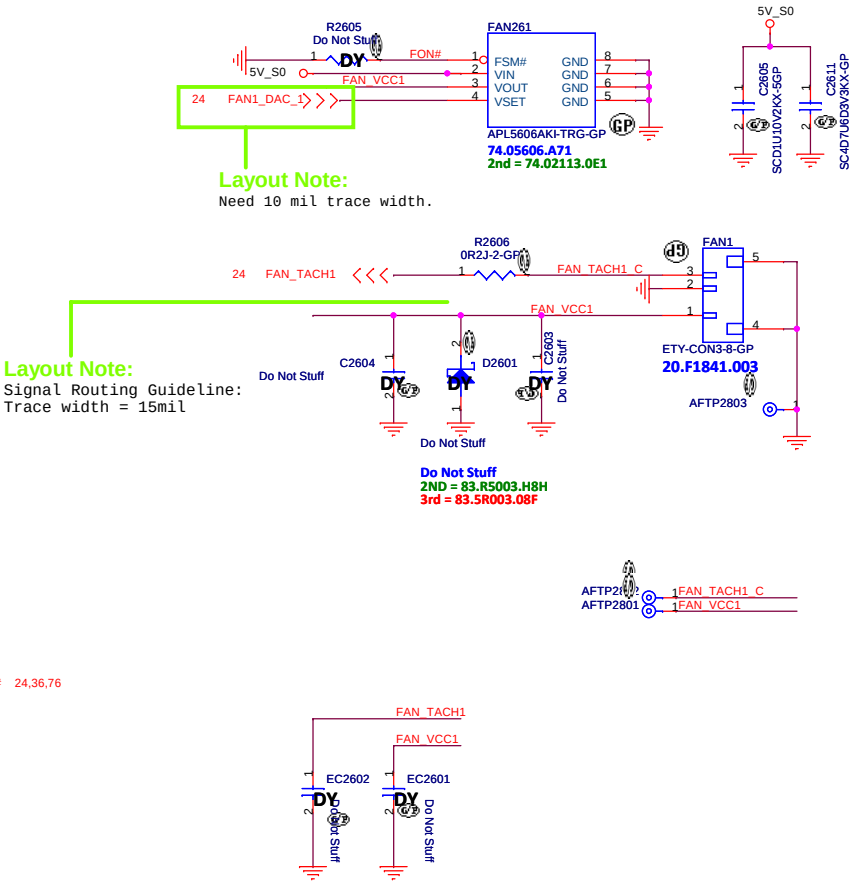
Size: A3 | Document Number: Latitude300 Haswell | Rev: X00

Date: Friday, March 15, 2013 | Sheet 25 of 104

SSID = Thermal



Fan controller1



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

UM

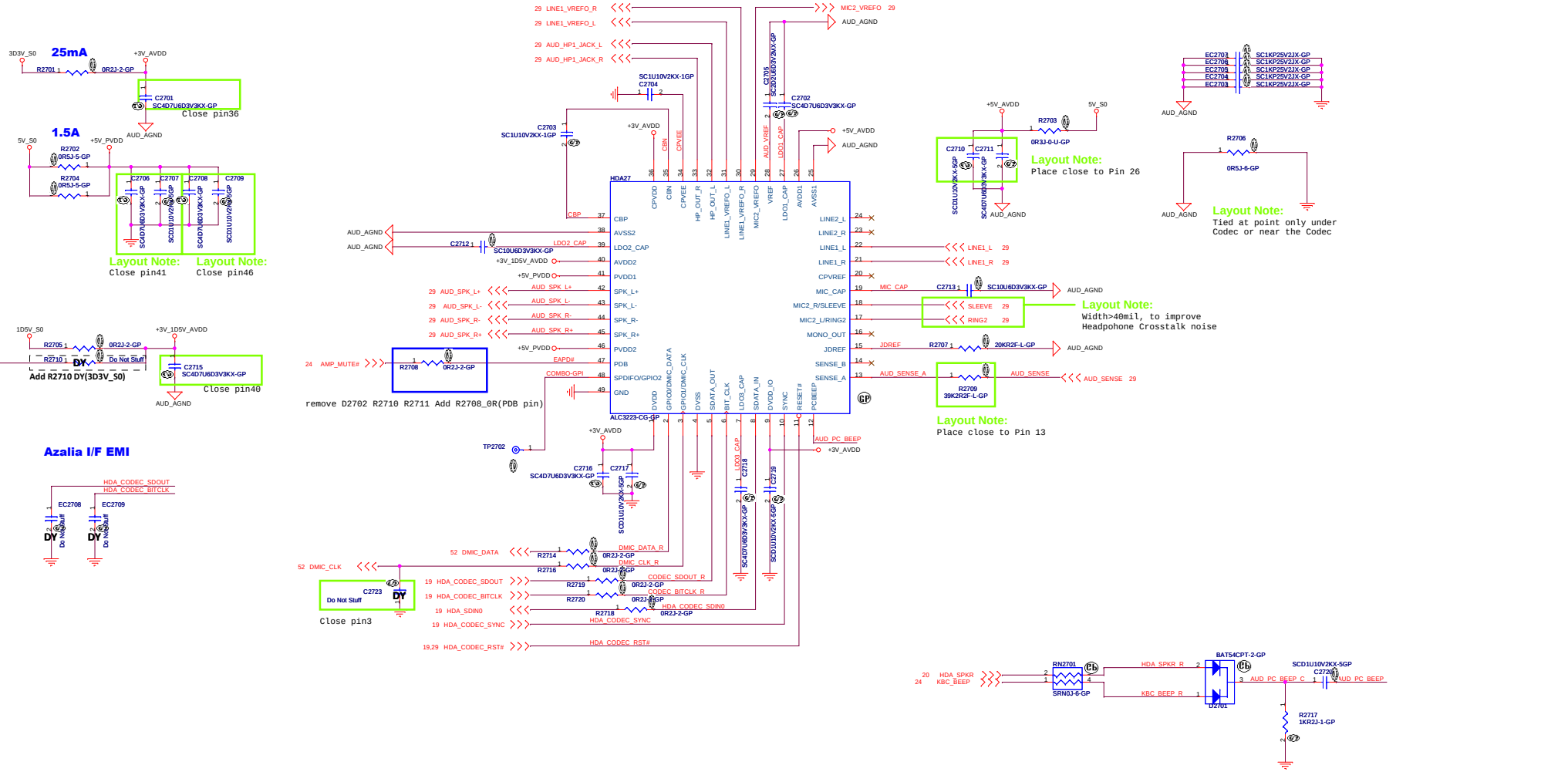
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

Size: A3 | Document Number: Latitude300 Haswell | Rev: X00

Date: Friday, March 15, 2013 | Sheet 26 of 104

SSID = AUDIO



UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3221

Size	Document Number	Rev
A2	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 27 of 104

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

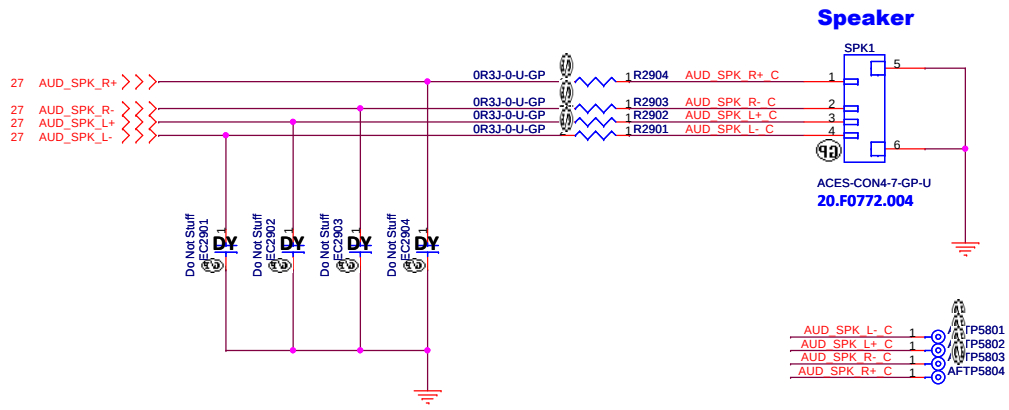
Title: ***Reserved***

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

Date: Friday, March 15, 2013 Sheet 28 of 104

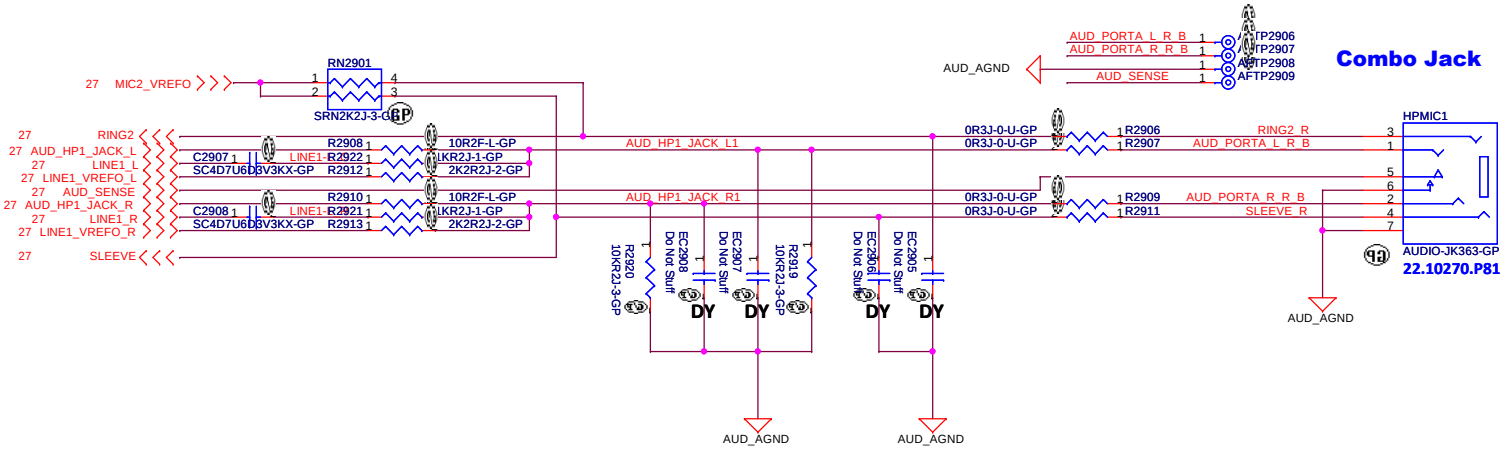
SSID = AUDIO

Speaker

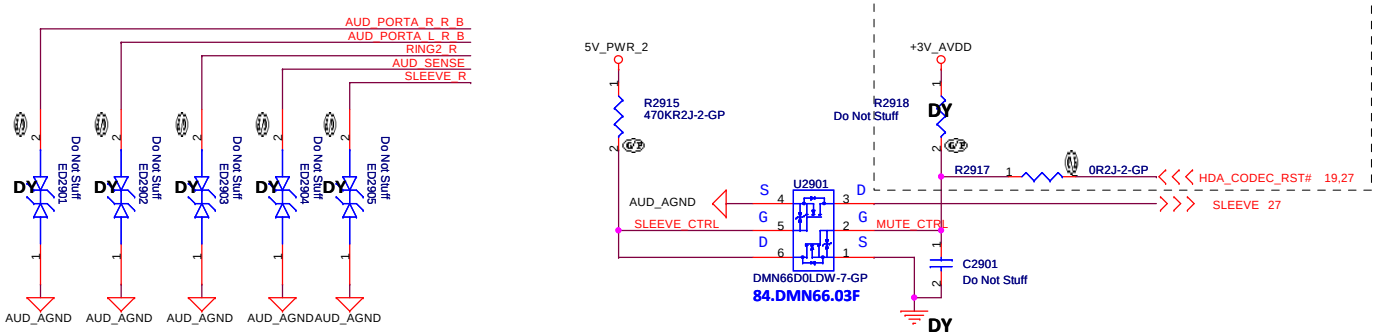


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L_

Combo Jack



1227 modify



UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal NCT7718W/Fan Controllor P2793*

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 29 of 104

LAN CHIP

10/100 Need Only need C3021, C3022, C3023, C3024 in Pin3, 8, 22, 30

X5R

40 mils

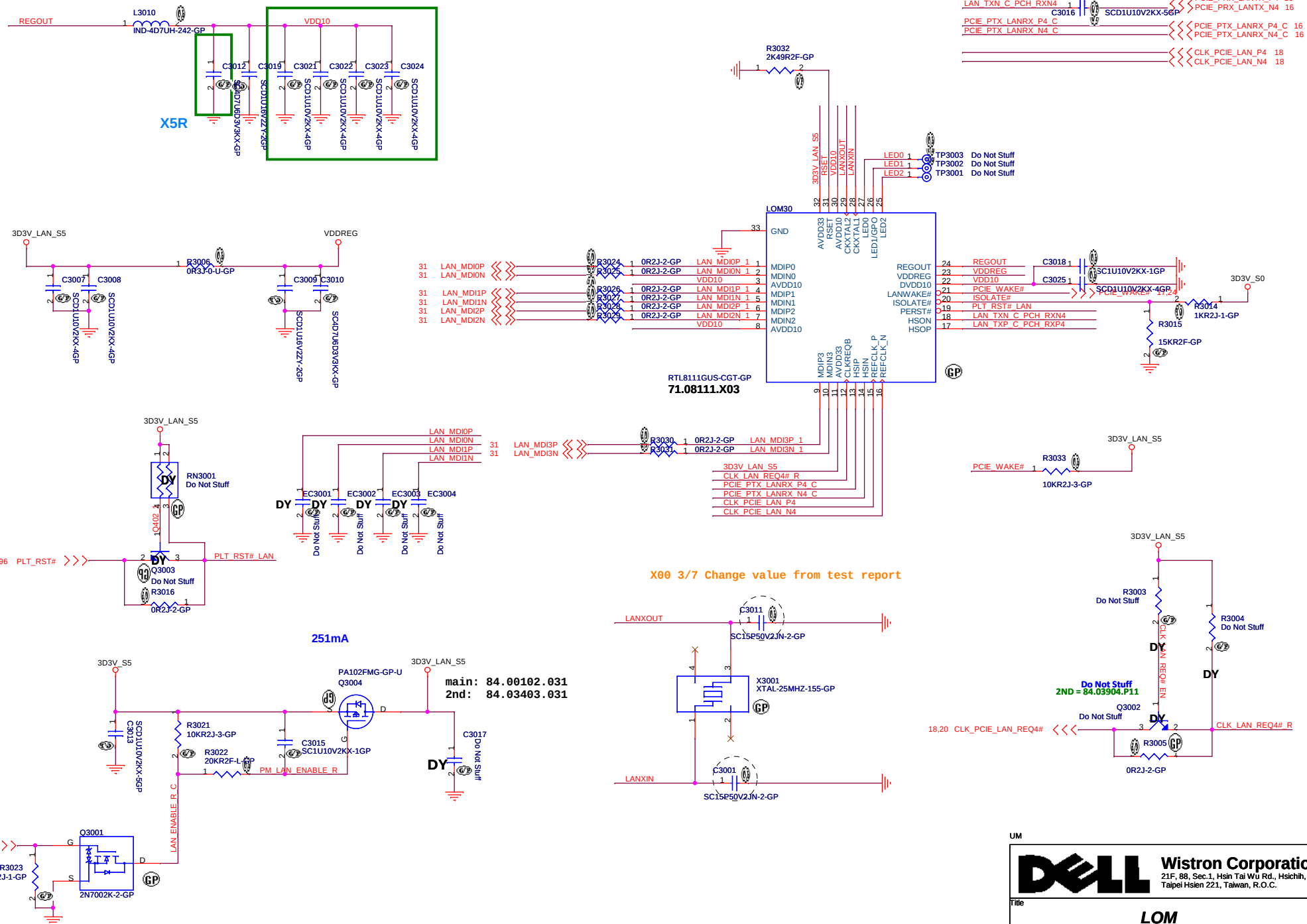
251mA

X00 3/7 Change value from test report

main: 84.00102.031
2nd: 84.03403.031

RTL8111GUS-CGT-GP
71.08111.X03

Do Not Stuff
2ND = 84.03904.P11



UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

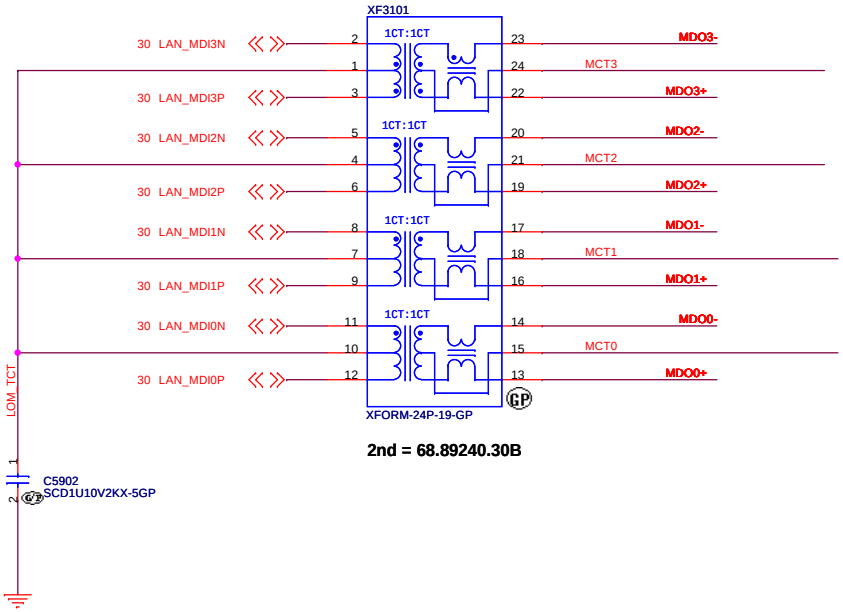
Title: **LOM**

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

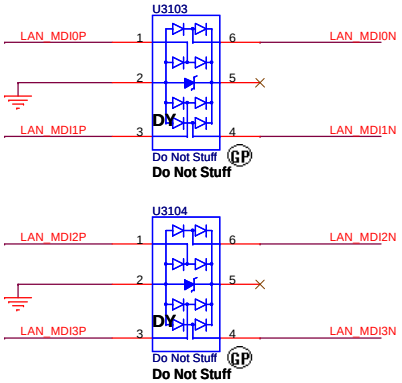
Date: Friday, March 15, 2013 Sheet 30 of 104

SSID = LOM

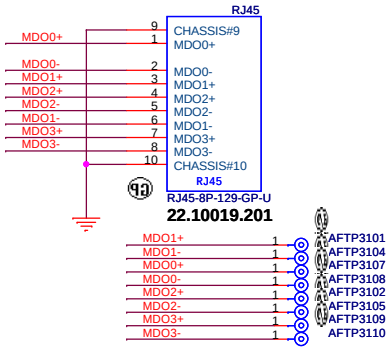
100/GIGA LAN TransFormer

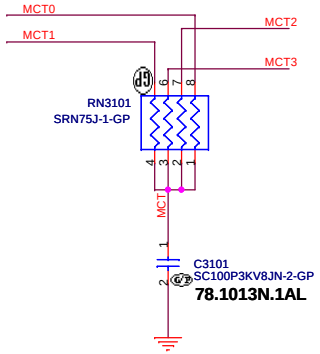


2nd = 68.89240.30B



RJ45 CONN



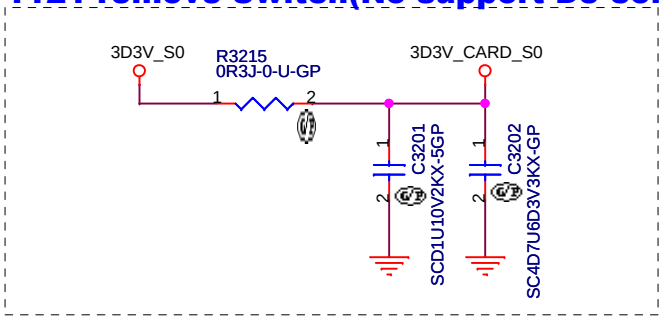


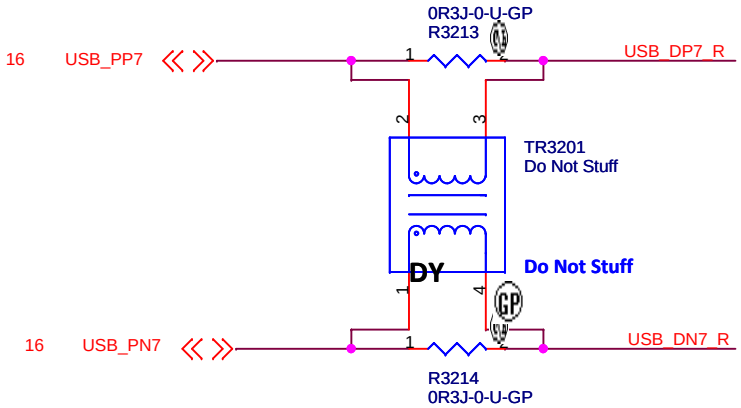
UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

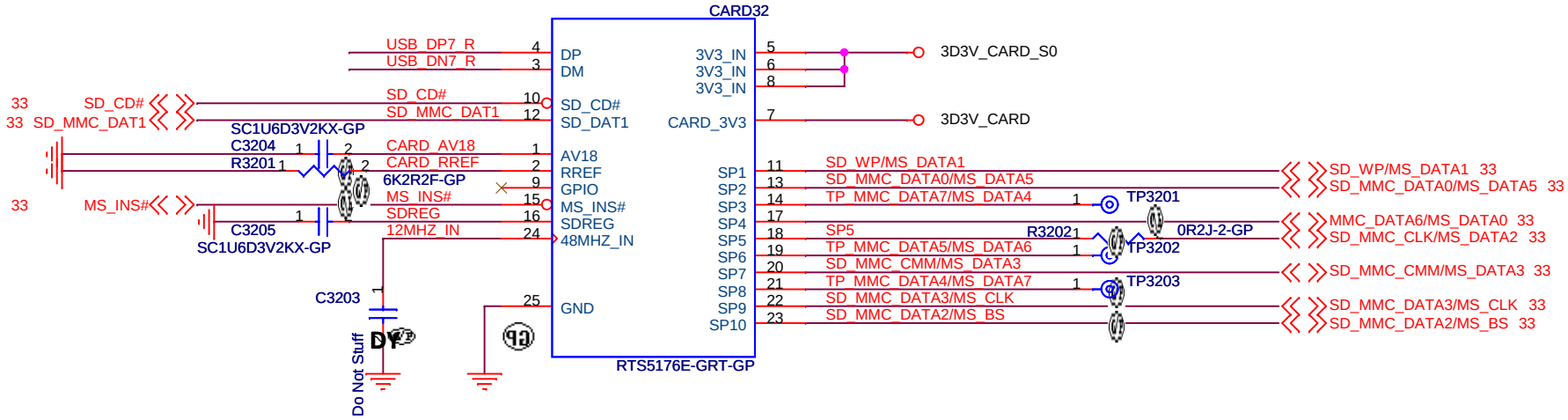
Title		
XFOM&RJ45		
Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet 31 of 104	

1121 remove Switch(No support D3 cold)





Pin name	Net name
SD_DAT1	SD_MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD_MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD_MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD_MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD_MMC_DATA3/MS_CLK
SP10	SD_MMC_DATA2/MS_BS



UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

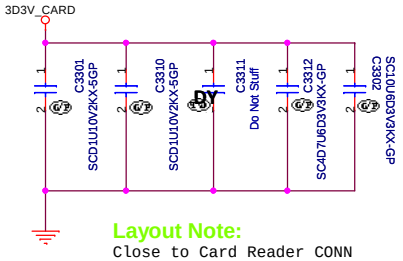
Card Reader-RTS5176

Size	Document Number	Rev
A4	*Latitude300 Haswell*	*X00*

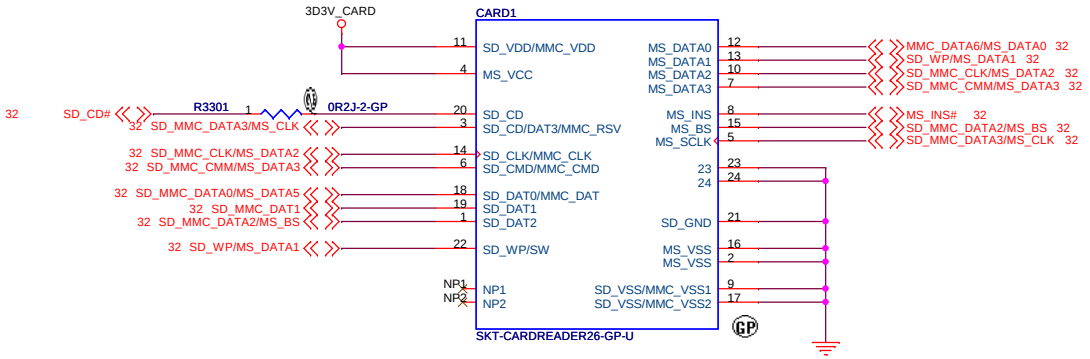
Date: Friday, March 15, 2013 Sheet 32 of 104

SSID = SDIO

SD/MS/MMC Card Connector

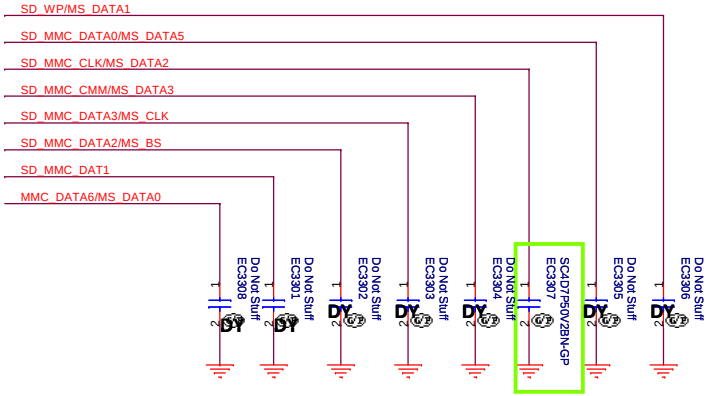


Layout Note:
Close to Card Reader CONN



62.10051.C21

For EMI Reserved



Layout Note:
please close U3201

1203 modify 10P change to 4.7P

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

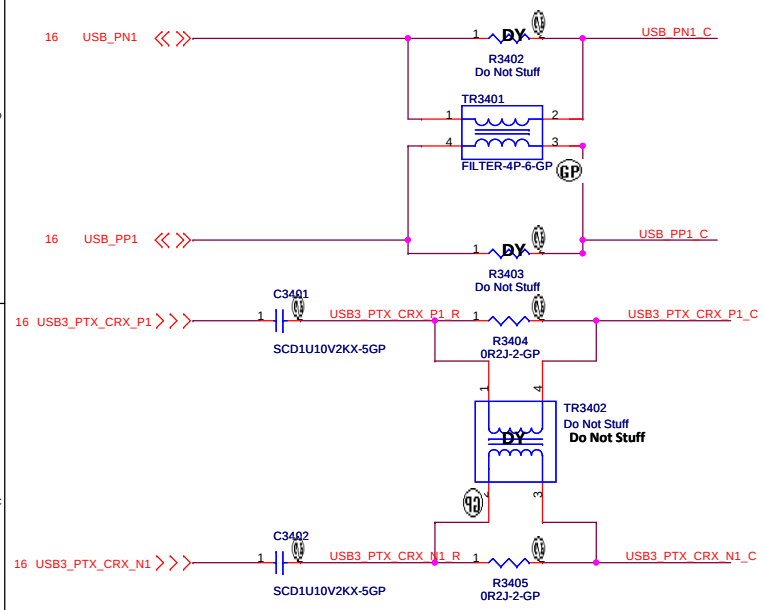
Title: SD/XD/MS/MMC Card CONN

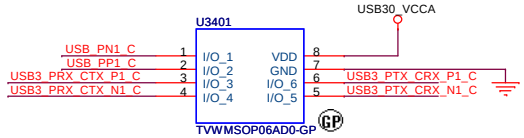
Size	Document Number	Rev
A3	Latitude300 Haswell	X00

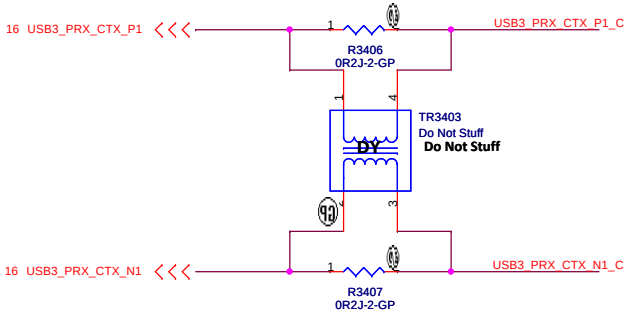
Date: Friday, March 15, 2013 Sheet 33 of 104

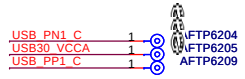
SSID = USB

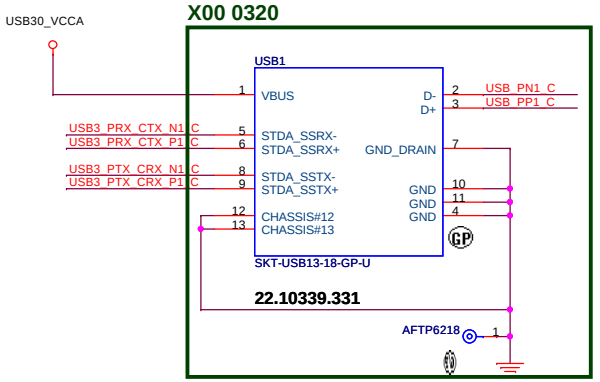
USB3.0 Port1



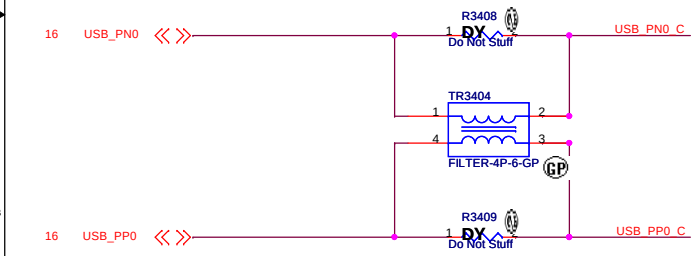


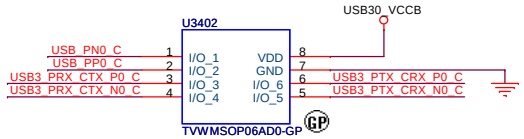


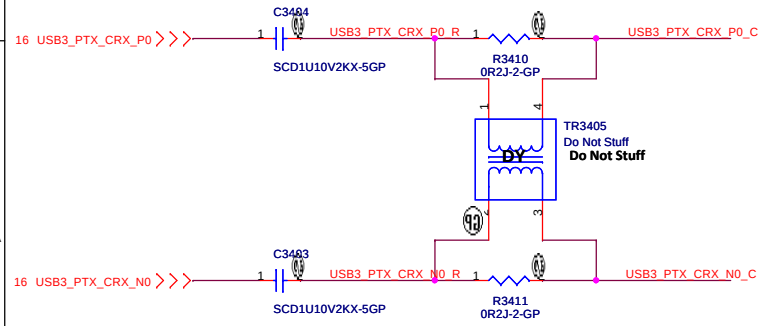


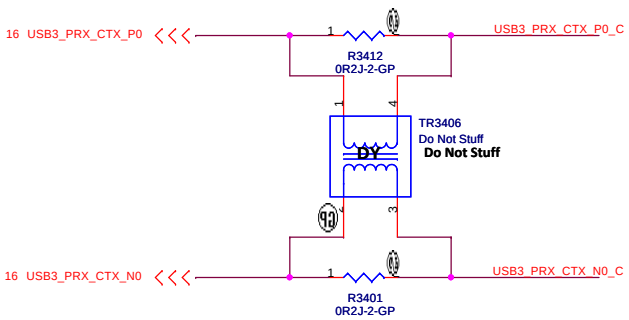


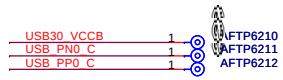
USB3.0 Port2

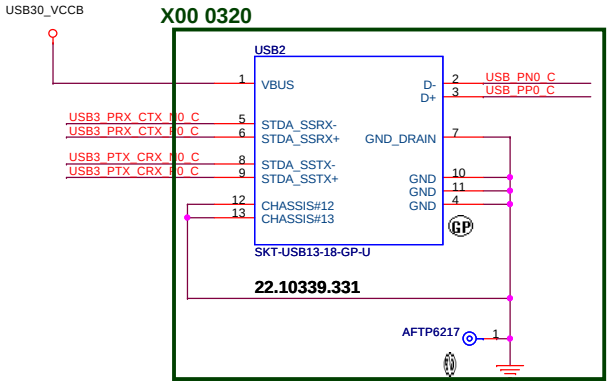












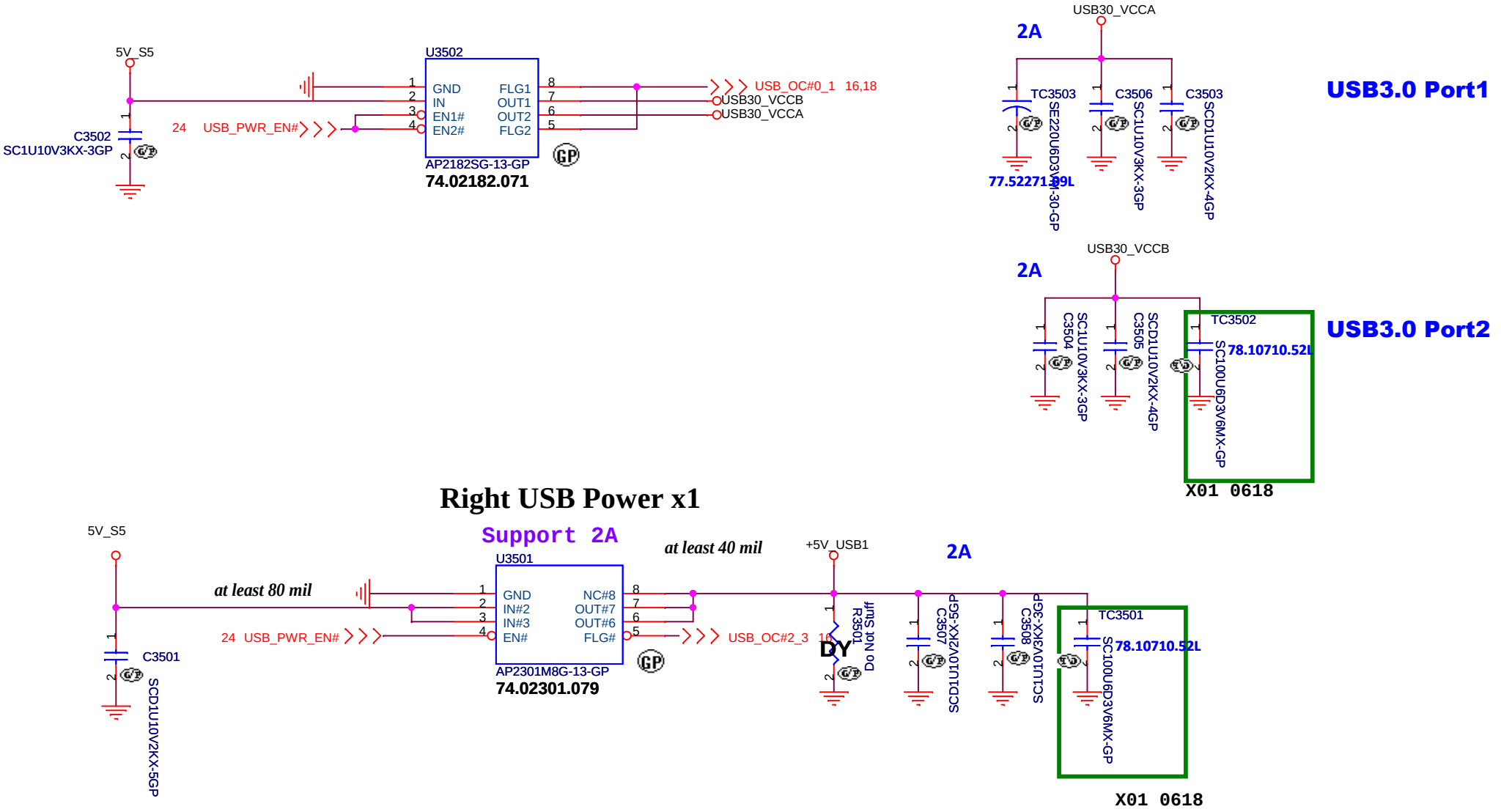
UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0***

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

Date: Friday, March 15, 2013 Sheet 34 of 104



UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

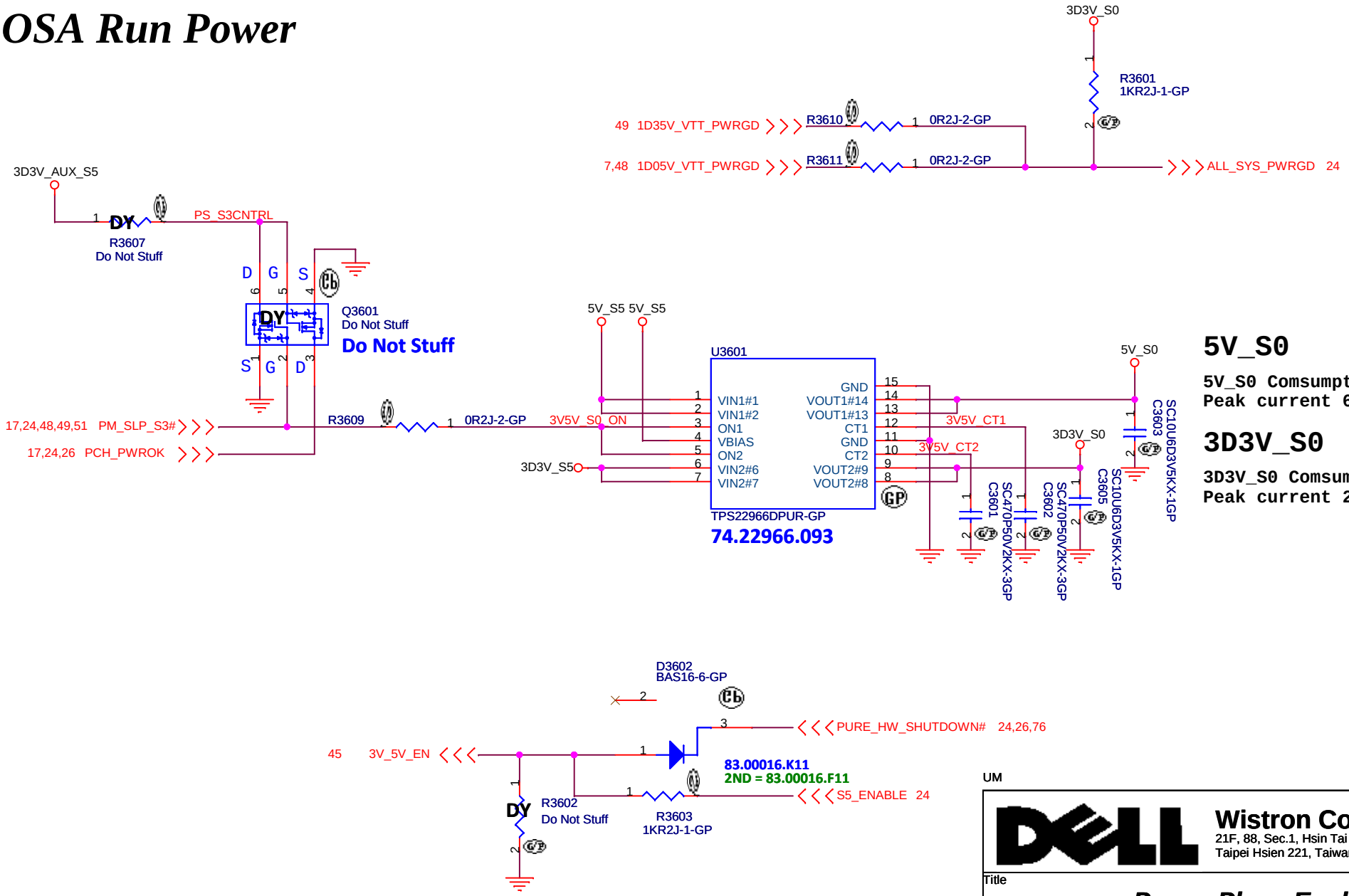
Size	Document Number	Rev
	Latitude300 Haswell	***X00***

Date: Friday, March 15, 2013 Sheet 35 of 104

SSID = Reset.Suspend

Power Good

ROSA Run Power



UM

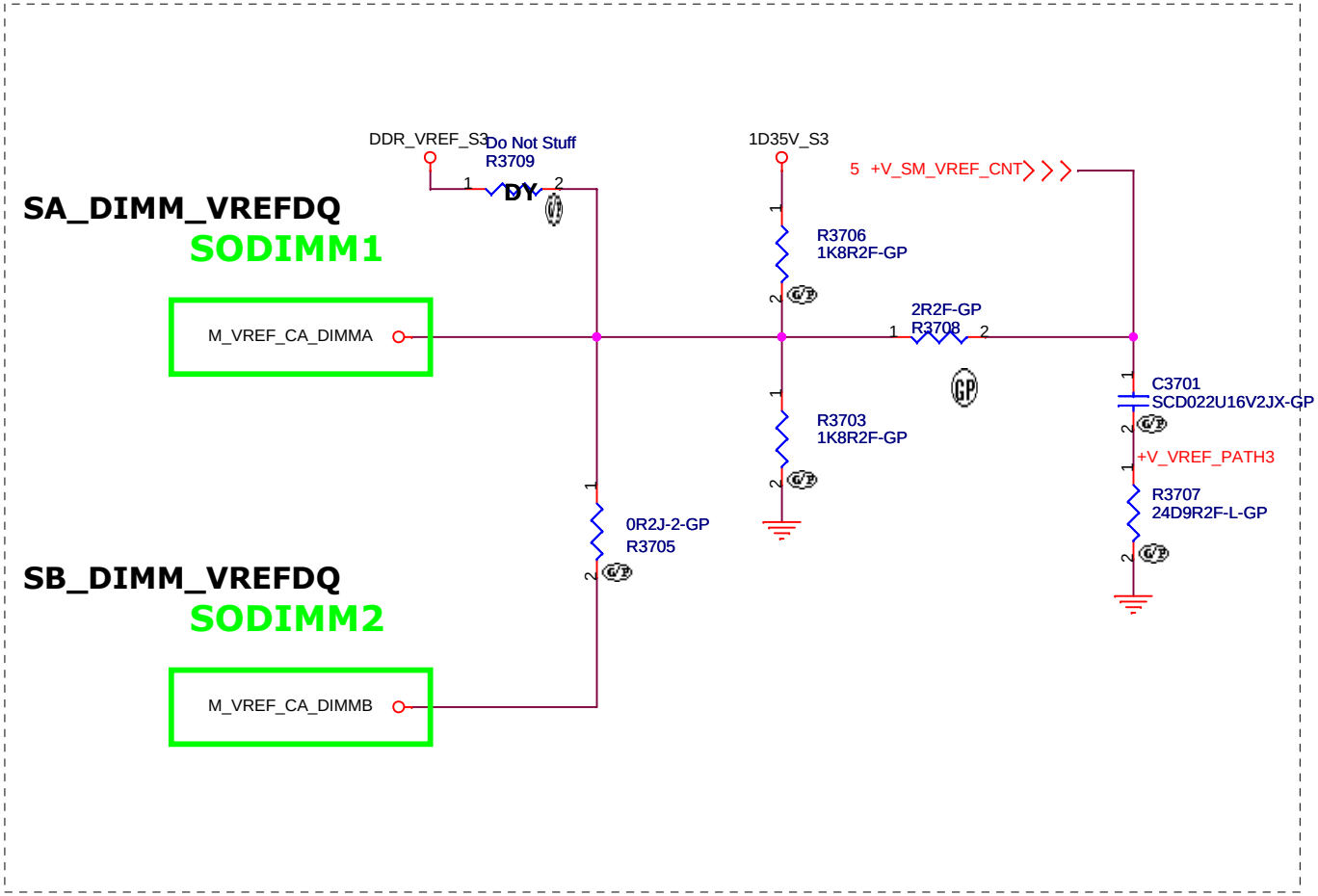
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Plane Enable***

Size	Document Number	Rev
A4	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 36 of 104

Layout Note:
Place Close SO-DIMM



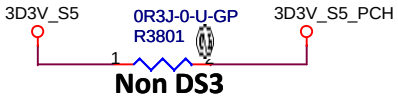
UM

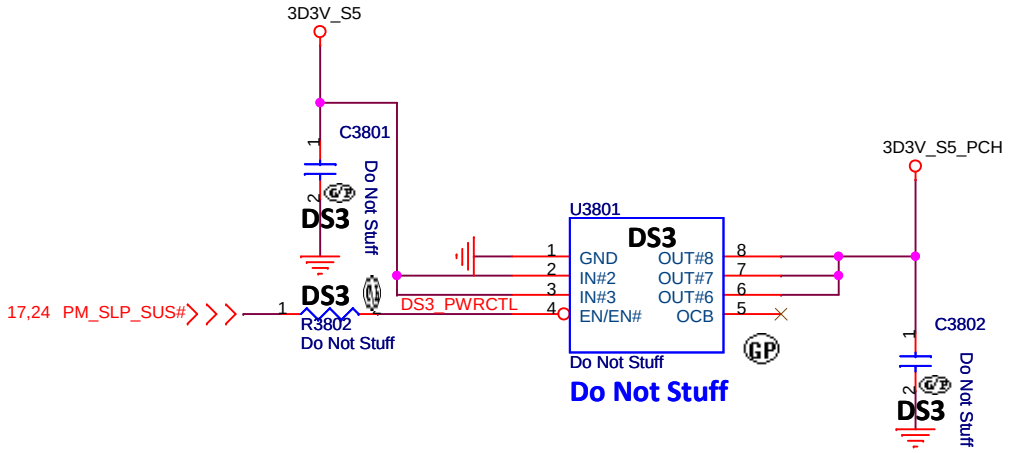
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
S3 Reduction Circuit

Size	Document Number	Rev
A4	**Latitude300 Haswell**	X00

Date: Friday, March 15, 2013 Sheet 37 of 104





1210 change power switch (RdsON:100m ohm)

UM

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DSW*		
Size: A4	Document Number: *Latitude300 Haswell*	Rev: *X00*
Date: Friday, March 15, 2013	Sheet 38 of 104	

SSID = CPU

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (POWER1)*

Size: Custom | Document Number: *Latitude300 Haswell* | Rev: *X00*

Date: Friday, March 15, 2013 | Sheet 39 of 104

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	***Latitude300 Haswell***	***X00***

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

SSID = PWR.Support

Layout Note:
PSID Layout width > 25mil

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

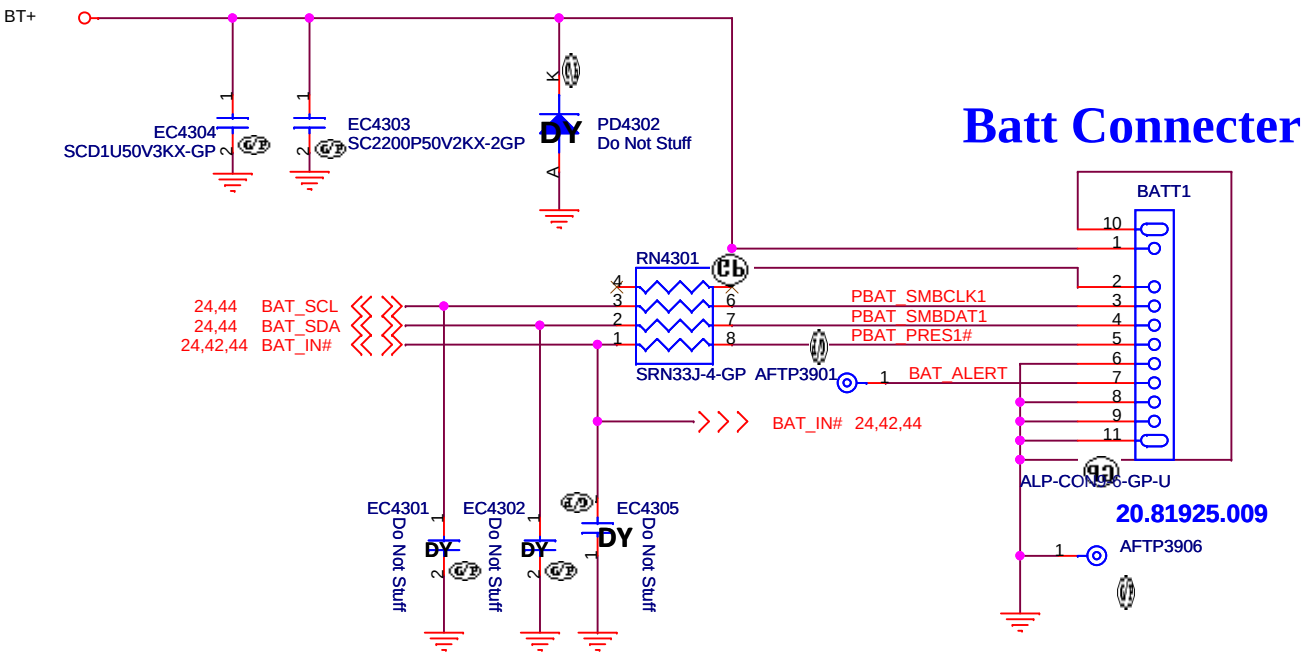
Id=-9.6A
Qg=-25nC
Rdson=18~30mohm

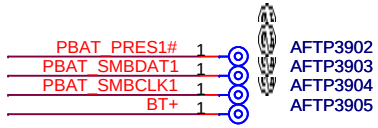
DT MODE

Title	DCIN
Size	A3
Document Number	Latitude300 Haswell
Rev	X00
Date	Friday, March 15, 2013
Sheet	42 of 104

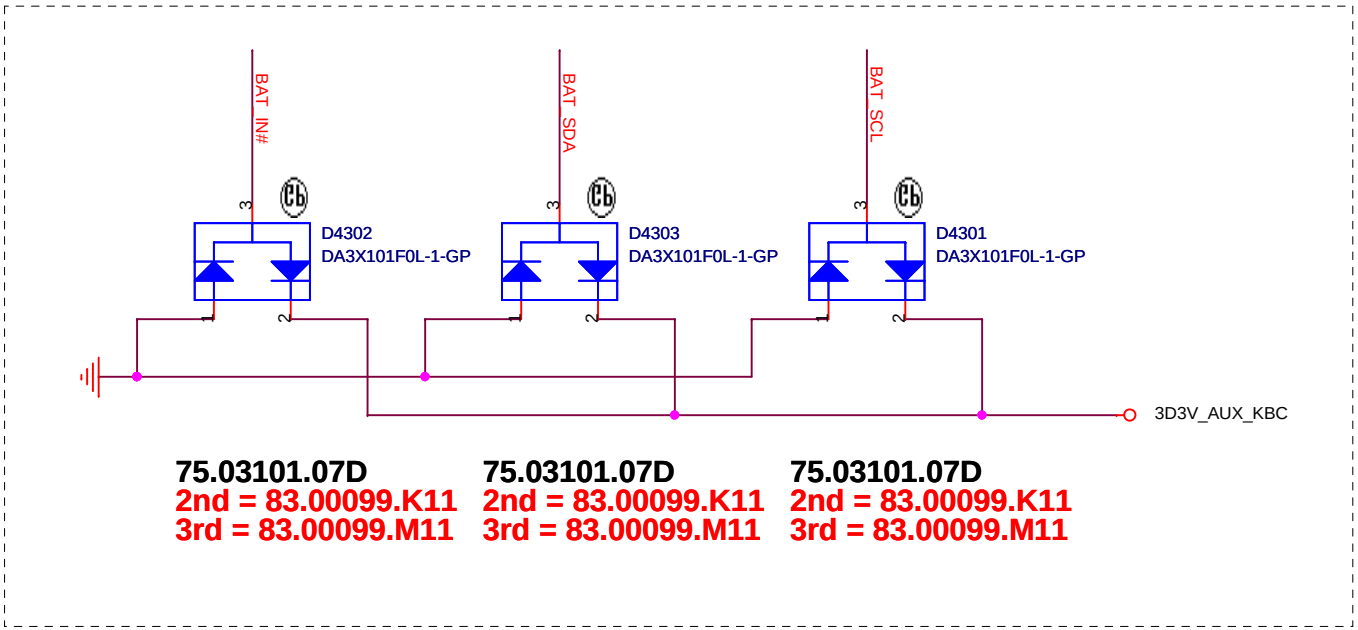
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

SSID = PWR.Support





Placement: Close to Batt Connector



75.03101.07D
2nd = 83.00099.K11
3rd = 83.00099.M11

75.03101.07D
2nd = 83.00099.K11
3rd = 83.00099.M11

75.03101.07D
2nd = 83.00099.K11
3rd = 83.00099.M11

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

Size	Document Number	Rev
A4	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 43 of 104

SSID = Charger

REGN REGULATOR						
VREGN_REG	REGN Regulator Voltage	VVCC > 6.5V, VACDET>0.6V (0-50mA load)	5.5	6	6.5	V

KBC FOR DT MODE
CHECK EE PULL HIGH

VacDET=2.4V
Acok setting=2.4*((PR4444+PR4411)/PR4411)
Setting=18.178v

ACAV_IN
H=ACIN
L=UNAC

DIS_DTM:
H= cell is plus to GND. (reset charger ic)
L=nornal

PWR_CHG_ACOK:
PWR_CHG_REGN=6V
V+=6*(PR4404/(PR4410+PR4404))=3.27V

PWR_CHG_CMPIN:
V-=3.3*(PR4402/(PR4428+PR4402))=1.1099V

Close PR4443

PU4406 and PU4407:
main source: 84.03660.037

X01 3/07 Power modify

CHECK EE

CHECK PM BATTERY TYPE
CHECK CELL for DT mode

BATTERY MON

Follow customer circuits

X01 3/1 Power modify

CHECK PM ADAPTER TYPE
And setting adapter type

X01 3/1 Power modify

X01 3/4 Power modify

(AD_IA_HW)

(AD_IA_HW_2)

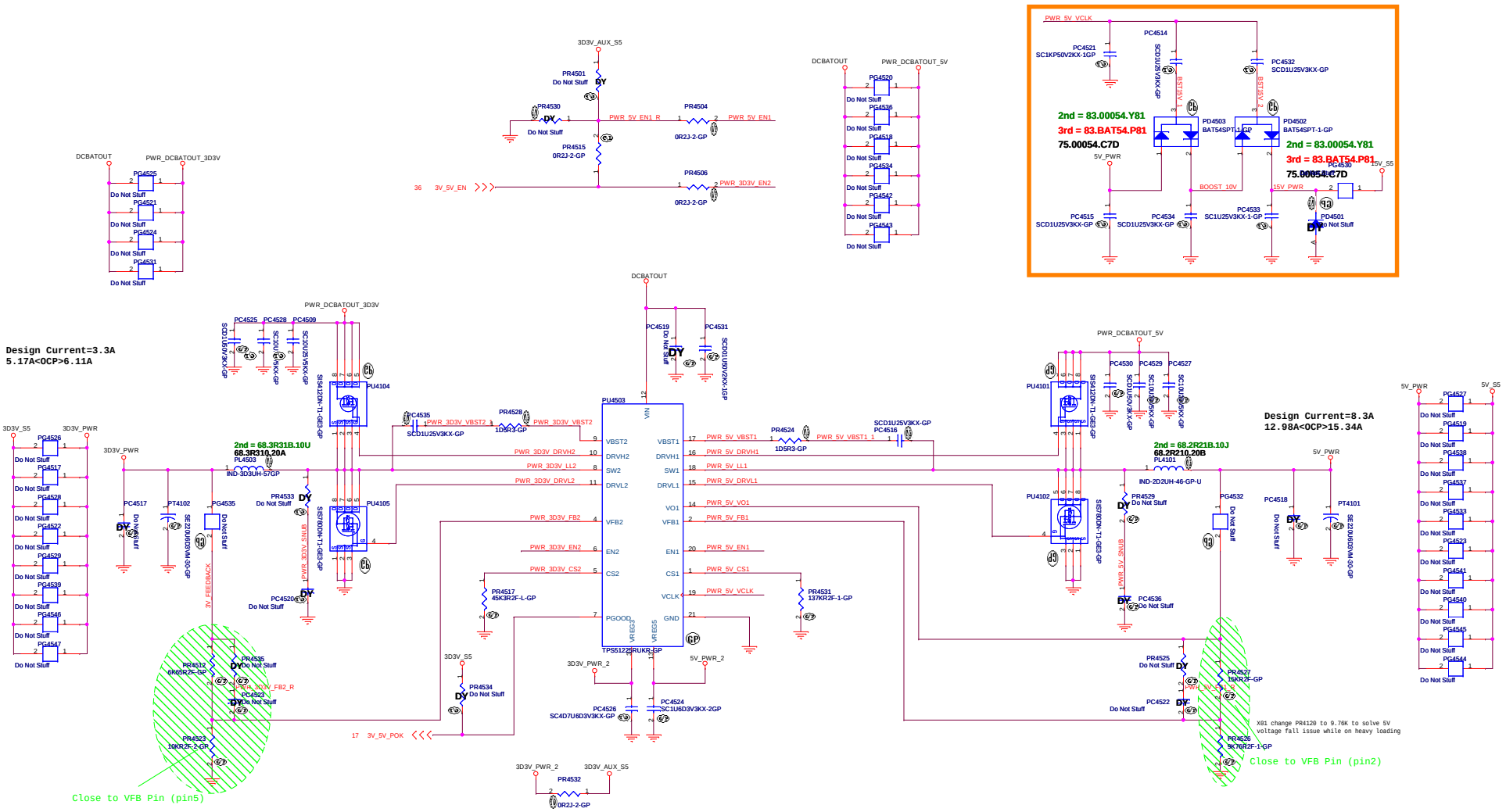
DIS_DTM_HW:
5V_S5
V+=5*(PR4440/(PR4460+PR4440))=2.73V
Setting=2.73*((PR4442+PR4447)/PE4447)=9V

CHECK EE
follow customer circuits.

ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329V
45W	L	H	0.659648V

UM	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	CHARGER BQ24717		
Size: Custom	Document Number: Latitude300 Haswell		Rev: X00
Date: Friday, March 15, 2013	Sheet 44 of 104		

SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
PR4510	45.3KK	9.09K
PR4511	110K	22.1K

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

UM

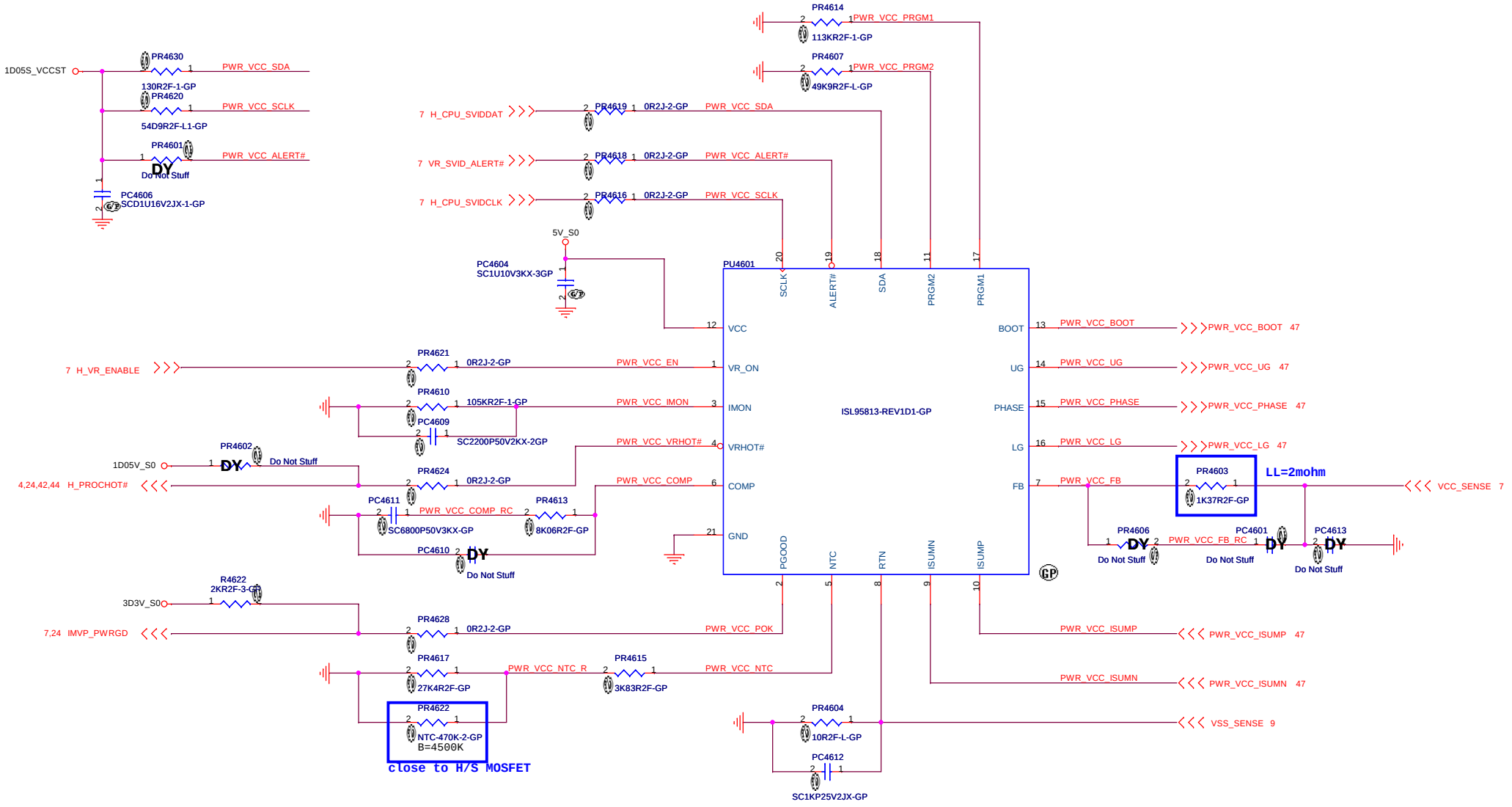
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3V/5V TPS51225

Size	Document Number	Rev
A2	Latitude300 Haswell	X00

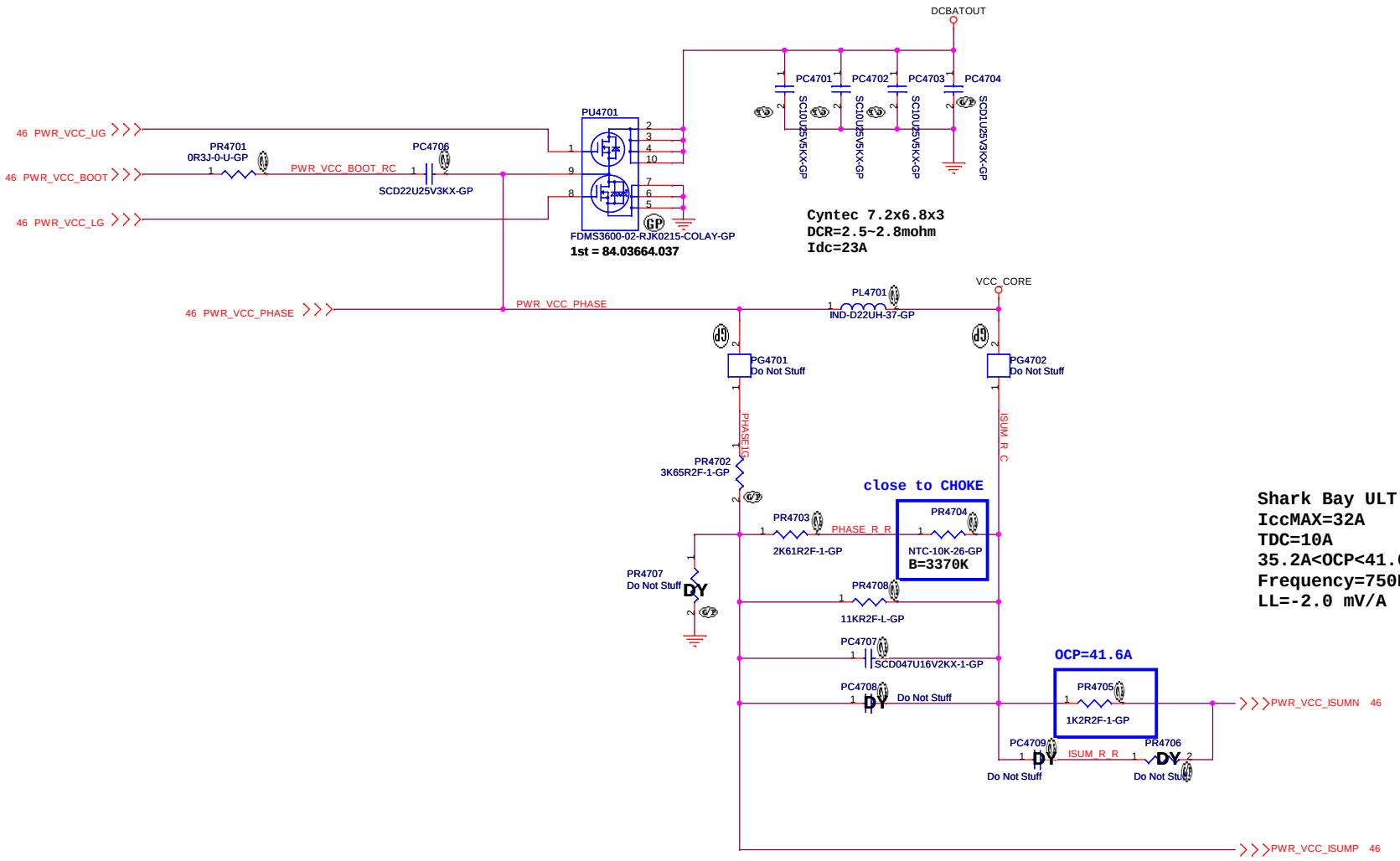
Date: Friday, March 15, 2013 Sheet 45 of 104

SSID = CPU.Regulator



UM

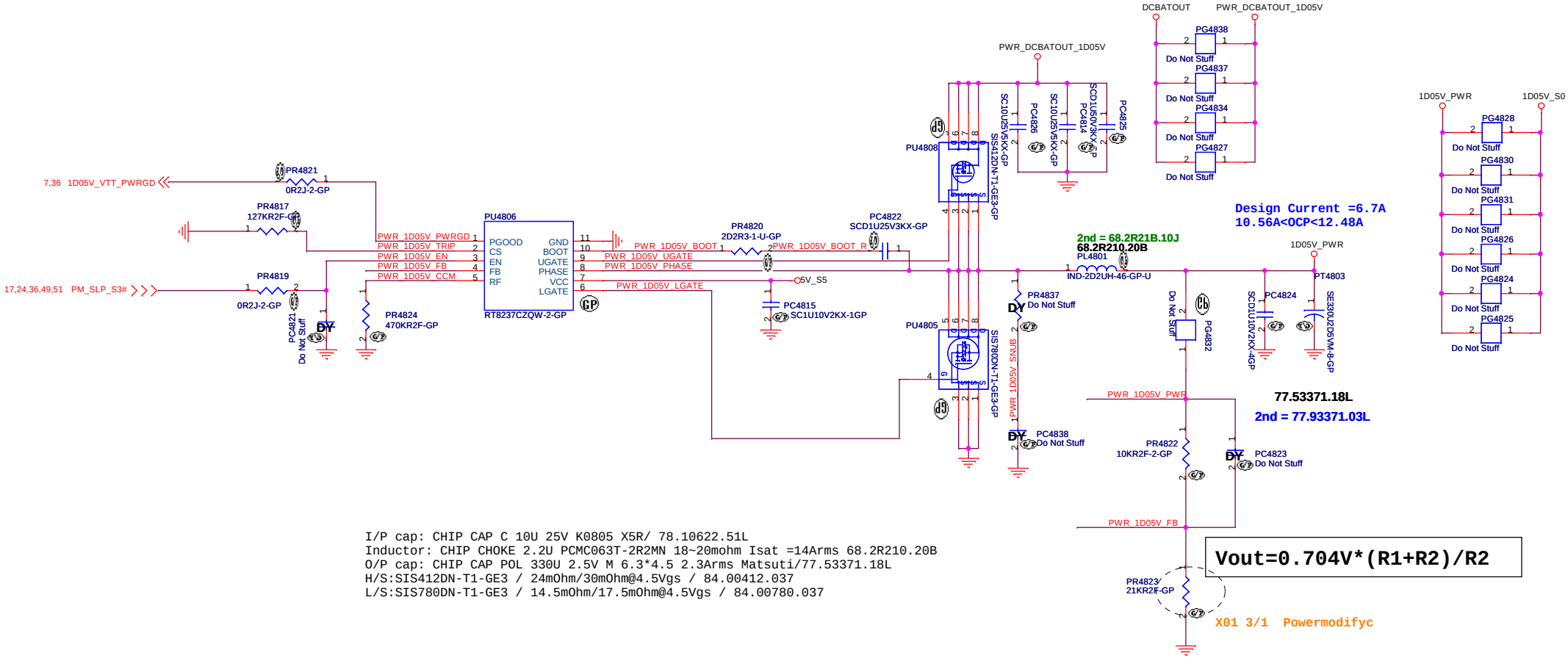
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *TPS51622_CPUCORE(1/2)*		
Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet 46 of 104	



UM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TPS51622_CPUCORE(2/2)		
Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet 47 of 104	

SSID = PWR.Plane.Regulator_1p05v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

Vout=0.704V*(R1+R2)/R2

X01 3/1 Powermodifyc

UM

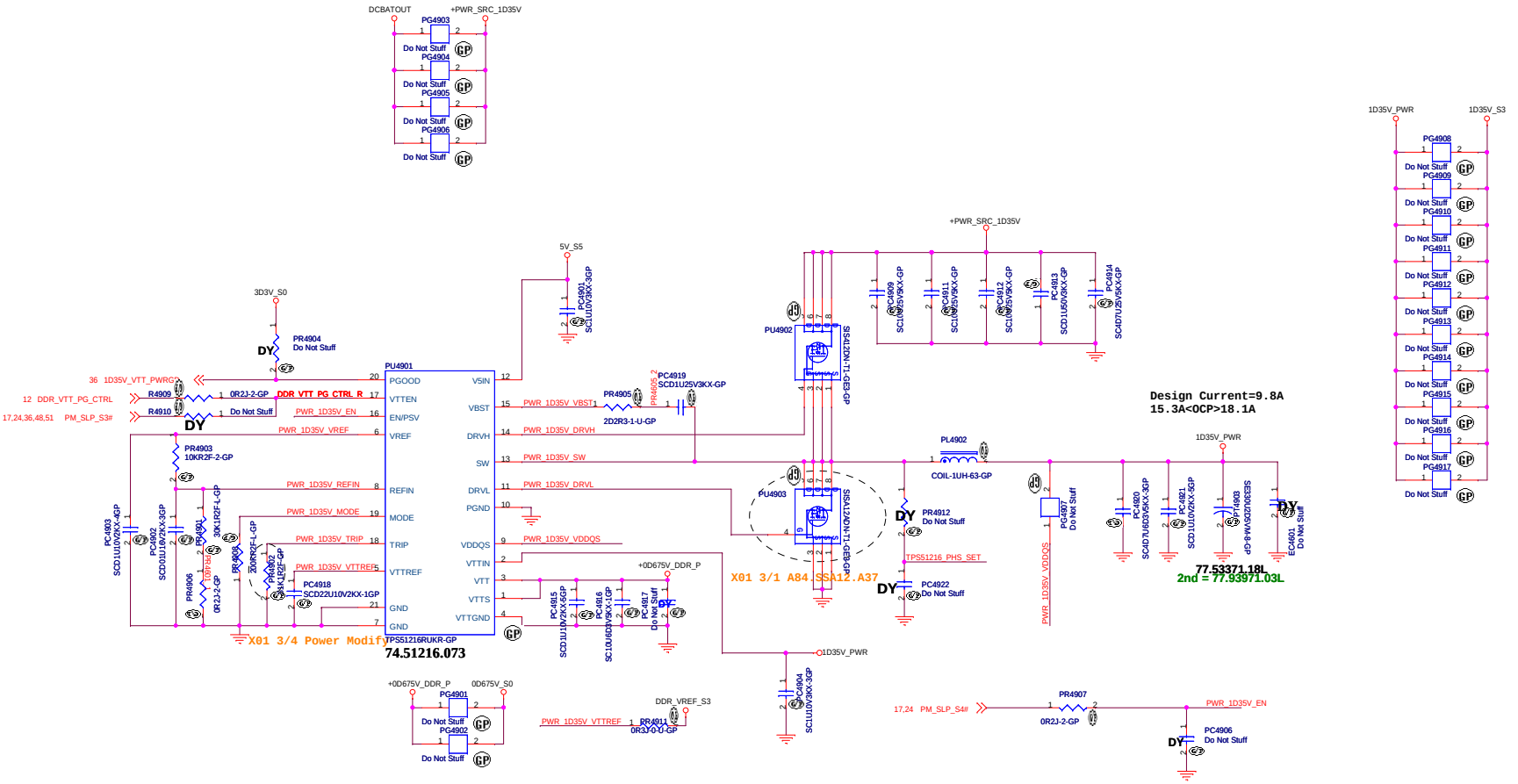
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51367_1D05V***

Size	Document Number	Rev
A3		X00

Date: Friday, March 15, 2013 Sheet 48 of 104

SSID = PWR.Plane.Regulator_1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.1UH M PCMC063T-R10MN 1.5~1.7mohm Isat =60Arms 68.R1010.10T
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S MOS: FET MOS SIS412DN-T1-GE3 NC 8P / 84.00412.037 / Rds(on)=24~30mohm @Vgs=4.5V
L/S MOS: FET MOS SIS780DN-T1-GE3 NC POWERPAK 121 / 84.00780.037 / Rds(on)=14.5~17.5mohm @Vgs=4.5V

UM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51367+51206_1D35V & 0D675V

Size: C | Document Number: Latitude300 Haswell | Rev: X00

Date: Friday, March 15, 2013 | Sheet 49 of 104

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

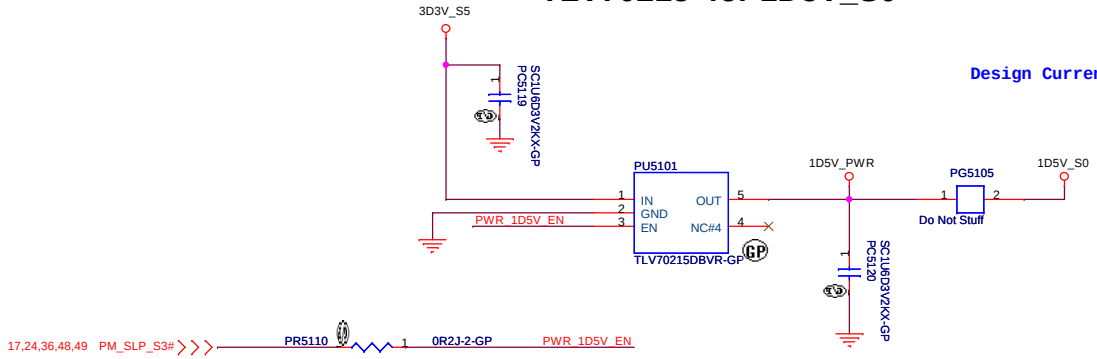
Reserved

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

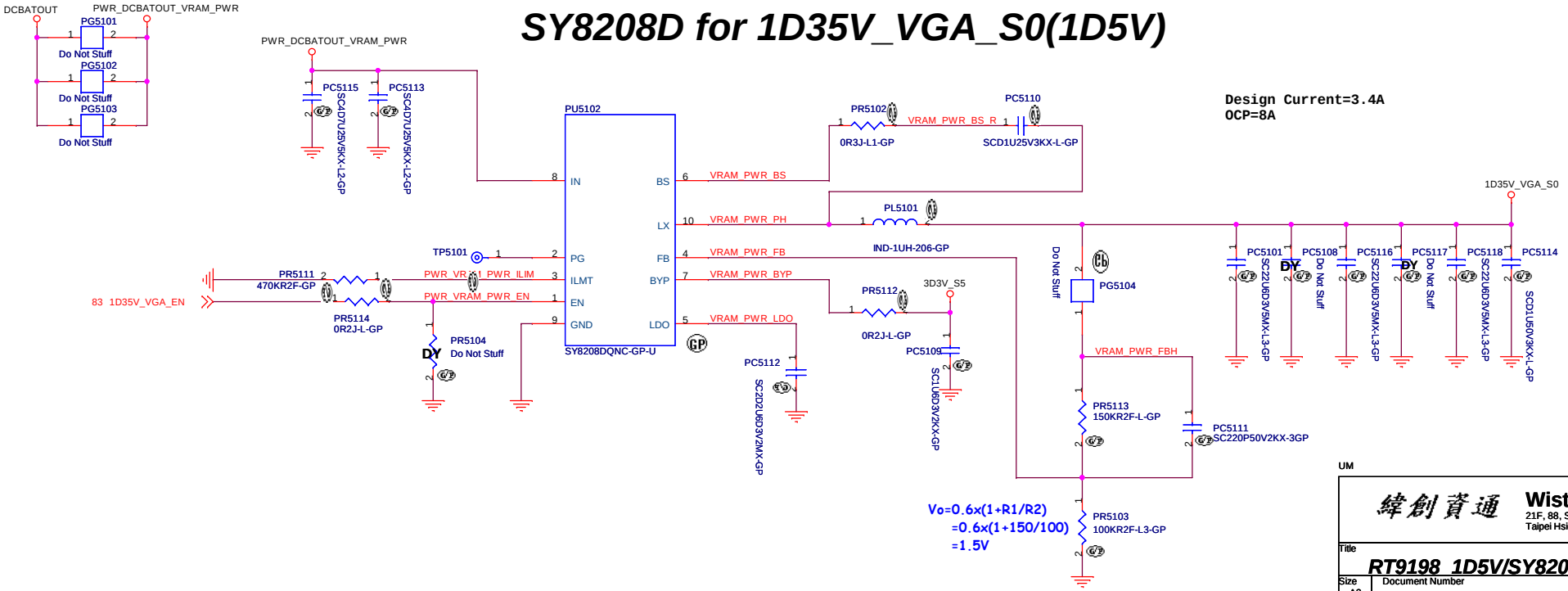
Date: Friday, March 15, 2013 Sheet 50 of 104

SSID = PWR.Plane.Regulator_1p5v

TLV70215 for 1D5V_S0



SY8208D for 1D35V_VGA_S0(1D5V)



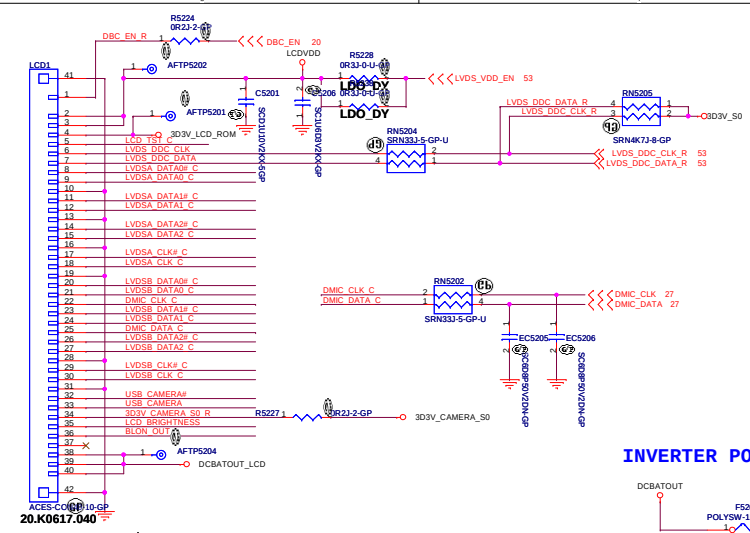
UM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9198_1D5V/SY8208D_1D5V(VGA)

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

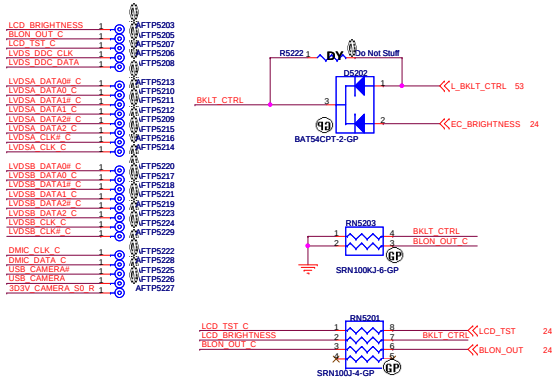
Date: Friday, March 15, 2013 Sheet 51 of 104



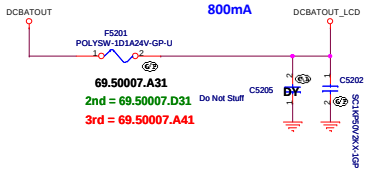
CN Table	
1	Diag_loop
2	USB+
3	USB-
4	3.3V
5	MIC_CLK
6	MIC_GND
7	MIC_SIG
8	DGND

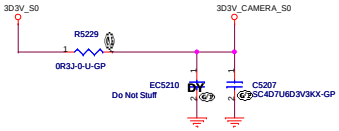
MB Connecter		是否接線	Wire (40 PIN)	FFC(40 PIN)
Pin 10	GND	Y	Pin 10(GND 實體線)	Pin 10 GND
Pin 13	GND	Y	Pin 13(GND 實體線)	Pin 13 GND
Pin 16	GND	Y	Pin 16 (GND實體線)	Pin 16 GND
Pin 19	GND	Y	Camera Module Pin 6 DMIC_GND(實體線)	Pin 19 GND
Pin 22	GND	Y	Camera Module Pin 5 AUD_DMIC_CLK	Pin 22 GND
Pin 25	GND	Y	Camera Module Pin 7 AUD_DMIC_IN0	o
Pin 28	GND	Y	Camera Module Pin 8 CCD GND(實體線)	Pin 28 GND
Pin 31	GND	Y	Pin 31 (實體線)	Pin 31 GND
Pin 32	GND	Y	Camera Module Pin 3 USB_CAMERA#	Pin 32 GND
Pin 33	GND	Y	Camera Module Pin 2 USB_CAMERA	Pin 33 GND
Pin 34	3D3V_CAMERA_S0	Y	Camera Module Pin 4 3D3V_CAMERA_S0	NC(0 ohm DY)

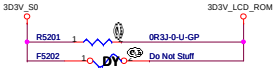
PIN	MB Connecter	是否接線	PIN	Camera Module Conn
1	DGND	Y	8	DGND
2	USB_CAMERA_C (USB+)	Y	2	USB_CAMERA_C (USB+)
3	USB_CAMERA#_C (USB-)	Y	3	USB_CAMERA#_C (USB-)
4	DMIC_GND	Y	6	DMIC_GND
5	DMIC_CLK_C	Y	5	DMIC_CLK_C
6	DMIC_DATA_C	Y	7	DMIC_DATA_C
7	NC	N	1	NC
8	3D3V_CAMERA_S0	Y	4	3D3V_CAMERA_S0



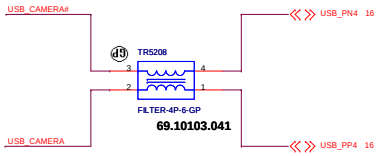
INVERTER POWER

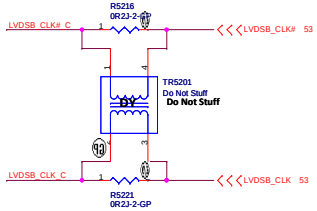


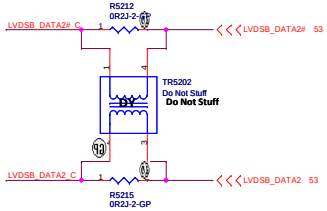


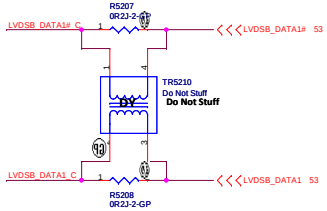


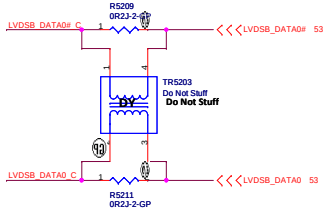
Close to LCD connector

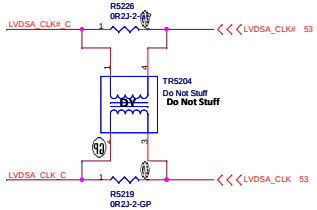


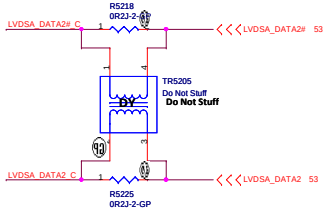


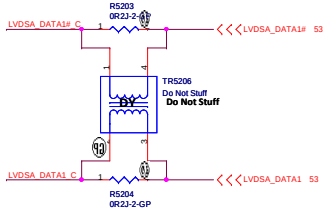


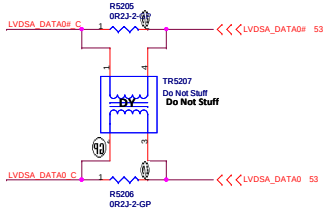




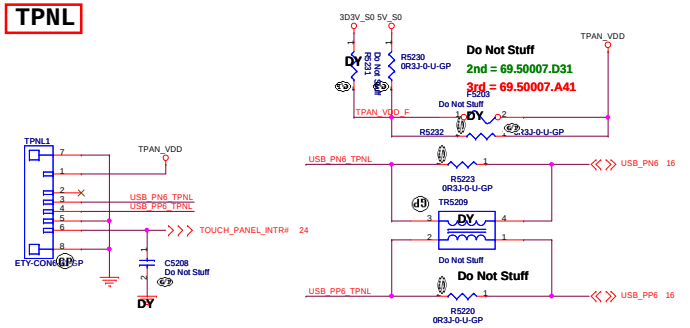




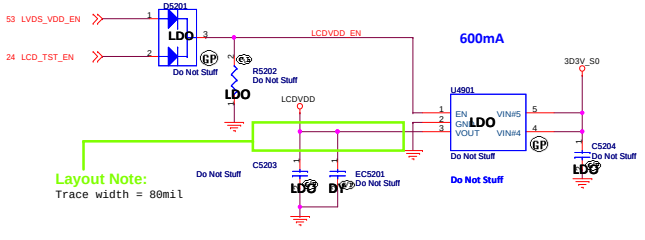




TPNL



LCDVDD



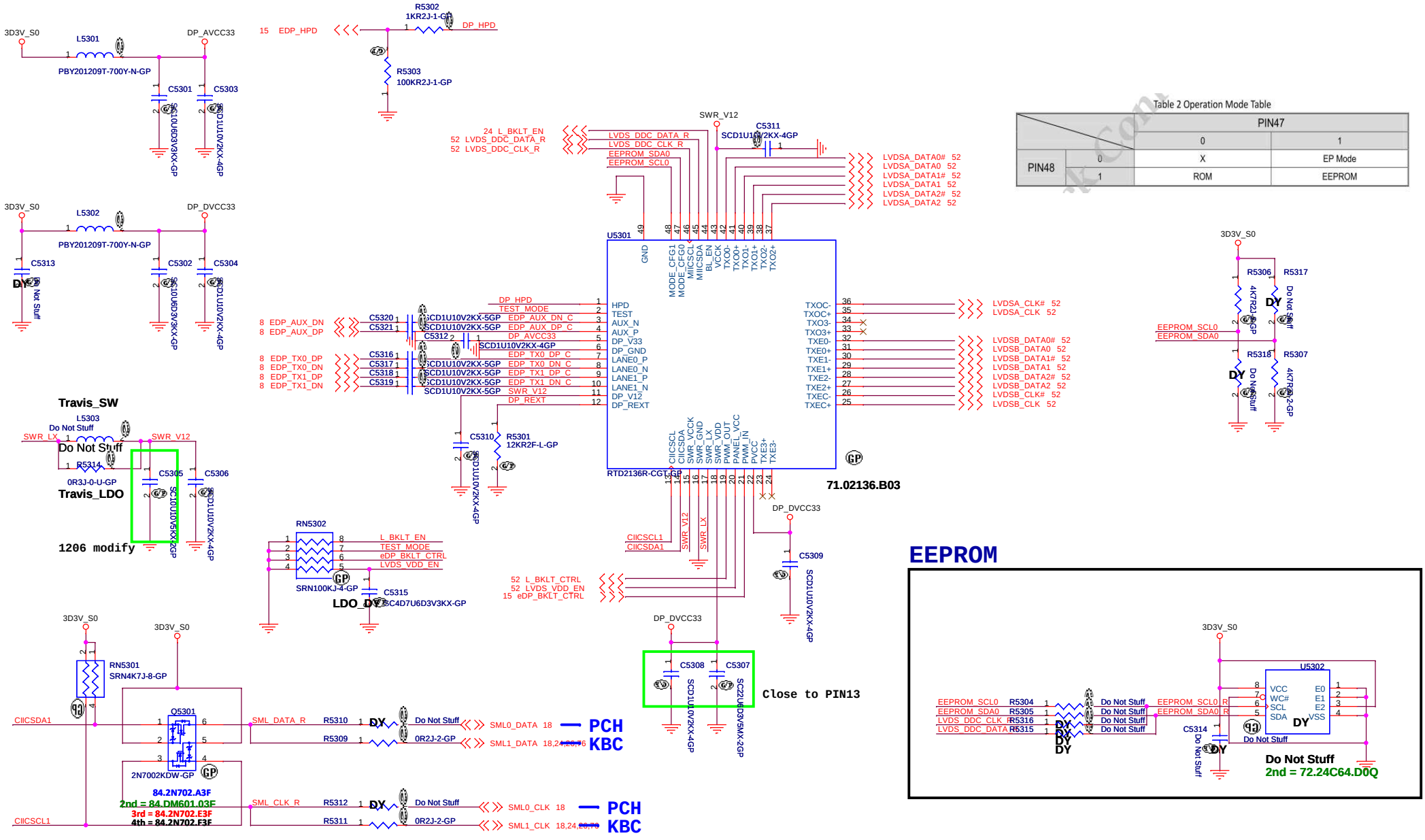
UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A2	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 52 of 104



UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS_Switch

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 53 of 104

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

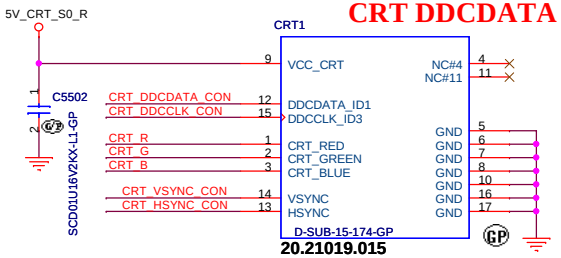
Title

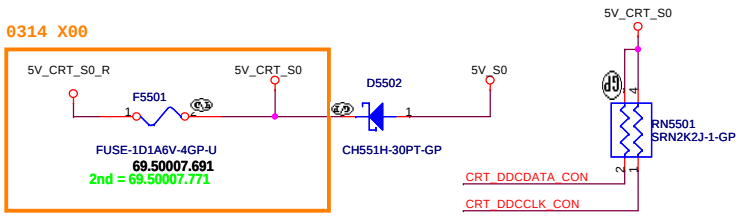
HDMI Level Shifter/Connector

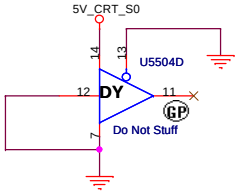
Size	Document Number	Rev
A3	***Latitude300 Haswell***	***X00***

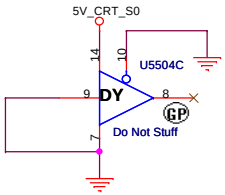
Date: Friday, March 15, 2013 Sheet 54 of 104

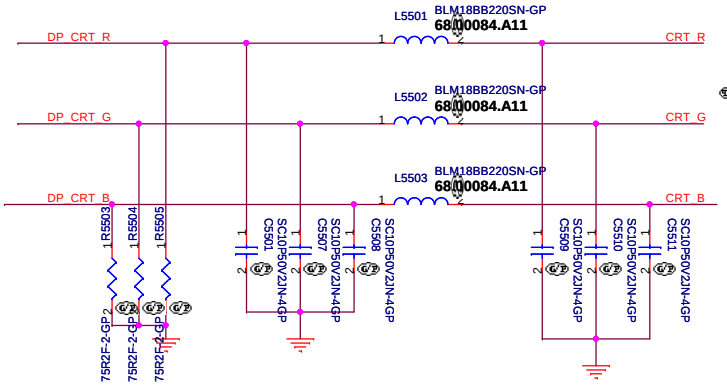
CRT DDCDATA & DDCCLK level shift

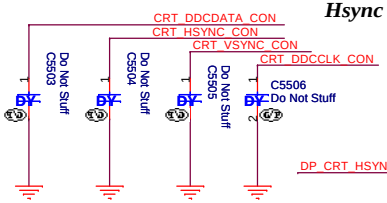




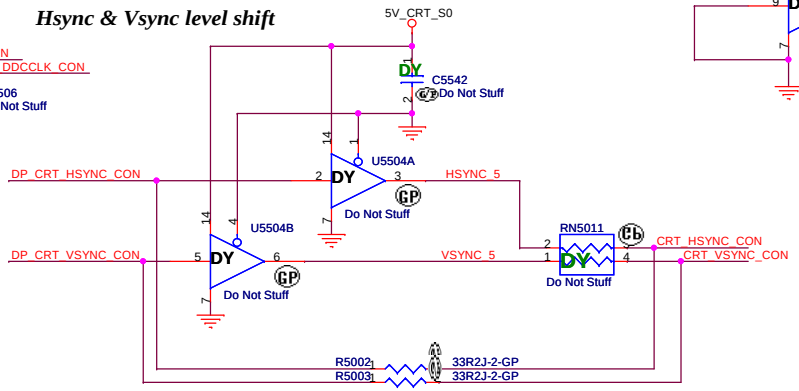


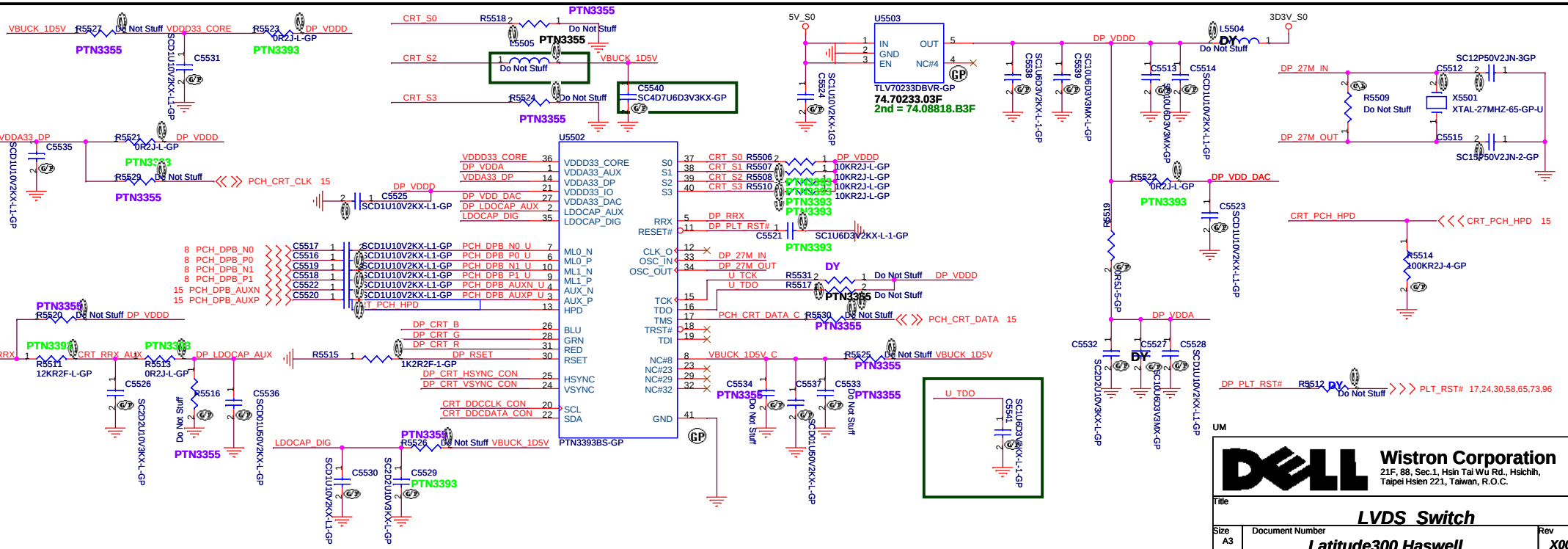






Hsync & Vsync level shift





UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

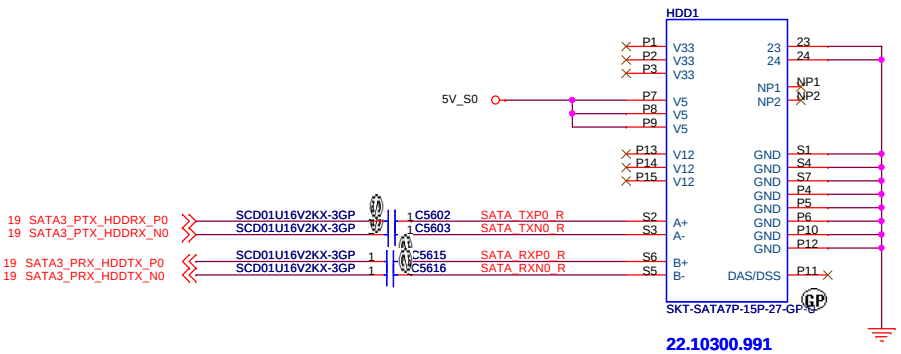
Title: **LVDS Switch**

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

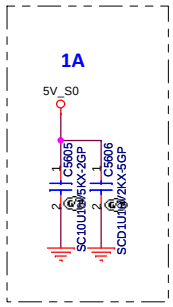
Date: Friday, March 15, 2013 Sheet 55 of 104

SSID = SATA

SATA HDD Connector

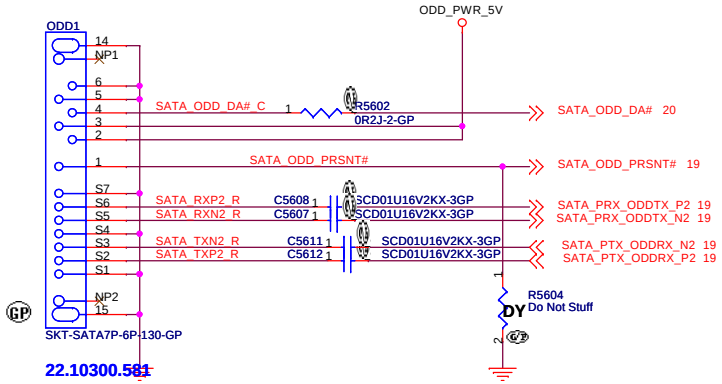


22.10300.991

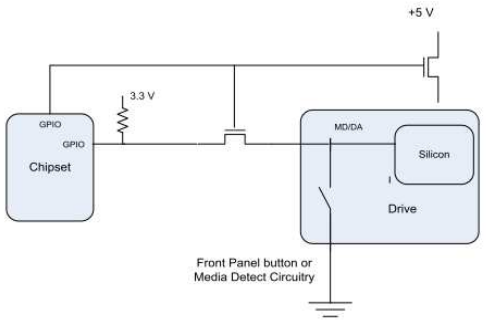


Close to HDD1

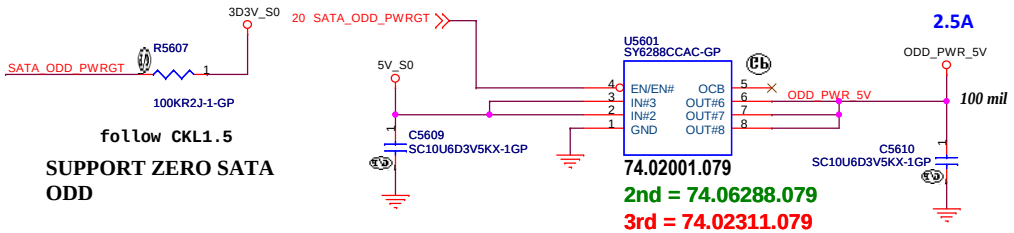
ODD Connector



22.10300.581



SATA Zero Power ODD



follow CKL1.5

SUPPORT ZERO SATA ODD

74.02001.079

2nd = 74.06288.079

3rd = 74.02311.079

Current limit
Active High
typ =>2.5A

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *HDD/ODD*		
Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet 56 of 104	

SSID = ESATA

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

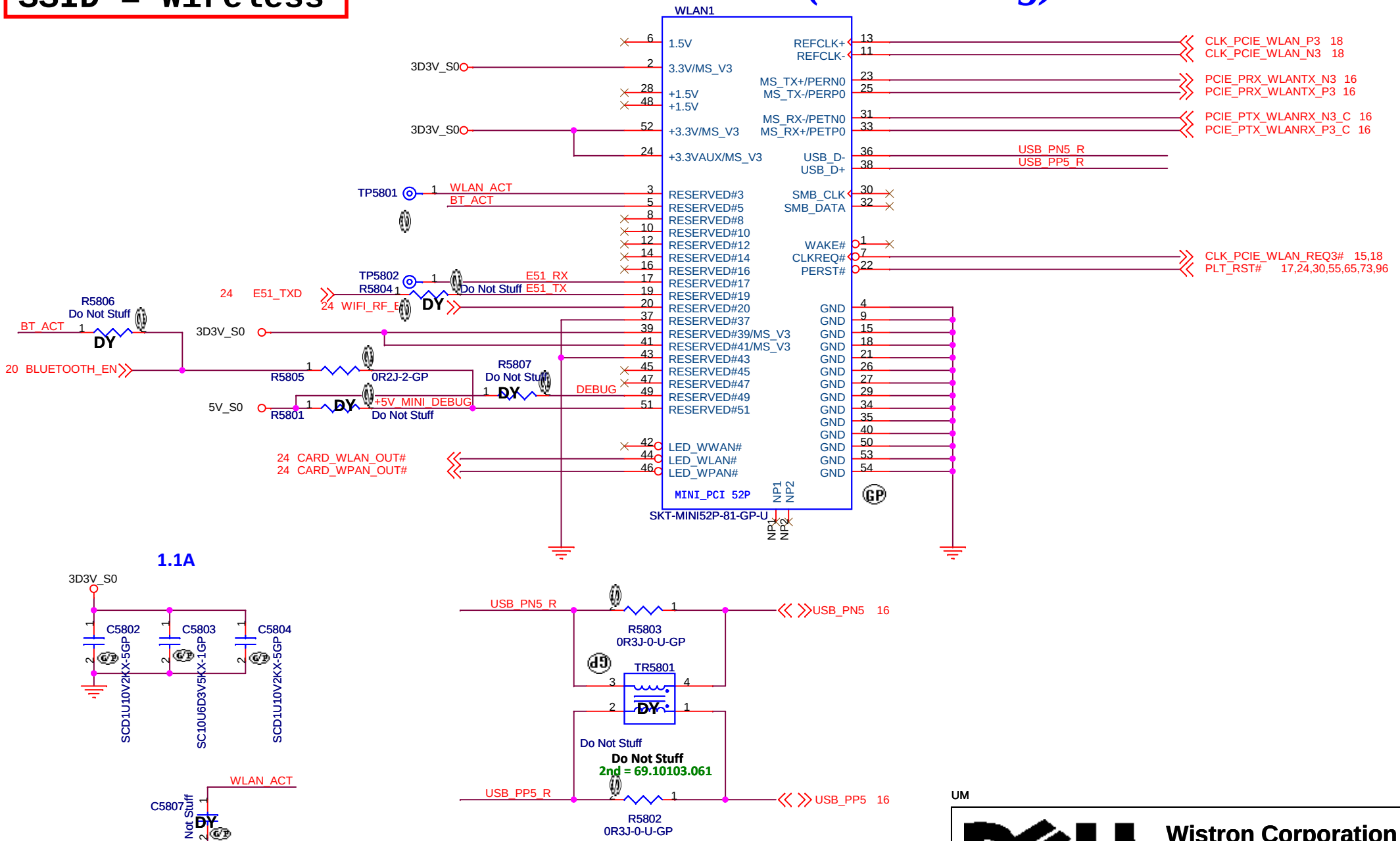
Title: ESATA

Size: A3 | Document Number: Latitude300 Haswell | Rev: X00

Date: Friday, March 15, 2013 | Sheet 57 of 104

Mini Card Connector(802.11a/b/g)

SSID = Wireless



1.1A

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINICARD(WLAN)/ITP CONN***

Size	Document Number	Rev
A4	***Latitude300 Haswell***	*X00*

Date: Friday, March 15, 2013 Sheet 58 of 104

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

Date: Friday, March 15, 2013 Sheet 59 of 104

SSID = PCH

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

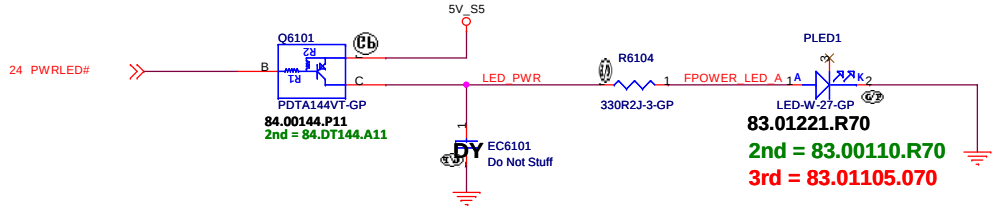
Title: ***(Reserved)***

Size	Document Number	Rev
A4	***Latitude300 Haswell***	***X00***

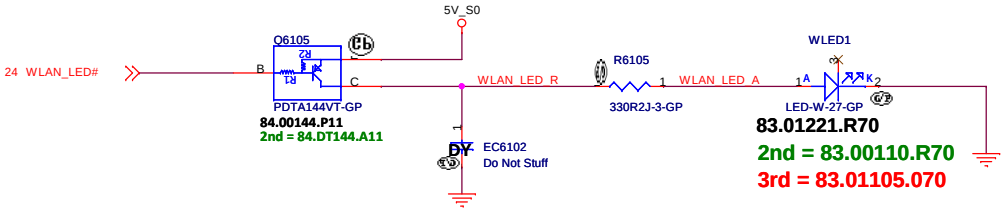
Date: Friday, March 15, 2013 Sheet 60 of 104

SSID = User.Interface

FRONT POWER LED
Low actived from KBC GPIO

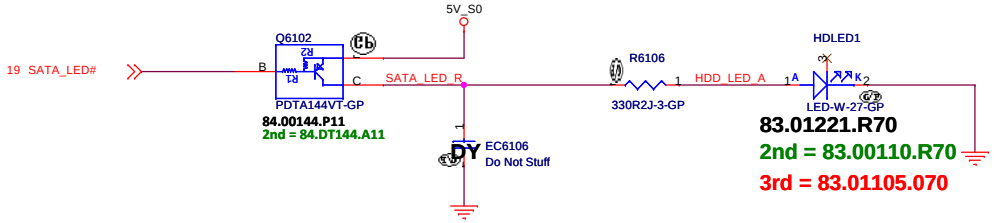


Wireless LED
Low actived from KBC GPIO

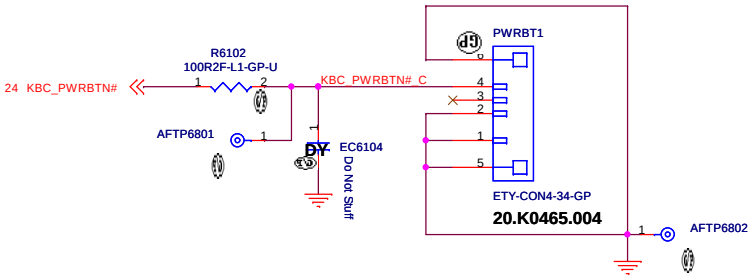


Place EC6806 near WLED1

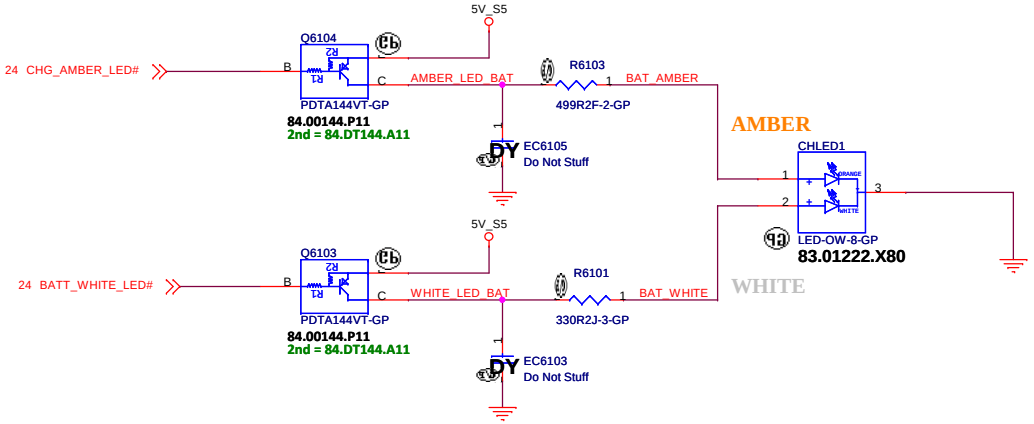
SATA HDD LED(White)
Low actived from PCH GPIO



Power button



Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

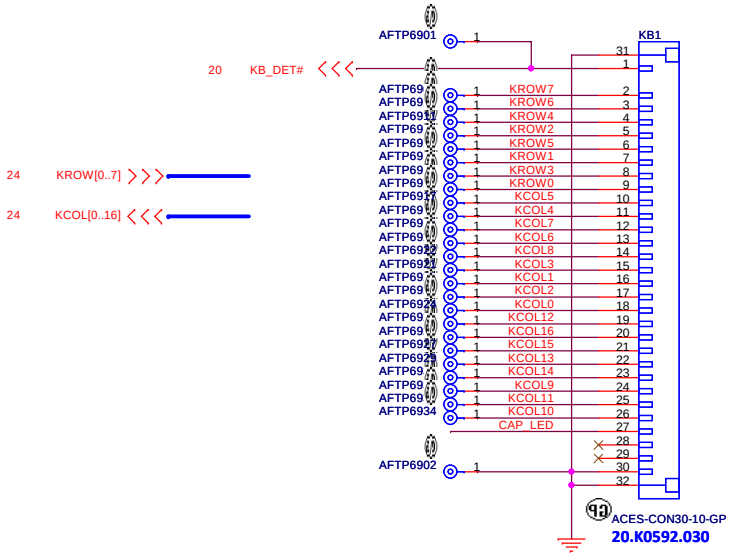
Title: *LED Bard/Power Button*

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 61 of 104

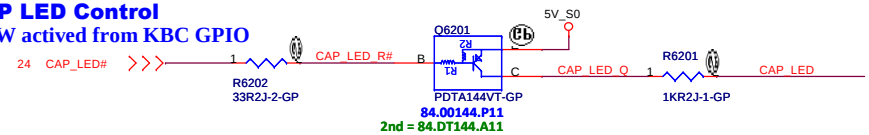
SSID = KBC

Internal Keyboard Connector

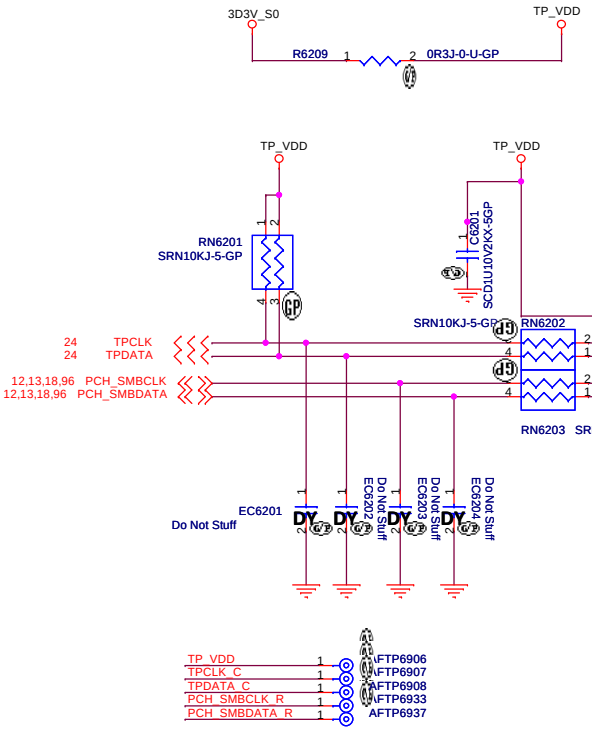


CAP LED Control

LOW actived from KBC GPIO



SSID = Touch.Pad



Refer "PN 510-002792-01 Rev 2 " module spec

Pin number	Pin name
1	VDD
2	PS2_CLK
3	PS2_DATA
4	GND
5	SMBUS_CLK
6	SMBUS_DATA

UM

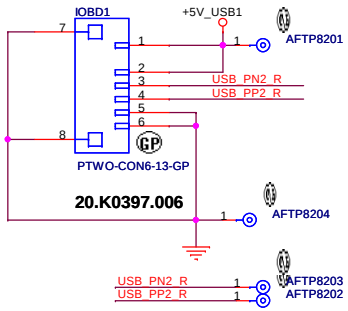
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

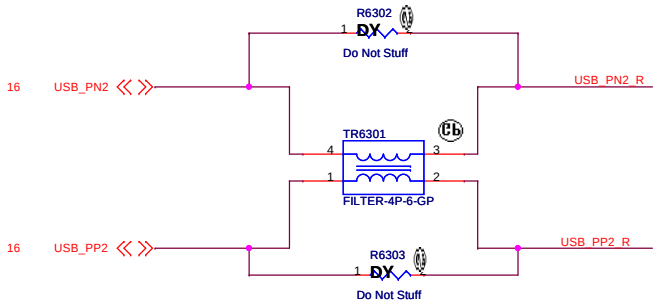
Title: Key Board/Touch Pad

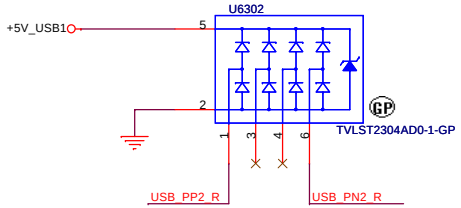
Size: A3 | Document Number: Latitude300 Haswell | Rev: X00

Date: Friday, March 15, 2013 | Sheet 62 of 104

SSID = User.Interface







UM

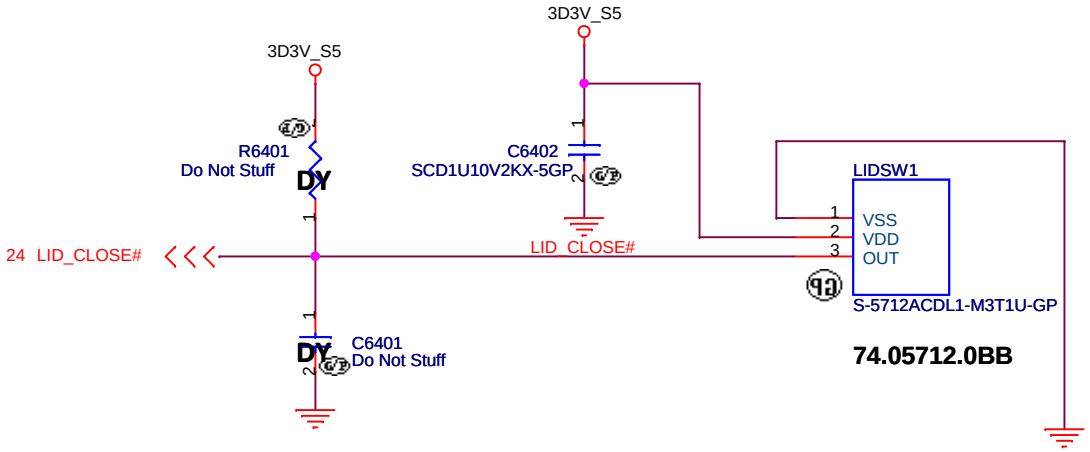
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: Latitude300 Haswell | Rev: X00

Date: Friday, March 15, 2013 | Sheet 63 of 104

SSID = User.Interface



UM

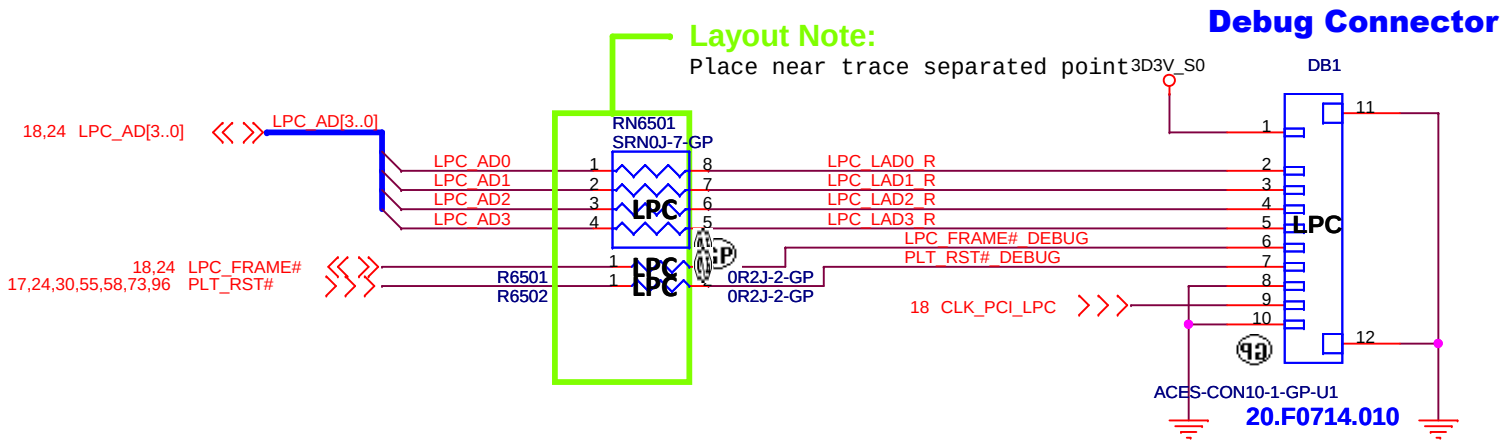
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	***Latitude300 Haswell***	***X00***

Date: Friday, March 15, 2013 Sheet 64 of 104

SSID = DEBUG PORT



UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	***Latitude300 Haswell***	***X00***

Date: Friday, March 15, 2013 Sheet 65 of 104

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

Date: Friday, March 15, 2013 Sheet 66 of 104

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

Date: Friday, March 15, 2013 Sheet 67 of 104

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB3.0 PORT

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

Date: Friday, March 15, 2013 Sheet 69 of 104

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

Date: Friday, March 15, 2013 Sheet 70 of 104

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

(Blanking)

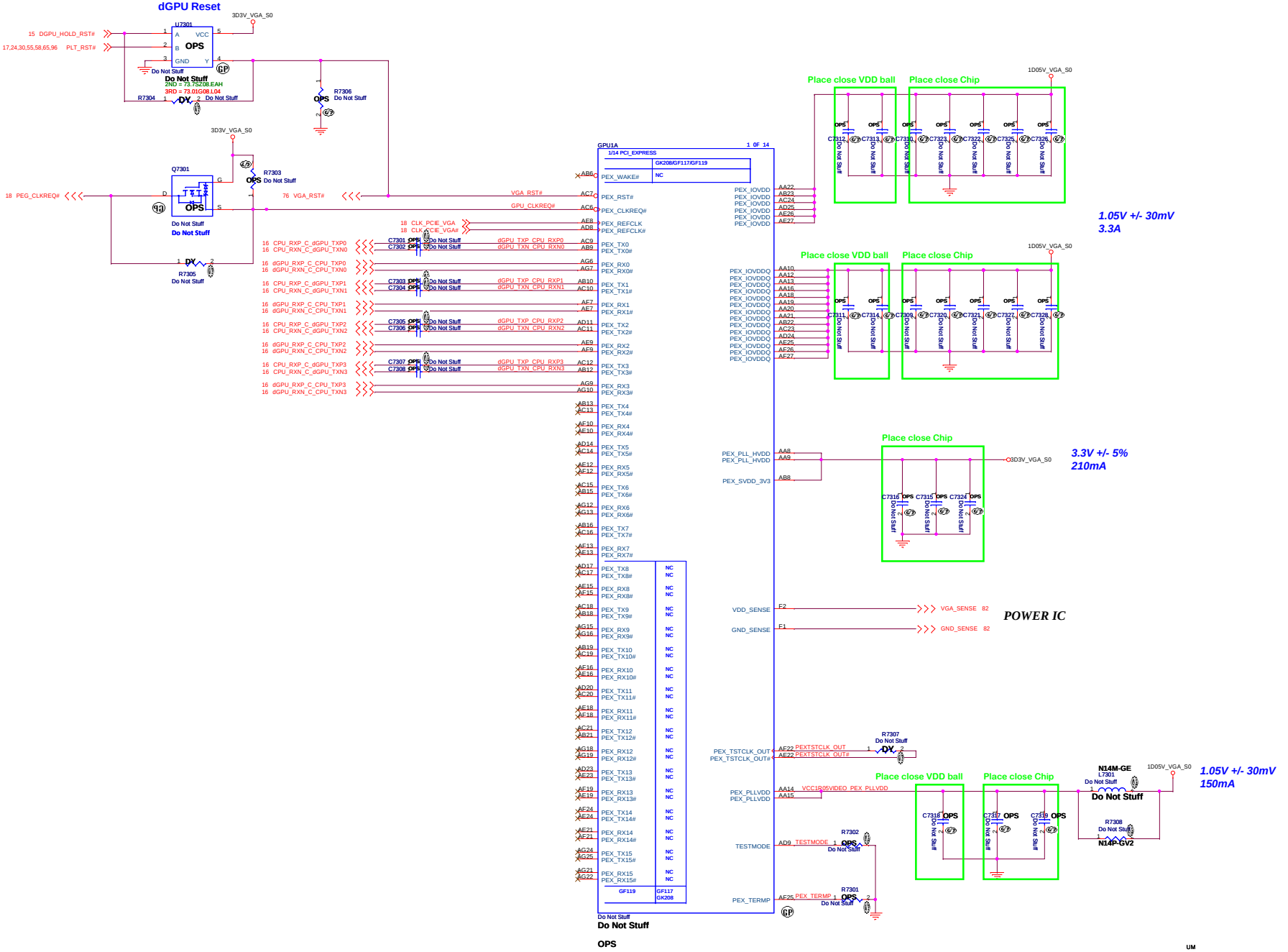
UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

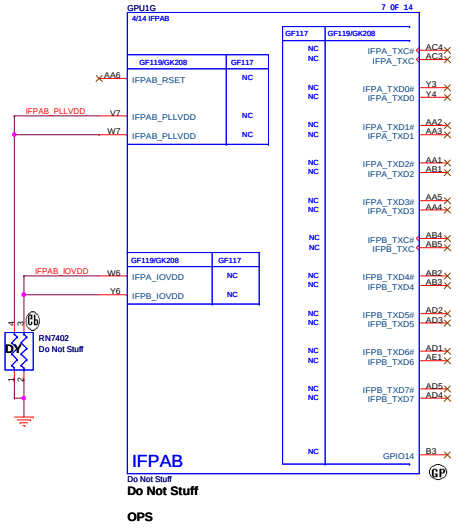
Title: ***Reserved***

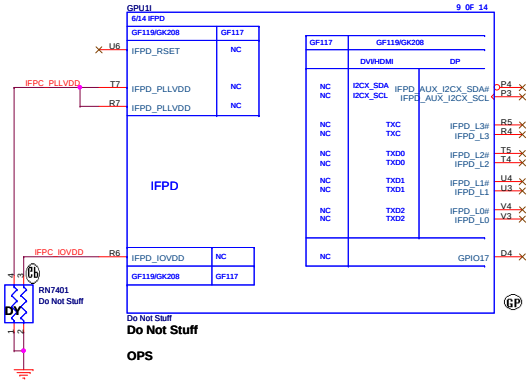
Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

Date: Friday, March 15, 2013 Sheet 72 of 104

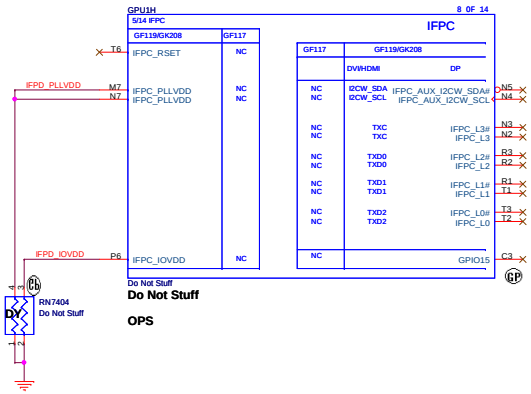

dGPU Reset
3D3V_VGA_S0
15 DGPU_HOLD_RST#
17,24,30,55,58,65,96 PLT_RST#
U7301
OPS
Do Not Stuff
2ND = 73.7SZ08.EAH
3RD = 73.01G08.L04
R7304
R7306
R7303
Q7301
18 PEG_CLKREQ#
76 VGA_RST#
VGA_RST#
GPU_CLKREQ#
18 CLK_PCIE_VGA
18 CLK_PCIE_VGA#
R7305
GPU1A
1 0F 14
1/14 PCI_EXPRESS
GK208/GF117/GF119
PEX_WAKE#
PEX_RST#
PEX_CLKREQ#
PEX_REFCLK
PEX_REFCLK#
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
PEX_RX4#
PEX_TX5
PEX_TX5#
PEX_RX5
PEX_RX5#
PEX_TX6
PEX_TX6#
PEX_RX6
PEX_RX6#
PEX_TX7
PEX_TX7#
PEX_RX7
PEX_RX7#
PEX_TX8
PEX_TX8#
PEX_RX8
PEX_RX8#
PEX_TX9
PEX_TX9#
PEX_RX9
PEX_RX9#
PEX_TX10
PEX_TX10#
PEX_RX10
PEX_RX10#
PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
PEX_RX12#
PEX_TX13
PEX_TX13#
PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#
GF119
GF117
GK208
Do Not Stuff
OPS
C7301
C7302
C7303
C7304
C7305
C7306
C7307
C7308
dGPU_TXP_CPU_RXP0
dGPU_TXN_CPU_RXN0
dGPU_TXP_CPU_RXP1
dGPU_TXN_CPU_RXN1
dGPU_TXP_CPU_RXP2
dGPU_TXN_CPU_RXN2
dGPU_TXP_CPU_RXP3
dGPU_TXN_CPU_RXN3
16 CPU_RXP_C_dGPU_TXP0
16 CPU_RXN_C_dGPU_TXN0
16 dGPU_RXP_C_CPU_TXP0
16 dGPU_RXN_C_CPU_TXN0
16 CPU_RXP_C_dGPU_TXP1
16 CPU_RXN_C_dGPU_TXN1
16 dGPU_RXP_C_CPU_TXP1
16 dGPU_RXN_C_CPU_TXN1
16 CPU_RXP_C_dGPU_TXP2
16 CPU_RXN_C_dGPU_TXN2
16 dGPU_RXP_C_CPU_TXP2
16 dGPU_RXN_C_CPU_TXN2
16 CPU_RXP_C_dGPU_TXP3
16 CPU_RXN_C_dGPU_TXN3
16 dGPU_RXP_C_CPU_TXP3
16 dGPU_RXN_C_CPU_TXN3
Place close VDD ball
Place close Chip
1D05V_VGA_S0
PEX_IOVDDQ
PEX_IOVDD
1.05V +/- 30mV
3.3A
3.3V +/- 5%
210mA
PEX_PLL_HVDD
PEX_SVDD_3V3
3D3V_VGA_S0
POWER IC
VDD_SENSE
GND_SENSE
VGA_SENSE 82
GND_SENSE 82
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PEXTSTCLK_OUT
PEXTSTCLK_OUT#
R7307
PEX_PLLVDD
VCC1R05VIDEO_PEX_PLLVDD
1.05V +/- 30mV
150mA
N14M-GE
L7301
N14P-GV2
R7308
TESTMODE
R7302
PEX_TERMP
R7301
UM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU_PCIE/STRAPPING(1/5)
Size A2
Document Number
Latitude300 Haswell
Rev X00
Date: Friday, March 15, 2013
Sheet 73 of 104

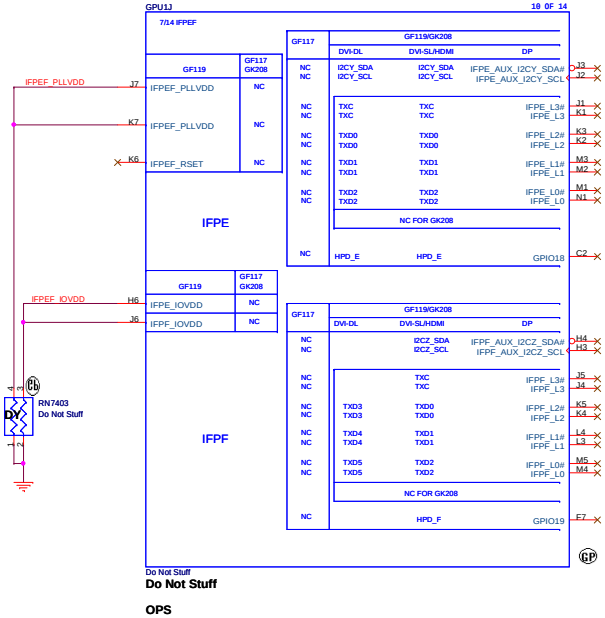
LVDS Interface





HDMI Interface





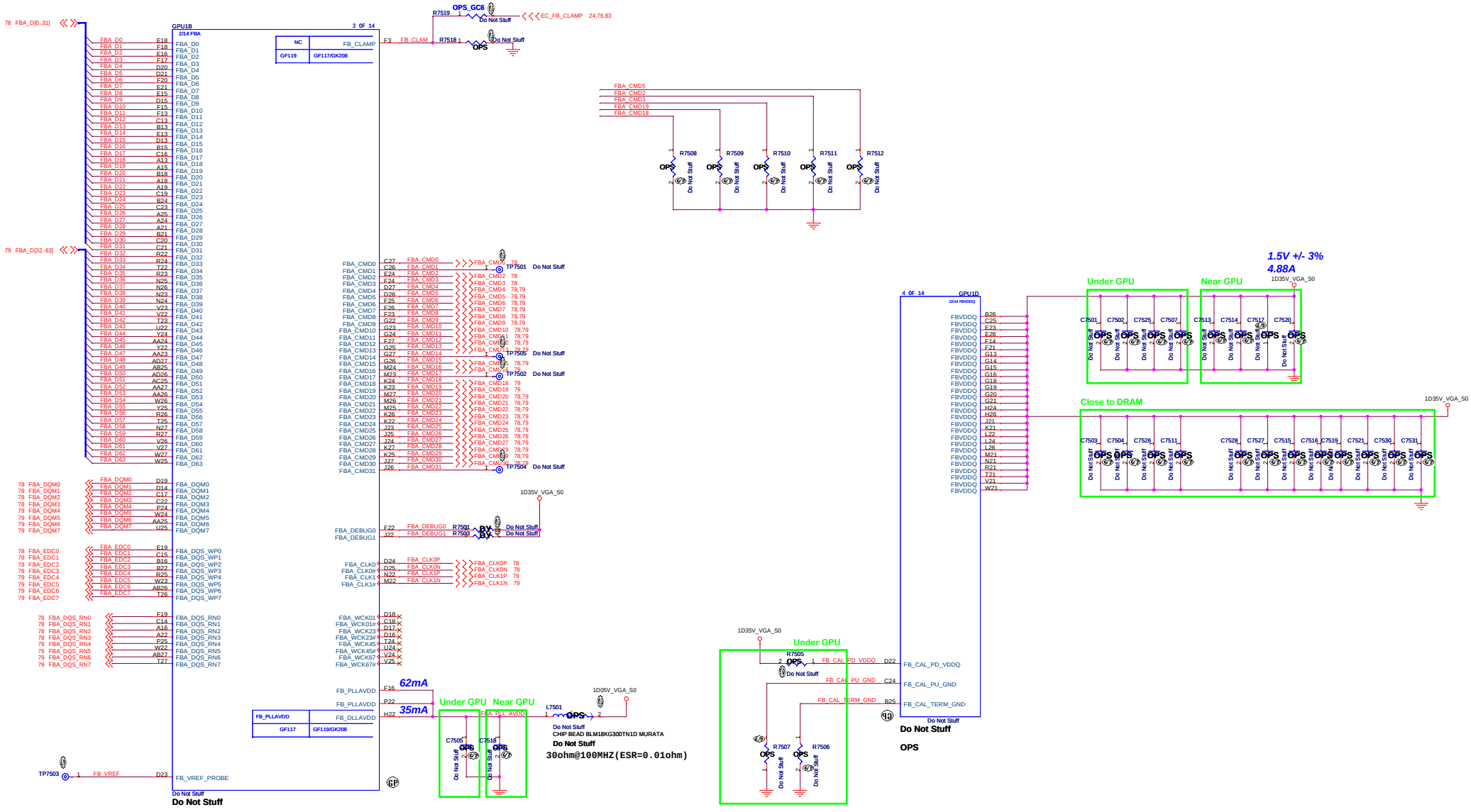
UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU Memory(2/5)*

Size: A2 | Document Number: Latitude300 Haswell | Rev: X00

Date: Friday, March 15, 2013 | Sheet 74 of 104



UM

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU_DP/LVDS/CRT/GPIO(3/5)		
Size: A2	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet 75 of 104	

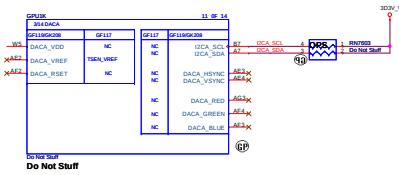
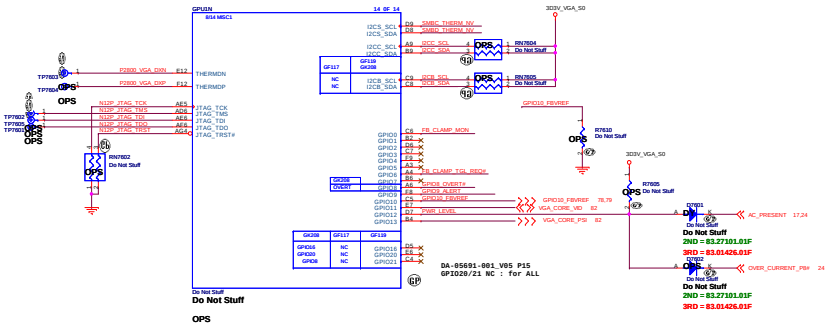


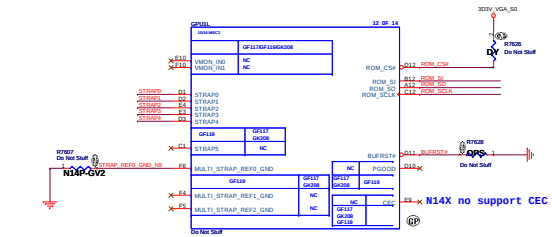
Table 112. GB2-64 and GB4-128 PLL Power Rail Filter - PLL_VDD

GPU Package Type	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2-64 and GB4-128	PLL_VDD	100 nF	X7R	0402	1	Under GPU
		22 µF	X7R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 for N14E-GE; 0.05 for all others)		0402	1	Near GPU

Table 113. GB2-64, GB4-128, GB2-192 and GB3-256 PLL Power Rail Filter - SP_PLLVDD and VID_PLLVDD Combined

GPU Package Type	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2-64, GB4-128 and GB3-256	SP_PLLVDD and VID_PLLVDD combined	100 nF	X7R	0402	2	Under GPU
		4.7 µF	X5R	0402	1	Near GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		180 Ω (ESR=0.2)		0603	1	Near GPU





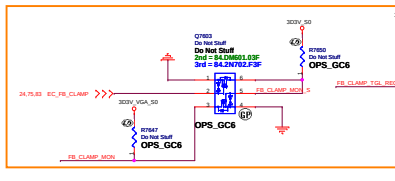
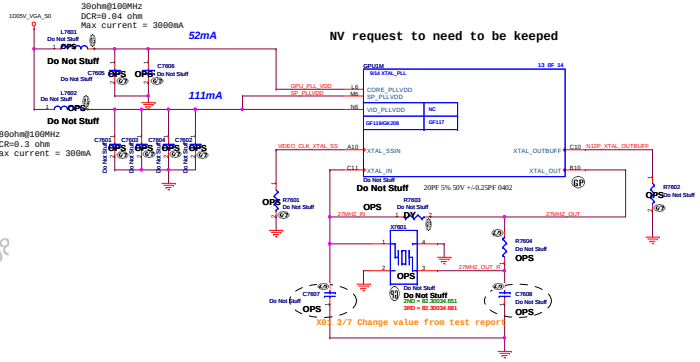
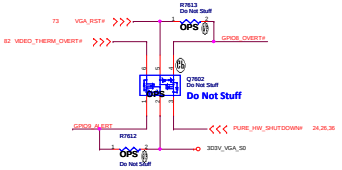
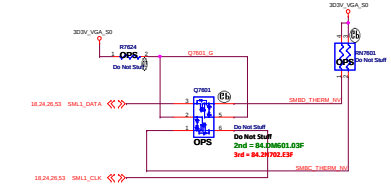


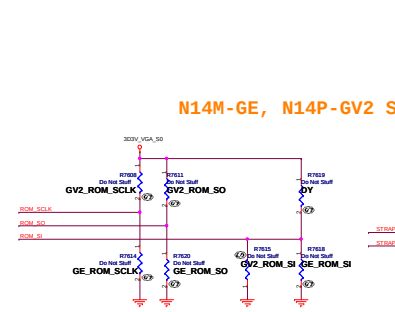
Table 120. Device Specific Strap Mode Selection

	N14M-GE/-GL	Other N14x GPUs
Multi_Strap_Ref2_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref1_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref0_GND	No Connect	40.2k 1% to GND
Strap Mode Selected	Binary	Multi-Level









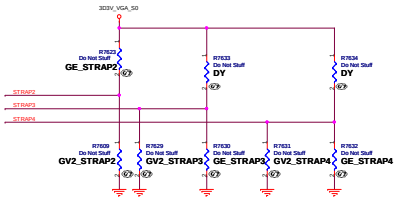


Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
				MT41J128M16JT-107G:K	900	1150	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
				K4W2G1646E-BC11	900	1204	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	N/A	Production ready
				H5TQ2G63DFR-11C	900	N/A	Production ready
		0xC	1.5V/ 1.5V	H5TC2G63FFR-11C	1000	N/A	Post-production candidate

Table 5. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production ready
	Hynix	0x2	1.5V/ 1.5V	H5TC4G63AFR-11C	900	N/A	Production ready

Table 121. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

	N14M-LP	N14M-GS	N14P-GV	N14P-GV2
Chip Part #	GK208-640 (Small package) GK208-740 (Big package)	GK208-630 (Small package) GK208-730 (Big package)	GK208-650 (Small package) GK208-750 (Big package)	GK208-632 (Small package) GK208-732 (Big package)
Device ID	0x1291	0x1290	0x1294	0x1292

Strap Pin Name	Logical strapping name: bit[0]	Logical strapping name: bit[1]	Logical strapping name: bit[2]	Logical strapping name: bit[3]
ROM_SCLK	PCI_DEVID[0]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TER_M
	1	*	0	*
ROM_SI	RAMCFG[0]	RAMCFG[1]	RAMCFG[2]	RAMCFG[3]
	0	0	1	1
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
	*	*	*	*
STRAP0	USER[0]	USER[2]	USER[1]	USER[3]
	↑	↑	↑	↑
STRAP1	IGIO_PADCFG[3]	IGIO_PADCFG[2]	IGIO_PADCFG[1]	IGIO_PADCFG[0]
	*	*	*	*
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	0	0	1	0
STRAP3	SOR1_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
	↑	↑	↑	↑
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V
	*	*	*	*

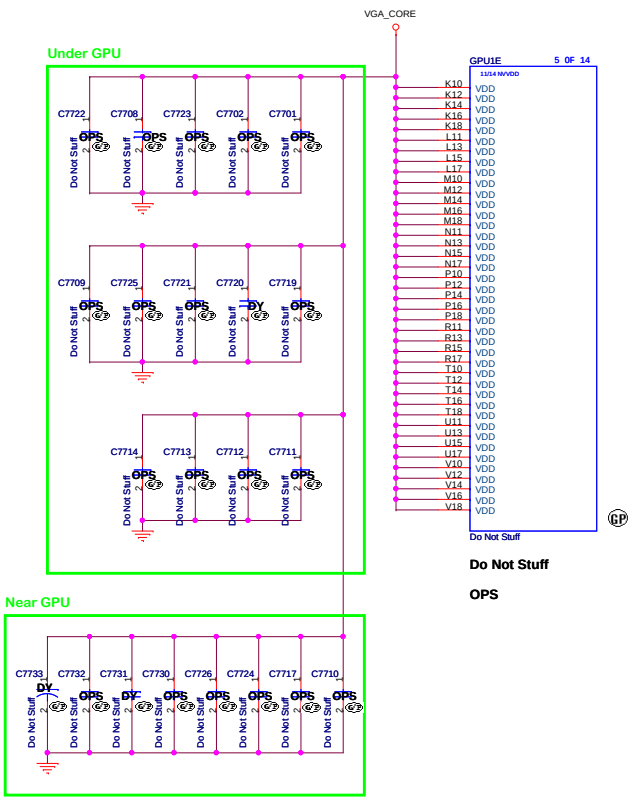
10K ohm pull-up
10K ohm pull-up
10K ohm pull-down
10K ohm pull-down
10K ohm pull-down

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

GPU_POWER(4/5)

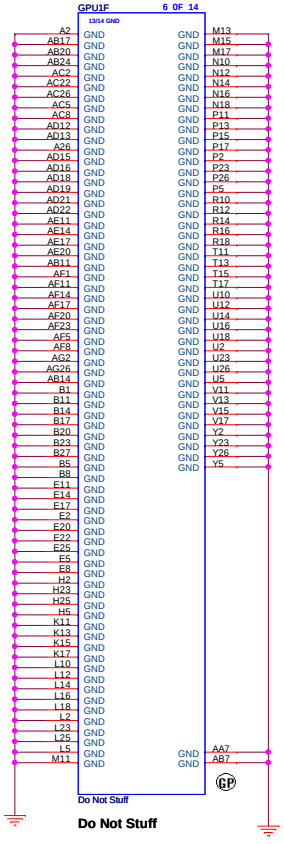
Size: A1 | Document Number: Latitude300 Haswell | Rev: X00

Date: Friday, March 15, 2013 | Sheet 76 of 104



Do Not Stuff

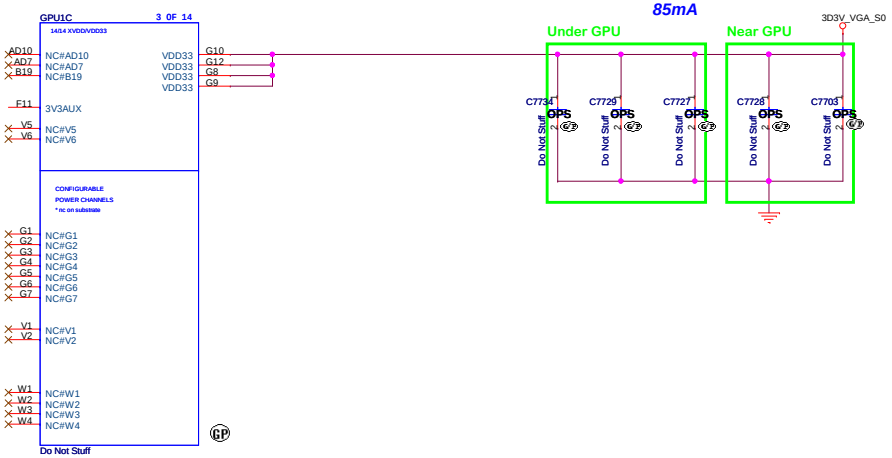
OPS



Do Not Stuff

OPS

3.3V +/- 5%
85mA



Do Not Stuff

OPS

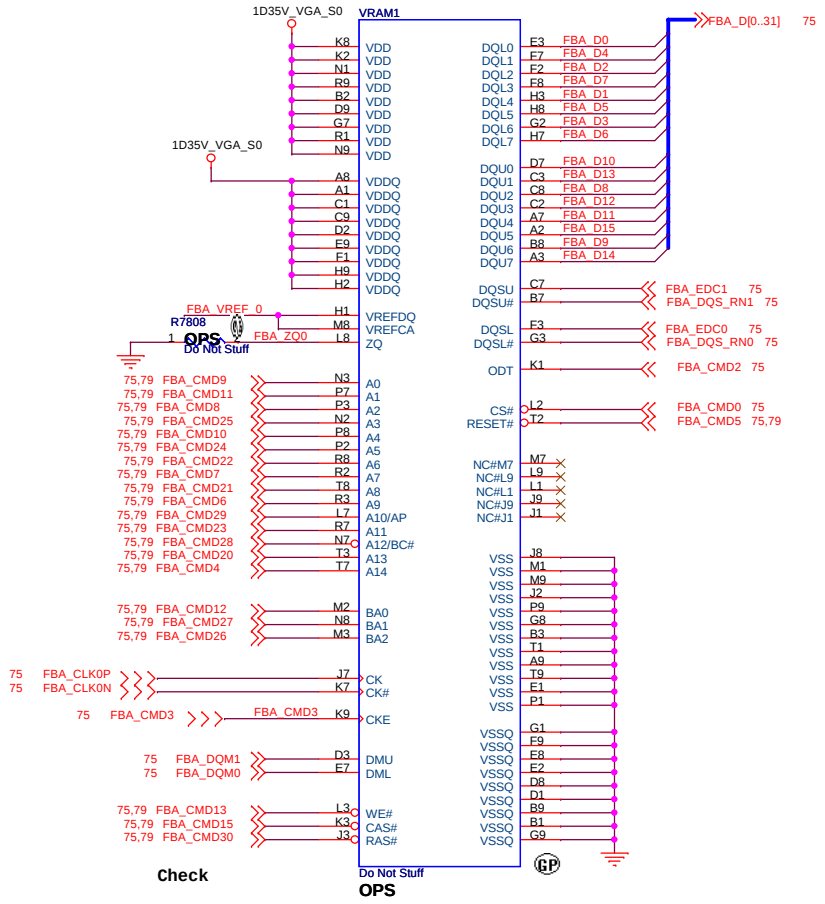
UM

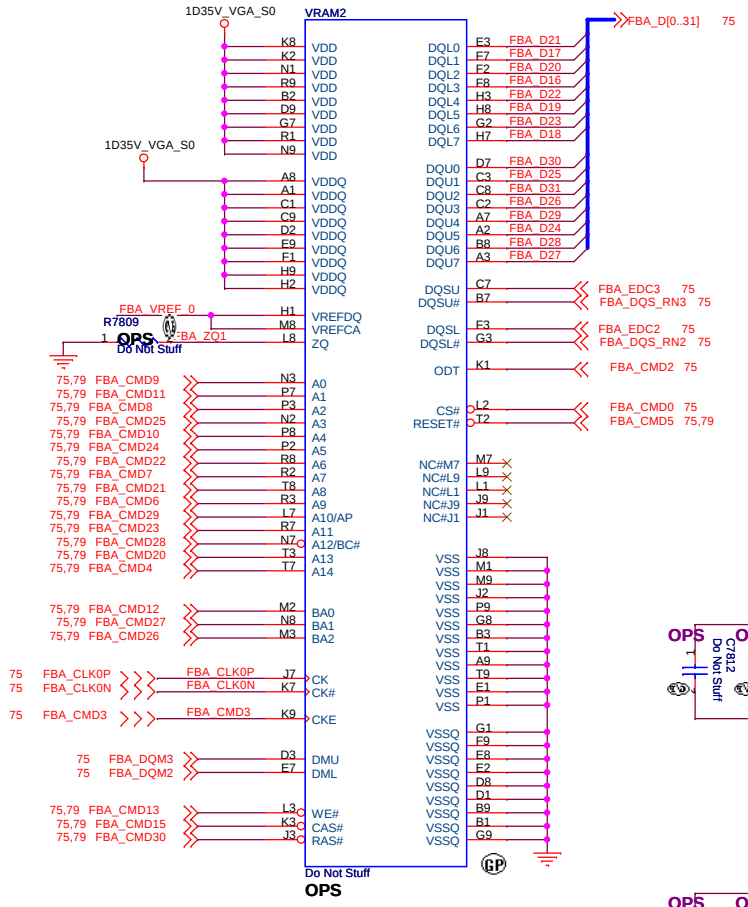
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU_DPPWR/GND(5/5)***

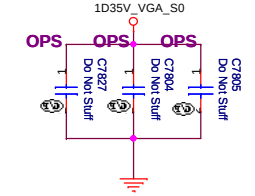
Size	Document Number	Rev
Custom	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 77 of 104

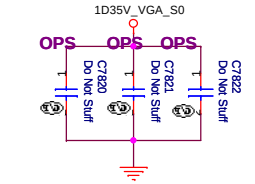




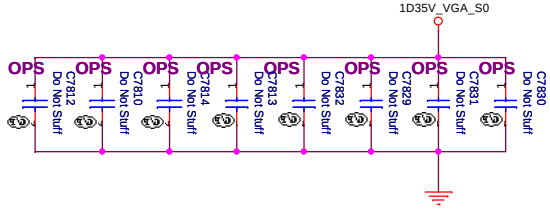
Place close VRAM1 VDD ball



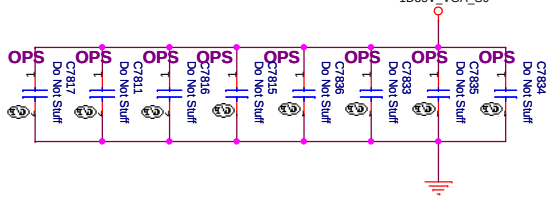
Place close VRAM2 VDD ball



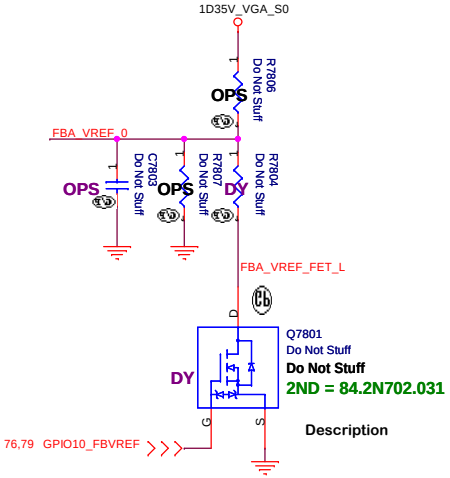
Place close VRAM1VDDQ ball

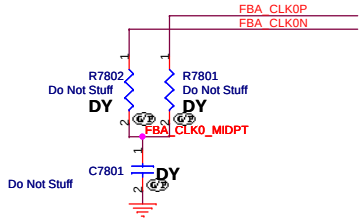


Place close VRAM1VDDQ ball

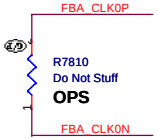


Frame Buffer Patition A-Lower Half





FBCLK Termination place on VRAM side



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

20110613

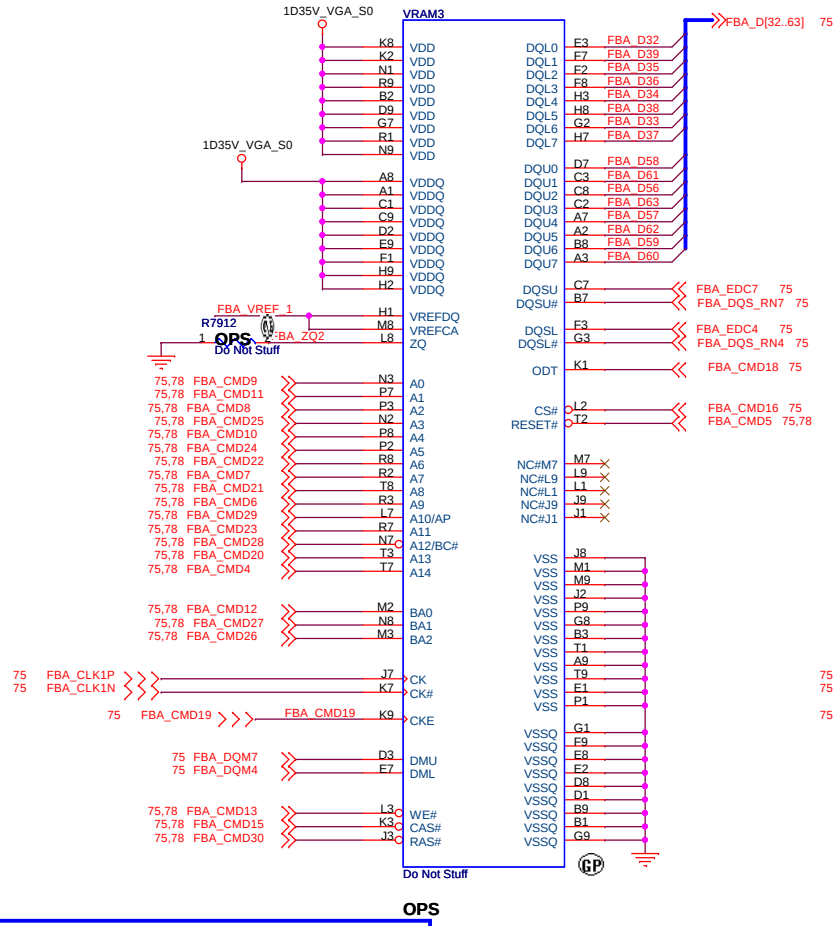
UM

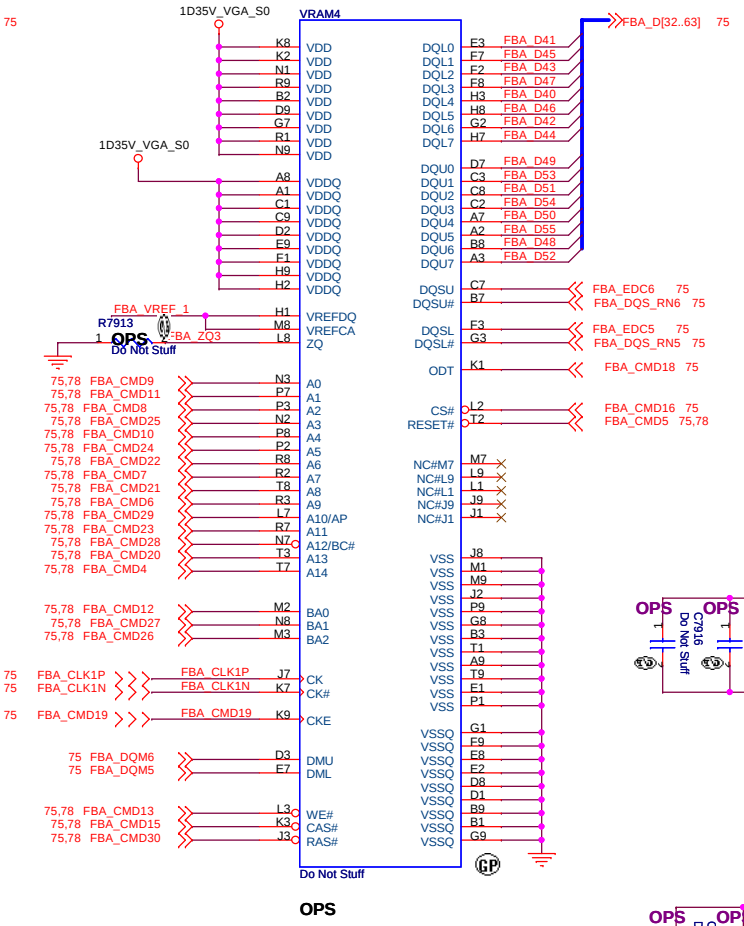
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM1,2 (1/4)*

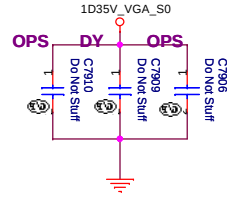
Size	Document Number	Rev
A3	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 78 of 104

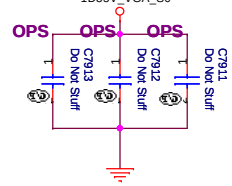




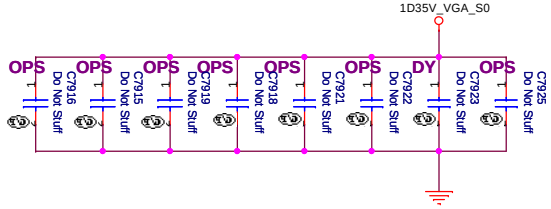
Place close VRAM3 VDD ball



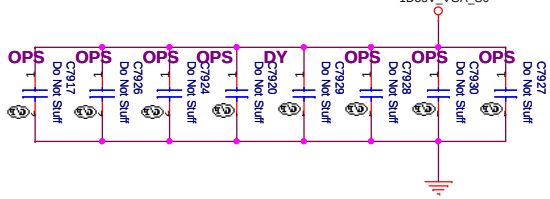
Place close VRAM4 VDD ball



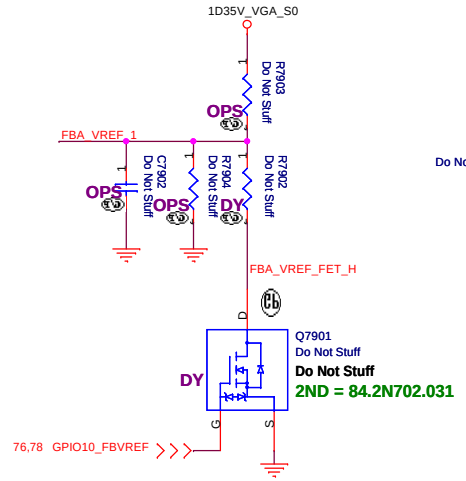
Place close VRAM3 VDDQ ball

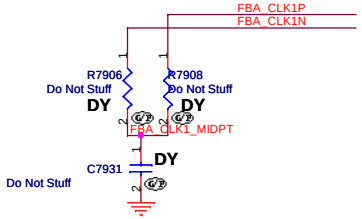


Place close VRAM4 VDDQ ball

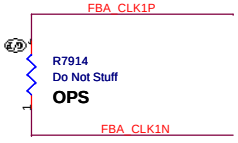


Frame Buffer Patition A-Lower Half





FBCLK Termination place on VRAM side



UM

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *GPU-VRAM3,4 (2/4)*		
Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet 79 of 104	

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 80 of 104

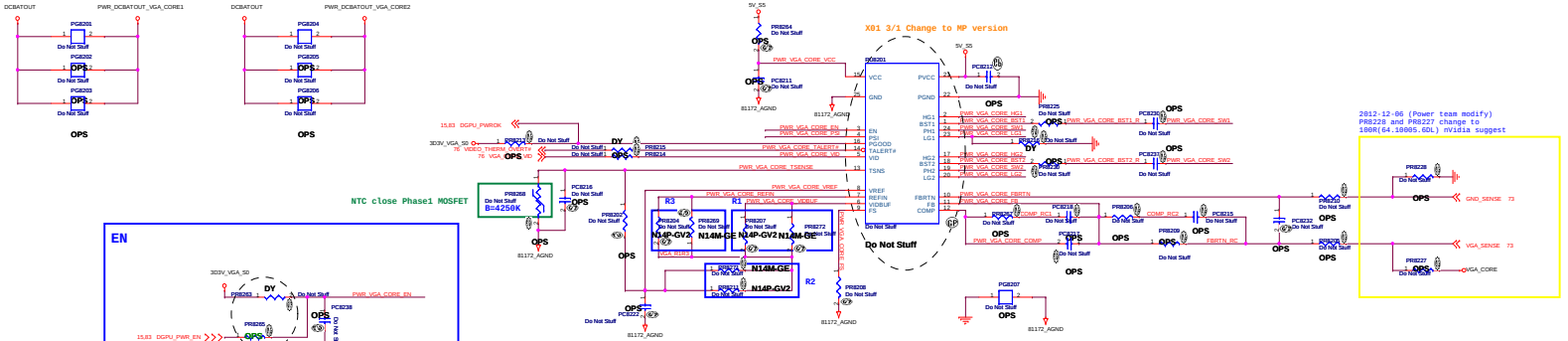
UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM7,8 (4/4)*

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

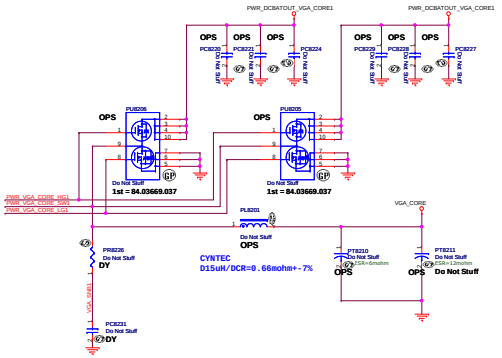
Date: Friday, March 15, 2013 Sheet 81 of 104



EDC=45A
EDP=72A

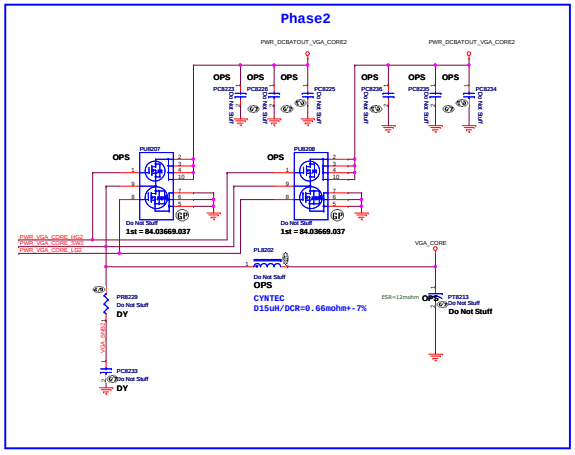
TYPE	config	TDC	EDP	OCP	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14M-GE	C	35A	41A		39kohm	30kohm	3kohm	24kohm	3kohm	1.8nF
N14P-GV2	B	32A	55A		20kohm	20kohm	2kohm	18kohm	0ohm	2.7nF
N14P-GT	B	45A	75A		20kohm	20kohm	2kohm	18kohm	0ohm	2.7nF

Phase1



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
MOS: Q1: Id=10A,Rdson=9.8~13.2 mohm ; Q2: Id=17A, Rdson=3.6~5.2mohm 84.03669.037
Inductor: CHIP CHOKE 0.22UH PCMB063T-R22MS 2.5~3mohm Isat =34Arms 68.R2210.20C
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L

Phase2



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
MOS: Q1: Id=10A,Rdson=9.8~13.2 mohm ; Q2: Id=17A, Rdson=3.6~5.2mohm 84.03669.037
Inductor: CHIP CHOKE 0.22UH PCMB063T-R22MS 2.5~3mohm Isat =34Arms 68.R2210.20C
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L

Table 1. PWM-VID Spec and Component Values

PWM-VID Spec				
		Config A	Config B	Config C
Vmin	V	0.6	0.6	0.65
Vmax	V	1.2	1.2	1.15
Vboot	V	0.875	0.9	0.9
Voltage Step Vstep	mV	6.25	6.25	25
Number of Voltage Levels N	level	96	96	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676
PWM Minimum Pulse Width T_{DWF1}	ns	9.26	9.26	74
VID Transient Time T	us	<100	<100	<100
Component Value				
R1 (1%)	KΩ	39	20	39
R2 (1%)	KΩ	39	20	30
R3 (1%)	KΩ	1.5	2	3
R4 (1%)	KΩ	30	18	24
R5 (1%)	KΩ	1.5	0	3
C	nF	1.5	2.7	1.8

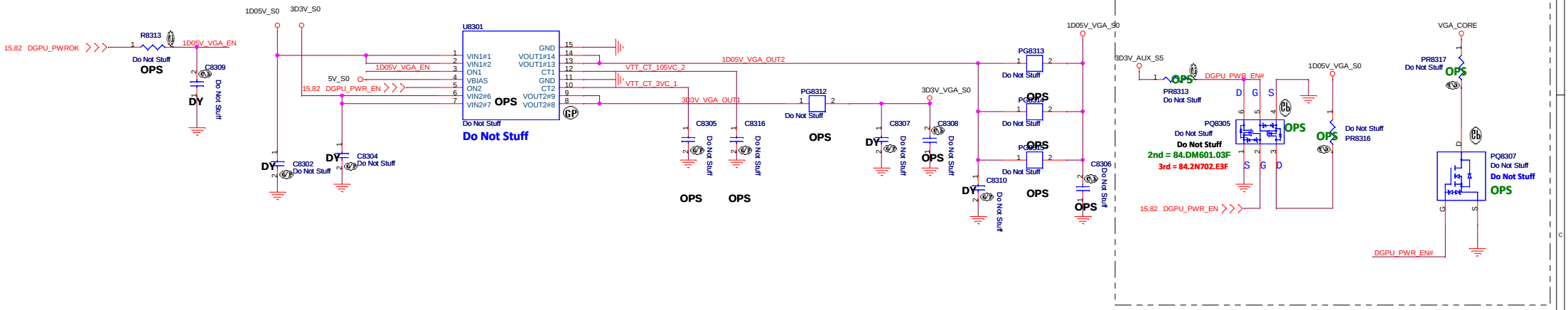
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP3211 +VGA_CORE
Size: Custom | Document Number: Latitude300 Haswell | Rev: X00
Date: Friday, March 15, 2013 | Sheet 82 of 104

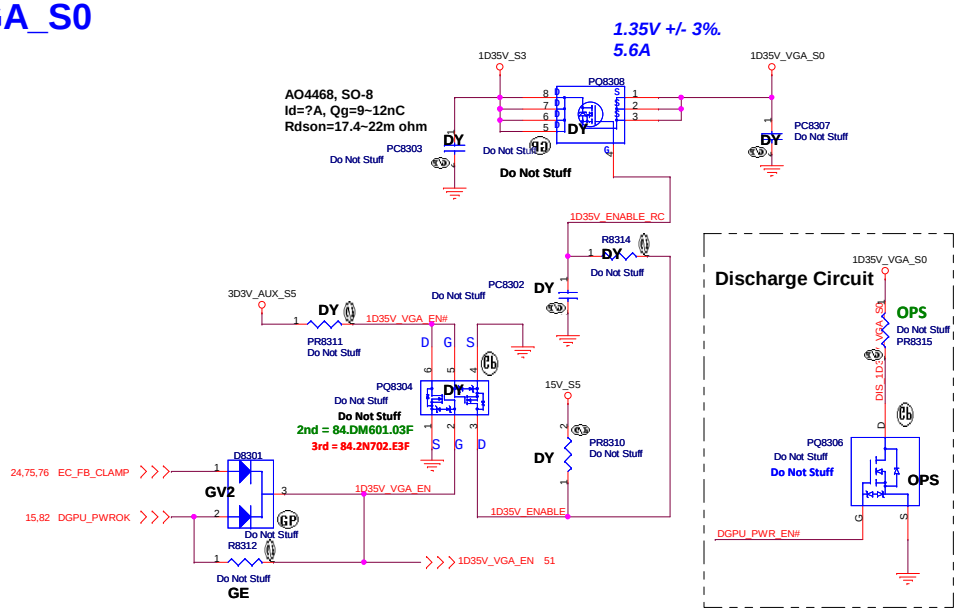
3D3V_VGA_S0
1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0

3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0



1D35V_VGA_S0



CTx (pF)	Rise Time (µs) 10% - 90%, COUT = 0.1µF @ VIN; VOUT=0 ohm load Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. CTx value

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size: Custom | Document Number: Latitude300 Haswell | Rev: X00

Date: Tuesday, March 19, 2013 | Sheet 83 of 104

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

Date: Friday, March 15, 2013 Sheet 84 of 104

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

SSID = Mechanical

S1 STF237R117H83-1-GP — 34.4CK01.001

S2 STF237R117H83-1-GP — 34.4CK01.001

S3 STF237R113H111-GP — 34.4V802.001

H1 Do Not Stuff — Do Not Stuff

H2 Do Not Stuff — Do Not Stuff

H3 Do Not Stuff — Do Not Stuff

H4 Do Not Stuff — Do Not Stuff

H5 Do Not Stuff — Do Not Stuff

H6 Do Not Stuff — Do Not Stuff

H9 Do Not Stuff — Do Not Stuff

H8 Do Not Stuff — Do Not Stuff

SP02 SPRING-102-GP — 34.41V01.001

SP03 SPRING-102-GP — 34.41V01.001

C1 Do Not Stuff — Do Not Stuff

C2 Do Not Stuff — Do Not Stuff

C3 Do Not Stuff — Do Not Stuff

CPU BRACKET

SP04 SPRING-62-GP — 34.39S07.003

SP05 SPRING-102-GP — 34.41V01.001

SSID = EMI

DCBATOUT

EC9701 EC9702 EC9703 EC9708 EC9705 EC9710 — DY Do Not Stuff — SC1KP25V2JX-GP

EC9711 EC9712 EC9713 EC9716 EC9714 — DY Do Not Stuff — SC1KP25V2JX-GP

1D35V_VGA_S0

EC9727 EC9725 EC9726 EC9730 EC9728 EC9729 EC9731 — DY Do Not Stuff — SC1KP25V2JX-GP

AUD_AGND

EC9739 EC9744 EC9743 EC9745 — DY Do Not Stuff — SC1KP25V2JX-GP

X01 2/27 Change to 0.1u/25V for rating

DCBATOUT

EC9740 EC9741 EC9742 EC9747 EC9748 EC9749 EC9750 EC9751 — DY Do Not Stuff — SC1KP25V2JX-GP

5V_S0

EC9720 EC9719 EC9718 EC9723 EC9721 EC9722 EC9724 — DY Do Not Stuff

3D3V_S0

EC9737 EC9735 EC9736 EC9738 — DY Do Not Stuff

5V_S5

EC9734 EC9732 EC9733 — DY Do Not Stuff

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *UNUSED PARTS/EMI Capacitors*

Size: A3 | Document Number: Latitude300 Haswell | Rev: X00

Date: Friday, March 15, 2013 | Sheet 86 of 104

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

Date: Friday, March 15, 2013 Sheet 90 of 104

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Express Card

Size	Document Number	Rev
A3	***Latitude300 Haswell***	***X00***

Date: Friday, March 15, 2013 Sheet 93 of 104

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 94 of 104

(Blanking)

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

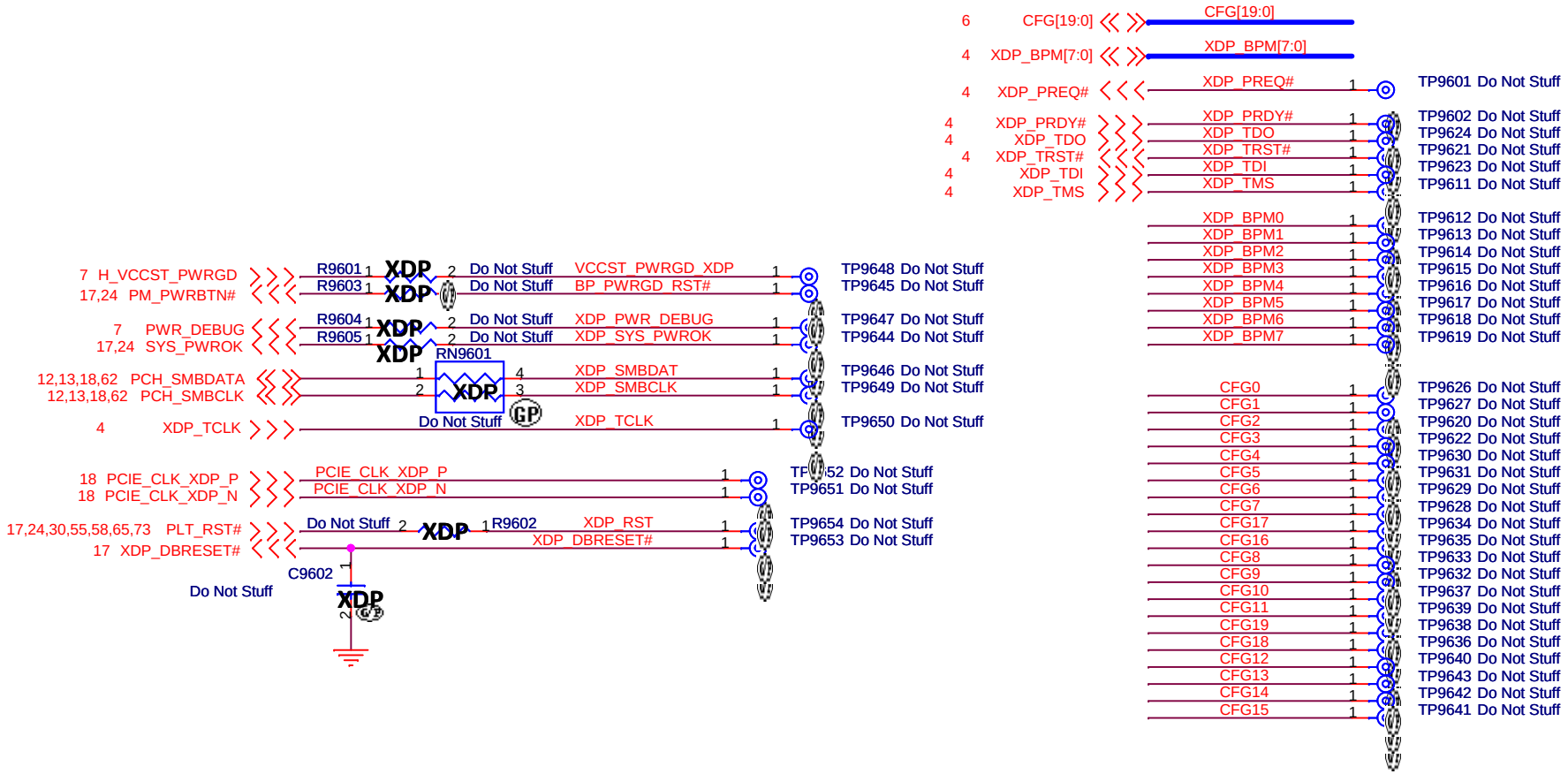
Title: *CRT_Switch*

Size	Document Number	Rev
A3	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 95 of 104

SSID = XDP

CPU XDP



UM

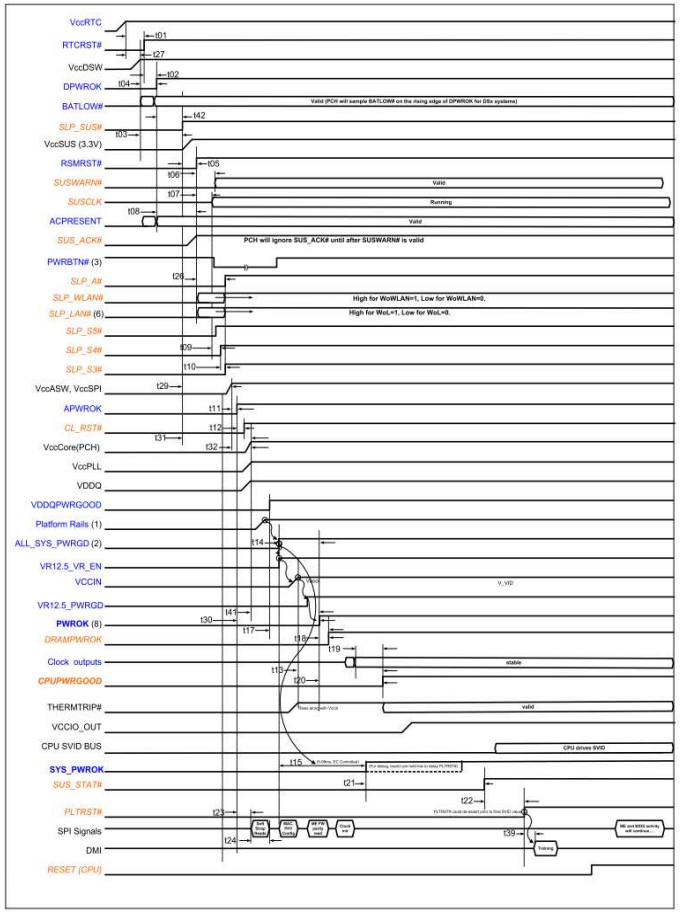
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TOUCH PANEL

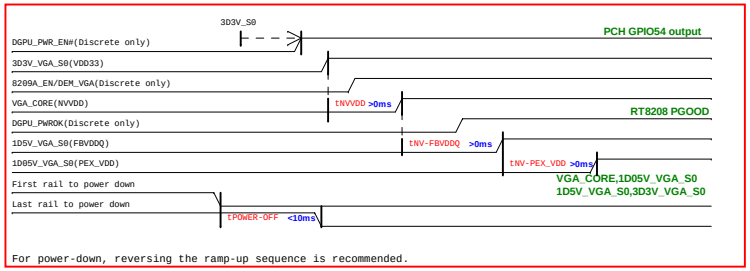
Size	Document Number	Rev
A4	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 96 of 104

Shark Bay Platform Power Sequence



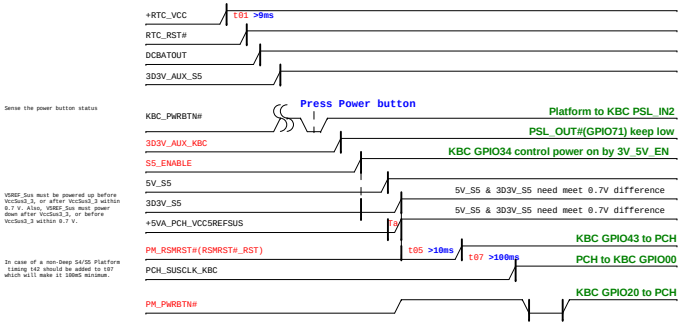
N14P-GT Power-Up/Down Sequence

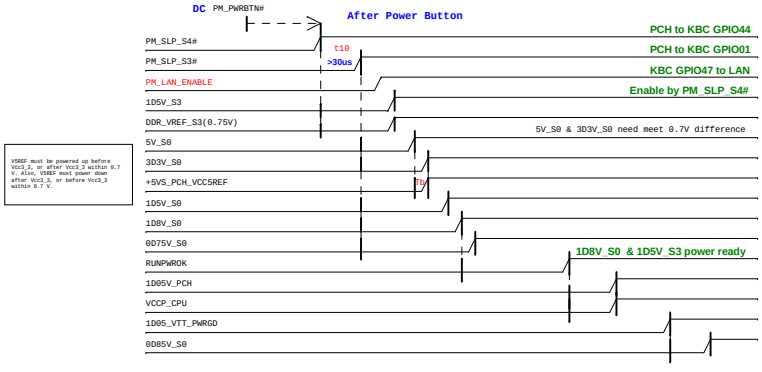


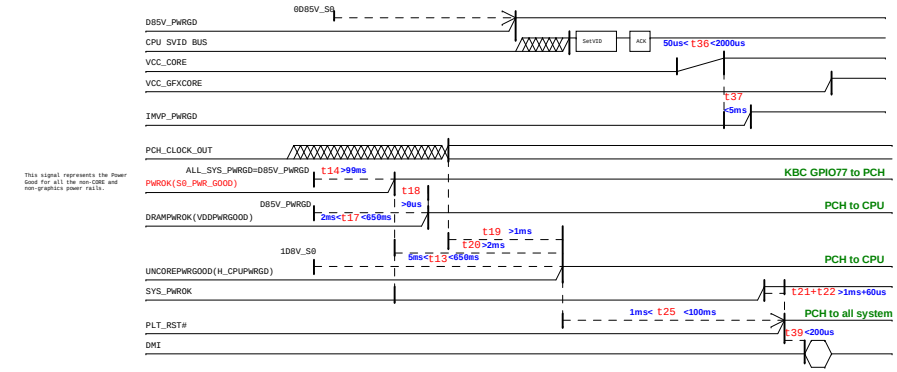
For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

Red Words: Controlled by EC GPIO







UM

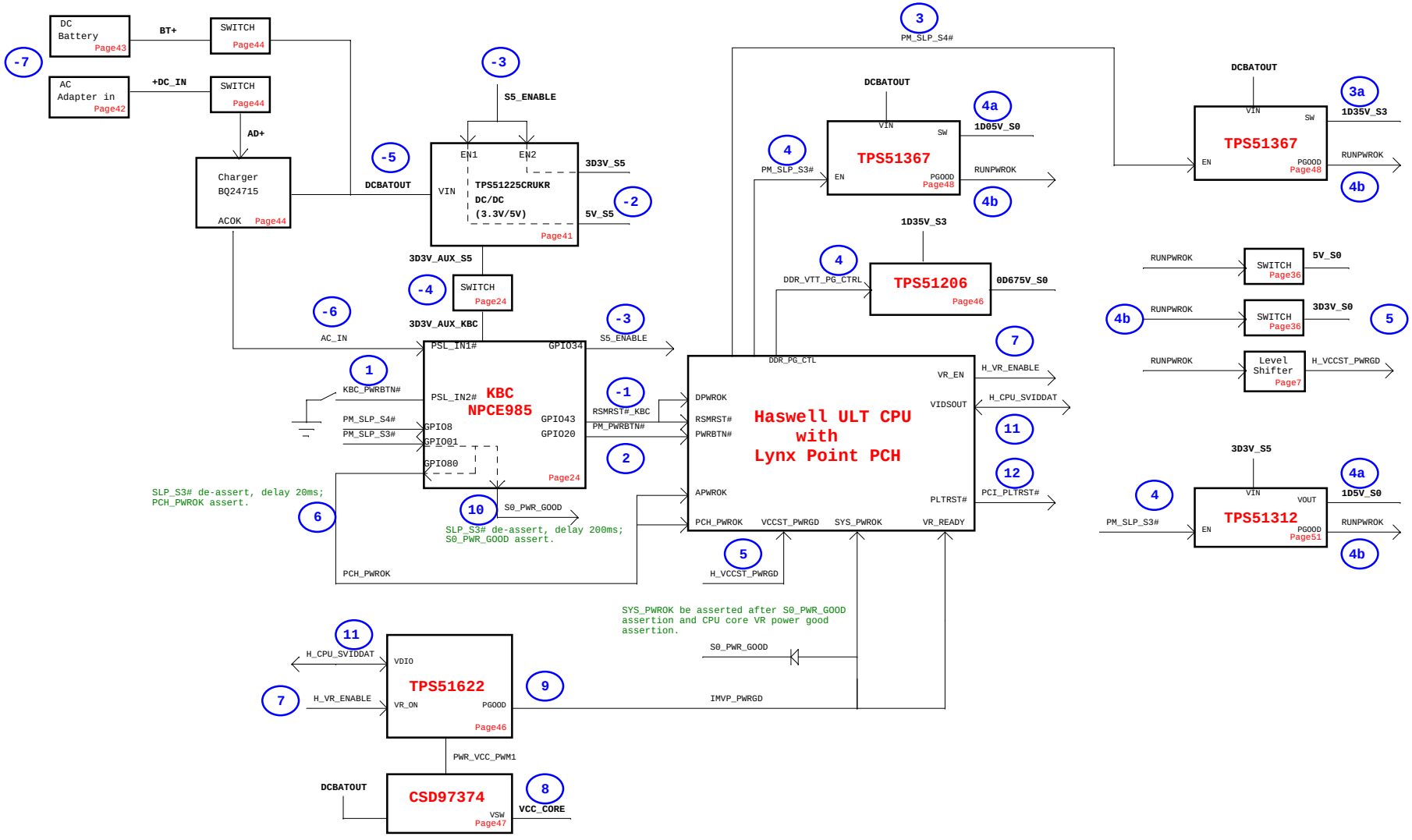
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size	Document Number	Rev
A1	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 97 of 104

Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



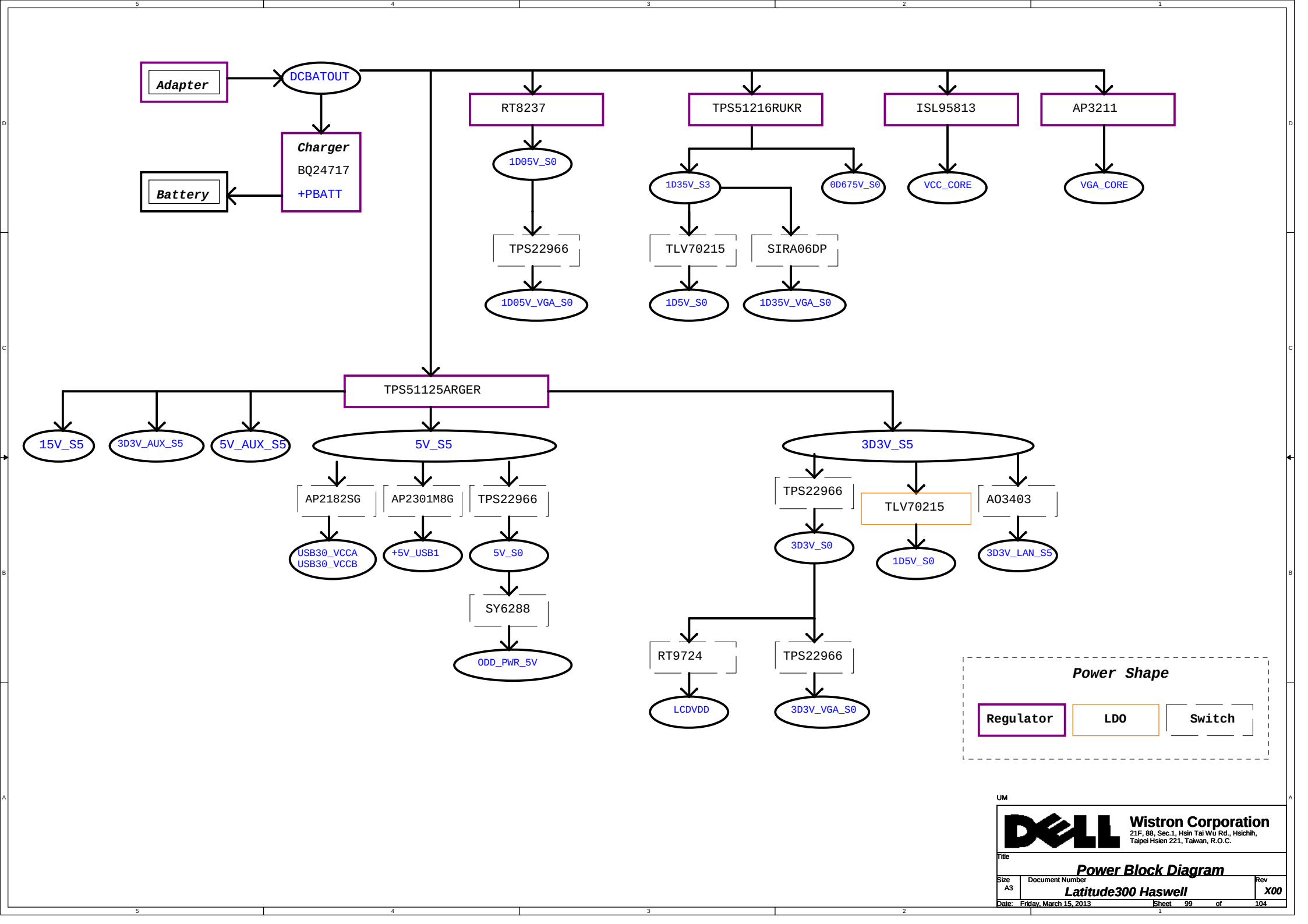
UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence Diagram

Size	Document Number	Rev
A2	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 98 of 104



UM

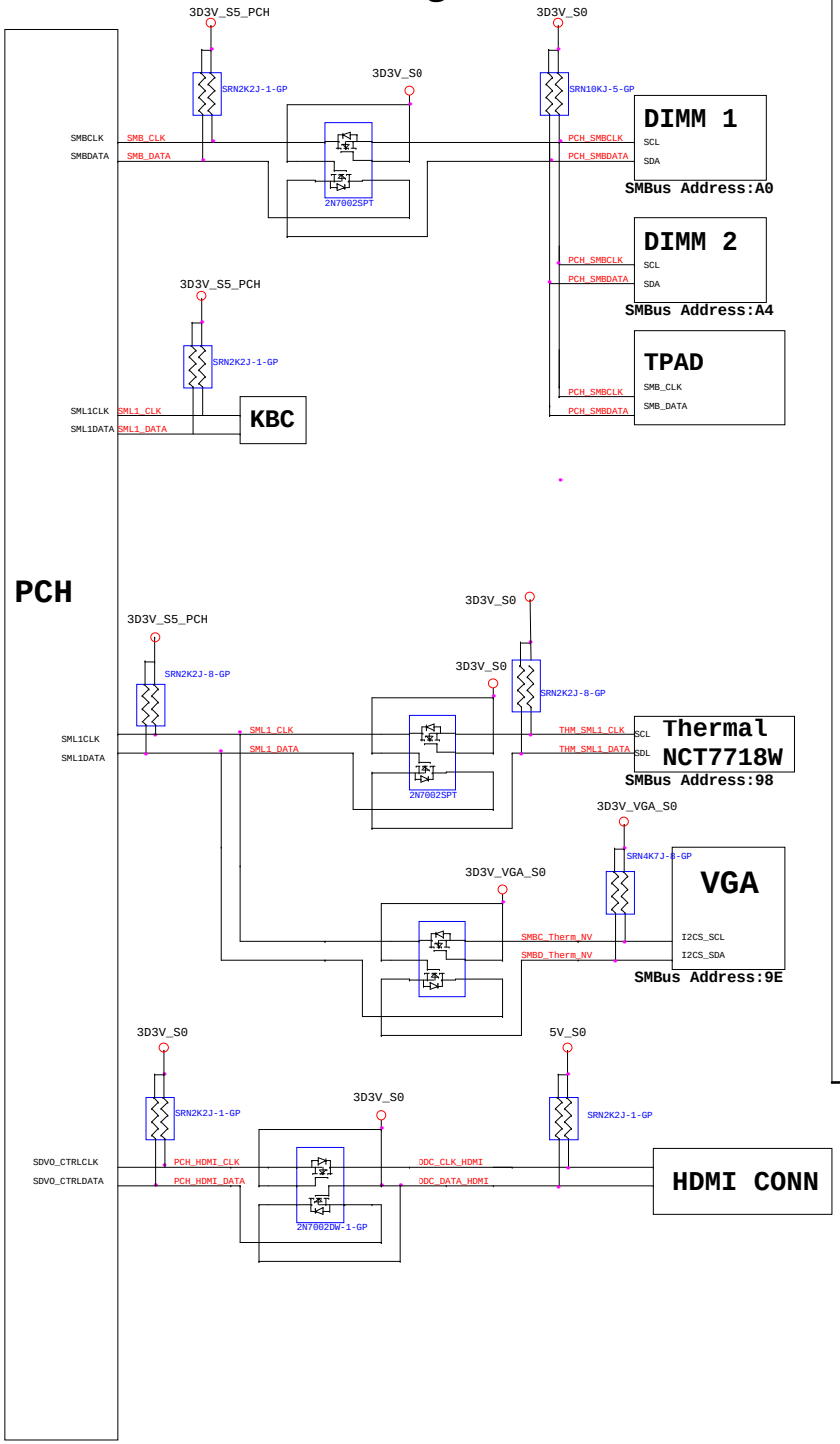
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

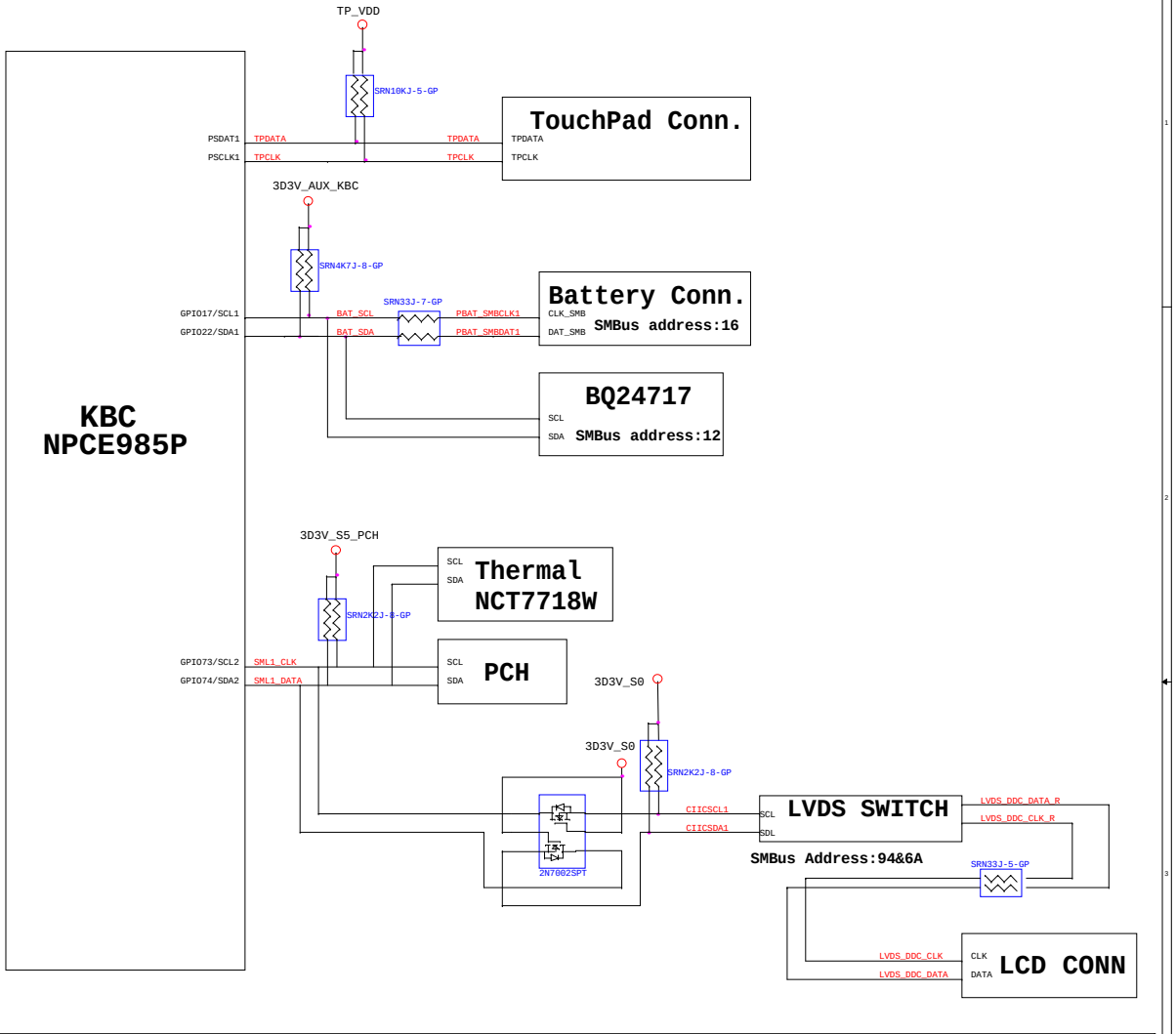
Size	Document Number	Rev
A3	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 99 of 104

PCH SMBus Block Diagram



KBC SMBus Block Diagram



UM

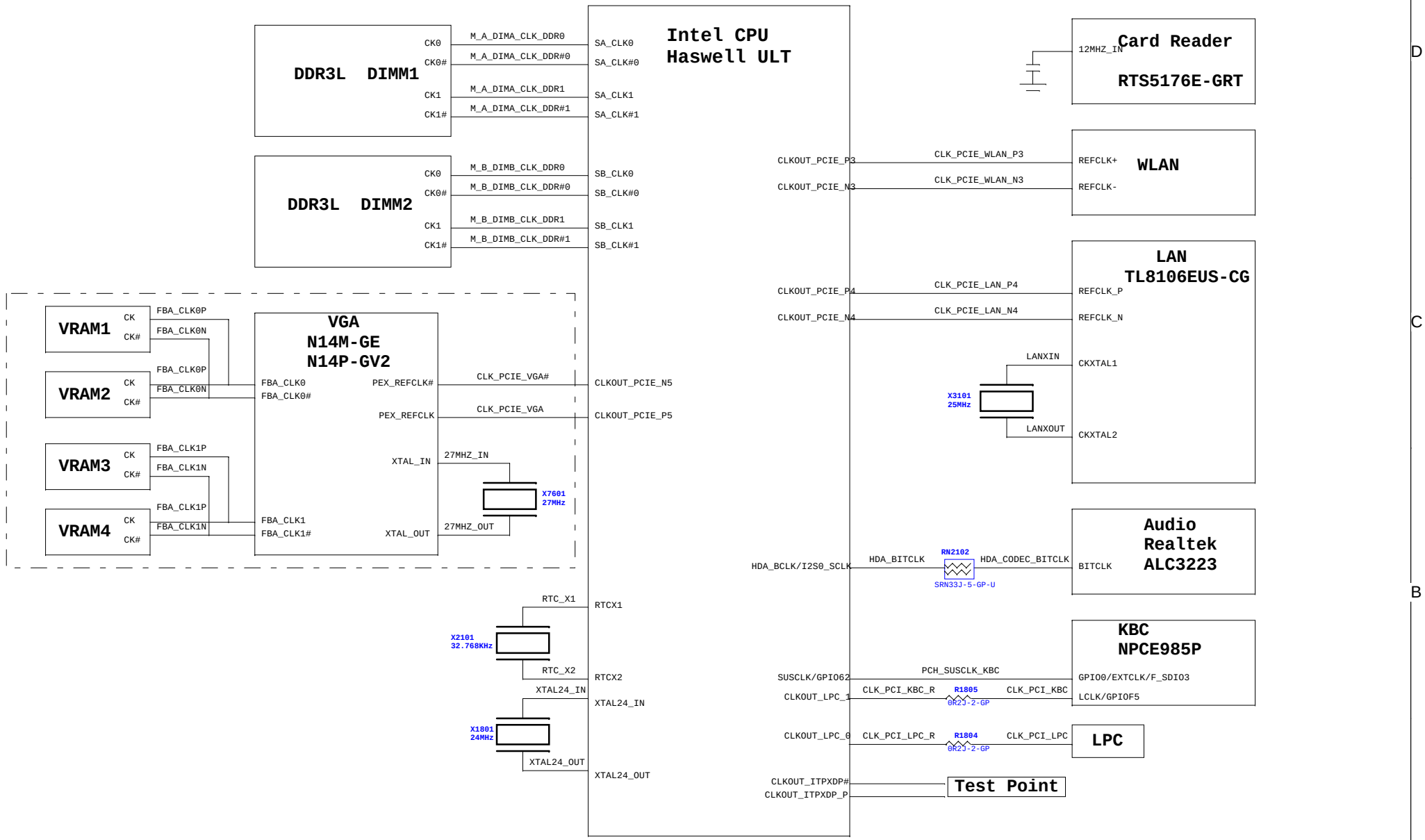
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 100 of 104

OAK Haswell CLK Block Diagram



UM

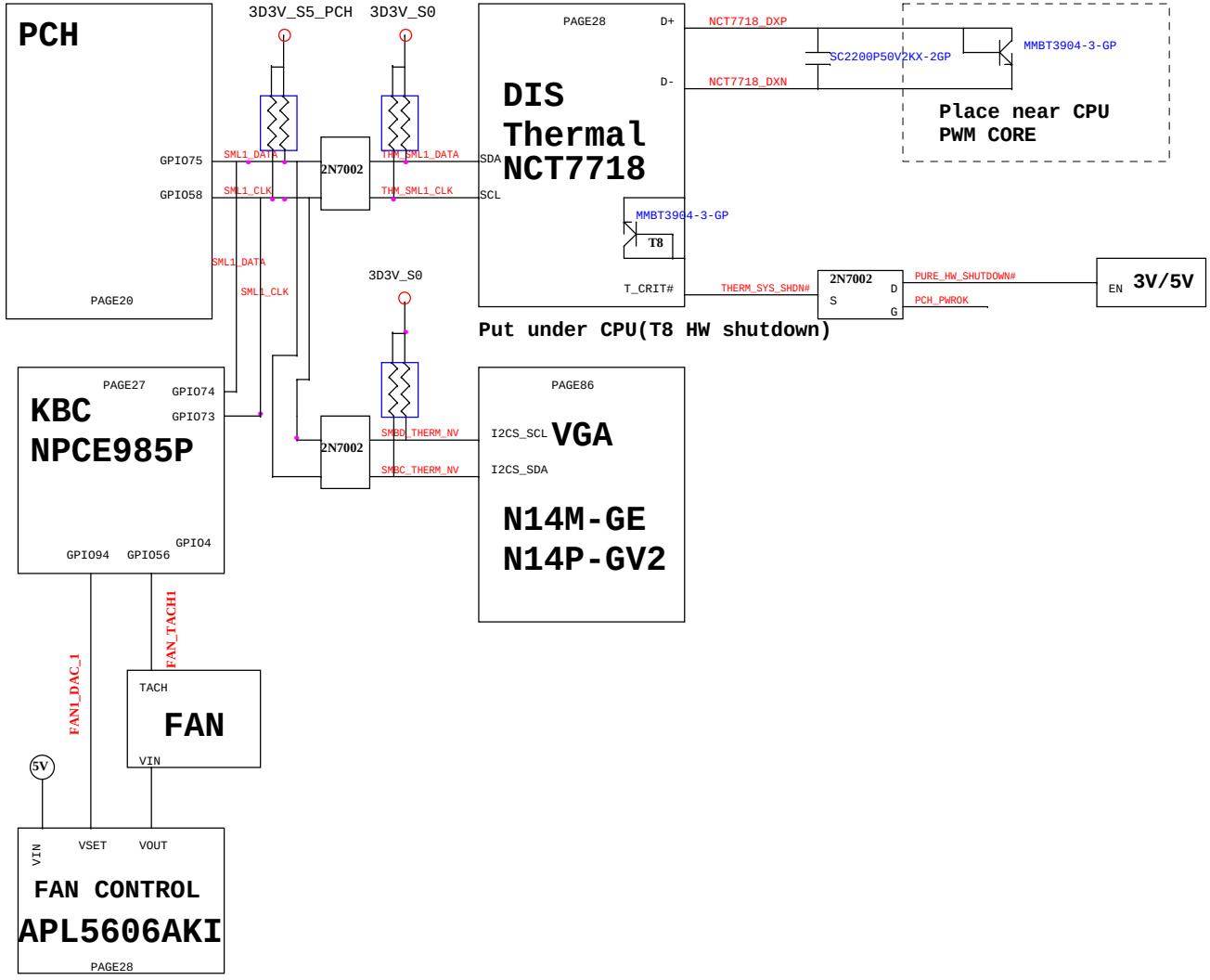
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLK Block Diagram

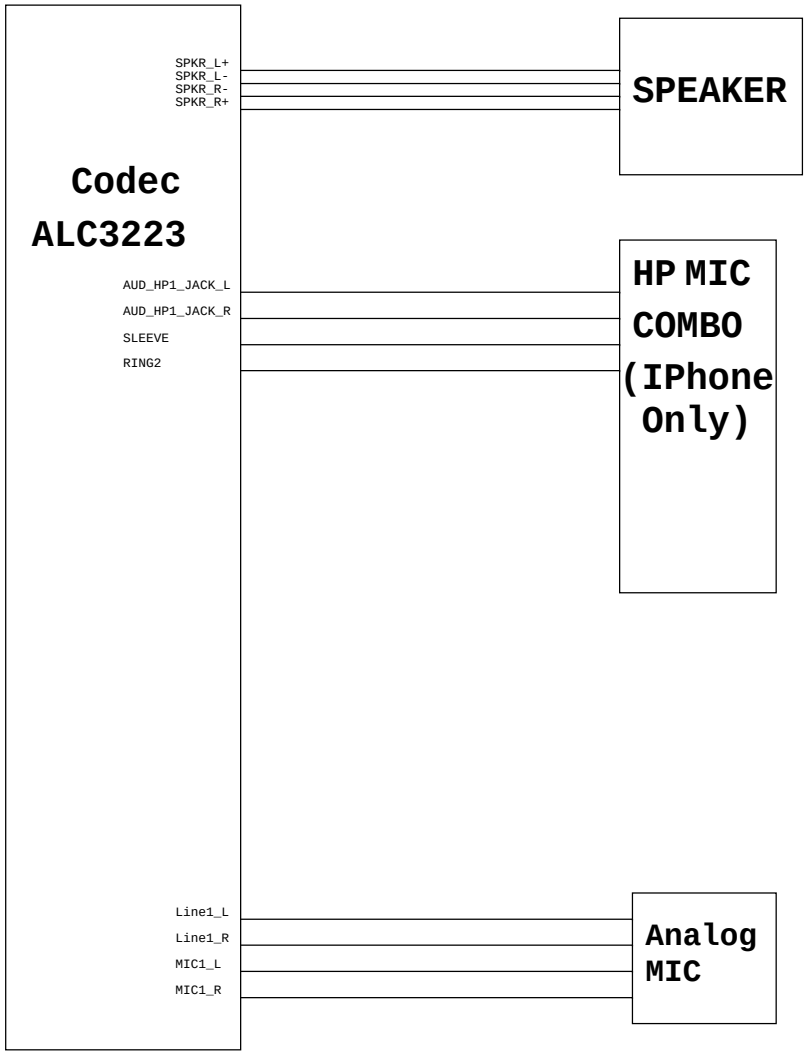
Size	Document Number	Rev
A2	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 101 of 104

Thermal Block Diagram



Audio Block Diagram



UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	Latitude300 Haswell	X00

Date: Friday, March 15, 2013 Sheet 102 of 104

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER
	X01	2/26	17	XDP_DBRESET# 10K to 3.3V	EE
		2/26	17	PCH_Wake# to 1K and DY R1705	EE

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size	Document Number	Rev
A3	*Latitude300 Haswell*	*X00*

Date: Friday, March 15, 2013 Sheet 103 of 104

VERSION	DATA	PAGE	Change Iteam

UM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Change History***

Size	Document Number	Rev
A3	***Latitude300 Haswell***	***X00***

Date: Friday, March 15, 2013 Sheet 104 of 104