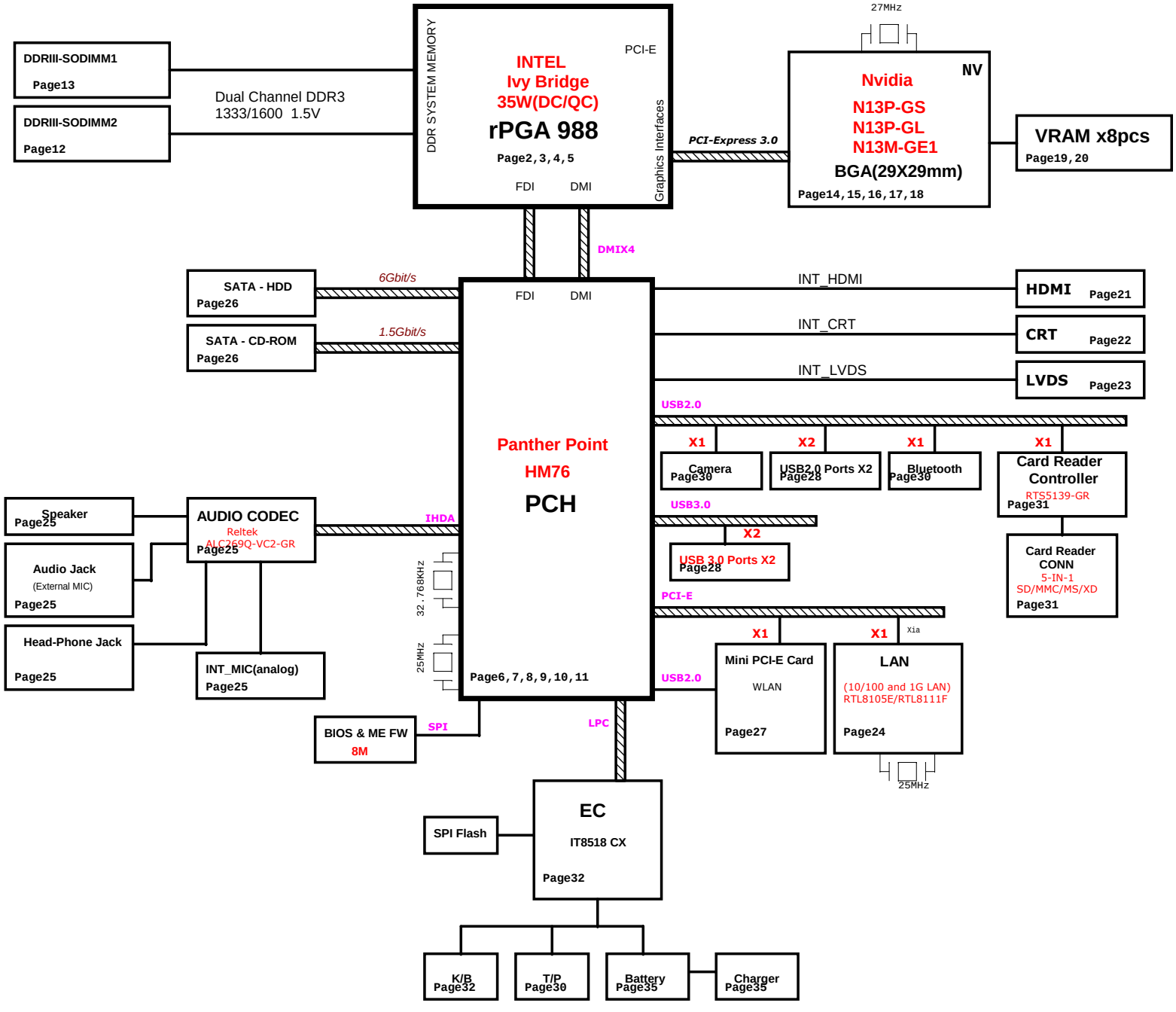
LZ2/LZ2A (Z480) Intel Chief River Platform (Optimus) Block Diagram

01



PROJECT : LZ2A
Quanta Computer Inc.

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Ivy Bridge Processor (DMI,PEG,FDI)

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

U36A

DMI_TXN0 B27 DMI_RX#[0]
DMI_TXN1 B25 DMI_RX#[1]
DMI_TXN2 A25 DMI_RX#[2]
DMI_TXN3 B24 DMI_RX#[3]
DMI_TXP0 B28 DMI_RX[0]
DMI_TXP1 B26 DMI_RX[1]
DMI_TXP2 A24 DMI_RX[2]
DMI_TXP3 B23 DMI_RX[3]
DMI_RXN0 G21 DMI_TX#[0]
DMI_RXN1 E22 DMI_TX#[1]
DMI_RXN2 F21 DMI_TX#[2]
DMI_RXN3 D21 DMI_TX#[3]
DMI_RXP0 G22 DMI_TX[0]
DMI_RXP1 D22 DMI_TX[1]
DMI_RXP2 F20 DMI_TX[2]
DMI_RXP3 C21 DMI_TX[3]

DMI

FDI_TXN0 A21 FDI0_TX#[0]
FDI_TXN1 H19 FDI0_TX#[1]
FDI_TXN2 E19 FDI0_TX#[2]
FDI_TXN3 F18 FDI0_TX#[3]
FDI_TXN4 B21 FDI1_TX#[0]
FDI_TXN5 C20 FDI1_TX#[1]
FDI_TXN6 D18 FDI1_TX#[2]
FDI_TXN7 E17 FDI1_TX#[3]
FDI_TXP0 A22 FDI0_TX[0]
FDI_TXP1 G19 FDI0_TX[1]
FDI_TXP2 E20 FDI0_TX[2]
FDI_TXP3 G18 FDI0_TX[3]
FDI_TXP4 B20 FDI1_TX[0]
FDI_TXP5 C19 FDI1_TX[1]
FDI_TXP6 D19 FDI1_TX[2]
FDI_TXP7 F17 FDI1_TX[3]
FDI_FSYNC0 J18 FDI0_FSYNC
FDI_FSYNC1 J17 FDI1_FSYNC
FDI_INT H20 FDI_INT
FDI_LSYNC0 J19 FDI0_LSYNC
FDI_LSYNC1 H17 FDI1_LSYNC

Intel(R) FDI

eDP_COMP A18 eDP_COMPIO
INT_eDP_HPD_Q A17 eDP_ICOMPO
B16 eDP_HPD
C15 eDP_AUX
D15 eDP_AUX#
C17 eDP_TX[0]
E16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
F15 eDP_TX#[3]

eDP

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils. eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

PEG_ICOMPI J22 PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_RX#[0] K33 PEG_RXN0
PEG_RX#[1] M35 PEG_RXN1
PEG_RX#[2] L34 PEG_RXN2
PEG_RX#[3] J35 PEG_RXN3
PEG_RX#[4] J32 PEG_RXN4
PEG_RX#[5] H34 PEG_RXN5
PEG_RX#[6] H31 PEG_RXN6
PEG_RX#[7] G33 PEG_RXN7
PEG_RX#[8] G30 PEG_RXN8
PEG_RX#[9] F35 PEG_RXN9
PEG_RX#[10] E34 PEG_RXN10
PEG_RX#[11] E32 PEG_RXN11
PEG_RX#[12] D33 PEG_RXN12
PEG_RX#[13] D31 PEG_RXN13
PEG_RX#[14] B33 PEG_RXN14
PEG_RX#[15] C32 PEG_RXN15

PEG_RXN[0..15] [14]

PEG_RX[0] J33 PEG_RXP0
PEG_RX[1] L35 PEG_RXP1
PEG_RX[2] K34 PEG_RXP2
PEG_RX[3] H35 PEG_RXP3
PEG_RX[4] H32 PEG_RXP4
PEG_RX[5] G34 PEG_RXP5
PEG_RX[6] G31 PEG_RXP6
PEG_RX[7] F33 PEG_RXP7
PEG_RX[8] F30 PEG_RXP8
PEG_RX[9] E35 PEG_RXP9
PEG_RX[10] E33 PEG_RXP10
PEG_RX[11] E32 PEG_RXP11
PEG_RX[12] D34 PEG_RXP12
PEG_RX[13] E31 PEG_RXP13
PEG_RX[14] C33 PEG_RXP14
PEG_RX[15] B32 PEG_RXP15

PEG_RXP[0..15] [14]

PEG_TX#[0] M29 PEG_TXN0_C
PEG_TX#[1] M32 PEG_TXN1_C
PEG_TX#[2] M31 PEG_TXN2_C
PEG_TX#[3] L32 PEG_TXN3_C
PEG_TX#[4] L29 PEG_TXN4_C
PEG_TX#[5] K31 PEG_TXN5_C
PEG_TX#[6] K28 PEG_TXN6_C
PEG_TX#[7] J30 PEG_TXN7_C
PEG_TX#[8] J28 PEG_TXN8_C
PEG_TX#[9] H29 PEG_TXN9_C
PEG_TX#[10] G27 PEG_TXN10_C
PEG_TX#[11] E29 PEG_TXN11_C
PEG_TX#[12] F27 PEG_TXN12_C
PEG_TX#[13] D28 PEG_TXN13_C
PEG_TX#[14] F26 PEG_TXN14_C
PEG_TX#[15] E25 PEG_TXN15_C

PEG_TX[0] M28 PEG_TXP0_C
PEG_TX[1] M33 PEG_TXP1_C
PEG_TX[2] M30 PEG_TXP2_C
PEG_TX[3] L31 PEG_TXP3_C
PEG_TX[4] L28 PEG_TXP4_C
PEG_TX[5] K30 PEG_TXP5_C
PEG_TX[6] K27 PEG_TXP6_C
PEG_TX[7] J29 PEG_TXP7_C
PEG_TX[8] J27 PEG_TXP8_C
PEG_TX[9] H28 PEG_TXP9_C
PEG_TX[10] G28 PEG_TXP10_C
PEG_TX[11] E28 PEG_TXP11_C
PEG_TX[12] F28 PEG_TXP12_C
PEG_TX[13] D27 PEG_TXP13_C
PEG_TX[14] E26 PEG_TXP14_C
PEG_TX[15] D25 PEG_TXP15_C

PCI EXPRESS* - GRAPHICS

Ivy Bridge_rPGA_2DPC_Rev0p61

Ivy Bridge Processor (CLK,MISC,JTAG)

U36B

H_SNB_IVB# [7] C26 PROC_SELECT#
TP12 SKTOCC# AN34 SKTOCC#

MISC

TP9 TP_CATERR# AL33 CATERR#
EC_PECI [32] AN33 PECI
H_PROCHOT# [32,41] R168 56_4 H_PROCHOT#_R AL32 PROCHOT#
PM_THRMTRIP# [9] AN32 THERMTRIP#

THERMAL

PM_SYNC [6] R448 *0_4_S PM_SYNC_R AM34 PM_SYNC
H_PWRGOOD [9] R450 *0_4_S H_PWRGOOD_R AP33 UNCOREPWRGOOD
R461 10K_4
C524 0.1U/10V_4
PM_DRAM_PWRGD_R V8 SM_DRAMPWROK
+1.05V_PCH
R421 *75_4
CPU_PLTRST# R444 *43_4 CPU_PLTRST#_R AR33 RESET#
R160 750/F_4
RV11 *EGA-0402

PWR MANAGEMENT

BCLK A28 CLK_CPU_BCLKP [8]
BCLK# A27 CLK_CPU_BCLKN [8]
DPLL_REF_CLK A16 DPLL_SSCLKP_R R533 1K/F_4 R534 *0_4 CLK_DPLL_SSCLKP [8]
DPLL_REF_CLK# A15 DPLL_SSCLKN_R R536 1K/F_4 +1.05V_PCH R537 *0_4 CLK_DPLL_SSCLKN [8]

CLOCKS

SM_DRAMRST# R8 CPU_DRAMRST#
SM_RCOMP[0] AK1 SM_RCOMP_0 R565 140/F_4
SM_RCOMP[1] AS SM_RCOMP_1 R559 25.5/F_4
SM_RCOMP[2] A4 SM_RCOMP_2 R560 200/F_4

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

DDR3 MISC

PRDY# AP29 XDP_PRDY#
PREQ# AP27 XDP_PREQ# TP19 TP17
TCK AR26 XDP_TCLK
TMS AR27 XDP_TMS TP47
TRST# AP30 XDP_TRST# TP41 TP38
TDI AR28 XDP_TDI_R TP43
TDO AP26 XDP_TDO TP56
DBR# AL35 XDP_DBRST# XDP_DBRST# [6]
BPM#[0] AT28
BPM#[1] AR29
BPM#[2] AR30
BPM#[3] AT30
BPM#[4] AP32
BPM#[5] AR31
BPM#[6] AT31
BPM#[7] AR32

JTAG & BPM

Ivy Bridge_rPGA_2DPC_Rev0p61

[4,6,7,8,10,33,34,38,43] +1.05V_PCH
[4,10,12,13,33,34,37,43] +1.5V_SUS
[6,7,8,9,10,27,31,34] +3V_S5
[4,33] +1.5V_CPU

+1.5V_SUS
R278 1K/F_4
[12,13] DDR3_DRAMRST# R280 1K/F_4 CPU_DRAMRST#_R
R275 *0_4
CPU_DRAMRST#
For ESD SC52 *0.1U/10V_4
Q31 ME2N7002E
[8] DRAMRST_CNTRL_PCH R613 0_4
FOR DEEP S3 [32] EC_DRAMRST_GATE R614 *0_4
C289 0.047U/10V_4
R271 4.99K/F_4
[12,13] DRAMRST_CNTRL_DDR

CPU_PLTRST#_R
R147 1.5K/F_4
+3V_S5
C500 *0.1U/10V_4
U32 NC VCC IN GND OUT *74LVC1G07GW
[8,14,24,27] PLTRST#
CPU_PLTRST#

+3V_S5
C290 *0.1U/10V_4
U15 *74AHC1G09GW
[6] SYS_PWROK
[6] PM_DRAM_PWRGD
R268 *0_4
R270 *0_4_S
PM_DRAM_PWRGD_Q
R272 *3K/F_4
PM_DRAM_PWRGD_Q
R269 130/F_4
PM_DRAM_PWRGD_R
+1.5V_CPU
R274 200/F_4
R273 39_4
Q30 ME2N7002E
MAINON# [4,34]

PEG x16 (UMA Non-stuff)

0.1uF AC coupling Caps for PCIE GEN2
0.22uF AC coupling Caps for PCIE GEN3

PEG_TXP[0..15] [14]

PEG_TXP0_C C499 DIS@0.1U/10V/X5R_4 PEG_TXP0
PEG_TXP1_C C475 DIS@0.1U/10V/X5R_4 PEG_TXP1
PEG_TXP2_C C513 DIS@0.1U/10V/X5R_4 PEG_TXP2
PEG_TXP3_C C493 DIS@0.1U/10V/X5R_4 PEG_TXP3
PEG_TXP4_C C487 DIS@0.1U/10V/X5R_4 PEG_TXP4
PEG_TXP5_C C508 DIS@0.1U/10V/X5R_4 PEG_TXP5
PEG_TXP6_C C477 DIS@0.1U/10V/X5R_4 PEG_TXP6
PEG_TXP7_C C504 DIS@0.1U/10V/X5R_4 PEG_TXP7
PEG_TXP8_C C478 DIS@0.1U/10V/X5R_4 PEG_TXP8
PEG_TXP9_C C502 DIS@0.1U/10V/X5R_4 PEG_TXP9
PEG_TXP10_C C481 DIS@0.1U/10V/X5R_4 PEG_TXP10
PEG_TXP11_C C494 DIS@0.1U/10V/X5R_4 PEG_TXP11
PEG_TXP12_C C483 DIS@0.1U/10V/X5R_4 PEG_TXP12
PEG_TXP13_C C491 DIS@0.1U/10V/X5R_4 PEG_TXP13
PEG_TXP14_C C484 DIS@0.1U/10V/X5R_4 PEG_TXP14
PEG_TXP15_C C497 DIS@0.1U/10V/X5R_4 PEG_TXP15

0.1uF AC coupling Caps for PCIE GEN2
0.22uF AC coupling Caps for PCIE GEN3

PEG_TXN[0..15] [14]

PEG_TXN0_C C498 DIS@0.1U/10V/X5R_4 PEG_TXN0
PEG_TXN1_C C474 DIS@0.1U/10V/X5R_4 PEG_TXN1
PEG_TXN2_C C514 DIS@0.1U/10V/X5R_4 PEG_TXN2
PEG_TXN3_C C492 DIS@0.1U/10V/X5R_4 PEG_TXN3
PEG_TXN4_C C486 DIS@0.1U/10V/X5R_4 PEG_TXN4
PEG_TXN5_C C509 DIS@0.1U/10V/X5R_4 PEG_TXN5
PEG_TXN6_C C476 DIS@0.1U/10V/X5R_4 PEG_TXN6
PEG_TXN7_C C503 DIS@0.1U/10V/X5R_4 PEG_TXN7
PEG_TXN8_C C479 DIS@0.1U/10V/X5R_4 PEG_TXN8
PEG_TXN9_C C501 DIS@0.1U/10V/X5R_4 PEG_TXN9
PEG_TXN10_C C480 DIS@0.1U/10V/X5R_4 PEG_TXN10
PEG_TXN11_C C495 DIS@0.1U/10V/X5R_4 PEG_TXN11
PEG_TXN12_C C482 DIS@0.1U/10V/X5R_4 PEG_TXN12
PEG_TXN13_C C490 DIS@0.1U/10V/X5R_4 PEG_TXN13
PEG_TXN14_C C485 DIS@0.1U/10V/X5R_4 PEG_TXN14
PEG_TXN15_C C496 DIS@0.1U/10V/X5R_4 PEG_TXN15

DP & PEG Compensation

+1.05V_PCH R527 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

+1.05V_PCH R532 *10K_4 INT_eDP_HPD_Q
+1.05V_PCH R528 24.9/F_4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)

+1.05V_PCH
H_PROCHOT# R164 62/F_4
XDP_TDO R178 51_4
XDP_TMS R480 51_4
XDP_TDI_R R477 51_4
XDP_PREQ# R172 *51_4
XDP_TCLK R487 51_4
XDP_TRST# R470 51_4

PROJECT : LZ2A
Quanta Computer Inc.

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	IVY Bridge 1/4	1A

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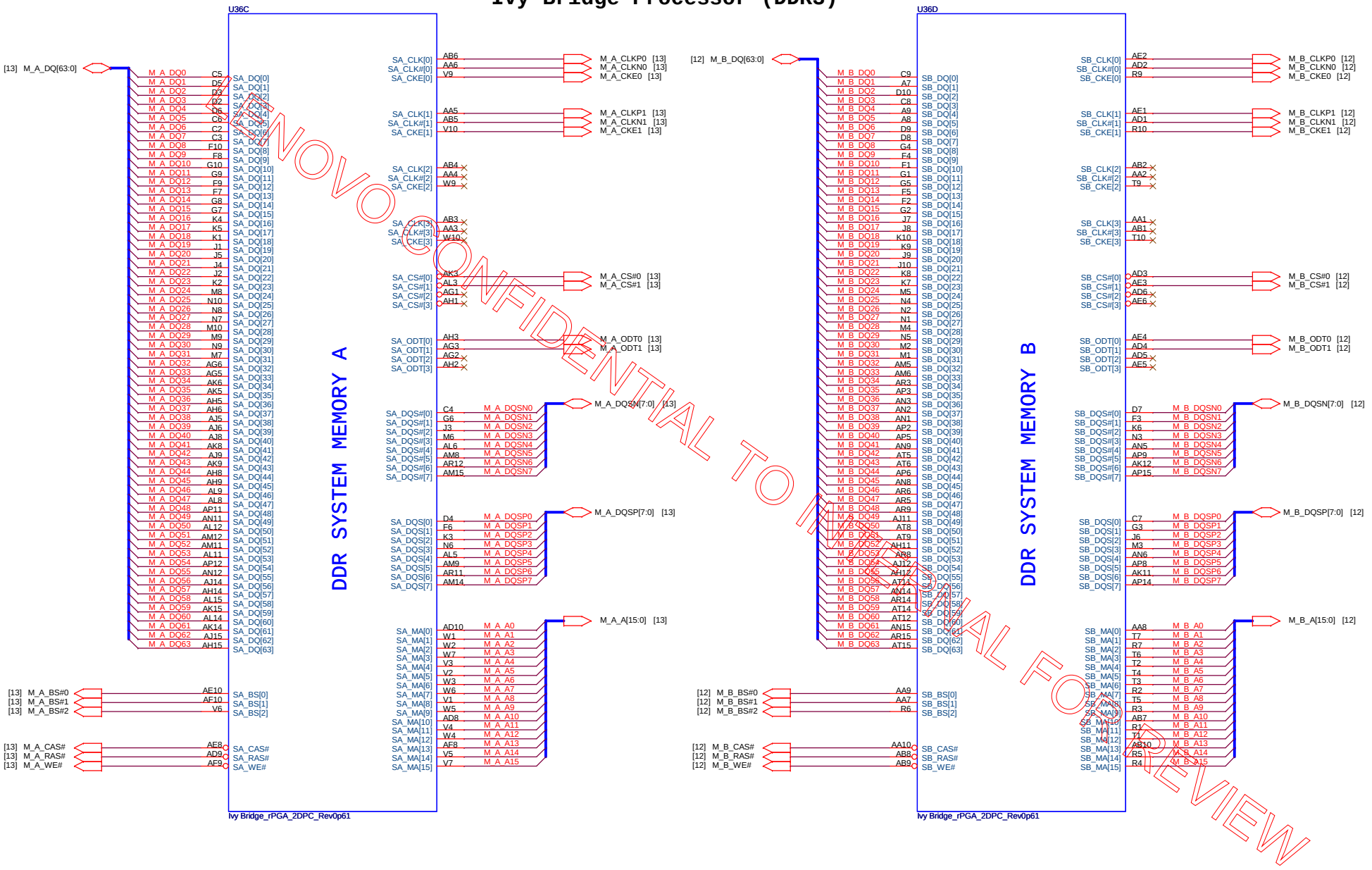
Ivy Bridge Processor (DDR3)



PROJECT : LZ2A
Quanta Computer Inc.

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Ivy Bridge Processor (GRAPHIC POWER)

04

POWER

POWER

U36F

U36G

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

GRAPHICS

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

+VCC_CORE

SNB: 55A
IVY: 55A

22uF_8 x8 Socket TOP cavity

10uF_8 x10 Socket BOT cavity

+VCC_CORE:
22uF_8 x8 TOP Socket cavity
22uF_8 x8 TOP Socket edge
10uF_8 x10 BOT Socket cavity

+1.05V_PCH

SNB: 8.5A
IVY: 8.5A

22uF_8 x7 TOP Socket cavity
22uF_8 x5 BOT Socket cavity

22uF (Reserved)

+VCC_GFX

SNB: 21.5A
IVY: 33A

+VCC_GFX:
22uF_8 x2 TOP Socket cavity
22uF_8 x4 TOP Socket edge
22uF_8 x2 BOT Socket cavity
22uF_8 x4 BOT Socket edge

+1.8V

CPU VCCPL
SNB 45W:1.5A
330uF/7mohm x 1
10uF x 1
1uF x 2

Ivy Bridge_rPGA_2DPC_Rev0p61

VCC_SENSE [41]
VSS_SENSE [41]
VTT_SENSE [38]
VSSP_SENSE [38]
VR_SVID_CLK [41]
VR_SVID_DATA [41]
VR_SVID_ALERT# [41]

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
Close to VR
R484 54.9/F_4

Place PU resistor close to CPU
R158 130/F_4

SVID DATA
Close to VR
R469 130/F_4

Place PU resistor close to CPU
R157 75_4

SVID ALERT

+VDDR_REF_CPU
[12,13,37] SMDDR_VREF
[34] MAINON_15V
Q51 ME2N7002E
R563 100K_4

SNB: 5A
IVY: 5A

330uF x1, 10uF_8 x6 Socket BOT edge.

SNB: 6A
IVY: 6A

330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

5A
Q35 AON7406
Q36 ME2N7002E
40mile routing
Placement close to CPU.

PROJECT : LZ2A
Quanta Computer Inc.
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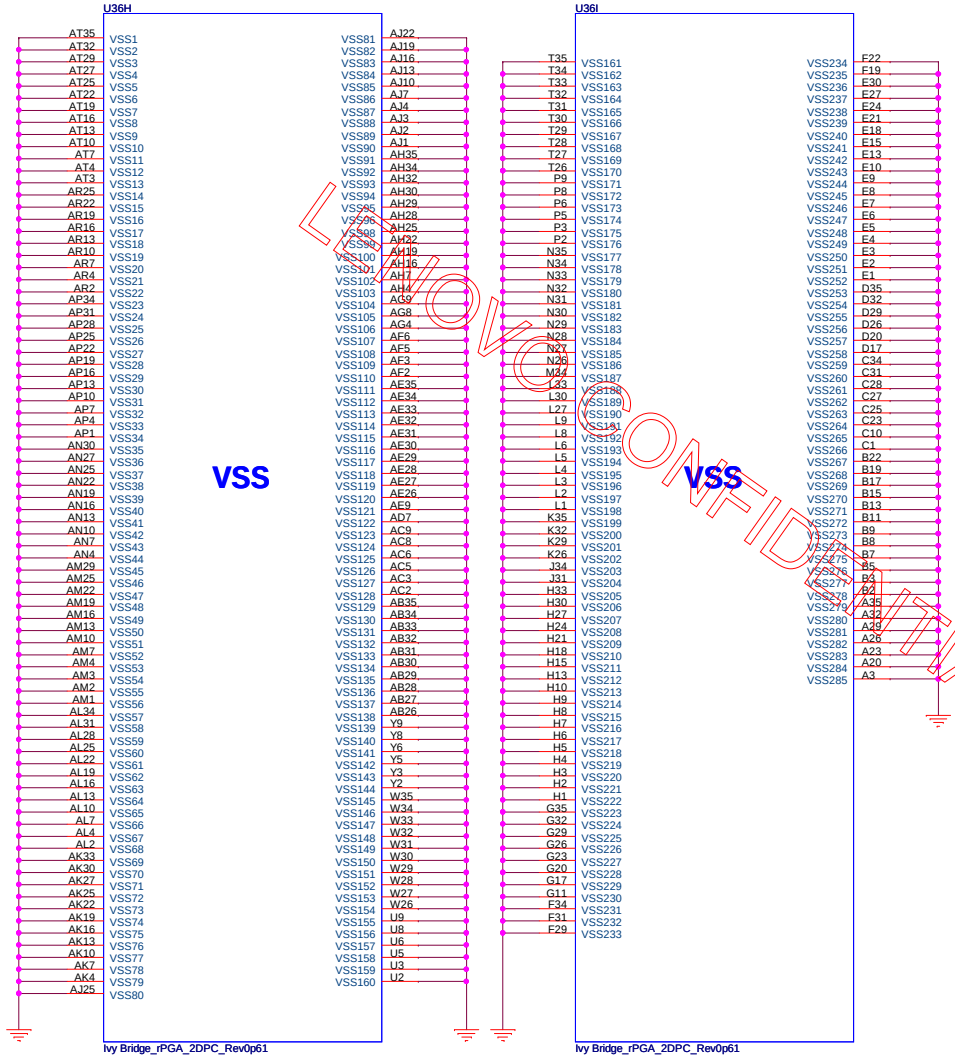
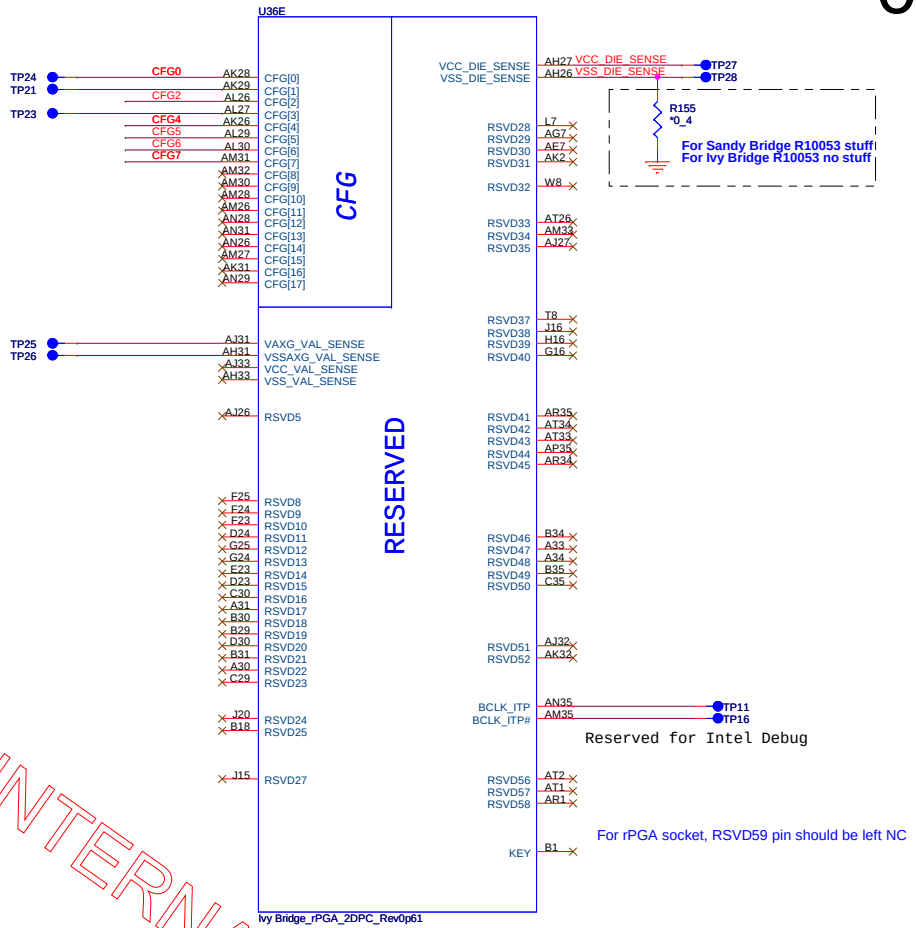
Ivy Bridge Processor (GND)



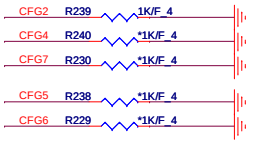
Ivy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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[2,4,7,8,10,33,34,38,43] +1.05V_PCH
[7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[2,7,8,9,10,27,31,34] +3V_S5
[7,10,32] +3V_RTC

Cougar Point/Panther Point (DMI,FDI,PM)

U13C

DMI: DMI0RXN DMI1RXN DMI2RXN DMI3RXN / DMI0RXP DMI1RXP DMI2RXP DMI3RXP / DMI0TXN DMI1TXN DMI2TXN DMI3TXN / DMI0TXP DMI1TXP DMI2TXP DMI3TXP / DMI_ZCOMP / DMI_IRCOMP / DMI2RBIAS

FDI: FDI_RXN0-7 / FDI_RXP0-7 / FDI_INT / FDI_FSYNC0 / FDI_FSYNC1 / FDI_LSYNC0 / FDI_LSYNC1

System Power Management: DSWVRMEN / DPWROK / WAKE# / CLKRUN# / GPIO32 / SUS_STAT# / GPIO61 / SUSCLK / GPIO62 / SLP_S5# / GPIO63 / SLP_S4# / SLP_S3# / SLP_A# / SLP_SUS# / PMSYNCH / SLP_LAN# / GPIO29 / SUSACK# / SYS_RESET# / SYS_PWROK / PWROK / APWROK / DRAMPWROK / RSMRST# / SUSWARN#/SUSPWRDNACK/GPIO30 / PWRBTN# / ACPRESENT / GPIO31 / BATLOW# / GPIO72 / RI#

CPT_PPT_Rev_0p5

FOR DEEP S3

Cougar Point/Panther Point (LVDS,DDI)

U13D

LVDS: L_BKLTEN L_VDD_EN L_BKLTCTL L_DDC_CLK L_DDC_DATA L_CTRL_CLK L_CTRL_DATA LVD_IBG LVD_VBG LVD_VREFH LVD_VREFL LVDSA_CLK# LVDSA_CLK LVDSA_DATA#0-3 LVDSA_DATA0-3 LVDSB_CLK# LVDSB_CLK LVDSB_DATA#0-3 LVDSB_DATA0-3

CRT: CRT_BLUE CRT_GREEN CRT_RED CRT_DDC_CLK CRT_DDC_DATA CRT_HSYNC CRT_VSYNC DAC_IREF CRT_IRTN

Digital Display Interface: SDVO_TVCLKINN/INP SDVO_STALLN/STALLP SDVO_INTN/INTP SDVO_CTRLCLK/CTRLDATA DDPB_AUXN/AUXP/HPD DDPB_0N/0P 1N/1P 2N/2P 3N/3P DDPC_CTRLCLK/CTRLDATA DDPC_AUXN/AUXP/HPD DDPC_0N/0P 1N/1P 2N/2P 3N/3P DDPD_CTRLCLK/CTRLDATA DDPD_AUXN/AUXP/HPD DDPD_0N/0P 1N/1P 2N/2P 3N/3P

INT. HDMI: INT_HDMI_SCL, INT_HDMI_SDA, INT_HDMI_HPD_Q, INT_HDMI_TXDN2/DP2/DN1/DP1/DN0/DP0/CN/CP

INT. DP: DDPC_HPD_PU R548 10K_4 — Follow PDG eDP disable guide; DDPD_HPD_PU R547 10K_4 — Follow PDG eDP disable guide

R place close to PCH: R183 150/F_4 INT_CRT_BLU; R193 150/F_4 INT_CRT_GRE; R192 150/F_4 INT_CRT_RED

R496 2.2K_4, R489 2.2K_4, R511 2.37K/F_4, T22 LVD_IBG

R176 33_4 INT_CRT_HSYNC_R, R182 33_4 INT_CRT_VSYNC_R, R506 1K/F_4

R535 *0_4_S, R523 *100K_4, R540 100K_4

CPT_PPT_Rev_0p5

DPWROK FOR DSW (DEEP S3)

+3V_DSW, +3VPCU, +3VPCU

FOR DEEP S3

D28 *RB500V-40, D29 *RB500V-40, Q55 *LTC044EUBFS8TL, Q56 *2N7002

R616 *10K_4, R617 *10K_4, C665 *0.1U/10V/X5R_4 add cap to timing tune

DPWROK

System PWR_OK(CLG)

+3V_S5

U7 TC7SH08FU

C171 0.1U/10V_4

[2] SYS_PWROK → SYS_PWROK → DELAY_VR_PWRGOOD [41]

EC_PWROK

R117 *0_4, R112 100K_4

On Die DSW VR Enable

High = Enable (Default)

Low = Disable

+3V_RTC

R127 330K_4

DSWVREN

R140 *330K_4

PCH Pull-high/low(CLG)

+3V, +3V_S5

CLKRUN# R198 8.2K_4

XDP_DBRST# R180 1K_4, R173 *1K_4

RSMRST# R139 10K_4

SYS_PWROK R457 100K_4

PM_RI# R142 10K_4

PM_BATLOW# R445 8.2K_4

PCIE_WAKE# R146 10K_4

WLAN_AOAC_ON R418 10K_4

SUSWARN# R409 10K_4

AC_PRESENT R442 10K_4

PM_DRAM_PWRGD R435 *200/F_4

For AOAC

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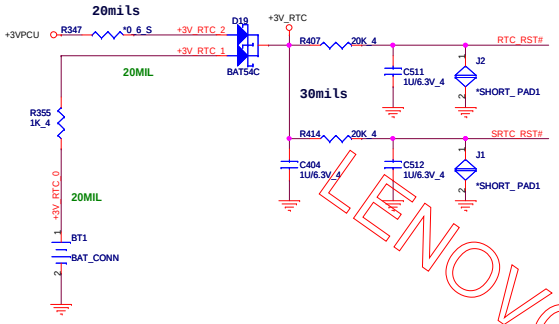
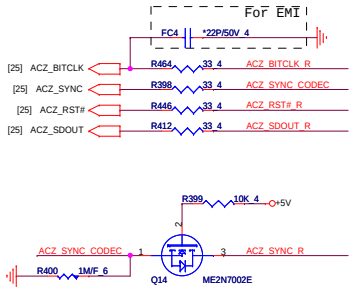
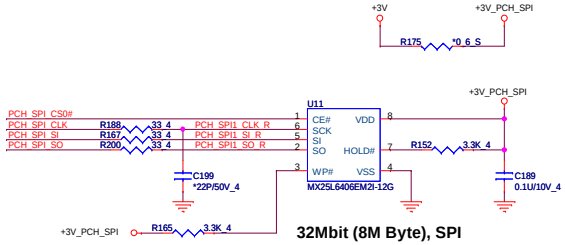
RTC Circuitry(RTC)



HDA Bus(CLG)

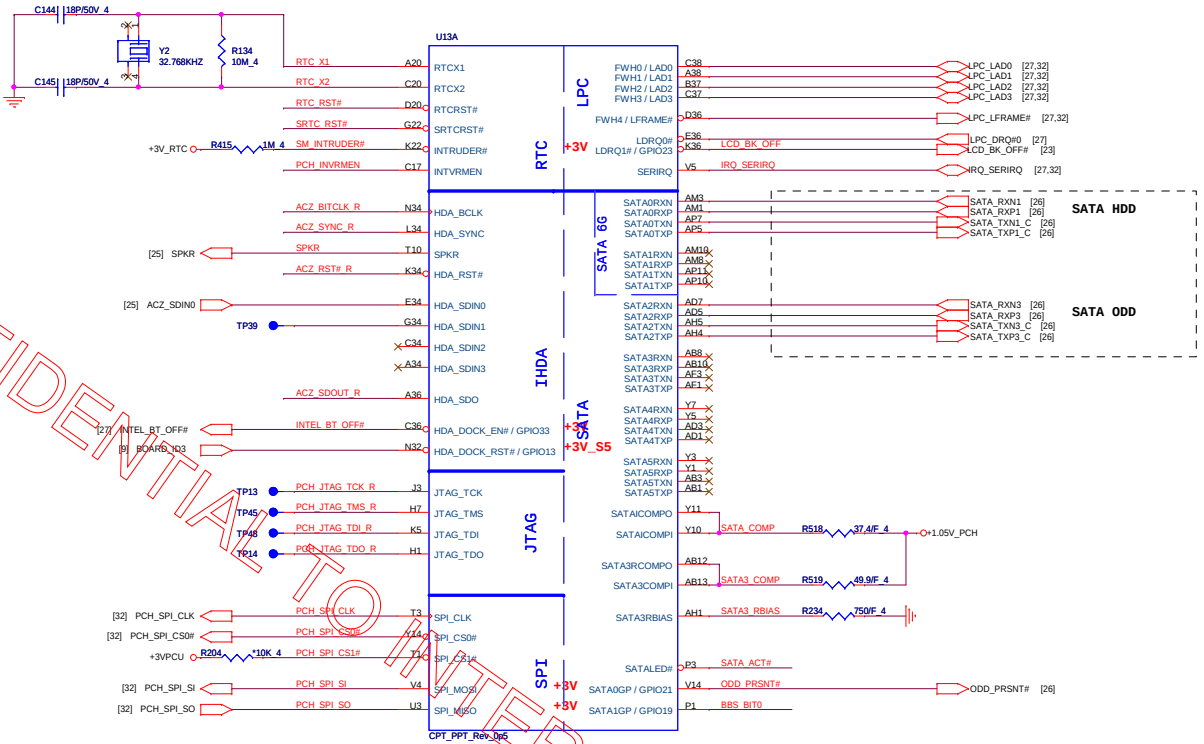


PCH Dual SPI (CLG)



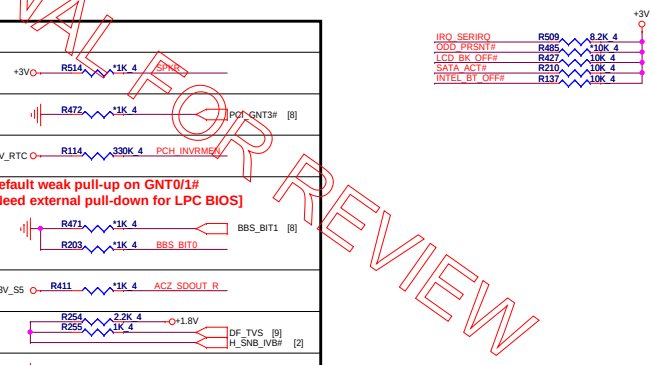
32Mbit (8M Byte), SPI

Cougar Point/Panther Point (HDA,JTAG,SATA)

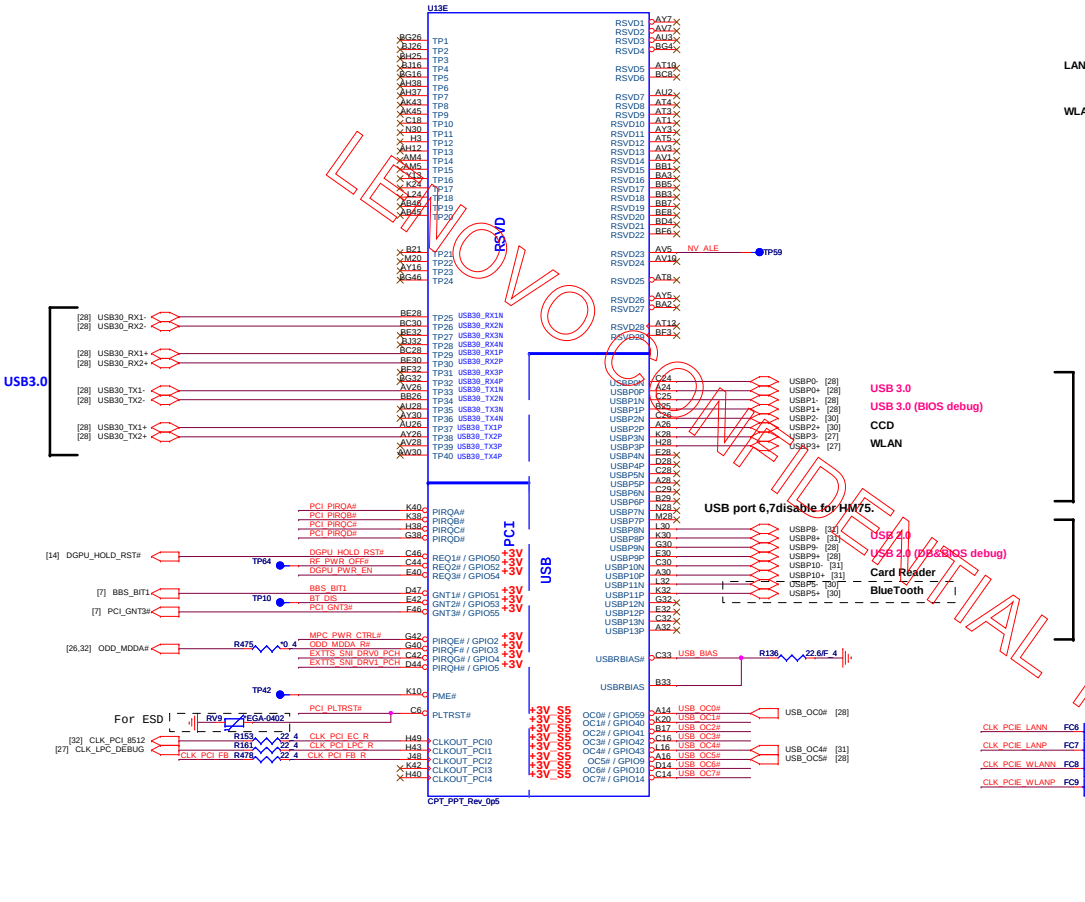


PCH Strap Table

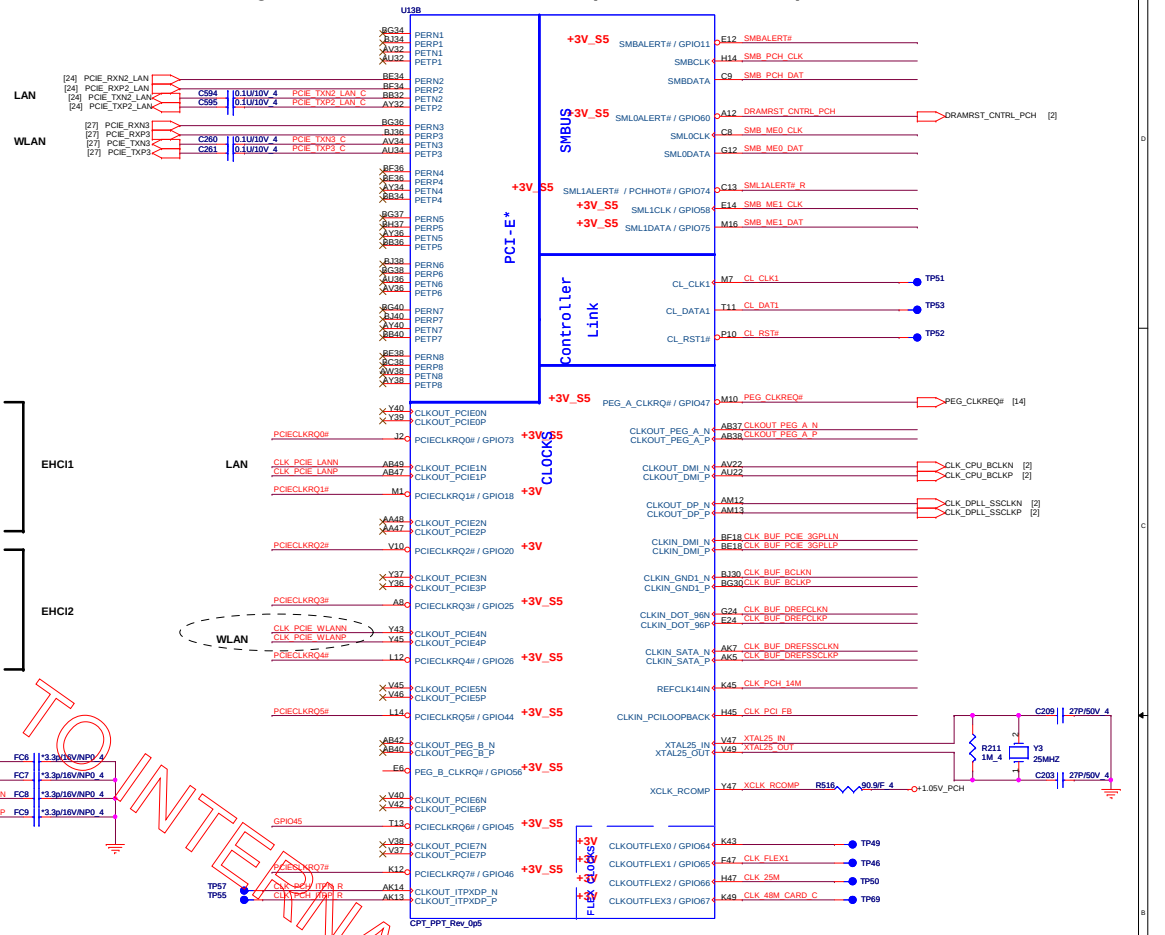
Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)



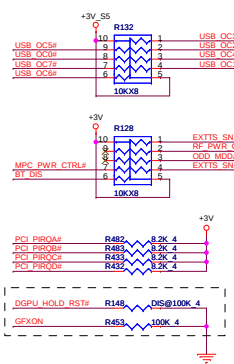
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



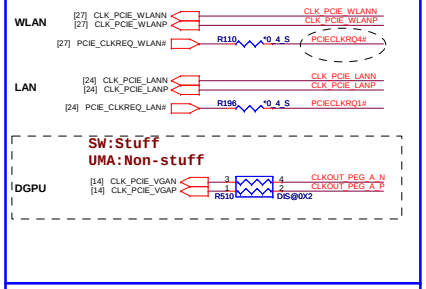
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



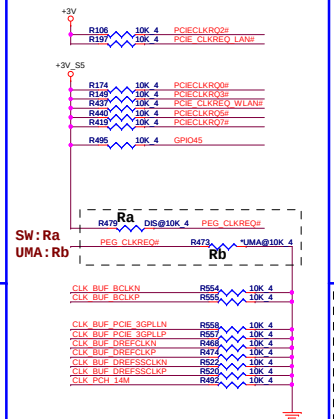
PCI/USBOC# Pull-up(CLG)



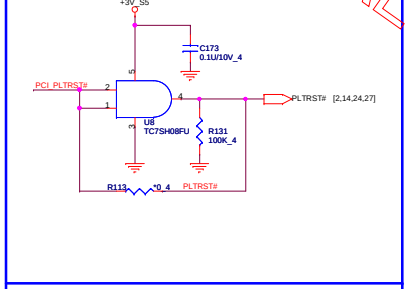
PCIE CLOCK



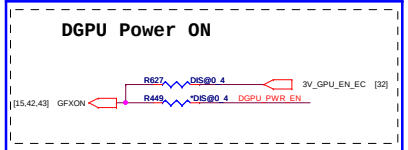
CLK_REQ/Strap Pin(CLG)



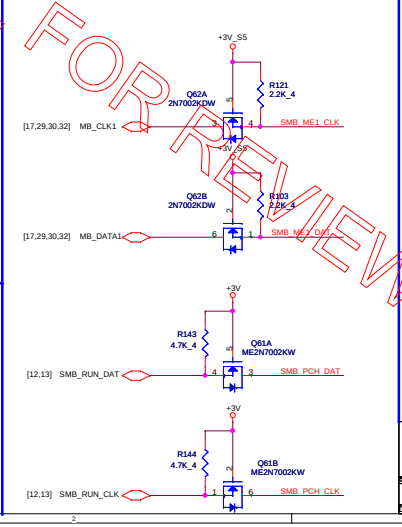
PLTRST#(CLG)



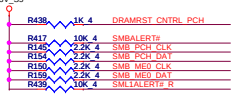
DGPU Power ON



SMBus(CLK)



SMBus/Pull-up(CLG)



MPC Switch Control	
MPC_PWR_CTRL#	LOw = MPC ON High = MPC OFF (Default)

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Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

[2,6,7,8,10,27,31,34] +3V_S5
[6,7,8,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V

U13F

GPIO

S_GPIO	R507 100_4	T7	BMBUSY# / GPIO0	+3V	+3V	TACH4 / GPIO68	C40 FB_CLAMP_PCH
[32] EC_EXT_SMI#	EC_EXT_SMI#	A42	TACH1 / GPIO1	+3V	+3V	TACH5 / GPIO69	B41 R122 1.5K/F_4
	BOARD_ID1	H36	TACH2 / GPIO6	+3V	+3V	TACH6 / GPIO70	C41 GPU_EVENT_PCH#
[32] EC_EXT_SCI#	EC_EXT_SCI#	E38	TACH3 / GPIO7	+3V	+3V	TACH7 / GPIO71	A40 PCB_LAYER_ID
TP8	ICC_EN#	C10	GPIO8	+3V_S5			
[27] LAN_DISABLE#	LAN_DISABLE#	C4	LAN_PHY_PWR_CTRL / GPIO12	+3V_S5			
	HOST_ALERT#1_R	G2	GPIO15	+3V_S5			
	BOARD_ID2	U2	SATA4GP / GPIO16	+3V			
[14,43] GFXPG	R100 *0_4_S GFXPG_R	D40	TACH0 / GPIO17	+3V			
	BIOS_REC	T5	SCLOCK / GPIO22	+3V			
	SYSTEM_ID1	E8	GPIO24 / MEM_LED	+3V_S5			
	GPIO27	E16	GPIO27	DSW			
[7] PLL_ODVR_EN	R494 *0_4_S PLL_ODVR_EN_R	P8	GPIO28	+3V_S5			
	SYSTEM_ID0	K1	STP_PCI# / GPIO34	+3V			
[30] BT_ON#	BT_ON#	K4	GPIO35	+3V			
[30] CCD_ON#	CCD_ON#	V8	SATA2GP / GPIO36	+3V			
	FDI_OVRVLTG	M5	SATA3GP / GPIO37	+3V			
	MFG_MODE	N2	SLOAD / GPIO38	+3V			
	DGPU_PRSNT#	M3	SDATAOUT0 / GPIO39	+3V			
	TEST_SET_UP	V13	SDATAOUT1 / GPIO48	+3V			
[29,32] TEMP_ALERT#		V3	SATA5GP / GPIO49	+3V			
	SV_DET	D6	GPIO57	+3V_S5			

CPU/MISC

A20GATE	P4	EC_A20GATE [32]
PECI	AU16 TP58	
RCIN#	P5 EC_RCIN#	EC_RCIN# [32]
PROCPWRGD	AY11	H_PWRGOOD [2]
THRMTRIP#	AY10 PCH_THRMTRIP# R539 390_4	PM_THRMTRIP# [2]
INIT3_3V#	T14	
DF_TVS	AY1	DF_TVS [7]
TS_VSS1	AH8	
TS_VSS2	AK11	
TS_VSS3	AH10	
TS_VSS4	AK10	
NC_1	P37	

NCTF

A4	VSS_NCTF_1	BG2	VSS_NCTF_15
A44	VSS_NCTF_2	BG48	VSS_NCTF_16
A45	VSS_NCTF_3	BH3	VSS_NCTF_17
A46	VSS_NCTF_4	BH47	VSS_NCTF_18
A5	VSS_NCTF_5	BJ4	VSS_NCTF_19
A6	VSS_NCTF_6	BJ44	VSS_NCTF_20
B3	VSS_NCTF_7	BJ45	VSS_NCTF_21
B47	VSS_NCTF_8	BJ46	VSS_NCTF_22
BD1	VSS_NCTF_9	BJ5	VSS_NCTF_23
BD49	VSS_NCTF_10	BJ6	VSS_NCTF_24
BE1	VSS_NCTF_11	C2	VSS_NCTF_25
BE49	VSS_NCTF_12	C48	VSS_NCTF_26
BF1	VSS_NCTF_13	D1	VSS_NCTF_27
BF49	VSS_NCTF_14	D49	VSS_NCTF_28
		E1	VSS_NCTF_29
		E49	VSS_NCTF_30
		F1	VSS_NCTF_31
		F49	VSS_NCTF_32

CPT_PPT_Rev_0p5

NVidia N13P-GS

R25 10K/F_4
R118 *GS@0_4 FB_CLAMP [15]
R462 *GS@0_4 GPU_EVENT# [17]
R634 10K/F_4@GS@NC +3V

NVidia N13P-GS

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT			
SOVP			

Board ID use below GPIO:
BOARD_ID1
BOARD_ID2
BOARD_ID3

PCB_LAYER_ID:
0-->6 layer
1-->8 layer

System ID[0],ID[1]:
-->LZ1 [0,0]
-->LZ2 [0,1]
-->LZ3 [1,0]

R209 *10K_4 BOARD_ID2 R213 10K_4
R429 10K_4 BOARD_ID1 R430 *10K_4
R129 *10K_4 PCB_LAYER_ID R138 10K_4
R187 10K_4 SYSTEM_ID0 R175 *10K_4
R476 *10K_4 SYSTEM_ID1 R467 10K_4
R503 10K_4 BOARD_ID3 R443 *10K_4
BOARD_ID3 [7]

GPIO Pull-up/Pull-down(CLG)

LAN_DISABLE# R162 10K_4
EC_EXT_SMI# R130 10K_4
EC_EXT_SCI# R431 10K_4
EC_A20GATE R498 10K_4
EC_RCIN# R500 10K_4
TEMP_ALERT# R223 10K_4
BT_ON# R481 10K_4
GPIO27 R441 10K_4

SATA2GP/GPIO36	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal should not be pulled high when strap is sampled.

CCD_ON# R515 *200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

R491 100K_4 FDI_OVRVLTG R486 *1K/F_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

SGPIO

S_GPIO R508 10K_4 R505 *0_4

BIOS_REC R499 10K_4 R501 *0_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

SV_SET_UP
High = Strong (Default)

TEST_SET_UP R194 10K_4 R185 *0_4

HOST_ALERT#1_R R466 1K_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

MFG-TEST

MFG_MODE R199 10K_4 R202 *0_4

R456 *10K_4 SV_DET R458 100K_4

	SWITCHABLE	UMA
Stuff	R186	R195
No Stuff	R195	R186

R195 *UMA@10K_4 DGPU_PRSNT# R186 DIS@100K_4

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Cougar Point/Panther Point (POWER)

VccCORE =1.3 A(60mils)

VccIO =2.925 A(140mils)

VccADAC =1mA(8mils)

VccALVDS=1mA(8mils)

VccTX_LVDS=60mA(10mils)

VCCDMI = 42mA(10mils)

VCCCLKDMI = 20mA(8mils)

VCCPNAND = 190 mA(15mils)

VCCSPI = 20mA(8mils)

VCCVRM: 1.8V (Destop) 1.5V (Mobile)

VCCDSW3_3= 3mA

VccASW =1.01 A(60mils)

VCCSUS3_3 = 119mA(15mils)

VCCSUS3_3 = 119mA(15mils)

VCCPCORE = 28mA(10mils)

VCCVRM= 114mA(15mils)

VCCDIFFCLKN= 55mA(10mils)

VCCSSC= 95mA(10mils)

VCCME = 1.01A(60mils)

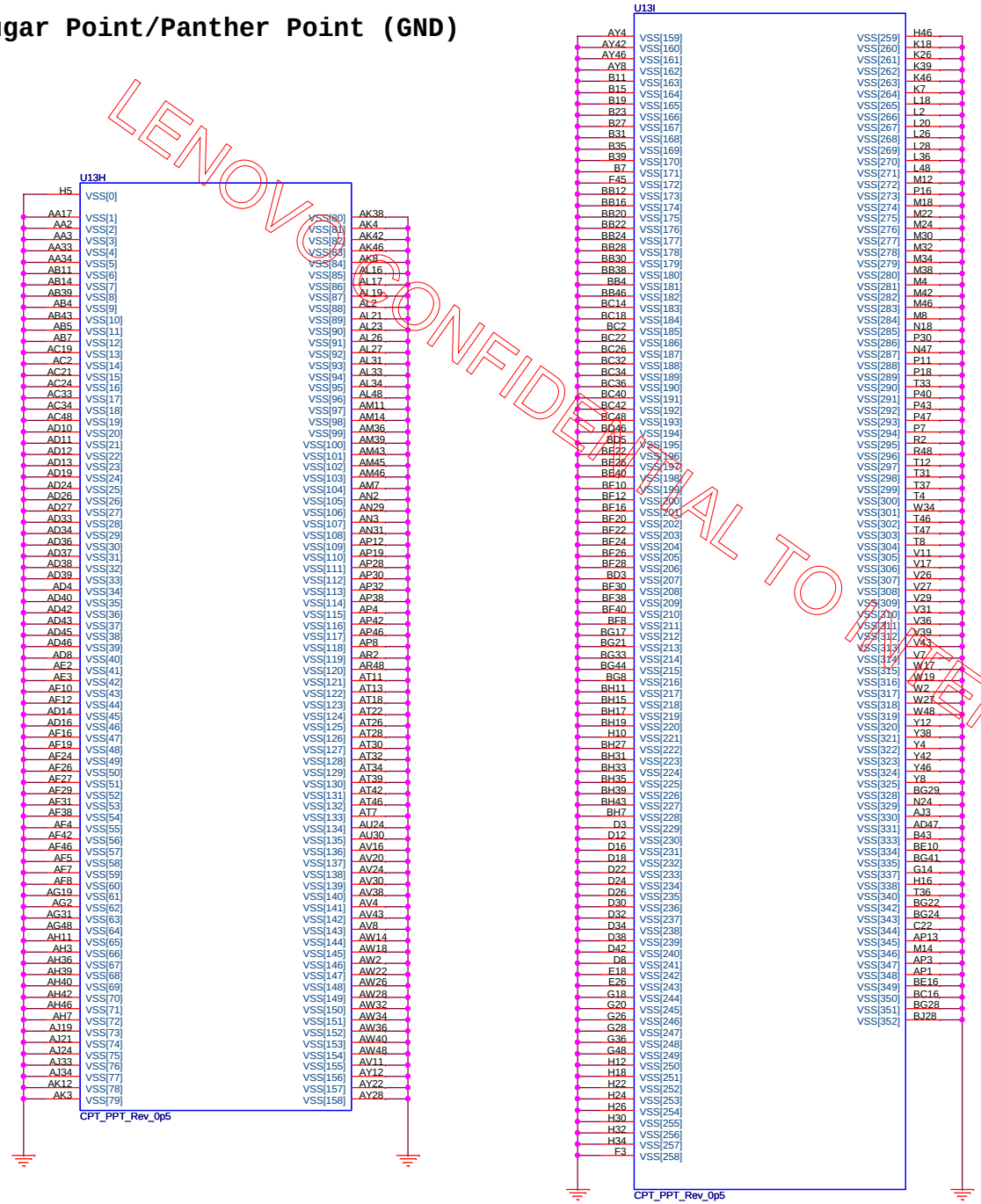
VCCSUSHDA= 10mA(8mils)

VCCRTC<1mA(8mils)

FOR DEEP S3

FOR DEEP S3

Cougar Point/Panther Point (GND)



PROJECT : LZ2A

Quanta Computer Inc.

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	Panther Point 6/6	1A

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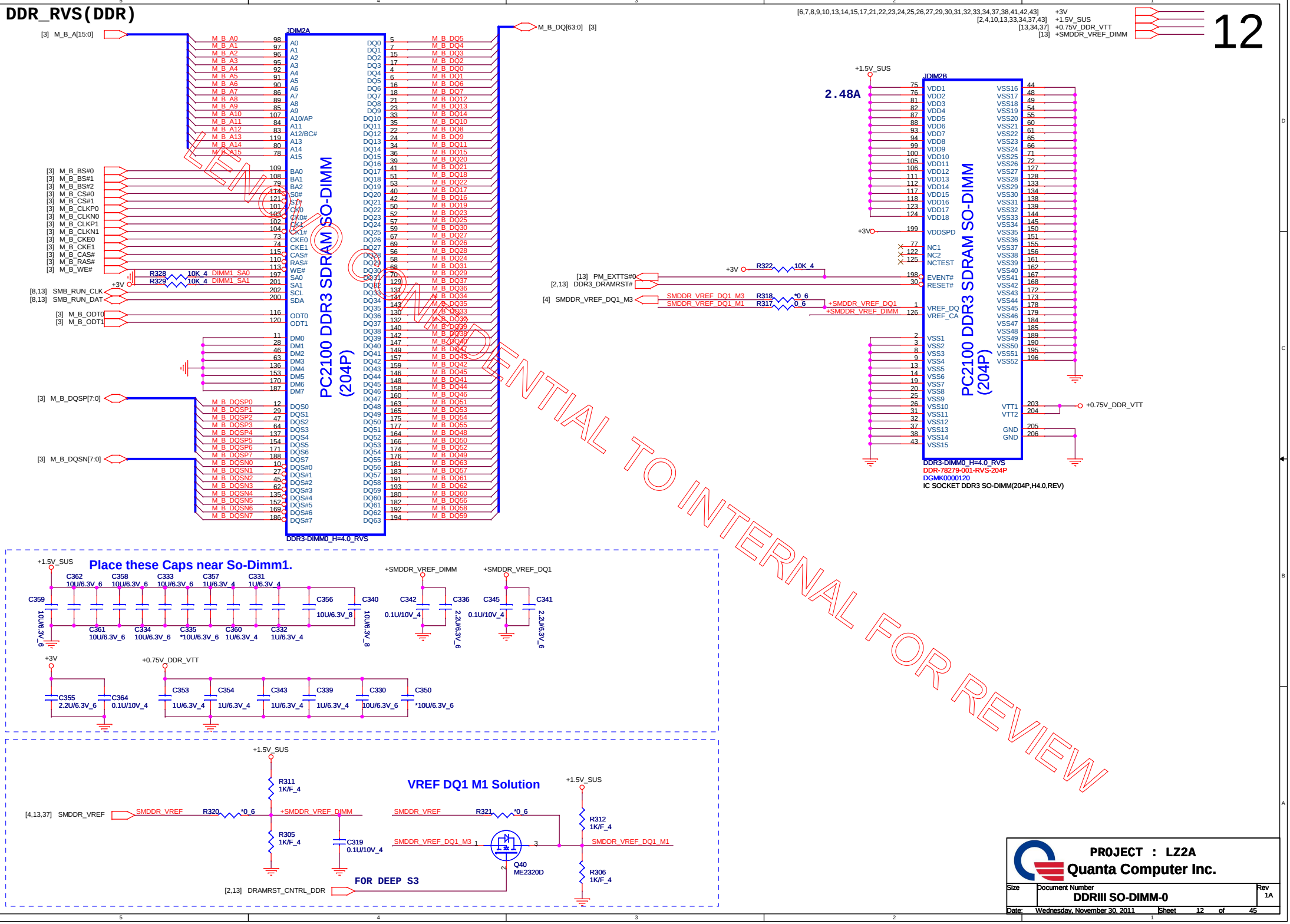
DDR_RVS(DDR)



DDR_RVS(DDR)

[6,7,8,9,10,12,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[2,4,10,12,33,34,37,43] +1.5V_SUS
[12,34,37] +0.75V_DDR_VTT
[12] +SMDDR_VREF_DIMM

JDIM1A — PC2100 DDR3 SDRAM SO-DIMM (204P)

[3] M_A_A[15:0]
M_A_A0 98, M_A_A1 97, M_A_A2 96, M_A_A3 95, M_A_A4 92, M_A_A5 91, M_A_A6 90, M_A_A7 86, M_A_A8 89, M_A_A9 85, M_A_A10 107, M_A_A11 84, M_A_A12 83, M_A_A13 119, M_A_A14 80, M_A_A15 78
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12/BC#, A13, A14, A15

[3] M_A_BS#0 109 BA0
[3] M_A_BS#1 108 BA1
[3] M_A_BS#2 79 BA2
[3] M_A_CS#0 114 S0#
[3] M_A_CS#1 121 S1#
[3] M_A_CLKP0 101 CK0
[3] M_A_CLKN0 103 CK0#
[3] M_A_CLKP1 102 CK1
[3] M_A_CLKN1 104 CK1#
[3] M_A_CKE0 73 CKE0
[3] M_A_CKE1 74 CKE1
[3] M_A_CAS# 115 CAS#
[3] M_A_RAS# 110 RAS#
[3] M_A_WE# 113 WE#

R308 10K_4 DIMM0_SA0 197 SA0
R307 10K_4 DIMM0_SA1 201 SA1
[8,12] SMB_RUN_CLK 202 SCL
[8,12] SMB_RUN_DAT 200 SDA

[3] M_A_ODT0 116 ODT0
[3] M_A_ODT1 120 ODT1

11, 28, 46, 63, 136, 153, 170, 187 DM0, DM1, DM2, DM3, DM4, DM5, DM6, DM7

[3] M_A_DQSP[7:0]
M_A_DQSP0 12, M_A_DQSP1 29, M_A_DQSP2 47, M_A_DQSP3 64, M_A_DQSP4 137, M_A_DQSP5 154, M_A_DQSP6 171, M_A_DQSP7 188
DQS0, DQS1, DQS2, DQS3, DQS4, DQS5, DQS6, DQS7

[3] M_A_DQSN[7:0]
M_A_DQSN0 10, M_A_DQSN1 27, M_A_DQSN2 45, M_A_DQSN3 62, M_A_DQSN4 135, M_A_DQSN5 152, M_A_DQSN6 169, M_A_DQSN7 186
DQS#0, DQS#1, DQS#2, DQS#3, DQS#4, DQS#5, DQS#6, DQS#7

M_A_DQ[63:0] [3]
DQ0 5 M_A_DQ4, DQ1 7 M_A_DQ5, DQ2 15 M_A_DQ6, DQ3 17 M_A_DQ7, DQ4 4 M_A_DQ0, DQ5 6 M_A_DQ1, DQ6 16 M_A_DQ3, DQ7 18 M_A_DQ2, DQ8 21 M_A_DQ13, DQ9 23 M_A_DQ9, DQ10 33 M_A_DQ15, DQ11 35 M_A_DQ14, DQ12 22 M_A_DQ12, DQ13 24 M_A_DQ8, DQ14 34 M_A_DQ10, DQ15 36 M_A_DQ11, DQ16 39 M_A_DQ22, DQ17 41 M_A_DQ19, DQ18 51 M_A_DQ16, DQ19 53 M_A_DQ21, DQ20 40 M_A_DQ18, DQ21 42 M_A_DQ23, DQ22 50 M_A_DQ17, DQ23 52 M_A_DQ20, DQ24 57 M_A_DQ31, DQ25 59 M_A_DQ27, DQ26 67 M_A_DQ30, DQ27 69 M_A_DQ29, DQ28 56 M_A_DQ24, DQ29 58 M_A_DQ26, DQ30 68 M_A_DQ25, DQ31 70 M_A_DQ28, DQ32 128 M_A_DQ37, DQ33 131 M_A_DQ33, DQ34 141 M_A_DQ38, DQ35 143 M_A_DQ34, DQ36 130 M_A_DQ32, DQ37 132 M_A_DQ36, DQ38 140 M_A_DQ35, DQ39 142 M_A_DQ39, DQ40 147 M_A_DQ44, DQ41 149 M_A_DQ47, DQ42 157 M_A_DQ46, DQ43 159 M_A_DQ45, DQ44 146 M_A_DQ41, DQ45 148 M_A_DQ40, DQ46 158 M_A_DQ42, DQ47 160 M_A_DQ43, DQ48 163 M_A_DQ54, DQ49 165 M_A_DQ55, DQ50 175 M_A_DQ51, DQ51 177 M_A_DQ50, DQ52 164 M_A_DQ48, DQ53 166 M_A_DQ49, DQ54 174 M_A_DQ53, DQ55 176 M_A_DQ52, DQ56 181 M_A_DQ61, DQ57 183 M_A_DQ58, DQ58 191 M_A_DQ57, DQ59 193 M_A_DQ63, DQ60 180 M_A_DQ56, DQ61 182 M_A_DQ60, DQ62 192 M_A_DQ59, DQ63 194 M_A_DQ62

DDR3-DIMM1_H=8.0_RVS

JDIM1B — PC2100 DDR3 SDRAM SO-DIMM (204P)

2.48A

+1.5V_SUS
VDD1 75, VDD2 76, VDD3 81, VDD4 82, VDD5 87, VDD6 88, VDD7 93, VDD8 94, VDD9 99, VDD10 100, VDD11 105, VDD12 106, VDD13 111, VDD14 112, VDD15 117, VDD16 118, VDD17 123, VDD18 124

+3V 199 VDDSPD

NC1 77, NC2 122, NCTEST 125

+3V R286 10K_4
[12] PM_EXTTS#0 → EVENT# 198
[2,12] DDR3_DRAMRST# → RESET# 30

SMDDR_VREF_DQ0_M1 R303 0_6 +SMDDR_VREF_DQ0
SMDDR_VREF_DQ0_M3 R314 *0_6 +SMDDR_VREF_DIMM
[4] SMDDR_VREF_DQ0_M3
VREF_DQ 1, VREF_CA 126

VSS1 2, VSS2 3, VSS3 8, VSS4 9, VSS5 13, VSS6 14, VSS7 19, VSS8 20, VSS9 25, VSS10 26, VSS11 31, VSS12 32, VSS13 37, VSS14 38, VSS15 43

VSS16 44, VSS17 48, VSS18 49, VSS19 54, VSS20 55, VSS21 60, VSS22 61, VSS23 65, VSS24 66, VSS25 71, VSS26 72, VSS27 127, VSS28 128, VSS29 133, VSS30 134, VSS31 138, VSS32 139, VSS33 144, VSS34 145, VSS35 150, VSS36 151, VSS37 155, VSS38 156, VSS39 161, VSS40 162, VSS41 167, VSS42 168, VSS43 172, VSS44 173, VSS45 178, VSS46 179, VSS47 184, VSS48 185, VSS49 189, VSS50 190, VSS51 195, VSS52 196

VTT1 203 +0.75V_DDR_VTT
VTT2 204
GND 205
GND 206

DDR3-DIMM1_H=8.0_RVS

Place these Caps near So-Dimm0.

+1.5V_SUS
C303 10U/6.3V_6, C324 10U/6.3V_6, C306 10U/6.3V_6, C301 1U/6.3V_4, C326 1U/6.3V_4
C300 10U/6.3V_6
C307 10U/6.3V_6, C325 10U/6.3V_6, C322 *10U/6.3V_6, C305 1U/6.3V_4, C327 1U/6.3V_4
C296 *330U/2V/ESR9_7343
C297 10U/6.3V_8, C323 10U/6.3V_8
+SMDDR_VREF_DIMM, +SMDDR_VREF_DQ0
C299 0.1U/10V_4, C304 2.2U/6.3V_6
C317 0.1U/10V_4, C318 2.2U/6.3V_6
+3V
C316 2.2U/6.3V_6, C321 0.1U/10V_4
+0.75V_DDR_VTT
C298 1U/6.3V_4, C302 1U/6.3V_4, C328 1U/6.3V_4, C320 1U/6.3V_4, C308 10U/6.3V_6, C311 *10U/6.3V_6

VREF DQ0 M3 Solution

+1.5V_SUS
R325 1K/F_4
[4,12,37] SMDDR_VREF
R323 *0_6
SMDDR_VREF_DQ0_M1
R324 1K/F_4
SMDDR_VREF_DQ0_M3 1 3 2
Q41 ME2320D
FOR DEEP S3
[2,12] DRAMRST_CNTRL_DDR

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	DDRIII SO-DIMM-1	1A

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[15,16,33,43] +1.05V_GFX_PCIE
[16,17,18,43] +3V_GPU
[15,19,20,33,43] +1.5V_GPU
[6,7,8,9,10,12,13,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[18,33,42] GFX_CORE

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >3.45A

U30A

N13P-GS

To be placed no further from the GPU than bewteen the PS and GPU

PLACE UNDER BGA | PLACE NEAR BALLS

+1.05V_GFX_PCIE

C94 DIS@22U/6.3V_8 | C149 DIS@22U/6.3V_8 | C108 DIS@10U/6.3V_8 | C150 DIS@10U/6.3V_8 | C105 DIS@4.7U/6.3V_6 | C116 DIS@1U/6.3V_4 | C117 DIS@1U/6.3V_4

AG19 AG21 AG22 AG24 AH21 AH25 PEX_IOVDD

AG13 AG15 AG16 AG18 AG25 AH15 AH18 AH26 AH27 AJ27 AK27 AL27 AM28 AN28 PEX_IOVDDQ

C106 DIS@22U/6.3V_8 | C130 DIS@22U/6.3V_8 | C107 DIS@10U/6.3V_8 | C138 DIS@10U/6.3V_8 | C104 DIS@4.7U/6.3V_6 | C129 DIS@1U/6.3V_4 | C113 DIS@1U/6.3V_4

CAP CLOSE TO BGA

12~16 mils width 210mA

+3V_GPU PLACE NEAR BGA

+PEX_SVDD_3V3 R86 *GS@0_4 AH12 PEX_PLL_HVDD

C467 DIS@0.1U/10V_4 | C77 DIS@4.7U/6.3V_6 | C118 DIS@4.7U/6.3V_6 AG12 PEX_SVDD_3V3

0ohm (R86)	
N13P-GS (GK107)	Stuff
N13P-GL (GF108) N13M-GE1 (GF119)	unstuff

1/19 PCI_EXPRESS

[42] GPU_VCCSENSE L4 VDD_SENSE

[42] GPU_VSSSENSE L5 GND_SENSE

16 mils width for 110mA

P8 3V3AUX_NC

R90 *DIS@200/F_4 PEX_TSTCLK AJ26 PEX_TSTCLK_OUT
PEX_TSTCLK# AK26 PEX_TSTCLK_OUT*

150mA

+1.05V_GFX_PCIE L5 DIS@0_6 PLACE UNDER GPU

C112 DIS@0.1U/10V_4 | C127 DIS@1U/6.3V_4 | C129 DIS@1U/6.3V_4 | C136 DIS@4.7U/6.3V_6 PLACE NEAR BGA

+PEX_PLLVDD AG26 PEX_PLLVDD

TESTMODE AK11 TESTMODE

R94 DIS@10K_4

PEX_TERMP AP29 PEX_TERMP

R98 DIS@2.49K/F_4

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PEX_WAKE AJ11

PEX_RST AJ12 GPU_RST#

PEX_CLKREQ AK12 R405 DIS@10K_4 +3V_GPU
PEX_CLKREQ#

PEX_REFCLK AL13 CLK_PCIE_VGAP [8]
PEX_REFCLK AK13 CLK_PCIE_VGAN [8]

PEX_TX15	AK14	PEG_RXP15_C	C143	DIS@0.1U/10V_4	PEG_RXP15 [2]
PEX_TX15	AJ14	PEG_RXN15_C	C141	DIS@0.1U/10V_4	PEG_RXN15 [2]
PEX_RX15	AN12				PEG_TXP15 [2]
PEX_RX15	AM12				PEG_TXN15 [2]
PEX_TX14	AH14	PEG_RXP14_C	C195	DIS@0.1U/10V_4	PEG_RXP14 [2]
PEX_TX14	AG14	PEG_RXN14_C	C196	DIS@0.1U/10V_4	PEG_RXN14 [2]
PEX_RX14	AN14				PEG_TXP14 [2]
PEX_RX14	AM14				PEG_TXN14 [2]
PEX_TX13	AK15	PEG_RXP13_C	C166	DIS@0.1U/10V_4	PEG_RXP13 [2]
PEX_TX13	AJ15	PEG_RXN13_C	C167	DIS@0.1U/10V_4	PEG_RXN13 [2]
PEX_RX13	AP14				PEG_TXP13 [2]
PEX_RX13	AP15				PEG_TXN13 [2]
PEX_TX12	AL16	PEG_RXP12_C	C186	DIS@0.1U/10V_4	PEG_RXP12 [2]
PEX_TX12	AK16	PEG_RXN12_C	C187	DIS@0.1U/10V_4	PEG_RXN12 [2]
PEX_RX12	AN15				PEG_TXP12 [2]
PEX_RX12	AM15				PEG_TXN12 [2]
PEX_TX11	AK17	PEG_RXP11_C	C152	DIS@0.1U/10V_4	PEG_RXP11 [2]
PEX_TX11	AJ17	PEG_RXN11_C	C153	DIS@0.1U/10V_4	PEG_RXN11 [2]
PEX_RX11	AN17				PEG_TXP11 [2]
PEX_RX11	AM17				PEG_TXN11 [2]
PEX_TX10	AH17	PEG_RXP10_C	C164	DIS@0.1U/10V_4	PEG_RXP10 [2]
PEX_TX10	AG17	PEG_RXN10_C	C165	DIS@0.1U/10V_4	PEG_RXN10 [2]
PEX_RX10	AP17				PEG_TXP10 [2]
PEX_RX10	AP18				PEG_TXN10 [2]
PEX_TX9	AK18	PEG_RXP9_C	C184	DIS@0.1U/10V_4	PEG_RXP9 [2]
PEX_TX9	AJ18	PEG_RXN9_C	C185	DIS@0.1U/10V_4	PEG_RXN9 [2]
PEX_RX9	AN18				PEG_TXP9 [2]
PEX_RX9	AM18				PEG_TXN9 [2]
PEX_TX8	AL19	PEG_RXP8_C	C163	DIS@0.1U/10V_4	PEG_RXP8 [2]
PEX_TX8	AK19	PEG_RXN8_C	C162	DIS@0.1U/10V_4	PEG_RXN8 [2]
PEX_RX8	AN20				PEG_TXP8 [2]
PEX_RX8	AM20				PEG_TXN8 [2]
PEX_TX7	AK20	PEG_RXP7_C	C183	DIS@0.1U/10V_4	PEG_RXP7 [2]
PEX_TX7	AJ20	PEG_RXN7_C	C182	DIS@0.1U/10V_4	PEG_RXN7 [2]
PEX_RX7	AP20				PEG_TXP7 [2]
PEX_RX7	AP21				PEG_TXN7 [2]
PEX_TX6	AH20	PEG_RXP6_C	C161	DIS@0.1U/10V_4	PEG_RXP6 [2]
PEX_TX6	AG20	PEG_RXN6_C	C160	DIS@0.1U/10V_4	PEG_RXN6 [2]
PEX_RX6	AN21				PEG_TXP6 [2]
PEX_RX6	AM21				PEG_TXN6 [2]
PEX_TX5	AK21	PEG_RXP5_C	C180	DIS@0.1U/10V_4	PEG_RXP5 [2]
PEX_TX5	AJ21	PEG_RXN5_C	C181	DIS@0.1U/10V_4	PEG_RXN5 [2]
PEX_RX5	AN23				PEG_TXP5 [2]
PEX_RX5	AM23				PEG_TXN5 [2]
PEX_TX4	AL22	PEG_RXP4_C	C158	DIS@0.1U/10V_4	PEG_RXP4 [2]
PEX_TX4	AK22	PEG_RXN4_C	C159	DIS@0.1U/10V_4	PEG_RXN4 [2]
PEX_RX4	AP23				PEG_TXP4 [2]
PEX_RX4	AP24				PEG_TXN4 [2]
PEX_TX3	AK23	PEG_RXP3_C	C157	DIS@0.1U/10V_4	PEG_RXP3 [2]
PEX_TX3	AJ23	PEG_RXN3_C	C156	DIS@0.1U/10V_4	PEG_RXN3 [2]
PEX_RX3	AN24				PEG_TXP3 [2]
PEX_RX3	AM24				PEG_TXN3 [2]
PEX_TX2	AH23	PEG_RXP2_C	C179	DIS@0.1U/10V_4	PEG_RXP2 [2]
PEX_TX2	AG23	PEG_RXN2_C	C178	DIS@0.1U/10V_4	PEG_RXN2 [2]
PEX_RX2	AN26				PEG_TXP2 [2]
PEX_RX2	AM26				PEG_TXN2 [2]
PEX_TX1	AK24	PEG_RXP1_C	C155	DIS@0.1U/10V_4	PEG_RXP1 [2]
PEX_TX1	AJ24	PEG_RXN1_C	C154	DIS@0.1U/10V_4	PEG_RXN1 [2]
PEX_RX1	AP26				PEG_TXP1 [2]
PEX_RX1	AP27				PEG_TXN1 [2]
PEX_TX0	AL25	PEG_RXP0_C	C176	DIS@0.1U/10V_4	PEG_RXP0 [2]
PEX_TX0	AK25	PEG_RXN0_C	C177	DIS@0.1U/10V_4	PEG_RXN0 [2]
PEX_RX0	AN27				PEG_TXP0 [2]
PEX_RX0	AM27				PEG_TXN0 [2]

PEG Capacitance	
N13P-GS (GK107)	CH4222K9B04: CAP CHIP 0.22U 10V(+-10%,X5R,0402)
N13P-GL (GF108) N13M-GE1 (GF119)	CH41002KB93: CAP CHIP 0.1U 10V(+-10%,X5R,0402)

GPU RST#(CLG)

+3V C510 DIS@0.1U/10V_4

[2,8,24,27] PLTRST#
[8] DGPU_HOLD_RST#
GPU_RST#
U9 DIS@TC7SH08FU

All GPU power rails must ramp up after VDD33. The following conditions must be met:

- tNVVDD > 0
- tFBVDDQ > 0
- tPEX_VDD > 0
- tIFPx_IOVDD ≥ 0
- tIFPy_IOVDD ≥ 0
- The ramp time for any rail must be more than 40 us.

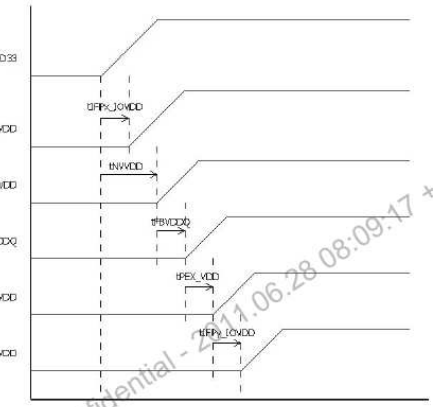

Figure 17. Recommended Power On Sequencing Order

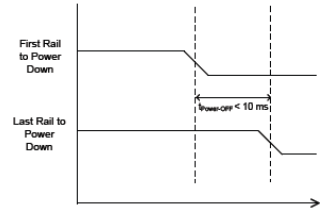

Figure 18. Recommended Power Off Sequencing Order

For power-down sequency

+3V_GPU +1.5V_GPU +3V_GPU GFX_CORE +3V_GPU +1.05V_GFX_PCIE

D1 DIS@RB500V-40 | D2 DIS@RB500V-40 | D25 DIS@RB500V-40

PEG CLK detect

GFXPG [9,43]

[8] PEG_CLKREQ# 3 Q15 DIS@ME2N7002E 1 PEX_CLKREQ#

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Quanta Computer Inc.

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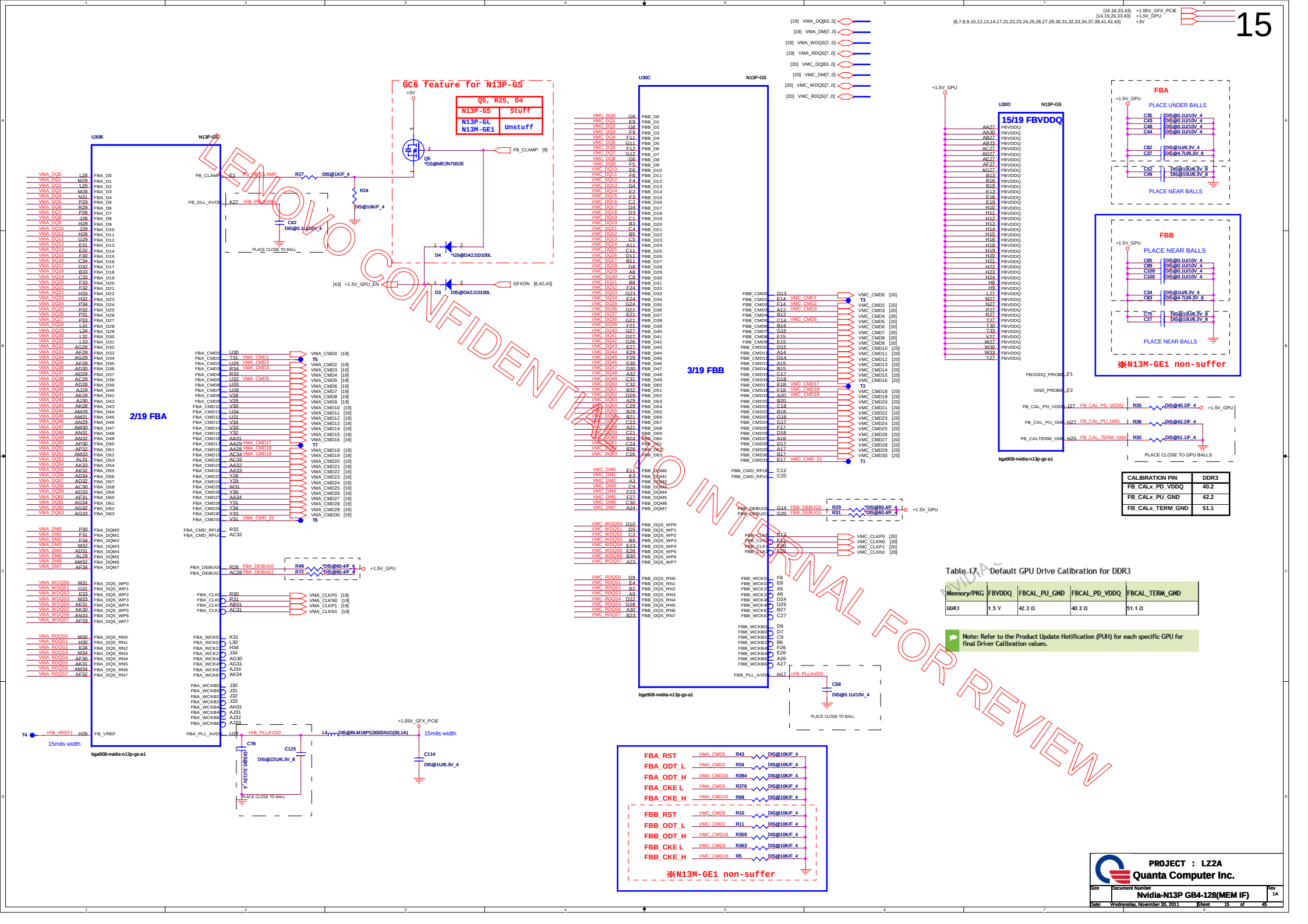
GC6 feature for N13P-GS
Q5, R25, D4
N13P-GS
Stuff
N13P-GL
N13M-GE1
Unstuff
2/19 FBA
3/19 FBB
15/19 FBVDDQ
FBA
PLACE UNDER BALLS
PLACE NEAR BALLS
FBB
※N13M-GE1 non-suffer
CALIBRATION PIN
DDR3
FB_CALx_PD_VDDQ
40.2
FB_CALx_PU_GND
42.2
FB_CALx_TERM_GND
51.1
Table 17. Default GPU Drive Calibration for DDR3
Memory/PKG
FBVDDQ
FBCAL_PU_GND
FBCAL_PD_VDDQ
FBCAL_TERM_GND
DDR3
1.5 V
42.2 Ω
40.2 Ω
51.1 Ω
Note: Refer to the Product Update Notification (PUN) for each specific GPU for final Driver Calibration values.
FBA_RST
FBA_ODT_L
FBA_ODT_H
FBA_CKE L
FBA_CKE_H
FBB_RST
FBB_ODT_L
FBB_ODT_H
FBB_CKE L
FBB_CKE_H
※N13M-GE1 non-suffer
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LENOVO CONFIDENTIAL B
INTERNAL FOR REVIEW

[14,15,33,43] +1.05V_GFX_PCIE

50 mA

160 mA+160 mA

200 mA

60mA 12~16 mil

90mA 12~16 mil

U30J N13P-GS — 6/19 IFPAB

ALL PINS NC FOR GF117

IFPAB

AJ8 IFPAB_RSET

+IFPAB_PLLVDD AH8 IFPAB_PLLVDD — R91 DIS@10K/F_4

+IFPAB_IOVDD AG8 IFPA_IOVDD, AG9 IFPB_IOVDD — R83 DIS@10K/F_4

IFPA_TXC AN6 / AM6

IFPA_TXD0 AN3 / AP3

IFPA_TXD1 AM5 / AN5

IFPA_TXD2 AK6 / AL6

IFPA_TXD3 AH6 / AJ6

IFPB_TXC AH9 / AJ9

IFPB_TXD0 AP5 / AP6

IFPB_TXD1 AL7 / AM7

IFPB_TXD2 AM8 / AN8

IFPB_TXD3 AL8 / AK8

GPIO14 N4

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U30K N13P-GS — 7/19 IFPC

ALL PINS NC FOR GF117

IFPC

AF8 IFPC_RSET

+IFPCD_PLLVDD AF7 IFPC_PLLVDD — R79 DIS@10K/F_4

+IFPCD_IOVDD AF6 IFPC_IOVDD — R84 DIS@10K/F_4

DVI/HDMI: I2CW_SDA, I2CW_SCL, TXC, TXD0, TXD1, TXD2

DP: IFPC_AUX AG2 / AG3; IFPC_L3 AG4 / AG5; IFPC_L2 AH4 / AH3; IFPC_L1 AJ2 / AJ3; IFPC_L0 AJ1 / AK1

GPIO15 P2

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U30L N13P-GS — 8/19 IFPD

ALL PINS NC FOR GF117

IFPD

AN2 IFPD_RSET

+IFPCD_PLLVDD AG7 IFPD_PLLVDD

+IFPCD_IOVDD AG6 IFPD_IOVDD

DVI/HDMI: I2CX_SDA, I2CX_SCL, TXC, TXD0, TXD1, TXD2

DP: IFPD_AUX AK2 / AK3; IFPD_L3 AK5 / AK4; IFPD_L2 AL4 / AL3; IFPD_L1 AM4 / AM3; IFPD_L0 AM2 / AM1

GPIO17 M6

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U30M N13P-GS — 9/19 IFPEF

ALL PINS NC FOR GF117

R60 DIS@10K_4 +IFPEF_PLLVDD — AB8 IFPEF_PLLVDD

AD6 IFPEF_RSET

R61 DIS@10K_4 +IFPEF_IOVDD — AC7 IFPE_IOVDD, AC8 IFPF_IOVDD

IFPE

DVI-DL / DVI-SL/HDMI: I2CY_SDA, I2CY_SCL, TXC, TXD0, TXD1, TXD2, HPD_E

DP: IFPE_AUX AB4 / AB3; IFPE_L3 AC5 / AC4; IFPE_L2 AC3 / AC2; IFPE_L1 AC1 / AD1; IFPE_L0 AD3 / AD2

GPIO18 R1

IFPF

DVI-SL/HDMI: I2CZ_SDA, I2CZ_SCL, TXC, TXD3, TXD0, TXD4, TXD1, TXD5, TXD2, HPD_F

DP: IFPF_AUX AF2 / AF3; IFPF_L3 AF1 / AG1; IFPF_L2 AD5 / AD4; IFPF_L1 AF5 / AF4; IFPF_L0 AE4 / AE3

GPIO19 P3

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U30N N13P-GS — 4/19 DACA

GF108/GKx / GF117: DACA_VDD AG10 (NC), DACA_VREF AP9 (TSEN_VREF), DACA_RSET AP8 (NC)

GF117 / GF108/GKx: I2CA_SCL R4, I2CA_SDA R5, DACA_HSYNC AM9, DACA_VSYNC AN9, DACA_RED AK9, DACA_GREEN AL10, DACA_BLUE AL9

R78 DIS@10K_4 — TP29, TP31

EV_CRTDCLK — R630 DIS@2.2K_4 — +3V_GPU

EV_CRTDDAT — R631 DIS@2.2K_4 — +3V_GPU

TP6, TP30, TP4, TP3, TP5

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U30O N13P-GS — 12/19 XTAL_PLL

+1.05V_GFX_PCIE — L2 DIS@BLM18PG300SN1D(30,1A) — C122 DIS@22U/6.3V_8 — C96 DIS@0.1U/10V_4 — PLACE CLOSE TO BGA

+1.05V_GFX_PCIE — L3 DIS@HCB1608KF(180,1.5A)_6 — +NV_PLLVDD — PLACE UNDER BGA — +PLLVDD

AD8 PLLVDD, AE8 SP_PLLVDD, AD7 VID_PLLVDD

GF108/GKx / GF117

C126 DIS@1U/6.3V_4

C111 DIS@22U/6.3V_8, C101 DIS@4.7U/6.3V_6

C98 DIS@0.1U/10V_4, C97 DIS@0.1U/10V_4, C99 DIS@0.1U/10V_4

XTAL_SSIN H1 — R33 DIS@10K_4 — H3

XTALSSIN, XTALIN

XTALOUTBUFF J4 BXTALOUT — R38 DIS@10K_4

XTALOUT H2

XTALI_27M — Y1 DIS@27MHZ — XTALO_27M

C39 DIS@27P/50V_4, C41 DIS@33P/50V/NPO_4

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PROJECT : LZ2A

Quanta Computer Inc.

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	Nvidia-N13P GB4-128(Display)	1A

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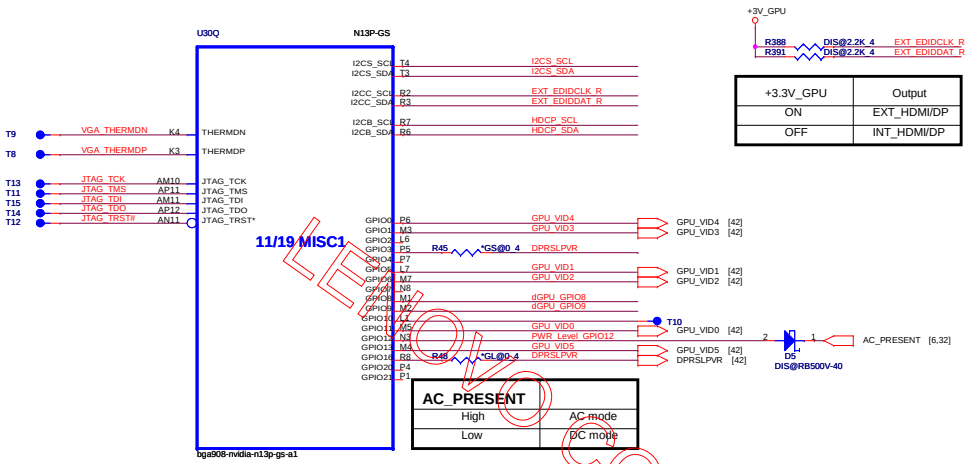
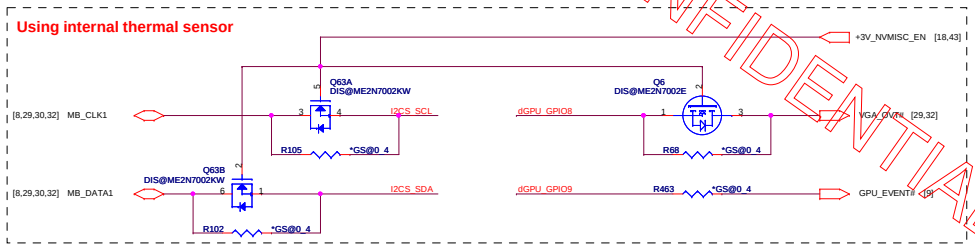


AC_PRESENT	
High	AC mode
Low	DC mode

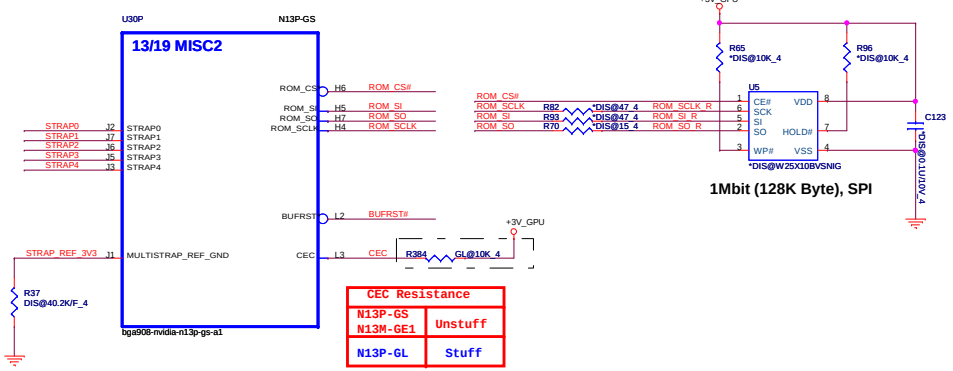
+3.3V_GPU	Output
ON	EXT_HDMI/DP
OFF	INT_HDMI/DP



	Q6,Q63, R81,R104	R68,R102, R105,R463
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

GPU	Signal/Rail	Stuffing Option
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor



CEC Resistance	
N13P-GS N13M-GE1	Unstuff
N13P-GL	Stuff

Table 2. GB4-128 Ballout Compatibility

Ball Number	N13P-PES/-GL/-NS1 Signal Names	N13M-GE1 Signal Names	N13P-GV / N13M-GS Signal Names	N13P-GT/-GS/-LP and N14P-Q1/-Q3 Signal Names	Comment
L3	CEC	NC	NC	NC	Place a 10k pull-up to 3V3 on N13P-PES/-GL/-NS1.

[14,16,18,43] +3V_GPU
[6,7,8,9,10,12,13,14,15,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[18] +3V_NVMISC

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	XXXX

Resistance	Quanta PN	DESCRIPTION
4.99K/F_4	CS24992FB26	RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4	CS31002FB26	RES CHIP 10K 1/16W +1% (0402)
15K/F_4	CS31502FB24	RES CHIP 15K 1/16W +1% (0402)
20K/F_4	CS32002FB29	RES CHIP 20K 1/16W +-1%(0402)
24.9K/F_4	CS32492FB16	RES CHIP 24.9K 1/16W +-1%(0402)
30K/F_4	CS33002FB13	RES CHIP 30K 1/16W +-1%(0402)]
34.8K/F_4	CS33482FB22	RES CHIP 34.8K 1/16W +-1%(0402)
45.3K/F_4	CS34532FB18	RES CHIP 45.3K 1/16W +-1% (0402)

Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

VRAM Configuration Table

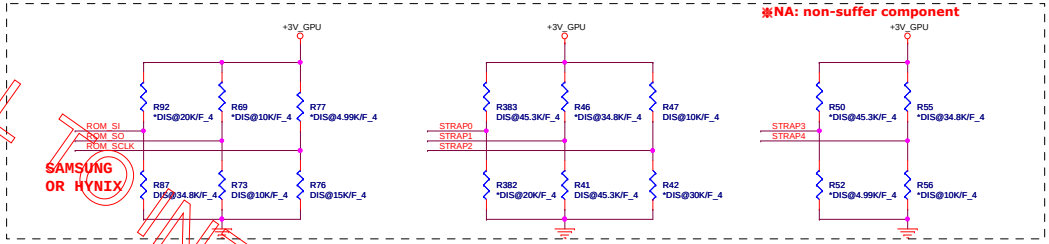
※ROM_SI Strap Bit for RAM Mapping

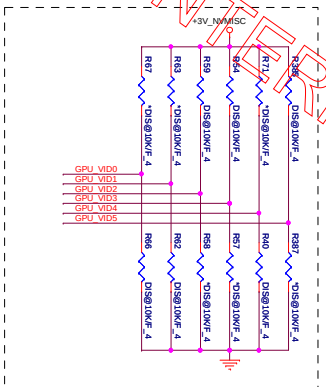
VRAM Configure	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN	RAMCFG [3:0]	ROM_SI
900MHz 2GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11	0x7(0111)	R87 (45.3K ohm)
900MHz 2GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C	0x6(0110)	R87 (34.8K ohm)
900MHz 1GB(64M*16) Samsung	AKD5EGGT500		K4W1G1646G-BC11	0x3(0011)	R87 (20K ohm)
900MHz 1GB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C	0x2(0010)	R87 (15K ohm)

GPU Model Strap Table

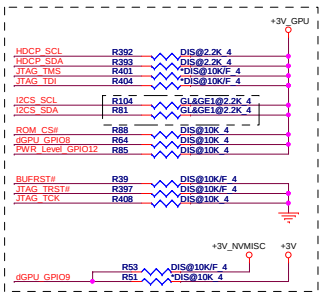
GPU Model	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1-A1 (GF119)	R73 (30K ohm) PD	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R47 (4.99K ohm) PU	R52 (4.99K ohm) PD	R56 (10K ohm) PD
N13P-GL-A1 (GF108)	R73 (10K ohm) PD	R76 (15K ohm) PD	R383 (45.3K ohm) PU	R41 (45.3K ohm) PD	R47 (10K ohm) PU	NA	NA
N13P-GS-A2 (GK107)	R69 (10K ohm) PU	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R42 (15K ohm) PD	R52 (4.99K ohm) PD	R56 (10K ohm) PD

※NA: non-suffer component





NVVDD Table	N13M-GE1-A1 (GF119)	N13P-GL-A1 (GF108)	N13P-GS-A1 (GK107)
	NVVDD (0.9V)	NVVDD (0.95V)	NVVDD (0.9V)
GPU_VID0	0 (R66)	0 (R66)	0 (R66)
GPU_VID1	0 (R62)	0 (R62)	0 (R62)
GPU_VID2	0 (R58)	1 (R59)	0 (R58)
GPU_VID3	0 (R57)	1 (R54)	0 (R57)
GPU_VID4	1 (R71)	0 (R40)	1 (R71)
GPU_VID5	1 (R385)	1 (R385)	1 (R385)



GPIO ASSIGNMENTS

GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	O	GPU Core VDD VID4
GPIO1	GPU_VID3	O	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding
GPIO4	LCD_BLEN	O	Panel Backlight Enable
GPIO5	GPU_VID1	O	GPU Core VDD VID1
GPIO6	GPU_VID2	O	GPU Core VDD VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB
GPIO15	HPD_C	I	Hot Plug Detect for IFPC
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID
GPIO17	HPD_D	I	Hot Plug Detect for IFPD
GPIO18	HPD_E	I	Hot Plug Detect for IFPE
GPIO19	HPD_F	I	Hot Plug Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		

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Quanta Computer Inc.
Size
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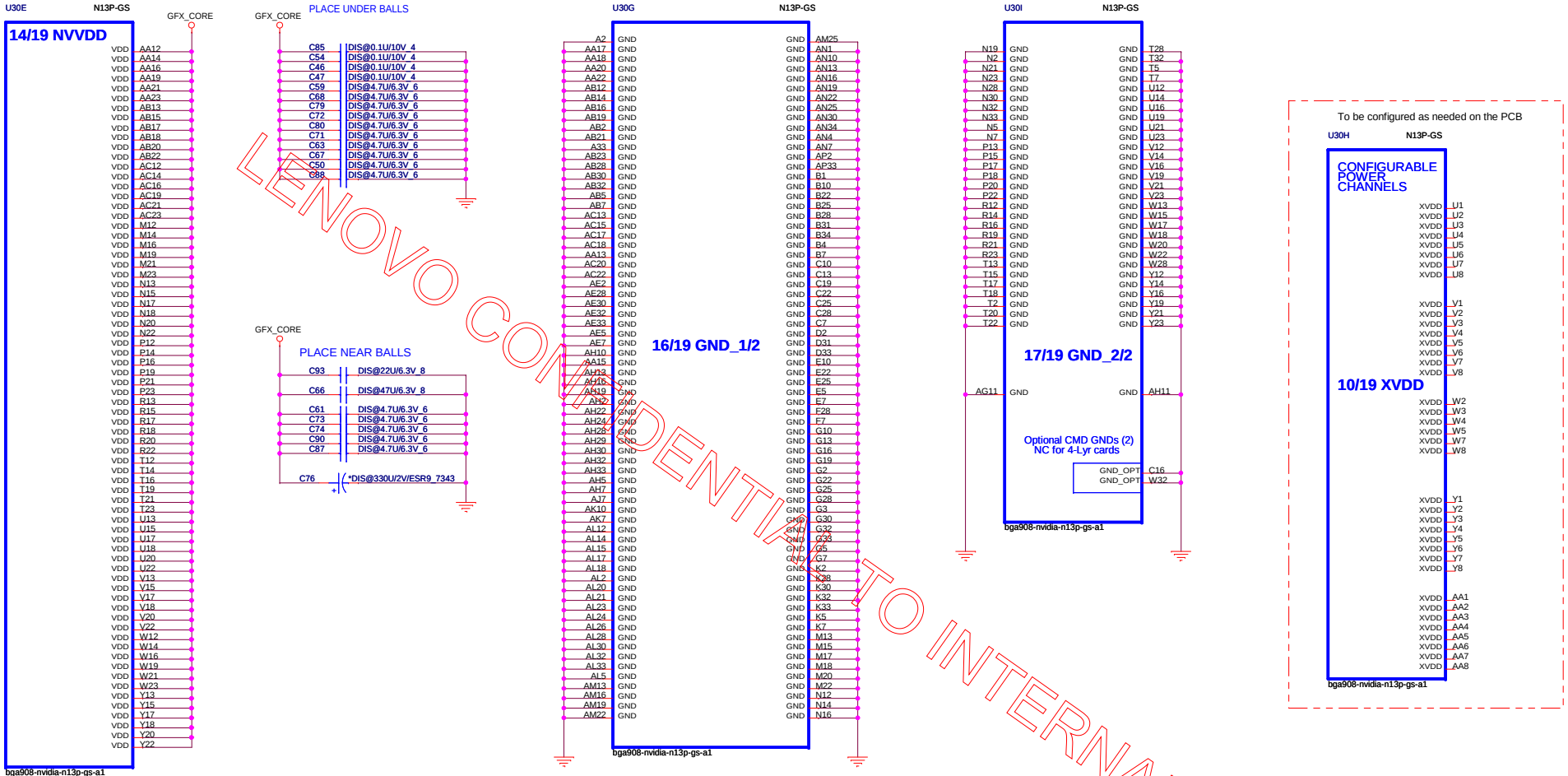

	R74	Q12
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

GPU	Signal/Rail	Stuffing Option
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor

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	Nvidia-N13P GB4-128(POWER)	1A

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[14,15,20,33,43] +1.5V_GPU

[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

CHANNEL A: 512MB/1024MB DDR3

U4 / U29 / U6 / U31 — 96-BALL SDRAM DDR3 DIS@K4W1G1646E-HC11

Should be 240 Ohms +-1%

R44 DIS@240/F_4
R377 DIS@240/F_4
R97 DIS@240/F_4
R390 DIS@240/F_4

+1.5V_GPU

R379 DIS@1.33K/F_4
R32 DIS@1.33K/F_4
R75 DIS@1.33K/F_4
R396 DIS@1.33K/F_4

VREFC_VMA1 / VREFD_VMA1 / VREFC_VMA3 / VREFD_VMA3

R378 DIS@1.33K/F_4
R28 DIS@1.33K/F_4
R80 DIS@1.33K/F_4
R395 DIS@1.33K/F_4

C452 DIS@0.01U/16V_4
C38 DIS@0.01U/16V_4
C115 DIS@0.01U/16V_4
C472 DIS@0.01U/16V_4

C461 *DIS@10U/6.3V_6

Placement has to be close to VRAM

VMA_CLKP0 — R26 DIS@162/F_4 — VMA_CLKN0
VMA_CLKP1 — R95 DIS@162/F_4 — VMA_CLKN1

C142	C45	C119	C459	C86
C81	C51	C91	C168	C169
C456	C473			

C507	C458	C468	C471	C463
C102	C465	C57	C505	C506
C170	C60			

C23	C32	C33	C36	C443
C62	C464	C40	C451	C470
C137	C124			

C442	C5	C446	C447	C439
C6	C70	C448	C121	C457
C128	C466			

All 0.1U/10V_4

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Quanta Computer Inc.		
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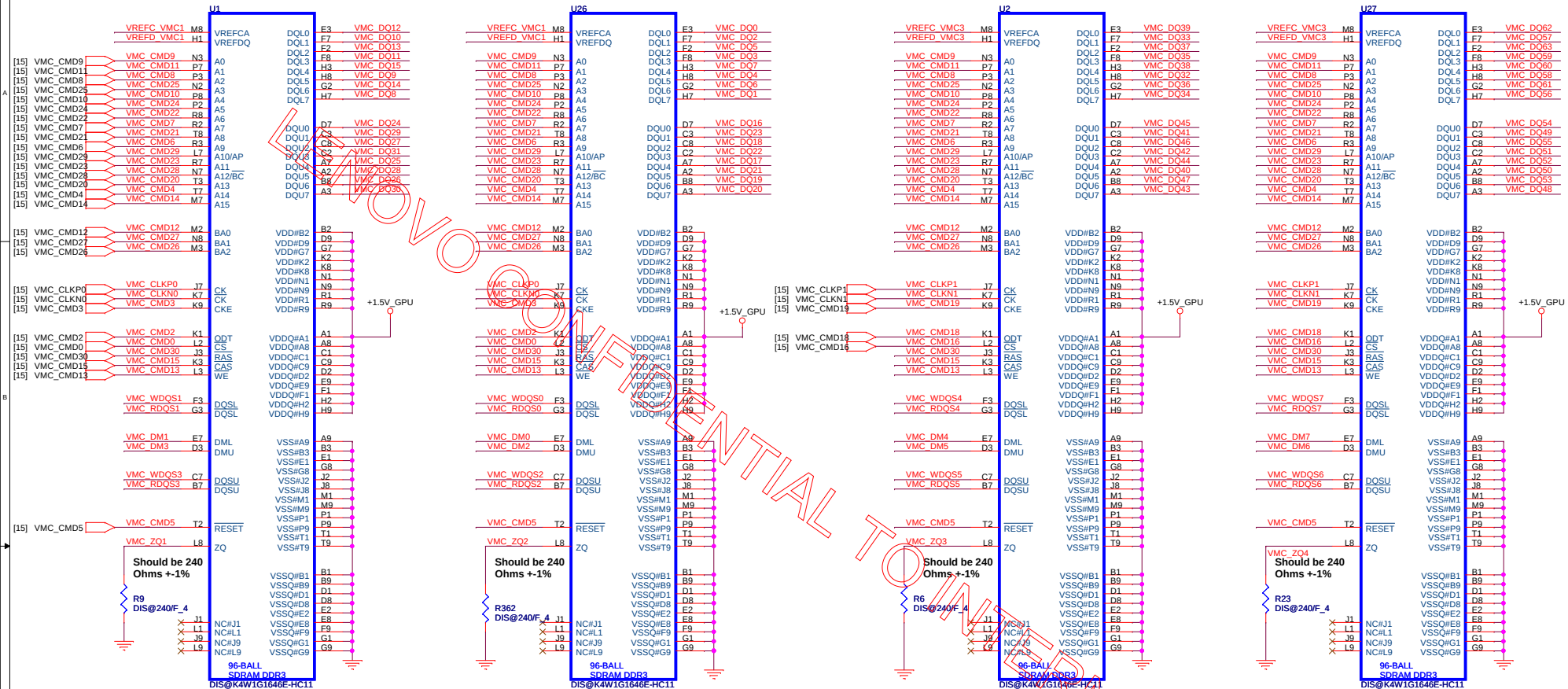
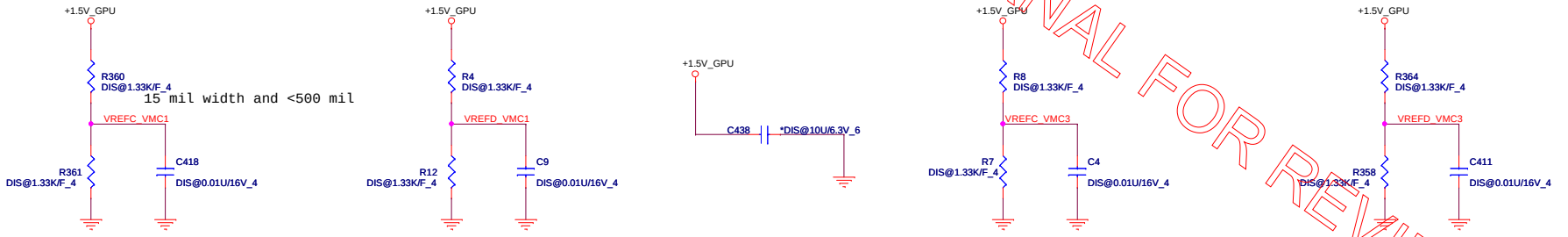
CHANNEL B: 512MB/1024MB DDR3

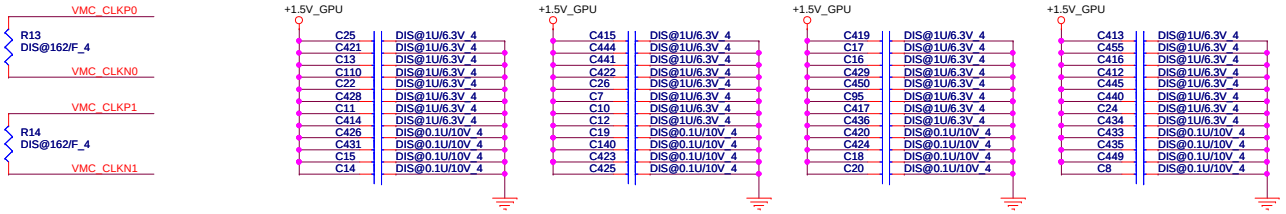
[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

[14,15,19,33,43] +1.5V_GPU





Placement has to be close to VRAM



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Nvidia-N13P GB4-128(VRAM-2)	1A

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[6,7,8,9,10,12,13,14,15,17,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[7,10,22,25,26,29,30,33,34] +5V

Change to KL6/BC HDMI CONN

[6] INT_HDMI_TXDP2 → C620 0.1U/10V_4 → HDMI_TX2+
[6] INT_HDMI_TXDN2 → C619 0.1U/10V_4 → HDMI_TX2-
[6] INT_HDMI_TXDP1 → C618 0.1U/10V_4 → HDMI_TX1+
[6] INT_HDMI_TXDN1 → C617 0.1U/10V_4 → HDMI_TX1-
[6] INT_HDMI_TXDP0 → C616 0.1U/10V_4 → HDMI_TX0+
[6] INT_HDMI_TXDN0 → C615 0.1U/10V_4 → HDMI_TX0-
[6] INT_HDMI_TXCP → C613 0.1U/10V_4 → HDMI_CLK+
[6] INT_HDMI_TXCN → C611 0.1U/10V_4 → HDMI_CLK-

[6] INT_HDMI_SCL → INT_HDMI_SCL
[6] INT_HDMI_SDA → INT_HDMI_SDA
[6] INT_HDMI_HPD → INT_HDMI_HPD

R316 2.2K_4, R297 2.2K_4
Q43 DMN5L06K-7
Q39 DMN5L06K-7
R313 2.2K_4, R568 2.2K_4
C668 *68p/50V_4, C669 *68p/50V_4
F2 FUSE_1.1A_8V_POLY
C667 0.1U/10V_4

CN16 CONN_HDMI
HDMI_TX2+ D2+
HDMI_TX2- D2 Shield
HDMI_TX1+ D2-
HDMI_TX1- D1+
HDMI_TX0+ D1 Shield
HDMI_TX0- D1-
HDMI_CLK+ D0+
HDMI_CLK- D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
HDMI_DDC_CLK DDC CLK
HDMI_DDC_DAT DDC DATA
GND
HDMIC_5V +5V
HP_DET HP DET
SHELL1, SHELL2, SHELL3, SHELL4

R315 590/F_4 → HDMI_TX2+
R310 590/F_4 → HDMI_TX2-
R304 590/F_4 → HDMI_TX1+
R302 590/F_4 → HDMI_TX1-
R300 590/F_4 → HDMI_TX0+
R298 590/F_4 → HDMI_TX0-
R294 590/F_4 → HDMI_CLK+
R291 590/F_4 → HDMI_CLK-
SC51 *0.1U/10V_4
3HDMI_LF
Q42 2N7002K

R551 10K_4
R553 10K_4
Q69A ME2N7002DKW-G
Q69B ME2N7002DKW-G
R549 20K_4
Place close to PCH

For ESD

U39 *CM1225
HDMI_TX2+ → HDMI_TX2+
HDMI_TX2- → HDMI_TX2-
HDMI_TX1+ → HDMI_TX1+
HDMI_TX1- → HDMI_TX1-

U38 *CM1225
HDMI_TX0+ → HDMI_TX0+
HDMI_TX0- → HDMI_TX0-
HDMI_CLK+ → HDMI_CLK+
HDMI_CLK- → HDMI_CLK-

U37 *CM1225
HDMI_DDC_DAT → HDMI_DDC_DAT
HDMI_DDC_CLK → HDMI_DDC_CLK
HDMIC_5V → HDMIC_5V
HP_DET → HP_DET

For EMI

R574 150/F_4 (HDMI_TX2+ / HDMI_TX2-)
R573 150/F_4 (HDMI_TX1+ / HDMI_TX1-)
R572 150/F_4 (HDMI_TX0+ / HDMI_TX0-)
R569 150/F_4 (HDMI_CLK+ / HDMI_CLK-)

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

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Layout Note:
Setting R,G,B trace impedance to 50 ohm.

[6] INT_CRT_RED
[6] INT_CRT_GRE
[6] INT_CRT_BLU
[6] INT_CRT_VSYNC
[6] INT_CRT_HSYNC
[6] INT_DDCCLK
[6] INT_DDCDAT

CRT_VCC
D22 RB500V-40
C526 0.1U/10V_4
+5V
C527 0.1U/10V_4
F1 FUSE_1.1A_8V_POLY
CRT_VCC_R

L7 BLM15BA470SS1D
L8 BLM15BA470SS1D
L9 BLM15BA470SS1D
CRT_R1
CRT_G1
CRT_B1

R231 150/F_4
R232 150/F_4
R228 150/F_4
C212 5.6P/50V/COG_4
C214 5.6P/50V/COG_4
C225 5.6P/50V/COG_4
C215 5.6P/50V/COG_4
C213 5.6P/50V/COG_4
C211 5.6P/50V/COG_4
TP15

CN12
CRT_CONN

ESD PROTECTION
U35
CRT_R1
CRT_G1
CRT_B1
CRT_VCC_R
CRT_VCC
*IP4220CZ6
U12
CRTVSYNC
CRTHSYNC
DDCCLK
DDCDAT
CRT_VCC
*IP4220CZ6

+5V
U33 AHCT1G125DCH
U34 AHCT1G125DCH
C554 0.1U/10V_4
VGAVSYNC_R
VGAHSYNC_R
R493 10_4
R502 10_4
Place near U37,U38 < 200 mil
CRTVSYNC1
CRTHSYNC1
C538 *10P/50V/COG_4
C529 *10P/50V/COG_4
L25 BK1608HS121-T
L26 BK1608HS121-T
CRTVSYNC
CRTHSYNC
C539 10P/50V/COG_4
C528 10P/50V/COG_4
Place near CN5002 connector < 200 mil

+3V
R201 2.2K_4
R163 2.2K_4
CRT_VCC
R191 4.7K_4
R177 4.7K_4
Q64A ME2N7002DKW-G
Q64B ME2N7002DKW-G
DDCCLK
DDCDAT
C201 *10P/50V/COG_4
C194 *10P/50V/COG_4
For EMI

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Quanta Computer Inc.
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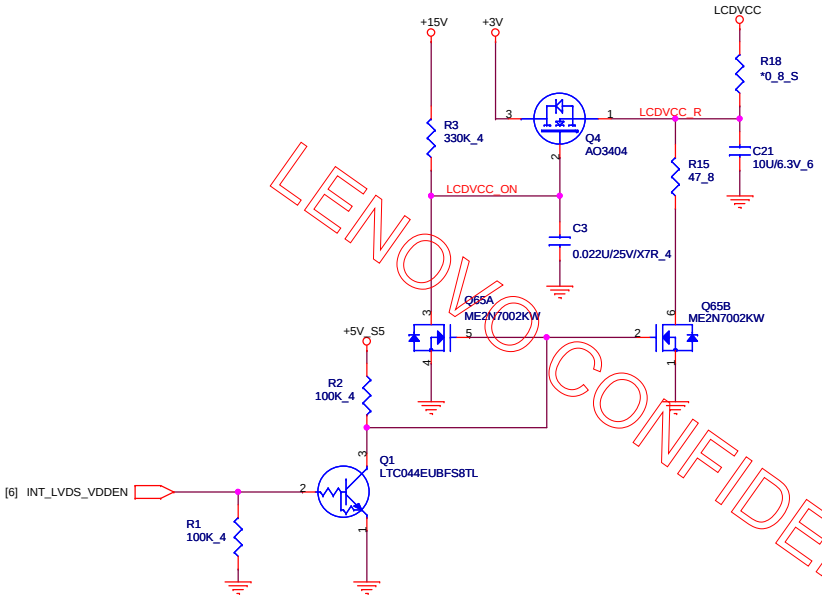
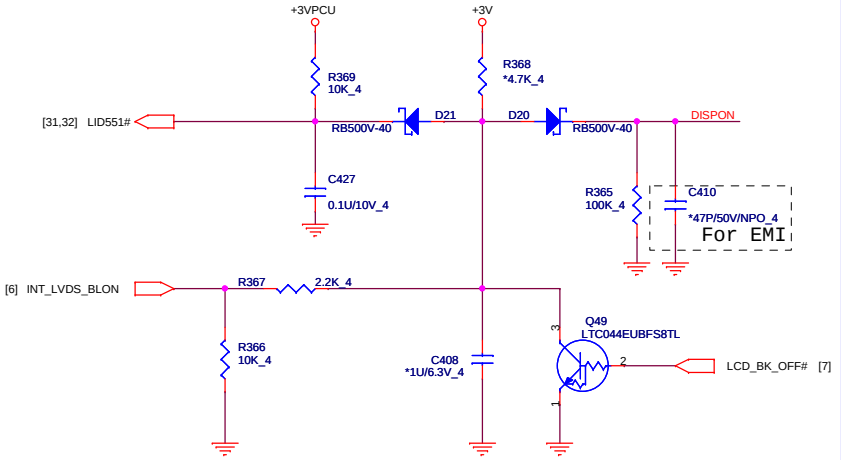
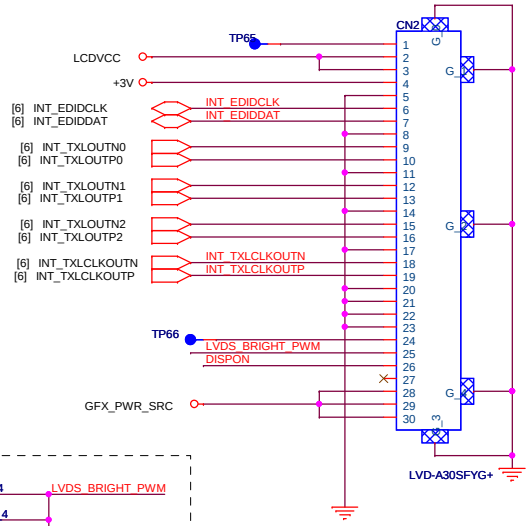
[26,30,34,36,43] +15V
[6,7,8,9,10,12,13,14,15,17,21,22,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[10,26,28,31,33,34] +5V_S5
[6,7,24,26,27,31,32,34,35,36,40] +3VPCU
[33,35,36,37,38,39,41,42] VIN

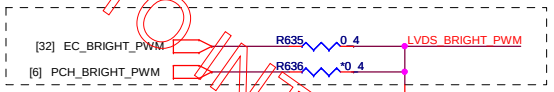
LCDVCC

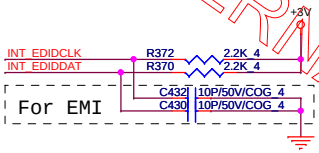


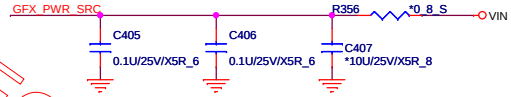
Back Light

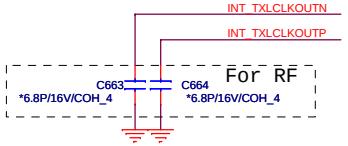












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Quanta Computer Inc.

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Custom	LCD CONN	1A

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[6,7,23,26,27,31,32,34,35,36,40] +3VPCU
[33,34] LANVCC
[6,7,8,9,10,12,13,14,15,17,21,22,23,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V

LANVCC

+3VPCU, LANVCC
Q47 AO6402A
[34] LAN_ON
R341 *0_8_S
LANVCC_R
C394 *10U/6.3V_8
C393 0.1U/10V_4

* R594 open when use RTL8105E

TP60, R594 *LAN1G@10K_4, R599 1K/F_4
C650 *10P/50V/COG_4 RJ45_LINKUP#
C644 *10P/50V/COG_4 RJ45_ACTIVITY#
LED3/EEDO, EECS R606 10K_4, EEDI R603 10K_4, TP62

U45 RTL81111F/RTL8105E

CTRL12/VDD, LANVCC, CTRL12A, LAN_DVDD12, LAN_EVDD12
VDDREG, AVDD33, AVDD33(NC), DVDD33, DVDD3, REGOUT, AVDD10, AVDD10(NC), DVDD10, DVDD10(NC), EVDD10
GPO/SMBALERT, SMBCLK(NC)/SMBDATA(NC), LED1/EESK, LED0, LED3/EEDO, EECS/SCL, EEDI/SDA
MDIP0/MDIN0 MDI 0+/0-, MDIP1/MDIN1 MDI 1+/1-, MDIP2(NC)/MDIN2(NC) MDI 2+/2-, MDIP3(NC)/MDIN3(NC) MDI 3+/3-
ISOLATEB, LANWAKEB, ENSWREG, CKXTAL1, CKXTAL2, RSET, PERSTB, CLKREQB, HSIP, HSIN, REFCLK_P, REFCLK_N, HSOP, HSON, GND

+3V
R601 1K_4
R600 15K_4
D24 RB500V-40
PCIE_WAKE# [6,27,32]
LANVCC
LAN_ISOLATEB [32]
Y4 25MHZ
C637 33P/50V/NPO_4
C638 33P/50V/NPO_4
R593 2.49K/F_4
[2,8,14,27] PLTRST#
[8] PCIE_CLKREQ_LAN#
GPP_TX2N_LAN C649 0.1U/10V_4
GPP_TX2P_LAN C646 0.1U/10V_4
PCIE_RXN2_LAN [8]
PCIE_RXP2_LAN [8]
CLK_PCIE_LANN [8]
CLK_PCIE_LANP [8]
PCIE_TXN2_LAN [8]
PCIE_TXP2_LAN [8]

LANVCC: C656 0.1U/10V_4, C654 0.1U/10V_4, C633 0.1U/10V_4, C648 0.1U/10V_4, C639 0.1U/10V_4, R607 *0_8_S, C634 0.1U/10V_4
CTRL12/VDD: C653 0.1U/10V_4, C657 4.7U/6.3V_6

* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.

Place C5113 ,C5094 closed to U5006 pins44,45.

* C476 and C472 are for U24 LAN_EVDD12 pin 21.

CTRL12A, L28 4.7uH, CTRL12A_R
C662 4.7U/6.3V_6, C661 0.1U/10V_4
R609 *0_8_S, R611 *0_8_S
LAN_EVDD12: C659 1U/6.3V_4, C642 0.1U/10V_4
LAN_DVDD12: C635 0.1U/10V_4, C632 0.1U/10V_4, C636 0.1U/10V_4, C655 0.1U/10V_4, C641 0.1U/10V_4, C630 0.1U/10V_4, C631 0.1U/10V_4

* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

Tramsformer

Reserve for Surge
Line to Line TVS
U41 *UCLAMP2512T.TCT

U43 *CM1293A-04SO
U22 *LAN1G@CM1293A-04SO
10/100 non-stuff
Reserve for Surge
Line to GND TVS

MDI_0-/0+/1-/1+/2-/2+/3-/3+ R590 1/F_4, R589 1/F_4, R584 1/F_4, R583 1/F_4, R588 *LAN1G@1/F_4, R587 *LAN1G@1/F_4, R586 *LAN1G@1/F_4, R585 *LAN1G@1/F_4
MDI_0-_C, MDI_0+_C, MDI_1-_C, MDI_1+_C, MDI_2-_C, MDI_2+_C, MDI_3-_C, MDI_3+_C

U40 TST1284R LF
TD4-/TD4+/TCT4/TD3-/TD3+/TCT3/TD2-/TD2+/TCT2/TD1-/TD1+/TCT1
MX4-/MX4+/MCT4/MX3-/MX3+/MCT3/MX2-/MX2+/MCT2/MX1-/MX1+/MCT1
LAN_MX0-/MX0+/MCT0/MX1-/MX1+/MCT1/MX2-/MX2+/MCT2/MX3-/MX3+/MCT3

Layout:All termination signal should have 30 mil trace

R570 75/F_8 LANCT3, D30 *BS201N-LV_1206 LANCT5
R571 75/F_8, D31 *BS201N-LV_1206
R296 0/F_8 For EMI, D32 *BS201N-LV_1206
R295 0/F_8 For EMI, D33 *BS201N-LV_1206
Gas Tube Discharge _ Reserve for Surge
Reserve for Surge
Line to GND Gas Tube Discharge
C366 10P/3KV/NPO_1808
R327 1M_8
PJP18 *SHORTPAD

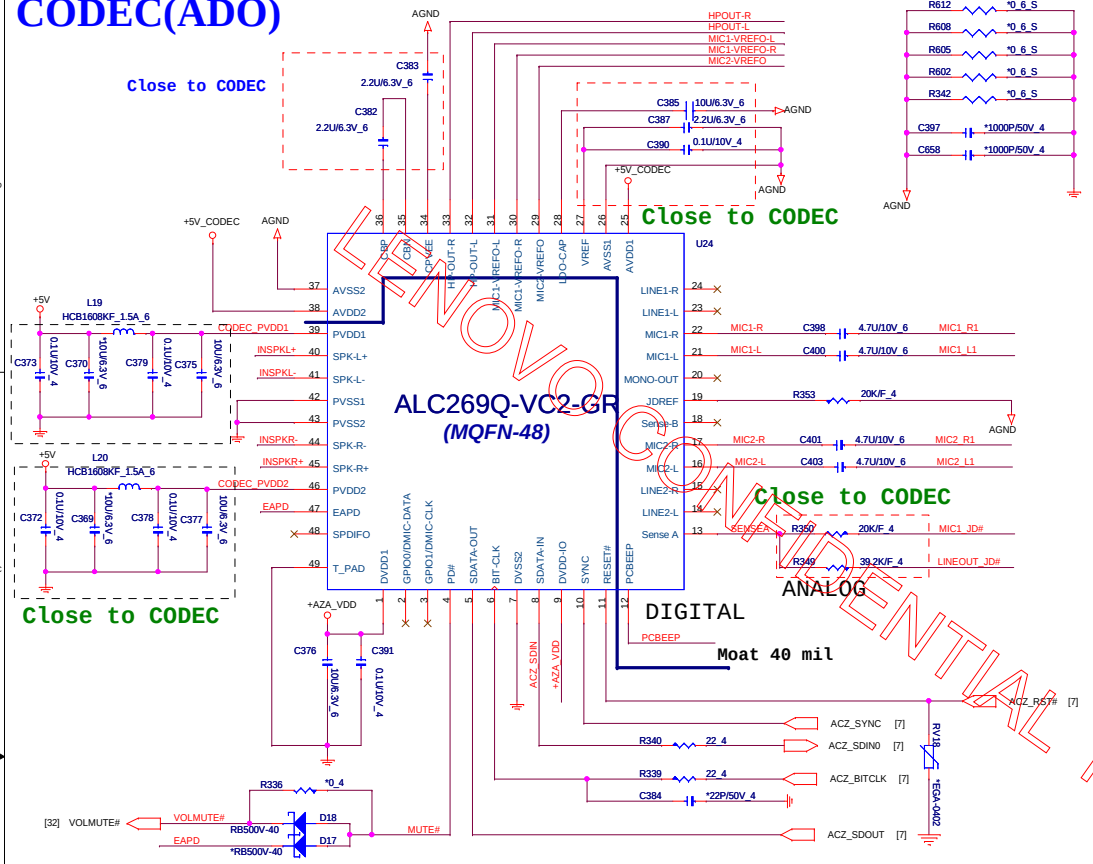
U20 *LAN1G@UCLAMP2512T.TCT
Reserve for Surge
Line to Line TVS
C623 0.01U/50V/X7R_4

RJ45 Connector

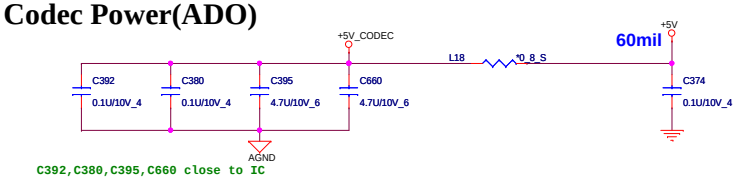
RV15 *AZ5123-01H, RV14 *AZ5123-01H
EMI:close RJ45
C270 *0.1U/10V_4
CN13
LANVCC R256 150_4
Orange LED
LAN_OLED, RJ45_LINKUP#
LAN_MX0+/0-/1+/1-/2+/2-/3+/3-
LANVCC R567 150_4
LAN_GLED, RJ45_ACTIVITY#
GREEN LED
RJ45
RV26 *AZ5123-01H, RV27 *AZ5123-01H
C609 *0.1U/10V_4
EMI:close RJ45

PROJECT : LZ2A			
Quanta Computer Inc.			
Size: Custom	Document Number: RTL81111F/RTL8105E		Rev: 1A
Date: Wednesday, November 30, 2011	Sheet 24 of 45		

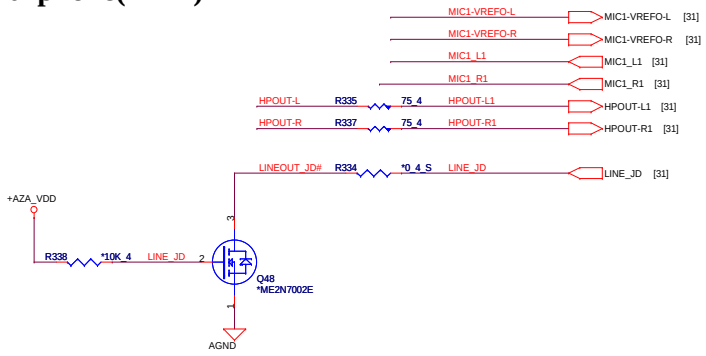
CODEC(ADO)



Codec Power(ADO)

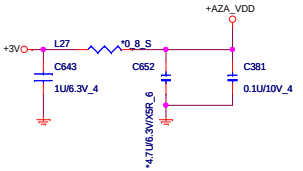


Earphone(AMP)

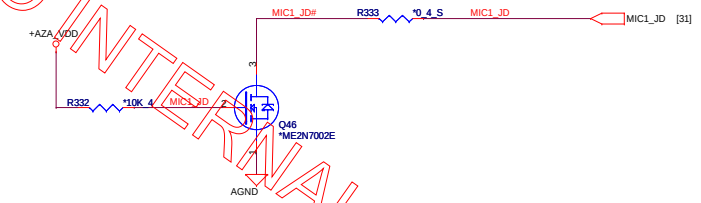


HDA Power(ADO)

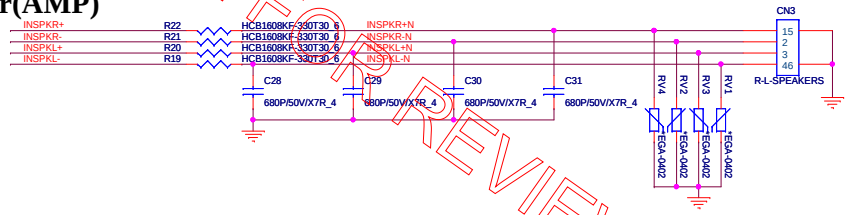
*Intel HDA Either +1.5V_S5 or +3V_S5



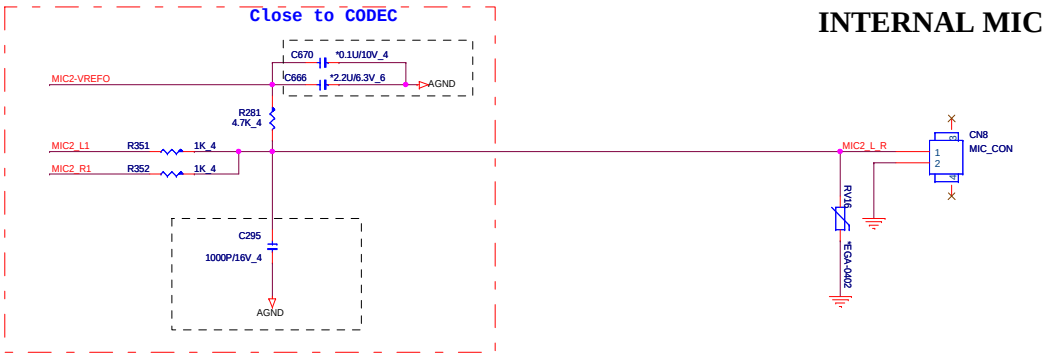
System MIC(AMP)



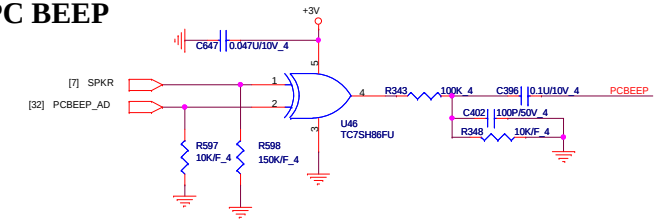
Speaker(AMP)



INTERNAL MIC



PC BEEP

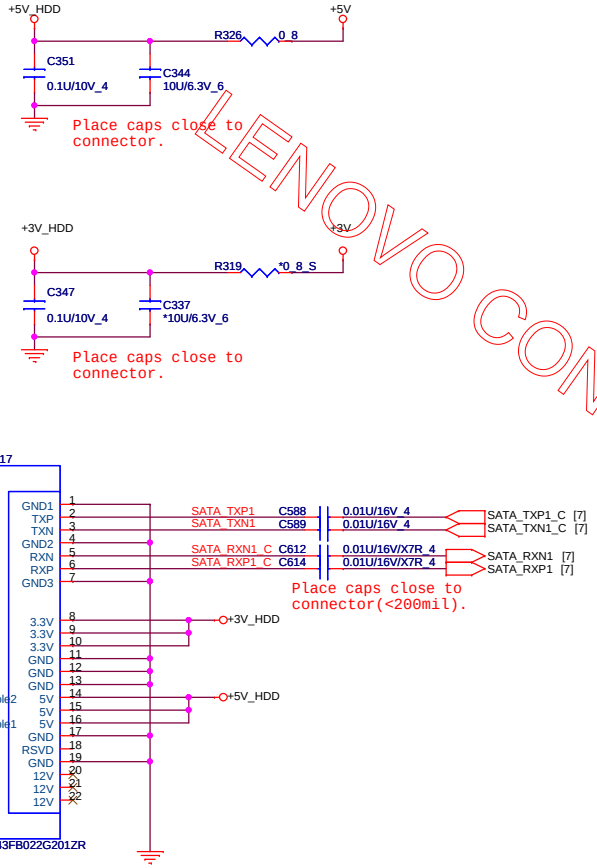


PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ALC269/MIC/Line out	1A

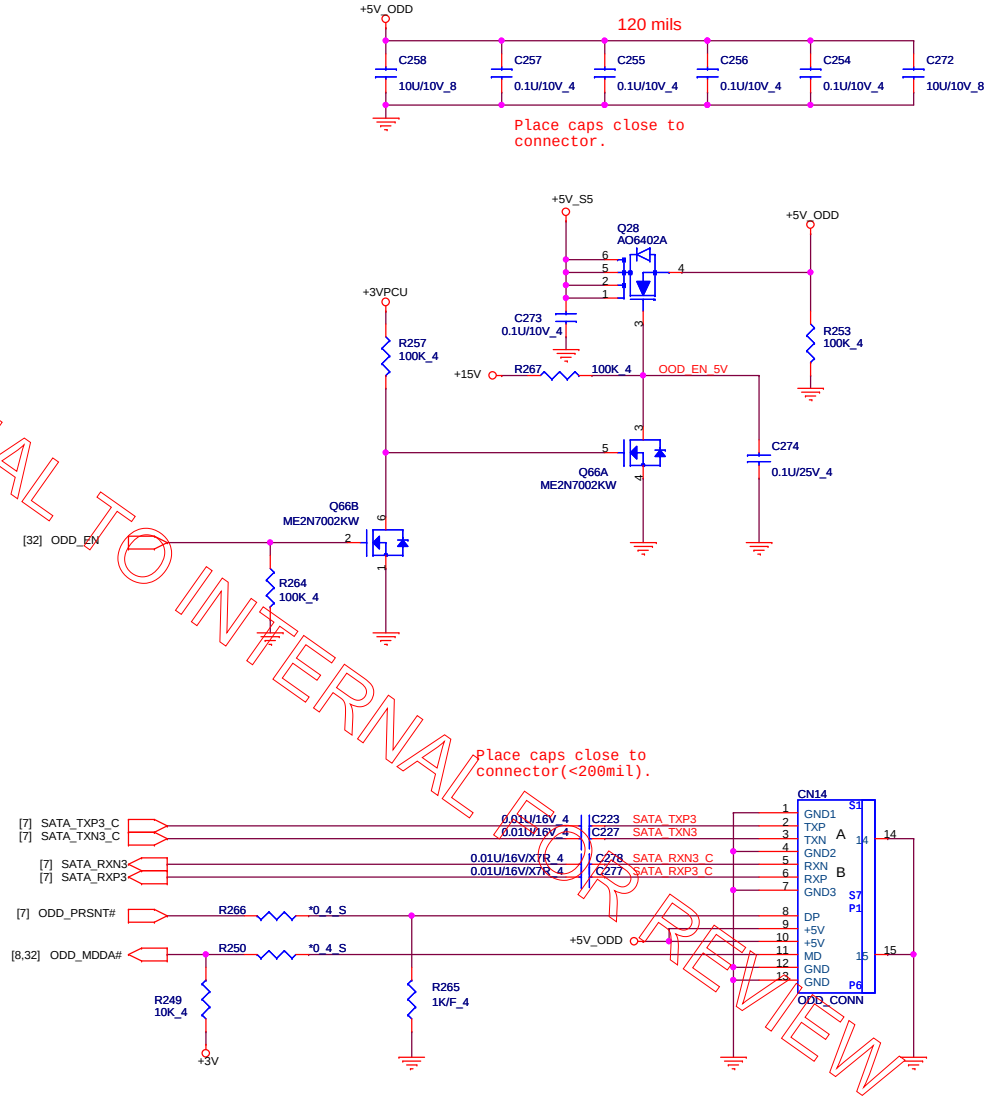
Date: Wednesday, November 30, 2011 Sheet 25 of 45

SATA HDD Connector.



SATA ODD Connector.

[7,10,21,22,25,29,30,33,34] +5V
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[10,34,35,36,37,38,39,40,41,42,43] +5VPCU
[6,7,23,24,27,31,32,34,35,36,40] +3VPCU
[23,30,34,36,43] +15V



PROJECT : LZ2A

Quanta Computer Inc.

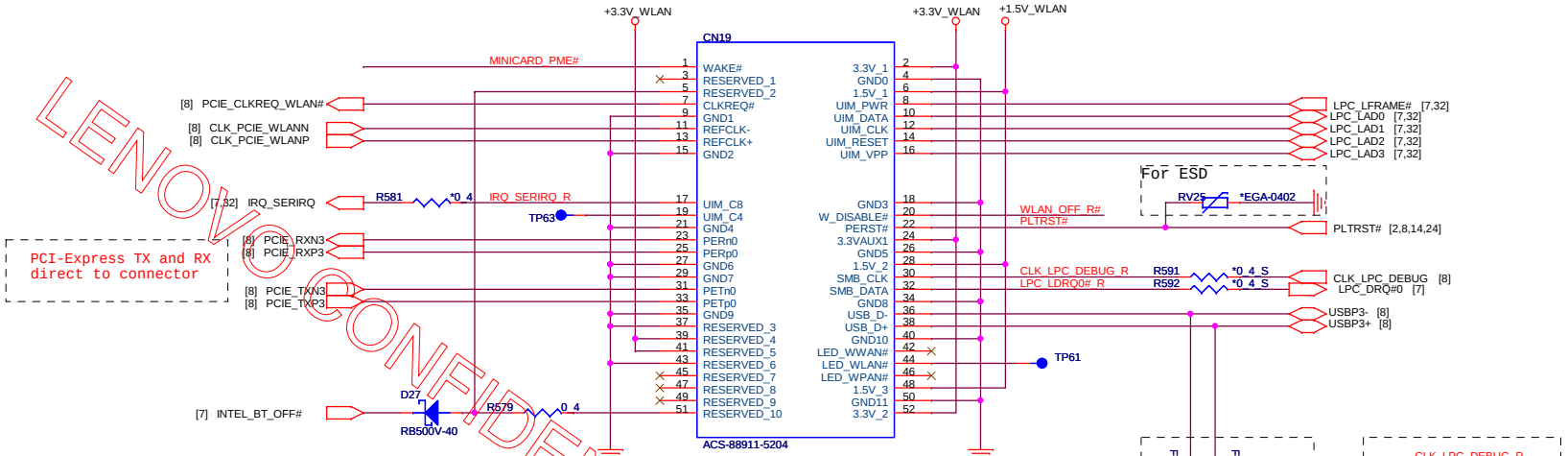
Size	Document Number	Rev
Custom	SATA HDD/CD-ROM	1A

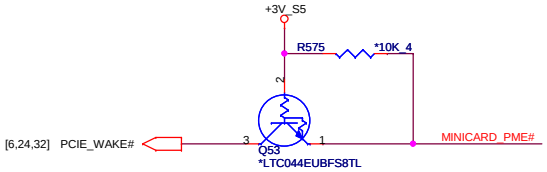
Date: Wednesday, November 30, 2011 Sheet 26 of 45

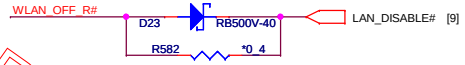
MiniCard WLAN connector

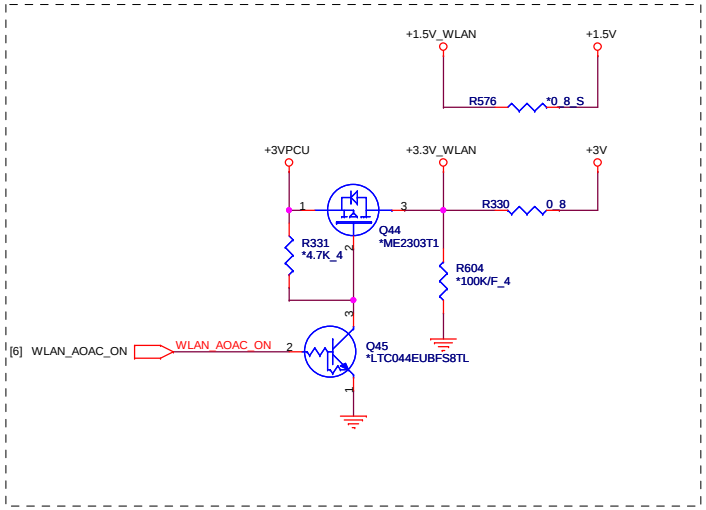
[2,6,7,8,9,10,31,34] +3V_S5
[4,10] +1.5V
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,29,30,31,32,33,34,37,38,41,42,43] +3V

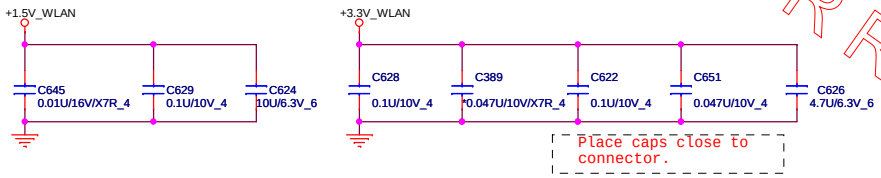
27









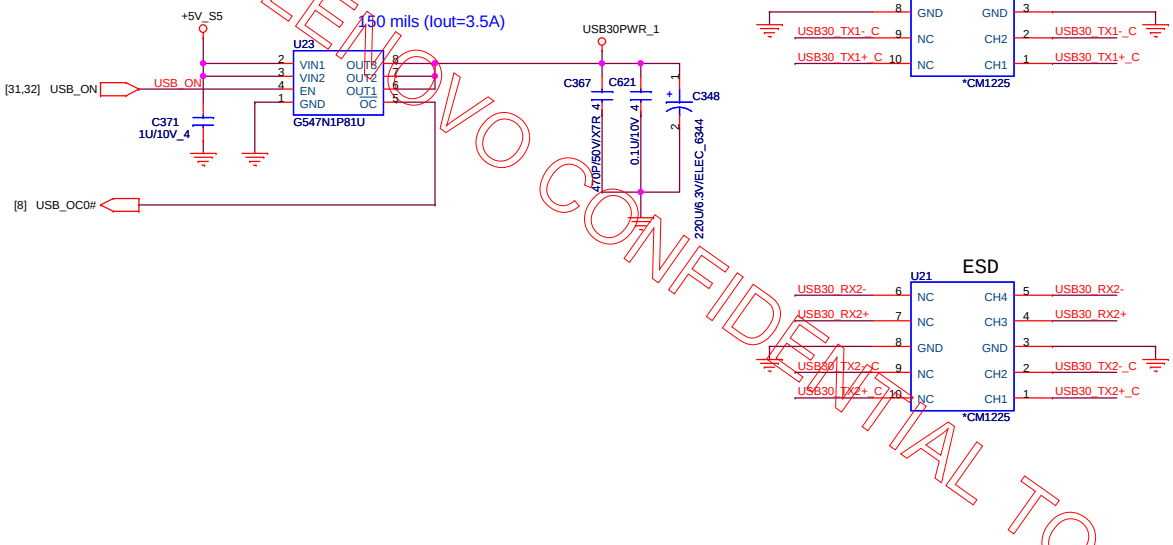


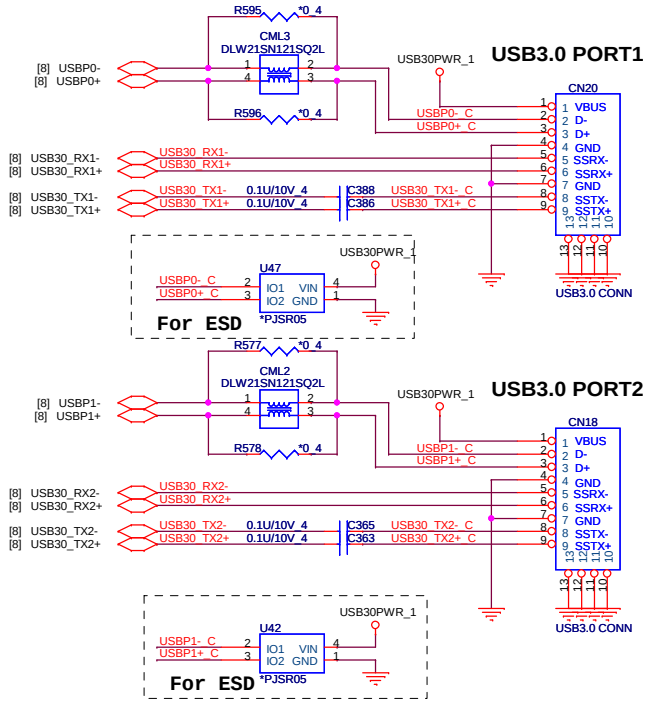
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB2.0*2/WLAN/BT	1A

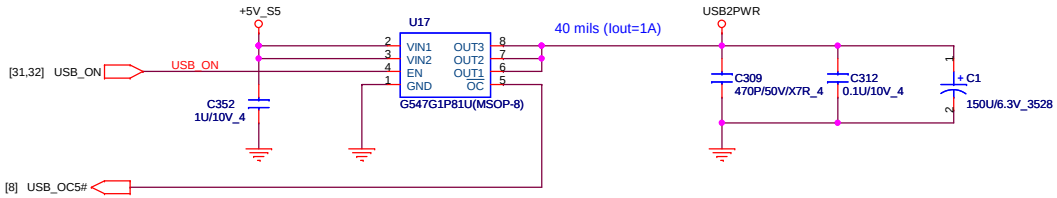
Date: Wednesday, November 30, 2011 Sheet 27 of 45

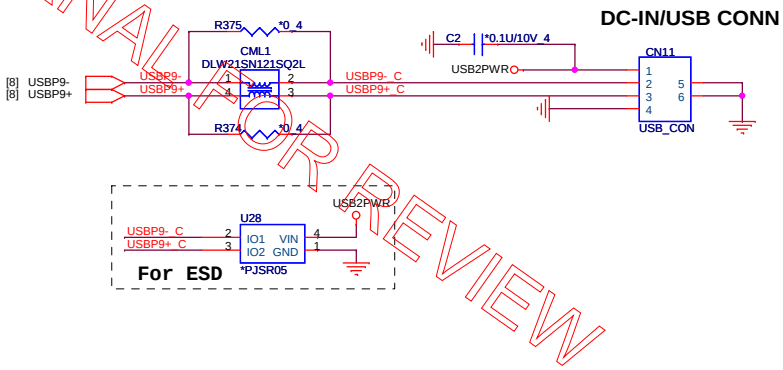
USB3.0*2





USB2.0*1

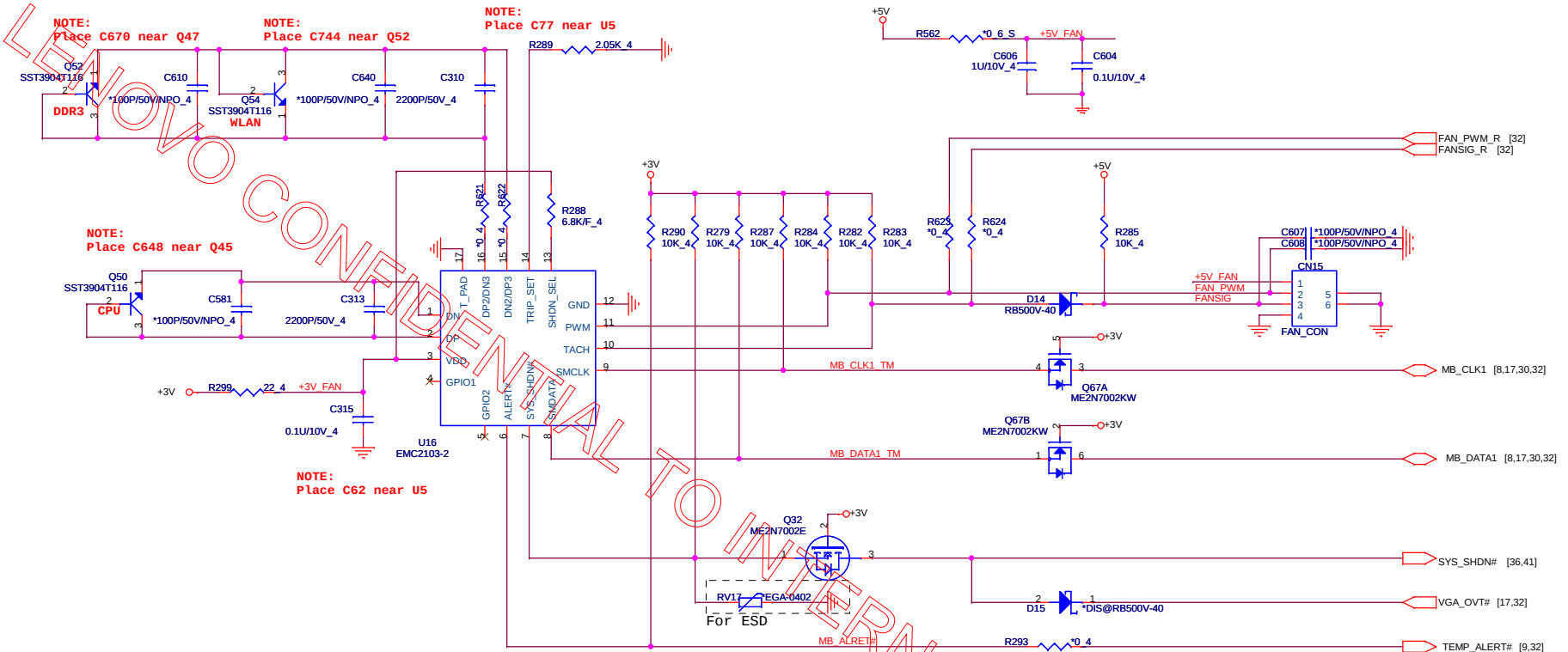




PROJECT : LZ2A		
Quanta Computer Inc.		
Size: Custom	Document Number: USB3.0 *1	Rev: 1A
Date: Wednesday, November 30, 2011	Sheet 28 of 45	

[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,30,31,32,33,34,37,38,41,42,43] +3V
[7,10,21,22,25,26,30,33,34] +5V

FAN CONTROL



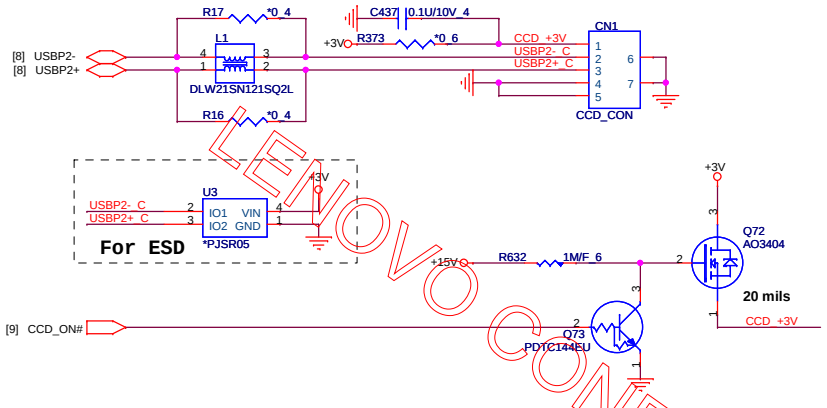
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN /THERMAL	1A

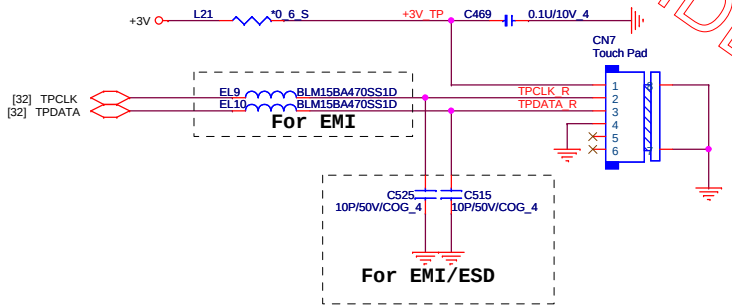
Date: Wednesday, November 30, 2011 Sheet 29 of 45

[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,31,32,33,34,37,38,41,42,43] +3V
[7,10,21,22,25,26,29,33,34] +5V
[23,26,34,36,43] +15V

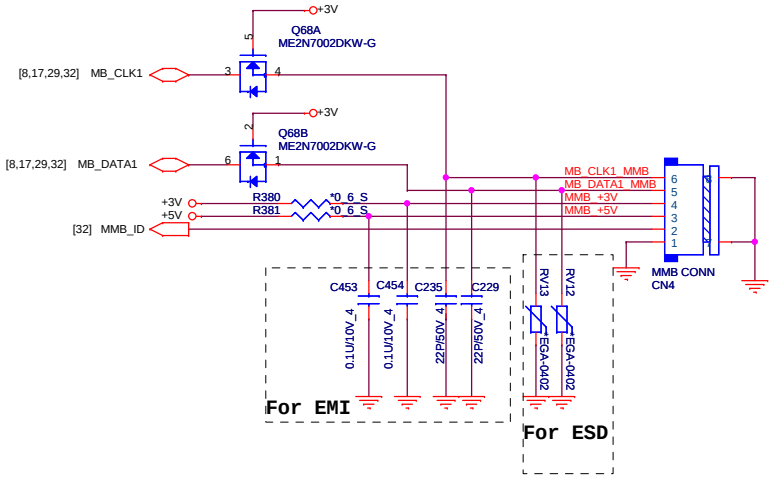
CCD BOARD



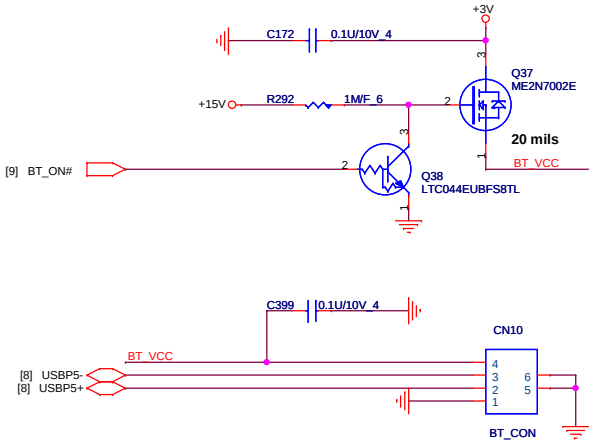
Touch pad



MMB



BLUETOOTH



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CCD/TP/BT/MMB	1A

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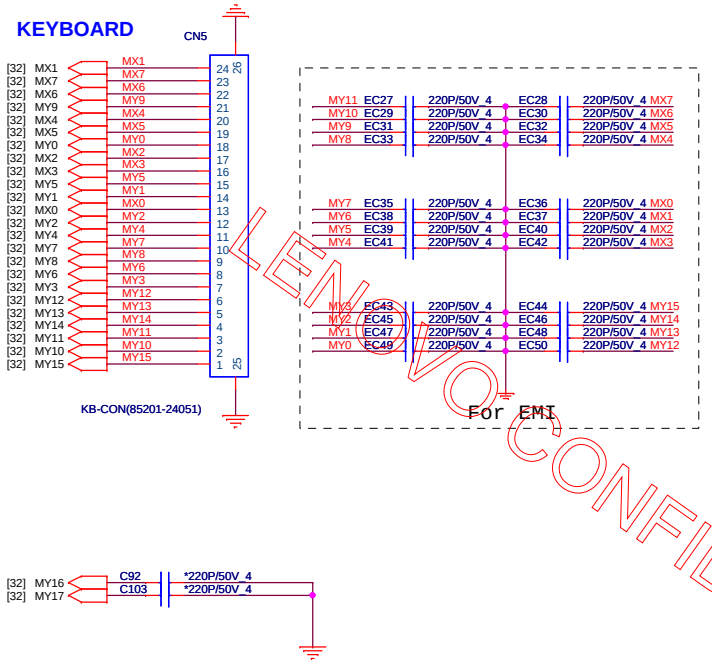
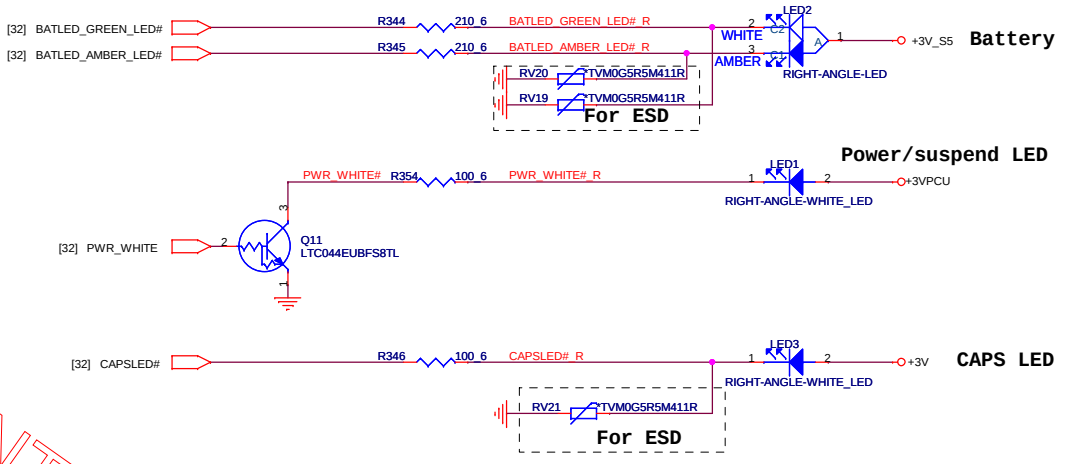
KEYBOARD

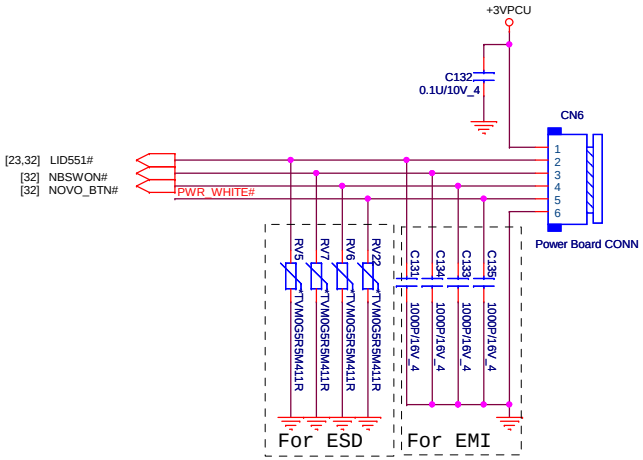


LED

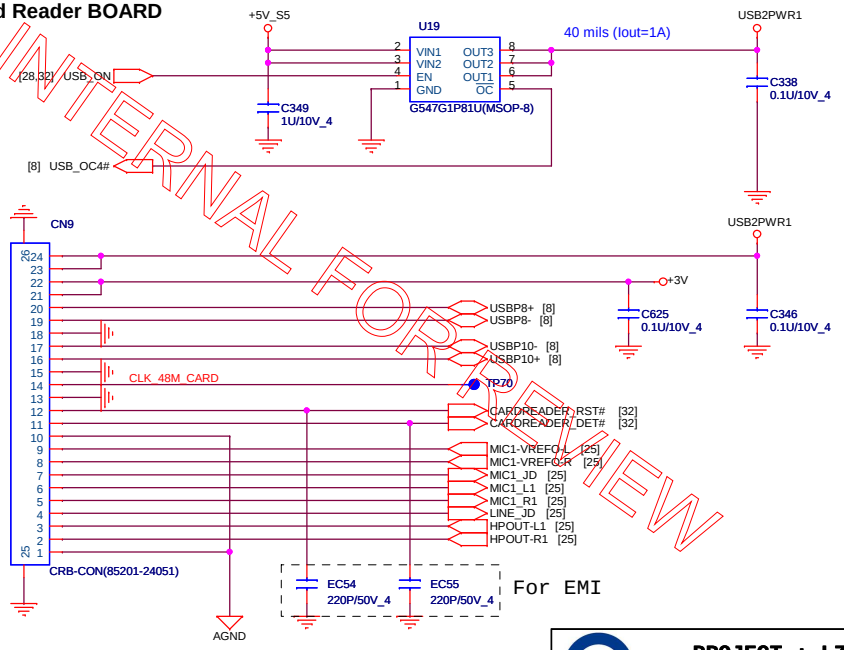
[6,7,23,24,26,27,32,34,35,36,40] +3VPCU
[10,23,26,28,33,34] +5V_S5
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,32,33,34,37,38,41,42,43] +3V
[2,6,7,8,9,10,27,34] +3V_S5



POWER BOARD



Card Reader BOARD



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/PB/LED/CRB	1A

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IT8518
IT8519

U10
IT8518

LPC
GPIO
SM_BUS
PS/2
CIR
UART port
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
PWM
WAKE UP
A/D D/A
CLOCK

Layout Note:
Place all capacitors close to IT8512

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512

For Deep S3

(For PLL Power)

Board ID

DIS =>R116
UMA=>R115

POWER SWITCH/ NOVO BUTTON

4Mbit (512K Byte), SPI

Winbond	AKE38ZP0N00
SST	AKE28FP0K07
MX	AKE37FP0Z13

W25X40BVSSIG

For EMI

Project	PU/PD
Z380(LZ1)-INTEL	PU
Z480(LZ2)-INTEL	PU
Z485(LZ2)-AMD	PU
Z580(LZ3)-INTEL	PD
Z585(LZ3)-AMD	PD

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBC IT8518	1A

Date: Wednesday, November 30, 2011 Sheet 32 of 45

Screw for ME

SPAD1 *SPAD-Z480-1
SPAD3 *SPAD-Z480-1
SPAD4 *SPAD-Z480-2
SPAD2 *SPAD-Z480-2

VGA
HOLE12 DIS@H-TC5_5BC4I3D3P2
HOLE13 H-TC5_5BC4I3D3P2
SMT NUT H=4/7mm

HOLE8 *HG-TC276BC315D106P2
HOLE10 *HG-TC276BC315D106P2
HOLE6 *HG-TC256BC315D106P2
HOLE11 *HG-TC276BC315D106P2

CPU BKT

HOLE4 *H-C86D86N
HOLE7 *C142D102N
HOLE3 *H-TC217BC256D118P2
HOLE14 *H-TC7IC3_7BC8D2_7P2
HOLE9 *H-C87D87N
HOLE5 *H-O316X276ID91P2
HOLE2 *H-O316X276ID91P2
HOLE1 *H-TC6_3IC3_7BC8D2_7P2

For ESD

+0.85V +1.8V SC23 SC24 *0.1U/10V_4
+1.05V_GFX_PCIE +1.05V_PCH SC31 SC32 *0.1U/10V_4
+0.85V +1.5V_CPU SC11 SC13 SC12 SC27 SC26 *0.1U/10V_4
+5V_S5 SC42 *0.1U/10V_4
+5V_S5 SC41 *0.1U/10V_4
+1.5V_SUS +1.5V_CPU SC29 SC28 *0.1U/10V_4
+1.5V_SUS VIN SC40 SC39 0.1U/25V_4
+3V +5V SC33 SC30 0.1U/10V_4
+VCC_CORE VIN SC9 SC46 0.1U/25V_4
+VCC_GFX SC15 SC18 *0.1U/10V_4
+5V SC38 SC25 SC37 0.1U/10V_4
+1.05V_GFX_PCIE GFX_CORE SC4 *0.1U/10V_4
+VCC_GFX SC17 SC16 SC14 SC20 SC19 SC21 *0.1U/10V_4
+1.05V_PCH SC49 SC22 SC50 SC47 SC48 *0.1U/10V_4
+1.05V_PCH
+1.05V_GFX_PCIE SC6 SC5 *0.1U/10V_4
+VCC_CORE SC8 SC10 *0.1U/10V_4
+1.5V_GPU SC2 SC43 SC3 *0.1U/10V_4
+1.5V_GPU SC7 SC45 *0.1U/10V_4
+1.5V_GPU SC44 SC1 *0.1U/10V_4
+1.5V_SUS SC35 SC34 SC36 *0.1U/10V_4

For EMI

VIN EC6 EC20 EC12 EC25 EC1 EC18 EC2 EC21 EC5 EC3 EC16 0.1U/25V_4
LANVCC EC11 0.1U/10V_4
VBATT EC22 0.1U/25V_4
+1.5V_SUS EC2 3.3p/16V/NP0_4
+1.5V_SUS EC1 3.3p/16V/NP0_4
+1.5V_WLAN EC5 47P/50V/NPO_4
+3.3V_WLAN EC3 47P/50V/NPO_4
+5V EC51 EC52 0.1U/10V_4 *0.1U/10V_4

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
B	HOLD/SKEW/ESD/EMI	1A

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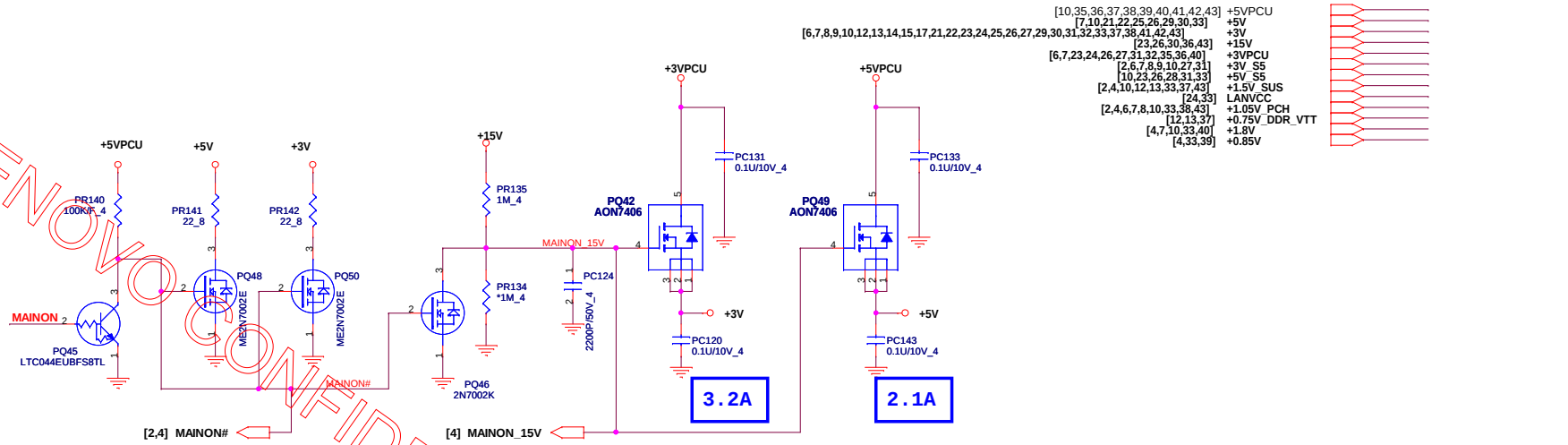
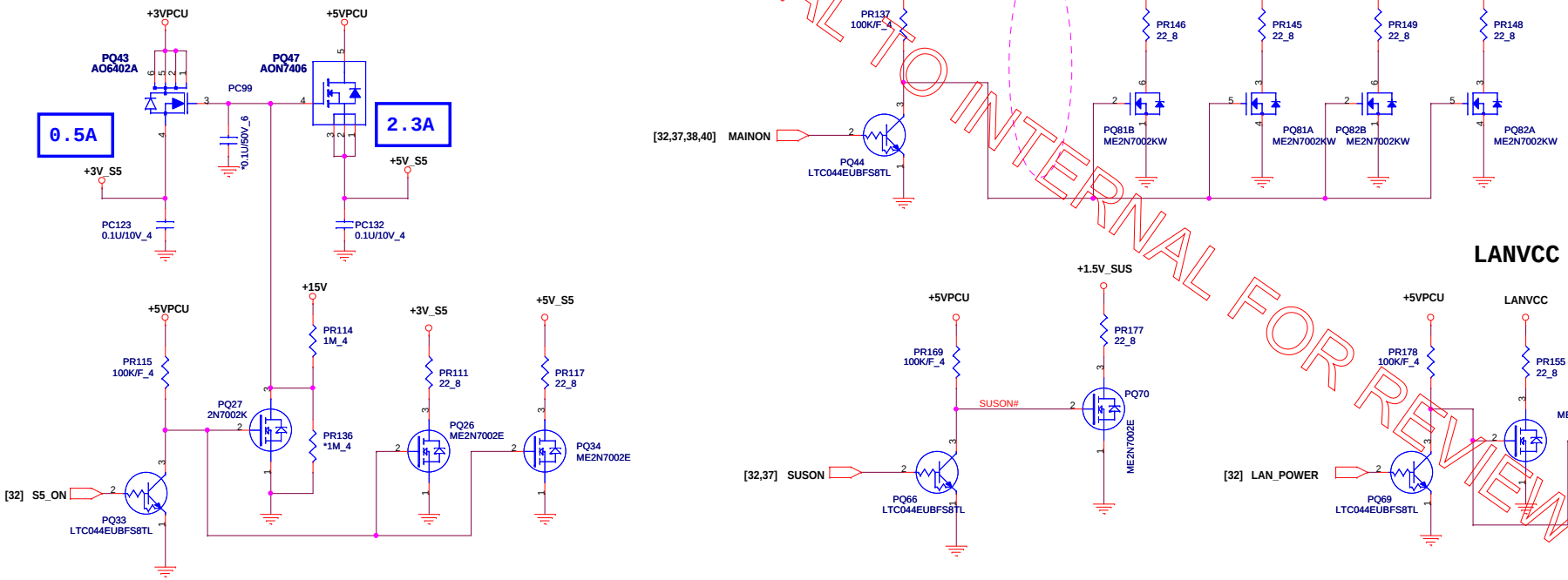
DISCHARGE

+3V, +5V



3V_S5, 5V_S5



PROJECT : LZ2A		
Quanta Computer Inc.		
Size	Document Number: Discharge	Rev
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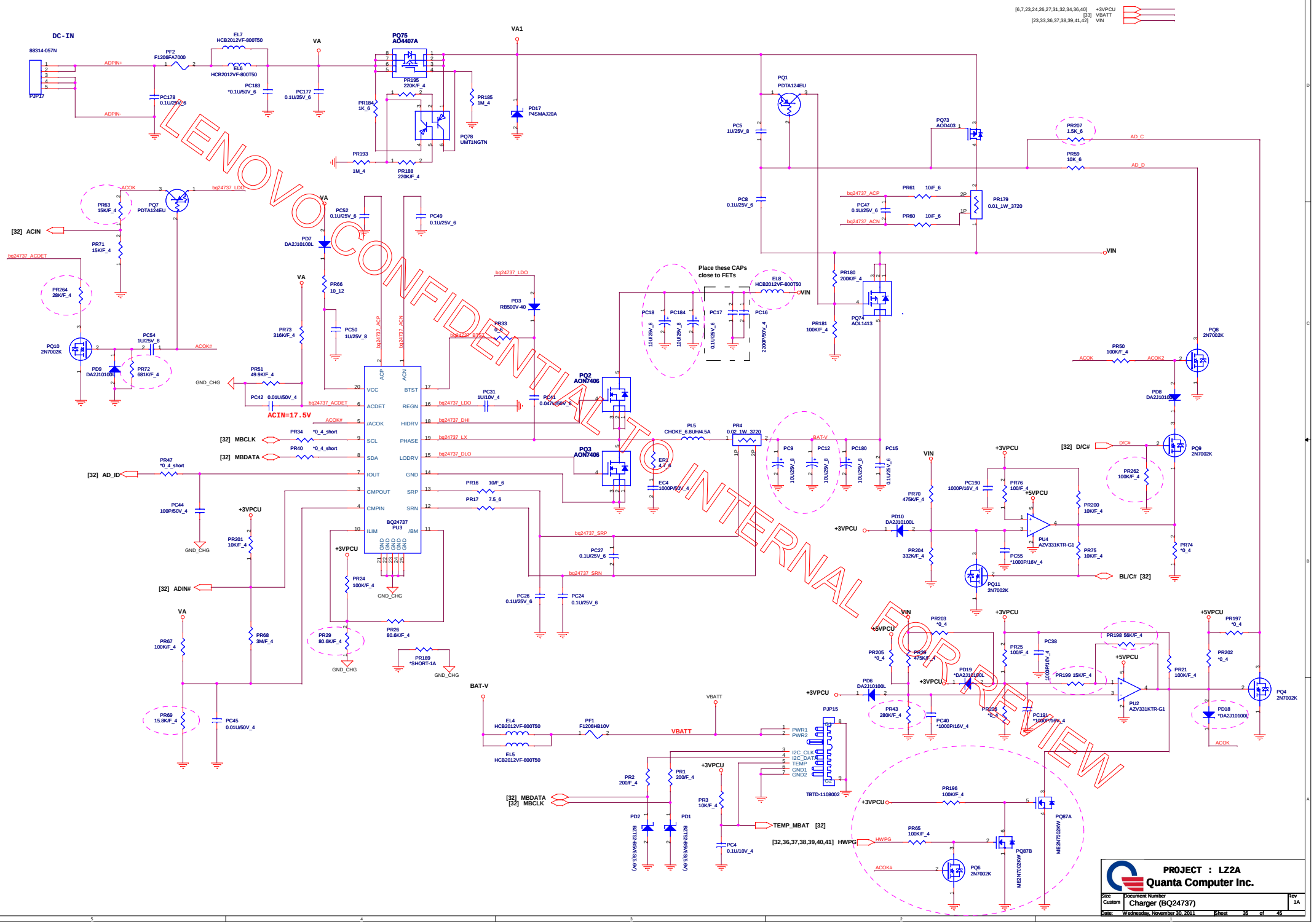

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (BQ24737)	1A
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[23,33,35,37,38,39,41,42] VIN
5V_AL
3V_AL
REF
[10,34,35,37,38,39,40,41,42,43] +5VPCU
[23,26,30,34,43] +15V
[6,7,23,24,26,27,31,32,34,35,40] +3VPCU

+5VPCU
Fs=400K
TDC :6A
Imax :8A
OCP :10A

+3VPCU
Fs=500K
TDC :6A
Imax :8A
OCP :10A

Place these CAPs close to FETs

PQ52 AON7406
PQ51 AON7702
PQ53 AON7406
PQ54 AON7702

PU9 TPS51123ARGER

PL11 2.2UH-PCMC063T-2R2MN
PL10 2.2UH-PCMC063T-2R2MN

HWPG [32,35,37,38,39,40,41]

[29,41] SYS_SHDN#

PROJECT : LZ2A
Quanta Computer Inc.

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	3V/5V (TPS51123ARGER)	

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[12,13,34] +0.75V_DDR_VTT
[23,33,35,36,38,39,41,42] VIN
[2,4,10,12,13,33,34,43] +1.5V_SUS

+0.75V_DDR_VTT
TDC : 1A

+1.5V_SUS
Fs=300K
TDC :16A
Imax :19A
OCP :22A

Place these CAPs close to FETs

VIN

+0.75V_DDR_VTT

PC165 *0.1U/10V_4
PC163 10U/6.3V_6
PC164 10U/6.3V_6

+1.5V_SUS

PC159 10U/6.3V_6

PR165 100K/F_4

PQ68 SK850305KL

PC173 0.1U/25V_6
PC162 2200P/50V_4
PC153 10U/25V_8
PC158 10U/25V_8

PR157 2.2_6
PC161 0.1U/25V_6

DDR_VBST
DRVH
DDR_LL
DRVL
DDR_V5IN

PL2 1.0uH/PCMC104T-1R0MN

+1.5V_SUS

PQ67 SK8603020L

ER9 *4.7_6
EC17 *1000P/50V_4

PC168 330U/2.5V/ELEC_6344
PC167 DIS@330U/2.5V/ELEC_6344
PC148 *330U/2V/ESR9_7343
PC171 10U/6.3V_6
PC172 0.1U/10V_4

R1
PR151 10K/F_4
R2
PR150 53.6K/F_4

PC150 0.1U/10V_4
PC149 0.01U/50V_4

DDR_REFIN
DDR_VDDQS
DDR_VTTREF_R

[4,12,13] SMDDR_VREF

PR153 0_4
PC154 0.22U/10V_4

PR152 *0.6_short
PC156 1U/10V_4

+5VPCU

PU6 TPS51216

VTTGND
VTTSNS
GND
MODE
VREF
VTT
VLDOIN
VBST
DRVH
LL
DRVL
PGND
V5IN
PGOOD
S3
S5
TRIP

DDR_VREF
DDR_REFIN
DDR_VDDQS
DDR_VTTREF_R
DDR_TRIP

PR167 10K/F_4

+3V

Vo=1.8*R2/(R1+R2)

[32] EC_SLP_S4#
[32,34,38,40] MAINON

PR143 *0_4
EC_SLP_S4#
PR163 100K_4
S3
PD16 DA2J10100L
PC170 0.1U/10V_4

PR166 *0_4_short
PD15 RB500V-40
PD14 RB500V-40

HWPG [32,35,36,38,39,40,41]
DRAMPWRGD [32]

PR164 71.5K/F_4

[32,34] SUSON

PR162 0_4
PR144 *0_4
EC_SLP_S4#
S5
PC169 *0.1U/10V_4

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Quanta Computer Inc.

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	DDR3/0.75V (TPS51216)	

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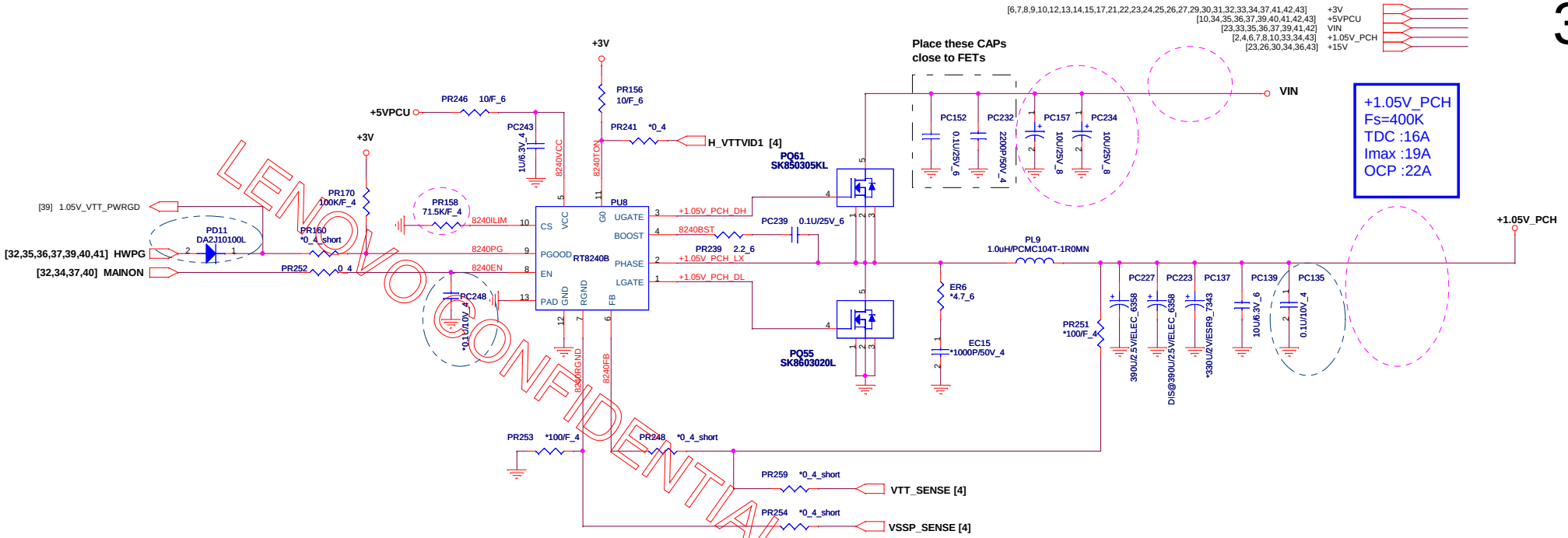

PROJECT : LZ2A		
Quanta Computer Inc.		
Size	Document Number: +1.05V_PCH	Rev
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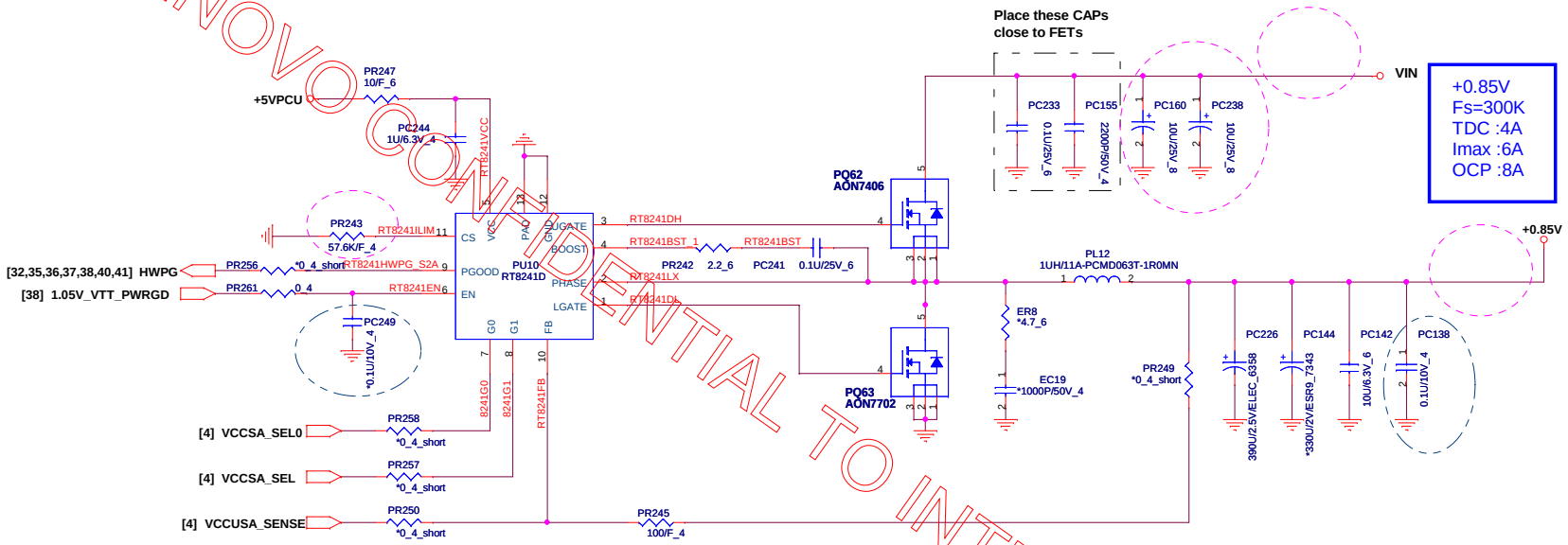
[10,34,35,36,37,38,40,41,42,43] +5VPCU
[23,33,35,36,37,38,41,42] VIN
[4,33,34] +0.85V



G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	VCCSA (RT8241A)	

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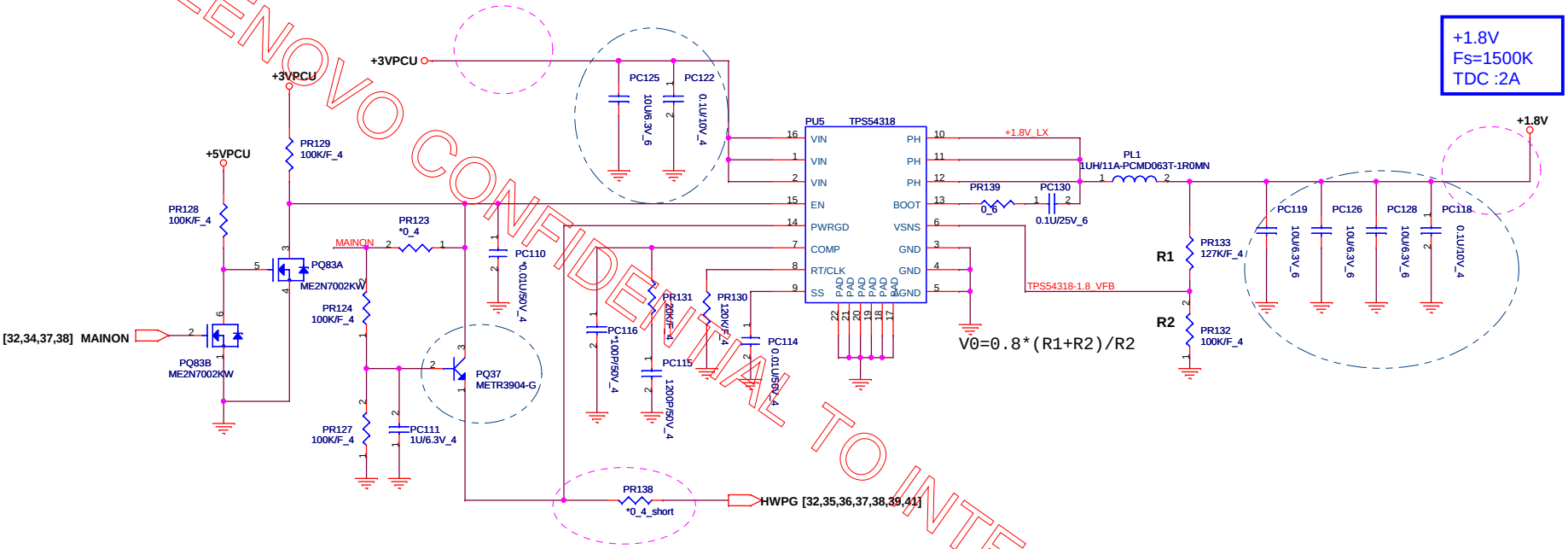
[10,34,35,36,37,38,39,41,42,43] +5VPCU
[6,7,23,24,26,27,31,32,34,35,36] +3VPCU
[4,7,10,33,34] +1.8V

+1.8V
Fs=1500K
TDC :2A



PROJECT : LZ2A
Quanta Computer Inc.

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	1.8V (TPS54318)	

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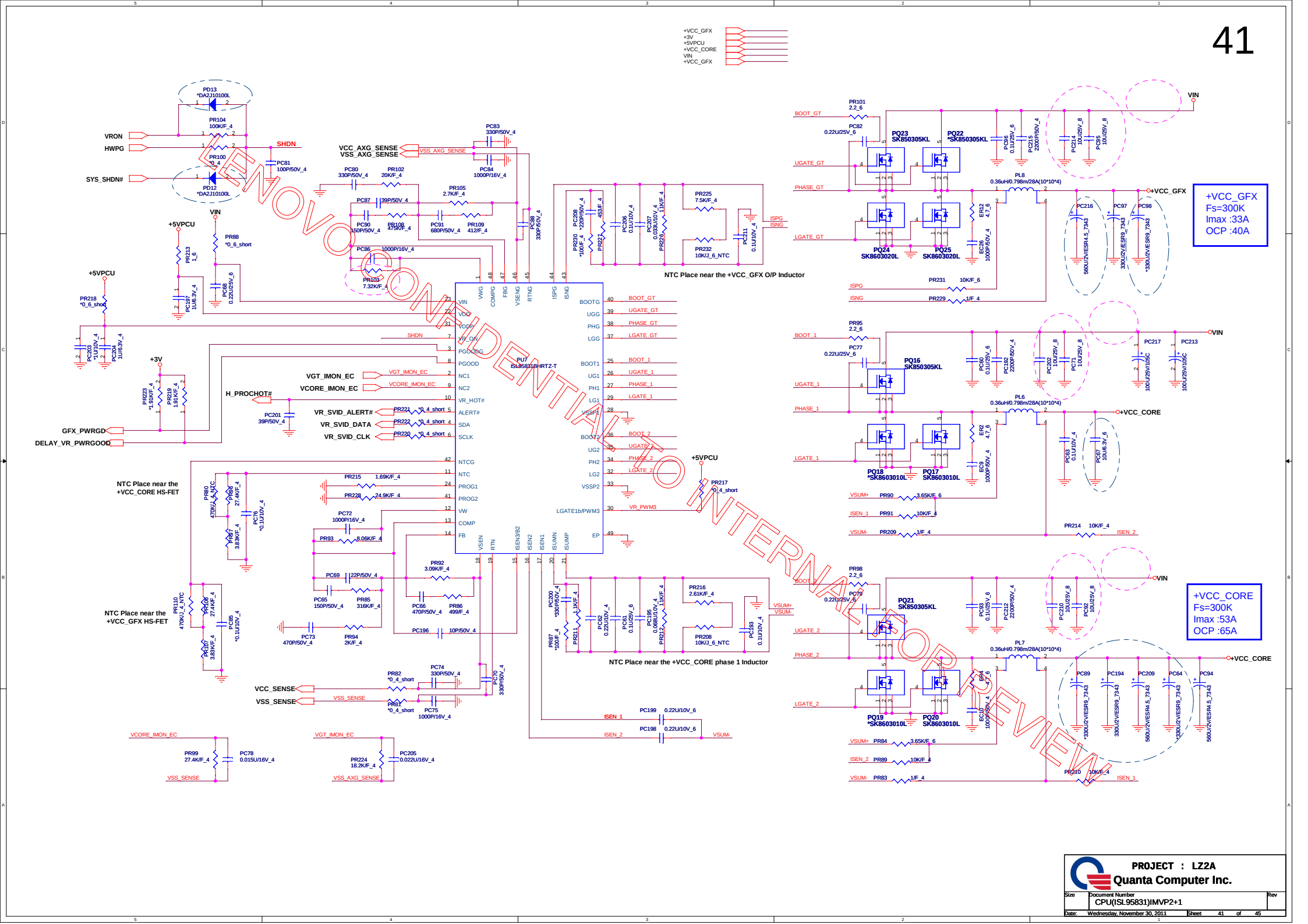

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	CPU(ISL95831)IMVP2+1	

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[4,33,41] +VCC_GFX
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,43] +3V
[10,34,35,36,37,38,39,40,41,43] +5VPCU
[4,33,41] +VCC_CORE
[23,33,35,36,37,38,39,41] VIN
[4,33,41] +VCC_GFX

Place these CAPs close to FETs

VIN

PC13 0.1U/25V_6
PC181 220P/50V_4
PC11 10U/25V_8
PC179 10U/25V_8

PQ76 SK850305KL

PQ77 SK8603020L

ER11 4.7_6
EC24 1000P/50V_4

PL4 0.36UH/24A-PCME064T-R36MS(7*7*4)

GFX_CORE

PC182 *330U/2V/ESR9_7343
PC14 330U/2V/ESR9_7343
PC7 *10U/6.3V_6
PC3 0.1U/10V_4

PR58 *0_4_short
PR64 *0_4_short

[8,15,43] GFXON
PD5 DA2J10100L
PR35 150K/F_4
PC29 0.1U/10V_4
GPU_SHDN

+5VPCU
PR15 10/F_6
PC25 0.22U/25V_6
PR13 2.2_6
VIN
+3V
PR32 1.91K/F_4
NVVDD_PG [43]

PU1 ISL62882C

PC28 1U/6.3V_4

PAD
VDD
VIN
CLK_EN#
PGOOD

+3V
PR27 2.2K_4
PR28 47K/F_4
PSI#
RBIAS
VR_TT#
NTC

[17] GPU_VID0 PR7 *0_4_short
[17] GPU_VID1 PR9 *0_4_short
[17] GPU_VID2 PR11 *0_4_short
[17] GPU_VID3 PR12 *0_4_short
[17] GPU_VID4 PR14 *0_4_short
[17] GPU_VID5 PR18 *0_4_short
GPU_VID6 PR19 *0_4_short
VID0
VID1
VID2
VID3
VID4
VID5
VID6
GPU_SHDN
PR22 1K/F_4
PR23 2.2K_4
VR_ON
DPRSLPVR
[17] DPRSLPVR

FB
FB2
COMP
VW

PR46 *60.4K/F_4
PR41 324K/F_4
PC34 22P/50V_4
PR187 *10K/F_4@NC
PC35 22P/50V_4
PC188 150P/50V_4
PR38 8.06K/F_4
PC33 1000P/16V_4

PR192 2.49K/F_4
PR190 536/F_4
PC189 390P/50V_4

VSEN
RTN
ISUM-
ISUM+

UGATE1
BOOT1
PHASE1
LGATE1a
LGATE1b
VSSP1
ISEN1

62882_UG1
PR8 2.2_6
PC23 0.22U/25V_6
62882_LX1
62882_LG1a
PR54 *10K/F_4@NC
62882_ISE1
PC37 0.22U/10V_4
62882_VSUM-

VCCP
PR5 *0_4_short
+5VPCU
PC21 1U/6.3V_4
PC20 1U/6.3V_4
62882_UG2

UGATE2
BOOT2
PR6 2.2_6
PC22 0.22U/25V_6
PHASE2
LGATE2
VSSP2
ISEN2
62882_LX2
62882_LG2
62882_ISE2
PC36 0.22U/10V_4
GPU_VSUM-

IMON
PR10 1K/F_4
+5VPCU

If IMON PULL HIGH, THEN DISABLE LOAD LINE

Place these CAPs close to FETs

VIN

PC1 0.1U/25V_6
PC175 2200P/50V_4
PC6 10U/25V_8
PC176 10U/25V_8

PQ72 SK850305KL

PQ71 SK8603020L

ER10 4.7_6
EC23 1000P/50V_4

PL3 0.36UH/24A-PCME064T-R36MS(7*7*4)

GFX_CORE

PC19 330U/2V/ESR9_7343
PC185 330U/2V/ESR9_7343
PC10 *10U/6.3V_6
PC2 0.1U/10V_4

PR45 *0_4_short
PR53 *0_4_short

PR55 10K/F_4
GPU_VSUM+ PR49 3.65K/F_4
GPU_VSUM- PR48 1/F_6

PR37 10K/F_4
GPU_VSUM+ PR30 3.65K/F_4
GPU_VSUM- PR62 1/F_6
PR56 *10K/F_4@NC

GFX_CORE
Fs=300K
TDC : 30A
Imax : 40A
OCP : 50A

Place PR331,PC313 close to PIN14 & PIN15

GFX_CORE
PR42 *10_4@NC
VCCSENSE_R
PR52 *0_4_short
[14] GPU_VCCSENSE
[14] GPU_VSSSENSE
Parallel
PR57 *0_4_short
PR194 *10_4@NC
PC46 330P/50V_4
PC48 330P/50V_4
PC51 1000P/16V_4
VSSSENSE_R

GPU_VSUM+
PR20 *82.5/F_4
PC30 *0.01U/50V_4
PC39 0.1U/16V_4
PC32 0.1U/16V_4
PR36 11K/F_4
PR186 2.61K/F_4
PR182 10K/J_6_NTC
Panasonic ERT-J1VR103J
GPU_VSUM-
PC187 0.1U/16V_4
Close to Phase 1 Inductor

PR44 1.47K/F_4
PC43 *1000P/50V_4
PR191 *100/F_4@NC
OCP

PR183 *SHORT-1A@NC

	PR44	PC14	OCP
N13P-GS N13P-GL	CS21472FB21(1.47K)	Stuff	TDC : 30A Imax : 40A OCP : 50A
N13M-GE1	CS21272FB15(1.27K)	Unstuff	TDC : 20A Imax : 25A OCP : 30A

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Quanta Computer Inc.
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[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42] +3V
[14,16,17,18] +3V_GPU
[10,34,35,36,37,38,39,40,41,42] +5VPCU
[14,15,19,20,33] +1.5V_GPU
[23,26,30,34,36] +15V
[2,4,10,12,13,33,34,37] +1.5V_SUS
[14,15,16,33] +1.05V_GFX_PCIE
[2,4,6,7,8,10,33,34,38] +1.05V_PCH

+3V_GPU
+3V
R109 EV@10K/F_4
R141 EV@10K/F_4
GFXPG
GFXPG [9,14]
Q16 METR3904-G
+1.5V_GPU
R120 EV@10K/F_4
*EV@1000P/50V_4@NC C147
Q18 METR3904-G
+1.05V_GFX_PCIE
R107 EV@10K/F_4
*EV@1000P/50V_4@NC C139
Q17 METR3904-G

5.5A
+1.5V_SUS
PQ40 DIS@SK8603020L
+1.5V_GPU
PC112 DIS@10U/6.3V_6
PC117 DIS@10U/6.3V_6
PC107 DIS@10U/6.3V_6
PC106 DIS@10U/6.3V_6
PC101 *330U/2.5V/9m_3528
PC102 *0.1U/10V_4
PR79 DIS@22_8
PR77 DIS@1M_4
+5VPCU
PQ85A ME2N7002KW
PR78 DIS@100K/F_4
PQ85B ME2N7002KW
PC100 DIS@0.022U/25V/X7R_4
[15] +1.5V_GPU_EN
PQ14 DIS@ME2N7002E
R688 100K_4

1.4A
+3V_GPU
PQ15 DIS@AO6402A
+3V_GPU [14,16,17,18]
PC59 DIS@10U/6.3V_6
PC57 DIS@10U/6.3V_6
PC58 *0.1U/10V_4
+15V
PR125 DIS@1M_4
PR113 DIS@22_8
PQ28 DIS@ME2N7002E
+5VPCU
PR118 DIS@100K/F_4
PQ84A 2N7002DW
PC56 *2200P/50V_4
[8,15,42] GFXON
GFXON
PQ84B 2N7002DW
+3V_NVMISC_EN [17,18]

3.9A
+1.05V_PCH
PQ41 DIS@AON7406
+1.05V_GFX_PCIE
PC121 DIS@10U/6.3V_6
PC127 DIS@10U/6.3V_6
PC104 DIS@10U/6.3V_6
PC105 DIS@10U/6.3V_6
PC108 *330U/2.5V/9m_3528
PC113 *DIS@0.1U/10V_4
PR116 DIS@22_8
PR265 DIS@1M_4
+5VPCU
PR266 DIS@100K/F_4
PQ32 DIS@ME2N7002E
PQ86A ME2N7002KW
PC109 *0.022U/25V_4
[42] NVVDD_PG
NVVDD_PG
PQ86B ME2N7002KW

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Quanta Computer Inc.
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LZ2 / Z480 Chief River Schematic EC Tracking Record B (for SDV --> SIV,B)OCT. 07, 2011

EC #	Page	CMVC #	Description	Date	Part Affected
B-00	15		To change D3 pin 2's connection from NVVDD_PG to GFXON for Deep_S3.	0921	
B-01	43		Add PR122 and D26 for +1.05V_GFX_PCIE discharge.	0921	
B-02	17		To change D5 pin1's connection from ACIN to AC_PRESENT for GPU Enable.	0922	
B-03	37		Change PR163 from 0R to 100K form Deep_S3	0922	
B-04	37		Add PD16 1SS355 for Deep_S3	0922	
B-05	32		Add Net EC_DRAMRST_GATE to connect U10's pin 106 and R614.	0925	
B-06	6		Add R615, Q55, Q56, D28 , D29 and Net DPWROK for Deep_S3.	0925	
B-07	10		Add Q57, Q58 and Net SLP_SUS# for Deep_S3.	0925	
B-08	32		Change U10 pin 76's net name from AB_CHARGING to SLP_SUS# for Deep_S3.	0925	
B-09	32		Change U10 pin 83's net name from RF_SW# to PCIE_WAKE#for Deep_S3.	0925	
B-10	32		Change U10 pin 100's connection from PCH to Net GFXON for Deep_S3.	1005	

LZ2 / Z480 Chief River Schematic EC Tracking Record C (for SDV --> SIV,C)Nov. 27, 2011

EC #	Page	CMVC #	Description	Date	Part Affected
C-00	24		Change LAN trandformer from dual mode to signal mode.	1126	
C-01	24		Change R295 and R296 to 0R.	1126	
C-02	24		Add D30,D31,D32,D33 for surge.	1126	
C-03	30		Net "CCD ON#" change connection from EC to PCH.	1120	
C-04	30		Change Bluetooth connection from USB PORT 5 to USB PORT 11 of PCH.	1118	
C-05	23		Add R635,636 fro brightness control.	1126	
C-06					
C-07					
C-08					
C-09					
C-10					

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	EC Tracking Record	

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