LCFC Confidential

AMD 2 Chip M/B Schematics Document

AMD Kaveri Processor with DDR3L + Bolton FCH

AMD GPU JET PRO/TOPAZ XT S3

2013-09-25

REV:0.1

Security Classification	LC Future Center Secret Data		
Issued Date	2013/05/17	Deciphered Date	2012/12/21

Title: Cover Page

Size: Custom | Document Number: ACLU7 | Rev: 0.1

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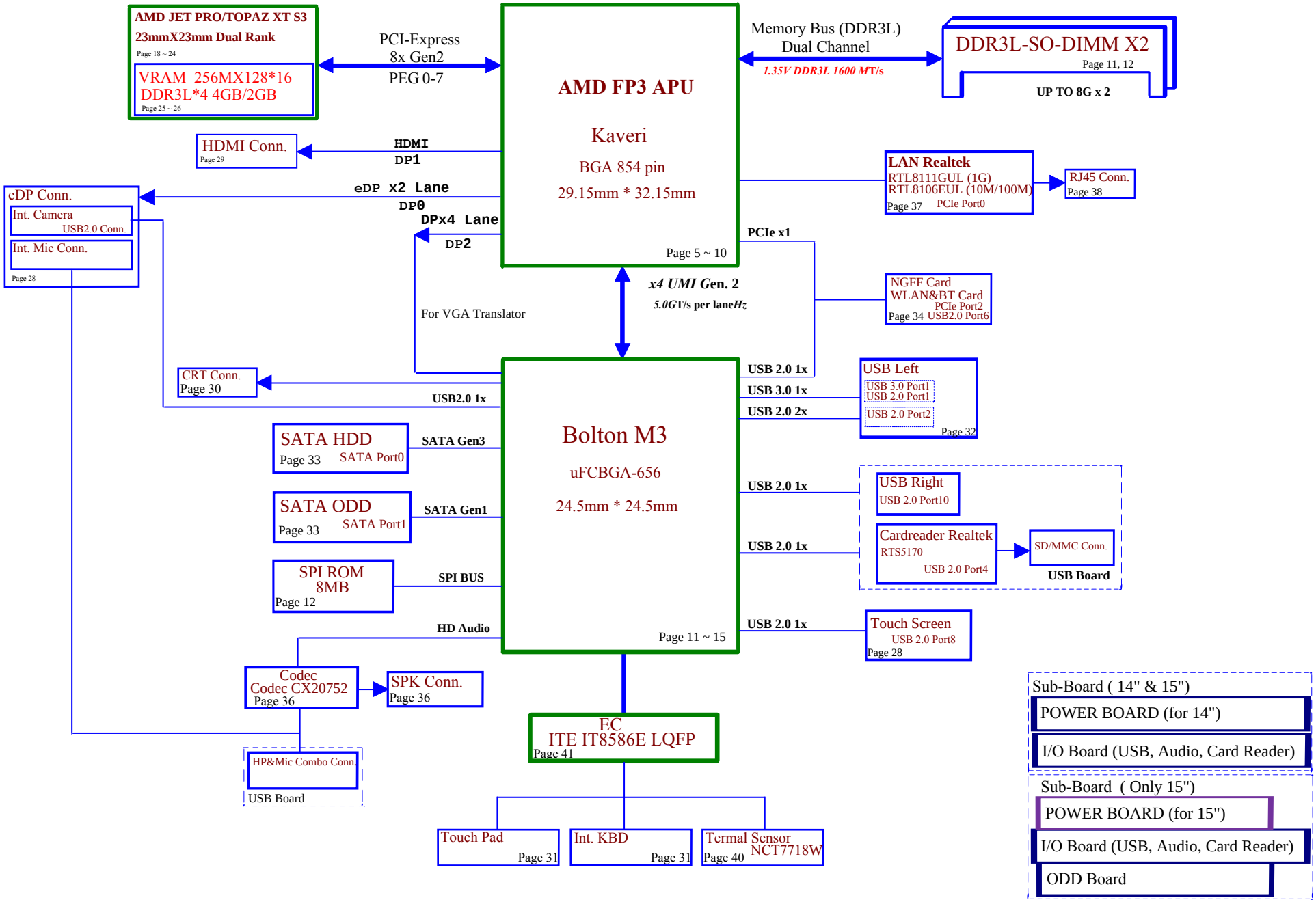
LCFC confidential **File Name: ACLU7 & 8**



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Title: **Block Diagram**

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Voltage Rails (O --> Means ON , X --> Means OFF)

power plane / State	B+	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +1.5s_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
EHCI1	xHCI	1	0 Camera
		2	1 USB Port (Right Side)
		3	2 USB Port (Left Side)
		4	3
			4
			5 USB Port (Right Side)
			6
			7
EHCI2			8
			9
			10 Mini Card (WLAN)
			11
			12
			13 Blue Tooth

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
100M@	100M LAN part
14@	For 14" part
15@	For 15" part
AOAC@	AOAC support part
GIGA@	Giga LAN Part
JET@	For AMD Jet GPU part
ME@	ME Part (connector, hole)
DIS@	Discrete GPU SKU part
UMA@	UMA SKU part
TS@	Touch Screen SKU part
TPOAZ@	For AMD Topaz GPU part
A10@	For AMD Kaveri A10 (19W)S IC KAVERI
A4@	For AMD Kaveri A4 (17W)S IC KAVERI
EMC@	EMC componets

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Termal Sensor	PCH	CP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
APU_SCLK APU_SDATA	PCH +3V_PCH	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	
5	
6	
7	
8	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001 101X b
Master VGA	0x9E
Slave VGA	0x9C

APU SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 010Xb

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Title: **Notes List**

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Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

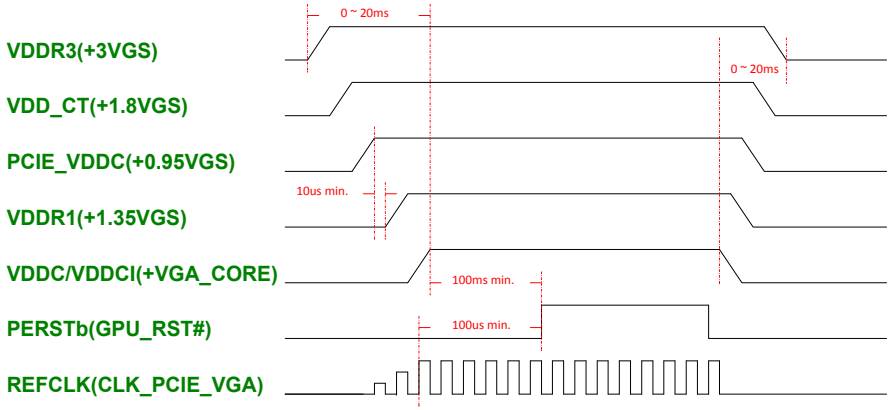
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 µs before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/µs).

For power down, reversing the ramp-up sequence is recommended.



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 100 = 256MB	X
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 0= Not support	X
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	X
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	X
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 000 = Hynix 256M*16 001 = Hynix 128M*16 100 = Samsung 256M*16 011 = Samsung 128M*16 010 = Micron 256M*16 111 = Micron 128M*16	X
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 111= No usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	11

VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV33	PD resistor RV36
128Mx16	Hynix H5TC2G63FFR-11C	100	4.53K	4.99K
	Micron MT41J128M16JT-093G	111	4.75K	NC
	Samsung K4W2G1646Q-BC1A	110	3.4K	10K
256Mx16	Hynix H5TC4G63AFR-11C	000	NC	4.75K
	Micron MT41J256M16HA-093G	010	4.53K	2K
	Samsung K4W4G1646D-BC1A	001	8.45K	2K

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Title: VGA Notes List

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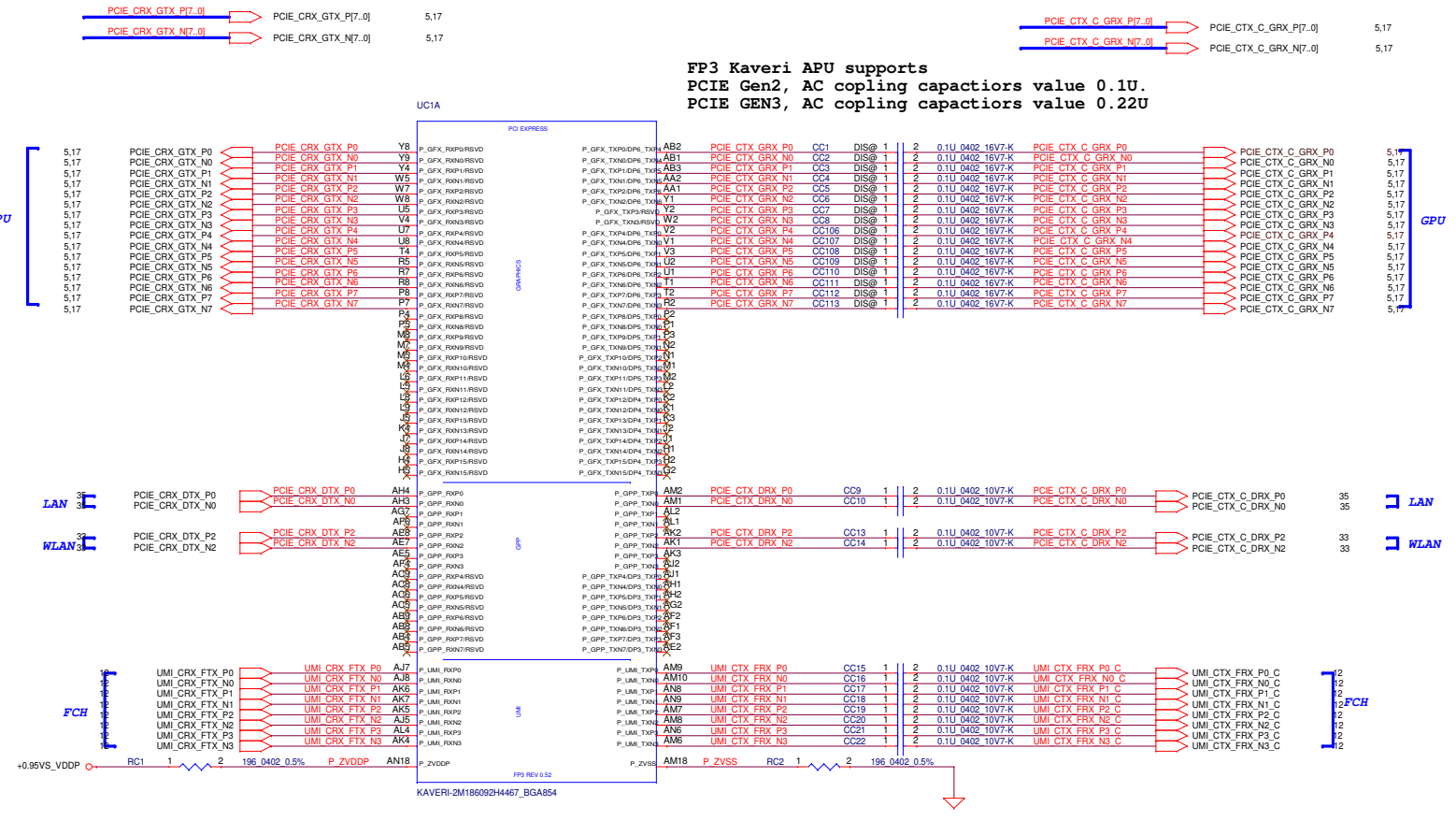

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Title: APU PEG/PCIe/UMI

Size	Document Number	Rev
Custom	ACLU7	0.4

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UC1B

MEMORY CHANNEL A

10 DDRA_MA[0..15]

DDRA_MA0	AB31	MA_ADD0	
DDRA_MA1	U33	MA_ADD1	
DDRA_MA2	U32	MA_ADD2	
DDRA_MA3	R30	MA_ADD3	
DDRA_MA4	T34	MA_ADD4	
DDRA_MA5	R31	MA_ADD5	
DDRA_MA6	R33	MA_ADD6	
DDRA_MA7	P33	MA_ADD7	
DDRA_MA8	P32	MA_ADD8	
DDRA_MA9	P30	MA_ADD9	
DDRA_MA10	AD34	MA_ADD10	
DDRA_MA11	P34	MA_ADD11	
DDRA_MA12	M30	MA_ADD12	
DDRA_MA13	AF33	MA_ADD13	
DDRA_MA14	M31	MA_ADD14	
DDRA_MA15	L32	MA_ADD15	

10 DDRA_BA0#
10 DDRA_BA1#
10 DDRA_BA2#

DDRA_BA0#	AC33	MA_BANK0
DDRA_BA1#	AB30	MA_BANK1
DDRA_BA2#	M34	MA_BANK2

10 DDRA_MA_DM[0..7]

DDRA_MA_DM0	E13	MA_DM0
DDRA_MA_DM1	D18	MA_DM1
DDRA_MA_DM2	H22	MA_DM2
DDRA_MA_DM3	H27	MA_DM3
DDRA_MA_DM4	AG30	MA_DM4
DDRA_MA_DM5	AK26	MA_DM5
DDRA_MA_DM6	AK20	MA_DM6
DDRA_MA_DM7	AF14	MA_DM7
	F34	MA_DM8

10 DDRA_DQS0
10 DDRA_DQS#0
10 DDRA_DQS1
10 DDRA_DQS#1
10 DDRA_DQS2
10 DDRA_DQS#2
10 DDRA_DQS3
10 DDRA_DQS#3
10 DDRA_DQS4
10 DDRA_DQS#4
10 DDRA_DQS5
10 DDRA_DQS#5
10 DDRA_DQS6
10 DDRA_DQS#6
10 DDRA_DQS7
10 DDRA_DQS#7

DDRA_DQS0	F14	MA_DQS_H0
DDRA_DQS#0	G14	MA_DQS_L0
DDRA_DQS1	H19	MA_DQS_H1
DDRA_DQS#1	J19	MA_DQS_L1
DDRA_DQS2	D24	MA_DQS_H2
DDRA_DQS#2	E24	MA_DQS_L2
DDRA_DQS3	F28	MA_DQS_H3
DDRA_DQS#3	E28	MA_DQS_L3
DDRA_DQS4	AJ30	MA_DQS_H4
DDRA_DQS#4	AK30	MA_DQS_L4
DDRA_DQS5	AH24	MA_DQS_H5
DDRA_DQS#5	AG24	MA_DQS_L5
DDRA_DQS6	AG19	MA_DQS_H6
DDRA_DQS#6	AF19	MA_DQS_L6
DDRA_DQS7	AH14	MA_DQS_H7
DDRA_DQS#7	AJ14	MA_DQS_L7
	G31	MA_DQS_H8
	F31	MA_DQS_L8

MB_CLK shift 0 to 1.from 1 to 2

10 DDRA_CLK0
10 DDRA_CLK0#
10 DDRA_CLK1
10 DDRA_CLK1#

DDRA_CLK0	Y30	MA_CLK_H0
DDRA_CLK0#	Y29	MA_CLK_L0
DDRA_CLK1	Y32	MA_CLK_H1
DDRA_CLK1#	Y33	MA_CLK_L1
	W33	MA_CLK_H2
	W34	MA_CLK_L2
	W30	MA_CLK_H3
	W31	MA_CLK_L3

10 DDRA_CKE0
10 DDRA_CKE1

DDRA_CKE0	L33	MA_CKE0
DDRA_CKE1	L30	MA_CKE1
	K34	MA_CKE2
	J30	MA_CKE3

10 DDRA_ODT0
10 DDRA_ODT1

DDRA_ODT0	AH34	MA0_ODT0
DDRA_ODT1	AH33	MA0_ODT1
	AE30	MA1_ODT0
	AJ34	MA1_ODT1

10 DDRA_CS0#
10 DDRA_CS1#

DDRA_CS0#	AE31	MA0_CS_L0
DDRA_CS1#	AG31	MA0_CS_L1
	AC30	MA1_CS_L0
	AF32	MA1_CS_L1

10 DDRA_RAS#
10 DDRA_CAS#
10 DDRA_WE#

DDRA_RAS#	AC32	MA_RAS_L
DDRA_CAS#	AF34	MA_CAS_L
DDRA_WE#	AE33	MA_WE_L

10 DDRA_RESET#
10 DDRA_EVENT#

DDRA_RESET#	J33	MA_RESET_L
DDRA_EVENT#	AB33	MA_EVENT_L
M_VREF	V36	M_VREF
+VREF_DQA	H11	MA_VREFDQ
+1.35V_APU_VDDIO	U30	MA_VZDDIO
	M33	RSVD_3
	AB34	RSVD_4

DDRA_DQ[0..63]

H13	DDRA_DQ0	MA_DATA0
F13	DDRA_DQ1	MA_DATA1
H16	DDRA_DQ2	MA_DATA2
F16	DDRA_DQ3	MA_DATA3
G11	DDRA_DQ4	MA_DATA4
E11	DDRA_DQ5	MA_DATA5
E14	DDRA_DQ6	MA_DATA6
J14	DDRA_DQ7	MA_DATA7
J17	DDRA_DQ8	MA_DATA8
F17	DDRA_DQ9	MA_DATA9
H21	DDRA_DQ10	MA_DATA10
E21	DDRA_DQ11	MA_DATA11
E16	DDRA_DQ12	MA_DATA12
G17	DDRA_DQ13	MA_DATA13
F19	DDRA_DQ14	MA_DATA14
D20	DDRA_DQ15	MA_DATA15
D22	DDRA_DQ16	MA_DATA16
E22	DDRA_DQ17	MA_DATA17
D26	DDRA_DQ18	MA_DATA18
E25	DDRA_DQ19	MA_DATA19
G21	DDRA_DQ20	MA_DATA20
F22	DDRA_DQ21	MA_DATA21
G24	DDRA_DQ22	MA_DATA22
H24	DDRA_DQ23	MA_DATA23
E27	DDRA_DQ24	MA_DATA24
G27	DDRA_DQ25	MA_DATA25
E30	DDRA_DQ26	MA_DATA26
G30	DDRA_DQ27	MA_DATA27
F25	DDRA_DQ28	MA_DATA28
H25	DDRA_DQ29	MA_DATA29
D30	DDRA_DQ30	MA_DATA30
H28	DDRA_DQ31	MA_DATA31
AJ31	DDRA_DQ32	MA_DATA32
AK32	DDRA_DQ33	MA_DATA33
AK28	DDRA_DQ34	MA_DATA34
AF27	DDRA_DQ35	MA_DATA35
AJ33	DDRA_DQ36	MA_DATA36
AK33	DDRA_DQ37	MA_DATA37
AH28	DDRA_DQ38	MA_DATA38
AJ28	DDRA_DQ39	MA_DATA39
AF25	DDRA_DQ40	MA_DATA40
AH25	DDRA_DQ41	MA_DATA41
AG22	DDRA_DQ42	MA_DATA42
AJ22	DDRA_DQ43	MA_DATA43
AH27	DDRA_DQ44	MA_DATA44
AJ27	DDRA_DQ45	MA_DATA45
AE24	DDRA_DQ46	MA_DATA46
AF22	DDRA_DQ47	MA_DATA47
AH21	DDRA_DQ48	MA_DATA48
AJ21	DDRA_DQ49	MA_DATA49
AF17	DDRA_DQ50	MA_DATA50
AJ17	DDRA_DQ51	MA_DATA51
AK22	DDRA_DQ52	MA_DATA52
AF21	DDRA_DQ53	MA_DATA53
AJ19	DDRA_DQ54	MA_DATA54
AE17	DDRA_DQ55	MA_DATA55
AF16	DDRA_DQ56	MA_DATA56
AJ16	DDRA_DQ57	MA_DATA57
AF13	DDRA_DQ58	MA_DATA58
AE13	DDRA_DQ59	MA_DATA59
AH17	DDRA_DQ60	MA_DATA60
AE16	DDRA_DQ61	MA_DATA61
AJ13	DDRA_DQ62	MA_DATA62
AG13	DDRA_DQ63	MA_DATA63
E33		MA_CHECK0
C33		MA_CHECK1
D31		MA_CHECK2
D32		MA_CHECK3
C34		MA_CHECK4
C33		MA_CHECK5
D34		MA_CHECK6
E19		RSVD_5
D28		RSVD_6
AK24		RSVD_7
AG16		RSVD_8

FP3 REV 0.52

KAVERI-2M186092H4467_BGA854

+1.35V_APU_VDDIO
RC5 1K_0402_1%
RC6 1K_0402_1%
100P_0402_50V7K
CC117
0.1U_0402_10V7-K
CC116
+VREF_DQA
RC21 0_0402_5%
+VREF_DQA_C
+1.35V_APU_VDDIO
RC4 39.2_0402_1%
MA_ZVDDIO
M_VREF

add cap on 20131002

UC1C

MEMORY CHANNEL B

10 11 DDRB_MA[0..15]

DDRB_MA0	AC36	MB_ADD0
DDRB_MA1	U36	MB_ADD1
DDRB_MA2	U37	MB_ADD2
DDRB_MA3	T35	MB_ADD3
DDRB_MA4	T37	MB_ADD4
DDRB_MA5	T36	MB_ADD5
DDRB_MA6	R36	MB_ADD6
DDRB_MA7	P37	MB_ADD7
DDRB_MA8	P36	MB_ADD8
DDRB_MA9	N36	MB_ADD9
DDRB_MA10	AD36	MB_ADD10
DDRB_MA11	P35	MB_ADD11
DDRB_MA12	N37	MB_ADD12
DDRB_MA13	AH37	MB_ADD13
DDRB_MA14	M36	MB_ADD14
DDRB_MA15	L36	MB_ADD15

11 DDRB_BA0#
11 DDRB_BA1#
11 DDRB_BA2#

DDRB_BA0#	AD35	MB_BANK0
DDRB_BA1#	AD37	MB_BANK1
DDRB_BA2#	M37	MB_BANK2

11 DDRB_MB_DM[0..7]

DDRB_MB_DM0	A20	MB_DM0
DDRB_MB_DM1	C24	MB_DM1
DDRB_MB_DM2	A30	MB_DM2
DDRB_MB_DM3	B35	MB_DM3
DDRB_MB_DM4	AL35	MB_DM4
DDRB_MB_DM5	AN32	MB_DM5
DDRB_MB_DM6	AN26	MB_DM6
DDRB_MB_DM7	AN21	MB_DM7
	E37	MB_DM8

11 DDRB_DQS0
11 DDRB_DQS#0
11 DDRB_DQS1
11 DDRB_DQS#1
11 DDRB_DQS2
11 DDRB_DQS#2
11 DDRB_DQS3
11 DDRB_DQS#3
11 DDRB_DQS4
11 DDRB_DQS#4
11 DDRB_DQS5
11 DDRB_DQS#5
11 DDRB_DQS6
11 DDRB_DQS#6
11 DDRB_DQS7
11 DDRB_DQS#7

DDRB_DQS0	C20	MB_DQS_H0
DDRB_DQS#0	B20	MB_DQS_L0
DDRB_DQS1	B25	MB_DQS_H1
DDRB_DQS#1	A25	MB_DQS_L1
DDRB_DQS2	C30	MB_DQS_H2
DDRB_DQS#2	B30	MB_DQS_L2
DDRB_DQS3	B36	MB_DQS_H3
DDRB_DQS#3	A36	MB_DQS_L3
DDRB_DQS4	AN36	MB_DQS_H4
DDRB_DQS#4	AM36	MB_DQS_L4
DDRB_DQS5	AN31	MB_DQS_H5
DDRB_DQS#5	AM31	MB_DQS_L5
DDRB_DQS6	AM26	MB_DQS_H6
DDRB_DQS#6	AL26	MB_DQS_L6
DDRB_DQS7	AM20	MB_DQS_H7
DDRB_DQS#7	AL20	MB_DQS_L7
	F37	MB_DQS_H8
	F36	MB_DQS_L8

MB_CLK shift 0 to 1.from 1 to 2

11 DDRB_CLK0
11 DDRB_CLK0#
11 DDRB_CLK1
11 DDRB_CLK1#

DDRB_CLK0	AA37	MB_CLK_H0
DDRB_CLK0#	AA36	MB_CLK_L0
DDRB_CLK1	Y37	MB_CLK_H1
DDRB_CLK1#	Y36	MB_CLK_L1
	Y34	MB_CLK_H2
	Y35	MB_CLK_L2
	V35	MB_CLK_H3
	W36	MB_CLK_L3

11 DDRB_CKE0
11 DDRB_CKE1

DDRB_CKE0	K36	MB_CKE0
DDRB_CKE1	K37	MB_CKE1
	K35	MB_CKE2
	J37	MB_CKE3

11 DDRB_ODT0
11 DDRB_ODT1

DDRB_ODT0	AH36	MB0_ODT0
DDRB_ODT1	AJ37	MB0_ODT1
	AF35	MB1_ODT0
	AK35	MB1_ODT1

11 DDRB_CS0#
11 DDRB_CS1#

DDRB_CS0#	AF36	MB0_CS_L0
DDRB_CS1#	AJ36	MB0_CS_L1
	AE36	MB1_CS_L0
	AH35	MB1_CS_L1

11 DDRB_RAS#
11 DDRB_CAS#
11 DDRB_WE#

DDRB_RAS#	AE37	MB_RAS_L
DDRB_CAS#	AG36	MB_CAS_L
DDRB_WE#	AF37	MB_WE_L

11 DDRB_RESET#
11 DDRB_EVENT#

DDRB_RESET#	J36	MB_RESET_L
DDRB_EVENT#	AB36	MB_EVENT_L
+VREF_DQB	B17	MB_VREFDQ
+1.35V_APU_VDDIO	V37	MB_ZVDDIO
	M35	RSVD_9
	AB35	RSVD_10

DDRB_DQ[0..63]

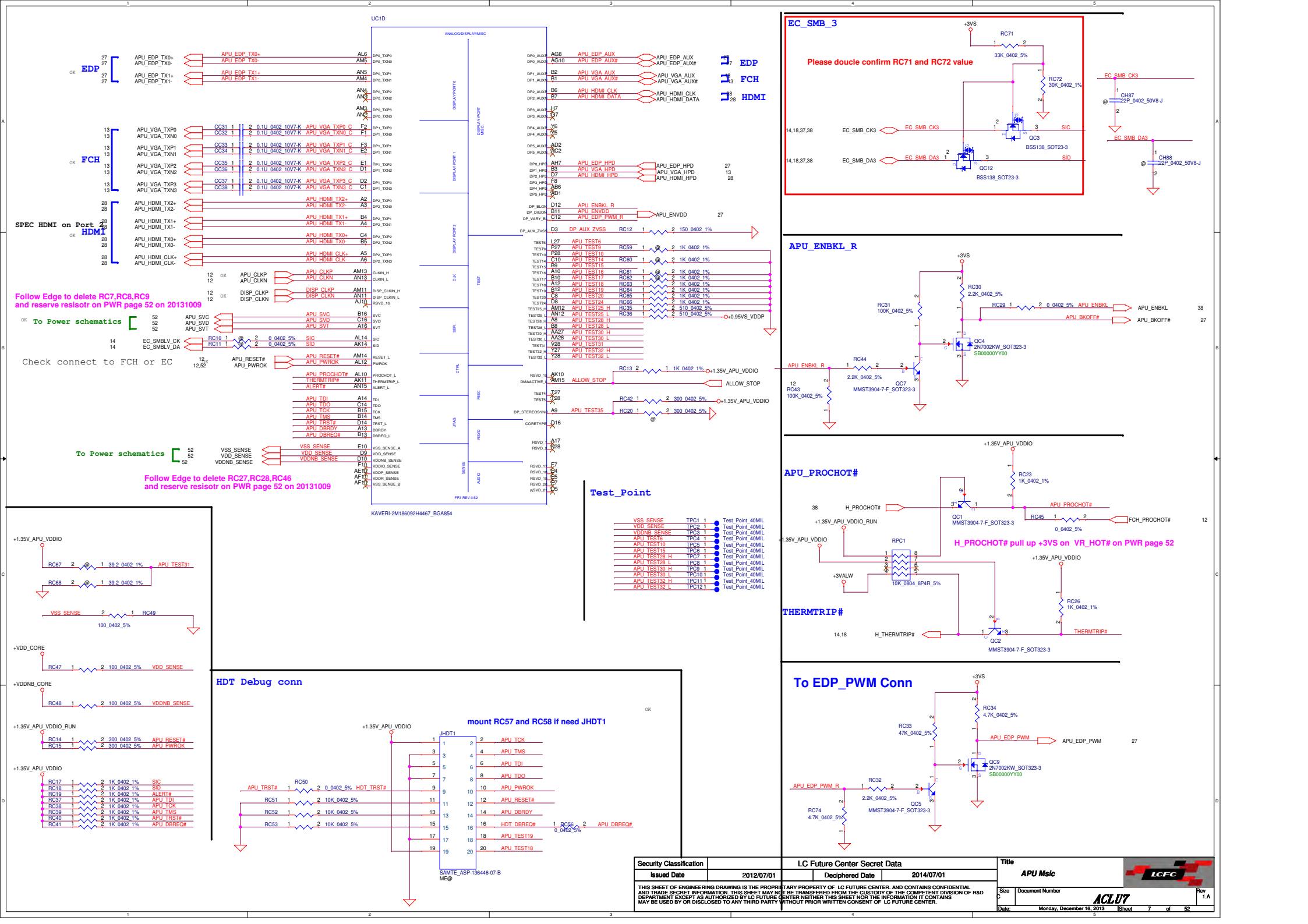
C18	DDRB_DQ0	MB_DATA0
B19	DDRB_DQ1	MB_DATA1
C22	DDRB_DQ2	MB_DATA2
A22	DDRB_DQ3	MB_DATA3
A18	DDRB_DQ4	MB_DATA4
B18	DDRB_DQ5	MB_DATA5
A21	DDRB_DQ6	MB_DATA6
B21	DDRB_DQ7	MB_DATA7
B24	DDRB_DQ8	MB_DATA8
A24	DDRB_DQ9	MB_DATA9
B27	DDRB_DQ10	MB_DATA10
A28	DDRB_DQ11	MB_DATA11
B22	DDRB_DQ12	MB_DATA12
B23	DDRB_DQ13	MB_DATA13
B26	DDRB_DQ14	MB_DATA14
C26	DDRB_DQ15	MB_DATA15
A29	DDRB_DQ16	MB_DATA16
B29	DDRB_DQ17	MB_DATA17
B32	DDRB_DQ18	MB_DATA18
C32	DDRB_DQ19	MB_DATA19
B28	DDRB_DQ20	MB_DATA20
C28	DDRB_DQ21	MB_DATA21
B31	DDRB_DQ22	MB_DATA22
A32	DDRB_DQ23	MB_DATA23
C34	DDRB_DQ24	MB_DATA24
A34	DDRB_DQ25	MB_DATA25
C36	DDRB_DQ26	MB_DATA26
C37	DDRB_DQ27	MB_DATA27
A33	DDRB_DQ28	MB_DATA28
B33	DDRB_DQ29	MB_DATA29
D35	DDRB_DQ30	MB_DATA30
B37	DDRB_DQ31	MB_DATA31
AL36	DDRB_DQ32	MB_DATA32
AM37	DDRB_DQ33	MB_DATA33
AN34	DDRB_DQ34	MB_DATA34
AM34	DDRB_DQ35	MB_DATA35
AK37	DDRB_DQ36	MB_DATA36
AK36	DDRB_DQ37	MB_DATA37
AN35	DDRB_DQ38	MB_DATA38
AL34	DDRB_DQ39	MB_DATA39
AL32	DDRB_DQ40	MB_DATA40
AM32	DDRB_DQ41	MB_DATA41
AN29	DDRB_DQ42	MB_DATA42
AL28	DDRB_DQ43	MB_DATA43
AM33	DDRB_DQ44	MB_DATA44
AN33	DDRB_DQ45	MB_DATA45
AM30	DDRB_DQ46	MB_DATA46
AM29	DDRB_DQ47	MB_DATA47
AM27	DDRB_DQ48	MB_DATA48
AM26	DDRB_DQ49	MB_DATA49
AN24	DDRB_DQ50	MB_DATA50
AM24	DDRB_DQ51	MB_DATA51
AN28	DDRB_DQ52	MB_DATA52
AM28	DDRB_DQ53	MB_DATA53
AN25	DDRB_DQ54	MB_DATA54
AL24	DDRB_DQ55	MB_DATA55
AN22	DDRB_DQ56	MB_DATA56
AL22	DDRB_DQ57	MB_DATA57
AK18	DDRB_DQ58	MB_DATA58
AL18	DDRB_DQ59	MB_DATA59
AM23	DDRB_DQ60	MB_DATA60
AM22	DDRB_DQ61	MB_DATA61
AN20	DDRB_DQ62	MB_DATA62
AM19	DDRB_DQ63	MB_DATA63
E36		MB_CHECK0
C35		MB_CHECK1
D36		MB_CHECK2
D37		MB_CHECK3
C36		MB_CHECK4
D37		MB_CHECK5
C36		MB_CHECK6
B35		MB_CHECK7
A26		RSVD_11
B34		RSVD_12
AL30		RSVD_13
AM21		RSVD_14

FP3 REV 0.52

KAVERI-2M186092H4467_BGA854

+VREF_DQB
+1.35V_APU_VDDIO
RC22 0_0402_5%
RC3 39.2_0402_1%
+VREF_DQB_C
MB_ZVDDIO

Title	APU DDRA/B		
Size	Document Number		Rev
Custom	ACLU7		1.A
Date:	Monday, December 16, 2013	Sheet	6 of 52


EC_SMB_3
Please doucle confirm RC71 and RC72 value
APU_ENBKL_R
APU_PROCHOT#
THERMTRIP#
To EDP_PWM Conn
HDT Debug conn
mount RC57 and RC58 if need JHDT1
Test_Point
EDP
FCH
HDMI
SPEC HDMI on Port 2
Follow Edge to delete RC7,RC8,RC9
and reserve resisotr on PWR page 52 on 20131009
To Power schematics
Check connect to FCH or EC
Follow Edge to delete RC27,RC28,RC46
and reserve resisotr on PWR page 52 on 20131009
H_PROCHOT# pull up +3VS on VR_HOT# on PWR page 52
UC1D
KAVERI-2M186092H4467_BGA854
SAMTE_ASP-136446-07-B
ME@
Security Classification
LC Future Center Secret Data
Issued Date
2012/07/01
Deciphered Date
2014/07/01
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Title
APU Msic
Size
C
Document Number
ACLU7
Rev
1.A
Date:
Monday, December 16, 2013
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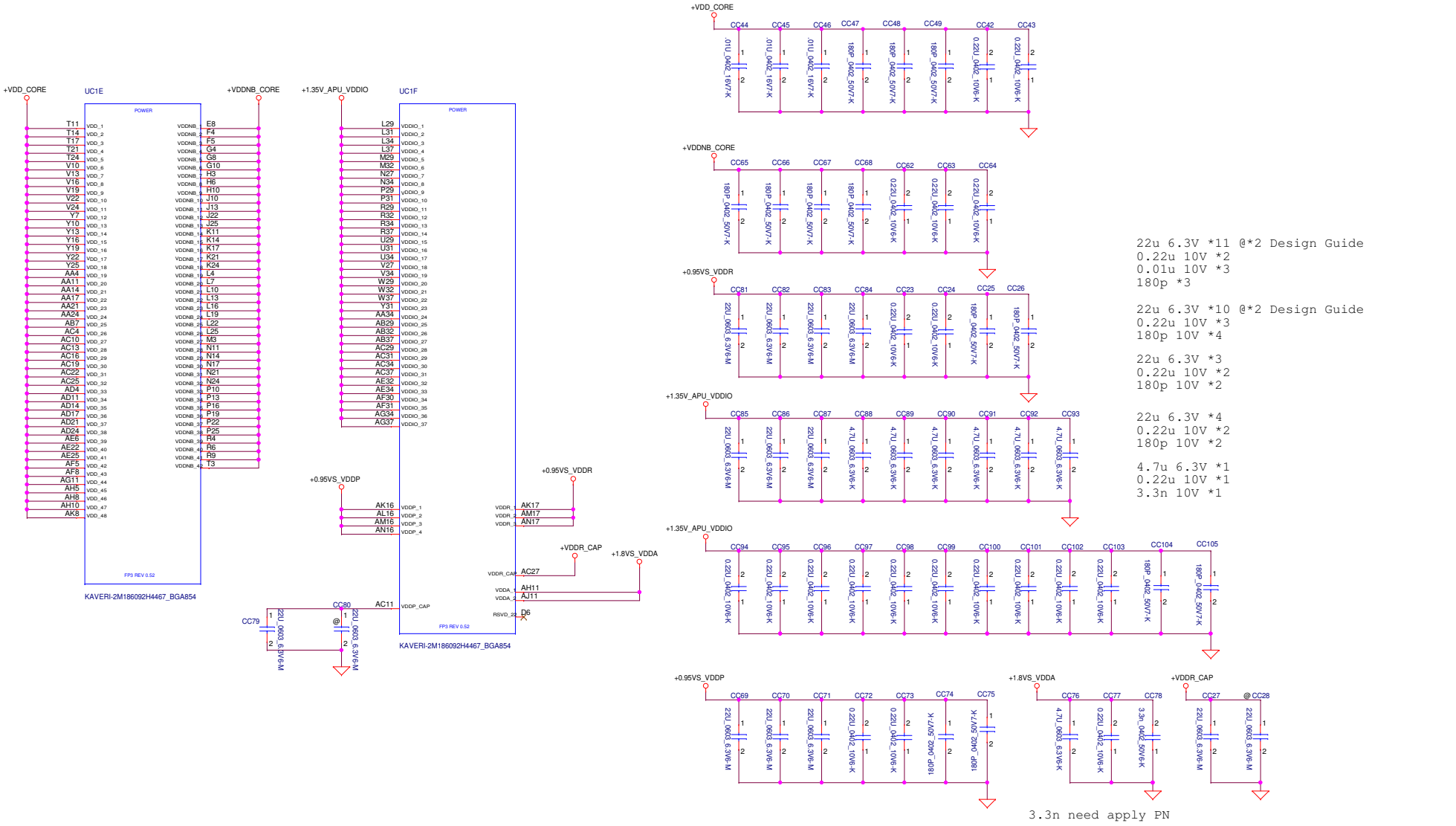
7
of
52



22u 6.3V *11 @*2 Design Guide
0.22u 10V *2
0.01u 10V *3
180p *3

22u 6.3V *10 @*2 Design Guide
0.22u 10V *3
180p 10V *4

22u 6.3V *3
0.22u 10V *2
180p 10V *2

22u 6.3V *4
0.22u 10V *2
180p 10V *2

4.7u 6.3V *1
0.22u 10V *1
3.3n 10V *1

3.3n need apply PN

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: APU Power

Size	Document Number	Rev
Custom	ACLU7	1.A

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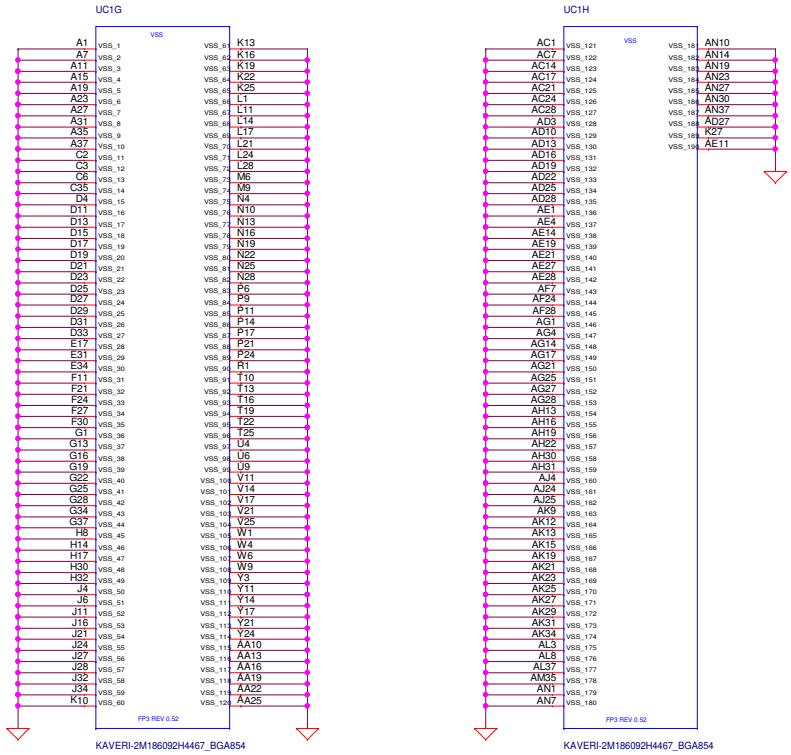

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: APU GND

Size	Document Number	Rev
Custom	ACLU7	1.A

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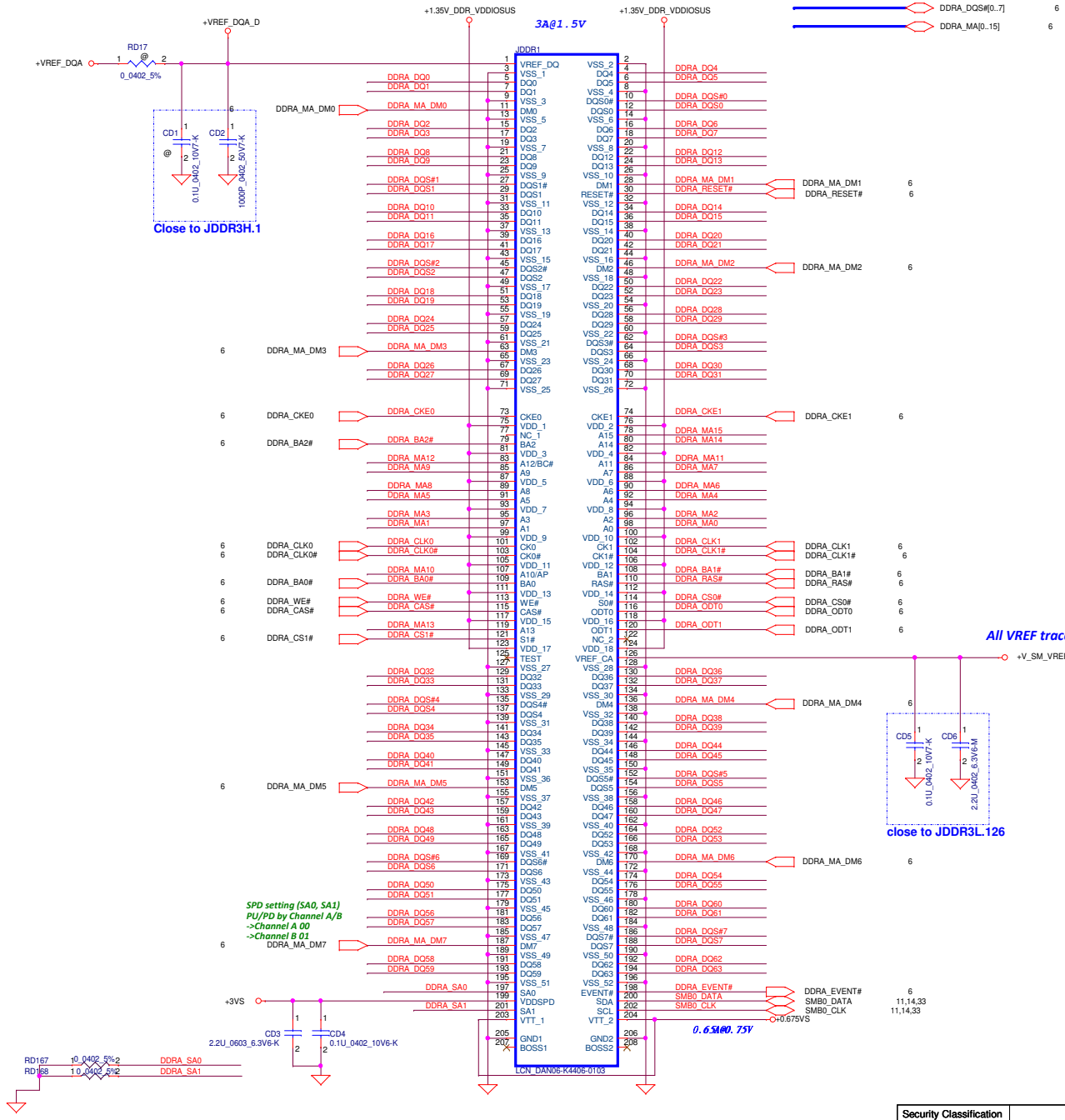
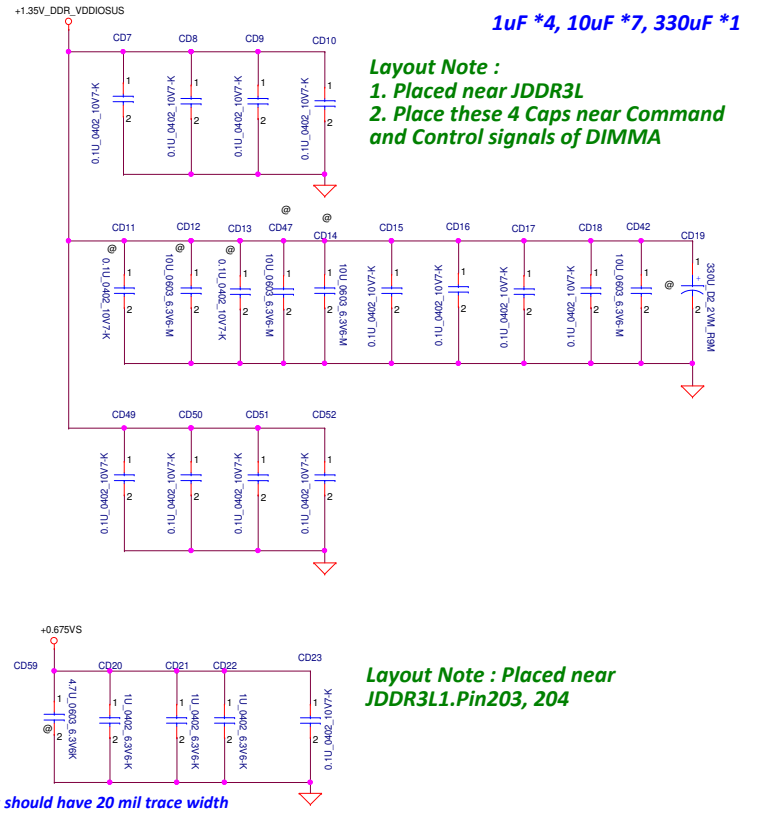
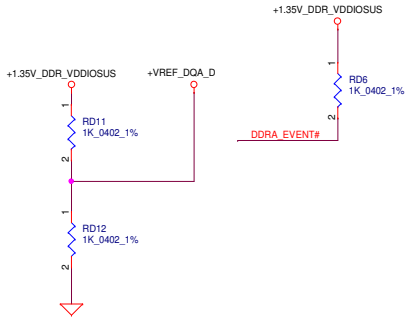
DDR3 SO-DIMM A



DDR Decoupling





Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title	DDR3 SO-DIMMA/1		
Size	Document Number		Rev
Custom	ACLU7		0.4
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DDR3 SO-DIMM B

DDRB_DQ[0..63] 6
DDRB_DQS[0..7] 6
DDRB_DQS#[0..7] 6
DDRB_MA[0..15] 6

+VREF_DQB_D
+VREF_DQB
RD18 @ 0_0402_5%
+1.35V_DDR_VDDIOSUS 3A@1.5V
+1.35V_DDR_VDDIOSUS

JDDR2

		1	VREF_DQ	VSS1	2		
DDRB_DQ0	DDRB_DQ1	3	VSS2	DQ4	4	DDRB_DQ4	DDRB_DQ5
		5	DQ0	DQ5	6		
		7	DQ1	VSS3	8		
		9	VSS4	DQS#0	10	DDRB_DQS#0	
6 DDRB_MB_DM0		11	DM0	DQS0	12	DDRB_DQS0	
DDRB_DQ2	DDRB_DQ3	13	VSS5	VSS6	14		
		15	DQ2	DQ6	16	DDRB_DQ6	DDRB_DQ7
		17	DQ3	DQ7	18		
		19	VSS7	VSS8	20		
DDRB_DQ8	DDRB_DQ9	21	DQ8	DQ12	22	DDRB_DQ12	DDRB_DQ13
		23	DQ9	DQ13	24		
		25	VSS9	VSS10	26		
DDRB_DQS#1	DDRB_DQS1	27	DQS#1	DM1	28	DDRB_MB_DM1	DDRB_MB_DM1 6
		29	DQS1	RESET#	30	DDRB_RESET#	DDRB_RESET# 6
		31	VSS11	VSS12	32		
DDRB_DQ10	DDRB_DQ11	33	DQ10	DQ14	34	DDRB_DQ14	DDRB_DQ15
		35	DQ11	DQ15	36		
		37	VSS13	VSS14	38		
DDRB_DQ16	DDRB_DQ17	39	DQ16	DQ20	40	DDRB_DQ20	DDRB_DQ21
		41	DQ17	DQ21	42		
		43	VSS15	VSS16	44		
DDRB_DQS#2	DDRB_DQS2	45	DQS#2	DM2	46	DDRB_MB_DM2	DDRB_MB_DM2 6
		47	DQS2	VSS17	48		
		49	VSS18	DQ22	50	DDRB_DQ22	DDRB_DQ23
DDRB_DQ18	DDRB_DQ19	51	DQ18	DQ23	52		
		53	DQ19	VSS19	54		
		55	VSS20	DQ28	56	DDRB_DQ28	DDRB_DQ29
DDRB_DQ24	DDRB_DQ25	57	DQ24	DQ29	58		
		59	DQ25	VSS21	60		
		61	VSS22	DQS#3	62	DDRB_DQS#3	
6 DDRB_MB_DM3		63	DM3	DQS3	64	DDRB_DQS3	
		65	VSS23	VSS24	66		
DDRB_DQ26	DDRB_DQ27	67	DQ26	DQ30	68	DDRB_DQ30	DDRB_DQ31
		69	DQ27	DQ31	70		
		71	VSS25	VSS26	72		
6 DDRB_CKE0		73	CKE0	CKE1	74	DDRB_CKE1	DDRB_CKE1 6
		75	VDD1	VDD2	76		
		77	NC1	A15	78	DDRB_MA15	DDRB_MA14
6 DDRB_BA2#		79	BA2	A14	80		
DDRB_MA12	DDRB_MA9	81	VDD3	VDD4	82		
		83	A12/BC#	A11	84	DDRB_MA11	DDRB_MA7
		85	A9	A7	86		
DDRB_MA8	DDRB_MA5	87	VDD5	VDD6	88		
		89	A8	A6	90	DDRB_MA6	DDRB_MA4
		91	A5	A4	92		
		93	VDD7	VDD8	94		
DDRB_MA3	DDRB_MA1	95	A3	A2	96	DDRB_MA2	DDRB_MA0
		97	A1	A0	98		
		99	VDD9	VDD10	100		
6 DDRB_CLK0	DDRB_CLK0# 6	101	CK0	CK1	102	DDRB_CLK1	DDRB_CLK1 6
		103	CK0#	CK1#	104	DDRB_CLK1#	DDRB_CLK1# 6
		105	VDD11	VDD12	106		
DDRB_MA10		107	A10/AP	BA1	108	DDRB_BA1#	DDRB_BA1 6
6 DDRB_BA0#		109	BA0	RAS#	110	DDRB_RAS#	DDRB_RAS 6
		111	VDD13	VDD14	112		
6 DDRB_WE#		113	WE#	S0#	114	DDRB_CS0#	DDRB_CS0 6
6 DDRB_CAS#		115	CAS#	ODT0	116	DDRB_ODT0	DDRB_ODT0 6
		117	VDD15	VDD16	118		
DDRB_MA13		119	A13	ODT1	120	DDRB_ODT1	DDRB_ODT1 6
6 DDRB_CS1#		121	S1#	NC2	122		
		123	VDD17	VDD18	124		
		125	NCTEST	VREF_CA	126		+V_SM_VREF_CNT
		127	VSS27	VSS28	128		
DDRB_DQ32	DDRB_DQ33	129	DQ32	DQ36	130	DDRB_DQ36	DDRB_DQ37
		131	DQ33	DQ37	132		
		133	VSS29	VSS30	134		
DDRB_DQS#4	DDRB_DQS4	135	DQS#4	DM4	136	DDRB_MB_DM4	DDRB_MB_DM4 6
		137	DQS4	VSS31	138		
		139	VSS32	DQ38	140	DDRB_DQ38	DDRB_DQ39
DDRB_DQ34	DDRB_DQ35	141	DQ34	DQ39	142		
		143	DQ35	VSS33	144		
		145	VSS34	DQ44	146	DDRB_DQ44	DDRB_DQ45
DDRB_DQ40	DDRB_DQ41	147	DQ40	DQ45	148		
		149	DQ41	VSS35	150		
		151	VSS36	DQS#5	152	DDRB_DQS#5	
6 DDRB_MB_DM5		153	DM5	DQS5	154	DDRB_DQS5	
		155	VSS37	VSS38	156		
DDRB_DQ42	DDRB_DQ43	157	DQ42	DQ46	158	DDRB_DQ46	DDRB_DQ47
		159	DQ43	DQ47	160		
		161	VSS39	VSS40	162		
DDRB_DQ48	DDRB_DQ49	163	DQ48	DQ52	164	DDRB_DQ52	DDRB_DQ53
		165	DQ49	DQ53	166		
		167	VSS41	VSS42	168		
DDRB_DQS#6	DDRB_DQS6	169	DQS#6	DM6	170	DDRB_MB_DM6	DDRB_MB_DM6 6
		171	DQS6	VSS43	172		
		173	VSS44	DQ54	174	DDRB_DQ54	DDRB_DQ55
DDRB_DQ50	DDRB_DQ51	175	DQ50	DQ55	176		
		177	DQ51	VSS45	178		
		179	VSS46	DQ60	180	DDRB_DQ60	DDRB_DQ61
DDRB_DQ56	DDRB_DQ57	181	DQ56	DQ61	182		
		183	DQ57	VSS47	184		
		185	VSS48	DQS#7	186	DDRB_DQS#7	
6 DDRB_MB_DM7		187	DM7	DQS7	188	DDRB_DQS7	
		189	VSS49	VSS50	190		
DDRB_DQ58	DDRB_DQ59	191	DQ58	DQ62	192	DDRB_DQ62	DDRB_DQ63
		193	DQ59	DQ63	194		
		195	VSS51	VSS52	196		
		197	SA0	EVENT#	198	DDRB_EVENT#	DDRB_EVENT# 6
		199	VDDSPD	SDA	200	SMB0_DATA	SMB0_DATA 10,14,33
		201	SA1	SCL	202	SMB0_CLK	SMB0_CLK 10,14,33
		203	VTT1	VTT2	204		+0.675VS
		205	G1	G2	206		

LCN_DAN06-K4406-0102

0.675@0.75V

CD24 @ 0.1U_0402_10V7-K
CD25 1000P_0402_50V7-K
Close to JDDR3L.1

CD28 6 0.1U_0402_10V7-K
CD29 1000P_0402_50V7-K
Close to JDDR3H.126

SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

+3VS
R167 10K_0402_5%
+3VS
DDRB_SA0
DDRB_SA1
RD170 0_0402_5%
CD26 2.2U_0603_6.3V6-K
CD27 0.1U_0402_10V6-K

CRB: DDRB_SA1 pull low / DDRB_SA0 pull high
Edge: DDRB_SA1 pull high / DDRB_SA0 pull low

DDR Decoupling

+1.35V_DDR_VDDIOSUS

CD30 CD31 CD32 CD33 0.1U_0402_10V7-K

CD34 CD35 CD36 CD54 CD55 CD37 CD38 CD39 CD40 CD41
10U_0603_6.3V6-M, 0.1U_0402_10V7-K

CD62 CD61 CD64 CD63 0.1U_0402_10V7-K

1uF *4, 10uF *7, 330uF *1

Layout Note :
1. Placed near JDDR3H
2. Place these 4 Caps near Command and Control signals of DIMMA

+0.675VS

CD58 @ 4.7U_0603_6.3V6K
CD43 CD44 CD45 CD46 1U_0402_6.3V6-K

Layout Note : Placed near JDDR3H.Pin203, 204

+1.35V_DDR_VDDIOSUS
RD8 1K_0402_1%
DDRB_EVENT#

+1.35V_DDR_VDDIOSUS
+V_SM_VREF_CNT
RD5 1K_0402_1%
RD7 1K_0402_1%

+1.35V_DDR_VDDIOSUS
+VREF_DQB_D
RD9 1K_0402_1%
RD10 1K_0402_1%

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title	DDR3 SO-DIMMB/2		
Size	Document Number		Rev
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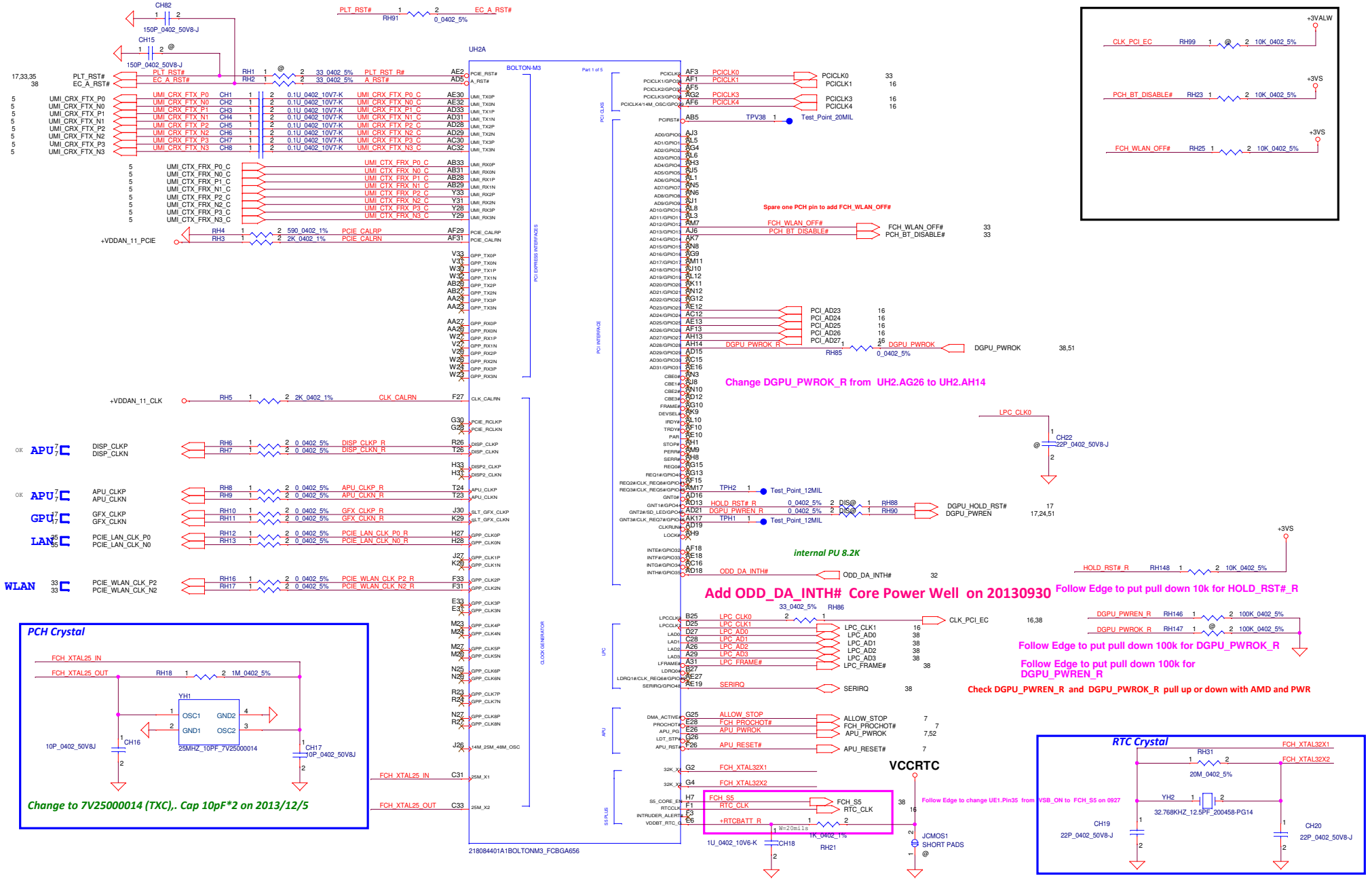
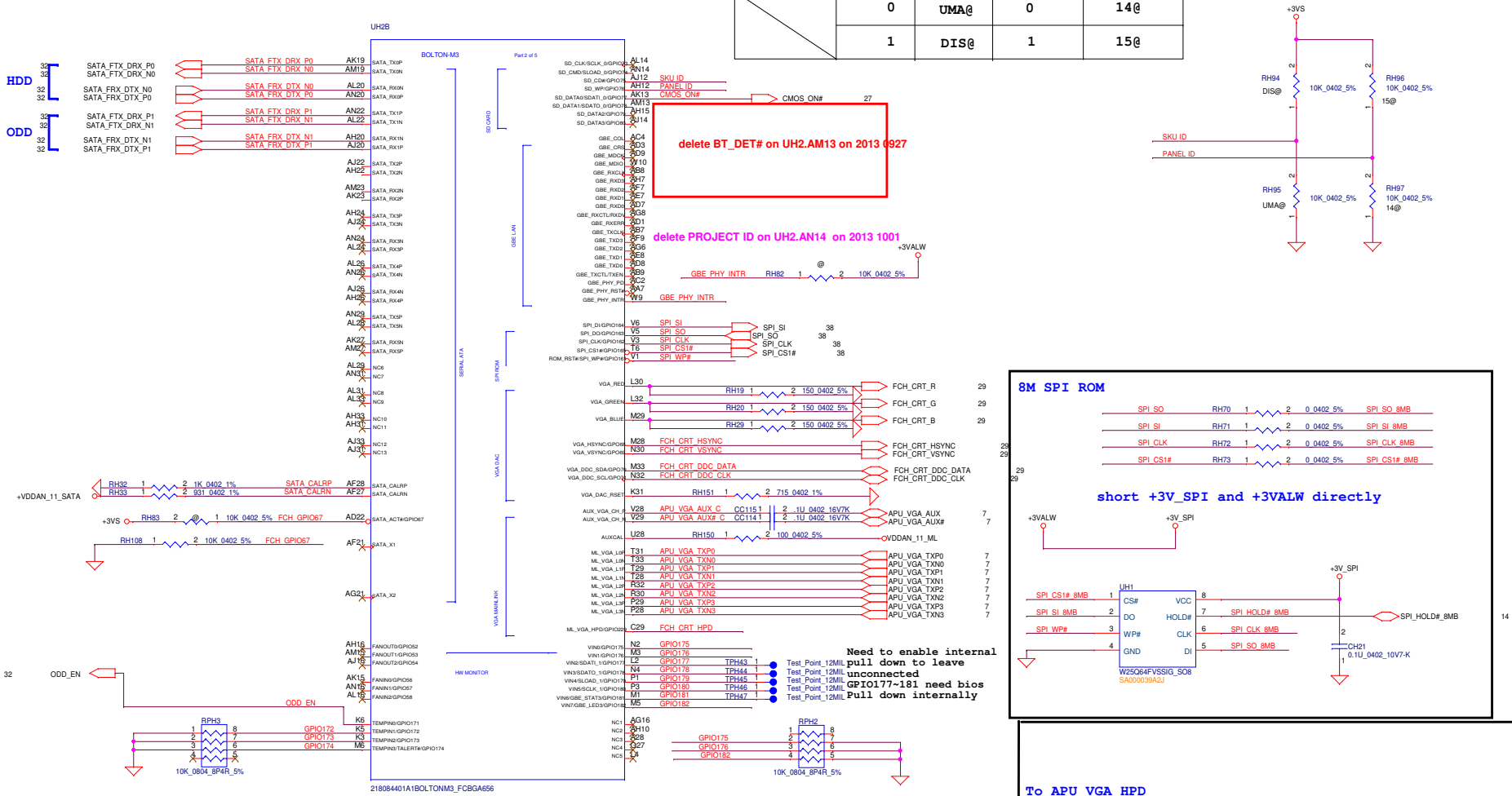


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	FCH PCIe/PCI/LPC/APU/S5+		
Size: Custom	Document Number: ACLU7		Rev: 1.A
Date: Monday, December 16, 2013	Sheet 12 of 52		

Add table on 2013 1001

BOARD ID Config.	SKU ID	Function	PANEL ID	Function
	0	UMA@	0	14@
	1	DIS@	1	15@



Security Classification	LC Future Center Secret Data			
Issued Date	2012/07/01	Deciphered Date	2014/07/01	

Title	FCH SATA/GBE/SPI		
Size	Document Number		Rev
C	ACLU7		1.A
Date:	Monday, December 16, 2013	Sheet	13 of 52

delete EC_LID_OUT# from UE1.Pin21 and UH2.R2 ,add GPU_WAKE#_R on UH2.R2

With S5 plus,PBTN_OUT# pull Up /Without S5 plus,PBTN_OUT# pull low

delete net name EC_SMI# on UH2.C26 on 20130928

Change net name from PCIE_WAKE# to EC_WAKE# on 20130928

Reserve CH9 and unmounted on 20130927

delete BATT_LEN# on UH1.J2

Change DGPU_PWROK_R from UH2.AG26 to UH2.AH14

GPU, EC, Thermal Sensor

2N7002KDWH
Vth= min 1V, max 2.5V
ESD 2KV

Follow Edge to connect with 0 ohm directly on 20131009

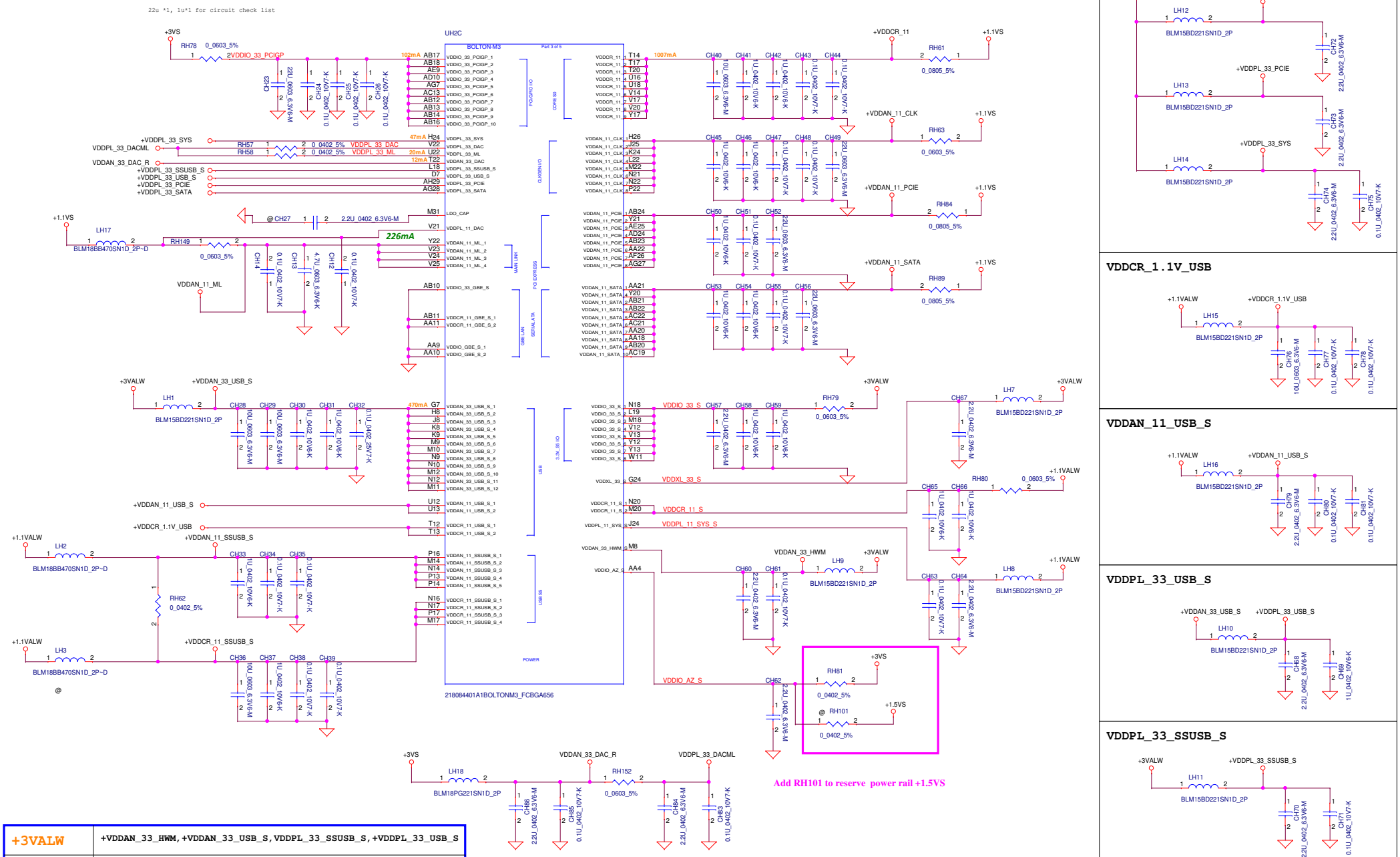
Delete Security EEPROM USROM3 ,unused

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: FCH ACPI/USB/GPIO

Size: Custom | Document Number: ACLU7 | Rev: 1.A

Date: Monday, December 16, 2013 | Sheet 14 of 52

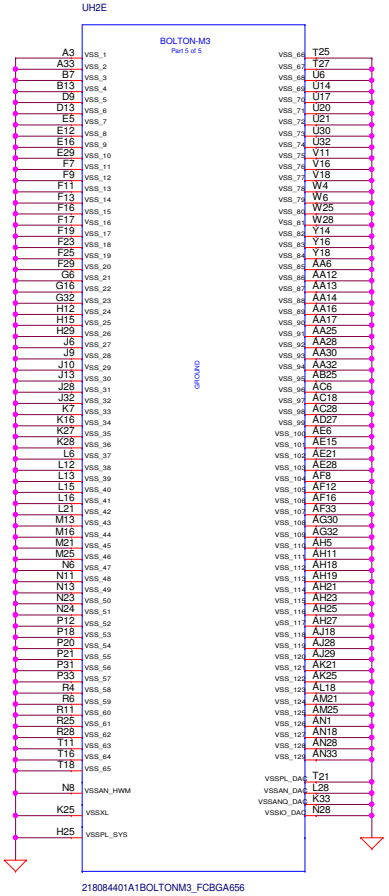


+3VALW	+VDDAN_33_HWM,+VDDAN_33_USB_S,VDDPL_33_SSUSB_S,+VDDPL_33_USB_S
+3VS	+VDDPL_33_SATA,+VDDPL_33_PCIE,+VDDPL_33_SYS
+1.1VALW	+VDDCR_11_SSUSB_S,+VDDAN_11_SSUSB_S,+VDDAN_11_USB_S, +VDDAN_11_USB_S,+VDDCR_1.1V_USB
+1.1VS	+VDDCR_11,+VDDAN_11_CLK,+VDDAN_11_PCIE,+VDDAN_11_SATA,

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: FCH POWER/GND

Size: Custom	Document Number: ACLU7		Rev: 1.A
Date: Monday, December 16, 2013	Sheet 15 of 52		



STRAP PINS

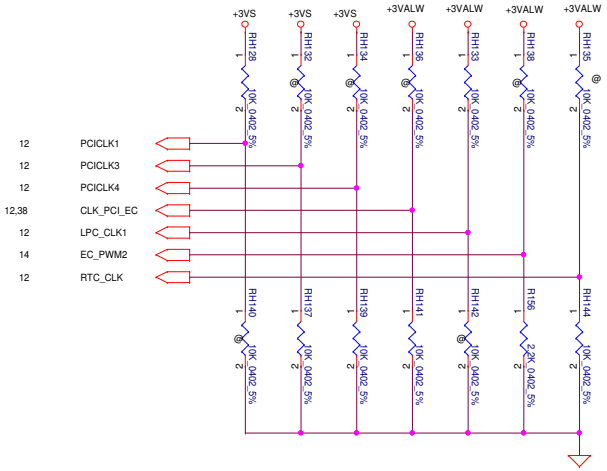
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED DEFAULT

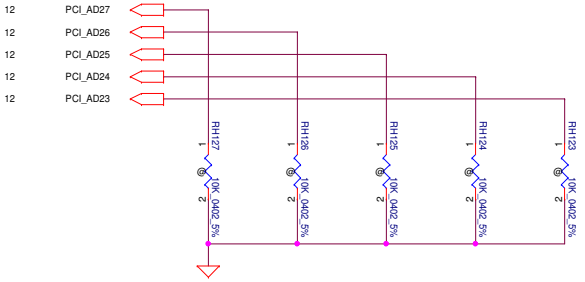
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

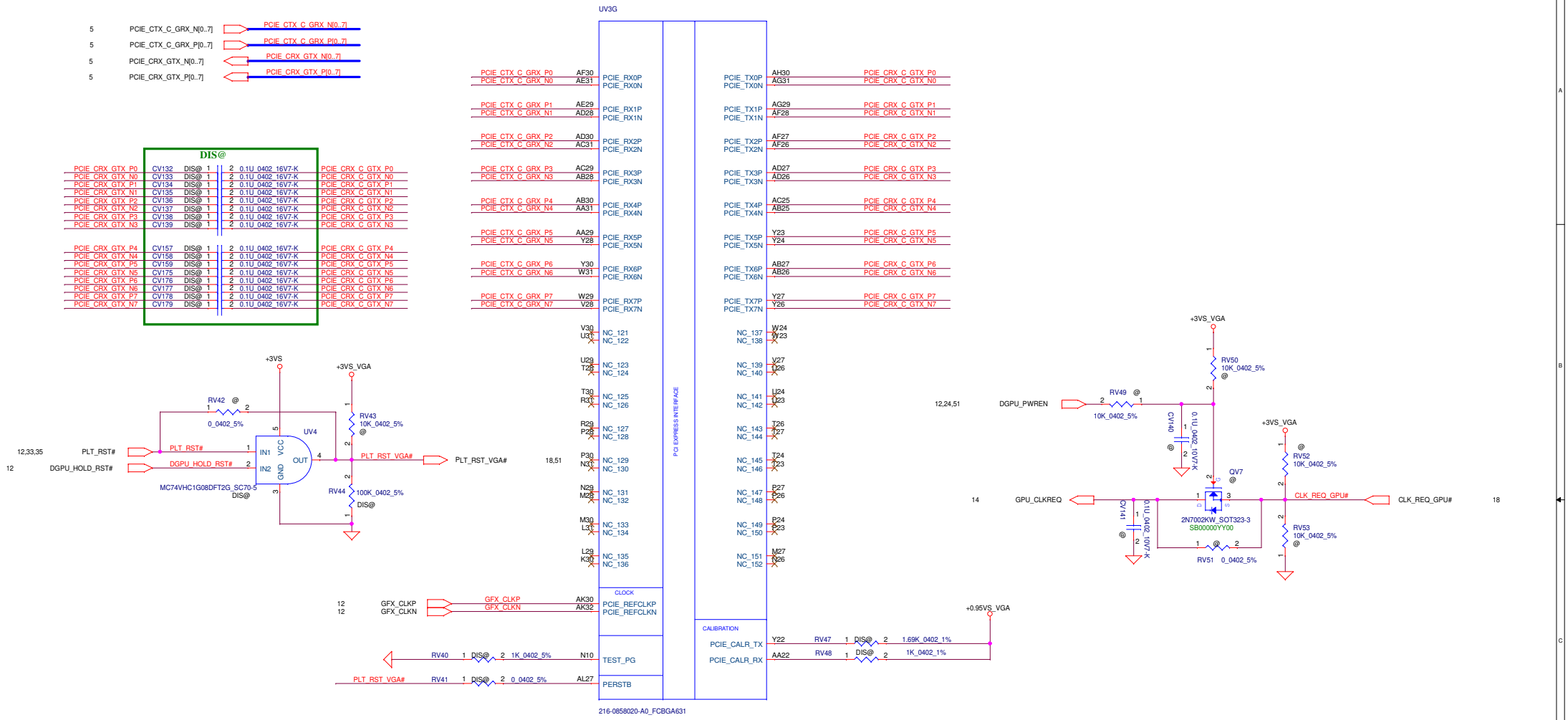
need confirm AD26





Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	FCH GND		
Size	Document Number		Rev
Custom	ACLU7		1.A
Date:	Monday, December 16, 2013	Sheet	16 of 52

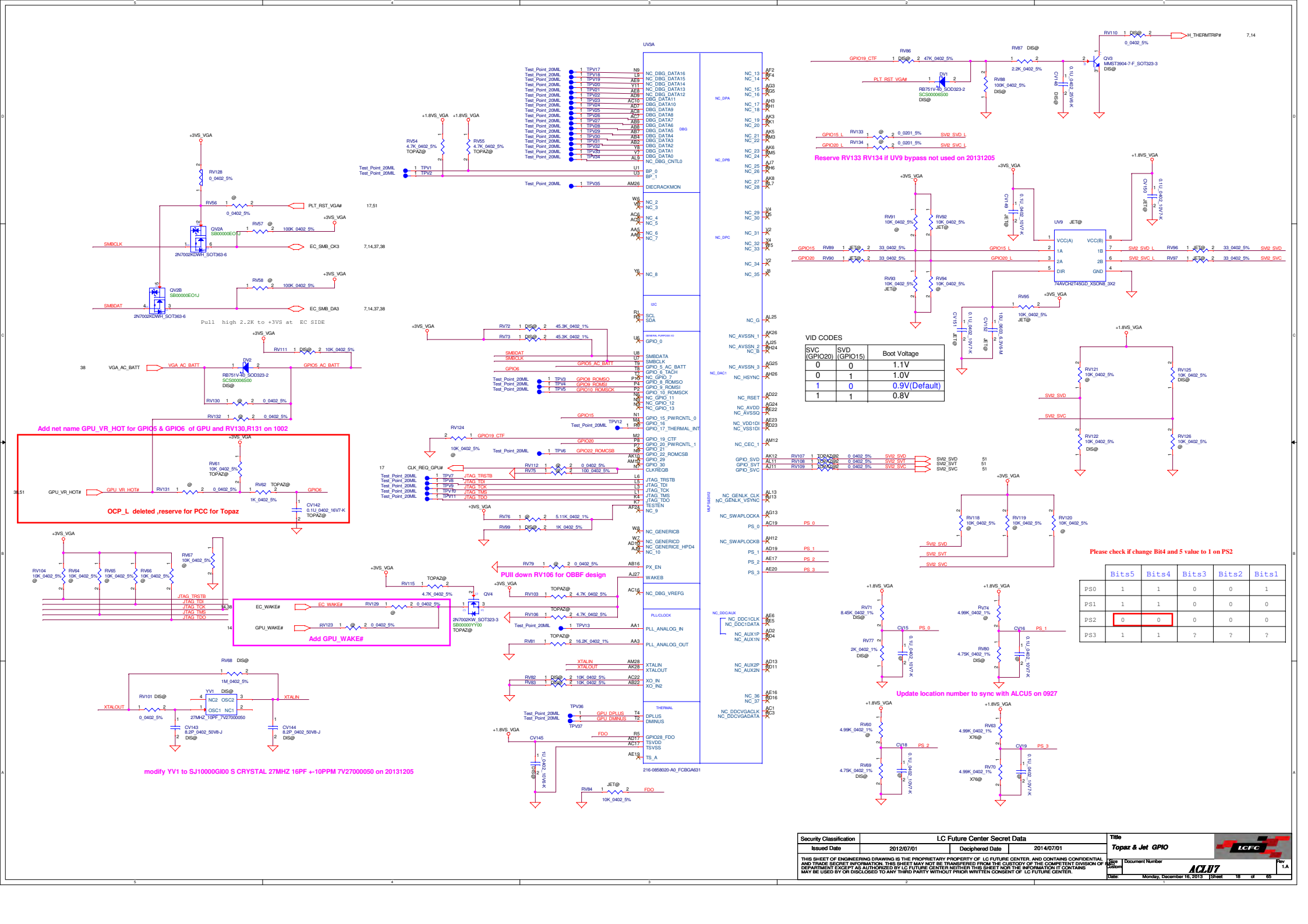


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: Topaz & Jet PCIE

Size	Document Number	Rev
Custom	ACLU7	1.A

Date: Monday, December 16, 2013 Sheet 17 of 65


Pull high 2.2K to +3VS at EC SIDE
Add net name GPU_VR_HOT for GPIO5 & GPIO6 of GPU and RV130,R131 on 1002
OCP_L deleted ,reserve for PCC for Topaz
Add GPU_WAKE#
modify YV1 to SJ10000GI00 S CRYSTAL 27MHZ 16PF +-10PPM 7V27000050 on 20131205
PUll down RV106 for OBBF design
Reserve RV133 RV134 if UV9 bypass not used on 20131205
Update location number to sync with ALCU5 on 0927
Please check if change Bit4 and 5 value to 1 on PS2
VID CODES
SVC (GPIO20) SVD (GPIO15) Boot Voltage
0 0 1.1V
0 1 1.0V
1 0 0.9V(Default)
1 1 0.8V
Bits5 Bits4 Bits3 Bits2 Bits1
PS0 1 1 0 0 1
PS1 1 1 0 0 0
PS2 0 0 0 0 0
PS3 1 1 ? ? ?
Security Classification LC Future Center Secret Data
Issued Date 2012/07/01 Deciphered Date 2014/07/01
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Title Topaz & Jet GPIO
Size Custom Document Number ACLU7 Rev 1.A
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Change power rail from +1.5VS_VGA to +1.35VS_VGA

+1.35VS_VGA

UV3B

MEM I/O

VMEMIO_1 H13
VMEMIO_2 H16
VMEMIO_3 H19
VMEMIO_4 J10
VMEMIO_5 J23
VMEMIO_6 J24
VMEMIO_7 J9
VMEMIO_8 K10
VMEMIO_9 K23
VMEMIO_10 K24
VMEMIO_11 K9
VMEMIO_12 L11
VMEMIO_13 L12
VMEMIO_14 L13
VMEMIO_15 L20
VMEMIO_16 L21
VMEMIO_17 L22

LEVEL TRANSLATION

VDD_GPIO18_1 AA20
VDD_GPIO18_2 AA21
VDD_GPIO18_3 AB20
VDD_GPIO18_4 AB21

I/O

VDD_GPIO33_1 AA17
VDD_GPIO33_2 AA18
VDD_GPIO33_3 AB17
VDD_GPIO33_4 AB18

NC_VDDR4_1 V12
NC_VDDR4_2 Y12
NC_VDDR4_3 U12

PLL

MPLL_PVDD L8
SPLL_PVDD H7
SPLL_VDDC H8
SPLL_PVSS J7

PCIE

PCIE_PVDD AM30

NC_38 AB23
NC_39 AC23
NC_40 AD24
NC_41 AE24
NC_42 AE25
NC_43 AE26
NC_44 AF25
NC_45 AG26

PCIE_VDDC_1 L23
PCIE_VDDC_2 L24
PCIE_VDDC_3 L25
PCIE_VDDC_4 L26
PCIE_VDDC_5 M22
PCIE_VDDC_6 N22
PCIE_VDDC_7 N23
PCIE_VDDC_8 N24
PCIE_VDDC_9 R22
PCIE_VDDC_10 T22
PCIE_VDDC_11 U22
PCIE_VDDC_12 V22

CORE

VDDC_1 AA15
VDDC_2 N15
VDDC_3 N17
VDDC_4 R13
VDDC_5 R16
VDDC_6 R18
VDDC_7 Y21
VDDC_8 T12
VDDC_9 T15
VDDC_10 T17
VDDC_11 T20
VDDC_12 U13
VDDC_13 U16
VDDC_14 U18
VDDC_15 V21
VDDC_16 V15
VDDC_17 V17
VDDC_18 V20
VDDC_19 Y13
VDDC_20 Y16
VDDC_21 Y18
VDDC_22 AA12
VDDC_23 M11
VDDC_24 N12
VDDC_25 U11
VDDC_26 AB13
VDDC_27 U10
VDDC_28 W9
VDDC_29 Y9
VDDC_30 W10
VDDC_31 T10
VDDC_32 AC14
VDDC_33 AB12
VDDC_34 AB11
VDDC_35 AC11
VDDC_36 AC13

POWER

FB_VDDC AC20
FB_GND_1 AD20

BIF_VDDC_1 R21
BIF_VDDC_2 U21

ISOLATED CORE I/O

VDDCI_1 M13
VDDCI_2 M15
VDDCI_3 M16
VDDCI_4 M17
VDDCI_5 M18
VDDCI_6 M20
VDDCI_7 M21
VDDCI_8 N20

FB_VDDCI W1
FB_GND_2 W3

216-0858020-A0_FCBGA631

TPV14
Test_Point_32MIL

+1.8VS_VGA

CV1 CV2 CV8 CV3 CV4 CV5 CV6 CV7
1U_0402_16V7-K 0.1U_0402_10V7-K 10U_0603_6.3V6-M 2.2U_0402_6.3V6-K

CV9 CV10
1U_0402_10V6-K

+3VS_VGA

+1.8VS_VGA

LV3
BLM18PG221SN1D_2P
DIS@

CV17 CV154 CV156
10U_0603_6.3V6-M 1U_0402_10V6-K

90mA
75mA
100mA

+1.8VS_VGA

LV4
BLM18PG121SN1D_2P
DIS@

CV20 CV21
10U_0603_6.3V6-M 1U_0402_10V6-K

+0.95VS_VGA

LV5
BLM18PG121SN1D_2P
DIS@

CV24 CV25
1U_0402_10V6-K 0.1U_0402_10V7-K

+1.8VS_VGA

CV26 CV27
10U_0603_6.3V6-M 1U_0402_10V6-K

+0.95VS_VGA

CV29 CV31 CV32 CV33 CV34 CV35 CV36
10U_0603_6.3V6-M 1U_0402_10V6-K

+VGA_CORE

CV37 CV38 CV39 CV40 CV41 CV42 CV43 CV44 CV45 CV46 CV47 CV48 CV49 CV50
2.2U_0402_6.3V6-K 10U_0603_6.3V6-M

CV51 CV52 CV53 CV54 CV55 CV56 CV57 CV58
2.2U_0402_6.3V6-K

Only available on TOPAZ, NC balls on JET

TOPAZ_VDDC_SEN
TOPAZ_VDDC_RTN

+0.95VS_VGA

CV22
1U_0402_10V6-K

+VGA_CORE

CV59 CV60 CV61 CV62 CV63 CV64 CV65
10U_0603_6.3V6-M 1U_0402_10V6-K 0.1U_0402_10V7-K

FOR JET,PUT VIAS UNDER ASIC

+VGA_CORE

51 VDDC_SEN — VDDC_SEN RV1 1 JET@ 2 0_0402_5%
51 VDDC_RTN — VDDC_RTN RV2 1 JET@ 2 0_0402_5%

VDDC_SEN RV3 1 TOPAZ@ 2 0_0402_5% TOPAZ_VDDC_SEN
VDDC_RTN RV4 1 TOPAZ@ 2 0_0402_5% TOPAZ_VDDC_RTN

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: Topaz & Jet Core Power

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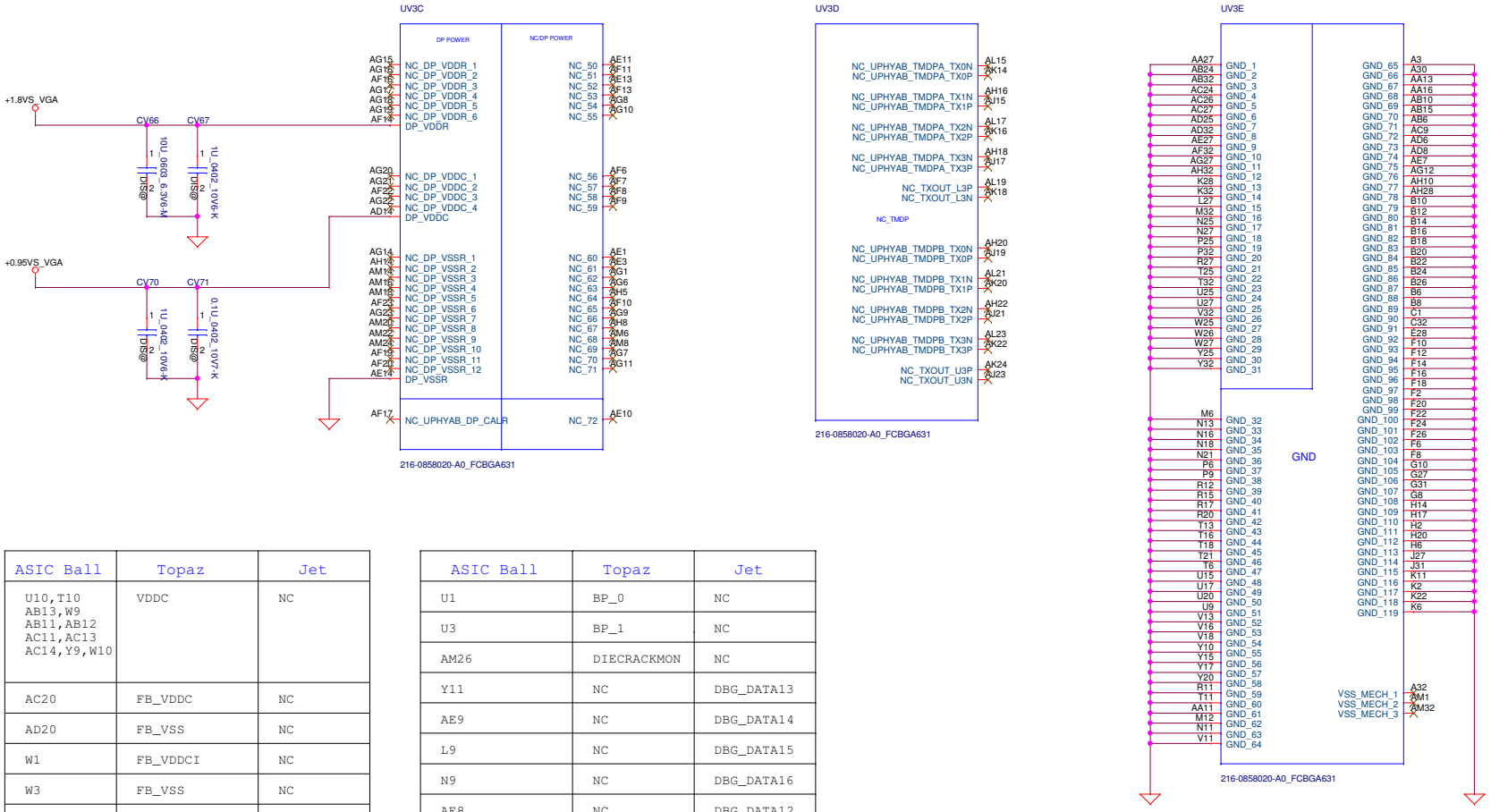

ASIC Ball	Topaz	Jet
U10,T10 AB13,W9 AB11,AB12 AC11,AC13 AC14,Y9,W10	VDDC	NC
AC20	FB_VDDC	NC
AD20	FB_VSS	NC
W1	FB_VDDCI	NC
W3	FB_VSS	NC
AJ11	GPIO_SVC	NC_SVI2
AK12	GPIO_SVD	NC_SVI2
AL11	GPIO_SVT	NC_SVI2
N6	GPIO_11	NC_GPIO11
N5	GPIO_12	NC_GPIO12
N3	GPIO_13	NC_GPIO13
AJ27	WAKEB	NC_VSYNC
T8	PCC/GPIO_6	GPIO_6
AA3	PLL_ANALOG_OUT	NC
AA1	PLL_ANALOG_IN	NC

ASIC Ball	Topaz	Jet
U1	BP_0	NC
U3	BP_1	NC
AM26	DIECRACKMON	NC
Y11	NC	DBG_DATA13
AE9	NC	DBG_DATA14
L9	NC	DBG_DATA15
N9	NC	DBG_DATA16
AE8	NC	DBG_DATA12
AL9	NC	DBG_CNTL0
H13,H16,H19,J10 J23,J24,J9,K10 K23,K24,K9,L11 L12,L13,L20,L21 L22	VMEMIO	VDDR1
AA17,AA18 AB17,AB18	VDD_GPIO33	VDDR3
AA20,AA21 AB20,AB21	VDD_GPIO18	VDD_CT

Title: *Topaz & Jet DP Power/GND*

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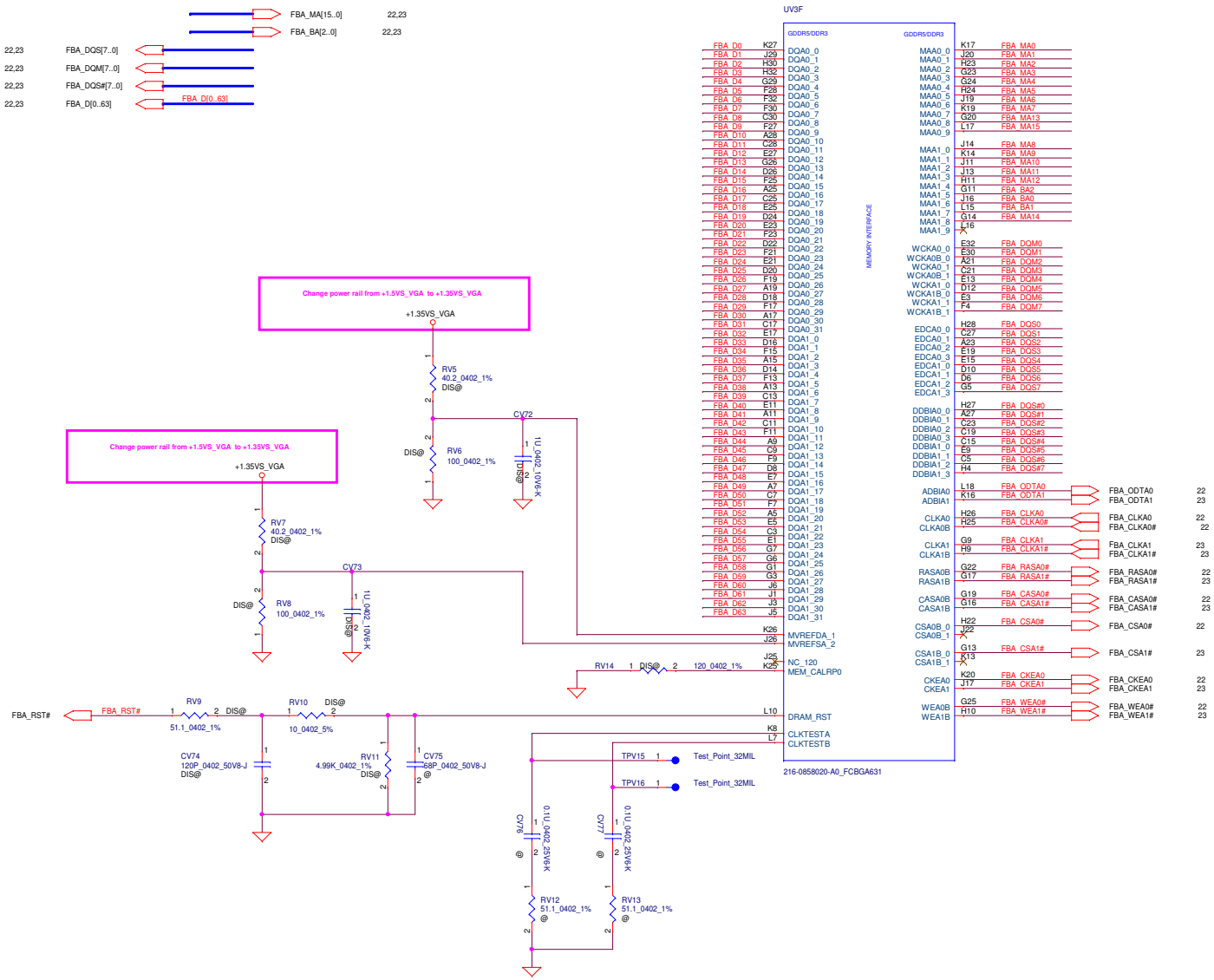

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: *Topaz & Jet MEM Interface*

Size	Document Number	Rev
C	ACLU7	1.A

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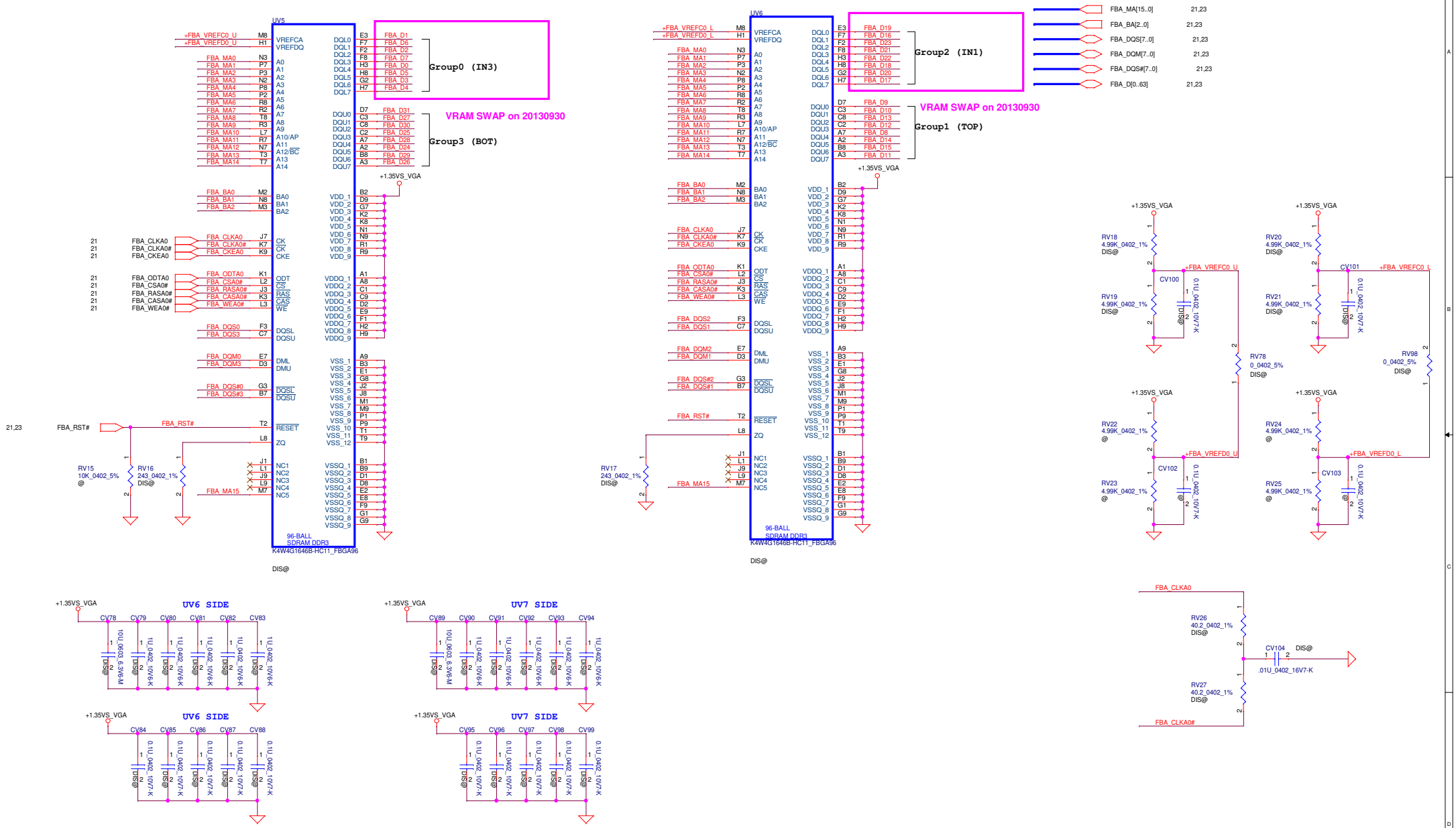
Memory Partition A - Lower 32 bits



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	Topaz & Jet DDR3 VRAM U		
Size Custom	Document Number ACLU7		Rev 1.A
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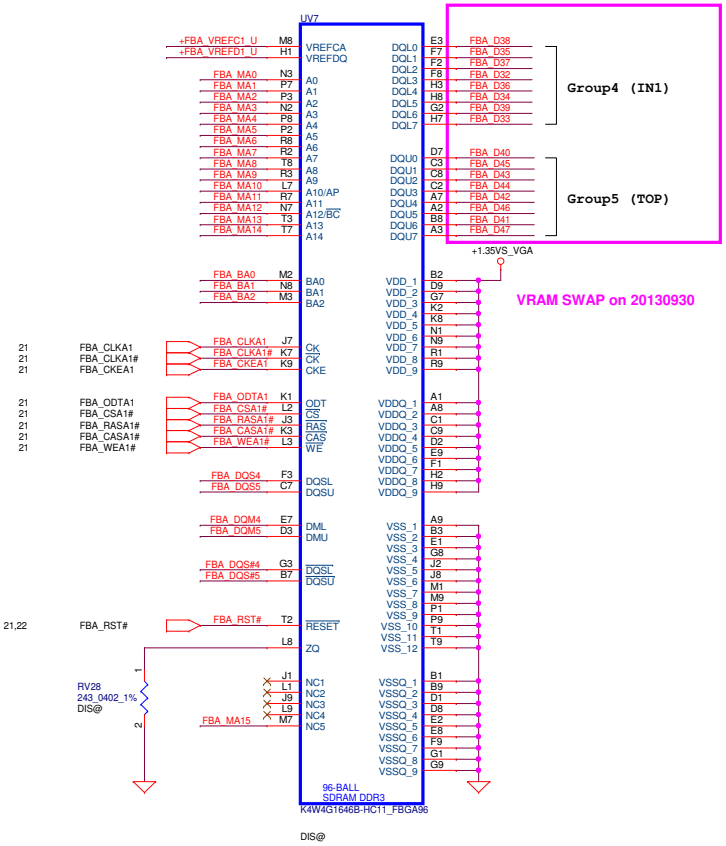
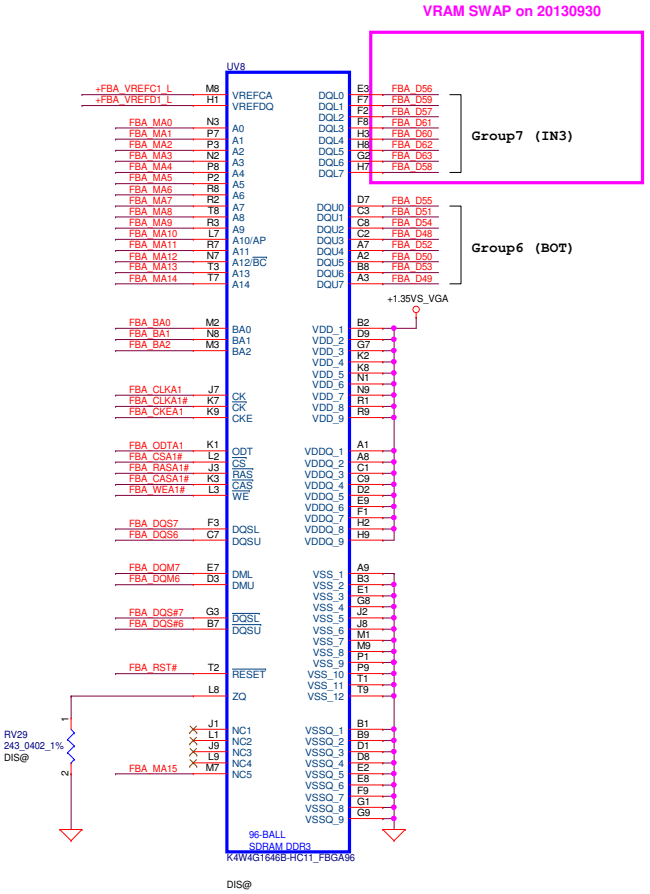
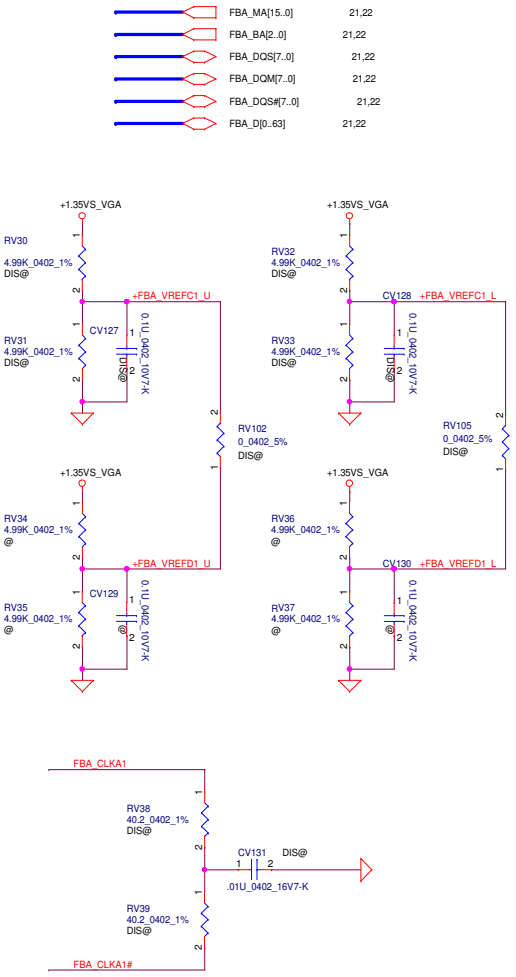
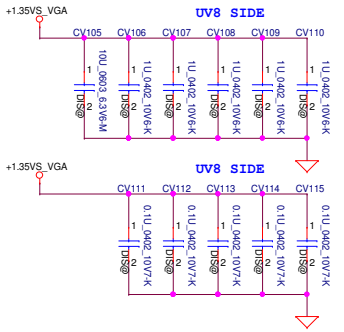
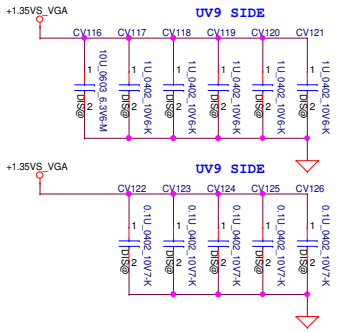
Memory Partition A - Upper 32 bits











Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: Topaz & Jet DDR3 VRAM L

Size	Document Number	Rev
Custom	ACLU7	1.A

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+0.95VS to +0.95VS_VGA

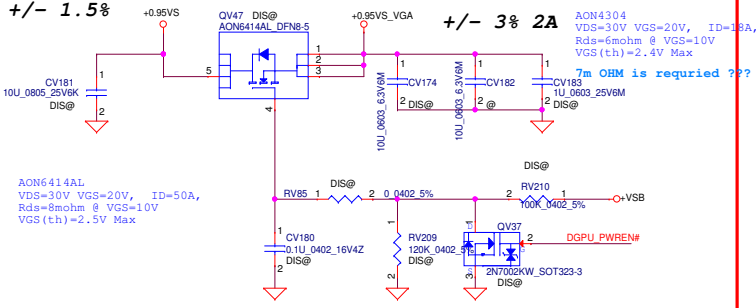
Reserve for GPU/APU share +0.95V

+/- 1.5%

+/- 3% 2A

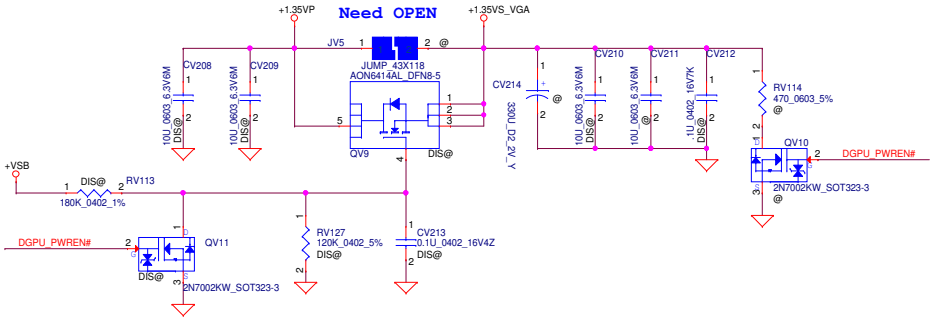
AON4304
VDS=30V VGS=20V, ID=18A,
Rds=6mohm @ VGS=10V
VGS(th)=2.4V Max

7m OHM is requried ???



Add 1.35VP to _+1.35VS_VGA on 20130925, RDS on less than 8,need to check, 4A for totally

+1.35VP TO +1.35VS_VGA



Check if QV46 need to replaced by LP2301ALT1G_SOT23-3 .

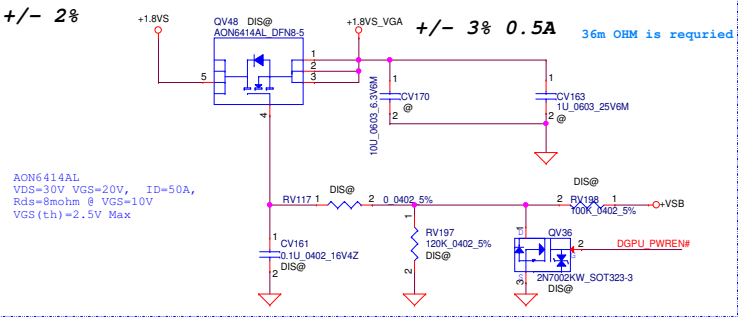
+1.8VS to +1.8VS_VGA

Reserve for GPU/APU share +1.8V

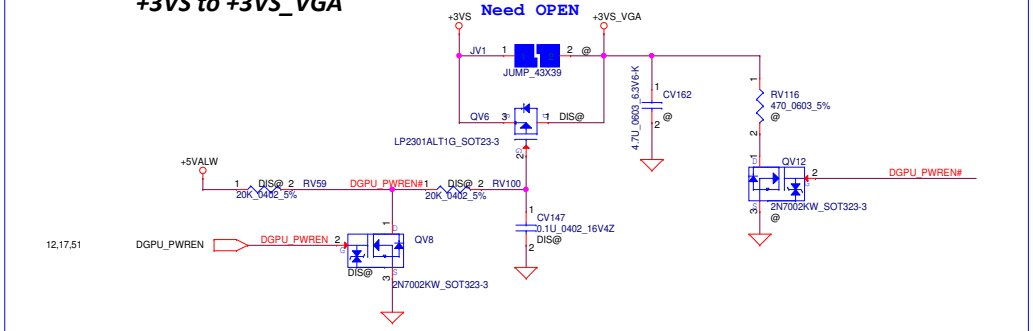
+/- 2%

+/- 3% 0.5A

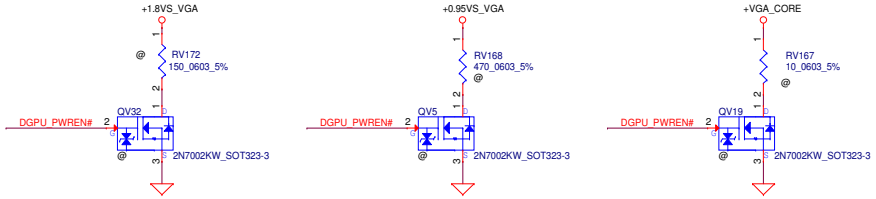
36m OHM is requried



+3VS to +3VS_VGA



GPU Power Discharger



reserve RV167 change to 10 ohm to meet power off sequence on 1202

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Title: Topaz & Jet SWITCH POWER

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BLANK

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title: *Topaz & Jet BLANK*

Size: Custom	Document Number: ACLU7	Rev: 0.4
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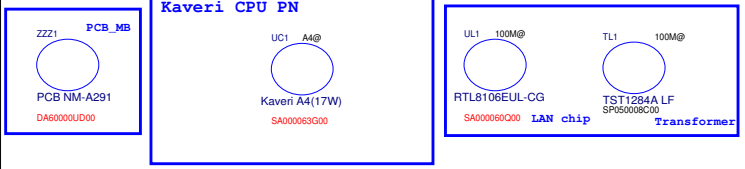

Board ID

BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description	Stuff Resistor
0	0	0	0	BDW + Jet-LE sku	RC107,RC108,RC109,RC123
0	0	1	0	BDW + Topaz-XT sku	RC107,RC108,RC102,RC123
0	1	0	0	BDW + N15V-GM sku	RC107,RC101,RC109,RC123
0	1	1	0	BDW + N15S-GT sku	RC107,RC101,RC102,RC123
1	0	0	0	HSW + Jet-LE sku	RC100,RC108,RC109,RC123
1	0	1	0	HSW + Topaz-XT sku	RC100,RC108,RC102,RC123
1	1	0	0	HSW + N15V-GM sku	RC100,RC101,RC109,RC123
1	1	1	0	HSW + N15S-GT sku	RC100,RC101,RC102,RC123
0	0	0	1	BDW + UMA sku	RC107,RC108,RC109,RC121
1	0	0	1	HSW + UMA sku	RC100,RC108,RC109,RC121

Title: *Virtual Symbol*

LCFC

Size	Document Number	Rev
C	ACLU7	0.1

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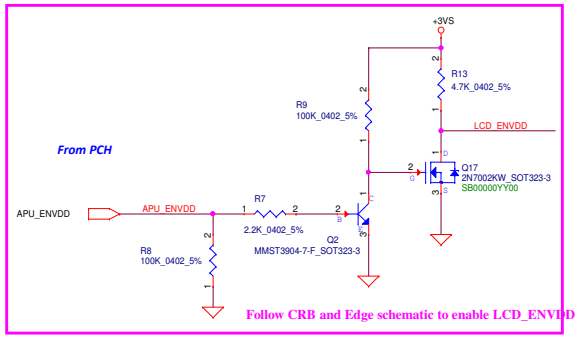
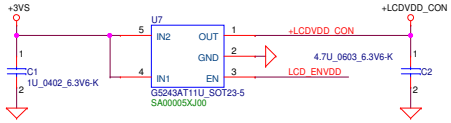
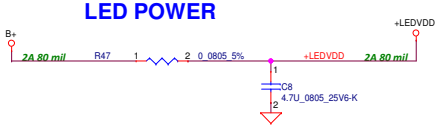


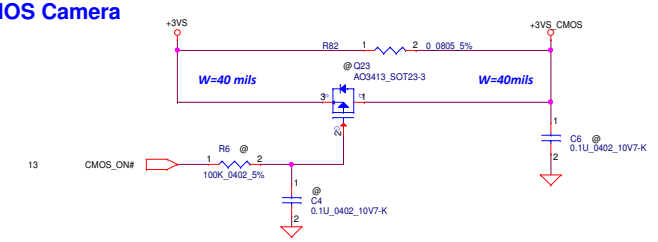
LCD POWER CIRCUIT



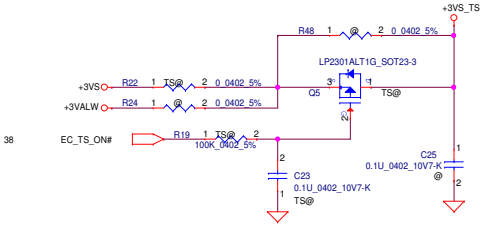
LED POWER



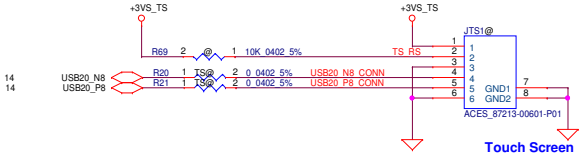
CMOS Camera



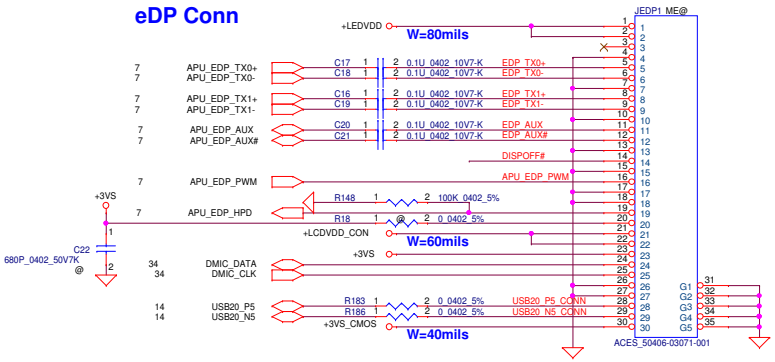
Touch Screen

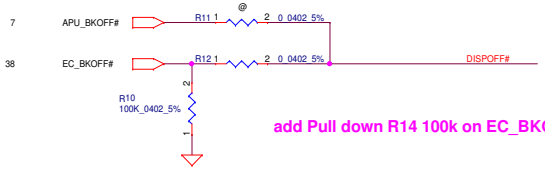


Touch Screen reserved

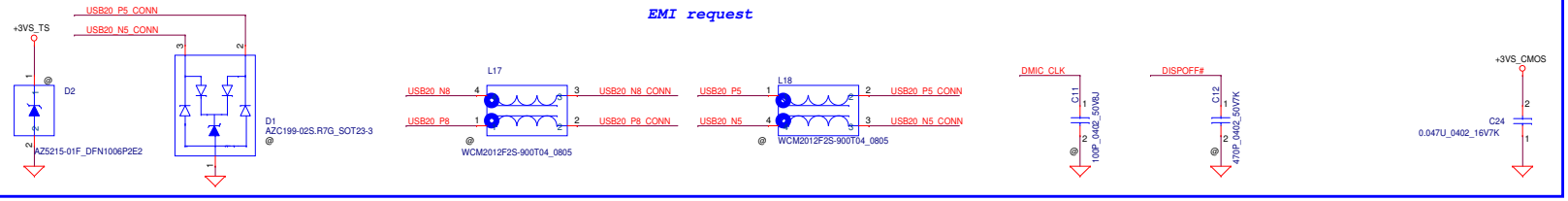


eDP Conn



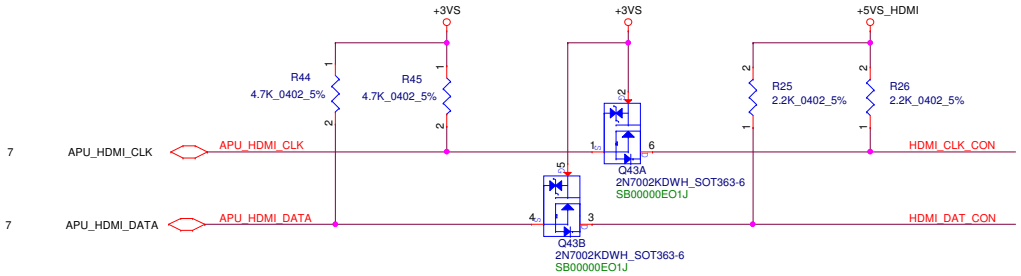


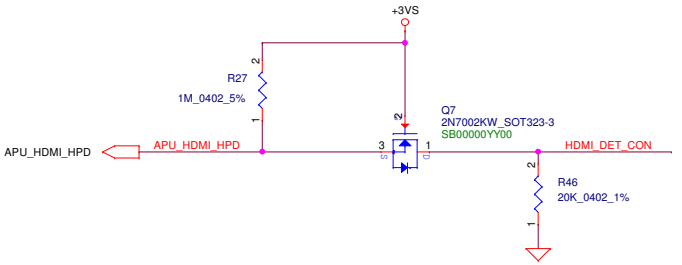
EMI request

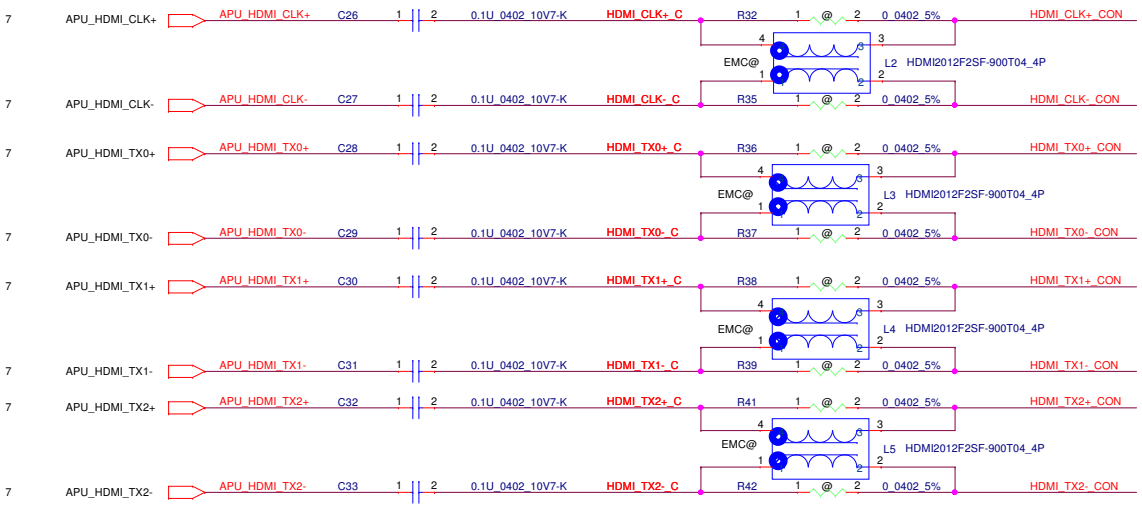


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

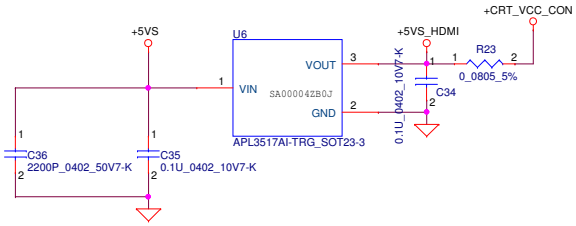
Title	eDP/ CMOS/Touch screen		
Size C	Document Number ACLU7		Rev 0.1
Date: Monday, December 16, 2013	Sheet 27 of 52		

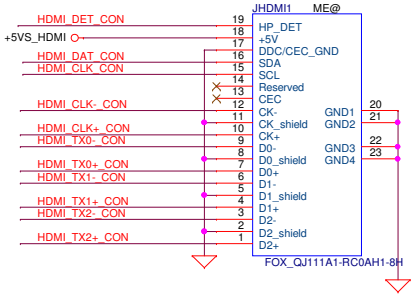


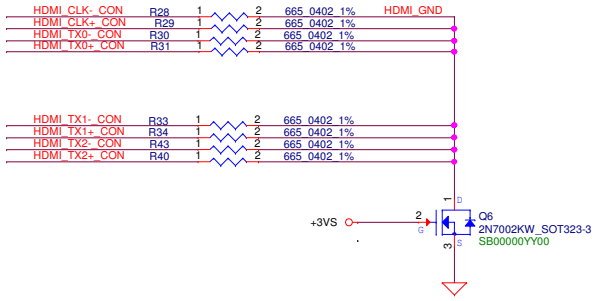




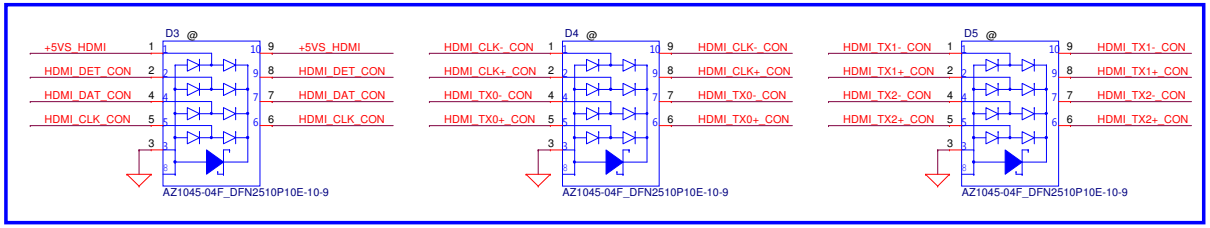
+CRT_VCC_CON and +5VS_HDMI trace width 100 mils







For ESD



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ***HDMI_CONN***

Size	Document Number	Rev
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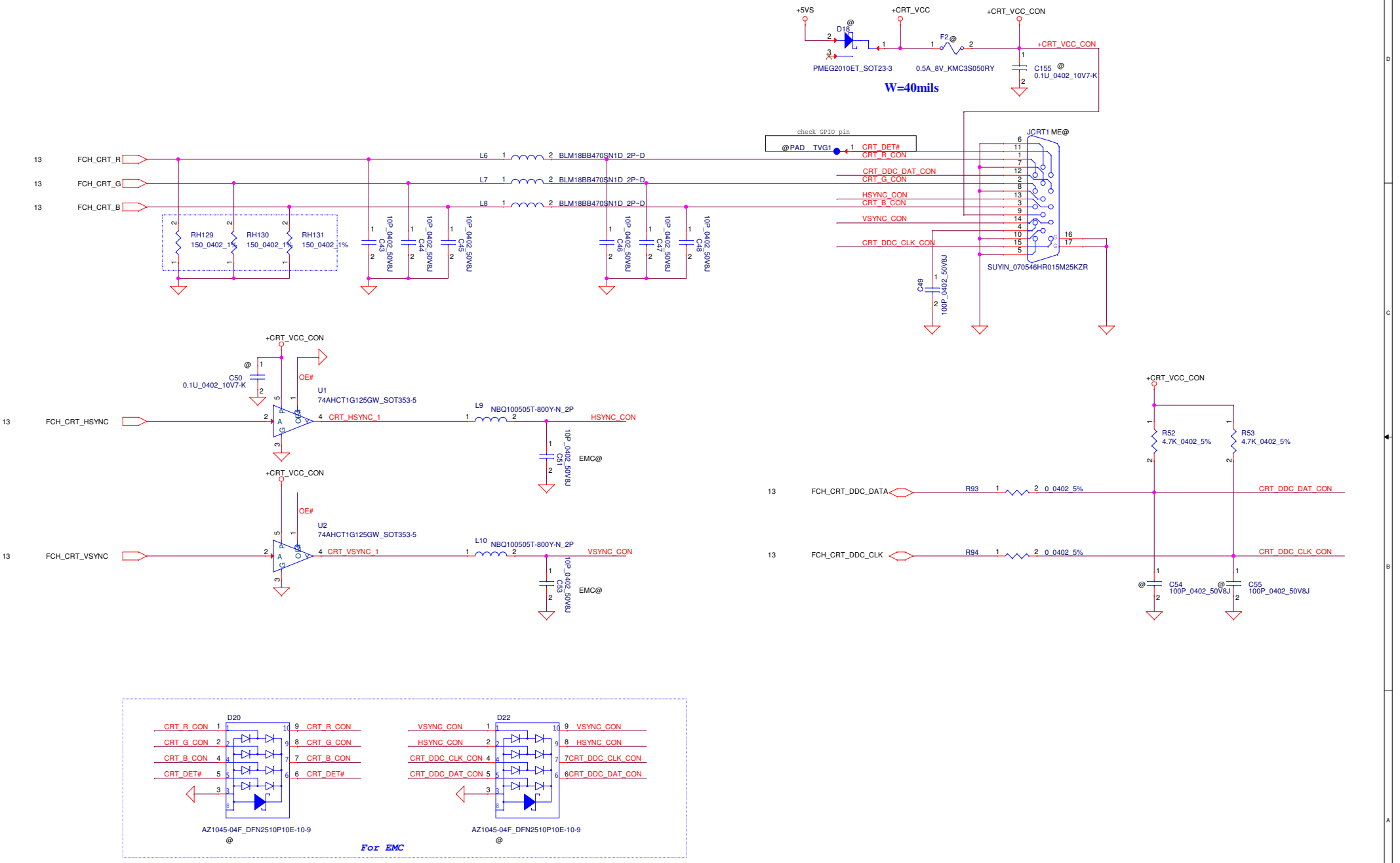
Date: Monday, December 16, 2013 Sheet 28 of 52

CRT Connector



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	CRT_CONN		
Size	Custom	Document Number	ACLU7
Rev	0.1		
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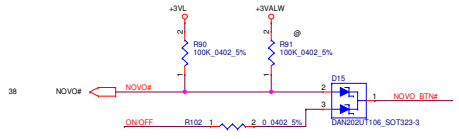
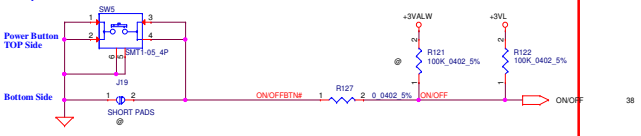
ON/OFF switch



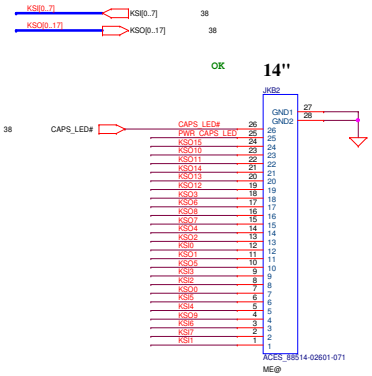
Power Button

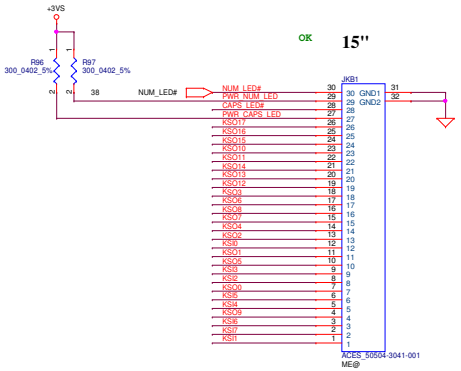
ON/OFF switch

Reserved SW5 for debug on 20130926

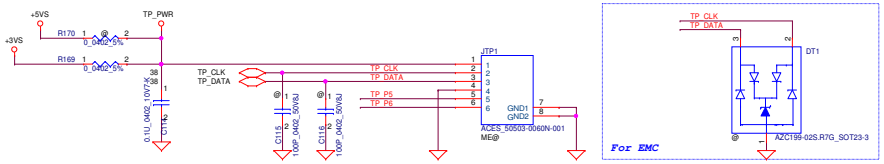


K/B Connector





TP/B Connector

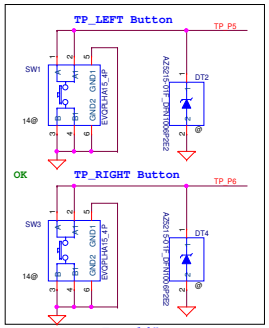


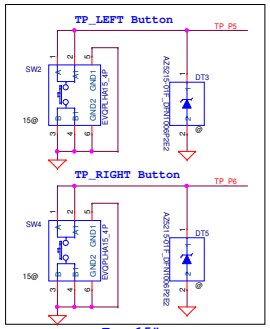
For 14"

1	VDD
2	CLK
3	DAT
4	GND
5	TP-L
6	TP-R

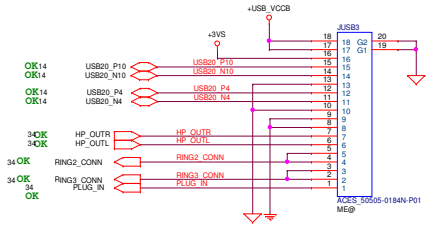
For 15"

1	VDD
2	CLK
3	DAT
4	GND
5	TP-L
6	TP-R

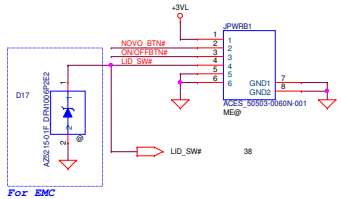




USB I/O Connector

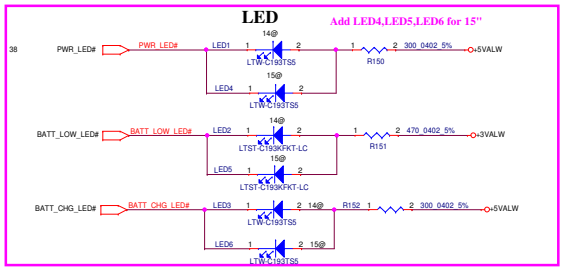


PWR/B Connector



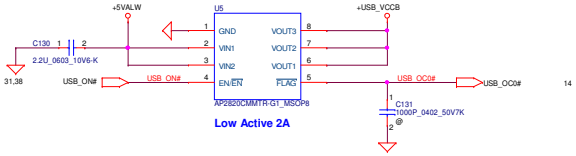
LED

Add LED4,LED5,LED6 for 15"



Delete JLED1 on due to both G14 and G15 move LED to MB

Right Side USB2.0 Port X 1 (USB/B)



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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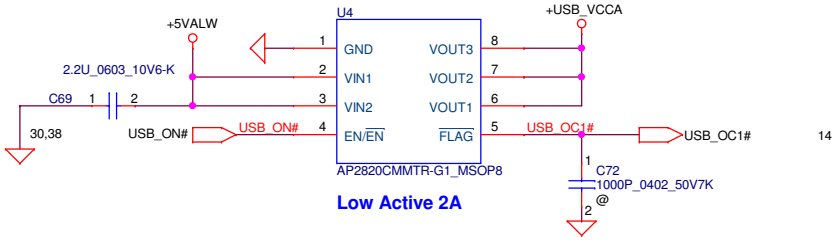
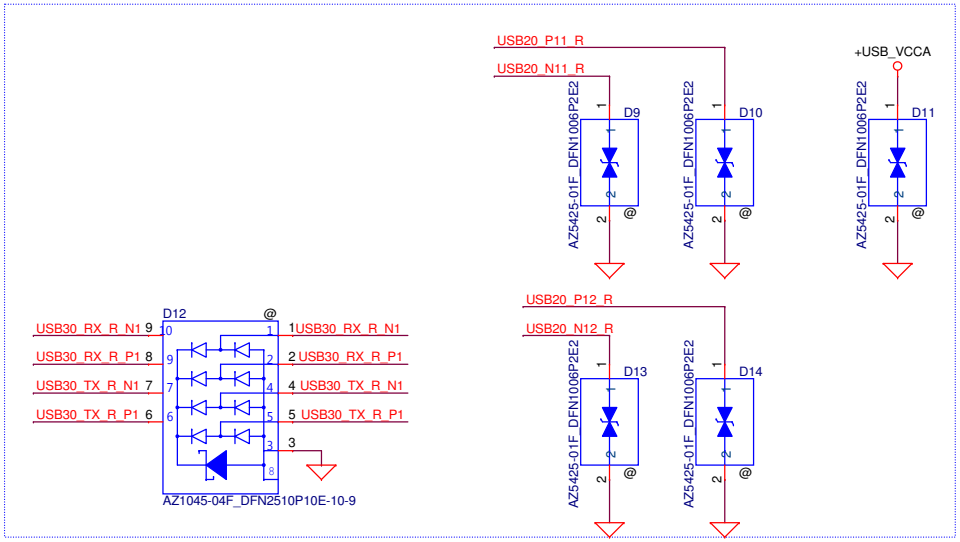
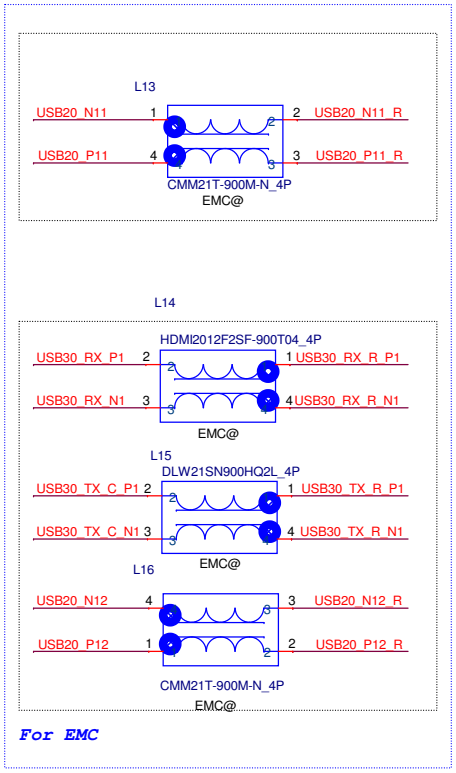
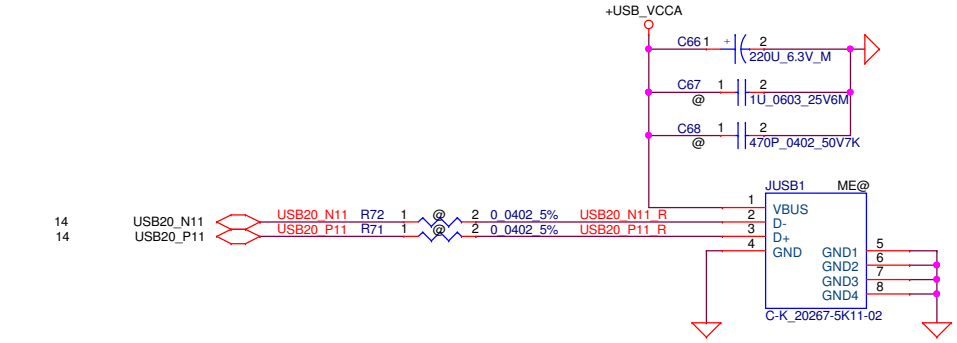
Title	KBD/PWR/IO/LED/TP Conn		
Size	Document Number		Rev
Custom		ACL07	0.1
Date:	Monday, December 16, 2013	Sheet	30 of 52

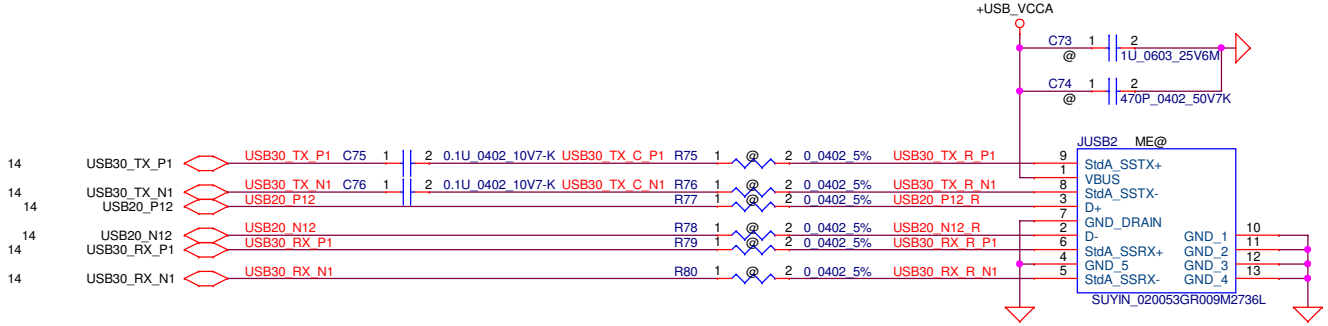
LEFT SIDE USB3.0 PORT X2









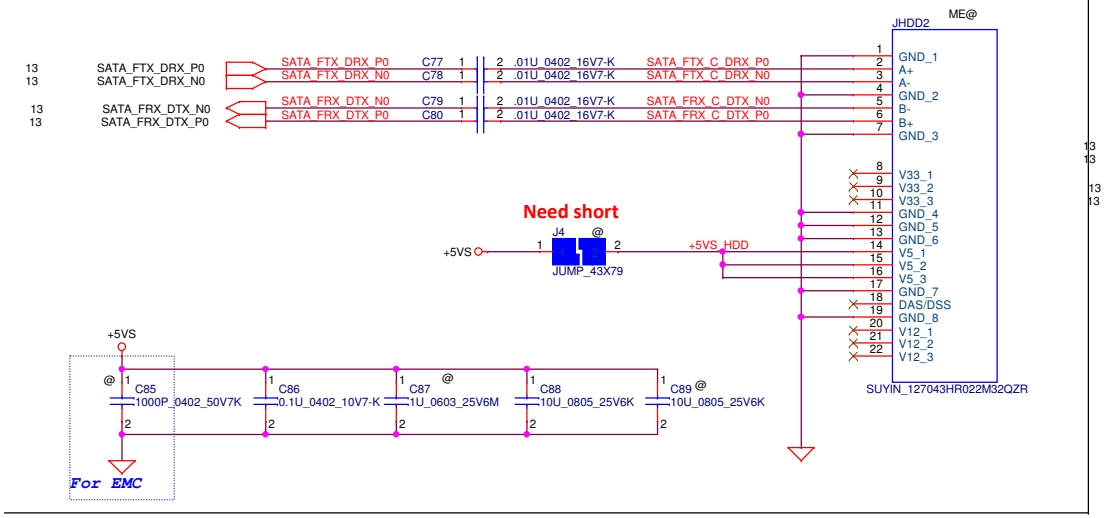


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

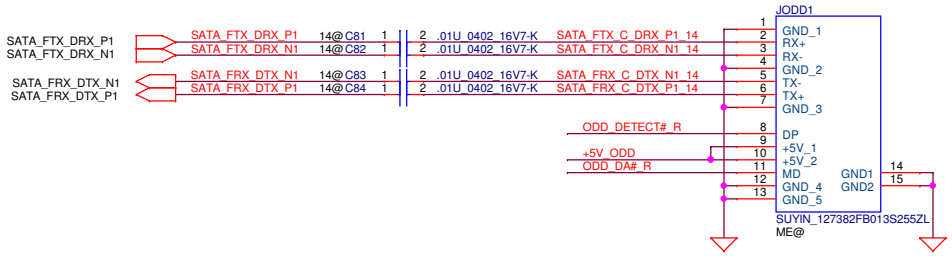
Title: **USB 3.0 PORT (LEFT)**

Size	Document Number	Rev
Custom	ACLU7	0.1
Date: Monday, December 16, 2013	Sheet 31 of 52	

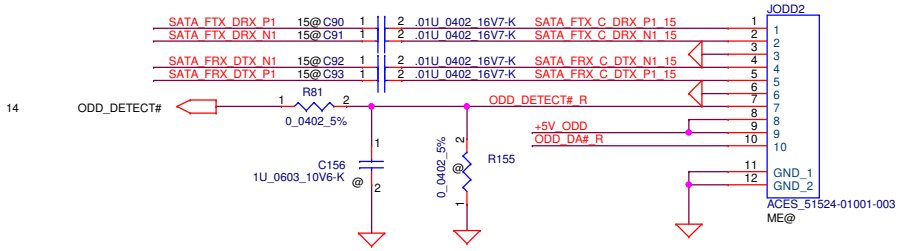
SATA HDD Conn.

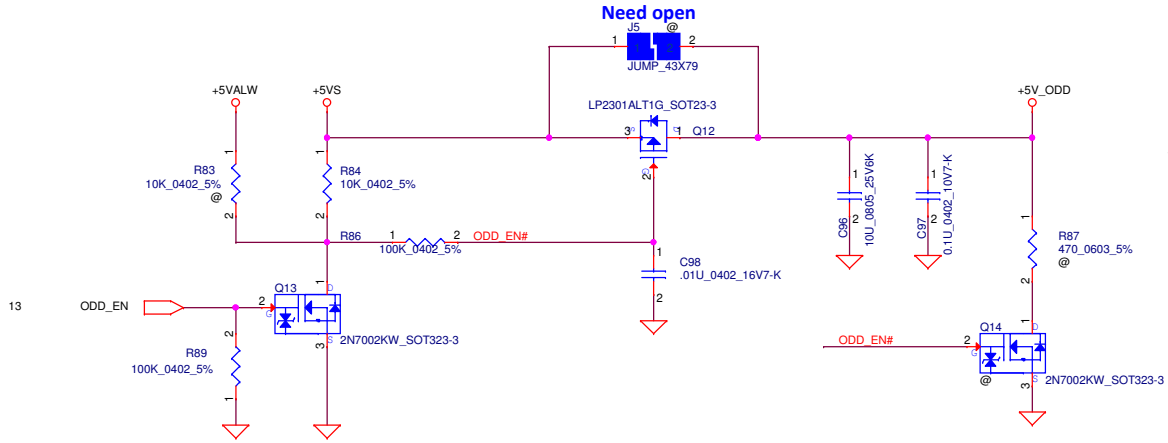


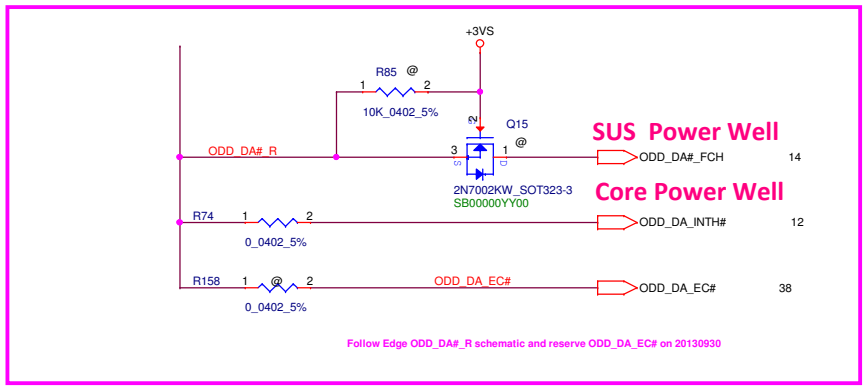
FOR 14" SATA ODD Conn.



FOR 15" SATA ODD FFC Conn

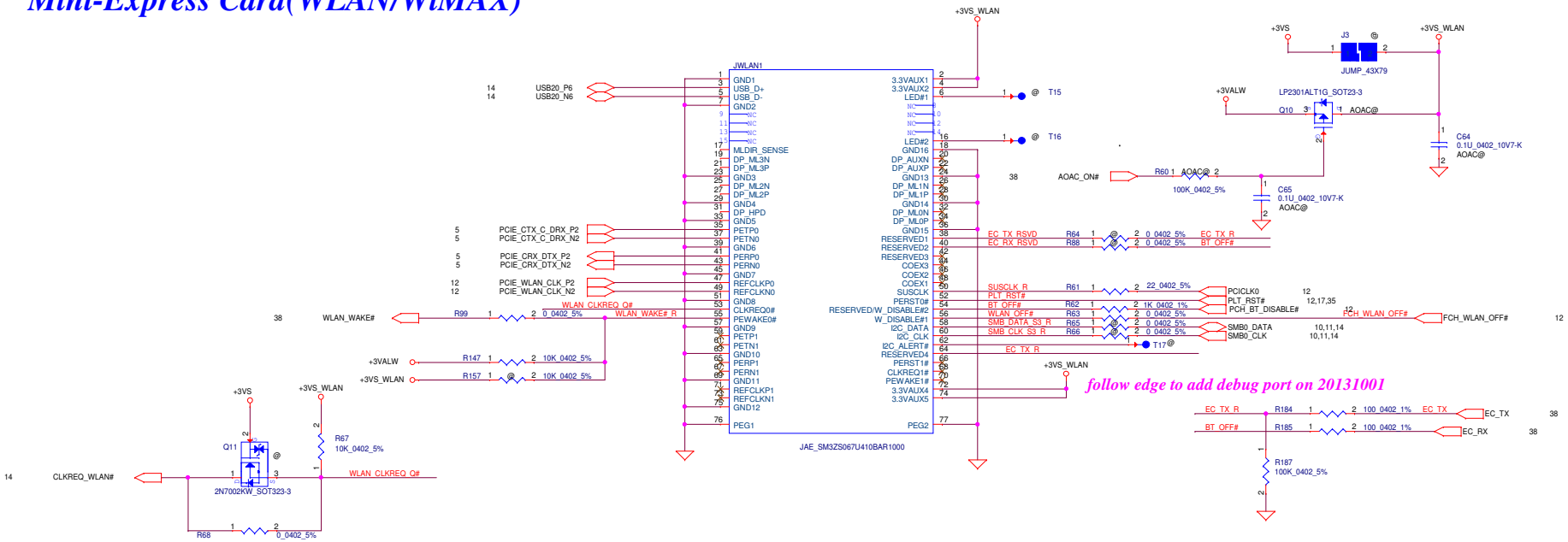






Title		
HDD/ODD CONN		
Size: Custom	Document Number: ACLU7	Rev: 0.1
Date: Monday, December 16, 2013	Sheet 32 of 52	

Mini-Express Card(WLAN/WiMAX)



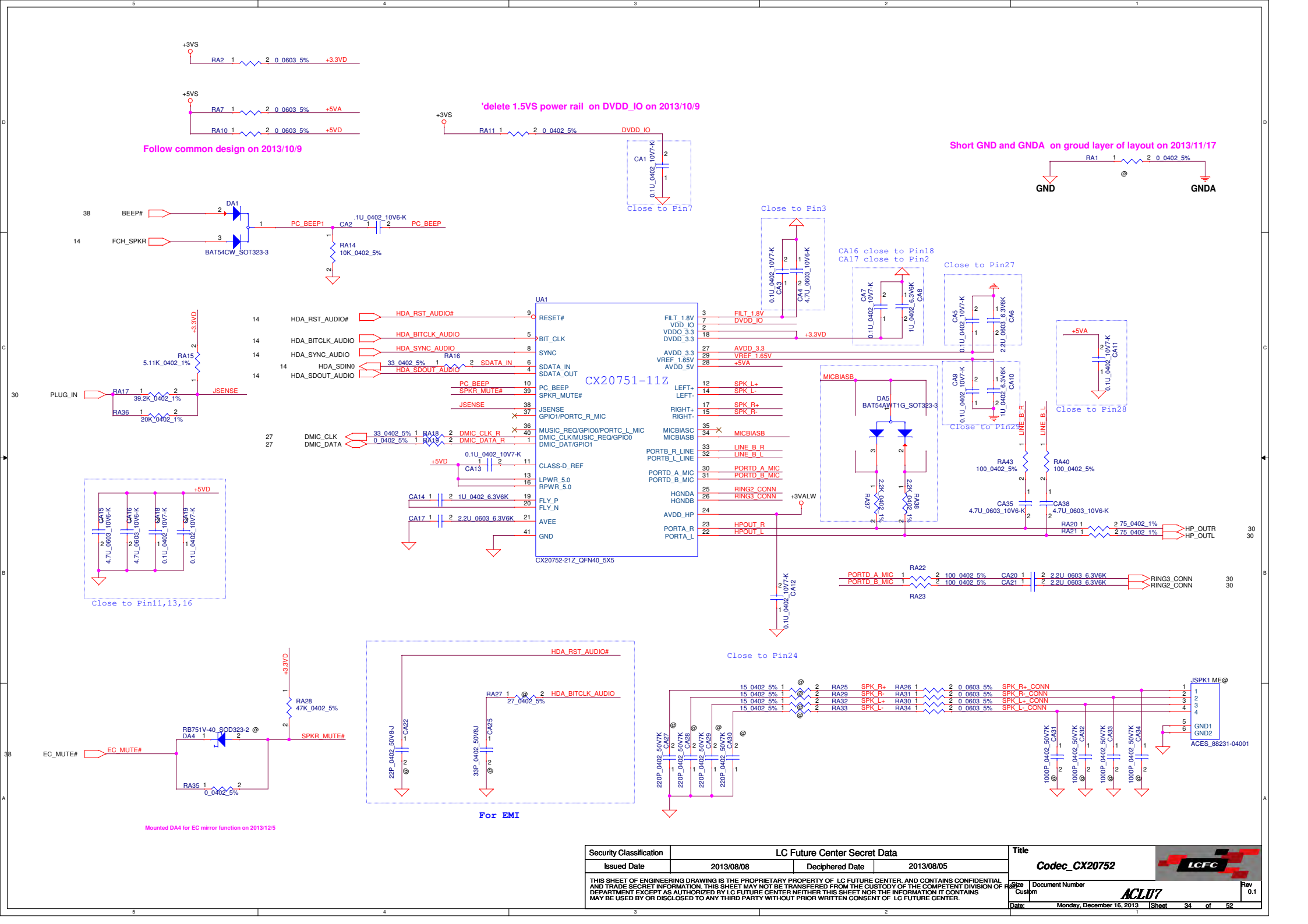
follow edge to add debug port on 20131001

Connect CLKREQ_WLAN# and WLAN_CLKREQ_Q# directly and reserve Q11 on 20131004

Change R67 power rail from 3VS to +3VS_WLAN on 20131011

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	NGFF-Card / SSD		
Size C	Document Number ACLU7		Rev 0.1
Date: Monday, December 16, 2013	Sheet 33 of 52		



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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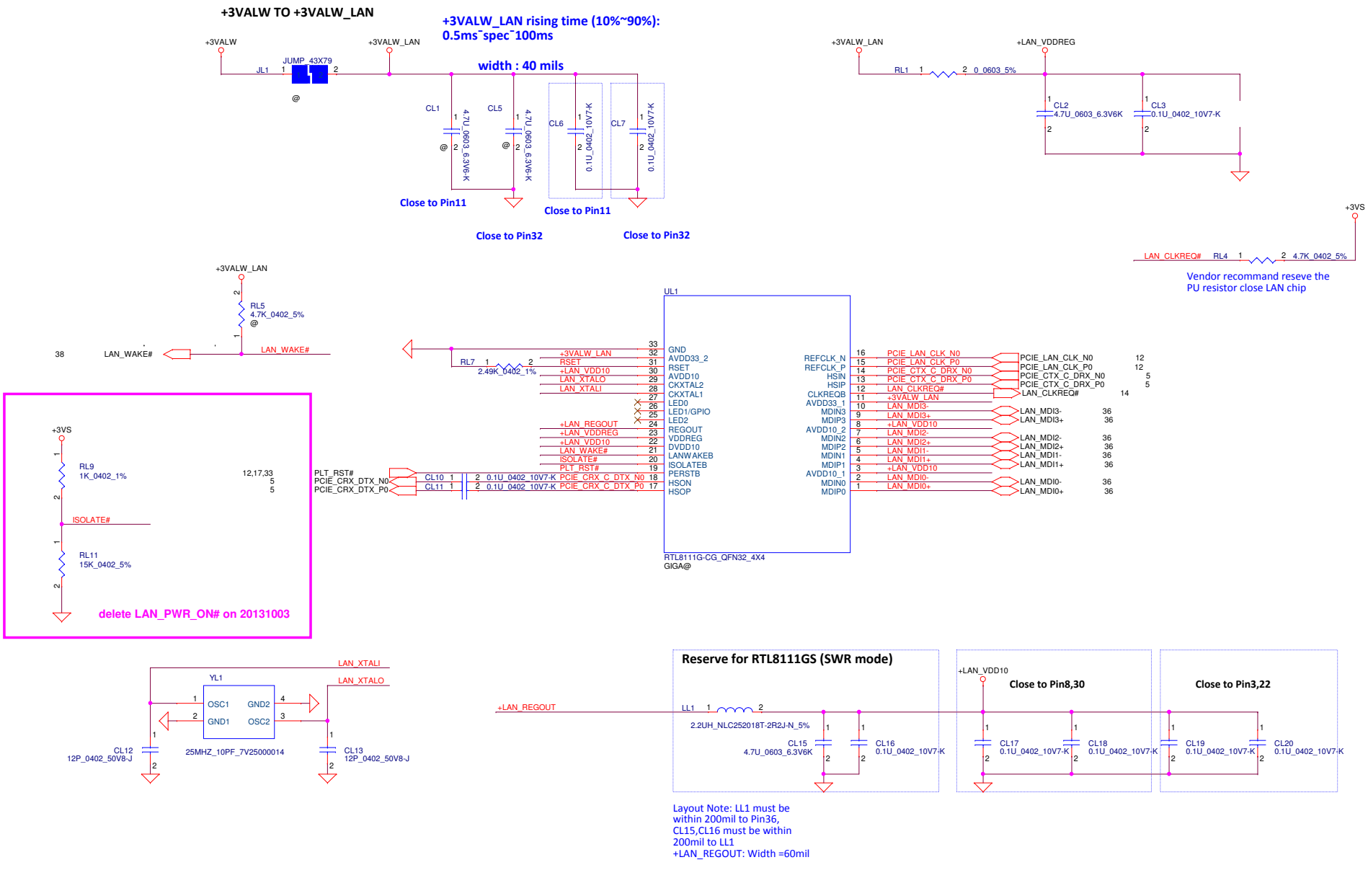
Title	Codec_CX20752		
Size	Custom	Document Number	ACLU7
Rev	0.1		
Date:	Monday, December 16, 2013	Sheet	34 of 52



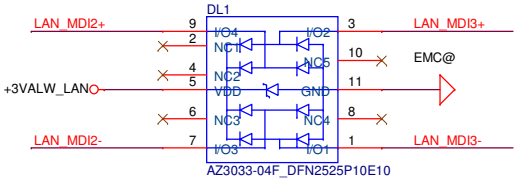
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: LAN_RTL8106E/8111G

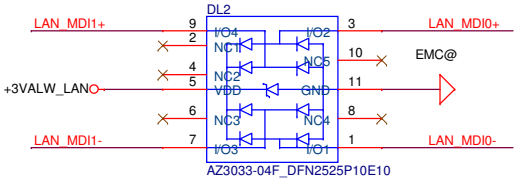
Size	Document Number	Rev
Custom	ACLV7	0.1

Date: Monday, December 16, 2013 Sheet 35 of 52

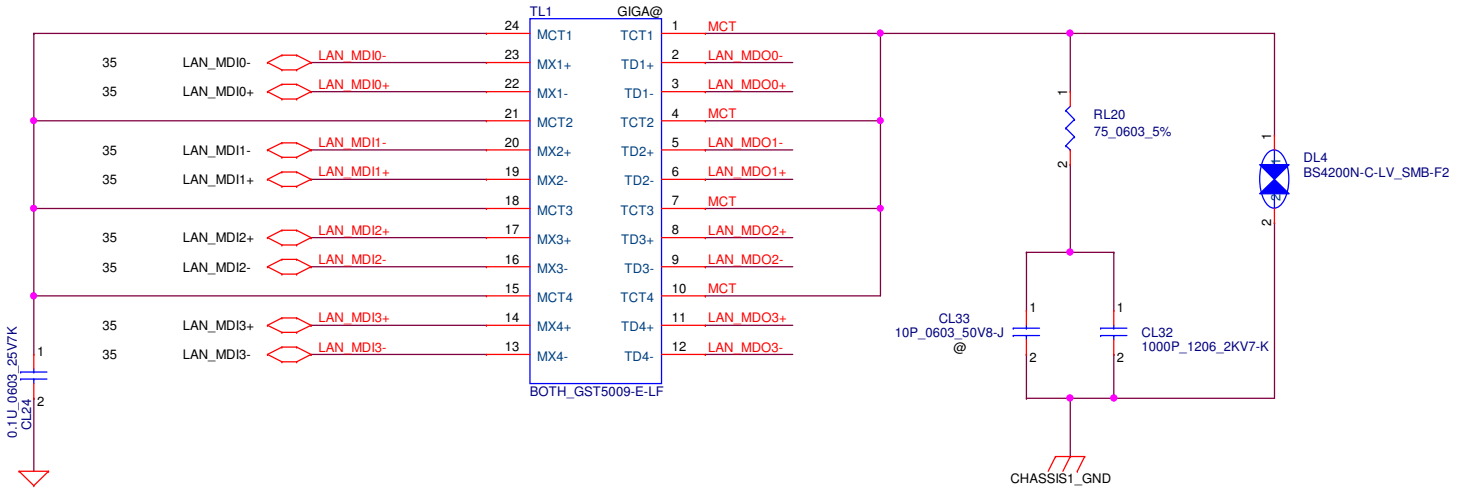
DL1/DL2
1'S PN:SC300003M00

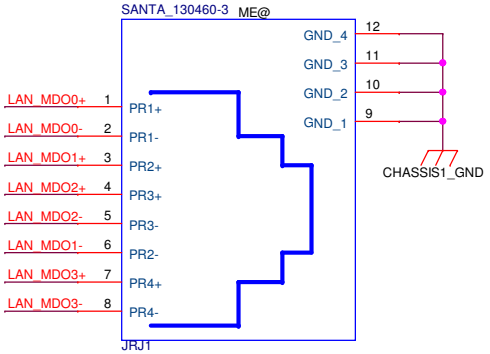


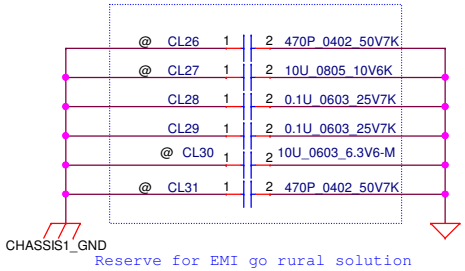
Place Close to TL1



Place Close to TL2







Reserve for EMI go rural solution

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: LAN_Transformer

Size	Document Number	Rev
B	ACLU7	0.1

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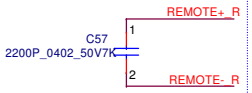
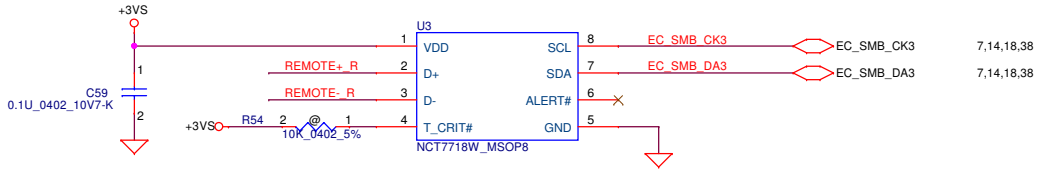
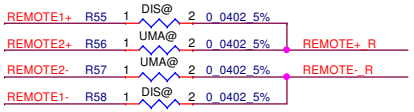
Close U3



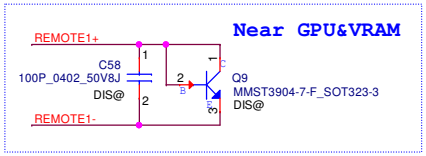
SMSC thermal sensor placed near DIMM



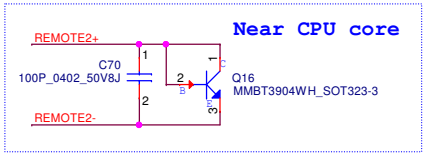
Address 1001_101xb



Near GPU&VRAM

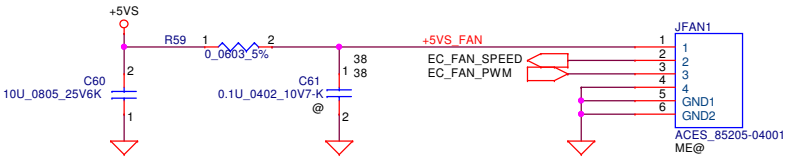


Near CPU core



REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN Conn



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: *Thermal sensor/FAN CONN*

Size	Document Number	Rev
Custom	ACLU7	0.1

Date: Monday, December 16, 2013 Sheet 37 of 52

Close EC

All capacitors close to EC

minimum trace width 12 mil

Change RE6 to 0ohm jump

Please change net name VGA_AC_DET on page51
to another net name XXX and spare one EC pin for this pin name XXX !!!

IT8586E/AX
LQFP-128L

Delete TURBO_V on UE1.67 ,PWR_unused

add DGPU_PWROK to UE1.85

reserved CE90 for EMC request

For factory EC flash

Change RE24 to 0ohm jump

delete LAN_PWR_ON# on 20131003

when mirror, RE45 RE47 RE48 RE49 mounted
when no mirror, RE45 RE47 RE48 RE49 reserved

when mirror, GPG2 pull high
when no mirror, GPG2 pull low

EMI/ESD

AC IN

Add Board ID ,please check with Edge

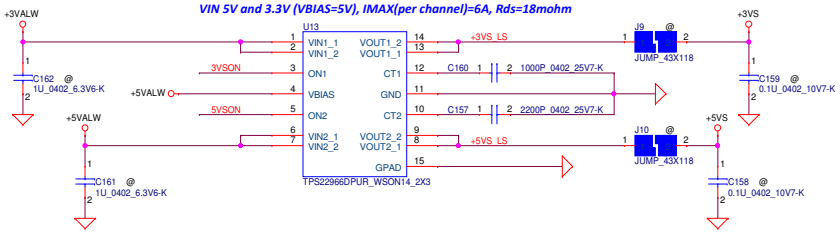
Vcc	3.3V +/- 5%			
RE33	100K +/- 1%			
Board ID	RE34	VAD_BID min	VAD_BID typ	VAD_BID max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

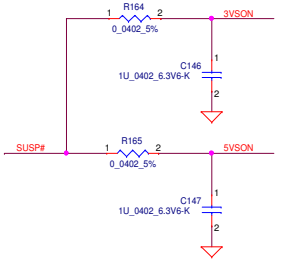
Title: EC ITE8586LQFP
Size: Custom | Document Number: AQU7 | Rev: 0.1
Date: Monday, December 16, 2013 | Sheet 38 of 52

Load Switch
+5VALW To +5VS
+3VALW To +3VS

+5VS, C159 --> 1.5ms
+3VS, C160 --> 2.5ms

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=18mohm





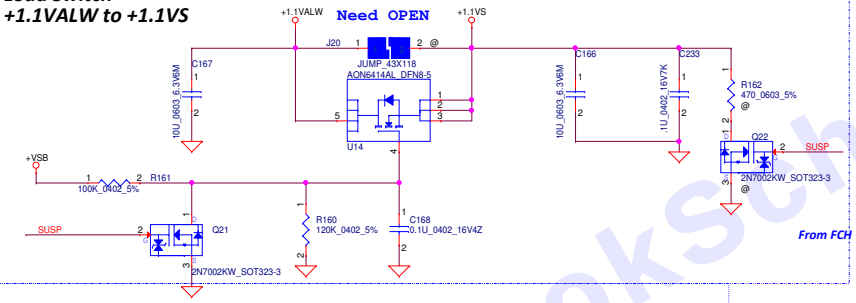
R164 and R165 to adjust 3VALW and 5VALW timing

Delete +3VALW To +3VALW_FCH on 20131001

Load Switch
+1.1VALW to +1.1VS

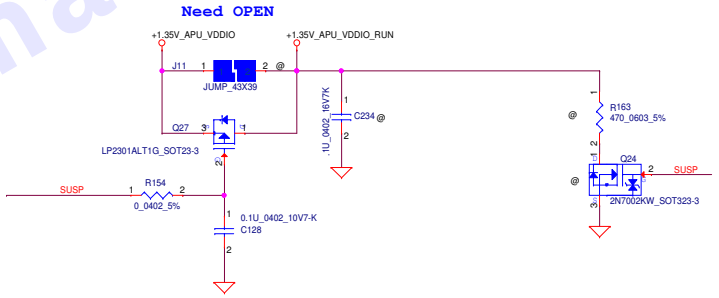
1.1VS :4A

Update Load Switch +1.1VALW to +1.1VS to AON6414AL on 20130926

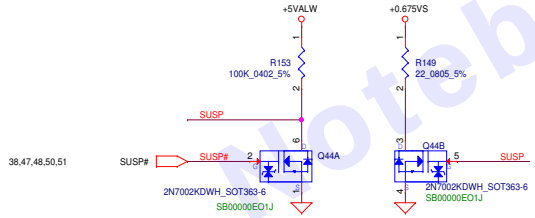


From FCH

+VDDIO to +VDDIO_RUN



For DisCharge



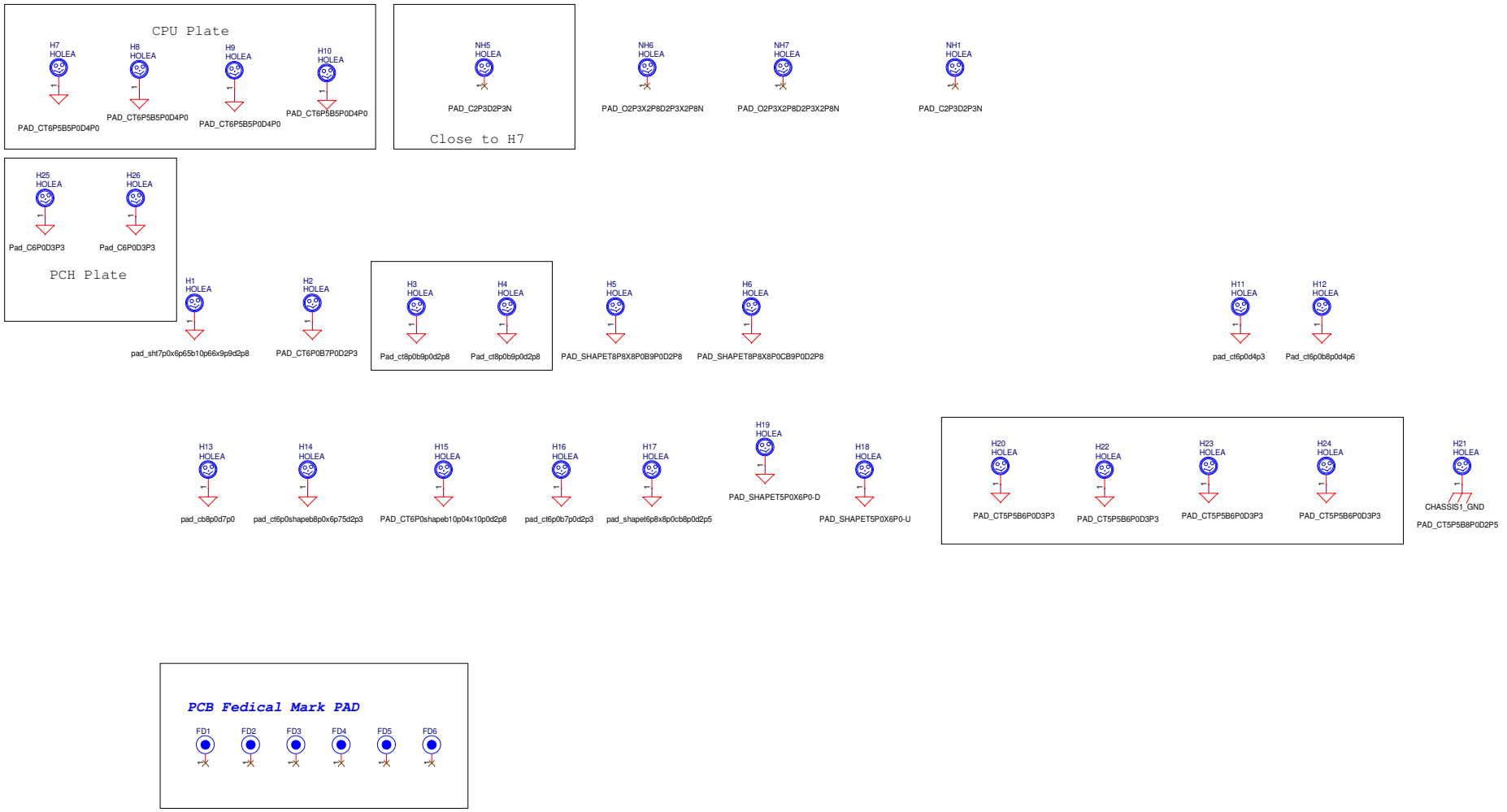
Short +1.35V_DDR_VDDIOSUS & +1.35V_APU_VDDIO directly on 20130930

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: DC V TO VS INTERFACE

Size	Document Number	Rev
C	ACLU7	0.1

Date: Monday, December 16, 2013 Sheet 39 of 52

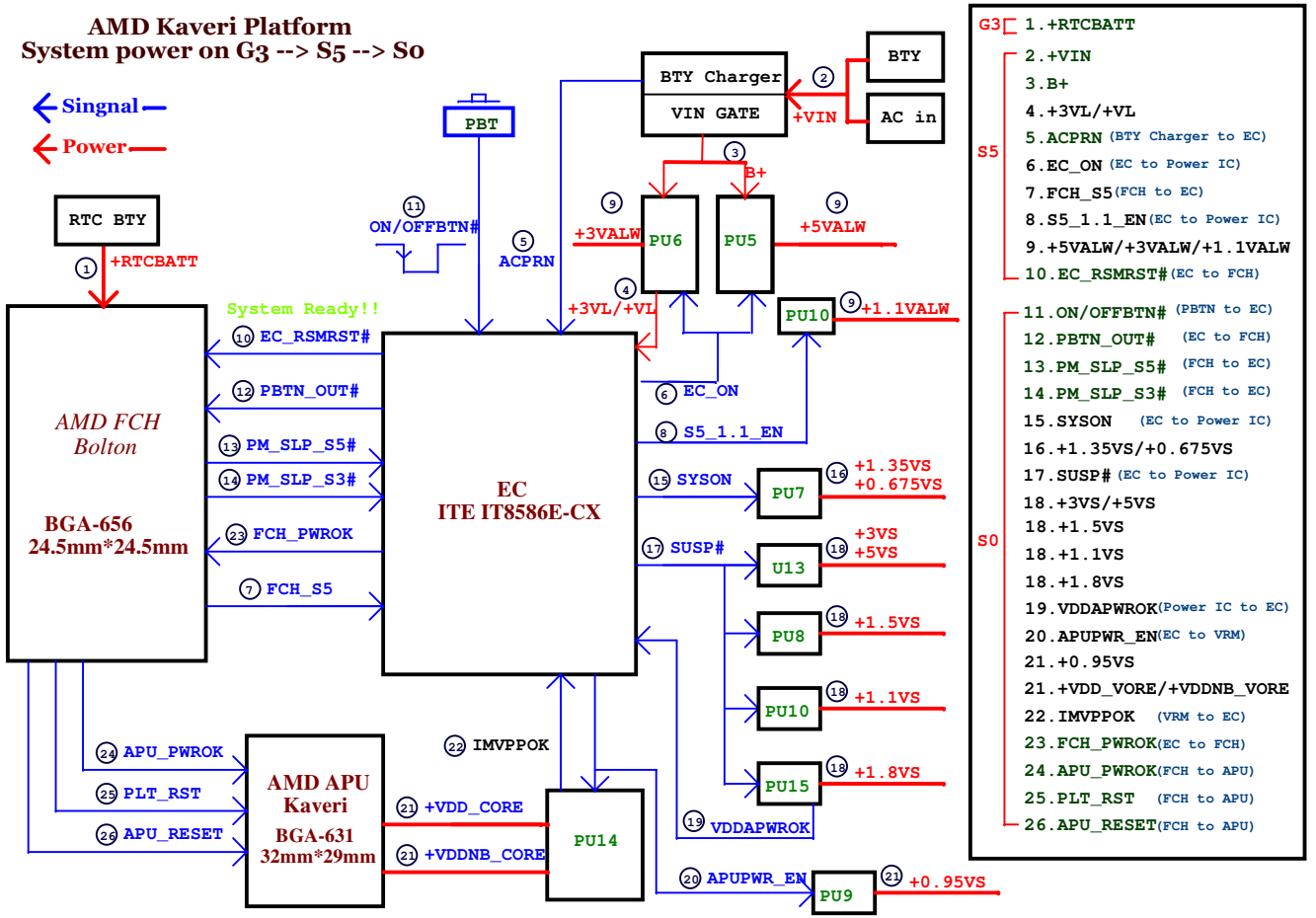


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: SCREW

Size	Document Number	Rev
Custom	ACLU7	1.A
Date: Monday, December 16, 2013	Sheet 40 of 52	

AMD Kaveri Platform
System power on G3 --> S5 --> S0



G3
1. +RTCBATT

S5
2. +VIN
3. B+
4. +3VL/+VL
5. ACPRN (BTY Charger to EC)
6. EC_ON (EC to Power IC)
7. FCH_S5 (FCH to EC)
8. S5_1.1_EN (EC to Power IC)
9. +5VALW/+3VALW/+1.1VALW
10. EC_RSMRST# (EC to FCH)

S0
11. ON/OFFBTN# (PBTN to EC)
12. PBTN_OUT# (EC to FCH)
13. PM_SLP_S5# (FCH to EC)
14. PM_SLP_S3# (FCH to EC)
15. SYSON (EC to Power IC)
16. +1.35VS/+0.675VS
17. SUSP# (EC to Power IC)
18. +3VS/+1.5VS/+1.1VS/+1.8VS
19. VDDAPWROK (Power IC to EC)
20. APUPWR_EN (EC to VRM)
21. +0.95VS/+VDD_VORE/+VDDNB_VORE
22. IMVPPOK (VRM to EC)
23. FCH_PWROK (EC to FCH)
24. APU_PWROK (FCH to APU)
25. PLT_RST (FCH to APU)
26. APU_RESET (FCH to APU)

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: *Power sequence block*

Size: D	Document Number: ACL07		Rev: 0.1
Date: Monday, December 16, 2013		Sheet 41 of 52	

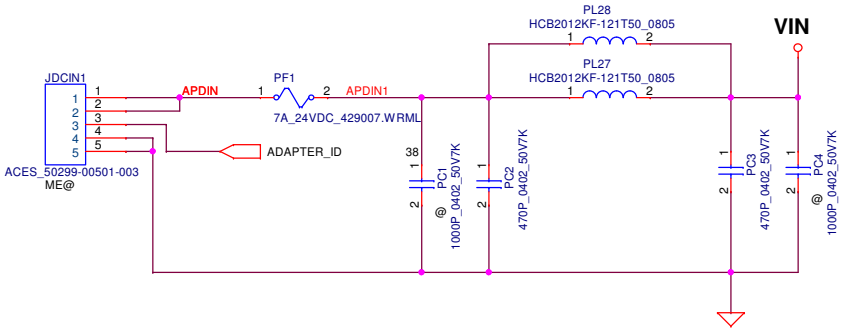
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

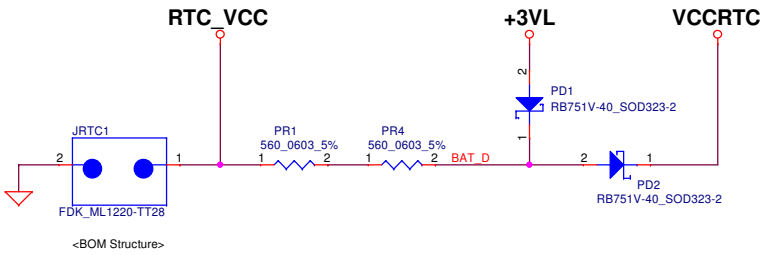
Title

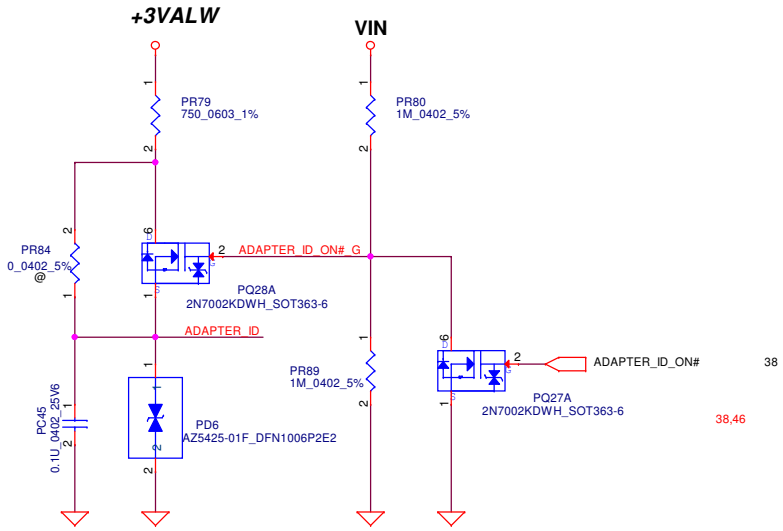
Virtual symbol

Size	Document Number	Rev
B	ACLU7	0.1

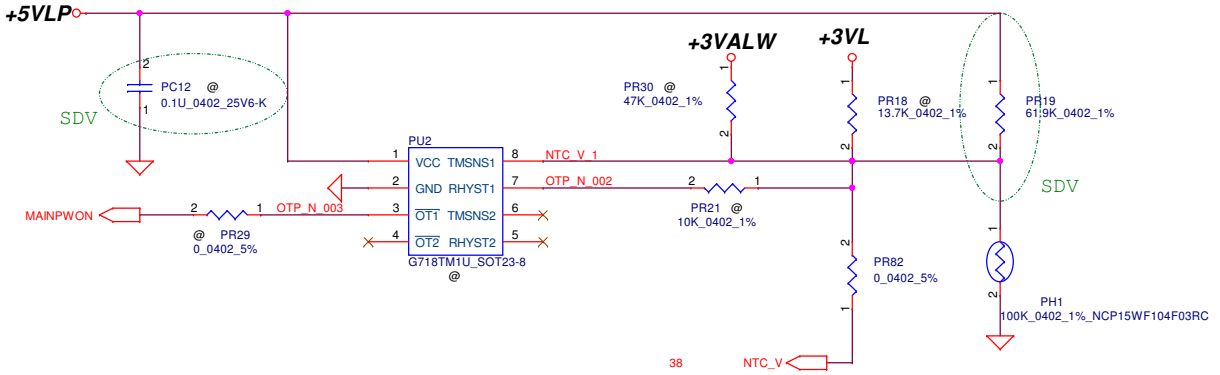
Date: Monday, December 16, 2013 Sheet 42 of 52







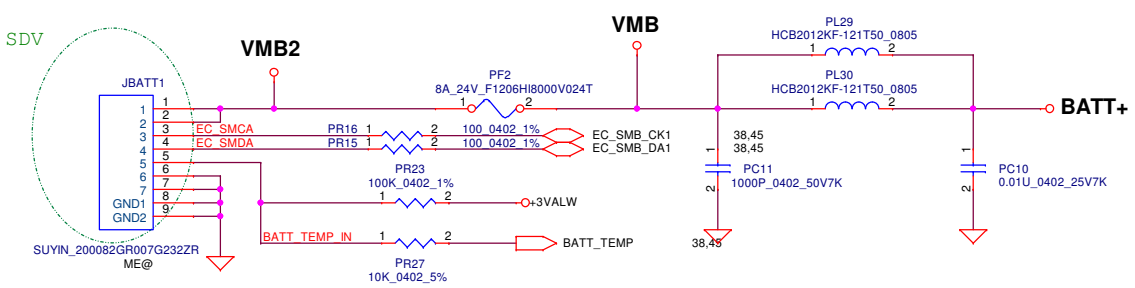
PH1 under CPU botten side :
CPU thermal protection at 92+-3 degree C
Recovery at 56 +-3 degree C



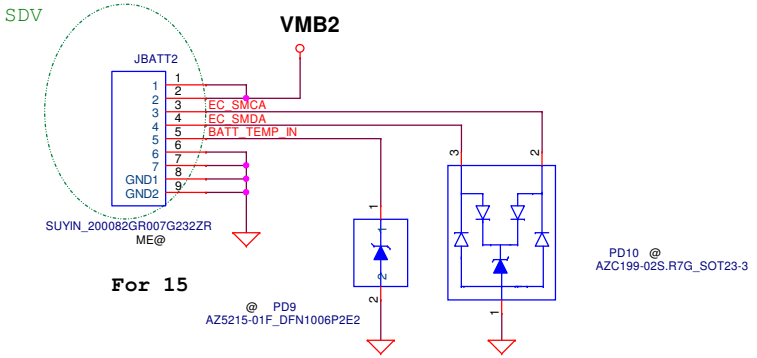
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: ***DCIN / RTC***

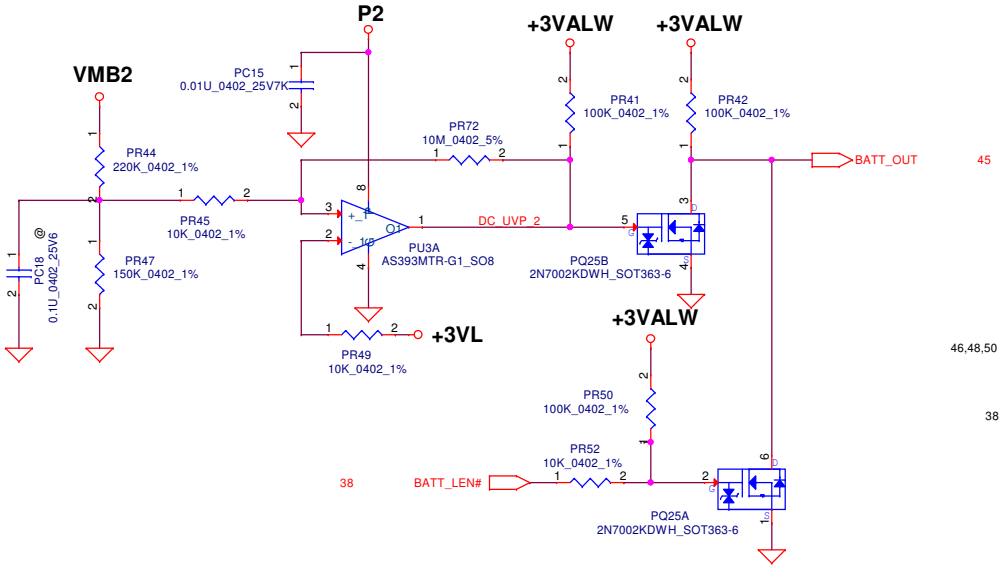
Size	Document Number	Rev
Custom	G(AMD Beema)	0.1
Date: Monday, December 16, 2013	Sheet 43 of 43	

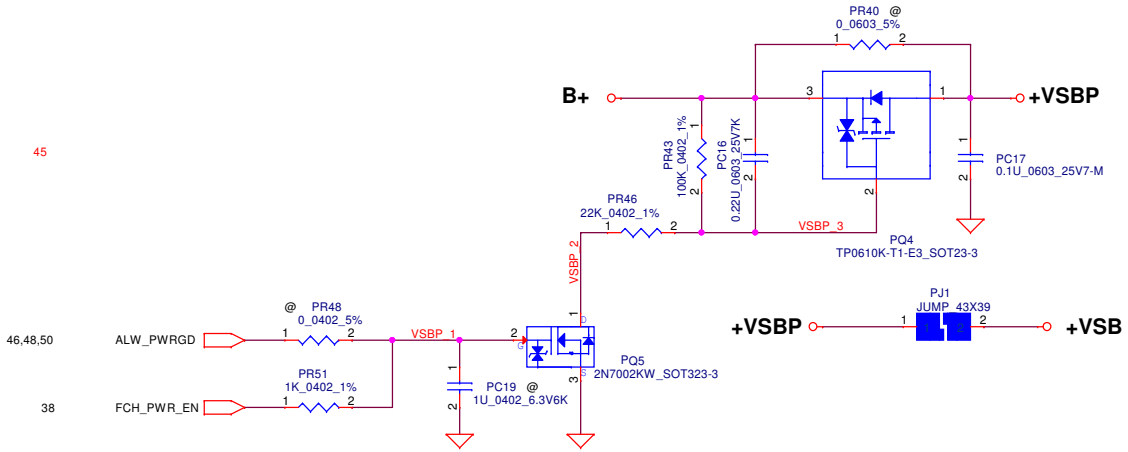


For 14



For 15



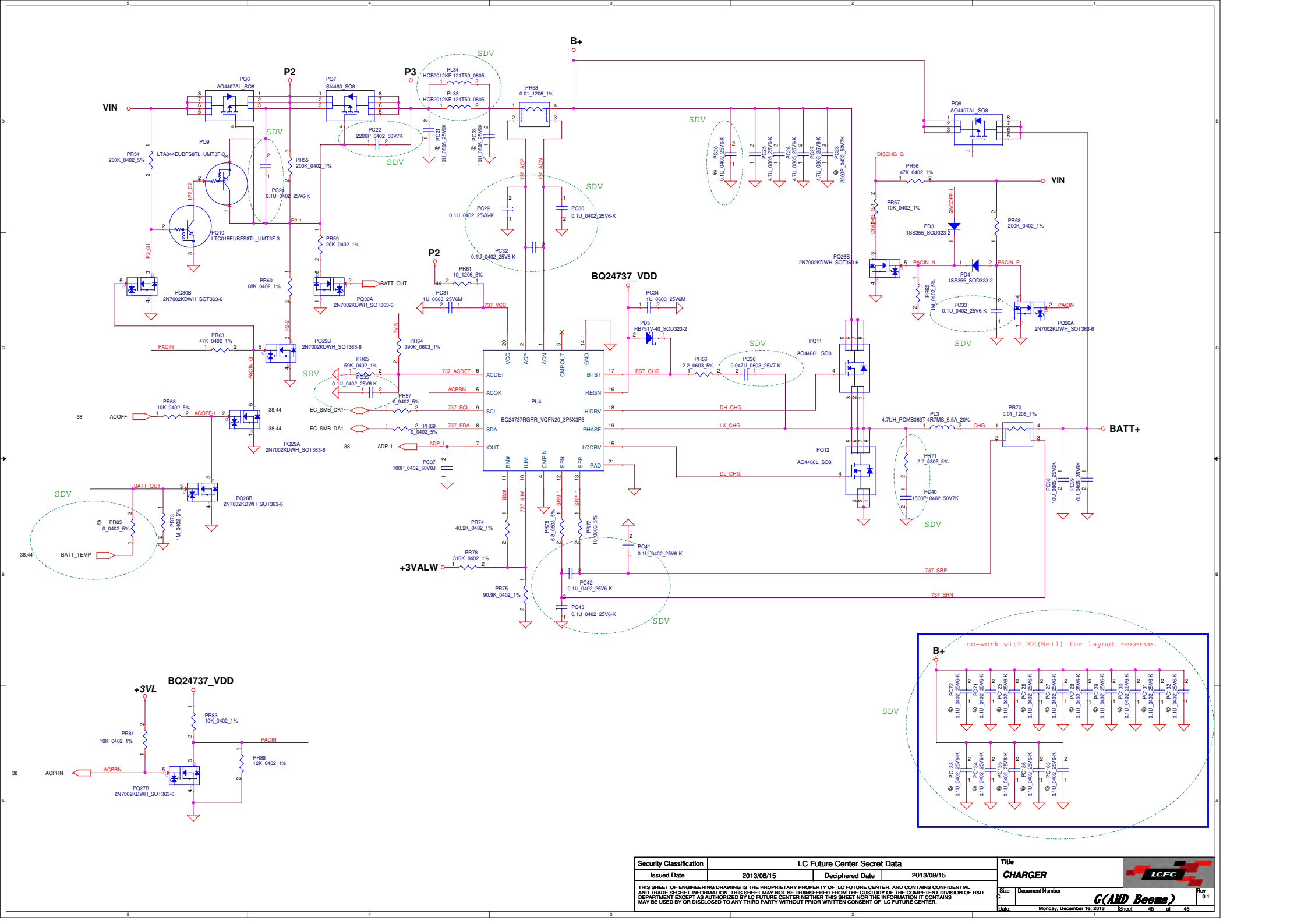


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	G(AMD Beema)	0.1

Date: Monday, December 16, 2013 | Sheet 44 of 44


B+
VIN
P2
P3
BQ24737_VDD
BATT+
BATT_OUT
PACIN
ACOFF
ACPRN
BATT_TEMP
+3VALW
+3VL
SDV
PQ6 AO4407AL_SO8
PQ7 SI4483_SO8
PQ8 AO4407AL_SO8
PQ9 LTA044EUBFS8TL_UMT3F-3
PQ10 LTC015EUBFS8TL_UMT3F-3
PQ11 AO4466L_SO8
PQ12 AO4466L_SO8
PQ26B 2N7002KDWH_SOT363-6
PQ26A 2N7002KDWH_SOT363-6
PQ30B 2N7002KDWH_SOT363-6
PQ30A 2N7002KDWH_SOT363-6
PQ29B 2N7002KDWH_SOT363-6
PQ29A 2N7002KDWH_SOT363-6
PQ28B 2N7002KDWH_SOT363-6
PQ27B 2N7002KDWH_SOT363-6
PU4 BQ24737RGRR_VQFN20_3P5X3P5
PL34 HCB2012KF-121T50_0805
PL33 HCB2012KF-121T50_0805
PL3 4.7UH_PCMB063T-4R7MS_5.5A_20%
PD3 1SS355_SOD323-2
PD4 1SS355_SOD323-2
PD5 RB751V-40_SOD323-2
co-work with EE(Neil) for layout reserve.
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/15
Deciphered Date
2013/08/15
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Title
CHARGER
Size
C
Document Number
G(AMD Beema)
Rev
0.1
Date:
Monday, December 16, 2013
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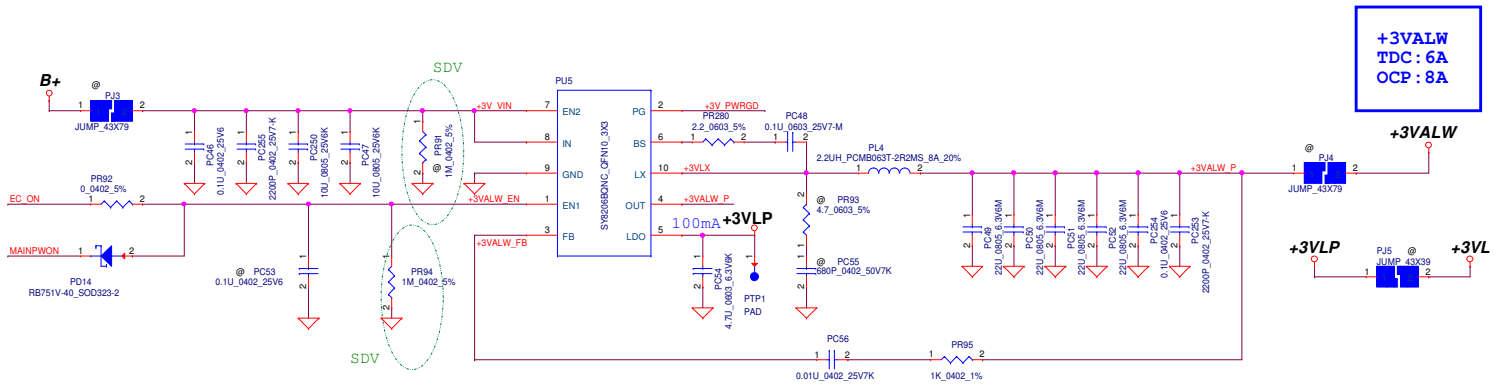
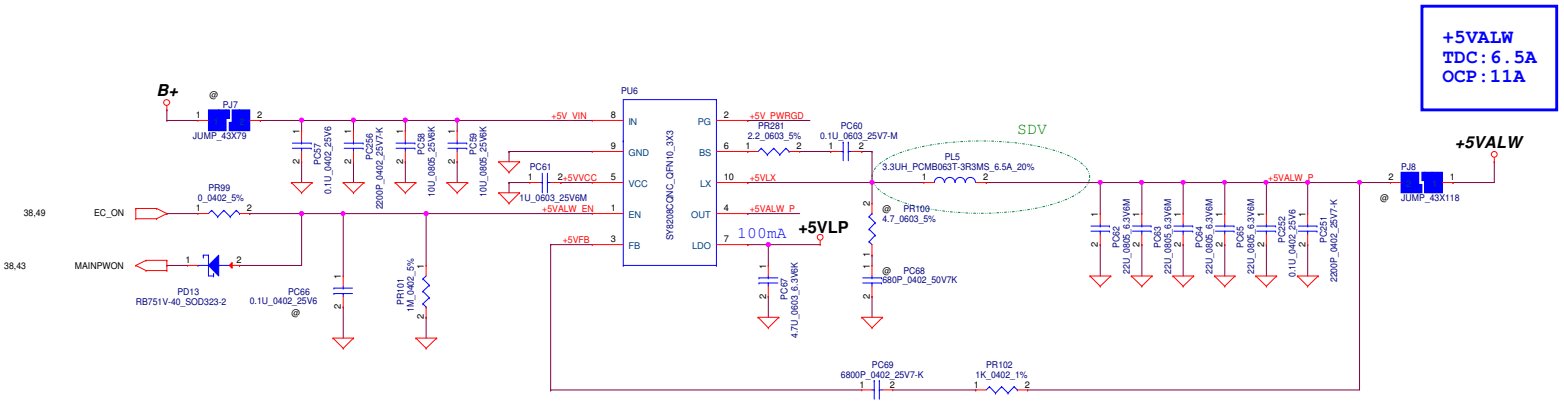
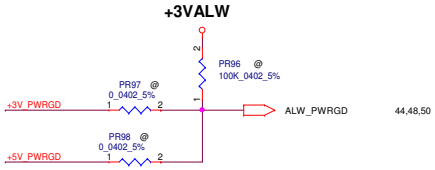
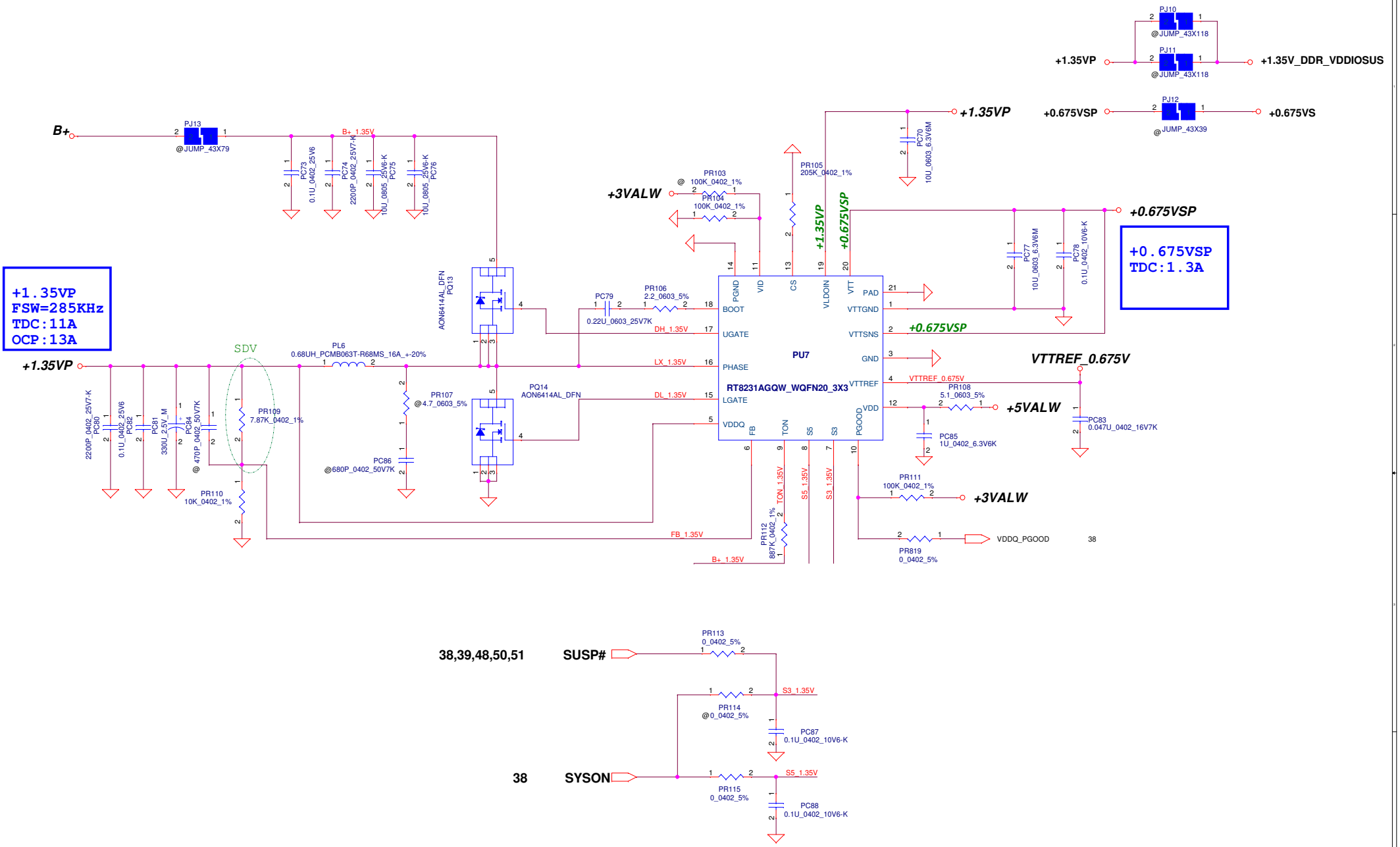






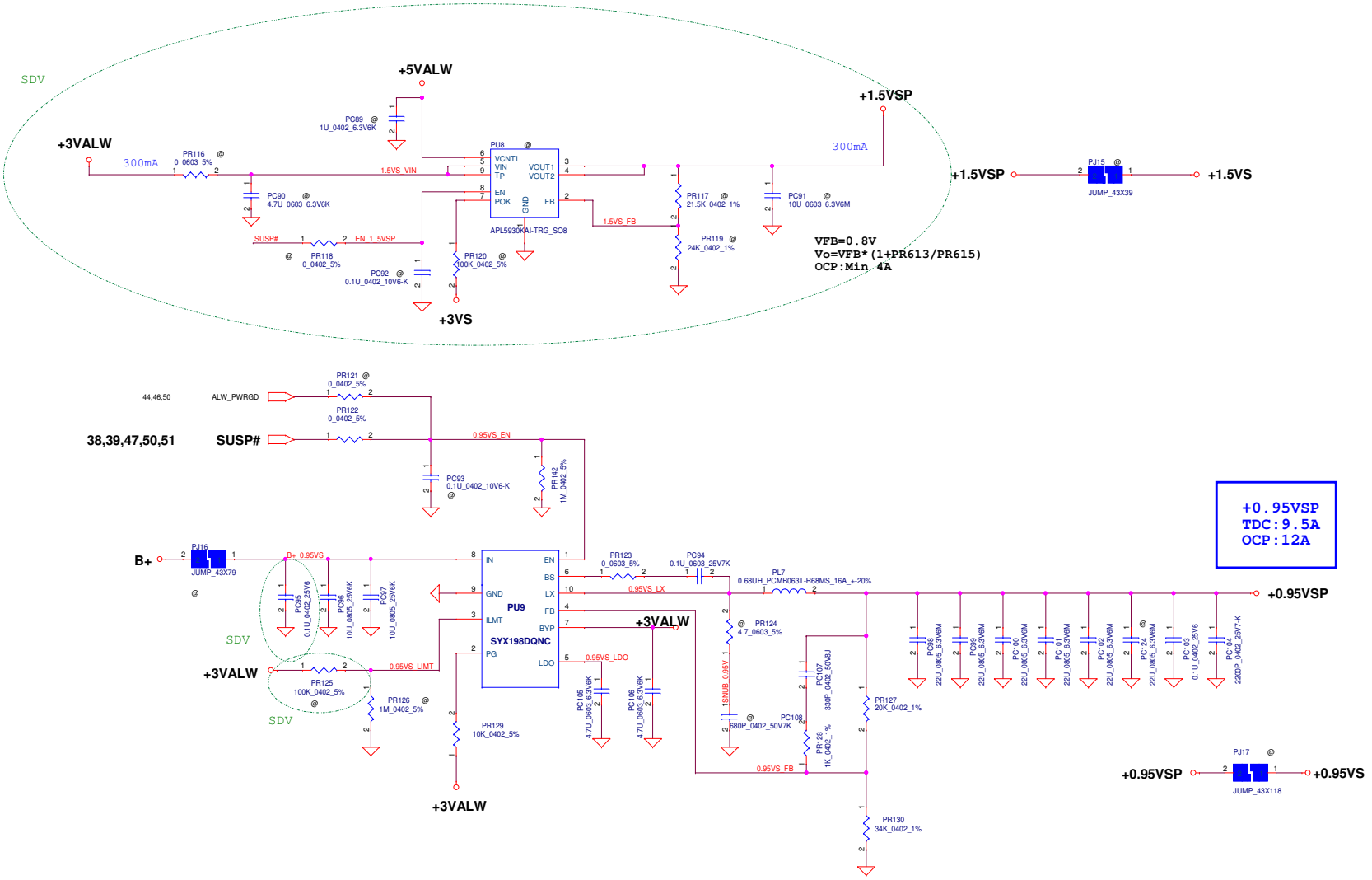
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	PWR_3VALW/5VALW		
Size	Document Number		Rev
C	G(AMD Beema)		0.1
Date:	Monday, December 16, 2013	Sheet	46 of 46



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/01	Deciphered Date	2014/08/01

Title	+1.35VP/+0.675VSP		
Size: Custom	Document Number: AAVE1		Rev: 0.1
Date: Monday, December 16, 2013	Sheet 47 of 47		



Current limit setting pin. The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

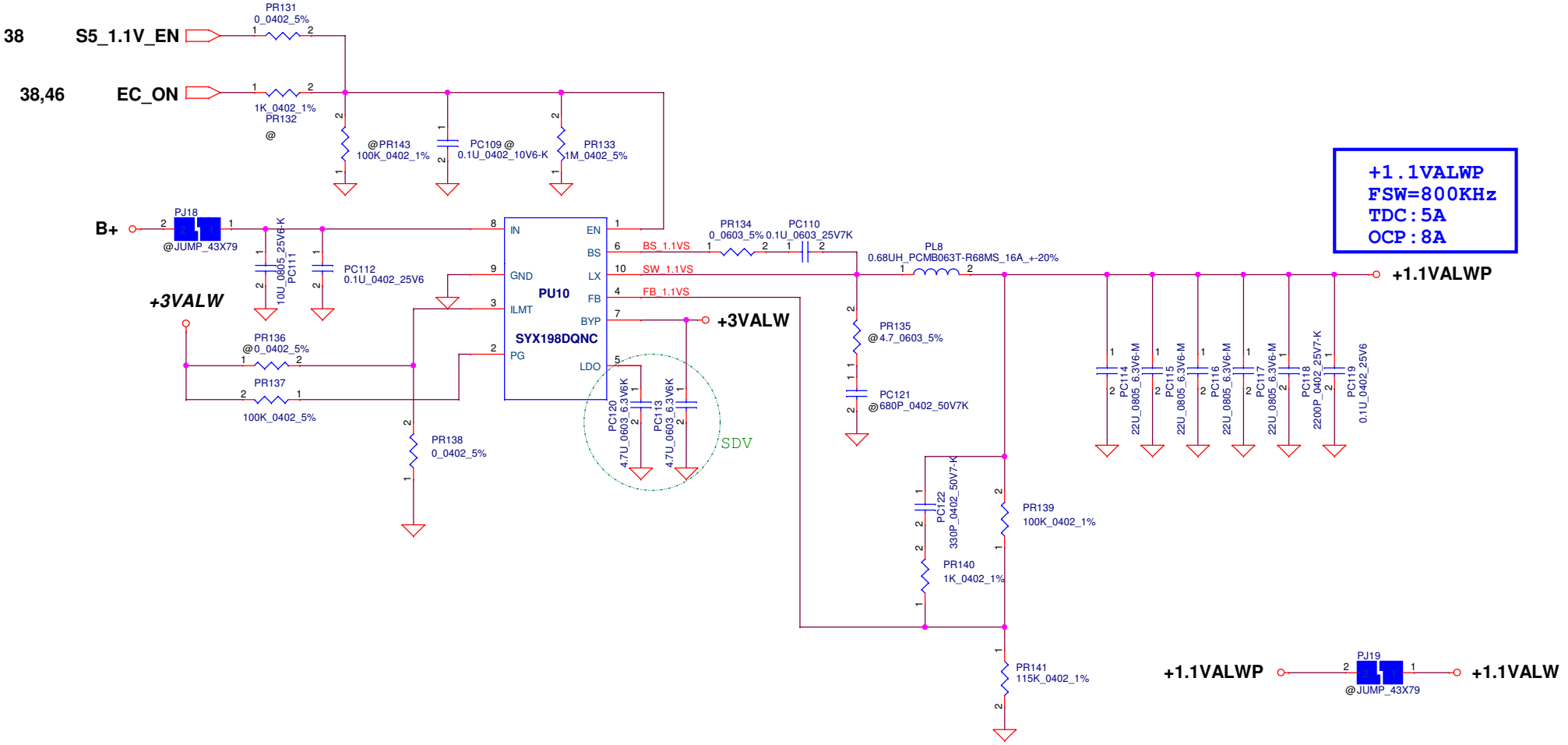
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: *+1.35VS_VGA/+1.5VS*

LCFC

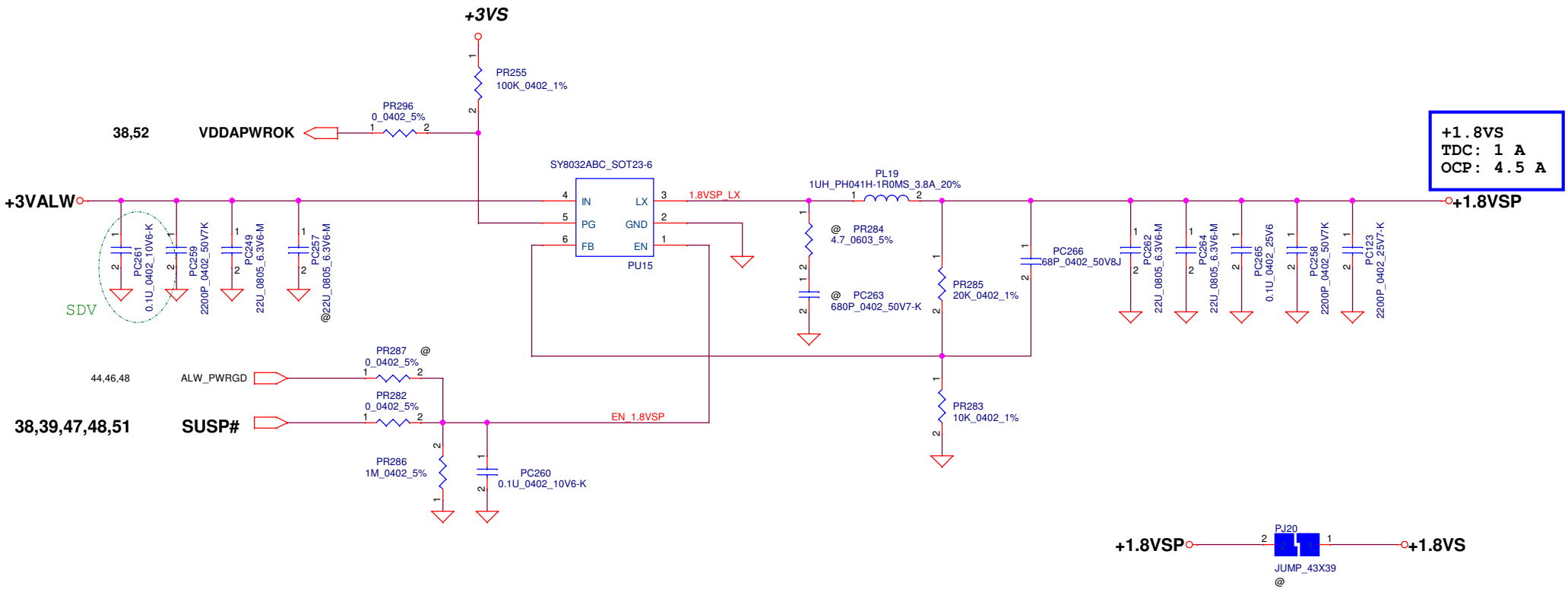
Size	Document Number	Rev
D	G(AMD Beema)	0.1

Date: Monday, December 16, 2013 Sheet 48 of 48



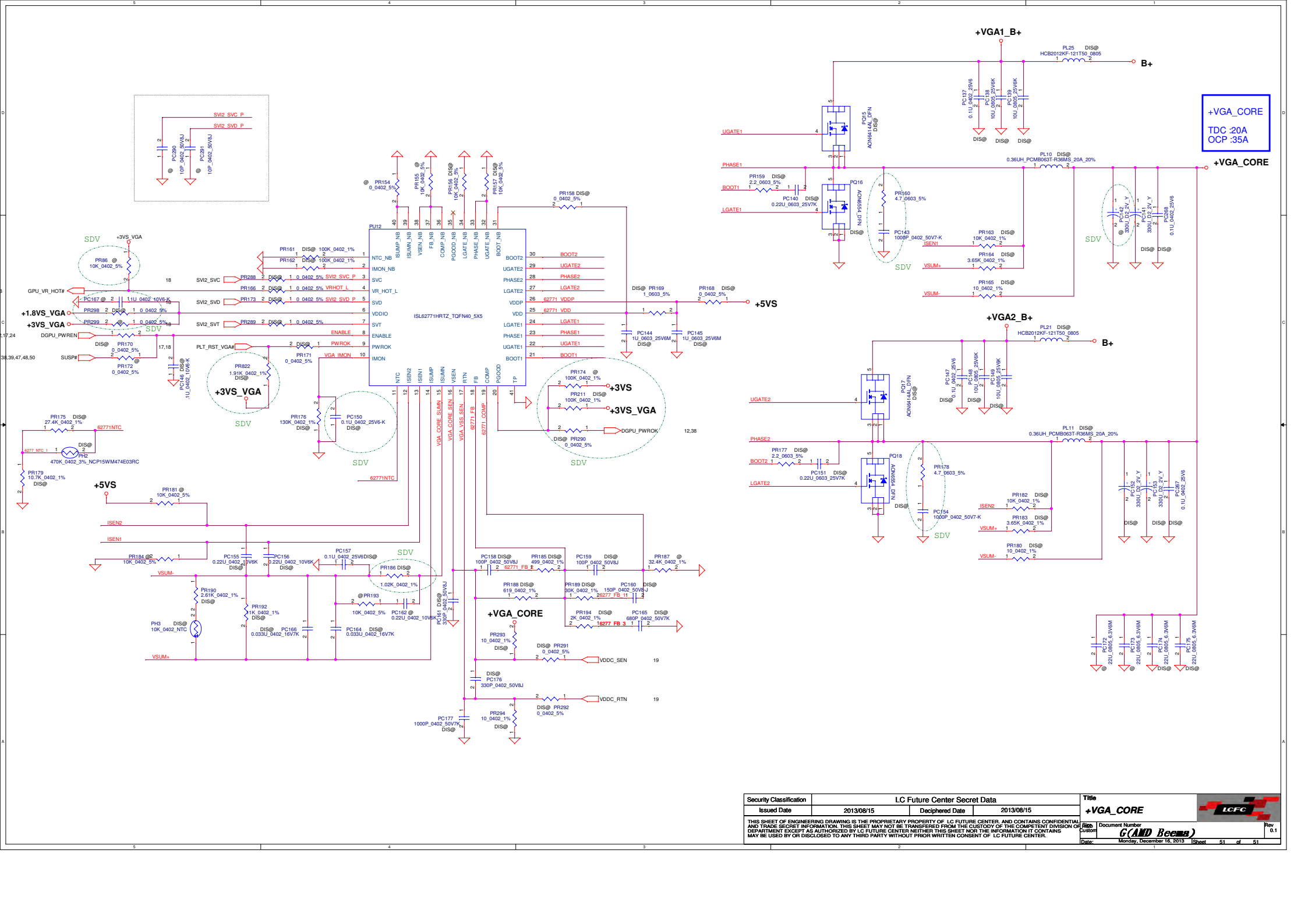
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/01	Deciphered Date	2014/08/01

Title	*+1.1VALWP*		
Size B	Document Number AAVE1		Rev 0.1
Date: Monday, December 16, 2013	Sheet 49 of 49		



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	+1.05VS/+1.05VS_VGA		
Size	Document Number		Rev
B	G(AMD Beema)		0.1
Date:	Monday, December 16, 2013	Sheet	50 of 50


+VGA_CORE
TDC :20A
OCP :35A
ISL62771HRTZ_TQFN40_5X5
+VGA1_B+
+VGA2_B+
B+
+5VS
+3VS
+3VS_VGA
+1.8VS_VGA
+VGA_CORE
SDV
SVI2_SVC_P
SVI2_SVD_P
GPU_VR_HOT#
DGPU_PWREN
SUSP#
PLT_RST_VGA#
DGPU_PWROK
VDDC_SEN
VDDC_RTN
VSUM-
VSUM+
ISEN1
ISEN2
62771NTC
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/15
Deciphered Date
2013/08/15
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Title
+VGA_CORE
Size
Custom
Document Number
G(AMD Beema)
Rev
0.1
Date:
Monday, December 16, 2013
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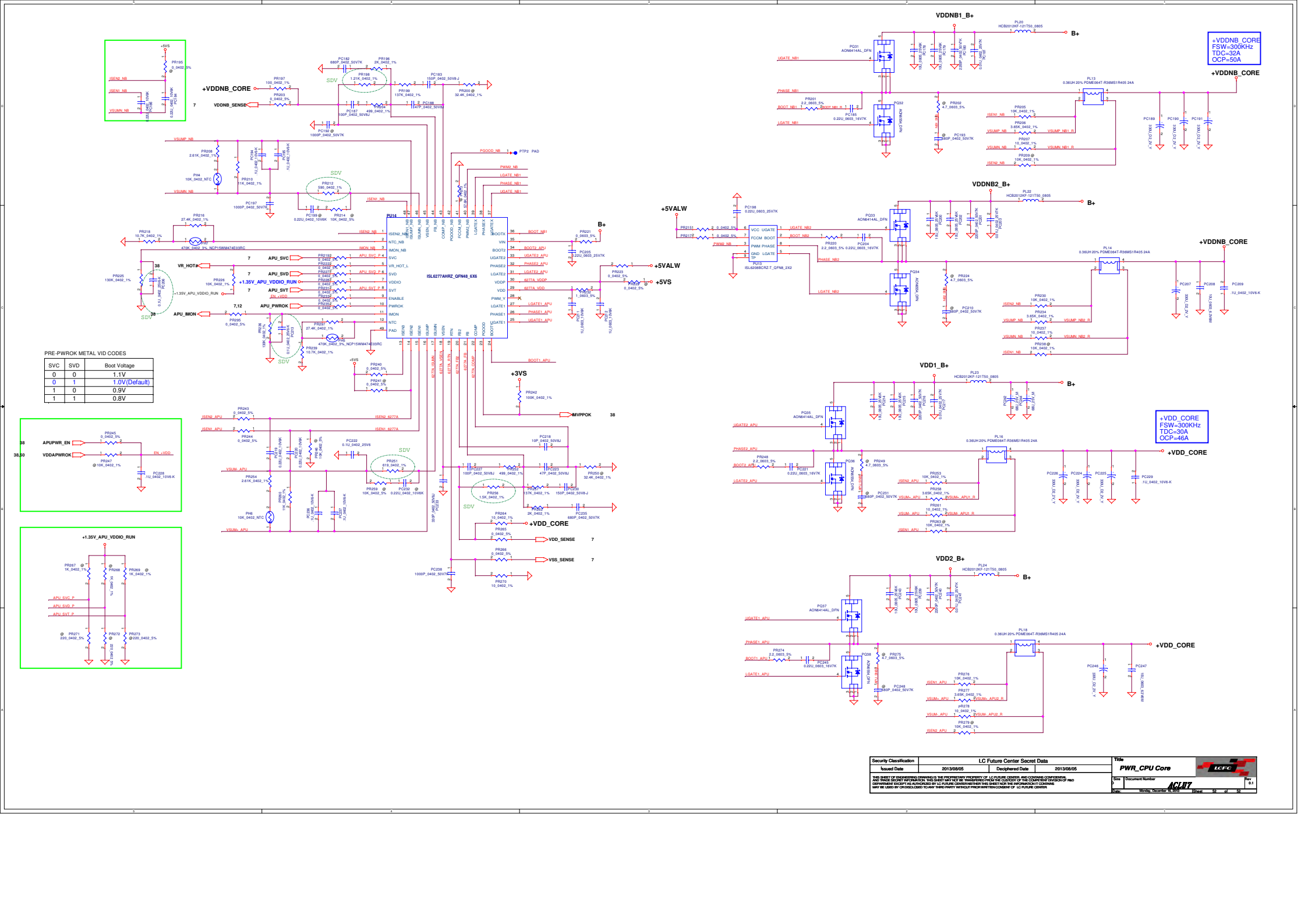
+VDDNB_CORE
FSW=300KHz
TDC=32A
OCP=50A
+VDD_CORE
FSW=300KHz
TDC=30A
OCP=46A
ISL6277AHRZ_QFN48_6X6
PU14
PU13
ISL6268CRZ-T_QFN8_2X2
VDDNB1_B+
VDDNB2_B+
VDD1_B+
VDD2_B+
B+
+5VALW
+5VS
+3VS
+VDDNB_CORE
+VDD_CORE
VDDNB_SENSE
VDD_SENSE
VSS_SENSE
VR_HOT#
APU_SVC
APU_SVD
APU_SVT
APU_PWROK
APU_IMON
+1.35V_APU_VDDIO_RUN
APUPWR_EN
VDDAPWROK
PRE-PWROK METAL VID CODES
SVC SVD Boot Voltage
0 0 1.1V
0 1 1.0V(Default)
1 0 0.9V
1 1 0.8V
Security Classification
LC Future Center Secret Data
Issued Date 2013/08/05
Deciphered Date 2013/08/05
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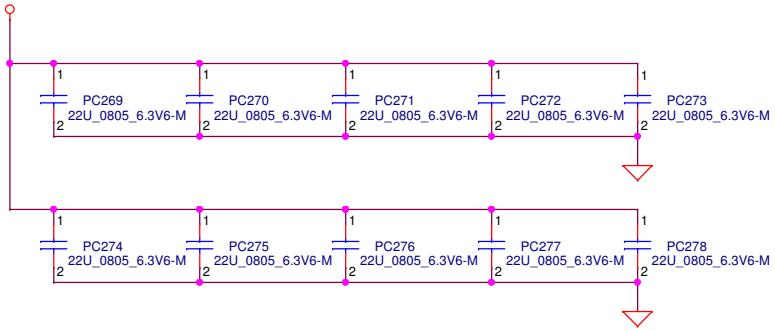
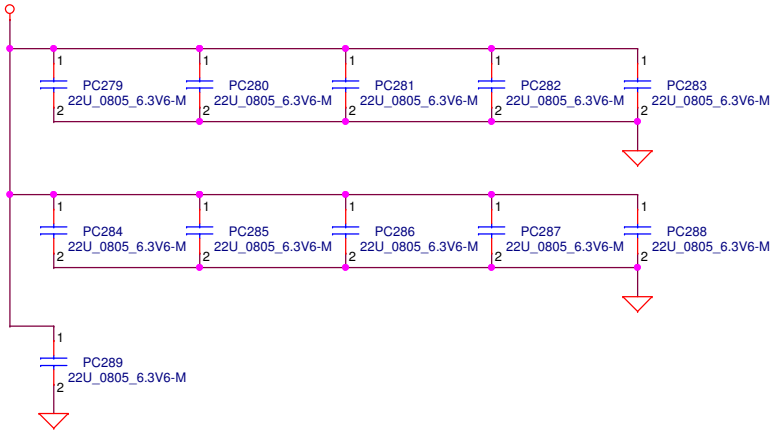
Title
PWR_CPU Core
Size D
Document Number
Rev 0.3
Date: Monday, December 16, 2013
Sheet 52 of 52

+VDDNB_CORE



+VDD_CORE



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/01	Deciphered Date	2014/08/01

Title: VCCCPUCORE DECOUPLING

Size	Document Number	Rev
B	AAVE1	0.1

Date: Monday, December 16, 2013 Sheet 53 of 53