UM8 UMA SYSTEM DIAGRAM

+3V/+5V PG.34
+1.05V/+1.8V PG.36
CPU Core PG.39
VGA Core/+1.1V PG.38
+1.5V/+0.75V PG.35
+1.05VTT PG.37
UMA VGACORE
Charger PG.33

14.318MHz
CLOCK GEN PG.2

SODIMM1 Max. 4GB PG.12 — DDR3 Channel A
SODIMM2 Max. 4GB PG.13 — DDR3 Channel B

INTEL Arrandale
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.3~6

FDI
DMI

PI3VDP411LSZDE PG.27 — HDMI — HDMI PG.24

DB1
CRT — CRT

LVDS — LVDS PG.22

4M ROM PG.26

FAN & THERMAL
GMT G990/
EMC1422-1-AIZL-TR PG.30

DB2

INTEL PCH
Ibex Peak-m
27mm X 25mm
1071pin FCBGA
TDP 5W
PG.7~11

LANE0
WWAN — USB 2.0 PORT5

PCI-E x 1
LANE6
LAN Atheros/AR8152 10/100
LANE1
WLAN — USB 2.0 PORT4

PCI-E x 1
LANE5
eSATA SN75LVCP412 Combo port PG.27 — USB 2.0 PORT8

SATA0 — HDD PG.28
SATA1 — ODD PG.28

USB2.0 X1 — PORT0,1,7
USB2.0 X1 — PORT0,1,7
Webcam PG.22 — PORT11
USB 2.0
PORT12 — Card Reader RTS5138 PG.23
PORT9 — BT BT365 PG.32

LPC
KBC ITE 8502 PG.25
KB PG.28
TP PG.28
1M ROM PG.26

Azalia
AUDIO CODEC ALC269-GR
Speaker PG.31
HP/MIC
Analog MIC

Stackup
TOP
VCC
IN1
IN2
GND
BOT

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25mA

+1.05V_PCH — L14 HCB1608KF-181T15_6 — +VDDIO_CLK

C113 0.1U/ 10V/X7R
C109 0.1U/ 10V/X7R
C112 10U/6.3V_8/X5R

Place each 0.1uF cap close to pin

8/20 Wait Victor check

300mA

+3.3V_RUN — L13 HCB1608KF-181T15_6 — +VDDSE_CLK

C106 10U/6.3V_8/X5R
C101 0.1U/ 10V/X7R
C110 0.1U/ 10V/X7R
C108 0.1U/ 10V/X7R
C107 0.1U/ 10V/X7R
C111 0.1U/ 10V/X7R

Place each 0.1uF cap close to pin

PDC (Power Cap quantities follow UM3)

Check CLK P/N and footprint

U6 — 9LRS3197 — QFN32

+VDDSE_CLK → VDD_LCD, VDD_REF
+VDDIO_CLK → VDD_CPU_IO, VDD_SRC_IO
VDD_USB, VDD_SRC, VDD_CPU

25,30 SMBDAT2 → SDATA
25,30 SMBCLK2 → SCLK

+3.3V_RUN — R113 10K — R99 33/J_4 — CPU_SEL
8 CLK_PCH_14M → CLK_PCH_14M
C96 *10P/50V_4_NC/COG

Place R8044 within 0.5" of C/G

CK_PWRGD_R → CK_PWRGD/PD#_3.3
XTAL_OUT, XTAL_IN → XOUT, XIN
VSS_SATA, VSS_USB, VSS_LCD

CPU_STOP#, REF_0/CPU_SEL
SATA, SATA#
27MHz_nonSS, 27MHz_SS
DOT96T_LPR, DOT96C_LPR
CPU-0, CPU-0#, CPU-1, CPU-1#
GND, VSS_REF, VSS_CPU, VSS_SRC

Place within 0.5" of C/G

RP4: CLK_BUF_BCLKP_R, CLK_BUF_BCLKN_R → CLK_BUF_BCLKP 8, CLK_BUF_BCLKN 8
RP5: CLK_BUF_DREFCLKP_R, CLK_BUF_DREFCLKN_R → CLK_BUF_DREFCLKP 8, CLK_BUF_DREFCLKN 8
RP6: CLK_BUF_PCIE_3GPLLP_R, CLK_BUF_PCIE_3GPLLN_R → CLK_BUF_PCIE_3GPLLP 8, CLK_BUF_PCIE_3GPLLN 8
RP7: CLK_BUF_DREFSSCLKP_R, CLK_BUF_DREFSSCLKN_R → CLK_BUF_DREFSSCLKP 8, CLK_BUF_DREFSSCLKN 8
0X2

Discrete only

SLG: SLG8SP590VTR Seligo QPN: AL8SP590000
SLG: SLG8SP585VTR Seligo QPN: AL8SP585000
RSC: RTM875N-632-VB-GRT Realtek QPN: AL000875002

+3.3V_RUN
R107 *10K_NC
CPU_SEL
R101 10K

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

BOM check

+3.3V_RUN
R106 1K/J_4
CK_PWRGD_R
Q14 FDN357N
39 VR_PWRGD_CLKEN#
R105 *100K/F_4_NC

R8253 => UM7 POP
UM9 DE-POP
0918 check

Y4 14.318MHZ
XTAL_IN — XTAL_OUT
C99 33P/50V_4/NPO
C100 33P/50V_4/NPO

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	Clock Gen(9LRS3197)/HOLES	1A
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DPLL_REF_SSCLK/DPLL_REF_SSCLK#:
Embedded Display Port PLL Differential Clock in.

	DIS	UMA
DPLL_REF_SSCLK	GND	PCH
DPLL_REF_SSCLK#	GND	PCH

03

U15A

DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3 → DMI_RX#[0] DMI_RX#[1] DMI_RX#[2] DMI_RX#[3]
DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3 → DMI_RX[0] DMI_RX[1] DMI_RX[2] DMI_RX[3]
DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3 → DMI_TX#[0] DMI_TX#[1] DMI_TX#[2] DMI_TX#[3]
DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3 → DMI_TX[0] DMI_TX[1] DMI_TX[2] DMI_TX[3]

DMI

FDI_TXN0 FDI_TXN1 FDI_TXN2 FDI_TXN3 FDI_TXN4 FDI_TXN5 FDI_TXN6 FDI_TXN7 → FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]
FDI_TXP0 FDI_TXP1 FDI_TXP2 FDI_TXP3 FDI_TXP4 FDI_TXP5 FDI_TXP6 FDI_TXP7 → FDI_TX[0] FDI_TX[1] FDI_TX[2] FDI_TX[3] FDI_TX[4] FDI_TX[5] FDI_TX[6] FDI_TX[7]
FDI_FSYNC0 FDI_FSYNC1 → FDI_FSYNC[0] FDI_FSYNC[1]
FDI_INT → FDI_INT
FDI_LSYNC0 FDI_LSYNC1 → FDI_LSYNC[0] FDI_LSYNC[1]

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI B26 — PEG_COMP R316 49.9/F_4
PEG_ICOMPO A26
PEG_RCOMPO B27
PEG_RBIAS A25 — PEG_RBIAS R315 750/F_4

PEG_RX#[0..15] → K35 J34 J33 G35 G32 F34 F31 D35 E33 C33 D32 B32 C31 B28 B30 A31
PEG_RX[0..15] → J35 H34 H33 E35 G33 E34 E32 D34 F33 B33 D31 A32 C30 A28 B29 A30
PEG_TX#[0..15] → L33 M35 M33 M30 L31 K32 M29 J31 K29 H30 H29 F29 E28 D29 D27 C26
PEG_TX[0..15] → L34 M34 M32 L30 M31 K31 M28 H31 K28 G30 G29 F28 E27 D28 C27 C25

IC,AUB_CFD_rPGA,R1P0

H_PWRGOOD — C259 *100P_NC

H_VTTPWRGD — C278 *100P_NC

U15B

MISC
COMP3 COMP2 COMP1 COMP0 SKTOCC#
R117 20/F_4 H_COMP3 AT23
R115 20/F_4 H_COMP2 AT24
R118 49.9/F_4 H_COMP1 G16
R116 49.9/F_4 H_COMP0 AT26
25 H_CPUDET# AH24

THERMAL
CATERR# PECI PROCHOT# THERMTRIP#
H_CATERR# AK14
10 H_PECI AT15
H_PROCHOT# AN26
10 H_THERM AK15

PWR MANAGEMENT
RESET_OBS# PM_SYNC VCCPWRGOOD_1 VCCPWRGOOD_0 SM_DRAMPWROK TAPPWRGOOD VTTPWRGOOD RSTIN#
H_CPURST# AP26
9 PM_SYNC AL15
TP30 AN14
10 H_PWRGOOD H_PWRGOOD AN27
9 PM_DRAM_PWRGD AK13
AM26
32 H_VTTPWRGD H_VTTPWRGD AM15
9,25,31 PLTRST# CPU_PLTRST# AL14
R139 1.5K/F_4
R137 750/F_4
TP35

TP24 TP25 TP19 TP23 TP26 TP29 TP18 TP27 → AJ22 AK22 AK24 AJ24 AJ25 AH22 AK23 AH23
BPM#[0..7]

JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

CLOCKS
BCLK BCLK# → A16 B16 → TP48 TP49 → CLK_CPU_BCLKP 10, CLK_CPU_BCLKN 10
BCLK_ITP BCLK_ITP# → A30 AT30 → For ITP Clk
PEG_CLK PEG_CLK# → E16 D16 → CLK_PCIE_3GPLLP 8, CLK_PCIE_3GPLLN 8
DPLL_REF_SSCLK DPLL_REF_SSCLK# → A18 A17 → R317 *0_NC, R318 *0_NC → CLK_DREFSSCLKP 8, CLK_DREFSSCLKN 8

DDR3 MISC
SM_DRAMRST# → F6 → DDR3_DRAMRST# 12,13
SM_RCOMP[0] SM_RCOMP[1] SM_RCOMP[2] → AL1 AM1 AN1 → SM_RCOMP_0 R319 100/F_4, SM_RCOMP_1 R320 24.9/F_4, SM_RCOMP_2 R321 130/F_4
R127 10K/J_4 → +1.05V_VTT
PM_EXT_TS#[0] PM_EXT_TS#[1] → AN15 AP15 → PM_EXTTS#0 12, PM_EXTTS#1 13
R123 10K/J_4, R122 *12.4K/F_NC → +1.05V_VTT

PRDY# PREQ# TCK TMS TRST# TDI TDO TDI_M TDO_M → AT28 AP27 AN28 AP28 AT27 AT29 AR27 AR29 AP29
TP47 TP16
XDP_TCLK → TP14
XDP_TMS → TP15
XDP_TRST# → TP12
XDP_TDI → TP13
XDP_TDO → TP28
XDP_TDI_M → TP21
XDP_TDO_M → TP20

DBR# → AN25 → R103 *0_NC → XDP_DBRESET# 9

+1.05V_VTT
H_CATERR# R119 49.9/F_4
H_PROCHOT# R102 49.9/F_4
CPU_PLTRST# R138 *68/J_4_NC
H_CPURST# R304 *68/J_4_NC

CPU THERMTRIP
+3.3V_RUN
R196 *10M_NC
PM_THRMTRIP# 34
Q12 *2N7002W-7-F_NC
H_THERM
*2.2K/J_4_NC R104
C361 *0.1U_NC
10
Q13 *MMST3904-7-F_NC

+1.5V_SUS
Use a voltage divider with VDDQ (1.5 V) rail (ON in S3) and resistor combination of 1.1K ± (to VDDQ)/3K ± (to GND) to convert to processor VTT level.
R136 1.1K/F
PM_DRAM_PWRGD
R135 3K/F
C277 *100P_NC

JTAG MAPPING
XDP_TDO_M — R100 0 — XDP_TDI_M
XDP_TRST# — R301 51/J_4
Intel Suggest to reserve 0 ohm below for CPU AP29 and AR29 pins. (DS 403777 Page 81)

Quanta Computer Inc.
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	PROCESSER 1/4(HOST&PEX)	1A

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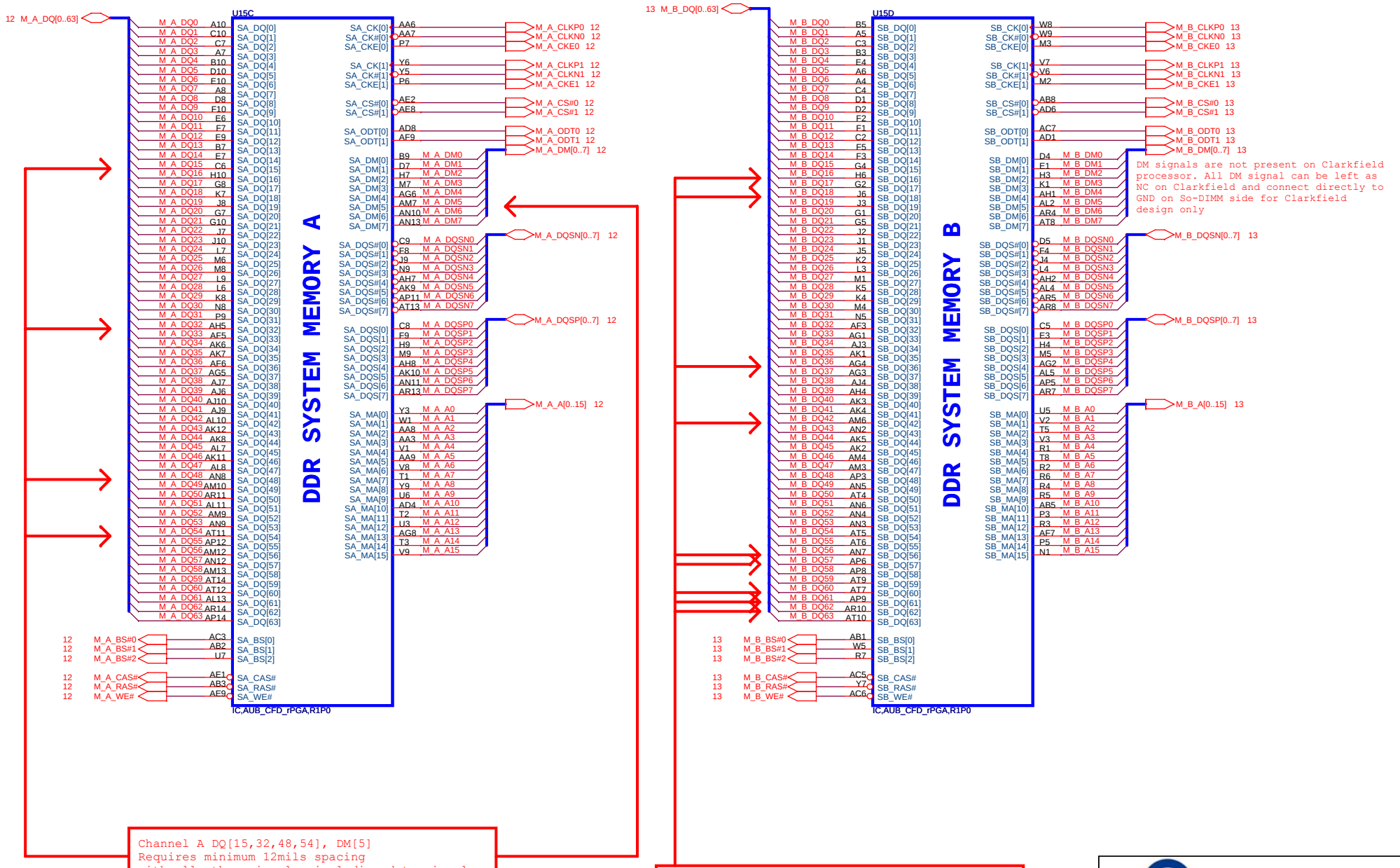
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	1A
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Name different with power

+VCC_CORE

C308 *22U/6.3V_8/X5R_NC
C329 22U/6.3V_8/X5R
C104 *22U/6.3V_8/X5R_NC
C102 22U/6.3V_8/X5R
C116 22U/6.3V_8/X5R
C128 22U/6.3V_8/X5R
C328 22U/6.3V_8/X5R
C117 22U/6.3V_8/X5R
C306 *22U/6.3V_8/X5R_NC
C319 *22U/6.3V_8/X5R_NC
C125 22U/6.3V_8/X5R
C97 22U/6.3V_8/X5R
C103 *10U/6.3V_8/X5R_NC
C330 10U/6.3V_8/X5R
C325 *10U/6.3V_8/X5R_NC
C305 10U/6.3V_8/X5R
C118 *10U/6.3V_8/X5R_NC
C307 10U/6.3V_8/X5R
C326 10U/6.3V_8/X5R
C119 10U/6.3V_8/X5R
C333 10U/6.3V_8/X5R
C320 10U/6.3V_8/X5R
C115 *10U/6.3V_8/X5R_NC
C98 10U/6.3V_8/X5R
C318 *10U/6.3V_8/X5R_NC
C332 10U/6.3V_8/X5R
C105 *10U/6.3V_8/X5R_NC
C122 *10U/6.3V_8/X5R_NC

C304 *470U_NC
C296 *470U_NC

U15F

CPU CORE SUPPLY

POWER

1.1V RAIL POWER

CPU VIDS

SENSE LINES

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

IC,AUB_CFD_rPGA,R1P0

18A

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

+1.05V_VTT

C341 10U/6.3V_8/X5R
C339 10U/6.3V_8/X5R
C121 10U/6.3V_8/X5R
C133 10U/6.3V_8/X5R
C124 *10U/6.3V_8/X5R_NC
C336 *10U/6.3V_8/X5R_NC
C127 *10U/6.3V_8/X5R_NC
C137 *10U/6.3V_8/X5R_NC
C136 *10U/6.3V_8/X5R_NC
C342 22U/6.3V_8/X5R
C130 22U/6.3V_8/X5R
C340 *22U/6.3V_8/X5R_NC

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

+1.05V_VTT

C139 22U/6.3V_8/X5R
C134 22U/6.3V_8/X5R

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

PSI# AN33 H_PSI# 39

VID[0] AK35 VID0 39
VID[1] AK33 VID1 39
VID[2] AK34 VID2 39
VID[3] AL35 VID3 39
VID[4] AL33 VID4 39
VID[5] AM33 VID5 39
VID[6] AM35 VID6 39
PROC_DPRSLPVR AM34 DPRSLPVR 39

VTT_SELECT G15 TP32

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

ISENSE AN35 I_MON 39

VTT_SENSE B15 VTT_SENSE 37
VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT T28

VCC_SENSE AJ34
VSS_SENSE AJ35

VCCSENSE 39
VSSSENSE 39

+VCC_CORE

R97 100/F
R98 100/F

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options
in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors
will depend on the POC configuration of AUB
and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

0525 Steg : As an option, VTT_SENSE pin on the processor can be left floating. But the platform needs to have the FB (feedback) pin of the VR tied to the VTT plane regulation.

U15G

POWER

GRAPHICS

FDI

PEG & DMI

SENSE LINES

GRAPHICS VIDs

DDR3 - 1.5V RAILS

1.1V

1.8V

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

AT21 AT19 AT18 AT16 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16

+VCC_GFX_CORE

C120 10U/6.3V_8/X5R
C126 10U/6.3V_8/X5R

8

C140 330U/2V_7343
C129 22U/6.3V_8/X5R
C123 22U/6.3V_8/X5R

+1.05V_VTT

C132 22U/6.3V_8/X5R
C327 *22U/6.3V_8/X5R_NC

VTT1_45 VTT1_46 VTT1_47

J24 J23 H25

+1.05V_VTT

C131 22U/6.3V_8/X5R
C138 22U/6.3V_8/X5R
C135 *22U/6.3V_8/X5R_NC
C141 *22U/6.3V_8/X5R_NC

K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25

VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58

VTT_SELECT:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield

IC,AUB_CFD_rPGA,R1P0

VAXG_SENSE AR22
VSSAXG_SENSE AT22

VCC_AXG_SENSE 38
VSS_AXG_SENSE 38

GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24

GFXVR_VID_0 38
GFXVR_VID_1 38
GFXVR_VID_2 38
GFXVR_VID_3 38
GFXVR_VID_4 38
GFXVR_VID_5 38
GFXVR_VID_6 38

GFX_VR_EN AR25 GFXVR_EN
GFX_DPRSLPVR AT25
GFX_IMON AM24

R306 4.7K/F_4
GFXVR_EN 38
GFXVR_IMON 38
R114 *1K/F_4_NC

2A

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18

AJ1 AF1 AE7 AE4 AC1 AB7 AB4 Y1 W7 W4 U1 T7 T4 P1 N7 N4 L1 H1

+1.5V_SUS

C147 1U/6.3V/X5R
C149 1U/6.3V/X5R
C148 1U/6.3V/X5R
C146 1U/6.3V/X5R
C145 1U/6.3V/X5R
C150 22U/6.3V_8/X5R
C151 *22U/6.3V_8/X5R_NC
C152 330U/2V_7343

VTT0_59 VTT0_60 VTT0_61 VTT0_62 VTT1_63 VTT1_64 VTT1_65 VTT1_66 VTT1_67 VTT1_68

P10 N10 L10 K10 J22 J20 J18 H21 H20 H19

+1.05V_VTT

C337 10U/6.3V_8/X5R
C338 *10U/6.3V_8/X5R_NC
C331 22U/6.3V_8/X5R
C335 *22U/6.3V_8/X5R_NC

VCCPLL1 VCCPLL2 VCCPLL3

L26 L27 M26

+1.8V_RUN

C114 22U/6.3V_8/X5R
C324 4.7U/6.3V/X5R
C323 2.2U/6.3V/X5R
C322 1U/6.3V/X5R
C321 1U/6.3V/X5R

VID0 R280 1K/J_4 *1K/J_4_NC
VID1 R290 1K/J_4 *1K/J_4_NC
VID2 R288 1K/J_4 *1K/J_4_NC
VID3 R298 1K/J_4 *1K/J_4_NC
VID4 R281 1K/J_4 *1K/J_4_NC
VID5 R291 1K/J_4 *1K/J_4_NC
VID6 R282 1K/J_4 *1K/J_4_NC
DPRSLPVR R292 1K/J_4 *1K/J_4_NC
H_PSI# R283 1K/J_4 *1K/J_4_NC
R293 1K/J_4
R287 1K/J_4 *1K/J_4_NC
R297 1K/J_4 *1K/J_4_NC
R284 1K/J_4 *1K/J_4_NC
R294 1K/J_4
R285 1K/J_4 *1K/J_4_NC
R295 1K/J_4 *1K/J_4_NC
R286 1K/J_4 *1K/J_4_NC
R296 1K/J_4

+1.05V_VTT

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	PROCESSER 3/4(POWER)	1A

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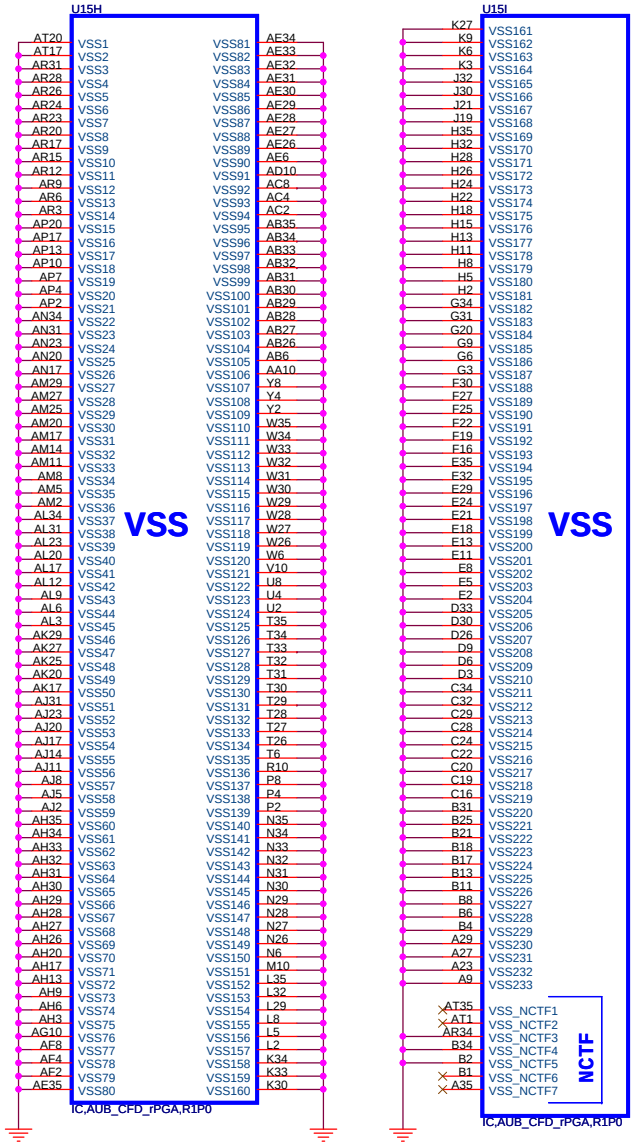
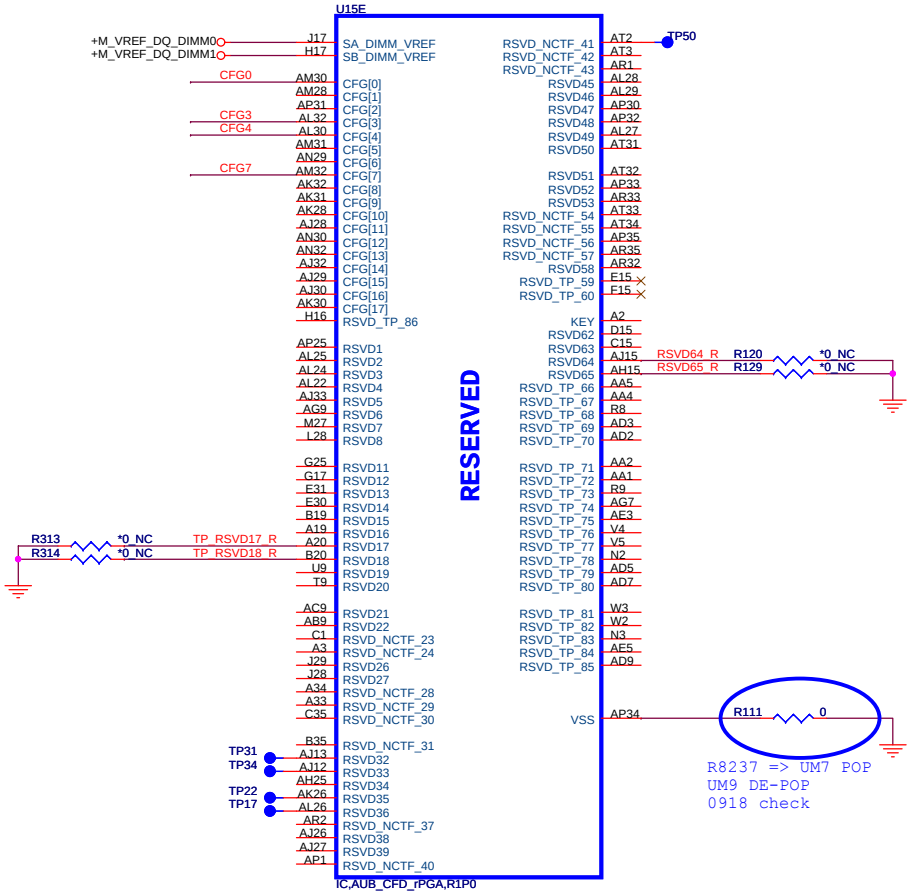
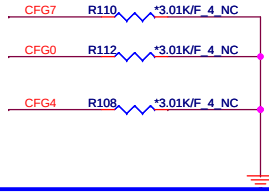
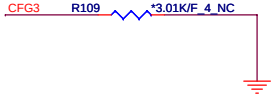
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)







	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U14A — Ibex-M 1 OF 10

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN# / GPIO33 (+3V), HDA_DOCK_RST# / GPIO13 (+3V_S5)
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO
LPC: FWH0 / LAD0, FWH1 / LAD1, FWH2 / LAD2, FWH3 / LAD3, FWH4 / LFRAME#, LDRQ0#, (+3V) LDRQ1# / GPIO23, SERIRQ
SATA: SATA0RXN/P, SATA0TXN/P, SATA1RXN/P, SATA1TXN/P, SATA2RXN/P, SATA2TXN/P, SATA3RXN/P, SATA3TXN/P, SATA4RXN/P, SATA4TXN/P, SATA5RXN/P, SATA5TXN/P, SATAICOMPO, SATAICOMPI, SATALED#, (+3V) SATA0GP / GPIO21, (+3V_S5) SATA1GP / GPIO19

IbexPeak-M_Rev1_0

C287 18P/50V_4/COG, C288 18P/50V_4/COG, Y5 32.768KHZ, R265 10M/J_4
RTC_X1, RTC_X2, T25 PAD RTC_RST#, T26 PAD SRTC_RST#, SM_INTRUDER#, +RTC_CELL R266 330K/J_6 PCH_INVRMEN, T24 PAD
ACZ_BITCLK, ACZ_SYNC, 31 ACZ_SPKR, ACZ_RST#, 31 ACZ_SDIN0, ACZ_SDOUT, 25 PCH_MELOCK R339 *0_NC PCH_GPIO33
TP37 PCH_JTAG_TCK_BUF, TP38 PCH_JTAG_TMS, TP39 PCH_JTAG_TDI, TP40 PCH_JTAG_TDO, TP41 PCH_JTAG_RST#
must add test point.
26 SPI_CLK, 26 SPI_CS0# TP4, TP43 SPI_CS1#, 26 SPI_SI TP6, 26 SPI_SO TP3, C362 *100P/NPO_NC
SATA_COMP R58 37.4/F_4, SATA_LED#, SATA_DET0#, SATA_DET1#

8 11 20 24 25 35 55

DG: Place TX cap close to connector
SATA port 2/3 are not support in HM55 . They are only in PM 55

ESATA: SATA_RXN4 27, SATA_RXP4 27, SATA_TXN4 27, SATA_TXP4 27

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

HDD: LAD0 25,31, LAD1 25,31, LAD2 25,31, LAD3 25,31, LFRAME# 25,31, SERIRQ 25

ODD: SATA_RXN0 28, SATA_RXP0 28, SATA_TXN0 28, SATA_TXP0 28, SATA_RXN1 28, SATA_RXP1 28, SATA_TXN1 28, SATA_TXP1 28

Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled

R62 1 2 *1K_NC PCH_GPIO33
(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

R242 10K/J_4 SATA_LED#
+3.3V_RUN R37 10K/J_4 SATA_DET0#, R240 10K/J_4 SATA_DET1#

Serial ATA LED: This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required.

iTPM ENABLE/DISABLE

+3.3V_RUN R263 *1K_NC SPI_SI

TPM Function	
Enable	Mount
Disable	NC (Default)

No Reboot strap.

SPKR	Low = Default. High = No Reboot.

For AUDIO

25,31 ACZ_RST#_AUDIO, 31 ACZ_SDOUT_AUDIO, 31 ACZ_SYNC_AUDIO, 31 ACZ_BITCLK_AUDIO
R276 33/J_4 ACZ_RST#, R273 33/J_4 ACZ_SDOUT, C292 *10P/50V_4_NC/COG, R274 33/J_4 ACZ_SYNC, C293 *10P/50V_4_NC/COG, R275 33/J_4 ACZ_BITCLK, C294 10P/50V_4/COG
+3.3V_RUN R226 *1K/F_4_NC ACZ_SPKR

RTC

1mA
+RTC_CELL
R267 20K/F_4 C289 1U/6.3V/X5R RTC_RST#
R271 20K/F_4 C291 1U/6.3V/X5R SRTC_RST#
R268 1M/J_4 SM_INTRUDER#

UMA CRT,LVDS&HDMI signals
IBEX PEAK-M (LVDS,DDI)

U14D — Ibex-M 4 OF 10

LVDS--A: LVDSA_CLK#, LVDSA_CLK, LVDSA_DATA#0, LVDSA_DATA#1, LVDSA_DATA#2, LVDSA_DATA#3
LVDS--B: LVDSB_CLK#, LVDSB_CLK, LVDSB_DATA#0, LVDSB_DATA#1, LVDSB_DATA#2, LVDSB_DATA#3
CRT: CRT_BLUE, CRT_GREEN, CRT_RED, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNC, DAC_IREF, CRT_IRTN
SDVO: SDVO_TVCLKINN, SDVO_TVCLKINP, SDVO_STALLN, SDVO_STALLP, SDVO_INTN, SDVO_INTP, SDVO_CTRLCLK, SDVO_CTRLDATA
DISPLAY PORT B: DDPB_AUXN, DDPB_AUXP, DDPB_HPD, DDPB_0N, DDPB_0P, DDPB_1N, DDPB_1P, DDPB_2N, DDPB_2P, DDPB_3N, DDPB_3P
DISPLAY PORT C: DDPC_CTRLCLK, DDPC_CTRLDATA, DDPC_AUXN, DDPC_AUXP, DDPC_HPD, DDPC_0N, DDPC_0P, DDPC_1N, DDPC_1P, DDPC_2N, DDPC_2P, DDPC_3N, DDPC_3P
DISPLAY PORT D: DDPD_CTRLCLK, DDPD_CTRLDATA, DDPD_AUXN, DDPD_AUXP, DDPD_HPD, DDPD_0N, DDPD_0P, DDPD_1N, DDPD_1P, DDPD_2N, DDPD_2P, DDPD_3N, DDPD_3P
Digital Display Interface

PANEL_BKEN T48, ENVDD T47, BIA_PWM Y48, LCD_DDCCLK AB48, LCD_DDCDAT Y45, L_CTRL_CLK AB46, L_CTRL_DATA V48, R65 2.37K/F_4 T6 PAD LVDS_VBG AP39, AP41, T3 PAD AT43, T10 PAD AT42
LCD_ACLK- AV53, LCD_ACLK+ AV51, LCD_A0- BB47, LCD_A1- BA52, LCD_A2- AY48, INT_TXLOUTN3 AV47, T8 PAD
LCD_A0+ BB48, LCD_A1+ BA50, LCD_A2+ AY49, INT_TXLOUTP3 AV48, T9 PAD
AP48, AP47, AY53, AT49, AU52, AT53, T13 PAD, AY51, AT48, AU50, AT51, T12 PAD
VGA_BLU AA52, VGA_GRN AB53, VGA_RED AD53, DDCCLK V51, DDCDAT V53, VGAHSYNC R85 33/J_4 Y53, VGAVSYNC R84 33/J_4 Y51, R78 1K/D_4 AD48, AB51

UMA 0.5%
DIS 1%

ibexPeak-M_Rev1_0

+3.3V_RUN R92 2.2K/J_4, R91 2.2K/J_4
HDMI_SCL 24, HDMI_SDA 24, INT_HDMI_HPD
INT_HDMI_TXDN0 C76, INT_HDMI_TXDP0 C74, INT_HDMI_TXDN1 C73, INT_HDMI_TXDP1 C71, INT_HDMI_TXDN2 C68, INT_HDMI_TXDP2 C66, INT_HDMI_TXCN C62, INT_HDMI_TXCP C57
0.1U/10V_4/K7R
INT_HDMI_TXDN2_C 24, INT_HDMI_TXDP2_C 24, INT_HDMI_TXDN1_C 24, INT_HDMI_TXDP1_C 24, INT_HDMI_TXDN0_C 24, INT_HDMI_TXDP0_C 24, INT_HDMI_TXCN_C 24, INT_HDMI_TXCP_C 24

Close to VGA side
VGA_BLU R95 150/F_4, VGA_GRN R83 150/F_4, VGA_RED R94 150/F_4
C592 *22P_NC, C593 *22P_NC, C594 *22P_NC, 50

PANEL_BKEN R76 100K/J_4, ENVDD R77 100K/J_4
LCD_DDCDAT R90 2.2K/J_4, LCD_DDCCLK R89 2.2K/J_4, L_CTRL_CLK R86 10K/F_4, L_CTRL_DATA R87 10K/F_4
+3.3V_RUN
+5V_RUN Q11 2N7002K-T1-E3
INT_HDMI_HPD, R74 100K/J_4, R96 *0/J_4_NC, HDMI_DET 24

+3.3V_SUS **Res. of TDI near PCH**
R228 *200_NC, R229 *200_NC, R230 *200_NC, R231 20K/F_4_NC
PCH_JTAG_TMS, PCH_JTAG_TDI, PCH_JTAG_TDO, PCH_JTAG_RST#
R245 *100_NC, R246 *100_NC, R247 *100_NC, R248 *10K_NC

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

R244 51/J_4 PCH_JTAG_TCK_BUF

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

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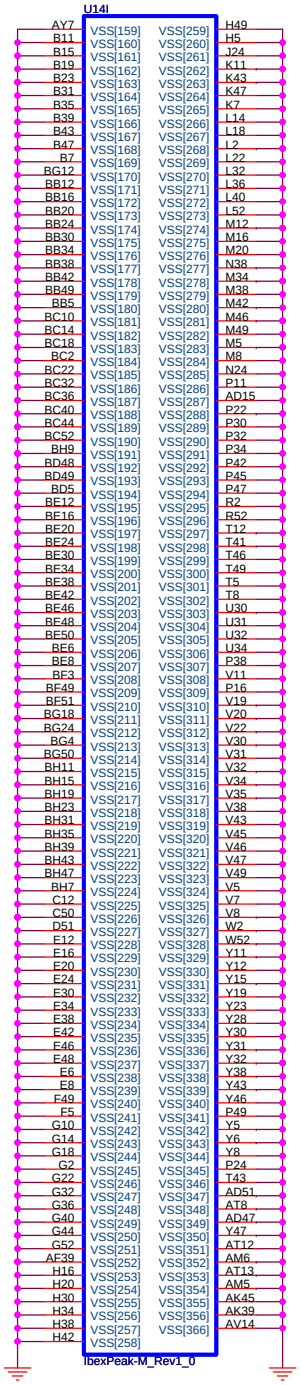
IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E,SMBUS,CLK)

08

U14B

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PCI-E*

[WLAN]
31 PCIE_RXN1
31 PCIE_RXP1
31 PCIE_TXN1
31 PCIE_TXP1
C54 0.1U/ 10V/X7R PCIE_TXN1_C
C53 0.1U/ 10V/X7R PCIE_TXP1_C
PCIE_RXN1 AW30
PCIE_RXP1 BA30
BC30
BD30

[LAN]
31 PCIE_RXN6_LAN
31 PCIE_RXP6_LAN
31 PCIE_TXN6_LAN
31 PCIE_TXP6_LAN
C50 0.1U/ 10V/X7R PCIE_TXN6_LAN_C
C56 0.1U/ 10V/X7R PCIE_TXP6_LAN_C
PCIE_RXN6_LAN BA34
PCIE_RXP6_LAN AW34
BC34
BD34

MiniWLAN
31 CLK_PCIE_WLANN
31 CLK_PCIE_WLANP
31 PCIE_CLK_REQ1#
PCIE_CLK_REQ0# P9
AM43
AM45
U4

LAN
31 CLK_PCIE_LANN
31 CLK_PCIE_LANP
31 PCIE_CLK_REQB#_R
AK53
AK51
PCIE_CLK_REQB#_R P13

SMBus
(+3V_S5) SMBALERT# / GPIO11
SMBCLK
SMBDATA
(+3V_S5) SML0ALERT# / GPIO60
SML0CLK
SML0DATA
(+3V_S5) SML1ALERT# / GPIO74
(+3V_S5) SML1CLK / GPIO58
(+3V_S5) SML1DATA / GPIO75
B9 SMBALERT# 10K/J_4 R261
H14 ICH_SMBCLK 2.2K/J_4 R51
C8 ICH_SMBDATA 2.2K/J_4 R259
J14 SMBL0ALERT# 10K/J_4 R49
C6 SMB_CLK_ME0 2.2K/J_4 R258
G8 SMB_DATA_ME0 2.2K/J_4 R33
M14 SML1ALERT# 10K/J_4 R45
E10 SMB_CLK_ME1 2.2K/J_4 R43
G12 SMB_DATA_ME1 2.2K/J_4 R48
+3.3V_SUS
SMB1 Check R value...
(R8283, R8296)

Controller Link
CL_CLK1 T13
CL_DATA1 T11
CL_RST1# T9
ICH_SMBCLK ICH_SMBCLK 31
ICH_SMBDATA ICH_SMBDATA 31

PEG
(+3V_S5) PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
H1 PEG_CLKREQ# T23
AD43
AD45
AN4 CLK_PCIE_3GPLLN 3
AN2 CLK_PCIE_3GPLLP 3

From CLK BUFFER
CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P
AT1 CLK_DREFSSCLKN
AT3 CLK_DREFSSCLKP
CLKIN_DMI_N
CLKIN_DMI_P
AW24 CLK_BUF_PCIE_3GPLLN 2
BA24 CLK_BUF_PCIE_3GPLLP 2
CLKIN_BCLK_N
CLKIN_BCLK_P
AP3 CLK_BUF_BCLKN 2
AP1 CLK_BUF_BCLKP 2
CLKIN_DOT_96N
CLKIN_DOT_96P
F18 CLK_BUF_DREFCLKN 2
E18 CLK_BUF_DREFCLKP 2
CLKIN_SATA_N / CKSSCD_N
CLKIN_SATA_P / CKSSCD_P
AH13 CLK_BUF_DREFSSCLKN 2
AH12 CLK_BUF_DREFSSCLKP 2
REFCLK14IN P41 CLK_PCH_14M 2
C67 *5.6P/50V_4_NC/COG
CLKIN_PCILOOPBACK J42 CLK_PCI_FB
CLK_PCI_FB 9
T27
Intel recommendation
XTAL25_IN AH51 XTAL25_IN
XTAL25_OUT AH53 XTAL25_OUT
R81 *0_NC RC0402
XCLK_RCOMP AF38 XCLK_RCOMP
R69 90.9/F_4
+1.05V_PCH

Clock Flex
(+3V) CLKOUTFLEX0 / GPIO64
(+3V) CLKOUTFLEX1 / GPIO65
(+3V) CLKOUTFLEX2 / GPIO66
(+3V) CLKOUTFLEX3 / GPIO67
T45 CLK_FLEX0 T11
P43 CLK_FLEX1 T7
T42 CLK_FLEX2 T5
N50 CLK_FLEX3
R277 22/J_4
CLK_48M_CARD 23
55
C295 5.6P/50V_4/COG
R8236 => UM7 POP 33ohm
UM9 POP 22ohm
0918 check

CLKOUT_PCIE0N
CLKOUT_PCIE0P
PCIECLKRQ0# / GPIO73 (+3V_S5)
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1# / GPIO18 (+3V)
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2# / GPIO20 (+3V)
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3# / GPIO25 (+3V_S5)
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4# / GPIO26 (+3V_S5)
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5# / GPIO44 (+3V_S5)
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ# / GPIO56 (+3V_S5)

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PCIE Clock Request

+3.3V_RUN
PCIE_CLK_REQ1# R241 10K/J_4
PCIE_CLK_REQ2# R243 10K/J_4
+3.3V_SUS
PCIE_CLK_REQ0# R42 10K/J_4
PCIE_CLK_REQ3# R260 10K/J_4
PCIE_CLK_REQ4# R31 10K/J_4
PCIE_CLK_REQB#_R R28 10K/J_4
PCIE_CLK_REQ5# R255 10K/J_4

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S (DS 401376 Table2-26)

6
PEG_CLKREQ# R249 10K/J_4 +3.3V_SUS

Q8 FDN357N
SMB_CLK_ME1 1 3 SMBCLK1 25
+3.3V_SUS
SMB_DATA_ME1 1 3 SMBDAT1 25
Q10 FDN357N

CLK_DREFSSCLKN
CLK_DREFSSCLKP
R252 *0_NC
R256 *0_NC

UMA	POP Y8201, C8411, C8412 and R8401, de-POP R8999 for Internal GFX
DIS	de-POP Y8201, C8411, C8412 and R8401, POP R8999 for Internal GFX

43
XTAL25_IN
XTAL25_OUT
R80 1M/F_4
25MHz Y3
C89 27p/NPO
C88 27p/NPO

Quanta Computer Inc.
PROJECT : UM8 UMA
Size | Document Number: PCH 2/5 (PCIE, SMBUS, CK) | Rev 1A
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IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)

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U14C — Ibex-M 3 OF 10

PCI

AD0–AD31, C/BE0#–C/BE3#, PIRQA#–PIRQD#, REQ0#–REQ3# / GPIO50–GPIO55 (+5V/+3V), GNT0#–GNT3#, PIRQE#–PIRQH# / GPIO2–GPIO5 (+5V), PCIRST#, SERR#, PERR#, IRDY#, PAR, DEVSEL#, FRAME#, PLOCK#, STOP#, TRDY#, PME#, PLTRST#, CLKOUT_PCI0–CLKOUT_PCI4

RP13 8.2KX8: PCI_PIRQD#, PCI_SERR#, REQ1#, PCI_FRAME#, PCI_IRDY#, PCI_STOP#, PCI_PIRQA#, PCI_PIRQC# — +3.3V_RUN

RP3 8.2KX8: USB_OC7#, USB_OC0#, USB_OC5#, USB_OC2#, USB_OC6#, USB_OC3#, USB_OC1#, USB_OC4# — +3.3V_SUS

RP14 8.2KX8: PCI_PLOCK#, PCI_PERR#, REQ0#, PCI_PIRQB#, PCI_DEVSEL#, PCI_TRDY#, INTH# — +3.3V_RUN

USB_MCARD1_DET# (31)

R88 *10K/F_4_NC; R75 *1K/F_4_NC; R73 *1K/F_4_NC; BT_DET#

TP8; TP7

R279 22/J_4 CLK_33M_LPC_R; R82 22/J_4 CLK_33M_KBC_R; R278 22/J_4 CLK_PCI_FB_R

CLK_33M_LPC (31); CLK_33M_KBC (25); CLK_PCI_FB (8)

CLKOUT_PCI[0..4]:
22 ohm series resistor is recommend
(single & double load) on PDG v1.1

R8404, R8403 and R8402
=> UM7 POP 22ohm
UM9 POP 22ohm
0918 check

NVRAM

NV_CE#0–NV_CE#3, NV_DQS0/NV_DQS1, NV_DQ0/NV_IO0 … NV_DQ15/NV_IO15, NV_ALE, NV_CLE, NV_RCOMP, NV_RB#, NV_WR#0_RE#, NV_WR#1_RE#, NV_WE#_CK0, NV_WE#_CK1

USB

USBP0N/P … USBP13N/P, USBRBIAS#, USBRBIAS

USB_BIAS R272 22.6/F_4

USB #0 (USBP0-/P0+, 31)
USB #1 (USBP1-/P1+, 31)
USB #2 (eSATA) (USBP2-/P2+, 27)
WLAN (USBP4-/P4+, 31)
WWAN (USBP5-/P5+, 31)
BT (USBP8-/P8+, 27)
Webcam (USBP11-/P11+, 22)
Card Reader (USBP12-/P12+, 23)

USB_OC0# / GPIO59 … USB_OC7# / GPIO14 (+3V_S5)

USB_OC0# (31); USB_OC1# (27)

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IbexPeak-M_Rev1_0

DMI

DMI0RXN–DMI3RXN, DMI0RXP–DMI3RXP, DMI0TXN–DMI3TXN, DMI0TXP–DMI3TXP, DMI_ZCOMP, DMI_IRCOMP

DMI_COMP R60 49.9/F_4 (+1.05V_PCH)

FDI

FDI_RXN0–FDI_RXN7, FDI_RXP0–FDI_RXP7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

FDI_TXN0–FDI_TXN7, FDI_TXP0–FDI_TXP7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

PCH_PWROK — C279 *100P_NC

System Power Management

SYS_RESET#, SYS_PWROK, PWROK, MEPWROK, LAN_RST#, DRAMPWROK, RSMRST#, PWRBTN#, RI#, WAKE#, PMSYNCH

SLP_S3# (SIO_SLP_S3# 25; TP9); SLP_S4#; SLP_M# (TP10); TP23

SUS_PWR_DN_ACK / GPIO30 (+3V_S5); ACPRESENT / GPIO31 (+3V_S5); CLKRUN# / GPIO32 (+3V); SUS_STAT# / GPIO61 (+3V_S5); SUSCLK / GPIO62 (+3V_S5); SLP_S5# / GPIO63 (+3V_S5); BATLOW# / GPIO72 (+3V_S5); SLP_LAN# / GPIO29 (+3V_S5)

SUS_PWR_ACK (25); AC_PRESENT (25); CLKRUN# (25); SIO_SLP_S5# (25; TP42); PM_BATLOW#

XDP_DBRESET# (3); ECPWROK (25); PM_DRAM_PWRGD (3); RSMRST# (25); PM_PWRBTN#_R (25); PCIE_WAKE# (31); PM_SYNC (3); PM_RI#

TP46; R30 *0_NC; TP44; TP45; RSV_ICH_LAN_RST#

IbexPeak-M_Rev1_0

CLKRUN# R221 8.2K; XDP_DBRESET# R41 10K/J_4 (+3.3V_RUN)

Connect this signal on PCH directly to the reset button and pull-up this signal to +V3.3 (Core rail) through a weak pull-up resistor (8.2 to 10-k).

RSMRST# R269 10K/J_4
RSV_ICH_LAN_RST# R262 10K/J_4
PCH_PWROK R270 10K/J_4

REQ2# R71 8.2K; PIRQE# R70 8.2K; PIRQF# R93 8.2K; BT_DET# R64 8.2K (+3.3V_RUN)

PM_RI# R52 10K/J_4; PM_BATLOW# R257 10K/J_4; PCIE_WAKE# R46 1K/J_4 (+3.3V_SUS)

SUS_PWR_ACK R227 10K/J_4; AC_PRESENT R27 10K/J_4

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

+1.8V_RUN

NV_ALE R264 *1K_NC; NV_CLE R53 *1K_NC

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

+3.3V_SUS

U5 *MC74VHC1G08DFT2G_NC; C21 *0.1U/10V_NC/X7R

PLT_RST-R# → PLTRST# 3,25,31

R44 100K/F_4; R34 *100K/F_4_NC; R23 *0_NC

Reserve capacitor pads for improving WWAN.

54

CLK_33M_KBC — C90 10P/50V/COG
CLK_33M_LPC — C297 *5.6P/50V_4_NC/COG

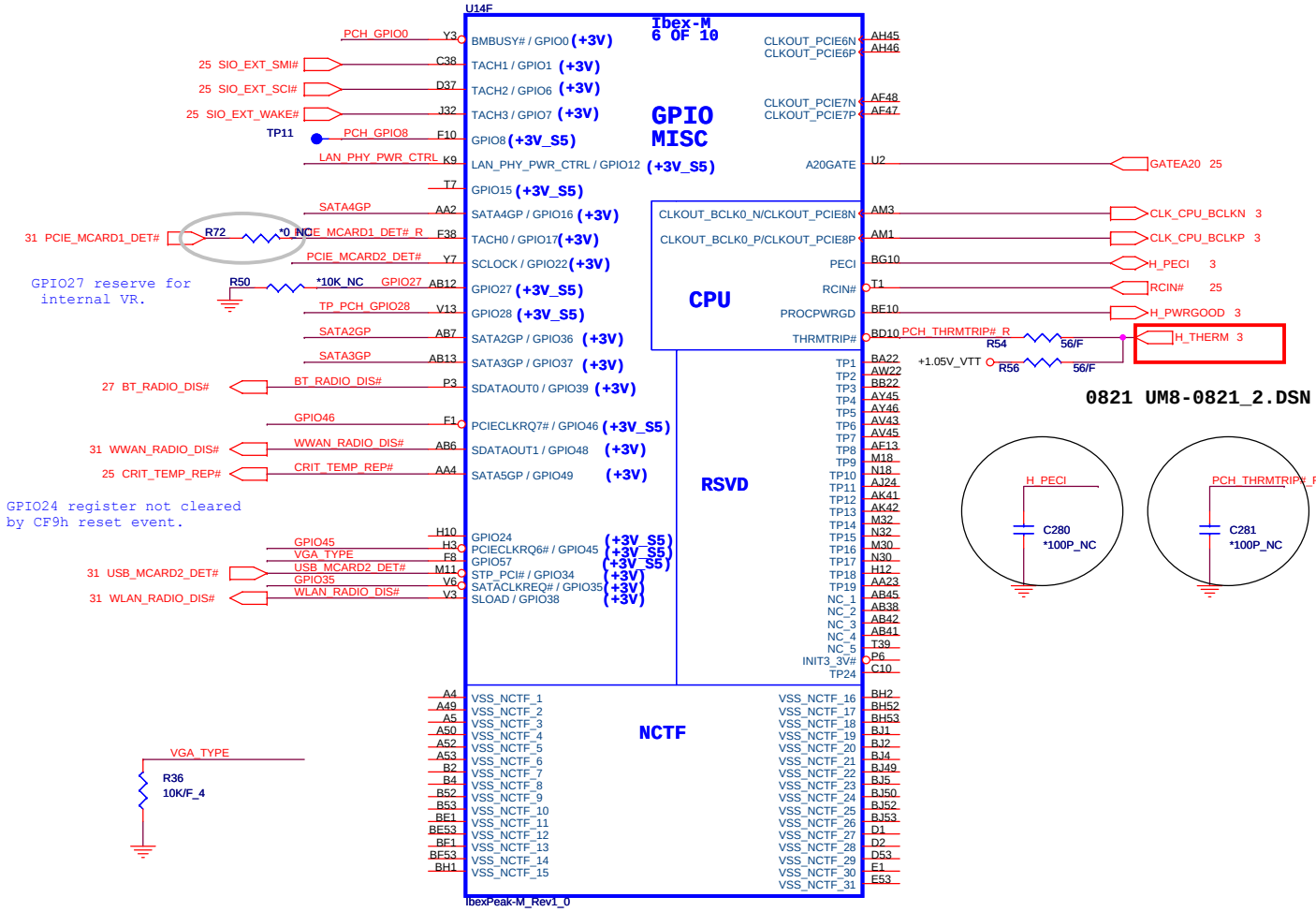
A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Quanta Computer Inc.
PROJECT : UM8 UMA

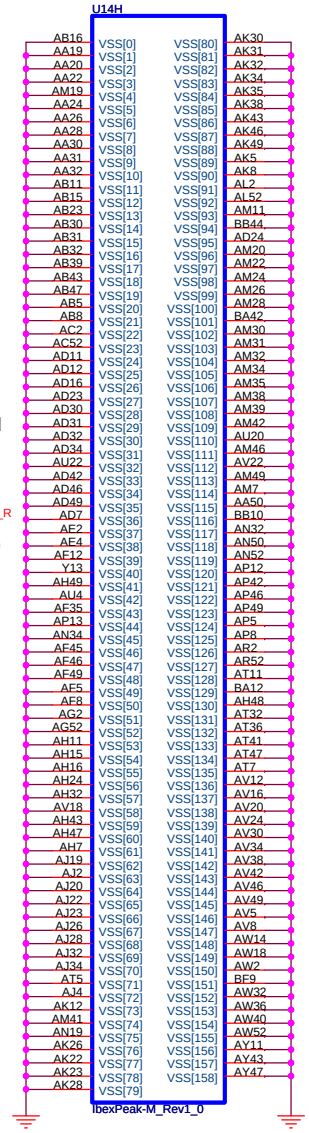
Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	1A
Date: Wednesday, February 10, 2010	Sheet 9 of 46	

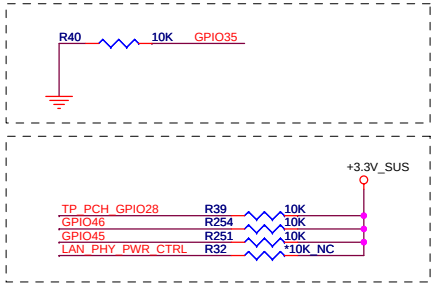
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

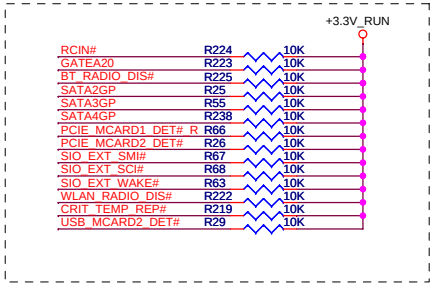


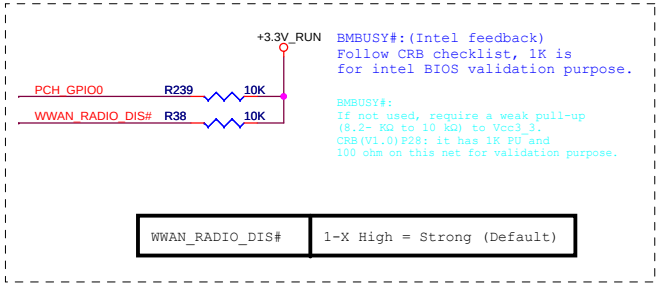
0821 UM8-0821_2.DSN

IBEX PEAK-M (GND)









Quanta Computer Inc.

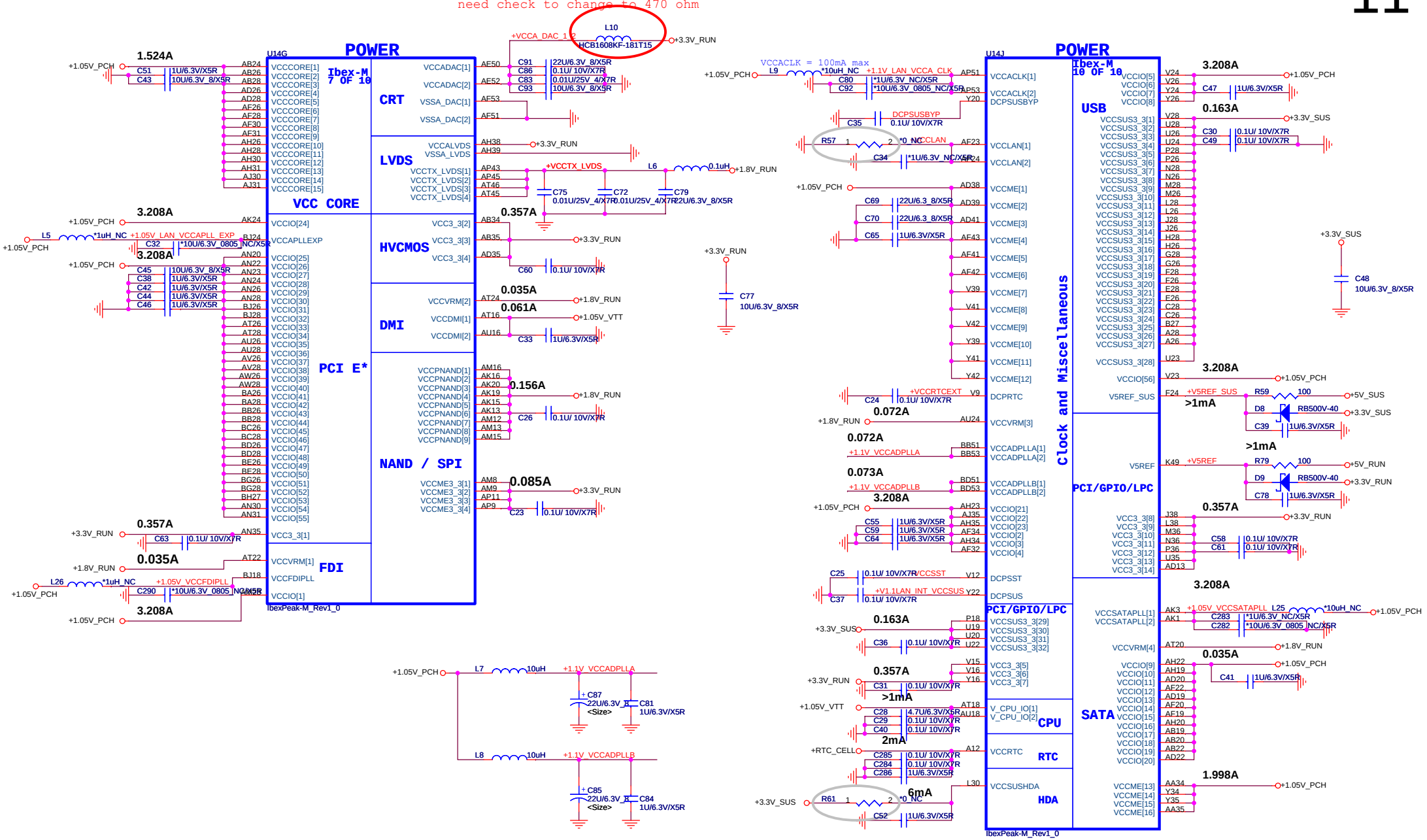
PROJECT : UM8 UMA

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	1A

Date: Wednesday, February 10, 2010 Sheet 10 of 46

Cap quantities follow UM3

need check to change to 470 ohm



Quanta Computer Inc.			
PROJECT : UM8 UMA			
Size	Document Number		Rev
	PCH 5/5 (POWER)		1A
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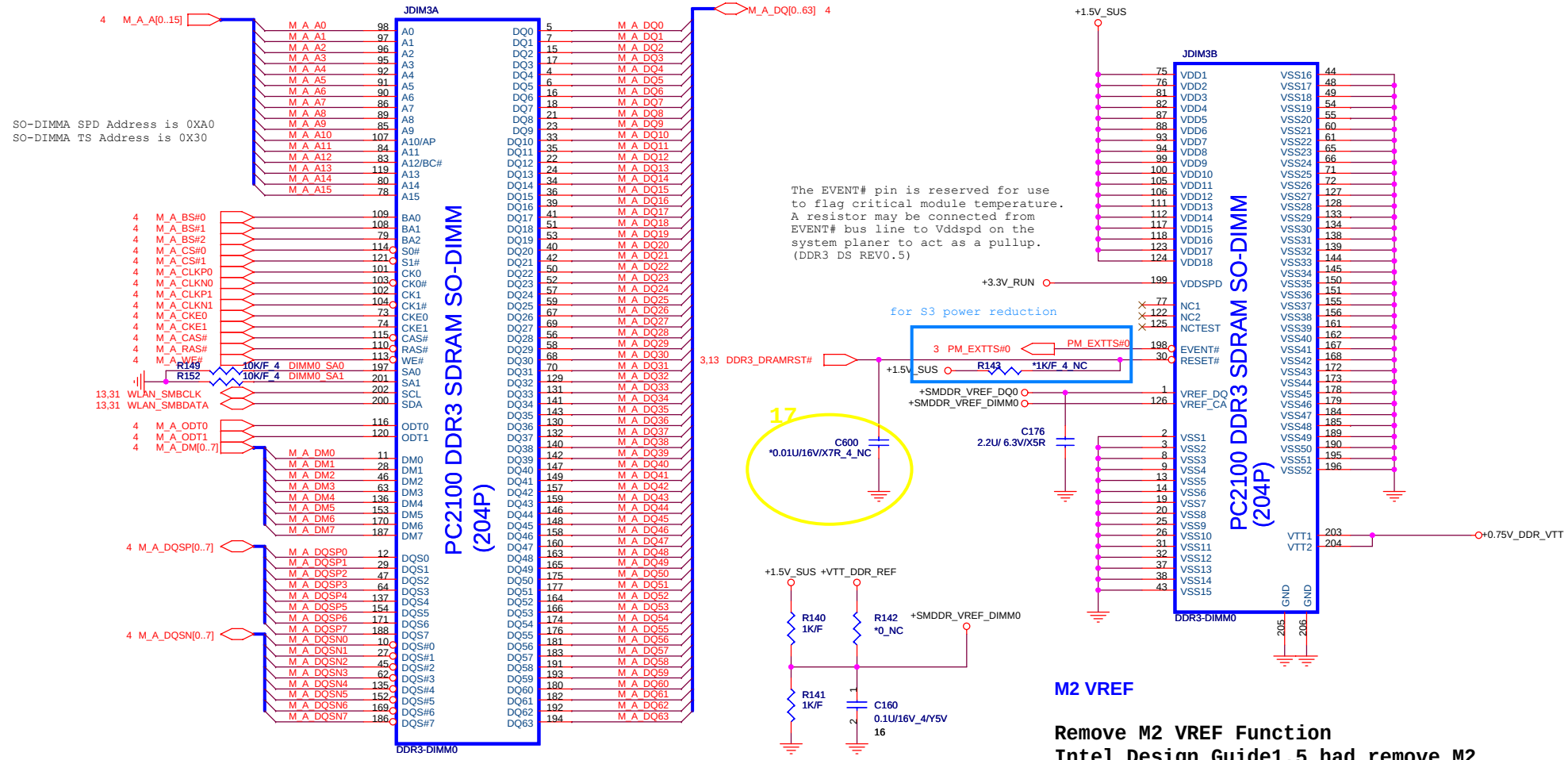


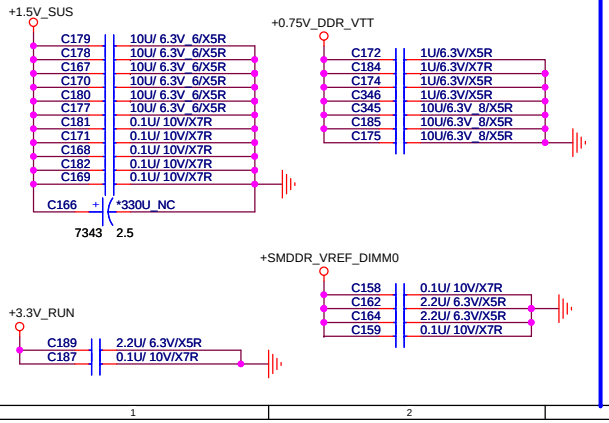
M2 VREF

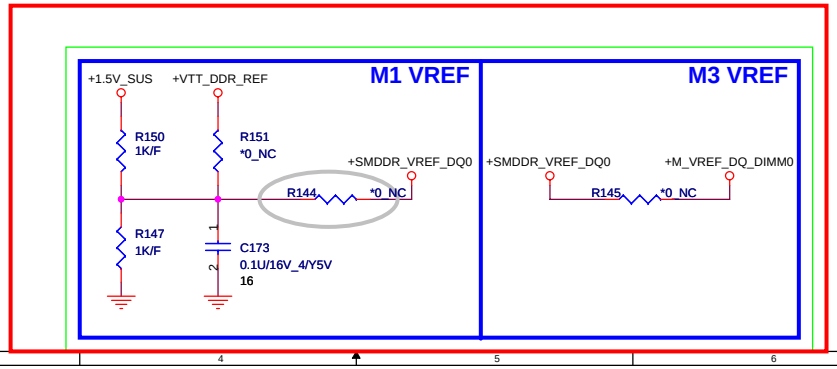
Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor

Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%





Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	DDR3 DIMM-0	1A

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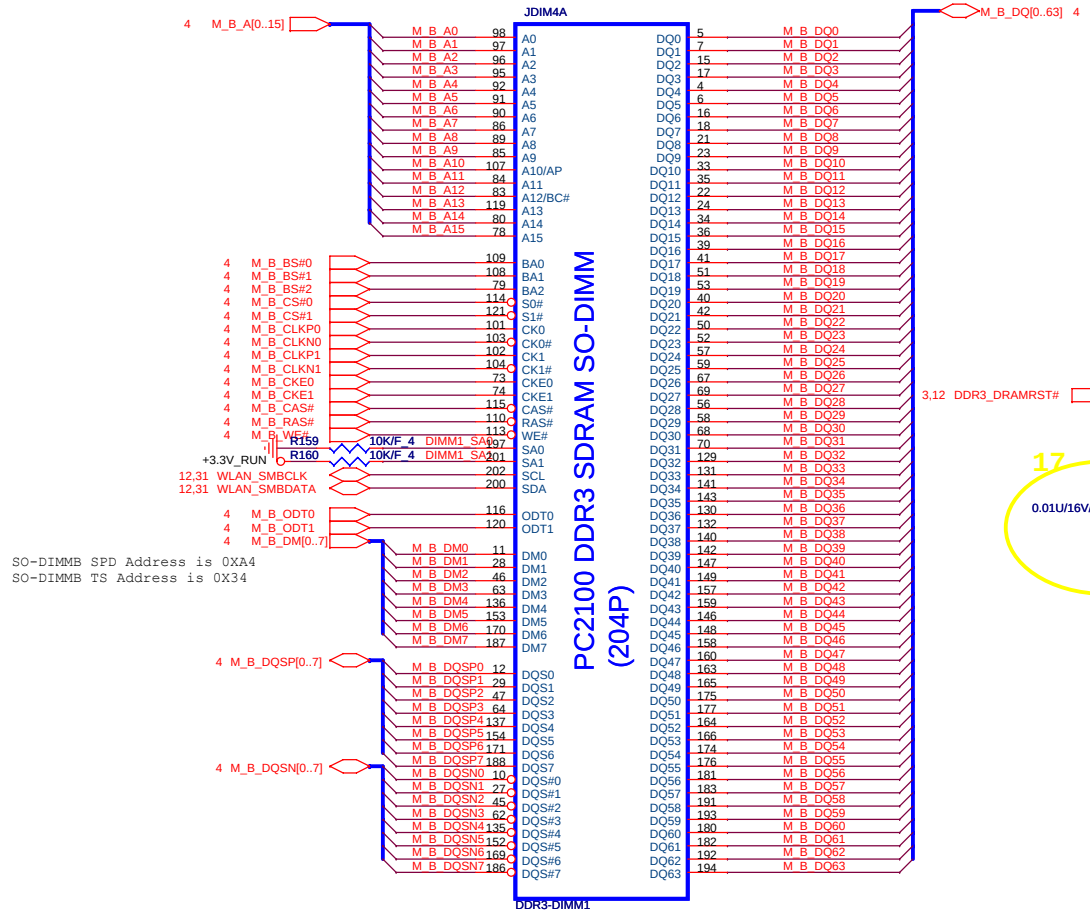
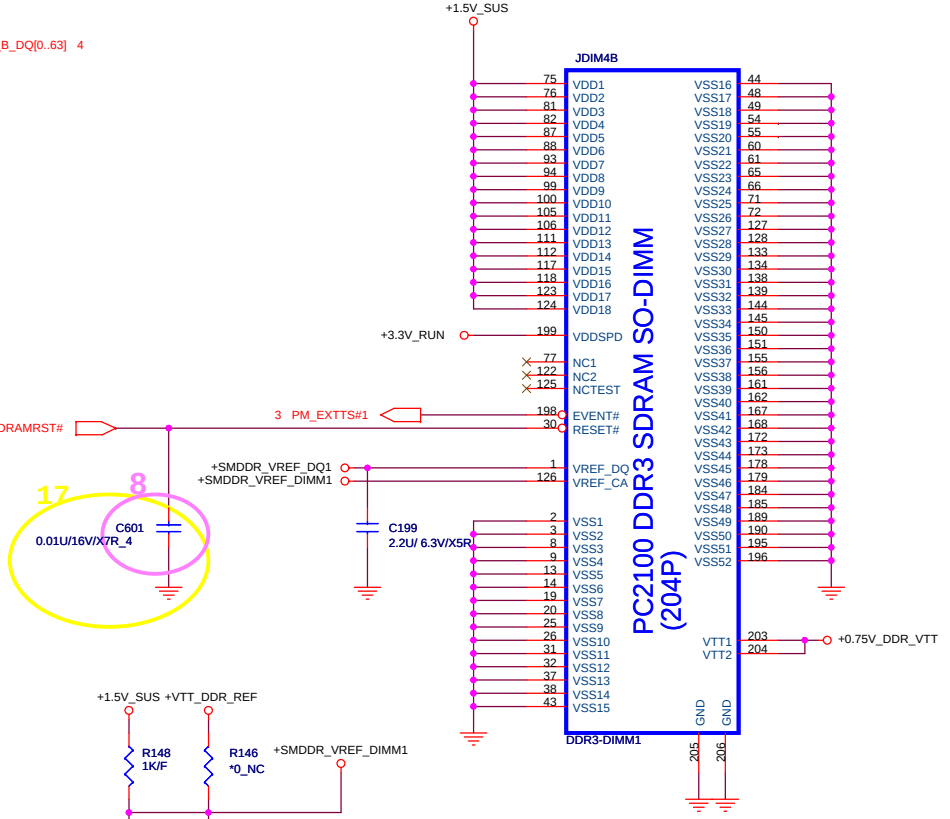


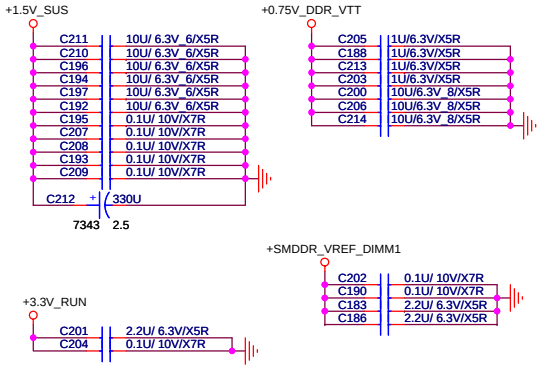


Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor

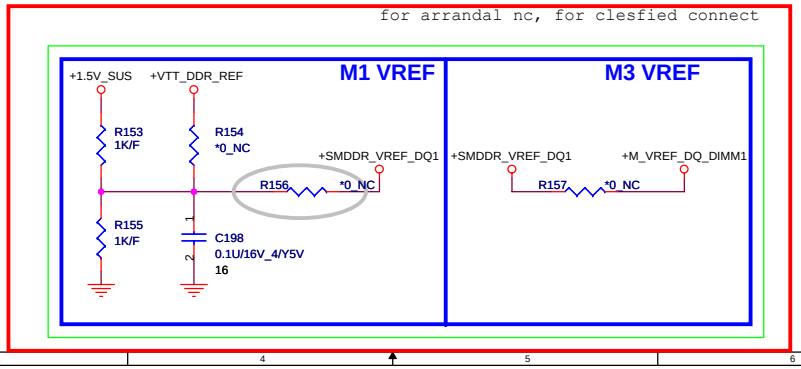
Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



Wait Victor check

for arrandal nc, for clesfied connect



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PROJECT : UM8 UMA

Size	Document Number	Rev
	DDR3 DIMM-1	1A

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Size	Document Number	Rev
	Blank	1A

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Size	Document Number	Rev
	Blank	1A

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Quanta Computer Inc.

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Size	Document Number	Rev
	Blank	1A

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Size	Document Number	Rev
	Blank	1A

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Size	Document Number	Rev
	Blank	1A

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Size	Document Number	Rev
	Blank	1A

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Size	Document Number	Rev
	Blank	1A

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Size	Document Number	Rev
	Blank	1A
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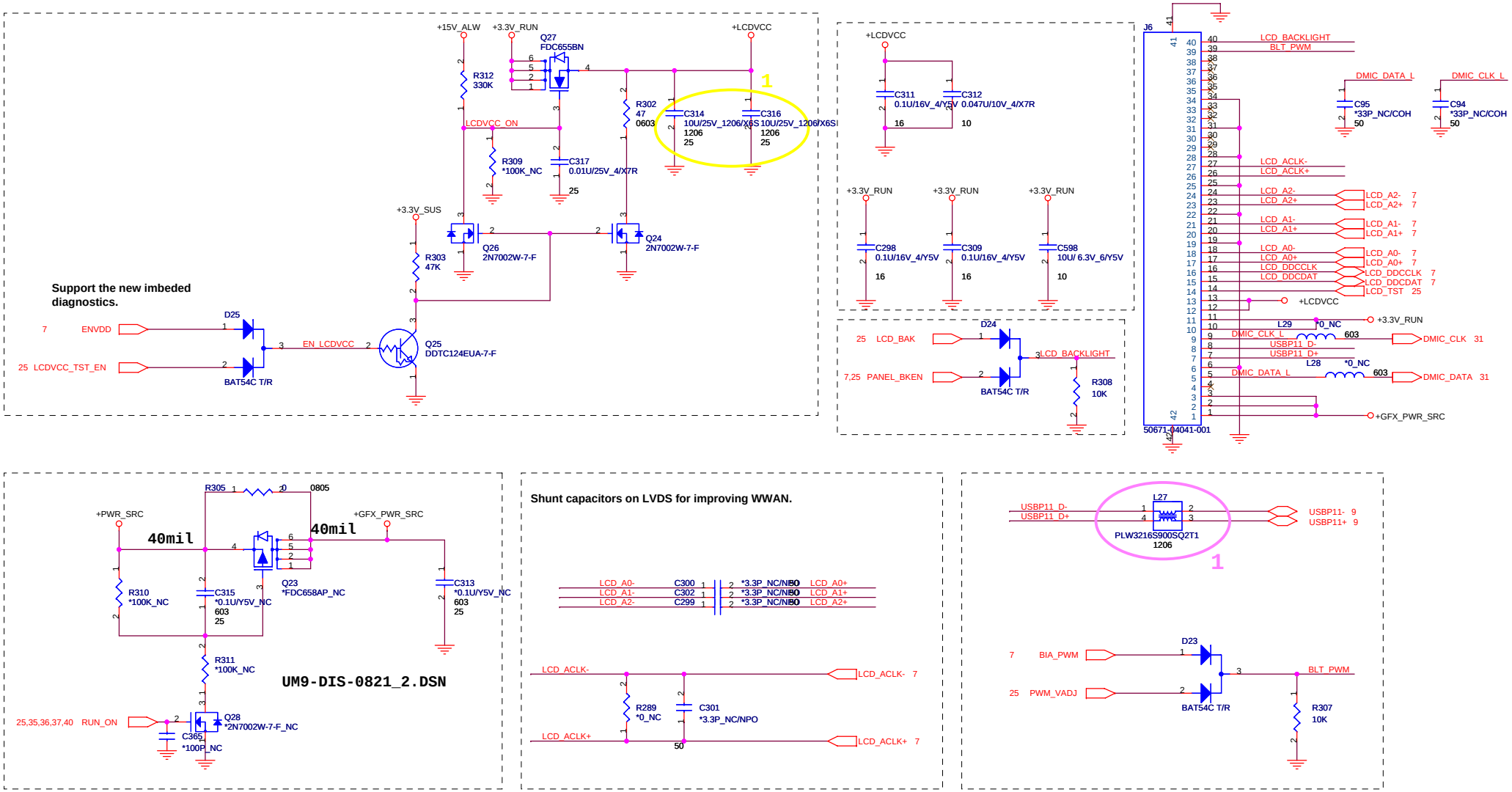

Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: LCD CONN	Rev: 1A
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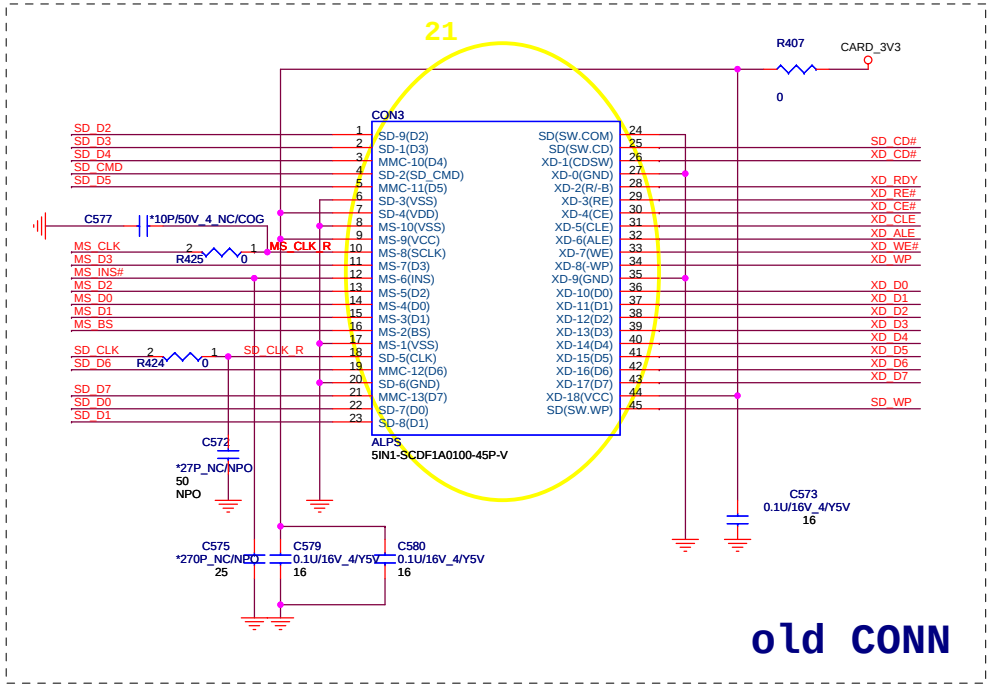
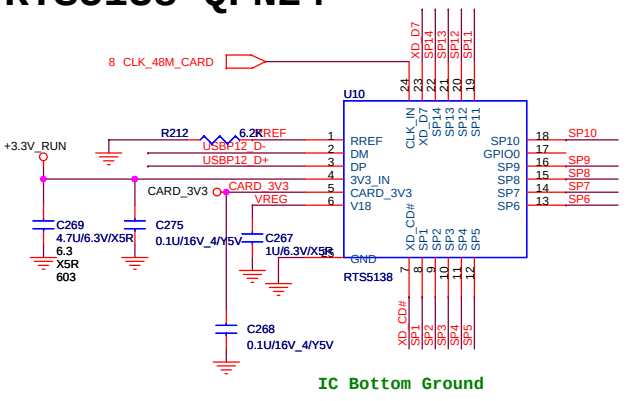


old CONN

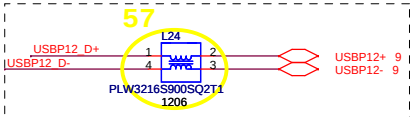
RTS5138-QFN24



IC Bottom Ground

SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin



Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	Card Reader(RST5138)	1A
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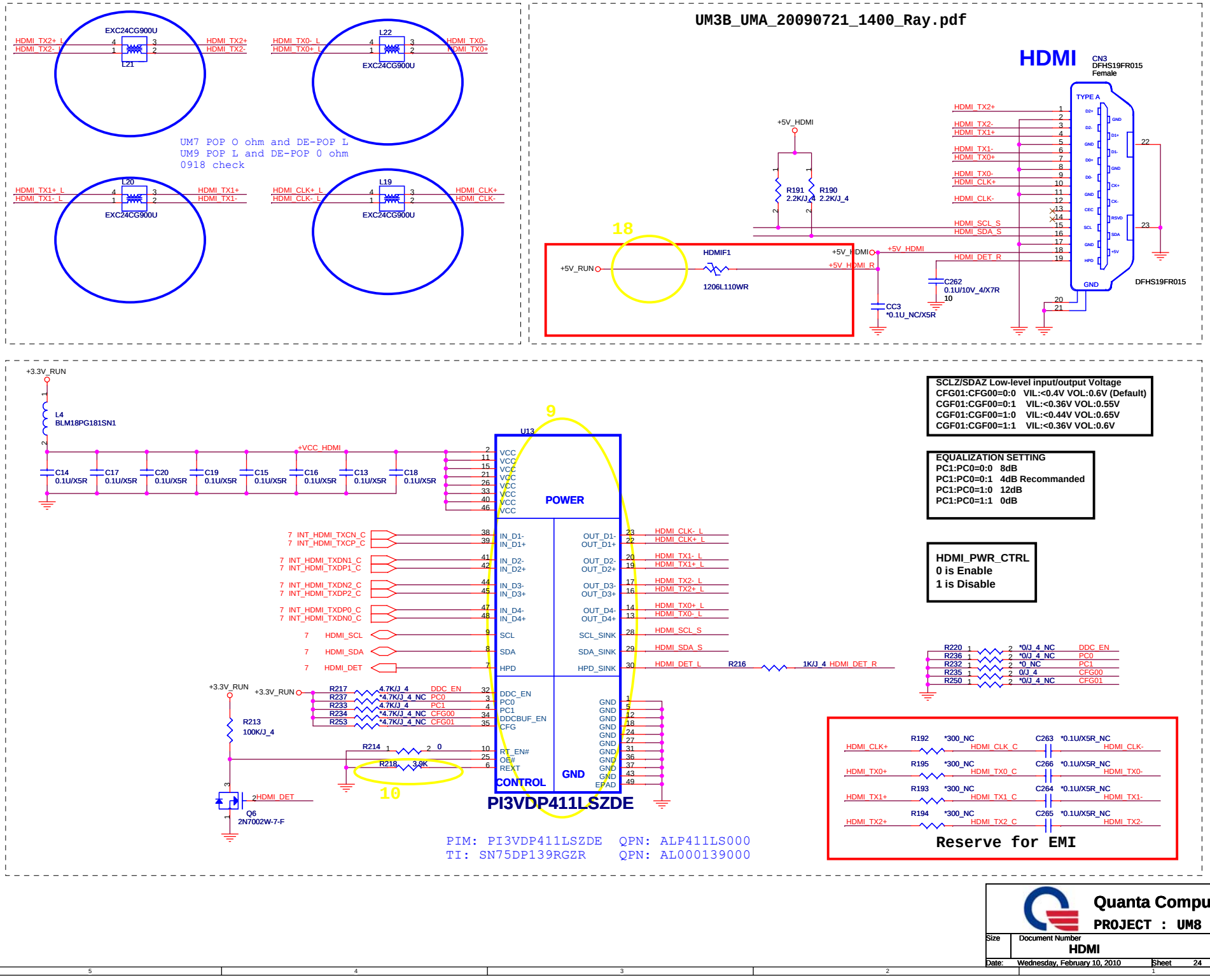
UM3B_UMA_20090721_1400_Ray.pdf
EXC24CG900U
L21
L22
L20
L19
HDMI_TX2+_L
HDMI_TX2-_L
HDMI_TX2+
HDMI_TX2-
HDMI_TX0-_L
HDMI_TX0+_L
HDMI_TX0-
HDMI_TX0+
HDMI_TX1+_L
HDMI_TX1-_L
HDMI_TX1+
HDMI_TX1-
HDMI_CLK+_L
HDMI_CLK-_L
HDMI_CLK+
HDMI_CLK-
UM7 POP 0 ohm and DE-POP L
UM9 POP L and DE-POP 0 ohm
0918 check
HDMI
CN3
DFHS19FR015
Female
TYPE A
DFHS19FR015
+5V_HDMI
R191
2.2K/J_4
R190
2.2K/J_4
HDMI_SCL_S
HDMI_SDA_S
HDMI_DET_R
18
HDMIF1
+5V_RUN
1206L110WR
+5V_HDMI_R
C262
0.1U/10V_4/X7R
10
CC3
*0.1U_NC/X5R
+3.3V_RUN
L4
BLM18PG181SN1
+VCC_HDMI
C14
C17
C20
C19
C15
C16
C13
C18
0.1U/X5R
U13
9
POWER
VCC
IN_D1-
IN_D1+
IN_D2-
IN_D2+
IN_D3-
IN_D3+
IN_D4-
IN_D4+
SCL
SDA
HPD
OUT_D1-
OUT_D1+
OUT_D2-
OUT_D2+
OUT_D3-
OUT_D3+
OUT_D4-
OUT_D4+
SCL_SINK
SDA_SINK
HPD_SINK
DDC_EN
PC0
PC1
DDCBUF_EN
CFG
RT_EN#
OE#
REXT
CONTROL
GND
EPAD
PI3VDP411LSZDE
10
R213
100K/J_4
R214
0
R218
3.9K
R217
R237
R233
R234
R253
4.7K/J_4
*4.7K/J_4_NC
R216
1K/J_4
HDMI_DET_L
Q6
2N7002W-7-F
HDMI_DET
SCLZ/SDAZ Low-level input/output Voltage
CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V
CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB
HDMI_PWR_CTRL
0 is Enable
1 is Disable
R220
R236
R232
R235
R250
*0/J_4_NC
*0_NC
0/J_4
DDC_EN
PC0
PC1
CFG00
CFG01
R192
R195
R193
R194
*300_NC
C263
C266
C264
C265
*0.1U/X5R_NC
HDMI_CLK_C
HDMI_TX0_C
HDMI_TX1_C
HDMI_TX2_C
Reserve for EMI
PIM: PI3VDP411LSZDE QPN: ALP411LS000
TI: SN75DP139RGZR QPN: AL000139000
Quanta Computer Inc.
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HDMI
Rev
1A
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UM3

ITE8502E LQFP-128L

U8

KEYBOARD
KSO17/GPC5
KSO16/GPC3
KSO15
KSO14
KSO13
KSO12/SLCT
KSO11/ERR
KSO10/PE
KSO9/BUSY
KSO8/ACK
KSO7/PD7
KSO6/PD6
KSO5/PD5
KSO4/PD4
KSO3/PD3
KSO2/PD2
KSO1/PD1
KSO0/PD0

KSI7
KSI6
KSI5
KSI4
KSI3/SLIN
KSI2/INIT
KSI1/AFD
KSI0/STB

ADC/DAC
ADC0/GPI0
ADC1/GPI1
ADC2/GPI2
ADC3/GPI3
ADC4/GPI4
ADC5/GPI5
ADC6/GPI6
ADC7/GPI7

DAC0/GPJ0
DAC1/GPJ1
DAC2/GPJ2
DAC3/GPJ3
DAC4/GPJ4
DAC5/GPJ5

LPC
LPCRST/WUI4/GPD2
LPCCLK
LFRAME
LAD0
LAD1
LAD2
LAD3

CLKRUN/GPH0/ID0
SERIRQ
ECSMI/GPD4
ECSCI/GPD3
GA20/GPB5
LPCPD/WUI6/GPE6

KBRST/GPB6
WRST
PWUREQ/GPC7

L80HLAT/GPE0
L80LLAT/WUI7/GPE7

PWM
PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
PWM6/GPA6
PWM7/GPA7

TACH0/GPD6
TACH1/GPD7

TMRI0/WUI2/GPC4
TMRI1/WUI3/GPC6

IR/UART
RXD/GPB0
TXD/GPB1
GPC0
CTX0/GPB2
CRX1/GPH1/ID1
CTX1/GPH2/ID2

SMBUS
SMCLK0/GPB3
SMDAT0/GPB4

SMCLK1/GPC1
SMDAT1/GPC2

SMCLK2/GPF6
SMDAT2/GPF7

LPC/FWH FLASH
FLFRAME/GPG2/LF
FLRST/GPG0/TM
FLAD3/GPG6

FLAD2/SO
FLAD1/SI
FLAD0/SCE
FLCLK

EGPC
EGAD/GPE1
EGCS/GPE2
EGCLK/GPE3

PS/2
PS2CLK0/GPF0
PS2DAT0/GPF1

PS2CLK1/GPF2
PS2DAT1/GPF3

PS2CLK2/GPF4
PS2DAT2/GPF5

GPIO
GPH3/ID3
GPH4/ID4
GPH5/ID5
GPH6/ID6
GPG1/ID7

RI1/WUI0/GPD0
RI2/WUI1/GPD1
WUI5/GPE5

RING/PWRFAIL/LPCRST/GPB7

PWRSW/GPE4

GINT/GPD5

CK32K
CK32KE

VCORE
VSS1
VSS3
VSS4
VSS5
VSS6
VSS7

AVCC
AVSS

ITE8502E
lqfp128-16x16-4

---

28 KSO[0..16]
28 KSI[0..7]

T37 PAD

+3.3V_ALW

C239 10U/ 6.3V_6/X5R 603 6.3
C229 0.1U/16V_4/Y5V 603 16
C223 0.1U/16V_4/Y5V 603 16
C221 0.1U/16V_4/Y5V 603 16
C220 0.1U/16V_4/Y5V 603 16

Place these caps close to ITE8502.

VBAT1
VCC
+3.3V_RUN
VSTBY1
VSTBY2
VSTBY3
VSTBY4
VSTBY5
VSTBY6
+3.3V_ALW

R183 *0_NC
+RTC_CELL
C238 0.1U/16V_4/Y5V 16

HWPG 30,32,39
PAD T29
SUS_PWR_ACK 9
PAD T30
V_ID1
PBAT_PRES# 41
IINP 33
SIO_SLP_S5# 9
SIO_SLP_S5# 9
CRIT_TEMP_REP# 10
SIO_EXT_WAKE# 10
USB_LEFT_EN# 31
FAN1_DA 30
RSMRST# 9
PM_PWRBTN#_R 9
D12 SDMK0340L-7-F

PAD T31
FAN1_PWM 30
PWM_VADJ 22
PAD T32
PAD T33
PAD T22
EC_BEEP 31

FAN1_TACH 30
PANEL_BKEN 7,22

LID_SW# 28
SIO_SLP_S3# 9

PAD T34
H_CPUDET# 3
IMVP_PWRGD 39
RUN_ON 22,35,36,37,40
BAT1_LED 29
IMVP_VR_ON
IMVP_VR_ON 39

SMBDAT0
SMBCLK0
RP9 2.2KX2
SMBDAT1
SMBCLK1
RP10 10KX2
USB_LEFT_EN#
R167 *10K_NC
SUS_ON
R175 100K
IMVP_VR_ON
R164 *100K_NC
+3.3V_RUN
SERIRQ
R184 10K/F_4
SMBDAT2
SMBCLK2
RP11 10KX2

UM7 POP 2.2k
UM9 POP 10k
0918 check
UM7 DE-POP
UM9 POP
0918 check

Check

R327 *0_NC
+3.3V_RUN
R331 *100K_NC
ICH_AZ_CODEC_RST0#
Q19 *2N7002W-7-F_NC
R326 *390K_NC
Q20 *MMST3904-7-F_NC
C352 *0.1U/10V_NC/X7R 10
7,31 ACZ_RST#_AUDIO

3,9,31 PLTRST#
9 CLK_33M_KBC
7,31 LFRAME#
7,31 LAD0
7,31 LAD1
7,31 LAD2
7,31 LAD3
R324 *0_NC

9 CLKRUN#
7 SERIRQ
10 SIO_EXT_SMI#
10 SIO_EXT_SCI#
10 GATEA20
22 LCD_TST
D18 SDMK0340L-7-F
D19 SDMK0340L-7-F
D16 SDMK0340L-7-F

10 RCIN#
D17 SDMK0340L-7-F
WRST#
22 LCD_BAK
LCD_BAK#

31 NB_MUTE#
ICH_AZ_CODEC_RST0#

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

Charge and BAT
PCH
LAN, Clock Thermal IC

33,41 SMBCLK0
33,41 SMBDAT0
8 SMBCLK1
8 SMBDAT1
2,30 SMBCLK2
2,30 SMBDAT2

11
7 PCH_MELOCK
T15 PAD
41 PS_ID
T17 PAD
28 CLK_TP_SIO
28 DAT_TP_SIO

+3.3V_ALW
R328 100K
WRST#
C240 1U/ 10V/Y5V 603 10

ITE8502_XTAL1
ITE8502_XTAL2
ITE8502IX_JX
+3.3V_ALW
L17 BLM11A05S 603
C217 0.1U/16V_4/Y5V 16
L18 BLM11A05S 603

32KHz Clock.
ITE8502_XTAL2
W3
32.768KHZ
C349 18P/50V_4/COG 50
ITE8502_XTAL1
C351 18P/50V_4/COG 50

CLK_33M_KBC
R323 10
C350 2.2P/NPO 50

ITE8502IX_JX
C348 0.1U/16V_4/Y5V 16

R325 *100K_NC
+3.3V_ALW
PAD T36
ACAV_IN 29,33
BAT2_LED 29
D20 SDMK0340L-7-F
AC_PRESENT 9
SYS_PWR_SW# 29
LCDVCC_TST_EN 22

Madison
Discrete
Park
UMA
8
23
+3.3V_ALW
R161 10K
R179 *10K_NC
R168 *10K_NC
R174 10K
R172 10K
R170 *10K_NC
R166 *10K_NC
R178 10K
R165 10K
R173 *10K_NC
R171 *10K_NC
R169 10K
USB_RIGHT_EN#
BID1
LCD_SIZE_ID
BID2
LCD_SIZE_ID2
V_ID1
VGA_TYPE
VGA_IDENTIFY

	LCD_SIZE_ID (99)	LCD_SIZE_ID2 (107)
13"	0	0
14"	1	0
17"	0	1

BID1	USB_RIGHT_EN#	UM9(UMA)	UM9C (Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	QT (A00)	QT (A00)
0	0	(A01)	(A01)

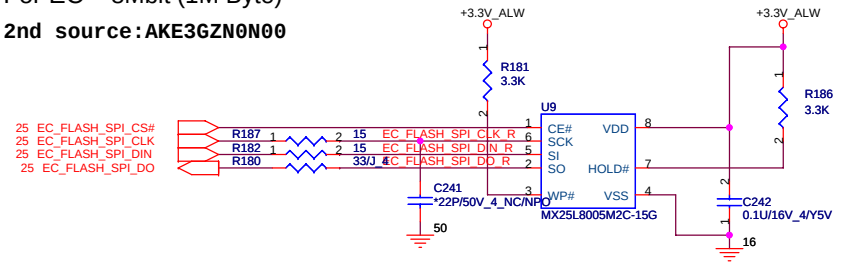
Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	SIO ITE8502	1A
Date: Wednesday, February 10, 2010	Sheet 25 of 46	

UM3

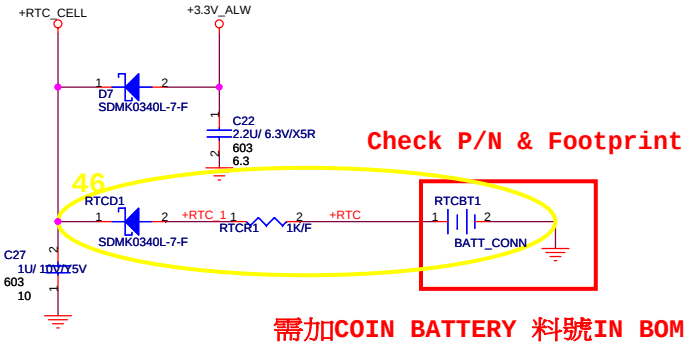
For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00

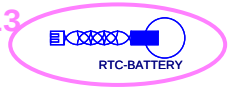


MACRONIX: MX25L3205DM2I-12G QPN: AKE39FP0Z00
WINBOND: W25X32VSSIG QPN: AKE39ZP0N00

RTC BATTERY



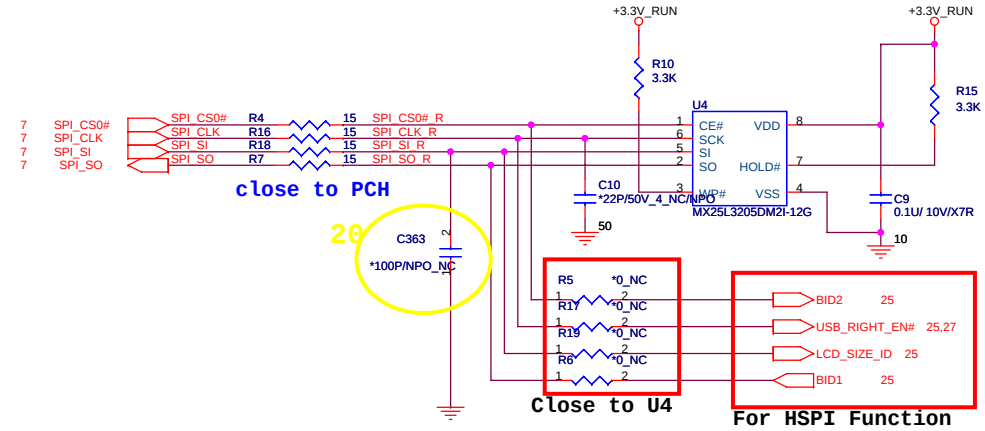
13



For PCH

32Mbit (4M Byte)

MACRONIX: MX25L8005M2C-15G QPN: AKE5GFK0Z09
WINBOND: W25X80AVSSIG QPN: AKE39ZP0N00

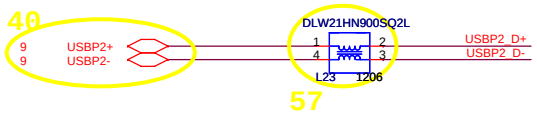


Quanta Computer Inc.
PROJECT : UM8 UMA

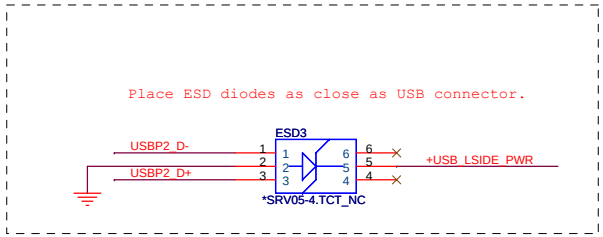
Size	Document Number	Rev
	FLASH/RTC	1A
Date: Wednesday, February 10, 2010	Sheet 26 of 46	

eSATA and USB To DB

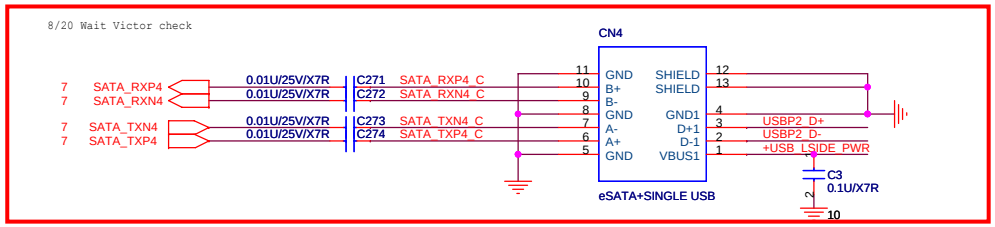
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

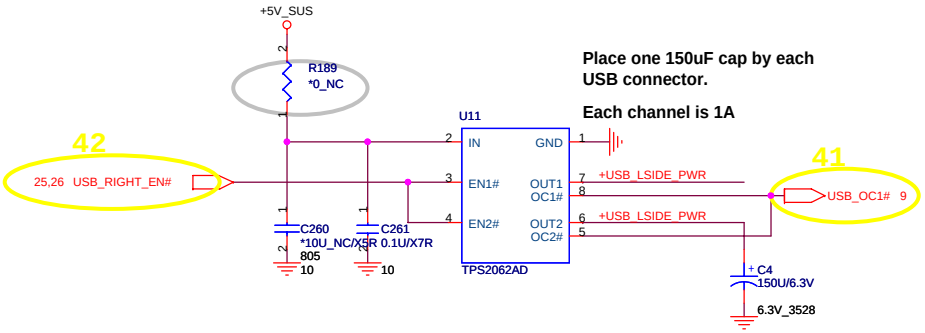


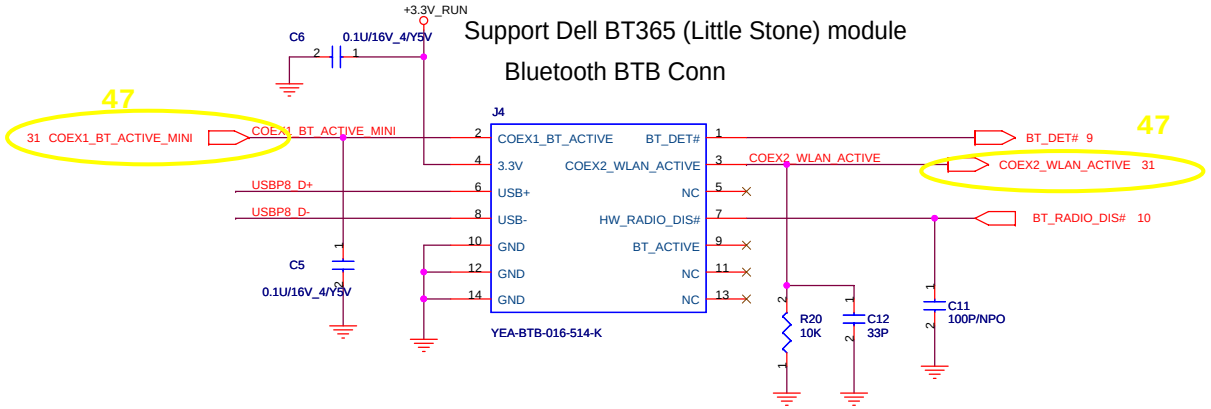
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

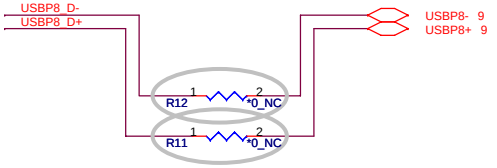


USB and eSATA Conn.









Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	eSATA & Right USB	1A

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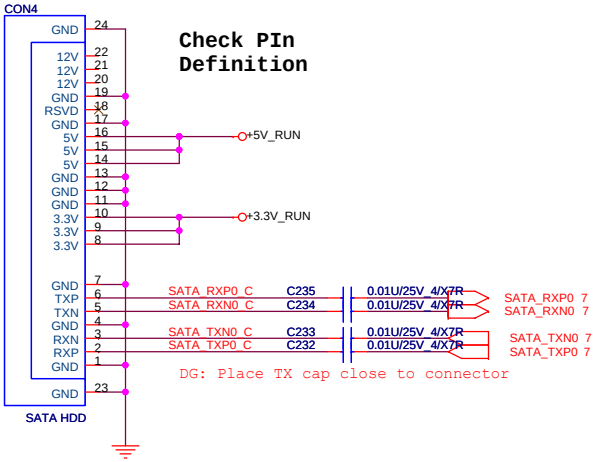
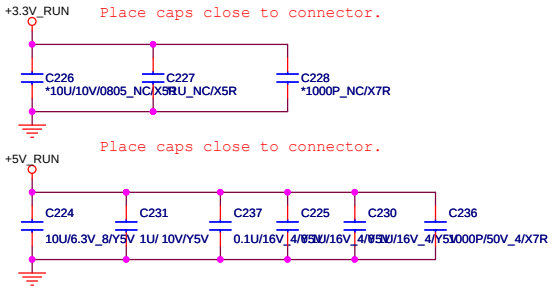
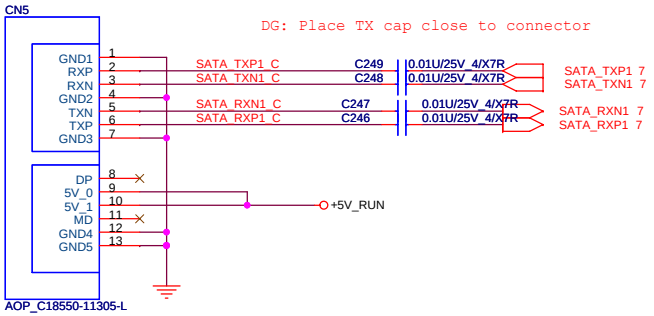
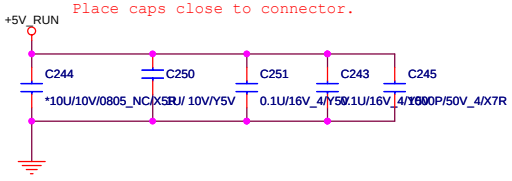
SATA Connector.

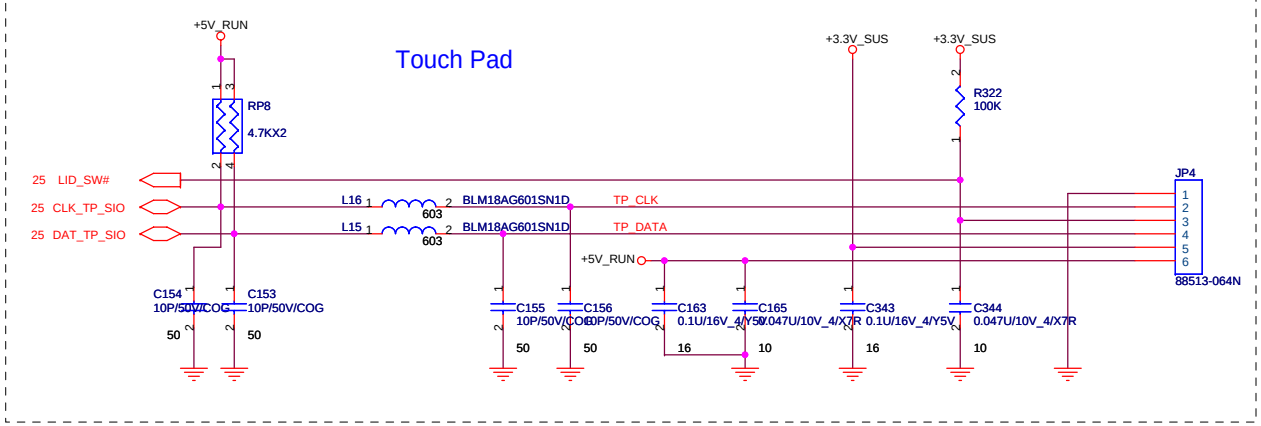




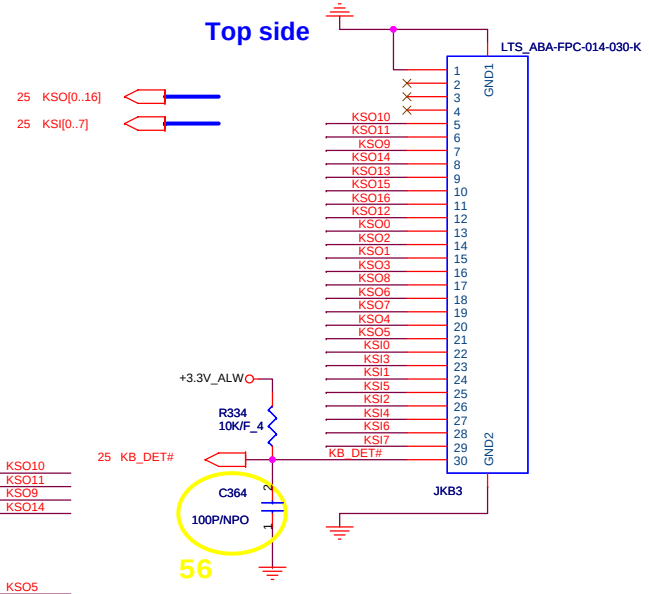
ODD Connector

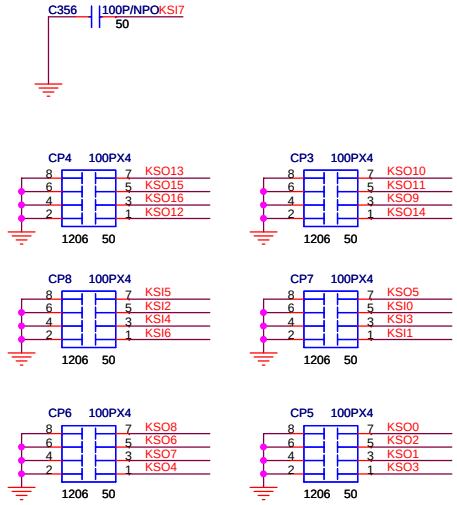






KEYBOARD CONNECTOR





100P CAPS CLOSE TO JKB1

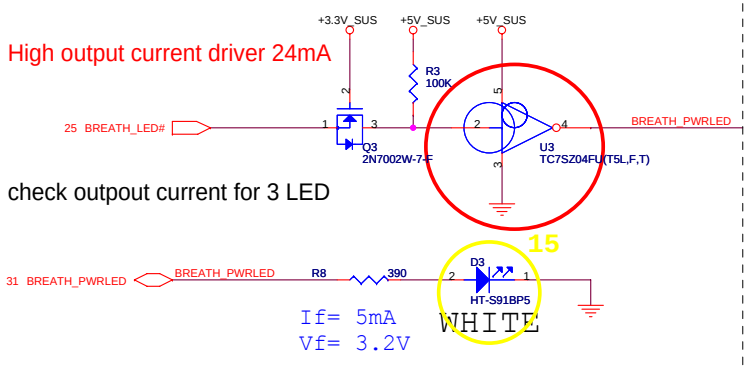
Quanta Computer Inc.

PROJECT : UM8 UMA

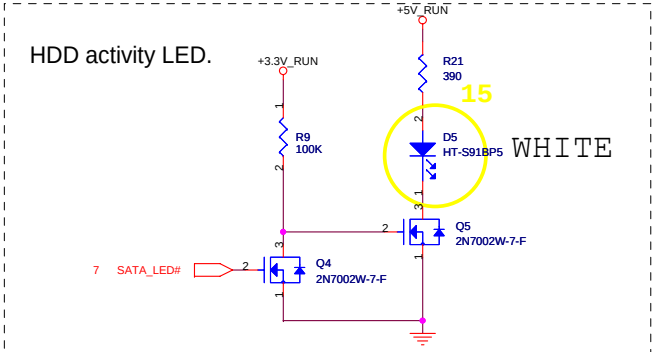
Size	Document Number	Rev
	SATA (HDD&ODD) & TP & KB	1A
Date: Wednesday, February 10, 2010	Sheet 28 of 46	

Power

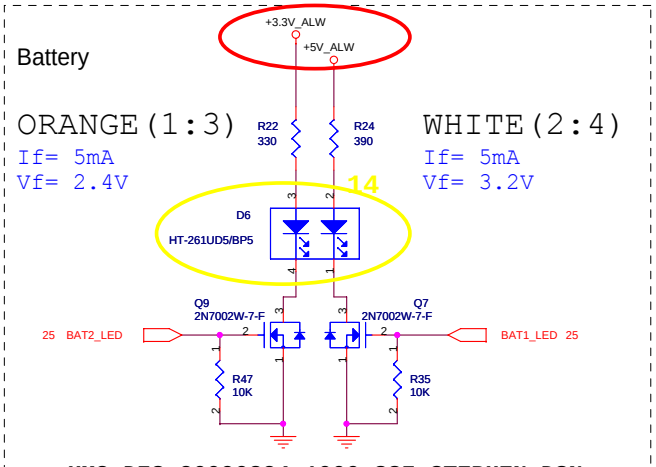
High output current driver 24mA



HDD activity LED.

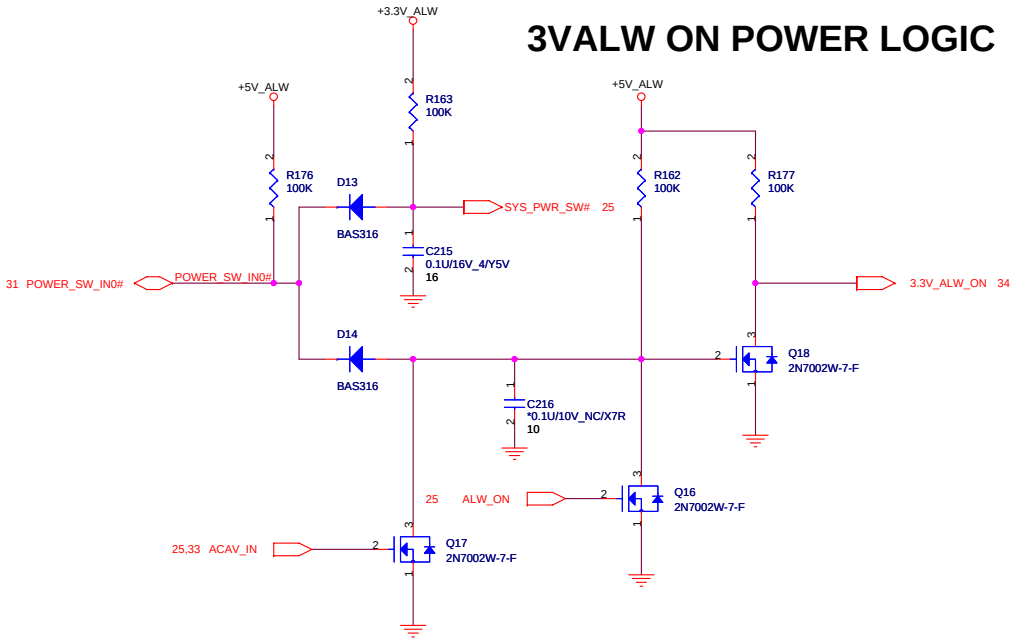


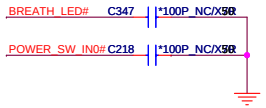
Battery



UM3_DIS_20090824_1000_SSI_STEPHEN.DSN

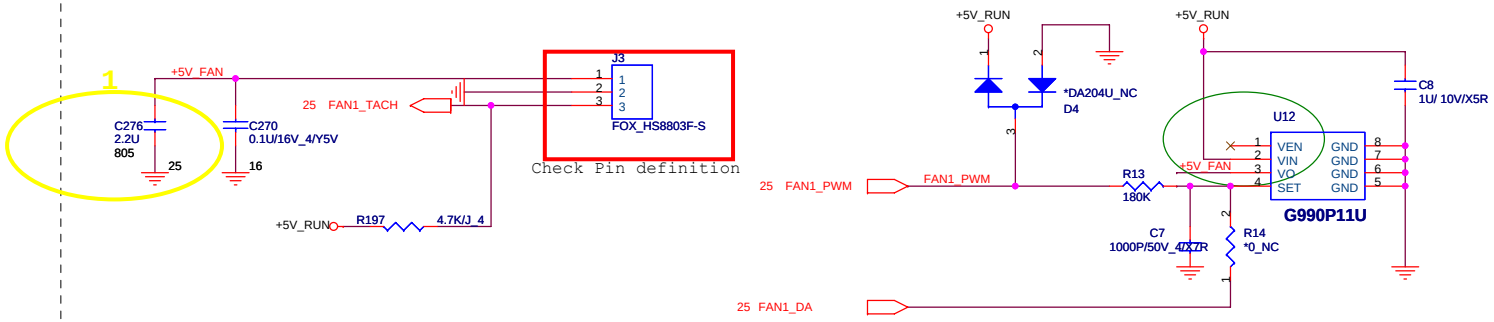
3VALW ON POWER LOGIC

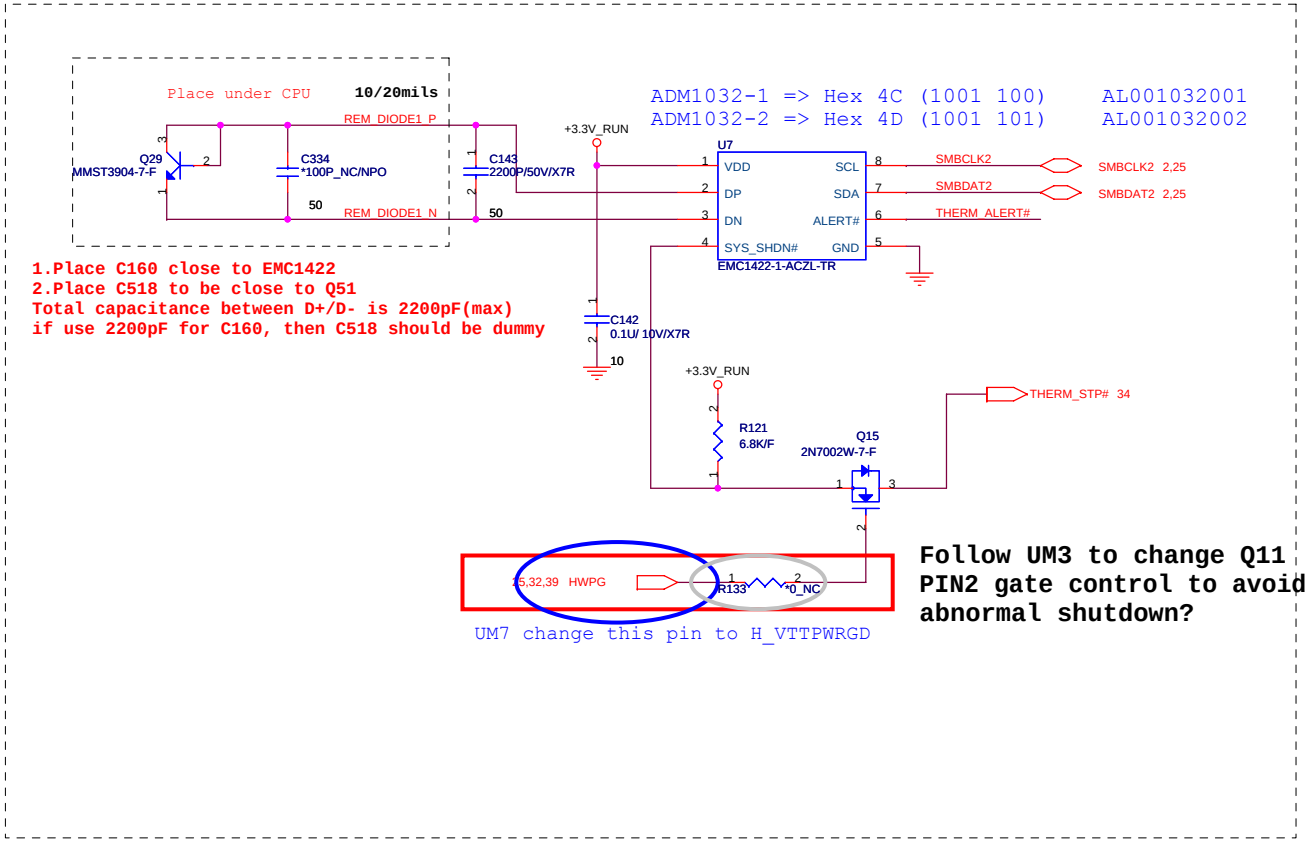




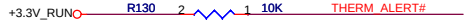
Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: SWITCH, LED	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 29 of 46	

FAN CONTROL





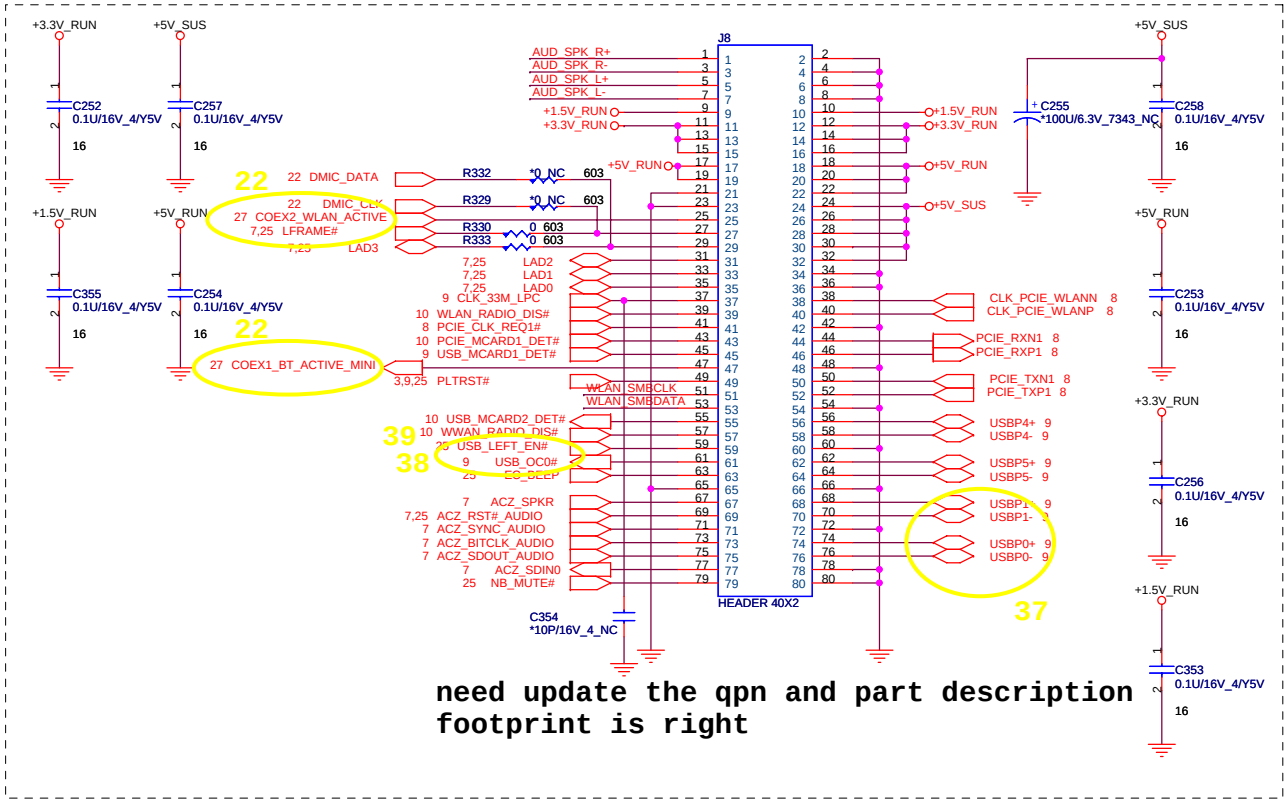
OTP 85 degree C



SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

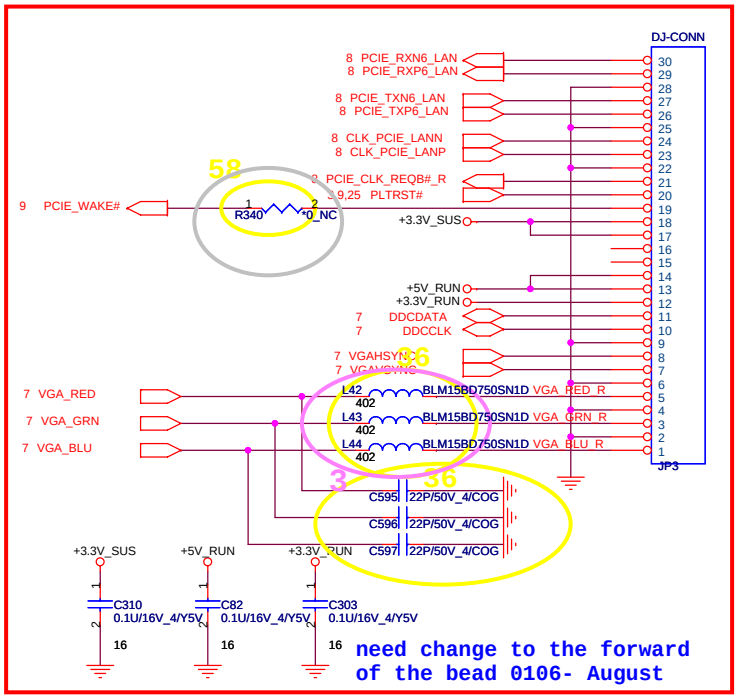
Quanta Computer Inc.
PROJECT : UM8 UMA

Size	Document Number	Rev
	FAN & THERMAL	1A
Date: Wednesday, February 10, 2010	Sheet 30 of 46	



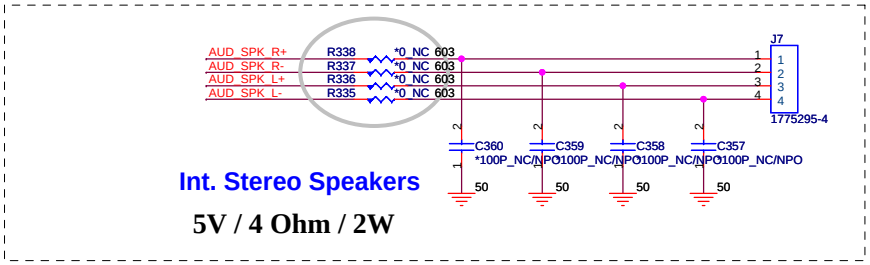
need update the qpn and part description
footprint is right

Check P/N and footprint



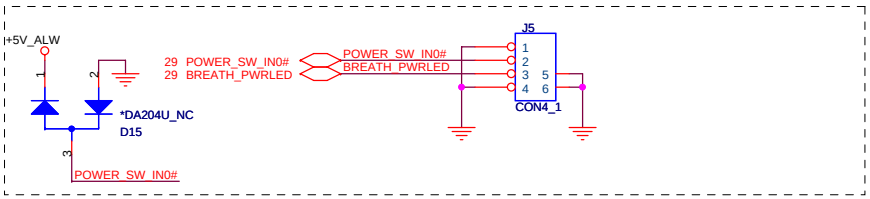
need change to the forward of the bead 0106- August

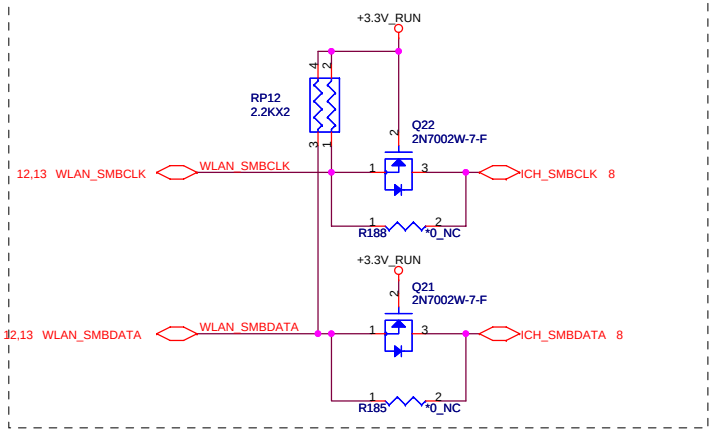
To CRT board



Int. Stereo Speakers

5V / 4 Ohm / 2W

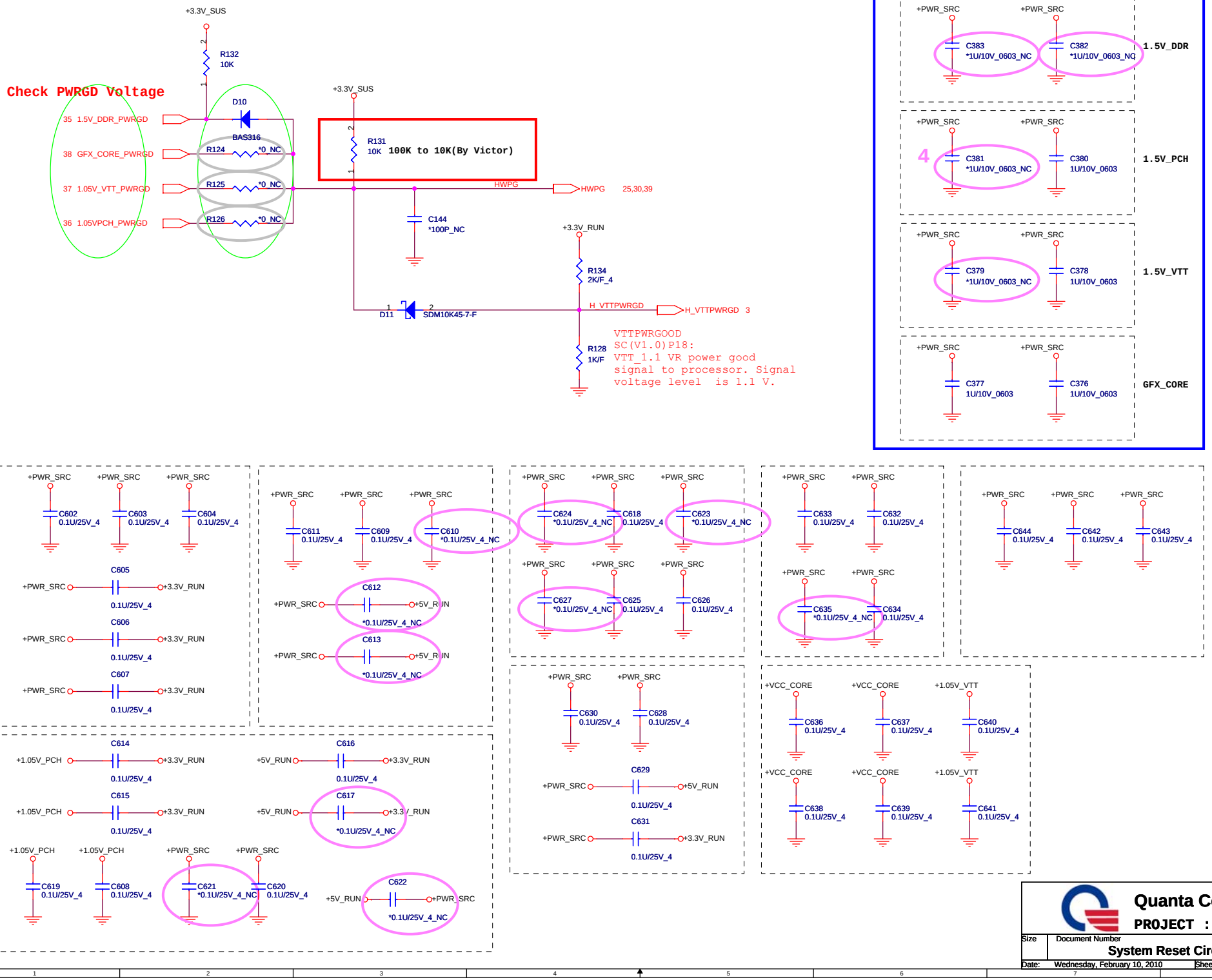




Quanta Computer Inc.

PROJECT : UM8B DIS

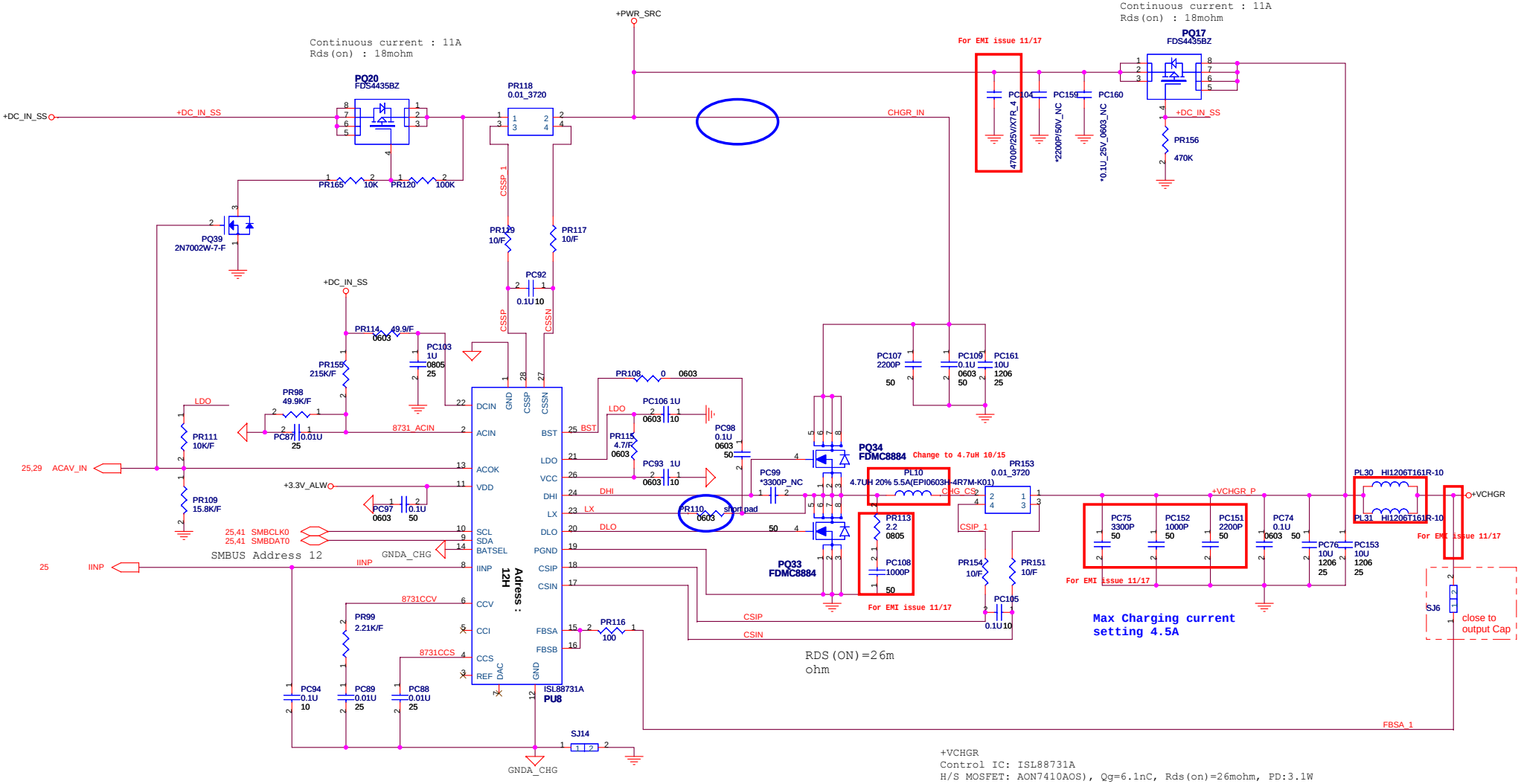
Size	Document Number	Rev
	BTB CONN & Audio conn	1A
Date: Wednesday, February 10, 2010	Sheet 31 of 46	



Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	System Reset Circuit	1A
Date: Wednesday, February 10, 2010	Sheet 32 of 46	

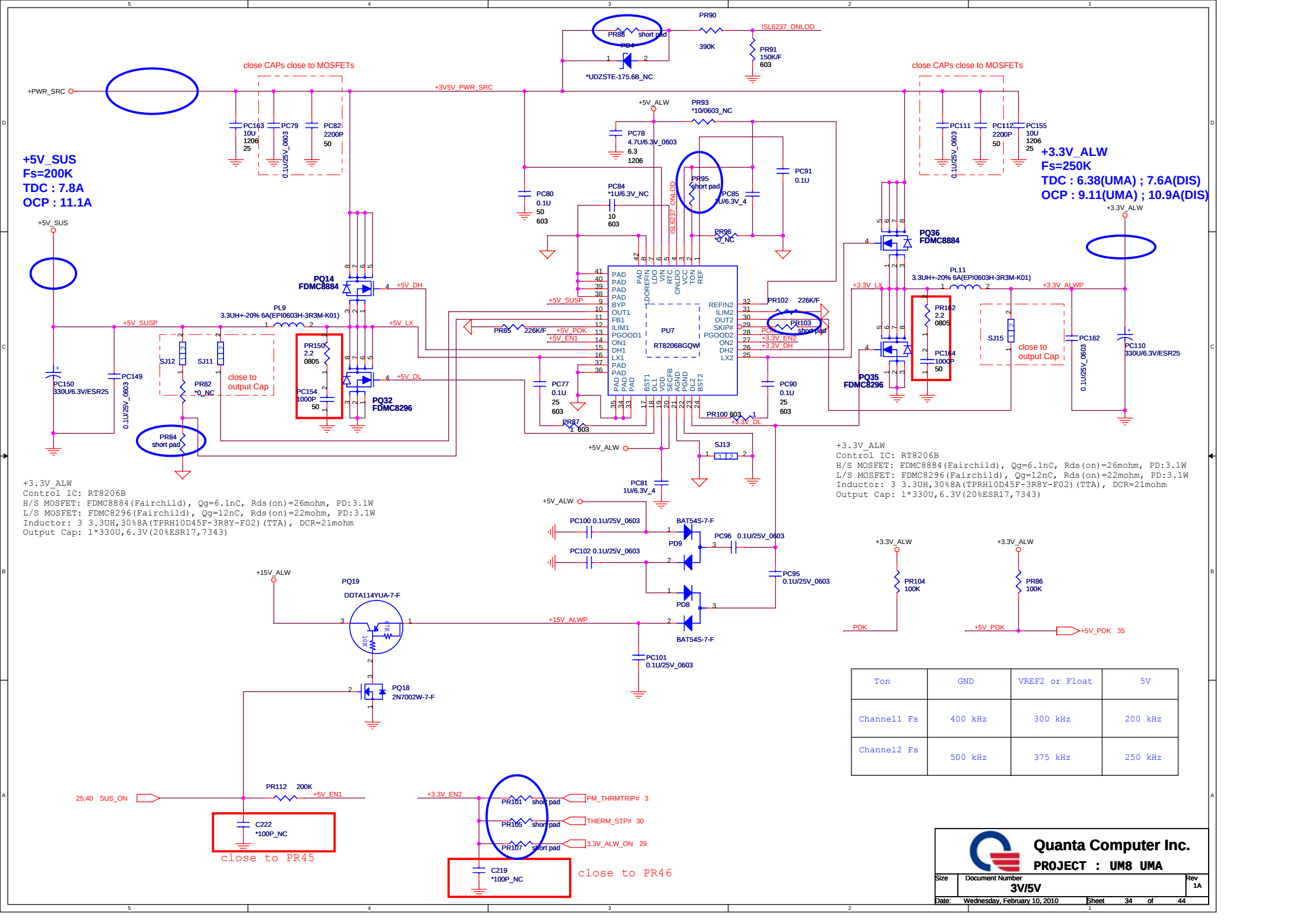


Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Charger	1A

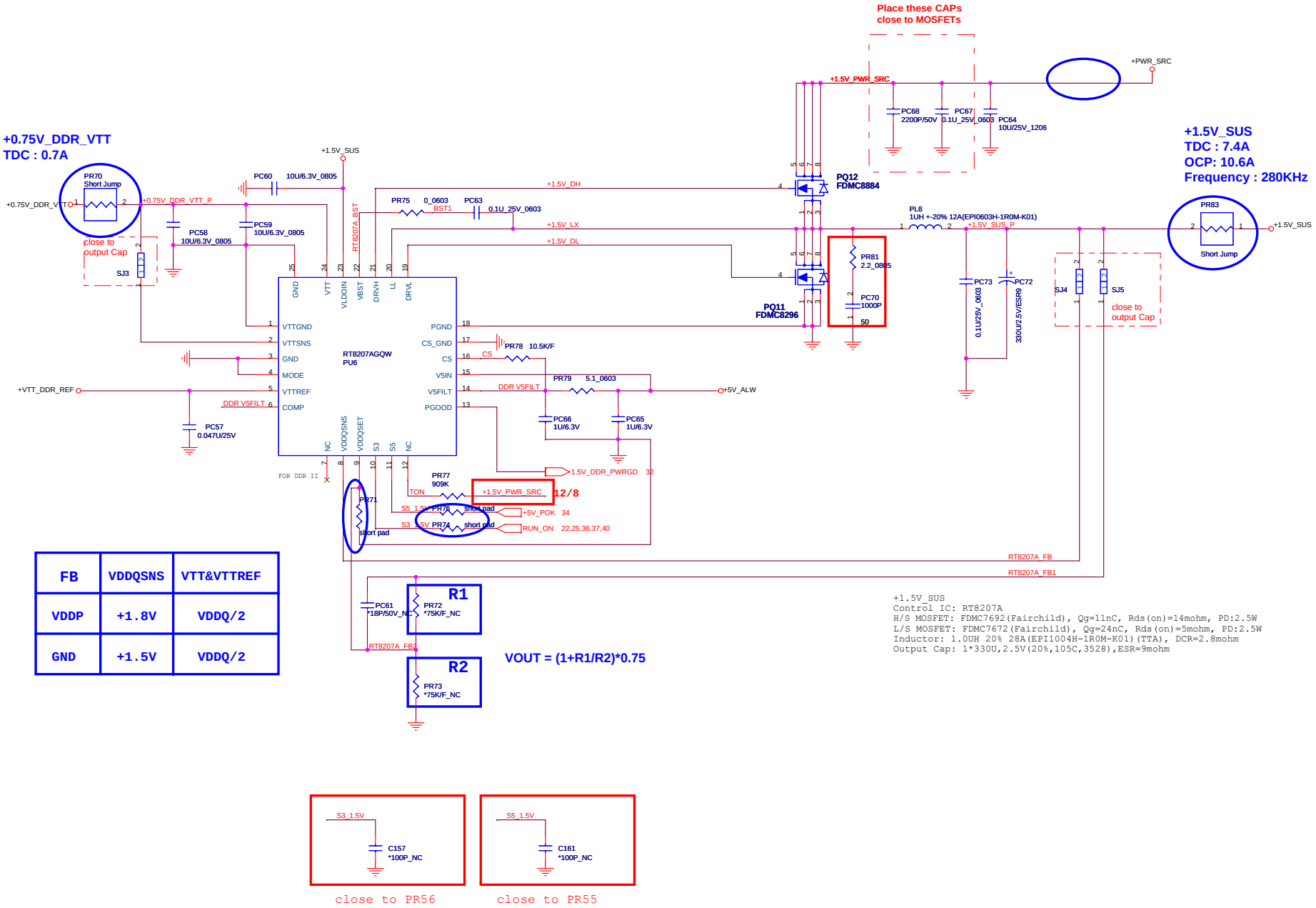
Date: Wednesday, February 10, 2010 Sheet 33 of 44



Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

Quanta Computer Inc.
PROJECT : UM8 UMA

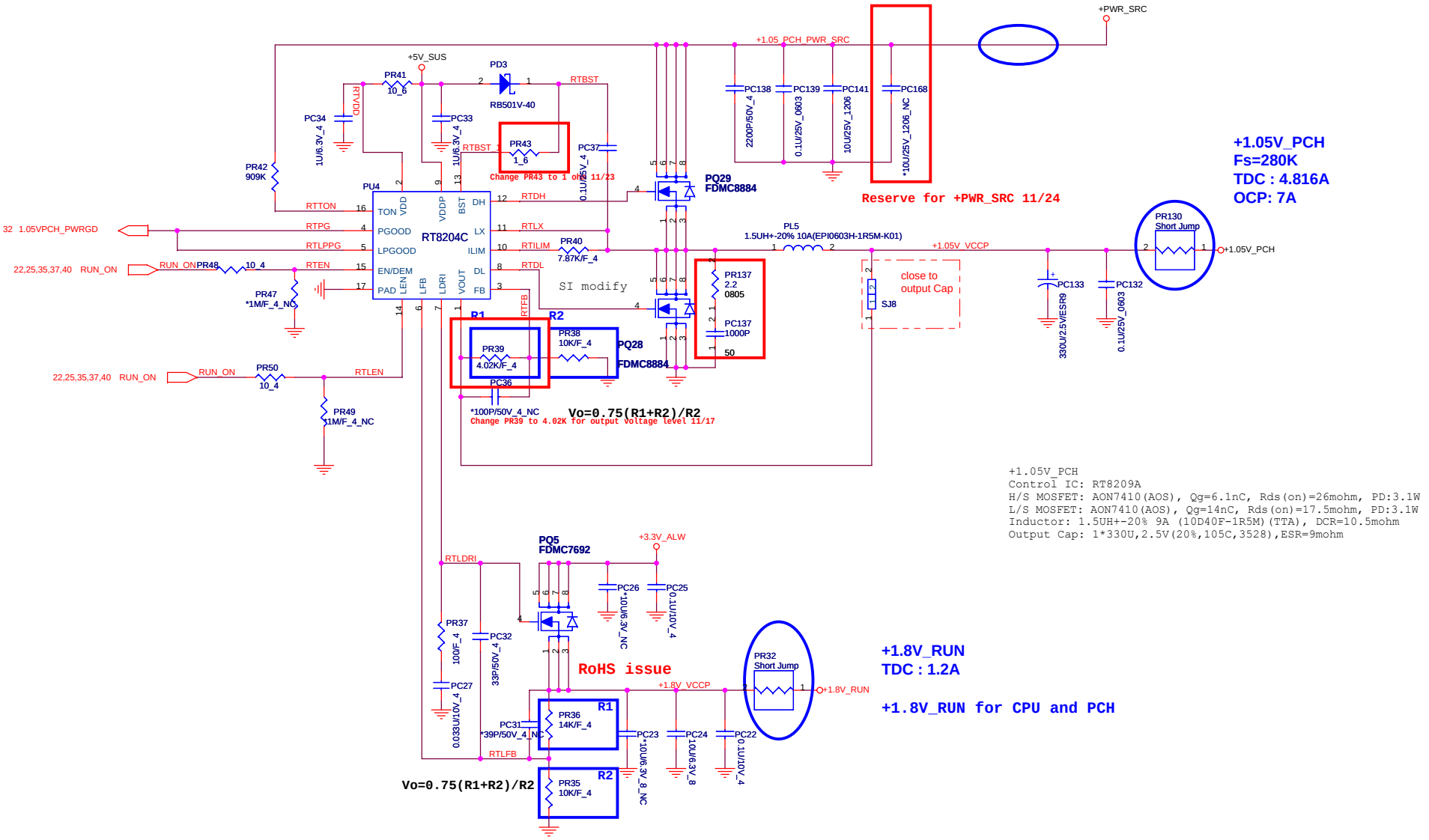
Size	Document Number	Rev
	3V/5V	1A
Date: Wednesday, February 10, 2010	Sheet 34 of 44	



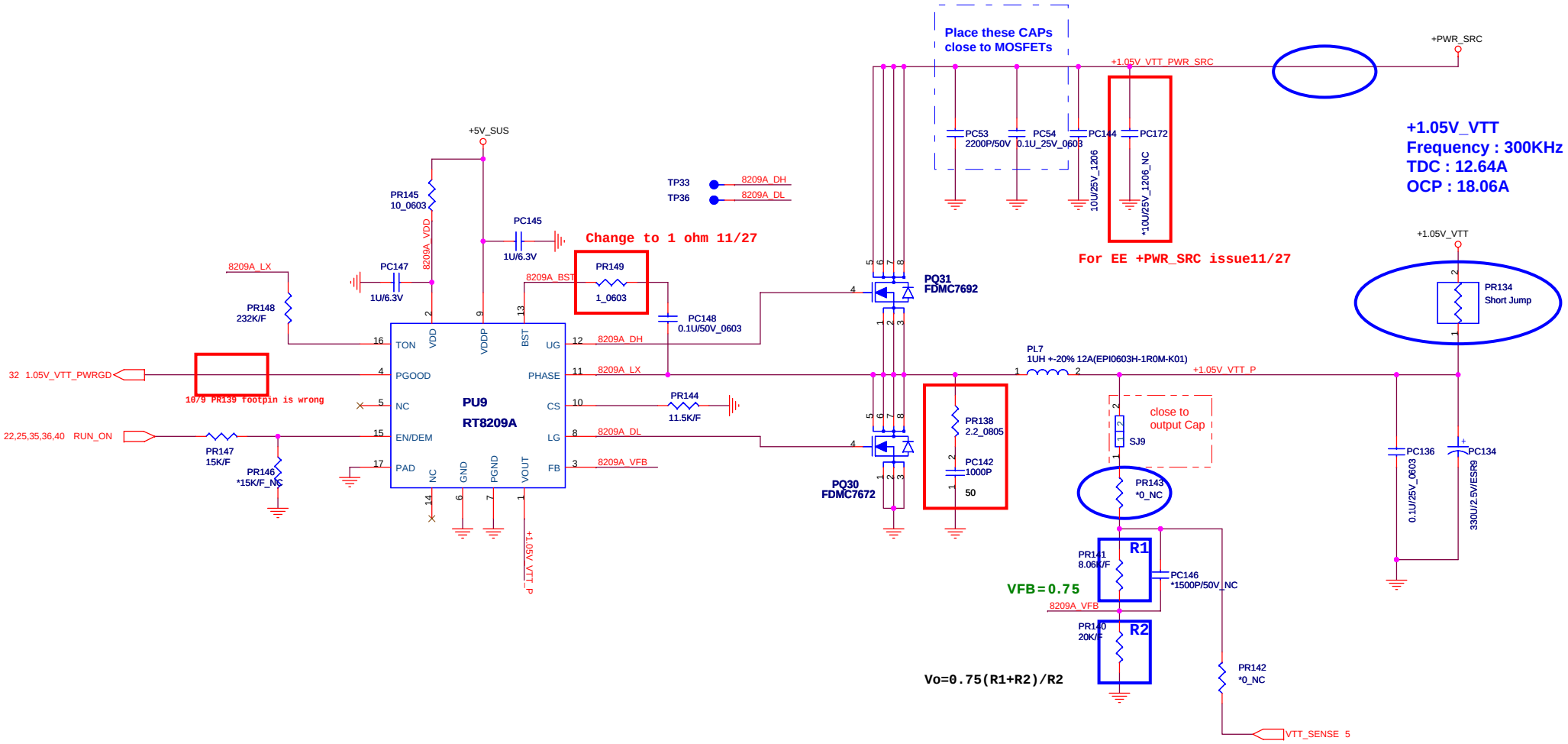
FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMC7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMC7672(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 1.0UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 1*330U,2.5V(20%,105C,3528),ESR=9mohm

Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: 1.5V_DDR	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 35 of 44	

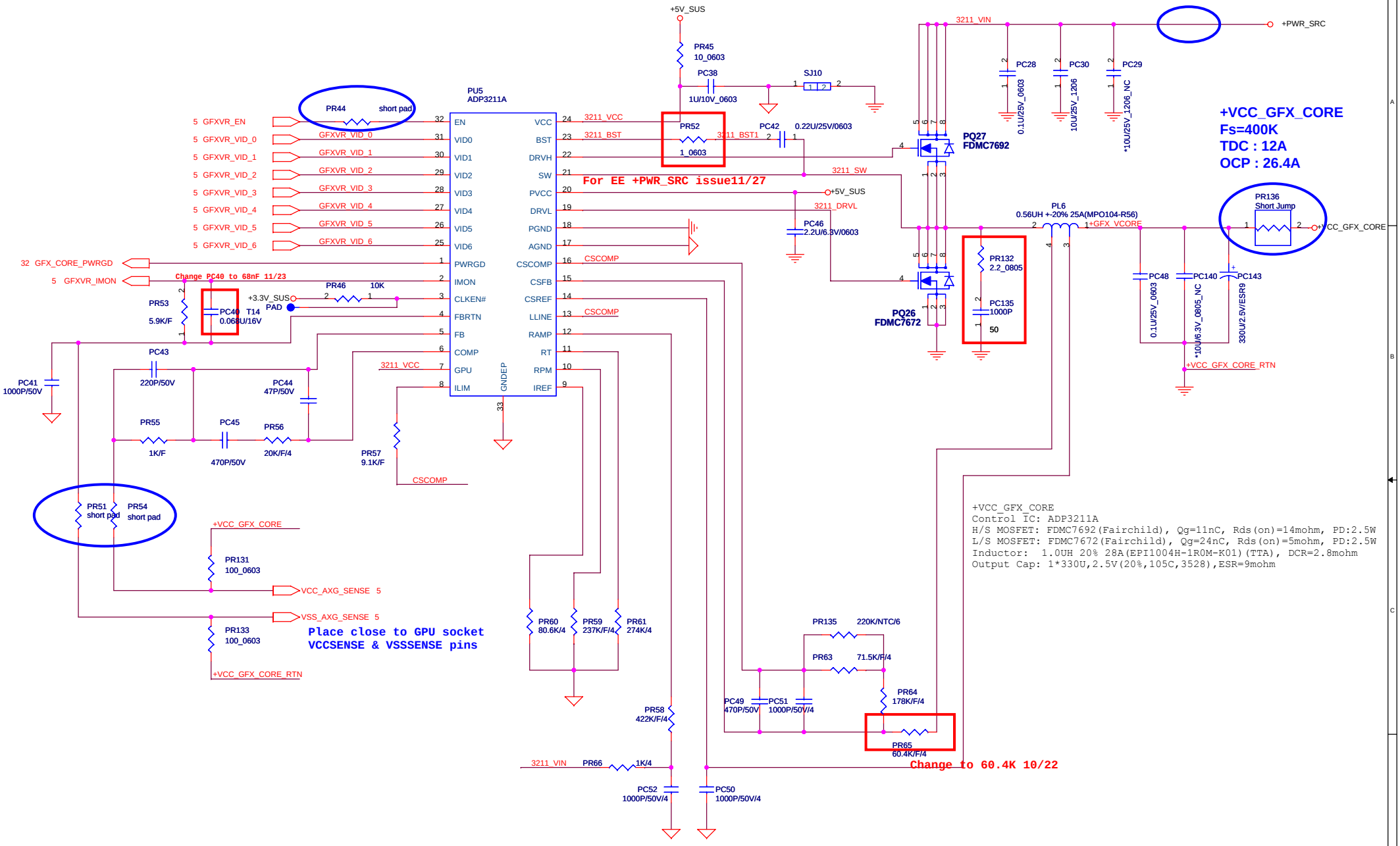


Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: 1.05_PCH	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 36 of 44	

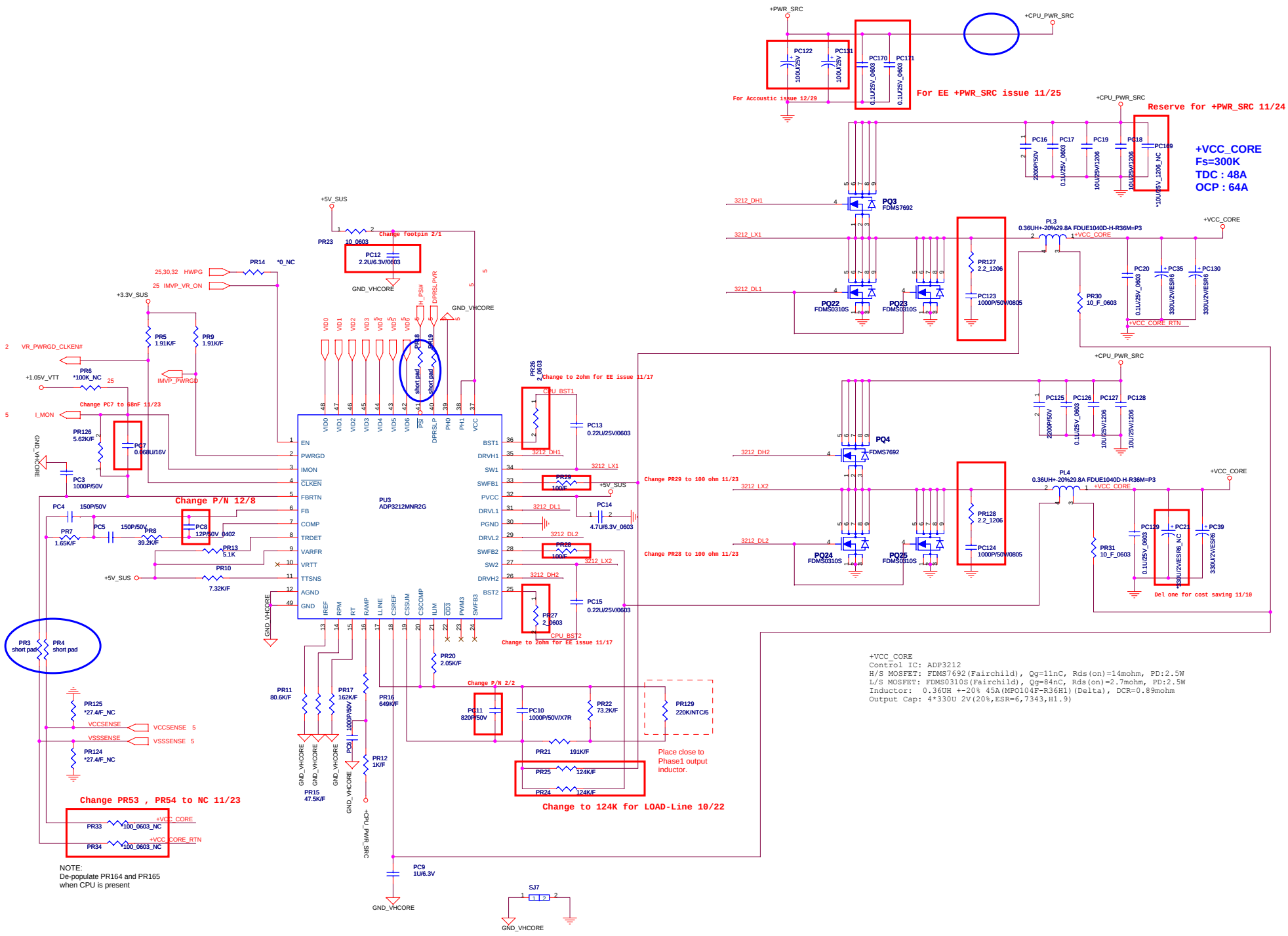


+1.05V_VTT
Control IC: RT8209A
H/S MOSFET: FDMC7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMC7672(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 1.0UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 1*330U,2.5V(20%,105C,3528),ESR=9mohm

Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: 1.05_VTT	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 37 of 44	



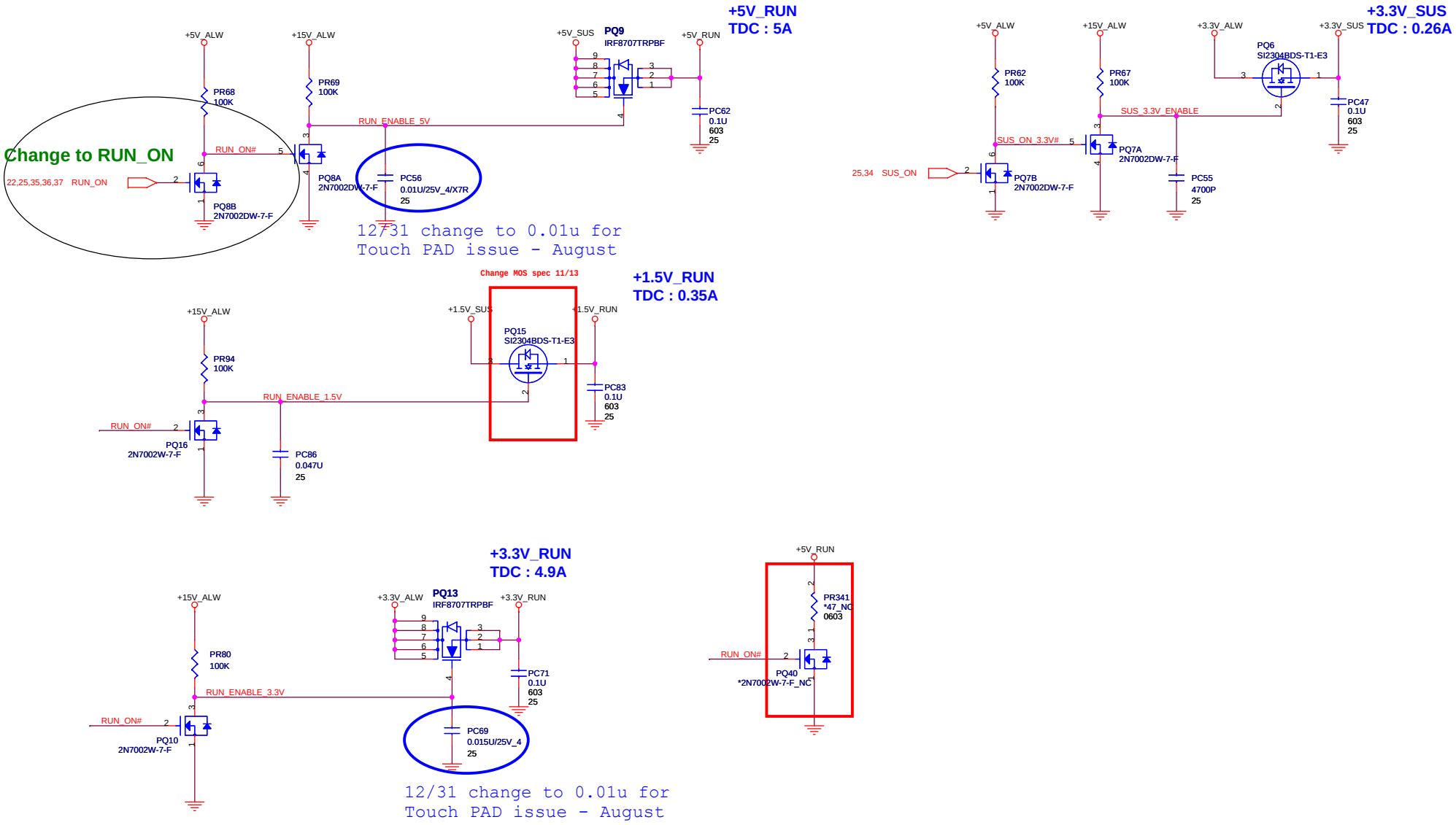
Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: GFX_CORE	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 38 of 44	



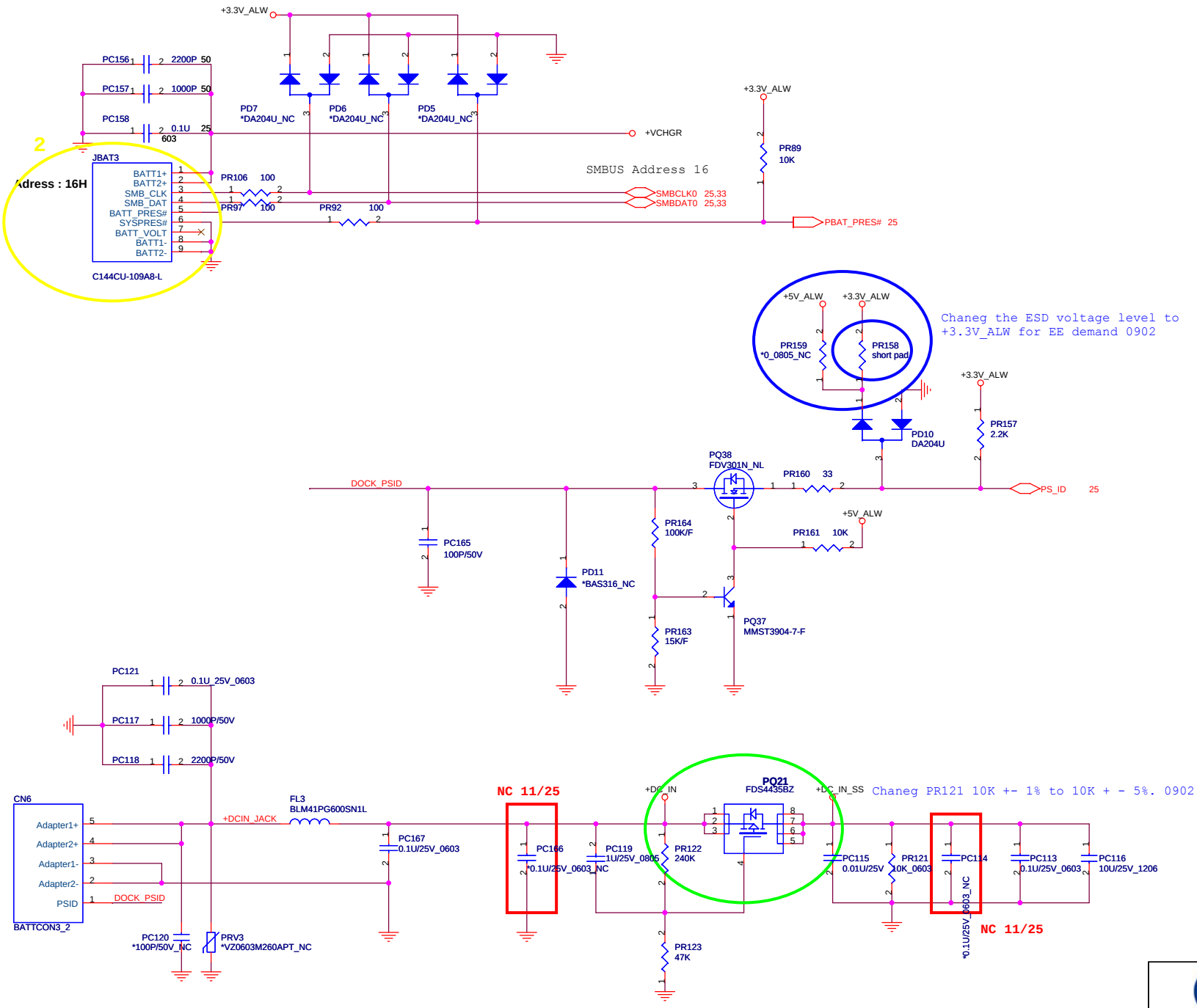
Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	CPU CORE	1A
Date: Wednesday, February 10, 2010	Sheet 39 of 44	



Quanta Computer Inc.		
PROJECT : UM8 UMA		
Size	Document Number: Run Power Switch	Rev: 1A
Date: Wednesday, February 10, 2010	Sheet 40 of 44	

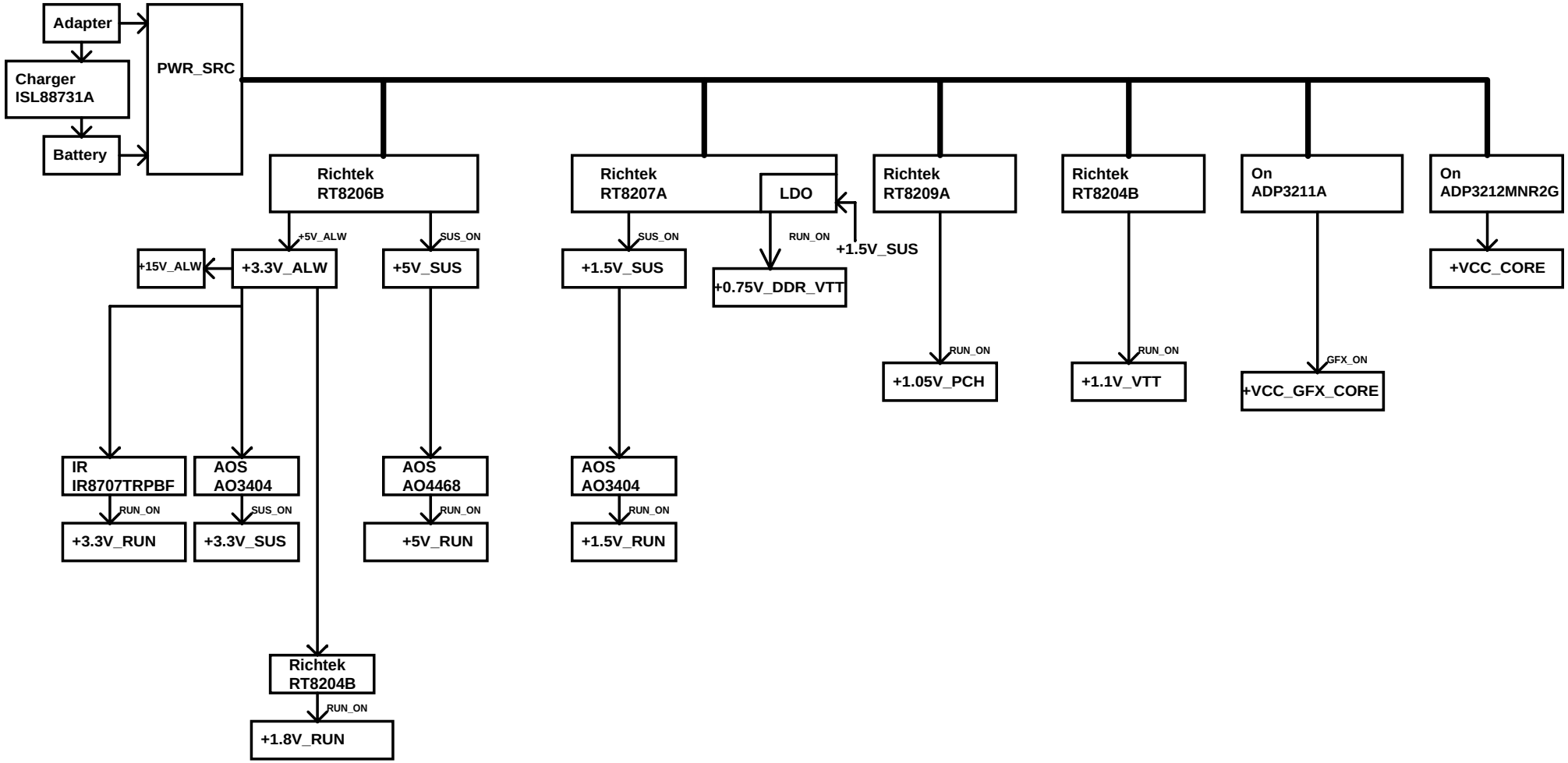


Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Batt & DC-IN	1A
Date: Wednesday, February 10, 2010	Sheet 41 of 44	

VER : 1A

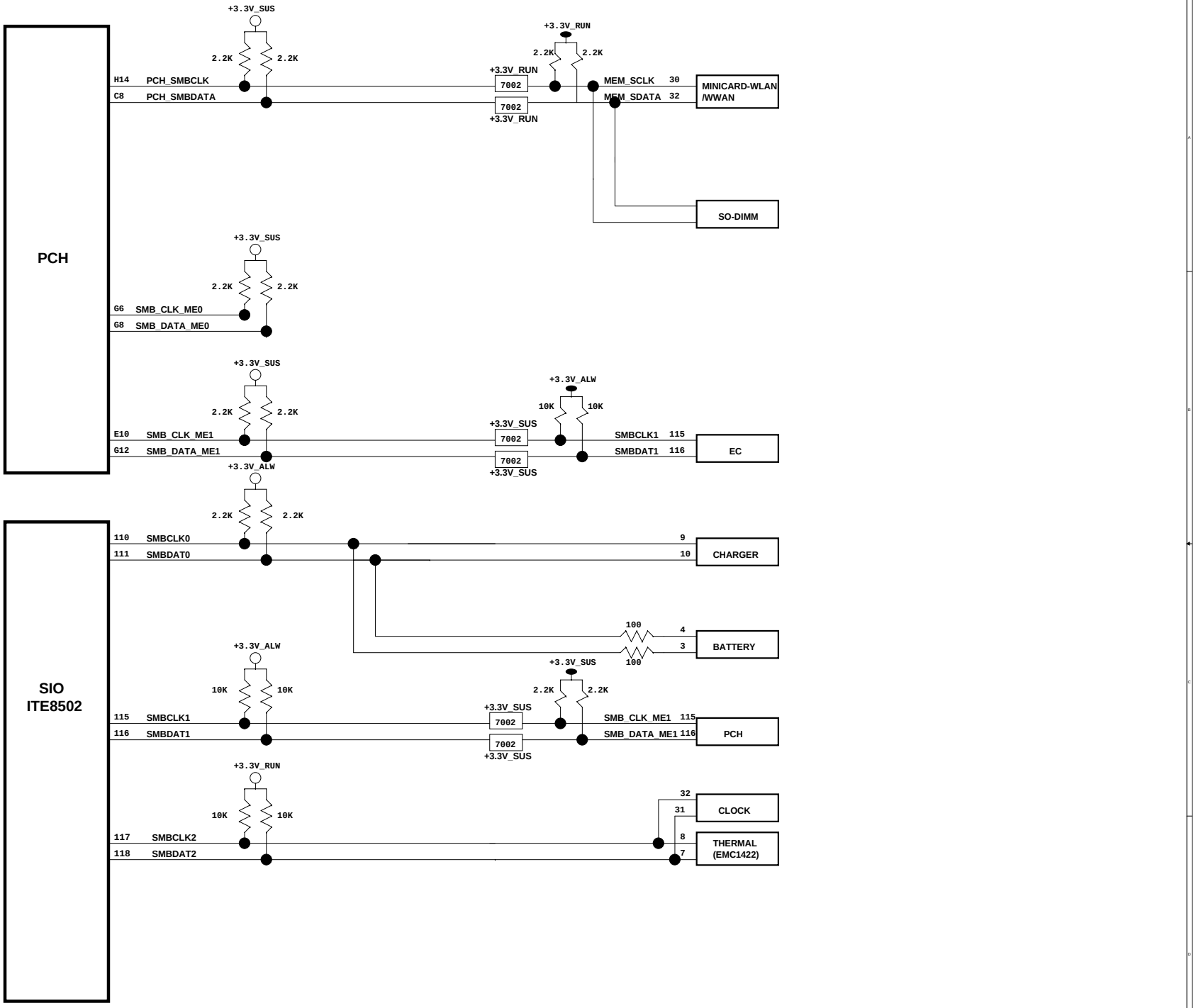


Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	Schematic Block Diagram1	1A

Date: Wednesday, February 10, 2010 Sheet 42 of 46



Quanta Computer Inc.

PROJECT : UM8 UMA

Size	Document Number	Rev
	SMBUS BLOCK	1A

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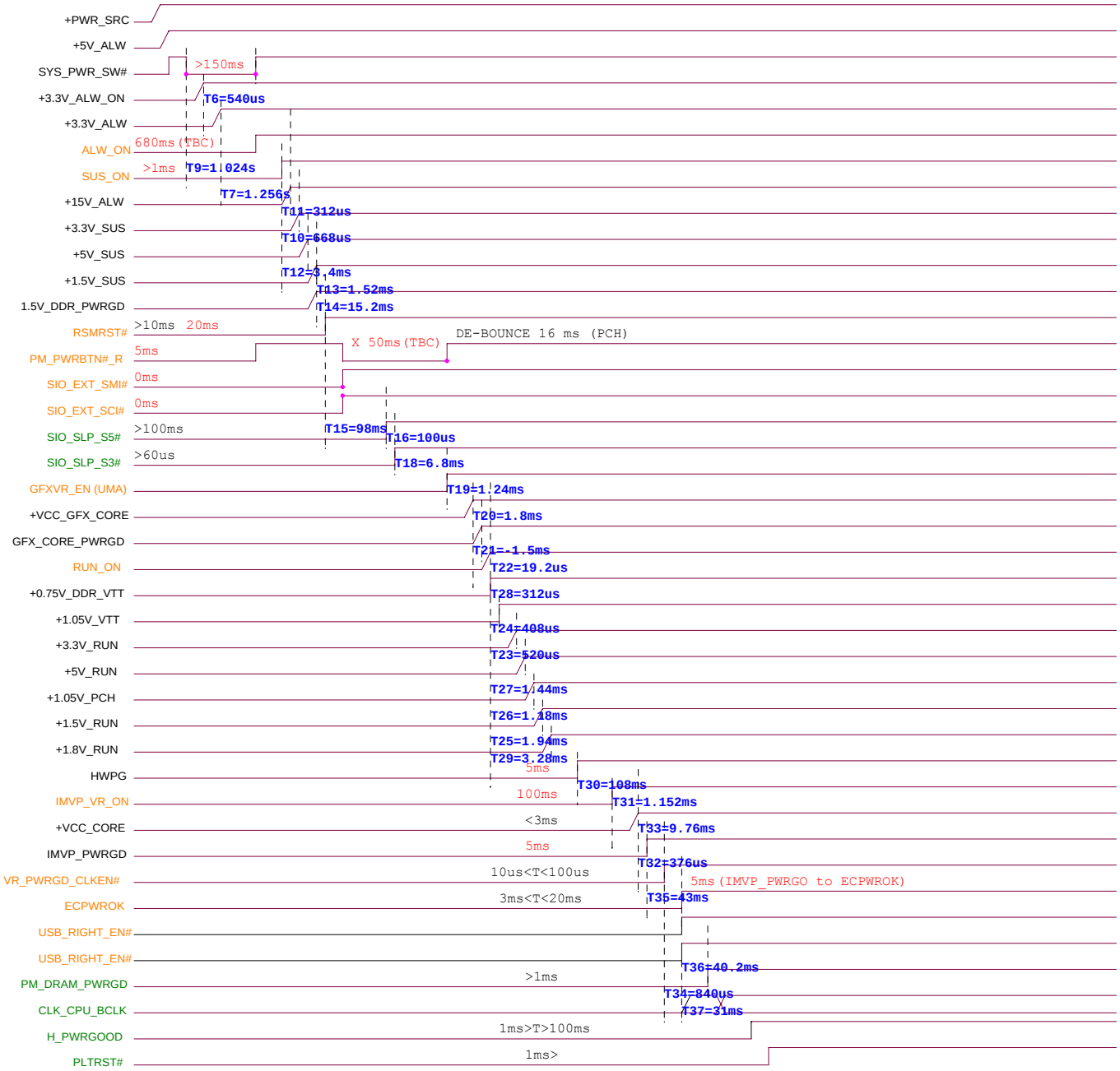
UM8_ X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



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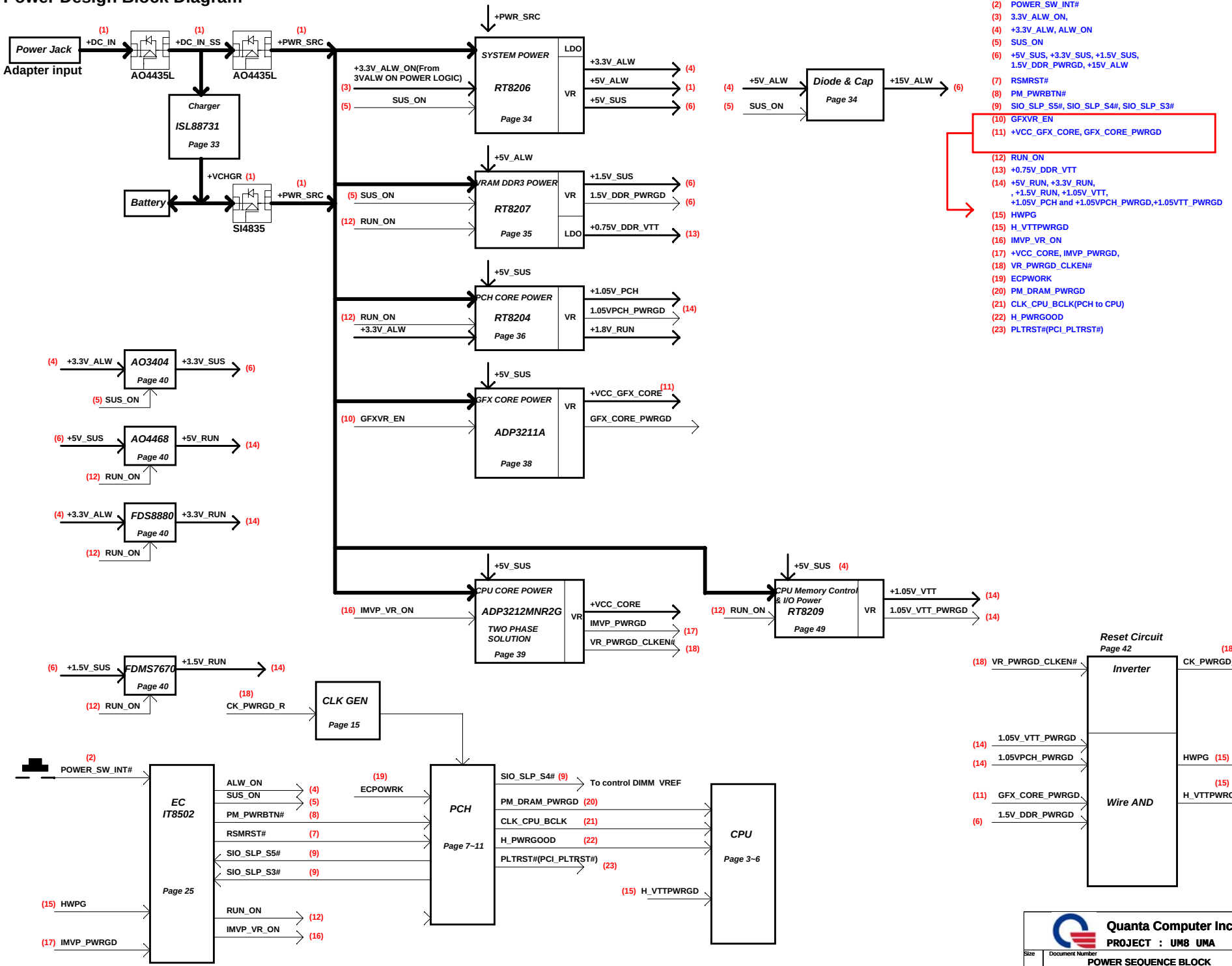
Power Design Block Diagram



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW
(2) POWER_SW_INT#
(3) 3.3V_ALW_ON,
(4) +3.3V_ALW, ALW_ON
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD, +15V_ALW
(7) RSMRST#
(8) PM_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFXVR_EN
(11) +VCC_GFX_CORE, GFX_CORE_PWRGD
(12) RUN_ON
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, , +1.5V_RUN, +1.05V_VTT, +1.05V_PCH and +1.05VPCH_PWRGD,+1.05VTT_PWRGD
(15) HWPG
(15) H_VTTPWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD,
(18) VR_PWRGD_CLKEN#
(19) ECPWORK
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

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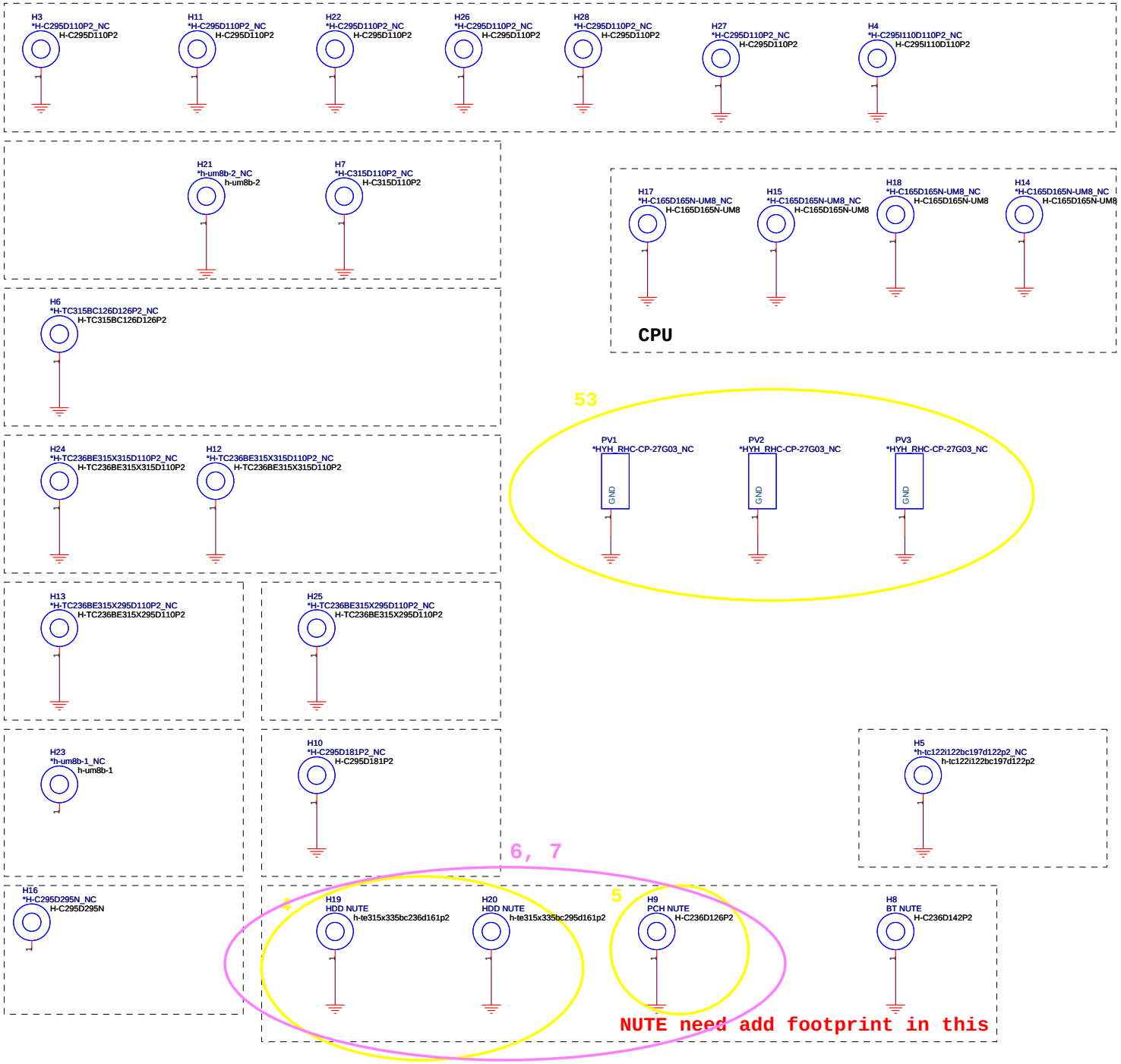

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