LCFC Confidential

NM-A221 Rev1.0 Schematic

Intel Crescent Bay Processor with DDRIIIL + Wild Cat Point PCH
AMD Opal-XT/ Jet-XT

2013-09-07 Rev1.0

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Issued Date	2013/09/07	Deciphered Date	2014/09/07

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Title: COVER PAGE

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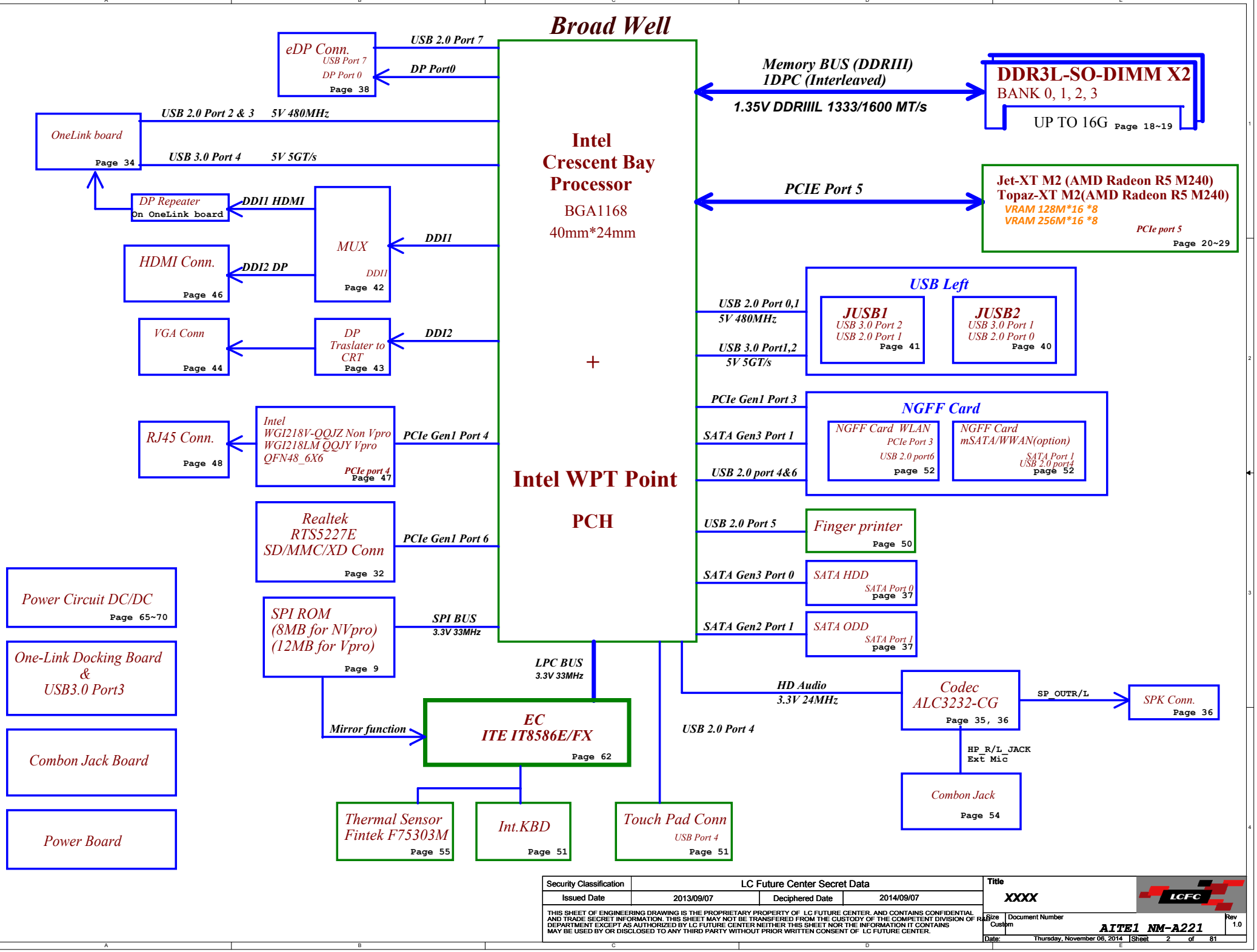

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	Main VGA	LAN	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Charger
PCH_SML0_CLK PCH_SML0_DAT	PCH +3V_PCH	X	V +3V_PCH	X	X	X	X	X	X	X	X
PCH_SML1CLK PCH_SML1DATA	PCH +3V_PCH	V +3VS	X	X	V +3VS	X	X	V +3VS	X	X	X
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL	X	X	V +3VL	X	X	X	X	X	X	V +3VL
PCH_SMBCLK PCH_SMBDATA	PCH +3V_PCH	X	X	X	X	V +3VS	X	X	V +3V_PCH	V +3VS	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

High Speed I/O port

I/O	High Speed Signal	Configuration	Port assignment
1	USB3 1	USB3 1	On MB USB
2	USB3 2	USB3 2	On MB USB
3	PCIE 1 / USB3 3	NC	NC
4	PCIE 2 / USB3 4	USB3 4	Docking USB
5	PCIE 3	PCIE 3	WLAN
6	PCIE 4	PCIE 4	LAN
7	PCIE 5 L0	PCIE 5 L0	GPU
8	PCIE 5 L1	PCIE 5 L1	GPU
9	PCIE 5 L2	PCIE 5 L2	GPU
10	PCIE 5 L3	PCIE 5 L3	GPU
11	PCIE 6 L0 / SATA 3	PCIE 6	Cardreader
12	PCIE 6 L1 / SATA 2	SATA 2	mSATA
13	PCIE 6 L2 / SATA 1	SATA 1	ODD
14	PCIE 6 L3 / SATA 0	SATA 0	HDD

BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
3G@	3G function(Option with TS@)
TPM@	Trusted Platform Module (TPM)
NM14@	14" SKU ID
NM15@	15" SKU ID
UMA@	UMA SKU ID
DIS@	Optimus SKU ID
X76@	GPU VRAM Setting
M2G@	Micron 256Mx16 VRAM
M1G@	Micron 128Mx16 VRAM
S2G@	Samsung 256Mx16 VRAM
S1G@	Samsung 128Mx16 VRAM
ME@	ME Connector
TS@	Touch screen function
DEBUG@	For debug
BYPASS@	For bypass
MIRROR@	For mirror function
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
X76_S2G@ S2G@	For Samsung 2G VRAM

UC1 Haswell-ULT-CL8064701478202_SR16Q SR16Q@ SA00005VY10
UC1 Broadwell-1.8GHz 15W 2+2U 1600 DDR ES2 QGH9@ SA000810900
UC1 Broadwell-ULT-CL8065801674128_QG21 QG21@ SA000067H00
UC1 Broadwell-1.6GHz ULV 15W 2+2U 1600 DDR ES2 QGHB@ SA000811100
UC1 Broadwell-ULT-CL8065801675027_QG22 QG22@ SA000067I00
UC1 Broadwell-1.6GHz 15W 2+2U 1333 DDR ES2 QGHA@ SA000811000
UC1 Haswell-ULT-CL8064701477400_SR1ED SR1ED@ SA00005YW10
UC1 Haswell-CL8064701478404 QEAR D0 QEAR@ SA00005YZ00
UV1 JET M2 XT JET@ SA000066500
UC1 Haswell-CL8064701477600 QEAH D0 2.0G QEAH@ SA000066W00

ZZZ7 X76_S2G@ K4W4G1646D-BC1A X7603901003
ZZZ8 X76_H2G@ H5TC4G63AFR-11C X7603901001
ZZZ9 X76_M2G@ MT41J256M16HA-093G:E X7603901002
ZZZ10 X76_S1G@ K4W2G1646Q-BC1A X7603901004
ZZZ11 X76_H1G@ H5TC2G63FFR-11C X7603901005
ZZZ12 X76_M1G@ MT41J128M16JT-093G:K X7603901006

UL1 VPRO@ WGI218LM-QQJY-B1_QFN48_6X6 SA00005TP10

UC1 BDW-3205U-1.5G QGZ6@ SA000072M00
UC1 BDW-3755U-1.7G QGZ5@ SA000072J00
UC1 BDW-i7-2.2G QH15@ SA000072L00
UC1 BDW-i3-2G QH18@ SA000072H00
UC1 BDW-i3-2G QGZ3@ SA000072P00
UC1 BDW-i5-2G QH17@ SA000072K00
UC1 BDW-3805U-1.9G QGZ4@ SA000072N00
UC1 HSW I3 4030U SR1EN@ SA000810100
UC1 HSW I5 4210U SR1EF@ SA000066Y20
UC1 HSW I3 4005U SR1EK@ SA00005YZ20
ZZZ1 NM-A221 PCB@ DAZ0TS00100

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Title: NOTE LIST

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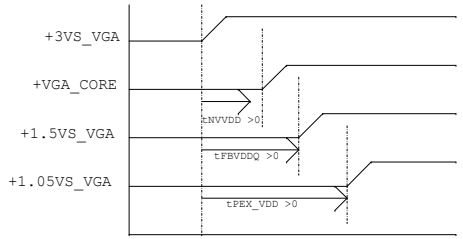
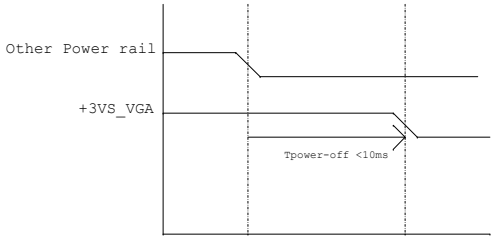
Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	_	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	_	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	_	HPD_IRQ



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GT (28nm)	0x0FDB

	setting	I2C Slave addrees ID
SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
	1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU		N13P-GT		
FB Memory (GDDR5)		ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K		

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Title: VGA NOTE

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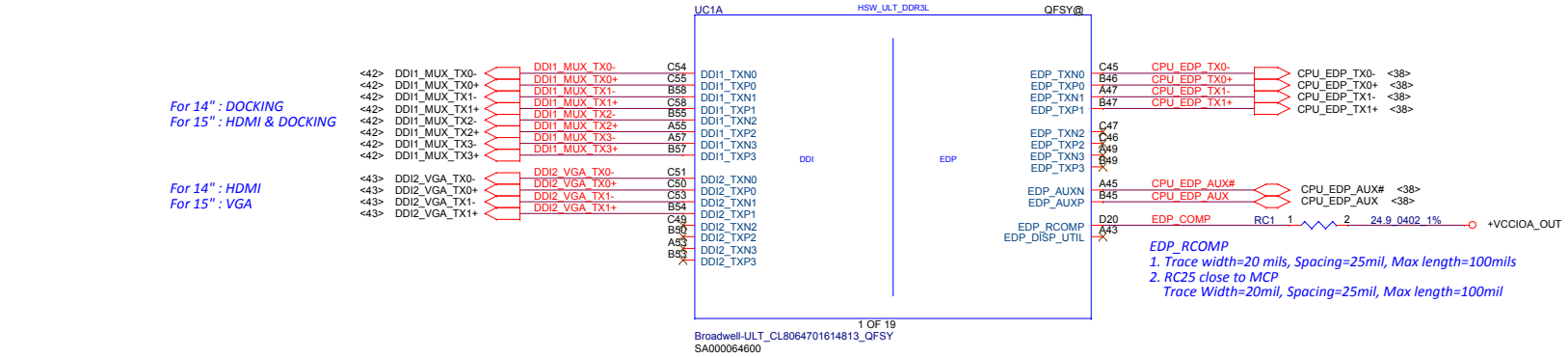

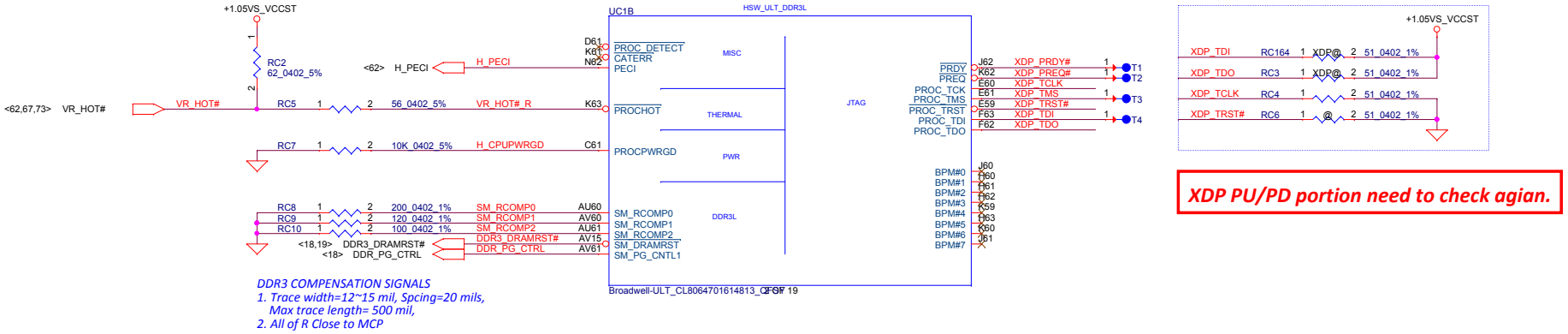

XDP PU/PD portion need to check agian.

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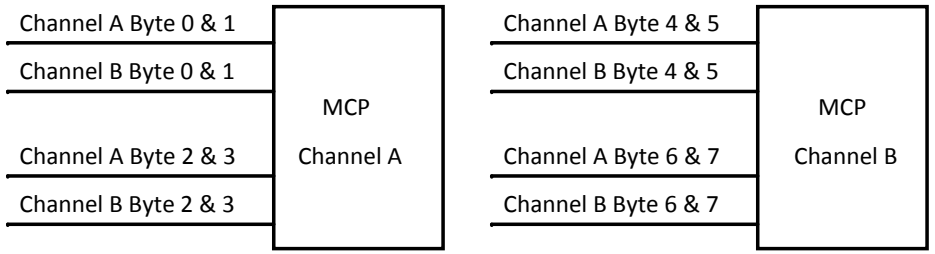
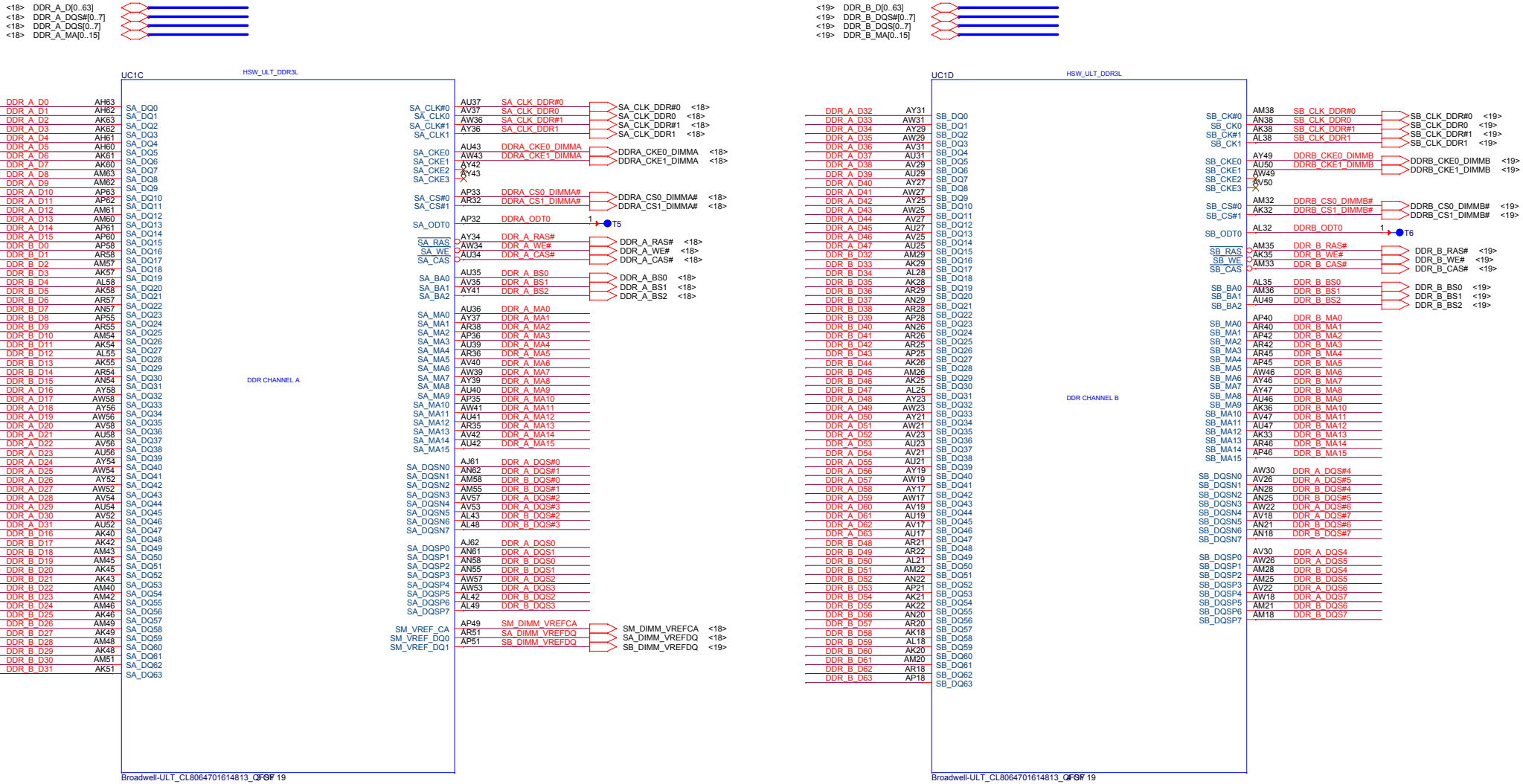
Interleaved (Butterfly Topology)
Broadwell Platform System Memory Interface
Document Number: 528378
BDW U DDR3L/DDR3L-RS SO-DIMM Interleaved Recommendations





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Title: **BDW_DDR3L INT**

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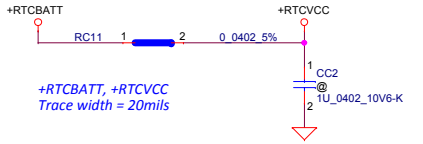
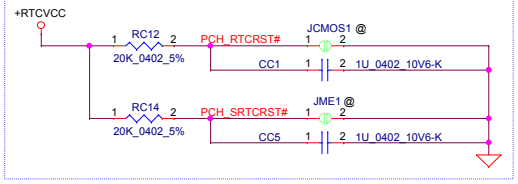
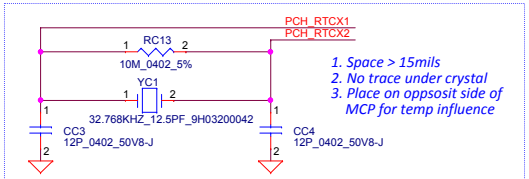
RTC External Circuit

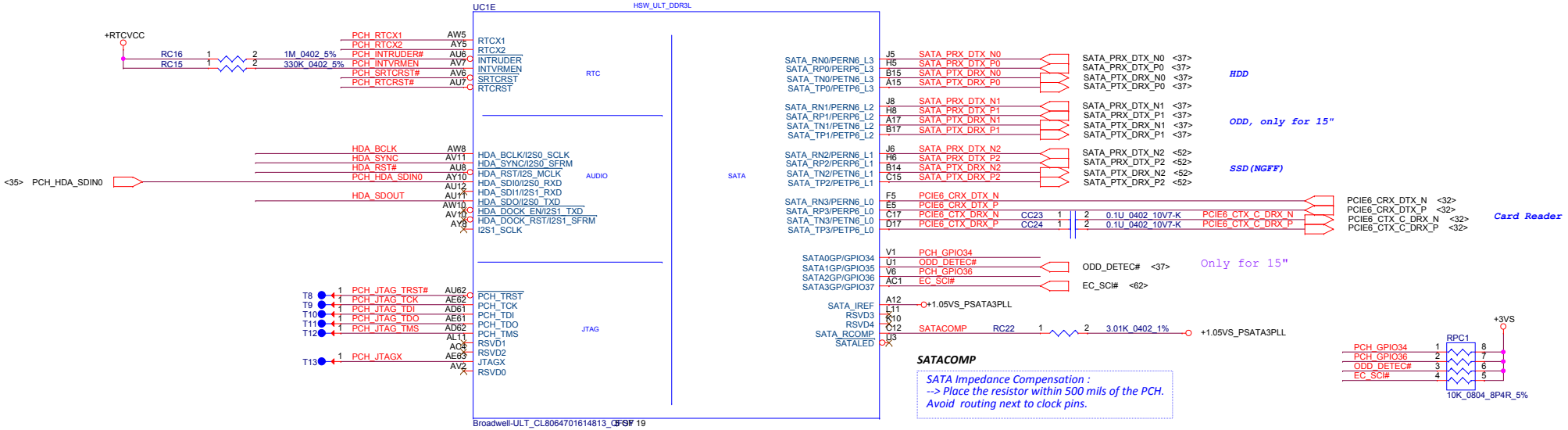


JCMOS, JME Setting, Need Under DDR Door



RTC Crystal





SATACOMP

SATA Impedance Compensation :
--> Place the resistor within 500 mils of the PCH.
Avoid routing next to clock pins.

INTVRMEN

1. INTVRMEN, should always be pull high
   - ★ H Integrated VRM enable (Default)
   - L Integrated VRM disable
2. Internal Voltage Regulator Enable:
   This signal enables the internal 1.05 V regulators.

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Title: **RTC/HDA/SATA/PCIe/JTAG**

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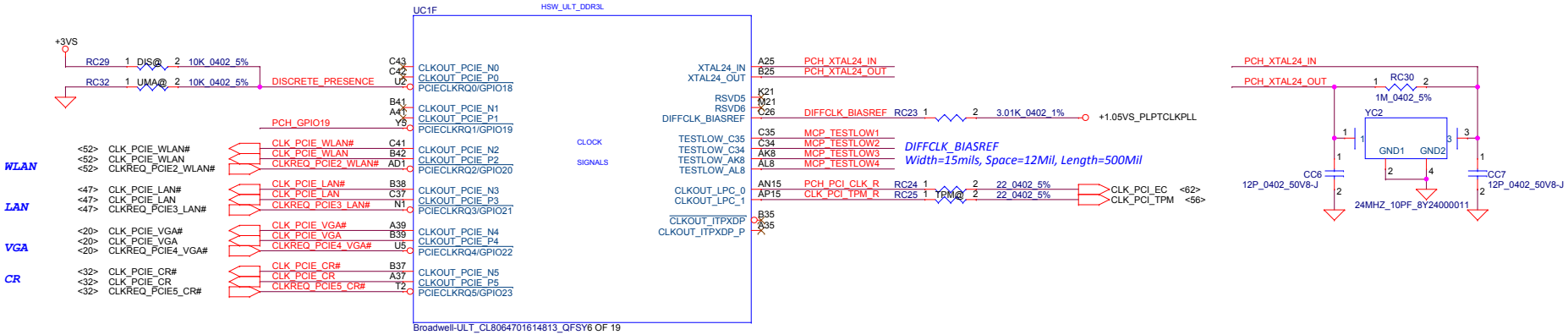

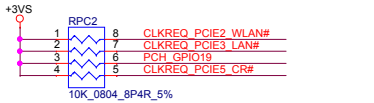

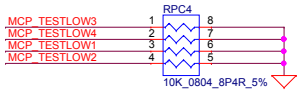

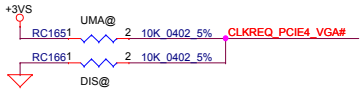

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Title: BDW_CLOCK/PM

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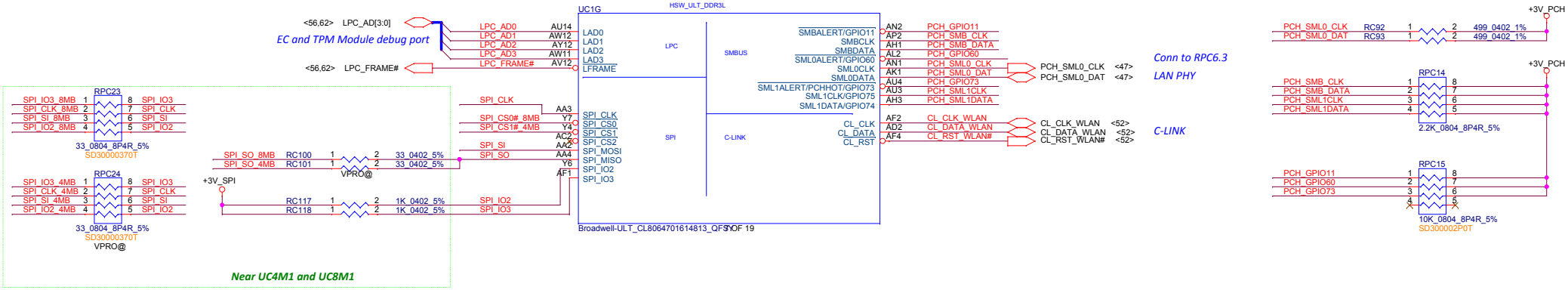
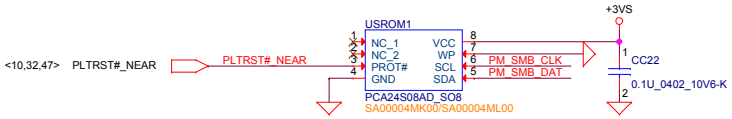
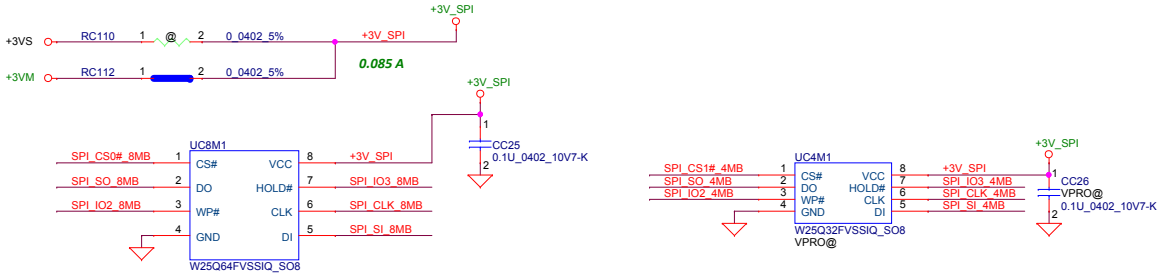


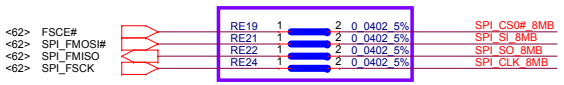
Security ROM



M3 Support + Intel LAN PHY / Wireless LAN Solution



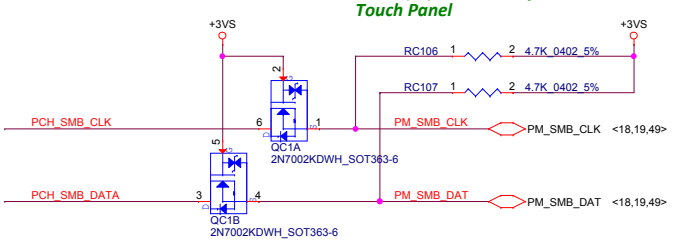
Mirror Code



Close to SPI ROM (UC8M1).

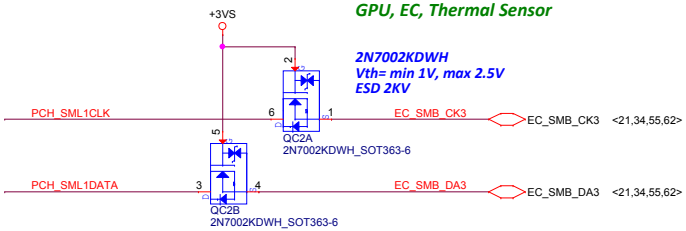
SM Bus

DIMM1, DIMM2,
WLAN(@), CP, Security ROM
Touch Panel



GPU, EC, Thermal Sensor

2N7002KDWH
Vth= min 1V, max 2.5V
ESD 2KV



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Title	BDW_LPC/SPI/SM BUS		
Size	Document Number		Rev
Custom	AITE1 NM-A221		1.0
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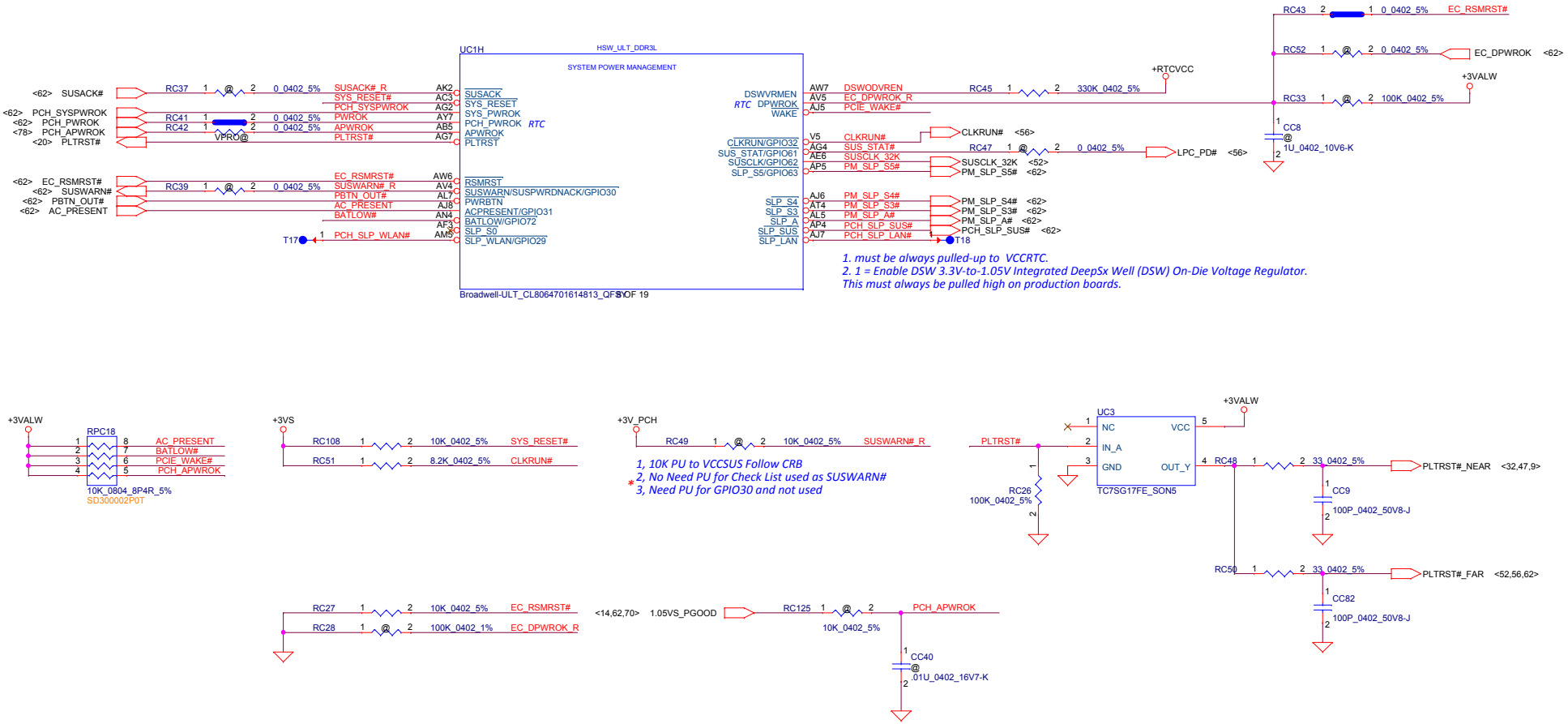

SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.

For platforms not supporting IntelR AMT it can be connected to PWROK.

This signal can be tied to RSMRST# for platforms that do not support the Deep Sx state.
RSMRST# <--> DPWROK

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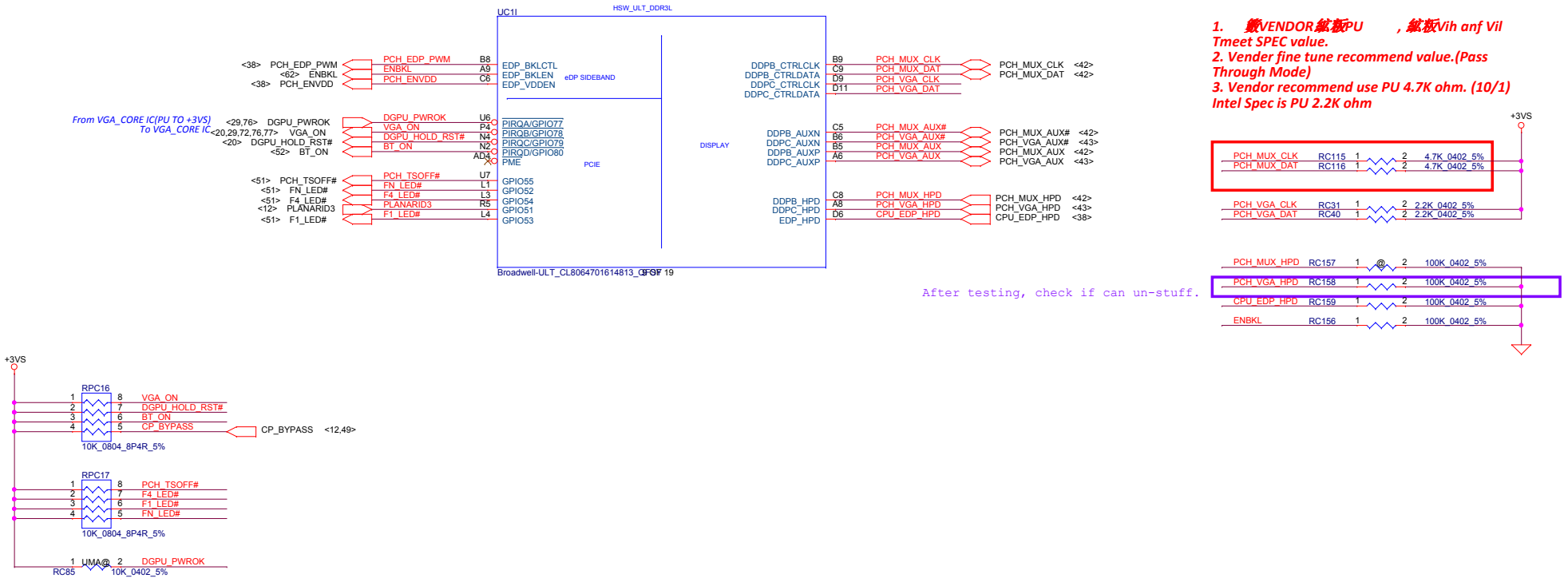
Title		
BDW_SYS PM		
Size: Custom	Document Number: AITE1 NM-A221	Rev: 1.0
Date: Thursday, November 06, 2014	Sheet 10 of 81	



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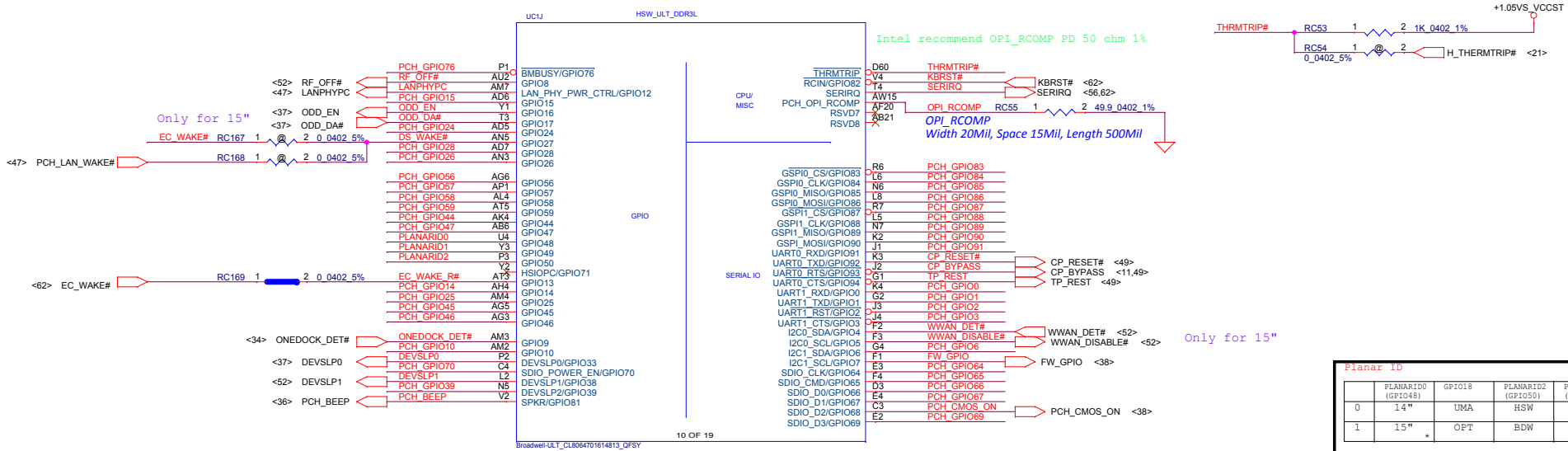
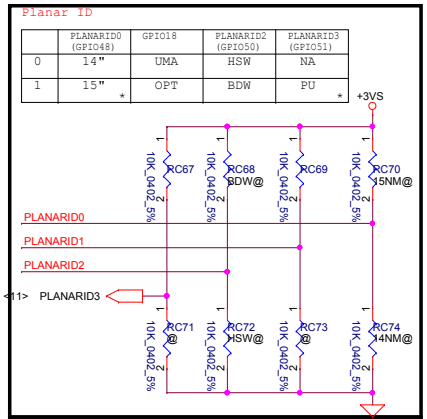
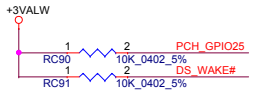
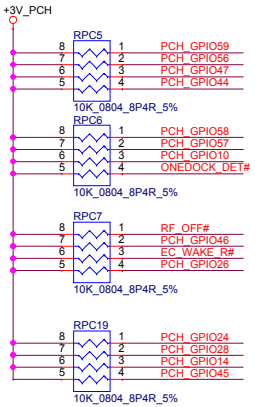
Title		
BDW_eDP SBAND/DDPx		
Size: Custom	Document Number: AITE1 NM-A221	Rev: 1.0
Date: Thursday, November 06, 2014	Sheet 11 of 81	

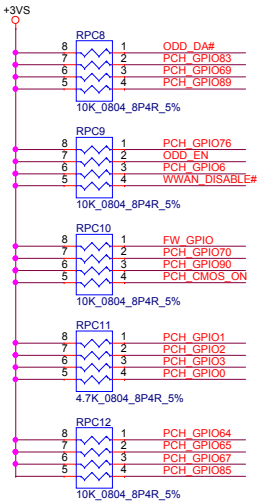


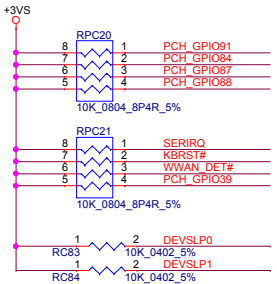
	SATA Port
DEVSLP0	SATA Port 0
DEVSLP1	SATA Port 1

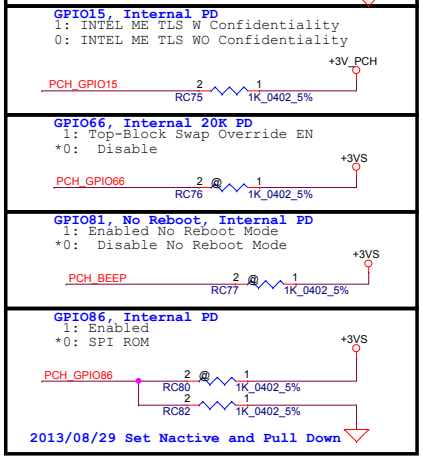












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Title: **BDW_GPIO/SIO**

Size	Document Number	Rev
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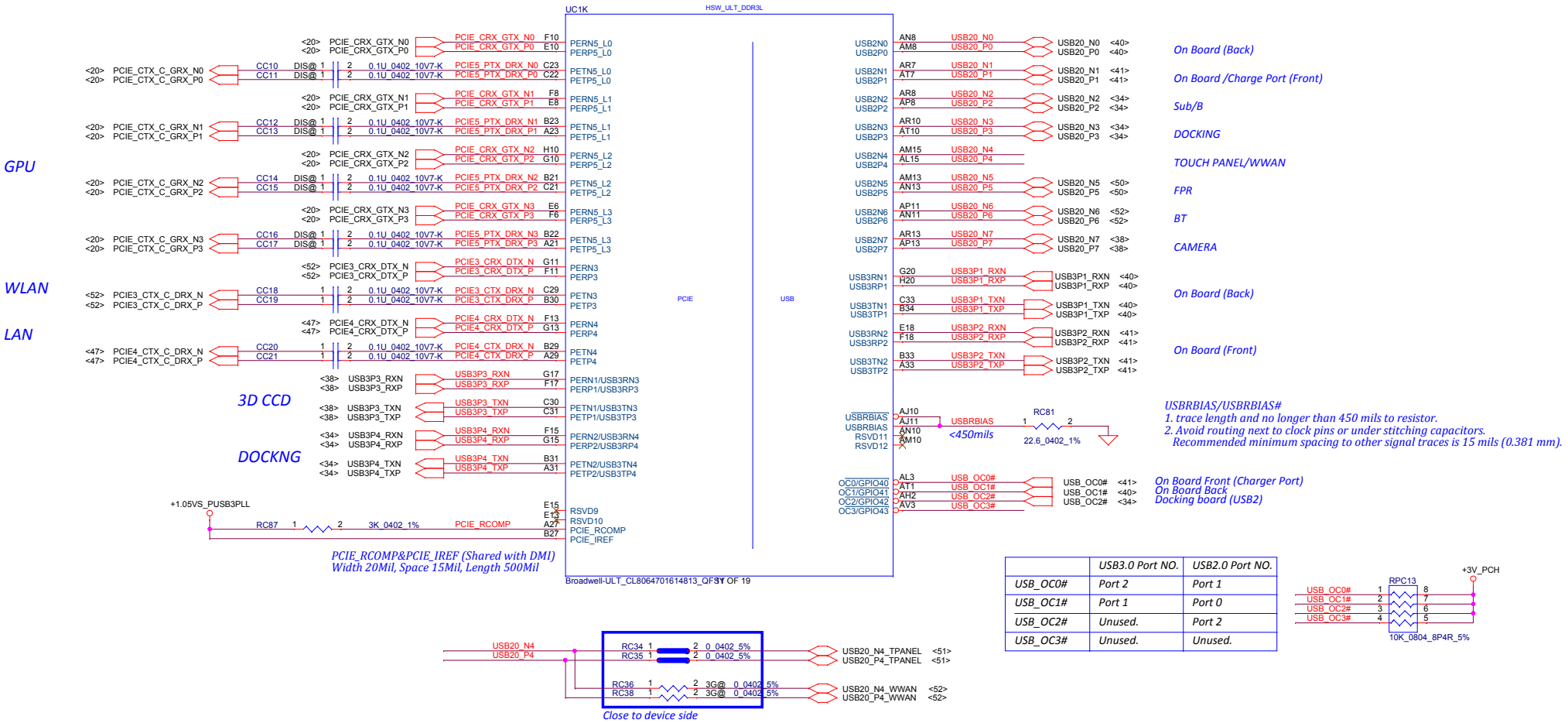

	USB3.0 Port NO.	USB2.0 Port NO.
USB_OC0#	Port 2	Port 1
USB_OC1#	Port 1	Port 0
USB_OC2#	Unused.	Port 2
USB_OC3#	Unused.	Unused.

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Title: BDW_PCIE/USB BUS

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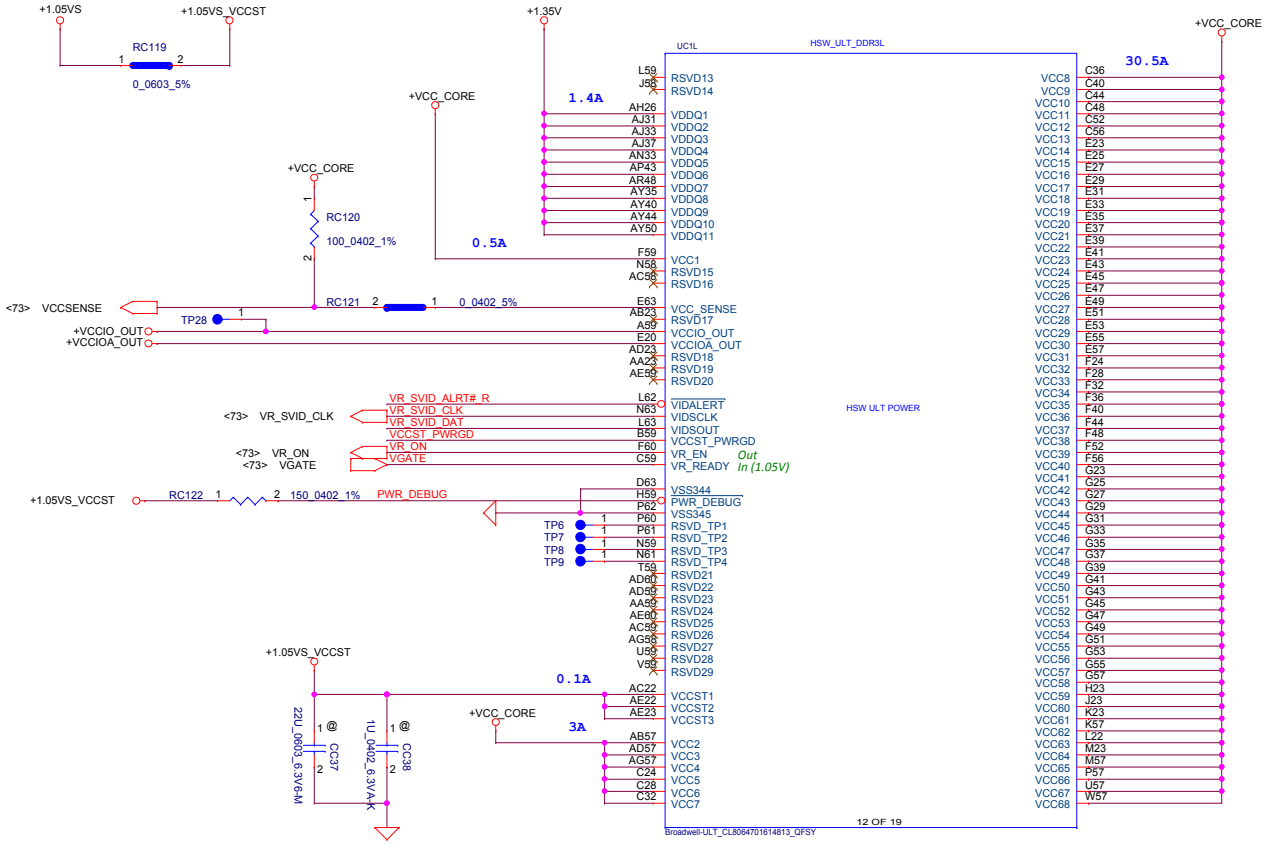
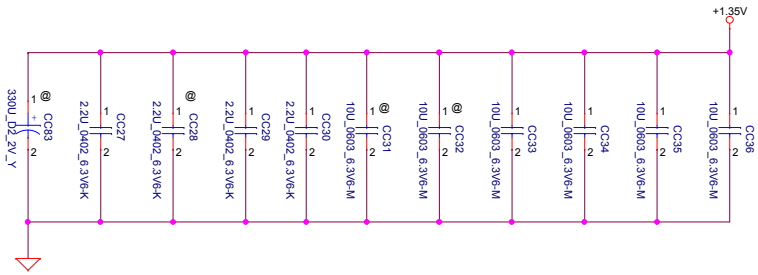
Haswell MCP (Power)





HW 4PCS 2.2UF CAP Mounted
HW 6PCS 10UF CAP Mounted
PWR 2PCS 470U Near VR Output

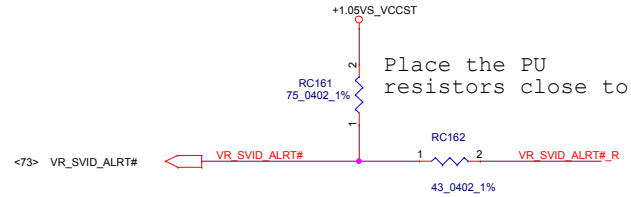
VCC_SENSE
Length Match: No More Than 25Mil
Space: More Than 25Mil
GND Reference

SVID

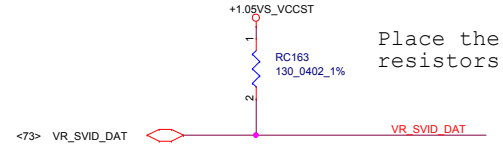
1, Stripline Line, No More Than 6000Mil
2, Alert# Route Between CLK and Data
3, CLK Length<Data Length<CLK Length + 2000Mil
4, Space at least 18Mil

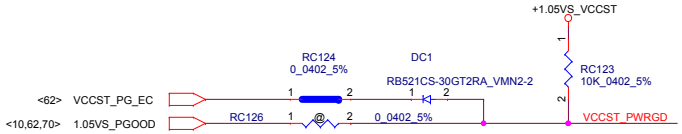
+VCC_CORE[1..68]	32A
+1.05VS_VCCST[1..3]	0.1A
VDDQ[1..11]	1.4A

SVID ALERT



SVID DATA





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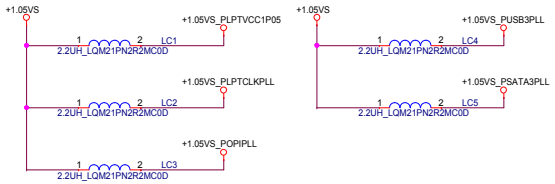
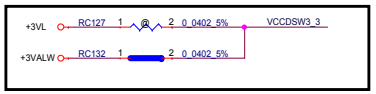
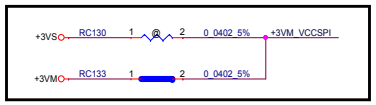
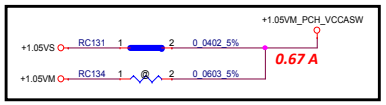
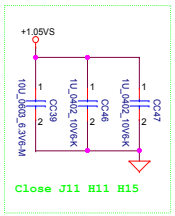
Haswell MCP (Power2)

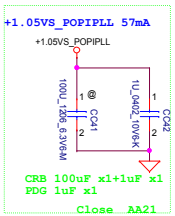


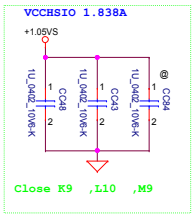


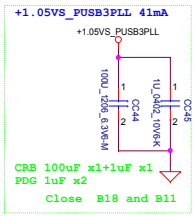


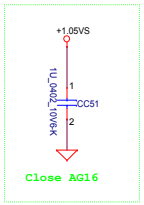


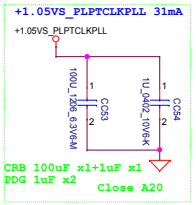


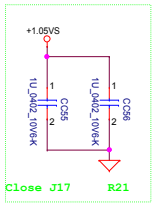


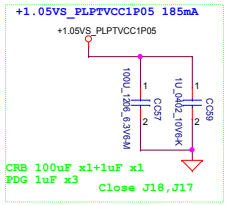


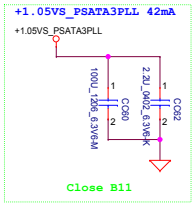


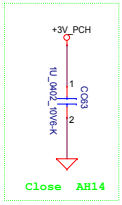


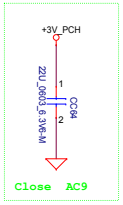


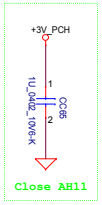


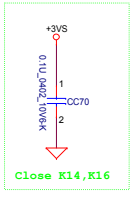


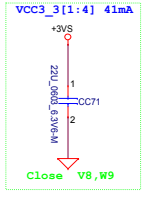


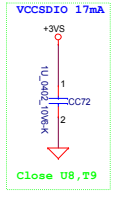


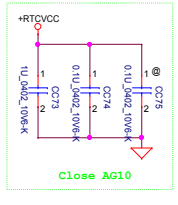


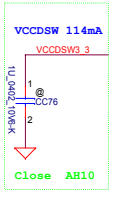


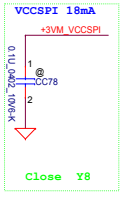


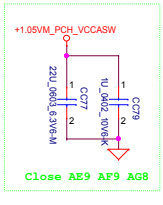


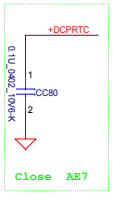


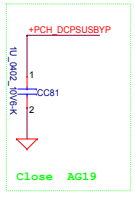


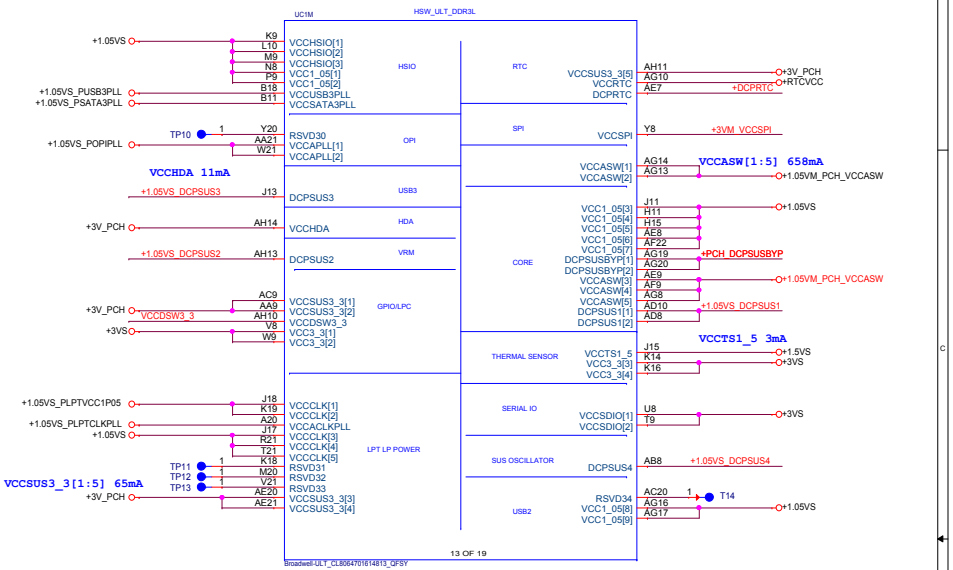












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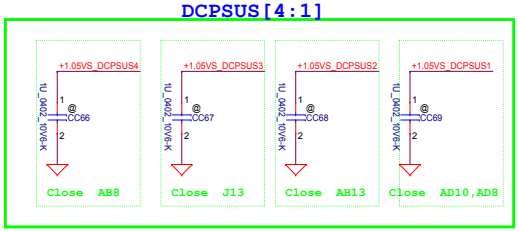

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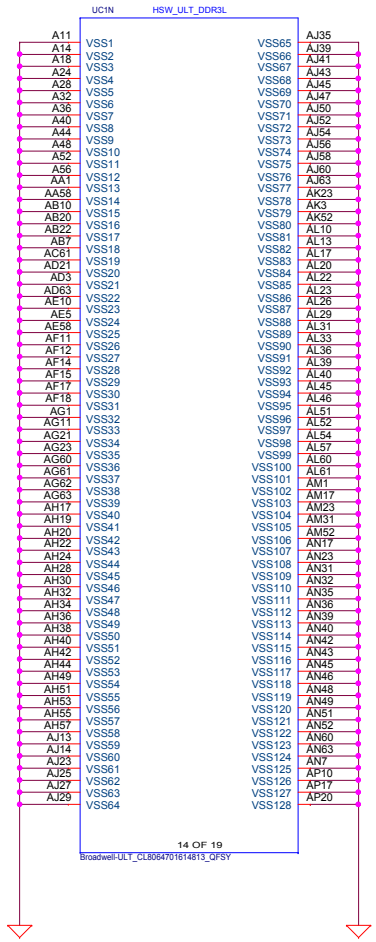
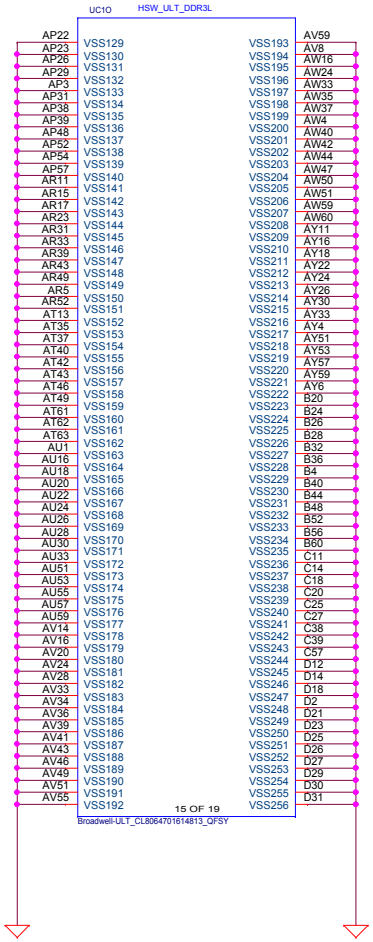
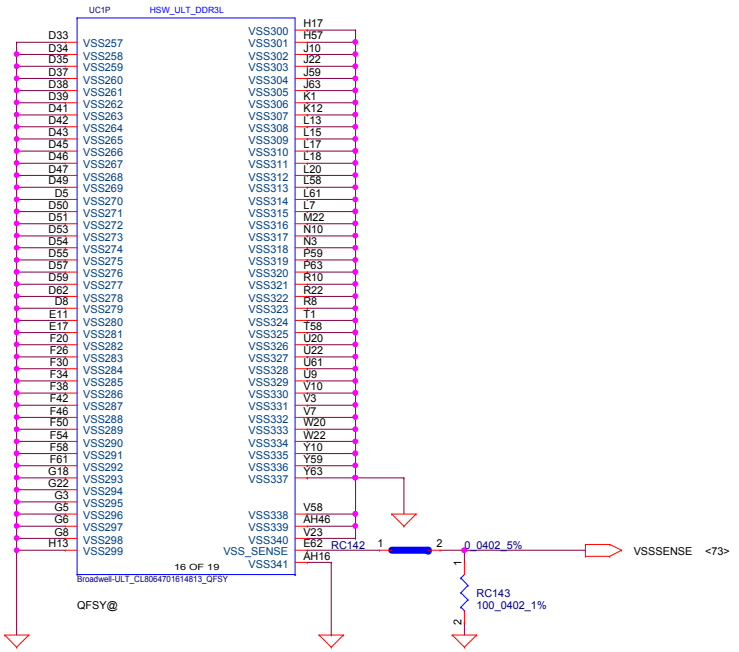
Haswell MCP (VSS)







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GND Reference

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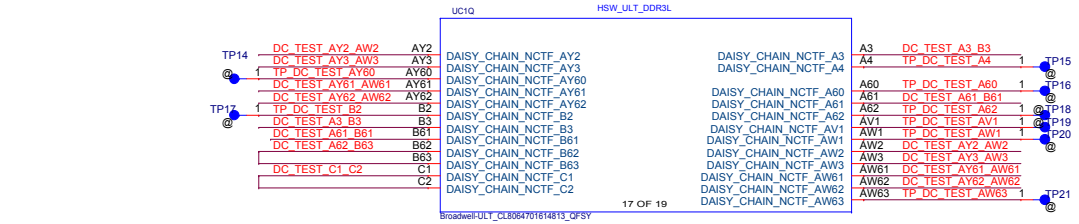
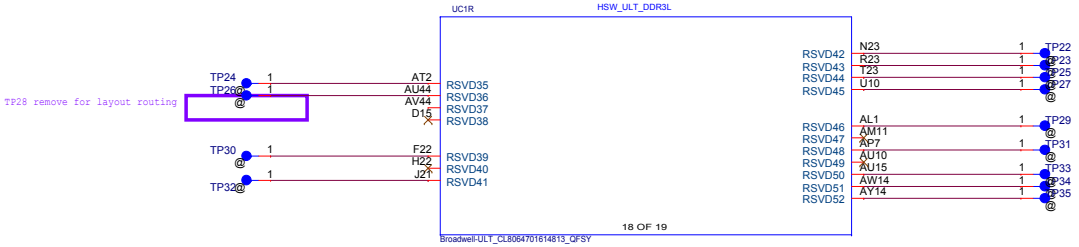
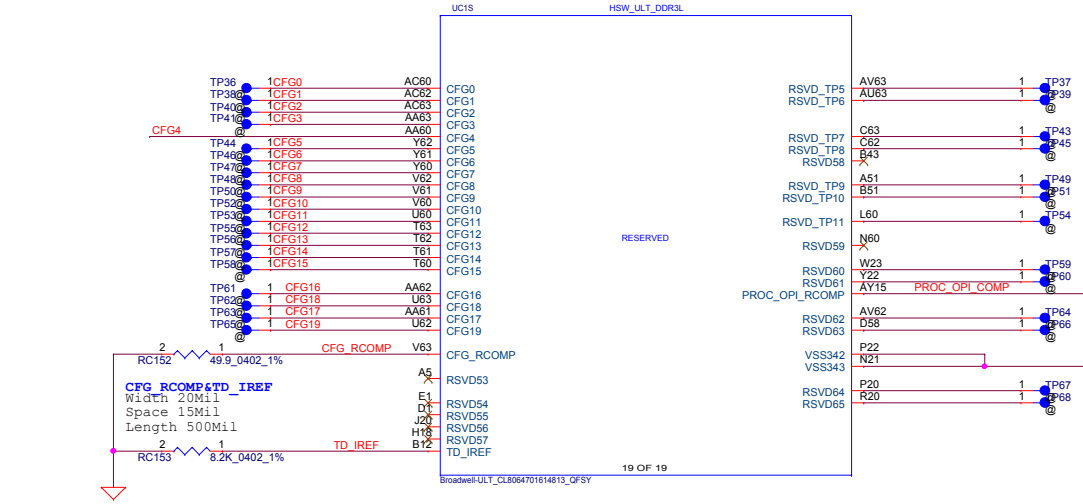
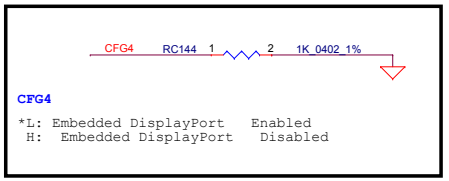
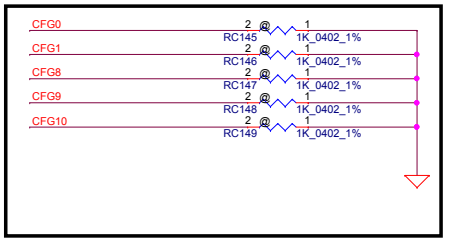
Haswell MCP (OTHER)

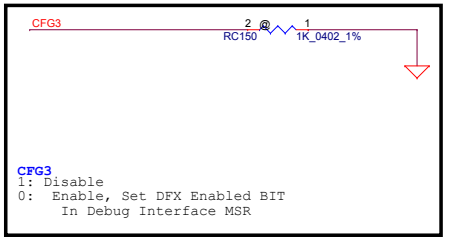












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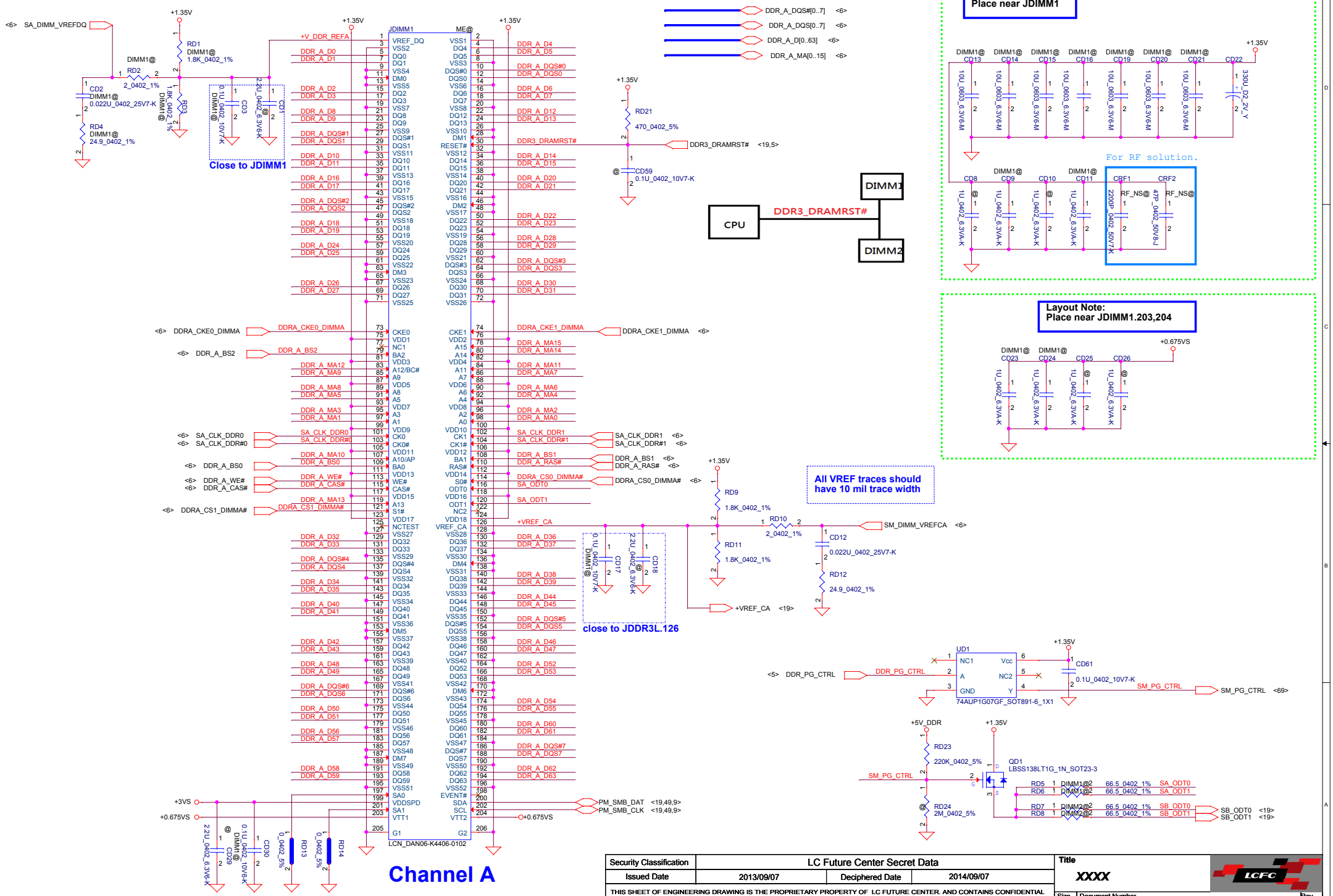

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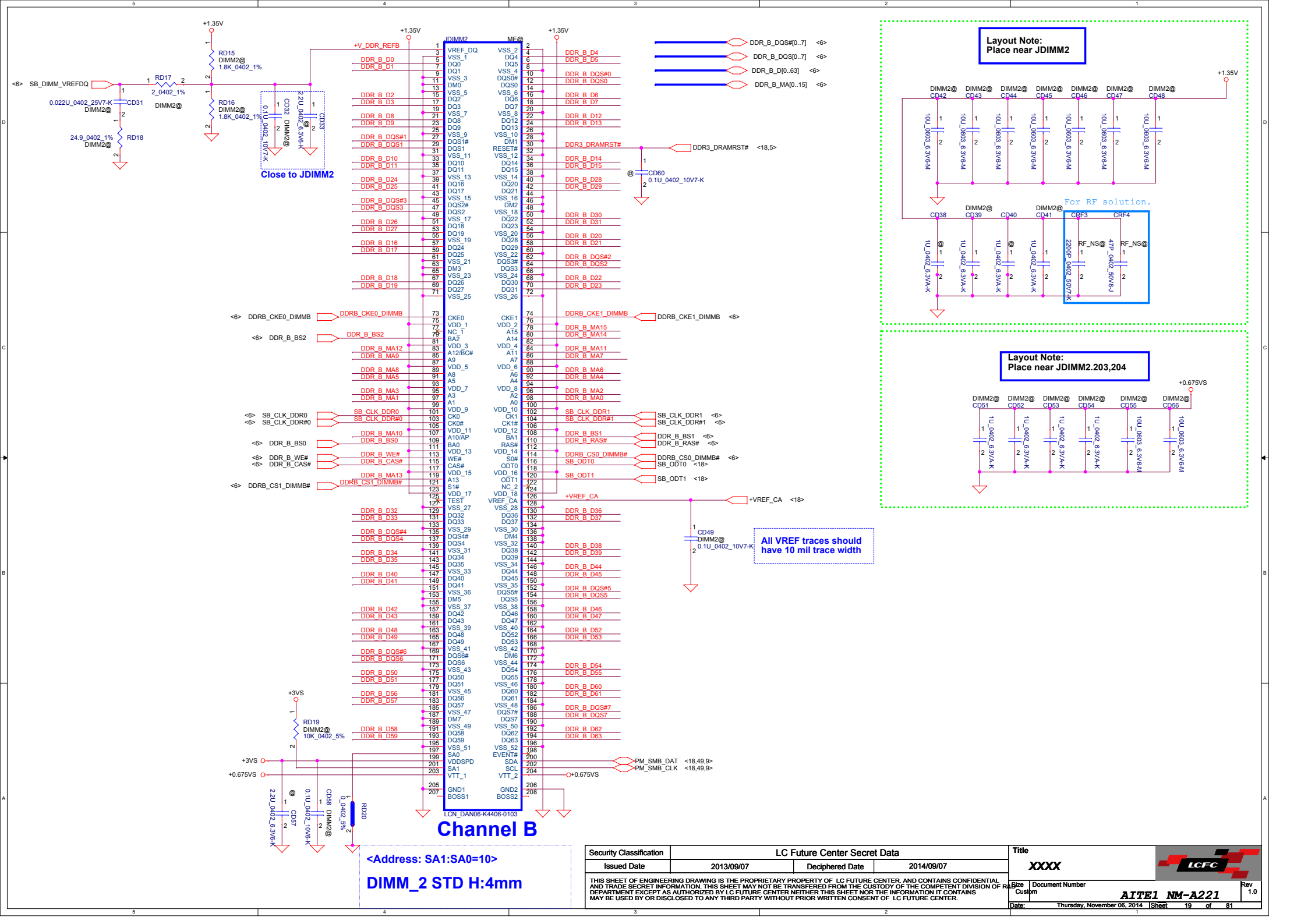

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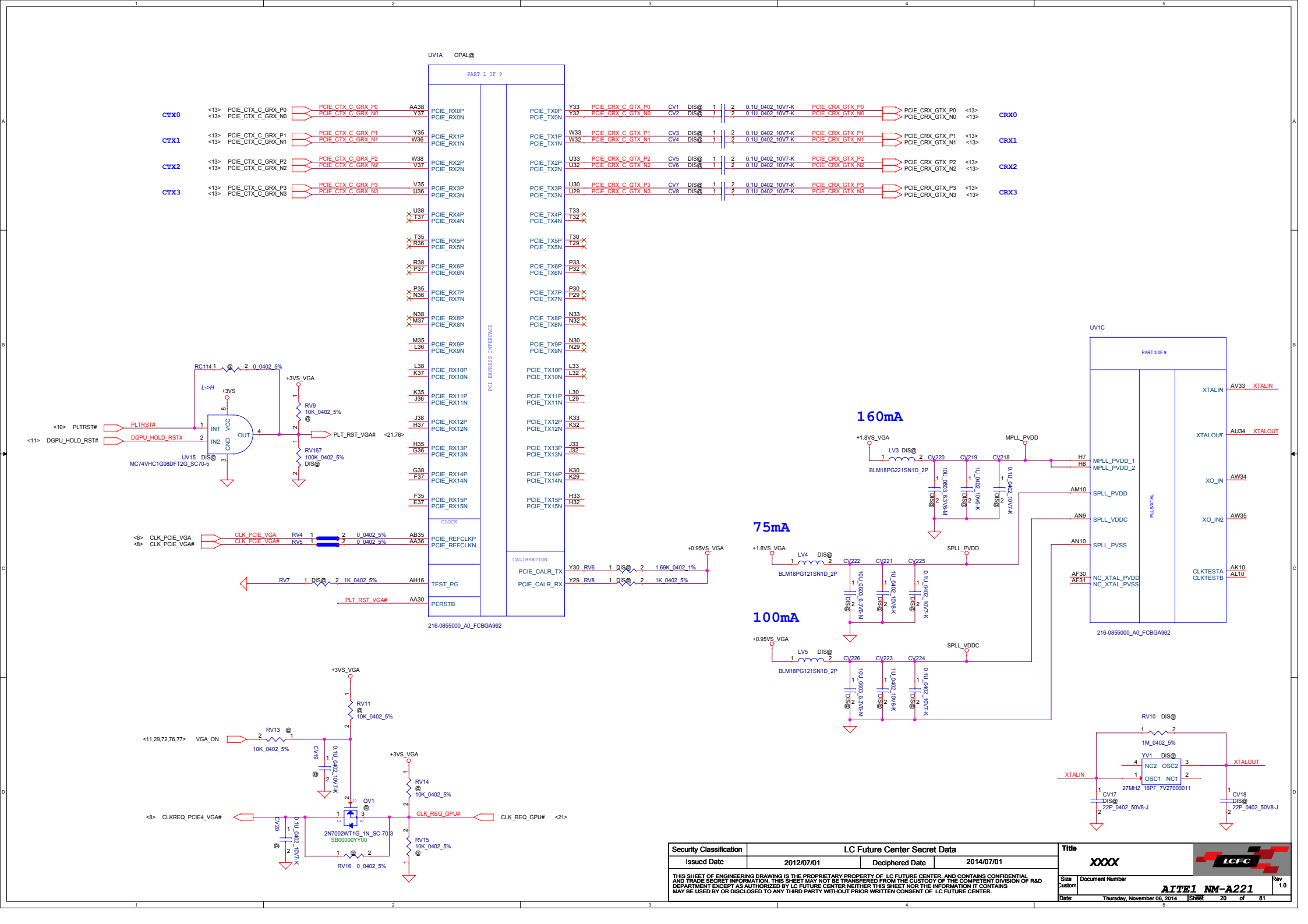

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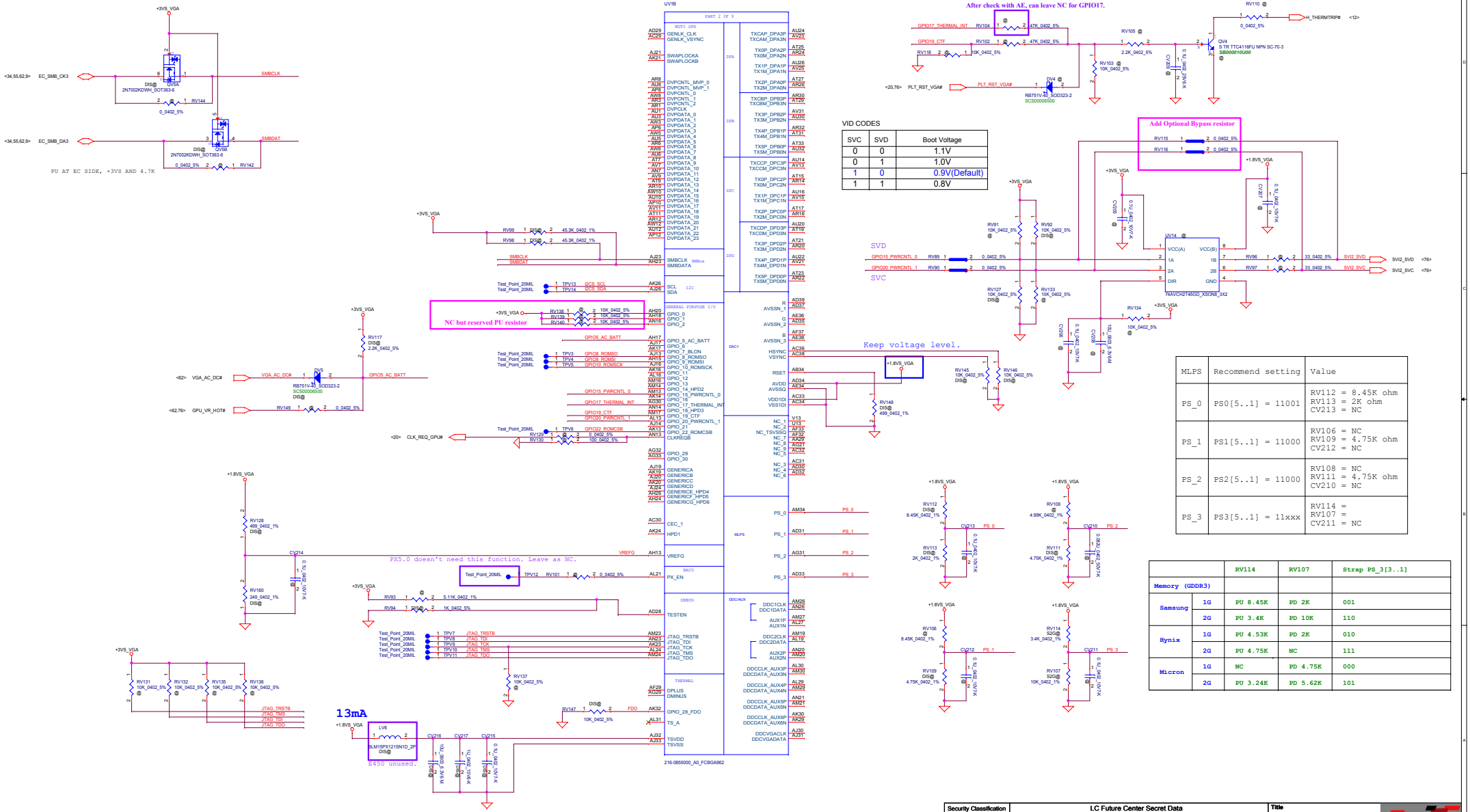
After check with AE, can leave NC for GPIO17.
VID CODES
SVC SVD Boot Voltage
0 0 1.1V
0 1 1.0V
1 0 0.9V(Default)
1 1 0.8V
Add Optional Bypass resistor
SVD
SVC
Keep voltage level.
NC but reserved PU resistor
PX5.0 doesn't need this function. Leave as NC.
13mA
B450 unused.
MLPS Recommend setting Value
PS_0 PS0[5..1] = 11001 RV112 = 8.45K ohm RV113 = 2K ohm CV213 = NC
PS_1 PS1[5..1] = 11000 RV106 = NC RV109 = 4.75K ohm CV212 = NC
PS_2 PS2[5..1] = 11000 RV108 = NC RV111 = 4.75K ohm CV210 = NC
PS_3 PS3[5..1] = 11xxx RV114 = RV107 = CV211 = NC
Memory (GDDR3) RV114 RV107 Strap PS_3[3..1]
Samsung 1G PU 8.45K PD 2K 001
2G PU 3.4K PD 10K 110
Hynix 1G PU 4.53K PD 2K 010
2G PU 4.75K NC 111
Micron 1G NC PD 4.75K 000
2G PU 3.24K PD 5.62K 101
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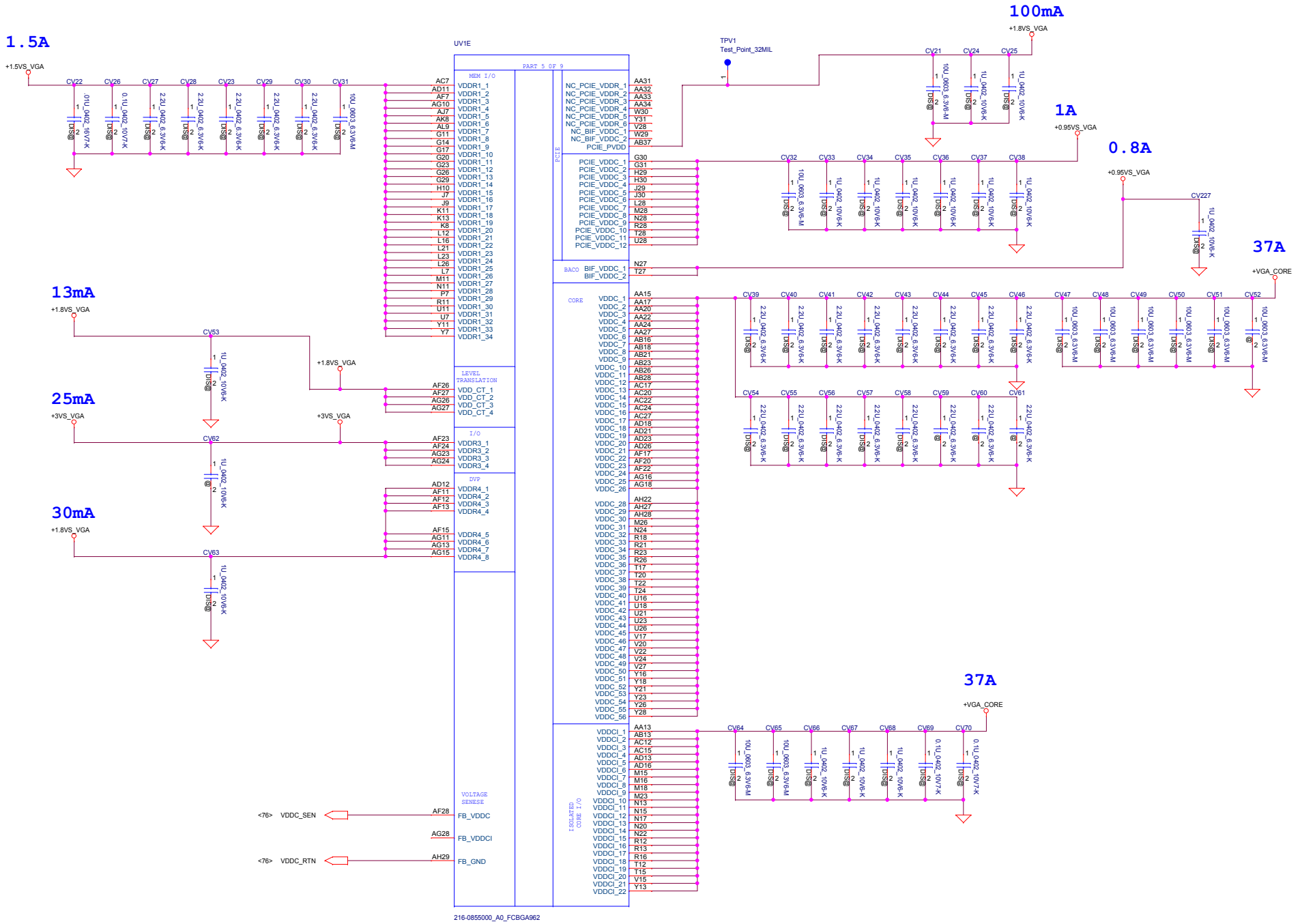

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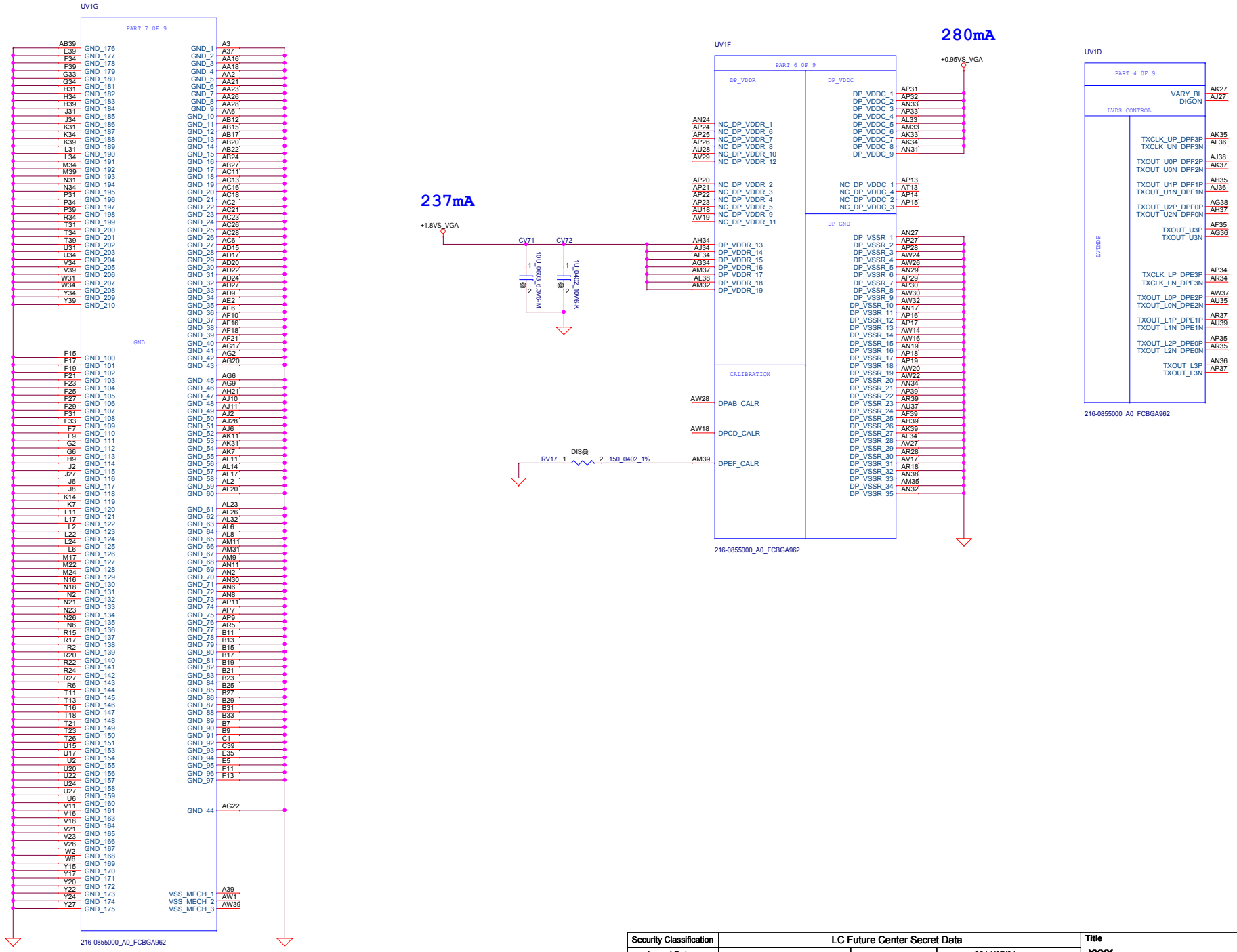

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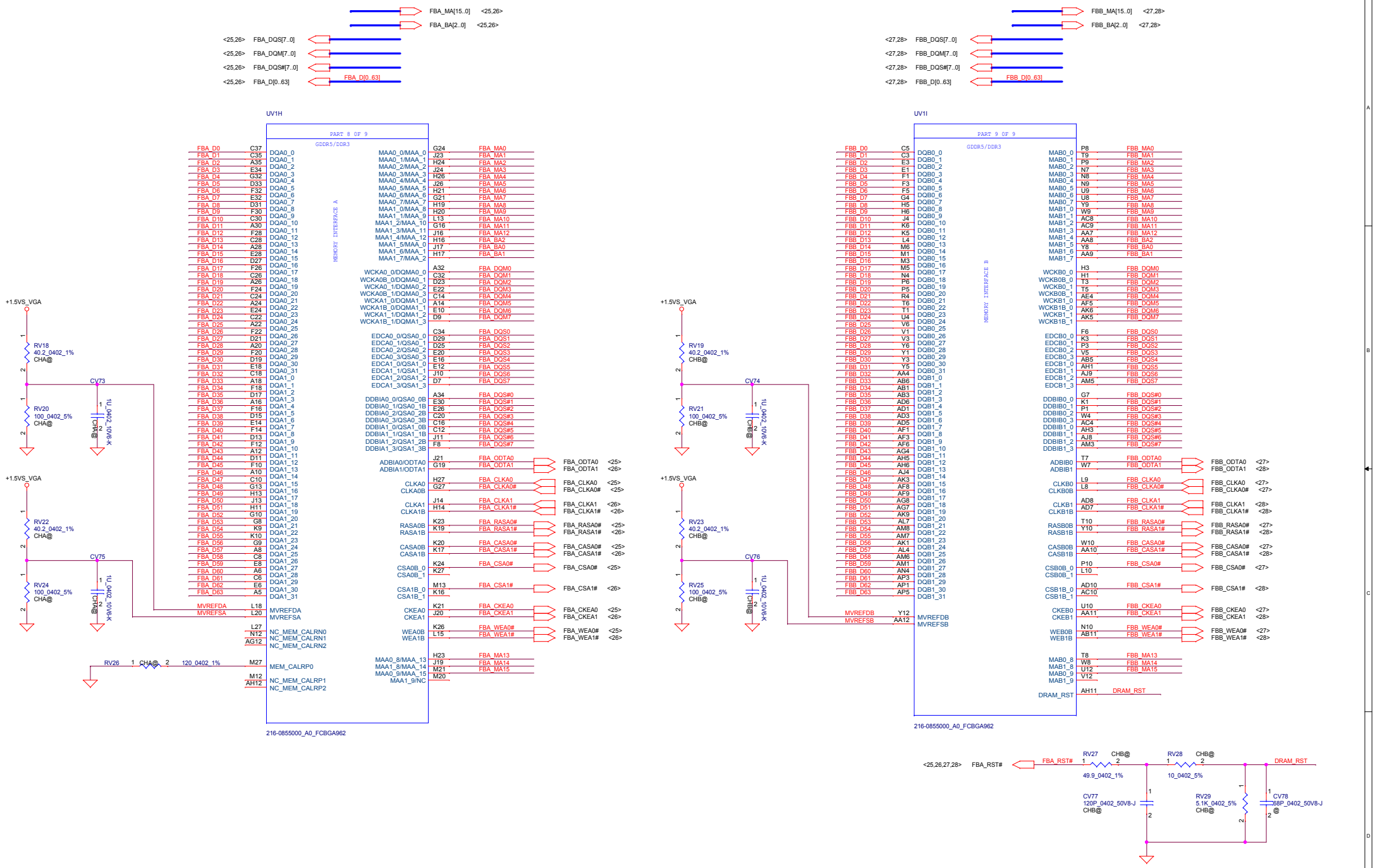

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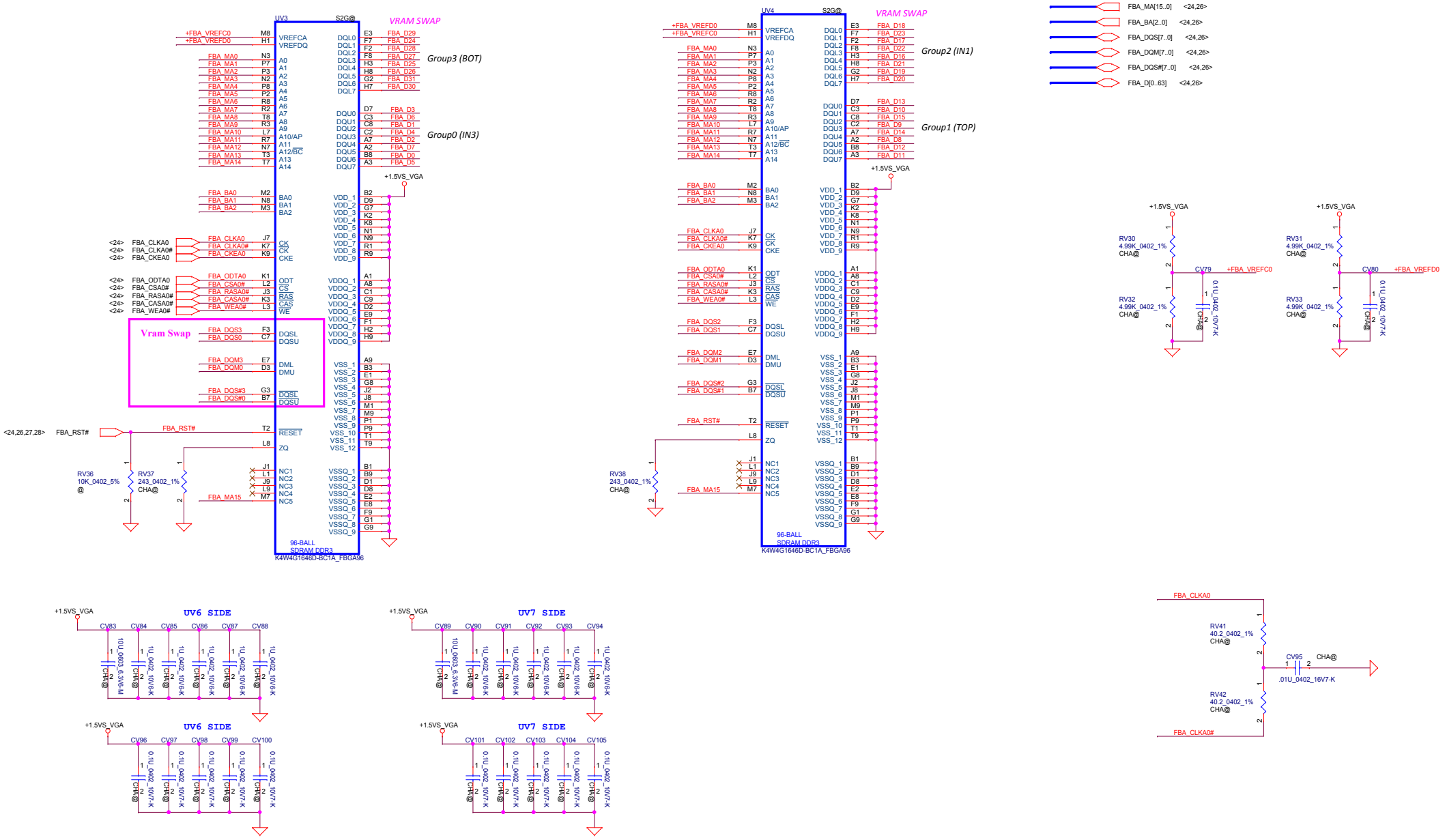
Memory Partition A - Lower 32 bits

Change all VRAM footprint to MT41K256M16HA107_FBGA_96P-A39P



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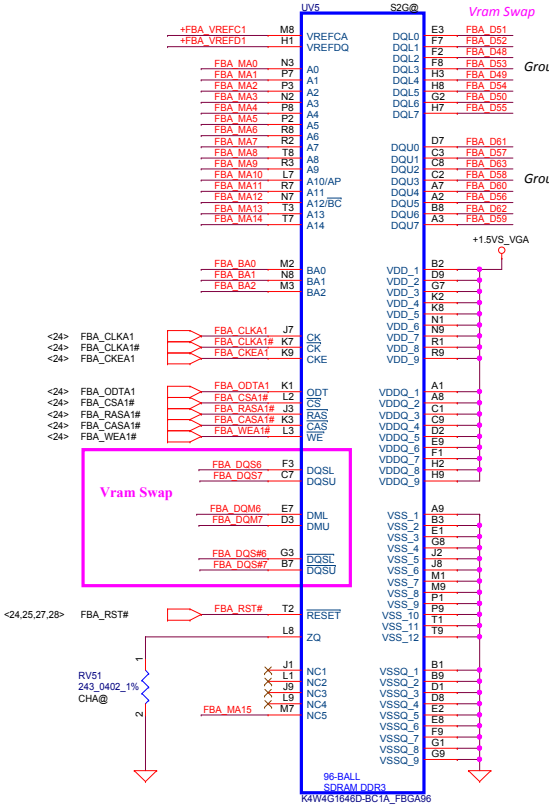
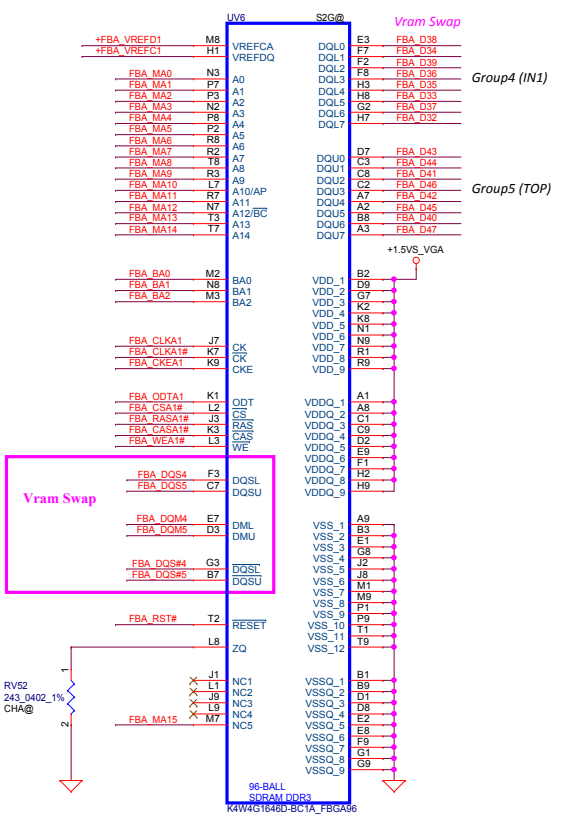
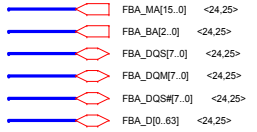
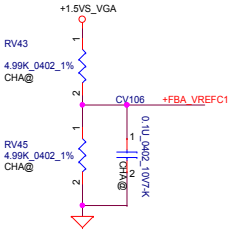
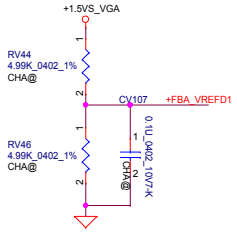
Memory Partition A - Upper 32 bits

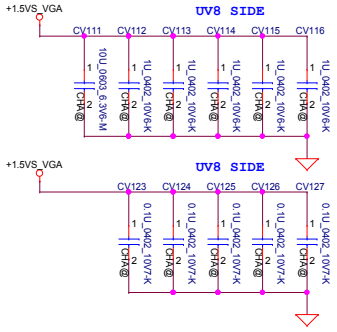


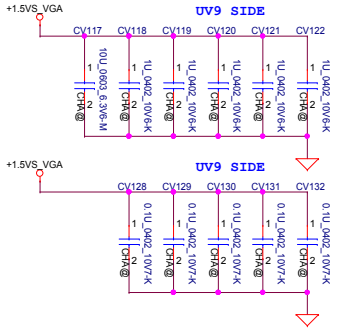


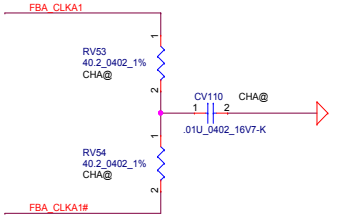












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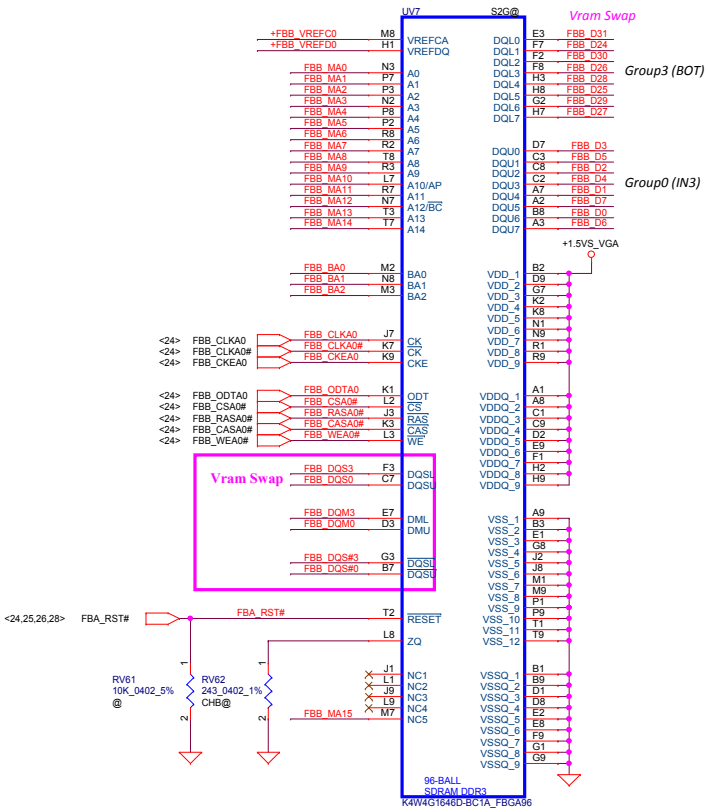
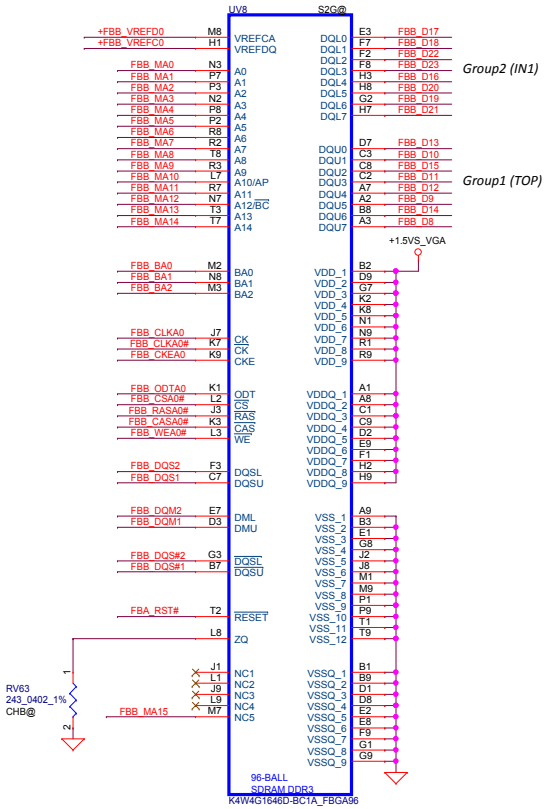
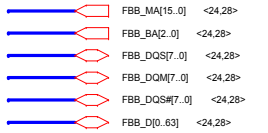
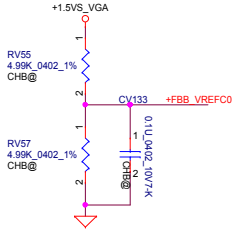
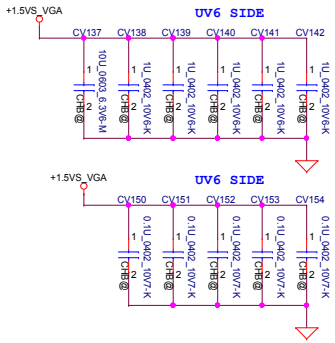
Memory Partition A - Lower 32 bits

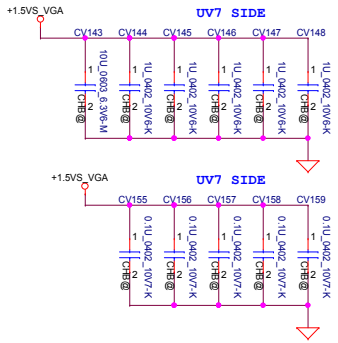


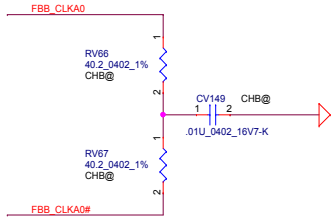












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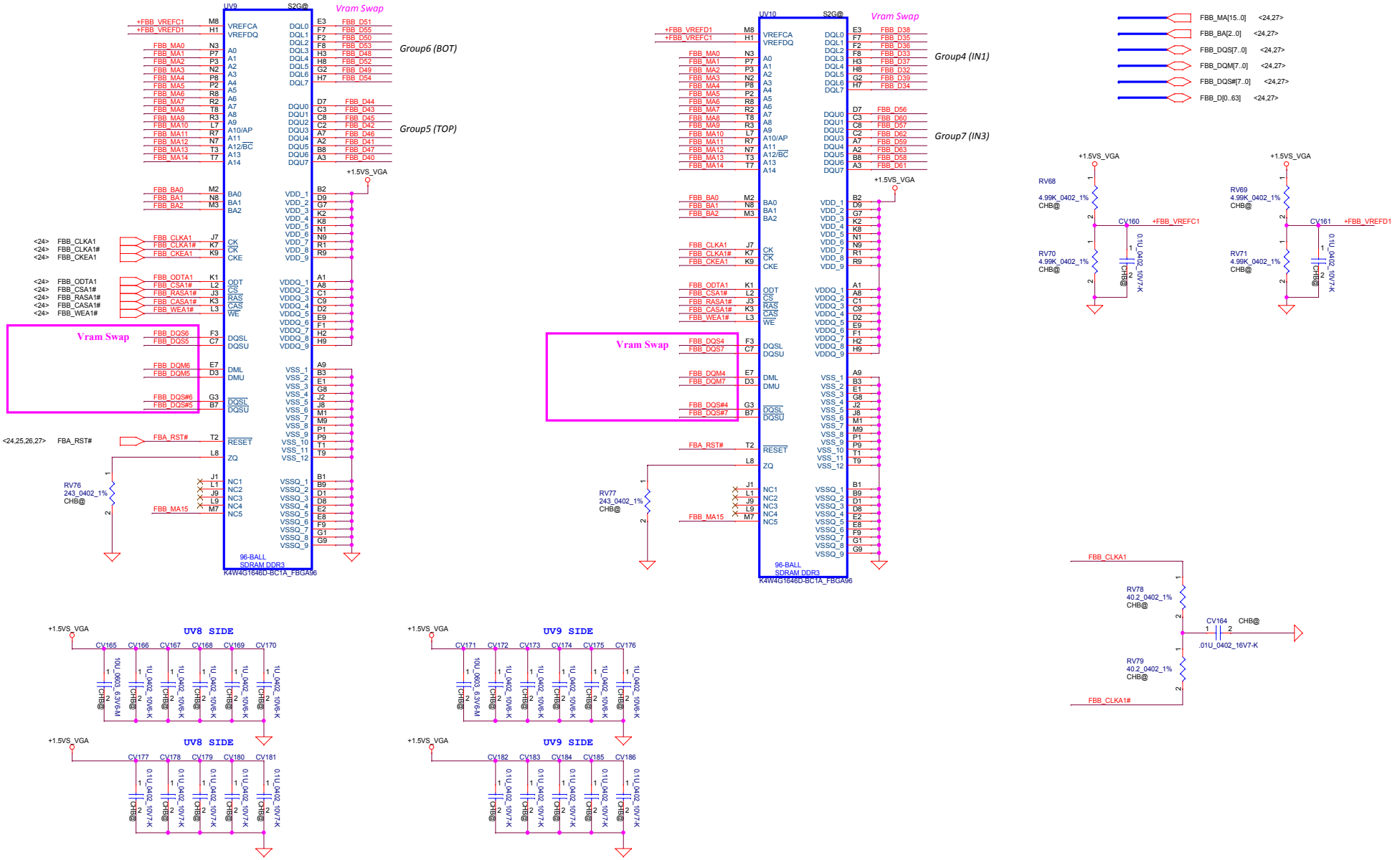
Memory Partition A - Upper 32 bits



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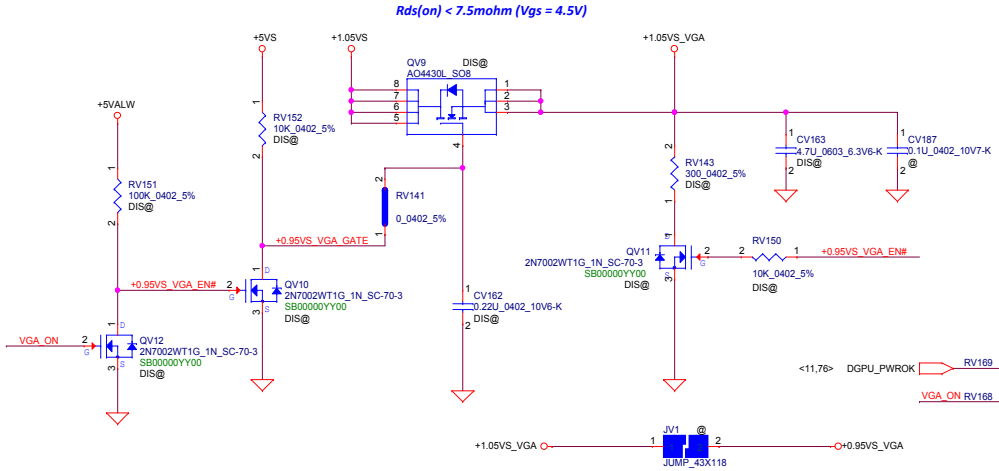
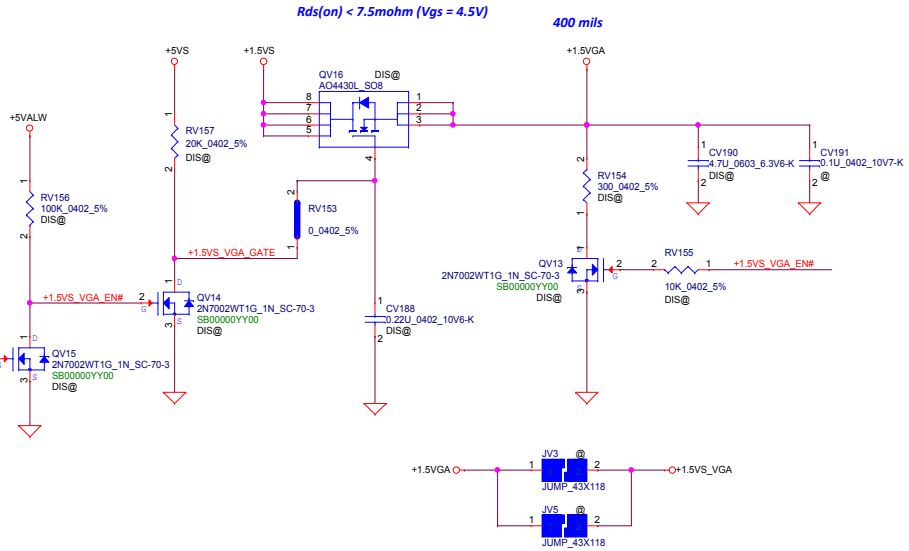
+1.05VS to +0.95VS_VGA



+1.5VS to +1.5VS_VGA



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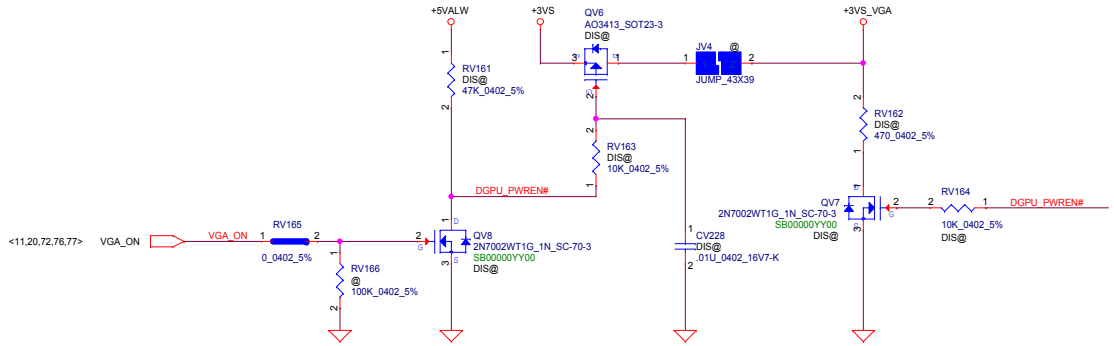

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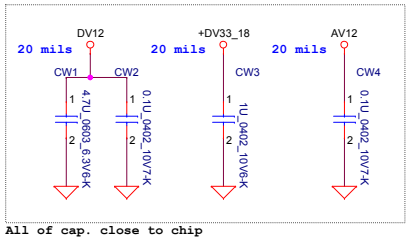

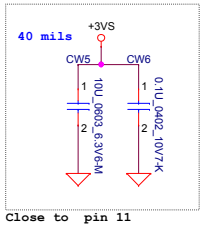

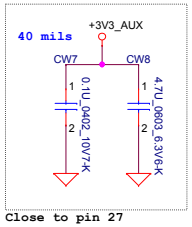

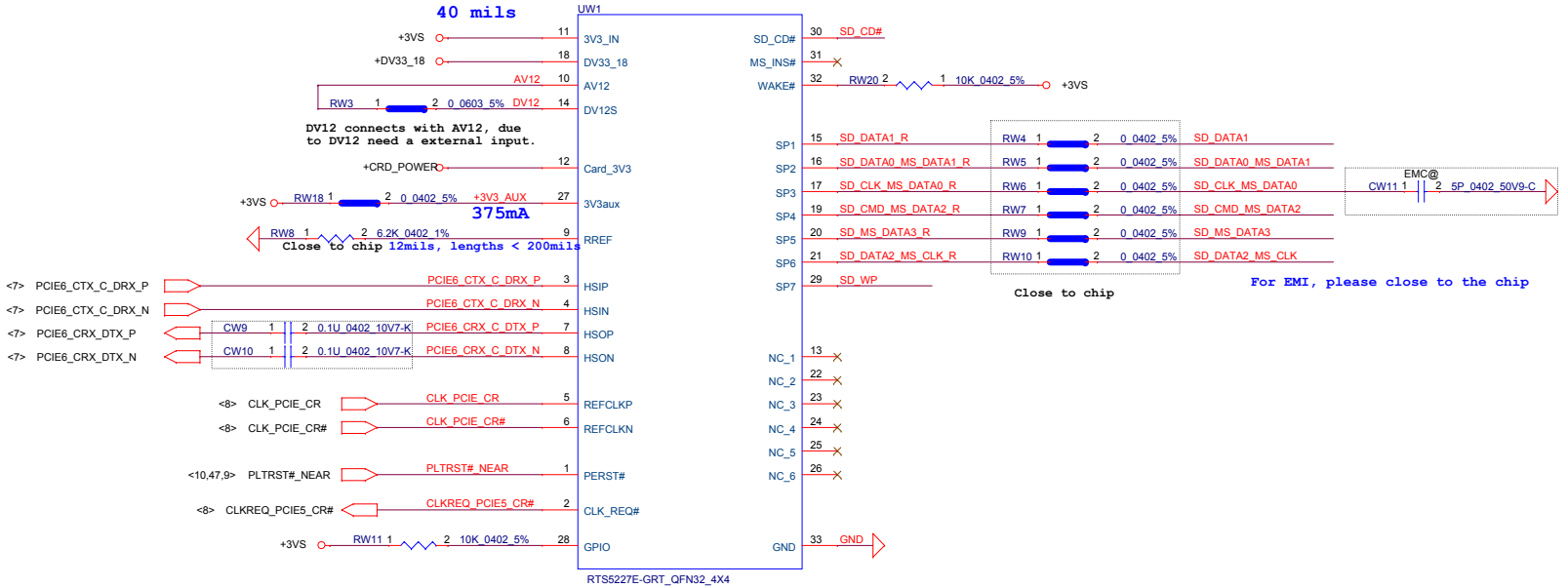

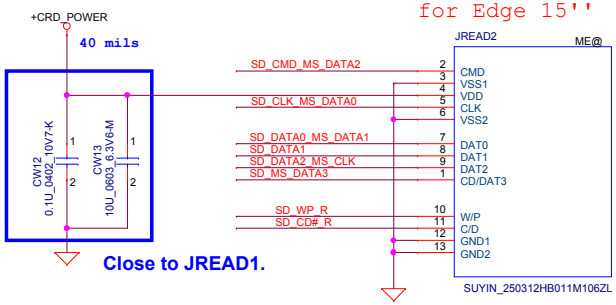

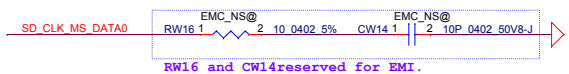

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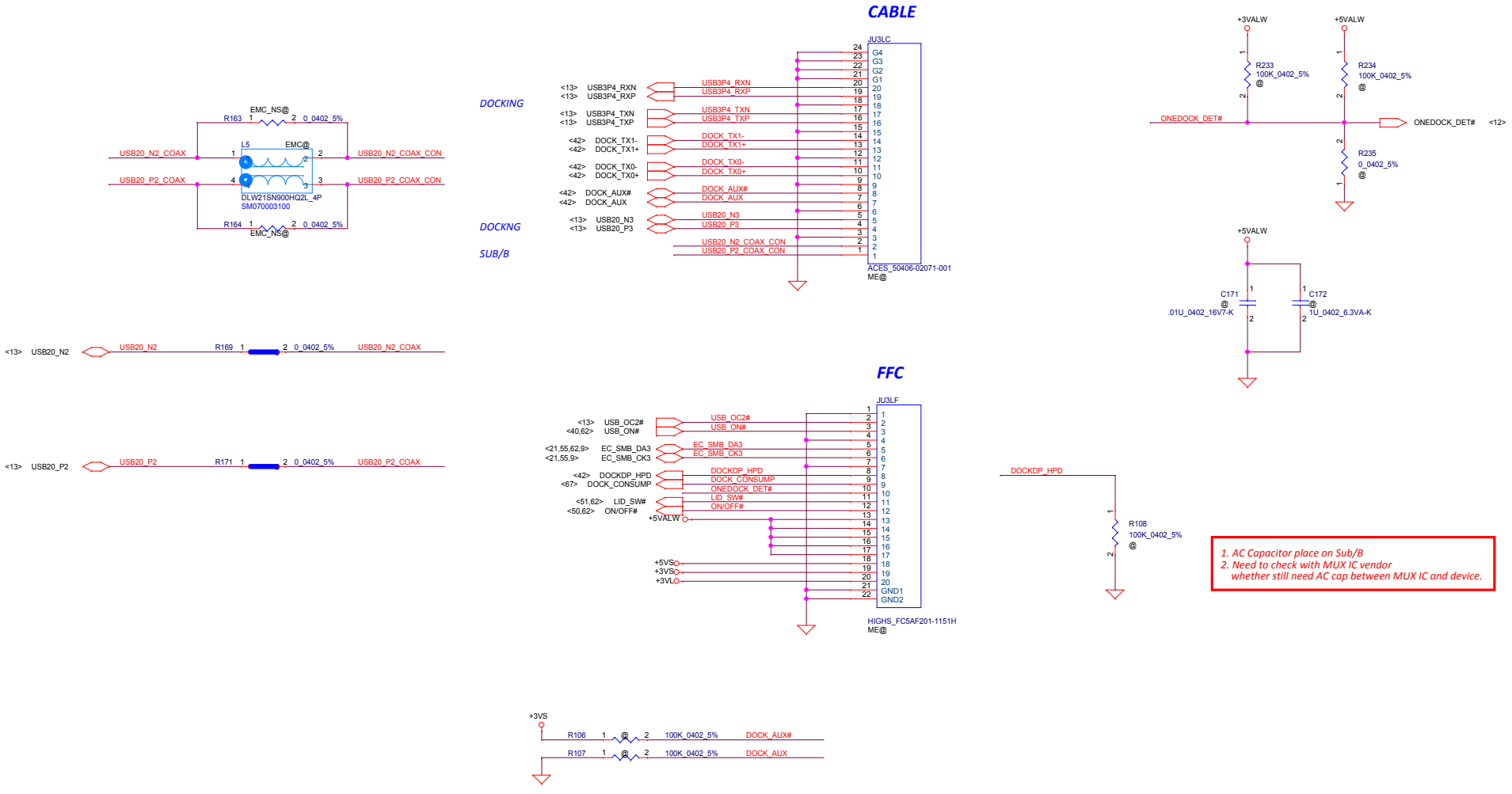

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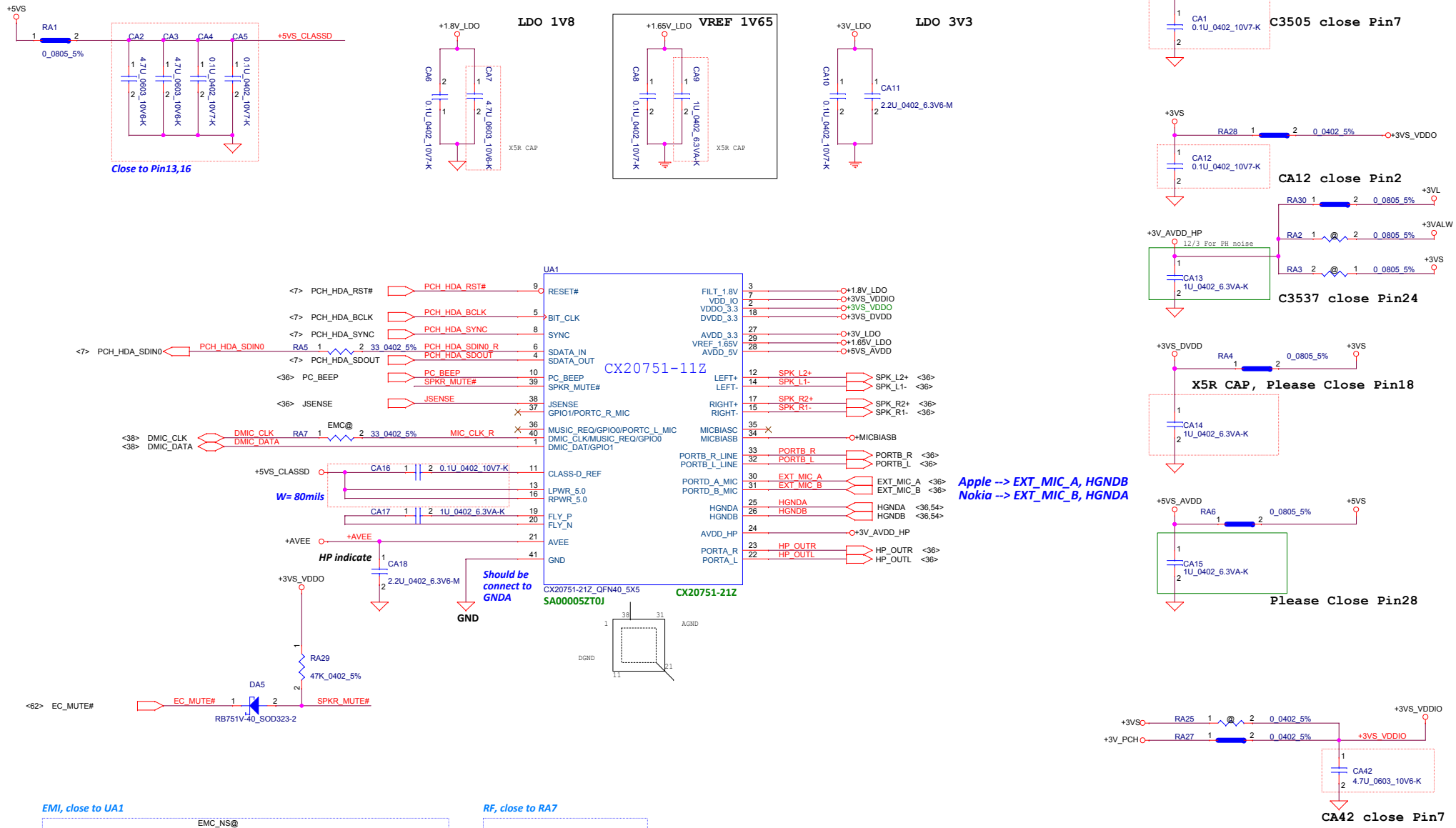

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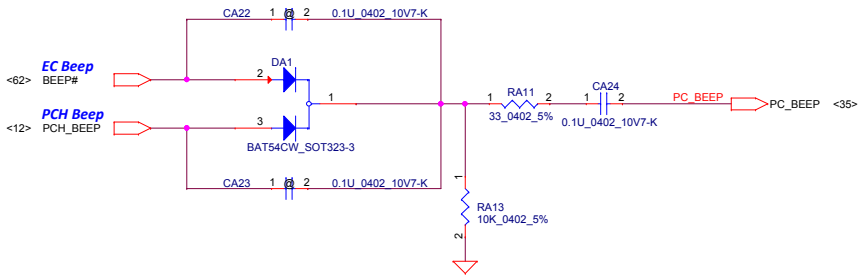
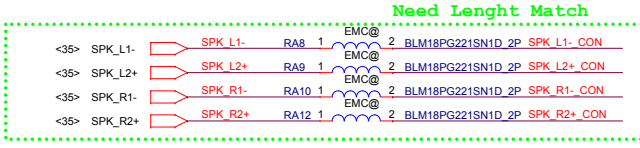
PC Beep



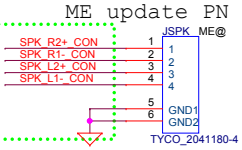
Speaker OUT

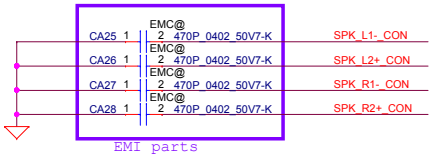
Need Lenght Match



SPK CONN.

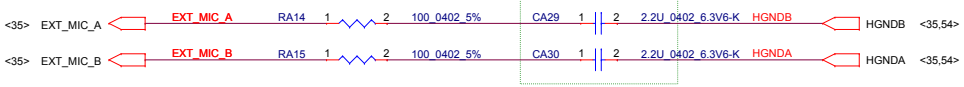
ME update PN



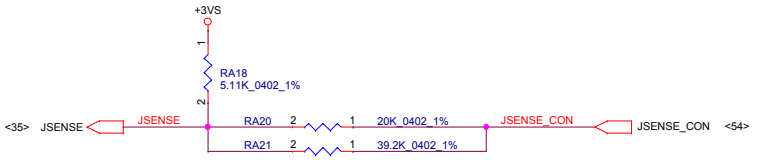


EXT. MIC/LINE IN

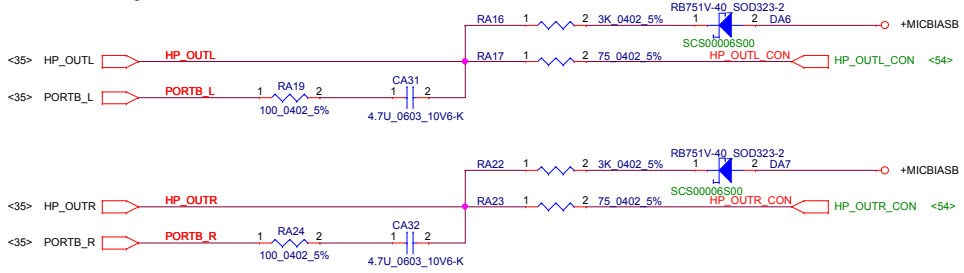
Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA



Changed CA29 & CA30 from 1uF to 2.2uF/X5R
to meet Port-D(headset-Mic) THD+N <= -65 dB



HeadPhone/LINE OUT



CA31, CA32 change to 4.7U for Quality requirement

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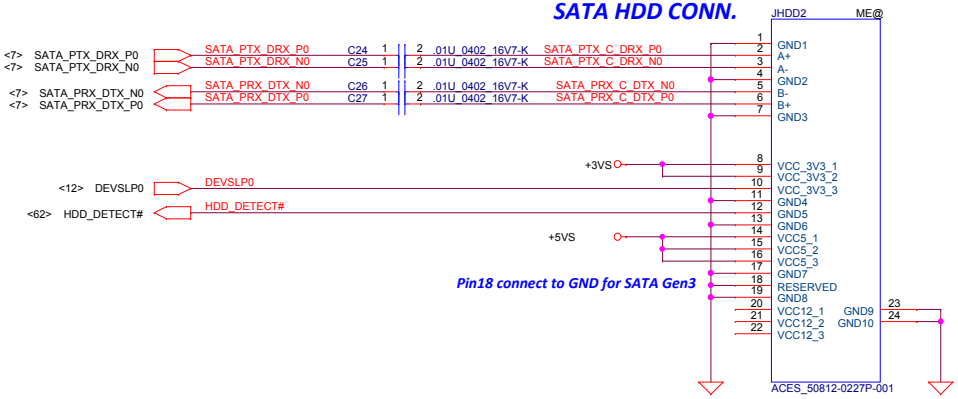
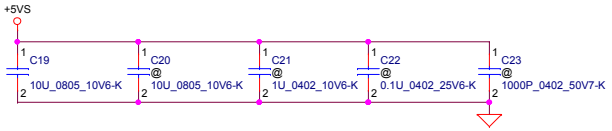
SATA HDD CONN.





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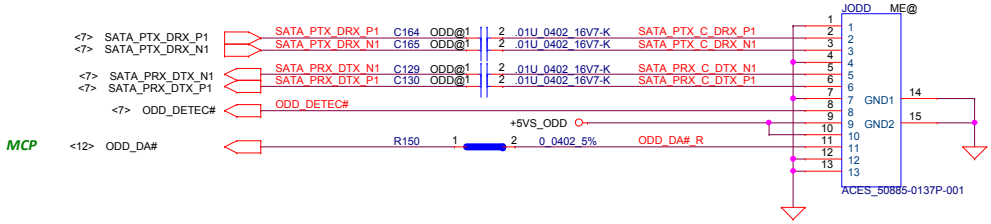
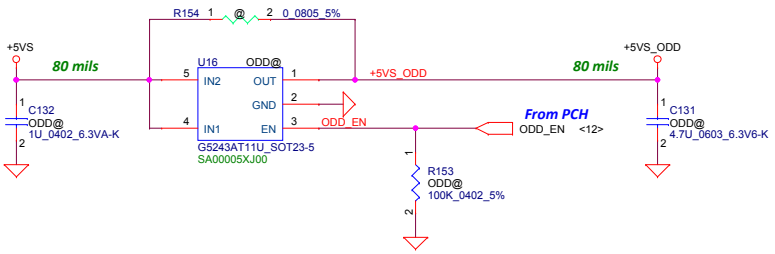
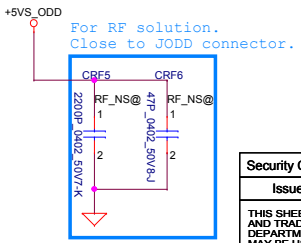


+5VS TO +5VS_ODD





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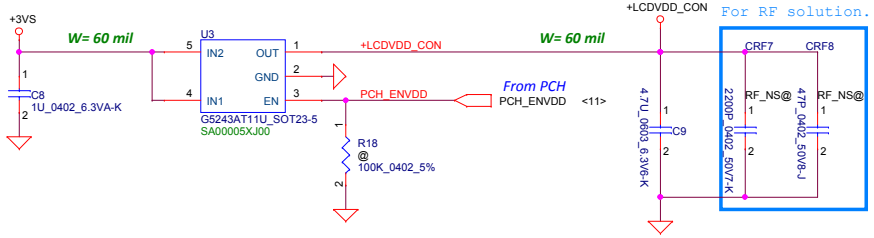
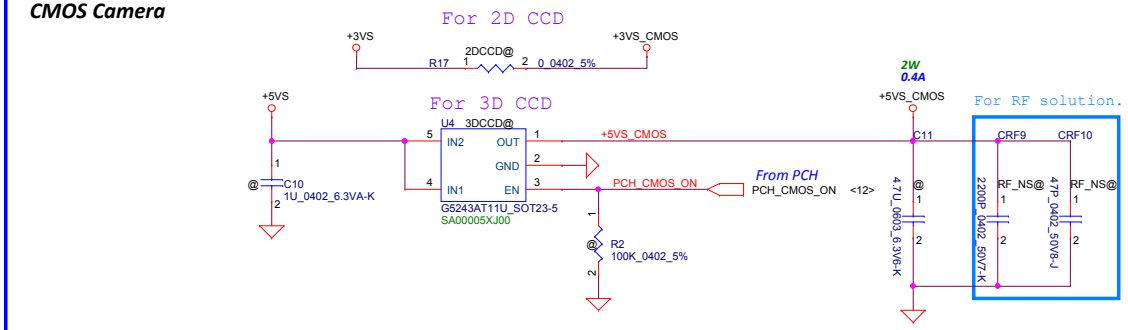
LCDVDD Circuit



CMOS Camera



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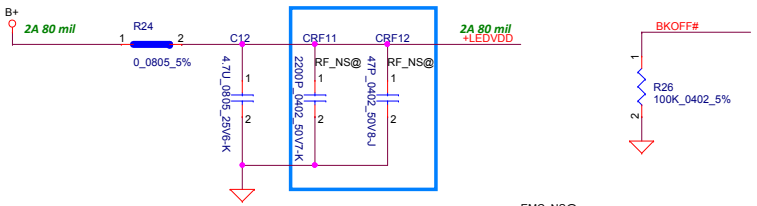

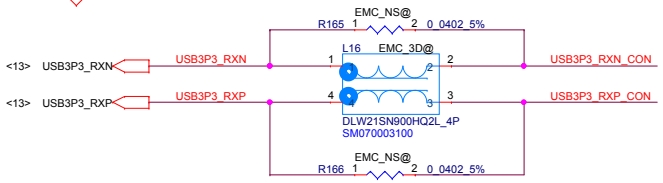

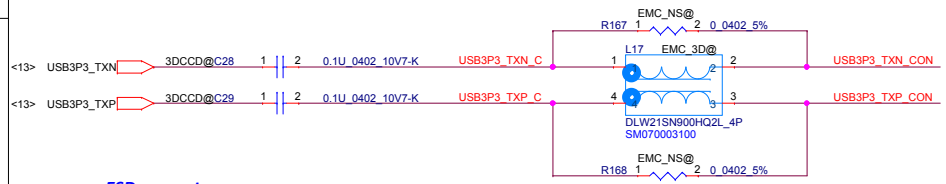

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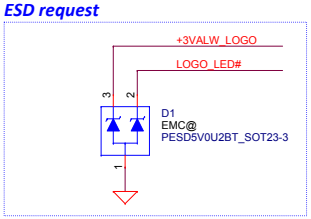
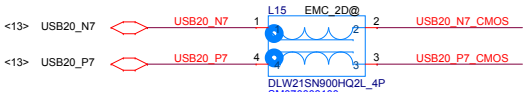
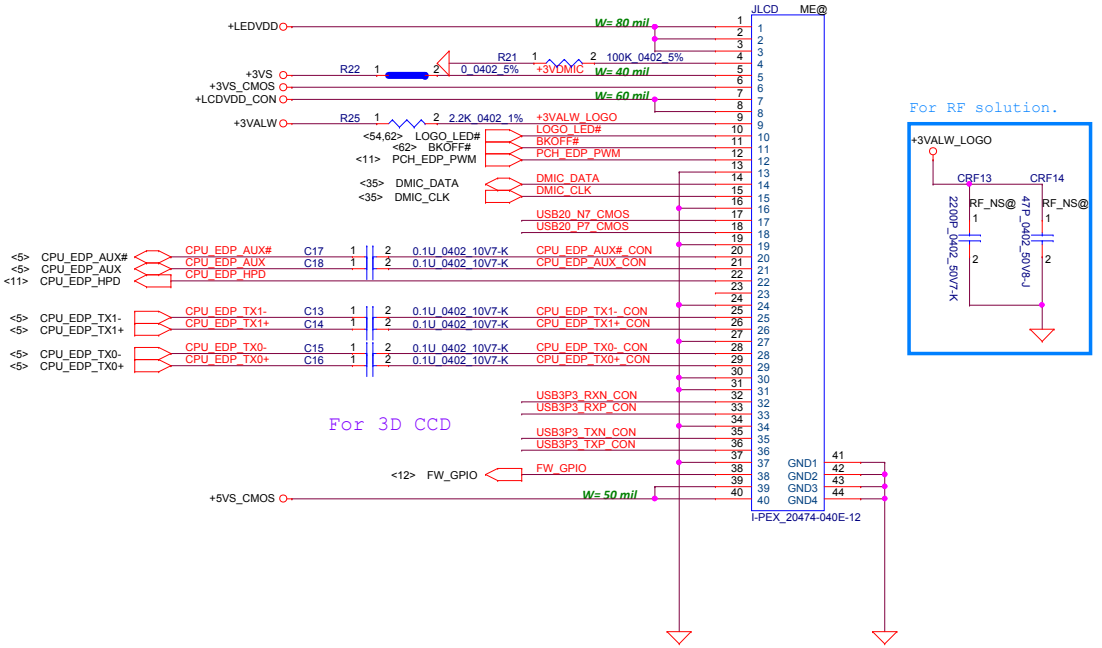


CMOS USB Port 2



eDP CONN.



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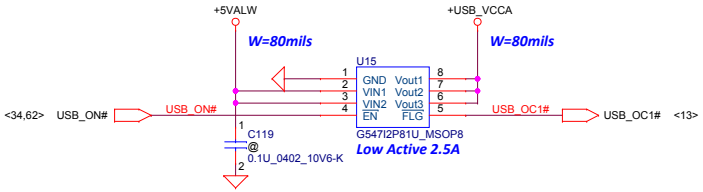
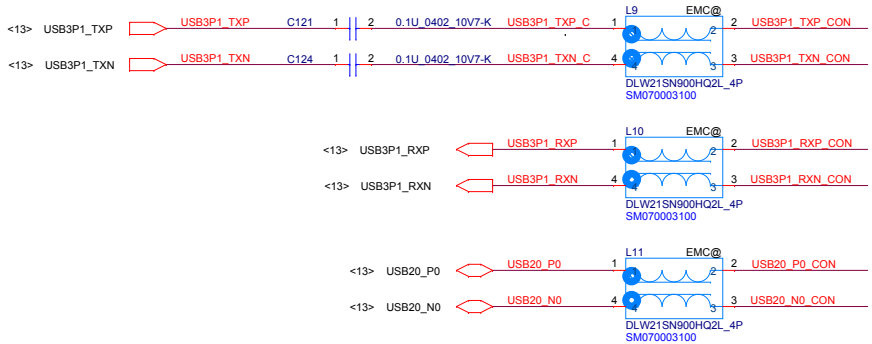
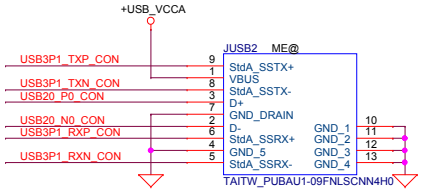
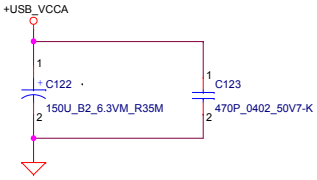
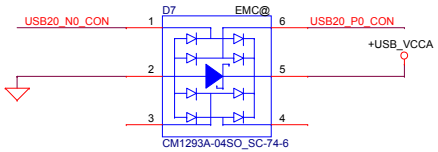
POWER SWITCH

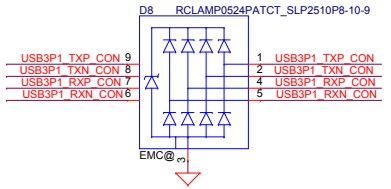












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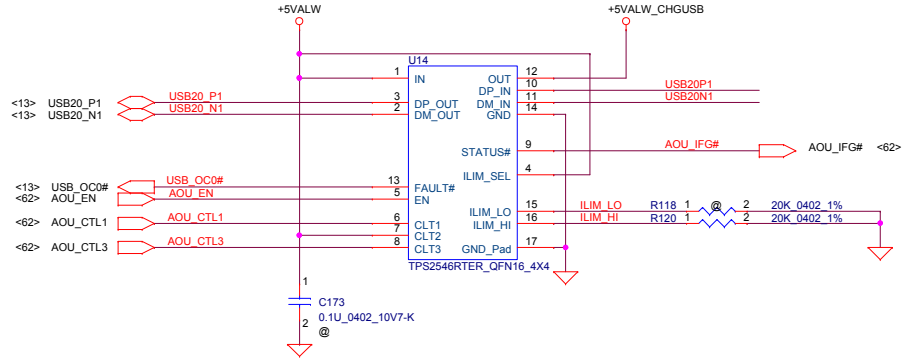

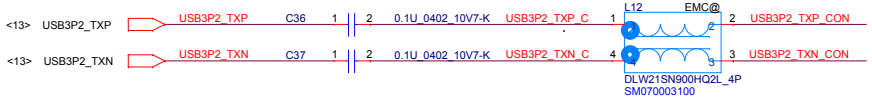

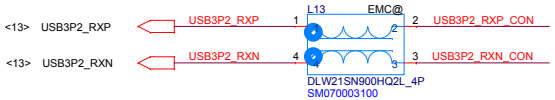

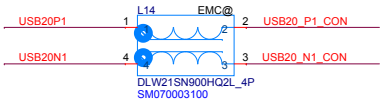

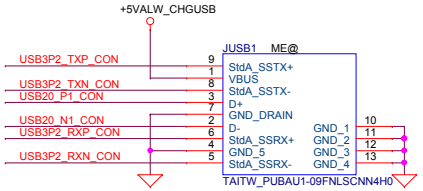

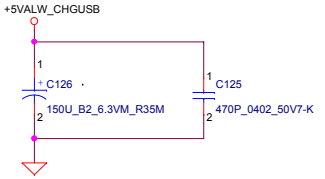

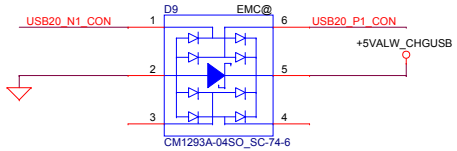

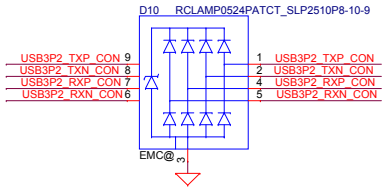

TI TPS2546

	CLT1	CLT2	CLT3	ILIM_SEL	MOD	
	0	0	0	X	**DCH**	OUT held low
*	1	1	1	1	**CDP**	Data Connected and Port Power Mgt. Function Active
*	1	1	1	0	**SDP2**	Data Connected
*	1	1	0	X	**SDP1**	Data Connected
*	0	1	0	X	**SDP1**	Data Connected
	1	0	0	X	**DCP_Short**	Device Forced to stay in DCP BC 1.2 charging mode
	1	0	1	X	**DCP_Divider**	Device Forced to stay in DCP Divider 1 Charging Mode
*	0	1	1	X	**DCP_Auto**	Data Disconnected and Port Power Mgt. Function Active
	0	0	1	X	**DCP_Auto**	Data Disconnected and Power Wake Function Active

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Title: **USB3 PORT2-FRONT(AOU)**

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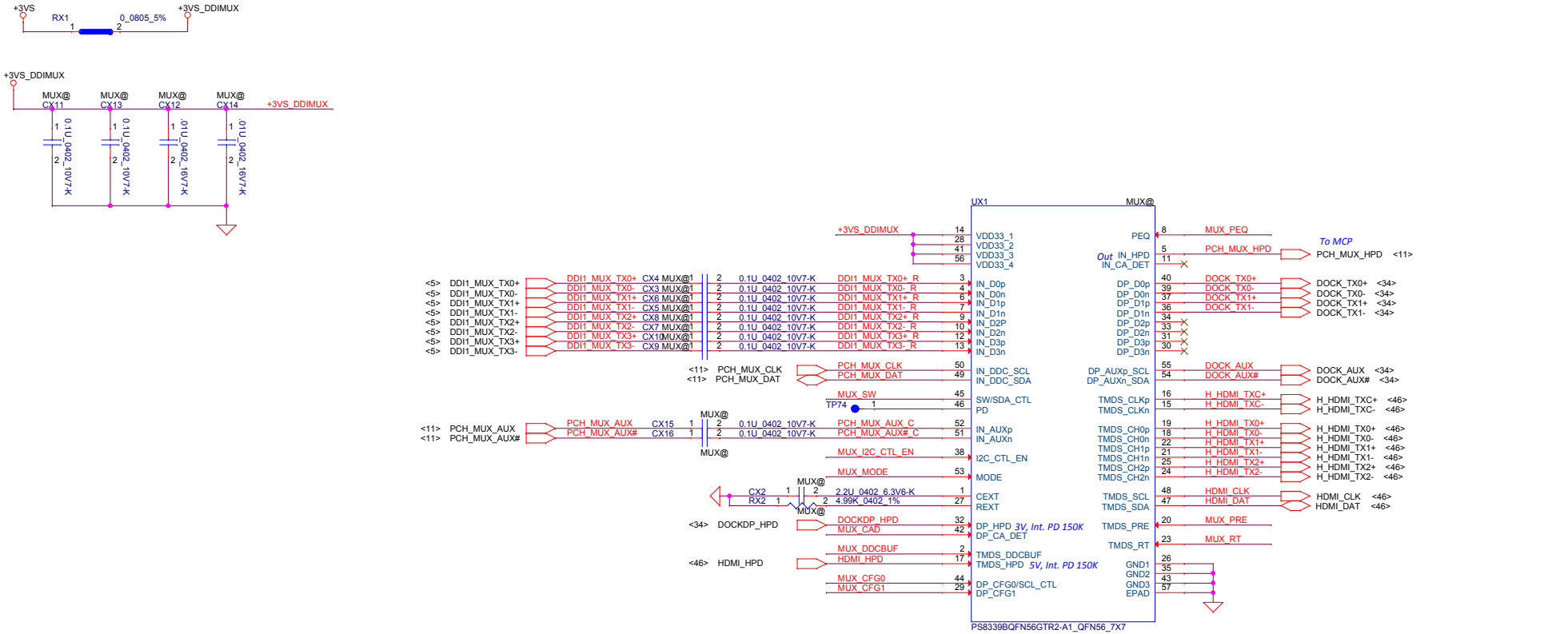

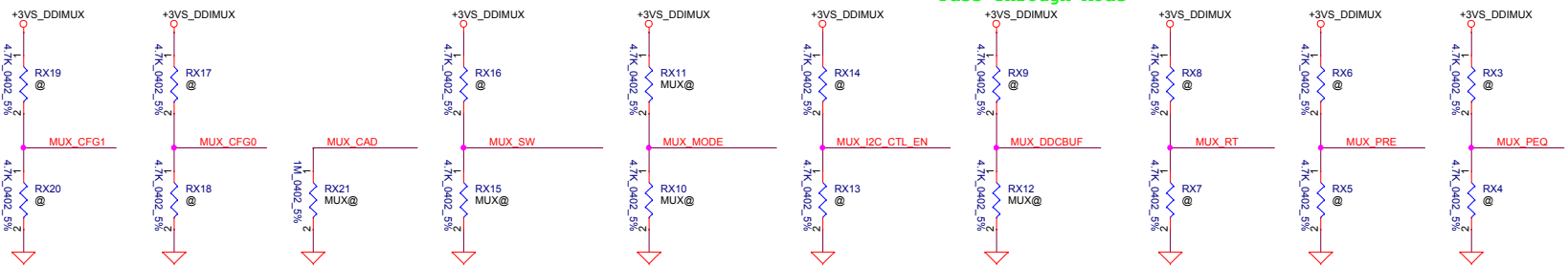

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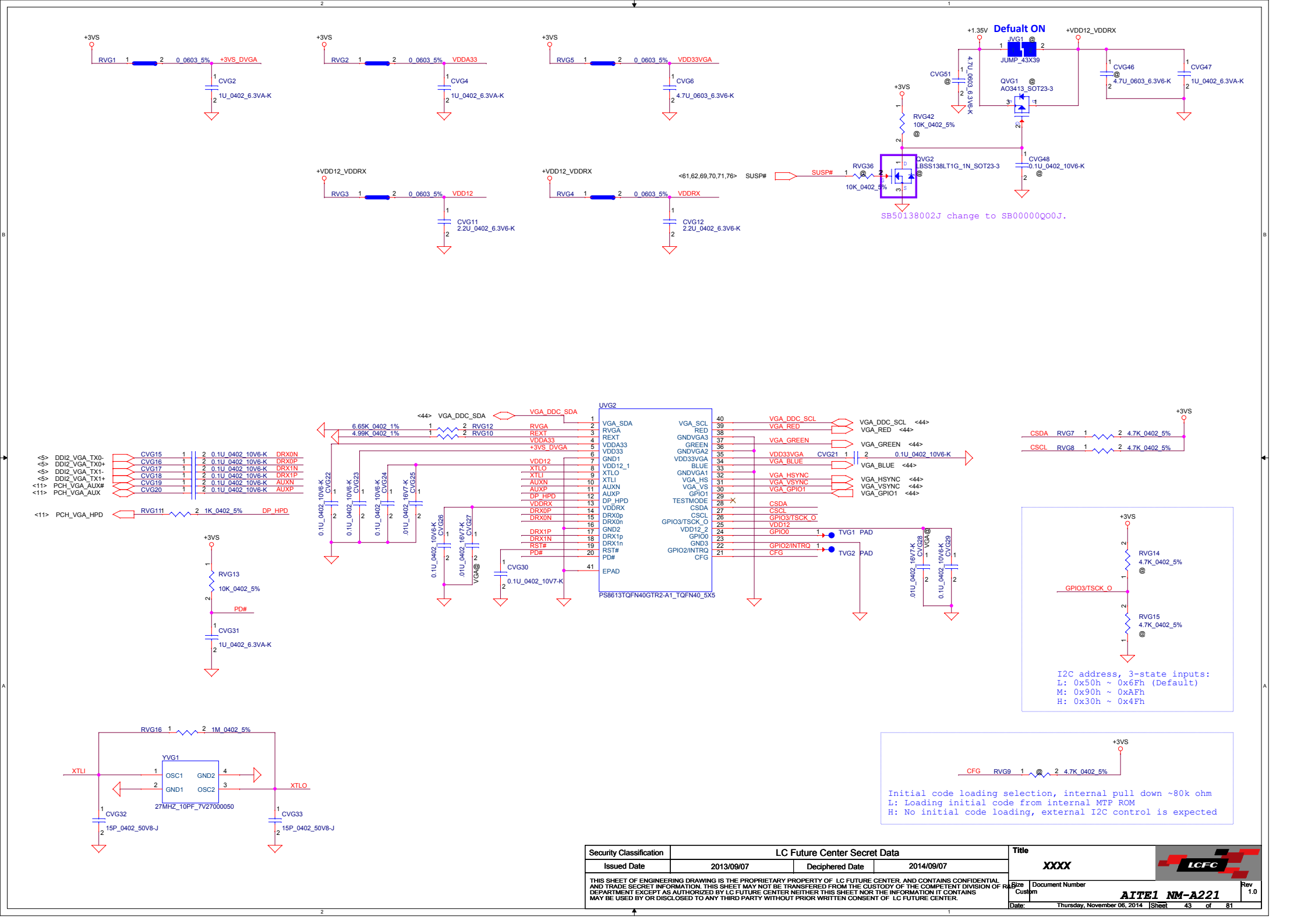
Date:	Thursday, November 06, 2014	Sheet	42 of 81



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Size	Document Number		Rev
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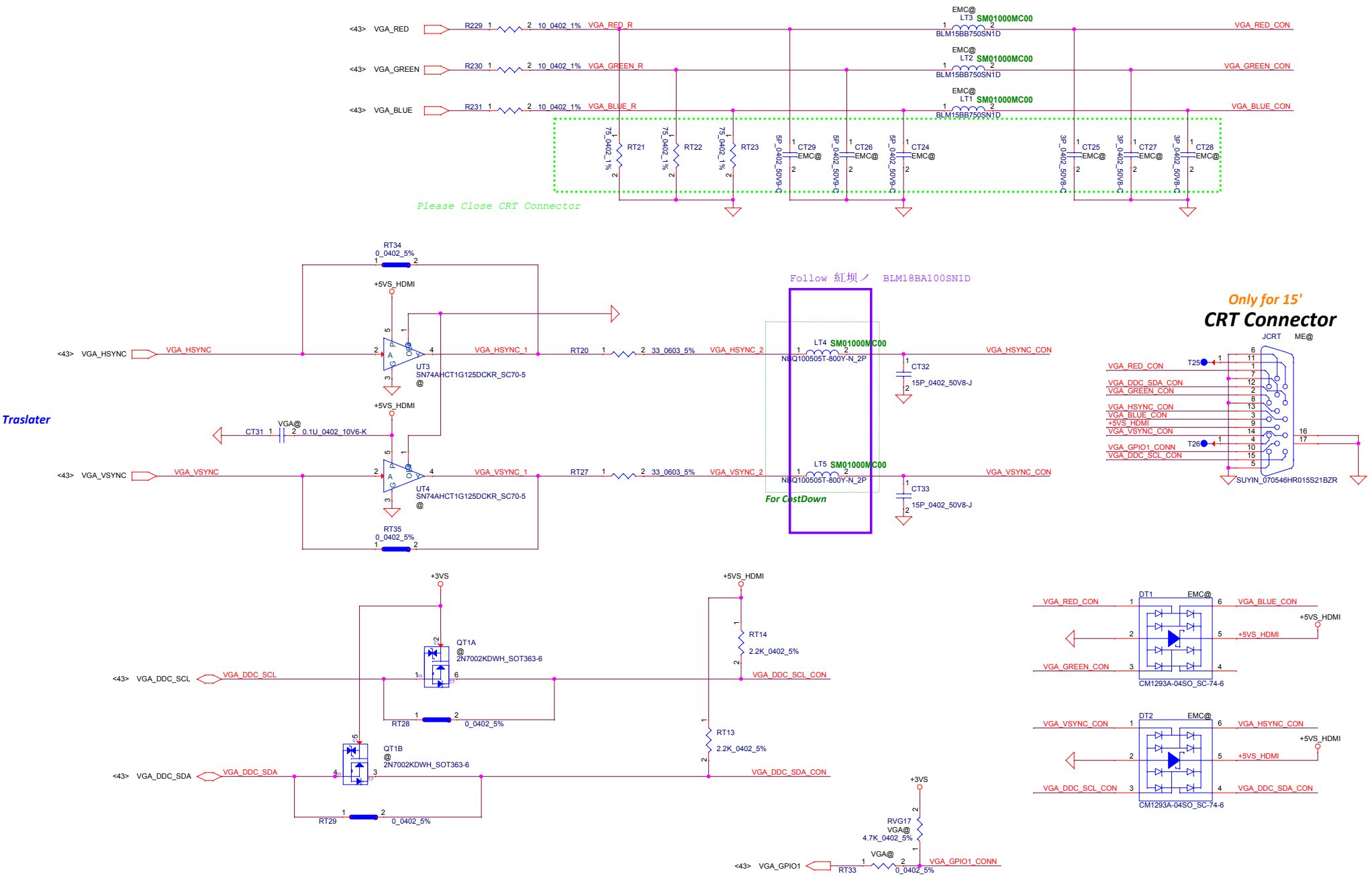
Date:	Thursday, November 06, 2014	Sheet	43 of 81



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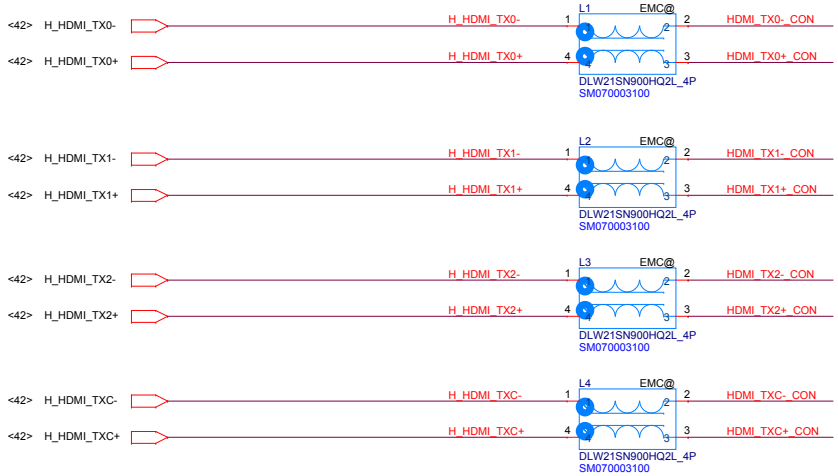
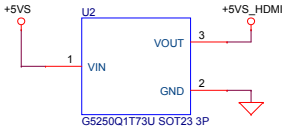
Title: *HDMI RP --> BLANK*

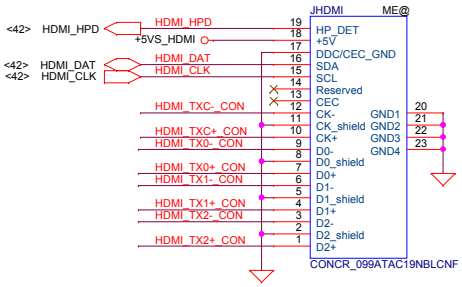
Size	Document Number	Rev
Custom	AITE1 NM-A221	1.0

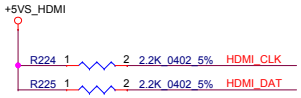
Date: Thursday, November 06, 2014 Sheet 45 of 81

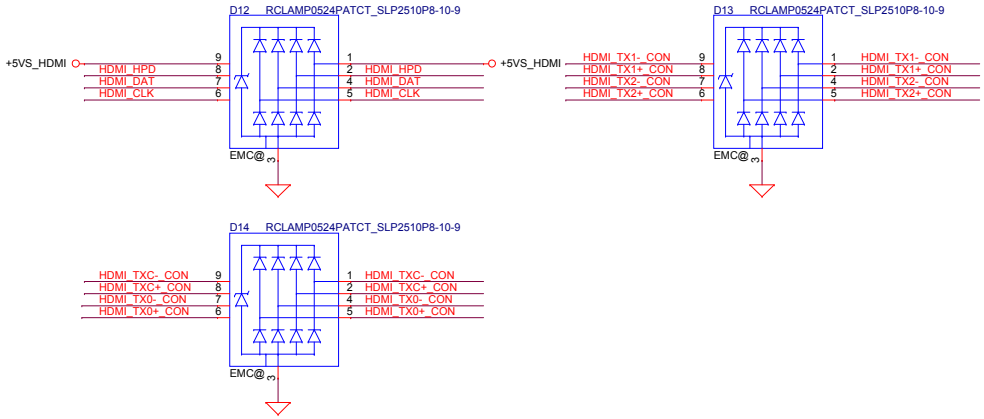




HDMI CONN.







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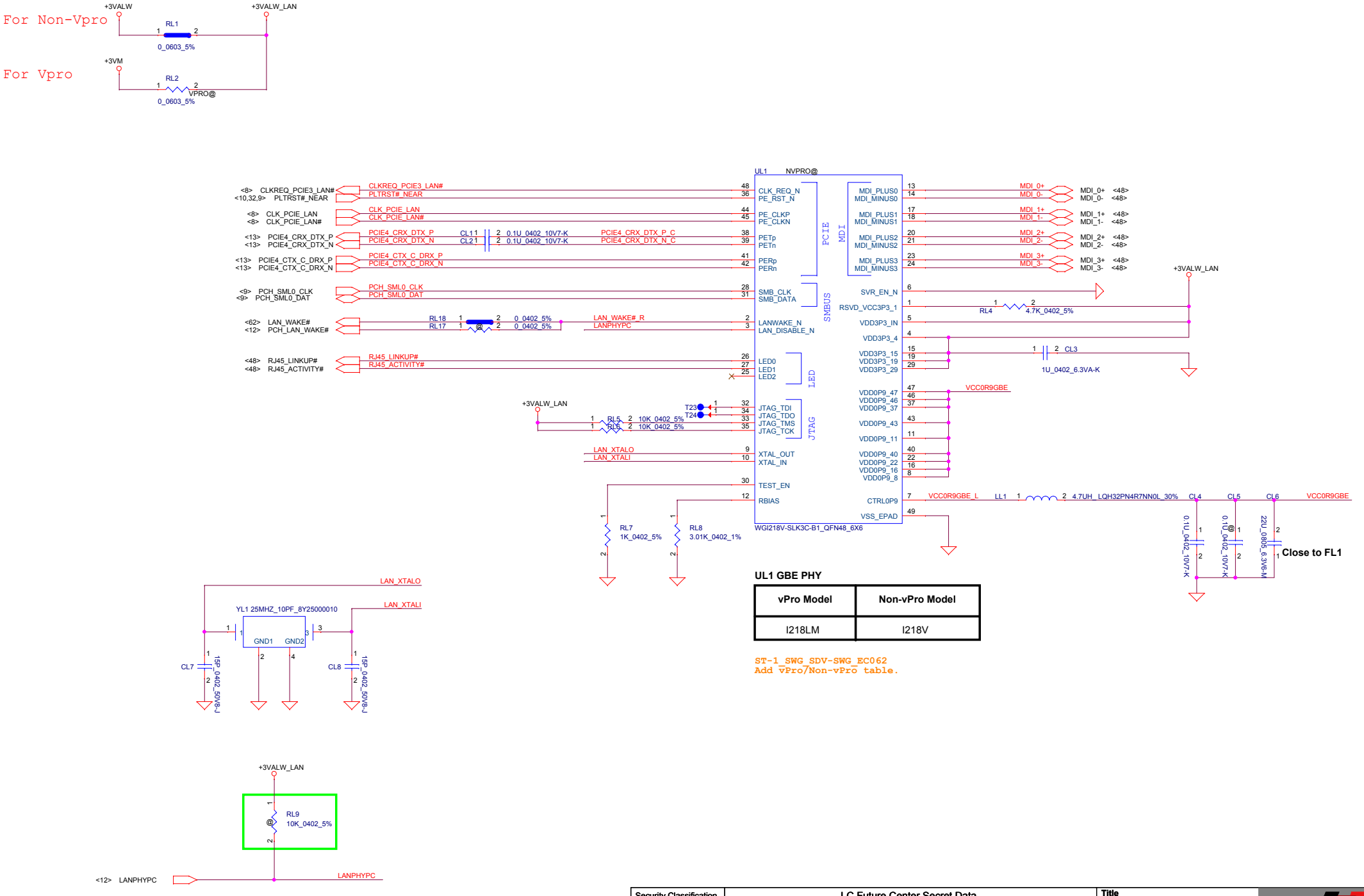

UL1 GBE PHY

vPro Model	Non-vPro Model
I218LM	I218V

ST-1_SWG_SDV-SWG_EC062
Add vPro/Non-vPro table.

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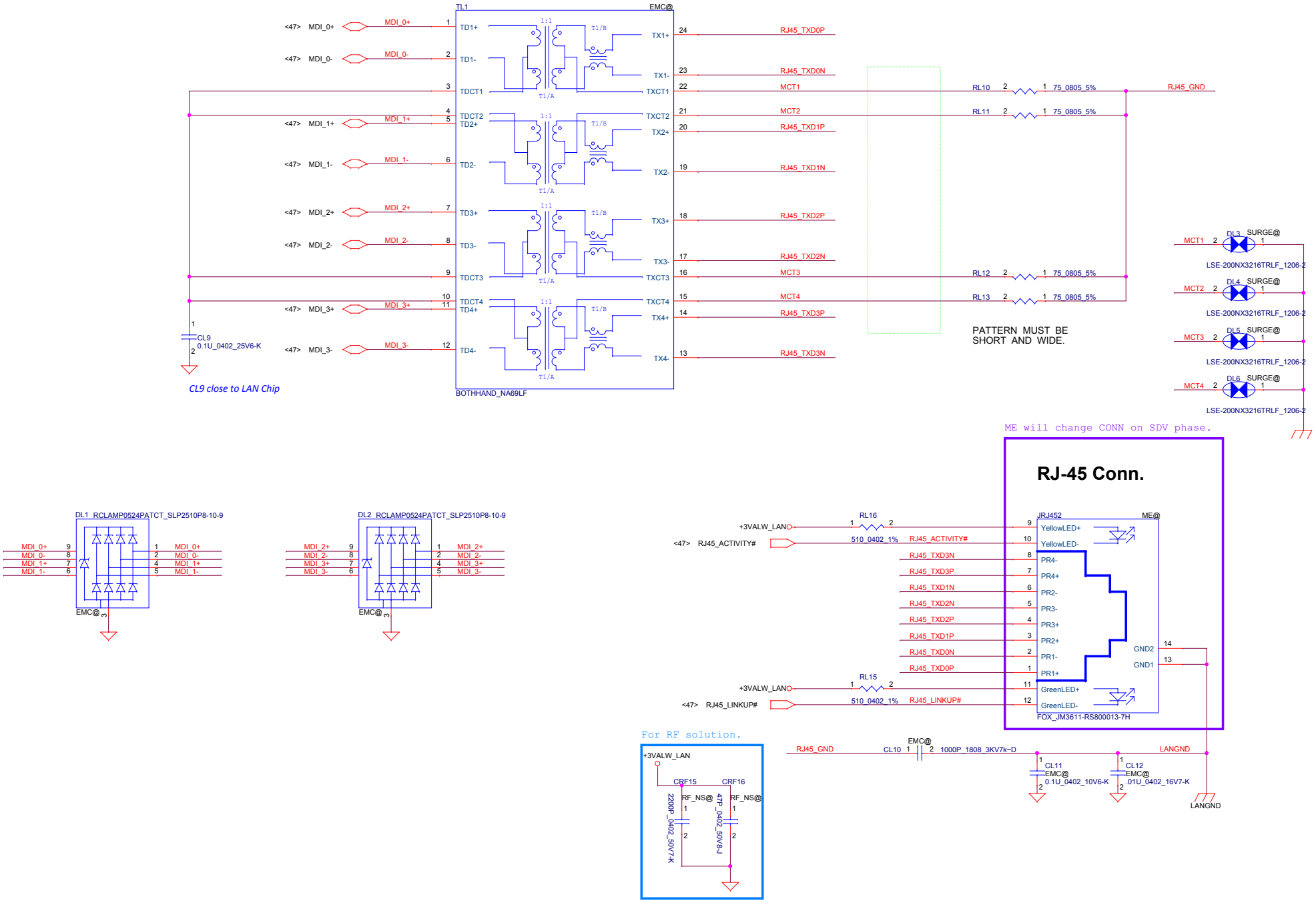

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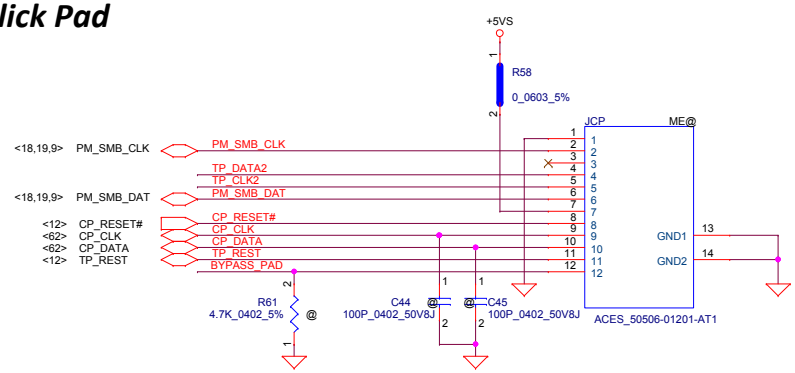
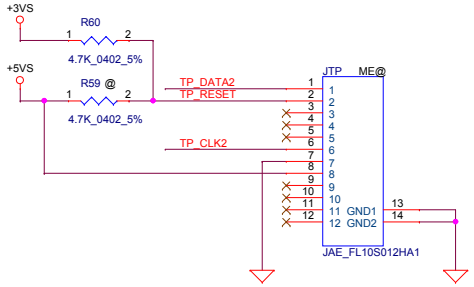
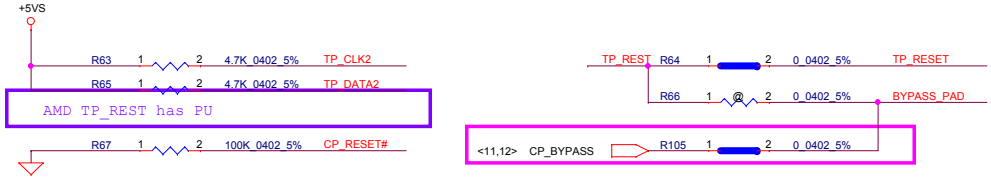
Click Pad



Track point





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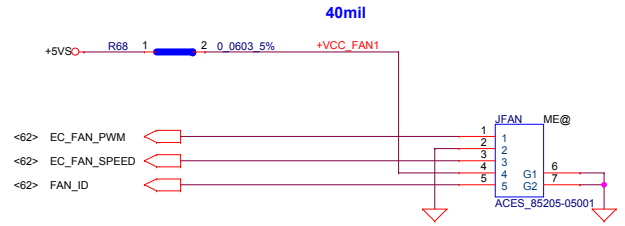
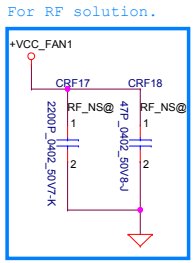
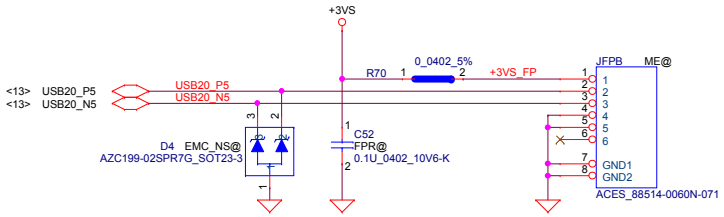
FAN CONN.



惠璶籔AMD籔THERMAL絋板PIN define



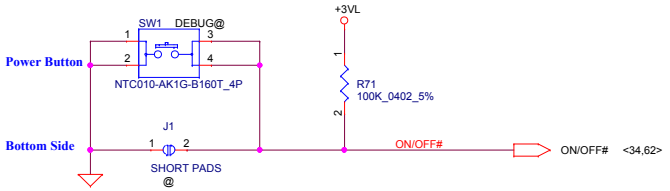
FingerPrint CONN.



PWR BTN/LID SW CONN.

For 14" on board
For 15" on Sub/B

ON/OFF Switch --> 簿 :Sub/B



Lid Switch --> 簿 :Sub/B

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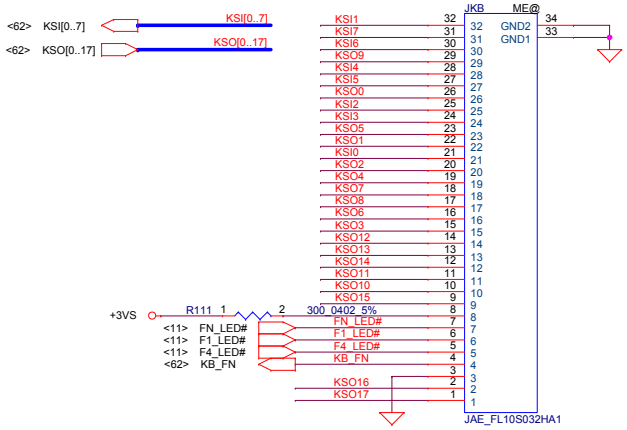
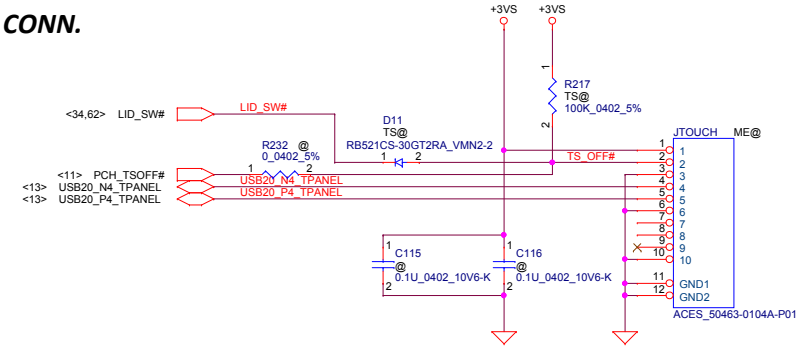
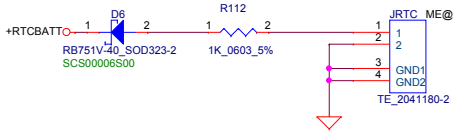
KB CONN



TOUCH PANEL CONN.



RTC CONN.



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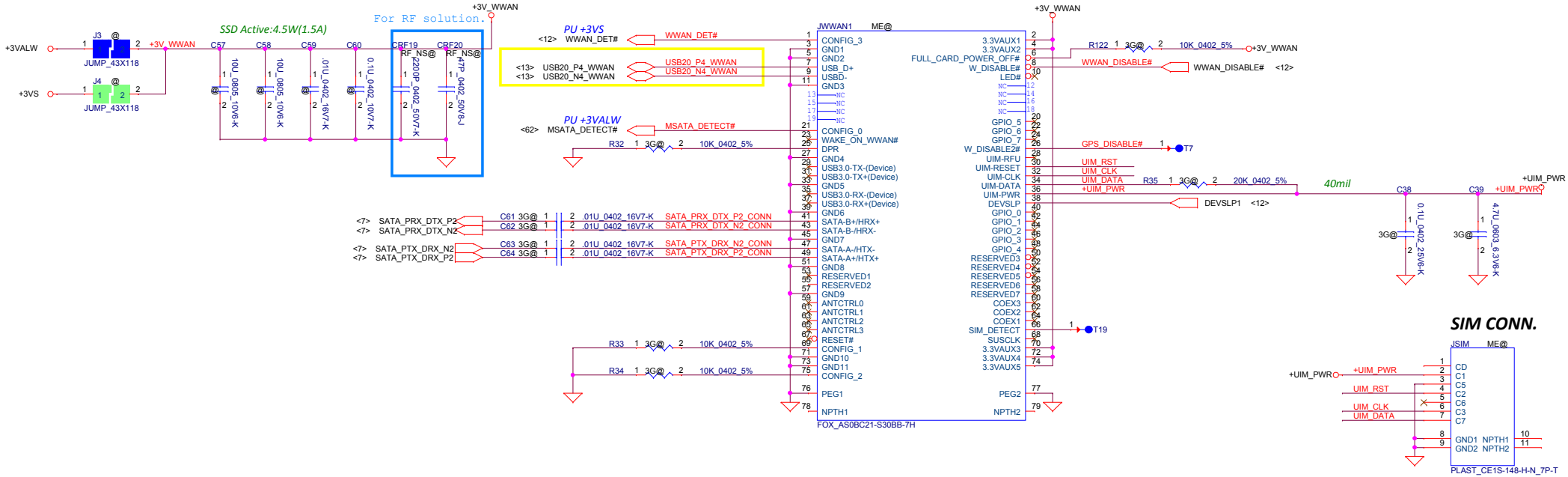
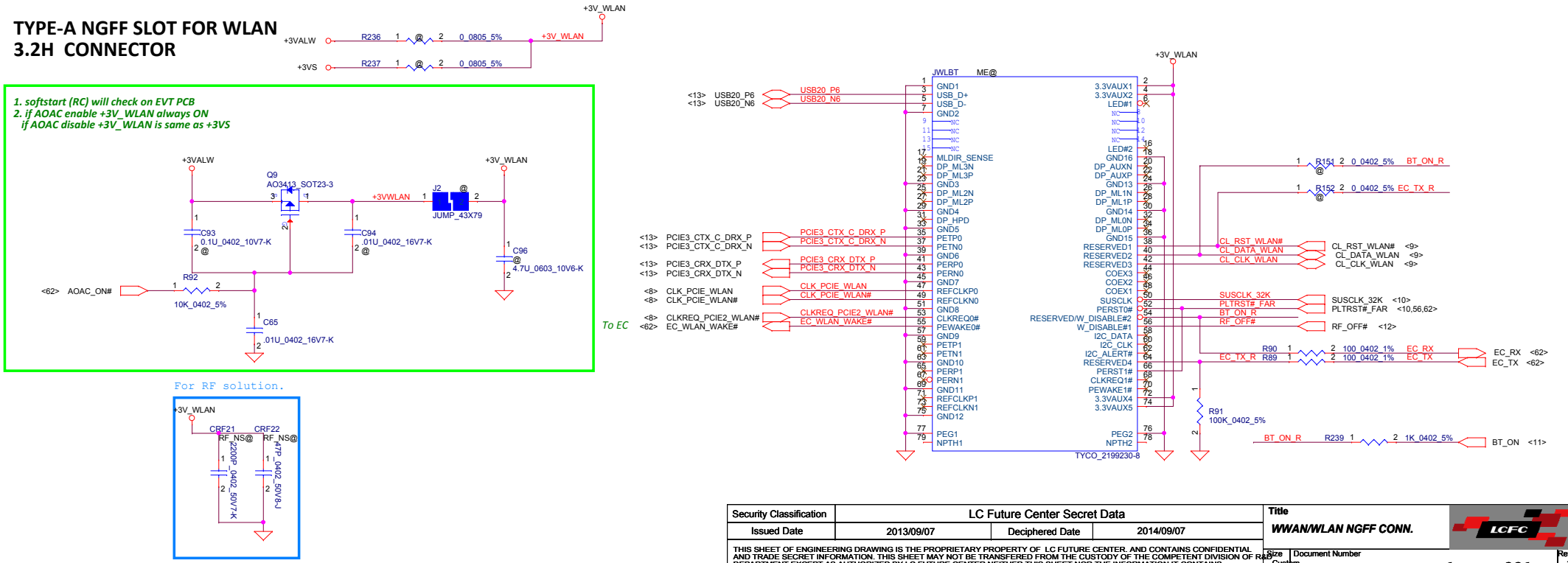
TYPE-B NGFF SLOT FOR WWAN/SSD
3.2H CONNECTOR



TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR



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Title: WWAN/WLAN NGFF CONN.

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Title: XXXX

LCFC

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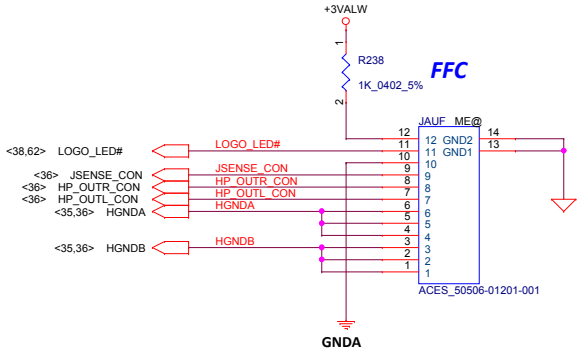
For Edge 15" Audio board CONNECTOR



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Title: ***SUB-AUDIO JACK CONN.***

Size	Document Number	Rev
Custom	***AITE1 NM-A221***	1.0

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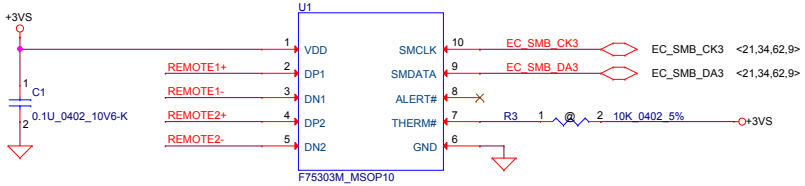
Thermal Sensor

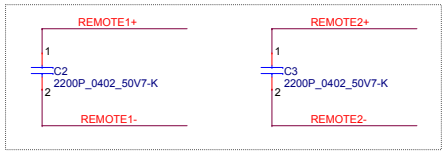
Thermal Sensor
placed near by VRAM



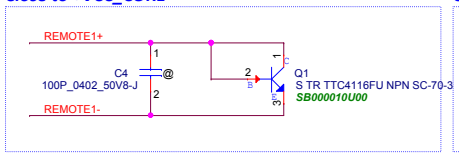
Address 1001_101xb

Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

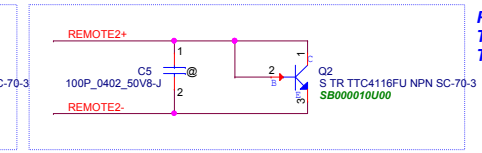
Close to U1



Close to +VCC_CORE



Close JDIMM1&JDIMM2



REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

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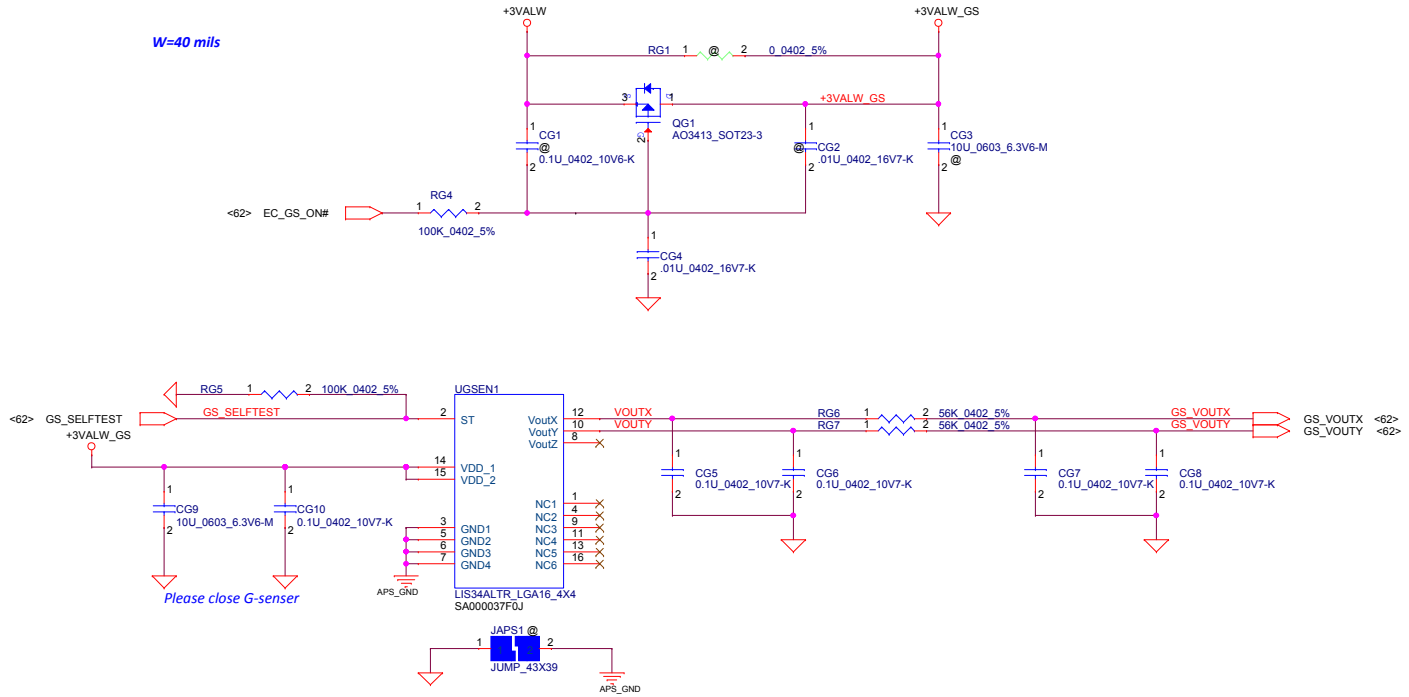
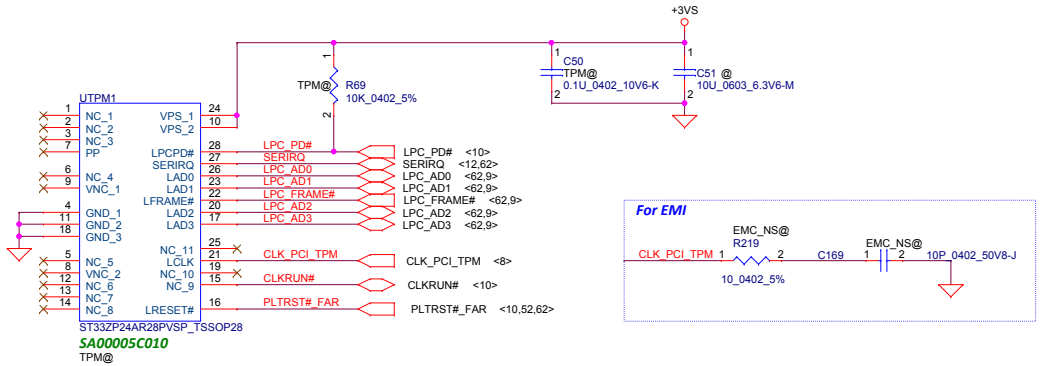
APS G-Sensor



TPM IC



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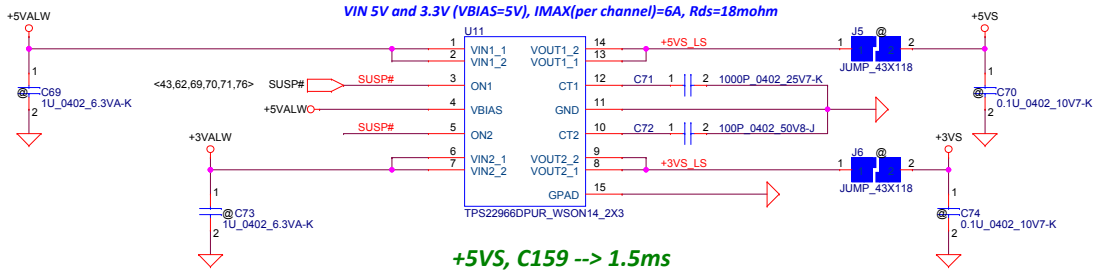
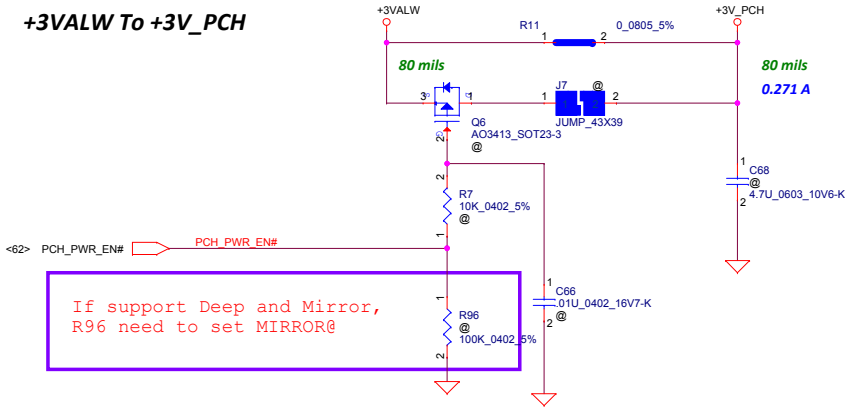
Load Switch
+5VALW To +5VS
+3VALW To +3VS

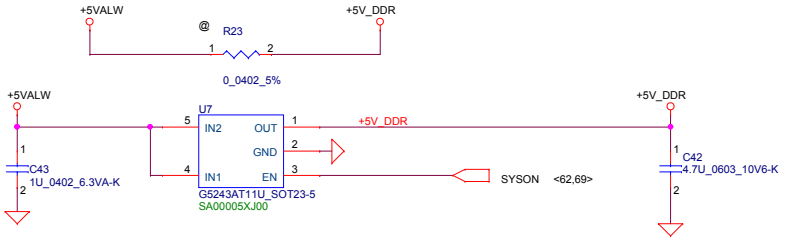


+5VS, C159 --> 1.5ms
+3VS, C160 --> 2.5ms

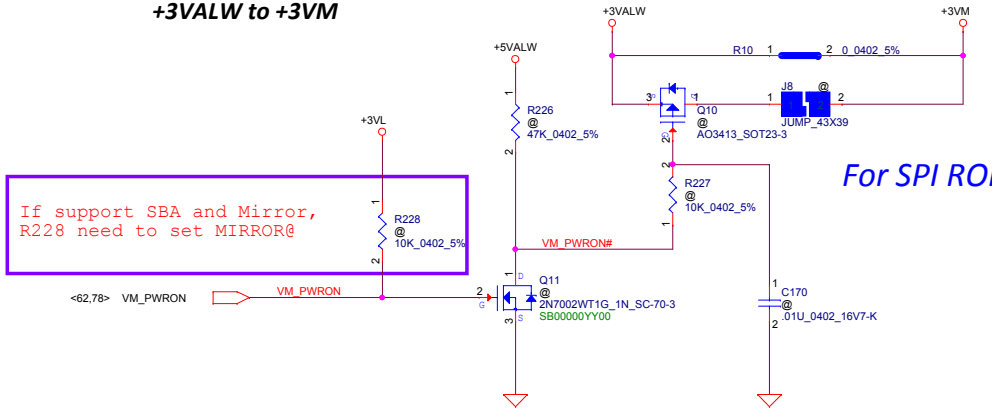
+3VALW To +3V_PCH



+5VALW To +5V_DDR



+3VALW to +3VM



For SPI ROM/LAN VPRO

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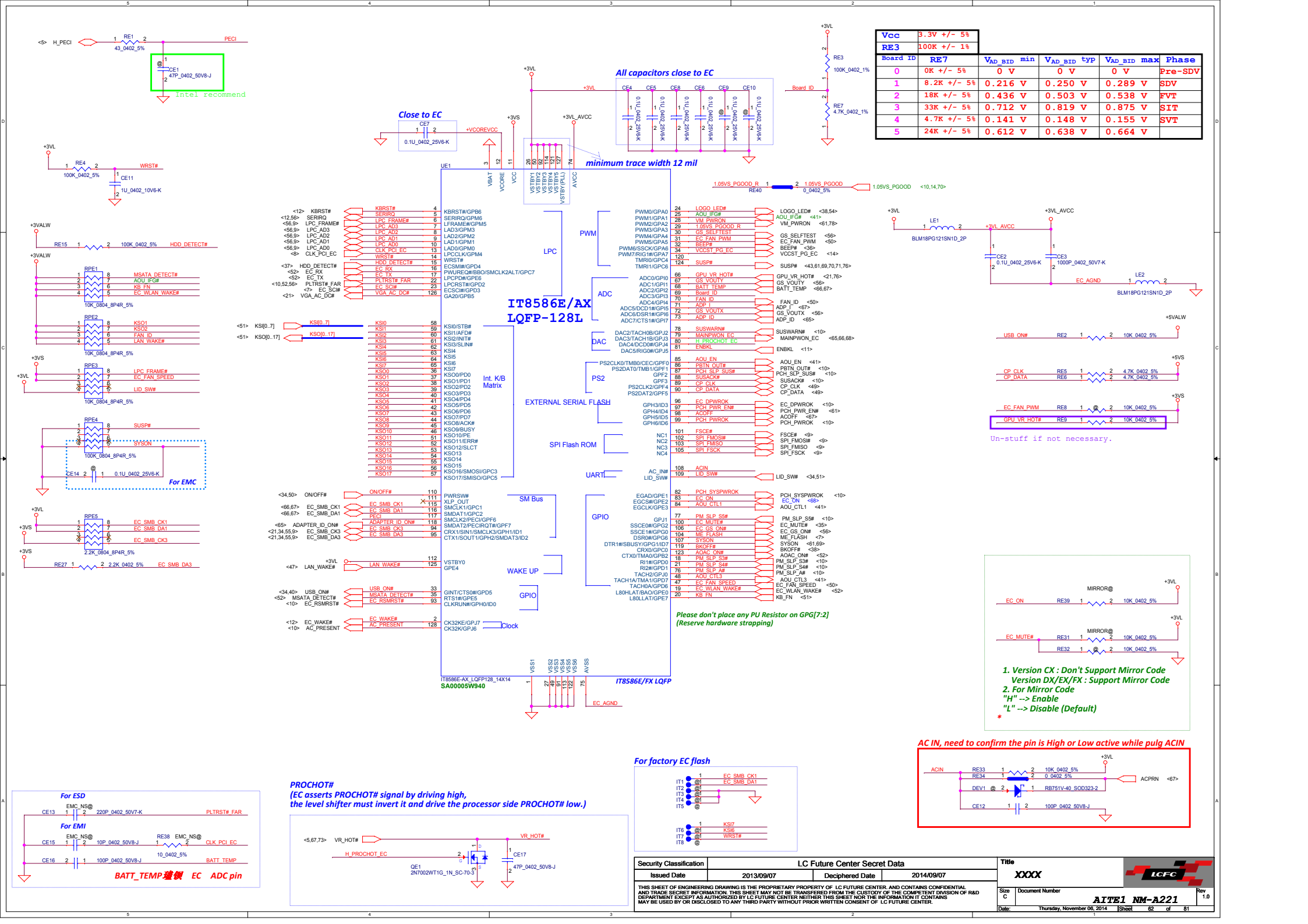

Vcc	3.3V +/- 5%
RE3	100K +/- 1%

Board ID	RE7	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	Pre-SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SDV
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	SVT
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

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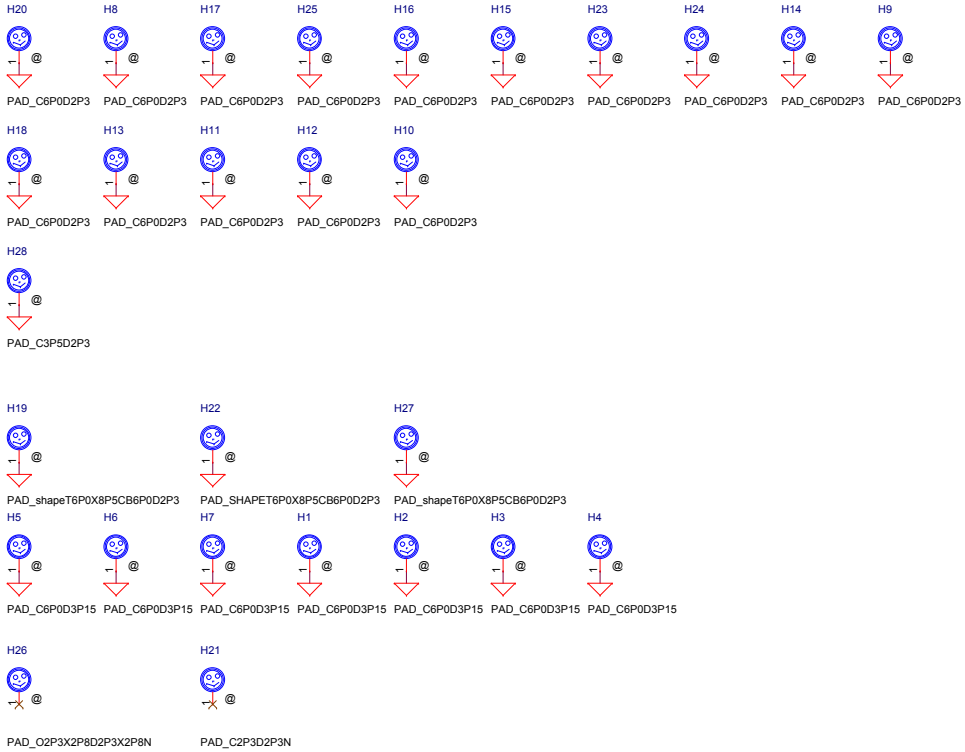
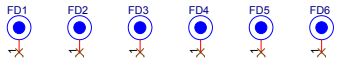
Screw Hole



Center Zero

PCB Fedical Mark PAD



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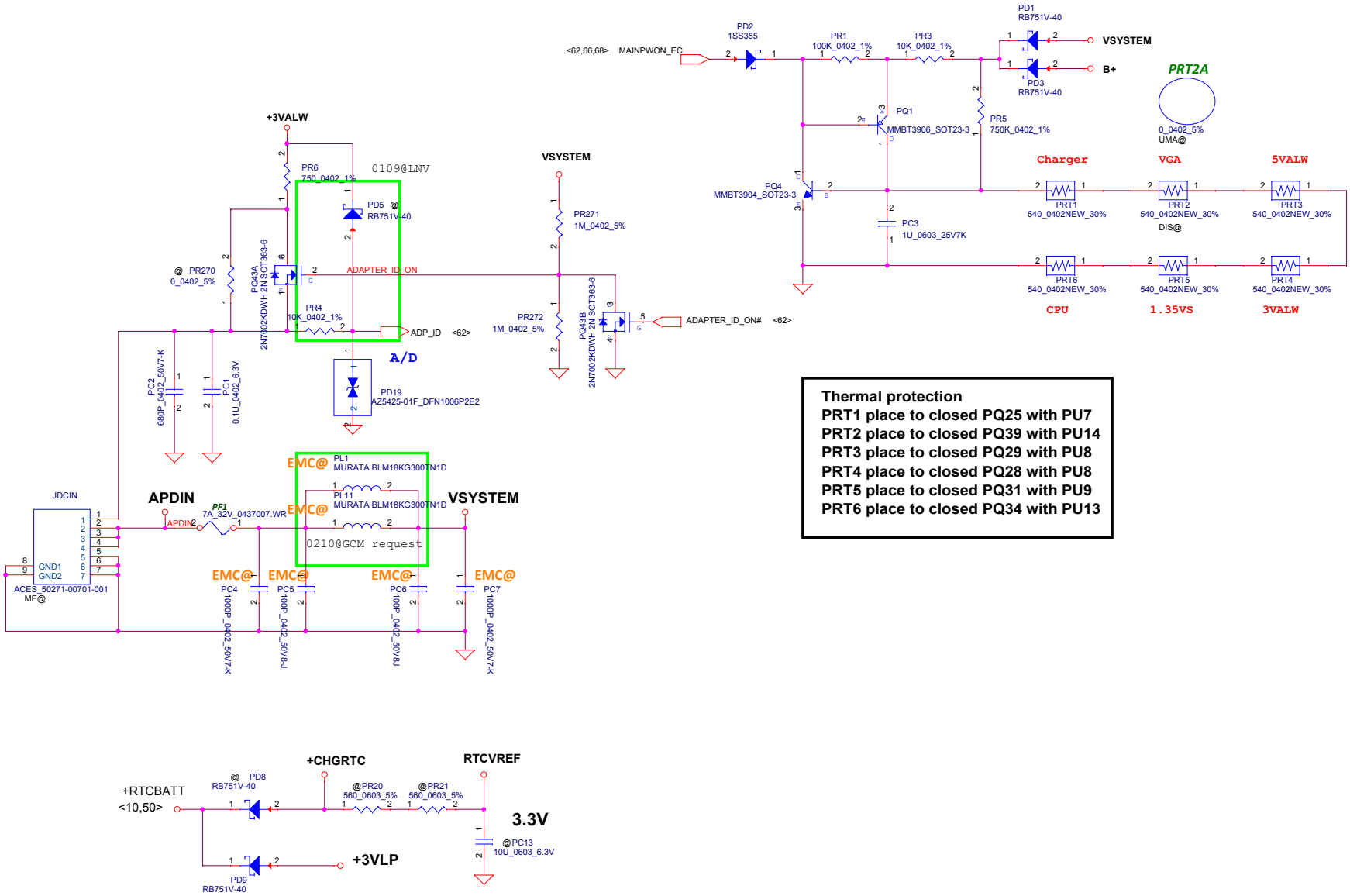

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Title: *DCIN / Vin Detector*

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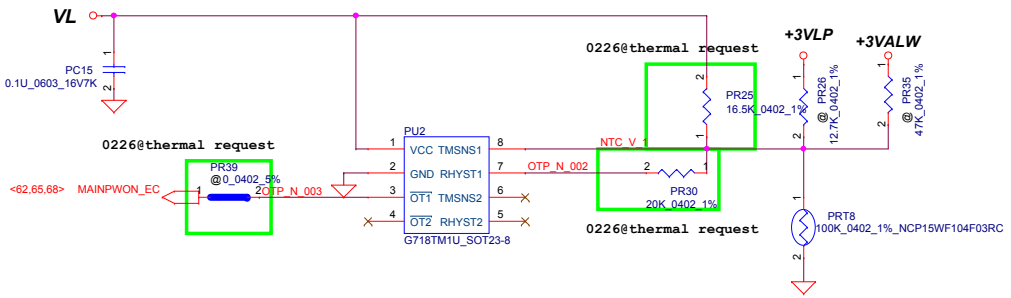
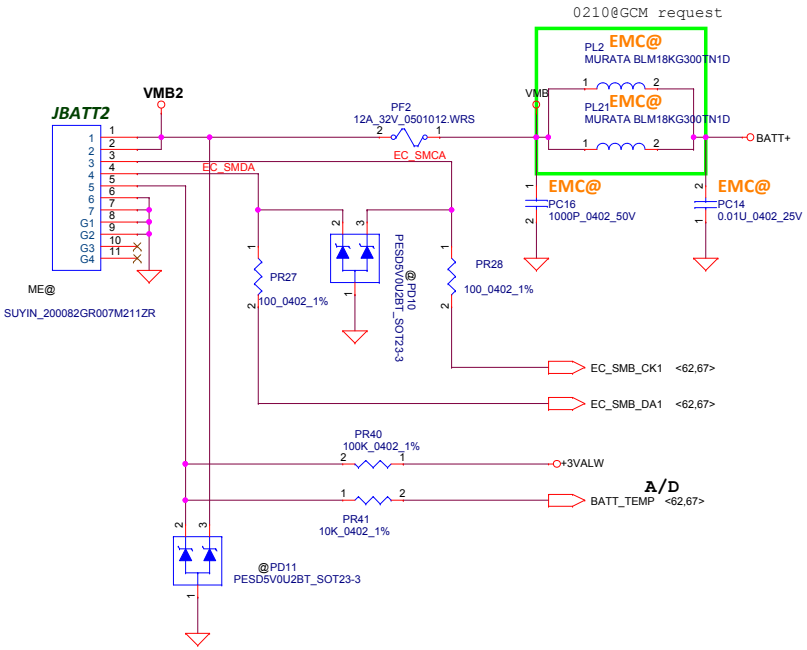
PRT8 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C





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Title: BATTERY CONN/OTP

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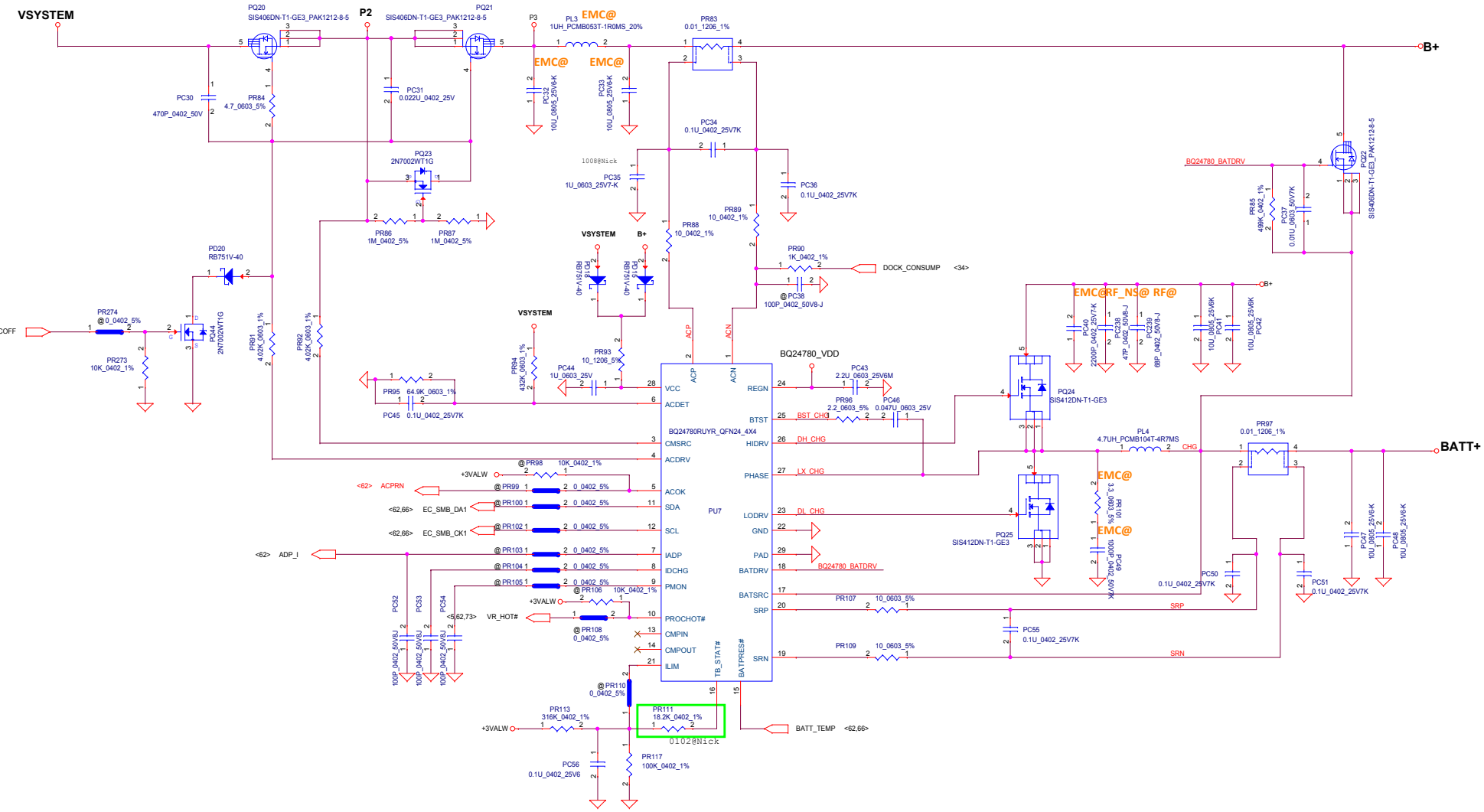

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Issued Date	2013/08/05	Deciphered Date	2014/12/31

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Title: CHARGER

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C	AITE1 NM-A221	1.0

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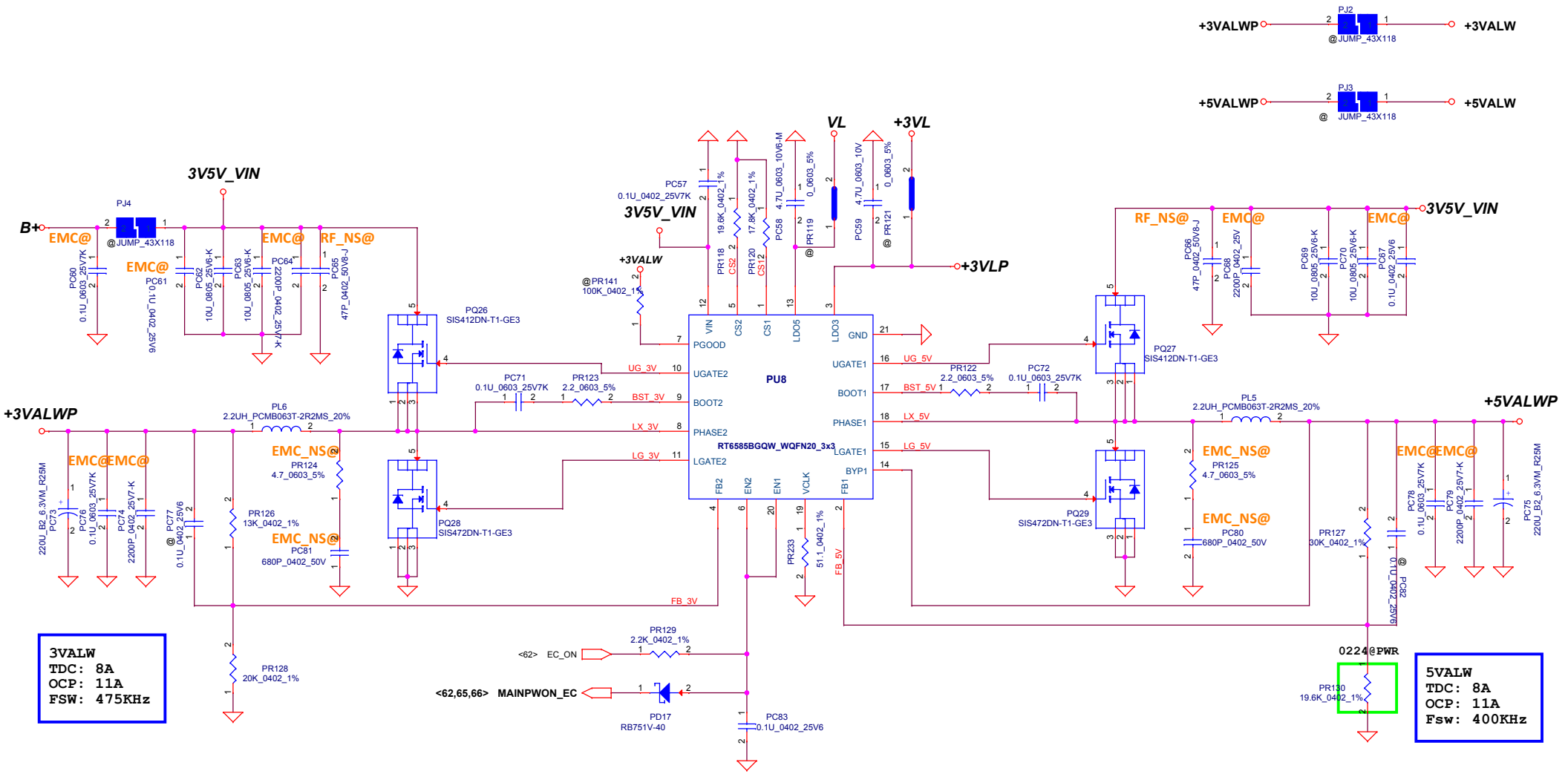

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Title: 3VALW/5VALW

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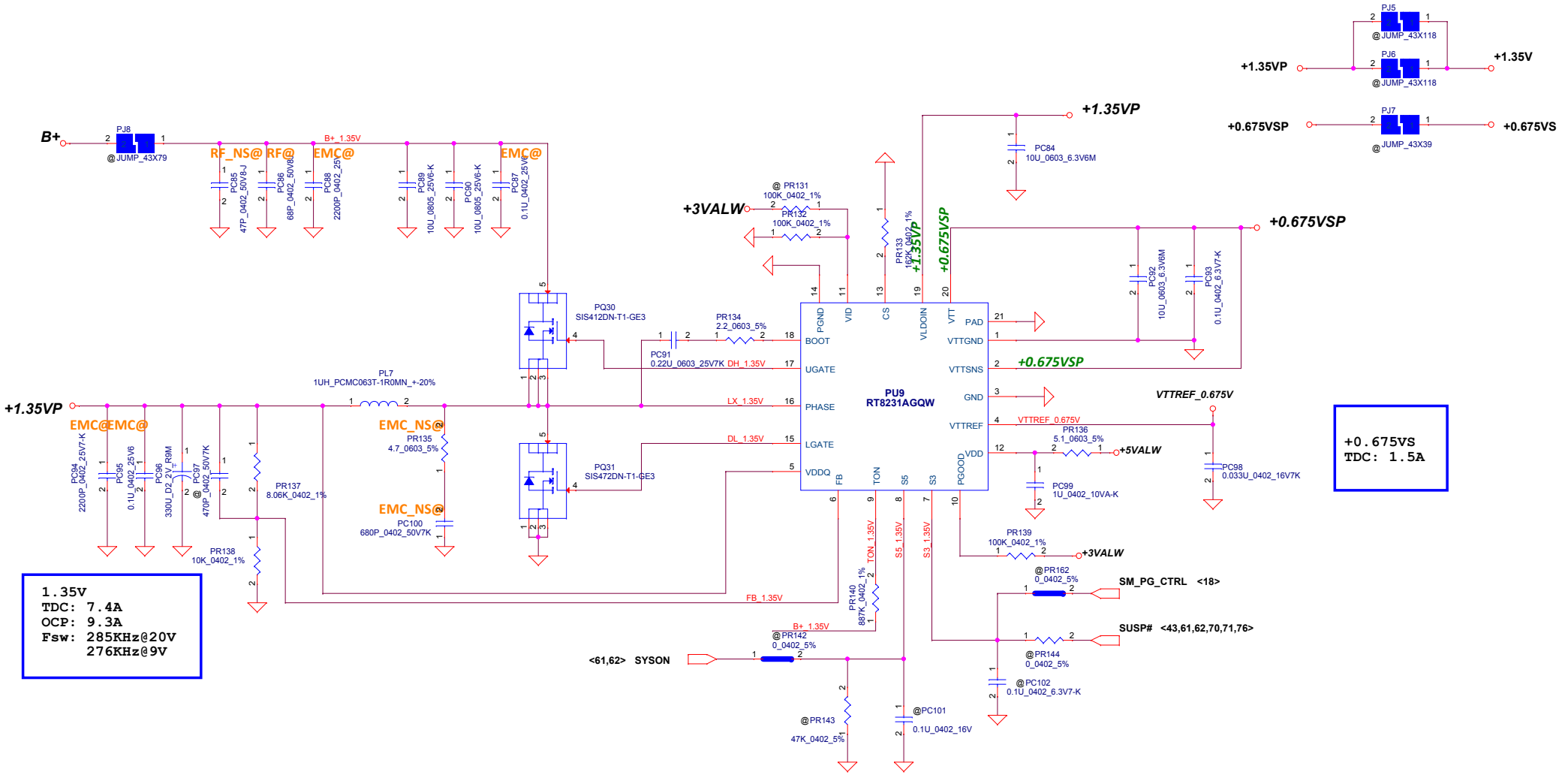

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Title: +1.35V/+0.675VS

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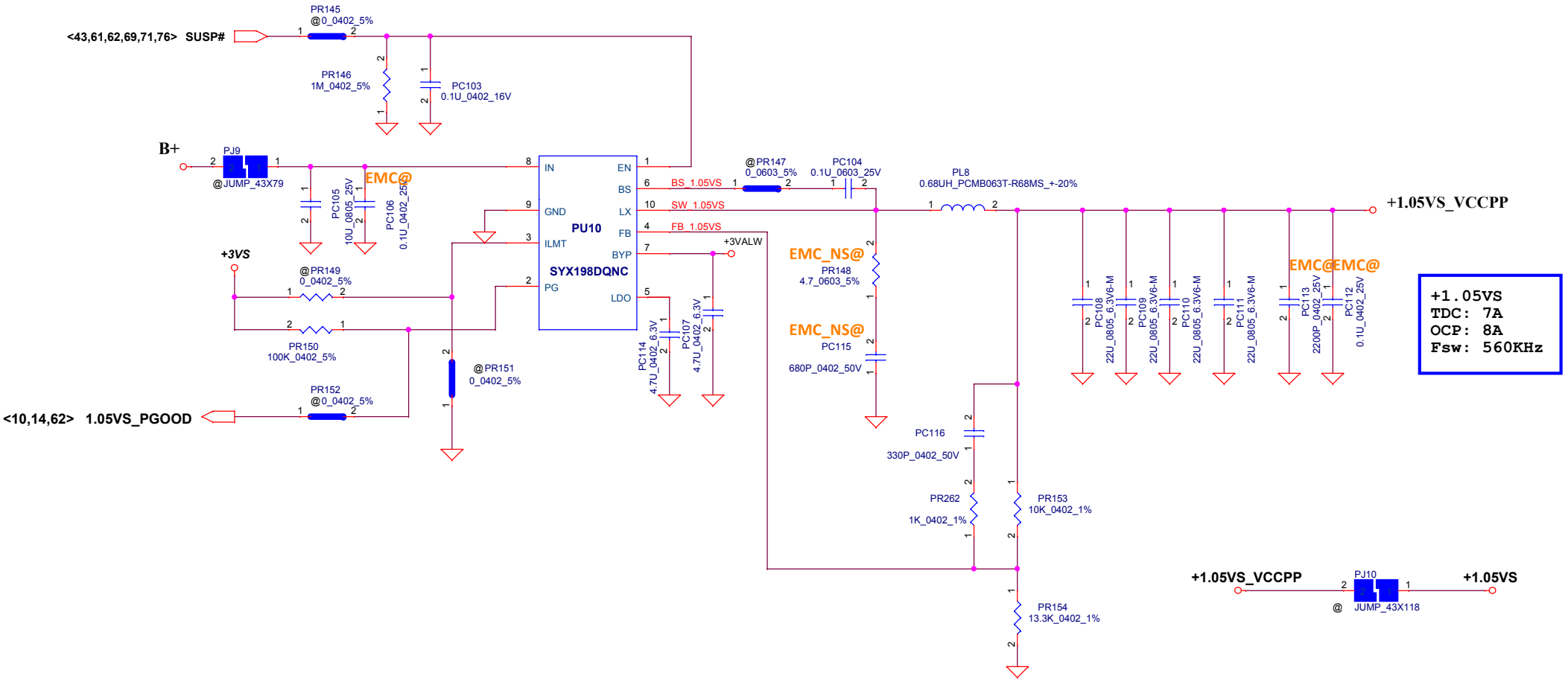

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Title	*+1.05VS*		
Size: B	Document Number: *AITE1 NM-A221*		Rev: 1.0
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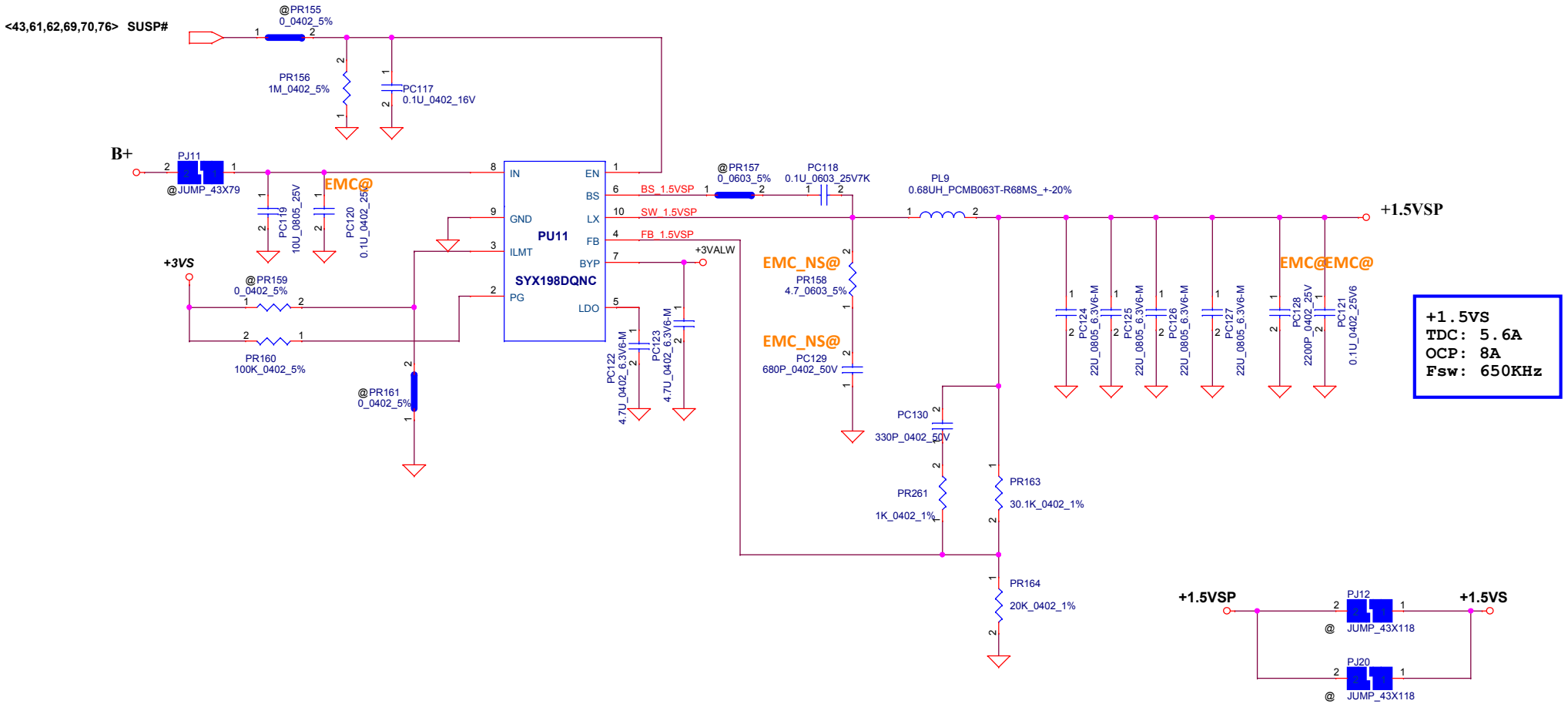

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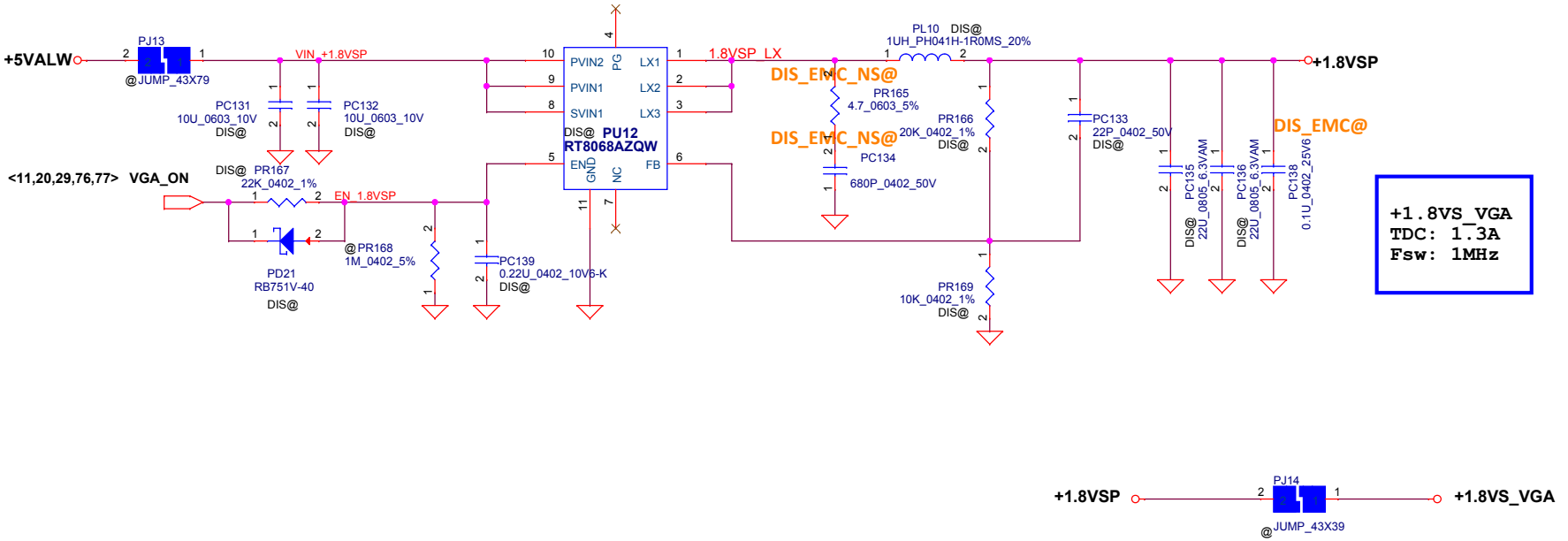
Title	+1.5VS		
Size: B	Document Number: AITE1 NM-A221		Rev: 1.0
Date: Thursday, November 06, 2014	Sheet 71 of 81		



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Title: +1.8VS_VGA

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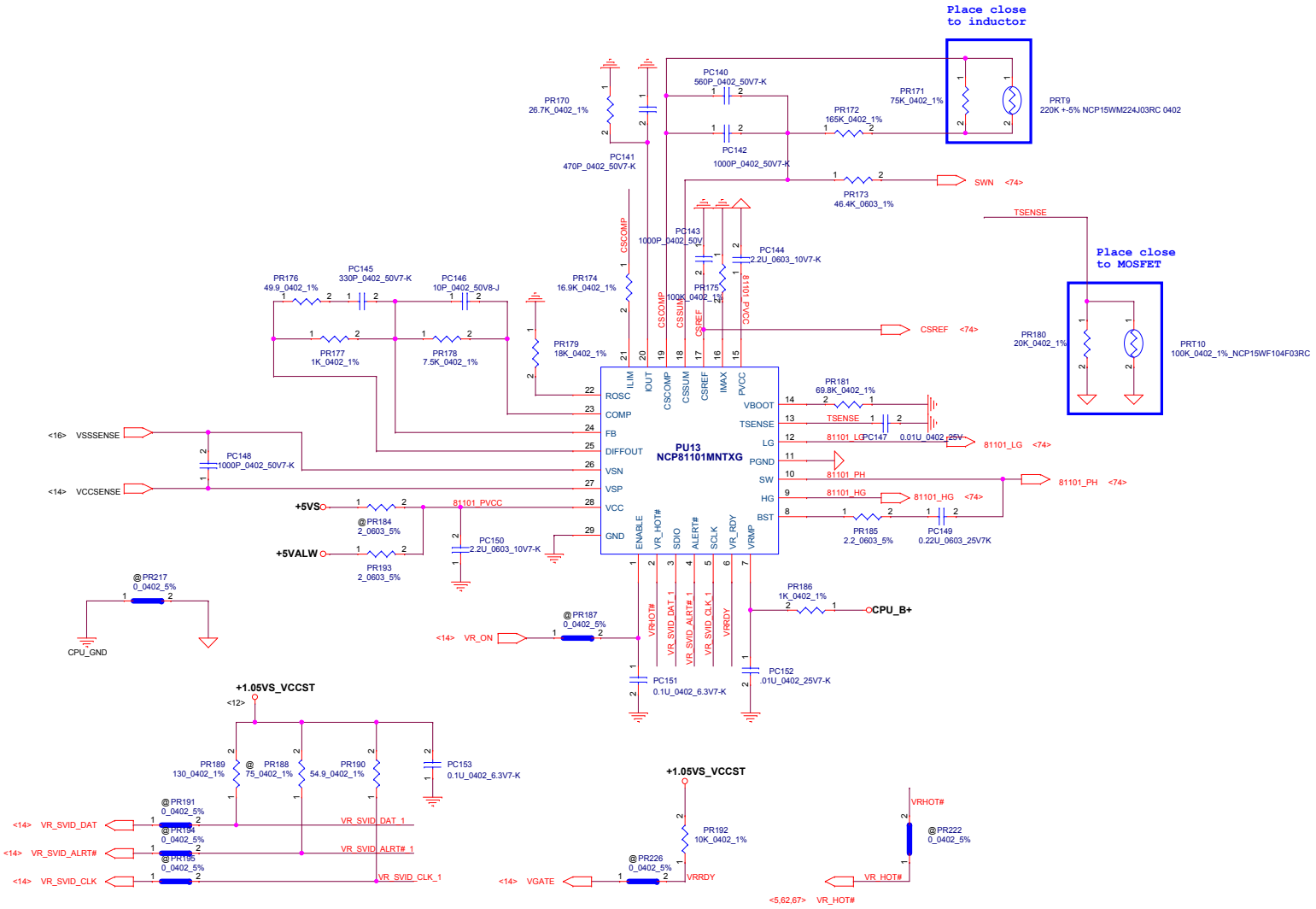

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Title: +CPU_CORE

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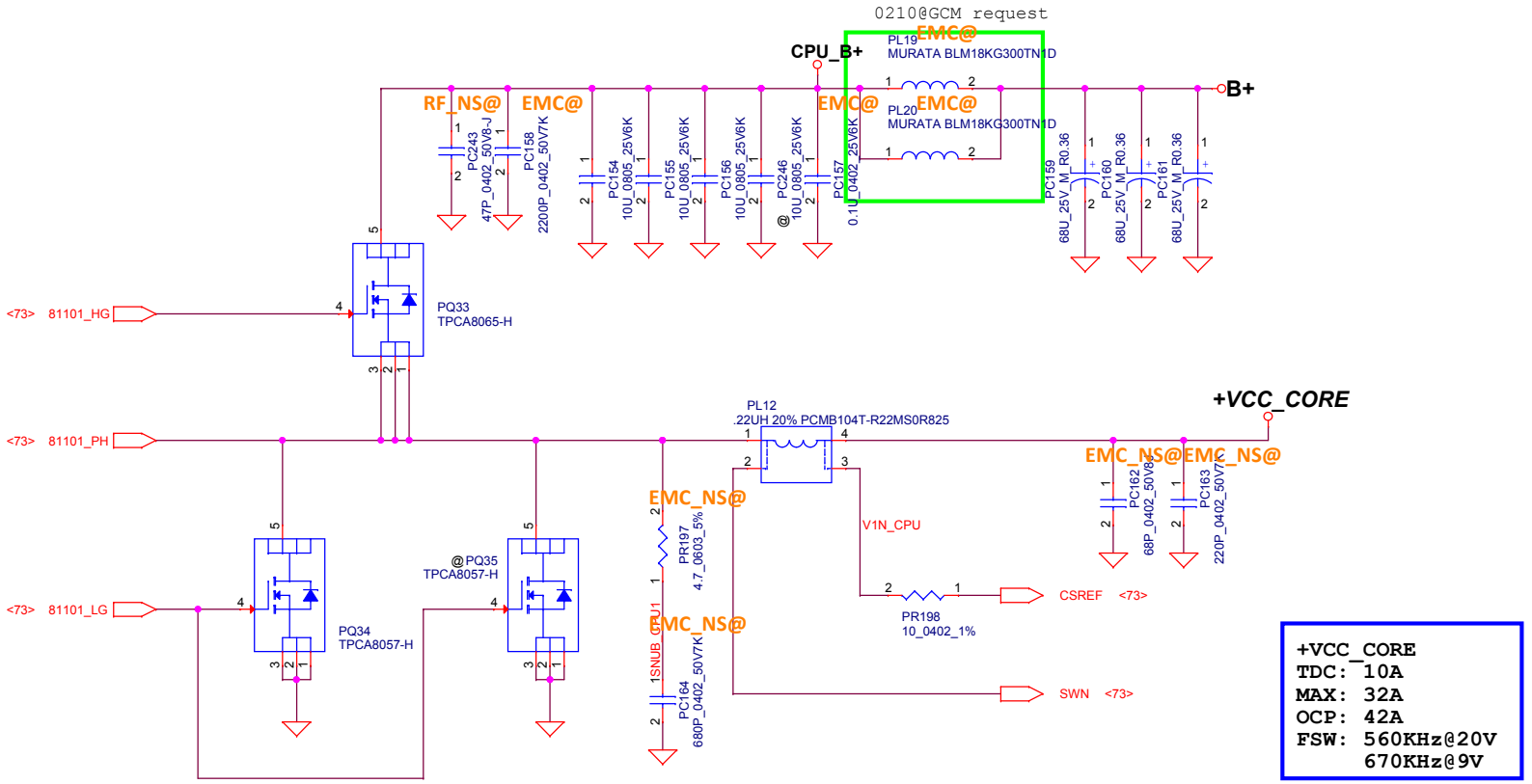

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Title: +CPU_CORE2

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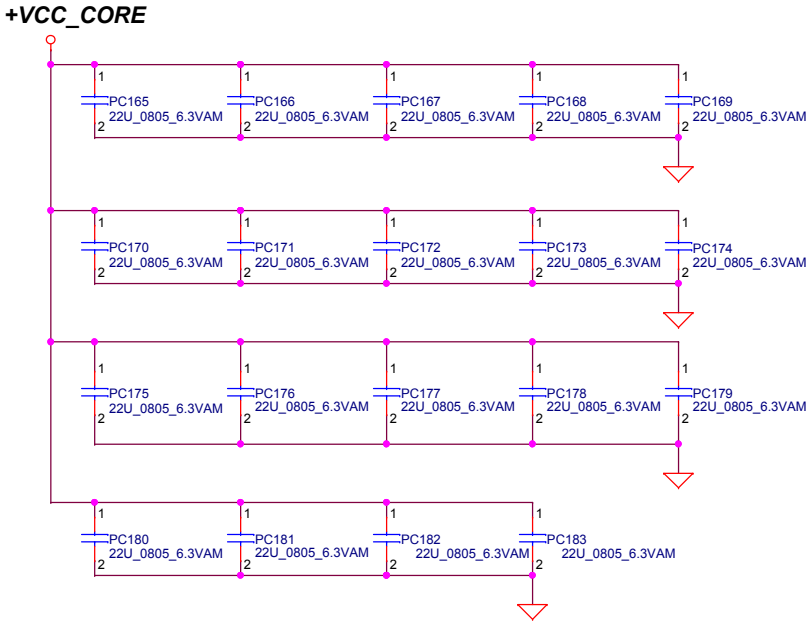
Based on PDDG rev 0.7 Table 5-1.



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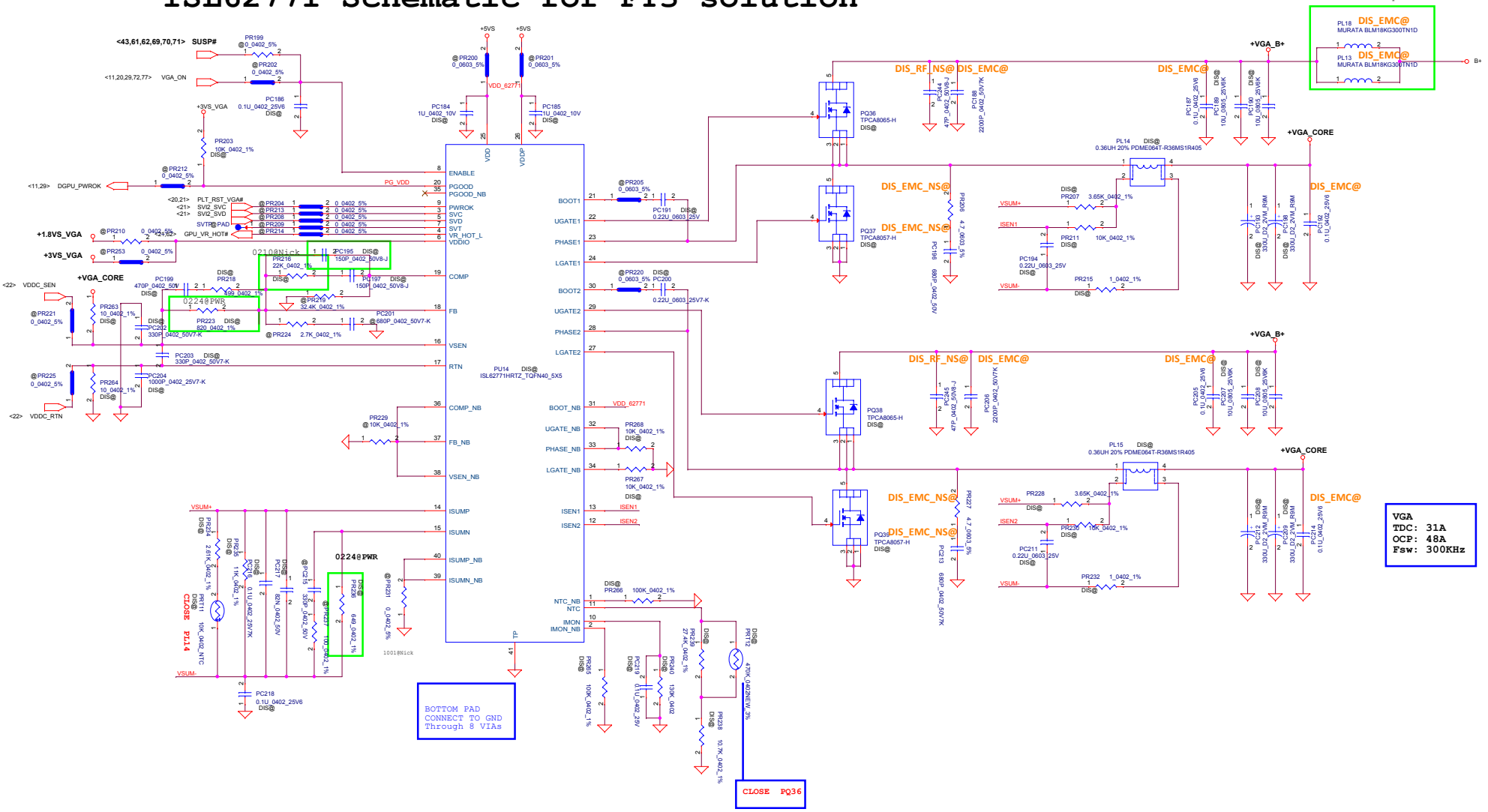
ISL62771 Schematic for FT3 solution



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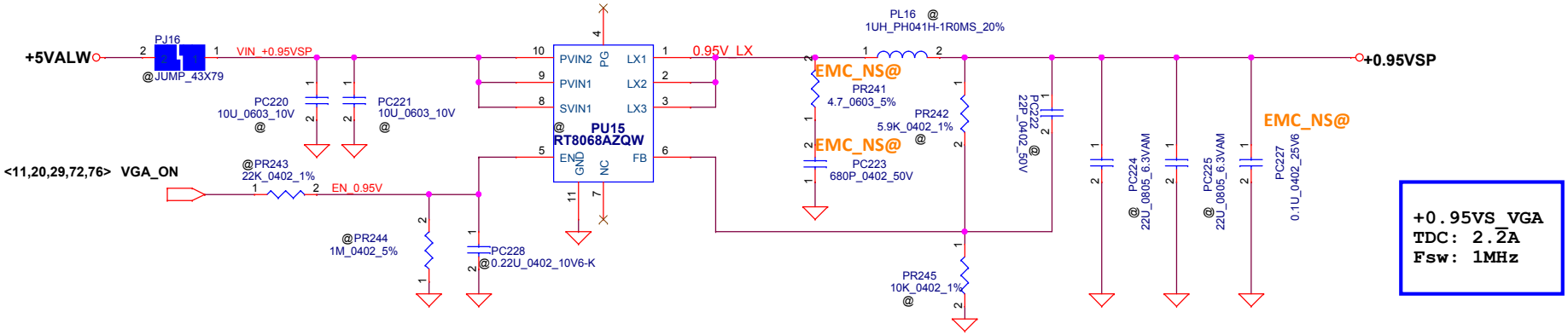

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Title	+0.95VS_VGA		
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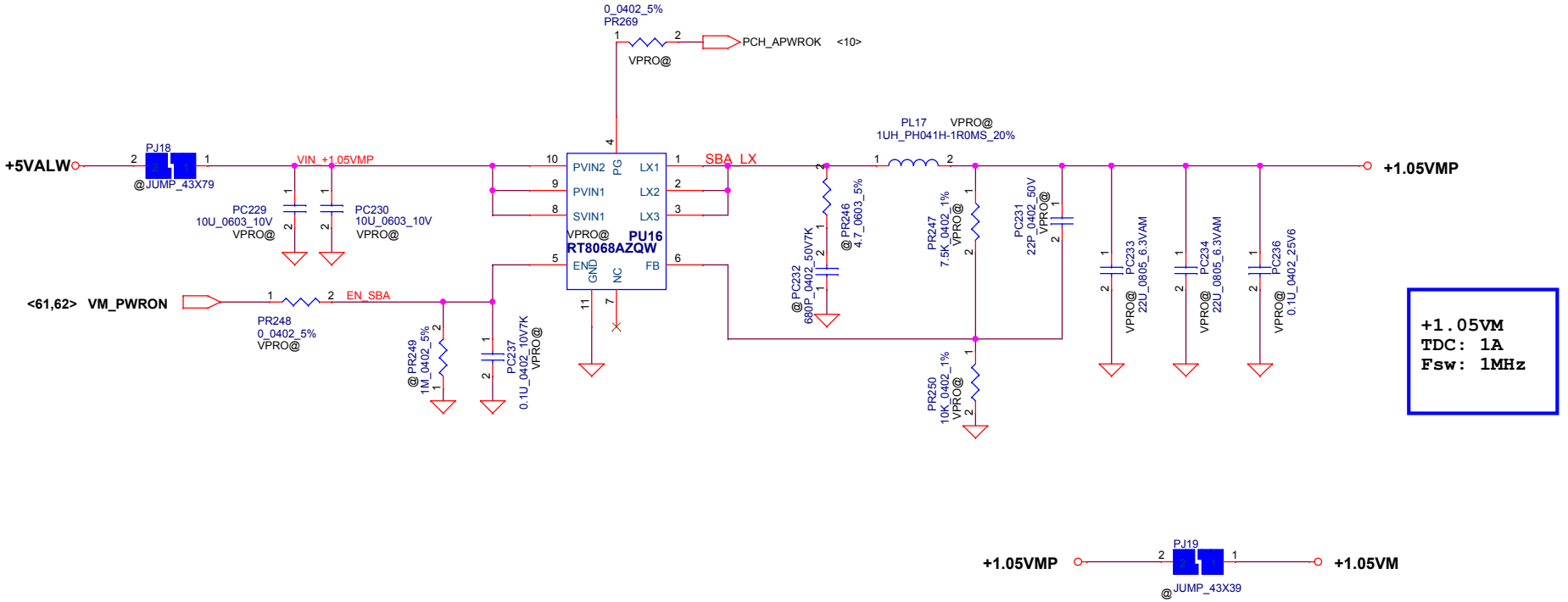

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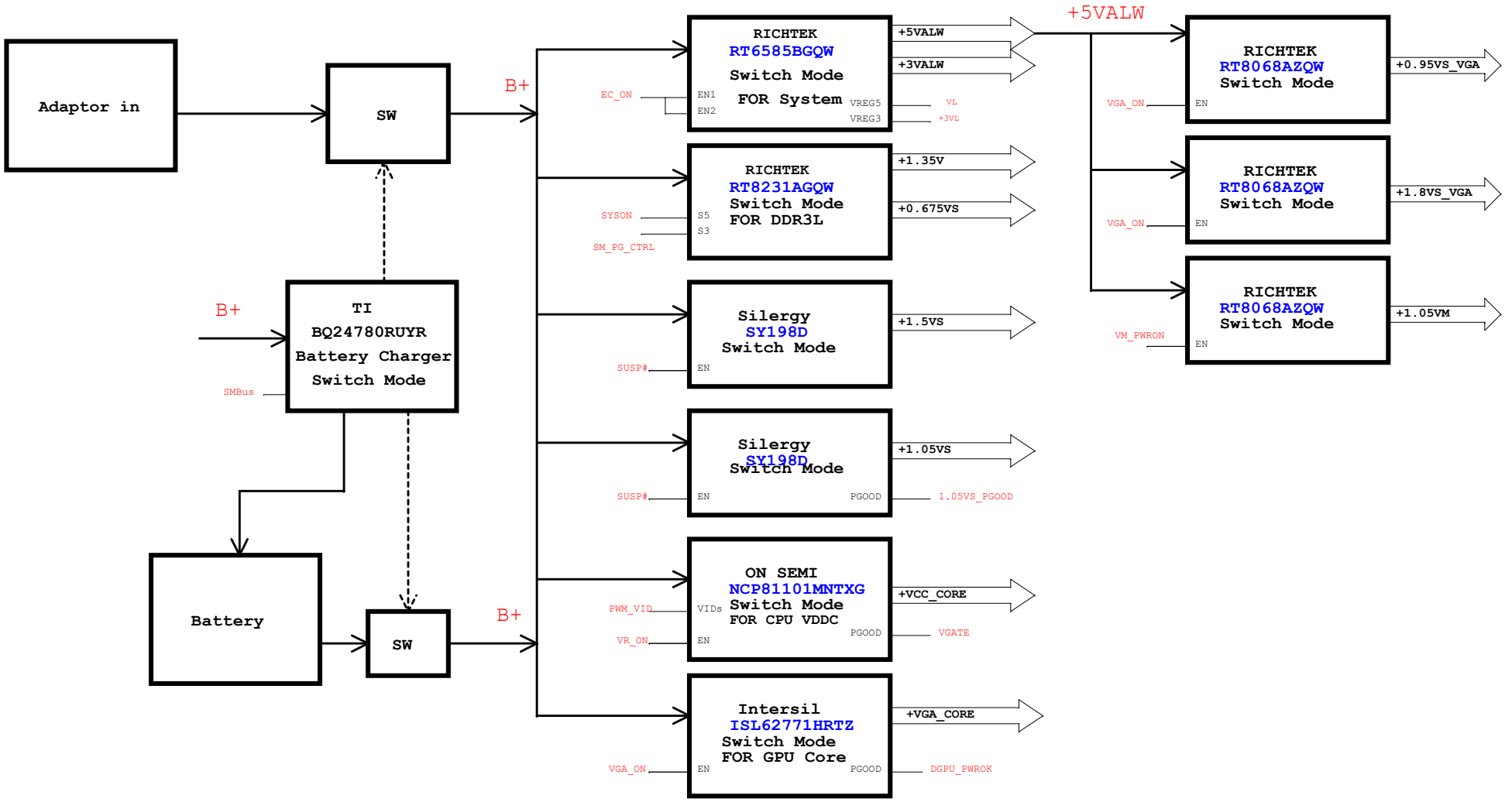
POWER PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/01/16

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE



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Issued Date	2013/08/05	Deciphered Date	2014/12/31

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HW PIR (Product Improve Record)

AIVE1 NM-AXXX SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/10/15

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Gordon SDV LOGIC SCHEMATICS

NMA-221
VER 0.1
Nov/13/2013

1.COVER PAGE
2.BLOCK DIAGRAM
3.NOTE LIST
4.VGA NOTE
5.BDW_DDI/EDP/XDP
6.BDW_DDR3L INT
7.BDW_RTC/HDA/SATA/PCIe/JTAG
8.BDW_CLOCK/PM
9.BDW_LPC/SPI/SM BUS
10.BDW_SYS PM
11.BDW_eDP SBAND/DDPx
12.BDW_GPIO/SIO
13.BDW_PCIE/USB BUS
14.BDW (Power)
15.BDW (Power2)
16.BDW (VSS)
17.BDW (OTHER)
18.DDR3L DIMM1
19.DDR3L DIMM2
20.Opal & Jet PCIE
21.Opal & Jet GPIO
22.Opal & Jet Core Power
23.Opal & Jet DP Power/GND
24.Opal & Jet MEM Interface
25.Opal & Jet DDR3 VRAM U
26.Opal & Jet DDR3 VRAM L
27.Opal 22 TO 24 VRAM U2
28.Opal 23 TO 25 VRAM L2
29.Opal & Jet swich power
30.BLANK
31.BLANK
32.CARDREADER IC/CONN.
33.DP RP --> BLANK
34.DOCKING/ DCIN CONN
35.CX20751
36.HP/MIC JACK/Speaker
37.SATA HDD/ODD CONN.
38.eDP/CMOS CONN.
39.USB30 RP --> BLANK
40.USB3 PORT1-BACK
41.USB3 PORT2-FRONT(AOU)
42.MUX IC
43.DP TO VGA
44.VGA CONN.
45.HDMI RP --> BLANK
46.HDMI CONN.
47.GBE LAN PHY
48.RJ45 CONN.
49.CP/TPOINTCONN.
50.PBTN/LID/FP/FAN CONN.
51.KB/RTC/TOUCH PAN CONN.
52.WWAN/WLAN NGFF CONN.
53.SUB CONN. --> BLANK
54.SUB-AUDIO JACK CONN.
55.THERMAL SENSOR
56.G SENSOR/TPM
57.BLANK
58.BLANK
59.BLANK
60.BLANK
61.DC V TO VS/ V-PCH/VM
62.EC_IT8586E/FX
63.PLM/SCREW HOLE
64.BLANK
65.DCIN / Vin Detector
66.BATTERY CONN/OTP
67.CHARGER(BQ24780)
68.3V/5VALW(RT6585B)
69.+1.35V/+0.675V(RT8231A)
70.+1.05VS(SYX198DQNC)
71.+1.5VS(SYX198DQNC)
72.+1.8VS_VGA(RT8068A)
73.+VCC_CORE(NCP81101MNTXG)
74.+VCC_CORE2
75.PROCESSOR DECOUPLING
76.+VGA_CORE(ISL62771)
77.+0.95VS_VGA(RT8068A)
78.+1.05VM(RT8068A)
79.PWR-PIR
80.HW PIR

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