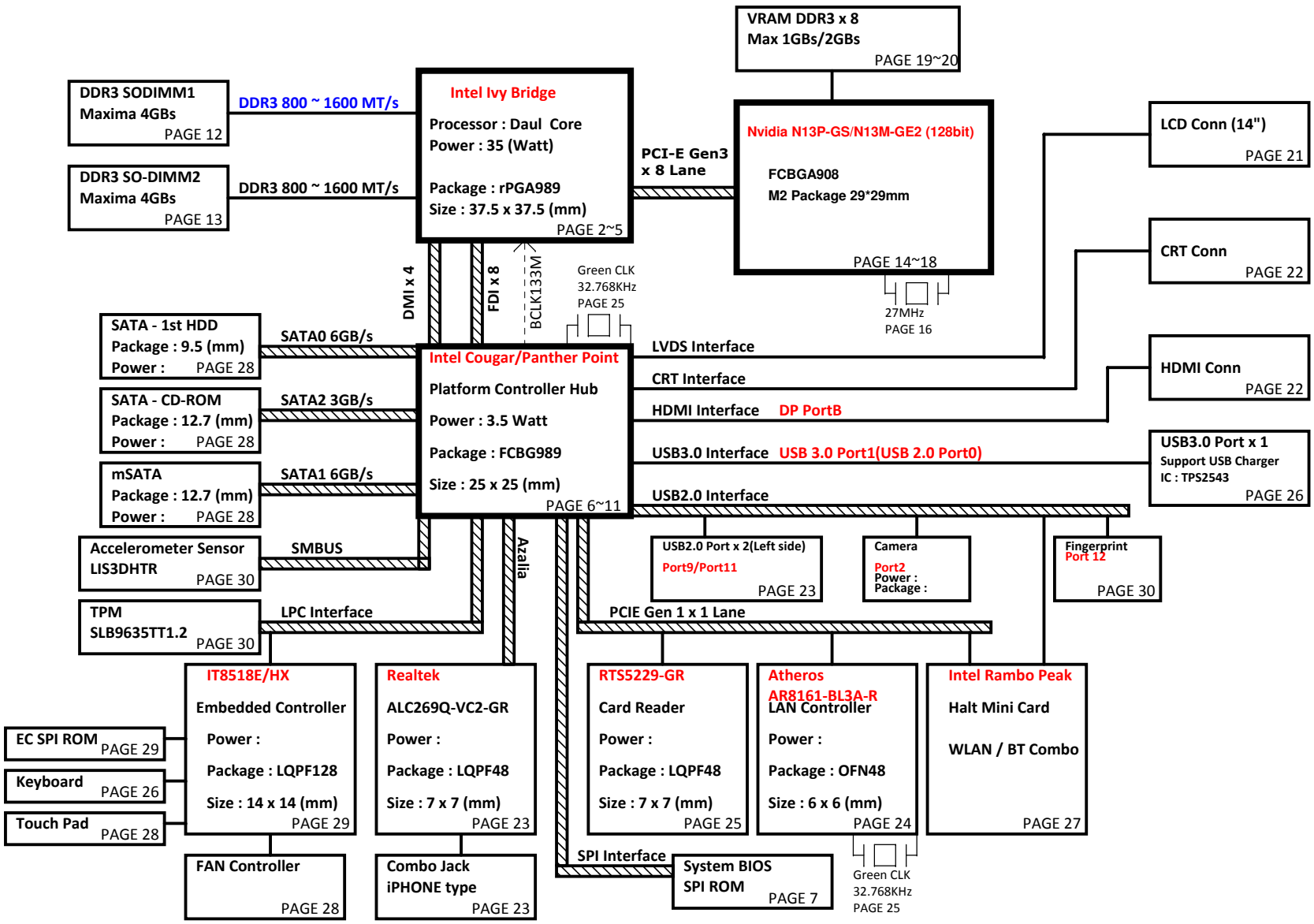
JW3/4 DIS/UMA (14") Slim
Intel Chief River Platform Block Diagram

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT
SMT

Power Source

O2Micro OZ8681
System Charge Power (+BATCHG)

P2806
System Discharge Power (+1.5V/+3V/+5V)

Ricktek RT8205
System Power (+3VPCU/+5VPCU/ +3VS5/+5VS5)

NCP6132/NCP5911/RT8209/G9334
Processor Power (+VCC_CORE/ +1.05_VTT/+VCCSA)

Richtek RT8207
System Memory Power (+1.5VSUS/ +0.75V_DDR_VTT)

Richtek RT8209/RT9025
PCH Power (+1.05/+1.8V)

O2Micro OZ8122
DGPU Power (+VGACORE/+3.3V_GFX/ +1.8_VGA/+1.5_GFX/+1.05_GFX)

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
A3	Block Diagram	A

Date: Tuesday, March 27, 2012 Sheet 1 of 42

Ivy Bridge Processor (DMI,PEG,FDI)

CPU Type (Reversed Version)

Footprint: pz98927-364r-01f-socket
CPU BKT P/N: FBSTD266010

02

PEG_COMP connect to PIN G3&G4 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.

H=4.5mm ? DGG^9000022 (3A)
H=4.7mm ? DGG^9000024 (3A)

U16A

DMI
Intel(R) FDI
PCI EXPRESS* - GRAPHICS
eDP

Ivy Bridge_rPGA_2DPC_Rev0p61

U16B

MISC
THERMAL
PWR MANAGEMENT
CLOCKS
DDR3 MISC
JTAG & BPM

Ivy Bridge_rPGA_2DPC_Rev0p61

Placement close to EC.

PEG x8

CPU RESET#

20110816 modify:
REGULATOR DEL FOR SHORT

Processor pull-up (CPU)

DDR3 DRAM RESET

SM_DRAMPWROK
Processor Input.

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

For iFDIM Trigger Point

Connect a Test Point on BPM# 6 signal, very close to processor.

Connect a Test Point on BPM# 7 signal, very close to processor.

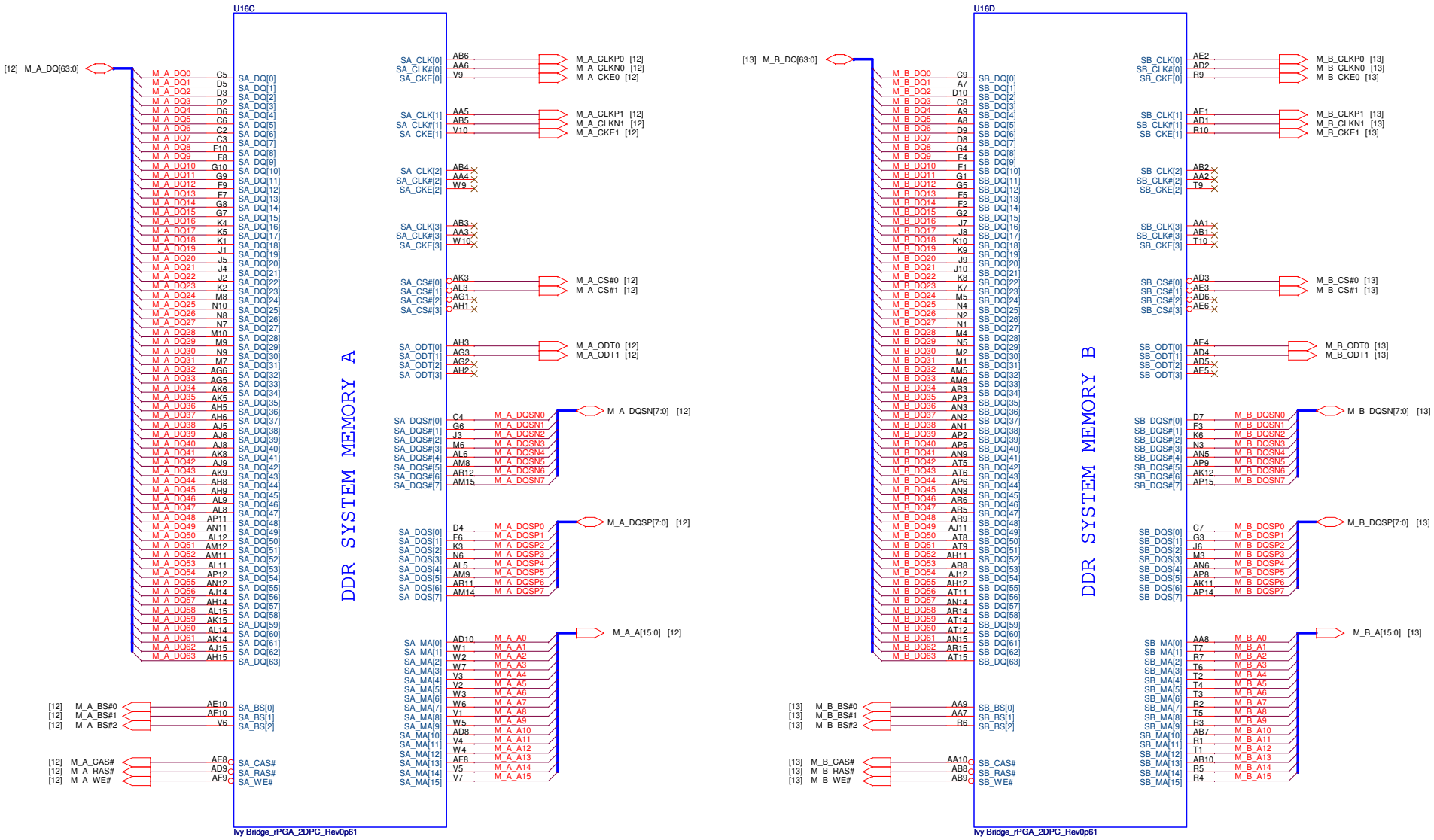
NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Processor 1/4 (Host/GPU)	A

Date: Tuesday, March 27, 2012 Sheet 2 of 42

Ivy Bridge Processor (DDR3)



NB5	PROJECT :JW3/4 (Chief River) Quanta Computer Inc.	
Size: Custom	Document Number: Processor 2/4 (DDR3 I/F)	Rev: A
Date: Tuesday, March 27, 2012	Sheet 3 of 42	

POWER

U16F

IVB:55A

+VCC_CORE

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

CORE SUPPLY

PEG AND DDR

SNB: 8.5A

+1.05V

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

SVID

VIDALERT#
VIDSCLK
VIDSOUT

H_CPU_SVIDALRT#
VR_SVID_CLK
VR_SVID_DATA

SENSE LINES

VCC_SENSE
VSS_SENSE

VCCIO_SENSE
VSS_SENSE_VCCIO

R50 100/F_4 +VCC_CORE
VCC_SENSE [39]
VSS_SENSE [39]
R49 100/F_4

R446 10/F_4 +1.05V
VCCP_SENSE [35]
VSSP_SENSE [35]
R443 10/F_4

100- ±1% pull-up to VCC near processor.

R91,R98,R109 close to CPU

Zo impedance: 27.4ohm

Zo impedance: 27.4ohm

+1.05V
R74 130/F_4
C201 0.1U/10V_4
R75 75/F_4
R67 43_4
VR_SVID_ALERT# [39]
VR_SVID_CLK [39]
VR_SVID_DATA [39]

Ivy Bridge_rPGA_2DPC_Rev0p61

POWER

U16G

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

SNB: 21.5A

+VCC_GFX

GRAPHICS

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

SENSE LINES

VAXG_SENSE
VSSAXG_SENSE

R53 100/F_4 +VCC_GFX
VCC_AXG_SENSE [39]
VSS_AXG_SENSE [39]
R52 100/F_4

VREF

SM_VREF
SA_DIMM_VREFDQ
SB_DIMM_VREFDQ

+VDDR_REF_CPU
+VDDR_REF_CPU and DDR_VTTREF must use 10mils width
C248 0.1U/10V_4
Q12 ME2N7002D
DDR_VTTREF [12,13,33]
R118 3.3K/F_4 MAIND [41]

R456 *1K/F_4
SMDDR_VREF_DQ0_M3 [12]
SMDDR_VREF_DQ1_M3 [13]
20mils width
C273 470P/50V_4
R458 *1K/F_4

DDR3 -1.5V RAILS

IVB: 5A

+1.5V_CPU

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15

C249 10U/6.3V_6
C247 10U/6.3V_6
C49 10U/6.3V_6
C246 10U/6.3V_6
C259 10U/6.3V_6
C250 10U/6.3V_6

SA RAIL

IVB: 6A

+VCCSA

VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8

C189 10U/6.3V_6
C177 10U/6.3V_6
C196 10U/6.3V_6
C200 10U/6.3V_6

330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

1.8V RAIL

+1.8V

IVB: 1.5A

VCCPLL1
VCCPLL2
VCCPLL3

C671 1U/6.3V_4
C670 1U/6.3V_4
C672 10U/6.3V_6

330uF x1, 10uF_8 x1, 1uF_4 x2 Socket BOT edge.

MISC

VCCSA_SENSE
VCCSA_VID[0]
VCCSA_VID[1]
VCCIO_SEL

R77 *100/F_4 +VCCSA
VCCUSA_SENSE [34]
R68 10K_4
VCCSA_SEL0 [34]
VCCSA_SEL [34]
R71 10K_4

Zo:55 ohm

+1.5VSUS

Q13 AON7410
MAIND
C276 *470P/50V_4

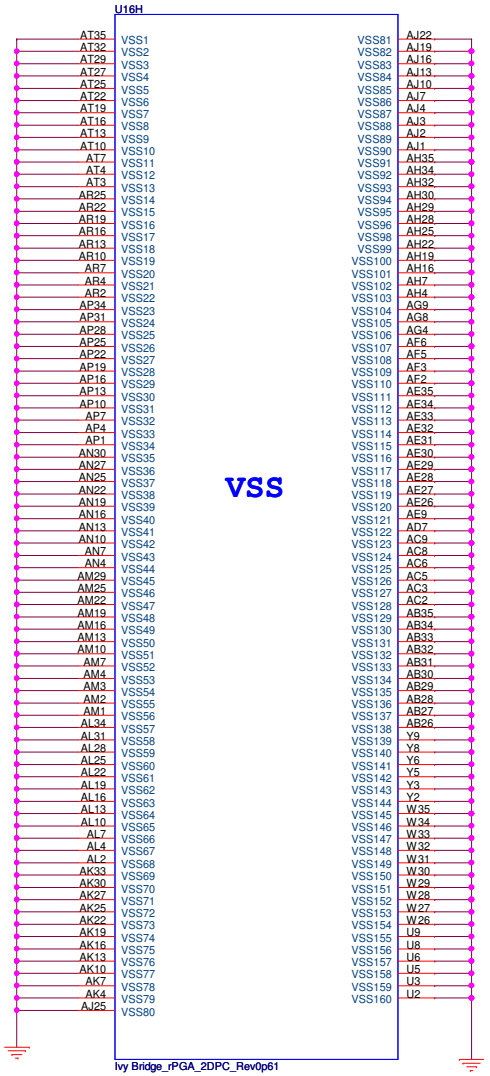
+1.5V_CPU

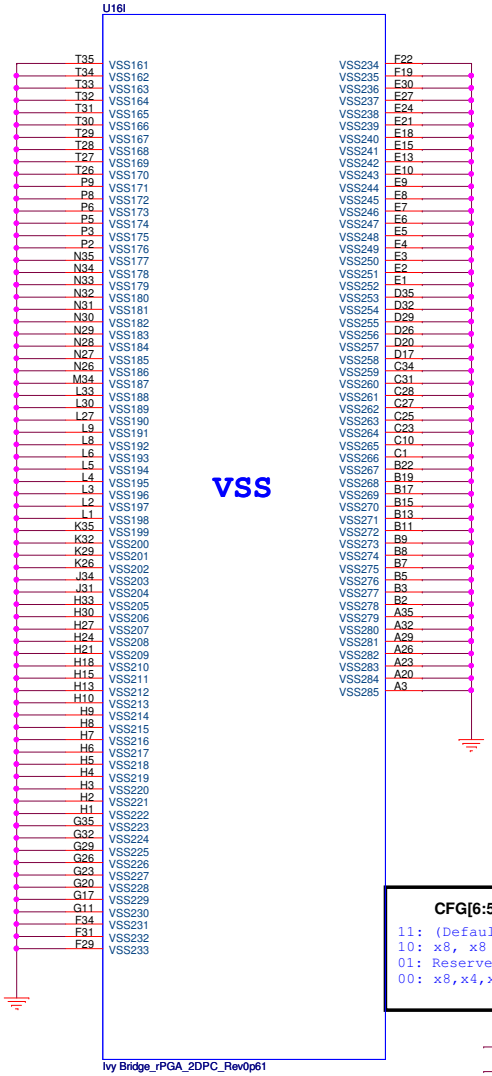
R100 220_8
Q11 ME2N7002D
MAIN_ONG [2,41]

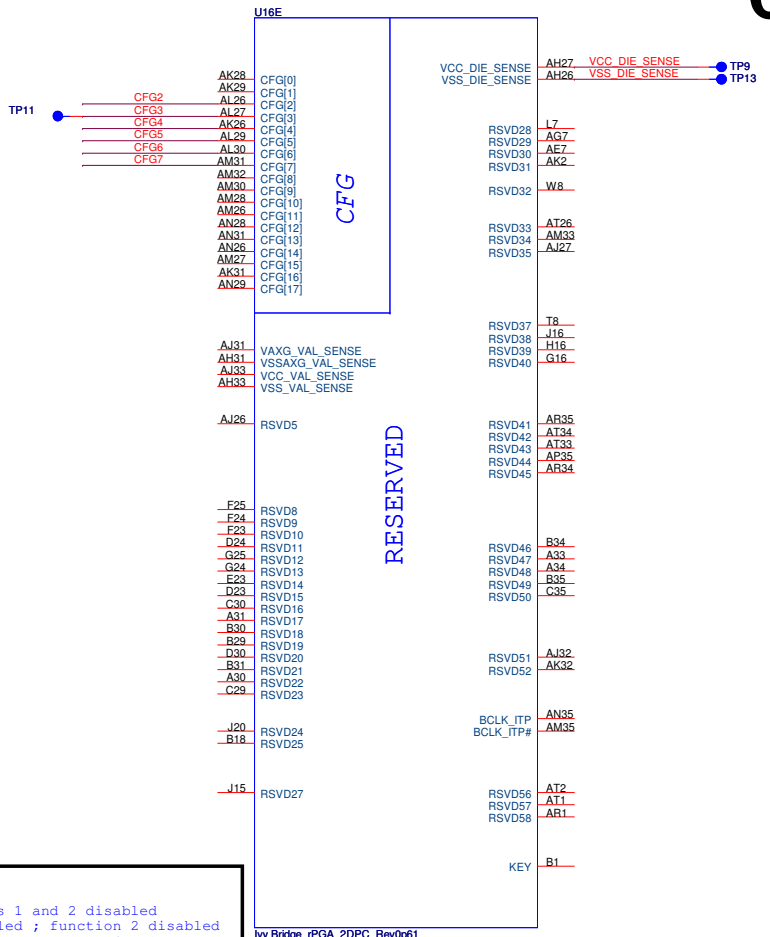
C285 0.1U/10V_4
C286 0.1U/10V_4
C284 0.1U/10V_4
C283 0.1U/10V_4

Ivy Bridge_rPGA_2DPC_Rev0p61

NB5	PROJECT : JW3/4 (Chief River) Quanta Computer Inc.		
Size Custom	Document Number Processor 3/4 (POWER)		Rev A
Date: Tuesday, March 27, 2012	Sheet 4 of 42		

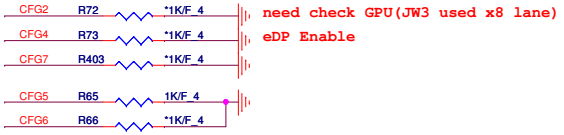






CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

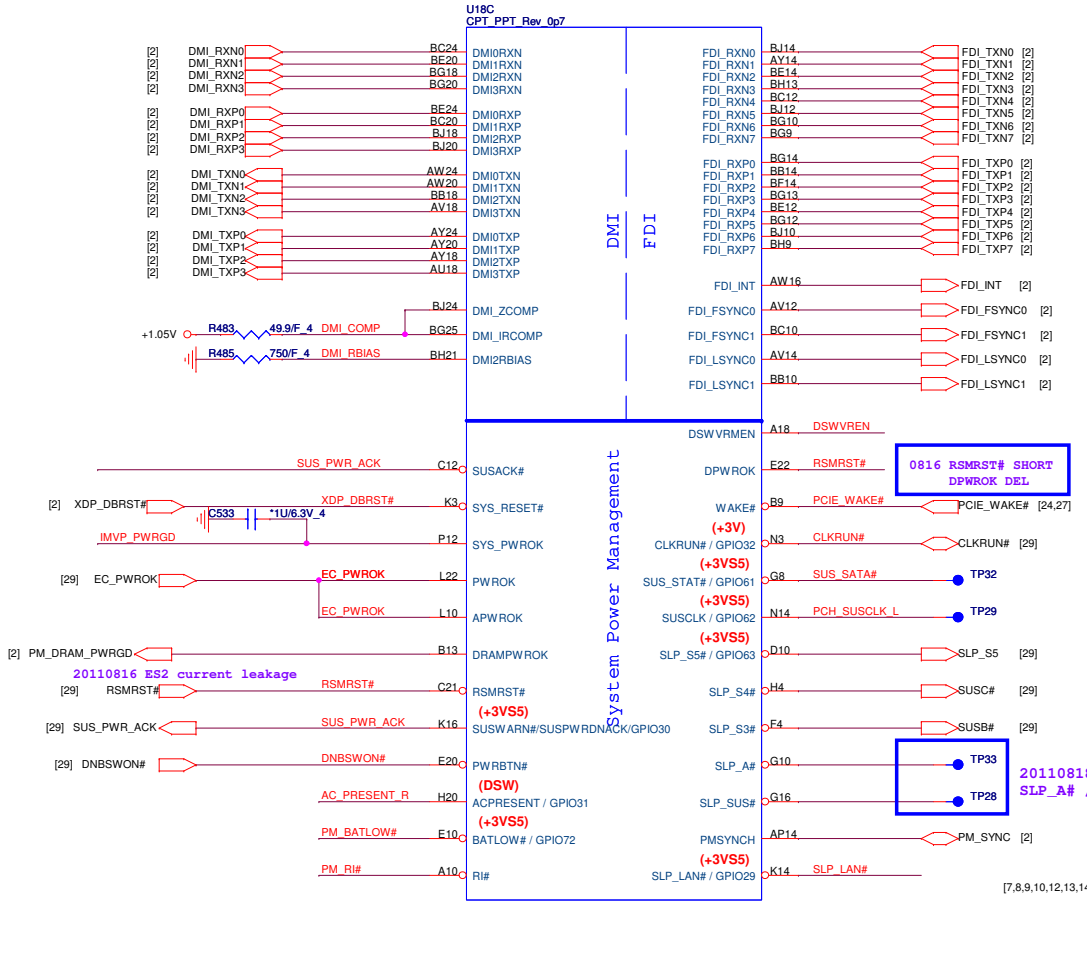
	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal.)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

NB5

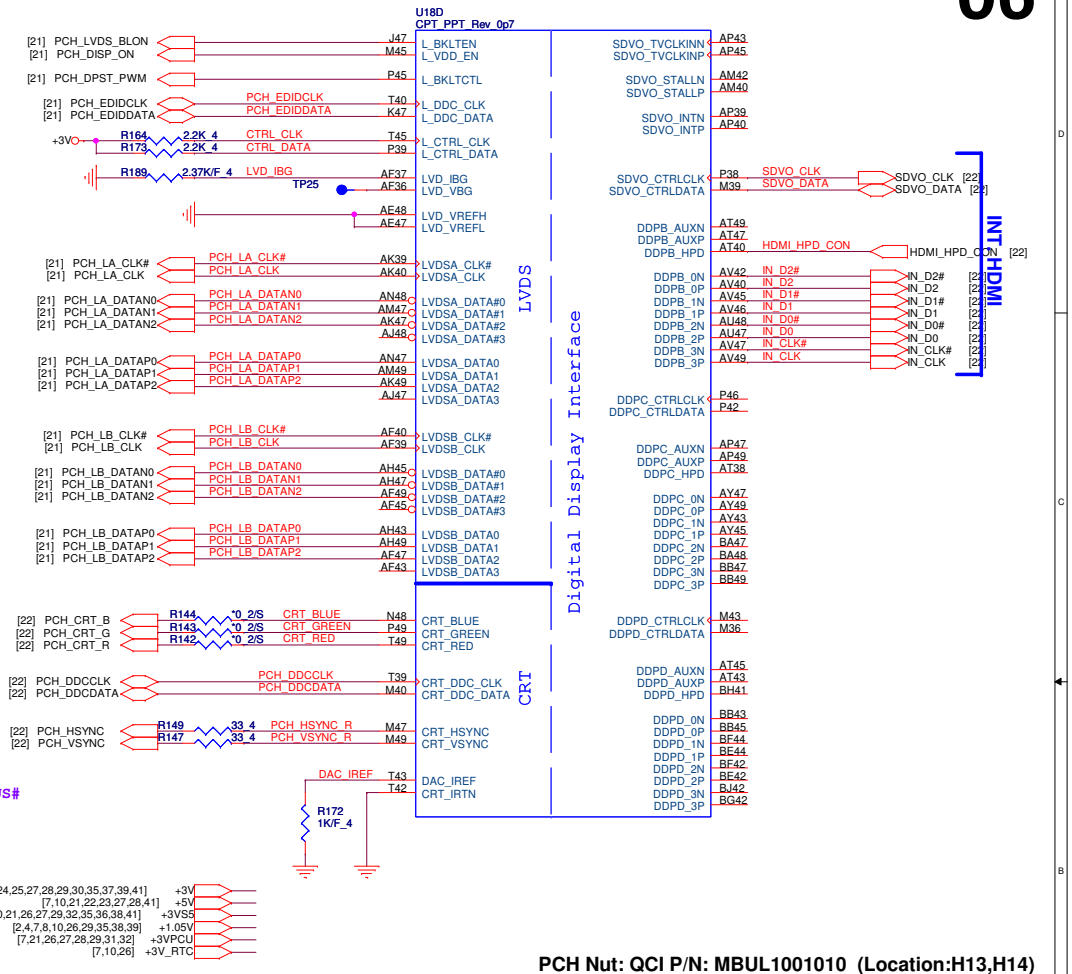
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Processor 4/4 (RSV,Ground)	A
Date: Tuesday, March 27, 2012	Sheet 5 of 42	

Cougar Point/Panther Point (DMI,FDI,PM)



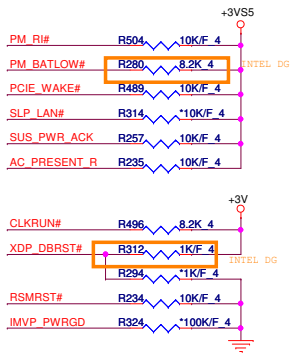
Cougar Point/Panther Point (LVDS,DDI)



[7,8,9,10,12,13,14,18,21,22,23,24,25,27,28,29,30,35,37,39,41] +3V
[7,10,21,22,23,27,28,41] +5V
[7,8,9,10,21,26,27,29,32,35,36,38,41] +3VS5
[2,4,7,8,10,26,29,35,38,39] +1.05V
[7,21,26,27,28,29,31,32] +3VPCU
[7,10,26] +3V_RTC

PCH Nut: QCI P/N: MBUL1001010 (Location:H13,H14)

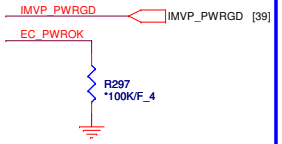
PCH Pull-high/low(CLG)



PD Res place close to PCH

PCH to Res routeing 50 ohm Impedance.
Res to connector filter routeing 37.5ohm Impedance.

System PWR_OK(CLG)



On Die DSW VR Enable
High = Enable (Default) Low = Disable

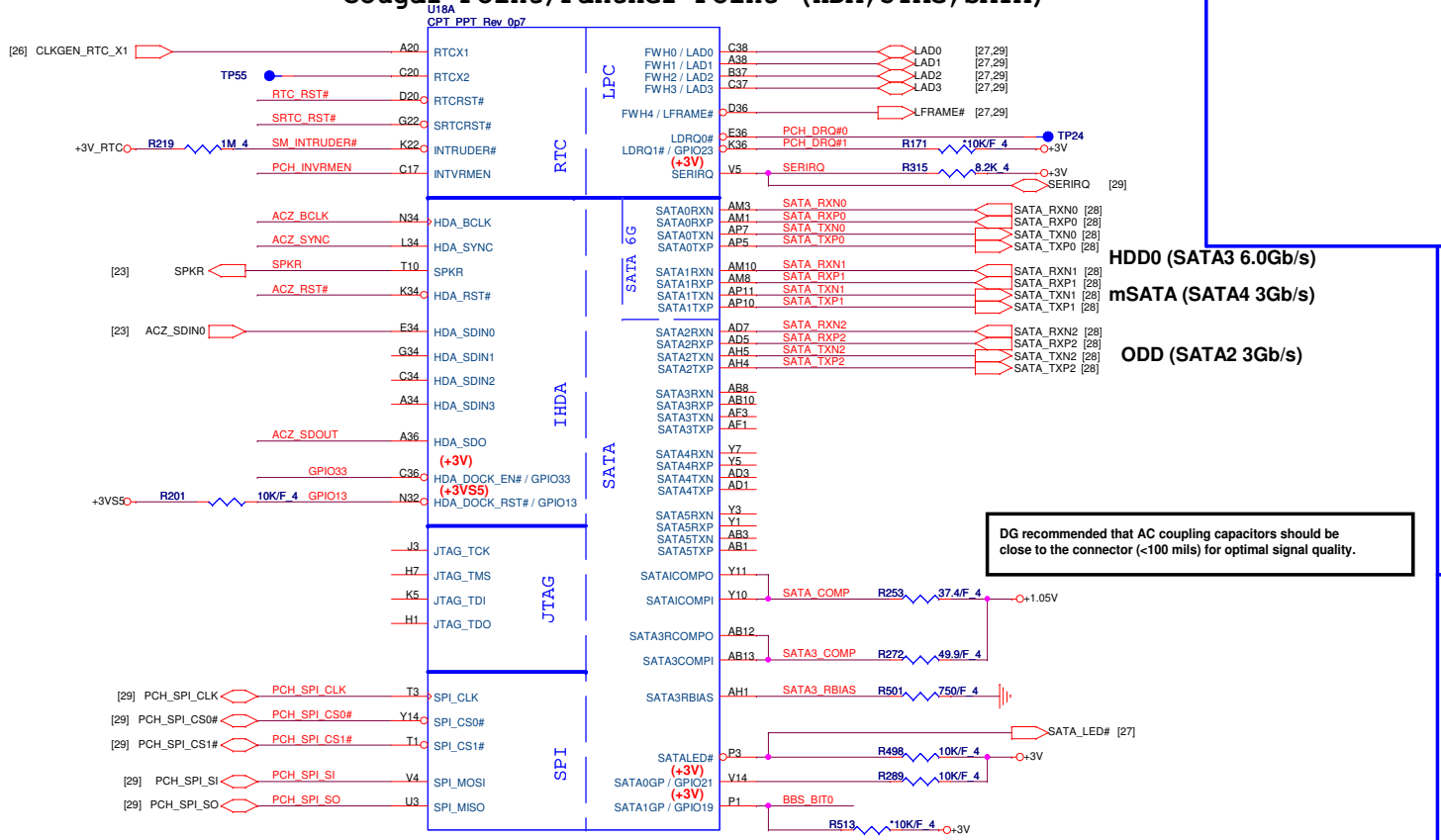
NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (Host/Display)	A
Date: Tuesday, March 27, 2012	Sheet 6 of 42	

06

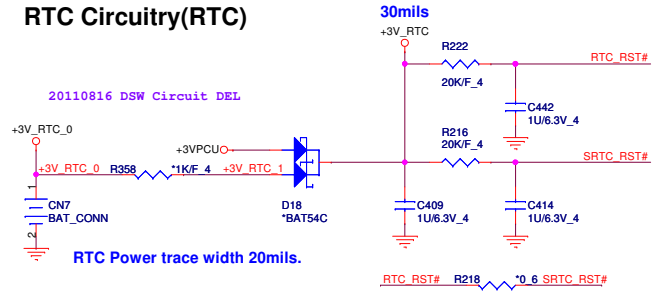
Cougar Point/Panther Point (HDA, JTAG, SATA)



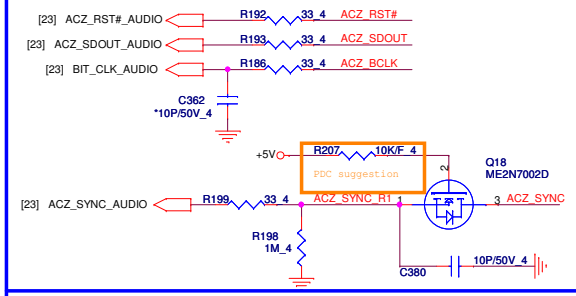
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI; 1 / 0 / LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

RTC Circuitry(RTC)

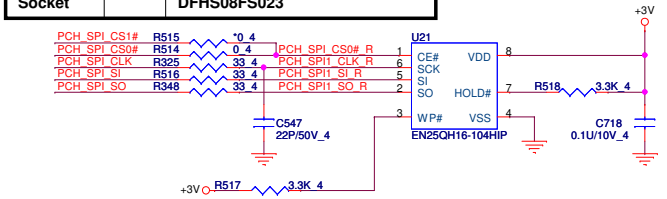


HDA Bus(CLG)



PCH SPI ROM(CLG)

Vender	Size	P/N
EON	2MB	AKE38ZN0Q00 (EN25QH16-104HIP)
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
Socket		DFHS08FS023



+3V [6,8,9,10,12,13,14,18,21,22,23,24,25,27,28,29,30,35,37,39,41]
+5V [10,21,22,23,27,28,41]
+1.8V [4,10,36]
+1.05V [2,4,6,8,10,26,29,35,38,39]
+3VS5 [6,8,9,10,21,26,27,29,32,35,36,38,41]
+3VPCU [21,26,27,28,29,31,32]
+3V_RTC [6,10,26]

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

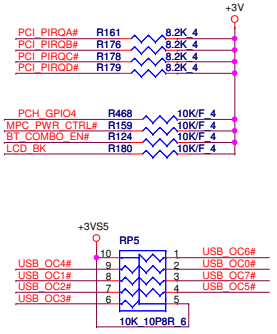
Size	Document Number	Rev
Custom	PCH 2/6 (HDA/RTC/SATA/SPI)	A
Date: Tuesday, March 27, 2012	Sheet 7 of 42	

Cougar Point-M/Panther Point (PCI,USB,NVRAM)

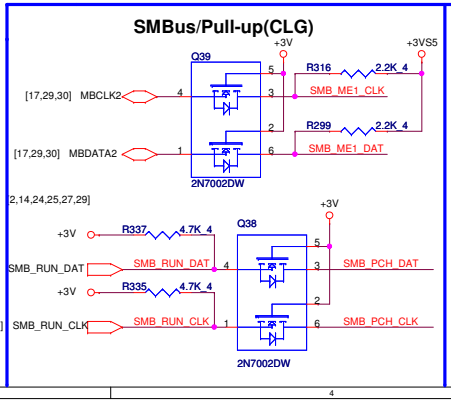
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

08

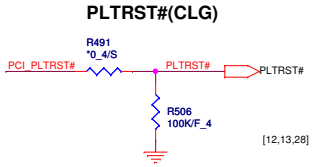
PCI/USBOC# Pull-up(CLG)



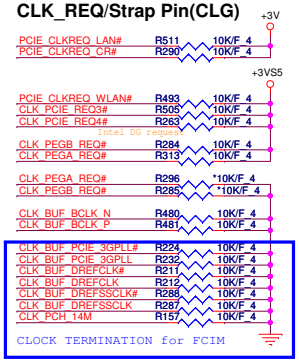
SMBus/Pull-up(CLG)



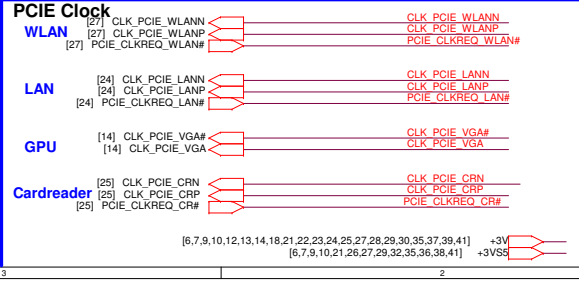
PLTRST#(CLG)



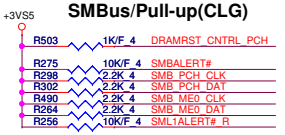
CLK_REQ/Strap Pin(CLG)



PCIE Clock



SMBus/Pull-up(CLG)



MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R160 *1K/F_4

USB3.0

[26] USB30_RX1-
[26] USB30_RX1+
[26] USB30_TX1-
[26] USB30_TX1+

20111130 Modify USB3.0 for HM70

USB2.0 R_down / WLAN / USB2.0 R_up / FP

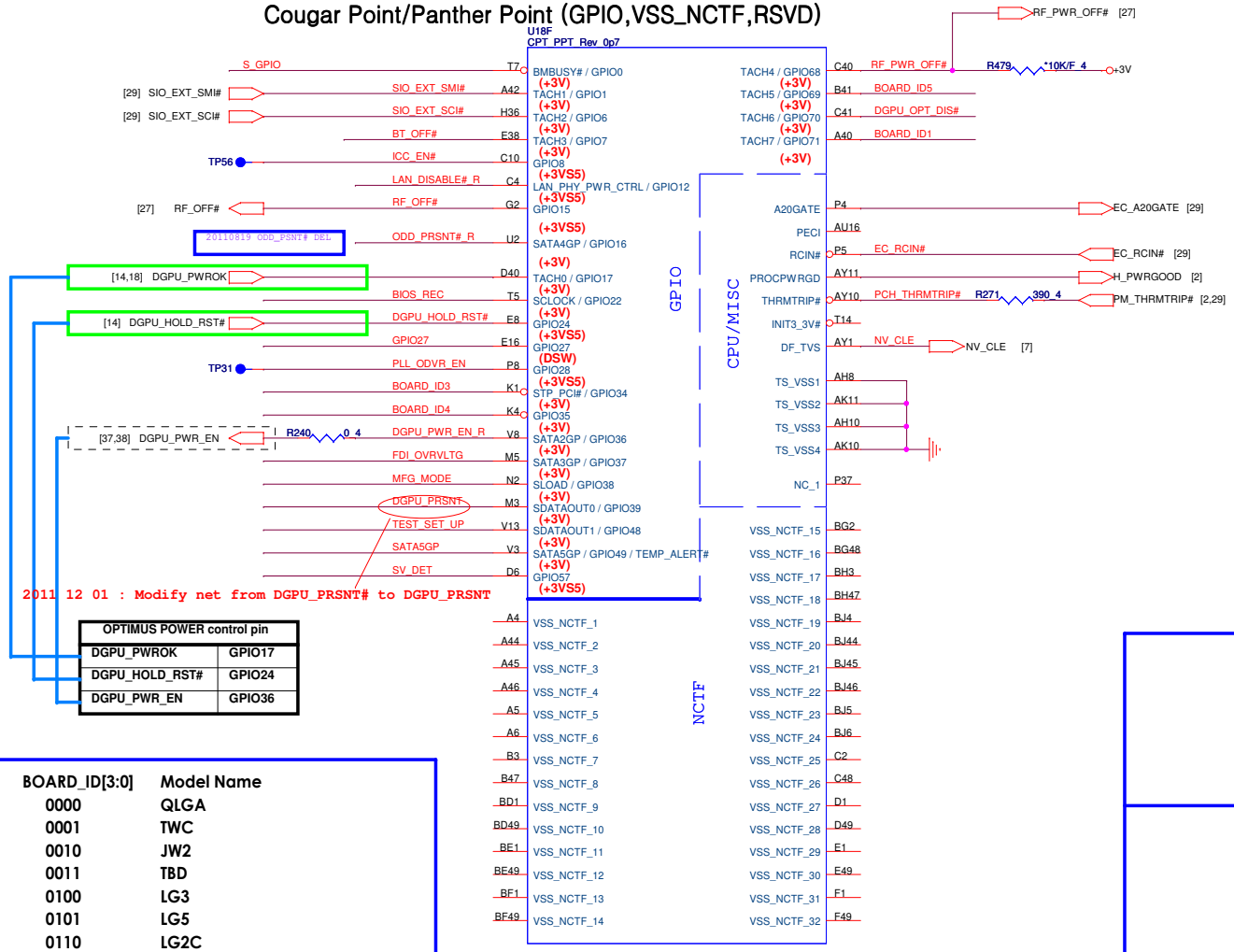
Camera

WLAN / LAN / Cardreader

EMI(near PCH)

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.
NB5
Size: Custom
Document Number: PCH 3/6 (Clock/PCI/PCIE/USB)
Rev: A
Date: Tuesday, March 27, 2012
Sheet 8 of 42

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



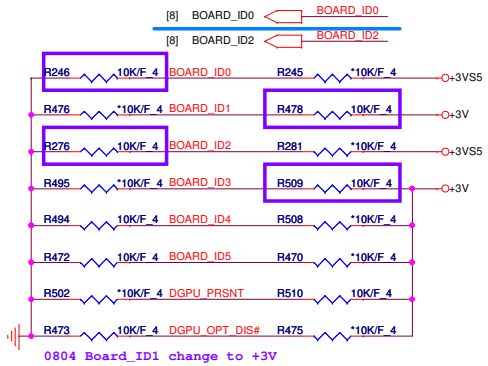
OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

BOARD_ID[3:0]	Model Name
0000	QLGA
0001	TWC
0010	JW2
0011	TBD
0100	LG3
0101	LG5
0110	LG2C
0111	LG4C
1000	TBD
1001	JW6/JW7
1010	JW3

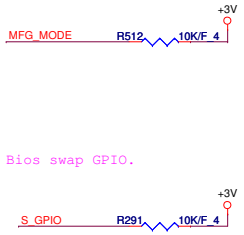
Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	No Dolby=0, Dolby=1
BOARD_ID5	GPIO69	HM76=0,HM70=1
DGPU_PRSNT	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

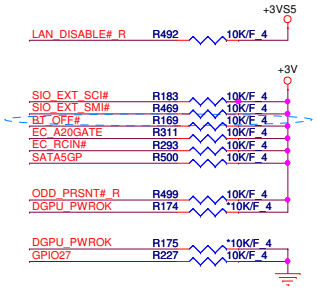
20110816 Define BRD_ID[3:0]

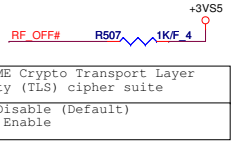


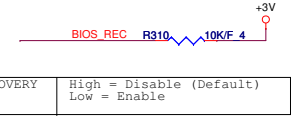
MFG-TEST

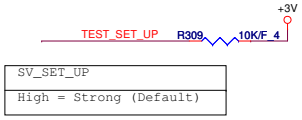


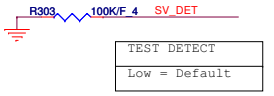
GPIO Pull-up/Pull-down(CLG)

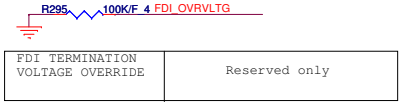












[6,7,8,10,12,13,14,18,21,22,23,24,25,27,28,29,30,35,37,39,41] +3V
[6,7,8,10,21,26,27,29,32,35,36,38,41] +3VS5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

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Size	Document Number	Rev
Custom	PCH 4/6 (GPIO)	A

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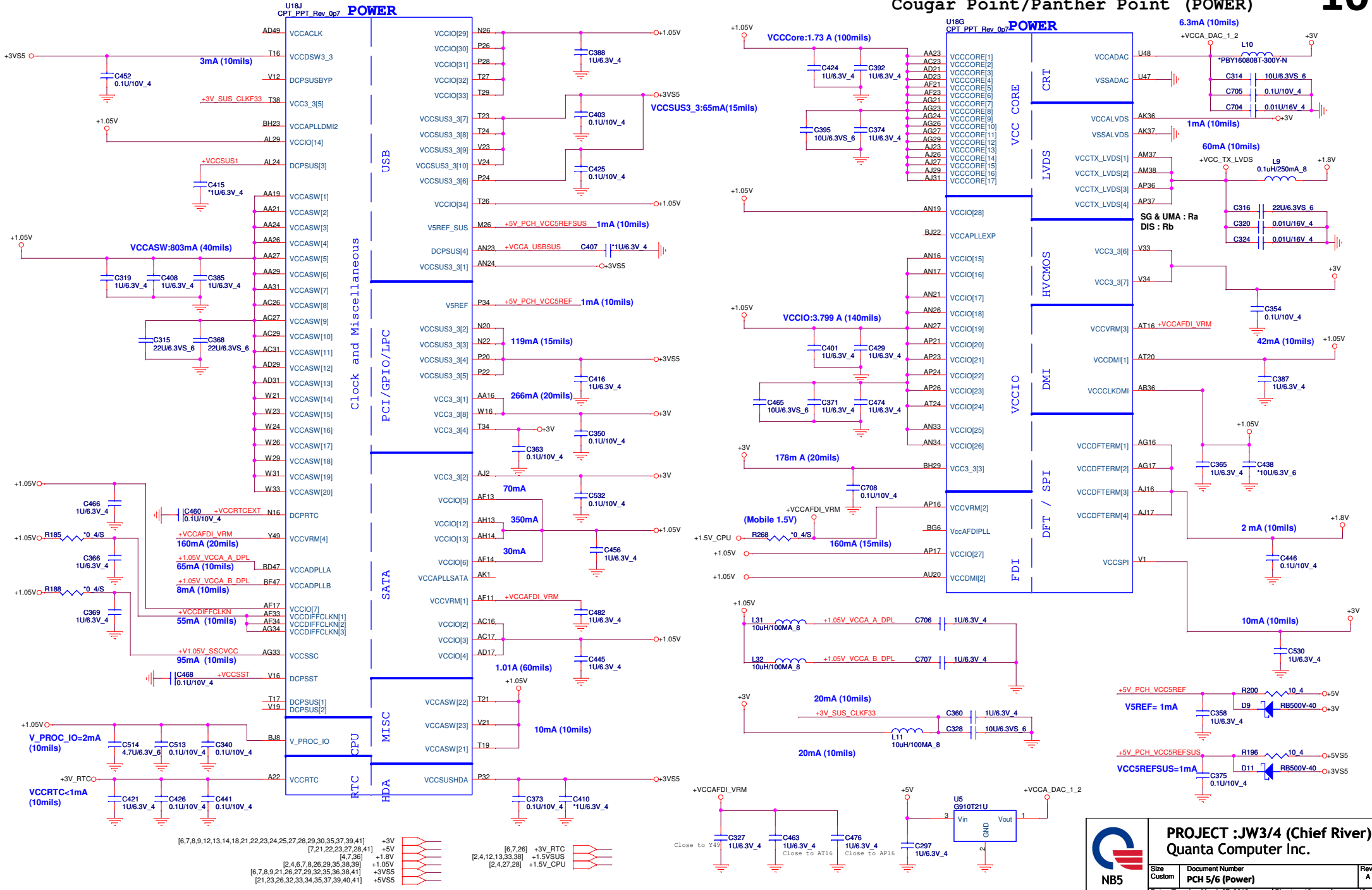
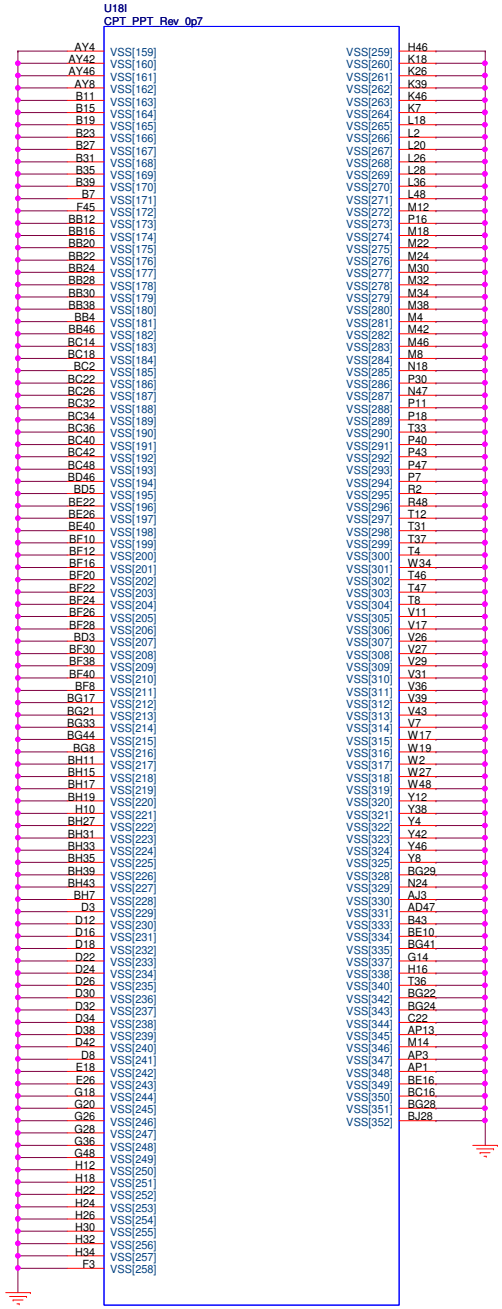
Cougar Point/Panther Point (POWER)

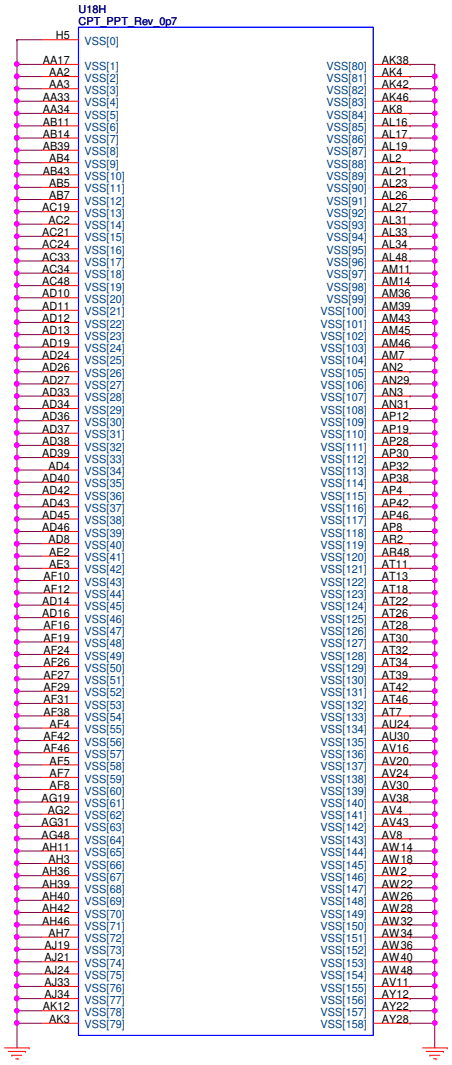
Cougar Point/Panther Point (POWER)



Cougar Point/Panther Point (GND)



Cougar Point/Panther Point (GND)



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PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

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Custom	PCH 6/6 (Ground)	A

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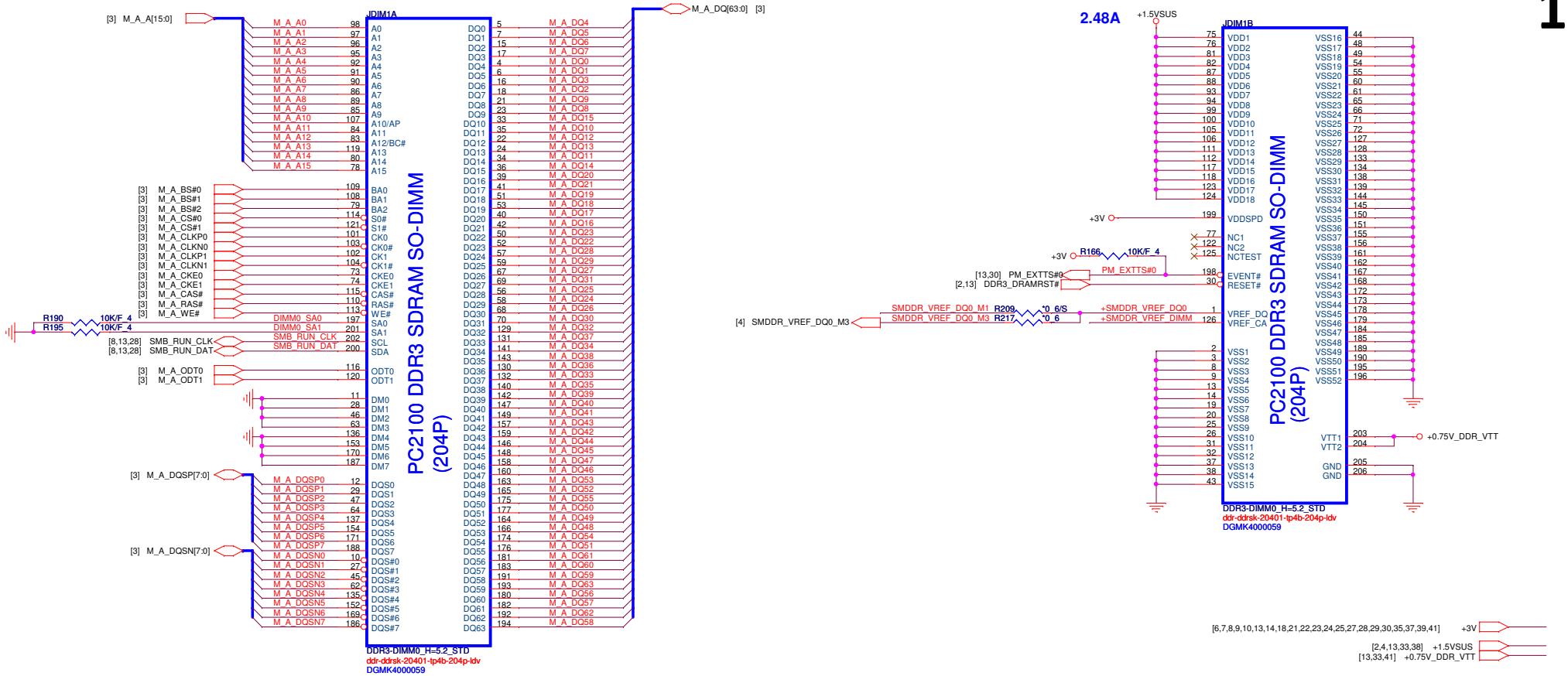
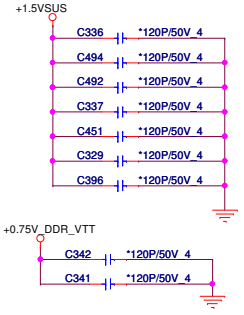
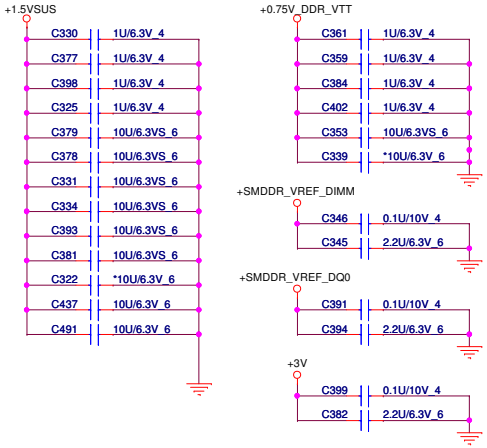


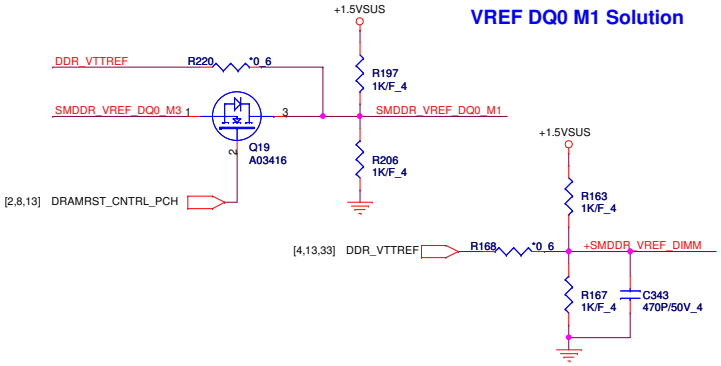
For EMI RESERVE 8/30



Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution



NB5

PROJECT :JW3/4 (Chief River)
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Size	Document Number	Rev
Custom	System Memory 1/2 (5.2H)	A
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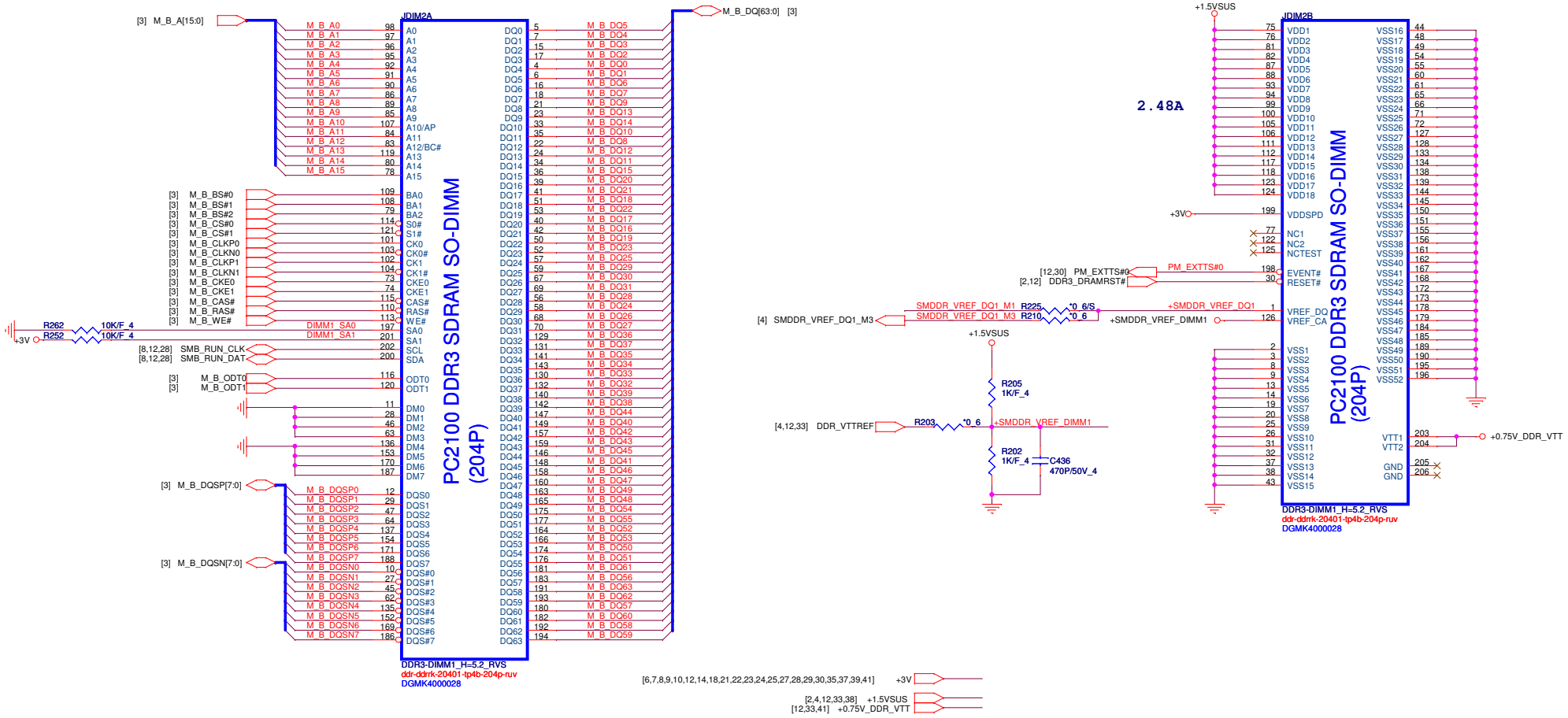
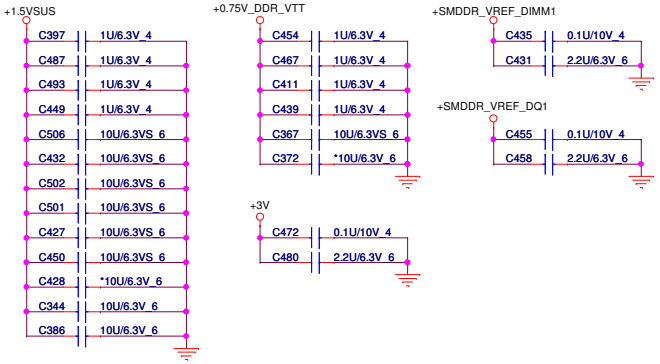
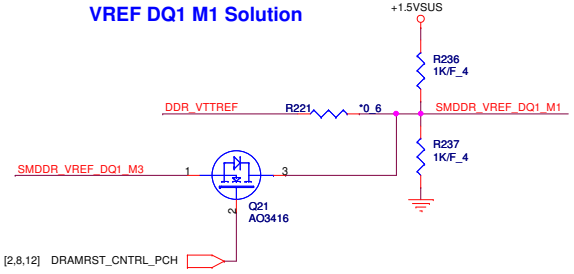


Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Memory 2/2 (9.2H)	A
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+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C67	22U/6.3VS_6	
C68	22U/6.3VS_6	
C108	10U/6.3VS_6	
C110	10U/6.3VS_6	
PLACE UNDER BGA C109	4.7U/6.3V_6	
C102	1U/6.3V_4	
PLACE NEAR BALLS C113	1U/6.3V_4	

+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C61	22U/6.3VS_6	
C60	22U/6.3VS_6	
C73	10U/6.3VS_6	
C72	10U/6.3VS_6	
PLACE UNDER BGA C111	4.7U/6.3V_6	
C103	1U/6.3V_4	
PLACE NEAR BALLS C104	1U/6.3V_4	

0727 PEX_IOVDD/Q
TOTAL 3500mA

U15A

[PEG Interface]
0.088mA

2500mA

AG19	PEX_IOVDD_1
AG21	PEX_IOVDD_2
AG22	PEX_IOVDD_3
AG24	PEX_IOVDD_4
AH21	PEX_IOVDD_5
AH25	PEX_IOVDD_6
AG13	PEX_IOVDDQ_1
AG15	PEX_IOVDDQ_2
AG16	PEX_IOVDDQ_3
AG18	PEX_IOVDDQ_4
AG25	PEX_IOVDDQ_5
AH15	PEX_IOVDDQ_6
AH18	PEX_IOVDDQ_7
AH26	PEX_IOVDDQ_8
AH27	PEX_IOVDDQ_9
AJ27	PEX_IOVDDQ_10
AK27	PEX_IOVDDQ_11
AL27	PEX_IOVDDQ_12
AM28	PEX_IOVDDQ_13
AN28	PEX_IOVDDQ_14

PEX_RX0	AN12	PEG_TX0	PEG_TX0 [2]
PEX_RX0_N	AM12	PEG_TX#0	PEG_TX#0 [2]
PEX_RX1	AN14	PEG_TX1	PEG_TX1 [2]
PEX_RX1_N	AM14	PEG_TX#1	PEG_TX#1 [2]
PEX_RX2	AP14	PEG_TX2	PEG_TX2 [2]
PEX_RX2_N	AP15	PEG_TX#2	PEG_TX#2 [2]
PEX_RX3	AN15	PEG_TX3	PEG_TX3 [2]
PEX_RX3_N	AM15	PEG_TX#3	PEG_TX#3 [2]
PEX_RX4	AN17	PEG_TX4	PEG_TX4 [2]
PEX_RX4_N	AM17	PEG_TX#4	PEG_TX#4 [2]
PEX_RX5	AP17	PEG_TX5	PEG_TX5 [2]
PEX_RX5_N	AP18	PEG_TX#5	PEG_TX#5 [2]
PEX_RX6	AN18	PEG_TX6	PEG_TX6 [2]
PEX_RX6_N	AM18	PEG_TX#6	PEG_TX#6 [2]
PEX_RX7	AN20	PEG_TX7	PEG_TX7 [2]
PEX_RX7_N	AM20	PEG_TX#7	PEG_TX#7 [2]
PEX_RX8	AP20		
PEX_RX8_N	AP21		
PEX_RX9	AN21		
PEX_RX9_N	AM21		
PEX_RX10	AN23		
PEX_RX10_N	AM23		
PEX_RX11	AP23		
PEX_RX11_N	AP24		
PEX_RX12	AN24		
PEX_RX12_N	AM24		
PEX_RX13	AN26		
PEX_RX13_N	AM26		
PEX_RX14	AP26		
PEX_RX14_N	AP27		
PEX_RX15	AN27		
PEX_RX15_N	AM27		

PEX_TX0	AK14	C_PEG_RX0	C70	0.22U/10V_4
PEX_TX0_N	AJ14	C_PEG_RX#0	C69	0.22U/10V_4
PEX_TX1	AH14	C_PEG_RX1	C80	0.22U/10V_4
PEX_TX1_N	AG14	C_PEG_RX#1	C81	0.22U/10V_4
PEX_TX2	AK15	C_PEG_RX2	C75	0.22U/10V_4
PEX_TX2_N	AJ15	C_PEG_RX#2	C74	0.22U/10V_4
PEX_TX3	AL16	C_PEG_RX3	C76	0.22U/10V_4
PEX_TX3_N	AK16	C_PEG_RX#3	C77	0.22U/10V_4
PEX_TX4	AK17	C_PEG_RX4	C82	0.22U/10V_4
PEX_TX4_N	AJ17	C_PEG_RX#4	C83	0.22U/10V_4
PEX_TX5	AH17	C_PEG_RX5	C85	0.22U/10V_4
PEX_TX5_N	AG17	C_PEG_RX#5	C84	0.22U/10V_4
PEX_TX6	AK18	C_PEG_RX6	C88	0.22U/10V_4
PEX_TX6_N	AJ18	C_PEG_RX#6	C89	0.22U/10V_4
PEX_TX7	AL19	C_PEG_RX7	C86	0.22U/10V_4
PEX_TX7_N	AK19	C_PEG_RX#7	C87	0.22U/10V_4
PEX_TX8	AK20			
PEX_TX8_N	AJ20			
PEX_TX9	AH20			
PEX_TX9_N	AG20			
PEX_TX10	AK21			
PEX_TX10_N	AJ21			
PEX_TX11	AL22			
PEX_TX11_N	AK22			
PEX_TX12	AK23			
PEX_TX12_N	AJ23			
PEX_TX13	AH23			
PEX_TX13_N	AG23			
PEX_TX14	AK24			
PEX_TX14_N	AJ24			
PEX_TX15	AL25			
PEX_TX15_N	AK25			

AC6	NC_1	
AJ28	NC_2	
AJ4	NC_3	
AJ5	NC_4	
AL11	NC_5	
C15	NC_6	
D19	NC_7	
D20	NC_8	
D23	NC_9	
D26	NC_10	
H31	NC_11	
T8	NC_12	
V32	NC_13	

+3V_GFX J8 VDD33_1
+3V_GFX K8 VDD33_2
L8 VDD33_3
M8 VDD33_4

0.085mA

PEX_REFCLK	AL13	CLK_PCIE_VGA	CLK_PCIE_VGA [8]	
PEX_REFCLK_N	AK13	CLK_PCIE_VGA#	CLK_PCIE_VGA# [8]	
PEX_TSTCLK_OUT	AJ26	PEX_TSTCLK	R383	*200/F_4
PEX_TSTCLK_OUT_N	AK26	PEX_TSTCLK#		
PEX_WAKE	AJ11			
PEX_RST_N	AJ12	VGA_RST#	R382	*0_4/S PEGX_RST#
PEX_CLKREQ_N	AK12	PEX_CLKREQ#	R445	10K/F_4 +3V_GFX
PEX_TERMP	AP29	PEX_TERMP	R376	2.49K/F_4
TESTMODE	AK11	TESTMODE	R380	10K/F_4

+3V_GFX
PLACE CLOSE TO BGA
C627 4.7U/6.3V_6
C667 2.2U/6.3V_6
C183 0.1U/10V_4
C168 0.1U/10V_4
C161 0.1U/10V_4
C171 0.1U/10V_4
PLACE CLOSE TO GPU BALLS

0.130mA
0.022mA
0.167mA

PEX_PLLVDD	AG26	PEX_PLLVDD	L2 HCB1608KF-300T30 +1.05V_GFX
PEX_PLL_HVDD	AH12		C71 4.7U/6.3V_6 PLACE NEAR BGA CLOSE TO CAPS
PEX_SVDD_3V3	AG12		C79 1U/6.3V_4 PLACE UNDER BGA
3.3V_AUX_NC	P8		C78 0.1U/10V_4 PLACE NEAR BALLS
VDD_SENSE	L4		
GND_SENSE	L5		

PLACE NEAR BGA
0.1U/10V_4 C105
4.7U/6.3V_6 C600
4.7U/6.3V_6 C64
+3V_GFX
12~16 mils width

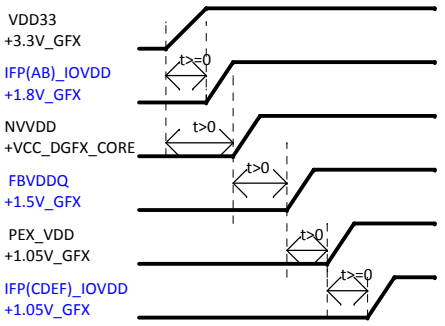
VGPU_CORE_SENSE [37]
VSS_GPU_SENSE [37]

N13x
N13P

+3V_GFX
R448 4.7K_4
[9,18] DGPU_PWROK
R449 *0_4/S
Q35 DTC144EUA
CLK_PEGA_REQ# [8]
PEX_CLKREQ#
Q36 *DTC144EUA

+3V
U19 MC74VHC1G08DFT2G
C469 0.1U/10V_4
[2,8,24,25,27,29] PLTRST#
[9] DGPU_HOLD_RST#
DGPU_HOLD_RST#
PEGX_RST#
R329 100K/F_4
R318 *330/F_4

Power up sequence



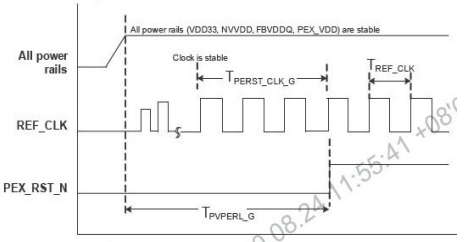
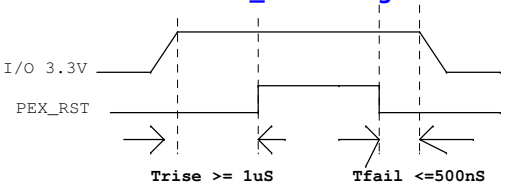


Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

PEX_RST timing



[15,16,18,38] +1.05V_GFX
[16,17,18,37,38] +3V_GFX

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

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A3	DGPU 1/5 (PEG)	A
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U15B

[MEMORY I/F A]

[19] FBA_CMD[30:0]

FBA_CMD0 U30
FBA_CMD1 T31
FBA_CMD2 U29
FBA_CMD3 R34
FBA_CMD4 R33
FBA_CMD5 U32
FBA_CMD6 U33
FBA_CMD7 U28
FBA_CMD8 V28
FBA_CMD9 V29
FBA_CMD10 V30
FBA_CMD11 U34
FBA_CMD12 U31
FBA_CMD13 V34
FBA_CMD14 V33
FBA_CMD15 Y32
FBA_CMD16 AA31
FBA_CMD17 AA29
FBA_CMD18 AA28
FBA_CMD19 AC34
FBA_CMD20 AC33
FBA_CMD21 AA32
FBA_CMD22 AA33
FBA_CMD23 Y28
FBA_CMD24 Y29
FBA_CMD25 W31
FBA_CMD26 Y30
FBA_CMD27 AA34
FBA_CMD28 Y31
FBA_CMD29 Y34
FBA_CMD30 Y33
V31

FBA_CMD0 (FBA_CMD25)
FBA_CMD1 (FBA_CMD23)
FBA_CMD2
FBA_CMD3 (FBA_CMD0)
FBA_CMD4 (FBA_CMD10)
FBA_CMD5 (FBA_CMD26)
FBA_CMD6 (FBA_CMD14)
FBA_CMD7
FBA_CMD8 (FBA_CMD1)
FBA_CMD9 (FBA_CMD22)
FBA_CMD10 (FBA_CMD20)
FBA_CMD11 (FBA_CMD24)
FBA_CMD12 (FBA_CMD18)
FBA_CMD13 (FBA_CMD9)
FBA_CMD14 (FBA_CMD29)
FBA_CMD15 (FBA_CMD8)
FBA_CMD16 (FBA_CMD27)
FBA_CMD17 (FBA_CMD15)
FBA_CMD18 (FBA_CMD11)
FBA_CMD19 (FBA_CMD16)
FBA_CMD20 (FBA_CMD28)
FBA_CMD21 (FBA_CMD3)
FBA_CMD22 (FBA_CMD17)
FBA_CMD23 (FBA_CMD5)
FBA_CMD24 (FBA_CMD4)
FBA_CMD25 (FBA_CMD21)
FBA_CMD26 (FBA_CMD6)
FBA_CMD27 (FBA_CMD13)
FBA_CMD28 (FBA_CMD19)
FBA_CMD29 (FBA_CMD12)
FBA_CMD30
FBA_CMD31 (NC)

[19] VMA_DM[7:0]

VMA_DM0 P30
VMA_DM1 F31
VMA_DM2 F34
VMA_DM3 M32
VMA_DM4 AD31
VMA_DM5 AL29
VMA_DM6 AM32
VMA_DM7 AF34

FBA_DQM0
FBA_DQM1
FBA_DQM2
FBA_DQM3
FBA_DQM4
FBA_DQM5
FBA_DQM6
FBA_DQM7

[19] VMA_WDQS[7:0]

VMA_WDQS0 M31
VMA_WDQS1 G31
VMA_WDQS2 E33
VMA_WDQS3 M33
VMA_WDQS4 AE31
VMA_WDQS5 AK32
VMA_WDQS6 AN33
VMA_WDQS7 AF33

FBA_DQS_WP0
FBA_DQS_WP1
FBA_DQS_WP2
FBA_DQS_WP3
FBA_DQS_WP4
FBA_DQS_WP5
FBA_DQS_WP6
FBA_DQS_WP7

[19] VMA_RDQS[7:0]

VMA_RDQS0 M30
VMA_RDQS1 H30
VMA_RDQS2 E34
VMA_RDQS3 M34
VMA_RDQS4 AF30
VMA_RDQS5 AK31
VMA_RDQS6 AM34
VMA_RDQS7 AF32

FBA_DQS_RN0
FBA_DQS_RN1
FBA_DQS_RN2
FBA_DQS_RN3
FBA_DQS_RN4
FBA_DQS_RN5
FBA_DQS_RN6
FBA_DQS_RN7

+1.5V_GFX

AA27 AA30 AB27 AB33 AC27 AD27 AE27 AF27 AG27 B13 B16 B19 E13 E16 E19 H10 H11 H12 H13 H14 H15 H16 H18 H19 H20 H21 H22 H23 H24 H8 H9 L27 M27 N27 P27 R27 T27 T30 T33 V27 W27 W30 W33 Y27

FBVDDQ_1 FBVDDQ_2 FBVDDQ_3 FBVDDQ_4 FBVDDQ_5 FBVDDQ_6 FBVDDQ_7 FBVDDQ_8 FBVDDQ_9 FBVDDQ_10 FBVDDQ_11 FBVDDQ_12 FBVDDQ_13 FBVDDQ_14 FBVDDQ_15 FBVDDQ_16 FBVDDQ_17 FBVDDQ_18 FBVDDQ_19 FBVDDQ_20 FBVDDQ_21 FBVDDQ_22 FBVDDQ_23 FBVDDQ_24 FBVDDQ_25 FBVDDQ_26 FBVDDQ_27 FBVDDQ_28 FBVDDQ_29 FBVDDQ_30 FBVDDQ_31 FBVDDQ_32 FBVDDQ_33 FBVDDQ_34 FBVDDQ_35 FBVDDQ_36 FBVDDQ_37 FBVDDQ_38 FBVDDQ_39 FBVDDQ_40 FBVDDQ_41 FBVDDQ_42 FBVDDQ_43 FBVDDQ_44

FBVDDQ+FBVDDQ
8A
0.062mA

PLACE CLOSE TO GPU BALLS

C244 4.7U/6.3V_6
C185 4.7U/6.3V_6
C166 2.2U/6.3V_6
C184 2.2U/6.3V_6
C143 0.1U/10V_4
C159 0.1U/10V_4
C170 0.1U/10V_4
C135 0.1U/10V_4
C123 0.1U/10V_4
C179 0.1U/10V_4
C173 0.1U/10V_4
C181 0.1U/10V_4

C280 10U/6.3V_6
C282 10U/6.3V_6
C210 10U/6.3V_6
C53 10U/6.3V_6

PLACE CLOSE TO BGA

N13x

FBA_D0 L28 VMA_DQ0
FBA_D1 M29 VMA_DQ1
FBA_D2 L29 VMA_DQ2
FBA_D3 M28 VMA_DQ3
FBA_D4 N31 VMA_DQ4
FBA_D5 P29 VMA_DQ5
FBA_D6 R29 VMA_DQ6
FBA_D7 P28 VMA_DQ7
FBA_D8 J28 VMA_DQ8
FBA_D9 H29 VMA_DQ9
FBA_D10 J29 VMA_DQ10
FBA_D11 H28 VMA_DQ11
FBA_D12 G29 VMA_DQ12
FBA_D13 E31 VMA_DQ13
FBA_D14 E32 VMA_DQ14
FBA_D15 F30 VMA_DQ15
FBA_D16 C34 VMA_DQ16
FBA_D17 D32 VMA_DQ17
FBA_D18 B33 VMA_DQ18
FBA_D19 C33 VMA_DQ19
FBA_D20 F33 VMA_DQ20
FBA_D21 F32 VMA_DQ21
FBA_D22 H33 VMA_DQ22
FBA_D23 H32 VMA_DQ23
FBA_D24 P34 VMA_DQ24
FBA_D25 P32 VMA_DQ25
FBA_D26 P31 VMA_DQ26
FBA_D27 P33 VMA_DQ27
FBA_D28 L31 VMA_DQ28
FBA_D29 L34 VMA_DQ29
FBA_D30 L32 VMA_DQ30
FBA_D31 L33 VMA_DQ31
FBA_D32 AG28 VMA_DQ32
FBA_D33 AF29 VMA_DQ33
FBA_D34 AG29 VMA_DQ34
FBA_D35 AF28 VMA_DQ35
FBA_D36 AD30 VMA_DQ36
FBA_D37 AD29 VMA_DQ37
FBA_D38 AC29 VMA_DQ38
FBA_D39 AD28 VMA_DQ39
FBA_D40 AJ29 VMA_DQ40
FBA_D41 AK29 VMA_DQ41
FBA_D42 AJ30 VMA_DQ42
FBA_D43 AK28 VMA_DQ43
FBA_D44 AM29 VMA_DQ44
FBA_D45 AM31 VMA_DQ45
FBA_D46 AN29 VMA_DQ46
FBA_D47 AM30 VMA_DQ47
FBA_D48 AN31 VMA_DQ48
FBA_D49 AN32 VMA_DQ49
FBA_D50 AP30 VMA_DQ50
FBA_D51 AP32 VMA_DQ51
FBA_D52 AM33 VMA_DQ52
FBA_D53 AL31 VMA_DQ53
FBA_D54 AK33 VMA_DQ54
FBA_D55 AK32 VMA_DQ55
FBA_D56 AD34 VMA_DQ56
FBA_D57 AD32 VMA_DQ57
FBA_D58 AC30 VMA_DQ58
FBA_D59 AD33 VMA_DQ59
FBA_D60 AF31 VMA_DQ60
FBA_D61 AG34 VMA_DQ61
FBA_D62 AG32 VMA_DQ62
FBA_D63 AG33 VMA_DQ63

FBA_CLK0 R30 VMA_CLK0 VMA_CLK0 [19]
FBA_CLK0_N R31 VMA_CLK0# VMA_CLK0# [19]
FBA_CLK1 AB31 VMA_CLK1 VMA_CLK1 [19]
FBA_CLK1_N AC31 VMA_CLK1# VMA_CLK1# [19]
15mils width

(FBA_DEBUG) FBA_DEBUG0 R28 FBA_DEBUG *60.4/F_4 R439 +1.5V_GFX
(NC) FBA_DEBUG1 AC28 FBA_DEBUG1 *60.4/F_4 R14
FB_VREF_NC H26 T1

FBA_CMD_RFU0 R32
FBA_CMD_RFU1 AC32

FBA_WCK01 K31
FBA_WCK01_N L30
FBA_WCK23 H34
FBA_WCK23_N J34
FBA_WCK45 AG30
FBA_WCK45_N AG31
FBA_WCK67 AJ34
FBA_WCK67_N AK34

FBA_WCKB01 J30
FBA_WCKB01_N J31
FBA_WCKB23 J32
FBA_WCKB23_N J33
FBA_WCKB45 AH31
FBA_WCKB45_N AJ31
FBA_WCKB67 AJ32
FBA_WCKB67_N AJ33

N13M-GE2	N13P-GS
N13P-GL	
Reserve Ra	Stuff Ra

PLACE CLOSE TO BALL
RSVD E1 PS_FB_CLAMP
Ra R437 10K/F_4
Rb
FB_DLL_AVDD K27 +FB_PLLAVDD C172 0.1U/10V_4
FBA_PLL_AVDD U27 +FB_PLLAVDD L27 HCB1608KF-300T30 +1.05V_GFX
PLACE NEAR BGA CLOSE TO CAPS
C601 22U/6.3VS_6
C155 0.1U/10V_4
C149 0.1U/10V_4
PLACE CLOSE TO BGA
PLACE CLOSE TO BALL
FBVDDQ_PROBE F1 FBVDDQ_SENSE TP52
GND_PROBE F2 FB_GND_SENSE TP53
FB_CAL_PD_VDDQ J27 FB_CAL_PD_VDDQ R441 40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND H27 FB_CAL_PU_GND R442 40.2/F_4
FB_CALTERM_GND H25 FB_CAL_TERM_GND R443 51_4
PLACE CLOSE TO GPU BALLS
2011 12 07 : Change to 51ohm for NVIDIA requirement

U15C

MEMORY I/F C

[20] FBC_CMD[30:0]

FBC_CMD0 D13
FBC_CMD1 E14
FBC_CMD2 F14
FBC_CMD3 A12
FBC_CMD4 B12
FBC_CMD5 C14
FBC_CMD6 B14
FBC_CMD7 G15
FBC_CMD8 F15
FBC_CMD9 E15
FBC_CMD10 D15
FBC_CMD11 A14
FBC_CMD12 D14
FBC_CMD13 A15
FBC_CMD14 B15
FBC_CMD15 C17
FBC_CMD16 D18
FBC_CMD17 E18
FBC_CMD18 F18
FBC_CMD19 A20
FBC_CMD20 B20
FBC_CMD21 C18
FBC_CMD22 B18
FBC_CMD23 G18
FBC_CMD24 G17
FBC_CMD25 F17
FBC_CMD26 D16
FBC_CMD27 A18
FBC_CMD28 D17
FBC_CMD29 A17
FBC_CMD30 B17
E17

FBB_CMD0 (FBC_CMD25)
FBB_CMD1 (FBC_CMD23)
FBB_CMD2
FBB_CMD3 (FBC_CMD0)
FBB_CMD4 (FBC_CMD10)
FBB_CMD5 (FBC_CMD26)
FBB_CMD6 (FBC_CMD14)
FBC_CMD7
FBB_CMD8 (FBC_CMD1)
FBB_CMD9 (FBC_CMD22)
FBB_CMD10 (FBC_CMD20)
FBB_CMD11 (FBC_CMD24)
FBB_CMD12 (FBC_CMD18)
FBB_CMD13 (FBC_CMD9)
FBB_CMD14 (FBC_CMD29)
FBB_CMD15 (FBC_CMD8)
FBB_CMD16 (FBC_CMD27)
FBB_CMD17 (FBC_CMD15)
FBB_CMD18 (FBC_CMD11)
FBB_CMD19 (FBC_CMD16)
FBB_CMD20 (FBC_CMD28)
FBB_CMD21 (FBC_CMD3)
FBB_CMD22 (FBC_CMD17)
FBB_CMD23 (FBC_CMD5)
FBB_CMD24(FBC_CMD4)
FBB_CMD25 (FBC_CMD21)
FBB_CMD26 (FBC_CMD6)
FBB_CMD27 (FBC_CMD13)
FBB_CMD28 (FBC_CMD19)
FBB_CMD29 (FBC_CMD12)
FBC_CMD30
FBC_CMD31 (NC)

[20] VMC_DM[7:0]

VMC_DM0 E11
VMC_DM1 E3
VMC_DM2 A3
VMC_DM3 C9
VMC_DM4 F23
VMC_DM5 F27
VMC_DM6 C30
VMC_DM7 A24

FBC_DQM0
FBC_DQM1
FBC_DQM2
FBC_DQM3
FBC_DQM4
FBC_DQM5
FBC_DQM6
FBC_DQM7

[20] VMC_WDQS[7:0]

VMC_WDQS0 D10
VMC_WDQS1 D5
VMC_WDQS2 C3
VMC_WDQS3 B9
VMC_WDQS4 E23
VMC_WDQS5 E28
VMC_WDQS6 B30
VMC_WDQS7 A23

FBC_DQS_WP0
FBC_DQS_WP1
FBC_DQS_WP2
FBC_DQS_WP3
FBC_DQS_WP4
FBC_DQS_WP5
FBC_DQS_WP6
FBC_DQS_WP7

[20] VMC_RDQS[7:0]

VMC_RDQS0 D9
VMC_RDQS1 E4
VMC_RDQS2 B2
VMC_RDQS3 A9
VMC_RDQS4 D22
VMC_RDQS5 D28
VMC_RDQS6 A30
VMC_RDQS7 B23

FBC_DQS_RN0
FBC_DQS_RN1
FBC_DQS_RN2
FBC_DQS_RN3
FBC_DQS_RN4
FBC_DQS_RN5
FBC_DQS_RN6
FBC_DQS_RN7

FBC_D0 G9 VMC_DQ0
FBC_D1 E9 VMC_DQ1
FBC_D2 G8 VMC_DQ2
FBC_D3 F9 VMC_DQ3
FBC_D4 F11 VMC_DQ4
FBC_D5 G11 VMC_DQ5
FBC_D6 F12 VMC_DQ6
FBC_D7 G12 VMC_DQ7
FBC_D8 G6 VMC_DQ8
FBC_D9 F5 VMC_DQ9
FBC_D10 E6 VMC_DQ10
FBC_D11 F6 VMC_DQ11
FBC_D12 F4 VMC_DQ12
FBC_D13 G4 VMC_DQ13
FBC_D14 E2 VMC_DQ14
FBC_D15 F3 VMC_DQ15
FBC_D16 C2 VMC_DQ16
FBC_D17 D4 VMC_DQ17
FBC_D18 D3 VMC_DQ18
FBC_D19 C1 VMC_DQ19
FBC_D20 B3 VMC_DQ20
FBC_D21 C4 VMC_DQ21
FBC_D22 B5 VMC_DQ22
FBC_D23 C5 VMC_DQ23
FBC_D24 A11 VMC_DQ24
FBC_D25 C11 VMC_DQ25
FBC_D26 D11 VMC_DQ26
FBC_D27 B11 VMC_DQ27
FBC_D28 D8 VMC_DQ28
FBC_D29 A8 VMC_DQ29
FBC_D30 C8 VMC_DQ30
FBC_D31 B8 VMC_DQ31
FBC_D32 F24 VMC_DQ32
FBC_D33 G23 VMC_DQ33
FBC_D34 E24 VMC_DQ34
FBC_D35 G24 VMC_DQ35
FBC_D36 D21 VMC_DQ36
FBC_D37 E21 VMC_DQ37
FBC_D38 G21 VMC_DQ38
FBC_D39 F21 VMC_DQ39
FBC_D40 G27 VMC_DQ40
FBC_D41 D27 VMC_DQ41
FBC_D42 G26 VMC_DQ42
FBC_D43 E27 VMC_DQ43
FBC_D44 E29 VMC_DQ44
FBC_D45 F29 VMC_DQ45
FBC_D46 E30 VMC_DQ46
FBC_D47 D30 VMC_DQ47
FBC_D48 A32 VMC_DQ48
FBC_D49 C31 VMC_DQ49
FBC_D50 C32 VMC_DQ50
FBC_D51 B32 VMC_DQ51
FBC_D52 D29 VMC_DQ52
FBC_D53 A29 VMC_DQ53
FBC_D54 C29 VMC_DQ54
FBC_D55 B29 VMC_DQ55
FBC_D56 B21 VMC_DQ56
FBC_D57 C23 VMC_DQ57
FBC_D58 A21 VMC_DQ58
FBC_D59 C21 VMC_DQ59
FBC_D60 B24 VMC_DQ60
FBC_D61 C24 VMC_DQ61
FBC_D62 B26 VMC_DQ62
FBC_D63 C26 VMC_DQ63

FBC_CLK0 D12 VMC_CLK0 VMC_CLK0 [20]
FBC_CLK0_N E12 VMC_CLK0# VMC_CLK0# [20]
FBC_CLK1 E20 VMC_CLK1 VMC_CLK1 [20]
FBC_CLK1_N F20 VMC_CLK1# VMC_CLK1# [20]

(FBC_DEBUG) FBB_DEBUG0 G14 FBC_DEBUG *60.4/F_4 R91 +1.5V_GFX
(NC) FBB_DEBUG1 G20 FBC_DEBUG1 *60.4/F_4 R92

FBB_CMD_RFU0 C12
FBB_CMD_RFU1 C20

FBB_WCK01 F8
FBB_WCK01_N F8
FBB_WCK23 A5
FBB_WCK23_N A6
FBB_WCK45 D24
FBB_WCK45_N D25
FBB_WCK67 B27
FBB_WCK67_N C27

FBB_WCKB01 D6
FBB_WCKB01_N D7
FBB_WCKB23 C6
FBB_WCKB23_N B6
FBB_WCKB45 F26
FBB_WCKB45_N E26
FBB_WCKB67 A26
FBB_WCKB67_N A27

FBB_PLL_AVDD H17 +FB_PLLAVDD C178 0.1U/10V_4
PLACE CLOSE TO BALL

N13x

For Fermi

FBA_CMD2 R86 10K/F_4
FBA_CMD3 R434 10K/F_4
FBA_CMD5 R55 10K/F_4
FBA_CMD18 R369 10K/F_4
FBA_CMD19 R43 10K/F_4
FBC_CMD2 R122 10K/F_4
FBC_CMD3 R461 10K/F_4
FBC_CMD5 R463 10K/F_4
FBC_CMD18 R457 10K/F_4
FBC_CMD19 R452 10K/F_4

VMA_DQ[63:0] VMA_DQ[63:0] [19]
VMC_DQ[63:0] VMC_DQ[63:0] [20]

[18,19,20,38] +1.5V_GFX
[14,16,18,38] +1.05V_GFX

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

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Custom	DGPU 2/5 (Memory)	A
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[14,15,18,38] +1.05V_GFX
[14,17,18,37,38] +3V_GFX

U15D

R374 10K/F_4 IFPAB_PLLVDD → AH8 IFPAB_PLLVDD
IFPAB_IOVDD → AG8 IFPA_IOVDD
R372 10K/F_4 → AG9 IFPB_IOVDD
R373 *1K/F_4 → AJ8 IFPAB_RSET

[IFPA/B_LVDS]
IFPA_TXC AM6
IFPA_TXC_N AN6
IFPA_TXD0 AP3
IFPA_TXD0_N AN3
IFPA_TXD1 AN5
IFPA_TXD1_N AM5
IFPA_TXD2 AL6
IFPA_TXD2_N AK6
IFPA_TXD3 AJ6
IFPA_TXD3_N AH6
IFPB_TXC AJ9
IFPB_TXC_N AH9
IFPB_TXD4 AP6
IFPB_TXD4_N AP5
IFPB_TXD5 AM7
IFPB_TXD5_N AL7
IFPB_TXD6 AN8
IFPB_TXD6_N AM8
IFPB_TXD7 AK8
IFPB_TXD7_N AL8

0824 Update Symbol

AF7 → IFPC_PLLVDD
R388 10K/F_4 IFPCD_PLLVDD → AG7 IFPD_PLLVDD

[IFPC/D_TMDS]
IFPC_AUX_I2CW_SCL AG3
IFPC_AUX_I2CW_SDA_N AG2
IFPC_L0 AK1
IFPC_L0_N AJ1
IFPC_L1 AJ3
IFPC_L1_N AJ2
IFPC_L2 AH3
IFPC_L2_N AH4
IFPC_L3 AG5
IFPC_L3_N AG4

AF6 → IFPC_IOVDD
R387 10K/F_4 IFPCD_IOVDD → AG6 IFPD_IOVDD

IFPD_AUX_I2CX_SCL AK3
IFPD_AUX_I2CX_SDA_N AK2
IFPD_L0 AM1
IFPD_L0_N AM2
IFPD_L1 AM3
IFPD_L1_N AM4
IFPD_L2 AL3
IFPD_L2_N AL4
IFPD_L3 AK4
IFPD_L3_N AK5

R375 *1K/F_4 → AF8 IFPC_RSET
AN2 IFPD_RSET

R391 10K/F_4 IFPEF_PLLVDD → AB8 IFPEF_PLLVDD

[IFPE/F_DP]
IFPE_AUX_I2CY_SCL AB3
IFPE_AUX_I2CY_SDA_N AB4
IFPE_L0 AD2
IFPE_L0_N AD3
IFPE_L1 AD1
IFPE_L1_N AC1
IFPE_L2 AC2
IFPE_L2_N AC3
IFPE_L3 AC4
IFPE_L3_N AC5

AC7 → IFPE_IOVDD
R389 10K/F_4 IFPEF_IOVDD → AC8 IFPF_IOVDD

AD6 → IFPEF_RSET

IFPF_AUX_I2CZ_SCL AF3
IFPF_AUX_I2CZ_SDA_N AF2
IFPF_L0 AE3
IFPF_L0_N AF4
IFPF_L1 AF5
IFPF_L1_N AD4
IFPF_L2 AD5
IFPF_L2_N AG1
IFPF_L3 AF1
IFPF_L3_N AE1

R371 10K/F_4 DACA_VDD → AG10 DACA_VDD

[DACA/B_CRT]
DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9

T3 → AP9 DACA_VREF
T2 → AP8 DACA_RSET

DACA_HSYNC AM9
DACA_VSYNC AN9

I2CA_SCL R4 I2CA_SCL R64 2.2K_4 +3V_GFX
I2CA_SDA R5 I2CA_SDA R70 2.2K_4

+1.05V_GFX L28 HCB1608KF-300T30 NV_PLLVDD → AD8 PLLVDD 0.052mA
C614 22U/6.3VS_6
C613 0.1U/10V_4

AE8 SP_PLLVDD 0.067mA

PLACE CLOSE TO GPU

AD7 VID_PLLVDD 0.041mA
C144 C129
C124 22U/6.3VS_6 4.7U/6.3V_6 0.1U/10V_4

PLACE CLOSE TO BALLS
within 150mils

[XTAL IN]
XTAL_IN H3 CLK_27M_XTAL_IN
XTAL_OUT H2 CLK_27M_XTAL_OUT
XTAL_OUTBUFF J4 R78 10K/F_4
XTAL_SSIN H1 R428 10K/F_4

Y2 27MHZ +-10PPM
C198 12P/50V_4
C192 12P/50V_4

N13x

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

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A3	DGPU 3/5 (Display)	A
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Net name	N13M-GE2	N13P-GS(QS)
ROM_SI		
ROM_SO	PD 10K	PU 10K
ROM_SCLK	PD 15K	PU 5K
STRAP0	PU 45K	PU 45K
STRAP1	PD 45K	PD 5K
STRAP2	PU 15K	PD 15K
STRAP3	UN-STUFF	PD 5K
STRAP4	UN-STUFF	PD 45K

For N13M-GE2
ROM_SO PD 10K
ROM_SCLK PD 15K

N13M-GE2-A1 ID:0X0DEA
N13P-GS ID:0X0FD2

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Default: Hynix VRAM

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	1001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0011
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0111
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	XXXX
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	XXXX

U15E

[MIOA]

[MIOB]

[MISC_GPIO/I2C/JTAG/THER]

[MISC2_ROM]

N13x

VID 0 0 0 0 1 1 0 ---> 0.9V

Q34 *ME2N7002D

	N13M-GE2	N13P-GS
Ra	Un-Stuff	Stuff
Qa	Stuff	Un-Stuff

For N13M-GE2, N13M-GS (QS)
Defult : 2G Samsung

VRAM Configuration Table
ROM_SI
1G Hynix 64Mx16 -->15K PD
1G Samsung 64Mx16 -->20K PD
2G Hynix 128Mx16 -->35K PD
2G Samsung 128Mx16 -->45K PD

2011 12 01 : Add net DGPU_PROCHOT#

GFx SMBus Isolation **

Q33 2N7002DW

2011 12 01 : Add off-page connector

N13M-GE2 N13P-GL	N13P-GS
Stuff Rc	Un-stuff Rc

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

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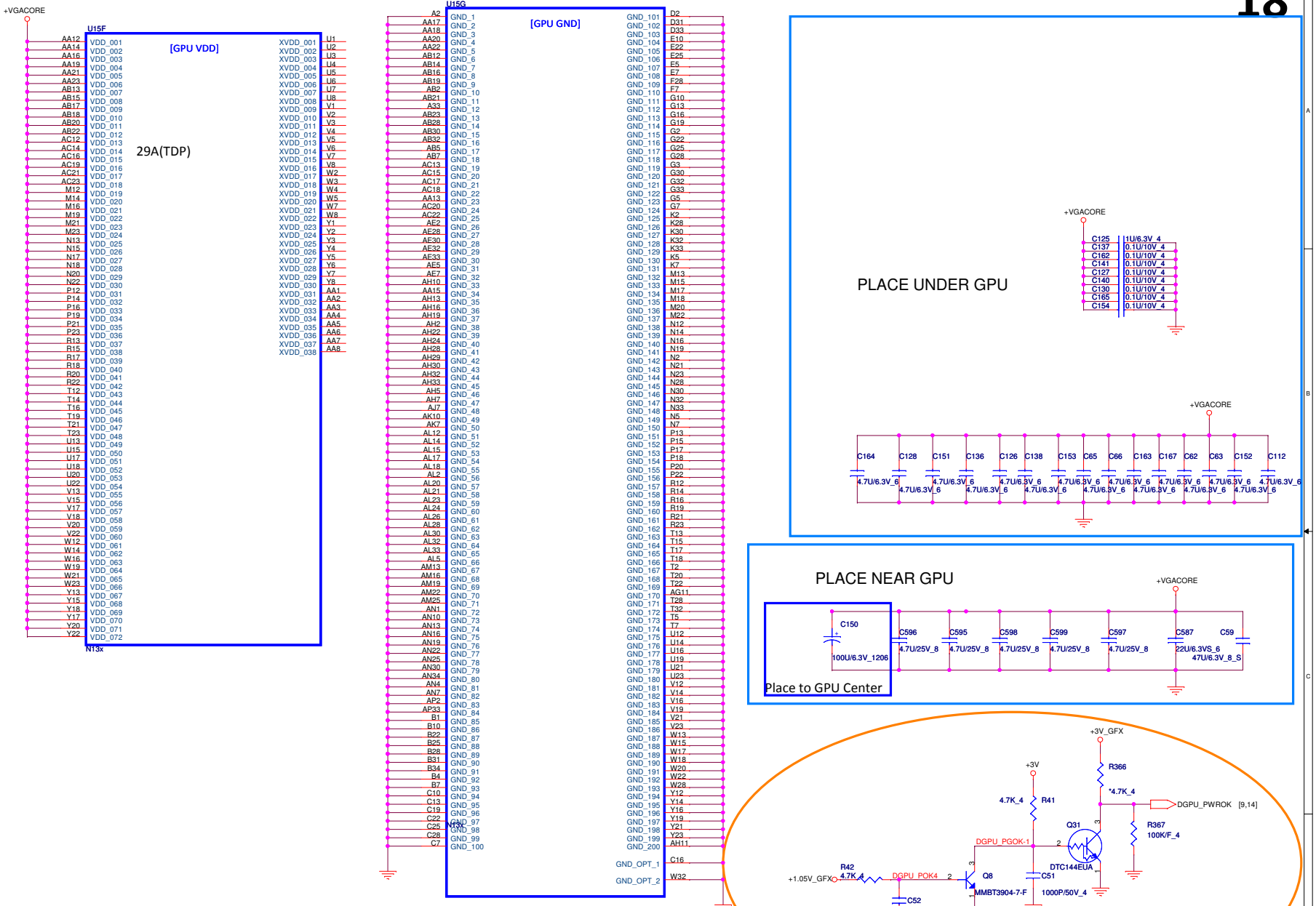
U15F
[GPU VDD]
29A(TDP)
N13x
U15G
[GPU GND]
N13x
PLACE UNDER GPU
+VGACORE
C125 1U/6.3V_4
C137 0.1U/10V_4
C162 0.1U/10V_4
C141 0.1U/10V_4
C127 0.1U/10V_4
C140 0.1U/10V_4
C130 0.1U/10V_4
C165 0.1U/10V_4
C154 0.1U/10V_4
C164 C128 C151 C136 C126 C138 C153 C65 C66 C163 C167 C62 C63 C152 C112
4.7U/6.3V_6
PLACE NEAR GPU
C150
100U/6.3V_1206
C596 C595 C598 C599 C597 C587 C59
4.7U/25V_8
22U/6.3V5_6
47U/6.3V_8_S
Place to GPU Center
+3V_GFX
+3V
R366
*4.7K_4
4.7K_4
R41
DGPU_PWROK [9,14]
Q31
R367
100K/F_4
DGPU_PGOK-1
R42
4.7K_4
+1.05V_GFX
DGPU_POK4
Q8
MMBT3904-7-F
DTC144EUA
C51
1000P/50V_4
C52
*1000P/50V_4
R40
4.7K_4
+1.5V_GFX
DGPU_POK2
Q7
MMBT3904-7-F
C50
*1000P/50V_4
11/10 add for DGPU_PWROK circuit
for meet Power down sequence for +3V_GFX
+VGACORE
RB500V-40
D22
+1.5V_GFX
RB500V-40
D21
+3V_GFX
[37] +VGACORE
[14,15,16,38] +1.05V_GFX
[15,19,20,38] +1.5V_GFX
[14,16,17,37,38] +3V_GFX
[6,7,8,9,10,12,13,14,21,22,23,24,25,27,28,29,30,35,37,39,41] +3V
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.
NB5
Size Custom
Document Number
DGPU 5/5 (Power/Ground)
Rev A
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900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

CHANNEL A: 256MB/512MB DDR3

[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

VRAM2 / VRAM6 / VRAM1 / VRAM5

VREFC_VMA1 / VREFD_VMA1 (VRAM2)
VREFC_VMA1 / VREFD_VMA1 (VRAM6)
VREFC_VMA3 / VREFD_VMA3 (VRAM1)
VREFC_VMA3 / VREFD_VMA3 (VRAM5)

[15] FBA_CMD9
[15] FBA_CMD11
[15] FBA_CMD8
[15] FBA_CMD25
[15] FBA_CMD10
[15] FBA_CMD24
[15] FBA_CMD22
[15] FBA_CMD7
[15] FBA_CMD21
[15] FBA_CMD6
[15] FBA_CMD29
[15] FBA_CMD23
[15] FBA_CMD28
[15] FBA_CMD20
[15] FBA_CMD4
[15] FBA_CMD14

[15] FBA_CMD12
[15] FBA_CMD27
[15] FBA_CMD26

[15] VMA_CLK0
[15] VMA_CLK0#
[15] FBA_CMD3

[15] FBA_CMD2
[15] FBA_CMD0
[15] FBA_CMD30
[15] FBA_CMD15
[15] FBA_CMD13

VMA_WDQS0 / VMA_RDQS0
VMA_DM1 / VMA_DM0

[15] FBA_CMD5

VMA_ZQ1

Should be 240 Ohms +-1%

R56 243/F_4

VRAM_DDR3_SAMSUNG_64MX16

+1.5V_GFX

[15] VMA_CLK1
[15] VMA_CLK1#
[15] FBA_CMD19

[15] FBA_CMD18
[15] FBA_CMD16

VMA_WDQS5 / VMA_RDQS5
VMA_DM5 / VMA_DM4
VMA_WDQS4 / VMA_RDQS4
VMA_ZQ3

R45 243/F_4

VMA_WDQS7 / VMA_RDQS7
VMA_DM7 / VMA_DM6
VMA_WDQS6 / VMA_RDQS6
VMA_ZQ4

R386 243/F_4

VMA_WDQS2 / VMA_RDQS2
VMA_DM3 / VMA_DM2
VMA_ZQ2

R433 243/F_4

[15] FBA_CMD17
[15] FBA_CMD1

TP3
TP10

VMA_CLK0
R429
162/F_4
VMA_CLK0#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

VMA_CLK1
R46
162/F_4
VMA_CLK1#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R392 1.33K/F_4
R393 1.33K/F_4
C608 0.1U/10V_4
VREFC_VMA1

R436 1.33K/F_4
R431 1.33K/F_4
C650 0.1U/10V_4
VREFD_VMA1

R385 1.33K/F_4
R384 1.33K/F_4
C604 0.1U/10V_4
VREFC_VMA3

R368 1.33K/F_4
R370 1.33K/F_4
C589 0.1U/10V_4
VREFD_VMA3

[15,18,20,38] +1.5V_GFX

C131 1U/6.3V_4
C603 1U/6.3V_4
C605 1U/6.3V_4
C610 1U/6.3V_4

C607 10U/6.3V_6
C593 1U/6.3V_4
C591 1U/6.3V_4
C611 1U/6.3V_4
C588 1U/6.3V_4
C57 1U/6.3V_4

C122 10U/6.3V_6
C592 1U/6.3V_4
C205 1U/6.3V_4
C612 1U/6.3V_4
C646 1U/6.3V_4
C132 1U/6.3V_4
C206 1U/6.3V_4
C609 1U/6.3V_4

C652 10U/6.3V_6
C90 10U/6.3V_6
C55 0.1U/10V_4
C133 0.1U/10V_4
C93 0.1U/10V_4
C134 0.1U/10V_4
C56 0.1U/10V_4

C651 10U/6.3V_6
C54 10U/6.3V_6
C207 0.1U/10V_4
C594 0.1U/10V_4
C590 0.1U/10V_4

NB5

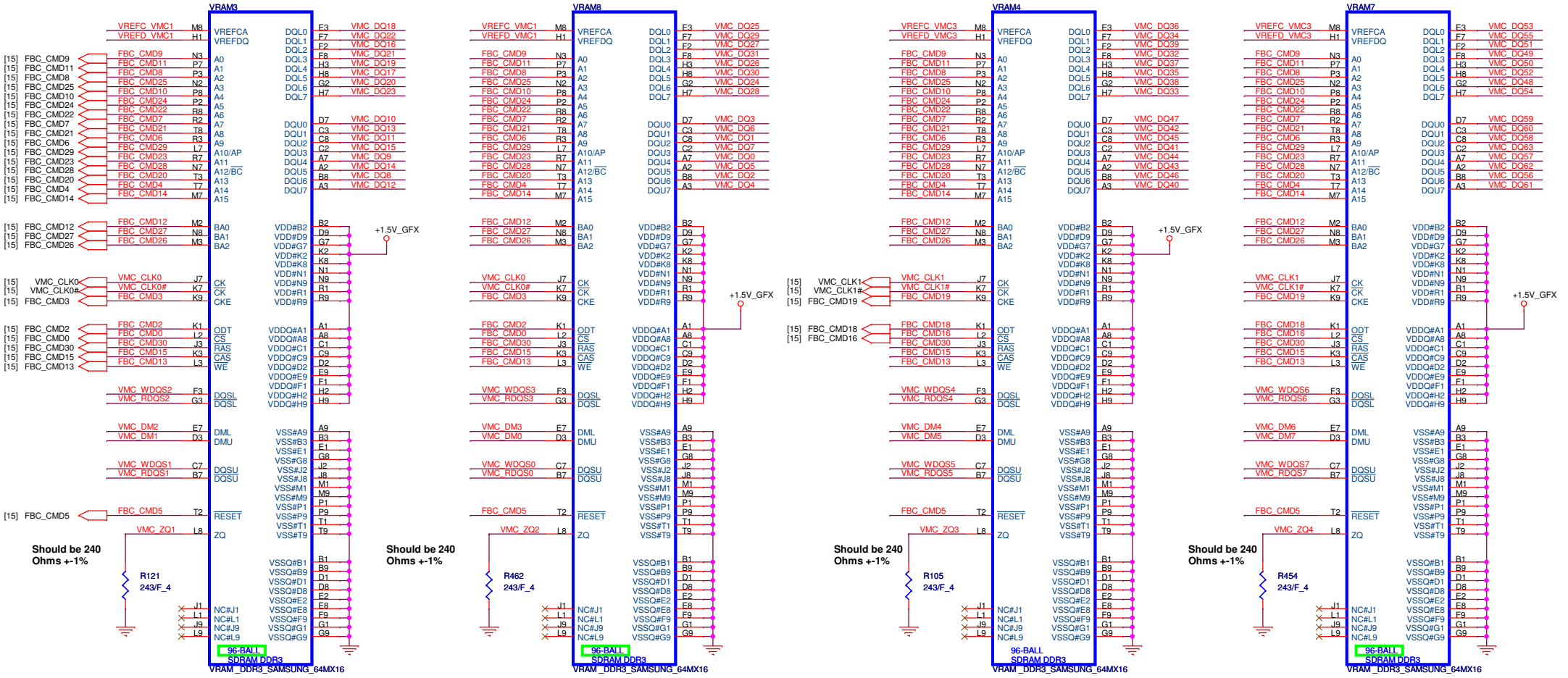
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU Memory 1/2 (DDR3)	1A

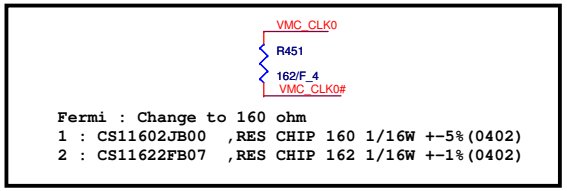
Date: Tuesday, March 27, 2012 | Sheet 19 of 42

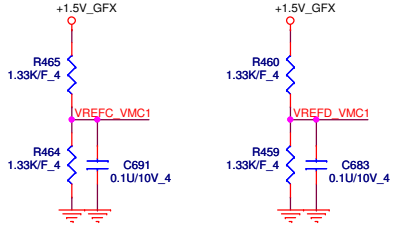
CHANNEL B: 256MB/512MB DDR3

[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

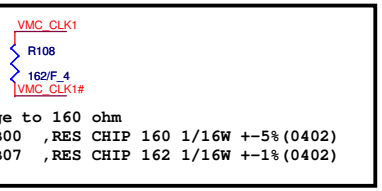


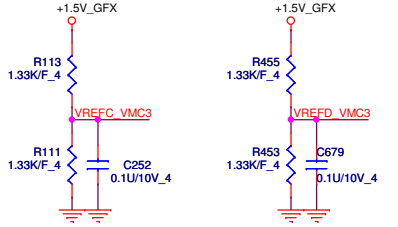
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

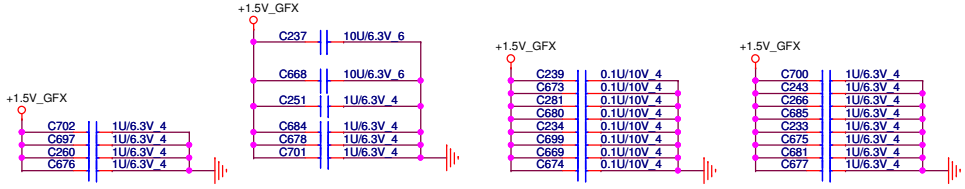




Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)







[15] FBC_CMD17 — FBC_CMD17 — TP19
[15] FBC_CMD1 — FBC_CMD1 — TP20

900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

[15,18,19,38] +1.5V_GFX

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU Memory 2/2 (DDR3)	1A
Date: Tuesday, March 27, 2012	Sheet 20 of 42	

USB Camera Connector

MIC

[23] DIGITAL_D1
[23] DIGITAL_CLK

L26 FCM1608KF-301T02/S DIGITAL_D1_R
L25 FCM1608KF-301T02/S DIGITAL_CLK_R

R283 0_4
R307 0_4

[8] USBP2-
[8] USBP2+

CAMERA

L1 *WCM2012-90

USBP2-_R
USBP2+_R

C576 100P/50V_4
C575 100P/50V_4

EMI request

C37 *10P/50V_4 USBP2-_R
C44 *10P/50V_4 USBP2+_R
C582 33P/50V_4 DIGITAL_D1
C581 33P/50V_4 DIGITAL_CLK

+3V
C42 0.01U/16V_4
C573 *4.7U/6.3V_6

Change from +5V to +3V

+3V
R30 2.2K_4
R29 2.2K_4

[6] PCH_EDIDCLK
[6] PCH_EDIDDATA

PCH_EDIDCLK
PCH_EDIDDATA

CN1

+3VLCD_CON
+3V
C41 1000P/50V_4

PCH_EDIDCLK
PCH_EDIDDATA
PCH_LA_DATAN0
PCH_LA_DATAP0
PCH_LA_DATAN1
PCH_LA_DATAP1
PCH_LA_DATAN2
PCH_LA_DATAP2
PCH_LA_CLK#
PCH_LA_CLK
PCH_LB_DATAN0
PCH_LB_DATAP0
PCH_LB_DATAN1
PCH_LB_DATAP1
PCH_LB_DATAN2
PCH_LB_DATAP2
PCH_LB_CLK#
PCH_LB_CLK
DIGITAL_D1_R
DIGITAL_CLK_R
USBP2-_R
USBP2+_R
PCH_DPST_PWM_R
BLON_CON
+VIN_BLIGHT

GS12407-11141-9F

Change from +5V to +3V

[6] PCH_DPST_PWM
R363 1K/F_4
C578 22P/50V_4

+3V
C580 1U/6.3V_4
U12
IN
IN
ON/OFF
OUT
GND
IC(5P) G5243AT11U
+LCDVCC
L22 TI160808U600/S
+3VLCD_CON
C43 *10U/6.3V_6
C40 *0.01U/16V_4
C39 0.1U/10V_4

[6] PCH_DISP_ON
PCH_DISP_ON
R361 100K/F_4

[29] LID_CONTROL
LID_CONTROL
D19 RB500V-40
R362 100K/F_4
C577 22P/50V_4
BLON_CON
R360 47K/F_4
+3VPCU
[6] PCH_LVDS_BLON
PCH_LVDS_BLON
R365 1K/F_4
D20 *RB500V-40
LID_EC# [28,29]
R364 100K/F_4

[8] LCD_BK
Q30 *DTC144EUA

+VIN_BLIGHT
+VIN
L24 *TI160808U600/S
L23 TI160808U600/S
C574 0.1U/50V_6
C579 *4.7U/25V_8
C583 0.1U/50V_6
C584 0.01U/25V_4

EMI/ESD

Stitching Cap(each 1" place one cap)

+5V
C142 0.1U/10V_4
C58 0.1U/10V_4
C443 0.1U/10V_4
C253 0.1U/10V_4
C570 0.1U/10V_4
C560 0.1U/10V_4

+3VS5
C545 0.1U/10V_4
C352 0.1U/10V_4
C542 0.1U/10V_4
C523 0.1U/10V_4
C531 0.1U/10V_4
C534 0.1U/10V_4

+3V
C193 0.1U/10V_4
C333 0.1U/10V_4
C229 0.1U/10V_4
C303 0.1U/10V_4
C516 0.1U/10V_4
C507 0.1U/10V_4

+5V
C564 0.1U/10V_4
C241 0.1U/10V_4
C400 0.1U/10V_4
C561 0.1U/10V_4
C563 0.1U/10V_4
C191 0.1U/10V_4

+5VS5

+3VS5
C553 0.1U/10V_4
C548 0.1U/10V_4
C351 0.1U/10V_4
C556 0.1U/10V_4
C557 0.1U/10V_4
C712 0.1U/10V_4

+5VS5

+VIN
C725 0.1U/25V_4
C726 0.1U/25V_4
C727 0.1U/25V_4
C728 0.1U/25V_4

[6,7,8,9,10,12,13,14,18,22,23,24,25,27,28,29,30,35,37,39,41] +3V
[7,26,27,28,29,31,32] +3VPCU
[7,10,22,23,27,28,41] +5V
[31,32,33,35,37,38,40,41] +VIN
[38,41] +12VALW
[10,23,26,32,33,34,35,37,39,40,41] +5VS5

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD Connector (LVDS)	A
Date: Tuesday, March 27, 2012	Sheet 21 of 42	

CRT PORT

40 MIL

40 mil F1 FUSE1A6V_POLY +5V +5VCRT +5VCRT
C139 0.1U/10V_4
SSM14 spec is 40V 1A

[6] PCH_CRT_R
[6] PCH_CRT_G
[6] PCH_CRT_B
L5 BK1608LL680 CRT_R_CON
L4 BK1608LL680 CRT_G_CON
L3 BK1608LL680 CRT_B_CON
R63 150/F_4
R59 150/F_4
R54 150/F_4
C180 6.8P/50V_4
C158 6.8P/50V_4
C121 6.8P/50V_4
C120 6.8P/50V_4
C160 6.8P/50V_4
C186 6.8P/50V_4
EMI
+5VCRT
CRT CONN CN12

C602 .1U/10V_4
[6] PCH_VSYNC PCH_VSYNC
U13 M74VHC1GT125DF2G
[6] PCH_HSYNC PCH_HSYNC
U14 M74VHC1GT125DF2G
CRTVSYNC1 R390 *0_4/S CRTVSYNC2
CRTHSYNC1 R394 *0_4/S CRTHSYNC2
R51 *0_4/S DDCCLK3
R402 *0_4/S DDCDAT3

+3V R48 10K/F_4
[6] PCH_DDCCLK
C169 .1U/10V_4
Q9 ME2N7002D
DDCCLK2
+3V R413 10K/F_4
[6] PCH_DDCDATA
C95 .1U/10V_4
Q32 ME2N7002D
DDCDATA2
R47 2.2K_4
R395 2.2K_4
D23 RB500V-40 +5VCRT +5V_CRT2

PCH_CRT_R PCH_CRT_G PCH_CRT_B DDCCLK3 DDCDAT3 CRTHSYNC2 CRTVSYNC2
D5 *BAV99W
D4 *BAV99W
D3 *BAV99W
D2 *BAV99W
D26 *BAV99W
D25 *BAV99W
D24 *BAV99W
+3V +5V

C91 *470P/50V_4
C606 *47P/50V_6
C615 *470P/50V_4
C617 *47P/50V_6

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

HDMI PORT

HDMI SMBus Isolation

+3V R177 2.2K_4 Q17
[6] SDVO_CLK HDMI_SCL_R HDMI_SCLK
[6] SDVO_DATA HDMI_SDA_R HDMI_SDATA
+3V R194 2.2K_4
2N7002DW
Close to HDMI connector

EMI Solution

C_TX2_HDMI+ R156 *150/F_4 C_TX2_HDMI-
C_TX1_HDMI+ R139 *150/F_4 C_TX1_HDMI-
C_TX0_HDMI+ R145 *150/F_4 C_TX0_HDMI-
C_IN_CLK R131 *150/F_4 C_IN_CLK#
R128 0_4
C_IN_CLK# C_IN_CLK RP1 *WCM2012-90 C_TXC_HDMI- C_TXC_HDMI+
R133 0_4

CN15
[6] IN_D2 IN_D2 C335 0.1U/10V_4 C_TX2_HDMI+
[6] IN_D2# IN_D1 C326 0.1U/10V_4 C_TX2_HDMI-
[6] IN_D1 C317 0.1U/10V_4 C_TX1_HDMI+
[6] IN_D1# IN_D1 C313 0.1U/10V_4 C_TX1_HDMI-
[6] IN_D0 IN_D0 C321 0.1U/10V_4 C_TX0_HDMI+
[6] IN_D0# IN_D0 C318 0.1U/10V_4 C_TX0_HDMI-
[6] IN_CLK IN_CLK C309 0.1U/10V_4 C_IN_CLK C_TXC_HDMI+
[6] IN_CLK# IN_CLK# C304 0.1U/10V_4 C_IN_CLK# C_TXC_HDMI-
RB500V-40
+5V D8 D7 RB500V-40 5V_HSMBCK 5V_HSMBDT
R137 2.2K_4
R136 2.2K_4
HDMI_SCLK HDMI_SDATA
C305 *10P/50V_4
C306 *10P/50V_4
+5VCRT
HDMI_HPD R123 *0_4/S HDMI_DET_C
C296 220P/50V_4
HDMI CONN_4 pin GND
add for EMI
D6 BAV99W
R130 110K/F_4
B-stage change

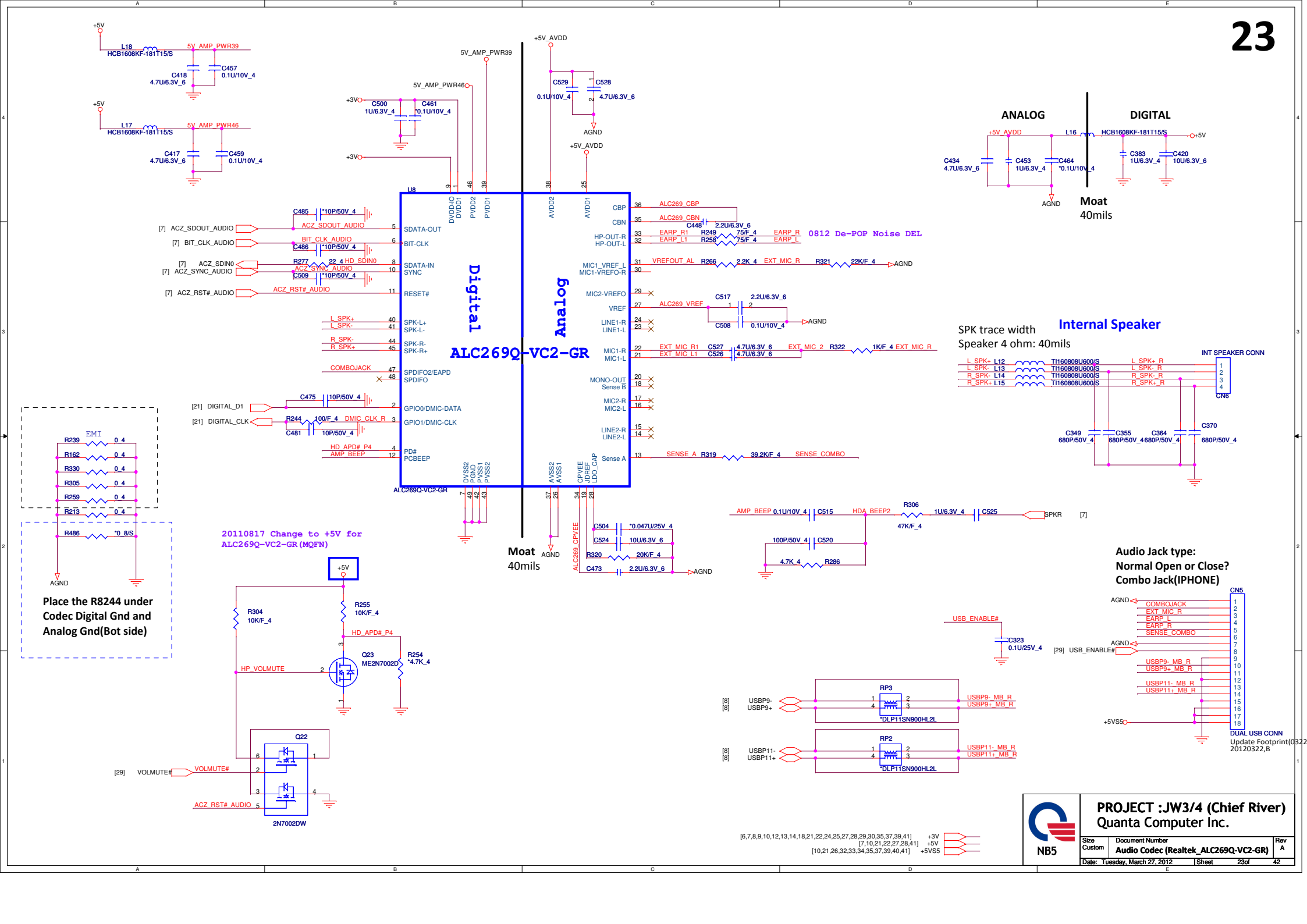
SHELL3 SHELL1 D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET SHELL2 SHELL4

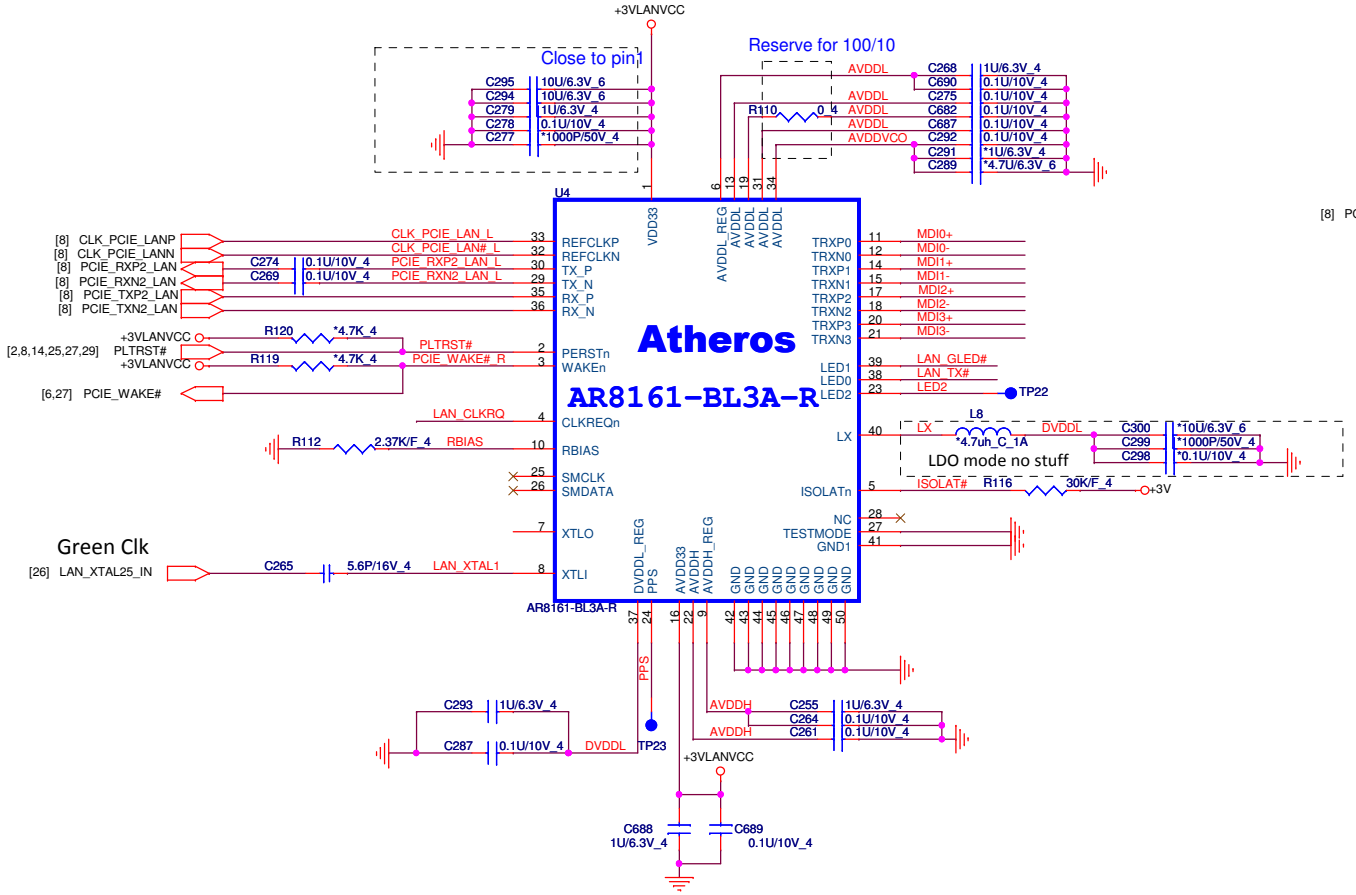
+3V DGPU_CL_HDMIP R158 680/F_4 C_TX2_HDMI+ R150 680/F_4 C_TX2_HDMI-
R140 680/F_4 C_TX1_HDMI+ R138 680/F_4 C_TX1_HDMI-
R148 680/F_4 C_TX0_HDMI+ R141 680/F_4 C_TX0_HDMI-
R134 680/F_4 C_IN_CLK R129 680/F_4 C_IN_CLK#
R184 100K/F_4 Q16 ME2N7002D
C348 0.1U/10V_4
Close to Q24

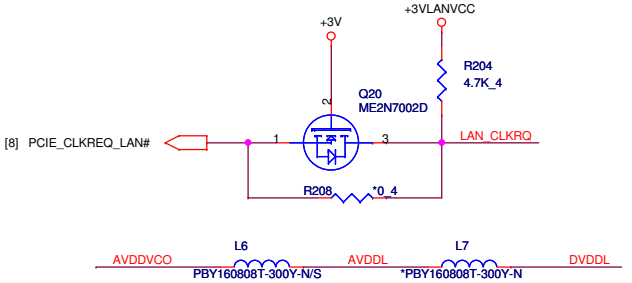
+3V Q14 MMBT3904-7-F HDMI_DET_P R126 150K/F_4 HDMI_HPD
[6] HDMI_HPD_CON HDMI_HPD_CON
R135 10K/F_4

+5VCRT C267 *0.01U/16V_4
for EMI request

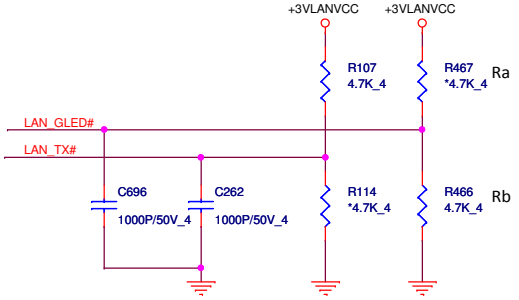
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.
NB5
Size Custom | Document Number CRT/HDMI Connector | Rev A
Date: Tuesday, March 27, 2012 | Sheet 22of 42

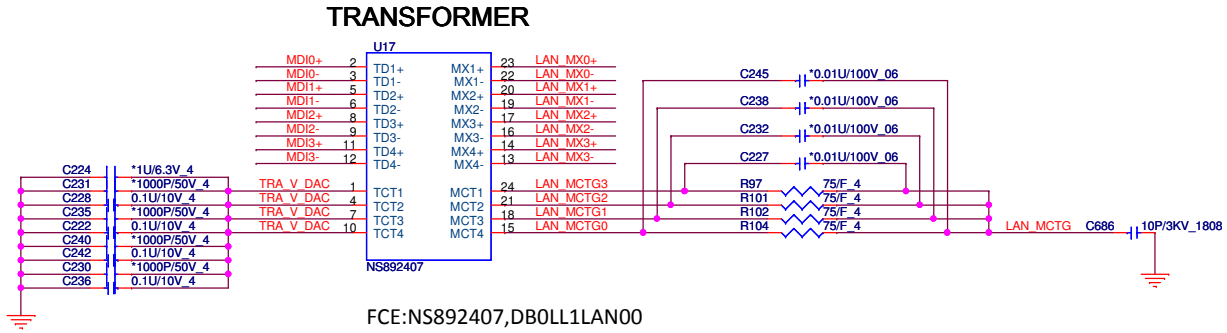

ALC269Q-VC2-GR
Digital
Analog
U8
ALC269Q-VC2-GR
Moat
40mils
ANALOG
DIGITAL
Moat
40mils
0812 De-POP Noise DEL
Internal Speaker
SPK trace width
Speaker 4 ohm: 40mils
INT SPEAKER CONN
CN6
EMI
Place the R8244 under
Codec Digital Gnd and
Analog Gnd(Bot side)
20110817 Change to +5V for
ALC269Q-VC2-GR(MQFN)
Audio Jack type:
Normal Open or Close?
Combo Jack(IPHONE)
CN5
DUAL USB CONN
Update Footprint(0322
20120322,B
2N7002DW
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.
NB5
Audio Codec (Realtek_ALC269Q-VC2-GR)
Tuesday, March 27, 2012





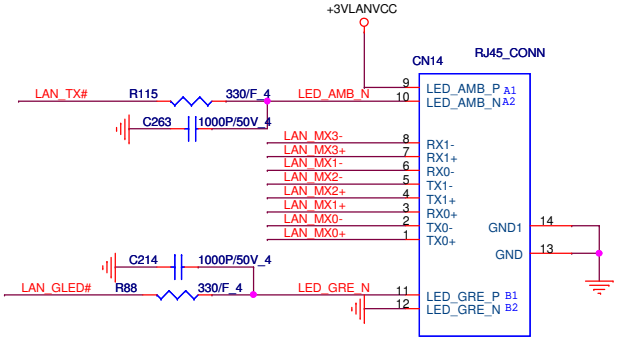
LDO mode:	
Rb(R5208)	**Stuff**
L5006	No stuff
L5004	No stuff
C5291	No stuff
C5293.	No stuff
C5294	No stuff
Ra(R5210)	No stuff





FCE:NS892407,DB0LL1LAN00

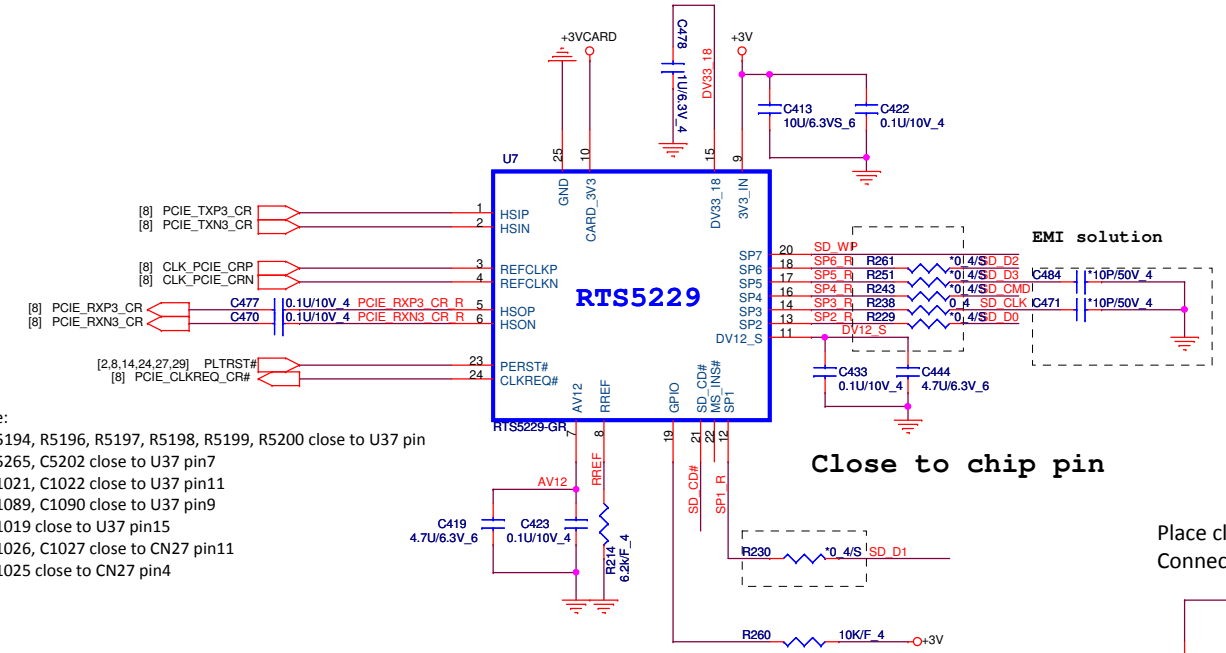
BOT:GST5009B LF,DB0Z06LAN00



NB5

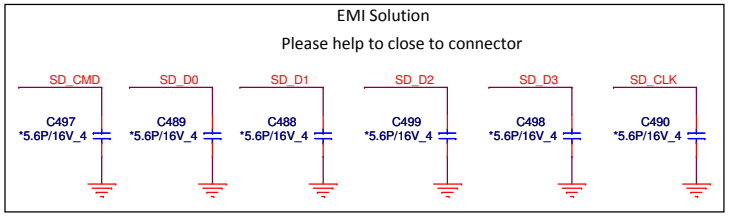
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

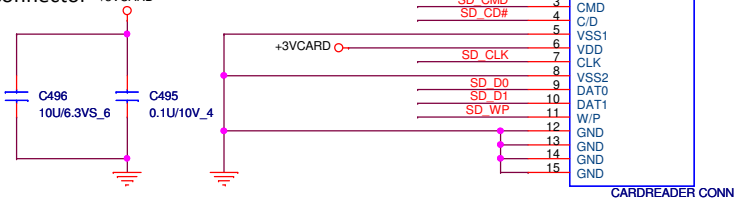
Size	Document Number	Rev
Custom	LAN Controller (Atheros_AR8161)	A
Date: Tuesday, March 27, 2012	Sheet 24of 42	



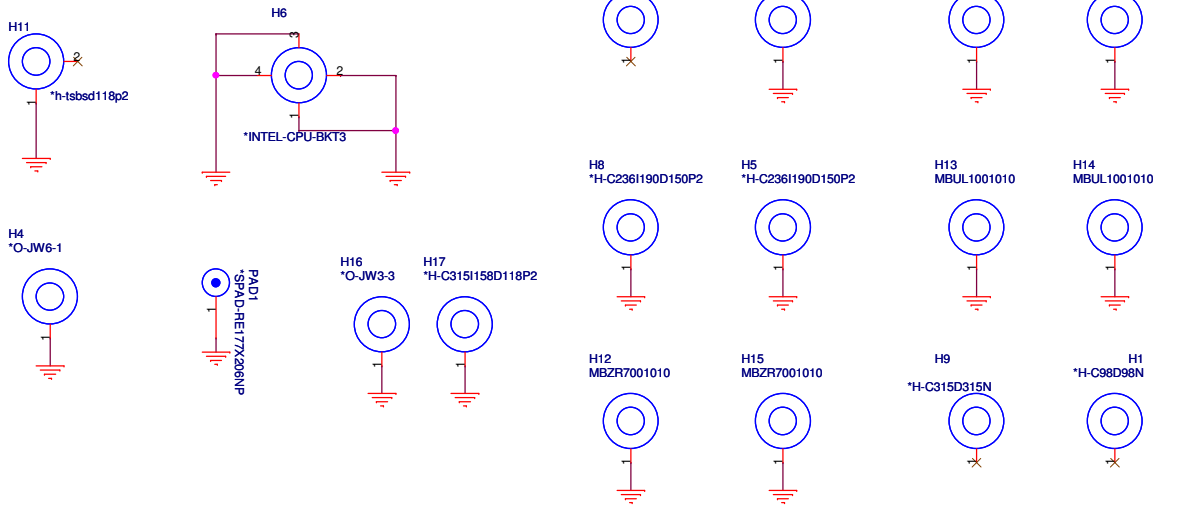
Note:
1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4

Share Pin





CPU Bracket



NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Card Reader control (RTS5229-GR)	A
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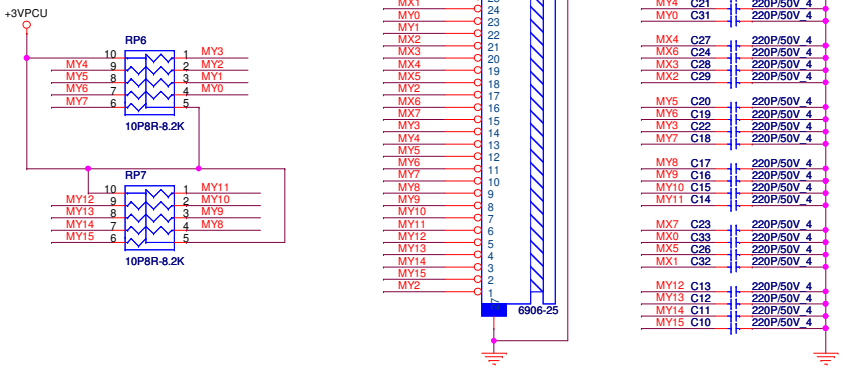
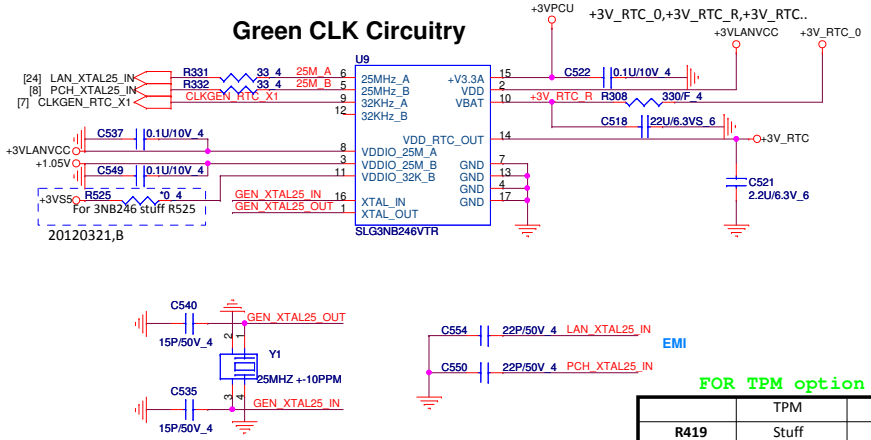
Keyboard Connector



Green CLK Circuitry

20mils width(min)
+3V_RTC_0,+3V_RTC_R,+3V_RTC..

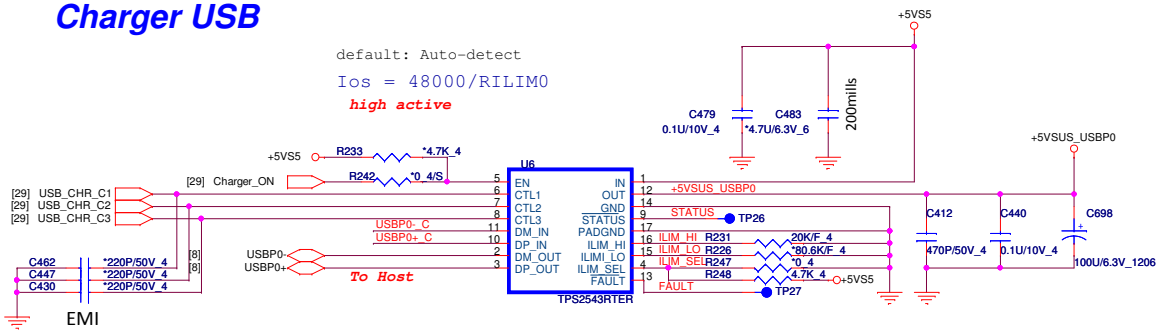


FOR TPM option

	TPM	Non-TPM
R419	Stuff	NA
U5	AL3NB246000	AL3NB244000

Charger USB

default: Auto-detect
Ios = 48000/RILIM0
high active



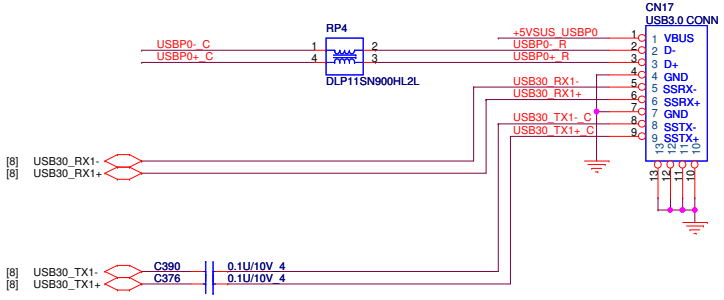
TPS2543/45 Control Truth Table

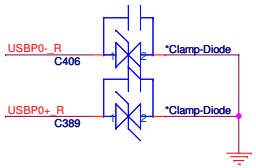
CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	1	Discharge	NA	off
0	0	1	1	DCP/auto	IOS_PW & ILIM_HI (1)	DCP load present
0	1	0	1	SDP	ILIM_HI	off
0	1	1	1	DCP/auto	ILIM_HI	DCP load present
1	1	0	1	SDP	ILIM_HI	off
1	1	1	1	CDP	ILIM_HI	CDP load present

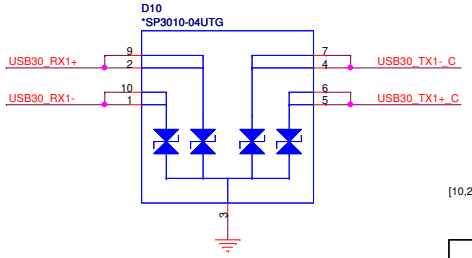
(1) ILIM_HI: 20K(R5233), 2.4A

USB3.0 X 1/USB2.0 COMBO

USB 3.0







[10,21,23,32,33,34,35,37,39,40,41] +5VS5
[7,21,27,28,29,31,32] +3VPCU

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB 3.0/KB/Green CLK	A
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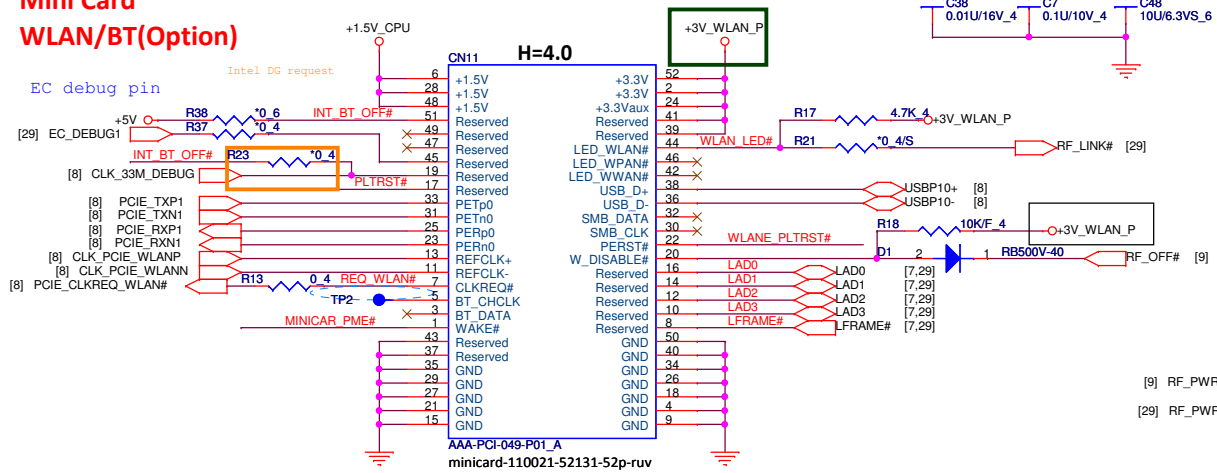
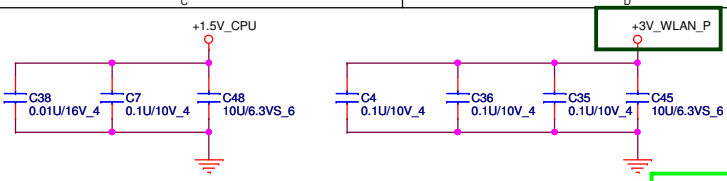
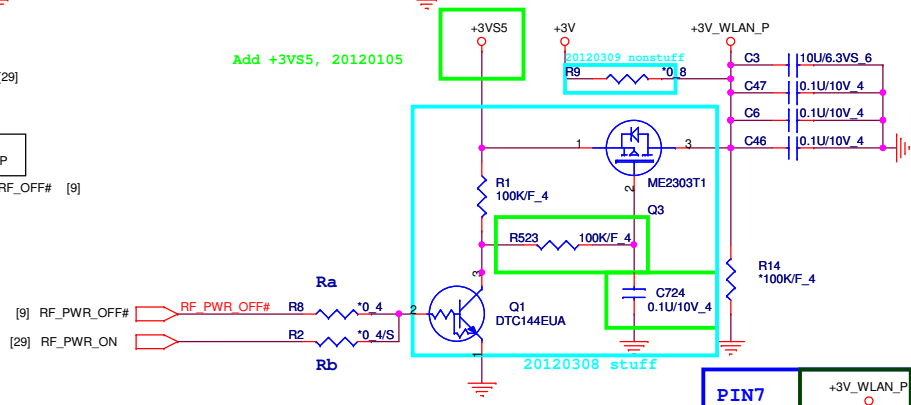
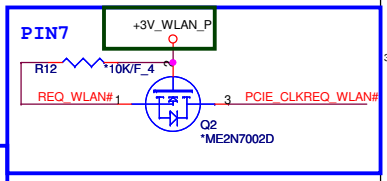
Mini Card WLAN/BT(Option)

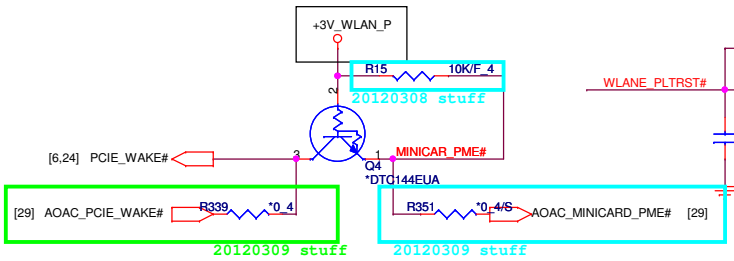






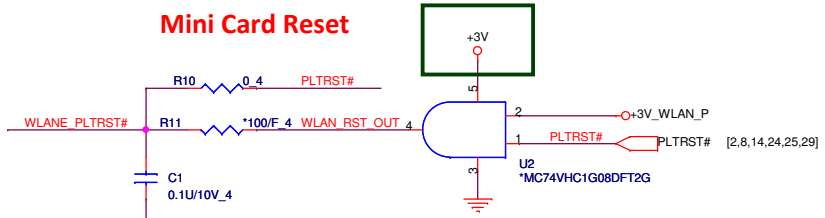


Support Wake Function(Reserve)

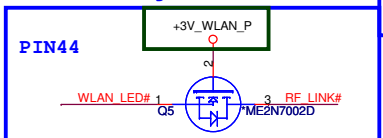


Add for AOAC

Mini Card Reset



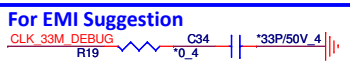
Avoid leakage issue



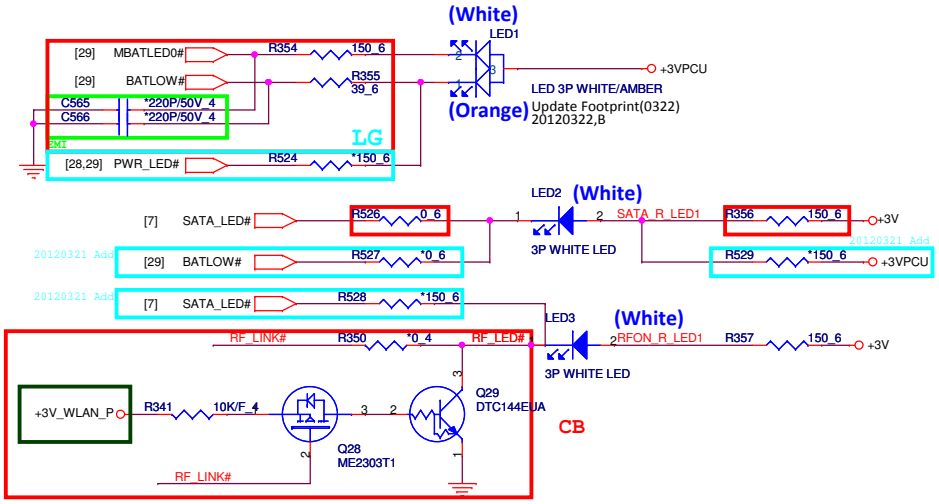
LGE mini-pcie power status

WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

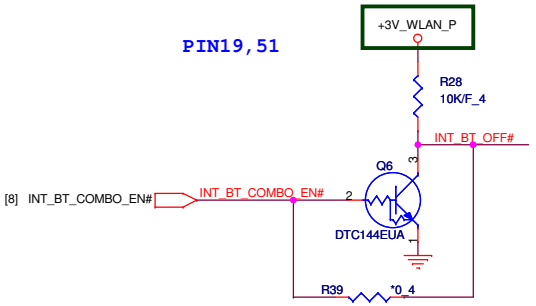
For EMI Suggestion



LED Status



PIN19, 51



9/4 Intel COMBO card control circuit
1.add R1001,R1002,Q1001
2.add net name"INT_BT_COMBO_EN#" -> "INT_BT_OFF#"

[6,7,8,9,10,12,13,14,18,21,22,23,24,25,28,29,30,35,37,39,41] +3V
[7,10,21,22,23,28,41] +5V
[7,21,26,28,29,31,32] +3VPCU
[2,4,10,28] +1.5V_CPU

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-PCIE/LED	A
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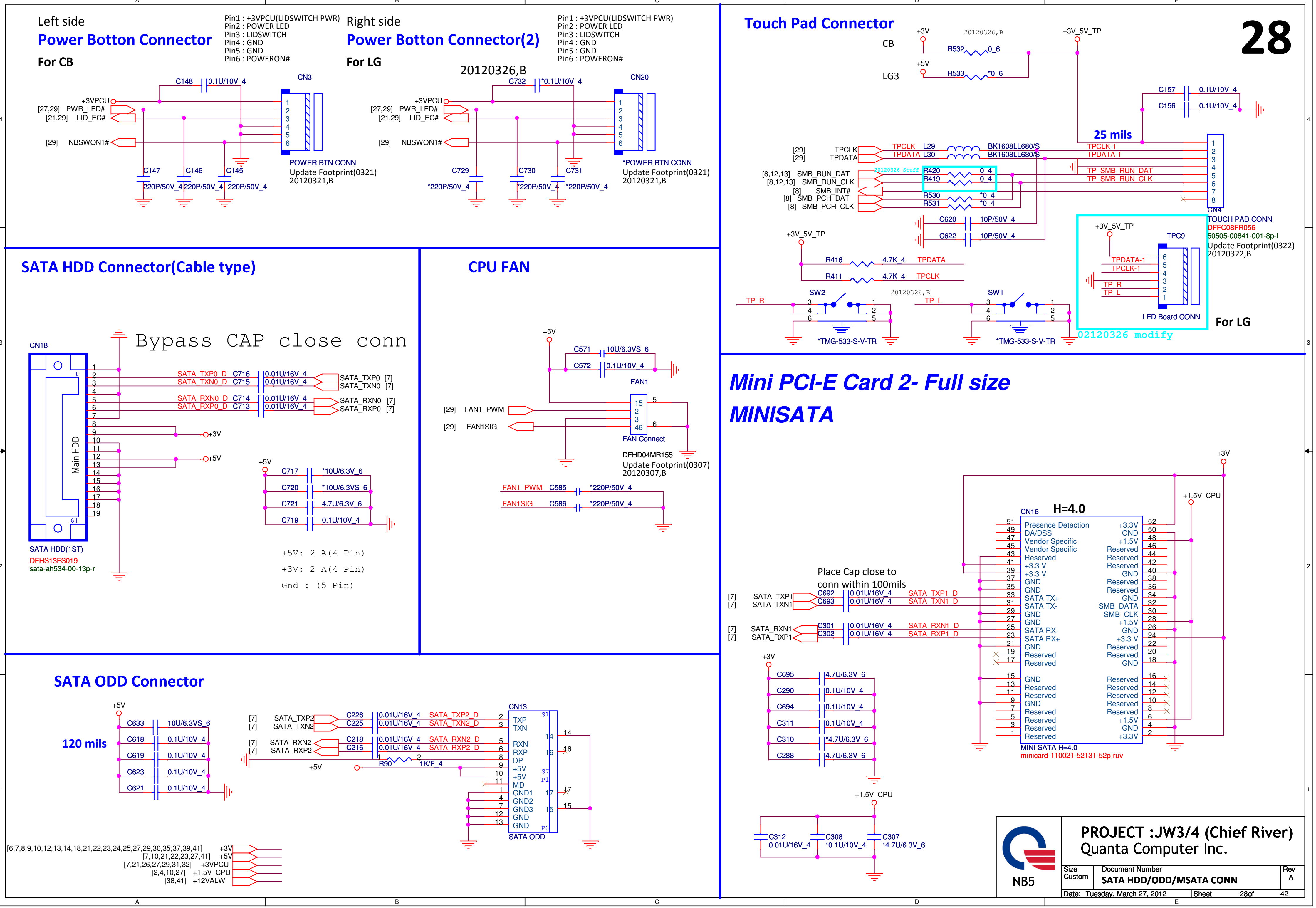

28
Left side
Power Botton Connector
For CB
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#
Right side
Power Botton Connector(2)
For LG
20120326,B
+3VPCU
[27,29] PWR_LED#
[21,29] LID_EC#
[29] NBSWON1#
C148 0.1U/10V_4
CN3
C147 C146 C145
220P/50V_4 220P/50V_4 220P/50V_4
POWER BTN CONN
Update Footprint(0321)
20120321,B
C732 *0.1U/10V_4
CN20
C729 C730 C731
*220P/50V_4 *220P/50V_4 *220P/50V_4
*POWER BTN CONN
Update Footprint(0321)
20120321,B
Touch Pad Connector
CB
LG3
+3V
+5V
R532 0_6
R533 *0_6
20120326,B
+3V_5V_TP
C157 0.1U/10V_4
C156 0.1U/10V_4
25 mils
[29] TPCLK
[29] TPDATA
L29 BK1608LL680/S
L30 BK1608LL680/S
TPCLK-1
TPDATA-1
[8,12,13] SMB_RUN_DAT
[8,12,13] SMB_RUN_CLK
[8] SMB_INT#
[8] SMB_PCH_DAT
[8] SMB_PCH_CLK
20120326 Stuff
R420 0_4
R419 0_4
R530 *0_4
R531 *0_4
TP_SMB_RUN_DAT
TP_SMB_RUN_CLK
CN4
TOUCH PAD CONN
DFFC08FR056
50505-00841-001-8p-l
Update Footprint(0322)
20120322,B
C620 10P/50V_4
C622 10P/50V_4
R416 4.7K_4 TPDATA
R411 4.7K_4 TPCLK
TPC9
TPDATA-1
TPCLK-1
TP_R
TP_L
LED Board CONN
For LG
02120326 modify
SW2
SW1
20120326,B
*TMG-533-S-V-TR
*TMG-533-S-V-TR
SATA HDD Connector(Cable type)
Bypass CAP close conn
CN18
SATA_TXP0_D C716 0.01U/16V_4 SATA_TXP0 [7]
SATA_TXN0_D C715 0.01U/16V_4 SATA_TXN0 [7]
SATA_RXN0_D C714 0.01U/16V_4 SATA_RXN0 [7]
SATA_RXP0_D C713 0.01U/16V_4 SATA_RXP0 [7]
+3V
+5V
Main HDD
SATA HDD(1ST)
DFHS13FS019
sata-ah534-00-13p-r
C717 *10U/6.3V_6
C720 *10U/6.3VS_6
C721 4.7U/6.3V_6
C719 0.1U/10V_4
+5V: 2 A(4 Pin)
+3V: 2 A(4 Pin)
Gnd : (5 Pin)
CPU FAN
C571 10U/6.3VS_6
C572 0.1U/10V_4
FAN1
[29] FAN1_PWM
[29] FAN1SIG
FAN Connect
DFHD04MR155
Update Footprint(0307)
20120307,B
FAN1_PWM C585 *220P/50V_4
FAN1SIG C586 *220P/50V_4
Mini PCI-E Card 2- Full size
MINISATA
+3V
+1.5V_CPU
CN16
H=4.0
Presence Detection, DA/DSS, Vendor Specific, Vendor Specific, Reserved, +3.3 V, +3.3 V, GND, GND, SATA TX+, SATA TX-, GND, GND, SATA RX-, SATA RX+, GND, Reserved, Reserved
+3.3V, GND, +1.5V, Reserved, Reserved, Reserved, GND, Reserved, Reserved, GND, SMB_DATA, SMB_CLK, +1.5V, GND, +3.3 V, Reserved, Reserved, GND
GND, Reserved, Reserved, GND, Reserved, Reserved, Reserved, Reserved
Reserved, Reserved, Reserved, Reserved, Reserved, +1.5V, GND, +3.3V
MINI SATA H=4.0
minicard-110021-52131-52p-ruv
Place Cap close to
conn within 100mils
[7] SATA_TXP1 C692 0.01U/16V_4 SATA_TXP1_D
[7] SATA_TXN1 C693 0.01U/16V_4 SATA_TXN1_D
[7] SATA_RXN1 C301 0.01U/16V_4 SATA_RXN1_D
[7] SATA_RXP1 C302 0.01U/16V_4 SATA_RXP1_D
C695 4.7U/6.3V_6
C290 0.1U/10V_4
C694 0.1U/10V_4
C311 0.1U/10V_4
C310 *4.7U/6.3V_6
C288 4.7U/6.3V_6
C312 0.01U/16V_4
C308 *0.1U/10V_4
C307 *4.7U/6.3V_6
SATA ODD Connector
120 mils
C633 10U/6.3VS_6
C618 0.1U/10V_4
C619 0.1U/10V_4
C623 0.1U/10V_4
C621 0.1U/10V_4
[7] SATA_TXP2 C226 0.01U/16V_4 SATA_TXP2_D
[7] SATA_TXN2 C225 0.01U/16V_4 SATA_TXN2_D
[7] SATA_RXN2 C218 0.01U/16V_4 SATA_RXN2_D
[7] SATA_RXP2 C216 0.01U/16V_4 SATA_RXP2_D
R90 1K/F_4
CN13
TXP, TXN, RXN, RXP, DP, +5V, +5V, MD, GND1, GND2, GND3, GND, GND
SATA ODD
[6,7,8,9,10,12,13,14,18,21,22,23,24,25,27,29,30,35,37,39,41] +3V
[7,10,21,22,23,27,41] +5V
[7,21,26,27,29,31,32] +3VPCU
[2,4,10,27] +1.5V_CPU
[38,41] +12VALW
NB5
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.
Size Custom
Document Number
SATA HDD/ODD/MSATA CONN
Rev A
Date: Tuesday, March 27, 2012
Sheet 28 of 42

20110818
RTC XTAL DEL

Select Pin

Vpro Select	
Vpro	Ra
Non-Vpro	Rb

Select Pin

CB/LG Select	
LG	Ra
CB	Rb

Layout Note:
Place all capacitors close to IT8502N.

IT8518E/HX

LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK

2011 12 05 : Change to CX8BA121000

2011 11 30 : Delete net"Cap_int" for non-Capacity function

For Battery charge

For PCH SMB/DDR Thermal IC/VGA and Cap board

2011 12 01 :Add USB_CHR_C2

0815 DEL PC_BEEP_EC

LAN_S5_WAKE#

9/15 Modify for EC

Platfrom	ADC
JW6/7	0V
Reserve	0.75V
Reserve	1.5V
Reserve	2.25V
JW3	3V

thermal shutdown circuit

Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023

Socket : DG008000031

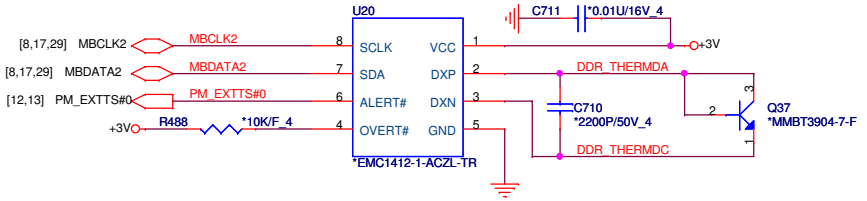
20110818 RTC XTAL DEL

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

NB5

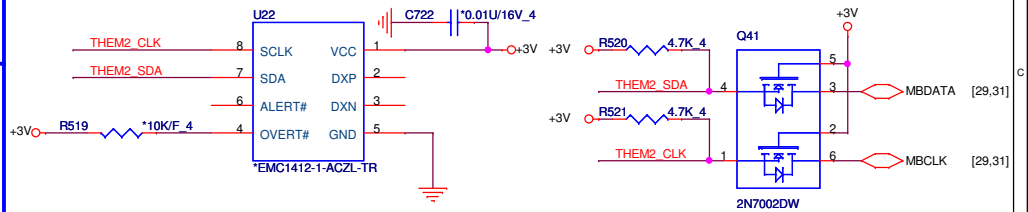
Size	Document Number	Rev
Custom	Embedded Controller (ITE_IT8518)	A
Date: Tuesday, March 27, 2012	Sheet 29of 42	

DDR3 Thermal Sensor

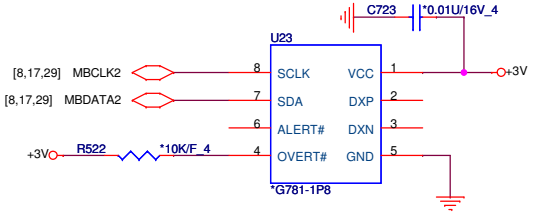


Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

Thermal Solution(Close to CRT)

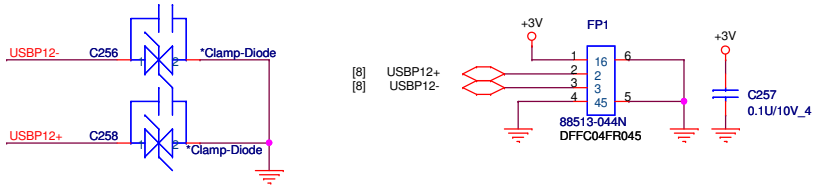


Thermal Solution(Close to GPU)

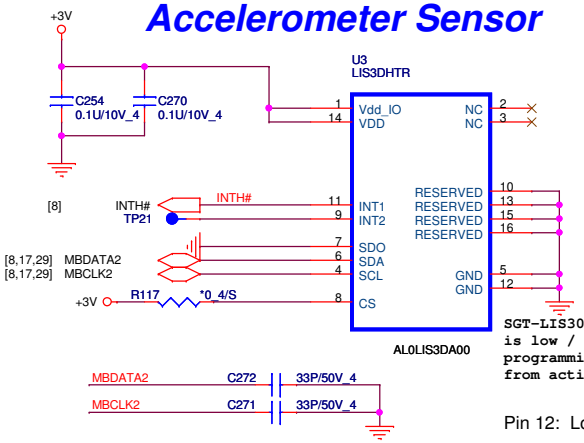


Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Finger Printer



Accelerometer Sensor



SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

Pin 12: Low 38hex
Pin 12: unconnected/floating 3Ahex

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	G-SENSOR	1A
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TOP DC_JACK
90W/4.75A

IDEA diode for shipmode only

Place this ZVS close to idea diode

Do Not add test point on BATDIS_G signal

Kelvin Connections for the Current-Sense Resistors

Parallel routing

New Battery Pack
3S2P (2200mAH)

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

include charger boost function

Using Kevin connection for layout

Place this cap close to IC

Place this cap close to EC

Place this cap close to EC

For shipmode

EMI Suggestion

PU1
OZ8682

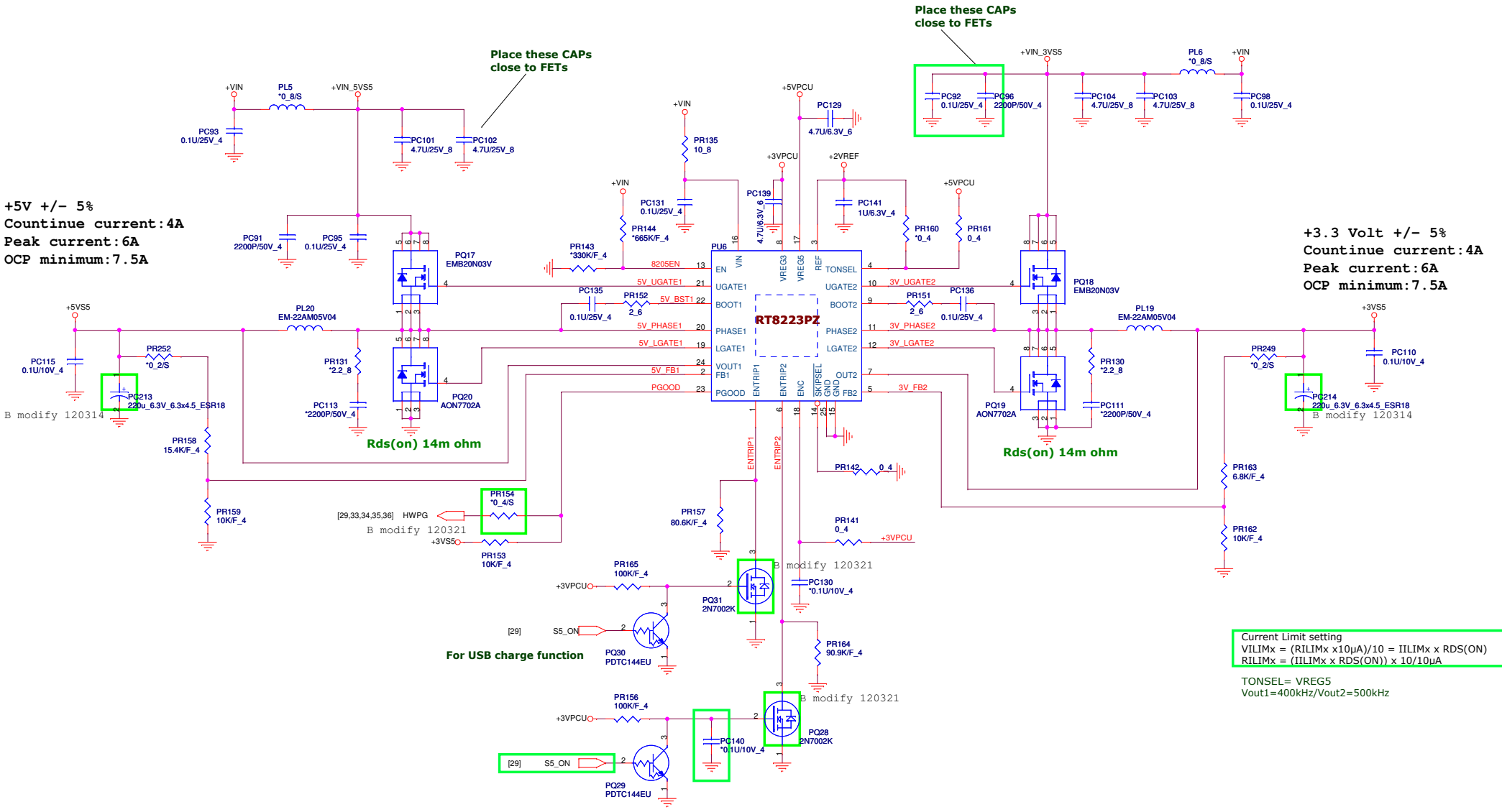
B modify 120314
B modify 120321

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Charger (OZ8682)	A
Date: Tuesday, March 27, 2012	Sheet 31of 42	

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

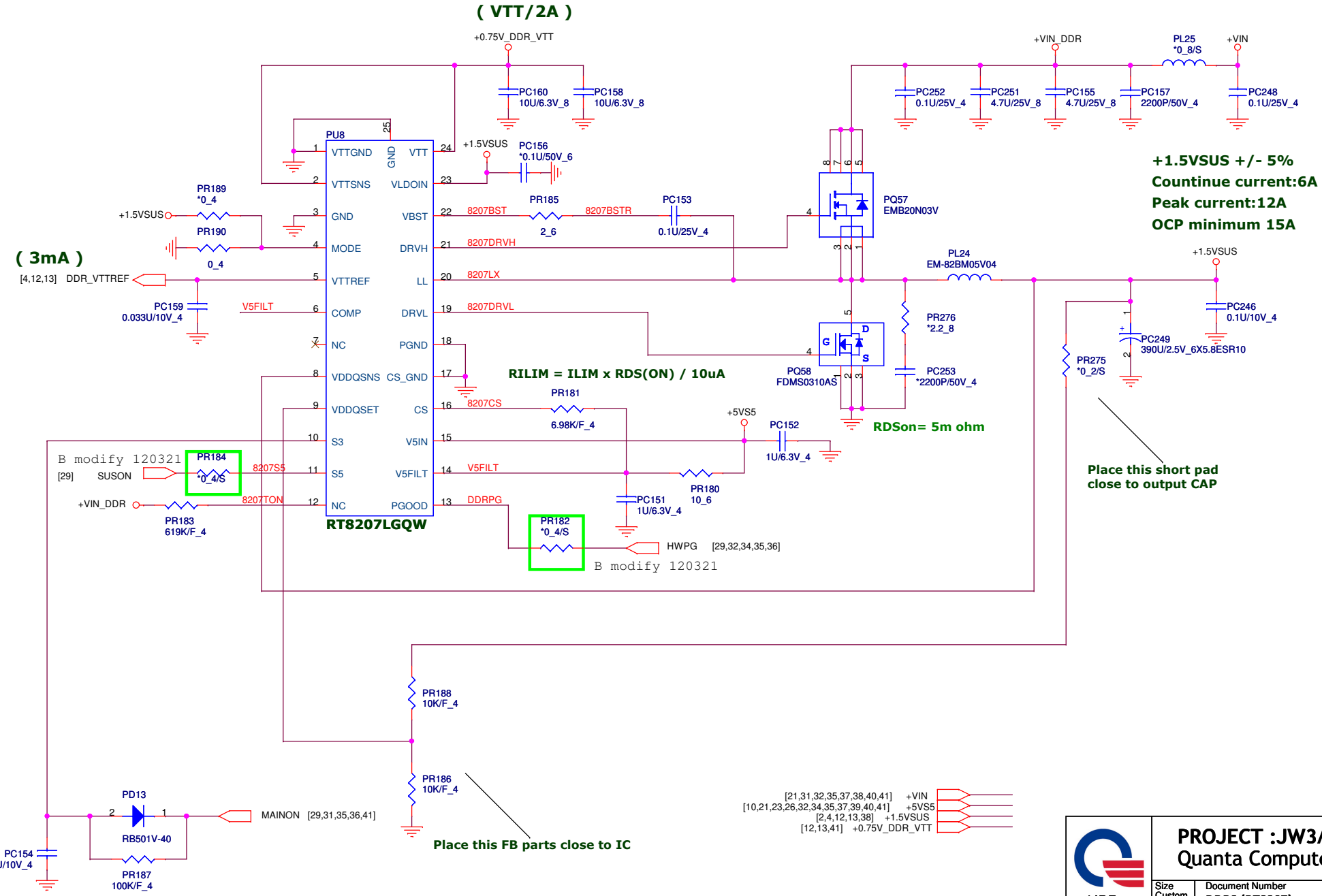


[21,31,33,35,37,38,40,41] +VIN
[6,7,8,9,10,21,26,27,29,35,36,38,41] +3VS5
[10,21,23,26,33,34,35,37,39,40,41] +5VS5
[7,21,26,27,28,29,31] +3VPCU

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (RT8223P)	A
Date: Tuesday, March 27, 2012	Sheet 32of 42	



NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	A
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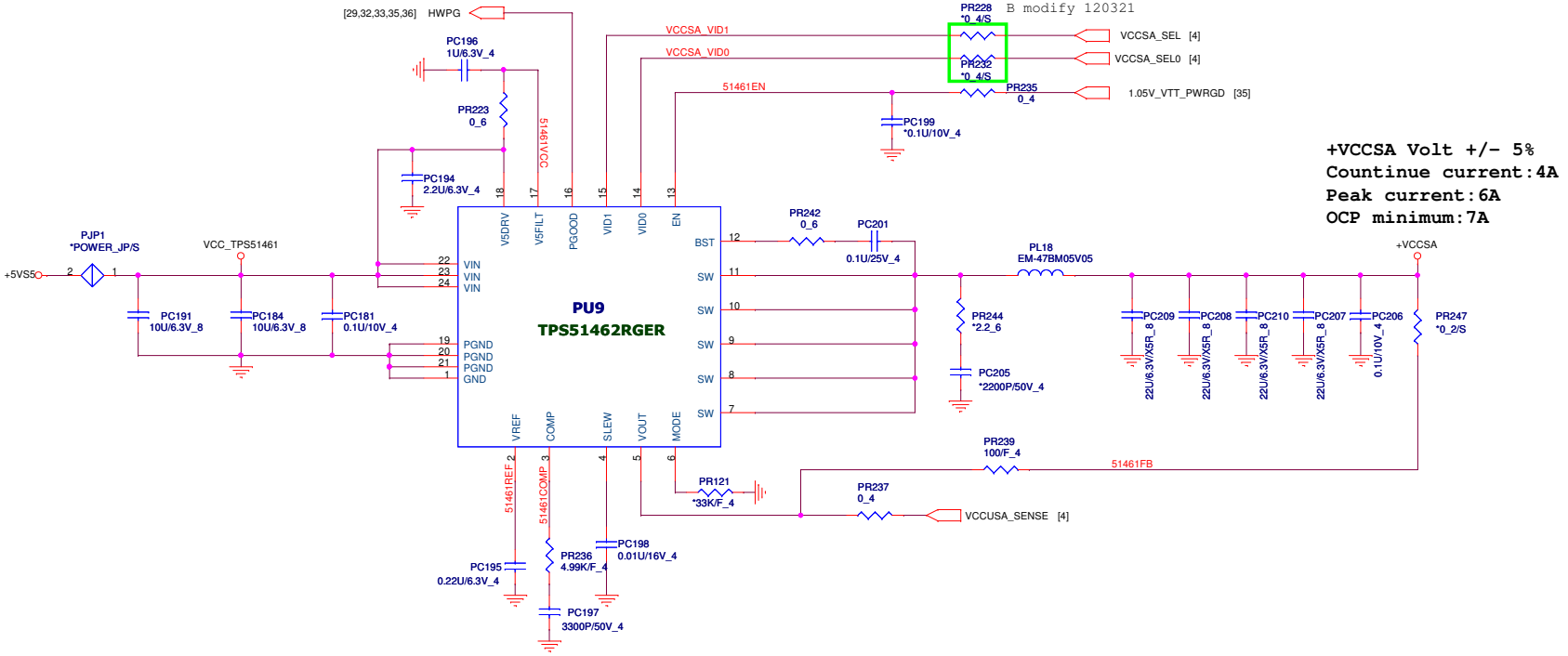
CPU system agent
voltage slew rate of 0.5 -10 mV/μs

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

TPS51462RGER for SV CPU



+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (TPS51462RGER)	A
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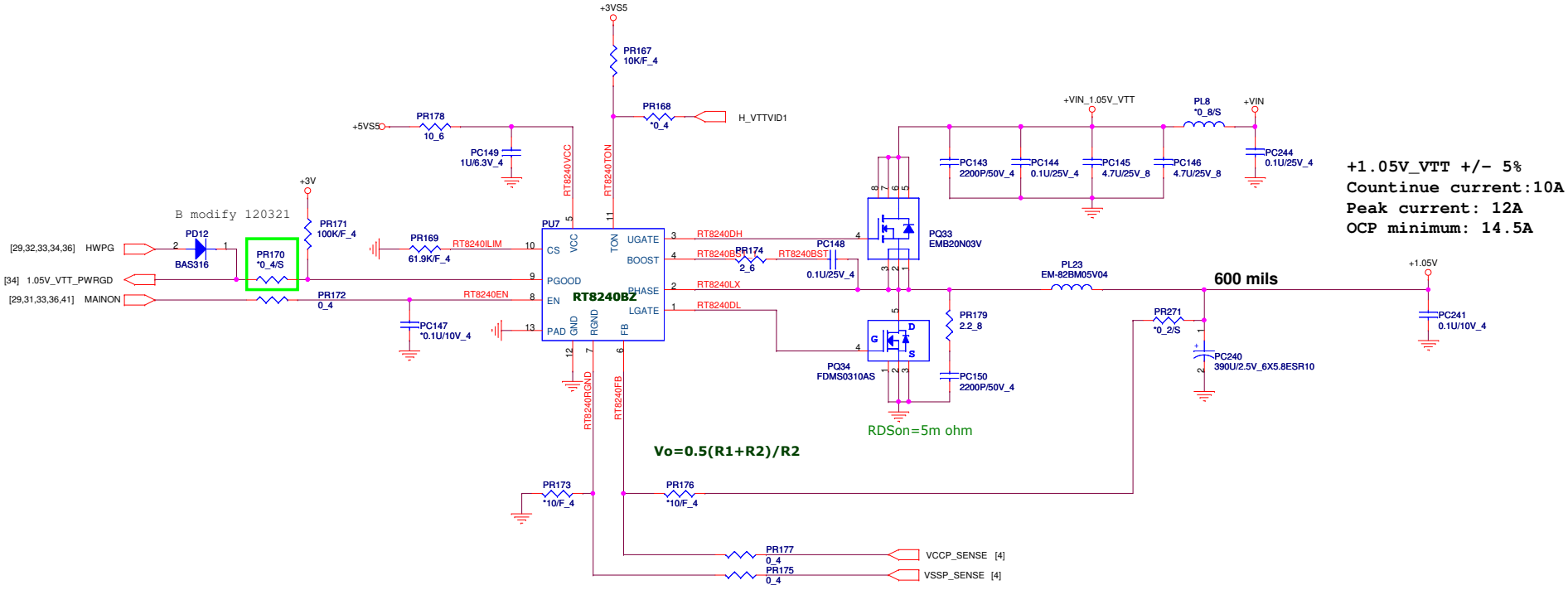
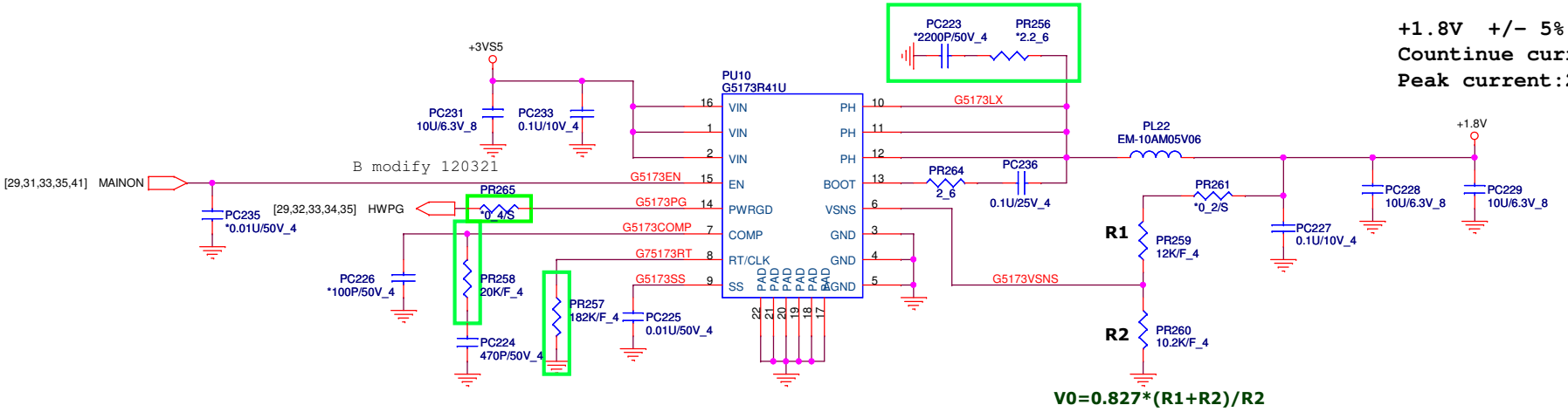


+1.05V_VTT +/- 5%
Countinue current:10A
Peak current: 12A
OCP minimum: 14.5A

NB5	PROJECT :JW3/4 (Chief River) Quanta Computer Inc.		
	Size: Custom	Document Number: +1.05V (RT8240B)	Rev: A
	Date: Tuesday, March 27, 2012	Sheet: 35of	42



NB5	PROJECT :JW3/4 (Chief River) Quanta Computer Inc.	
Size B	Document Number +1.8V (G9661)	Rev A
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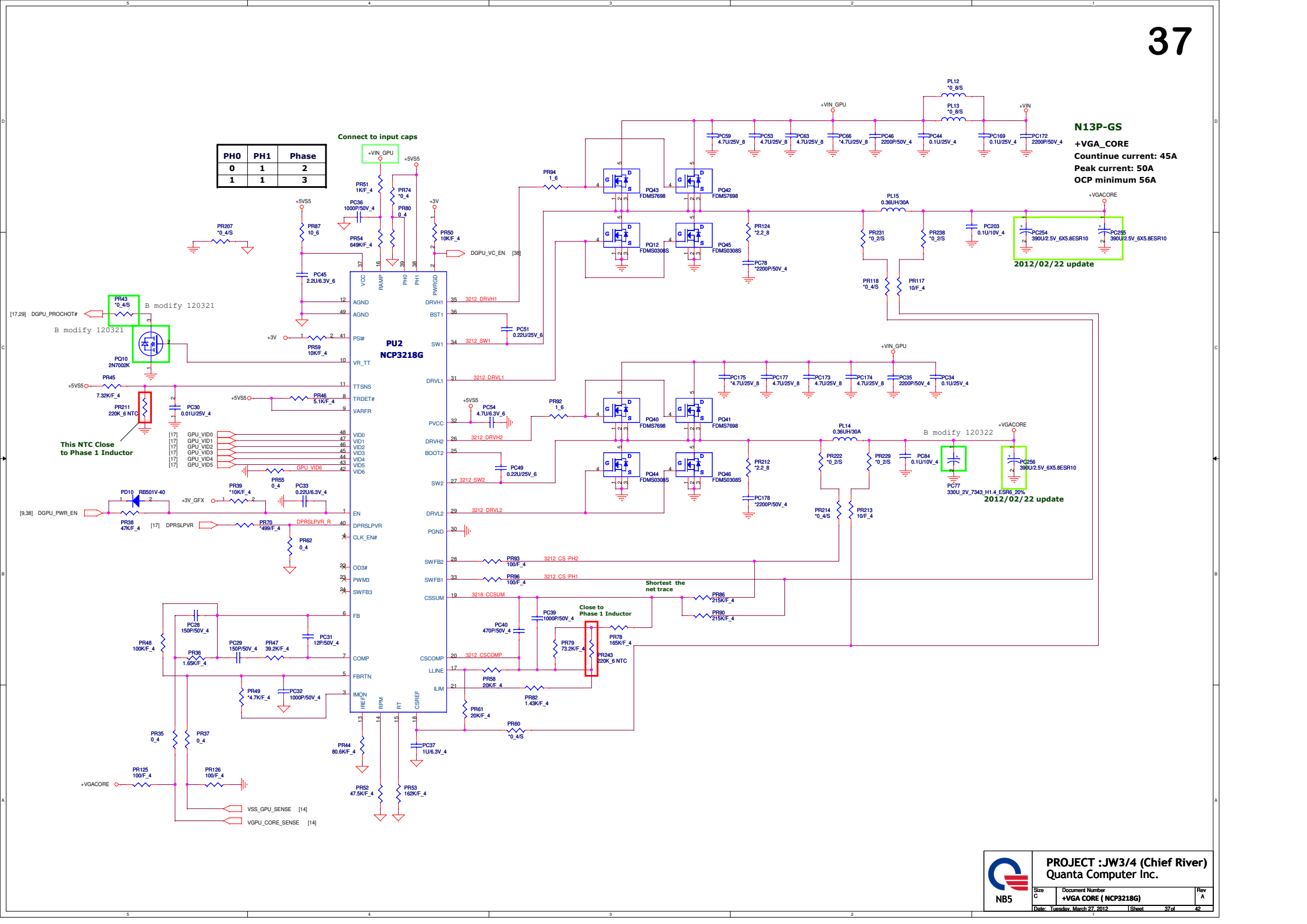
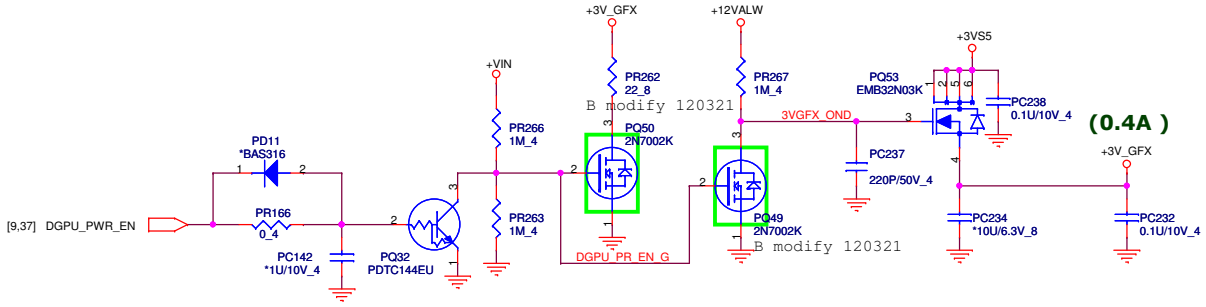
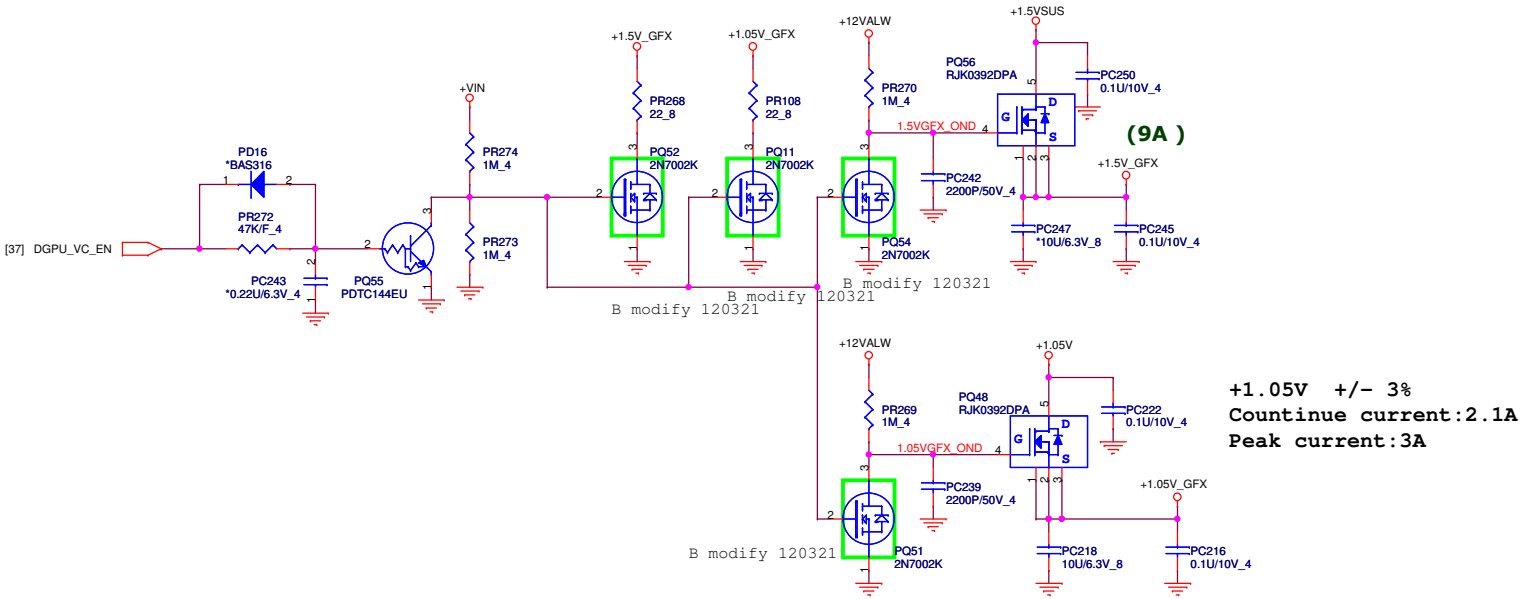

Connect to input caps
PH0 PH1 Phase
0 1 2
1 1 3
PU2
NCP3218G
N13P-GS
+VGA_CORE
Countinue current: 45A
Peak current: 50A
OCP minimum 56A
2012/02/22 update
2012/02/22 update
B modify 120321
B modify 120321
B modify 120322
This NTC Close to Phase 1 Inductor
Close to Phase 1 Inductor
Shortest the net trace
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.
NB5
+VGA_CORE (NCP3218G)

VGA

[2,4,12,13,33] +1.5VSUS
[2,3,6,7,8,9,10,21,26,27,29,32,35,36,41] +3VS5
[14,16,17,18,37] +3V_GFX
[15,18,19,20] +1.5V_GFX
[14,15,16,18] +1.05V_GFX
[41] +12VALW
[2,4,6,7,8,10,26,29,35,39] +1.05V





+1.05V +/- 3%
Countinue current:2.1A
Peak current:3A

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGA POWER	A
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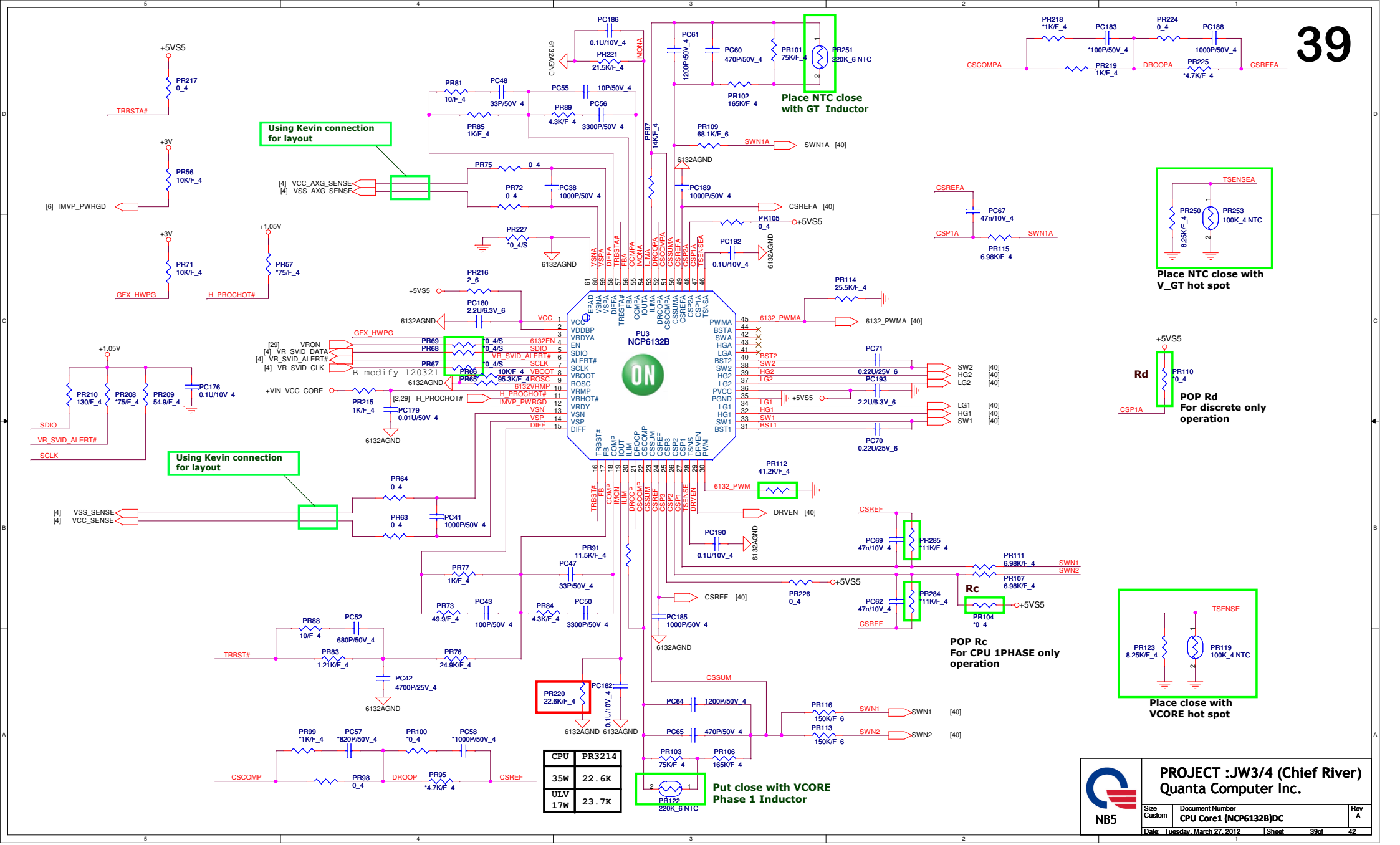
PU3
NCP6132B
ON
Using Kevin connection for layout
Using Kevin connection for layout
Place NTC close with GT Inductor
Place NTC close with V_GT hot spot
Rd
POP Rd
For discrete only operation
Rc
POP Rc
For CPU 1PHASE only operation
Place close with VCORE hot spot
Put close with VCORE Phase 1 Inductor
B modify 120321
CPU | PR3214
35W | 22.6K
ULV 17W | 23.7K
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.
NB5
Size Custom
Document Number CPU Core1 (NCP6132B)DC
Rev A
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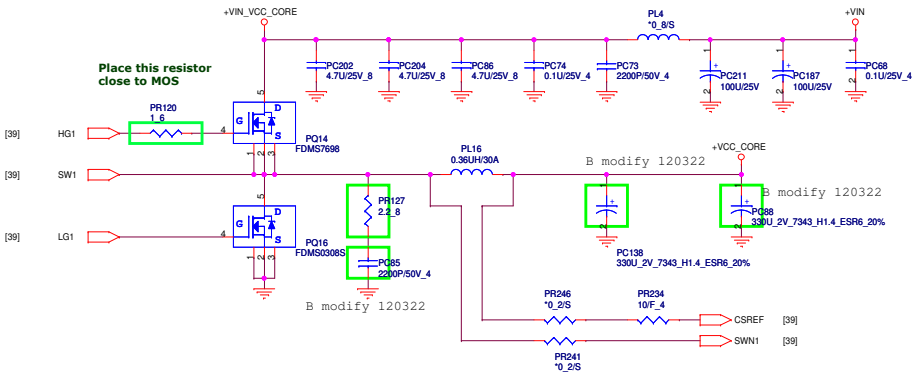
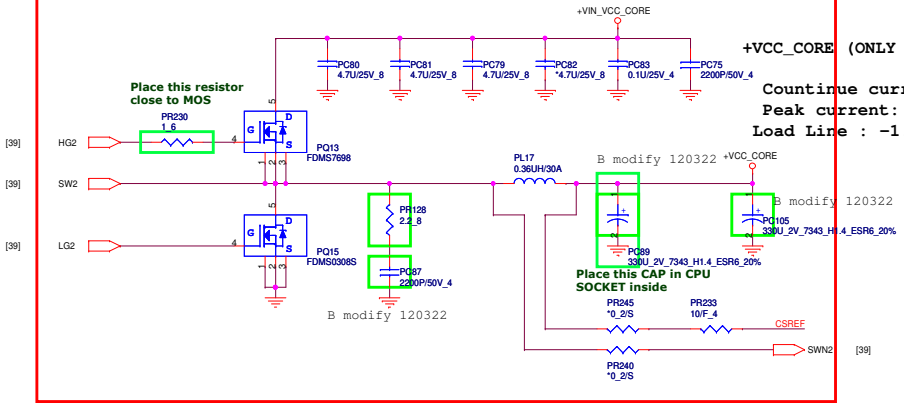


Dummy This Schematic
For CPU 1-Phase operation



+VCC_CORE (ONLY SUPPORT 35W)

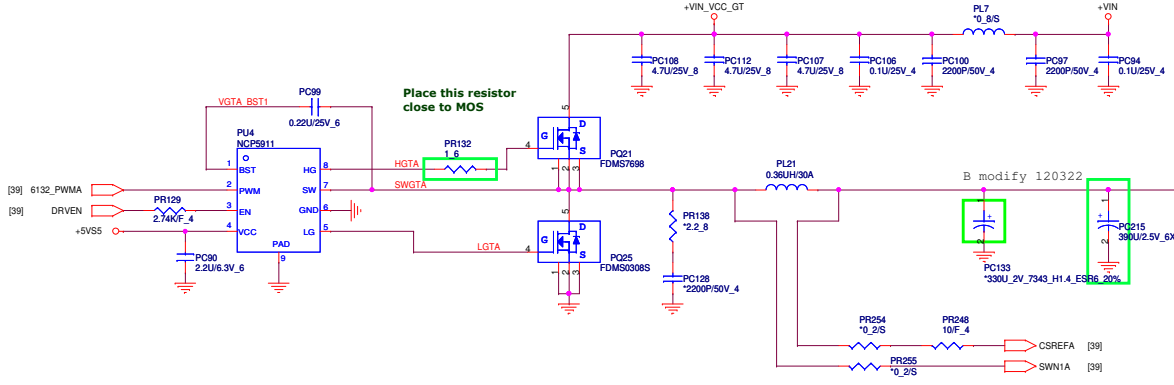
Countinue current:33A
Peak current: 53A
Load Line : -1.9mV/A

+VCC_CORE (ONLY SUPPORT 35W)

Countinue current:33A
Peak current: 53A
Load Line : -1.9mV/A

+VCC_CORE (ULV 17W)

TDC : 25A
Peak current: 33A
Load Line : -2.9mV/A



+VCC_GFX
Countinue current:21.5A
Peak current: 33A
Load Line : -3.9mV/A

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Quanta Computer Inc.

NB5

Size	Document Number	Rev
C	CPU Core2 (NCP5911)DC	A
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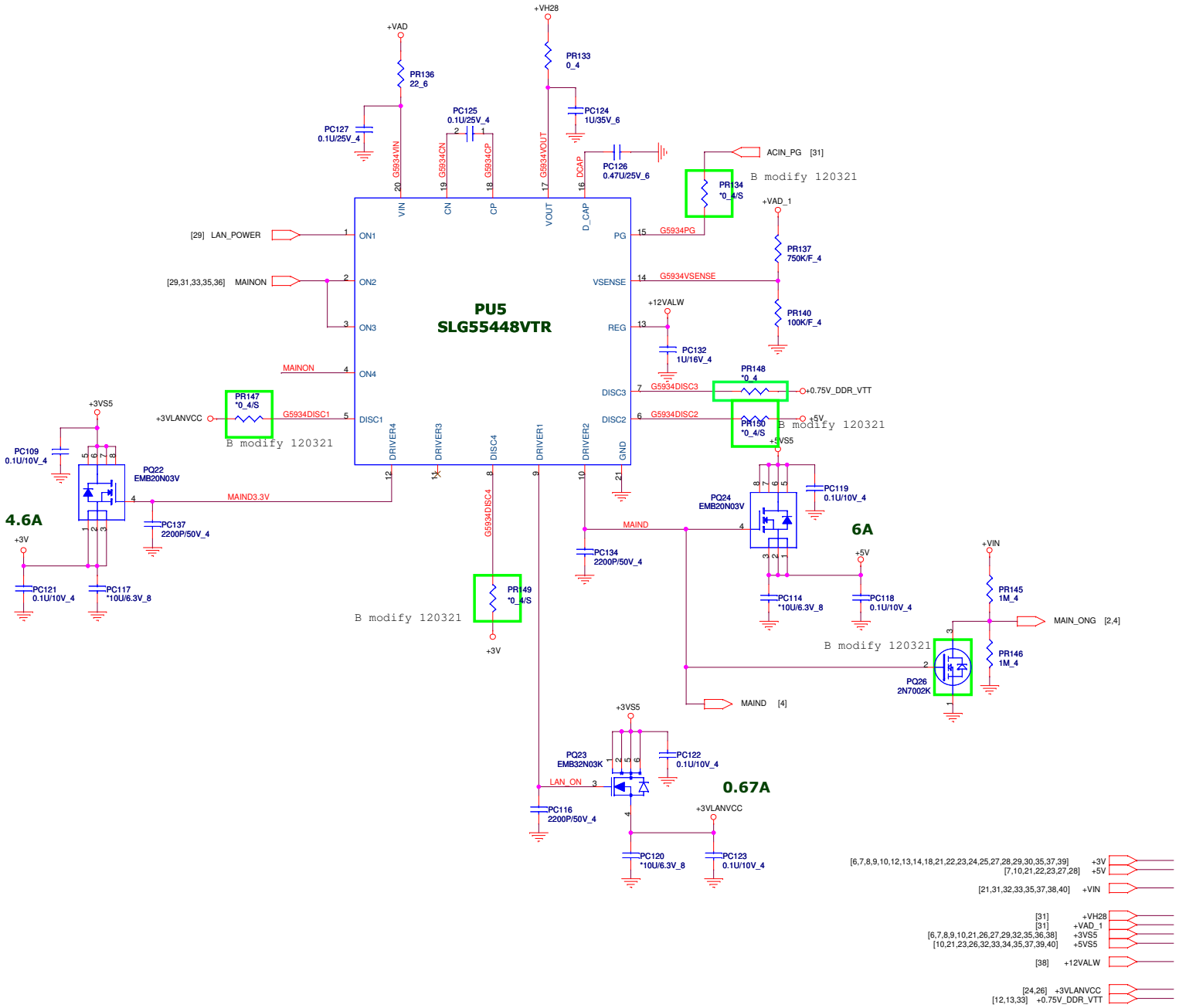

NB5	PROJECT :JW3/4 (Chief River) Quanta Computer Inc.	
Size: Custom	Document Number: Dis-charge IC (SLG55448V)	Rev: A
Date: Tuesday, March 27, 2012	Sheet 41 of 42	

NB5

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
C	History	A

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