# E440

# NM-A151 Rev1.0 Schematic

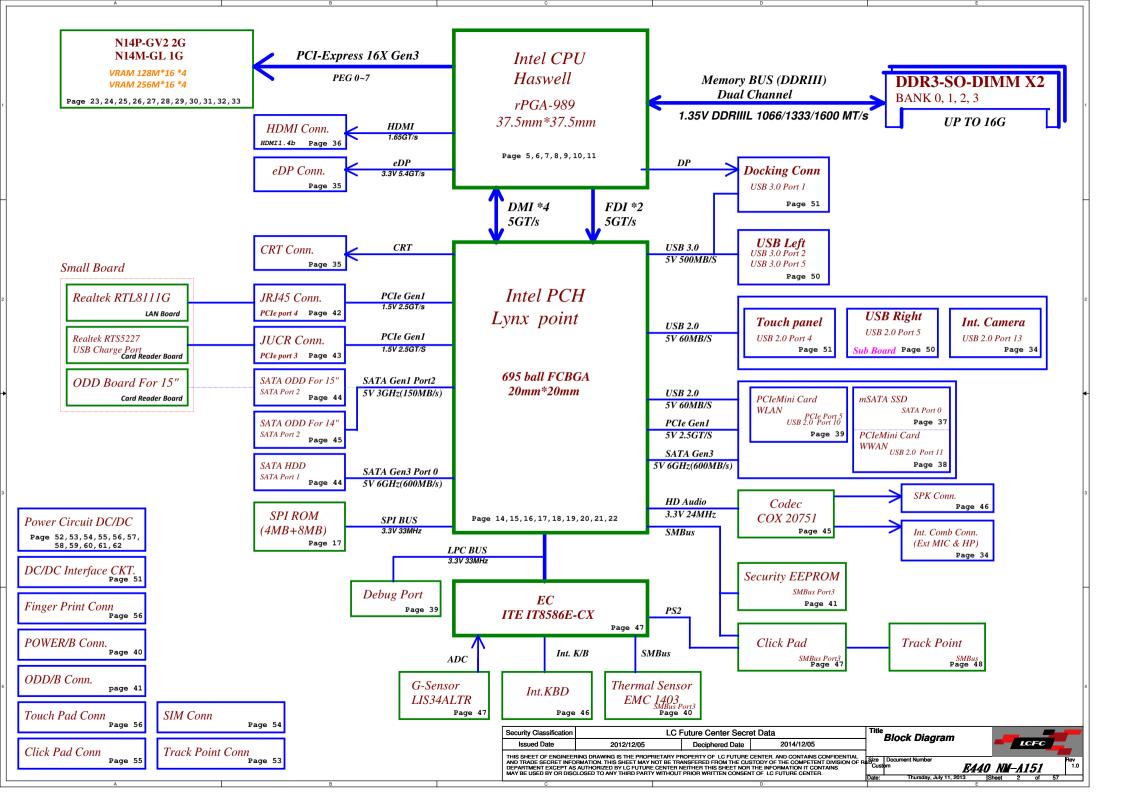
Intel Haswell Processor with DDRIII + Lynx point PCH nVIDIA N14P-GV2/ N14M-GL

2013-07-11 Rev 1.0

Security Classification	LC Future Center Secret Data								
Issued Date	2012/12/05	2014/12/05	1						
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## Voltage Rails (O --> Means ON , X --> Means OFF)

ronago mano (		<u>-</u>	•	
Power Plane State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
so	0	0	0	0
<i>s</i> 3	0	0	0	x
S5 S4/AC Only	0	0	X	х
S5 S4 Battery only	0	x	x	X
S5 S4 AC & Battery don't exist	х	х	х	х

STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

**USB Port Table** 

USB 2.0	USB 3.0	Port	4 External USB Port
	1	0	Camera
	XHCI 2	1	USB Port (Right Side)
EHCI1	3	2	USB Port (Left Side)
	4	3	
	$\overline{}$	4	
		5	USB Port (Right Side)
		6	
		7	
EHCI2		8	
EHCIZ		9	
		10	Mini Card(WLAN)
		11	
		12	
		13	Blue Tooth

**BOM Structure Table** 

BOM Structure	BTO Item
HDMI@	HDMI part
CHG@	USB charger part
NOCHG@	No USB charger part
CMOS@	omosocamerauppert part
8171@	QCA8171 LAN part
8171S@	QCA8171 LAN surge part
SURGE@	QCA8171&8172 LAN surge part
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC 6@	
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
SLI@	For SLI function part
DS3@	Deep S3 support part
<b>S3</b> @	For S3 function part
GT@	NV chip part
@	Unpop
EDP@	Support EDP panel function
daul@	Support daul channel panel function

## **SMBUS Control Table**

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	<b>V</b> +3VALW	х	x	х	х	х	х
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	<b>V</b> +3VS	<b>V</b> +3VS	х	х	х	х	<b>V</b> +3VS	<b>V</b> +3V_PCH	х
PM_SMBCLK PM_SMBDATA	PCH +3V_PCH	X	X	X	X	<b>V</b> +3VS	<b>V</b> +3VS	Х	<b>V</b> +3V_PCH	<b>V</b> +3VS

### **PCIE PORT LIST**

Port	Device
1	LAN
2	WLAN
S	
4	Card Reader
5	
6	
7	
8	

# EC SM Bus1 address

**EC SM Bus2 address** 

**PCH SM Bus address** 

Device	
Smart Battery	

0001 011X b

Device Thermal Sensor EMC1403-2 1001\_101xb Master VGA Slave VGA

Address 0x9E 0x9C

Device DDR DIMM0 DDR DIMM2 Address 1001 000Xb 1001 010Xb

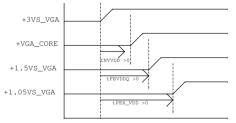
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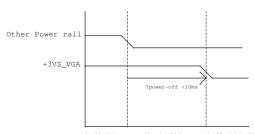
#### Hot plug detect for IFP link E

## VGA and GDDR5 Voltage Rails (N13Px GPIO)

			nago nano (nito x di 10)		
GPIO	I/O	ACTIVE	Function Description		
GPIO0	OUT	-	GPU VID4		
GPIO1	OUT	-	GPU VID3		
GPIO2	OUT	-	VGA_BL_PWM		
GPIO3	OUT	-	VGA ENVDD		
GPIO4	OUT	-	VGA_ENBKL		
GPIO5	OUT	-	GPU VID1		
GPIO6	OUT	-	GPU VID2		
GPIO7	OUT	-	DPRSLPVR_VGA		
GPIO8	I/O	-	Thermal Catastrophic Over Temperature		
GPIO9	OUT	-	GPIO9		
GPIO10	OUT	-	Memory VREF Control		
GPIO11	OUT	-	GPU VID0		
GPIO12	IN		AC Power Detect Input (10K pull High)		
GPIO13	OUT	-	GPU VID5		
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#		
GPIO15	IN	N/A	(100K pull low)		
GPIO16	OUT	-	FRMLCK#		
GPIO17	IN	N/A			
GPIO18	IN	-	dGPU_HDMI_HPD		
GPIO19	IN	-	HPD_IRQ		



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms 2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C\* (GDDR5)

	GPU (4)	Mem (1,5)	NVCLK /MCLK		NVVDE	)	FB\ (1.3	/DD (5V)	FBVE (GPU (1.35	+Mem)	PCI E (1.05 (6)	xpress V)	I/O ar PLLV (1.8V	DD	I/O ar PLLV (1.05)	v) DD (V)	Oth (3.3	- 1
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical		Logical	Logical	Logical	Logical
Strapping pin	Power Rail	Strapping Bit3	Strapping Bit2	Strapping Bit1	Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SORO_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GT (28nm)	0x0FDB

		·
	setting	I2C Slave addrees ID
SMB_ALT_ADDR (ROM_SO Bit 1)	0	0×9E
	1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
		PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	
N13P-GT1 28nm		PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	

Master
Slave

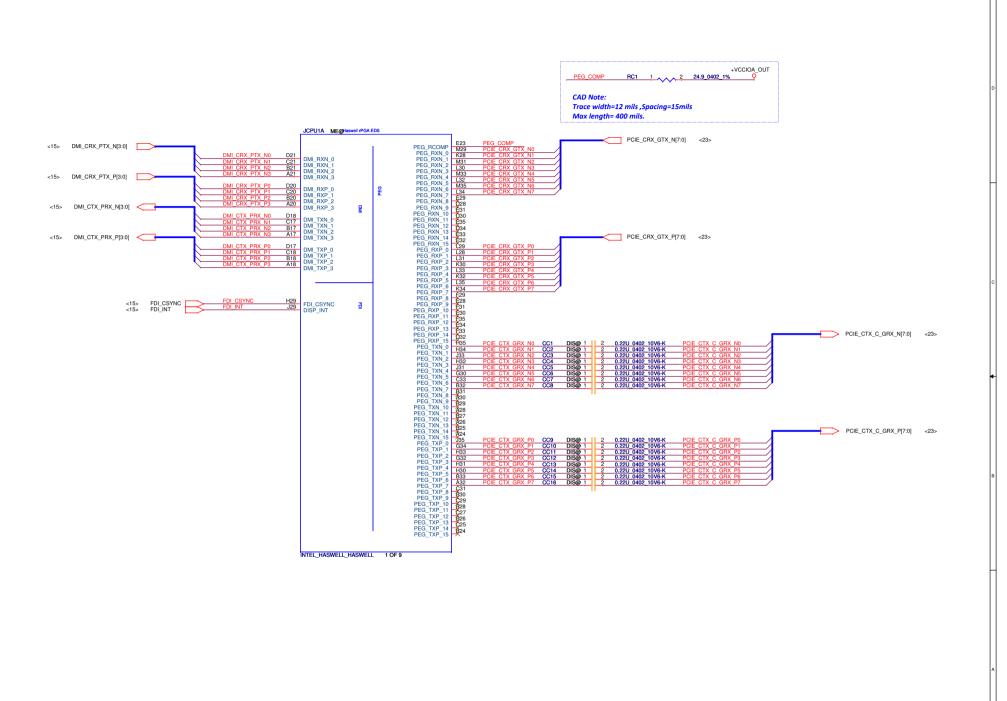
	GPU		
FB Mem	ory (GDDR5)	ROM_SI	
Samsung			
2500MHz	32Mx32	PD 45K	
Hynix	H5GQ1H24BFR-T2C		
2500MHz	32Mx32	PD 35K	
Samsung	K4G20325FD-FC04		
2500MHz	64Mx32	PD 30K	
Hynix	H5GQ2H24MFR-T2C		
2500MHz	64Mx32	PD 25K	

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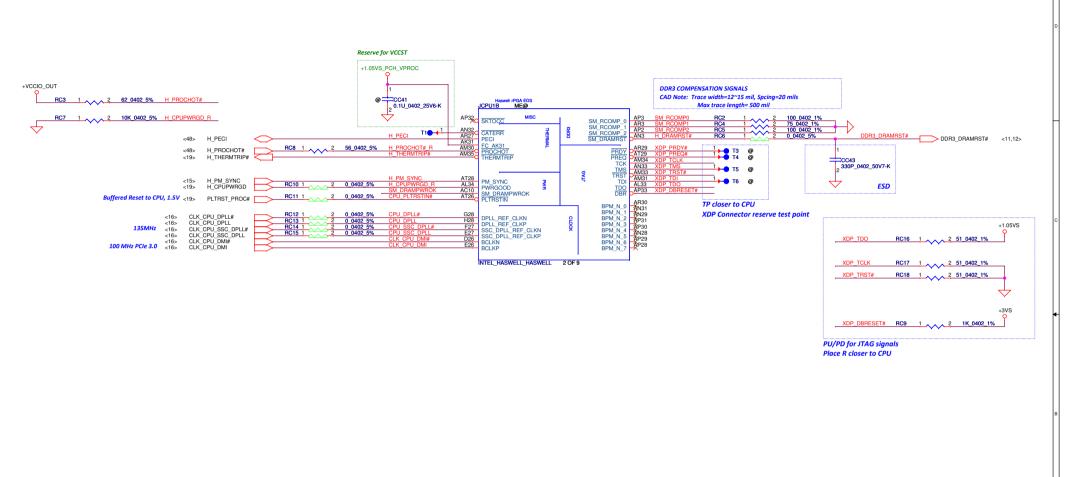
VGA Notes List

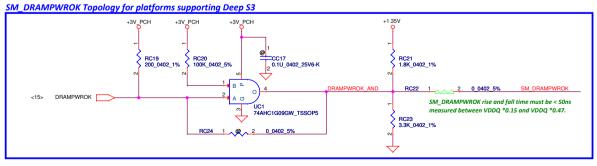


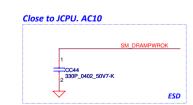
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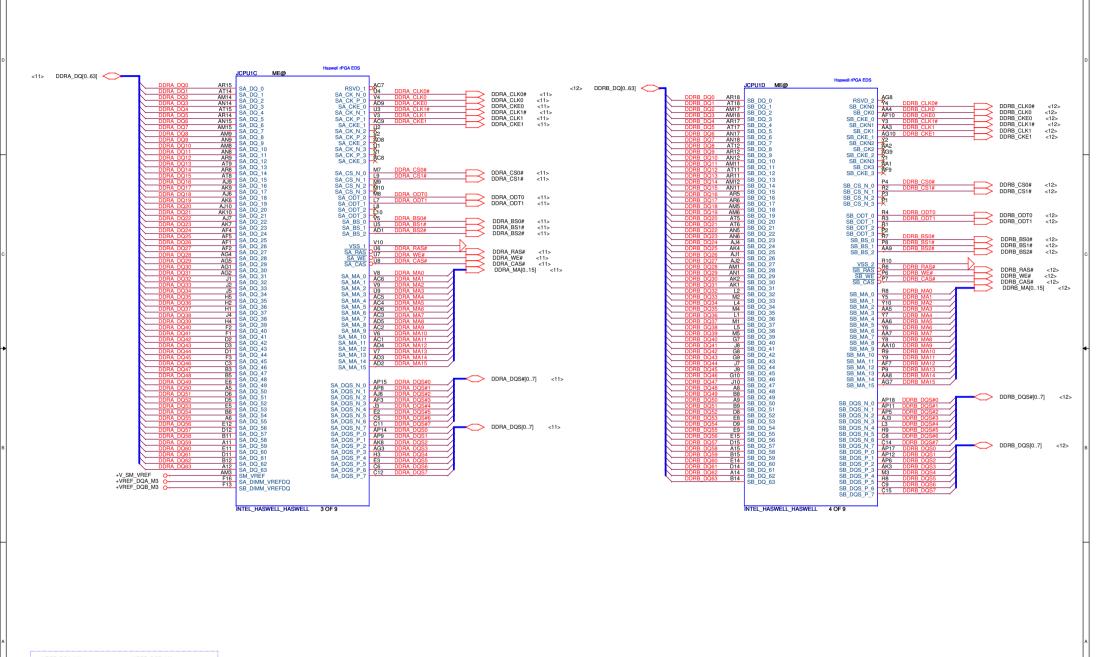
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Issued Date	2012/12/05	Deciphered Date	2014/12/05	CF	PU_DMI/PEG/FDI	LCFC	
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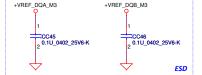






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Issued Date	2012/12/05	Deciphered Date	2014/12/05	CF	PU_JTAG/XDP/CLK	LCFC	
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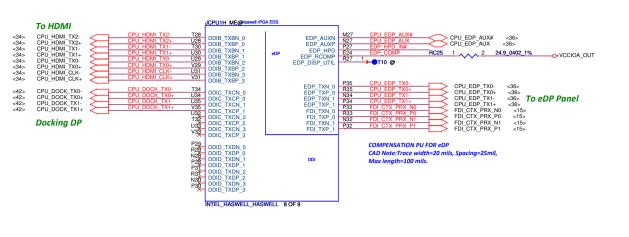


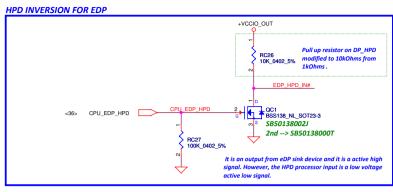
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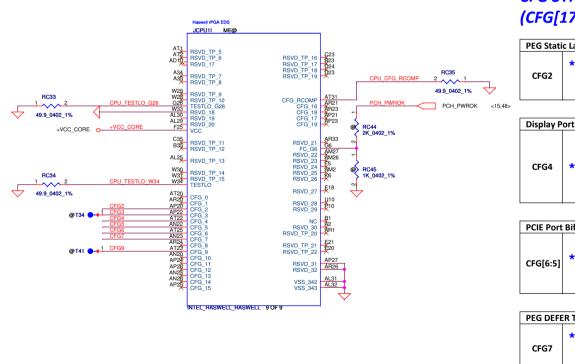
CPU\_DDR3 INTERFACE

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| Date: Thursday, July 11, 2013 | Sheet 7 of 57

1.0







Security Classification

2012/12/05

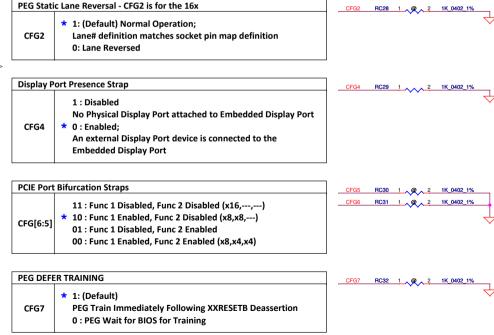
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# CFG STRAPS For CPU (CFG[17:0] internal pull high 5 ~15K to VCCIO)

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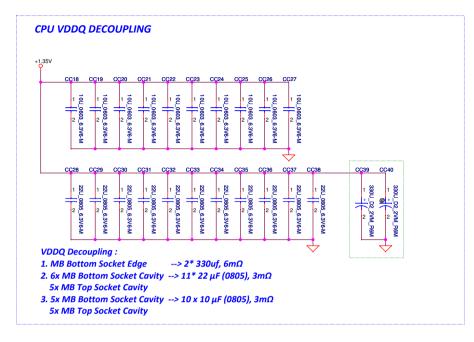
2014/12/05

CPU eDP/DDI/RSVD/CFG LCFC

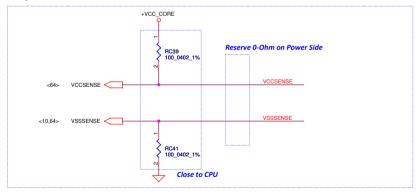
Thursday, July 11, 2013

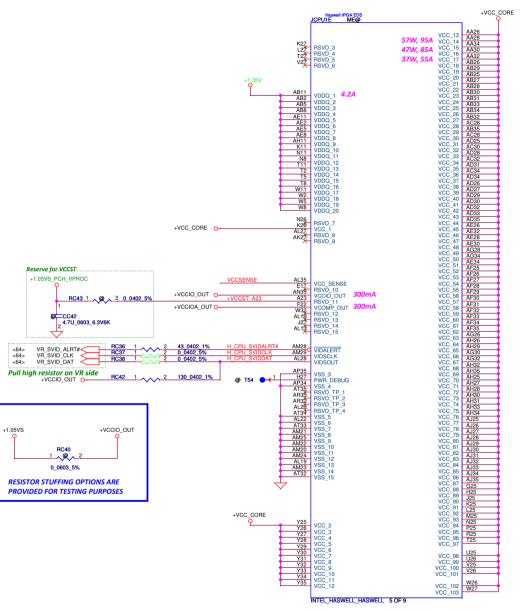
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Size Document Number

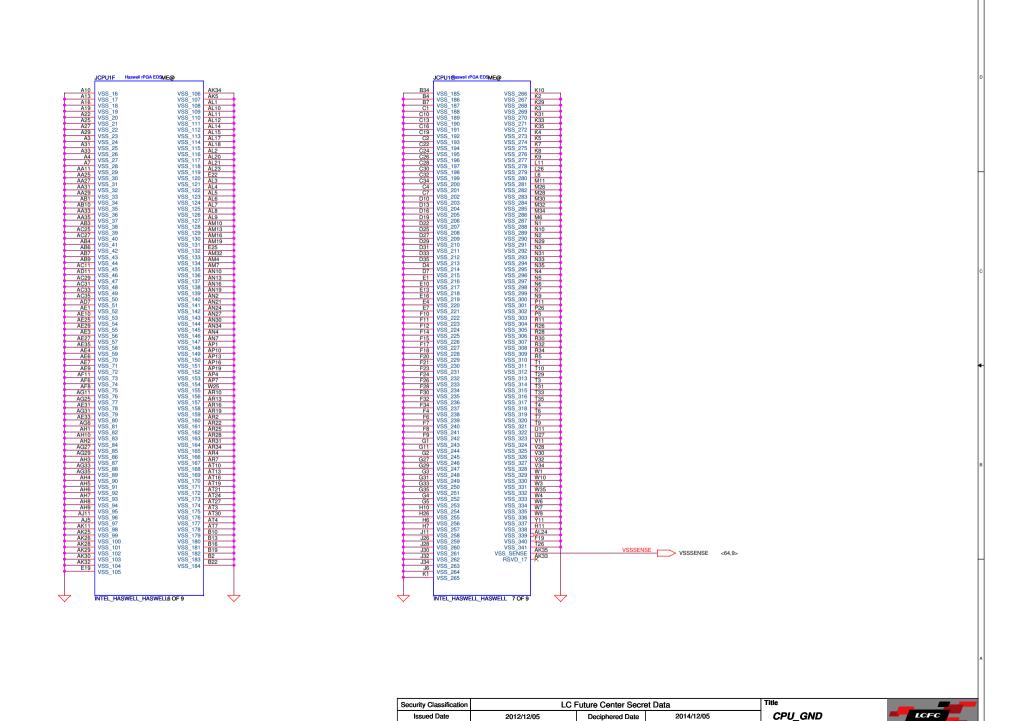


#### **VCC/VSS SENSE**





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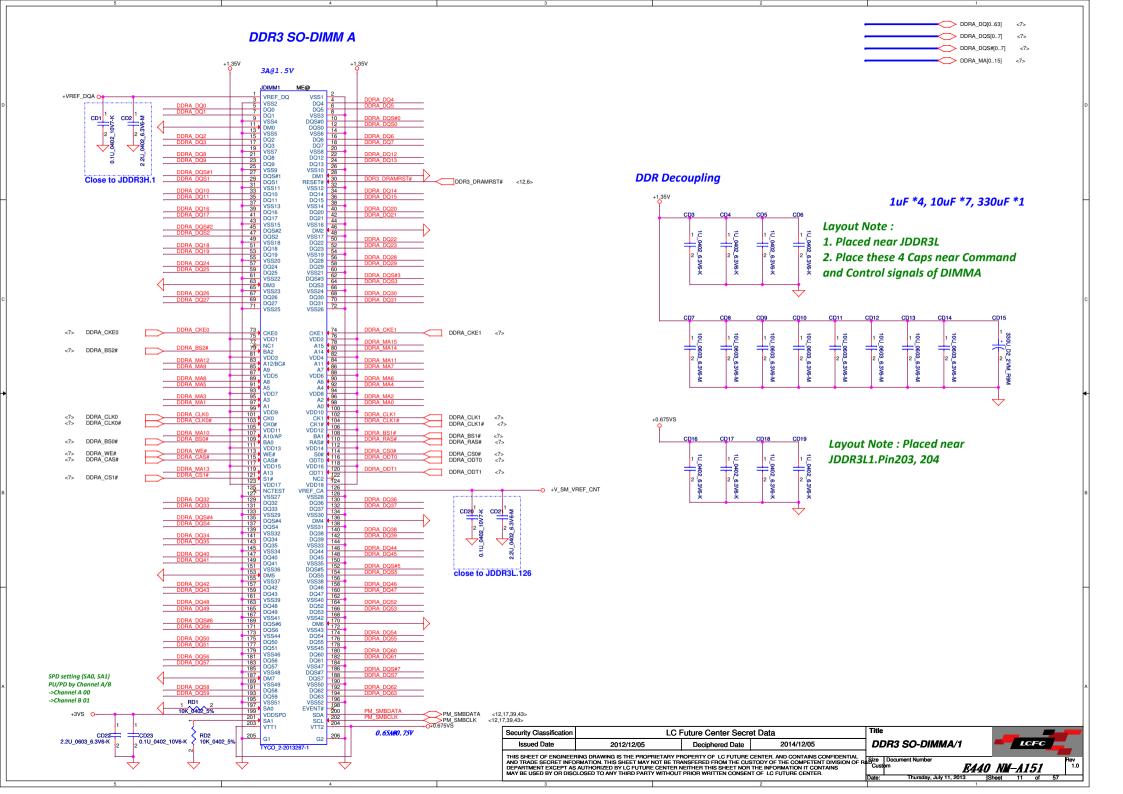
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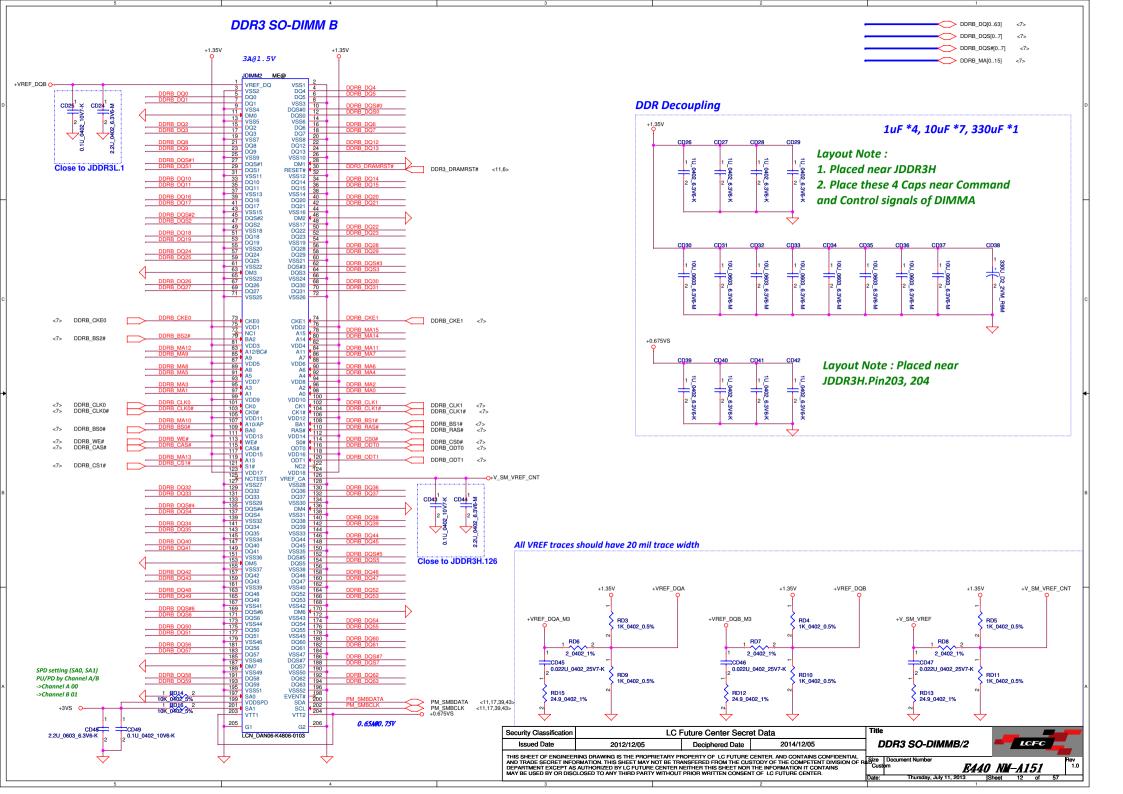
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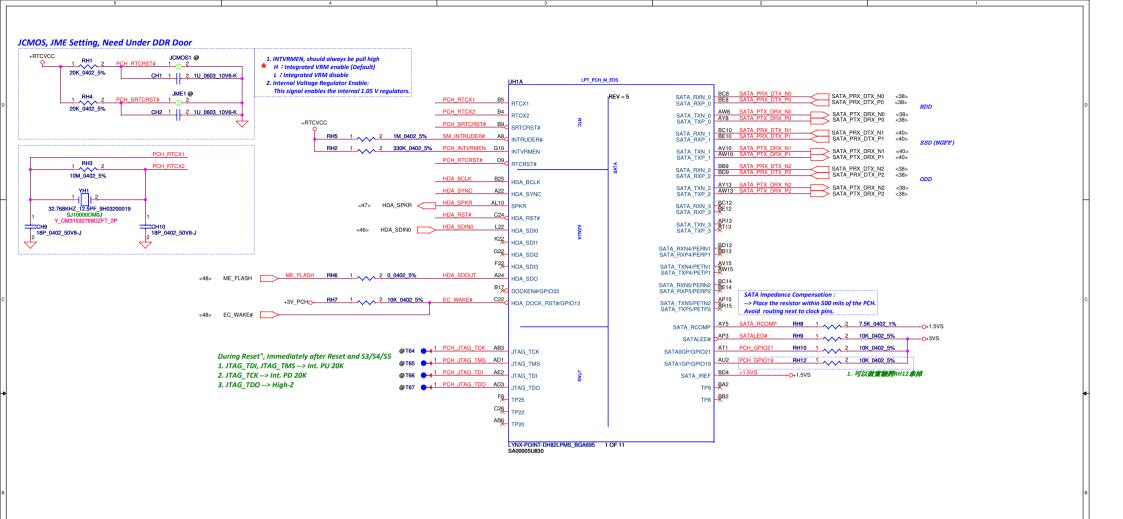
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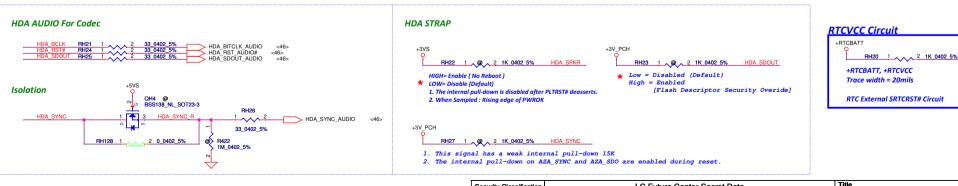
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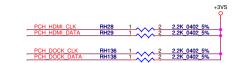
#### **HDA AUDIO SIGNAL**



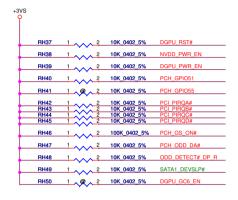
+RTCVCC

CH11

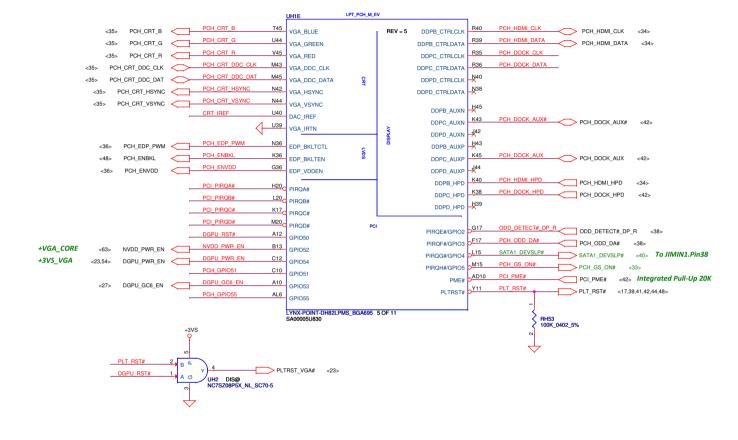
1U\_0603\_10V6-K







1 2 649 0402 1% CRT\_IREF





- 1. The signal has a weak internal pull-up, which is disabled after PLTRST# deasserts.
- 2. When sampled : Rising edge of PWROK

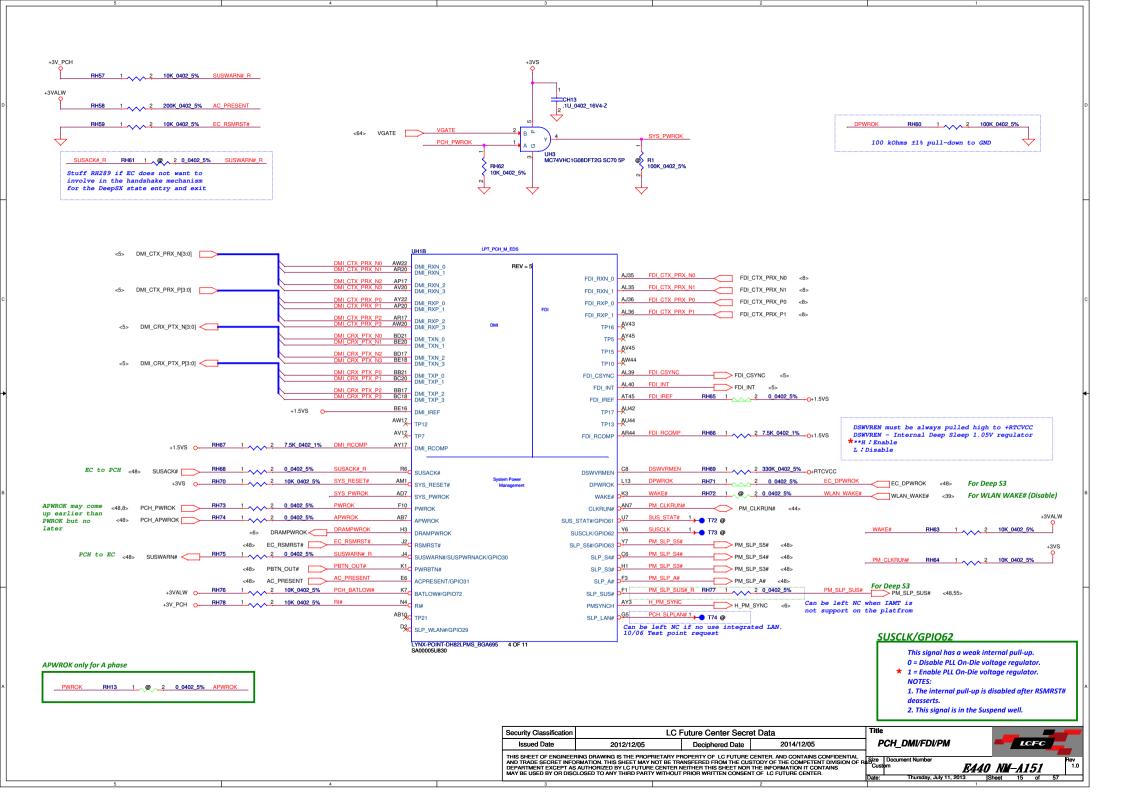
Boot BIOS Straps (BBS)							
BBS_BIT1 (GPIO51)	BBS_BIT0 (GPIO19)	Boot BIOS Location					
0	0	LPC					
0	1	Reserved (NAND)					
1	0	PCI					
1	1	SPI *					

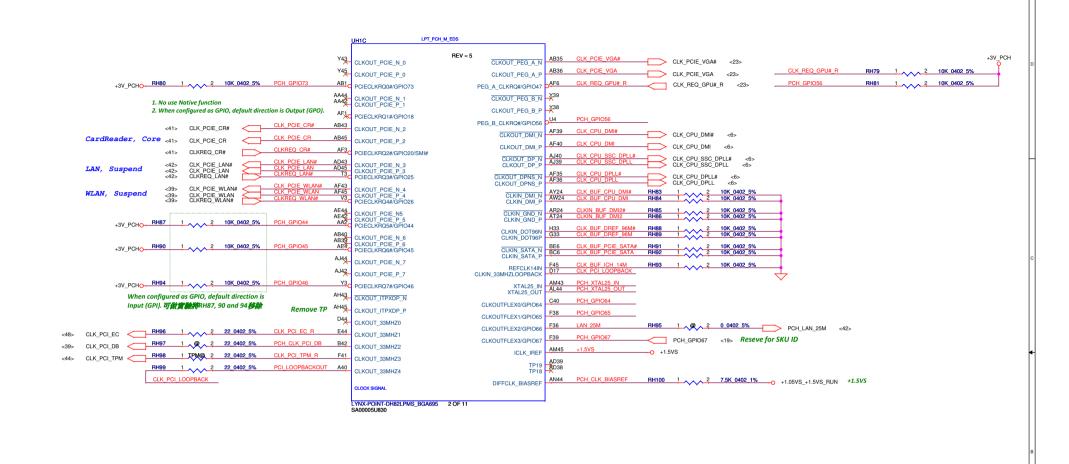
1. GPIO51/19 has weak internal pull-up via 20kohm

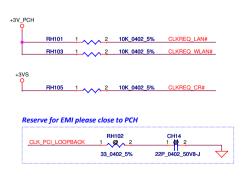
- 2. The internal pull-up is disabled after PLTRST# deasserts.
- 3. GPIO51 (bit 11) at the rising edge of PWROK SATA1GP/GPIO19 (bit 10) at the rising edge of PWROK.

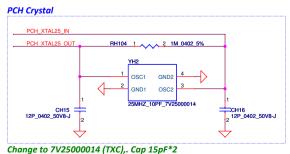
For ESD	
PCH_ODD_DA#	0 CH12 220P_0402_50V8-J

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Project Phase ID					
Project Phase	PCH_GPIO64	PCH_GPIO65			
SDV, FVT	0	0			
SIT2 (R 0.5)	0	1			
SIT (R 0.4)	1	0			
*SVT	1	1			

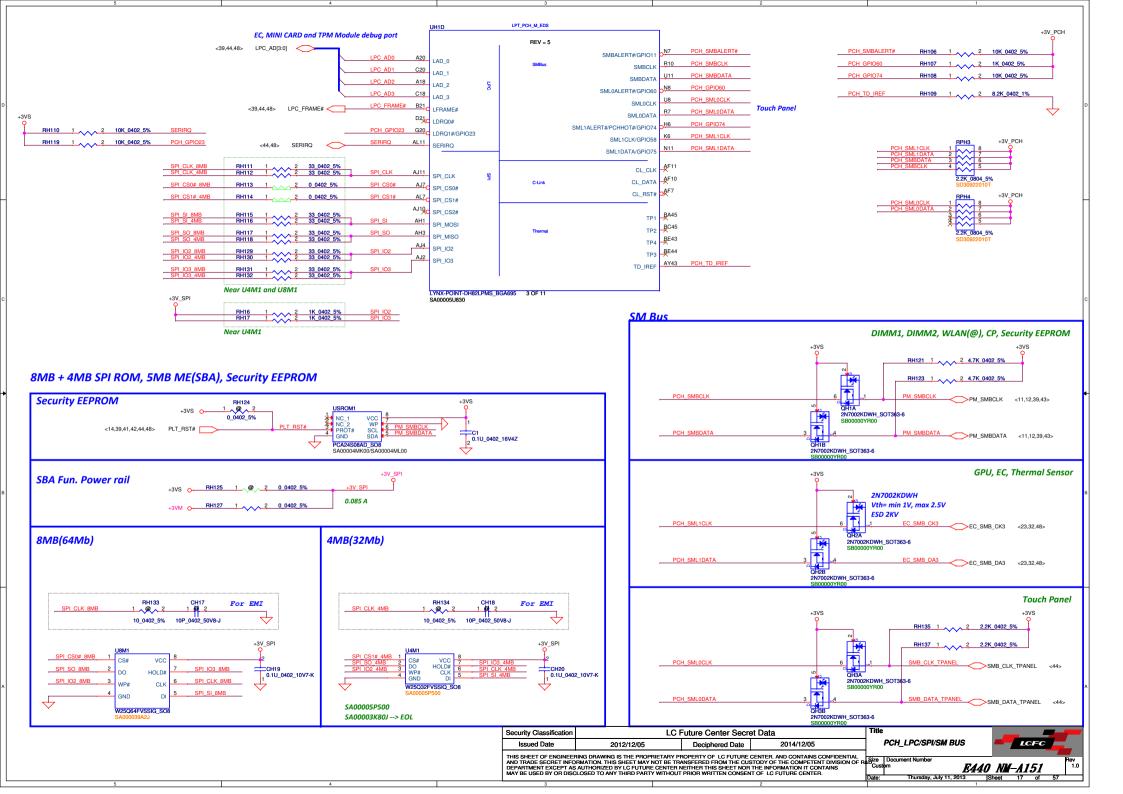
+3VS				
	RH31	1 2	10K 0402 5%	PCH_GPIO64
	RH82	1 ~ ~ 2	10K_0402_5%	PCH_GPIO65
		• •		
_	RH152	1 @ 2	10K_0402_5%	PCH_GPIO64
L	RH162	1 @ 2	10K_0402_5%	PCH_GPIO65
$\Rightarrow$				

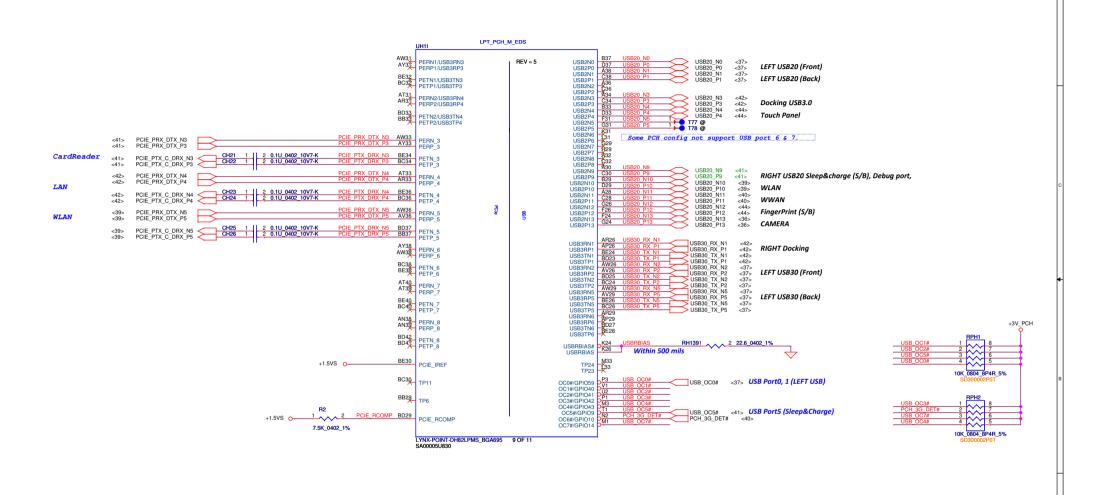
LCFC |

E440 NM-A151

Thursday, July 11, 2013

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Issued Date	2012/12/05	Deciphered Date	2014/12/05	PCH_PCIE/CLK
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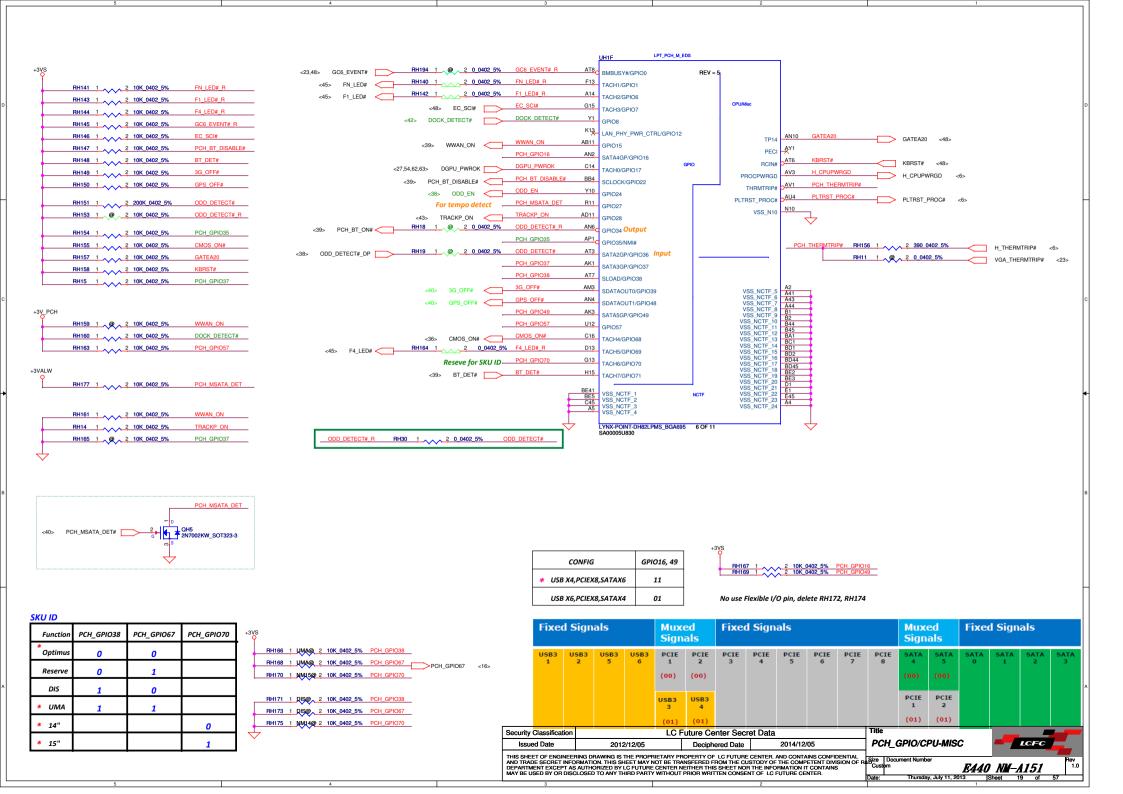


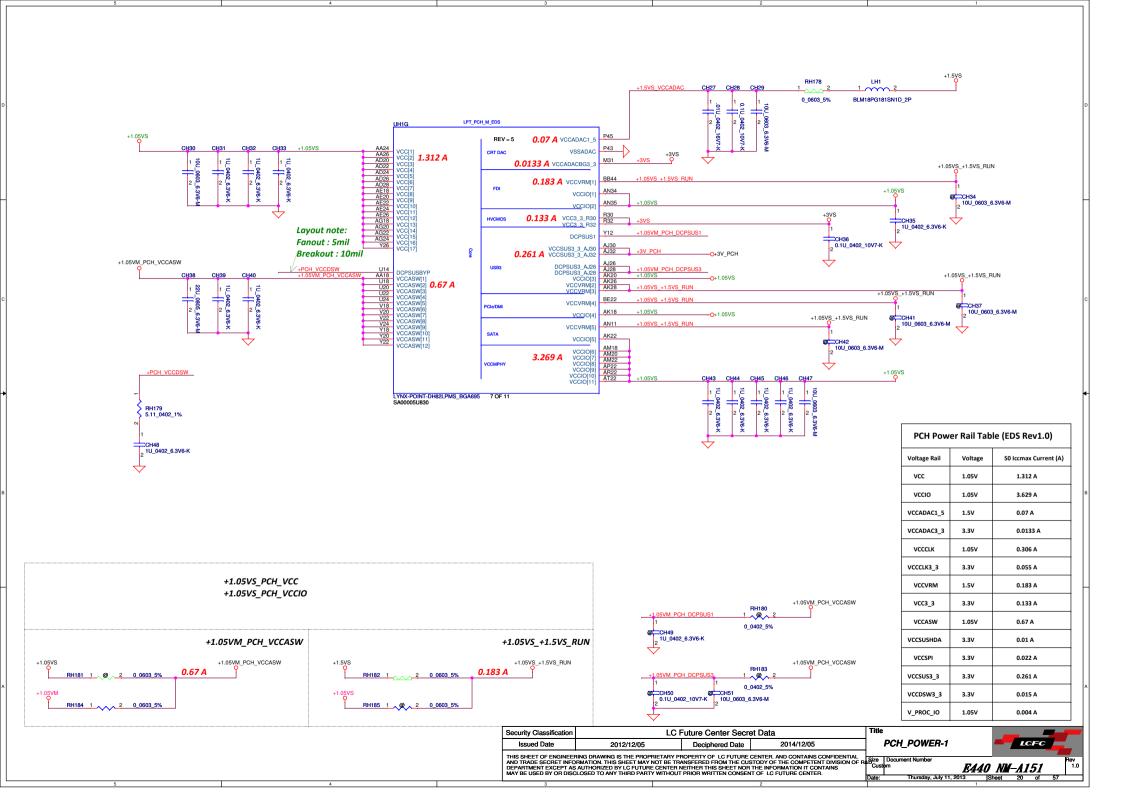


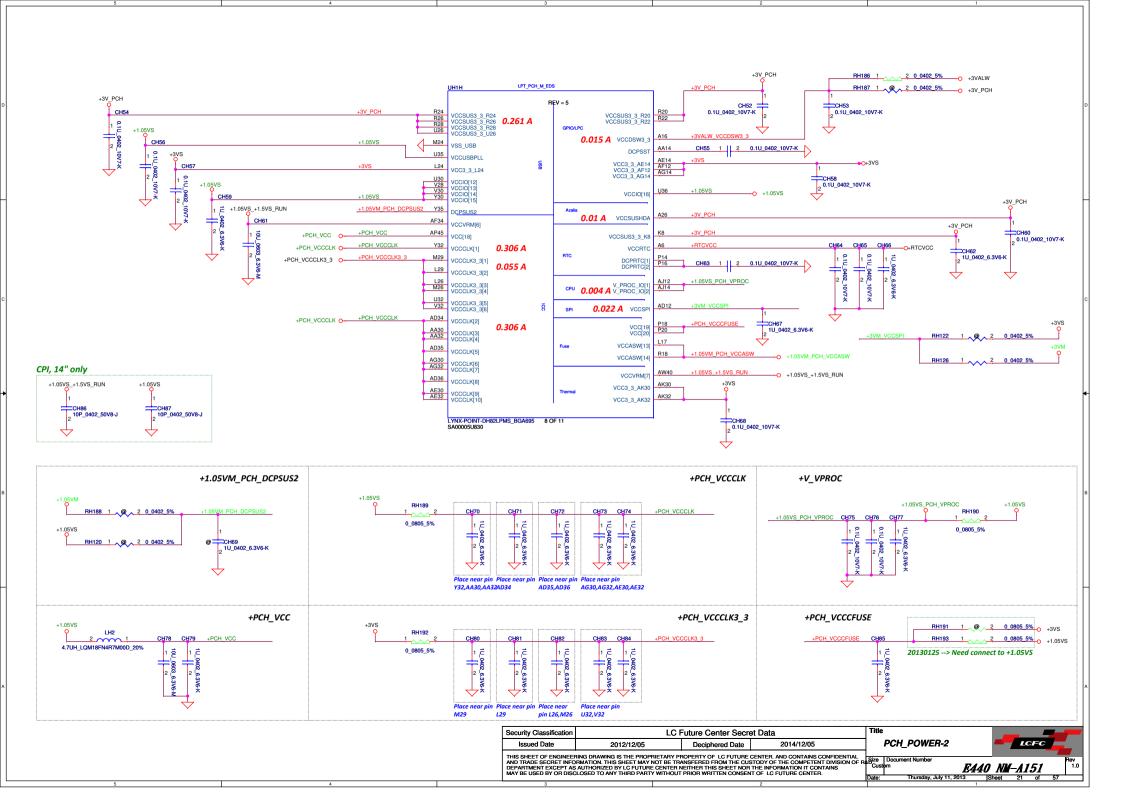


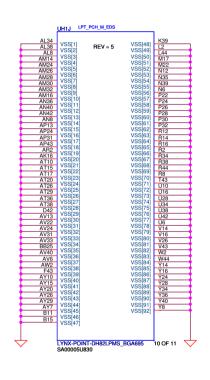
USB3.0	USB2.0	OC#	Note
Port1	Port3	x	Docking (Right)
Port2	Port0	OC0#	LEFT USB (Front)
Port5	Port1	OC0#	LEFT USB (Back)
x	Port9	OC5#	Sleep&Charge (Right)

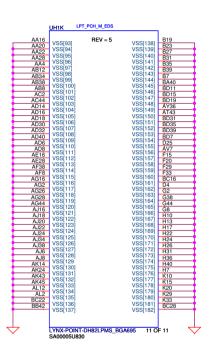
Security Classification	LC F	uture Center Secre	et Data	Title		
Issued Date	2012/12/05	Deciphered Date	2014/12/05	P	CH_PCIE/USB/OC#	LCFC
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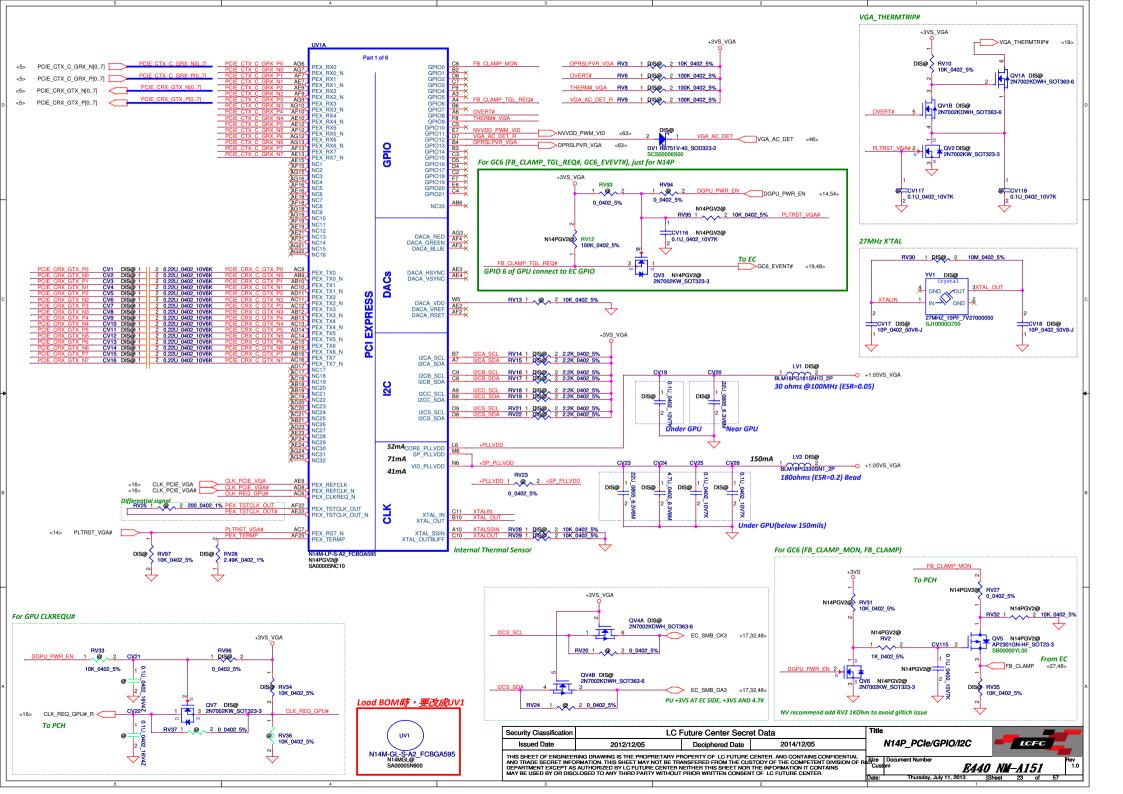


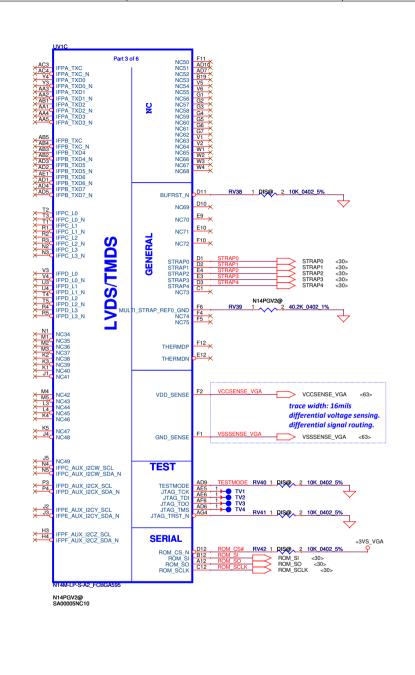
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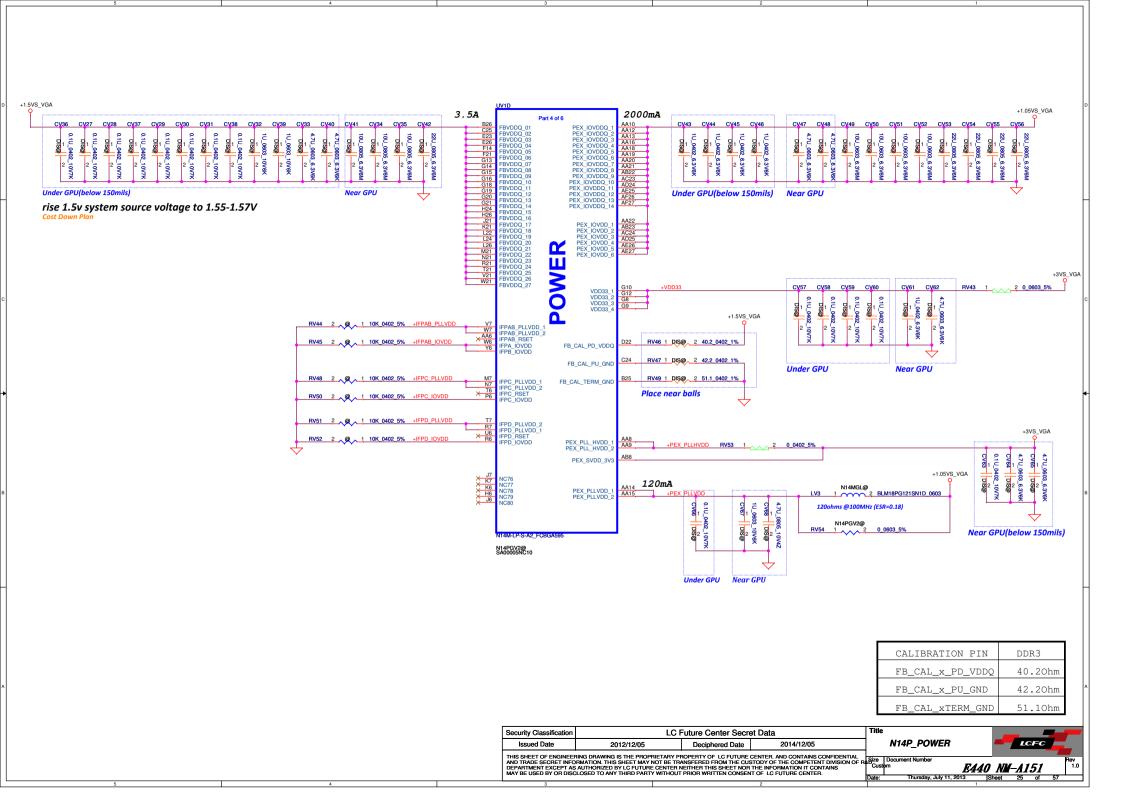
Date: Thursday,

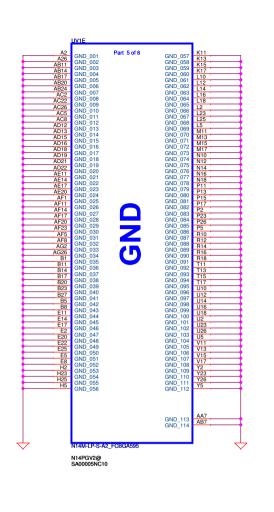


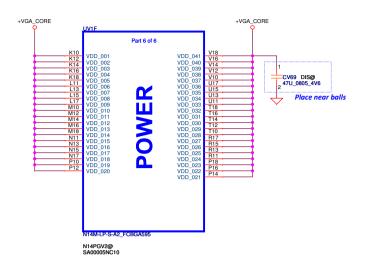


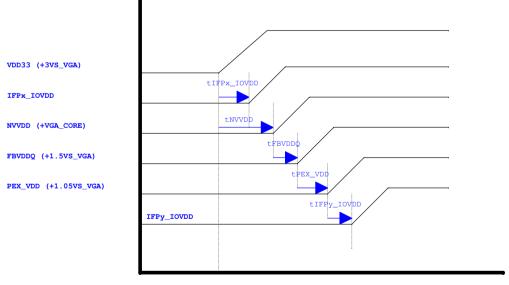


Security Classification	LC	Future Center Secre	et Data	Title		
Issued Date	2012/12/05	Deciphered Date	2014/12/05	N14P_SPI ROM/SENSE	LCFC	
	RING DRAWING IS THE PROPRIETARY P RMATION. THIS SHEET MAY NOT BE TR AUTHORIZED BY LC FUTURE CENTER I LOSED TO ANY THIRD PARTY WITHOUT			L440	7 <b>NM-A151</b> Rev 1.0 Sheet 24 of 57	





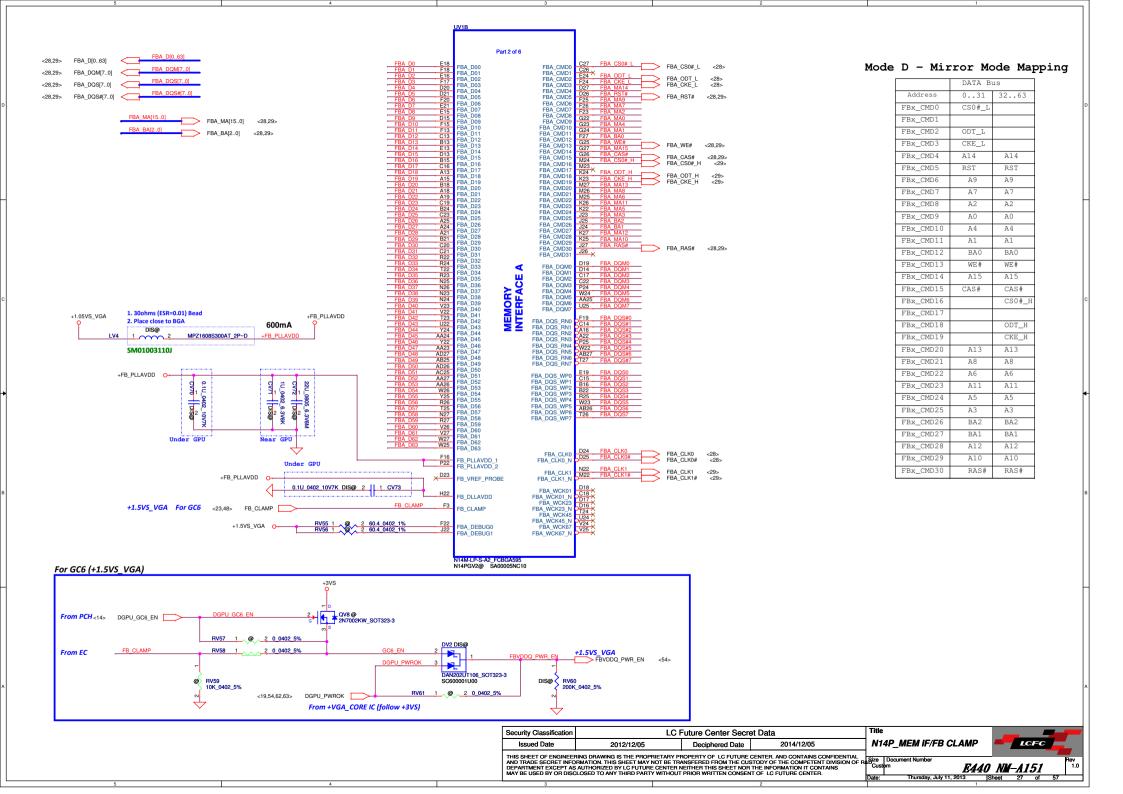




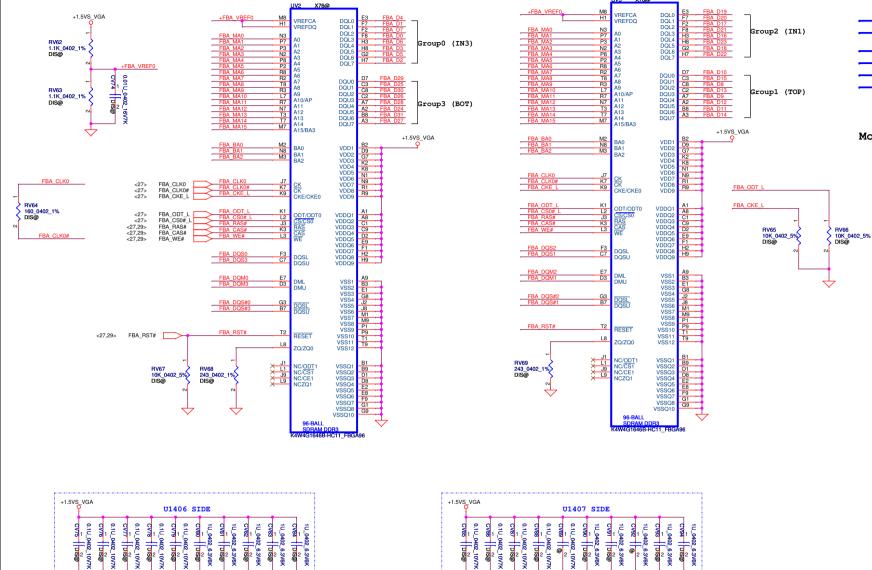
### **NV Recommended Power On Sequencing Order**

X=A and B Y=C,D,E and F

Security Classification	LC F	uture Center Secre	et Data	Title			_	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	N14P_VD	D/GND		LCFC	
AND TRADE SECRET INFO DEPARTMENT EXCEPT AS	RING DRAWING IS THE PROPRIETARY PR RMATION. THIS SHEET MAY NOT BE TRA AUTHORIZED BY LO FUTURE CENTER N LOSED TO ANY THIRD PARTY WITHOUT	INSFERED FROM THE CUS	CENTER. AND CONTAINS CONFIDENTIAL STODY OF THE COMPETENT DIVISION OF R THE INFORMATION IT CONTAINS IT OF LC FUTURE CENTER.		E440	NA -	- <b>A151</b>	Rev 1.0



# Memory Partition A - Lower 32 bits



Mode	D -	Mirror	Mode	Mapping

FBA MA[15..0] <27.29>

<27,29>

<27,29>

<27,29>

<27,29>

<27.29>

FBA\_BA[2..0]

FBA DOMI7.01

FBA DQS[7..0]

FBA DOS#[7..0]

	DATA Bi	
Address	031	3263
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification LC Future Center Secret Data Issued Date 2012/12/05 2014/12/05 Deciphered Date

N14P\_DDR3-A LOWER Rasize Document Number Custom

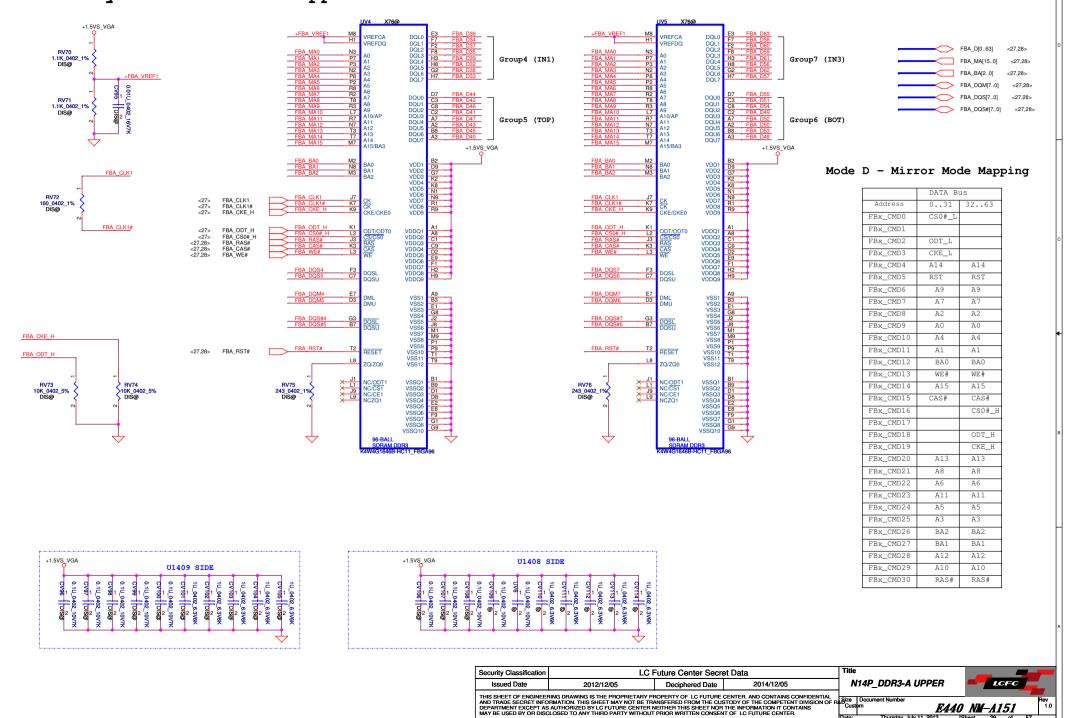
Date: Thursday,

Thursday, July 11, 2013



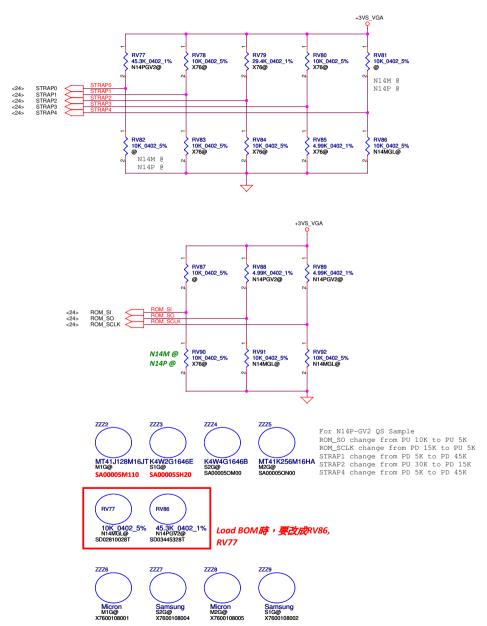
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# Memory Partition A - Upper 32 bits



Size Document Number Custom

E440 NM-A151



Physical Strapping pin	ing pin Power Rail Strapping Bit3		Logical Strapping Bit2	Logical Strapping Bitl	Logical Strapping Bit0 PEX_PLL_EN_TERM		
ROM_SCLK			SUB_VENDOR	PCI_DEVID[5]			
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]		
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE		
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]		
STRAP1	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]		
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]		
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SORO_EXPOSED		
STRAP4	P4 +3VS_VGA RESERVED		PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V		

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR						
0	No VBIOS ROM					
1	BIOS ROM is present (Default)					

3GIO_PADCFG[3:0]				
0110	Gen1/Gen2 support only			
0000	Gen3 support			

FB[1:0]						
0	Reserved					
1	Reserved					
2	256MB (Default)					
3	Reserved					

USER Straps					
User[3:0]					
1000-1100	Customer defined				

Security Classification

SMBUS_ALT_ADDR							
0 0x9E (Default)							
1	0x9C (Multi-GPU usage)						
1	0x9C (Multi-GPU usage)						

PCIE\_MAX\_SPEED

E_MAX_SPEED	PEX	_PLL_EN_TERM
Limit booting to PCIE Gen1	0	Disable (Default)
Allow booting to PCIE Gen 2/3	1	Enable

VGA\_DEVICE

PCI	E_SPEED_CHANGE_GEN3
0	Disable PCIE Gen3 operation
1	Enable PCIE Gen3 operation

DP_	PLL_VDD33V
0	Reserved
1	Default

3D Device (Class Code 302h)

VGA Device (Default)

Issued Date	2012/12/05	Deciphered Date	2014/12/05
AND TRADE SECRET INFO DEPARTMENT EXCEPT AS		ANSFERED FROM THE CU: NEITHER THIS SHEET NOR	

LC Future Center Secret Data

N14P\_MISC(1/2) LCFC Rabize Document Number Custom Thursday, E440 NM-A151

X76 RV90

PD 10K

PU, RV78 PU, RV79 PU, RV80 RV77 PD, RV83 PD, RV84 PD, RV85 PD, RV86

GPU	FB Memory GDDR3		FB Memory GDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
	Samsung	K4W2G1646E-BC1A			PD 45K							
	1000MHz	128Mx16			15458							
	Micron	MT41J128M16JT-093G			PD 30K							
N14P-GV2	1000MHz	128Mx16	PU	5K		FD 30K	PU 45.3K	PD 45.3K	PD 15K	PD 5K	PD 45.3K	

K4W4G1646B-HC11

MT41K256M16HA-107

256Mx16

256Mx16

Samsung 900MHz

Micron

900МНz

S2G, X76~04 SA00005OM00

M2G, X76~05 SA00005ON00

PU, RV78 PU, RV79 PU, RV80

RV77 PD, RV83 PD, RV84 PD, RV85 PD, RV86

S1G, X76~02 SA00005SH20

M1G, X76~01 SA00005M110

	GPU	FB IV	lemory GDDR3	ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
o !	N14M-GL	* Samsung 1000MHz	K4W2G1646E-BC1A 128Mx16				PU 10K	PD 10K	PU 10K	PD 10K	
		Hynix 1000MHz	H5TQ2G63DFR-N0C			PD 10K	PU 10K	PU 10K	PD 10K	PD 10K	
		* Micron 1000MHz	MT41J128M16JT-093G	PD 10K		PU 10K	PU 10K	PD 10K	PD 10K		PD 10K
0			128Mx16								
		Samsung 900MHz	K4W4G1646B-HC11		PU 10K		PU 10K	PU 10K	PU 10K		
			256Mx16								
		Hynix 900MHz	H5TQ4G63MFR-11C		PU 10K		PU 10K	PD 10K	PD 10K		
			256Mx16								
		Micron	MT41K256M16HA-107G				PD 10K	PD 10K	PU 10K	PU 10K	
		900MHz	256Mx16			10100	. 2 20K	. 5 100	. 5 20K		

	Security Classification	LCF	et Data	Т	
	Issued Date	2012/12/05	Deciphered Date	2014/12/05	l
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N14P\_MISC(2/2)

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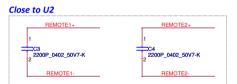
Thursday.

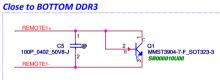
### Thermal Sensor

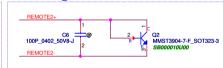
# Thermal Sensor placed near by VRAM



Address 1001\_101xb
Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp







Close to +CPU\_CORE

REMOTE2+/-: Trace width/space:10/10 mil Trace length:<8"

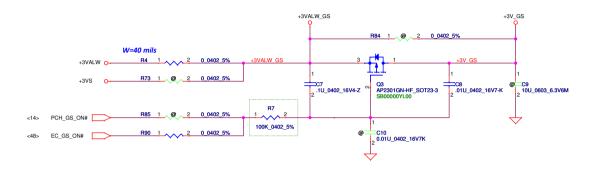
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Issued Date	2012/12/05	Deciphered Date	2014/12/05	T.	
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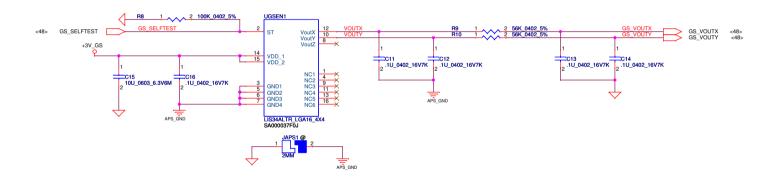
THERMAL SENSOR

IZE | Document Number |
Custom | E440 NM-A151 |
ate: Thursday, July 11, 2013 | Sheet 32 of 57

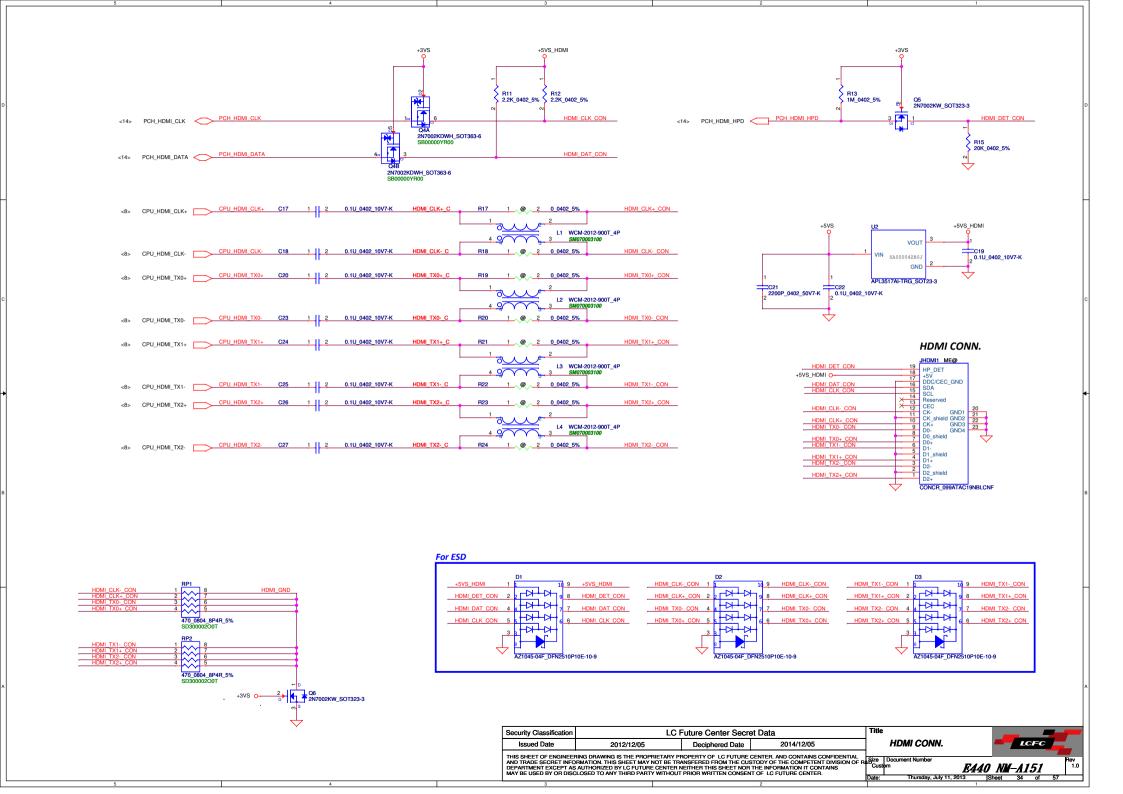
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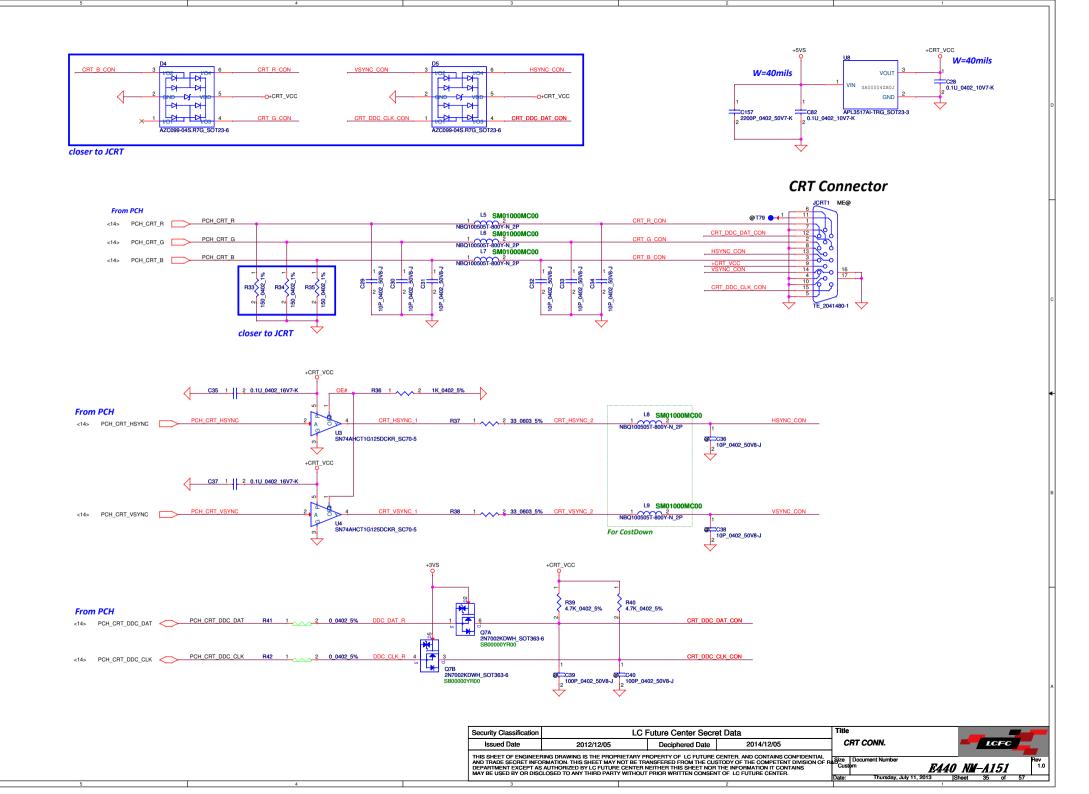
# APS G-Sensor

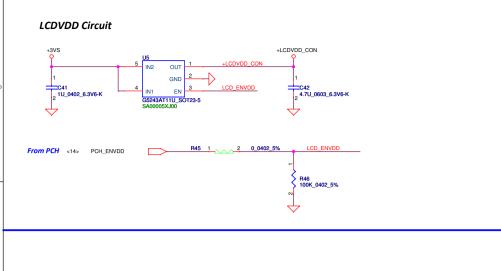




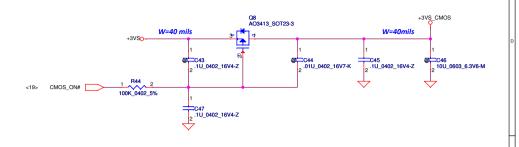
Security Classification	ion LC Future Center Secret Data			Title	Title				
Issued Date	2012/12/05	Deciphered Date	2014/12/05	AP	APS G-SENSOR		LCFC		
AND TRADE SECRET INFO	RMATION. THIS SHEET MAY NO AUTHORIZED BY LC FUTURE (	ETARY PROPERTY OF LC FUTURE OF BE TRANSFERED FROM THE CUS CENTER NEITHER THIS SHEET NOR WITHOUT PRIOR WRITTEN CONSEN		Custom Custom	E440			Rev 1.0	



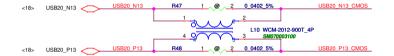


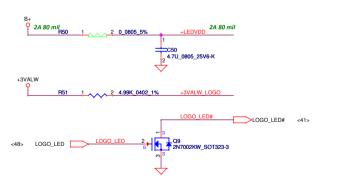


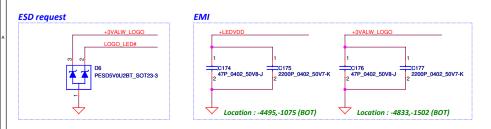
#### **CMOS Camera**

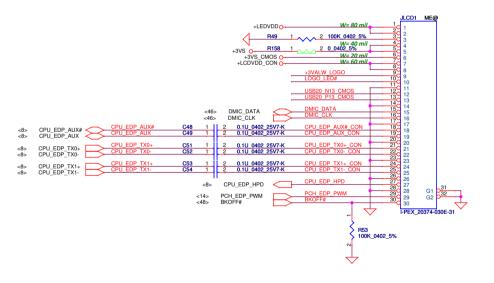


#### **CMOS USB Port10**

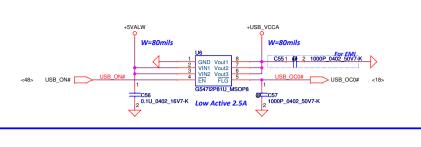




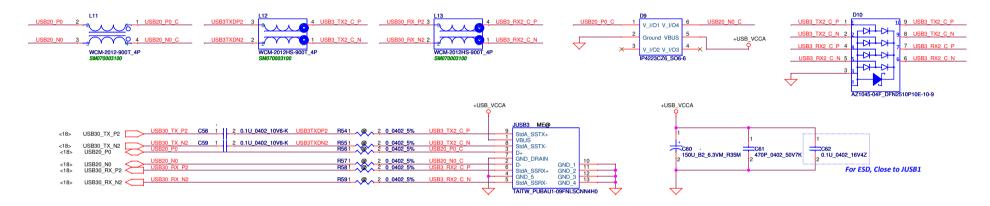




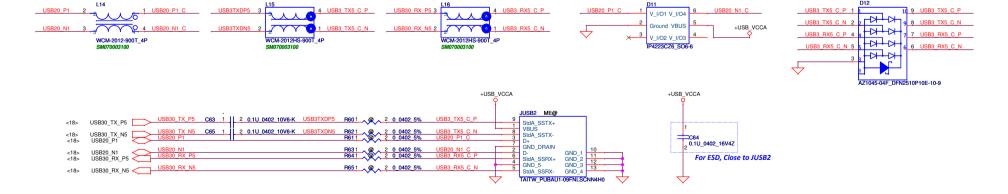
Security Classification LC Future Center Secret Data				Title				
Issued Date 2012/12/05 Deciphered Date 2014/12/05			LCD/CMOS CONN.	LCFC				
AND TRADE SECRET INFO DEPARTMENT EXCEPT AS	RING DRAWING IS THE PROPRIETARY PI RIMATION. THIS SHEET MAY NOT BE TRA AUTHORIZED BY LC FUTURE CENTER IN BLOSED TO ANY THIRD PARTY WITHOUT	ANSFERED FROM THE CUS IEITHER THIS SHEET NOR	IT OF LC FUTURE CENTER.	Size Cust	<u> L440</u>	<b>NM-A151</b>	Rev 1.0	



#### USB30 Front

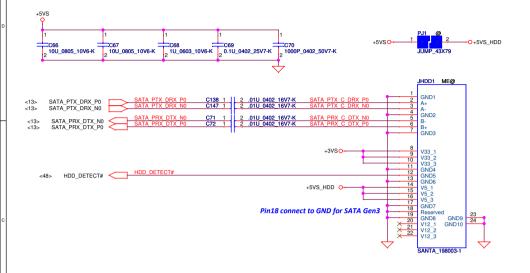


## USB30 Back

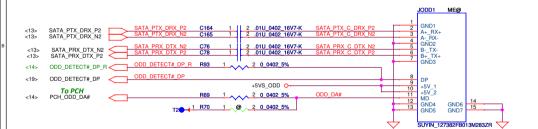


Security Classification	LC Future Center Secret Data			Title			
Issued Date	2012/12/05	Deciphered Date	2014/12/05	Ì	USB30 PORT CONN.	LCFC	
AND TRADE SECRET INFO DEPARTMENT EXCEPT AS	RING DRAWING IS THE PROPRIETARY PRISHMATION. THIS SHEET MAY NOT BE TRAS A MUTHORIZED BY LC FUTURE CENTER N SLOSED TO ANY THIRD PARTY WITHOUT	INSFERED FROM THE CUS	CENTER. AND CONTAINS CONFIDENTIAL STODY OF THE COMPETENT DIVISION OF R THE INFORMATION IT CONTAINS IT OF LC FUTURE CENTER.	Size Cust		NM-A151	Rev 1.0

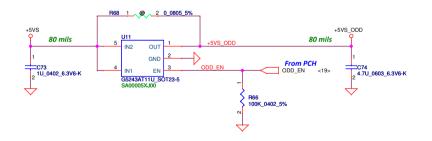




#### SATA ODD CONN & ODD Power Control



## +5VS TO +5VS\_ODD





Security Classification

LC Future Center Secret Data

Issued Date

2012/12/05

Deciphered Date

2014/12/05

Title

SATA HDD/ODD CONN.

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Thursday, July 11, 201

Date: Thursday, July 11, 201

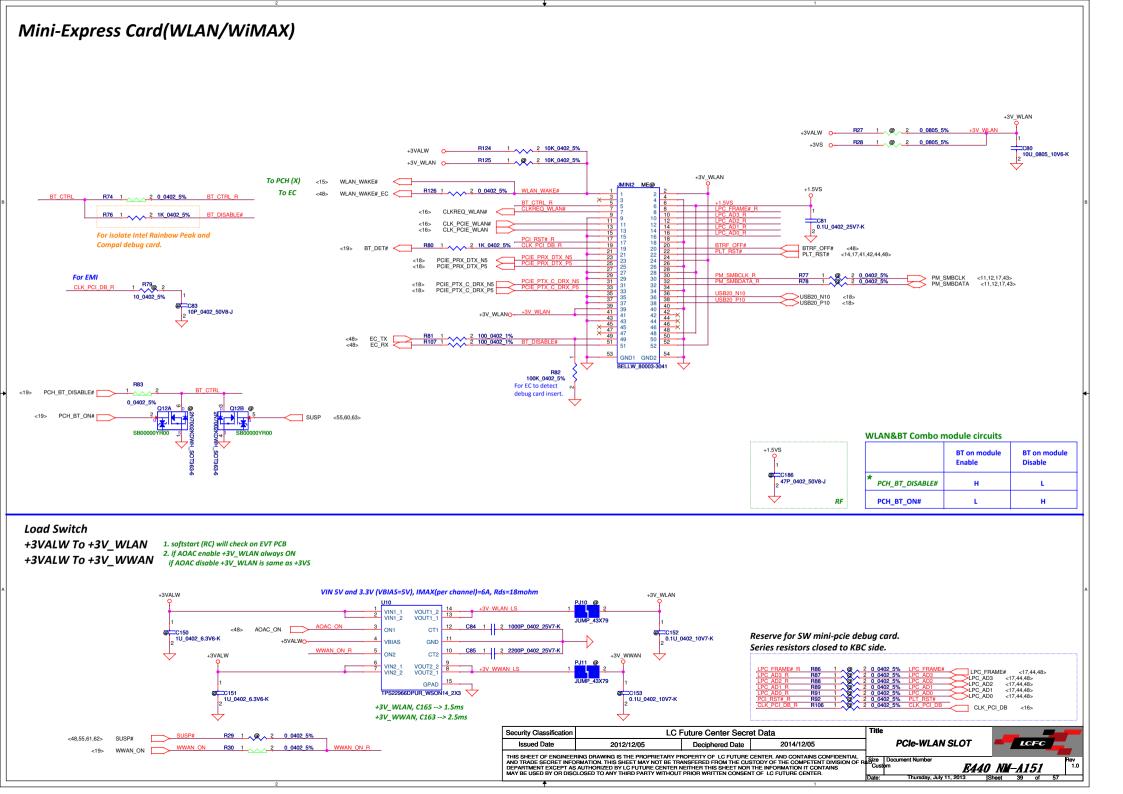
IDD/ODD CONN.

ICFC

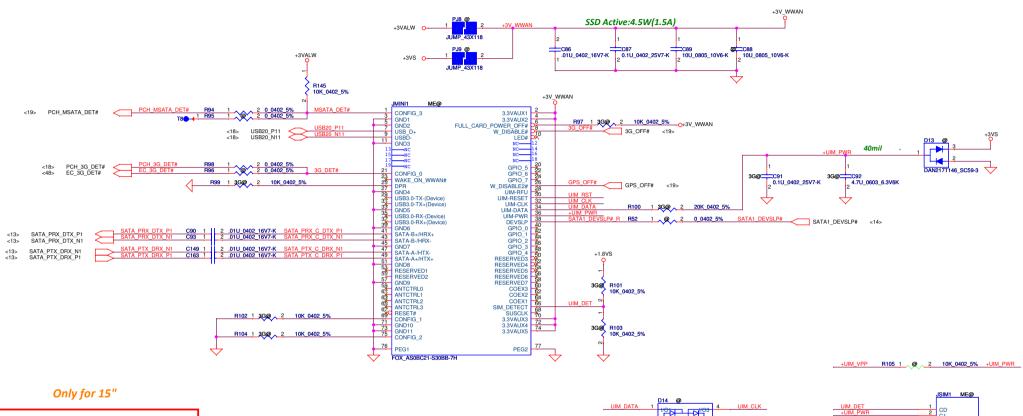
Int Number

E440 NI - A151

Thursday, July 11, 2013 | Sheet 38 of 57



## NGFF(SSD) & SIM CARD CONN.



#/小心EC # 型PCH 3. EC don't have GPIO pin for DET# pin as below

a. PCH\_3G\_DET#
b. PCH\_MSATA\_DET#

UIM_DATA	D14 @	4 UIM_CLK
4	2 SND D V00	5
+UIM_VPP_	3 1/02 1/04	6 UIM RST
	AZC099-04S.R7G_SC	T23-6

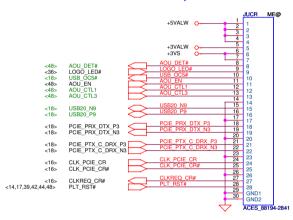
				JSIM1	ME@
UIM DET			1		
+UIM_PWR		_	2	CD	
LINA DOT		_	3	C1 C5	
UIM_RST +UIM_VPP		-	4 5	C2	
UIM_CLK			6	C6	
UIM_DATA			7	C3 C7	
	1		8		
3G@ C94 =	<b>=</b> :		9	GND1 GND2	
0.1U_0402_25V7-K	2	T i		GINDZ	
_	ら く	5		PLAST	CE1S-14

NGFF Dete	NGFF Detect Desc.							
	MSATA_DET#	3G_DET#						
No Card	1	1						
WWAN CARD	1	o						
SSD CARD	0	О						

Security Classification	LC Future Center Secret Data			Title			
Issued Date	2012/12/05	Deciphered Date	2014/12/05	PCIe-WWAN/SIM SLOT			
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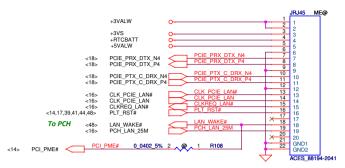
SYSON



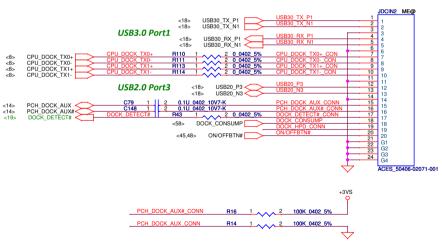
curity Classifica	tion LC	LC Future Center Secret Data							,	7
Issued Date	2012/12/05	Deciphered Date	2014/12/05	i	PCI	e-CR/USB-Chai	rge CONN.		LCFC	
TRADE SECRET PARTMENT EXCE	NEERING DRAWING IS THE PROPRIETARY INFORMATION. THIS SHEET MAY NOT BE T PT AS AUTHORIZED BY LC FUTURE CENTER DISCLOSED TO ANY THIRD PARTY WITHOU	RANSFERED FROM THE CU: NEITHER THIS SHEET NOR	STODY OF THE COMPET THE INFORMATION IT C	ENT DIVISION OF RA ONTAINS ER.	Size I Custor Date:	Document Number m Thursday, July 11	<i>E440</i>	<b>NM</b> -	A151	

LAN (Port4) USB3.0/2.0 (Port1/3) DP(DDIC)

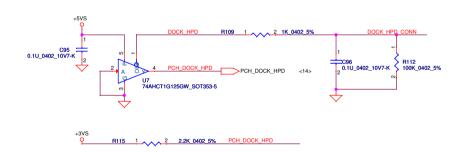
## LAN CONN. (FFC)



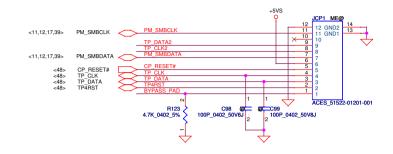
## DCIN CONN. (Coaxial)

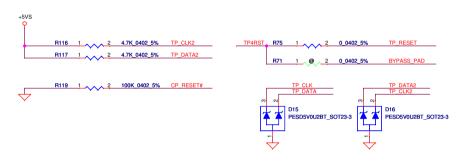


Security Classification	LCF	uture Center Secre	et Data	Title		
Issued Date	2012/12/05	Deciphered Date	2014/12/05	PCIe-RJ45/RTC/Docking CON LCFC		
AND TRADE SECRET INFO DEPARTMENT EXCEPT AS	RING DRAWING IS THE PROPRIETARY PR RMATION. THIS SHEET MAY NOT BE TRA AUTHORIZED BY LC FUTURE CENTER IN LOSED TO ANY THIRD PARTY WITHOUT	ANSFERED FROM THE CUS NEITHER THIS SHEET NOR	IT OF LC FUTURE CENTER.	Size Cust	Document Number P440 NW-A151 Rev 1.0 Thursday, July 11, 2013 Sheet 42 of 57	

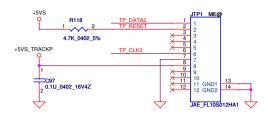


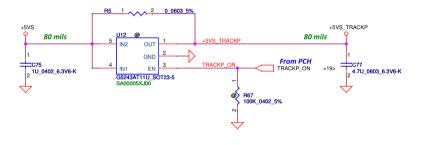
## Click Pad



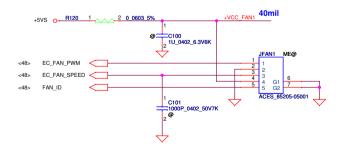


# Track point



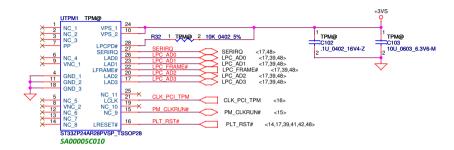


## FAN CONN.

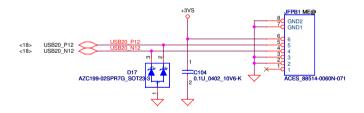


Security Classification	LC Future Center Secret Data			LC Future Center Secret Data			Title		_ ~	7
Issued Date	2012/12/05	Deciphered Date	2014/12/05	CP/TP/FAN CONN.		LCFC				
AND TRADE SECRET INFO DEPARTMENT EXCEPT AS	RING DRAWING IS THE PROPRIETARY PRIBE TARY PRIBE TRAINS SHEET MAY NOT BE TRAIN AUTHORIZED BY LC FUTURE CENTER NOT SHOULD TO ANY THIRD PARTY WITHOUT	ANSFERED FROM THE CUS IEITHER THIS SHEET NOR	CENTER. AND CONTAINS CONFIDENTIAL STODY OF THE COMPETENT DIVISION OF R THE INFORMATION IT CONTAINS IT OF LC FUTURE CENTER.	Size I Custor	Occument Number n <b>E440</b>	NW-A151	Rev 1.0			

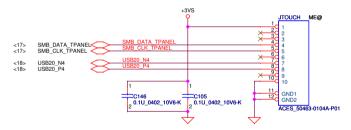
## TPM IC



## FingerPrint CONN.



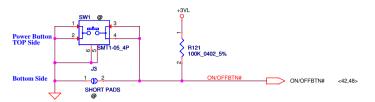
## **Touch Panel CONN.**



Security Classification	LC Future Center Secret Data			Title			7	_
Issued Date	2012/12/05	Deciphered Date	2014/12/05	TPM/TPanel/FP CONN.			LCFC	
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# PWR BTN/LID SW CONN.

### ON/OFF switch



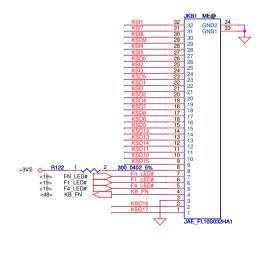
- 1. Power Button/B link to Function/B Conn. 10pin
- 2. Lid Switch



# KeyBoard CONN.(14")



KSIO C108 1 60 2 100P 0402 50V8J		KSO0	C109	1	<b>@</b>	2	100P 0402 50V8J
KSI1 C110 1 @ 2 100P_0402_50V8J	] '	KSO1	C111		0		100P_0402_50V8J
KSI2 C106 1 @ 2 100P 0402 50V8J	]	KSO2	C112	1	ø	2	100P_0402_50V8J
KSI3 C107 1 6 2 100P 0402 50V8J	Ţ	KSO3	C113	1	0	2	100P_0402_50V8J
KSI4 C114 1 60 2 100P_0402_50V8J	<b>.</b> .	KSO4	C115	1	ø	2	100P_0402_50V8J
KSI5 C116 1 60 2 100P_0402_50V8J	↓ .	KSO5	C117	1	ø	2	100P_0402_50V8J
KSI6 C118 1 60 2 100P_0402_50V8J	<b>.</b> .	KSO6	C119	1	ø	2	100P_0402_50V8J
KSI7 C120 1 60 2 100P 0402 50V8J	↓ .	KSO7	C121	1	ø	2	100P_0402_50V8J
"	1 .	KSO8	C122	1	ø	2	100P_0402_50V8J
F- 1 FD# 0404 4 FB 0 400D 0400 F0V01		KSO9	C123	1	ø	2	100P_0402_50V8J
Fn_LED# C124 1 @ 2 100P_0402_50V8J	┪.	KSO10	C125	1	ø	2	100P_0402_50V8J
F1_LED# C126 1 @ 2 100P_0402_50V8J	┪.	KSO11	C127	1	ø	2	100P_0402_50V8J
F4_LED# C128 1 60 2 100P 0402 50V8J	┪.	KSO12	C129	1	ø	2	100P_0402_50V8J
KB FN C130 1 6 2 100P 0402 50V8J	┪.	KSO13	C131	1	ø	2	100P_0402_50V8J
	Д.	KSO14	C132	1	ø	2	100P_0402_50V8J
CONN PIN define need double check	Υ .	KSO15	C133	1	ø	2	100P_0402_50V8J
		KSO16	C134	1	ø	2	100P_0402_50V8J
		KSO17	C135	1	ø	2	100P_0402_50V8J
					11		



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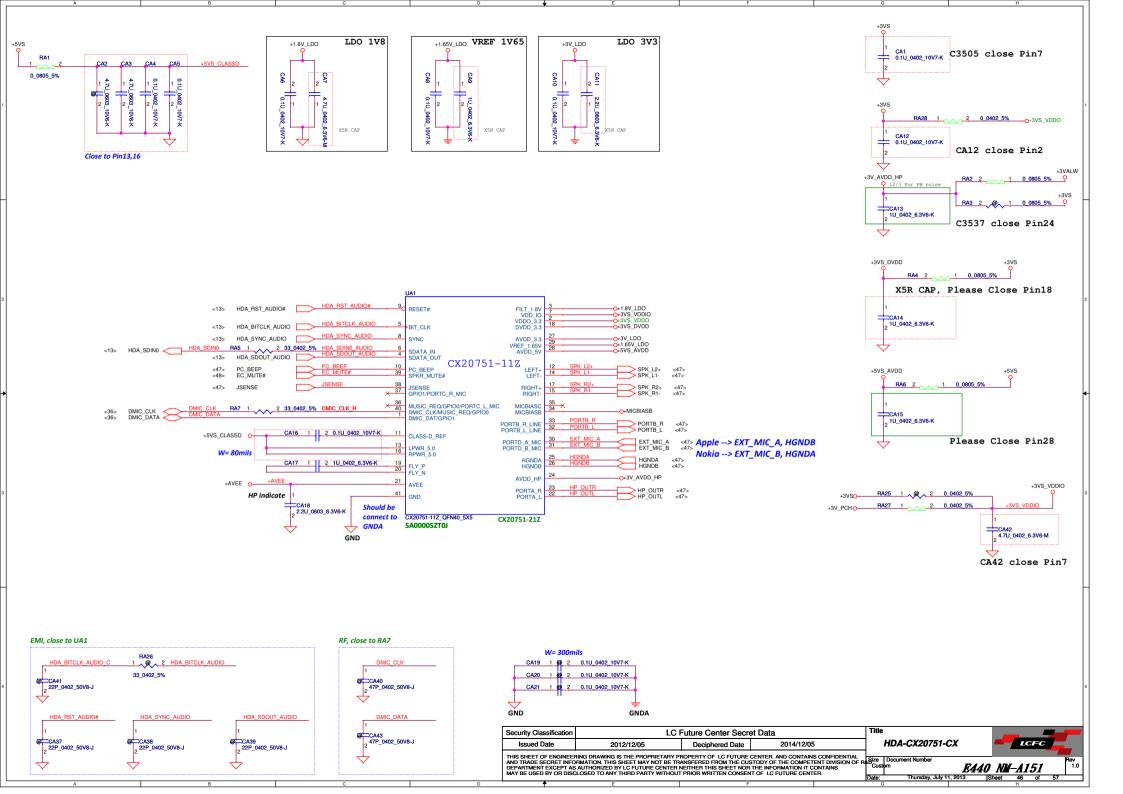
KB/PWR BTN CONN.

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OF Ra
Cushm

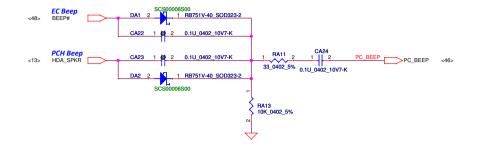
E440 NM-A151

Date: Thursday, July 11, 2013 | Sheet 45 of 57

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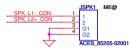
## РС Веер

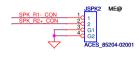


## Speaker OUT

	CA25	1 🙋	2	1000P_0402_50V7-K	SPK_L1CON
	CA26	1 @	2	1000P_0402_50V7-K	SPK_L2+_CON
	CA27	1 @	2	1000P 0402 50V7-K	SPK R1- CON
	CA28	1 (2)	2	1000P 0402 50V7-K	SPK R2+ CON
4	7				

## SPK CONN.



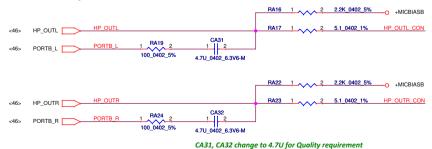


# EXT. MIC/LINE IN Apple --> EXT\_MIC\_A, HGNDB Nokia --> EXT\_MIC\_B, HGNDA

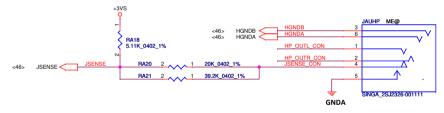


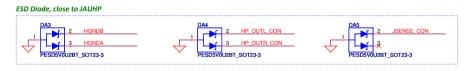
Changed CA29 & CA30 from 1uF to 2.2uF/X5R to meet Port-D(headset-Mic) THD+N <= -65 dB

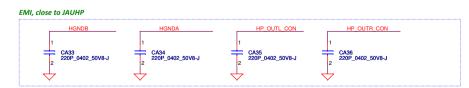
## HeadPhone/LINE OUT



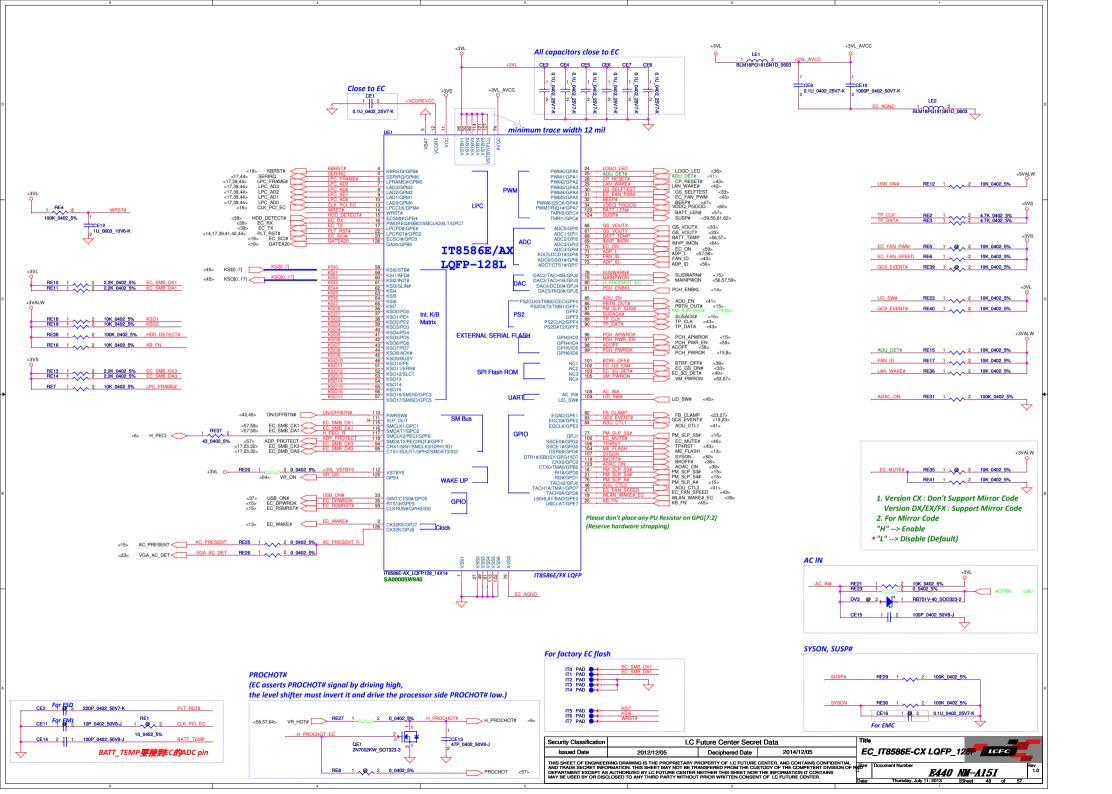
## **Audio Jack**

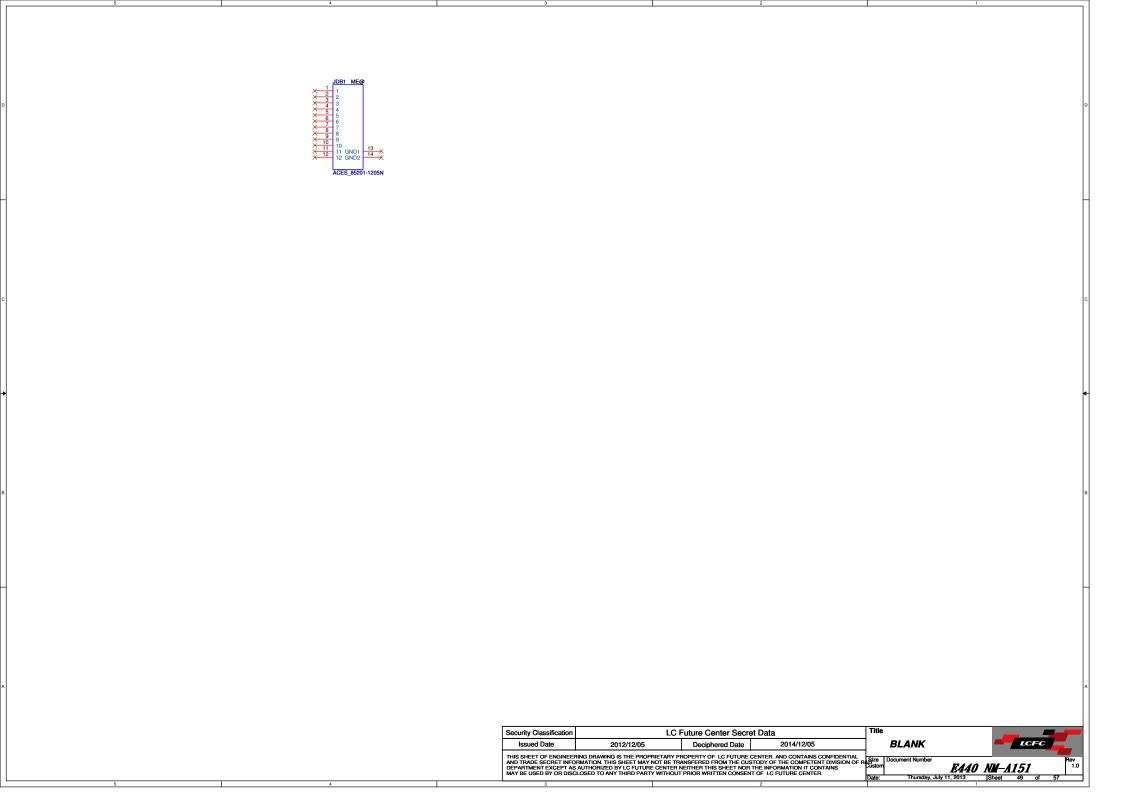


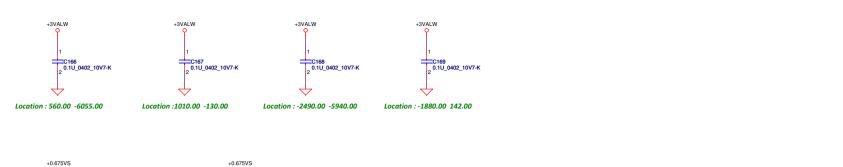


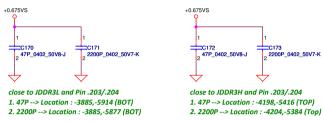


Security Classification	LC Future Center Secret Data							
Issued Date	2012/12/05	Deciphered Date	2014/12/05		HDA-HP/EXT N	MIC/SPI	CC I.CFC	
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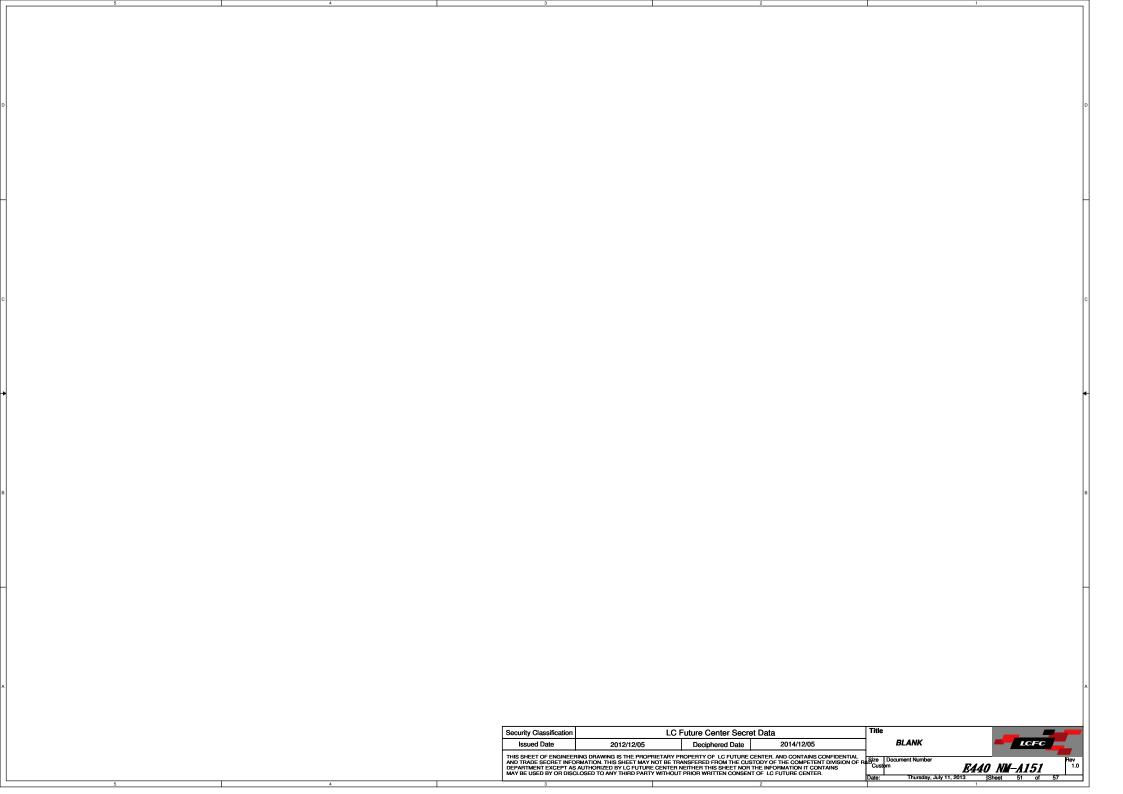
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DENTIAL SIZE Document Number

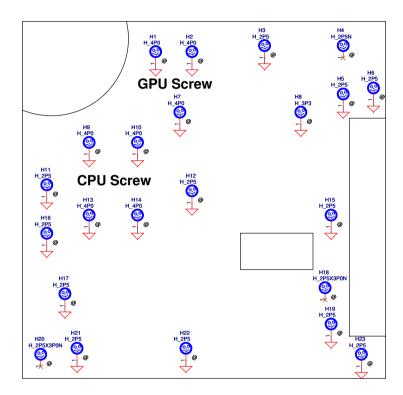
Custom B440 NN-A151

Rev
1.0

Date: Thursday, July 11, 2013 | Sheet 50 of 57



# Screw Hole













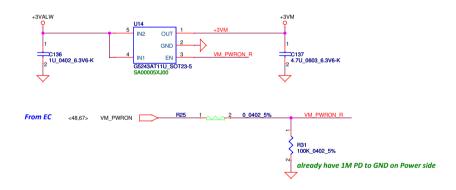




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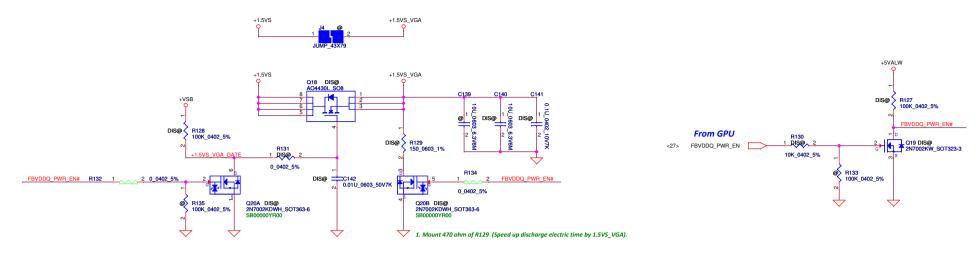
## +3VALW to +3VM

FOR SBA Function POWER(always mount)

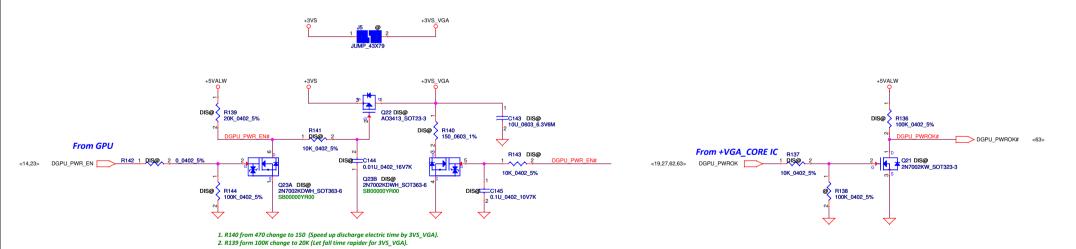


Security Classification	LC F	Title					
Issued Date	2012/12/05	Deciphered Date	2014/12/05	ONOFF SW/ PWR-B (	CONN/ ISPD	LCF	-c
AND TRADE SECRET INFO	RING DRAWING IS THE PROPRIETARY PRIPERING DRAWING IS THE PROPRIETARY PRIPERING THE TRAY NOT BE TRAY AUTHORIZED BY LC FUTURE CENTER NO LOSED TO ANY THIRD PARTY WITHOUT	ANSFERED FROM THE CUS IEITHER THIS SHEET NOR		Size Document Number Cust m JITR1_LA- Date: Thursday, July 1	-4141 <b>E540</b> 11, 2013  Sh		Rev 1.0 of 57

## +1.5V to +1.5VS\_VGA



## +3VS to +3VS\_VGA



Power Up -->

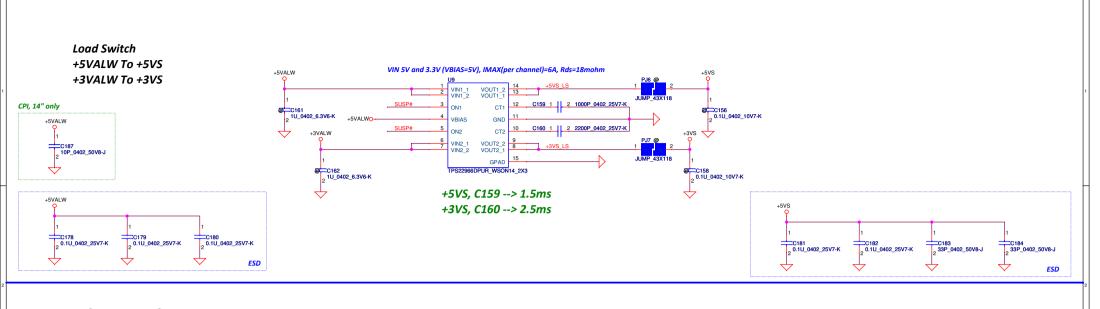
+3VS\_VGA (En:DGPU\_PWR\_EN)

+VGA\_CORE (En:NVDD\_PWR\_EN, POK:DGPU\_PWROK)

+1.5VS\_VGA (En:FBVDDQ\_PWR\_EN# = FB\_CLAMP and DGPU\_PWROK)

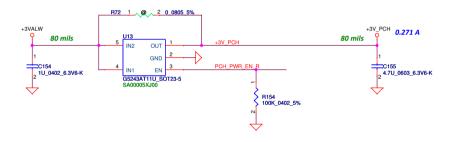
+1.05VS\_VGA (En:DGPU\_PWROK#)

Security Classification	LCF	uture Center Secre	et Data	Title			
Issued Date	2012/12/05	Deciphered Date	2014/12/05	D	OCKING USB30/DP	LCFC	
AND TRADE SECRET INFO	RING DRAWING IS THE PROPRIETARY PR RIMATION. THIS SHEET MAY NOT BE TRA BAUTHORIZED BY LC FUTURE CENTER IN CLOSED TO ANY THIRD PARTY WITHOUT	ANSFERED FROM THE CUS NEITHER THIS SHEET NOR		Size Do Custom	£440	NM-A151	Rev 1.0

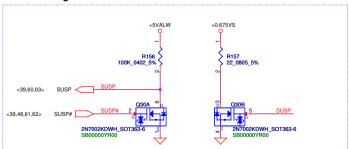


### +3VALW To +3V\_PCH

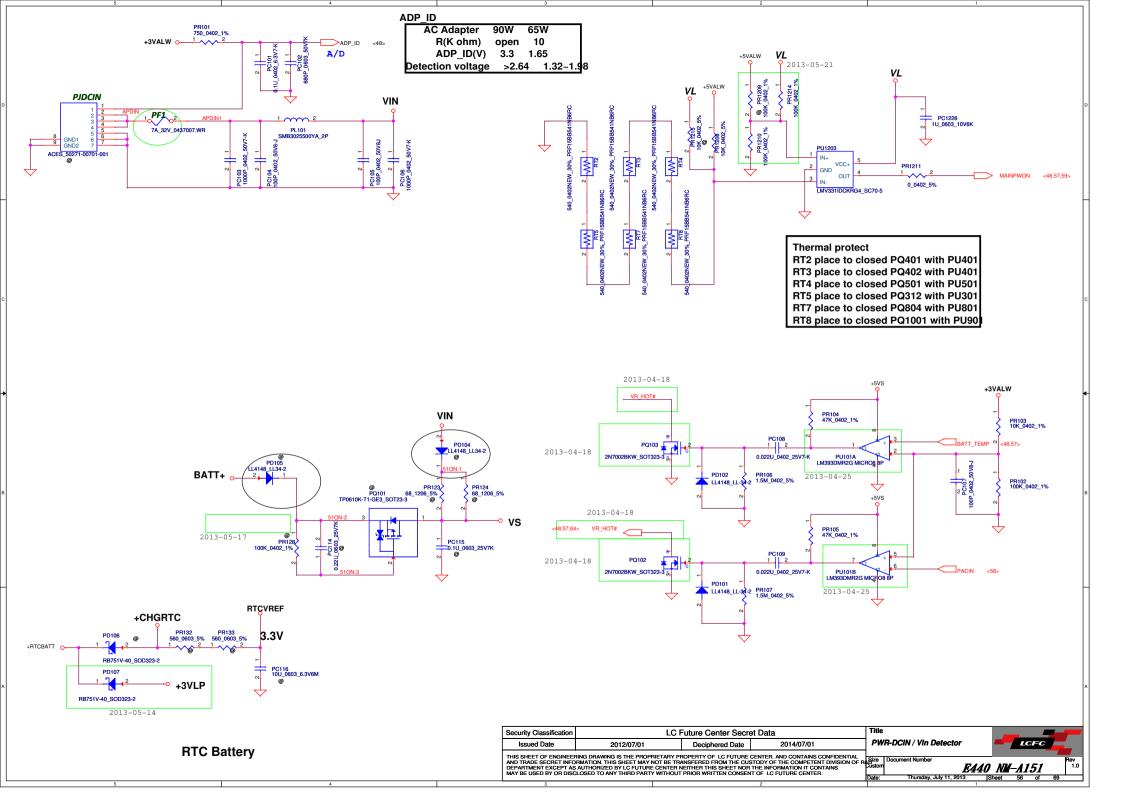


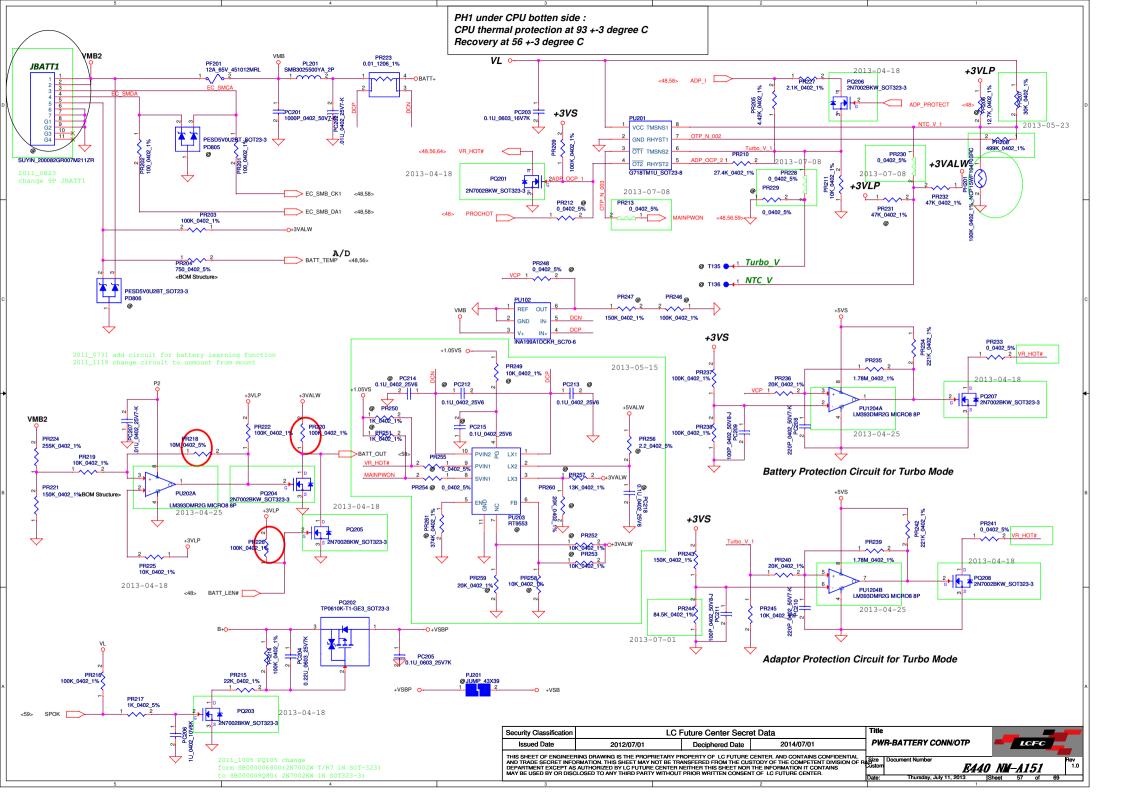


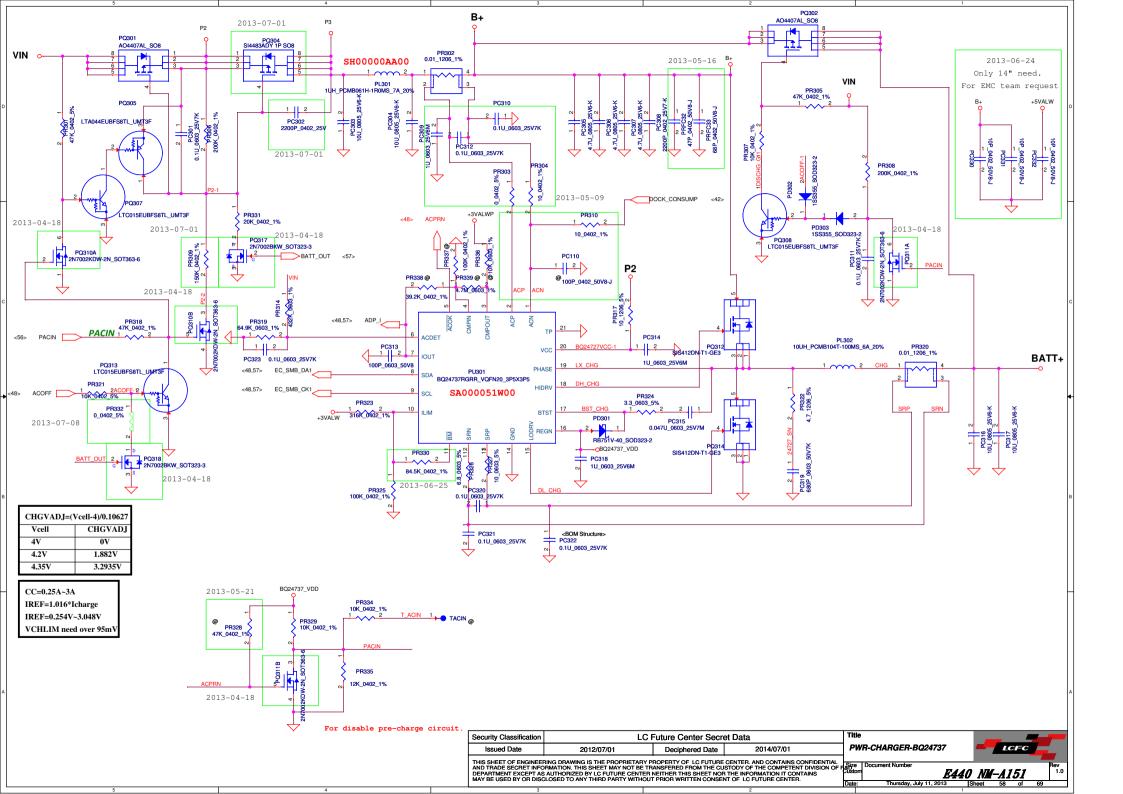
## For DisCharge

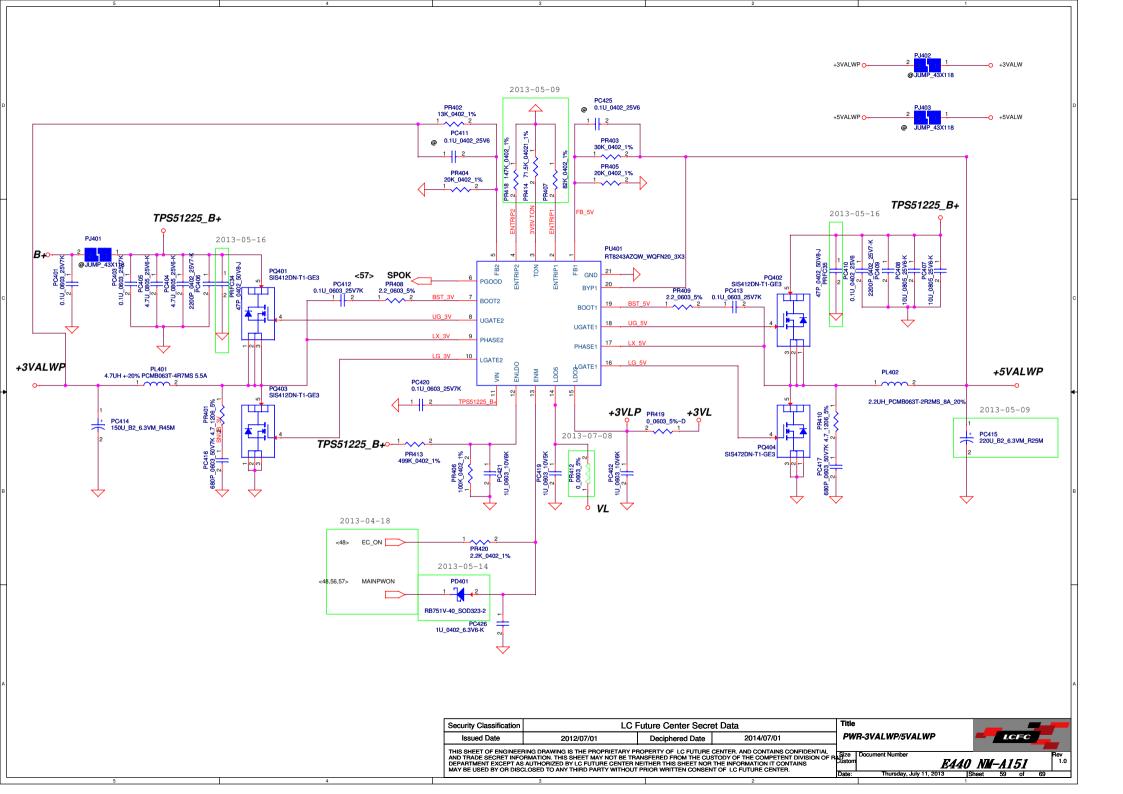


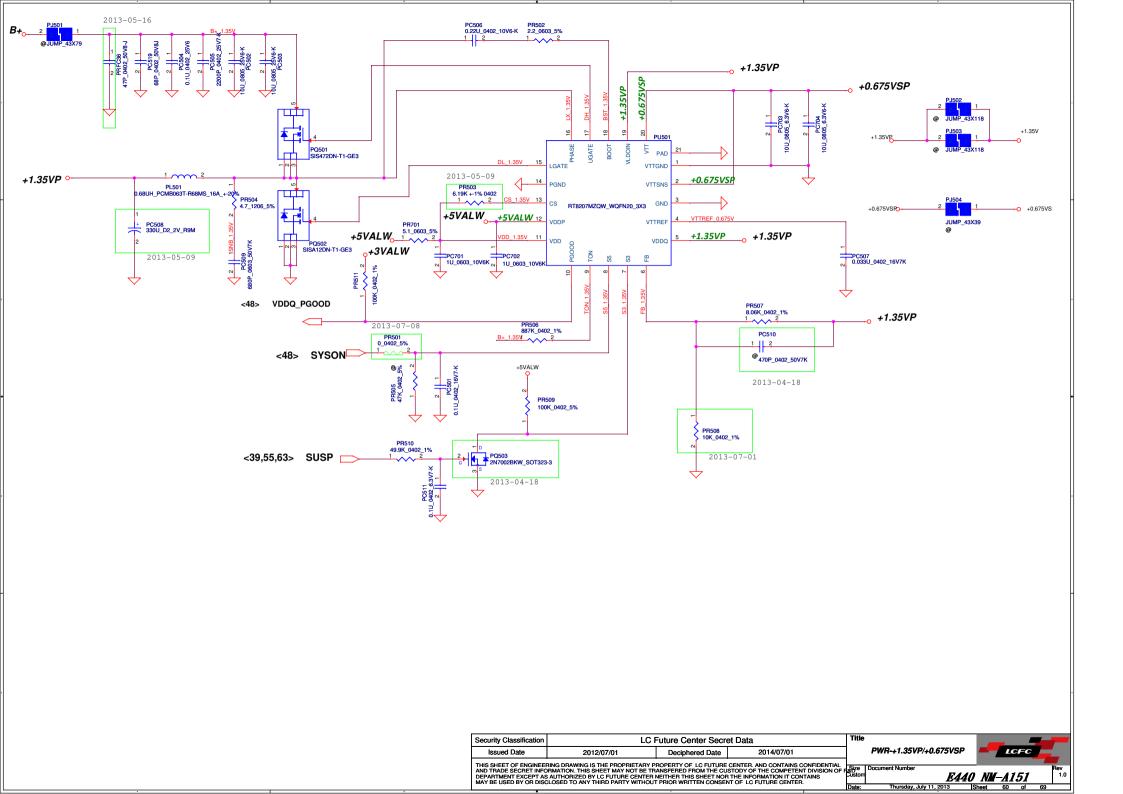
Security Classification	LC Future Center Secret Data			Title				
Issued Date	2012/12/05	Deciphered Date	2014/12/05		DC V TO V/VS INTERFACE	LCFC		
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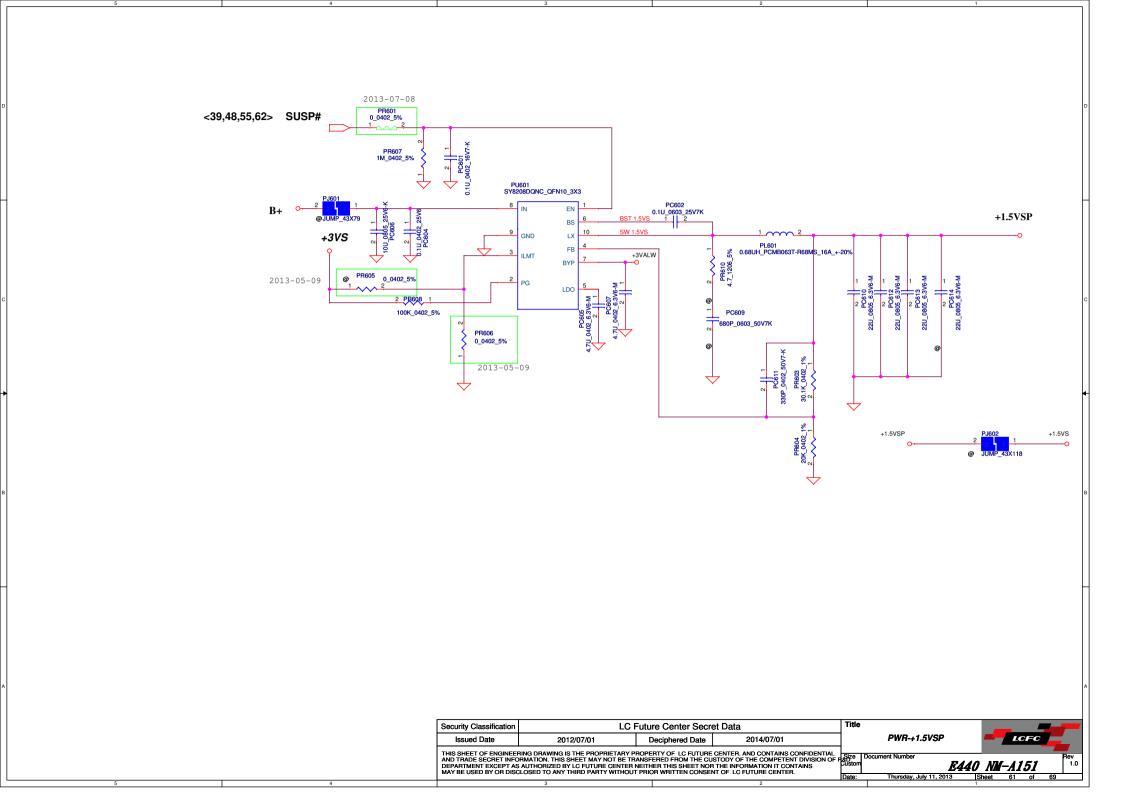


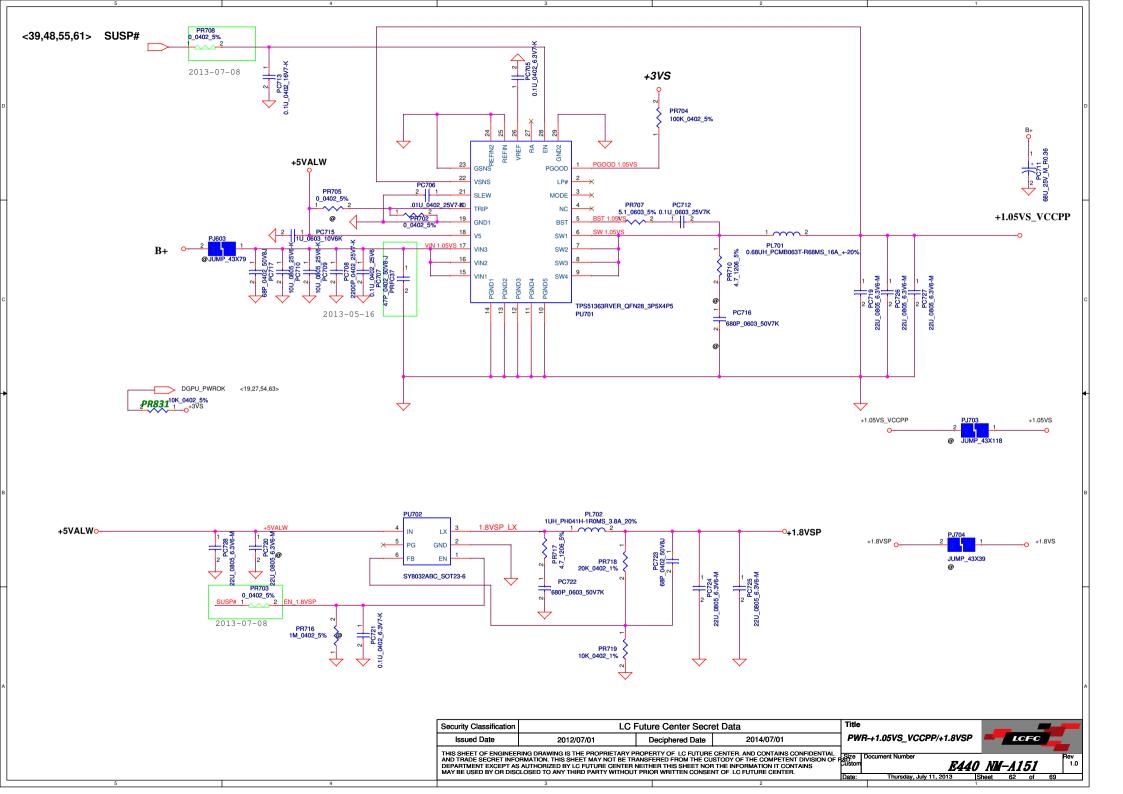


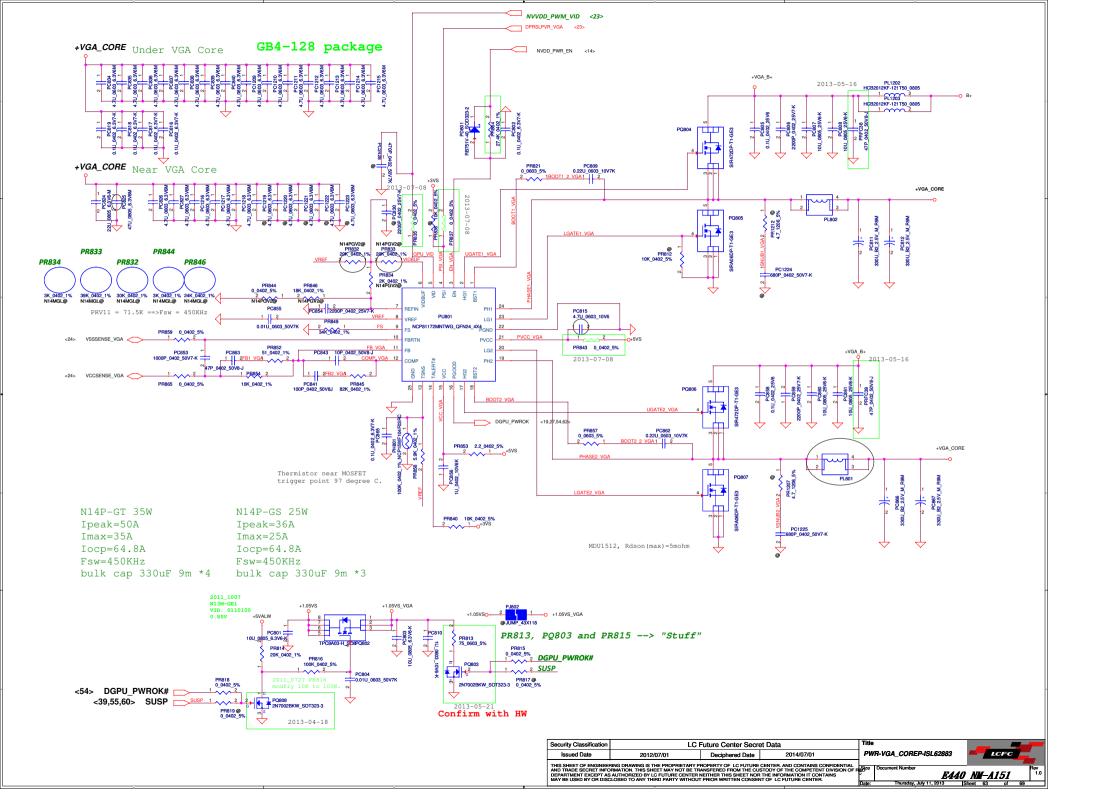


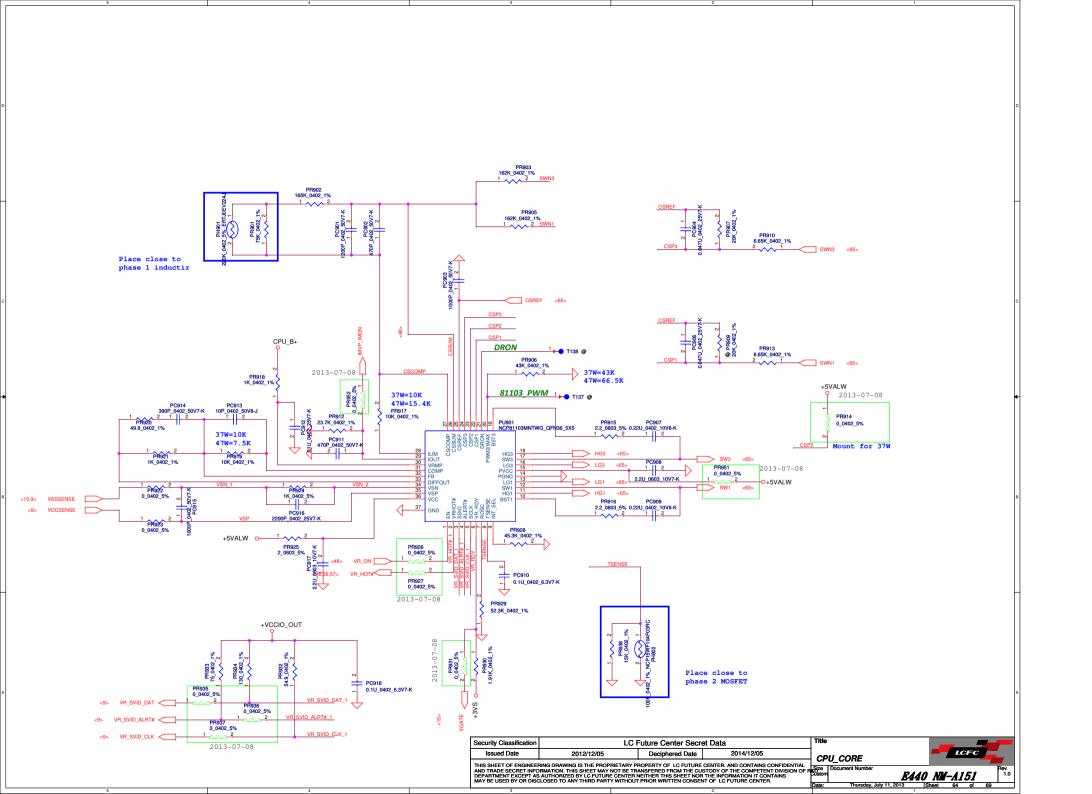


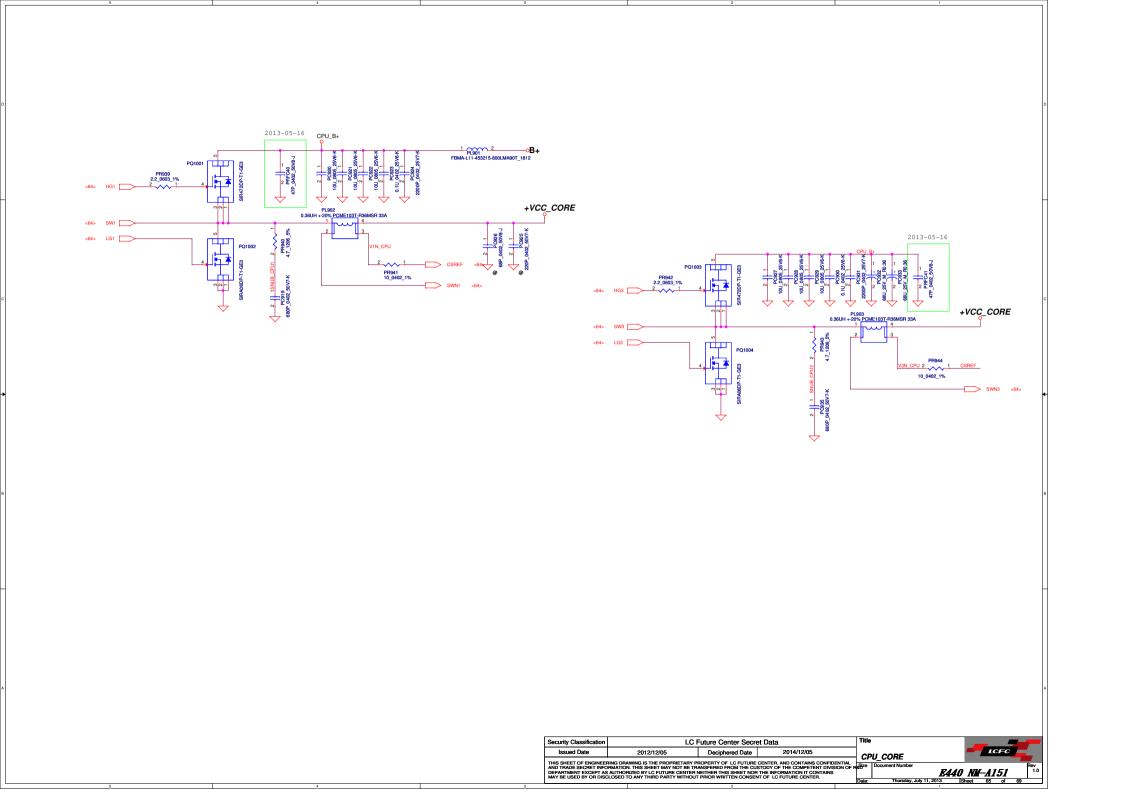


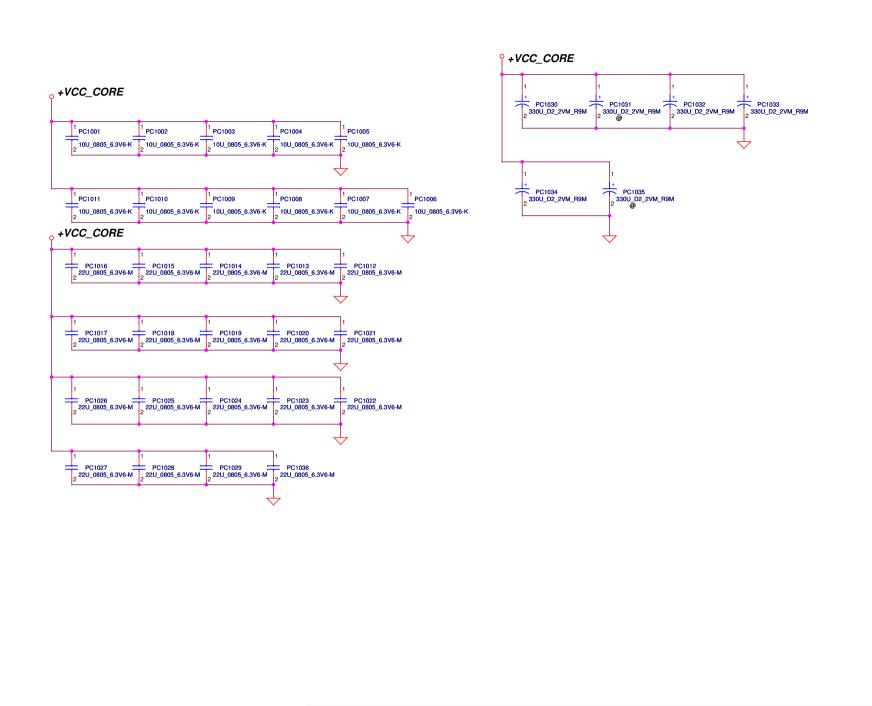








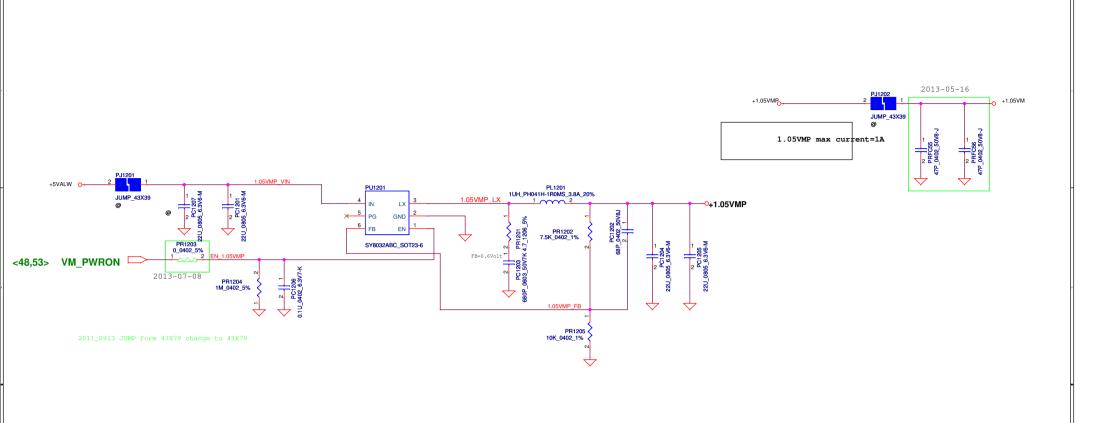


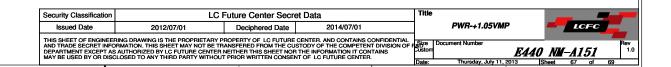


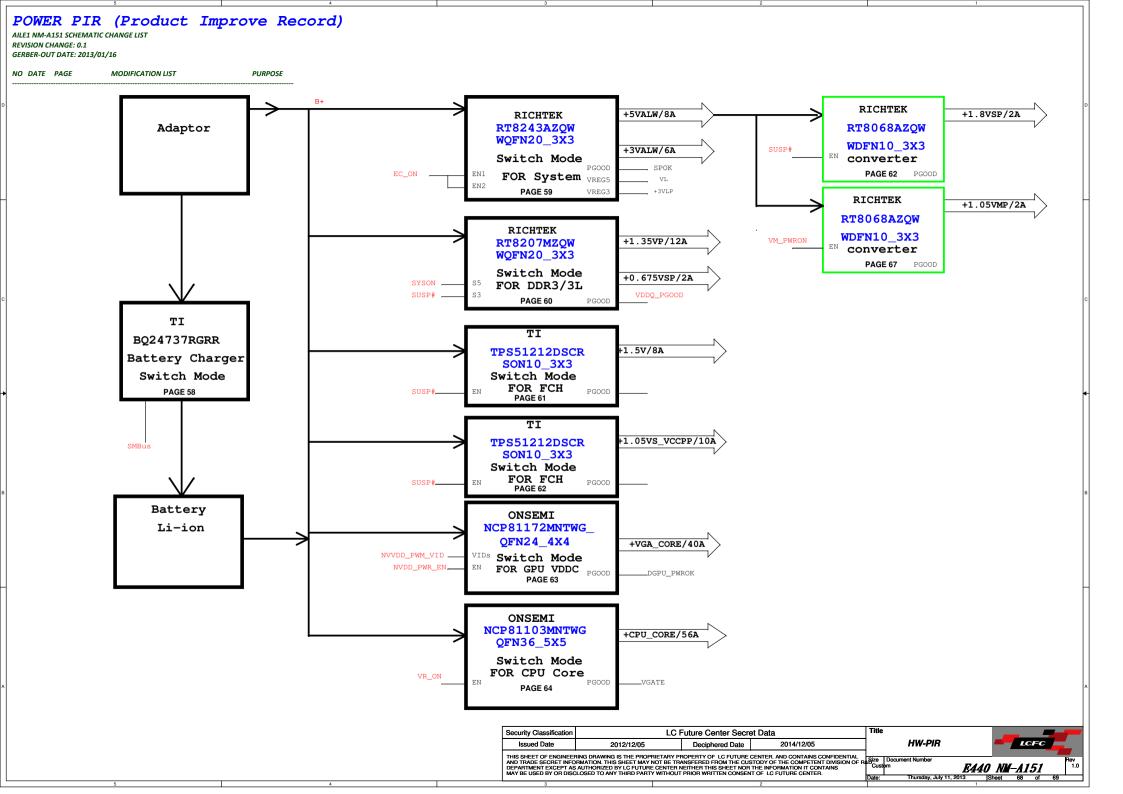
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HW PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1

GERBER-OUT DATE: 2013/01/16

 NO
 DATE
 PAGE
 MODIFICATION LIST
 PURPOSE

 01)
 03/14
 10
 R64
 Change R64 BOM structure from "@" to "DS3@"
 For Deep S3 Function

Security Classification	Con	npal Secret Data			Compal Electronics, Inc.	
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				Date:	Thursday, July 11, 2013 Sheet 69 of	69