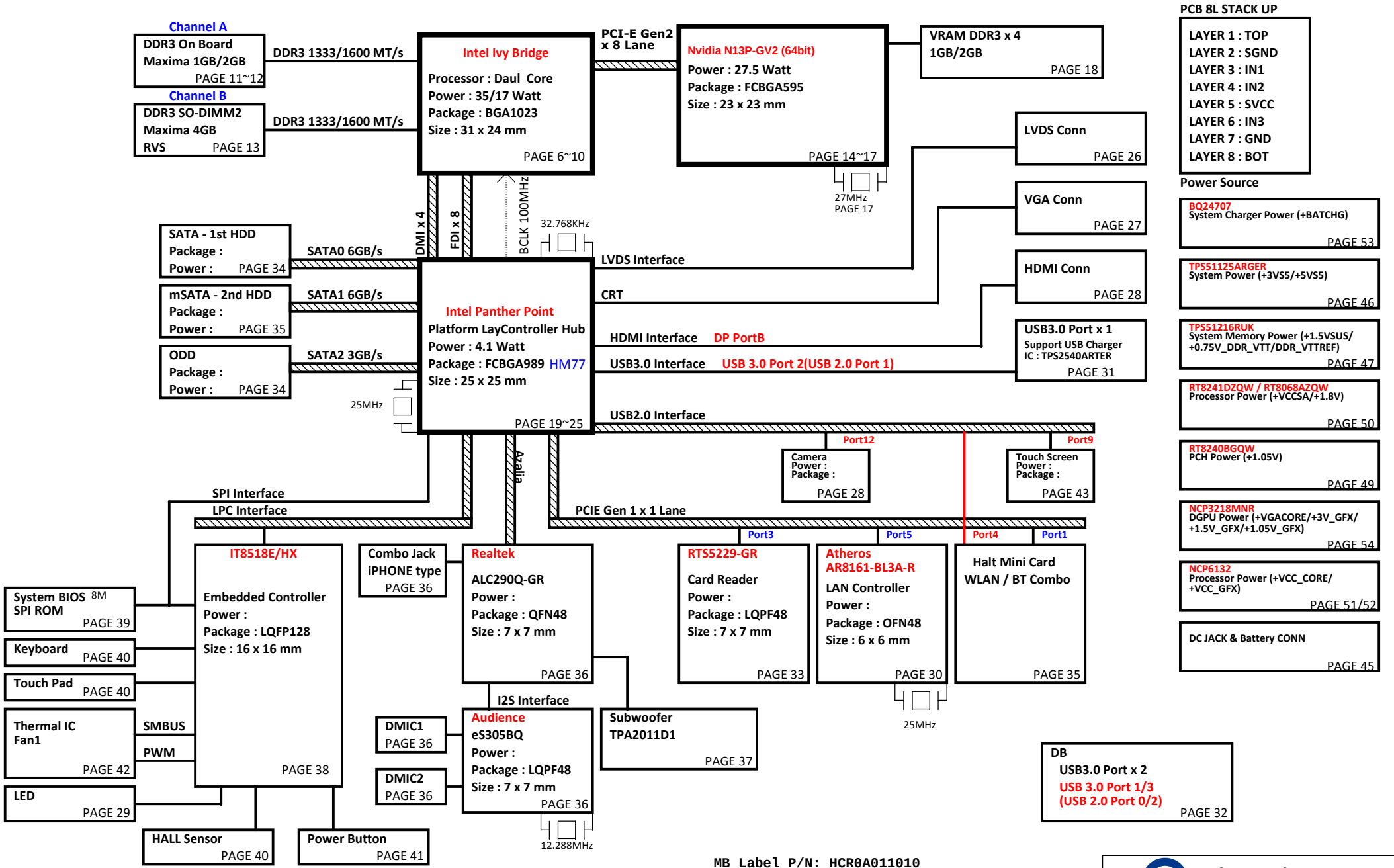
JWA 15.6" Intel Chief River Platform Block Diagram

01

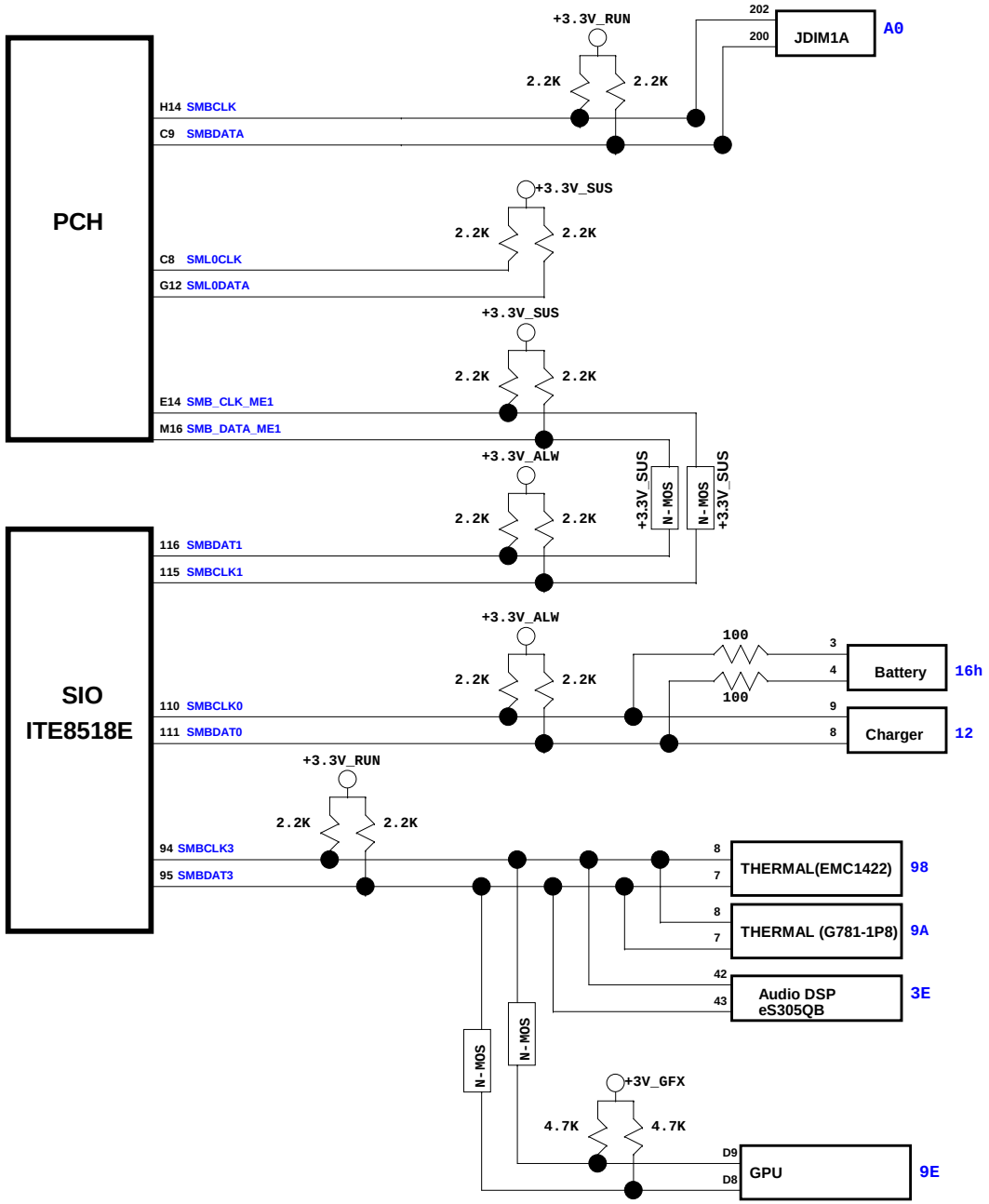


MB Label P/N: HCR0A011010

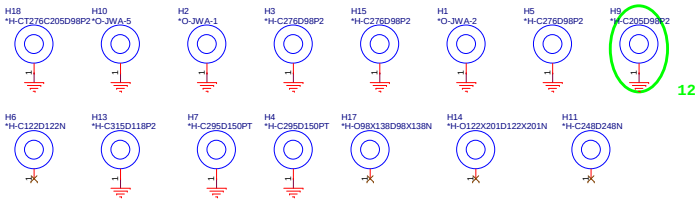
Quanta Computer Inc.

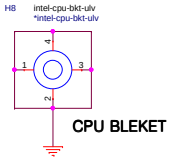
PROJECT : JWA

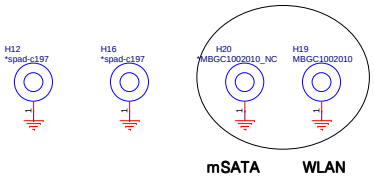
Size	Document Number	Rev
	Block Diagram	3A
Date: Tuesday, February 26, 2013	Sheet 1 of 54	



SCREW PAD







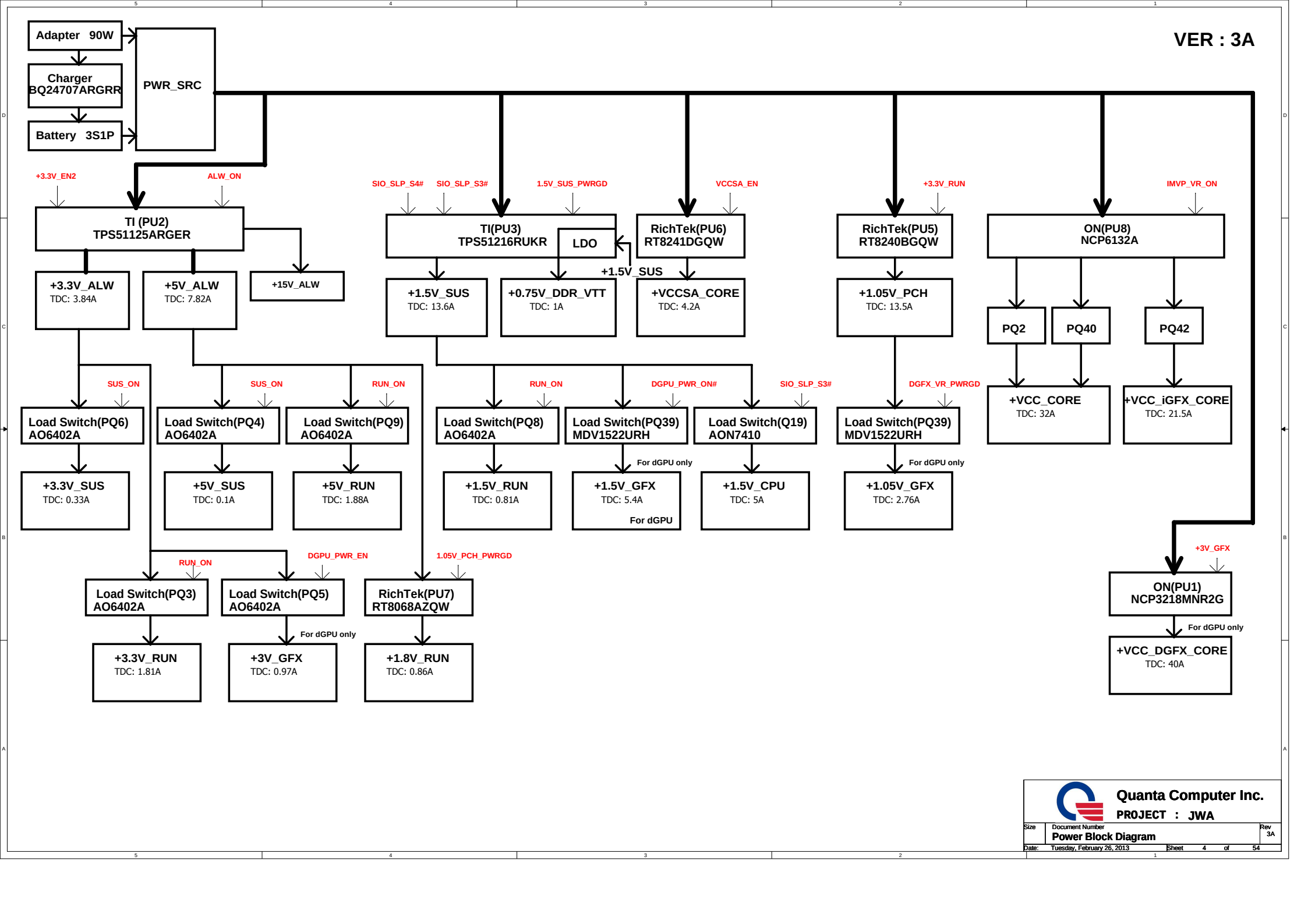
Function	IC	SMBus Address
DDR3	JDIM1A	A0h
Thermal IC	EMC1422	1001100xb (98h)
	G781-1P8	1001101xb (9Ah)
Charge IC	BQ24707ARGRR	0b0001001x (0x12h)
Battery	Battery	16h
Audio DSP	eS305QB	3Eh
GPU	N13P-GV2	9Eh

Quanta Computer Inc.
PROJECT : JWA
Size | Document Number: SMB/SCREW PAD | Rev 3A
Date: Friday, March 01, 2013 | Sheet 2 of 54

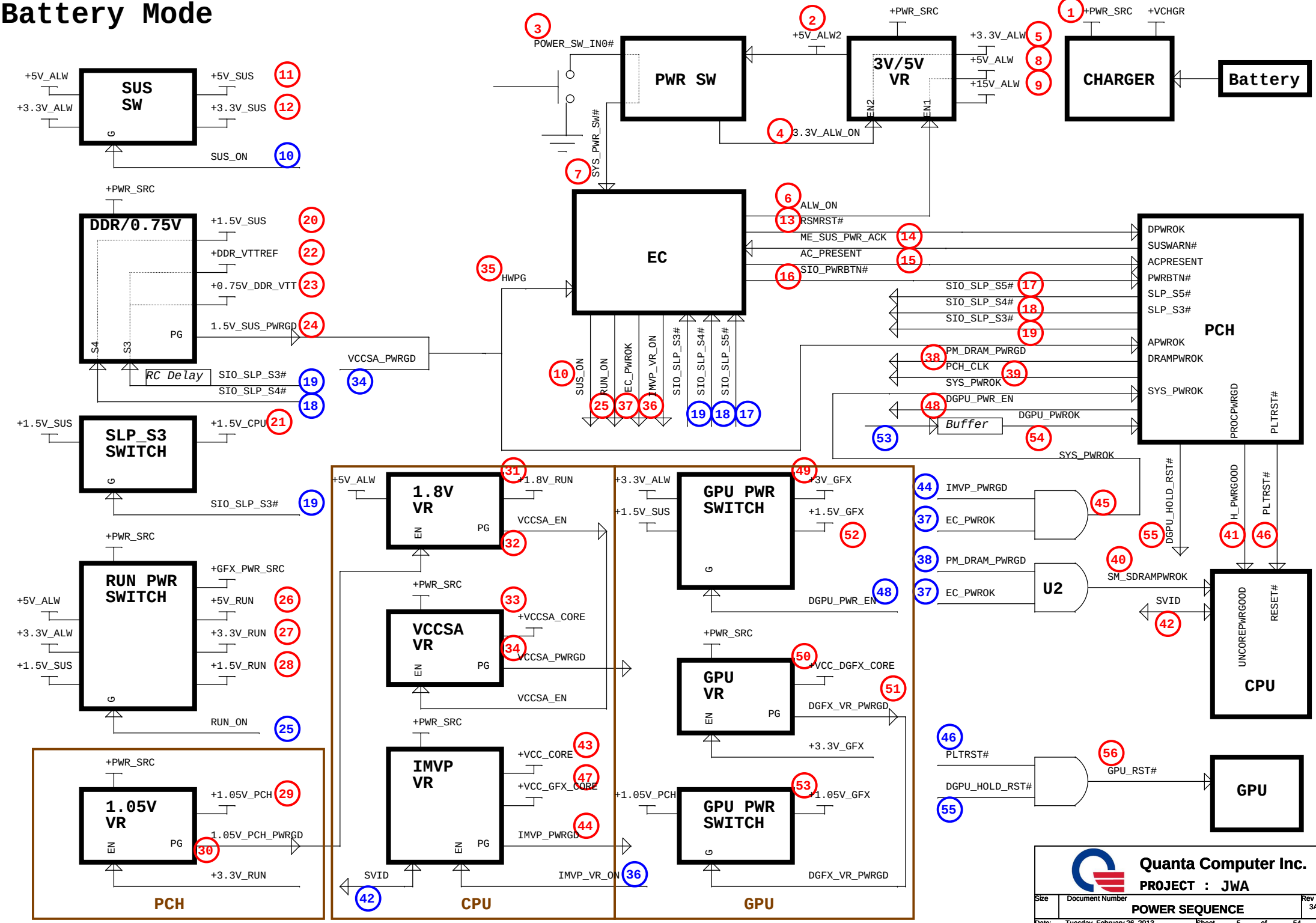
USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0 /Power share/debug port)
USB2	External port#3 (USB3.0)
USB3	NC
USB4	MiniCard 1 (WLAN/BT)
USB5	NC
USB6	NC
USB7	NC
USB8	NC
USB9	Touch panel
USB10	NC
USB11	NC
USB12	Camera
USB13	NC

SATA Master	Port Assignment
SATA0	HDD
SATA1	mSATA
SATA2	NC
SATA3	ODD
SATA4	NC
SATA5	NC

PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	NC
PCIE 3	Card reader
PCIE 4	NC
PCIE 5	LAN
PCIE 6	NC
PCIE 7	NC
PCIE 8	NC


VER : 3A
Adapter 90W
Charger BQ24707ARGRR
Battery 3S1P
PWR_SRC
+3.3V_EN2
ALW_ON
TI (PU2) TPS51125ARGER
+3.3V_ALW TDC: 3.84A
+5V_ALW TDC: 7.82A
+15V_ALW
SIO_SLP_S4#
SIO_SLP_S3#
1.5V_SUS_PWRGD
TI(PU3) TPS51216RUKR
LDO
+1.5V_SUS TDC: 13.6A
+0.75V_DDR_VTT TDC: 1A
VCCSA_EN
RichTek(PU6) RT8241DGQW
+1.5V_SUS
+VCCSA_CORE TDC: 4.2A
+3.3V_RUN
RichTek(PU5) RT8240BGQW
+1.05V_PCH TDC: 13.5A
IMVP_VR_ON
ON(PU8) NCP6132A
PQ2
PQ40
PQ42
+VCC_CORE TDC: 32A
+VCC_iGFX_CORE TDC: 21.5A
SUS_ON
Load Switch(PQ6) AO6402A
+3.3V_SUS TDC: 0.33A
SUS_ON
Load Switch(PQ4) AO6402A
+5V_SUS TDC: 0.1A
RUN_ON
Load Switch(PQ9) AO6402A
+5V_RUN TDC: 1.88A
RUN_ON
Load Switch(PQ8) AO6402A
+1.5V_RUN TDC: 0.81A
DGPU_PWR_ON#
Load Switch(PQ39) MDV1522URH
For dGPU only
+1.5V_GFX TDC: 5.4A
For dGPU
SIO_SLP_S3#
Load Switch(Q19) AON7410
+1.5V_CPU TDC: 5A
DGFX_VR_PWRGD
Load Switch(PQ39) MDV1522URH
For dGPU only
+1.05V_GFX TDC: 2.76A
RUN_ON
Load Switch(PQ3) AO6402A
+3.3V_RUN TDC: 1.81A
DGPU_PWR_EN
Load Switch(PQ5) AO6402A
For dGPU only
+3V_GFX TDC: 0.97A
1.05V_PCH_PWRGD
RichTek(PU7) RT8068AZQW
+1.8V_RUN TDC: 0.86A
+3V_GFX
ON(PU1) NCP3218MNR2G
For dGPU only
+VCC_DGFX_CORE TDC: 40A
Quanta Computer Inc.
PROJECT : JWA
Size
Document Number
Power Block Diagram
Rev 3A
Date: Tuesday, February 26, 2013
Sheet 4 of 54

Battery Mode

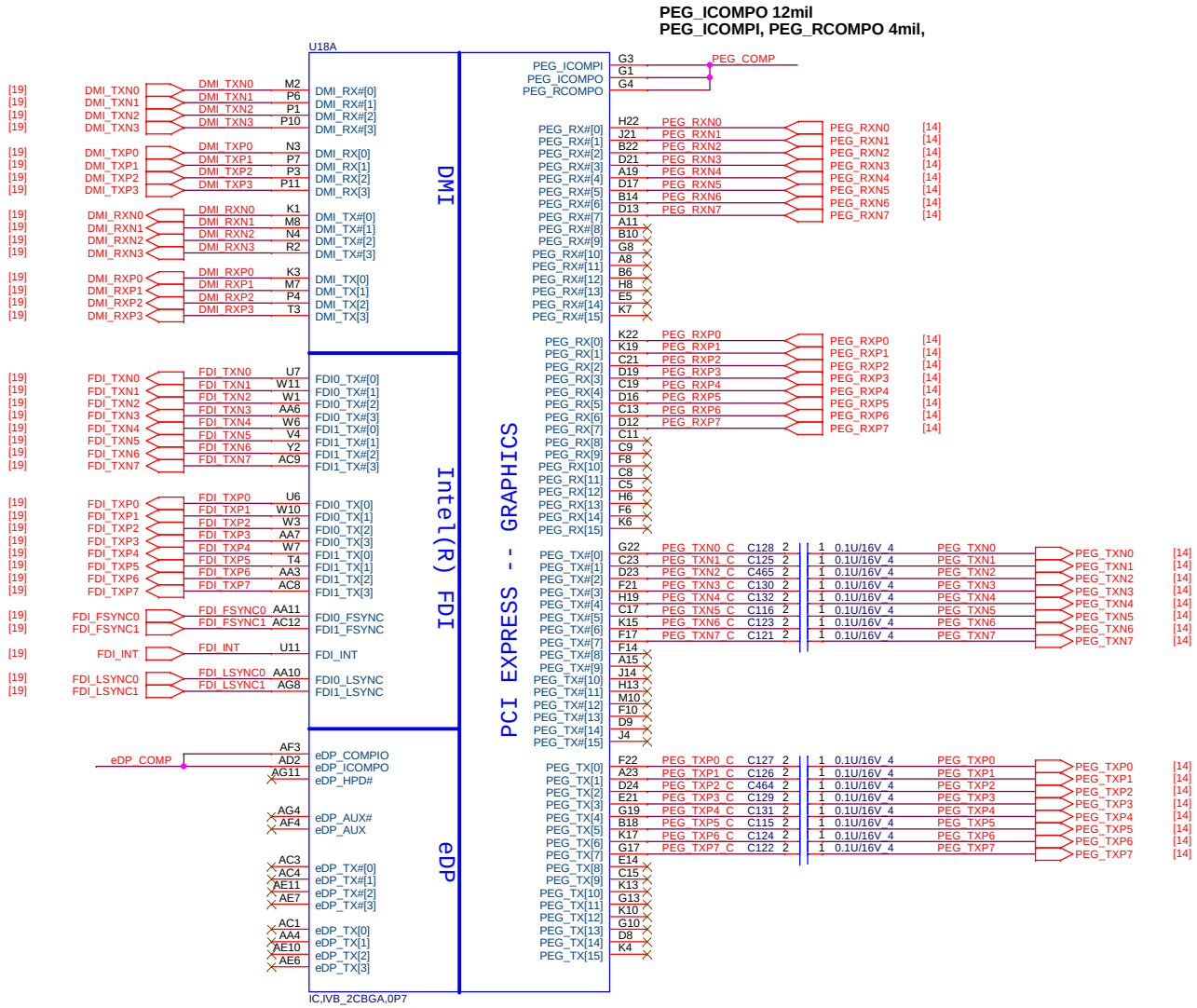


Quanta Computer Inc.
PROJECT : JWA

Size	Document Number	Rev
	POWER SEQUENCE	3A

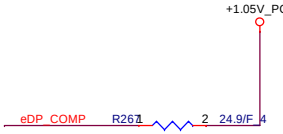
Date: Tuesday, February 26, 2013 Sheet 5 of 54

Ivy Bridge Processor (RESERVED, CFG)

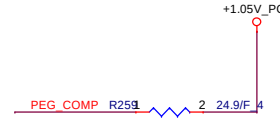


eDP_ICOMPO 12mil
eDP_COMPIO 4mil

DP & PEG Compensation



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed within 500 mils



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils

PEG_ICOMPO signals should be routed within 500 mils

CPU	QPN	
i7-3540M	AJ0QD5J8T00	Quanta B 35W
i5-3230M	AJSR0WXQT01	WIN BS 35W
i3-3120M	AJSR0TYRT01	WIN BS 35W

Quanta Computer Inc.
PROJECT : JWA

Size	Document Number	Rev
	Ivy Bridge 1/5	3A
Date: Tuesday, February 26, 2013	Sheet 6 of 54	

Ivy Bridge Processor (CLK,MISC,JTAG)

U18B

SNB_IVB# N.A at SNB EDS #27637 0.7v1

[22] H_SNB_IVB# — H_SNB_IVB# — F49 PROC_SELECT#

TP1 — H_CPUDET# — C57 PROC_DETECT#

TP1 — CATERR# — C49 CATERR#

[38] PECI_EC — PECI_EC — R46 1 2 43_4 — PECI_EC_R — A48 PECI

[38,51,53] IMVP7_PROCHOT# — IMVP7_PROCHOT# — R247 1 2 56_4 — H_PROCHOT# — C45 PROCHOT#

Over 130 degree C will drive low [24] PM_THRMTRIP# — PM_THRMTRIP# — D45 THERMTRIP#

[19] H_PM_SYNC — H_PM_SYNC — C48 PM_SYNC

[24] H_PWRGOOD — H_PWRGOOD — B46 UNCOREPWRGOOD

10K_4 2 1 R52

SM_DRAMPWROK — BE45 SM_DRAMPWROK

[22,30,33,35,38] PLTRST# — PLTRST# — R250 2 1 1.5K/F_4 — CPU_PLTRST#_R — D44 RESET#

R251 750/F_4

MISC | THERMAL | PWR MANAGEMENT

CLOCKS

BCLK — J3 CLK_CPU_BCLKP — CLK_CPU_BCLKP [23]

BCLK# — H2 CLK_CPU_BCLKN — CLK_CPU_BCLKN [23]

DPLL_REF_CLK — AG3 CLK_DP_P_R — R265 1 2 1K_4

DPLL_REF_CLK# — AG1 CLK_DP_N_R — R266 1 2 1K_4 — +1.05V_PCH

DDR3 MISC

SM_DRAMRST# — AT30 CPU_DRAMRST#

SM_RCOMP[0] — BF44 SM_RCOMP_0 — R271 1 2 140/F_4

SM_RCOMP[1] — BE43 SM_RCOMP_1 — R270 1 2 25.5/F_4

SM_RCOMP[2] — BG43 SM_RCOMP_2 — R269 1 2 200/F_4

SM_RCOMP_0, SM_RCOMP_1 20mil / SM_RCOMP_2 15mil.

JTAG & BPM

PRDY# — N53

PREQ# — N55

TCK — L56 XDP_TCLK — TP60

TMS — L55 XDP_TMS — TP58

TRST# — J58 XDP_TRST# — TP59

TDI — M60 XDP_TDI — TP62

TDO — L59 XDP_TDO — TP61

DBR# — K58 XDP_DBRST# — R256 1 2 1K_4 — +3.3V_RUN

BPM#[0] — G58

BPM#[1] — E55

BPM#[2] — E59

BPM#[3] — G55

BPM#[4] — G59

BPM#[5] — H60

BPM#[6] — J59

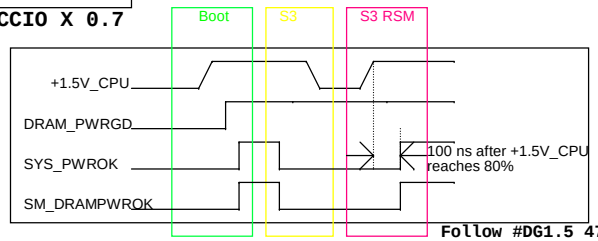
BPM#[7] — J61

IC,IVB_2CBGA,0P7

+1.05V_PCH

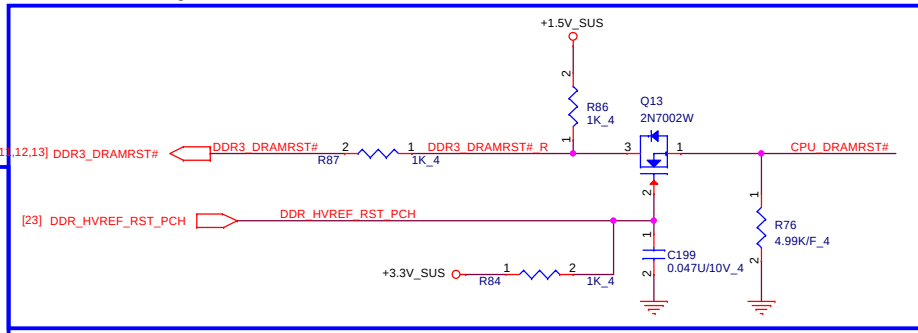
IMVP7_PROCHOT# R246 2 1 62_4

Intel spec VinH min =VCCIO X 0.7

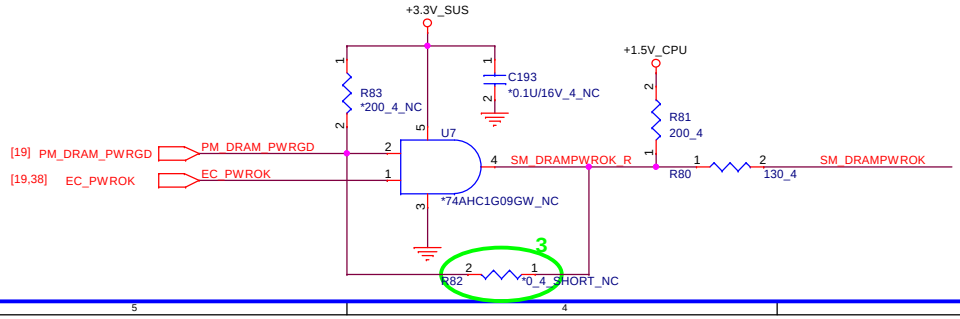


Follow #DG1.5 471984 P119

Follow #DG1.5 471984 P130
DRAMRST# Routing Illustration



Follow #DG1.5 471984 P128
DDR Power Gating Topology



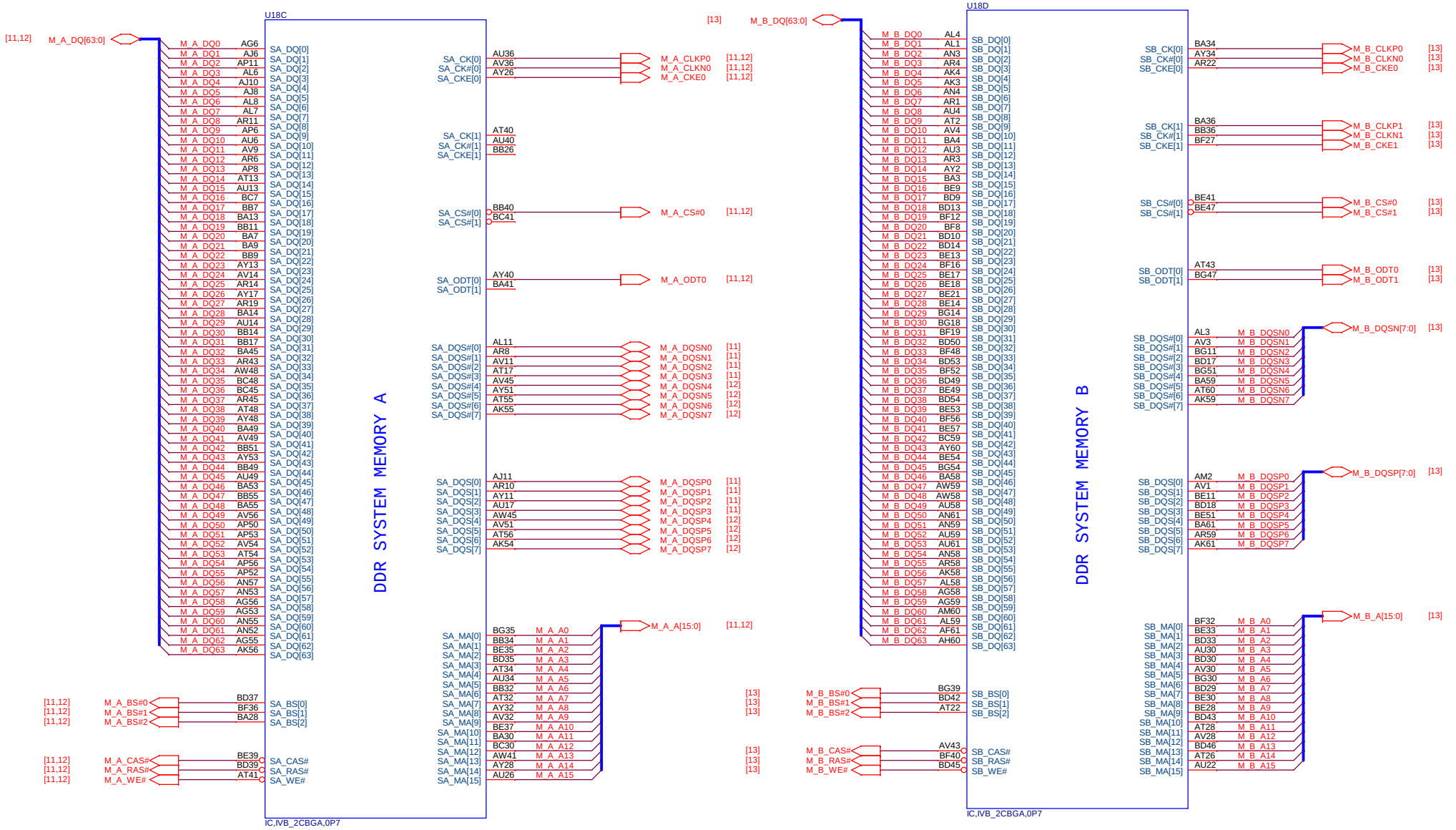
Quanta Computer Inc.

PROJECT : JWA

Size	Document Number	Rev
	Ivy Bridge 2/5	3A

Date: Tuesday, February 26, 2013 Sheet 7 of 54

Ivy Bridge Processor (DDR3)



Quanta Computer Inc.			
PROJECT : JWA			
Size	Document Number		Rev
	Ivy Bridge 3/5		3A
Date: Tuesday, February 26, 2013	Sheet 8	of 54	

Ivy Bridge Processor

Ivy Bridge Processor (GRAPHIC POWER)

CPU Core Power
SNB: 53A
IVY: 53A
10uF x 24

1.05V_PCH
SNB: 8.5A
IVY: 8.5A
10F x12

CPU VGT
SNB: 21.5A
IVY: 33A
10uF x 12

CPU MCH
SNB: 5A
IVY: 5A
10uF x 6

CPU VCCPL
SNB: 1.2A
IVY: 1.2A
10uF x 1
1uF x 2

CPU SA
SNB: 6A
IVY: 6A
10uF x 3

POWER

CORE SUPPLY

PEG IO AND DDR IO

QUIET RAILS

SVID

SENSE LINES

GRAPHICS

DDR3 - 1.5V RAILS

VREF

1.8V RAIL

SA RAIL

VCCSA VID Lines

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	100Ω	27-33Ω	<25 mils
VCCAXG_SENSE / VSSAXG_SENSE	100Ω		
VCCIO_SENSE / VSS_SENSE_VCCIO	10Ω	55Ω	
VCCSA	100Ω		

Only BGA

Take care Q3 Vgs(MAX)=2.5

S3 Power reduce

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

Place PU resistor close to CPU

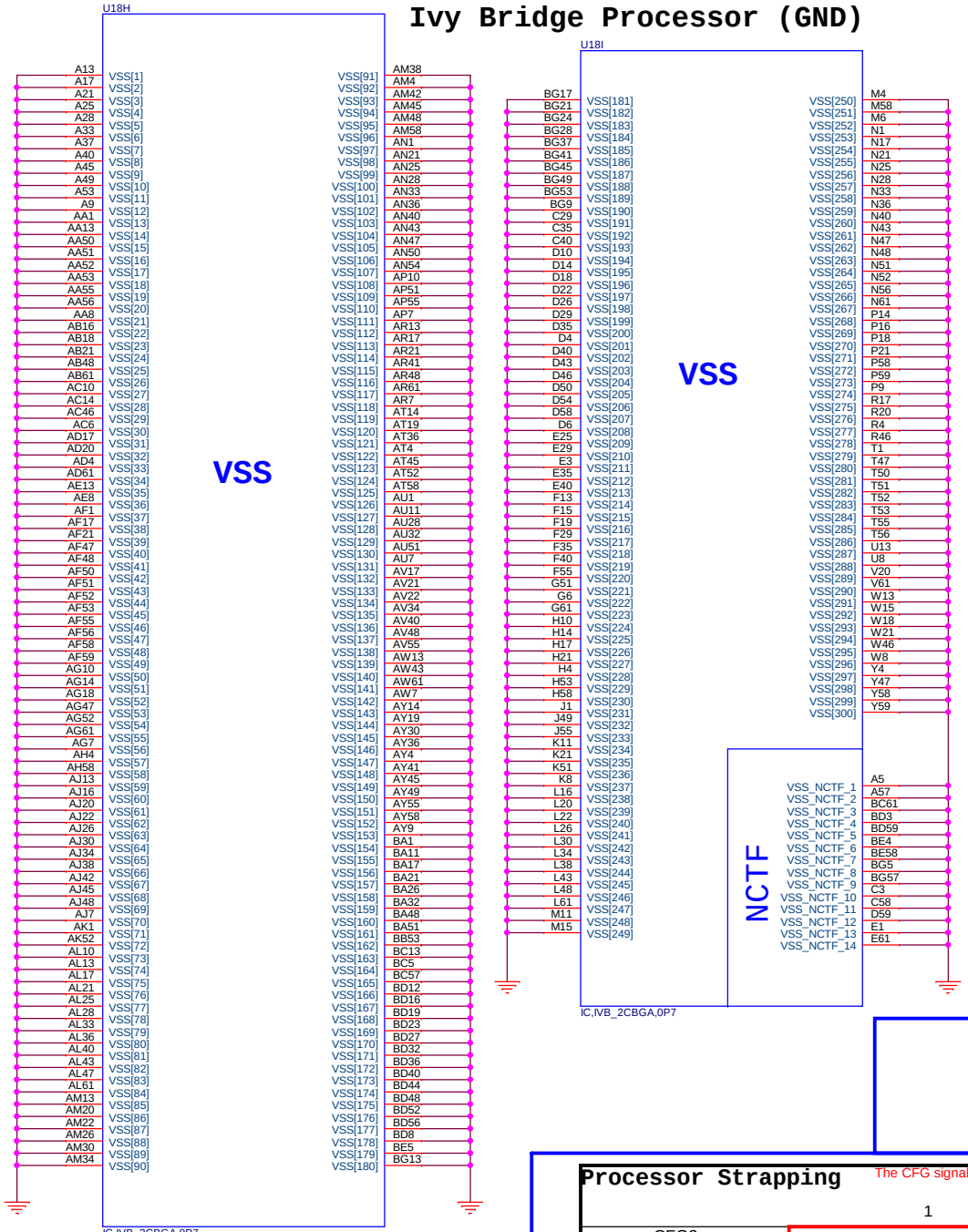
SVID DATA

Place PU resistor close to CPU

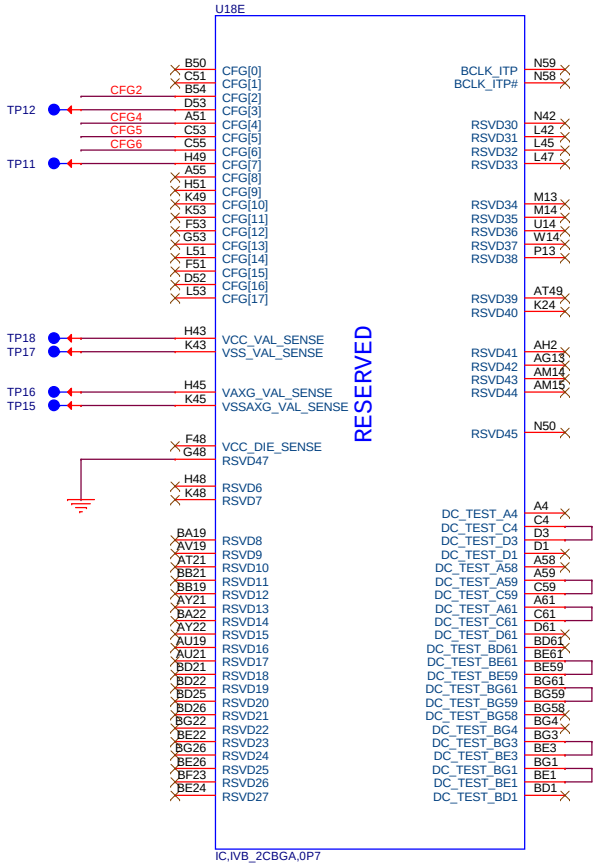
SVID ALERT

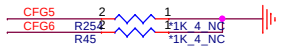
Quanta Computer Inc.
PROJECT : JWA
Ivy Bridge 4/5
Size: Document Number: Rev 3A
Date: Tuesday, February 26, 2013 Sheet 9 of 54

Ivy Bridge Processor (GND)



Ivy Bridge Processor (RESERVED, CFG)





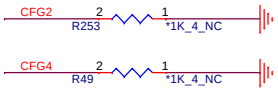
CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP



Quanta Computer Inc.
PROJECT : JWA

Size	Document Number	Rev
	Ivy Bridge 5/5	3A
Date: Tuesday, February 26, 2013	Sheet 10 of 54	

DDR3 TERMINATION FOR MEMORY DOWN

Please these resistor closely DIMMA,all trace length<750 mil.

16

D0

U9

D1

U8

+0.75V_DDR_VTT

RN4: M_A_A1, M_A_A2, M_A_A5, M_A_BS#1 — 36X4

RN5: M_A_A13, M_A_A11, M_A_A9, M_A_A4 — 36X4

RN3: M_A_A3, M_A_A12, M_A_A0, M_A_BS#2 — 36X4

RN6: M_A_A8, M_A_A6, M_A_A7, M_A_A14 — 36X4

RN2: M_CS#0, M_ODT0, M_A_A10, M_A_BS#0 — 36X4

RN1: M_A_WE#, M_A_CAS#, M_A_RAS#, M_A_CKE0 — 36X4

R133 36/F_4 — M_A_A15

M_A_A[15:0] [8,12]

M_A_DQ[15:0] [8]

M_A_DQ[31:16] [8]

M_A_DQSP1 M_A_DQSP0 M_A_DQSN1 M_A_DQSN0 [8]

M_A_DQSP3 M_A_DQSP2 M_A_DQSN3 M_A_DQSN2 [8]

M_A_BS#0 M_A_BS#1 M_A_BS#2 M_A_CS#0 M_A_CLKP0 M_A_CLKN0 M_A_CKE0 M_A_CAS# M_A_RAS# M_A_WE# [8,12]

M_A_ODT0 [8,12]

+1.5V_SUS

M_A_CLKP0 — R110 30.1/F_4 — C297 1.8P/50V_4 — R114 30.1/F_4 — C235 0.1U/10V_4 — M_A_CLKN0

+M_VREF_DQ_MD

+M_VREF_CA_MD

C288 0.1U/10V_4 — C257 0.1U/10V_4

C298 0.1U/10V_4 — C258 0.1U/10V_4

RESET# — DDR3_DRAMRST#[7,12,13]

ZQ — DDR_ZQ1 — R127 240/F_4

ZQ — DDR_ZQ2 — R139 240/F_4

96-BALL SDRAM DDR3

H5TC4G63AFR-11C

bga96-samsung-k4b4g1646b-hck0

+0.75V_DDR_VTT: C212 1U/6.3V_4, C239 1U/6.3V_4, C322 1U/6.3V_4, C268 1U/6.3V_4, C282 1U/6.3V_4, C307 1U/6.3V_4

+1.5V_SUS: C306 1U/10V_6, C226 1U/10V_6, C227 1U/10V_6, C244 1U/10V_6, C270 1U/10V_6, C264 1U/10V_6, C219 1U/10V_6, C233 1U/10V_6

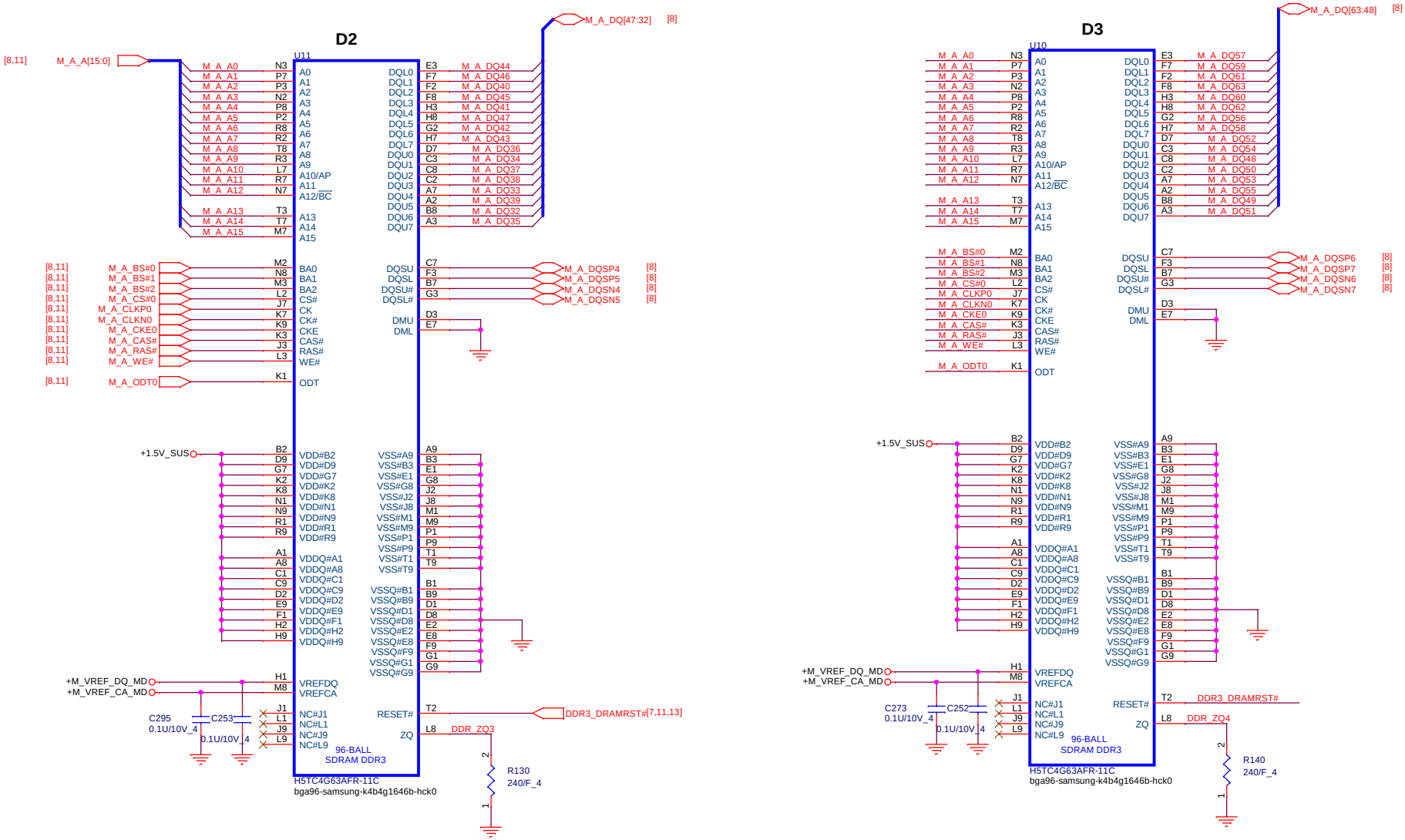
+1.5V_SUS: C251 10U/6.3V_6, C265 10U/6.3V_6, C223 10U/6.3V_6, C230 10U/6.3V_6, C243 10U/6.3V_6, C245 10U/6.3V_6, C314 10U/6.3V_6, C232 10U/6.3V_6

+1.5V_SUS — R146 1K/F_4 — R129 1K/F_4 — +M_VREF_DQ_MD

+1.5V_SUS — R141 1K/F_4 — R131 1K/F_4 — +M_VREF_CA_MD

Hynix: Vendor PN is H5TC4G63AFR-11C. Quanta buy QPN is AKD5PGWTW05.

Quanta Computer Inc.		
PROJECT : JWA		
Size	Document Number: DDR3 (A) On Board_A,1Rank	Rev: 3A
Date: Tuesday, February 26, 2013	Sheet 11 of 54	



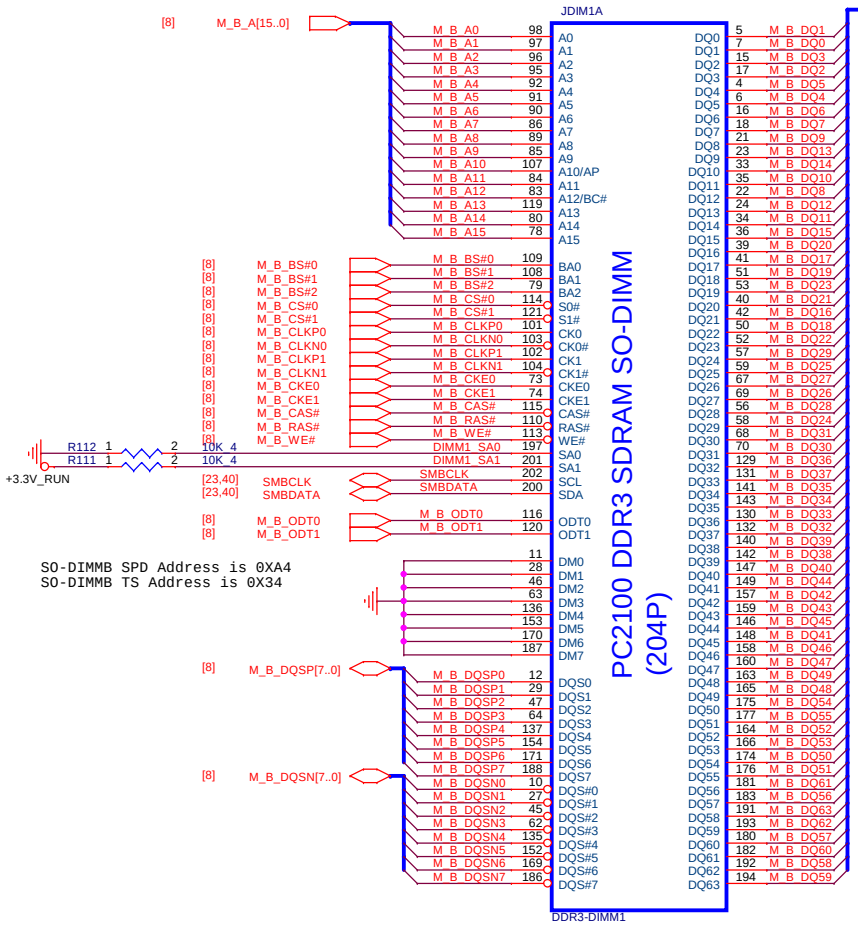
Quanta Computer Inc.

PROJECT : JWA

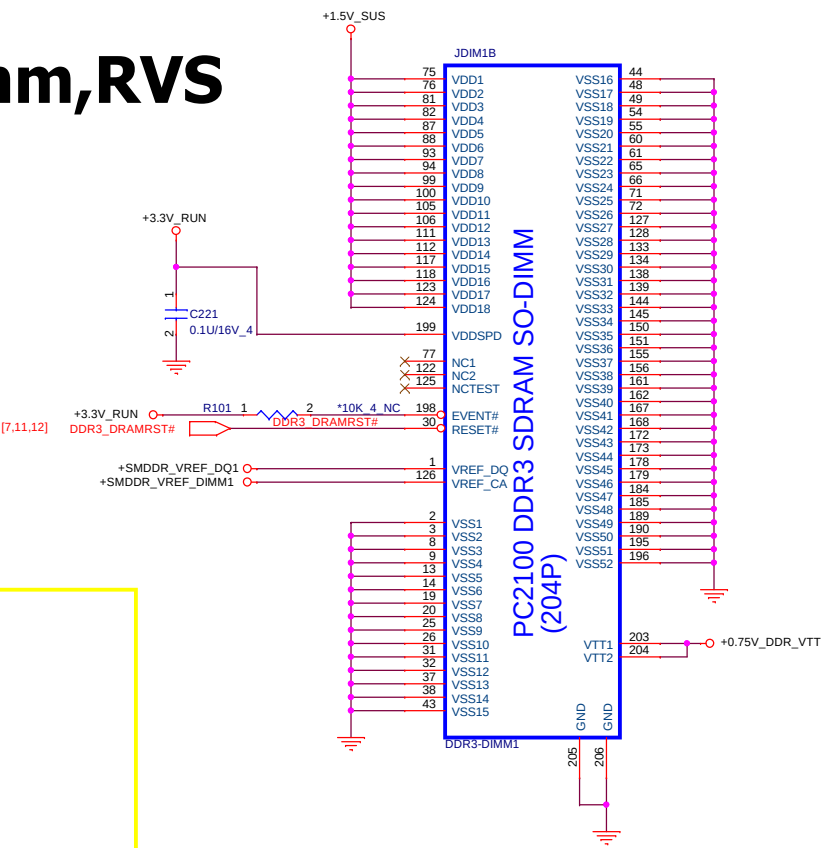
Size	Document Number	Rev
	DDR3 (A) On Board_B,1Rank	3A

Date: Tuesday, February 26, 2013 Sheet 12 of 54

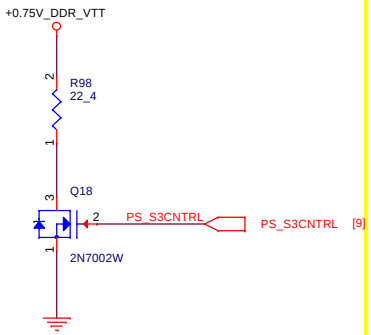
H=4mm,RVS



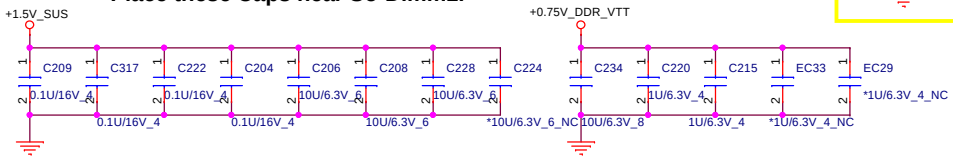
SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34



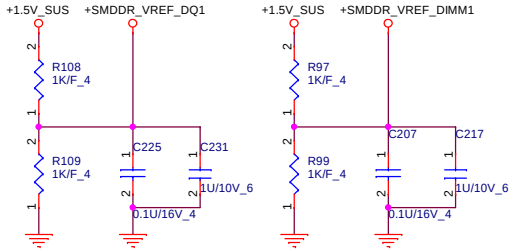
S3 Power reduce



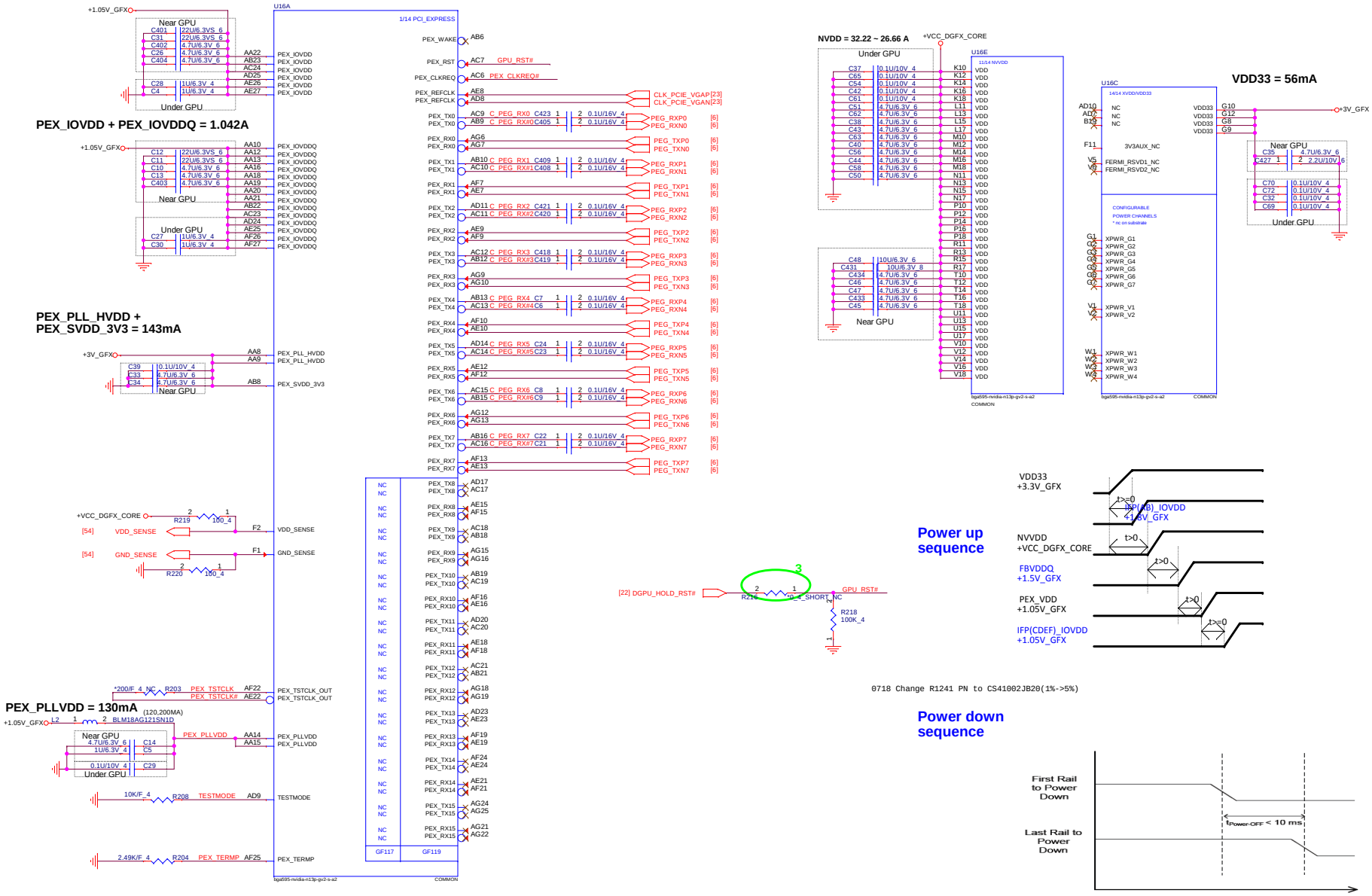
Place these Caps near So-Dimm1.

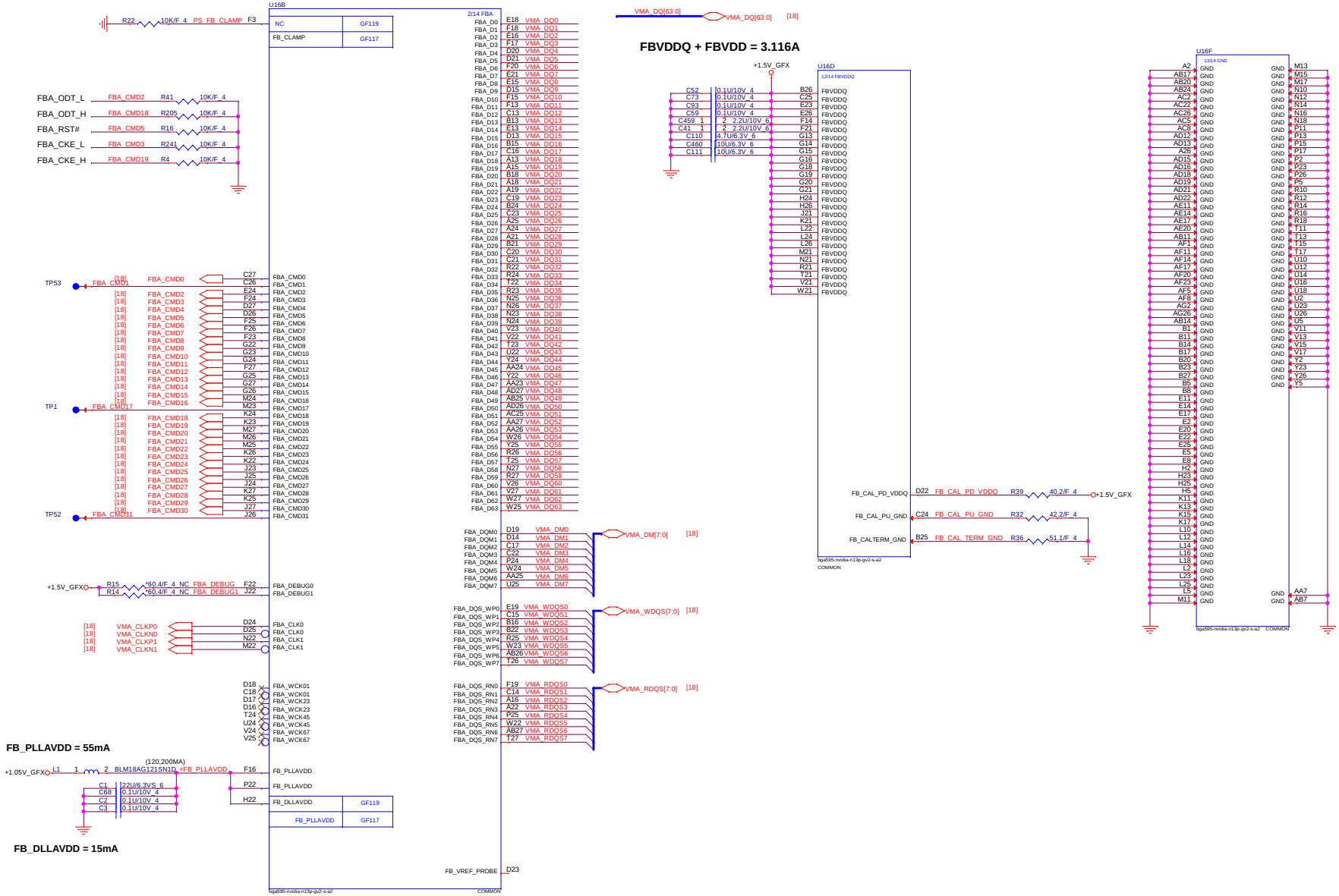


M1 VREF

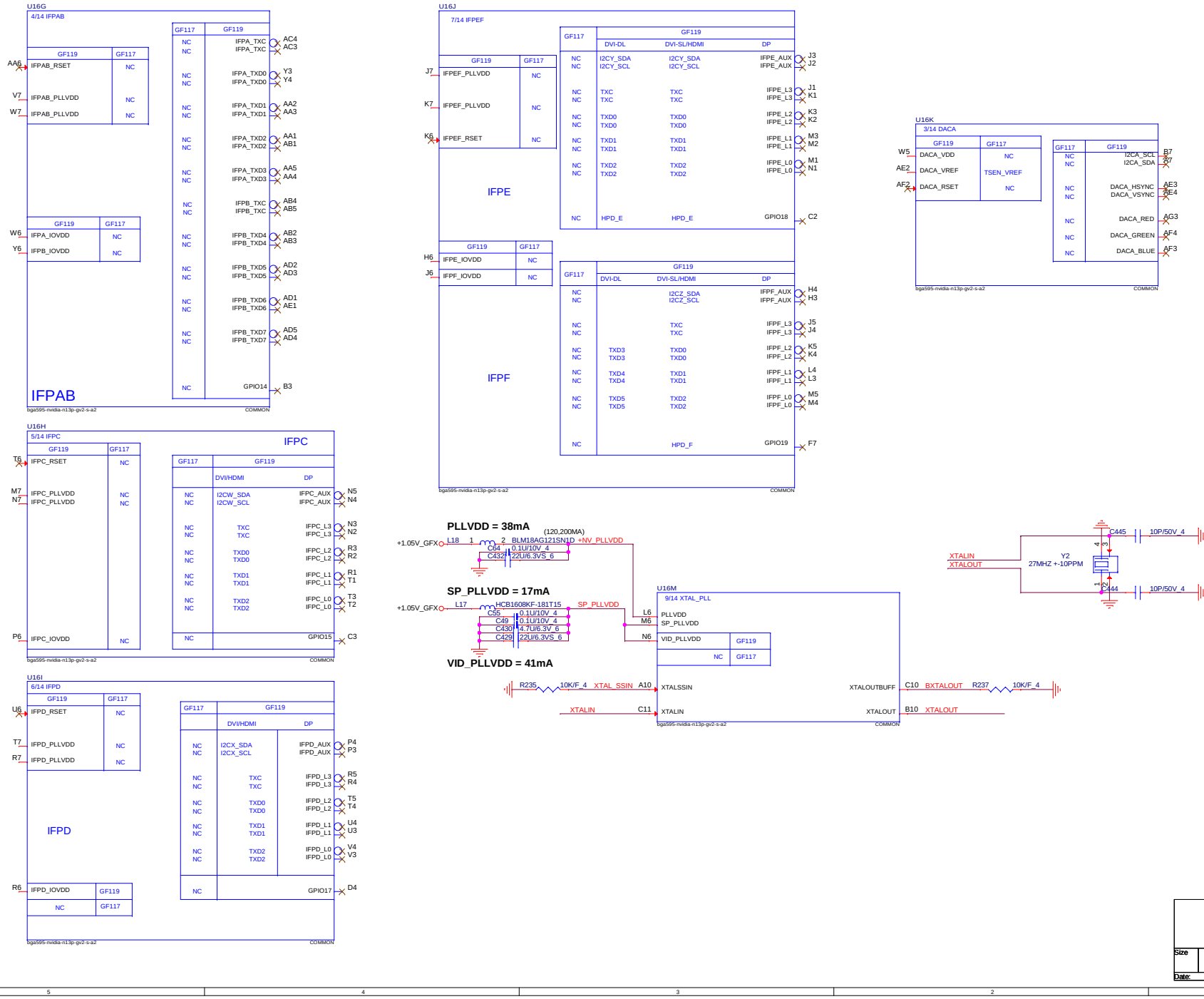


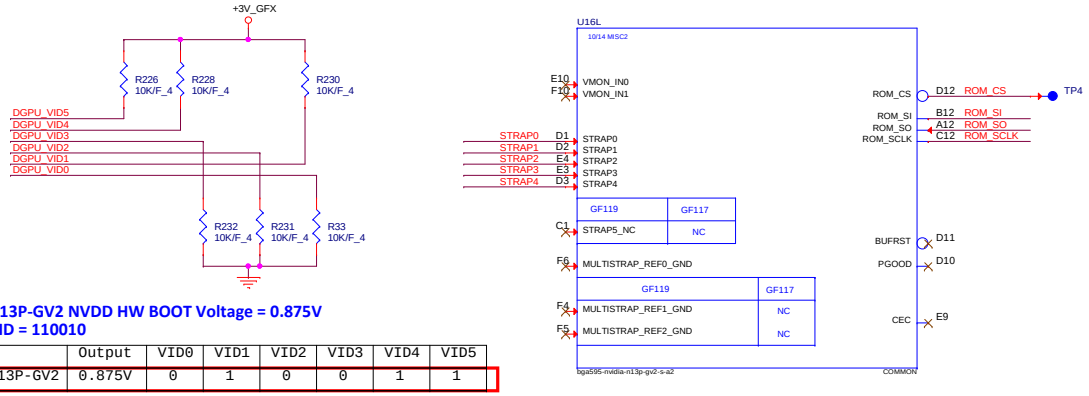
Quanta Computer Inc.		
PROJECT : JWA		
Size	Document Number: DDR3 DIMM-1	Rev: 3A
Date: Tuesday, February 26, 2013	Sheet 13 of 54	

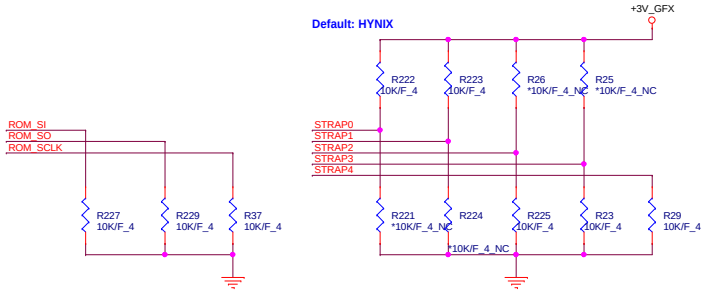

PEX_IOVDD + PEX_IOVDDQ = 1.042A
PEX_PLL_HVDD +
PEX_SVDD_3V3 = 143mA
PEX_PLLVDD = 130mA
(120,200MA)
NVDD = 32.22 ~ 26.66 A
VDD33 = 56mA
Power up sequence
Power down sequence
VDD33
+3.3V_GFX
NVVDD
+VCC_DGFX_CORE
FBVDDQ
+1.5V_GFX
PEX_VDD
+1.05V_GFX
IFP(AB)_IOVDD
+1.05V_GFX
t>=0
t>0
First Rail to Power Down
Last Rail to Power Down
tPower-OFF < 10 ms
0718 Change R1241 PN to CS41002JB20(1%->5%)
PU in PCH
Quanta Computer Inc.
PROJECT : JWA
N13P-GV2 (PCIE I/F) /NVDD
Size
Document Number
Rev
3A
Date: Tuesday, February 26, 2013
Sheet 14 of 54



Quanta Computer Inc.		
PROJECT : JWA		
Size	Document Number: N13P-GV2 (MEMORY/GND)	Rev: 3A
Date: Tuesday, February 26, 2013	Sheet 15 of 54	


U16G
4/14 IFPAB
IFPAB
U16J
7/14 IFPEF
IFPE
IFPF
U16K
3/14 DACA
U16H
5/14 IFPC
IFPC
U16I
6/14 IFPD
IFPD
PLLVDD = 38mA
(120,200MA)
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA
U16M
9/14 XTAL_PLL
Y2
27MHZ +-10PPM
Quanta Computer Inc.
PROJECT : JWA
N13P-GV2 (DISPLAY)
Tuesday, February 26, 2013



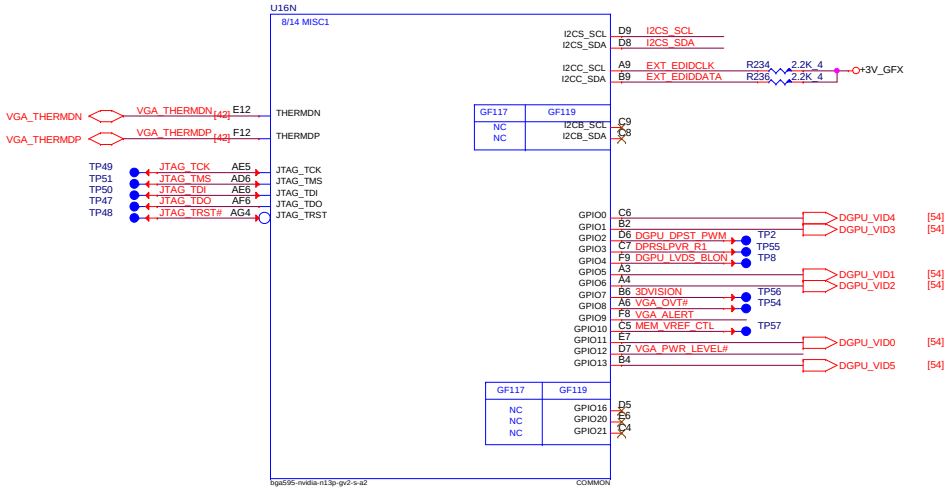


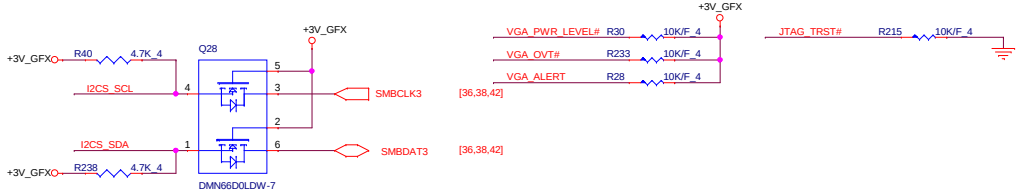
N13P-GV2 NVDD HW BOOT Voltage = 0.875V
VID = 110010

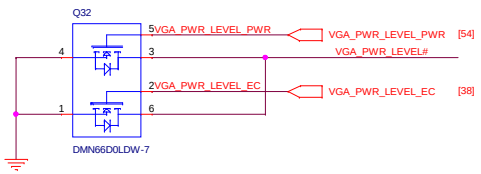
	Output	VID0	VID1	VID2	VID3	VID4	VID5
N13P-GV2	0.875V	0	1	0	0	1	1

Binary Strap Mode Mapping

Strap Pin name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10Kohm	Pull-down to GND
ROM_SI	SUB_VENDOR	10Kohm	Pull-UP to 3V3 if VBIOS ROM Exists Pull-down to GND if no VBIO ROM
ROM_SO	VGA_DEVICE	10Kohm	Pull-down to GND (no dispaly)
STRAP0	RAMCFG[0]	10Kohm	USER defined
STRAP1	RAMCFG1]	10Kohm	USER defined
STRAP2	RAMCFG[2]	10Kohm	USER defined
STRAP3	RAMCFG[3]	10Kohm	USER defined
STRAP4	PCIE_MAX_SPEED	10Kohm	Pull-down to GND







ROM_SI
VRAM Configuration Table

	RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N
	0000		Reserved		
2Gb	1100	IC SDRAM(96P)H5TQ2G63DFR-11C(FBGA)	HYNIX	H5TQ2G63DFR-11C	AKD5MGWTW16
2Gb	1011	IC SDRAM(96P)K4W2G1646E-BC11(FBGA)	SAMSUNG	K4W2G1646E-BC11	AKD5MGGT520
4Gb	0011	IC SDRAM(96P)H5TQ4G63MFR-11C(FBGA)	HYNIX	H5TQ4G63MFR-11C	AKD5PGWTW04
4Gb	0001	IC SDRAM(96P)K4W4G1646B-HC11(FBGA)	SAMSUNG	K4W4G1646B-HC11	AKD5MGWT516
4Gb	0101	IC SDRAM(96P) MT41K256M16HA-107G:E(FBGA)	Micron	MT41K256M16HA-107G	AKD5PGSTL00

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

Quanta Computer Inc.
PROJECT : JWA

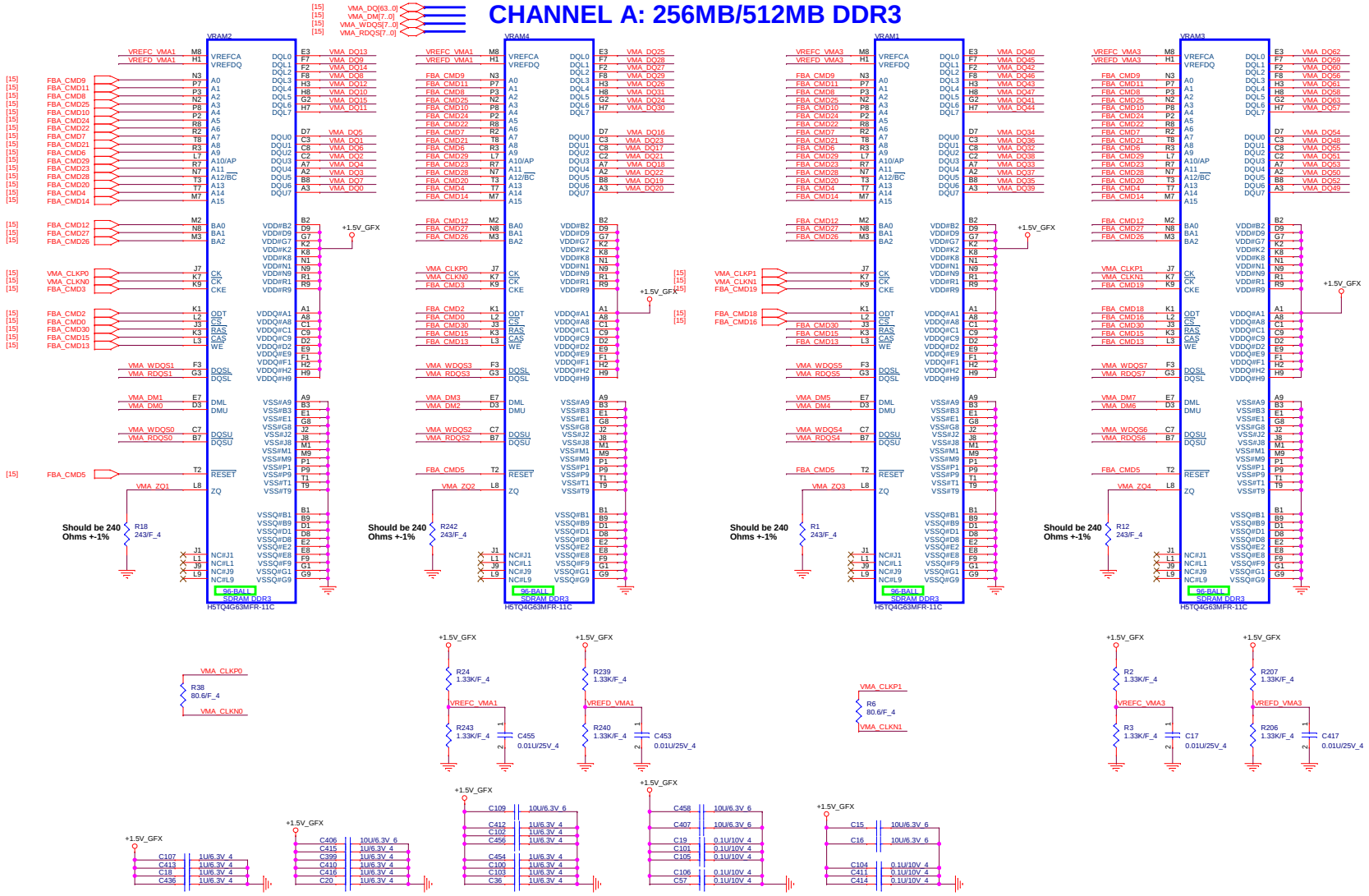
Size	Document Number	Rev
	N13P-GV2 (GPIO/STRAPS)	3A

Date: Tuesday, February 26, 2013 Sheet 17 of 54

900MHz VRAM size:

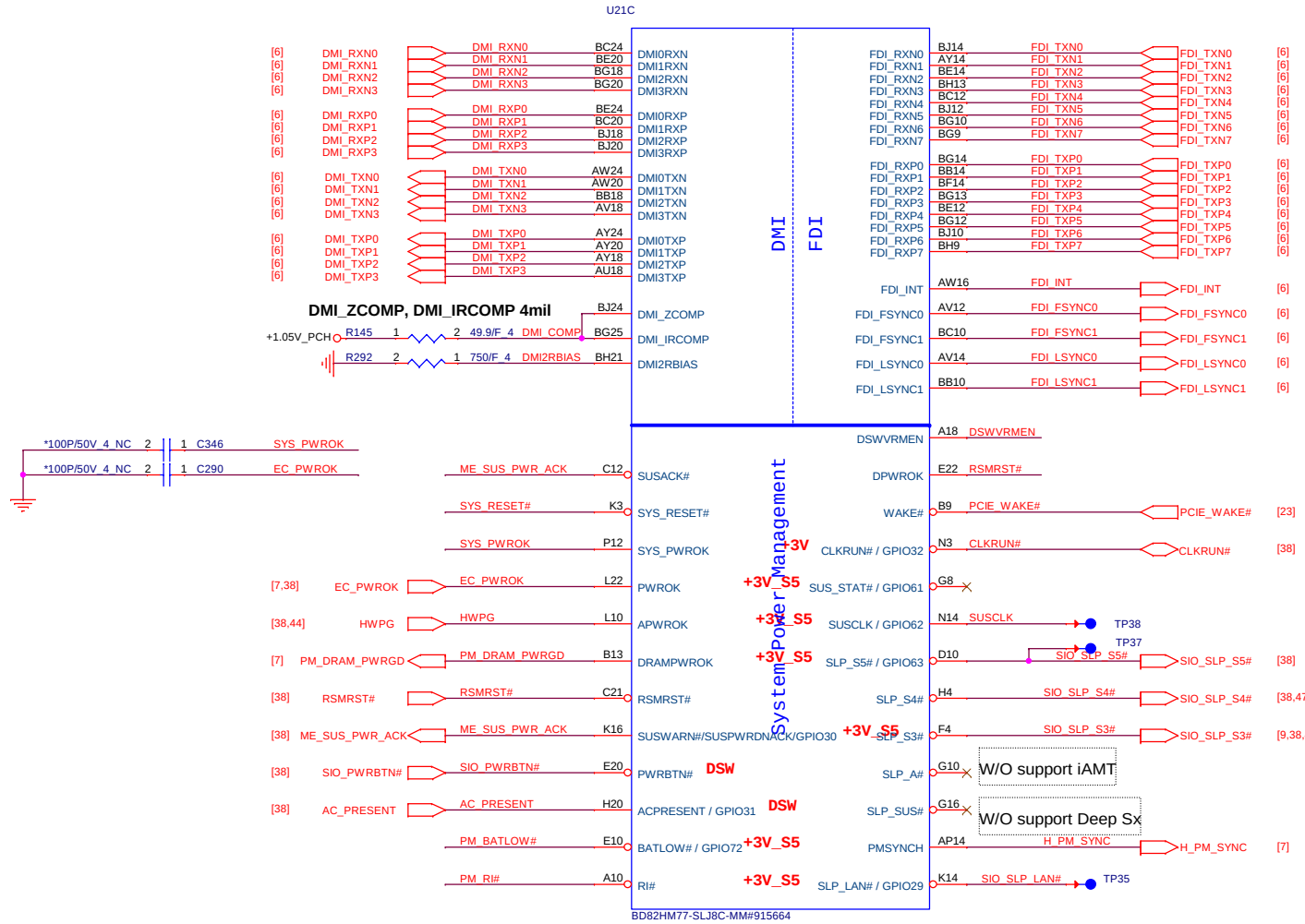
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT516
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5PGWTW04

CHANNEL A: 256MB/512MB DDR3

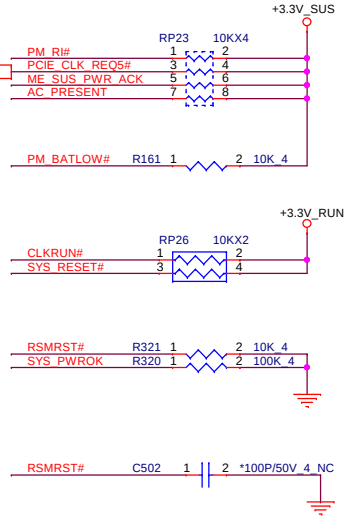


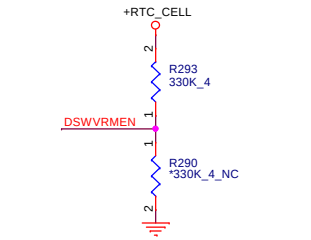
Quanta Computer Inc.			
PROJECT : JWA			
Size	Document Number		Rev
	N13P-GV2 DDR3 VRAM		3A
Date: Tuesday, February 26, 2013	Sheet 18	of 54	

Cougar Point/Panther Point (DMI,FDI,PM)

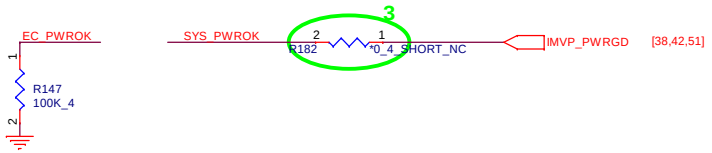


PCH Pull-high/low(CLG)



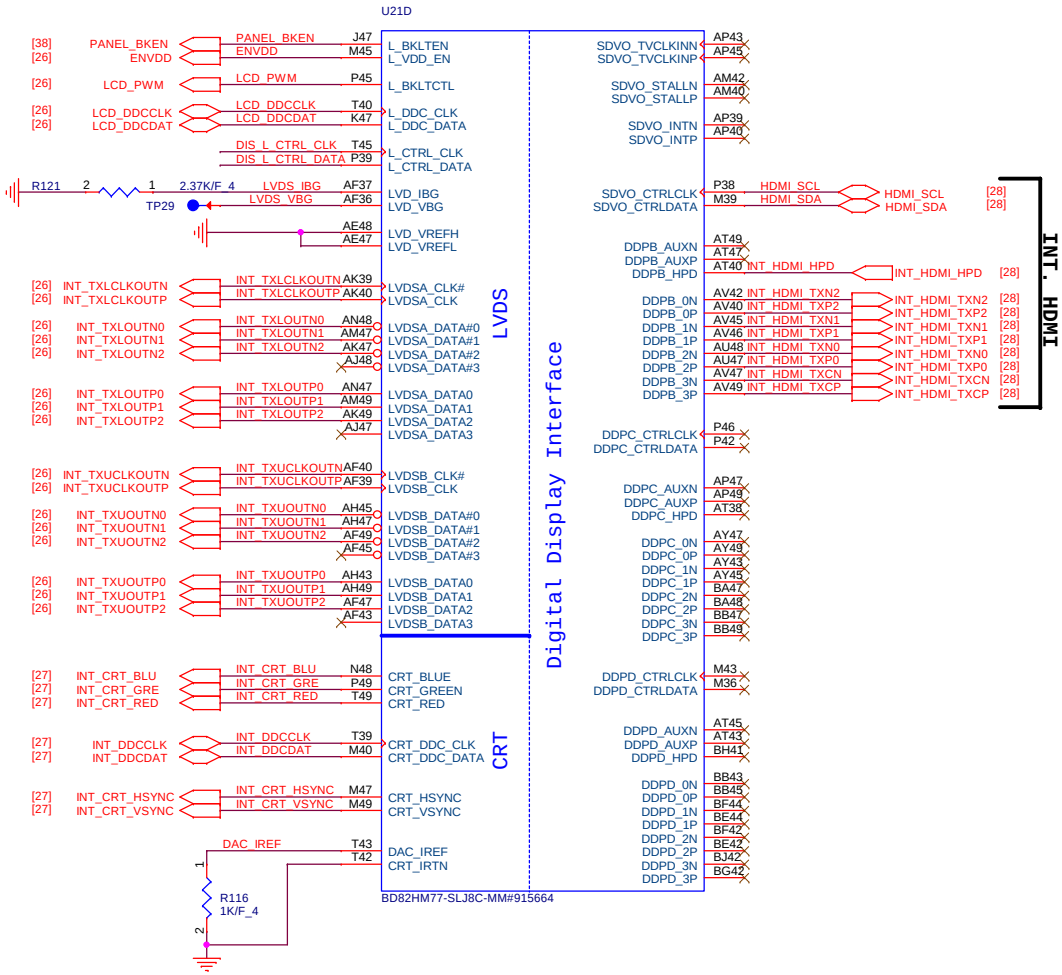


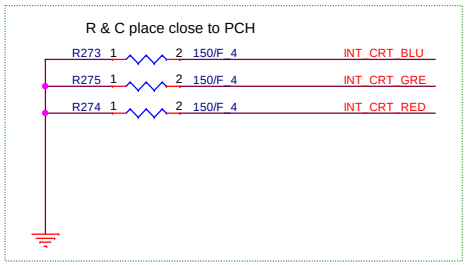
On Die DSW VR Enable
High = Enable (Default)
Low = Disable

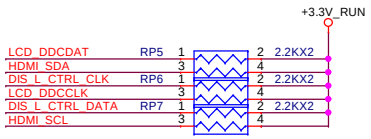


Quanta Computer Inc.		
PROJECT : JWA		
Size	Document Number: Panther Point 1/7	Rev: 3A
Date: Tuesday, February 26, 2013	Sheet 19 of 54	

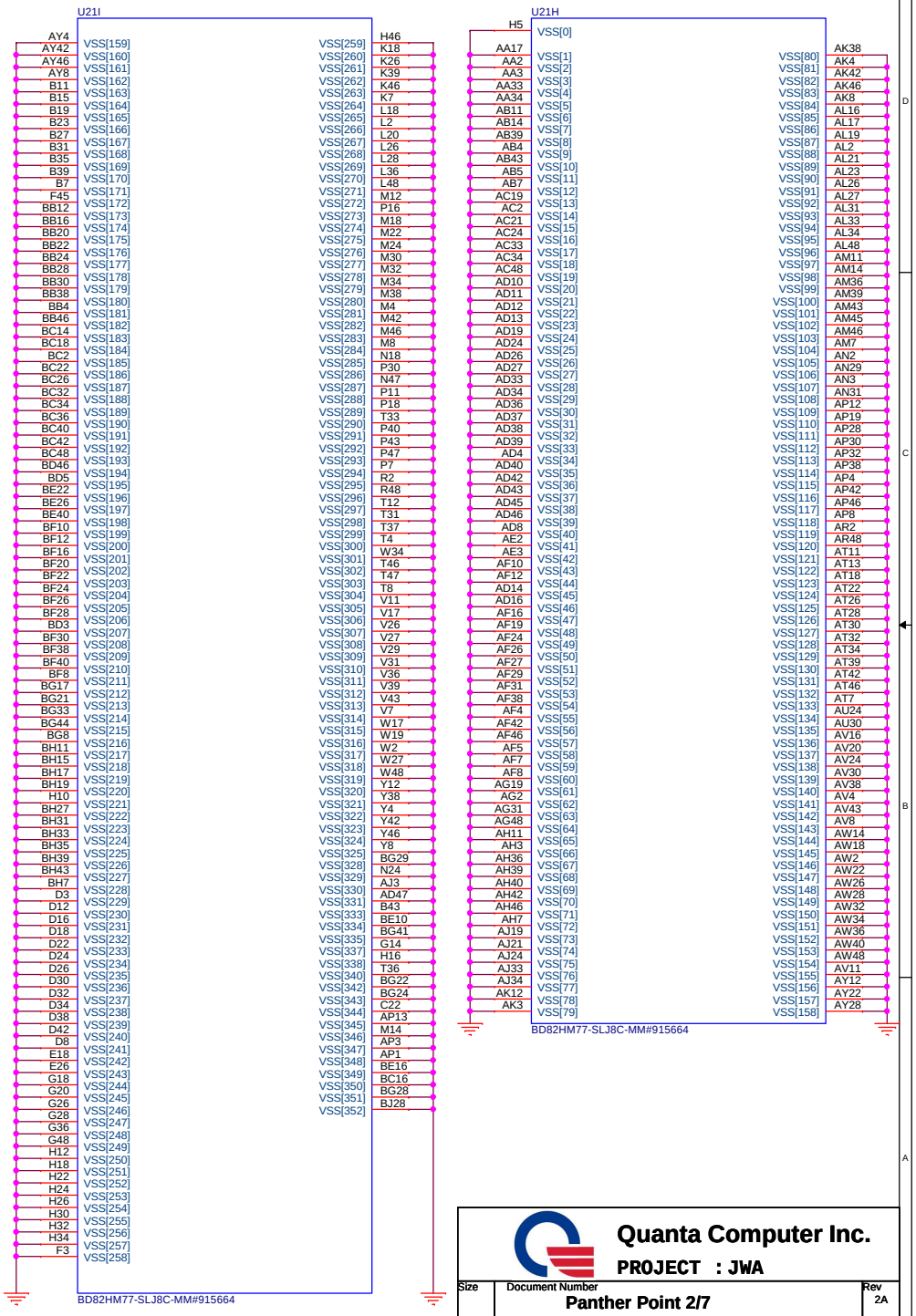
Cougar Point/Panther Point (LVDS,DDI)





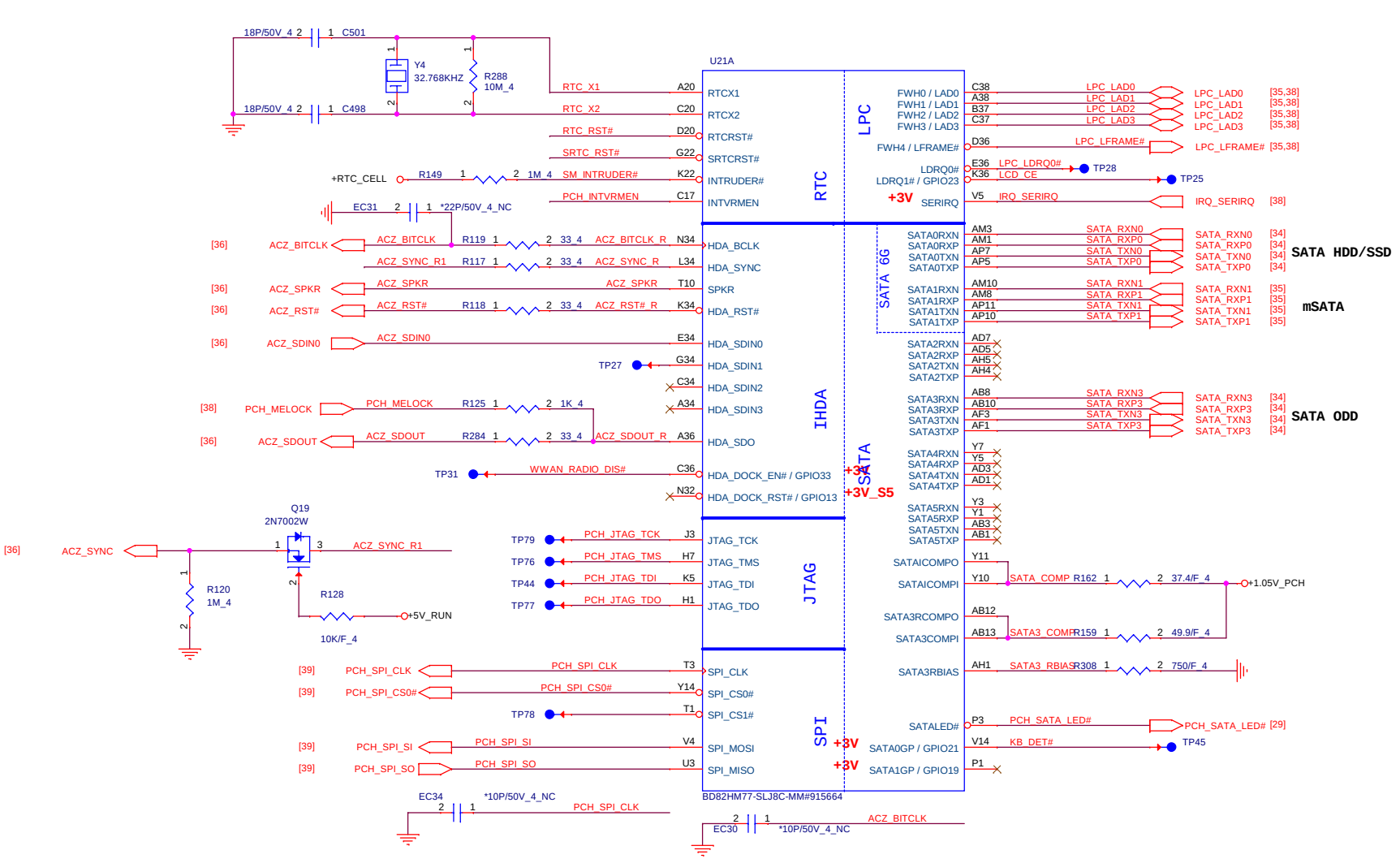


Cougar Point/Panther Point (GND)



Quanta Computer Inc.	
PROJECT : JWA	
Size	Document Number: Panther Point 2/7 — Rev: 2A
Date: Tuesday, February 26, 2013	Sheet 20 of 54

Cougar Point/Panther Point (HDA,JTAG,SATA)



PCH Strap Table

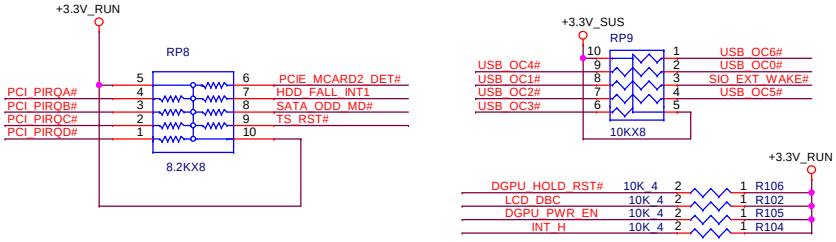
Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+RTC_CELL R294 330K_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R115 1K_4 ACZ_SYNC_R

Quanta Computer Inc.
PROJECT : JWA

Size	Document Number	Rev
	Panther Point 3/7	3A

Date: Tuesday, February 26, 2013 Sheet 21 of 54

Cougar Point-M/Panther Point (PCI,USB,NVRAM)

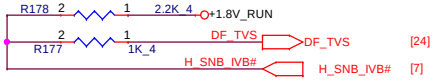


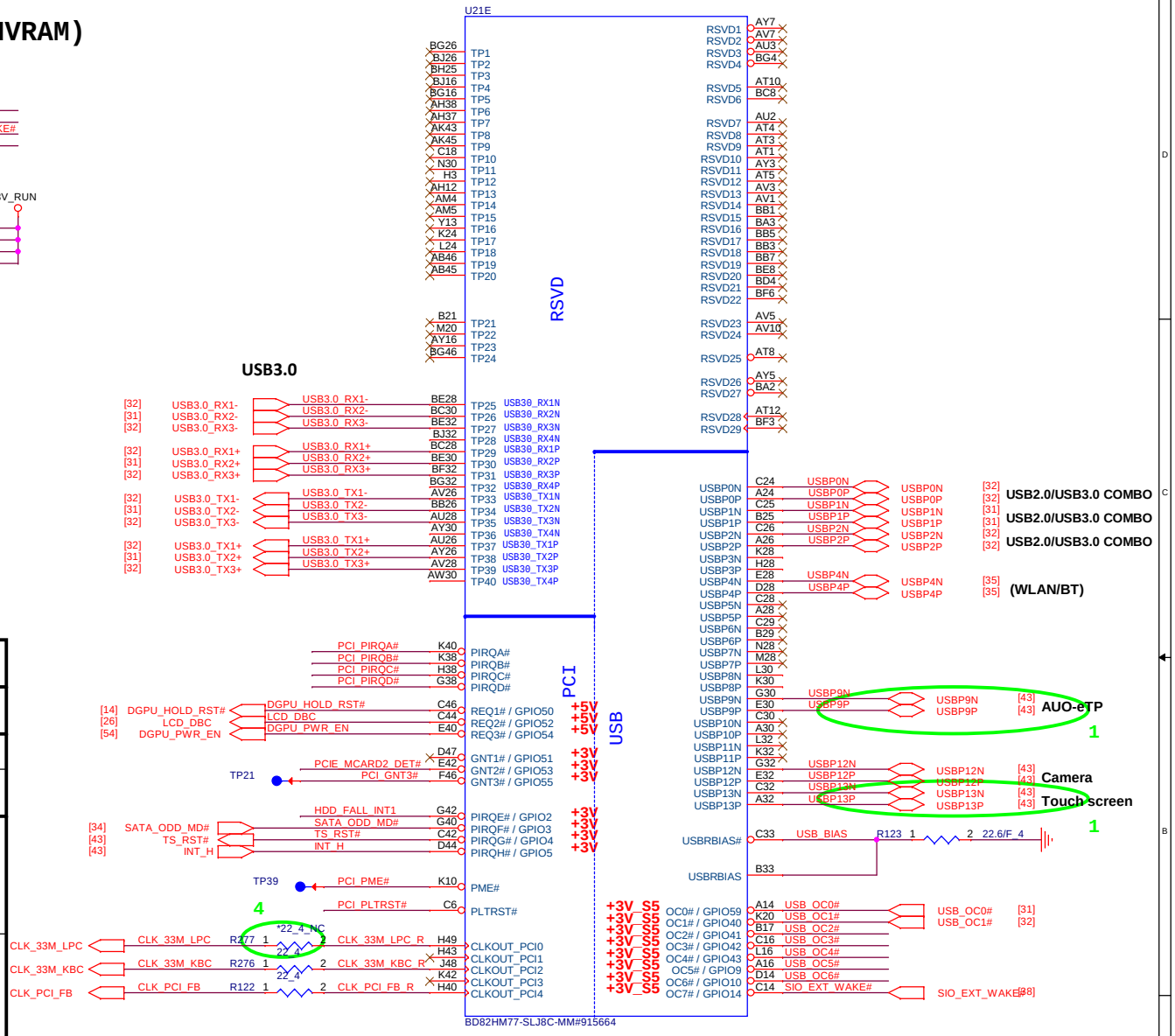
Pin Name	Strap description	Sampled	Configuration
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	

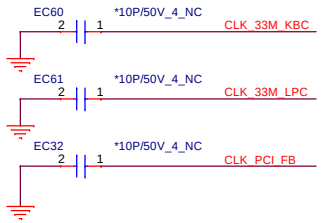
Bit 0	Bit 1	Boot Location
1	1	**SPI** *
0	0	LPC

Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] [35] [38] [23]

DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm



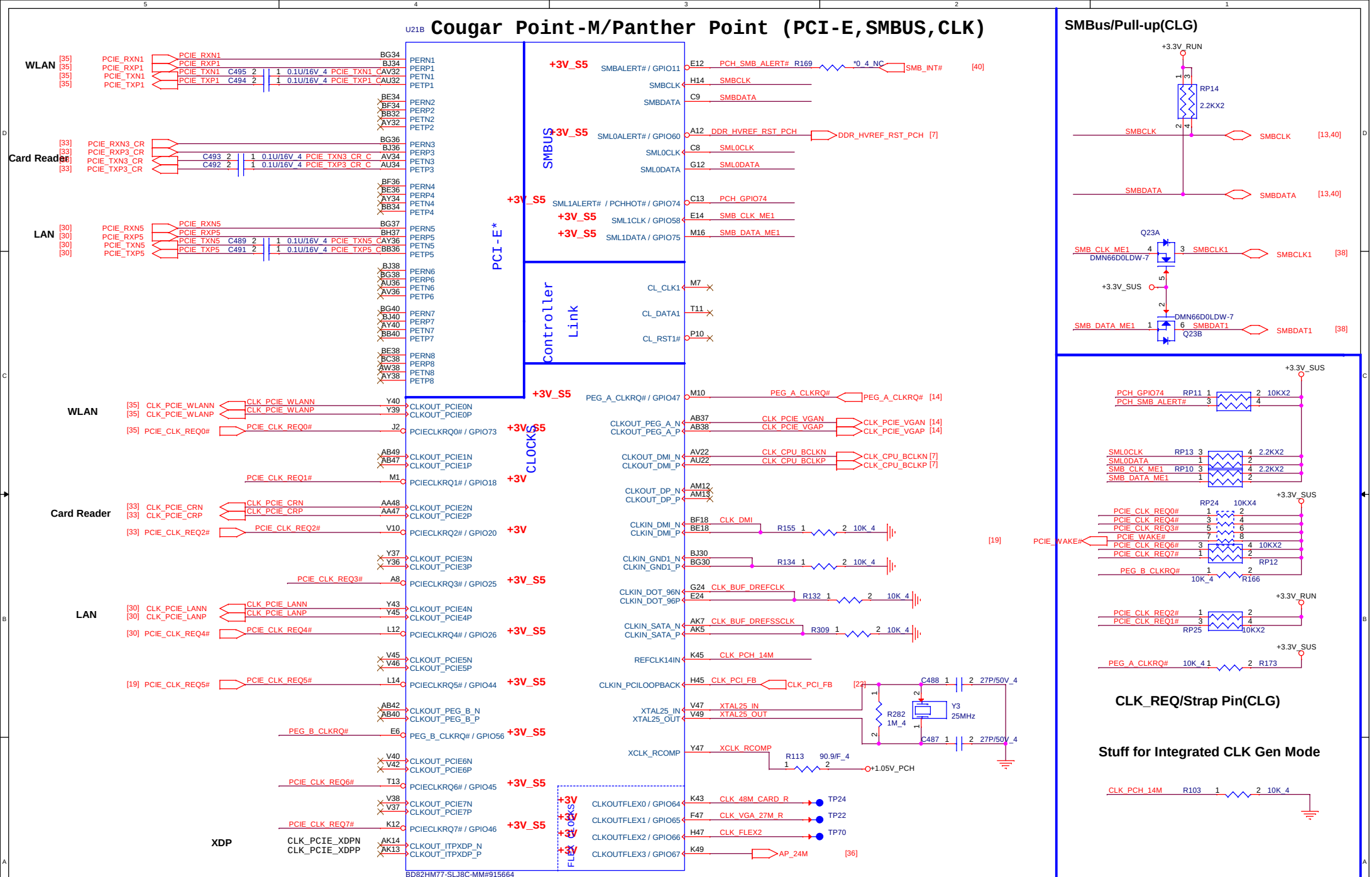




Quanta Computer Inc.
PROJECT : JWA

Size	Document Number	Rev
	Panther Point 4/7	3A
Date: Tuesday, February 26, 2013	Sheet 22 of 54	

U21B Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 /GPIO64	• 33 /27 /48/ 14.318 MHz / DC Output logic ‘0’
CLKOUTFLEX1 /GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX2 /GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic ‘0’
CLKOUTFLEX3 /GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

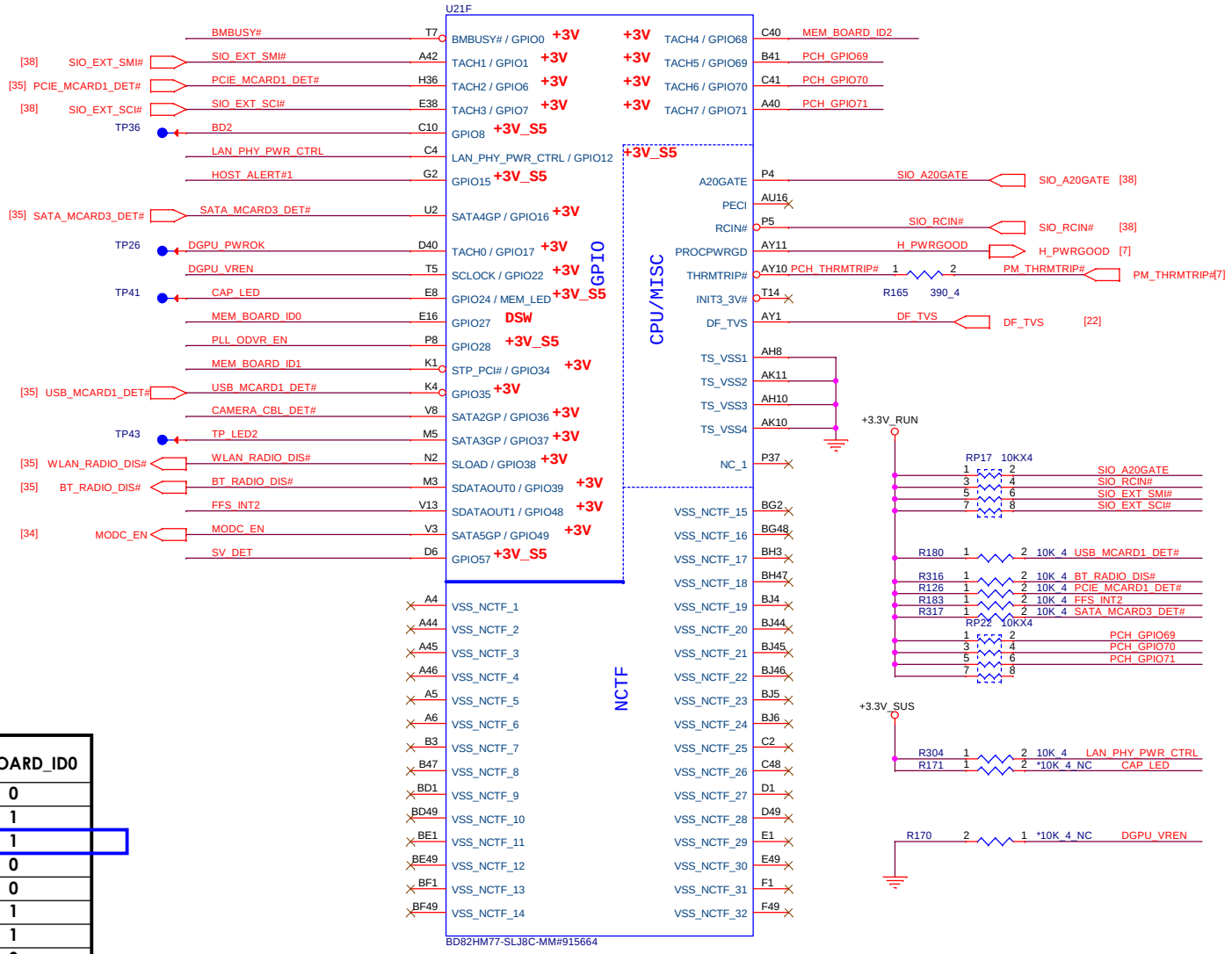
Stuff for Integrated CLK Gen Mode

Quanta Computer Inc.

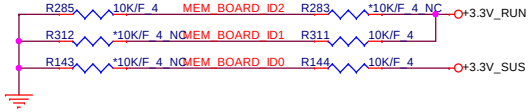
PROJECT : JWA

Size	Document Number	Rev
	Panther Point 5/7	3A
Date: Tuesday, February 26, 2013	Sheet 23 of 54	

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



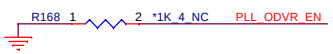
Default: On Board DDR3

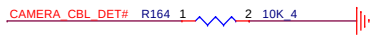


System Memory BOARD ID SETTING

	GPIO68 MEM_BOARD_ID2	GPIO35 MEM_BOARD_ID1	GPIO27 MEM_BOARD_ID0
HYNIX DDR3-1600 2GB	0	0	0
SAMSUNG DDR3-1600 2GB	0	0	1
On Board DDR3 N.C	0	1	1
RESERVE	0	1	0
RESERVE	1	0	0
RESERVE	1	0	1
RESERVE	1	1	1
RESERVE	1	1	0

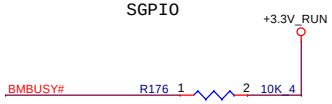
Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)





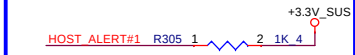
DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

SGPIO

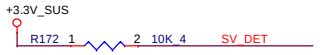


BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

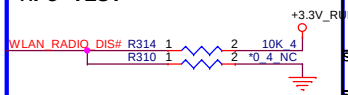
BMBUSY#:
If not used, require a weak pull-up
(8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and
100 ohm on this net for validation purpose.



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable



MFG-TEST

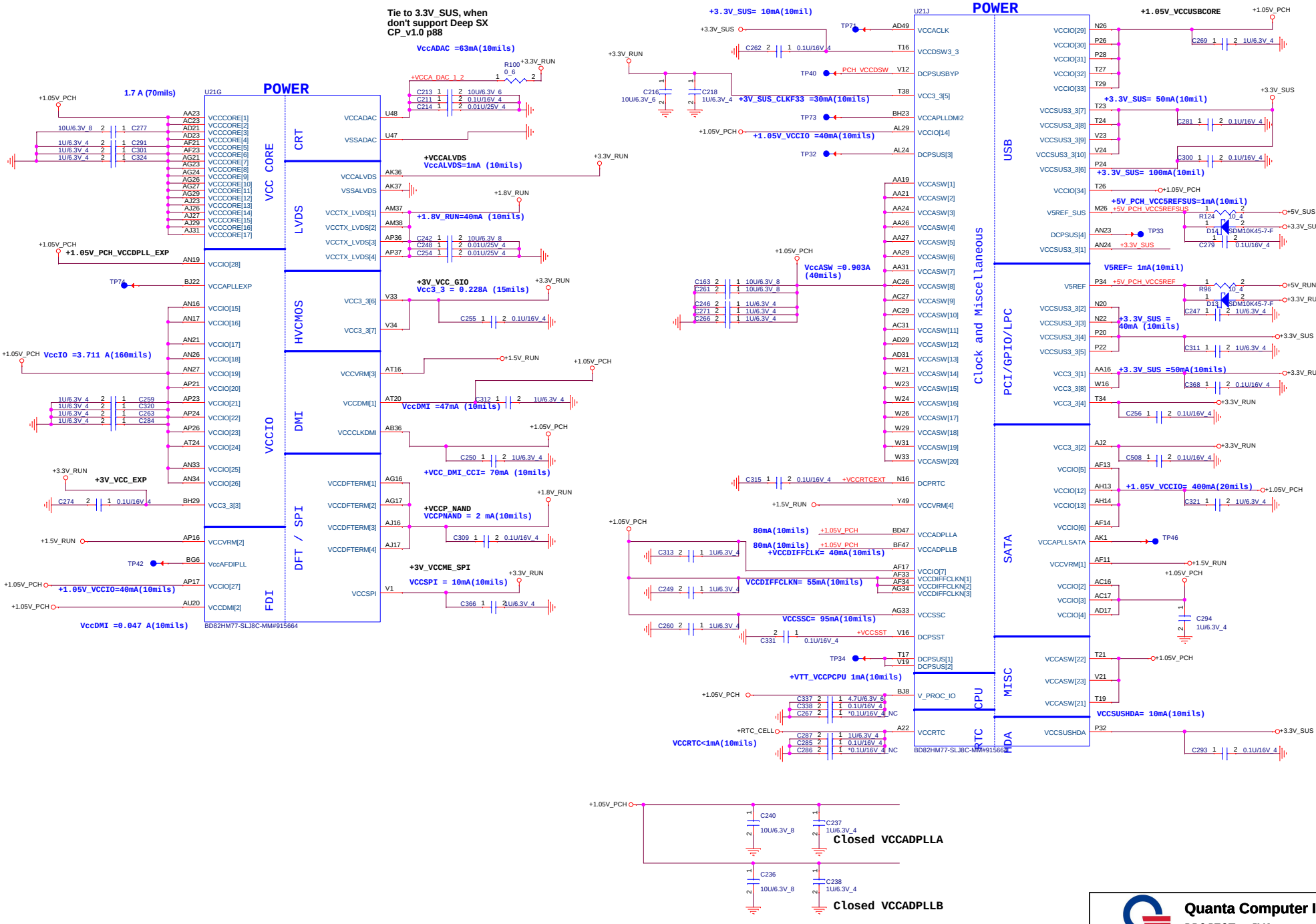


Quanta Computer Inc.
PROJECT : JWA

Size	Document Number	Rev
	Panther Point 6/7	3A
Date: Tuesday, February 26, 2013	Sheet 24 of 54	

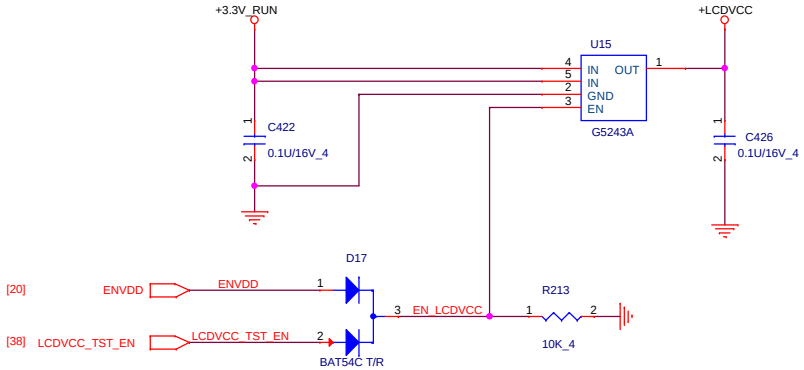
Cougar Point/Panther Point (POWER)

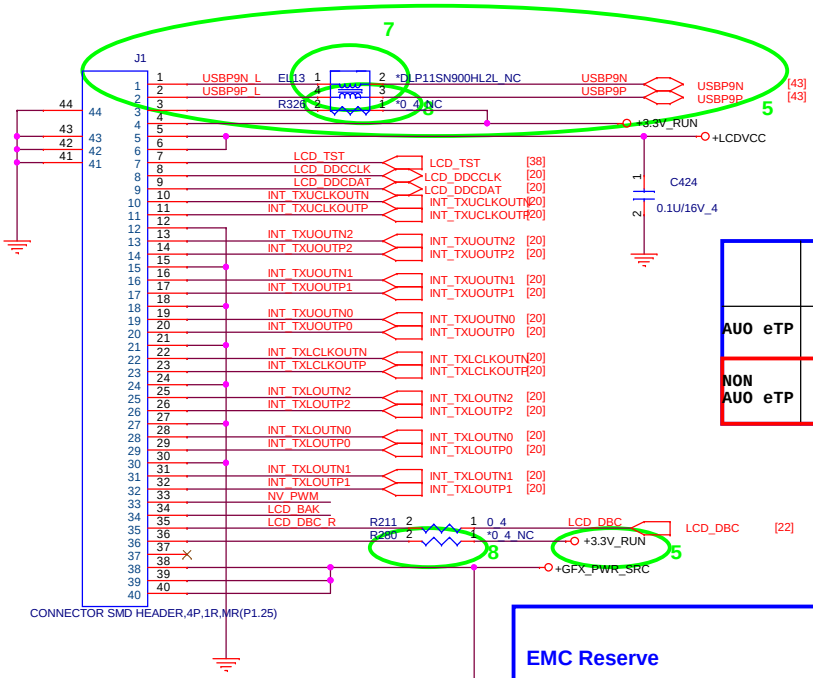
Cougar Point/Panther Point (POWER)



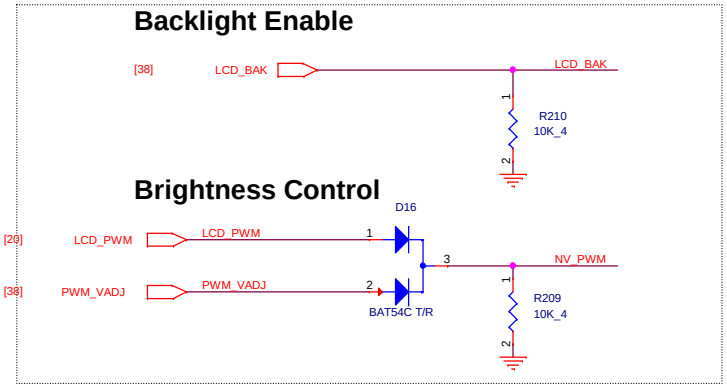
Quanta Computer Inc.			
PROJECT : JWA			
Size	Document Number		Rev
	Panther Point 7/7		3A
Date: Tuesday, February 26, 2013		Sheet 25 of 54	

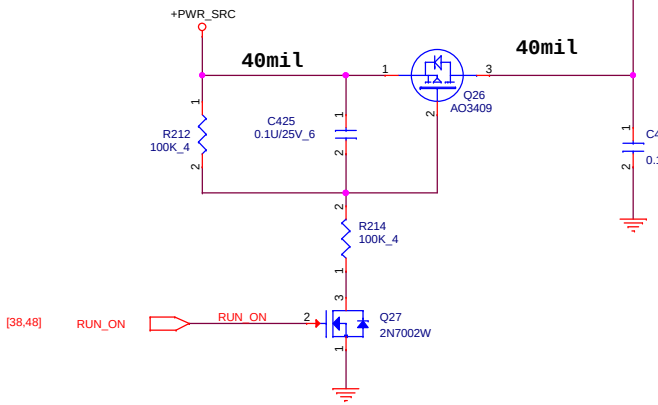
Follow PDC LVDS pin define & LVDS connector P/N.

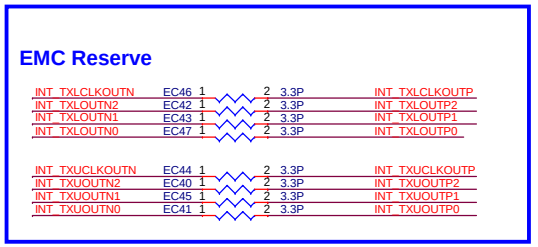


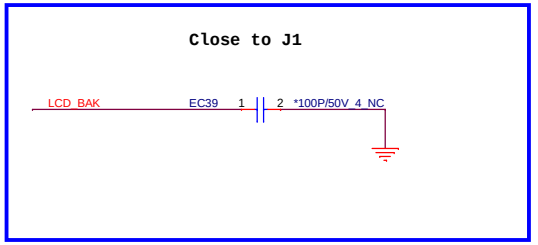


	EL13	R326	R280
AUO eTP	0	0	0
NON AUO eTP	X	X	X





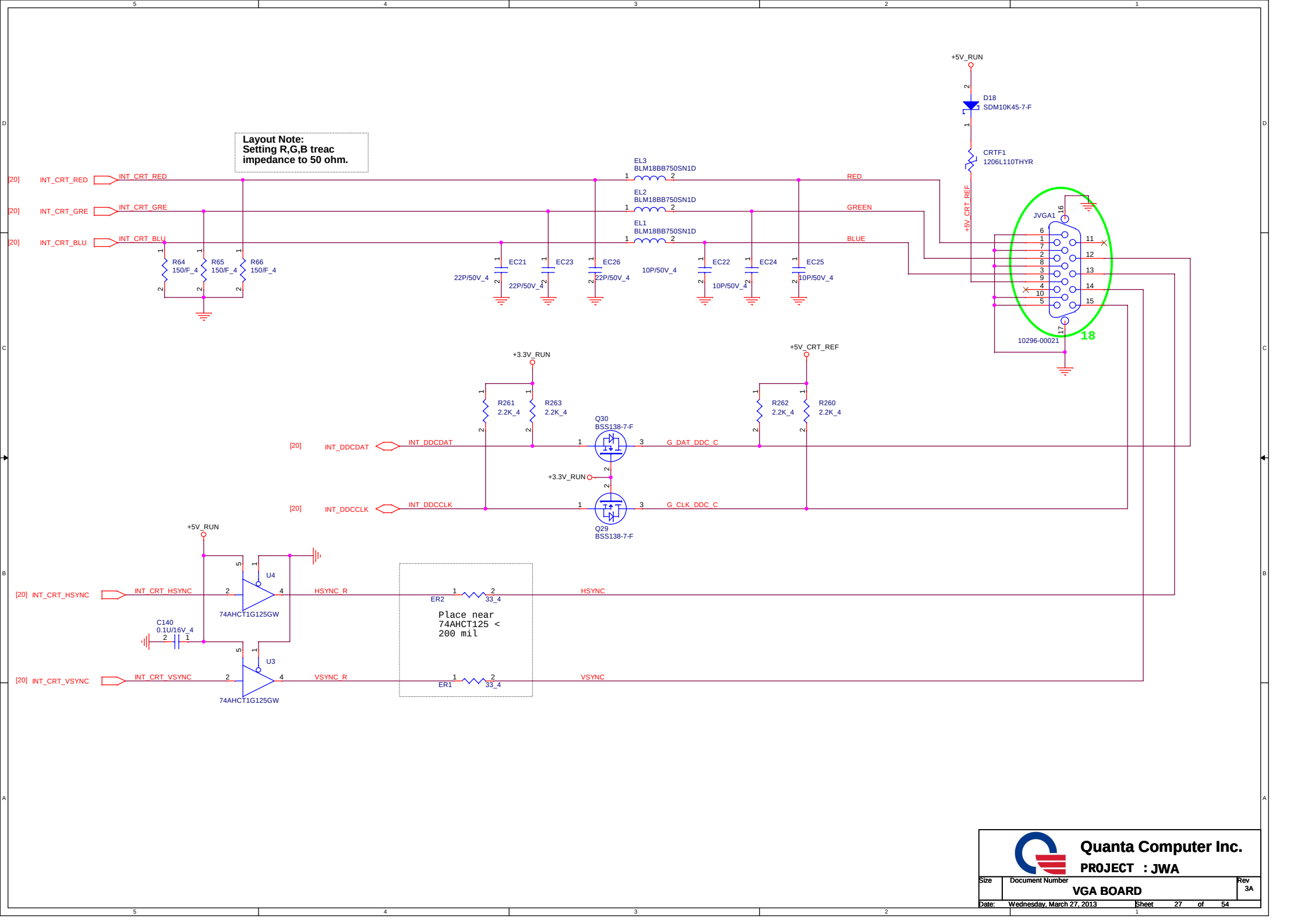




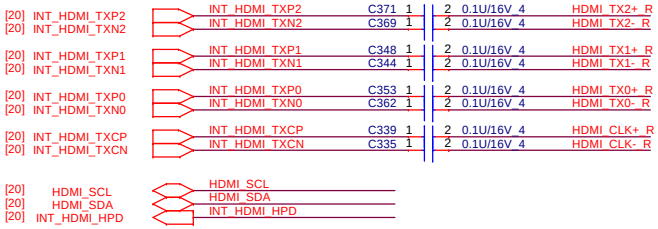
Quanta Computer Inc.
PROJECT : JWA

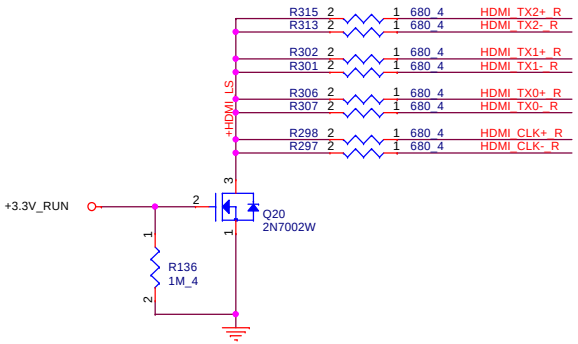
Size	Document Number	Rev
	LVDS CONN	2A

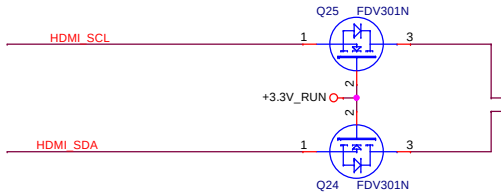
Date: Tuesday, March 05, 2013 Sheet 26 of 54

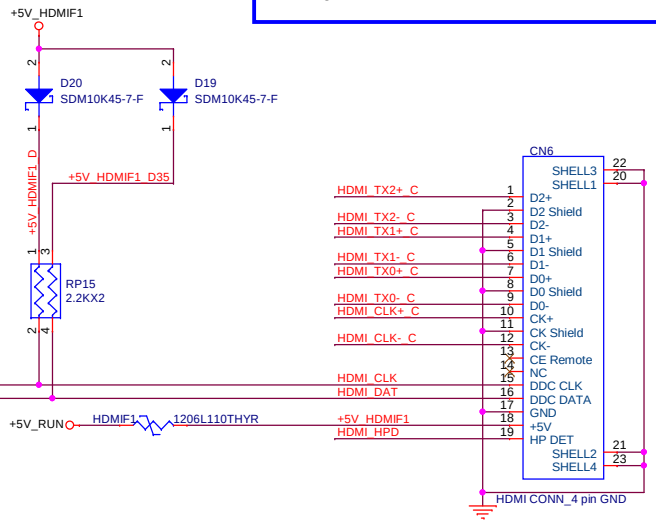

Layout Note:
Setting R,G,B treac
impedance to 50 ohm.
[20] INT_CRT_RED
[20] INT_CRT_GRE
[20] INT_CRT_BLU
INT_CRT_RED
INT_CRT_GRE
INT_CRT_BLU
R64 150/F_4
R65 150/F_4
R66 150/F_4
EL3 BLM18BB750SN1D
EL2 BLM18BB750SN1D
EL1 BLM18BB750SN1D
EC21 22P/50V_4
EC23 22P/50V_4
EC26 22P/50V_4
EC22 10P/50V_4
EC24 10P/50V_4
EC25 10P/50V_4
RED
GREEN
BLUE
+5V_RUN
D18 SDM10K45-7-F
CRTF1 1206L110THYR
+5V CRT REF
JVGA1
10296-00021
18
+3.3V_RUN
+5V_CRT_REF
R261 2.2K_4
R263 2.2K_4
R262 2.2K_4
R260 2.2K_4
Q30 BSS138-7-F
Q29 BSS138-7-F
[20] INT_DDCDAT
[20] INT_DDCCLK
INT_DDCDAT
INT_DDCCLK
G_DAT_DDC_C
G_CLK_DDC_C
+5V_RUN
U4
U3
74AHCT1G125GW
74AHCT1G125GW
C140 0.1U/16V_4
[20] INT_CRT_HSYNC
[20] INT_CRT_VSYNC
INT_CRT_HSYNC
INT_CRT_VSYNC
HSYNC_R
VSYNC_R
ER2 33_4
ER1 33_4
HSYNC
VSYNC
Place near
74AHCT125 <
200 mil
Quanta Computer Inc.
PROJECT : JWA
Size
Document Number
VGA BOARD
Rev
3A
Date: Wednesday, March 27, 2013
Sheet 27 of 54

HDMI

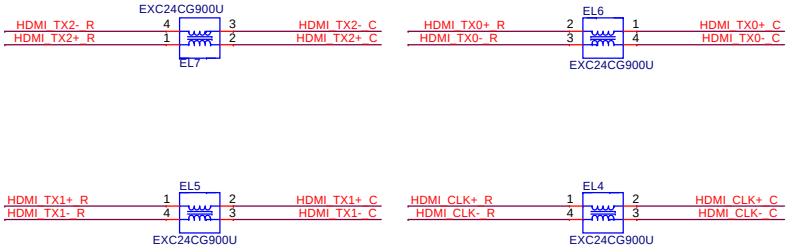






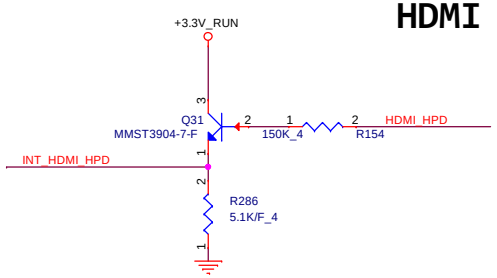


Reserve for EMI and close to HDMI CONN



HDMI_HPD spec VinH_min=2.0V

HDMI HPD

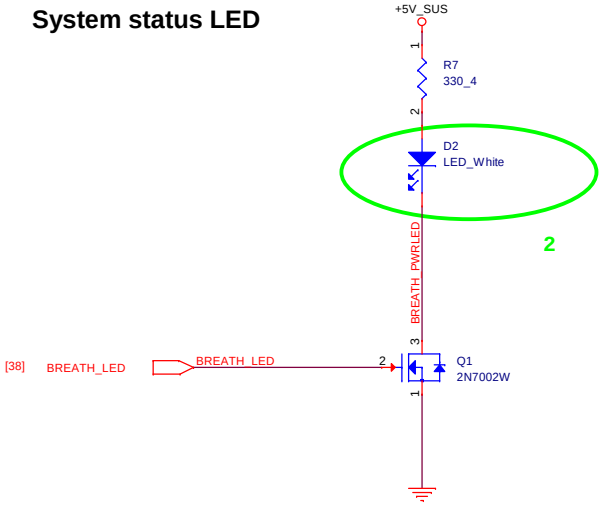


IB=(5V-0.7V)/(150K+(70+1)5.1K)=8.4uA
IE=(1+70)X8.4uA=596.4uA
VE=596.4uA X 5.1K=3.04V
B=70

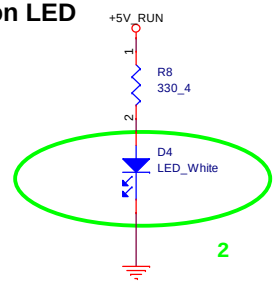
HDMI Conn.

Quanta Computer Inc.		
PROJECT : JWA		
Size	Document Number: HDMI CONN	Rev: 3A
Date: Tuesday, February 26, 2013	Sheet 28 of 54	

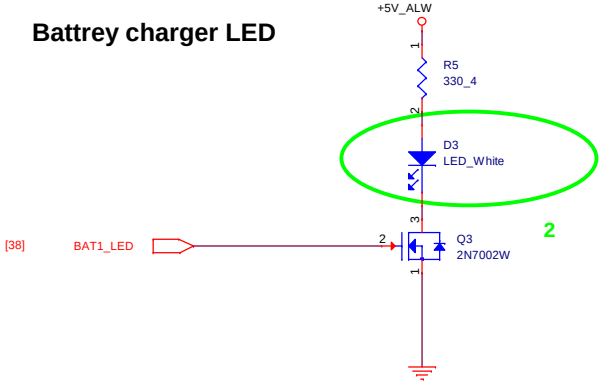
System status LED



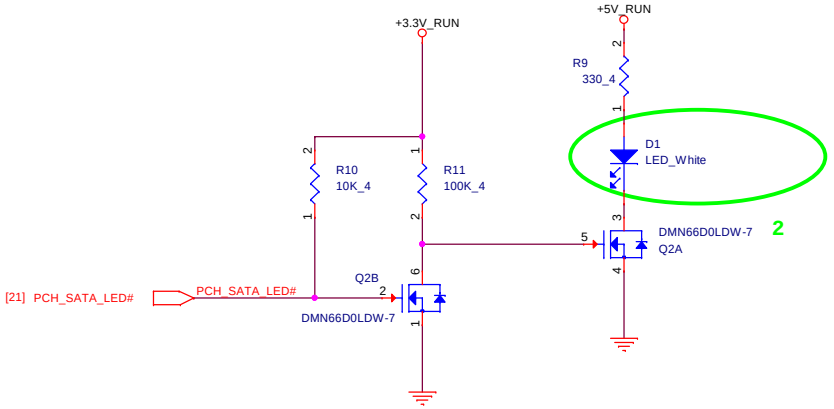
Power Button LED



Battrey charger LED



HDD access LED



Quanta Computer Inc.		
PROJECT : JWA		
Size	Document Number: LED	Rev: 3A
Date: Tuesday, February 26, 2013	Sheet 29 of 54	

These Caps close to LAN Chip VDD33 pins

+3.3V_ALW

+3.3V_LAN wider>30mil

C449 10U/6.3V/X5R_8
C470 1U/6.3V/X5R_4
C441 0.1U/16V_4
C442 1000P/50V/X7R_4

Close to Pin6

+1.1V_AVDD
C443 1U/6.3V/X5R_4
C446 0.1U/16V_4

Close to Pin9

+2.7V_AVDD
C447 1U/6.3V/X5R_4
C448 0.1U/16V_4

Close to Pin37

+1.1V_DVDD
C81 1U/6.3V/X5R_4
C78 0.1U/16V_4

U1

Atheros
AR8161
AR8162

AR8161-BL3A-R

[23] PCIE_RXN5 — C85 0.1U/16V_4 — PCIE_RXN5_C — 29 TX_N
[23] PCIE_RXP5 — C84 0.1U/16V_4 — PCIE_RXP5_C — 30 TX_P
[23] PCIE_TXN5 — 36 RX_N
[23] PCIE_TXP5 — 35 RX_P

[23] CLK_PCIE_LANN — 32 REFCLKN
[23] CLK_PCIE_LANP — 33 REFCLKP

TP5 LAN_SMBDAT — 26 SMDATA
TP6 LAN_SMBCLK — 25 SMCLK

[7,22,33,35,38] PLTRST# — 2 PERSTn
[38] PCIE_EC_WAKE# — 3 WAKEn
R31 2.37K/F_4 — 10 RBIAS
27 TESTMODE
28 TEST_RST

LAN_XTALI — 8 XTLI
LAN_XTALO — 7 XTLO
41 GND_PAD

24 DVDDL — PPS — TP7
37 DVDDL_REG — +1.1V_DVDD
+1.1V_DVDD wider>20mil
40 LX — LX
1 VDD33 — +3.3V_ALW
9 AVDDH_REG — +2.7V_AVDD
16 AVDDH
22 AVDDH — C90 0.1U/16V_4 — +3.3V_ALW — C92 0.1U/16V_4 — C89 *1U/6.3V/X5R_4_NC
+2.7V_AVDD wider>20mil
6 AVDDL_REG — +1.1V_AVDD
13 AVDDL — C97 0.1U/16V_4
19 AVDDL — C98 0.1U/16V_4
31 AVDDL — C80 0.1U/16V_4
34 AVDDL — AVDDVCO — C82 0.1U/16V_4
+1.1V_AVDD wider>20mil
4 VDDCT_REG/CLKREQn — PCIE_CLK_REQ4#
5 VDDCT/ISOLATn — +VDDCT R27 2 — 1 30K/F_4 — +3.3V_RUN
PCIE_CLK_REQ4#[23]

AVDDVCO — L4 HCB1608KF-181T15_6 — +1.1V_AVDD
C79 *1U/6.3V/X5R_4_NC
C71 *4.7U/6.3V_6_NC

21 TRXN[3] — NB_LOM_TRDN3
20 TRXP[3] — NB_LOM_TRDP3
18 TRXN[2] — NB_LOM_TRDN2
17 TRXP[2] — NB_LOM_TRDP2
15 TRXN[1] — NB_LOM_TRDN1
14 TRXP[1] — NB_LOM_TRDP1
12 TRXN[0] — NB_LOM_TRDN0
11 TRXP[0] — NB_LOM_TRDP0

38 LED0 — LED_ACT
39 LED1
23 CLKREQn/LED2

R19 *4.7K_4_NC
R20 2 — 1 *4.7K_4_NC — LED_ACT

Y1 25MHz
LAN_XTALI — C91 33P/50V/NPO_4
LAN_XTALO — C87 33P/50V/NPO_4

LED1 (Pin39)	Regulator select	
LDO	Low	
SWR*	High	SWR mode

L5 4.7uH/700mA_8
LX — +1.1V_DVDD
L3 HCB1608KF-181T15_6 — +1.1V_AVDD
C67 0.1U/16V_4
C66 10U/6.3V/X5R_6

	Core voltage select	
LED_ACT	High core voltage	Low core voltage
	1	0

RJ-45 Connector

R244 75/F_4 TXCT0
R245 75/F_4 TXCT1
R257 75/F_4 TXCT2
R258 75/F_4 TXCT3
EC50 4.7P/3KV/NPO_18

CN2
RJ45-TX3- 8 RX1-
RJ45-TX3+ 7 RX1+
RJ45-TX1- 6 RX0-
RJ45-TX2- 5 TX1-
RJ45-TX2+ 4 TX1+
RJ45-TX1+ 3 RX0+
RJ45-TX0- 2 TX0-
RJ45-TX0+ 1 TX0+
GND2 9
GND1 10
GND3 11
GND4 12
RJ45_CONN
DFTJ08FR322
rj45-jm361c-hp34aa03-9h-8p

EC18 *6.8P/50V/NPO_4_NC NB_LOM_TRDP0
EC17 *6.8P/50V/NPO_4_NC NB_LOM_TRDN0
EC16 *6.8P/50V/NPO_4_NC NB_LOM_TRDP1
EC15 *6.8P/50V/NPO_4_NC NB_LOM_TRDN1
EC14 *6.8P/50V/NPO_4_NC NB_LOM_TRDP2
EC13 *6.8P/50V/NPO_4_NC NB_LOM_TRDN2
EC12 *6.8P/50V/NPO_4_NC NB_LOM_TRDP3
EC10 *6.8P/50V/NPO_4_NC NB_LOM_TRDN3

Place ESD diodes as close as TRANSFORMER

ESD2 *SRV05-4.TCT_NC
NB_LOM_TRDP0 — NB_LOM_TRDP1
NB_LOM_TRDN0 — NB_LOM_TRDN1
+3.3V_ALW
C467 *0.1U/16V_4_NC

ESD1 *SRV05-4.TCT_NC
NB_LOM_TRDP2 — NB_LOM_TRDP3
NB_LOM_TRDN2 — NB_LOM_TRDN3
+3.3V_ALW
C462 *0.1U/16V_4_NC

L19 DTA_LFE9276C-R
C120 0.1U/16V_4
C134 0.1U/16V_4
C137 0.1U/16V_4
C113 0.1U/16V_4

1 TCT0 — NB_LOM_TRDP3
2 TD0+
3 TD0-
4 TCT1 — NB_LOM_TRDN3
5 TD1+ — NB_LOM_TRDP2
6 TD1- — NB_LOM_TRDN2
7 TCT2
8 TD2+ — NB_LOM_TRDP1
9 TD2- — NB_LOM_TRDN1
10 TCT3
11 TD3+ — NB_LOM_TRDP0
12 TD3- — NB_LOM_TRDN0

MCT0 — 24 TXCT0
TX0+ — 23 RJ45-TX3+
TX0- — 22 RJ45-TX3-
MCT1 — 21 TXCT1
TX1+ — 20 RJ45-TX2+
TX1- — 19 RJ45-TX2-
MCT2 — 18 TXCT2
TX2+ — 17 RJ45-TX1+
TX2- — 16 RJ45-TX1-
MCT3 — 15 TXCT3
TX3+ — 14 RJ45-TX0+
TX3- — 13 RJ45-TX0-

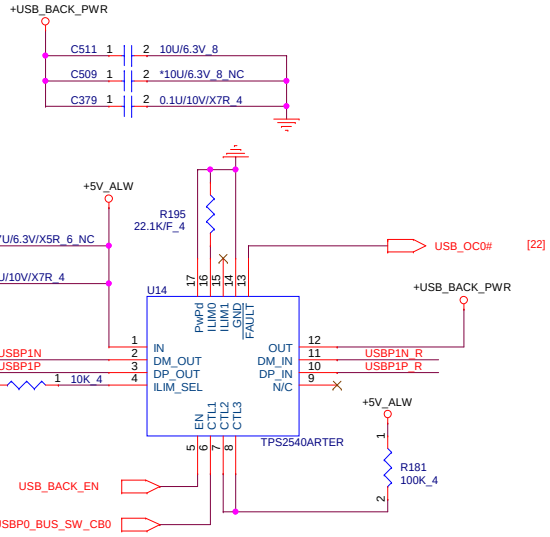
Quanta Computer Inc.
PROJECT : JWA

Size	Document Number	Rev
	LAN (AR8161A / AR8162)colay	3A
Date: Tuesday, February 26, 2013	Sheet 30 of 54	

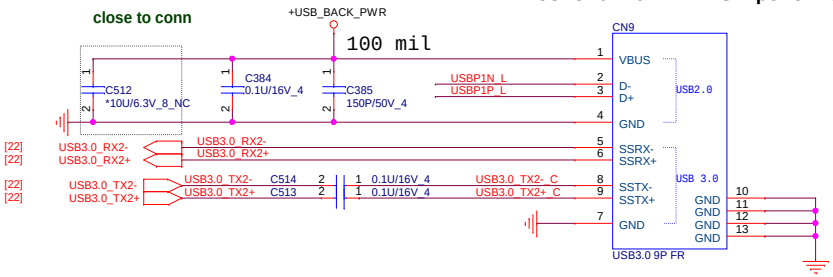
USB CONN with Power share (USB3.0 port 2)

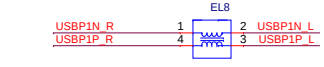
USBP0_BUS_SW_CB0	Mode	Operating at
Low	DCP, Auto-detect	S3/S4/S5, 1.5 A
High	CDP, BC Spec 1.1	S0, 1.5 A

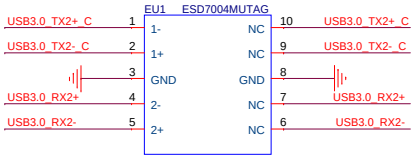
	R109	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

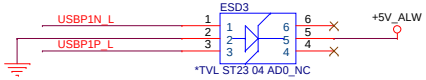


USB3.0 PORT2 with power share





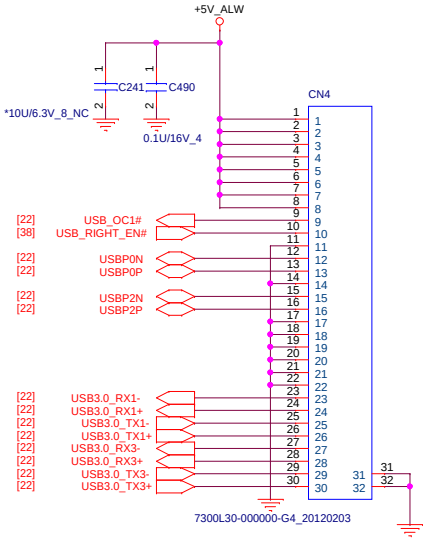




Quanta Computer Inc.
PROJECT : JWA

Size	Document Number	Rev
	USB 3.0 port / USB power share	3A
Date: Tuesday, February 26, 2013	Sheet 31 of 54	

USB CONN*2 (USB3.0 port 0 & 3) BTB CN

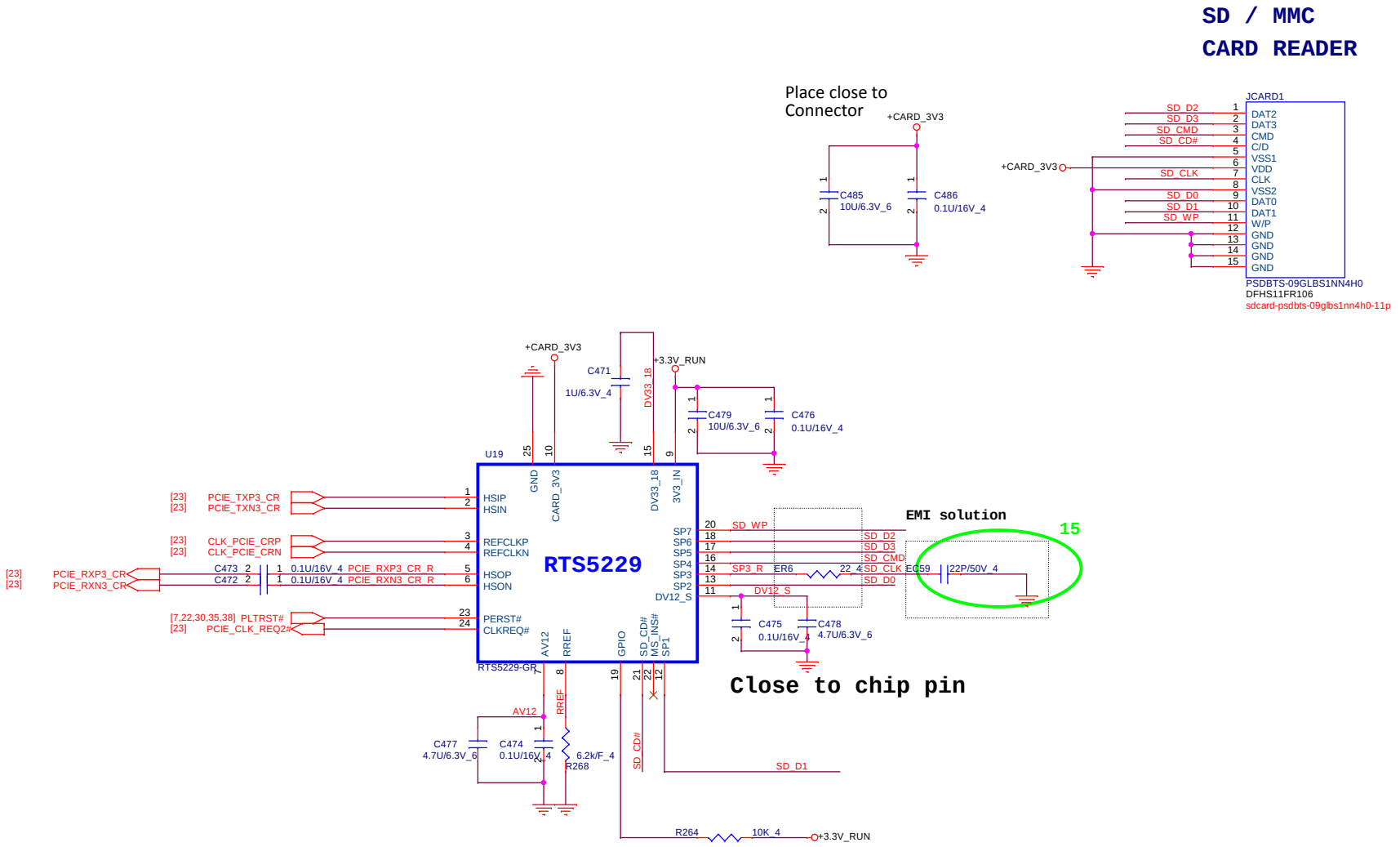


USB3.0 PORT1
USB3.0 PORT1
USB3.0 PORT3
USB3.0 PORT3

Quanta Computer Inc.
PROJECT : JWA

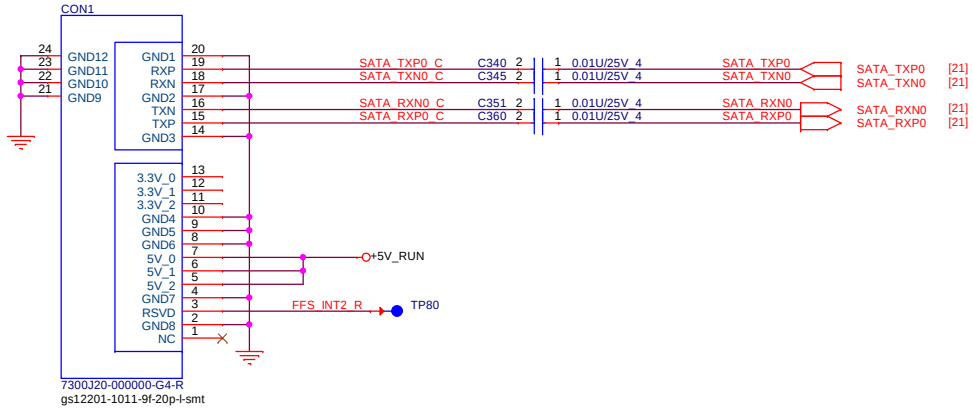
Size	Document Number	Rev
	USB 3.0 port*2	3A
Date: Tuesday, February 26, 2013	Sheet 32 of 54	

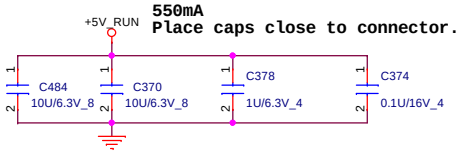
Cardreader (RTS5229) Support Micro SD/ MMC



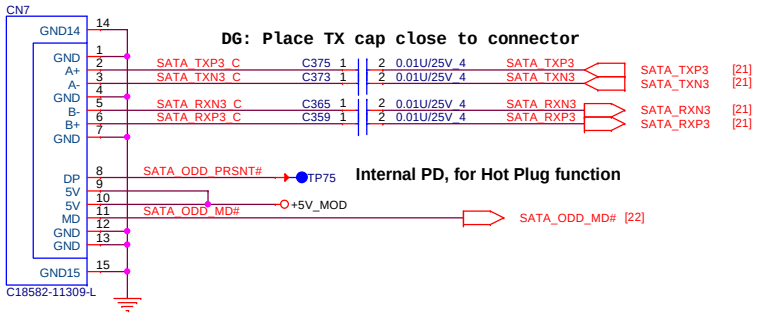
Quanta Computer Inc.		
PROJECT : JWA		
Size	Document Number: Card Reader (RTS5229)	Rev: 3A
Date: Wednesday, March 06, 2013	Sheet 33 of 54	

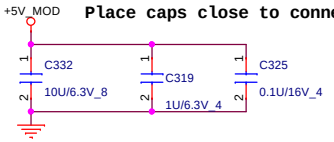
HDD



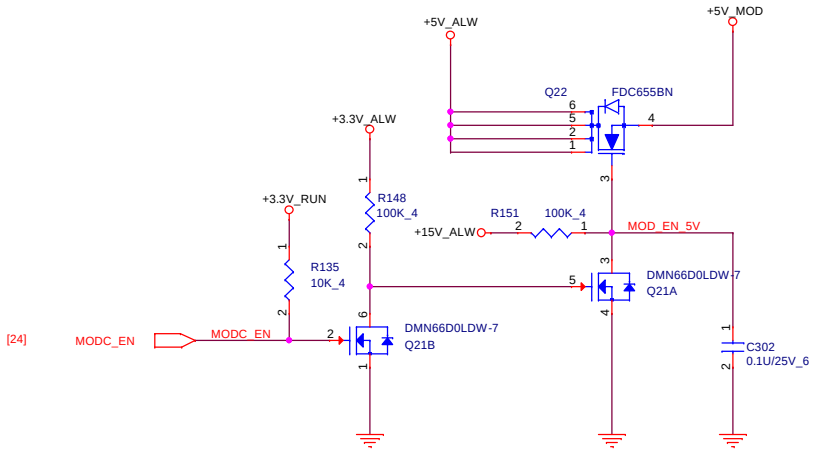


ODD





Support Zero power ODD



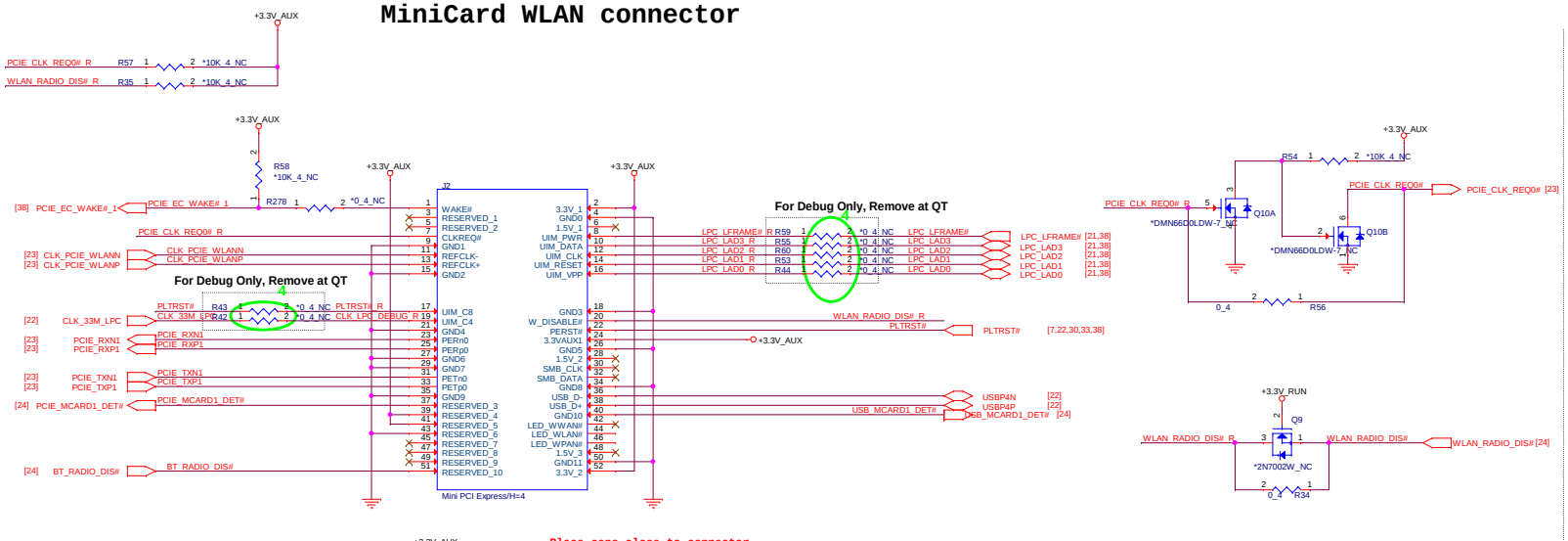
Quanta Computer Inc.

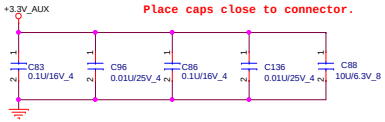
PROJECT : JWA

Size	Document Number	Rev
	SATA HDD/ODD	3A

Date: Tuesday, February 26, 2013 Sheet 34 of 54

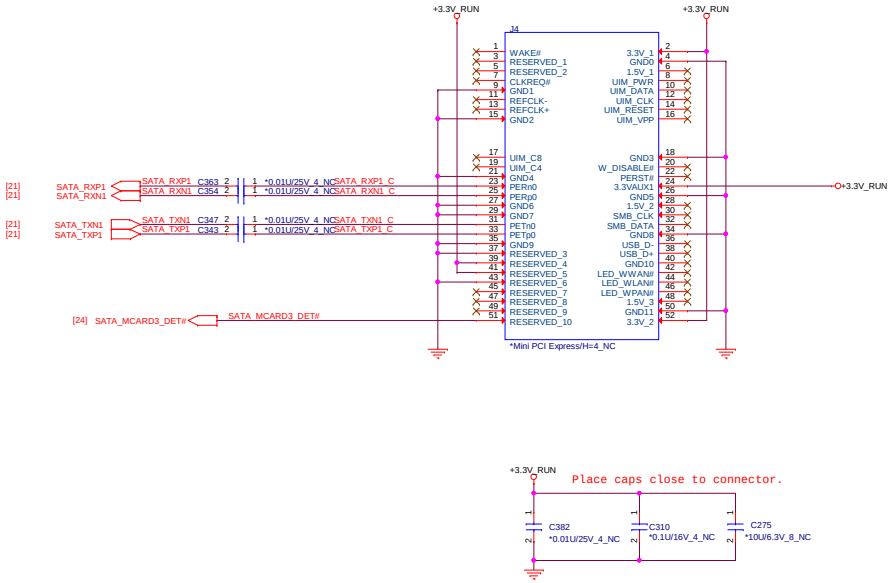
MiniCard WLAN connector





	R57	R58	R56	R54	R34	R179	R17	R35	Q10	Q8	Q4	Q9	C74	R278
AOAC	0	0	X	0	X	X	0	0	0	0	0	0	0	0
No AOAC	X	X	0	X	0	0	X	X	X	X	X	X	X	X

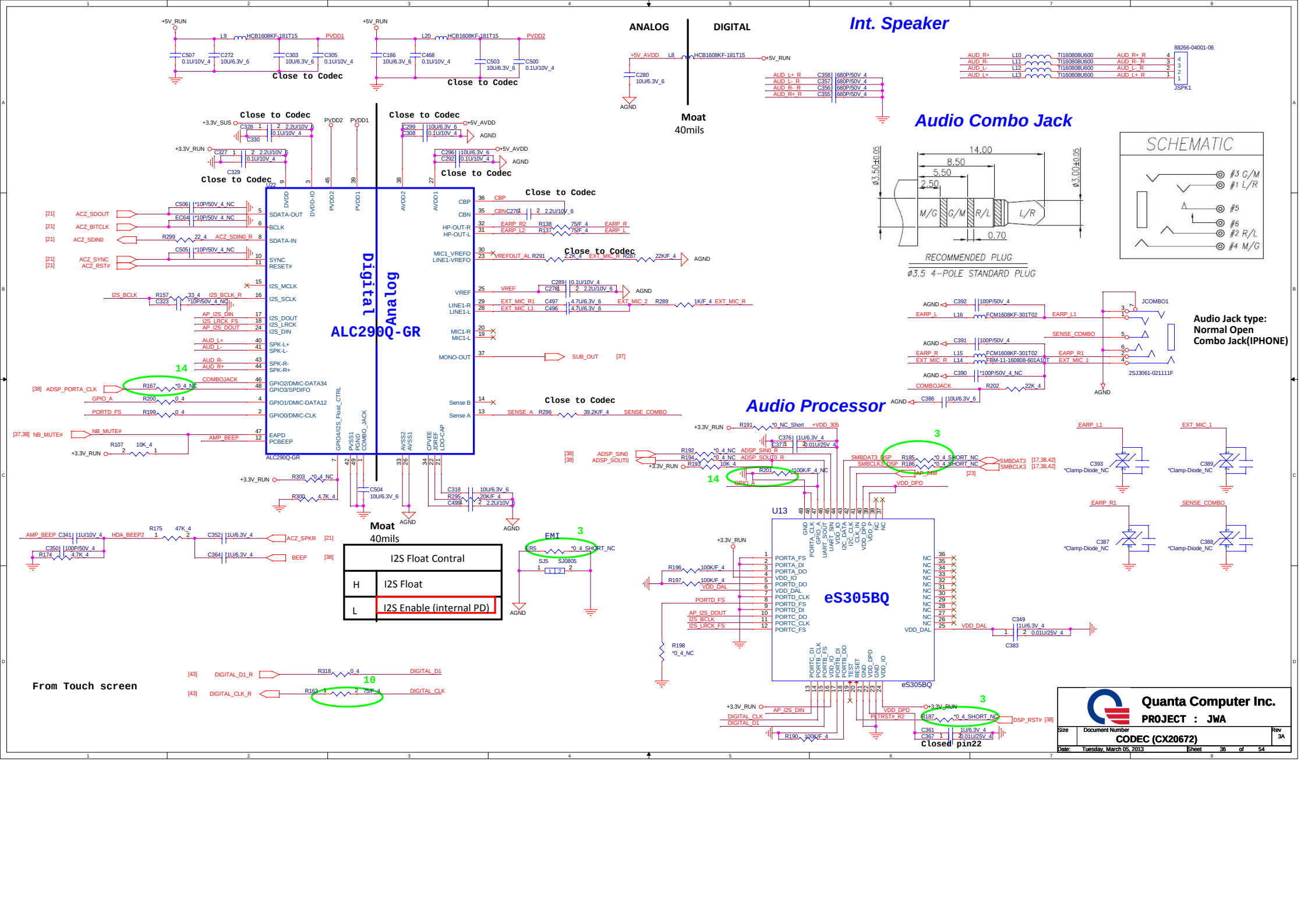
mSATA Connector



	J4	C363	C354	C347	C343	C382	C310	C275	H20
MSATA	0	0	0	0	0	0	0	0	0
Non MSATA	X	X	X	X	X	X	X	X	X

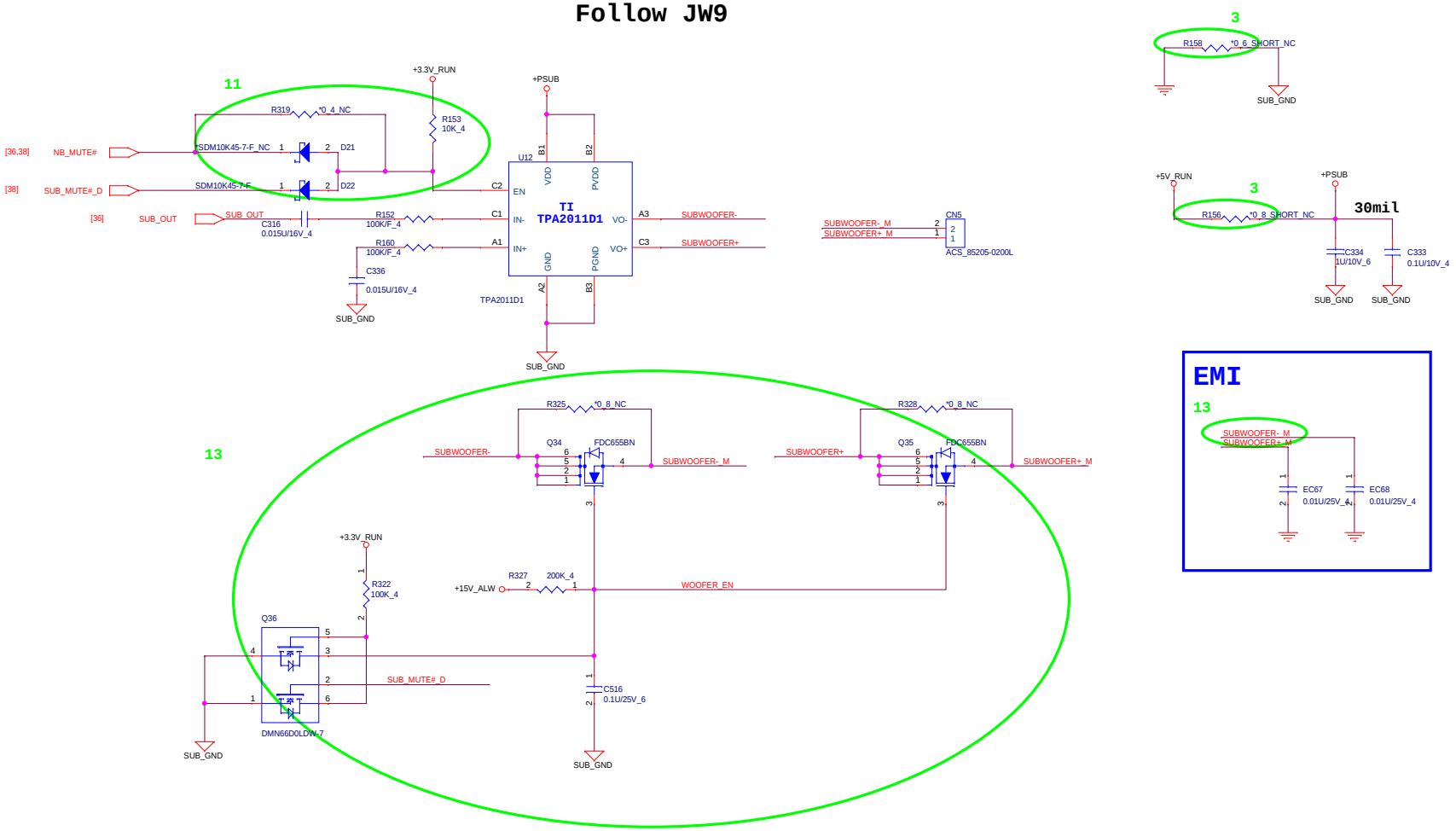
Quanta Computer Inc.
PROJECT : JWA

Size	Document Number	Rev
	MiniCard / mSATA	3A
Date: Tuesday, February 26, 2013	Sheet 35 of 54	


Int. Speaker
Audio Combo Jack
Audio Processor
ALC290Q-GR
Digital
Analog
ANALOG
DIGITAL
Moat
40mils
Close to Codec
SCHEMATIC
#3 G/M
#1 L/R
#5
#6
#2 R/L
#4 M/G
RECOMMENDED PLUG
Ø3.5 4-POLE STANDARD PLUG
Audio Jack type:
Normal Open
Combo Jack(IPHONE)
I2S Float Contral
H
I2S Float
L
I2S Enable (internal PD)
From Touch screen
eS305BQ
Closed pin22
Quanta Computer Inc.
PROJECT : JWA
CODEC (CX20672)
Tuesday, March 05, 2013

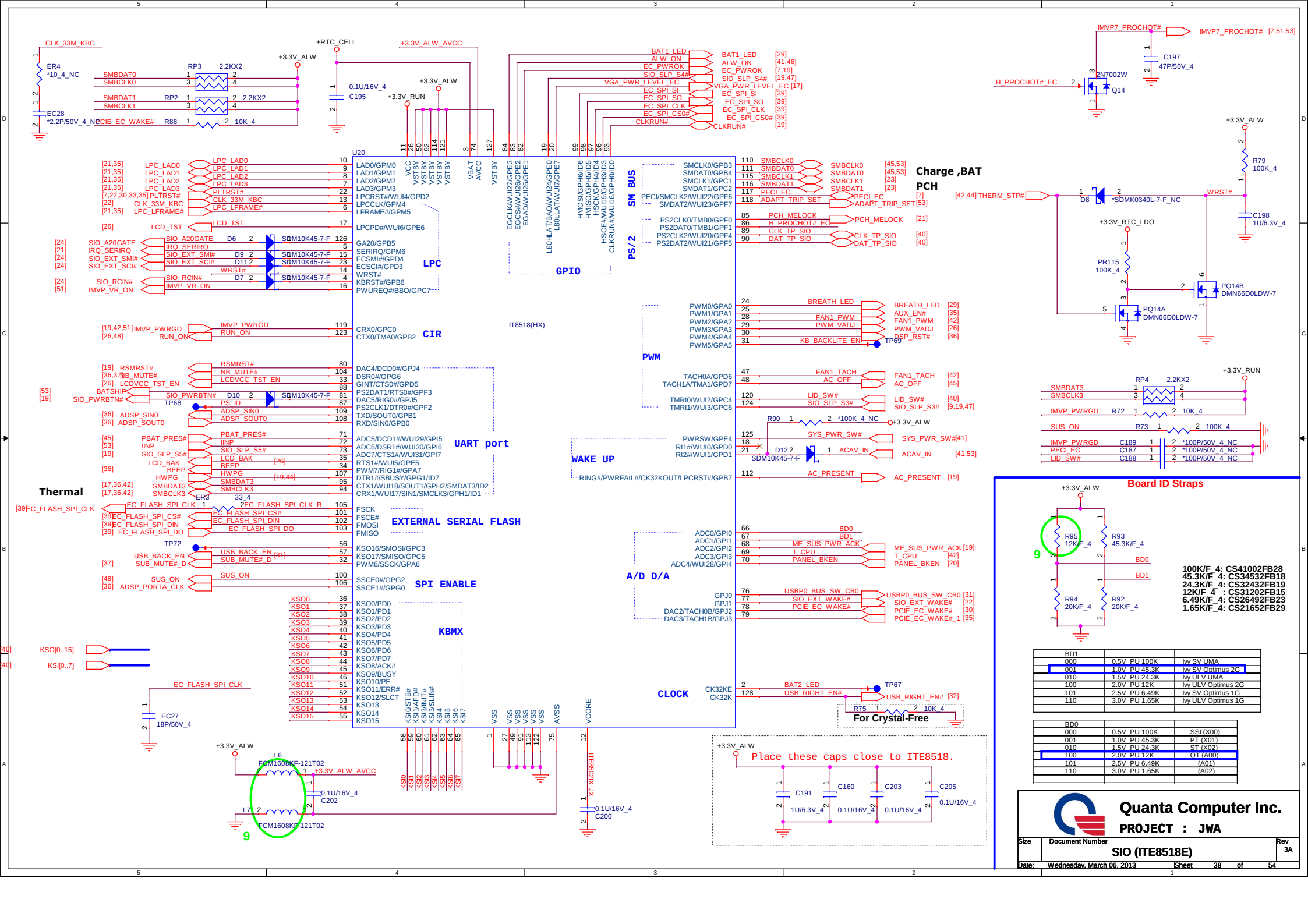
Subwoofer Amp

Follow JW9



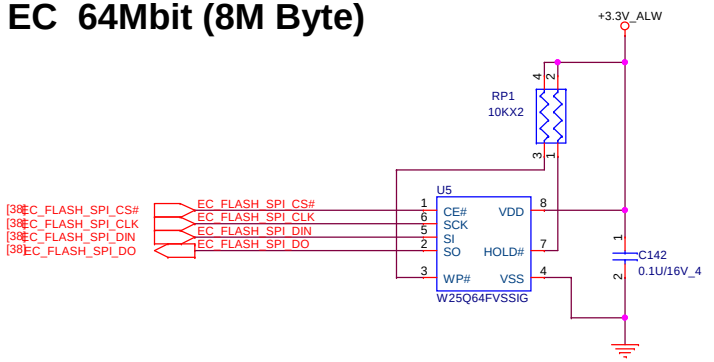
	R319	D21	D22	R153
NB_MUTE control SUB.	X	X	X	0
SUB can be controlled separately.	0	X	0	X

Quanta Computer Inc.	PROJECT : JWA		
Size	Document Number: Subwoofer		Rev 3A
Date: Tuesday, March 05, 2013	Sheet 37 of 54		

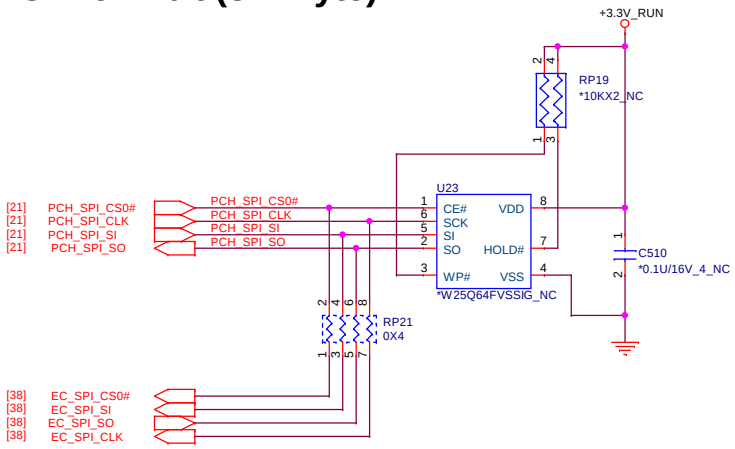

U20
IT8518(HX)
LPC
CIR
GPIO
SM BUS
PS/2
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Charge ,BAT
PCH
Thermal
Board ID Straps
For Crystal-Free
Place these caps close to ITE8518.
100K/F_4: CS41002FB28
45.3K/F_4: CS34532FB18
24.3K/F_4: CS32432FB19
12K/F_4 : CS31202FB15
6.49K/F_4: CS26492FB23
1.65K/F_4: CS21652FB29
Quanta Computer Inc.
PROJECT : JWA
SIO (ITE8518E)
Wednesday, March 06, 2013

FLASH / RTC

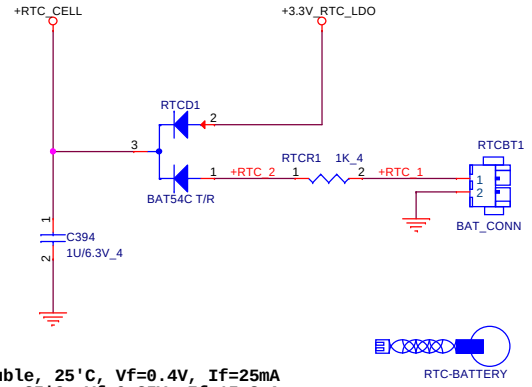
For EC 64Mbit (8M Byte)



For PCH 64Mbit (8M Byte)



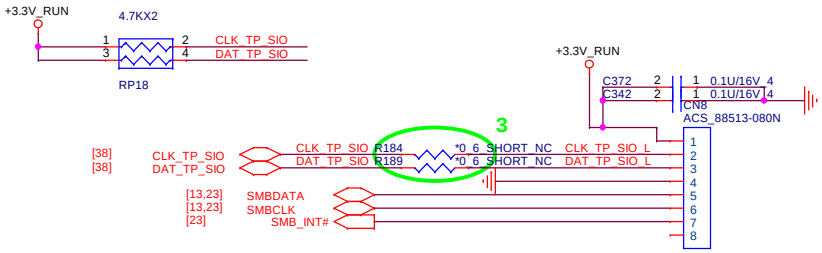
RTC



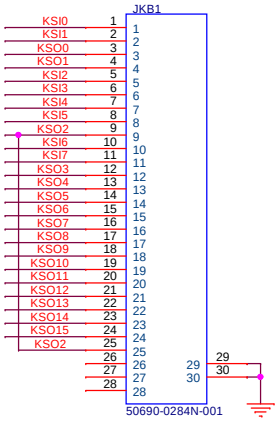
Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA

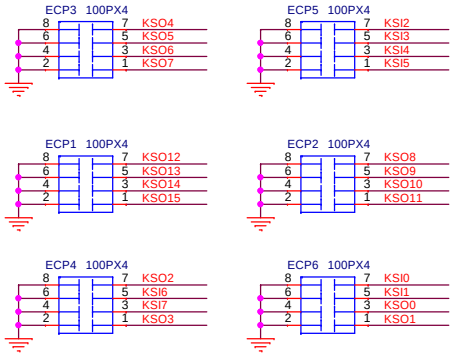
Quanta Computer Inc.		
PROJECT : JWA		
Size	Document Number: FLASH / RTC	Rev: 3A
Date: Tuesday, February 26, 2013	Sheet 39 of 54	

TP CONNECTOR



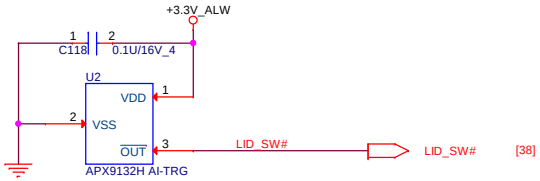
KB CONN





Layout Note: 100P CAPS CLOSE TO JKB1

HALL Sensor



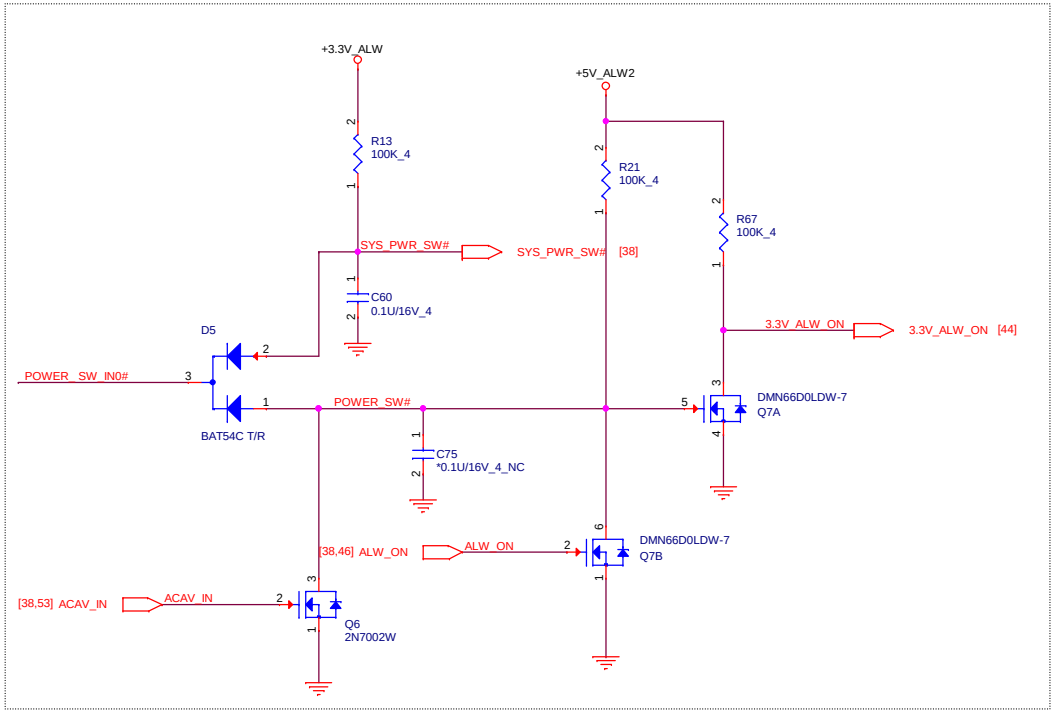
Quanta Computer Inc.

PROJECT : JWA

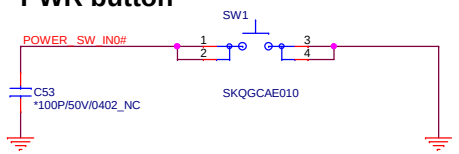
Size	Document Number	Rev
	TP / KB/HALL	3A

Date: Tuesday, February 26, 2013 Sheet 40 of 54

3V ALW ON POWER LOGIC



PWR button

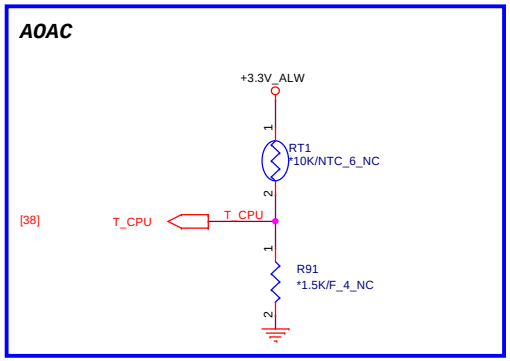


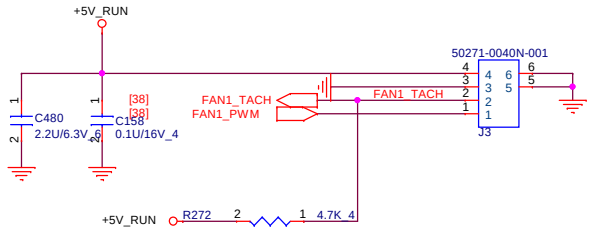
Quanta Computer Inc.

PROJECT : JWA

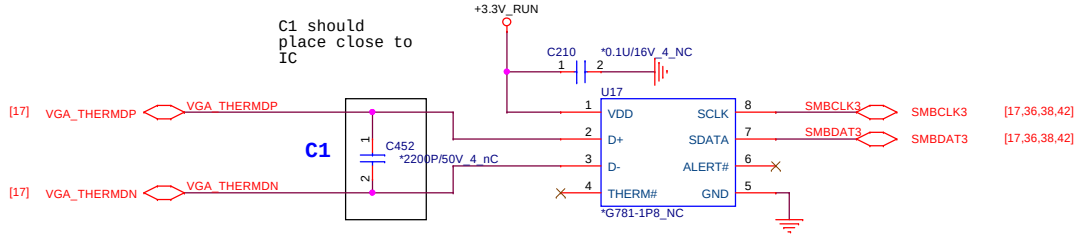
Size	Document Number	Rev
	PWR SW/LED	3A
Date: Tuesday, February 26, 2013	Sheet 41 of 54	

FAN CONN





G781-1P8
SMBus address is 1001101xb (9Ah) (x is R/W bit).

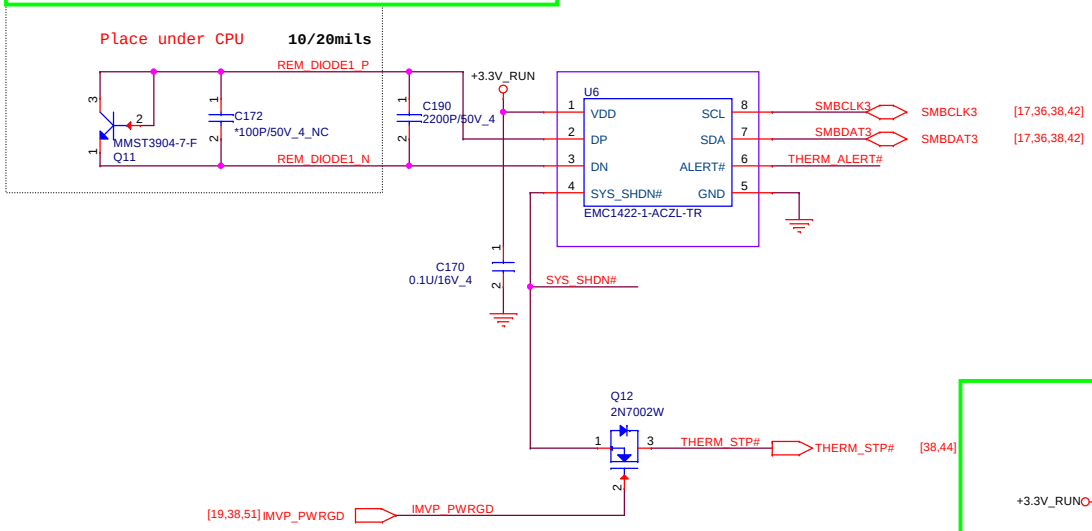


EMC1422 SMBus address is 1001_100xb (98h) (x is R/W bit).

SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

THERMAL IC

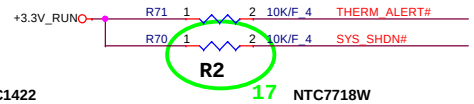
1.Place C586 close to EMC1422-U1
2.Place C585 to be close to Q38
Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C586, then C585 should be dummy



CHECK OTP WITH Thermal.

OTP 85 degree C

R1



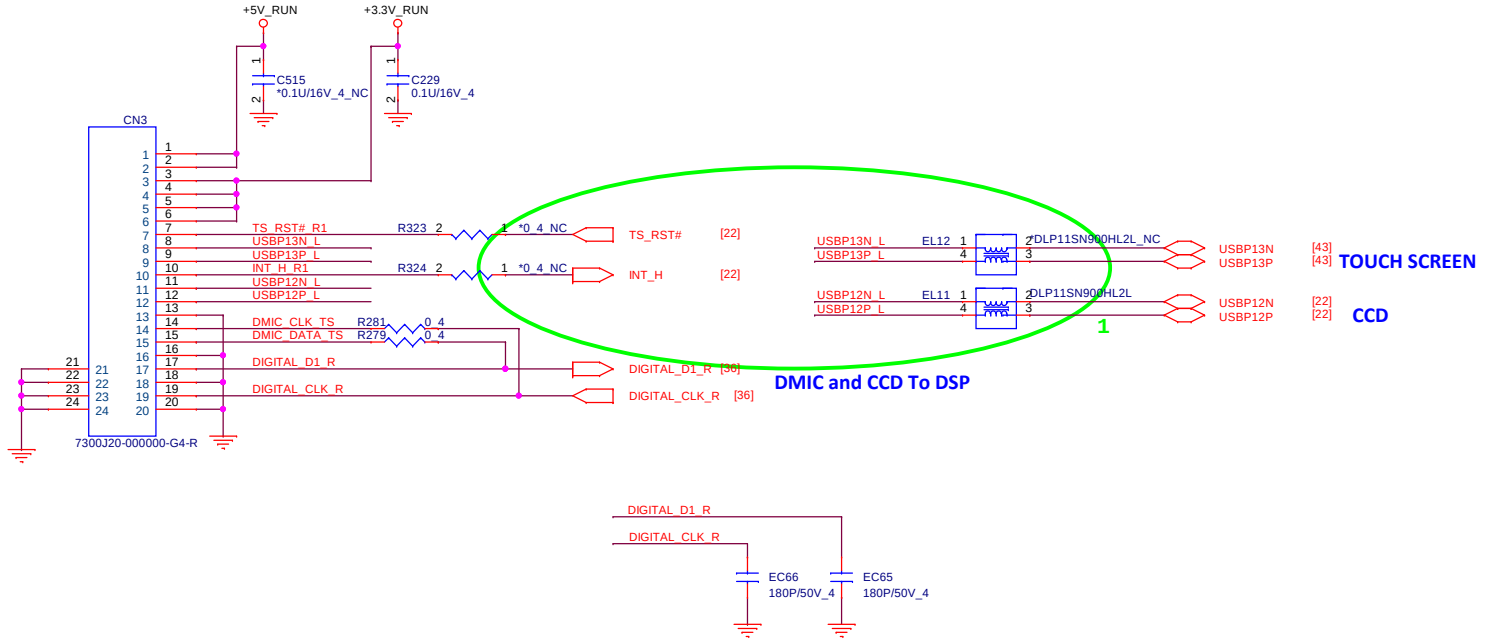
R2

EMC1422
OTP 85 degree : R1 = 10K, R2 = 6.8K
OTP 90 degree : R1 = 6.8K, R2 = 10K
OTP 90 degree : R1 = 10K, R2 = 10K

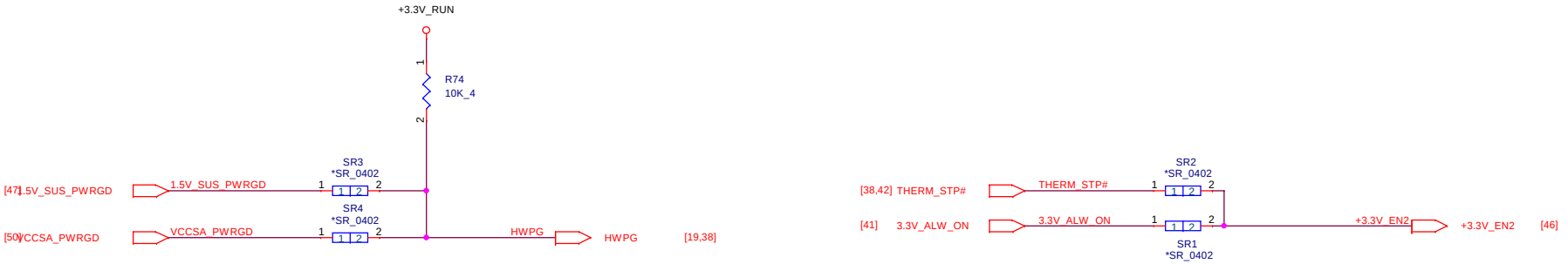
NTC7718W
OTP 85 degree : R361 = 18.7K, R362 = 2K
OTP 91 degree : R361 = 10.5K, R362 = 7.5K

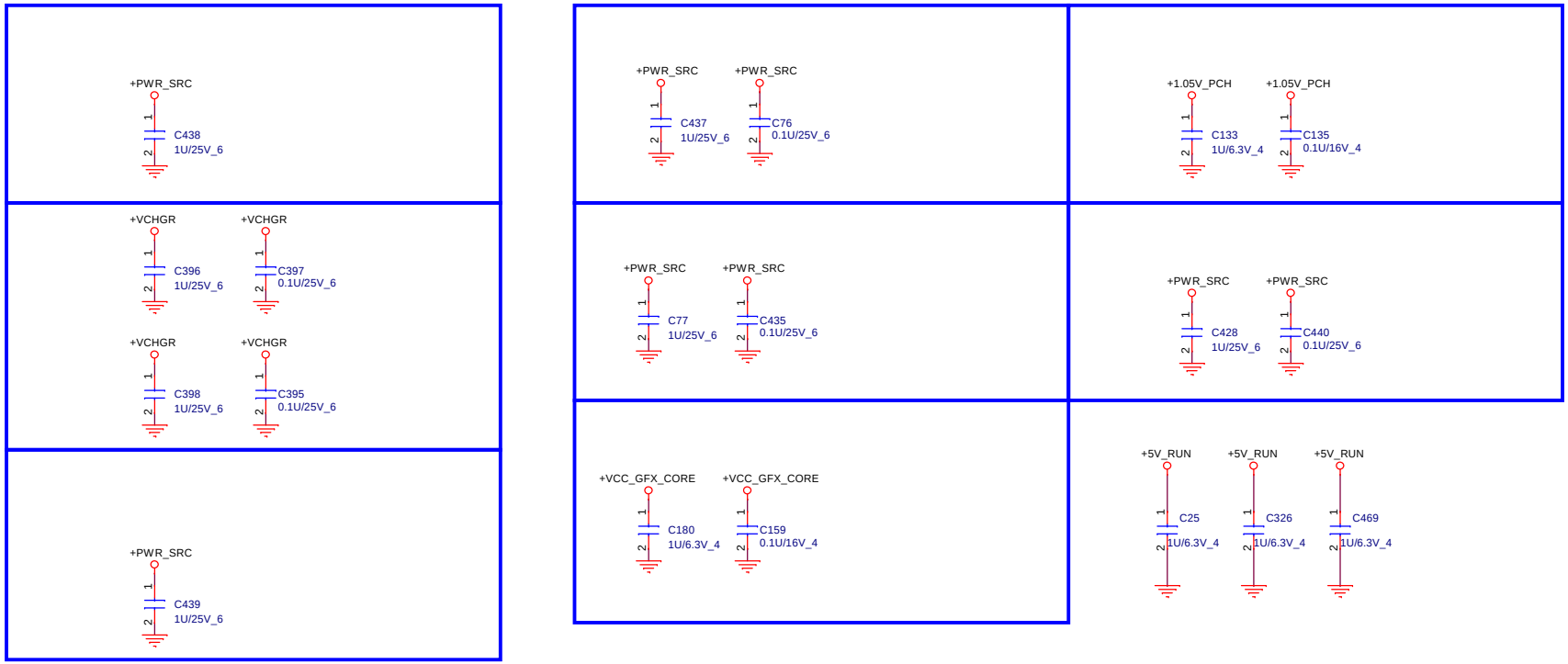
Quanta Computer Inc.
PROJECT : JWA
Size | Document Number: **FAN & THERMAL** | Rev: 3A
Date: Wednesday, March 06, 2013 | Sheet 42 of 54

Touch Screen



Quanta Computer Inc.		
PROJECT : JWA		
Size	Document Number: Touch Screen	Rev: 3A
Date: Tuesday, March 05, 2013	Sheet 43 of 54	



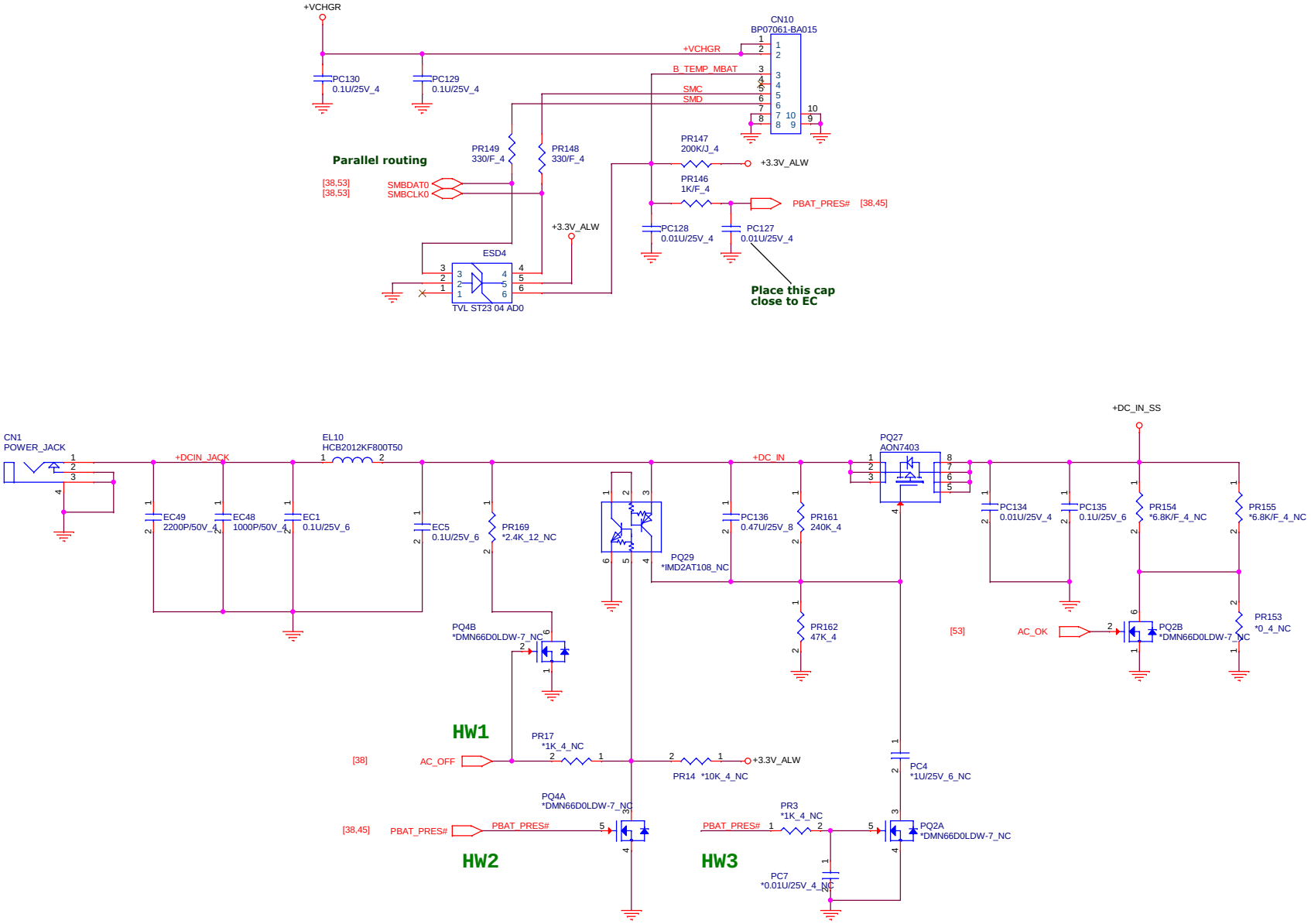


Quanta Computer Inc.

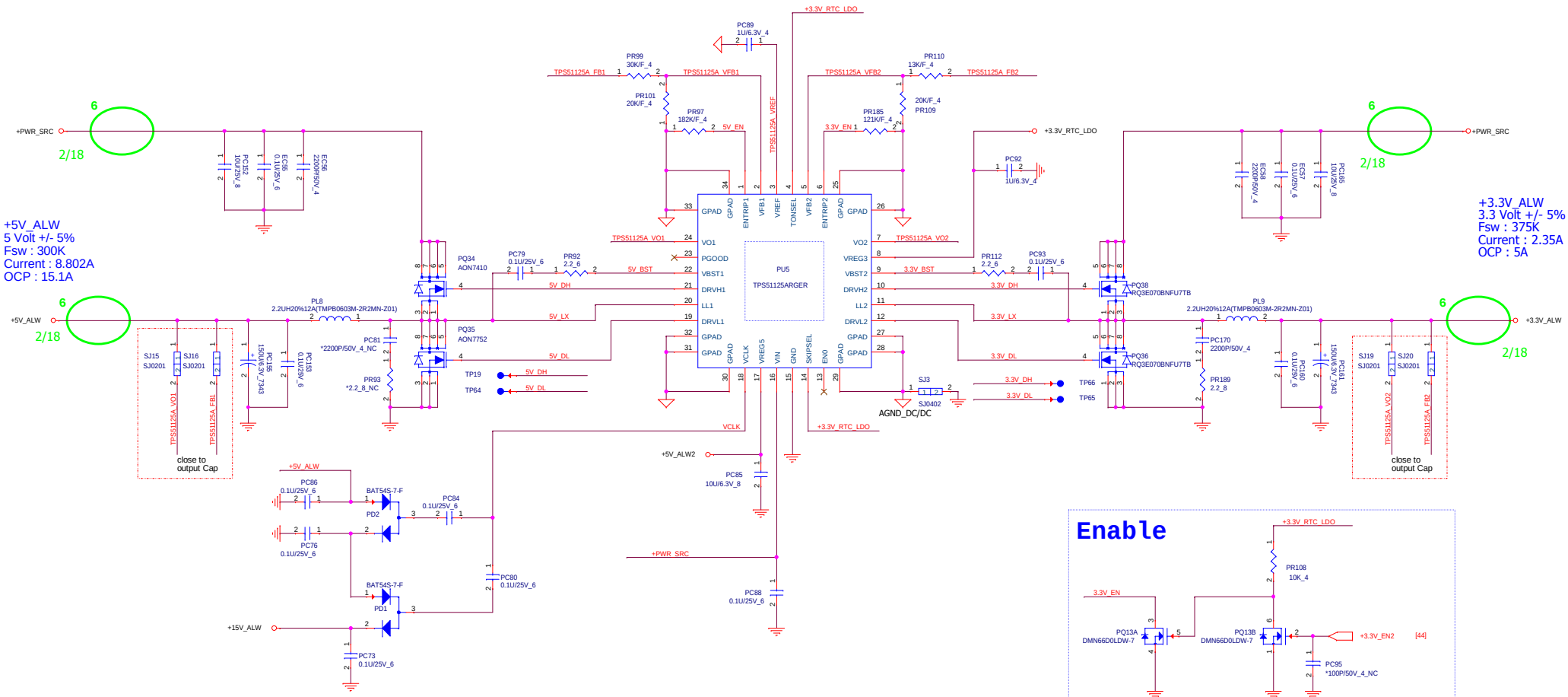
PROJECT : JWA

Size	Document Number	Rev
	System Reset Circuit	1A

Date: Tuesday, February 26, 2013 Sheet 44 of 54



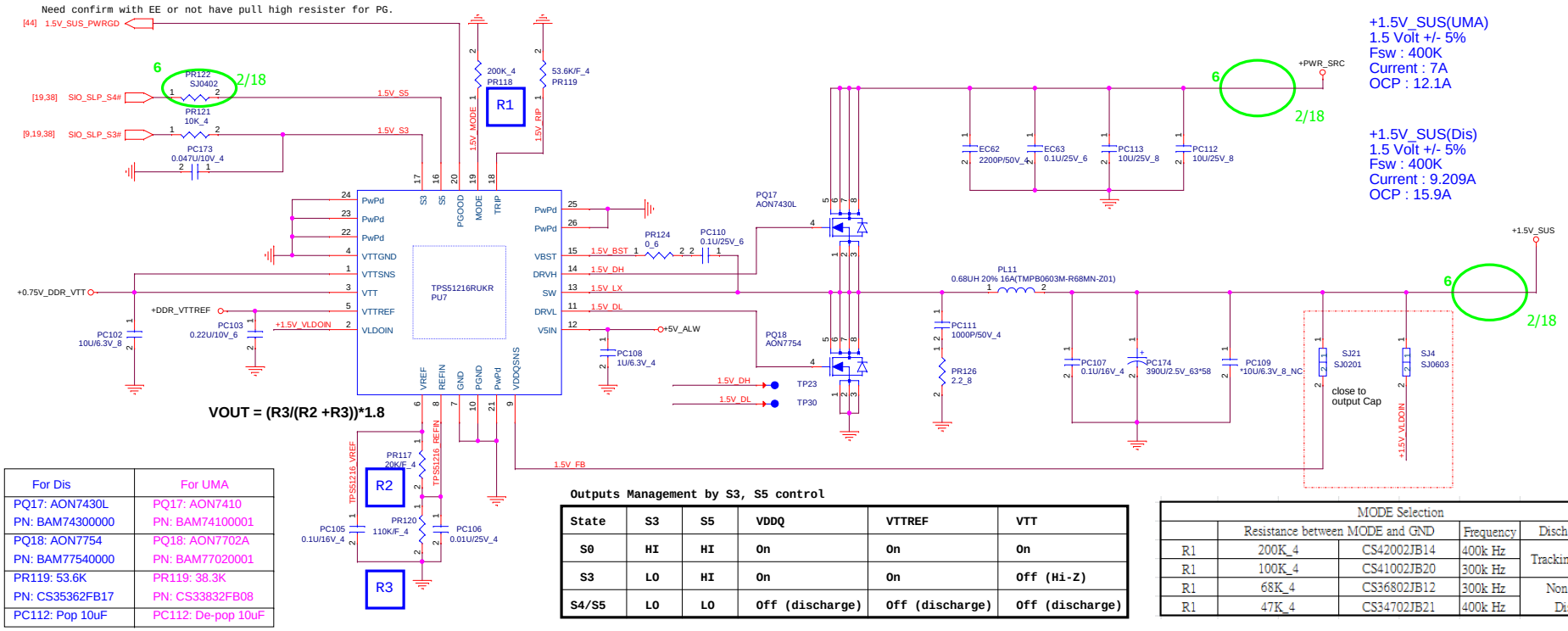
Quanta Computer Inc.		
PROJECT : JWA		
Size	Document Number: DC IN / BATT	Rev: 1A
Date: Tuesday, February 26, 2013	Sheet 45 of 54	



TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz

Quanta Computer Inc.
PROJECT : JWA

Size	Document Number	Rev
	3.3V_ALW / 5V_ALW (TPS51125ARGER)	1A
Date: Tuesday, February 26, 2013	Sheet 46 of 54	



+1.5V_SUS(UMA)
1.5 Volt +/- 5%
Fsw : 400K
Current : 7A
OCP : 12.1A

+1.5V_SUS(Dis)
1.5 Volt +/- 5%
Fsw : 400K
Current : 9.209A
OCP : 15.9A

VOUT = (R3/(R2 +R3))*1.8

For Dis	For UMA
PQ17: AON7430L	PQ17: AON7410
PN: BAM74300000	PN: BAM74100001
PQ18: AON7754	PQ18: AON7702A
PN: BAM77540000	PN: BAM77020001
PR119: 53.6K	PR119: 38.3K
PN: CS35362FB17	PN: CS33832FB08
PC112: Pop 10uF	PC112: De-pop 10uF

Outputs Management by S3, S5 control

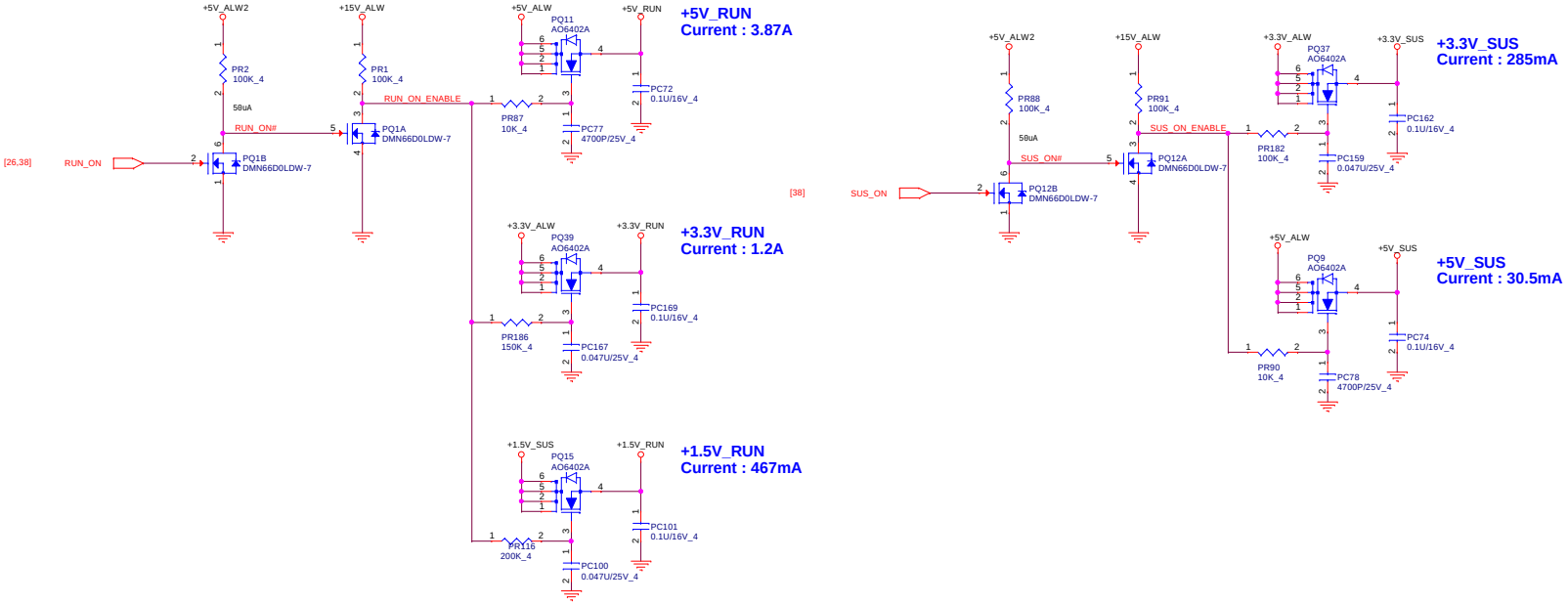
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

MODE Selection				
	Resistance between MODE and GND		Frequency	Discharge Mode
R1	200K_4	CS42002JB14	400k Hz	Tracking Discharge
R1	100K_4	CS41002JB20	300k Hz	
R1	68K_4	CS36802JB12	300k Hz	Non-tracking
R1	47K_4	CS34702JB21	400k Hz	Discharge

Quanta Computer Inc.
PROJECT : JWA

Size	Document Number	Rev
	1.5_SUS/0.75_DDR_VTT (TPS51216RUKR)	1A

Date: Tuesday, February 26, 2013 Sheet 47 of 54

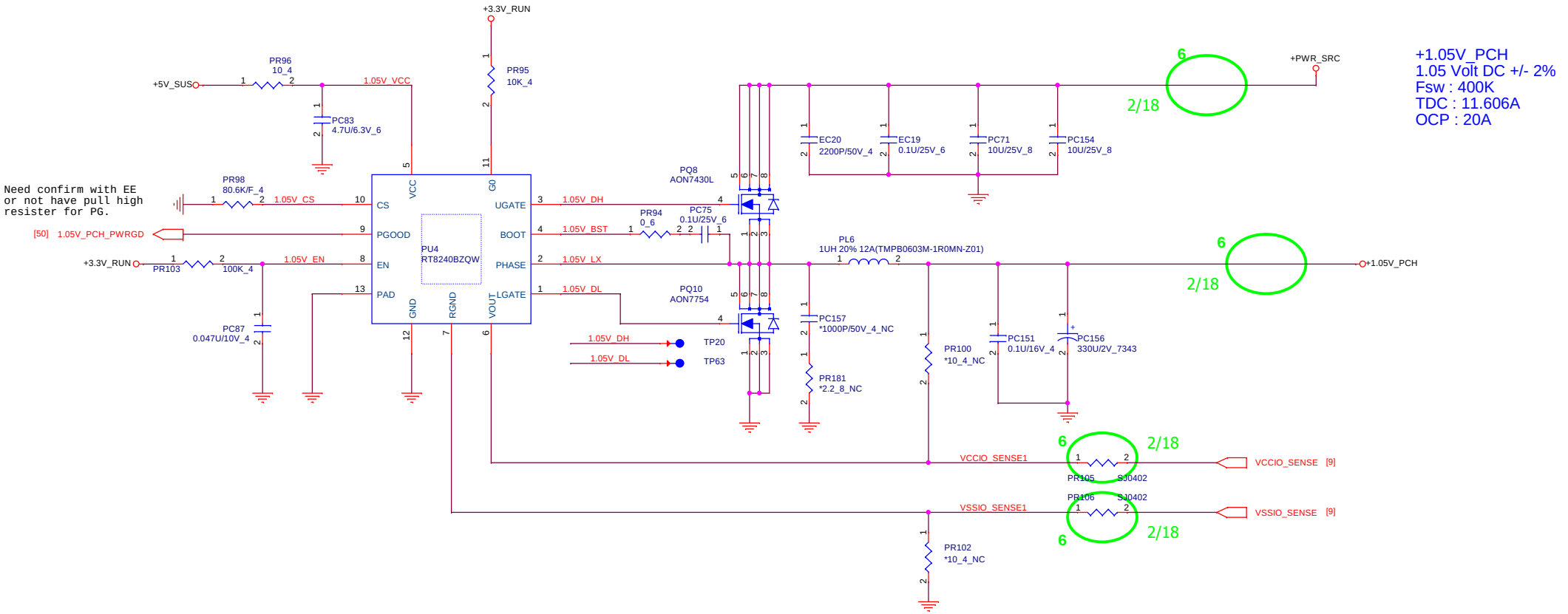


Quanta Computer Inc.

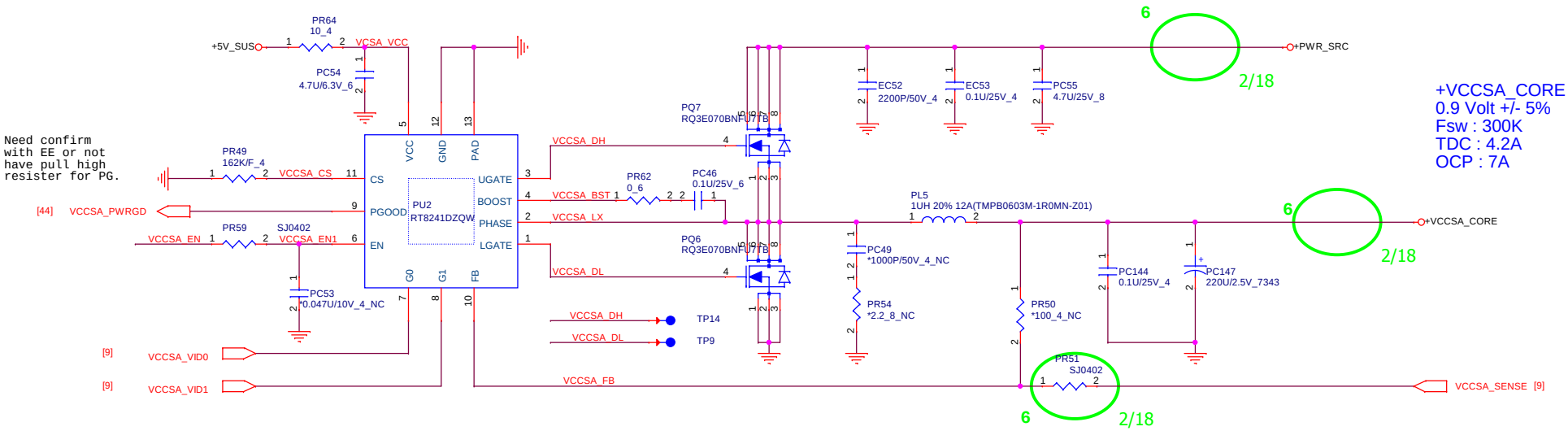
PROJECT : JWA

Size	Document Number	Rev
	Load Switch	1A

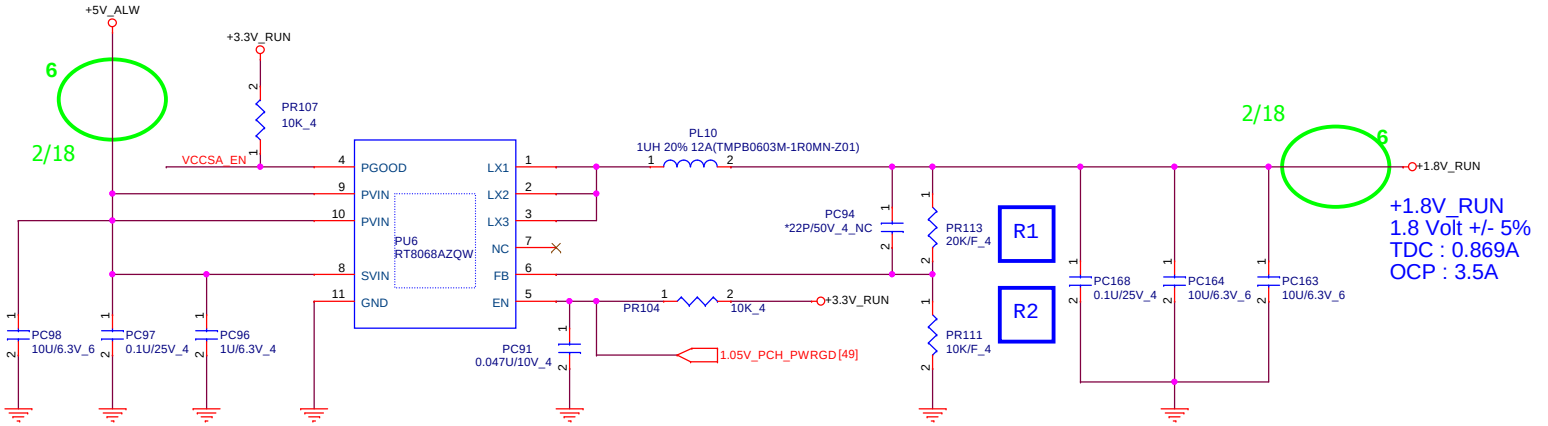
Date: Tuesday, February 26, 2013 Sheet 48 of 54



Quanta Computer Inc.		
PROJECT : JWA		
Size	Document Number: +1.05V_PCH / VTT (RT8240BZQW)	Rev: 1A
Date: Tuesday, February 26, 2013	Sheet 49 of 54	

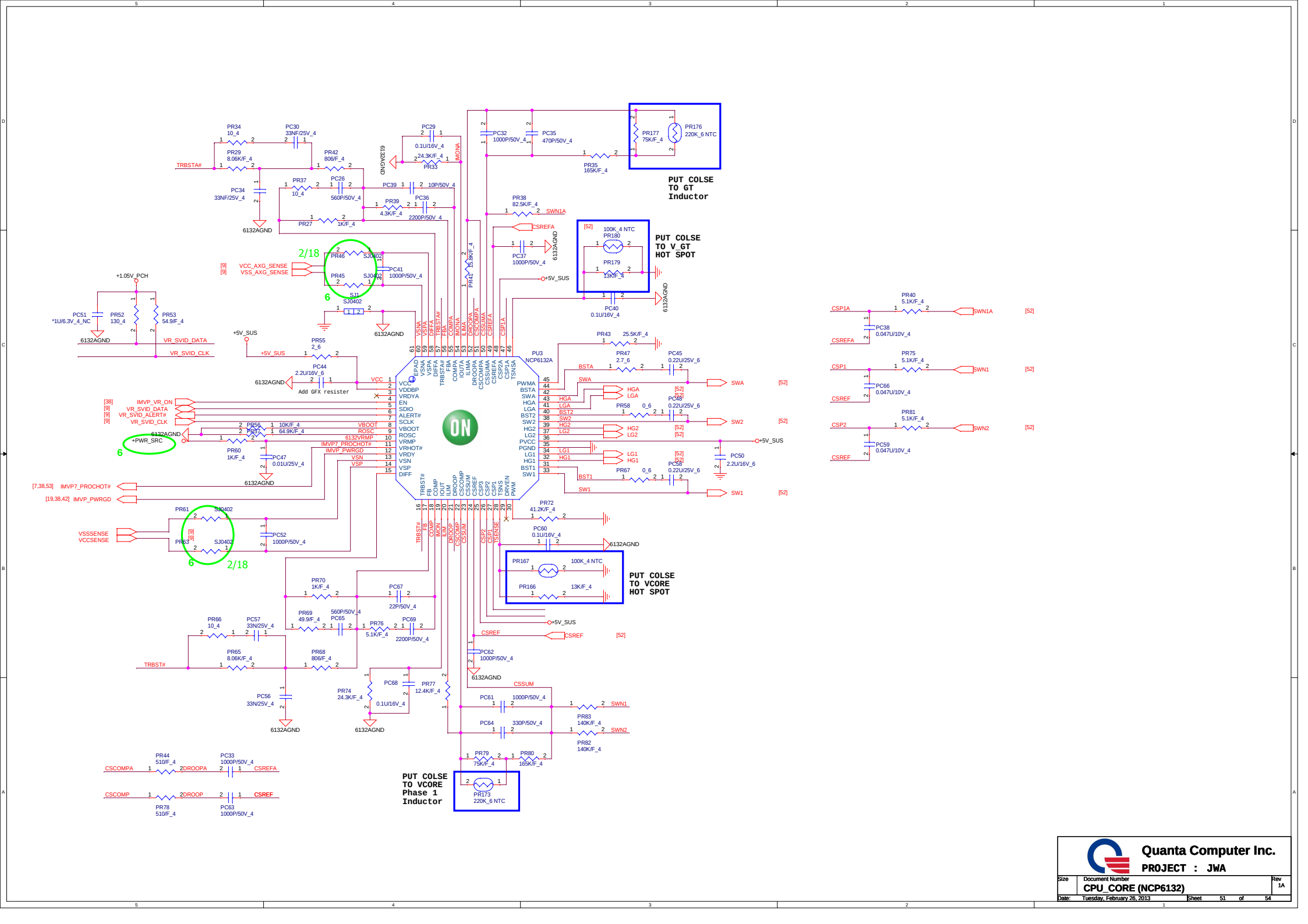


VCCSA_VID1	VCCSA_VID0	VCCSA_CORE
Low	Low	0.9V
High	Low	0.8V
Low	High	0.725V
High	High	0.675V

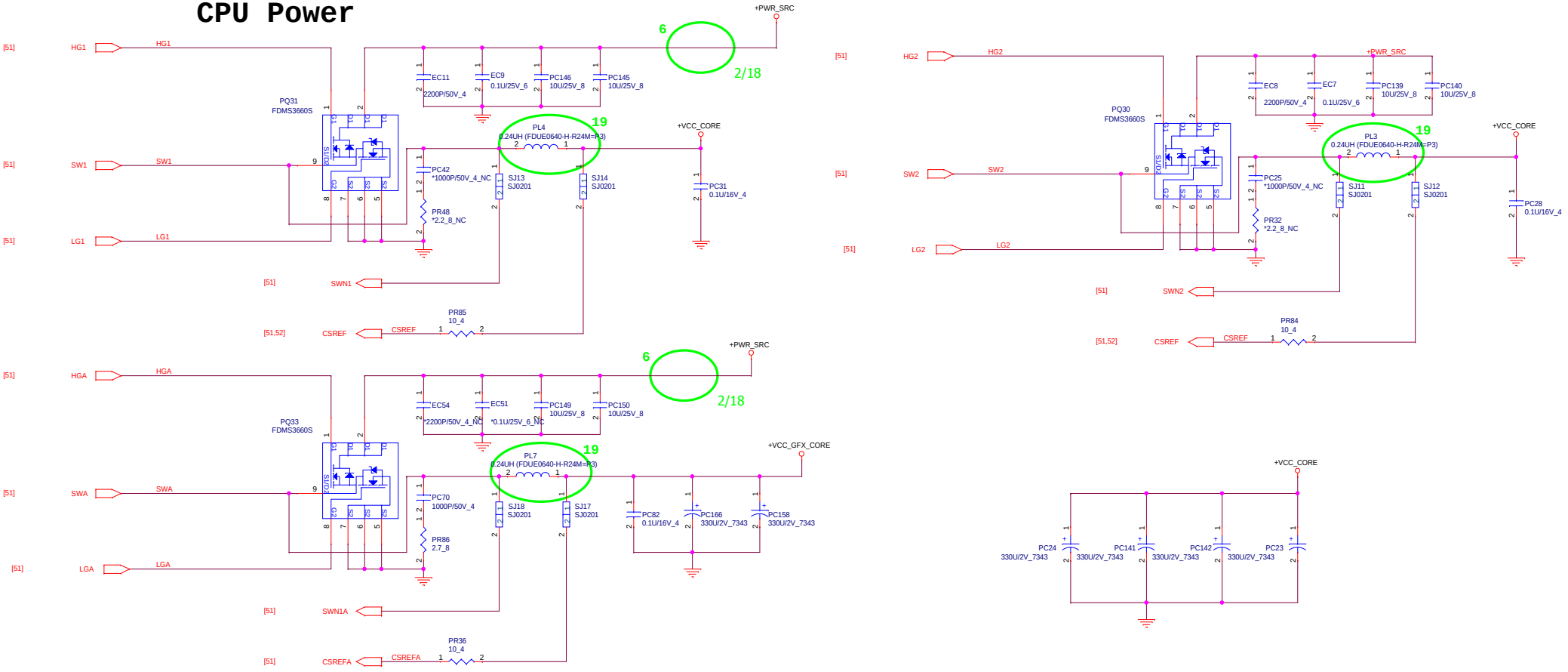


VOUT = 0.6(1+R1/R2)

Quanta Computer Inc.		
PROJECT : JWA		
Size	Document Number: VCCSA (RT8241DZQW)	Rev: 1A
Date: Tuesday, February 26, 2013	Sheet 50 of 54	


PUT COLSE TO GT Inductor
PUT COLSE TO V_GT HOT SPOT
PUT COLSE TO VCORE HOT SPOT
PUT COLSE TO VCORE Phase 1 Inductor
PU3 NCP6132A
Add GFX resister
+PWR_SRC
+1.05V_PCH
+5V_SUS
6132AGND
VR_SVID_DATA
VR_SVID_CLK
IMVP_VR_ON
IMVP7_PROCHOT#
IMVP_PWRGD
VSSSENSE
VCCSENSE
VCC_AXG_SENSE
VSS_AXG_SENSE
TRBSTA#
TRBST#
CSREFA
CSREF
SWN1A
SWN1
SWN2
SWA
SW1
SW2
HGA
LGA
HG1
LG1
HG2
LG2
CSP1A
CSP1
CSREFA
CSREF
CSP2
CSREF
Quanta Computer Inc.
PROJECT : JWA
CPU_CORE (NCP6132)
Rev 1A
Tuesday, February 26, 2013
Sheet 51 of 54

CPU Power

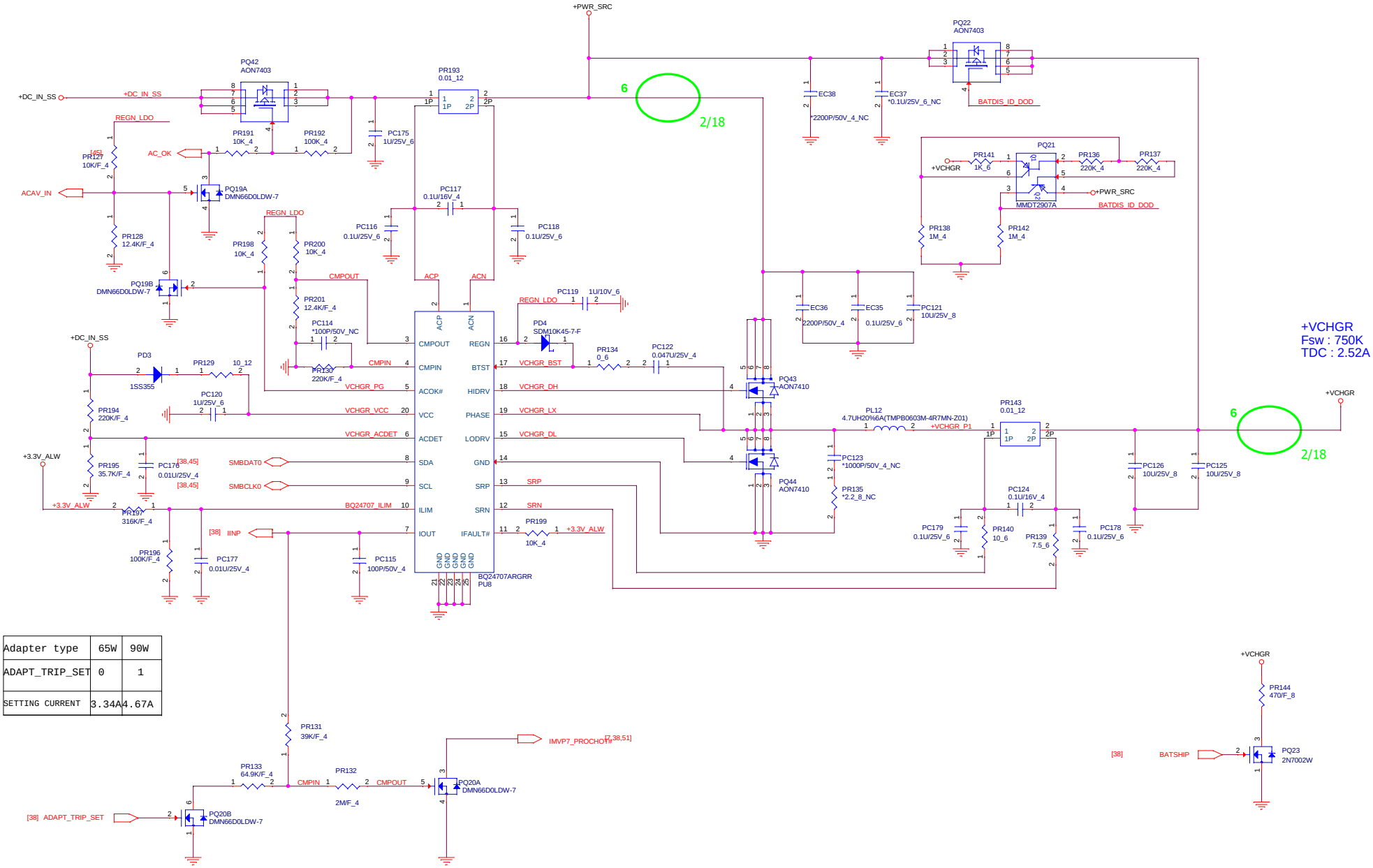


Quanta Computer Inc.

PROJECT : JWA

Size	Document Number	Rev
	CPU_CORE (NCP6132)	1A

Date: Wednesday, March 27, 2013 Sheet 52 of 54



Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.34A	4.67A

Quanta Computer Inc.

PROJECT : JWA

Size	Document Number	Rev
	Charger (BQ24707ARGRR)	1A

Date: Tuesday, February 26, 2013 Sheet 53 of 54

+VCC_GFX_CORE
Fsw : 400K
Current : 27A
OCP : 50A

+3V_GFX
Current : 140mA

+1.5V_GFX
Current : 1.41A

+1.05V_GFX
Current : 937mA

Need confirm with EE
or not have pull high
resister for PG.

PUT COLSE TO
+VCC_GFX_CORE
Phase 1 Inductor

20120209
Change PR217, PR224 to shortpad(short0603)

PU1
NCP3218MNR2G

Quanta Computer Inc.	
PROJECT : JWA	
Size	Document Number: VGA_N11P-dGFX (NCP3218MNR2G) Rev: 1A
Date: Wednesday, March 27, 2013	Sheet 54 of 54