

QIQY5

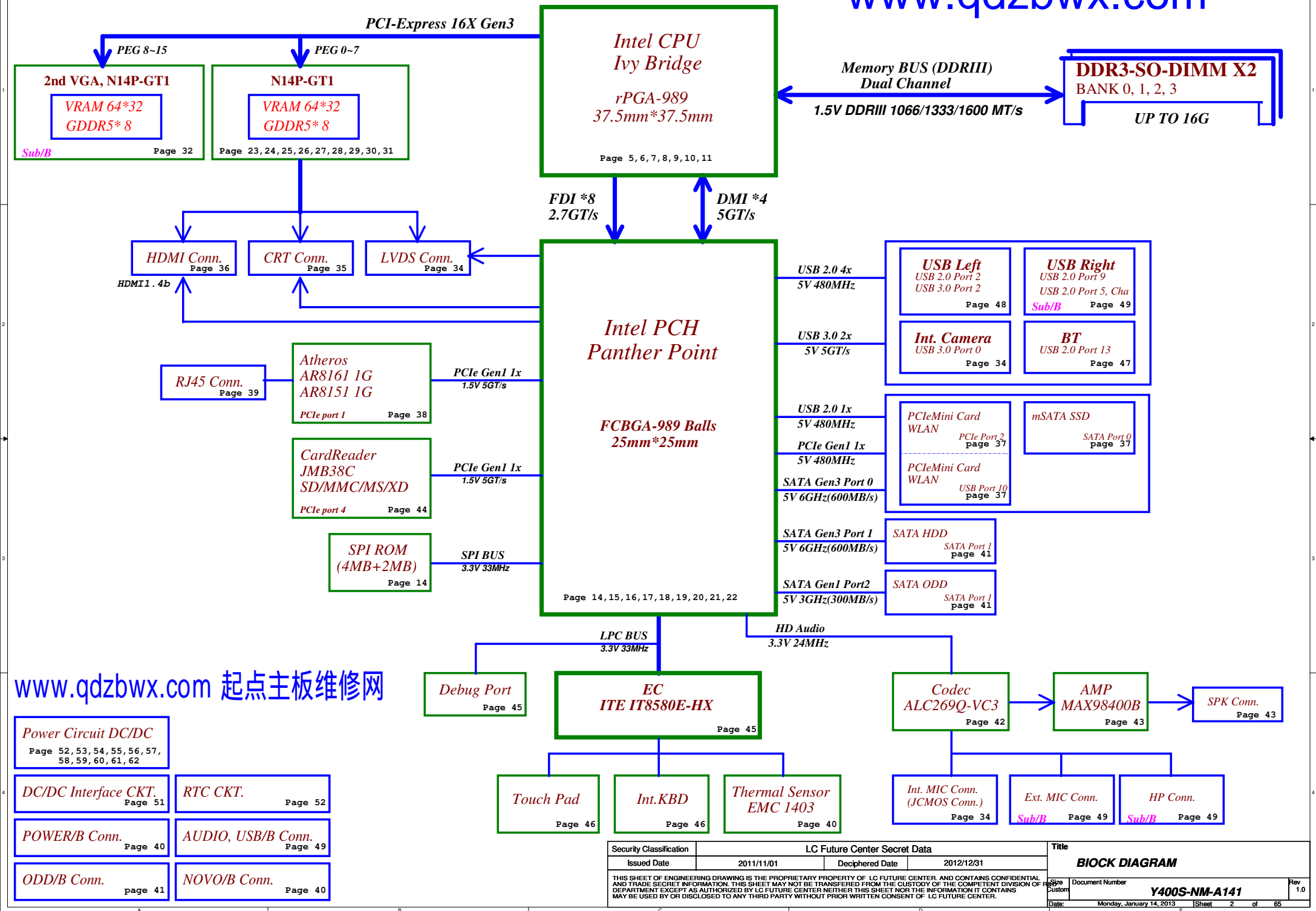
Whisky3.0 (Y400S)

NM-A141 Rev0.2 Schematic

***Intel IVY Bridge Processor with DDRIII + Panther Point PCH
nVIDIA N14P GT + 2nd VGA N14P GT***

2012-10-25-Rev0.2

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
SMB_CLK_S3 SMB_DATA_S3	PCH +3VS	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

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STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
		0	Camera
	XHCI 1	1	
		2	USB Port (Left Side)
		3	
		4	
		5	USB Port (Right Side)
		6	
		7	
		8	
		9	USB Port (Right Side)
		10	Mini Card(WLAN)
		11	
		12	
		13	Blue Tooth

BOM Structure Table

BOM Structure	BTO Item
HDMI@	HDMI part
CHG@	USB charger part
NOCHG@	No USB charger part
CMOS@	CMOS Camera part
8161@	AR8161 LAN part
8151@	AR8151 LAN part
8161S@	AR8161 LAN surge part
8151S@	AR8151 LAN surge part
SURGE@	AR8151/8161 LAN surge part --> Delete (201200627)
61@	X76 P/N for AR8161
51@	X76 P/N for AR8151
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
OPT@	For optimus function part
SLI@	For SLI function part
DS3@	Deep S3 support part
S3@	For S3 function part
GT@	NV chip part
@	Unpop

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	Card Reader
5	
6	
7	
8	

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Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB_CLAMP
GPIO1	OUT	-	
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	
GPIO6	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO7	OUT	-	
GPIO8	I/O	-	OVERT#
GPIO9	OUT	-	VGA_ALERT#
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	NVVD PWM_VID
GPIO12	IN		VGA_AC_DET_R (10K pull High)
GPIO13	OUT	-	DPRS LPVR_VGA
GPIO14	OUT	-	
GPIO15	IN	N/A	
GPIO16	OUT	-	
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HP
GPIO19	IN	-	

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

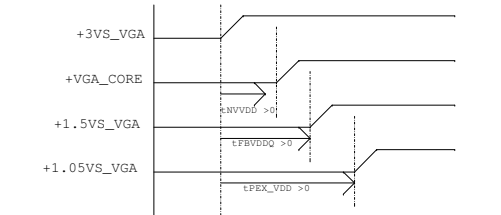
	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

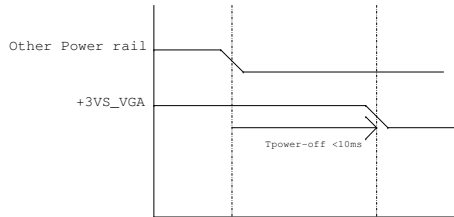
Device ID		setting	I2C Slave addresses ID
N13P-GT (28nm)	0x0FDB	0	0x9E
		1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU		N13P-GT		
FB Memory (GDDR5)		ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K		

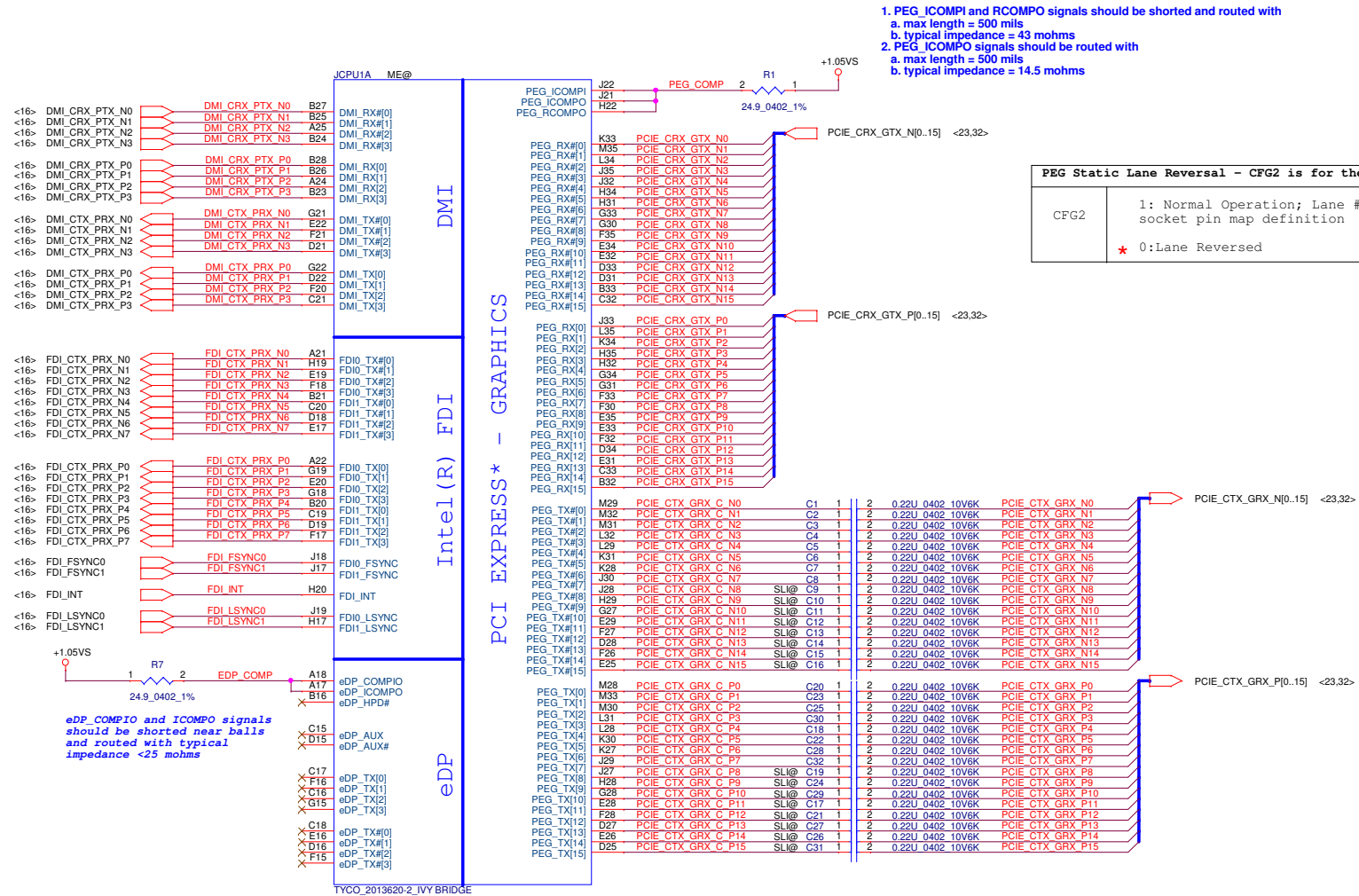


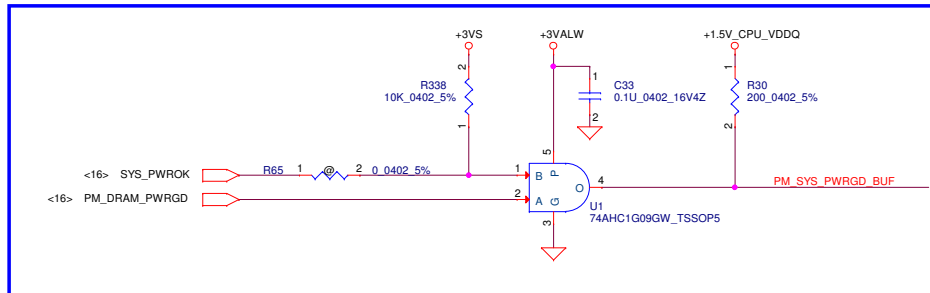
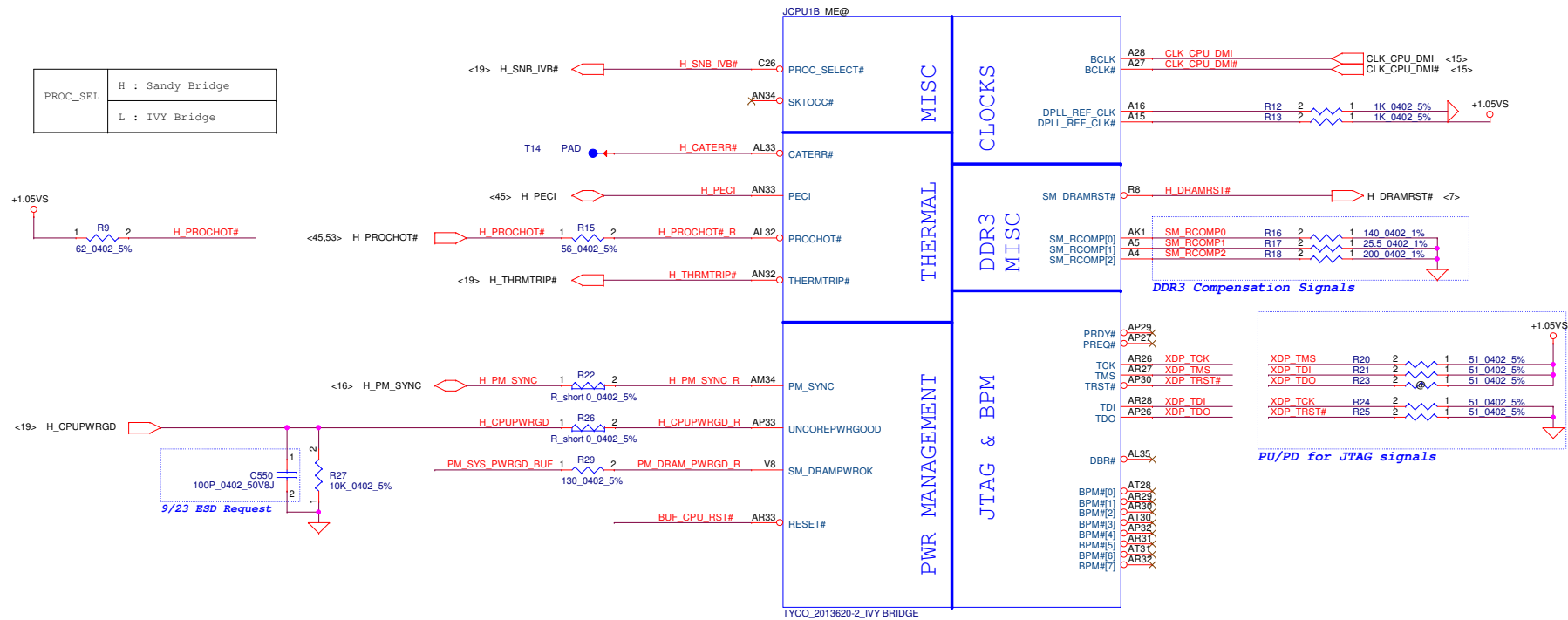
1. all power rail ramp up time should be larger than 40us



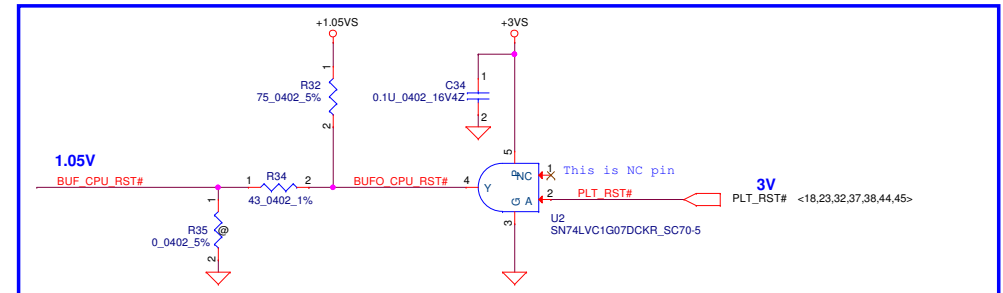
1. all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

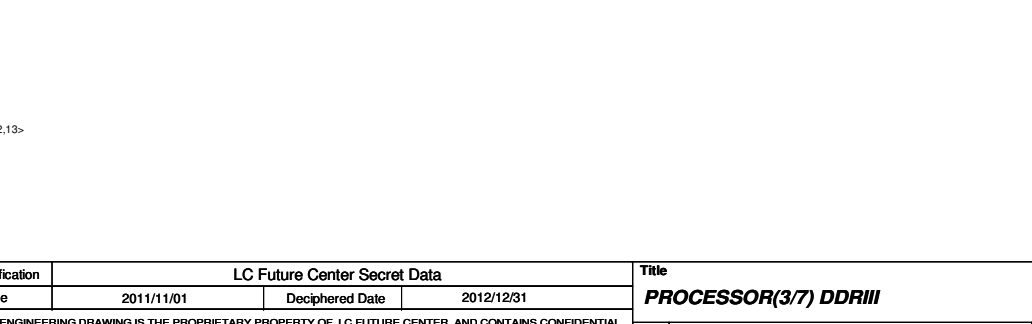
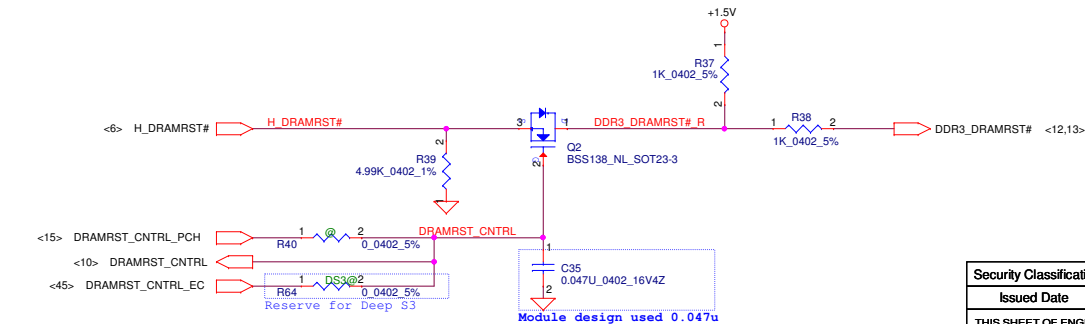
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Buffered Reset to CPU

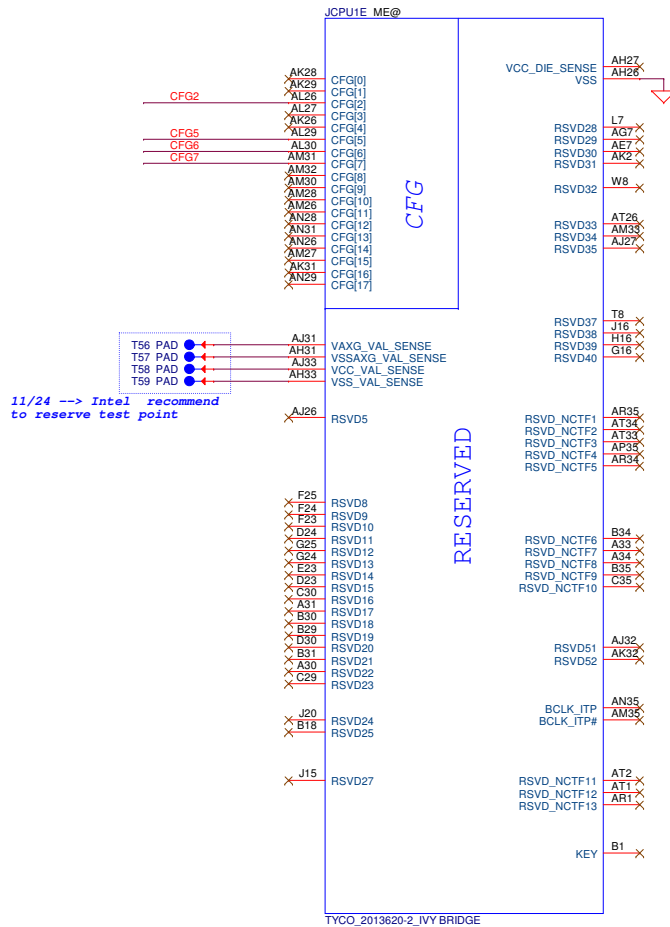


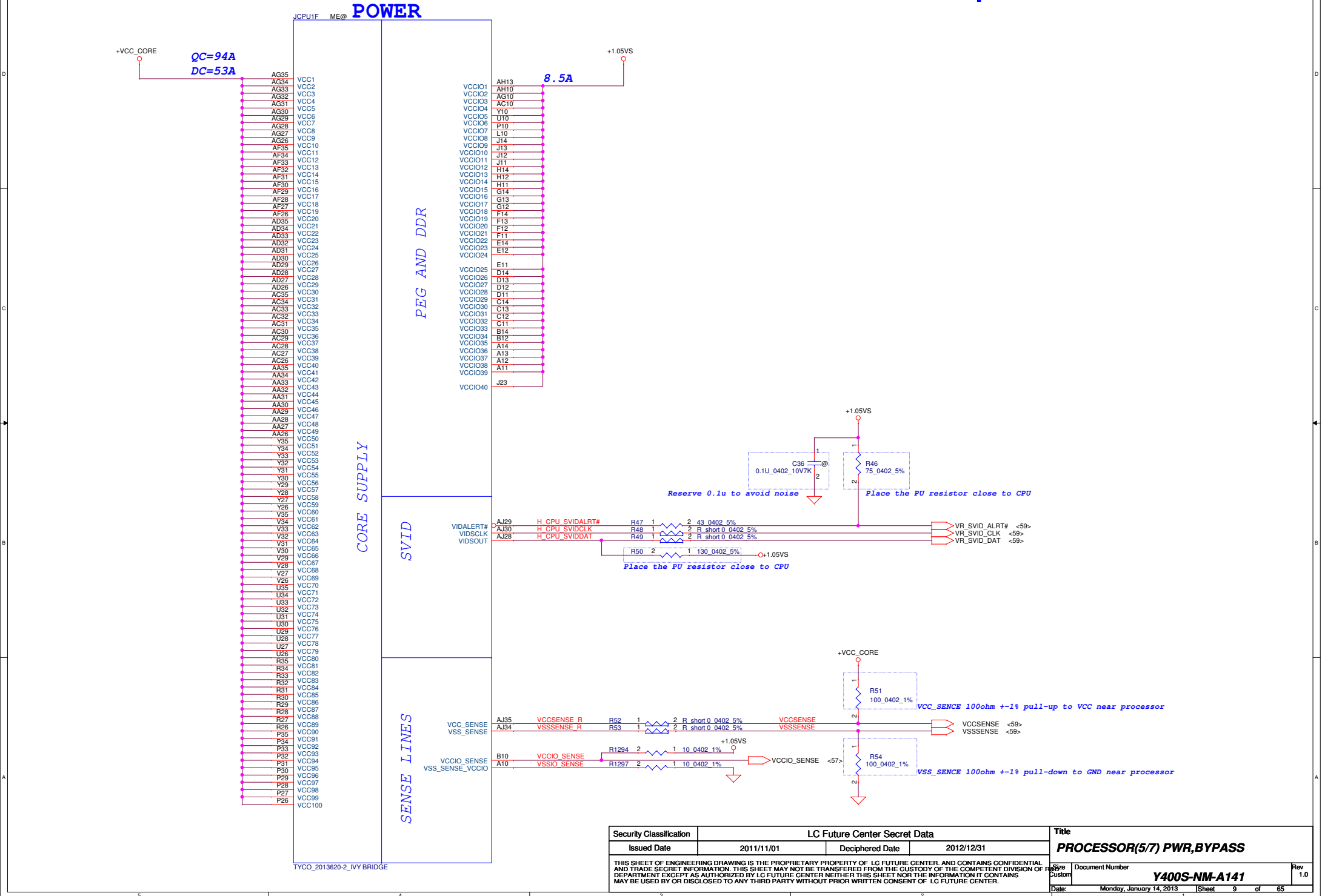


The drawing is a technical schematic of a DDR3 memory module, specifically the Y400S-NM-A141. It shows the internal circuitry, including the memory controller, memory array, and various support components like resistors, capacitors, and a diode. The module is labeled with various signals and components, including JCPU1C, JCPU1D, and JCPU1E. The drawing also includes a table with security information, including the title 'PROCESSOR(3/7) DDRIII', the document number 'Y400S-NM-A141', and the date 'Monday, January 14, 2013'.

Security Classification Table:

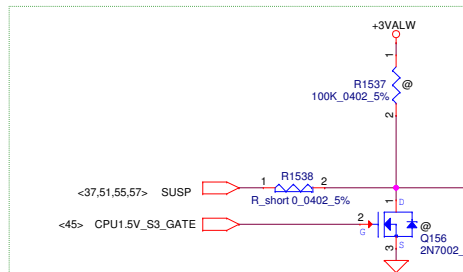
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+1.5V_CPU_VDDQ

For Deep S3



+VSB
R56 need to check on SDV

R56 100K_0402_5%

RUN_ON_CPU1.5VS3

R1349 470K_0402_5%

Q4A 2N7002KDWL_SOT363-6

Q156 2N7002_SOT23

R57 470K_0402_5%

C97 0.01U 50V K X7R 0603

Q4B 2N7002KDWL_SOT363-6

SUSP

POWER

GRAPHICS

1.8V RAIL

SENSE LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

MISC

AT24	VAXG1
AT23	VAXG2
AT21	VAXG3
AT18	VAXG4
AT17	VAXG5
AR24	VAXG6
AR23	VAXG7
AR21	VAXG8
AR20	VAXG9
AR18	VAXG10
AR17	VAXG11
AP24	VAXG12
AP23	VAXG13
AP21	VAXG14
AP20	VAXG15
AP18	VAXG16
AP17	VAXG17
AN24	VAXG18
AN23	VAXG19
AN21	VAXG20
AN20	VAXG21
AN18	VAXG22
AN17	VAXG23
AM24	VAXG24
AM23	VAXG25
AM21	VAXG26
AM20	VAXG27
AM18	VAXG28
AM17	VAXG29
AL24	VAXG30
AL23	VAXG31
AL21	VAXG32
AL20	VAXG33
AL18	VAXG34
AL17	VAXG35
AK24	VAXG36
AK23	VAXG37
AK21	VAXG38
AK20	VAXG39
AK18	VAXG40
AK17	VAXG41
AJ24	VAXG42
AJ23	VAXG43
AJ21	VAXG44
AJ20	VAXG45
AJ18	VAXG46
AJ17	VAXG47
AH24	VAXG48
AH23	VAXG49
AH21	VAXG50
AH20	VAXG51
AH18	VAXG52
AH17	VAXG53
AH16	VAXG54

VCCSA1	M27
VCCSA2	M26
VCCSA3	L26
VCCSA4	J26
VCCSA5	J25
VCCSA6	J24
VCCSA7	H25
VCCSA8	H25

VCCSA_SENSE	H23
VCCSA_VID[0]	C22
VCCSA_VID[1]	C24
VCCIO_SEL	A19

TYCO_2013620_2_IVY BRIDGE

ME@

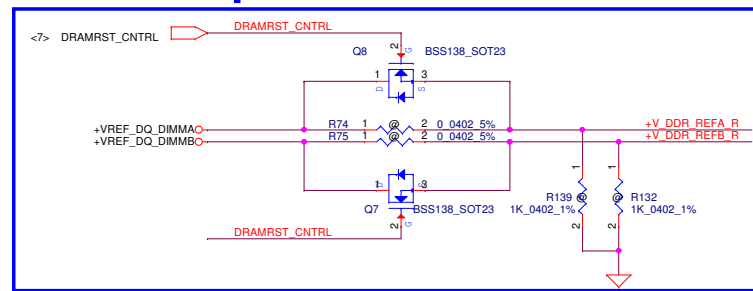
11/24 change 22U X2 to 330U B2 size

11/24 change 22U X2 to 330U B2 size

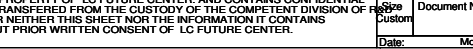
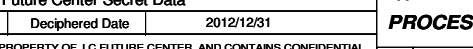
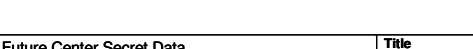
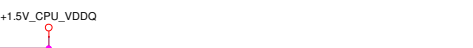
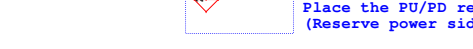
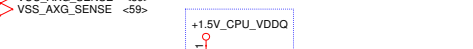
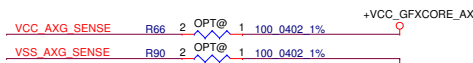
11/24 change 22U X2 to 330U B2 size

11/24 change 22U X2 to 330U B2 size

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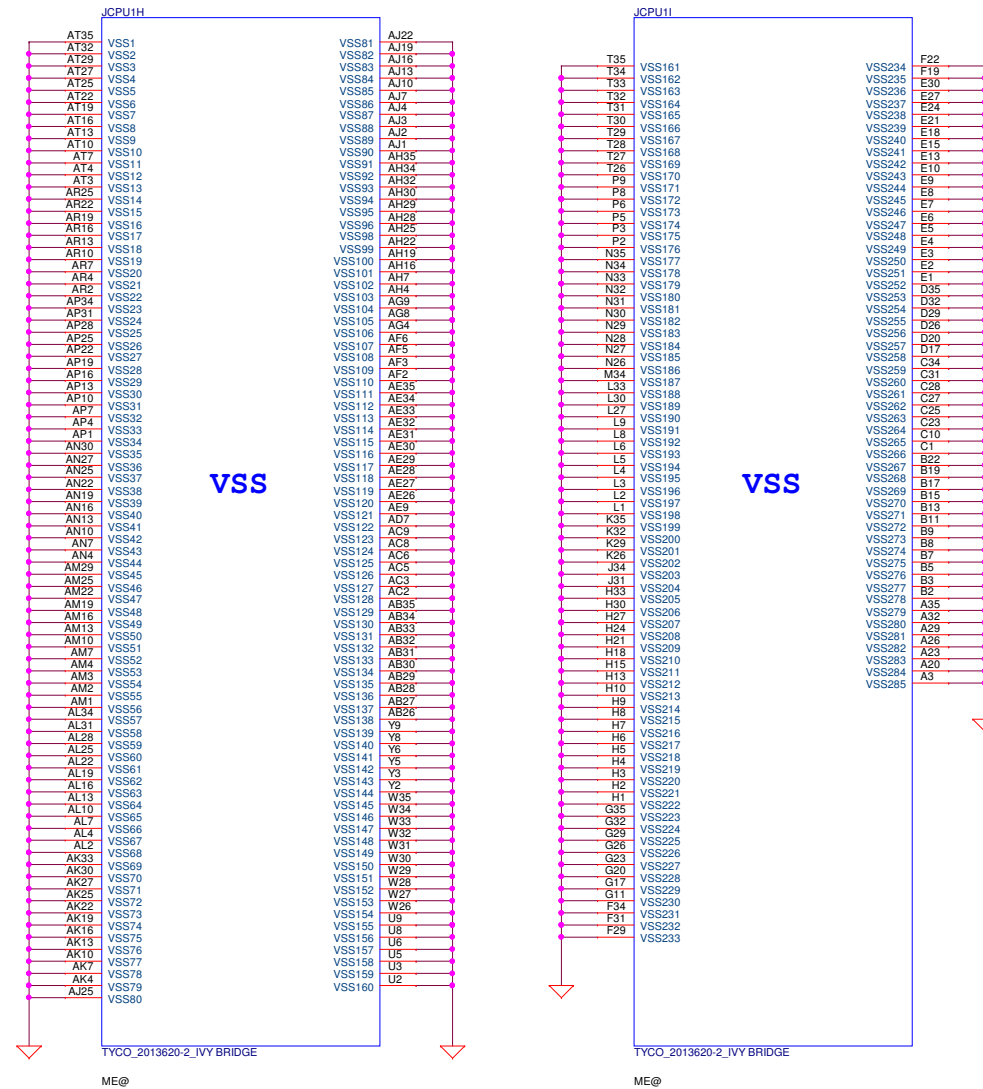


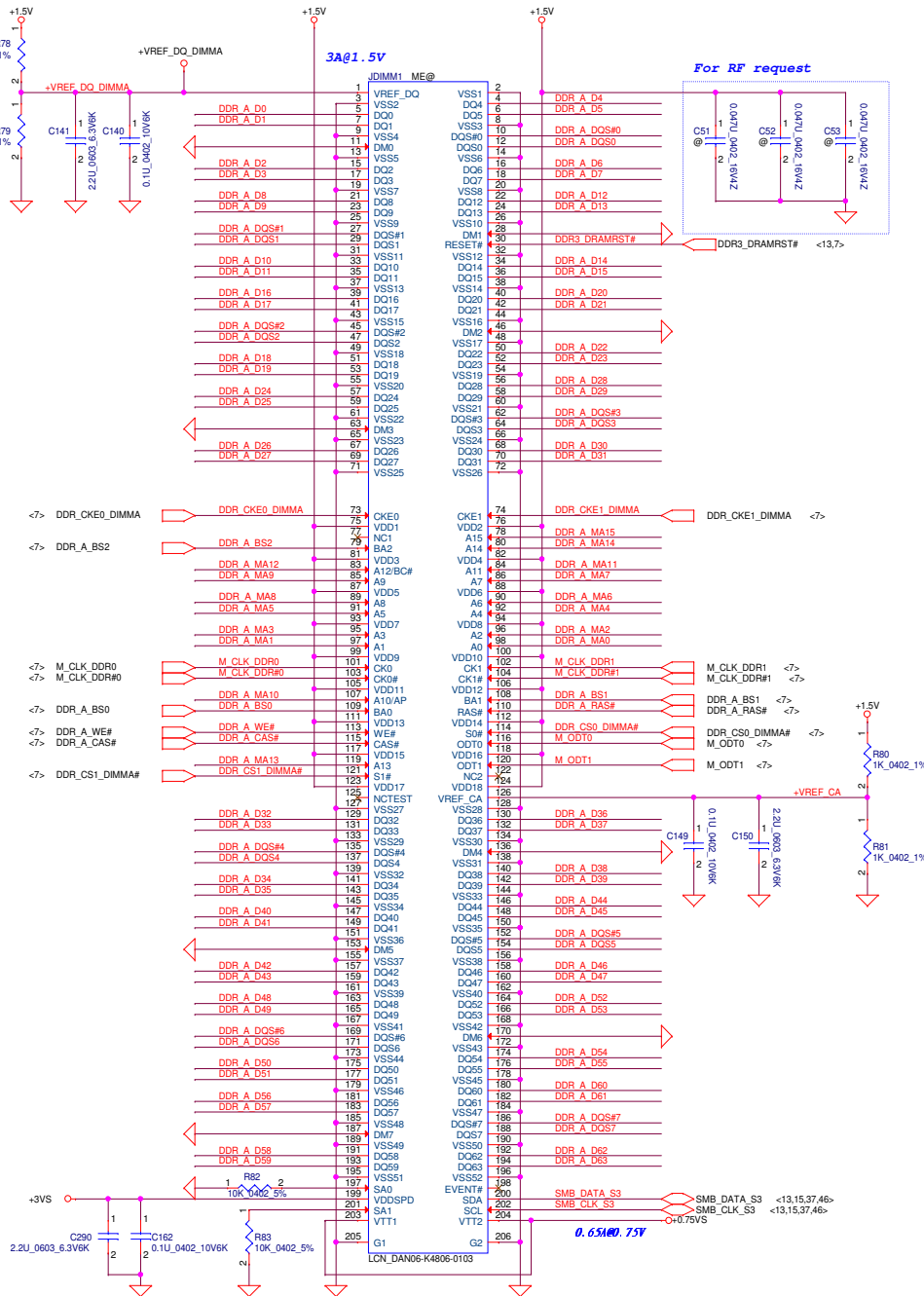
6/8: Add M3 Circuit (Processor Generated SO-DIMM VREF_DQ)



Place the PU/PD resistor close to CPU within 2 inch (Reserve power side)

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DDR_A_D[0..63] <7>

DDR_A_DQS[0..7] <7>

DDR_A_DQS# [0..7] <7>

DDR_A_MA[0..15] <7>

Layout Note:
Place near DIMM

OSCON (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM

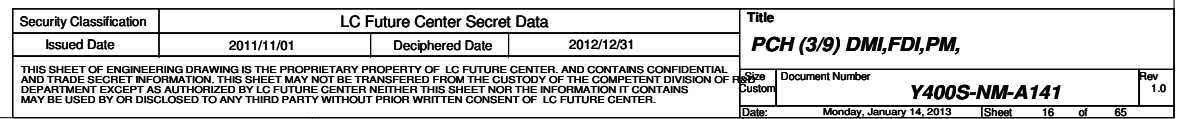
Layout Note:
Place near DIMM

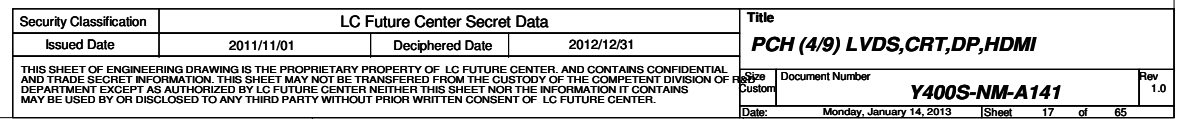
DDR_DM[0:7] connect to GND

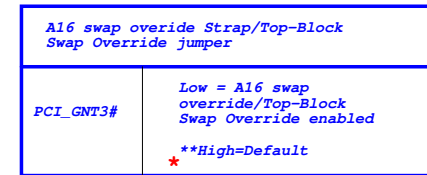
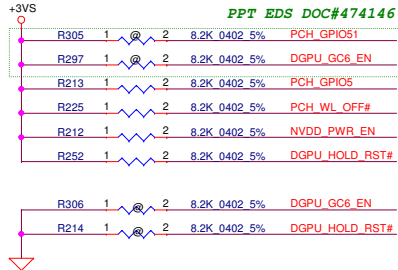
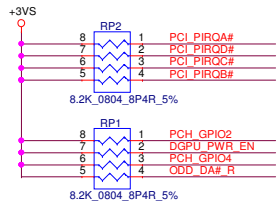
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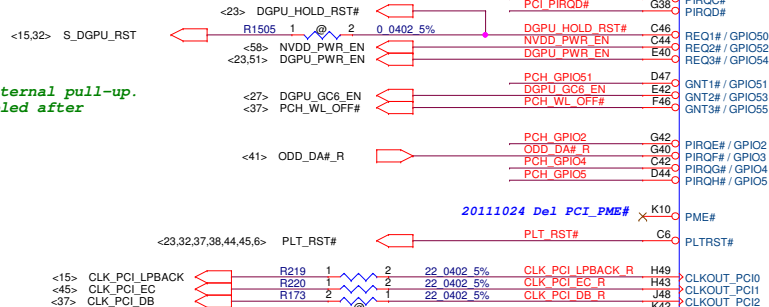
DDR_B_DM[0:7] connect to GND





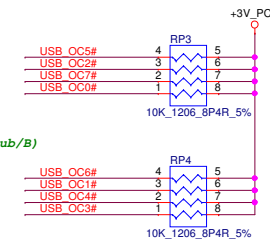
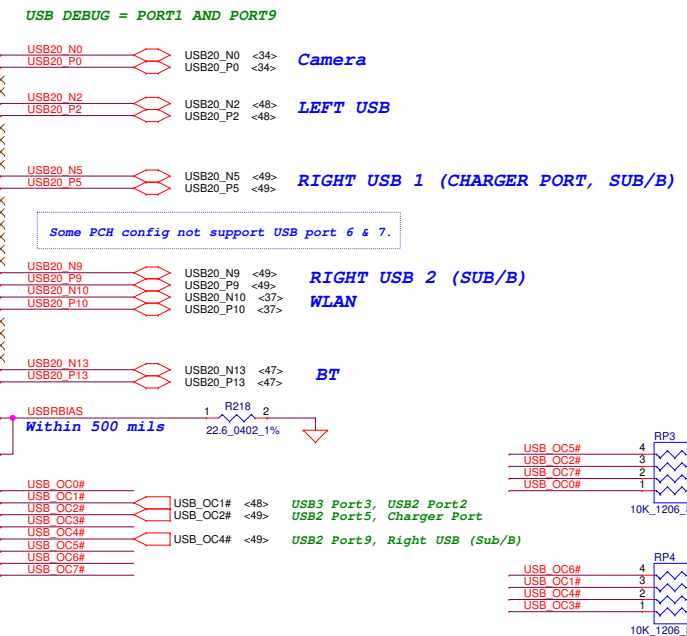
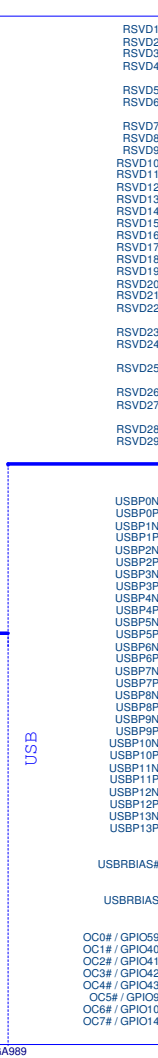
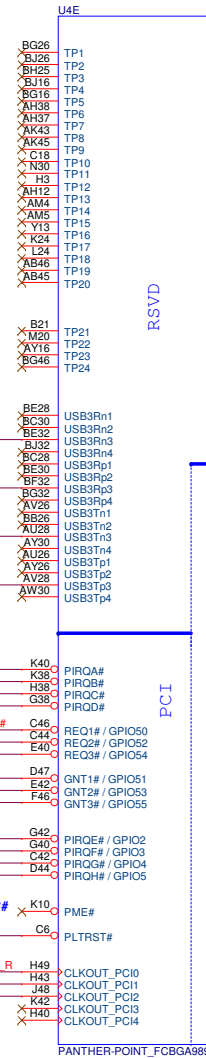
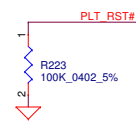
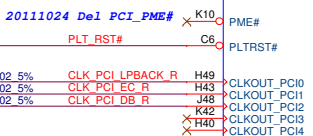
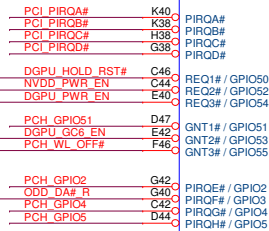
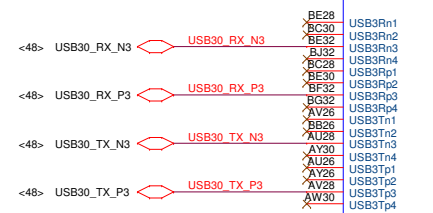


GPI053 => This Signal has a weak internal pull-up.
NOTE: The internal pull-up is disabled after PLTRST# deasserts.



Boot BIOS Strap bit1 BBS1		
	Bit11	Bit10
	Destination	
GNT1# / GPI051	0	1
	1	0
	1	1
	0	0
	Reserved	
	Reserved	
	★ SPI (Default)	
	LPC	

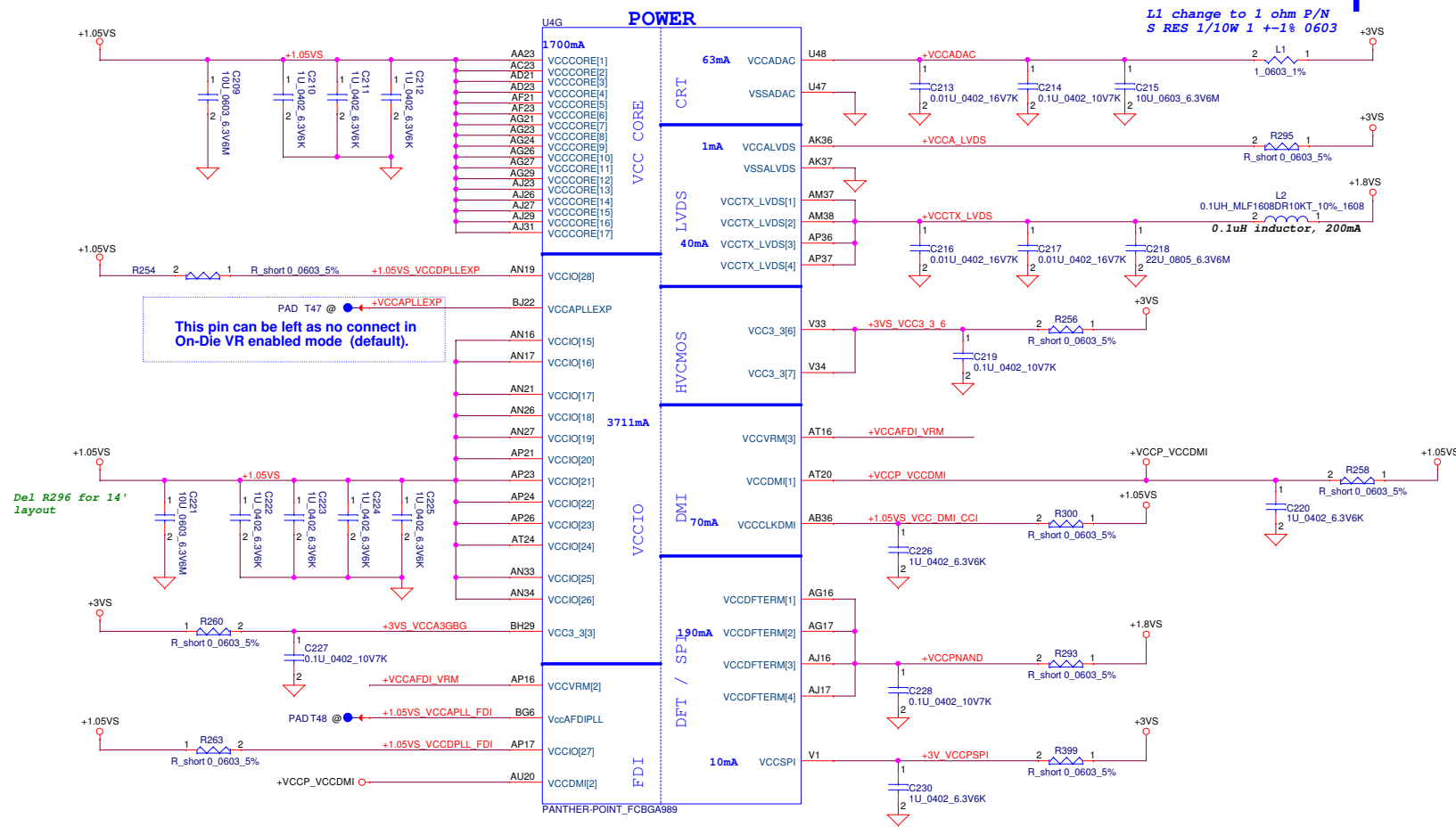
USB3.0	
Port1	
Port2	
Port3	LEFT USB
Port4	



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Issued Date	2011/11/01	Deciphered Date	2012/12/31	PCH (5/9) PCI, USB	
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				Custom	Y400S-NM-A141
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				Rev	1.0

Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
Optimus	0	0	X
Reserve	0	1	X
DIS (SLI)	1	0	X
Reserve	1	1	X
14"	X	X	0
15"	X	X	1

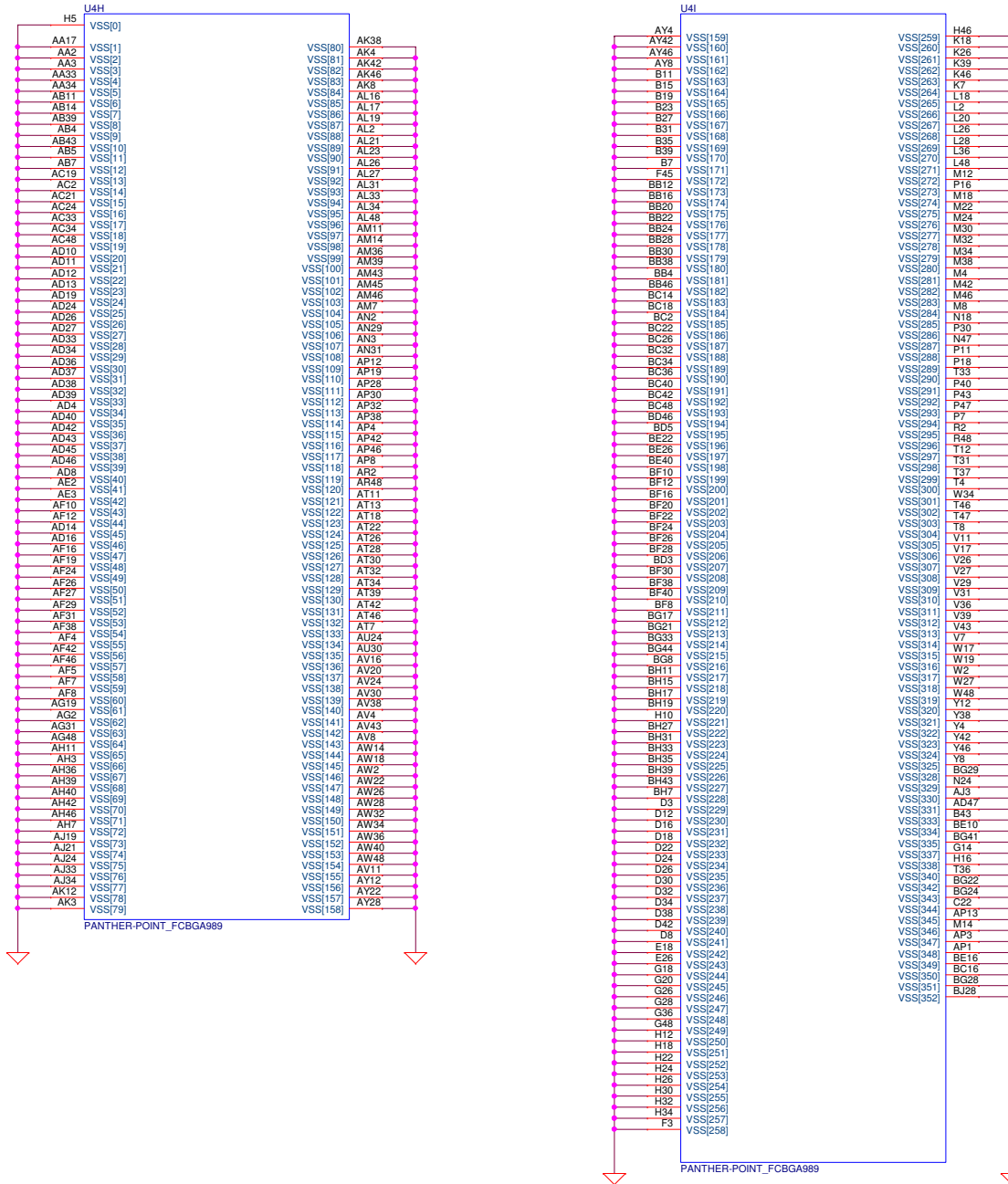




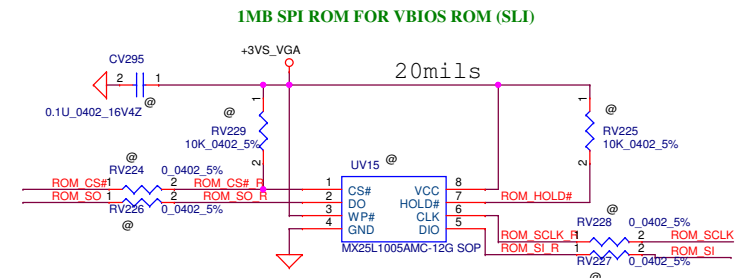
PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKLN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Intel recommend VCCVRM==>1.5V FOR MOBILE
stuff R265 and unstuff R266 VCCVRM==>1.8V FOR DESKTOP

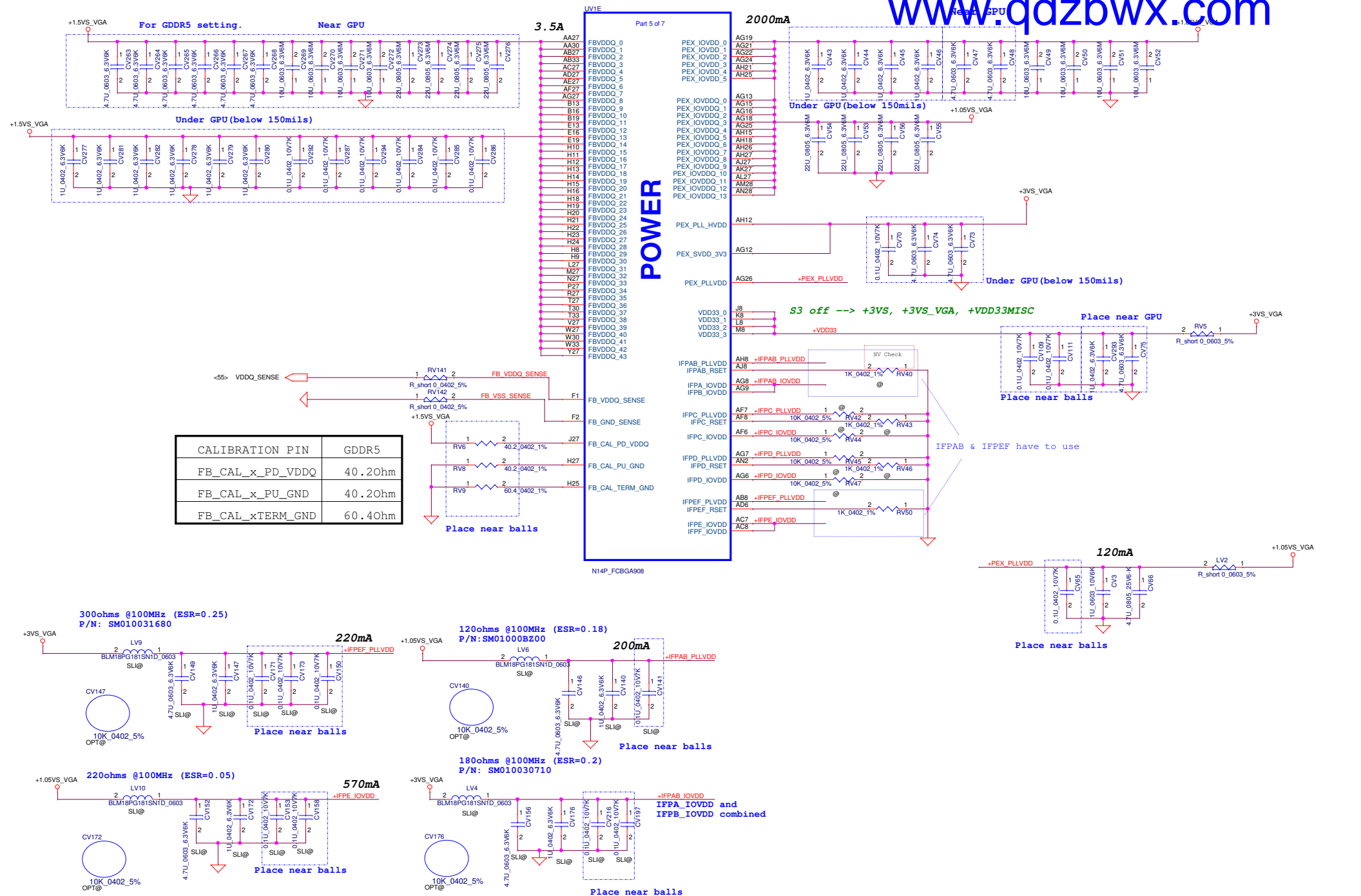
VCCVRM = 160mA detal waiting for newest spec

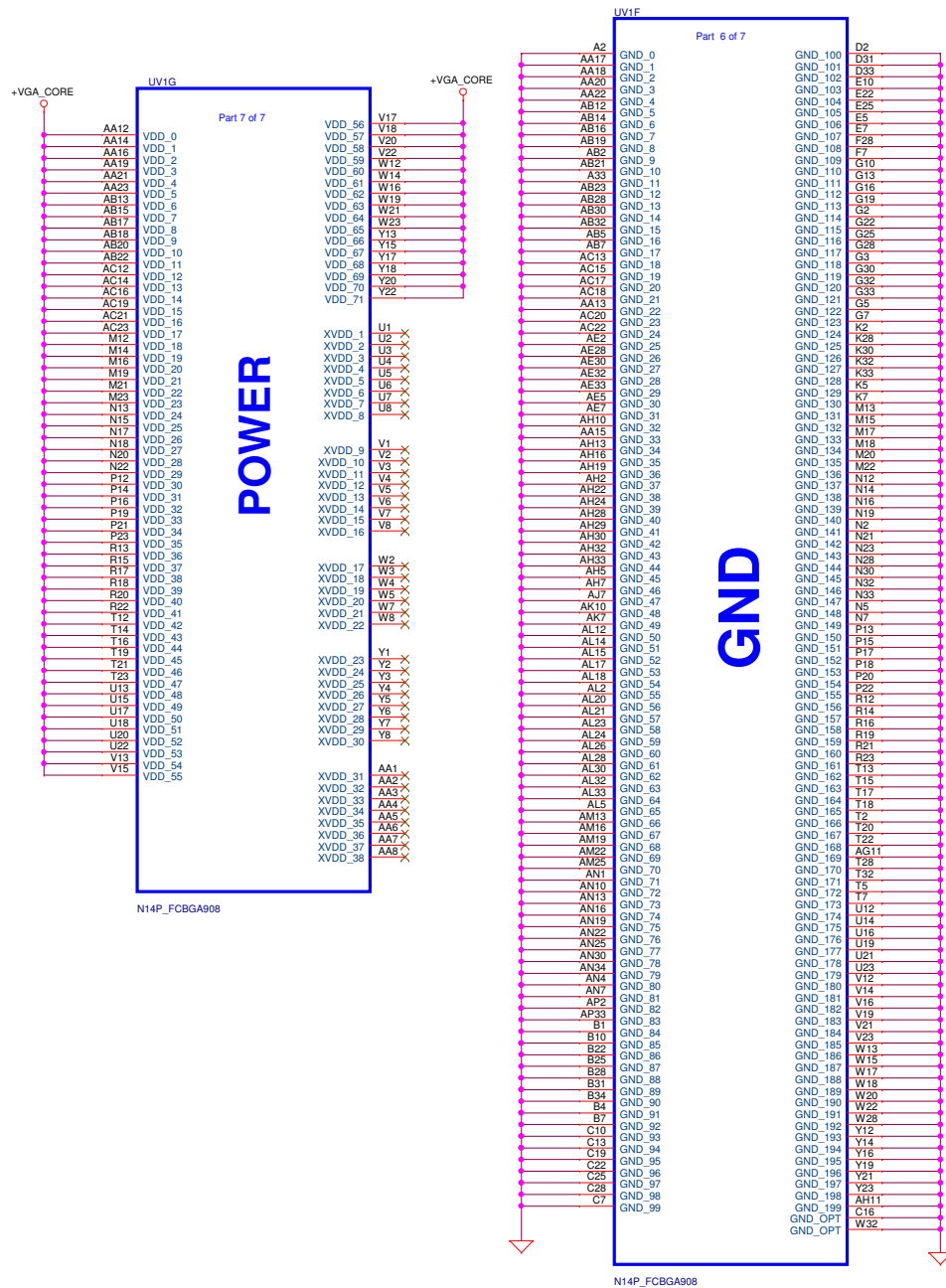




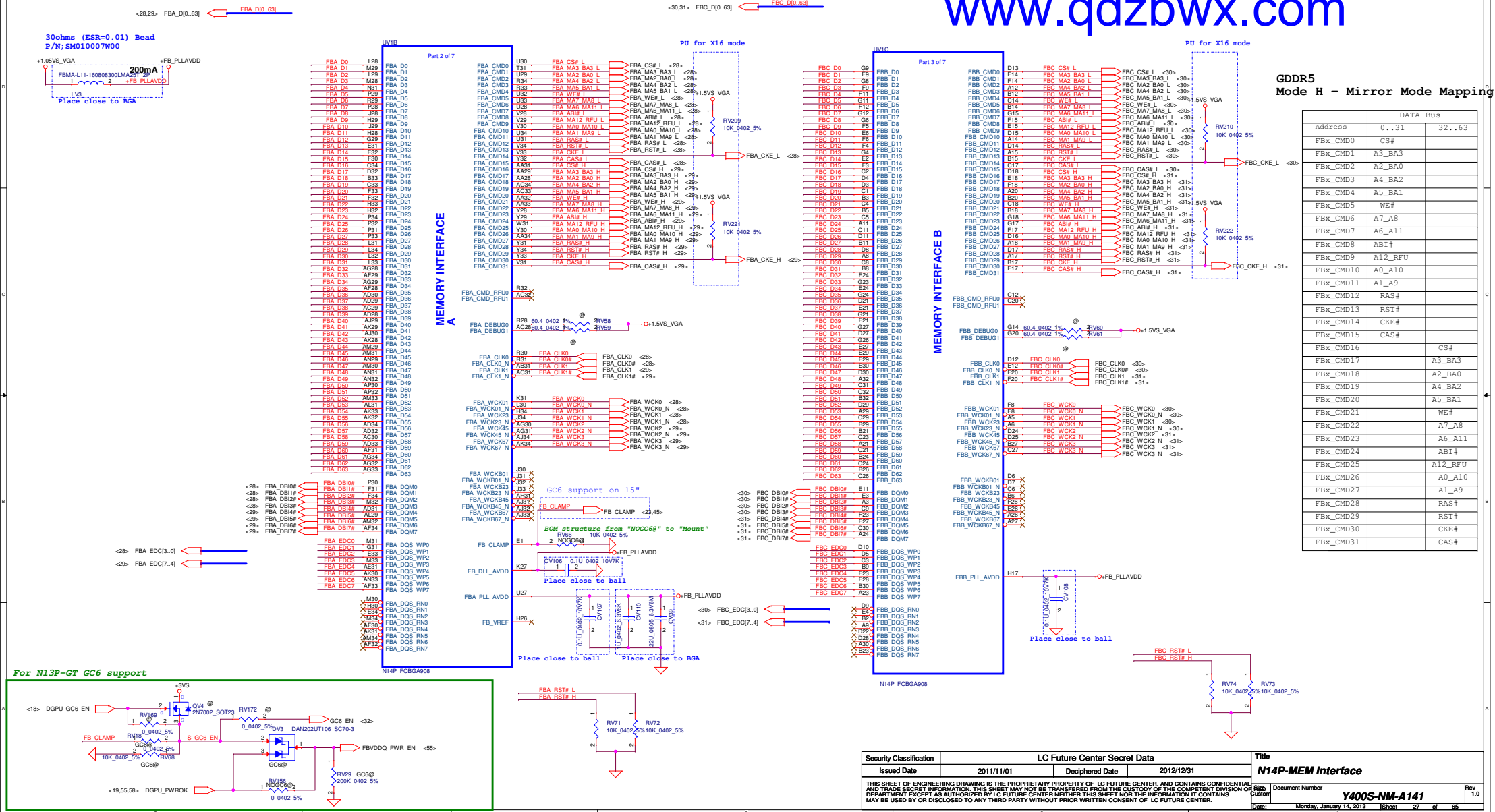


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				Rev 1.0	

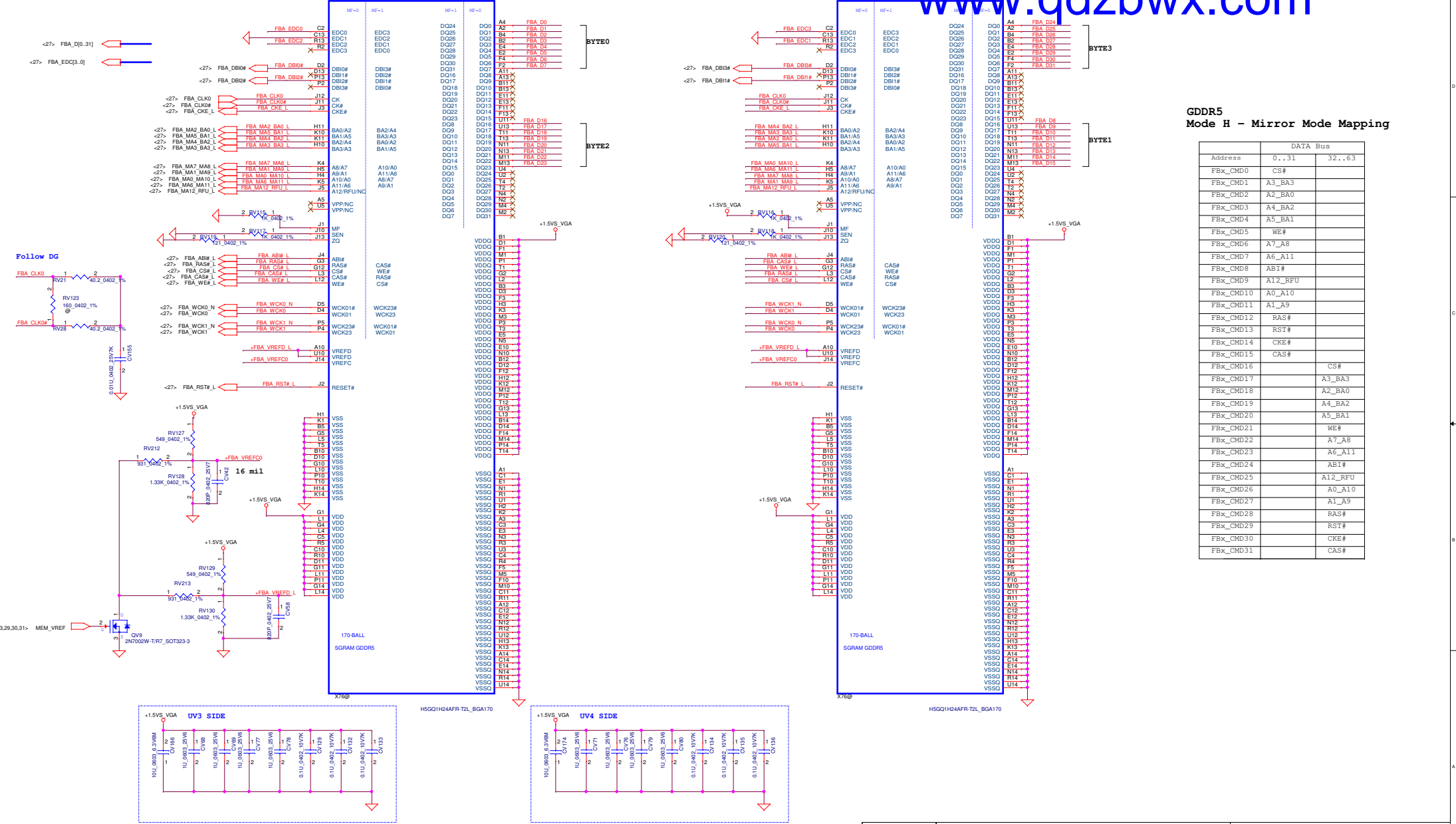




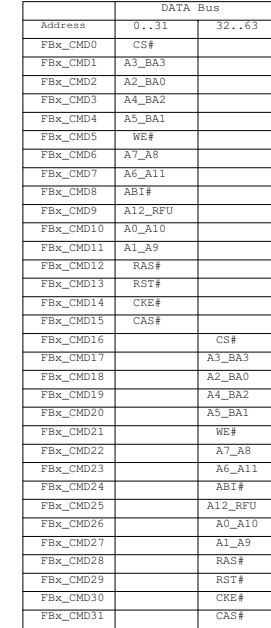
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	N14P-VGA CORE, GND
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	Y400S-NM-A141		1.0	
Date:	Monday, January 14, 2013	Sheet	26	of 65



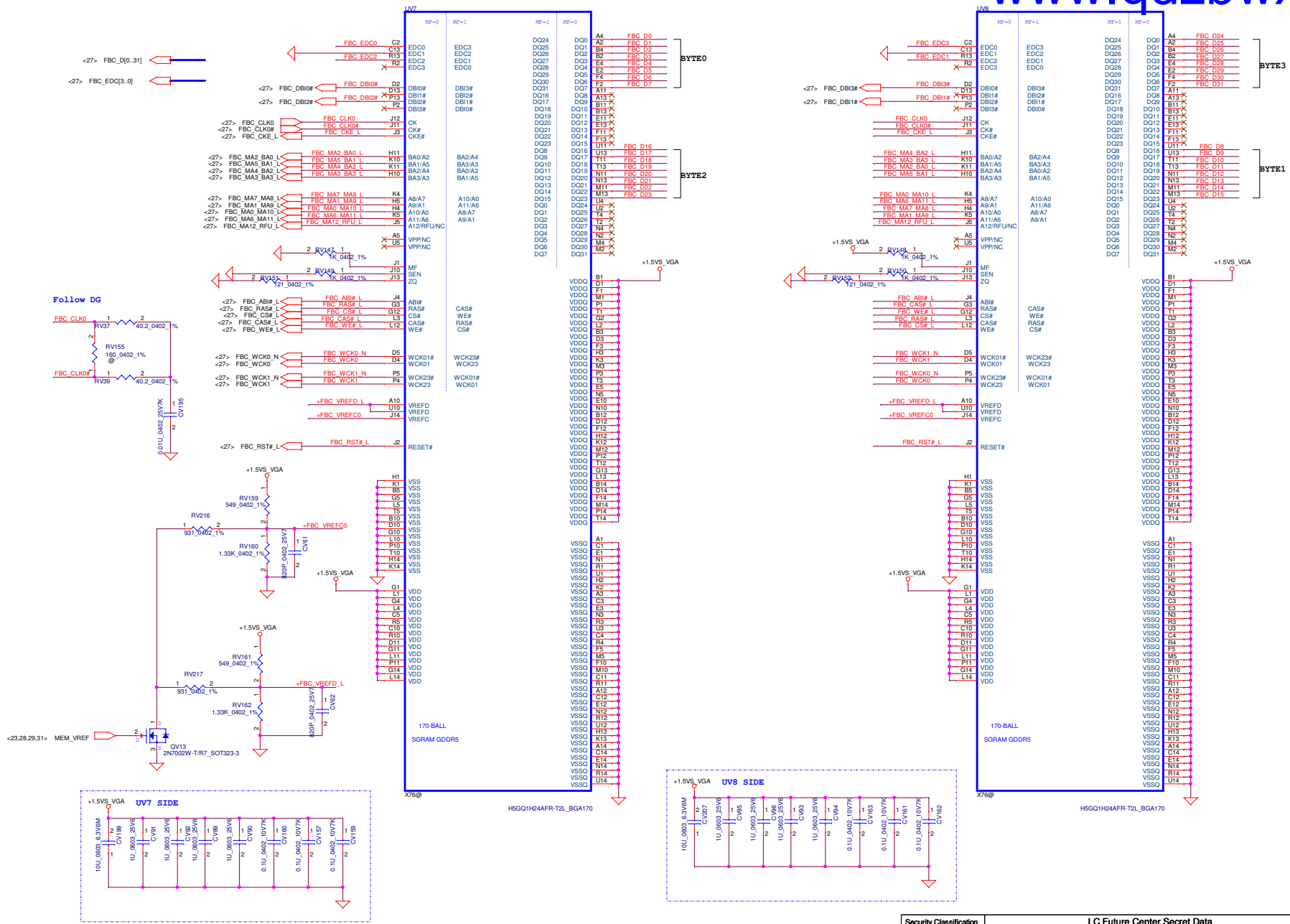
Memory - Lower 32 bits



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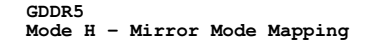
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Issued Date		2011/11/01	Deciphered Date	2012/12/31	N14P-VRAM A Upper
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GDDR5 Mode H - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	AB1#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		AB1#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

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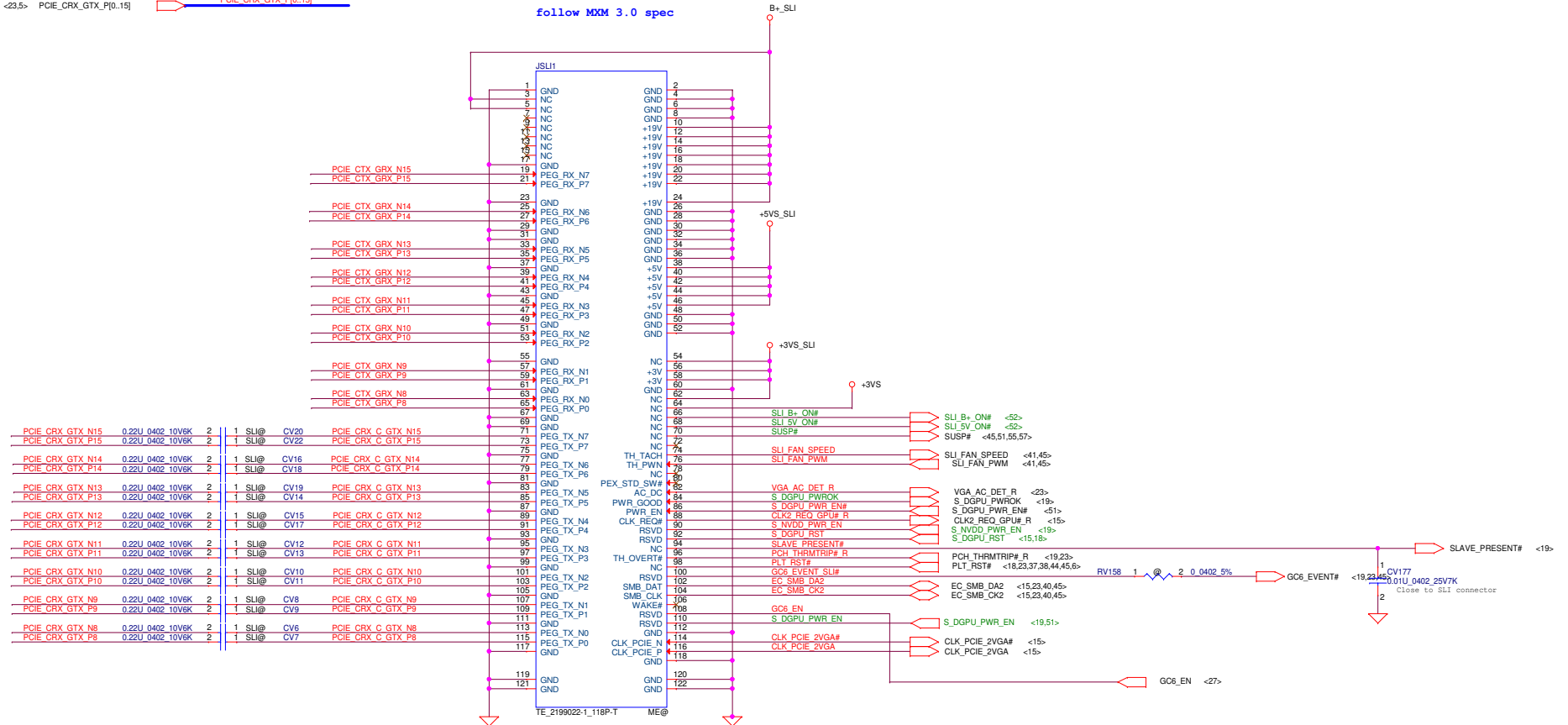
	DATA Bus	
Address	0..31	32..63
FbX_CMD0	CS#	
FbX_CMD1	A3_BA3	
FbX_CMD2	A2_BA0	
FbX_CMD3	A4_BA2	
FbX_CMD4	A5_BA1	
FbX_CMD5	WE#	
FbX_CMD6	A7_A8	
FbX_CMD7	A6_A11	
FbX_CMD8	AB1#	
FbX_CMD9	A12_RFU	
FbX_CMD10	A0_A10	
FbX_CMD11	A1_A9	
FbX_CMD12	RAS#	
FbX_CMD13	RST#	
FbX_CMD14	CKE#	
FbX_CMD15	CAS#	
FbX_CMD16		CS#
FbX_CMD17	A3_BA3	
FbX_CMD18	A2_BA0	
FbX_CMD19	A4_BA2	
FbX_CMD20	A5_BA1	
FbX_CMD21	WE#	
FbX_CMD22	A7_A8	
FbX_CMD23	A6_A11	
FbX_CMD24	AB1#	
FbX_CMD25	A12_RFU	
FbX_CMD26	A0_A10	
FbX_CMD27	A1_A9	
FbX_CMD28	RAS#	
FbX_CMD29	RST#	
FbX_CMD30	CKE#	
FbX_CMD31	CAS#	


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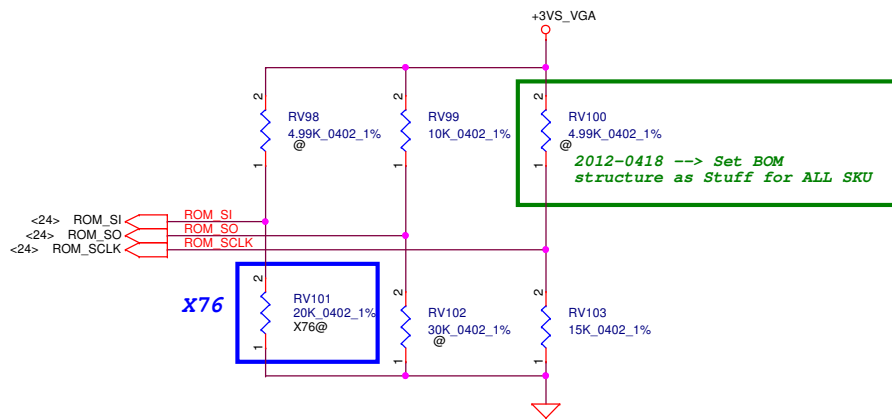
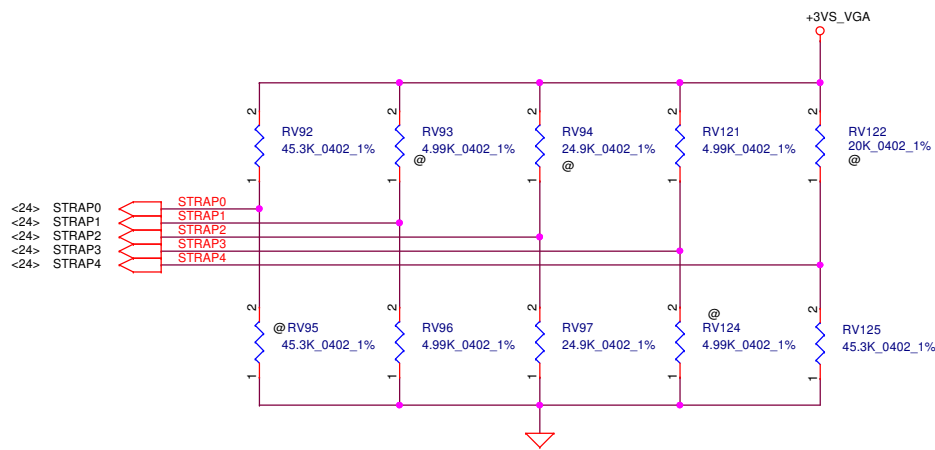
11/11 for 2nd VGA fan
need to notice EC

<23.5> PCIE_CTX_GRX_N[0..15]
<23.5> PCIE_CTX_GRX_P[0..15]
<23.5> PCIE_CRX_GTX_N[0..15]
<23.5> PCIE_CRX_GTX_P[0..15]

PCIE_CTX_GRX_N[0..15]
PCIE_CTX_GRX_P[0..15]
PCIE_CRX_GTX_N[0..15]
PCIE_CRX_GTX_P[0..15]



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2011/11/01		2012/12/31			
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Custom	Y400S-NM-A141			1.0	
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X76

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GT1 28nm	Samsung	K4G20325FD-FC04 2G 64Mx32	PD 30K	PU 10K	PU 35K (ALL SKU)	PU 45K	PD 5K	PD 25K	PU 5K	PD 45K
		K4G10325FG-HC04 1G 32Mx32	PD 45K							
	Hynix	H5GQ2H24MFR-T2C 2G 64Mx32	PD 25K							
		H5GQ1H24BFR-T2C 1G 32Mx32	PD 20K							
		H5GQ2H24AFR-T2C 2G 64Mx32	PD 5K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01 (2G 64Mx32)	SA00005B70J
	X76409JVL51 (1G 32Mx16)	SA00003RS0J
Hynix	X76409JVL02 (2G 64Mx32)	SA00004GD0J EOL
	X76409JVL02 (2G 64Mx32)	SA00004GD1J
	X76409JVL52 (1G 32Mx16)	SA00003WL1J

Physical Strapping pin	Power Rail	Physical Strapping Bit	Logical Strapping Bit	Logical Strapping Bit	Logical Strapping Bit
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0000	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

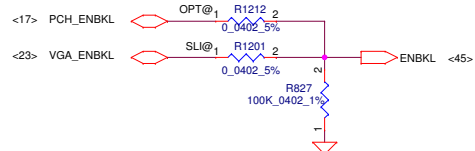
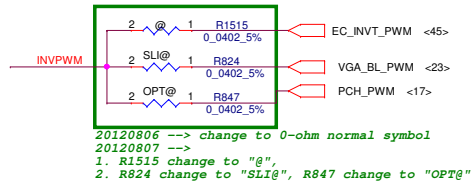
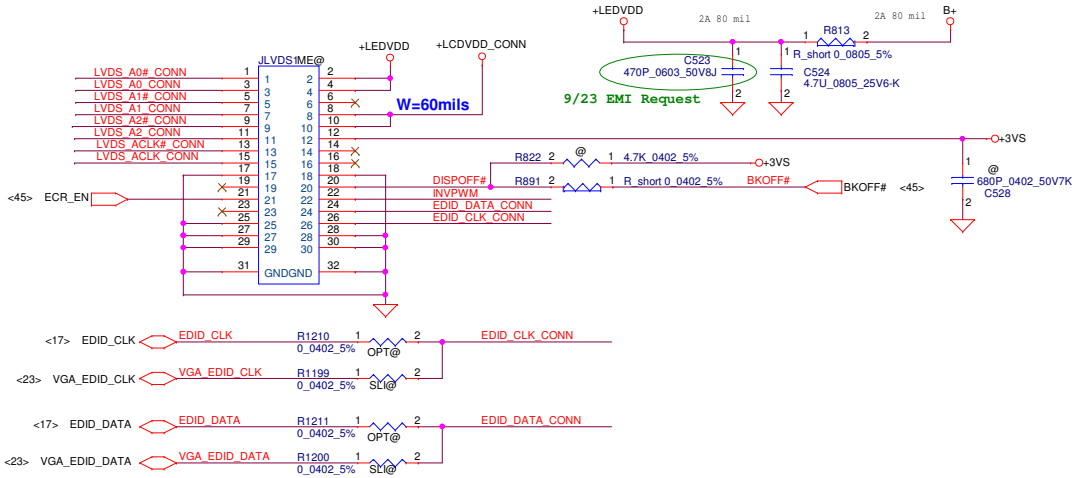
PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

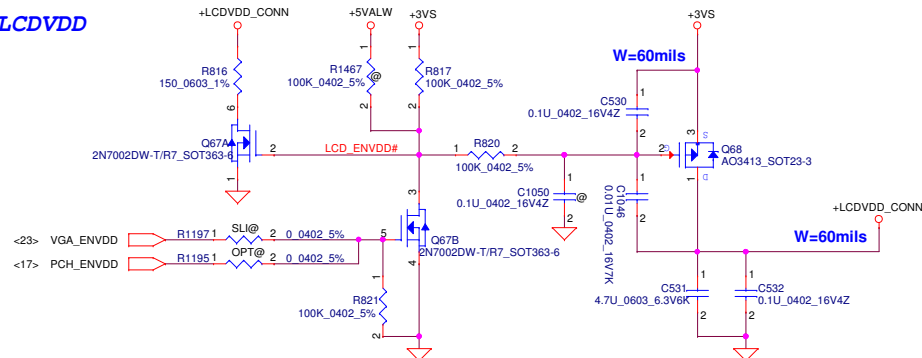


PCH

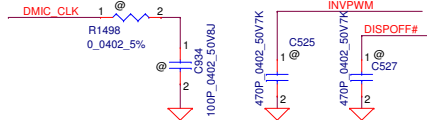
VGA

<17>	LVDS_ACLK#	LVDS_ACLK#	R1255	1	OPT@	2	0.0402_5%	LVDS_ACLK#_CONN
<17>	LVDS_ACLK	LVDS_ACLK	R1257	1	OPT@	2	0.0402_5%	LVDS_ACLK#_CONN
<17>	LVDS_A0#	LVDS_A0#	R1259	1	OPT@	2	0.0402_5%	LVDS_A0#_CONN
<17>	LVDS_A0	LVDS_A0	R1261	1	OPT@	2	0.0402_5%	LVDS_A0#_CONN
<17>	LVDS_A1#	LVDS_A1#	R1262	1	OPT@	2	0.0402_5%	LVDS_A1#_CONN
<17>	LVDS_A1	LVDS_A1	R1265	1	OPT@	2	0.0402_5%	LVDS_A1#_CONN
<17>	LVDS_A2#	LVDS_A2#	R1267	1	OPT@	2	0.0402_5%	LVDS_A2#_CONN
<17>	LVDS_A2	LVDS_A2	R1269	1	OPT@	2	0.0402_5%	LVDS_A2#_CONN
<24>	VGA_TXCLK-	VGA_TXCLK-	R1260	1	SLI@	2	0.0402_5%	LVDS_ACLK#_CONN
<24>	VGA_TXCLK+	VGA_TXCLK+	R1264	1	SLI@	2	0.0402_5%	LVDS_ACLK#_CONN
<24>	VGA_TXOUT0-	VGA_TXOUT0-	R1263	1	SLI@	2	0.0402_5%	LVDS_A0#_CONN
<24>	VGA_TXOUT0+	VGA_TXOUT0+	R1266	1	SLI@	2	0.0402_5%	LVDS_A0#_CONN
<24>	VGA_TXOUT1-	VGA_TXOUT1-	R1268	1	SLI@	2	0.0402_5%	LVDS_A1#_CONN
<24>	VGA_TXOUT1+	VGA_TXOUT1+	R1270	1	SLI@	2	0.0402_5%	LVDS_A1#_CONN
<24>	VGA_TXOUT2-	VGA_TXOUT2-	R1271	1	SLI@	2	0.0402_5%	LVDS_A2#_CONN
<24>	VGA_TXOUT2+	VGA_TXOUT2+	R1272	1	SLI@	2	0.0402_5%	LVDS_A2#_CONN

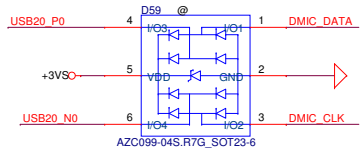
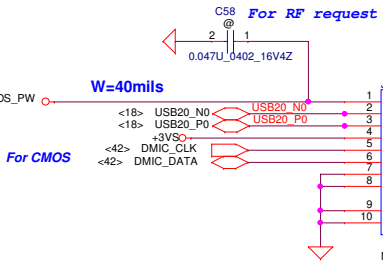
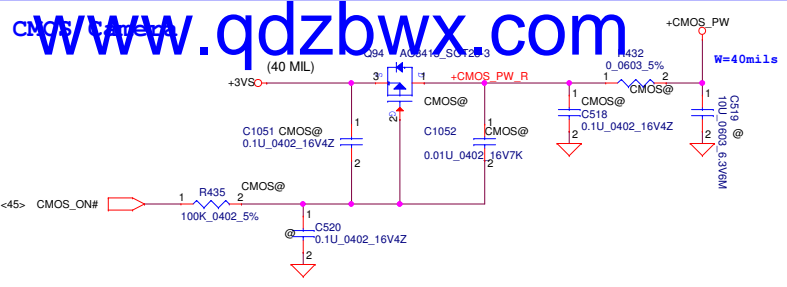
LCDVDD




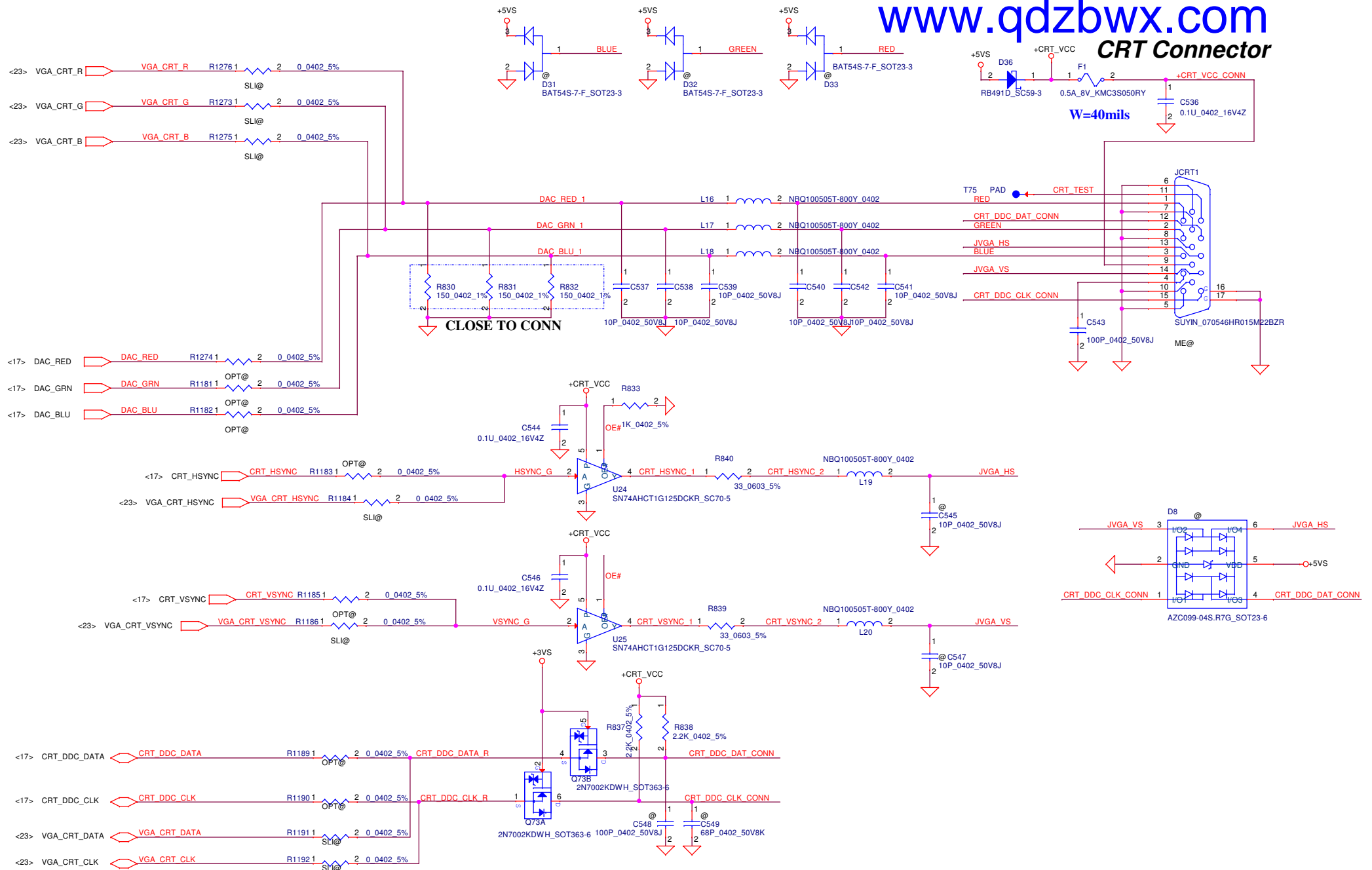
EMI request




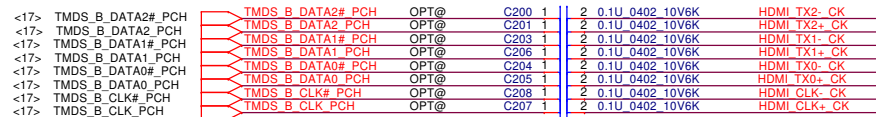
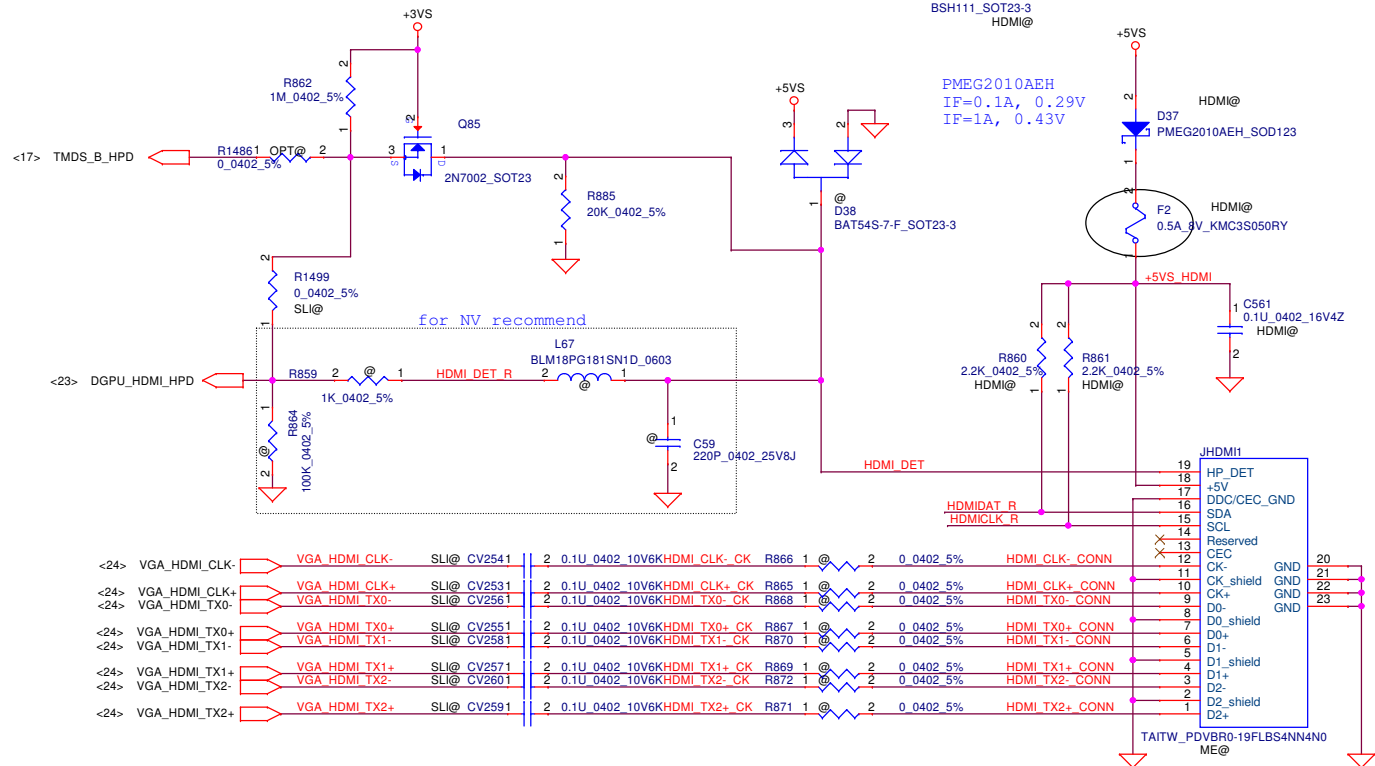
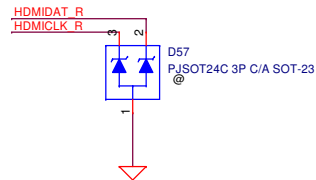
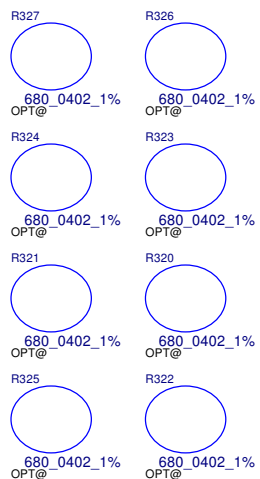
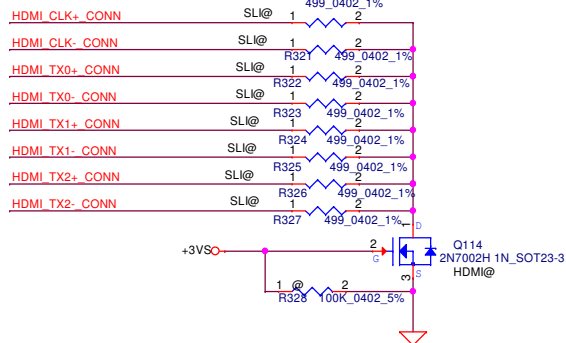
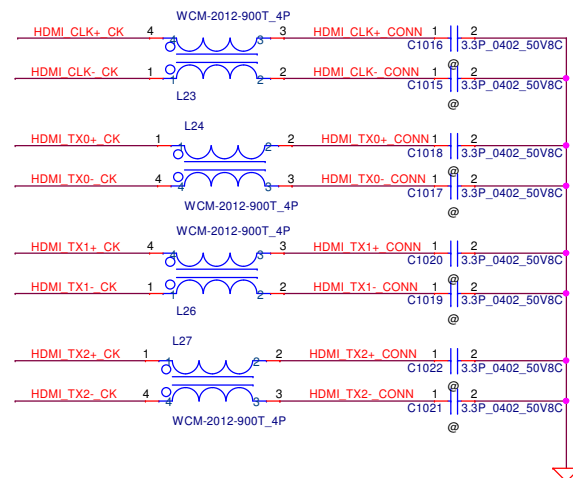
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				Document Number	1.0	
				Y400S-NM-A141		
				Date: Monday, January 14, 2013	Sheet 34 of 65	



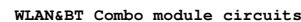
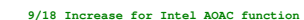
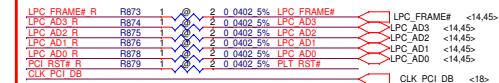
Security Classification		LC Future Center Secret Data		Title			
Issued Date	2011/11/01	Deciphered Date	2012/12/31	CRT CONN.			
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				Date: Monday, January 14, 2013		Sheet 35 of 65	



HDMI W/O Logo: R00000001HM

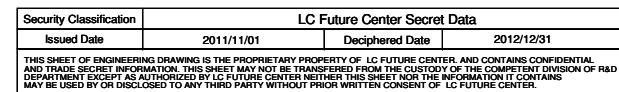
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2011/11/01	Deciphered Date	2012/12/31	HDMI CONN.		
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				Date:	Monday, March 11, 2013	Sheet 36 of 65 Rev 1.0

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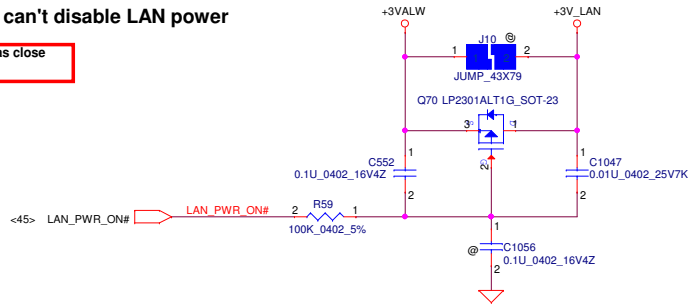
	BT on module Enable	BT on module Disable
★ BT_CTRL (GPIO22)	H	L
PCH_BT_ON#	L	H

SSD Active:4.5W(1.5A)

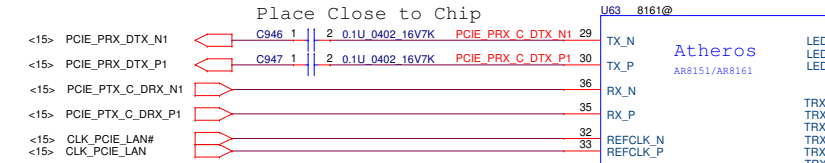
Rev
1.0

Atheros request can't disable LAN power

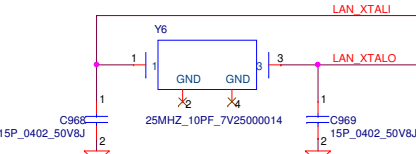
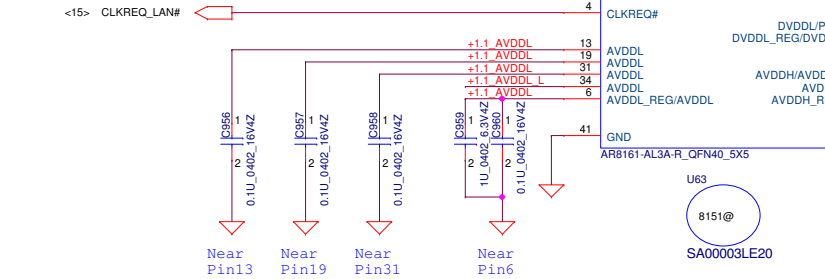
Layout Notice : Place as close chip as possible.



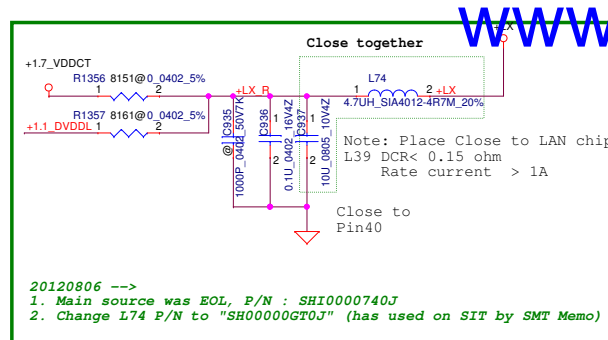
Vendor recommend reseve the PU resistor close LAN chip



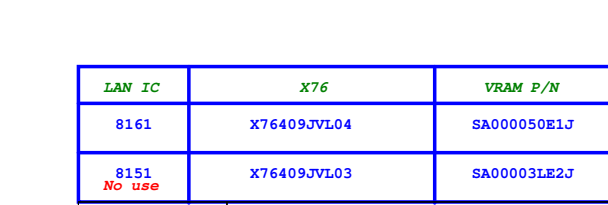
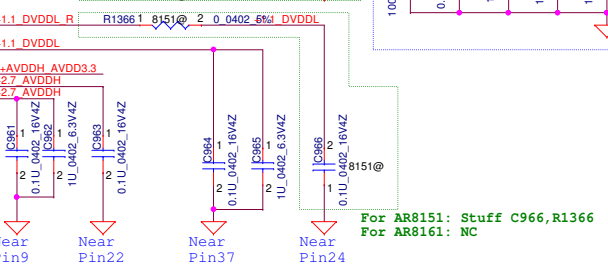
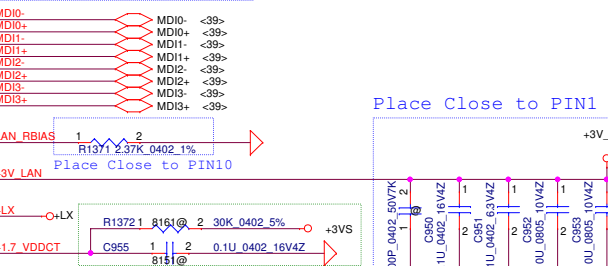
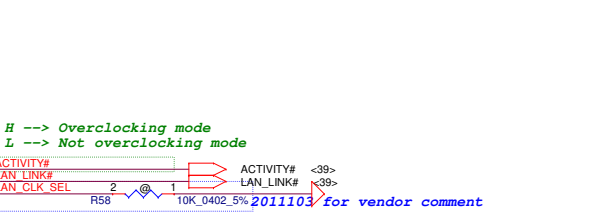
20120718 --> for LAN wakeup backlight issue
1. R1369 to "Mount"
2. R1370 to "g"



20120816 -->
1. change P/N to 7V2500014(10pf), SJ10000E80J

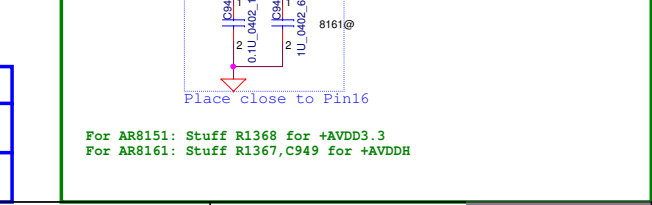
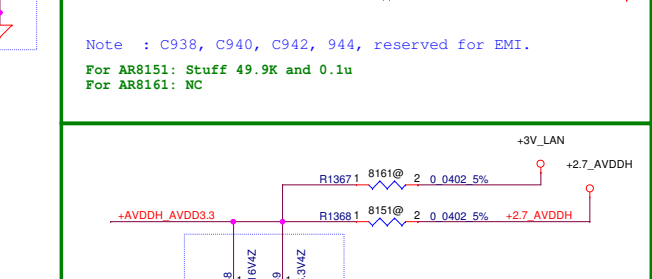
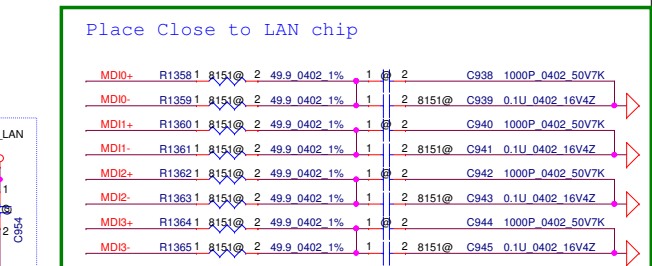
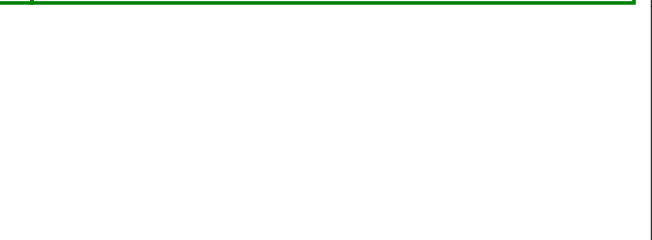
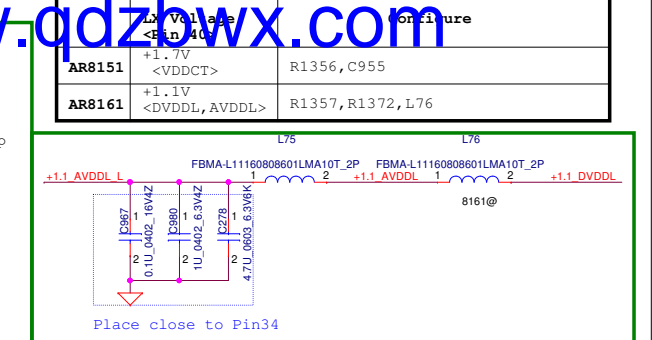


20120806 -->
1. Main source was EOL, P/N : SH10000740J
2. Change L74 P/N to "SH00000GT0J" (has used on SIT by SMT Memo)



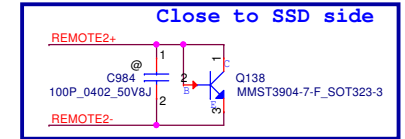
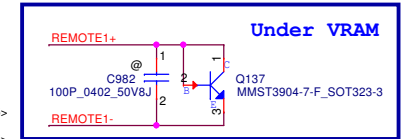
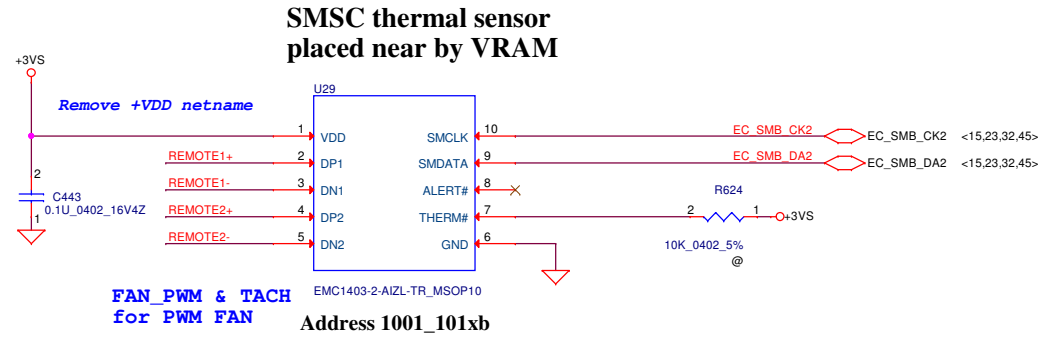
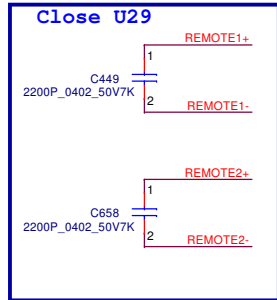
LAN IC	X76	VRAM P/N
8161	X76409JVL04	SA000050E1J
8151 No use	X76409JVL03	SA00003LE2J

Security Classification	LC Future Center Secret Data	
Issued Date	2011/11/01	Deciphered Date
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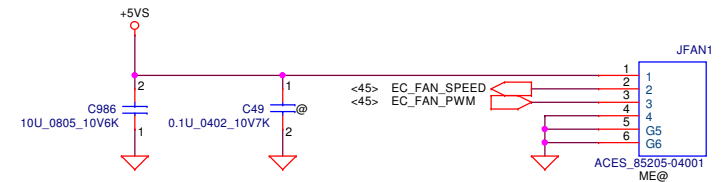
Security Classification	LC Future Center Secret Data	
Issued Date	2011/11/01	Deciphered Date
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LAN AR8151/8161	Document Number	Rev
Y400S-NM-A141	Monday, March 11, 2013	1.0

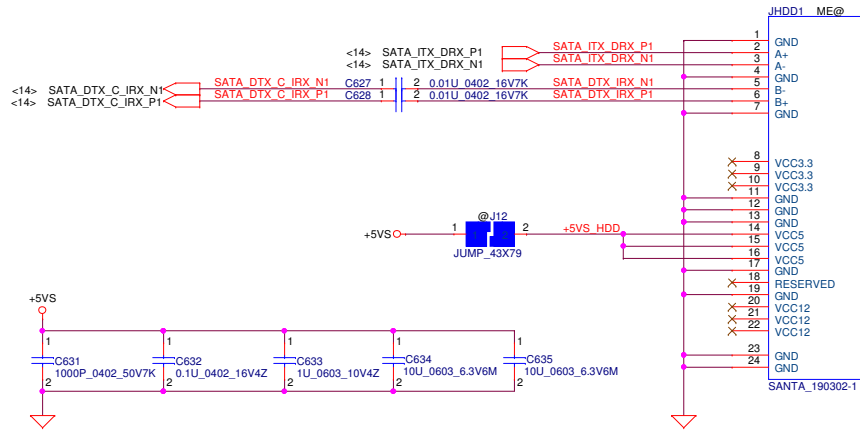


REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

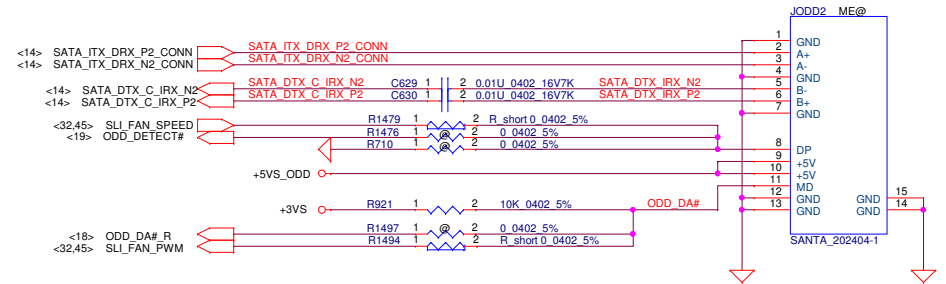
FAN1 Conn



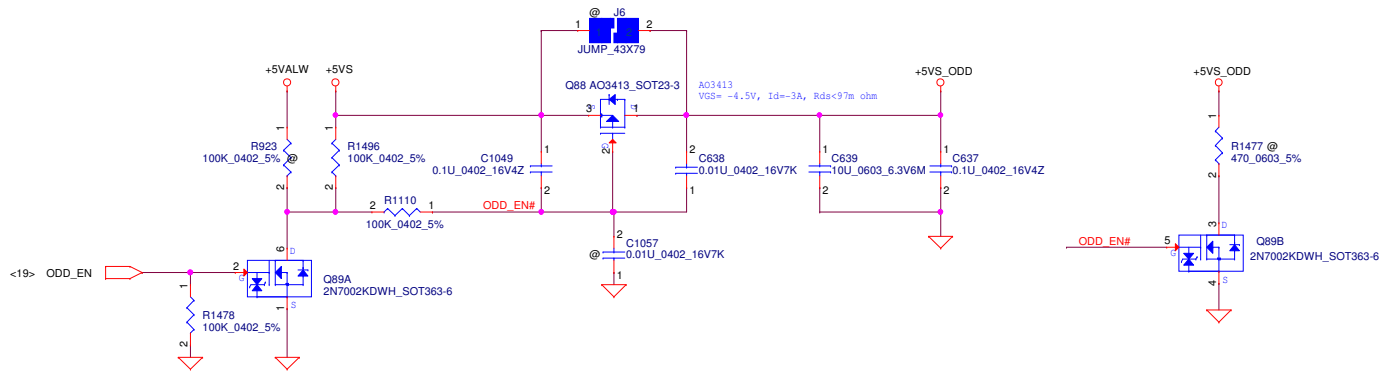
SATA HDD Conn.

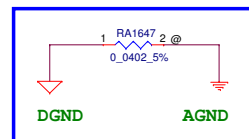
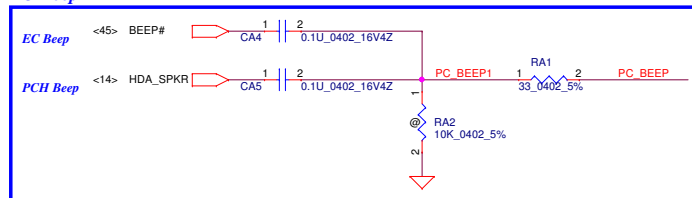
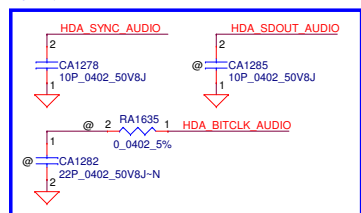
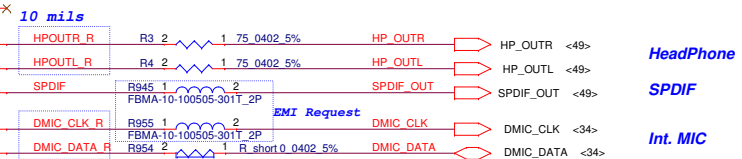
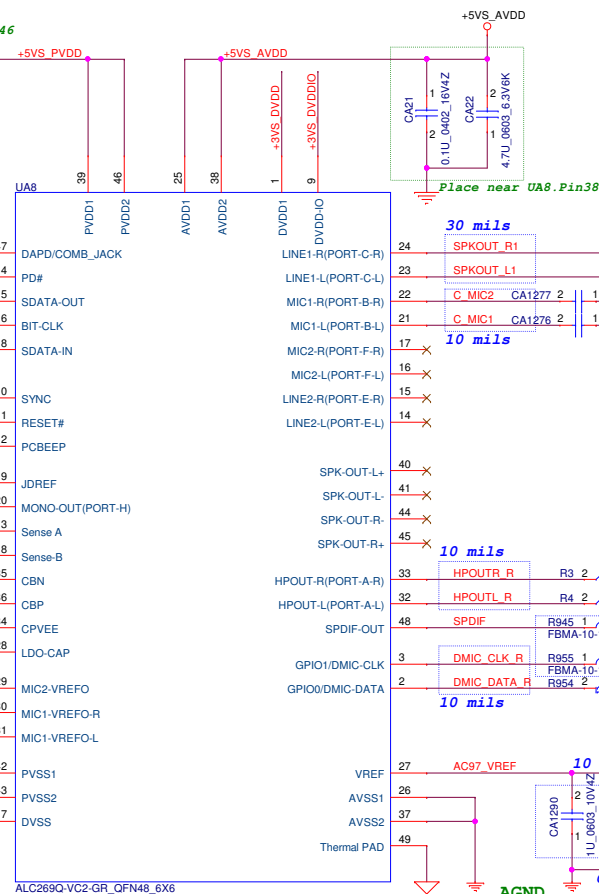
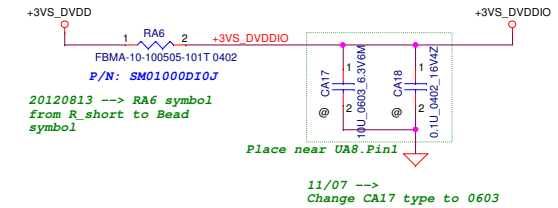
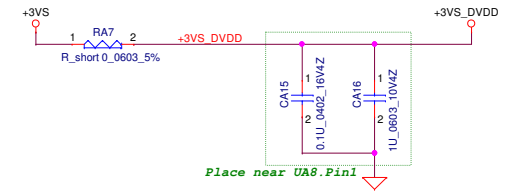



SATA ODD Conn.

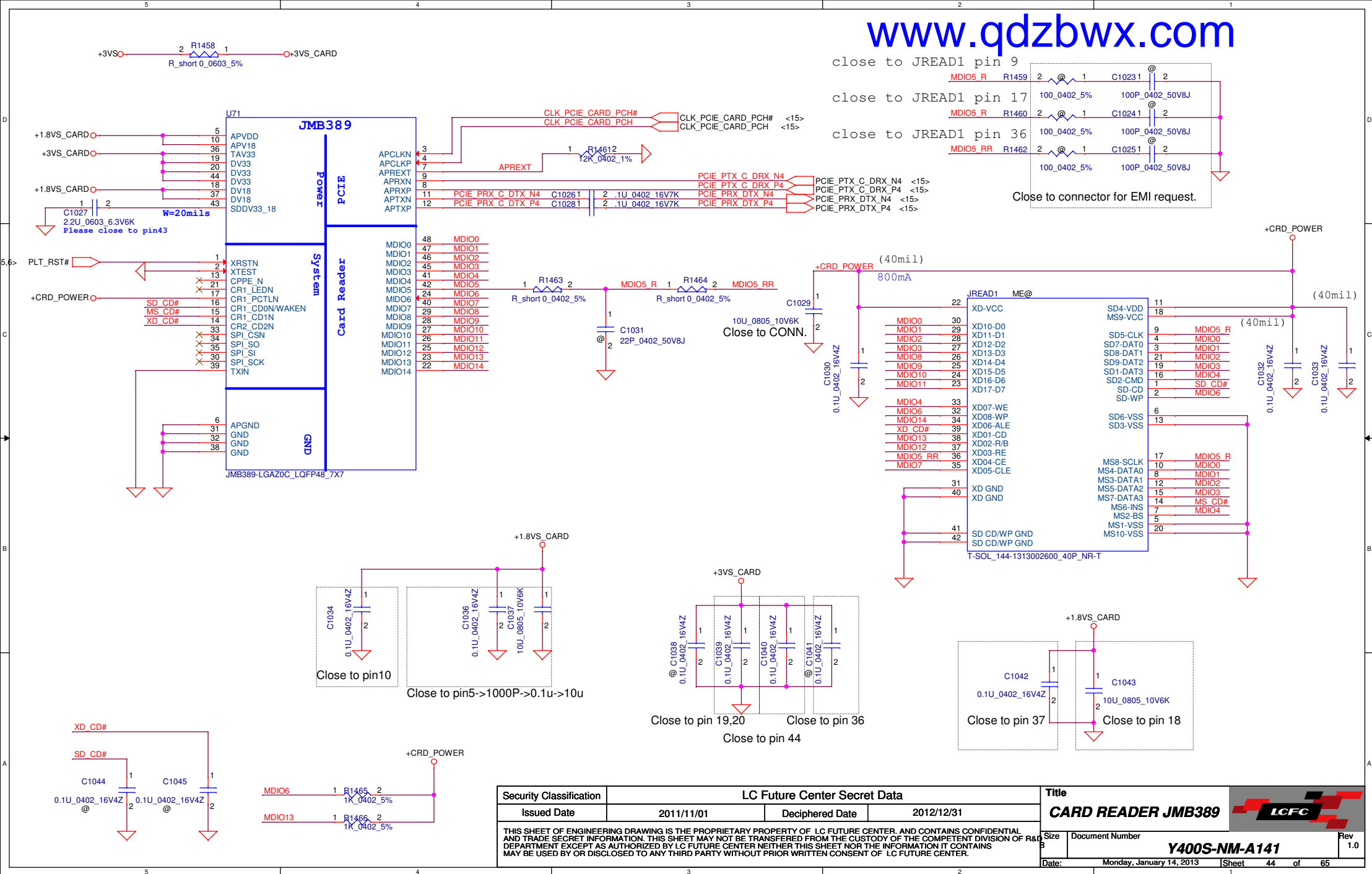



ODD Power Control

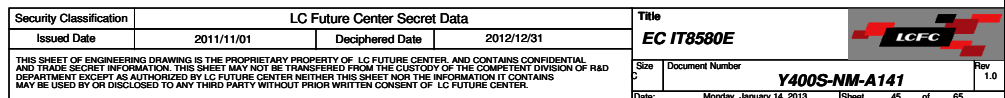




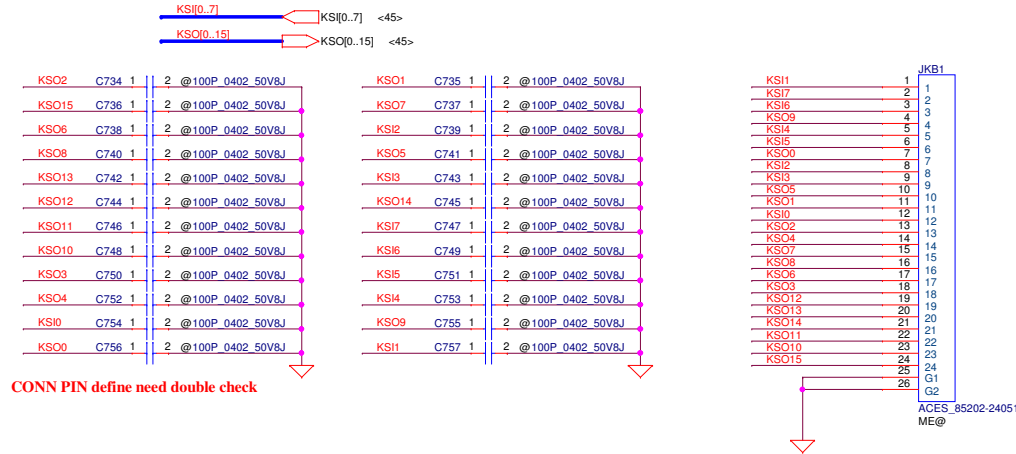
Security Classification		LC Future Center Secret Data		Title			
Issued Date	2011/11/01	Deciphered Date	2012/12/31	HD AUDIO ALC269Q-VC3			
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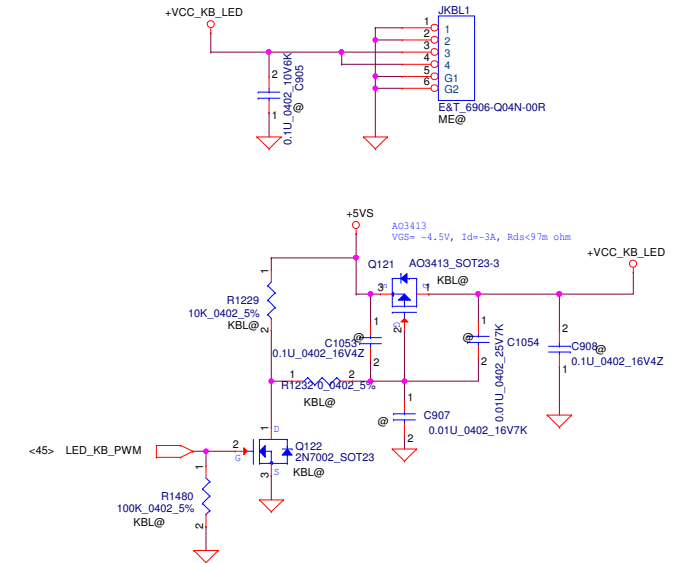
Security Classification		LC Future Center Secret Data				Title							
Issued Date		2011/11/01		Deciphered Date		2012/12/31							
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						Size		Document Number		Y400S-NM-A141		Rev 1.0	
						Date:		Monday, January 14, 2013		Sheet 44 of 65			



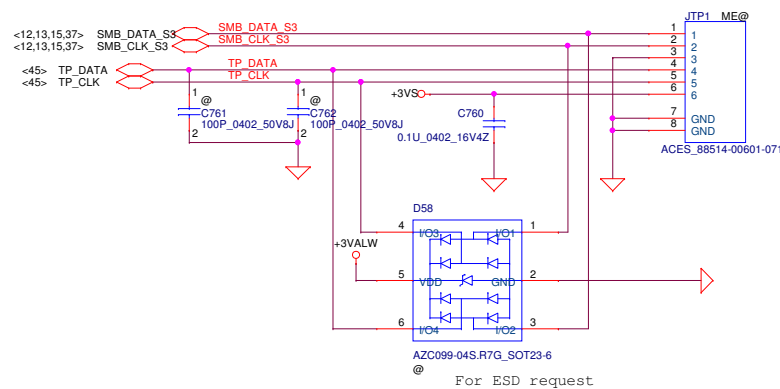
14" INT_KBD Conn.



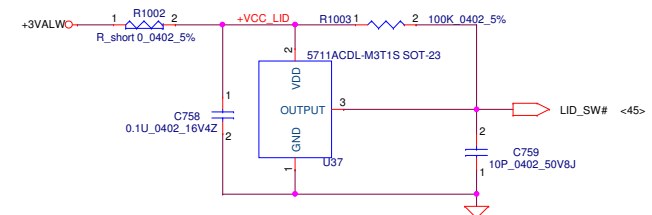
KB Lighting CONN.4pin

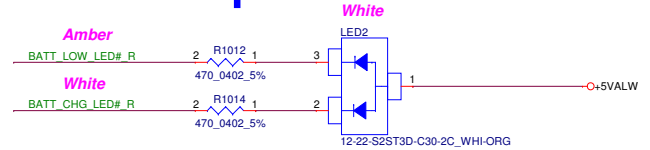
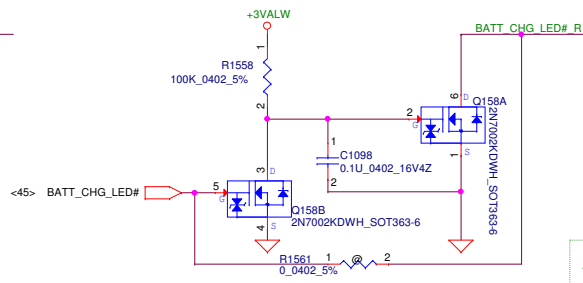
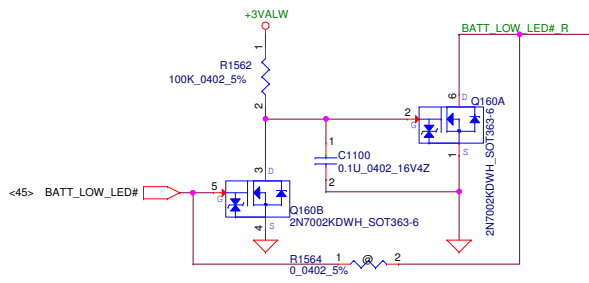


To TP/B Conn.

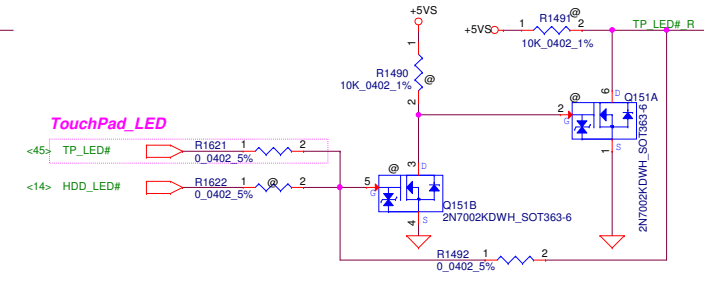
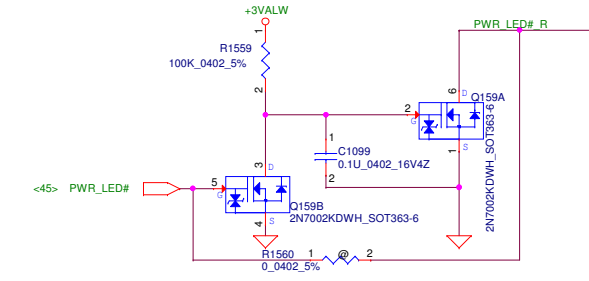


Lid Switch

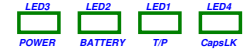
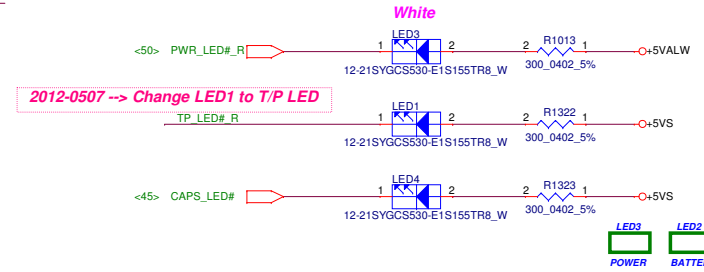




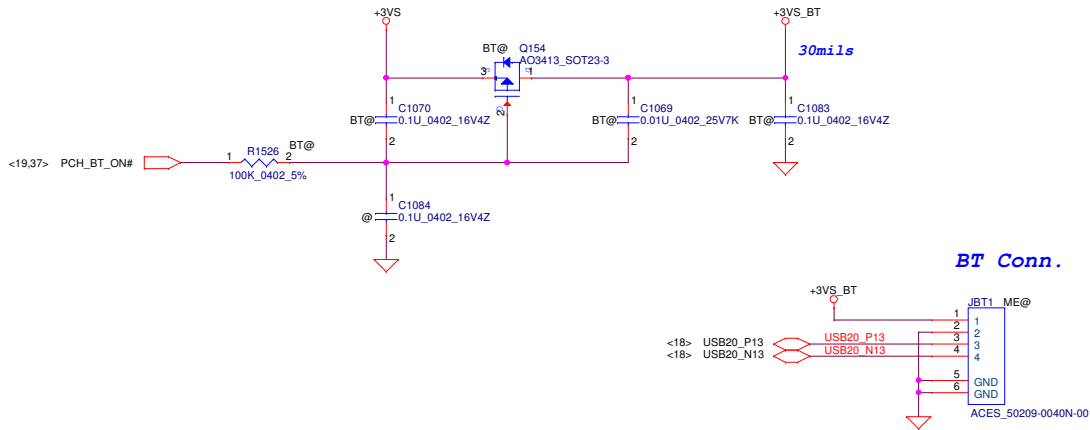
2012-0507 --> Add MOS solution onLED3, 2 to avoid the light blinked.



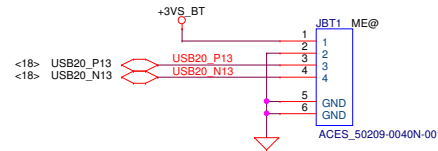
PWR LED HDD LED CapsLK LED



BlueTooth DC



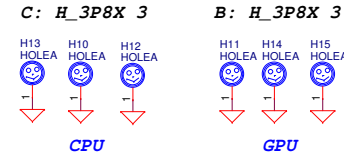
BT Conn.



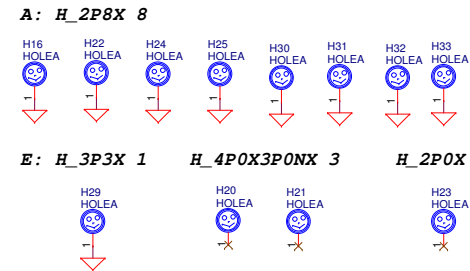
Screw Hole

CPU and GPU: H_3P8X 6

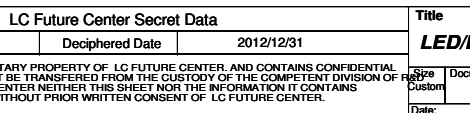
MIN PCIE: H_3P3 X 1



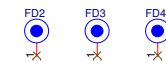
ME: H_8P0 X 8; H_3P3X 1; H_4P0X3P0N X 2; H_2P0X 1



E: H_3P3X 1 H_4P0X3P0NX 3 H_2P0X 2

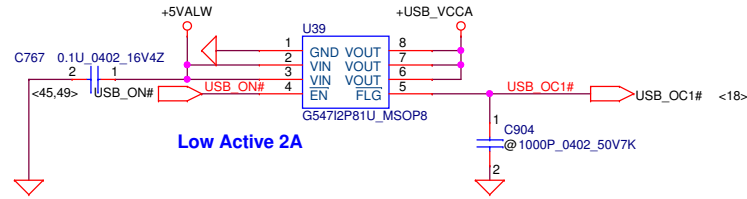


PCB Federal Mark PAD



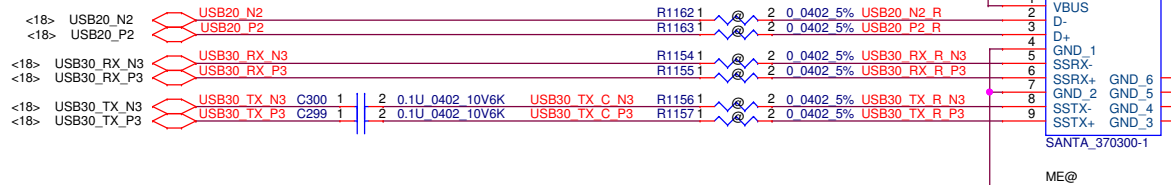
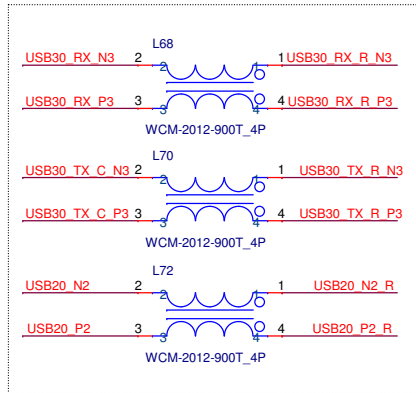
Security Classification	LC Future Center Secret Data			Title
Issued Date	2011/11/01	Deciphered Date	2012/12/31	LED/EC SPI ROM/BT
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Date: Monday, January 14, 2013				Sheet 47 of 65

LEFT SIDE USB3.0 PORT X1

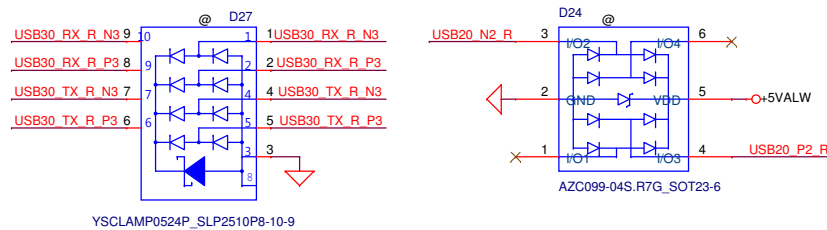


Low Active 2A

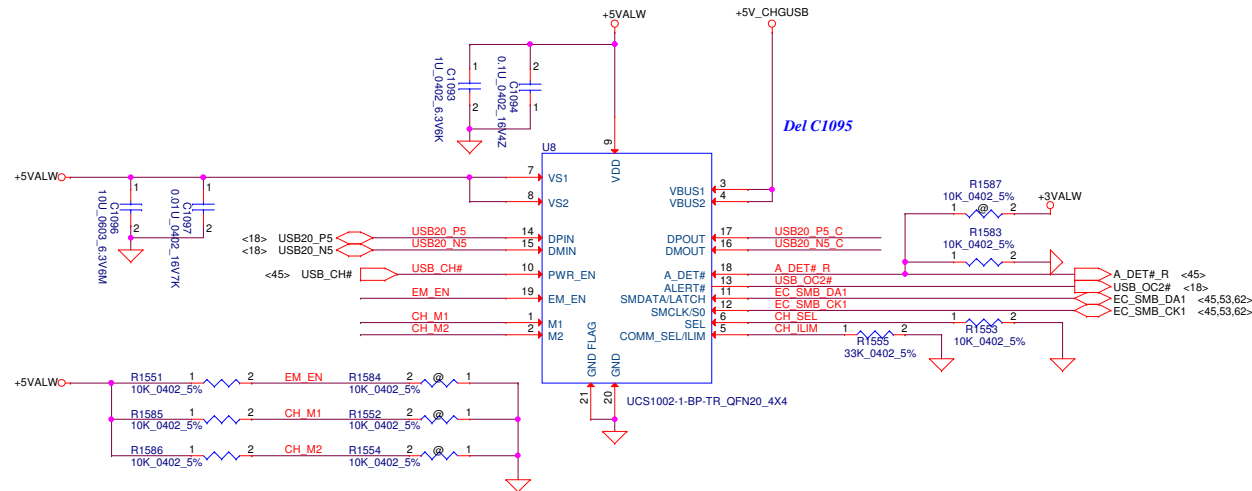
For EMI request
USB2.0 choke --> SM070000I00
USB3.0 Choke --> SM070001U00



For ESD request



Sleep & Charge
Right side USB Charger Port (USB_Port5, near JMIC1)



2012-0429 --> Set default mode is "BC1.2 CDP" Mode (2.5A on S0) for USB Port5

Active Mode Selection:

M1	M2	EM_EN	ACTIVE MODE
0	0	1	Dedicated Charger Emulation Cycle
0	1	0	Date Pass-Through
0	1	1	BC1.2 DCP
1	0	0	BC1.2 SDP
1	1	0	Dedicated Charger Emulation Cycle
1	1	1	Date Pass-Through
★ 1	1	1	BC1.2 CDP

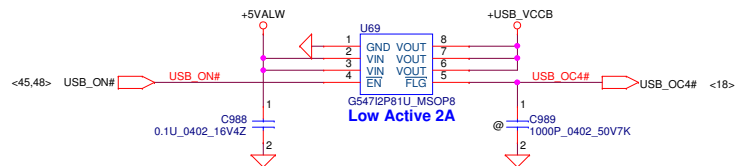
ILIM SETTING

Pull Low
0R-500mA
10K-900mA
12K-1000mA
15K-1200mA
18K-1500mA
22K-1800mA
27K-2000mA
★ 33K-2500mA

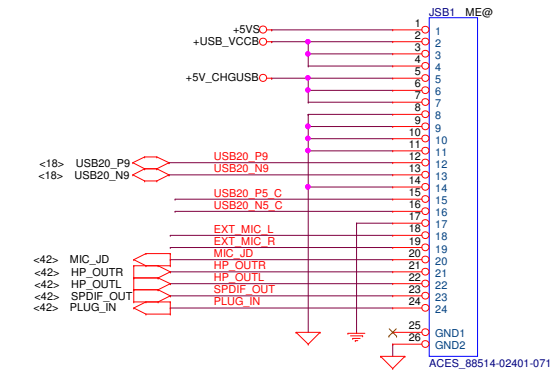
SEL Pin Decode

Pull Low
0R-1010_000
★ 10K-1010_000
12K-1010_000
15K-1010_000
18K-0110_000
22K-0110_000
27K-0110_000
33K-0110_000

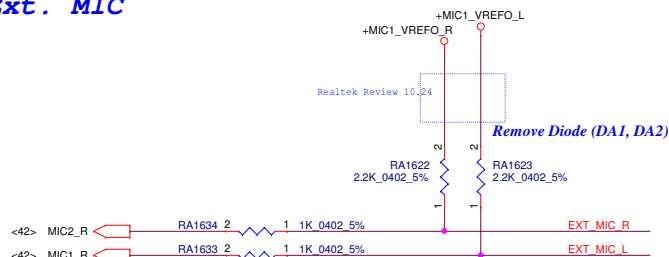
USB Power (USB20_P9)



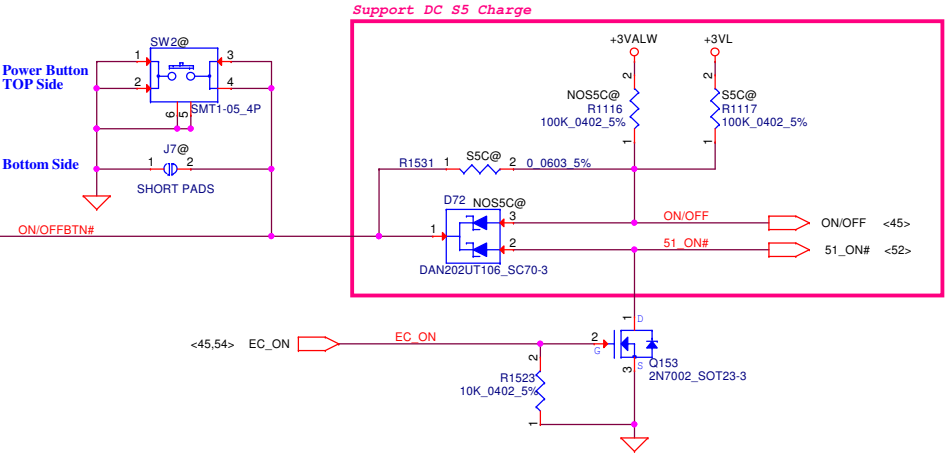
AUDIO/B Conn.



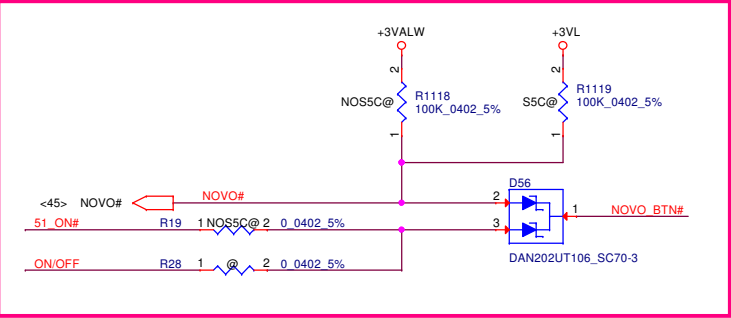
Ext. MIC



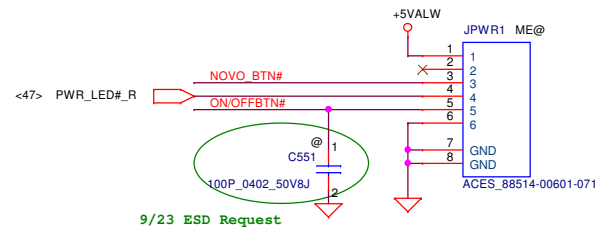
ON/OFF switch



Support DC S5 Charge



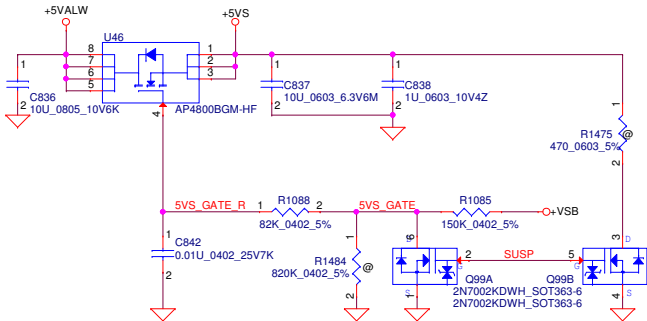
Power Button/Link to Function/B Conn. 10pin



EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

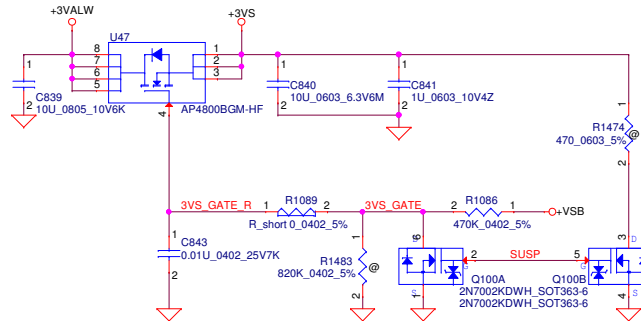
+5VALW to +5VS

AP4800BGM
VGS=1.0V, ID=9A, Rds=12m ohm
VGS=-25V



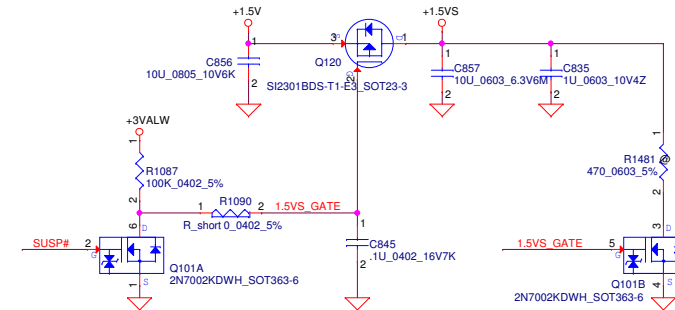
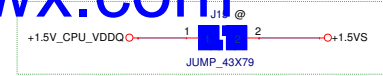
+3VALW to +3VS

AP4800BGM
VGS=1.0V, ID=9A, Rds=12m ohm
VGS=-25V



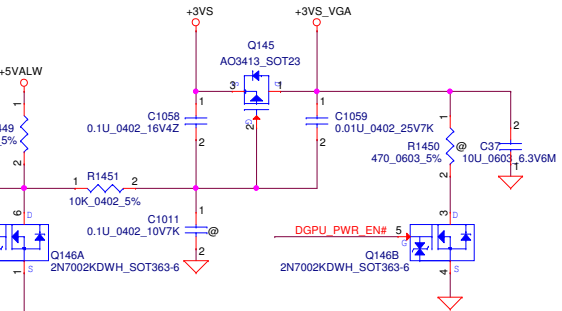
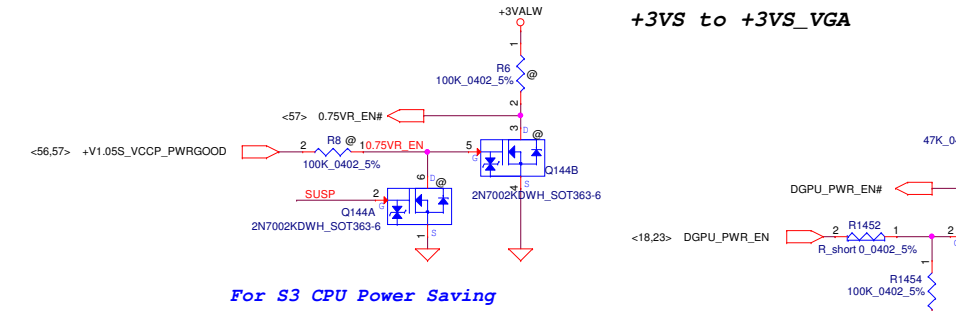
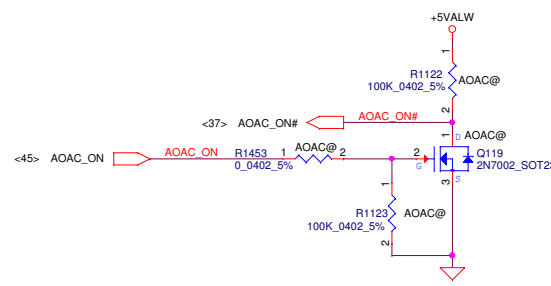
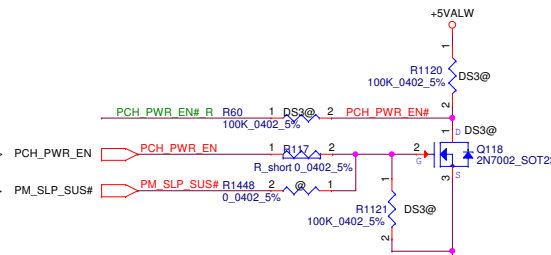
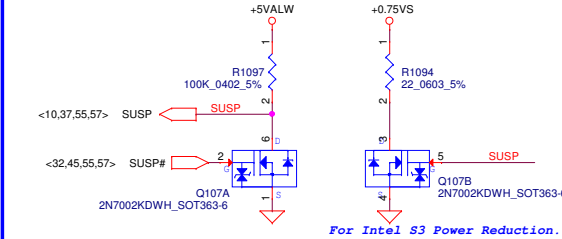
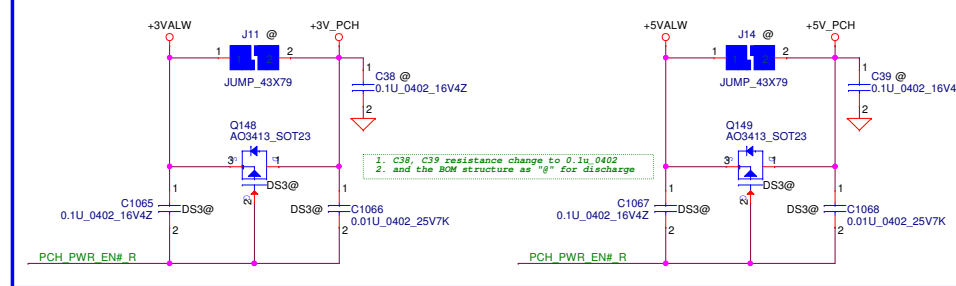
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+1.5V to +1.5VS



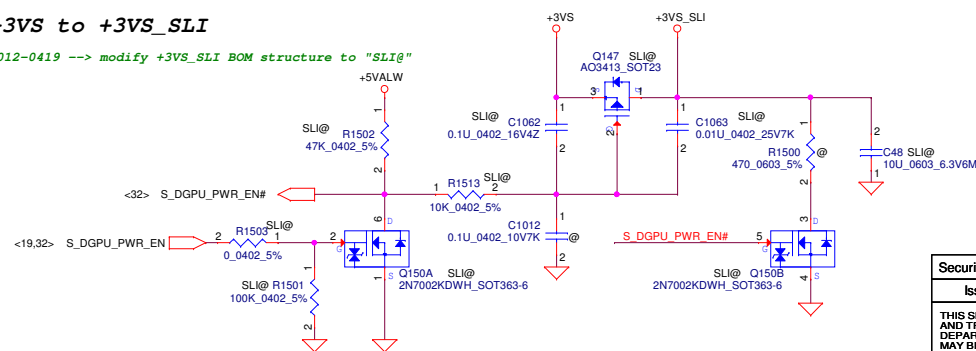
+3VALW to +3V_PCH


+5VALW to +5V_PCH



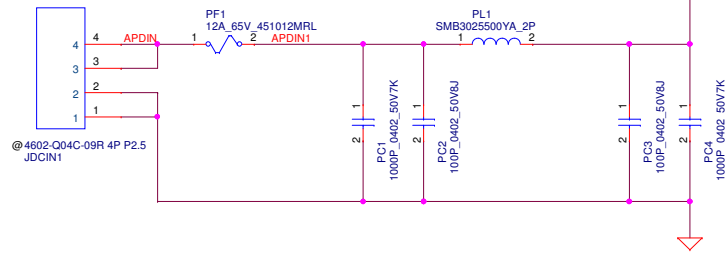
+3VS to +3VS_SLI

2012-0419 --> modify +3VS_SLI BOM structure to "SLI@"

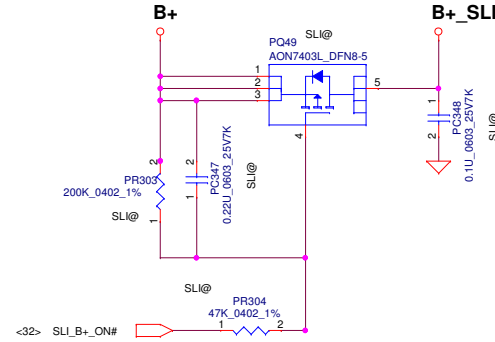


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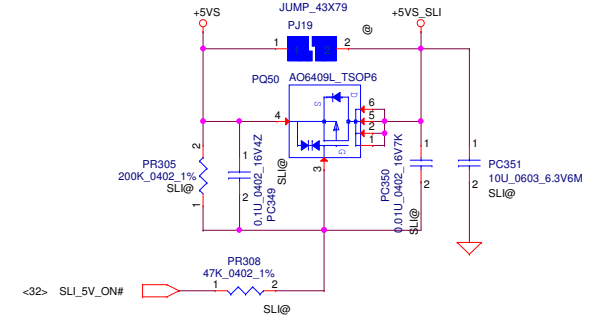
DC030006J00



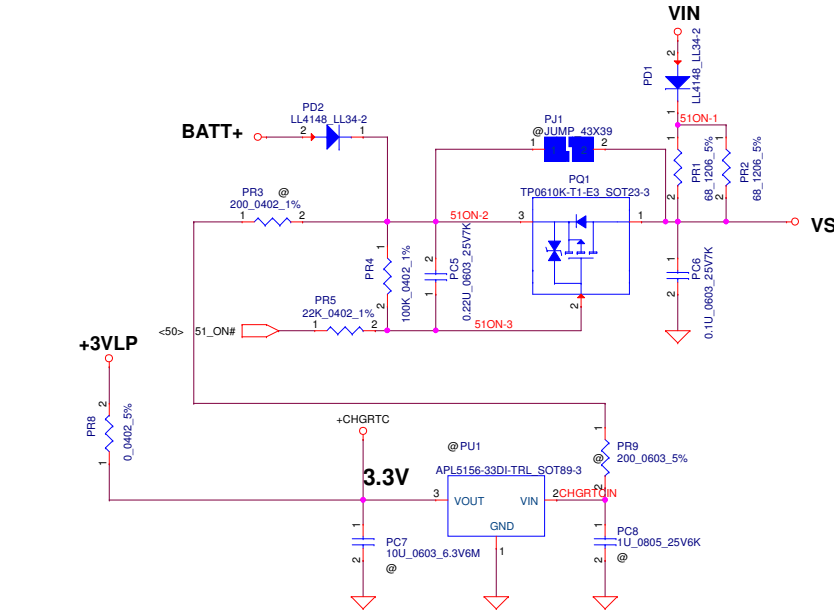
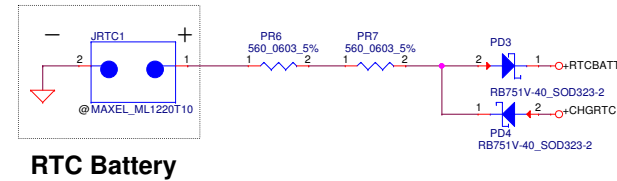
B+ to SLI_B+



+5VS to +5VS_SLI



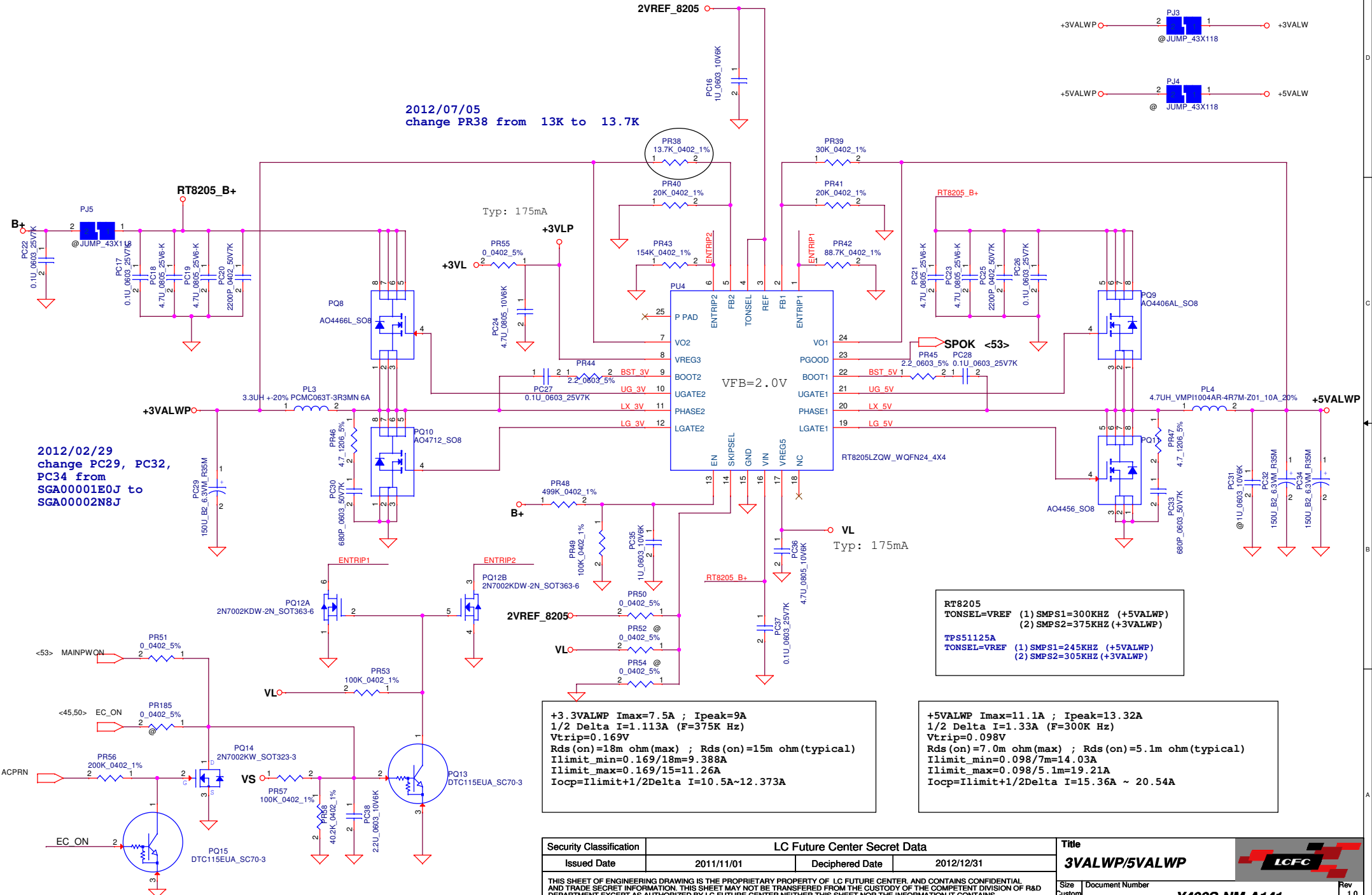
2012/04/13
add SLI Hot-plug Load-SW solution



Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

2012/07/05
change PR38 from 13K to 13.7K

2012/02/29
change PC29, PC32,
PC34 from
SGA00001E0J to
SGA00002N8J




RT8205
TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)
TPS51125A
TONSEL=VREF (1) SMPS1=245KHZ (+5VALWP)
(2) SMPS2=305KHZ (+3VALWP)

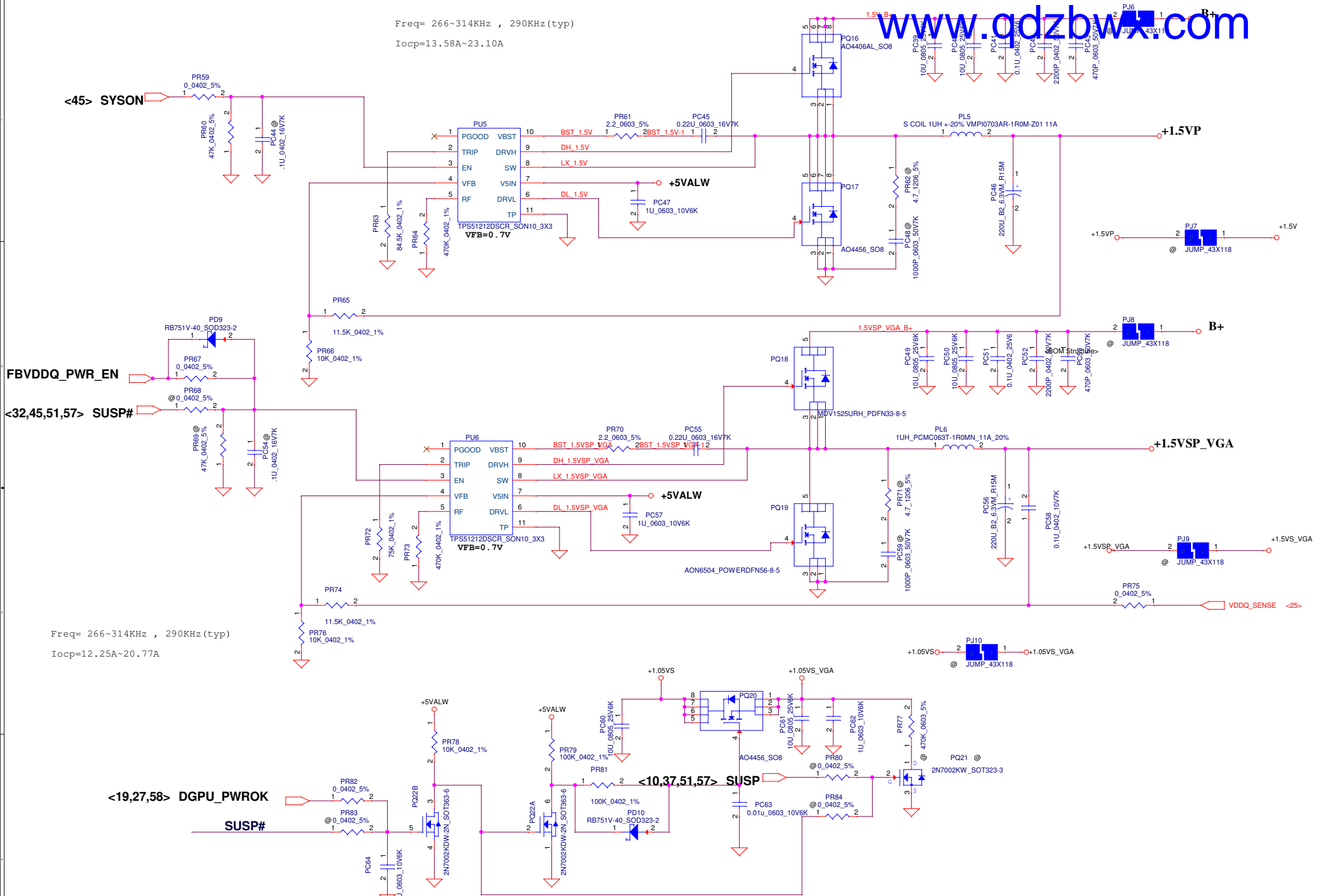
+3.3VALWP Imax=7.5A ; Ipeak=9A
1/2 Delta I=1.113A (F=375K Hz)
Vtrip=0.169V
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=0.169/18m=9.388A
Ilimit_max=0.169/15m=11.26A
Iocp=Ilimit+1/2Delta I=10.5A~12.373A

+5VALWP Imax=11.1A ; Ipeak=13.32A
1/2 Delta I=1.33A (F=300K Hz)
Vtrip=0.098V
Rds(on)=7.0m ohm(max) ; Rds(on)=5.1m ohm(typical)
Ilimit_min=0.098/7m=14.03A
Ilimit_max=0.098/5.1m=19.21A
Iocp=Ilimit+1/2Delta I=15.36A ~ 20.54A

Security Classification		LC Future Center Secret Data		Title	
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Size Custom	Document Number			Rev	
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Date:	Monday, January 14, 2013	Sheet	54	of	65



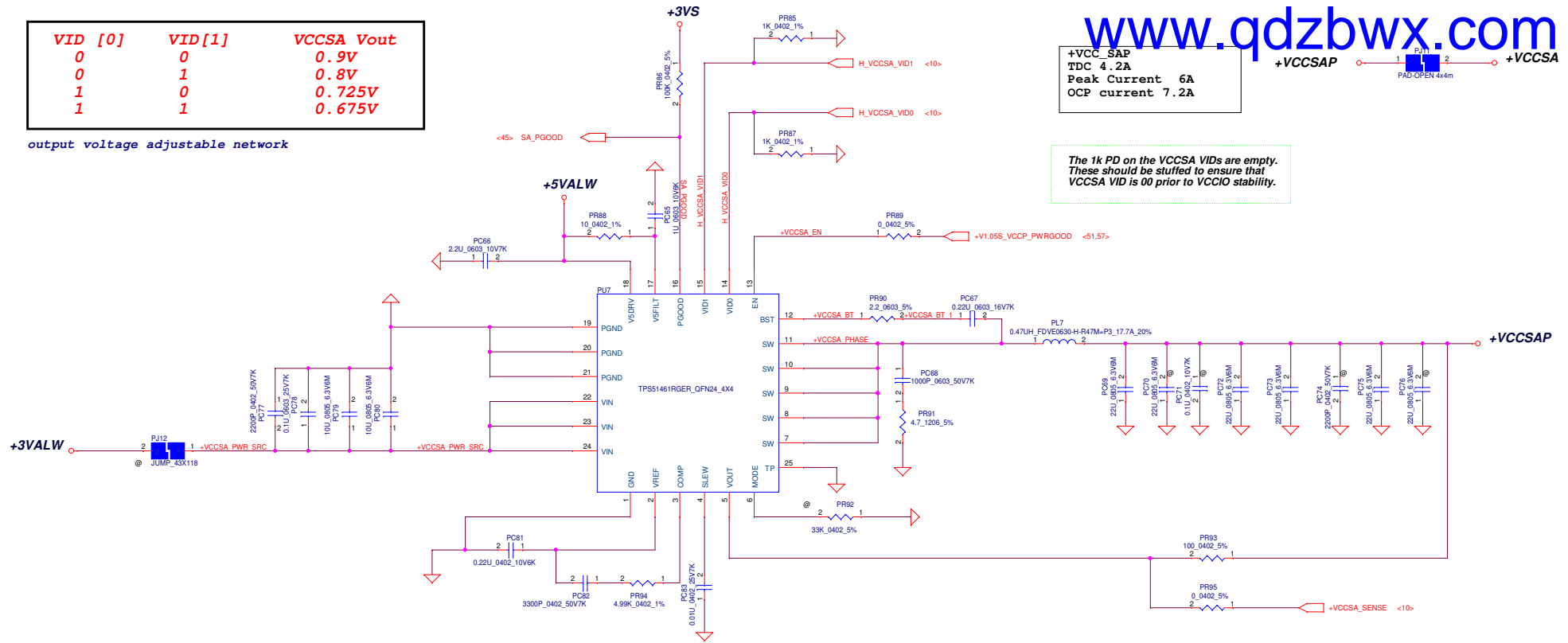
Freq= 266~314KHz , 290KHz(typ)
Iocp=13.58A~23.10A



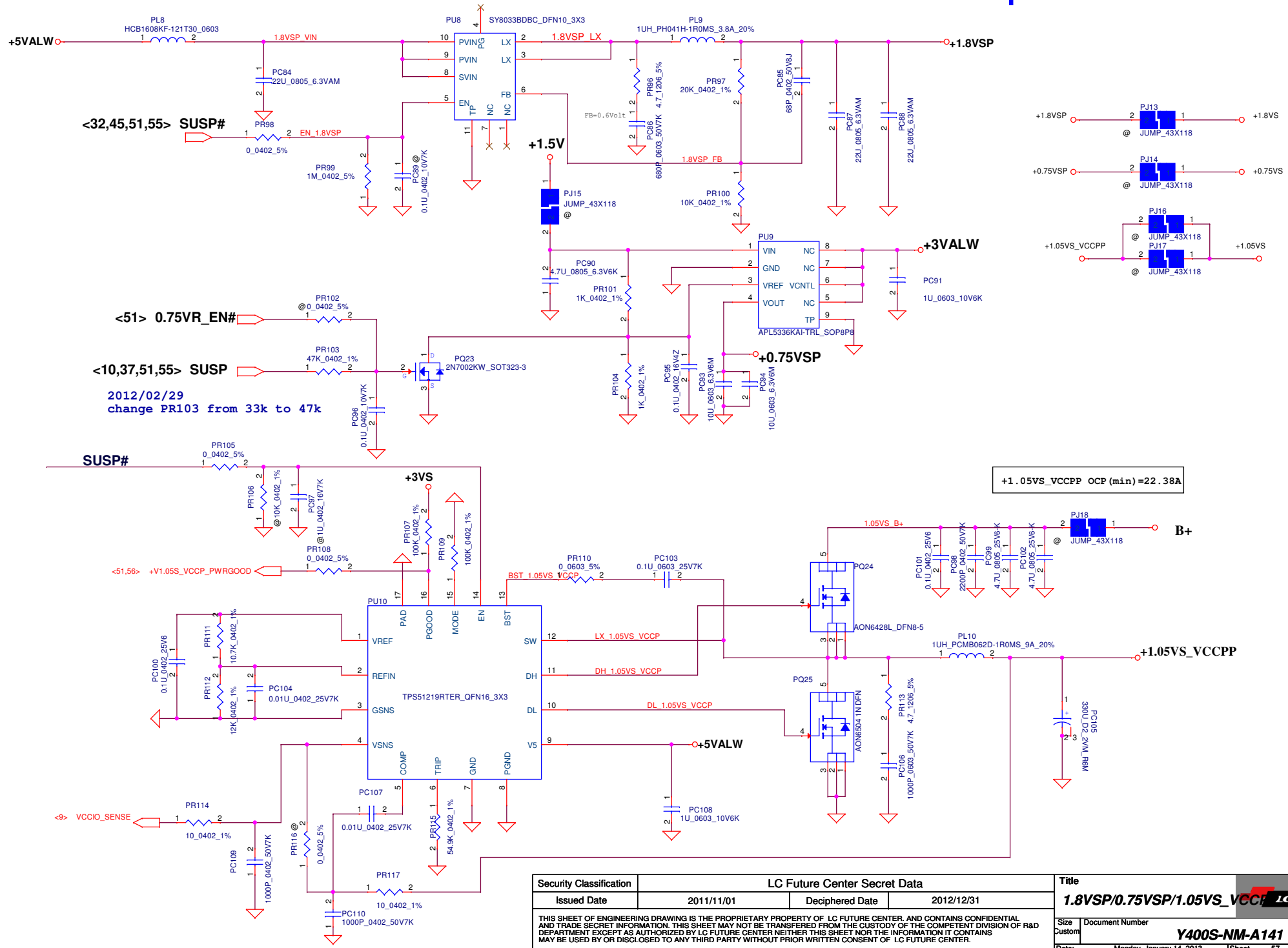
Freq= 266~314KHz , 290KHz(typ)
Iocp=12.25A~20.77A

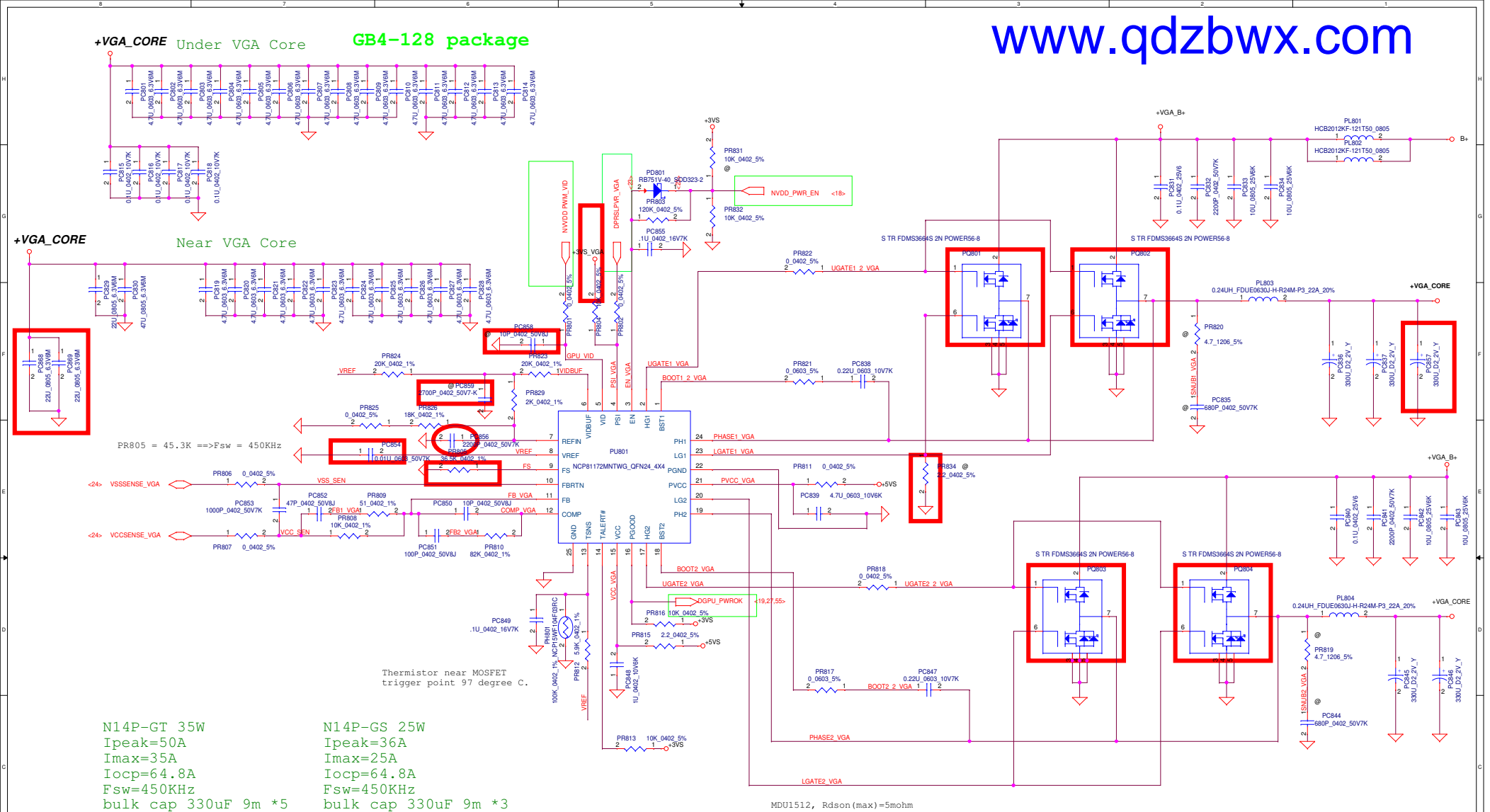
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

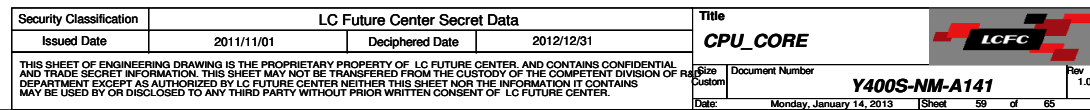
output voltage adjustable network

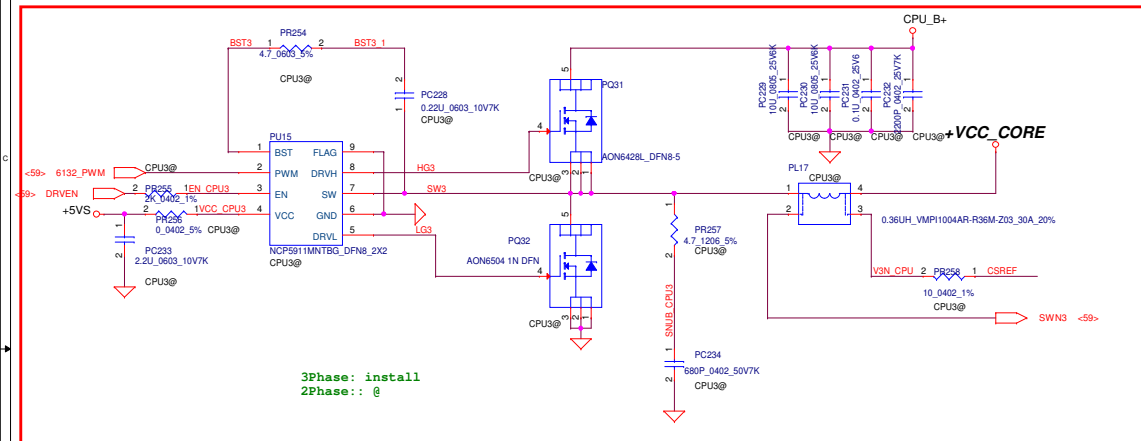
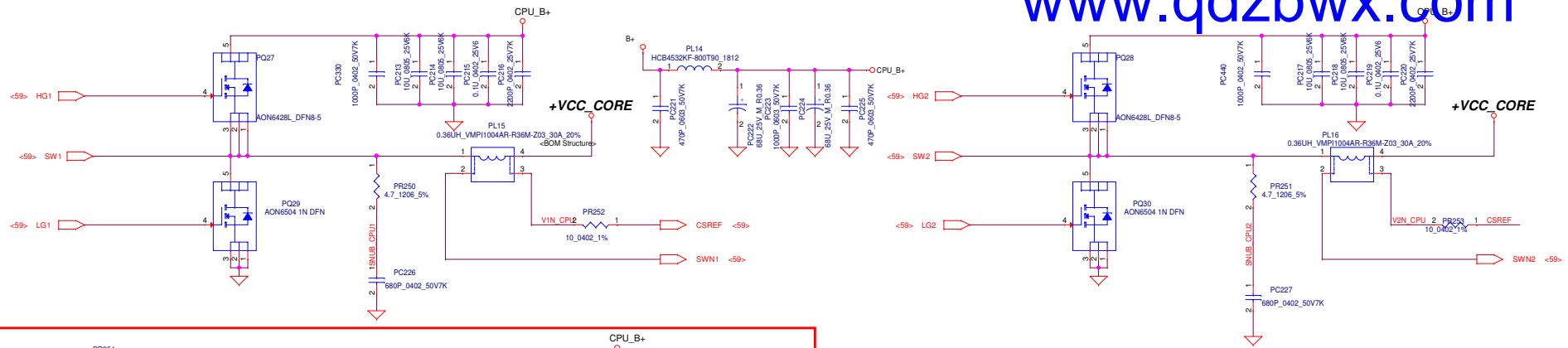


The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



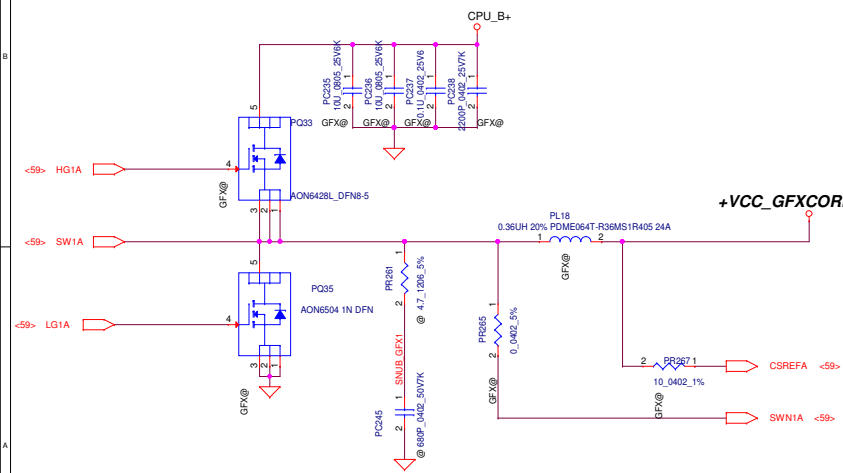






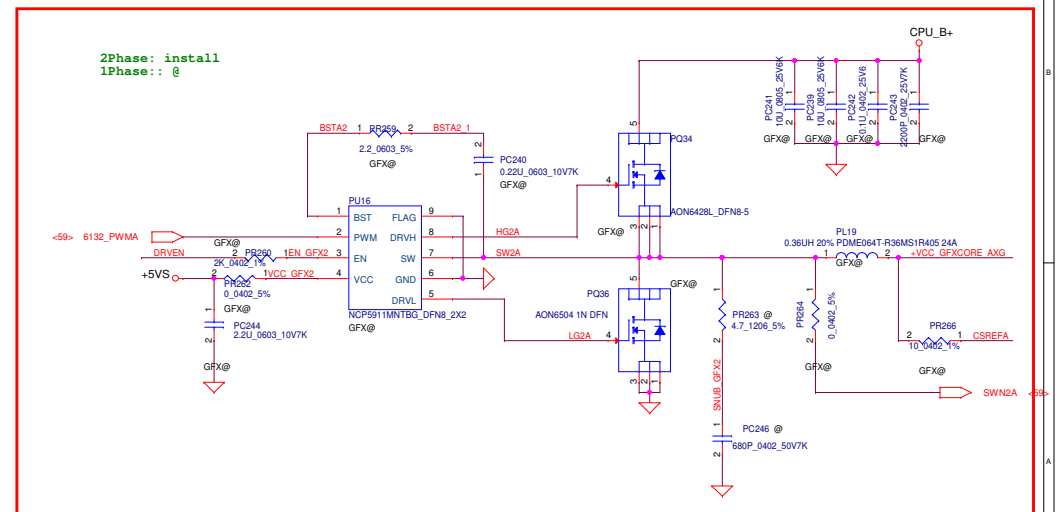
QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A


DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A

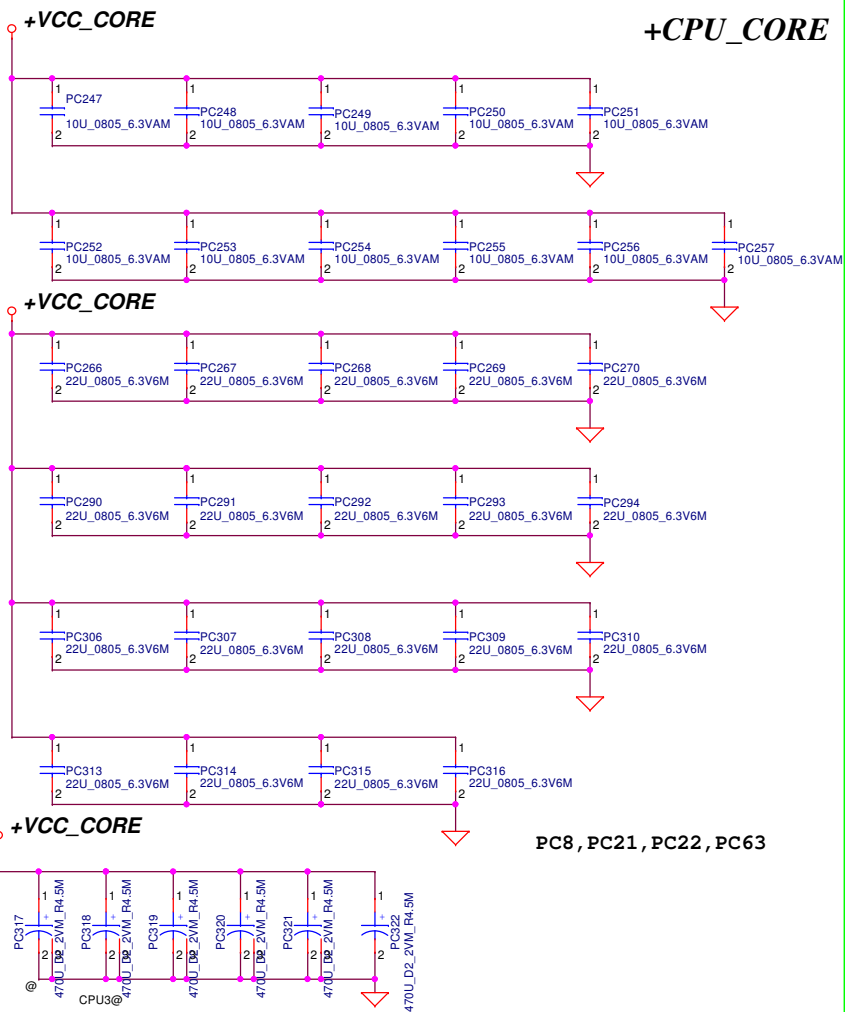


QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_OL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_OL=3.9m ohm
OCP~40A

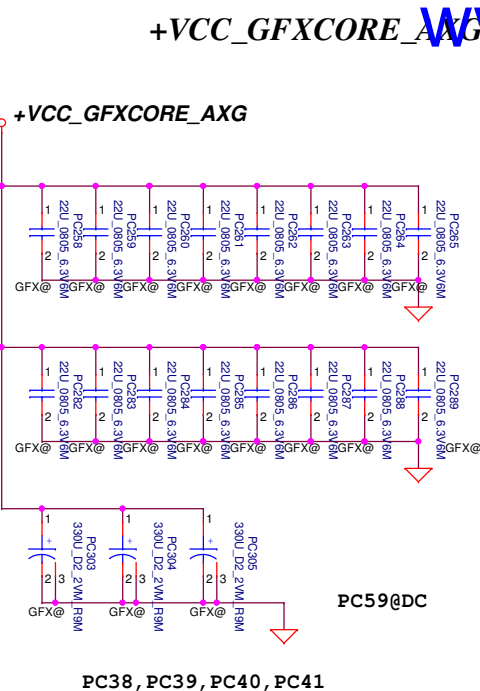


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DC: PC73, PC74, PC75, PC76, PC77, PC78 (330uF/9m)
 QC: PC76, PC78 (470uF/4.5m), PC73, PC74, PC75 (330uF/9m)

PC8, PC21, PC22, PC63



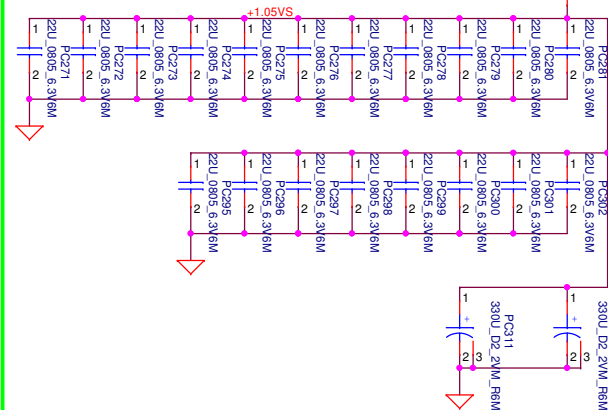
PC38, PC39, PC40, PC41

PC38, PC39, PC40, PC41

Below is 75514 GVF PDDG (1.5 Table 5-8.

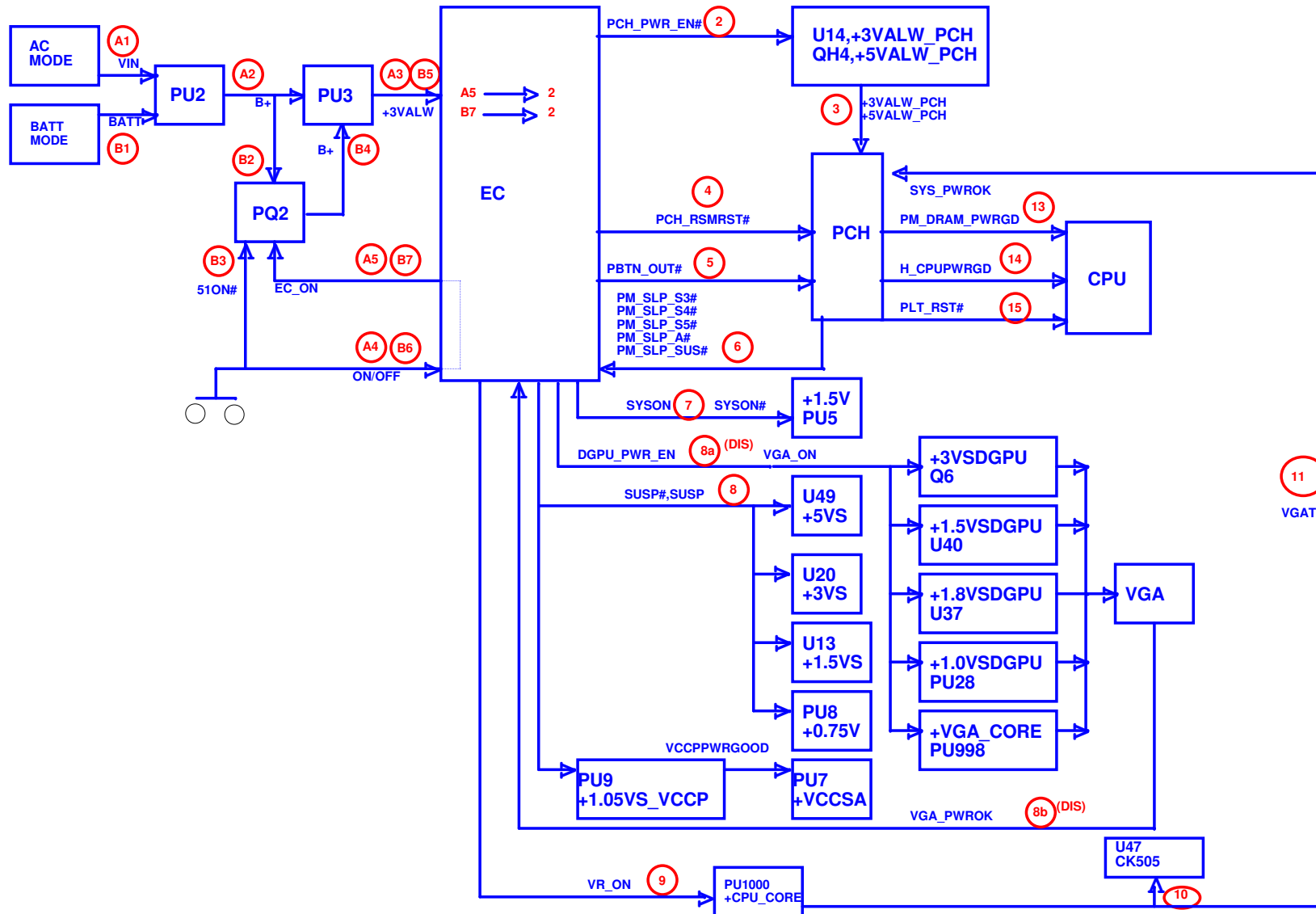
Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+1.05VS



PC32, PC49, PC54, PC55, PC56






Version change list (P.I.R. List)

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Item	Reason for change	PG#	Modify List	Date	Phase
1	For NV suggest	58	Add (reserve parts) PC859		
2	For TI suggest	58	Add (reserve parts) PR834		
3					
4					
5					
6					
7					
8					
9					
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11					
12					
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14					
15					
16					
17					

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							Custom	MM-A141	1.0
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1		P23	Change DGPU_PWR_EN to PLT_RST_VGA#	For GC6 function
2		P23	Add CV148	For GC6 function
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				