

# Essentials Oak 14 Schematic

## Haswell-ULT

2013-5-23  
REV : A00

*DY : None Installed*  
*UMA: UMA only installed*  
*OPS: DISCRTE OPTIMUS installed*

<Core Design>



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Title

**Cover Page**

Size  
A3

Document Number

**OAK14 Haswell**

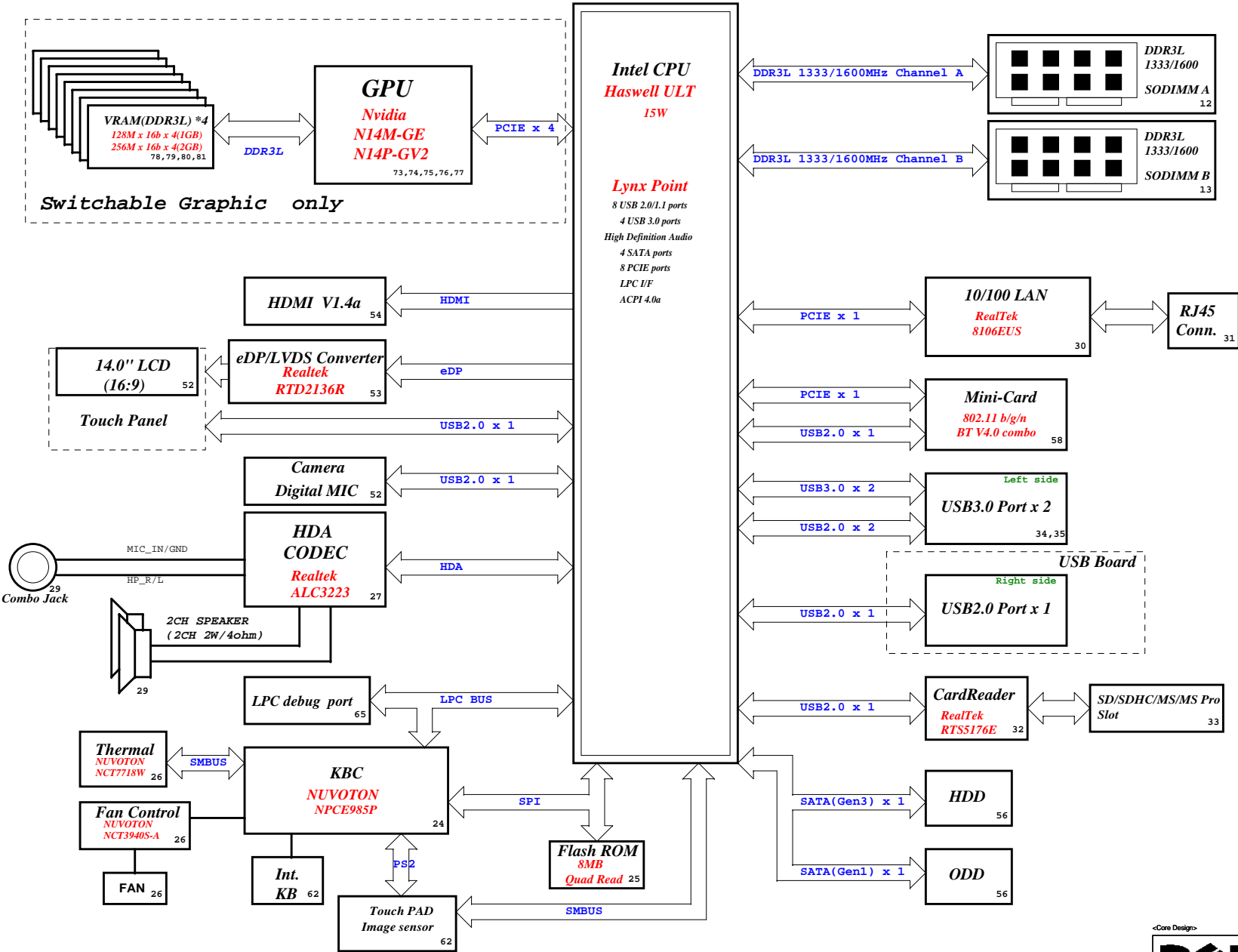
Rev

**X00**

Date: Thursday, May 23, 2013

Sheet 1 of 104


Oak14 Block Diagram



CHARGER		
BQ24717		44
INPUTS	OUTPUTS	
AD+	DCBATOUT	
BT+		
SYSTEM DC/DC		45
TPS51225		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5	
CPU Core Power		46,47
ISL95813		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
DDR3L SUS		49
TPS51216		
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3 0D65V_S0	
CPU 1.05V		48
RT8237		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0	
CPU 1D5V_S0		51
TLV70215		
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	
Switches		36 83
INPUTS	OUTPUTS	
1D35V_S3	1D35V_S0	
5V_S5	5V_S0	
3D3V_S5	0D675V_S0	
VCCP_CPU	3D3V_S0	
3D3V_S0	1D05V_VGA_S0	
	3D3V_VGA_S0	
	1D35V_VGA_S0	
PCB LAYER		
L1:Top	L5:VCC	
L2:GND	L6:Signal	
L3:Signal	L7:GND	
L4:Signal	L8:Bottom	

( Blanking )

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Title

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Size  
A3

Document Number  
OAK14 Haswell

Date: Thursday, January 10, 2013

Rev  
X00

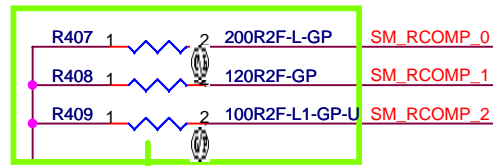
Sheet 3 of 104

SSID = CPU

24,42,44,46 H\_PROCHOT# <<>>

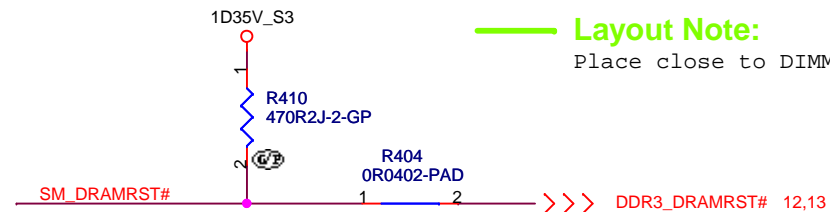
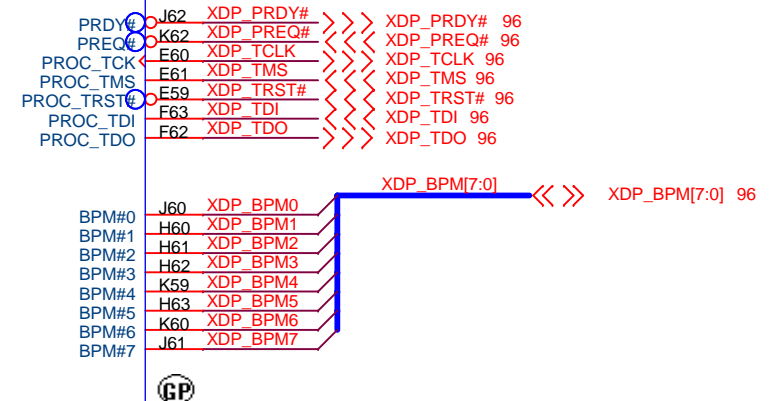
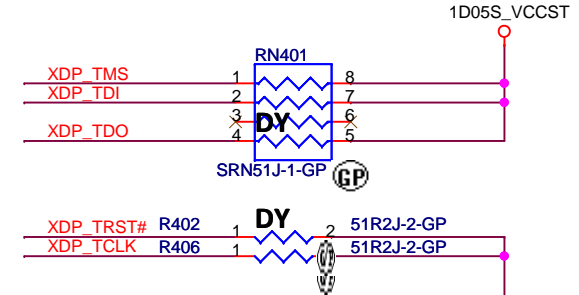
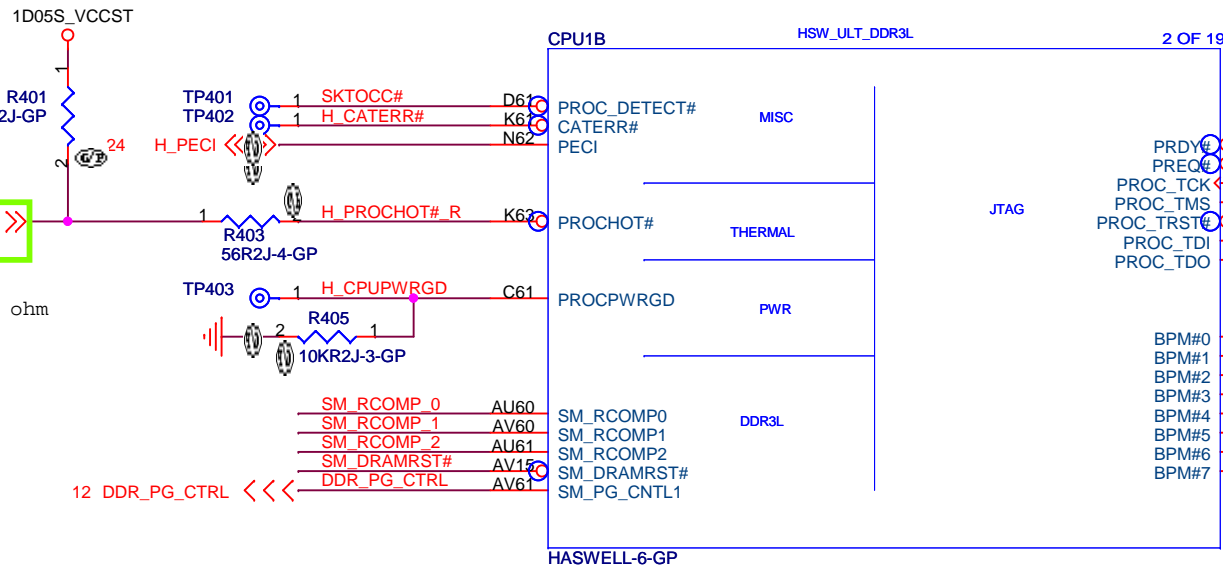
### Layout Note:

Impedance control:50 ohm



### Layout Note:

Design Guideline:  
SM\_RCOMP keep routing length less than 500 mils.



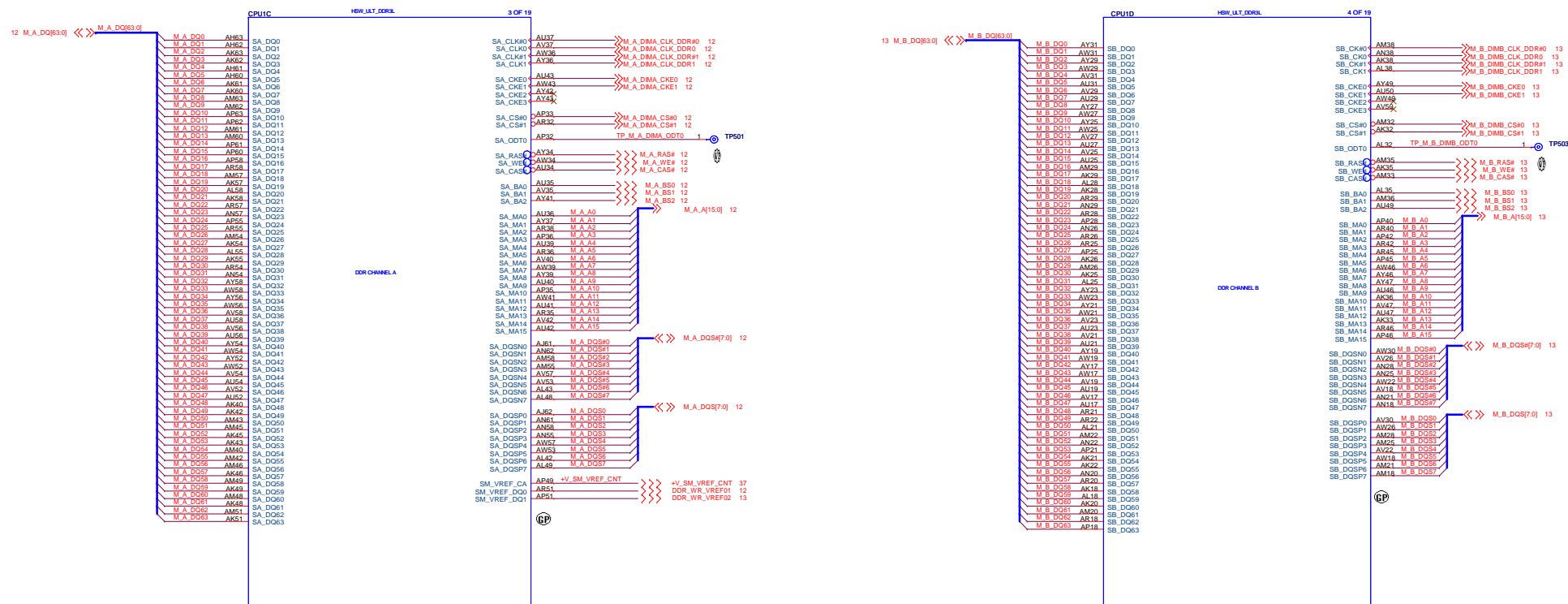
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Title			CPU (THERMAL/MISC/PM)	
Size	Document Number		Rev	
A4	OAK14 Haswell		X00	
Date: Monday, June 03, 2013		Sheet 4 of 104		

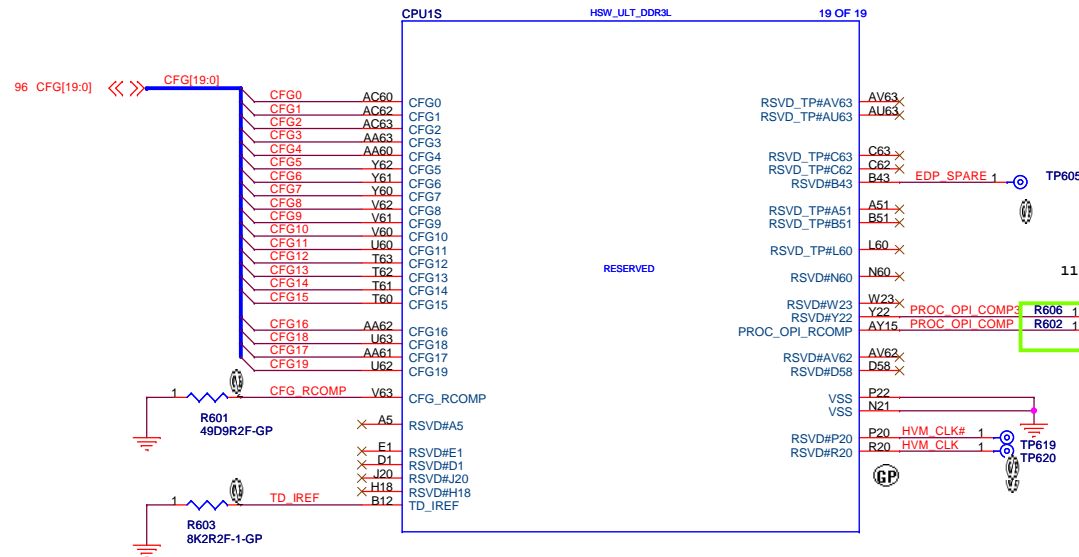
SSID = CPU



Title **CPII (DDR)**

Size A2	Document Number <b>OAK14 Haswell</b>	Rev <b>X0</b>
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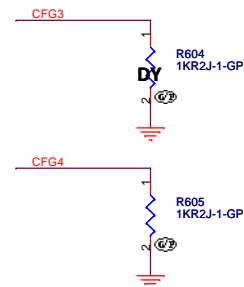
**SSID = CPU**



(follow EA40)

**Layout Note:**

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12-15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT



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Title	Author	Year	Journal	Volume	Page
...	...	...	...	...	...

**CPU (RESERVED)**

Size  
A3

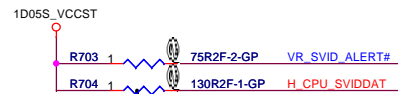
Document Number
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**OAK14 Haswell**Rev  
**X00**

Date: Thursday, March 07, 2013

Sheet 6 of 104

SSID = CPU

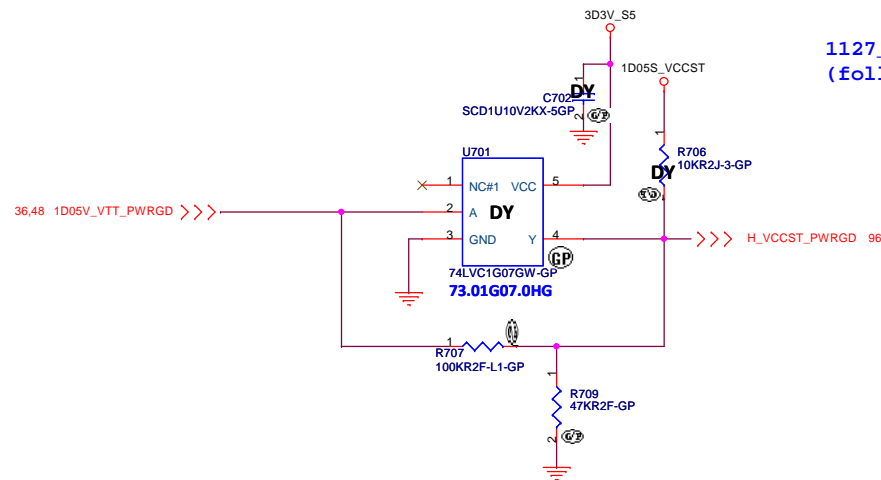


1127 130R change to 110R  
1203 110R change to 130R

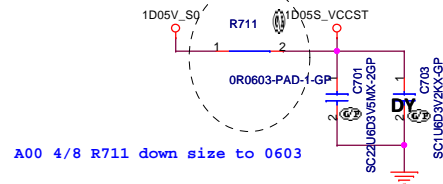
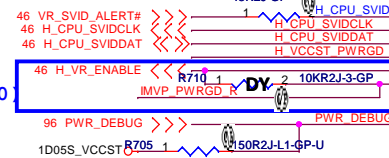
1127 Change net name of R703.2  
from VR\_SVID\_ALERT# to  
H\_CPU\_SVIDALRT#

Layout Note:

1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
3. Lwngh match<25mil

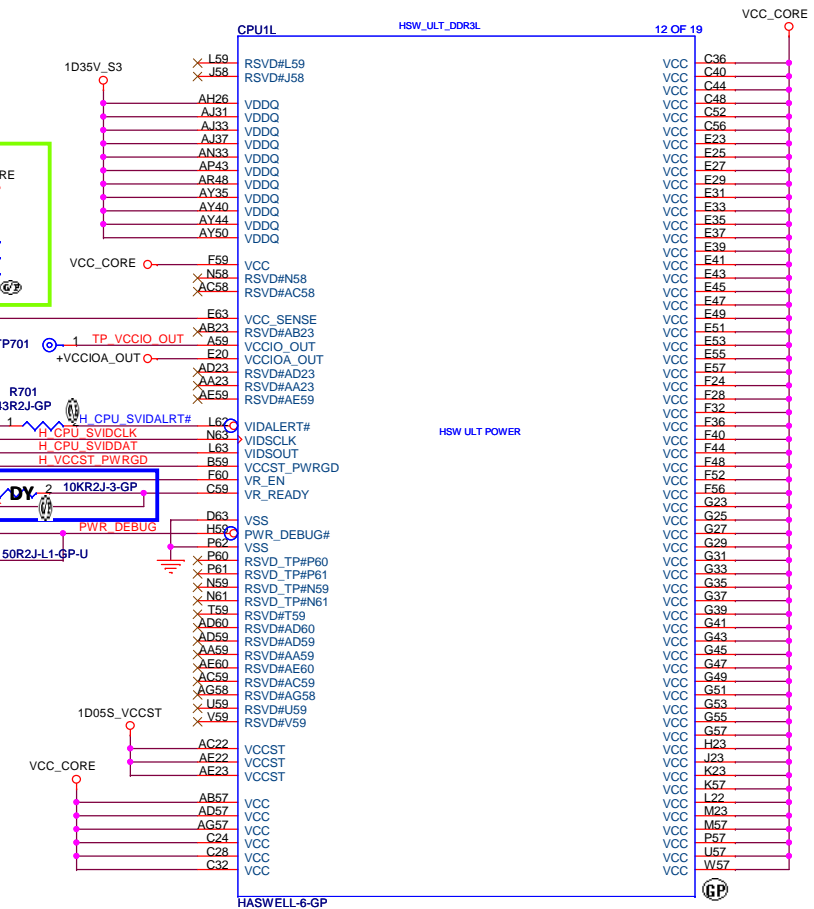
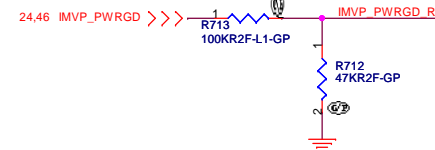


1127 modify  
(follow EA40)



A00 4/8 R711 down size to 0603

1205 Add



<Core Design>



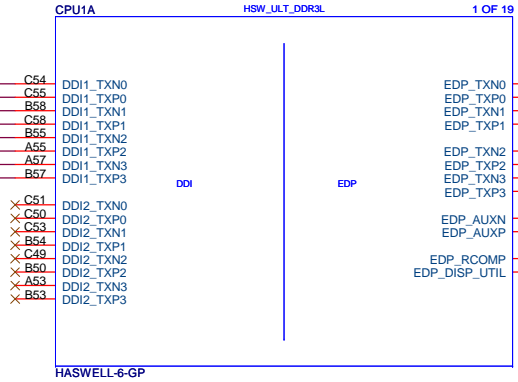
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Title			CPU (VCC CORE)	
Size	Document Number	OAK14 Haswell		Rev
A3				X00
Date:	Monday, April 22, 2013	Sheet	7	of 104

SSID = CPU

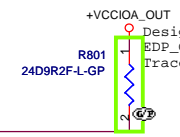
HDMI

54 HDMI\_DATA2#  
54 HDMI\_DATA2#  
54 HDMI\_DATA1#  
54 HDMI\_DATA1#  
54 HDMI\_DATA0#  
54 HDMI\_DATA0#  
54 HDMI\_CLK#  
54 HDMI\_CLK#



EDP\_TXN0  
EDP\_TXP0  
EDP\_TXN1  
EDP\_TXP1  
EDP\_TXN2  
EDP\_TXP2  
EDP\_TXN3  
EDP\_TXP3  
EDP\_AUXN  
EDP\_AUXP  
EDP\_RCOMP  
EDP\_DISP\_UTIL

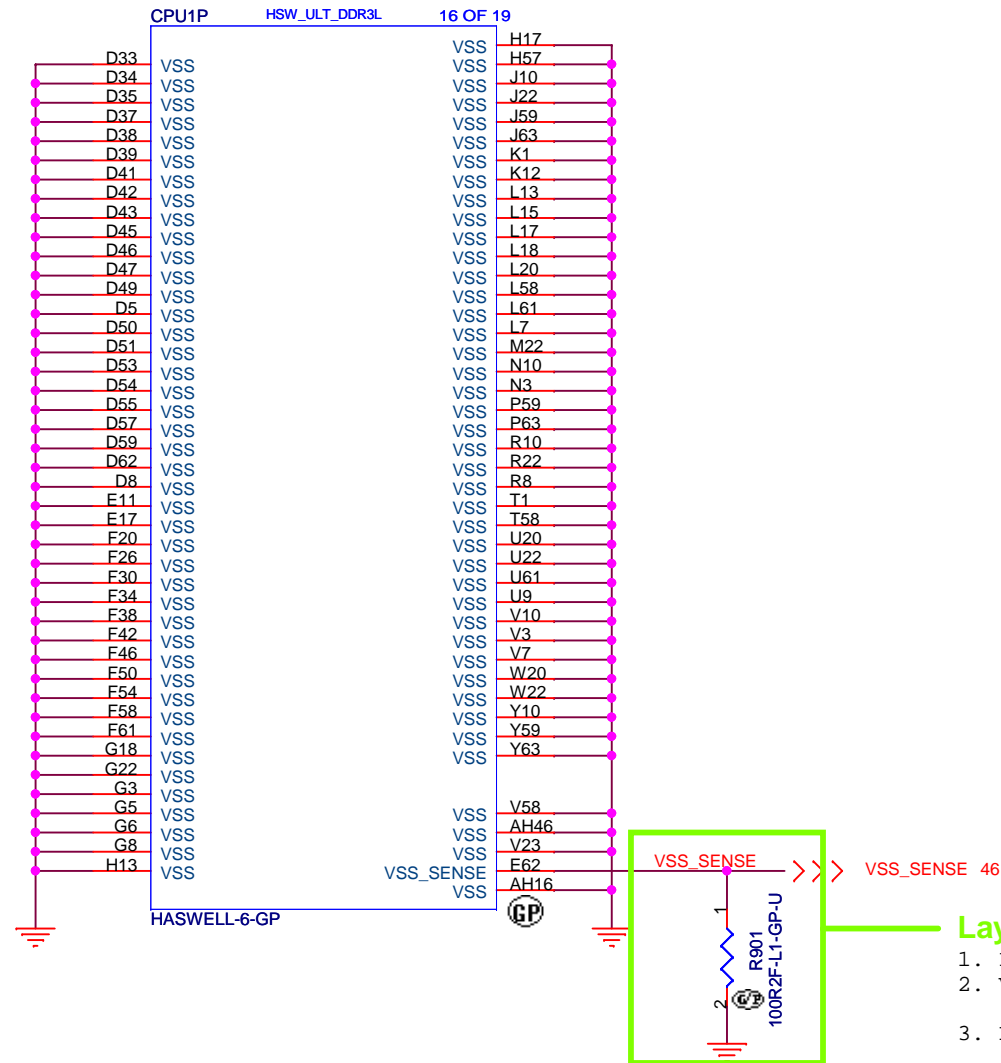
EDP\_TX0\_DN 53  
EDP\_TX0\_DP 53  
EDP\_TX1\_DN 53  
EDP\_TX1\_DP 53  
EDP\_AUX\_DN 53  
EDP\_AUX\_DP 53  
EDP\_COMP  
EDP\_BRIGHTNESS



Design Guideline:  
EDP\_COMP keep routing length max 100 mils.  
Trace Width:20 mils.



**SSID = CPU**



- **Layout Note:**

1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
3. Lwngth match<25mil

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**CPU (VSS)**

Size  
A4

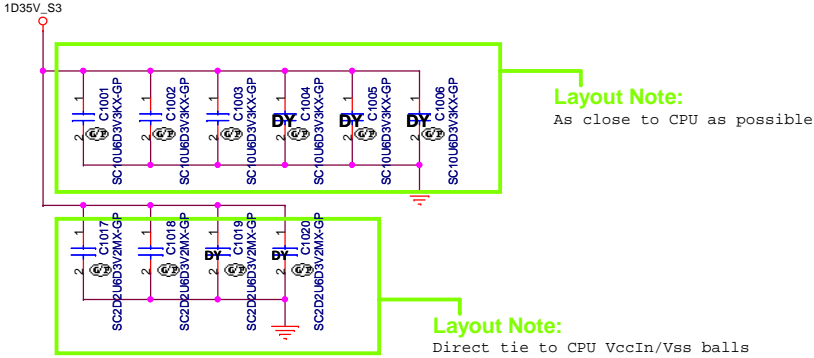
Document Number
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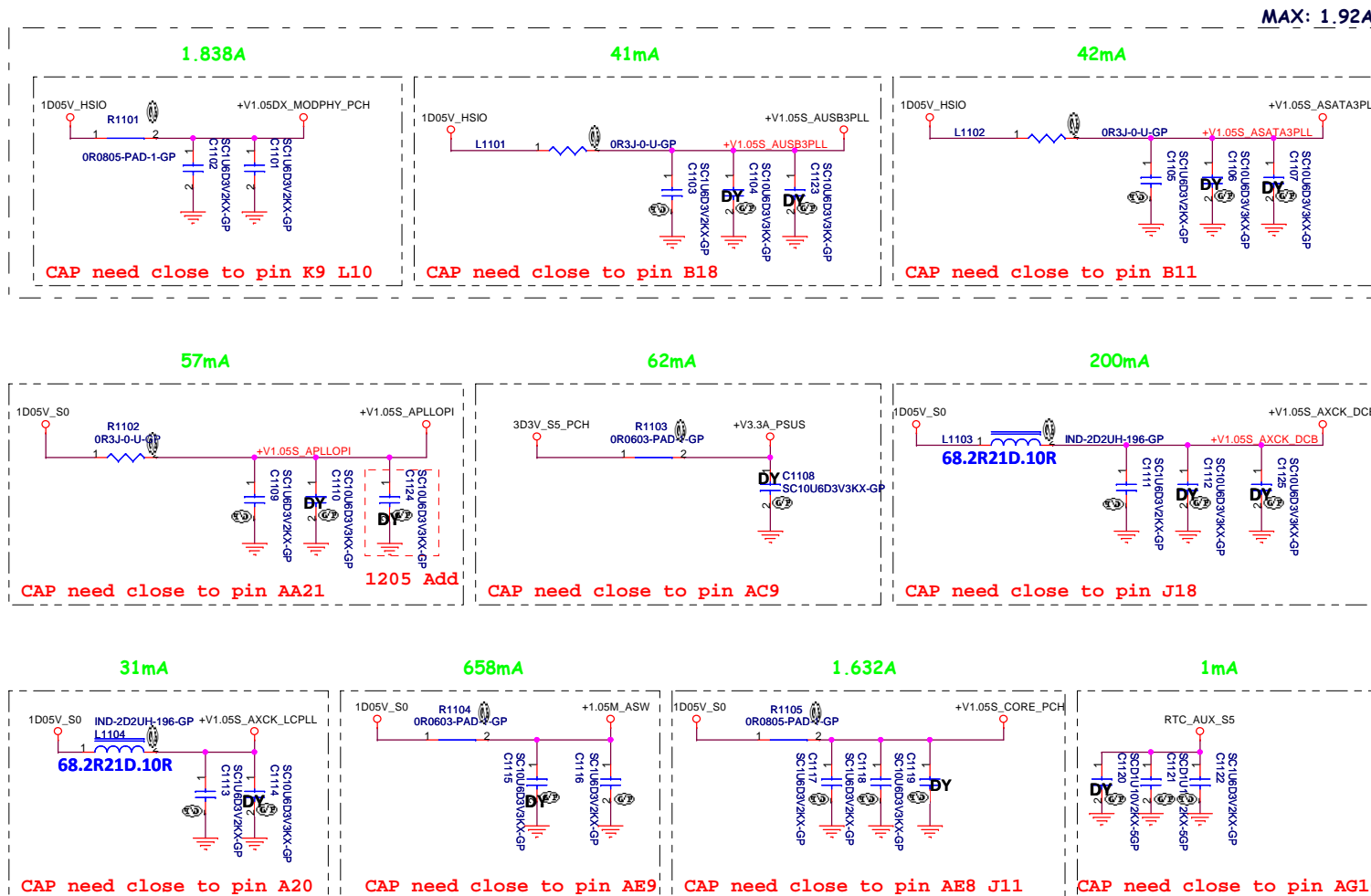
**OAK14 Haswell**Rev  
**X00**

Date: Thursday, March 07, 2013

Sheet 9 of 104

SSID = CPU





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**Reserved**

Size  
A3

Document Number

**OAK14 Haswell**

Rev

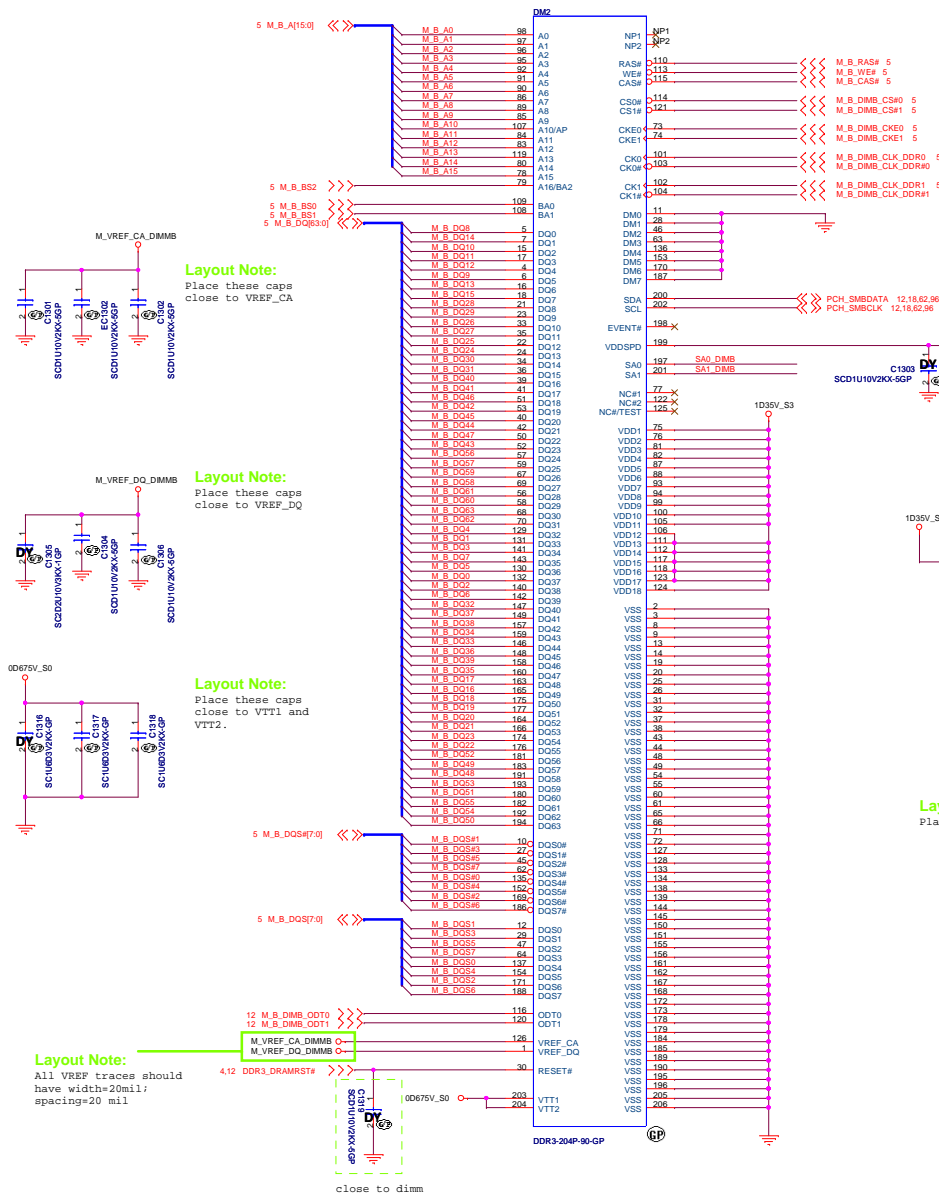
**X00**

Date: Wednesday, May 15, 2013

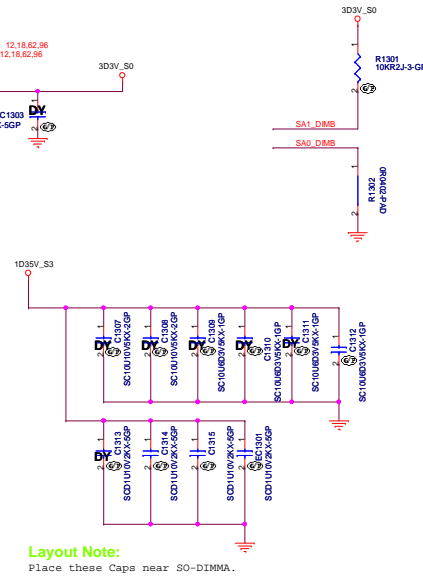
Sheet 11 of 104



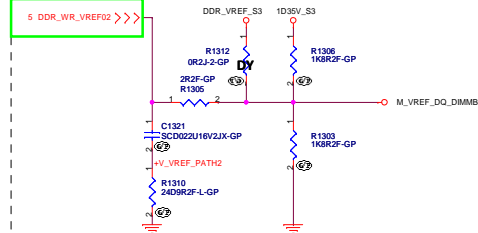
## SSID = MEMORY

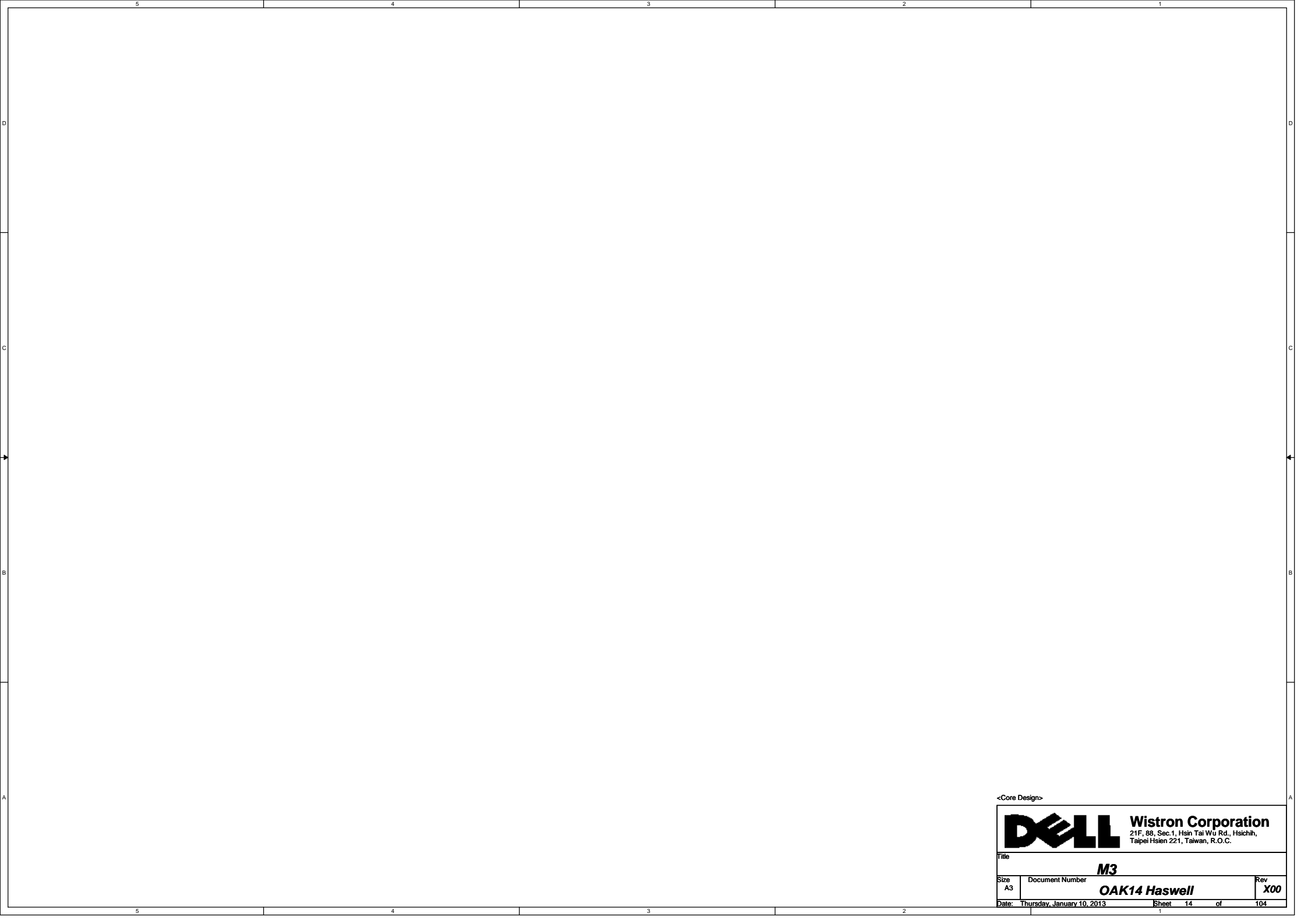


**Note:**  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34




**Layout Note:**  
Place Close SO-DIMMA.





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Title			
<b>M3</b>			
Size	Document Number		Rev
A3	<b>OAK14 Haswell</b>		<b>X00</b>
Date:	Thursday, January 10, 2013		Sheet 14 of 104



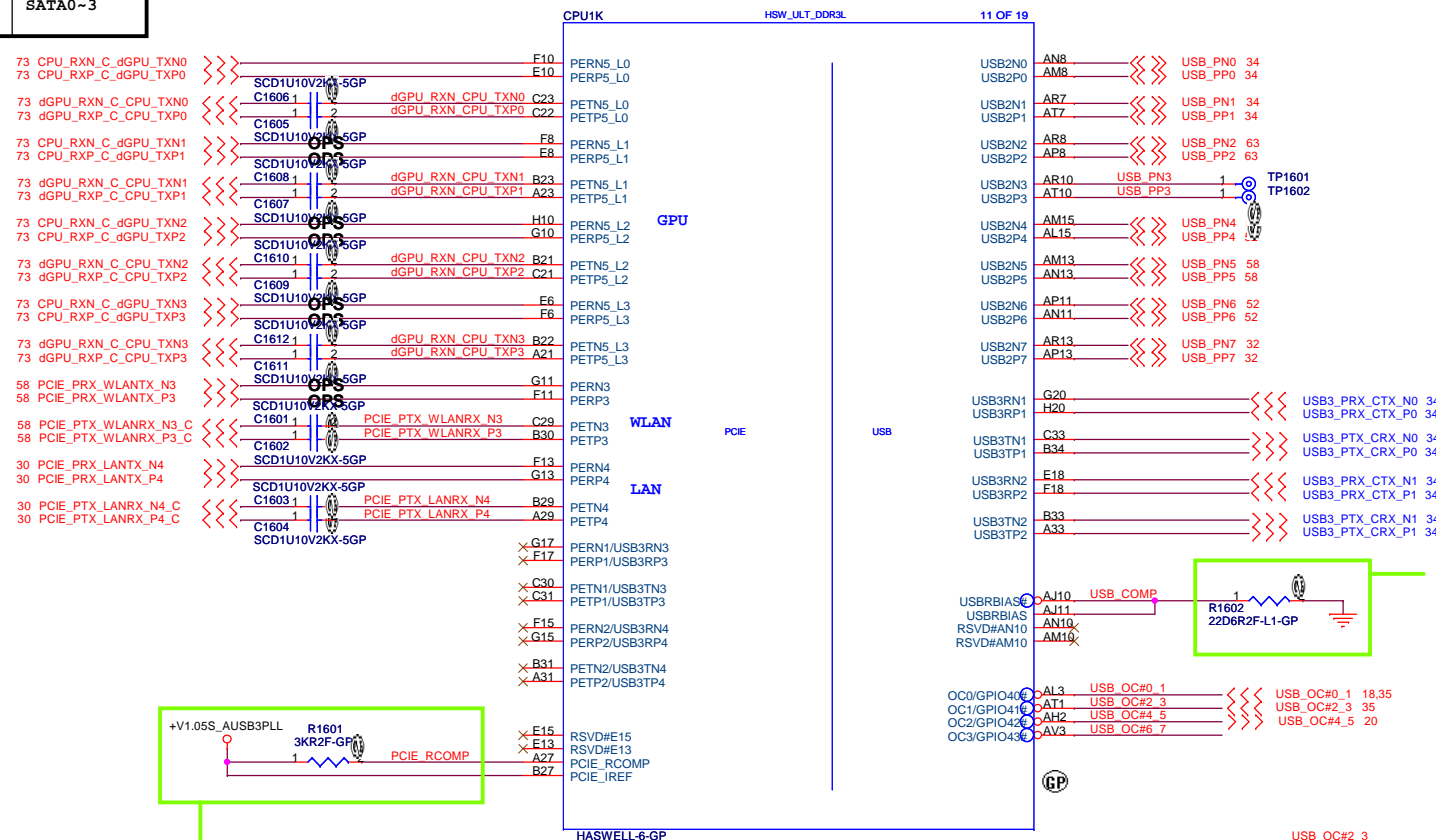
SSID = PCH

## PCIE Table

Port	Device	Share BUS
1	TBD	USB3.0_3
2	TBD	USB3.0_4
3	WLAN	
4	LAN	
5(4lane)	GPU	
6(4lane)	TBD	SATA0~3

## USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2
2	USB2.0 Port3
3	TBD
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader



### Layout Note:

1. PCIE\_RCOMP/ PCIE\_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

### Layout Note:

1. USB\_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

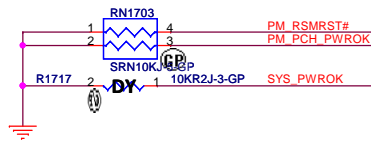
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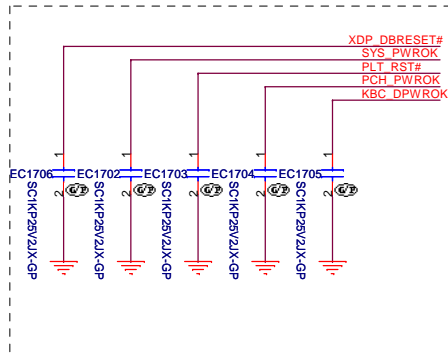
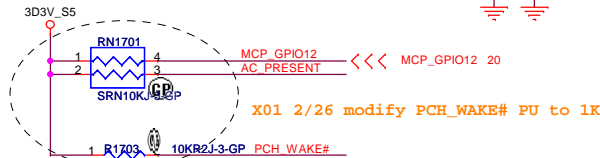
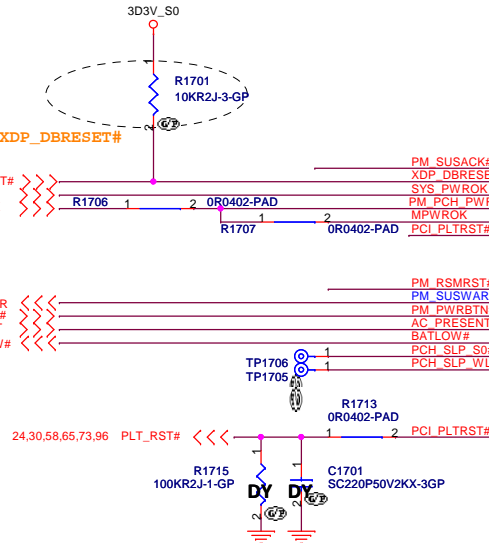
Title			PCH (PCIE/USB)		
Size	Document Number	Rev			
A3	OAK14 Haswell	X00			
Date:	Thursday, March 07, 2013	Sheet	16	of	104



**SSID = PCH**



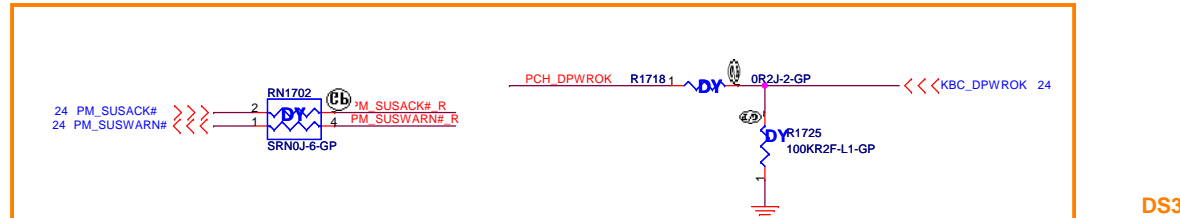
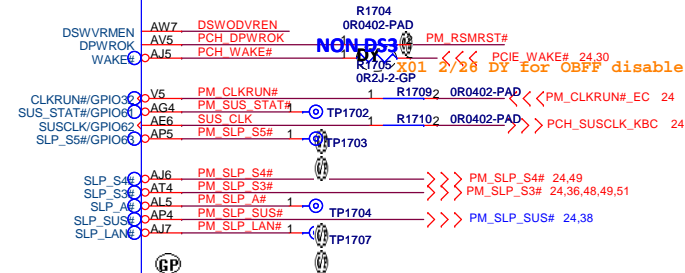
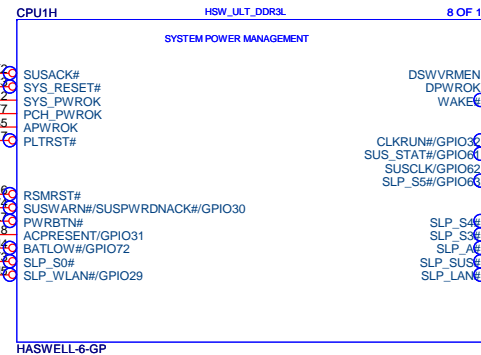
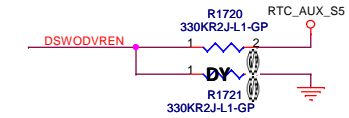
X01 2/26 Add PH 10K on XDP\_DBRESET#



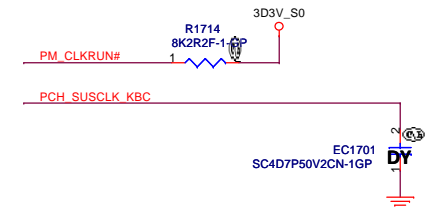
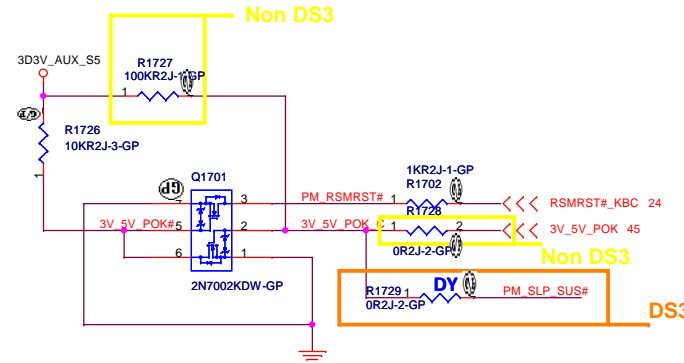
EMI 12/20

**PCH strap pin:**

On Die DSW VR Enable	
DSWODVREN	Low = Disable * High = Enable (default)



DS3



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**PCH (PM)**

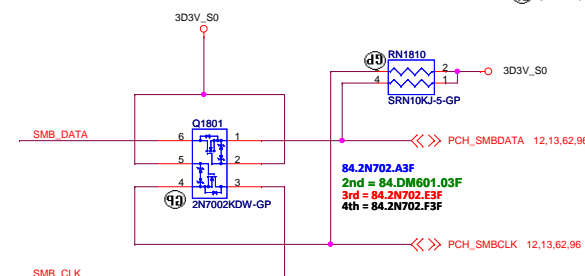
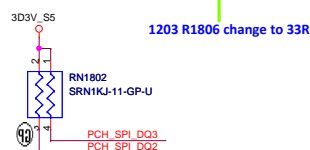
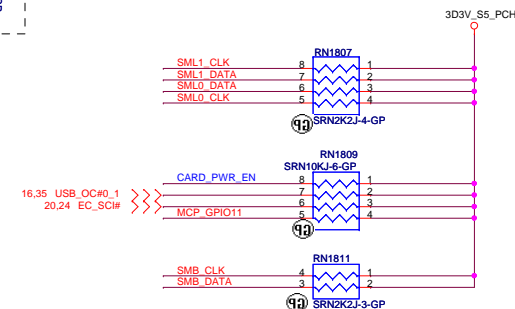
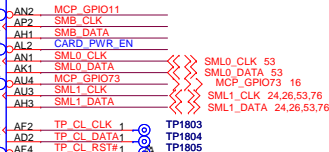
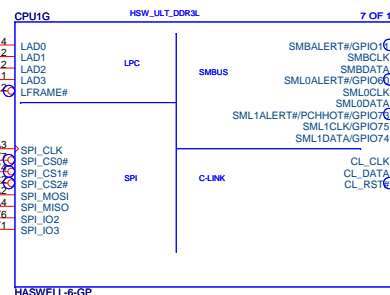
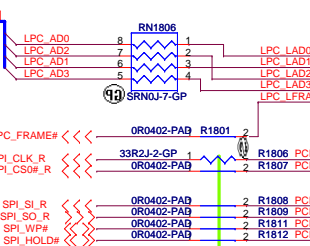
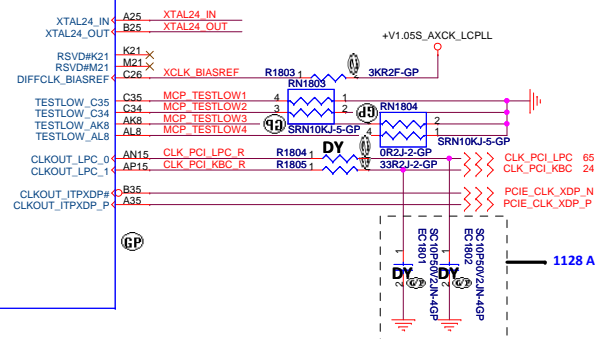
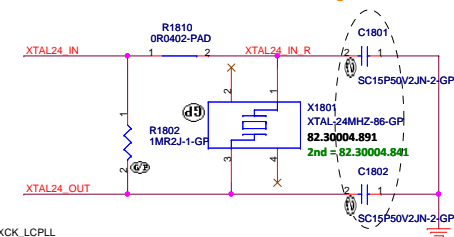
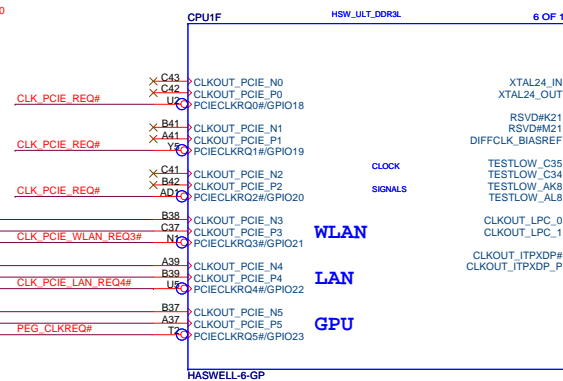
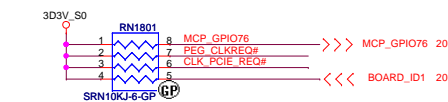
**OAK14 Haswell**

Rev	<b>X00</b>
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Date: Monday, June 03, 2013

Sheet 17 of 104

**SSID = PCH**



&lt;Core Design&gt;

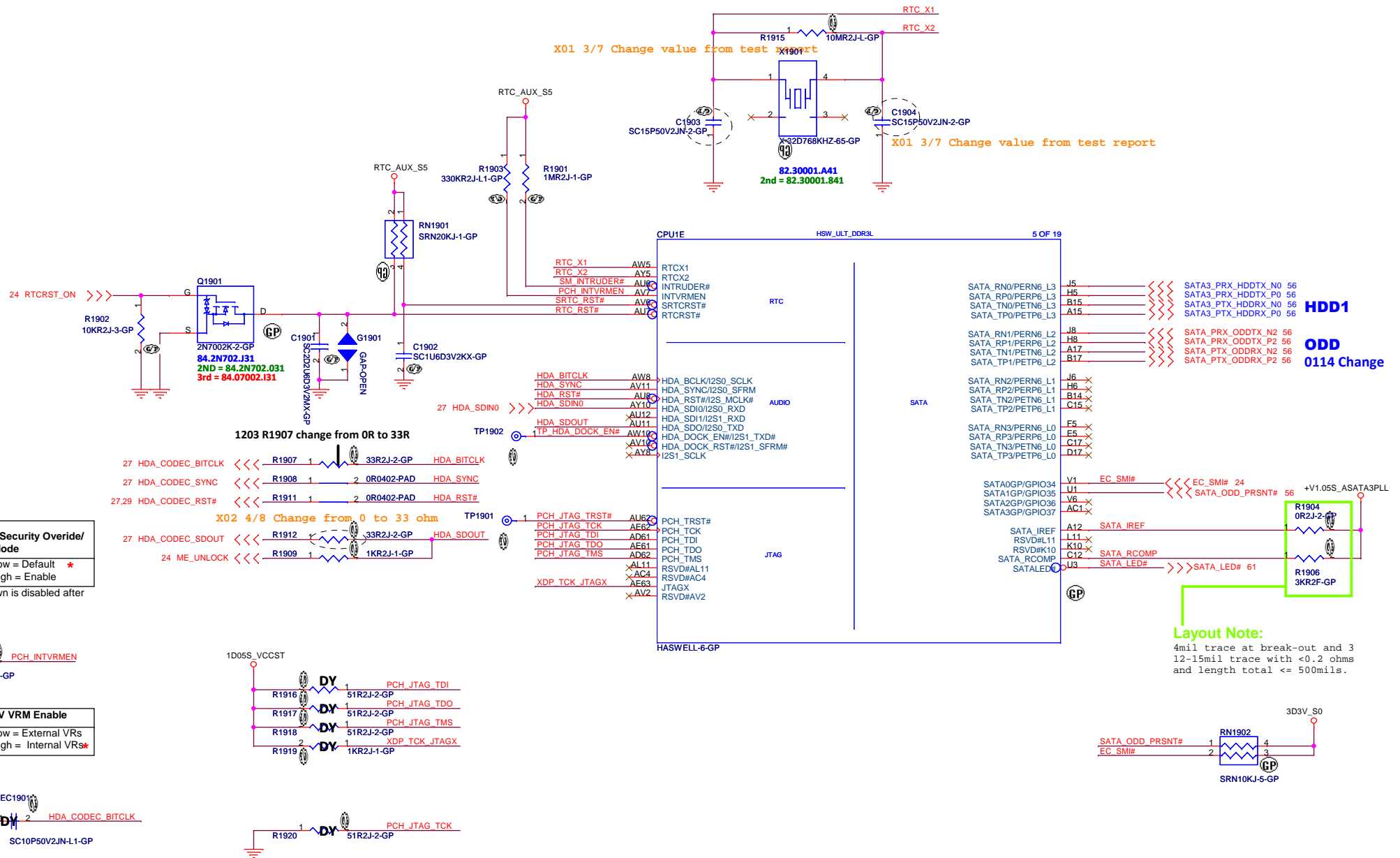


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Title  
**PCH (CLOCK/SMBUS/CL/LPC/SPI)**

Size	Document Number	Rev
Custom	<b>OAK14 Haswell</b>	<b>X</b>
Date:	Wednesday, April 17, 2013	Sheet 18 of 104

SSID = CPU



## <Core Design>



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Title

### PCH (RTC/SATA/HDA/JTAG)

Size  
A


Document Number

**OAK14 Haswell**Rev  
X00

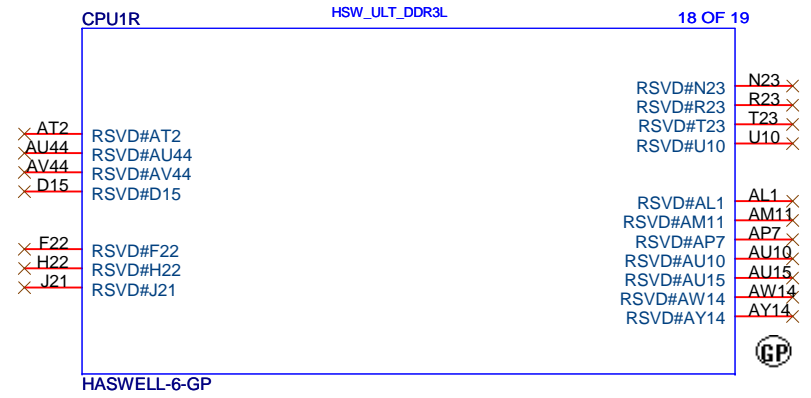
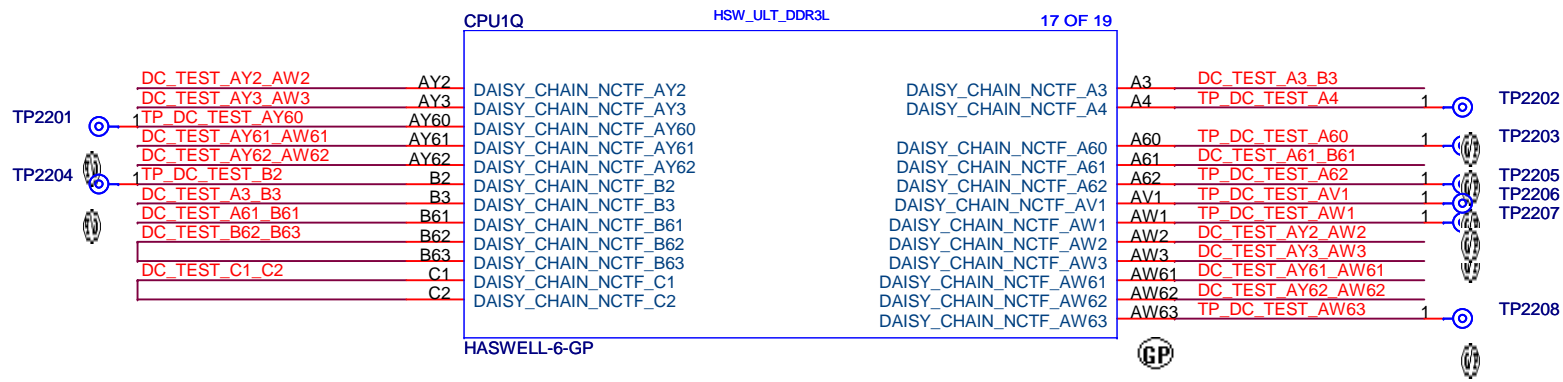
Date: Thursday, April 25, 2013

Sheet 19 of 104



<div> <div>  <div> <b>Wistron Corporation</b>            2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,            Taipei Hsien 221, Taiwan, R.O.C.         </div> </div> </div>			
Title			
<div> <div>CPU (POWER2)</div> <div> <div>Size A3</div> <div>Document Number</div> <div>Rev</div> </div> </div>			
<div> <div>OAK14 Haswell</div> <div>X00</div> </div>			
Date: Monday, June 03, 2013	Sheet	21 of	104

SSID = PCH



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Title

(Reserved)

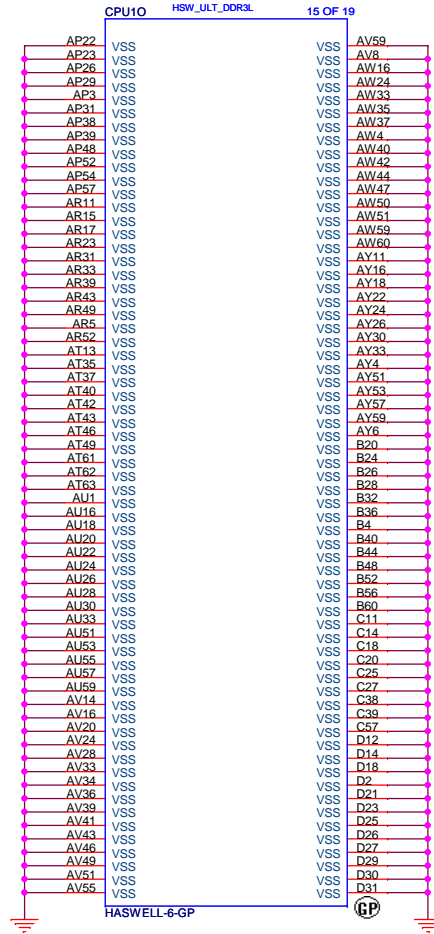
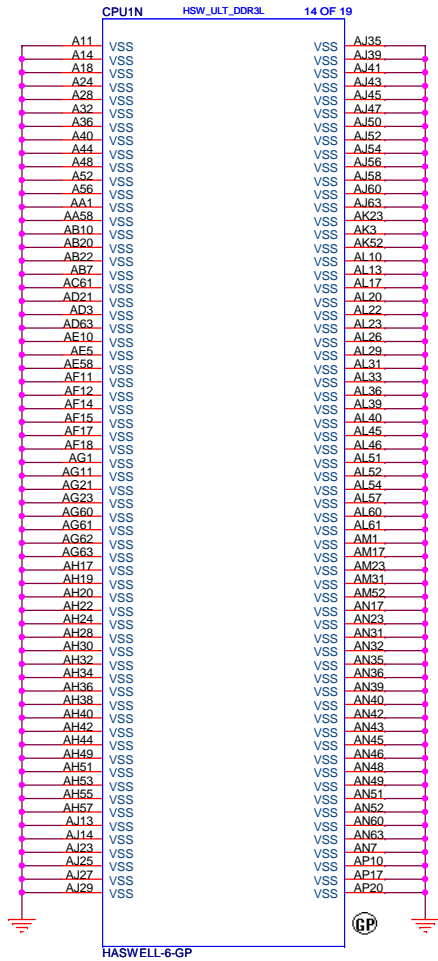
SizeA4

Document Number

RevX00

Date: Thursday, January 10, 2013Sheet 22 of 104

SSID = PCH



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Title

(Reserved)

Size  
A3

Document Number

**OAK14 Haswell**

Rev

**X00**

Date: Thursday, January 10, 2013

Sheet 23 of 104

D

C

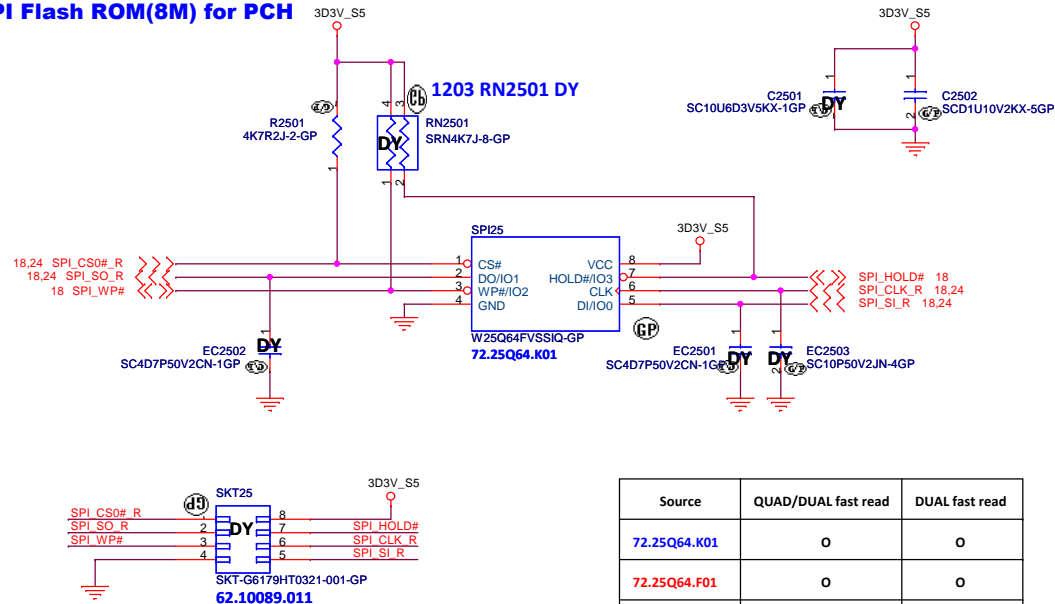
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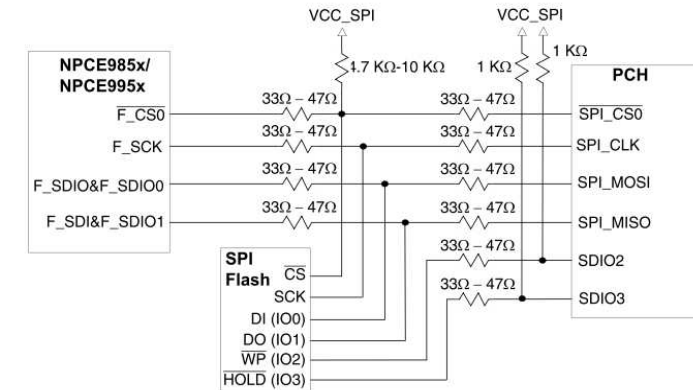
SSID = Flash.ROM

### SPI Flash ROM(8M) for PCH



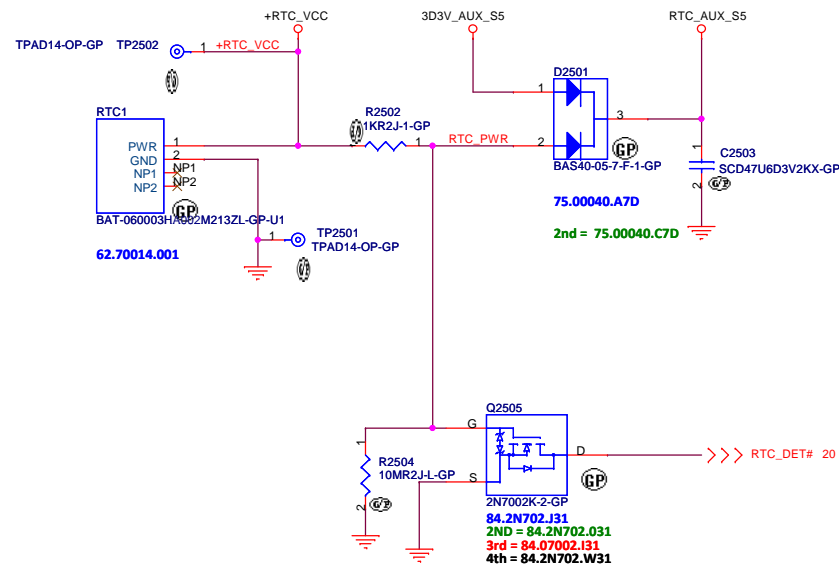
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25Q64.F01	O	O
72.25Q64.D01	O	O

### Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT



## <Core Design>



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Title

**Flash/RTC**Size  
A3

Document Number
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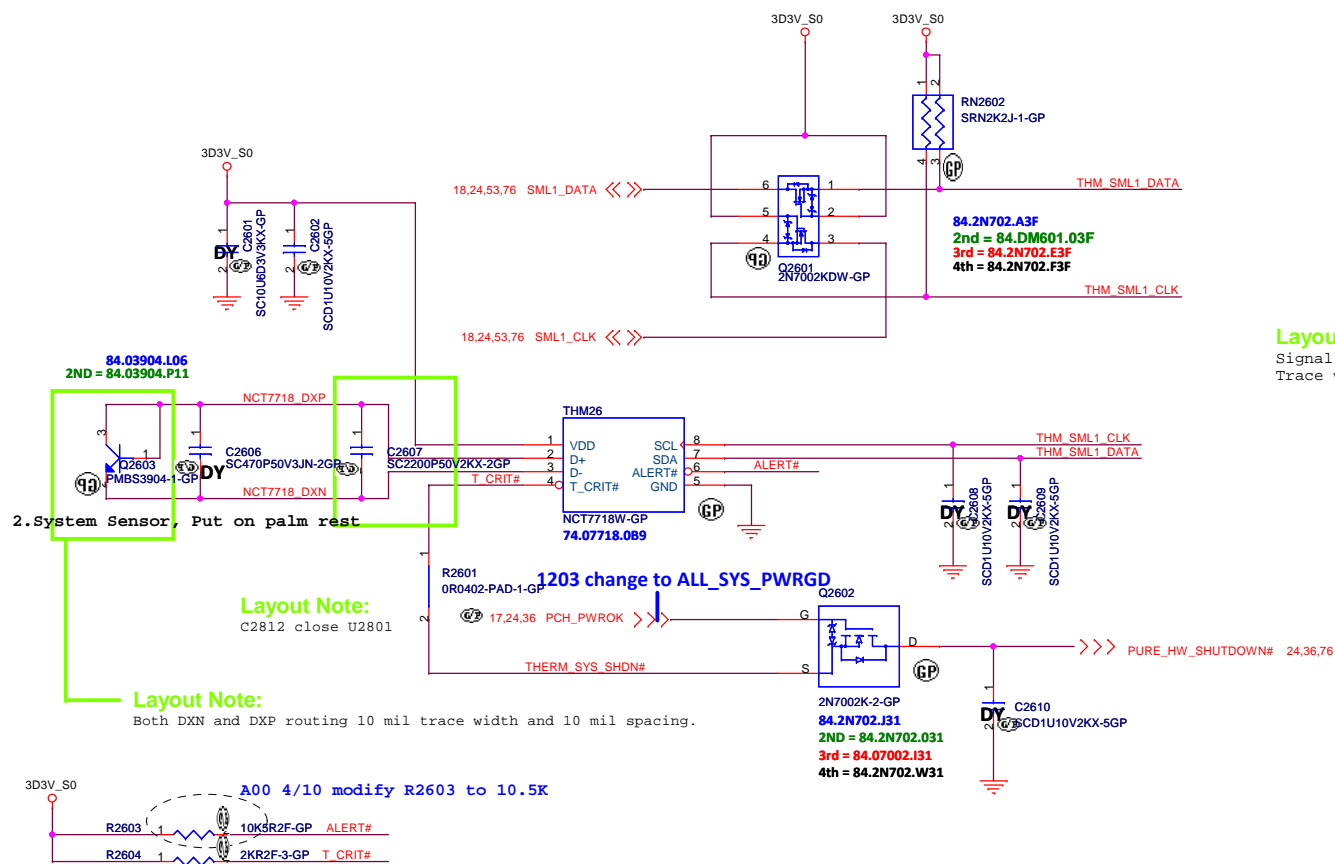
**OAK14 Haswell**

Rev	X00
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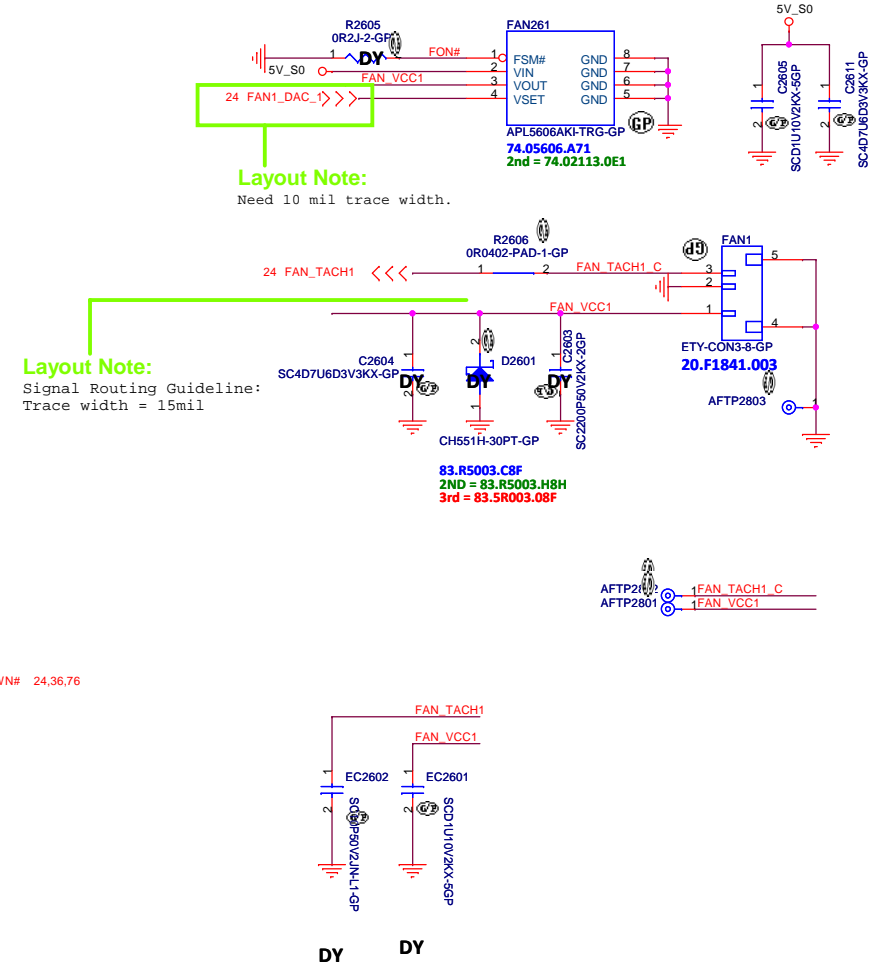
Date: Monday, June 03, 2013

Sheet 25 of 104

SSID = Thermal

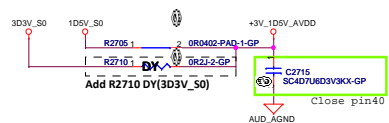
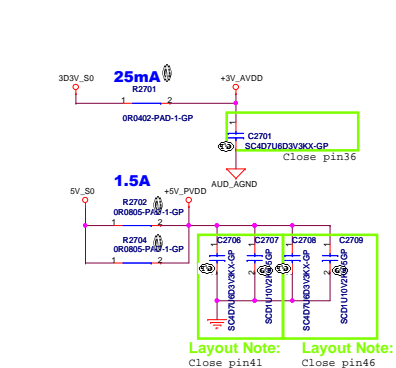
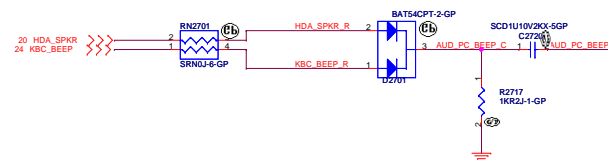
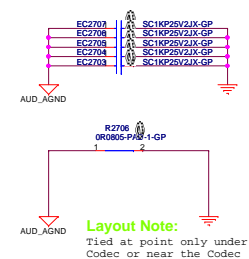
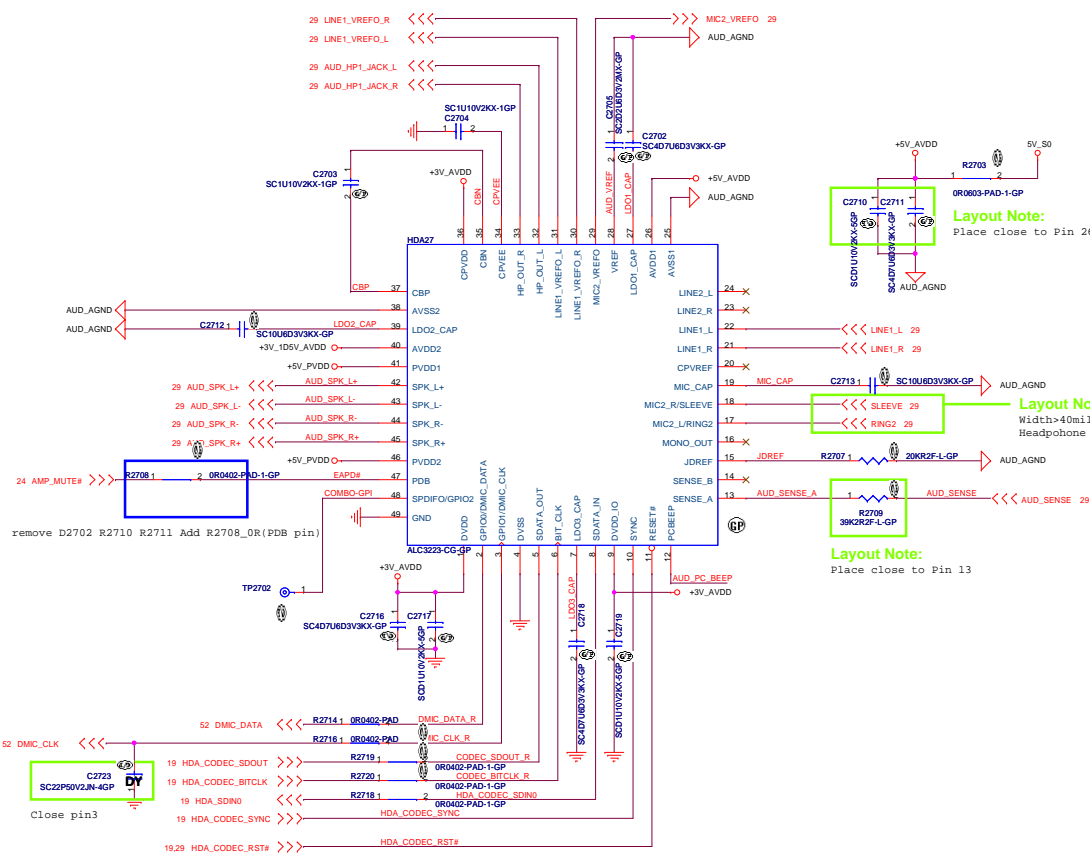
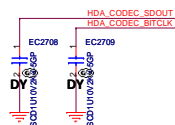


## Fan controller1



<Core Design>

SSID = AUDIO

**Azalia I/F EMI**

(Blanking)

<Core Design>



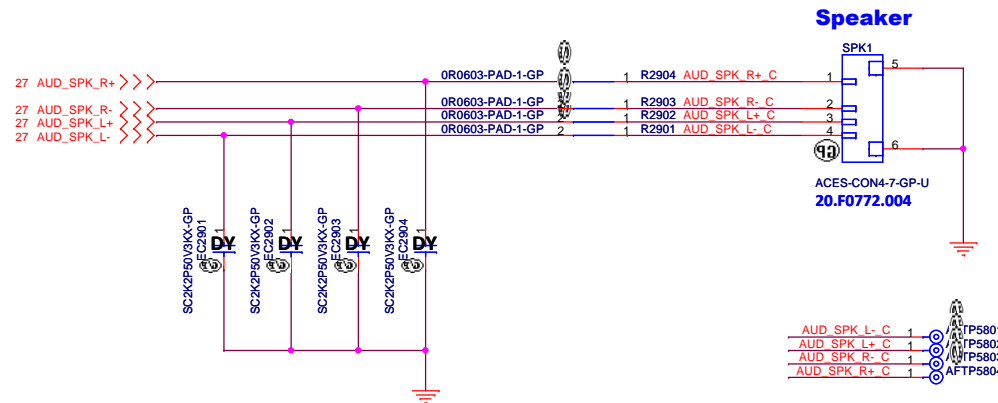
Wistron Corporation  
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Title

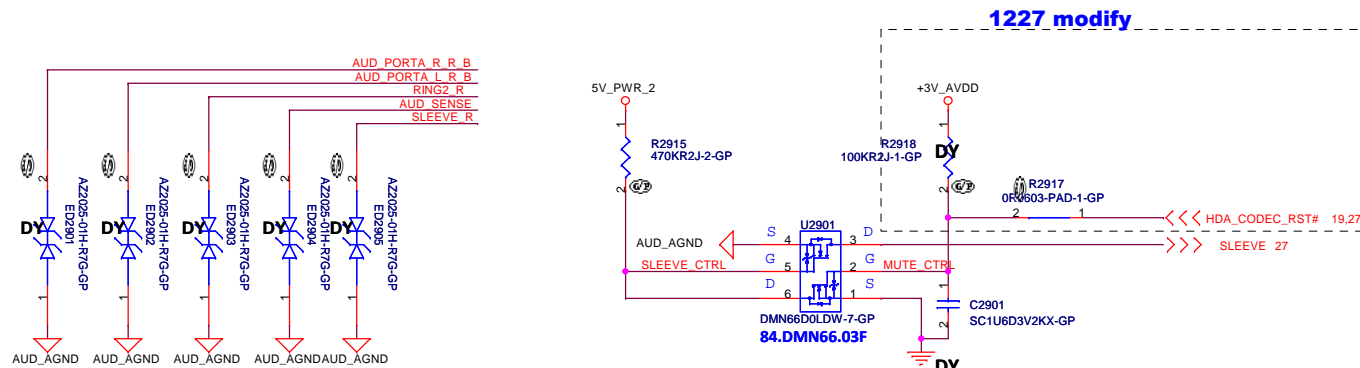
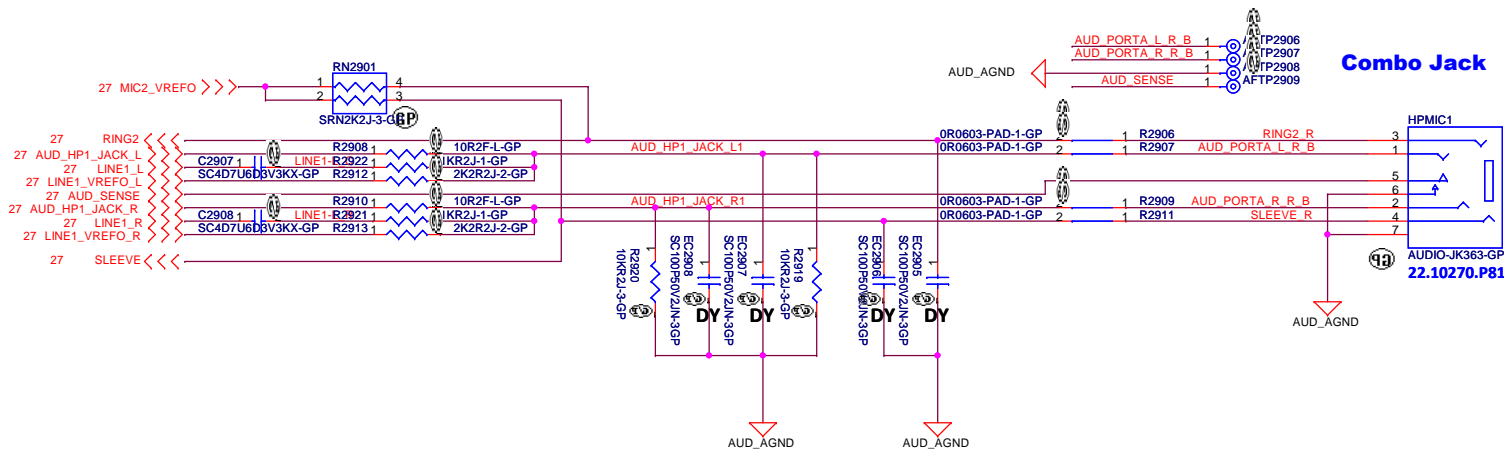
Reserved

Size A3	Document Number OAK14 Haswell	Rev X00
Date: Thursday, January 10, 2013	Sheet 28 of	104

SSID = AUDIO

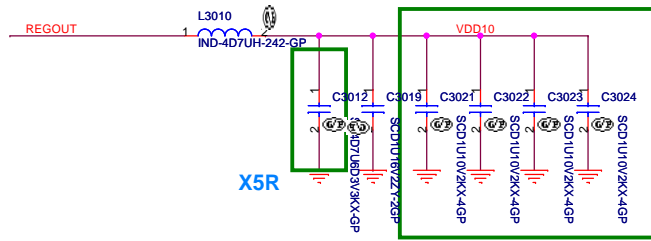


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

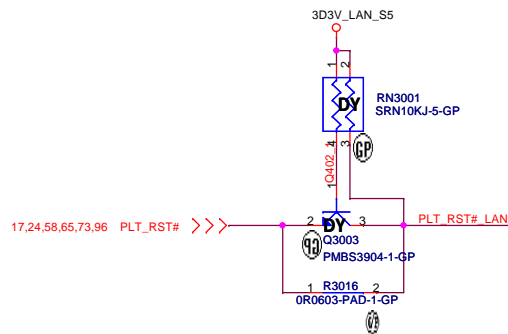
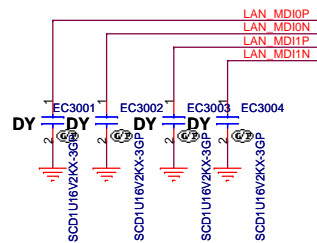
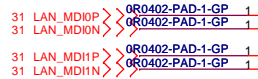
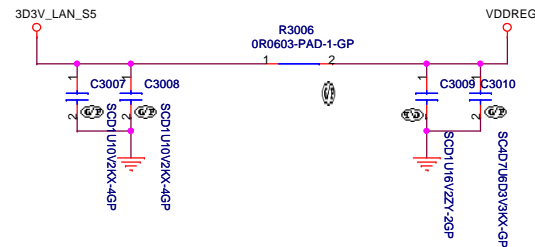


## LAN CHIP

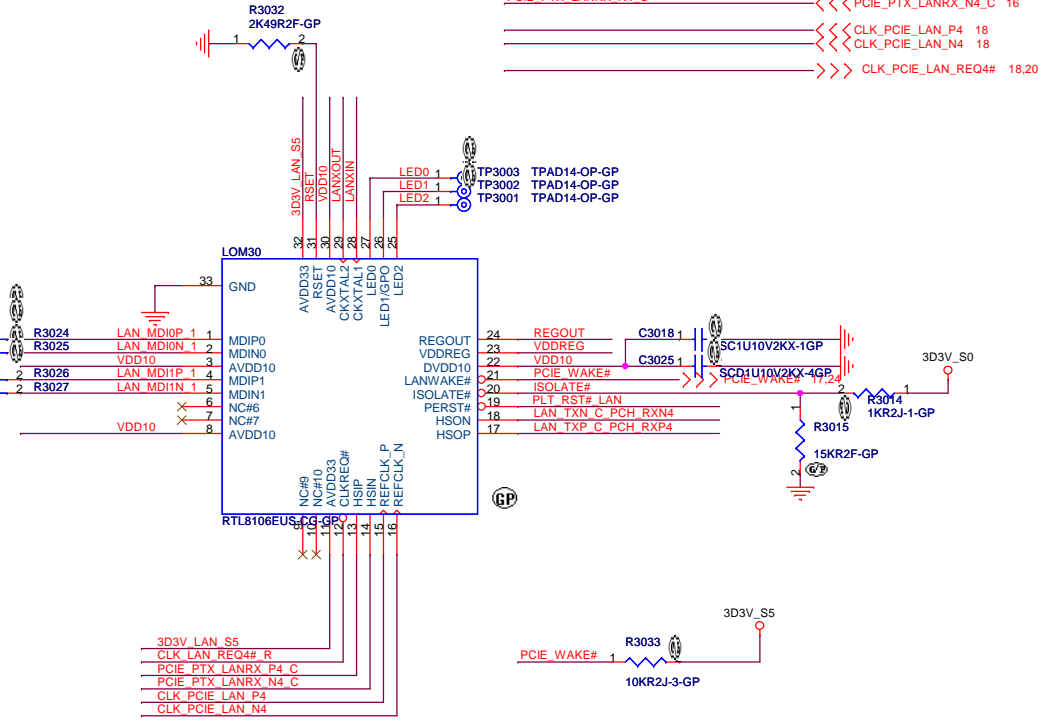
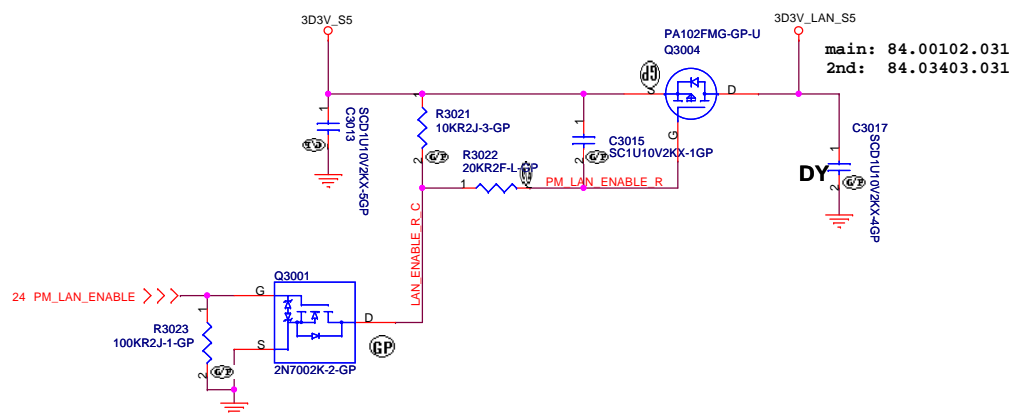
10/100 Need Only need C3021, C3022, C3023, C3024 in Pin3, 8, 22, 30



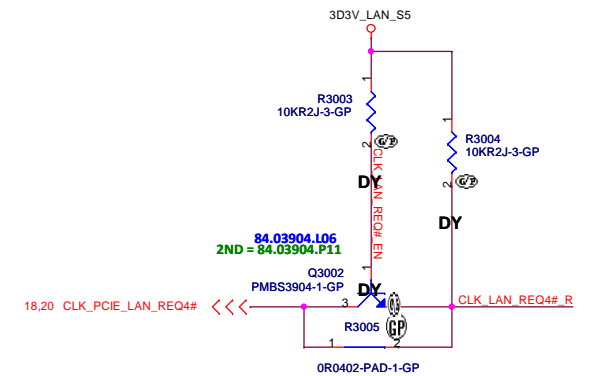
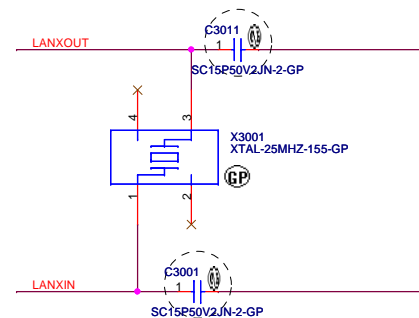
40 mils



251mA



X01 3/7 Change value from test report



## <Core Design>



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Title

**LOM**

Size

Document Number
-----------------

**OAK14 Haswell**

Rev

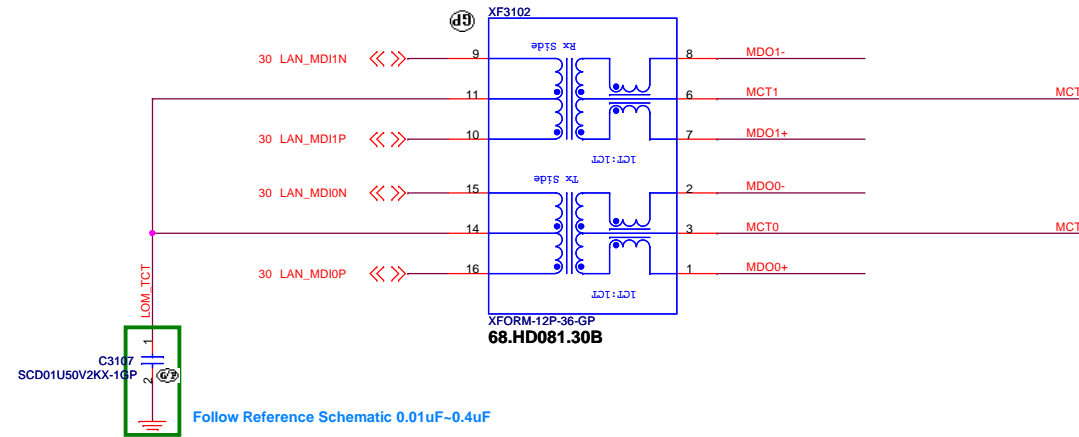
Date: Wednesday, April 17, 2013

Sheet 30

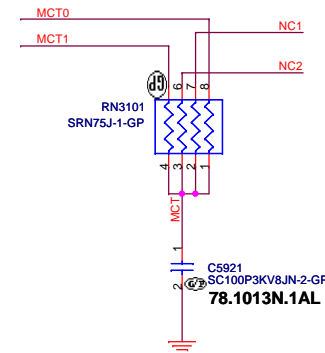
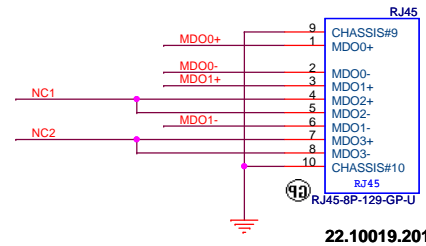
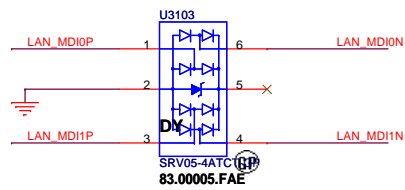
104

SSID = LOM

## 10/100 LAN TransFormer



## RJ45 CONN



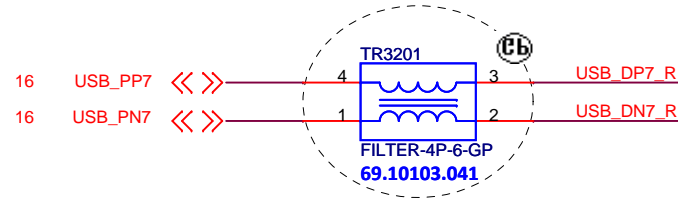
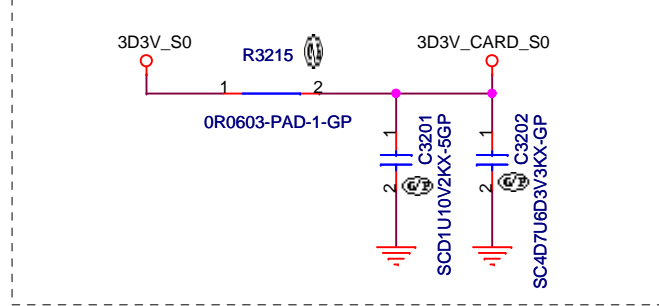
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Taipei Hsien 221, Taiwan, R.O.C.

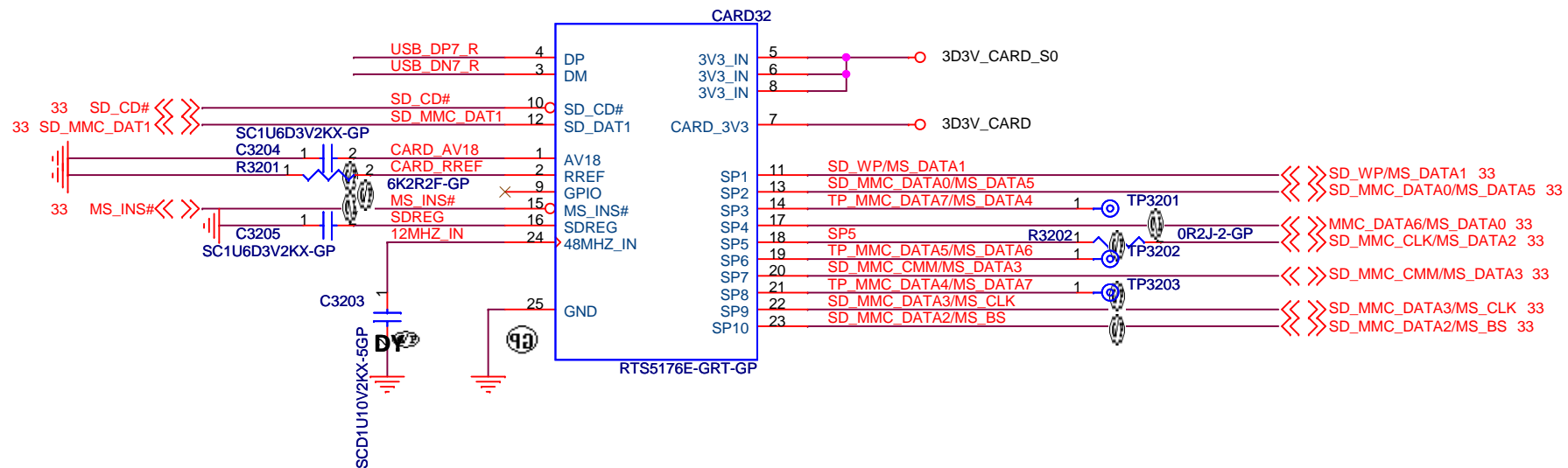
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Size	Document Number	Rev		
A3	<b>OAK14 Haswell</b>	<b>X00</b>		
Date:	Monday, April 15, 2013	Sheet	31	of 104

## 1121 remove Switch(No support D3 cold)



A00 4/10 Add TR3201

Pin name	Net name
SD_DAT1	SD_MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD_MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD_MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD_MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD_MMC_DATA3/MS_CLK
SP10	SD_MMC_DATA2/MS_BS

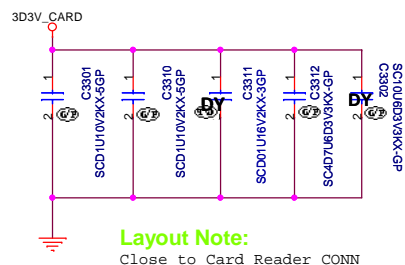


<Core Design>

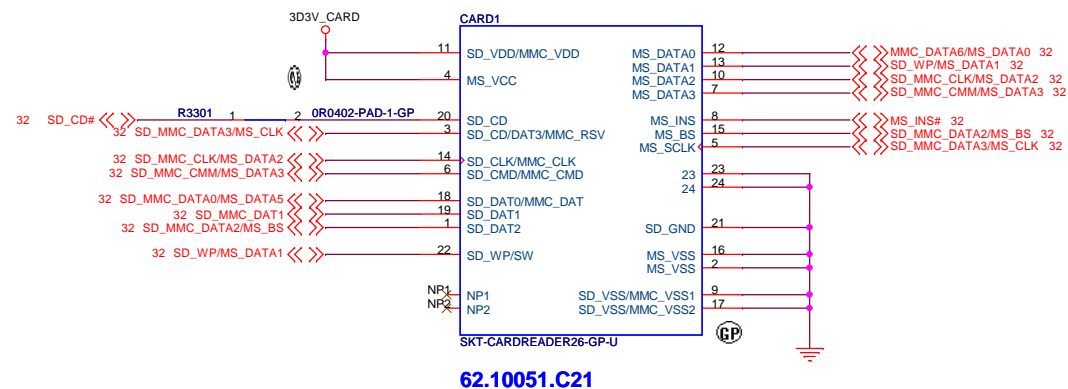
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <b>Card Reader-RTS5176</b>	
Size A4	Document Number <b>OAK14 Haswell</b>		Rev <b>X00</b>
Date: Wednesday, April 17, 2013		Sheet 32 of 104	



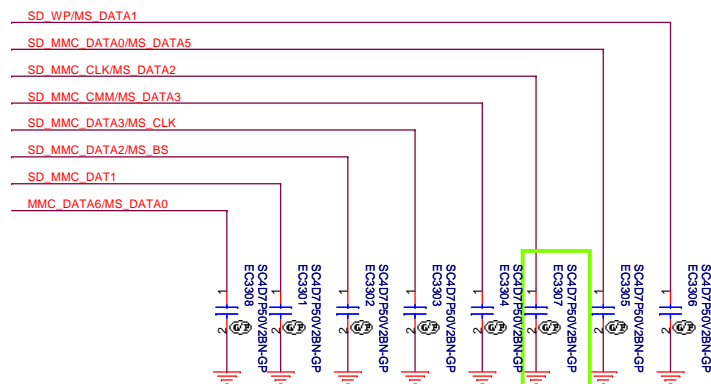
SSID = SDIO



SD/MS/MMC Card Connector



For EMI Reserved



Layout Note:  
please close U3201

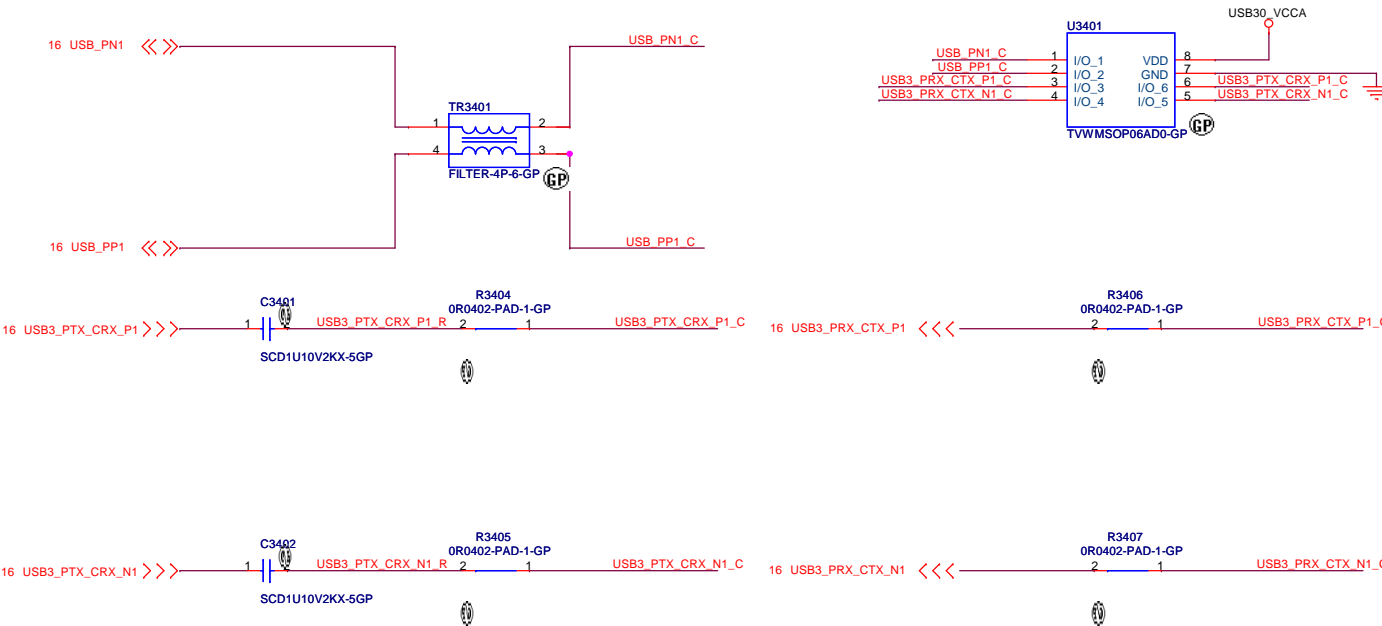
1203 modify 10P change to 4.7P

<Core Design>

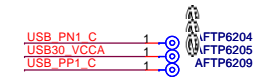
**DELL** Wistron Corporation  
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Title			SD/XD/MS/MMC Card CONN	
Size	Document Number	Rev		
A3	OAK14 Haswell	X00		
Date:	Tuesday, April 16, 2013	Sheet	33	of 104

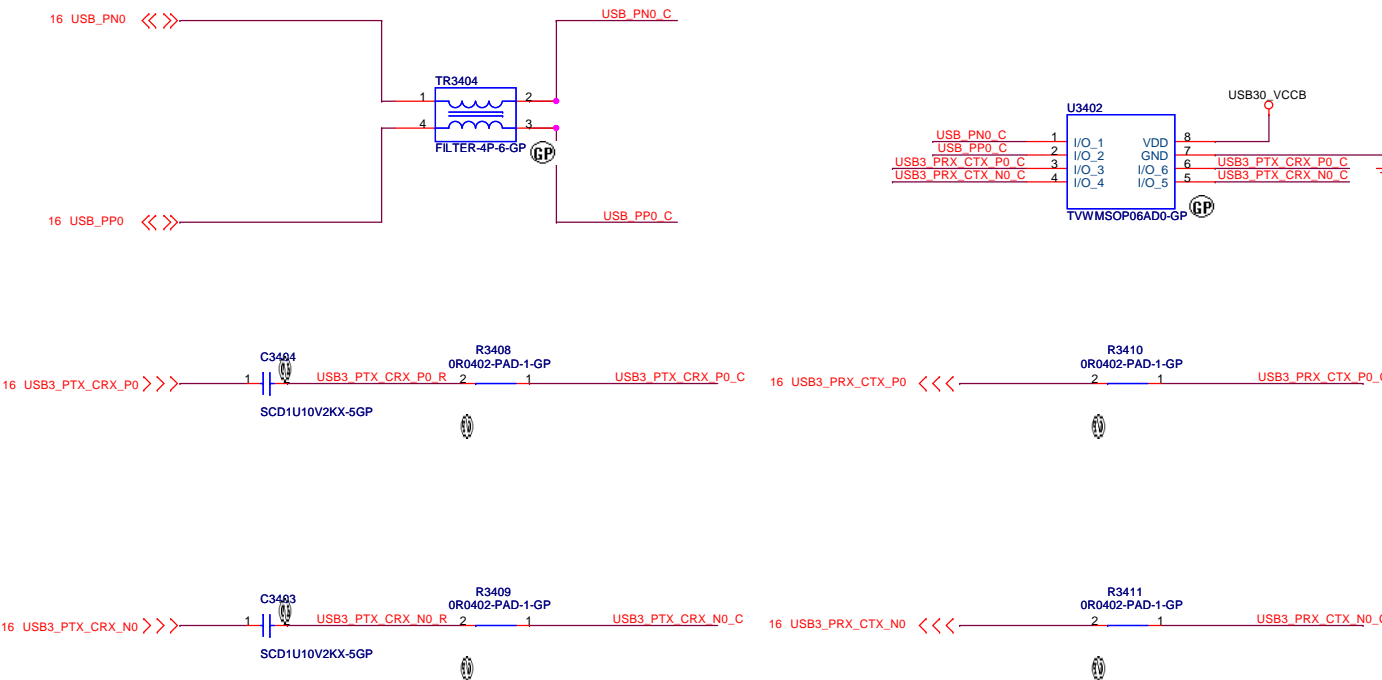
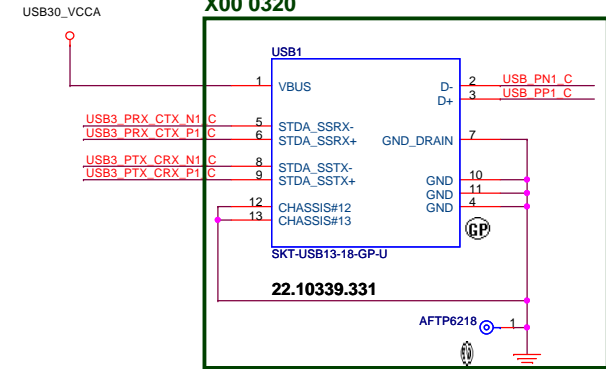
SSID = USB



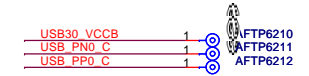
## USB3.0 Port1



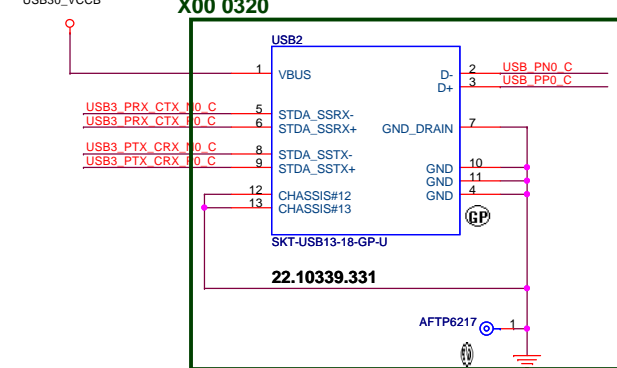
## X00 0320



## USB3.0 Port2



## X00 0320



<Core Design>

**DELL** Wistron Corporation  
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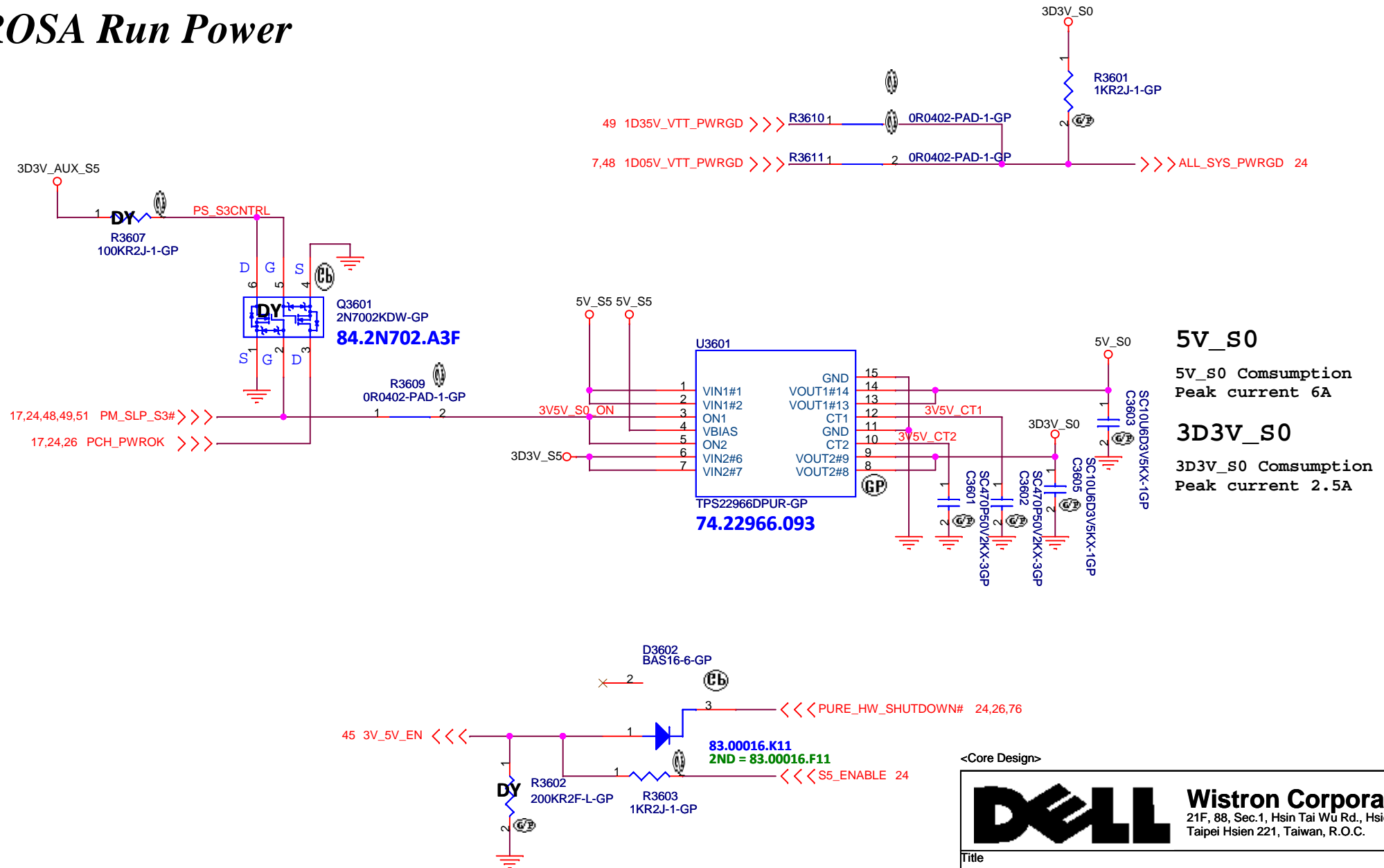
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Size	Document Number	Rev		
A3	<b>OAK14 Haswell</b>	<b>X00</b>		
Date:	Friday, April 12, 2013	Sheet	34	of 104



```
SSID = Reset.Suspend
```

*Power Good*

## ***ROSA Run Power***



## <Core Design>



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Title
-------

## Power Plane Enable

Size

Document Number
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## OAK14 Haswell

Rev

X00

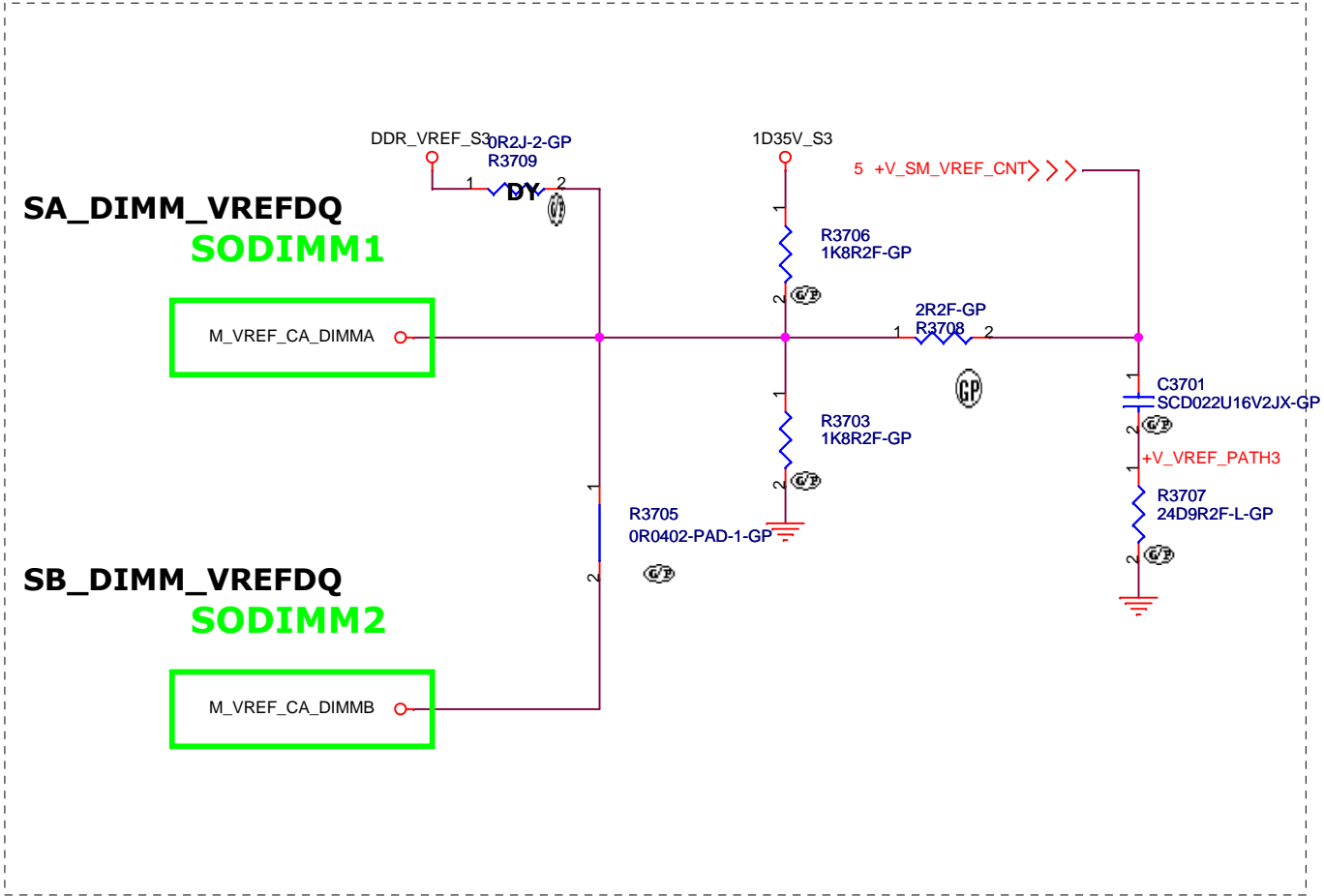
Date: Wednesday, April 17, 2013

Sheet 36 of 104


104

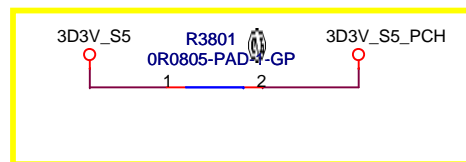
**Layout Note:**

Place Close SO-DIMM

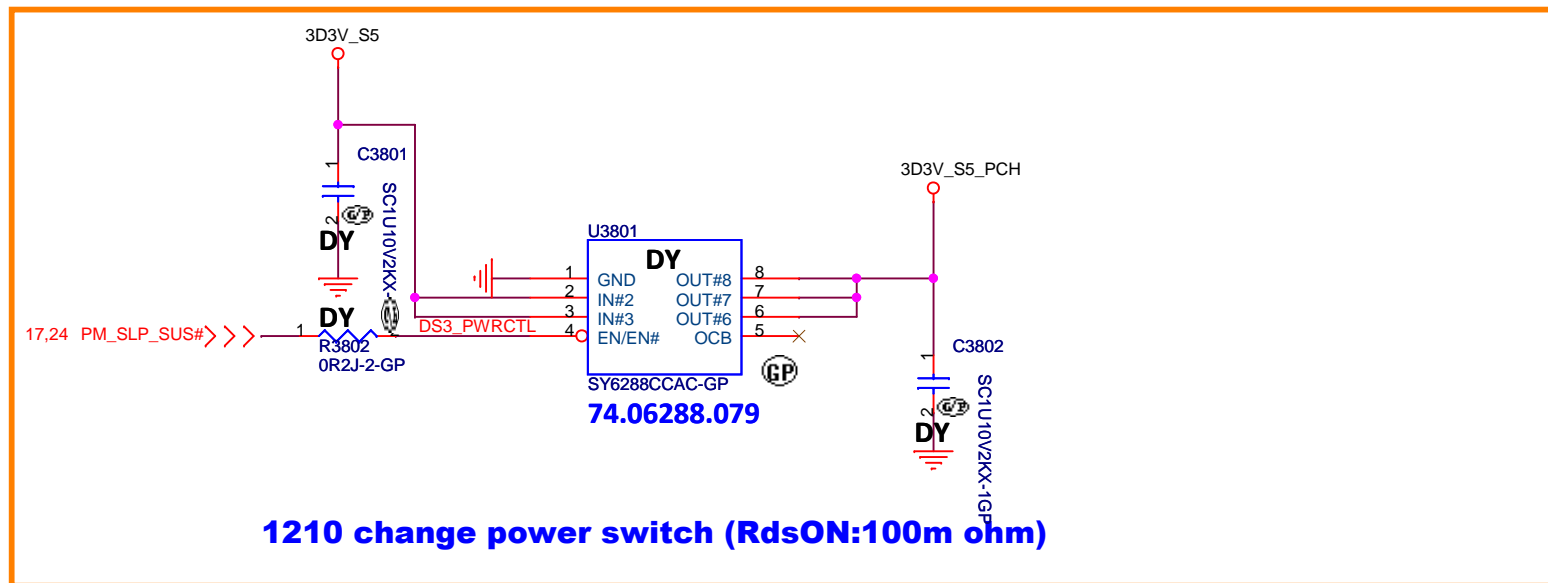


<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>S3 Reduction Circuit</b>			
<b>Size</b> A4	<b>Document Number</b> <b>OAK14 Haswell</b>		<b>Rev</b> <b>X00</b>
<b>Date:</b> Wednesday, April 17, 2013		<b>Sheet</b> 37	<b>of</b> 104




DS3




DS3

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		<b>DSW</b>	
Size A4	Document Number <b>OAK14 Haswell</b>		Rev <b>X00</b>
Date: Monday, June 03, 2013		Sheet 38 of 104	

SSID = CPU

<Core Design>



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Title

**CPU (POWER1)**

Size	Document Number	Rev
Custom	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 39 of 104
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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
A3	<b>OAK14 Haswell</b>		<b>X00</b>
Date: Thursday, January 10, 2013		Sheet 40 of	104



(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

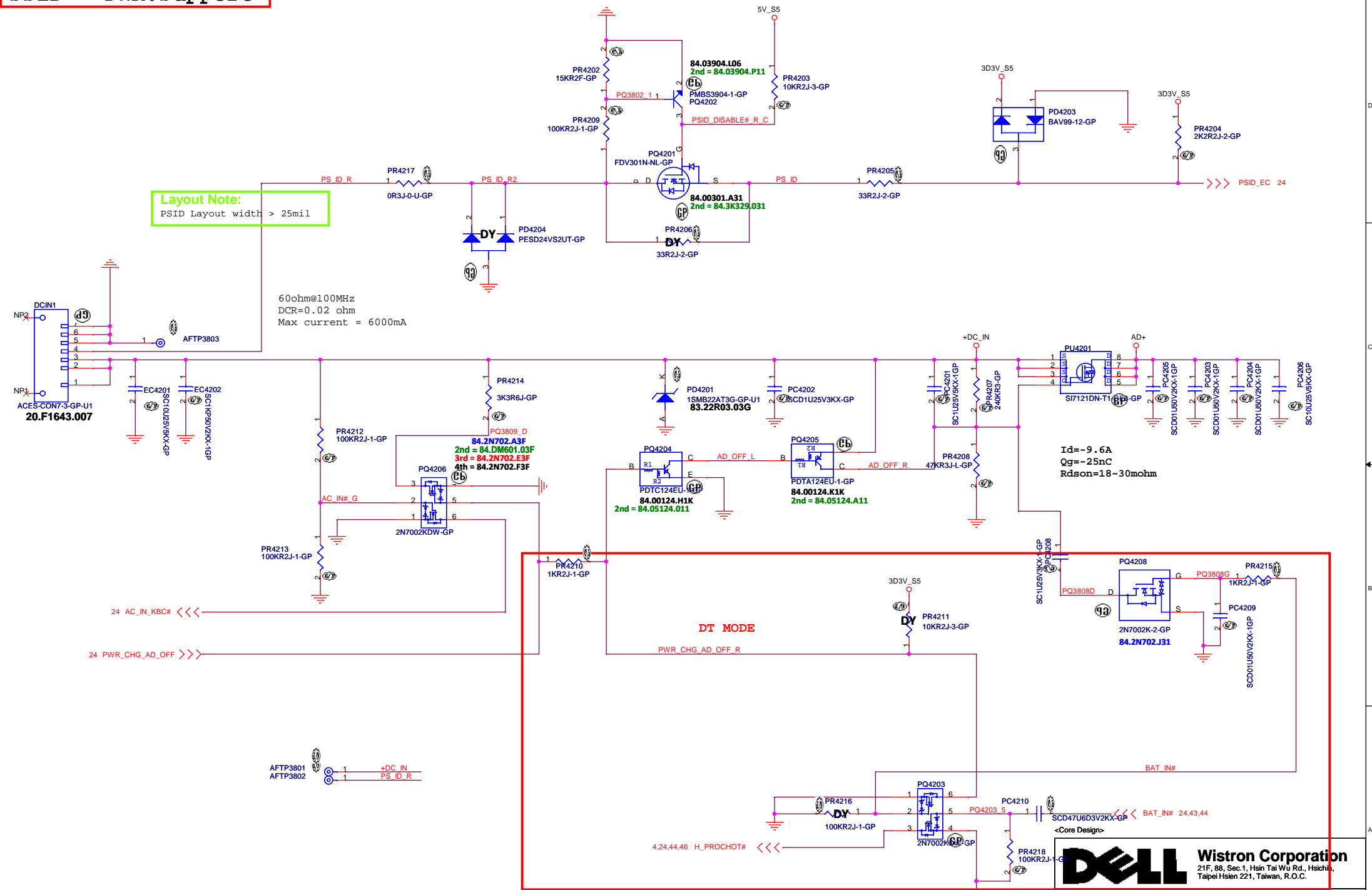
Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 41 of 104
----------------------------------	-----------------

SSID = PWR.Support

**Layout Note:**  
PSID Layout width > 25mil

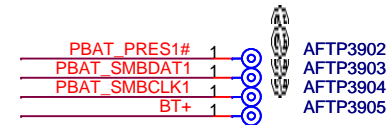
60ohm@100MHz  
DCR=0.02 ohm  
Max current = 6000mA



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Title		
DCIN		
Size	Document Number	Rev
A3	OAK14 Haswell	X00
Date:	Thursday, April 25, 2013	Sheet 42 of 104

```
SSID = PWR.Support
```



**Placement:** Close to Batt Connector



## <Core Design>



Title
-------

## ***BATT CONN***

Size	A4
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Document Number

**OAK14 Haswell**Rev  
***X00***

Date: Thursday, March 07, 2013

Sheet 43 of 104

REGN REGULATOR				
VREGN_RE	G	REGN Regulator Voltage	VVCC = 6.5V, VACDET=0.6V (0-50mA load)	5.5 6 6.5 V

A00 0516 Change PD4405 to short pad

KBC FOR DT MODE  
CHECK EE PULL HIGH

DIS\_DTM:  
H= cell is plus to GND. (reset charger ic)  
L=normal

CHECK EE

BATTERY MON

Close PR4443

CHECK PM BATTERY TYPE  
CHECK CELL for DT mode

Follow customer circuits

CHECK PM ADAPTER TYPE  
And setting adapter type

DIS\_DTM\_HW:  
5V\_S5  
V+=5\*(PR4440/(PR4460+PR4440))+2.73V  
Setting=2.73\*((PR4442+PR4447)/PR4447)+9V

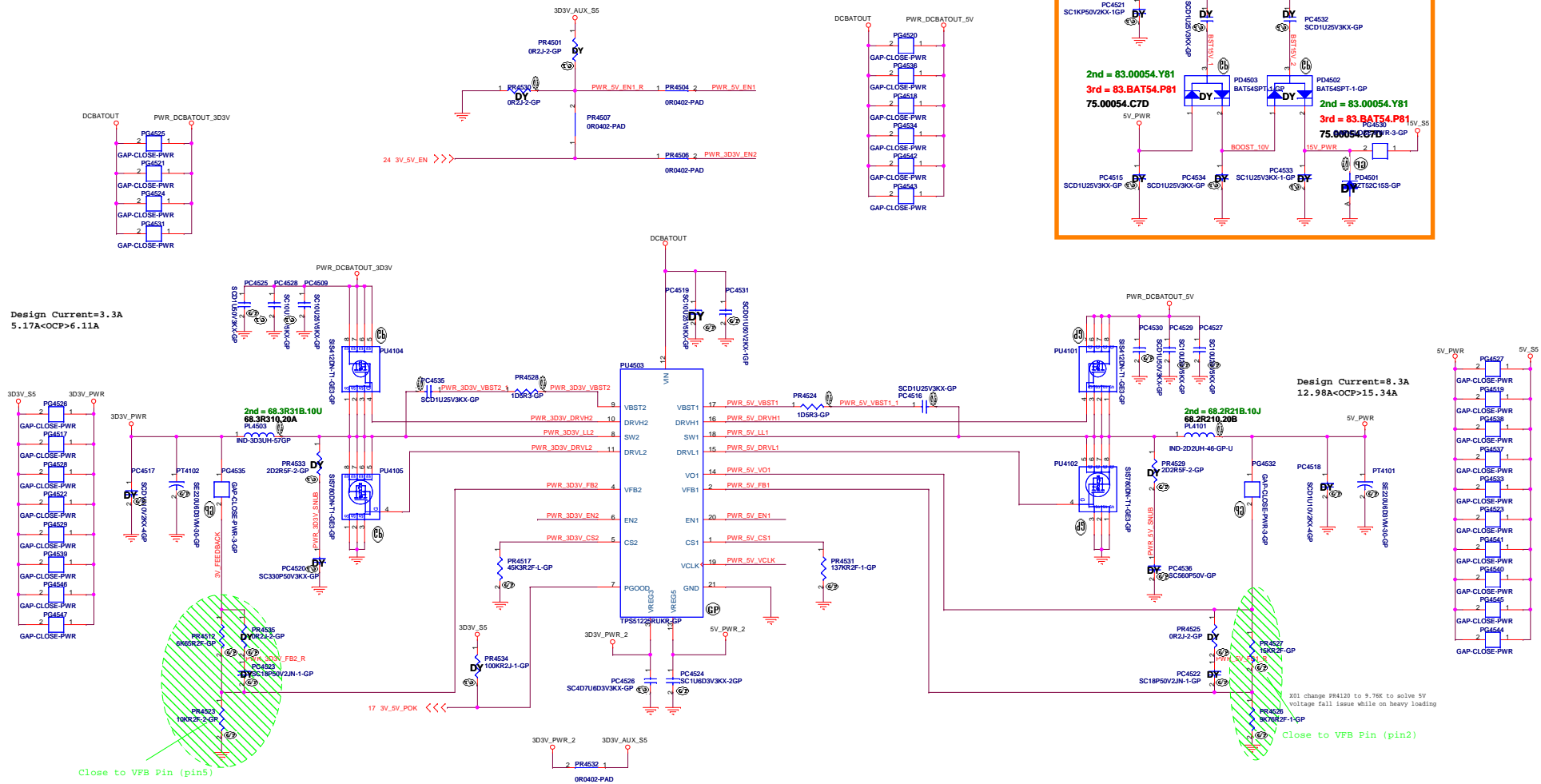
CHECK EE  
follow customer circuits.

ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329V
45W		H	0.659648V

Core Design



```
SSID = PWR.Plane.Regulator_5v3p3v
```



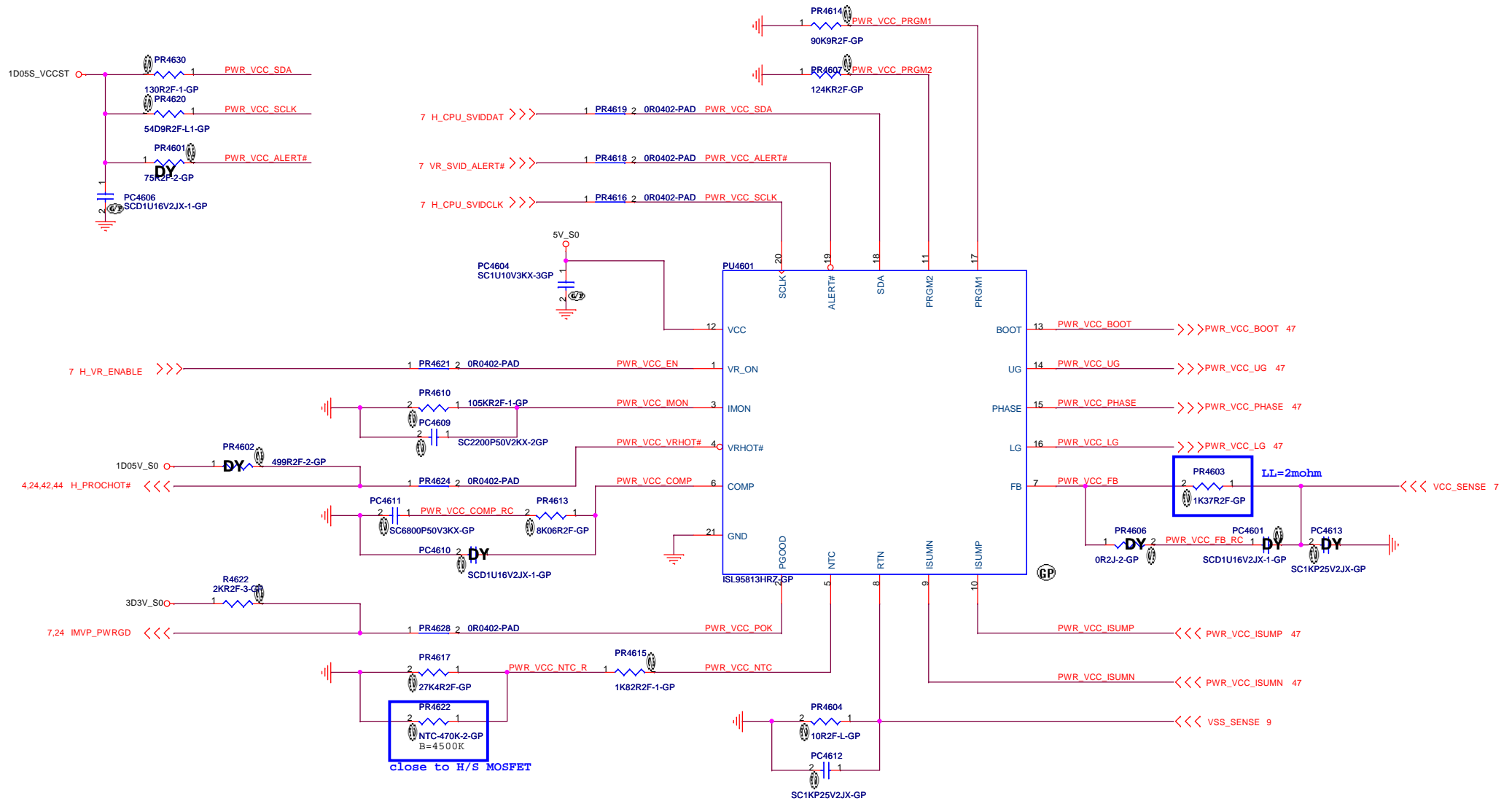
I/P cap: CHIP CAP C 10 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A  
O/P cap:CHIP CAP POL 220U 6.3V M 6.3\*4.5 /Matsuki/ 17mOhm / 77.52271.09L  
H/S:SIS412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037  
L/S:SIS780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037

TPS51225 &amp; TPS51285 Co-lay

	TPS51225	TPS51285
PR4510	45.3KK	9.09K
PR4511	110K	22.1K

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP COLE 2.2U PCMC063T 2\*2MM 18mohm/20mohm Isat =14Arms 68.2R210.20B  
O/P cap:CHIP CAP POK 220U 6.3V M 3\*4.5 /Matsuki/ 17mOhm / 77.52271.09L  
H/S:SIS412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037  
L/S:SIS780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037

SSID = CPU.Regulator



<Core Design>

緯創資通

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Title

**TPS51622 CPUCORE(1/2)**

Size  
A3

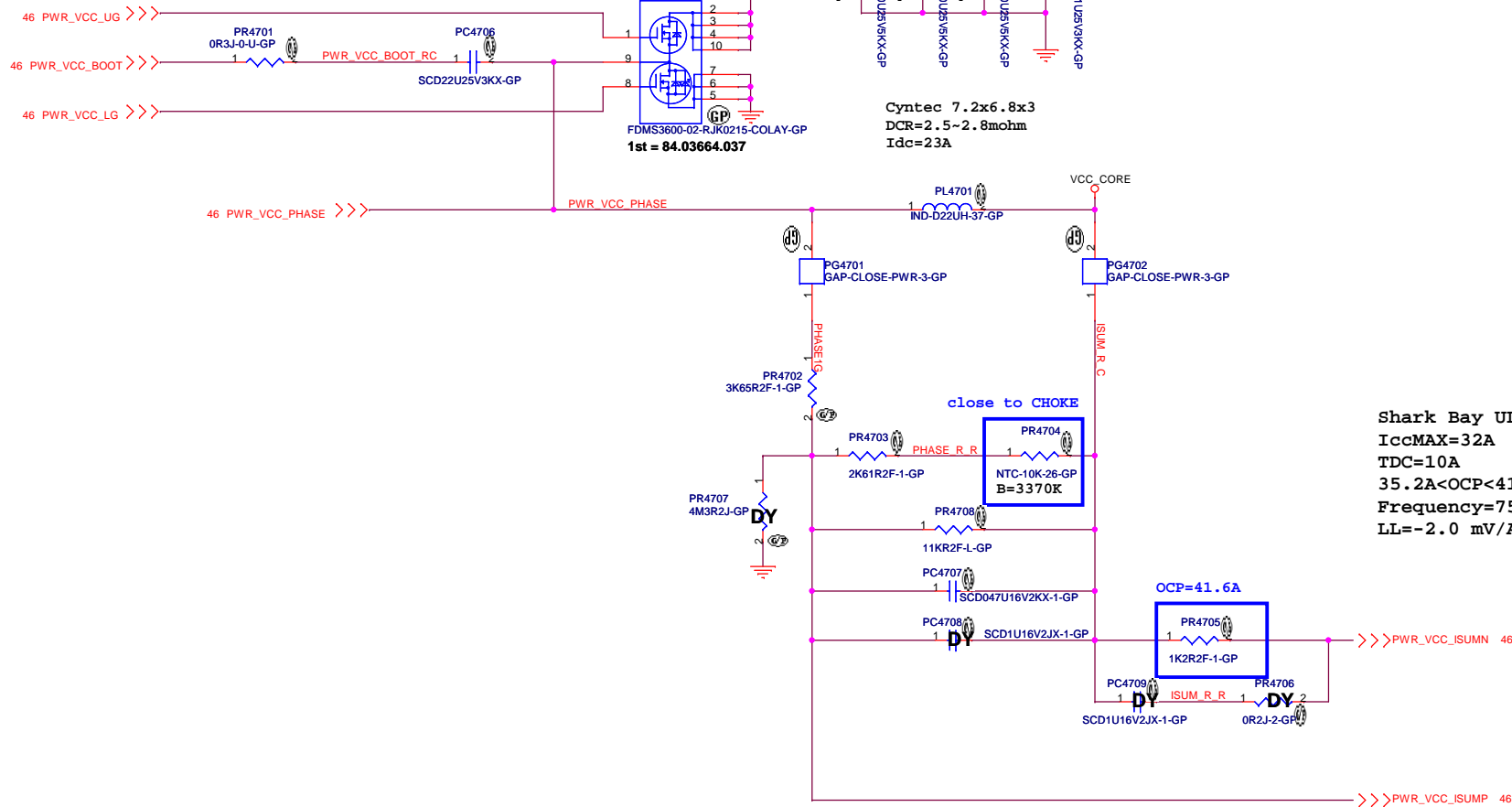
Document Number

**OAK14 Haswell**

Rev  
**X00**

Date: Wednesday, May 29, 2013

Sheet 46 of 104



Shark Bay ULT 15W CPU

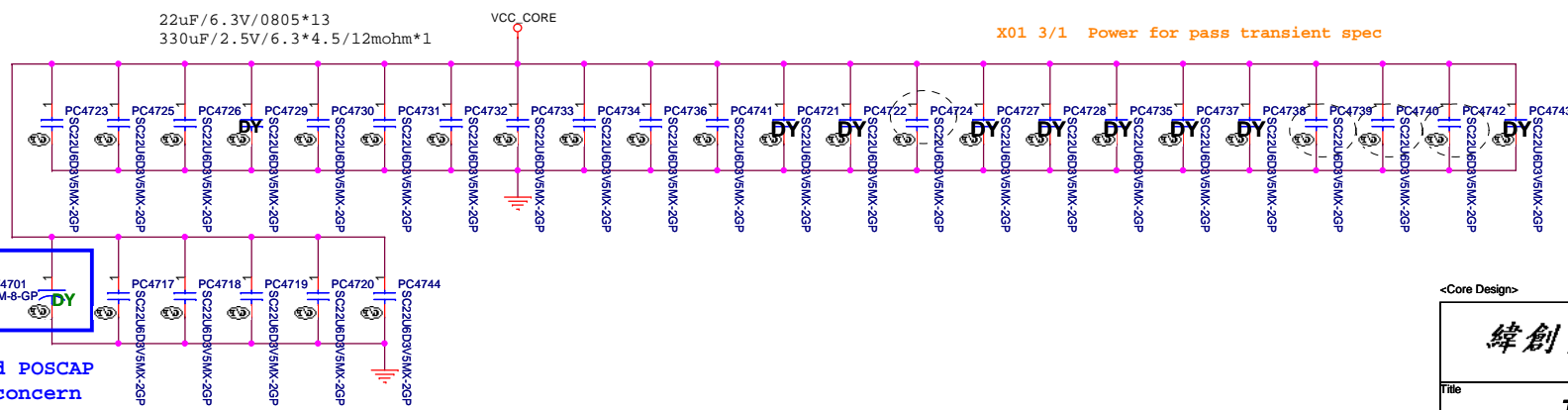
IccMAX=32A

TDC=10A

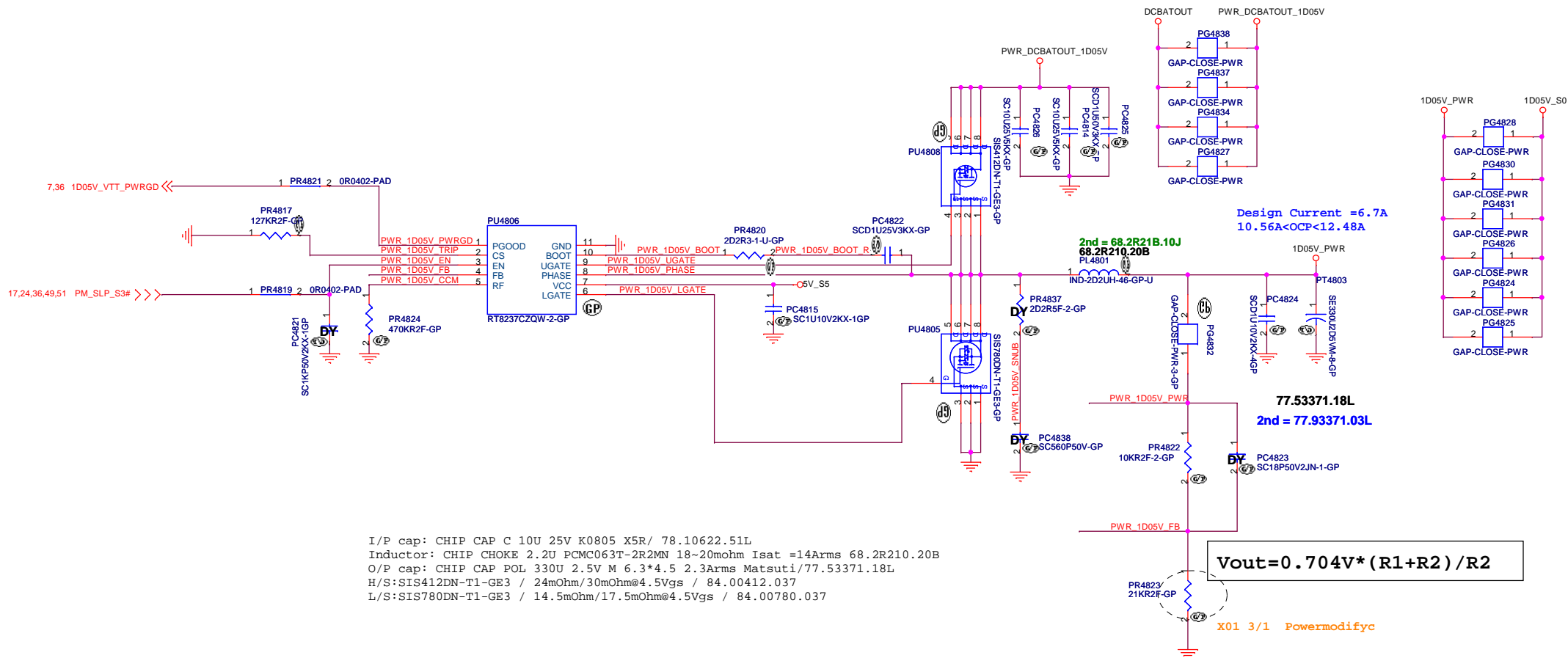
35.2A<OCP<41.6A

Frequency=750KHZ

LL=-2.0 mV/A



SSID = PWR.Plane.Regulator\_1p05v



&lt;Core Design&gt;

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Title

**TPS51367 1D05V**Size  
A

Document Number

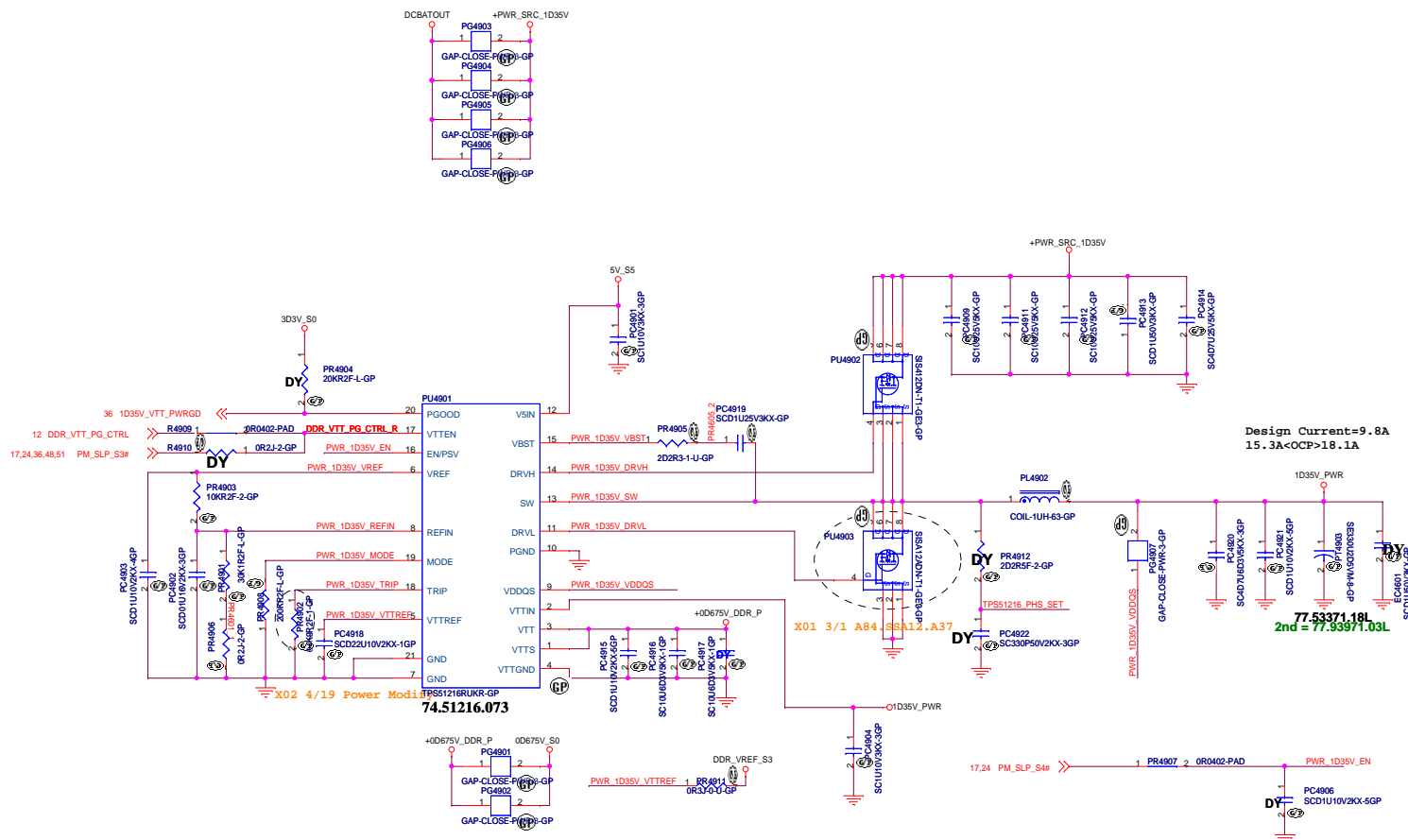
Rev	X00
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Date: Monday, April 15, 2013

Sheet 48 of 104



SSID = PWR.Plane.Regulator 1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

## MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP LND 0.1UH M PCMC063T-R10NN 1.5-1.7mohm Isat =60Arms 68.R1010.10T  
O/P cap: CHIP CAP POL 330U 2.5V M 6.3\*4.5 2.3Arms Matsuti/77.53371.18L  
H/S MOS: FET MOS ISi412DN-T1-GE3 NC BP / 84.00412.037 / Rds(on)=24-30mohm @Vgs=4.5V  
L/S MOS: FET MOS ISi780DN-T1-GE3 NC BP POWERPAK 121 / 84.00780.037 / Rds(on)=14.5-17.5mohm @Vgs=4.5V

**<Core Design>**



<Core Design>



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Title

**Reserved**

Size  
A3

Document Number  
**OAK14 Haswell**

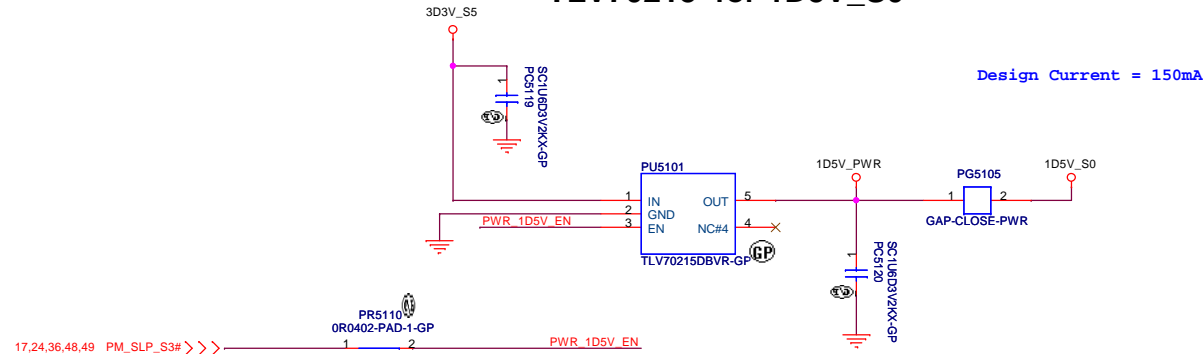
Rev  
**X00**

Date: Thursday, January 10, 2013

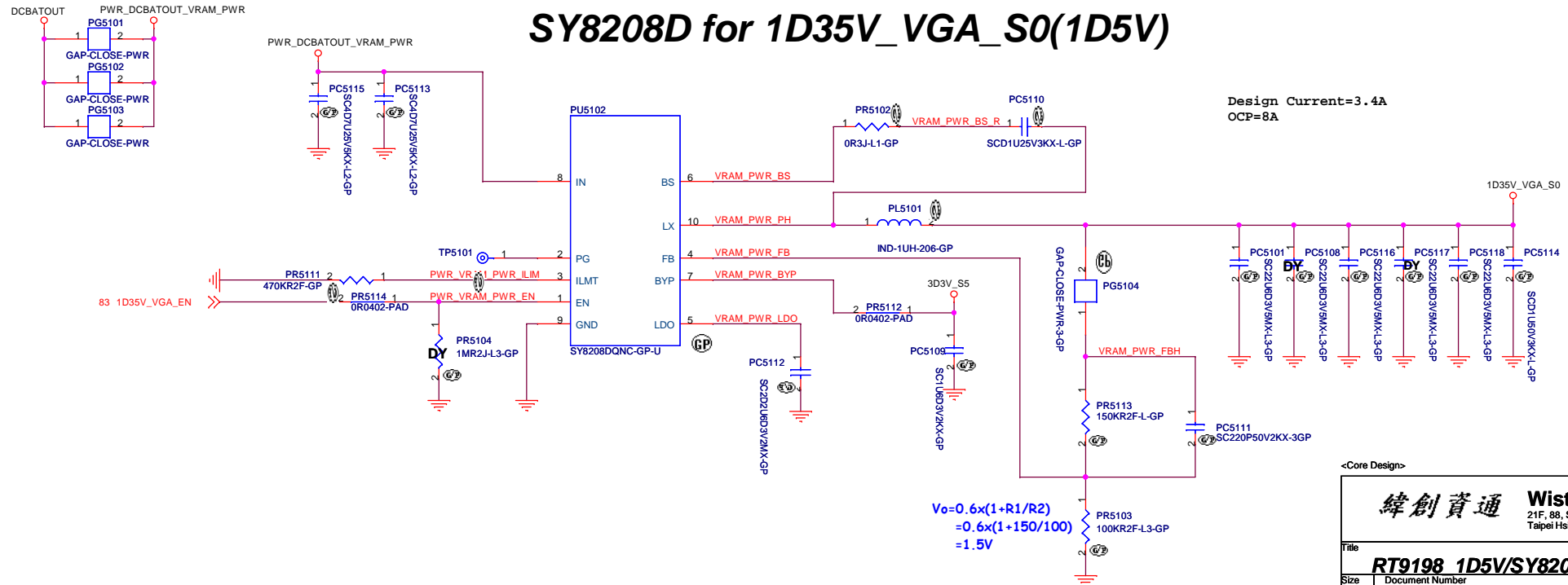
Sheet 50 of 104

SSID = PWR.Plane.Regulator\_1p5v

## TLV70215 for 1D5V\_S0



## SY8208D for 1D35V\_VGA\_S0(1D5V)



<Core Design>

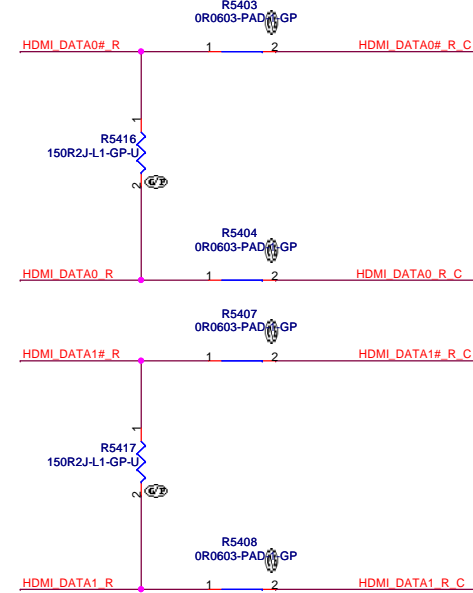
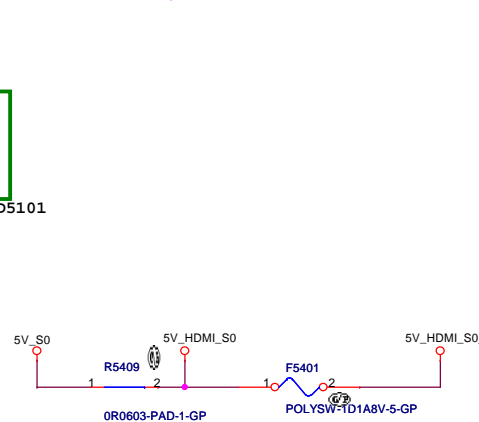
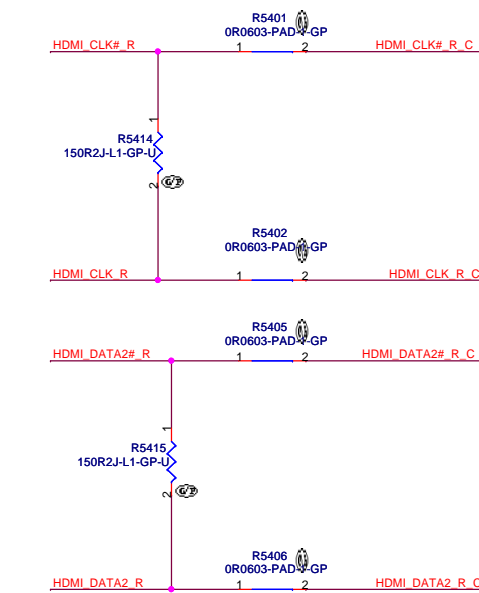
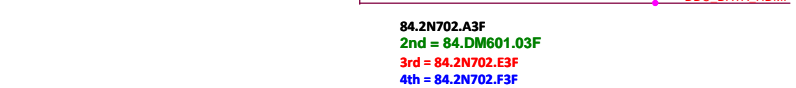
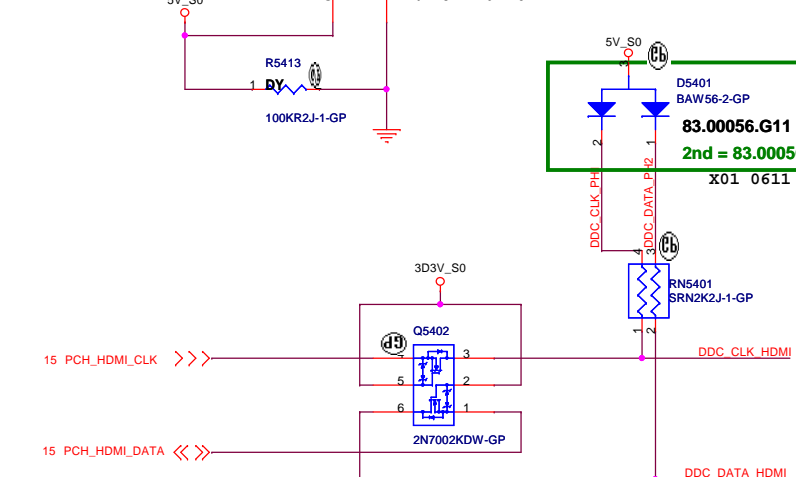
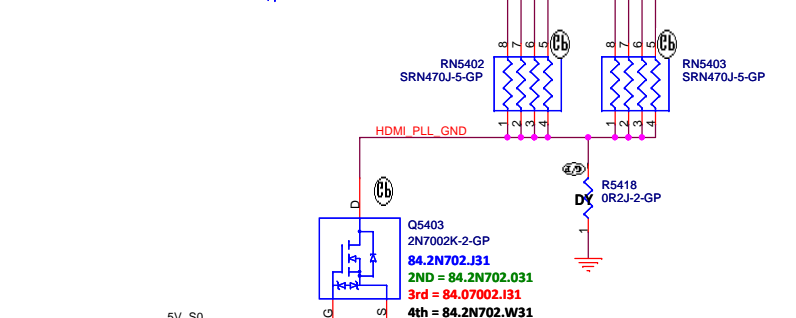
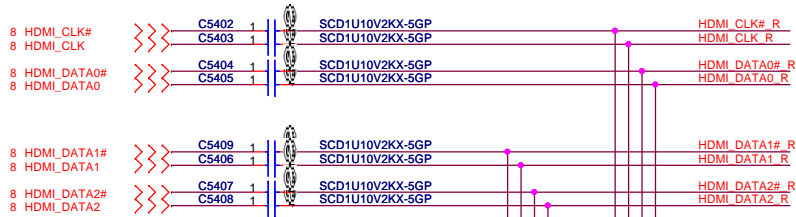
緯創資通 Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title			RT9198 1D5V/SY8208D 1D5V(VGA)
Size	Document Number	Rev	X00
A3	OAK14 Haswell		
Date:	Wednesday, May 29, 2013	Sheet	51 of 104

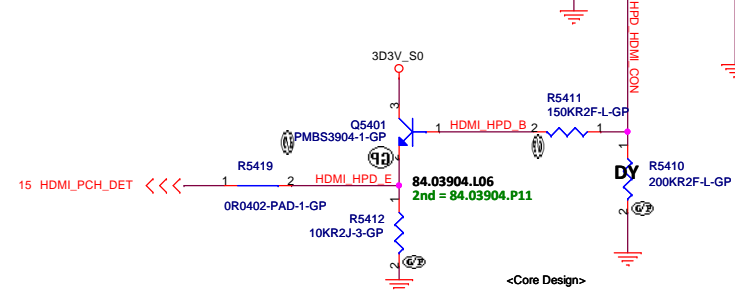
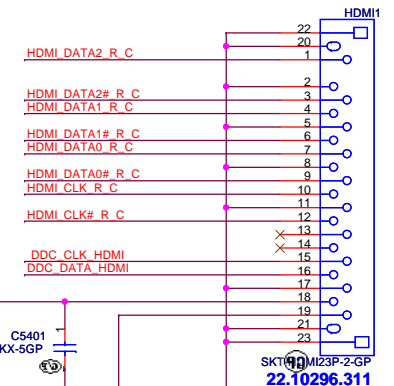




# SSID = VIDEO



HDMI CONN



<Core Design>


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Title: **HDMI Level Shifter/Connector**  
Size: A3 Document Number: **OAK14 Haswell** Rev: **X00**  
Date: Friday, April 19, 2013 Sheet 54 of 104

SSID = User.Interface

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<Core Design>



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Title

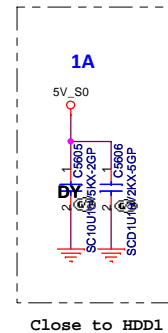
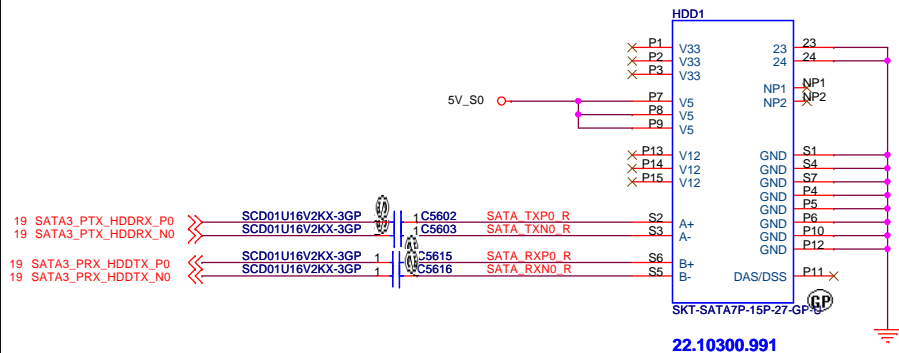
***ITP/Fan Connector***

Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 55 of 104
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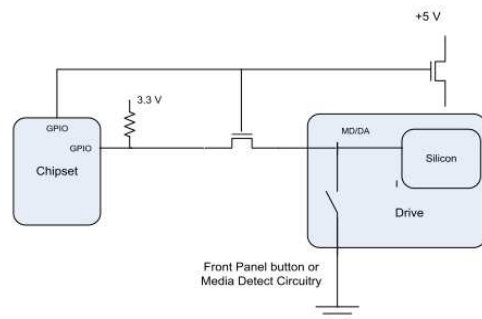
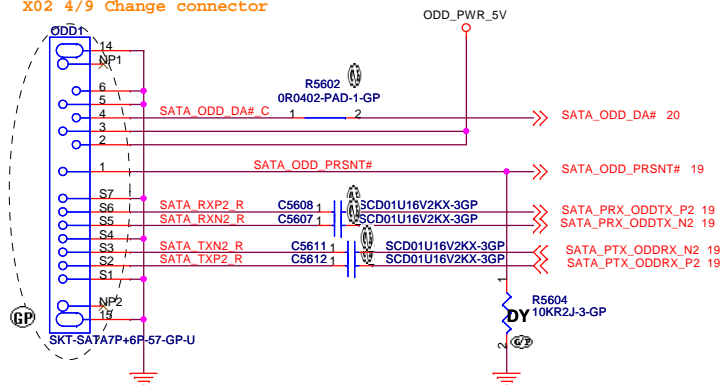
SSID = SATA

## SATA HDD Connector

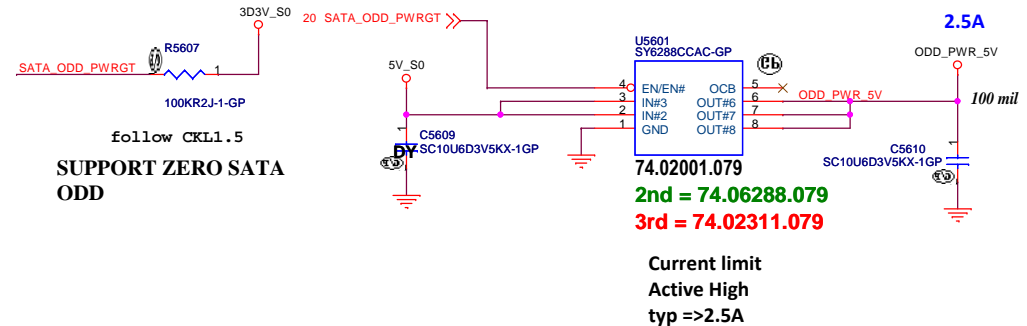


## ODD Connector

X02 4/9 Change connector



## SATA Zero Power ODD



### <Core Design>



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1	Title
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**HDD/ODD**Size  
A3

Document Number
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**OAK14 Haswell**

Rev  
X00

Date: Tuesday, May 28, 2013

Sheet 56

of


104



SSID = ESATA

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

ESATA

Size

A3

Document Number

OAK14 Haswell

Rev

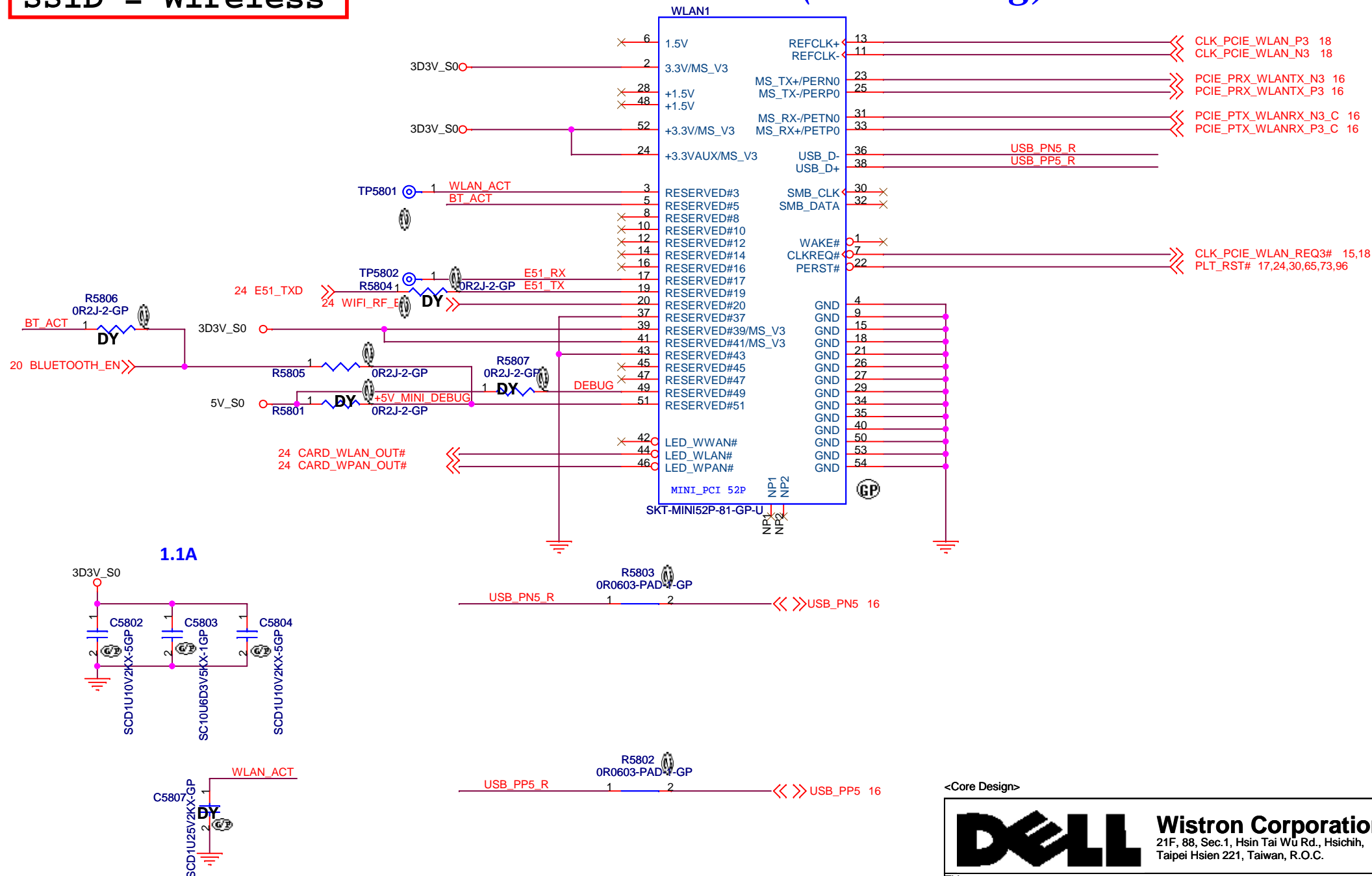
X00

Date: Thursday, January 10, 2013

Sheet 57 of 104

SSID = Wireless

# Mini Card Connector(802.11a/b/g)



<Core Design>



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Title

**MINICARD(WLAN)/ITP CONN**

Size  
A4

Document Number

**OAK14 Haswell**

Rev

**X00**

Date: Tuesday, May 28, 2013

Sheet 58 of 104

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<Core Design>



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Title

Size  
A3

Document Number  
**OAK14 Haswell**

Date: Thursday, January 10, 2013

**Reserved**


Rev  
**X00**

Sheet 59 of 104

E

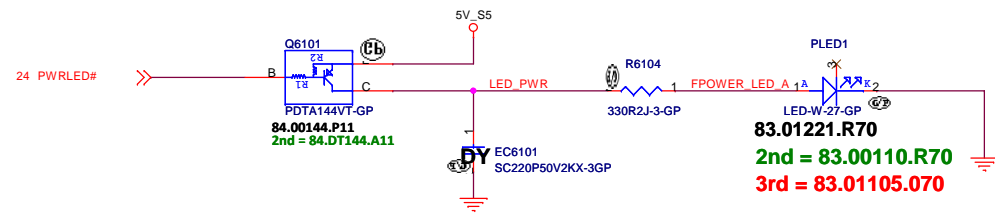
SSID = PCH

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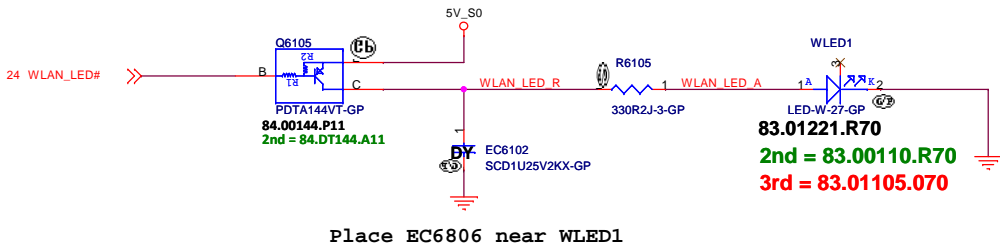
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Title (Reserved)			
Size A4	Document Number <b>OAK14 Haswell</b>		Rev <b>X00</b>
Date: Thursday, January 10, 2013		Sheet 60 of	104

SSID = User.Interface

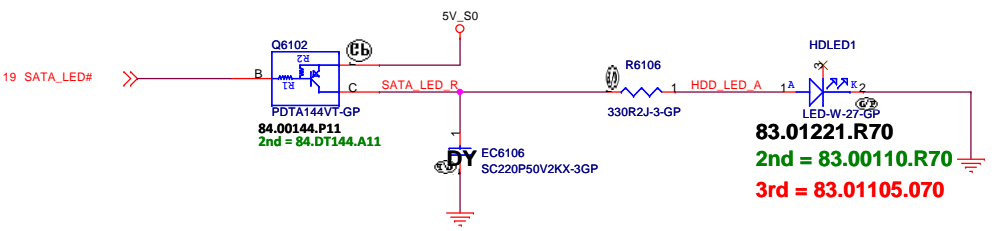
FRONT POWER LED  
Low actived from KBC GPIO



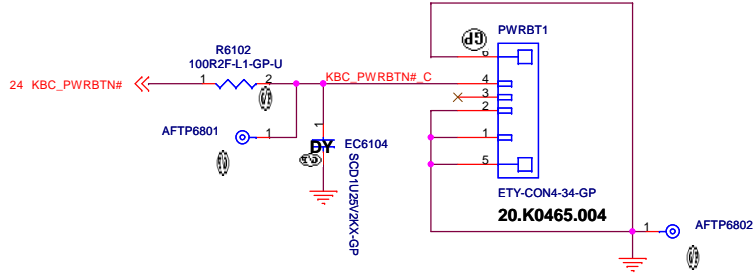
Wireless LED  
Low actived from KBC GPIO



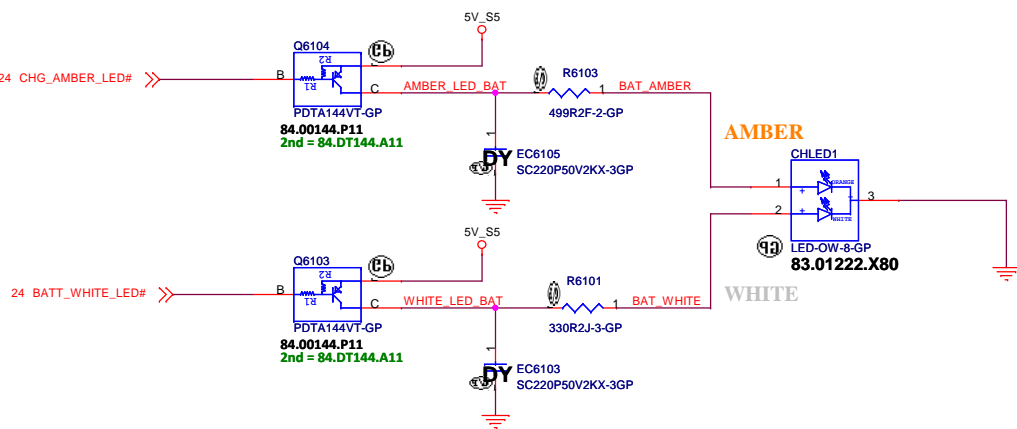
SATA HDD LED(White)  
Low actived from PCH GPIO



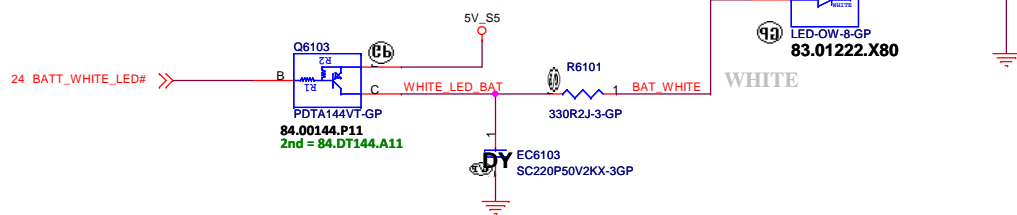
Power button



Battery LED1 (AMBER\_LED)  
Low actived from KBC GPIO

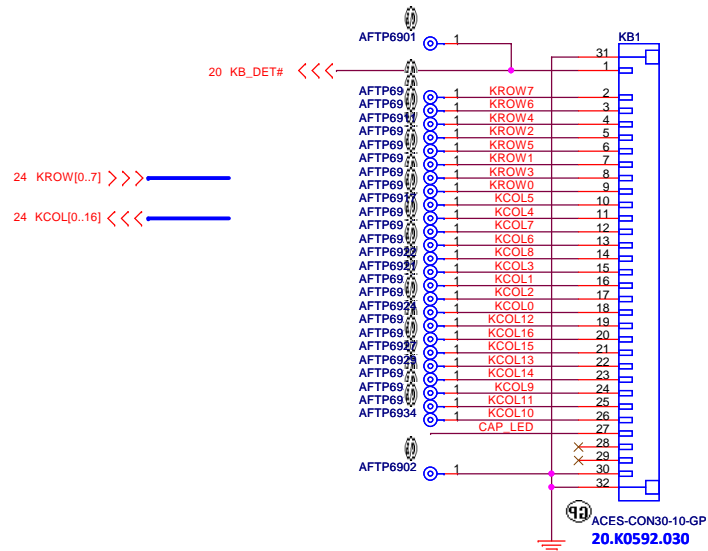


Battery LED2 (WHITE\_LED)  
Low actived from KBC GPIO

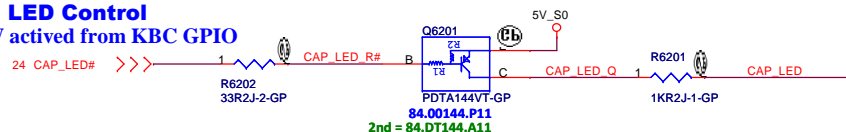


SSID = KBC

## Internal Keyboard Connector

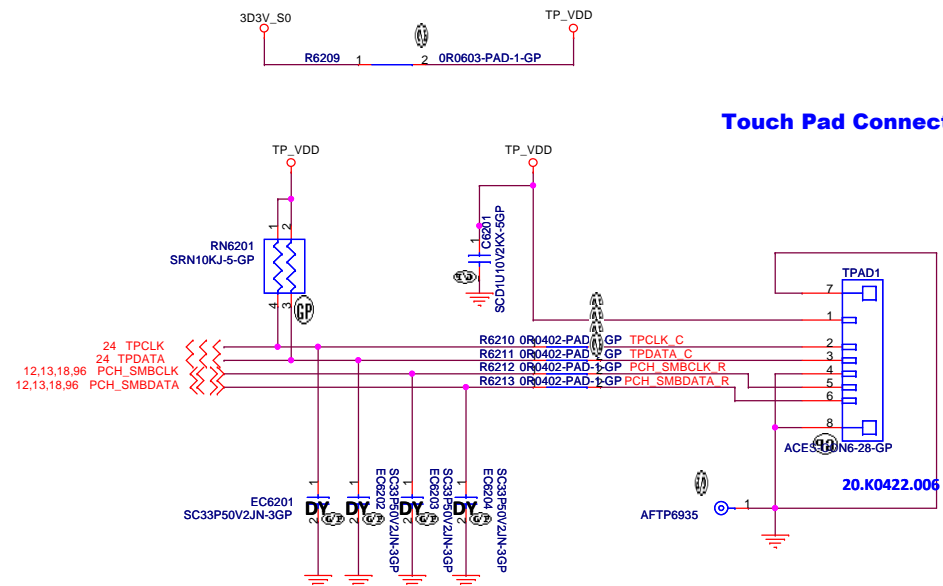


## CAP LED Control LOW acted from KBC GPIO



SSID = Touch.Pad

## Touch Pad Connector



Refer "PN 510-002792-01 Rev 2 "  
module spec

Pin number	Pin name
1	VDD
2	PS2_CLK
3	PS2_DATA
4	GND
5	SMBUS_CLK
6	SMBUS_DATA

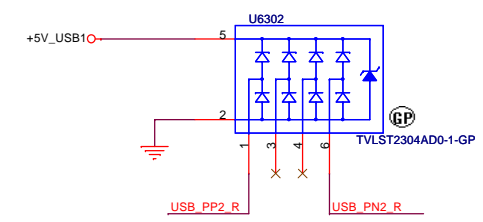
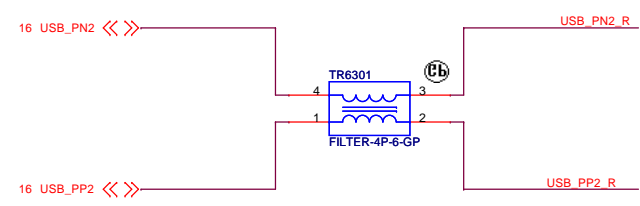
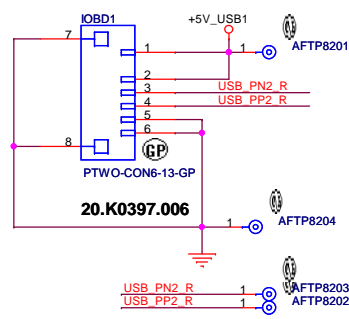
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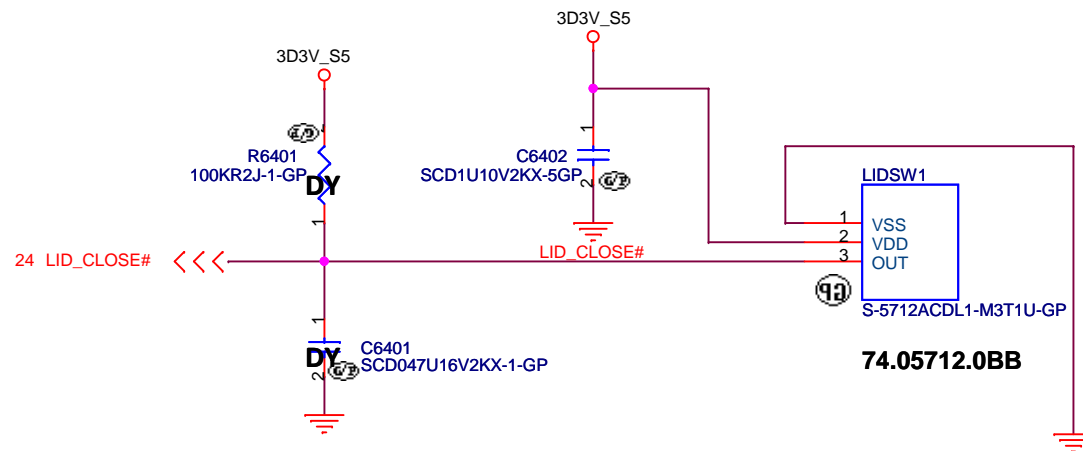
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Taipei Hsien 221, Taiwan, R.O.C.

Title <b>Key Board/Touch Pad</b>		
Size A3	Document Number <b>OAK14 Haswell</b>	Rev <b>X00</b>
Date: Wednesday, April 17, 2013	Sheet 62	of 104

SSID = User.Interface



SSID = User.Interface



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Title

**Hall Sensor**

Size  
A4

Document Number

**OAK14 Haswell**

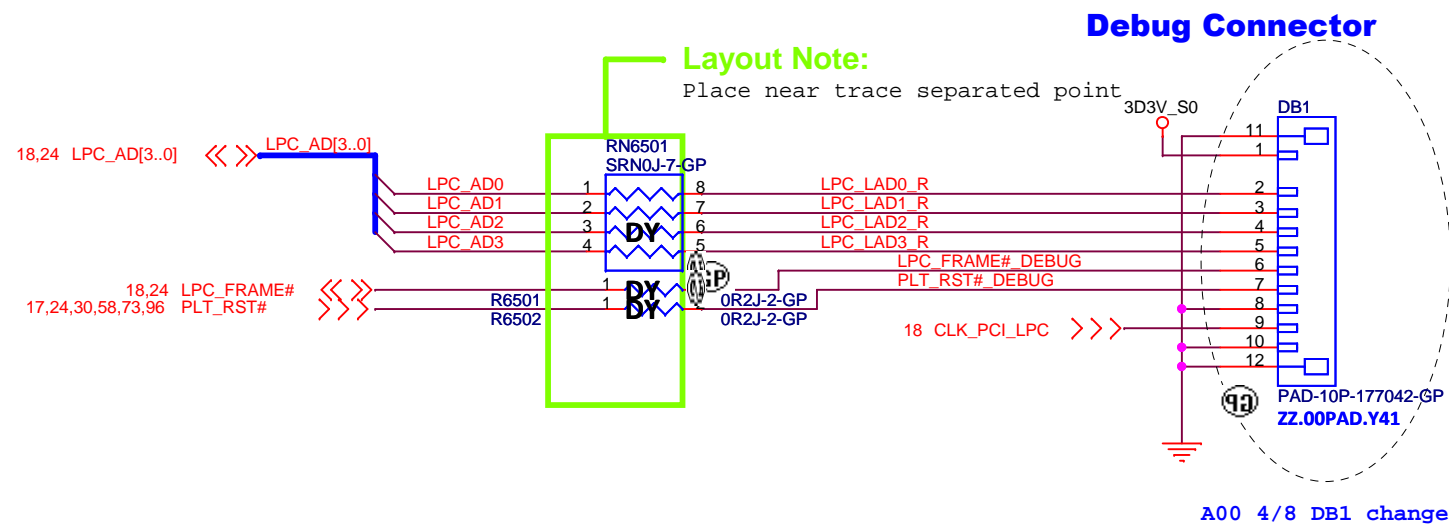
Rev  
**X00**

Date: Thursday, March 07, 2013


Sheet 64 of 104



SSID = DEBUG PORT



<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Dubug connector</b>			
Size A4	Document Number <b>OAK14 Haswell</b>		Rev <b>X00</b>
Date: Monday, April 08, 2013		Sheet 65 of	104

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<Core Design>



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Title

**Reserved**

Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 66 of 104
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<Core Design>



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Title

**Reserved**

Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 67 of 104
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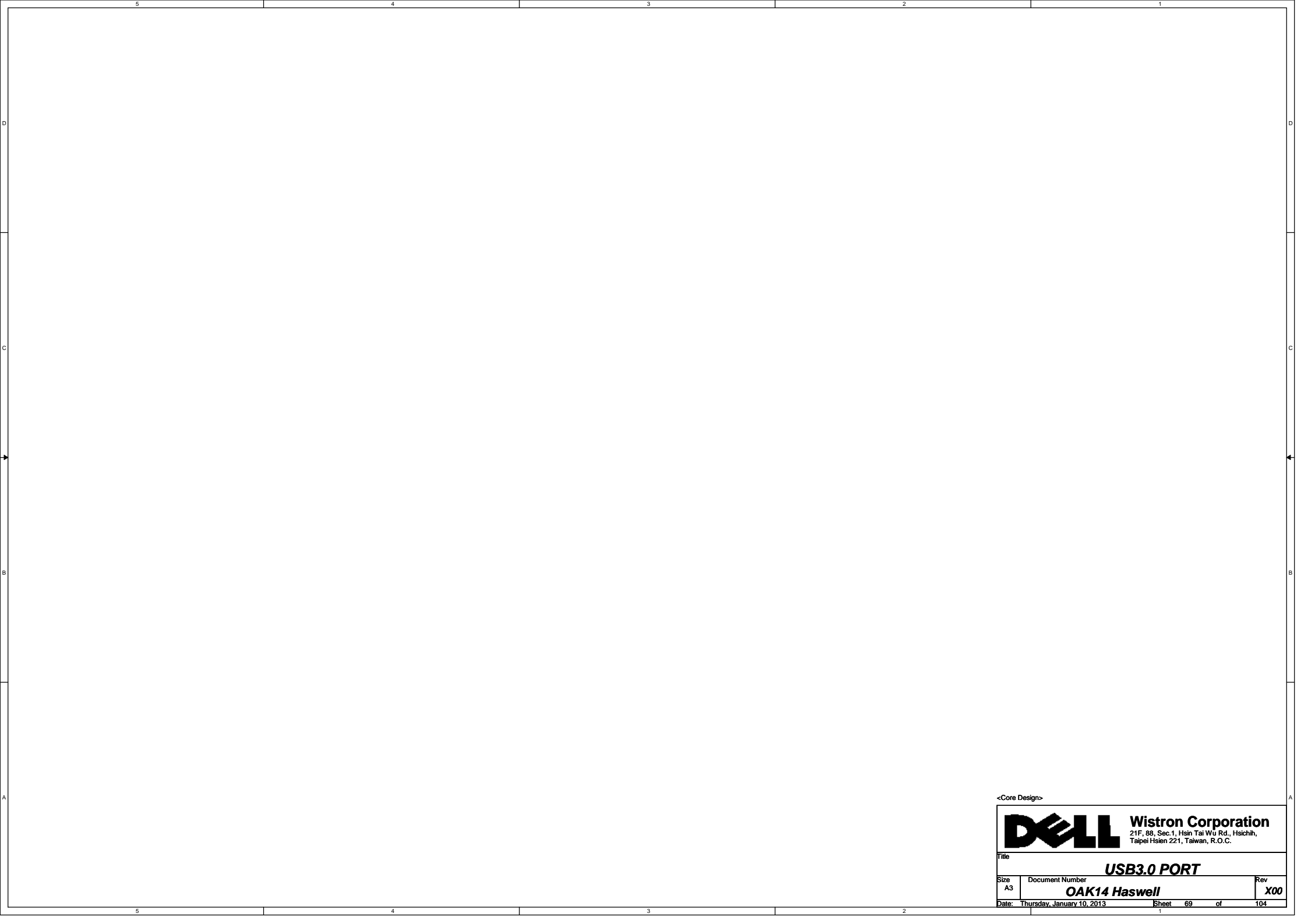
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Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>RESERVED</b>	
Size	Document Number	Rev		
A3	<b>OAK14 Haswell</b>	<b>X00</b>		
Date: Thursday, January 10, 2013		Sheet	68	of 104



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Title

**USB3.0 PORT**

Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 69 of 104
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 70 of 104
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 71 of 104
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

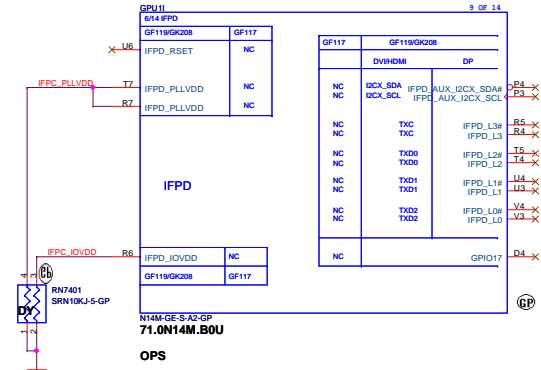
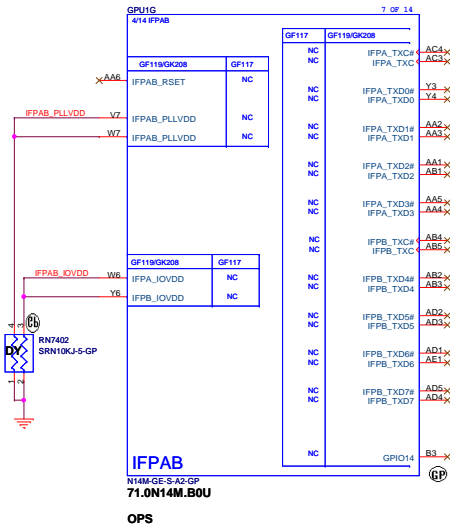
Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 72 of 104
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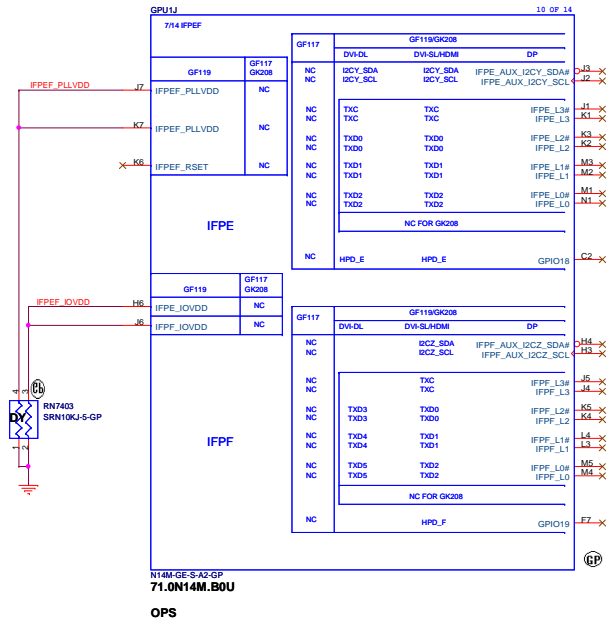
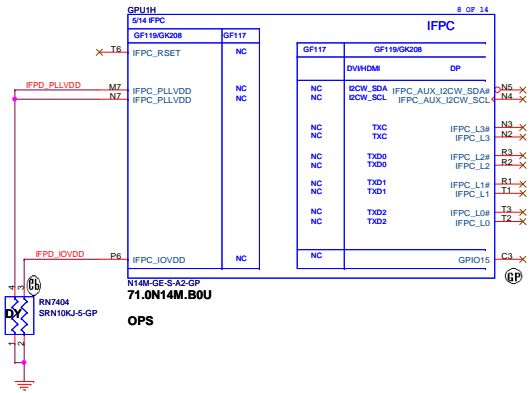




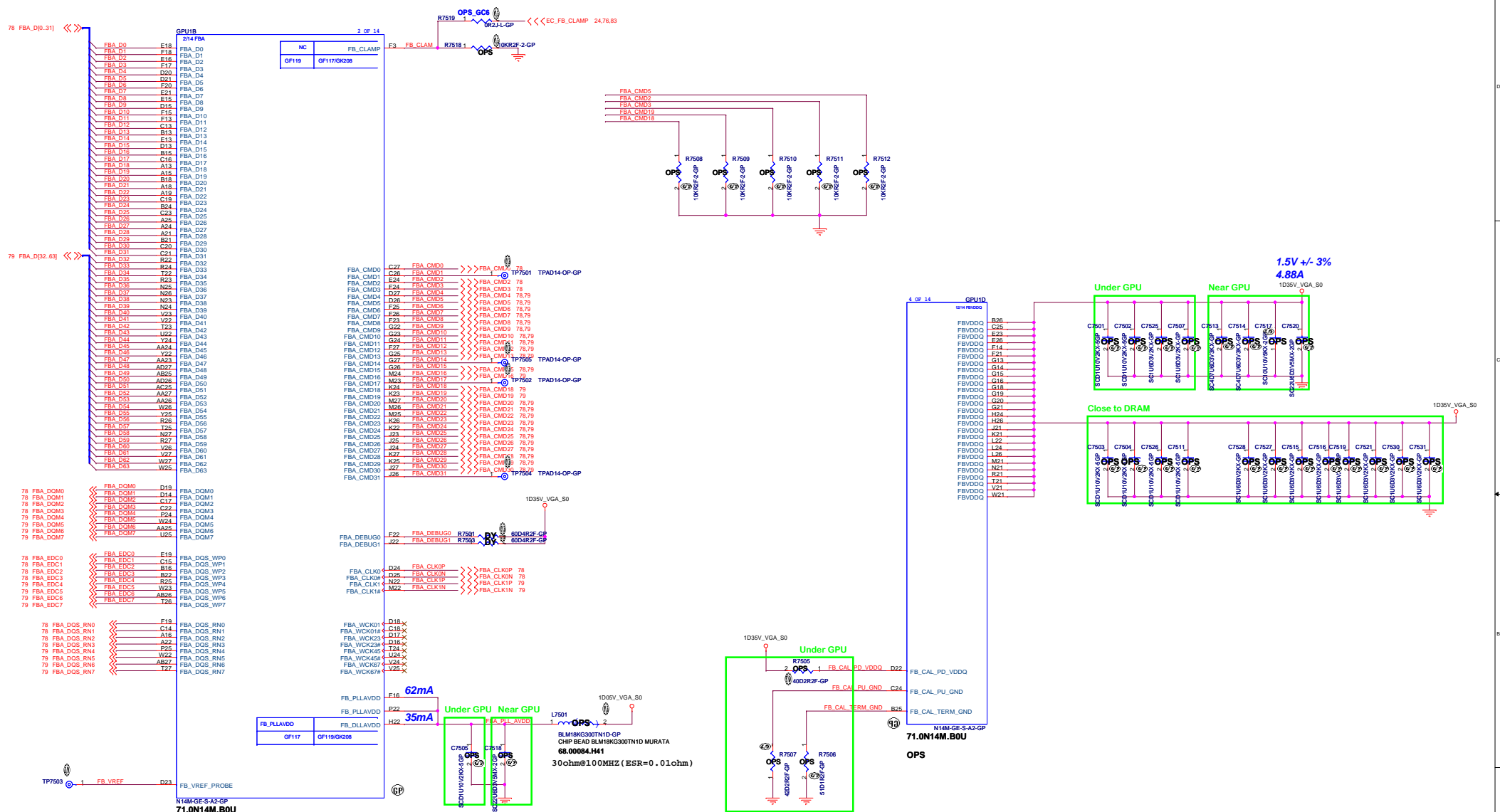
## LVDS Interface

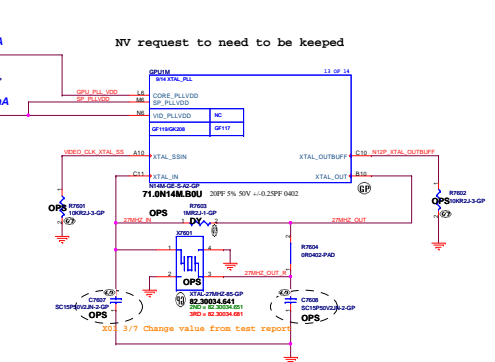


## HDMI Interface



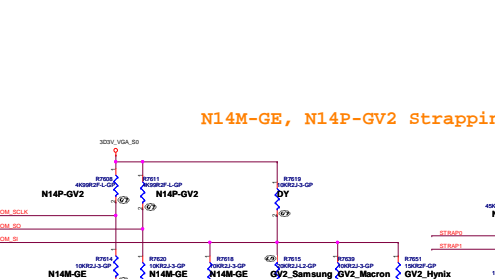
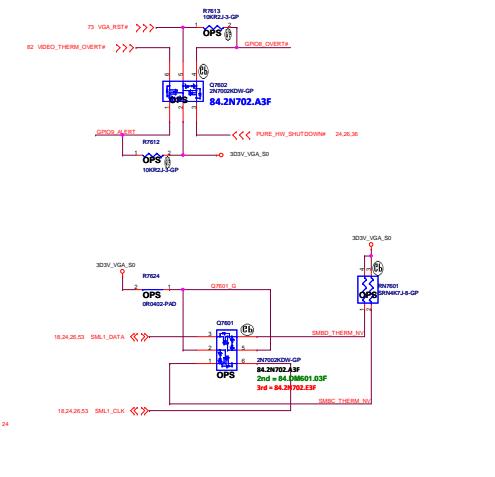
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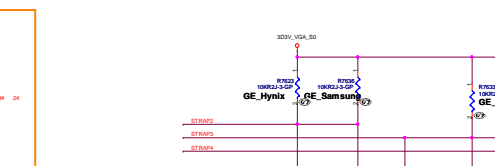
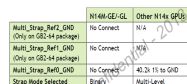


GPU Package Type	PLL Rail	Capacitor Type	Footprint	Population	Location
GB2-64 and GB4-128	PLL_VDD	100 nF	X7R	0402	1 Under GPU
		22 $\mu$ F	X7R	0805	1 Near GPU
		Bead Type			
		30 $\Omega$ [ESR=0.010 for H4E-GE; 0.05 for all others]	0402	1	Near GPU

GPU Package Type	PLL Rails	Capacitor Type	Footprint	Population	Location	
GB2-64, GB4-128 and GB3-256	SP_PLLVDD and -VDD	100 nF	0402	2	Under GPU	
	PLL_VDD combined	4.7 $\mu$ F	0402	1	Near GPU	
		22 $\mu$ F	X5R	0805	1	Near GPU
<b>Board Type</b>						
	180 $\Omega$ (ESR=0.2)		0603	1	Near GPU	



ing



Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Data Code Minimum	Status
128Mx16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093C-K	1000	1234	Production ready
				MT41J128M16JT-107C-K	900	1150	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G164AE-BC1A	1000	1204	Production ready
				K4W2G164AE-BC11	900	1204	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DR-10C	1000	II/A	Production ready
				H5TQ2G63DR-11C	900	II/A	Production ready
		0xC	1.5V/ 1.5V	H5T2G63FFR-11C	1000	II/A	Post-production candidate

Configuration	Vendor	Strap	FBVDD/ FBVDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Data Code Altimode	Status
256Mx16 DDR3	Samsung	0x3	1.5 V / 1.5 V	K4W4G1648-HC11	900	H/A	Production ready
	Micron	0x1	1.5 V / 1.5 V	MT41R256M16HA- 1070C-E	900	H/A	Production ready
	Hynix	0x2	1.5V / 1.5V	H5TC4G63AFR-11C	900	H/A	Production ready

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_S0	SWB_ALT_A0ER	10k $\Omega$	Pull-down to GND
ROM_SI	SWB_VEH0DR	10k $\Omega$	Pull-up to 3V3 if VBIOS ROM exists, Pull-down to GND if no VBIOS ROM
ROM_S0	VGA_VEH0E	10k $\Omega$	Pull-down to GND (no display)
STRAP0	RAIL_CFG[0]	10k $\Omega$	See HwInfo below
STRAP1	RAIL_CFG[1]	10k $\Omega$	See HwInfo below
STRAP2	RAIL_CFG[2]	10k $\Omega$	See HwInfo below
STRAP3	RAIL_CFG[3]	10k $\Omega$	See HwInfo below
STRAP4	PCIEX_MAX_SPEED	10k $\Omega$	Pull-down to GND

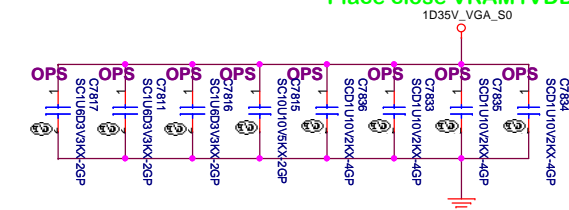
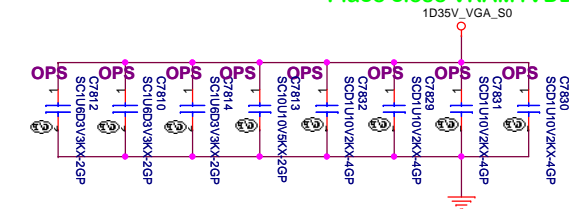
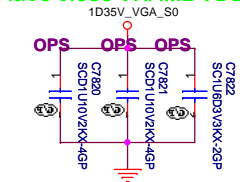
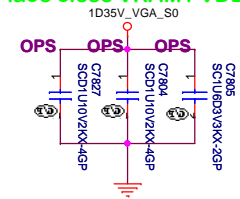
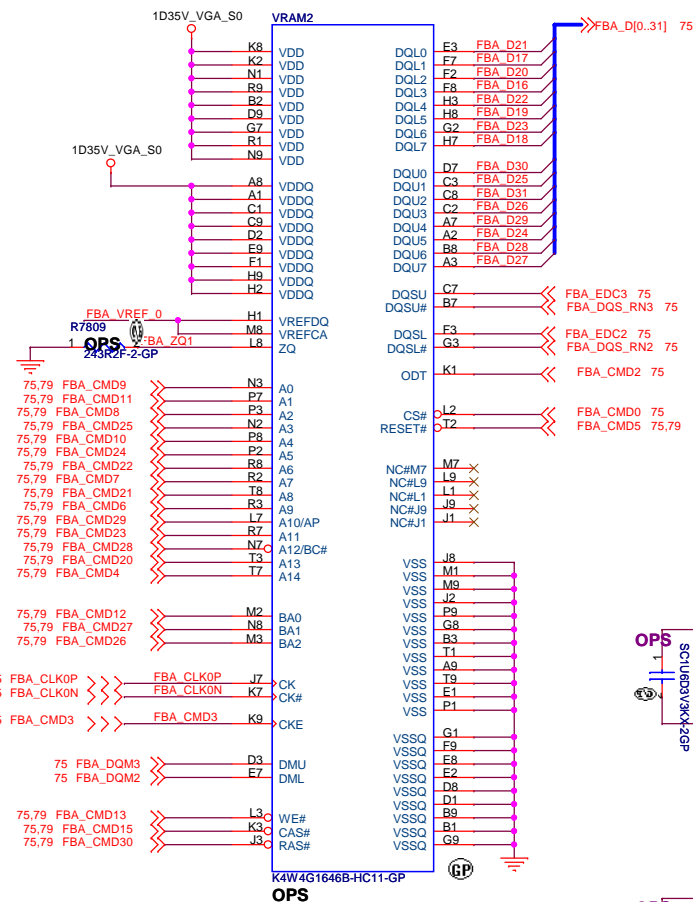
Chip Part #	GK208-640 (Small package)	GK208-630 (Small package)	GK208-650 (Small package)	GK208-632 (Small package)
	GK208-740 (Big package)	GK208-730 (Big package)	GK208-750 (Big package)	GK208-732 (Big package)
Device ID	0x1291	0x1290	0x1294	0x1292

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Taippei Hsien 321, Taiwan, R.O.C.

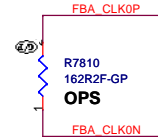
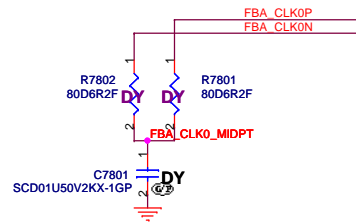
File: **GPU POWER(4/5)**

Doc: **OAK14 Haswell**




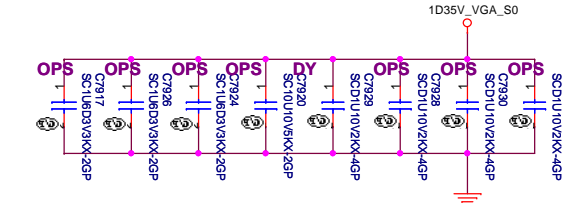
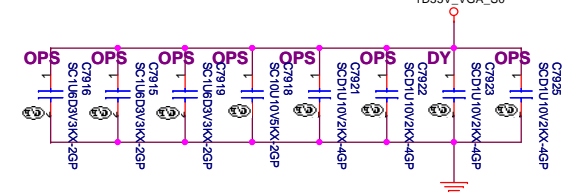
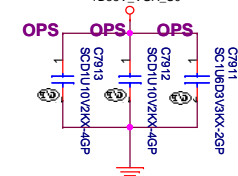
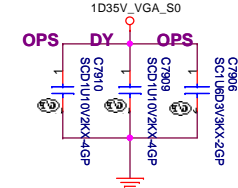
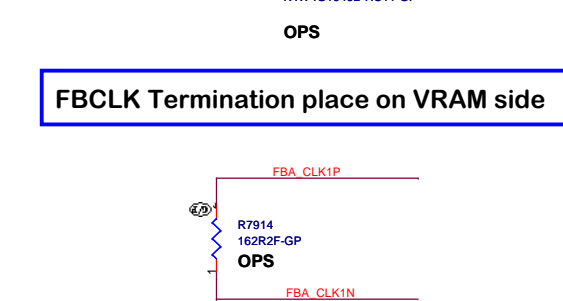
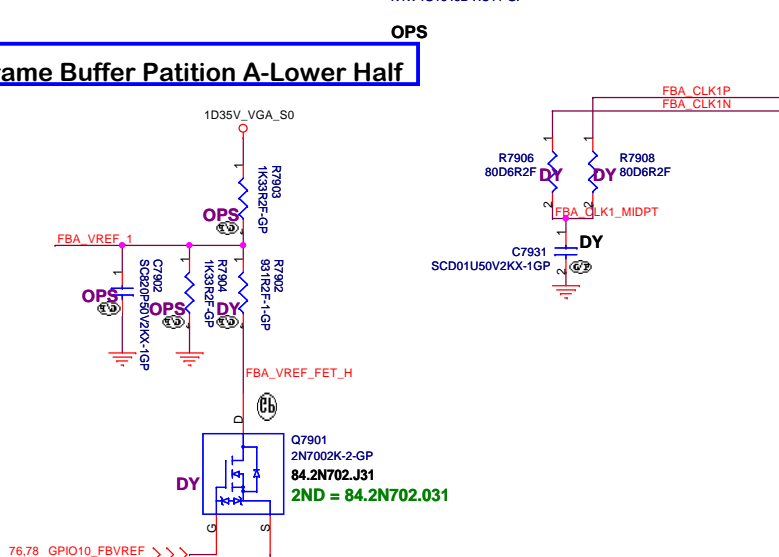


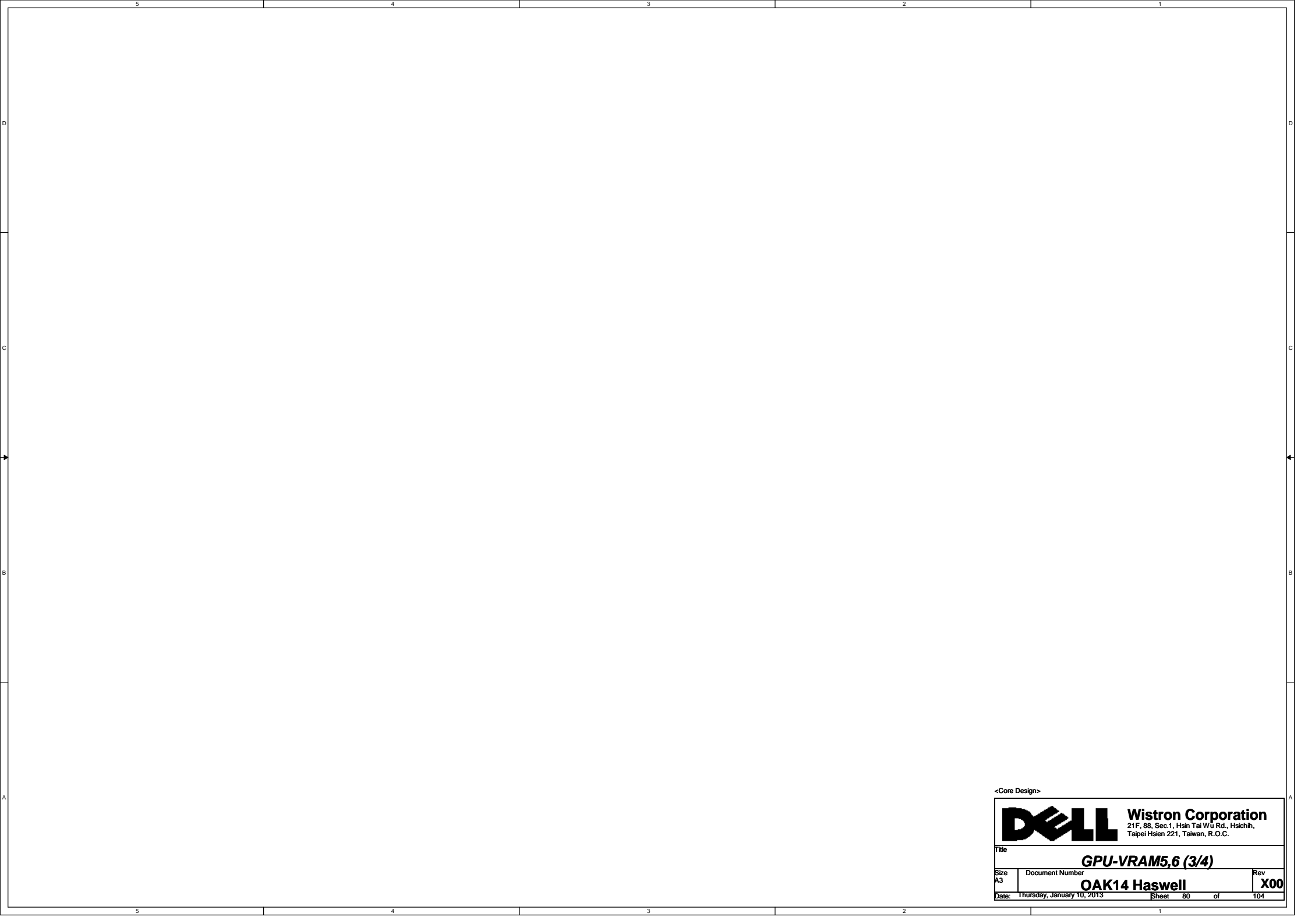
### FBCLK Termination place on VRAM side




Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

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		Title _____	
Size A3		Document Number <b>GPU-VRAM1,2 (1/4)</b> <b>OAK14 Haswell</b>	
Date: Wednesday, Apr 17, 2013		Sheet 78 of 104	
		<b>X000</b>	

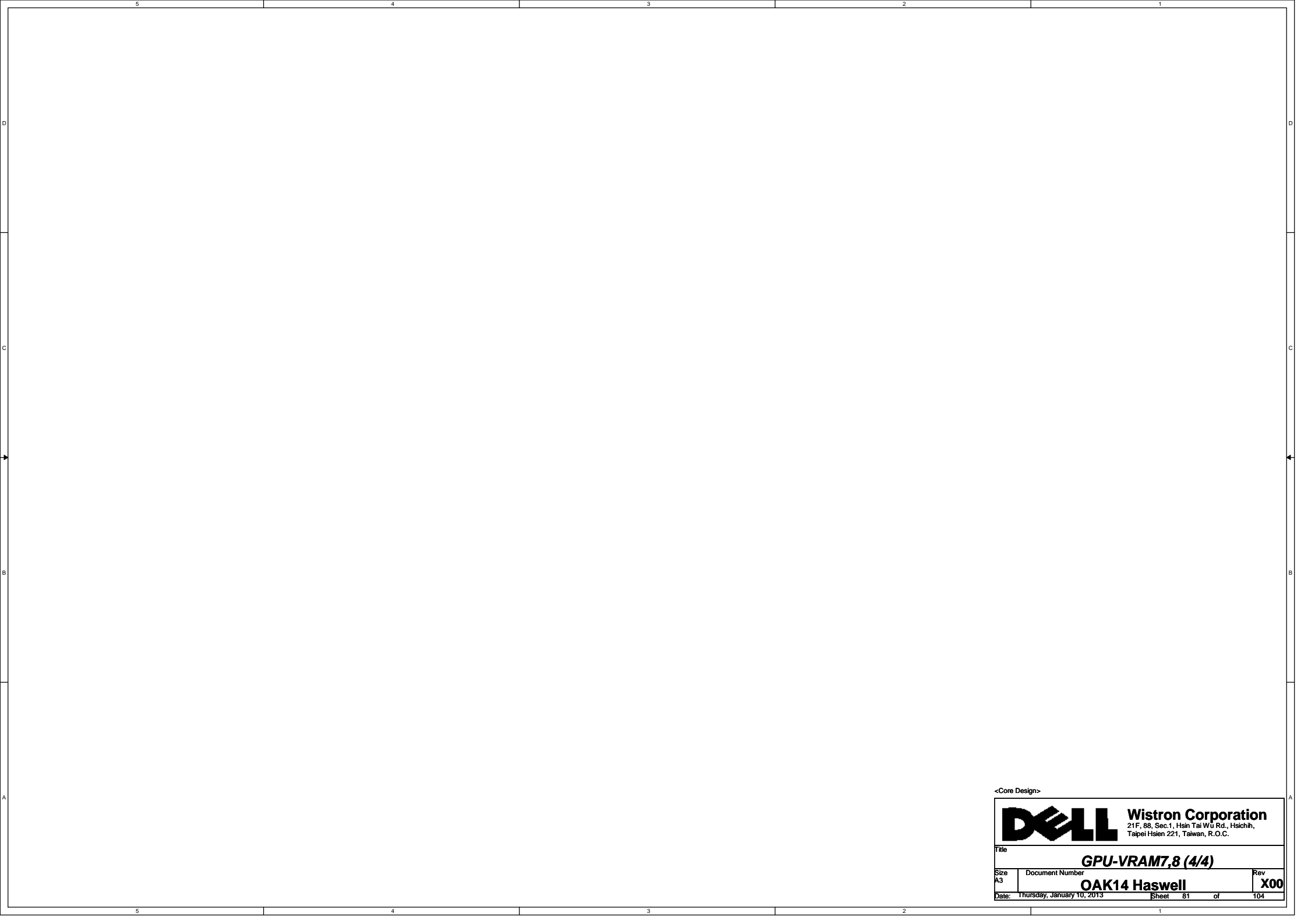





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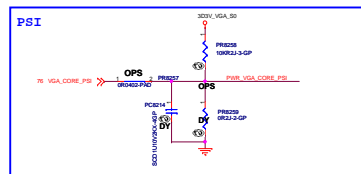
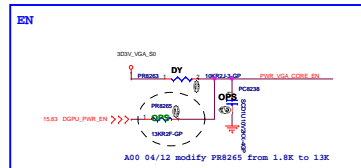
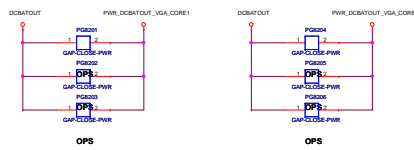
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Title					
GPU-VRAM5,6 (3/4)					
Size	Document Number				Rev
A3	OAK14 Haswell				X00
Date:	Thursday, January 10, 2013		Sheet	80	of 104



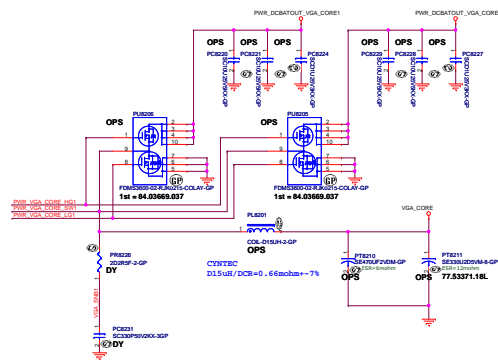


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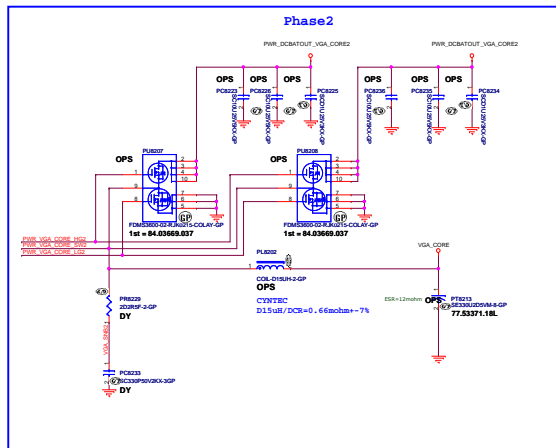
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Title					
GPU-VRAM7,8 (4/4)					
Size	Document Number				Rev
A3	OAK14 Haswell				X00
Date:	Thursday, January 10, 2013		Sheet	81	of 104



#### Phase1



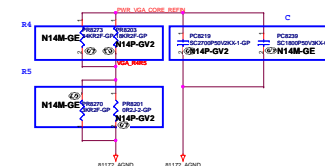
I/P cap: 100 25V K8005 XSR/ 78.10622.51L  
 MOS: Q1: Id=10A, Rds(on)=9.8-13.2 mOhm / Q2: Id=17A, Rds(on)=3.6-5.2mOhm 84.03669.037  
 Inductor: CHIP CHOKER 0.22mH PCB0693T-R22M0 2.5-3mOhm Isat =34Arms 68.R2210.20C  
 O/P cap: CHIP CAP POL 3300 2.5V M 6.3\*4.5 2.3Arms Matsuti/77.53371.18L



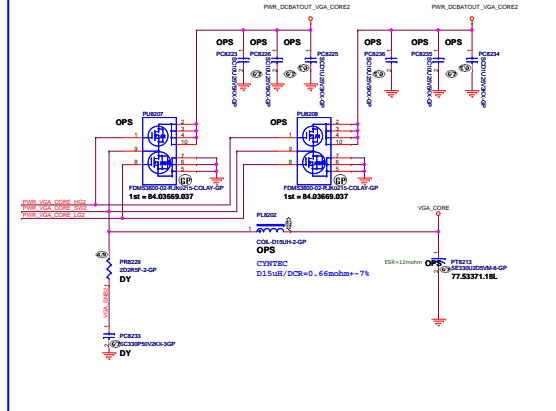
I/P cap: 100 25V K8005 XSR/ 78.10622.51L  
 MOS: Q1: Id=10A, Rds(on)=9.8-13.2 mOhm / Q2: Id=17A, Rds(on)=3.6-5.2mOhm 84.03669.037  
 Inductor: CHIP CHOKER 0.22mH PCB0693T-R22M0 2.5-3mOhm Isat =34Arms 68.R2210.20C  
 O/P cap: CHIP CAP POL 3300 2.5V M 6.3\*4.5 2.3Arms Matsuti/77.53371.18L

#### NTC close Phasel MOSFET

NTC close Phasel MOSFET

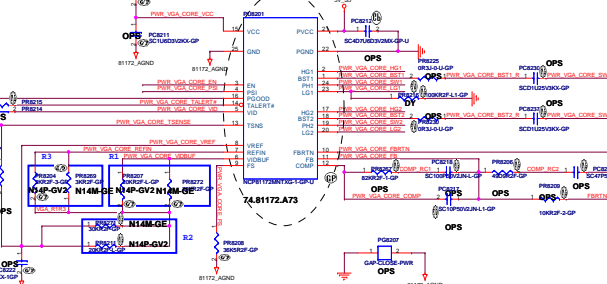


#### Phase2



I/P cap: 100 25V K8005 XSR/ 78.10622.51L  
 MOS: Q1: Id=10A, Rds(on)=9.8-13.2 mOhm / Q2: Id=17A, Rds(on)=3.6-5.2mOhm 84.03669.037  
 Inductor: CHIP CHOKER 0.22mH PCB0693T-R22M0 2.5-3mOhm Isat =34Arms 68.R2210.20C  
 O/P cap: CHIP CAP POL 3300 2.5V M 6.3\*4.5 2.3Arms Matsuti/77.53371.18L

#### X01 3/1 Change to MP version



EDC=45A  
 EDP=72A

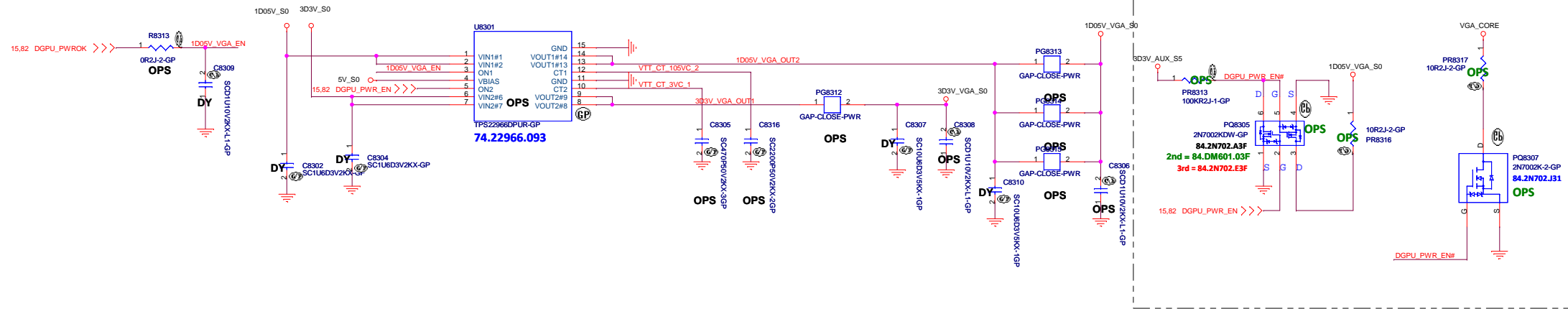
TYPE	config	TDC	SDP	OCF	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14M-GE	C	35A	41A		39kohm	30kohm	3kohm	24kohm	3kohm	1.8nF
N14P-GV2	B	32A	55A		20kohm	20kohm	2kohm	18kohm	0ohm	2.7nF
N14P-GT	B	45A	75A		20kohm	20kohm	2kohm	18kohm	0ohm	2.7nF

Table 1. PWM-VID Spec and Component Values

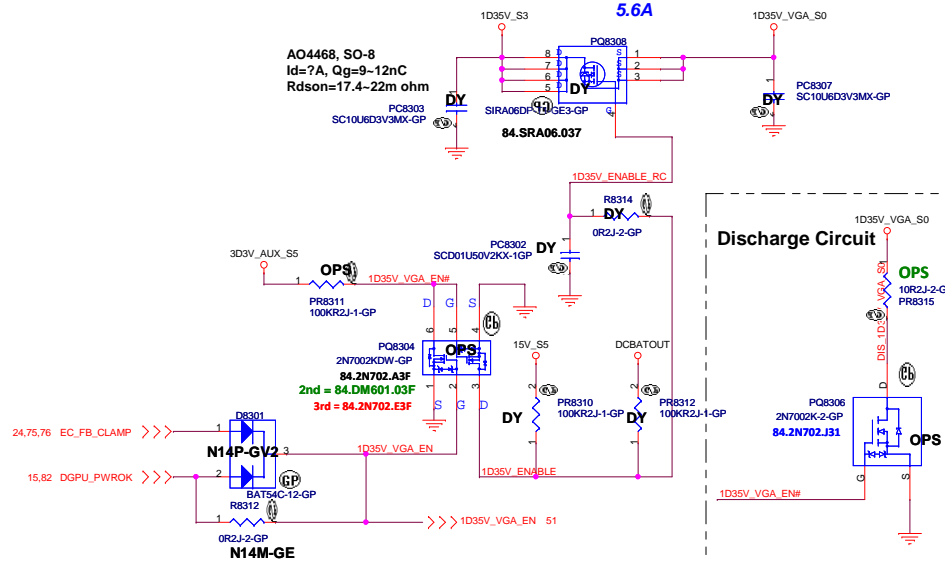
PWM-VID Spec	Config A	Config B	Config C
Vmin	0.6	0.6	0.65
Vmax	1.2	1.2	1.15
Vboot	0.875	0.9	0.9
Voltage Step Vstep	6.25	6.25	3.5
Number of Voltage Levels N	level	96	20
PWM Frequency F <sub>SW</sub>	1.125	1.125	0.676
PWM Minimum Pulse Width T <sub>ON</sub>	ns	9.26	0.26
VID Transient Time T	us	<100	<100
Component Value			
R1 (1%)	KQ	20	39
R2 (1%)	KQ	20	30
R3 (1%)	KQ	1.5	2
R4 (1%)	KQ	30	18
R5 (1%)	KQ	1.5	0
C	nF	1.5	2.7

```
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0
```

### 0307 Add Discharge Circuit

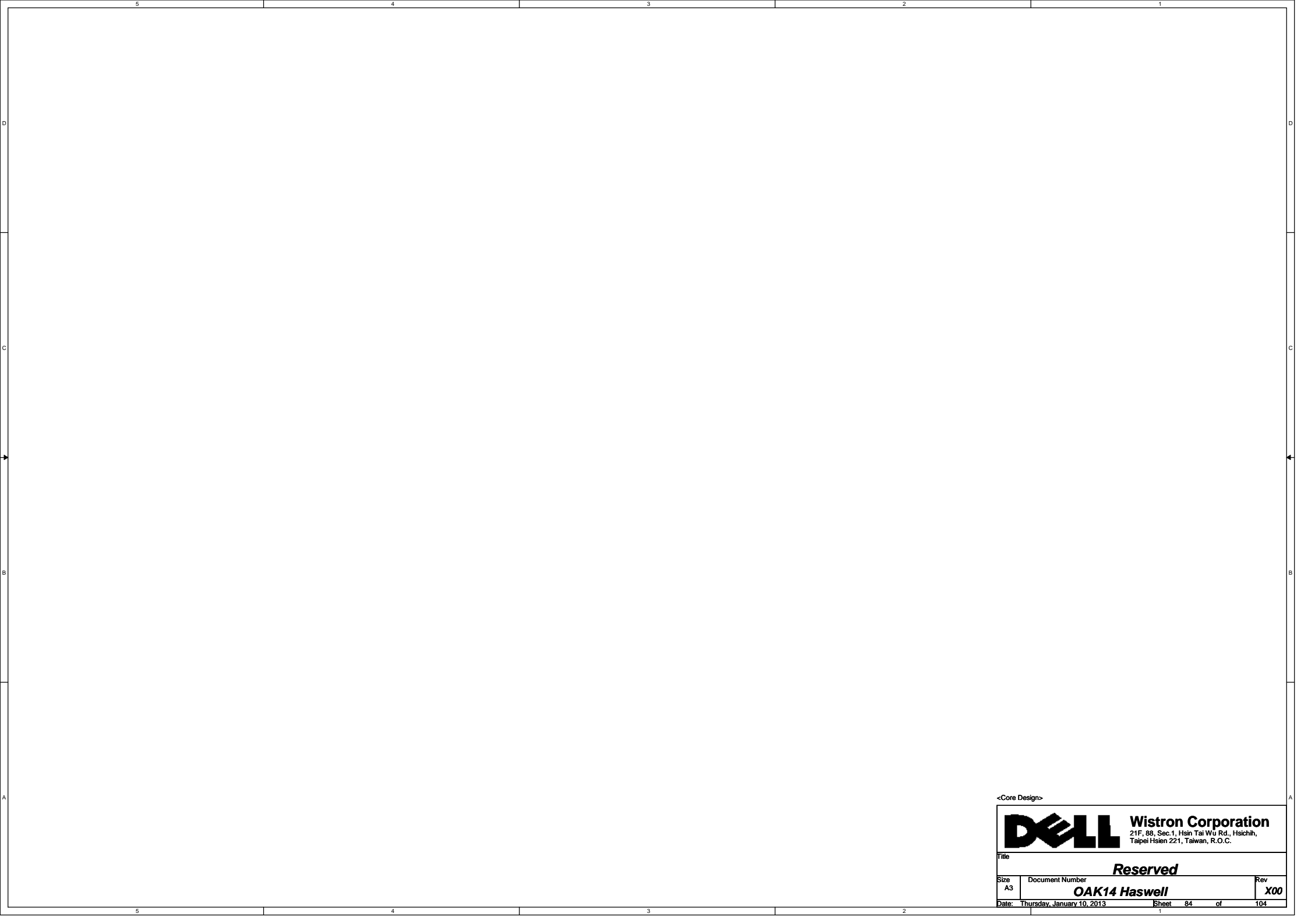


1.35V +/- 3%.  
5.6A




	Rise Time (μs) 10% - 90%, COUT = 0.1μF @ VIN; VOUT=0 ohm load							
	Typical values @ 25°C, 25V X7R 10% ceramic cap							
CTx (pF)	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. CTx value



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Size	Document Number		Rev
A3	<b><i>OAK14 Haswell</i></b>		<b><i>X00</i></b>
Date:	Thursday, January 10, 2013		Sheet 84 of 104

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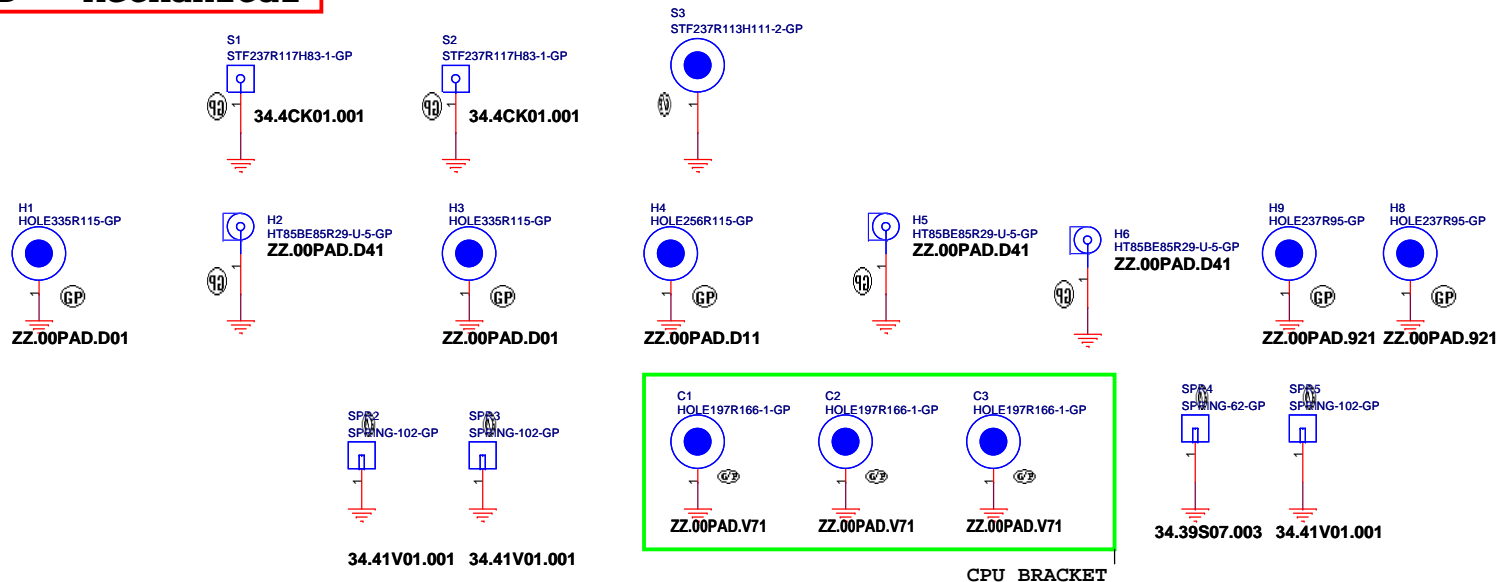
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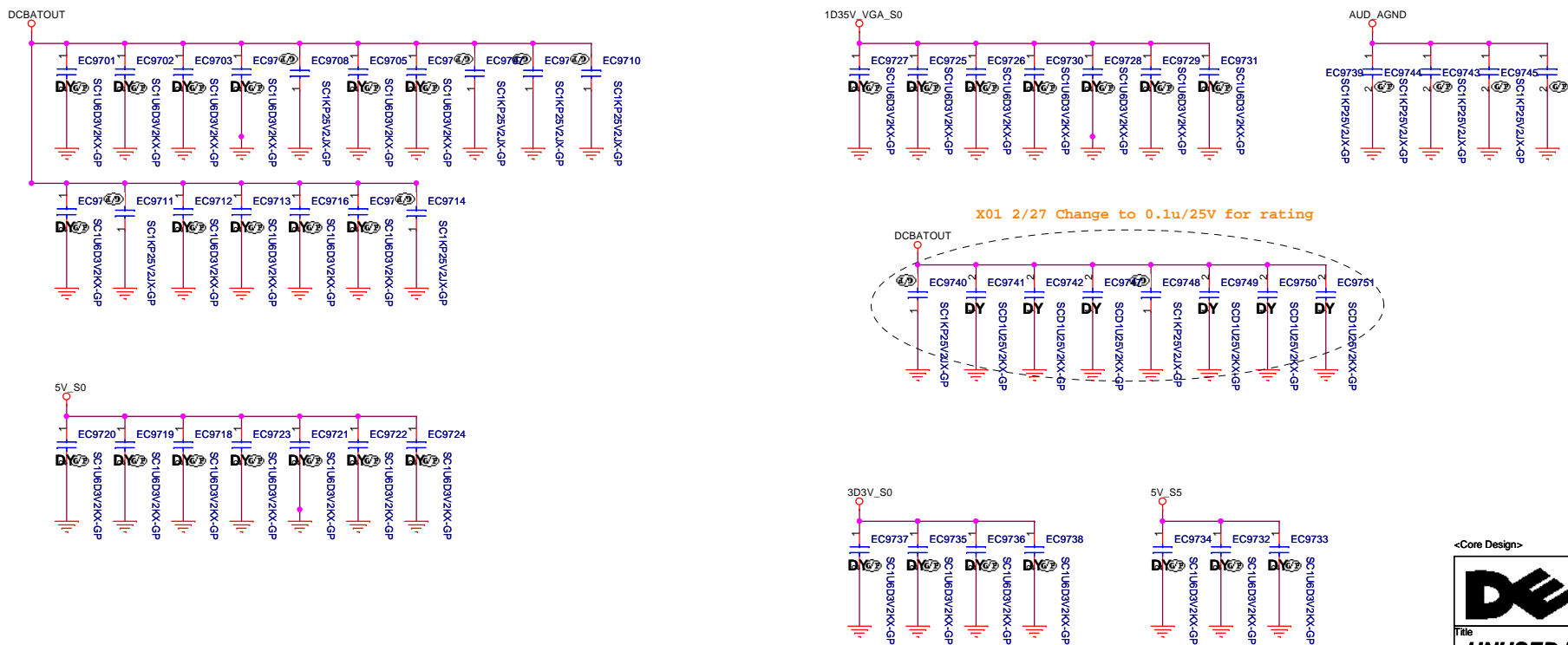
Sheet 85 of 104

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## SSID = Mechanical



## SSID = EMI



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Size

A3

Document Number

OAK14 Haswell

Date: Thursday, January 10, 2013

Sheet 87 of 104

Rev

X00

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Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 88 of 104
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Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 89 of 104
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*Free Fall Sensor*

Size  
A3

Document Number  
**OAK14 Haswell**

Date: Thursday, January 10, 2013

Rev  
**X00**

Sheet 90 of 104

(Blanking)

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**Reserved**

Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 91 of 104
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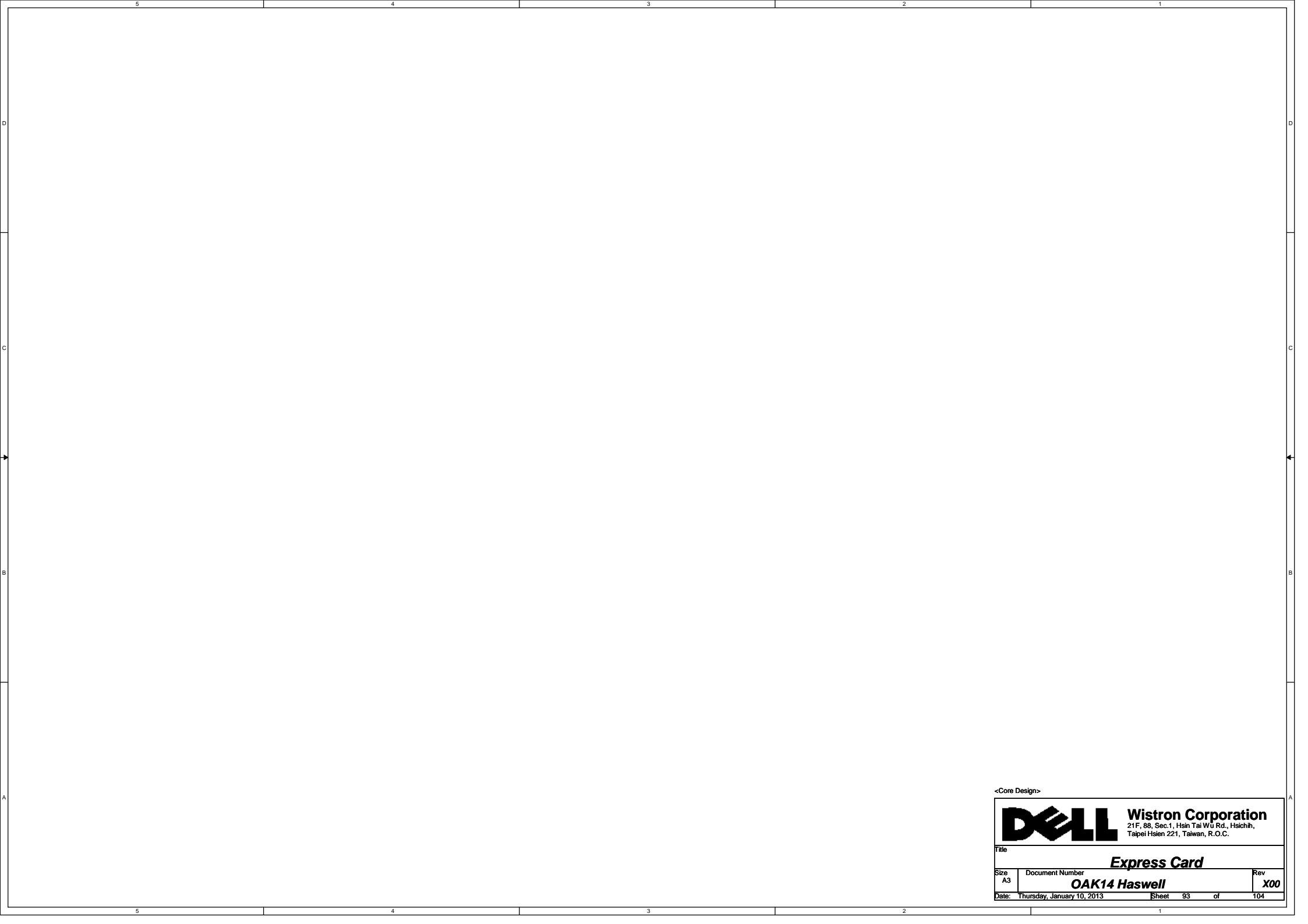
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Size	Document Number	Rev
A3	<b>OAK14 Haswell</b>	<b>X00</b>

Date: Thursday, January 10, 2013	Sheet 92 of 104
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Size A3	Document Number <b>OAK14 Haswell</b>		Rev <b>X00</b>
Date: Thursday, January 10, 2013		Sheet 93 of	104

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Title

LVDS Switch

Size  
A3

Document Number  
**OAK14 Haswell**


Rev  
**X00**

Date: Thursday, January 10, 2013

Sheet 94 of 104

(Blanking)

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Title

CRT Switch

Size

A3

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OAK14 Haswell

Rev

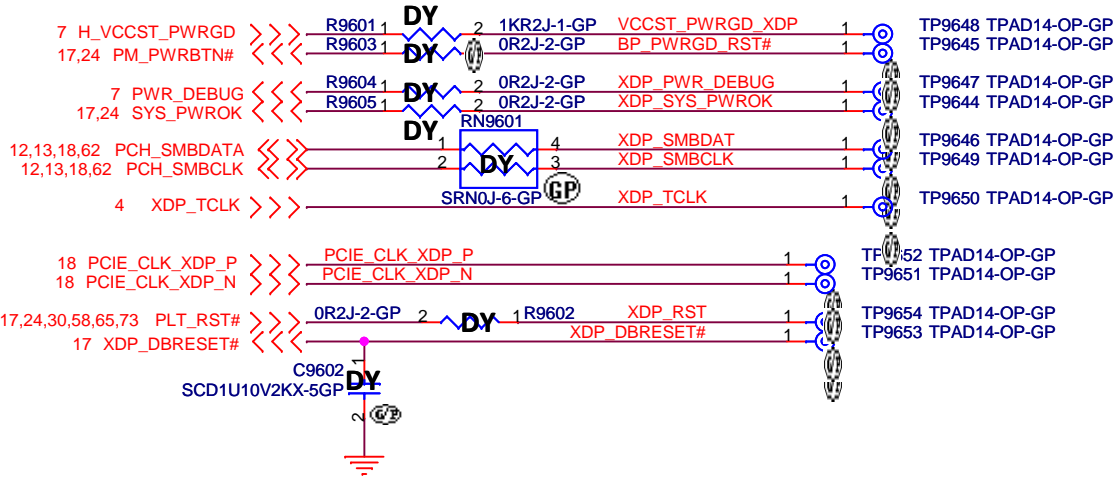
X00

Date: Thursday, January 10, 2013


Sheet 95 of 104

SSID = XDP

CPU XDP



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Title

TOUCH PANEL

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Document Number

Rev

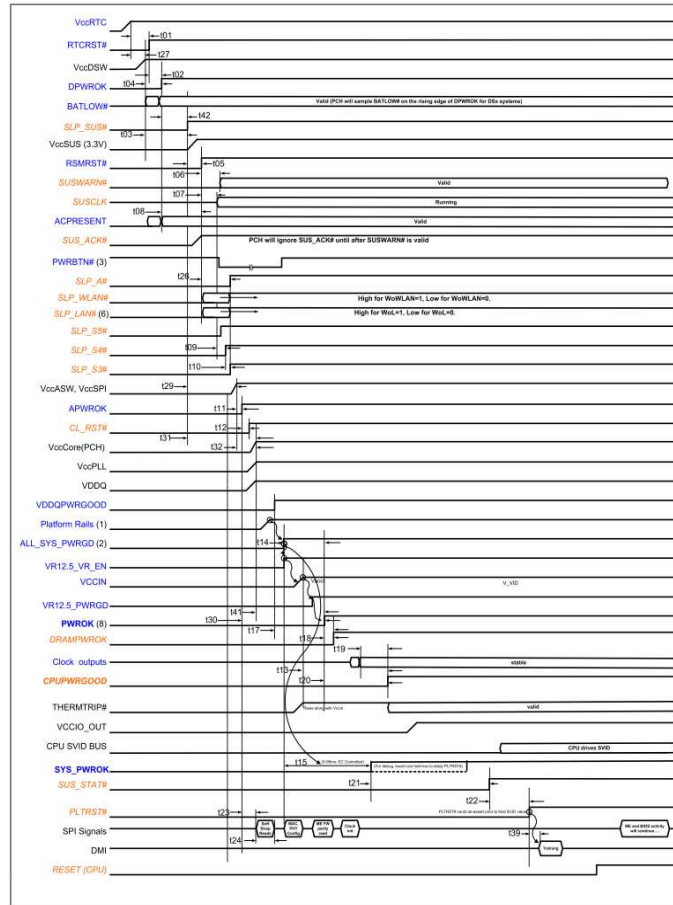
Date: Monday, June 03, 2013

Sheet 96 of 104

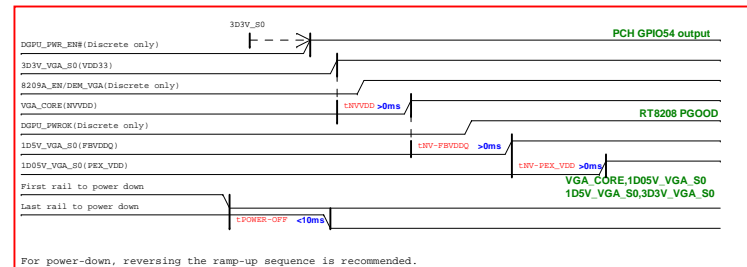
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## Shark Bay Platform Power Sequence

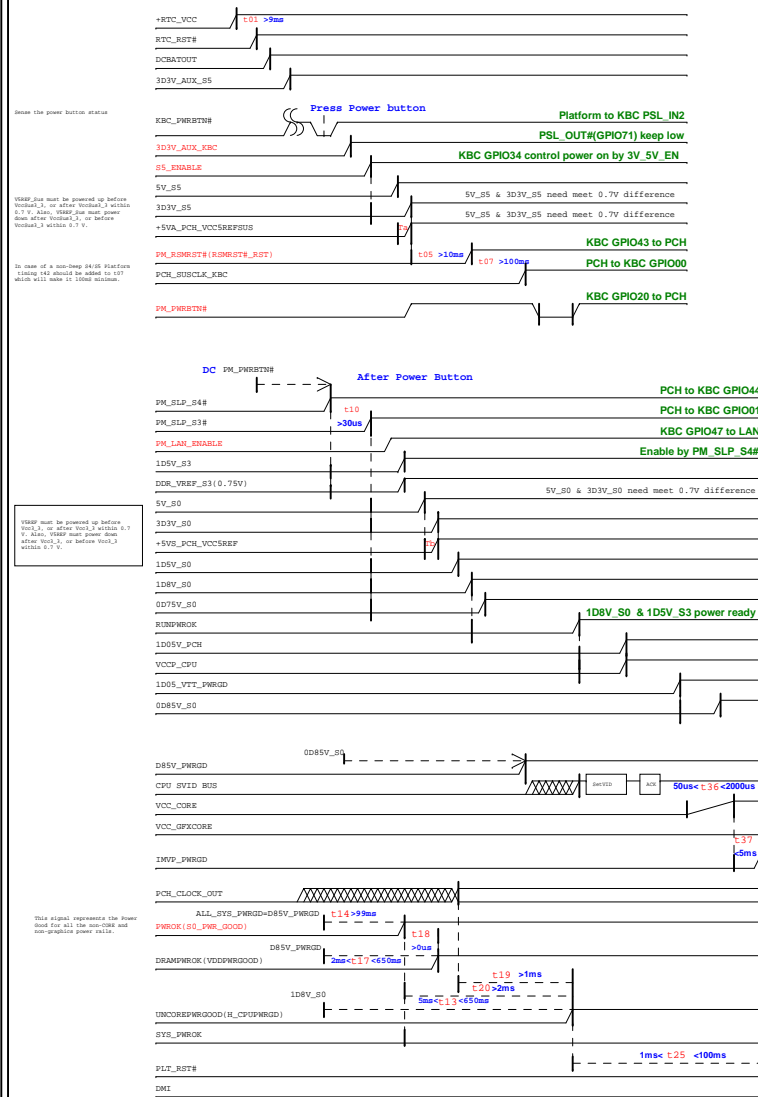


### N14P-GT Power-Up/Down Sequence

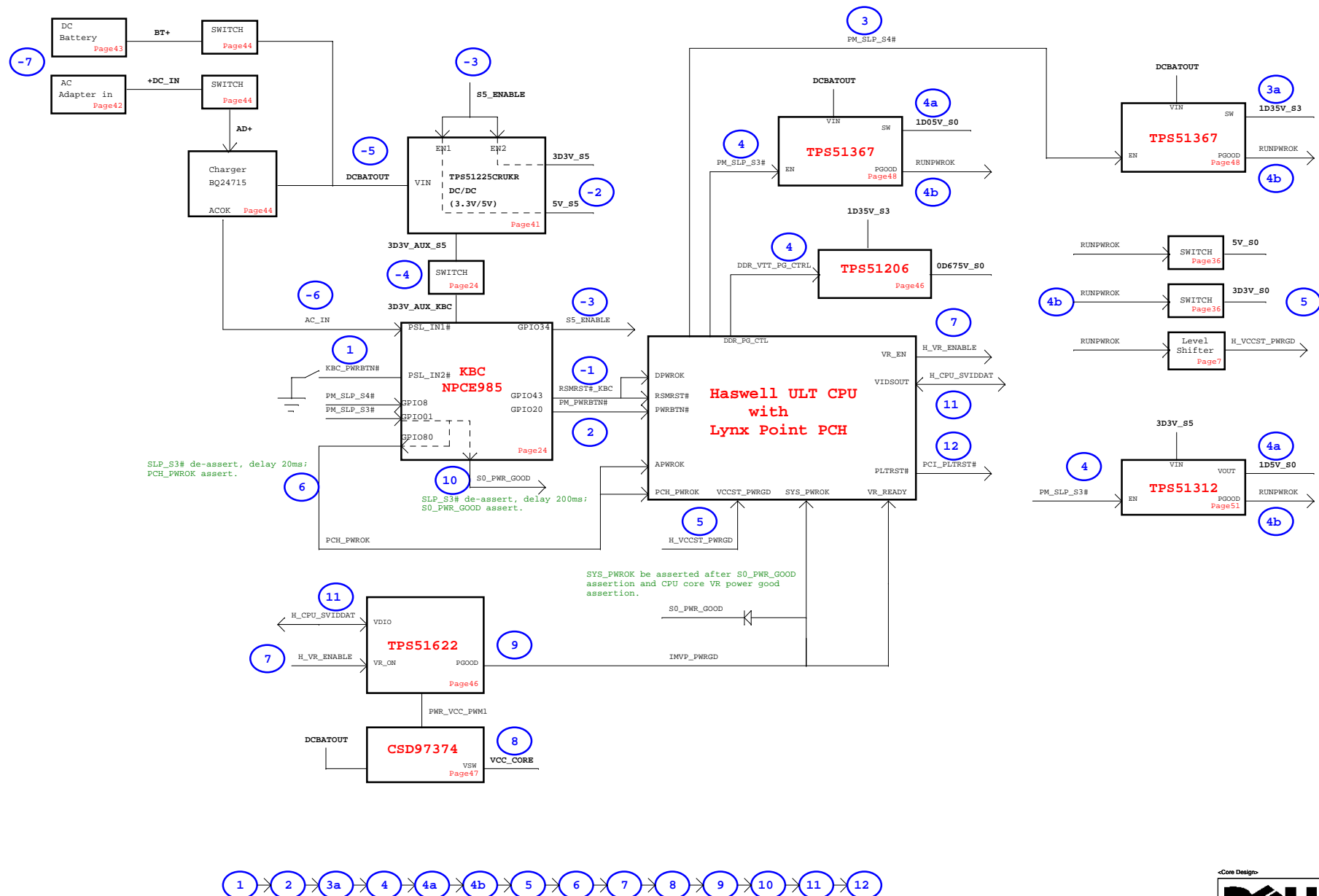


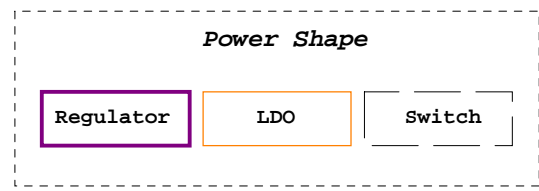
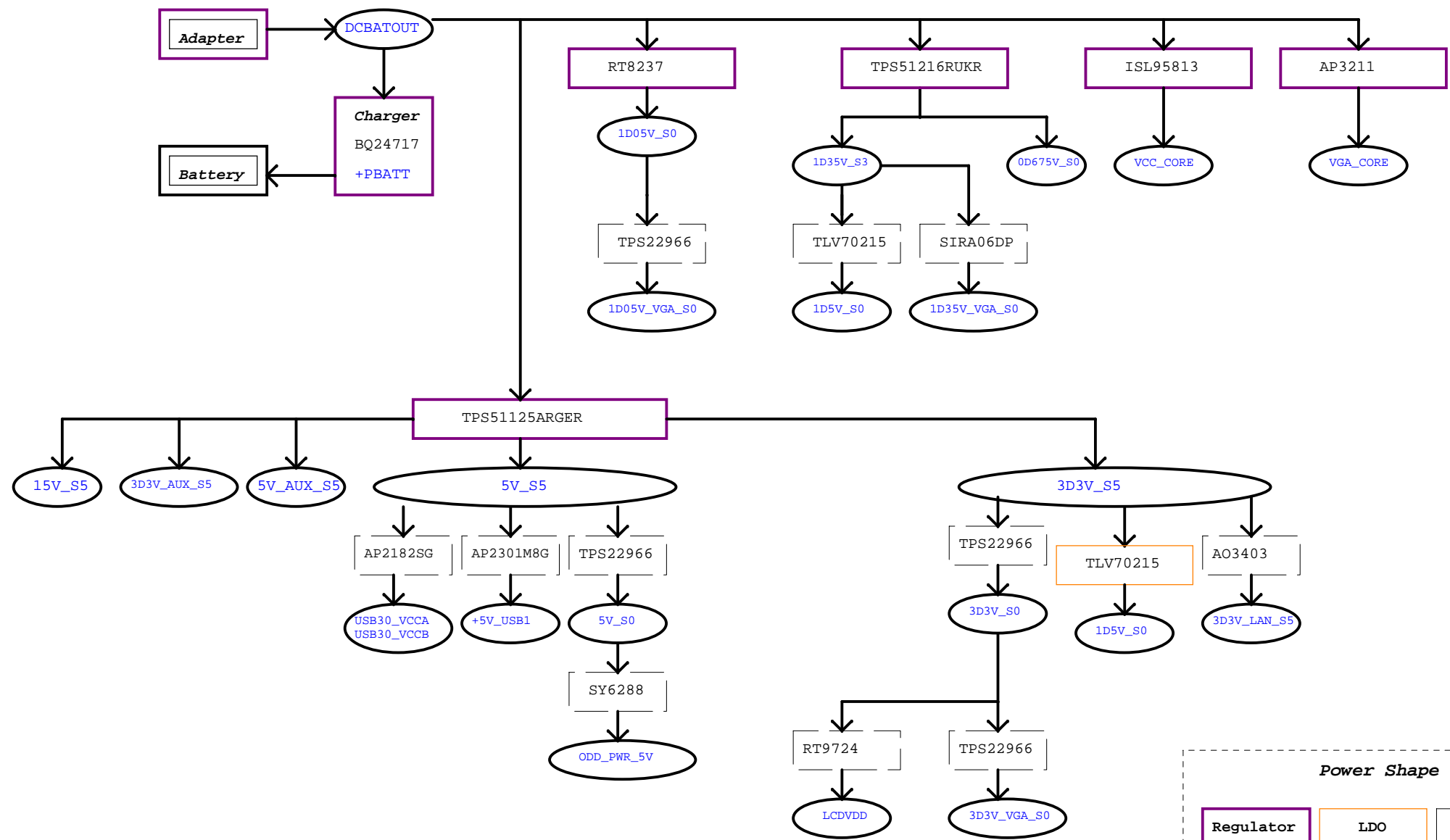
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Red Words: Controlled by EC GPIO

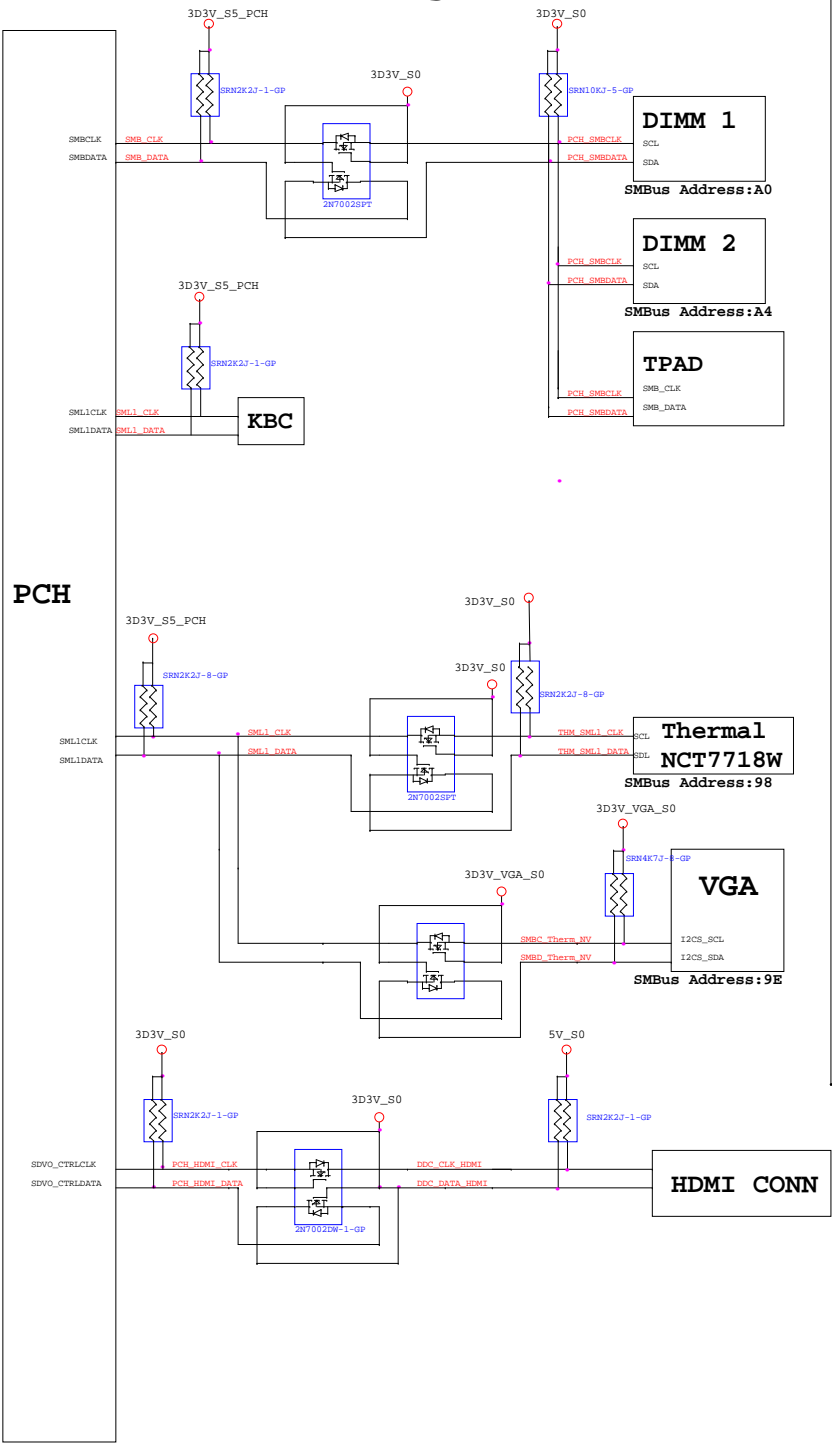


# Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM

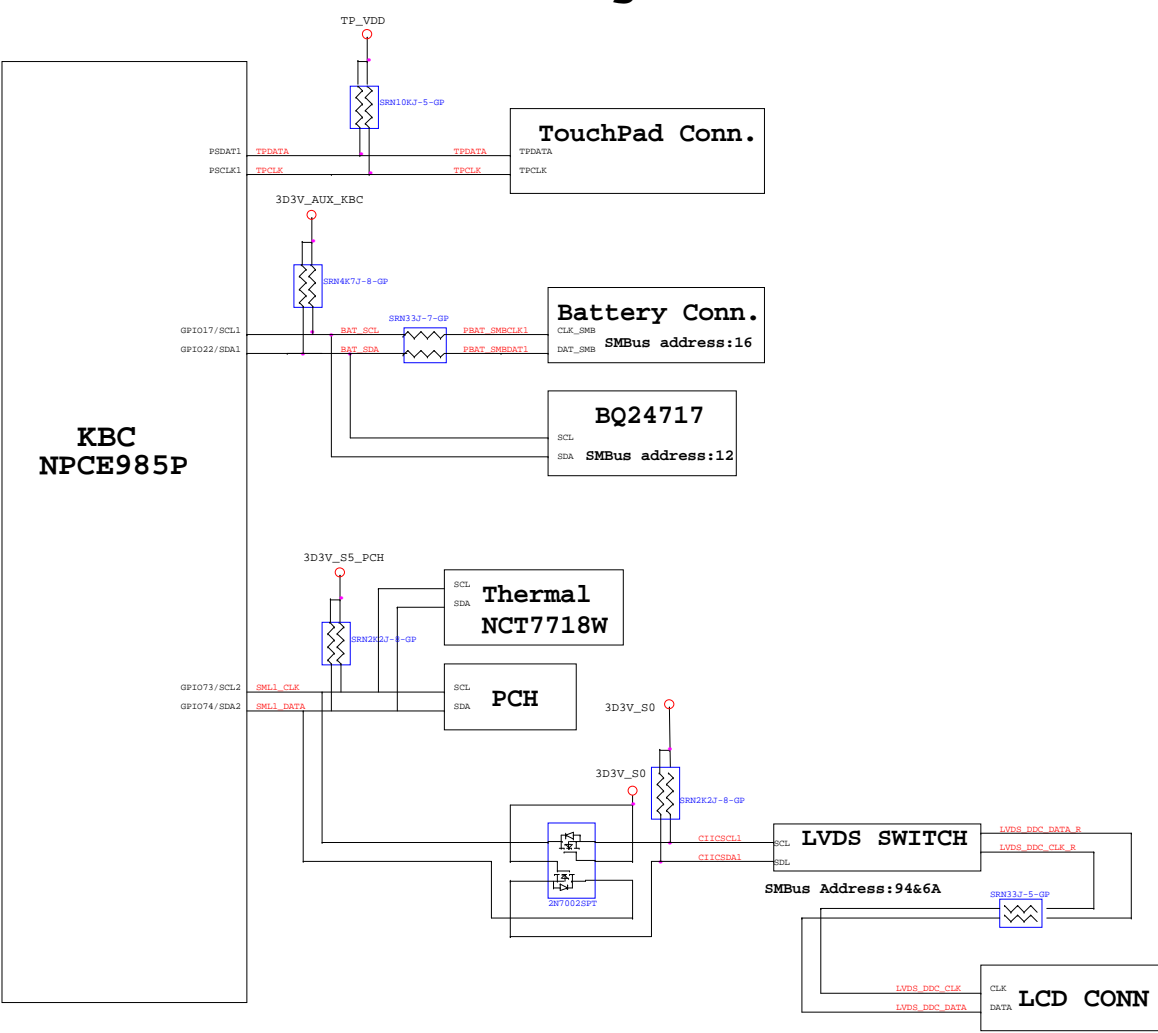




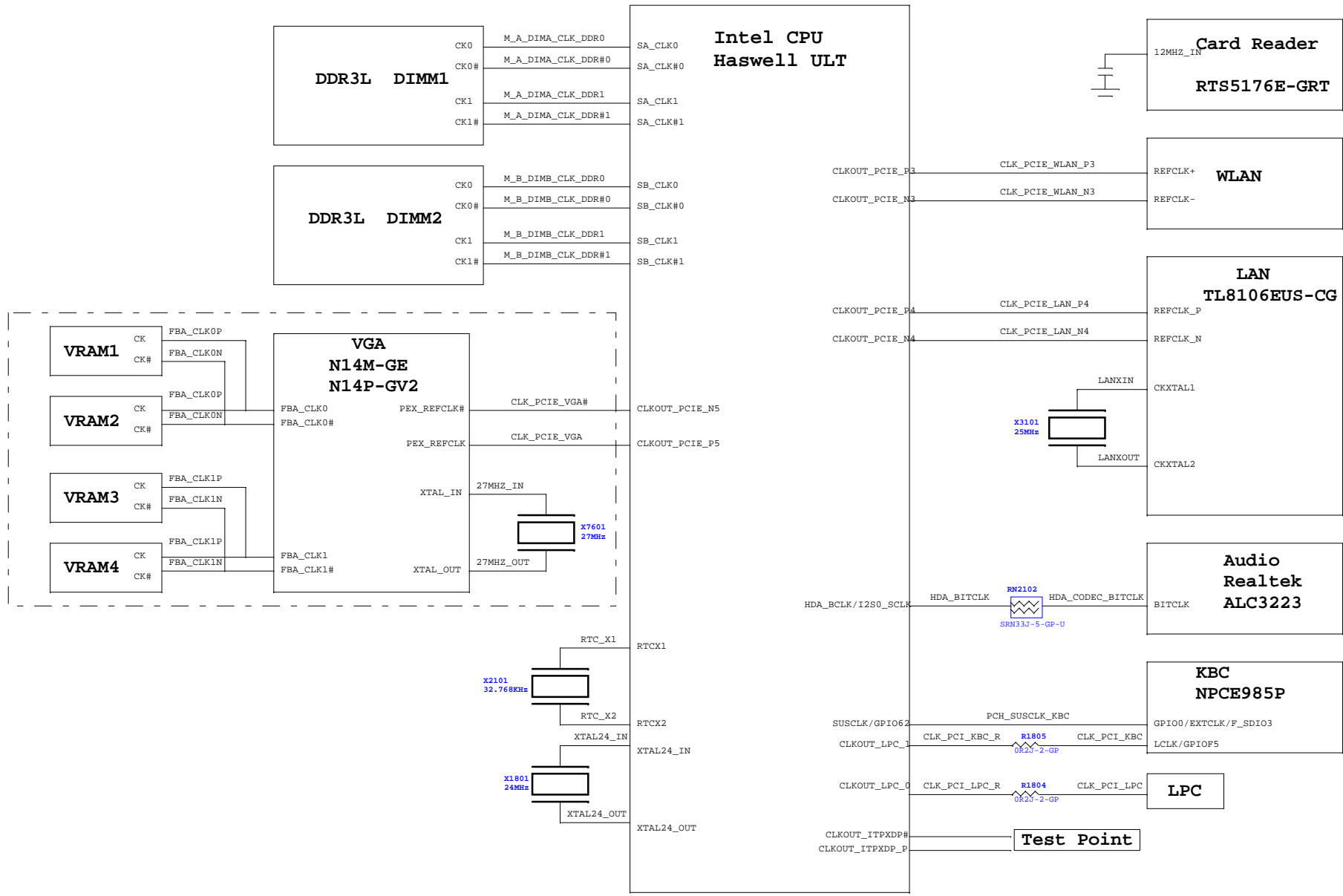
PCH SMBus Block Diagram



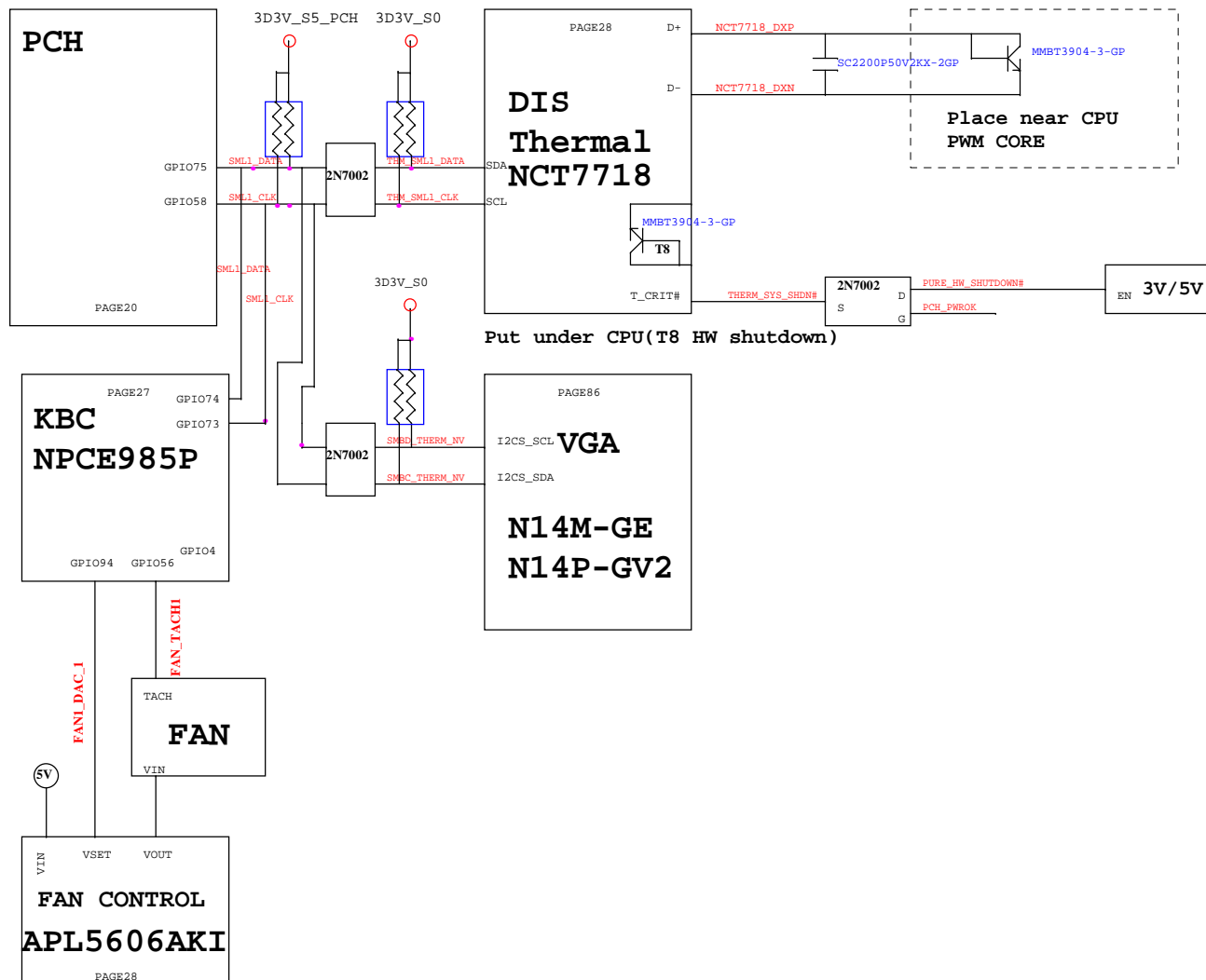
KBC SMBus Block Diagram



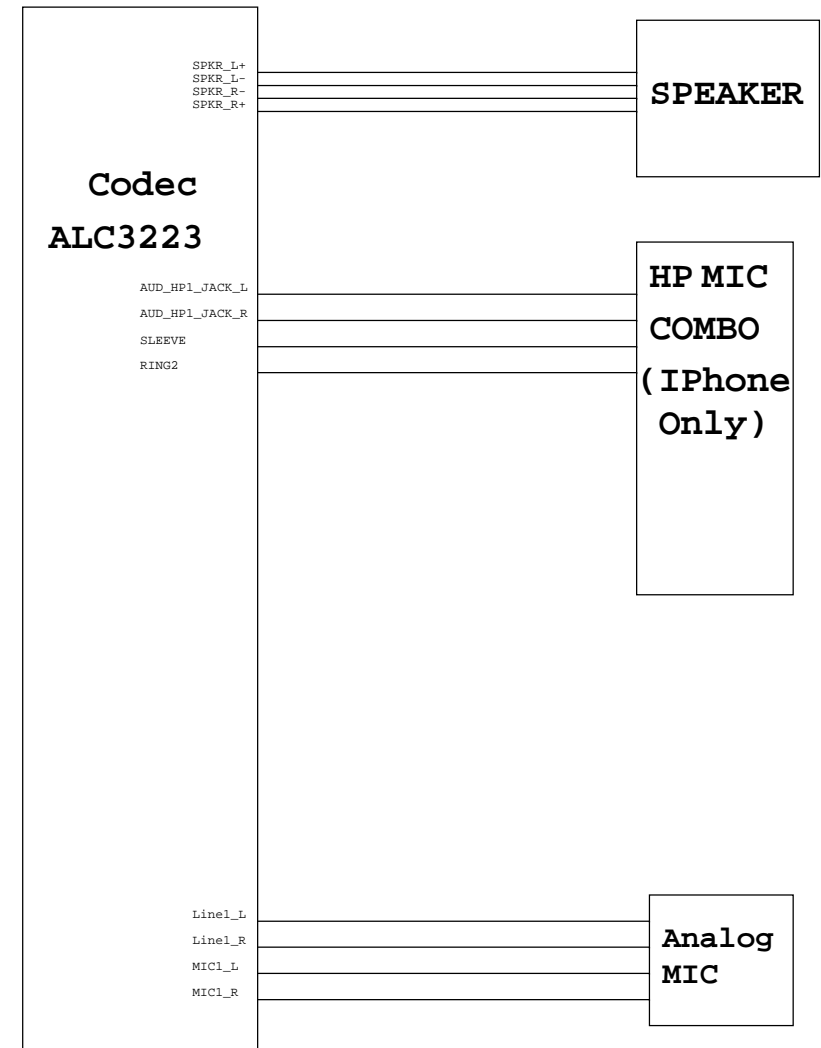
OAK Haswell CLK Block Diagram



## Thermal Block Diagram



## Audio Block Diagram



*Change notes -*

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### Change History

Size	A3
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Document Number
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**OAK14 Haswell**


Rev	X00
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Date: Tuesday, February 26, 2013

Sheet 103 of 104

VERSION	DATA	PAGE	Change Item
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Size  
A3

Document Number  
**OAK14 Haswell**

Rev  
**X00**

Date: Thursday, January 10, 2013

Sheet 104 of 104