Hummingbird1_HR
DIS/UMA/Muxless Schematics Document
Sandy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

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Project code : 91.4QP01.001
PCB P/N :
Revision : 2

Hummingbird1_HR Block Diagram

SYSTEM DC/DC APL5916KAI 48	
INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0

CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

Intel CPU
Sandy Bridge
FSB: 1066 MHz
4,5,6,7,8,9,10,11,12,13

DDRIII 1066/1333 Channel A

RAM x 8 | RAM x 8
RAM x 8 | RAM x 8
RAM x 8 | RAM x 8
RAM x 8 | RAM x 8

FDIx4x2
DMIx4

HDMI 51
LCD 49

HDMI
LVDS(Single Channel)

Intel
PCH
Cougar Point
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
17,18,19,20,21,22,23,24,25,26

FPC
FFC
MINI Board
PCI-E x1
USB x1
Mini-Card
802.11a/b/g
SATA x1
M-SATA
Charger signal
Charger Circuit

Left Side: USB x 2
CAMERA 49
USB2.0 x 3

FFC
Card Reader Board
USB 2.0 x 1
CardReader
RTS5129
SD/MMC

AZALIA
SPI
LPC Bus
SATA x1
HDD 56

Internal Digital MIC
HP1
Azalia CODEC
ALC271X-VB3
29
2CH SPEAKER

Flash ROM 4MB 60
LPC debug port 71

KBC
NUVOTON
NPCE795P 27
SMBus

Touch PAD 69
Int. KB 69
Thermal ENE P2800 28
Fan 28

HR PX

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Title		
Block Diagram		
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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Variant Name>

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Title: Table of Content

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

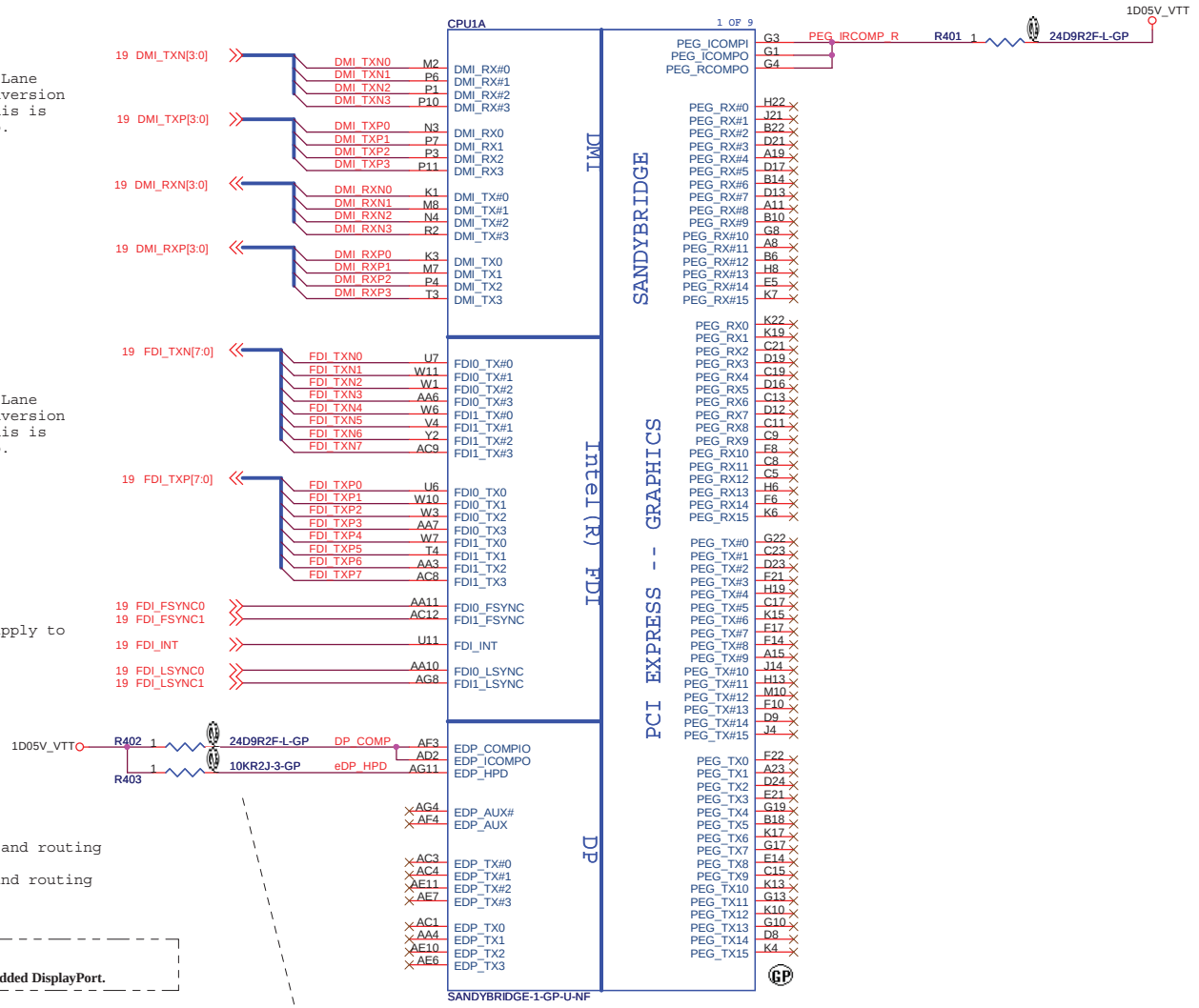
Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.



<Core Design>
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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
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Date: Tuesday, April 17, 2012 Sheet 4 of 102

SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics or without eDP:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

CPU1B — 2 OF 9 — SANDYBRIDGE-1-GP-U-NF

MISC
- PROC_SELECT# F49 ← 18 H_SNB_IVB#
- PROC_DETECT# C57

CLOCKS
- BCLK J3 / BCLK# H2 → CLK_EXP_P 20 / CLK_EXP_N 20
- DPLL_REF_CLK AG3 / DPLL_REF_CLK# AG1 → CLK_DP_P_R / CLK_DP_N_R → RN504 SRN1KJ-7-GP (1,2,3,4) → 1D05V_VTT
- DY
- BCLK_ITP N59 / BCLK_ITP# N58

THERMAL
- CATERR# C49
- PECI A48 ↔ 22,27 H_PECI
- PROCHOT# C45 ← 27,42 H_PROCHOT# ← R513 1 H_PROCHOT# R 56R2J-4-GP ← H_PROCHOT#
- THERMTRIP# D45 ← 22,36 H_THERMTRIP#

1D05V_VTT — R501 1 62R2J-GP — H_PROCHOT#
- C502 SC47P50V2JN-3GP
- CRB : 47pf
- CEKLT:43pf
- Connect EC to PROCHOT# through inverting OD buffer.

DDR3 MISC
- SM_DRAMRST# AT30 ← SM_DRAMRST# 37 ← 4K99R2F-L-GP ← R502
- SM_RCOMP0 BF44 / SM_RCOMP1 BE43 / SM_RCOMP2 BG43 → SM_RCOMP_0 R506 140R2F-GP / SM_RCOMP_1 R507 25D5R2F-GP / SM_RCOMP_2 R508 200R2F-L-GP
- Signal Routing Guideline:
  SM_RCOMP keep routing length less than 500 mils.

PWR MANAGEMENT
- PM_SYNC C48 ← 19 H_PM_SYNC
- UNCOREPWRGOOD B46 ← 22,36,97 H_CPUPWRGD ← R503 1 10KR2J-3-GP
- SM_DRAMPWROK BE45 ← 19,37 PM_DRAM_PWRGD ← R505 1 VDDPWRGOOD 2 0R2J-2-GP (DY) ← 37 VDDPWRGOOD
- RESET# D44 ← BUF_CPU_RST#

JTAG & BPM
- PRDY# N53 / PREQ# N55
- TCK L56 / TMS L55 / TRST# J58 → XDP_TRST#
- TDI M60 / TDO L59 → XDP_TDO
- DBR# K58 → XDP_DBRESET#
- BPM#0 G58 / BPM#1 E55 / BPM#2 E59 / BPM#3 G55 / BPM#4 G59 / BPM#5 H60 / BPM#6 J59 / BPM#7 J61

1D05V_VTT — RN502 SRN51J-GP — XDP_TDO 2 / XDP_TRST# 1

3D3V_S0 — RN503 SRN1K5J-1-GP — XDP_DBRESET# → BUF_CPU_RST# ← 18,27,36,71,82,97 PLT_RST#

<Core Design>

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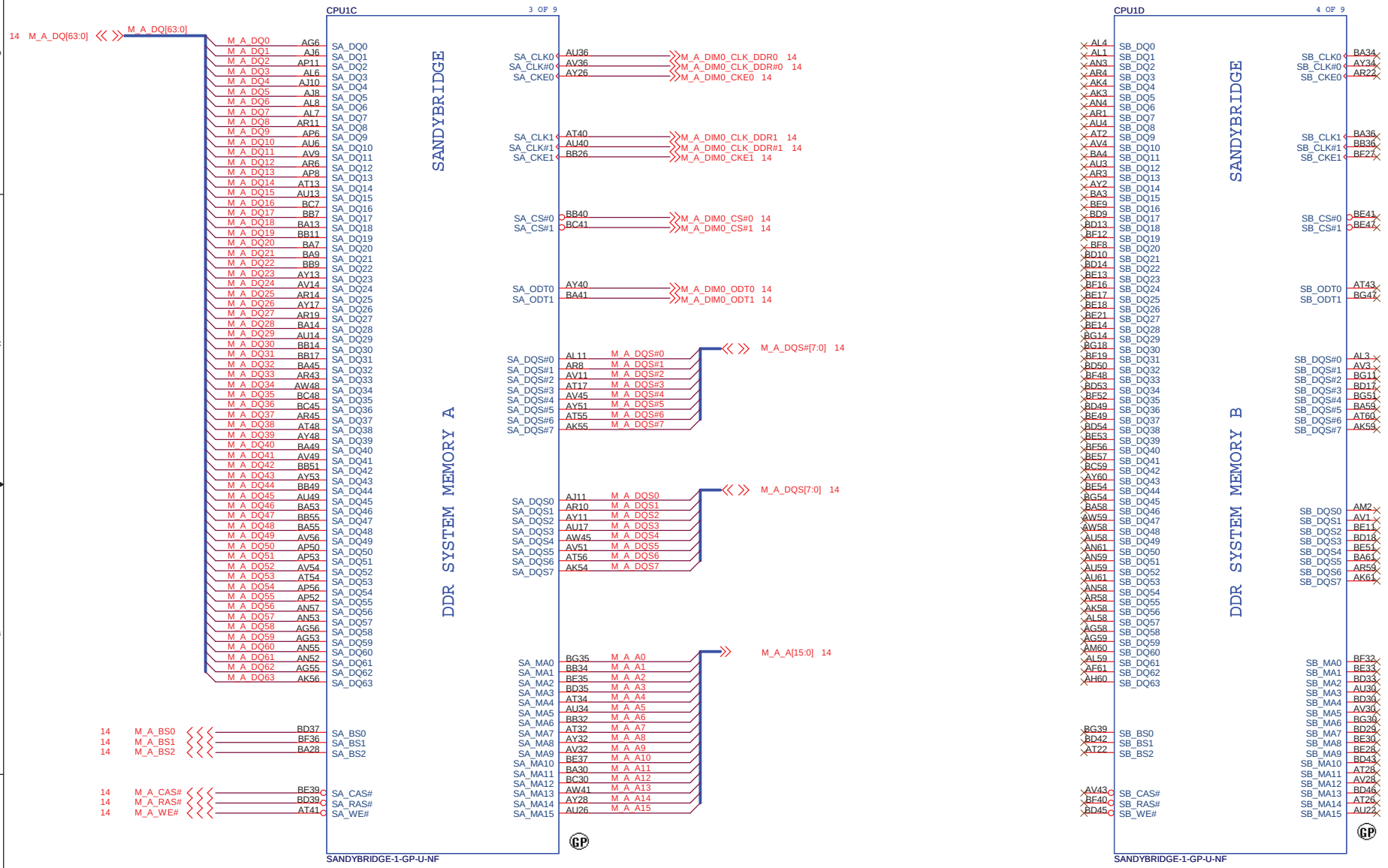
Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 5 of 102

SSID = CPU



<Core Design>

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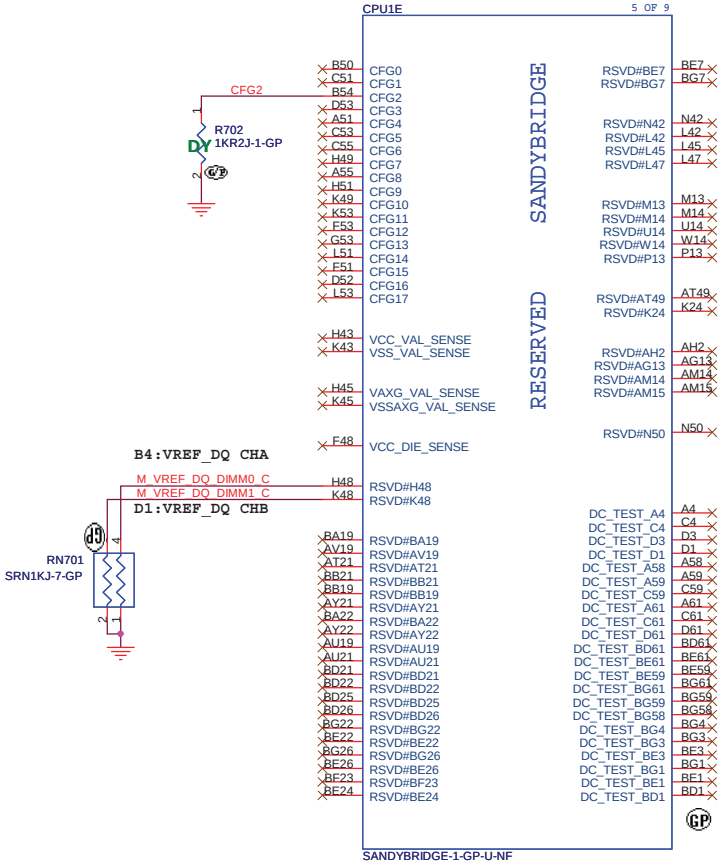
Title: CPU (DDR)

Size	Document Number	Rev
A3	Hummingbird1 HR	-2

Date: Tuesday, April 17, 2012 Sheet 6 of 102

SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

<Core Design>

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Title: CPU (RESERVED)

Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 7 of 102

SSID = CPU

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

VCC_CORE

PROCESSOR CORE POWER: 53A

SC2D2U6D3V2MX-GP: C821, C822, C823, C824, C825, C826, C827, C828, C829, C830, C831, C832, C833, C834

Layout Note: 2.2u Cap place under CPU

SC2D2U6D3V2MX-GP: C837, C841, C847, C848

VCC Output Decoupling CAP Recommendation:

1. 1.9m ohm loadline design: (for 8V)
4 x 470 uF
25 x 22 uF
35 x 2.2uF

2. 2.9m ohm loadline design: (for ULV/LV)
3 x 330uF
12 x 22uF
16 x 2.2uF

CPU1F — 6 OF 9

SANDYBRIDGE

POWER

CORE SUPPLY

PEG AND DDR

QUIET RAILS

SVID

SENSE LINES

VCC_CORE: A26, A29, A31, A34, A35, A38, A39, A42, C26, C27, C32, C34, C37, C39, C42, D27, D32, D34, D37, D39, D42, E26, E28, E32, E34, E37, E38, F25, F26, F28, F32, F34, F37, F38, F42, G42, H25, H26, H28, H29, H32, H34, H35, H37, H38, H40, J25, J26, J28, J29, J32, J34, J35, J37, J38, J40, J42, K26, K27, K29, K32, K34, K35, K37, K39, K42, L25, L28, L33, L36, L40, N26, N30, N34, N38

VCCIO: AF46, AG48, AG50, AG51, AJ17, AJ21, AJ25, AJ43, AJ47, AK50, AK51, AL14, AL15, AL16, AL20, AL22, AL26, AL45, AL48, AM16, AM17, AM21, AM43, AM47, AN20, AN42, AN45, AN48

VCCIO Output Decoupling CAP Recommendation:
2 x 330 uF 10 x 10 uF (0603)
26 x 1uF(0402)

PROCESSOR VCCIO: 8.5A

1D05V_VTT

SC10U6D3V3MX-GP: C853, C854, C856

Layout Note: 10u Cap place during CPU & VR

VCCIO: AA14, AA15, AB17, AB20, AC13, AD16, AD18, AD21, AE14, AE15, AF16, AF18, AF20, AG15, AG16, AG17, AG20, AG21, AJ14, AJ15

SC1U10V2KX-1GP: C857, C858, C859, C860, C861, C862, C863, C864, C866

Layout Note: 1u Cap place under CPU

SC1U10V2KX-1GP: C883, C884, C885, C886, C887, C878, C880

VCCIO: W16, W17

Check Pull high ??

VCCIO_SEL — BC22 H_VCCP_SEL_L — TP805

PROCESSOR 1.05V Quiet rail for DDR block (BGA only)
+V1.05S_VCCPQE should be short to +V1.05S_VCCP_DDR_R on board

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

VCCPQE: AM25, AN22 — +V1.05S_VCCPQE — R806 0R0402-PAD — C877 SC1U6D3V2KX-GP

1D05V_VTT

VIDALERT#: A44 H_CPU_SVIDALRT# — R803 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK: B43 H_CPU_SVIDCLK — H_CPU_SVIDCLK 42
VIDSOUT: C44 H_CPU_SVIDDAT — H_CPU_SVIDDAT 42

R804 130R2F-1-GP

VCC_CORE

Place near processor

R801 100R2F-L1-GP-U

VCC_SENSE: F43 — VCCSENSE 42
VSS_SENSE: G43 — VSSSENSE 42

R805 10R2F-L-GP — 1D05V_VTT

DY

R802 100R2F-L1-GP-U

VCCIO_SENSE: AN16 — VCCIO_SENSE 45
VSS_SENSE_VCCIO: AN17 — VSSIO_SENSE 45

R807 10R2F-L-GP

DY

SANDYBRIDGE-1-GP-U-NF

<Core Design>

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Title: **CPU (VCC_CORE)**

Size: Custom | Document Number: **Hummingbird1_HR** | Rev: -2

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SSID = CPU

CPU1G

7 OF 9

SANDYBRIDGE

POWER

GRAPHICS

DDR3 - 1.5V RAILS

SENSE LINES

1.8V RAIL

QUIET RAILS

SA RAIL

SENSE LINES

SANDYBRIDGE-1-GP-U-NF

S3 power reduction DDR Vref schematic

Refer to the latest Huron River Mainstream PDG (Doc# 438297) for more details

SM_VREF AY43 — +V_SM_VREF_CNT <<< +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

VCC_GFXCORE

VAXG: AA46 AB47 AB50 AB51 AB52 AB53 AB55 AB56 AB58 AB59 AC61 AD47 AD48 AD50 AD51 AD52 AD53 AD55 AD56 AD58 AD59 AE46 N45 P47 P48 P50 P51 P52 P53 P55 P56 P61 T48 T58 T59 T61 U46 U47 V48 V50 V51 V52 V53 V55 V56 V58 V59 W50 W51 W52 W53 W55 W56 W61 Y48 Y61

C919 C940 C941 C942 C943 C949 C950 — SC1U10V2KX-1GP

C911 C912 C913 C914 C915 C916 C917 C918 — SC1U10V2KX-1GP

VAXG Output Decoupling CAP Recommendation:

1. 3.9m ohm loadline design:(for GT2)
2 x 470 uF 6 x 22 uF (0805)
6 x 10 uF (0603) 11 x 1 uF (0402)

2. 4.8m ohm loadline design:(for GT1)
2 x 330 uF 5 x 22 uF (0805)
6 x 10 uF (0603) 6 x 1 uF (0402)

VCC_GFXCORE

R906 10R2F-L-GP

42 VCC_AXG_SENSE
42 VSS_AXG_SENSE

R907 10R2F-L-GP

VCC_AXG_SENSE F45 — VAXG_SENSE
VSS_AXG_SENSE G45 — VSSAXG_SENSE

1D8V_S0

PROCESSOR VCCPLL: 1.2A

BB3 BC1 BC4 — VCCPLL

C928 C929 — SC1U10V2KX-1GP

VCCPLL Output Decoupling CAP Recommendation:
1 x 330 uF
2 x 1 uF (0402)

1D05V_VTT 0D85V_S0

PROCESSOR VCCSA: 6A

R911 Celeron
R910 0R5J-5-GP Celeron
0R5J-5-GP
R913 Celeron
0R5J-5-GP

C921 C923 — SC10U6D3V3MX-GP

Layout Note: Place under CPU

C927 C951 — SC1U10V2KX-1GP

L17 L21 N16 N20 N22 P17 P20 R16 R18 R21 U15 V16 V17 V18 V21 W20 — VCCSA

SM_VREF

VDDQ: AJ28 AJ33 AJ36 AJ40 AL30 AL34 AL38 AL42 AM33 AM36 AM40 AN30 AN34 AN38 AR26 AR28 AR30 AR32 AR34 AR36 AR40 AV41 AW26 BA40 BB28 BG33

1D5V_S0

PROCESSOR VDDQ: 10A

C930 C931 C932 C933 — SC22U4V3MX-GP

EC901 SCD1U50V3KX-GP

Layout Note: Place during CPU & VR

Layout Note: Place under CPU

C936 C937 C938 C939 C952 C953 C954 C955 C956 — SC1U10V2KX-1GP

Layout Note:
Place near SM_VREF pin

VDDQ Output Decoupling Recommendation:
1 x 330 uF 8 x 10uF (0603)
10 x 1 uF (0402)

1D5V_S0

R909 0R0402-PAD

VCCDQ: AM28 AN26 — +1.5S_VCCD_Q

C948 SC1U6D3V2KX-GP

PROCESSOR DDR 1.5V QUIET RAIL (BGA only)
+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board

VDDQ_SENSE BC43 TP_VDDQ_SENSE — TP901 TPAD14-GP
VSS_SENSE_VDDQ BA43 TP_VDDQ_SENSE — TP902 TPAD14-GP

R912 10R2J-2-GP Notice: pull-high 100k or 10k
Delete off page VCCSA_SENSE SA

VCCSA_SENSE U10 — VCCSA_SENSE

Delete off page H_FC_C22 SA

VID0 VID1 — VCCSA_VID: D48 H_FC_C22, D49 VCCSA_SEL — VCCSA_SEL 48

RN901 SRN1KJ-11-GP-U

Power Delivery DG; #139028
A 1-K pull-down resistor should be placed on the VCCSA_VID lines.

<Core Design>

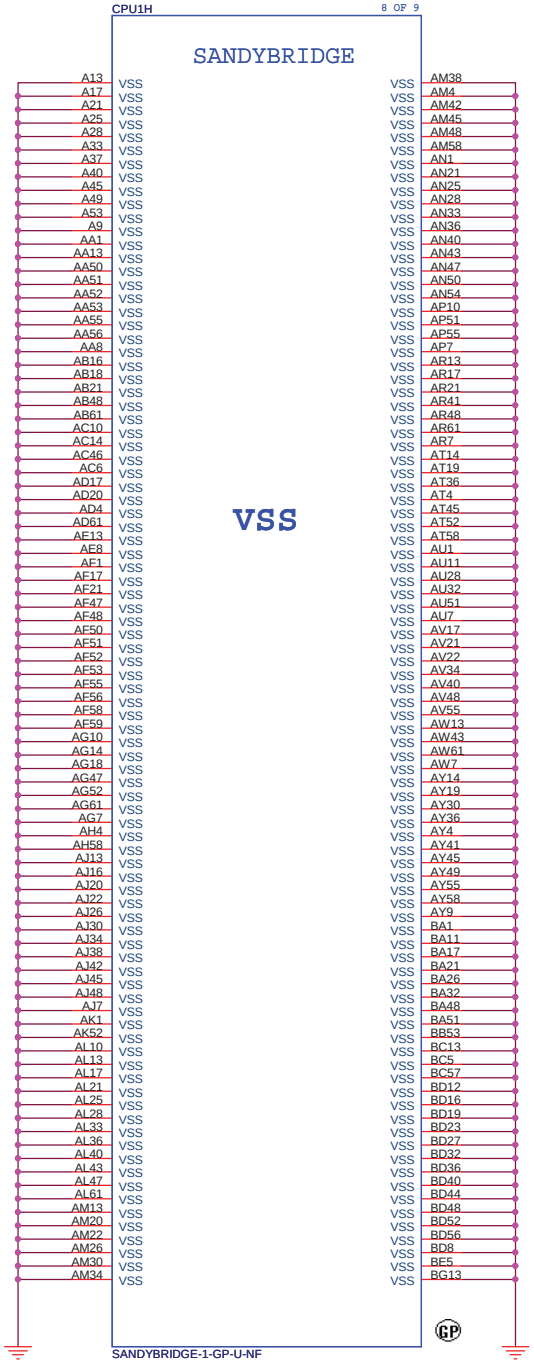
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

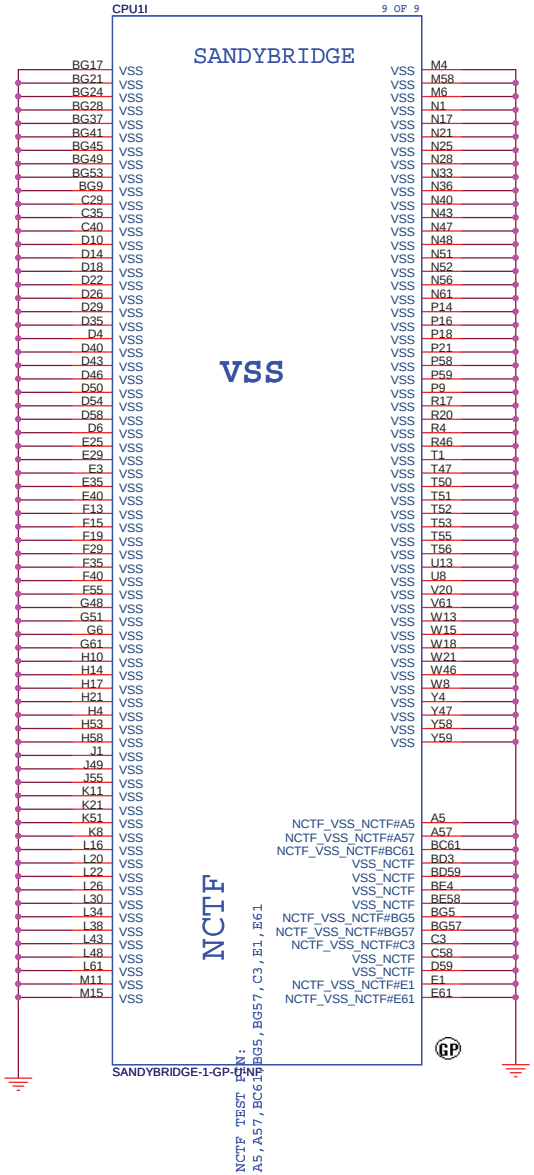
Title: CPU (VCC_GFXCORE)

Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 9 of 102

SSID = CPU





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 10 of 102

Blanking

HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XDP

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 11 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 12 of 102

(Blanking)

<Variant Name>

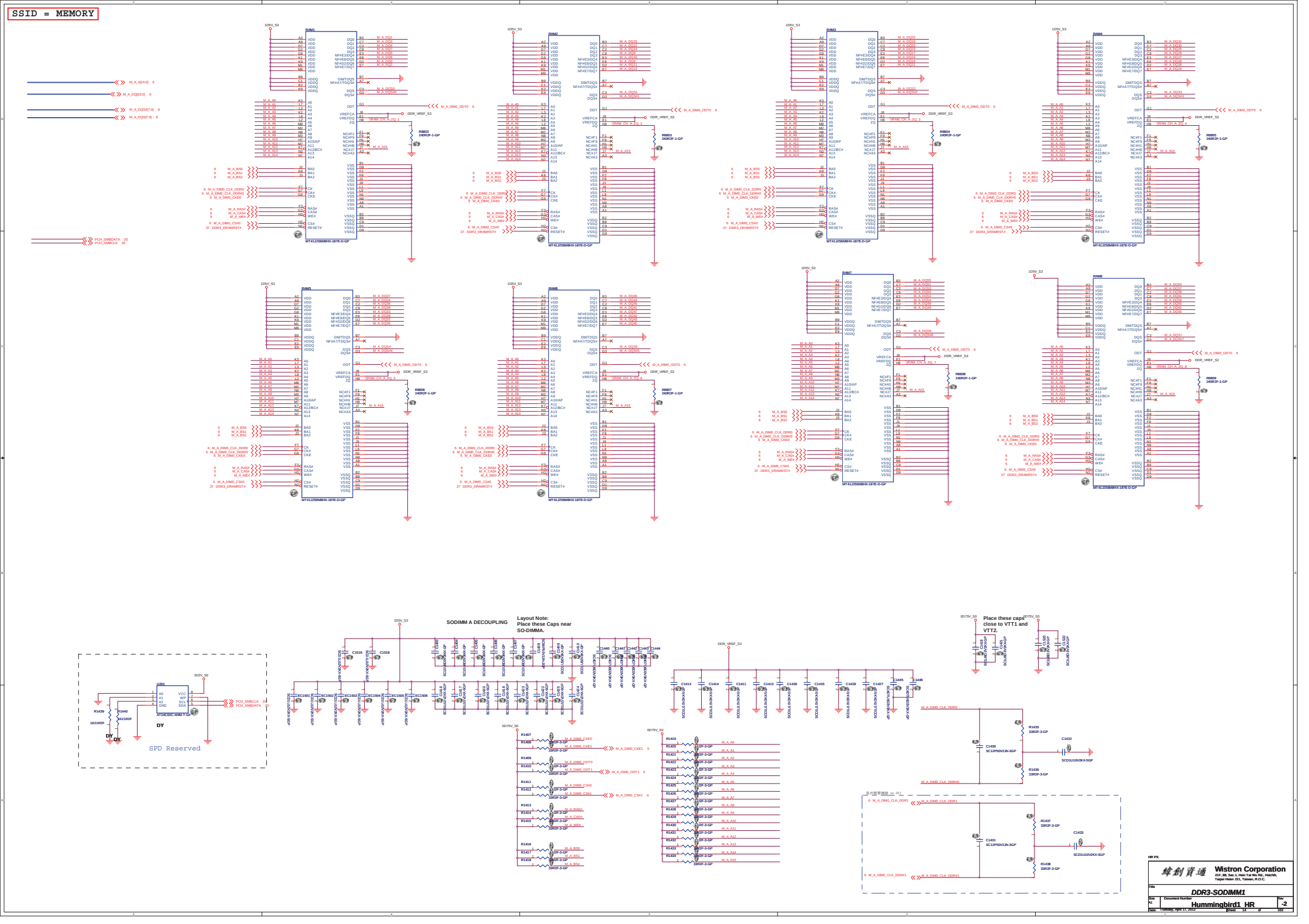
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 13 of 102

SSID = MEMORY


RAM1
RAM2
RAM3
RAM4
RAM5
RAM6
RAM7
RAM8
1D5V_S3
DDR_VREF_S3
MT41J256M8HX-187E-D-GP
SODIMM A DECOUPLING
Layout Note:
Place these Caps near
SO-DIMMA.
Place these caps
close to VTT1 and
VTT2.
SPD Reserved
DY
Wistron Corporation
DDR3-SODIMM1
Hummingbird1_HR
-2

SSID = MEMORY

HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: Custom | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 15 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DDR3-SODIMM2

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 16 of 102

3D3V_S0

RN1703 SRN2K2J-1-GP
LVDS_DDC_CLK
LVDS_DDC_DATA

RN1701 SRN2K2J-1-GP
L_CTRL_DATA
L_CTRL_CLK

RN1702 SRN100KJ-6-GP
PANEL_BLEN
LCDVDD_EN

L_DDC_DATA(PAGE17):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is used for the local flat panel display

Place near PCH

R1701 2K37R2F-GP

RN1704 SRN0J-6-GP

Impedance:90 ohm

PCH1D — 4 OF 10 — Cougar Point — Digital Display Interface

27 PANEL_BLEN, 49 LCDVDD_EN	J47, M45	L_BKLTEN, L_VDD_EN	
49 LBKLT_CTL	P45	L_BKLTCTL	
49 LVDS_DDC_CLK, 49 LVDS_DDC_DATA	T40, K47	L_DDC_CLK, L_DDC_DATA	
L_CTRL_CLK, L_CTRL_DATA	T45, P39	L_CTRL_CLK, L_CTRL_DATA	
LVDS_IBG	AF37	LVD_IBG	
	AF36	LVD_VBG	
LVDS_VREFH	AE48	LVD_VREFH	
LVDS_VREFL	AE47	LVD_VREFL	
49 LVDSA_CLK#, 49 LVDSA_CLK	AK39, AK40	LVDSA_CLK#, LVDSA_CLK	LVDS
49 LVDSA_DATA0#, 49 LVDSA_DATA1#, 49 LVDSA_DATA2#	AN48, AM47, AK47, AJ48	LVDSA_DATA#0, LVDSA_DATA#1, LVDSA_DATA#2, LVDSA_DATA#3	LVDS
49 LVDSA_DATA0, 49 LVDSA_DATA1, 49 LVDSA_DATA2	AN47, AM49, AK49, AJ47	LVDSA_DATA0, LVDSA_DATA1, LVDSA_DATA2, LVDSA_DATA3	LVDS
	AF40, AF39	LVDSB_CLK#, LVDSB_CLK	
	AH45, AH47, AF49, AF45	LVDSB_DATA#0, LVDSB_DATA#1, LVDSB_DATA#2, LVDSB_DATA#3	
	AH43, AH49, AF47, AF43	LVDSB_DATA0, LVDSB_DATA1, LVDSB_DATA2, LVDSB_DATA3	
	N48, P49, T49	CRT_BLUE, CRT_GREEN, CRT_RED	
DDCCLK, DDCDATA	T39, M40	CRT_DDC_CLK, CRT_DDC_DATA	CRT
	M47, M49	CRT_HSYNC, CRT_VSYNC	
DAC_IREF_R	T43, T42	DAC_IREF, CRT_IRTN	
	AP43, AP45	SDVO_TVCLKINN, SDVO_TVCLKINP	
	AM42, AM40	SDVO_STALLN, SDVO_STALLP	
	AP39, AP40	SDVO_INTN, SDVO_INTP	
SDVO_CTRLCLK, SDVO_CTRLDATA	P38, M39	SDVO_CTRLCLK, SDVO_CTRLDATA	
	AT49, AT47, AT40	DDPB_AUXN, DDPB_AUXP, DDPB_HPD	
	AV42, AV40, AV45, AV46, AU48, AU47, AV47, AV49	DDPB_0N, DDPB_0P, DDPB_1N, DDPB_1P, DDPB_2N, DDPB_2P, DDPB_3N, DDPB_3P	
	P46, P42	DDPC_CTRLCLK, DDPC_CTRLDATA	
	AP47, AP49, AT38	DDPC_AUXN, DDPC_AUXP, DDPC_HPD	
	AY47, AY49, AY43, AY45, BA47, BA48, BB47, BB49	DDPC_0N, DDPC_0P, DDPC_1N, DDPC_1P, DDPC_2N, DDPC_2P, DDPC_3N, DDPC_3P	
	M43, M36	DDPD_CTRLCLK, DDPD_CTRLDATA	
	AT45, AT43, BH41	DDPD_AUXN, DDPD_AUXP, DDPD_HPD	
	BB43, BB45, BF44, BE44, BF43, BE42, BJ42, BG42	DDPD_0N, DDPD_0P, DDPD_1N, DDPD_1P, DDPD_2N, DDPD_2P, DDPD_3N, DDPD_3P	

COUGAR-GP-U2-NF

3D3V_S0

RN1707 SRN4K7J-8-GP

R1702 1KR2D-1-GP

Close to PCH side

Delete CRT pull down resistor

3D3V_S0

RN1706 SRN2K2J-1-GP

DDI Port B Detect:(SDVO_CTRL_ DATA)
1: Port B detected
0: Port B not detected

PCH_HDMI_CLK 51
PCH_HDMI_DATA 51

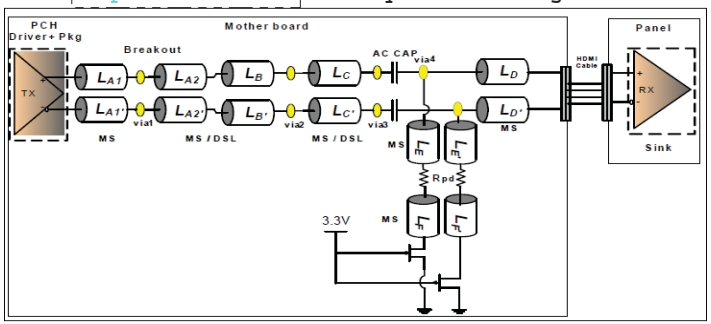
HDMI_PCH_DET 51

DDBP_DATA2#	HDMI	1	C1701	SCD1U10V2KX-5GP
DDBP_DATA2	HDMI	1	C1702	SCD1U10V2KX-5GP
DDBP_DATA1#	HDMI	1	C1703	SCD1U10V2KX-5GP
DDBP_DATA1	HDMI	1	C1704	SCD1U10V2KX-5GP
DDBP_DATA0#	HDMI	1	C1705	SCD1U10V2KX-5GP
DDBP_DATA0	HDMI	1	C1706	SCD1U10V2KX-5GP
DDBP_CLK#	HDMI	1	C1707	SCD1U10V2KX-5GP
DDBP_CLK	HDMI	1	C1708	SCD1U10V2KX-5GP

HDMI_DATA2_R#	51
HDMI_DATA2_R	51
HDMI_DATA1_R#	51
HDMI_DATA1_R	51
HDMI_DATA0_R#	51
HDMI_DATA0_R	51
HDMI_CLK_R#	51
HDMI_CLK_R	51

Close to Connector side

Impedance:90 ohm TM request to change 85-ohm



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size: A3 | Document Number: Hummingbird1 HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 17 of 102

SSID = PCH

RN1801
SRN8K2J-2-GP-U

INT_PIRQF#	1	10	3D3V_S0
INT_PIRQD#	2	9	USB30_SMI#
INT_PIRQC#	3	8	INT_PIRQA#
INT_PIRQB#	4	7	INT_PIRQE#
3D3V_S0	5	6	INT_PIRQH#

GP

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

RN1803
SRN10KJ-5-GP
DY

DGPU_HOLD_RST# 2
DGPU_PWR_EN# 1
4

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

PCH1E
5 OF 10
Cougar Point
RSVD
NVRAM
PCI
USB

TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20
TP21 TP22 TP23 TP24
TP25 TP26 TP27 TP28 TP29 TP30 TP31 TP32 TP33 TP34 TP35 TP36 TP37 TP38 TP39 TP40

RSVD
DF_TVS
NV_CLE

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P
USBRBIAS# USBRBIAS

USB_PN1 61 USB_PP1 61
USB_PN5 82 USB_PP5 82
USB_PN9 61 USB_PP9 61
USB_PN11 82 USB_PP11 82
USB_PN12 49 USB_PP12 49
USB_RBIAS
R1811 22D6R2F-L1-GP

INT_PIRQA# INT_PIRQB# INT_PIRQC# INT_PIRQD#
PIRQA# PIRQB# PIRQC# PIRQD#
REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54
GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55
DGPU_HOLD_RST# DGPU_SELECT# DGPU_PWR_EN#
DGPU_PWM_SELECT#

INT_PIRQE# INT_PIRQF# USB30_SMI# INT_PIRQH#
PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5

PME# PLTRST#
5,27,36,71,82,97 PLT_RST#

CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4
CLK_PCI_LPC_R CLK_PCI_FB_R CLK_PCI_KBC_R
R1804 R1805 R1806 22R2J-2-GP

DEBUG Card 71 CLK_PCI_LPC
PCH 20 CLK_PCI_FB
KBC 27 CLK_PCI_KBC

OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO9 OC6#/GPIO10 OC7#/GPIO14
3D3V_S5
R1820 10KR2J-3-GP
OC

COUGAR-GP-U2-NF

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

TPAD14-GP TP1806
TPAD14-GP TP1804
Strap pin ,Internal PU

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

CRB : 2.2K
CEKLT: 1K

Sandy Bridge / Ivy Bridge Processor
PROC_SELECT# connected to DF_TVS via 1kΩ (MB) , via 4.7kΩ (DT).
DF_TVS needs PU via 2.2kΩ to VccDFTERM

1D8V_S0
R1808 2K2R2J-2-GP
R1809 1KR2J-1-GP
NV_CLE
H_SNB_IVB# 5

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	Touch Panel / 3G SIM(DY)
1	USB Ext. port 1 (HS)
2	Fingerprint(DY)
3	BLUETOOT
4	Mini Card2 (WWAN) (DY)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA(DY)
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card(DY)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

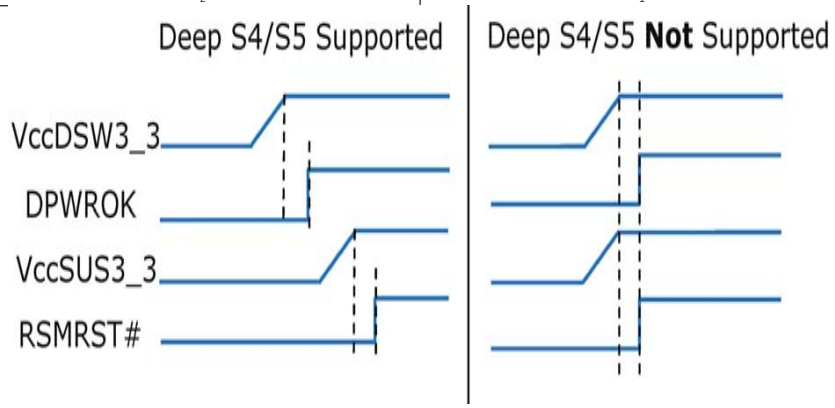
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: Hummingbird1 HR | Rev: -2
Date: Tuesday, April 17, 2012 | Sheet 18 of 102

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

PCH1C — 3 OF 10 — Cougar Point — System Power Management — COUGAR-GP-U2-NF

DMI: DMI0RXN/DMI1RXN/DMI2RXN/DMI3RXN, DMI0RXP/DMI1RXP/DMI2RXP/DMI3RXP, DMI0TXN/DMI1TXN/DMI2TXN/DMI3TXN, DMI0TXP/DMI1TXP/DMI2TXP/DMI3TXP

FDI: FDI_RXN0–7, FDI_RXP0–7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

DMI_ZCOMP, DMI_IRCOMP, DMI2RBIAS

SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT/GPIO31, BATLOW#/GPIO72, RI#

DSWVRMEN, DPWROK, WAKE#, CLKRUN#/GPIO32, SUS_STAT#/GPIO61, SUSCLK/GPIO62, SLP_S5#/GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN#/GPIO29

R1901 49D9R2F-GP DMI_COMP_R; R1902 750R2F-GP RBIAS_CPY (1D05V_VTT)

R1926 10KR2J-3-GP DY; R1904 100KR2J-1-GP — SYS_PWROK, PWROK

R1905 10KR2J-3-GP — SUS_PWR_ACK, SYS_RESET#

R1924 0R0402-PAD — PWROK, 27,42 S0_PWR_GOOD

R1910 0R0402-PAD DY; R1911 10KR2J-3-GP — PCH_DPWROK, PM_RSMRST#, RTC_AUX_S5

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5 — R1917 330KR2J-L1-GP; R1918 330KR2J-L1-GP DY — DSWODVREN

R1919 8K2R2J-3-GP (3D3V_S0) — PM_CLKRUN#

RN1901 SRN10KJ-6-GP (3D3V_S5) — BATLOW#, AC_PRESENT, SUS_PWR_ACK, PM_RI#

R1921 10KR2J-3-GP — PCIE_WAKE#

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

R1908 100KR2J-1-GP — PM_RSMRST#

PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K

3D3V_AUX_S5: R1909 100KR2J-1-GP; R1916 10KR2J-3-GP — 3V_5V_POK_#

Q1901 2N7002KDW-GP — PM_RSMRST# → R1912 1KR2J-1-GP → RSMRST#_KBC 27; 3V_5V_POK 41

84.2N702.A3F
2nd = 84.DM601.03F

<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**
Size: A3 | Document Number: **Hummingbird1_HR** | Rev: **-2**
Date: Tuesday, April 17, 2012 | Sheet 19 of 102

SSID = PCH

USB3.0 CLK

RN2018 SRN10KJ-5-GP
PCIE_CLK_RQ2#
CLK_PCIE_WLAN_REQ1#

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

check list:
A 10K-ohm PU still need to be used

WWAN CLK

WLAN CLK

PCH1B — 2 OF 10

Cougar Point

PCI-E*
- PERN1 / PERP1 / PETN1 / PETP1 — W-WAN
- PERN2 / PERP2 / PETN2 / PETP2 — WLAN
- PERN3 / PERP3 / PETN3 / PETP3 — Card Reader
- PERN4 / PERP4 / PETN4 / PETP4 — LAN
- PERN5 / PERP5 / PETN5 / PETP5 — USB3.0
- PERN6 / PERP6 / PETN6 / PETP6 — Intel GBE LAN
- PERN7 / PERP7 / PETN7 / PETP7 — Dock
- PERN8 / PERP8 / PETN8 / PETP8 — NEW CARD

82 PCIE_RXN6
82 PCIE_RXP6
82 PCIE_TXN6
82 PCIE_TXP6
C2001 SCD1U10V2KX-5GP PCIE_TXN6_C
C2002 SCD1U10V2KX-5GP PCIE_TXP6_C

SMBUS
- SMBALERT#/GPIO11 E12 — EC_SW# 27
- SMBCLK H14 — SMB_CLK
- SMBDATA C9 — SMB_DATA
- SML0ALERT#/GPIO60 A12 — DRAMRST_CNTRL_PCH 37
- SML0CLK C8 — SML0_CLK
- SML0DATA G12 — SML0_DATA
- SML1ALERT#/PCHHOT#/GPIO74 C13 — PCH_GPIO74
- SML1CLK/GPIO58 E14 — SML1_CLK 27
- SML1DATA/GPIO75 M16 — SML1_DATA 27

DDR3 DIMM

KBC

Controller Link
- CL_CLK1 M7
- CL_DATA1 T11
- CL_RST1# P10

For DIS_PX mode or MXM mode.

CLOCKS
- CLKOUT_PCIE0N Y40 / CLKOUT_PCIE0P Y39
- CLK_PCIE_WWAN_REQ# — PCIECLKRQ0#/GPIO73 J2
- CLKOUT_PCIE1N AB49 / CLKOUT_PCIE1P AB47
- CLK_PCIE_WLAN_REQ1# — PCIECLKRQ1#/GPIO18 M1
- CLKOUT_PCIE2N AA48 / CLKOUT_PCIE2P AA47
- PCIE_CLK_RQ2# — PCIECLKRQ2#/GPIO20 V10
- CLKOUT_PCIE3N Y37 / CLKOUT_PCIE3P Y36
- PCIE_CLK_LAN_RQ# — PCIECLKRQ3#/GPIO25 A8
- CLKOUT_PCIE4N Y43 / CLKOUT_PCIE4P Y45
- USB3_PEGB_CLKREQ# — PCIECLKRQ4#/GPIO26 L12
- CLKOUT_PCIE5N V45 / CLKOUT_PCIE5P V46
- PCIE_CLK_REQ5# — PCIECLKRQ5#/GPIO44 L14
- CLKOUT_PEG_B_N AB42 / CLKOUT_PEG_B_P AB40
- PEG_B_CLKRQ# — PEG_B_CLKRQ#/GPIO56 E6
- CLKOUT_PCIE6N V40 / CLKOUT_PCIE6P V42
- PCIE_CLK_REQ6# — PCIECLKRQ6#/GPIO45 T13
- CLKOUT_PCIE7N V38 / CLKOUT_PCIE7P V37
- CLK_PCIE_NEW_REQ# — PCIECLKRQ7#/GPIO46 K12
- CLKOUT_ITPXDP_N AK14 / CLKOUT_ITPXDP_P AK13

RN2012 SRN0J-6-GP
82 CLK_PCIE_WLAN#
82 CLK_PCIE_WLAN
CLK_PCH_SRC6_N V45
CLK_PCH_SRC6_P V46
82 CLK_PCIE_WLAN_REQ#

- PEG_A_CLKRQ#/GPIO47 M10 — PEG_CLKREQ# R
- CLKOUT_PEG_A_N AB37 / CLKOUT_PEG_A_P AB38
- CLKOUT_DMI_N AV22 / CLKOUT_DMI_P AU22 — CLK_EXP_N 5 / CLK_EXP_P 5
- CLKOUT_DP_N AM12 / CLKOUT_DP_P AM13
- CLKIN_DMI_N BE18 CLK_BUF_EXP_N / CLKIN_DMI_P BE18 CLK_BUF_EXP_P
- CLKIN_GND1_N BJ30 CLK_BUF_CPYCLK_N / CLKIN_GND1_P BG30 CLK_BUF_CPYCLK_P — RN2008 SRN10KJ-5-GP
- CLKIN_DOT_96N G24 CLK_BUF_DOT96_N / CLKIN_DOT_96P E24 CLK_BUF_DOT96_P
- CLKIN_SATA_N AK7 CLK_BUF_CKSSCD_N / CLKIN_SATA_P AK5 CLK_BUF_CKSSCD_P
- REFCLK14IN K45 CLK_BUF_REF14
- CLKIN_PCILOOPBACK H45 — CLK_PCI_FB 18
- XTAL25_IN V47 XTAL25_IN / XTAL25_OUT V49 XTAL25_OUT
- XCLK_RCOMP Y47 XCLK_RCOMP — R2007 90D9R2F-1-GP — 1D05V_VTT

FLEX CLOCKS
- CLKOUTFLEX0/GPIO64 K43
- CLKOUTFLEX1/GPIO65 F47 VRAM_SIZE3 — VRAM_SIZE3 22
- CLKOUTFLEX2/GPIO66 H47
- CLKOUTFLEX3/GPIO67 K49 DGPU_PRSNT#

COUGAR-GP-U2-NF

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

3D3V_S5
- RN2003 SRN2K2J-1-GP — SMB_CLK / SMB_DATA
- RN2004 SRN2K2J-1-GP — SML0_DATA / SML0_CLK
- RN2005 SRN2K2J-1-GP — SML1_CLK / SML1_DATA
- RN2006 SRN10KJ-5-GP — PCH_GPIO74 / PCIE_CLK_REQ6#
- R2009 1KR2J-1-GP — DRAMRST_CNTRL_PCH

3D3V_S0
- RN2007 SRN2K2J-1-GP
- SMB_DATA — PCH_SMBDATA 14
- Q2001 2N7002KDW-GP 84.2N702.A3F 2nd = 84.DM601.03F
- PCH_SMBCLK 14 — SMB_CLK

3D3V_S5
- R2004 10KR2J-3-GP — PEG_CLKREQ# R
- XTAL25_IN / XTAL25_OUT
- R2006 1M1R2J-GP
- X2001 XTAL-25MHZ-102-GP 82.30020.851 2nd = 82.30020.791
- C2008 SC12P50V2JN-3GP
- C2007 SC12P50V2JN-3GP

3D3V_S0
- RN2010 SRN10KJ-5-GP
- DGPU_PRSNT# — UMA_DIS# 22

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0

Delete Pull down R

check list:
A 10K-ohm PU still need to be used

RN2009 SRN10KJ-L3-GP
- CLK_BUF_REF14
- CLK_BUF_CKSSCD_P
- CLK_BUF_CKSSCD_N
- CLK_BUF_EXP_P
- CLK_BUF_EXP_N
- CLK_BUF_DOT96_N
- CLK_BUF_DOT96_P

need very close to PCH

3D3V_S5
-SA Athero suggest PU 4.7K
- R2003 4K7R2J-2-GP — PCIE_CLK_LAN_RQ#
- RN2001 SRN10KJ-5-GP — CLK_PCIE_WWAN_REQ# / USB3_PEGB_CLKREQ#
- RN2002 SRN10KJ-6-GP — PCIE_CLK_REQ5# / CLK_PCIE_NEW_REQ# / EC_SW# / PCH_GPIO24
- PCH_GPIO24 — PCH_GPIO24 22

<Variant Name>

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Title: PCH (PCI-E/SMBUS/CLOCK/CL)
Size: A3 | Document Number: Hummingbird1 HR | Rev: -2
Date: Tuesday, April 17, 2012 | Sheet 20 of 102

SSID = PCH

RTC_X1 — R2101 10MR2J-L-GP — RTC_X2
X2101 X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.B21
C2101 SC5P50V2CN-2GP — C2102 SC5P50V2CN-2GP
CL = 7pF
Freq tolertance :+/- 20 ppm

RTC_AUX_S5 — RN2104 SRN20KJ-GP-U — C2103 SC1U6D3V2KX-GP
C2104 SC1U6D3V2KX-GP — G2101 GAP-OPEN

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

RTC_AUX_S5 — R2105 330KR2F-L-GP — PCH_INTVRMEN

RTC Reset

29 HDA_CODEC_SYNC — R2122 33R2J-2-GP — HDA_SYNC
29 HDA_CODEC_SDOUT — R2123 33R2J-2-GP — HDA_SDOUT
29 HDA_CODEC_RST# — HDA_RST#
29 HDA_CODEC_BITCLK — RN2102 SRN33J-5-GP-U — HDA_BITCLK

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

+3VS_+1.5VS_HDA_IO — DY R2102 1KR2J-1-GP — HDA_SDOUT

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

+3VS_+1.5VS_HDA_IO — R2103 1KR2J-1-GP — HDA_SYNC

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PCH1A — 1 OF 10 — Cougar Point

RTC: RTCX1 A20 RTC_X1; RTCX2 C20 RTC_X2; RTCRST# D20 RTC_RST#; SRTCRST# G22 SRTC_RST#; INTRUDER# K22 SM_INTRUDER#; INTVRMEN C17 PCH_INTVRMEN (R2104 1M1R2J-GP)

IHDA: HDA_BCLK N34 HDA_BITCLK; HDA_SYNC L34 HDA_SYNC; SPKR T10 29 HDA_SPKR; HDA_RST# K34 HDA_RST#; HDA_SDIN0 E34 29 HDA_SDIN0; HDA_SDIN1 G34; HDA_SDIN2 C34; HDA_SDIN3 A34; HDA_SDO A36 HDA_SDOUT (27 ME_UNLOCK — R2107 1KR2J-1-GP); HDA_DOCK_EN#/GPIO33 C36; HDA_DOCK_RST#/GPIO13 N32

JTAG: JTAG_TCK J3 (R2121 4K7R2J-2-GP — PCH_JTAG_TCK_BUF); JTAG_TMS H7; JTAG_TDI K5; JTAG_TDO H1

SPI: SPI_CLK T3 (27,60 SPI_CLK_R — R2108 33R2J-2-GP — PCH_SPI_CLK); SPI_CS0# Y14 (27,60 SPI_CS0#_R — R2109 33R2J-2-GP — PCH_SPI_CS0#); SPI_CS1# T1; SPI_MOSI V4 (27,60 SPI_SI_R — R2110 33R2J-2-GP — PCH_SPI_SI); SPI_MISO U3 (27,60 SPI_SO_R)

LPC: FWH0/LAD0 C38 LPC_AD0; FWH1/LAD1 A38 LPC_AD1; FWH2/LAD2 B37 LPC_AD2; FWH3/LAD3 C37 LPC_AD3 — LPC_AD[0..3] 27,71
FWH4/LFRAME# D36 — LPC_FRAME# 27,71
LDRQ0# E36; LDRQ1#/GPIO23 K36
SERIRQ V5 — INT_SERIRQ 27

SATA 6G: SATA0RXN AM3 SATA_RXN0 56; SATA0RXP AM1 SATA_RXP0 56; SATA0TXN AP7 SATA_TXN0 56; SATA0TXP AP5 SATA_TXP0 56
SATA1RXN AM10 SATA_RXN1 82; SATA1RXP AM8 SATA_RXP1 82; SATA1TXN AP11 SATA_TXN1 82; SATA1TXP AP10 SATA_TXP1 82

SATA: SATA2RXN AD7; SATA2RXP AD5; SATA2TXN AH5; SATA2TXP AH4
SATA3RXN AB8; SATA3RXP AB10; SATA3TXN AF3; SATA3TXP AF1
SATA4RXN Y7; SATA4RXP Y5; SATA4TXN AD3; SATA4TXP AD1
SATA5RXN Y3; SATA5RXP Y1; SATA5TXN AB3; SATA5TXP AB1
SATAICOMPO Y11; SATAICOMPI Y10 — SATA_COMP — R2112 — 37D4R2F-GP — 1D05V_VTT
SATA3RCOMPO AB12; SATA3COMPI AB13 — SATA3_COMP — R2113 — 49D9R2F-GP — 1D05V_VTT
SATA3RBIAS AH1 — RBIAS_SATA3 — R2114 — 750R2F-GP
SATALED# P3 — SATA_LED# — SATA_LED# 22
SATA0GP/GPIO21 V14 — SATA_DET#0
SATA1GP/GPIO19 P1 — Strap pin ,Internal PU

COUGAR-GP-U2-NF
71.COUGA.00U

check list:8.2K PU
CRB :10K PU

HDD1
M-SATA

HDA_CODEC_BITCLK — EC2102 DY SC4D7P50V2CN-1GP
HDA_CODEC_SDOUT — EC2103 DY SC4D7P50V2CN-1GP
SPI_CS0#_R — EC2101 DY SC4D7P50V2CN-1GP

5V_S0 — Q2101 2N7002K-2-GP (G, S, D) — HDA_SYNC_R — R2124 33R2J-2-GP — HDA_SYNC
HDA_CODEC_SYNC
84.2N702.J31
2ND = 84.2N702.031

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

SWAP pin from Page 22
22 S_GPIO
22,27 PCH_TEMP_ALERT#
RN2103 SRN10KJ-6-GP — 3D3V_S0
S_GPIO
PCH_TEMP_ALERT#
INT_SERIRQ
SATA_DET#0

<Variant Name>

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Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: A3 | Document Number: Hummingbird1 HR | Rev: -2
Date: Tuesday, April 17, 2012 | Sheet 21 of 102

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

3D3V_S0 — RN2203 SRN10KJ-5-GP — H_RCIN# — H_A20GATE

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

PCH1F — 6 OF 10 — Cougar Point

21	S_GPIO	T7	BMBUSY#/GPIO0	TACH4/GPIO68	C40 SATA_ODD_PWRGT — TP2205 TPAD14-GP
	EC_SMI#	A42	TACH1/GPIO1	TACH5/GPIO69	B41 — UMA_DIS# 20
	DGPU_HPD_INTR#	H36	TACH2/GPIO6	TACH6/GPIO70	C41 VRAM_SIZE1
27	EC_SCI#	E38	TACH3/GPIO7	TACH7/GPIO71	A40 VRAM_SIZE2
	ICC_EN#	C10	GPIO8		
	PCH_GPIO12	C4	LAN_PHY_PWR_CTRL/GPIO12		
	PCH_GPIO15	G2	GPIO15	A20GATE	P4 — H_A20GATE 27
3D3V_S0 — R2202 10KR2J-3-GP				PECI	AU16 H_PECI_R — R2203 0R2J-2-GP (DY) — H_PECI 5,27
	SATA_ODD_PRSNT#	U2	SATA4GP/GPIO16	RCIN#	P5 — H_RCIN# 27
check list: if are unused,PU or PD	DGPU_PWROK	D40	TACH0/GPIO17	PROCPWRGD	AY11 — H_CPUPWRGD 5,36,97
TPAD14-GP TP2204	PCH_GPIO22	T5	SCLOCK/GPIO22	THRMTRIP#	AY10 PCH_THERMTRIP_R
20 PCH_GPIO24	PCH_GPIO24	E8	GPIO24/MEM_LED	INIT3_3V#	T14
TPAD14-GP TP2203	PCH_GPIO27	E16	GPIO27		
	PLL_ODVR_EN	P8	GPIO28		
PSW_CLR#		K1	STP_PCI#/GPIO34	TS_VSS1	AH8
G2201 GAP-OPEN	FP_DET#	K4	GPIO35	TS_VSS2	AK11
	DMI_OVRVLTG	V8	SATA2GP/GPIO36	TS_VSS3	AH10
	FDI_OVRVLTG	M5	SATA3GP/GPIO37	TS_VSS4	AK10
	MFG_MODE	N2	SLOAD/GPIO38	NC_1	P37
	GFX_CRB_DET	M3	SDATAOUT0/GPIO39		
	VRAM_SIZE4	V13	SDATAOUT1/GPIO48		
21,27 PCH_TEMP_ALERT#	PCH_TEMP_ALERT#	V3	SATA5GP/GPIO49	NCTF_VSS#BG2	BG2
	USB3_PWR_ON	D6	GPIO57	NCTF_VSS#BG48	BG48
				NCTF_VSS#BH3	BH3
				NCTF_VSS#BH47	BH47
		A4	NCTF_VSS#A4	NCTF_VSS#BJ4	BJ4
		A44	NCTF_VSS#A44	NCTF_VSS#BJ44	BJ44
		A45	NCTF_VSS#A45	NCTF_VSS#BJ45	BJ45
		A46	NCTF_VSS#A46	NCTF_VSS#BJ46	BJ46
		A5	NCTF_VSS#A5	NCTF_VSS#BJ5	BJ5
		A6	NCTF_VSS#A6	NCTF_VSS#BJ6	BJ6
		B3	NCTF_VSS#B3	NCTF_VSS#C2	C2
		B47	NCTF_VSS#B47	NCTF_VSS#C48	C48
		BD1	NCTF_VSS#BD1	NCTF_VSS#D1	D1
		BD49	NCTF_VSS#BD49	NCTF_VSS#D49	D49
		BE1	NCTF_VSS#BE1	NCTF_VSS#E1	E1
		BE49	NCTF_VSS#BE49	NCTF_VSS#E49	E49
		BF1	NCTF_VSS#BF1	NCTF_VSS#F1	F1
		BF49	NCTF_VSS#BF49	NCTF_VSS#F49	F49

NCTF TEST PIN: A4,A44,A45,A46,A5,A6,B3,B47,BD1,BD49,BE1,BE49,BF1,BF49
BG2,BG48,BH3,BH47,BJ4,BJ44,BJ45,BJ46,BJ5,BJ6,C2,C48
D1,D49,E1,E49,F1,F49

COUGAR-GP-U2-NF

GPIO | CPU/MISC | NCTF

PCH_THERMTRIP_R — R2204 390R2F-2GP — H_THERMTRIP# 5,36

design guide and CRB cirucit stuff 390-ohm
JE40_HR stuff 54.9-ohm

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

GFX_CRB_DET — R2206 100KR2J-1-GP

Pass Word Clear

RN2201 SRN10KJ-6-GP — EC_SMI# / EC_SCI# / DGPU_HPD_INTR#
RN2202 SRN10KJ-6-GP — PSW_CLR# / FP_DET# / MFG_MODE / SATA_LED#
SWAP pin from Page 20 — 21 SATA_LED#
RN2204 SRN10KJ-6-GP — SWAP pin from Page 20 — 20 PEG_B_CLKRQ# / USB3_PWR_ON / PCH_GPIO12
PCH_GPIO15 — R2201 1KR2J-1-GP

FDI_OVRVLTG — R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI_OVRVLTG — R2210 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

ICC_EN# — R2211 1KR2J-1-GP

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL_ODVR_EN — R2212 1KR2J-1-GP (DY)

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

3D3V_S0 — R2218 10KR2J-3-GP — PCH_GPIO22 — R2219 10KR2J-3-GP (DY)

3D3V_S0 — R2214 (4G) / R2220 MICRON_ELPIDA / R2216 ELPIDA_S/H — (GPIO70 Pin2) VRAM_SIZE1 / VRAM_SIZE2 (GPIO71 Pin1) — VRAM_SIZE4 (GPIO48 Pin4) — R2221 (2G) / R2215 NANY_S/H / R2217 MICRON_NANY

3D3V_S0 — R2230 DYRAM — VRAM_SIZE3 — VRAM_SIZE3 20 (GPIO65 Pin3) — R2231 RAM

GPIO48 DRAM_Type4	GPIO65 DRAM_Type3	GPIO70 DRAM_Type1	GPIO71 DRAM_Type2	Status
0	0	0	0	Nanya 2G
0	0	0	1	Micron 2G
0	0	1	0	HYNIX 2G
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	Nanya 4G
1	0	0	1	Micron 4G
1	0	1	0	Samsung 4G
1	0	1	1	ELPIDA 4G
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

<Core Design>

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Title: PCH (GPIO/CPU)
Size: A3 | Document Number: Hummingbird1_HR | Rev: -2
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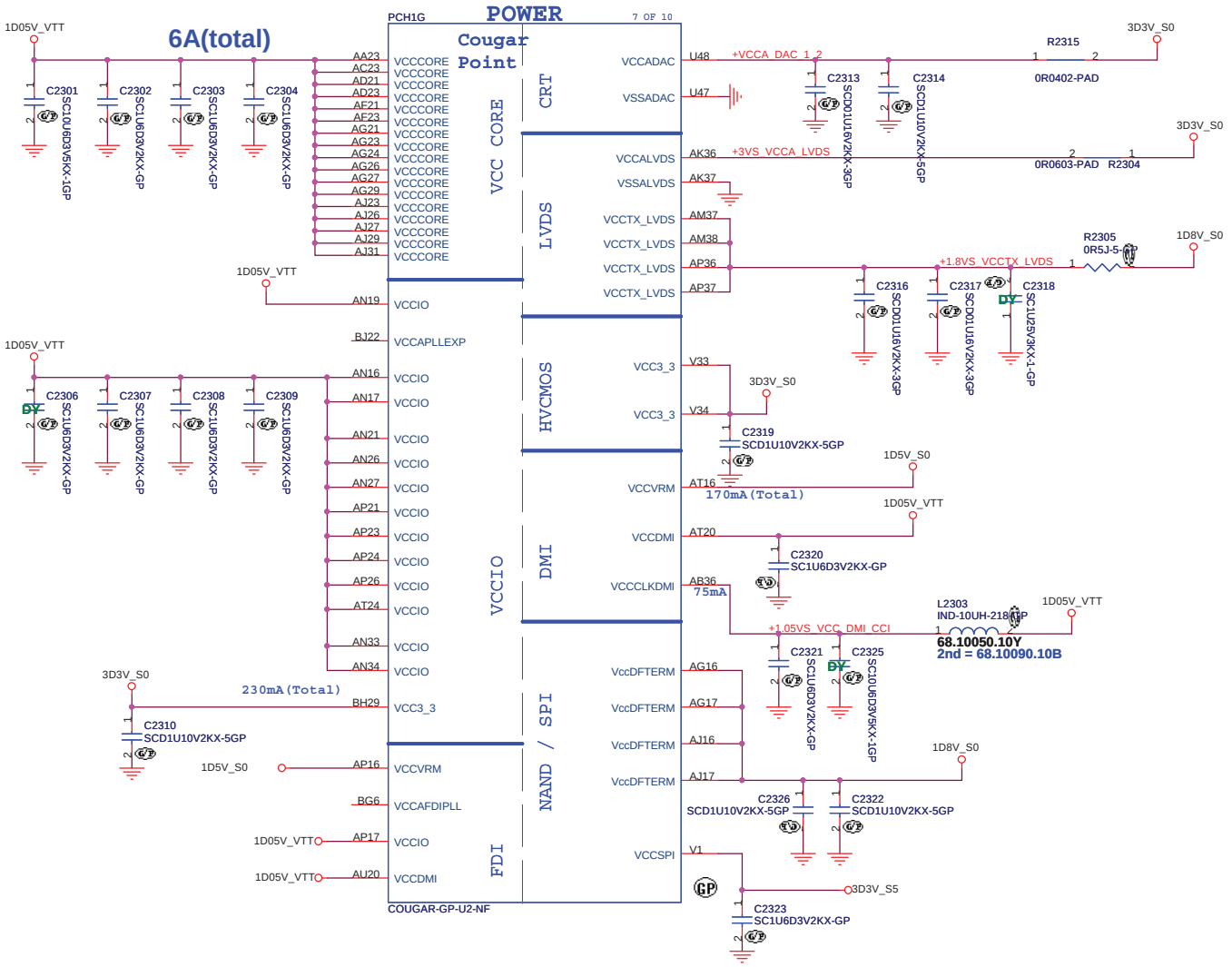

<Variant Name>

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Title: PCH (POWER1)

Size: A3 | Document Number: Hummingbird1 HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 23 of 102

SSID = PCH

PCH1J

POWER

10 OF 10

Cougar Point

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

COUGAR-GP-U2-NF

0.002A

0.097A (Totally current of VCCSUS3_3)

0.001A

1.01A (Total current of VCCASW)

0.16A (Totally current of VCCVRM)

0.055A

0.095A

0.001A

6uA

0.01A

Change to 0603 package

DY

AFR suggest DY Cayp to prevent leakage current

L2402 IND-10UH-218GP 68.10050.10Y 2nd = 68.10090.10B

L2403 IND-10UH-218GP 68.10050.10Y 2nd = 68.10090.10B

D2401 CH751H-40PT-GP 83.R0304.A8F 2nd = 83.R2004.B8F

D2402 CH751H-40PT-GP 83.R0304.A8F 2nd = 83.R2004.B8F

Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	a) VCCSREF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCCSREF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCCSREF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)

<Variant Name>

緯創資通 Wistron Corporation
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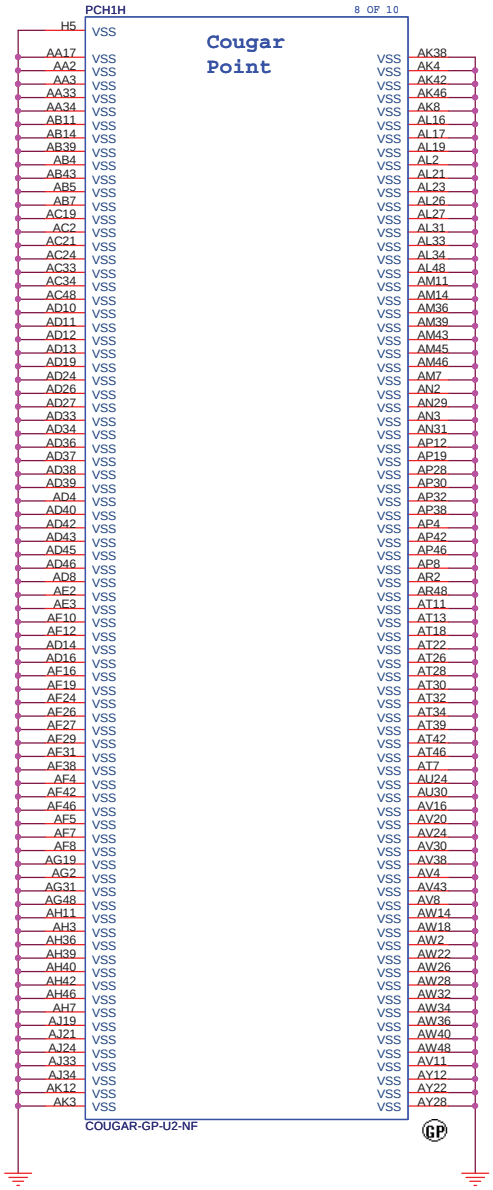
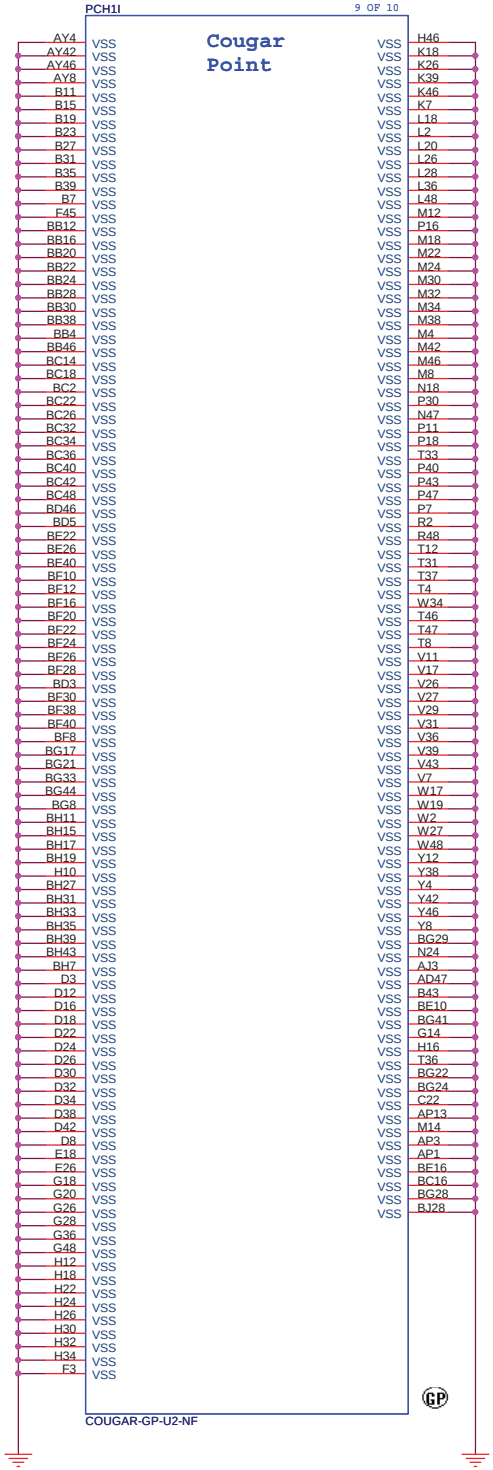
Title: PCH (POWER2)

Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 24 of 102

SSID = PCH





<Variant Name>

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Title: PCH (VSS)

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Blanking

<Variant Name>

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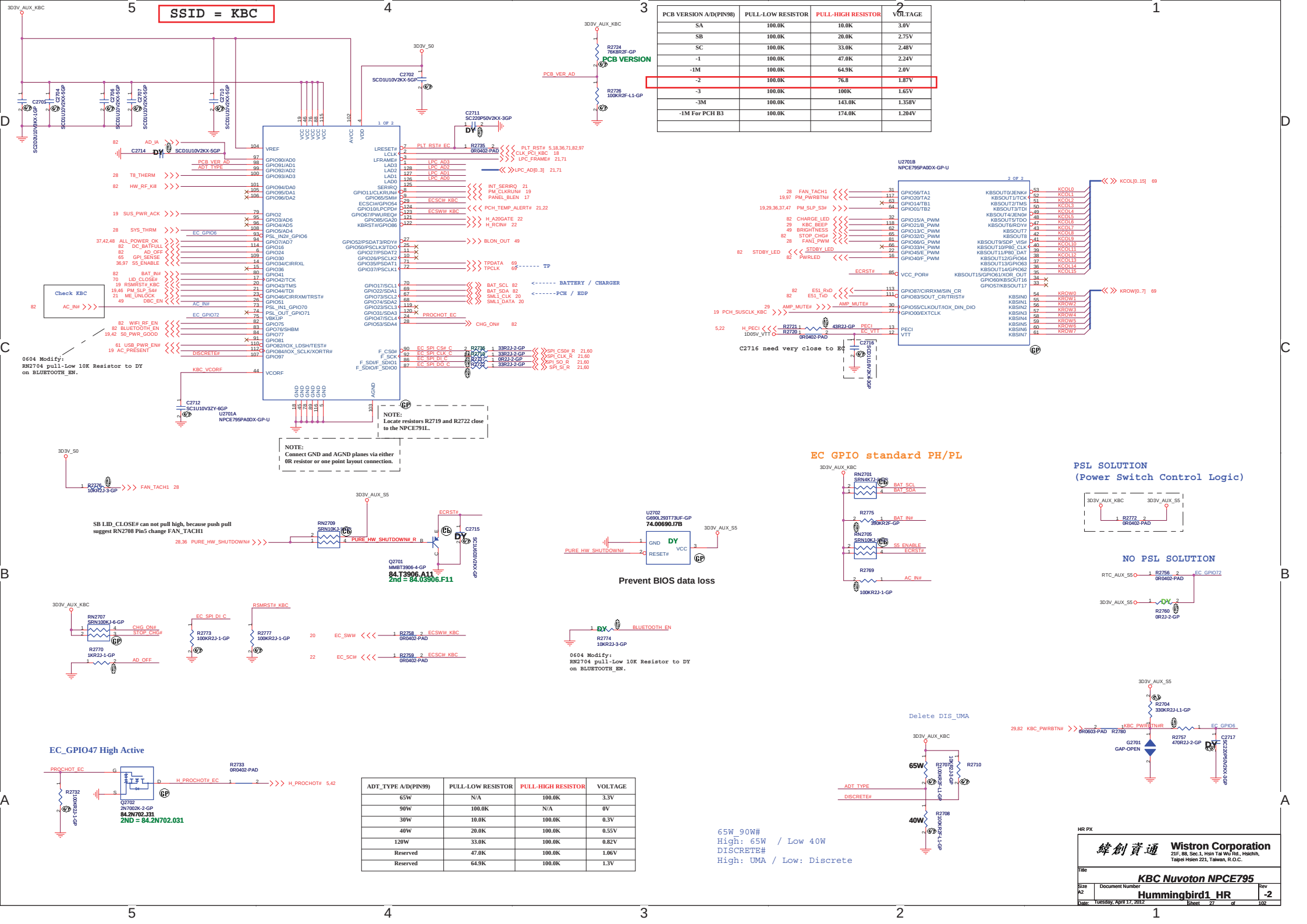
Title: *Clock(colay)*		
Size: A4	Document Number: **Hummingbird1_HR**	Rev: **-2**
Date: Tuesday, April 17, 2012	Sheet 26 of 102	

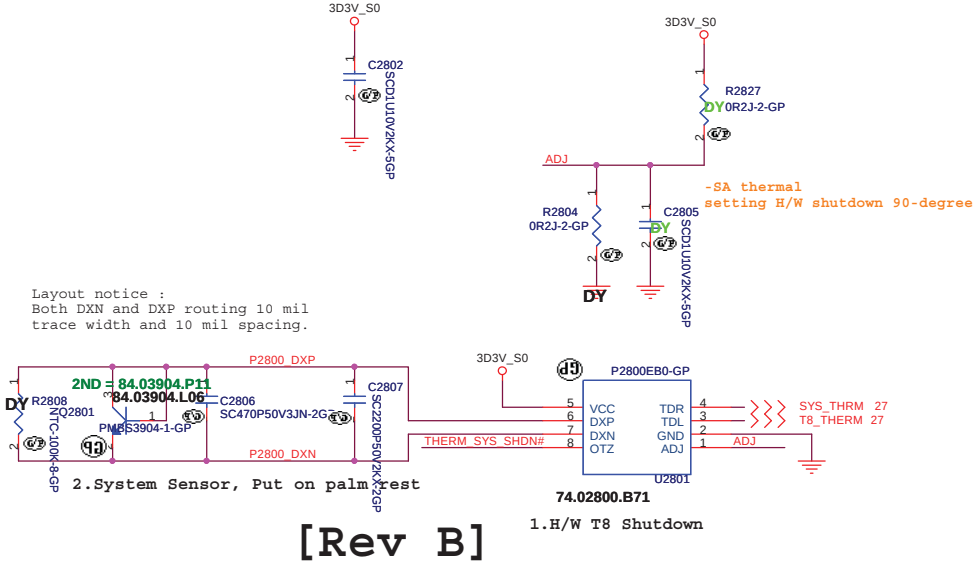


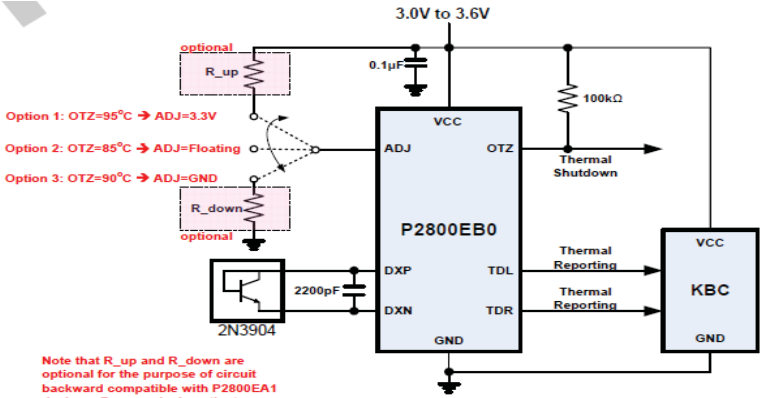
PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
-1M	100.0K	64.9K	2.0V
-2	100.0K	76.8	1.87V
-3	100.0K	100K	1.65V
-3M	100.0K	143.0K	1.358V
-1M For PCH B3	100.0K	174.0K	1.204V

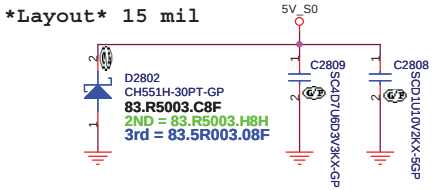
ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

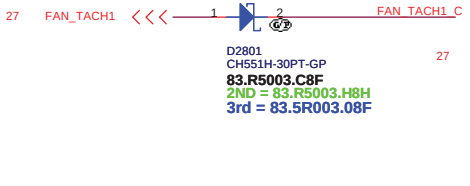
SSID = Thermal

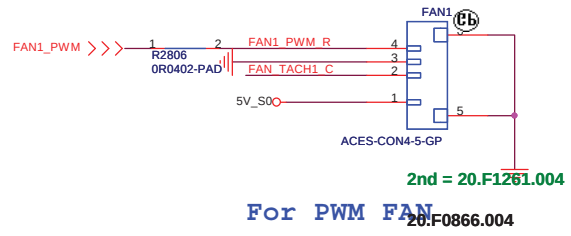
Thermal sensor P2800

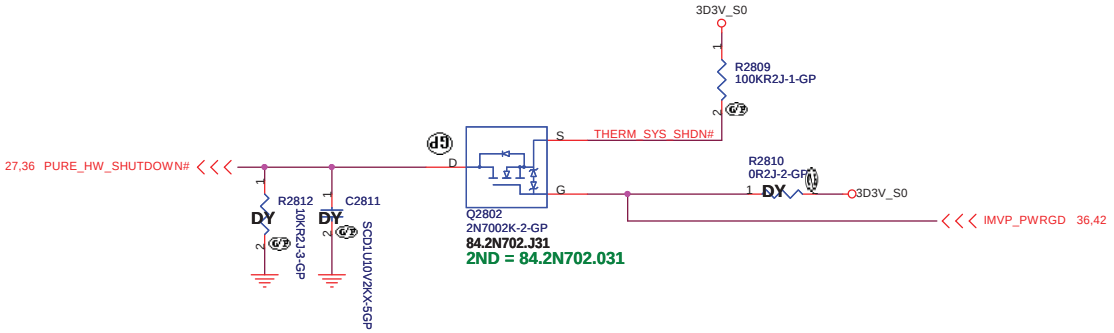












HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793

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A3	Hummingbird1 HR	-2

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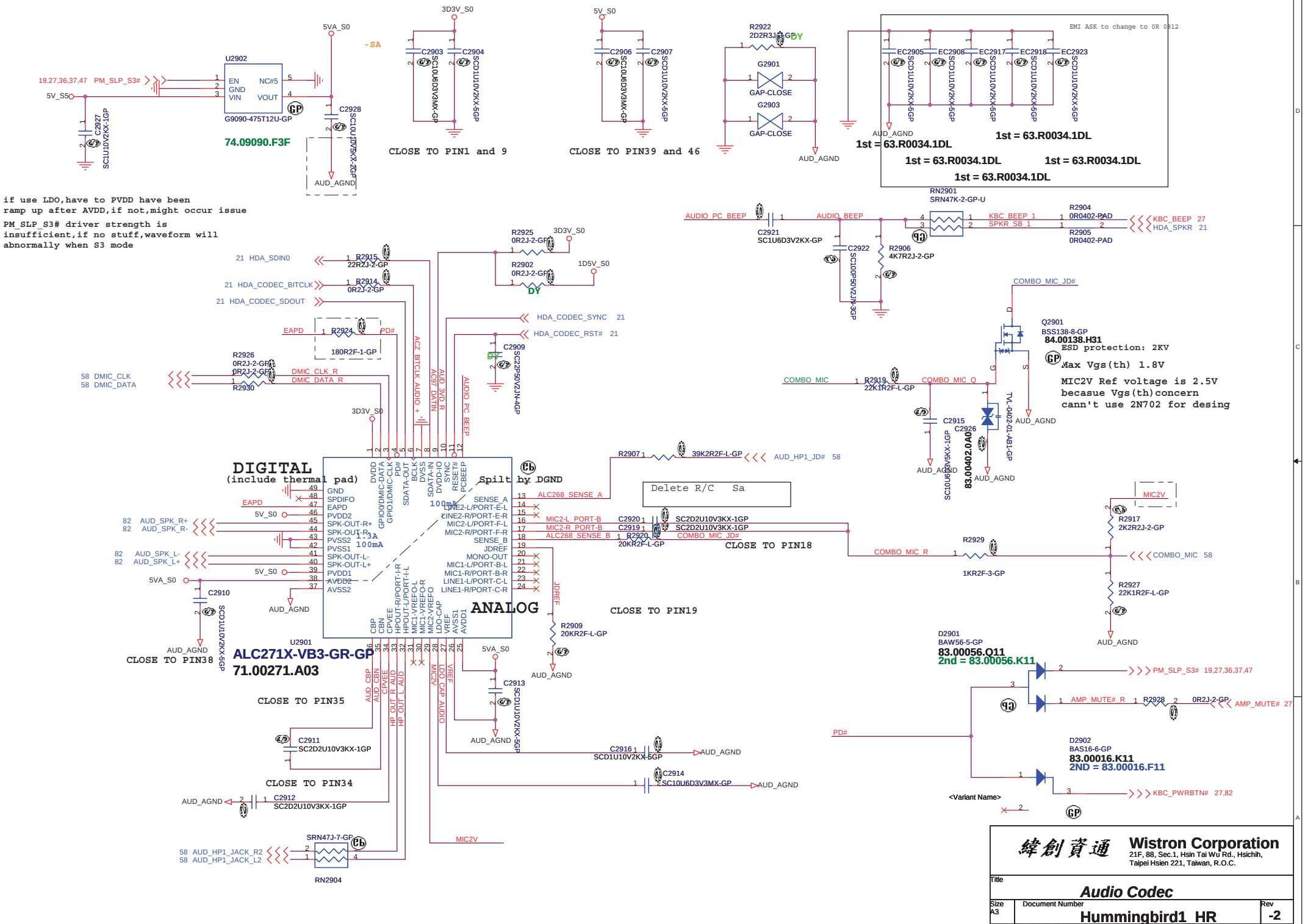
5VA_S0
-SA
U2902
19,27,36,37,47 PM_SLP_S3#
5V_S5
EN
GND
VIN
NC#5
VOUT
G9090-475T12U-GP
74.09090.F3F
C2927
SC1U10V2KX-1GP
C2928
SC10U10V5KX-2GP
AUD_AGND
3D3V_S0
C2903
C2904
SC10U6D3V3MX-GP
SCD1U10V2KX-5GP
CLOSE TO PIN1 and 9
5V_S0
C2906
C2907
CLOSE TO PIN39 and 46
R2922
2D2R3J-GP
DY
G2901
GAP-CLOSE
G2903
EMI ASK to change to 0R 0812
EC2905
EC2908
EC2917
EC2918
EC2923
1st = 63.R0034.1DL
if use LDO,have to PVDD have been
ramp up after AVDD,if not,might occur issue
PM_SLP_S3# driver strength is
insufficient,if no stuff,waveform will
abnormally when S3 mode
RN2901
SRN47K-2-GP-U
AUDIO_PC_BEEP
C2921
SC1U6D3V2KX-GP
AUDIO_BEEP
C2922
SC100P50V2JN-3GP
R2906
4K7R2J-2-GP
KBC_BEEP_1
SPKR_SB_1
R2904
0R0402-PAD
R2905
0R0402-PAD
KBC_BEEP 27
HDA_SPKR 21
21 HDA_SDIN0
21 HDA_CODEC_BITCLK
21 HDA_CODEC_SDOUT
R2915
22R2J-2-GP
R2914
0R2J-2-GP
R2925
0R2J-2-GP
R2902
0R2J-2-GP
1D5V_S0
HDA_CODEC_SYNC 21
HDA_CODEC_RST# 21
EAPD
R2924
180R2F-1-GP
PD#
C2909
SC22P50V2JN-4GP
R2926
0R2J-2-GP
R2930
0R2J-2-GP
58 DMIC_CLK
58 DMIC_DATA
DMIC_CLK_R
DMIC_DATA_R
AC97_BIT_CLK
AUDIO_PC_BEEP
COMBO_MIC_JD#
Q2901
BSS138-8-GP
84.00138.H31
ESD protection: 2KV
Max Vgs(th) 1.8V
MIC2V Ref voltage is 2.5V
becasue Vgs(th)concern
cann't use 2N702 for desing
COMBO_MIC
R2919
22K1R2F-L-GP
COMBO_MIC_Q
C2915
C2926
SC100P50V5KX-1GP
TVL-0402-01-AB1-GP
83.00402.0A0
DIGITAL
(include thermal pad)
Spilt by DGND
GND
SPDIFO
EAPD
PVDD2
SPK-OUT-R+
SPK-OUT-R-
PVSS2
PVSS1
SPK-OUT-L-
SPK-OUT-L+
PVDD1
AVDD2
AVSS2
82 AUD_SPK_R+
82 AUD_SPK_R-
82 AUD_SPK_L-
82 AUD_SPK_L+
1.3A
100mA
C2910
SCD1U10V2KX-5GP
AUD_AGND
CLOSE TO PIN38
U2901
ALC271X-VB3-GR-GP
71.00271.A03
ANALOG
SENSE_A
LINE2-L/PORT-E-L
LINE2-R/PORT-E-R
MIC2-L/PORT-F-L
MIC2-R/PORT-F-R
SENSE_B
JDREF
MONO-OUT
MIC1-L/PORT-B-L
MIC1-R/PORT-B-R
LINE1-L/PORT-C-L
LINE1-R/PORT-C-R
ALC268_SENSE_A
ALC268_SENSE_B
MIC2-L_PORT-B
MIC2-R_PORT-B
R2907
39K2R2F-L-GP
AUD_HP1_JD# 58
Delete R/C Sa
C2920
C2919
C2921
SC2D2U10V3KX-1GP
R2920
20KR2F-L-GP
COMBO_MIC_JD#
CLOSE TO PIN18
CLOSE TO PIN19
R2909
20KR2F-L-GP
5VA_S0
C2913
SCD1U10V2KX-5GP
C2911
SC2D2U10V3KX-1GP
CLOSE TO PIN35
C2912
SC2D2U10V3KX-1GP
CLOSE TO PIN34
C2916
SCD1U10V2KX-5GP
C2914
SC10U6D3V3MX-GP
MIC2V
SRN47J-7-GP
58 AUD_HP1_JACK_R2
58 AUD_HP1_JACK_L2
RN2904
COMBO_MIC_R
R2929
1KR2F-3-GP
R2917
2K2R2J-2-GP
R2927
22K1R2F-L-GP
COMBO_MIC 58
D2901
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
PM_SLP_S3# 19,27,36,37,47
AMP_MUTE# R
R2928
0R2J-2-GP
AMP_MUTE# 27
PD#
D2902
BAS16-6-GP
83.00016.K11
2ND = 83.00016.F11
KBC_PWRBTN# 27,82
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio Codec
Size A3
Document Number
Hummingbird1 HR
Rev -2
Date: Tuesday, April 17, 2012
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AUDIO OP AMPLIFIER

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio AMP***		
Size: A4	Document Number: **Hummingbird1_HR**	Rev: **-2**
Date: Tuesday, April 17, 2012	Sheet 30 of 102	

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AR8158		
Size: A3	Document Number: Hummingbird1_HR	Rev: -2
Date: Tuesday, April 17, 2012	Sheet 31 of 102	

Card reader move to small board

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5159 (CARD READER)***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 32 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 33 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

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HR PX

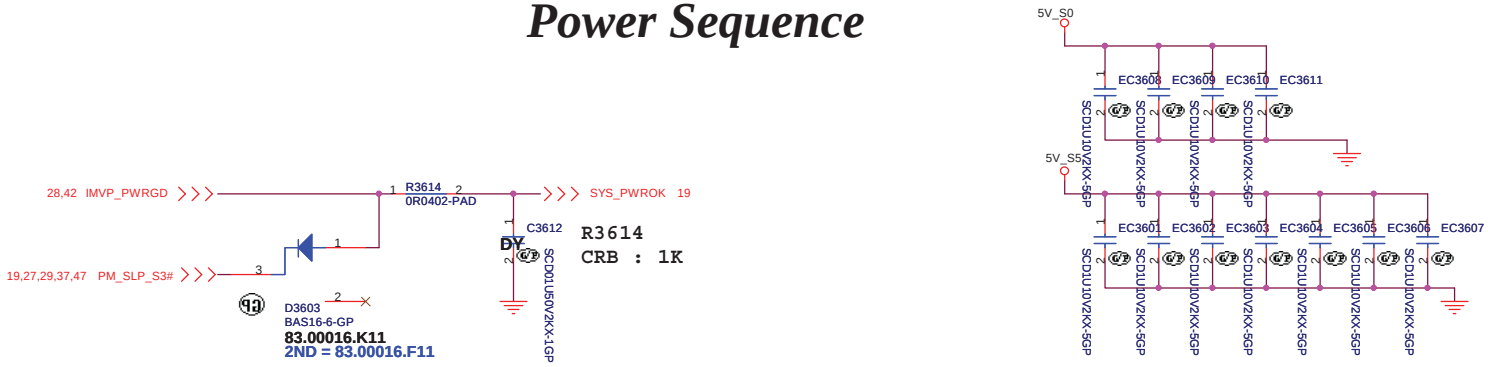
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

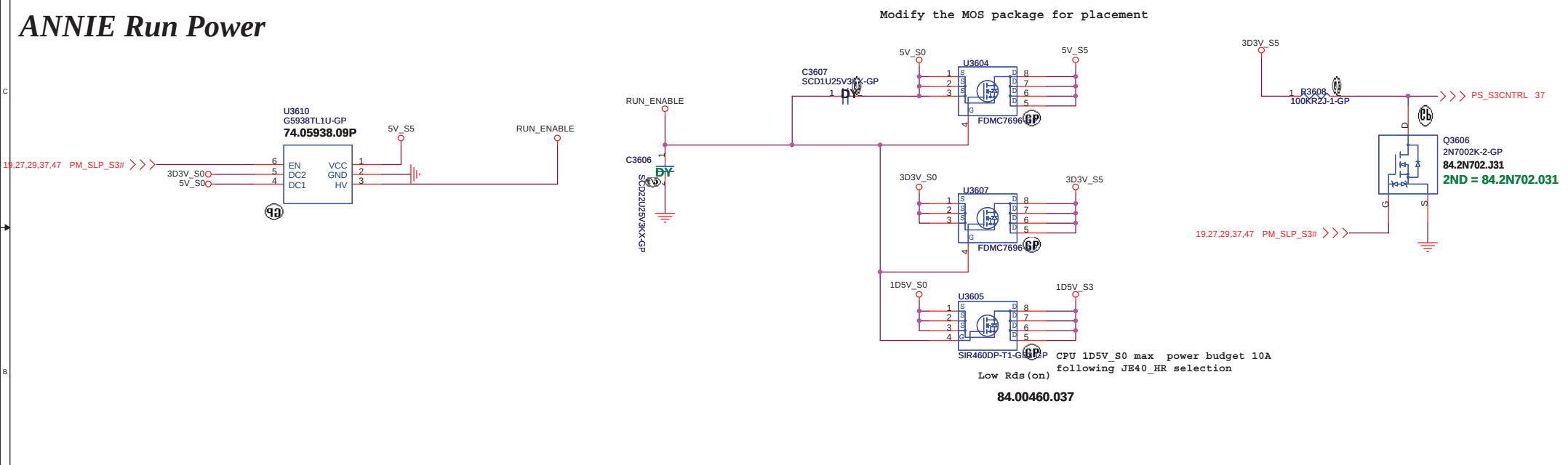
Size	Document Number	Rev
A3	**Hummingbird1_HR**	**-2**

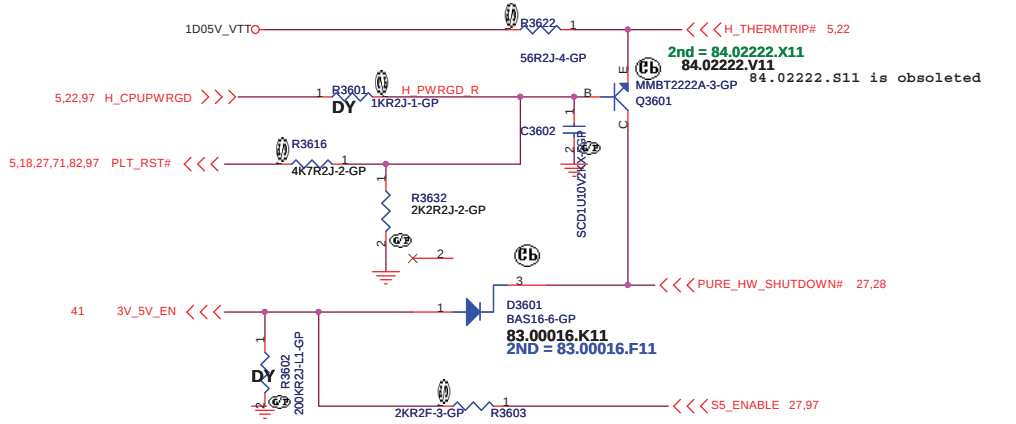
Date: Tuesday, April 17, 2012 Sheet 35 of 102

Power Sequence



ANNIE Run Power



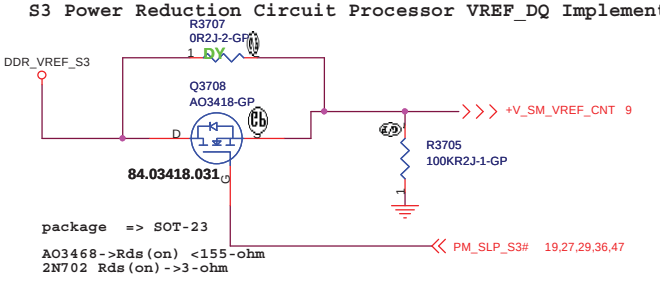


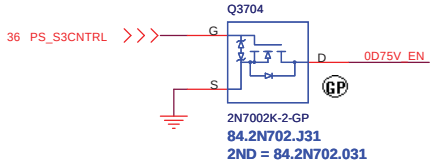
HR PX

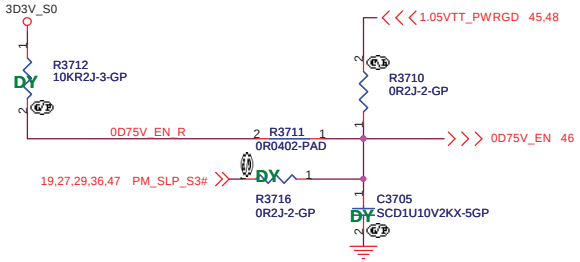
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**		
Size: A3	Document Number: **Hummingbird1 HR**	Rev: -2
Date: Tuesday, April 17, 2012	Sheet 36 of 102	

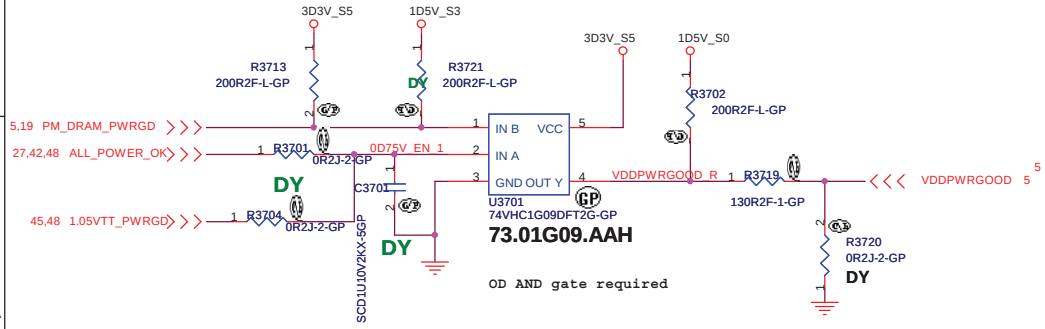
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



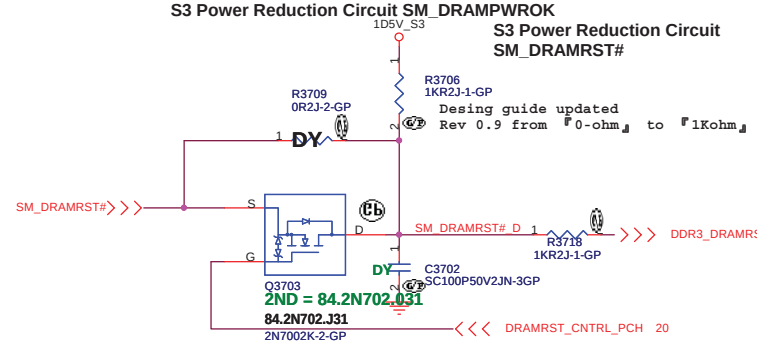


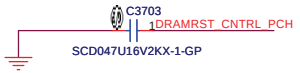


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

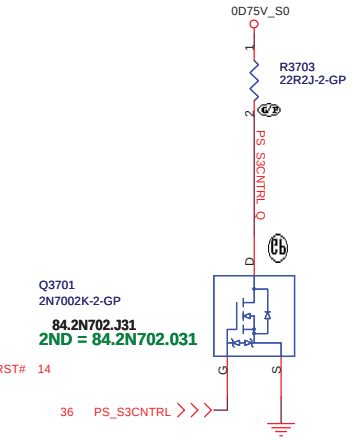


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK
S3 Power Reduction Circuit
SM_DRAMRST#





Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time
over VDDQ * 0.55± 200mV and the edge must be monotonic

HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

Size	Document Number	Rev
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Move to small board

HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DCIN JACK***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

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Move to small board

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BATT CONN***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 39 of 102

Move to small board

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

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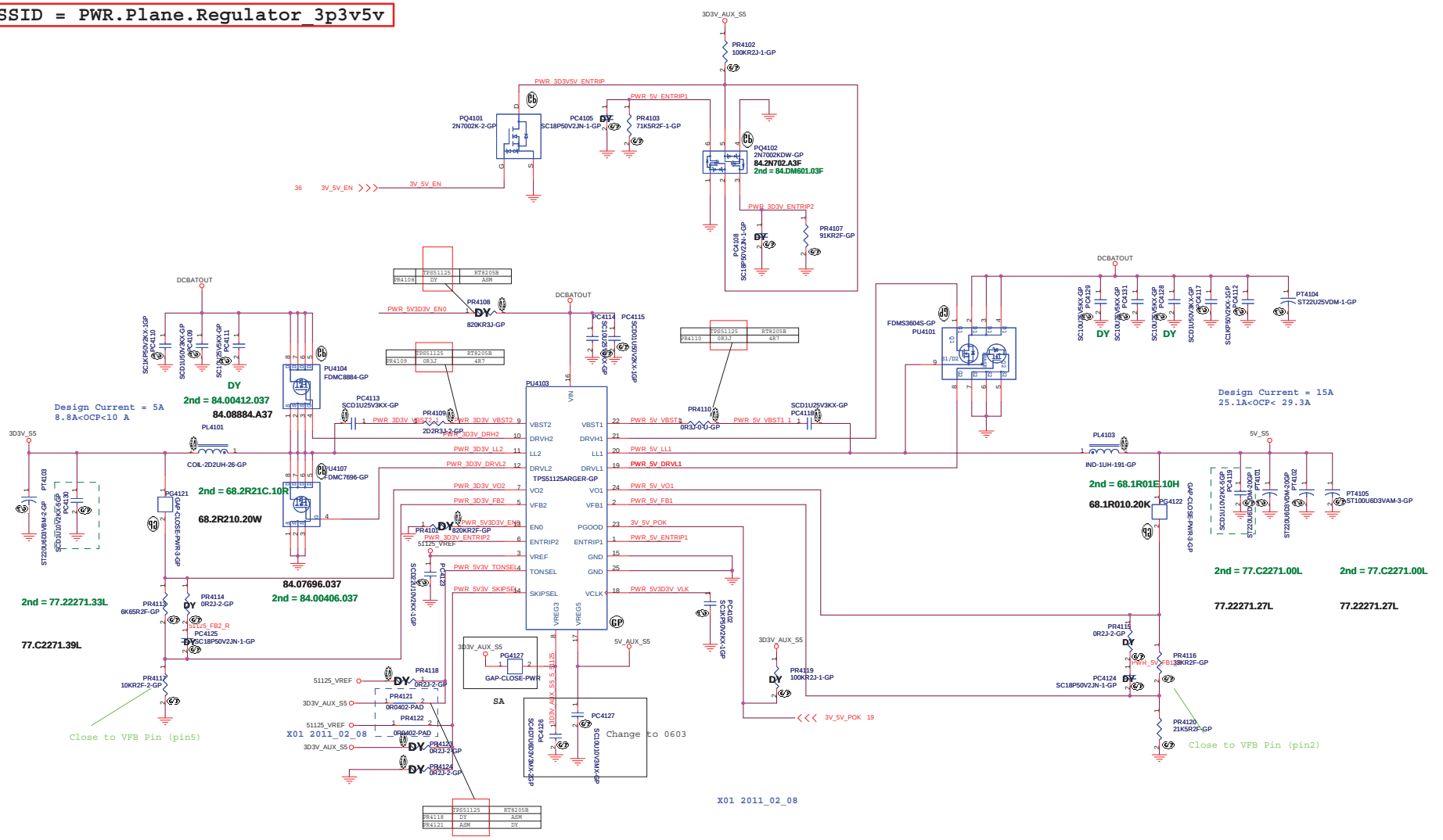
SSID = PWR.Plane.Regulator_3p3v5v

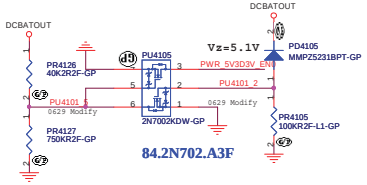


I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =10Arms 68.2R210.20B
O/P cap: ST220U6D3VDM-20GP 25mOhm / 77.22271.27L
H/S: FDMC8884-GP / 22mOhm/30mOhm@4.5Vgs / 84.08884.A37
L/S: FDMC7692-GP / 9.5mOhm/11.5mOhm@4.5Vgs / 84.07692.A37

I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.50UH PCMC104T-1R5 Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: ST220U6D3VDM-20GP 25mOhm / 77.22271.27L
H/S: SIR172DP-T1-GE3-GP / 10.3mOhm/12.4mOhm@4.5Vgs / 84.00172.037
L/S: SIR460DP-T1-GE3-GP / 4.9mOhm/6.1mOhm@4.5Vgs / 84.00460.037

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit



TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

<Variant Name>

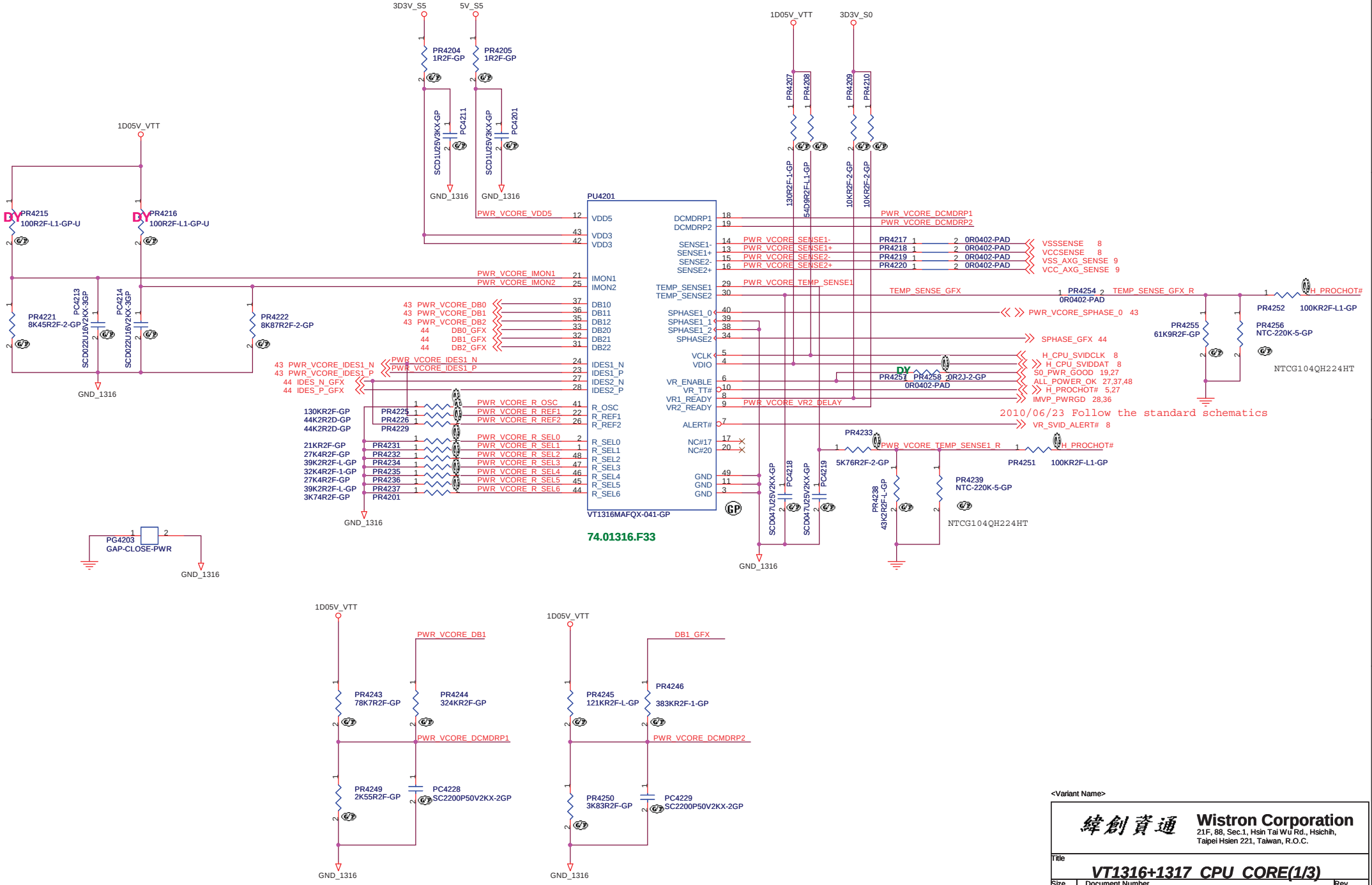
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51125A_5V/3D3V

Size: Custom | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 41 of 102

SSID = CPU.Regulator



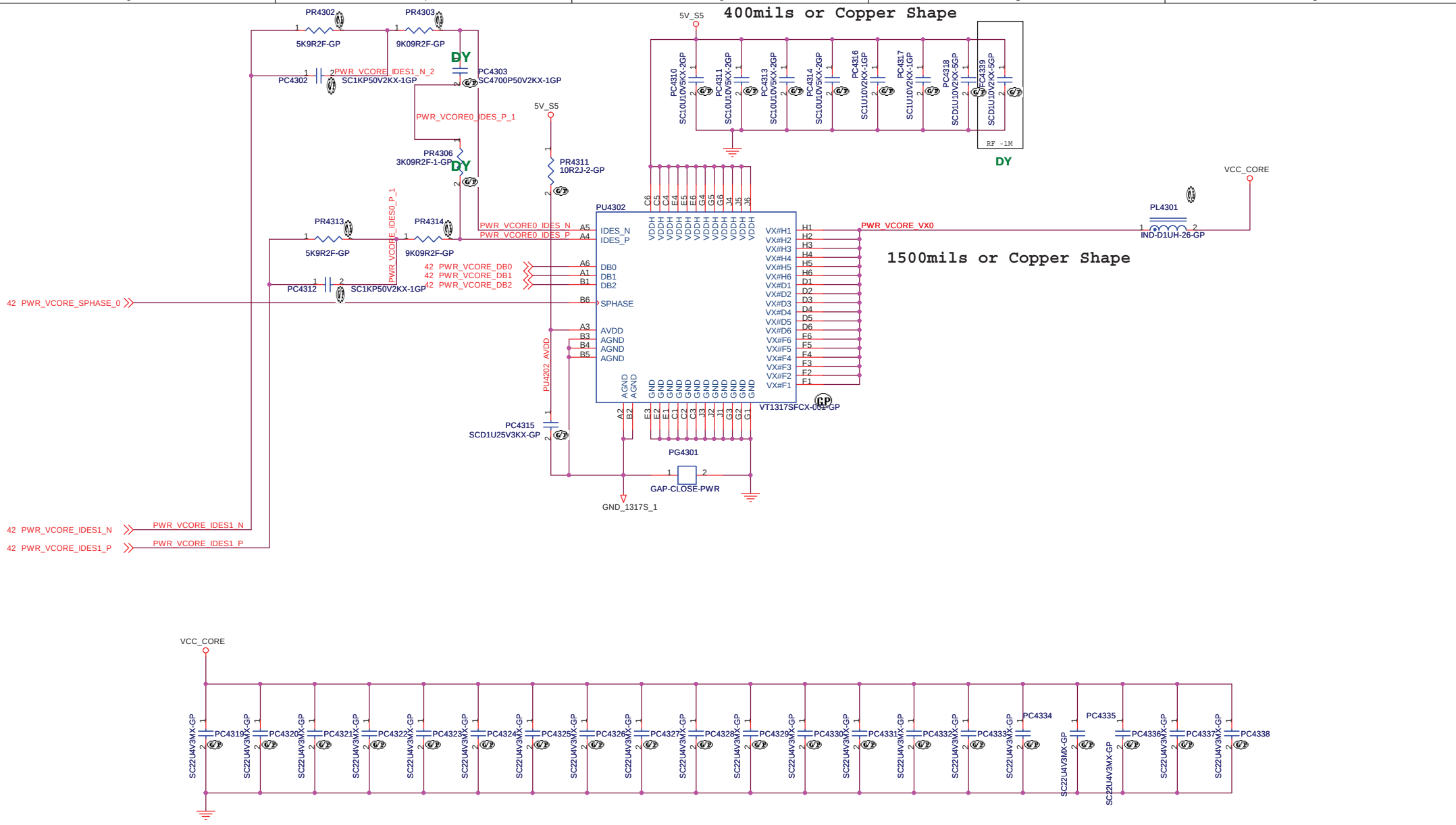
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1317 CPU CORE(1/3)

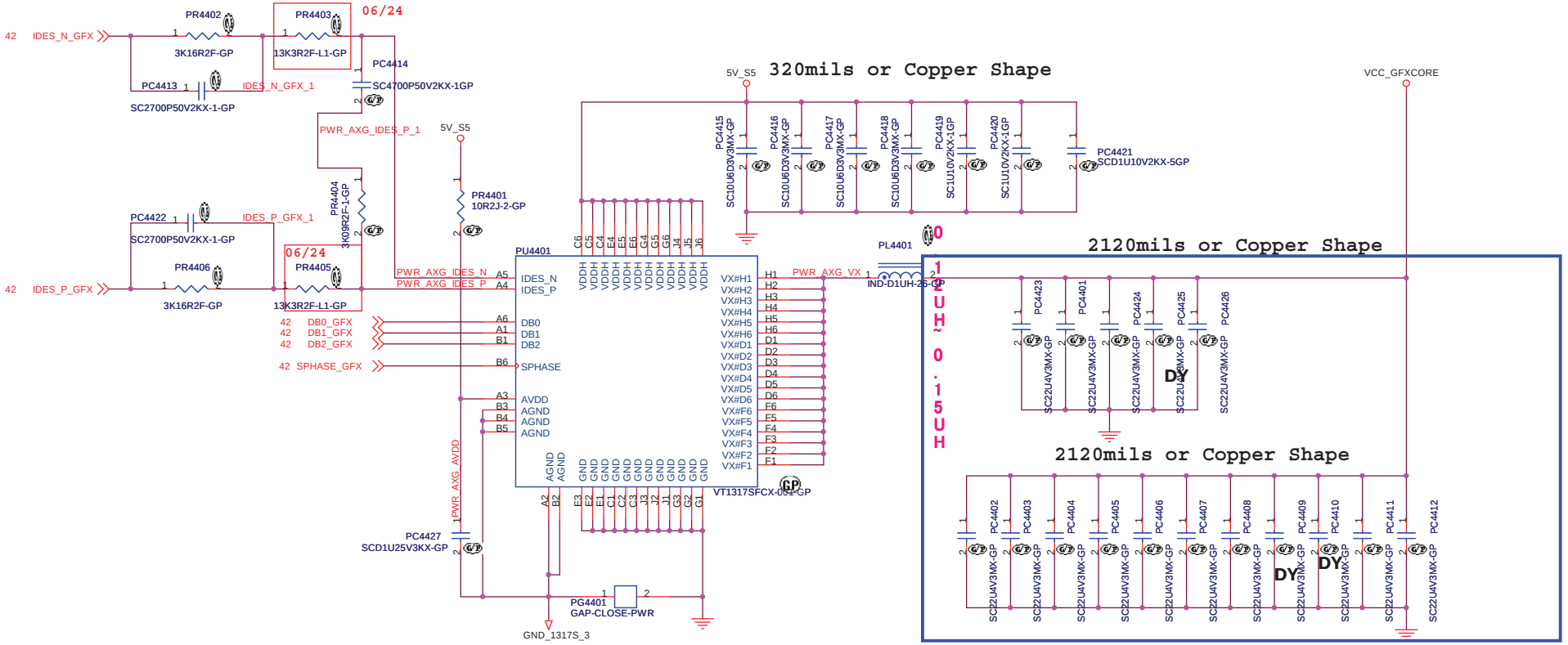
Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 42 of 102



<variant_name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*VT1316+1317 CPU CORE(2/3)*
Size A3	Document Number: Hummingbird1 HR
Rev	-2
Date: Tuesday, April 17, 2012	Sheet 43 of 102



Change to 0603_4V

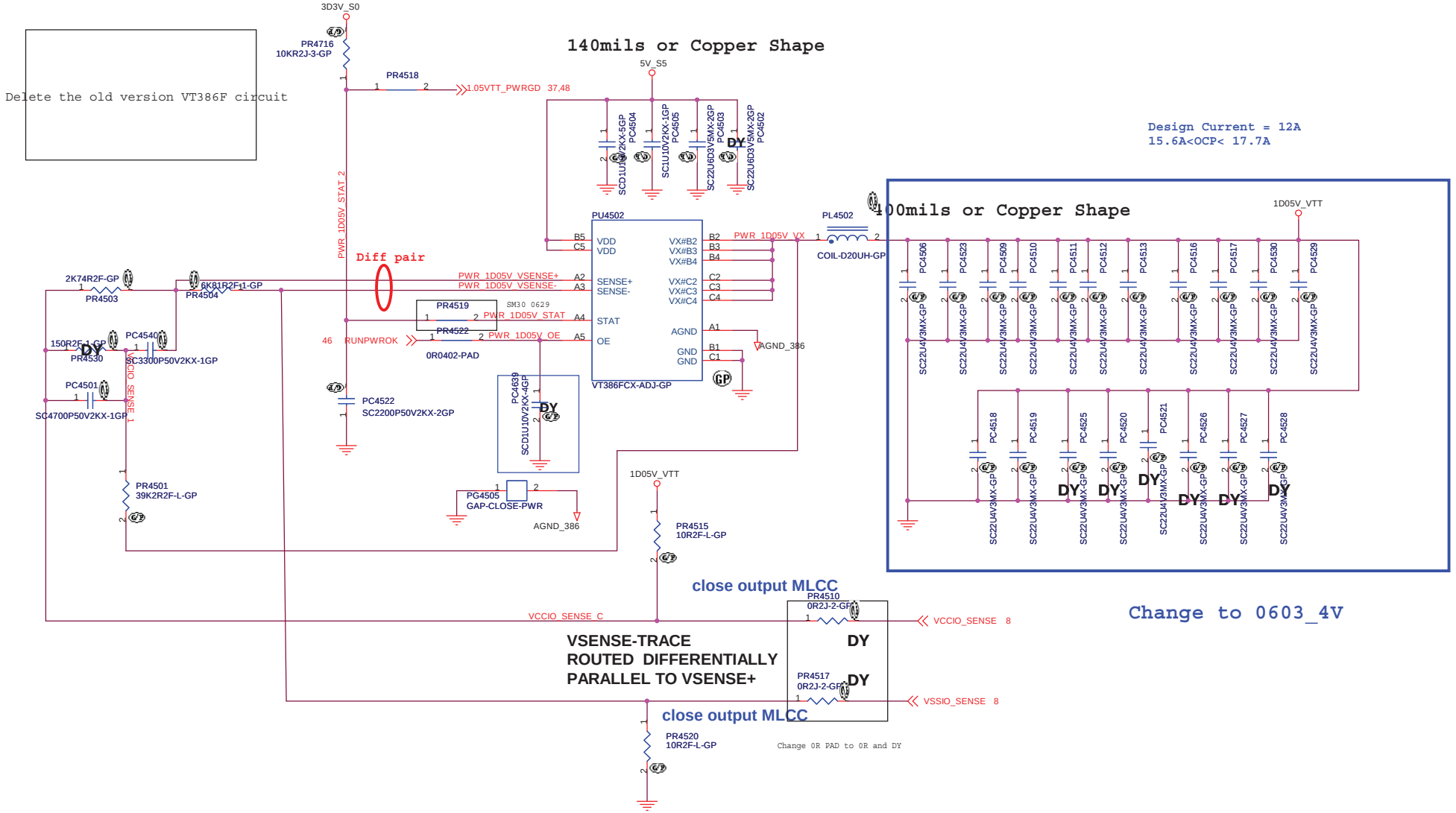
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VT1316+1317 CPU CORE(3/3)***

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 44 of 102



<Variant Name>

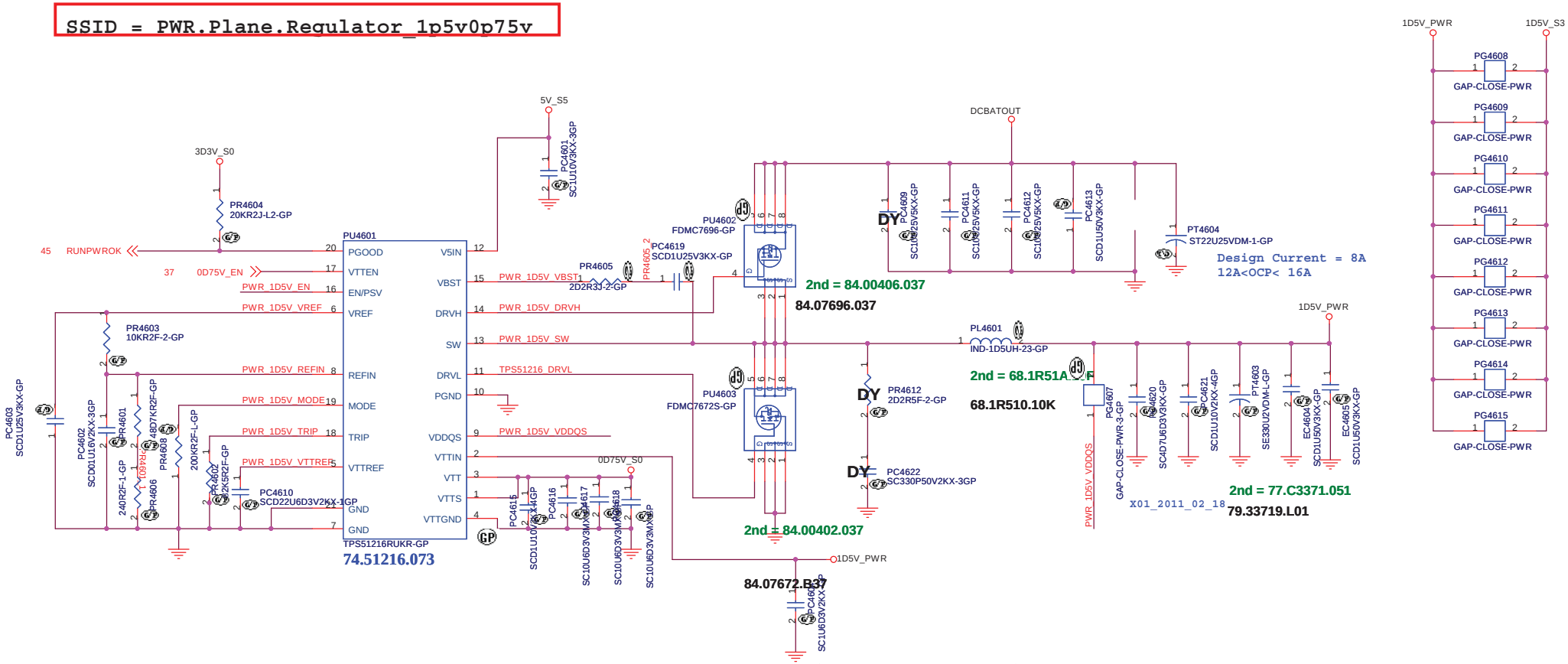
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT386 +1.05V VTT

Size: A3 | Document Number: Hummingbird1 HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 45 of 102

SSID = PWR.Plane.Regulator_1p5v0p75v

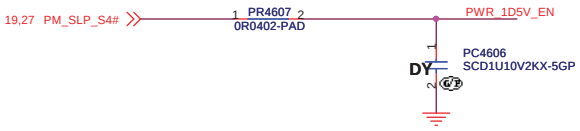


I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: IND-1D5UH-23-GP 14mohm/15mohm Isat =18Arms 68.1R510.10K
O/P cap: SE330U2VDM-L-GP 9mOhm / 79.33719.L01
H/S: SIS412DN-T1-GE3-GP / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S: SI7716ADN-T1-GE3-GP / 13.5mOhm/16.5mOhm@4.5Vgs / 84.07716.037

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR5003	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	



<Variant Name>

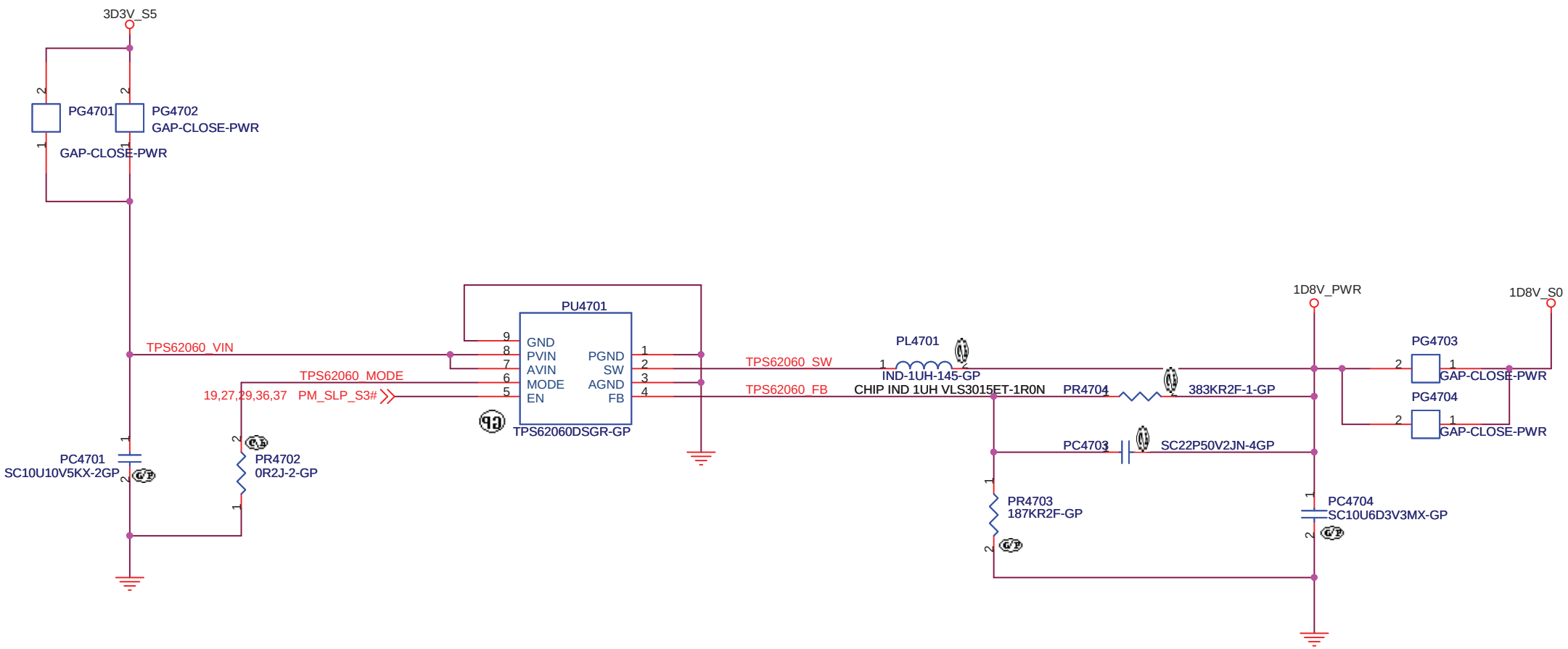
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116 +1.5V SUS

Size	Document Number	Rev
A3	Hummingbird1 HR	-2

Date: Tuesday, April 17, 2012 Sheet 46 of 102

SSID = PWR.Plane.Regulator_1p8v

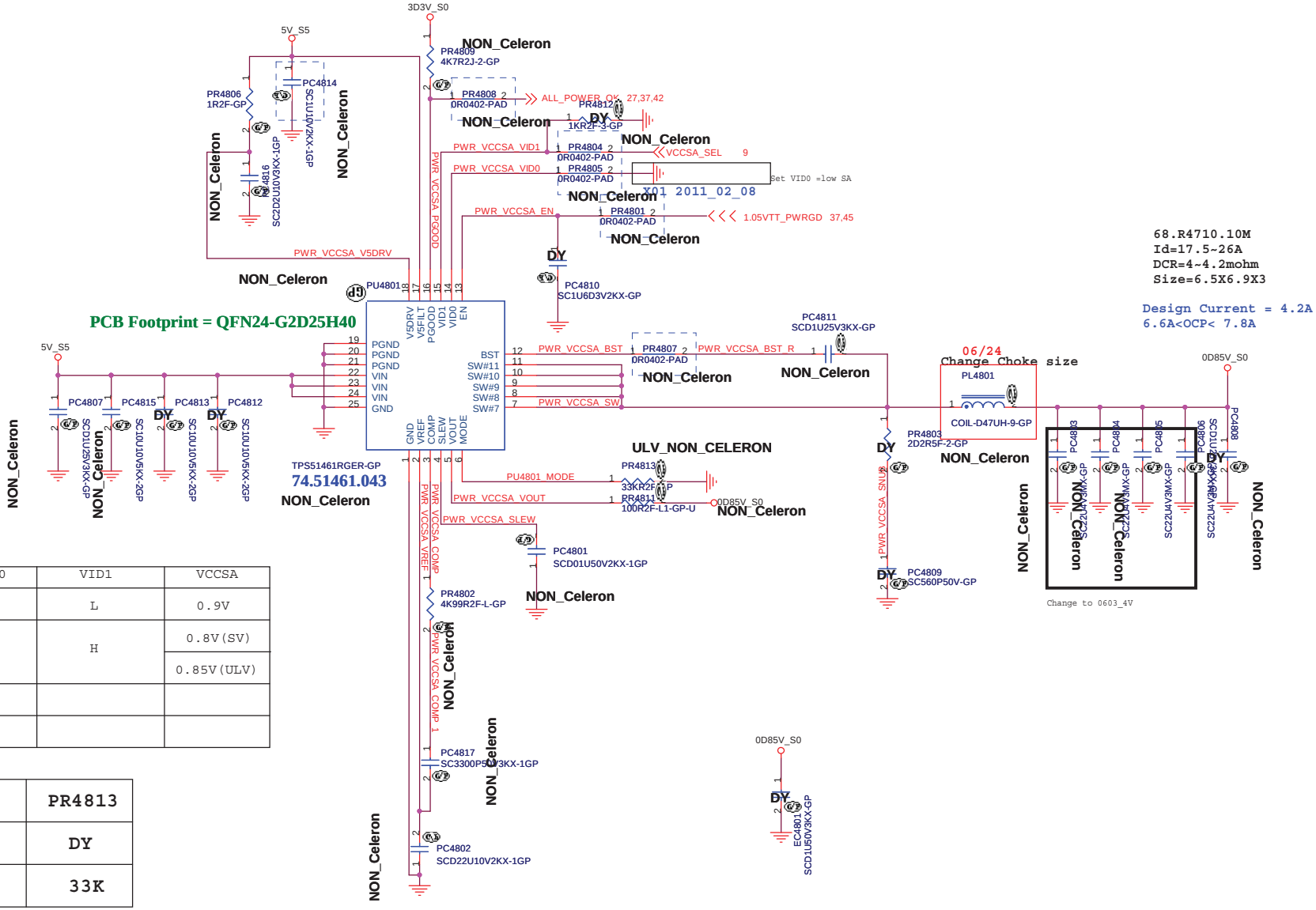


<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***DC CONVERTER_1D8V***	
Size A4	Document Number **Hummingbird1_HR**	Rev **-2**
Date: Tuesday, April 17, 2012	Sheet 47 of 102	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V(SV)
		0.85V(ULV)

TYPE	PR4813
SV	DY
ULV	33K

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51461_VCCSA

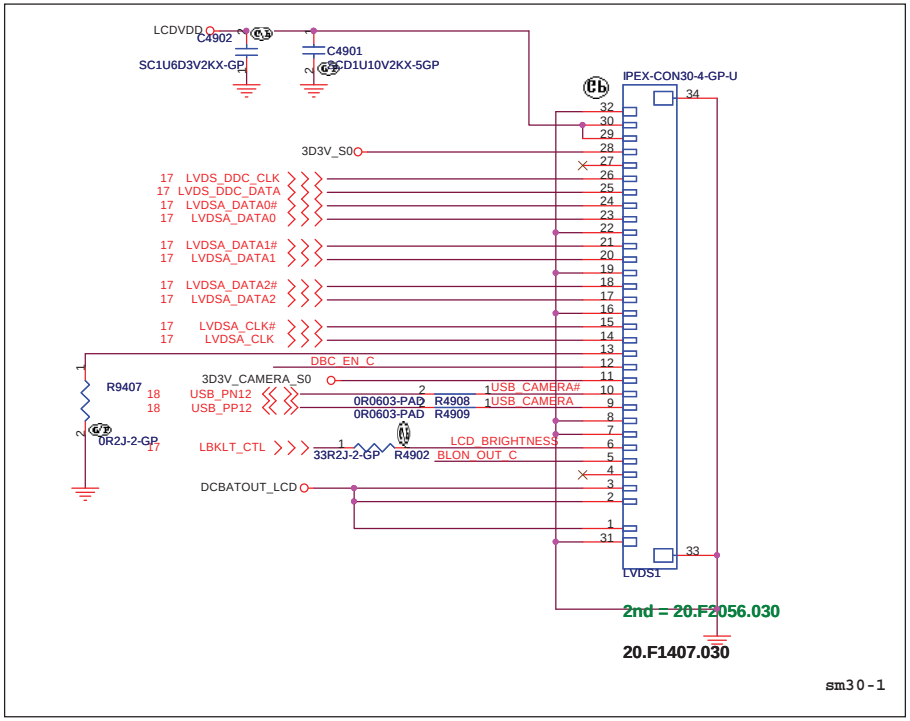
Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 48 of 102

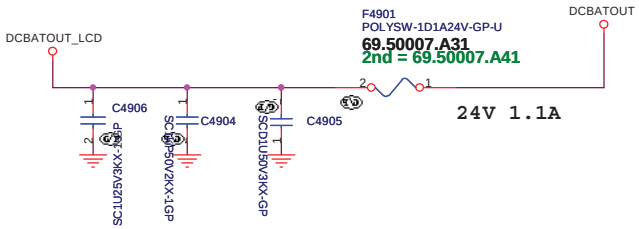
SSID = VIDEO

Reverse the pin define becasue of cable issue

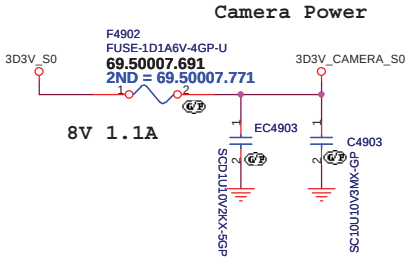
LVDS CONNECTOR



INVERTER POWER

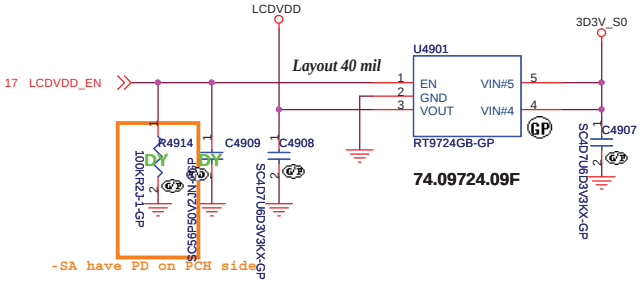


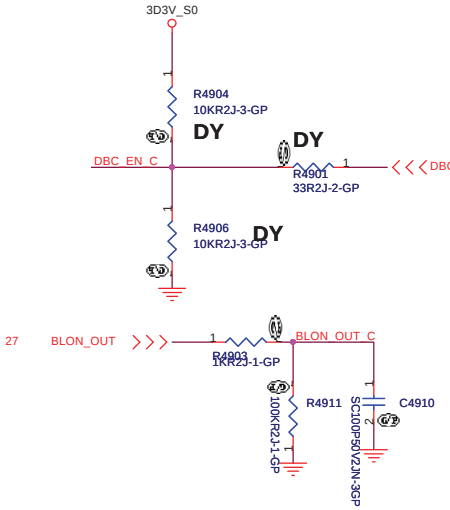
Camera Power



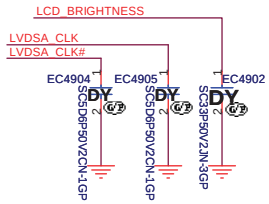
SSID = VIDEO

LCD POWER for ANNIE





For EMI request
Close to LVDS connector



-SA

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
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Pull High 5V Design on CRT Board

CRT DDCDATA & DDCCLK level shift

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 50 of 102

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

17 HDMI_CLK_R#
17 HDMI_CLK_R
17 HDMI_DATA0_R#
17 HDMI_DATA0_R
17 HDMI_DATA1_R#
17 HDMI_DATA1_R
17 HDMI_DATA2_R#
17 HDMI_DATA2_R

Close to HDMI Connector

HDMI_CLK_R#
HDMI_CLK_R
HDMI_DATA0_R#
HDMI_DATA0_R
HDMI_DATA1_R#
HDMI_DATA1_R
HDMI_DATA2_R#
HDMI_DATA2_R

RN5114
SRN499F-GP
RN5115
SRN499F-GP

Intel desging suggestion Stuff 680-ohm,
CRB board stuff 618-ohm
TM said that following JE40_HR stuff 499-ohm

HDMI_PLL_GND

Q5105
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

5V_S0

Close to Level Shift

3D3V_S0

17 PCH_HDMI_CLK
17 PCH_HDMI_DATA

Q5104
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F

5V_S0

RN5101
SRN2K2J-1-GP

DDC_CLK_HDMI
DDC_DATA_HDMI

HDMI1
SKT-HDMI25-GP-GP

HDMI_DATA2_R
HDMI_DATA2_R#
HDMI_DATA1_R
HDMI_DATA1_R#
HDMI_DATA0_R
HDMI_DATA0_R#
HDMI_CLK_R
HDMI_CLK_R#
DDC_CLK_HDMI
DDC_DATA_HDMI

2nd = 22.10296.311
3rd = 22.10296.501
22.10296.271

5V_S0
F5101
FUSE-1D1A6V-4GP-U
69.50007.691
87 1 : 1A
2nd = 69.50007.771

FC5101
SCD1U10V2KX-5GP
DY

HPD_HDMI_CON

3D3V_S0
84.03904.L06
2ND = 84.03904.P11
Q5102
PMBS3904-1-GP
HDMI_HPD_B
R5111
150KR2J-L1-GP
R5110
200KR2J-L1-GP
DY

HDMI_DET
R5112
10KR2J-3-GP
R5113
10KR2J-2-GP
HDMI_PCH_DET 17

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector
Size: A3
Document Number: Hummingbird1 HR
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LED BACKLIGHT CONVERTER POWER

HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*

Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 52 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

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(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

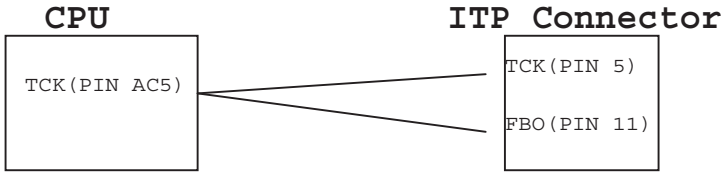
Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP		
Size: A4	Document Number: Hummingbird1_HR	Rev: -2
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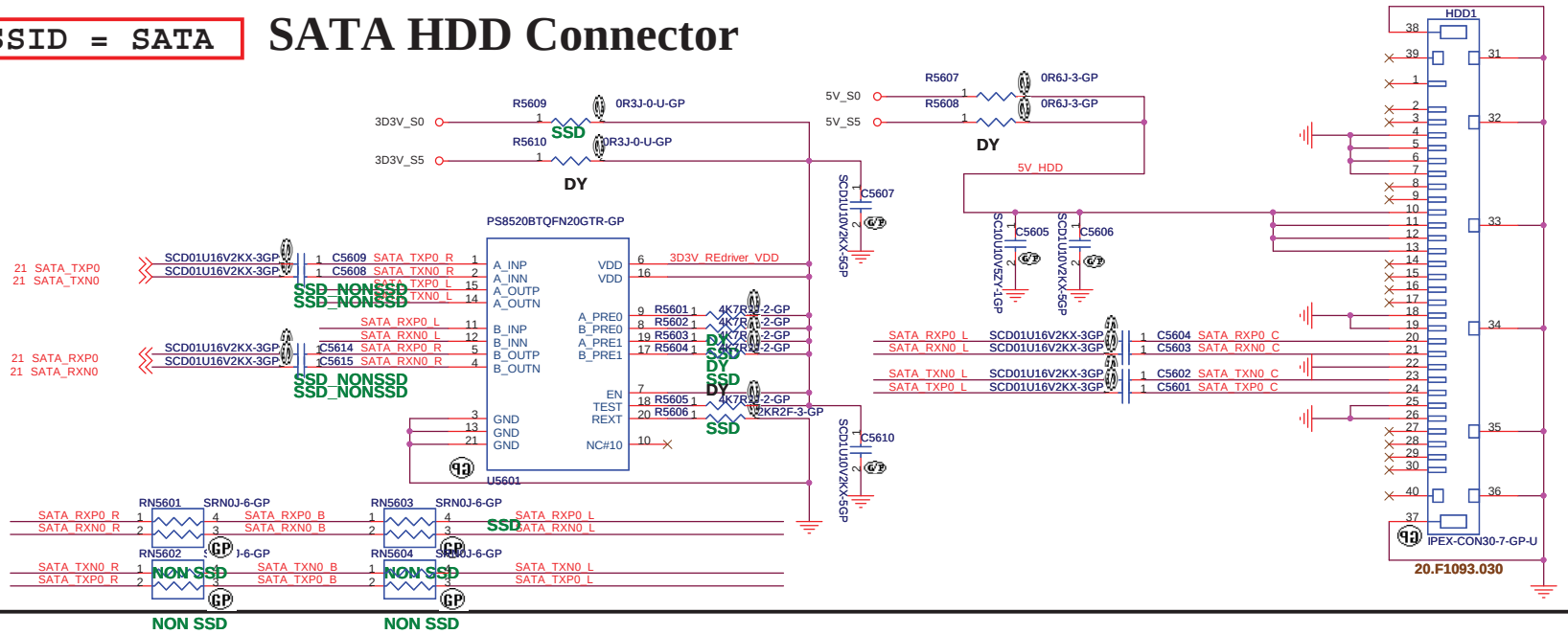
SSID = SATA

SATA HDD Connector



ODD Connector

Without ODD

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 56 of 102

ESATA Power

USB CHARGER

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: E-SATA/USB CHARGER

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

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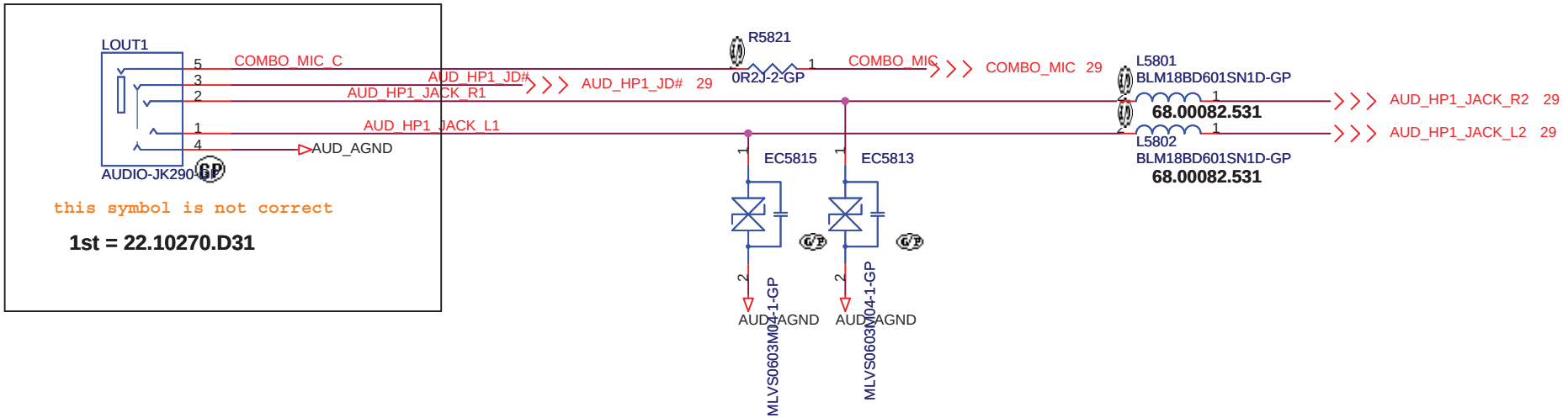
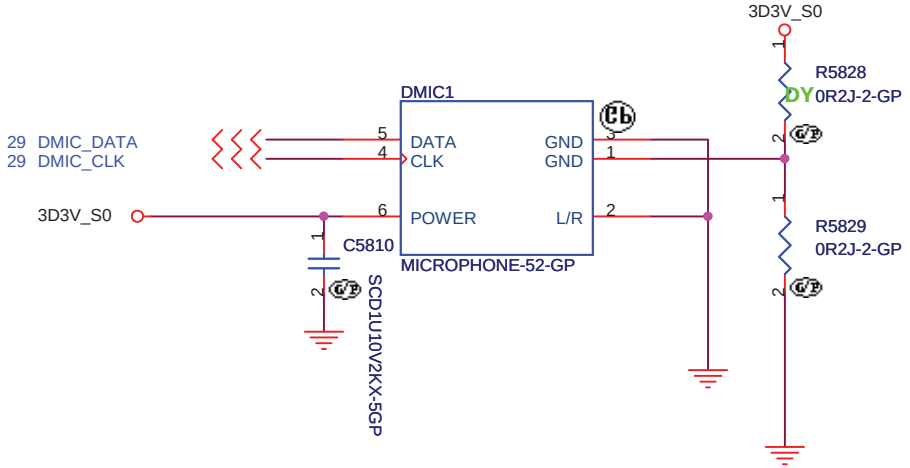
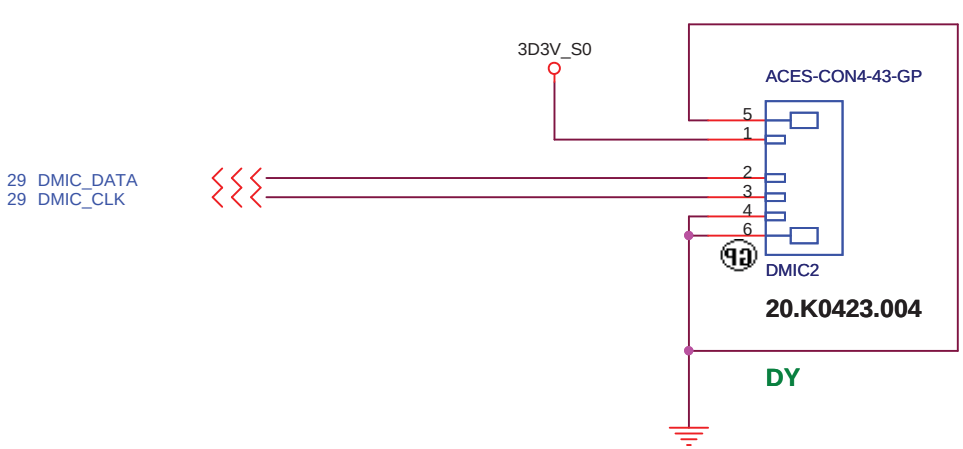
SSID = AUDIO







<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio Jack***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 58 of 102

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

Without LAN

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

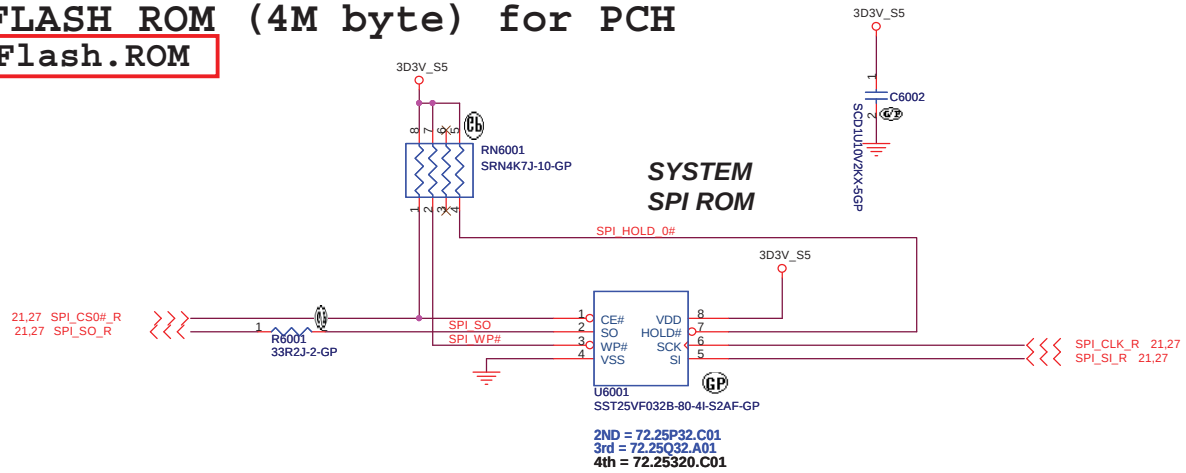
Title: LAN CONNECTOR

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

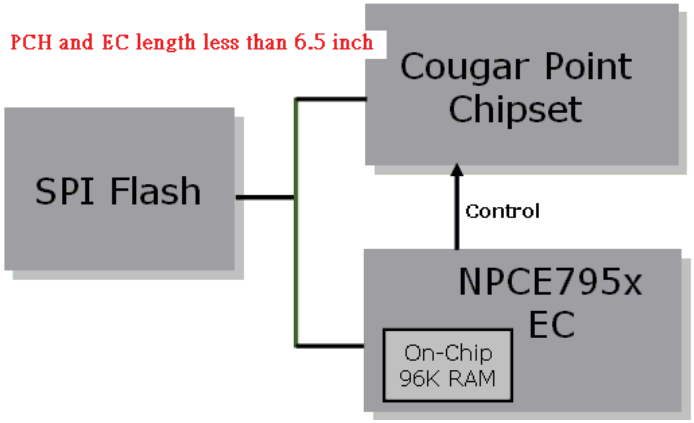
Date: Tuesday, April 17, 2012 Sheet 59 of 102

SPI FLASH ROM (4M byte) for PCH

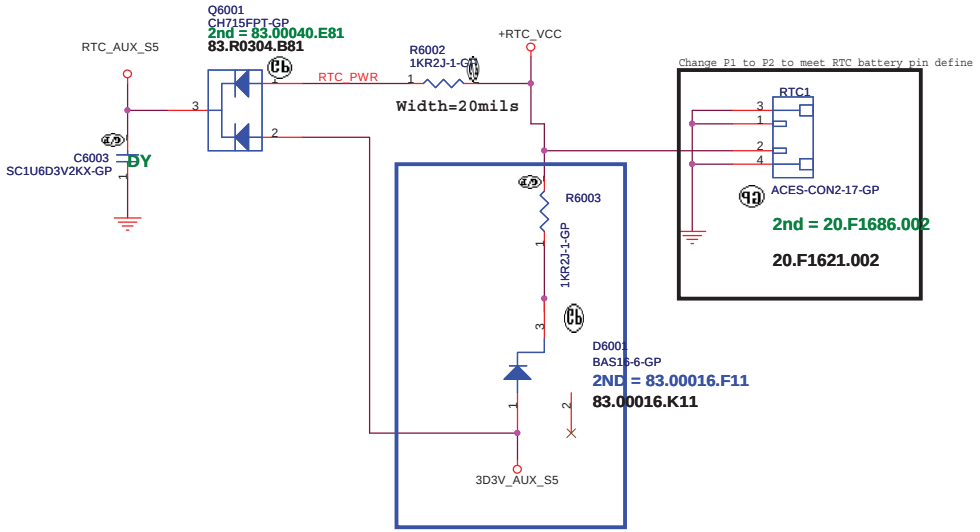
SSID = Flash.ROM



SPI ROM Equal length need to less than 500mil
SPI ROM Equal length need to less than 500mil



SSID = RBATT



RTC battery charger sircuit

HR PX

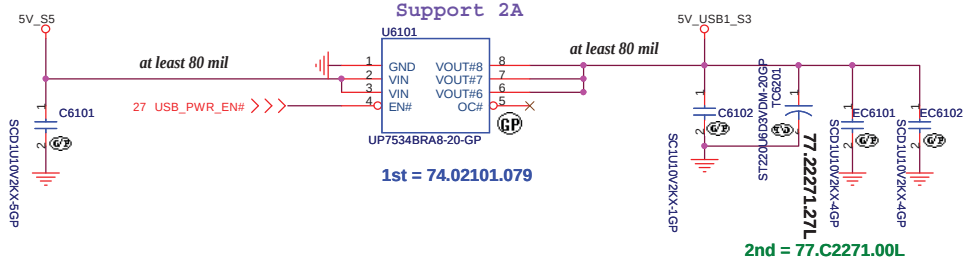
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Flash/RTC	
Size A3	Document Number Hummingbird1 HR	Rev -2
Date: Tuesday, April 17, 2012	Sheet 60 of 102	

SSID = USB

IO Board USB Power

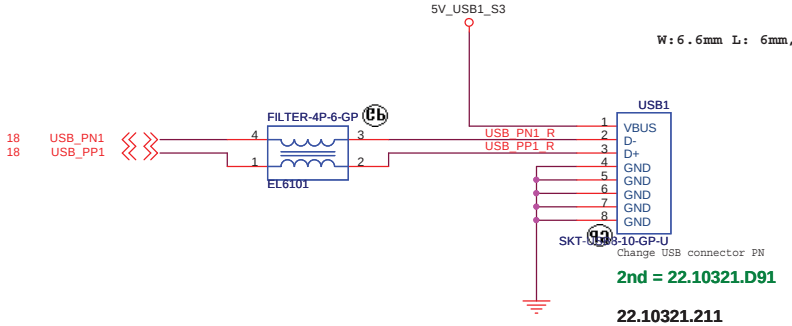
Change Main source
Support 2A



1st = 74.02101.079

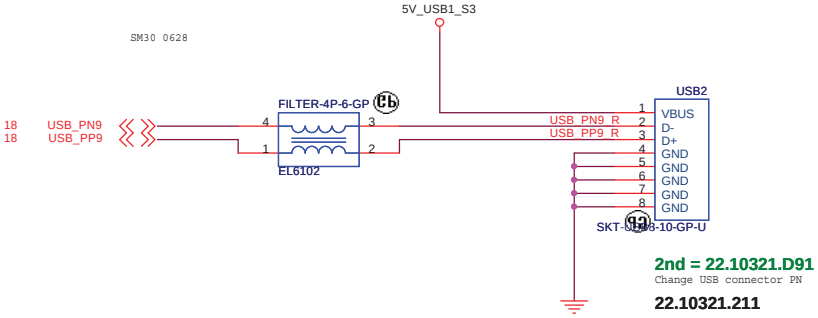
77.22271.27L

2nd = 77.C2271.00L



2nd = 22.10321.D91

22.10321.211



2nd = 22.10321.D91

Change USB connector PN

22.10321.211

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

Size: A3 | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 61 of 102

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB 3.0 Port*

Size	Document Number	Rev
A3	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 62 of 102

SSID = User.Interface

Bluetooth Module conn.

Without BT

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Bluetooth*

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 63 of 102

Finger printer

JE40 delete FP function

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

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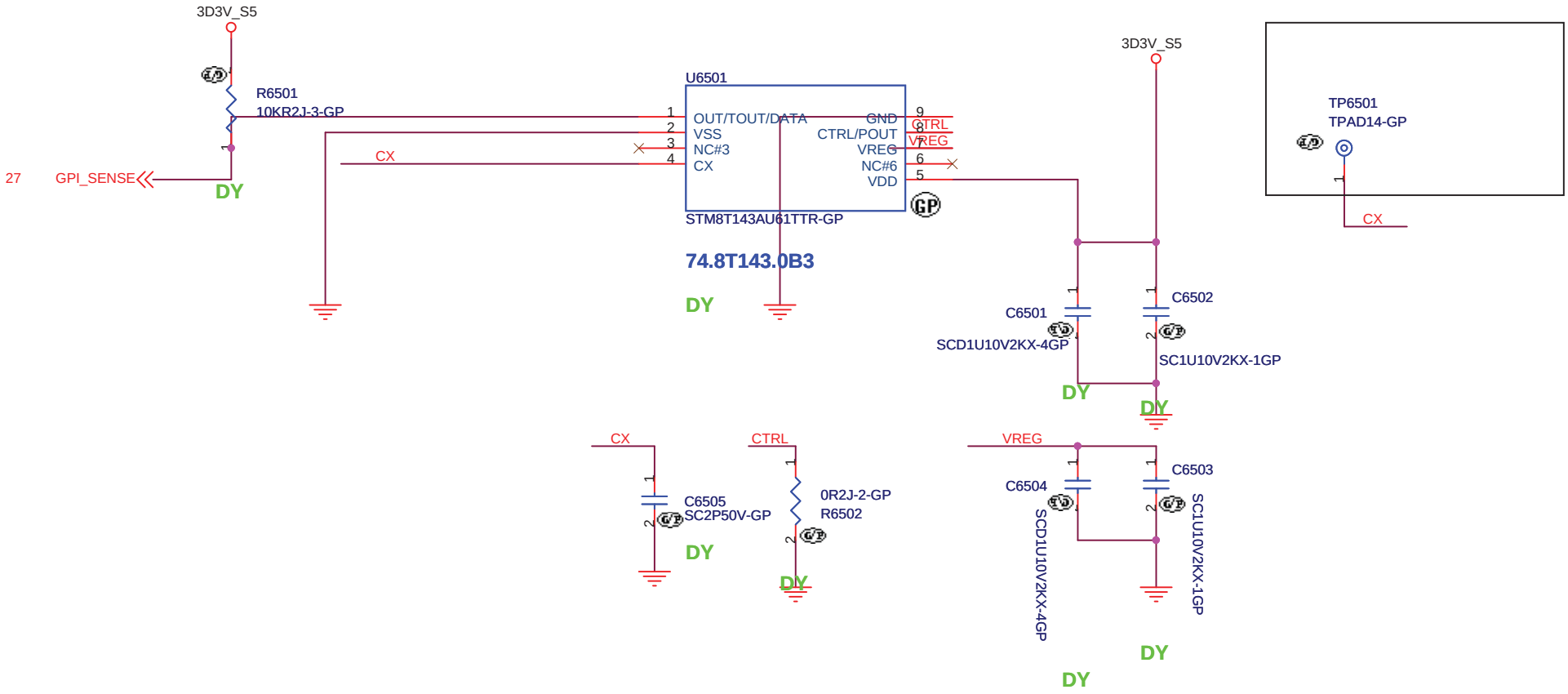
SSID = Wireless

C Sensor



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *MINICARD(WLAN)/ITP CONN*

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 65 of 102

SSID = Wireless

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***WWAN Connector***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 66 of 102

Blanking

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***M-SATA***		
Size: A4	Document Number: **Hummingbird1_HR**	Rev: **-2**
Date: Tuesday, April 17, 2012	Sheet 67 of 102	

SSID = User.Interface

Move to power board

for factory test

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

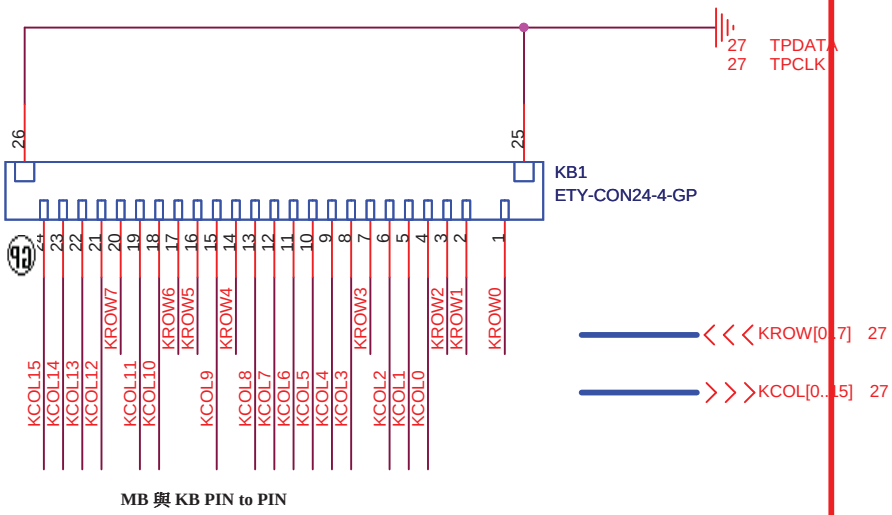
Title: ***LED Bard/Power Button***

Size	Document Number	Rev
Custom	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 68 of 102

SSID = KBC

Internal KeyBoard Connector

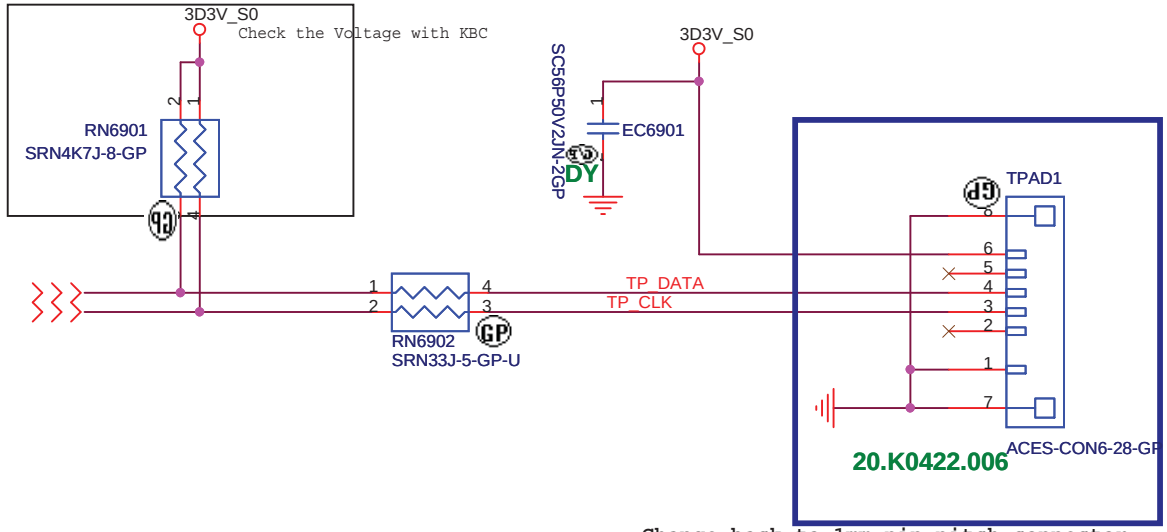


MB 與 KB PIN to PIN

Change KB from 下接觸 to 上接觸

KB Pin define need to check again

TOUCH PAD



Change back to 1mm pin pitch connector

Switch the pin order SA

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad		
Size: A4	Document Number: Hummingbird1_HR	Rev: -2
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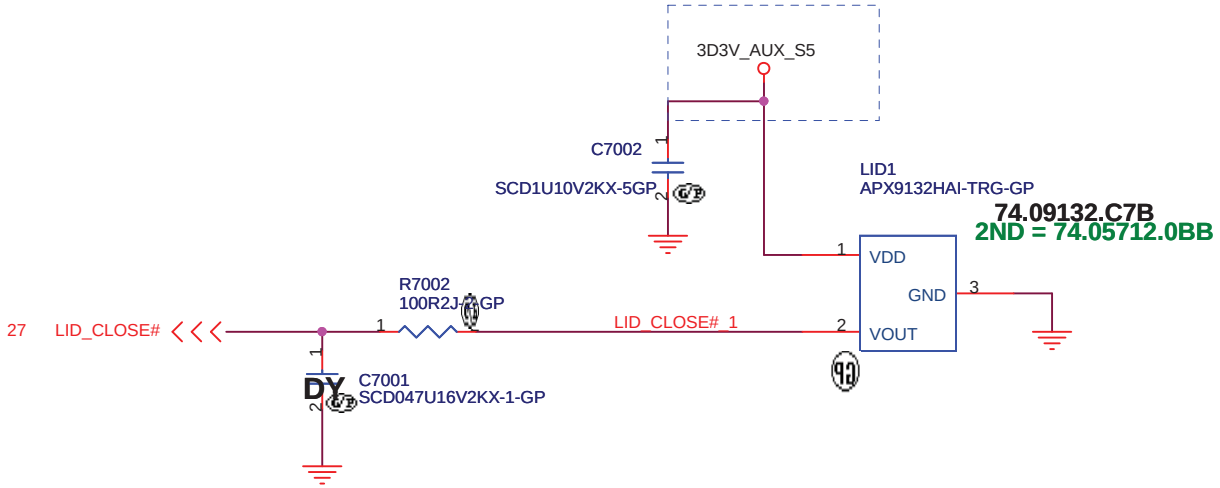
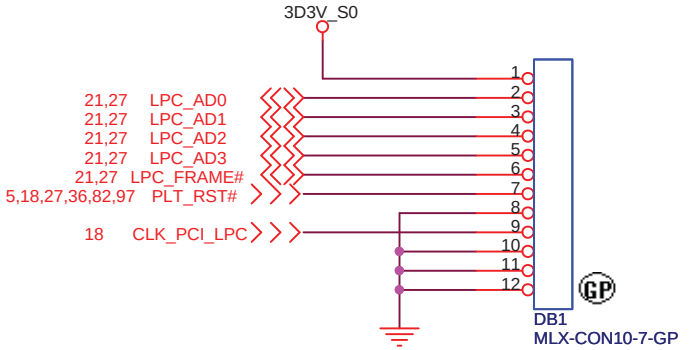
Change from 3D3V_AUX_KBC to 3D3V_AUX_S5



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***		
Size: A4	Document Number: **Hummingbird1_HR**	Rev: **-2**
Date: Tuesday, April 17, 2012	Sheet 70 of 102	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 71 of 102

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	**Hummingbird1_HR**	**-2**

Date: Tuesday, April 17, 2012 Sheet 72 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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SD/XD/MS Card Reader

Card reader move to small board

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size	Document Number	Rev
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SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card

Size: A3 | Document Number: Hummingbird1 HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 75 of 102

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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A4	Hummingbird1_HR	-2

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A4	Document Number: **Hummingbird1_HR**	Rev: **-2**
Date: Tuesday, April 17, 2012	Sheet 77 of 102	

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

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SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Delete G Sensor Function

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Free Fall Sensor*		
Size: A4	Document Number: Hummingbird1_HR	Rev: -2
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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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<Variant Name>

緯創資通 **Wistron Corporation**
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Title
Reserved

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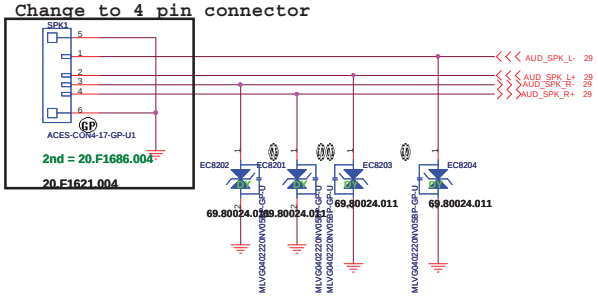
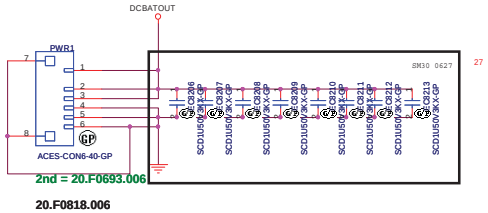
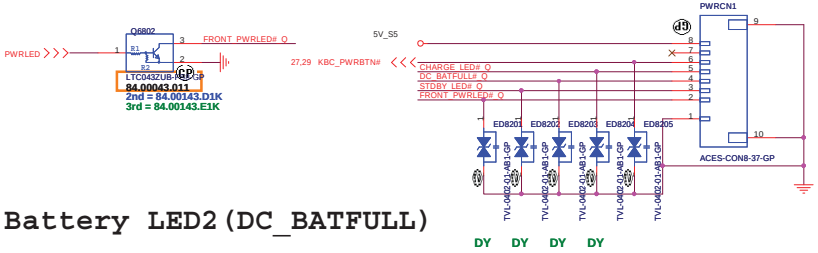
Change to 4 pin connector



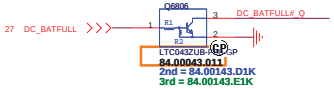
Change the connection



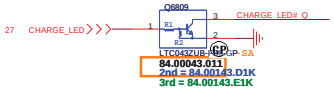


Battery LED2(DC_BATFULL)

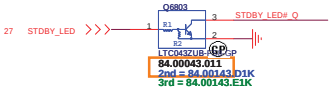
DY DY DY DY

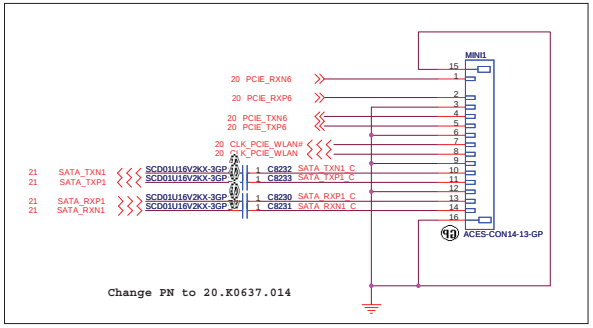


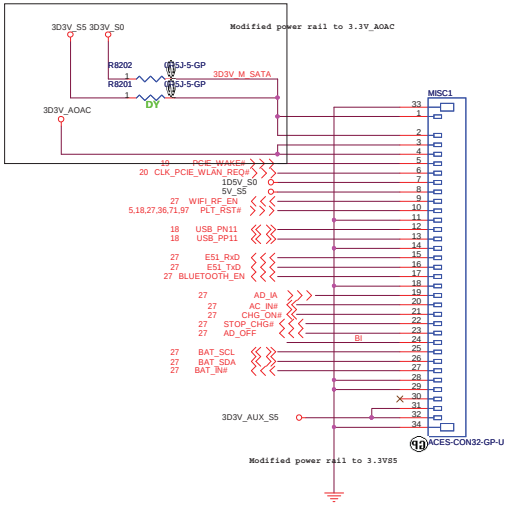
Battery LED1(CHARGE)



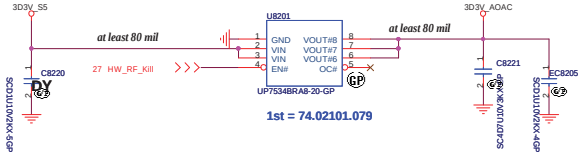
Power STDBY_LED

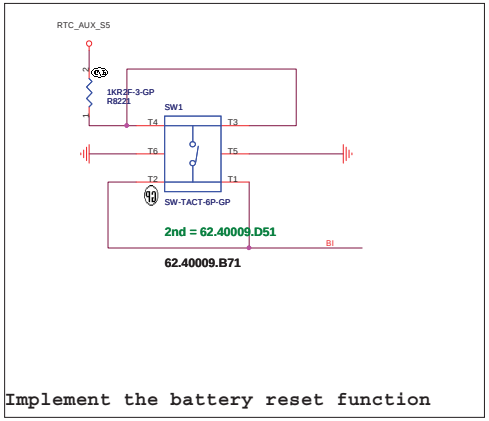


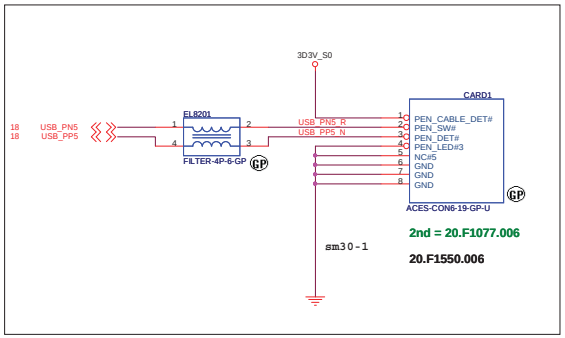




AOAC circuit







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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size	Document Number	Rev
A2	Hummingbird1_HR	-2

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size	Document Number	Rev
Custom	Hummingbird1_HR	-2
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU_DP/LVDS/CRT/GPIO(3/5)

Size	Document Number	Rev
Custom	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 85 of 102

<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., HsiChih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU_POWER(4/5)

Size	Document Number	Rev
A1	Hummingbird1_HR	-2

Date: Tuesday, April 17, 2012 Sheet 85 of 102

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU_DPPWR/GND(5/5)***

Size	Document Number	Rev
A3	**Hummingbird1_HR**	**-2**

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: Custom | Document Number: Hummingbird1_HR | Rev: -2

Date: Tuesday, April 17, 2012 | Sheet 88 of 102

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM3,4 (2/4)***

Size	Document Number	Rev
Custom	**Hummingbird1_HR**	**-2**
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
Custom	Hummingbird1_HR	-2
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<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
Custom	**Hummingbird1_HR**	**-2**
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<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RT8208B_+VGA_CORE***

Size	Document Number	Rev
Custom	**Hummingbird1_HR**	**-2**

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DISCRETE VGA POWER***

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

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LVDS Channel A

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size	Document Number	Rev
A4	Hummingbird1_HR	-2

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CRT_Switch*		
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SSID = SDIO

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TOUCH PANEL

Size	Document Number	Rev
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H1
HOLE237R95-GP

H2
HOLE237R95-GP

H3
HOLE237R95-GP

H4
HOLE237R95-GP

H5
HOLE237R95-GP

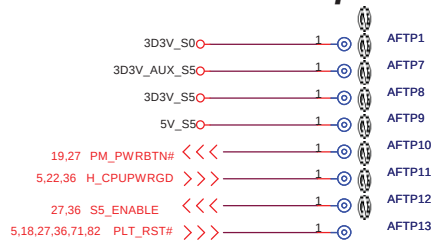
H6
HOLE237R95-GP

HS1
STF236R128H34-1-GP
34.4QP10.001

HS2
STF236R128H34-1-GP
34.4QP10.001

HS3
STF236R128H34-1-GP
34.4QP10.001

Check test point



Test Point放在Dimm Door打開可量測處

TPAD14-GPTP9701
5V_AUX_S5

SPR1
SPRING-24-GP-U

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS/EMI Capacitors***

Size	Document Number	Rev
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(1) change U6001 to socket 62.10089.001

(2) change SW_L1 and SW_R1 PN to 『62.40089.221』

(3) KI.G6501.001 / IC BD82HM65 SLH9D MM#908753 B2 FCBGA 989
KI.G6501.004 / IC BD82HM65 SLJ4P MM#914377 B3 FCBGA989P

(4)U3101 change PN to 71.08158.M02
(5)DM2 1st -> change PN to 62.10024.G01
(6) IMIC1 =>82.40012.001
(7) RJ1 =>22.10177.J71
(8) CPU1 =>1st change PN to 62.10055.321
(9) USB2 =>1st change PN to22.10218.G01 -> only Lab stage

[Lab] S01G ==>1st
S02G ==>2nd(NEC Cap)

Coin Battery:
1st:23.20068.001
2nd:23.22063.001

-SA

-SB

-1

-2

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size	Document Number	Rev
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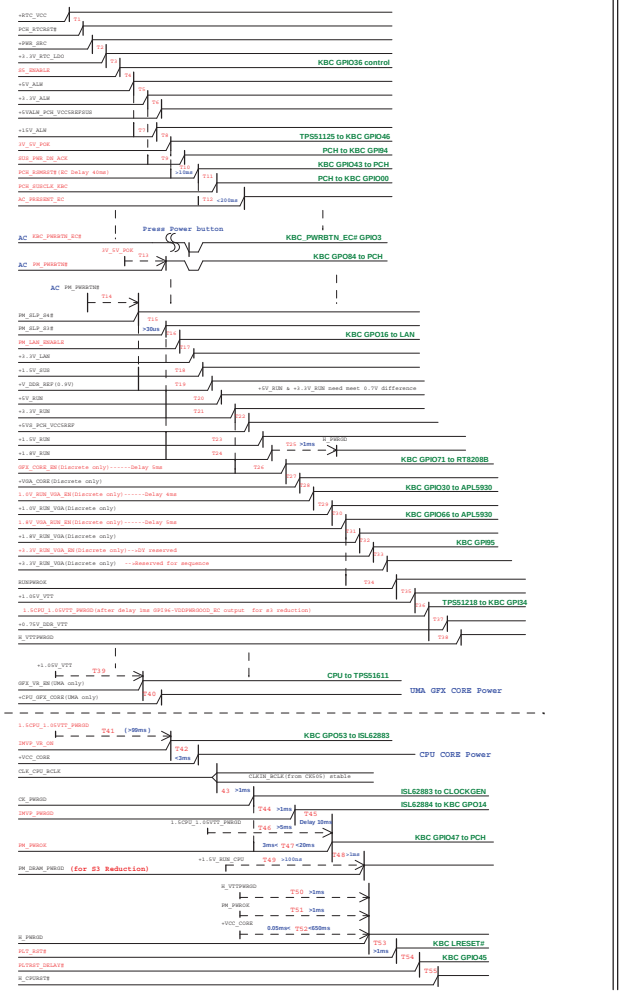
Intel-Power Up Sequence

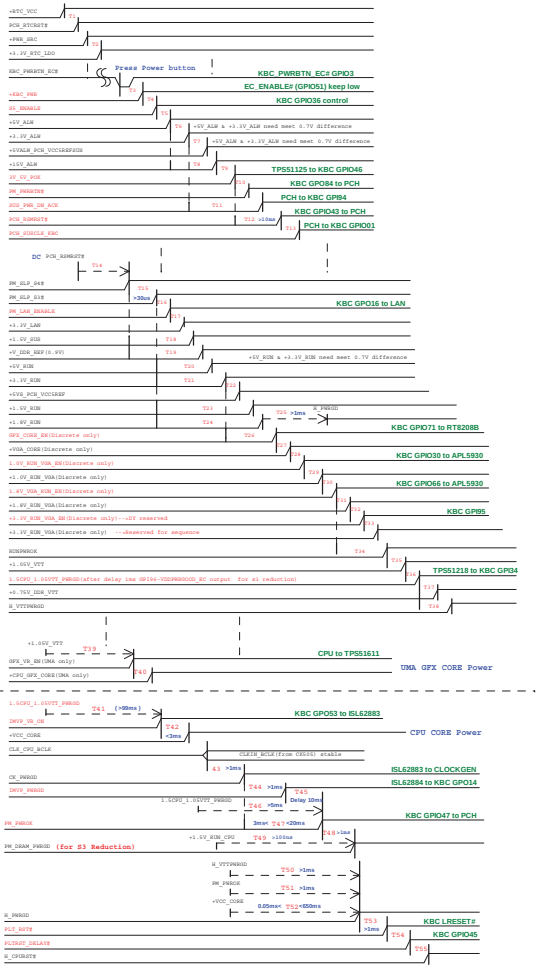
(AC mode)

red word: KBC GPIO

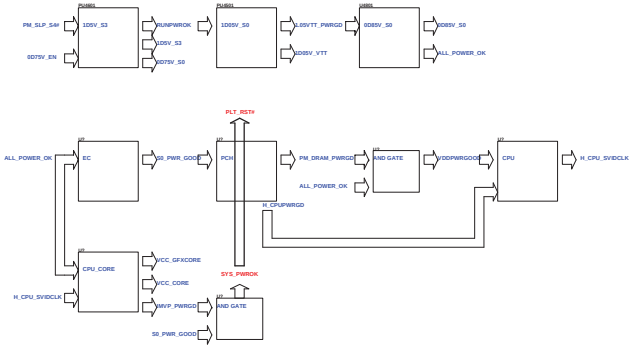


(DC mode)

red word: KBC GPIO



Power Sequence

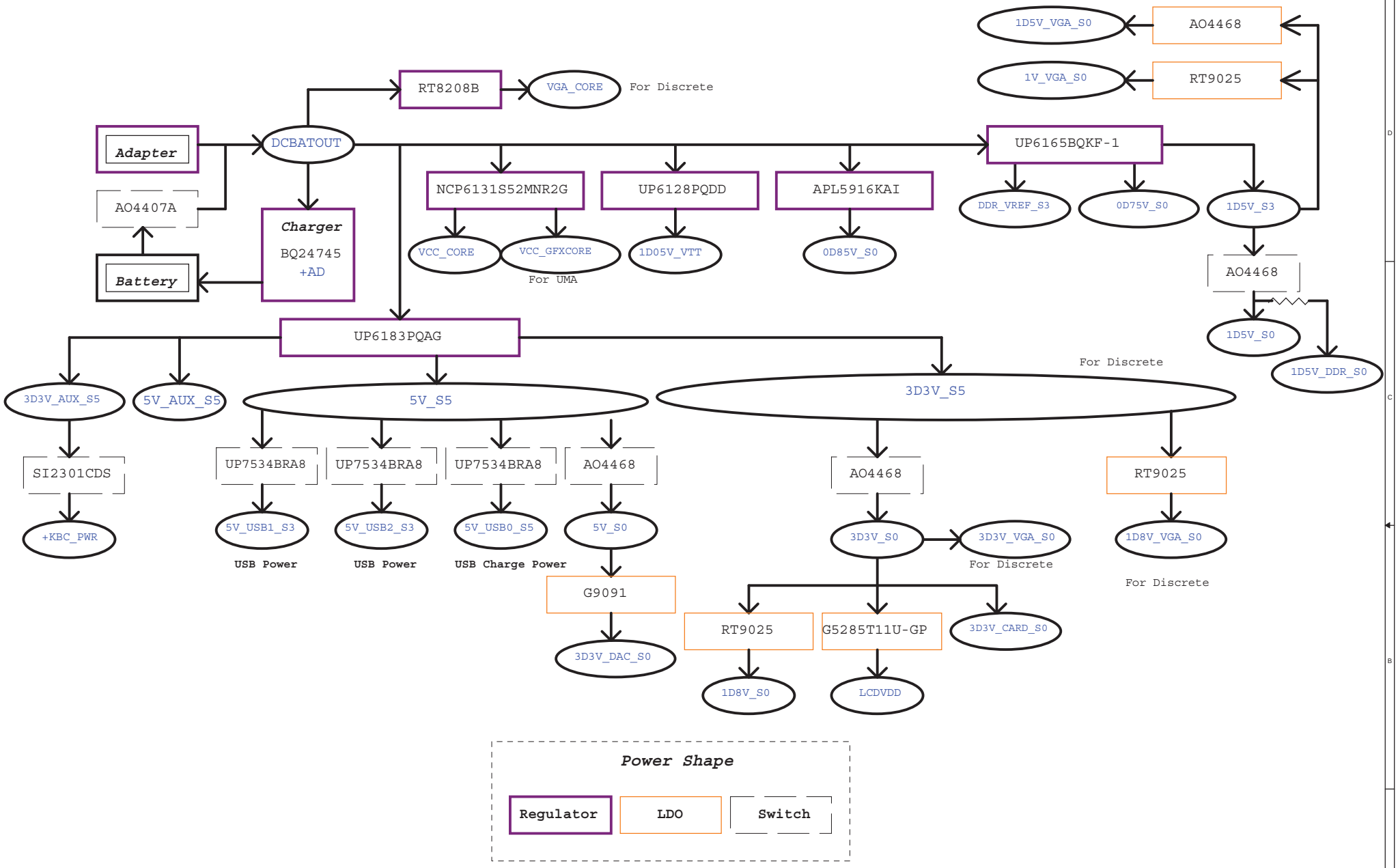


Wistron Corporation

Power Sequence

Hummingbird1_HR

-2



HR PX

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Power Block Diagram		
Size: A3	Document Number: Hummingbird1 HR	Rev: -2
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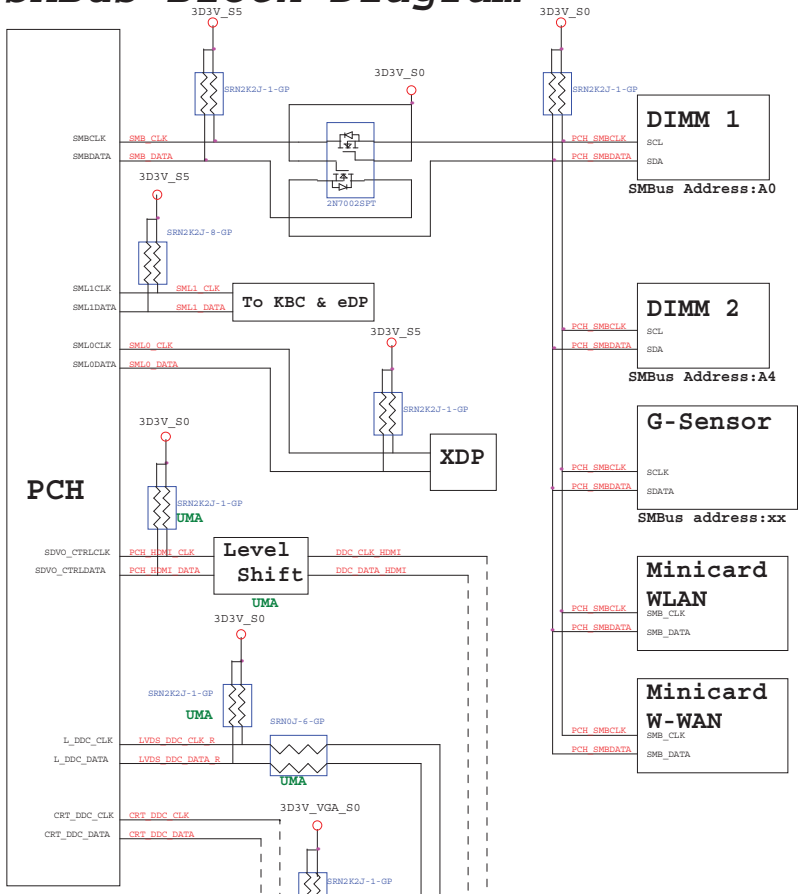
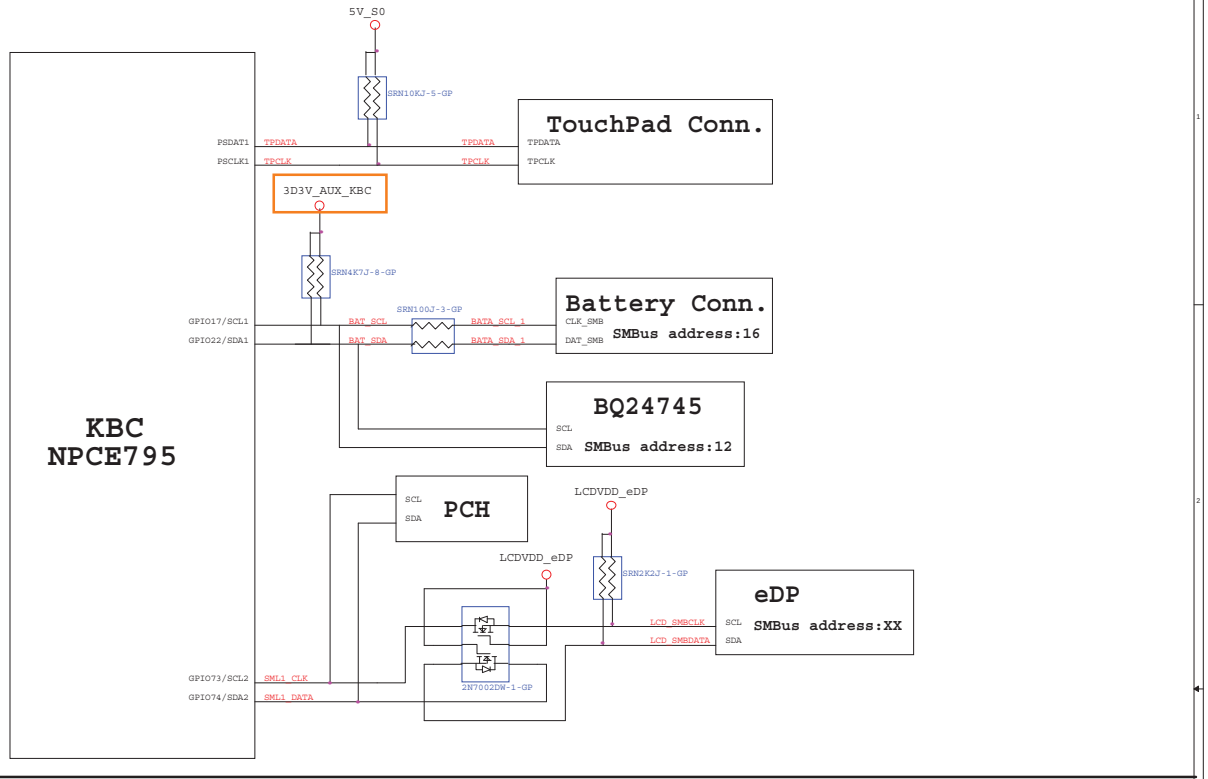
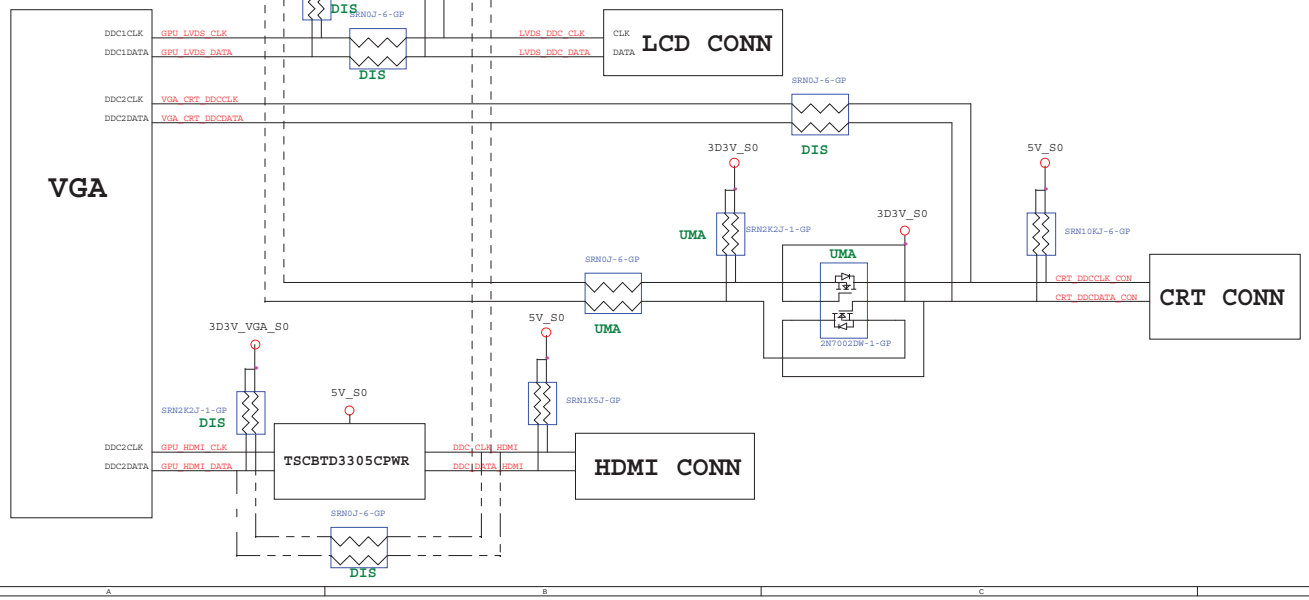
PCH SMBus Block Diagram



KBC SMBus Block Diagram





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

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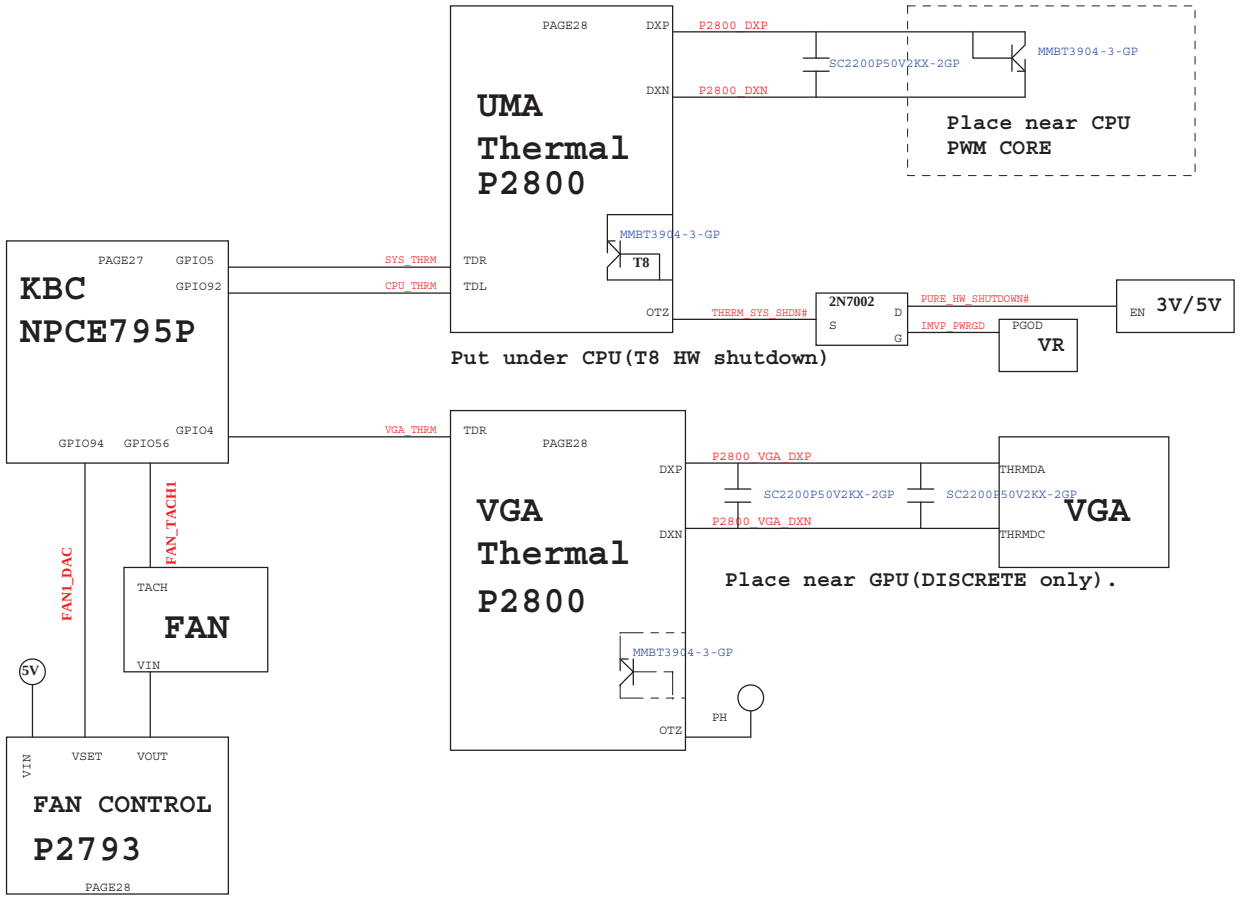
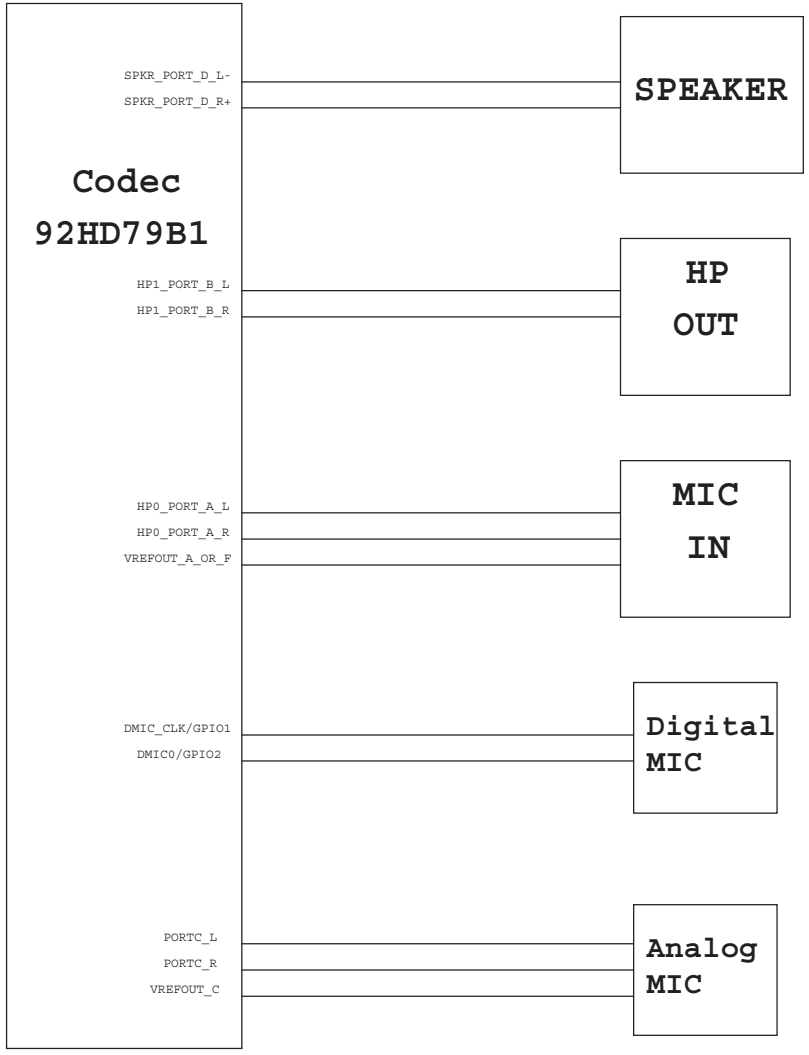
Thermal Block Diagram



Audio Block Diagram



<Variant Name>

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Title	Thermal/Audio Block Diagram	
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