

<b>REGULATOR (DDR3)</b> 1.5VSUS, 0.75VSMDDR_VTERM,1.5V 1.5V_GPU,1.5V_CPU
<b>REGULATOR</b> +1.05V_VTT,+1.8V
<b>DC/DC</b> 3VPCU, 5VPCU, +15V PG 42
<b>CPU Core</b> PG 43
<b>VGA Core Discrete</b> PG 44



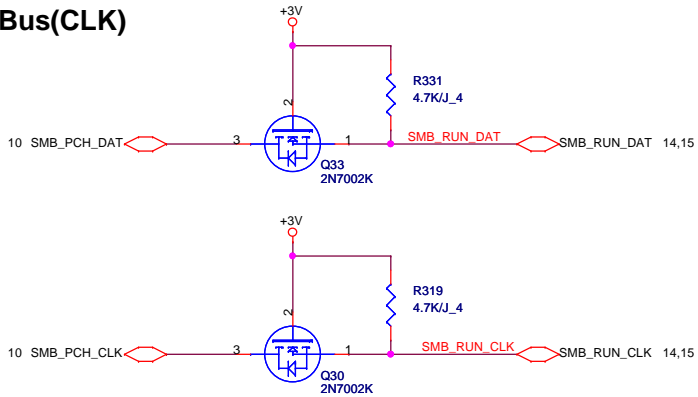
02/20 DEL for Pre-ES1


CPU\_CLK select(CLK)

02/20 DEL for Pre-ES1

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

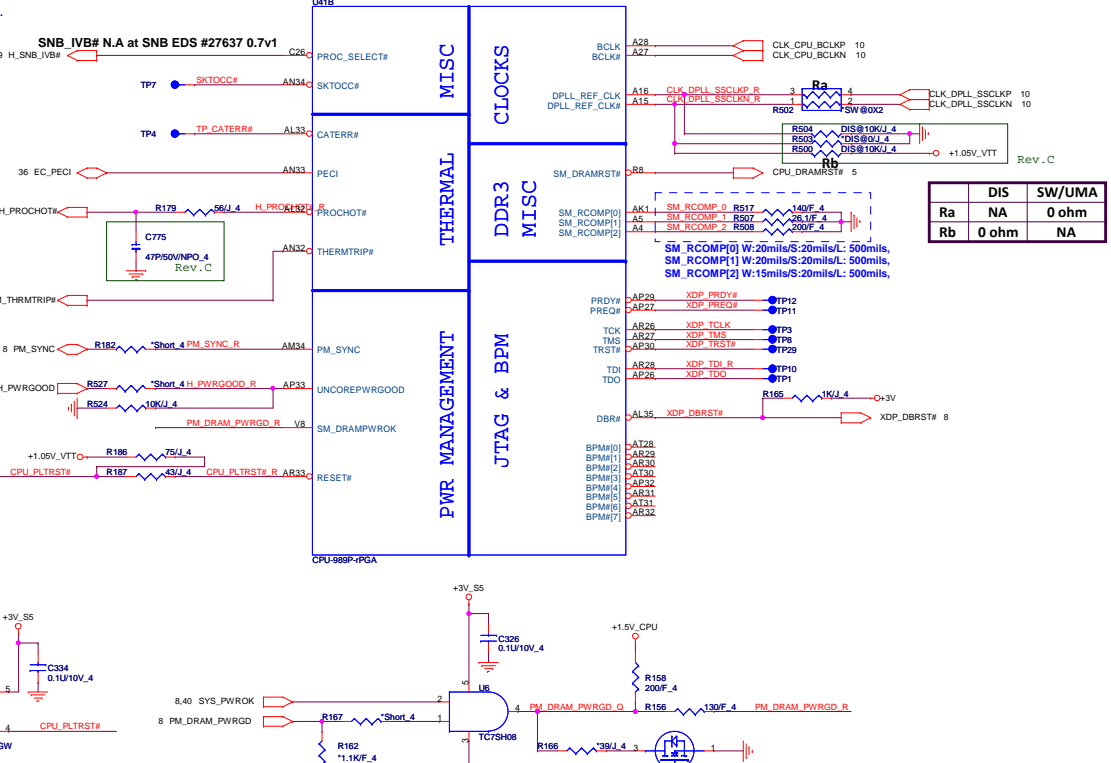
SMBus(CLK)



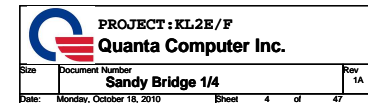
PROJECT:KL2E/F  
Quanta Computer Inc.

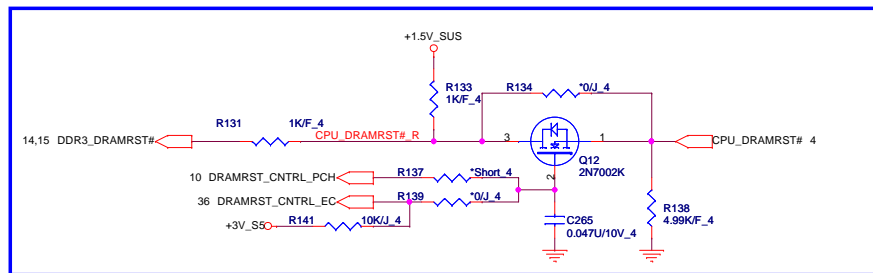
Size	Document Number	Rev
	<b>Clock Generator</b>	1A
Date:	Monday, October 18, 2010	Sheet 3 of 47

## Sandy Bridge Processor (CLK,MISC,JTAG)



### Processor pull-up(CPU)

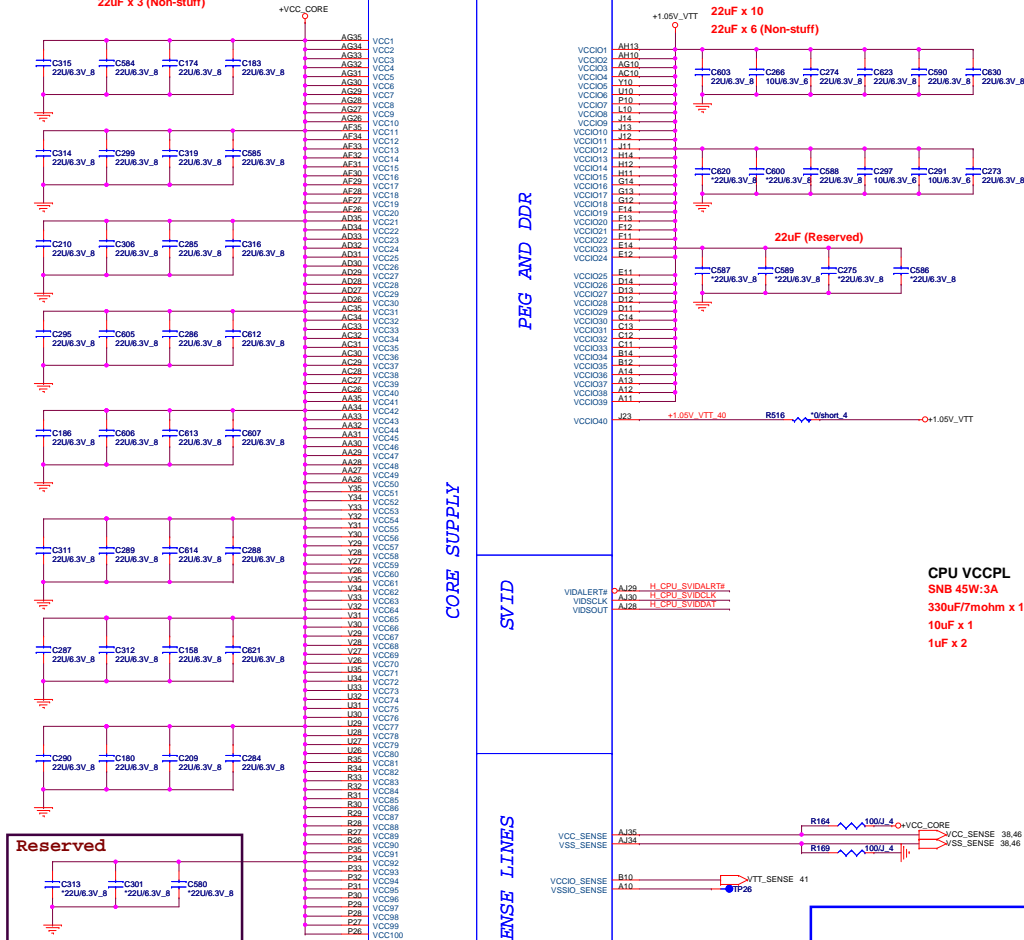




## Sandy Bridge Processor (POWER)

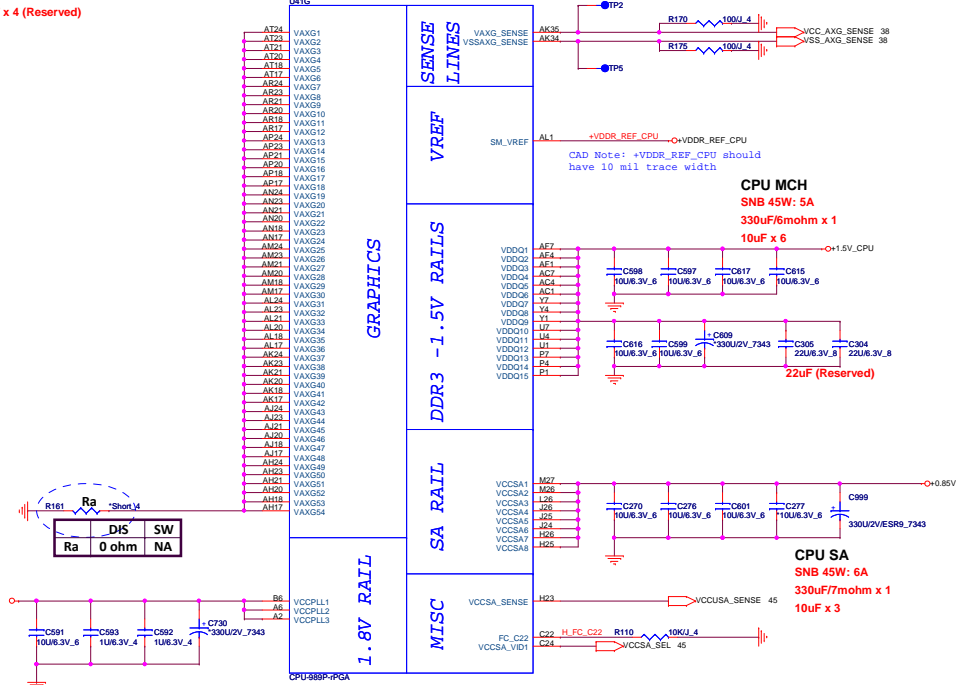
**CPU Core Power**  
**SNB 45W:55A**  
 22uF x 32  
 22uF x 3 (Non-stuff)

## POWER

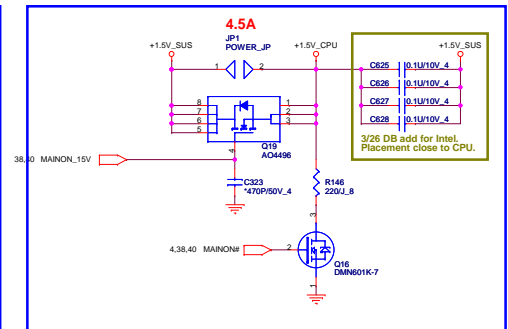
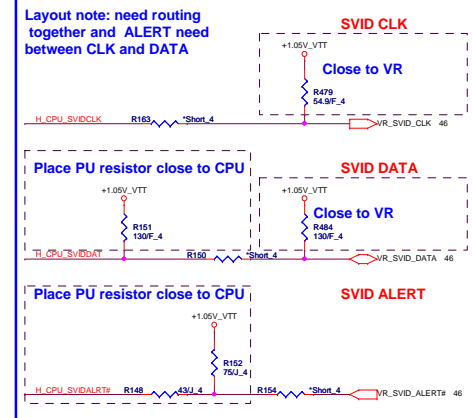


**CPU VGT**  
**SNB 45W:22A**  
**22uF x 12**  
**22uF x 4 (Reserved)**

## POWER



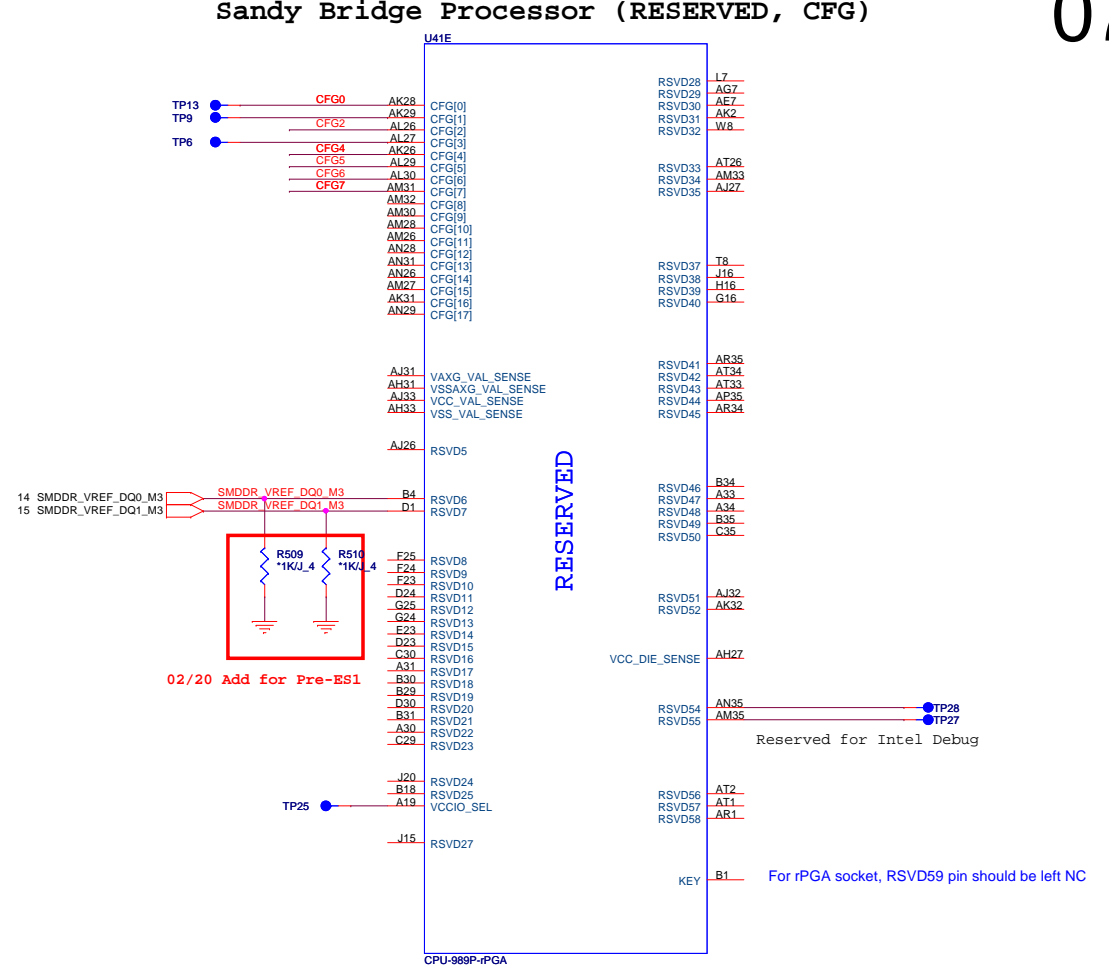
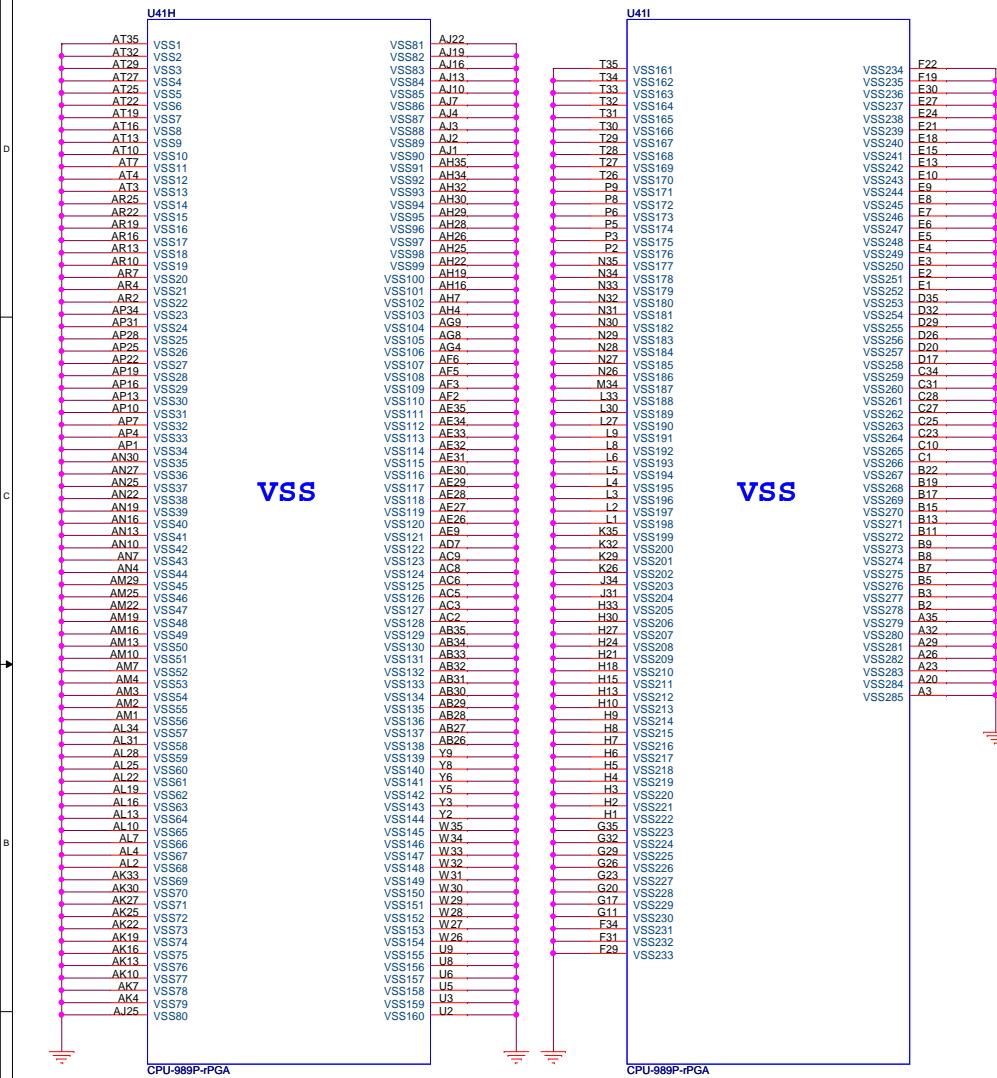
Layout note: need routing together and ALERT need between CLK and DATA



## Sandy Bridge Processor (GND)

## Sandy Bridge Processor (RESERVED, CFG)

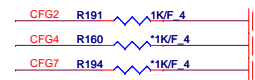
07



## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



## CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

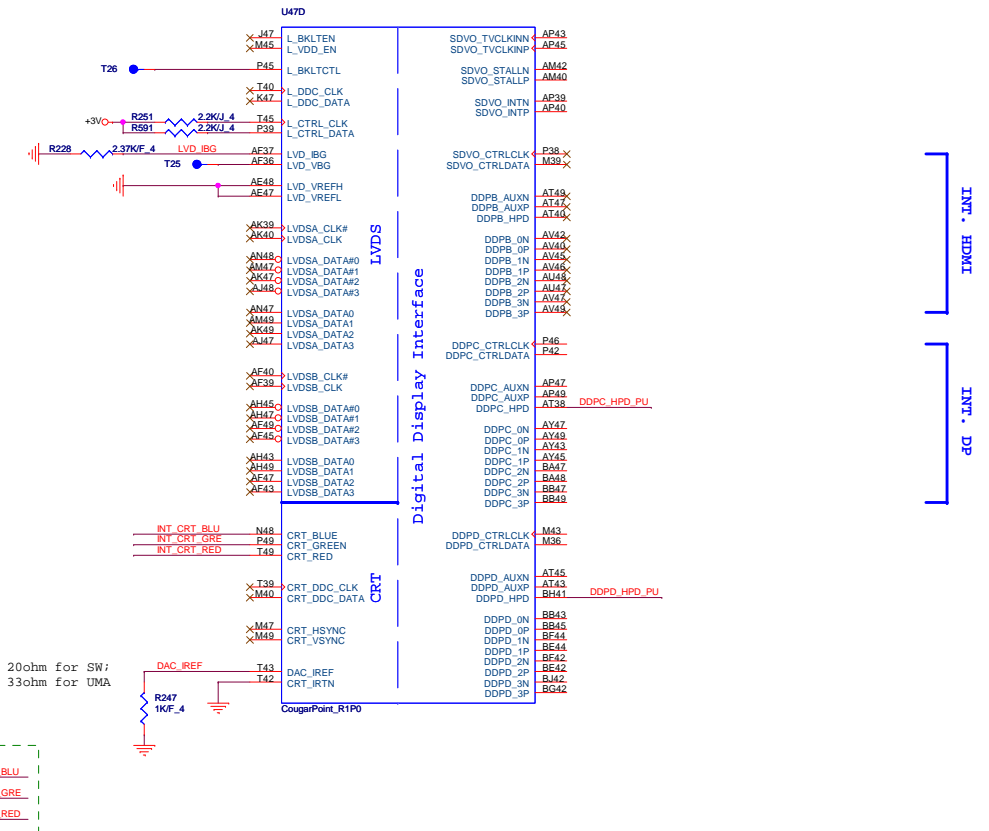
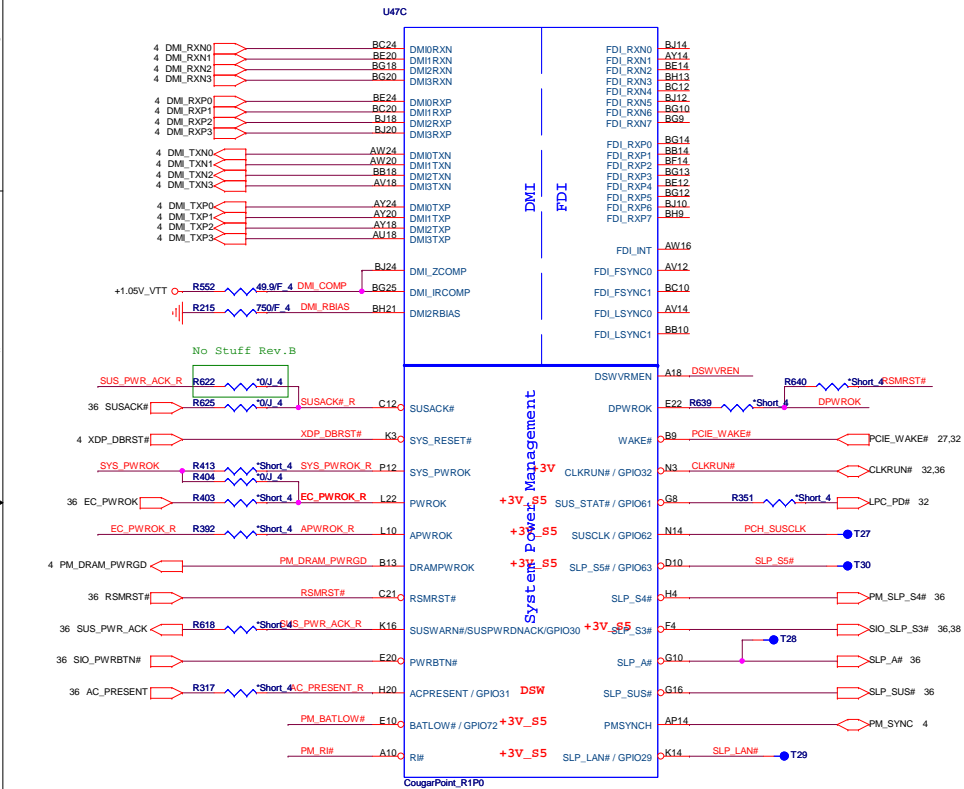
PROJECT : KL2E  
Quanta Computer Inc.

Size Document Number Rev 1A  
Sandy Bridge 4/4

Date: Monday, October 18, 2010 Sheet 7 of 47

## Cougar Point (LVDS,DDI)

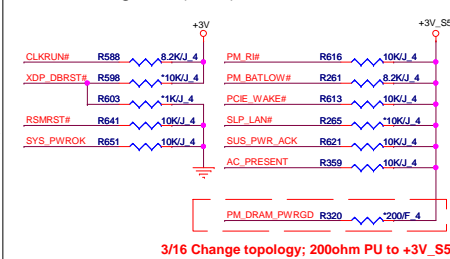
## Cougar Point (DMI,FDI,PM)



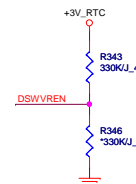
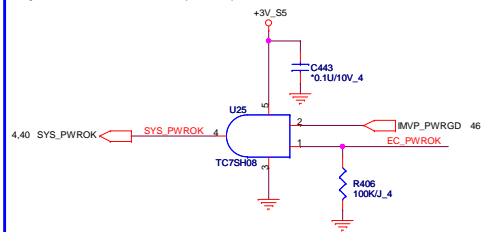
INT. HDMI

INT. DP

## PCH Pull-high/low(CLG)



## System PWR\_OK(CLG)

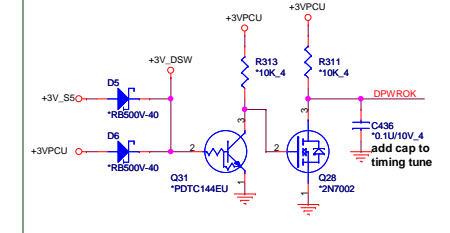


On Die DSW VR Enable

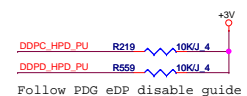
High = Enable (Default)

Low = Disable

## DPWROK FOR DSW



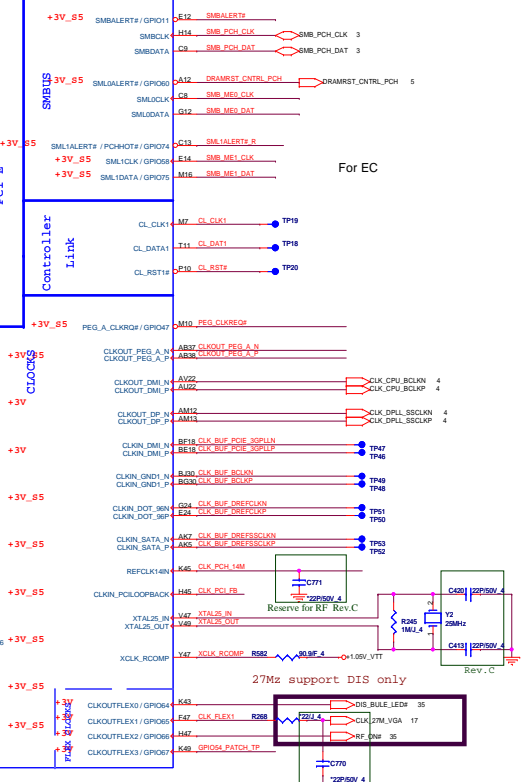
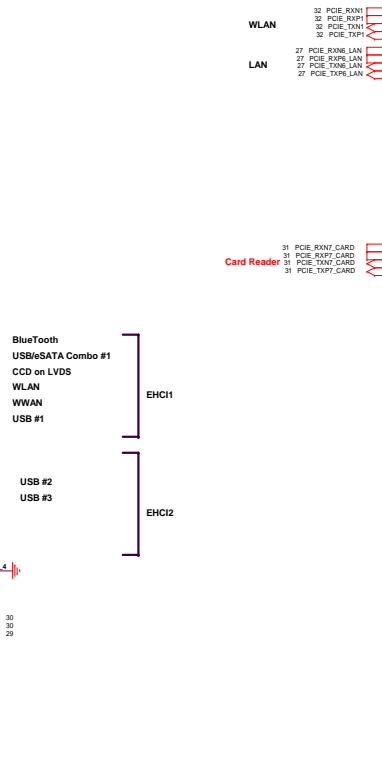
No Stuff Rev.c



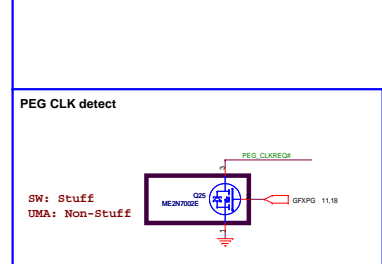


09

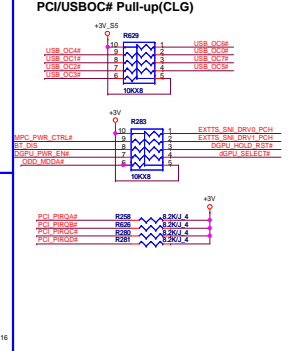
Cougar Point-M (PCI-E,SMBUS,CLK)



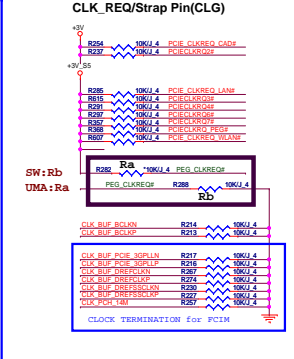
PEG CLK detect



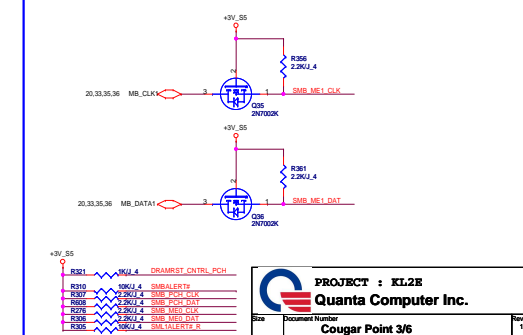
PCI/USBOC# Pull-up(CLG)



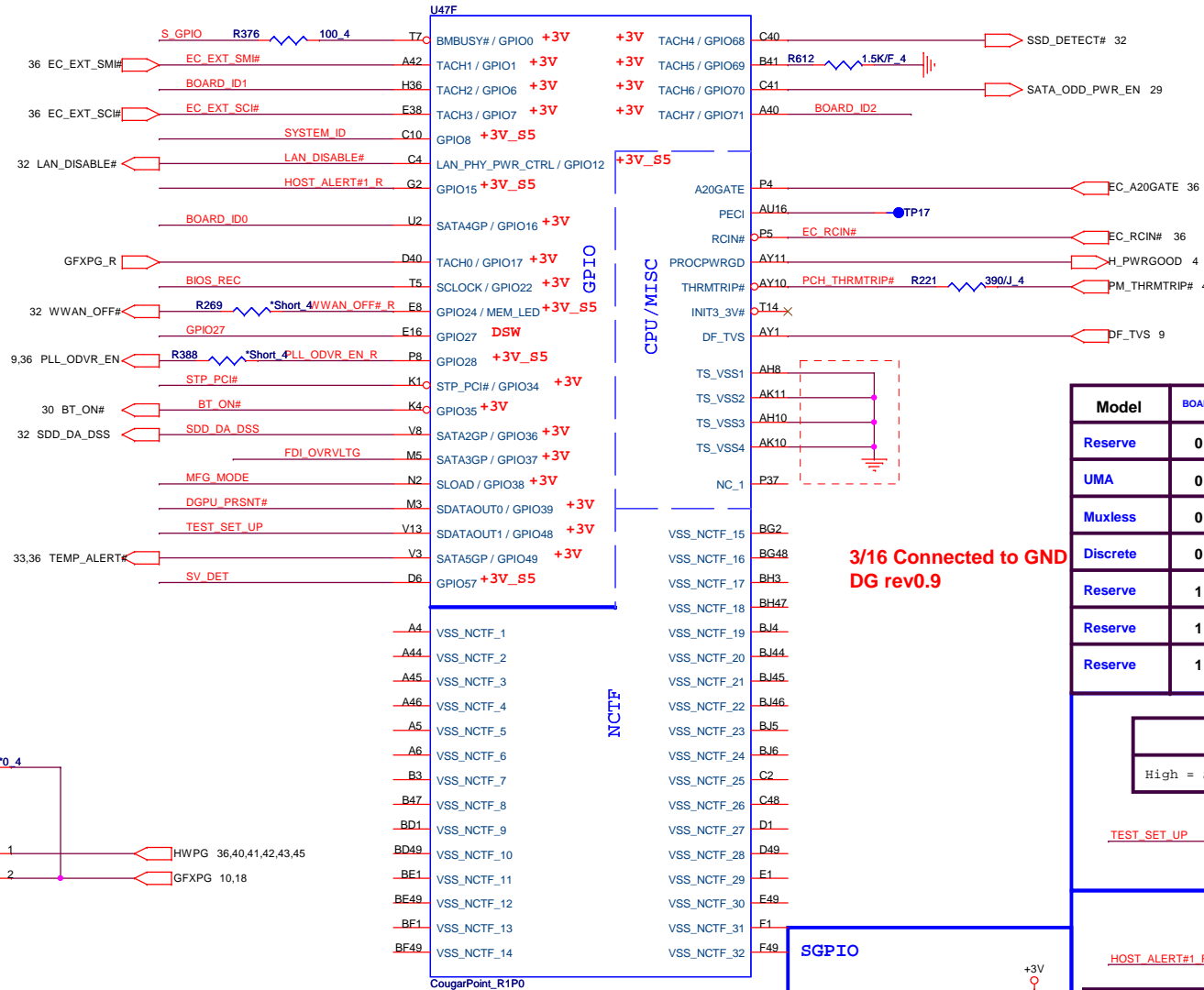
## 1



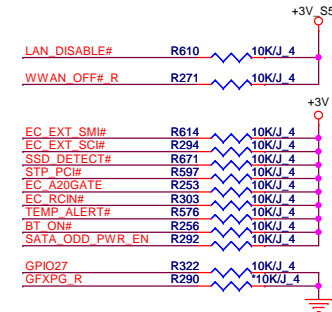
1000



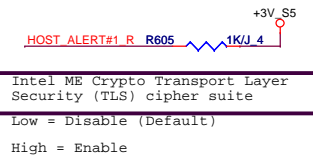
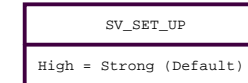
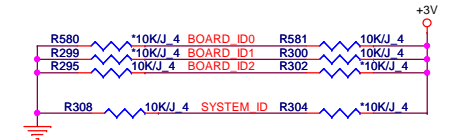
## Cougar Point (GPIO,VSS\_NCTF,RSVD)



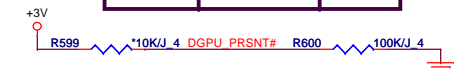
### **GPIO Pull-up/Pull-down(CLG)**



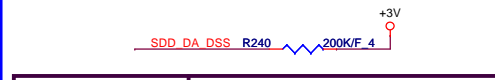
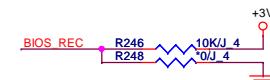
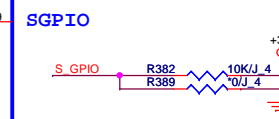
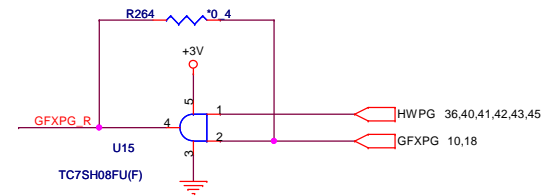
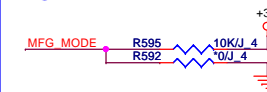
Model	BOARD_ID2	BOARD_ID1	BOARD_ID3
Reserve	0	0	0
UMA	0	0	1
Muxless	0	1	0
Discrete	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0



	SWITCHABLE	UMA
Stuff	R599	R600
No Stuff	R600	R599



## MFG-TEST

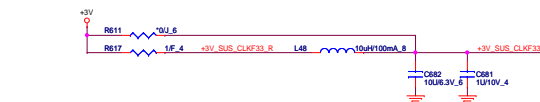


FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage
-------------------------------------	--

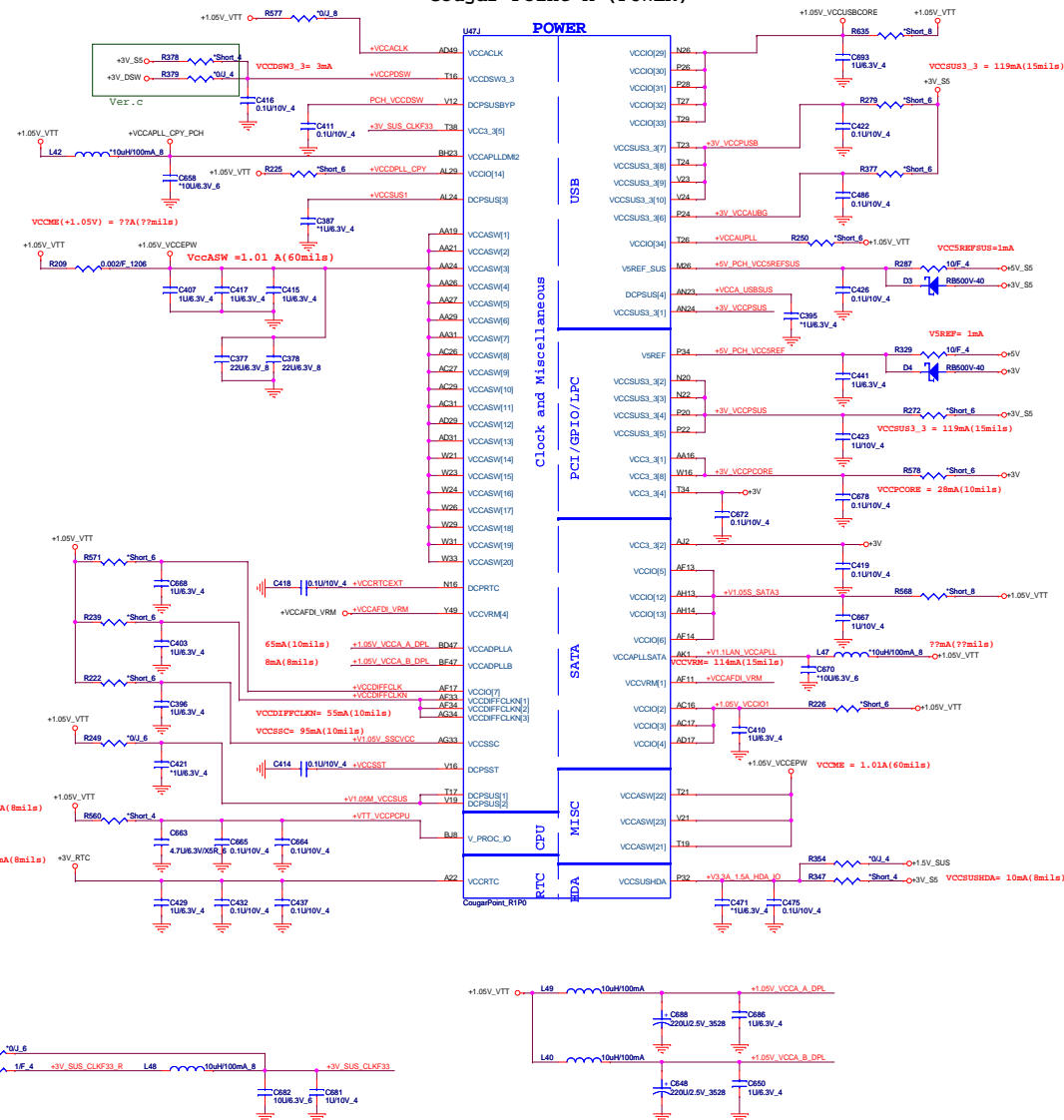
DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)
-------------------------------------	--

BIOS RECOVERY	High = Disable (Default) Low = Enable
---------------	--

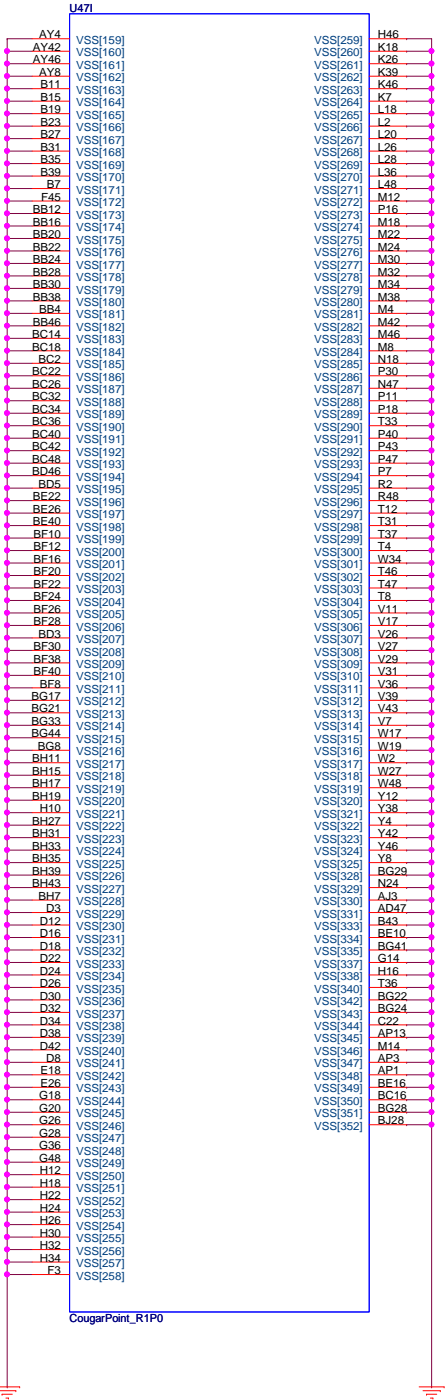
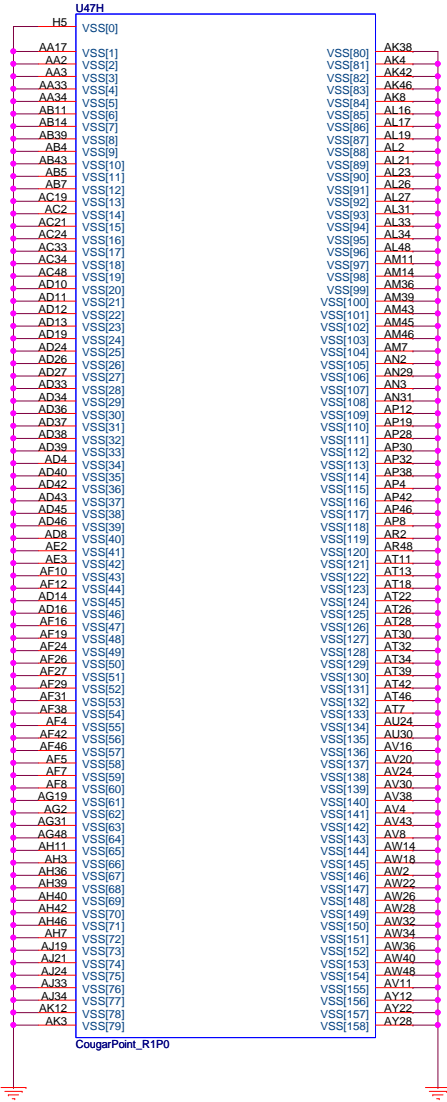
## COUGAR POINT (POWER)



## POWER

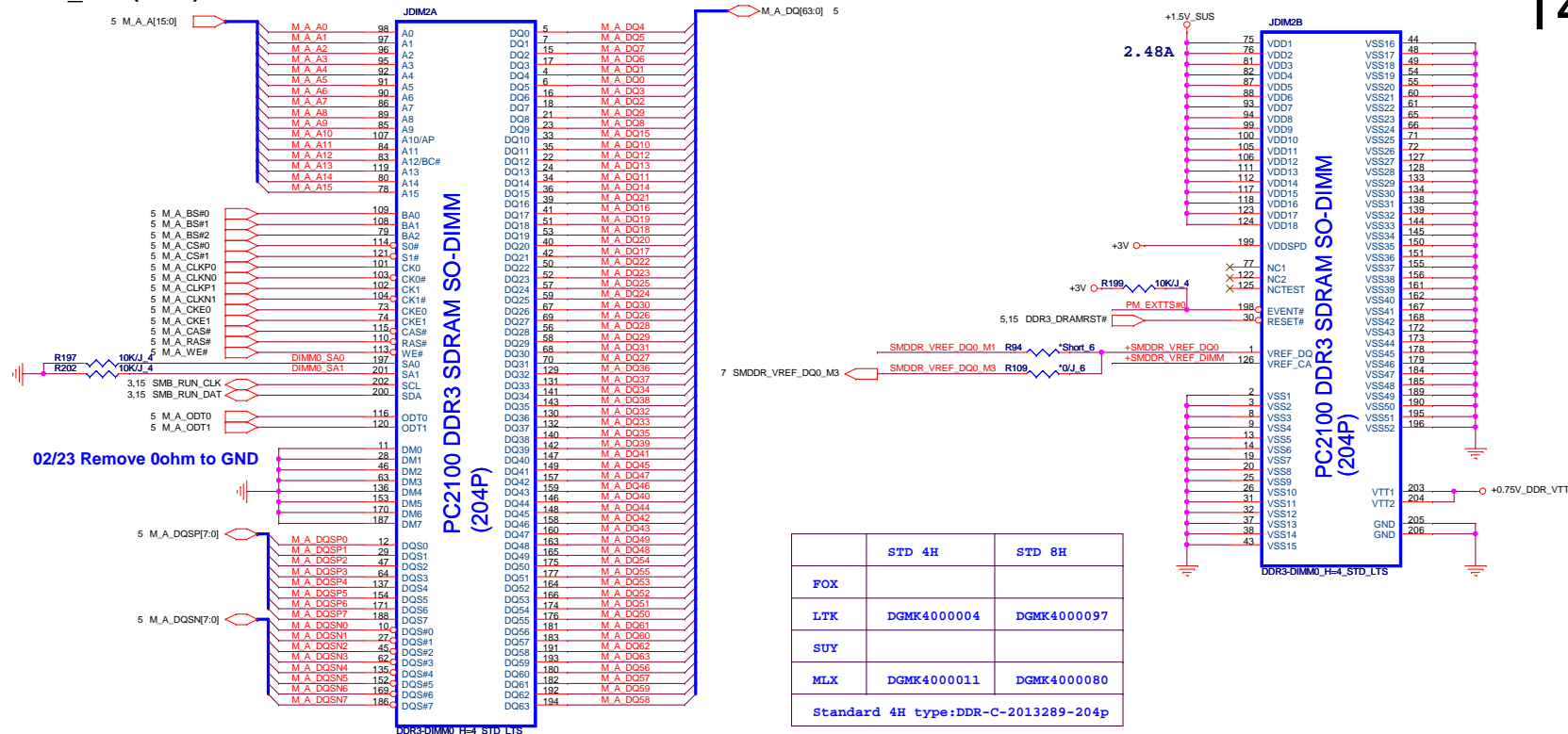


IBEX PEAK-M (GND)

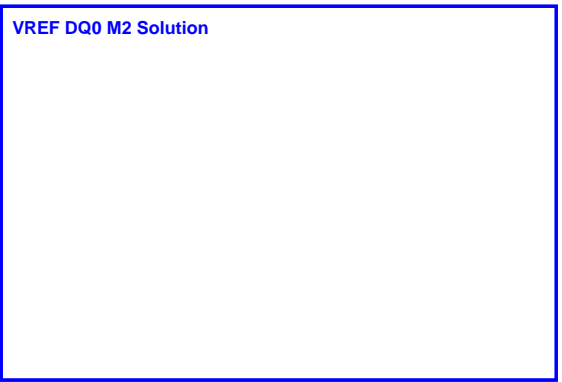


# DDR\_STD (DDR)

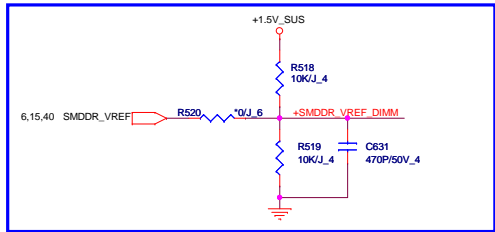
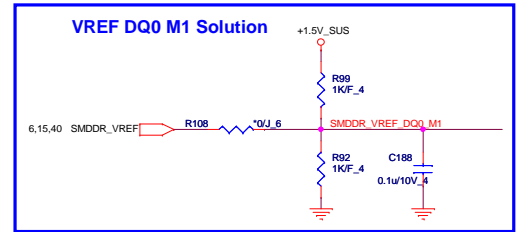
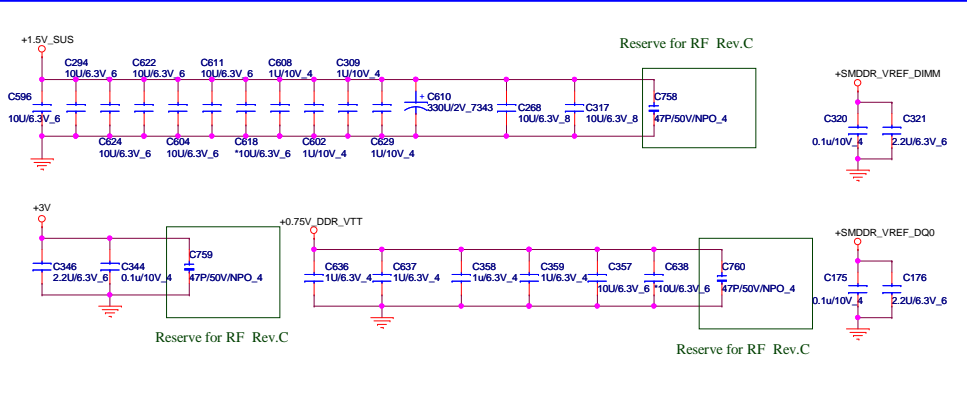
14



	STD 4H	STD 8H
FOX		
LTK	DGМК4000004	DGМК4000097
SUY		
MLX	DGМК4000011	DGМК4000080
Standard 4H type:DDR-C-2013289-204p		



Place these Caps near So-Dimm0.







	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

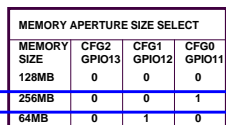






Note : Required Frequency = 800 MHz

### APERTURE SIZE



Access to SCL and SDA  
is mandatory on BAC0  
design for debug  
purposes.

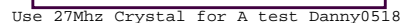


## Power PWM config

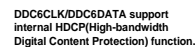
- ```
1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU PWROK
```



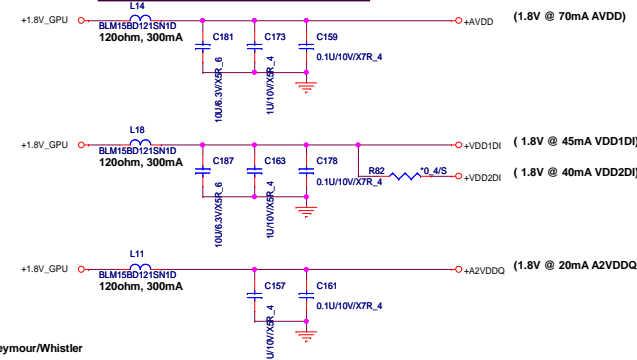
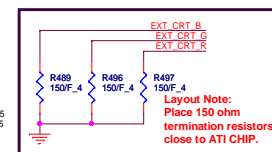
PLACE  
VREF  
DIVIDER  
AND CAP  
CLOSE TO  
ASIC



Capilano Pro/Robson\_M2



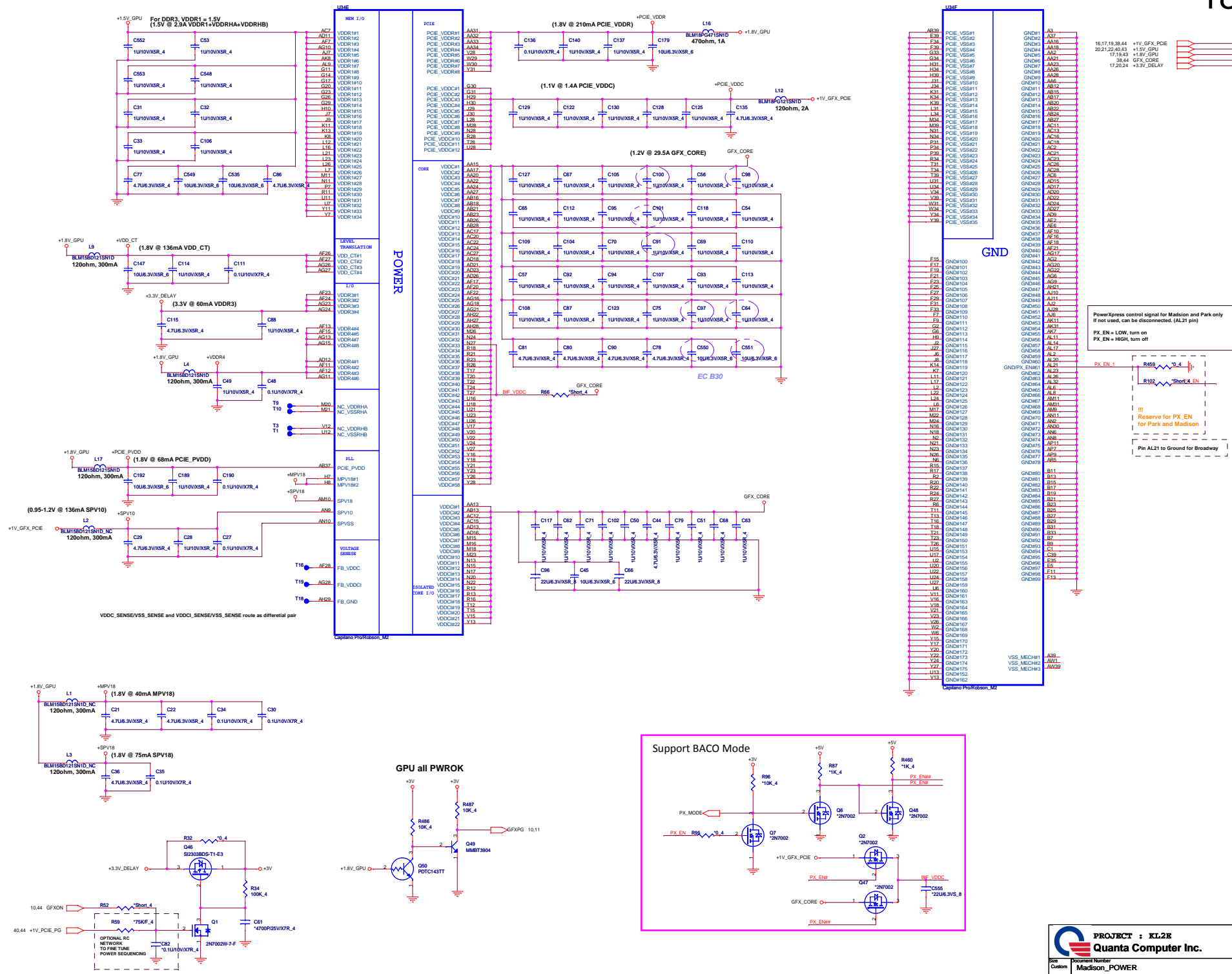
| CONFIGURATION STRAPS    |                       |                                                                                                                                                                                     |
|-------------------------|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STRAPS                  | PIN                   | DESCRIPTION                                                                                                                                                                         |
| TX_PWRS_ENB             | GPIO0                 | PCIE FULL TX OUTPUT SWING<br>0 = 50% Tx output swing<br>1 = Full Tx output swing                                                                                                    |
| TX_DEEMPH_EN            | GPIO1                 | PCIE TRANSMITTER DE-EMPHASIS ENABLED<br>0 = Disable ; 1 = Enable                                                                                                                    |
| BIF_GEN2_EN_A           | GPIO2                 | 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on.<br>1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.                                                  |
| GPIO_5_AC_BATT (M96-M2) | GPIO5                 | 1 = AC (Performance mode)<br>0 = Battery saving mode                                                                                                                                |
| VGA_DIS                 | GPIO9                 | 0: VGA Controller capacity enabled<br>1: The device will not be recognized as the system's VGA controller                                                                           |
| BIOS_ROM_EN             | GPIO22                | Enable external BIOS ROM device<br>0 = Disable ; 1 = Enable                                                                                                                         |
| AUD[1]<br>AUD[0]        | VGAAHSYNC<br>VGAVSYNC | AUD[1:0]:<br>00 - No audio function;<br>01 - Audio for DisplayPort only;<br>10 - Audio for DisplayPort and HDMI if dongle is detected;<br>11 - Audio for both DisplayPort and HDMI. |
| VIP_DEVICE_STRAP_EN     | BIOS_ROM_EN           | VIP Device Strap Enable<br>0 = Disable ; 1 = Enable                                                                                                                                 |



NC on Seymour/Whistler

HDM

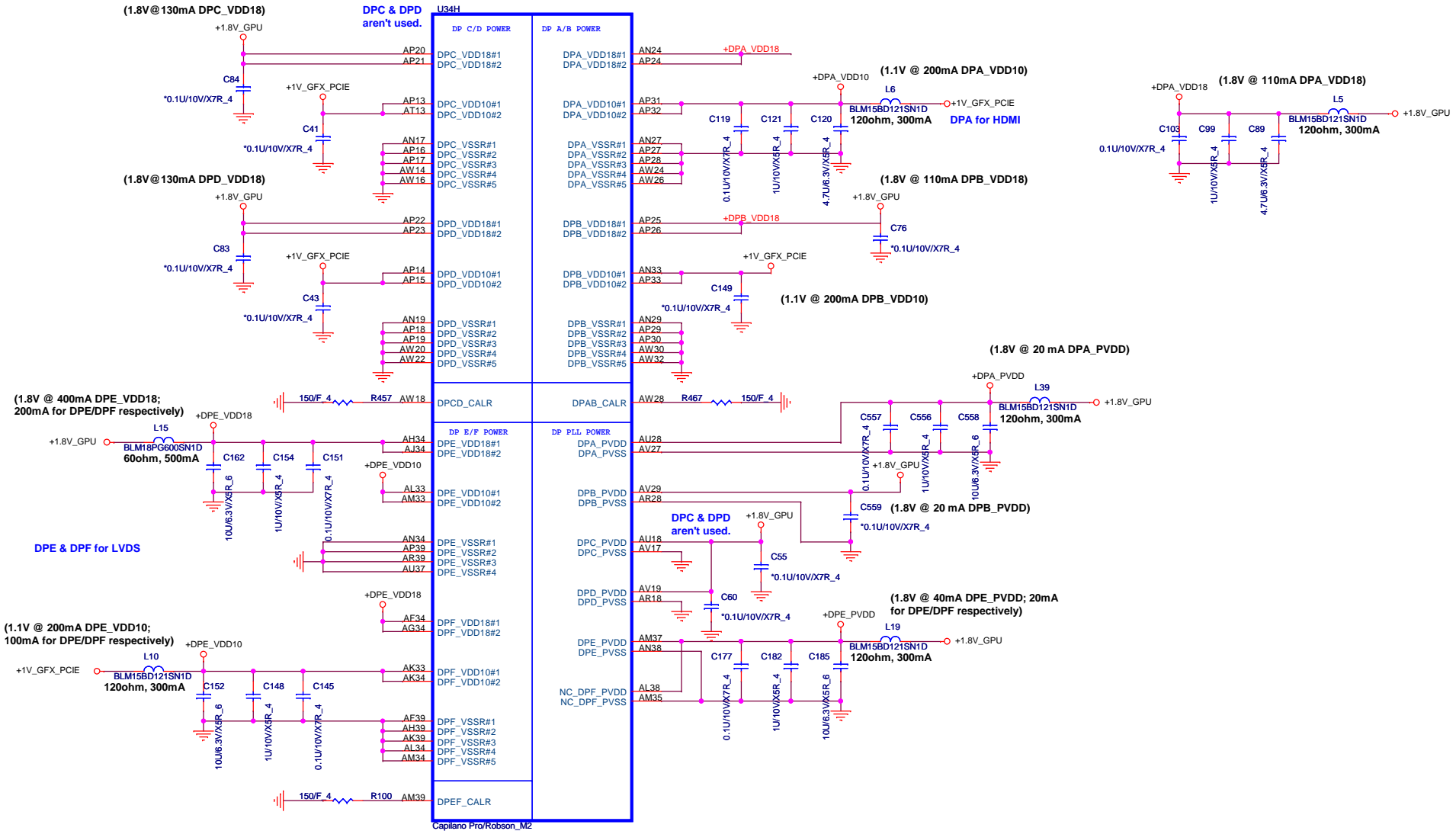
CRT



!!!  
For M96/92, DPx\_VDD10 = 1.1V  
For M97 DPx\_VDD10 = 1.0V

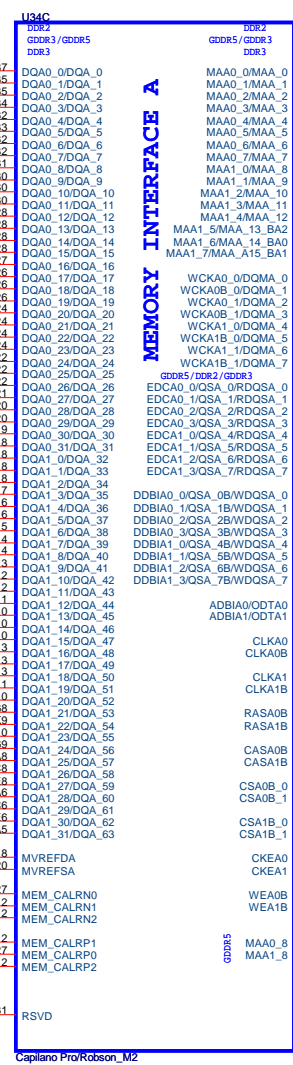
16,17,18,38,44 +1V\_GFX\_PCIE  
17,18,43 +1.8V\_GPU

19



18,21,22,40,43 +1.5V\_GPU  
17,18,24 +3.3V\_DELAY

### MEMORY INTERFACE A

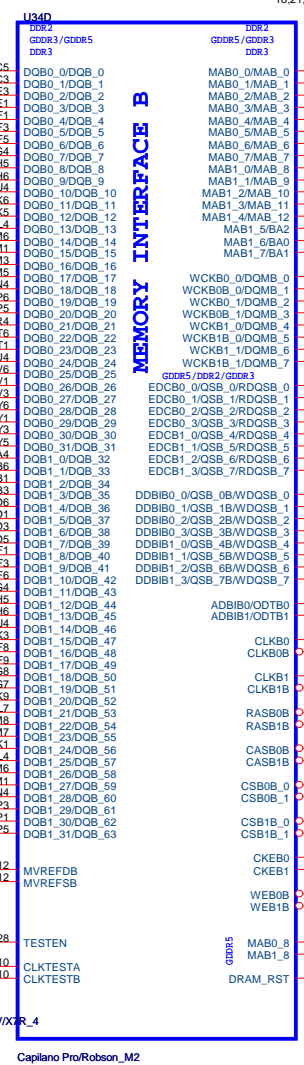


Caplano Pro/Robson\_M2

### DDR3/GDDR3 Memory Stuff Option

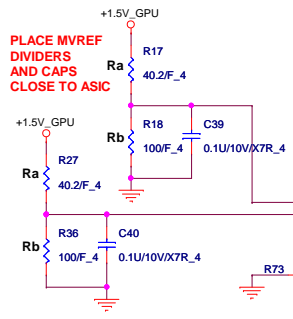
|       | GDDR3 | DDR3 |
|-------|-------|------|
| MVDDQ | 1.8V  | 1.5V |
| Ra    | 40.2R | 100R |
| Rb    | 100R  | 100R |

### MEMORY INTERFACE B

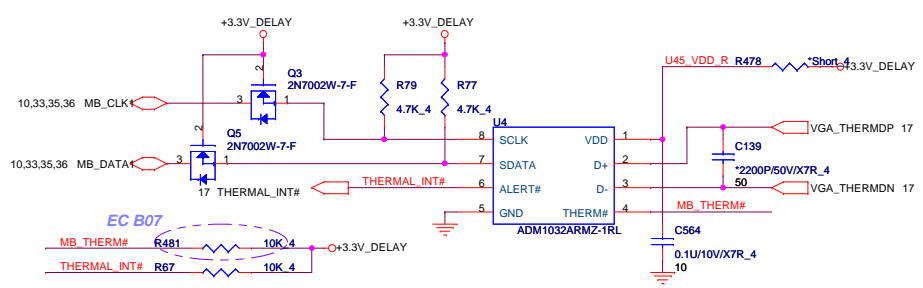


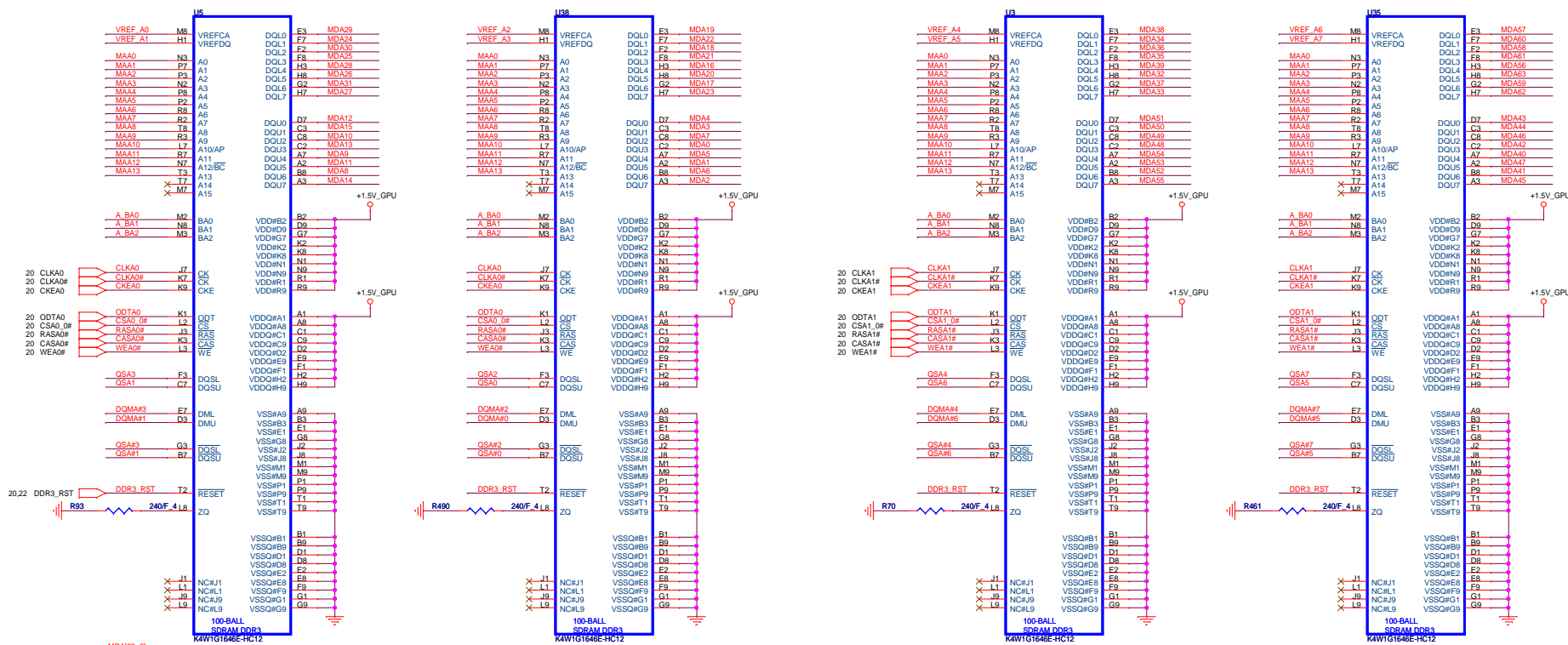
Caplano Pro/Robson\_M2

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



### THERMAL MONITOR





100-BALL SDRAM DDR3

KW1G1646E-HC12

100-BALL SDRAM DDR3

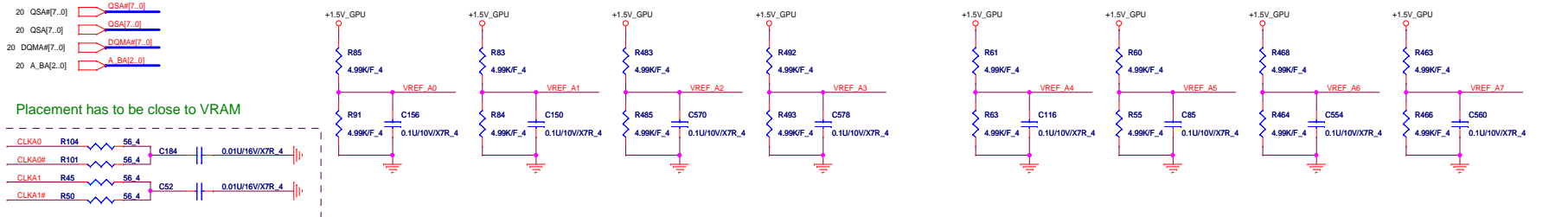
KW1G1646E-HC12

100-BALL SDRAM DDR3

KW1G1646E-HC12

100-BALL SDRAM DDR3

KW1G1646E-HC12



Placement has to be close to VRAM

Close to U4

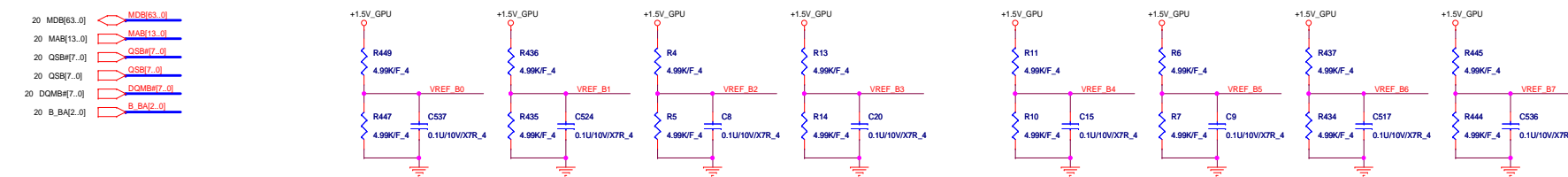
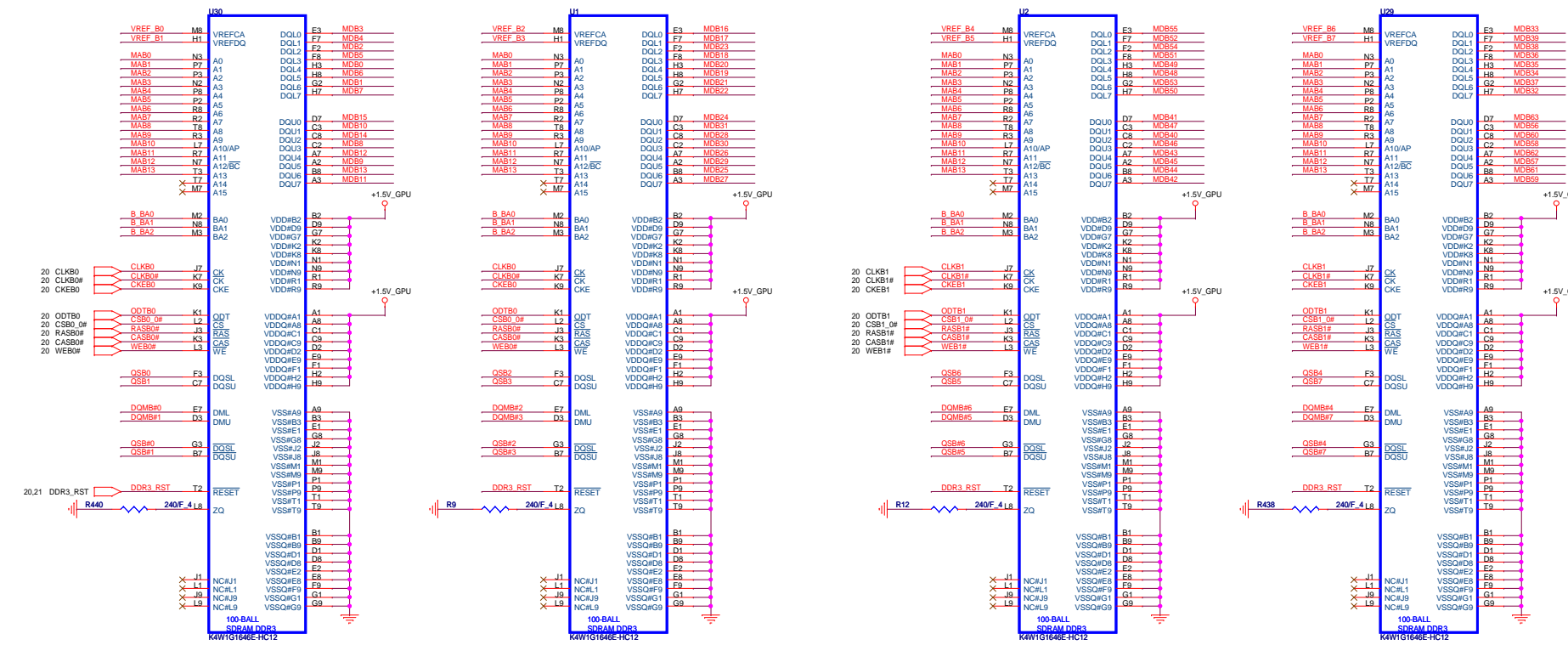
Close to U44

Close to U3

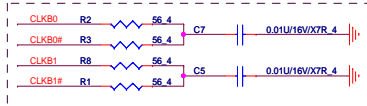
Close to U41

Close to U4 &amp; U44

Close to U3 &amp; U41



Placement has to be close to VRAM

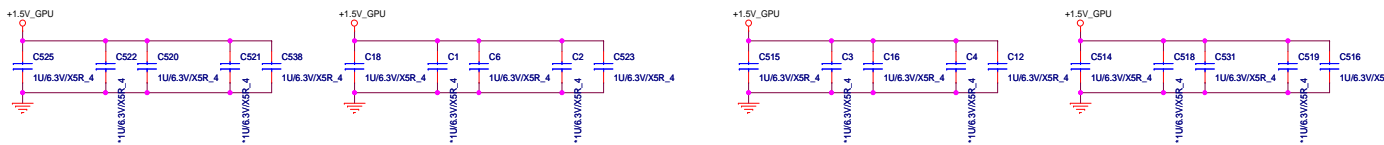


Close to U35

Close to U1

Close to U2

Close to U36



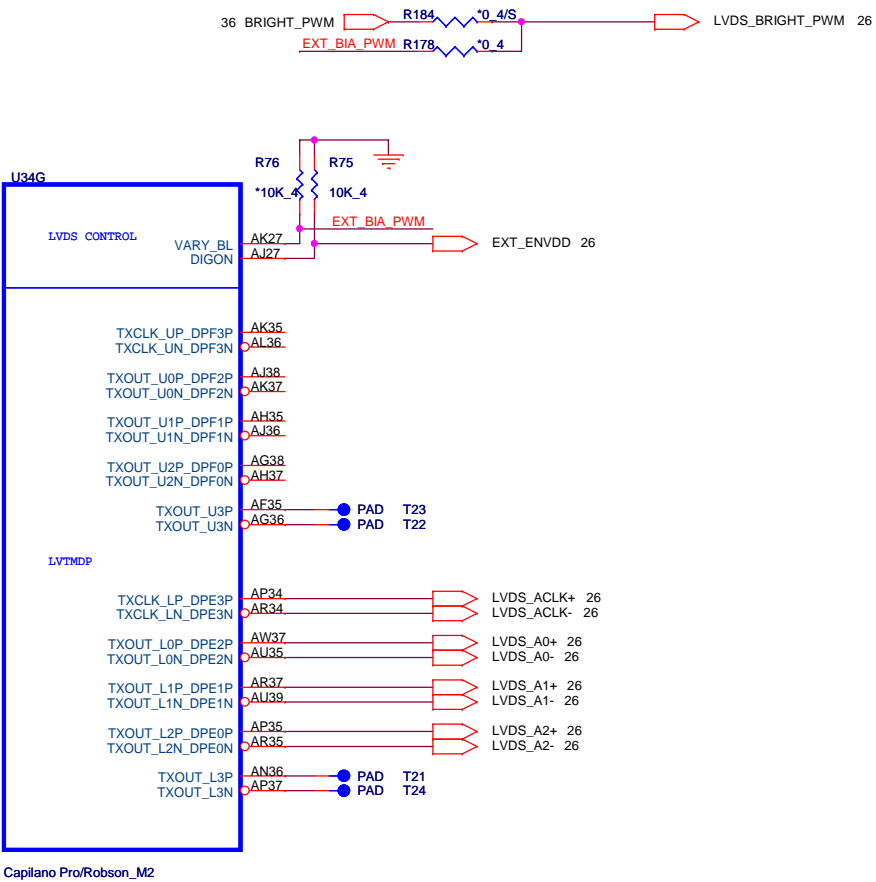
Close to U35 & U1

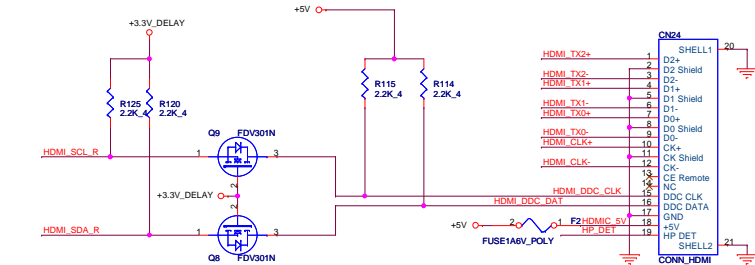
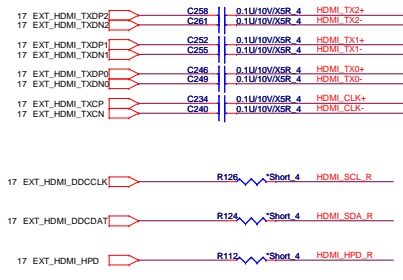
Close to U2 & U36



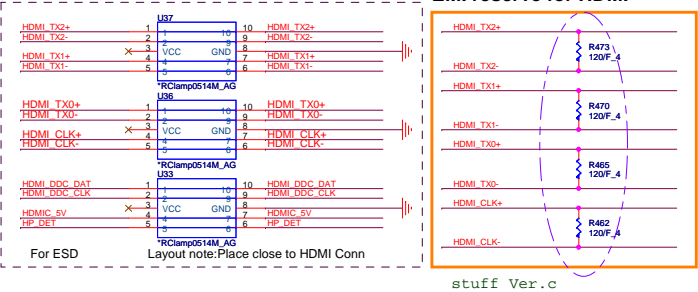
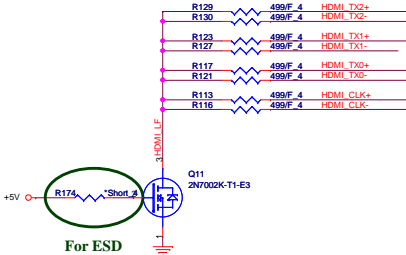
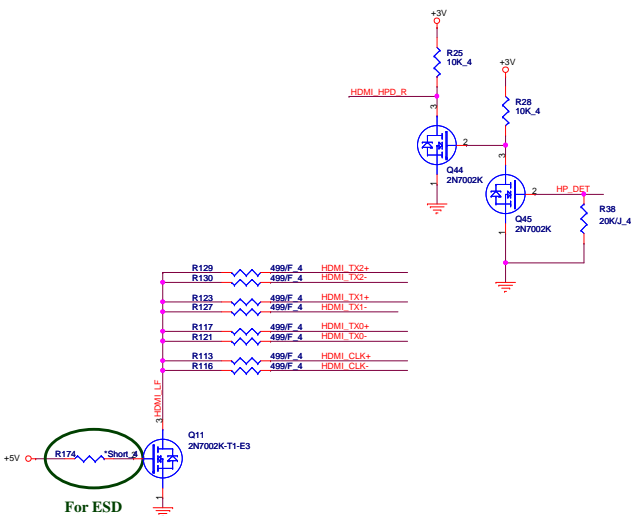


CRT SWITCH



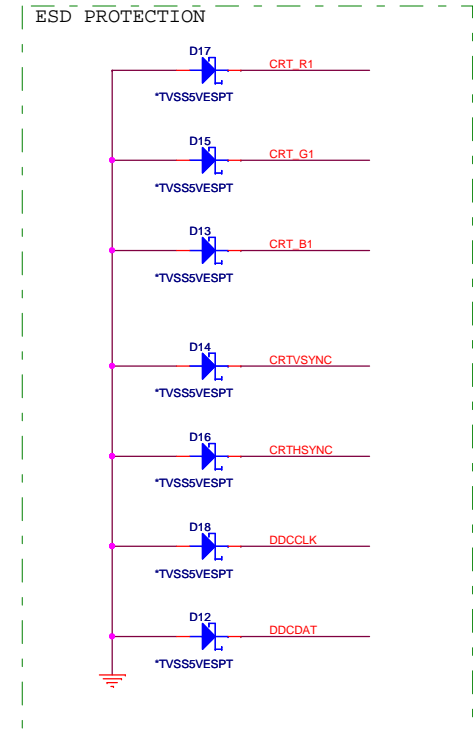
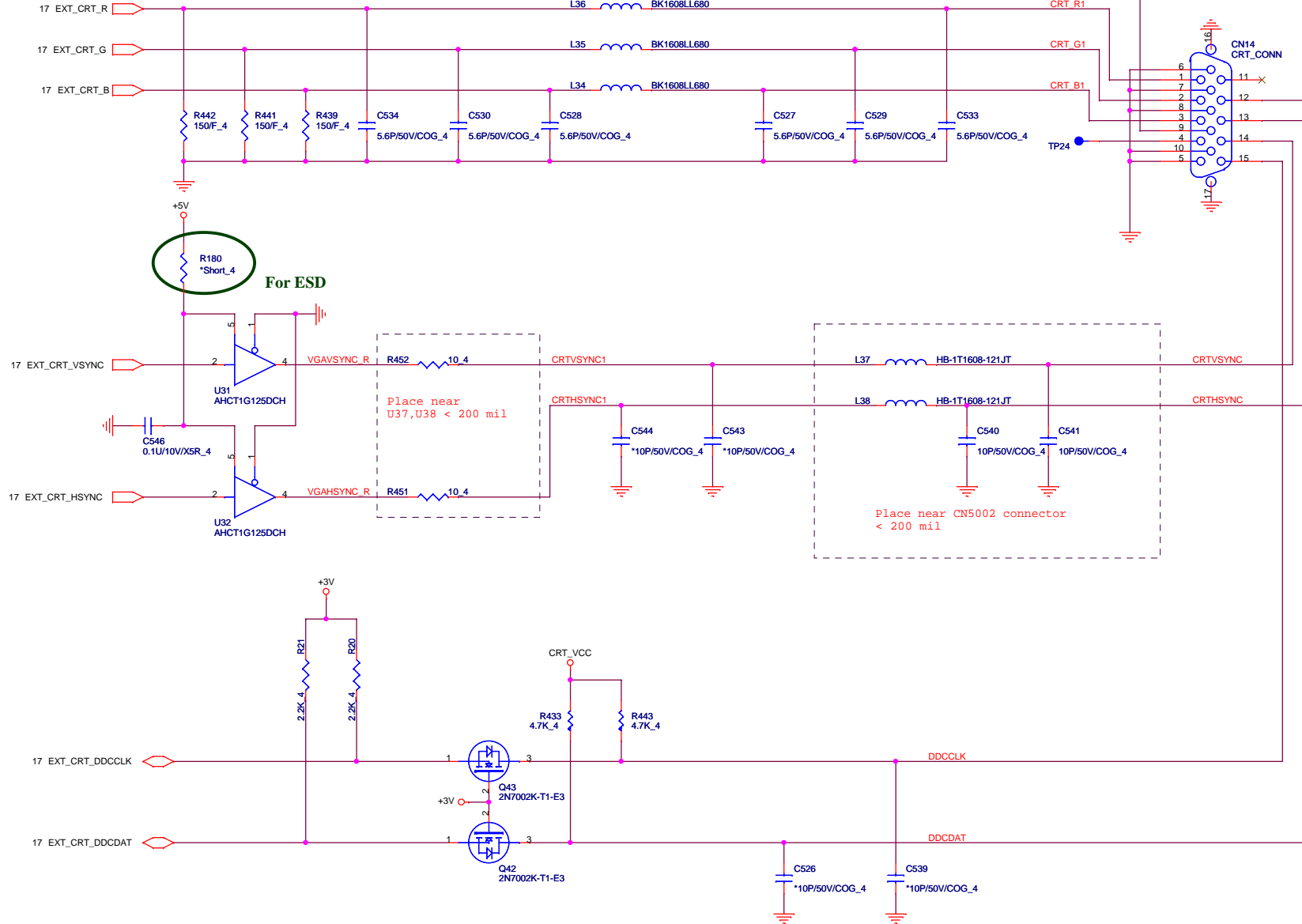


UMA Only / Muxless HDMI

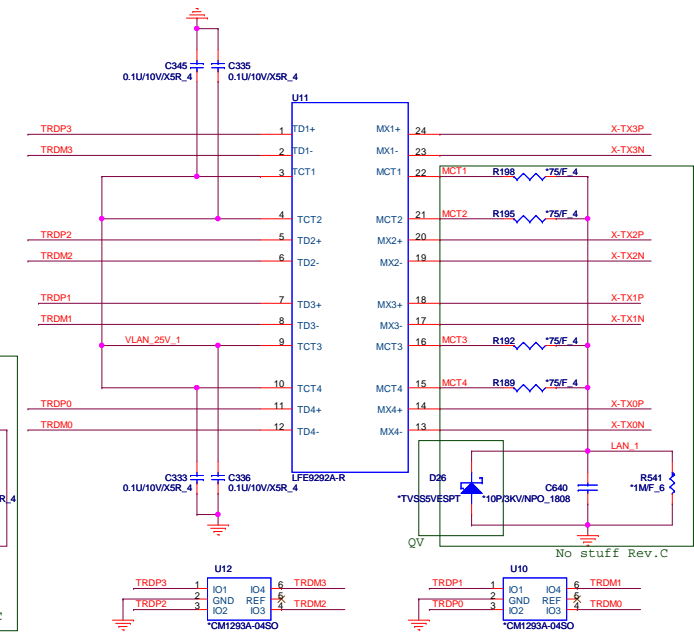
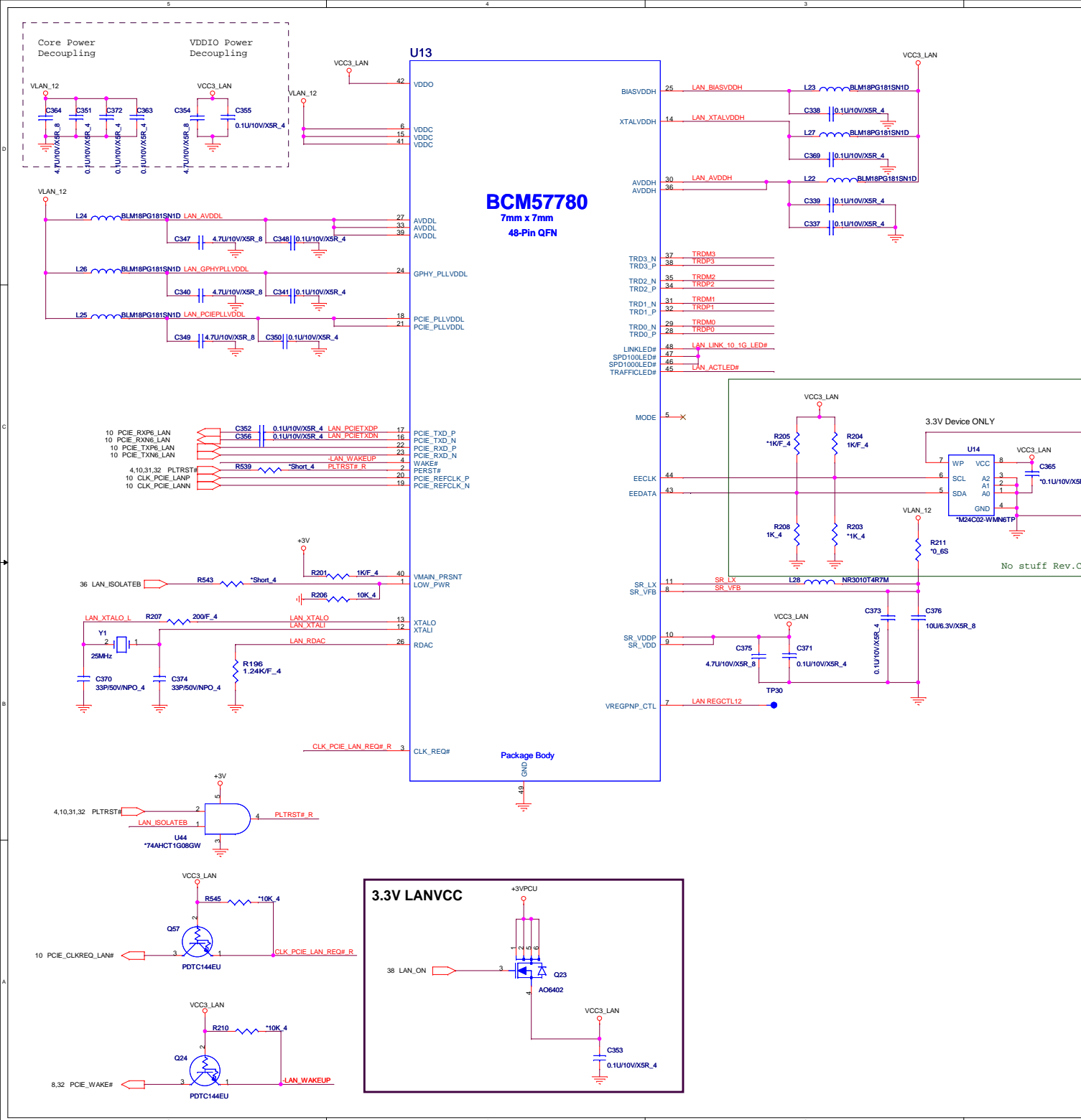




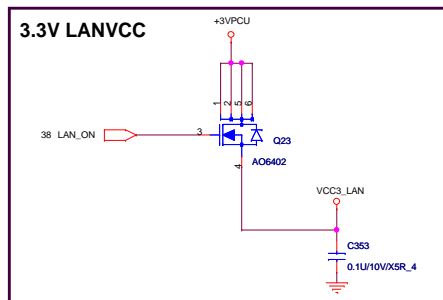
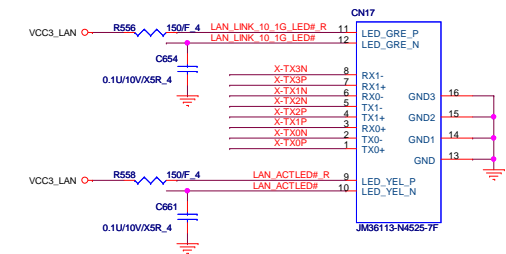
Layout Note:  
Setting R,G,B trace  
impedance to 50 ohm.



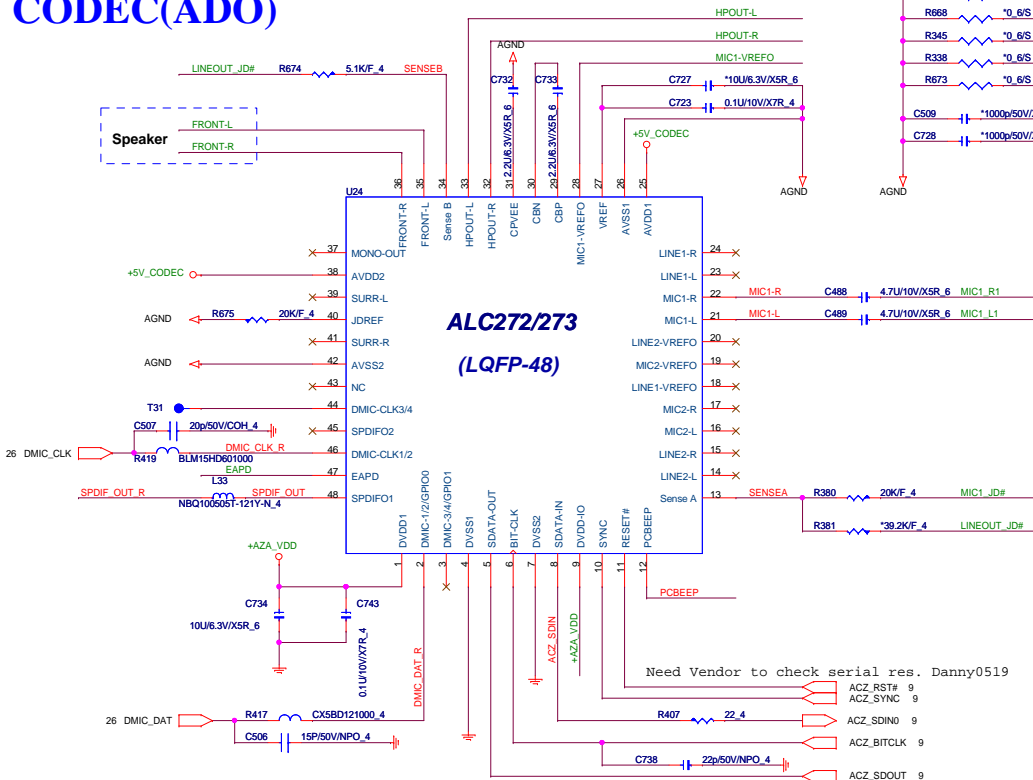




### RJ45 Connector

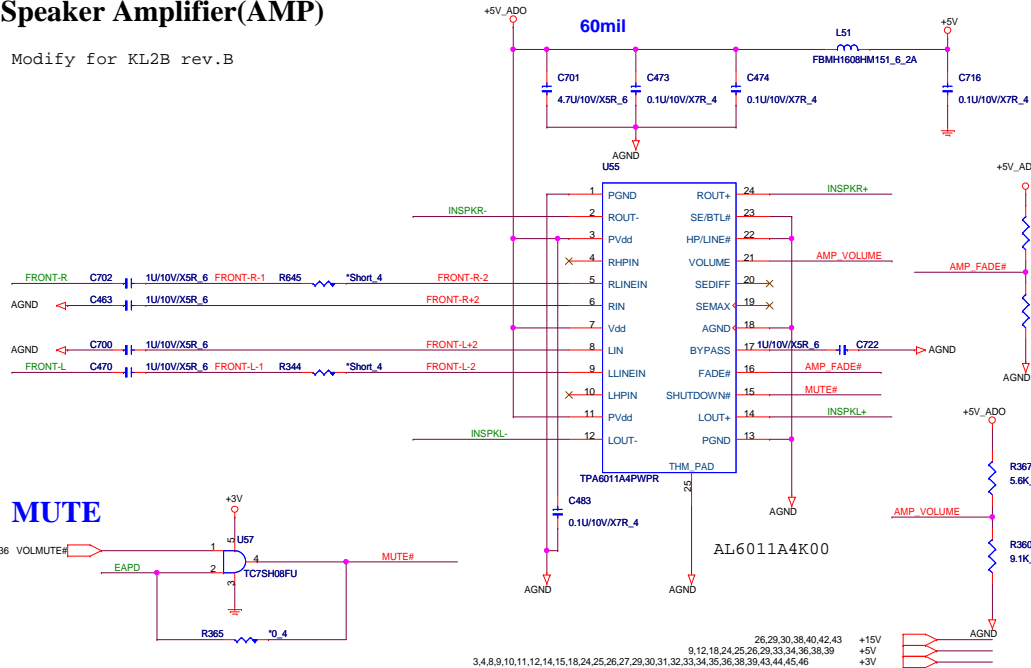


## CODEC(ADO)

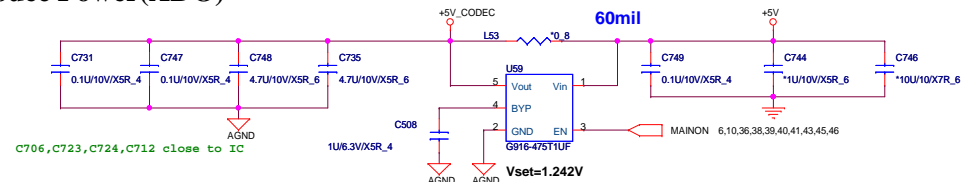


## Speaker Amplifier(AMP)

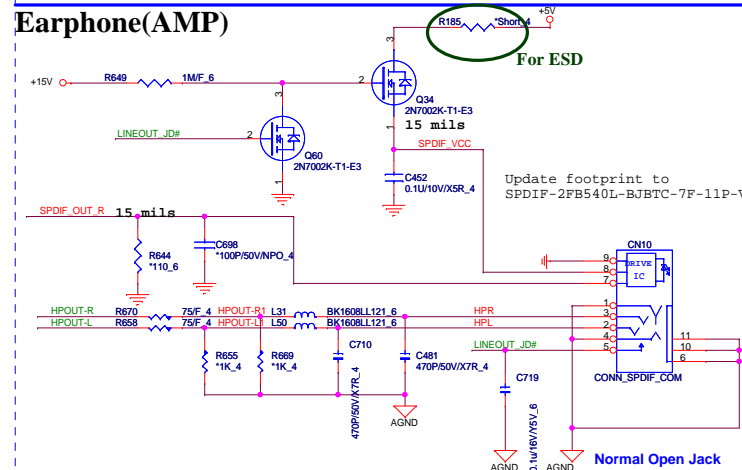
Modify for KL2B rev.B



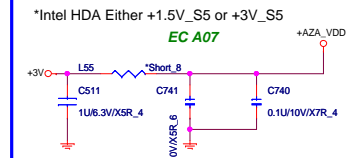
### Codec Power(ADO)



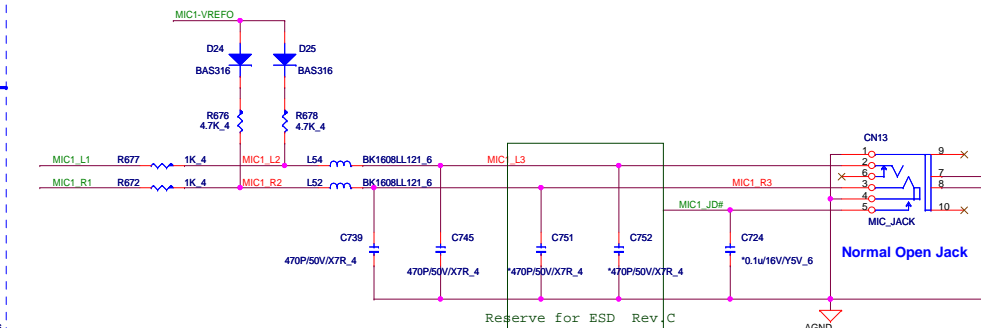
## Earphone(AMP)



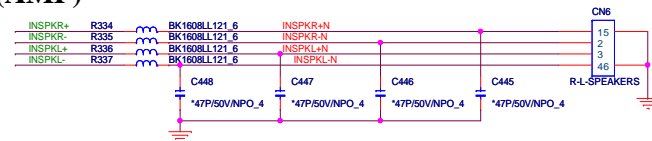
## HDA Power(ADO)



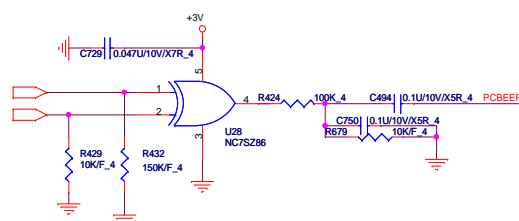
## System MIC(AMP)



## Speaker(AMP)

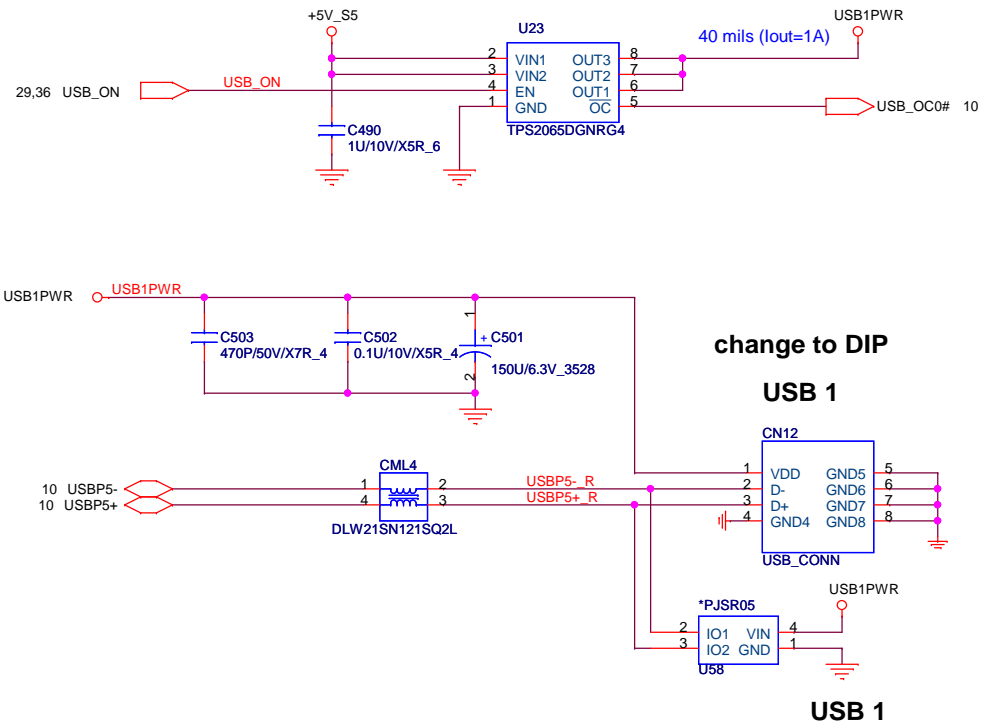


**PC BEEP**

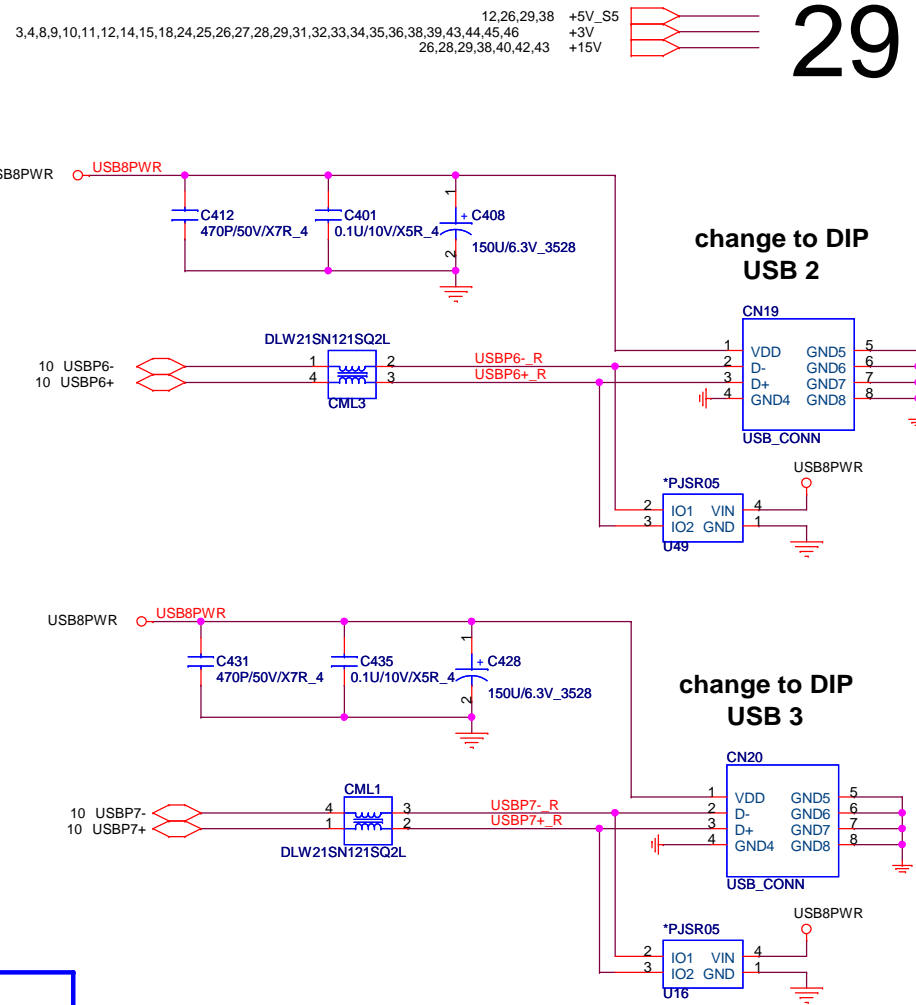
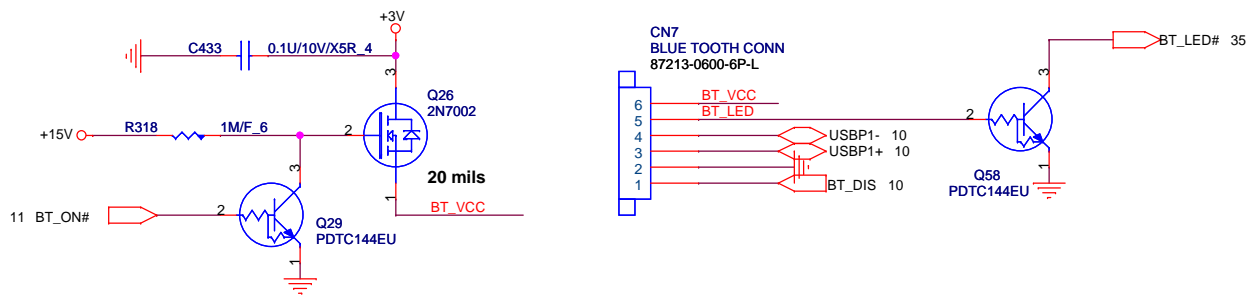


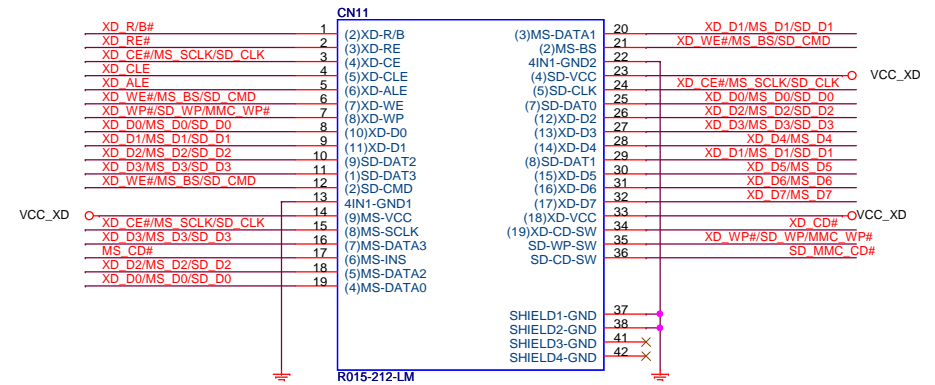


# USBX3

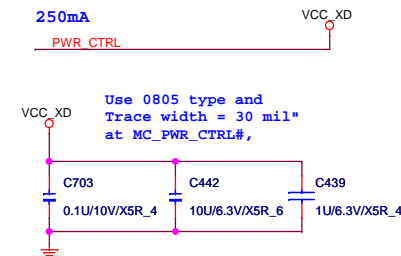


# BLUETOOTH



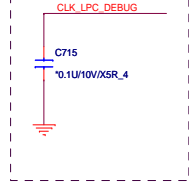


## Memory Card Power Supply

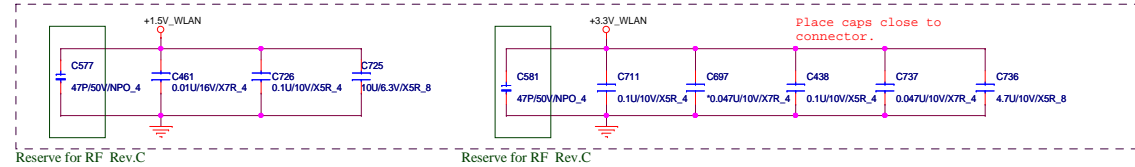
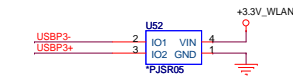
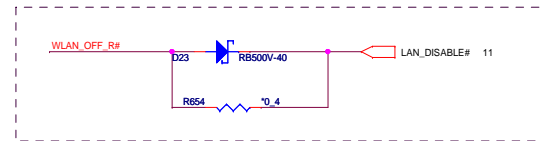
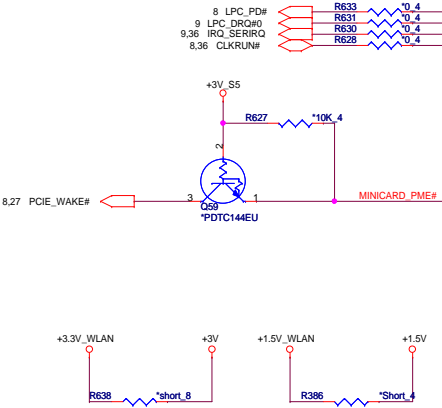


# MiniCard WLA connector

Reserved for EMI

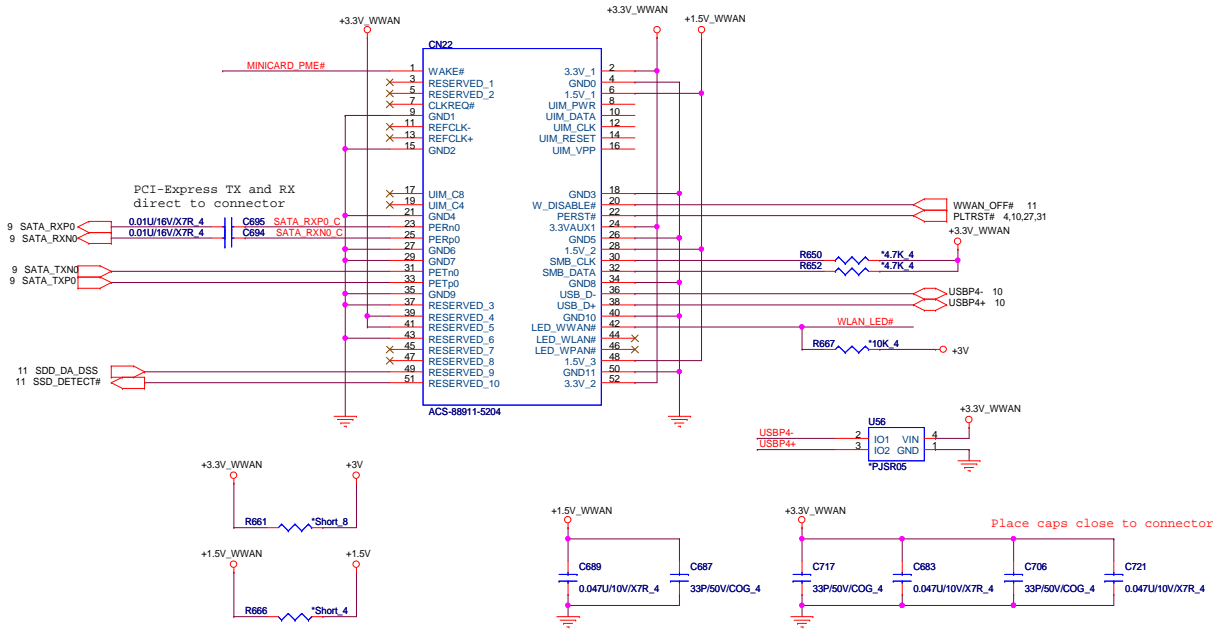


PCI-Express TX and RX direct to connector



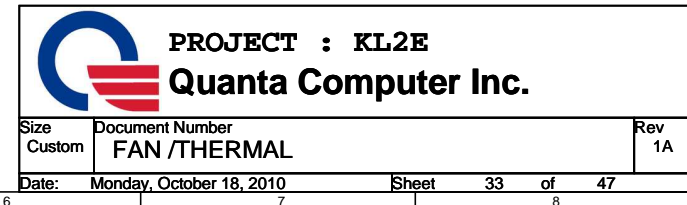
# MiniCard WWAN/SATA SSD connector

## SIM Card CONN



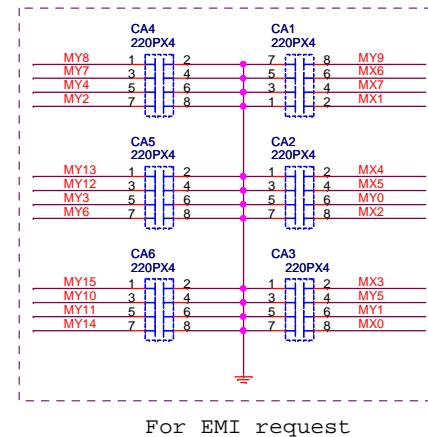
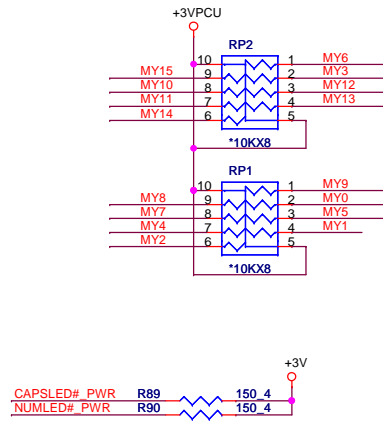
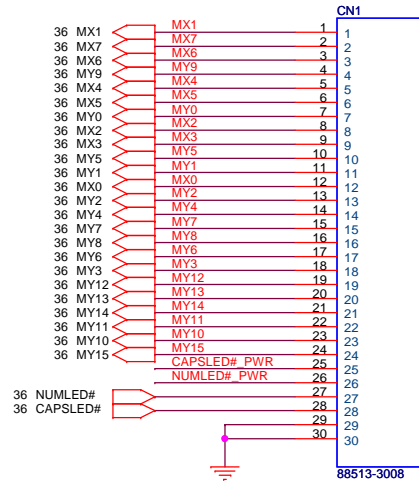


## 33



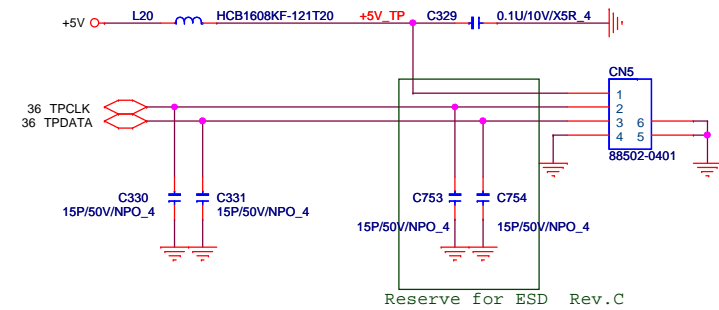
KEYBOARD

34

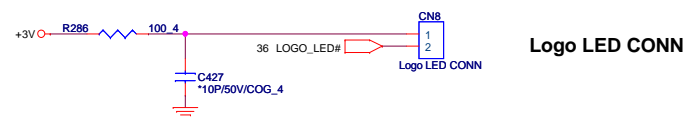
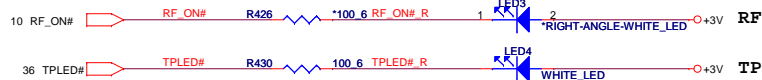
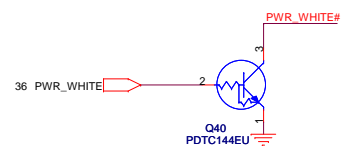
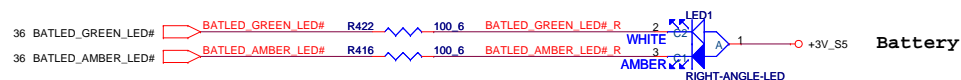
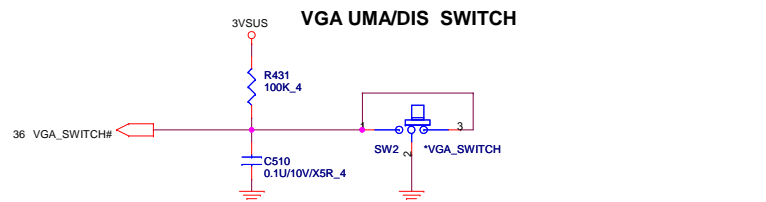


For EMI request

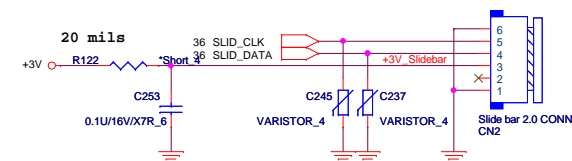
Touch pad



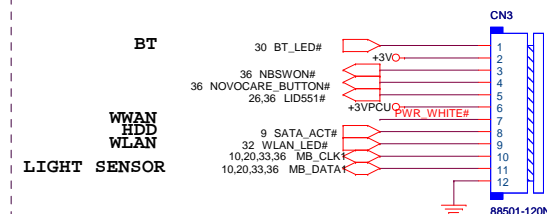
Backlight Keybaord Con.



## Slide bar 2.0



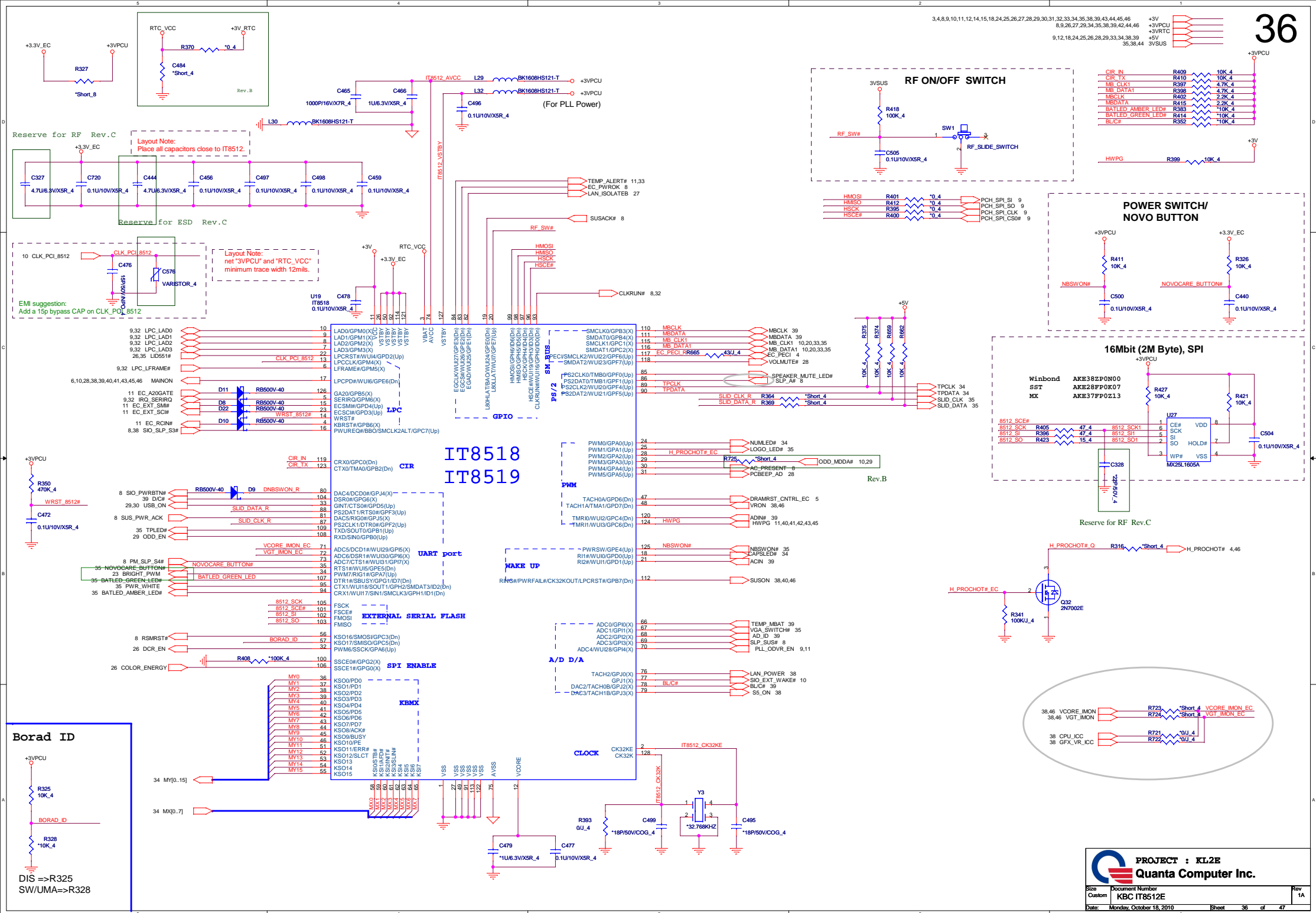
## POWER BOARD



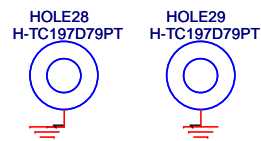
|            |      |                |
|------------|------|----------------|
| BT_LED#    | C764 | 220P/50V/X7R_4 |
| NBSWON#    | C765 | 220P/50V/X7R_4 |
| +3VPCU     | C766 | 220P/50V/X7R_4 |
| PWR_WHITE# | C767 | 220P/50V/X7R_4 |
| SATA_ACT#  | C768 | 220P/50V/X7R_4 |
| WLAN_LED#  | C769 | 220P/50V/X7R_4 |

For EMI Rev.C

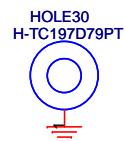
5VPCU Cable for CPU Core Power



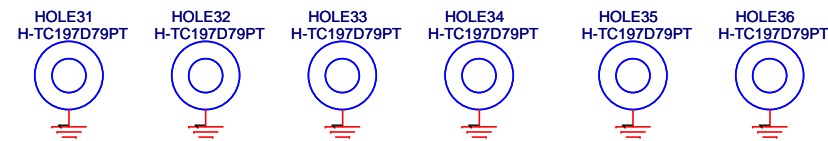
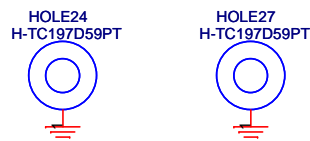
MiniCard WLAN



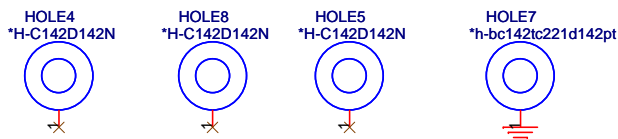
MiniCard WWAN



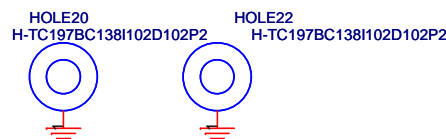
Hole for PCH support



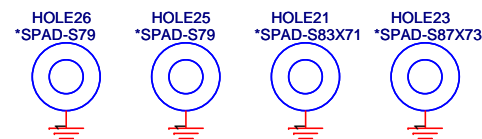
Hole for CPU support



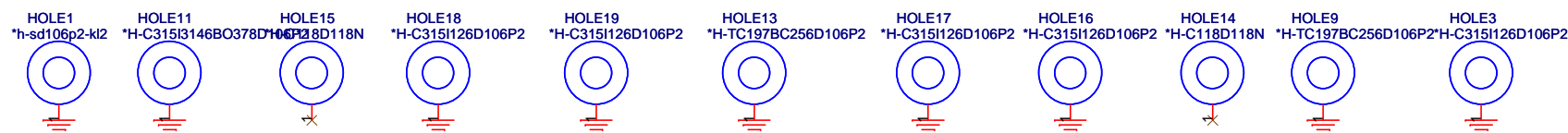
VGA nut



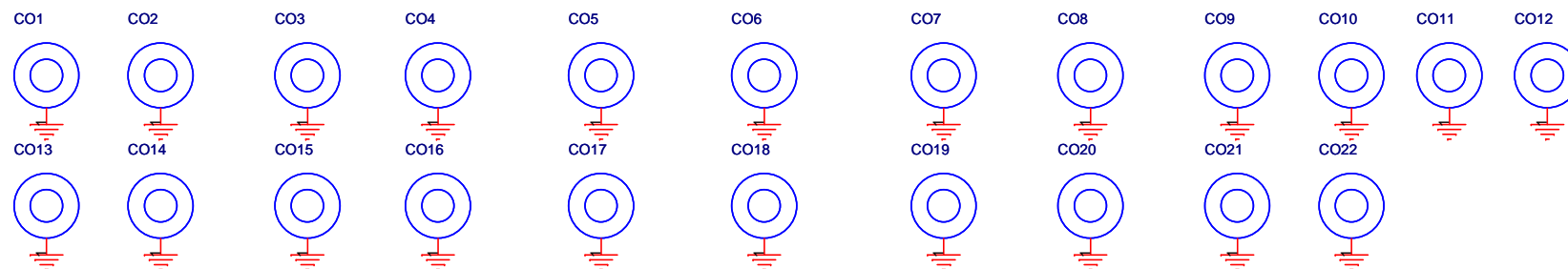
PAD



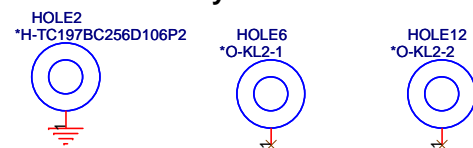
Boundary Hole



ESD Mask Copper

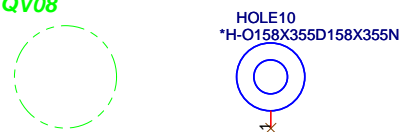



Boundary Hole

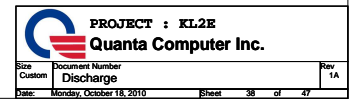


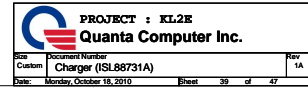
HDD PAD

EC QV08



|                                                                                       |                                |                |
|---------------------------------------------------------------------------------------|--------------------------------|----------------|
|  |                                |                |
| PROJECT : KL2E                                                                        |                                |                |
| Quanta Computer Inc.                                                                  |                                |                |
| Size<br>Custom                                                                        | Document Number<br>HOLD & SKEW | Rev<br>1A      |
| Date:                                                                                 | Monday, October 18, 2010       | Sheet 37 of 47 |



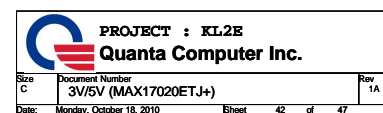


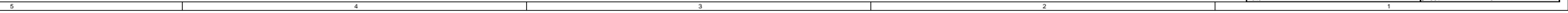


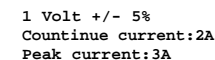
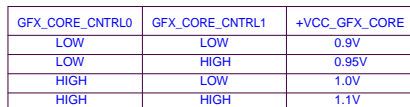
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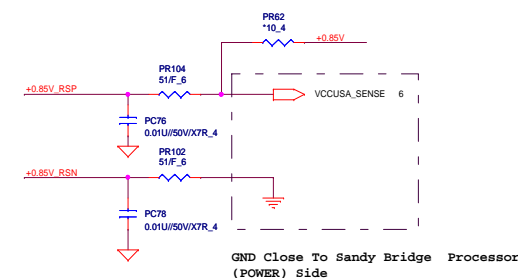
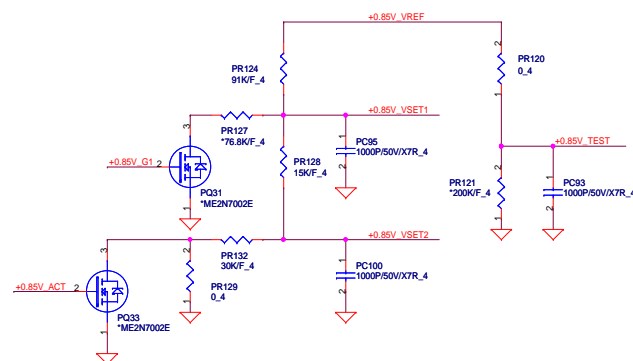
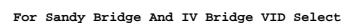
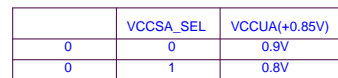


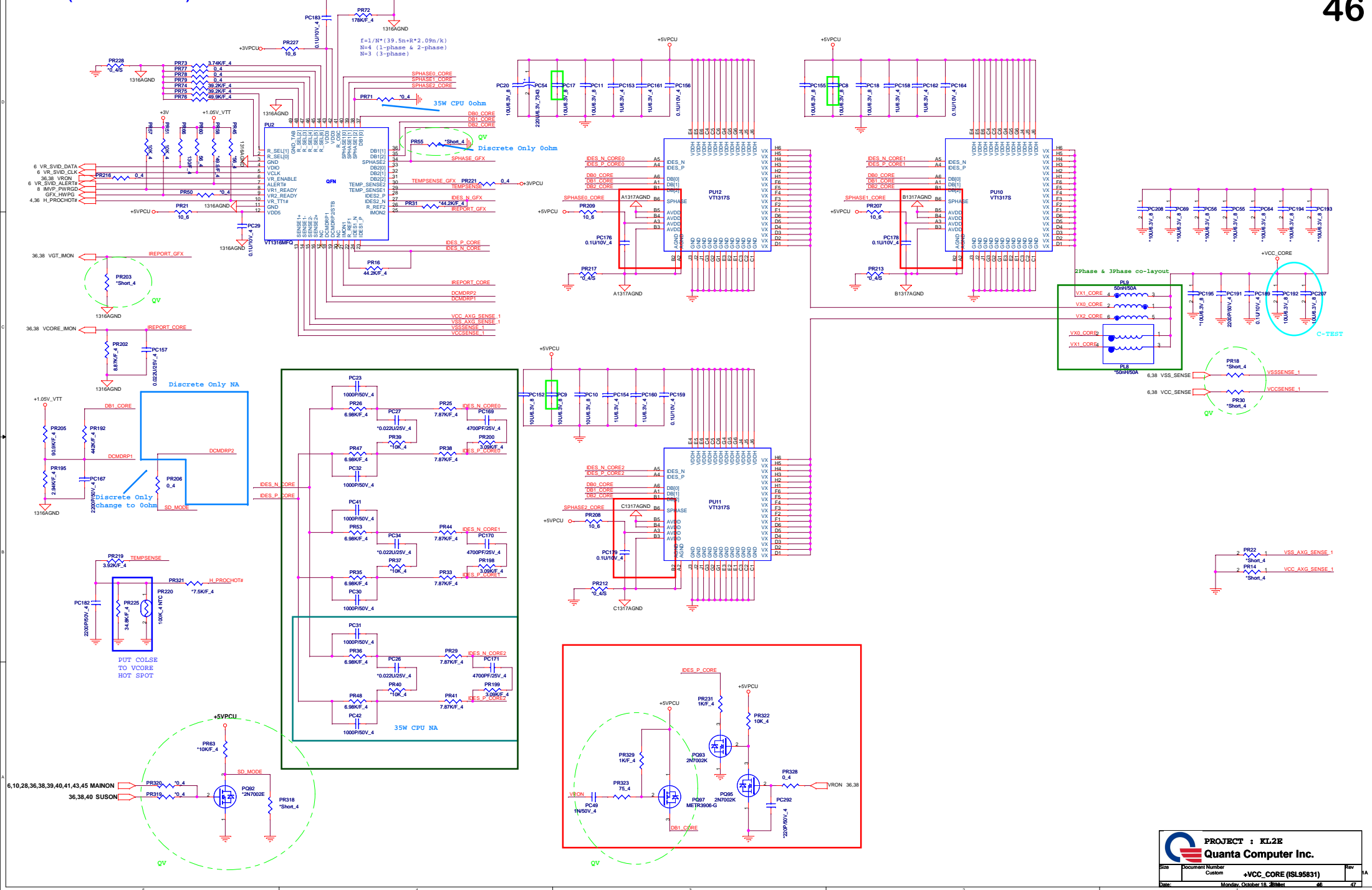












| EC # | Page | Description | Part Affected |
|------|------|-------------|---------------|
|      |      |             |               |