Compal Confidential

Gx00/Gx00 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

AMD Mars XT / SUN Pro

2013-02-27

LA-9631P

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: LA-9631P	Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 1 of 60	

Chief River

AMD MARS XT M2 128 bits / SUN PRO M2 64 bits
VRAM 512MB/1GB/2GB
MARS XT : DDR3 x 8
SUN PRO : DDR3 x 4
Page 23~32

PEG 8x
Gen2 / Gen3

Intel Processor Ivy Bridge
rPGA989
37.5mm x 37.5mm
Page 5~11

Memory Bus
Dual Channel
DDR3 1600MHz
DDR3 1333MHz
DDR3 1066MHz

204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2
Page 12, 13

FDI *8
2.7GT/s

DMI2 *4
5GT/s

LVDS Conn.
Page 33

HDMI Conn.
Page 35

CRT Conn.
Page 34

RJ45 Conn.
Page 38

LAN
PCIe Port 0
Atheros
AR8162/QCA8172(10/100)
Page 37

PCIe x1

PCIe Mini Card
WLAN
PCIe Port 1
Page 36

PCIe x1

Intel PCH
Panther Point
FCBGA 989Balls
25mm x 25mm
Page 14~22

USB30 x2

USB20 x6

Left USB3.0 x2
USB30 Port 0,1
Page 45

Right USB2.0
USB20 Port 9
Page 45

Int. Camera
USB20 Port 3
Page 33

Touch Screen
USB20 Port 2
Page 45

Card Reader
Realtek RTS5170
USB20 Port 11 page 28

SATA Gen3

HDD Conn.
SATA Port 0
Page 40

SATA

ODD Conn.
SATA Port 2
Page 40

AZALIA

Audio Codec
CONEXANT
CX20757
Page 41

Int. MIC Conn.
Page 41

Int. Speaker Conn.
Page 41

Audio Combo Jacks
HP & MIC
Page 41

SPI ROM
2MB + 4MB
Page 14

EC
ENE KB9012
Page 42

Thermal Sensor
Page 39

Touch Pad
Page 43

Int. KBD
Page 43

Sub-borad

15"
14"

Power/B
(LID)
LS9631

USB/B
LS9632

ODD/B
LS9634

IO/B
(Card Reader)
LS9633

Switch/B
(LED, LID)
LS9635

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Title: MB Block Diagram

Size: Custom | Document Number: LA-9631P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 2 of 60

Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V
R694	100K +/- 1%

Board ID / SKU ID Table for AD channel

Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0 V	0x00 – 0x0B	MP
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C – 0x1C	PVT
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D – 0x26	DVT
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 – 0x30	EVT

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

EC SM Bus2 address

Device	Address
Thermal Sensor	0100 1100

PCH SM Bus address

Device	Address	
DDR_JDIMM1	1010 000x	A0h
DDR_JDIMM2	1010 010x	A4h

AMD-GPU SM Bus address

Device	Address	
Internal thermal sensor	0100 0001	41h

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Touch Screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB Port (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

Item	BOM Structure
VIWGP (14")	14@
VIWGR (15")	15@
HDMI Logo	45@
LAN 10/100	8162@
LAN 10/100	8172@
LAN Switch mode	SWR@
LAN LDO Mode	LDO@
LAN Gas tube	GAS@
Camera	CMOS@
HDMI	HDMI@
PCH is HM76	HM76@
PCH is HM70	HM70@
PCH is NM70	NM70@
VGA is Mars XT	Mars@
VGA is Sun Pro	Sun@
For VGA	PX@
For VRAM and Strap	X76@
For UMA Strap	UMA@
Microphone	MIC@
Touch Screen	TS@
Connector	ME@
Board ID for EVT	EVT@
Board ID for DVT	DVT@
Board ID for PVT	PVT@
For USB2.0 (All PCH)	USB2@
For USB3.0 (HM76,HM70)	USB3@
For share ROM	SROM@
For non-share ROM	NOSROM@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	V +3VGS	X	X	X	X	V +3VS	V +3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
PCH_SML0CLK PCH_SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VGS	X	V +3VS	X	X	V +3VS	X

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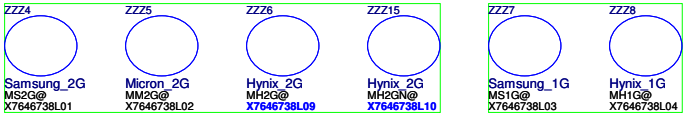
Title: Notes List

Size: B | Document Number: LA-9631P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 3 of 60

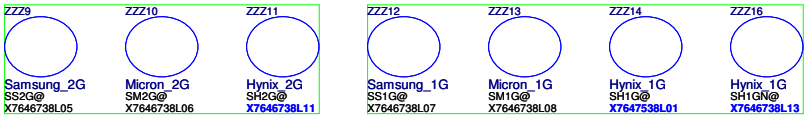
Mars XT VRAM STRAP

	X76@ Vendor UV5, UV6, UV7, UV8 UV9, UV10, UV11, UV12	ID	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV20	R_pd RV27
2GBytes	ZZZ4 MS2G@ Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	0	0	0	NC	4.75K
2GBytes	ZZZ5 MM2G@ Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	0	0	1	8.45K	2K
2GBytes	ZZZ6 MH2G@ Hynix 2048Mbits SA000065300 128M16 H5TQ2G63DFR-N0C	2	0	1	0	4.53K	2K
1GBytes	ZZZ7 MS1G@ Samsung 1028Mbits SA00004GS00 64Mx16 K4W1G1646G-BC11	3	0	1	1	6.98K	4.99K
2GBytes	ZZZ15 MH2GN@ Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	4	1	0	0	4.53K	4.99K
1GBytes	ZZZ8 MH1G@ Hynix 1024Mbits SA000041SB0 64Mx16 H5TQ1G63EFR-11C	7	1	1	1	4.75K	NC



Sun PRO VRAM STRAP

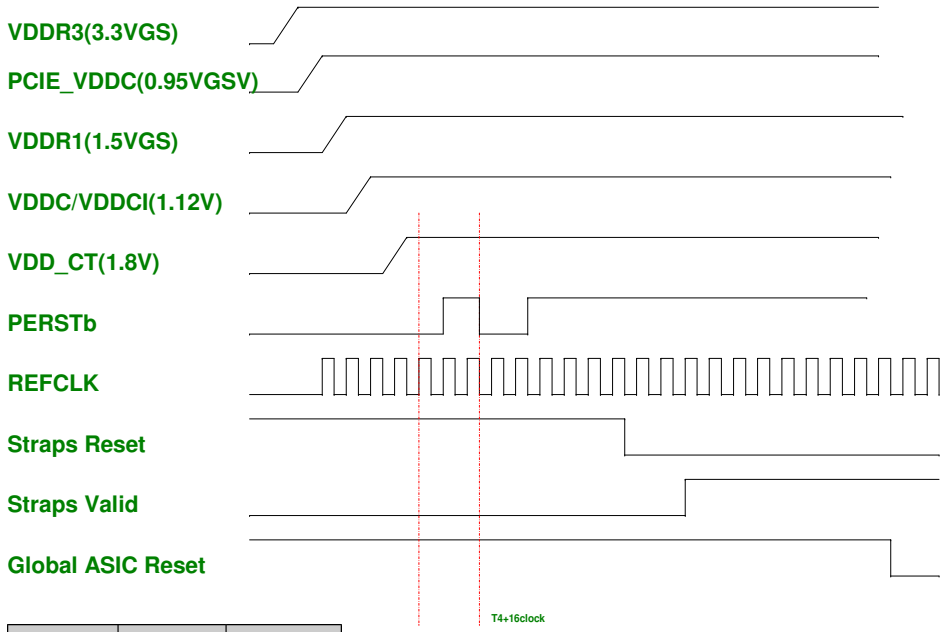
	X76@ Vendor UV9, UV10, UV11, UV12	ID	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV20	R_pd RV27
2GBytes	ZZZ9 SS2G@ Samsung 4096Mbits SA000068R00 256Mx16 K4W4G1646B-HC11	0	0	0	0	NC	4.75K
2GBytes	ZZZ10 SM2G@ Micron 4096Mbits SA000065D00 256Mx16/1866 MT41K256M16HA-107G:E	1	0	0	1	8.45K	2K
2GBytes	ZZZ11 SH2G@ Hynix 4096Mbits SA00006DG00 256MX16 H5TQ4G63MFR-11C	2	0	1	0	4.53K	2K
1GBytes	ZZZ12 SS1G@ Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	3	0	1	1	6.98K	4.99K
1GBytes	ZZZ16 SH1GN@ Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	4	1	0	0	4.53K	4.99K
1GBytes	ZZZ13 SM1G@ Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	6	1	1	0	3.4K	10K
1GBytes	ZZZ14 SH1G@ Hynix 2048Mbits SA000065300 128M16 H5TQ2G63DFR-N0C	7	1	1	1	4.75K	NC



Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

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Issued Date	2011/06/15	Deciphered Date 2012/07/11	Title: VGA Notes List
Size: Custom	Document Number: LA-9631P		Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 4 of 60		

ZZZ1 14@

14" DIS PCB LA9631P
DA6000WC000
PCB 0N1 LA-9631P REV0 M/B DIS 3

ZZZ2 15@

15" DIS PCB LA9631P
DA6000WC100
PCB 0N2 LA-9631P REV0 M/B DIS 5

PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils
- typical impedance = 14.5 mohms

+V1.05S_VCCP
R1
24.9_0402_1%
PEG_COMP

PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

JCPU1A

DMI
<16> DMI_CRX_PTX_N0 B27 DMI_RX#[0]
<16> DMI_CRX_PTX_N1 B25 DMI_RX#[1]
<16> DMI_CRX_PTX_N2 A25 DMI_RX#[2]
<16> DMI_CRX_PTX_N3 B24 DMI_RX#[3]
<16> DMI_CRX_PTX_P0 B28 DMI_RX[0]
<16> DMI_CRX_PTX_P1 B26 DMI_RX[1]
<16> DMI_CRX_PTX_P2 A24 DMI_RX[2]
<16> DMI_CRX_PTX_P3 B23 DMI_RX[3]
<16> DMI_CTX_PRX_N0 G21 DMI_TX#[0]
<16> DMI_CTX_PRX_N1 E22 DMI_TX#[1]
<16> DMI_CTX_PRX_N2 F21 DMI_TX#[2]
<16> DMI_CTX_PRX_N3 D21 DMI_TX#[3]
<16> DMI_CTX_PRX_P0 G22 DMI_TX[0]
<16> DMI_CTX_PRX_P1 D22 DMI_TX[1]
<16> DMI_CTX_PRX_P2 F20 DMI_TX[2]
<16> DMI_CTX_PRX_P3 C21 DMI_TX[3]

Intel(R) FDI
<16> FDI_CTX_PRX_N0 A21 FDI0_TX#[0]
<16> FDI_CTX_PRX_N1 H19 FDI0_TX#[1]
<16> FDI_CTX_PRX_N2 E19 FDI0_TX#[2]
<16> FDI_CTX_PRX_N3 F18 FDI0_TX#[3]
<16> FDI_CTX_PRX_N4 B21 FDI1_TX#[0]
<16> FDI_CTX_PRX_N5 C20 FDI1_TX#[1]
<16> FDI_CTX_PRX_N6 D18 FDI1_TX#[2]
<16> FDI_CTX_PRX_N7 E17 FDI1_TX#[3]
<16> FDI_CTX_PRX_P0 A22 FDI0_TX[0]
<16> FDI_CTX_PRX_P1 G19 FDI0_TX[1]
<16> FDI_CTX_PRX_P2 E20 FDI0_TX[2]
<16> FDI_CTX_PRX_P3 G18 FDI0_TX[3]
<16> FDI_CTX_PRX_P4 B20 FDI1_TX[0]
<16> FDI_CTX_PRX_P5 C19 FDI1_TX[1]
<16> FDI_CTX_PRX_P6 D19 FDI1_TX[2]
<16> FDI_CTX_PRX_P7 F17 FDI1_TX[3]
<16> FDI_FSYNC0 J18 FDI0_FSYNC
<16> FDI_FSYNC1 J17 FDI1_FSYNC
<16> FDI_INT H20 FDI_INT
<16> FDI_LSYNC0 J19 FDI0_LSYNC
<16> FDI_LSYNC1 H17 FDI1_LSYNC

+V1.05S_VCCP
R7
24.9_0402_1%
EDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

eDP
EDP_COMP A18 eDP_COMPIO
A17 eDP_ICOMPO
eDP_HPD B16 eDP_HPD#
C15 eDP_AUX
D15 eDP_AUX#
C17 eDP_TX[0]
F16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
F15 eDP_TX#[3]

PCI EXPRESS* - GRAPHICS
PEG_ICOMPI J22
PEG_ICOMPO J21
PEG_RCOMPO H22
PEG_RX#[0] K33
PEG_RX#[1] M35
PEG_RX#[2] L34
PEG_RX#[3] J35
PEG_RX#[4] J32
PEG_RX#[5] H34
PEG_RX#[6] H31
PEG_RX#[7] G33
PEG_RX#[8] G30 PCIE_CRX_GTX_N7
PEG_RX#[9] F35 PCIE_CRX_GTX_N6
PEG_RX#[10] E34 PCIE_CRX_GTX_N5
PEG_RX#[11] E32 PCIE_CRX_GTX_N4
PEG_RX#[12] D33 PCIE_CRX_GTX_N3
PEG_RX#[13] D31 PCIE_CRX_GTX_N2
PEG_RX#[14] B33 PCIE_CRX_GTX_N1
PEG_RX#[15] C32 PCIE_CRX_GTX_N0 → PCIE_CRX_GTX_N[0..7] <23>
PEG_RX[0] J33
PEG_RX[1] L35
PEG_RX[2] K34
PEG_RX[3] H35
PEG_RX[4] H32
PEG_RX[5] G34
PEG_RX[6] G31
PEG_RX[7] F33
PEG_RX[8] F30 PCIE_CRX_GTX_P7
PEG_RX[9] E35 PCIE_CRX_GTX_P6
PEG_RX[10] E33 PCIE_CRX_GTX_P5
PEG_RX[11] F32 PCIE_CRX_GTX_P4
PEG_RX[12] D34 PCIE_CRX_GTX_P3
PEG_RX[13] E31 PCIE_CRX_GTX_P2
PEG_RX[14] C33 PCIE_CRX_GTX_P1
PEG_RX[15] B32 PCIE_CRX_GTX_P0 → PCIE_CRX_GTX_P[0..7] <23>
PEG_TX#[0] M29
PEG_TX#[1] M32
PEG_TX#[2] M31
PEG_TX#[3] L32
PEG_TX#[4] L29
PEG_TX#[5] K31
PEG_TX#[6] K28
PEG_TX#[7] J30
PEG_TX#[8] J28 PCIE_CTX_GRX_C_N7 C9 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_N7
PEG_TX#[9] H29 PCIE_CTX_GRX_C_N6 C10 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_N6
PEG_TX#[10] G27 PCIE_CTX_GRX_C_N5 C11 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_N5
PEG_TX#[11] E29 PCIE_CTX_GRX_C_N4 C12 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_N4
PEG_TX#[12] F27 PCIE_CTX_GRX_C_N3 C13 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_N3
PEG_TX#[13] D28 PCIE_CTX_GRX_C_N2 C14 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_N2
PEG_TX#[14] F26 PCIE_CTX_GRX_C_N1 C15 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_N1
PEG_TX#[15] E25 PCIE_CTX_GRX_C_N0 C16 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_N0 → PCIE_CTX_GRX_N[0..7] <23>
PEG_TX[0] M28
PEG_TX[1] M33
PEG_TX[2] M30
PEG_TX[3] L31
PEG_TX[4] L28
PEG_TX[5] K30
PEG_TX[6] K27
PEG_TX[7] J29
PEG_TX[8] J27 PCIE_CTX_GRX_C_P7 C25 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_P7
PEG_TX[9] H28 PCIE_CTX_GRX_C_P6 C26 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_P6
PEG_TX[10] G28 PCIE_CTX_GRX_C_P5 C27 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_P5
PEG_TX[11] E28 PCIE_CTX_GRX_C_P4 C28 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_P4
PEG_TX[12] F28 PCIE_CTX_GRX_C_P3 C29 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_P3
PEG_TX[13] D27 PCIE_CTX_GRX_C_P2 C30 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_P2
PEG_TX[14] E26 PCIE_CTX_GRX_C_P1 C31 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_P1
PEG_TX[15] D25 PCIE_CTX_GRX_C_P0 C32 PX@ 1 2 0.22U 0402 10V6K PCIE_CTX_GRX_P0 → PCIE_CTX_GRX_P[0..15] <23>

TYCO_2013620-2_IVY BRIDGE
ME@

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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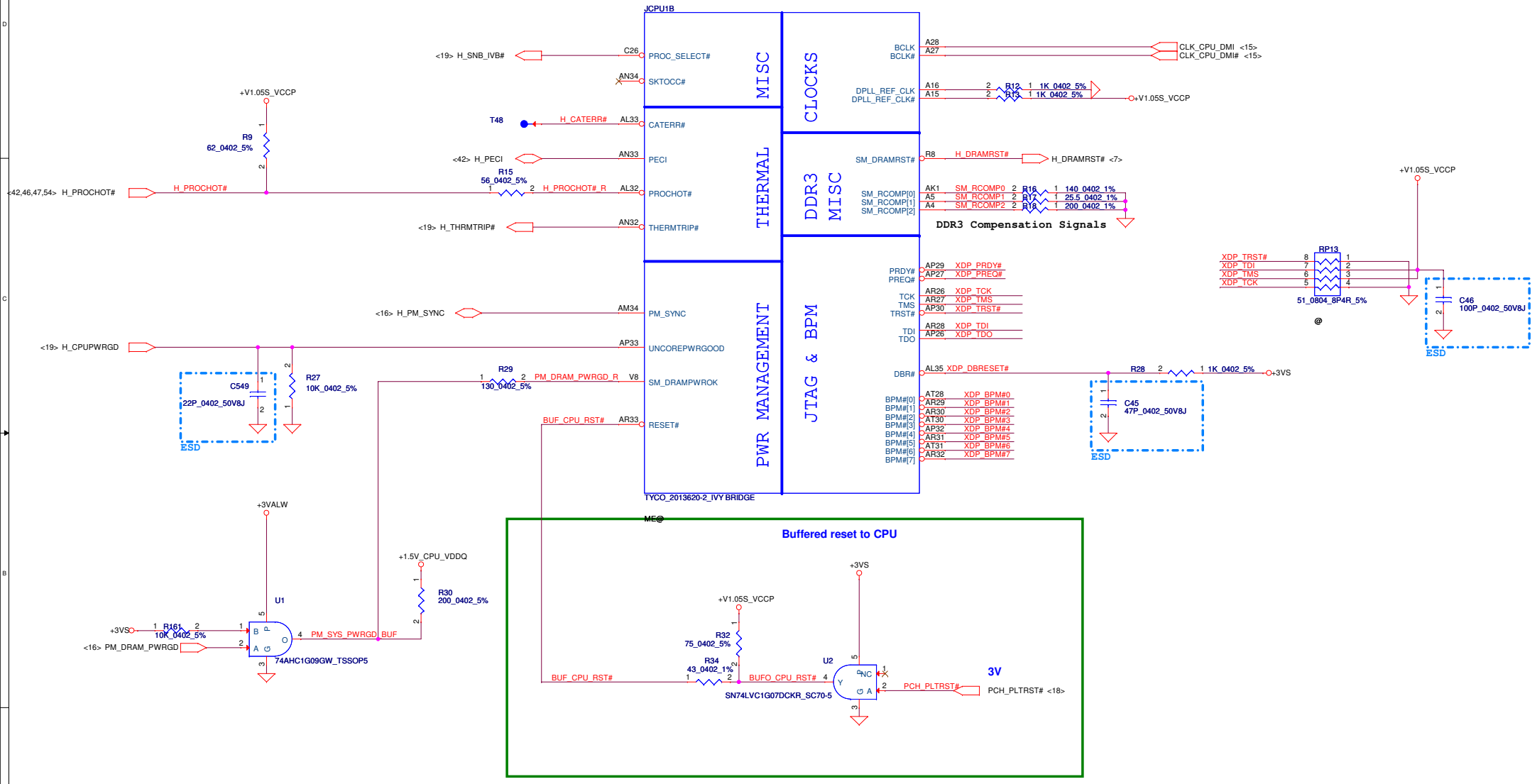
Custom	LA-9631P	1.0

Date: Wednesday, February 27, 2013 Sheet 5 of 60



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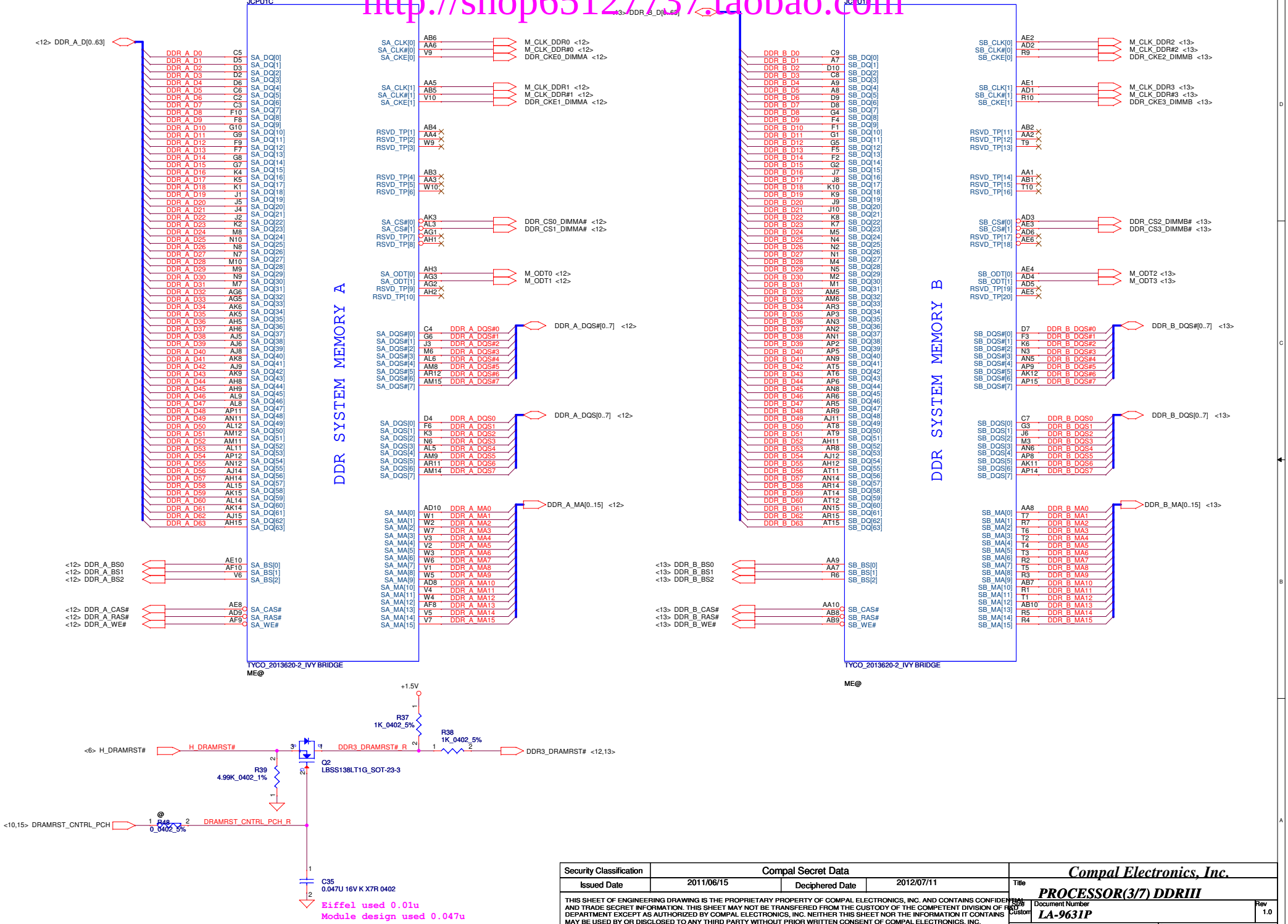
Compal Electronics, Inc.			
Title: PROCESSOR(2/7) PM,XDP,CLK			
Size: Custom	Document Number: LA-9631P		Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 6 of 60		



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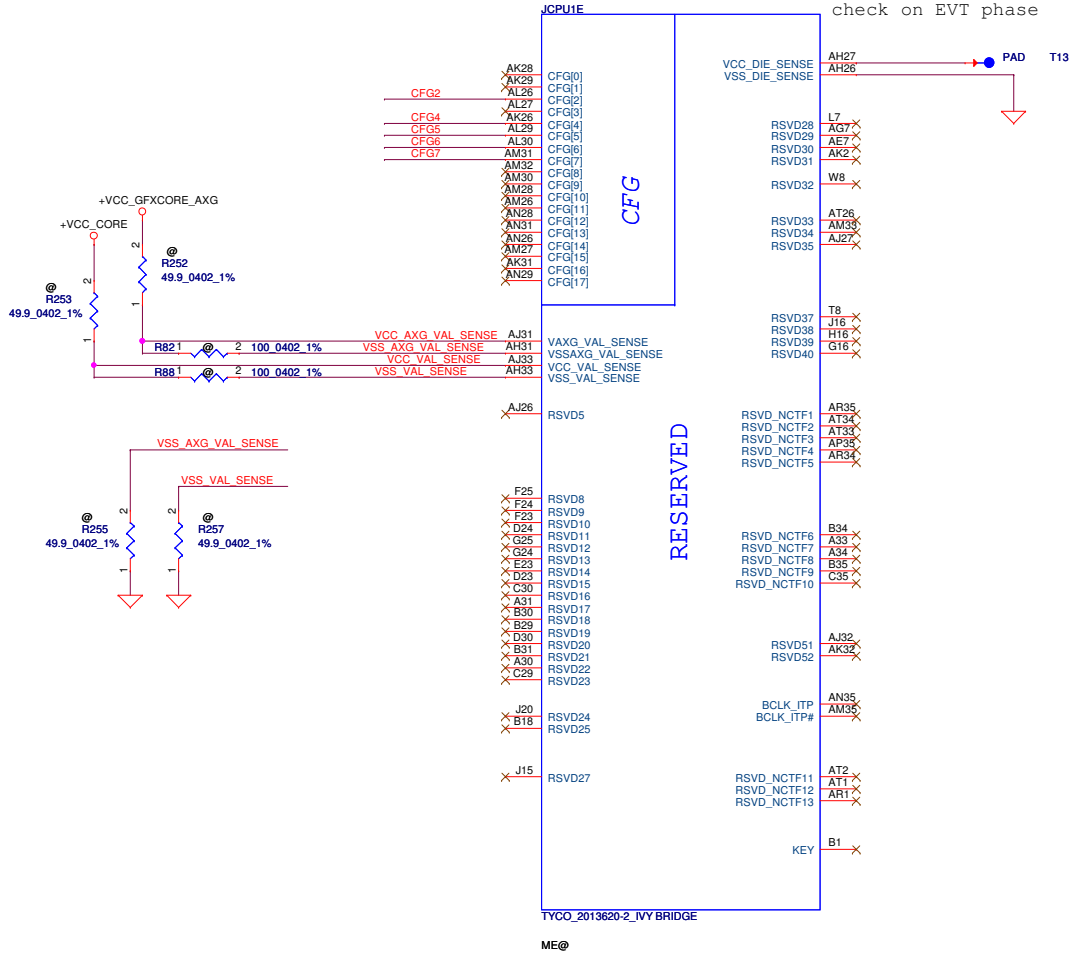
Title: PROCESSOR(3/7) DDRIII

Size: Custom | Document Number: LA-9631P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 7 of 60

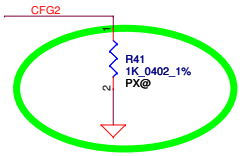
CFG Straps for Processor

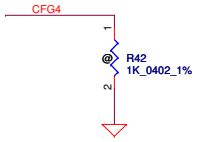
Interl request AH26 short GND
check on EVT phase



PEG Static Lane Reversal – CFG2 is for the 16x

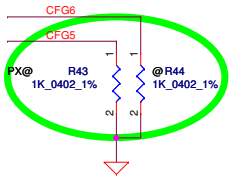
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed





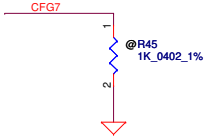
Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps

CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled *10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: LA-9631P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 8 of 60

POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

+V1.05S_VCCP

8.5A

CORE SUPPLY

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

PEG AND DDR

AH13	VCCIO1
AH10	VCCIO2
AG10	VCCIO3
AC10	VCCIO4
Y10	VCCIO5
U10	VCCIO6
P10	VCCIO7
L10	VCCIO8
J14	VCCIO9
J13	VCCIO10
J12	VCCIO11
J11	VCCIO12
H14	VCCIO13
H12	VCCIO14
H11	VCCIO15
G14	VCCIO16
G13	VCCIO17
G12	VCCIO18
F14	VCCIO19
F13	VCCIO20
F12	VCCIO21
F11	VCCIO22
E14	VCCIO23
E12	VCCIO24
E11	VCCIO25
D14	VCCIO26
D13	VCCIO27
D12	VCCIO28
D11	VCCIO29
C14	VCCIO30
C13	VCCIO31
C12	VCCIO32
C11	VCCIO33
B14	VCCIO34
B12	VCCIO35
A14	VCCIO36
A13	VCCIO37
A12	VCCIO38
A11	VCCIO39
J23	VCCIO40

SVID

+V1.05S_VCCP

R46 75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT#	AJ29	H_CPU_SVIDALRT#	R47 43_0402_5%	VR_SVID_ALRT# <54>
VIDSCLK	AJ30			VR_SVID_CLK <54>
VIDSOUT	AJ28			VR_SVID_DAT <54>

R50 130_0402_5% +V1.05S_VCCP 0.1uF on power side

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

SENSE LINES

+VCC_CORE

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

R51 100_0402_1%

VCC_SENSE	AJ35		VCCSENSE <54>
VSS_SENSE	AJ34		VSSSENSE <54>

R54 100_0402_1%

VCCIO_SENSE	B10		R74 10_0402_1%	VCCIO_SENSE <52>
VSS_SENSE_VCCIO	A10	VSSIO_SENSE_L	2VSSIO_SENSE	

R74 & R79 put together

R79 10_0402_1% +V1.05S_VCCP

VSSIO_SENSE_L <52>

VSS_SENCE 100ohm +-1% pull-down to GND near processor

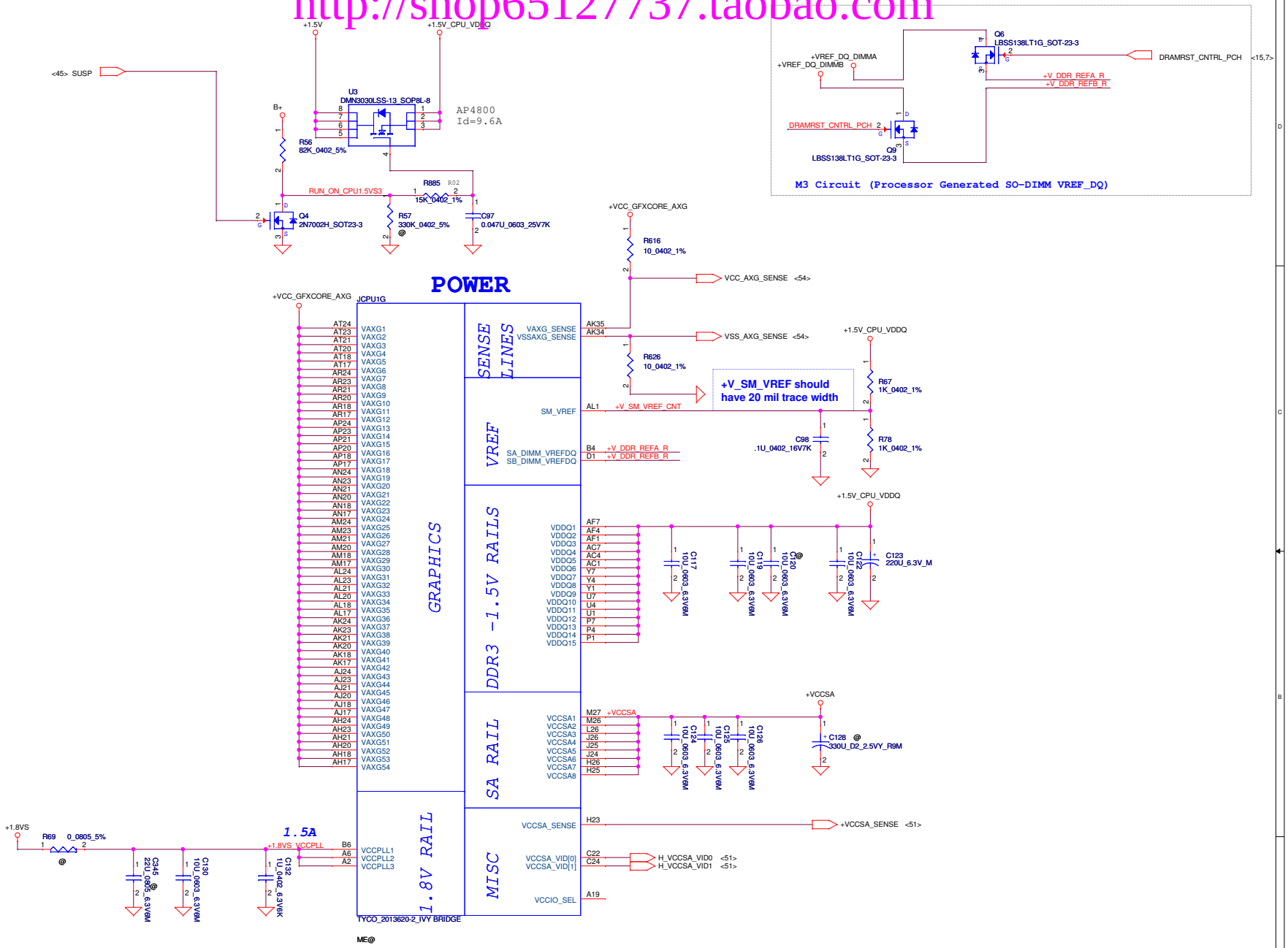
TYCO_2013620-2_IVY BRIDGE

ME@

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

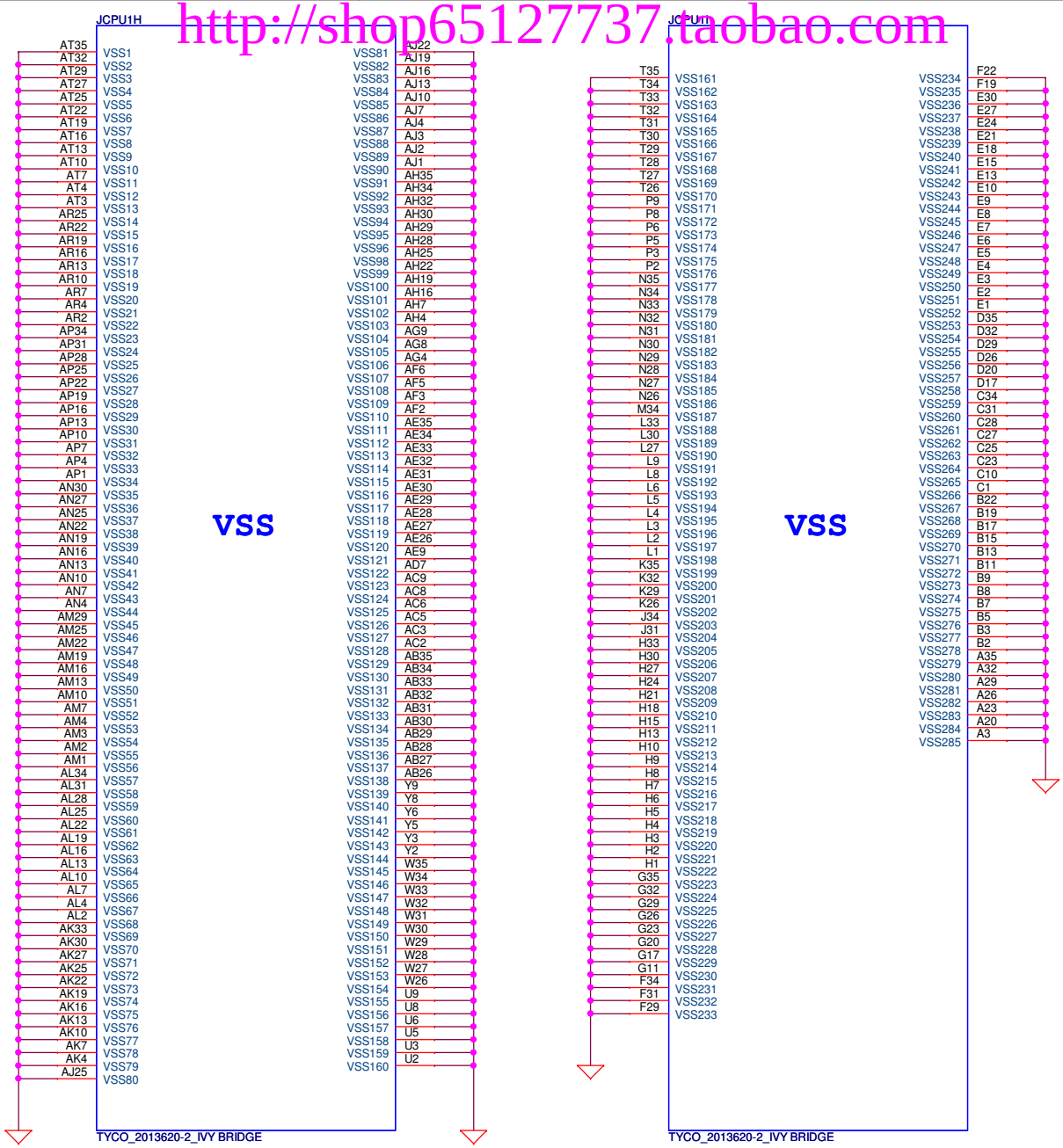
Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom	Document Number: LA-9631P	Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 9 of 60	



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	PROCESSOR(6/7) PWR		
Size: Custom	Document Number: LA-9631P		Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 10 of 60		



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	LA-9631P	1.0

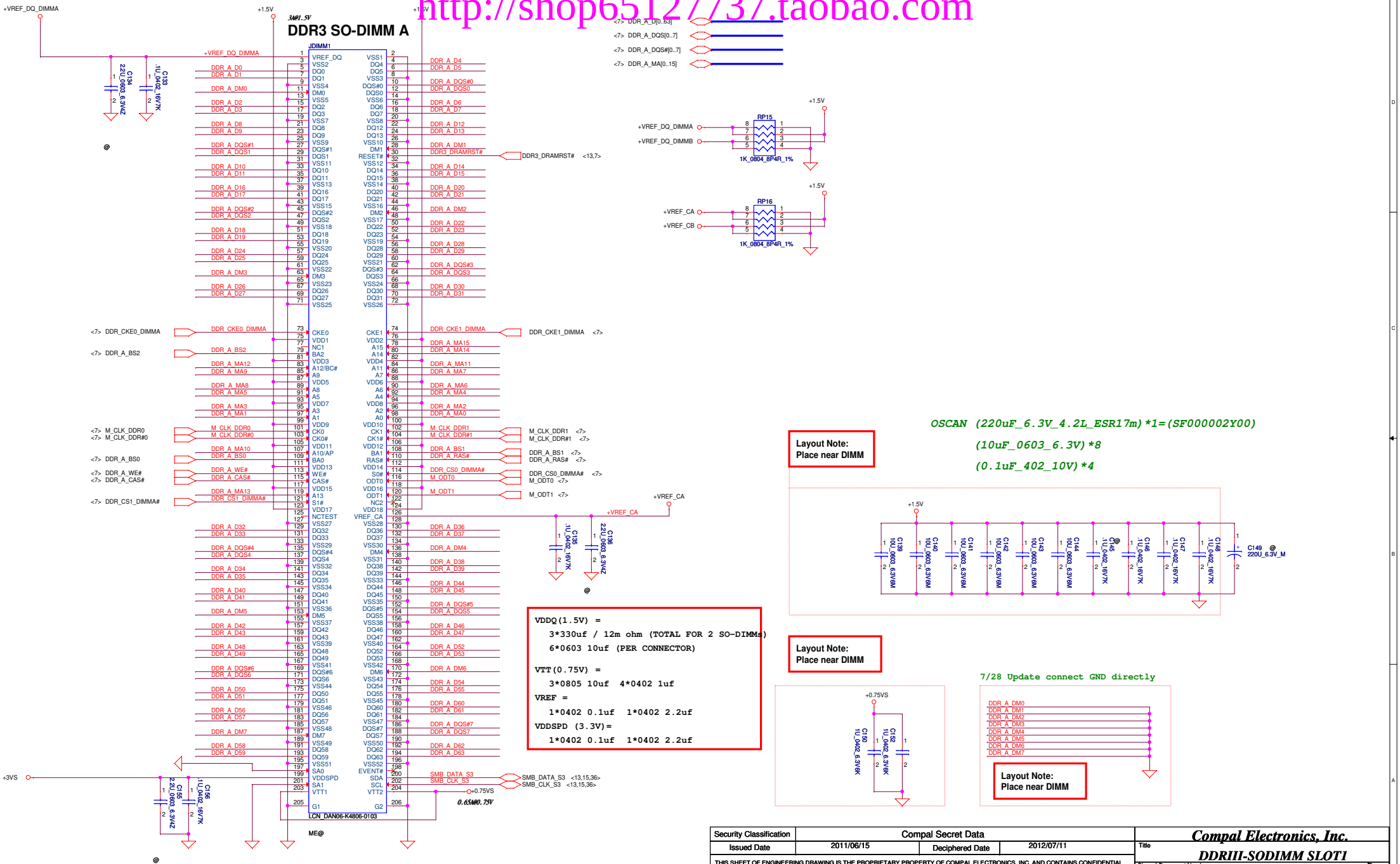
Date: Wednesday, February 27, 2013 Sheet 11 of 60

DDR3 SO-DIMM A

JDIMM1

LCN_DAN06-K4806-0103

ME@



VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

Layout Note:
Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM

7/28 Update connect GND directly

Layout Note:
Place near DIMM

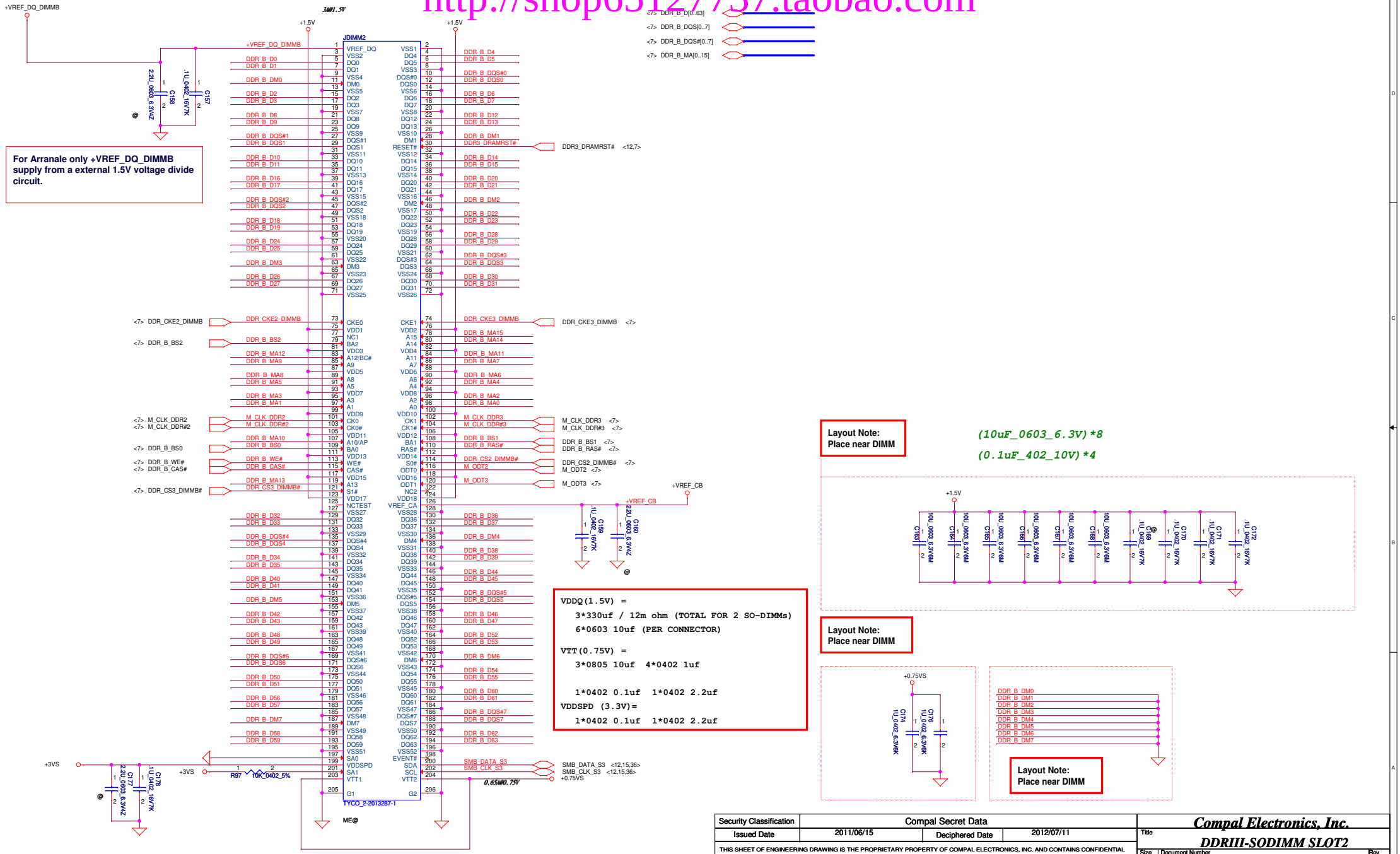
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size: Custom | Document Number: LA-9631P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 12 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size | Document Number: **LA-9631P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 13 of 60

CLRP2	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

CLRP3	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

W=20mils +RTCVCC — R99 1K_0402_5% — W=20mils +RTCBATT — C179 1U_0603_10V4Z

PCH_RTCX1 — R98 10M_0402_5% — PCH_RTCX2 — R104 0_0402_5% — Y1 32.768KHZ_12.5PF_CM31532768DZFT — C180 18P_0402_50V8J — C181 18P_0402_50V8J

+RTCVCC — R101 1M_0402_5% SM_INTRUDER# — R102 330K_0402_5% PCH_INTVRMEN

INTVRMEN

★ H : Integrated VRM enable
L : Integrated VRM disable

(INTVRMEN should always be pull high.)

+3VS — R105 1K_0402_5% HDA_SPKR

HIGH= Enable (No Reboot)
★ LOW= Disable (Default)

+3V_PCH — R106 1K_0402_5% ME_FLASH

★ Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3V_PCH — R108 1K_0402_5% HDA_SYNC

This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
★ 1.8V when sampled low
Needs to be pulled High for Chief River platfrom

DPDG1.1

+RTCVCC — C183 1U_0603_10V4Z — R103 20K_0402_5% — R100 20K_0402_5% — C182 1U_0603_10V4Z — RP2 @ SHORT PADS — RP3 @ SHORT PADS

U4A

PCH_RTCX1	A20	RTCX1	RTC
PCH_RTCX2	C20	RTCX2	
PCH_RTCRST#	D20	RTCRST#	
PCH_SRTCRST#	G22	SRTCRST#	
SM_INTRUDER#	K22	INTRUDER#	
PCH_INTVRMEN	C17	INTVRMEN	
HDA_BIT_CLK	N34	HDA_BCLK	IHDA
HDA_SYNC	L34	HDA_SYNC	
<41> HDA_SPKR	T10	SPKR	
HDA_RST#	K34	HDA_RST#	
<41> HDA_SDIN0	E34	HDA_SDIN0	
	G34	HDA_SDIN1	
	C34	HDA_SDIN2	
	A34	HDA_SDIN3	
<42> ME_FLASH	A36	HDA_SDO	
PCH_GPIO33	C36	HDA_DOCK_EN# / GPIO33	
PCH_GPIO13	N32	HDA_DOCK_RST# / GPIO13	
PCH_JTAG_TCK	J3	JTAG_TCK	JTAG
PCH_JTAG_TMS	H7	JTAG_TMS	
PCH_JTAG_TDI	K5	JTAG_TDI	
PCH_JTAG_TDO	H1	JTAG_TDO	
SPI_CLK_PCH_R	T3	SPI_CLK	SPI
SPI_SB_CS0#	Y14	SPI_CS0#	
	T1	SPI_CS1#	
SPI_SI	V4	SPI_MOSI	
SPI_SO_R	U3	SPI_MISO	

FWH0 / LAD0	C38	LPC_AD0	LPC_AD0 <42>
FWH1 / LAD1	A38	LPC_AD1	LPC_AD1 <42>
FWH2 / LAD2	B37	LPC_AD2	LPC_AD2 <42>
FWH3 / LAD3	C37	LPC_AD3	LPC_AD3 <42>
FWH4 / LFRAME#	D36	LPC_FRAME#	LPC_FRAME# <42>
LDRQ0#	E36		
LDRQ1# / GPIO23	K36		
SERIRQ	V5	SERIRQ	SERIRQ <42>

EC and Mini card debug port

SATA0RXN	AM3	SATA_DTX_C_IRX_N0	SATA_DTX_C_IRX_N0 <40>
SATA0RXP	AM1	SATA_DTX_C_IRX_P0	SATA_DTX_C_IRX_P0 <40>
SATA0TXN	AP7	SATA_ITX_C_DRX_N0	SATA_ITX_C_DRX_N0 <40>
SATA0TXP	AP5	SATA_ITX_C_DRX_P0	SATA_ITX_C_DRX_P0 <40>
SATA1RXN	AM10		
SATA1RXP	AM8		
SATA1TXN	AP11		
SATA1TXP	AP10		
SATA2RXN	AD7	SATA_DTX_C_IRX_N2	SATA_DTX_C_IRX_N2 <40>
SATA2RXP	AD5	SATA_DTX_C_IRX_P2	SATA_DTX_C_IRX_P2 <40>
SATA2TXN	AH5	SATA_ITX_C_DRX_N2	SATA_ITX_C_DRX_N2 <40>
SATA2TXP	AH4	SATA_ITX_C_DRX_P2	SATA_ITX_C_DRX_P2 <40>
SATA3RXN	AB8		
SATA3RXP	AB10		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	Y7		
SATA4RXP	Y5		
SATA4TXN	AD3		
SATA4TXP	AD1		
SATA5RXN	Y3		
SATA5RXP	Y1		
SATA5TXN	AB3		
SATA5TXP	AB1		
SATAICOMPO	Y11		
SATAICOMPI	Y10	SATA_COMP	R111 37.4_0402_1% +V1.05S_VCCP
SATA3RCOMPO	AB12		
SATA3COMPI	AB13	SATA3_COMP	R113 49.9_0402_1% +V1.05S_VCCP
SATA3RBIAS	AH1	RBIAS_SATA3	R115 750_0402_1%
SATALED#	P3	SATALED#	
SATA0GP / GPIO21	V14	PCH_GPIO21	
SATA1GP / GPIO19	P1	BBS_BIT0_R	

HDD

ODD

PANTHER-POINT_FCBGA989
HM76@
SA00005FH70
S IC BD82HM76 SLJ8E C1 BGA 989P PCH C38!

<41> HDA_BITCLK_AUDIO — HDA_BIT_CLK
<41> HDA_SYNC_AUDIO — HDA_SYNC_R
<41> HDA_RST_AUDIO# — HDA_RST#
<41> HDA_SDOUT_AUDIO — ME_FLASH
For EMI — RP12 33_0804_8P4R_5%

+5VS — Q10 LBSS138LT1G_SOT-23-3 — HDA_SYNC — R878 1M_0402_5%

check with vender
Del Q10 check with codec
VDDIO using 3VALW

SPI_CLK_PCH_R — R124 33_0402_5% @ — C190 22P_0402_50V8J @ For EMI

R124;c190 close to U4.T3 pin

U4 HM70@ — SA00005MQ80 — IC BD82HM70 SJTNV C1 BGA 989P PCH C38!

U4 NM70@ — SA00005WU60 — S IC BD82NM70 SLJTA C1 BGA 989P PCH C38!

+3V_ROM — R127 3.3K_0402_5% SPI_WP# — R129 3.3K_0402_5% SPI_HOLD#

<19> PCH_GPIO16 — BBS_BIT0_R, SATALED#, PCH_GPIO16, SERIRQ — RP17 10K_0804_8P4R_5% +3VS

Share ROM — RP2 @ — SPI_SO_R, SPI_SI, SPI_CLK_PCH_R, SPI_SB_CS0# — EC_SPI_SO, EC_SPI_SI, EC_SPI_CLK, EC_SPI_CS# — 0_0804_8P4R_5%

Share ROM — +3V_ROM

SPI_SB_CS0# — R131 0_0402_5% @ — SPI_SO_R — For EMI

U5 W25Q64FVSSIQ_SO8 — CS#, SO, WP#, GND, VCC, HOLD#, SCLK, SI — SPI_SO_L, SPI_WP#, SPI_HOLD#, SPI_CLK_1 — R133 0_0402_5% @ — SPI_CLK_PCH_R, SPI_SI — For EMI

SA000039A30
S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM

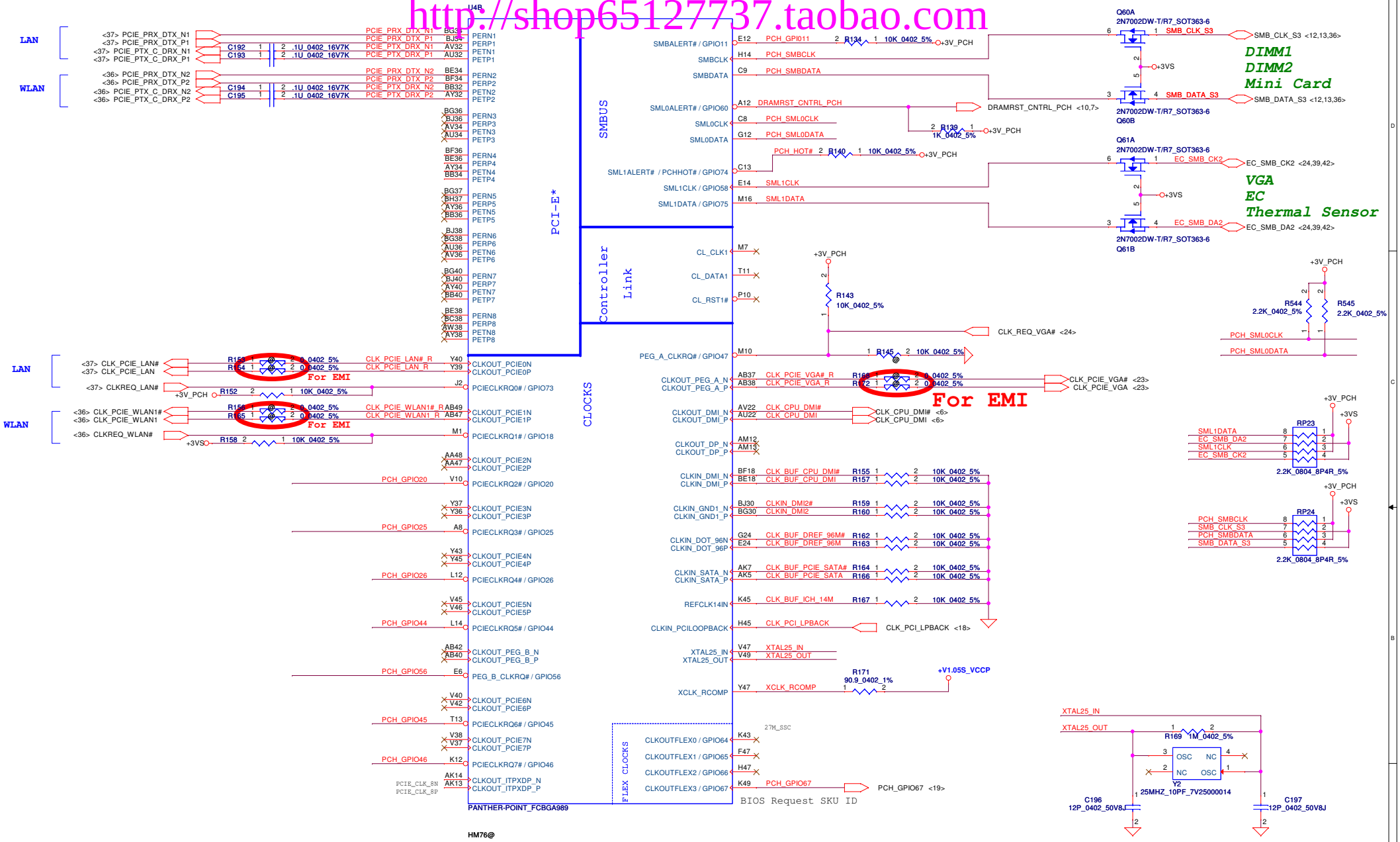
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: LA-9631P | Rev: 1.0

Date: Wednesday, March 06, 2013 | Sheet 14 of 60



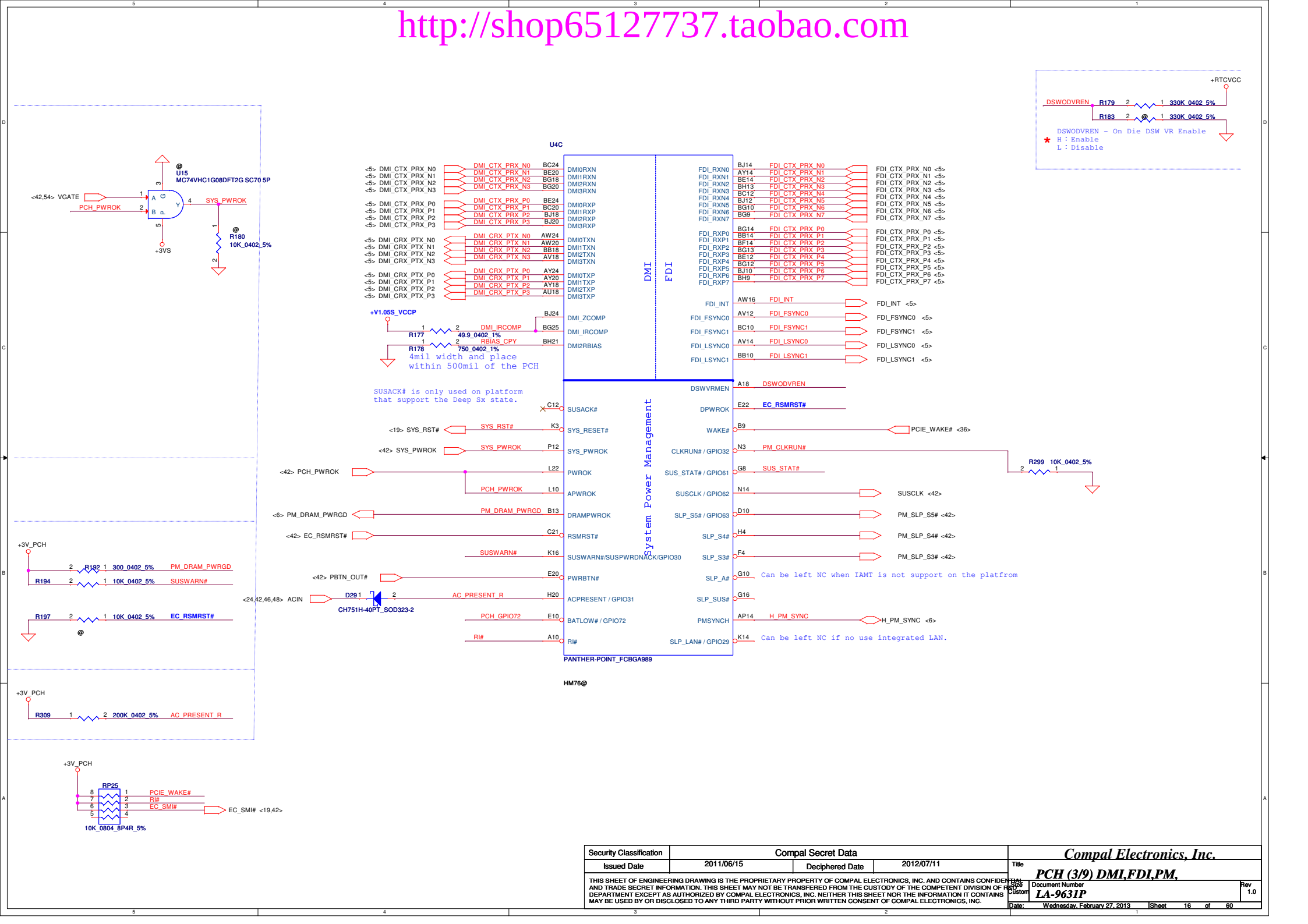
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	LA-9631P	1.0

Date: Wednesday, February 27, 2013 Sheet 15 of 60



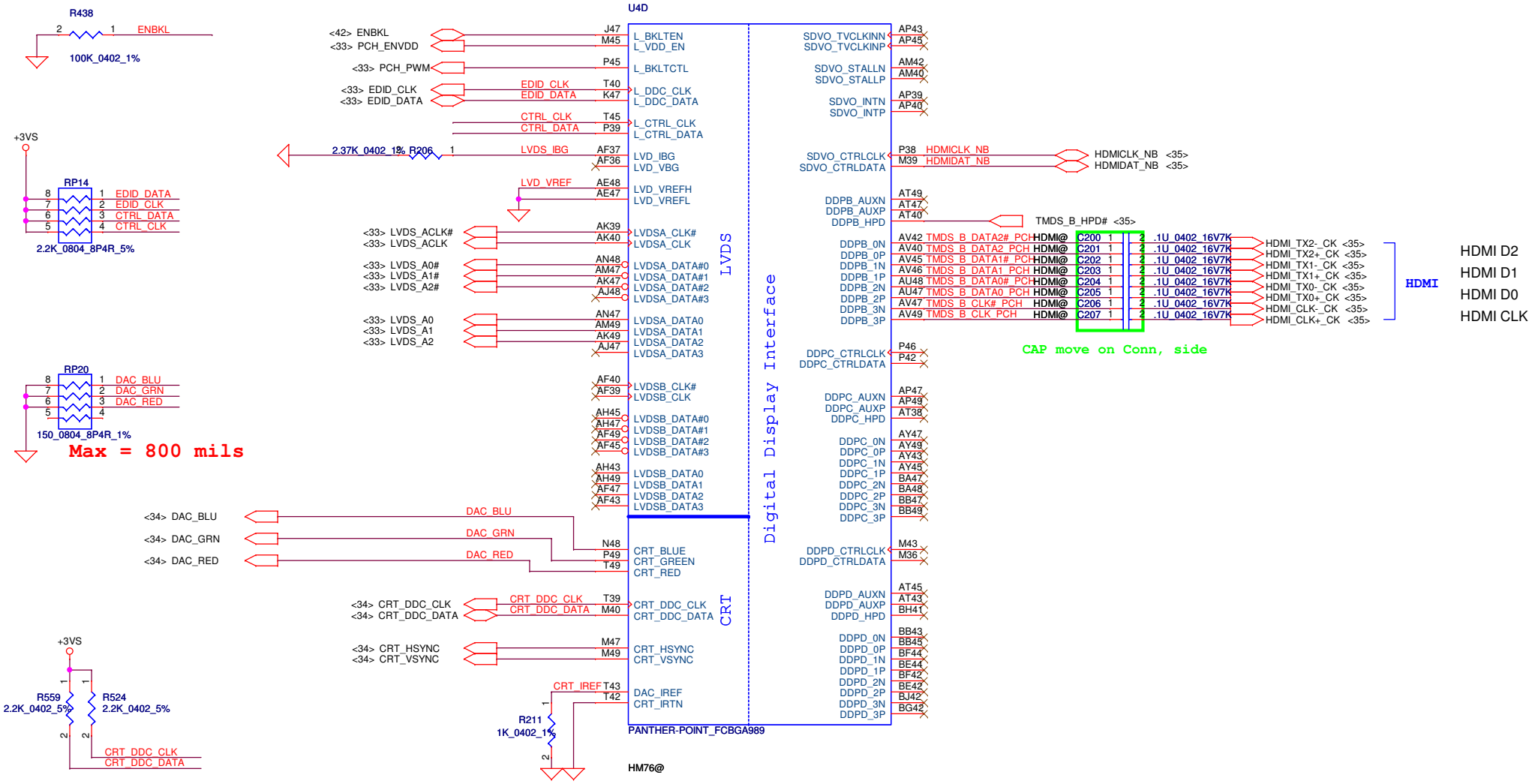
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size: Custom | Document Number: LA-9631P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 16 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
B	LA-9631P	1.0

Date: Wednesday, February 27, 2013 Sheet 17 of 60

RP1 8.2K_1206_10P8R_5%
PCI_PIRQA# PCI_PIRQD# PCI_PIRQC# PCI_PIRQB#
+3VS
PCH_GPIO2 DGPU_PWR_EN PCH_GPIO4 PCH_GPIO3

RP7 8.2K_0804_8P4R_5%
DGPU_HOLD_RST# PCH_WL_OFF# PCH_GPIO5 PCH_GPIO52

Pull-up resistors are not required on these signals

R292 @ 8.2K_0402_5% PCH_GPIO51
R557 @ 8.2K_0402_5% PCH_GPIO53

Boot BIOS Strap bit1 BBS1			
	Bit11	Bit10	Boot BIOS Destination
GNT1#/ GPIO51	0	1	Reserved
	1	0	Reserved
	1	1 *	SPI (Default)
	0	0	LPC

GPIO55
PCH_WL_OFF# R215 @ 1K_0402_5%

A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default *

U4E PANTHER-POINT_FCBGA989 HM76@

RSVD: TP1–TP24, RSVD1–RSVD29

USB3Rn1–USB3Rn4, USB3Rp1–USB3Rp4, USB3Tn1–USB3Tn4, USB3Tp1–USB3Tp4
<44> USB3_RX1_N / USB3_RX2_N / USB3_RX3_N / USB3_RX4_N
<44> USB3_RX1_P / USB3_RX2_P / USB3_RX3_P / USB3_RX4_P
<44> USB3_TX1_N / USB3_TX2_N
<44> USB3_TX1_P / USB3_TX2_P

PCI: PIRQA#, PIRQB#, PIRQC#, PIRQD#, REQ1#/GPIO50, REQ2#/GPIO52, REQ3#/GPIO54, GNT1#/GPIO51, GNT2#/GPIO53, GNT3#/GPIO55, PIRQE#/GPIO2, PIRQF#/GPIO3, PIRQG#/GPIO4, PIRQH#/GPIO5, PME#, PLTRST#, CLKOUT_PCI0–CLKOUT_PCI4

<23> DGPU_HOLD_RST#
<25,42,51,53> DGPU_PWR_EN
<36> PCH_WL_OFF#
<6> PCH_PLTRST#
<15> CLK_PCI_LPBACK
<42> CLK_PCI_EC
22_0402_5% R219 CLK_PCI_LPBACK_R
22_0402_5% R220 CLK_PCI_EC_R
CLK_PCI_DB_R
For EMI

USB: USBP0N–USBP3N, USBP0P–USBP3P, USBP4N–USBP7N, USBP4P–USBP7P, USBP8N–USBP11N, USBP8P–USBP11P, USBP12N–USBP13N, USBP12P–USBP13P, USBRBIAS, USBRBIAS#, OC0#/GPIO59 … OC7#/GPIO14

USB Debug Port = Port1 and Port9

USBP0N/P	USB20_N0/P0	USB20_N0/P0 <44>	LEFT USB (USB 3.0)
USBP1N/P	USB20_N1/P1	USB20_N1/P1 <44>	LEFT USB (USB 3.0)
USBP2N/P	USB20_N2/P2	USB20_N2/P2 <44>	Touch Screen
USBP3N/P	USB20_N3/P3	USB20_N3 <33> / USB20_P3 <33>	USB Camera
USBP8N/P	USB20_N9/P9	USB20_N9/P9 <44>	RIGHT USB
USBP9N/P	USB20_N10/P10	USB20_N10 <36> / USB20_P10 <36>	WLAN
USBP10N/P	USB20_N11/P11	USB20_N11 <43> / USB20_P11 <43>	CARD READER

USBRBIAS R218 22.6_0402_1% Within 500 mils

OC0#/GPIO59 USB_OC0# — For LEFT USB3.0 Port — USB_OC0# <44>
OC4#/GPIO43 USB_OC4# — USB_OC4# <44> — For RIGHT USB2.0 Port

RP18 10K_1206_10P8R_5%
+3V_PCH
USB_OC0# USB_OC1# USB_OC2# USB_OC3# USB_OC4# USB_OC5# USB_OC6# USB_OC7#

<23,36,37,42> PLT_RST#
@ R222 0_0402_5% PCH_PLTRST#
C208 @ 1U_0402_6.3V6K
R223 100K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PCH (5/9) PCI, USB
Size: Custom | Document Number: LA-9631P | Rev: 1.0
Date: Wednesday, February 27, 2013 | Sheet 18 of 60

PCH_GPIO69	PCH_GPIO70	Function
1	1	NM70
1	0	Reserved
0	1	HM70
0	0	HM76

PCH_GPIO71	Function
1	Mars XT
0	Sun Pro

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R240 1 @ 2 1K_0402_5% PCH_GPIO28

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R245 1 @ 2 10K_0402_5% PCH_GPIO27

GPIO36, 37
When Unused as GPIO or SATA*GP
Use 8.2K-10K pull-down to ground.

R244 @ 10K_0402_5% PCH_GPIO37
R881 10K_0402_5%
R250 @ 10K_0402_5% PCH_GPIO36
R547 @ 10K_0402_5%

BIOS Request SKU ID

R711 UMA@ 10K_0402_5% PCH_GPIO38
R246 UMA@ 10K_0402_5%
PCH_GPIO67 PCH_GPIO67 <15>
R708 PX@ 10K_0402_5%
R298 PX@ 10K_0402_5%

PCH_GPIO38	PCH_GPIO67	Function
0	0	SG(Optimus / PX)
0	1	Reserved
1	0	DIS
1	1	UMA

RP10 10K_0804_8P4R_5%
PCH_GPIO39
SYS_RST# SYS_RST# <16>
PCH_BT_ON#
PCH_GPIO35

U4F — PANTHER-POINT_FCBGA989 — HM76@

GPIO:
PCH_GPIO0 T7 BMBUSY# / GPIO0
PCH_GPIO1 A42 TACH1 / GPIO1
PCH_GPIO6 H36 TACH2 / GPIO6
<42> EC_SCI# EC_SCI# E38 TACH3 / GPIO7
<16,42> EC_SMI# EC_SMI# C10 GPIO8
PCH_GPIO12 C4 LAN_PHY_PWR_CTRL / GPIO12
+3V_PCH R230 1K_0402_5% EC_LID_OUT# G2 GPIO15
<42> EC_LID_OUT#
<14> PCH_GPIO16 PCH_GPIO16 U2 SATA4GP / GPIO16
<53> DGPU_PWROK PU on power side D40 TACH0 / GPIO17
PCH_BT_ON# T5 SCLOCK / GPIO22
<36> PCH_BT_ON#
+3V_PCH R241 10K_0402_5% ODD_EN E8 GPIO24
<40> ODD_EN
PCH_GPIO27 E16 GPIO27
+3VS R242 10K_0402_5% PCH_GPIO28 P8 GPIO28
INTEL_BT_OFF# K1 STP_PCI# / GPIO34
<36> INTEL_BT_OFF#
PCH_GPIO35 K4 GPIO35
PCH_GPIO36 V8 SATA2GP / GPIO36
PCH_GPIO37 M5 SATA3GP / GPIO37
PCH_GPIO38 N2 SLOAD / GPIO38
PCH_GPIO39 M3 SDATAOUT0 / GPIO39
PCH_GPIO48 V13 SDATAOUT1 / GPIO48
PCH_GPIO49 V3 SATA5GP / GPIO49 / TEMP_ALERT#
PCH_GPIO57 D6 GPIO57

CPU/MISC:
TACH4 / GPIO68 C40 PCH_GPIO68
TACH5 / GPIO69 B41 PCH_GPIO69
TACH6 / GPIO70 C41 PCH_GPIO70
TACH7 / GPIO71 A40 PCH_GPIO71
A20GATE P4 — R236 10K_0402_5% +3VS — GATEA20 <42>
PECI AU16
RCIN# P5 KBRST# — KBRST# <42>
PROCPWRGD AY11 — H_CPUPWRGD <6>
THRMTRIP# AY10 PCH_THRMTRIP# R 1 R239 2 390_0402_5% H_THRMTRIP# — H_THRMTRIP# <6>
INIT3_3V T14
DF_TVS AY1 — INIT3_3V This signal has weak internal PU,can't pull low
TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37

KBRST# R226 1 2 10K_0402_5% +3VS

DMI Termination Voltage

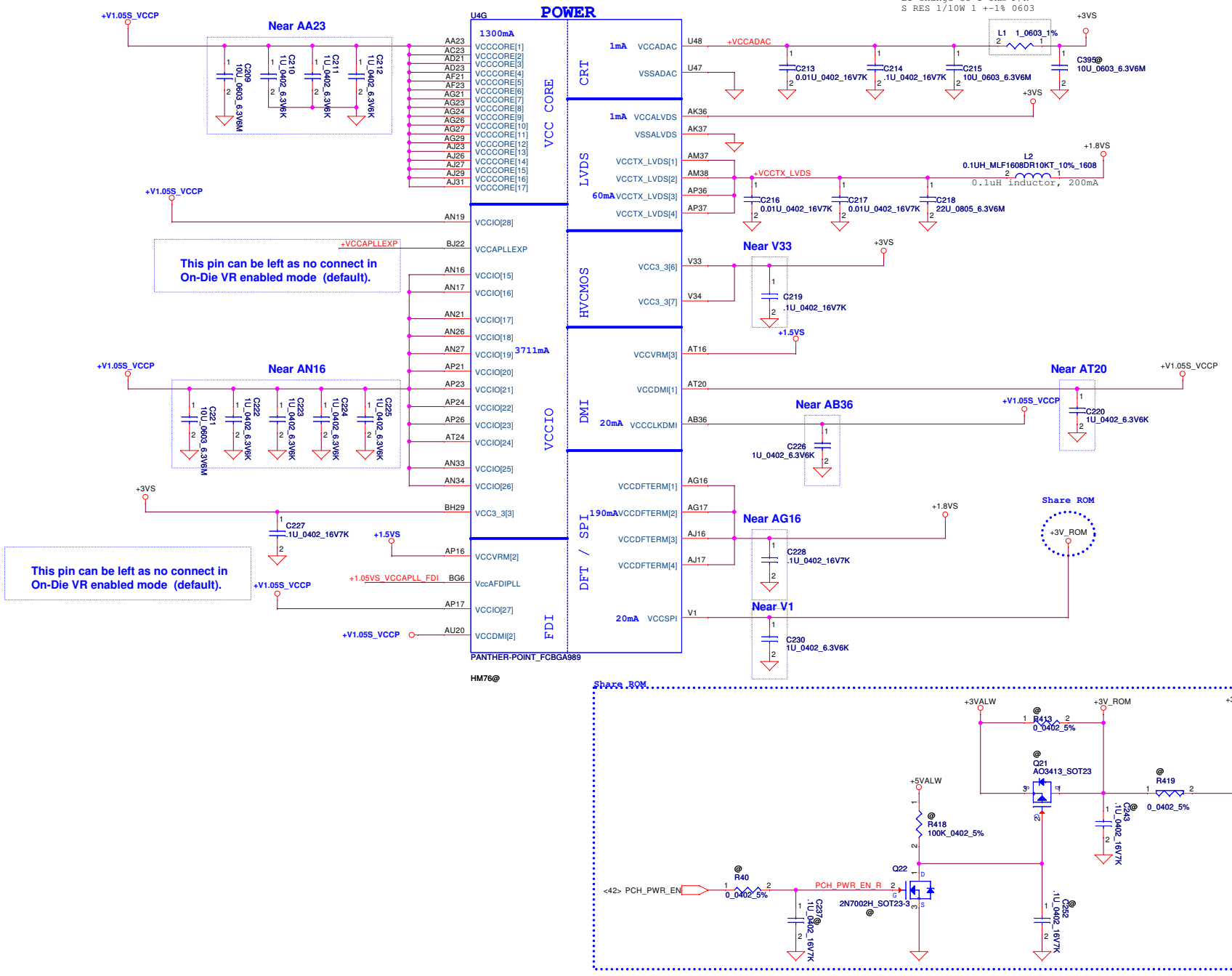
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

+1.8VS R216 2.2K_0402_5%
NV_CLE — R217 1K_0402_5% — H_SNB_IVB# <6>
Weak internal PU,Do not pull low
CLOSE TO THE BRANCHING POINT

NCTF:
VSS_NCTF_1 A4
VSS_NCTF_2 A44
VSS_NCTF_3 A45
VSS_NCTF_4 A46
VSS_NCTF_5 A5
VSS_NCTF_6 A6
VSS_NCTF_7 B3
VSS_NCTF_8 B47
VSS_NCTF_9 BD1
VSS_NCTF_10 BD49
VSS_NCTF_11 BE1
VSS_NCTF_12 BE49
VSS_NCTF_13 BF1
VSS_NCTF_14 BF49
VSS_NCTF_15 BG2
VSS_NCTF_16 BG48
VSS_NCTF_17 BH3
VSS_NCTF_18 BH47
VSS_NCTF_19 BJ4
VSS_NCTF_20 BJ44
VSS_NCTF_21 BJ45
VSS_NCTF_22 BJ46
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ6
VSS_NCTF_25 C2
VSS_NCTF_26 C48
VSS_NCTF_27 D1
VSS_NCTF_28 D49
VSS_NCTF_29 E1
VSS_NCTF_30 E49
VSS_NCTF_31 F1
VSS_NCTF_32 F49

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PCH (6/9) GPIO, CPU, MISC
Size: Custom | Document Number: LA-9631P | Rev: 1.0
Date: Wednesday, February 27, 2013 | Sheet 19 of 60



PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

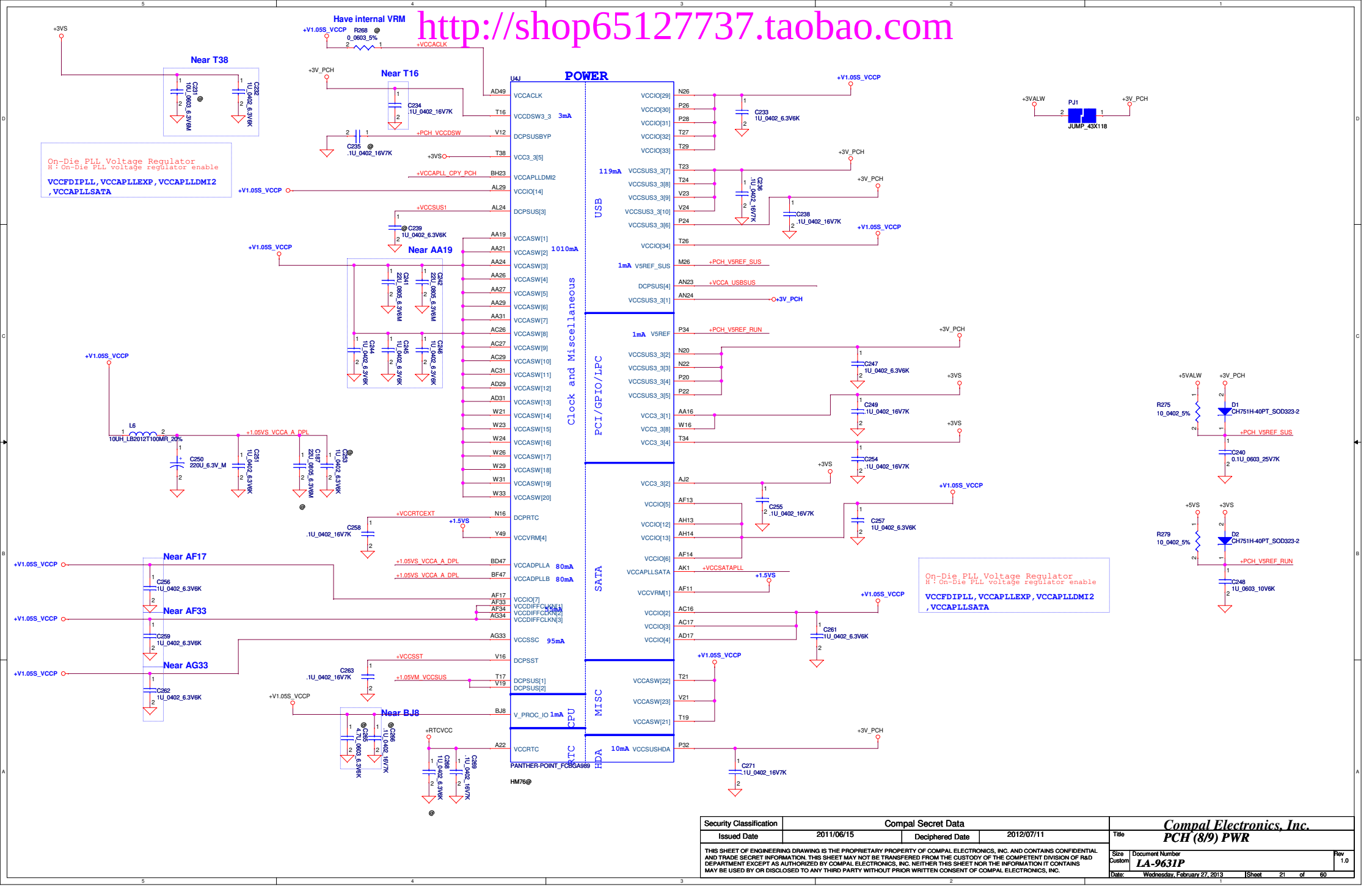
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (7/9) PWR

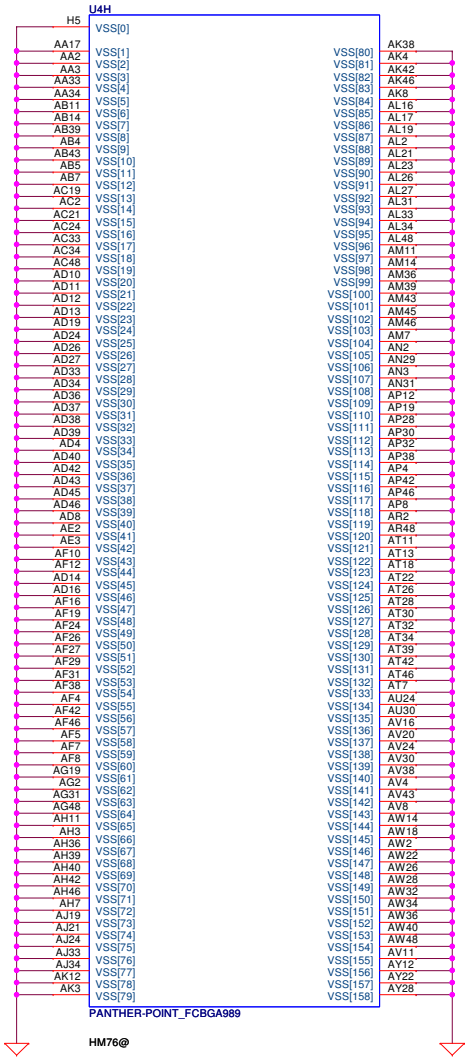
Size: Custom | Document Number: LA-9631P | Rev: 1.0

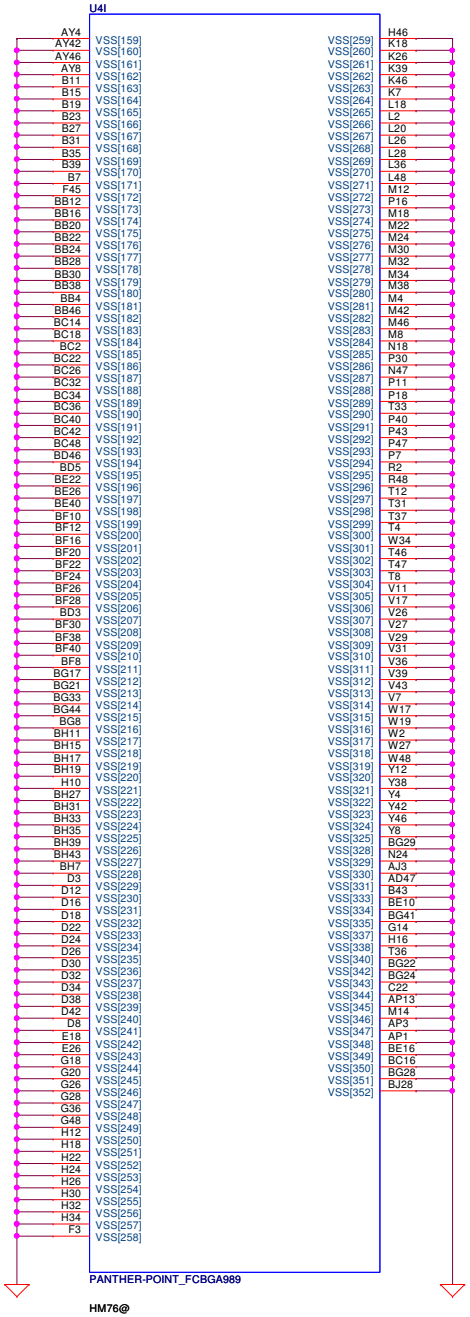
Date: Wednesday, February 27, 2013 | Sheet 20 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.		
Title: PCH (8/9) PWR		
Size: Custom	Document Number: LA-9631P	Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 21 of 60	





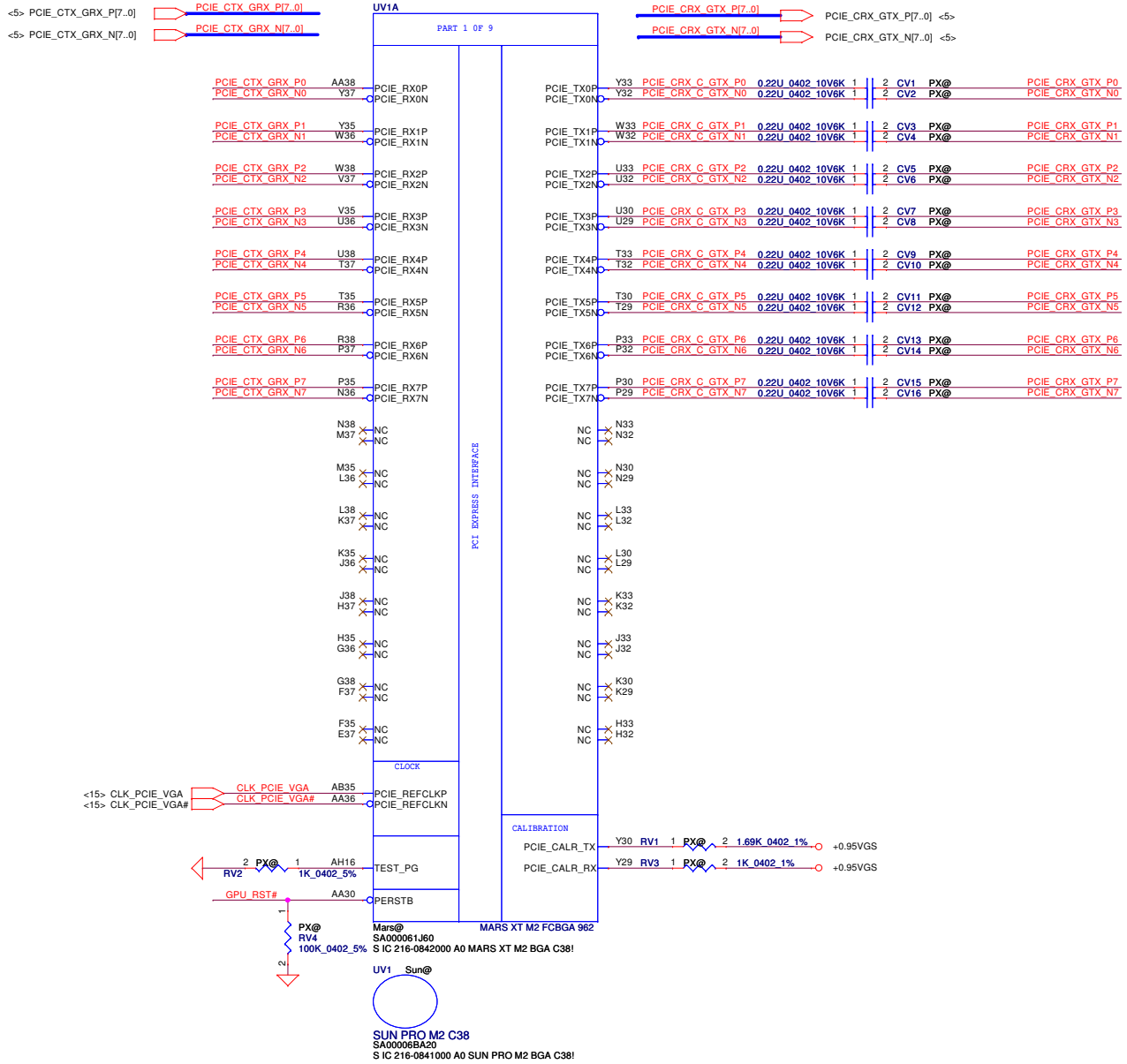
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

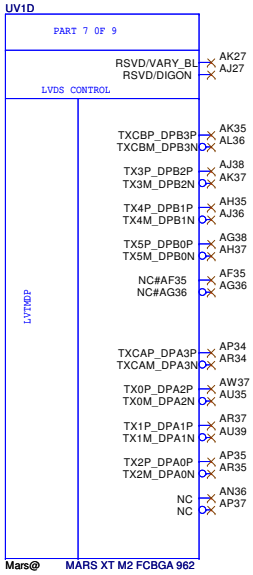
Title: PCH (9/9) VSS

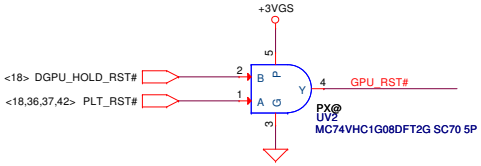
Size: Custom | Document Number: LA-9631P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 22 of 60



LVDS Interface





Security Classification	Compal Secret Data		Compal Electronics, Inc.
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			Date: Wednesday, March 06, 2013; Sheet 23 of 60

STRAPS

CONFIGURATION STRAPS

ALLOW FOR PULL UP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	PCIE Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	PCIE Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV010 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	X
AUD[1] AUD[0]	NA NA	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It isthe responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	Reserved for future ASIC	0
		NOTE:ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

GPIO_28_FDO	MLPS
H	Disable
L	Enable

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	11	000	NC	NC	4.75K
PS_1[5:1]	01	001	82nF	8.45K	2K
PS_2[5:1]	11	000	NC	NC	4.75K
PS_3[5:1]	11	XXX	NC	X	X

Mapping to VRAM type please refer to page 4

Place CLOSE VGA CHIP

0.60 V level, Please VREFG Divider ans cap close to ASIC

(1.8V@70mA AVDD)
(1.8V@117mA VDD1DI)
(1.8V@13mA TSVDD)

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_Main_MSIC

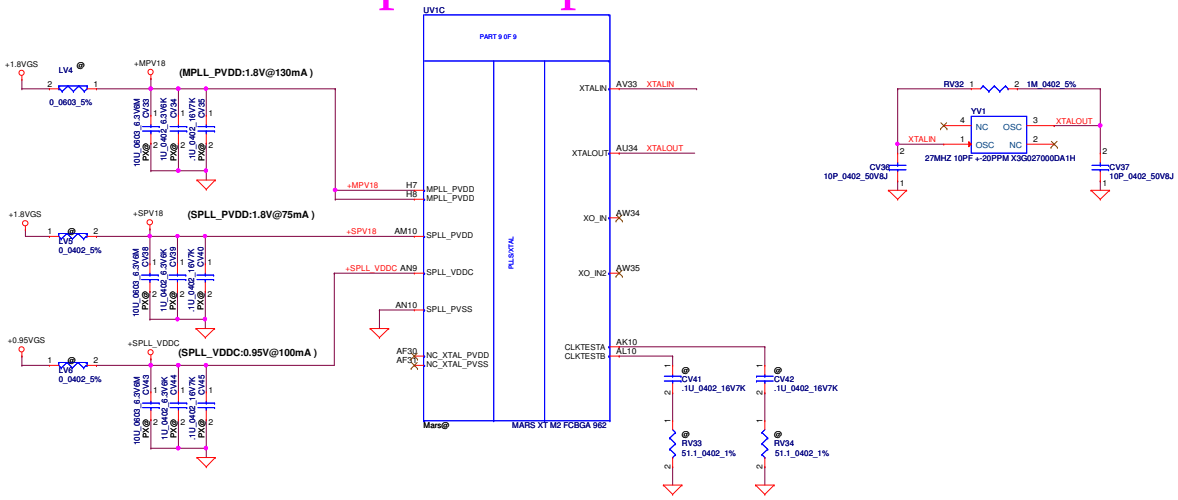
Size: C | Document Number: LA-9631P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 24 of 60

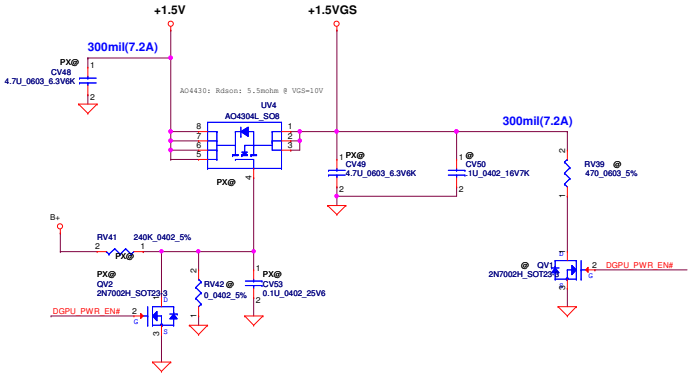
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

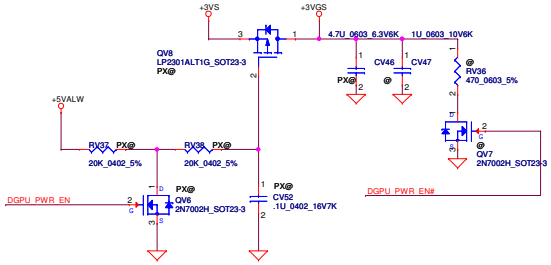
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



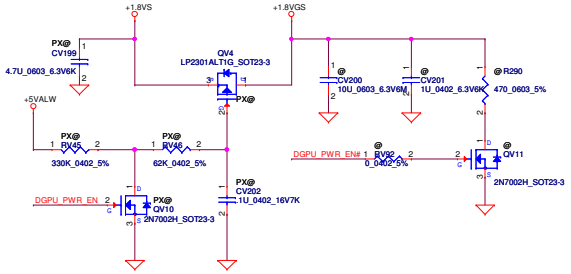
+1.5V to +1.5VGS

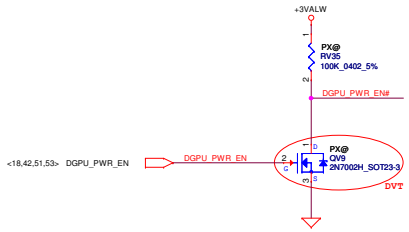


+3VS to +3VGS



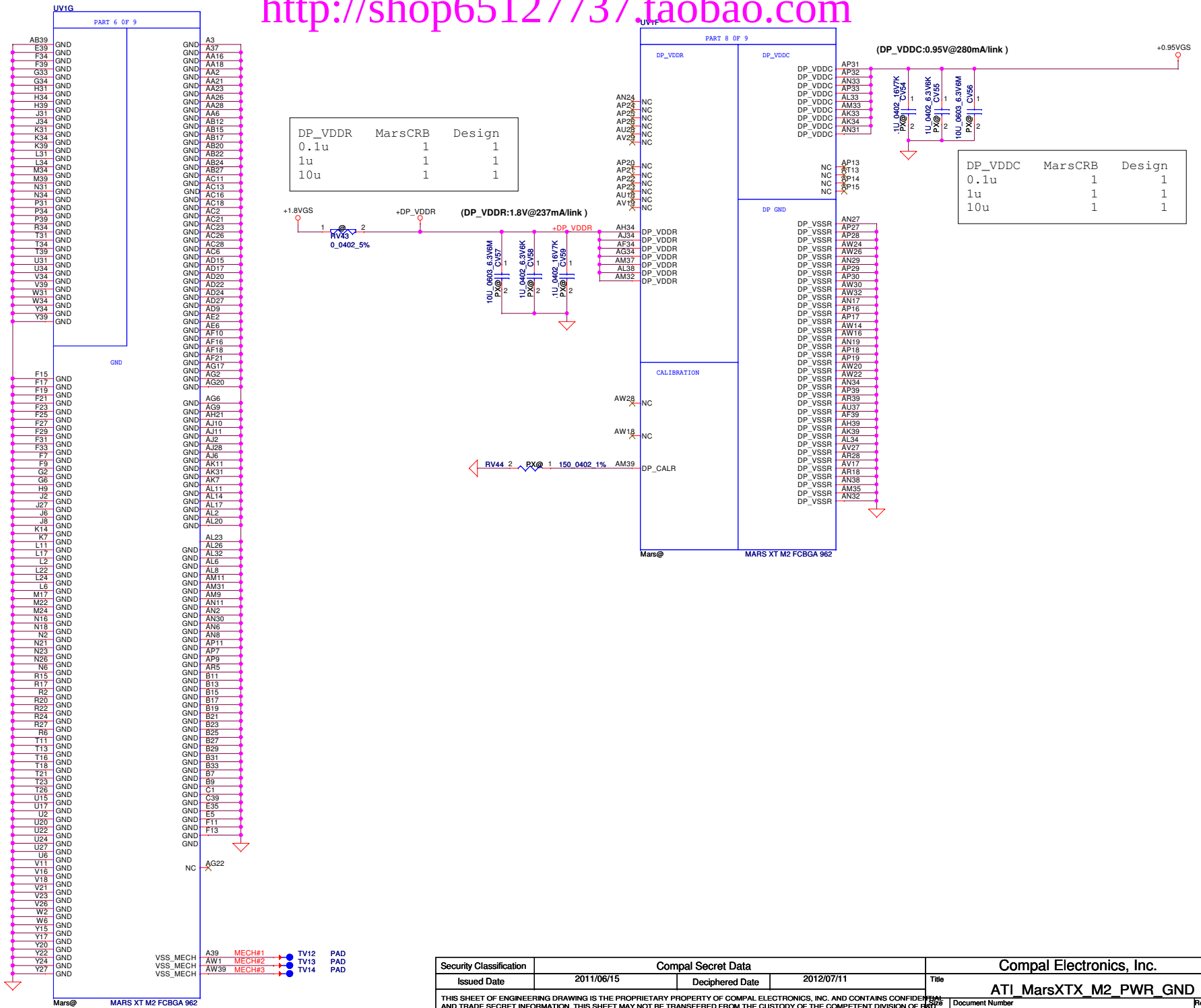
+1.8VS to +1.8VGS





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: ATI_MarsXTX_M2_BACO POWER			
Size: Custom	Document Number: LA-9631P		Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 25 of 60		



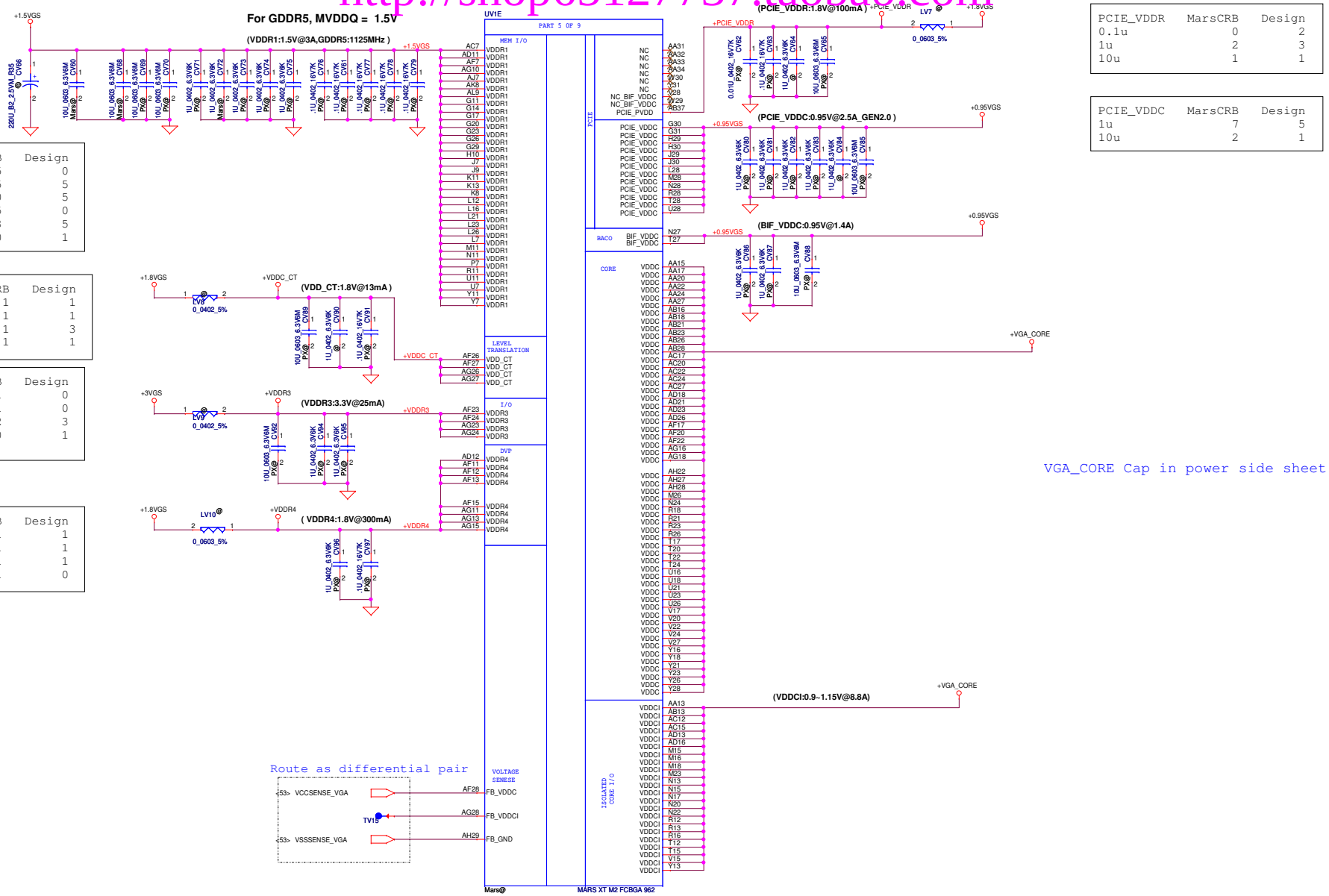
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_PWR_GND

Size: Custom | Document Number: LA-9631P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 26 of 60



VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

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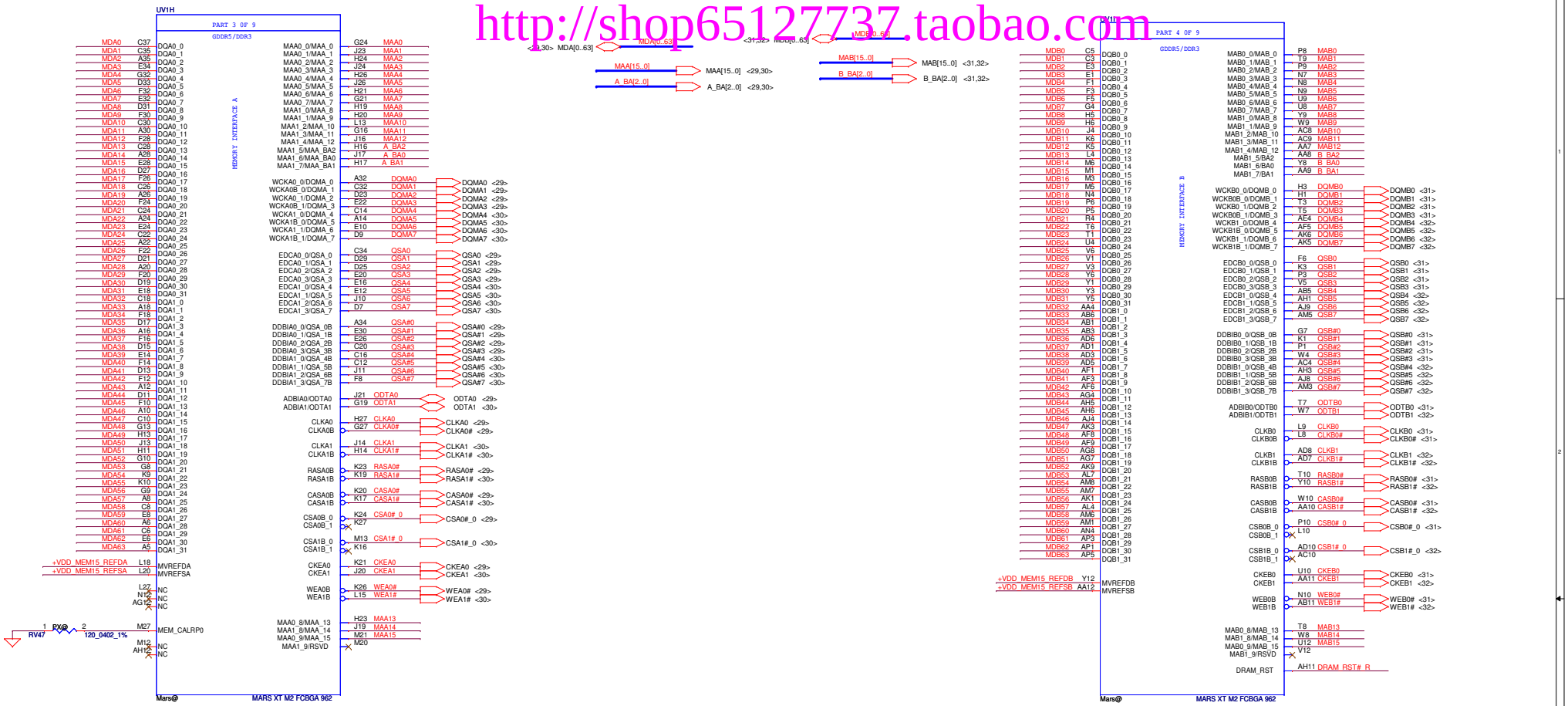
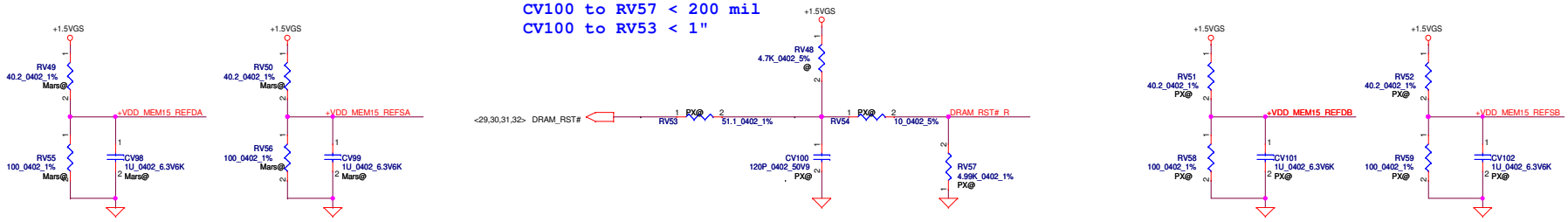


Ball to RV57 < 1"
CV100 to RV57 < 200 mil
CV100 to RV53 < 1"



DRAM_RST# is a daisy-chain net that connects to all VRAM

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

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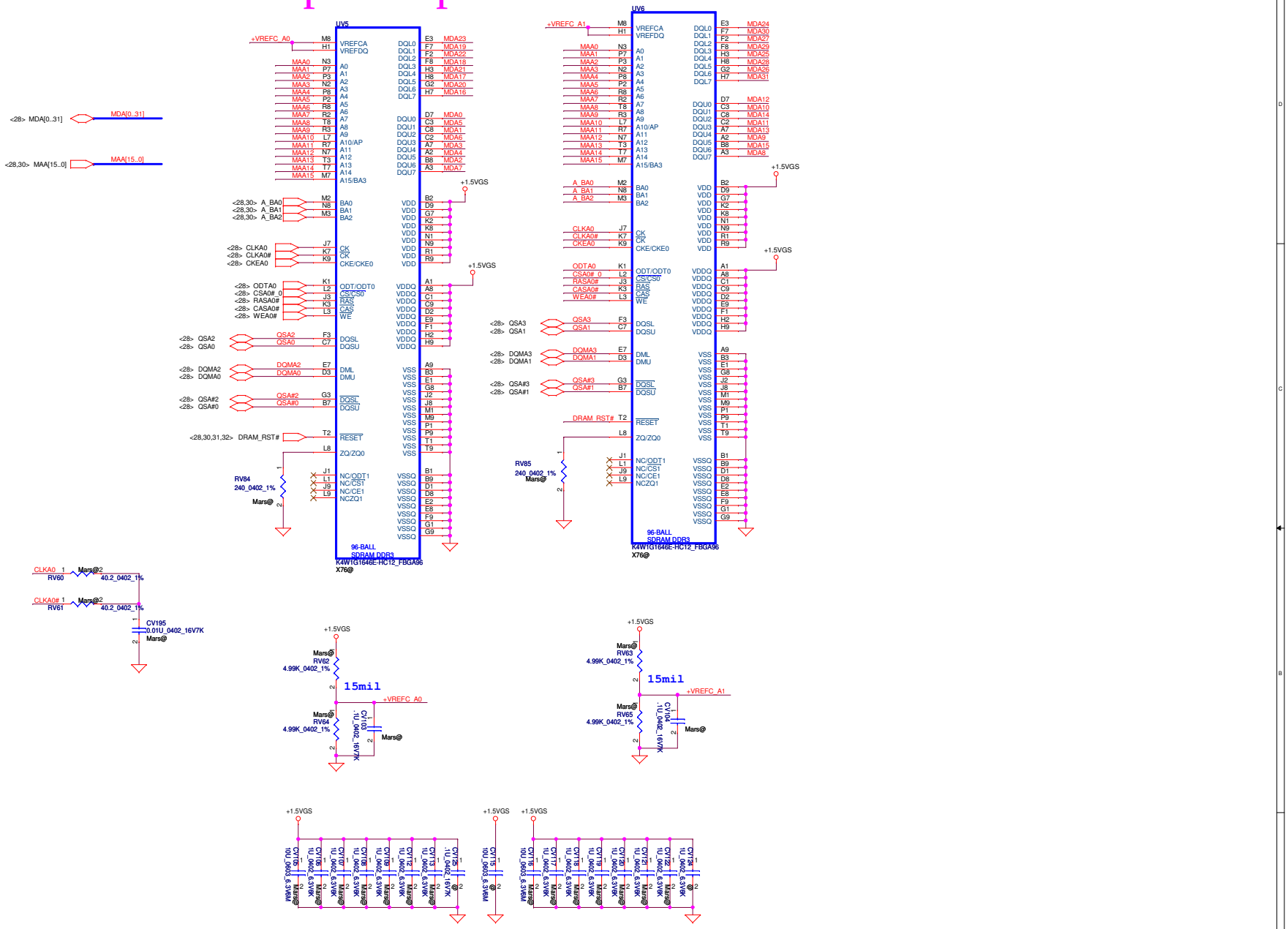
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_MEM IF

Size	Document Number	Rev
C	LA-9631P	1.0

Date: Wednesday, February 27, 2013 Sheet 28 of 60



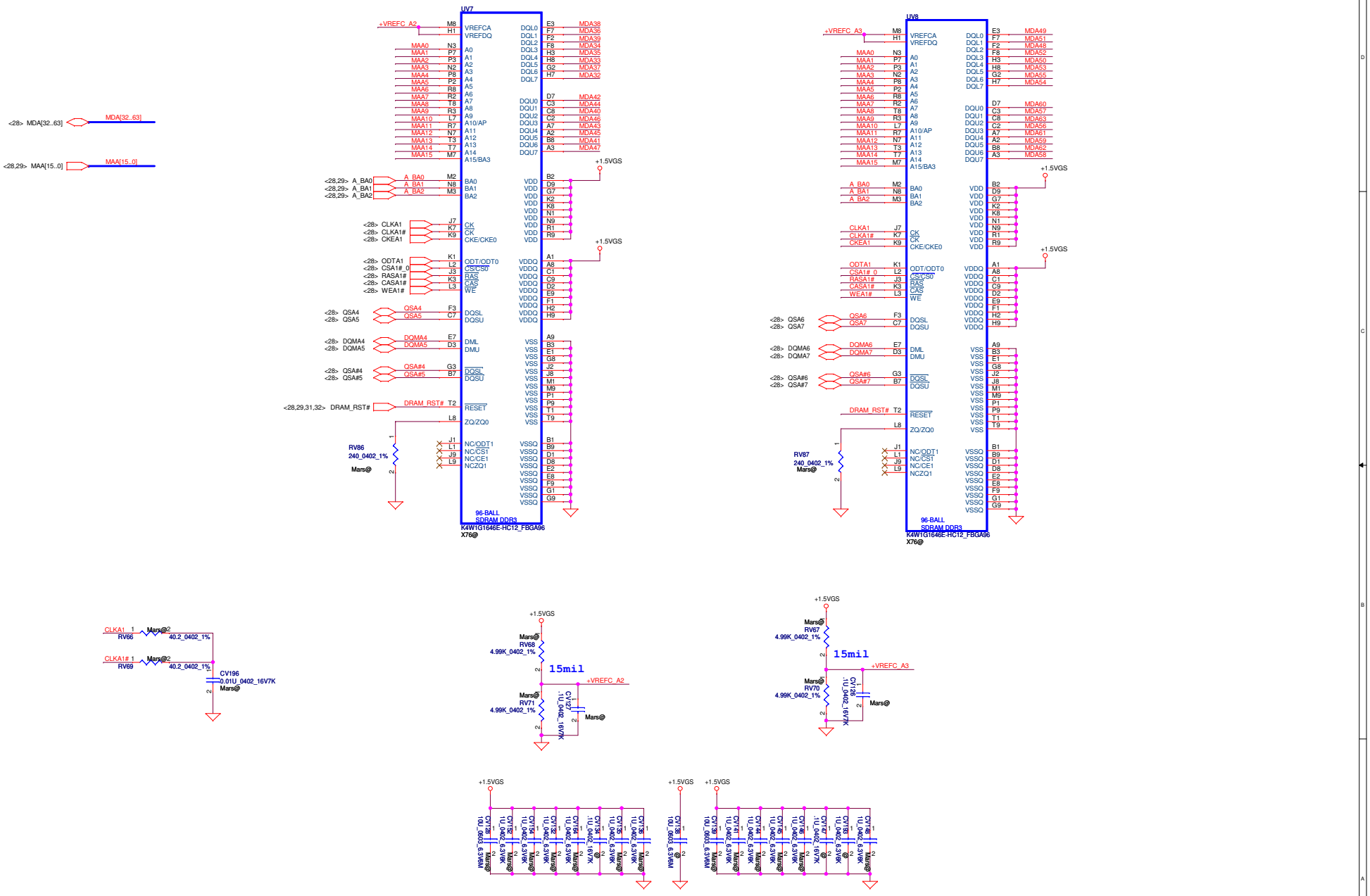
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_A

Size	Document Number	Rev
C	LA-9631P	1.0

Date: Wednesday, February 27, 2013 | Sheet 29 of 60



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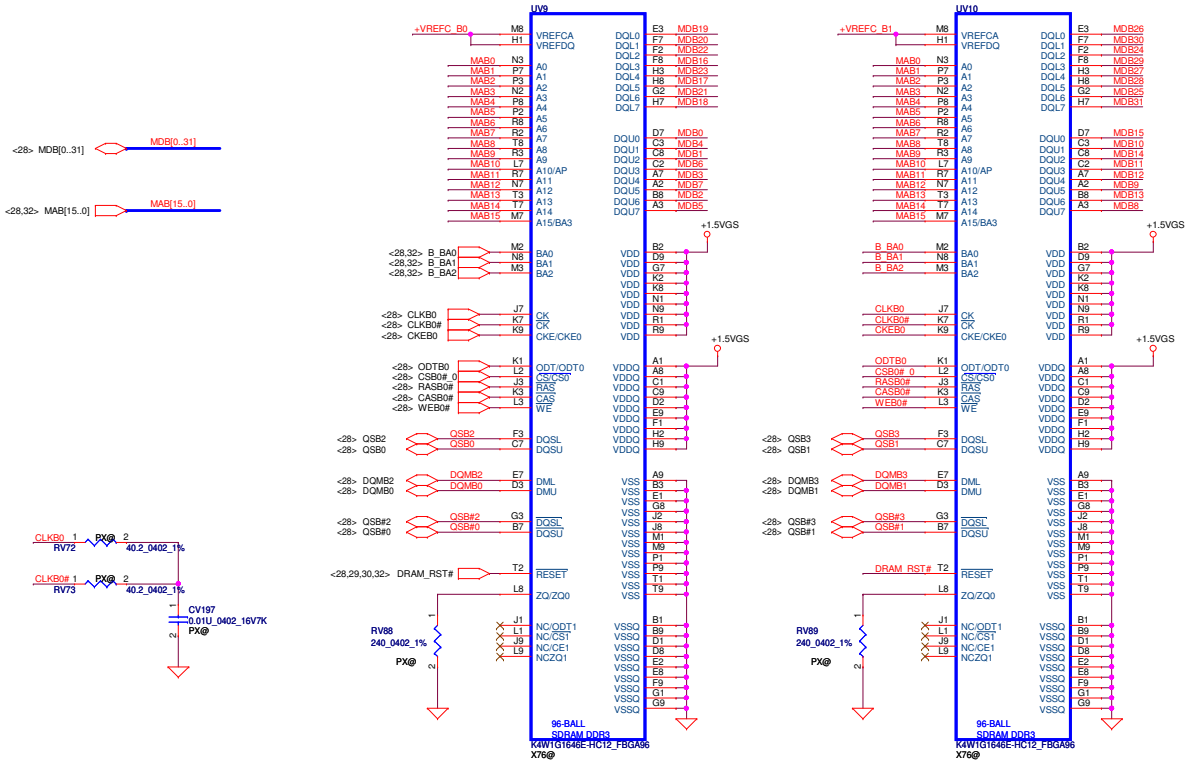
Title: ATI_Whistler_M2_VRAM_A

Size	Document Number	Rev
C	LA-9631P	1.0

Date: Wednesday, February 27, 2013 | Sheet 30 of 60



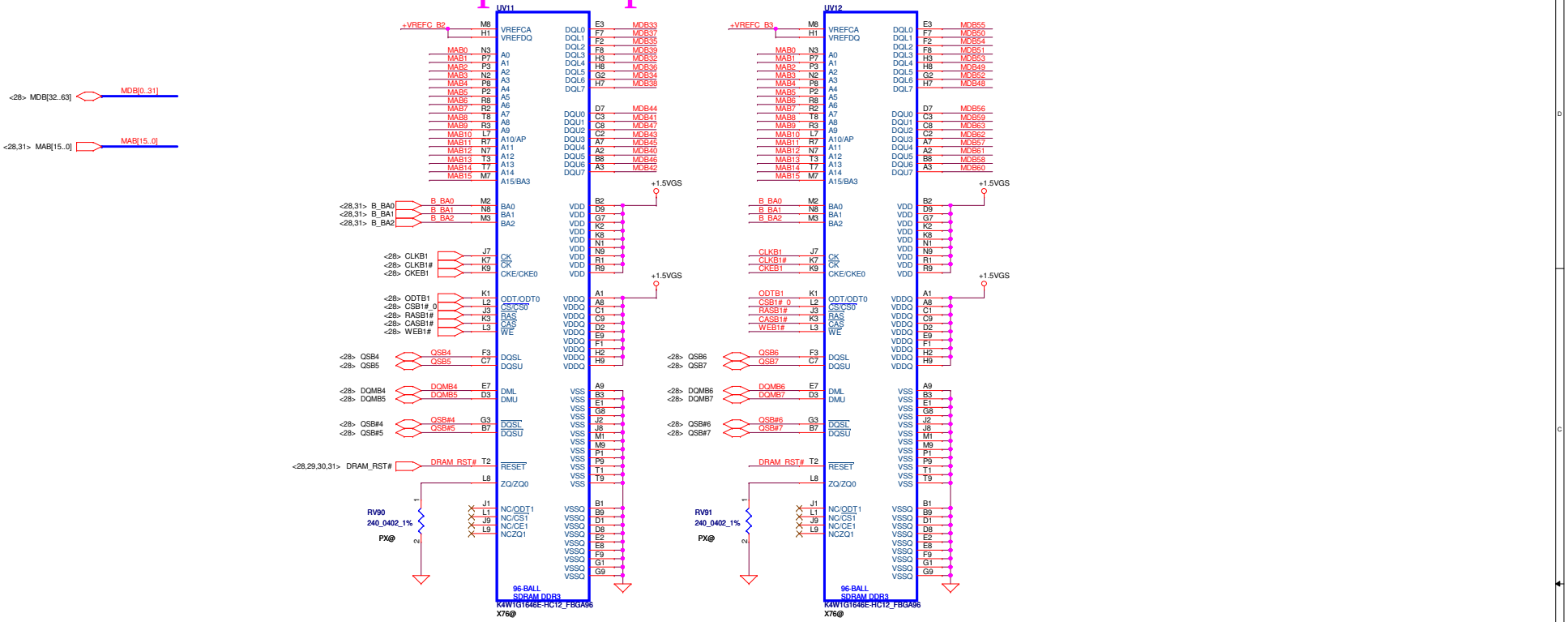
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_B

Size	Document Number	Rev
C	LA-9631P	1.0

Date: Wednesday, February 27, 2013 | Sheet 31 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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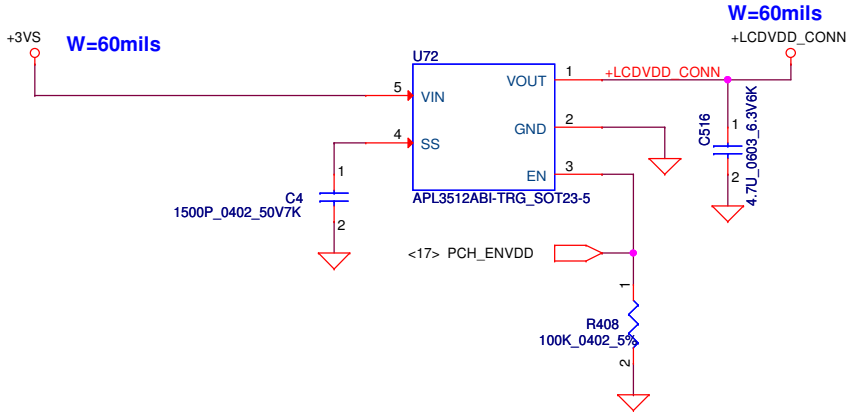
Compal Electronics, Inc.

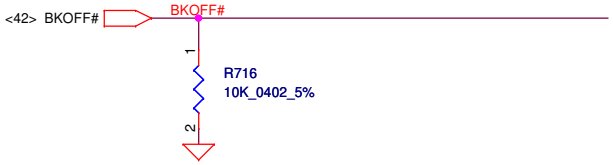
Title: ATI_Whistler_M2_VRAM_A

Size	Document Number	Rev
C	LA-9631P	1.0

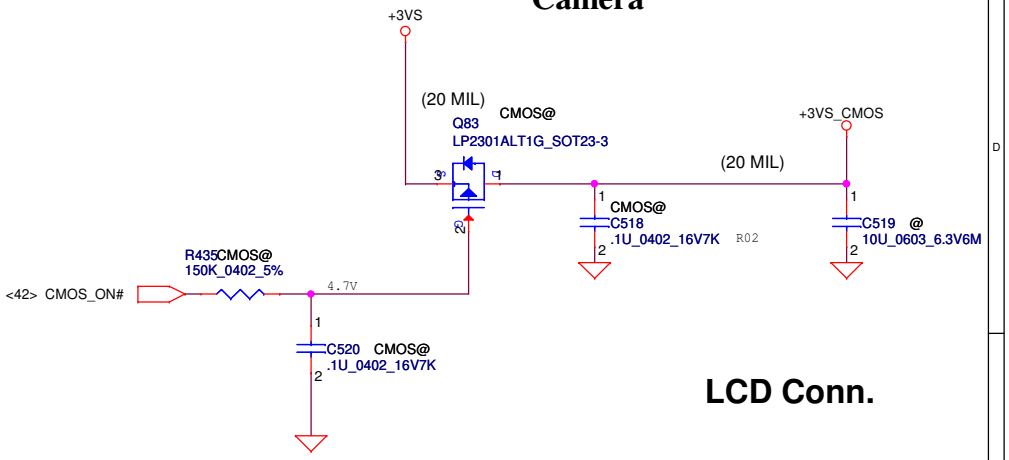
Date: Wednesday, February 27, 2013 | Sheet 32 of 60

LCD POWER CIRCUIT

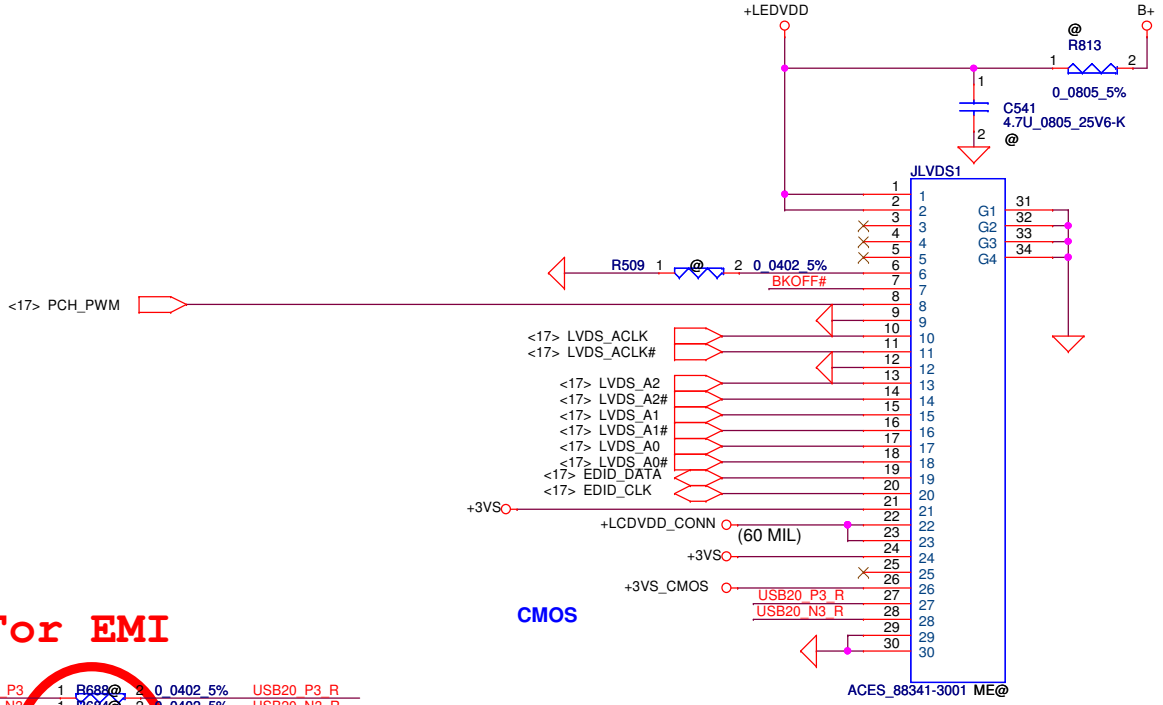




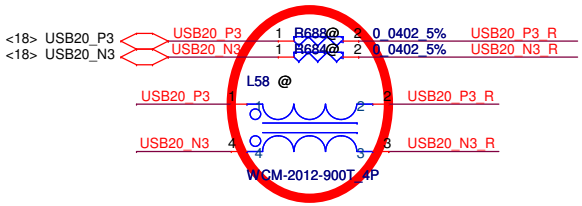
Camera



LCD Conn.



For EMI



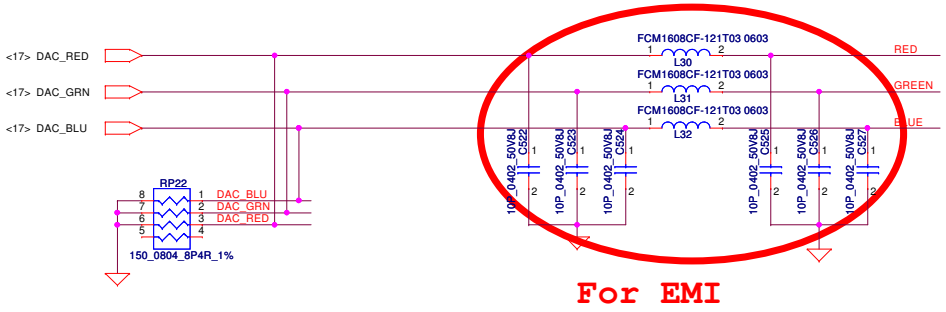
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

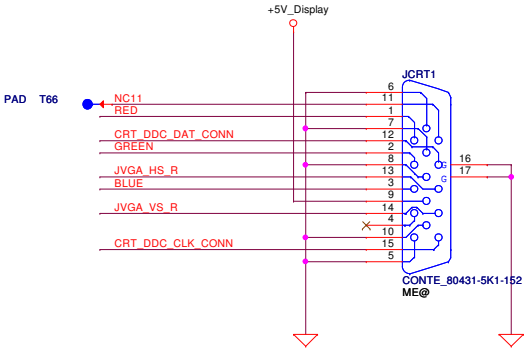
Compal Electronics, Inc.

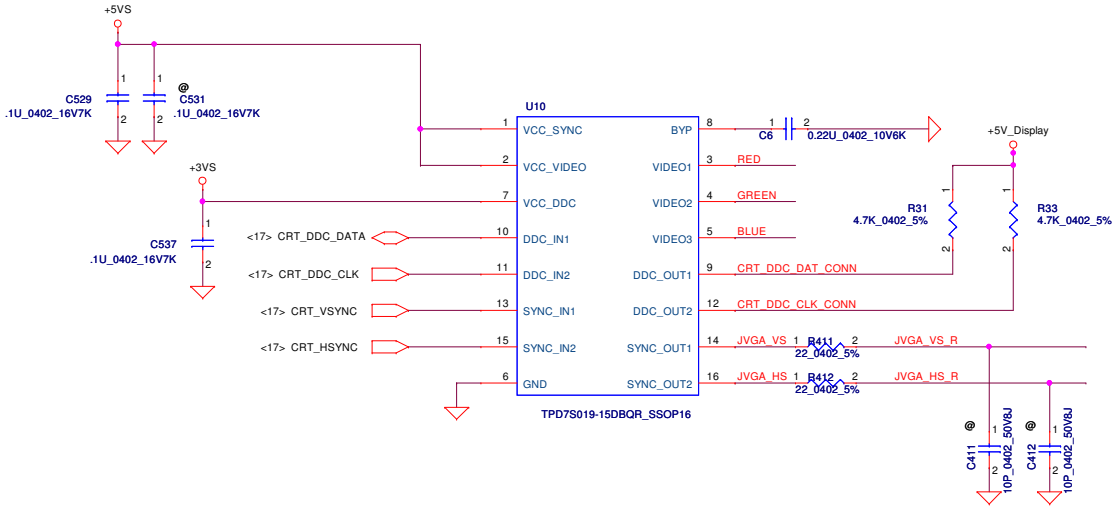
Title: **LVDS/CAMERA**

Size: Custom | Document Number: **LA-9631P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 33 of 60







Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title: CRT Connector
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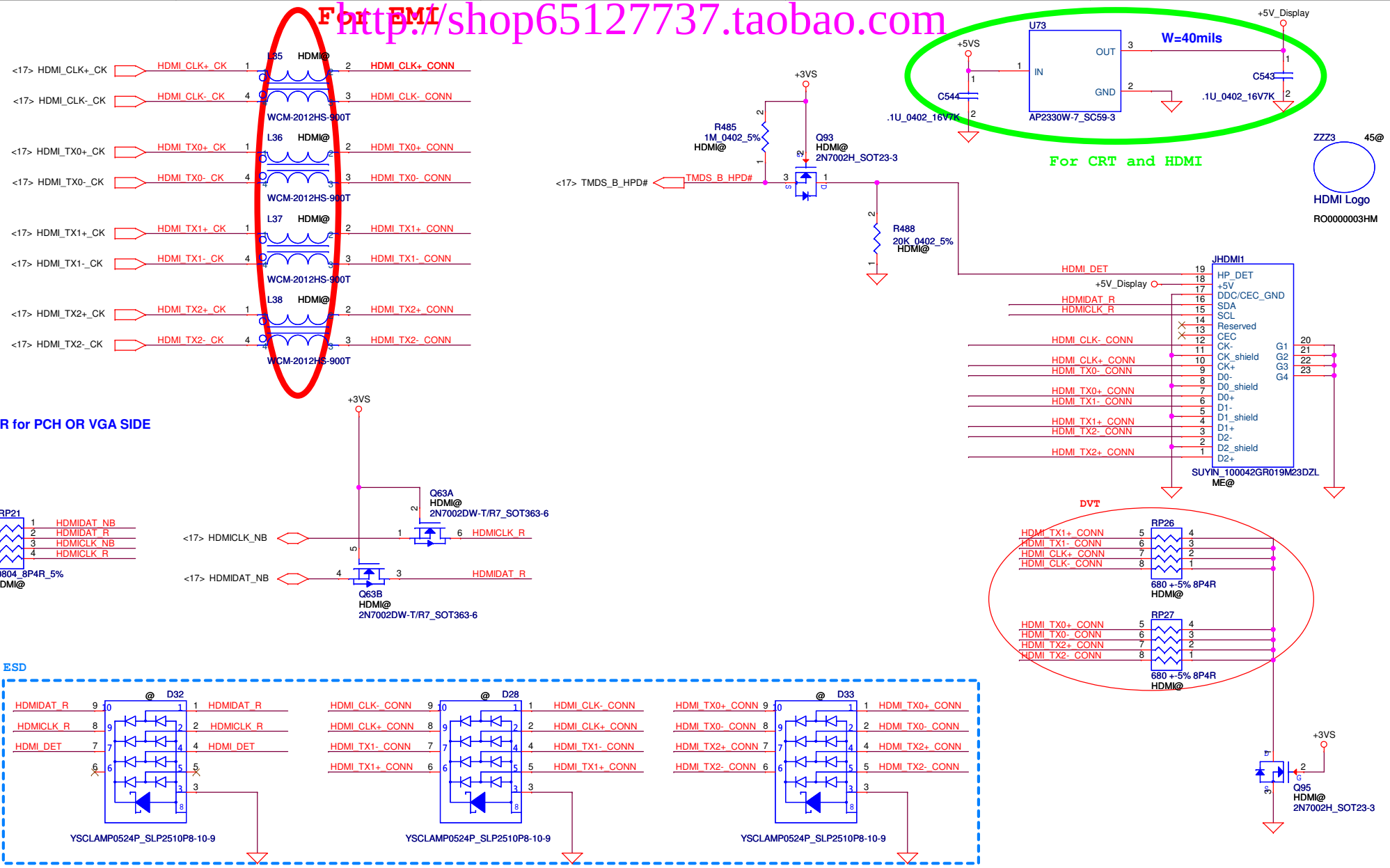
				Date: Wednesday, February 27, 2013; Sheet 34 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

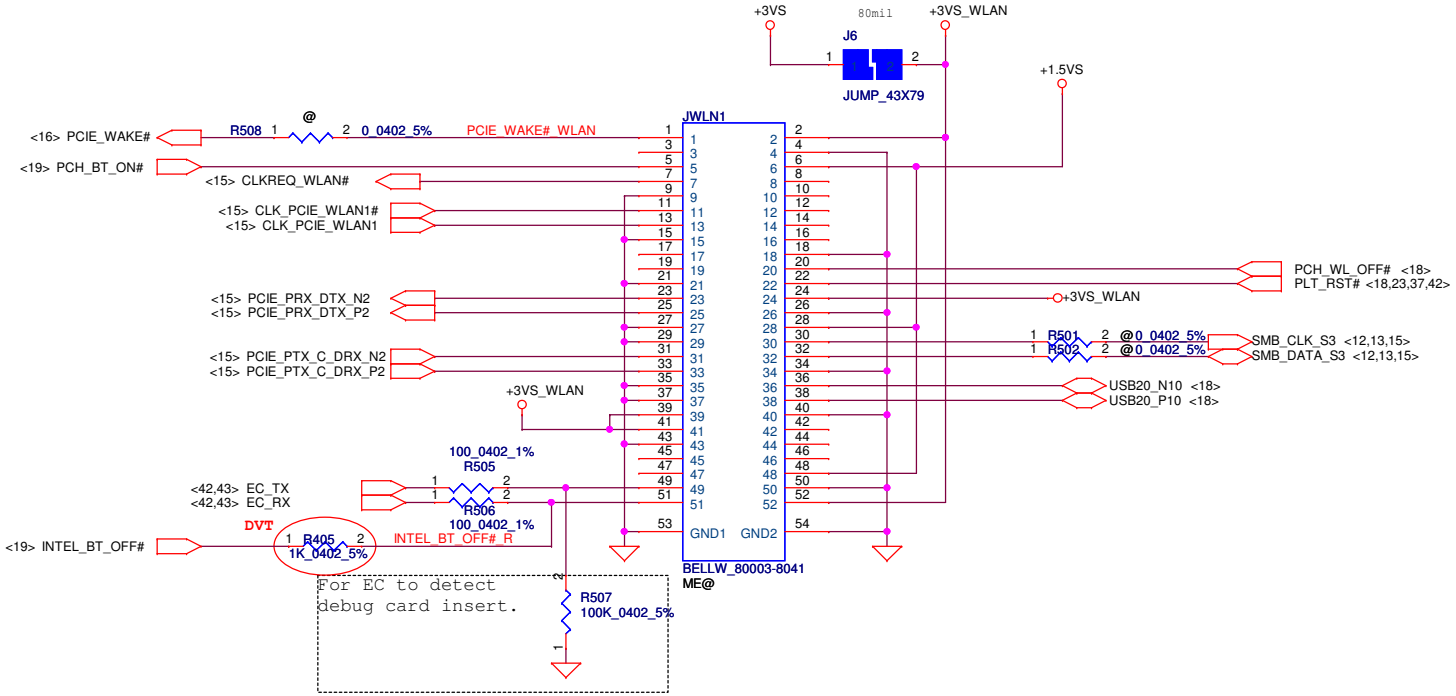
Compal Electronics, Inc.

Title: **HDMI CONN**

Size	Document Number	Rev
B	LA-9631P	1.0

Date: Wednesday, February 27, 2013 Sheet 35 of 60

Mini Card for WLAN/WiMAX(Half)



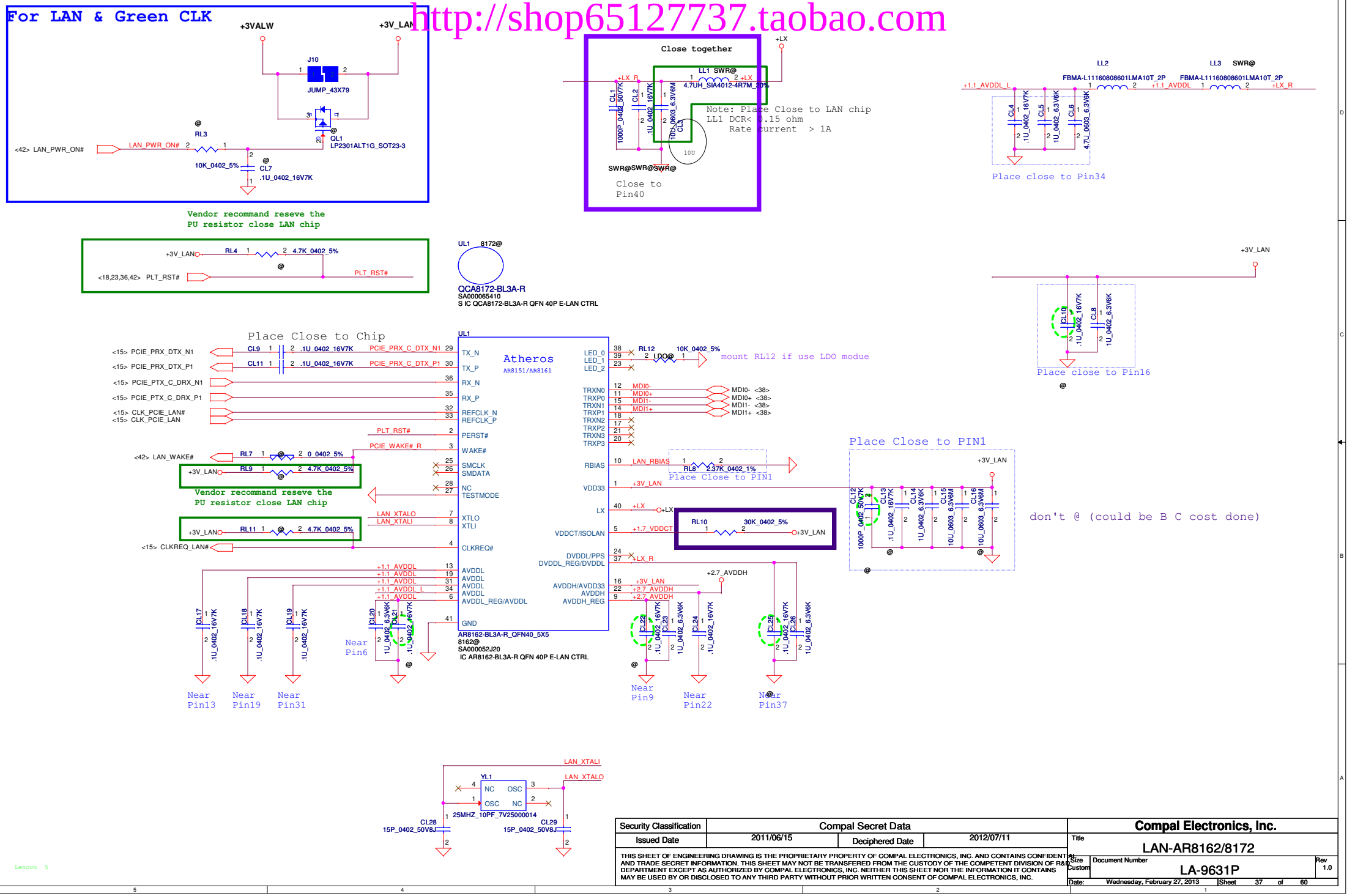
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **Mini-Card/NEW Card/SIM**

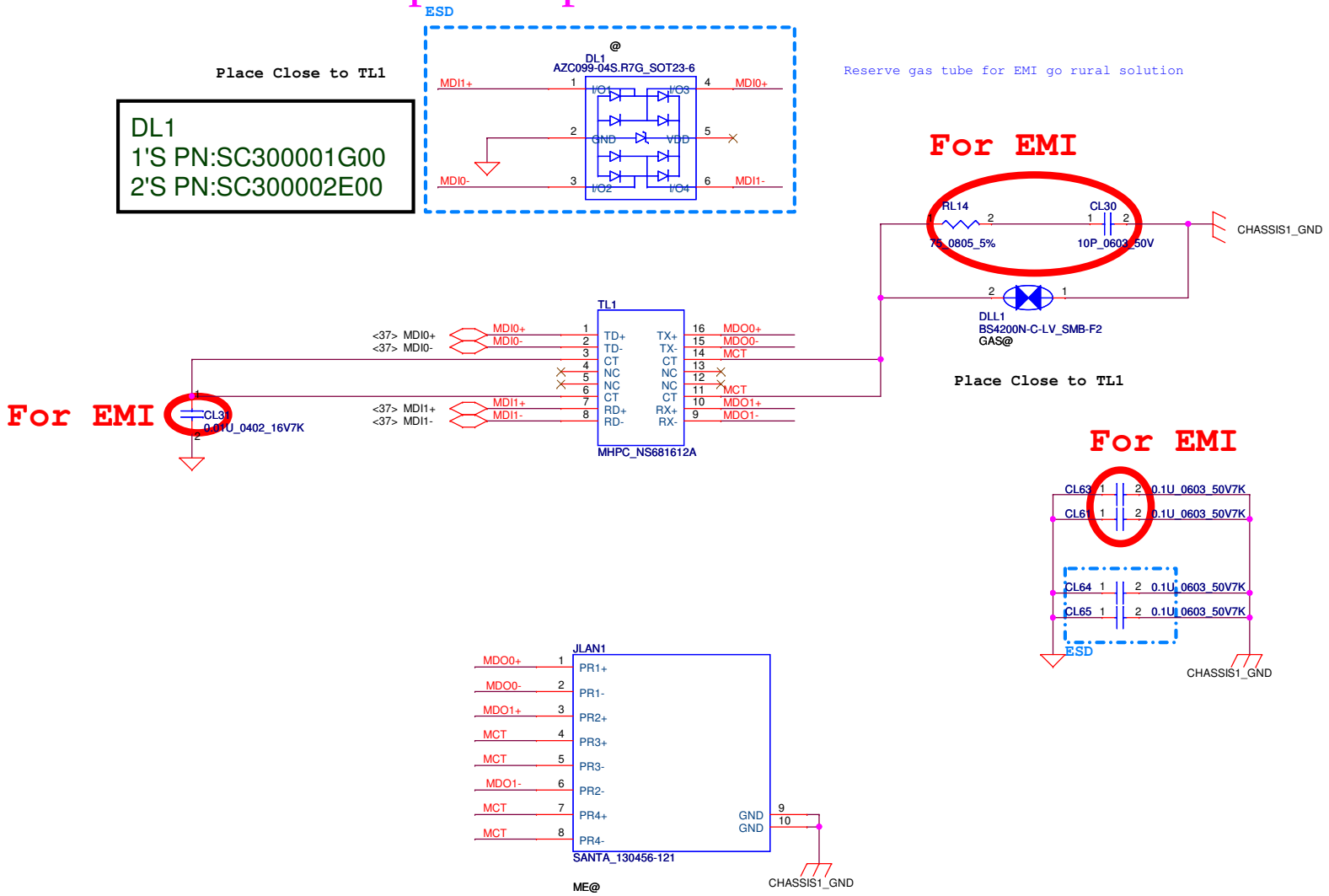
Size | Document Number: **LA-9631P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 36 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	LAN-AR8162/8172		
Size: Custom	Document Number: LA-9631P		Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 37 of 60		

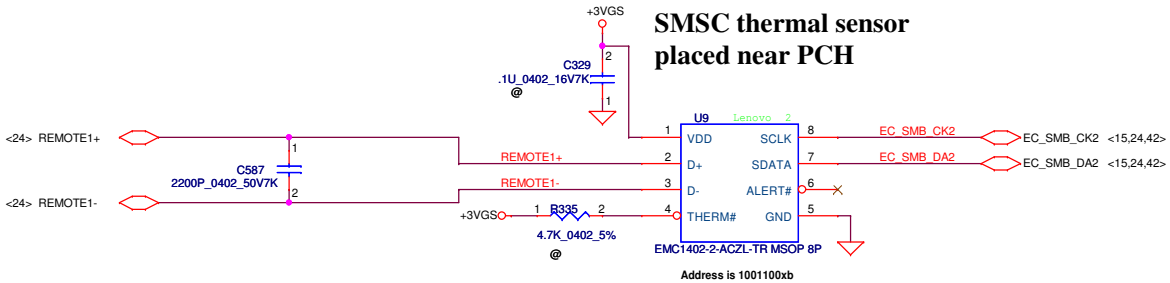


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	LAN_Transformer		
Size	Document Number		Rev
B	LA-9631P		1.0
Date:	Wednesday, February 27, 2013	Sheet	38 of 60

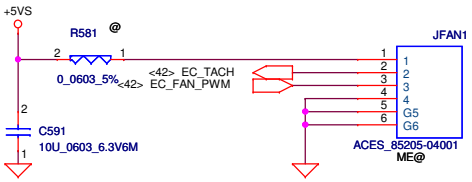
2 Channel

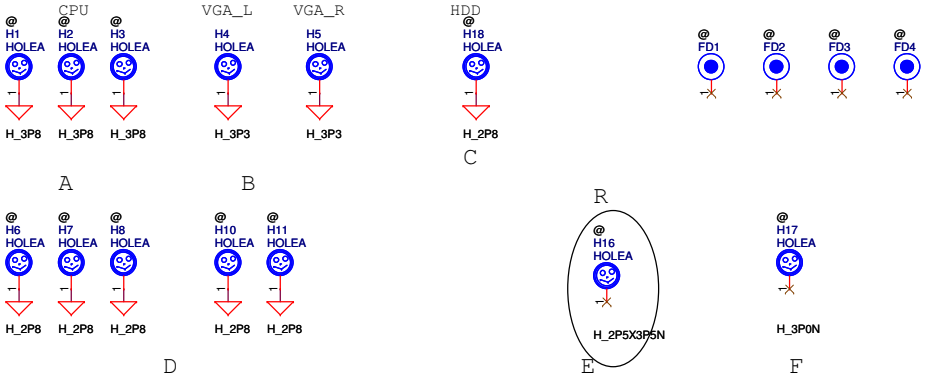
SMSC thermal sensor placed near PCH



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn





2P8 * 9 pcd

M/B 橢圓孔

M/B 圓孔

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

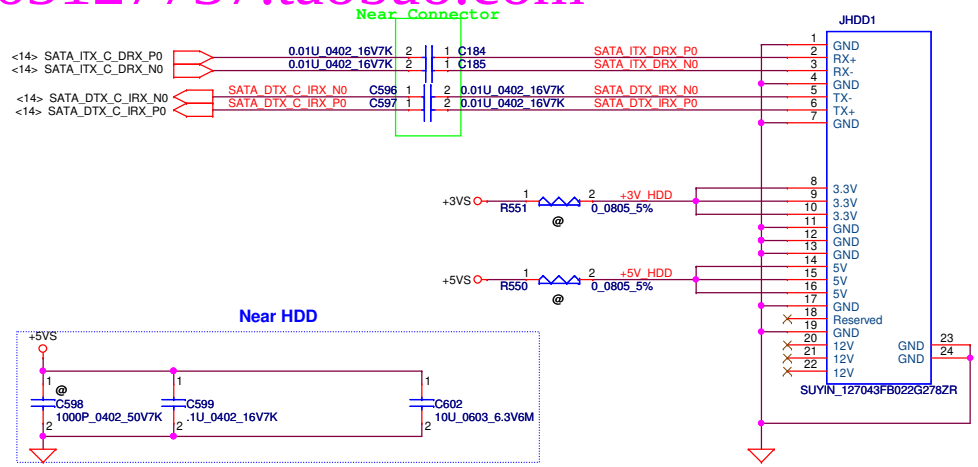
Compal Electronics, Inc.

Title: **Fintek-Thermal IC/FAN/screw**

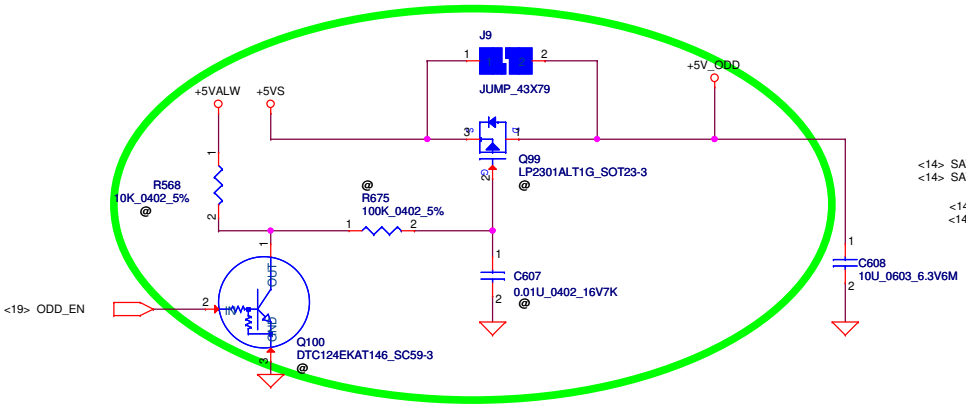
Size: Custom | Document Number: **LA-9631P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 39 of 60

SATA HDD Conn.

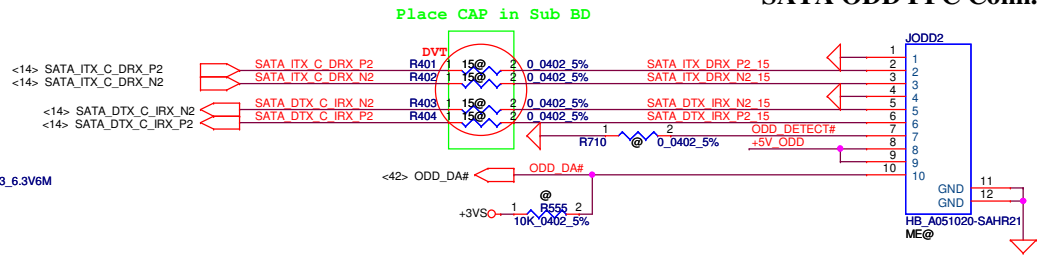


ODD Power Control



FOR 15"

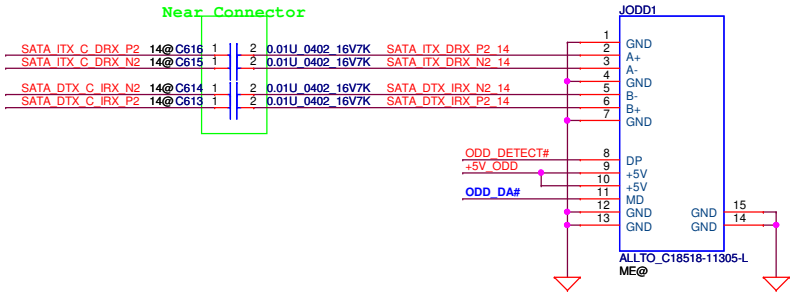
SATA ODD FFC Conn.



Co-lay

FOR 14"

SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **HDD/ODD/BT Connector**

Size	Document Number	Rev
Custom	LA-9631P	1.0

Date: Wednesday, February 27, 2013 Sheet 40 of 60

CX20751
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

Sense resistors must be connected same power that is used for VAUX_3.3

RA5 5.11K 0402 1% +3VS
RA6 10K_0402_1%
RA7 20K 0402 1%
RA8 39.2K 0402 1%
JSENSE PLUG_IN

mount RA6 on the Jack Sense circuit to configure Port-C for mono MIC.

Don't support LINE_IN function RA7 could be @

For Universal jack

+VREF_1V65
CA3 vendor suggest change to 2.2U
+LDO_OUT_3.3V
AVDD_3.3 pinis output of internal LDO. NOT connect to external supply.

+3VLP +3V_PCH +3V_AVDD_HP
+3VS
Should be same supply rail as used for PCH HDA bus controller section

Layout Note:Path from +5VS to LPWR_5.0 RPWR_5.0 must be very low resistance (<0.01 ohms)

+5VS
Please bypass caps very close to device.

ESD
RA15 4.7K_0402_5%
HDA_RST_AUDIO#
CA11 .1U_0402_16V7K

For EMI
CA7 22P_0402_50V8J
RA21 33_0402_5%

+LDO_1.8V
10 mils

UA1 CX20751-11Z_QFN40

<14> HDA_SYNC_AUDIO
<14> HDA_SDIN0
<14> HDA_SDOUT_AUDIO
<14> HDA_BITCLK_AUDIO
<14> HDA_RST_AUDIO#
RA9 33_0402_5%
<42> EC_MUTE#
PC_BEEP

Universal Jack
External MIC
Internal analog MIC
Headphone
Internal SPEAKER

For EMI
CA64 CA65 CA66 .1U_0402_16V7K

For EMI
HGNDA, HGNDB 80mils
APPLE_MIC NOKIA_MIC HP_L HP_R
RA16 RA12 RA13 RA14 100_0402_1% 15_0402_5%
CA28 CA27 2.2U_0402_6.3V6M
HGNDB HGNDA HPOUT_L HPOUT_R PLUG_IN
JHP1 SINGA_2SJ2352-000131F ME@

Combo Jack (Normal Open)

For Universal jack
MICB_L MICB_R +MICBIASB
RA17 RA18 100_0402_1%
RA20 3K_0402_5%
RA19 3K_0402_5%
CA36 CA46 2.2U_0402_6.3V6M
HP_L HP_R

SCHEMATIC

For EMI
HPOUT_L HPOUT_R HGNDB HGNDA
CA31 CA32 CA33 CA34 100P_0402_50V8J
DA1 DA2 AZ5125-02S.R7G_SOT23-3

ESD
HPOUT_L HPOUT_R HGNDB HGNDA
DA1 DA2 AZ5125-02S.R7G_SOT23-3

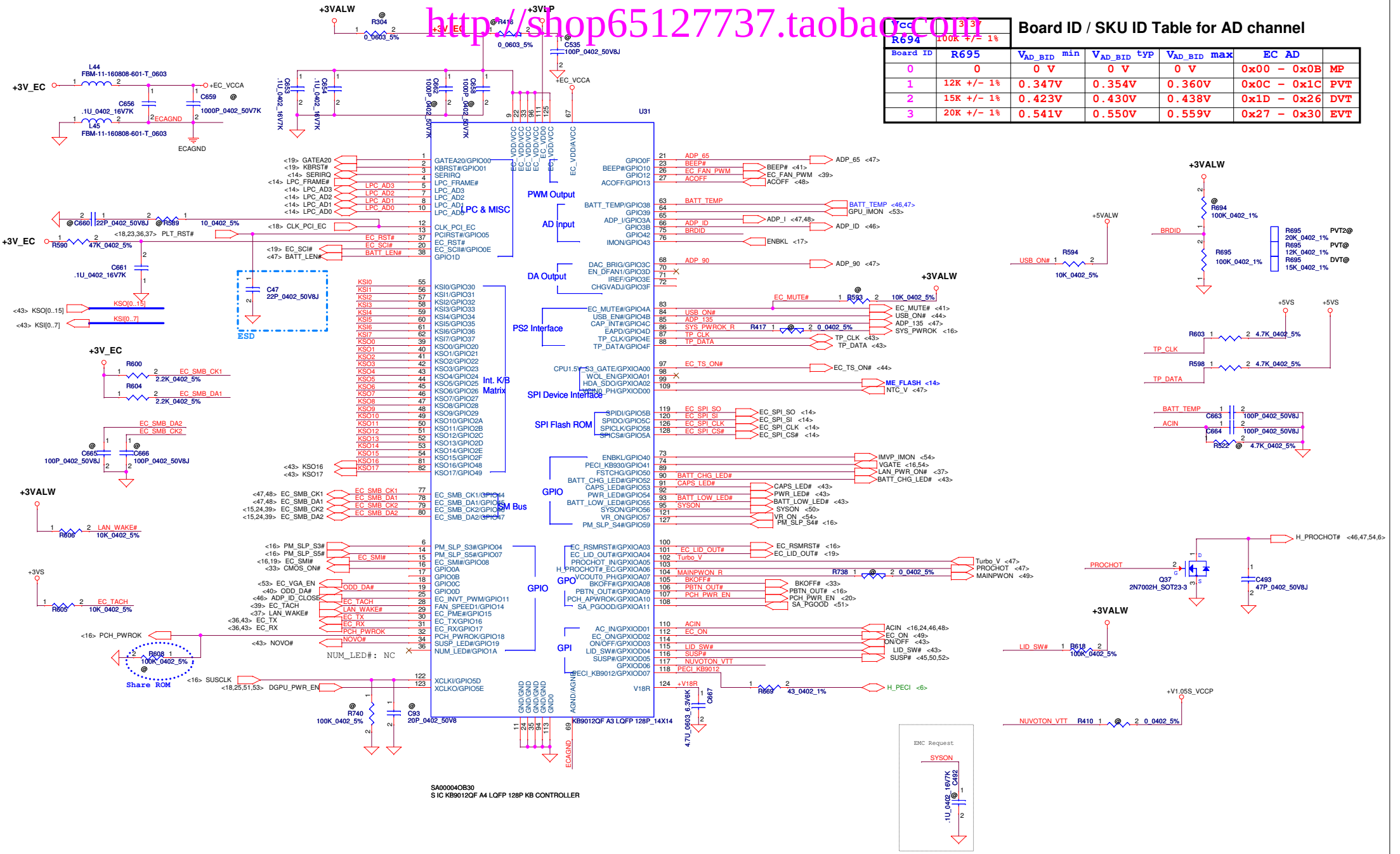
PC Beep
EC Beep
ICH Beep
<42> BEEP#
<14> HDA_SPKR
CA37 CA45 .1U_0402_16V7K
RA492 33_0402_5%
RA22 10K_0402_5%
PC_BEEP

Place colose to Codec chip
+MICBIASC
RA23 2.2K_0402_5%
CA41 1U_0603_10V4Z
MIC1 WM-64PCY_2P
MIC_IN GNDA
CA42 CA44 .1U_0402_16V7K

wide 20MIL
LA1 LA2 LA3 LA4 0_0603_5%
SPK_R1- SPK_R2+ SPK_L1- SPK_L2+
FCM1608CF-121T03 0603
SPK_R1- CONN SPK_R2+ CONN SPK_L1- CONN SPK_L2+ CONN
JSPK1 ME@

For EMI
CA38 CA39 CA40 CA43 100P_0402_50V7K

ESD
DA3 AZC099-04S.R7G_SOT23-6
ACES_85205-04001



Board ID / SKU ID Table for AD channel

R694 100K +/- 1%

Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0 V	0x00 – 0x0B	MP
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C – 0x1C	PVT
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D – 0x26	DVT
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 – 0x30	EVT

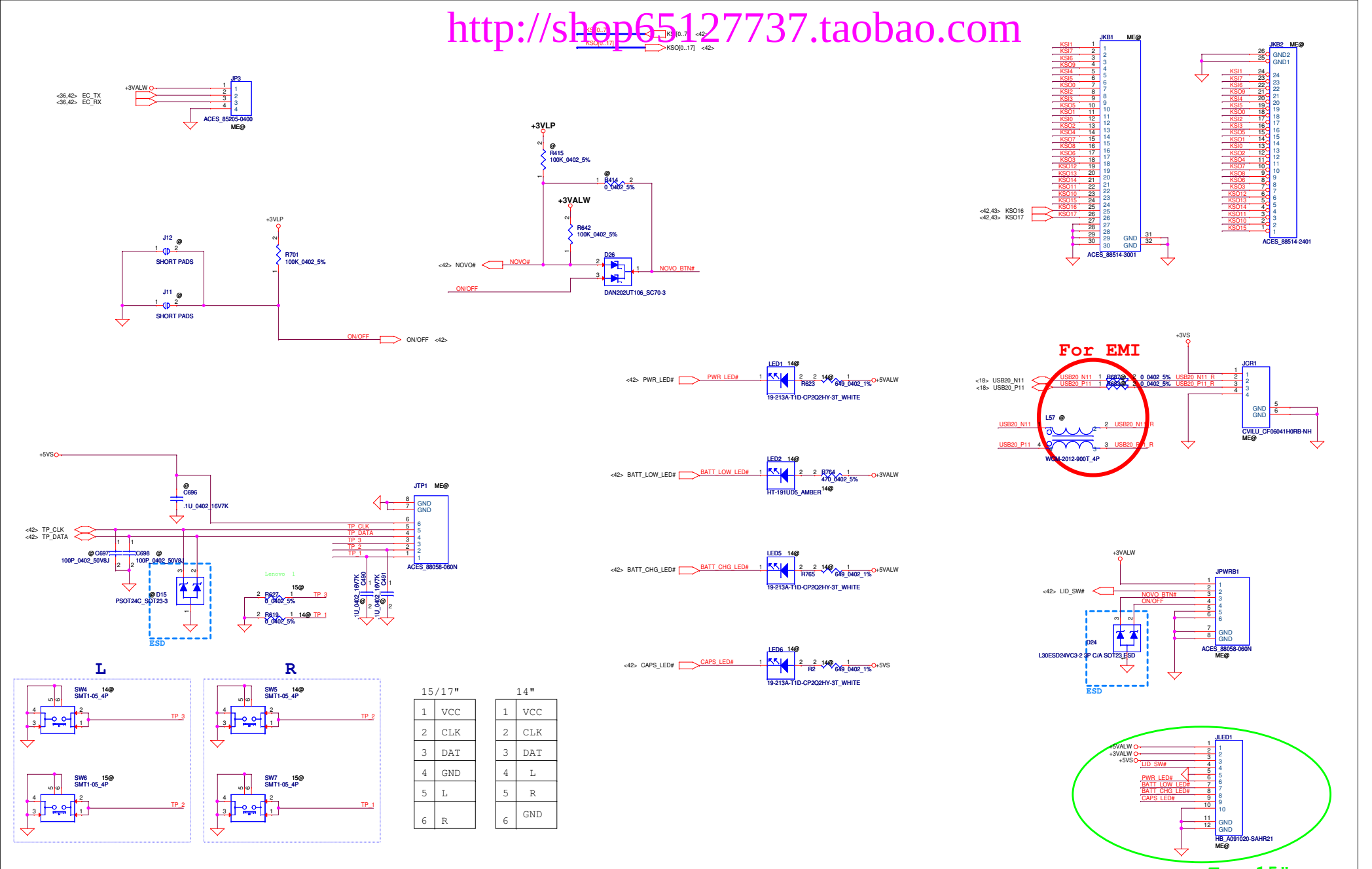
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: BIOS & EC I/O Port

Size	Document Number	Rev
Custom	LA-9631P	1.0

Date: Wednesday, March 06, 2013 Sheet 42 of 60



15/17"

1	VCC
2	CLK
3	DAT
4	GND
5	L
6	R

14"

1	VCC
2	CLK
3	DAT
4	L
5	R
6	GND

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

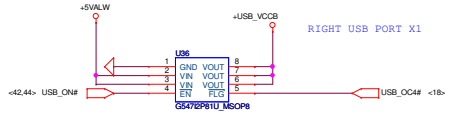
Compal Electronics, Inc.

Title: ROM/KBD/PWR/CR/LED/TP Conn.

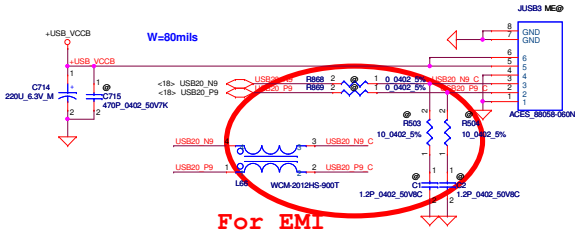
Size	Document Number	Rev
C	LA-9631P	1.0

Date: Wednesday, March 06, 2013 Sheet 43 of 60

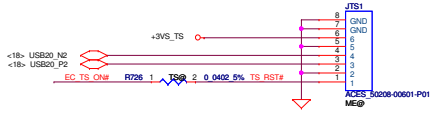
Ext. USB2.0

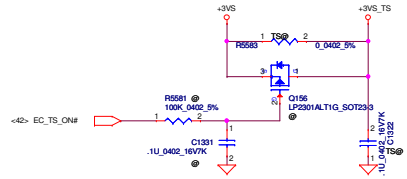


Right Ext.USB Conn.

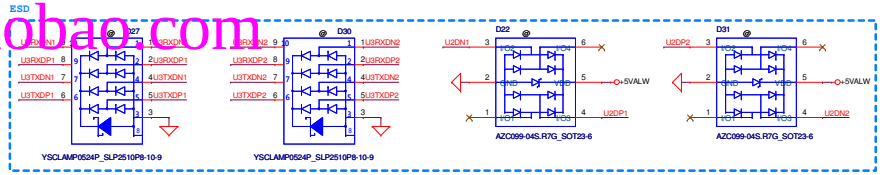


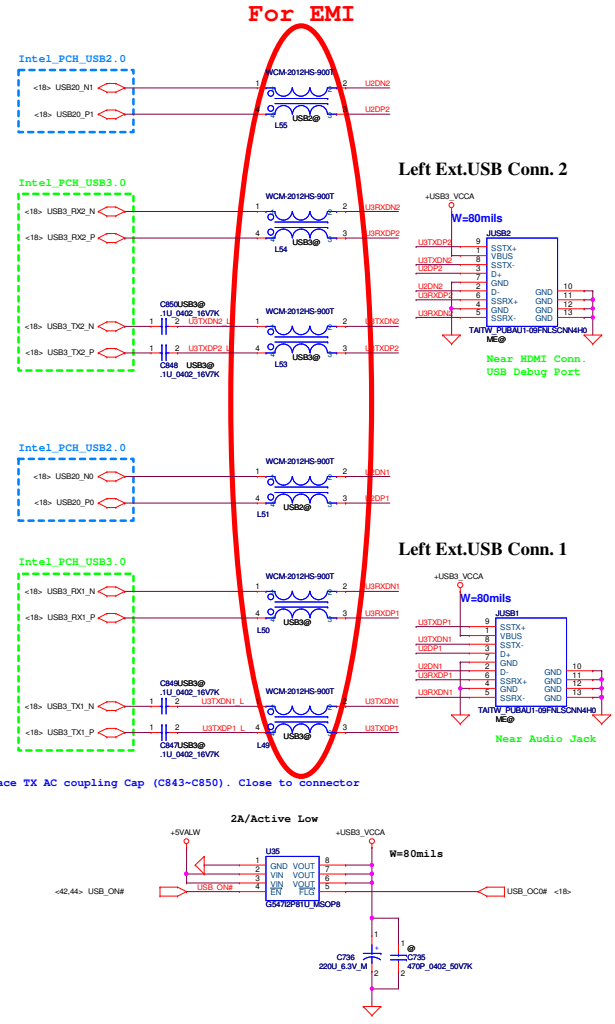
Touch Screen





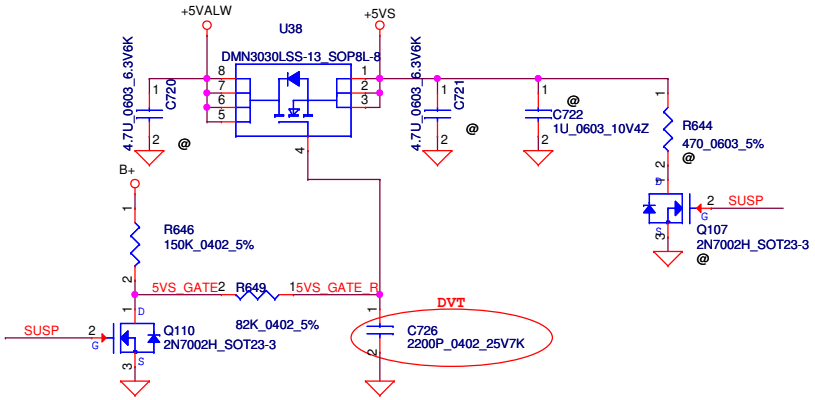
USB3.0



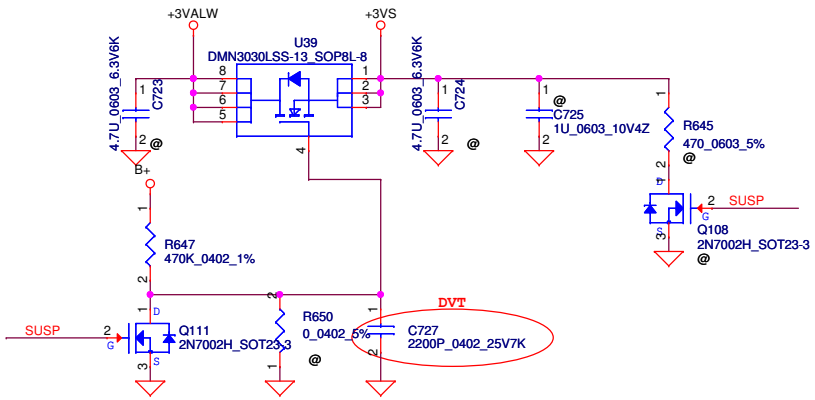


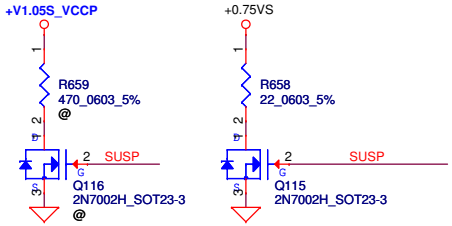
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date	2012/07/11
Title	USB3.0/Left USB Ports		
Size	Document Number		Rev 1.0
Date: Wednesday, February 27, 2013	Sheet 44 of 60		

+5VALW to +5VS

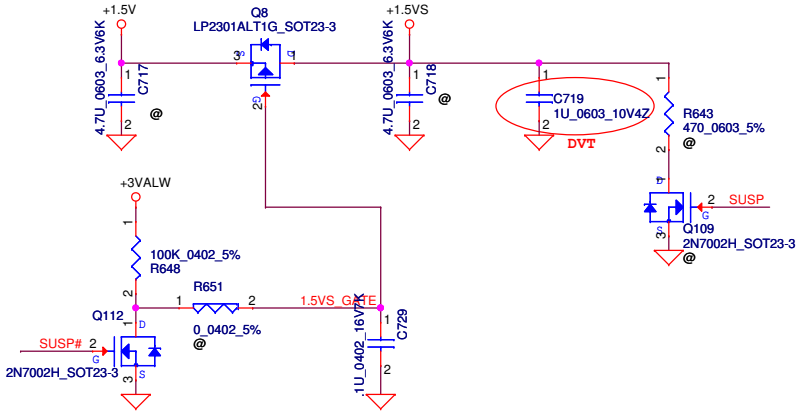


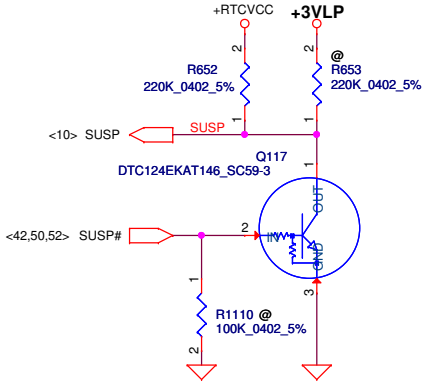
+3VALW to +3VS





+1.5V to +1.5VS





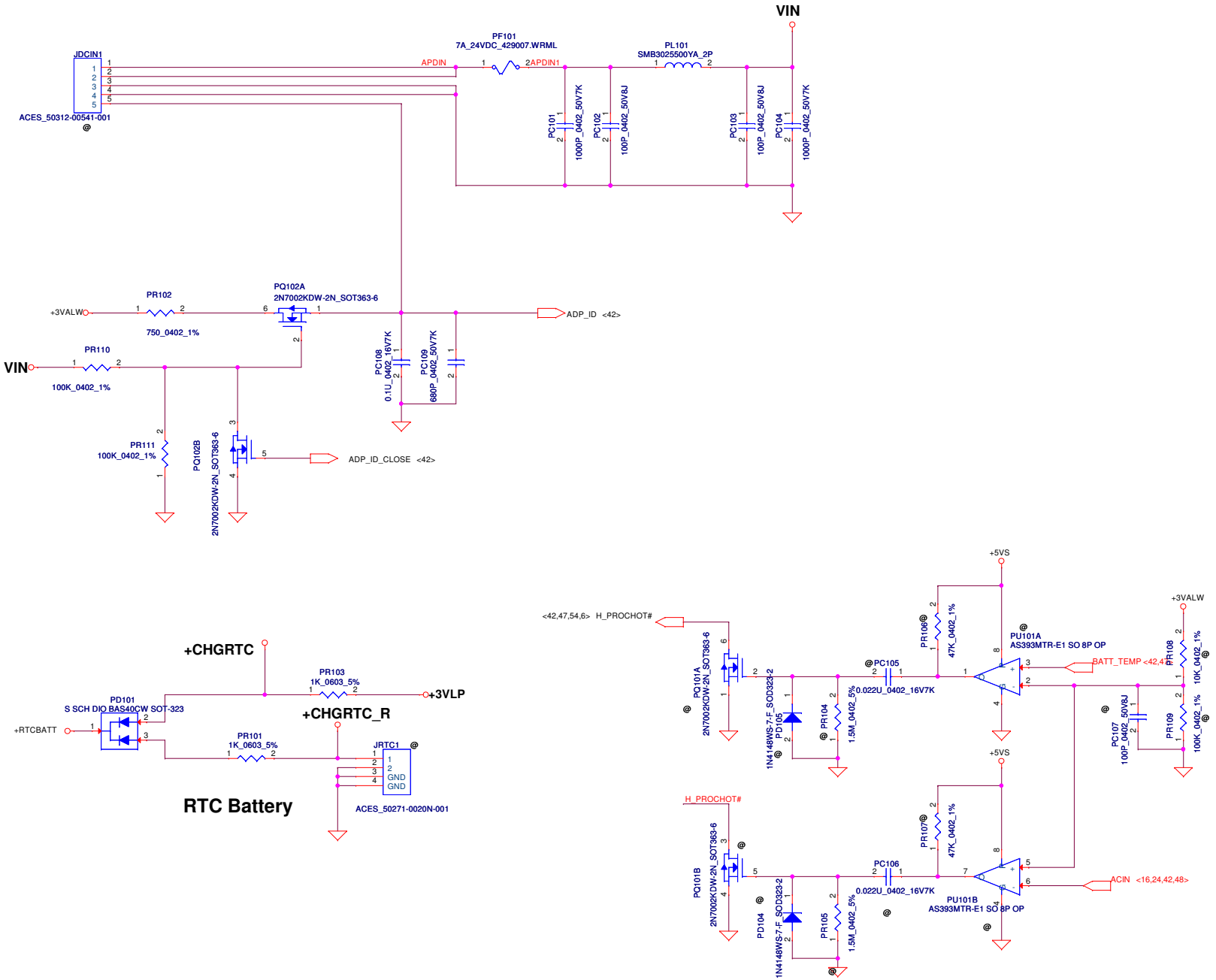
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-9631P	1.0

Date: Wednesday, February 27, 2013 Sheet 45 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR DCIN / RTC Battery

Size	Document Number	Rev
Custom	Gx00	1.0

Date: Wednesday, February 27, 2013 Sheet 46 of 60

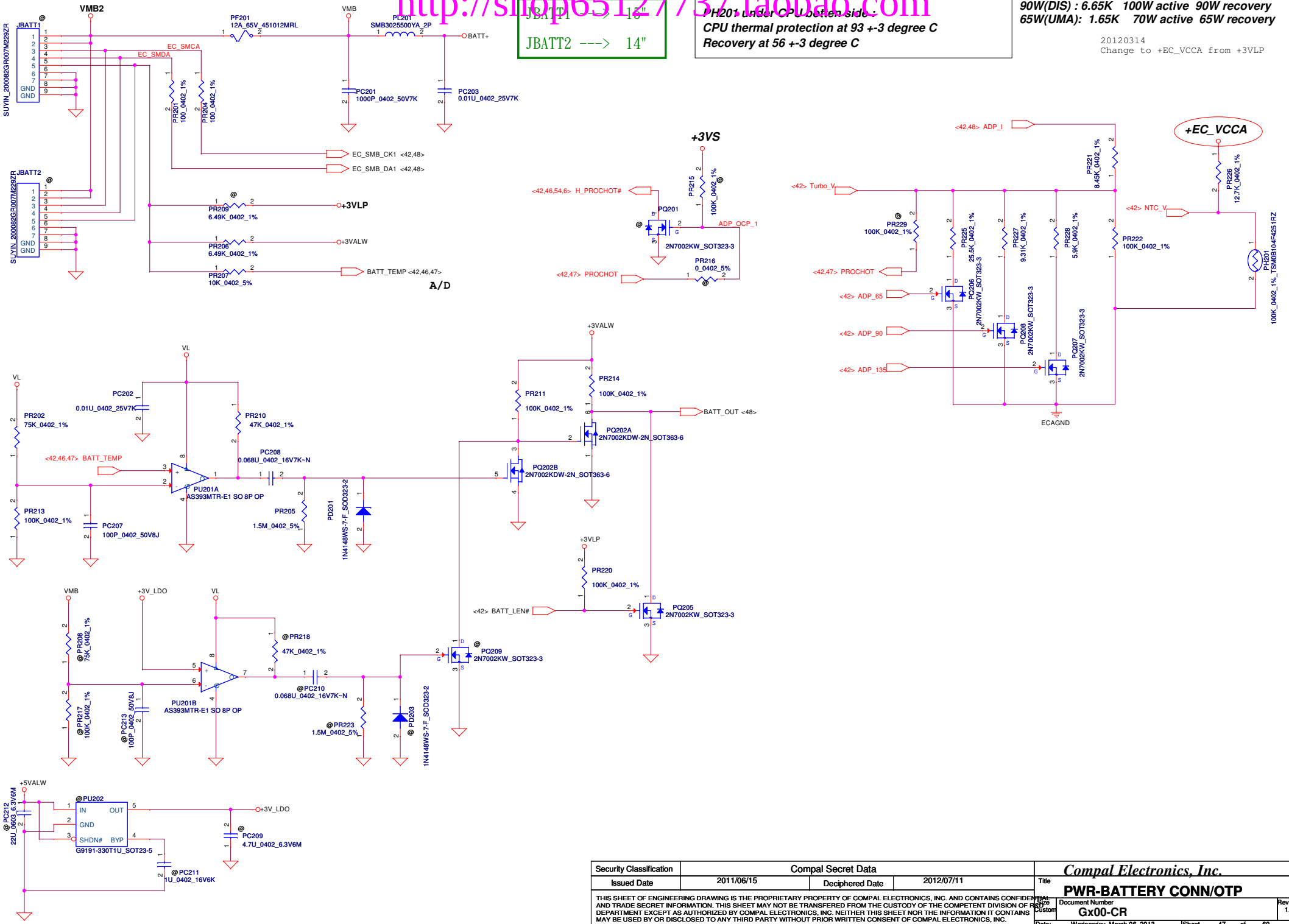
JBATT1 ---> 15"

JBATT2 ---> 14"

PH201 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

90W(DIS) : 6.65K 100W active 90W recovery
65W(UMA): 1.65K 70W active 65W recovery

20120314
Change to +EC_VCCA from +3VLP



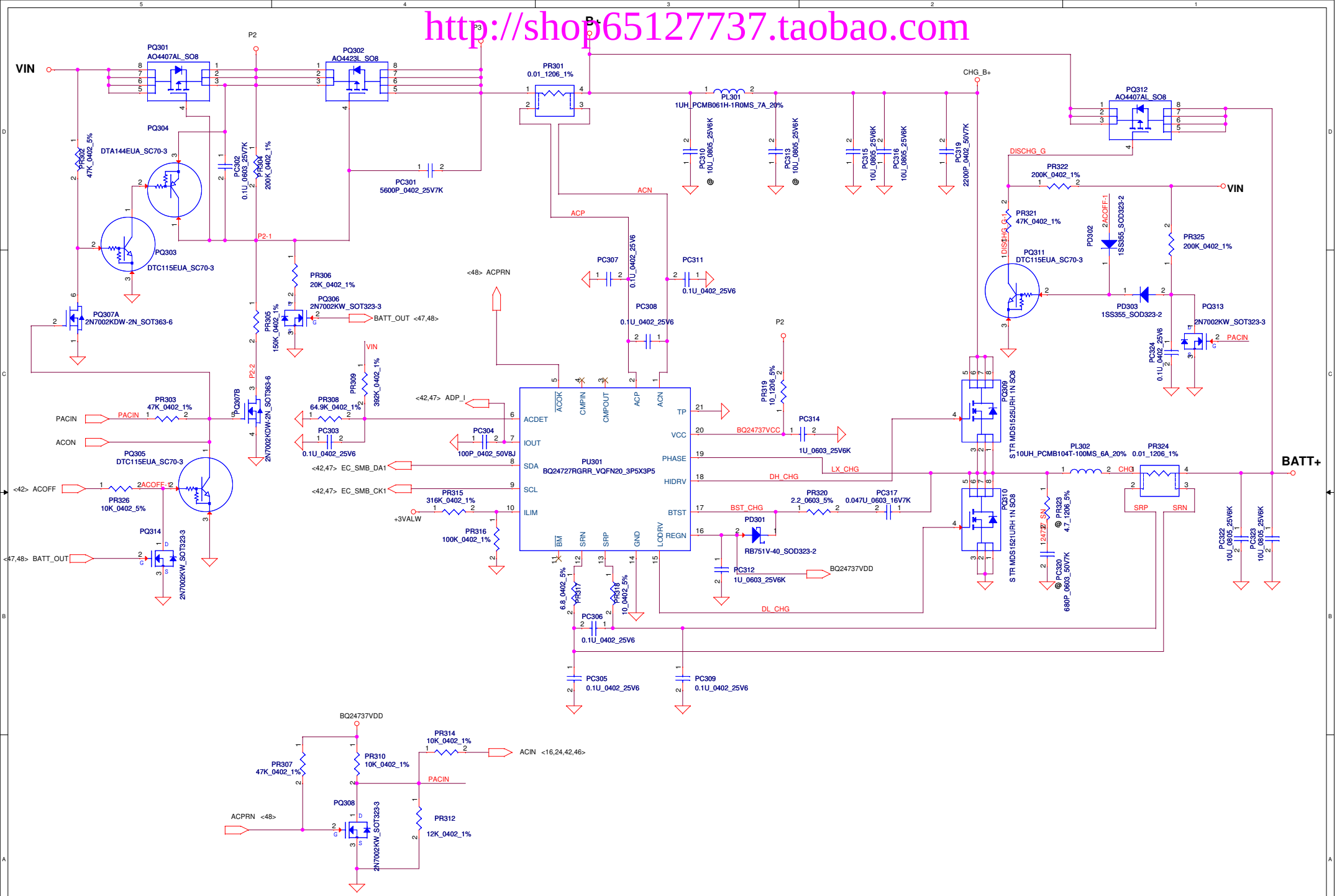
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 06, 2013 | Sheet 47 of 60



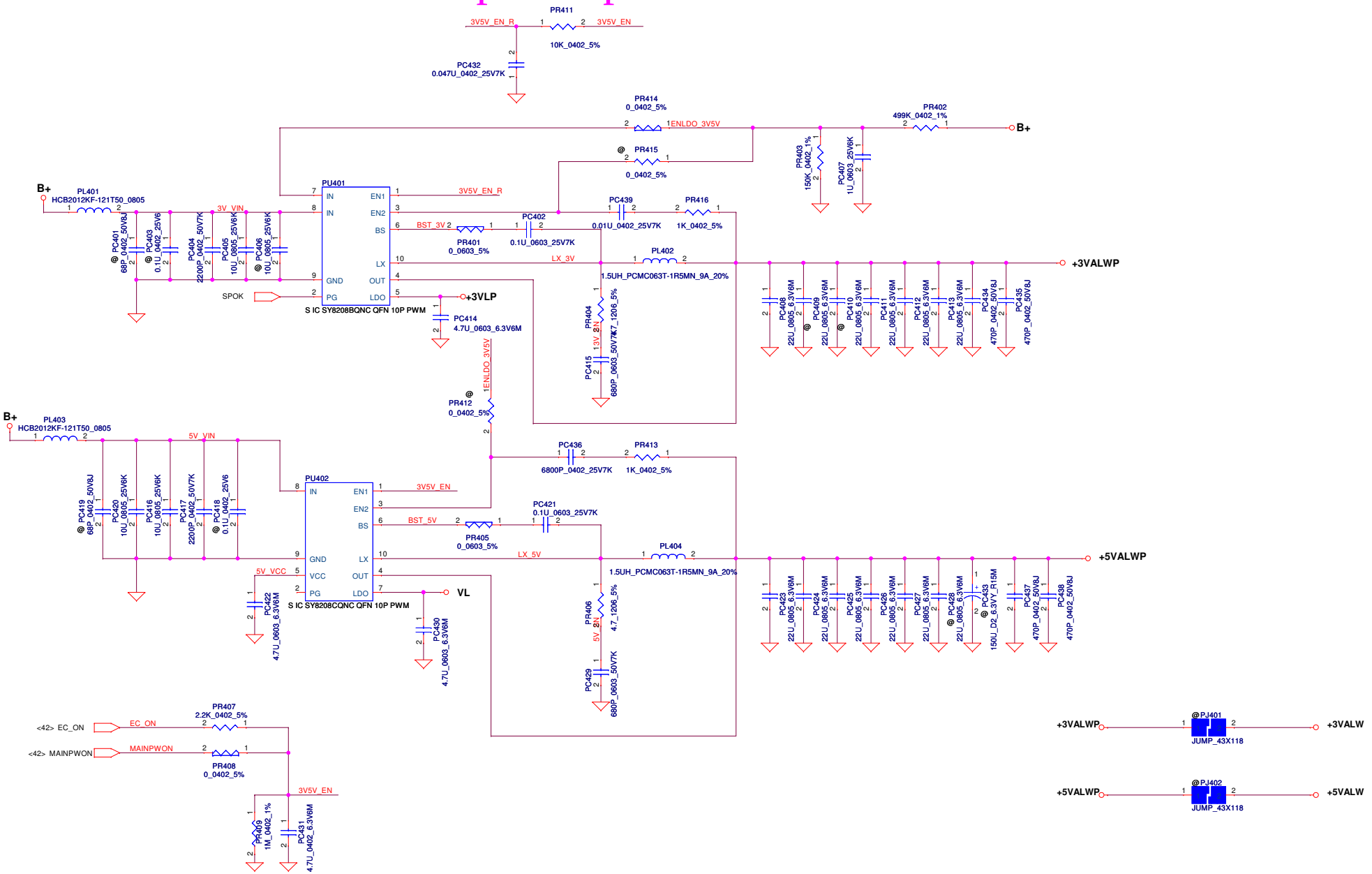
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
	Gx00-CR	1.0

Date: Wednesday, February 27, 2013 | Sheet 48 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

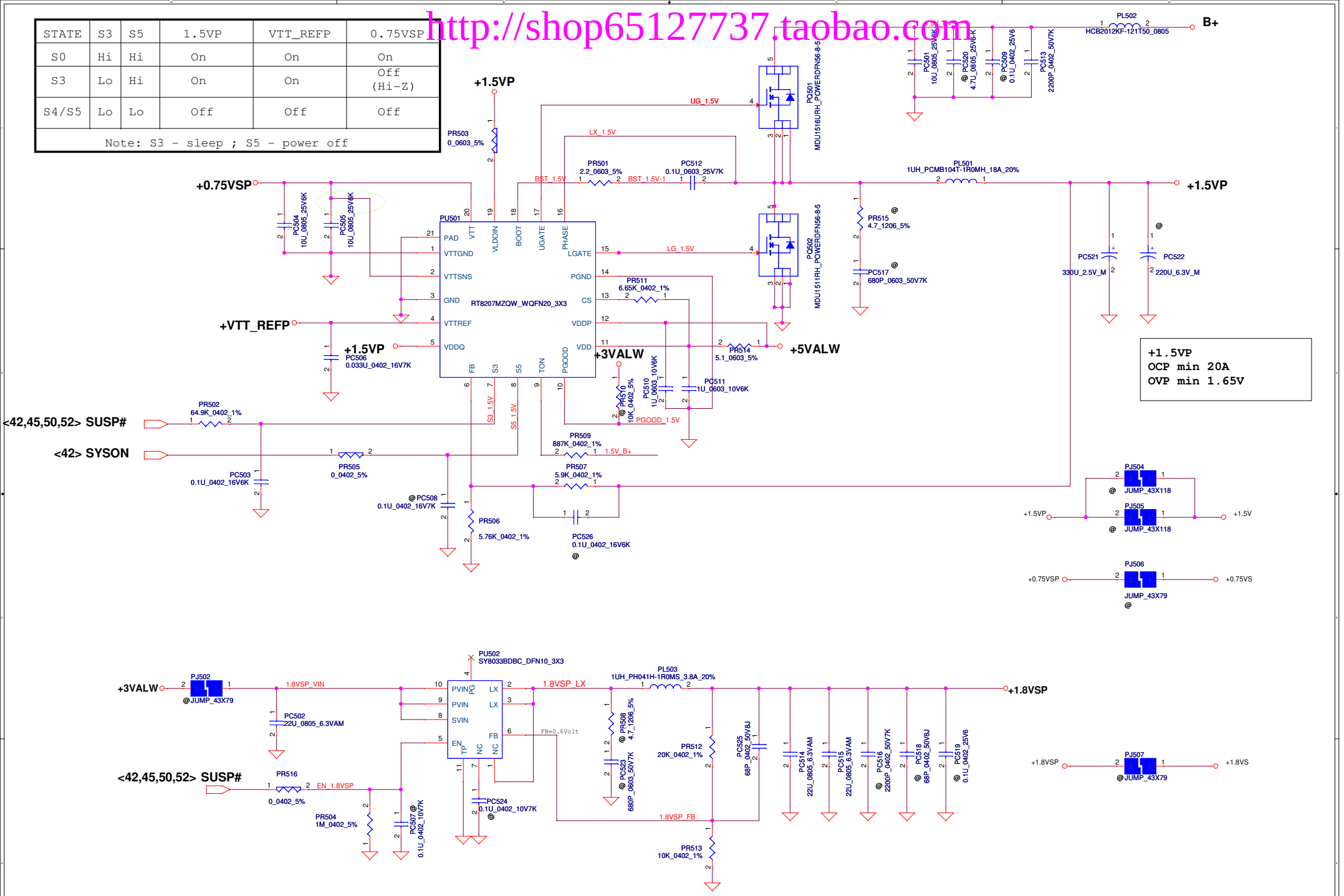
Title: +1.05VS_VCCP

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 49 of 60

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +1.5VP/+1.8VSP

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 50 of 60

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCCSAP — PJ601 JUMP_43X118 — +VCCSA

+V1.05S_VCCP — PR613 0.005_1206_1% — +VCCSA

+3VALW — PJ602 JUMP_43X79 — +VCCSA_PWR_SRC

PC608 22U_0805_6.3V6M

PC601 22U_0805_6.3V6M

PC602 68P_0402_50V8J — FB_VCCSA_IC

SY8037BDCC_DFN12_3X3

PU601

PVIN PVIN SVIN FB VOUT VID1 LX LX LX PG EN VID0 GND

+VCCSA_PHASE

SA_PGOOD <42>

PR601 100K_0402_5% — +3VS

@ PR614 0_0402_5%

+V1.05S_VCCP_PWRGOOD <52>

PR603 0_0402_5%

PR608 1M_0402_5%

@ PC606 .1U_0402_16V7K

H_VCCSA_VID0 <10>

PR604 1K_0402_5%

PR605 1K_0402_5%

H_VCCSA_VID1 <10>

FB_VCCSA

PL601 0.47UH_FDVE0630-H-R47M=P3_17.7A_20% — +VCCSAP

@ PR602 4.7_0603_5%

@ PC605 680P_0402_50V7K

PC603 22U_0805_6.3V6M

PC604 22U_0805_6.3V6M

PC607 22U_0805_6.3V6M

PC609 22U_0805_6.3V6M

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

PR606 100_0402_1%

PR607 0_0402_5% — +VCCSA_SENSE <10>

PR612 82.5K_0402_1% — DGPU_PWR_EN <18,25,42,53>

PR616 1M_0402_1%

PC637 0.1U_0402_25V6

@ PR610 4.7_1206_5%

@ PC634 680P_0603_50V7K

2SNB_0.95V

+0.95VGSP — PJ606 JUMP_43X118 — +0.95VGS

PL606 HCB2012KF-121T50_0805

B+

PC621 220P_0402_50V7K

@ PC636 0.1U_0402_25V6

10U_0805_25V6K PC627

B+_0.95V

PU604

IN GND BS LX EN FB BYP LDO ILMT PG

PC632 0.1U_0603_25V7K

PL605 1UH_PCMB063T-1R0MS_12A_20%

+0.95VGSP

+3VS — @ PR618 0_0402_5% — ILMT_0.95V — PR609 1M_0402_5%

+3VS — @ PR617 100K_0402_5% — PGD_0.95V

ILMT_0.95V

+3VALW

PC630 4.7U_0603_6.3V6K

PC628 4.7U_0603_6.3V6K

PR611 78.7K_0402_1%

PC635 220P_0402_50V7K

@ PC629 47U_0805_6.3V6M

PC633 47U_0805_6.3V6M

PC631 22U_0805_6.3V6M

PC622 22U_0805_6.3V6M

PR615 133K_0402_1%

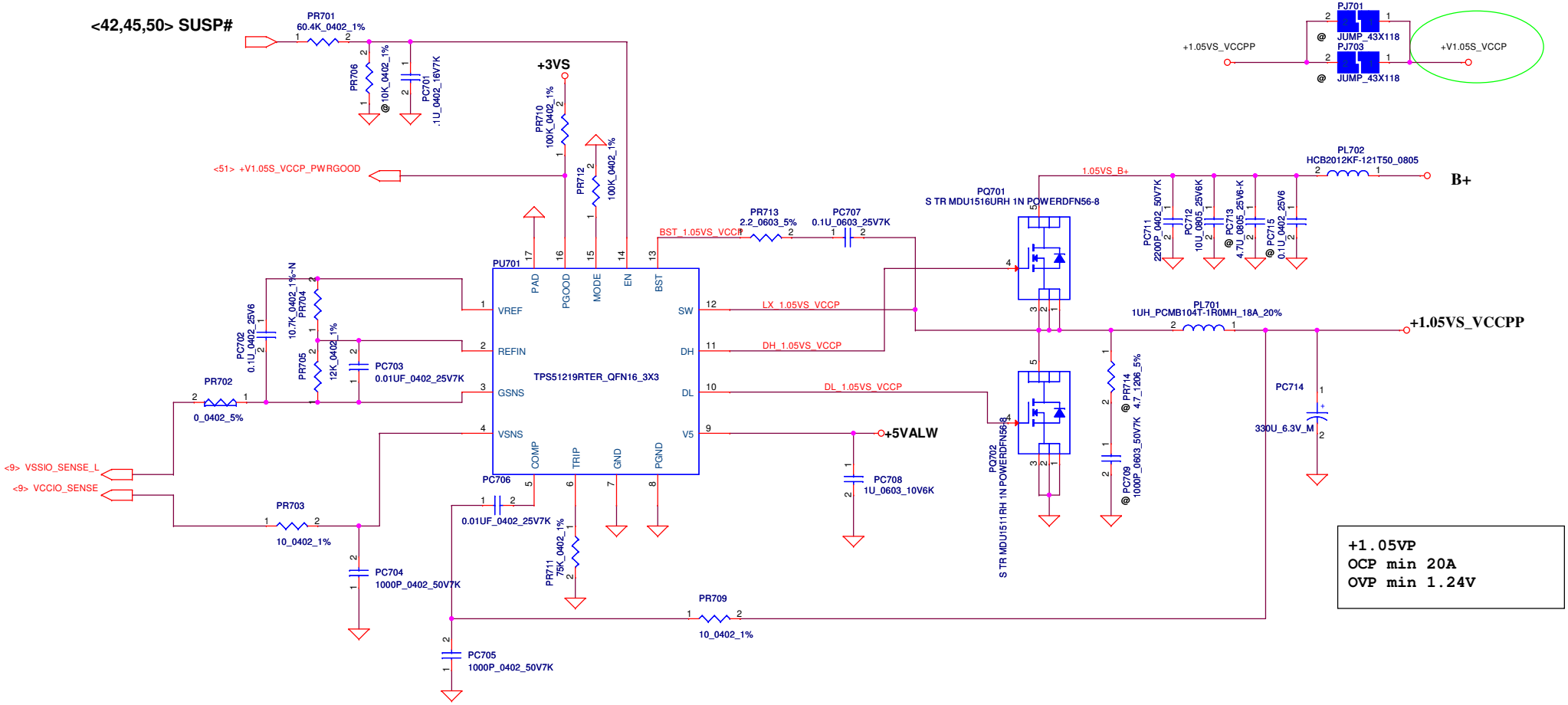
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +VCCSAP

Size	Document Number	Rev
C	Gx00-CR	1.0

Date: Wednesday, February 27, 2013 Sheet 51 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

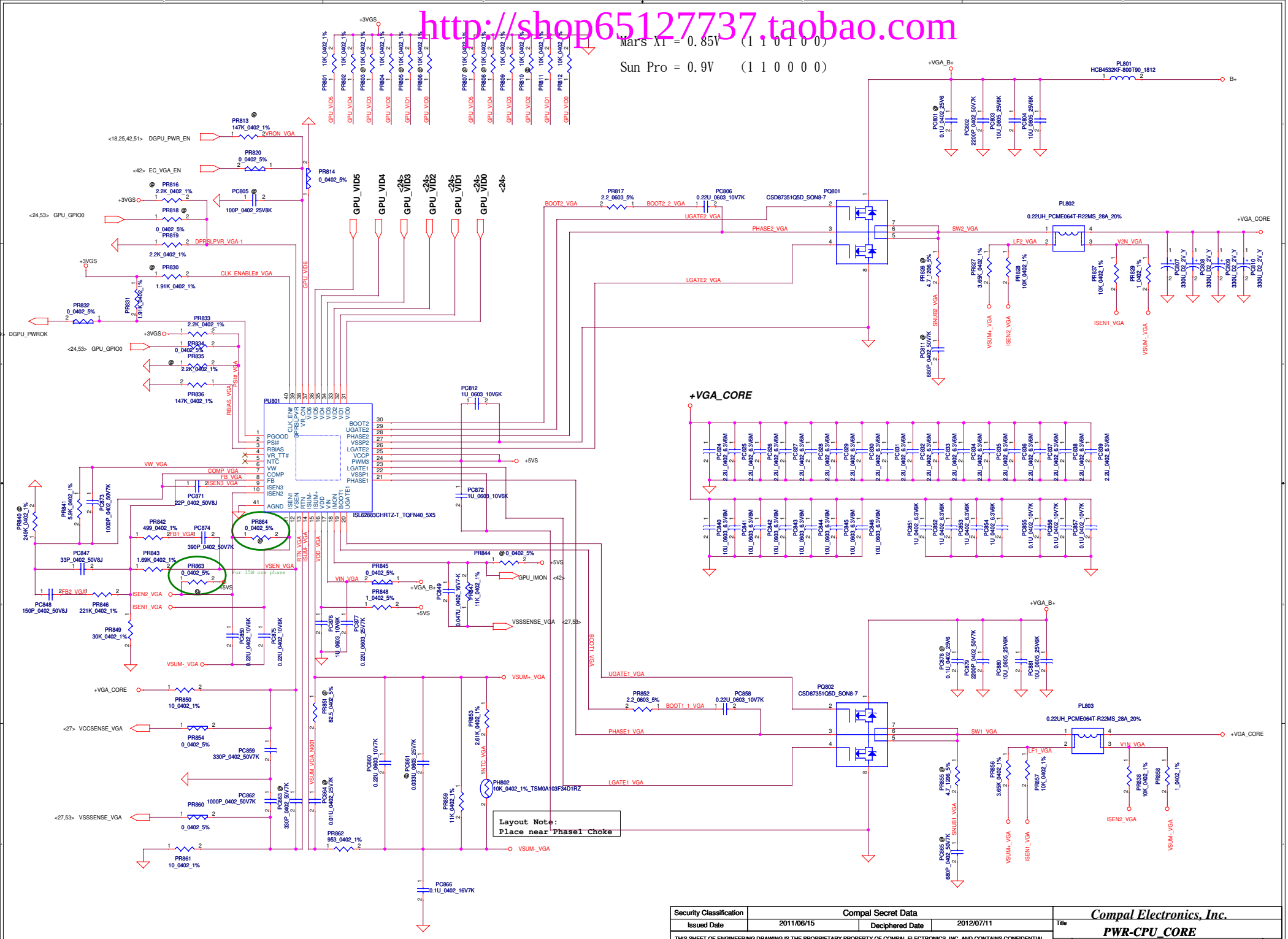
Title: +1.05VS_VCCP

Size	Document Number	Rev
Custom	Gx00-CR	1.0

Date: Wednesday, February 27, 2013 Sheet 52 of 60

Mars XT = 0.85V (1 1 0 1 0 0)

Sun Pro = 0.9V (1 1 0 0 0 0)



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: **PWR-CPU_CORE**

Size	Document Number	Rev
C	Gx00-CR	1.0

Date: Wednesday, February 27, 2013 Sheet 53 of 60

PR915,PR946=200K(setting 113 degreeC)
PR915,PR946=8.25K(setting 93 degreeC)

Switching Frequency = 450KHz

NCP6132AMNR2G_QFN60_7X7

PUT COLSE TO GT Inductor

PUT COLSE TO V_GT HOT SPOT

PUT COLSE TO VCORE Phase 1 Inductor

PUT COLSE TO VCORE HOT SPOT

Option for 1 phase GFX — 2Phase: @ 1Phase: install

Option for 2 phase CPU — 3Phase: @ 2Phase: install

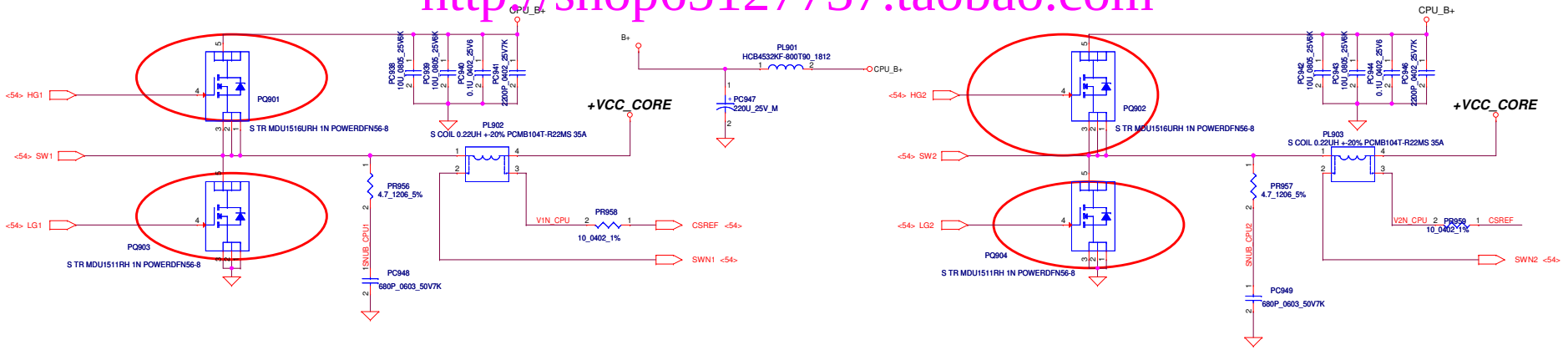
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-CPU_CORE

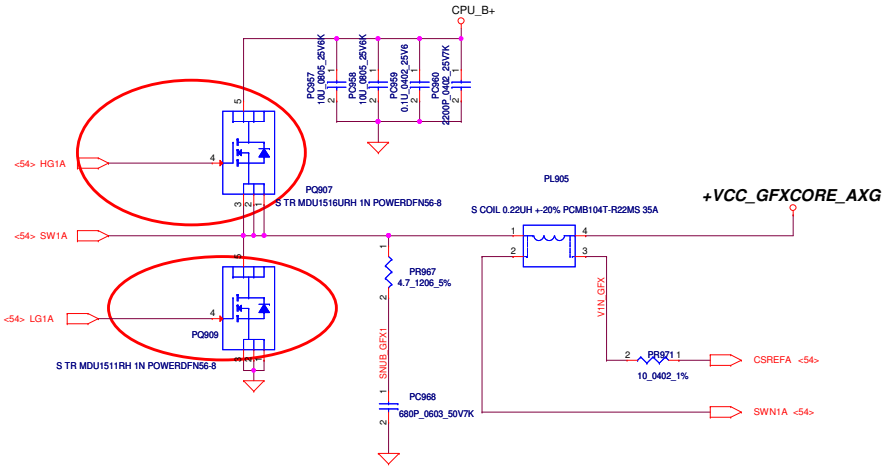
Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 54 of 60



QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	PWR-CPU_CORE		
Size C	Document Number Gx00-CR		Rev 1.0
Date: Wednesday, February 27, 2013	Sheet 55 of 60		

+VCC_CORE

PC1 10U_0805_6.3VAM
PC2 10U_0805_6.3VAM
PC3 10U_0805_6.3VAM
PC4 10U_0805_6.3VAM
PC5 10U_0805_6.3VAM
PC6 10U_0805_6.3VAM
PC7 10U_0805_6.3VAM
PC8 10U_0805_6.3VAM
PC9 10U_0805_6.3VAM
PC10 10U_0805_6.3VAM

+VCC_CORE

PC20 22U_0805_6.3V6M
PC21 22U_0805_6.3V6M
PC22 22U_0805_6.3V6M
PC23 22U_0805_6.3V6M
PC24 22U_0805_6.3V6M
PC44 22U_0805_6.3V6M
PC45 22U_0805_6.3V6M
PC46 22U_0805_6.3V6M
PC47 22U_0805_6.3V6M
PC48 22U_0805_6.3V6M
PC61 22U_0805_6.3V6M
PC62 22U_0805_6.3V6M
PC63 22U_0805_6.3V6M
PC64 22U_0805_6.3V6M
@
@ PC71 22U_0805_6.3V6M
@ PC72 22U_0805_6.3V6M

+VCC_CORE

PC73 330U_D2_2V_Y
PC74 330U_D2_2V_Y
PC76 330U_D2_2V_Y
PC77 330U_D2_2V_Y
PC78 330U_D2_2V_Y
@

+VCC_GFXCORE_AXG

+VCC_GFXCORE_AXG

PC13 22U_0805_6.3V6M
PC15 22U_0805_6.3V6M
PC17 22U_0805_6.3V6M
PC18 22U_0805_6.3V6M
PC19 22U_0805_6.3V6M @
PC36 22U_0805_6.3V6M
PC38 22U_0805_6.3V6M @
PC39 22U_0805_6.3V6M
PC40 22U_0805_6.3V6M
PC41 22U_0805_6.3V6M
PC42 22U_0805_6.3V6M
PC43 22U_0805_6.3V6M
PC58 330U_D2_2V_Y
PC59 330U_D2_2V_Y

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

+V1.05S_VCCP

+V1.05S_VCCP

PC27 22U_0805_6.3V6M
PC28 22U_0805_6.3V6M
PC29 22U_0805_6.3V6M
PC30 22U_0805_6.3V6M
PC31 22U_0805_6.3V6M
PC32 22U_0805_6.3V6M
PC33 22U_0805_6.3V6M
PC50 22U_0805_6.3V6M
PC51 22U_0805_6.3V6M
PC52 22U_0805_6.3V6M
PC53 22U_0805_6.3V6M
PC56 22U_0805_6.3V6M
@ PC66 330U_D2_2V_Y
PC67 330U_D2_2V_Y

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	LA-9631P	1.0

Date: Wednesday, February 27, 2013 Sheet 56 of 60

VIWGP/R PWR PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			EVT TO DVT
1	P.46	Add PR102,PC108,PC109	For ADP_ID pin detect
2	P.47	Add PR225,PR227,PR228,PQ206,PQ207,PQ208	For protect adapter function
3	P.49	Add PR410,PC433	For 3VALWP/5VALWP sequence
4	P.49	Add PC434,PC435,PC436,PC437	For EMI solution
5	P.49	Add PC432 and change PL404 from 1.5uH to 3.3uH	For improve output voltage ripple
6	P.50	Change PR502 from 49.9k to 64.9k	For +0.75VSP sequence
7	P.51	Add PC637	For +0.95VGSP sequence
8	P.54	Change PC907,PR912,PR927,PC928	For CPU Transient Compensation
			PVT TO PVT2
9	P.48	Add PR326 and PQ314	For battery health function
10	P.49	Add PR411,PC432	To delay +3VALW enable. PR411 change to 10K and PC432 change to 0.047uF
11	P.49	Change PC439 from 4700P to 10nF ,PC436 from 47nF to 6.8nF	Adjust +3VALW and +5VALW rising time.
12	P.51	Add PR614	For Celeron CPU SA_PGOOD
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			

Compal Electronics, Inc.

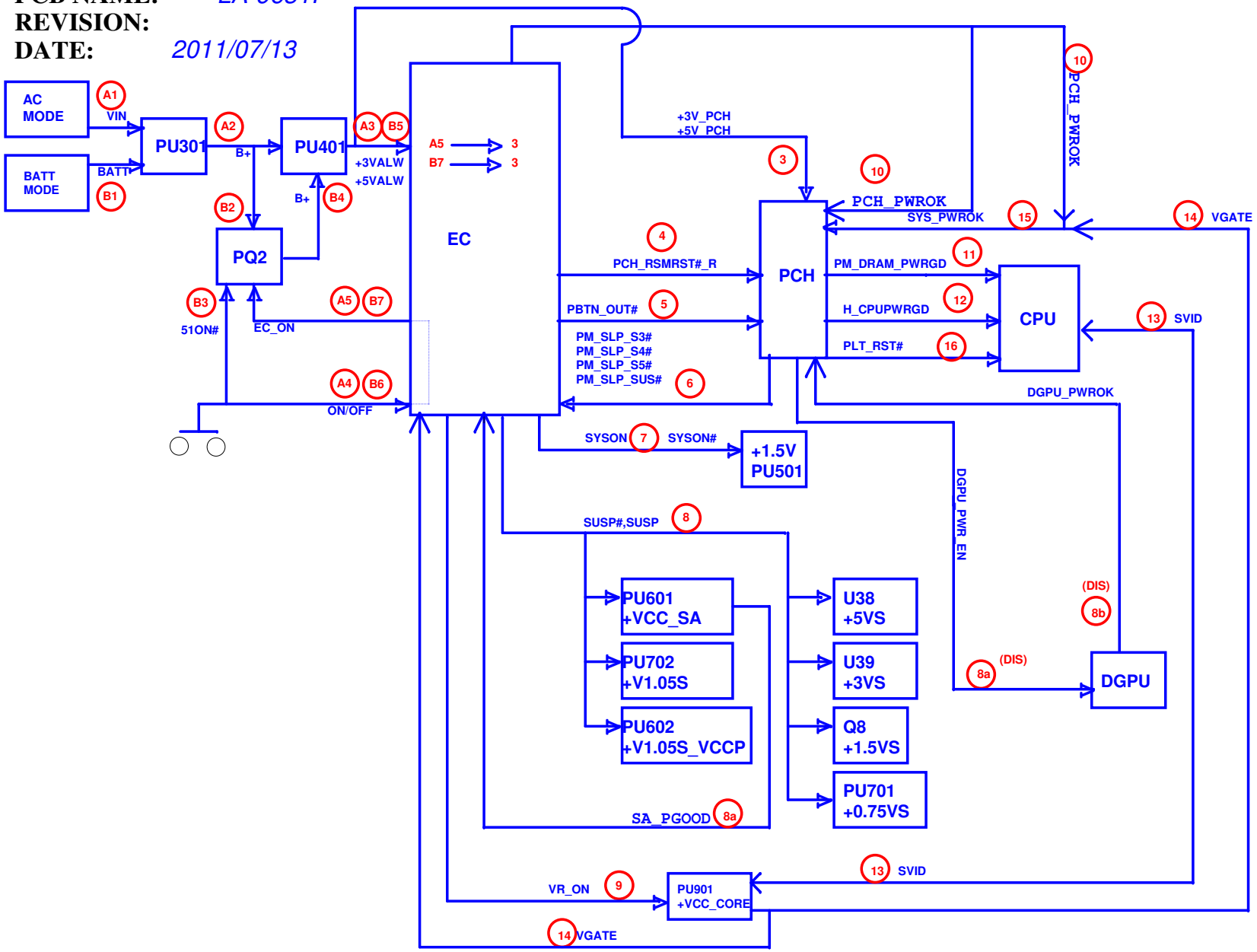
Title: HW-PIR1

Size: Custom | Document Number: LA-9631P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 57 of 60

COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-9631P*
REVISION:
DATE: *2011/07/13*



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ***Power sequence***

Size: Custom | Document Number: ***LA-9631P*** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 58 of 60

VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			EVT TO DVT
1	P.46	Change C726, C727 to 2.2nF	For Sequence
2	P.36	Add R405	For Intel Combo Card
3	P.35	Delete RP19. Add RP26, RP27	Because ME modify MIC location
4	P.14	Add R406, R407, R408, R409	Reserve for improvement factory processes
5	P.42	Add EC_SPI_SO, EC_SPI_SI, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes
6	P.42	Add PCH_PWR_EN to EC Pin.107	Reserve for improvement factory processes
7	P.42	Reserve R410	Reserve Pull-high for GPIO
8	P.5~32	Change footprint of JCPU1, U4, UV1, UV5, UV6, UV7, UV8, UV9, UV10, UV11, UV12	For Lenovo rule
9	P.25	Change RV41 to 240K. Change CV53 to 0.1uF	For VGA sequence
10	P.21	Add Q21, R40, C237, R225, C243	Reserve for power consumption
11	P.34	Add R411, R412, C411, C412	Reserve for EMI
12	P.25	Change CV36, CV37 to 8.2pF	For Crystal fine-tune
13	P.42	Add ADP_65 to EC Pin.21	For adapter protection
14	P.42	Add ADP_90 to EC Pin.68	For adapter protection
15	P.42	Add ADP_135 to EC Pin.85	For adapter protection
16	P.42	Change EC_FAN_PWM from EC Pin.34 to EC Pin.26	For common design
17	P.42	Change NOVO# from EC Pin.26 to EC Pin.34	For common design
18	P.42	Add ADP_ID to EC Pin.66	For adapter
19	P.42	Change PCH_ENBKL from EC Pin.73 to EC Pin.76	For common design
20	P.42	Change IMVP_IMON from EC Pin.76 to EC Pin.73	For common design
21	P.42	Add VGATE to EC Pin.74	Reserve for sequence
22	P.42	Add SYS_PWROK to EC Pin.86	Reserve for sequence
23	P.42	Change EC_TS_ON# from EC Pin.85 to EC Pin.97	For common design
24	P.42	Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123	For common design
25	P.42	Change SUSCLK from EC Pin.123 to EC Pin.122	For common design

Compal Electronics, Inc.

Title: HW-PIR1

Size: Custom | Document Number: LA-9631P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 59 of 60

VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			DVT TO PVT
1	P.40	Delete R416, Add J9	No need Zero ODD Function
2	P.36	Reserve R508	For leakage current issue of Atheros WLAN
3	P.33	Add R509	protect BKOFF# damage
4	P.42	Reserve R416	Reserve +3VLP power rail to EC
5	P.42	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC.
6	P.42	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC	Using power rail which the same with EC.
7	P.14	Change U5 from 4MB to 8MB ROM	Follow common design
8	P.14	Delete R266, R221, U6	It is for 2MB ROM, we don't need it
1	P.41	Reserve resistance to +3VLP and +3VALW.	For Speaker Noise in S5
2	P.42	Reserve resistance in EC for share ROM.	Follow common design
3	P.51	Reserve +V1.05S_VCCP_PWRGOOD of +V.05S_VCCP to connect to SA_PGOOD	For Celeron CPU

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.		
Title: HW-PIR2		
Size: Custom	Document Number: LA-9631P	Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 60 of 60	