Compal Confidential

Guinness-2 M/B Schematics Document

Intel Shark Bay ULT Processor with DDR3L
+AMD SUN XT S3 GPU

REV:1.0_Final

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/20	Deciphered Date	2012/07/01
Title	SHEMATIC. MB AA171		
Size: Custom	Document Number: 4019OJ		Rev: D
Date: Friday, February 28, 2014	Sheet: 1 of 46		

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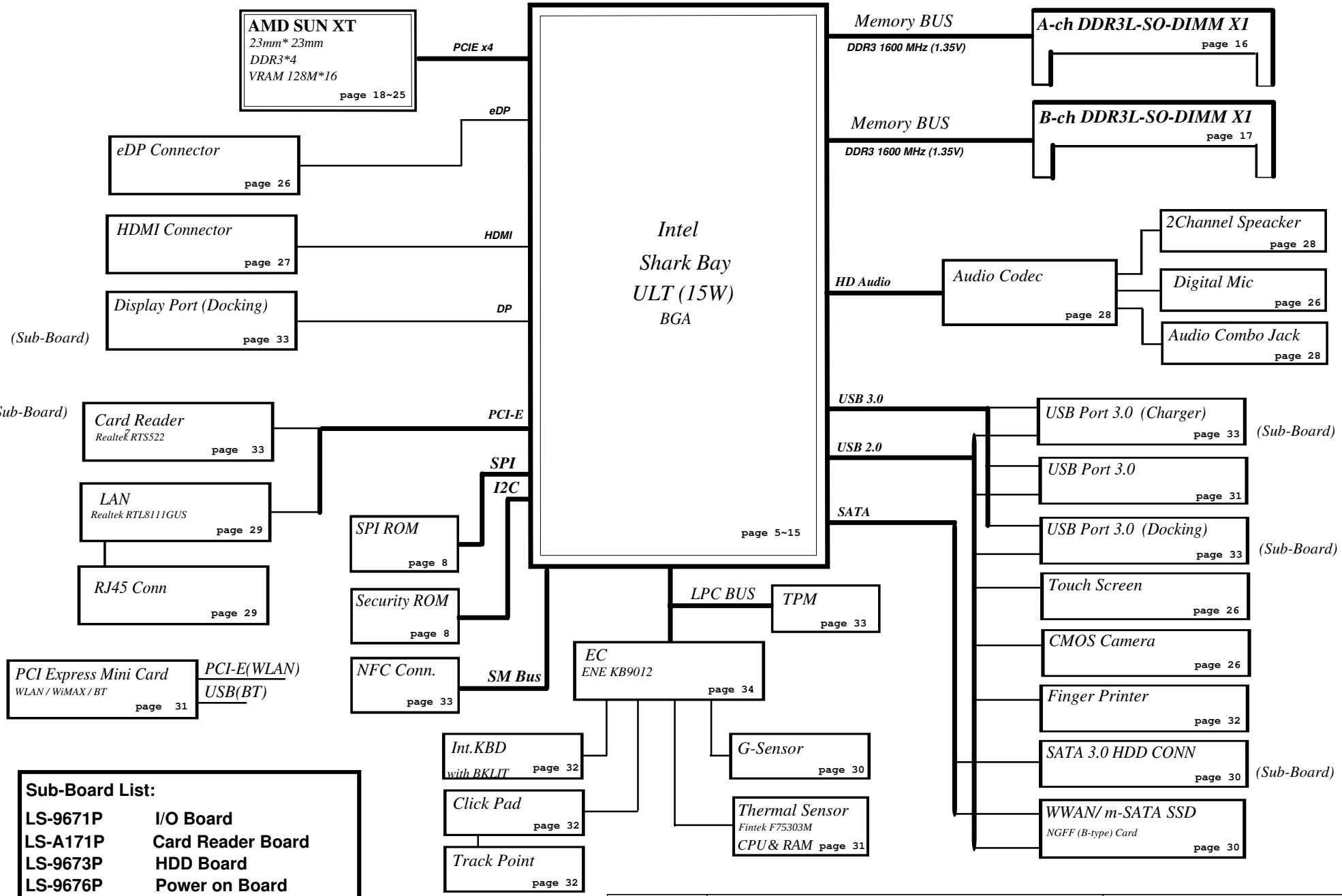

Sub-Board List:

LS-9671P	I/O Board
LS-A171P	Card Reader Board
LS-9673P	HDD Board
LS-9676P	Power on Board
LS-9677P	Hall Sensor Board

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Title: MB Block Diagram

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Voltage Rails

State \ power plane	B+	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.675VS +1.05VS	+3VM +1.05VM (SBA Only)
S0	O	O	O	O	O M3 Supported
S3	O	O	O	X	O M3 Supported
S5 S4/AC	O	O	X	X	O M3 Supported
S5 S4/ Battery only	X	X	X	X	
S5 S4/AC & Battery don't exist	X	X	X	X	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

USB 2.0 Port Table

	USB 2.0 Port	3 External USB Port
	0	USB 3.0 Port (I/O Board)
	1	USB 3.0 Port (MB)
	2	USB 3.0 Port (Docking)
	3	Mini Card (WLAN/BT)
	4	Touch Screen
	5	Camera
	6	FPR
	7	WWAN

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H
Charger	0001 011X b	12H

EC SM Bus2 address

Device	Address	HEX
Thermal Fintek F75303M	1001 101X b	9AH
Thermal ON-semi ADM1032	0100 110X b	4CH
Sinaptics Inter Touch Click Pad	0010 110X b	2CH

PCH SM Bus address

Device	Address	HEX
DDR DIMM1	1001 000X b	A0H
DDR DIMM2	1001 000X b	A4H
Securyti ROM	1010 100X b	A8H

BOM Structure Table

BTO Item	BOM Structure	
Connector	ME@	
Unpop	@	
AMD GPU	DIS@	
Intel UMA	UMA@	
MARS GPU	MARS@	
TPM	TPM@	
SIM	SIM@	
SBA	SBA@	Either SBA@ or NOSBA@
Non-SBA	NOSBA@	
LAN Switching mode	SWR@	Either SWR@ or LDO@
LAN LDO mode	LDO@	
VRAM Option	X76@	
Samsung VRAM Micron VRAM	X76S@ X76M@	Either X76S@ or X76M@
AOAC Mount	AOAC@	
EMI un-Mount EMI Mount	@EMI@ EMI@	

USB 3.0 Port Table

Port	
1	USB 3.0 Port (I/O Board)
2	USB 3.0 Port (MB)
3	USB 3.0 Port (Docking)
4	

SATA Port Table

Port	
3	
2	
1	NGFF SSD
0	HDD

PCIE Port Table

Port	Lane	
1		
2		LAN
3		WLAN
4		Cardreader
5	0	GPU
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

CPU

U1 — Haswell ULT 2+2 0.8GHz
CPU1@
SA000067010

U1 — Haswell ULT 2+2 1.2GHz
CPU2@
SA00006G100

U1 — Haswell ULT 2+3 0.2GHz
CPU3@
SA000067H20

U1 — Haswell ULT 1.5GHz
CPU4@
SA00006SJ20

U1 — Haswell ULT 1.4GHz
CPU5@
SA00006ST30

U1 — Haswell ULT 1.6GHz
CPU6@
SA00006SM40

U1 — Haswell ULT 1.7GHz
CPU7@
SA00006SX40

U1 — Haswell ULT 1.8GHz
CPU8@
SA00006SL50

U1 — Haswell ULT 1.3GHz
CPU9@
SA00006NM30

U1 — Haswell ULT 1.7GHz C0
CPU10@
SA00006SS20

U1 — Haswell ULT 1.7GHz C0
CPU11@
SA00006SX50

U1 — Haswell ULT 1.6GHz C0
CPU12@
SA00006SM70

U1 — Haswell ULT 1.7GHz C0
CPU13@
SA00006SL60

U1 — Haswell ULT 1.7GHz C0
CPU14@
SA00006SL60

U1 — Haswell ULT 1.7GHz C0
CPU15@
SA00006SS60

PCB

ZZZ — LA-A171P
DA PCB
DAZ0YW00100

VRAM

ZZZ2 — MICRON_512MB
X76M@
X7646039L01

ZZZ1 — Samsung_512MB
X76S@
X7646039L02

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Title: **Notes List**

Size: Custom | Document Number: **4019OJ** | Rev: D

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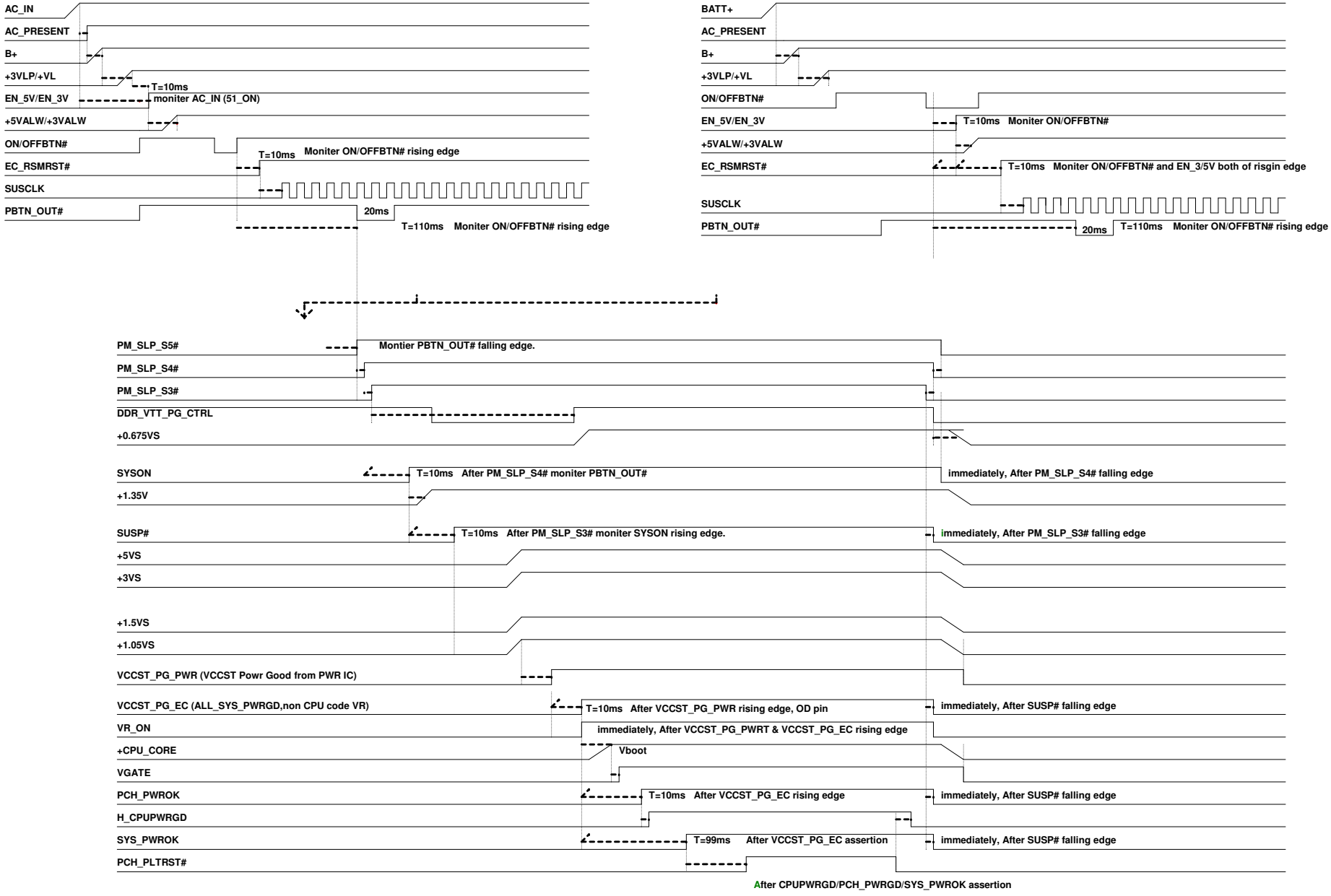
[AC Mode]



[DC Mode]

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Title	Power Sequence		
Size	Document Number	4019OJ	Rev D
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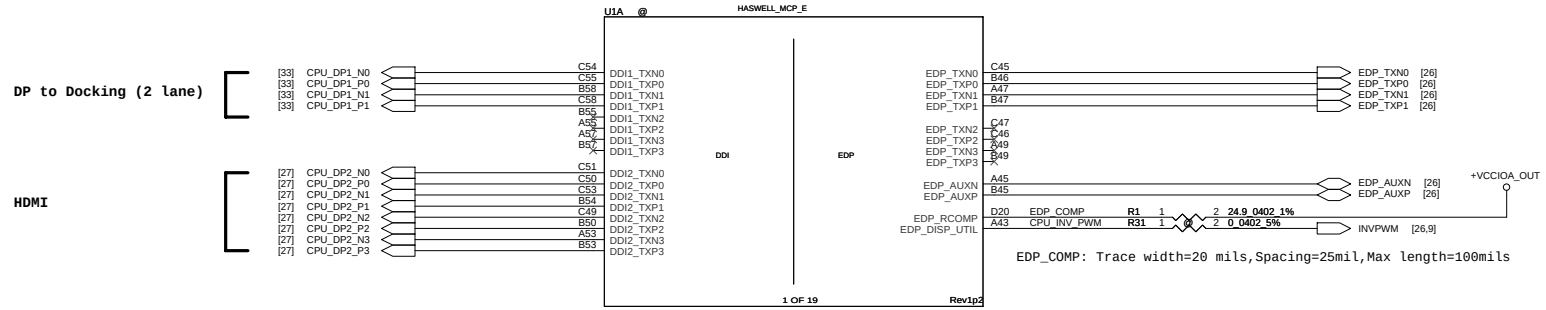
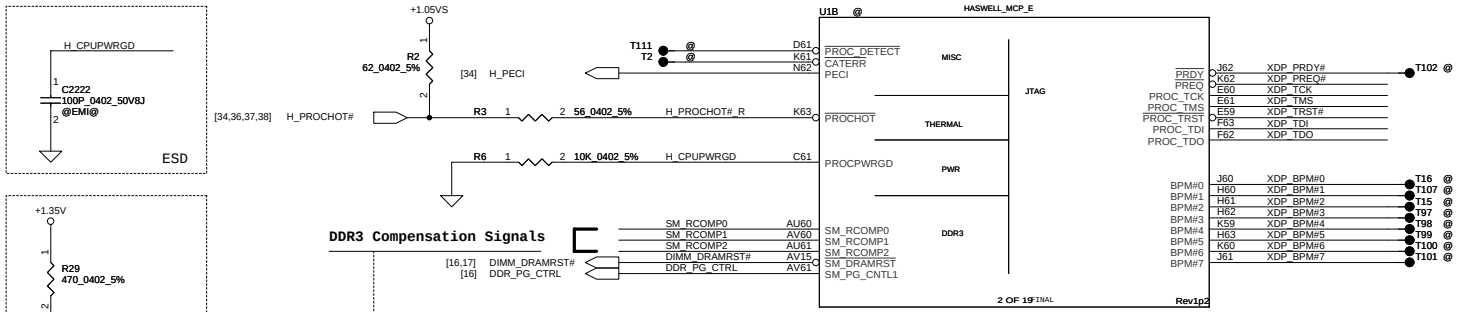
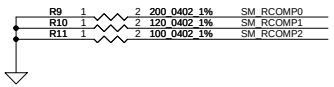
DDI/ MSIC/ XDP



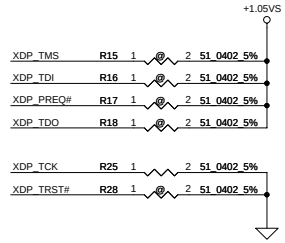


DDR3 Compensation Signals

DDR3 Compensation Signals:
20 mils to comp signals
25 mils to non-comp signals
500 mil for Max trace length



PU/PD for JTAG signals



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Compal Electronics, Inc.			
Title	HSW MCP(1/11) DDI,MSIC,XDP		
Size: Custom	Document Number: 4019QJ		Rev: D
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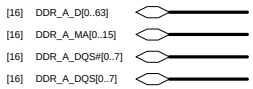
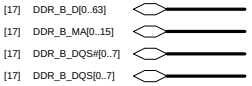
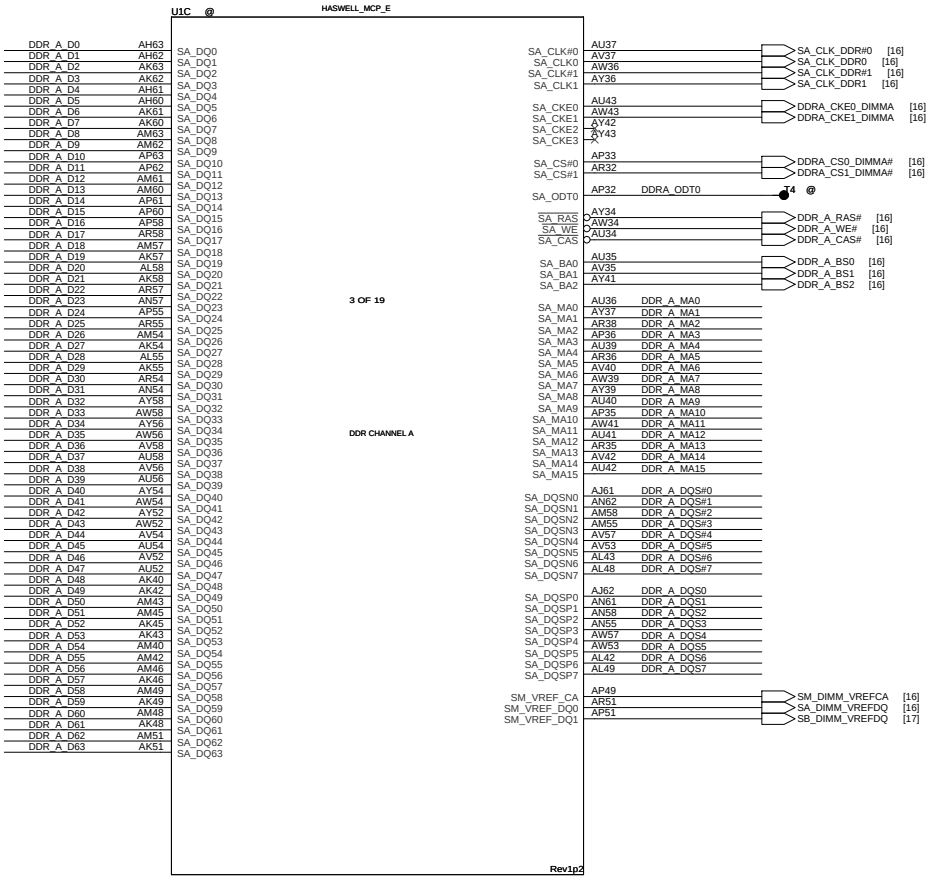
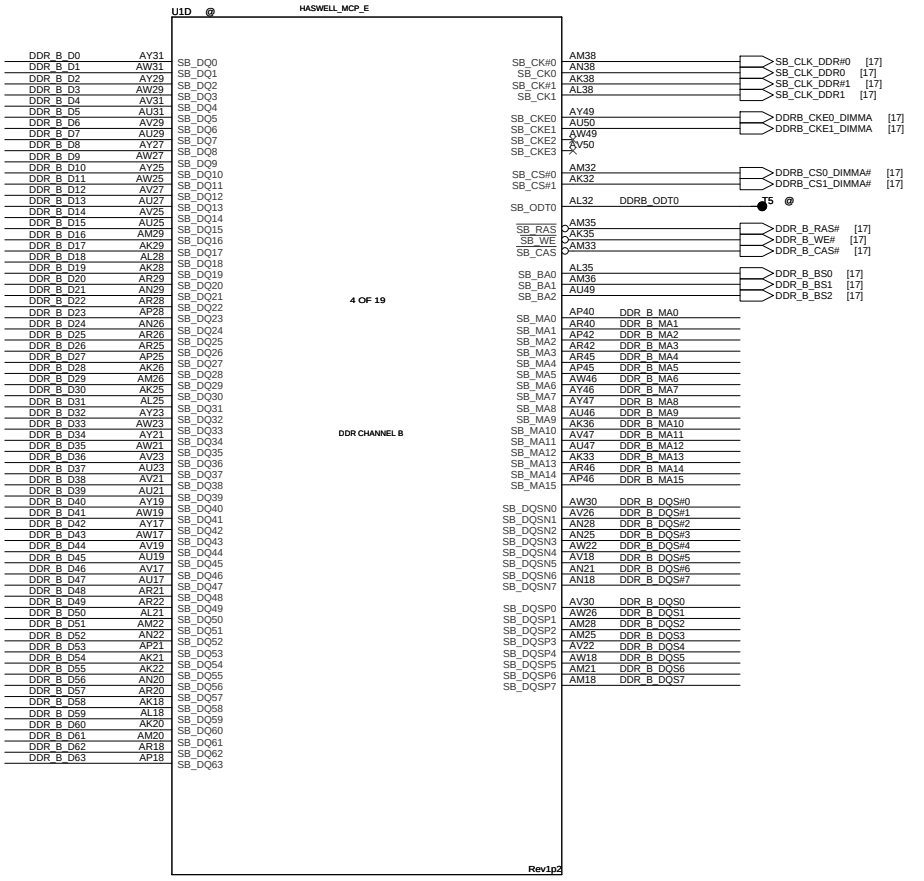
Memory I/F









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Title: HSW MCP(2/11) DDRIII			
Size: Custom	Document Number: 4019QJ		Rev: D
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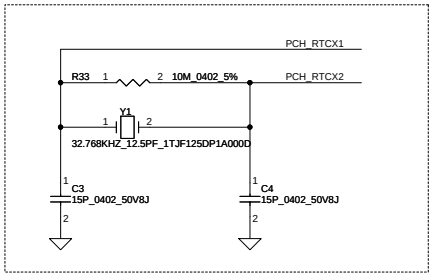
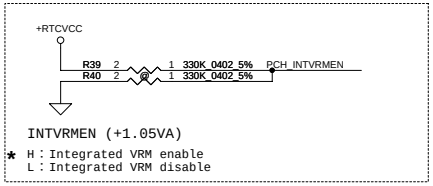
RTC/ SATA/ XDP

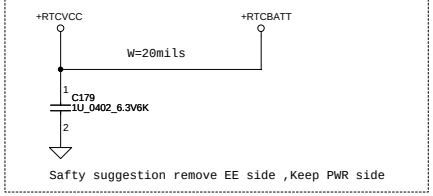




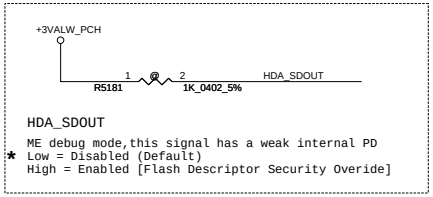
INTVRMEN (+1.05VA)

* H : Integrated VRM enable
L : Integrated VRM disable

RTC Battery



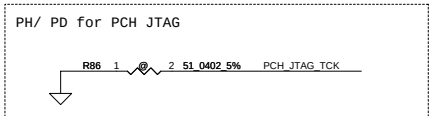
Safty suggestion remove EE side ,Keep PWR side

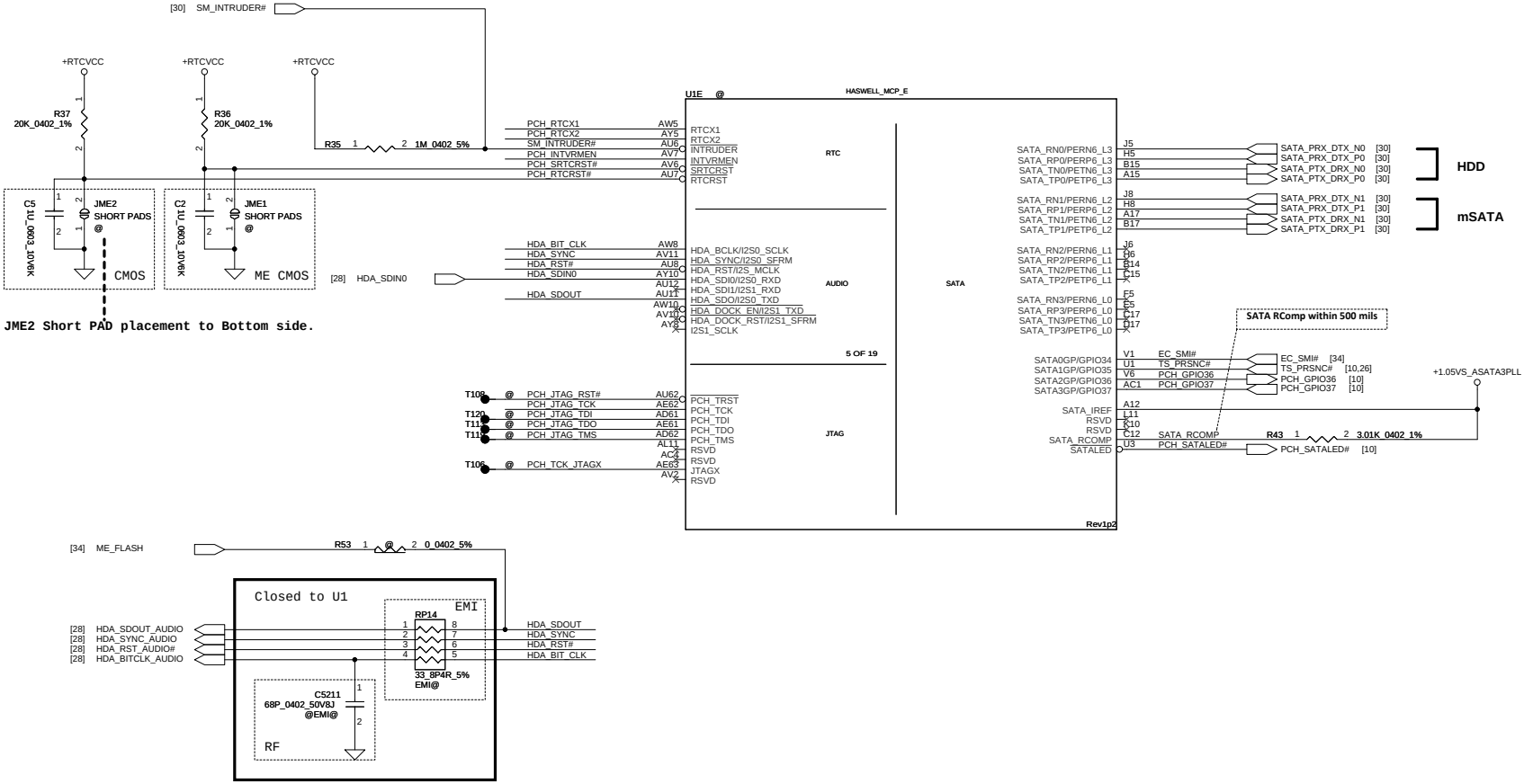


HDA_SDOUT

ME debug mode,this signal has a weak internal PD
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

PH/ PD for PCH JTAG





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Title	HSW MCP(3/11) RTC,SATA,XDP		
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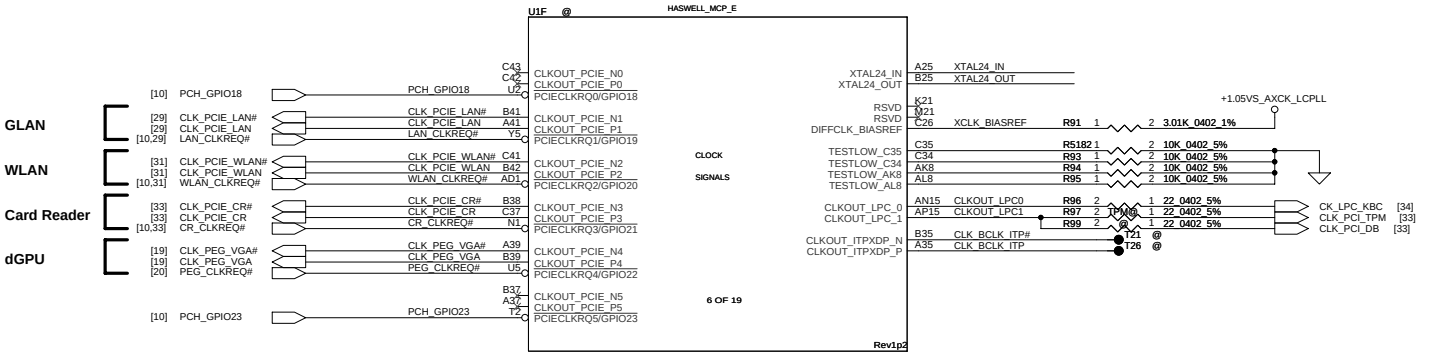
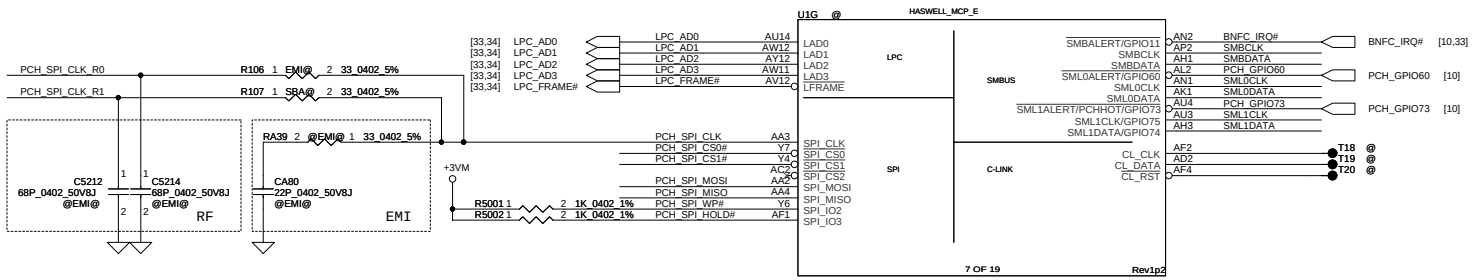
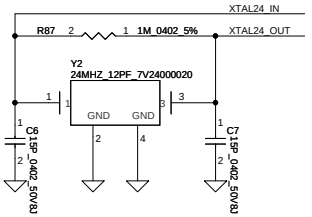
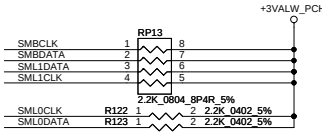
CLK/ SPI/ SMBUS

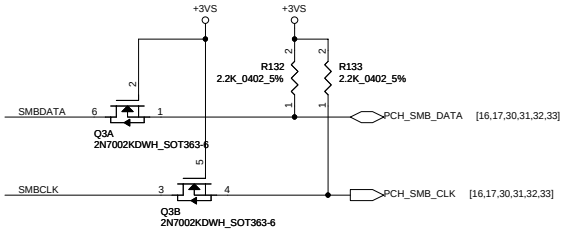




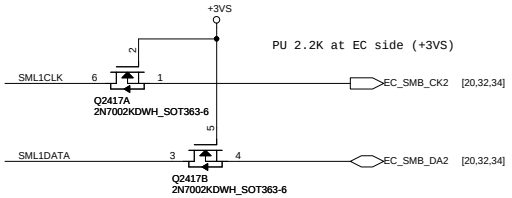




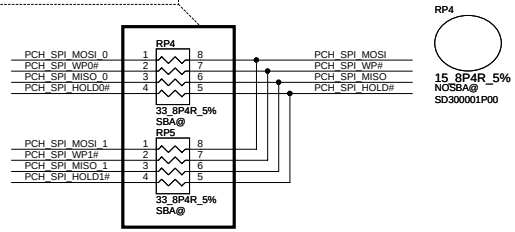
SMBus :SPD/PCIe/Security/TP/NFC



SML1 Bus :EC/Sensors

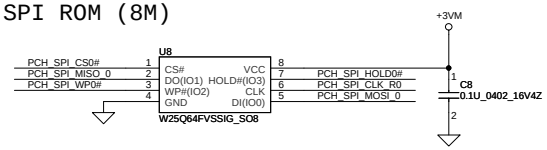


SBA - 2 SPI Device = 33 ohm - P/N: SD309330A80
Non-SBA - 1 SPI Device = 15 ohm - P/N: SD300001P00

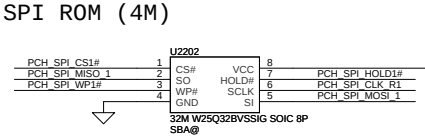


SPI ROM (8M)

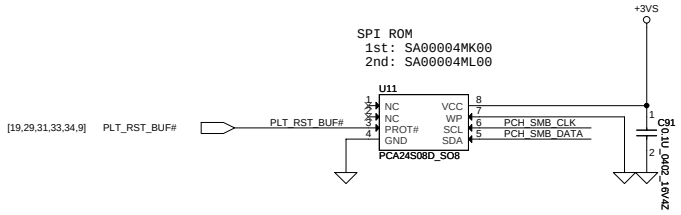
SPI ROM 8MB
1st: SA000039A20 - Winbond
2nd: SA000046400 - E-ON
SPI ROM 4MB
1st: SA00003K800 - Winbond
2nd: SA00004LI00 - E-ON



SPI ROM (4M)



Security ROM



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Compal Electronics, Inc.	
Title	HSW MCP(4/11) CLK,SPI,SMBUS
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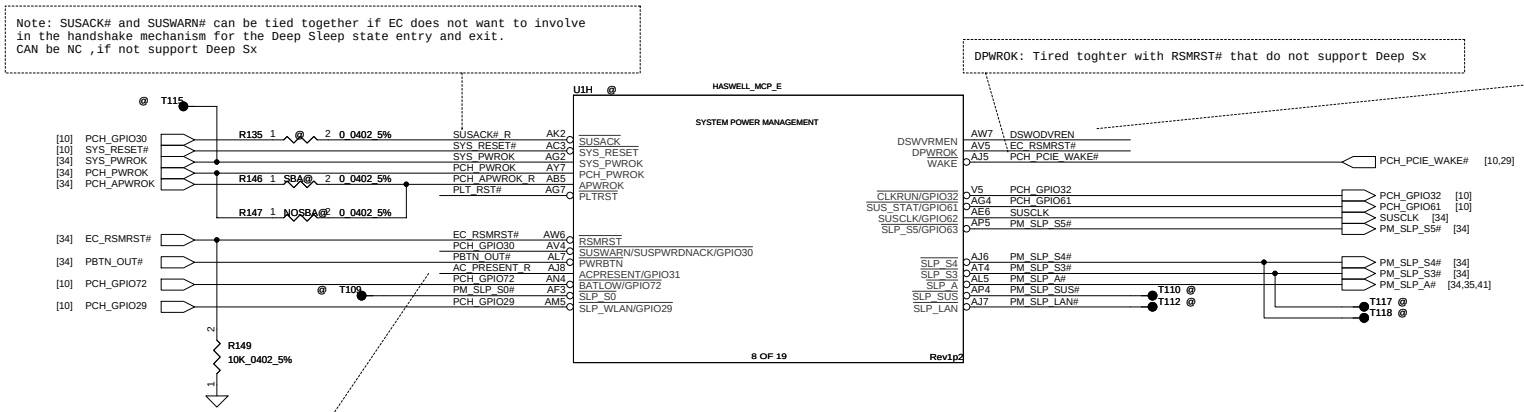
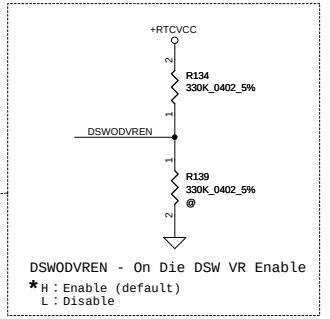
PM/ GPIO/ DDI

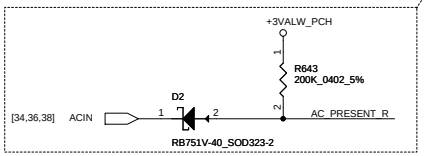
Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.
CAN be NC ,if not support Deep Sx

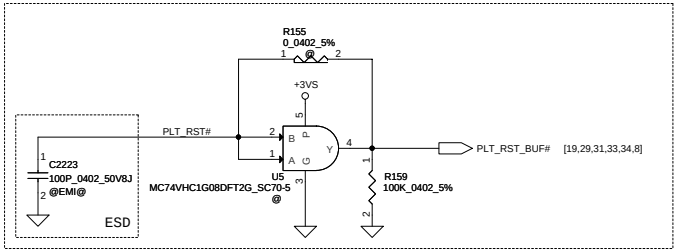
DPWROK: Tired toghter with RSMRST# that do not support Deep Sx

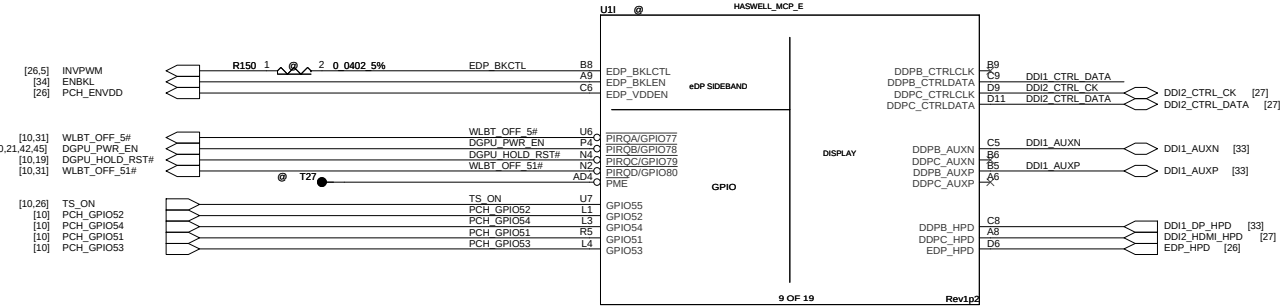


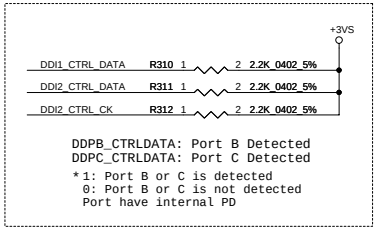


PCH_BATLOW# Need pull high to VCCDSW3_3
(If no deep Sx , connect to VCCSUS3_3)









Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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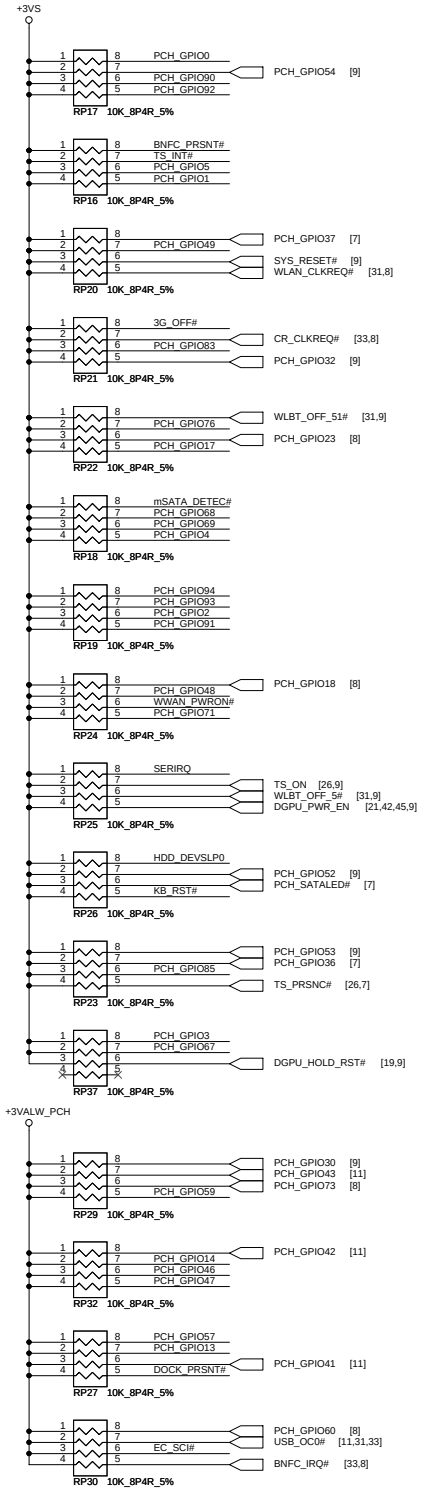
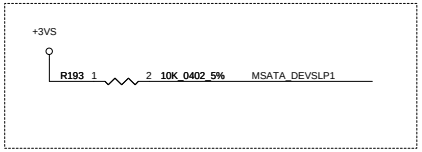
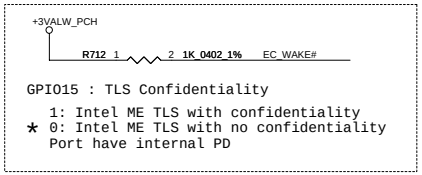
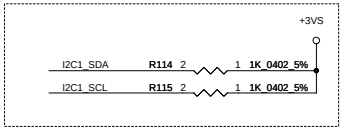
Compal Electronics, Inc.			
Title	HSW MCP(5/11) PM,GPIO,DDI		
Size: Custom	Document Number: 4019QJ		Rev: D
Date: Friday, February 28, 2014	Sheet 9 of 46		

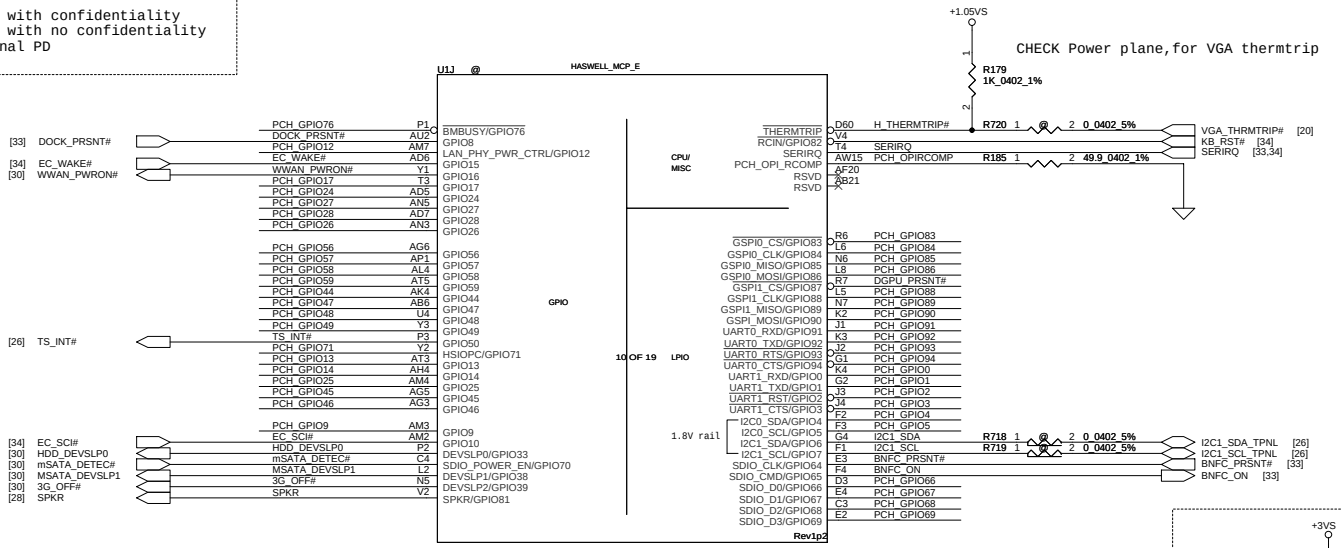
GPIO/ LPIO

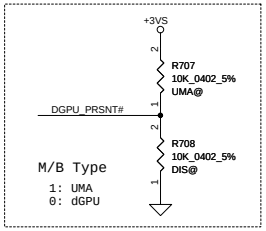


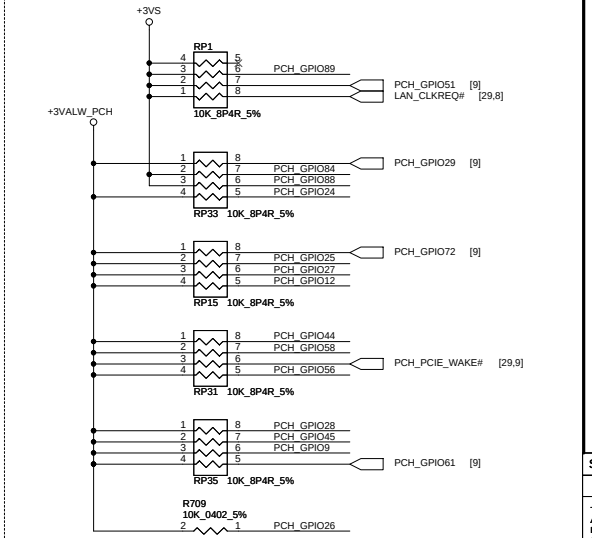


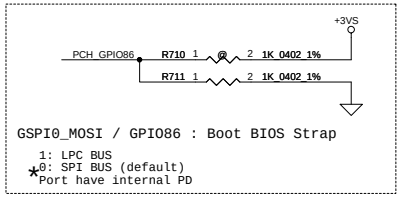


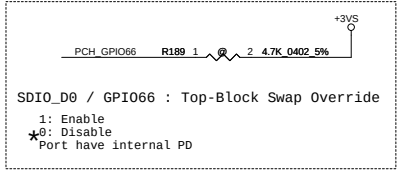












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Issued Date	2013/02/20	Deciphered Date	2012/07/01

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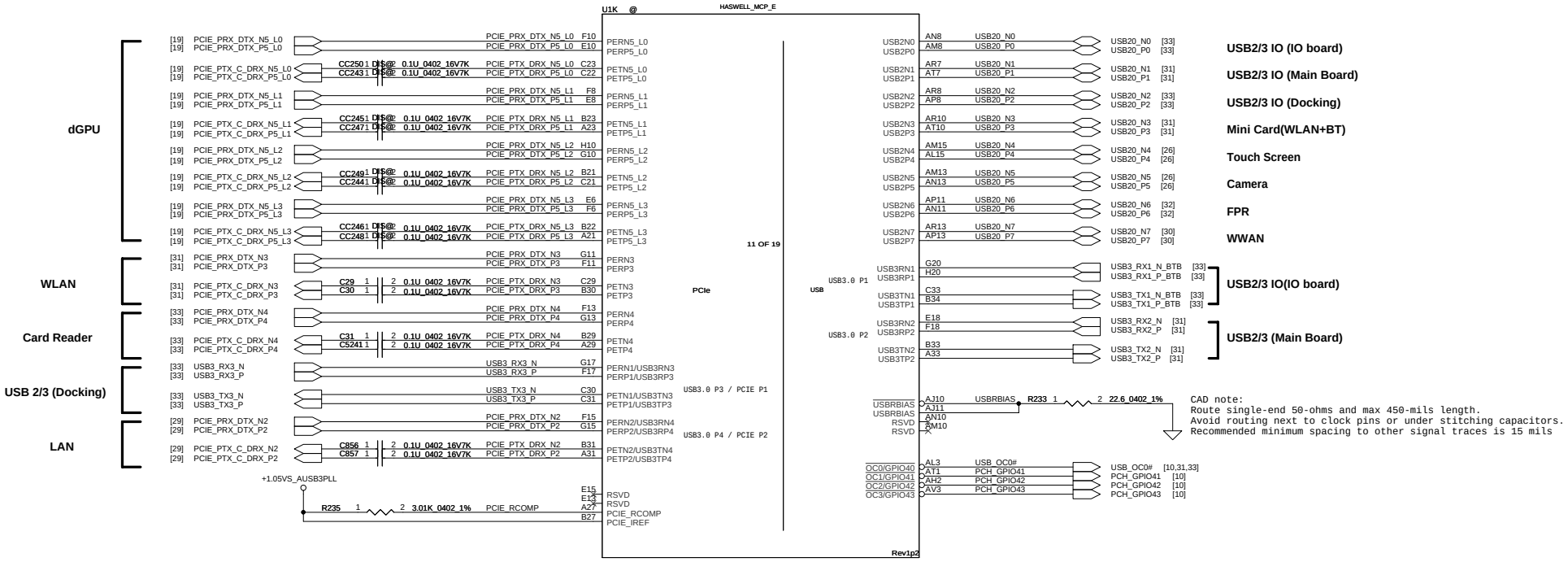
Compal Electronics, Inc.			
Title	HSW MCP(6/11) GPIO,LPIO		
Size: Custom	Document Number: 4019QJ		Rev: D
Date: Friday, February 28, 2014	Sheet 10 of 46		

PCIE/ USB



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Issued Date	2013/02/20	Deciphered Date	2012/07/01

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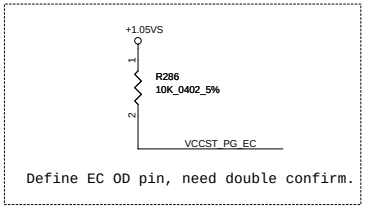
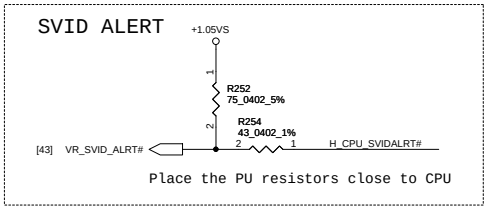
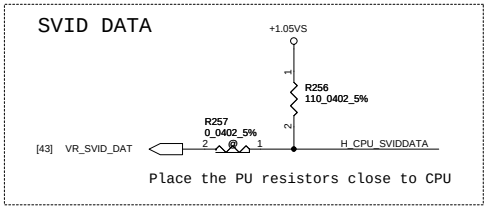
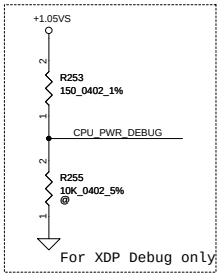
Compal Electronics, Inc.			
Title: HSW MCP(7/11) PCIE,USB			
Size: Custom	Document Number: 4019QJ		Rev: D
Date: Friday, February 28, 2014	Sheet 11 of 46		

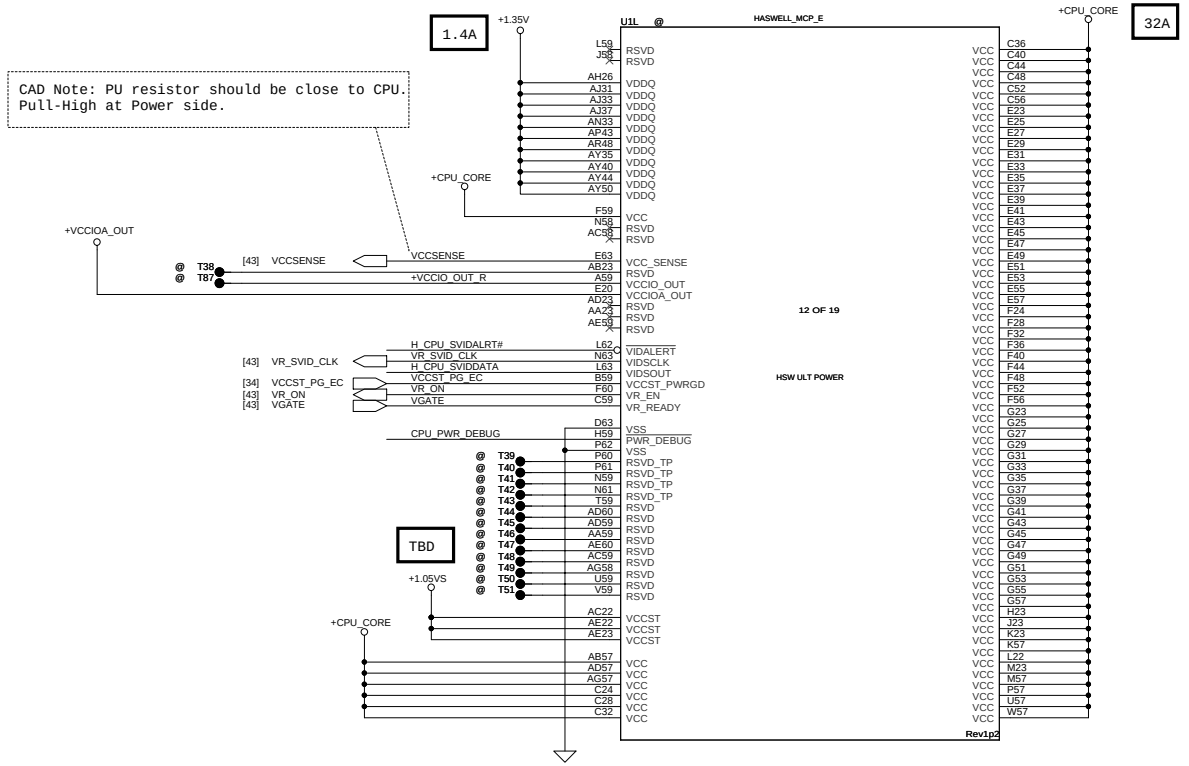
Power

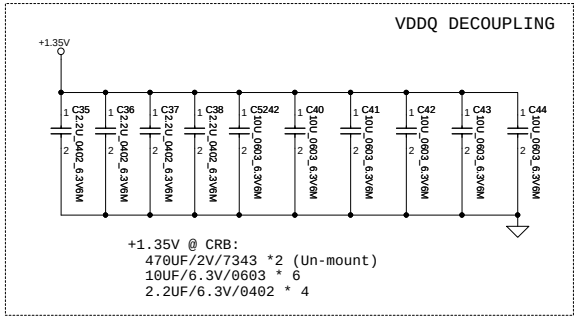












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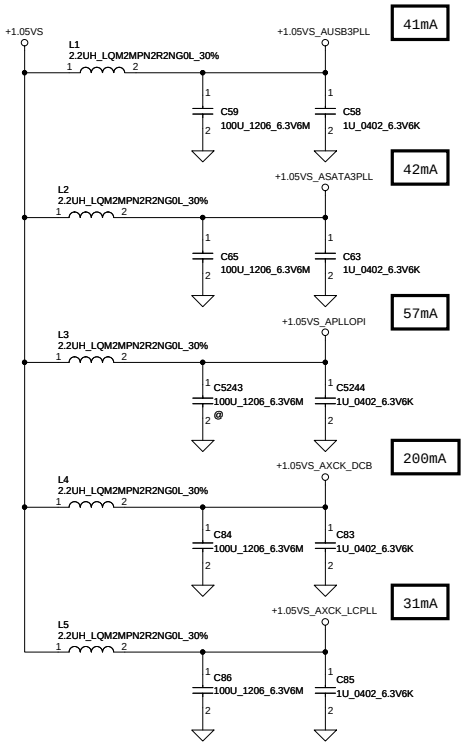
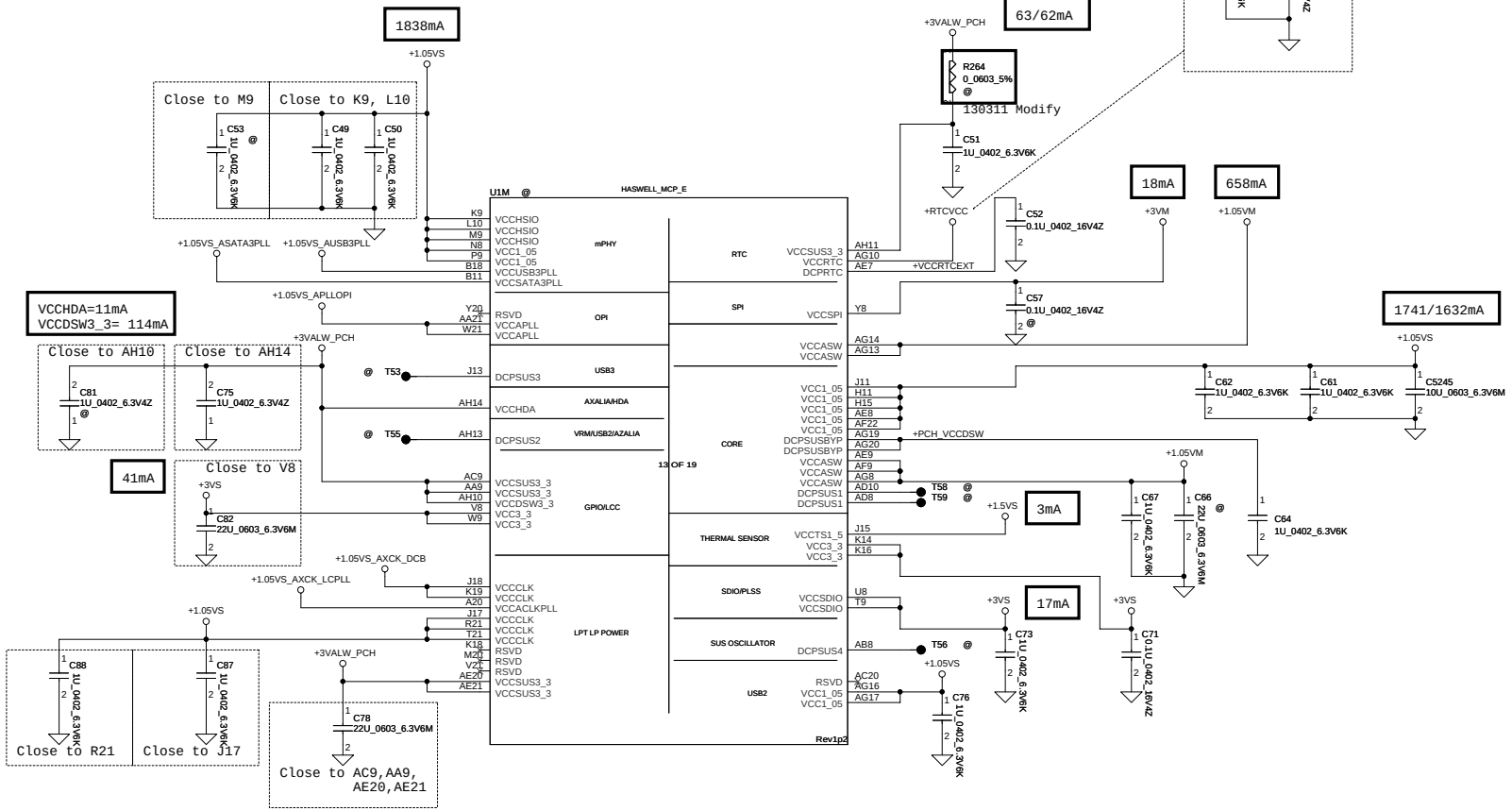
Compal Electronics, Inc.			
Title: HSW MCP(8/11) Power			
Size: Custom	Document Number: 4019QJ		Rev: D
Date: Friday, February 28, 2014	Sheet 12 of 46		

Power





Only availible on External Suspend VR powered.
DcpSus1= 109mA
DcpSus2= 25mA
DcpSus3= 10mA
DcpSus4= 1mA

Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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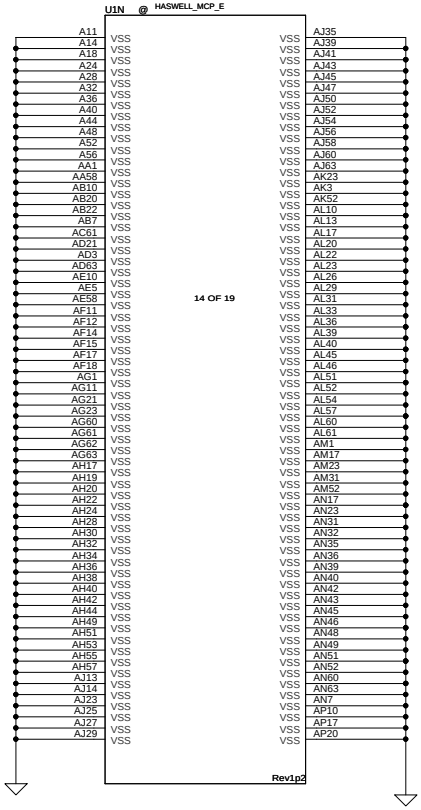
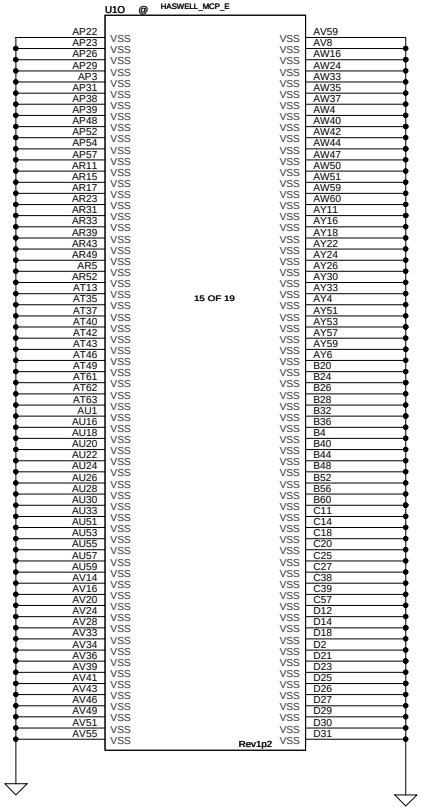
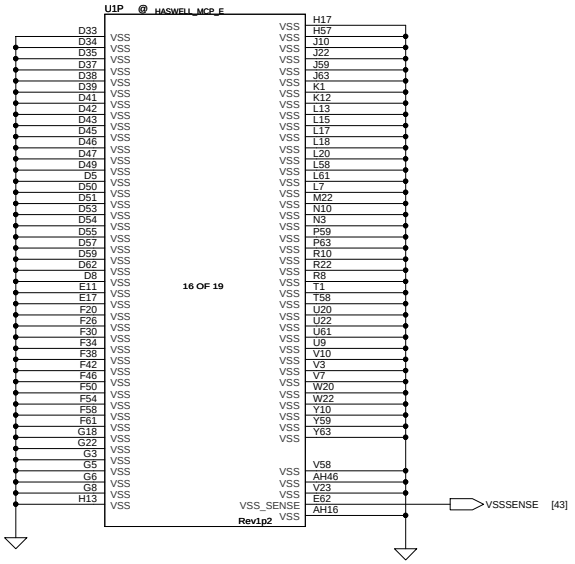
Compal Electronics, Inc.			
Title: HSW MCP(9/11) Power			
Size: Custom	Document Number: 4019QJ		Rev: D
Date: Friday, February 28, 2014	Sheet 13 of 46		

GND







Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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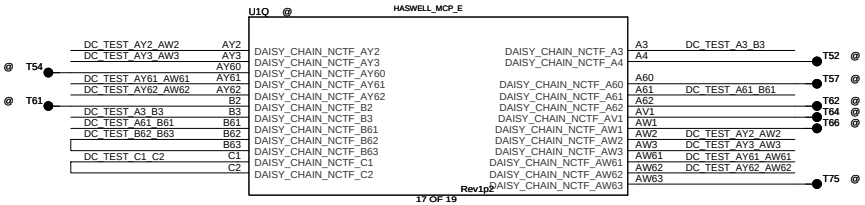
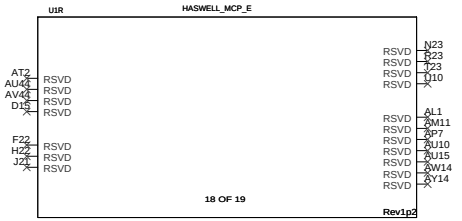
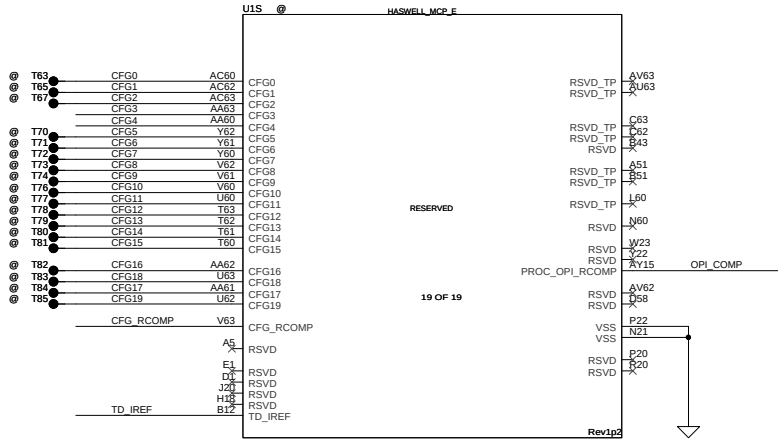
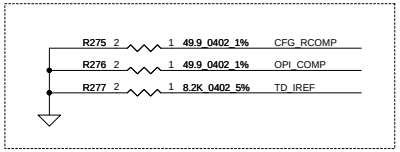
Compal Electronics, Inc.		
Title: HSW MCP(10/11) GND		
Size: Custom	Document Number: 4019QJ	Rev: D
Date: Friday, February 28, 2014	Sheet 14 of 46	

RSVD

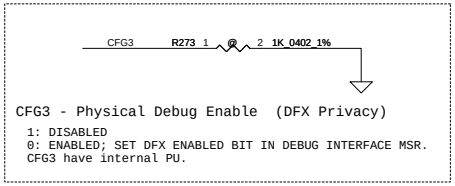


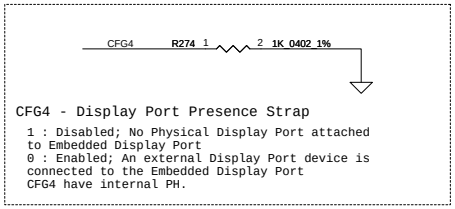






CFG Straps for Processor





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Issued Date	2013/02/20	Deciphered Date	2012/07/01

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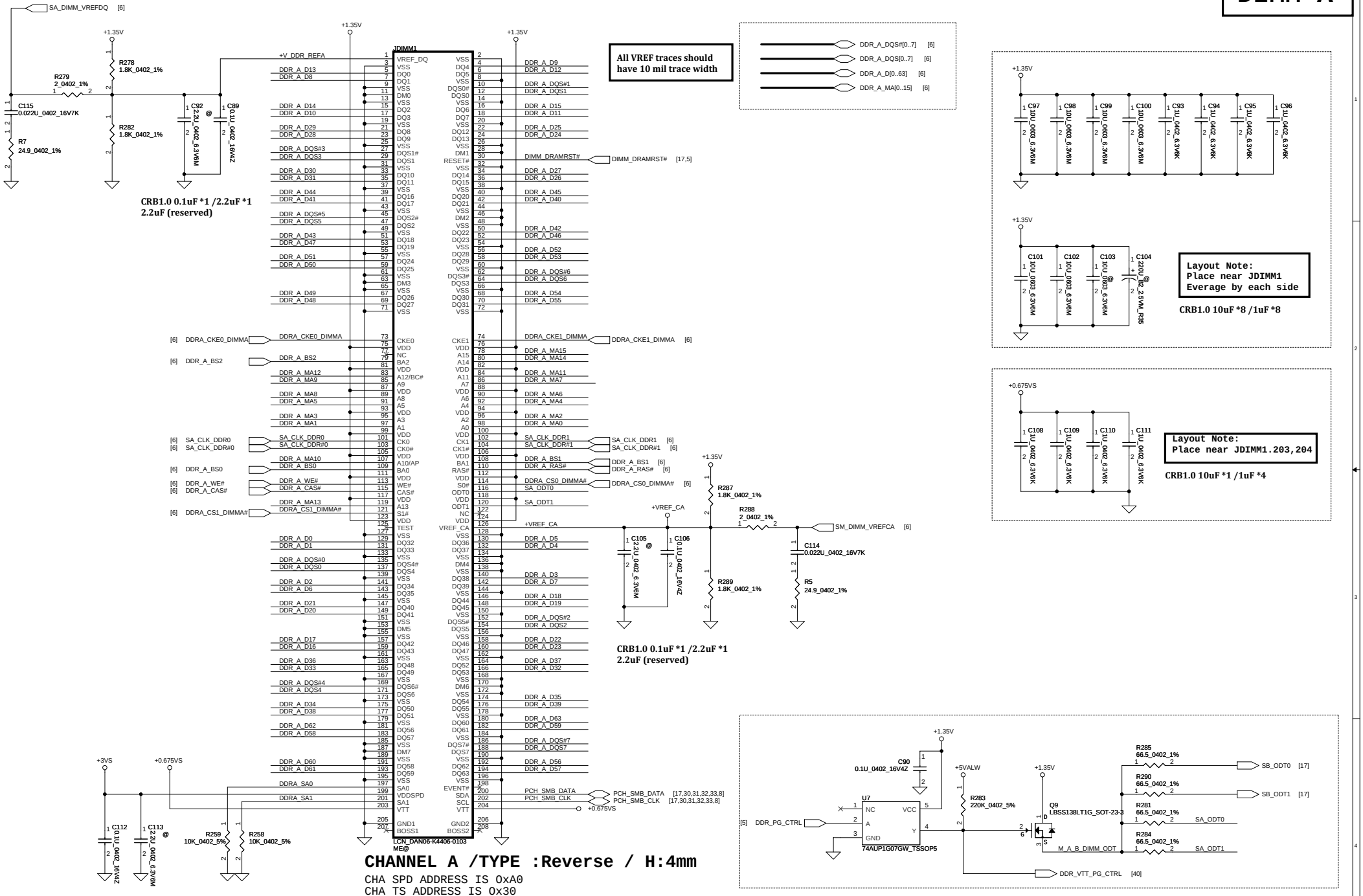
Compal Electronics, Inc.	
Title	HSW MCP(11/11) RSVD
Size: Custom	Document Number: 4019OJ
Rev: D	
Date: Friday, February 28, 2014	Sheet 15 of 46

DIMM A



CHANNEL A /TYPE :Reverse / H:4mm

CHA SPD ADDRESS IS 0xA0
CHA TS ADDRESS IS 0x30

P/N:SP07000LT00

Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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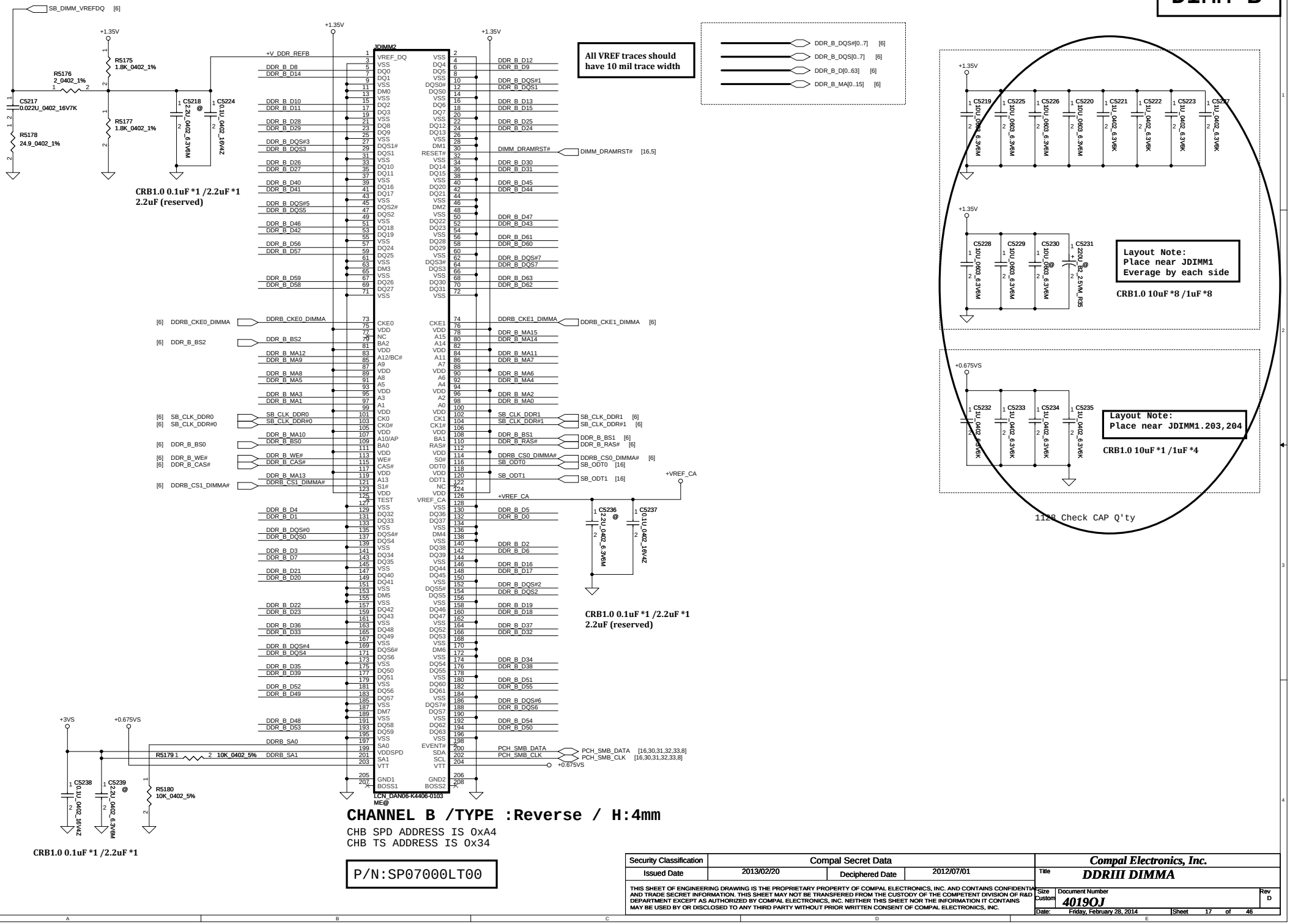
Compal Electronics, Inc.			
Title: DDRIII DIMMA			
Size: Custom	Document Number: 4019QJ		Rev: D
Date: Friday, February 28, 2014	Sheet 16 of 46		

DIMM B



CHANNEL B /TYPE :Reverse / H:4mm

CHB SPD ADDRESS IS 0xA4
CHB TS ADDRESS IS 0x34

P/N:SP07000LT00

Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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Compal Electronics, Inc.			
Title: DDRIII DIMMA			
Size: Custom	Document Number: 4019QJ		Rev: D
Date: Friday, February 28, 2014	Sheet 17 of 46		

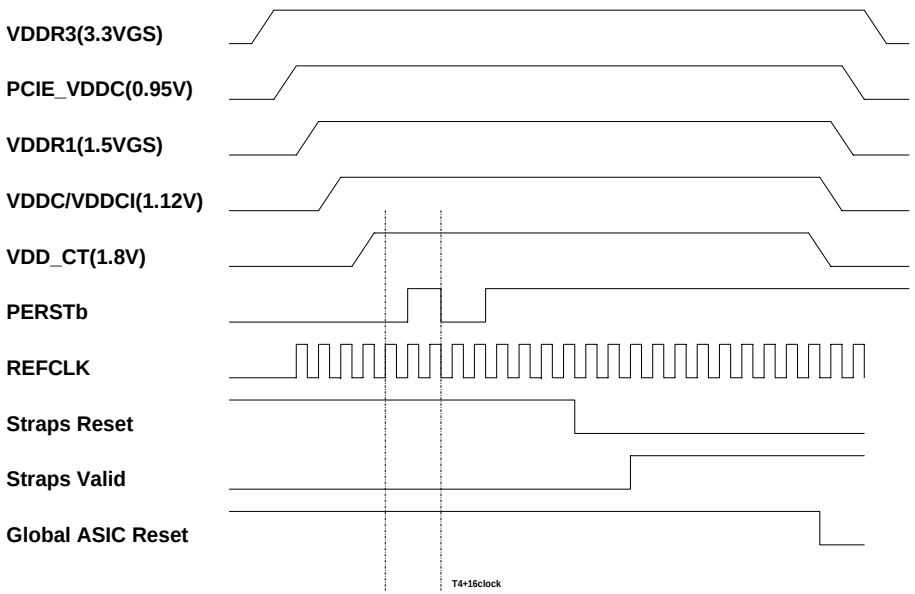
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

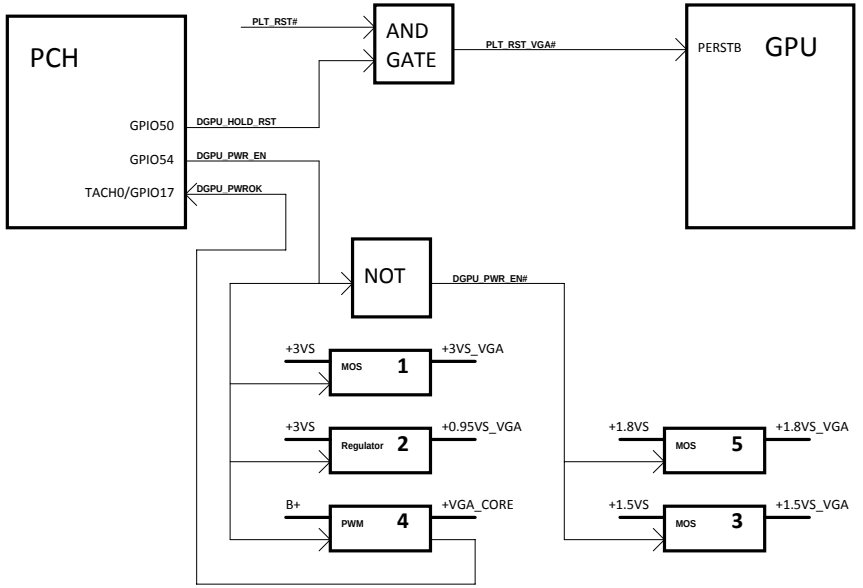
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.

3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

4. For power down, reversing the ramp-up sequence is recommended.



CPU part



Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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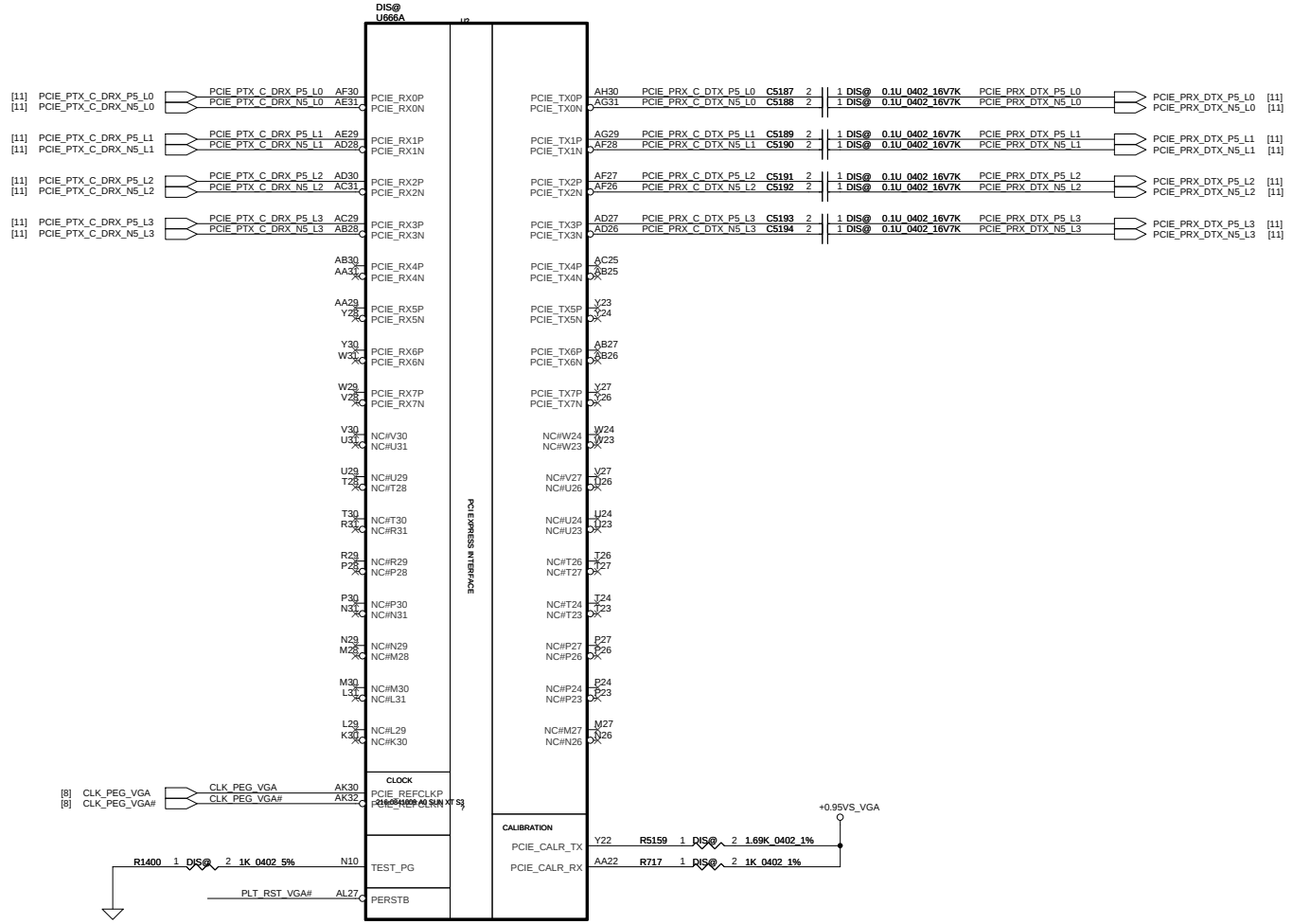
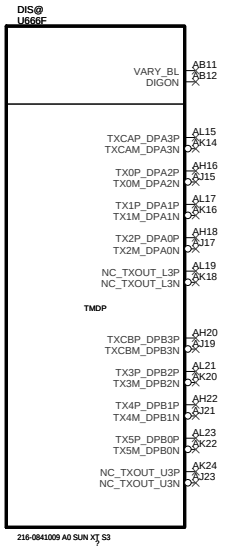
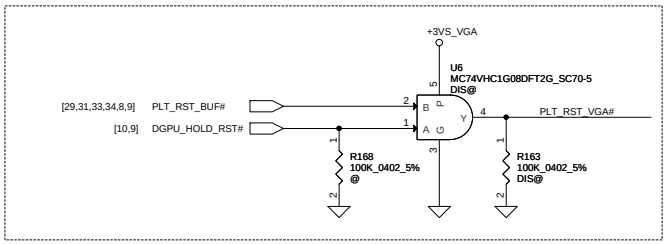
Compal Electronics, Inc.			
Title: SUN_Note			
Size: Custom	Document Number: 4019OJ		Rev: D
Date: Friday, February 28, 2014	Sheet 18 of 46		

PCIE/ DP



No Use GPU Display Port outpud





Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title: SUN_PCIE/DP

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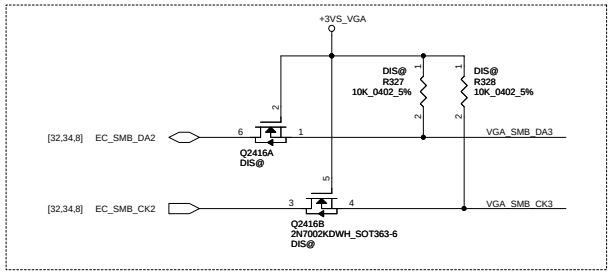
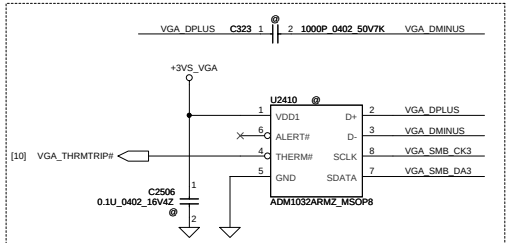
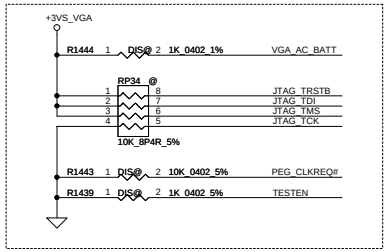
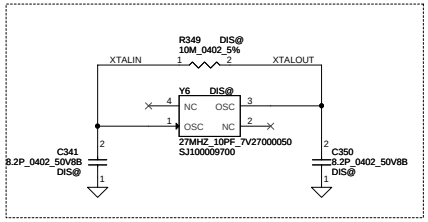
Date: Friday, February 28, 2014 | Sheet 19 of 46

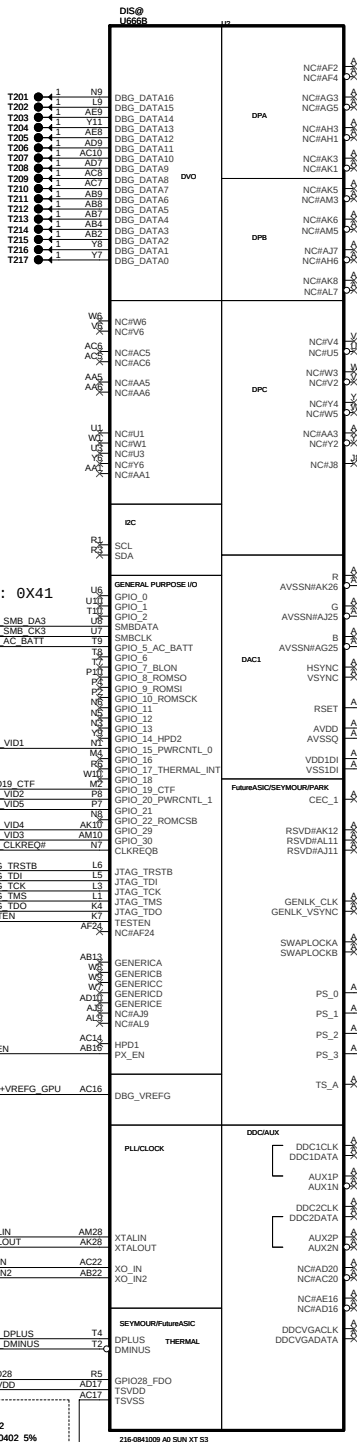
MSIC











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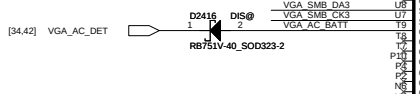

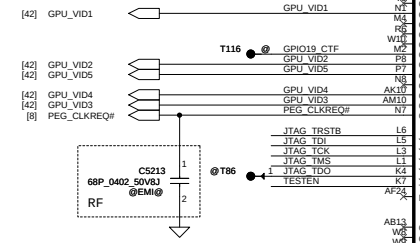

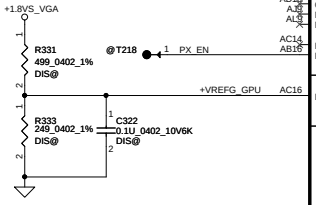

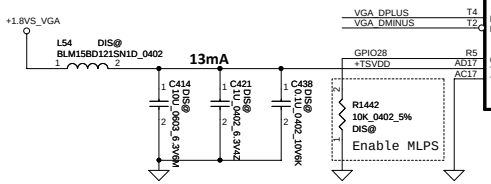

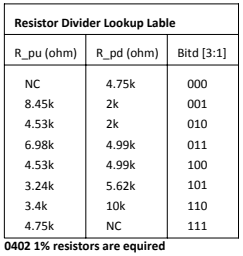

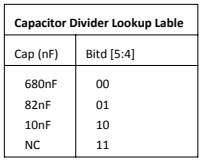

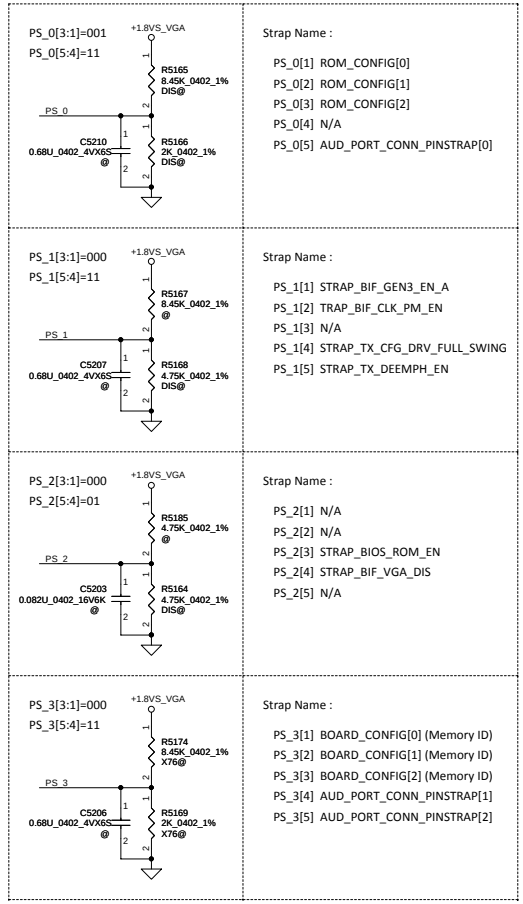

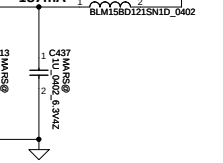

Memory ID PS_3[3..1]	R_pu (ohm) R5174	R_pd (ohm) R5169	Memory Type	Configuration	Size
0 0 1	8.45k SD000000680	2k SD034200180	gDDR3-2133	Samsung K4W2G1646E-BC1A P/N: SA000068U00	1GB
0 1 0	4.53k SD034453180	2k SD034200180	gDDR3-2000	Micron MT41J128M16JT-093G P/N: SA000067500	1GB
0 1 1	6.98k SD000002680	4.99k SD034499180	gDDR3-1866	Samsung K4W4G1646B-HC11 P/N: SA000068R00	2GB
1 0 0	4.53k SD034453180	4.99k SD034499180	gDDR3-1866	Micron MT41K256M16HA-107G: E P/N: SA000065D00	2GB

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Title: SUN_MSIC			
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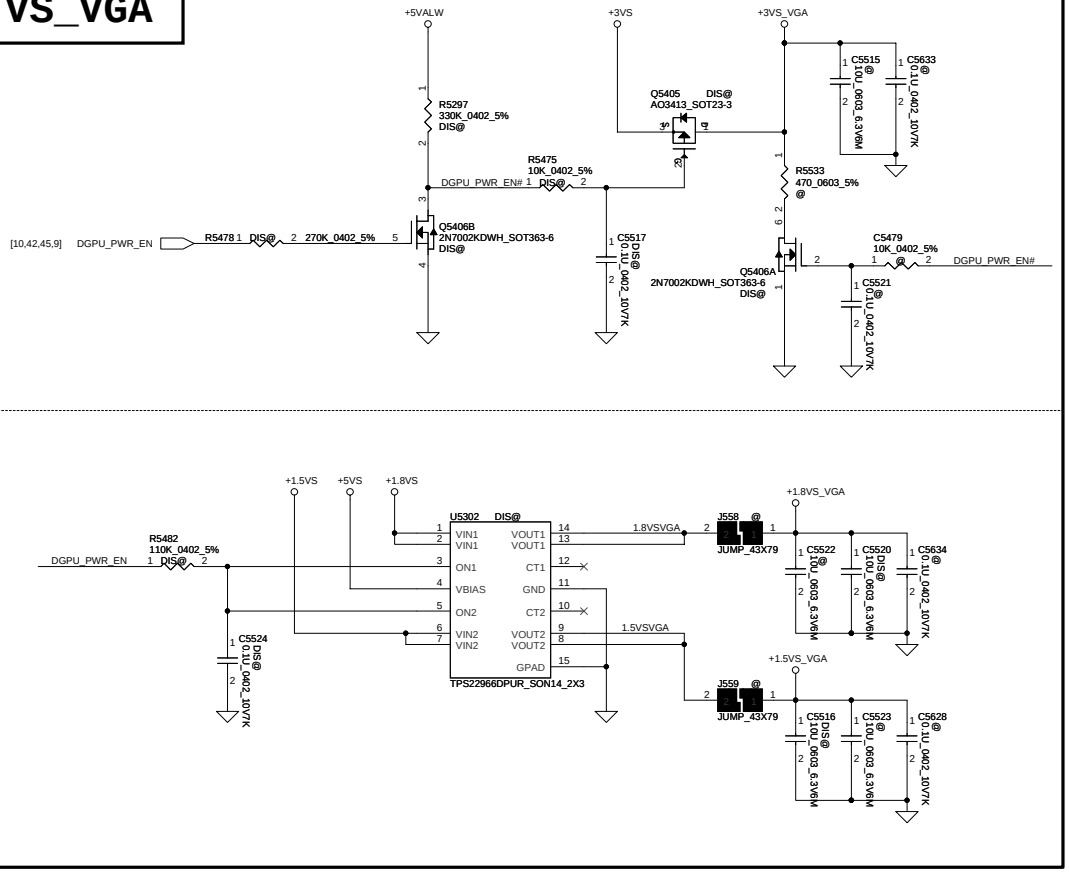
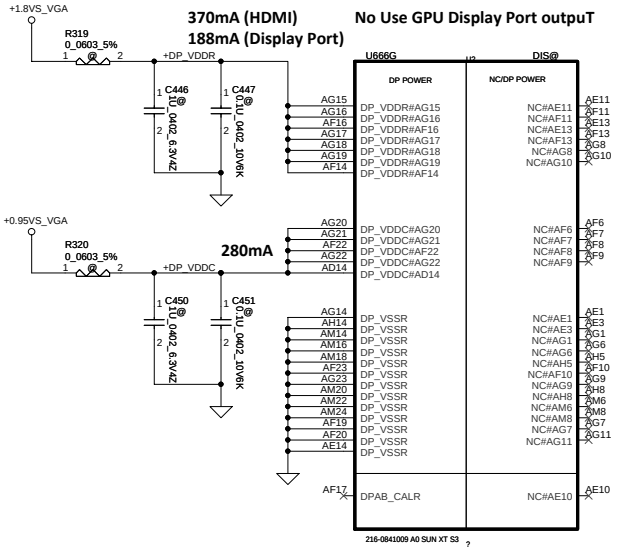
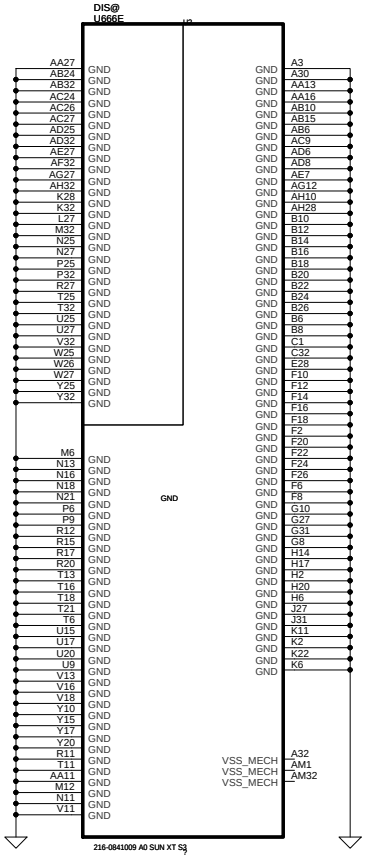
VS_VGA



PWR/GND





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Title: SUN_Power/GND

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POWER

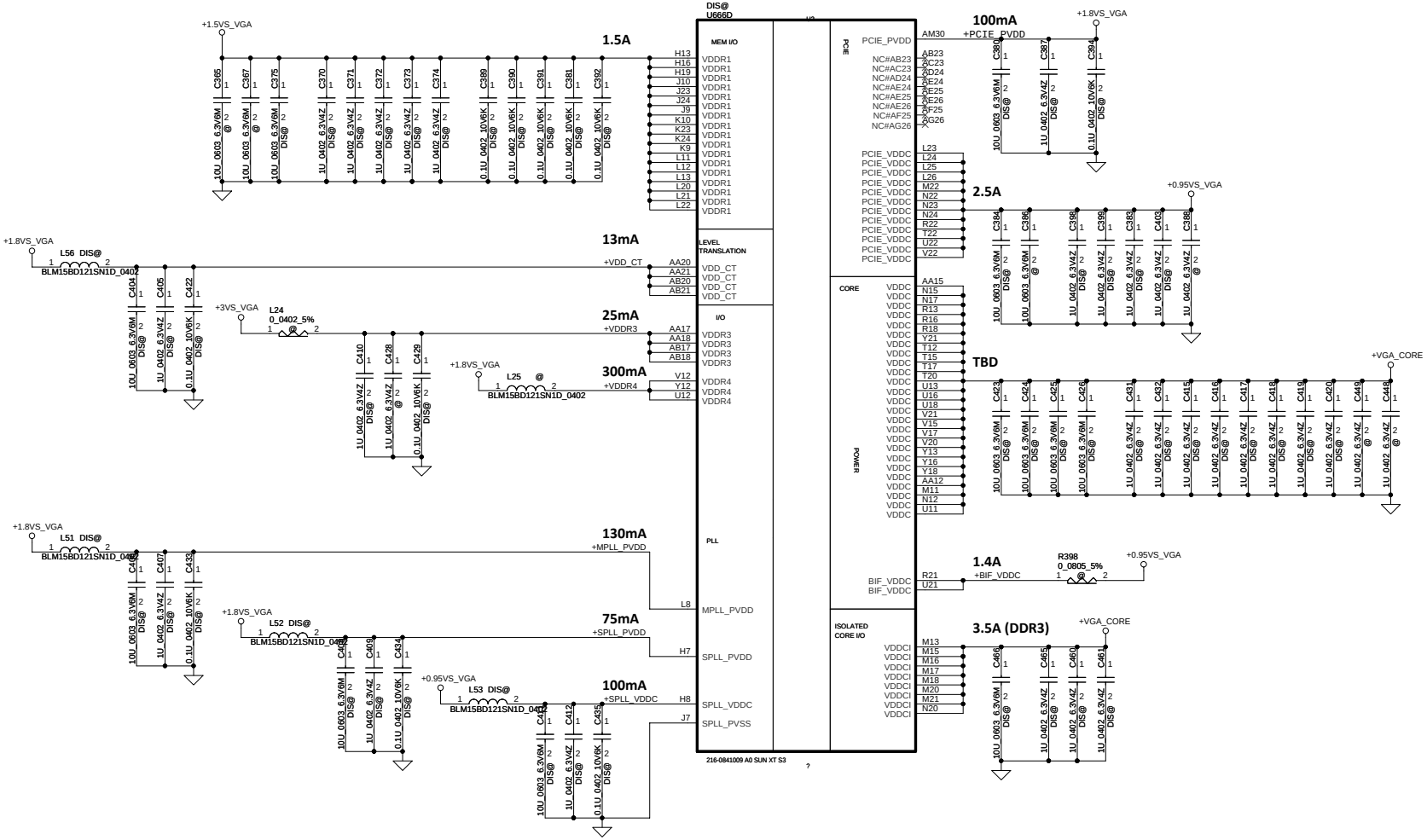
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



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Title: SUN_Power

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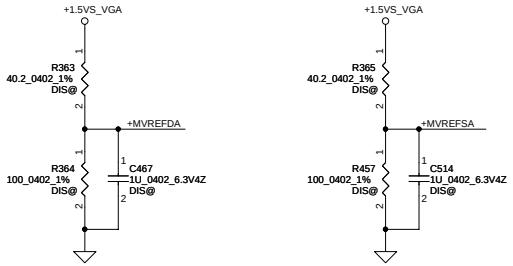
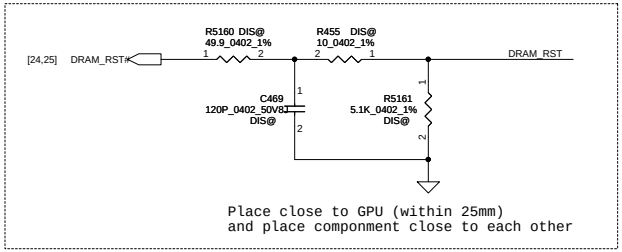
MEM I/F





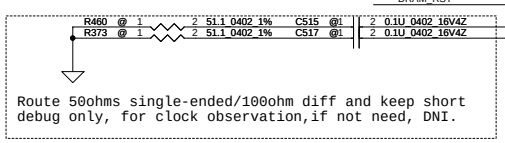
[24,25] M_DA[63..0] → M_DA[63..0]
[24,25] M_MA[15..0] → M_MA[15..0]
[24,25] M_DQM[7..0] → M_DQM[7..0]
[24,25] M_DQS[7..0] → M_DQS[7..0]
[24,25] M_DQS#[7..0] → M_DQS#[7..0]

DIS@
U666C

		GDDR5/DDR3	GDDR5/DDR3		
M_DA0	K27	DQA0_0	MAA0_0/MAA_0	K17	M_MA0
M_DA1	J29	DQA0_1	MAA0_1/MAA_1	J20	M_MA1
M_DA2	H30	DQA0_2	MAA0_2/MAA_2	H23	M_MA2
M_DA3	H32	DQA0_3	MAA0_3/MAA_3	G23	M_MA3
M_DA4	G29	DQA0_4	MAA0_4/MAA_4	G24	M_MA4
M_DA5	F28	DQA0_5	MAA0_5/MAA_5	H24	M_MA5
M_DA6	F32	DQA0_6	MAA0_6/MAA_6	J19	M_MA6
M_DA7	F30	DQA0_7	MAA0_7/MAA_7	K19	M_MA7
M_DA8	C30	DQA0_8	MAA0_8/MAA_13	G20	M_MA13
M_DA9	F27	DQA0_9	MAA0_9/MAA_15	L17	M_MA15
M_DA10	A28	DQA0_10			
M_DA11	C28	DQA0_11	MAA1_0/MAA_8	J14	M_MA8
M_DA12	E27	DQA0_12	MAA1_1/MAA_9	K14	M_MA9
M_DA13	G26	DQA0_13	MAA1_2/MAA_10	J11	M_MA10
M_DA14	D26	DQA0_14	MAA1_3/MAA_11	J13	M_MA11
M_DA15	F25	DQA0_15	MAA1_4/MAA_12	H11	M_MA12
M_DA16	A25	DQA0_16	MAA1_5/MAA_BA2	G11	M_BA2 → M_BA2 [24,25]
M_DA17	C25	DQA0_17	MAA1_6/MAA_BA0	J16	M_BA0 → M_BA0 [24,25]
M_DA18	E25	DQA0_18	MAA1_7/MAA_BA1	L15	M_BA1 → M_BA1 [24,25]
M_DA19	D24	DQA0_19	MAA1_8/MAA_14	G14	M_MA14
M_DA20	E23	DQA0_20	MAA1_9/RSVD	L16	NC
M_DA21	F23	DQA0_21			
M_DA22	D22	DQA0_22	WCKA0_0/DQMA0_0	E32	M_DQM0
M_DA23	F21	DQA0_23	WCKA0B_0/DQMA0_1	E30	M_DQM1
M_DA24	E21	DQA0_24	WCKA0_1/DQMA0_2	A21	M_DQM2
M_DA25	D20	DQA0_25	WCKA0B_1/DQMA0_3	C21	M_DQM3
M_DA26	F19	DQA0_26	WCKA1_0/DQMA1_0	E13	M_DQM4
M_DA27	A19	DQA0_27	WCKA1B_0/DQMA1_1	D12	M_DQM5
M_DA28	D18	DQA0_28	WCKA1_1/DQMA1_2	E3	M_DQM6
M_DA29	F17	DQA0_29	WCKA1B_1/DQMA1_3	F4	M_DQM7
M_DA30	A17	DQA0_30			
M_DA31	C17	DQA0_31		H28	M_DQS0
M_DA32	E17	DQA1_0	EDCA0_0/QSA0_0	C27	M_DQS1
M_DA33	D16	DQA1_1	EDCA0_1/QSA0_1	A23	M_DQS2
M_DA34	F15	DQA1_2	EDCA0_2/QSA0_2	E19	M_DQS3
M_DA35	A15	DQA1_3	EDCA0_3/QSA0_3	E15	M_DQS4
M_DA36	D14	DQA1_4	EDCA1_0/QSA1_0	D10	M_DQS5
M_DA37	F13	DQA1_5	EDCA1_1/QSA1_1	D6	M_DQS6
M_DA38	A13	DQA1_6	EDCA1_2/QSA1_2	G5	M_DQS7
M_DA39	C13	DQA1_7	EDCA1_3/QSA1_3		
M_DA40	E11	DQA1_8		H27	M_DQS#0
M_DA41	A11	DQA1_9	DDBIA0_0/QSA0_0B	A27	M_DQS#1
M_DA42	C11	DQA1_10	DDBIA0_1/QSA0_1B	C23	M_DQS#2
M_DA43	F11	DQA1_11	DDBIA0_2/QSA0_2B	C19	M_DQS#3
M_DA44	A9	DQA1_12	DDBIA0_3/QSA0_3B	C15	M_DQS#4
M_DA45	C9	DQA1_13	DDBIA1_0/QSA1_0B	E9	M_DQS#5
M_DA46	F9	DQA1_14	DDBIA1_1/QSA1_1B	C5	M_DQS#6
M_DA47	D8	DQA1_15	DDBIA1_2/QSA1_2B	H4	M_DQS#7
M_DA48	E7	DQA1_16	DDBIA1_3/QSA1_3B		
M_DA49	A7	DQA1_17	ADBIA0/ODTA0	L18	VRAM_ODT0 → VRAM_ODT0 [24]
M_DA50	C7	DQA1_18	ADBIA1/ODTA1	K16	VRAM_ODT1 → VRAM_ODT1 [25]
M_DA51	F7	DQA1_19			
M_DA52	A5	DQA1_20	CLKA0	H26	M_CLK0 → M_CLK0 [24]
M_DA53	E5	DQA1_21	CLKA0B	H25	M_CLK#0 → M_CLK#0 [24]
M_DA54	C3	DQA1_22			
M_DA55	E1	DQA1_23	CLKA1	G9	M_CLK1 → M_CLK1 [25]
M_DA56	G7	DQA1_24	CLKA1B	H9	M_CLK#1 → M_CLK#1 [25]
M_DA57	G6	DQA1_25			
M_DA58	G1	DQA1_26	RASA0B	G22	M_RAS#0 → M_RAS#0 [24]
M_DA59	G3	DQA1_27	RASA1B	G17	M_RAS#1 → M_RAS#1 [25]
M_DA60	J6	DQA1_28			
M_DA61	J1	DQA1_29	CASA0B	G19	M_CAS#0 → M_CAS#0 [24]
M_DA62	J3	DQA1_30	CASA1B	G16	M_CAS#1 → M_CAS#1 [25]
M_DA63	J5	DQA1_31			
			CSA0B_0	H22	M_CS#0 → M_CS#0 [24]
+MVREFDA	K26	MVREFDA	CSA0B_1	J22	NC
+MVREFSA	J26	MVREFSA			
			CSA1B_0	G13	M_CS#1 → M_CS#1 [25]
	J28		CSA1B_1	K13	NC
R5162 1 DIS@ 2 120_0402_1%	K25	NC#J25			
		MEM_CALRP0	CKEA0	K20	M_CKE0 → M_CKE0 [24]
			CKEA1	J17	M_CKE1 → M_CKE1 [25]
DRAM_RST	L10		WEA0B	G25	M_WE#0 → M_WE#0 [24]
		DRAM_RST	WEA1B	H10	M_WE#1 → M_WE#1 [25]
R460 @ 1 2 51.1_0402_1% C515 @1 2 0.1U_0402_16V4Z	K8	CLKTESTA			
R373 @ 1 2 51.1_0402_1% C517 @1 2 0.1U_0402_16V4Z	L7	CLKTESTB			

MEMORY INTERFACE

216-0841009 A0 SUN XT S3



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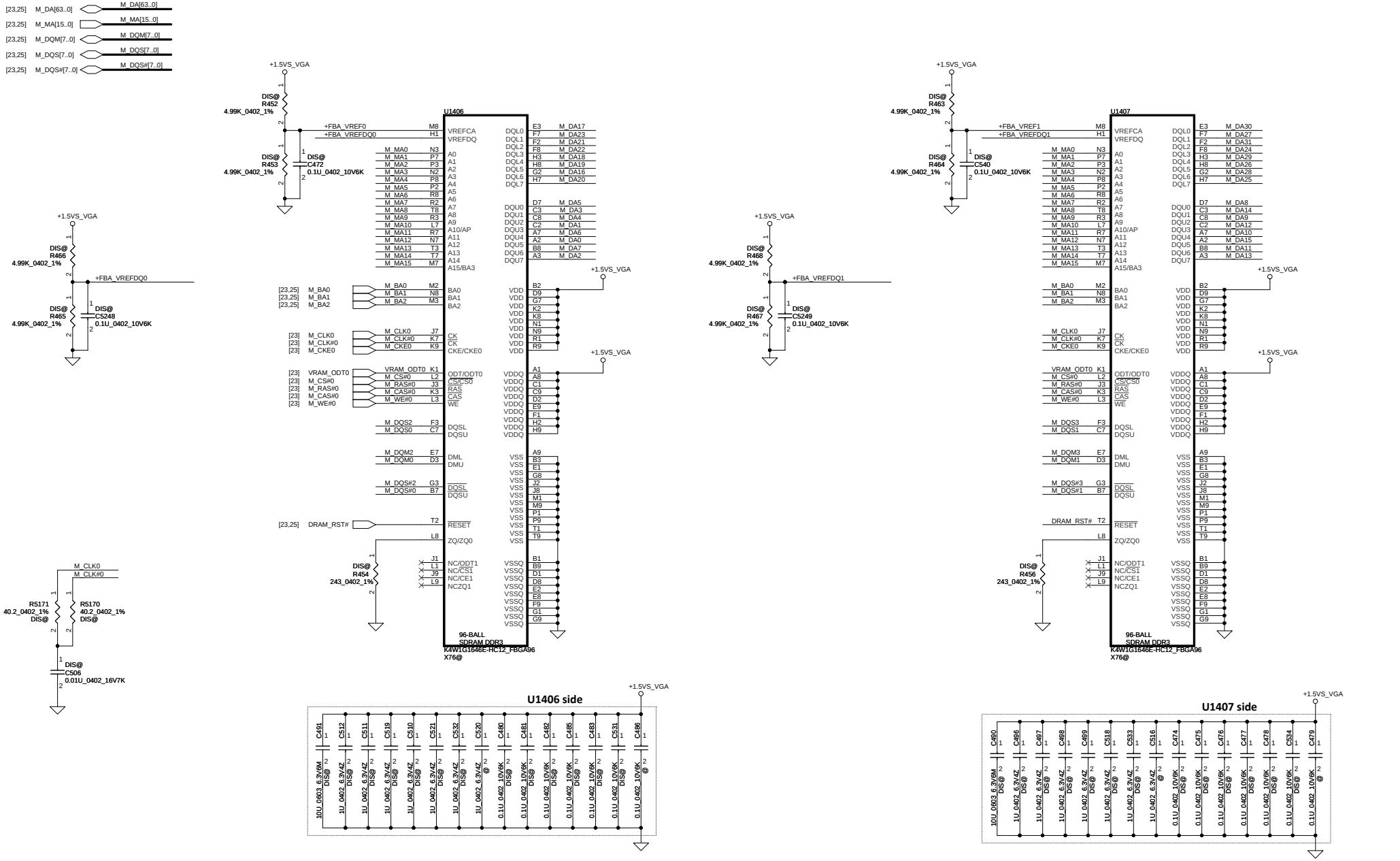
MEM Lower 32-bits



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Issued Date	2013/02/20	Deciphered Date	2012/07/01

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Compal Electronics, Inc.			
Title	SUN_VRAM A Lower		
Size: Custom	Document Number: 4019OJ		Rev: D
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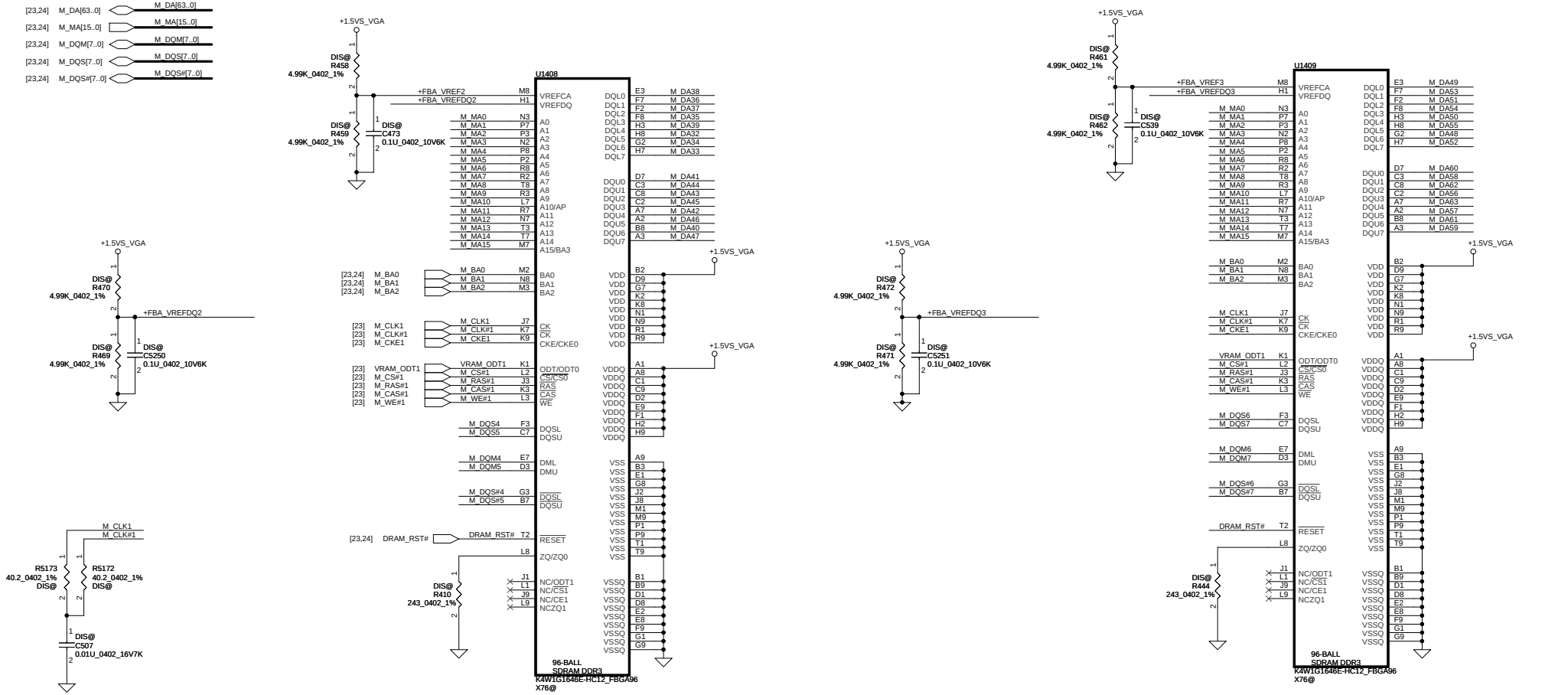
MEM Upper 32-bits



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Title: **SUN_VRAM A Upper**

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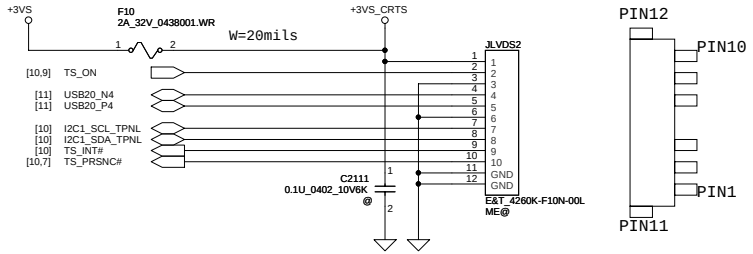
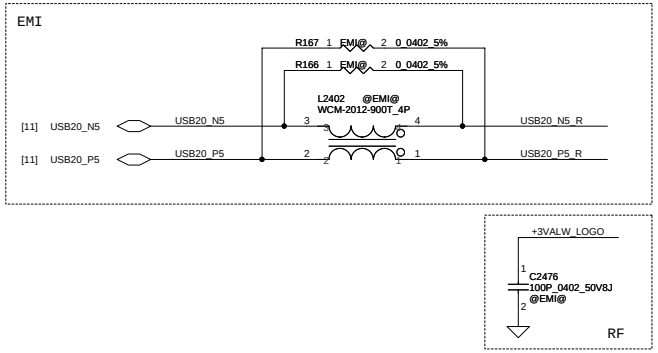
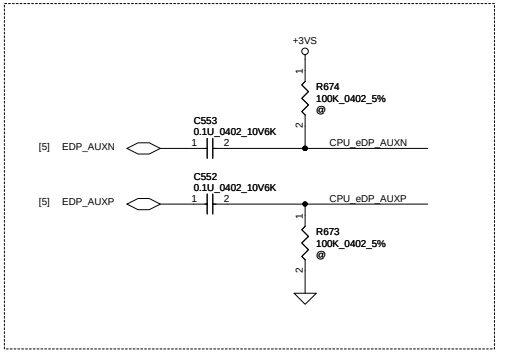
Touch Screen Conn

P/N:SP01000TF10

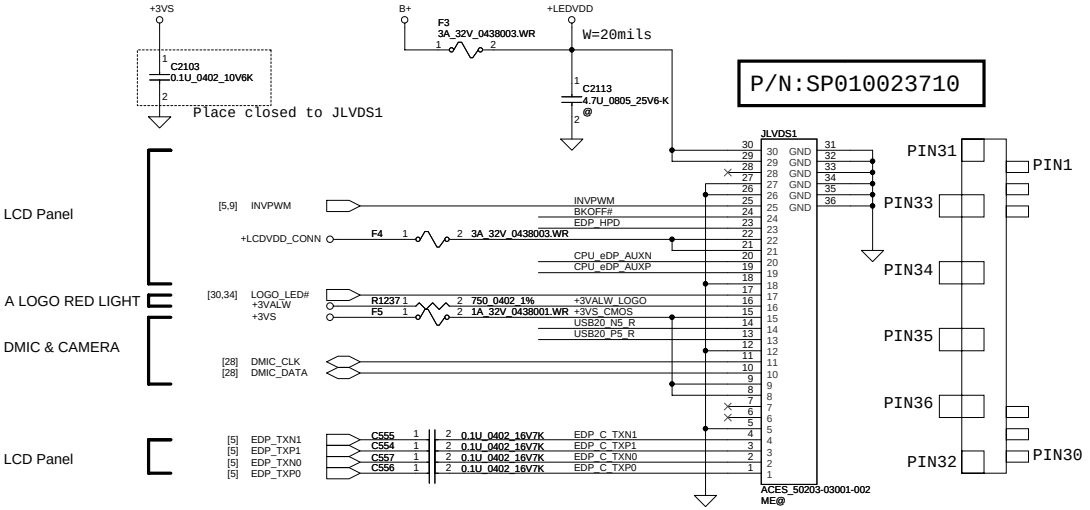


eDP Panel Conn

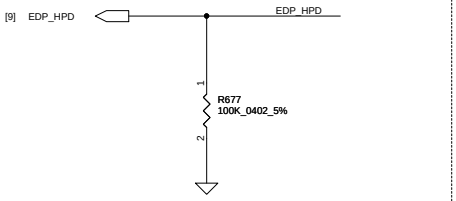


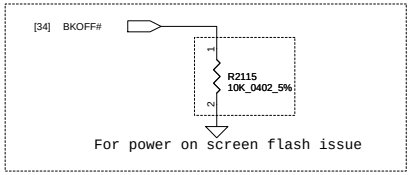


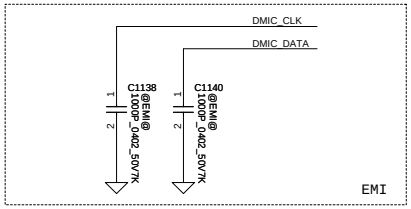
P/N:SP010023710



HPD Inversion for eDP



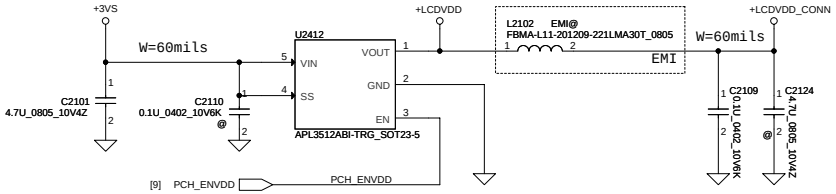




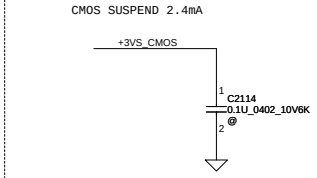
LCD POWER CIRCUIT

SS table

Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS



Camera Modual POWER CIRCUIT



DMIC & CAMERA module pin define

No	SIGNAL
1	VCC (3.3V)
2	D-
3	D+
4	GND_CAM
5	GND_DMIC
6	MIC_C
7	MIC_D
8	MIC_VCC

Touch PANEL module pin define

No	I2C	USB
1,2	VCC (3.3V)	VCC (3.3V)
3	Reset	Reset
4	SDA	NC
5	SCL	NC
6	INT	NC
7	NC	D-
8	NC	D+
9,10	GND	GND

Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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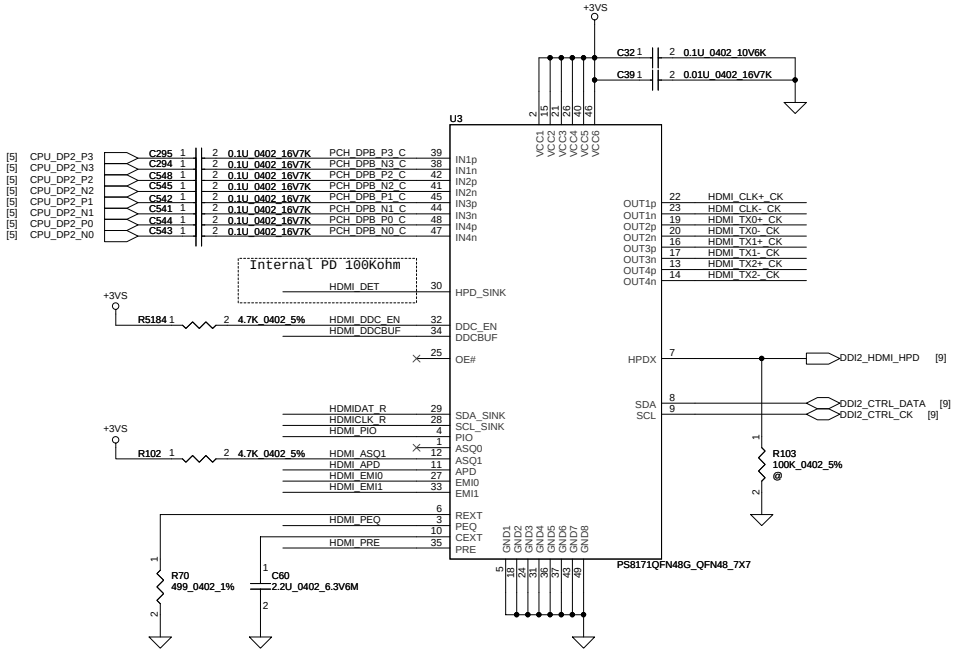
Compal Electronics, Inc.

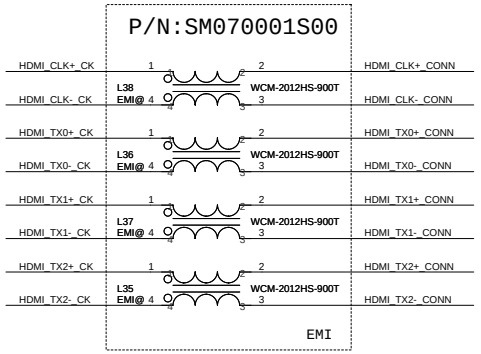
Title: **eDP Connector**

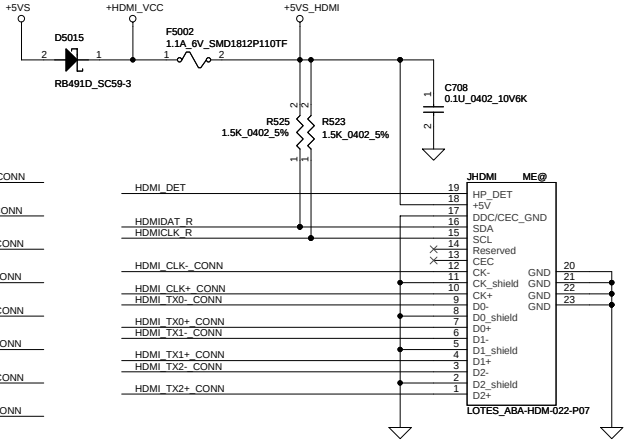
Size: Custom | Document Number: **4019OJ** | Rev: D

Date: Friday, February 28, 2014 | Sheet 26 of 46

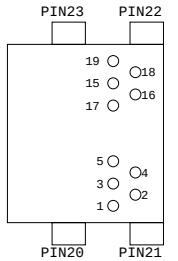
HDMI + Re-driver

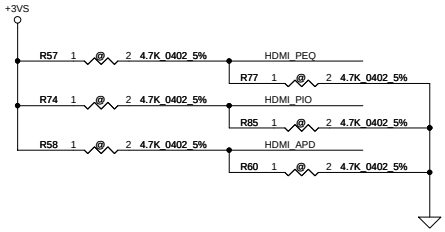


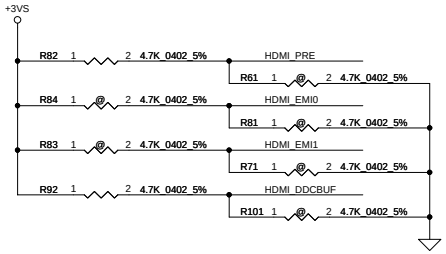




DC232000B10
TYPE A Connector







PS8171 setting table

PEQ:
TMDS inputs equalization control,
L: Mid level EQ (Default)
H: High level EQ
M: Low level EQ

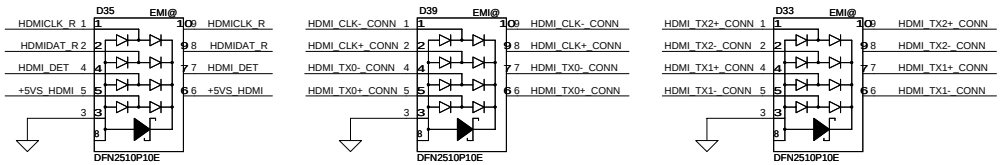
PIO:
Programmable I/O setting.
L: HPD = HPD_SINK @ 3.3V CMOS output (default)
H: HPD= HPD_SINK# (inverted HPD) @ 0.9V

APD:
Automatic power down management (APD)
L: Automatic power down disable
H: Automatic power down enable (default)
M: Reserved

PRE:
TMDS output driver pre-emphasis level setting.
L: No pre-emphasis (default)
H: Low level pre-emphasis is added
M: High level pre-emphasis is added

EMI0/ EMI1:
EMI reduction and filter setting.
[1,0] = HL: No EMI reduction (default)
0 = HIGH: Increased rise/fall time
MID: Increased rise/fall time, 2nd
1 = LOW: EMI filter setting 1
MID: Reserved

DDCBUF:
DDC Active Buffer enable and setting.
LOW: No DDC active buffer,
passive DDC level shifting (default)
HIGH: Active DDC buffer enable, setting 1
MID: Active DDC buffer enable, setting 2



P/N: SC300001Y00

ESD

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Issued Date	2013/02/20	Deciphered Date	2012/07/01

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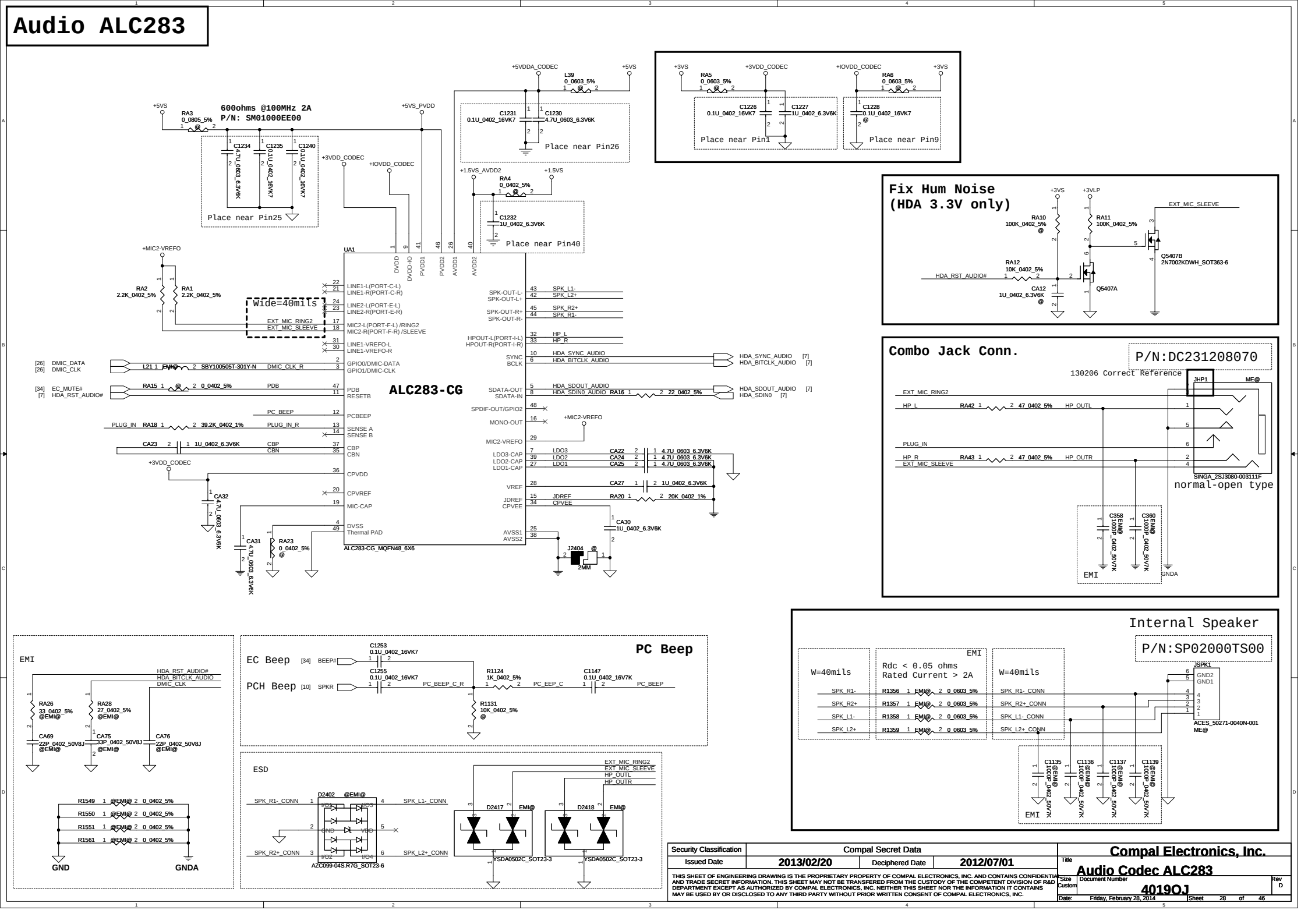
Compal Electronics, Inc.

Title: **HDMI CONN**

Size	Document Number	Rev
Custom	4019OJ	D

Date: Friday, February 28, 2014 Sheet 27 of 46

Audio ALC283



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Issued Date	2013/02/20	Deciphered Date	2012/07/01

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Compal Electronics, Inc.			
Title: Audio Codec ALC283			
Size: Custom	Document Number: 4019OJ		Rev: D
Date: Friday, February 28, 2014		Sheet 28 of 46	

LAN RTL8111GUS

+3_LAN Rising time (10%~90%) >0.5mS and <100mS

+3VALW — W=60mils — J1203 @ JUMP_43X39 — 370mA — +3V_LAN

+3V_LAN — R1239 @ 0_0603_5% — +LAN_VDDREG

C1249 4.7U_0603_6.3V6K SWR@

C1260 0.1U_0402_16V4Z SWR@

These caps close to U1201 : Pin 23

+3V_LAN — C5247 0.1U_0402_16V4Z — C5246 0.1U_0402_16V4Z

These caps close to U1201 : Pin 11,32

W=60mils — +LAN_REGOUT — R1240 LDO@ 0_0603_5% — L1201 SWR@ 2.2UH +-5% NLC252018T-2R2J-N — W=60mils — +LAN_VDD10

C1263 LDO@ 0.1U_0402_16V4Z

C1185 4.7U_0603_6.3V6K SWR@

C1183 0.1U_0402_16V4Z SWR@

C1245 @ 1U_0402_16V7K

C1248 @ 0.1U_0402_16V4Z

C1266 0.1U_0402_16V4Z

C1267 0.1U_0402_16V4Z

C1268 0.1U_0402_16V4Z

(Should be place within 200 mils)
These components close to U1201 : Pin 24

C1245 close to Pin 22 and others for Pin 3,8,30
1uF reserved on Pin 20

+3V_LAN — R2220 @ 10K_0402_5% — LAN_WAKE#

C1239 12P_0402_50V8J — XTLI_R — R1236 @ 0_0402_5% — XTLI

Y1201 25MHZ_10PF_7V25000014 (GND, GND)

C1237 12P_0402_50V8J — XTLO

U1201

C1238/ C1236 Close to Pin 17/18.

LAN_MDI0+	1	MDIP0	HSOP	17	PCIE_PRX_C_DTX_P2
LAN_MDI0-	2	MDIN0	HSON	18	PCIE_PRX_C_DTX_N2
+LAN_VDD10	3	AVDD10	PERSTB	19	PLT_RST_BUF#
LAN_MDI1+	4	MDIP1	ISOLATEB	20	ISOLATEB
LAN_MDI1-	5	MDIN1	LANWAKEB	21	LAN_WAKE#
LAN_MDI2+	6	MDIP2	DVDD10	22	+LAN_VDD10
LAN_MDI2-	7	MDIN2	VDDREG	23	+LAN_VDDREG
+LAN_VDD10	8	AVDD10	REGOUT	24	+LAN_REGOUT
LAN_MDI3+	9	MDIP3	LED2	25	LANLINK_STATUS#
LAN_MDI3-	10	MDIN3	LED1/GPIO	26	LAN_GPIO
+3V_LAN	11	AVDD33	LED0	27	LAN_ACTIVITY#
LAN_CLKREQ#_R	12	CLKREQB	CKXTAL1	28	XTLO
	13	HSIP	CKXTAL2	29	XTLI
	14	HSIN	AVDD10	30	+LAN_VDD10
	15	REFCLK_P	RSET	31	LAN_RSET
	16	REFCLK_N	AVDD33	32	+3V_LAN
			GND	33	

C1238 1 — 2 .1U_0402_16V7K — PCIE_PRX_DTX_P2

C1236 1 — 2 .1U_0402_16V7K — PCIE_PRX_DTX_N2

PCIE_PRX_DTX_P2 [11]
PCIE_PRX_DTX_N2 [11]
PLT_RST_BUF# [19,31,33,34,8,9]

R1244 @ 0_0402_5% — EC_PME# [34]

R1245 @ 0_0402_5% — PCH_PCIE_WAKE# [10,9]

T60 @

R1243 0_0402_5% — [10,8] LAN_CLKREQ#

[11] PCIE_PTX_C_DRX_P2
[11] PCIE_PTX_C_DRX_N2
[8] CLK_PCIE_LAN
[8] CLK_PCIE_LAN#

R1235 2.49K_0402_1%

RTL8111GUS-CG_QFN32_4X4

+3VS — R1238 1K_0402_5% — ISOLATEB — R1242 15K_0402_5%

+V_DAC — TS1202 — LAN_MDI0+ — LAN_MDI0- — LAN_MDI1+ — LAN_MDI1- — LAN_MDI2+ — LAN_MDI2- — LAN_MDI3+ — LAN_MDI3-

TCT1	1	MCT1	24	MCT1	R1260 75_0402_5% — RJ45_GND
TD1+	2	MX1+	23	RJ45_MDO0+	
TD1-	3	MX1-	22	RJ45_MDO0-	R1259 75_0402_5%
TCT2	4	MCT2	21	MCT2	
TD2	5	MX2+	20	RJ45_MDO1+	
TD2-	6	MX2-	19	RJ45_MDO1-	R1257 75_0402_5%
TCT3	7	MCT3	18	MCT3	
TD3+	8	MX3+	17	RJ45_MDO2+	
TD3-	9	MX3-	16	RJ45_MDO2-	R1258 75_0402_5%
TCT4	10	MCT4	15	MCT4	
TD4+	11	MX4+	14	RJ45_MDO3+	
TD4-	12	MX4-	13	RJ45_MDO3-	

350UH_IH-160

C1288 0.01U_0402_16V7K

C1289 EMI@ 100P_1206_2KV8J — EMI

ESD

D1207 EMI@ — LAN_MDI0- / LAN_MDI0+ — LAN_MDI1+ / LAN_MDI1-

D1208 EMI@ — LAN_MDI2- / LAN_MDI2+ — LAN_MDI3+ / LAN_MDI3-

AZC099-04S.R7G_SOT23-6

RJ-45 Conn.
P/N:DC231211131

+3V_LAN

R1241 510_0402_5% — LAN_ACTIVITY#

@ C1270 220P_0402_50V7K

R1246 510_0402_5% — LANLINK_STATUS#

@ C1265 220P_0402_50V7K

JRJ45 ME@

RJ45_MDO0+	1	Yellow LED+	9
RJ45_MDO0-	2	Yellow LED-	10
RJ45_MDO1+	3	PR1+	1
RJ45_MDO2+	4	PR1-	2
RJ45_MDO2-	5	PR2+	3
RJ45_MDO1-	6	PR3+	4
RJ45_MDO3+	7	PR3-	5
RJ45_MDO3-	8	PR2-	6
		PR4+	7
		PR4-	8
		Green LED+	11
		Green LED-	12

GND 14 — GND 13 — LANGND1

SANTA_130456-401

PIN17 PIN16 PIN15 PIN14

1	2	9	10
3	4		
5	6		
7	8		
11	12		
13			

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Compal Electronics, Inc.

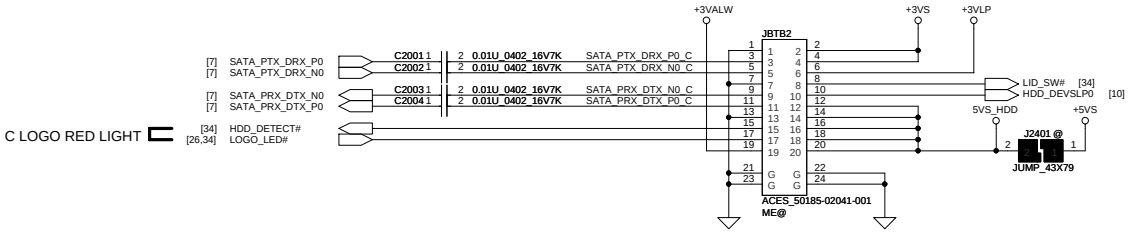
Title: LAN RTL8111GS

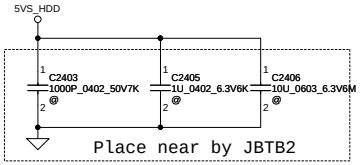
Size: Custom — Document Number: 4019OJ — Rev: D

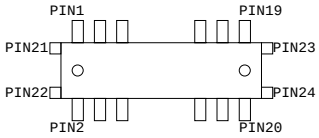
Date: Friday, February 28, 2014 — Sheet 29 of 46

SATA HDD BTB Conn

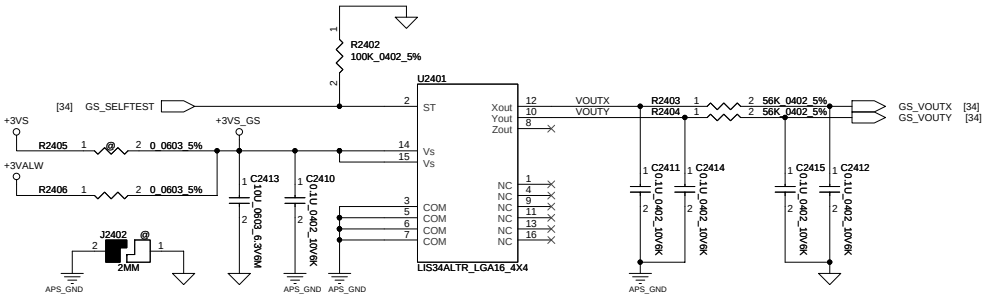
P/N:SP011208141





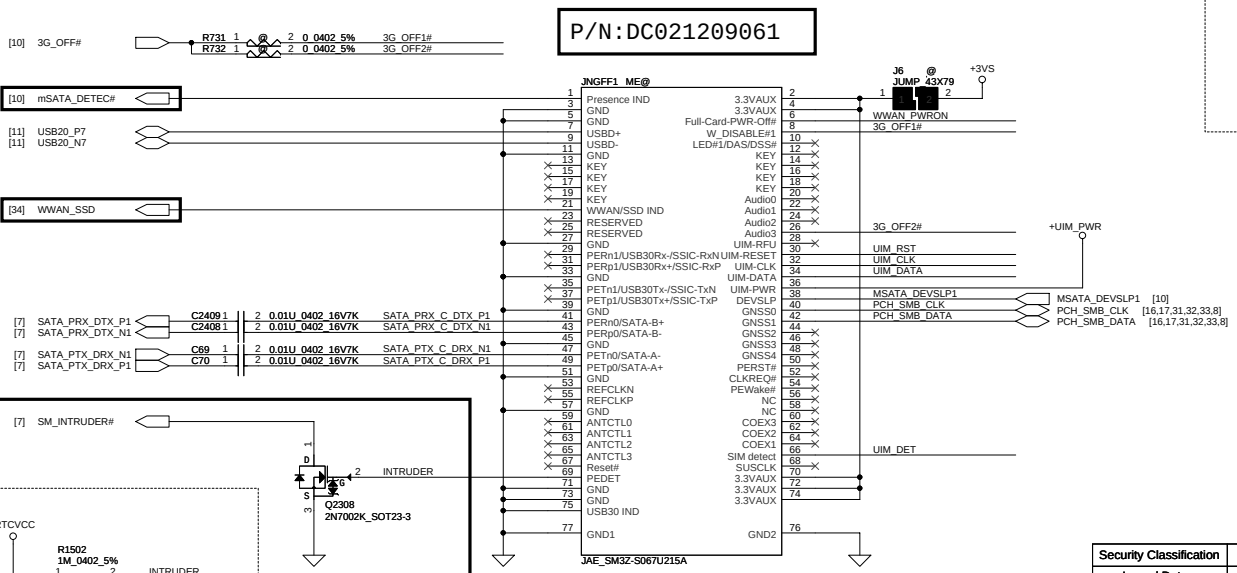


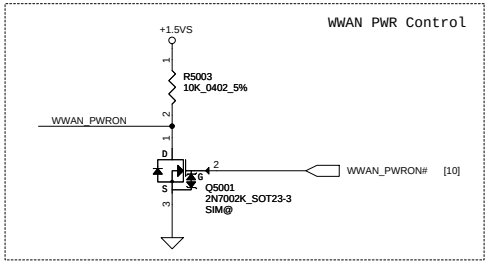
APS G-Sensor

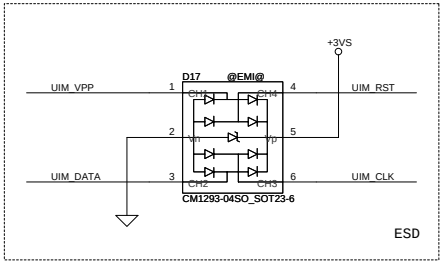


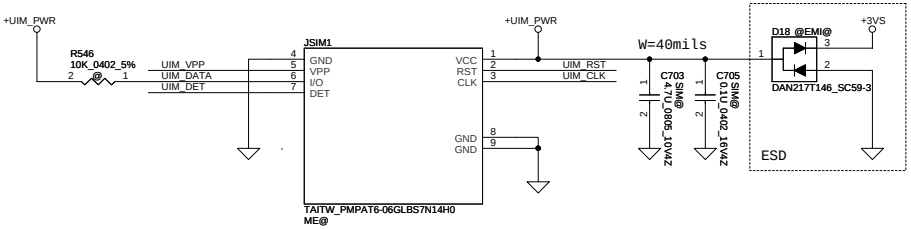
NGFF mSATA/WWAN Conn

P/N:DC021209061









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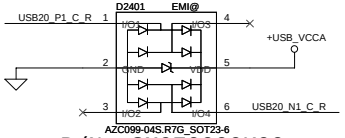
Title: HDD/NGFF/G-Sensor			
Size: Custom	Document Number: 4019OJ		Rev: D
Date: Friday, February 28, 2014	Sheet 30 of 46		

USB30 Conn

ESD



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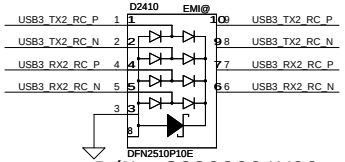

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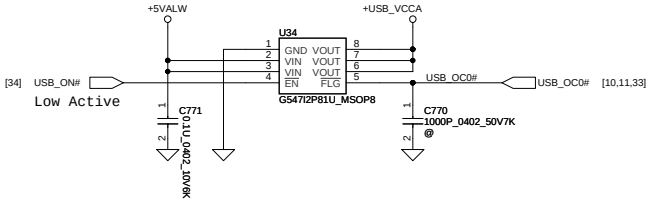

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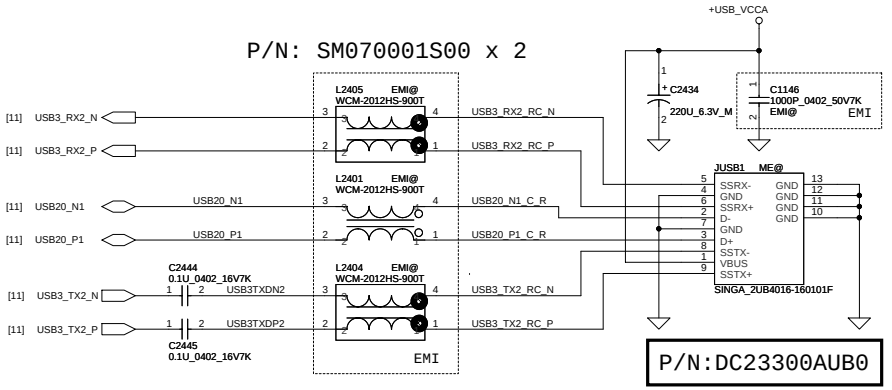


P/N:DC23300AUB0

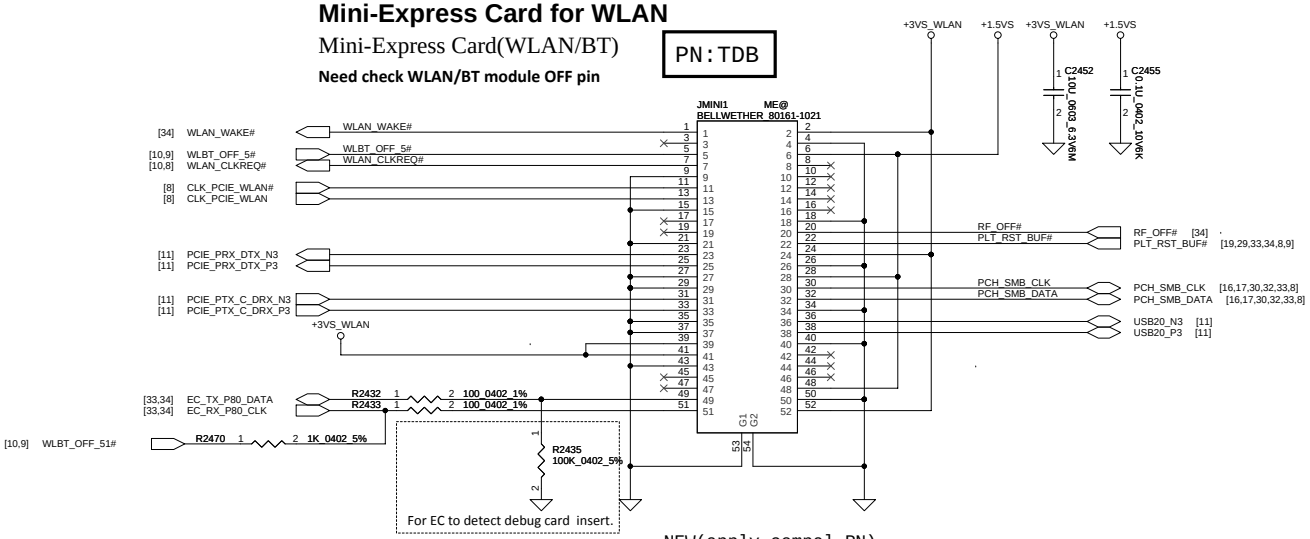
WLAN Mini Card

Mini-Express Card for WLAN

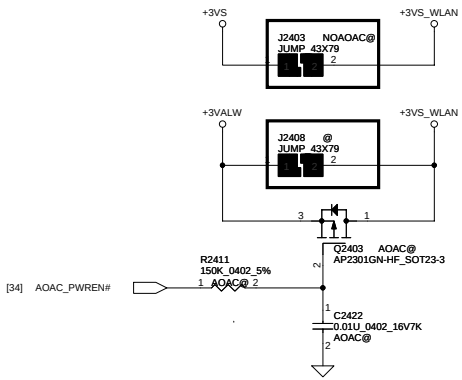
Mini-Express Card(WLAN/BT)

PN:TDB

Need check WLAN/BT module OFF pin

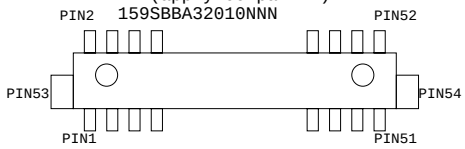


J2403 For NOAOAC
J2408 For AOAC (Default N/A)



Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

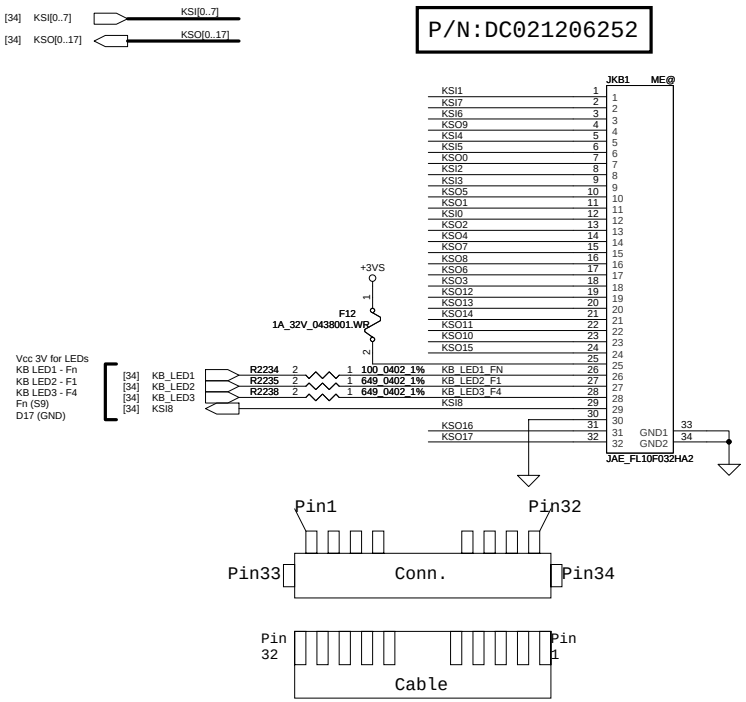
Title: **USB-3.0/MINI-PCIE/G-Sensor**

Size	Document Number	Rev
Custom	4019OJ	D

Date: Friday, February 28, 2014 Sheet 31 of 46

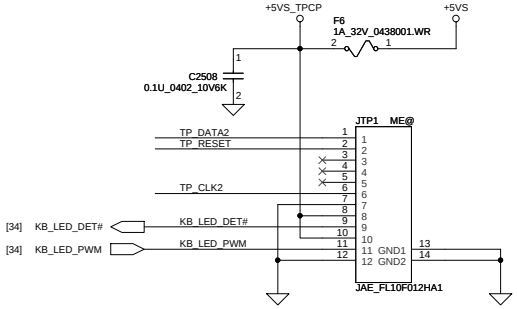
Int KB Conn

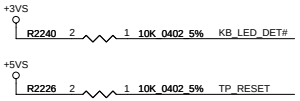
P/N:DC021206252

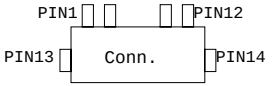


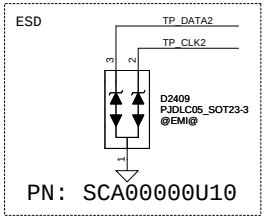
Track Point

P/N:SP01001BF00



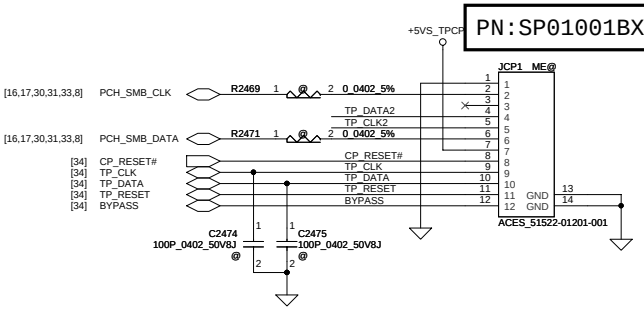


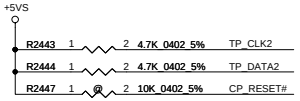


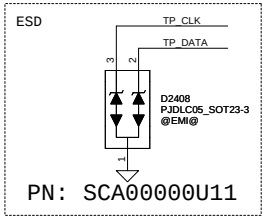


Click PAD

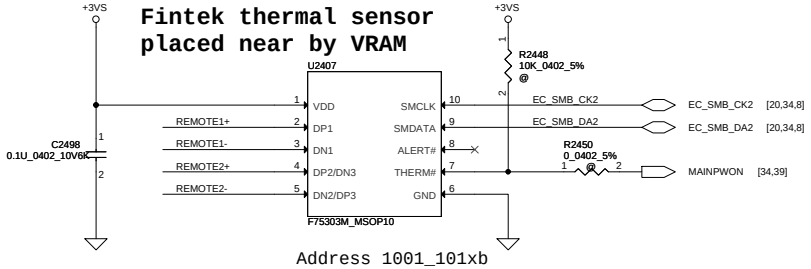
PN:SP01001BX00



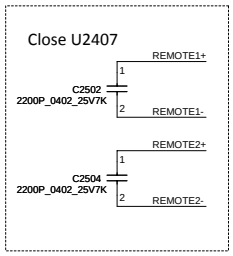


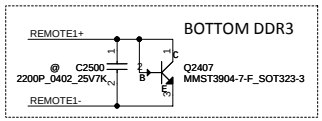


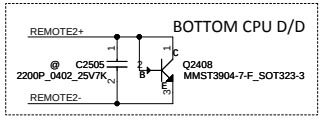
THRM Sensor



Address 1001_101xb
2nd source
SA000029210-->EMC1403-2-AIZL-TR

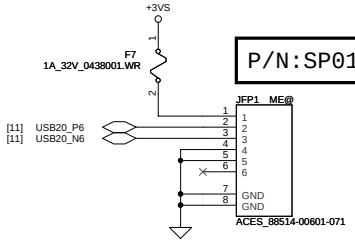






REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Finger Print CONN.



FP module pin define
(CDK1167)

No	SIGNAL
1	+3.3VCC
2	D+
3	D-
4	GND
5	GND
6	NC

Track Point pin define

NO	Signal
1	IPD DATA
2	IPD RST
3	NC
4	NC
5	NC
6	IPD CLK
7	GND
8	VCC5
9	BKLITE DEC
10	LED VCC5
11	LED PWM
12	LED GND

Click PAD pin define

NO	Signal
1	GND
2	SMB CLK
3	NC
4	DATA-TP
5	CLK-TP
6	SMB-DATA
7	VDD
8	RESET
9	CLK
10	DATA
11	TP4RST
12	BYPASS

Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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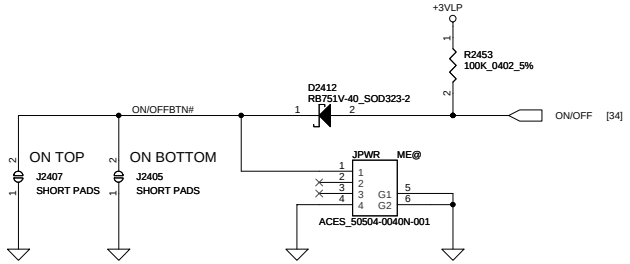
Compal Electronics, Inc.

Title: KB/CP/TP/FP/Thermal Sensor

Size: Custom | Document Number: 4019OJ | Rev: D

Date: Friday, February 28, 2014 | Sheet 32 of 46

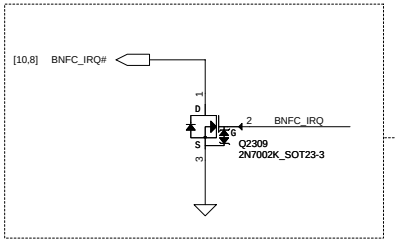
PWRBTN Conn

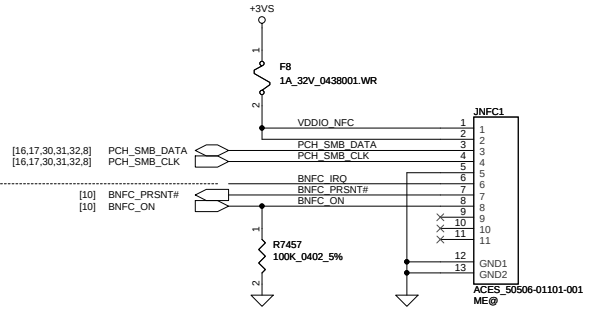


P/N:SP01000Z300

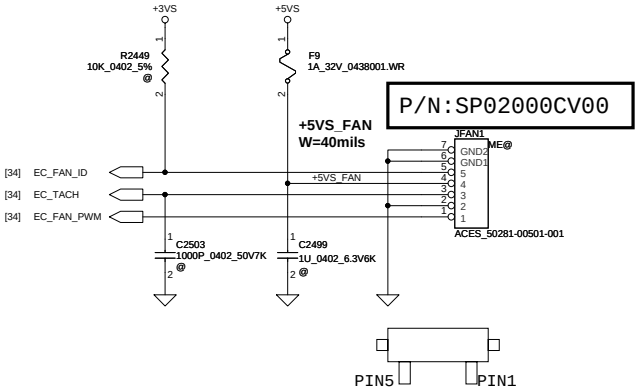
NFC

Module Pin define
1.IP/VBAT
2.IP/VDDIO
3.IO/I2C-SDA
4.I/I2C-SCL
5.G/GND
6.O/IRQ-NFC
7.O/NFC_Presence#
8.I/REG_UP
9.OP/VDD_Ext_SE
10.IP/UIM_PWR
11.IO/SWP

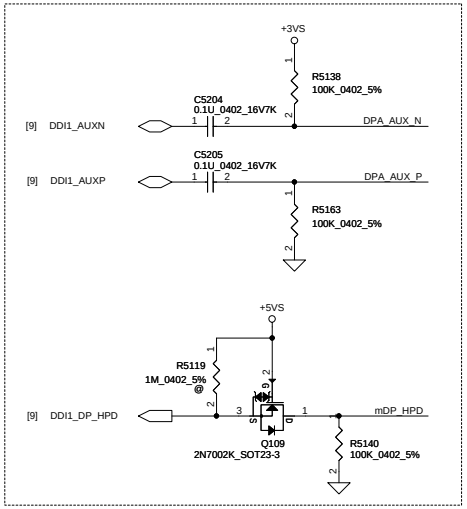




FAN Conn

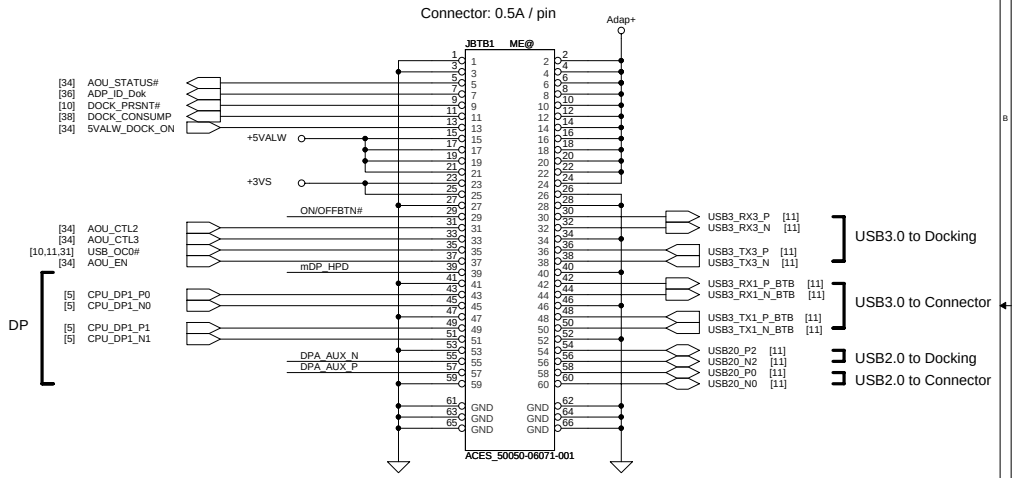


P/N:SP02000CV00

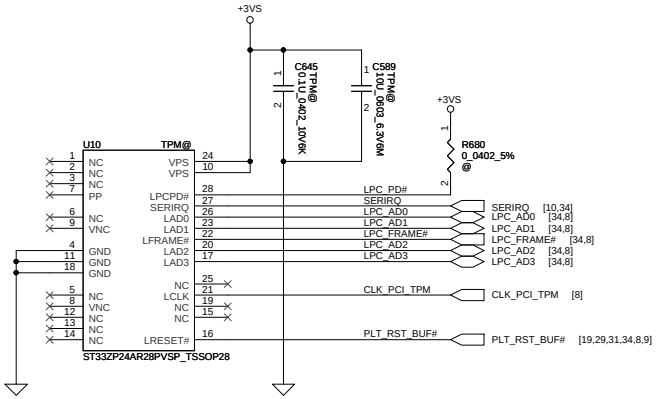


I/O Board Conn

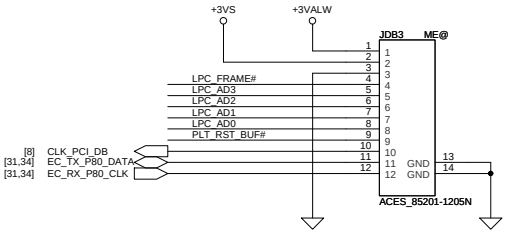
P/N:SP01001BY00



TPM

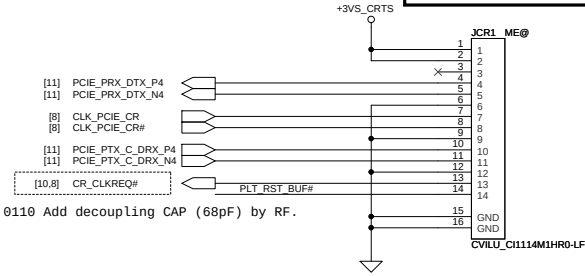


Debug Conn



Card Reader Conn

P/N:SP02000QS00



0110 Add decoupling CAP (68pF) by RF.

Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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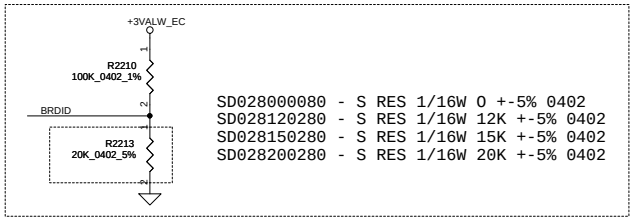
Compal Electronics, Inc.			
Title	PBTN/FAN/TPM/RTC/IO Board		
Size: Custom	Document Number: 4019OJ		Rev: D
Date: Friday, February 28, 2014	Sheet 33 of 46		

EC KB9012

KB9012 A4 v.22	
GPIO W/O internal-PH:	
1. GPIO44	6. GPIO4B
2. GPIO45	7. GPIO4E
3. GPIO46	8. GPIO4F
4. GPIO47	9. GPIO50
5. GPIO4A	10.GPIO5B

Vcc	3.3V +/- 5%				
R2210	100K +/- 1%				
Board ID	R2213	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD
SDV	0K +/- 5%		0.000V	0.300V	0x00 - 0x0B
FVT	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
SIT	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
SVT	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30



SD028000080 - S RES 1/16W 0 +-5% 0402
SD028120280 - S RES 1/16W 12K +-5% 0402
SD028150280 - S RES 1/16W 15K +-5% 0402
SD028200280 - S RES 1/16W 20K +-5% 0402

Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

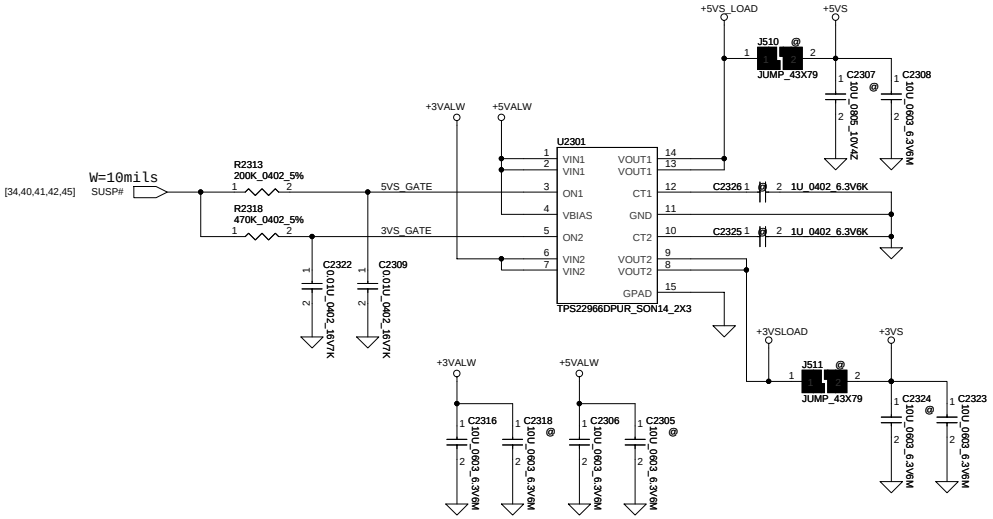
Title: EC ENE-KB9012

Size: Custom | Document Number: 4019OJ | Rev: D

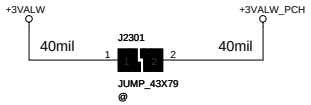
Date: Friday, February 28, 2014 | Sheet 34 of 46

DC/DC I/F

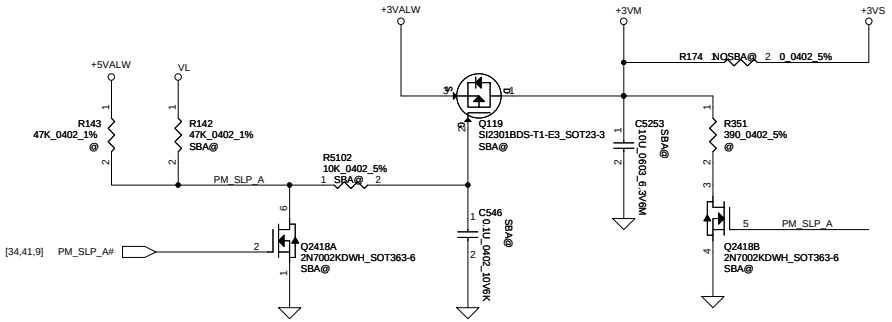
+5VALW TO +5VS
+3VALW TO +3VS



+3VALW TO +3VALW(PCH AUX Power)

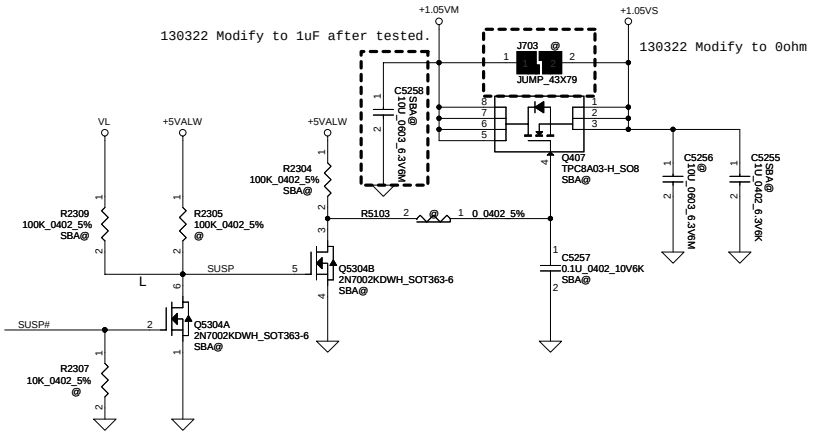


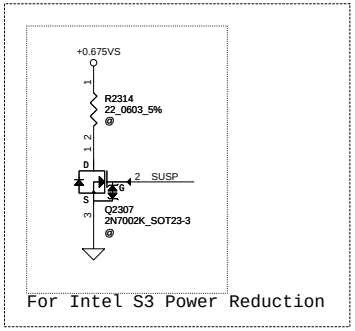
+3VALW TO +3VM (SBA)



PJ703 Short => NOSBA
PJ703 Open => SBA

Rds(on) VGS=4.5V,ID=8.5A,7mOhm(Max)





Security Classification	Compal Secret Data		
Issued Date	2013/02/20	Deciphered Date	2012/07/01

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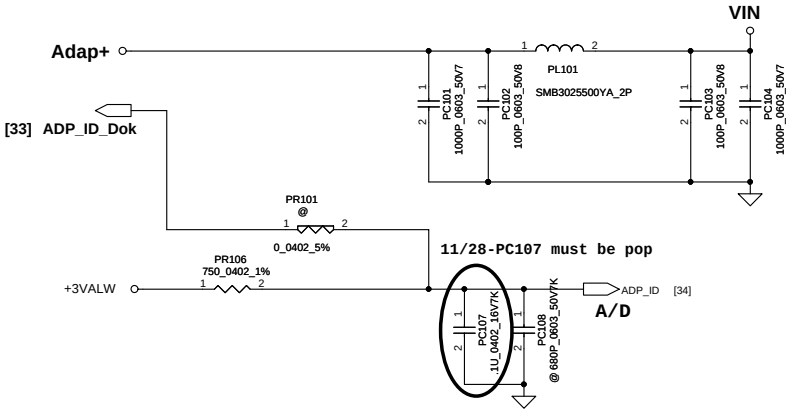
Compal Electronics, Inc.

Title: **DC Interface**

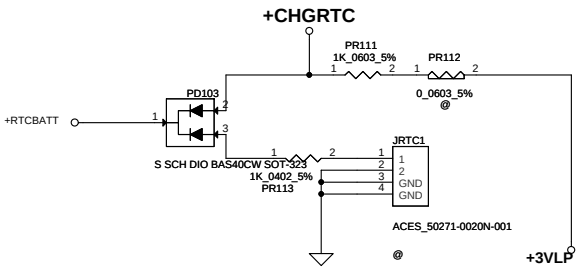
Size	Document Number	Rev
Custom	4019OJ	D

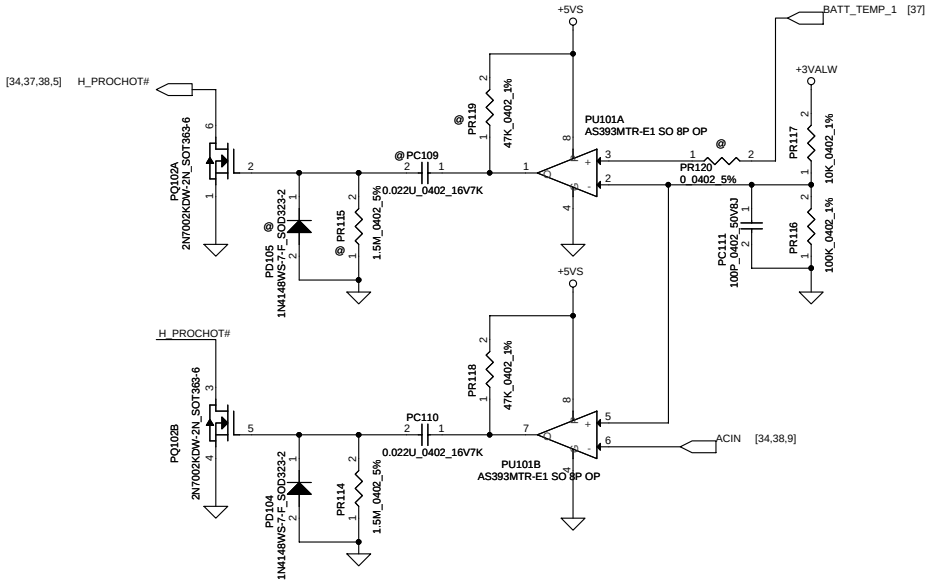
Date: Friday, February 28, 2014 | Sheet 35 of 46



ADP_ID

AC Adapter	45W	65W	90W
R(ohm)	118	287	549
ADP_ID(V)	0.449	0.913	1.395
Detection -Voltage(V)	<=0.663, >0.234	<=1.134, >0.693	<=1.618 >1.172





Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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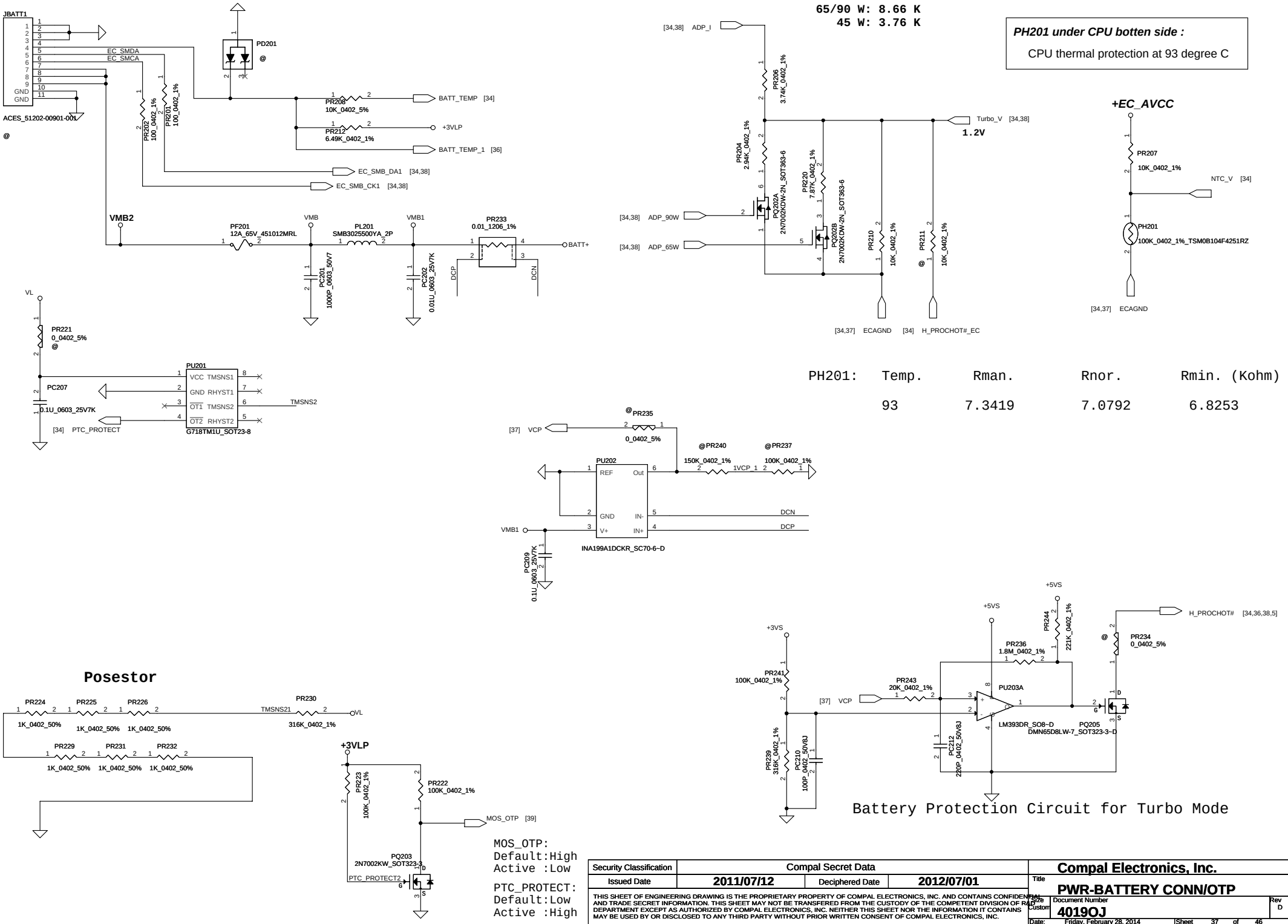
Compal Electronics, Inc.

Title: **PWR-DCIN**

Size: Custom | Document Number: **4019OJ** | Rev: D

Date: Friday, February 28, 2014 | Sheet 36 of 46



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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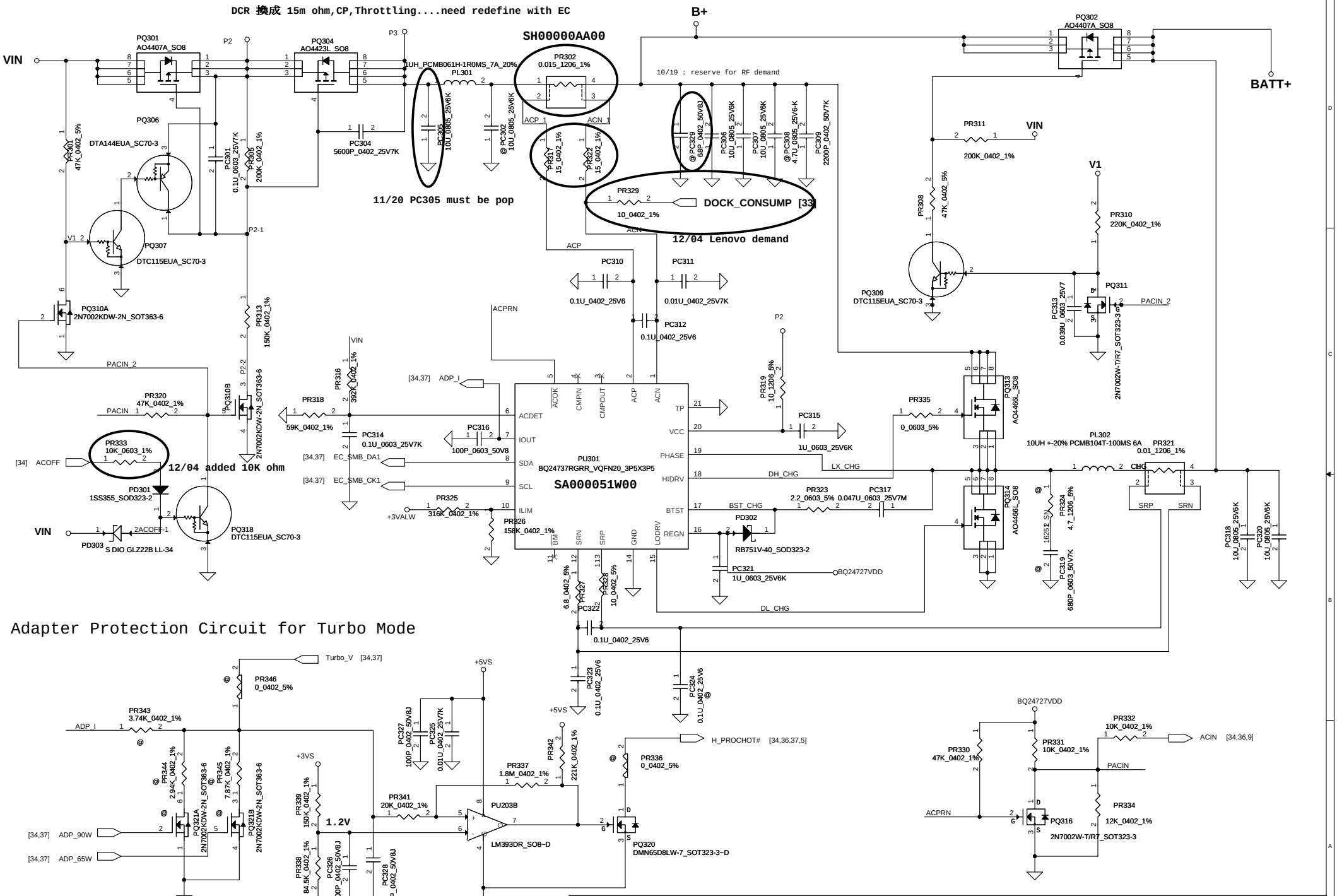
Compal Electronics, Inc.

Title: **PWR-BATTERY CONN/OTP**

Size: Custom | Document Number: **4019OJ** | Rev: D

Date: Friday, February 28, 2014 | Sheet 37 of 46



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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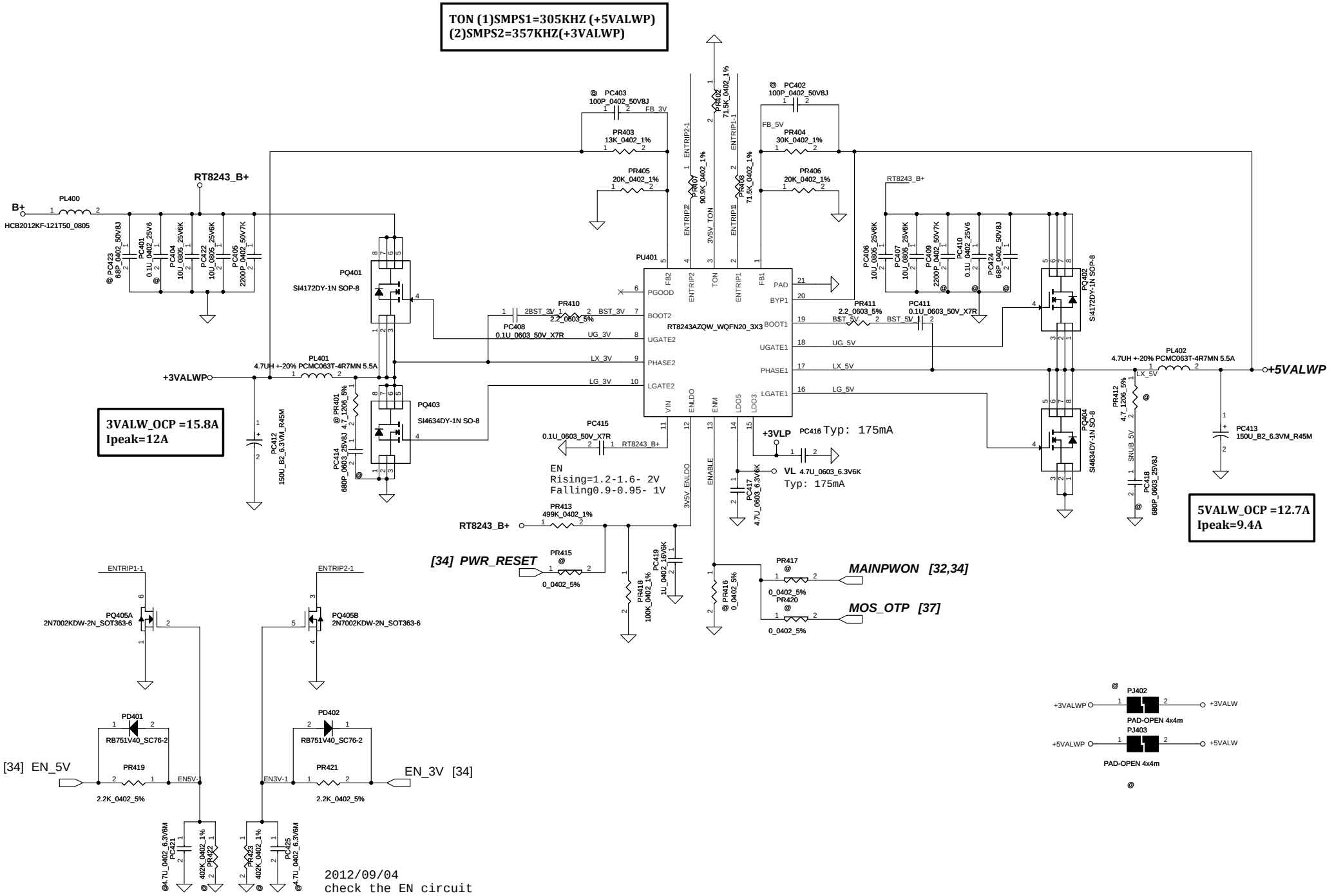
Compal Electronics, Inc.

Title: **PWR-CHARGER**

Size: Custom | Document Number: **4019OJ** | Rev: D

Date: Friday, February 28, 2014 | Sheet 38 of 46

TON (1)SMPS1=305KHZ (+5VALWP)
(2)SMPS2=357KHZ(+3VALWP)



2012/09/04
check the EN circuit

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Compal Electronics, Inc.			
Title	PWR-3VALWP/5VALWP		
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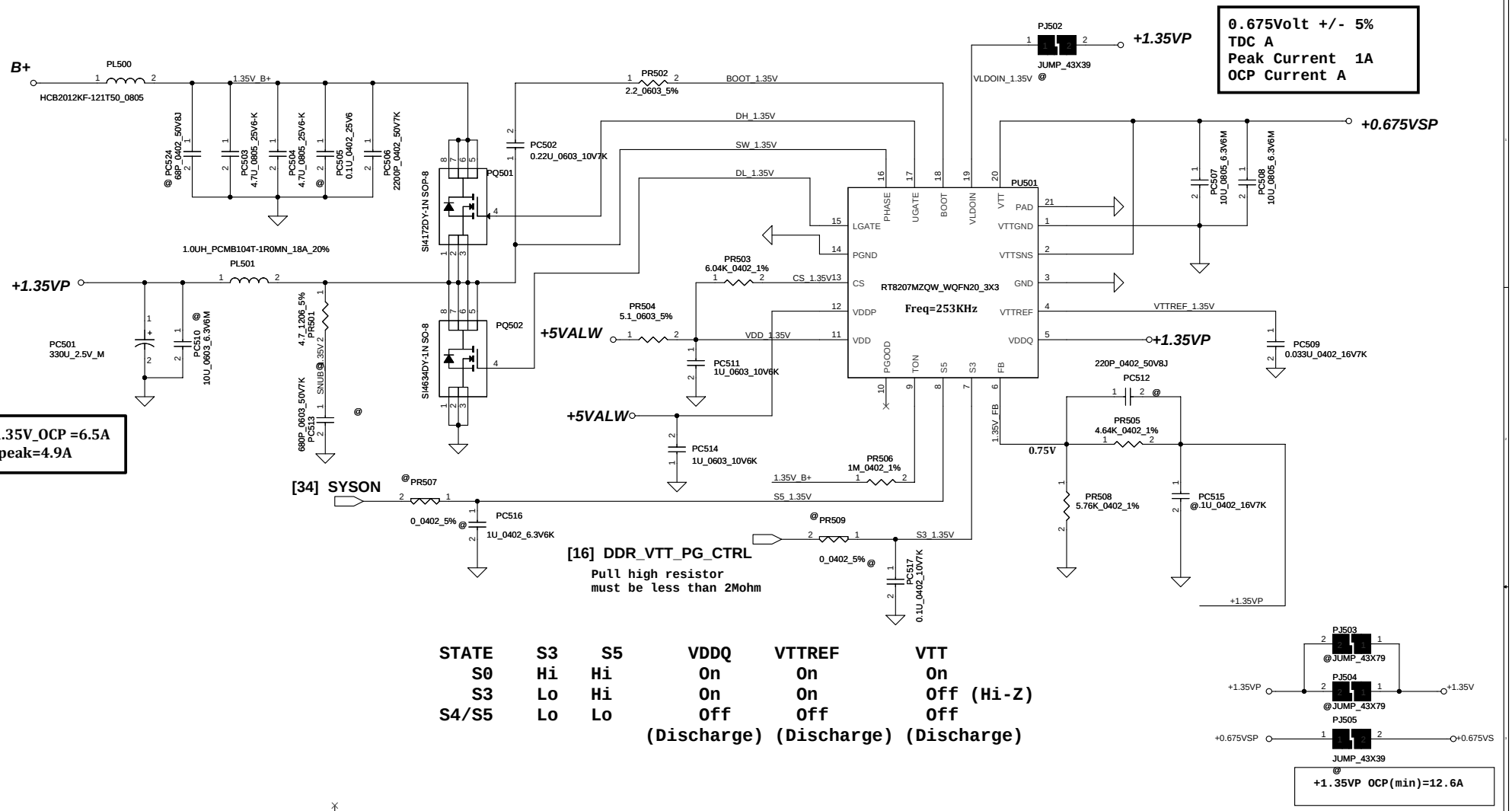
Date:	Friday, February 28, 2014	Sheet	39 of 46



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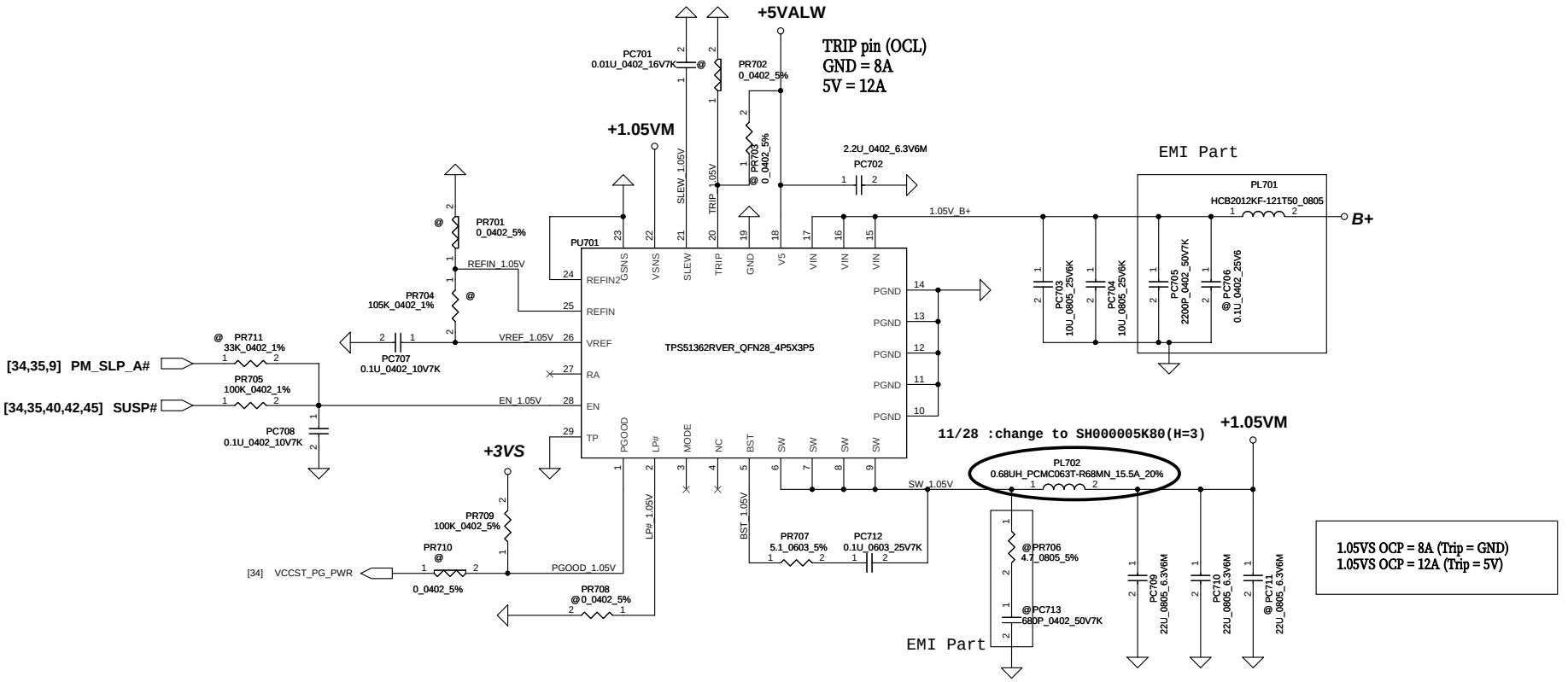
Compal Electronics, Inc.

Title: **PWR-+1.35VP/+1.8VSP**

Size: Custom | Document Number: **4019OJ** | Rev: D

Date: Friday, February 28, 2014 | Sheet 40 of 46



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Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title: **PWR-+1.05VM**

Size: Custom | Document Number: **4019OJ** | Rev: D

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GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

ISEN1_VGA是否要加

ISEN2_VGA是否要加

+VGA_CORE Near VGA Core

Layout Note:
Place near Phase1 Choke

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Compal Electronics, Inc.

Title: **PWR-+VGA_COREP**

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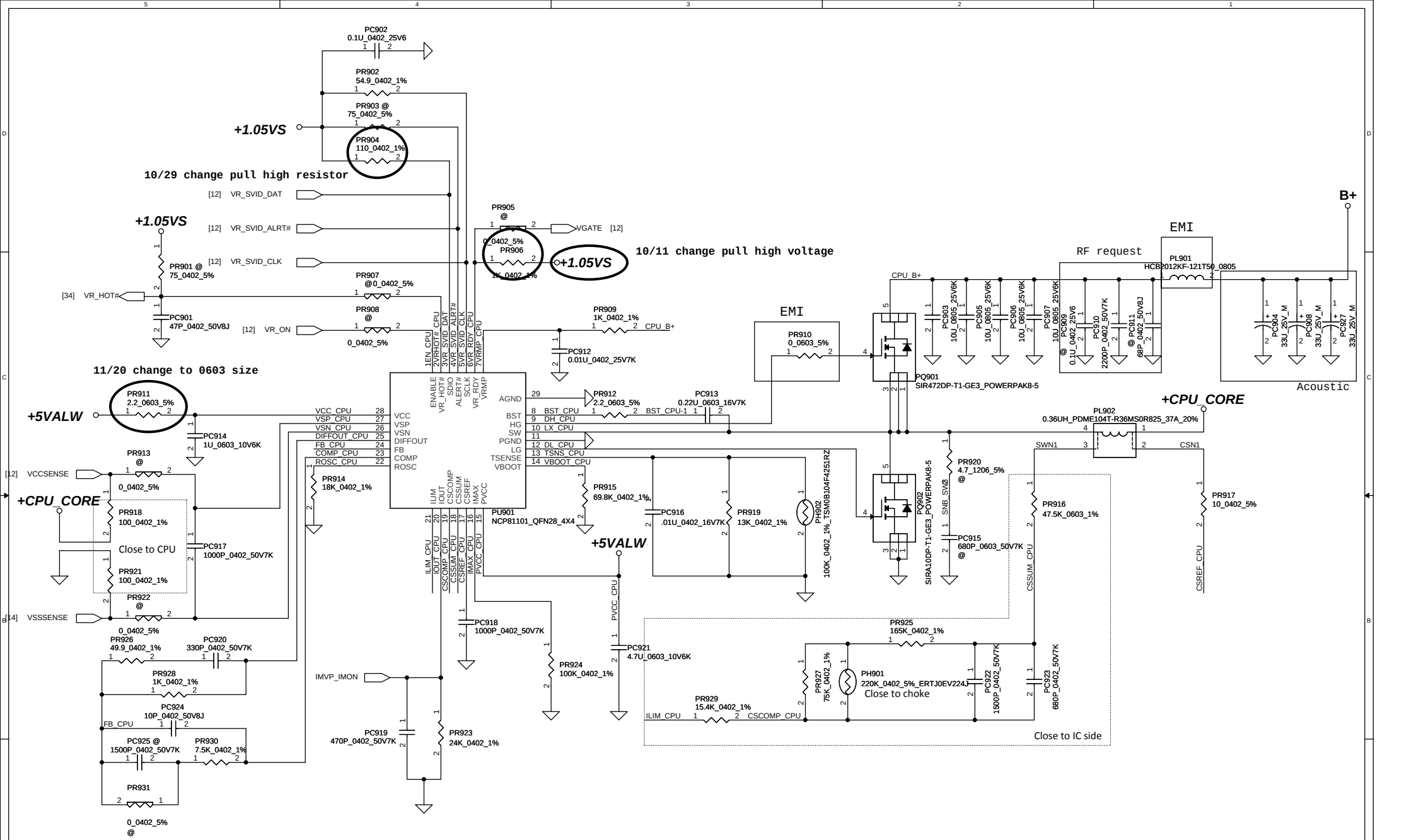

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Compal Electronics, Inc.

Title: **PWR-CPU_CORE**

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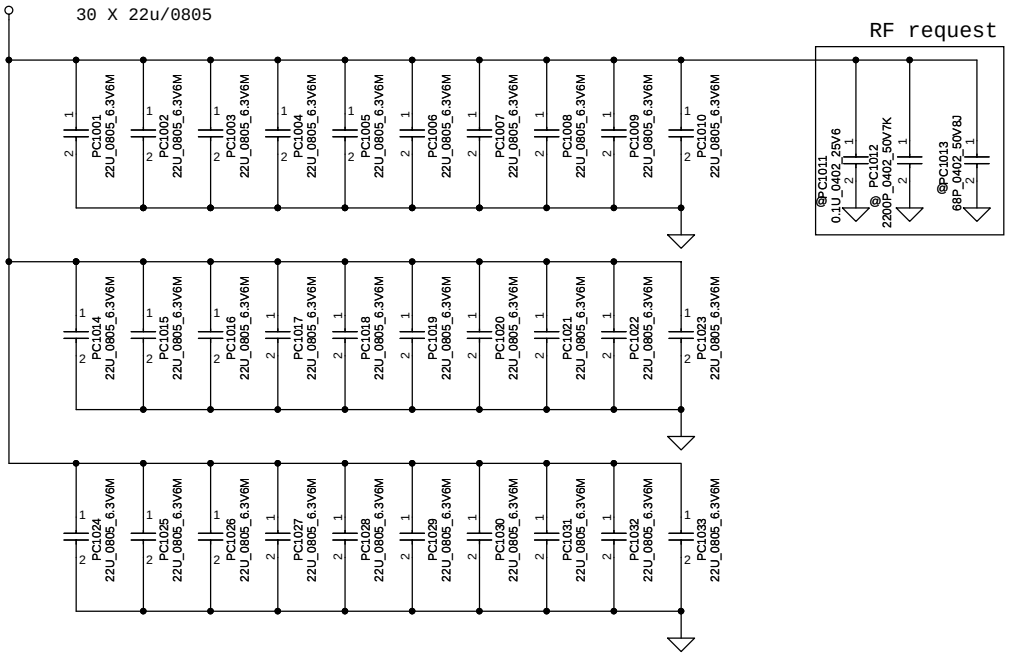
+CPU_CORE

30 X 22u/0805



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Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title: **PWR-PROCESSOR_DECOUPLING**

Size: Custom | Document Number: **4019OJ** | Rev: D

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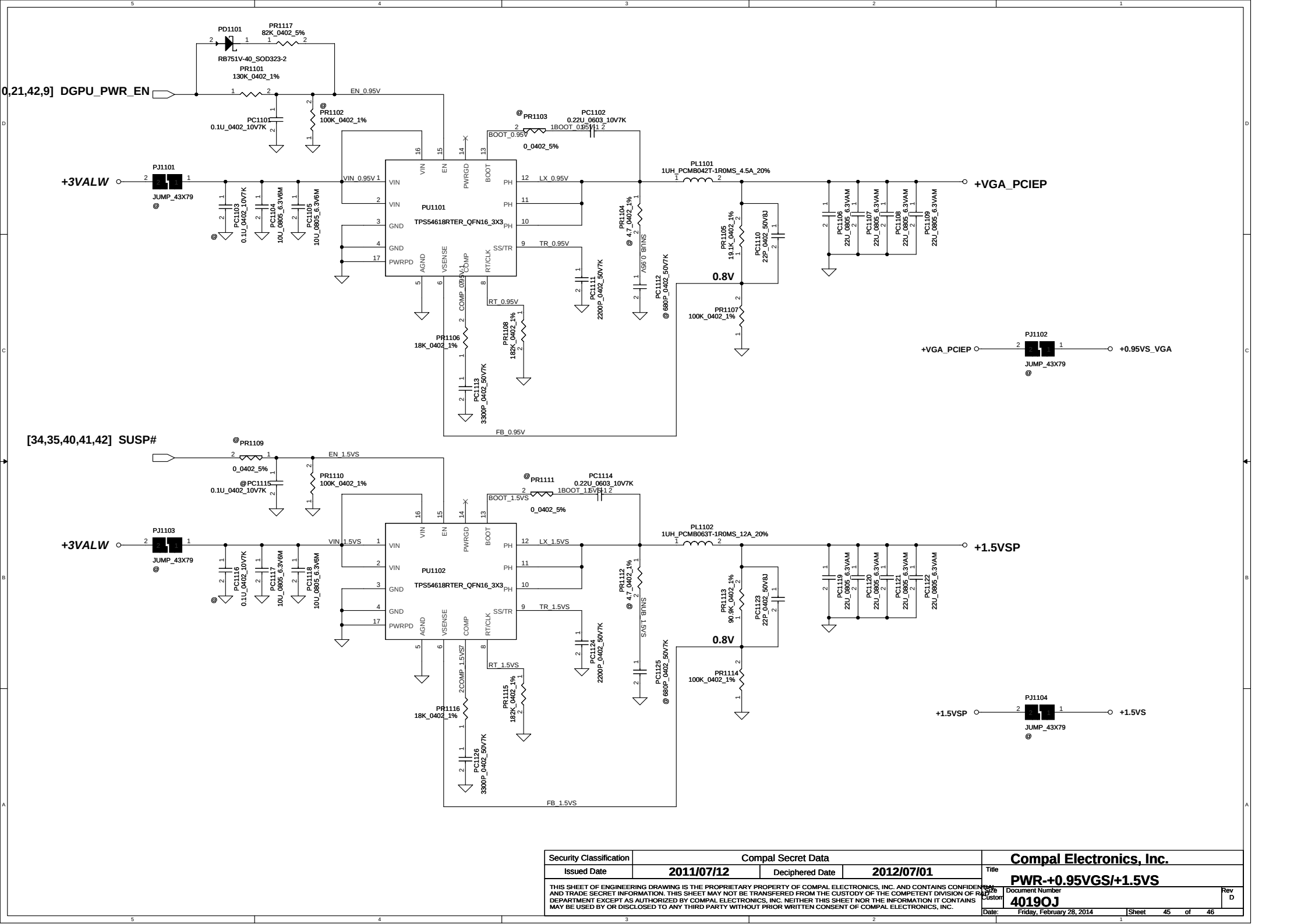

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Compal Electronics, Inc.

Title: **PWR-+0.95VGS/+1.5VS**

Size: Custom | Document Number: **4019OJ** | Rev: D

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	0 ohm change to short pad		PR101, PR221, PR415, PR417, PR420, PR710, PR815, PR832, PR843, PR848, PR859, PR905, PR907 , PR908, PR913, PR922, PR112		
2	HW's request, add SBC function.		net name from "PM_SLP_A#" to "M_PWR_ON"		
3	Increase charger current limit.		PR326 changes from 100k to 158k		
4	Shortage on 0.33u capacitor.		PR705 changes to 100k & PC708 changes to 0.1u		
5	HW changes power sequence.	P41	PR711 from 100k to 33k		FVT
6	Disable BATT one shoot circuit	P36	Unpop PR120, PC109, PC115, PR119, PD105	2013/04/25	SIT
7	0 ohm change to short pad	ALL	PR346, PR1103, PR1111, PR234, PR235, PR336, PR701, PR702, PR931, PR507, PR509, PR512, PR1109	2013/04/30	SIT
8					
9					
10					
11					
12					
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17					

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Compal Electronics, Inc.

Title: **PIR (PWR)**

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