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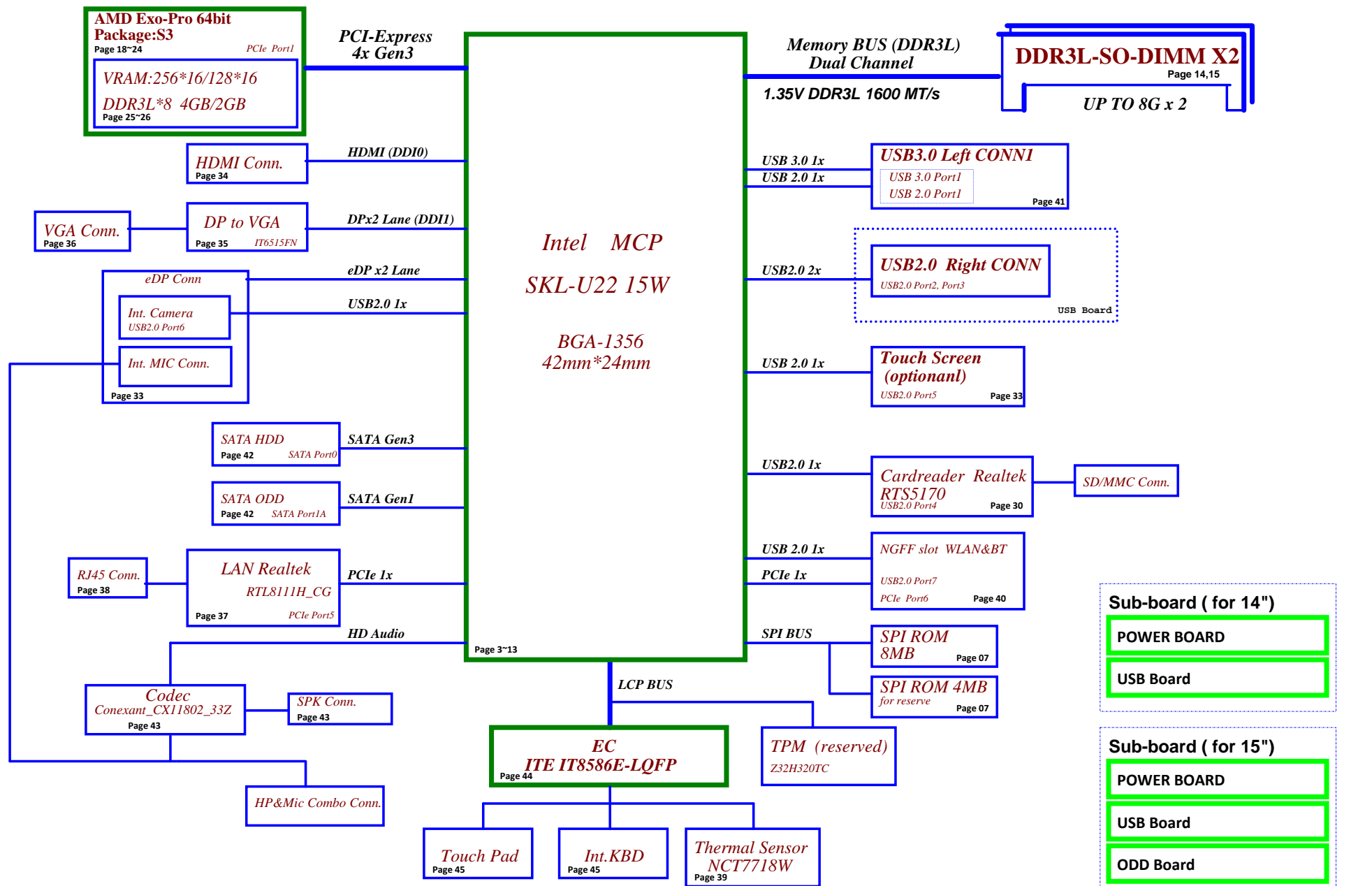
BMWQ1/Q2 M/B Schematics Document

Intel Skylake U22 with DDRIII L + AMD Exo-Pro-S3 GPU

2015-06-02

REV:0.3

| | | | | | | | |
|---|--|------------------------------|--|-----------------|------------------------|---|-------|
| Security Classification | | LC Future Center Secret Data | | Title | |  | |
| Issued Date | | 2014/12/11 | | Deciphered Date | | 2015/12/11 | |
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| | | | | Custom | BMWQ1 | | 0.3 |
| | | | | Date: | Tuesday, June 02, 2015 | | Sheet |



Voltage Rails (O --> Means ON , X --> Means OFF)

| Power Plane / State | B+ | +3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW | +1.35V +VCCST | +5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.675VS |
|--------------------------------|----|--|------------------|---|
| S0 | O | O | O | O |
| S3 | O | O | O | X |
| S3 Battery only | O | O | O | X |
| S5 S4/AC Only | O | O | X | X |
| S5 S4 Battery only | O | X | X | X |
| S5 S4 AC & Battery don't exist | X | X | X | X |

| STATE | SIGNAL | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|----------------------|--------|---------|---------|---------|-------|-----|-----|-------|
| Full ON | | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S3 (Suspend to RAM) | | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | | LOW | LOW | LOW | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | | LOW | LOW | LOW | ON | OFF | OFF | OFF |
| | | | | | | | | |

| HSIO PORT | Function | BOM Structure | BTO Item |
|-----------|----------------------|---------------|---------------------------|
| USB3.0 | 1 USB3.0 CONN left | @ | Not stuff |
| | 2 NC | 14@ | For 14" part |
| | 3 NC | 15@ | For 15" part |
| | 4 NC | 14or15@ | For 14" or 15" part |
| | 5 NC | 14or17@ | For 14" or 17" part |
| | 6 NC | AOAC@ | AOAC support part |
| USB2.0 | 1 USB3.0 CONN Left | | |
| | 2 USB2.0 CONN1 Right | Cannonlake@ | For Cannonlake part |
| | 3 USB2.0 CONN2 Right | CD@ | For C cost down |
| | 4 Camera | DUALMIC@ | For Dual MIC part |
| | 5 Cardreader | EMC@ | For EMC part |
| | 6 Touch Panel | EMC_15@ | For EMC 15" part |
| | 7 BT | EMC_NS@ | For EMC nu-stuff part |
| | 8 NC | EMC_PX@ | For EMC PX part |
| | 9 NC | EMC_PXNS@ | For EMC PX nu-stuff part |
| | 10 NC | ES@ | For ES CPU |
| PCIE | 1 NC | EXO@ | For EXO GPU |
| | 2 NC | GCLK@ | For GreenCLK part |
| | 3 NC | ME@ | For ME part |
| | 4 NC | NTS@ | For nu-touch part |
| | 5 LAN | PCH_SDIO@ | For PCH SDIO part |
| | 6 WLAN | | |
| | 7 used as SATA | | |
| | 8 used as SATA | | |
| SATA | X4 PCIE (9-12) DGPU | PX@ | For PX part |
| | 0 HDD | RANKA@ | For VRAM rank A part |
| | 1A ODD | RANKB@ | For VRAM rank B part |
| | 1B used as PCIE | Realtek_SD@ | For Realtek SD part |
| | 2 used as PCIE | SINGLEMIC@ | For single MIC part |
| | | SINGLERANK@ | For single VRAM rank part |
| | | DUALRANK@ | For dual VRAM rank part |
| | | TS@ | For touch screen part |
| | | TPM@ | For TPM part |
| | | UMA@ | For UMA part |

SMBUS Control Table

| | SOURCE | BATT | IT8586E | SODIMM | WLAN WIMAX | Thermal Sensor | PCH | TP Module | charger | DGPU |
|--------------|------------|------|---------|--------|------------|----------------|------------|-----------|---------|-------|
| EC_SMB_CK1 | IT8586E | V | V | X | X | X | X | X | V | X |
| EC_SMB_DA1 | +3VALW | V | +3VALW | X | X | X | X | X | V | X |
| EC_SMB_CK2 | IT8586E | X | V | X | X | V | V | X | X | V |
| EC_SMB_DA2 | +3VS | X | +3VS | X | X | +3VS | +3VALW_PCH | X | X | +3VGS |
| PCH_SMB_CLK | PCH | X | X | V | V | X | V | X | X | X |
| PCH_SMB_DATA | +3VALW_PCH | X | X | +3VS | +3VS | X | +3VALW_PCH | X | X | X |


EC SM Bus1 address

EC SM Bus2 address

PCH SM Bus address

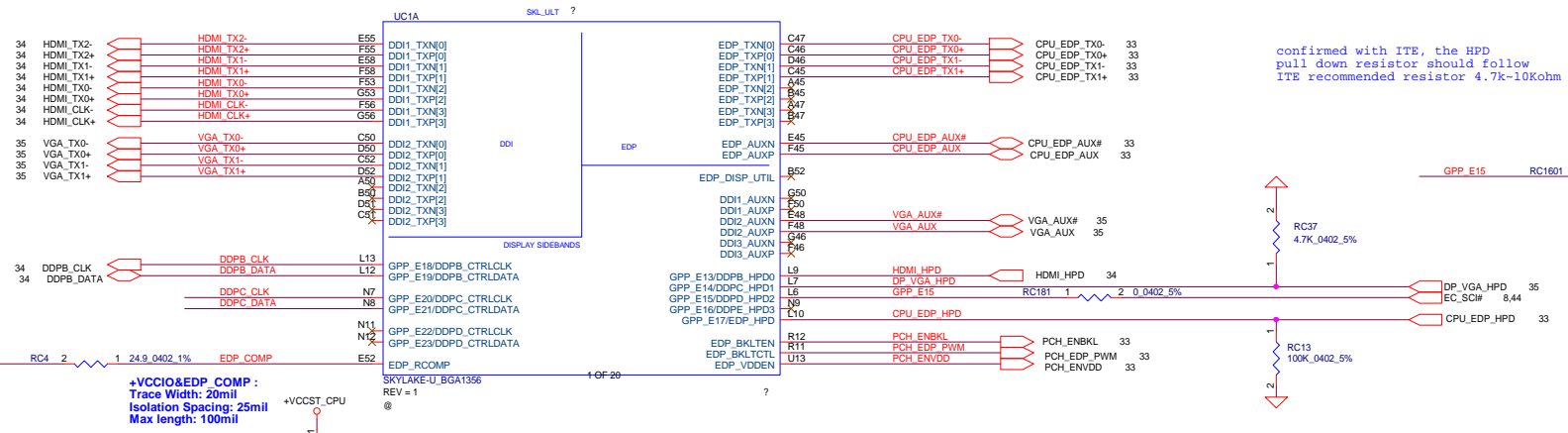
| Device | Address | Device | Address |
|---------------|-------------|-------------------------|----------------|
| Smart Battery | 0X16 | Thermal Sensor NCT7718W | 1001_100xb |
| Charger | 0001 0010 b | PCH | need to update |
| | | DGPU | need to update |

| Device | Address |
|-----------|------------|
| DDR DIMMA | 1010 000Xb |
| DDR DIMMB | 1010 010Xb |
| Wlan | Rsvd |

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|--|------------------------------|-----------------|------------|--|
| Issued Date | 2014/12/11 | Deciphered Date | 2015/12/11 | Notes List |
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HDMI D2
HDMI D1
HDMI D0
HDMI CLK

DP TO VGA Converter

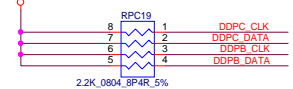


confirmed with ITE, the HPD
pull down resistor should follow
ITE recommended resistor 4.7k-10Kohm

check PROCHOT# circuit with PWR

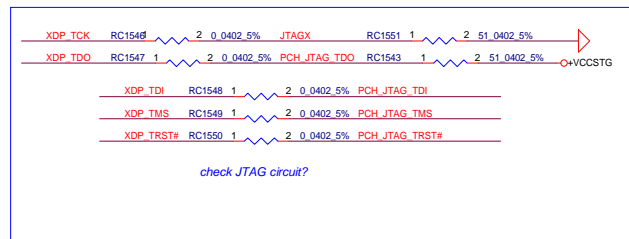
check H_THRMTRIP# if need to connector to EC

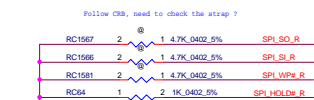
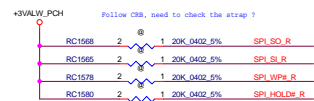
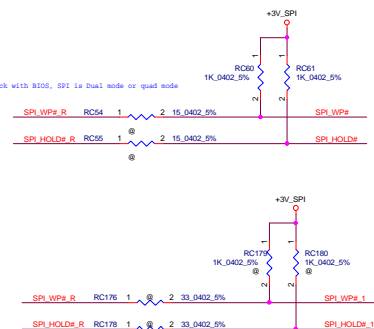
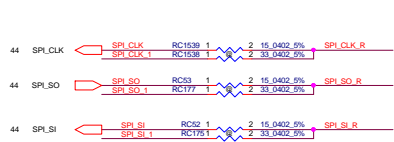
check DDPB_CLK pull high or not?



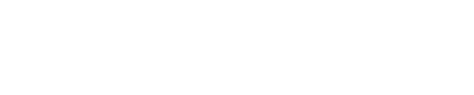
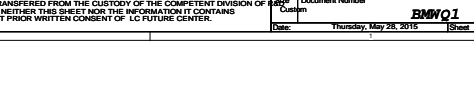
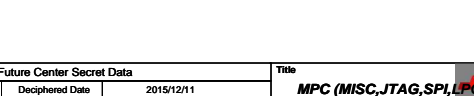
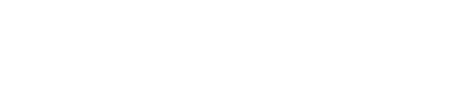
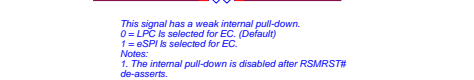
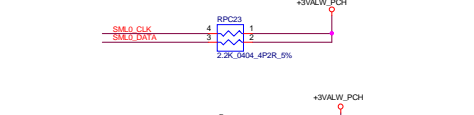
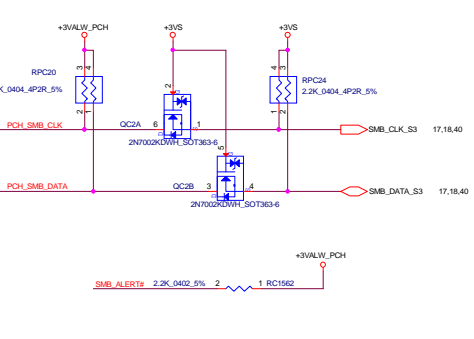
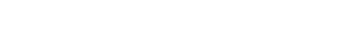
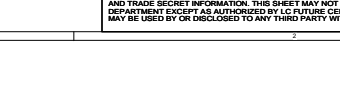
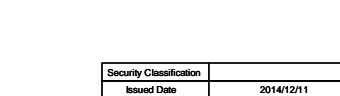
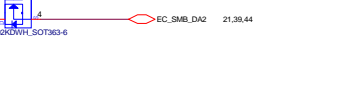
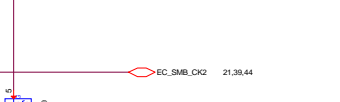
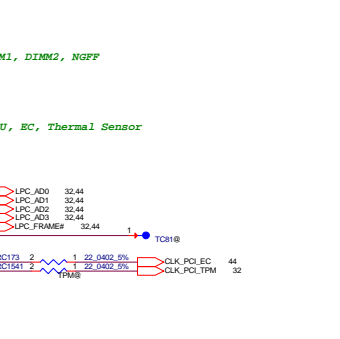
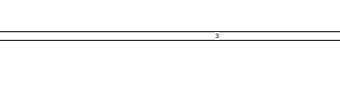
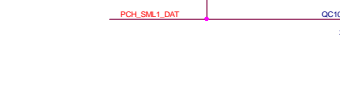
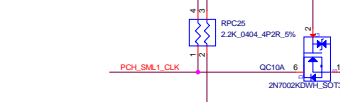
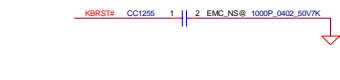
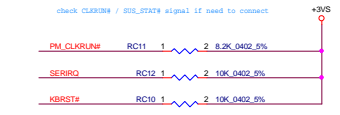
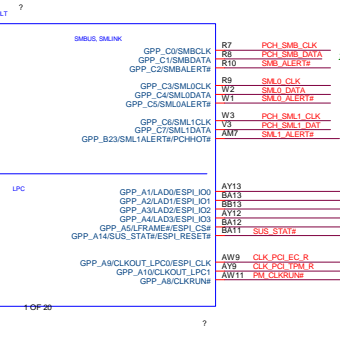
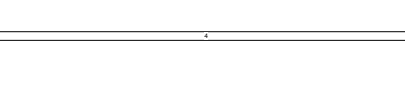
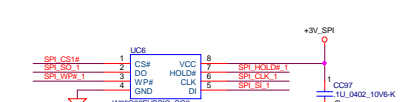
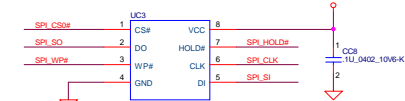
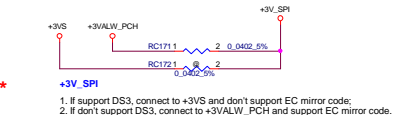
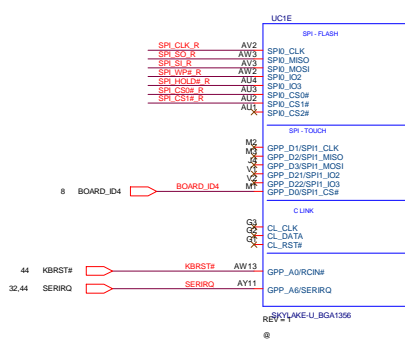
DDP_CTRLDATA strapping sampled on the rising edge of PWROK

| Port | Strap | Enable | Disable |
|--------|---------------|-------------------------------|---------|
| Port 1 | DDPB_CTRLDATA | Pull up to 3.3 V with 2.2Kohm | NC |
| Port 2 | DDPC_CTRLDATA | Pull up to 3.3 V with 2.2Kohm | NC |

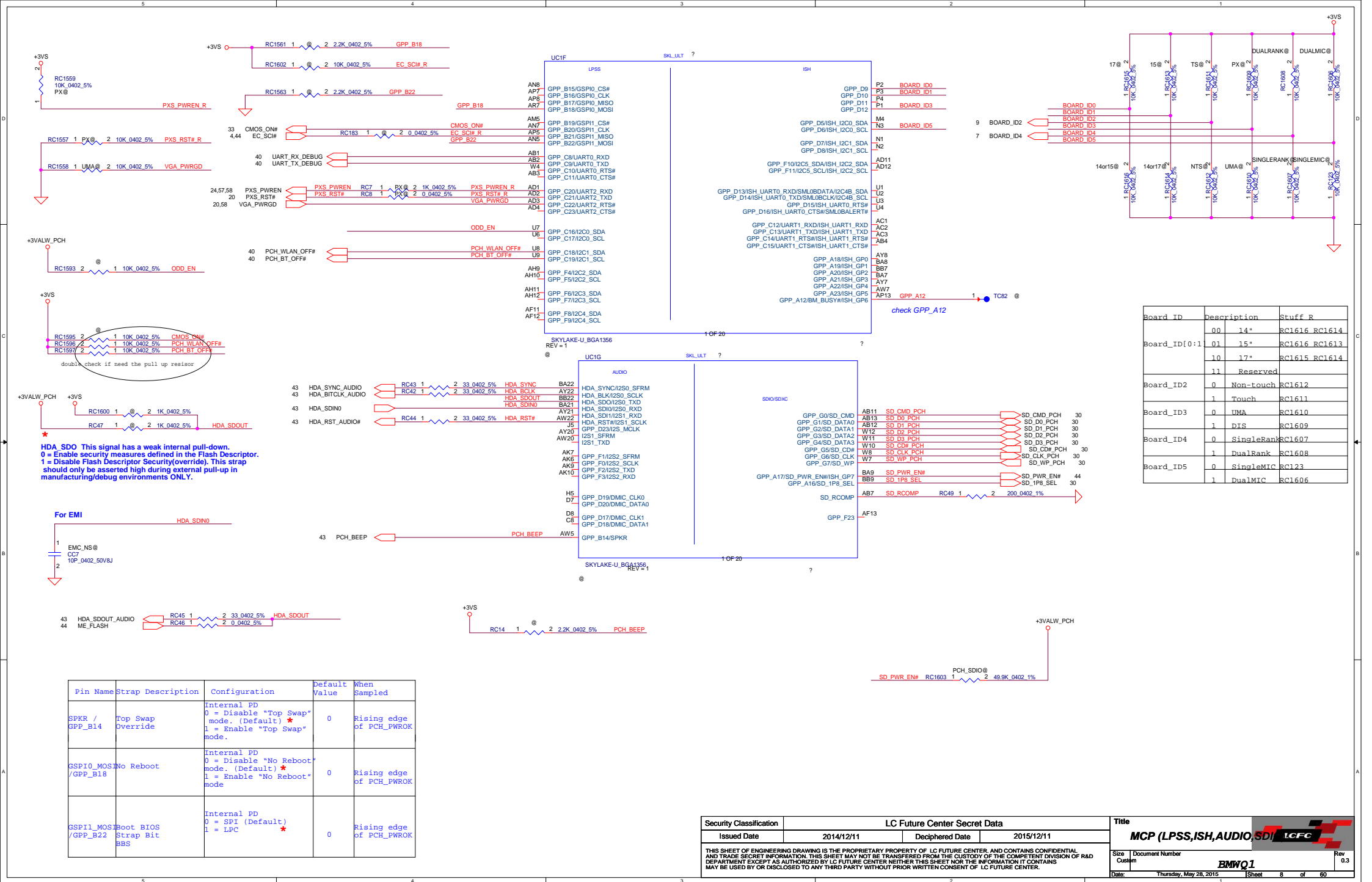




Based on WW36 SKL U&Y WOM, RC64 populated, and RC61 de-populated for SKL U ES sample. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.



| | | | | | |
|--|------------------------|------------------------------|------------|-------------------------|-----|
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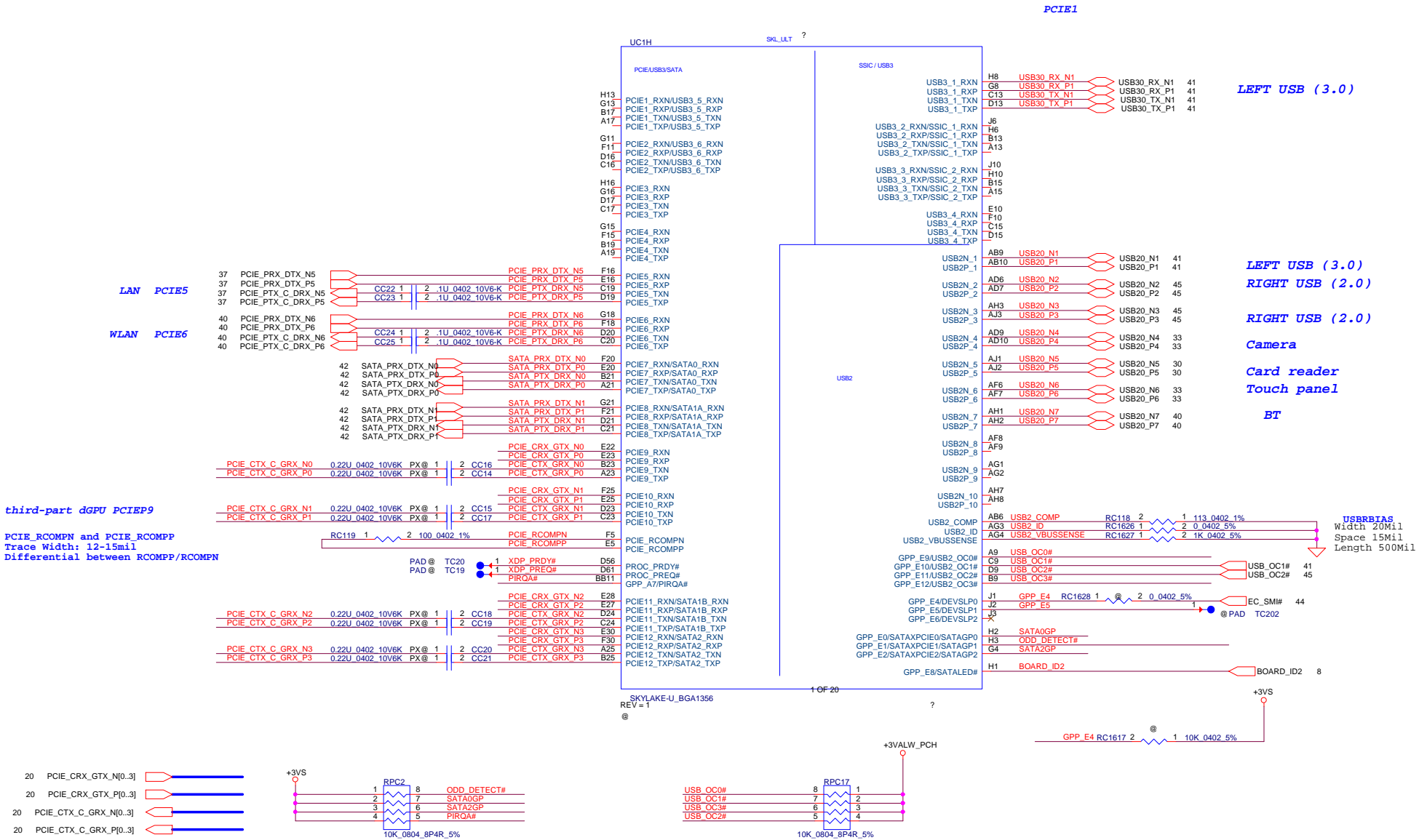


HDA SDO: This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.

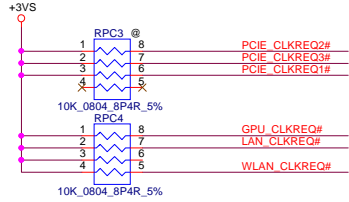
For EMI

| Pin Name | Strap Description | Configuration | Default Value | When Sampled |
|----------------------|-------------------------|---|---------------|--------------------------|
| SPKR / GPP_B14 | Top Swap Override | Internal PD 0 = Disable "Top Swap" mode. (Default) ★ 1 = Enable "Top Swap" mode. | 0 | Rising edge of PCH_PWROK |
| GPIO0_MOSI / GPP_B18 | No Reboot | Internal PD 0 = Disable "No Reboot" mode. (Default) ★ 1 = Enable "No Reboot" mode | 0 | Rising edge of PCH_PWROK |
| GPIO1_MOSI / GPP_B22 | Boot BIOS Strap Bit BBS | Internal PD 0 = SPI (Default) ★ 1 = LPC | 0 | Rising edge of PCH_PWROK |

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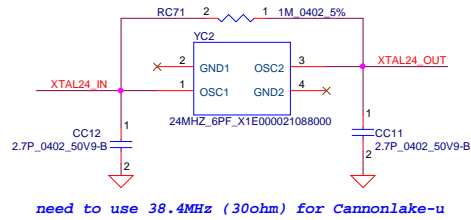
check the Pull up resistor



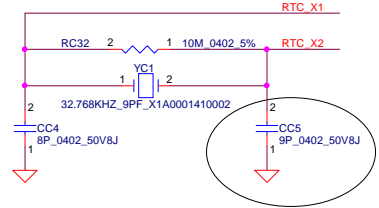
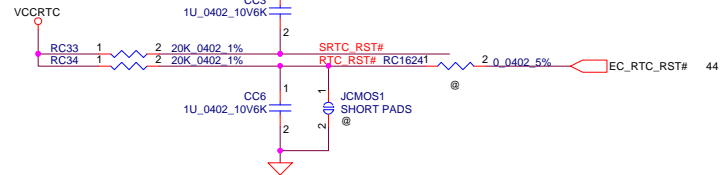
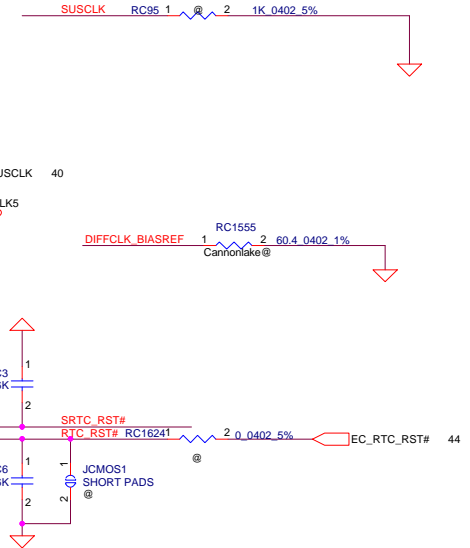
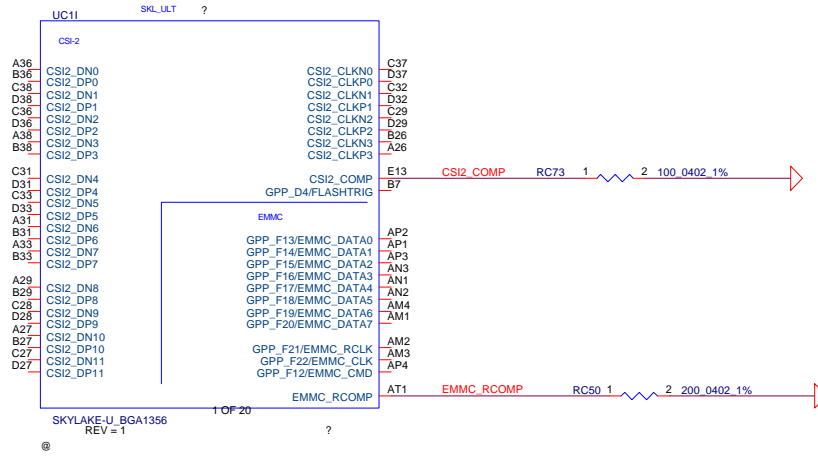
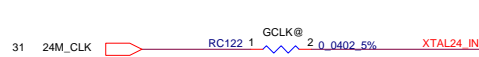
PCIE CLK5 LAN

PCIE CLK6 WLAN

check if need to change to 1M_0402_1% follow PDG, CRB is 1M_0402_5%



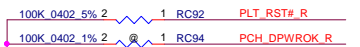
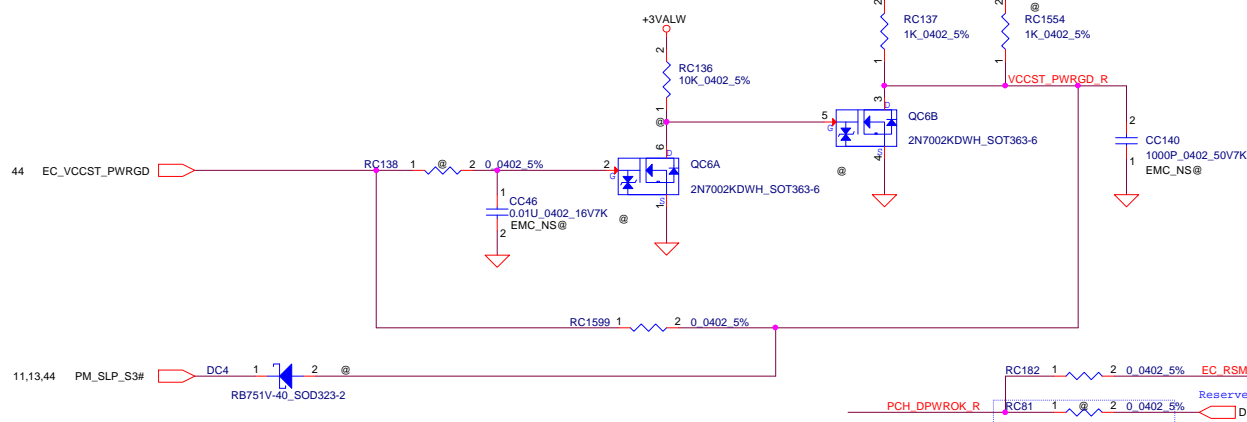
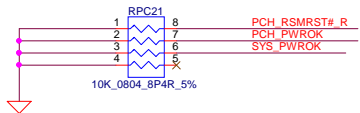
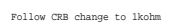
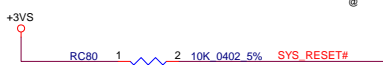
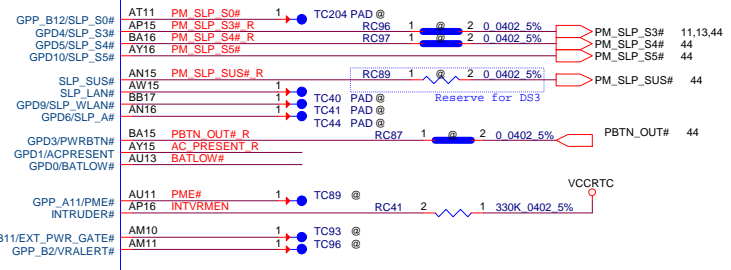
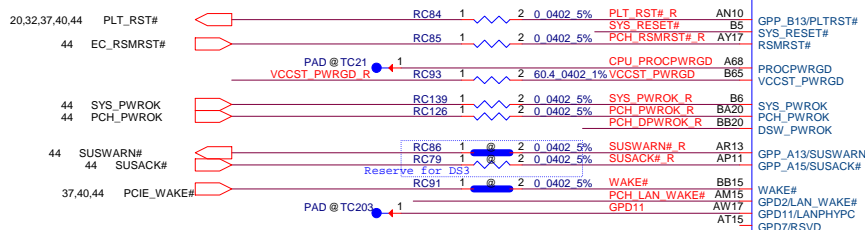
need to use 38.4MHz (30ohm) for Cannonlake-u






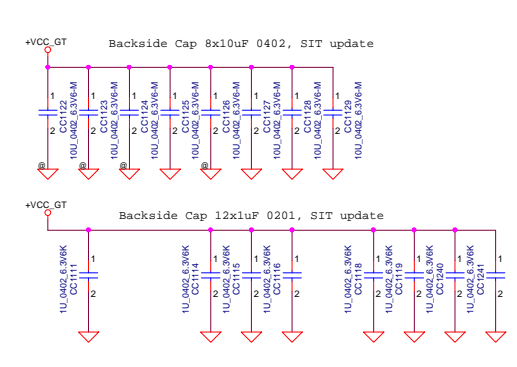
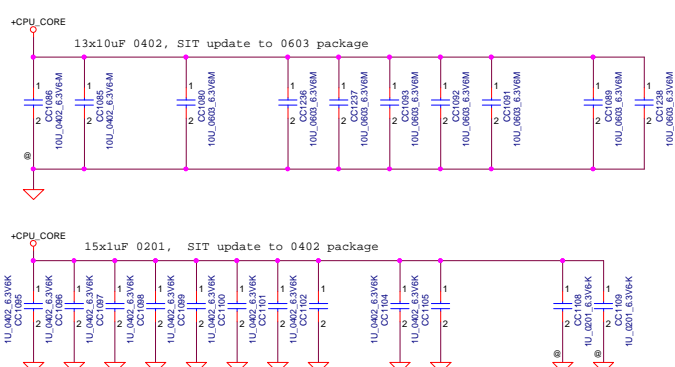
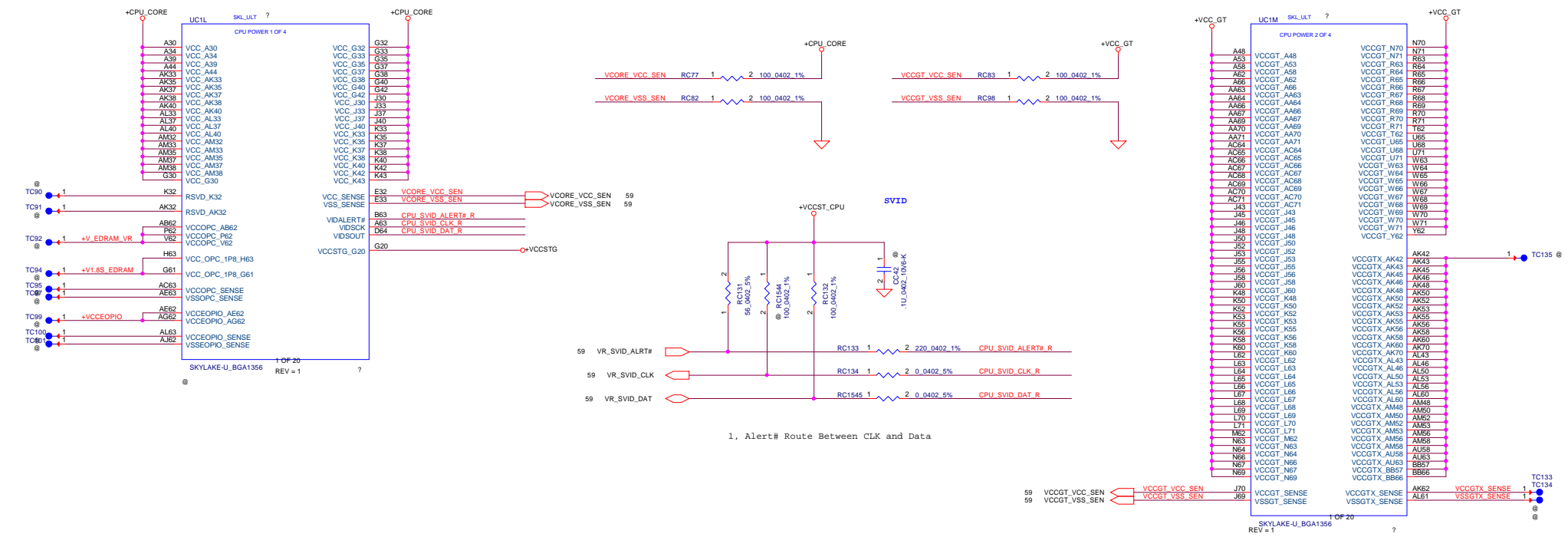
when single end external clock generator used, this pin should be grounded

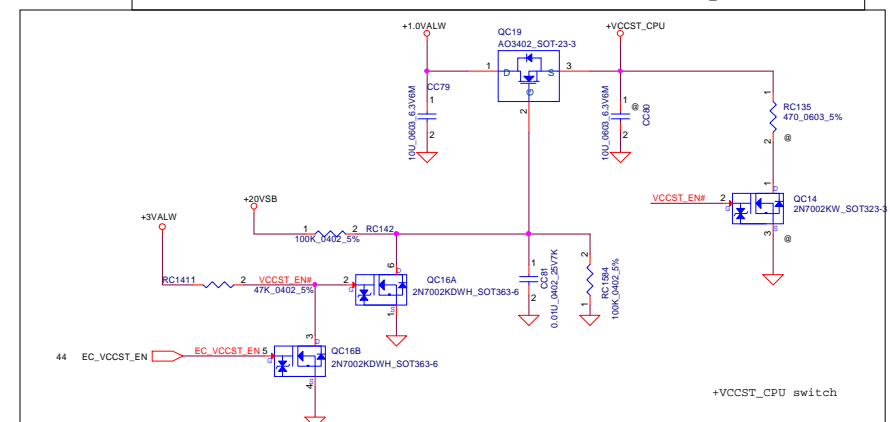
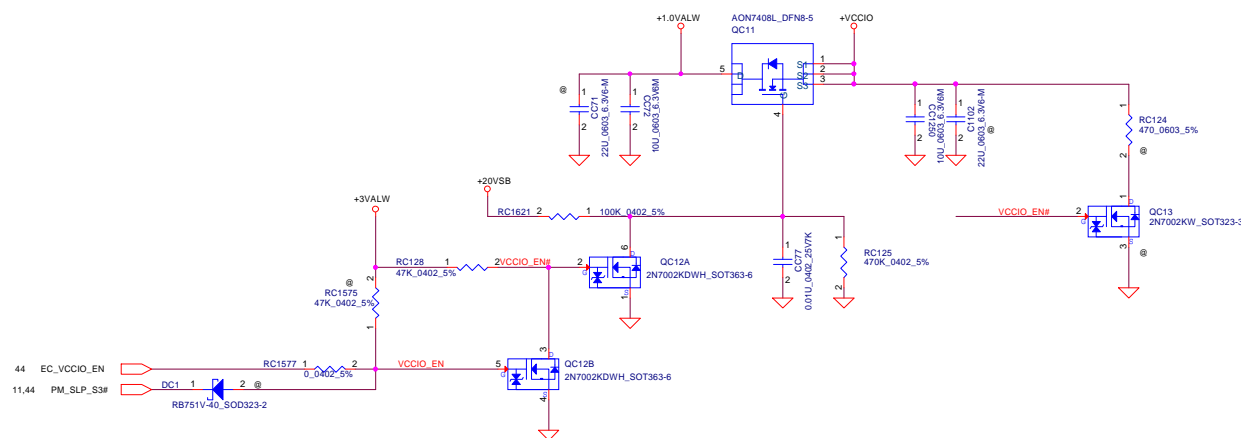
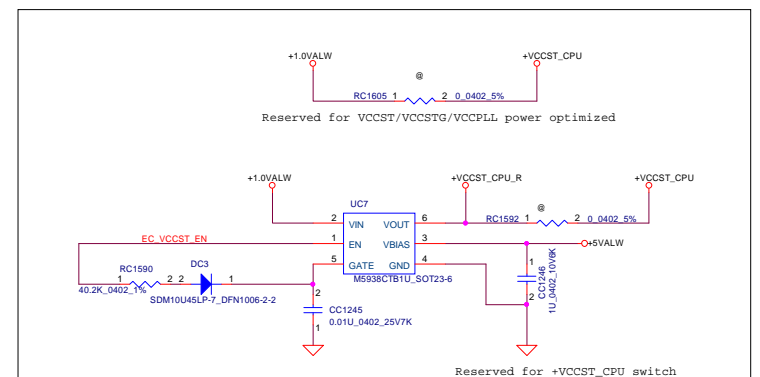
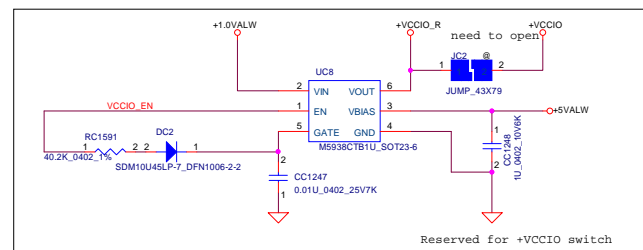
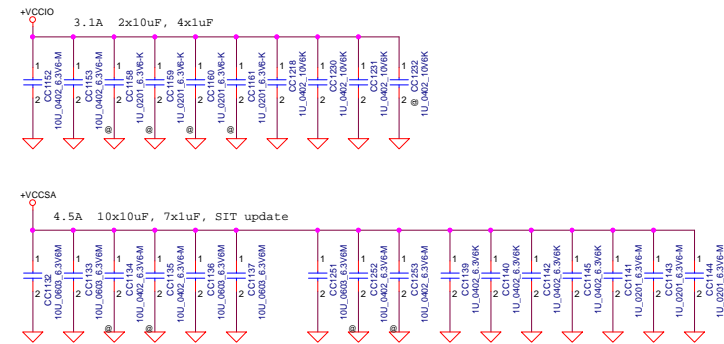
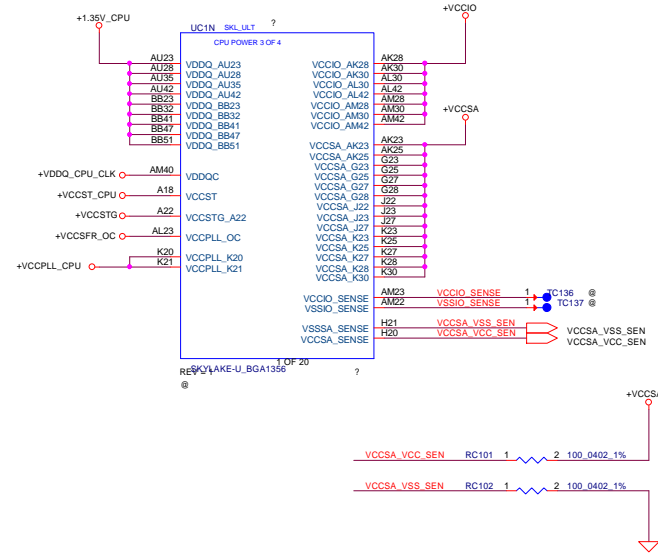
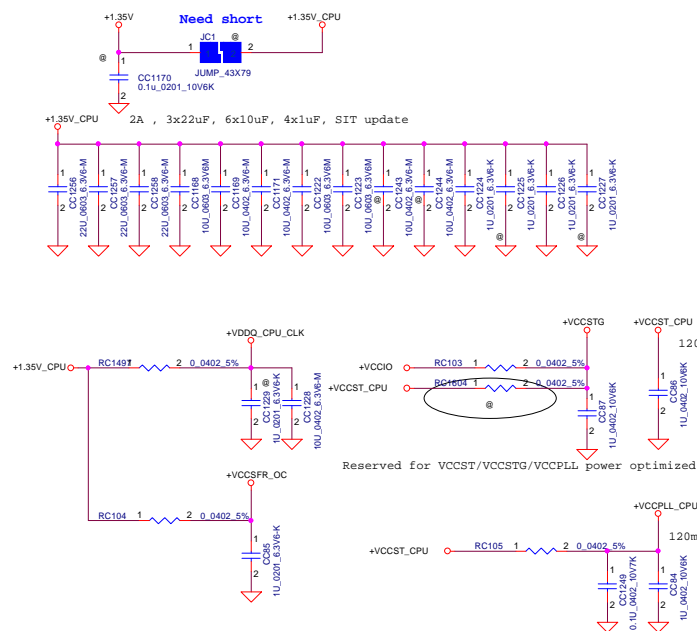



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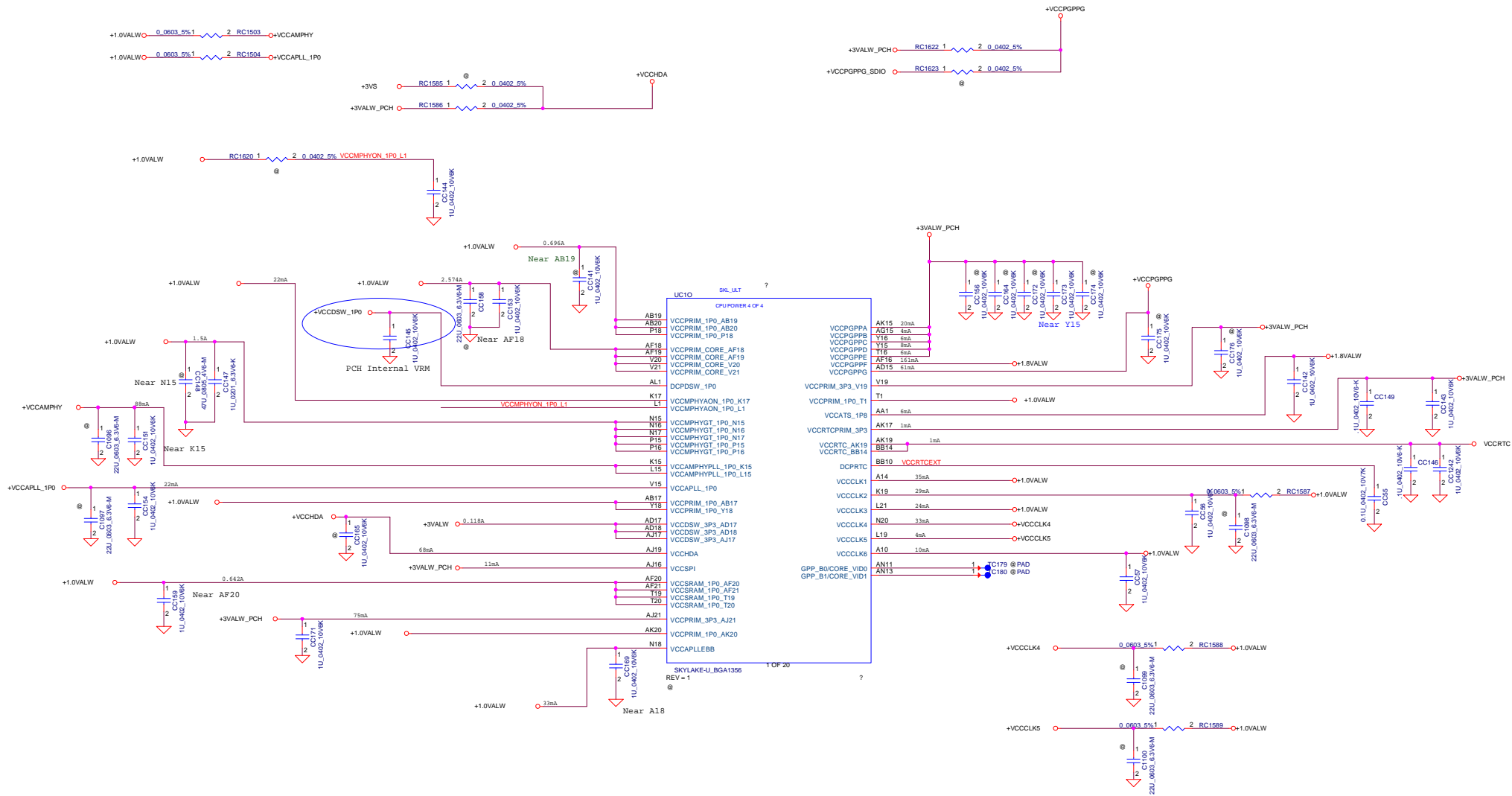


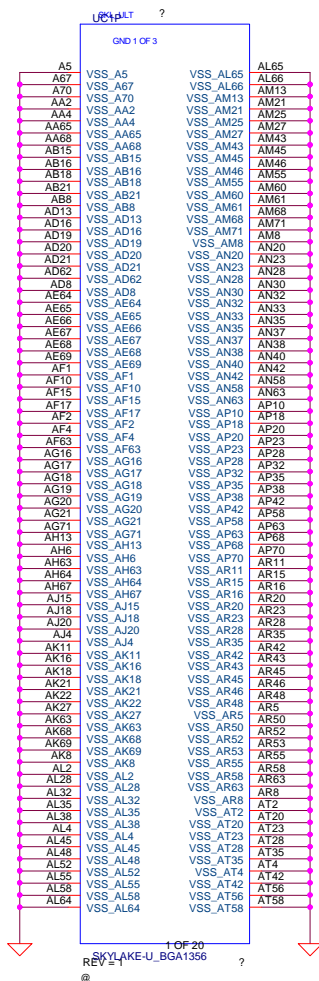
| | | | | | | | |
|--|------------------------|---|------------|-------------------------------|----|---|--|
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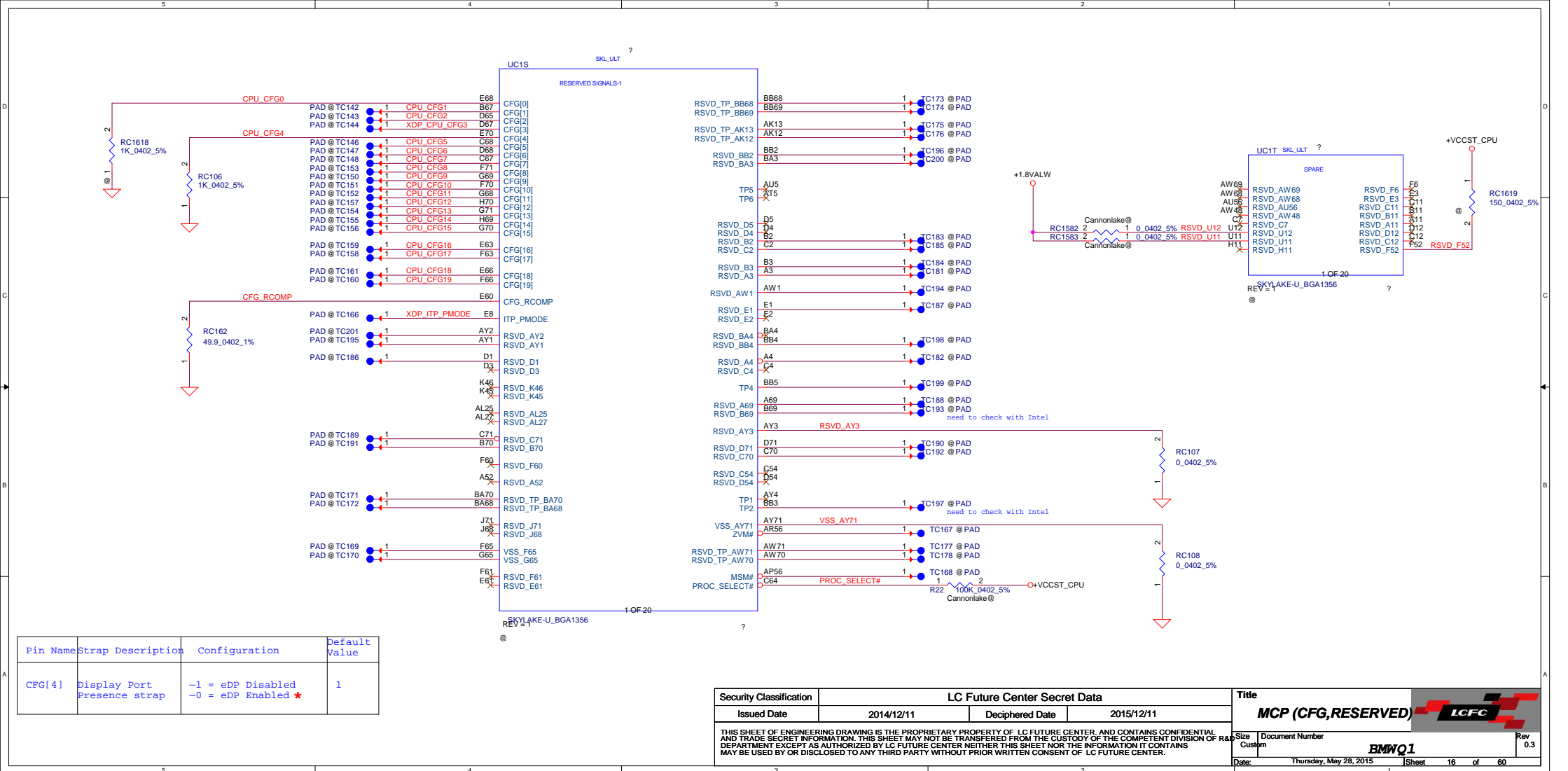


| | | | | | | |
|--|--|------------------------------|-----------------|-----------------|------------|---|
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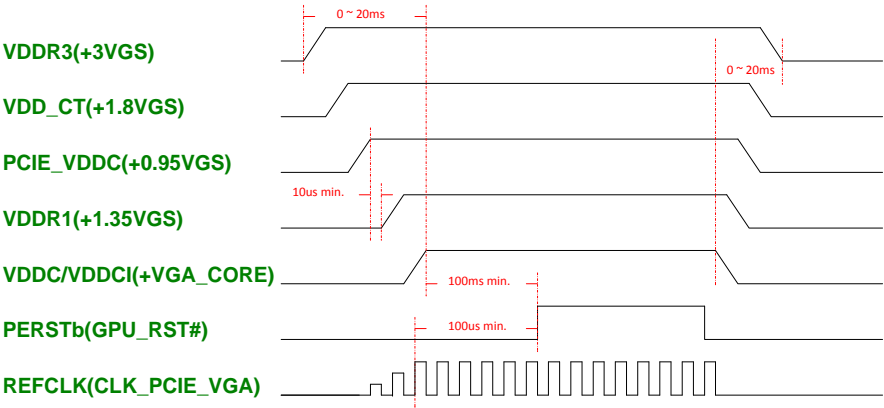


| Pin Number | Pin Name | Net Name | Pin Number | Pin Name | Net Name |
|------------|----------|------------|------------|----------|------------|
| 5 | DQ0 | DDRA_DQ1 | 5 | DQ32 | DDRA_DQ33 |
| 7 | DQ1 | DDRA_DQ5 | 7 | DQ33 | DDRA_DQ36 |
| 15 | DQ2 | DDRA_DQ6 | 15 | DQ34 | DDRA_DQ39 |
| 17 | DQ3 | DDRA_DQ7 | 17 | DQ35 | DDRA_DQ38 |
| 4 | DQ4 | DDRA_DQ0 | 4 | DQ36 | DDRA_DQ37 |
| 6 | DQ5 | DDRA_DQ4 | 6 | DQ37 | DDRA_DQ32 |
| 16 | DQ6 | DDRA_DQ2 | 16 | DQ38 | DDRA_DQ34 |
| 18 | DQ7 | DDRA_DQ3 | 18 | DQ39 | DDRA_DQ35 |
| 10 | DQS#0 | DDRA_DQS#0 | 10 | DQS#4 | DDRA_DQS#4 |
| 12 | DQ80 | DDRA_DQ80 | 12 | DQ84 | DDRA_DQ84 |
| 21 | DQ8 | DDRA_DQ12 | 21 | DQ40 | DDRA_DQ44 |
| 23 | DQ9 | DDRA_DQ9 | 23 | DQ41 | DDRA_DQ41 |
| 33 | DQ10 | DDRA_DQ14 | 33 | DQ42 | DDRA_DQ46 |
| 35 | DQ11 | DDRA_DQ10 | 35 | DQ43 | DDRA_DQ47 |
| 22 | DQ12 | DDRA_DQ13 | 22 | DQ44 | DDRA_DQ45 |
| 24 | DQ13 | DDRA_DQ8 | 24 | DQ45 | DDRA_DQ40 |
| 34 | DQ14 | DDRA_DQ11 | 34 | DQ46 | DDRA_DQ43 |
| 36 | DQ15 | DDRA_DQ15 | 36 | DQ47 | DDRA_DQ42 |
| 27 | DQS#1 | DDRA_DQS#1 | 27 | DQS#5 | DDRA_DQS#5 |
| 29 | DQ81 | DDRA_DQ81 | 29 | DQ85 | DDRA_DQ85 |
| 39 | DQ16 | DDRA_DQ20 | 39 | DQ48 | DDRA_DQ48 |
| 41 | DQ17 | DDRA_DQ21 | 41 | DQ49 | DDRA_DQ53 |
| 51 | DQ18 | DDRA_DQ18 | 51 | DQ50 | DDRA_DQ55 |
| 53 | DQ19 | DDRA_DQ23 | 53 | DQ51 | DDRA_DQ54 |
| 40 | DQ20 | DDRA_DQ17 | 40 | DQ52 | DDRA_DQ52 |
| 42 | DQ21 | DDRA_DQ16 | 42 | DQ53 | DDRA_DQ49 |
| 50 | DQ22 | DDRA_DQ22 | 50 | DQ54 | DDRA_DQ51 |
| 52 | DQ23 | DDRA_DQ19 | 52 | DQ55 | DDRA_DQ50 |
| 45 | DQS#2 | DDRA_DQS#2 | 45 | DQS#6 | DDRA_DQS#6 |
| 47 | DQS2 | DDRA_DQS2 | 47 | DQS6 | DDRA_DQS6 |
| 57 | DQ24 | DDRA_DQ29 | 57 | DQ56 | DDRA_DQ61 |
| 59 | DQ25 | DDRA_DQ25 | 59 | DQ57 | DDRA_DQ60 |
| 67 | DQ26 | DDRA_DQ26 | 67 | DQ58 | DDRA_DQ59 |
| 69 | DQ27 | DDRA_DQ30 | 69 | DQ59 | DDRA_DQ63 |
| 56 | DQ28 | DDRA_DQ24 | 56 | DQ60 | DDRA_DQ56 |
| 58 | DQ29 | DDRA_DQ28 | 58 | DQ61 | DDRA_DQ57 |
| 68 | DQ30 | DDRA_DQ31 | 68 | DQ62 | DDRA_DQ62 |
| 70 | DQ31 | DDRA_DQ27 | 70 | DQ63 | DDRA_DQ58 |
| 62 | DQS#3 | DDRA_DQS#3 | 62 | DQS#7 | DDRA_DQS#7 |
| 64 | DQ83 | DDRA_DQ83 | 64 | DQ87 | DDRA_DQ87 |

Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs. It is recommended that the 3.3-V rail ramp up first. The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μs before VDDC, VDDCI, and VMEMIO start to ramp up. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μs). For power down, reversing the ramp-up sequence is recommended.



CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

| MLPS Bit | Strap Name | Description | RECOMMENDED SETTINGS |
|-------------------------------|--|--|----------------------|
| PS_0[1] PS_0[2] PS_0[3] | ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2] | Define the ROM type when STRAP BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP BIOS_ROM_EN = 0. 100 = 256MB | X |
| PS_0[4] | N/A | Reserved for internal use only. Must be 1 at reset. | 1 |
| PS_0[5] | AUD_PORT_CONN_PINSTRAP[0] | The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs. | 1 |
| PS_1[1] | STRAP_BIF_GEN3_EN_A | 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 1= support | X |
| PS_1[2] | STRAP_BIF_CLK_PM_EN | 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled | 0 |
| PS_1[3] | N/A | Reserved for internal use only. Must be 0 at reset. | 0 |
| PS_1[4] | STRAP_TX_CFG_DRV_FULL_SWING | 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled | 1 |
| PS_1[5] | STRAP_TX_DEEMPH_EN | 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable | X |
| PS_2[1] | N/A | Reserved. | 0 |
| PS_2[2] | N/A | Reserved. | 0 |
| PS_2[3] | STRAP_BIOS_ROM_EN | 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable | X |
| PS_2[4] | STRAP_BIF_VGA_DIS | 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller. | 1 |
| PS_2[5] | N/A | Reserved | 1 |
| PS_3[1] PS_3[2] PS_3[3] | BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2] | Board configuration related strapping, such as for memory ID 000 = Hynix 256M*16 001 = Hynix 128M*16 100 = Samsung 256M*16 011 = Samsung 128M*16 010 = Micron 256M*16 111 = Micron 128M*16 | X |
| PS_3[4] PS_3[5] | AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2] | Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable. 111= No usable endpoints. | 11 |

VRAM ID config

| Memory Type | | VRAM ID PS_3[3:1] | PU resistor RV33 | PD resistor RV36 |
|-------------|---|----------------------|---------------------|---------------------|
| 128Mx16 | Hynix H5TC2G63FFR-11C | 100 | 4.53K | 4.99K |
| | Micron MT41J128M16JT-093G | 111 | 4.75K | NC |
| | Samsung K4W2G1646Q-BC1A | 110 | 3.4K | 10K |
| | | | | |
| 256Mx16 | Hynix H5TC4G63CFR-N0C (New) | 000 | NC | 4.75K |
| | Micron MT41J256M16HA-093G | 010 | 4.53K | 2K |
| | Samsung K4W4G1646E-BC1A (New no AVL) | 001 | 8.45K | 2K |
| | | | | |

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Title

VGA Notes List

Size

Document Number

Rev

0.3

Date:

Thursday, May 28, 2015

Sheet

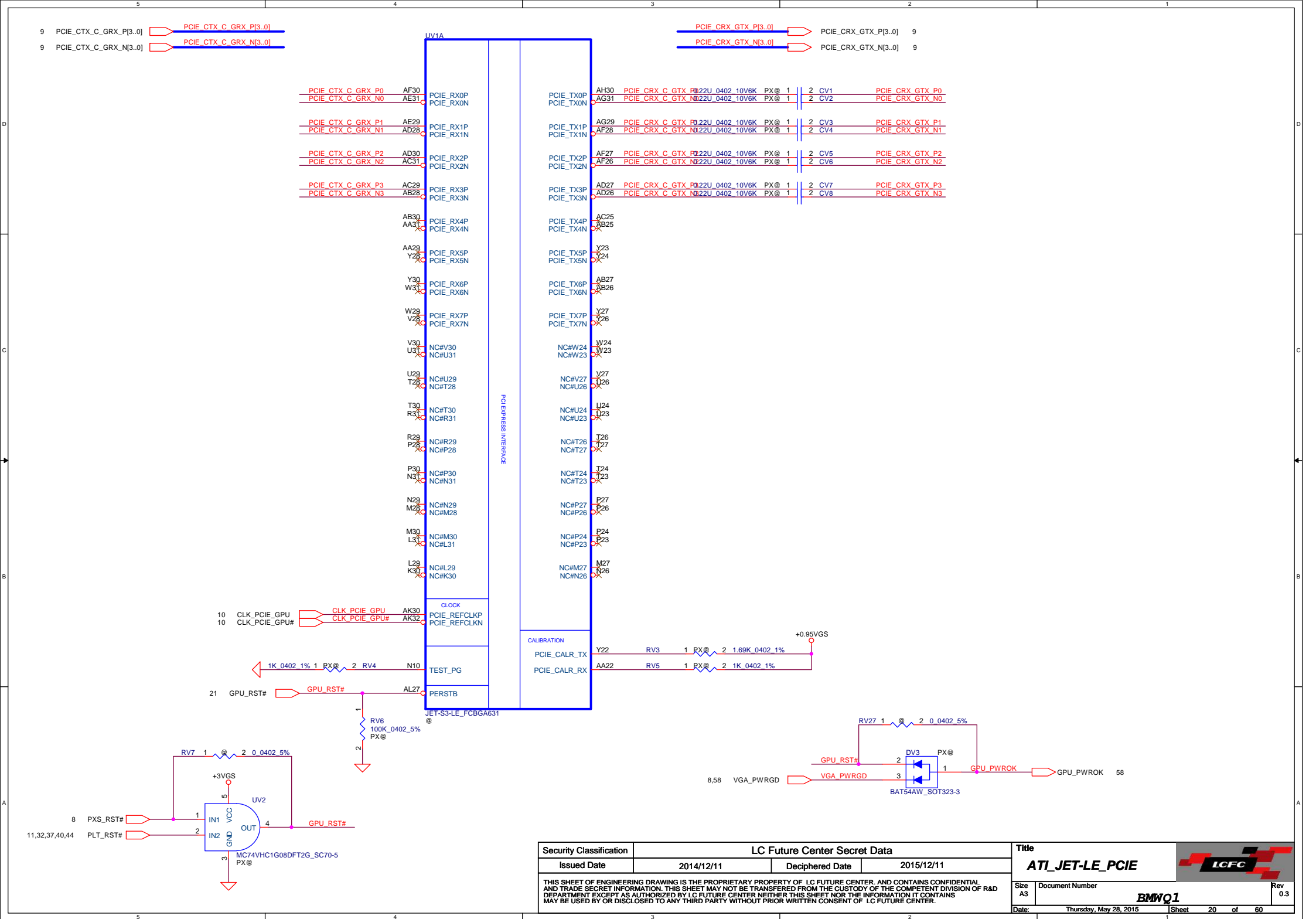
19

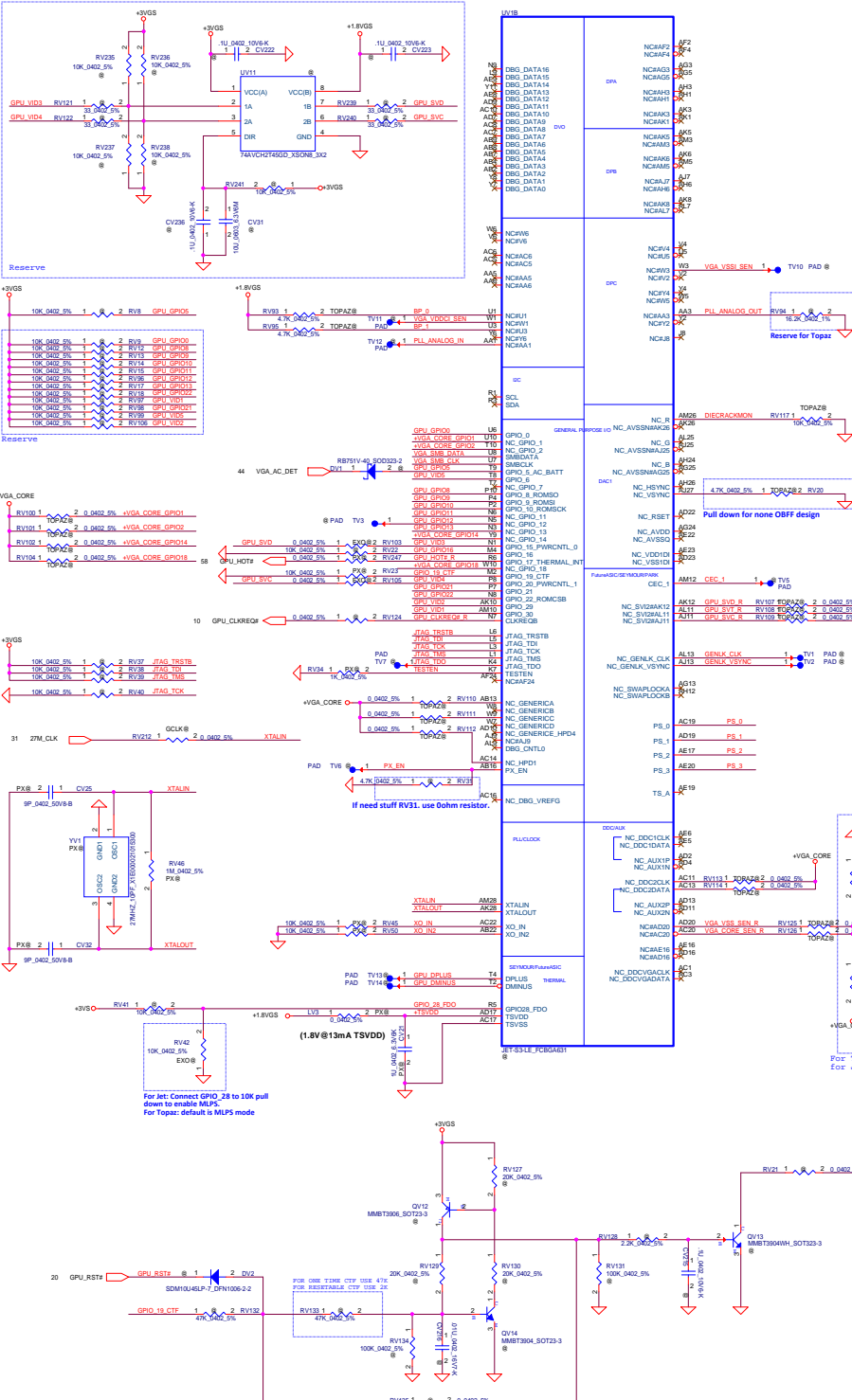
of

60

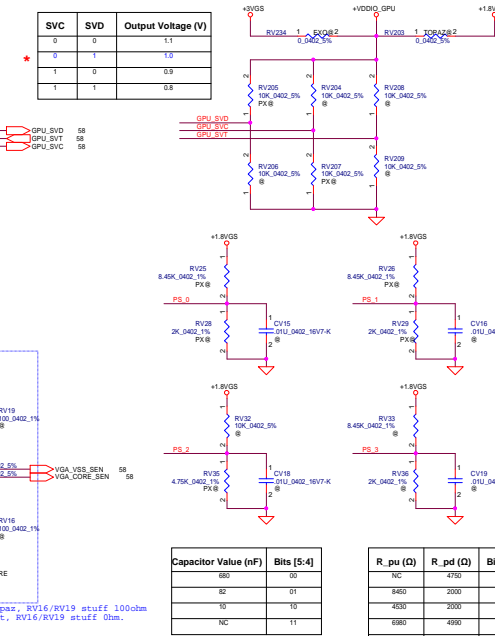
LCFC

BMWQ1





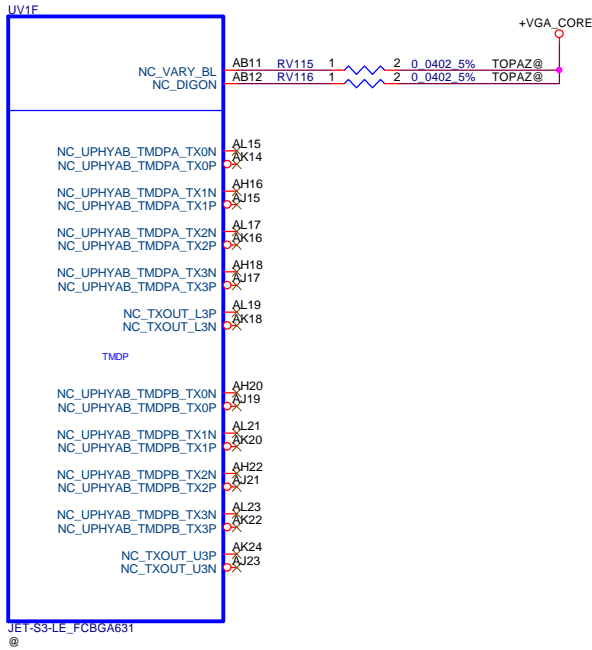
| CONFIGURATION STRAPS | | | RECOMMENDED SETTINGS | |
|---|-----------------------------------|--|---|--|
| ALLOW FOR PULL UP PADS FOR THESE STRAPS AND IF THESE STRAPS ARE USED, THEY MUST NOT CONFLICT DURING RESET | | | DO NOT INSTALL RESISTOR = INSTALL USE RESISTOR X = DESIGN DEPENDANT N/A = NOT APPLICABLE | |
| MLPS Bit | Strap Name | Description | RECOMMENDED SETTINGS | |
| PS_0[1] | ROM_CONFIG[0] | Defines the ROM type when STRAP_BIOS_ROM_EN = 1 | X | |
| PS_0[2] | ROM_CONFIG[1] | Defines the primary memory aperture size when STRAP_BIOS_ROM_EN = 0 | 100 = 256MB | |
| PS_0[3] | ROM_CONFIG[2] | | 1 | |
| PS_0[4] | N/A | Reserved for internal use only. Must be 0 at reset. | 1 | |
| PS_0[5] | AUD_PORT_CONL_PINSTRAP[0] | The LSB (least significant bit) of the strap option that indicates the number of auto-capable display outputs. | 1 | |
| PS_0[11] | STRAP_BIF_GENL_EN_A | 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. | 1 = GEN3 is supported | |
| PS_0[12] | STRAP_BIF_CLK_PML_EN | 0 = The CLKREQ power management capability is disabled. 1 = The CLKREQ power management capability is enabled. | 0 | |
| PS_0[13] | N/A | Reserved for internal use only. Must be 0 at reset. | 0 | |
| PS_0[14] | STRAP_TX_CPD_DRV... FULL_SWING | 0 = The transmitter full swing is disabled. 1 = The transmitter full swing is enabled. | 1 | |
| PS_0[15] | STRAP_TX_DEEMPH_EN | 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. | 1 = Enable | |
| PS_0[21] | N/A | Reserved. | 0 | |
| PS_0[22] | STRAP_BIOS_ROM_EN | 1 = Enable the external BIOS ROM device. 0 = Disable | X | |
| PS_0[24] | STRAP_BIF_VGA_DIS | 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller. | 1 | |
| PS_0[25] | N/A | Reserved. | 1 | |
| PS_0[31] | BOARD_CONFIG[0] | Board configuration related strap, such as for memory ID | X | |
| PS_0[32] | BOARD_CONFIG[1] | 00 = Hynix 56M16 01 = Hynix 128M16 02 = Samsung 25M16 03 = Samsung 128M16 04 = Micron 25M16 05 = Micron 128M16 | 11 = No usable endpoints. | |
| PS_0[33] | BOARD_CONFIG[2] | Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. (Combine with PS_0[35]) | 11 = No usable endpoints. | |
| PS_0[34] | AUD_PORT_CONL_PINSTRAP[1] | 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable. | 11 | |
| PS_0[35] | AUD_PORT_CONL_PINSTRAP[2] | | | |



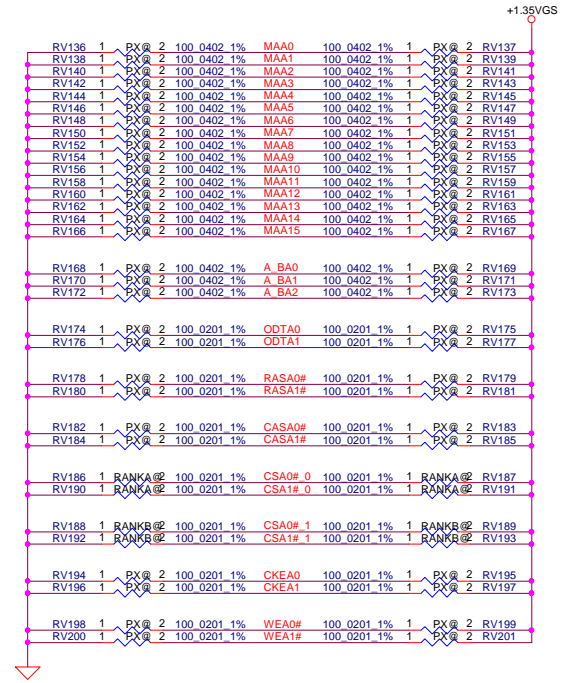
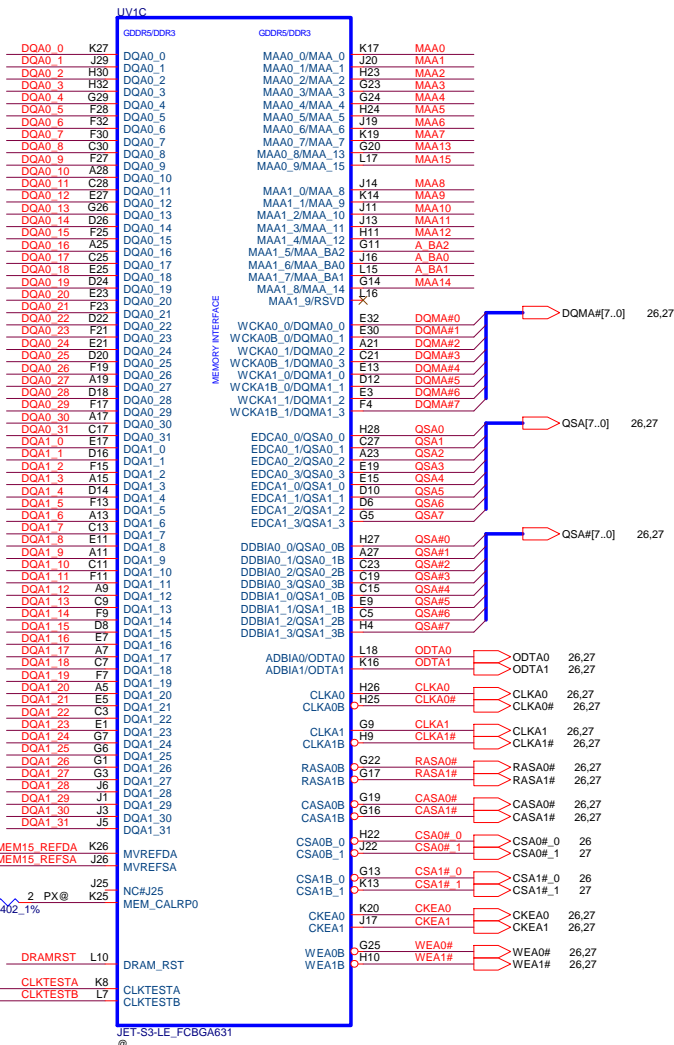
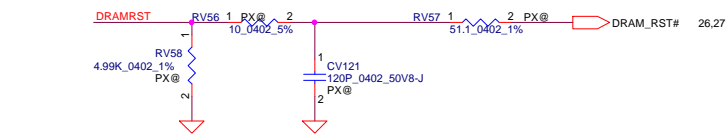
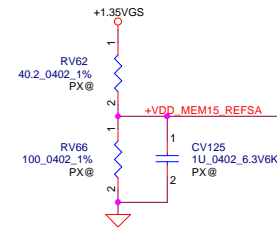
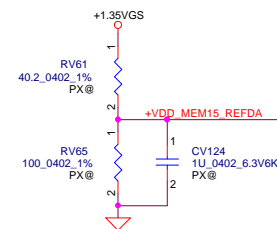
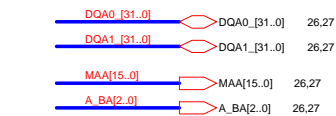
| Capacitor Value (nF) | | Bits [5:4] | |
|----------------------|----|------------|-------|
| 680 | 00 | NC | 4750 |
| 82 | 01 | 8450 | 2000 |
| 10 | 10 | 4500 | 2000 |
| NC | 11 | 6800 | 4900 |
| | | 4500 | 4900 |
| | | 3240 | 5620 |
| | | 3400 | 10000 |
| | | 4750 | NC |

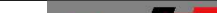
| R_pu (Ω) | R_pd (Ω) | Bits [3:1] |
|----------|----------|------------|
| NC | 4750 | 000 |
| 8450 | 2000 | 001 |
| 4500 | 2000 | 010 |
| 6800 | 4900 | 011 |
| 4500 | 4900 | 100 |
| 3240 | 5620 | 101 |
| 3400 | 10000 | 110 |
| 4750 | NC | 111 |

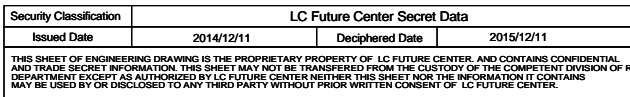
Note: 0402 1% resistors are required.

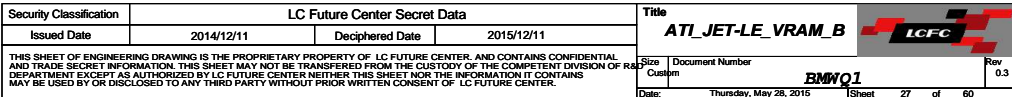



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|---|------------------------------|-----------------|------------|--|---------------------------------|---------------------------------|
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| | | | | | Sheet 22 | of 60 |




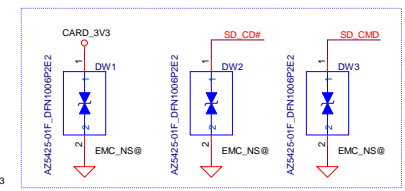
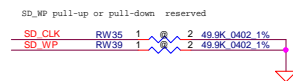
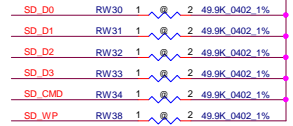
| | | | | | | | |
|--|------------|------------------------------|------------|---|------------------------|-----------------|----------|
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| | | | | Size | | Document Number | Rev |
| | | | | Custom | BMWQ1 | 0.3 | |
| | | | | Date: | Thursday, May 28, 2015 | Sheet | 25 of 60 |




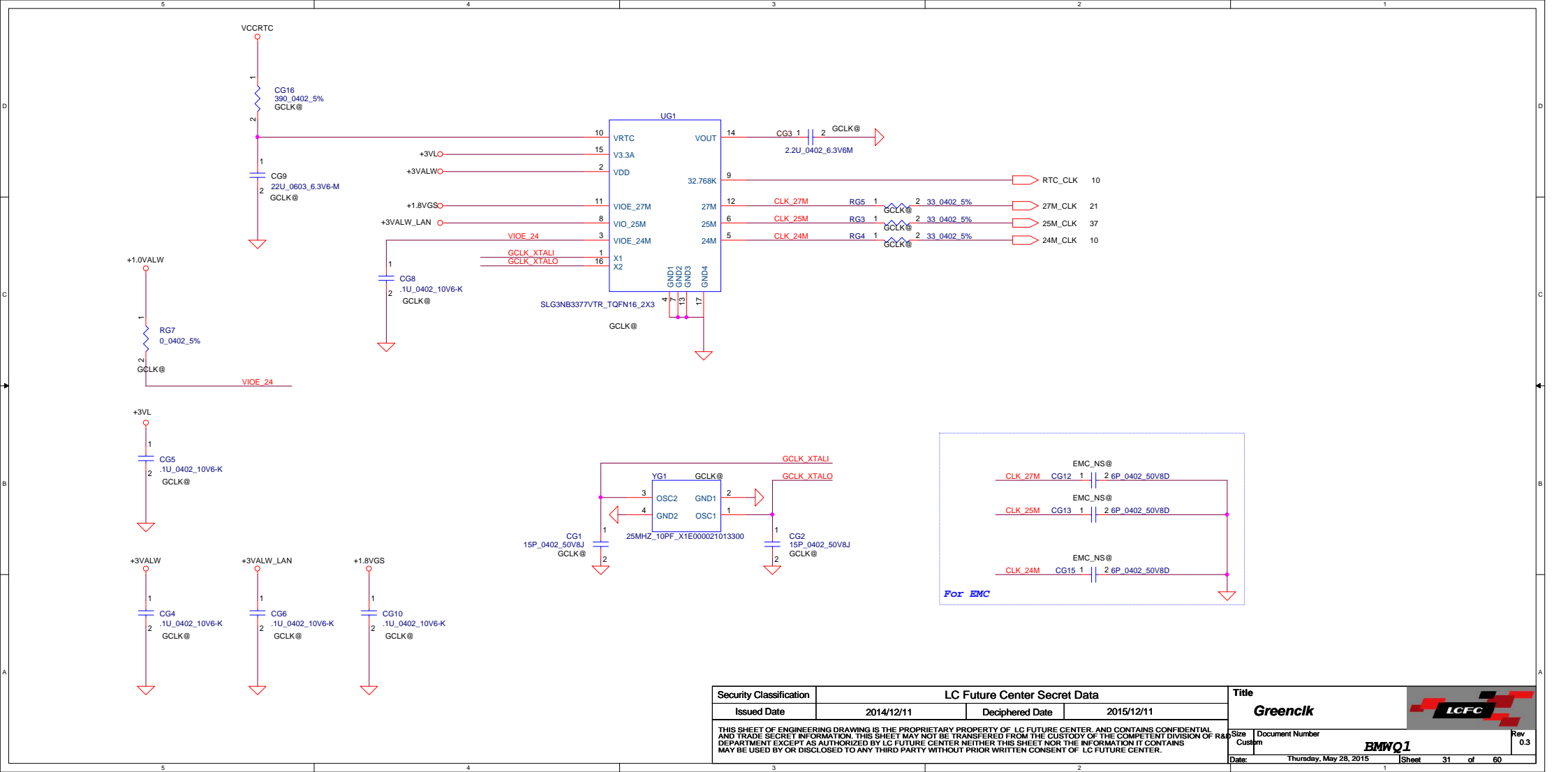


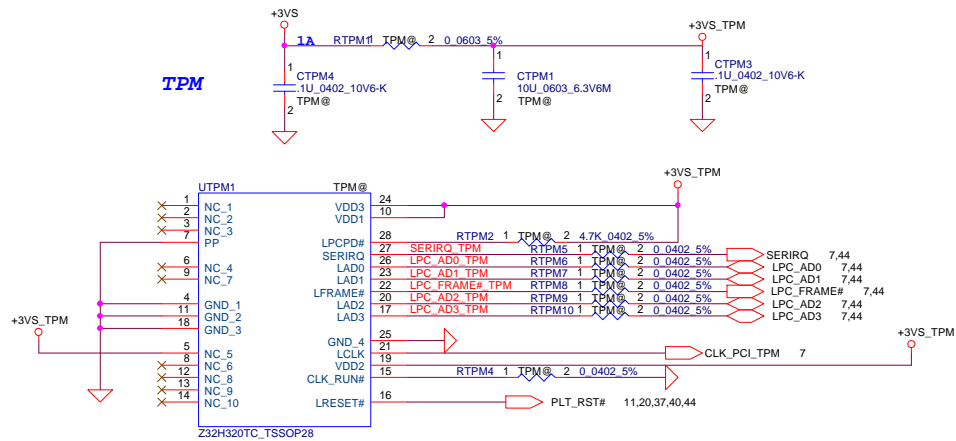
| | | | | | | | | | |
|--|--|------------------------------|--|-----------------|--|------------|--|---|--|
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| | | | | | Custom | | 0.3 |
| | | | | | Date: | Thursday, May 28, 2015 | Sheet 29 of 60 |



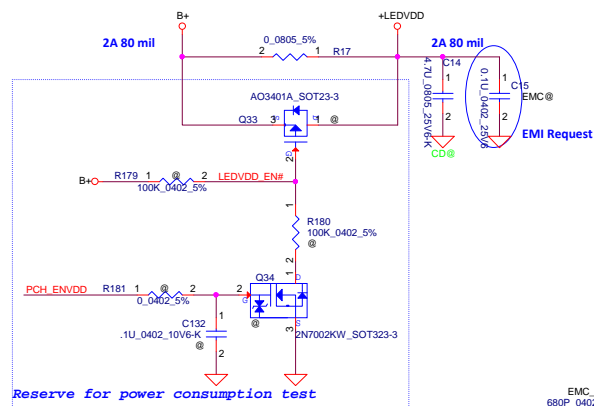
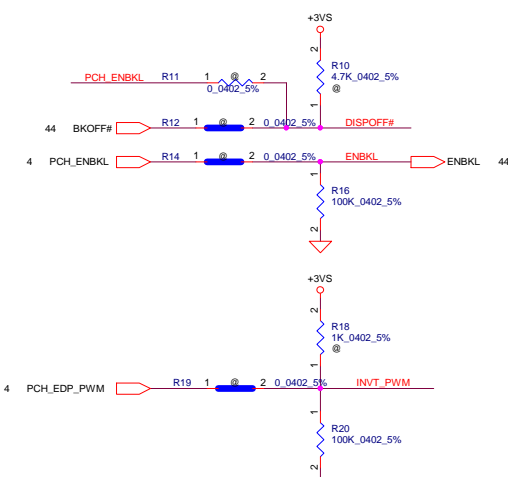
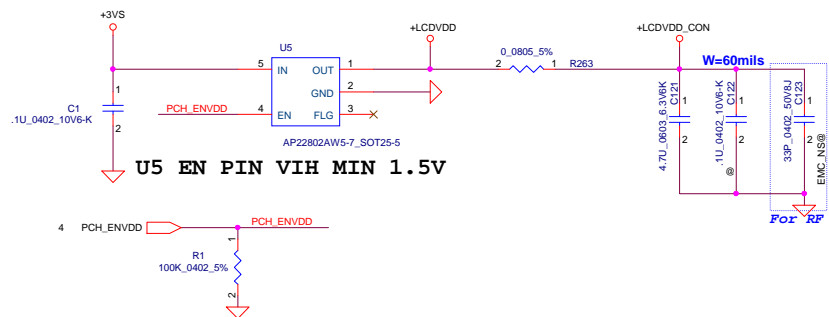
| | | | | | | | |
|---|--|------------------------------|--|------------|------------------------|---|----------|
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| Issued Date | | Deciphered Date | | Cardreader | | | |
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| | | | | Custum | | 0.3 | |
| | | | | Date: | Thursday, May 28, 2015 | Sheet | 30 of 60 |



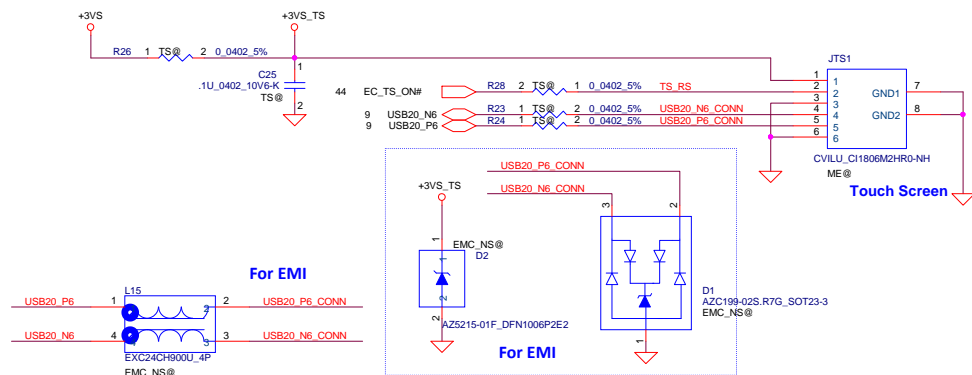


| | | | | | | | | |
|--|--|------------------------------|--|-----------------|--|--|------------|--|
| Security Classification | | LC Future Center Secret Data | | Title | |  | | |
| Issued Date | | 2014/12/11 | | Deciphered Date | | | 2015/12/11 | |
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| Size | | Document Number | | Rev | | | 0.3 | |
| Custom | | BMWQ1 | | | | | | |
| Date: | | Thursday, May 28, 2015 | | Sheet | | 32 of 60 | | |
| 3 | | 1 | | 2 | | 1 | | |

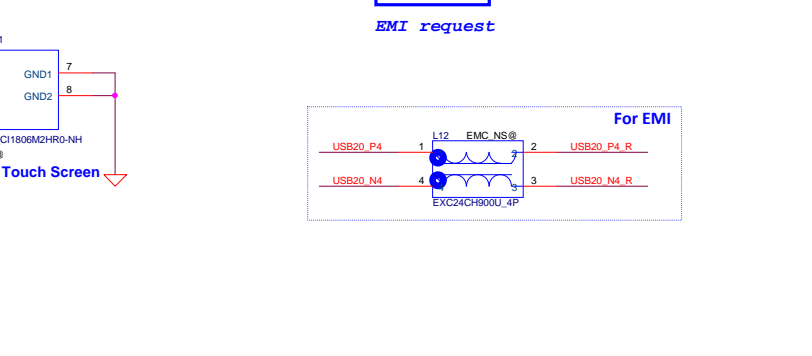
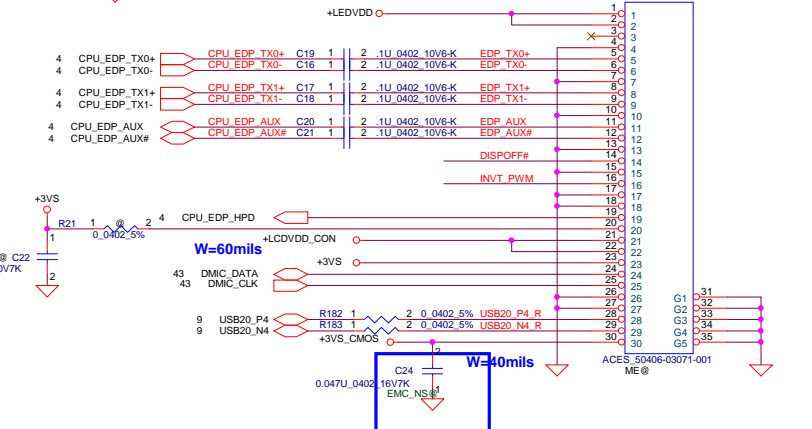
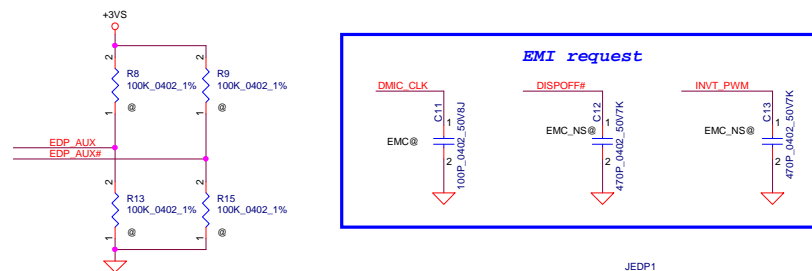
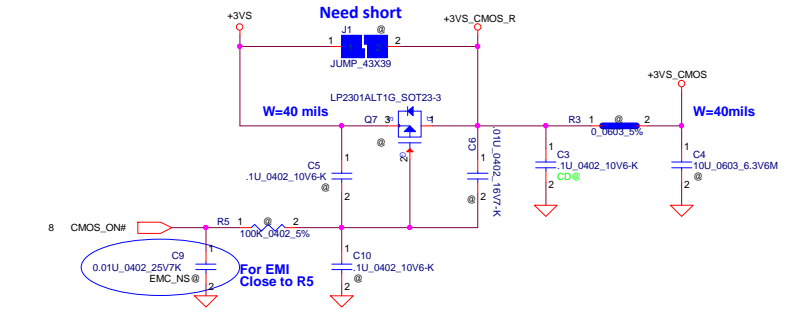
LCD POWER CIRCUIT

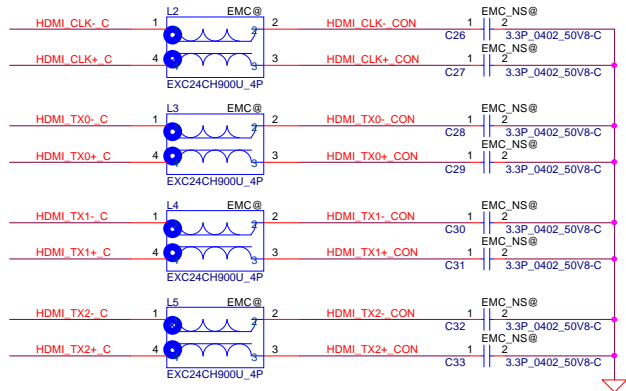


Touch Screen

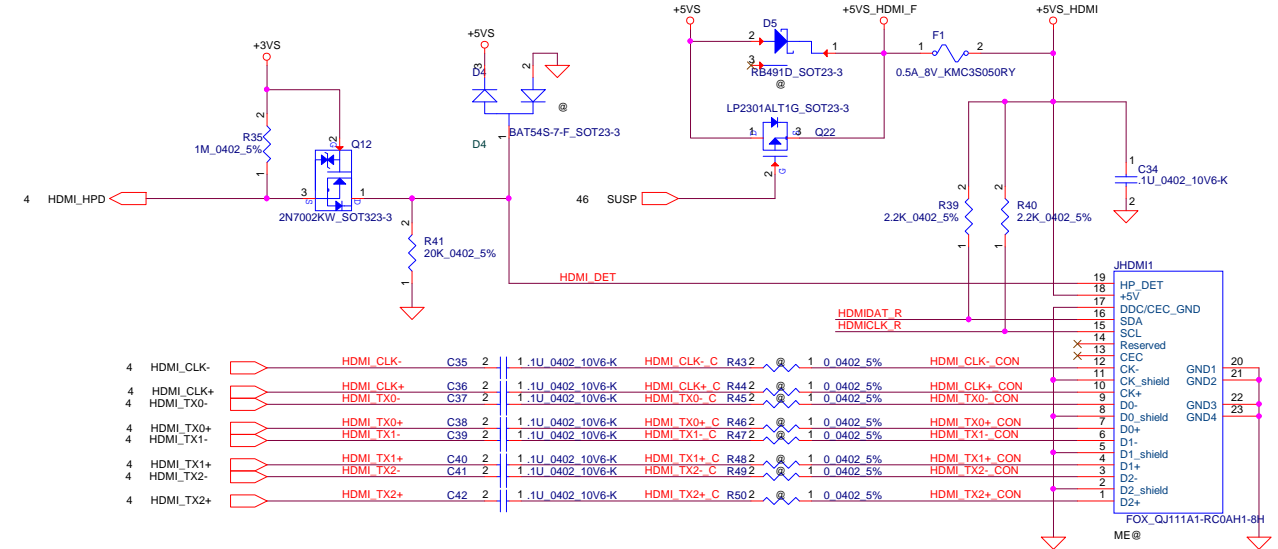
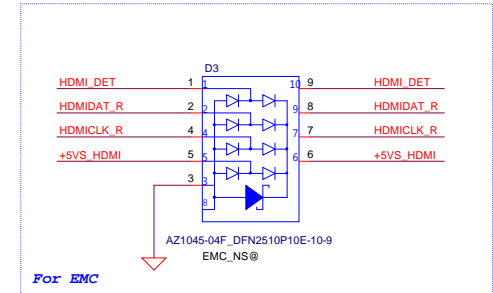
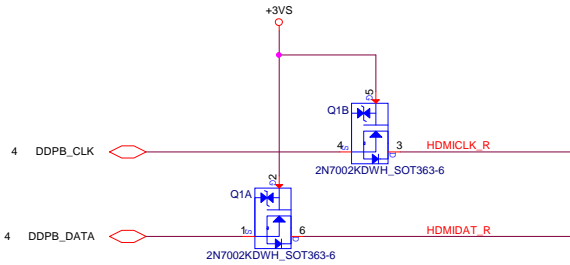
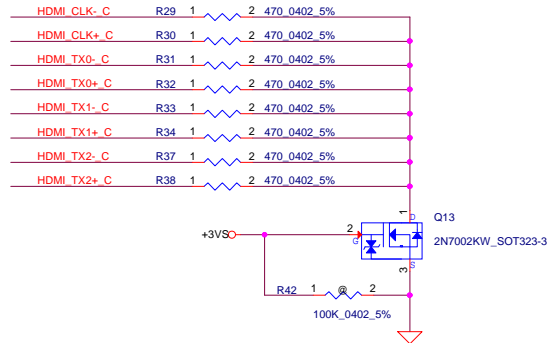


CMOS Camera

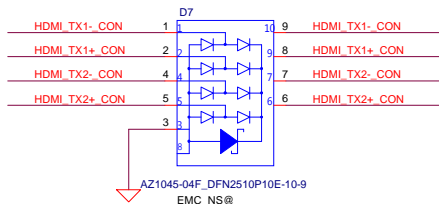
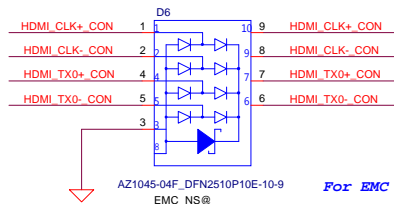




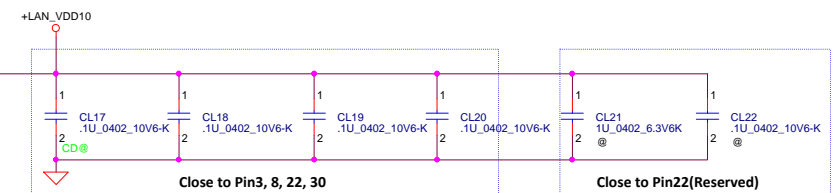
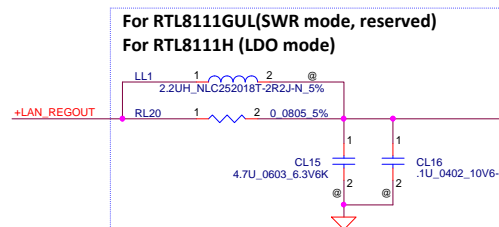
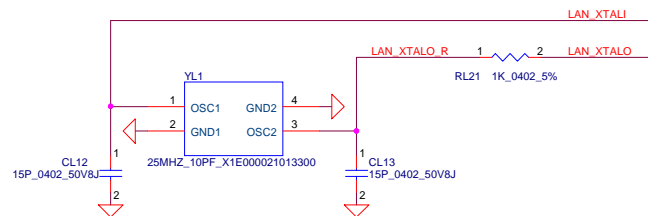
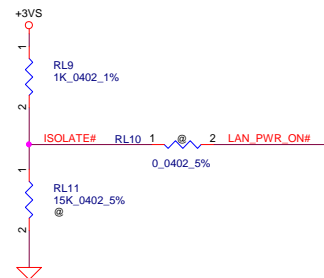
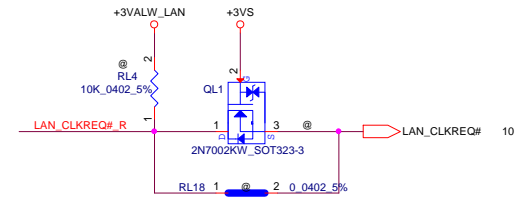
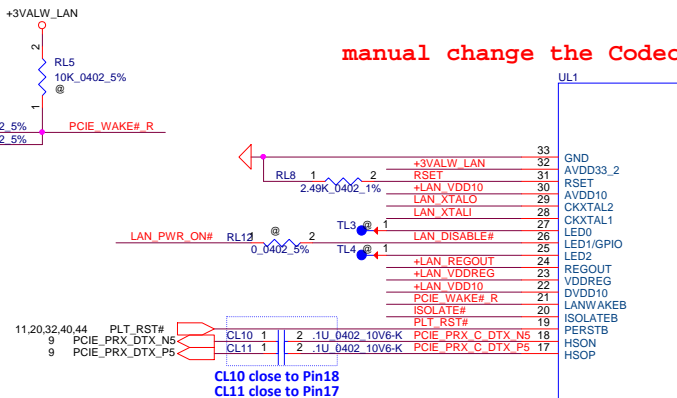
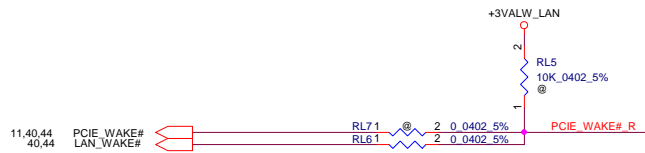
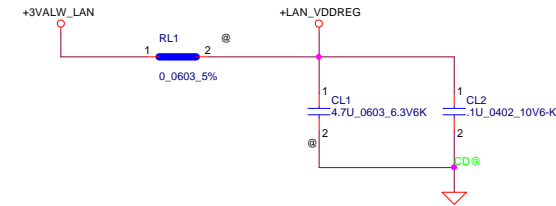
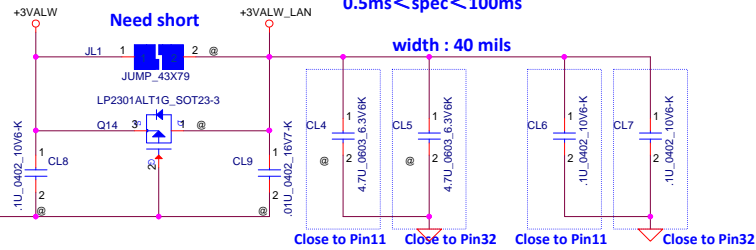
For EMC




Close to JHDMI1



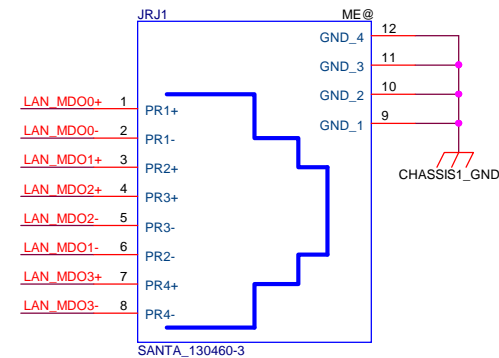
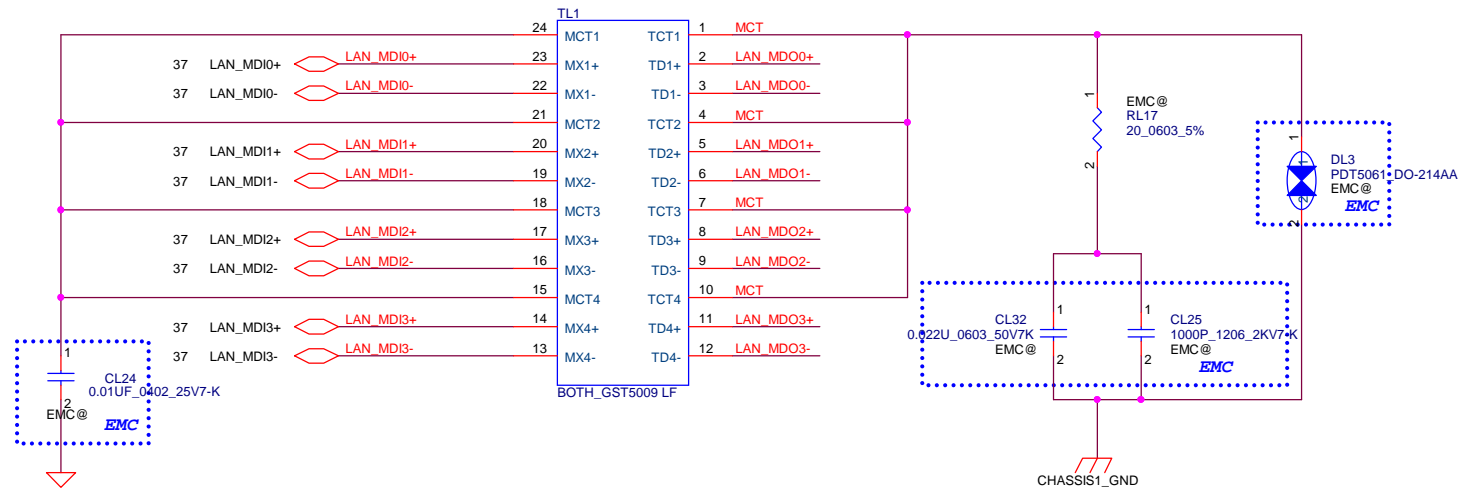
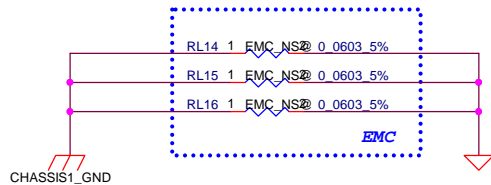
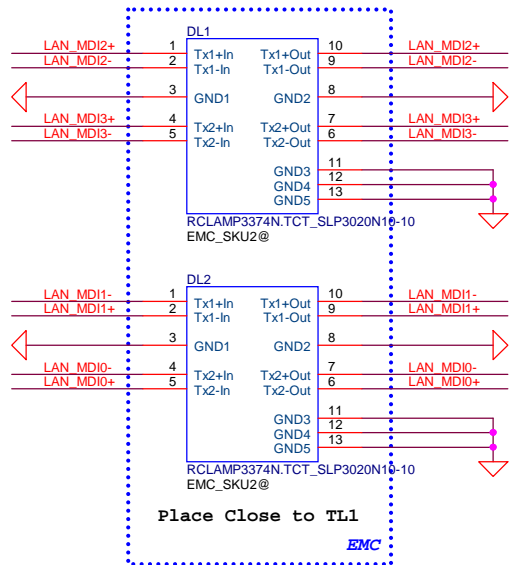
| Security Classification | LC Future Center Secret Data | | Title | | Rev |
|--|------------------------------|-----------------|------------|----------------|-----|
| Issued Date | 2014/12/11 | Deciphered Date | 2015/12/11 | HDMI_CONN | |
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| Date: Thursday, May 28, 2015 | | | | Sheet 34 of 60 | Rev |




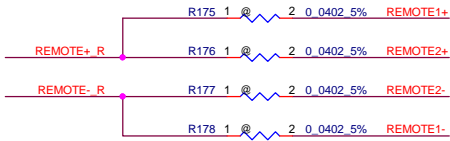
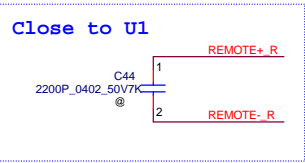
Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

| | | | | | |
|--|------------------------------|-----------------|------------|------------------------|---|
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| Issued Date | 2014/12/11 | Deciphered Date | 2015/12/11 | LAN_RTL8111H_CG | |
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| | | | | | Document Number BMWQ1 |
| Date: Thursday, May 28, 2015 | | | | | Sheet 37 of 60 Rev 0.3 |

DL1/DL2
1'S PN:SC300003M00

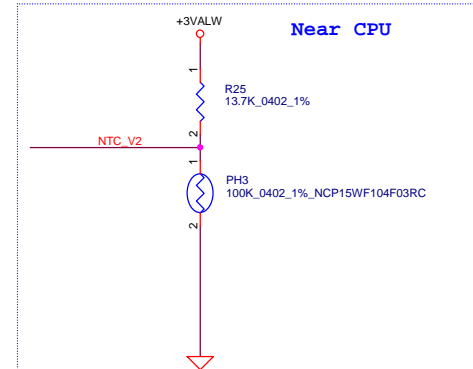
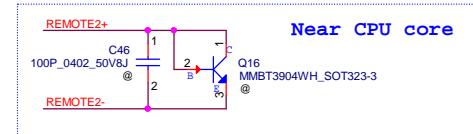
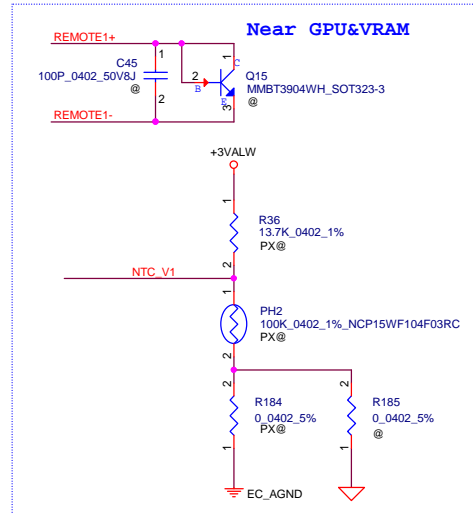
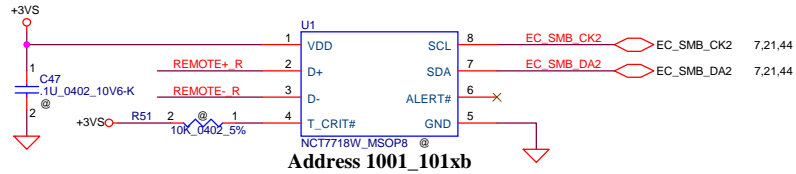


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|---|--|-------------------------------|--|--|--|---------------------------------|-----------------|---|----------|
| Security Classification | | LC Future Center Secret Data | | | | Title LAN_Transformer | |  | |
| Issued Date 2014/12/11 | | Deciphered Date 2015/12/11 | | | | | | | |
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| | | | | | | B | BMWQ1 | | 0.3 |
| Date: | | | | | | Thursday, May 28, 2015 | | Sheet | 38 of 60 |

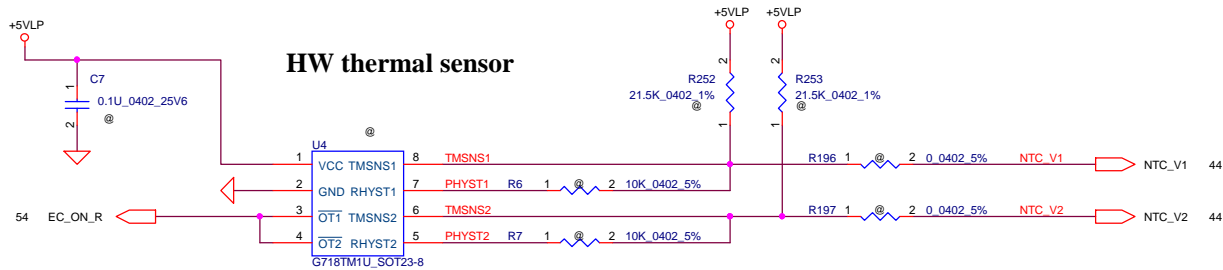


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

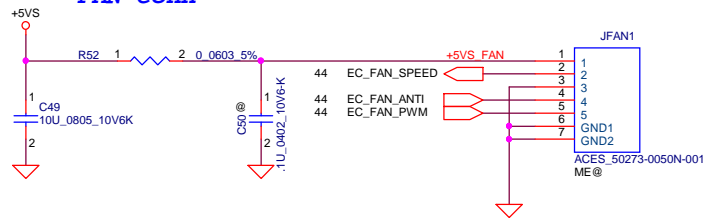


HW thermal sensor

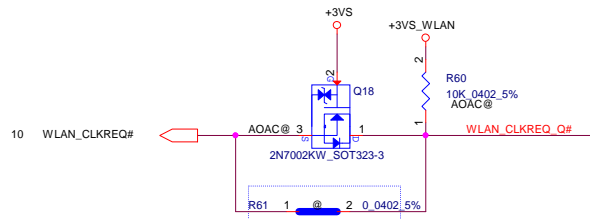
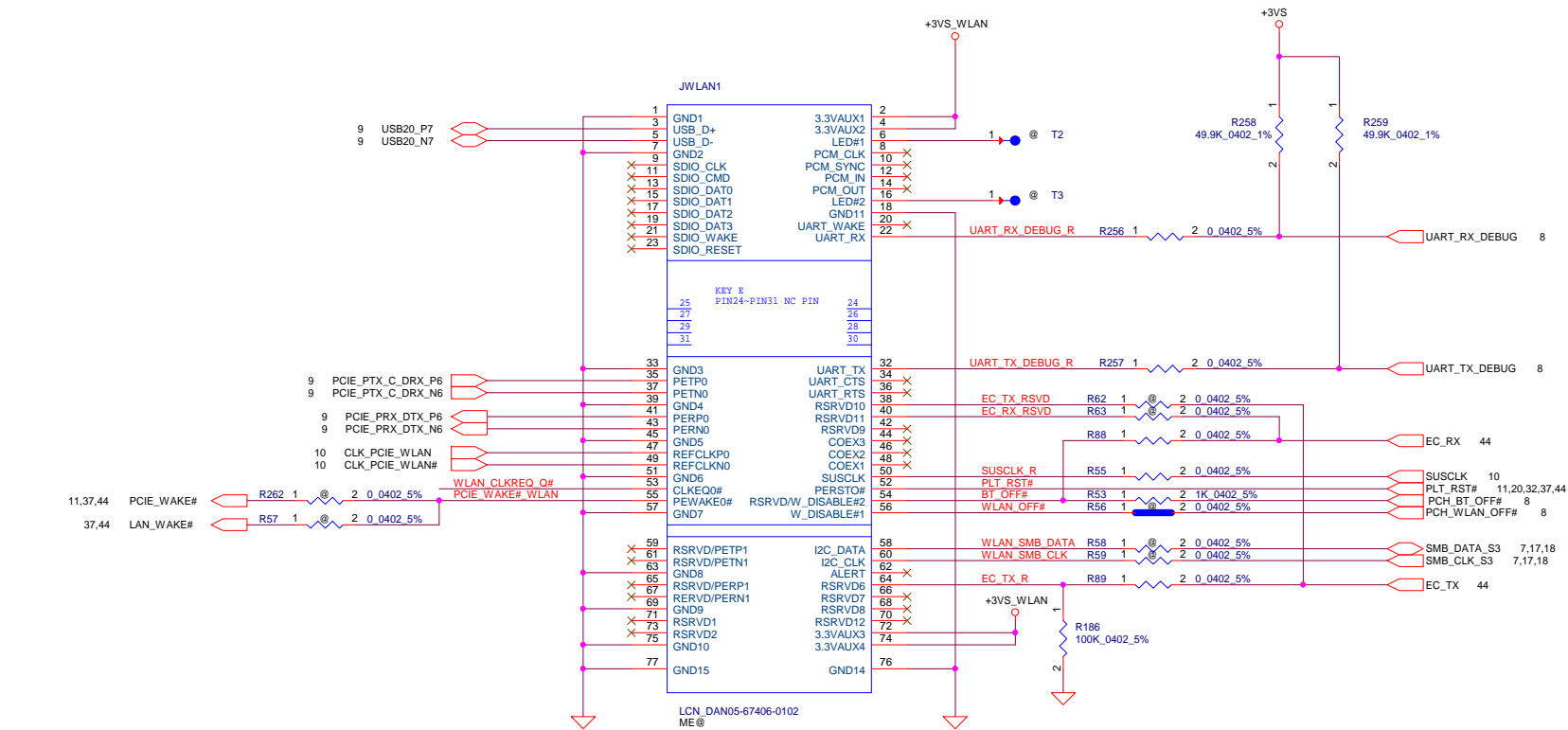


over temperature threshold:
 $RSET=3*RTMH$
92+/-30C
Hysteresis temperature threshold.
 $RHYST=(RSET*RTML)/(3*RTML-RSET)$
56+/-30C

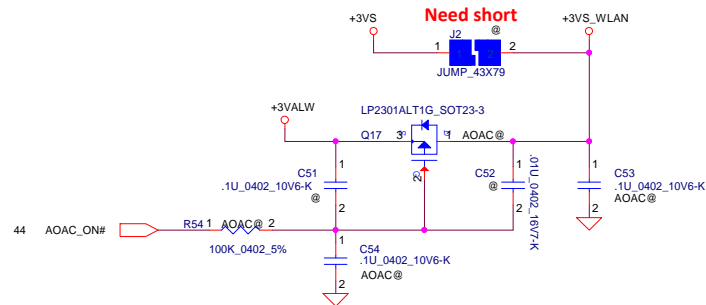
FAN Conn




Mini-Express Card(WLAN/WiMAX)

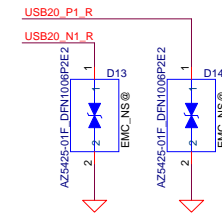
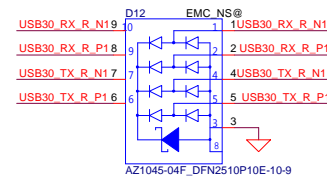
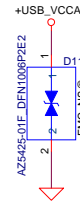
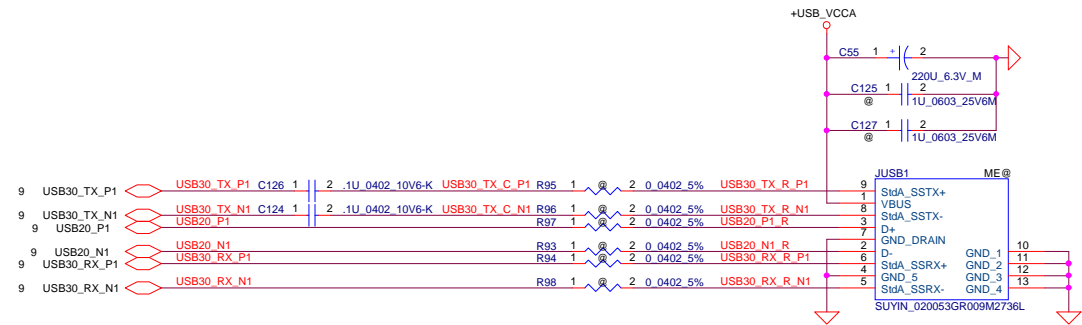
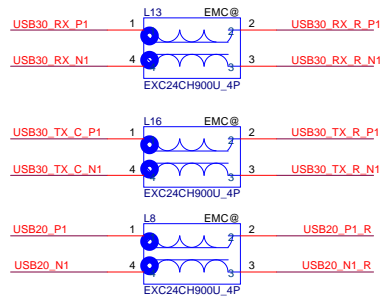
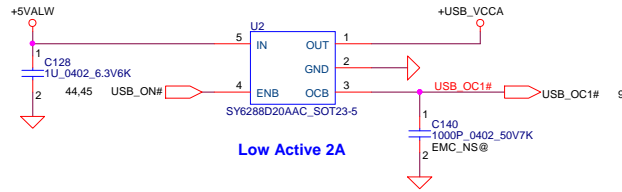


If support AOAC, NC R61;
if not support AOAC, stuff R61.

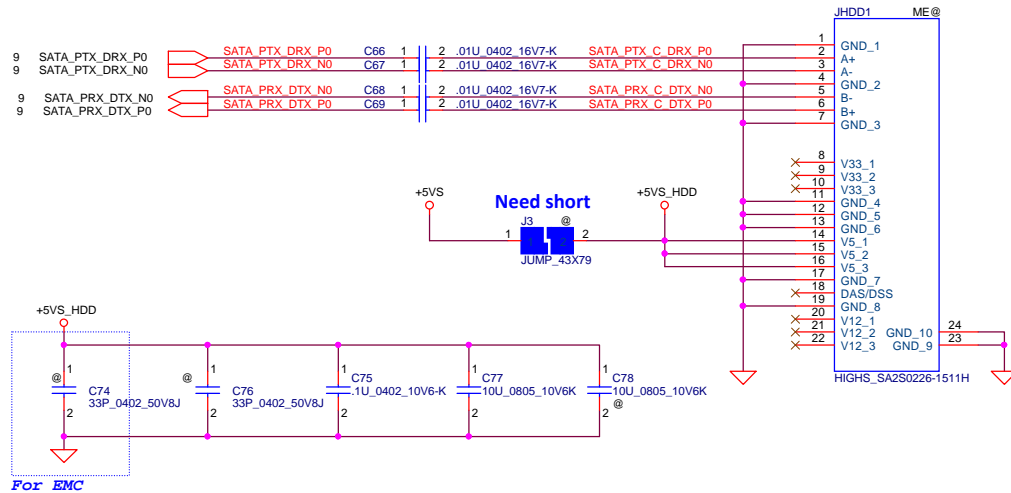


| | | | | | | |
|---|------------|------------------------------|------------|-----------|------------------------|---|
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| | | | | Custom | BMWQ1 | 0.3 |
| | | | | Date: | Thursday, May 28, 2015 | Sheet 40 of 60 |

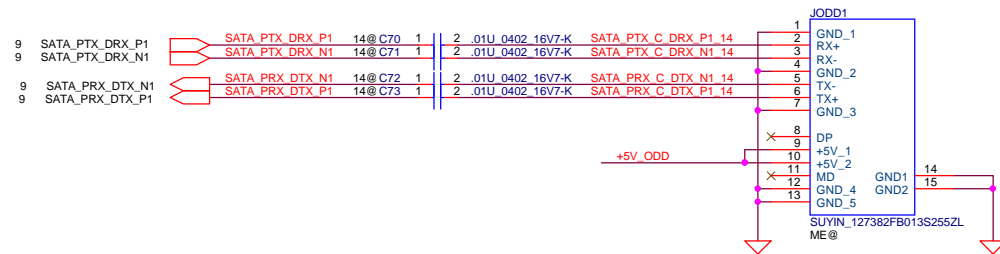
LEFT SIDE USB3.0 PORT x1



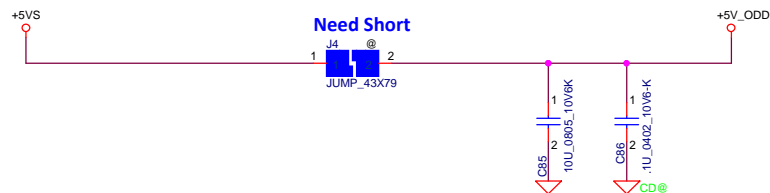
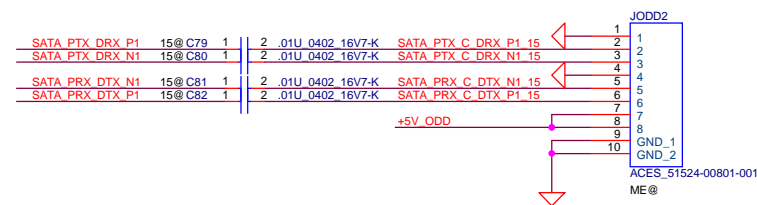
SATA HDD Conn.





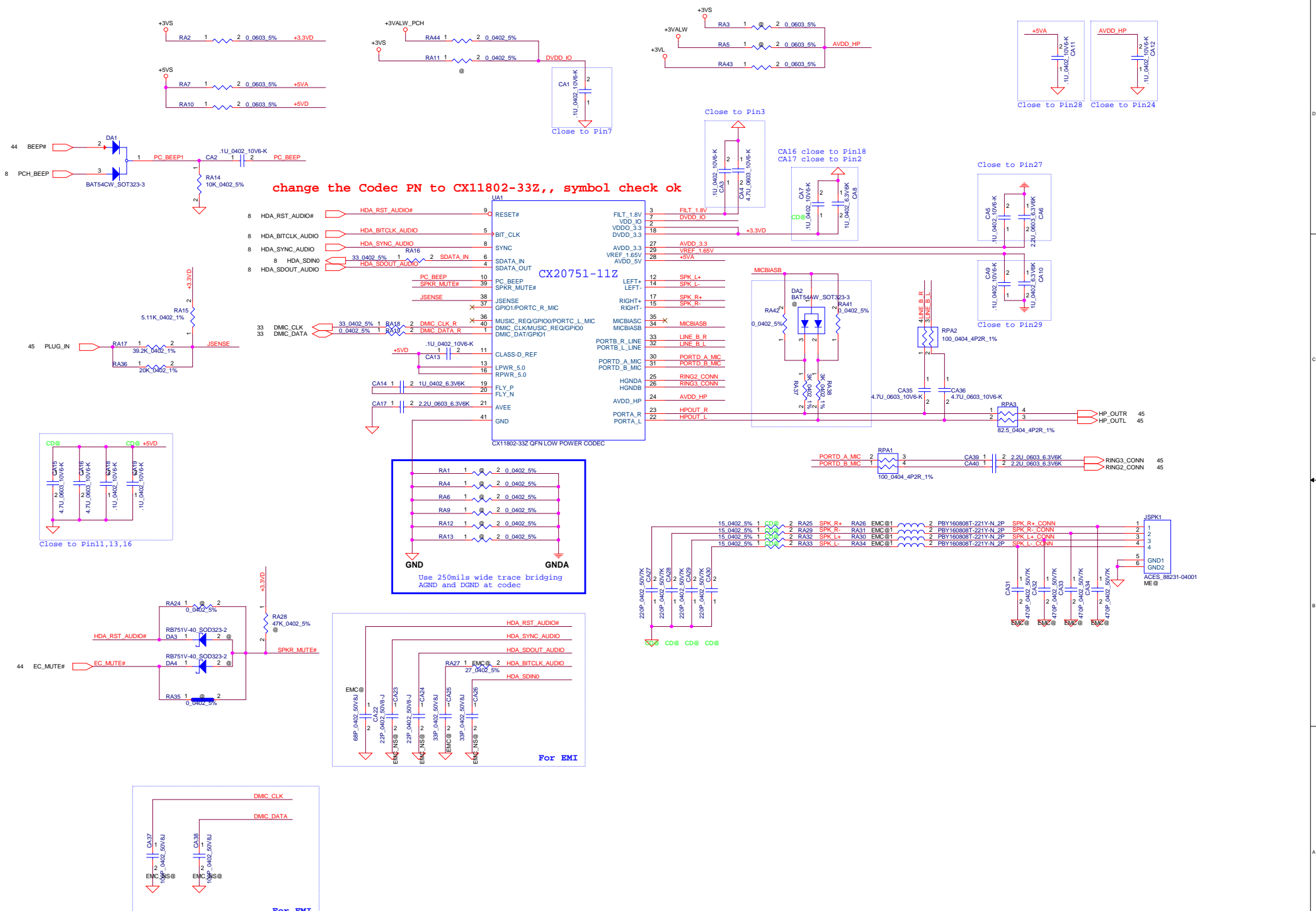
FOR 14" SATA ODD Conn.



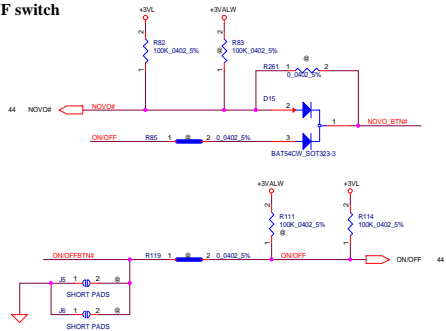
FOR 15" SATA ODD FFC Conn



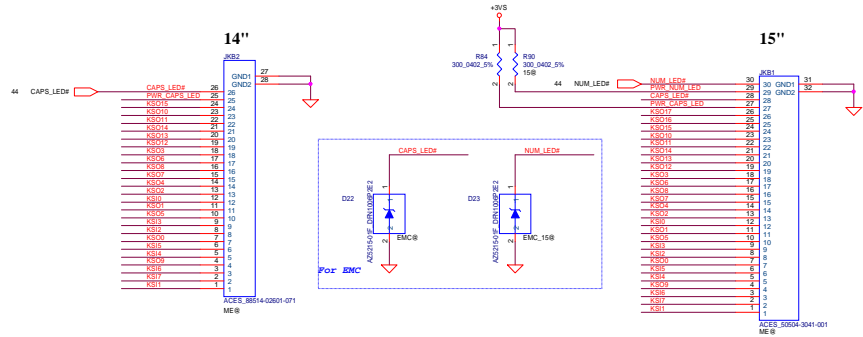
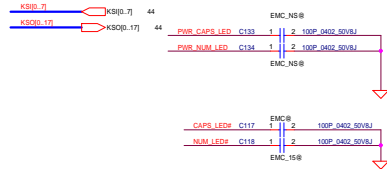
| | | | | | | | | | | | |
|--|--|------------------------------|--|-----------------|--|------------------------|--|---|--|---|--|
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| Custom | | BMWQ1 | | Rev | | 0.3 | | | | | |



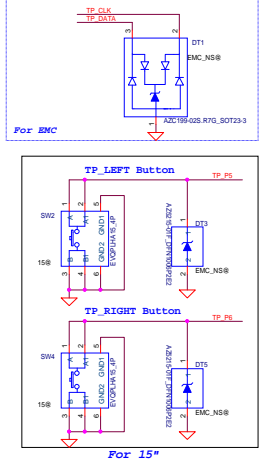
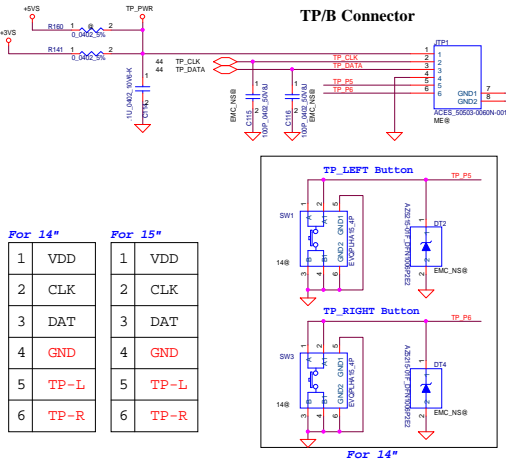
ON/OFF switch



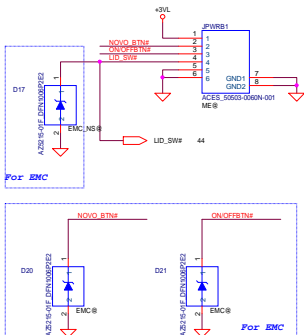
K/B Connector



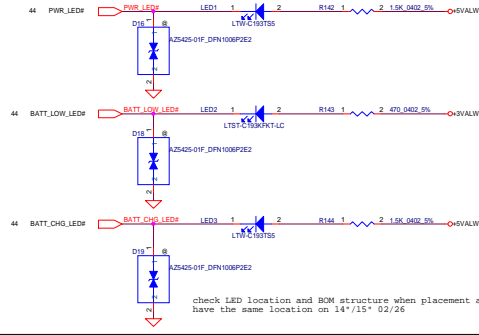
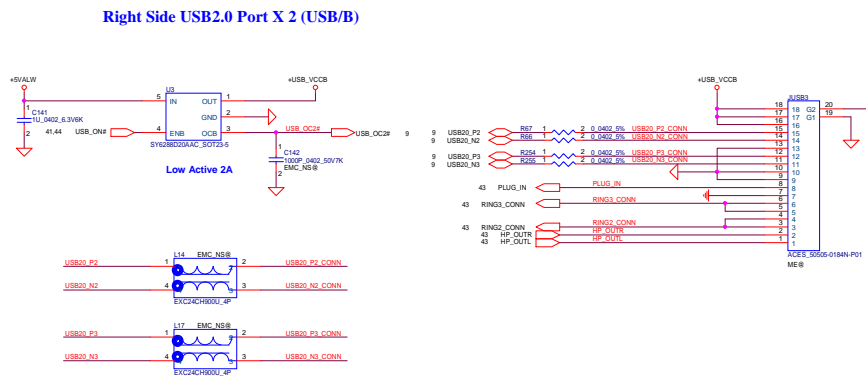
TP/B Connector



PWR/B Connector



USB I/O Connector



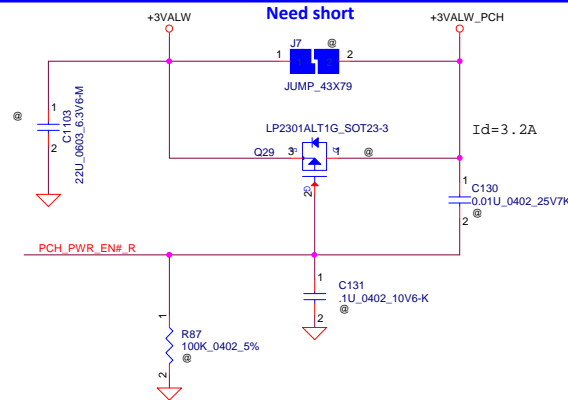
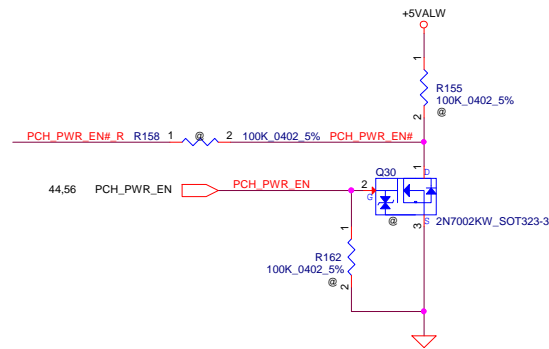
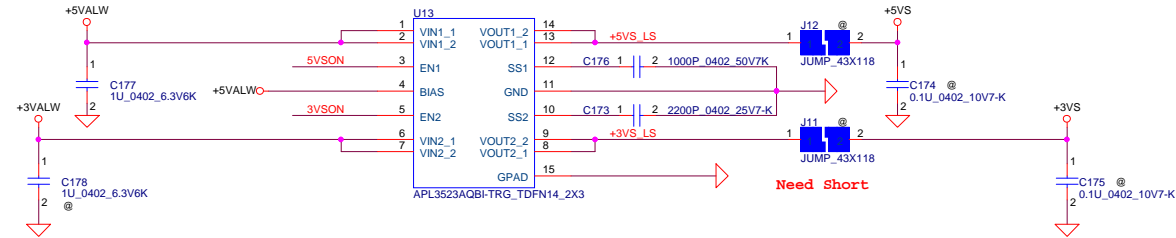
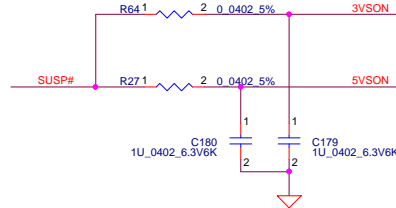
check LED location and BOM structure when placement and Load BOM, PWR LED and BATT LED have the same location on 14''/15'' Q2/26

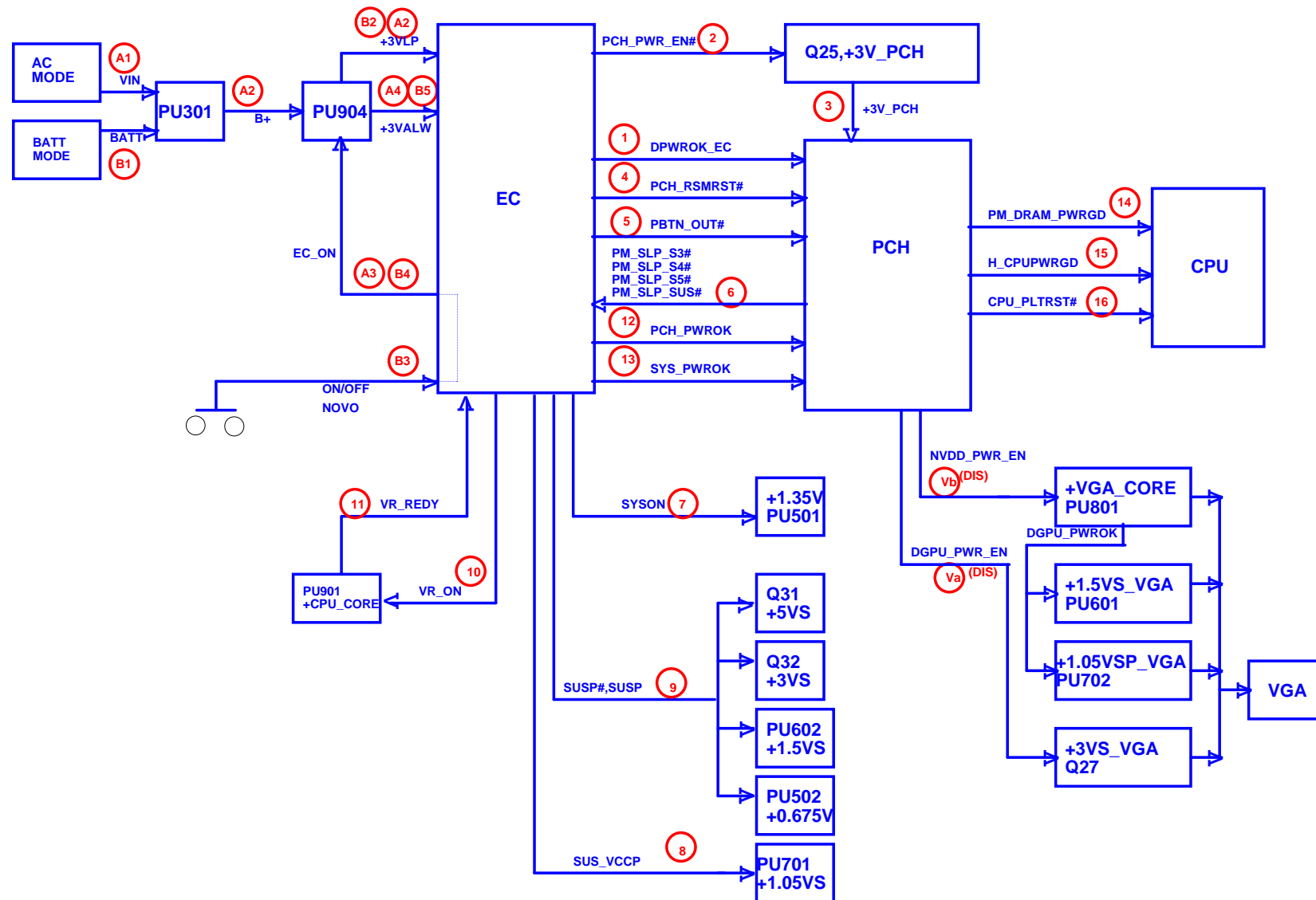
| | | | | | |
|---|--|------------------------------|--|-----------------------|--|
| Security Classification | | LC Future Center Secret Data | | Title | |
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| | | 2015/12/11 | | KBD/PWR/O/LD/TP Conn. | |
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Load Switch
+5VALW To +5VS
+3VALW To +3VS


+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

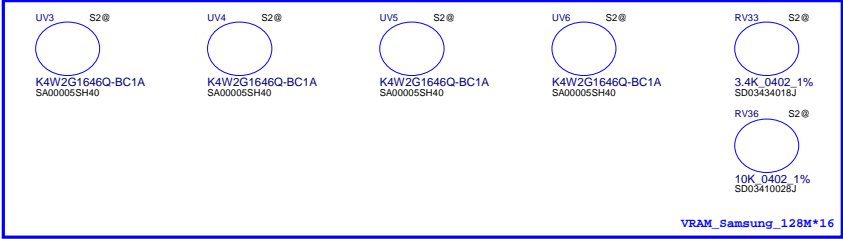
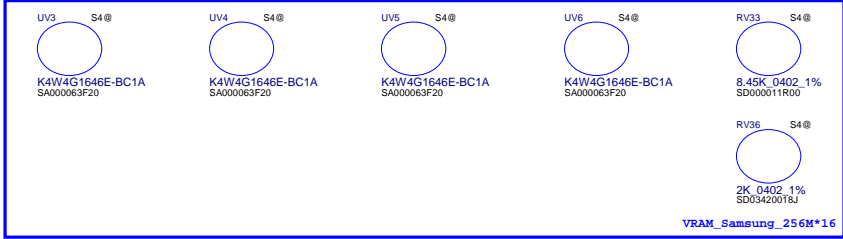
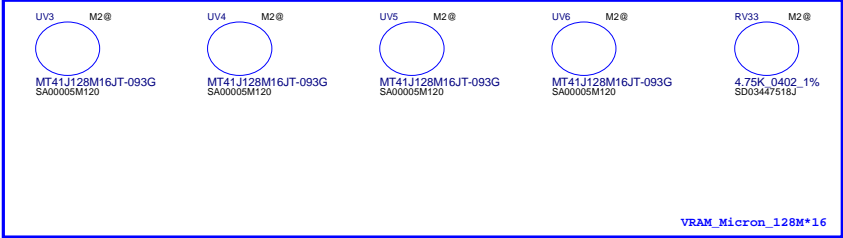
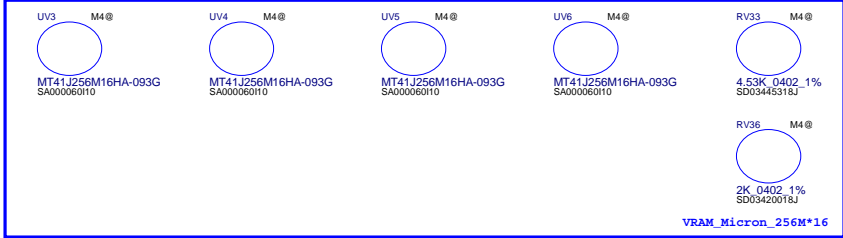
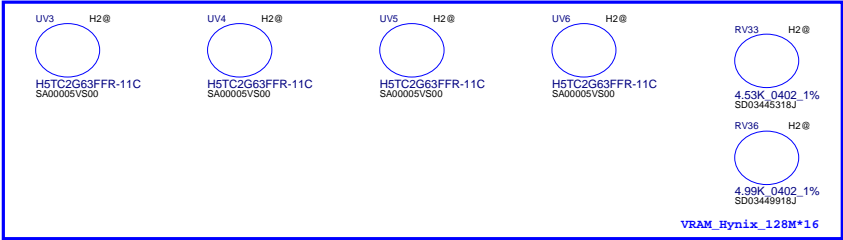
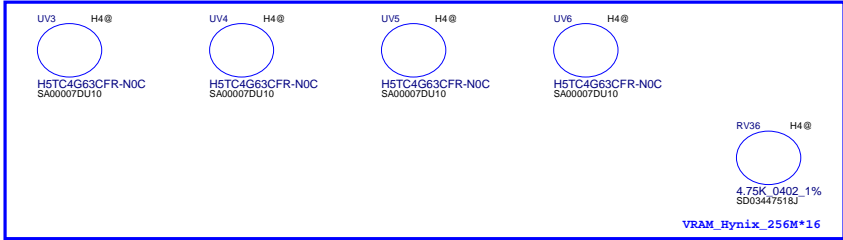
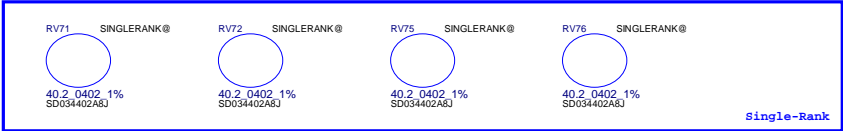
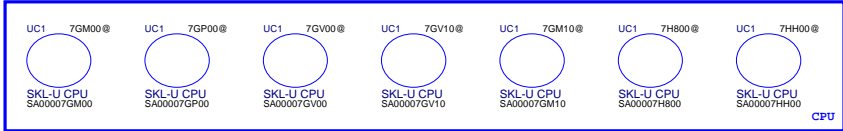
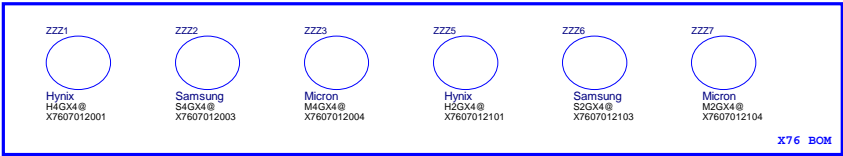
VIN 5V and 3.3V (VBIAS=5V), I_{MAX(per channel)}=6A, R_{ds}=16mohm

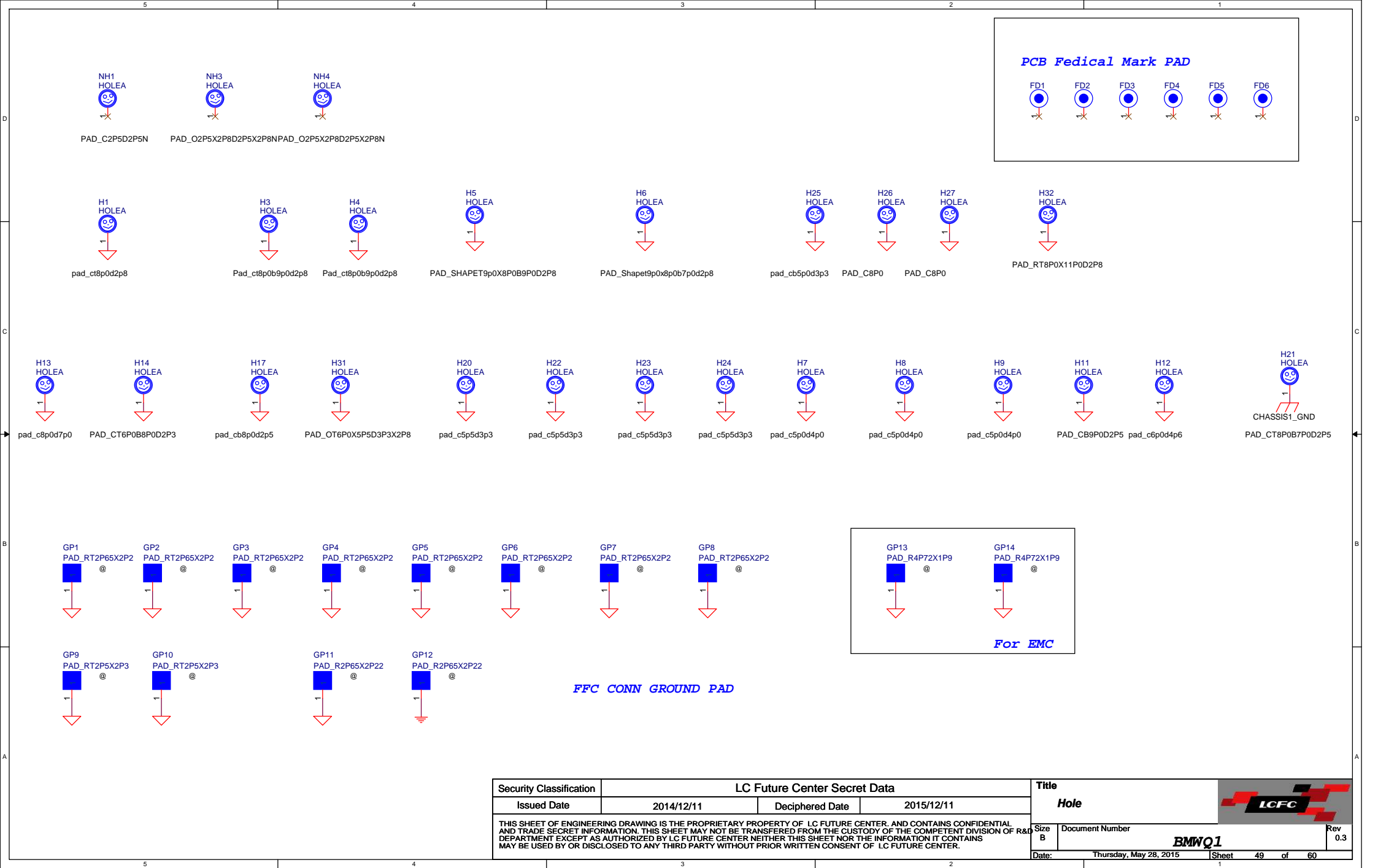


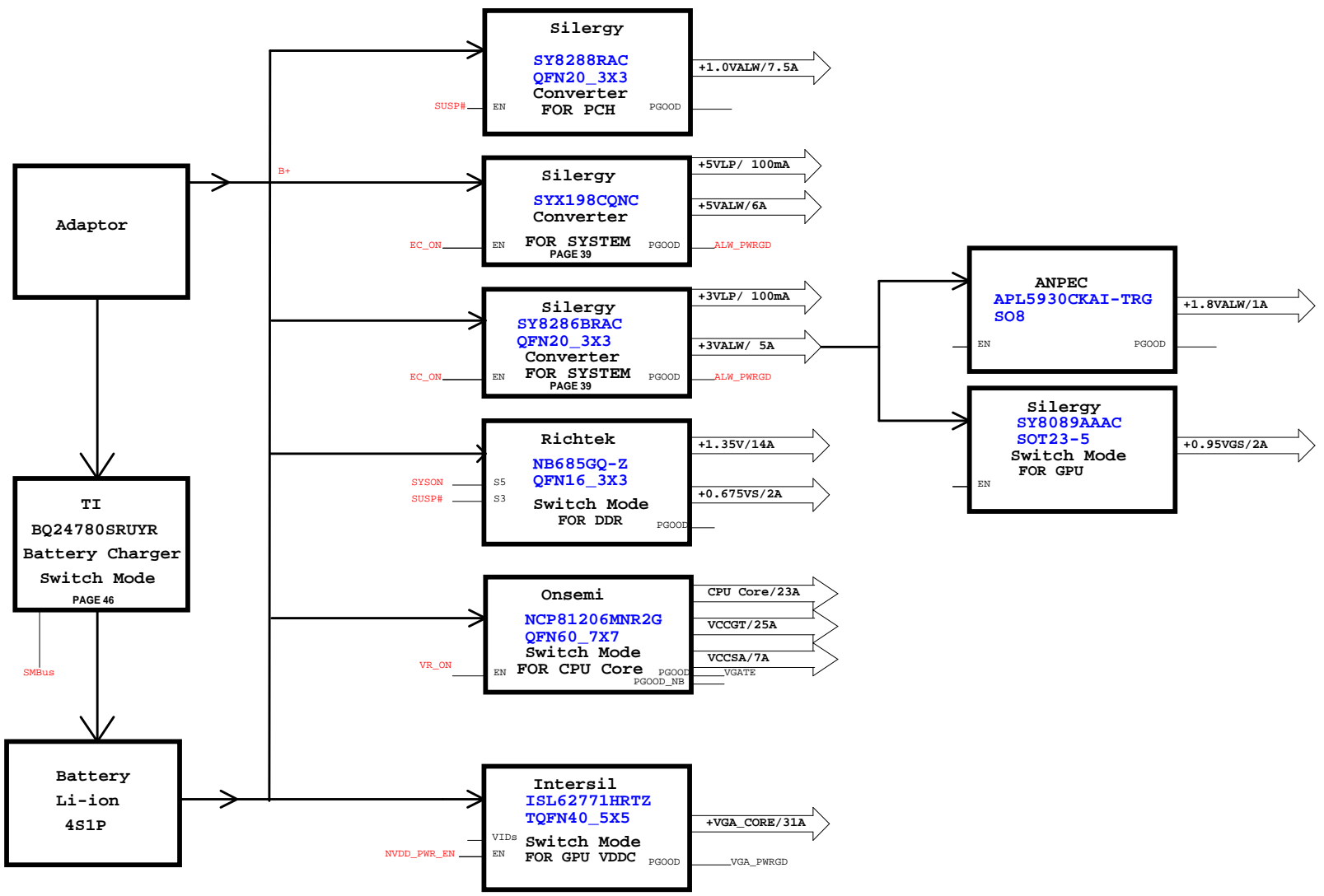


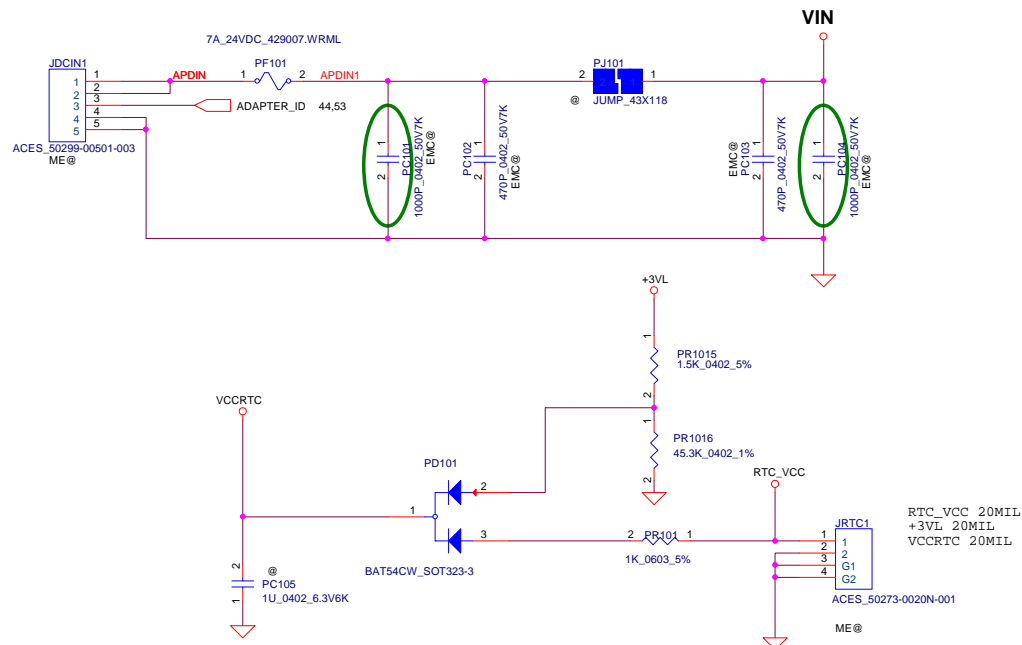
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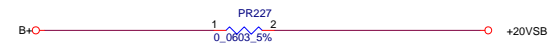
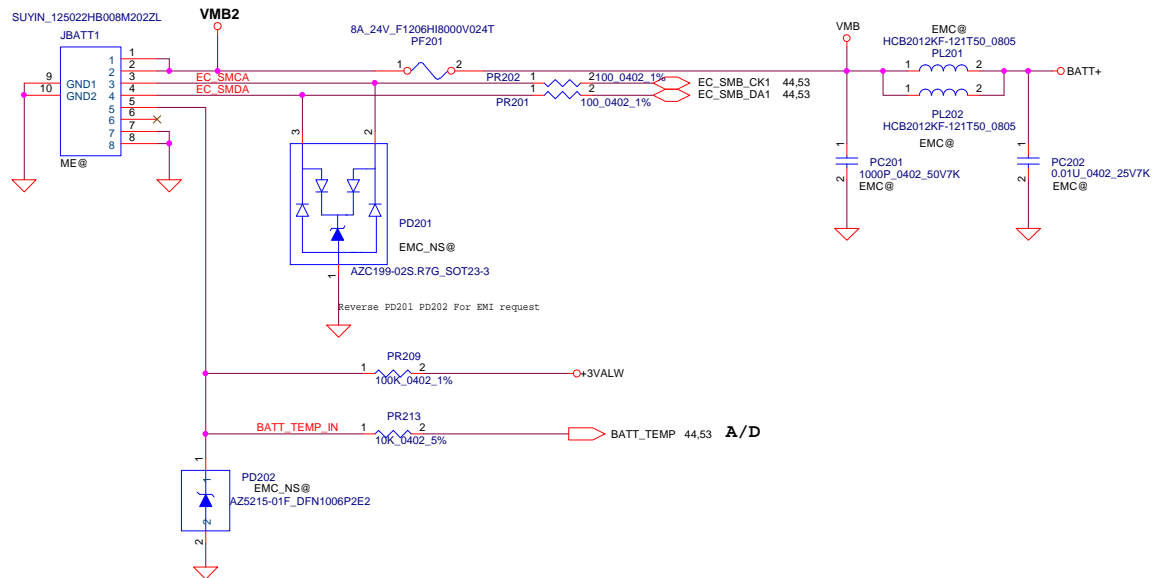
| | | | |
|----------------------|------------------------|---|--|
| Title | |  | |
| Power sequence Block | | | |
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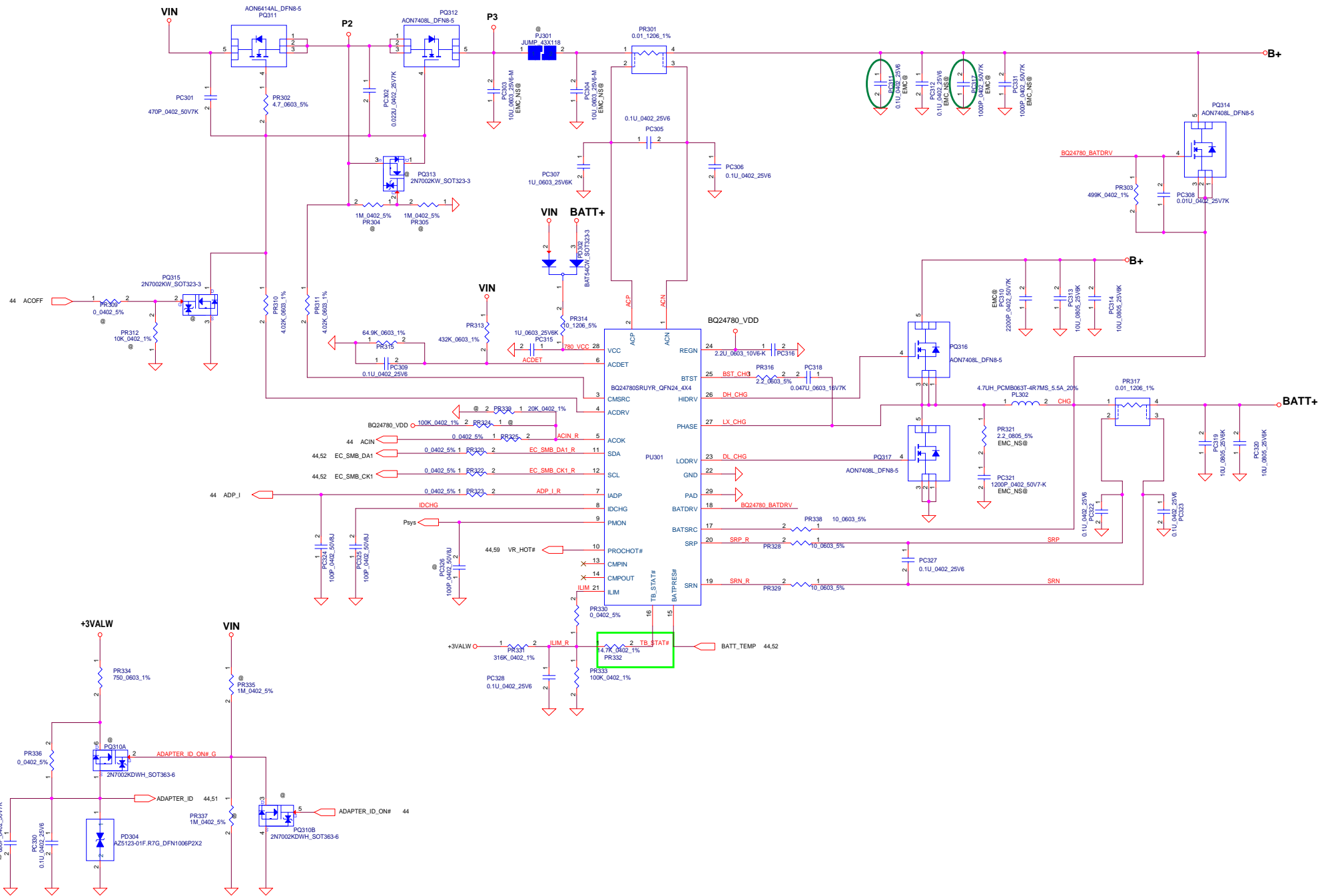


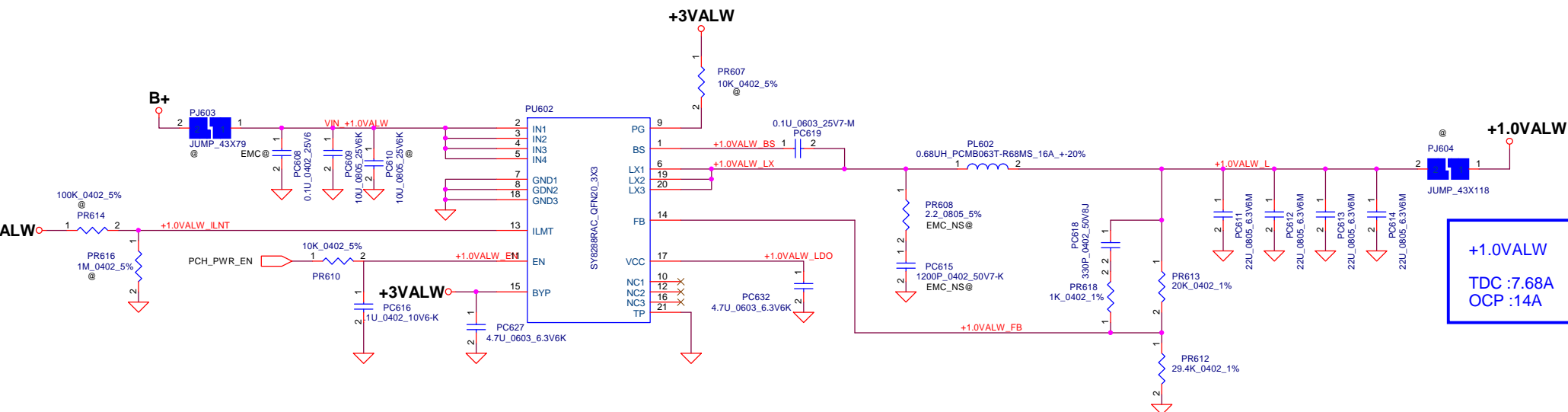
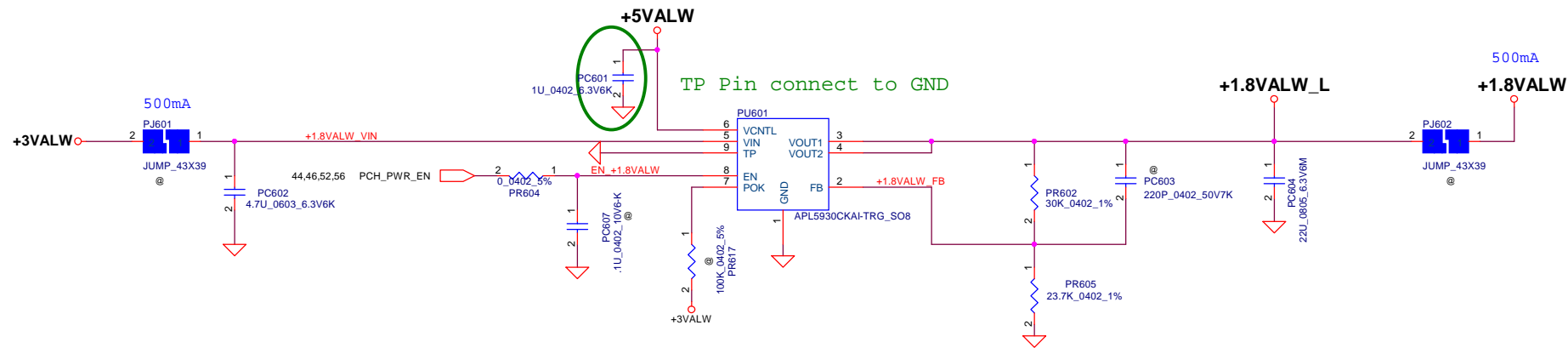










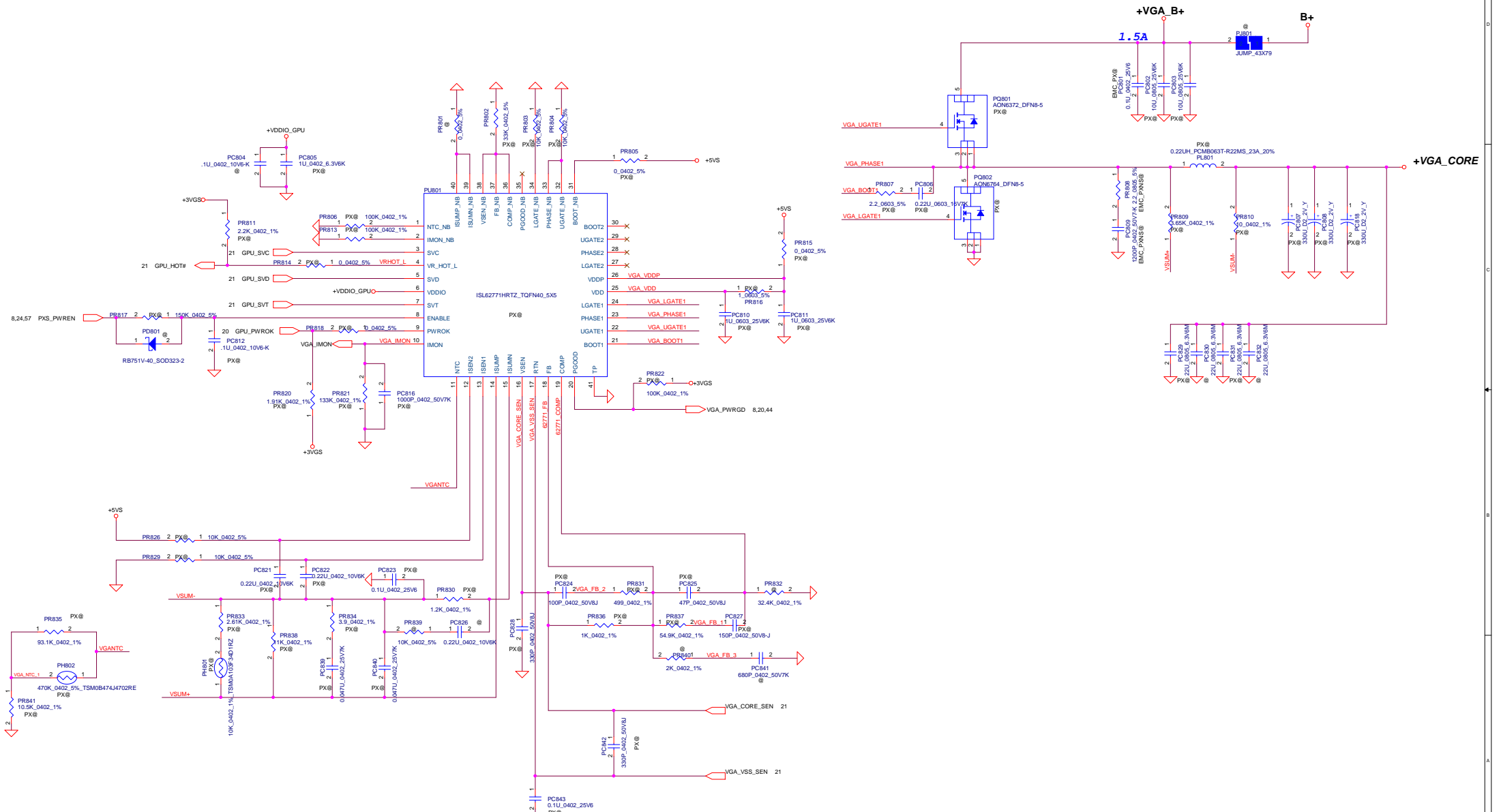



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