# DV14 CP UMA+DIS Schematics Document

# Arrandale

# Intel Ibex Peak-M

## 2011-03-18

## REV : X01

DY : Nopop Component

UMA: POP for UMA option
DIS: POP for DIS option

65 BOM : Nopop for 65 BOM option

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

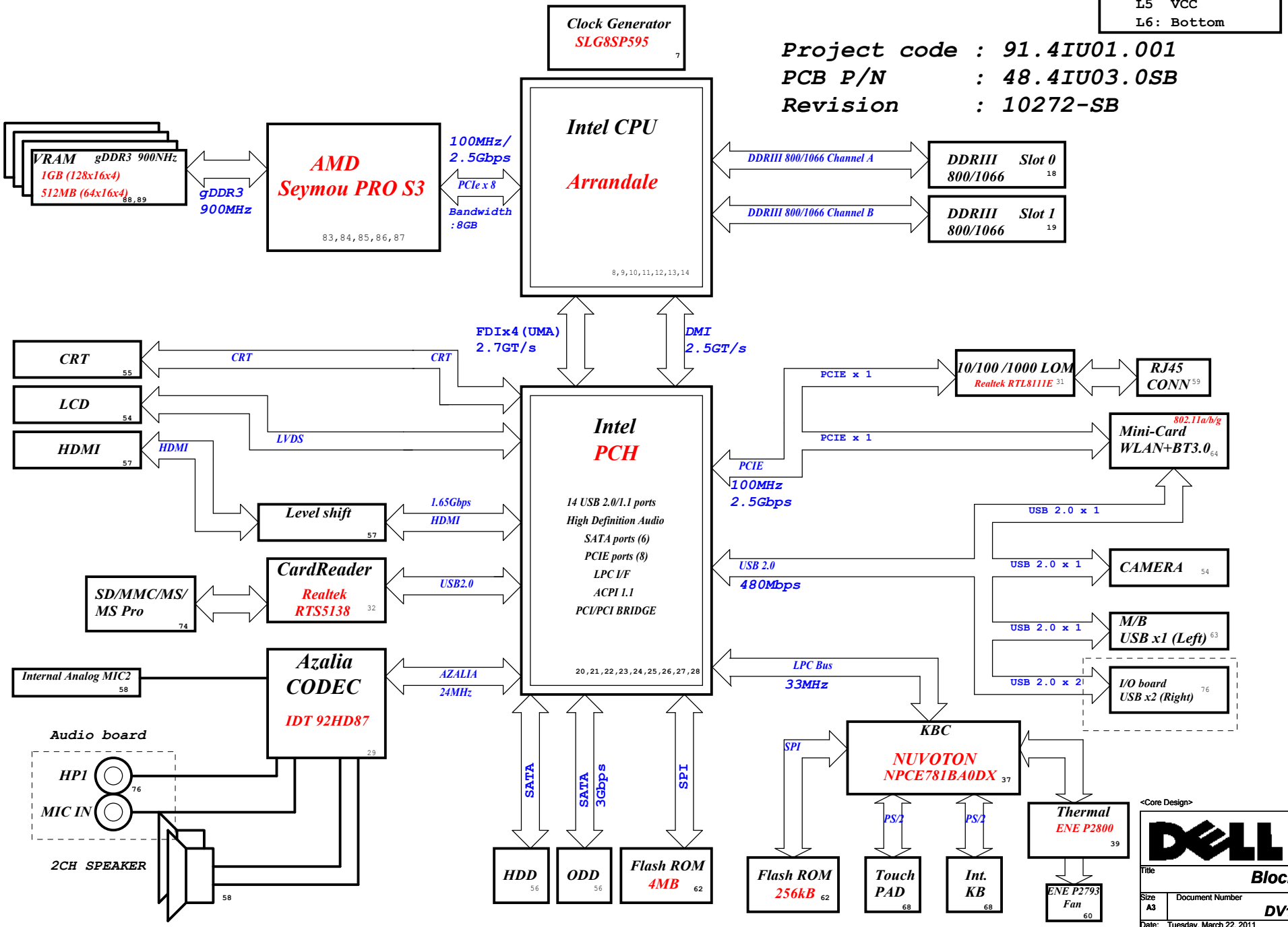
Title: Cover Page
Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00
Date: Friday, March 18, 2011 | Sheet 1 of 100

# DV14 CP Block Diagram (UMA/DIS Co-layout)



| PCB LAYER |
|---|
| L1: Top |
| L2: GND |
| L3: Signal |
| L4: Signal |
| L5 VCC |
| L6: Bottom |

Project code : 91.4IU01.001
PCB P/N : 48.4IU03.0SB
Revision : 10272-SB




**CPU DC/DC** ISL62882 47,48

| INPUTS | OUTPUTS |
|---|---|
| +PWR_SRC | +VCC_CORE |

**SYSTEM DC/DC** RT8237AGQW 49

| INPUTS | OUTPUTS |
|---|---|
| +PWR_SRC | +1.05V_VTT |

**SYSTEM DC/DC** TPS51123RGER 46

| INPUTS | OUTPUTS |
|---|---|
| +PWR_SRC | +5V_ALW2<br>+3.3V_RTC_LDO<br>+5V_ALW<br>+3.3V_ALW<br>+15V_ALW |

**SYSTEM DC/DC** RT8207LGQW 50

| INPUTS | OUTPUTS |
|---|---|
| +PWR_SRC | +1.5V_SUS<br>+0.75V_DDR_VTT<br>+V_DDR_REF |

**SYSTEM DC/DC** G9731F11U 93

| INPUTS | OUTPUTS |
|---|---|
| +1.5V_SUS | +1V_GPU_PCIE |

**VGA** RT8208BGQW 92

| INPUTS | OUTPUTS |
|---|---|
| +PWR_SRC | +VCC_GFX_CORE |

**MAXIM CHARGER** BQ24707RGRRG4 45

| INPUTS | OUTPUTS |
|---|---|
| +DC_IN<br>+PBATT | +PWR_SRC |

**SYSTEM DC/DC** RT9025-25PSP 51

| INPUTS | OUTPUTS |
|---|---|
| +3.3V_ALW | +1.8V_RUN |

**SYSTEM DC/DC** RT9025-25PSP 93

| INPUTS | OUTPUTS |
|---|---|
| +3.3V_ALW | +1.8V_RUN_GPU |

**SYSTEM DC/DC** Switches 42

| INPUTS | OUTPUTS |
|---|---|
| +1.5V_SUS<br>+5V_ALW<br>+3.3V_ALW | +1.5V_RUN<br>+5V_RUN<br>+3.3V_RUN |

<Core Design>

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Title: Block Diagram

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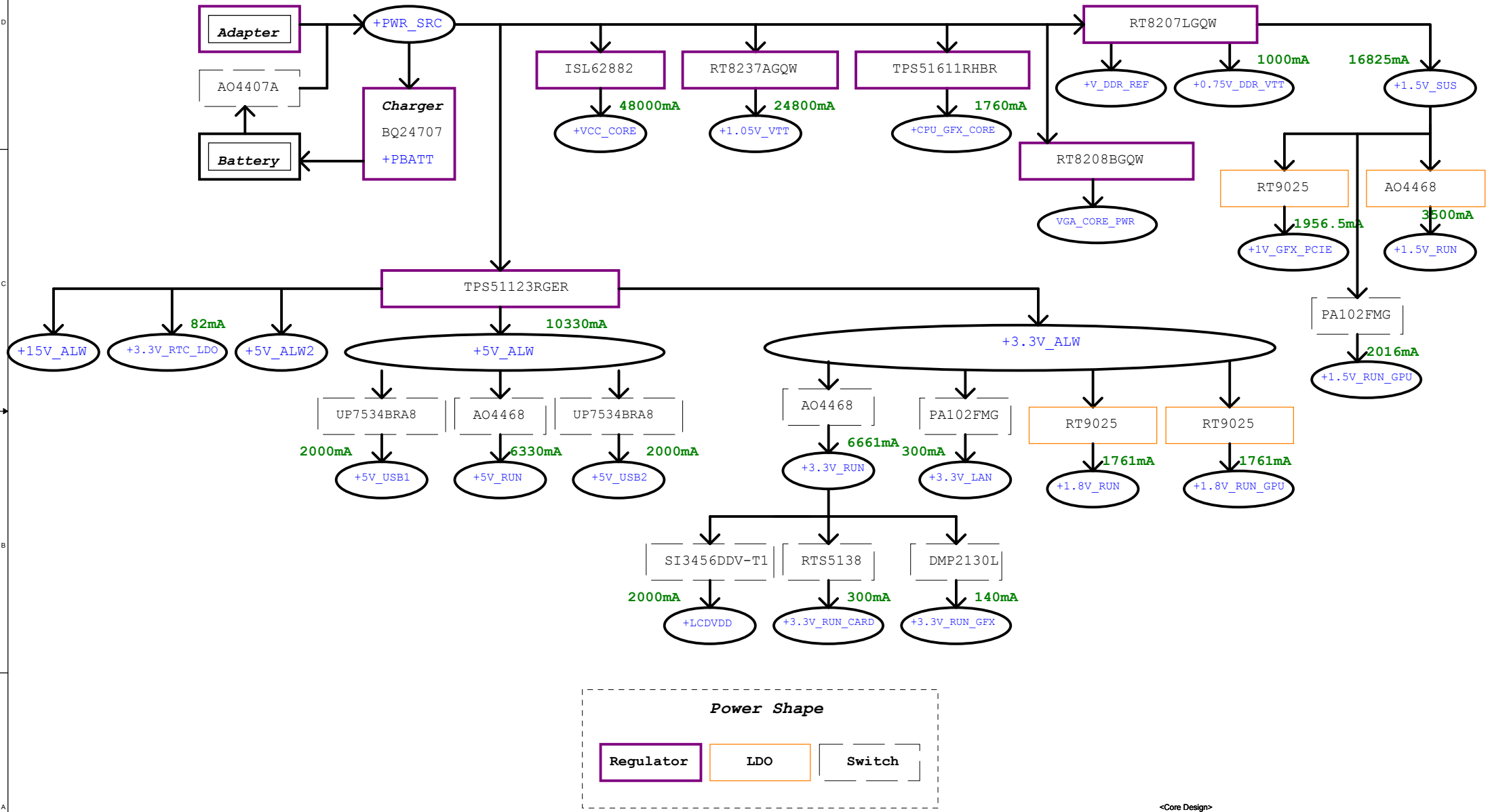


<Core Design>

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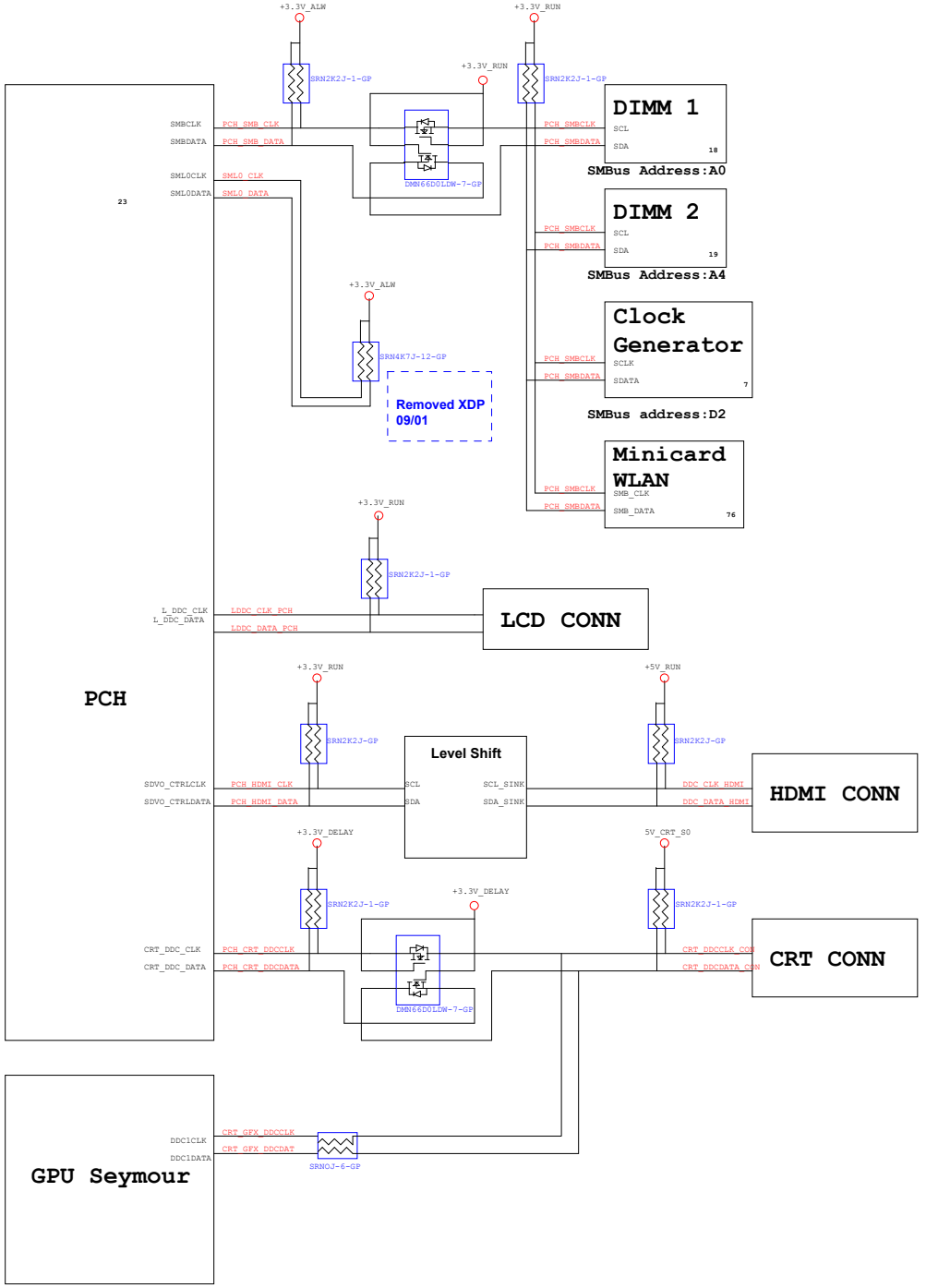
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

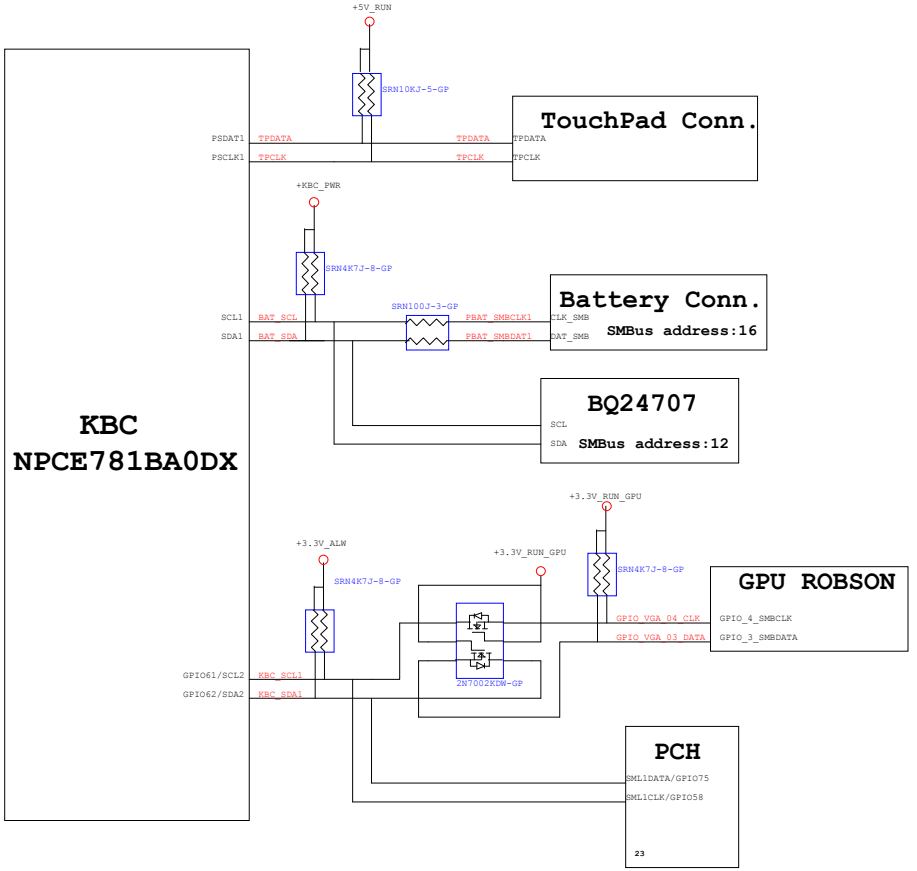
Date: Tuesday, March 15, 2011 Sheet 3 of 100

# PCH SMBus Block Diagram




# KBC SMBus Block Diagram






<Core Design>

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Title: SMBUS Block Diagram

| Size | Document Number | Rev |
|---|---|---|
| A2 | DV14 CP UMA+DIS | X00 |

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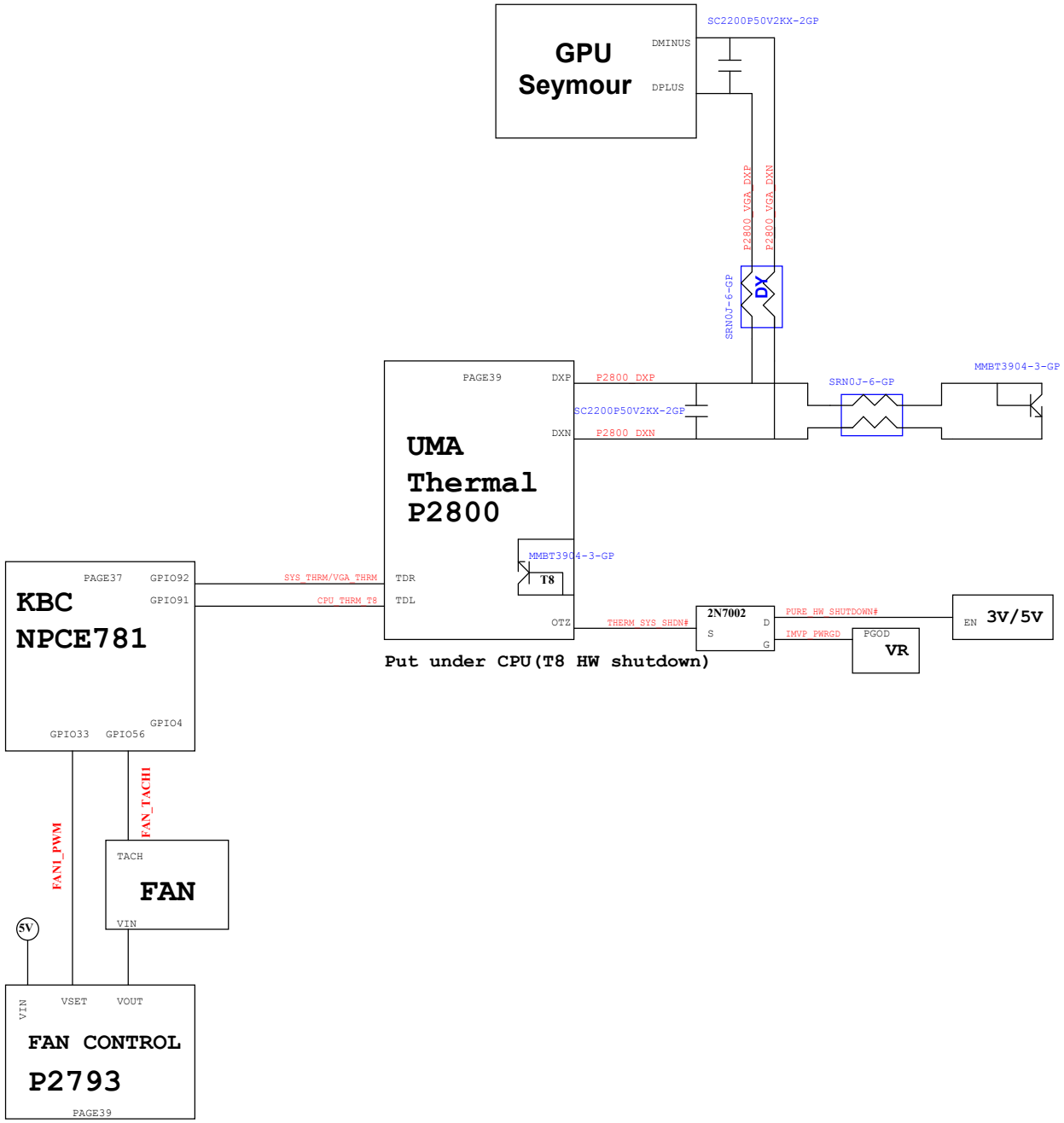
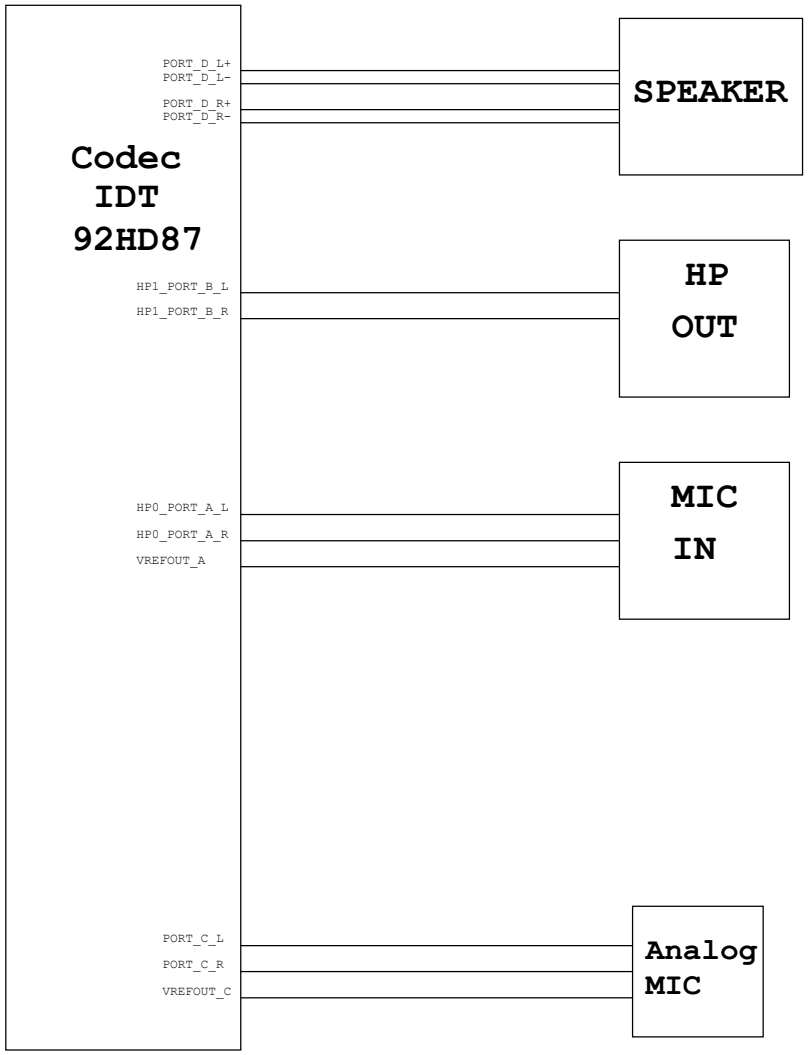
# Thermal Block Diagram




# Audio Block Diagram




<Core Design>

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Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: DV14 CP UMA+DIS | Rev: X00

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# PCH Strapping

Calpella Schematic Checklist Rev.0_7

| Name | Schematics Notes |
|---|---|
| SPKR | **Reboot option at power-up**<br>**Default Mode:** Internal weak Pull-down.<br>**No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-k<br>- 10-k weak pull-up resistor. |
| INIT3_3V# | Weak internal pull-down. Do not pull high. |
| GNT3#/<br>GPIO55 | **Default Mode:** Internal pull-up.<br>**Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-k weak<br>pull-down resistor). |
| INTVRMEN | **High (1) = Integrated VRM is enabled**<br>**Low (0) = Integrated VRM is disabled** |
| GNT0#,<br>GNT1#/GPIO51 | **Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required.<br>**Boot from PCI:** Connect GNT1# to ground with 1-k pull-down<br>resistor. Leave GNT0# Floating.<br>**Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-k<br>pull-down resistor. |
| GNT2#/<br>GPIO53 | **Default - Internal pull-up.**<br>**Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops). |
| GPIO33 | **Default:** Do not pull low.<br>**Disable ME in Manufacturing Mode:** Connect to ground with 1-k pull-down resistor. |
| SPI_MOSI | **Enable iTPM:** Connect to Vcc3_3 with 8.2-k weak pull-up<br>**Disable iTPM:** left floating, no pull-down required. |
| NV_ALE | **Enable Danbury:** Connect to Vcc3_3 with 8.2-k weak pull-up resistor.<br>**Disable Danbury:** Connect to ground with 4.7-k weak pull-down resistor. |
| NC_CLE | Weak internal pull-up. Do not pull low. |
| HAD_DOCK_EN#<br>/GPIO[33] | **Low (0):** Flash Descriptor Security will be overridden.<br>**High (1) :** Flash Descriptor Security will be in effect. |
| HDA_SDO | Weak internal pull-down. Do not pull high. |
| HDA_SYNC | Weak internal pull-down. Do not pull high. |
| GPIO15 | Weak internal pull-down. Do not pull high. |
| GPIO8 | Weak internal pull-up. Do not pull low. |
| GPIO27 | **Default = Do not connect (floating)**<br>High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.<br>Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails. |

# Processor Strapping

Calpella Schematic Checklist Rev.0_7

| Pin Name | Strap Description | Configuration (Default value for each bit is 1 unless specified otherwise) | Default Value |
|---|---|---|---|
| CFG[4] | **Embedded DisplayPort Presence** | **1:** Disabled - No Physical Display Port attached to Embedded DisplayPort.<br>**0:** Enabled - An external Display Port device is connected to the Embedded Display Port. | **1** |
| CFG[3] | **PCI-Express Static Lane Reversal** | **1:** Normal Operation.<br>**0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ... | **1** |
| CFG[0] | **PCI-Express Configuration Select** | **1:** Single PCI-Express Graphics<br>**0:** Bifurcation enabled | **1** |
| CFG[7] | **Reserved - Temporarily used for early Clarksfield samples.** | **Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor<br>**Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].<br>For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality. | **0** |

# PCIE Routing

| | |
|---|---|
| LANE2 | MiniCard WLAN |
| LANE3 | LAN |

# USB Table

| USB | |
|---|---|
| Pair | Device |
| 0 | X |
| 1 | USB1 |
| 2 | USB2 |
| 3 | USB3 |
| 4 | X |
| 5 | X |
| 6 | X |
| 7 | X |
| 8 | X |
| 9 | WLAN for BLUETOOTH |
| 10 | CARD READER |
| 11 | CAMERA |
| 12 | X |
| 13 | X |

<Core Design>

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Title: Table of Content

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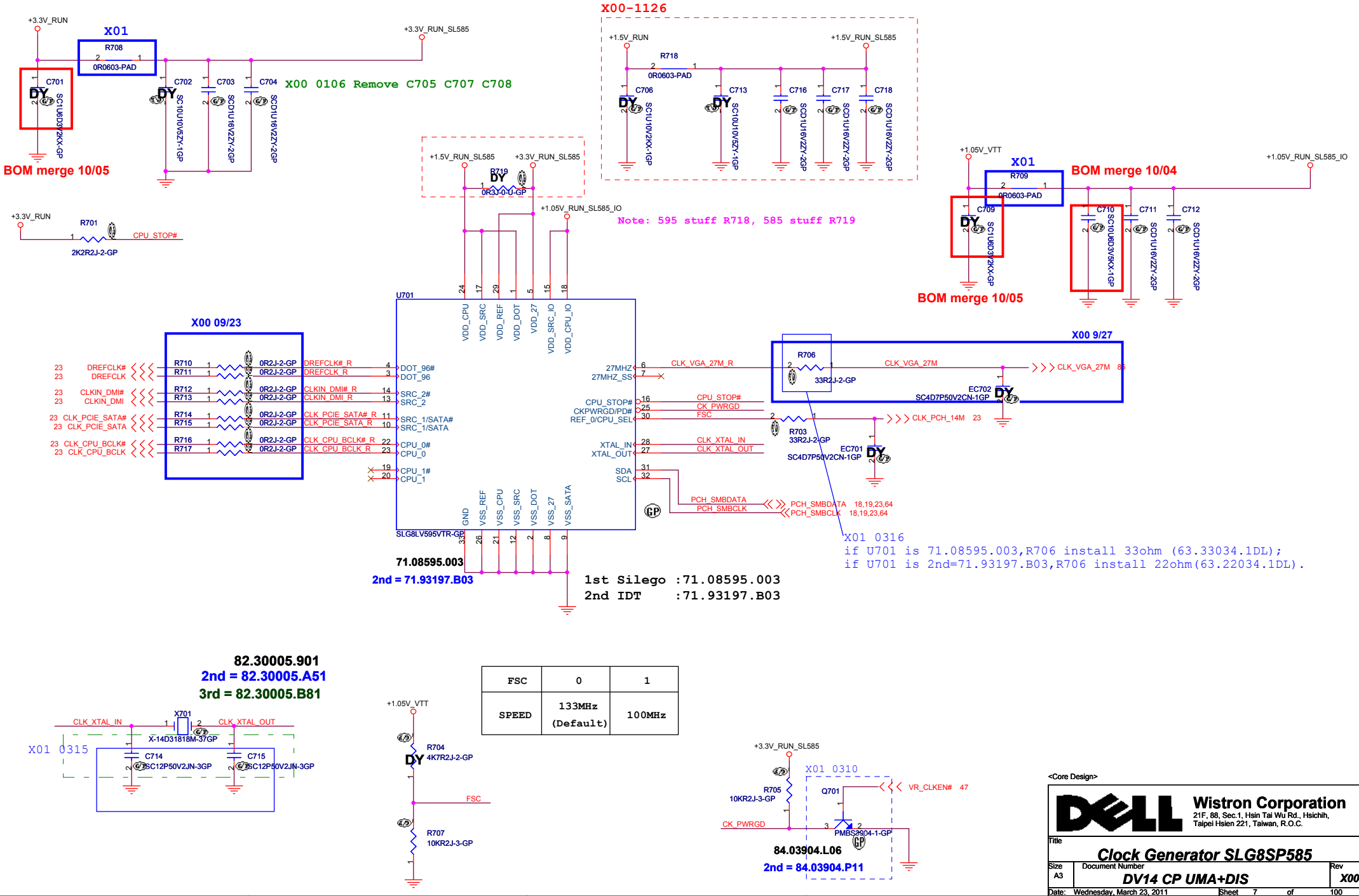
SSID = CLOCK






| FSC | 0 | 1 |
|---|---|---|
| SPEED | 133MHz (Default) | 100MHz |

<Core Design>

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Title: Clock Generator SLG8SP585

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

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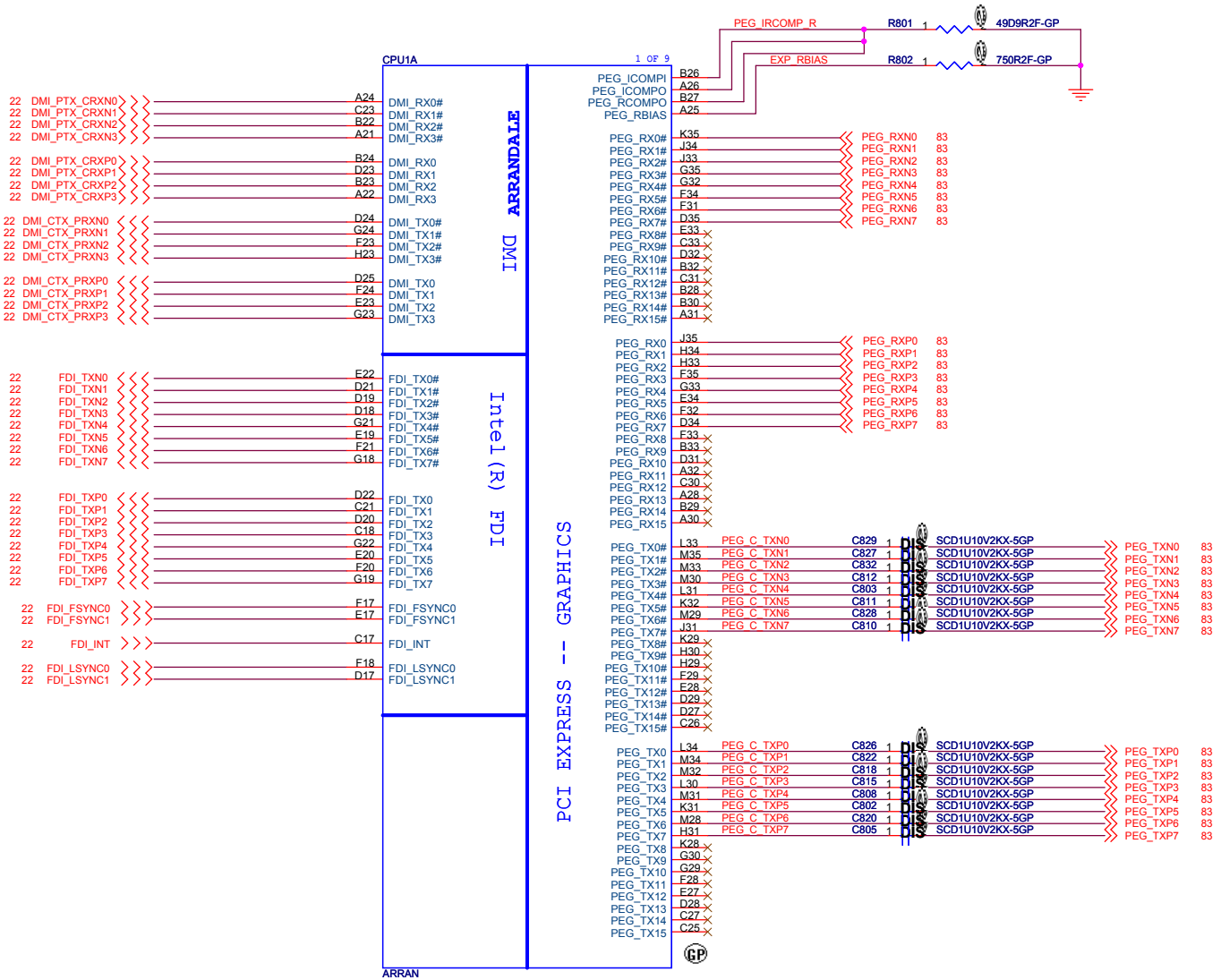
SSID = CPU






62.10055.321

2nd = 62.10040.821

3rd = 62.10055.551

<Core Design>

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Title: CPU (PCIE/DMI/FDI)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

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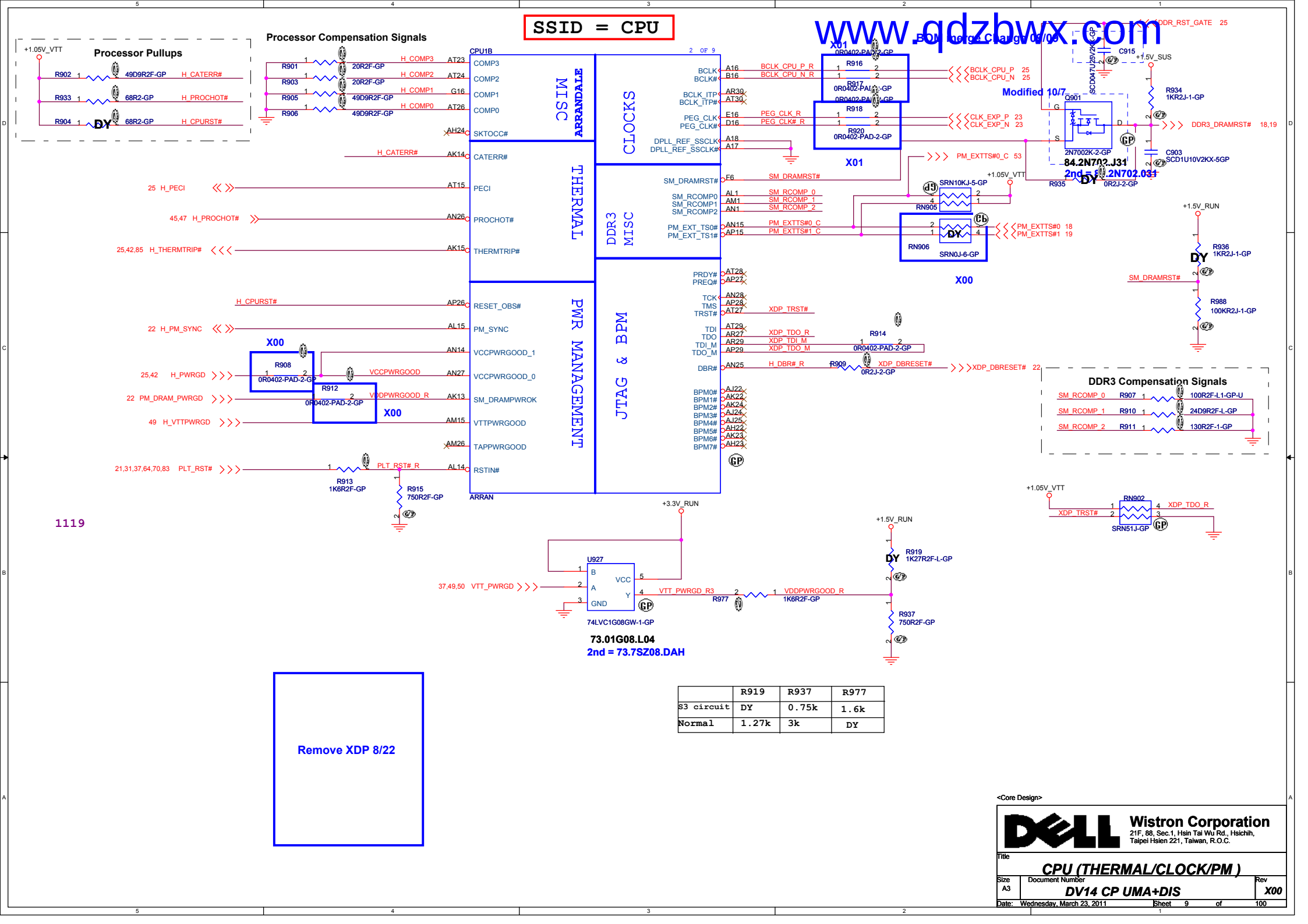


| | R919 | R937 | R977 |
|---|---|---|---|
| S3 circuit | DY | 0.75k | 1.6k |
| Normal | 1.27k | 3k | DY |

SSID = CPU



CPU1C

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DDR SYSTEM MEMORY A

ARRAN

18 M_A_DQ[63..0]

M_A_DQ0 A10 SA_DQ0
M_A_DQ1 C10 SA_DQ1
M_A_DQ2 C7 SA_DQ2
M_A_DQ3 A7 SA_DQ3
M_A_DQ4 B10 SA_DQ4
M_A_DQ5 D10 SA_DQ5
M_A_DQ6 E10 SA_DQ6
M_A_DQ7 A8 SA_DQ7
M_A_DQ8 D8 SA_DQ8
M_A_DQ9 F10 SA_DQ9
M_A_DQ10 E6 SA_DQ10
M_A_DQ11 F7 SA_DQ11
M_A_DQ12 E9 SA_DQ12
M_A_DQ13 B7 SA_DQ13
M_A_DQ14 E7 SA_DQ14
M_A_DQ15 C6 SA_DQ15
M_A_DQ16 H10 SA_DQ16
M_A_DQ17 G8 SA_DQ17
M_A_DQ18 K7 SA_DQ18
M_A_DQ19 J8 SA_DQ19
M_A_DQ20 G7 SA_DQ20
M_A_DQ21 G10 SA_DQ21
M_A_DQ22 J7 SA_DQ22
M_A_DQ23 J10 SA_DQ23
M_A_DQ24 L7 SA_DQ24
M_A_DQ25 M6 SA_DQ25
M_A_DQ26 M8 SA_DQ26
M_A_DQ27 L9 SA_DQ27
M_A_DQ28 L6 SA_DQ28
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M_A_DQ45 AL7 SA_DQ45
M_A_DQ46 AK11 SA_DQ46
M_A_DQ47 AL8 SA_DQ47
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M_A_DQ56 AM12 SA_DQ56
M_A_DQ57 AN12 SA_DQ57
M_A_DQ58 AM13 SA_DQ58
M_A_DQ59 AT14 SA_DQ59
M_A_DQ60 AT12 SA_DQ60
M_A_DQ61 AL13 SA_DQ61
M_A_DQ62 AR14 SA_DQ62
M_A_DQ63 AP14 SA_DQ63

18 M_A_BS0 AC3 SA_BS0
18 M_A_BS1 AB2 SA_BS1
18 M_A_BS2 U7 SA_BS2

18 M_A_CAS# AE1 SA_CAS#
18 M_A_RAS# AB3 SA_RAS#
18 M_A_WE# AE9 SA_WE#

SA_CK0 AA6 M_CLK_DDR0 18
SA_CK0# AA7 M_CLK_DDR#0 18
SA_CKE0 P7 M_CKE0 18

SA_CK1 Y6 M_CLK_DDR1 18
SA_CK1# Y5 M_CLK_DDR#1 18
SA_CKE1 P6 M_CKE1 18

SA_CS0# AE2 M_CS#0 18
SA_CS1# AE8 M_CS#1 18

SA_ODT0 AD8 M_ODT0 18
SA_ODT1 AF9 M_ODT1 18

SA_DM0 B9 M_A_DM0
SA_DM1 D7 M_A_DM1
SA_DM2 H7 M_A_DM2
SA_DM3 M7 M_A_DM3
SA_DM4 AG6 M_A_DM4
SA_DM5 AM7 M_A_DM5
SA_DM6 AN10 M_A_DM6
SA_DM7 AN13 M_A_DM7

M_A_DM[7..0] 18
M_A_DQS#[7..0] 18
M_A_DQS[7..0] 18
M_A_A[15..0] 18

SA_DQS0# C9 M_A_DQS#0
SA_DQS1# F8 M_A_DQS#1
SA_DQS2# J9 M_A_DQS#2
SA_DQS3# N9 M_A_DQS#3
SA_DQS4# AH7 M_A_DQS#4
SA_DQS5# AK9 M_A_DQS#5
SA_DQS6# AP11 M_A_DQS#6
SA_DQS7# AT13 M_A_DQS#7

SA_DQS0 C8 M_A_DQS0
SA_DQS1 F9 M_A_DQS1
SA_DQS2 H9 M_A_DQS2
SA_DQS3 M9 M_A_DQS3
SA_DQS4 AH8 M_A_DQS4
SA_DQS5 AK10 M_A_DQS5
SA_DQS6 AN11 M_A_DQS6
SA_DQS7 AR13 M_A_DQS7

SA_MA0 Y3 M_A_A0
SA_MA1 W1 M_A_A1
SA_MA2 AA8 M_A_A2
SA_MA3 AA3 M_A_A3
SA_MA4 V1 M_A_A4
SA_MA5 AA9 M_A_A5
SA_MA6 V8 M_A_A6
SA_MA7 T1 M_A_A7
SA_MA8 Y9 M_A_A8
SA_MA9 U6 M_A_A9
SA_MA10 AD4 M_A_A10
SA_MA11 T2 M_A_A11
SA_MA12 U3 M_A_A12
SA_MA13 AG8 M_A_A13
SA_MA14 T3 M_A_A14
SA_MA15 V9 M_A_A15

GP

19 M_B_DQ[63..0]

M_B_DQ0 B5 SB_DQ0
M_B_DQ1 A5 SB_DQ1
M_B_DQ2 C3 SB_DQ2
M_B_DQ3 B3 SB_DQ3
M_B_DQ4 E4 SB_DQ4
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M_B_DQ59 AT9 SB_DQ59
M_B_DQ60 AT7 SB_DQ60
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M_B_DQ62 AR10 SB_DQ62
M_B_DQ63 AT10 SB_DQ63

19 M_B_BS0 AB1 SB_BS0
19 M_B_BS1 W5 SB_BS1
19 M_B_BS2 R7 SB_BS2

19 M_B_CAS# AC5 SB_CAS#
19 M_B_RAS# Y7 SB_RAS#
19 M_B_WE# AC6 SB_WE#

CPU1D

ARRANDALE

DDR SYSTEM MEMORY - B

ARRAN

SB_CK0 W8 M_CLK_DDR2 19
SB_CK0# W9 M_CLK_DDR#2 19
SB_CKE0 M3 M_CKE2 19

SB_CK1 V7 M_CLK_DDR3 19
SB_CK1# V6 M_CLK_DDR#3 19
SB_CKE1 M2 M_CKE3 19

SB_CS0# AB8 M_CS#2 19
SB_CS1# AD6 M_CS#3 19

SB_ODT0 AC7 M_ODT2 19
SB_ODT1 AD1 M_ODT3 19

SB_DM0 D4 M_B_DM0
SB_DM1 E1 M_B_DM1
SB_DM2 H3 M_B_DM2
SB_DM3 K1 M_B_DM3
SB_DM4 AH1 M_B_DM4
SB_DM5 AL2 M_B_DM5
SB_DM6 AR4 M_B_DM6
SB_DM7 AT8 M_B_DM7

M_B_DM[7..0] 19
M_B_DQS#[7..0] 19
M_B_DQS[7..0] 19
M_B_A[15..0] 19

SB_DQS0# D5 M_B_DQS#0
SB_DQS1# F4 M_B_DQS#1
SB_DQS2# J4 M_B_DQS#2
SB_DQS3# L4 M_B_DQS#3
SB_DQS4# AH2 M_B_DQS#4
SB_DQS5# AL4 M_B_DQS#5
SB_DQS6# AR5 M_B_DQS#6
SB_DQS7# AR8 M_B_DQS#7

SB_DQS0 C5 M_B_DQS0
SB_DQS1 E3 M_B_DQS1
SB_DQS2 H4 M_B_DQS2
SB_DQS3 M5 M_B_DQS3
SB_DQS4 AG2 M_B_DQS4
SB_DQS5 AL5 M_B_DQS5
SB_DQS6 AP5 M_B_DQS6
SB_DQS7 AR7 M_B_DQS7

SB_MA0 U5 M_B_A0
SB_MA1 V2 M_B_A1
SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
SB_MA4 R1 M_B_A4
SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
SB_MA7 R6 M_B_A7
SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AF7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15

GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

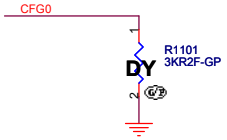
Title: CPU (DDR)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

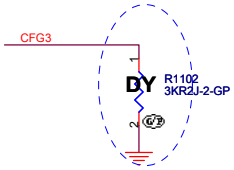
Date: Wednesday, March 23, 2011 | Sheet 10 of 100

SSID = CPU



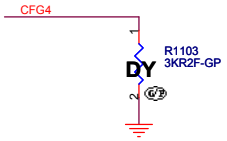



| PCI-Express Configuration Select | |
|---|---|
| CFG0 | 1:Single PEG<br>0:Bifurcation enabled |

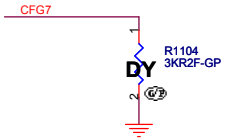



Change to Normal operation
20100202

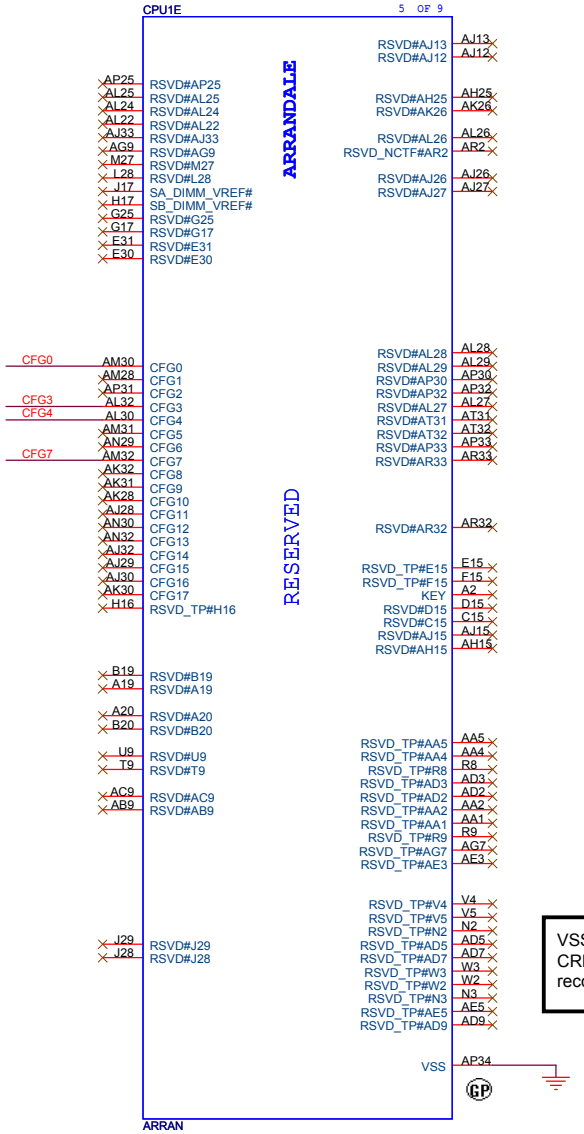
| CFG3 - PCI-Express Static Lane Reversal | |
|---|---|
| CFG3 | 1 :Normal Operation<br>0 :Lane Numbers Reversed<br>15 -> 0, 14 -> 1, ... |




| CFG4 - Display Port Presence | |
|---|---|
| CFG4 | 1:Disabled; No Physical Display Port attached to Embedded Display Port<br>0:Enabled; An external Display Port device is connected to the Embedded Display Port |




| CFG7(Reserved) - Temporarily used for early Clarksfield samples. | |
|---|---|
| CFG7 | Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.<br><br>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].<br>For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality. |




VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RESERVED)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Monday, March 07, 2011 | Sheet 11 of 100

SSID = CPU



PROCESSOR CORE POWER

48A

+VCC_CORE

CPU1F

6 OF 9

ARRANDALE

CPU CORE SUPPLY

1.1V RAIL POWER

Merge bom 09/10

Delete 14 pcs 10U caps 9/9

Simulation 10/07

Modified 09/09

Simulation 10/07

+1.05V_VTT

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

POWER

CPU VIDS

PSI# AN33 — PSI# 47

VID0 AK35 H_VID0
VID1 AK33 H_VID1
VID2 AK34 H_VID2
VID3 AL35 H_VID3
VID4 AL33 H_VID4
VID5 AM33 H_VID5
VID6 AM35 H_VID6

H_VID[6..0] 47

PROC_DPRSLPVR AM34 — PM_DPRSLPVR 47

VTT_SELECT G15 H_VTTVID1 — TP1201TPAD14-GP

H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

SENSE LINES

ISENSE AN35 — IMVP_IMON 47

VCC_SENSE AJ34 — VCC_SENSE 47
VSS_SENSE AJ35 — VSS_SENSE 47

VTT_SENSE B15 — VTT_SENSE 49
VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT — TP1202TPAD14-GP

R1201 100R2F-L1-GP-U

R1204 100R2F-L1-GP-U

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | CPU (VCC_CORE) | |
| Size: Custom | Document Number: DV14 CP UMA+DIS | Rev: X00 |
| Date: Wednesday, March 23, 2011 | Sheet 12 of 100 | |

SSID = CPU



425302_425302_Calpella_S3PowerReduction_WhitePape

Revision 0.7

+CPU_GFX_CORE

22A

Please note that the VTT Rail Values are: Auburndale VTT=1.05V Clarksfield VTT=1.1V

CPU1G

7 OF 9

ARRANDALE

POWER

GRAPHICS

SENSE LINES

GRAPHICS VIDs

DDR3 - 1.5V RAILS

1.1V

1.8V

FDI

PEG & DMI

ARRAN

VAXG_SENSE
VSSAXG_SENSE

VCC_AXG_SENSE 53
VSS_AXG_SENSE 53

GFX_VID0
GFX_VID1
GFX_VID2
GFX_VID3
GFX_VID4
GFX_VID5
GFX_VID6

GFX_VR_EN
GFX_DPRSLPVR
GFX_IMON

R1305 4K7R2J-2-GP

R1304 DY 0R2J-2-GP

Simulation 10/07

3A

+1.5V_RUN

Delete 330U cap 09/09

+1.05V_VTT

18A

1.35A

+1.8V_RUN

BOM merge Change 09/09

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

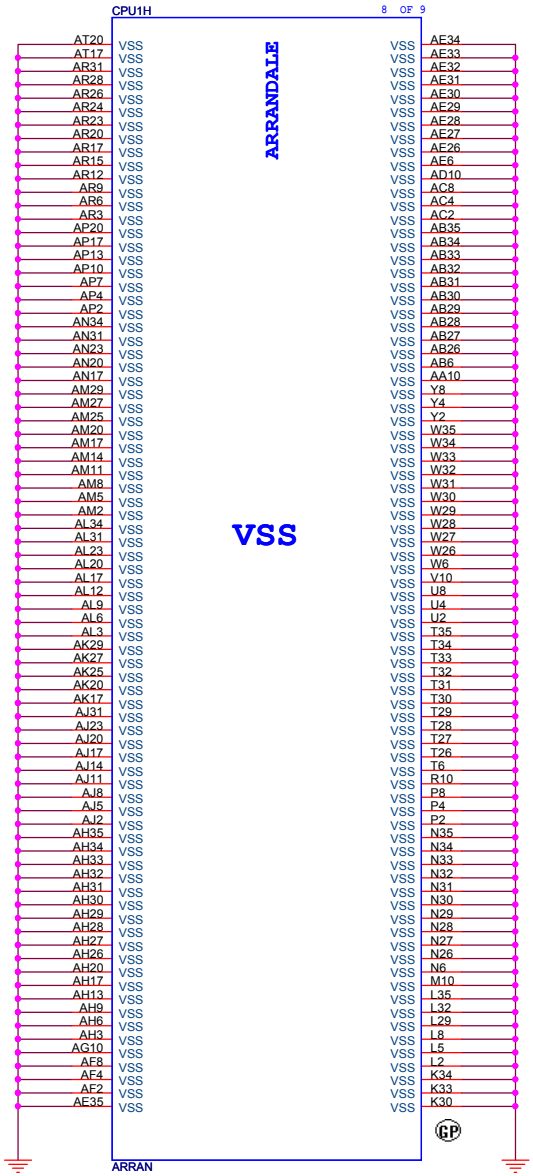
Title: CPU (VCC_GFXCORE)

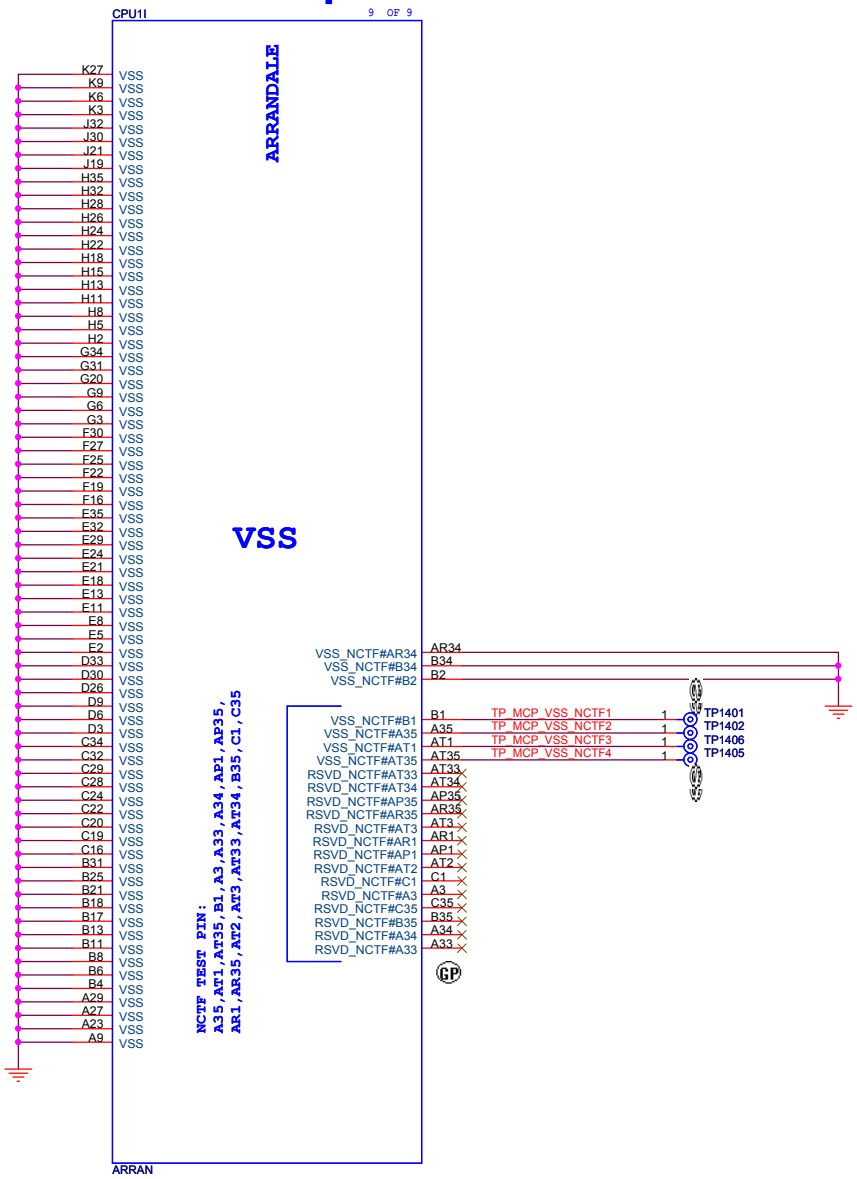
Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 13 of 100

SSID = CPU






<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

Date: Monday, March 07, 2011 Sheet 14 of 100

# (Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | *DV14 CP UMA+DIS* | *X00* |

Date: Thursday, January 06, 2011 Sheet 15 of 100

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | *DV14 CP UMA+DIS* | *X00* |

Date: Thursday, January 06, 2011 Sheet 16 of 100

# (Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | *DV14 CP UMA+DIS* | *X00* |

Date: Thursday, January 06, 2011 Sheet 17 of 100

SSID = MEMORY



DM1

DDR3-204P-128-GP

62.10024.D51

2nd = 62.10024.D91

3rd = 62.10017.Q41

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM A DECOUPLING

Simulation 10/07

Simulation 10/07

Layout Note:
Place these Caps near SO-DIMMA.

Place these caps close to VTT1 and VTT2.

2 S3 Power Reduction

Modified 10/7

84.2N702.J31

2nd = 84.2N702.031

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: C | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 18 of 100

SSID = MEMORY



DM2

DDR3-204P-135-GP

62.10024.E21

2nd = 62.10017.Z81

3rd = 62.10017.P61

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

Note:
If SA0 DIM1 = 0, SA1_DIM1 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

X00 09/23

SODIMM B DECOUPLING

Layout Note:
Place these Caps near
SO-DIMMB.

Simulation 10/07

Place these caps
close to VTT1 and
VTT2.

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from
the Processor than SO-DIMMA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

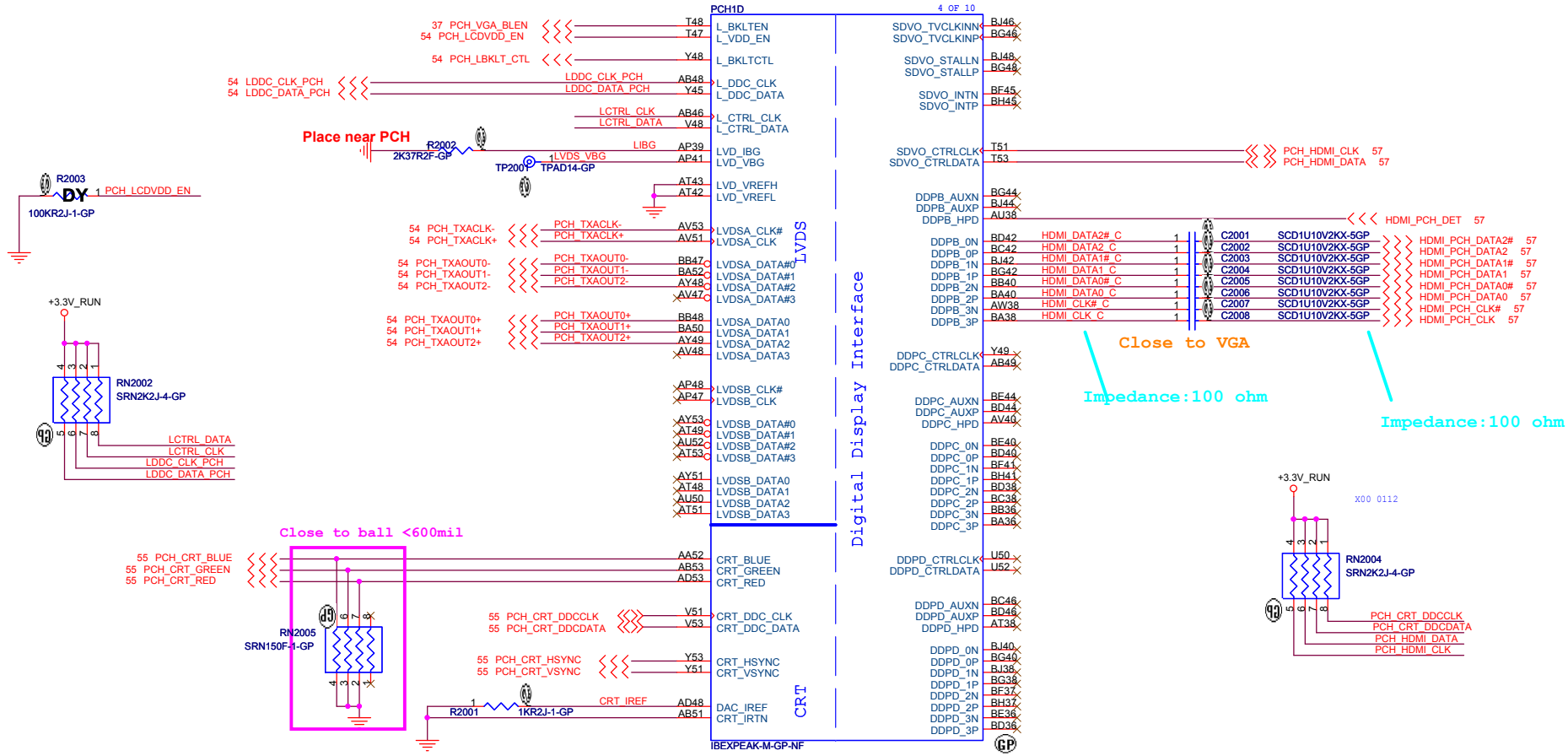
Title: DDR3-SODIMM2

Size | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 19 of 100

SSID = PCH






<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 20 of 100

# SSID = PCH



RN2101
SRN8K2J-2-GP-U
INT_PIRQG#
INT_PIRQC#
INT_PIRQE#
PCI_STOP#
PCI_REQ2#
INT_PIRQD#
PCI_SERR#
PCI_IRDY#
+3.3V_RUN

RN2102
SRN8K2J-2-GP-U
PCI_REQ0#
INT_PIRQB#
INT_PIRQF#
PCI_REQ3#
INT_PIRQH#
PCI_TRDY#
PCI_REQ1#
PCI_FRAME#

RN2103
SRN10KJ-L3-GP
25,37 SIO_EXT_SCI#
25 PCH_GPIO6
25,37 SIO_EXT_WAKE#
SIO_EXT_SCI#
PCH_GPIO6
SIO_EXT_WAKE#
INT_PIRQA#
PCI_DEVSEL#
PCI_PLOCK#
PCI_PERR#

U2101
74LVC1G08GW-GP
73.01G08.L04
2nd = 73.7SZ08.DAH
9,31,37,64,70,83 PLT_RST#
PCI_PLTRST#
R2104 0R0402-PAD-2-GP
C2101 SC220P50V2KX-3GP
X01

PCH1E
IBEXPEAK-M-GP-NF
PCI
NVRAM
USB

Danbury Technology:
Disabled when Low.
Enable when High.

TP2100
TP2101
TP2102
NV_ALE
NV_CLE
NV_RCOMP

| USB | |
|---|---|
| Pair | Device |
| 0 | X |
| 1 | USB1 |
| 2 | USB2 |
| 3 | USB3 |
| 4 | X |
| 5 | X |
| 6 | X |
| 7 | X |
| 8 | X |
| 9 | WLAN for BLUETOOTH |
| 10 | CARD READER |
| 11 | CAMERA |
| 12 | X |
| 13 | X |

0106 change to port 9 from port5

USB_RBIAS_PN
R2106 22D6R2F-L1-GP

| BOOT BIOS Strap | | |
|---|---|---|
| PCI_GNT#1 | PCI_GNT#0 | BOOT BIOS Location |
| 0 | 0 | LPC |
| 0 | 1 | Reserved |
| 1 | 0 | PCI |
| 1 | 1 | SPI(Default) |

| A16 swap override Strap/Top-Block Swap Override jumper | |
|---|---|
| PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled<br>High = Default |

TPAD14-GP TP2116
TPAD14-GP TP2117
TPAD14-GP TP2103
TPAD14-GP TP2108
TPAD14-GP TP2115

70 PCLK_FWH
23 CLK_PCI_FB
37 PCLK_KBC
R2110 22R2J-2-GP
R2108 22R2J-2-GP
R2111 22R2J-2-GP
EC2102 SC10P50V2JN-4GP
EC2103 SC10P50V2JN-4GP
EC2104 SC10P50V2JN-4GP
EMI suggestion 7/27

A00
R2119 10KR2J-3-GP
R2109 4K7R2J-2-GP
PCI_GNT3#
+3.3V_RUN

RN2104
SRN10KJ-L3-GP
SMC_WAKE_SCI#_R
USB_OC#0_1
PCH_GPIO28
USB_OC#2_3
USB_OC#10_11
TPM_ID1
LPD_SPI_INTR#
USB_OC#6_7
+3.3V_ALW

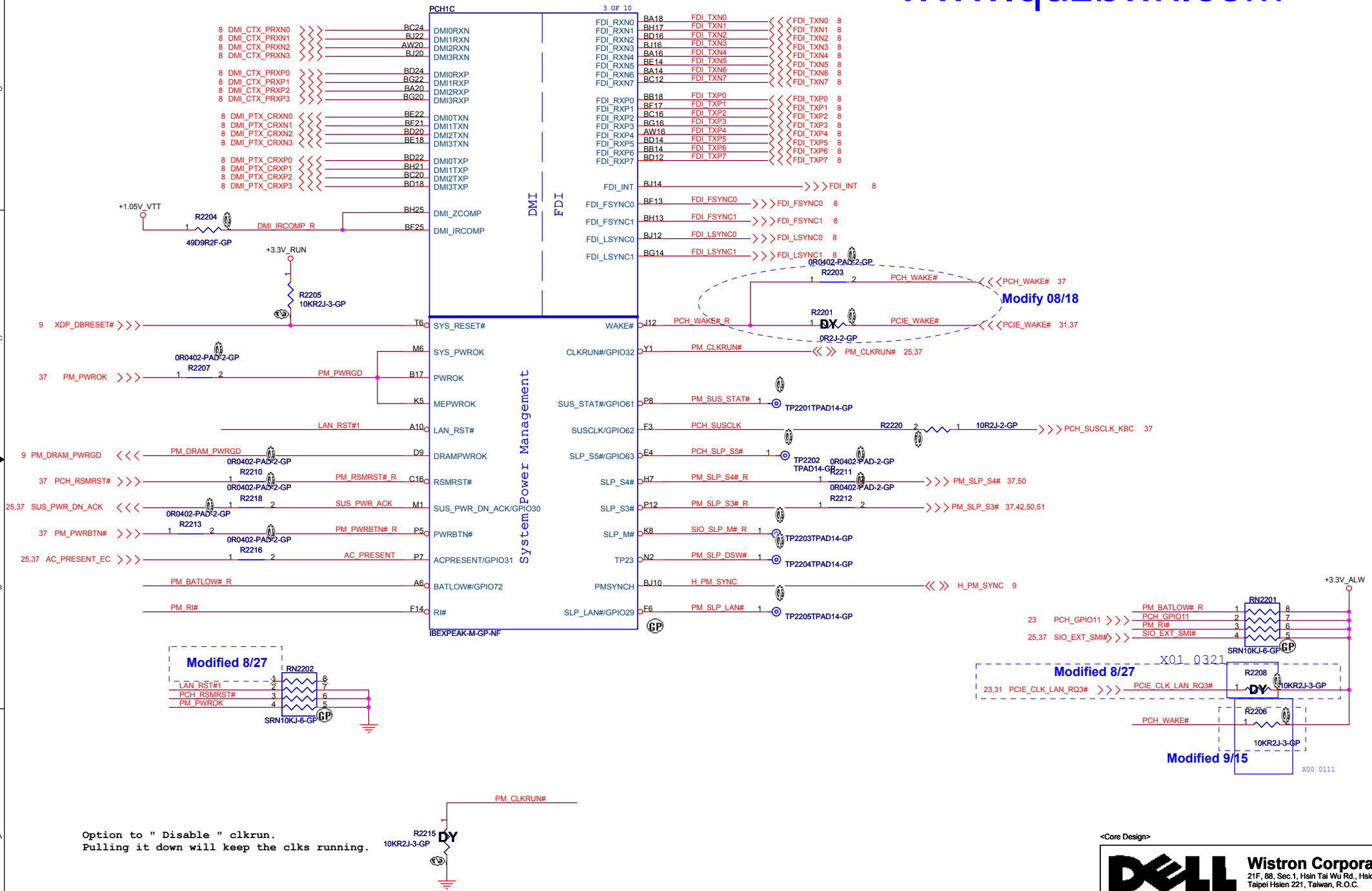
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: A3
Document Number: DV14 CP UMA+DIS
Rev: X00
Date: Wednesday, March 23, 2011
Sheet 21 of 100

SSID = PCH






Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

SSID = PCH



PCH1B

2 OF 10

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

Add serial resistor 8/27

WLAN

LAN

SMBus

PCI-E*

Controller Link

PEG

From CLK BUFFER

Clock Flex

IBEXPEAK-M-GP-NF

X00 2011 0105

Add for GPU 8/10

Modified 1/5

When HDMI parts stuffed, the R2311 need DY.

X02 1118

EMI suggestion 7/27

X01 0228

X01 0315

84.2N702.A3F

2nd = 84.DM601.03F

82.30020.D41

2nd = 82.30020.G71

3rd = 82.30020.G61

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 23 of 100

SSID = RTC

SSID = PCH

Modify 9/29

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

82.30001.A81
2nd = 82.30001.691
3rd = 82.30001.861

X01

EMI suggestion 7/27

NO REBOOT STRAP

| No Reboot Strap R23 | |
|---|---|
| HDA_SPKR | Low = Default<br>High = No Reboot |

PCH1A

HDD

ODD

IBEXPEAK-M-GP-NF

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

Date: Wednesday, March 23, 2011 Sheet 24 of 100

SSID = PCH

X01 0309

+3.3V_RUN

RN2508 SRN10KJ-5-GP

PCH_GPIO22 — INT_SERIRQ 24,37

PCH1F — 6 OF 10

IBEXPEAK-M-GP-NF

Change NET DGPU_HOLD_RST# to PE_GPIO0 to reset GPU ,09/23

C2501 SC47P50V2JN-3GP DY

C2502 SC47P50V2JN-3GP DY

Remove GPIO12,GPIO24 Pull high 09/10

R2519 1KR2J-1-GP

X01 0309

R2508 10KR2J-3-GP UMA

R2507 10KR2J-3-GP DIS

RN2509 SRN100KJ-6-GP

X00 R2518 0R0402-PAD-2-GP

X00 2011 0105 add R2506

R2504 10KR2J-3-GP UMA

R2505 10KR2J-3-GP DY

R2503 10KR2J-3-GP DIS

R2506 10KR2J-3-GP DIS

Add PE_GPIO0 , PE_GPIO1 09/09 , pull high/low check H/L active ?

RN2505 SRN56J-4-GP

Placed Within 2" from PCH

R2516 10KR2J-3-GP DY

R2517 10KR2J-3-GP

HDMI function detect.

| PCH_GPIO45 | 0 | 1 |
|---|---|---|
| HDMI Function | YES | NO |

RN2507 SRN10KJ-L3-GP

RN2506 SRN10KJ-L3-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

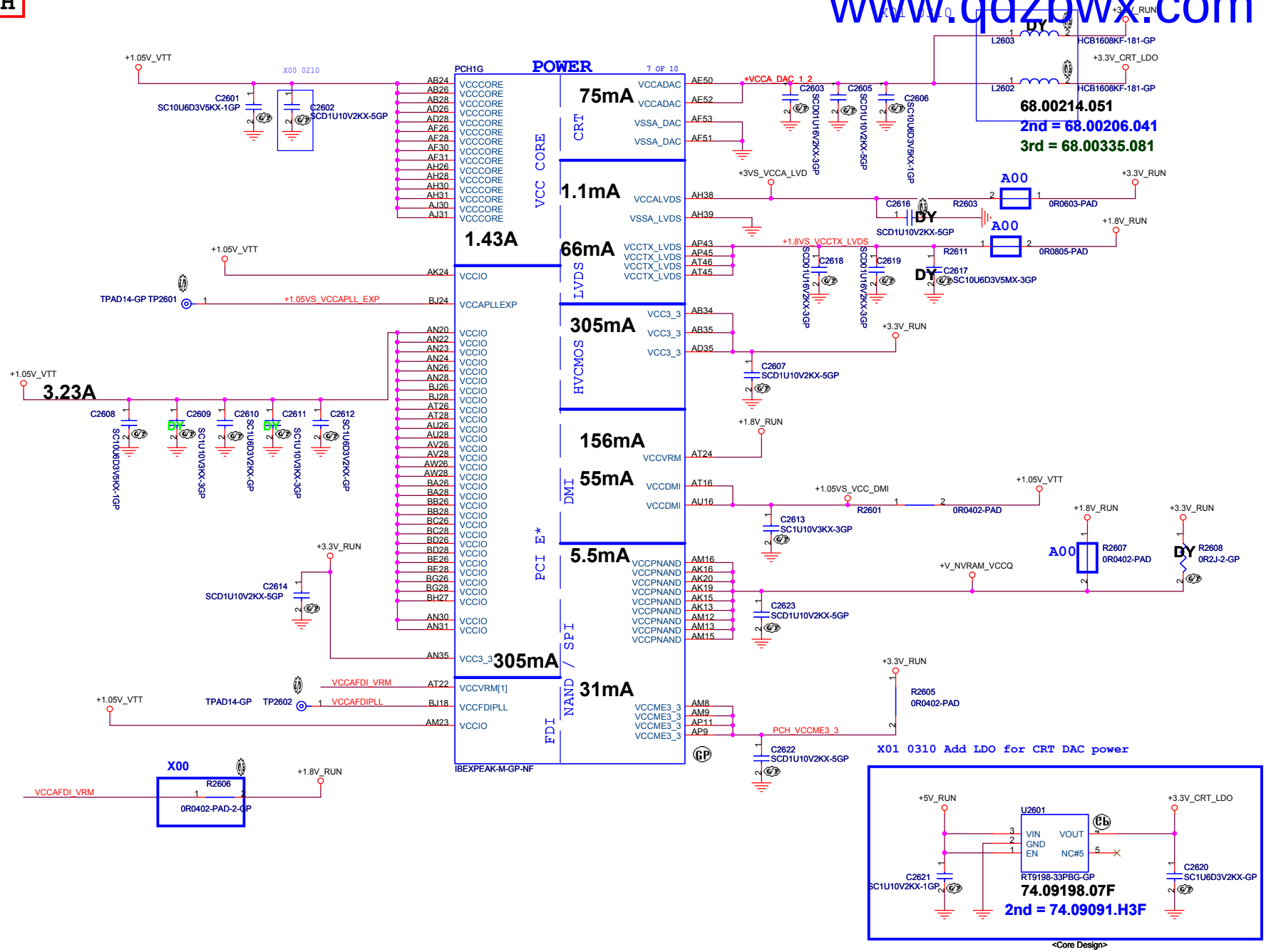
Title: PCH (GPIO/CPU)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 25 of 100

SSID = PCH






<Core Design>

| | | |
|---|---|---|
| Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: PCH (POWER1) | | |
| Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00 |
| Date: Tuesday, March 22, 2011 | Sheet 26 of 100 | |

SSID = PCH

PCH1J

POWER

10 OF 10

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

CPU

RTC

HDA

IBEXPEAK-M-GP-NF

TPAD14-GP TP2515 1VCCACLK

AP51 VCCACLK
AP53 VCCACLK

AF23 VCCLAN
AF24 VCCLAN

DCPSUSBYP Y20 DCPSUSBYP

C2707 SCD1U10V2KX-5GP

AD38 VCCME
AD39 VCCME
AD41 VCCME
AF43 VCCME
AF41 VCCME
AF42 VCCME
V39 VCCME
V41 VCCME
V42 VCCME
Y39 VCCME
Y41 VCCME
Y42 VCCME

+1.05V_VTT

1.2A

C2704 SC10U6D3V5KX-1GP
C2705 DY SC10U6D3V5MX-3GP
C2708 SC1U6D3V2KX-GP

Simulation 10/07

C2710 DY SCD1U10V2KX-5GP

+VCCRTCEXT V9 DCPRTC

C2713 SCD1U10V2KX-5GP

+1.8V_RUN AU24 VCCVRM

L2702 SC10U6D3V5MX-3GP
IND-10UH-218-GP
68.10050.10Y
2nd = 68.1001E.10N
+1.05VS_VCCA_A_DPL
C2734 DY
C2711 SC1U6D3V2KX-GP

L2703 IND-10UH-218-GP
68.10050.10Y
2nd = 68.1001E.10N
+1.05VS_VCCA_B_DPL
C2735 DY SC10U6D3V5MX-3GP
C2714 SC1U6D3V2KX-GP

88mA +1.05VS_VCCA_A_DPL BB51 VCCADPLLA BB53 VCCADPLLA

88mA +1.05VS_VCCA_B_DPL BD51 VCCADPLLB BD53 VCCADPLLB

Isolate the power supply for pin AF34,AH34,AF32 these pins can be shorted together . NOT with AH35,AJ35

X00 09/23

+1.05V_VTT
C2719 SC1U6D3V2KX-GP
C2720 SC1U6D3V2KX-GP
C2718 SC1U6D3V2KX-GP

AH23 VCCIO
AJ35 VCCIO
AH35 VCCIO
AF34 VCCIO
AH34 VCCIO
AF32 VCCIO

V12 DCPSST

+VCCSST
C2723 SCD1U10V2KX-5GP
C2724 SCD1U10V2KX-5GP

+1.05VALW_INT_VCCSUS Y22 DCPSUS

+3.3V_ALW
133mA
C2726 SCD1U10V2KX-5GP

P18 VCCSUS3_3
U19 VCCSUS3_3
U20 VCCSUS3_3
U22 VCCSUS3_3

+3.3V_RUN
C2727 SCD1U10V2KX-5GP

V15 VCC3_3
V16 VCC3_3
Y16 VCC3_3

+1.05V_VTT
1mA
Simulation 10/07
X00 0210
C2728 SC10U6D3V5KX-1GP
C2729 SCD1U10V2KX-5GP
C2730 SC1U6D3V2KX-GP

AT18 V_CPU_IO
AU18 V_CPU_IO

+RTC_CELL
6mA
C2732 SCD1U10V2KX-5GP
C2733 SCD1U10V2KX-5GP

A12 VCCRTC

VCCIO V24
VCCIO V26
VCCIO Y24
VCCIO Y26

DY C2706 SC1U6D3V2KX-GP

+3.3V_ALW

VCCSUS3_3 V28
VCCSUS3_3 U28
VCCSUS3_3 U26
VCCSUS3_3 U24
VCCSUS3_3 P28
VCCSUS3_3 P26
VCCSUS3_3 N28
VCCSUS3_3 N26
VCCSUS3_3 M28
VCCSUS3_3 M26
VCCSUS3_3 L28
VCCSUS3_3 L26
VCCSUS3_3 J28
VCCSUS3_3 J26
VCCSUS3_3 H28
VCCSUS3_3 H26
VCCSUS3_3 G28
VCCSUS3_3 G26
VCCSUS3_3 F28
VCCSUS3_3 F26
VCCSUS3_3 E28
VCCSUS3_3 E26
VCCSUS3_3 C28
VCCSUS3_3 C26
VCCSUS3_3 B27
VCCSUS3_3 A28
VCCSUS3_3 A26

C2703 SCD1U10V2KX-5GP

+3.3V_ALW
C2709 SCD1U10V2KX-5GP

VCCSUS3_3 U23
VCCIO V23

+1.05V_VTT

V5REF_SUS F24 +5VALW_PCH_VCC5REFSUS

1mA

83.R0304.A8F
2nd = 83.R2004.B8F
D2701 CH751H-40PT-GP

+5V_ALW
R2701 100R2F-L1-GP-U

C2712 SC1U6D3V2KX-GP

V5REF K49 +5VS_PCH_VCC5REF

1mA

83.R0304.A8F
2nd = 83.R2004.B8F
D2702 CH751H-40PT-GP

+3.3V_RUN
+5V_RUN
R2702 100R2F-L1-GP-U

C2715 SC1U6D3V2KX-GP

VCC3_3 J38
VCC3_3 L38
VCC3_3 M36
VCC3_3 N36
VCC3_3 P36
VCC3_3 U35

+3.3V_RUN
C2716 SCD1U10V2KX-5GP

VCC3_3 AD13

+3.3V_RUN
C2717 SCD1U10V2KX-5GP

VCCSATAPLL AK3
VCCSATAPLL AK1

VCCSATAPLL 1 TP2514 TPAD14-GP

VCCIO AH22
VCCVRM AT20

+1.05V_VTT
+1.8V_RUN
C2725 SC1U6D3V2KX-GP

VCCIO AH19
VCCIO AD20
VCCIO AF22

VCCIO AD19
VCCIO AF20
VCCIO AF19
VCCIO AH20

VCCIO AB19
VCCIO AB20
VCCIO AB22
VCCIO AD22

+1.05V_VTT

VCCME AA34
VCCME Y34
VCCME Y35
VCCME AA35

VCCSUSHDA L30

1mA

R2707 2 0R0402-PAD +3.3V_ALW

C2731 SC1U6D3V2KX-GP

+3VS_+1.5VS_HDA_IO

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

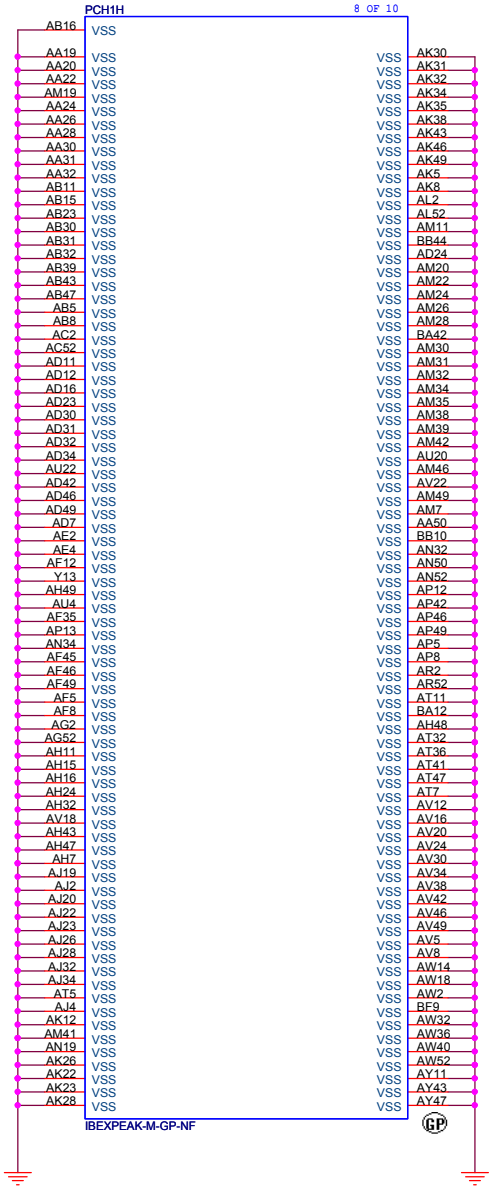
Title: PCH (POWER2)

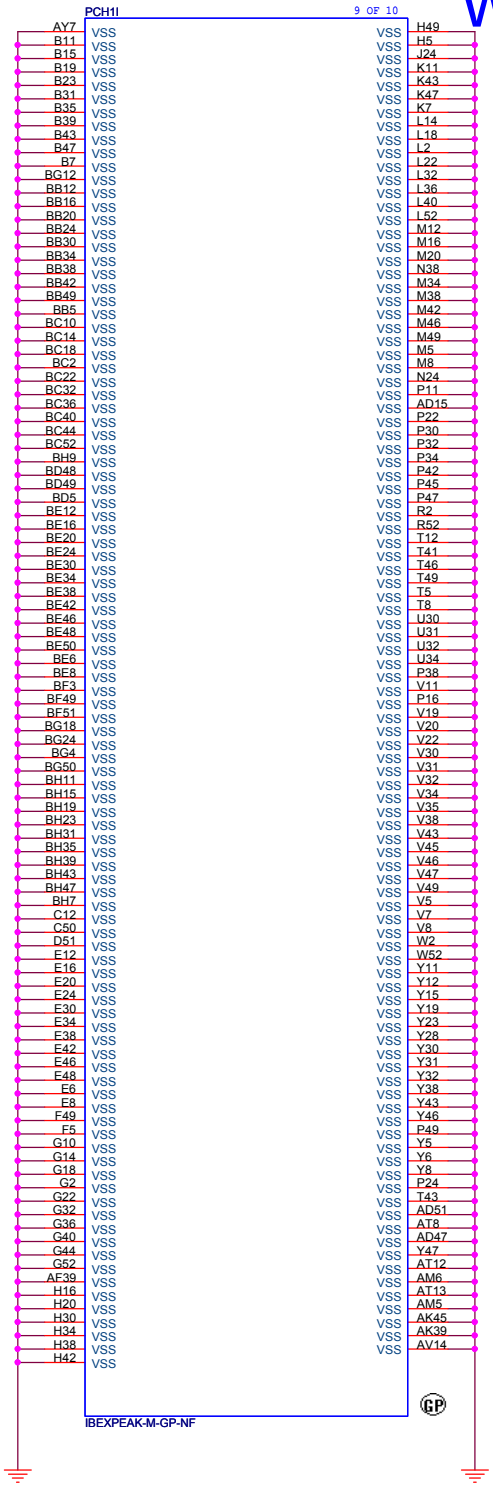
Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Tuesday, March 22, 2011 | Sheet 27 of 100

SSID = PCH






<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Tuesday, January 25, 2011 | Sheet 28 of 100

SSID = AUDIO



Close to codec

0625 Modify:
AUD_DMIC_CLK&AUD_DMIC_IN0 connector
to LVDS pin define.

0707 Modify:
updated U2901 part number from data base.

2010/06/30 Change to 92HD87 (71.92H87.A03)

CLOSE TO CODEC

Put C2921 and C2922 close to codec

0707 Modify:
Change R2911,R2914,R2917 change
to 0ohm 0603 from short pad.

0809 Vendor recommand

0730 Add internal MIC

From SB

From EC

AUD_PC_BEEP
Trace width>15 mils

0719 Modify:
Move RN2901 to closed AUDIO CODEC from speaker connector.

MIC IN

Azalia I/F EMI

X00 20101230 C2919 change to 0402

Close to Pin13

Close to Pin14

<Core Design>

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Title: Audio Codec 92HD87B1

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 29 of 100

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<Core Design>

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Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | *DV14 CP UMA+DIS* | *X00* |

Date: Thursday, January 06, 2011 Sheet 30 of 100

SSID = LOM

# LAN CHIP



Modified 0328

X01 0315

+3.3V_LAN

R3102 10KR2J-3-GP DY

R3101 10KR2J-3-GP DY

84.03904.L06

DY 2nd = 84.03904.P11

CLK_LAN_REQ#_R

Q3101 PMBS3904-1-GP

PCIE_CLK_LAN_RQ3# 22,23

R3108 0R2J-2-GP DY

R3122 10KR2J-3-GP DY

X00 09/23

60 mils

X01 0228

L3101 LANOUP_1.05S CTRL10A_R IND-4D7UH-192-GP

C3120 SCD1U16V2ZY-2GP

C3115 SC4D7U6D3V3KX-GP X5R

R3117 0R0603-PAD

R3115 0R0603-PAD

EVDD10

C3106 SC1U10V3ZY-6GP

DVDD10

C3113 C3109 C3114 C3117 C3112 C3123 C3116 SCD1U16V2ZY-2GP

GIGA GIGA GIGA

68.4R750.20C

2nd = 68.4R710.20J

40 mils

+3.3V_LAN

C3118 C3121 C3119 SCD1U16V2ZY-2GP

R3104 0R0603-PAD

AVDD33_REG

C3101 SC4D7U6D3V3KX-GP

C3111 SCD1U16V2ZY-2GP

X5R

U3101 RTL8111E-VB-GP

GND

RSET R3113 2K49R2F-GP

+3.3V_LAN

DVDD10

LANOUT

LANXIN

GPO

AVDD33 AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 AVDD33 DVDD10 LED0 DVDD33 GPO/SMBALERT# LED1/EESK

MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 AVDD10 MDIP2 MDIN2 AVDD10 MDIP3 MDIN3 AVDD33

59 LAN_MDI0P 59 LAN_MDI0N

59 LAN_MDI1P 59 LAN_MDI1N

59 LAN_MDI2P 59 LAN_MDI2N

59 LAN_MDI3P 59 LAN_MDI3N

REGOUT VDDREG VDDREG ENSWREG EEDI/SDA LED3/EEDO EECS/SCL DVDD10 LANWAKE# DVDD33 ISOLATE# PERST#

LANOUP_1.05S AVDD33_REG AVDD33_REG ENSWREG EEDI/SDA

EECS/SCL DVDD10

R3107 10KR2J-3-GP

PCIE_WAKE# 22,37

+3.3V_RUN

+3.3V_LAN ISOLATE#

R3110 1KR2J-1-GP

R3109 15KR2F-GP

PLT_RST# 9,21,37,64,70,83

For Switch Regulator enable

+3.3V_LAN

R3105 0R0402-PAD-2-GP

R3106 0R2J-2-GP DY

DVDD10 SMBCLK SMBDATA CLKREQ# HSIP HSIN REFCLK_P REFCLK_N EVDD10 HSOP HSON GND

TPAD14-GP TP3101 DVDD10

0720

SMBDATA_LAN

CLK_LAN_REQ#_R

PCIE_TXP3

PCIE_TXN3

CLK_PCIE_LAN

CLK_PCIE_LAN#

EVDD10

PCIE_RXP3_C

PCIE_RXN3_C

C3132 SCD1U10V2KX-5GP

R3116 10KR2J-3-GP SMBDATA_LAN

GIGA

+3.3V_LAN

R3103 1KR2J-1-GP GPO

R3114 10KR2J-3-GP EEDI/SDA

X01 0315

LANXOUT

X00 0112

X3101 XTAL-25MHZ-155-GP

LANXIN

C3102 SC18P50V2JN-1-GP

C3103 SC18P50V2JN-1-GP

82.30020.D41

2nd = 82.30020.G71

3rd = 82.30020.G61

C3105 SCD1U10V2KX-5GP

C3104 SCD1U10V2KX-5GP

PCIE_RXP3_C PCIE_RXN3_C

PCIE_RXP3 23 PCIE_RXN3 23

PCIE_TXP3 PCIE_TXN3

PCIE_TXP3 23 PCIE_TXN3 23

CLK_PCIE_LAN 23

CLK_PCIE_LAN# 23

+3.3V_RUN

R3119 0R3J-0-U-GP DY

+3.3V_LAN

X01 0228

R3120 0R3J-0-U-GP DY

84.00102.031

2nd = 84.02301.G31

3rd = 84.21607.031

PA102FMG-GP-U Q3103

Change 09/09

+3.3V_ALW

C3130 SCD1U10V2KX-5GP

R3121 10KR2J-3-GP

R3118 20KR2J-L2-GP

C3127 SC1U6D3V2KX-GP

PM_LAN_ENABLE_R

X01 0316

C3125 SC1U6D3V2KX-GP DY

C3129 C3126 C3128 SCD1U10V2KX-5GP

GIGA

0721

Modified 10/7

37 PM_LAN_ENABLE

Q3102 2N7002K-2-GP

LAN_ENABLE_R_C

84.2N702.J31

2nd = 84.2N702.031

<Core Design>

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN-RTL8111E

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

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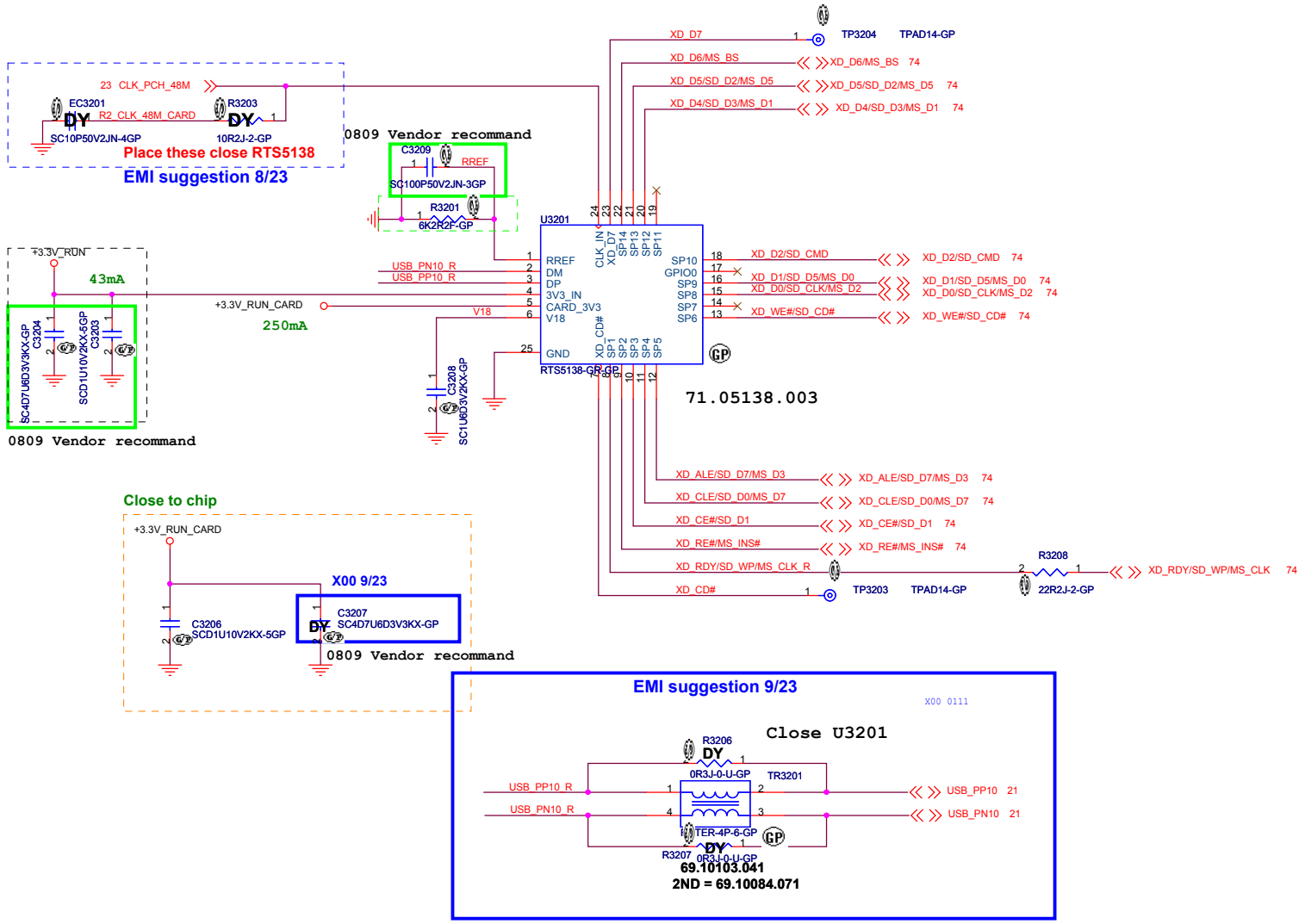
**SSID = SDIO**




<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

Date: Wednesday, March 23, 2011 Sheet 32 of 100

# (Blanking)

<Core Design>

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Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | *DV14 CP UMA+DIS* | *X00* |

Date: Thursday, January 06, 2011 Sheet 33 of 100

(Blanking)

<Core Design>

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Title: Reserved

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

Date: Thursday, January 06, 2011 Sheet 34 of 100

# (Blanking)

<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: *X00*

Date: Thursday, January 06, 2011 | Sheet 35 of 100

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<Core Design>

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Title: *Reserved*

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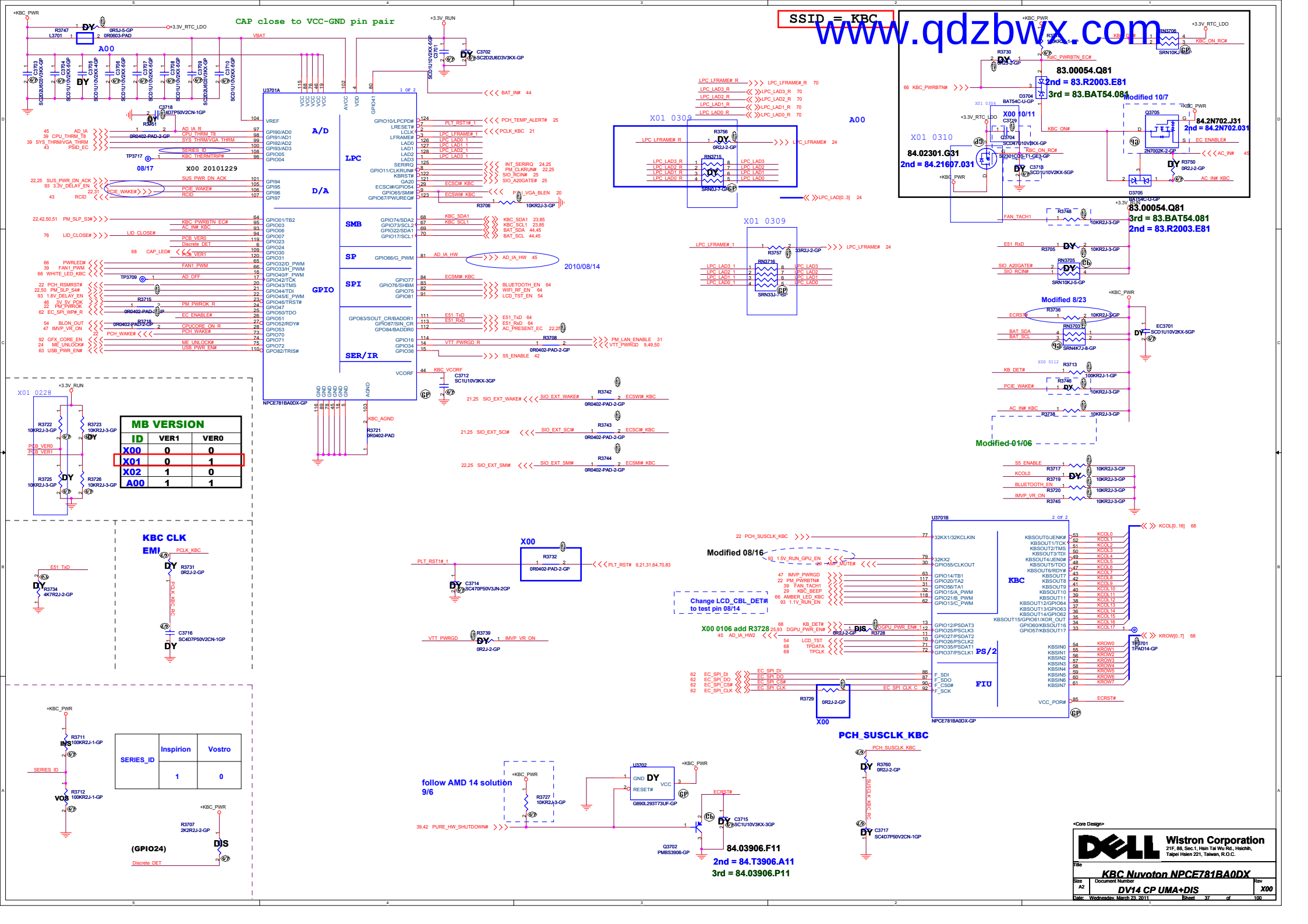
SSID = KBC
www.qdzbwx.com
CAP close to VCC-GND pin pair
MB VERSION
ID | VER1 | VER0
X00 | 0 | 0
X01 | 0 | 1
X02 | 1 | 0
A00 | 1 | 1
KBC CLK EMI
SERIES_ID | Inspirion | Vostro
1 | 0
(GPIO24)
follow AMD 14 solution 9/6
PCH_SUSCLK_KBC
Modified 08/16
Change LCD_CBL_DET# to test pin 08/14
X00 0106 add R3728
Modified 10/7
Modified 8/23
Modified 01/06
2010/08/14
84.02301.G31
2nd = 84.21607.031
83.00054.Q81
2nd = 83.R2003.E81
3rd = 83.BAT54.081
84.2N702.J31
2nd = 84.2N702.031
84.03906.F11
2nd = 84.T3906.A11
3rd = 84.03906.P11
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC Nuvoton NPCE781BA0DX
DV14 CP UMA+DIS
X00
Wednesday, March 23, 2011

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<Core Design>

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Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | *DV14 CP UMA+DIS* | *X00* |

Date: Thursday, January 06, 2011 Sheet 38 of 100

SSID = Thermal

# Thermal sensor P2800

# Fan controller P2793

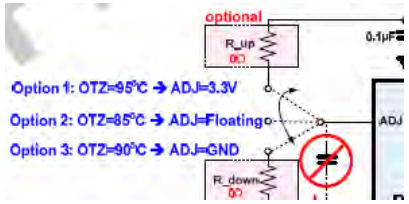
01/05 change R3903&R3904 to 0ohm.Remove C3905

+3.3V_RUN — C3901 SCD1U10V2KX-5GP

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

+3.3V_RUN — R3903 0R2J-2-GP (DY) — ADJ — R3904 0R2J-2-GP (DY)

87.1 Degree




Very Close to CPU1

U3901 P2800EB0-GP

| | | | |
|---|---|---|---|
| 5 | VCC | TDR | 4 |
| 6 | DXP | TDL | 3 |
| 7 | DXN | GND | 2 |
| 8 | OTZ | ADJ | 1 |

P2800_DXP_R
P2800_DXN_R
SYS_THRM/VGA_THRM 37
CPU_THRM_T8 37
ADJ
THERM_SYS_SHDN# — R3911 0R2J-2-GP — T8_P2800

74.02800.B71
1.H/W T8 Shutdown

R(K )= 0.0012*T^2- 0.9308T+ 96.147

X01 0303

37 FAN1_PWM — R3914 4K7R2J-2-GP — FAN1_PWM_R

R3902 DY 0R2J-2-GP — FON# — FAN_VCC — +5V_RUN

U3902 G991P11U-GP

| | | | |
|---|---|---|---|
| 1 | FON# | GND | 8 |
| 2 | VIN | GND | 7 |
| 3 | VO | GND | 6 |
| 4 | VSET | GND | 5 |

C3911 SCD1U10V2KX-5GP

*Layout* 10 mil

For linear FAN

74.00991.031
2nd = 74.02793.A31

+5V_RUN — C3903 SC4D7U6D3V3KX-5GP — C3904 SCD1U10V2KX-5GP

Very close to CPU1

12/15 Remove 3rd source

11/4 Vendor recommand

X01 0309 DY G709 function

+3.3V_RUN — R3913 470KR2J-2-GP (DY)

R3905 150R2J-1-GP (DY) — R3328 0R2J-2-GP (DY)

U3905 G709T1UF-GP

| | | | |
|---|---|---|---|
| SET | | VCC | 5 |
| GND | DY | | |
| OUT# | | HYST | 4 |

ADJ_G709 — G709_VCC — HYST_PH

37 THERM_SYS_SHDN# — R3910 0R2J-2-GP (DY) — T8_G709

R3912 24K3R2F-1-GP (DY)

86.9

C3908 SCD1U10V2KX-5GP (DY)

X01 0311

AFTP2803 — AFTP2802

FAN1

37 FAN_TACH1 — R3907 0R0402-PAD-2-GP — FAN_TACH1_C

*Layout* 15 mil

FAN_VCC

C3909 SC4D7UD3V3KX-GP — D3902 CH551H-30PT-GP — C3910 SC2200P50V2KX-2GP (DY)

AFTP2801

FOX-CON3-6-GP-U
20.D0210.103
2nd = 20.D0246.103
3rd = 20.F1716.003

83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F

R3908 NTC-100K-8-GP (DY) — Q3901 PMBS3904-1-GP — C3906 SC470P50V3JN-2GP

RN3901 SRN0J-6-GP

C3907 SC2200P50V2KX-2GP

P2800_DXP_R
P2800_DXN_R

84.03904.L06
2nd = 84.03904.P11

2.System Sensor, Put on palm rest

Modified 8/27

85 P2800_VGA_DXP — P2800_VGA_DXP

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

85 P2800_VGA_DXN — P2800_VGA_DXN

RN3902 SRN0J-6-GP (DY)

+3.3V_RUN — R3909 100KR2J-1-GP

Q3902 2N7002K-2-GP

37,42 PURE_HW_SHUTDOWN# — THERM_SYS_SHDN# — +3.3V_RUN

C2811 SCD1U10V2KX-GP (DY)

84.2N702.J31
2ND = 84.2N702.031

## EMI/ESD

FAN_VCC — EC3901 SCD1U16V2KX-3GP (DY)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793
Size: A3 | Document Number: Enrico Caruso 14 | Rev: X00
Date: Wednesday, March 23, 2011 | Sheet 39 of 100

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<Core Design>

Wistron Corporation
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Title: *Reserved*

| Size | Document Number | Rev |
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| A3 | *DV14 CP UMA+DIS* | *X00* |

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(Blanking)

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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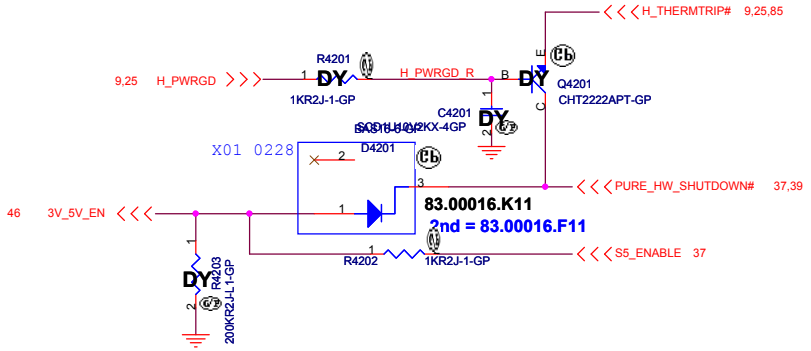
Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | *DV14 CP UMA+DIS* | *X00* |

Date: Thursday, January 06, 2011 Sheet 41 of 100

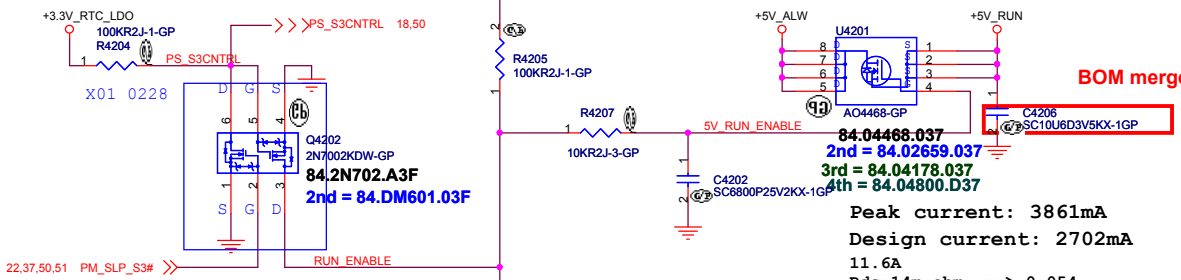
SSID = Reset.Suspend





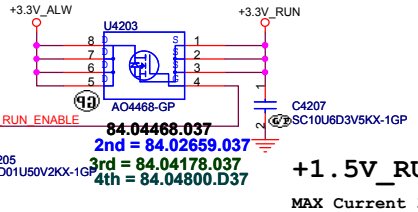

# Run Power

Peak current: 6370mA ( HD:1100 ODD:2500 )
Design current: 4459 mA
11.6A
Rds=14m ohm ==> 0.09V




BOM merge 10/04

Peak current: 3861mA
Design current: 2702mA
11.6A
Rds=14m ohm ==> 0.054



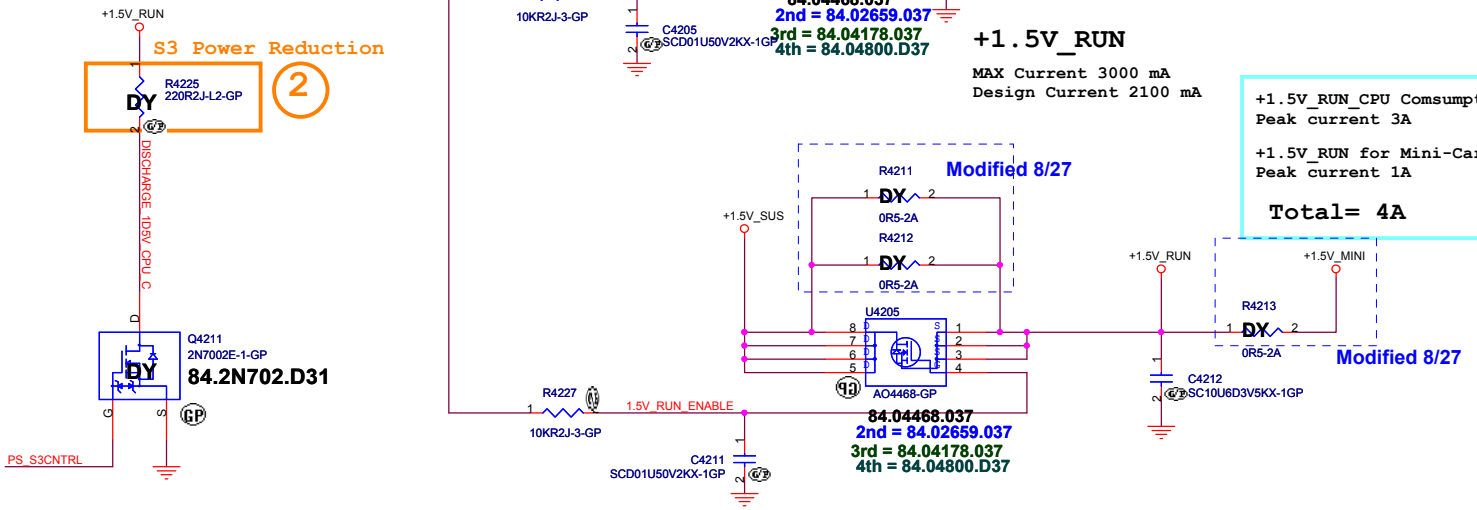

## +1.5V_RUN

MAX Current 3000 mA
Design Current 2100 mA

+1.5V_RUN_CPU Comsumption
Peak current 3A

+1.5V_RUN for Mini-Card Comsumption
Peak current 1A

Total= 4A




<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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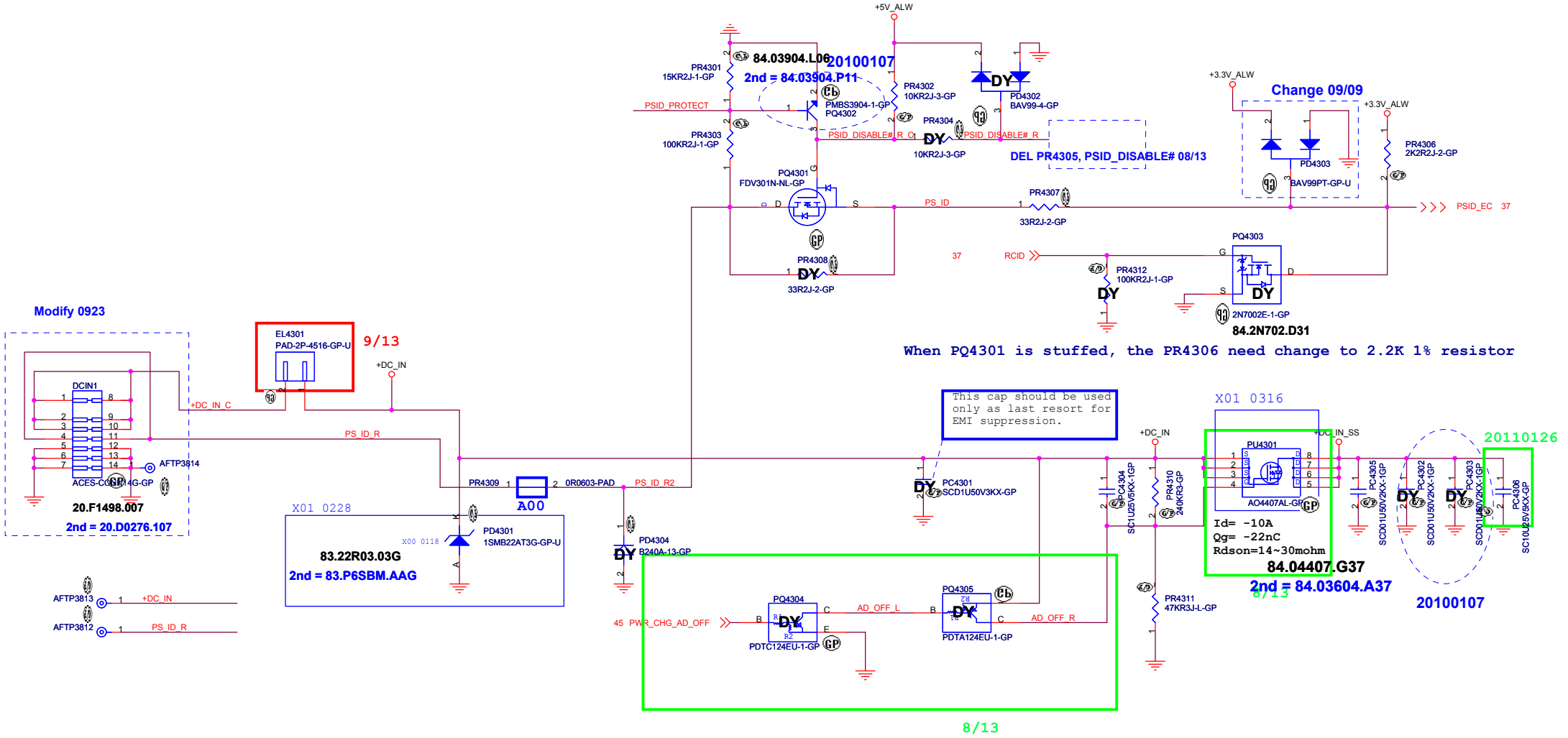
Title: Power Plane Enable

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

Date: Wednesday, March 23, 2011 Sheet 42 of 100

SSID = PWR.Support

# DCin CONN



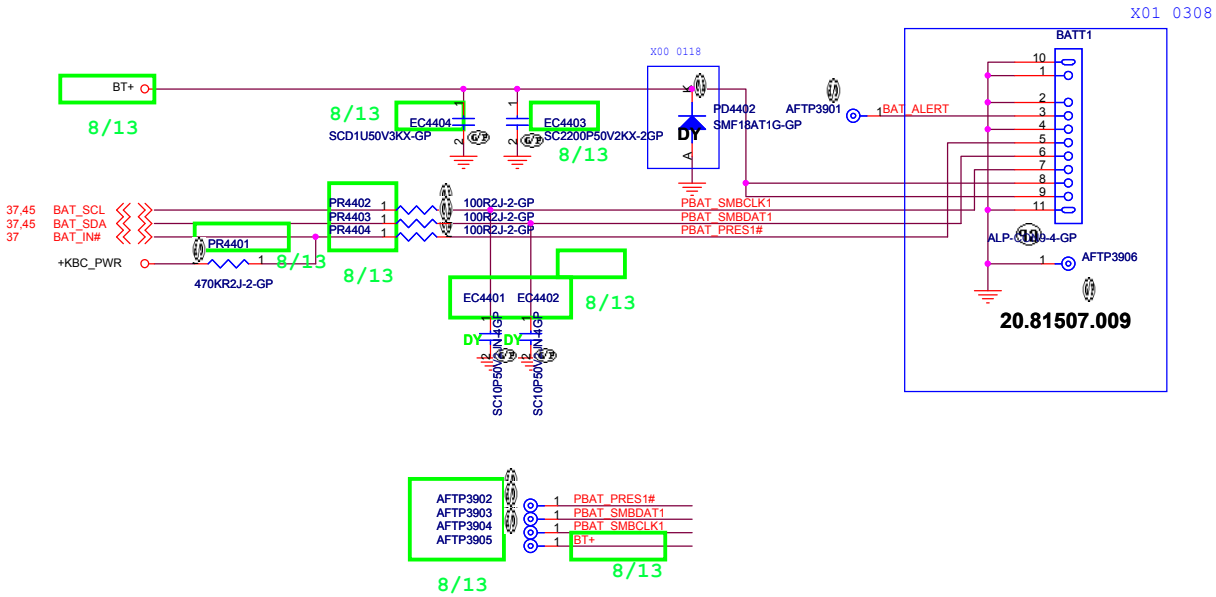

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

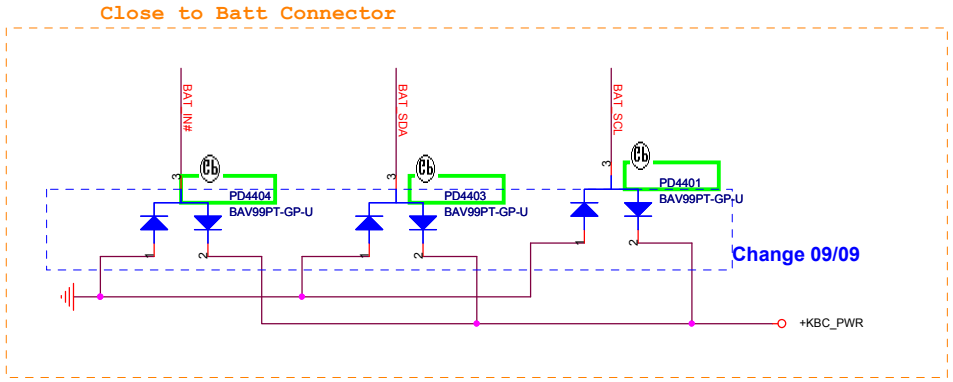
| | | |
|---|---|---|
| Title | DCIN Jack | |
| Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00 |
| Date: Wednesday, March 23, 2011 | Sheet 43 of 100 | |

SSID = PWR.Support

# Batt Connecter




For actual location, need to be swap all pin



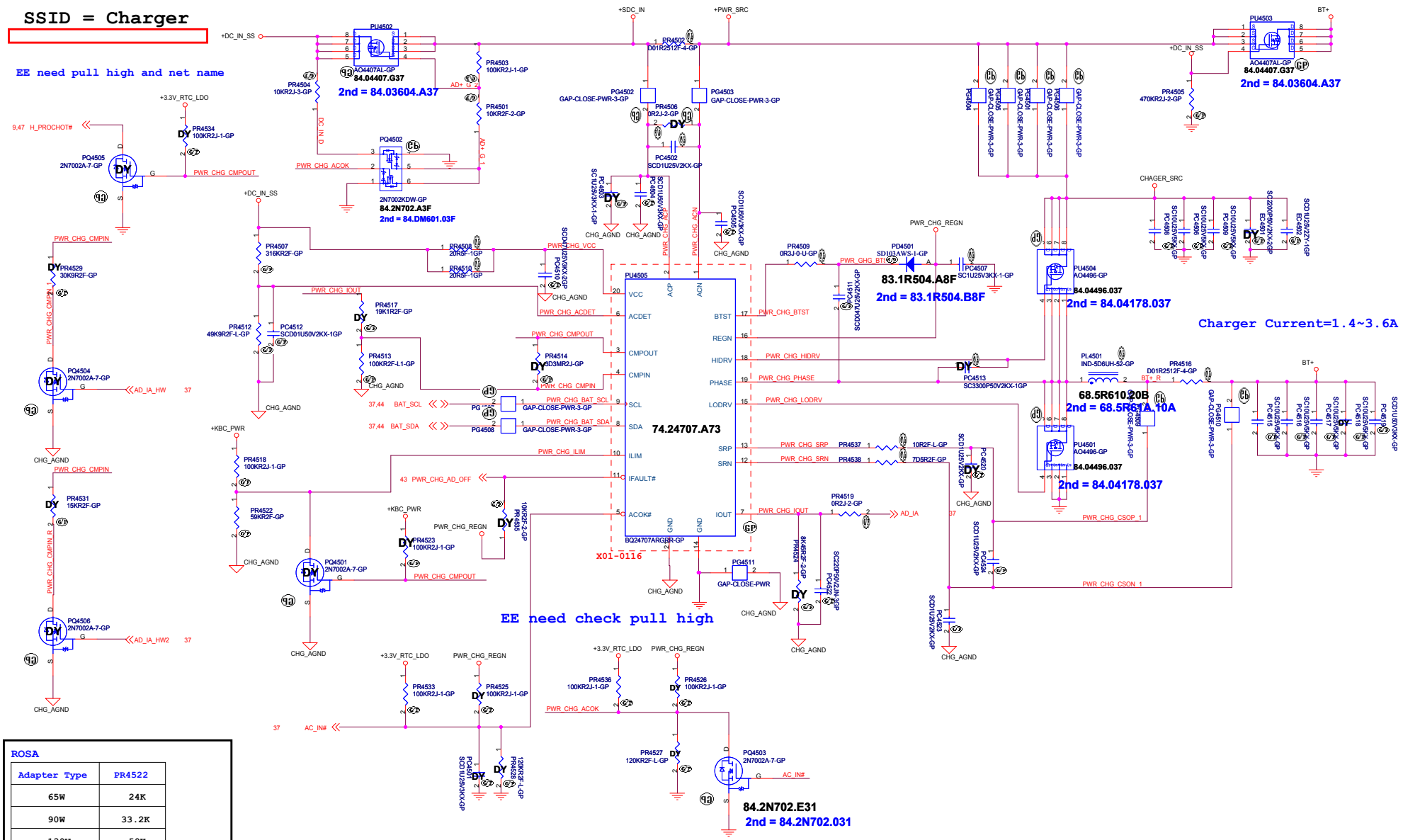

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 44 of 100




**ROSA**

| Adapter Type | PR4522 |
|---|---|
| 65W | 24K |
| 90W | 33.2K |
| 130W | 59K |

**EC code only BQ24707**

| H_PROCHOT# | AD_IA_HW | AD_IA_HW2 |
|---|---|---|
| 65W | 0 | 0 |
| 90W | 1 | 0 |
| 130W | 0 | 1 |

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

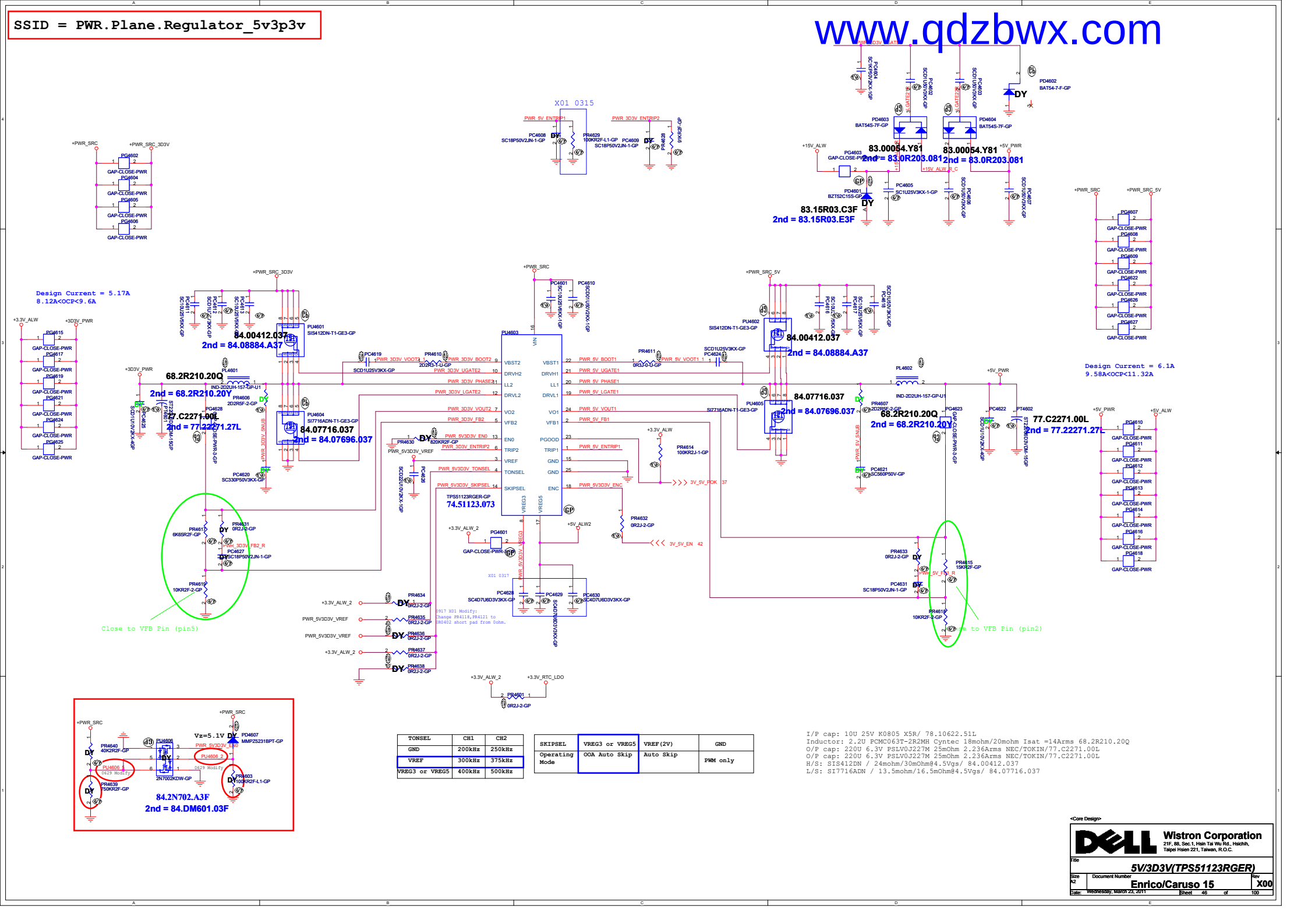
Title: CHARGER BQ24707

Size: C | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 45 of 100

SSID = PWR.Plane.Regulator_5v3p3v






| TONSEL | CH1 | CH2 |
|---|---|---|
| GND | 200kHz | 250kHz |
| VREF | 300kHz | 375kHz |
| VREG3 or VREG5 | 400kHz | 500kHz |

| SKIPSEL | VREG3 or VREG5 | VREF(2V) | GND |
|---|---|---|---|
| Operating Mode | OOA Auto Skip | Auto Skip | PWM only |

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U PCMC063T-2R2MH Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20Q
O/P cap: 220U 6.3V PSLV0J227M 25mOhm 2.236Arms NEC/TOKIN/77.C2271.00L
O/P cap: 220U 6.3V PSLV0J227M 25mOhm 2.236Arms NEC/TOKIN/77.C2271.00L
H/S: SIS412DN / 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN / 13.5mohm/16.5mOhm@4.5Vgs/ 84.07716.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V/3D3V(TPS51123RGER)

| Size | Document Number | Rev |
|---|---|---|
| A2 | Enrico/Caruso 15 | X00 |

Date: Wednesday, March 23, 2011 Sheet 46 of 100

SSID = CPU.Regulator

PU4701 ISL62882CHRTZ-T-GP

74.62882.A73

69.60013.141

2nd = 69.60026.081

69.60013.131

2nd = 69.60037.011

79.10712.6JL

2nd = 79.10112.3JL

3rd = 79.10712.6BL

4th = 79.10712.3BL

79.47612.3CL

2nd = 79.47612.3GL

3rd = 79.47612.30L

NTC 470K close to H_S MOSFET of Phase1

NTC 10K close to Choke of Phase1

BOM merge 9/14

BOM merge 10/07

BOM merge 10/04

BOM merge 9/14

BOM merge 9/14

BOM merge 10/07

BOM merge 9/14

0919 SA

Intel support POC (power on current).

<Core Design>

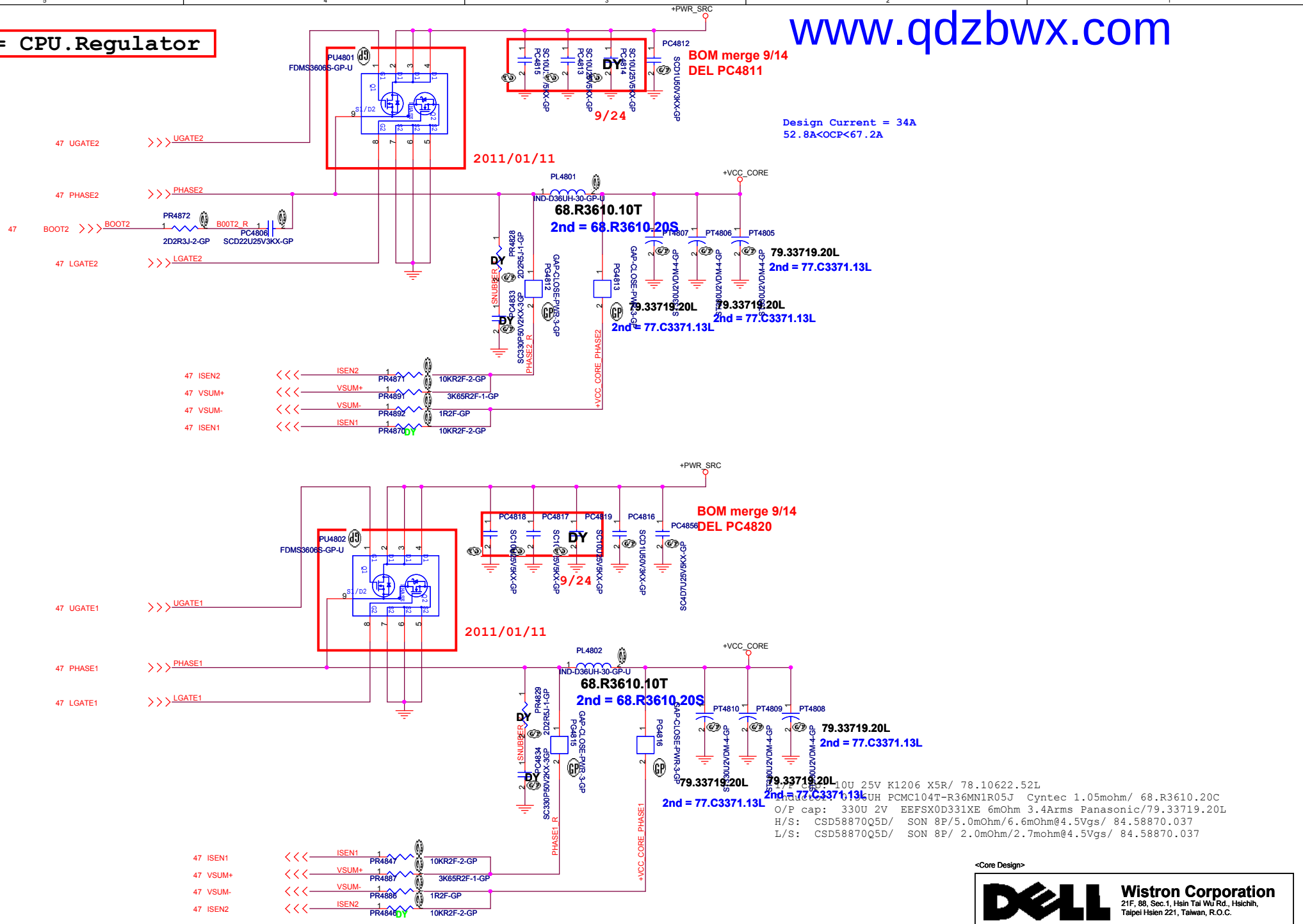
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 47 of 100

SSID = CPU.Regulator




```
P/P cap:  10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J  Cyntec 1.05mohm/ 68.R3610.20C
O/P cap:  330U 2V  EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
H/S:  CSD58870Q5D/  SON 8P/5.0mOhm/6.6mOhm@4.5Vgs/ 84.58870.037
L/S:  CSD58870Q5D/  SON 8P/ 2.0mOhm/2.7mohm@4.5Vgs/ 84.58870.037
```

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

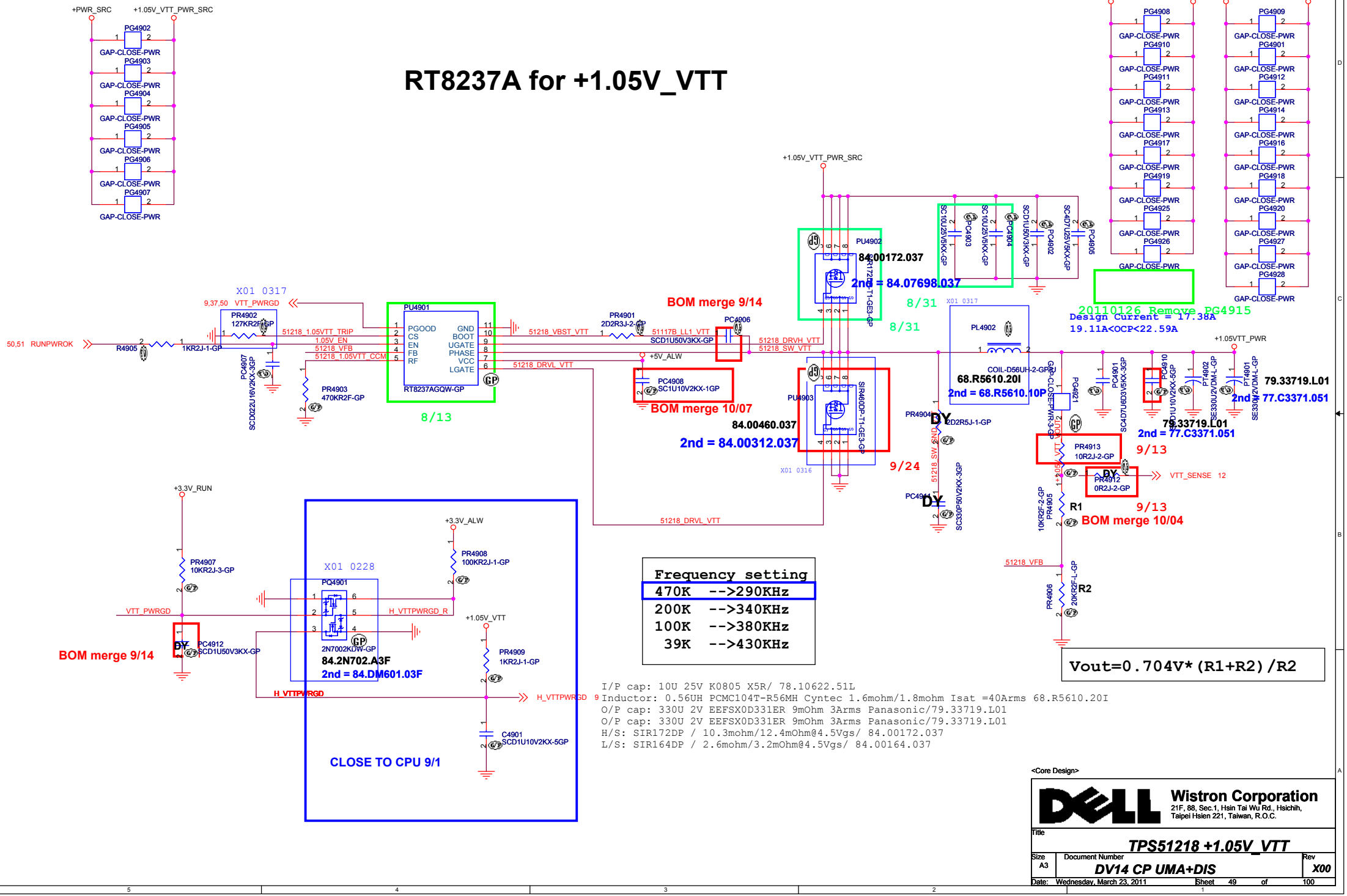
Title: ISL62883 CPU_CORE

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

Date: Wednesday, March 23, 2011 Sheet 48 of 100

SSID = CPU.Regulator

# RT8237A for +1.05V_VTT




| Frequency setting |
|---|
| 470K -->290KHz |
| 200K -->340KHz |
| 100K -->380KHz |
| 39K -->430KHz |

Vout=0.704V*(R1+R2)/R2

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 0.56UH PCMC104T-R56MH Cyntec 1.6mohm/1.8mohm Isat =40Arms 68.R5610.20I
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
H/S: SIR172DP / 10.3mohm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SIR164DP / 2.6mohm/3.2mOhm@4.5Vgs/ 84.00164.037

<Core Design>

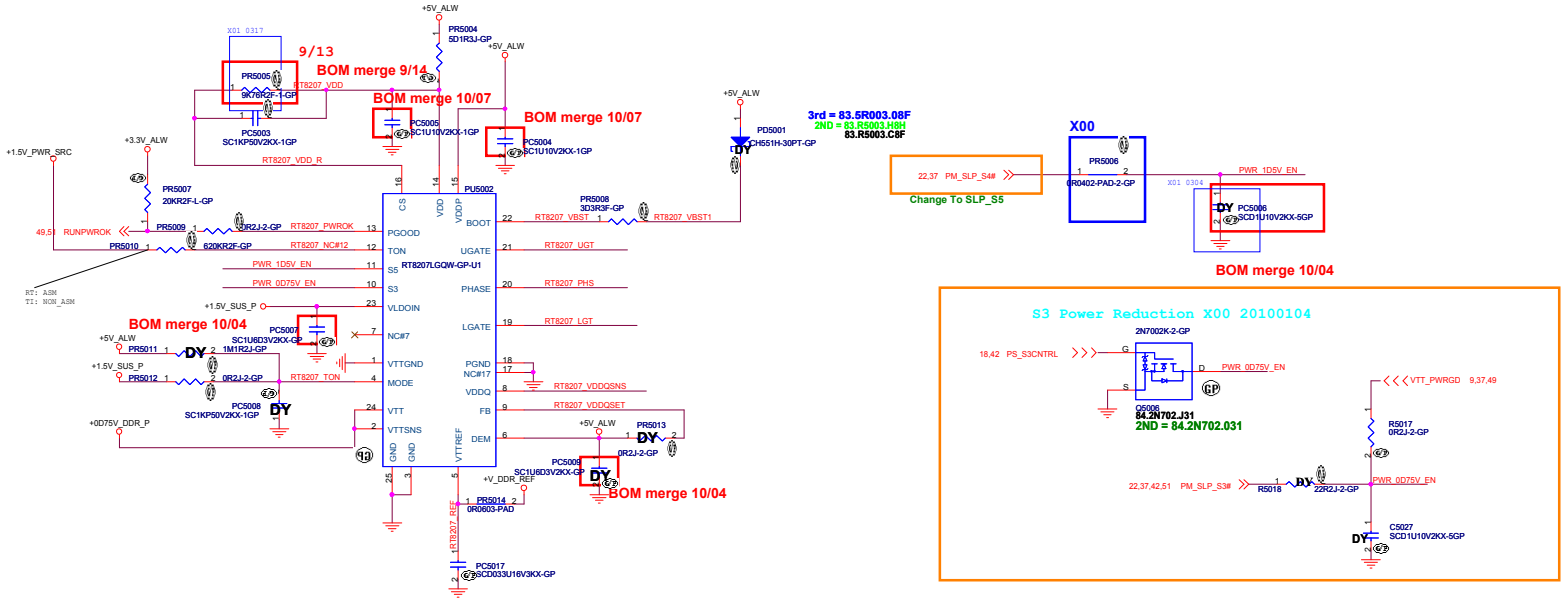
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218 +1.05V_VTT

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

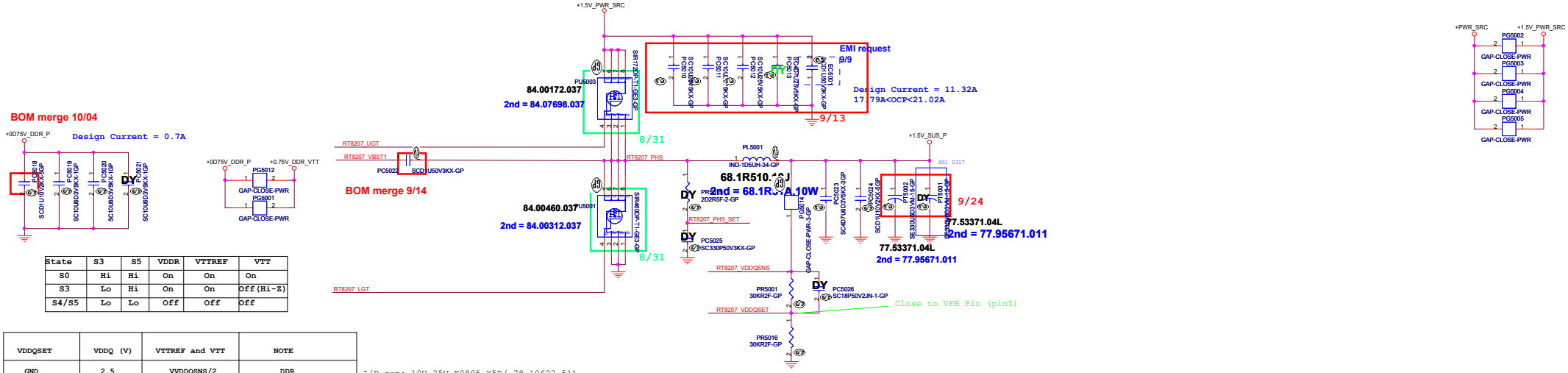
Date: Wednesday, March 23, 2011 | Sheet 49 of 100

SSID = PWR.Plane.Regulator_1p5v0p75v




S3 Power Reduction X00 20100104




| State | S3 | S5 | VDDR | VTTREF | VTT |
|---|---|---|---|---|---|
| S0 | Hi | Hi | On | On | On |
| S3 | Lo | Hi | On | On | Off(Hi-Z) |
| S4/S5 | Lo | Lo | Off | Off | Off |

| VDDQSET | VDDQ (V) | VTTREF and VTT | NOTE |
|---|---|---|---|
| GND | 2.5 | VVDDQSNS/2 | DDR |
| V5IN | 1.8 | VVDDQSNS/2 | DDR2 |
| FB Resistors | Adjustable | VVDDQSNS/2 | 1.5 V < VVDDQ < 3 V |

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.5U PCMC104T-1R5MH Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
H/S: SIR172DP / 10.3mohm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SIR460DP / 4.9mohm/6.1mOhm@4.5Vgs/ 84.00460.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8207 +1.5V_SUS

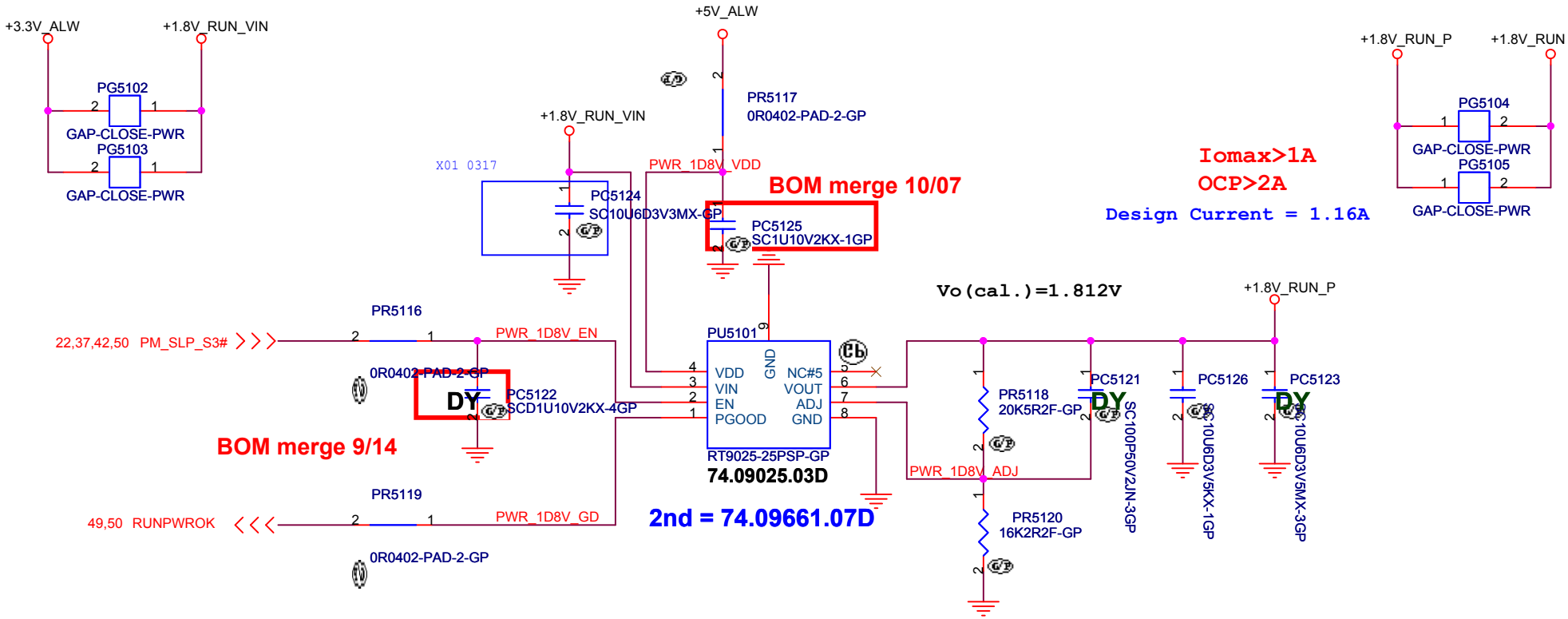
| Size | Document Number | Rev |
|---|---|---|
| A2 | DV14 CP UMA+DIS | X00 |

Date: Wednesday, March 23, 2011 Sheet 50 of 100

SSID = PWR.Plane.Regulator_1p8v



# RT9025 for +1.8V_RUN




<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | RT9025_+1.8V_RUN | |
| Size: A4 | Document Number: DV14 CP UMA+DIS | Rev: X00 |
| Date: Wednesday, March 23, 2011 | Sheet 51 of 100 | |

(Blanking)

<Core Design>

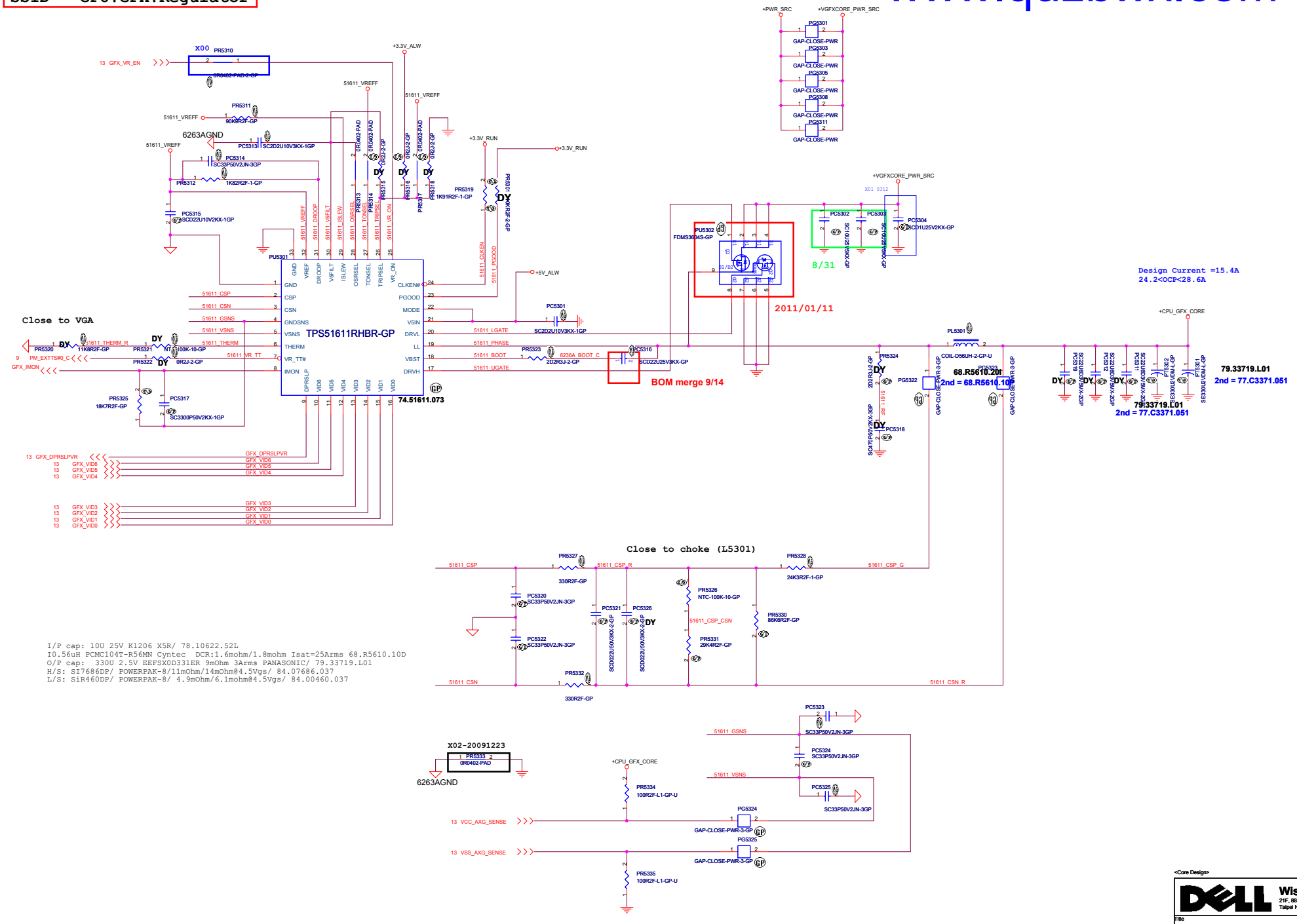
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | *DV14 CP UMA+DIS* | *X00* |

Date: Thursday, January 06, 2011 Sheet 52 of 100

SSID = CPU.GFX.Regulator




Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Core Design>

Title: TPS51611 +GFX_CORE

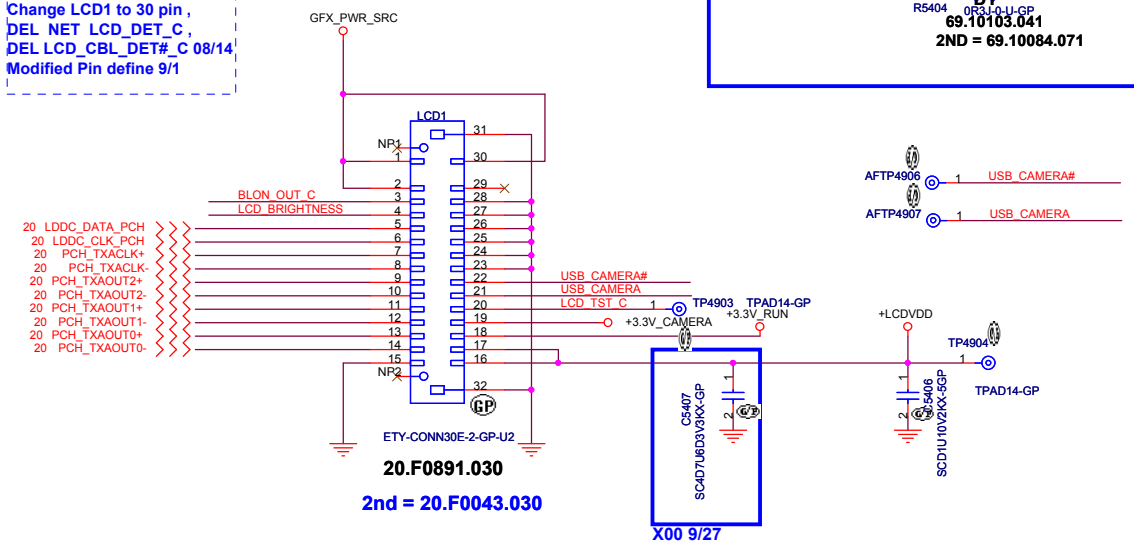
Size: A2 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 53 of 100

SSID = VIDEO

## LVDS CONNECTOR

Change LCD1 to 30 pin ,
DEL NET LCD_DET_C ,
DEL LCD_CBL_DET#_C 08/14
Modified Pin define 9/1

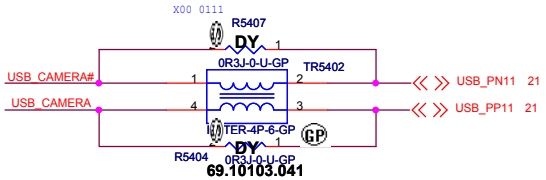



20.F0891.030

2nd = 20.F0043.030

X00 9/27

EMI suggestion 9/23

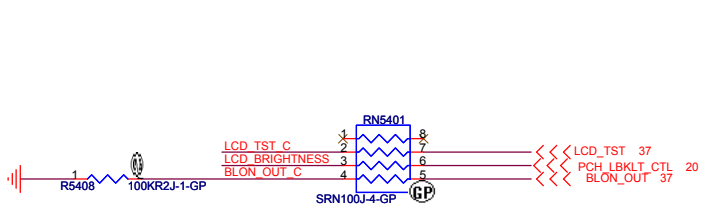


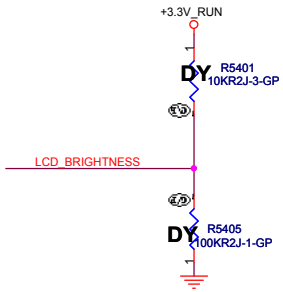

69.10103.041

2ND = 69.10084.071

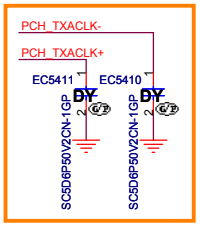
AFTP4906 USB_CAMERA#

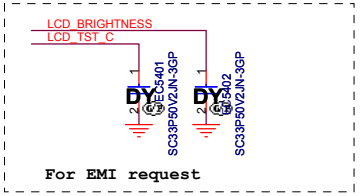
AFTP4907 USB_CAMERA



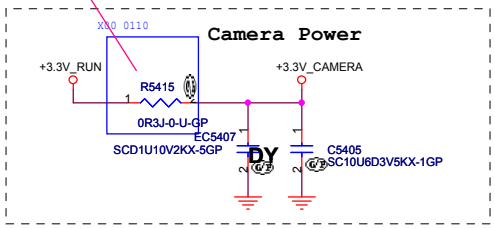




Close to LVDS connector



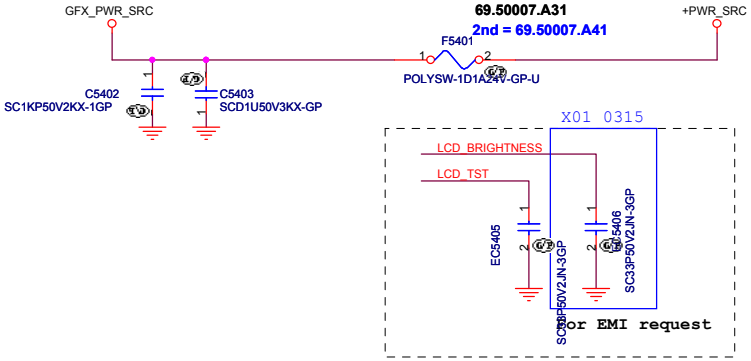




Note:R5415 cannot use short pad for safty



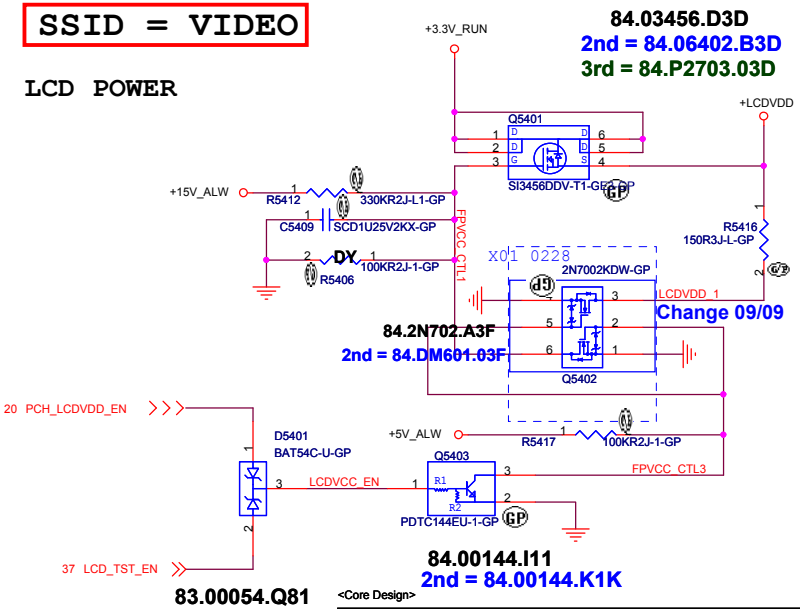

SSID = Inverter

## INVERTER POWER




SSID = VIDEO

## LCD POWER




<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 54 of 100

SSID = VIDEO



X01 0228

+3.3V_RUN

2N7002KDW-GP

20 PCH_CRT_DDCDATA

CRT_DDCDATA_CON

20 PCH_CRT_DDCCLK

CRT_DDCCLK_CON

Q5501

84.2N702.A3F

2nd = 84.DM601.03F

5V Tolerance

85 CRT_GFX_DDCDAT

85 CRT_GFX_DDCCLK

RN5506

DIS_CRT

SRN0J-6-GP

CRT_DDCDATA_CON

CRT_DDCCLK_CON

5V_CRT_S0

RN5501

SRN2K2J-1-GP

CRT_DDCDATA_CON

CRT_DDCCLK_CON

C5514

SC22P50V2JN-4GP

C5513

SC22P50V2JN-4GP

5V_CRT_S0_R

X01 0308

CRT1

VCC_CRT

NC#4

NC#11

CRT_DDCDATA_CON

CRT_DDCCLK_CON

DDCDATA_ID1

DDCCLK_ID3

CHASSIS#16

CHASSIS#17

CRT_R

CRT_G

CRT_B

CRT_RED

CRT_GREEN

CRT_BLUE

GND

CRT_VSYNC_CON

CRT_HSYNC_CON

VSYNC

HSYNC

D-SUB-15-129-GP

AFTP509

20.20948.015

2nd = 20.20945.015

Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.

* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

20 PCH_CRT_BLUE

20 PCH_CRT_GREEN

20 PCH_CRT_RED

RN5507

SRN0J-7-GP

CRT_BLUE

CRT_GREEN

CRT_RED

85 CRT_GFX_R

85 CRT_GFX_G

85 CRT_GFX_B

RN5505

DIS_CRT

SRN0J-7-GP

AFTP501 5V_CRT_S0

AFTP502 CRT_DDCDATA_CON

AFTP503 CRT_DDCCLK_CON

AFTP504 CRT_R

AFTP505 CRT_G

AFTP506 CRT_B

AFTP507 CRT_HSYNC_CON

AFTP508 CRT_VSYNC_CON

CRT_VSYNC_CON

CRT_HSYNC_CON

C5518

SC33P50V2JN-3GP

C5517

SC33P50V2JN-3GP

A00

68.00084.D61

2nd = 68.00217.991

3rd = 68.00213.021

BLM15BA330SS1D-GP

CRT_RED

CRT_GREEN

CRT_BLUE

L5501

L5502

L5503

CRT_R

CRT_G

CRT_B

RN5503

SRN150F-1-GP

C5504

C5505

C5506

SC8P250V2CC-GP

C5507

C5508

C5509

SC10P50V2JN-4GP

X01

5V_CRT_S0_R

F5501

FUSE-1D1A6V-4GP-U

5V_CRT_S0

D5502

CH551H-30PT-GP

+5V_RUN

69.50007.691

2nd = 69.50007.771

83.R5003.C8F

2ND = 83.R5003.H8H

3rd = 83.5R003.08F

*Hsync & Vsync level shift*

5V_CRT_S0

C5512

SCD1U16V2KX-3GP

U5501A

TSAHCT125PW-GP

CRT_HSYNC

HSYNC_5

U5501B

TSAHCT125PW-GP

CRT_VSYNC

VSYNC_5

RN5502

SRN33J-5-GP-U

CRT_HSYNC_CON

CRT_VSYNC_CON

X00 9/23

R5502 0R2J-2-GP

R5503 0R2J-2-GP

20 PCH_CRT_HSYNC

20 PCH_CRT_VSYNC

RN5508

SRN0J-6-GP

CRT_HSYNC

CRT_VSYNC

83,85 VGA_CRT_HSYNC

83,85 VGA_CRT_VSYNC

RN5509

DIS_CRT

SRN0J-6-GP

CRT_HSYNC

CRT_VSYNC

CLOSE TO TRANSFORMER

5V_CRT_S0

D5501

CRT_R

BAV99PT-GP-U

D5503

CRT_G

BAV99PT-GP-U

D5504

CRT_B

BAV99PT-GP-U

5V_CRT_S0

U5501C

TSAHCT125PW-GP

5V_CRT_S0

U5501D

TSAHCT125PW-GP

<Core Design>

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size: A3

Document Number: DV14 CP UMA+DIS

Rev: X00

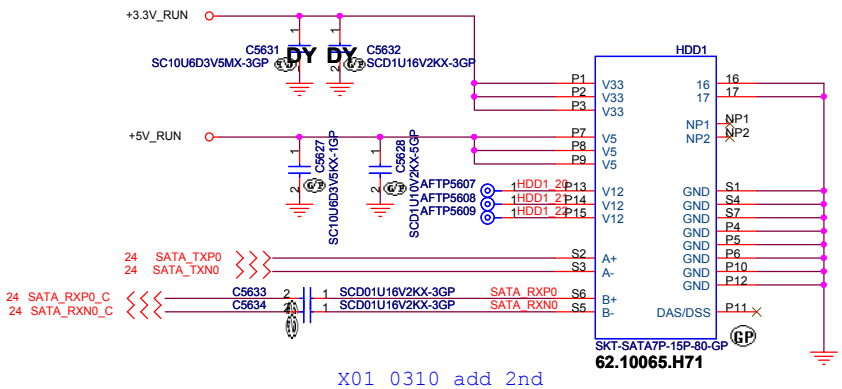
Date: Wednesday, March 23, 2011

Sheet 55 of 100

SSID = SATA



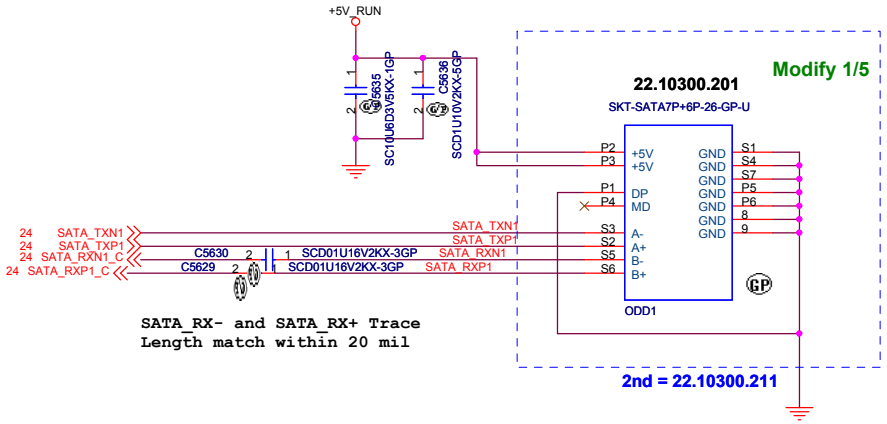
# SATA HDD Connector




X01 0310 add 2nd

2nd = 62.10065.H81

# SATA ODD Connector




2nd = 22.10300.211

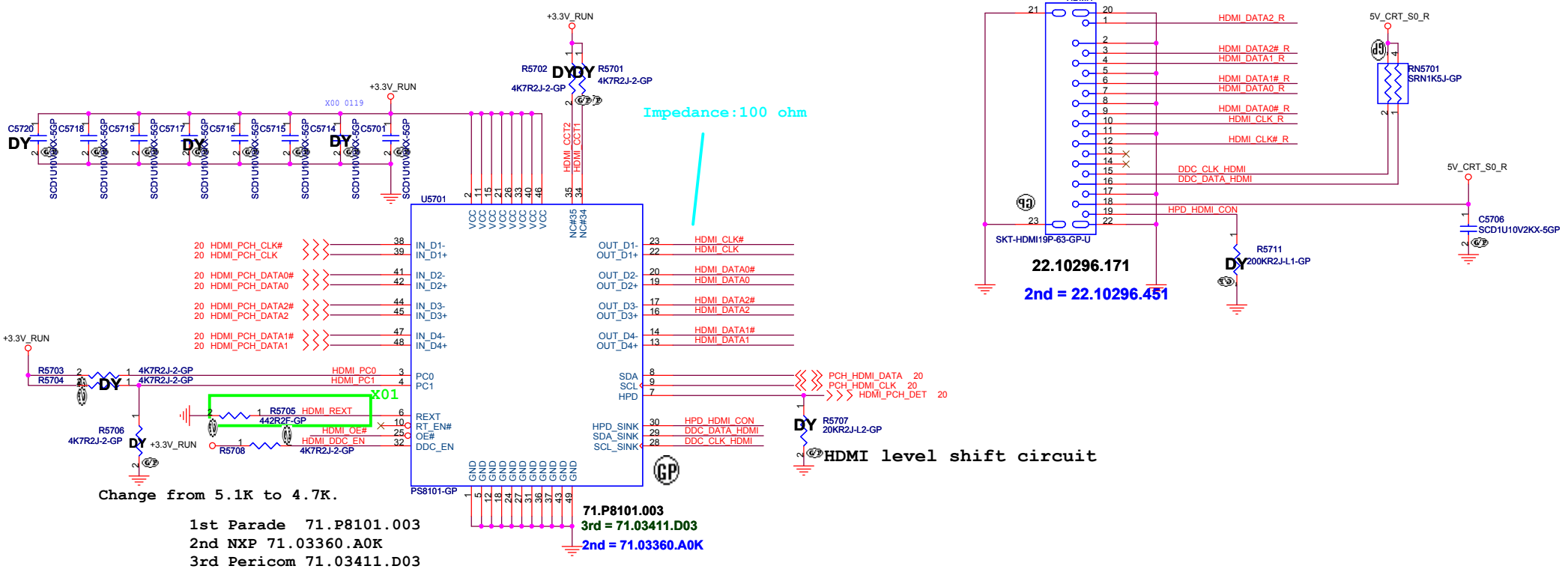
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | HDD/ODD | |
| Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00 |
| Date: Wednesday, March 23, 2011 | Sheet 56 of 100 | |

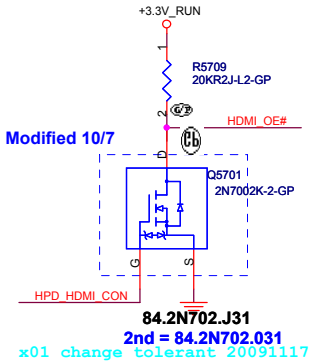
SSID = VIDEO

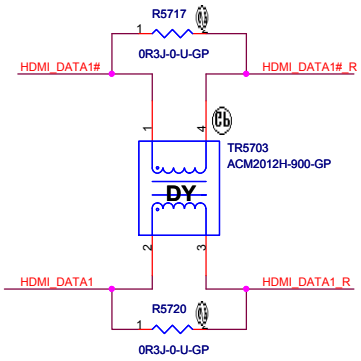
# HDMI Level Shifter & CONNECTOR

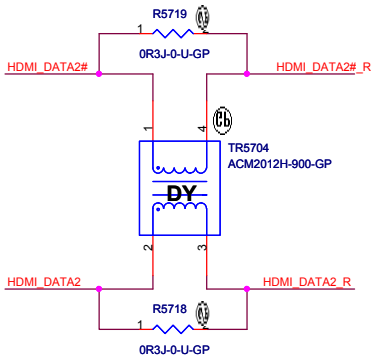


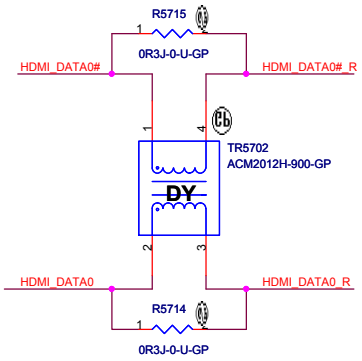


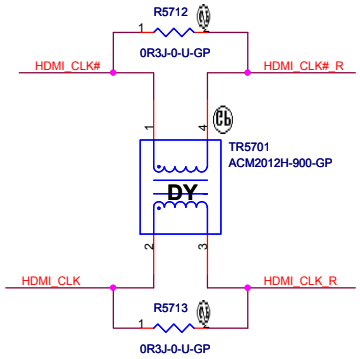





<Core Design>

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Title: HDMI Level Shift/ Connector

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

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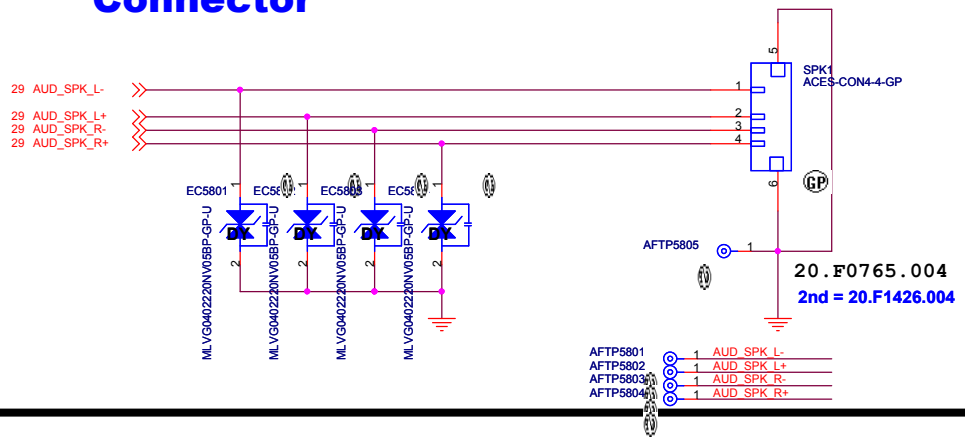
SSID = AUDIO

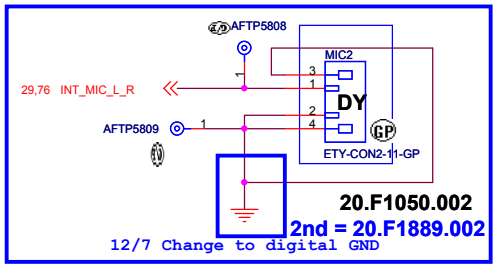
# Speaker Connector






11/26 reserve MIC2

12/7 change MIC2 to 20.F1050.002 X01 0309




X01 0309
20.F1889.002 20.F1050.002

<Core Design>

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Title: Audio Jack

| Size | Document Number | Rev |
|---|---|---|
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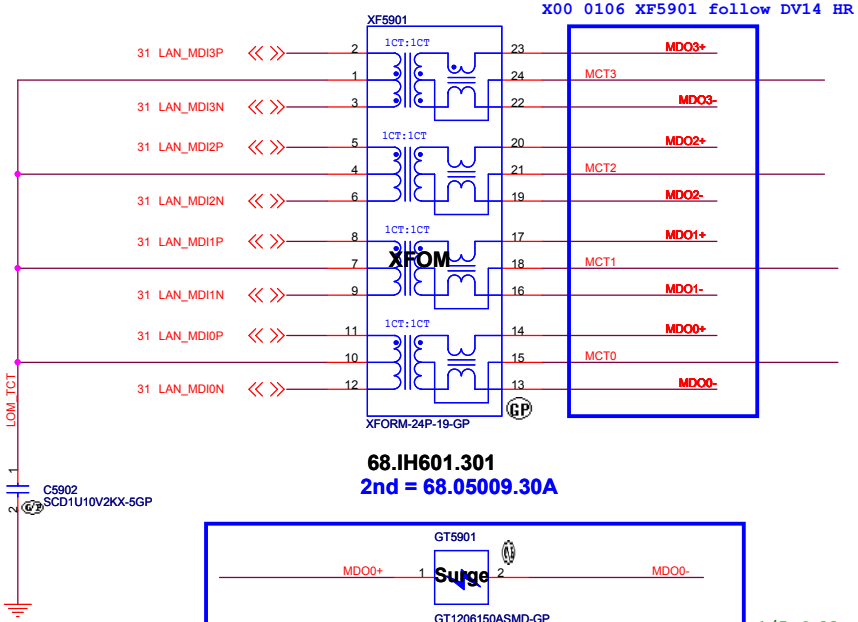
SSID = LOM

# LAN TransFormer

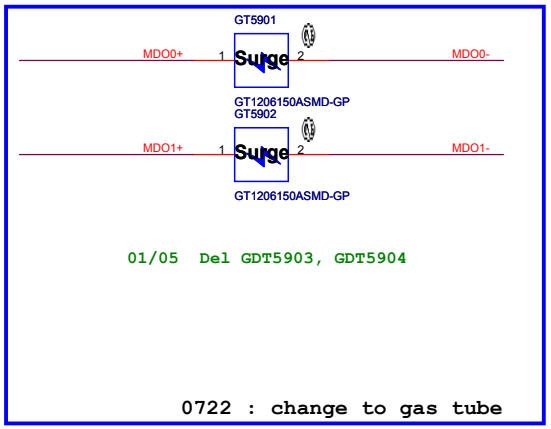
X01-0312
Add EMI solution for surge

X00 0106 XF5901 follow DV14 HR

X00 0210
For GIGA LAN, use Transformer
68.IH601.301
For 10/100M LAN, use Transformer
68.HH035.301

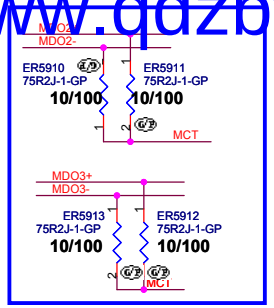


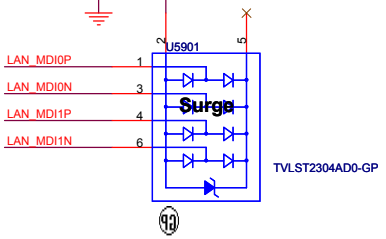

68.IH601.301
2nd = 68.05009.30A



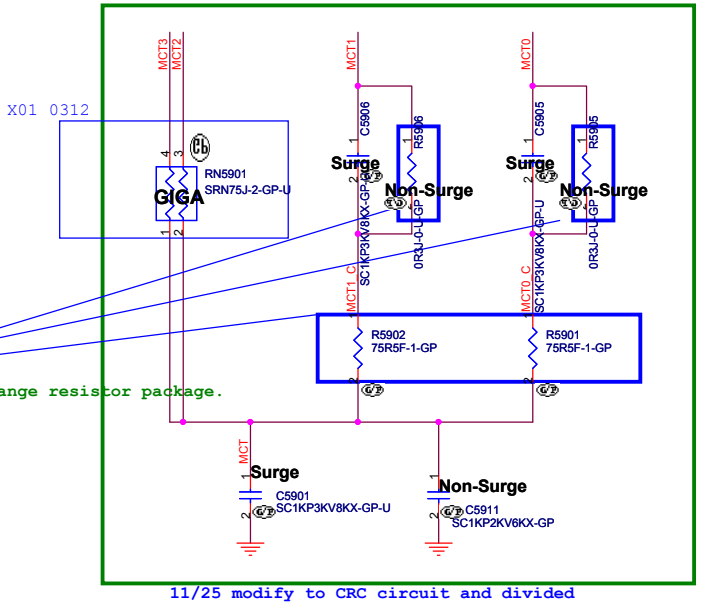

01/05 Del GDT5903, GDT5904

0722 : change to gas tube



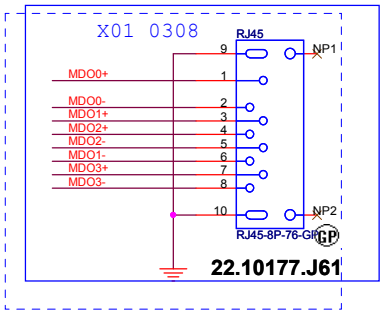

X00 20110105

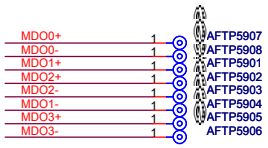



1/5 follow HR change resistor package.

11/25 modify to CRC circuit and divided resistor as EMI suggest
11/29 Change C5911 to 78.1022S.22L

# RJ45




<Core Design>

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Title: LAN CONN
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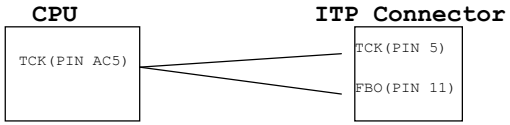
SSID = User.Interface



# ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil ( max ),
others place near CPU side.




<Core Design>

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Title: ITP/Fan Connector

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

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# (Blanking)

<Core Design>

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Title: *Reseved*

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|---|---|---|
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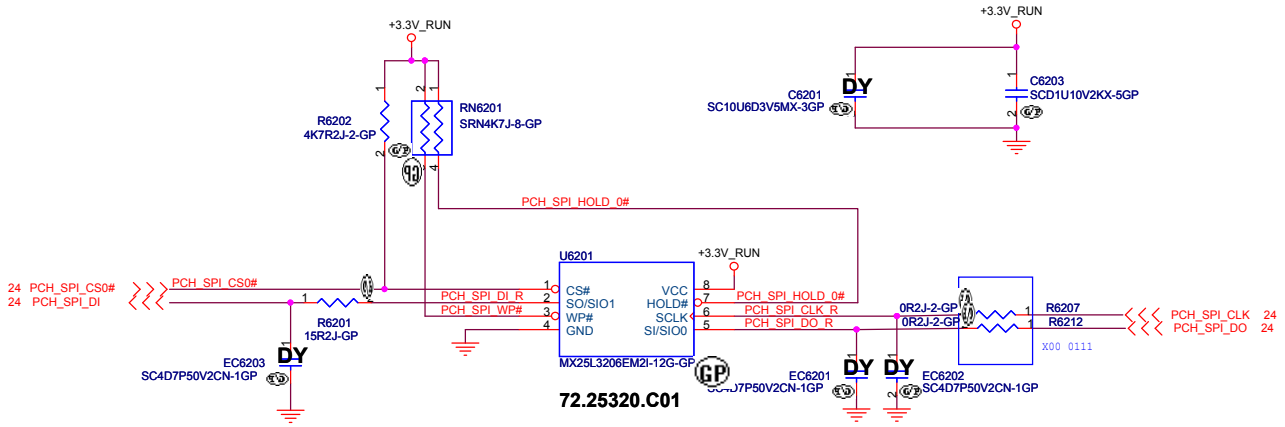
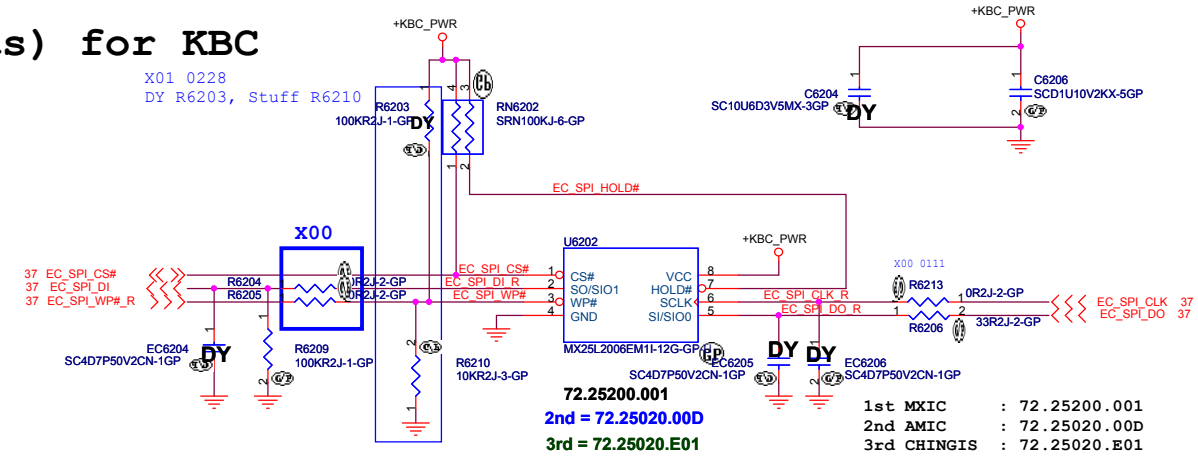
**SSID = Flash.ROM**

# SPI FLASH ROM (32M bits) for PCH

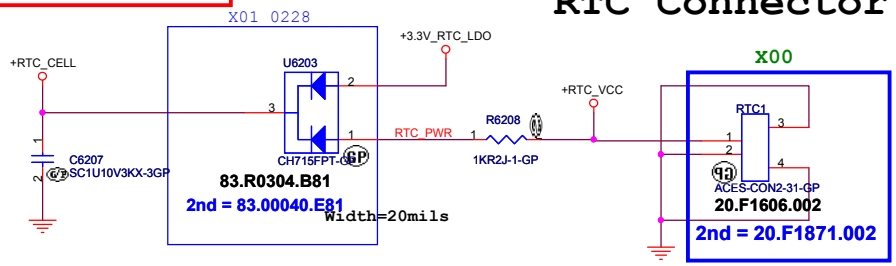


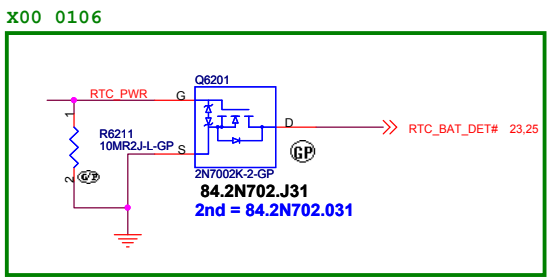

# SPI FLASH ROM (2M bits) for KBC




**SSID = RBATT**

# RTC Connector




<Core Design>

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Title: Flash/RTC

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

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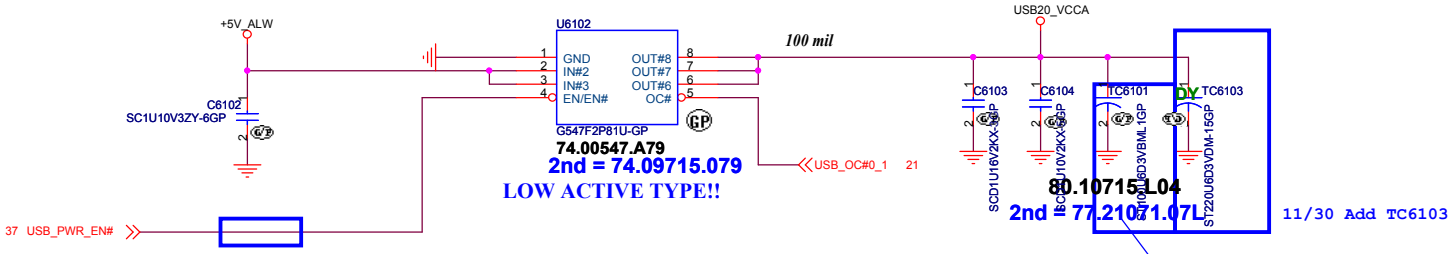
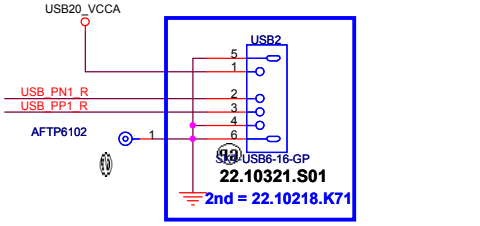
SSID = USB






11/30 Add TC6103

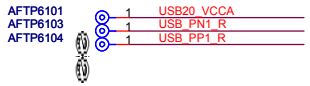
12/22 change TC6101 to 100uF

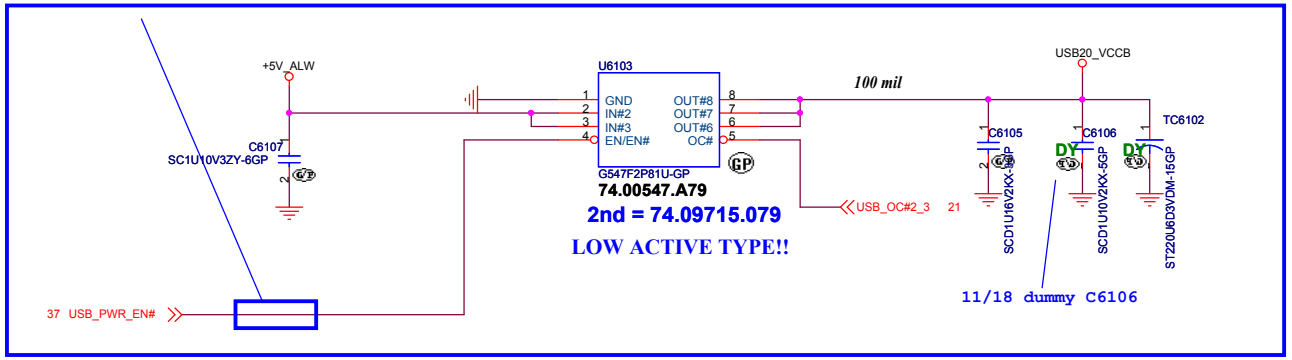



11/29 change USB2 to 22.10321.S01

11/18 remove R6101, R6104

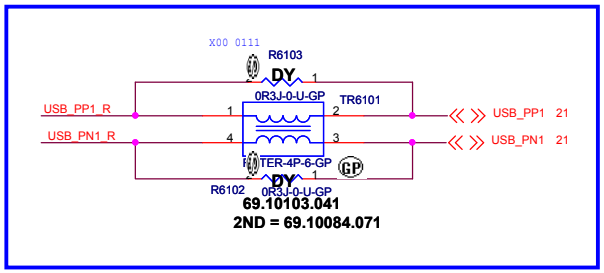
11/10 Move USB power SW to Mainboard

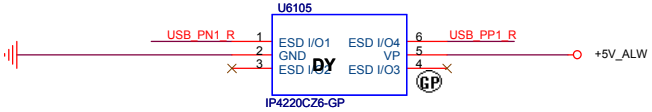



11/18 dummy C6106

11/1 Stuff TR6101 for EMI




<Core Design>

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Title: USB

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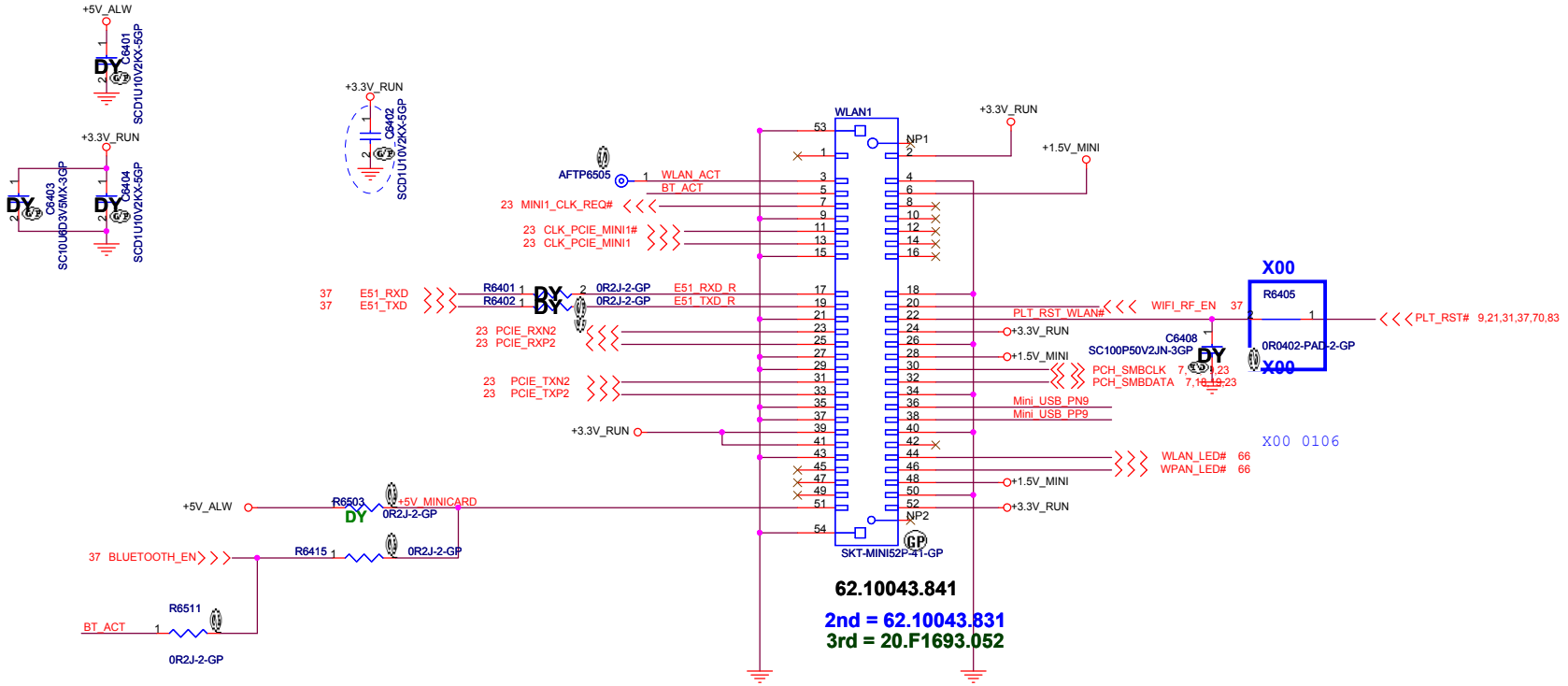
SSID = Wireless



# Mini Card Connector(802.11a/b/g)



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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: *X00*

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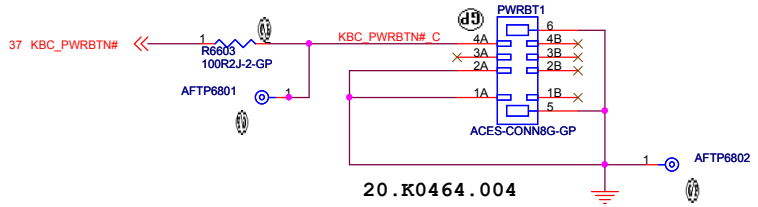
SSID = User.Interface



# Power BTN Connector




20.K0464.004

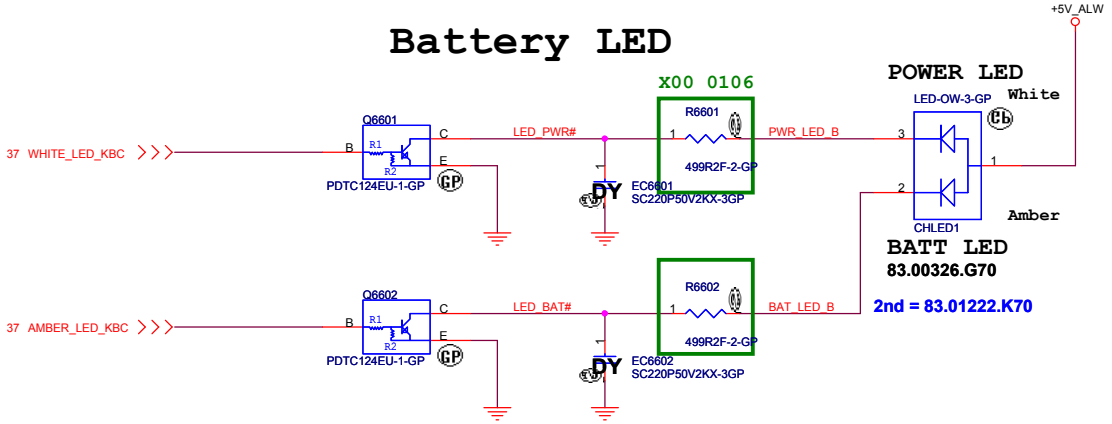
2nd = 20.K0341.004

12/10 change PWRBT1 pin define

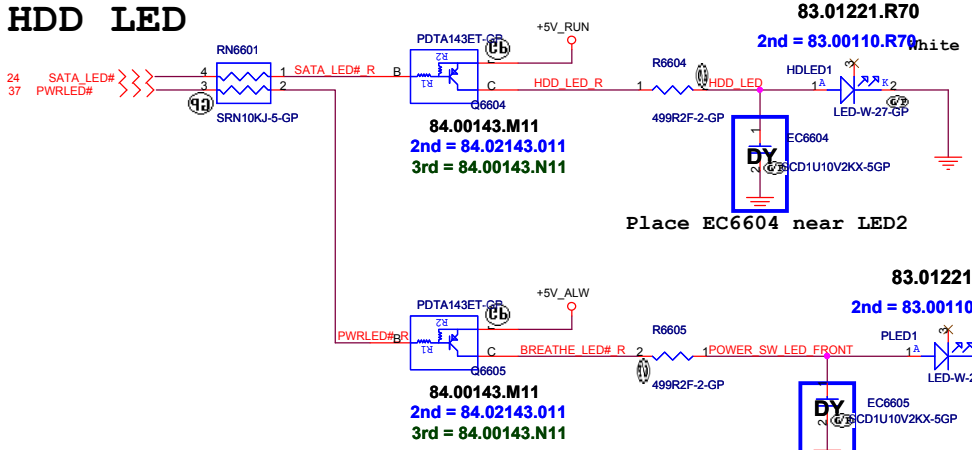
12/21 change PWRBT1 to 20.K0464.004

Modify 09/02

# Battery LED

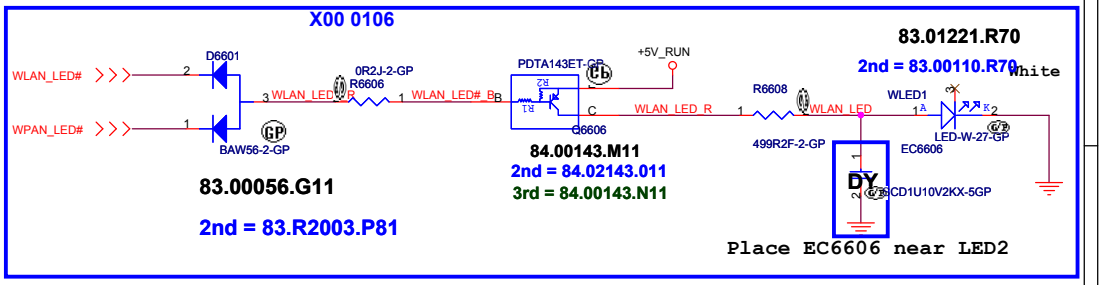



# HDD LED




# BREATHE PWR LED (Front)

# WLAN LED




<Core Design>

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| | | |
|---|---|---|
| Title | PWR_BTN/LED | |
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<Core Design>

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Title: *Reserved*

| Size | Document Number | Rev |
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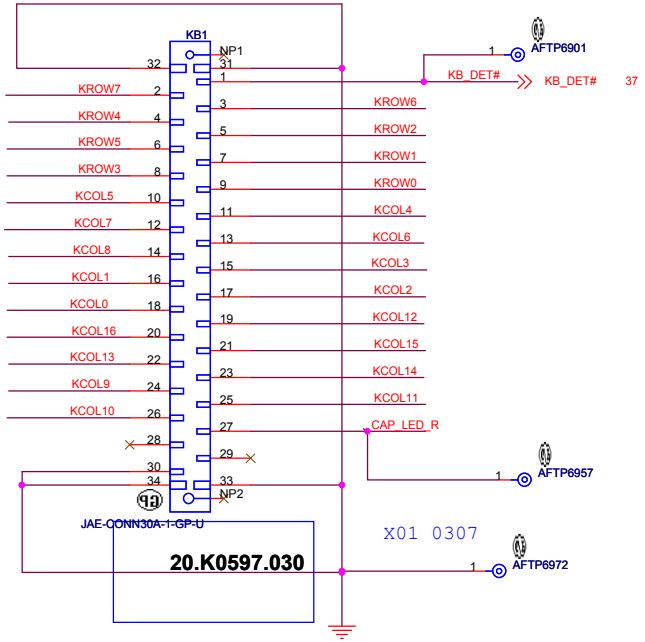
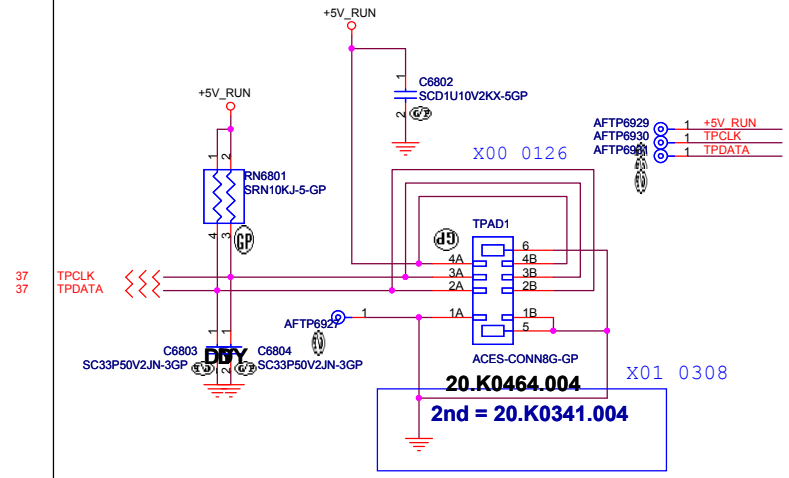
SSID = KBC

## Internal KeyBoard Connector



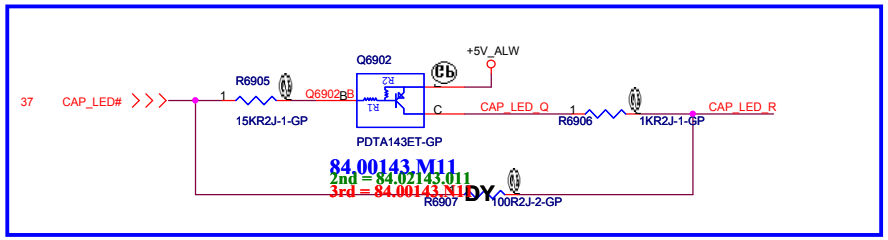

SSID = Touch.Pad

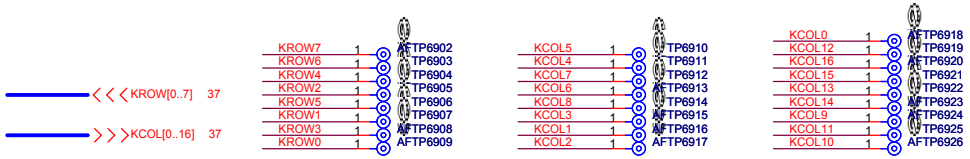
## TouchPad Connector




12/8 Add Cap LED control circuit

# CAP LED CONTROL




11/23 change TPAD1 to 20.K0320.004

<Core Design>

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Title: Key Board/Touch Pad

| Size | Document Number | Rev |
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SSID = User.Interface

<Core Design>

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Title

# Hall Sensor

| Size | Document Number | Rev |
|---|---|---|
| A4 | DV14 CP UMA+DIS | X00 |

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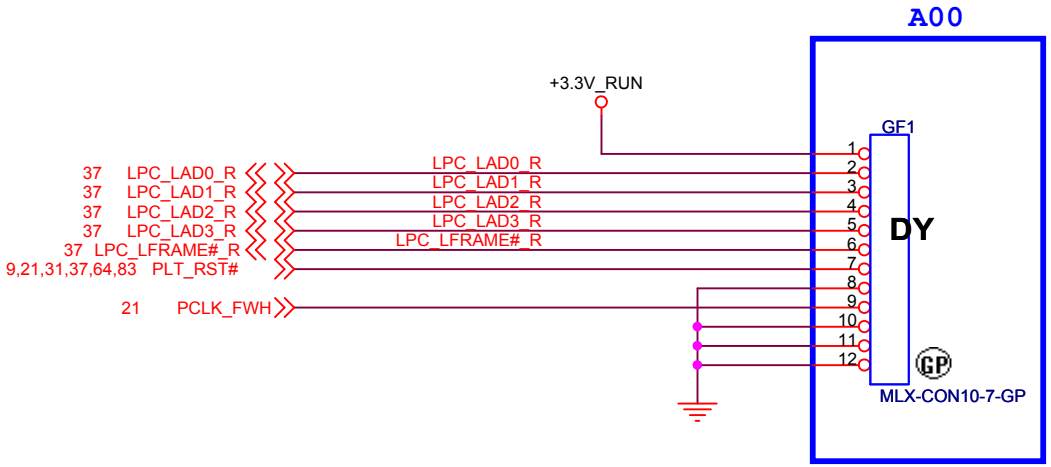
**SSID = User.Interface**




<Core Design>

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Title: ***Reserved***

| Size | Document Number | Rev |
|---|---|---|
| A4 | ***DV14 CP UMA+DIS*** | ***X00*** |

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# (Blanking)

<Core Design>

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Title: *Reserved*

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<Core Design>

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Title: RESERVED

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

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(Blanking)

<Core Design>

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Title: *Reserved*

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|---|---|---|
| A3 | *DV14 CP UMA+DIS* | *X00* |

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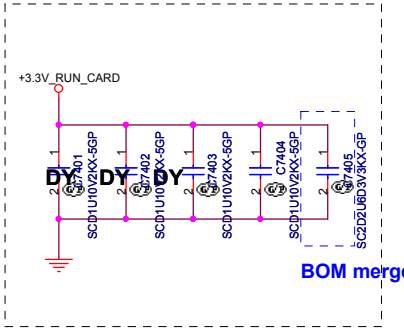
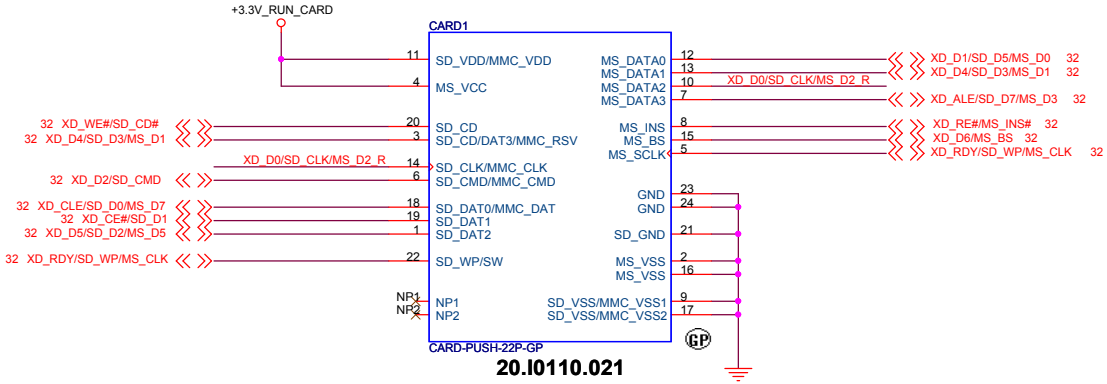
SSID = SDIO

# SD/XD/MS Card Reader



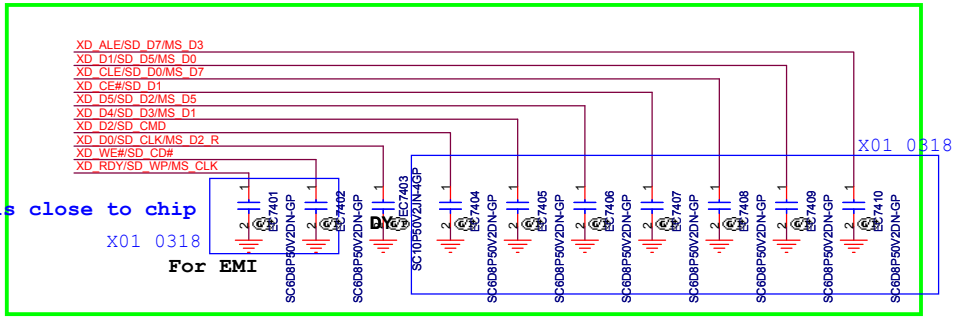

BOM merge Change 09/09

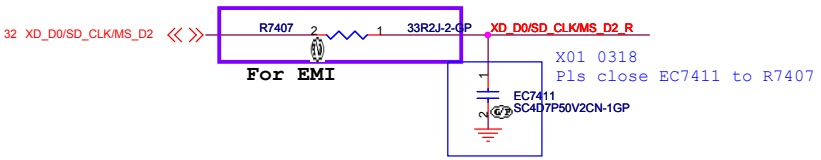



20.I0110.021

2nd = 20.I0133.001

0810 Vendor Recommand




<Core Design>

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| | | |
|---|---|---|
| Title | Reserved | |
| Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00 |
| Date: Wednesday, March 23, 2011 | Sheet 74 of 100 | |

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: *X00*

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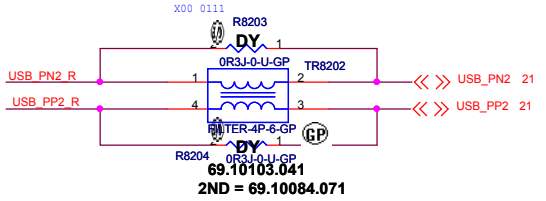
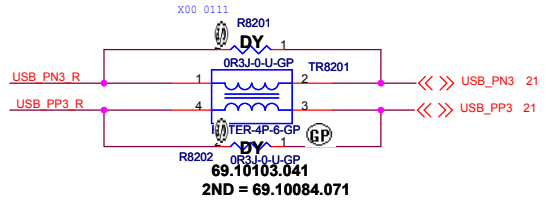
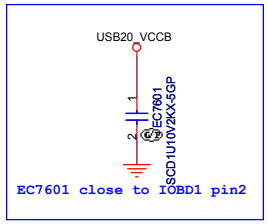
**SSID = User.Interface**

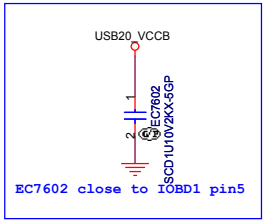
11/1 Stuff TR8201, TR8202 for EMI



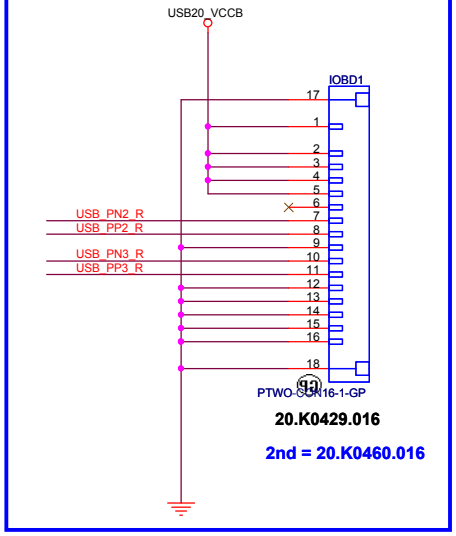

X00 0111



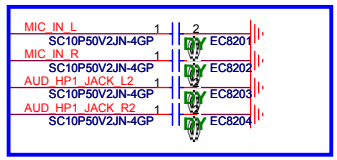




X00 0111

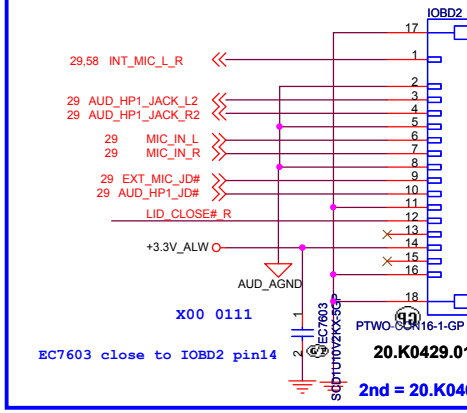
IOBD1 is for USB board

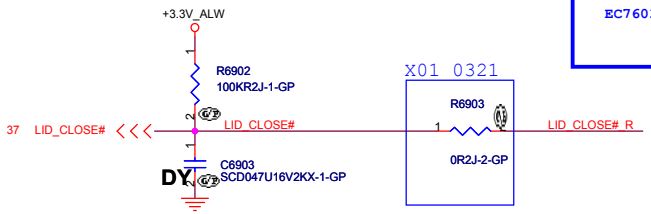



11/1 Add EC2901~EC2904 for EMI request




IOBD2 is for Audio board




<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 76 of 100

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | *DV14 CP UMA+DIS* | *X00* |

Date: Thursday, January 06, 2011 Sheet 77 of 100

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | *DV14 CP UMA+DIS* | *X00* |

Date: Thursday, January 06, 2011 Sheet 78 of 100

XSID = Mechanical

H1 HT85BE85R29-U-5-GP
H2 HOLE256R115-GP
H3 HT85BE85R29-U-5-GP
H4 HT85BE85R29-U-5-GP
H5 HT85BE85R29-U-5-GP
H6 HT85BE85R29-U-5-GP
H7 HT85B95X975R29-S-GP

X01 0316
SPR4 SPRING-13-GP-U
34.43E24.001

For CPU BRACKET
H8 HOLE197R166-1-GP
H9 HOLE197R166-1-GP
H10 HOLE197R166-1-GP

VGA Stand-Off
H11 STF237R117H83-1-GP DIS
34.4CK01.001

PCH Stand-Off
H12 STF237R117H83-1-GP
H13 STF237R117H83-1-GP
X01 0308
34.4CK01.001 34.4CK01.001

X01 0315
SPR1 SPRING-58-GP
34.4B312.002
SPR2 SPRING-62-GP
34.39S07.003

X00 0126
+1.05V_VTT +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +5V_ALW +5V_ALW
DY EC7970 SCD1U10V2KX-5GP
DY EC7971 SCD1U10V2KX-5GP
DY EC7972 SCD1U10V2KX-5GP
DY EC7973 SCD1U10V2KX-5GP
DY EC7974 SCD1U10V2KX-5GP
DY EC7975 SCD1U10V2KX-5GP
DY EC7976 SCD1U10V2KX-5GP
DY EC7977 SCD1U10V2KX-5GP
DY EC7978 SCD1U10V2KX-5GP
DY EC7979 SCD1U10V2KX-5GP
DY EC7980 SCD1U10V2KX-5GP
DY EC7981 SCD1U10V2KX-5GP
X01 0312

Add 9/27
EC7964 DY SCD1U10V2KX-5GP AUD_AGND
EC7965 DY SCD1U10V2KX-5GP AUD_AGND
EC7966 DY SCD1U10V2KX-5GP AUD_AGND
X01 0312
+PWR_SRC EC7965 SCD1U25V2KX-GP

Modified 8/24
Add 9/16
+PWR_SRC EC7901 SCD1U25V2KX-GP
EC7902 EC7903 EC7904 EC7905 EC7906 EC7907 EC7929 EC7930 EC7931 EC7932 EC7933 EC7934 EC7935 EC7936 EC7937 EC7938 EC7939 EC7940 EC7941 EC7942 EC7943 EC7944 EC7945 EC7946 EC7947
X01 0312

+5V_RUN EC7908 SCD1U10V2KX-5GP
EC7909 EC7910 EC7911 EC7982 EC7983
X00 0126
Add 9/16
+1.5V_SUS EC7952 EC7953 EC7954 EC7955 EC7956 EC7957 EC7958 EC7959 EC7960 EC7961 EC7966 EC7987
X01 0312
EC7985 near 5969.49 5620.99
Add 9/23

+3.3V_RUN EC7912 EC7913 EC7914 EC7915 EC7916 EC7917 EC7918 EC7919 EC7920 EC7962
Add 9/16
+3.3V_RUN EC7984
X00 0126
+1.05V_VTT EC7948 EC7949 EC7950 EC7951
Add 9/16
+1.5V_SUS EC7986
X01 0312
EC7985 near 5270.66 5222.88
+1.5V_SUS EC7988
X01 0312
EC7985 near 6101.25 5812.89

+3.3V_ALW EC7921 EC7922 EC7923 EC7924 EC7925 EC7926 EC7927 +5V_ALW EC7928 SCD1U25V2KX-GP
Modified 8/24
+3.3V_ALW EC7963 EC7964
Add 9/16
+1.5V_SUS EC7985
X01 0312
EC7985 near 6167.13 5283.03

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: DV14 CP UMA+DIS
Rev: X00
Date: Tuesday, March 22, 2011
Sheet 79 of 100

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: X00

Date: Thursday, January 06, 2011 | Sheet 80 of 100

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
*Reserved*

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

Date: Thursday, January 06, 2011 Sheet 81 of 100

(Blanking)

<Core Design>

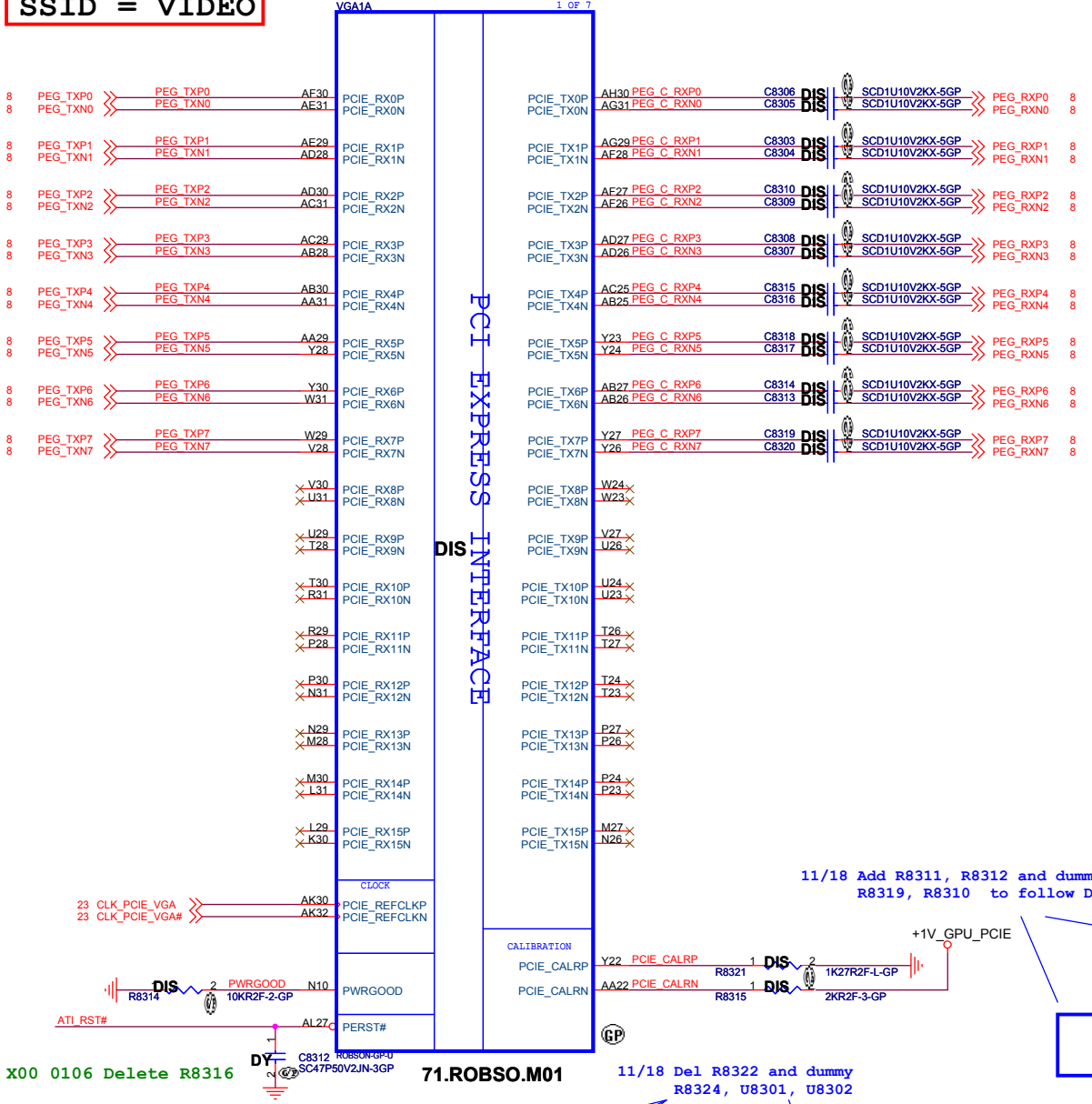
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: X00

Date: Thursday, January 06, 2011 | Sheet 82 of 100

# SSID = VIDEO




X00 0106 Delete R8316

11/18 Add R8311, R8312 and dummy R8319, R8310 to follow DN13

11/18 Del R8322 and dummy R8324, U8301, U8302

## CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

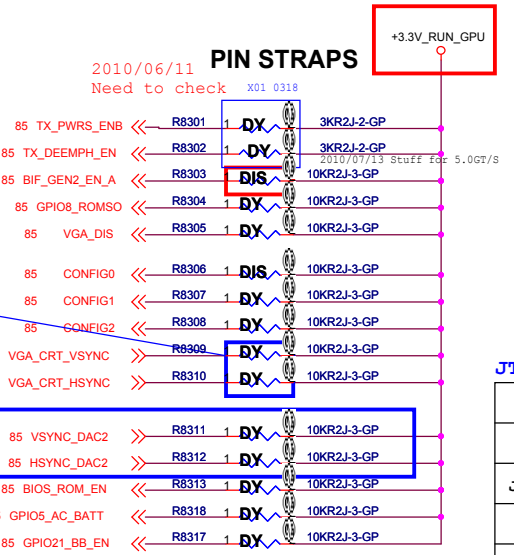
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

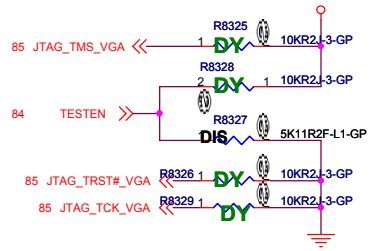
| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | RECOMMEND | PLATFORM SETTING |
|---|---|---|---|---|
| TX_PWRS_ENB | GPIO0 | Transmitter Power Savings Enable<br>0: 50% Tx output swing 1: Full Tx output swing | X | 1 |
| TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS ENABLED<br>0:Tx de-emphasis disabled 1:Tx de-emphasis enabled | X | 1 |
| BIF_GEN2_EN_A | GPIO2 | 0:Advertises the PCIe device as 2.5GT/s capable at power on.<br>1:Advertises the PCIe device as 5.0GT/s capable at power on. | 0 | 0 |
| GPIO5_AC_BATT | GPIO5 | optional input allow the system to request a fast power reduction by setting GPIO5 to low. | ? | 0 |
| GPIO8_ROMSO | GPIO8 | RESERVED | 0 | 0 |
| VGA_DIS | GPIO9 | 0:VGA Controller capacity enabled<br>1:The device won't be recognized as the system's VGA controller | 0 | 0 |
| ROMIDCFG[2:0] | GPIO[13:11] | BIOS_ROM_EN=1, Config[2:0] defines the ROM type<br>BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size | X X X | 0 0 1 (256MB) |
| GPIO21_BB_EN | GPIO21 | RESERVED | 0 | 0 |
| BIOS_ROM_EN | GPIO_22_ROMCSB | 0:Disable external BIOS ROM device<br>1:Enable external BIOS ROM device | X | 0 |
| VIP_DEVICE_STRAP_EN | V2SYNC | VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface. | X | 0 |
| RSVD | H2SYNC | RESERVED | 0 | 0 |
| RSVD | GENERICC | RESERVED | 0 | 0 |
| AUD[1] | HSYNC | AUD[1:0]:11-Audio for both DisplayPort and HDMI | X | 1 |
| AUD[0] | VSYNC | | X | 1 |

2010/06/11

## PIN STRAPS

2010/06/11 Need to check X01 0318

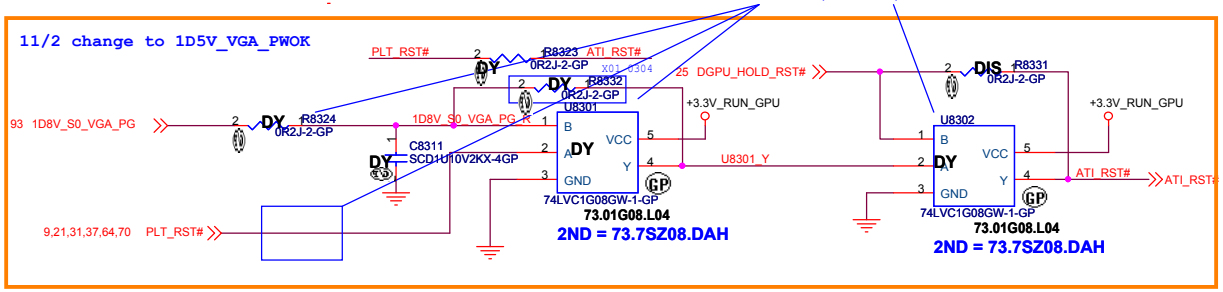



## JTAG SIGNAL OPTION

| Signal | Normal mode | Debug mode | pilot run mode |
|---|---|---|---|
| TESTEN | "1"(PU) | "1"(PU) | "0"(PD) |
| JTAG_TRST# | "0"(PD) | "1"(PU) | NC |
| JTAG_TCK | CLK | "1"(PU) | NC |
| JTAG_TMS | "1"(PU) | "1"(PU) | NC |

11/2 change to 1D5V_VGA_PWOK




| PE_GPIO0 | |
|---|---|
| dGPU mode | H |
| IGPU | L |
| IGPU with BACO | H |

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

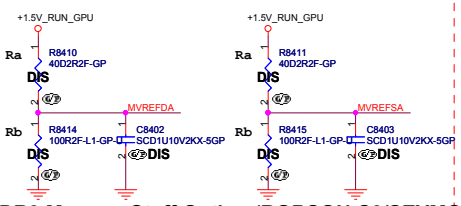
Size: A3 | Document Number: Enrico Caruso 14 | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 83 of 100

SSID = VIDEO

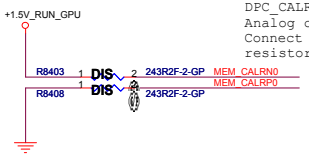


PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

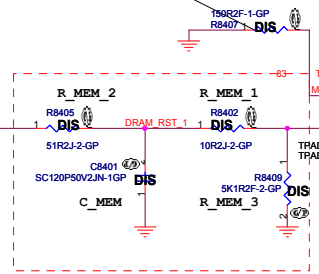



## DDR3/GDDR3 Memory Stuff Option (ROBSON-S3/SEYMOUR-XT-S3)

| | DDR5 | DDR3 |
|---|---|---|
| MVDDQ | 1.5V | 1.5V/1.8V |
| Ra | 40.2R | 40.2R |
| Rb | 100R | 100R |




DPC_CALR (Park/Robson-S3):
Analog calibration.
Connect DPxx_CALR to GND through a 150- (1%)
resistor.




88,89 MEM_RST

** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

| Designator | For SEYMOUR | For Robson |
|---|---|---|
| R_MEM_1 | 10R | 10R |
| R_MEM_2 | 50R | 50R |
| R_MEM_3 | 5K | 5K |
| C_MEM | 120pF | 120pF |

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except R_MEM_2

88 MDA[0..31]

89 MDA[32..63]

VGA1C 3 OF 7

MEMORY INTERFACE

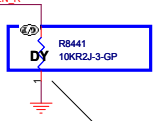
DIS

| | | | |
|---|---|---|---|
| MDA0 | K27 | DQA_0 | |
| MDA1 | J29 | DQA_1 | |
| MDA2 | H30 | DQA_2 | |
| MDA3 | H32 | DQA_3 | |
| MDA4 | G29 | DQA_4 | |
| MDA5 | F28 | DQA_5 | |
| MDA6 | F32 | DQA_6 | |
| MDA7 | F30 | DQA_7 | |
| MDA8 | C30 | DQA_8 | |
| MDA9 | F27 | DQA_9 | |
| MDA10 | A28 | DQA_10 | |
| MDA11 | C28 | DQA_11 | |
| MDA12 | E27 | DQA_12 | |
| MDA13 | G26 | DQA_13 | |
| MDA14 | D26 | DQA_14 | |
| MDA15 | F25 | DQA_15 | |
| MDA16 | A25 | DQA_16 | |
| MDA17 | C25 | DQA_17 | |
| MDA18 | E25 | DQA_18 | |
| MDA19 | D24 | DQA_19 | |
| MDA20 | E23 | DQA_20 | |
| MDA21 | F23 | DQA_21 | |
| MDA22 | D22 | DQA_22 | |
| MDA23 | F21 | DQA_23 | |
| MDA24 | E21 | DQA_24 | |
| MDA25 | D20 | DQA_25 | |
| MDA26 | F19 | DQA_26 | |
| MDA27 | A19 | DQA_27 | |
| MDA28 | D18 | DQA_28 | |
| MDA29 | F17 | DQA_29 | |
| MDA30 | A17 | DQA_30 | |
| MDA31 | C17 | DQA_31 | |
| MDA32 | E17 | DQA_32 | |
| MDA33 | D16 | DQA_33 | |
| MDA34 | F15 | DQA_34 | |
| MDA35 | A15 | DQA_35 | |
| MDA36 | D14 | DQA_36 | |
| MDA37 | F13 | DQA_37 | |
| MDA38 | A13 | DQA_38 | |
| MDA39 | C13 | DQA_39 | |
| MDA40 | E11 | DQA_40 | |
| MDA41 | A11 | DQA_41 | |
| MDA42 | C11 | DQA_42 | |
| MDA43 | F11 | DQA_43 | |
| MDA44 | A9 | DQA_44 | |
| MDA45 | C9 | DQA_45 | |
| MDA46 | F9 | DQA_46 | |
| MDA47 | D8 | DQA_47 | |
| MDA48 | E7 | DQA_48 | |
| MDA49 | A7 | DQA_49 | |
| MDA50 | C7 | DQA_50 | |
| MDA51 | F7 | DQA_51 | |
| MDA52 | A5 | DQA_52 | |
| MDA53 | E5 | DQA_53 | |
| MDA54 | C3 | DQA_54 | |
| MDA55 | E1 | DQA_55 | |
| MDA56 | G7 | DQA_56 | |
| MDA57 | G6 | DQA_57 | |
| MDA58 | G1 | DQA_58 | |
| MDA59 | G3 | DQA_59 | |
| MDA60 | J6 | DQA_60 | |
| MDA61 | J1 | DQA_61 | |
| MDA62 | J3 | DQA_62 | |
| MDA63 | J5 | DQA_63 | |
| MVREFDA | K26 | MVREFDA | |
| MVREFSA | J26 | MVREFSA | |
| MEM_CALRN0 | J25 | MEM_CALRN0 | |
| TESTEN | K7 | TESTEN | |
| MEM_CALRP1/DPC_CALR | J8 | MEM_CALRP1/DPC_CALR | |
| MEM_CALRP0 | K25 | MEM_CALRP0 | |
| DRAM_RST | L10 | DRAM_RST | |
| CLKTESTA | K8 | CLKTESTA | |
| CLKTESTB | L7 | CLKTESTB | |

| | | | |
|---|---|---|---|
| MAA_0 | K17 | MAA0 | 88,89 |
| MAA_1 | J20 | MAA1 | 88,89 |
| MAA_2 | H23 | MAA2 | 88,89 |
| MAA_3 | G23 | MAA3 | 88,89 |
| MAA_4 | G24 | MAA4 | 88,89 |
| MAA_5 | H24 | MAA5 | 88,89 |
| MAA_6 | J19 | MAA6 | 88,89 |
| MAA_7 | K19 | MAA7 | 88,89 |
| MAA_8 | J14 | MAA8 | 88,89 |
| MAA_9 | K14 | MAA9 | 88,89 |
| MAA_10 | J11 | MAA10 | 88,89 |
| MAA_11 | J13 | MAA11 | 88,89 |
| MAA_12 | H11 | MAA12 | 88,89 |
| MAA_13 | G20 | MAA13 | 88,89 |
| MAA_14/BA0 | J16 | A_BA0 | 88,89 |
| MAA_15/BA1 | L15 | A_BA1 | 88,89 |
| MAA_BA2 | G11 | A_BA2 | 88,89 |
| DQMA_0 | E32 | DQMA0 | 88 |
| DQMA_1 | E30 | DQMA1 | 88 |
| DQMA_2 | A21 | DQMA2 | 88 |
| DQMA_3 | C21 | DQMA3 | 88 |
| DQMA_4 | E13 | DQMA4 | 89 |
| DQMA_5 | D12 | DQMA5 | 89 |
| DQMA_6 | E3 | DQMA6 | 89 |
| DQMA_7 | F4 | DQMA7 | 89 |
| RDQSA_0 | H28 | QSAP_0 | 88 |
| RDQSA_1 | C27 | QSAP_1 | 88 |
| RDQSA_2 | A23 | QSAP_2 | 88 |
| RDQSA_3 | E19 | QSAP_3 | 88 |
| RDQSA_4 | E15 | QSAP_4 | 89 |
| RDQSA_5 | D10 | QSAP_5 | 89 |
| RDQSA_6 | D6 | QSAP_6 | 89 |
| RDQSA_7 | G5 | QSAP_7 | 89 |
| WDQSA_0 | H27 | QSAN_0 | 88 |
| WDQSA_1 | A27 | QSAN_1 | 88 |
| WDQSA_2 | C23 | QSAN_2 | 88 |
| WDQSA_3 | C19 | QSAN_3 | 88 |
| WDQSA_4 | C15 | QSAN_4 | 89 |
| WDQSA_5 | E9 | QSAN_5 | 89 |
| WDQSA_6 | C5 | QSAN_6 | 89 |
| WDQSA_7 | H4 | QSAN_7 | 89 |
| ODTA0 | L18 | ODTA0 | 88 |
| ODTA1 | K16 | ODTA1 | 89 |
| CLKA0 | H26 | CLKA0 | 88 |
| CLKA0# | H25 | CLKA0# | 88 |
| CLKA1 | G9 | CLKA1 | 89 |
| CLKA1# | H9 | CLKA1# | 89 |
| RASA0# | G22 | RASA0# | 88 |
| RASA1# | G17 | RASA1# | 89 |
| CASA0# | G19 | CASA0# | 88 |
| CASA1# | G16 | CASA1# | 89 |
| CSA0#_0 | H22 | CSA0#_0 | 88 |
| CSA0#_1 | J22 | | |
| CSA1#_0 | G13 | CSA1#_0 | 89 |
| CSA1#_1 | K13 | | |
| CKEA0 | K20 | CKEA0 | 88 |
| CKEA1 | J17 | CKEA1 | 89 |
| WEA0# | G25 | WEA0# | 88 |
| WEA1# | H10 | WEA1# | 89 |
| PX_EN | AB16 | PX_EN_R | |
| RSVD#G14 | G14 | | |

ROBSON-GP-0

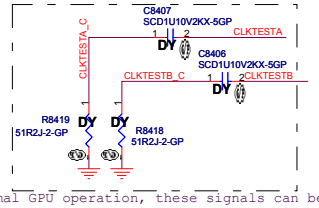
71.ROBSO.M01




11/16 change part reference to R8441 and stuff

11/18 move R8441 before R8440

2010/07/06
Schematics check list:
A pull-down resistor is required.




For normal GPU operation, these signals can be left floating (do not populate the capacitors and resistors).

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size: Custom | Document Number: Enrico Caruso 14 | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 84 of 100

## MEMORY ID Table

| DVPDATA[3:0] | Description |
|---|---|
| 0000 | DDR3 SAMSUNG-K4W1G1646G-BC11(900MHz)64M*16 |
| 0001 | DDR3 Hynix-H5TQ1G63DFR-11C (900MHz) 64M*16 |
| 0010 | DDR3 SAMSUNG K4W2G1646C-HC11 (900MHz) 128M*16 |
| 0011 | DDR3 Hynix-H5TQ2G63BFR-11C (900MHz) 128M*16 |

DVPDATA[0:3] Default:Pull down

X00 2011 0105 DY R8526 R8525 Q8501

For Seymour,
DPC_PVDD is DPC_VDD18
DPC_PVSS and all DPC_VSSR are DP_VSSR

2010/06/11

SSID = VIDEO

0923 Modify for DV14 Config

MEM_ID Control

2010/06/11

2010/07/15 Modify:
Q8501 change to dual 2n7002.
Add R8512,R8521,C8529 for Q8501 pin2 turn on timming control.

2nd = 84.DM601.03F

11/18 Del C8529 to follow DN13

2010/07/07 Remove TP8517,TP8518,TP8506,TP8519,TP8512

Vendor suggest to reserve test point 09/06

GPIO_6,GPIO_15_PWRCNTL_0,GPIO_16_SSIN,GPIO_20_PWRCNTL_1:
Voltage control signals for the core (VDDC and VDDCI).
At Reset, these signals will be inputs with weak internal pull-down resistors.
VBIOS can define all voltage control signals to be either 3.3-V or open drain outputs (all signals must be the same type). The output state (high/low) of these signals is programmable for each PowerPlay state.

12/17 dummy R8523 for panel interface unused.

2010/07/07
Change to RSVD based on DS v3.05

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

68.00143.181
2nd = 68.00214.211

68.00143.181
2nd = 68.00214.211

X00 9/23
Voltage Swing:1.8V

2010/07/06
Schematics check list: X00 20101230 DY
A 1~M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.

82.30034.641
2nd = 82.30034.651
3rd = 82.30034.681

68.00084.F81
2nd = 68.00217.701

Change to DY 9/20

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

Seymou XT S3 PN:71.SEYMR.M01

71.ROBSO.M01

12/20 NC R-,G-,B- on SSI and try to co-layout with Rosbson in PT stage

12/20 Add R8504 for Robson.

12/9 chnage R8501 to ROB

0820

0723 Add SMBUS

AUXP PD 100K
AUXN PD 100K
Draw on EDP circuit page

12/16 change R8507, R8505 and R8513 to ROB

LVDS Interface

71.ROBSO.M01

68.00084.F81
2nd = 68.00217.701

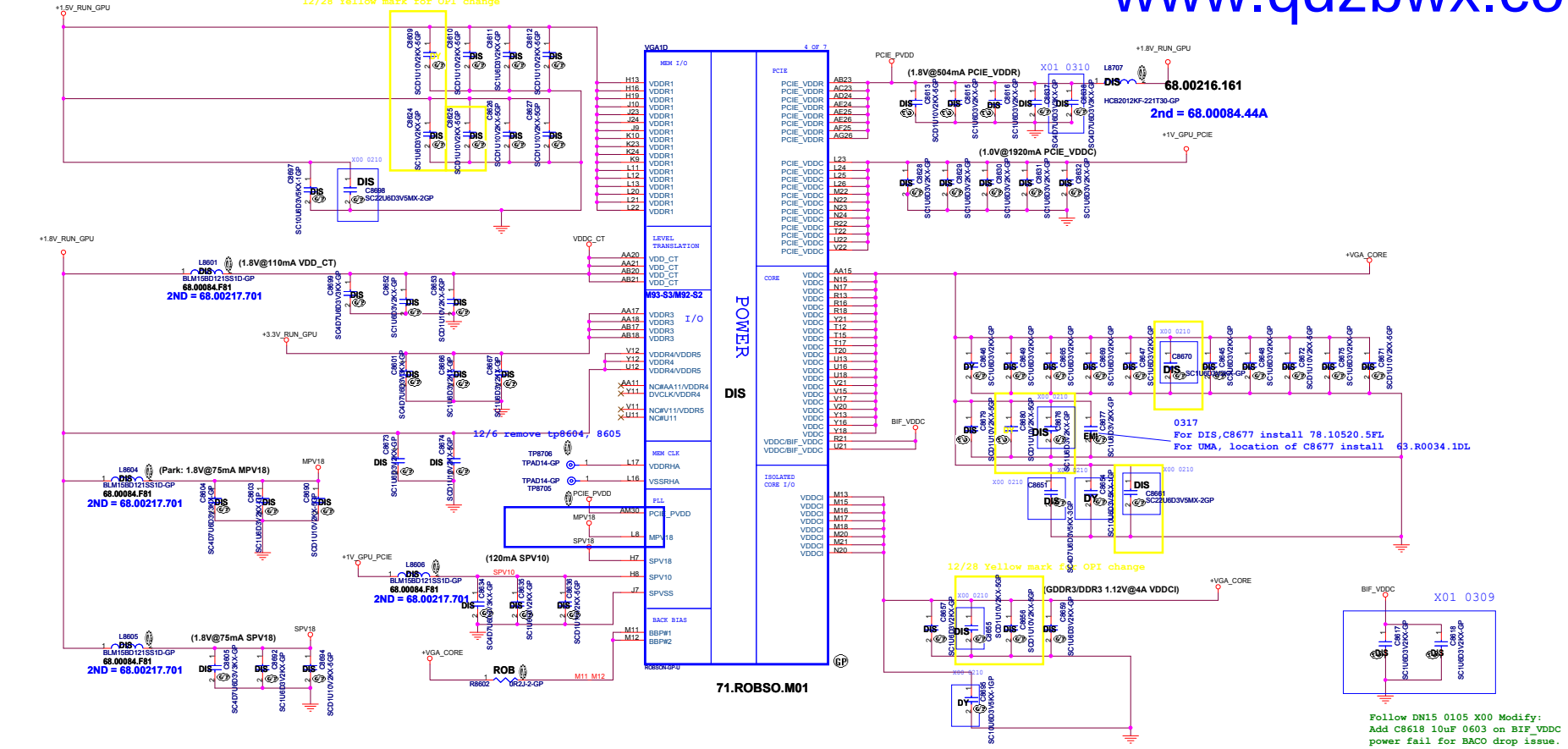
<Core Design>

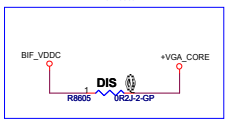
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)
Size: A2 | Document Number: Enrico Caruso 14 | Rev: X00
Date: Wednesday, March 23, 2011 | Sheet 85 of 109

SSID = VIDEO






X01 0309 DEL BACO function

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size: A2 | Document Number: Enrico Caruso 14 | Rev: X00

Date: Tuesday, March 22, 2011 | Sheet 86 of 100

**SSID = VIDEO**

VGA1E 5 OF 7

PCIE_VSS: AA27, AB24, AB32, AC24, AC26, AC27, AD25, AD32, AE27, AF32, AG27, AH32, K28, K32, L27, M32, N25, N27, P25, P32, R27, T25, T32, U25, U27, V32, W25, W26, W27, Y25, Y32

GND: M6, N11, N12, N13, N16, N18, N21, P6, P9, R12, R15, R17, R20, T13, T16, T18, T21, T6, U15, U17, U20, U9, V13, V16, V18, Y10, Y15, Y17, Y20

GND: A3, A30, AA13, AA16, AB10, AB15, AB6, AC9, AD6, AD8, AE7, AG12, AH10, AH28, B10, B12, B14, B16, B18, B20, B22, B24, B26, B6, B8, C1, C32, E28, F10, F12, F14, F16, F18, F2, F20, F22, F24, F26, F6, F8, G10, G27, G31, G8, H14, H17, H2, H20, H6, J27, J31, K11, K2, K22, K6, T11, R11

GND/EVDDQ: GND, GND/EVDDQ, GND/EVDDQ

VSS_MECH: A32 VSS_MECH1, AM1 VSS_MECH2, AM32 VSS_MECH3

TP8704TPAD14, TP8702TPAD14, TP8703TPAD14

N11_GND, N12_GND

GND

DIS

ROBSON-GP-U

71.ROBSO.M01

**Vendor suggest 09/23**

LVDS mode(1.8V@440mA DPEF_VDD18)
DP mode(1.8V@300mA DPEF_VDD18)

+1.8V_RUN_GPU, +1V_GPU_PCIE

R8711 DIS 0R2J-2-GP

R8713 DIS 0R2J-2-GP

C8717 SC4D7U6D3V3KX-GP, C8718 SC1U6D3V2KX-GP, C8719 SCD1U10V2KX-5GP

C8721 SC4D7U6D3V3KX-GP, C8720 SC1U6D3V2KX-GP, C8725 SCD1U10V2KX-5GP

DPEF_VDD18: AG15, AG16

DPEF_VDD10: AG20, AG21

AG14, AH14, AM14, AM16, AM18

DPEF_VDD18: AE16, AG17

DPEF_VDD10: AE22, AG22

AF23, AG23, AM20, AM22, AM24

LVDS mode(1V@240mA DPEF_VDD10)
DP mode(1V@220mA DPEF_VDD10)

2010/07/09 N11 and N12: in Seymour is NC

N11_GND R8702 0R2J-2-GP N12_GND

R8704 0R2J-2-GP

DIS R8701 150R2F-1-GP DPCD_CALR AF17

DPEF_VDD18, DPEF_VDD10

AG18, AF19, AG19, AF20

VGA1G 7 OF 7

DP E/F POWER

DPE_VDD18, DPE_VDD10, DPE_VSSR, DPEF_CALR, DPE_PVDD, DPE_PVSS, DPF_PVDD, DPF_PVSS

DP A/B POWER

DPA_VDD18: AE11, AF11

DPA_VDD10: AF6, AF7

DPA_VSSR: AE1, AE3, AG1, AG6, AH5

DPB_VDD18: AE13, AF13

DPB_VDD10: AF8, AF9

DPB_VSSR: AE10, AG9, AH8, AM6, AM8

DPAB_CALR AE10

DP PLL POWER

DPA_PVDD: AG8, AG7

DPB_PVDD: AG10, AG11

DIS

ROBSON-GP-U

71.ROBSO.M01

**Vendor suggest 09/23**

(1.8V@300mA DPAB_VDD18) R8714 DIS 0R2J-2-GP

C8714 SCD1U10V2KX-5GP, C8712 SC1U6D3V2KX-GP, C8713 SC4D7U6D3V3KX-GP

(1.0V@220mA DPAB_VDD10) R8716 DIS 0R2J-2-GP

C8702 SCD1U10V2KX-5GP, C8703 SC1U6D3V2KX-GP, C8705 SC10U6D3V5KX-1GP

R8703 150R2F-1-GP DIS

**Vendor suggest 9/23**

+1.8V_RUN_GPU R8715 DIS 0R2J-2-GP (1.8V@150mA DPB_VDD18) DPB_VDD18

11/18 Del R8709, C8710,C8711

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

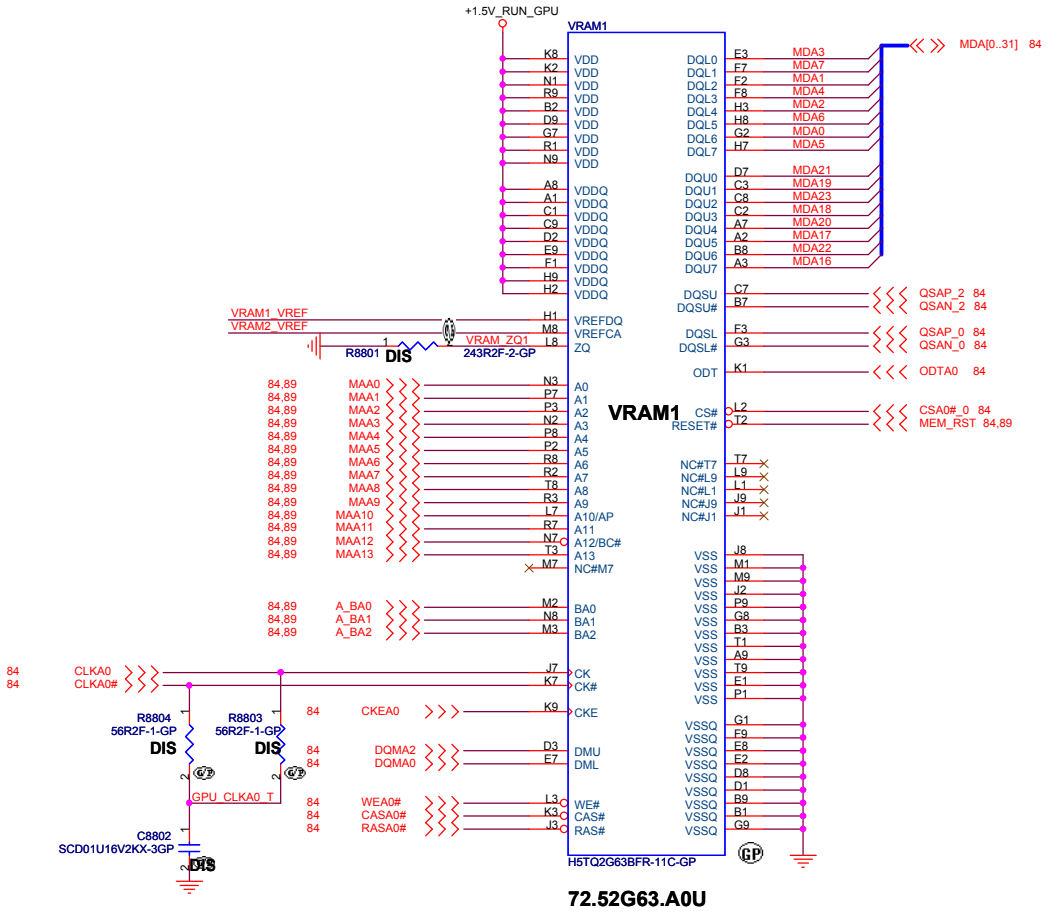
Title: GPU_DPPWR/GND(5/5)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: X00

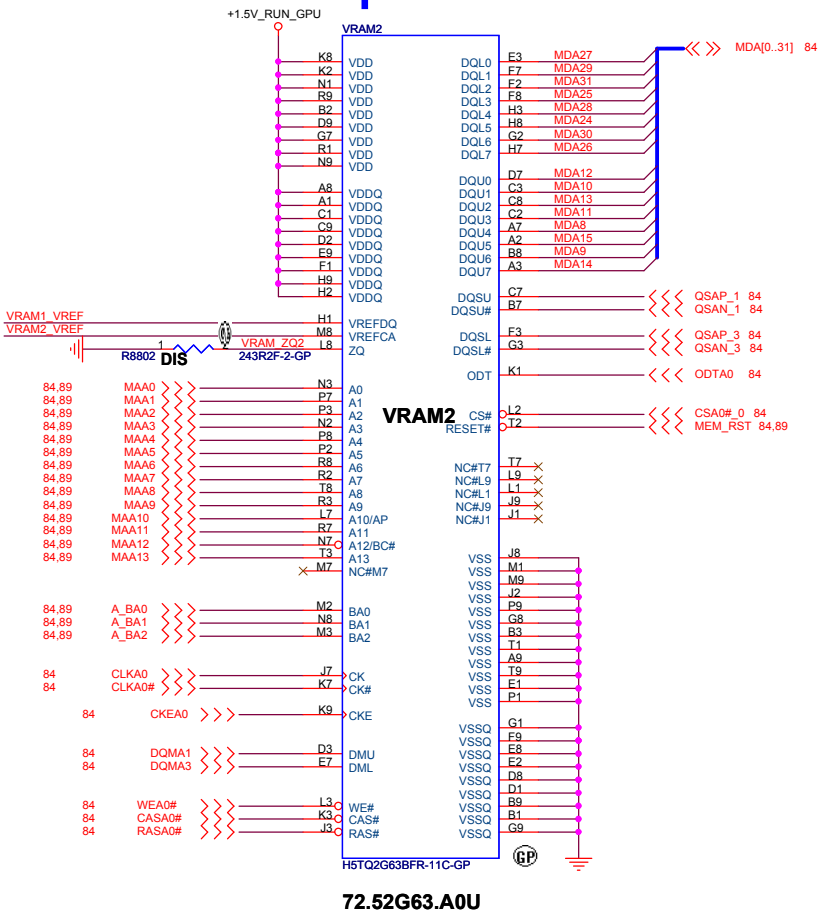
Date: Tuesday, March 22, 2011 | Sheet 87 of 100

SSID = VIDEO






72.52G63.A0U

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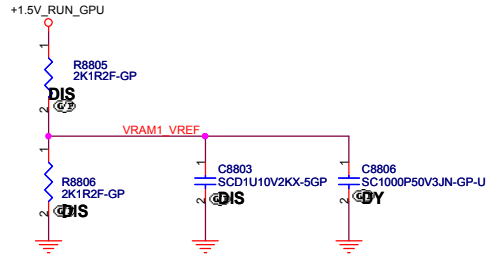


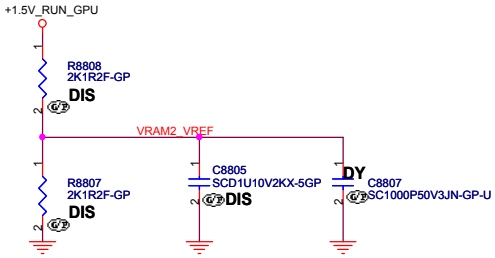


<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

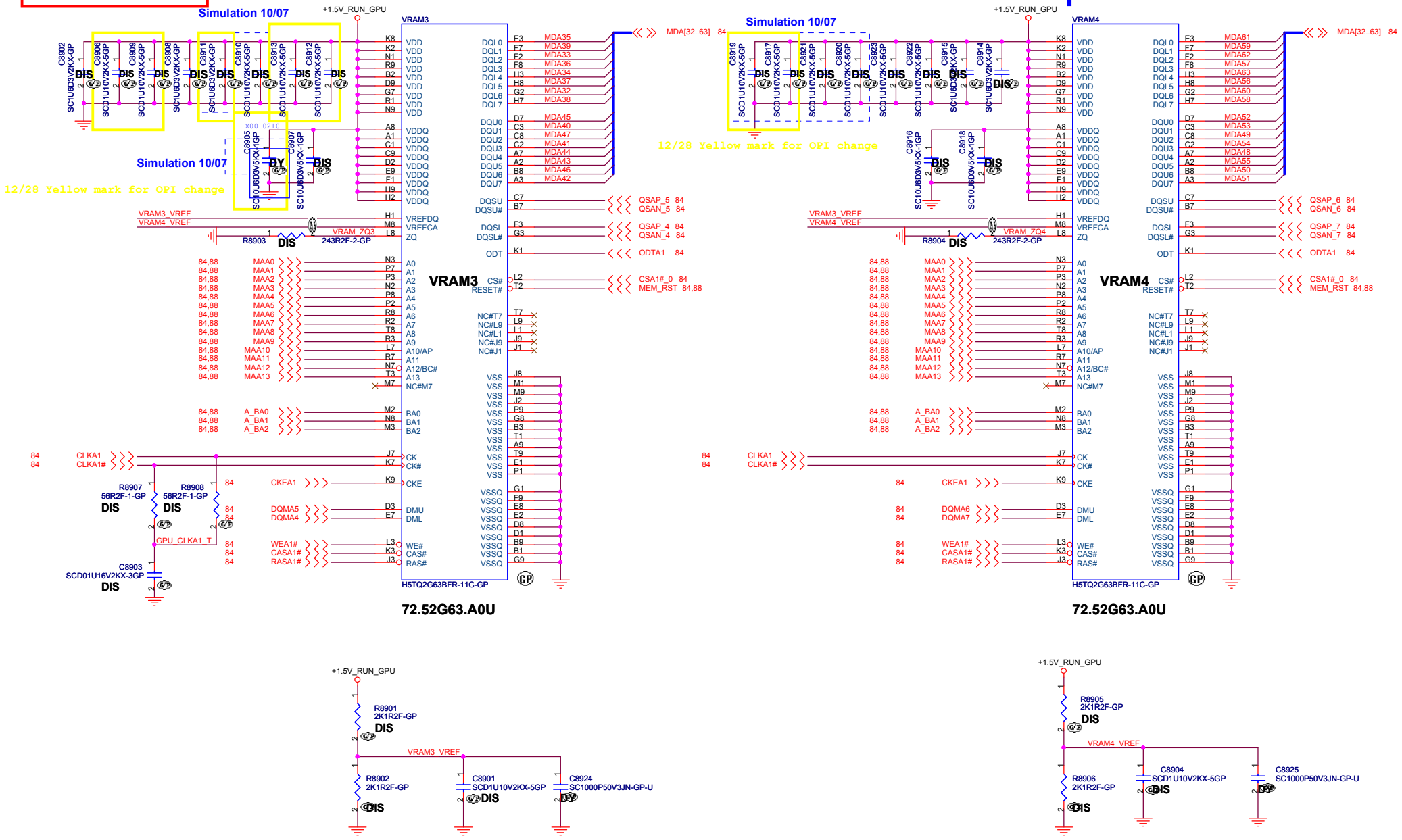
Title: GPU-VRAM1,2 (1/4)

Size: Custom | Document Number: Enrico Caruso 14 | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 88 of 100

SSID = VIDEO












<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: Enrico Caruso 14 | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 89 of 100

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: X00

Date: Thursday, January 06, 2011 | Sheet 90 of 100

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

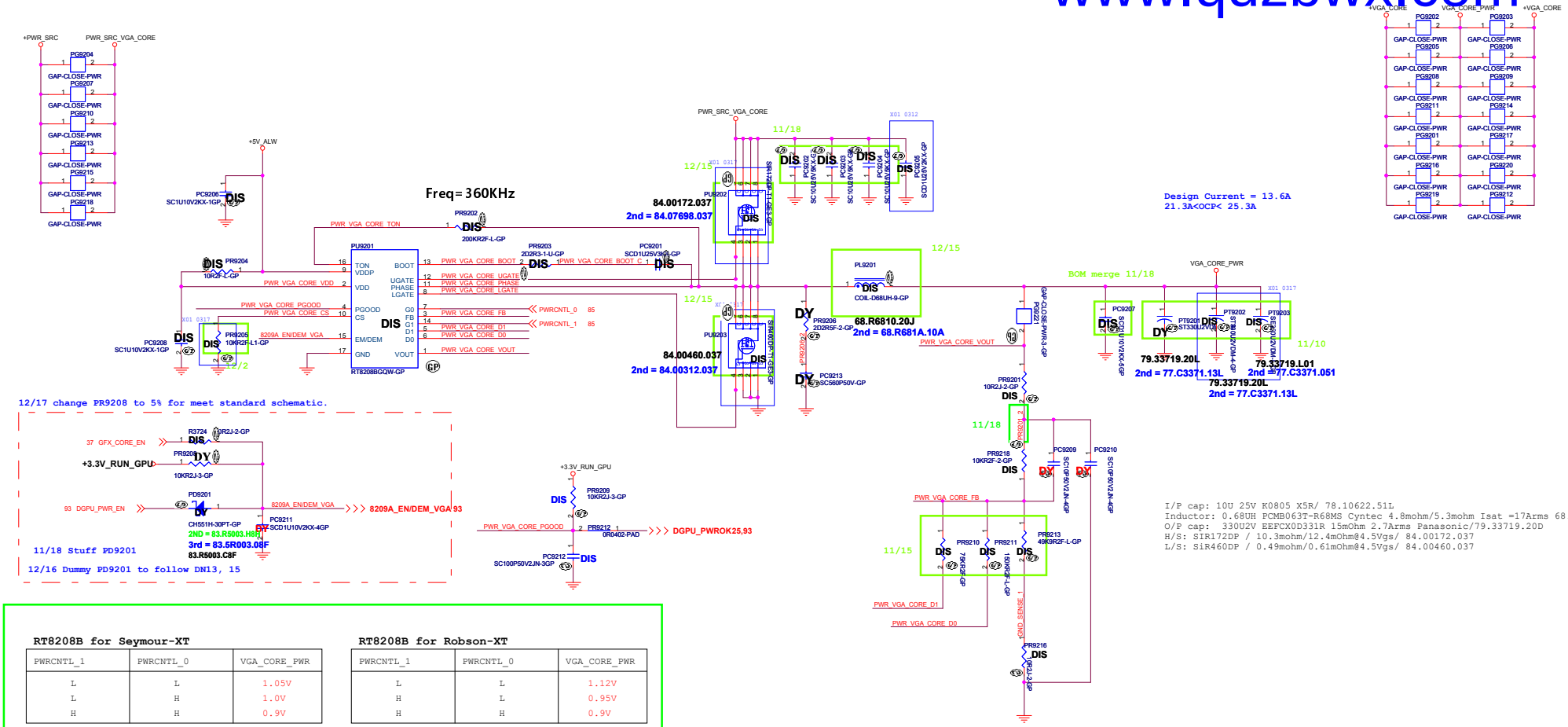
Title: GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: X00

Date: Thursday, January 06, 2011 | Sheet 91 of 100

SSID = PWR.Plane.Regulator_VGACORE






**RT8208B for Seymour-XT**

| PWRCNTL_1 | PWRCNTL_0 | VGA_CORE_PWR |
|---|---|---|
| L | L | 1.05V |
| L | H | 1.0V |
| H | H | 0.9V |

**RT8208B for Robson-XT**

| PWRCNTL_1 | PWRCNTL_0 | VGA_CORE_PWR |
|---|---|---|
| L | L | 1.12V |
| H | L | 0.95V |
| H | H | 0.9V |

For Robson:
PR9218=10K
PR9213=49.9K
PR9211=150K
PR9210=44.2K

Vout=0.75V*(R1+R2)/R2

11/15

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

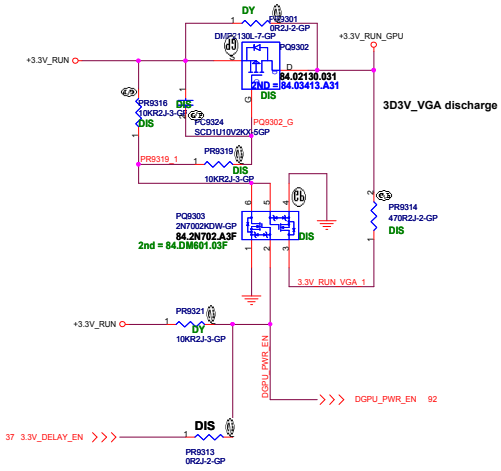
Title: RT8208B +VGA_CORE

Size: A2 | Document Number: Enrico Caruso 14 | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 92 of 100

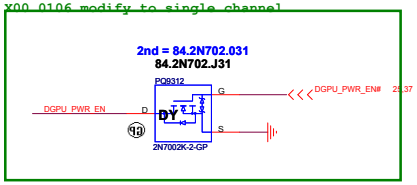
## 3D3V_S0 to 3D3V_VGA_S0 Transfer

Change DUMMY Reference Name to PX_BACO



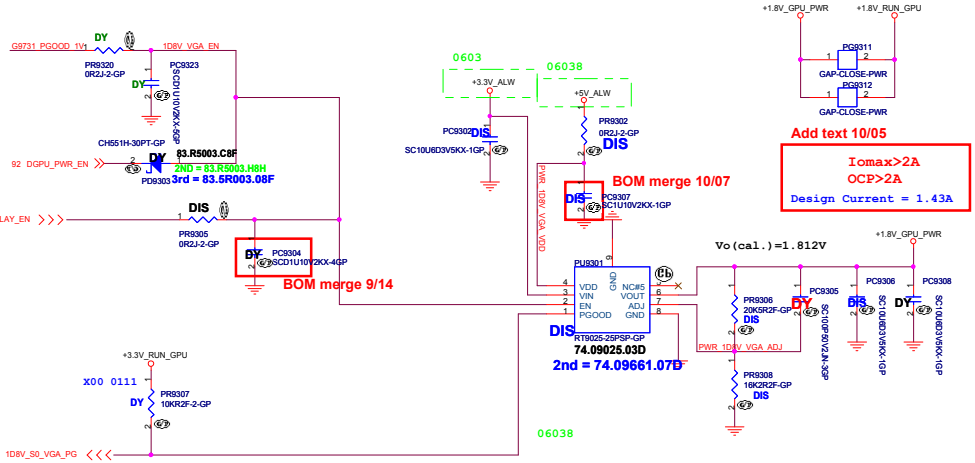

| | DGPU_PWR_EN# |
|---|---|
| dGPU mode | L |
| IGPU | H |
| IGPU with BACO | L |

X00_0106 modify to single channel




11/18 Merge PQ9803 PQ9804 to PQ9312

## +1.8V_RUN_GPU



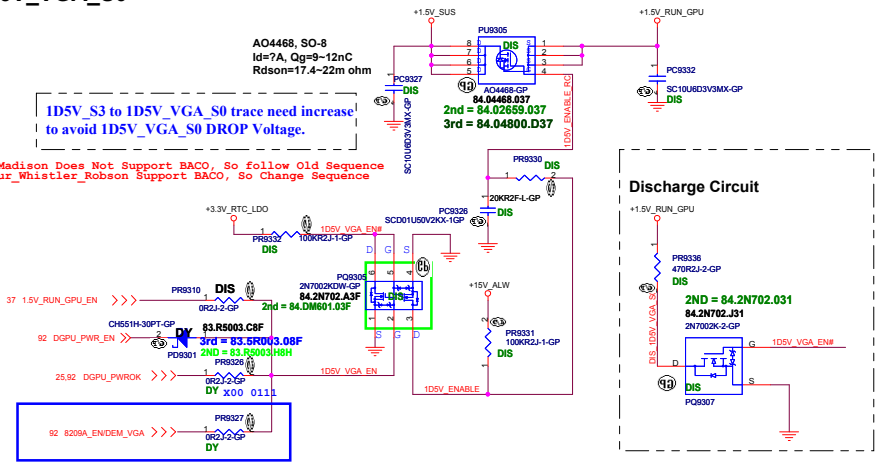

## 1D5V_VGA_S0

change low Rds(on) MOSFET

AO4468, SO-8
Id=7A, Qg=9~12nC
Rdson=17.4~22m ohm

1D5V_S3 to 1D5V_VGA_S0 trace need increase to avoid 1D5V_VGA_S0 DROP Voltage.

Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence




### Discharge Circuit




11/18 Add PR9327 for 8209A_EN/DEM_VGA turn on 1D5V_VGA_S0 power.

## G9731 for 1V_VGA_S0

Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence

1V_VGA_S0
Design current = 2.445A

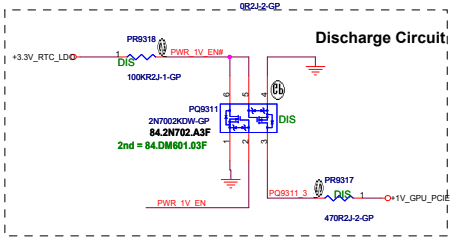
Vout=0.8V*(R1+R2)/R2= 1.0036V

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core




### Discharge Circuit




<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | DISCRETE VGA POWER | |
| Size: A2 | Document Number: Enrico Caruso 14 | Rev: X00 |
| Date: Wednesday, March 23, 2011 | Sheet 93 of 100 | |

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: *X00*

Date: Thursday, January 06, 2011 | Sheet 94 of 100

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: *X00*

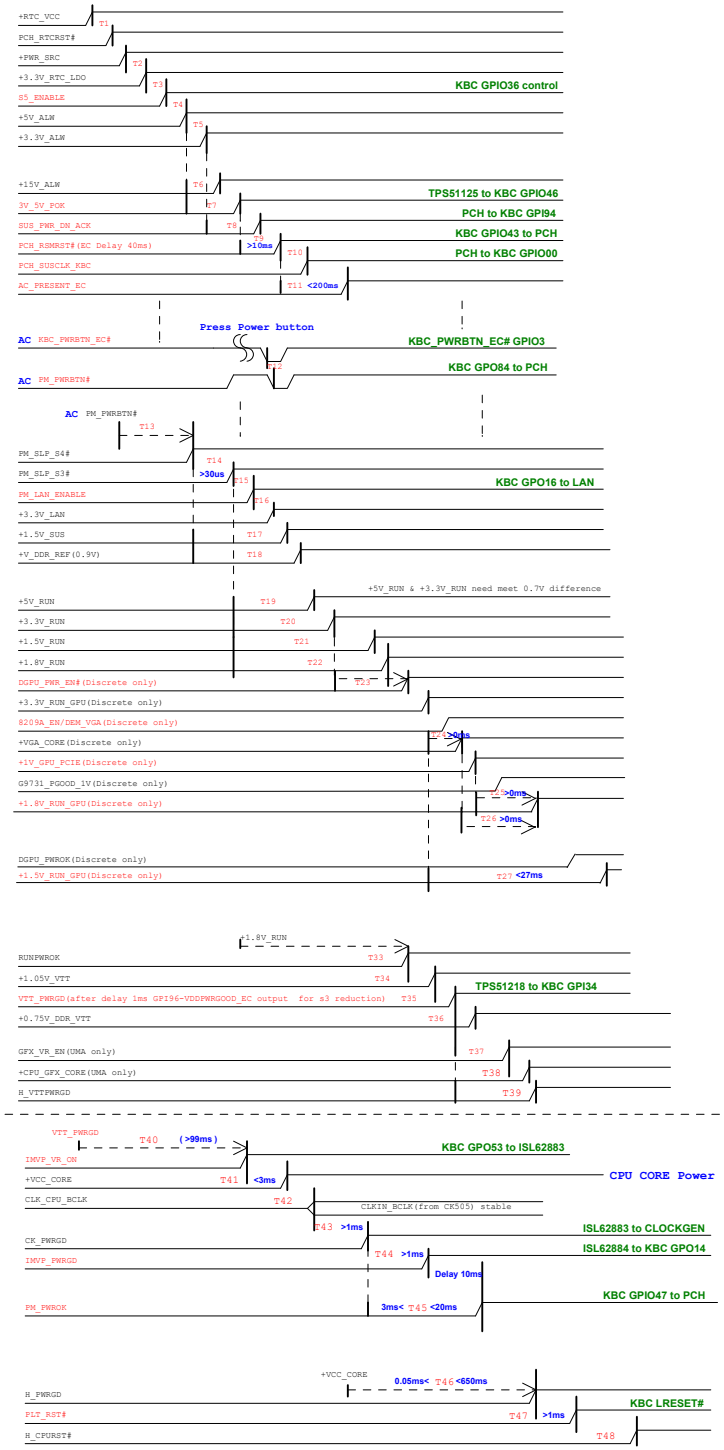
Date: Thursday, January 06, 2011 | Sheet 95 of 100

# DV14 Calpella UMA&DIS Power Up Sequence



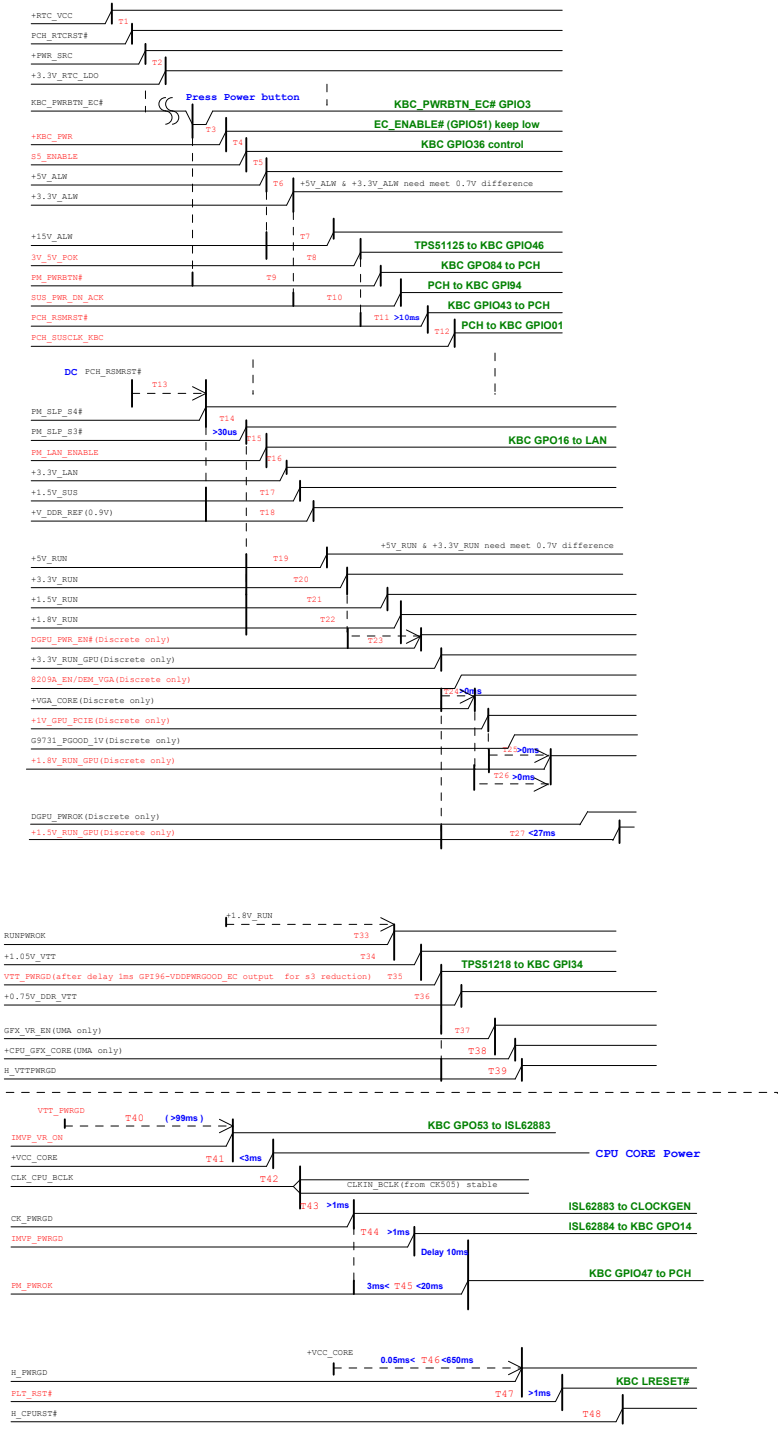
## (AC mode)

red word: KBC GPIO




## (DC mode)

red word: KBC GPIO





<Core Design>
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
File: Power Sequence
Size: A1 | Document Number: DV14 CP UMA+DIS | Rev: X00
Date: Monday, February 28, 2011 | Sheet 98 of 100

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

# Change History

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

Date: Thursday, January 06, 2011 Sheet 97 of 100

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

# Change History

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

Date: Thursday, January 06, 2011 Sheet 98 of 100

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

# Change History

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

Date: Thursday, January 06, 2011 Sheet 99 of 100

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

# Change History

| Size | Document Number | Rev |
|---|---|---|
| A3 | DV14 CP UMA+DIS | X00 |

Date: Thursday, January 06, 2011 Sheet 100 of 100