MODEL NAME : VAW00
PROJECT CODE : ANRVAW0000
PCB NO : LA-9104P (Thames XT)

DA60000VV00 LA-9104P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

ZZZ R1@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P
DAZ0SZ00200

ZZZ GCER3@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P GOLD A31 !
DAZ0SZ00201

ZZZ TRIR3@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P TRIPOD A31 !
DAZ0SZ00202

ZZZ HANNR3@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P HANNSTARB A31 !
DAZ0SZ00203

ZZZ ZDTR3@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P ZDT A31 !
DAZ0SZ00204

Dell / Compal Confidential

Schematic Document

Intel Chief River
Ivy Bridge(BGA) + Panther Point
OAK 15" UMA/DIS AMD Thames XT

2012-08-22
Rev: 1.0

46@ : for 46 level
@ : Nopop Component
CONN@ : Connector Component
KB9012@ : ENE KB9012 Implemented
UMA@ : Only for UMA
EMC@ : EMI/ESD parts

GCLK@ : Green CLK implemented
GCLKUMA@ : Green CLK for UMA
GCLKDIS@ : Green CLK for DIS
XTAL@ : X'tal implemented
XTALDIS@ : X'tal with DIS implemented

R1@ : R1 P/N
R3@ : R3 P/N

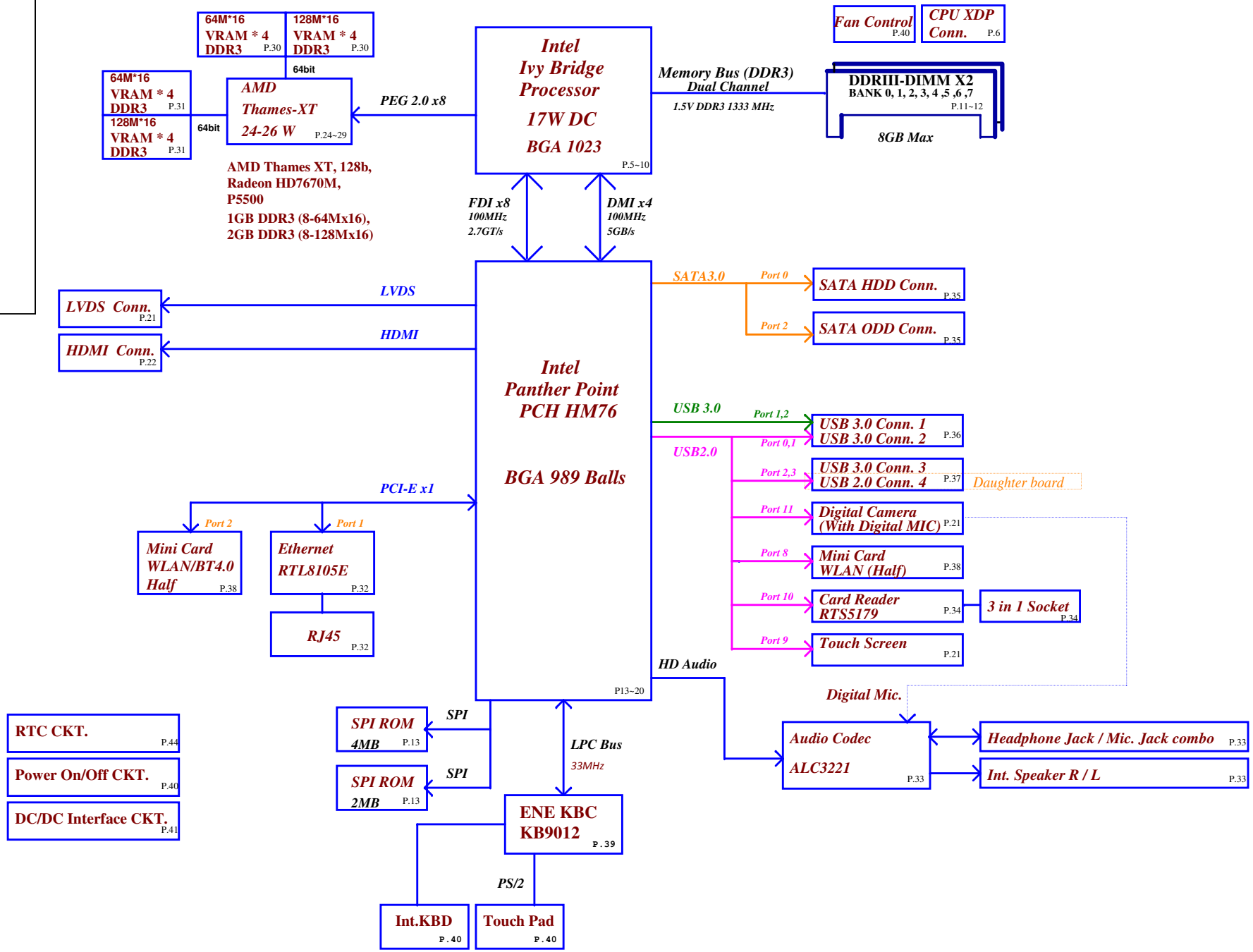
i3R1@ : CPU i3-3217 1.8G
i3VOSR1@ : CPU i3-2365 1.4G
i5R1@ : CPU i5-3317 1.7G
i7R1@ : CPU i7-3517 1.9G
CELR1@ : CPU Celeron 887 1.5G
PENR1@ : CPU Pentium 997 1.6G

DIS@ : Only for Discrete
TH@/THR1@ : Thames-XT
MS@/MSR1@ : Mars Pro
X76@ :
SPI-ROM & VRAM Group

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: Cover Page
Size: Custom | Document Number: LA-9104P | Rev: 1.0
Date: Wednesday, August 29, 2012 | Sheet 1 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: Block diagram

Size	Document Number	Rev
	LA-9104P	1.0

Date: Wednesday, August 29, 2012 Sheet 2 of 57

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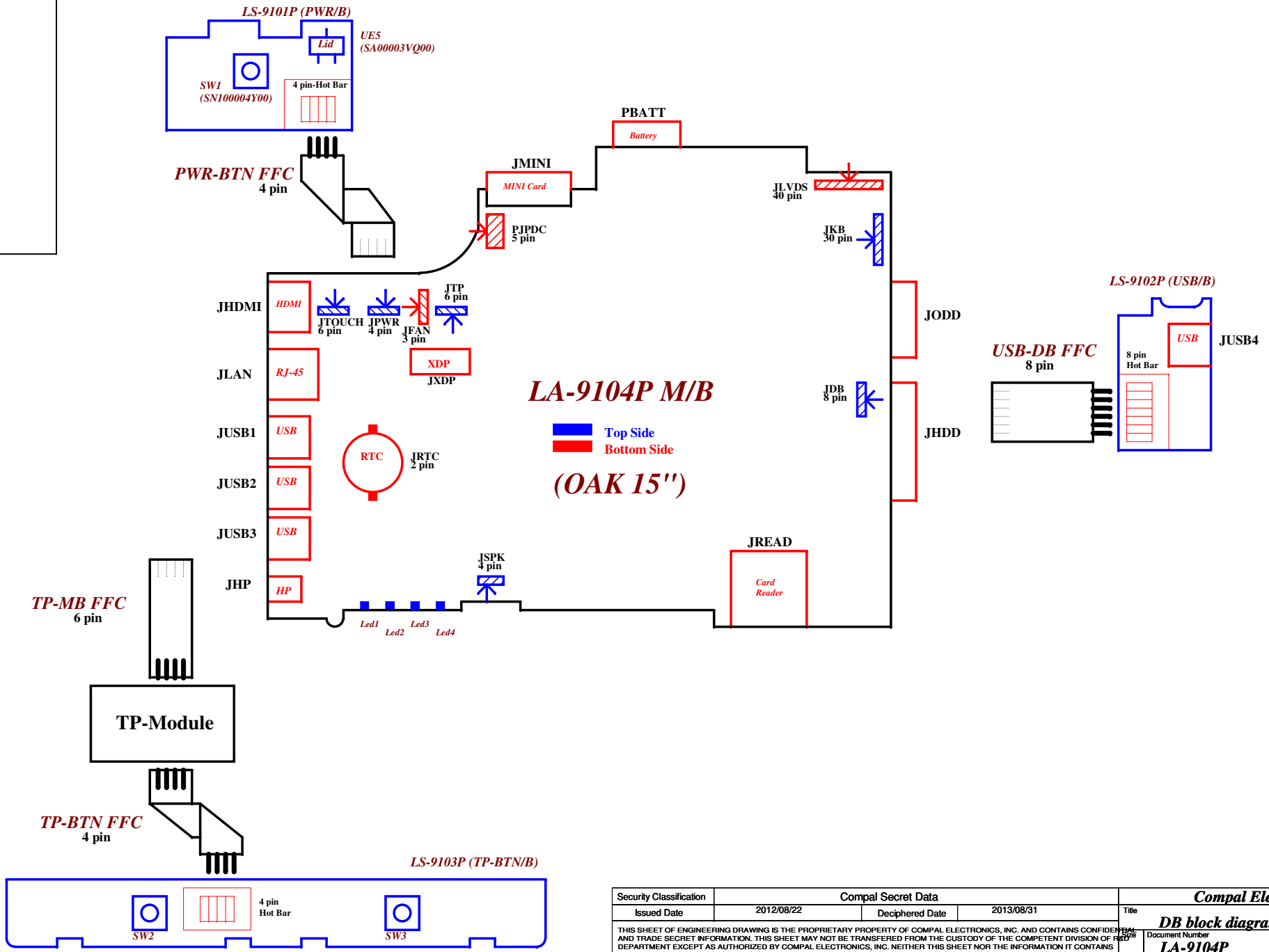
Project Code : VAW00
File Name : LA-9104P



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **DB block diagram**

Size: | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 3 of 57

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

ID	PCB Revision		
	UMA	THM	MARS
0	0.1		
1		0.1	0.1
2	0.2		
3		0.2	0.2
4	0.3		
5		0.3	0.3
6	1.0		
7		1.0	1.0

Project ID Table

ID	Project Revision
0	
1	
2	
3	
4	
5	UMA
6	DIS THAMES
7	DIS MARS PRO

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	

Link

PCH	USB PORT#	DESTINATION
	0	USB conn.2
	1	USB conn.1
	2	USB conn.3
	3	USB conn.4 (DB)
	4	NC
	5	NC
	6	NC
	7	NC
	8	MINI CARD (WLAN)
	9	Touch Screen
	10	Card Reader
	11	Camera
	12	NC
	13	NC

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100 LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

Symbol Note :

: means Digital Ground

: means Analog Ground

Compal Electronics, Inc.

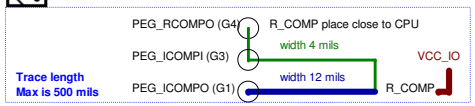
Title: Notes List

Size: B | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 4 of 57

UC1 i3R1@ SA00005L52L AV8063801058401-SR0N9-L1-1.8G_BGA1023~D
UC1 i3R3@ SA00005L53L AV8063801058401-SR0N9-L1-1.8G_BGA1023~D
UC1 i3VOSR1@ SA00005UH1L AV8062701313000-SR0U3-J1-1.4G_BGA1023~D
UC1 i3VOSR3@ SA00005UH2L AV8062701313000-SR0U3-J1-1.4G_BGA1023~D
UC1 i5R3@ SA00005K62L AV8063801058002-SR0N8-L1-1.7G_BGA1023~D
UC1 i7R1@ SA00005K53L AV8063801057605-SR0N6-L1-1.9G_BGA1023~D
UC1 i7R3@ SA00005K52L AV8063801057605-SR0N6-L1-1.9G_BGA1023~D
UC1 CELR1@ SA00006021L AV8062701085401-SR0VA-Q0-1.5G_BGA1023~D
UC1 CELR3@ SA00006022L AV8062701085401-SR0VA-Q0-1.5G_BGA1023~D
UC1 PENR1@ SA00005ZZ1L AV8062701084801-SR0V5-Q0-1.6G_BGA1023~D
UC1 PENR3@ SA00005ZZ2L AV8062701084801-SR0V5-Q0-1.6G_BGA1023~D

(1)PEG_RCOMPO (G4) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC1.
(2)PEG_ICOMPO use 12mil connect to RC1



SA00005K63L
UC1A i5R1@
AV8063801058002-SR0N8-L1-1.7G_BGA1023~D

DMI
FDI (Q) FDI
PCI EXPRESS -- GRAPHICS
eDP

+VCCP
RC2 24.9_0402_1%
PEG_COMP

PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils
- typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near
balls and routed with typical impedance <25 mohms

+VCCP
RC36 24.9_0402_1% +EDP_COM
RC158 10K_0402_5%

UC1I i5R1@
VSS
NCTF
AV8063801058002-SR0N8-L1-1.7G_BGA1023~D

@ RC20 1K_0402_5%

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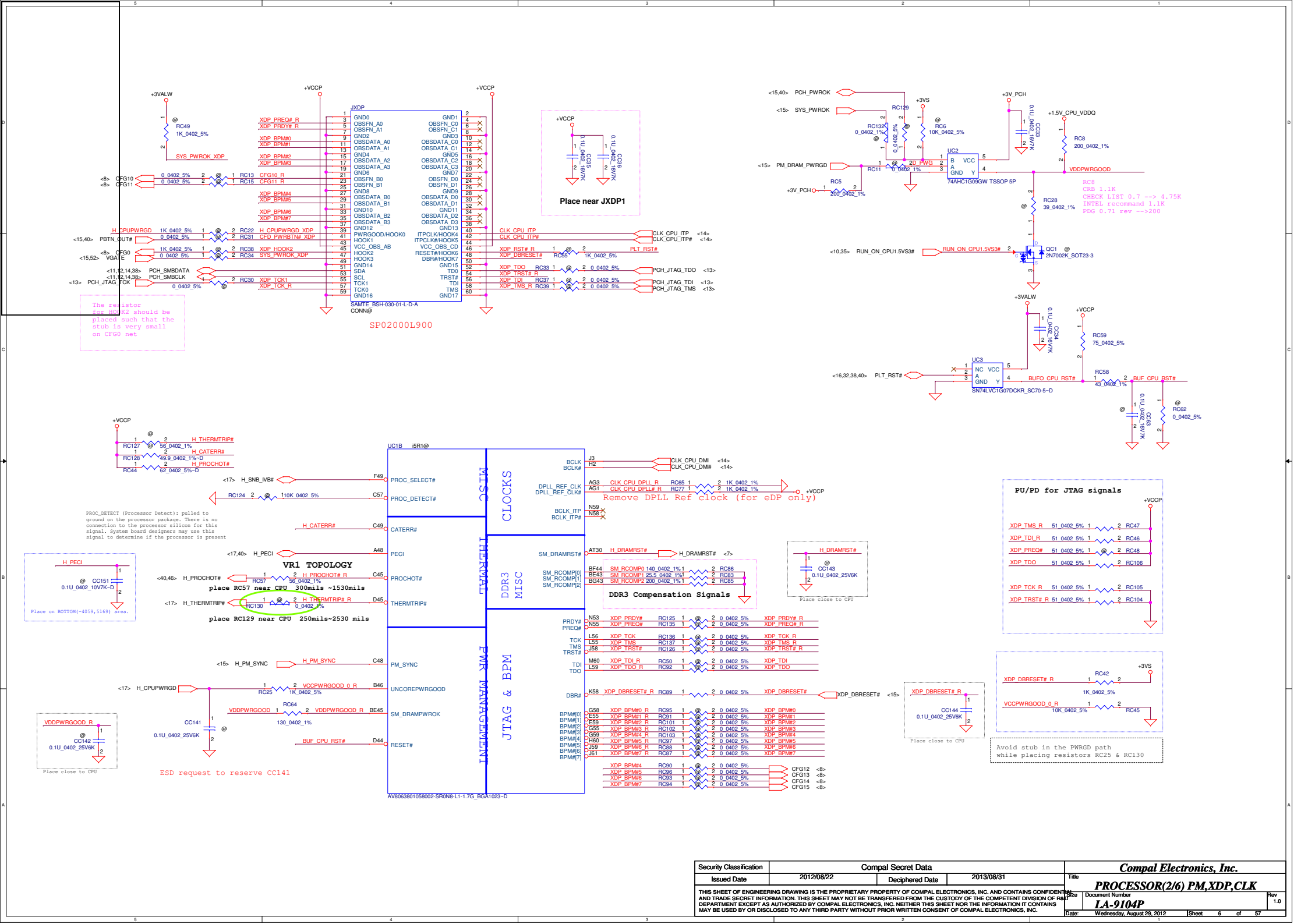
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.
Title: PROCESSOR(1/6) DMI,FDI,PEG
Size: Document Number: LA-9104P
Rev: 1.0
Date: Wednesday, August 29, 2012 Sheet 5 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.	
Title	PROCESSOR(2/6) PM,XDP,CLK
Size	Document Number: LA-9104P
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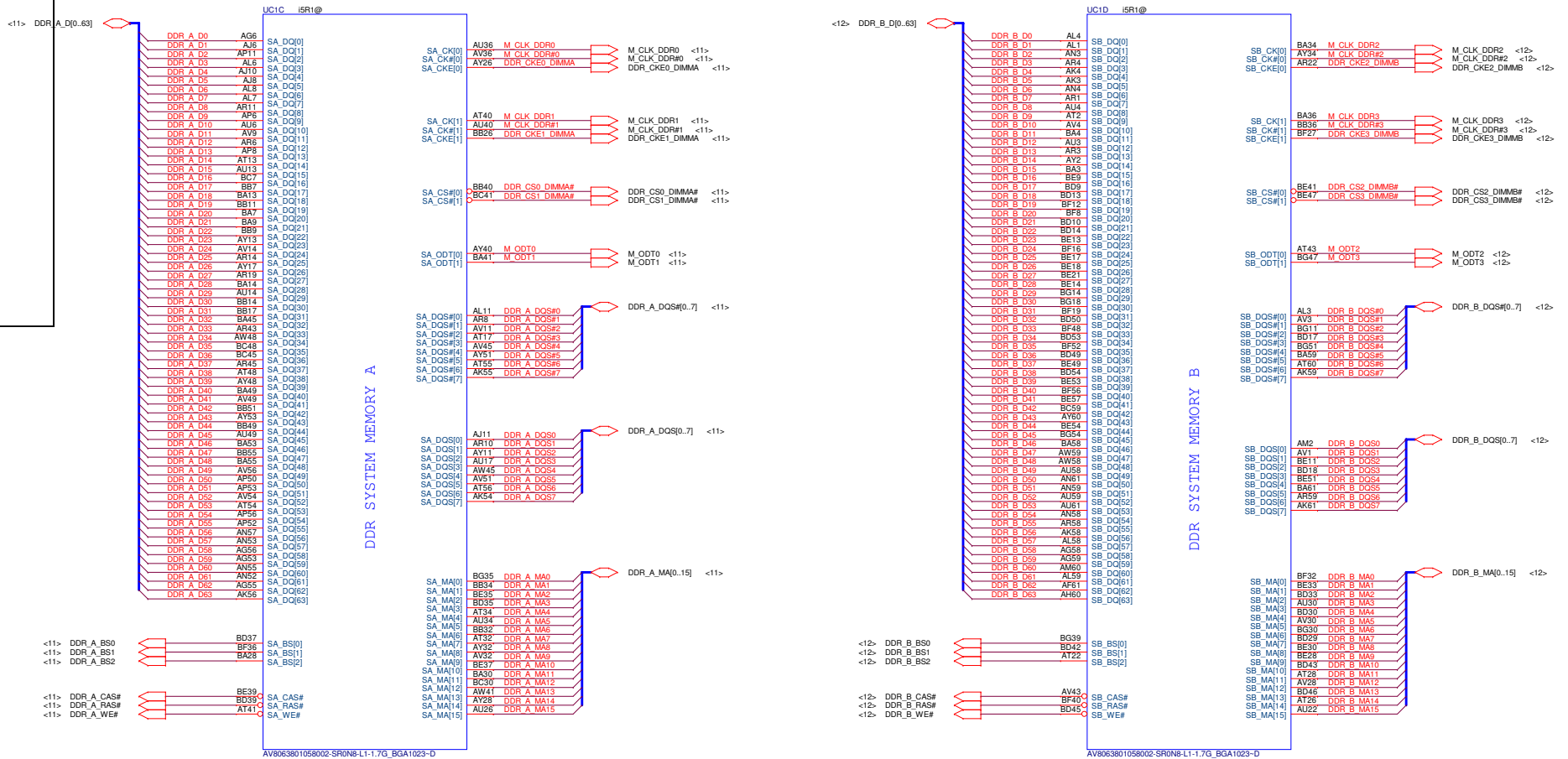
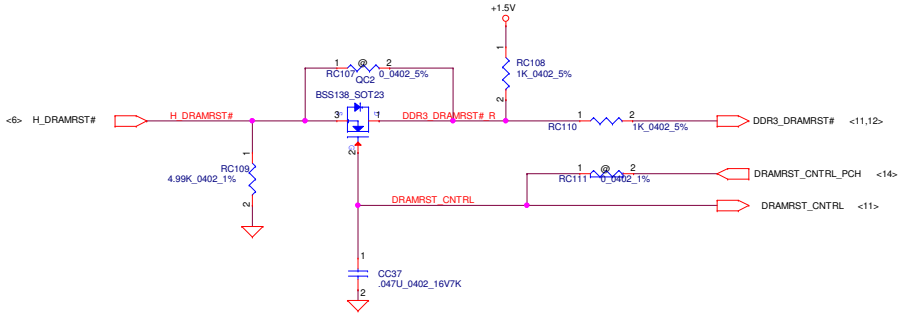
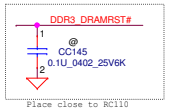
Date:	Wednesday, August 29, 2012
Sheet	6 of 57

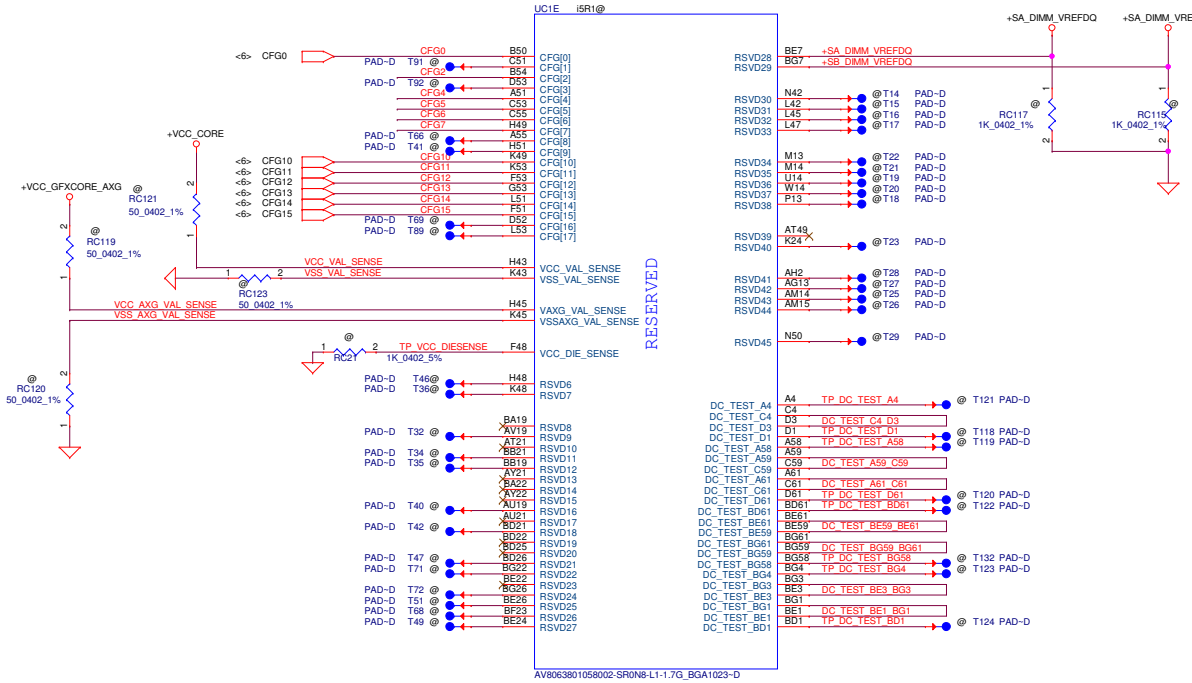


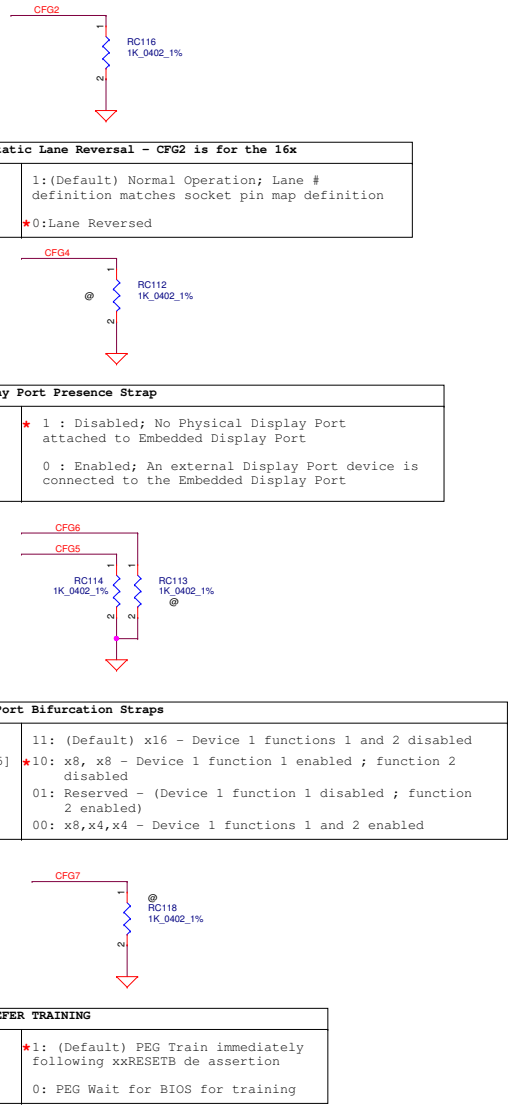




Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title: PROCESSOR(3/6) DDRIII
Size	Document Number: LA-9104P			Rev: 1.0
Date: Wednesday, August 29, 2012	Sheet 7 of 57			

CFG Straps for Processor





Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

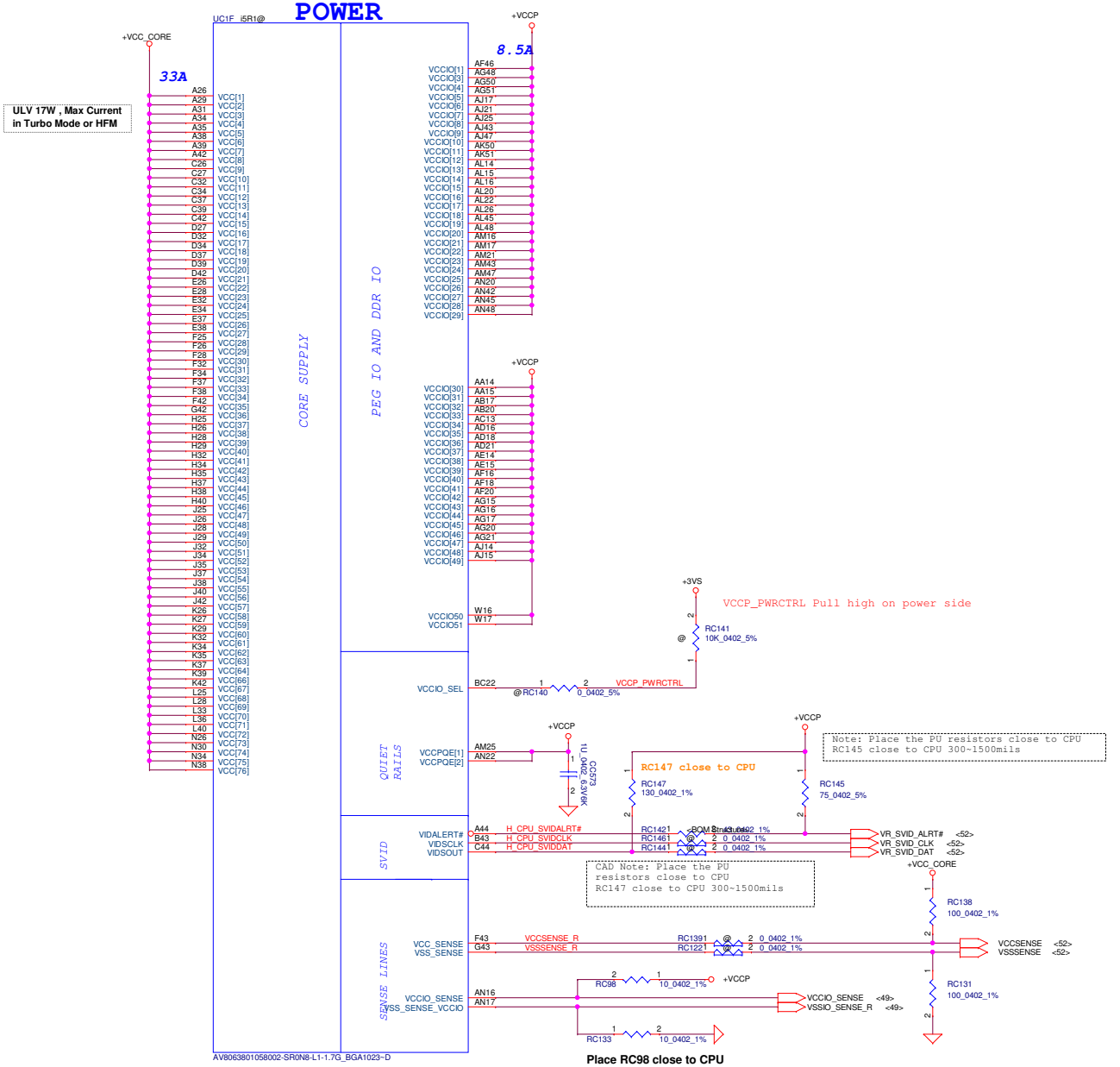
Compal Electronics, Inc.

Title: PROCESSOR(4/6) RSVD,CFG

Size | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 8 of 57

POWER



Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65~1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0~1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65~0.9	6
+1.5V_MEM	1.5	12~16 ★

★ Description

5A to Mem controller(+1.5V_CPU_VDDQ)
5~6A to 2 DIMMs/channel
2~5A to +1.5V_RUN & +0.75V_DDR_VTT

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

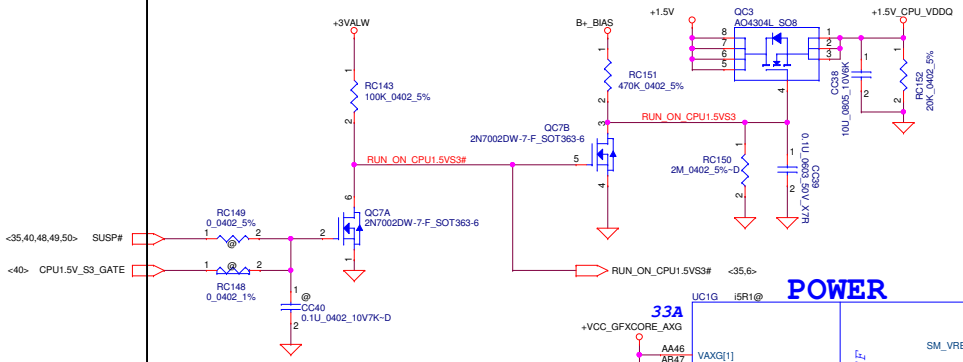
Compal Electronics, Inc.

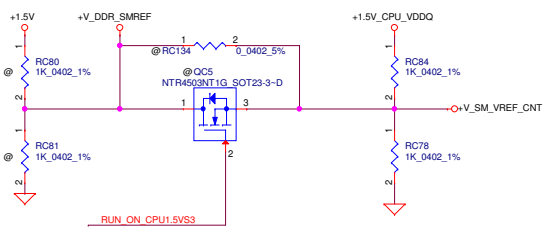
Title: PROCESSOR(5/6) PWR,BYPASS

Size | Document Number: LA-9104P | Rev: 1.0

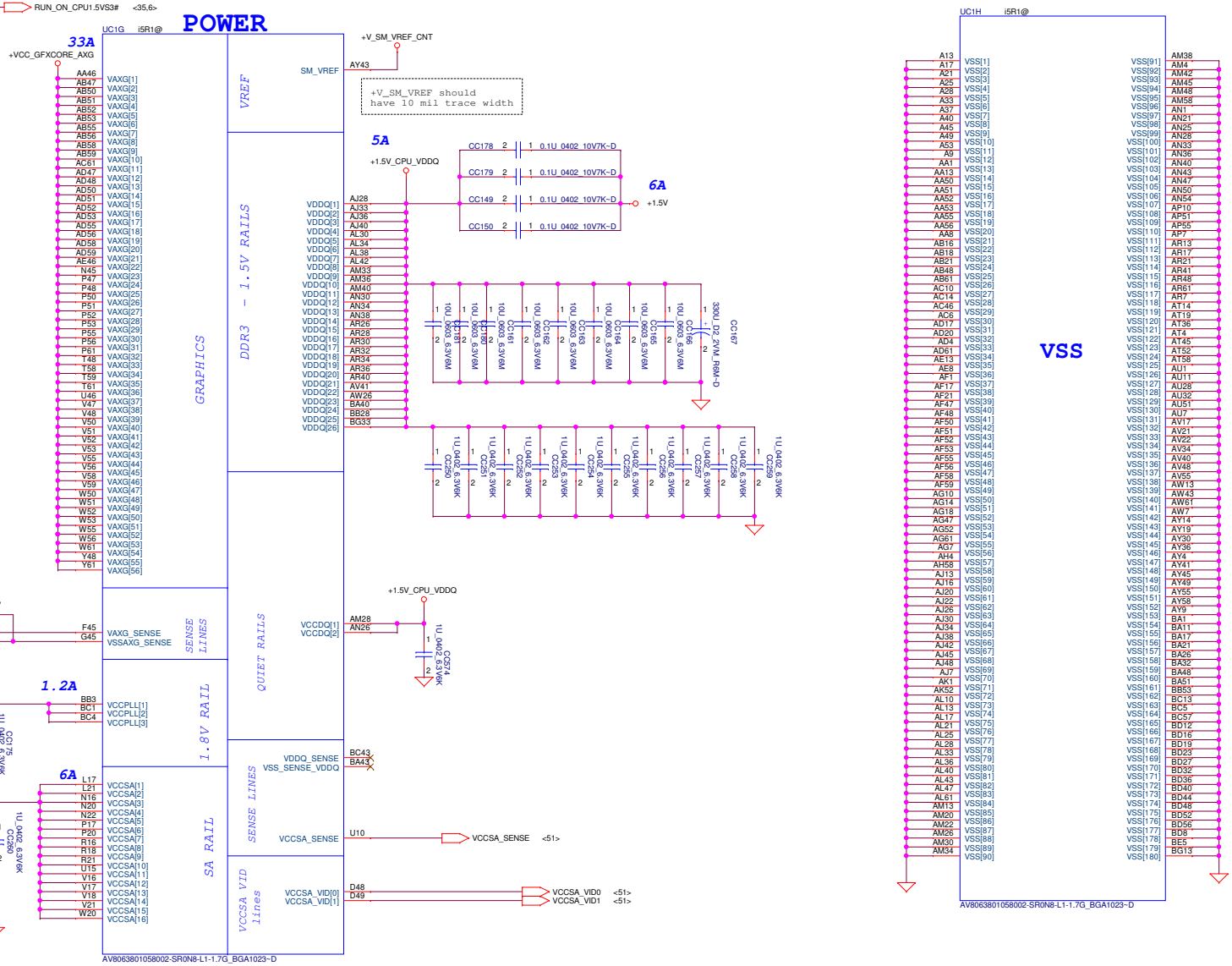
Date: Wednesday, August 29, 2012 | Sheet 9 of 57

+1.5V_CPU_VDDQ Source





POWER



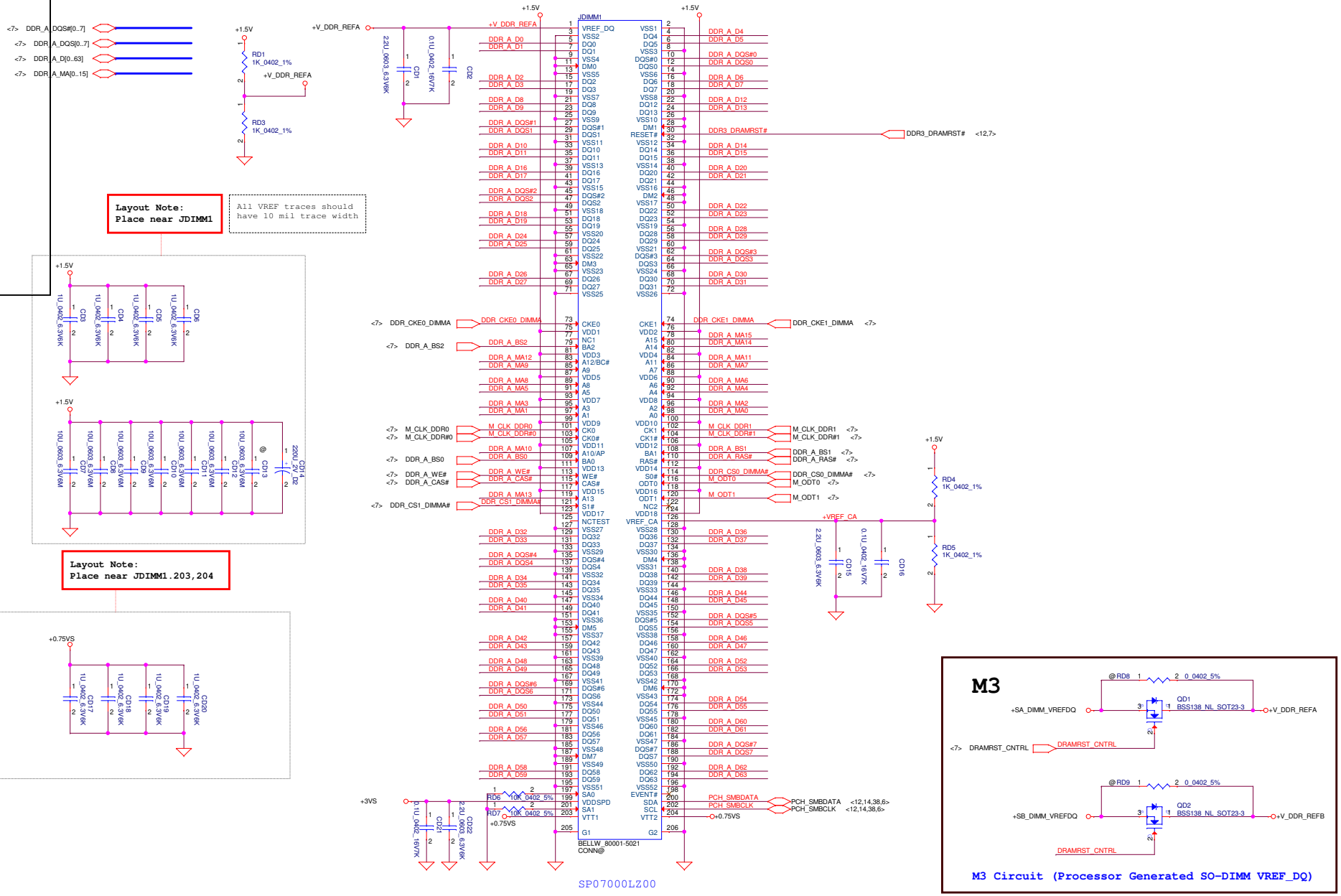
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PROCESSOR(6/6) PWR,VSS

Size | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 10 of 57



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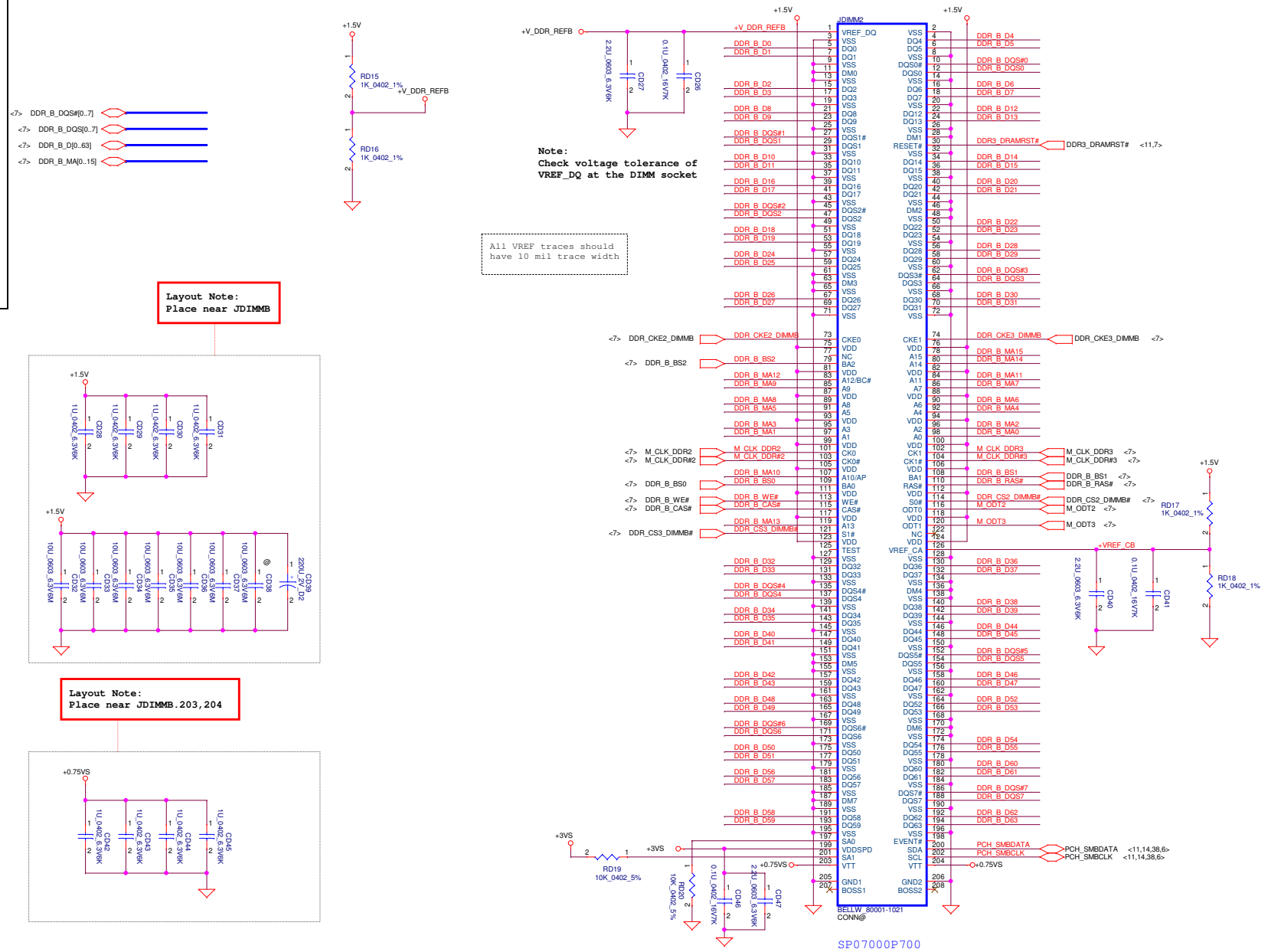
Compal Electronics, Inc.

Title: **DDRIII DIMMA**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 11 of 57



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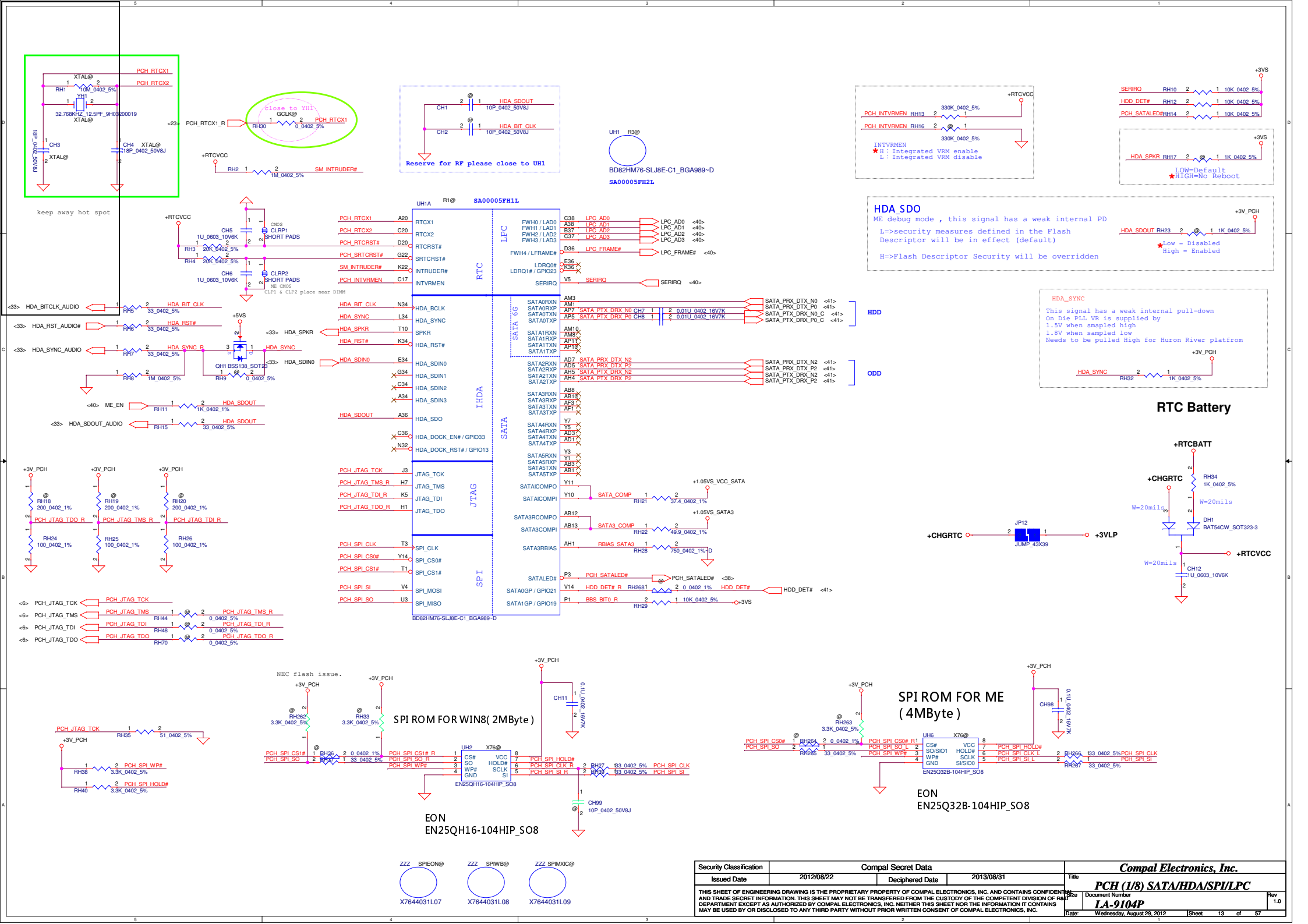
Compal Electronics, Inc.			
Title: DDRIII DIMMB			
Size	Document Number: LA-9104P		Rev: 1.0
Date: Wednesday, August 29, 2012	Sheet 12 of 57		



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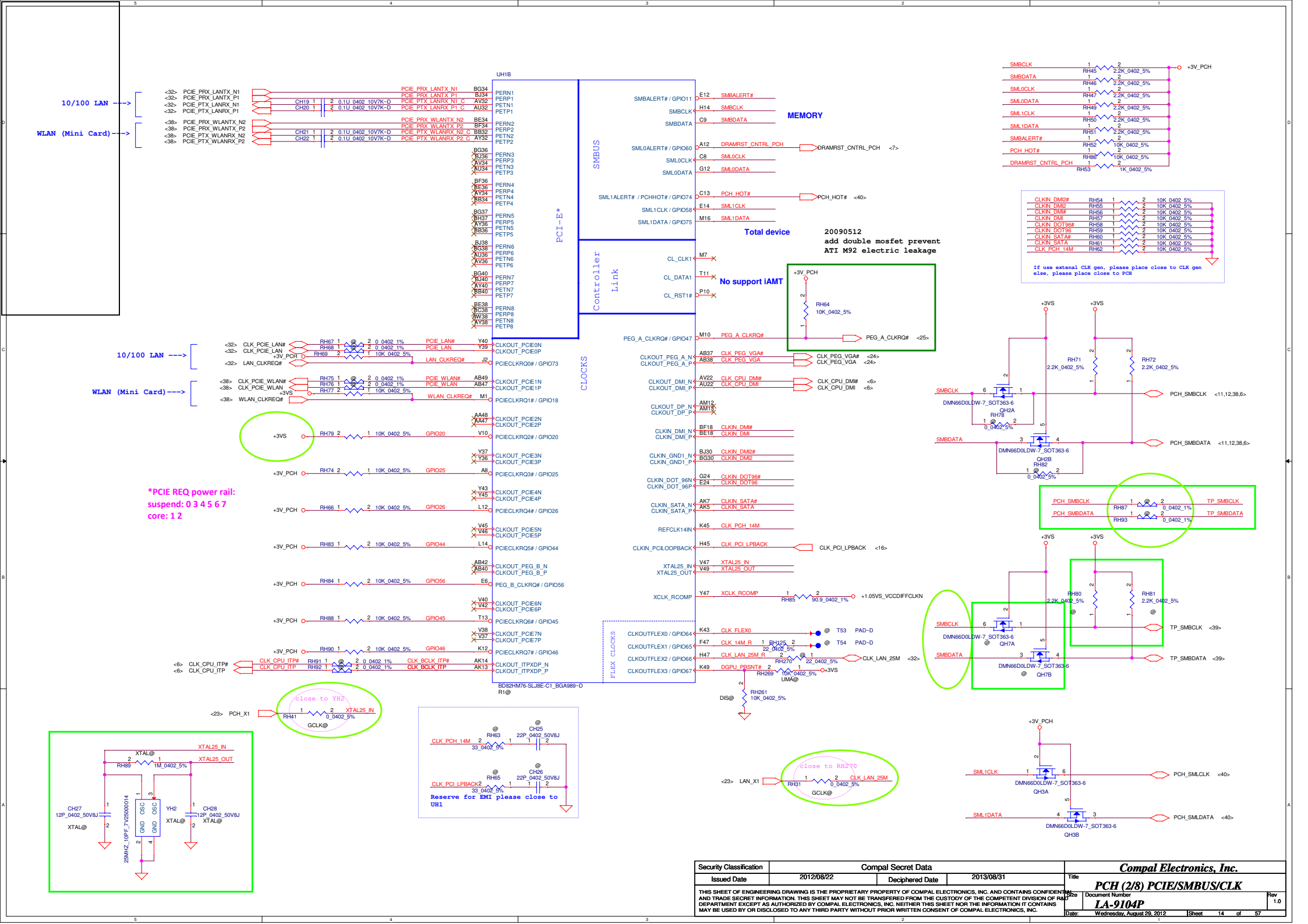
Compal Electronics, Inc.

Title: **PCH (1/8) SATA/HDA/SPI/LPC**

Size: | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 13 of 57



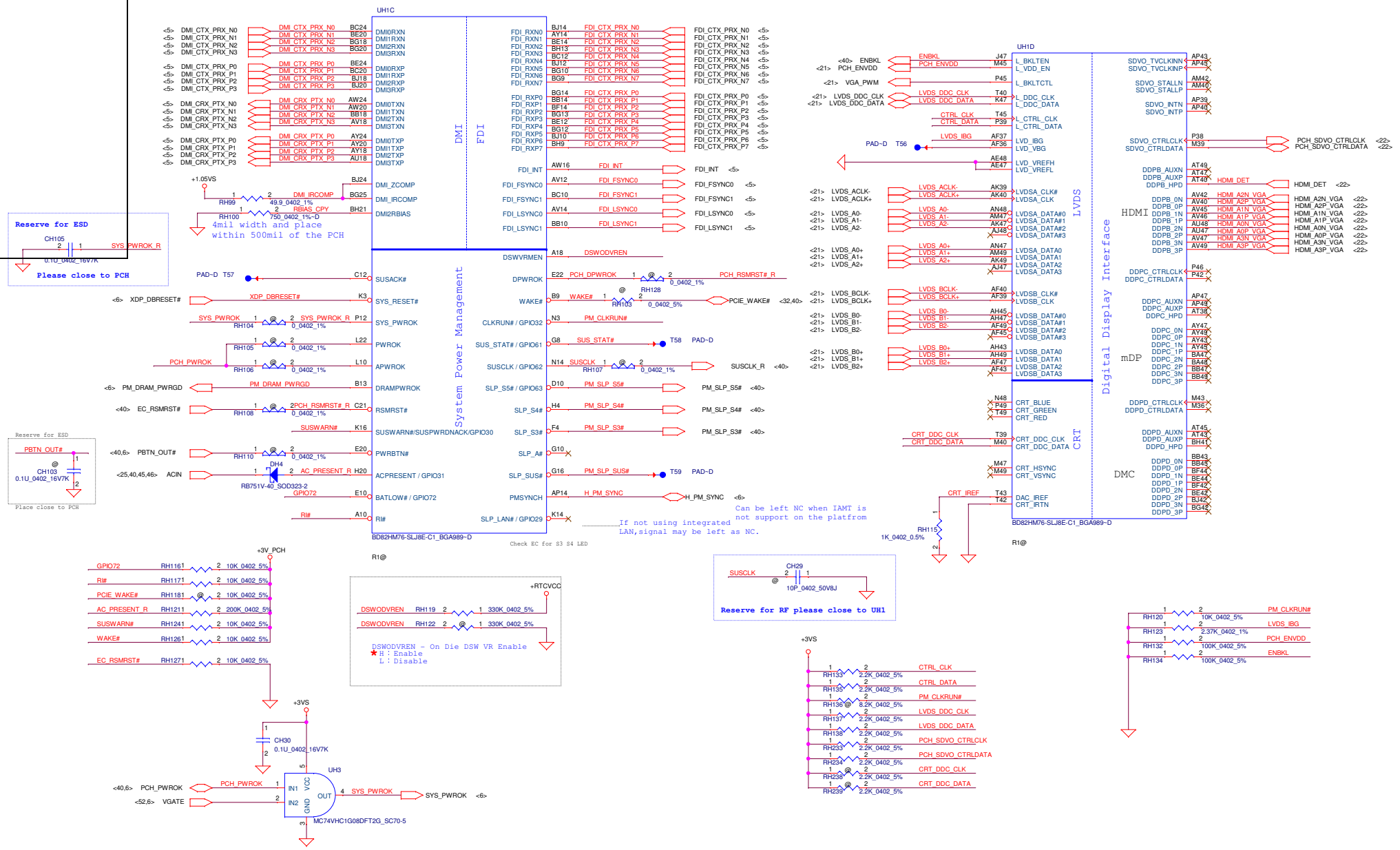
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **PCH (2/8) PCIE/SMBUS/CLK**

Size	Document Number	Rev
	LA-9104P	1.0

Date: Wednesday, August 29, 2012 Sheet 14 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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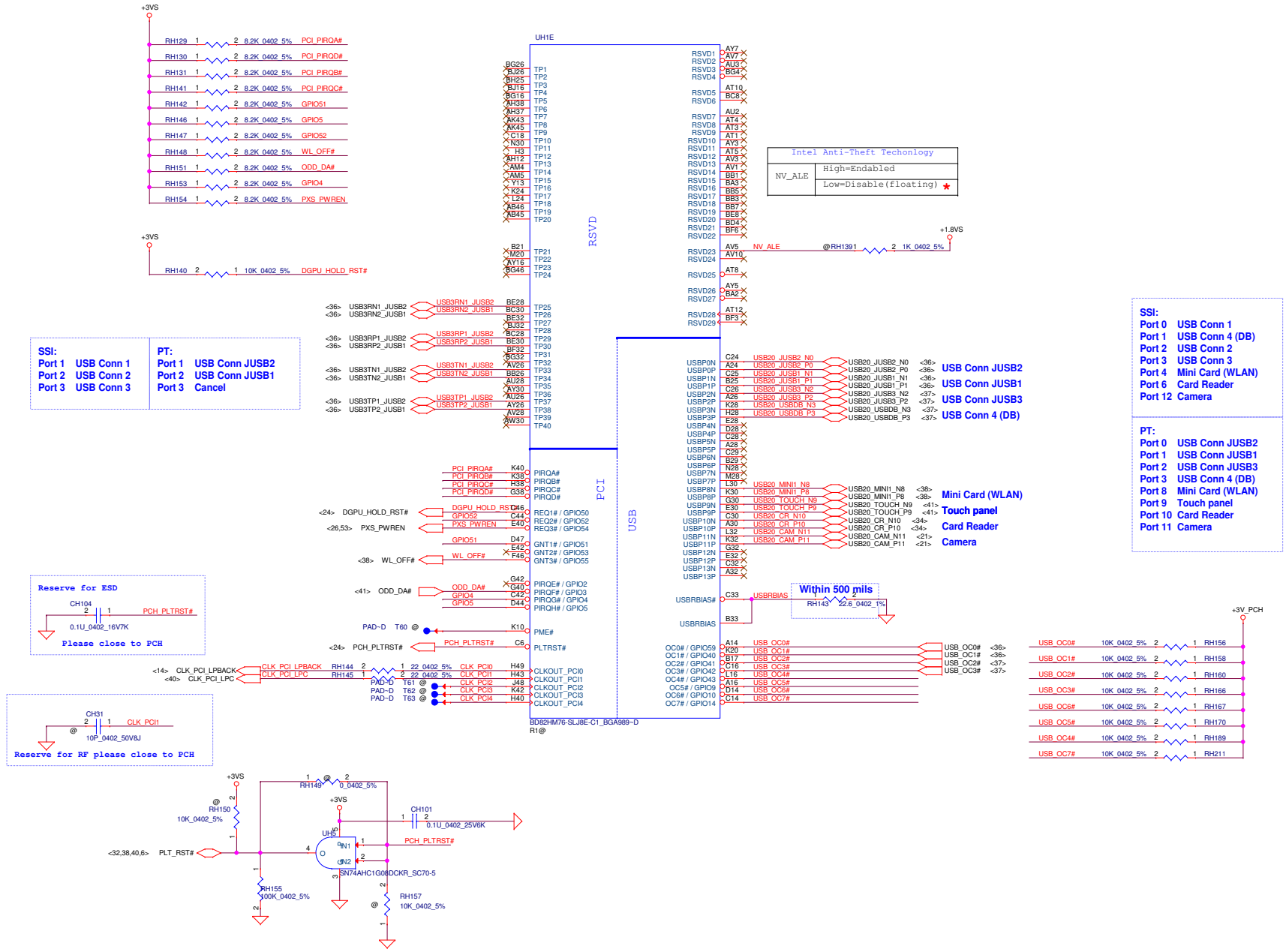
Compal Electronics, Inc.

Title: **PCH (3/8) DMI/FDI/PM/GFX/DP**

Size	Document Number	Rev
	LA-9104P	1.0

Date: Wednesday, August 29, 2012 Sheet 15 of 57



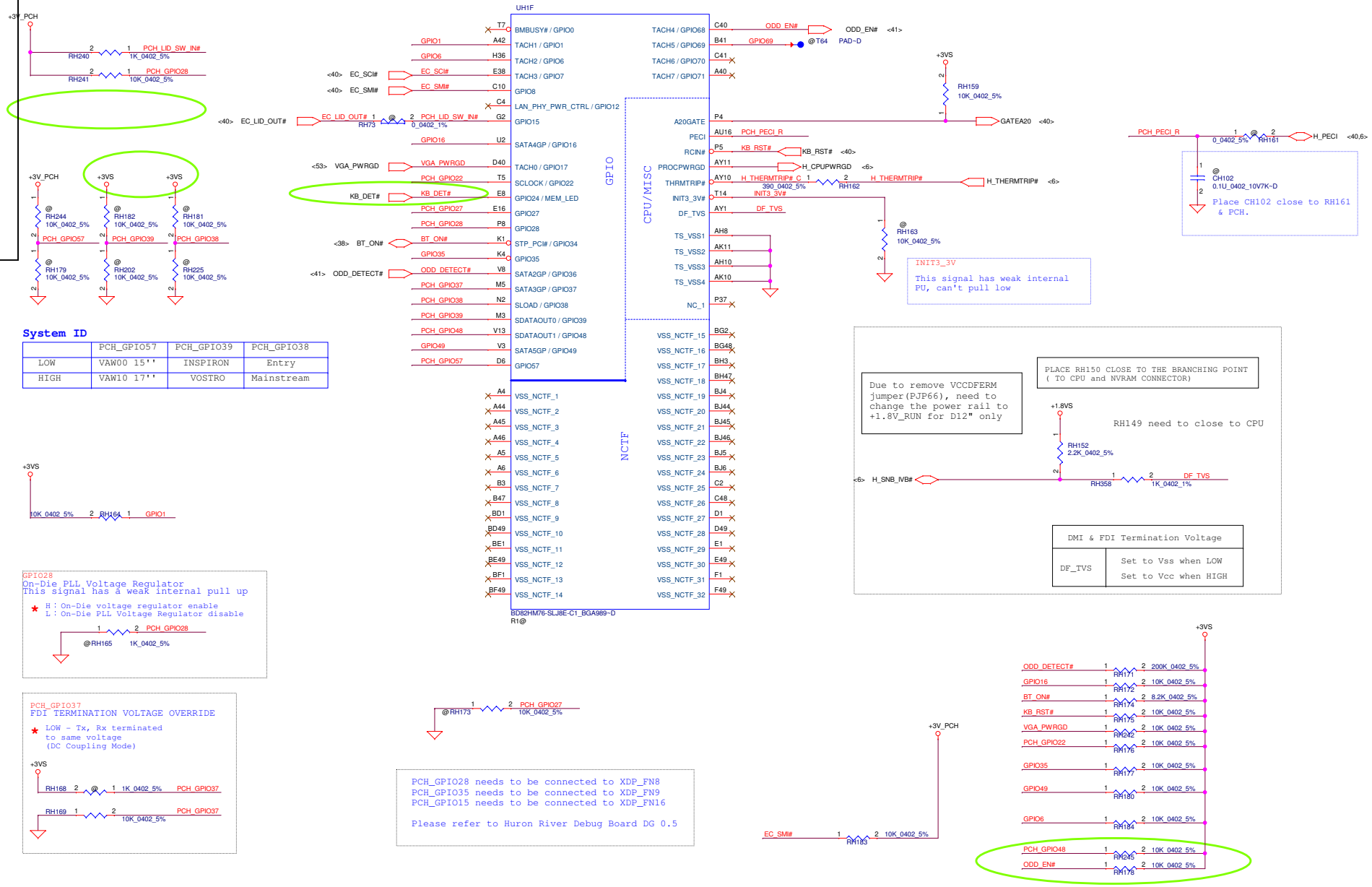
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **PCH (4/8) PCI/USB/NVRAM**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 16 of 57



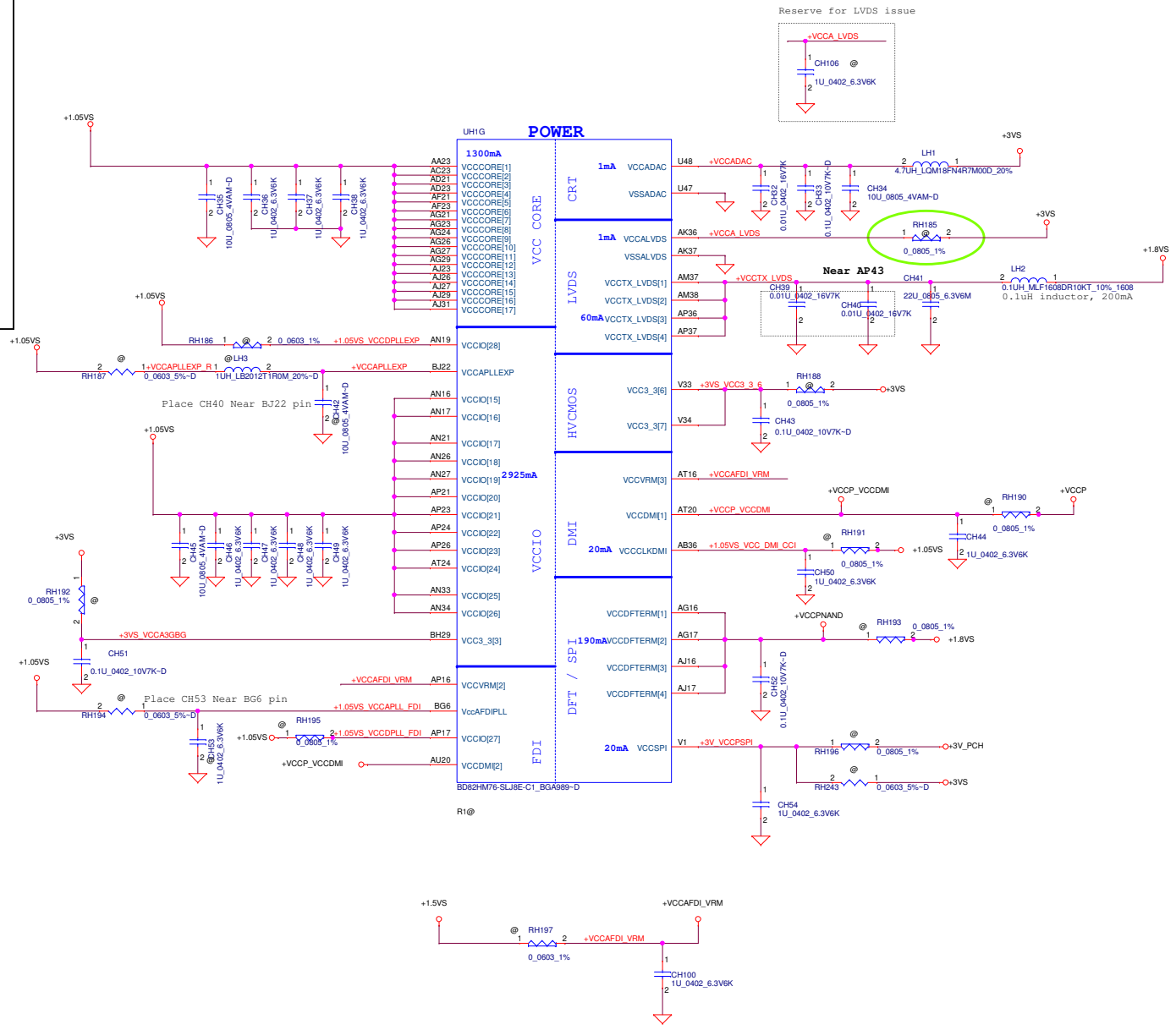
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **PCH (5/8) GPIO/CPU/MISC**

Size	Document Number	Rev
	LA-9104P	1.0

Date: Wednesday, August 29, 2012 Sheet 17 of 57



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size: | Document Number: LA-9104P | Rev: 1.0

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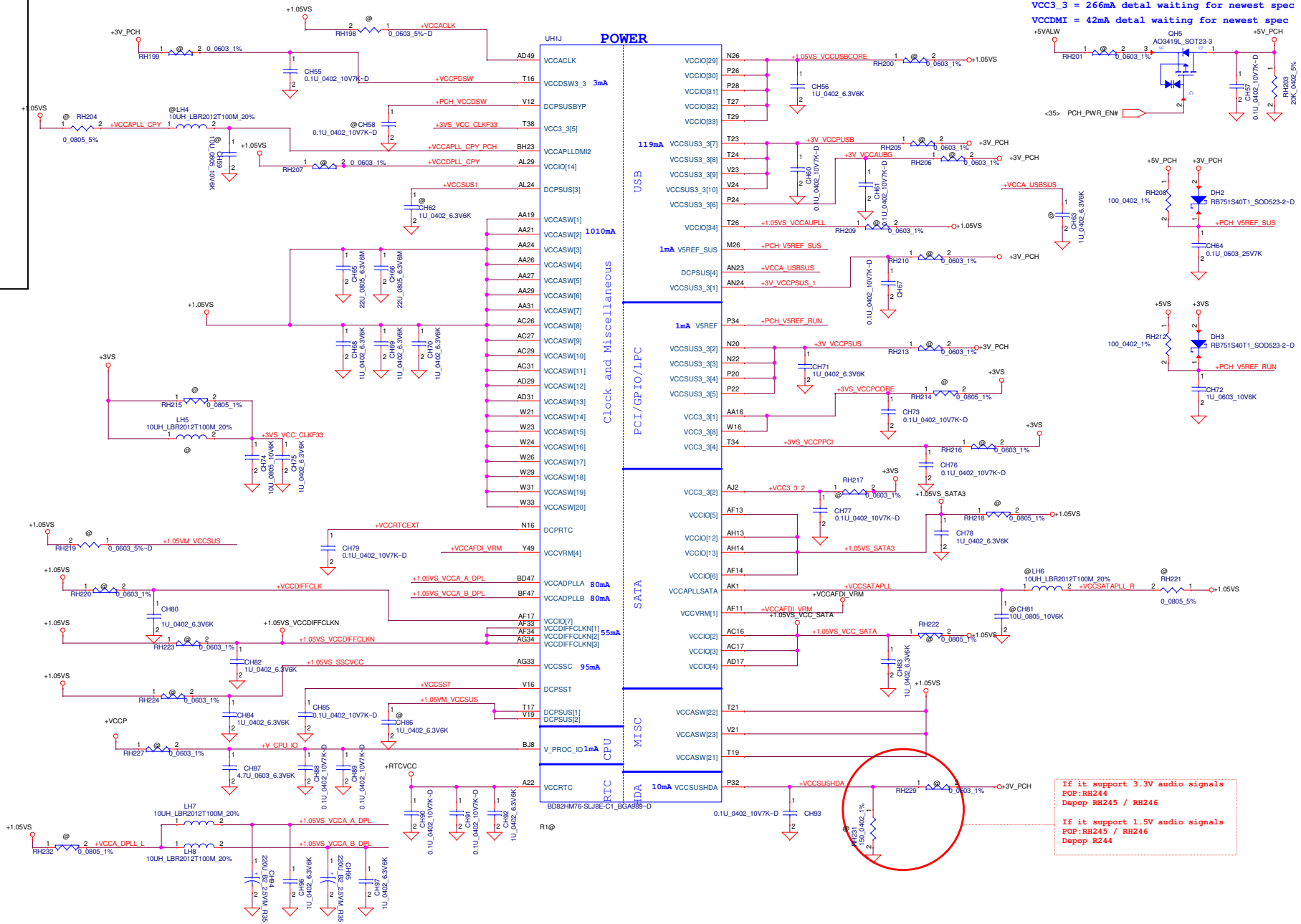

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.	
Title	PCH (7/8) PWR
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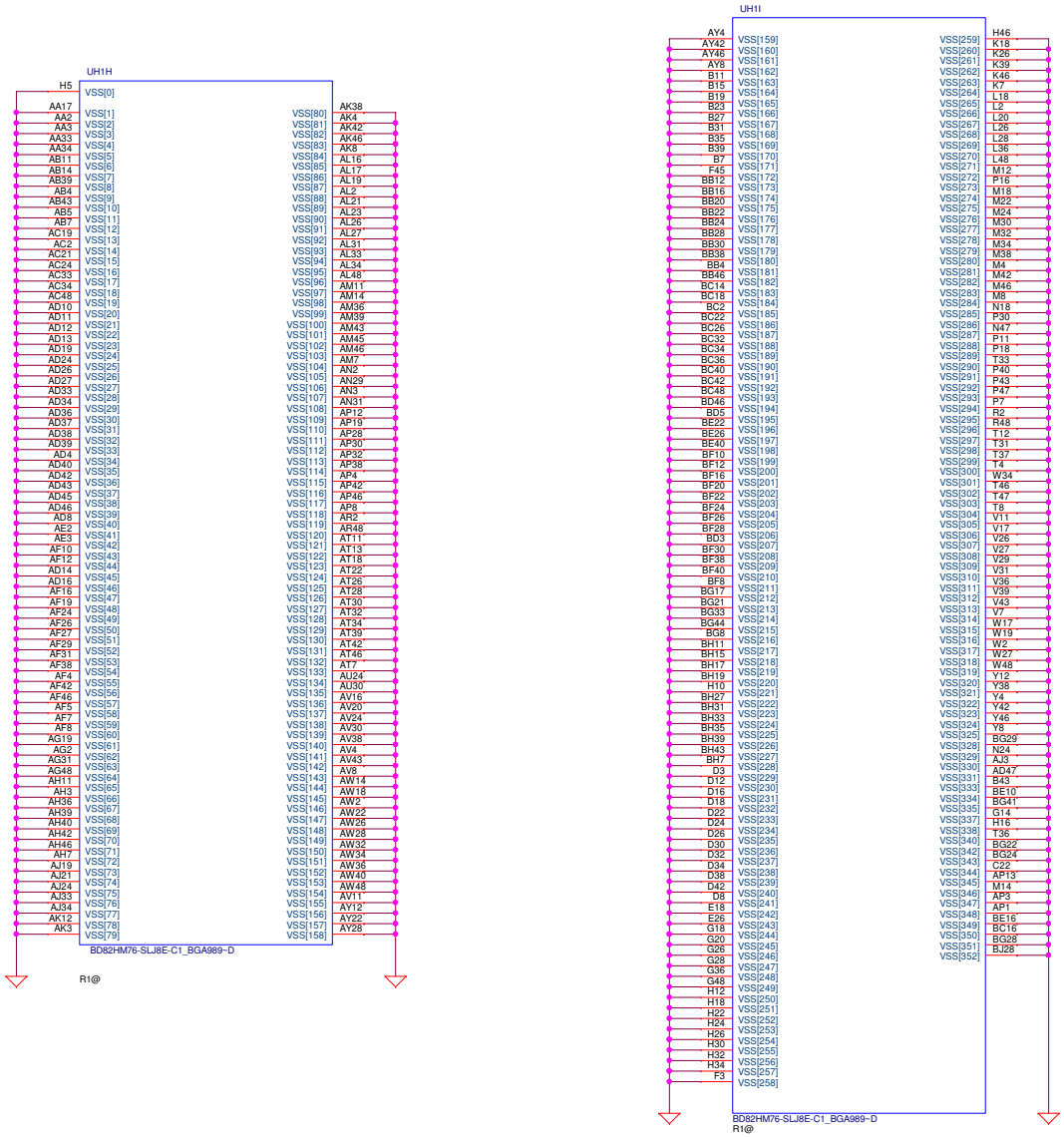

Security Classification	Compal Secret Data			
Issued Date	2012/08/22	Deciphered Date	2013/08/31	

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

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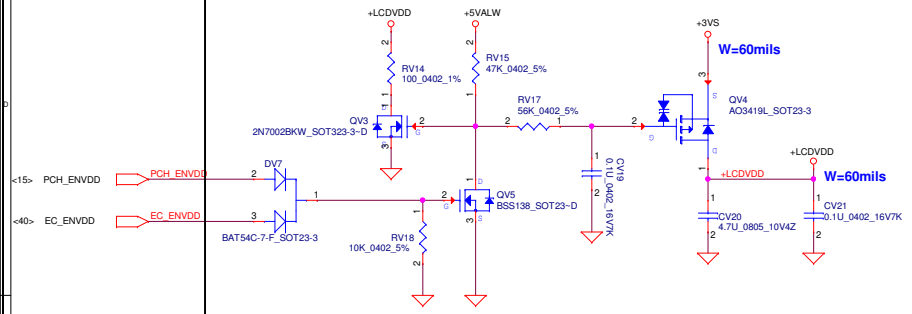
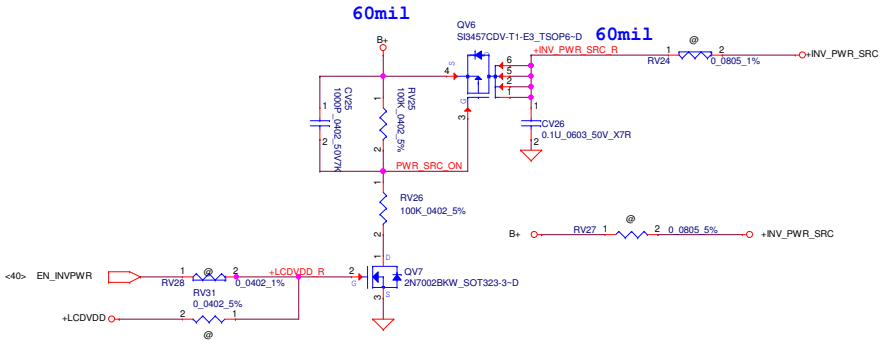
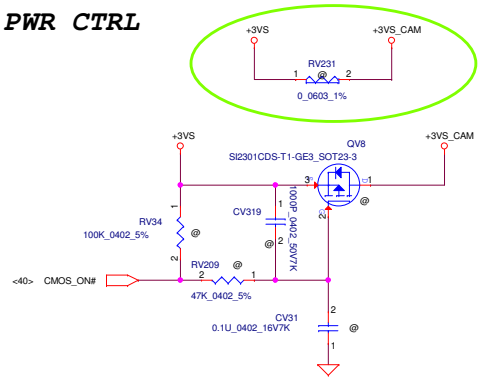
LCD PWR CTRL



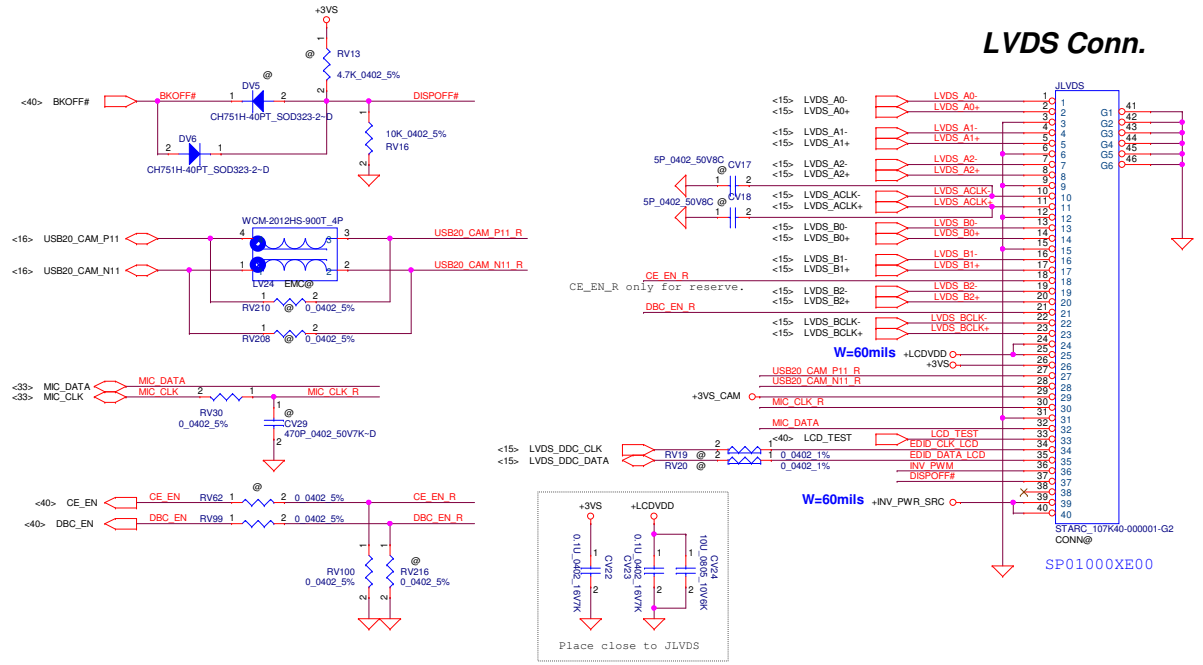
LCD backlight PWR CTRL



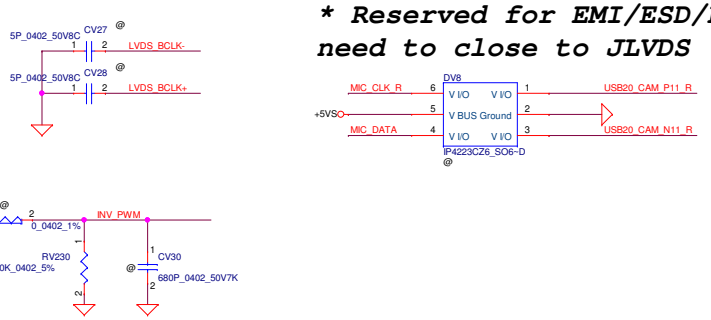
Webcam PWR CTRL



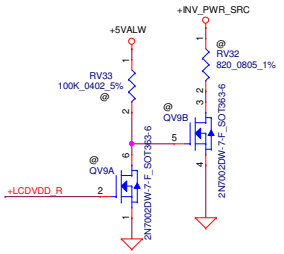
LVDS Conn.



* Reserved for EMI/ESD/RF need to close to JLVDS



* Reserved for LCD sequence tuning



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Compal Electronics, Inc.			
Title: LVDS/webcam			
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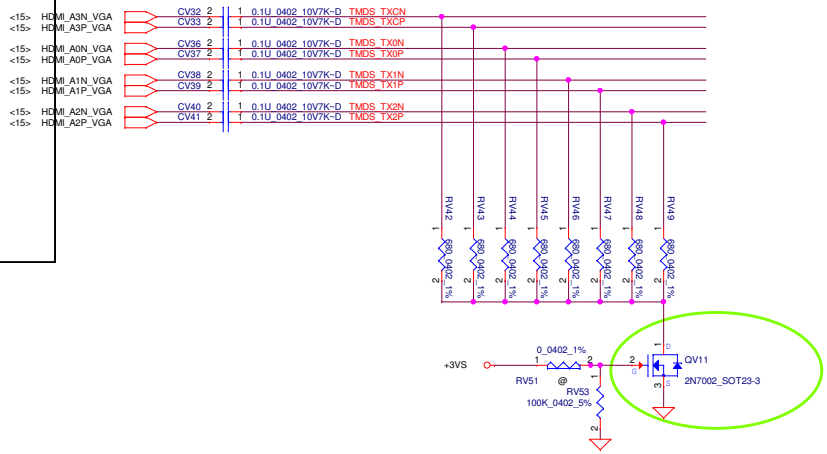
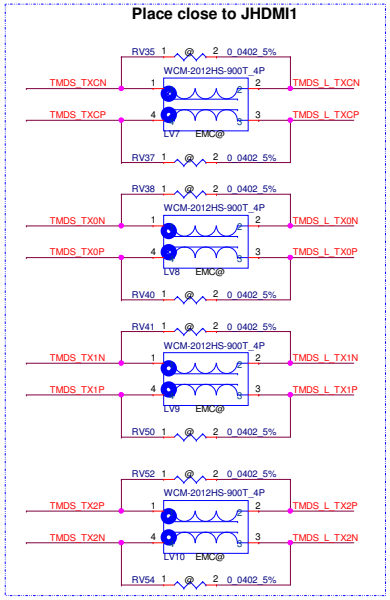
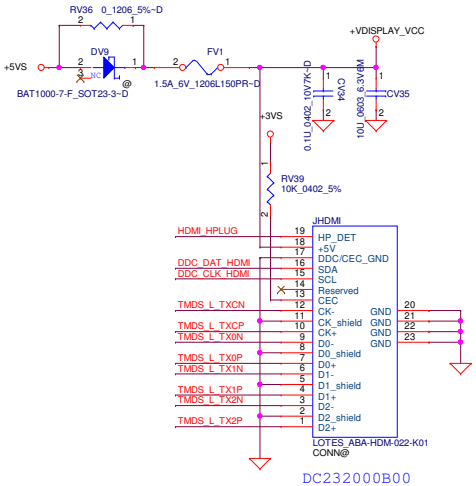
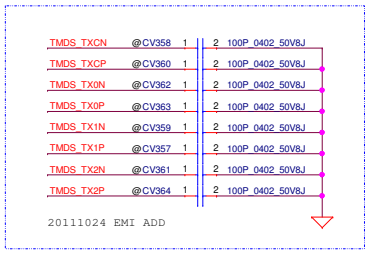
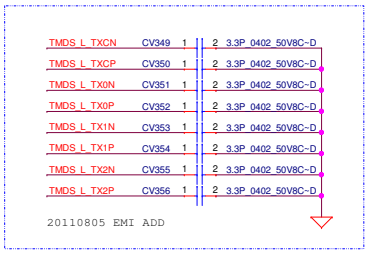
W=40mils

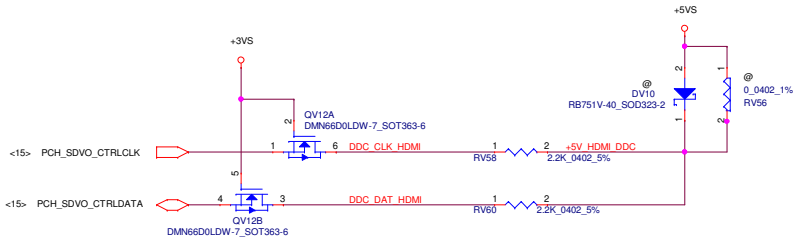


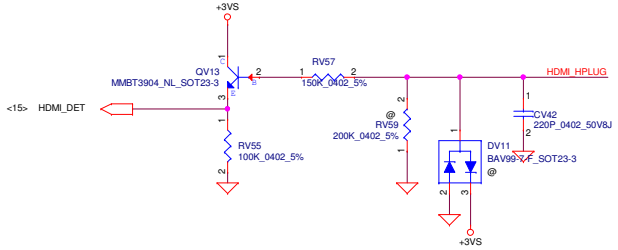












46@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: HDMI

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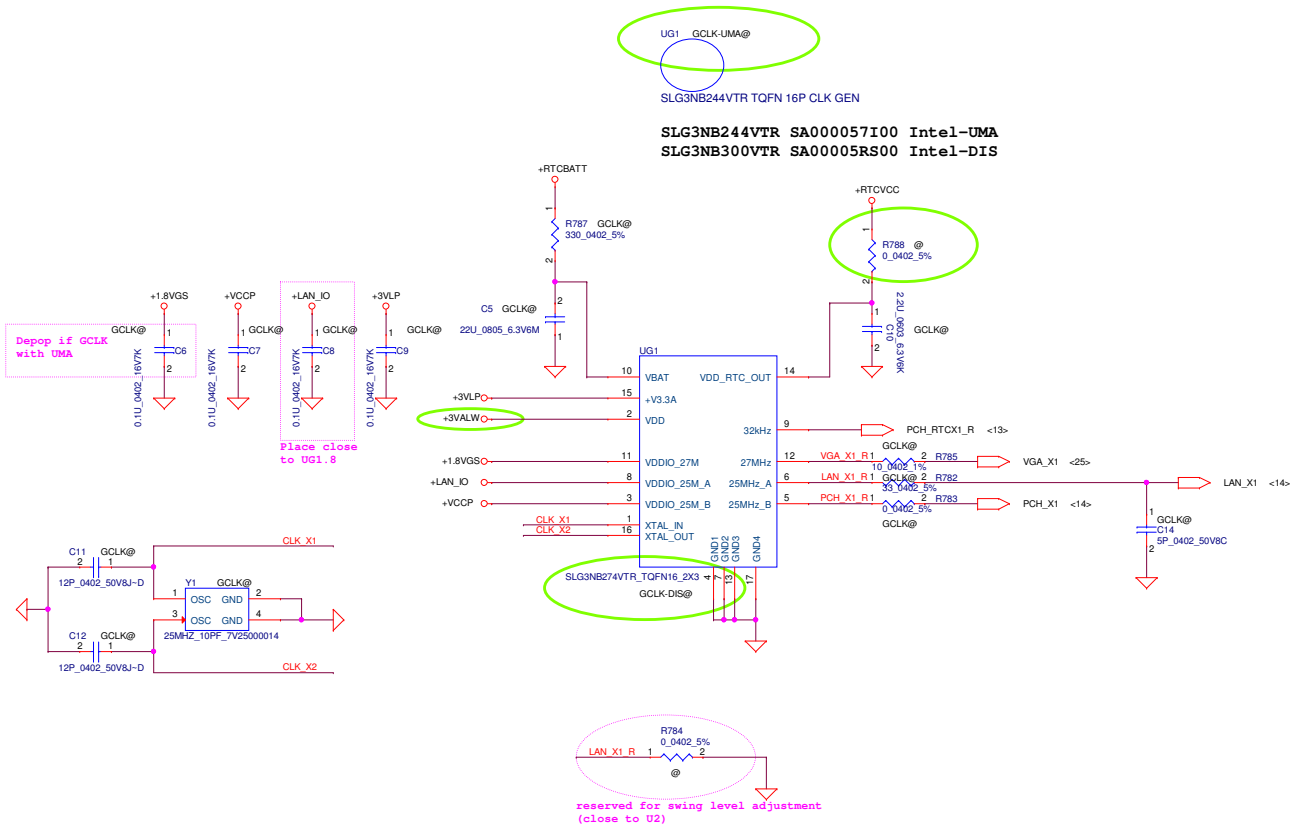

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: GCLK

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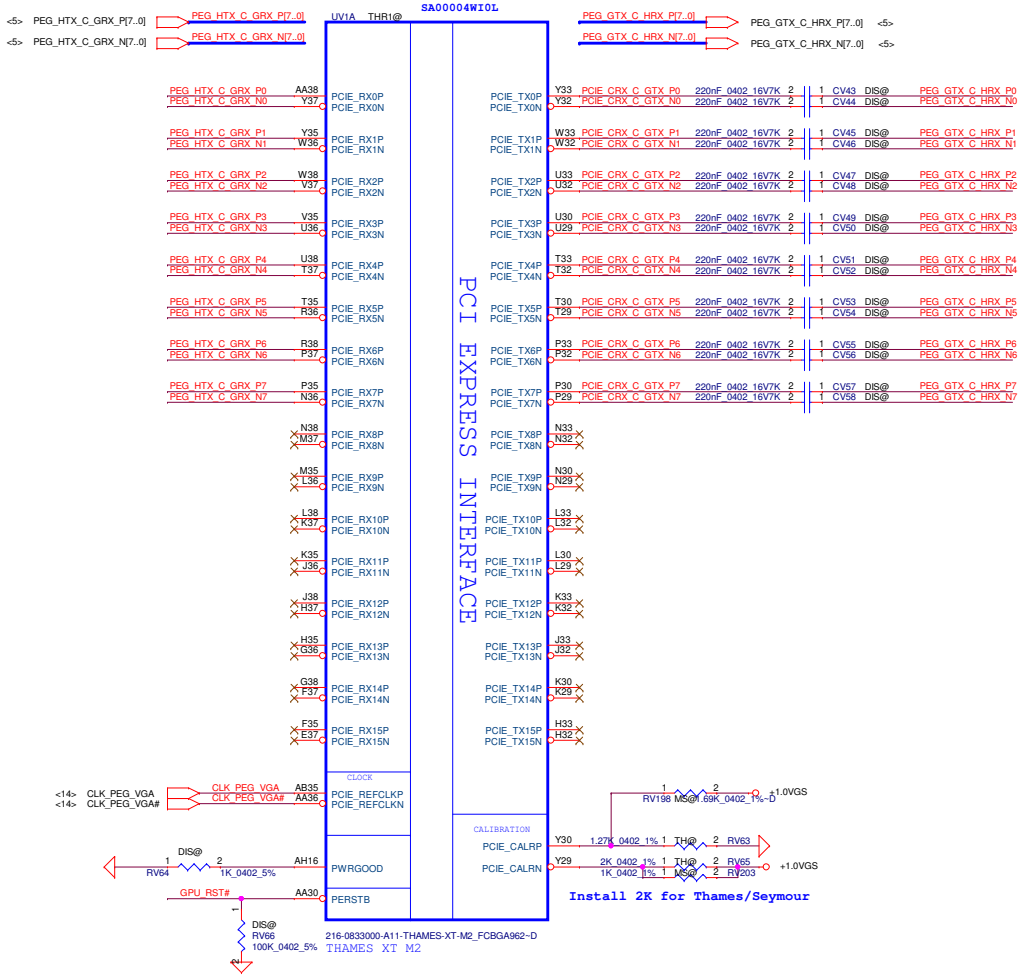
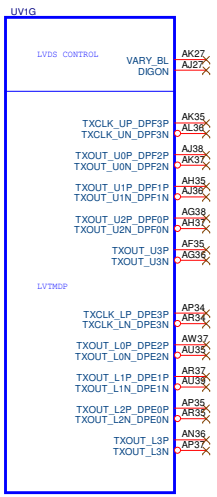
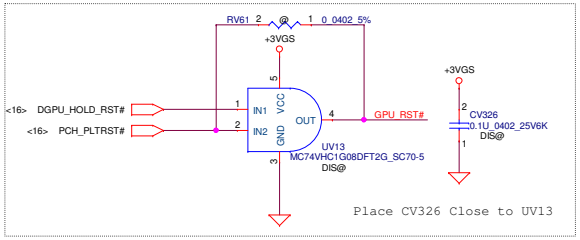
GFX PCIE LANE REVERSAL



LVDS Interface





UV1 THR3@ SA00004WI1L
216-0833000-A11-THAMES-XT-M2_FCBGA962~D

UV1 MSR1@ SA00005X10L
MARS-PRO_FCBGA962~D
MARS Pro

UV1 MSR3@ SA00005X10L
MARS-PRO_FCBGA962~D

UV1 CHR1@
Chelsea Pro

UV1 CHR3@
Chelsea Pro

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_PCIE/LVDS

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ZZZ8 Sam1GR1@ ZZZ4 Sam1GR3@
X7644031L01 X7644031L10
ZZZ5 Micron1GR1@ ZZZ3 Micron1GR3@
X7644031L02 X7644031L11
ZZZ7 Sam2GR1@ ZZZ2 Sam2GR3@
X7644031L05 X7644031L12
ZZZ6 Hyn2GR1@ ZZZ1 Hyn2GR3@
X7644031L06 X7644031L13

+1.8VGS

RV67 1 2 X76@ 10K_0402_5% VRAM_ID0
RV68 1 2 X76@ 10K_0402_5% VRAM_ID1
RV69 1 2 X76@ 10K_0402_5% VRAM_ID2
RV71 1 2 X76@ 10K_0402_5%
RV72 1 2 X76@ 10K_0402_5%

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2	
H5TQ1G63DFR-11C Samsung 1GB SA00004GS0L(R1) SA00004GS1L(R3)	RV68 0	RV69 1	RV72 0	64MX16 (1G)
H5TQ1G63DFR-11C Hynix 1GB SA000041S3L	RV67 1	RV70 0	RV72 0	64MX16 (1G)
MT41J64M16JT-107G:G Micron 1GB SA00004Y20L(R1) SA00004Y21L(R3)	RV67 1	RV69 1	RV71 1	64MX16 (1G)
H5TQ2G63DFR-11C Samsung 2GB SA00005SH0L(R1) SA00005SH1L(R3)	RV68 0	RV69 1	RV71 1	128Mx16 (2G)
H5TQ2G63DFR-11C Hynix 2GB SA00003YO2L(R1) SA00003YO3L(R3)	RV67 1	RV70 0	RV71 1	128Mx16 (2G) ★ PT
H5TQ2G63DFR-11C Micron 2GB SA00005XB0L(R1) SA00005XB1L(R3)				128Mx16 (2G)

VRAM_ID0
VRAM_ID1
VRAM_ID2

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

STRAPS

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

Mars Pro MLPs	RV241	RV242	Bits [3:1]
Hynix	NC	4.75k	000
Samsung	8.45k	2k	001
Micron	4.75k	NC	111

Add 12/6 for MLPS 0402 1% resistors are required.

Internal VGA Thermal Sensor

VGA Thermal Sensor ADM1032ARMZ

Closed to GPU

Address:100_1101

(Thames 75mA)
(Thames 125mA)
0.935V@ Mars Pro
(Thames 5mA)
(1.8V@20mA TSVDD)
0.60 V level, Please VREFG Divider ans cap close to ASIC
XTALIN Voltage Swing: 1.8 V
Add 12/6 for MLPS
Need to CHECK CIS symbol
Close to YV1
NC_TSVSSQ should be tied to GND on Thames/Seymour
65mA
100mA
10mil
20mil

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Title: ATI_ThamesXT_M2_Main_MSIC

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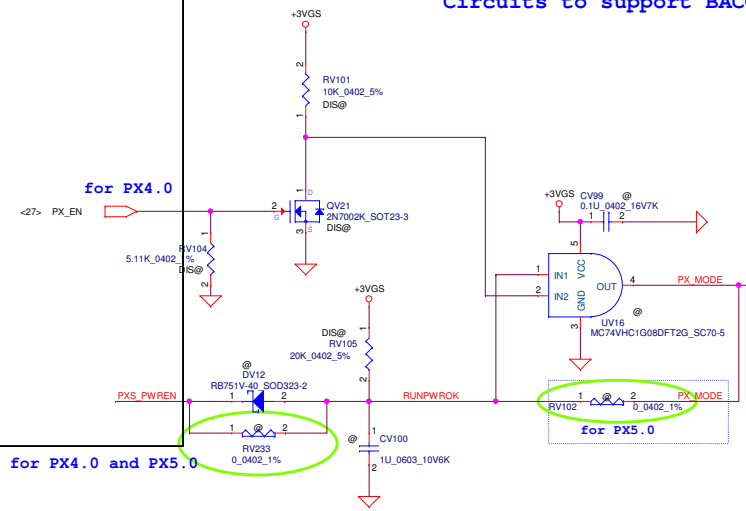
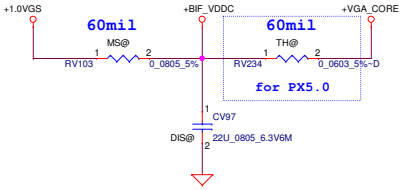
Circuits to support BACO

Switch circuits in BACO desingns for Thanes/Seymour only

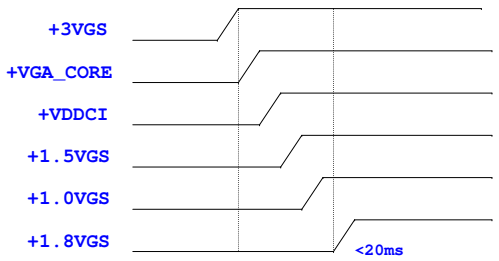
55mA@1.0V, in BACO mode

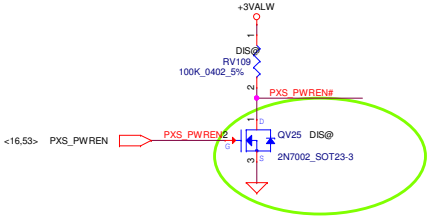




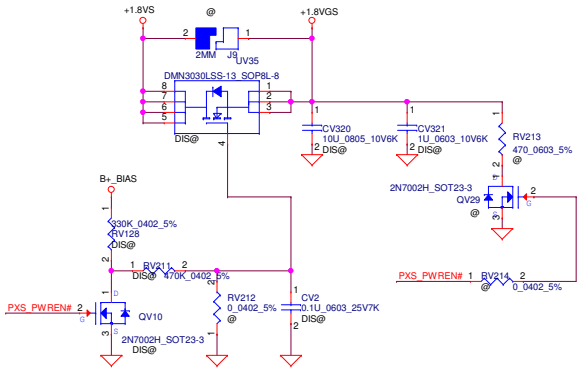
Note:
PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

Power Seguence of Thames and Mars Pro

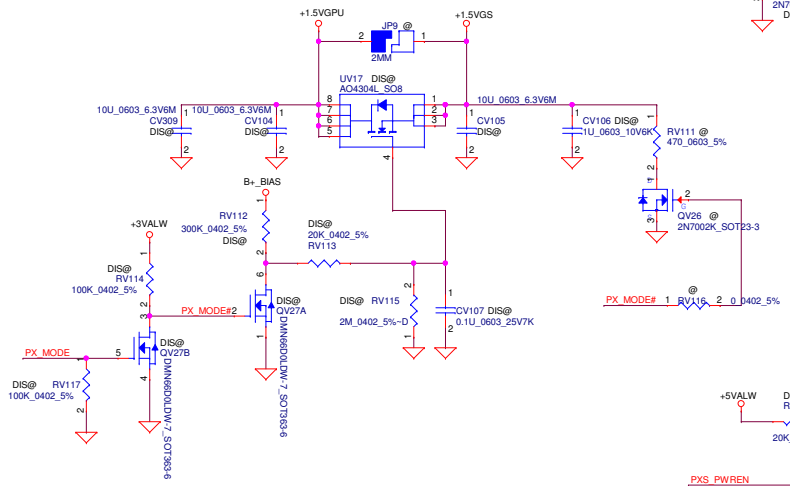




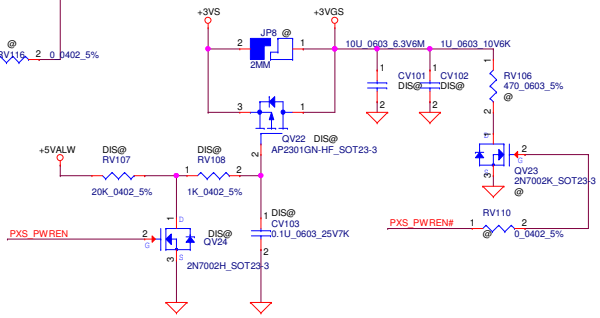
+1.8VS TO +1.8VGS



+1.5VGPU TO +1.5VGS



+3.3VS TO +3.3VGS



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_BACO POWER

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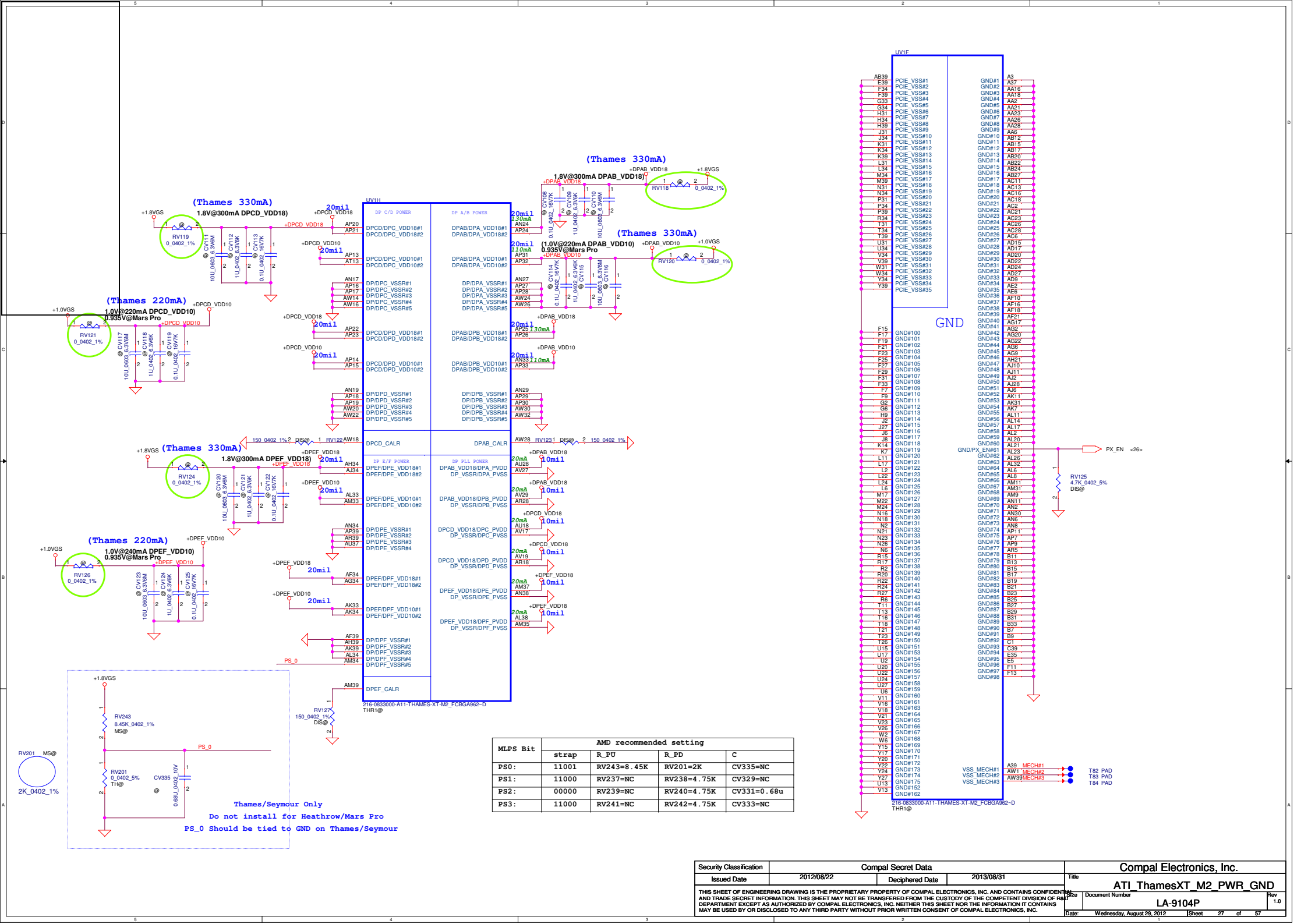

MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_PWR_GND

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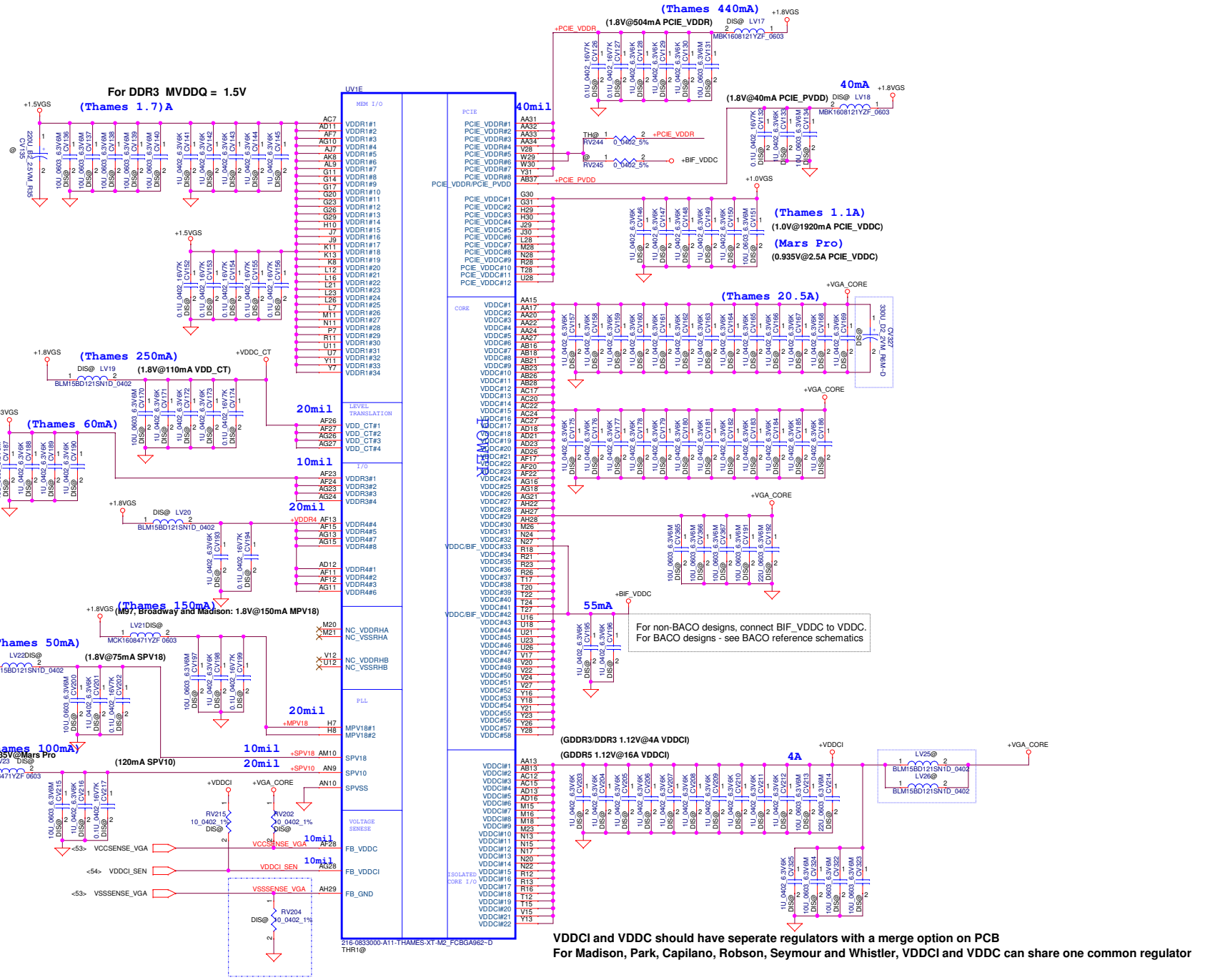

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title	ATI_ThamesXT_M2_Power		
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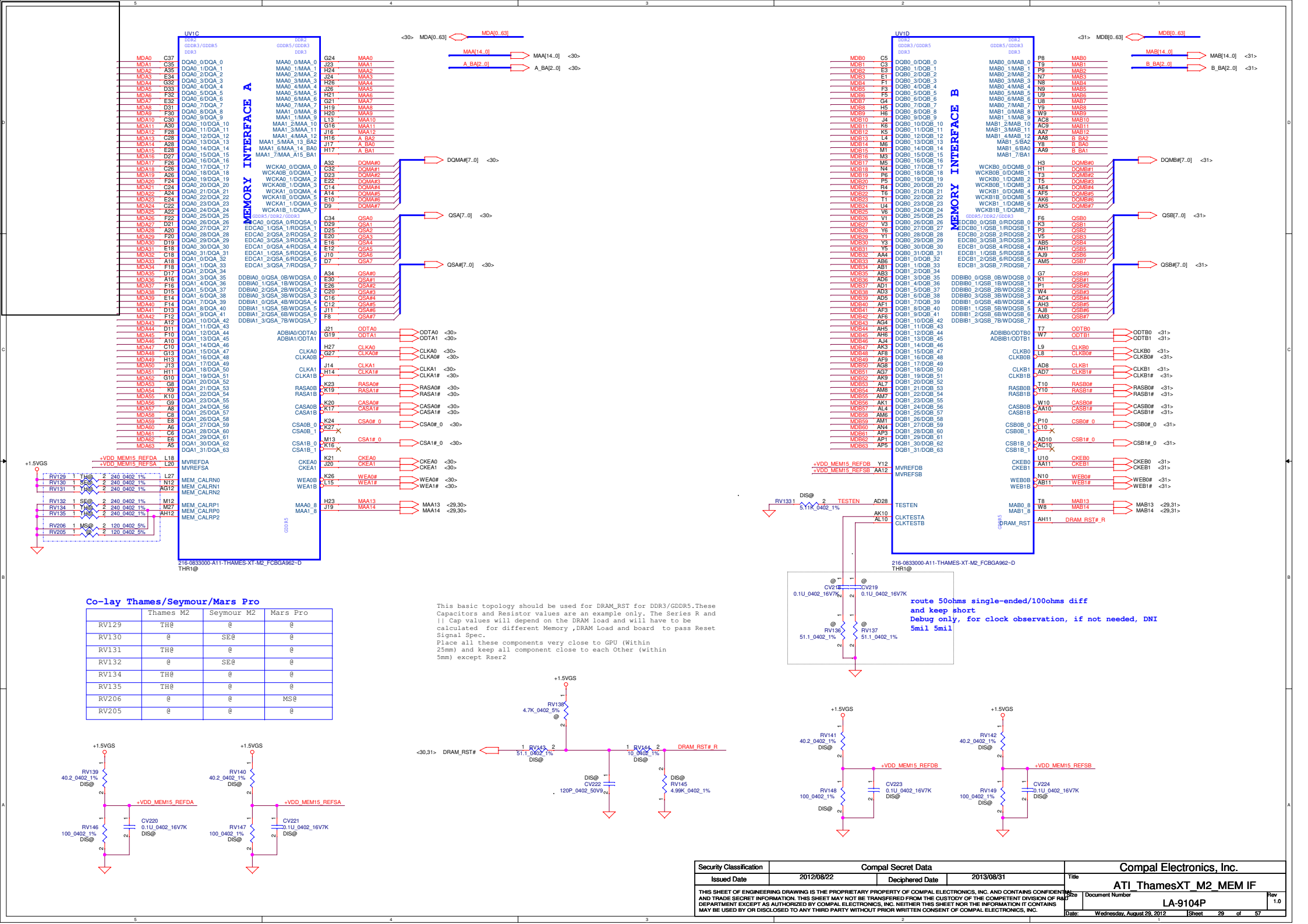
UV1C
MEMORY INTERFACE A
DDR2
GDDR3/GDDR5
DDR3
MDA0 C37
MDA1 C35
MDA2 A35
MDA3 E34
MDA4 G32
MDA5 D33
MDA6 F32
MDA7 E32
MDA8 D31
MDA9 F30
MDA10 C30
MDA11 A30
MDA12 F28
MDA13 C28
MDA14 A28
MDA15 E28
MDA16 D27
MDA17 F26
MDA18 C26
MDA19 A26
MDA20 F24
MDA21 C24
MDA22 A24
MDA23 E24
MDA24 C22
MDA25 A22
MDA26 F22
MDA27 D21
MDA28 A20
MDA29 F20
MDA30 D19
MDA31 E18
MDA32 C18
MDA33 A18
MDA34 F18
MDA35 D17
MDA36 A16
MDA37 F16
MDA38 D15
MDA39 E14
MDA40 F14
MDA41 D13
MDA42 F12
MDA43 A12
MDA44 D11
MDA45 F10
MDA46 A10
MDA47 C10
MDA48 G13
MDA49 H13
MDA50 J13
MDA51 H11
MDA52 G10
MDA53 G8
MDA54 K9
MDA55 K10
MDA56 G9
MDA57 A8
MDA58 C8
MDA59 E8
MDA60 A6
MDA61 C6
MDA62 E6
MDA63 A5
DQA0_0/DQA_0
DQA0_1/DQA_1
DQA0_2/DQA_2
DQA0_3/DQA_3
DQA0_4/DQA_4
DQA0_5/DQA_5
DQA0_6/DQA_6
DQA0_7/DQA_7
DQA0_8/DQA_8
DQA0_9/DQA_9
DQA0_10/DQA_10
DQA0_11/DQA_11
DQA0_12/DQA_12
DQA0_13/DQA_13
DQA0_14/DQA_14
DQA0_15/DQA_15
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DQA1_28/DQA_60
DQA1_29/DQA_61
DQA1_30/DQA_62
DQA1_31/DQA_63
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MVREFSA
MEM_CALRN0
MEM_CALRN1
MEM_CALRN2
MEM_CALRP1
MEM_CALRP0
MEM_CALRP2
GDDR5
MAA0_0/MAA_0
MAA0_1/MAA_1
MAA0_2/MAA_2
MAA0_3/MAA_3
MAA0_4/MAA_4
MAA0_5/MAA_5
MAA0_6/MAA_6
MAA0_7/MAA_7
MAA1_0/MAA_8
MAA1_1/MAA_9
MAA1_2/MAA_10
MAA1_3/MAA_11
MAA1_4/MAA_12
MAA1_5/MAA_13_BA2
MAA1_6/MAA_14_BA0
MAA1_7/MAA_A15_BA1
WCKA0_0/DQMA_0
WCKA0B_0/DQMA_1
WCKA0_1/DQMA_2
WCKA0B_1/DQMA_3
WCKA1_0/DQMA_4
WCKA1B_0/DQMA_5
WCKA1_1/DQMA_6
WCKA1B_1/DQMA_7
GDDR5/DDR2/GDDR3
EDCA0_0/QSA_0/RDQSA_0
EDCA0_1/QSA_1/RDQSA_1
EDCA0_2/QSA_2/RDQSA_2
EDCA0_3/QSA_3/RDQSA_3
EDCA1_0/QSA_4/RDQSA_4
EDCA1_1/QSA_5/RDQSA_5
EDCA1_2/QSA_6/RDQSA_6
EDCA1_3/QSA_7/RDQSA_7
DDBIA0_0/QSA_0B/WDQSA_0
DDBIA0_1/QSA_1B/WDQSA_1
DDBIA0_2/QSA_2B/WDQSA_2
DDBIA0_3/QSA_3B/WDQSA_3
DDBIA1_0/QSA_4B/WDQSA_4
DDBIA1_1/QSA_5B/WDQSA_5
DDBIA1_2/QSA_6B/WDQSA_6
DDBIA1_3/QSA_7B/WDQSA_7
ADBIA0/ODTA0
ADBIA1/ODTA1
CLKA0
CLKA0B
CLKA1
CLKA1B
RASA0B
RASA1B
CASA0B
CASA1B
CSA0B_0
CSA0B_1
CSA1B_0
CSA1B_1
CKEA0
CKEA1
WEA0B
WEA1B
MAA0_8
MAA1_8
DMA#
QSA#
ODTA0
ODTA1
CLKA0
CLKA0#
CLKA1
CLKA1#
RASA0#
RASA1#
CASA0#
CASA1#
CSA0#_0
CSA1#_0
CKEA0
CKEA1
WEA0#
WEA1#
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MAA14
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THR1@
+1.5VGS
+VDD_MEM15_REFDA
+VDD_MEM15_REFSA
RV129 TH@ 240_0402_1%
RV130 SE@ 240_0402_1%
RV131 TH@ 240_0402_1%
RV132 SE@ 240_0402_1%
RV134 TH@ 240_0402_1%
RV135 TH@ 240_0402_1%
RV206 MS@ 120_0402_5%
RV205 @ 120_0402_5%
UV1D
MEMORY INTERFACE B
MDB0 C5
MDB1 C3
MDB2 E3
MDB3 E1
MDB4 F1
MDB5 F3
MDB6 F5
MDB7 G4
MDB8 H5
MDB9 H6
MDB10 J4
MDB11 K6
MDB12 K5
MDB13 L4
MDB14 M6
MDB15 M1
MDB16 M3
MDB17 M5
MDB18 N4
MDB19 P6
MDB20 P5
MDB21 R4
MDB22 T6
MDB23 T1
MDB24 U4
MDB25 V6
MDB26 V1
MDB27 V3
MDB28 Y6
MDB29 Y1
MDB30 Y3
MDB31 Y5
MDB32 AA4
MDB33 AB6
MDB34 AB1
MDB35 AB3
MDB36 AD6
MDB37 AD1
MDB38 AD3
MDB39 AD5
MDB40 AF1
MDB41 AF3
MDB42 AF6
MDB43 AG4
MDB44 AH5
MDB45 AH6
MDB46 AJ4
MDB47 AK3
MDB48 AF8
MDB49 AF9
MDB50 AG8
MDB51 AG7
MDB52 AK9
MDB53 AL7
MDB54 AM8
MDB55 AM7
MDB56 AK1
MDB57 AL4
MDB58 AM6
MDB59 AM1
MDB60 AN4
MDB61 AP3
MDB62 AP1
MDB63 AP5
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DQB0_1/DQB_1
DQB0_2/DQB_2
DQB0_3/DQB_3
DQB0_4/DQB_4
DQB0_5/DQB_5
DQB0_6/DQB_6
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DQB0_8/DQB_8
DQB0_9/DQB_9
DQB0_10/DQB_10
DQB0_11/DQB_11
DQB0_12/DQB_12
DQB0_13/DQB_13
DQB0_14/DQB_14
DQB0_15/DQB_15
DQB0_16/DQB_16
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DQB1_30/DQB_62
DQB1_31/DQB_63
MVREFDB
MVREFSB
CLKTESTA
CLKTESTB
TESTEN
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MAB0_2/MAB_2
MAB0_3/MAB_3
MAB0_4/MAB_4
MAB0_5/MAB_5
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MAB0_7/MAB_7
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MAB1_6/BA0
MAB1_7/BA1
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WCKB0B_0/DQMB_1
WCKB0_1/DQMB_2
WCKB0B_1/DQMB_3
WCKB1_0/DQMB_4
WCKB1B_0/DQMB_5
WCKB1_1/DQMB_6
WCKB1B_1/DQMB_7
EDCB0_0/QSB_0/RDQSB_0
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EDCB0_2/QSB_2/RDQSB_2
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EDCB1_3/QSB_7/RDQSB_7
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DDBIB0_1/QSB_1B/WDQSB_1
DDBIB0_2/QSB_2B/WDQSB_2
DDBIB0_3/QSB_3B/WDQSB_3
DDBIB1_0/QSB_4B/WDQSB_4
DDBIB1_1/QSB_5B/WDQSB_5
DDBIB1_2/QSB_6B/WDQSB_6
DDBIB1_3/QSB_7B/WDQSB_7
ADBIB0/ODTB0
ADBIB1/ODTB1
CLKB0
CLKB0B
CLKB1
CLKB1B
RASB0B
RASB1B
CASB0B
CASB1B
CSB0B_0
CSB0B_1
CSB1B_0
CSB1B_1
CKEB0
CKEB1
WEB0B
WEB1B
MAB0_8
MAB1_8
DRAM_RST_R
MAB#
QSB#
ODTB0
ODTB1
CLKB0
CLKB0#
CLKB1
CLKB1#
RASB0#
RASB1#
CASB0#
CASB1#
CSB0#_0
CSB1#_0
CKEB0
CKEB1
WEB0#
WEB1#
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MAB14
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216-0833000-A11-THAMES-XT-M2_FCBGA962~D
THR1@
+VDD_MEM15_REFDB
+VDD_MEM15_REFSB
RV1331 DIS@ 5.11K_0402_1%
CV218 0.1U_0402_16V7K
CV219 0.1U_0402_16V7K
RV136 51.1_0402_1%
RV137 51.1_0402_1%
route 50ohms single-ended/100ohms diff
and keep short
Debug only, for clock observation, if not needed, DNI
5mil 5mil
Co-lay Thames/Seymour/Mars Pro
Thames M2
Seymour M2
Mars Pro
RV129 TH@ @ @
RV130 @ SE@ @
RV131 TH@ @ @
RV132 @ SE@ @
RV134 TH@ @ @
RV135 TH@ @ @
RV206 @ @ MS@
RV205 @ @ @
This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2
+1.5VGS
RV138 4.7K_0402_5%
<30,31> DRAM_RST#
RV143 51.1_0402_1%
RV144 10_0402_1%
DRAM_RST#_R
CV222 120P_0402_50V9
RV145 4.99K_0402_1%
RV139 40.2_0402_1%
RV140 40.2_0402_1%
RV146 100_0402_1%
RV147 100_0402_1%
CV220 0.1U_0402_16V7K
CV221 0.1U_0402_16V7K
RV141 40.2_0402_1%
RV142 40.2_0402_1%
RV148 100_0402_1%
RV149 100_0402_1%
CV223 0.1U_0402_16V7K
CV224 0.1U_0402_16V7K
Security Classification
Compal Secret Data
Issued Date
2012/08/22
Deciphered Date
2013/08/31
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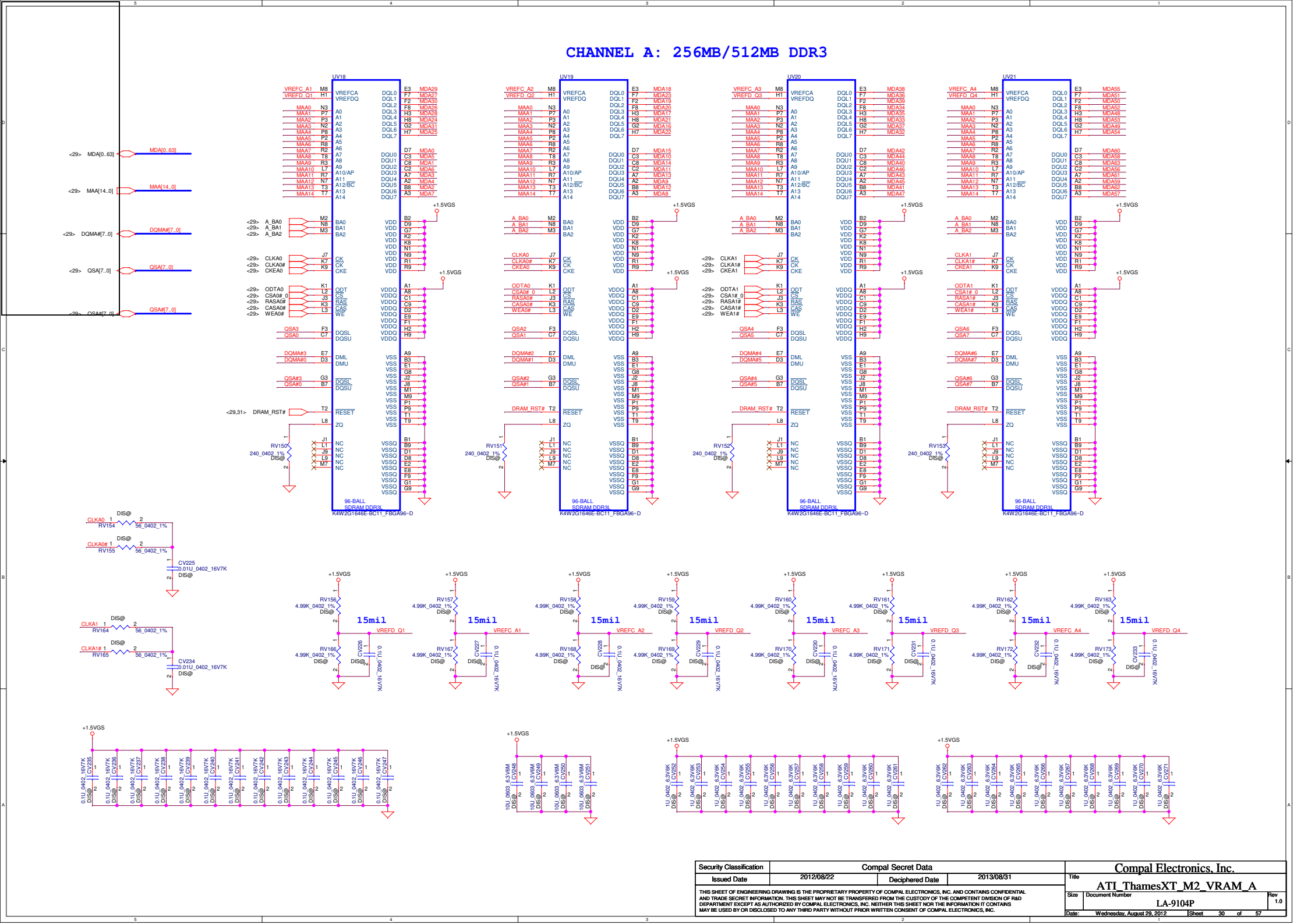
Compal Electronics, Inc.
Title
ATI_ThamesXT_M2_MEM IF
Size
Document Number
LA-9104P
Rev
1.0
Date: Wednesday, August 29, 2012
Sheet 29 of 57

CHANNEL A: 256MB/512MB DDR3



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

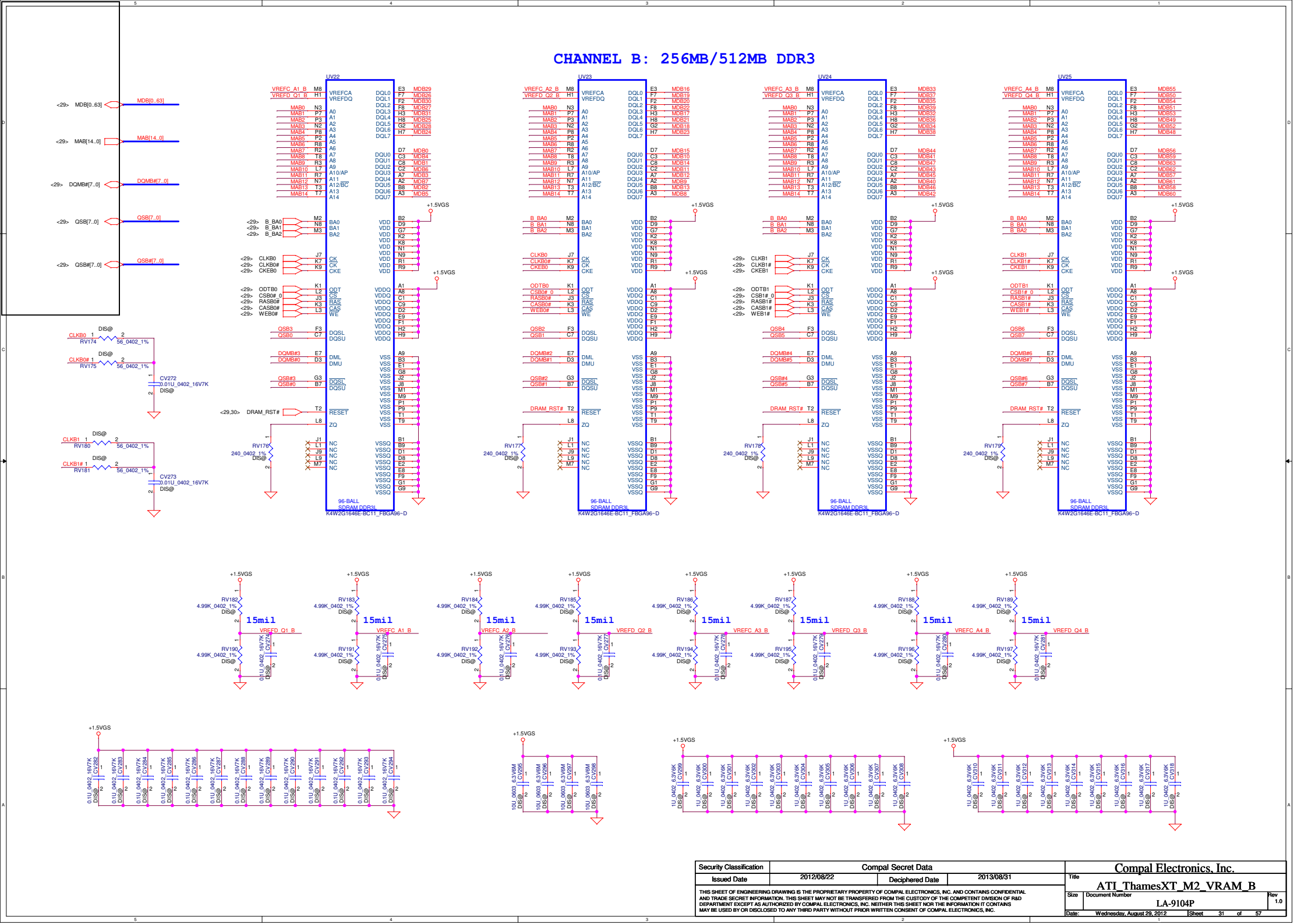
Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_VRAM_A

Size: | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 30 of 57

CHANNEL B: 256MB/512MB DDR3



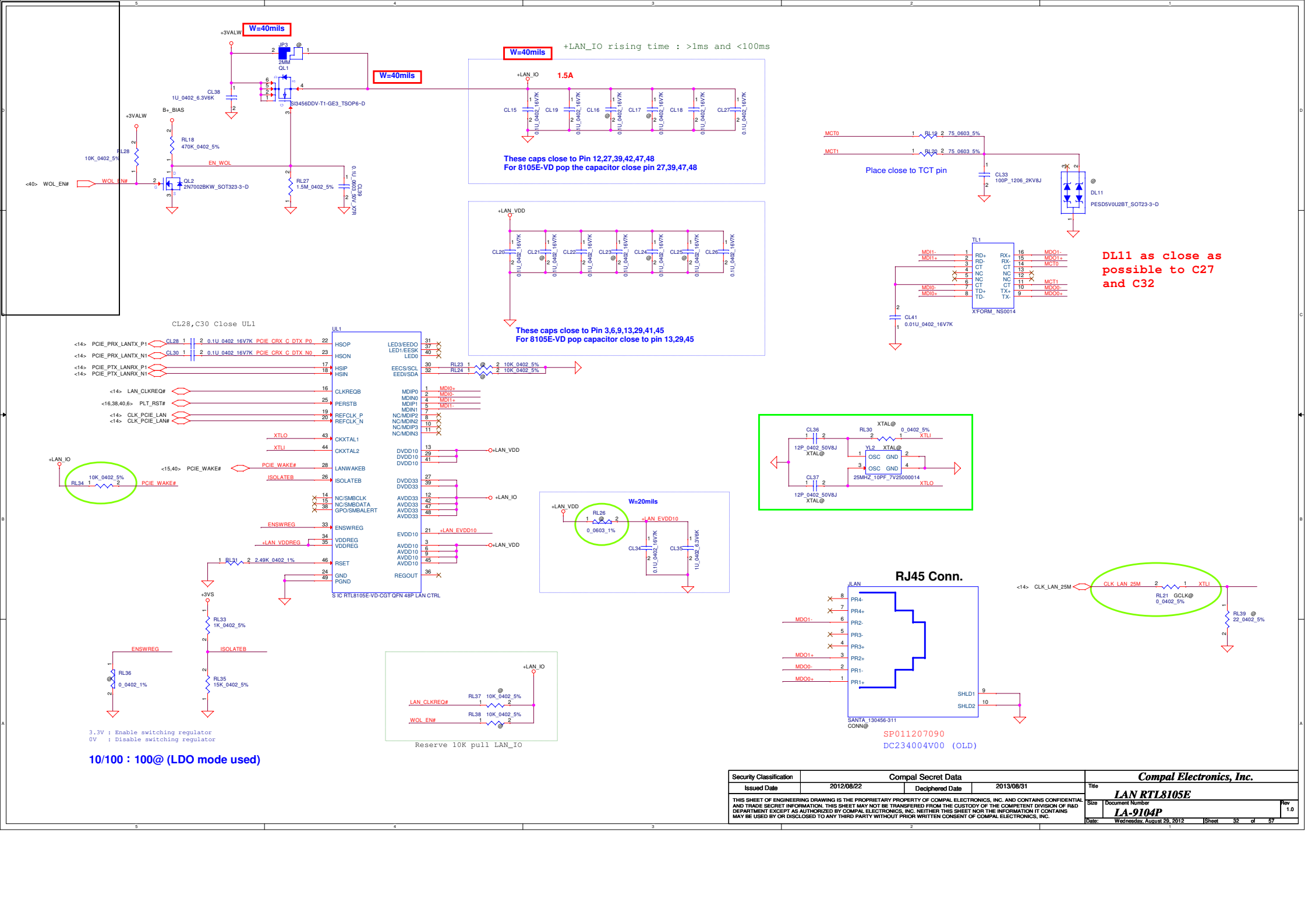
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_VRAM_B

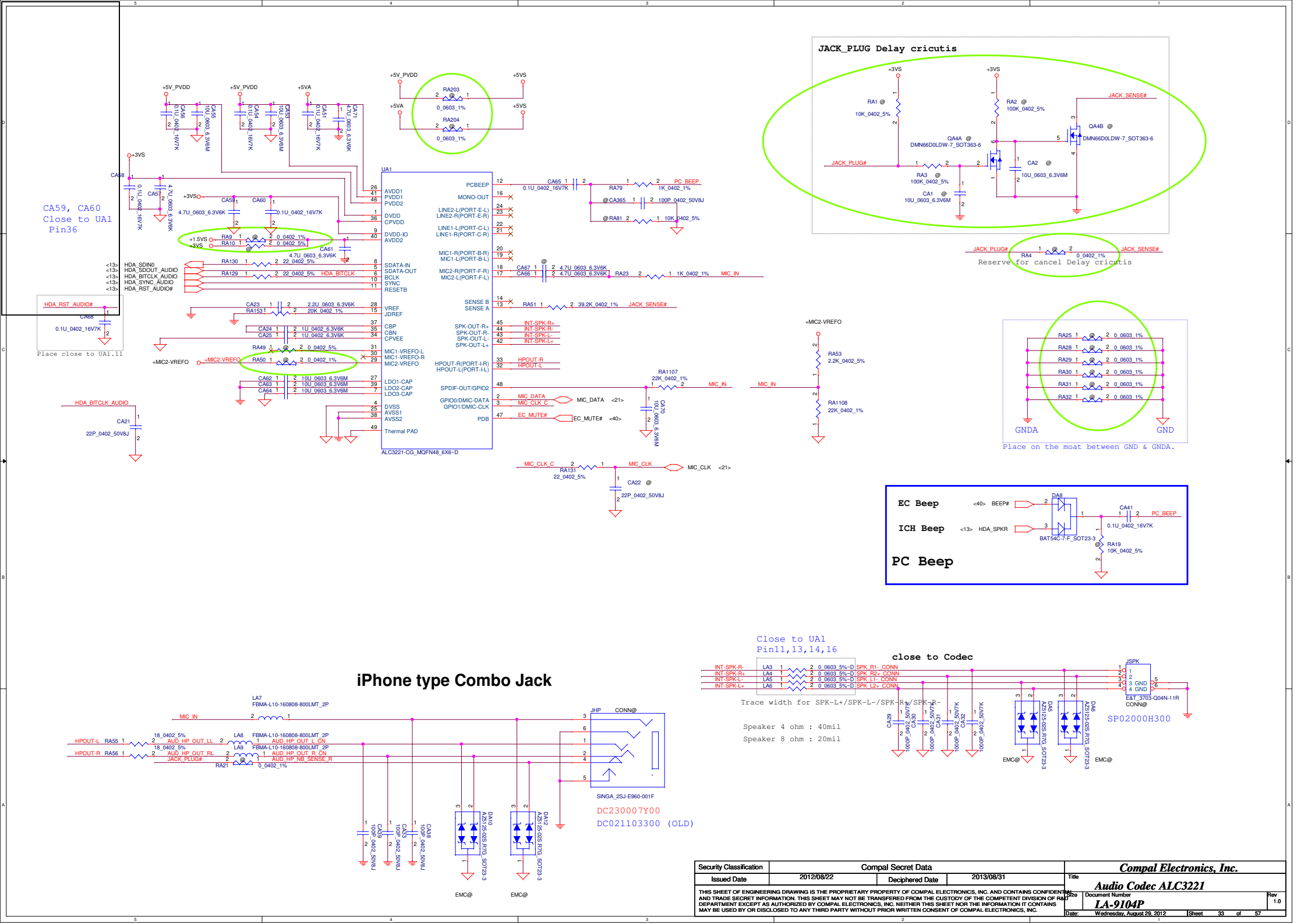
Size	Document Number	Rev
	LA-9104P	1.0

Date: Wednesday, August 29, 2012 | Sheet 31 of 57



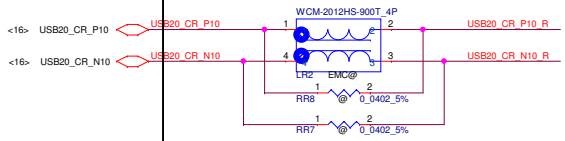
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

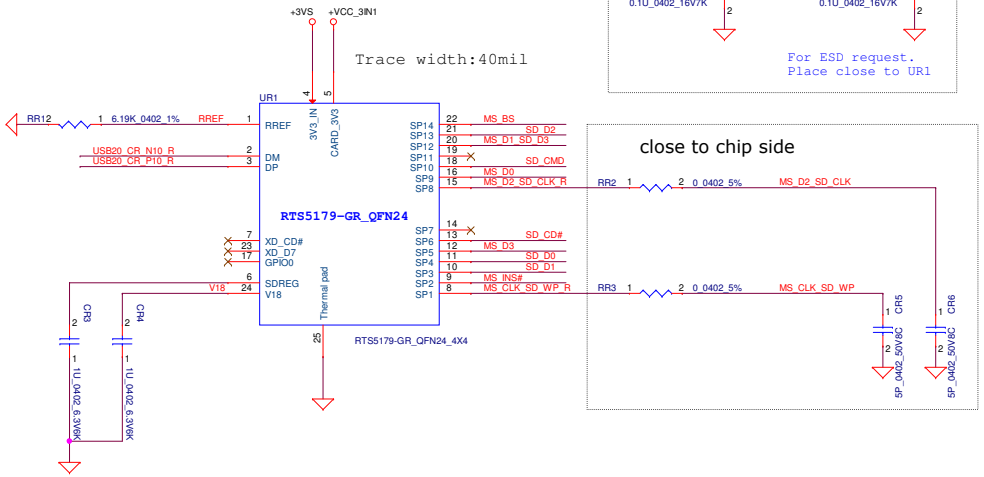
Compal Electronics, Inc.			
Title: LAN RTL8105E			
Size	Document Number: LA-9104P		Rev: 1.0
Date: Wednesday, August 29, 2012	Sheet 32 of 57		



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

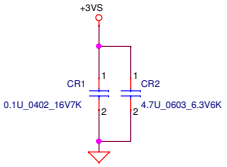
Compal Electronics, Inc.	
Title	Audio Codec ALC3221
Size	Document Number: LA-9104P
Rev	1.0
Date:	Wednesday, August 29, 2012
Sheet	33 of 57

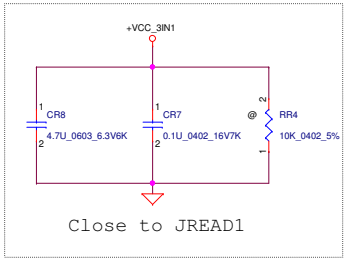


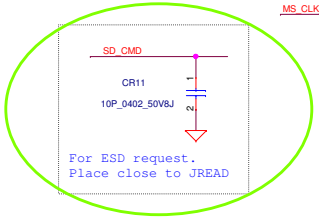


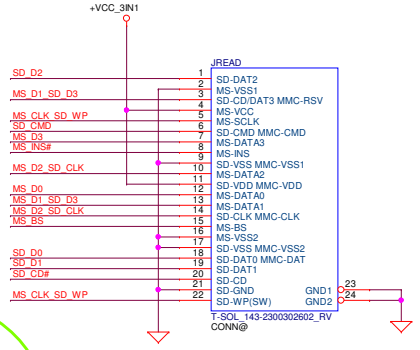
拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W









SP071204100
LTCX004AK00

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

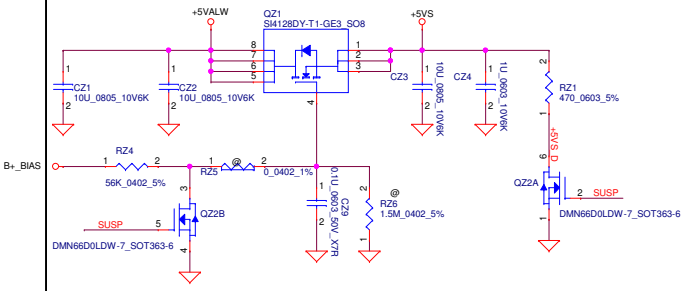
Compal Electronics, Inc.

Title: Card Reader RTS5179

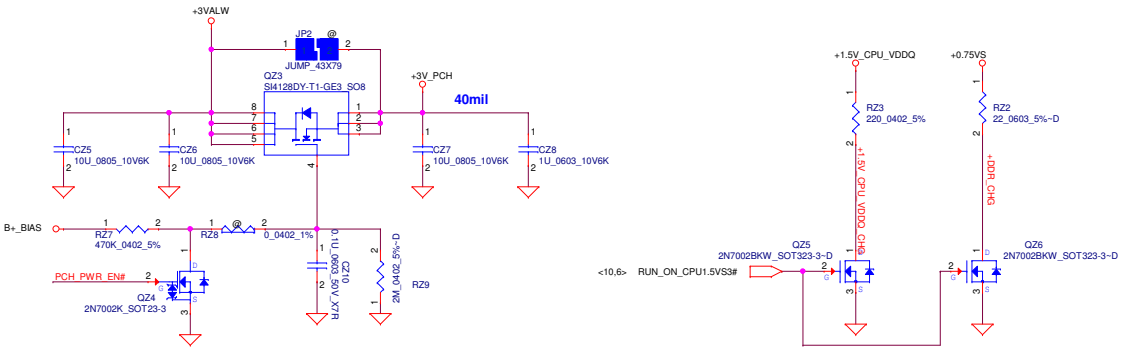
Size | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 34 of 57

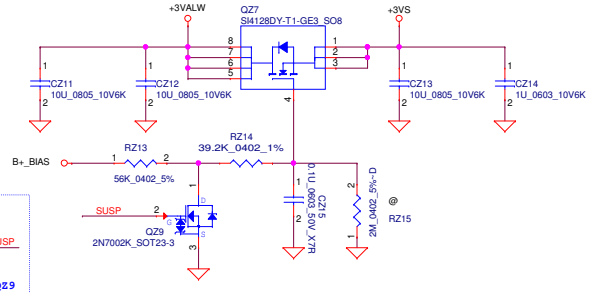
+5VALW to +5VS

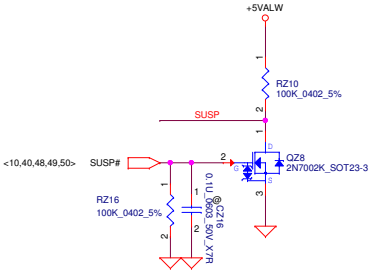


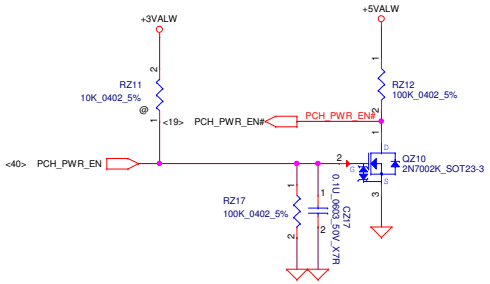
+3VALW to +3V_PCH



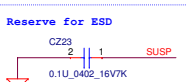
+3VALW to +3VS



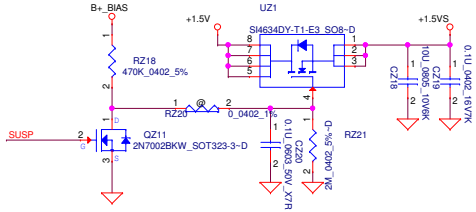


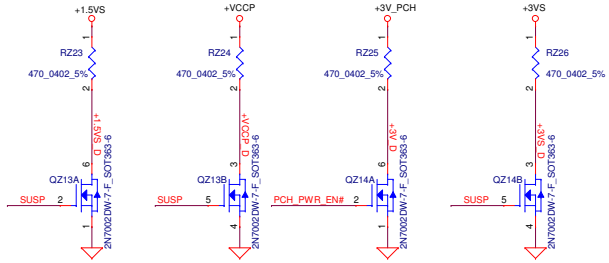


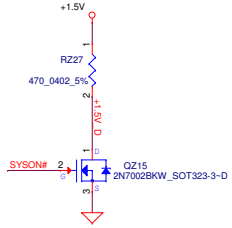
Reserve for ESD

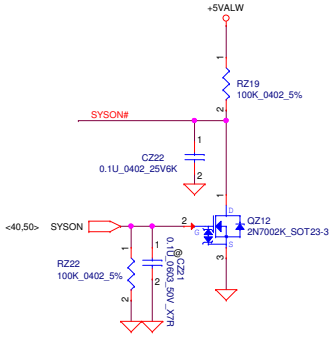


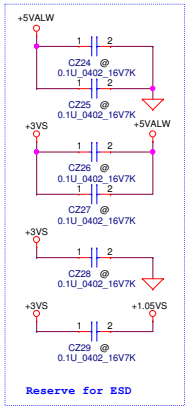
+1.5V To +1.5VS











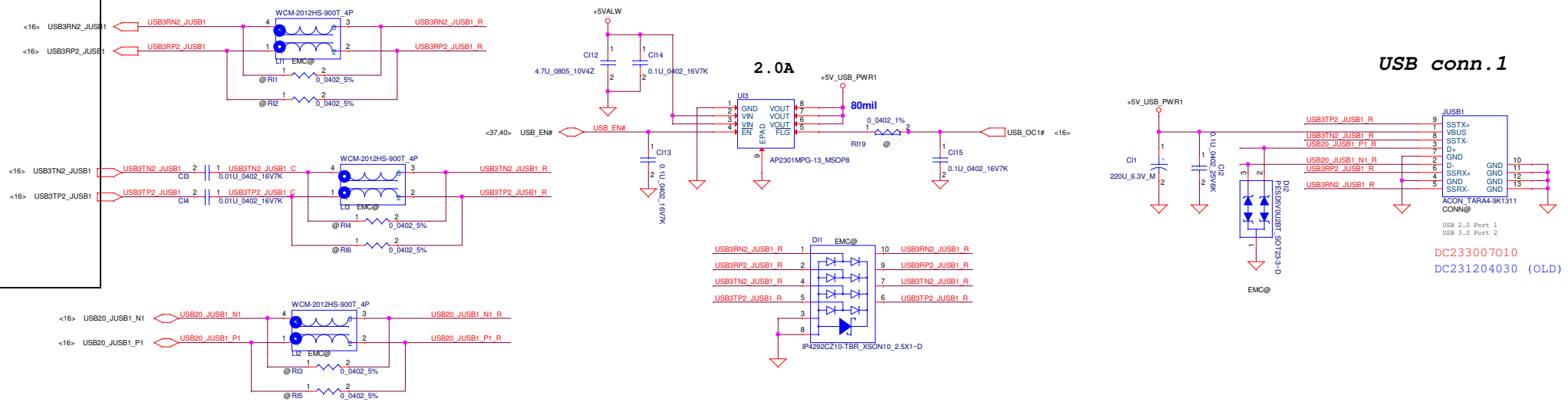
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

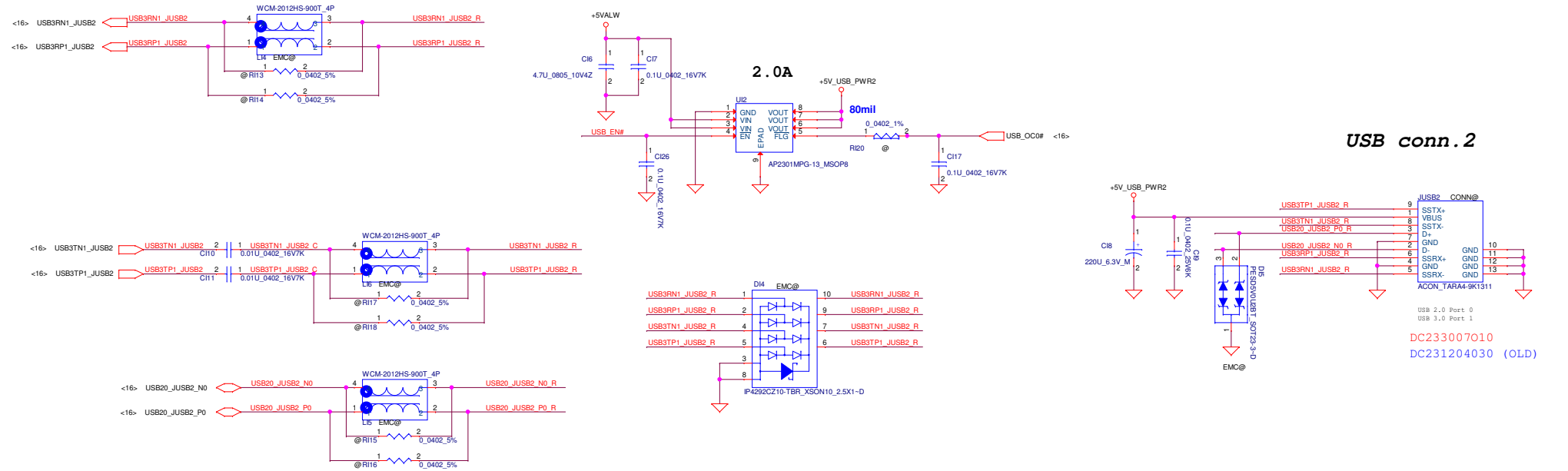
Compal Electronics, Inc.

Title: DC/DC Interface

Size | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 35 of 57





Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **USB3.0**

Size: Document Number: **LA-9104P** Rev: 1.0

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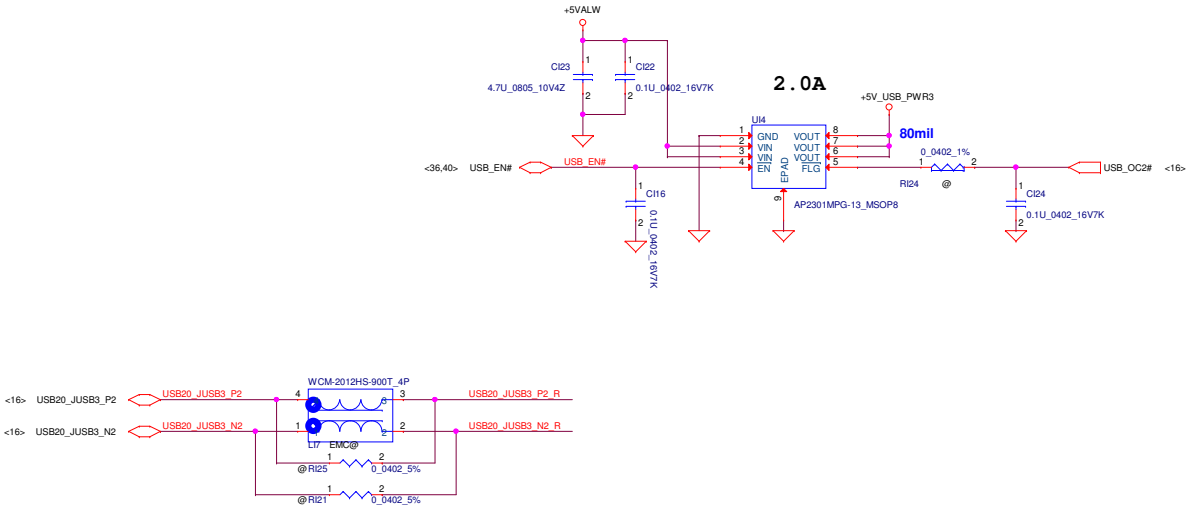
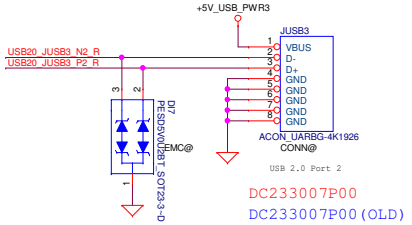
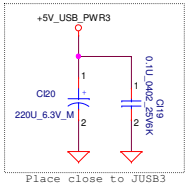
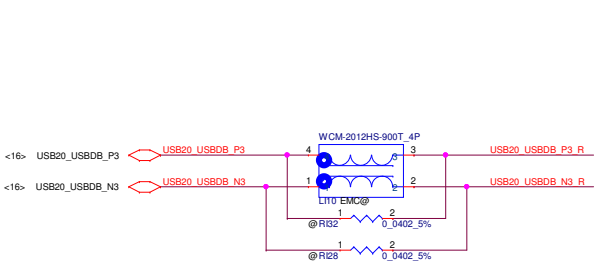
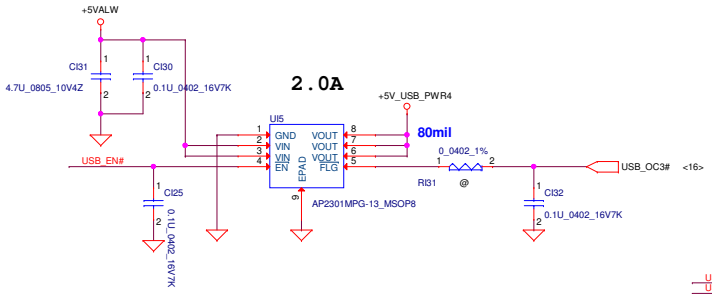


USB conn.3

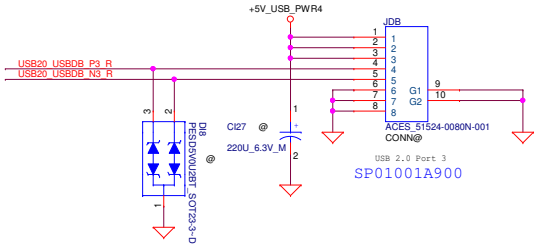








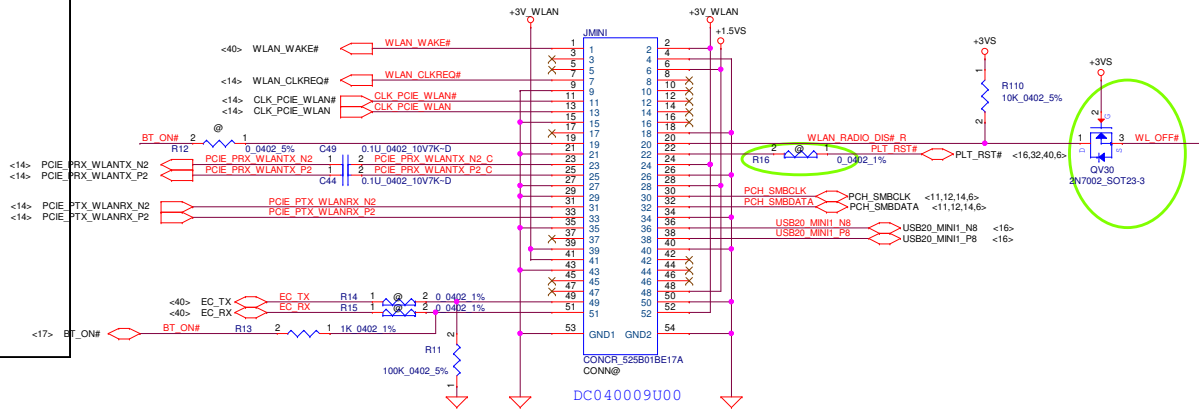
USB conn.4



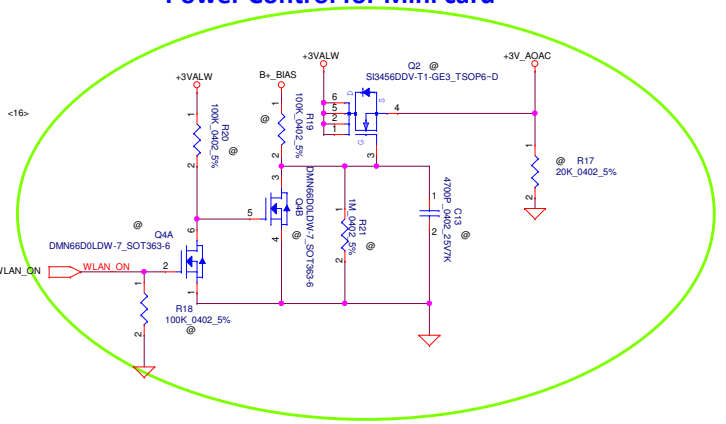
Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title: MB to USB2.0 DB			
Size	Document Number: LA-9104P		Rev: 1.0
Date: Wednesday, August 29, 2012	Sheet 37 of 57		

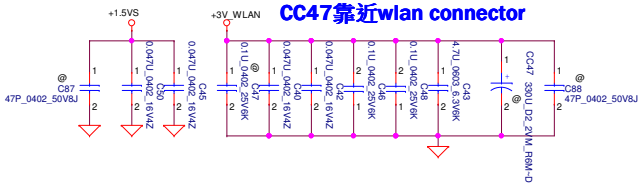
Mini WLAN/WIMAX H=6.7

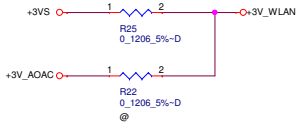


Power Control for Mini card

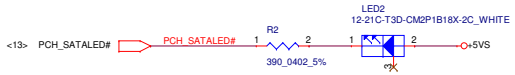


CC47靠近wlan connector

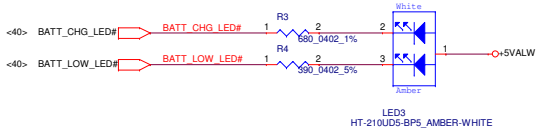




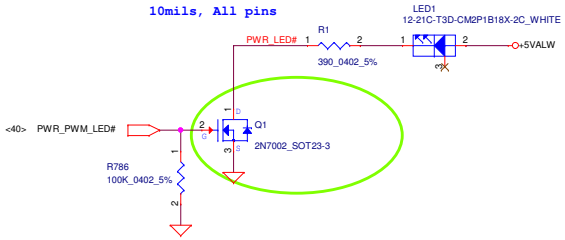
HDD LED



Battery LED



Power LED



Wireless LED

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: Mini Card/LED

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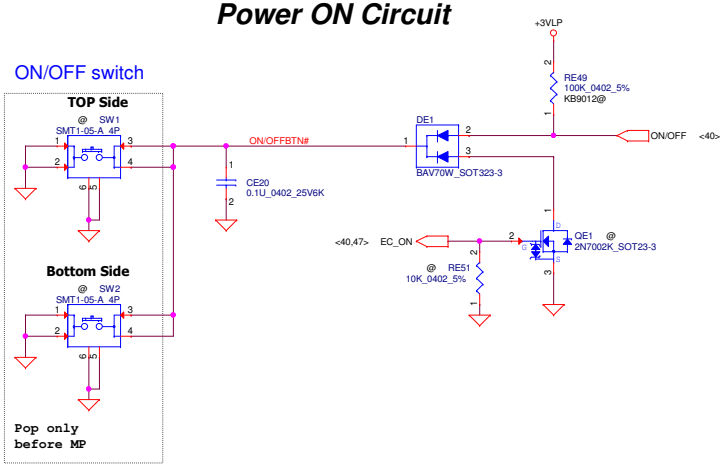
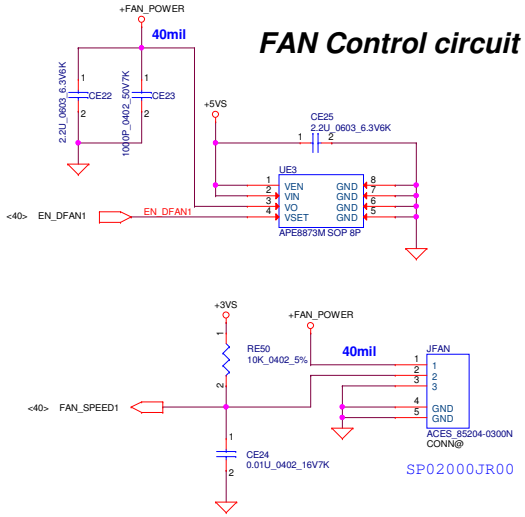
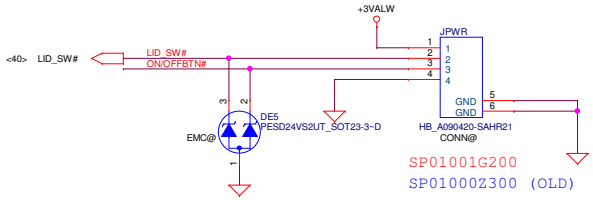
Power ON Circuit



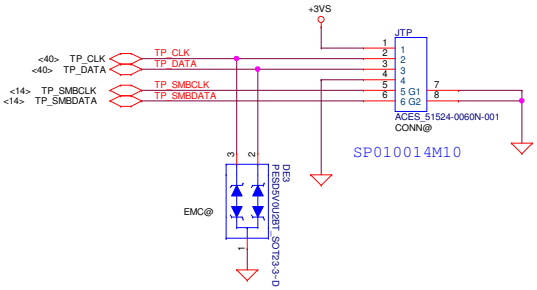
FAN Control circuit



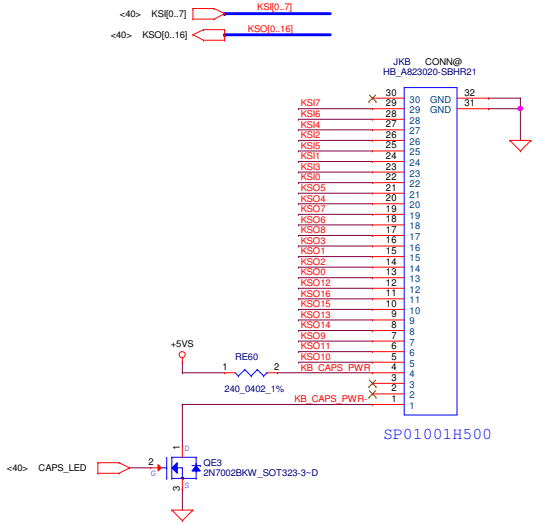
POWER/B



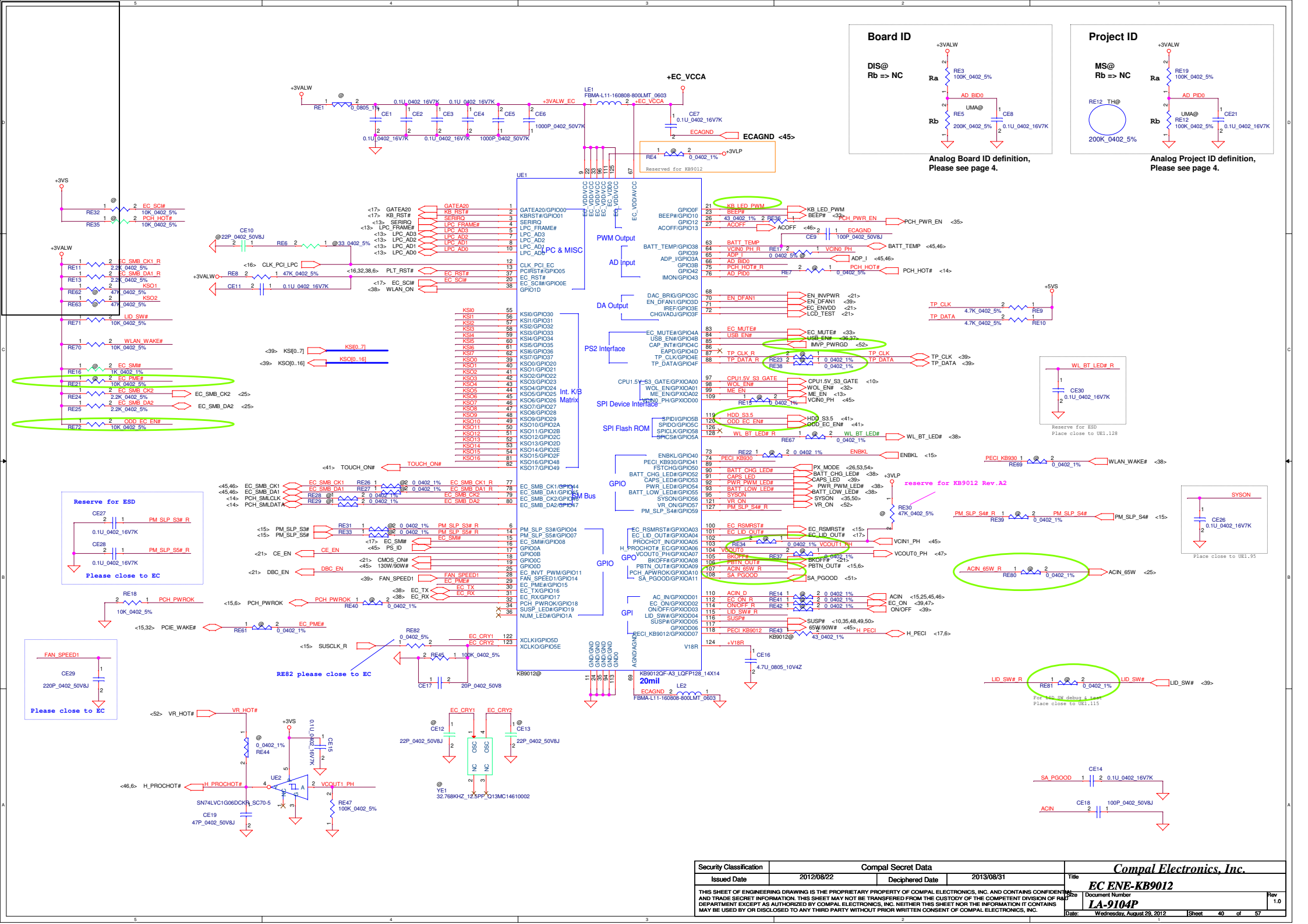
Touch pad



INT_KBD Conn.



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title: FAN/TP/KB/PWR SW
				Size: Document Number: LA-9104P Rev: 1.0
				Date: Wednesday, August 29, 2012 Sheet 39 of 57


Board ID
DIS@
Rb => NC
Analog Board ID definition,
Please see page 4.
Project ID
MS@
Rb => NC
200K_0402_5%
Analog Project ID definition,
Please see page 4.
+EC_VCCA
ECAGND <45>
UE1
PC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
KB9012@
KB9012QF-A3_LQFP128_14X14
20mil
reserve for KB9012 Rev.A2
Reserve for ESD
Please close to EC
RE82 please close to EC
Please close to UE1.128
Please close to UE1.95
Please close to UE1.115
Compal Electronics, Inc.
EC ENE-KB9012
LA-9104P
Compal Secret Data
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2013/08/31
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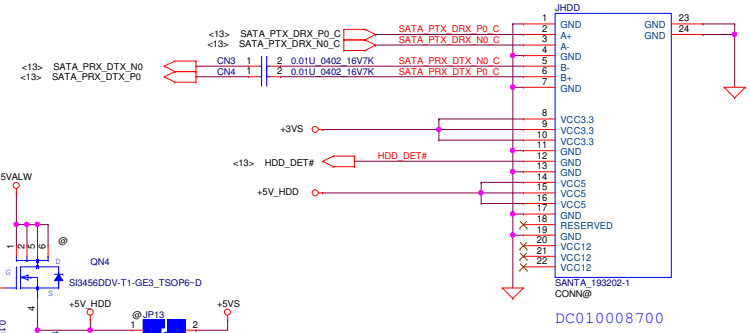
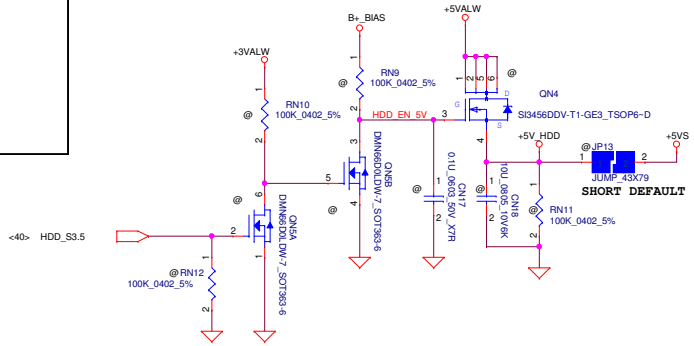
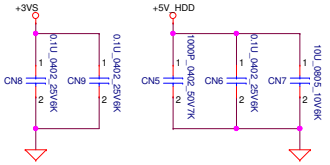
1.0

SATA HDD Conn.

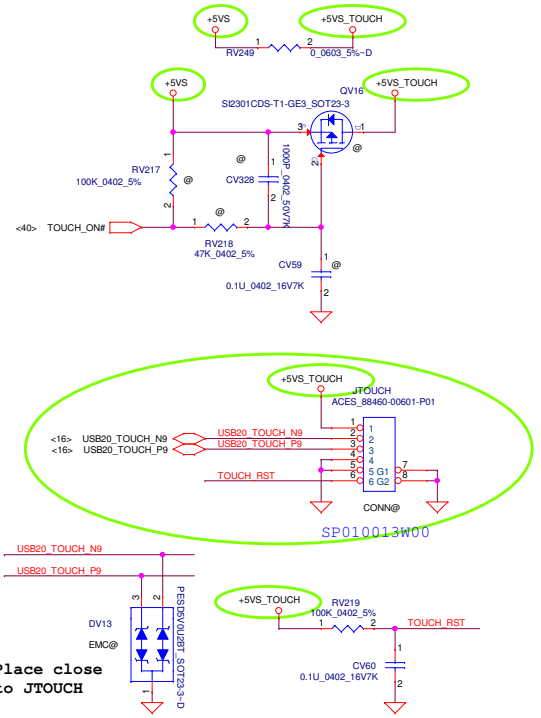


+5V_HDD Source

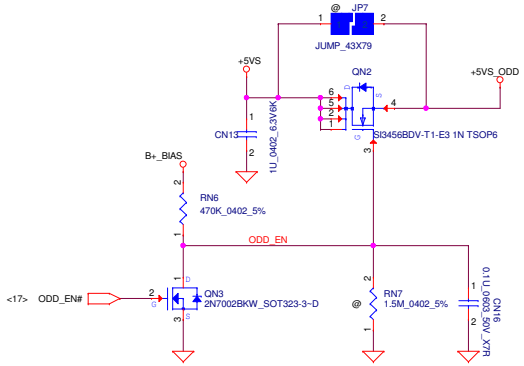


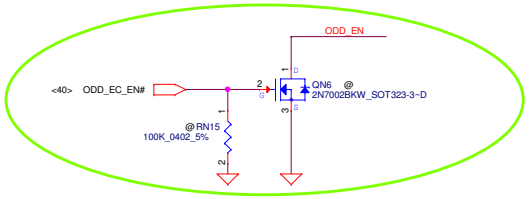


* Touch Screen Panel

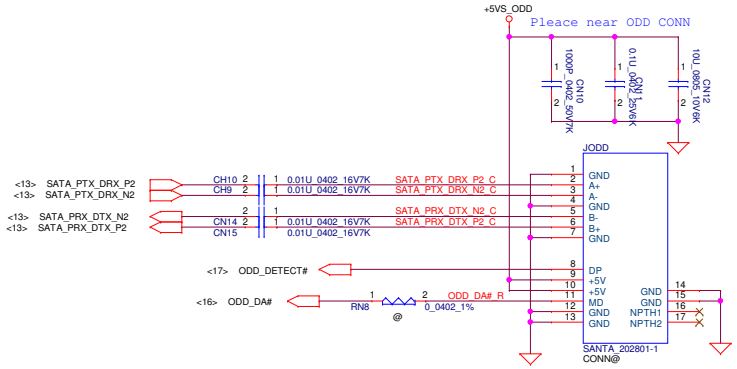


ODD Power Control





SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: HDD / ODD

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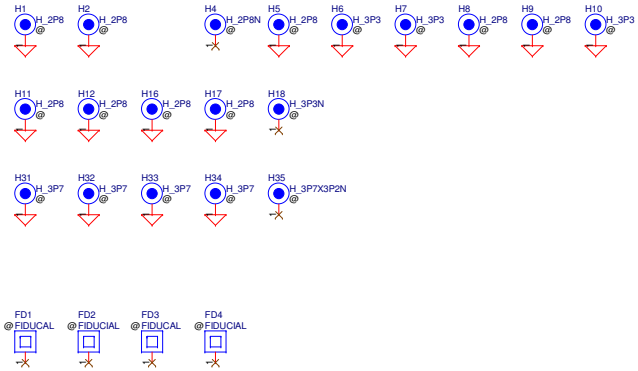
Screw Hole



Compal Electronics, Inc.		
Title: Screw Hole		
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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	21,39	LVDS	2012/05/17	SED	Add FHD Panel CE_ENABLE, DBC_ENABLE function from SED request	Add CE_EN, DBC_EN control pin to EC	0.2
2	21	LVDS	2012/05/22	SED	Follow SED team request disable CE_EN function	Change RV62 to DE-POP and RV100 to POP for disable CE_EN function	0.2
3	33	Audio codec	2012/05/23	CODEC	Follow CODEC vendor suggestion	Add AUDIO JACK PLUG delay circuit, Spearate NET JACK_PLUG to => JACK_SENSE# & => JACK_PLUG#	0.2
4	16,21	Touch Screen	2012/05/29	HW	Add touch screen function	Add RV217, RV218, RV219, RV249, CV59, CV60, CV328, DV13, QV16, JTOUCH	0.2
5	39	Board ID	2012/05/30	HW	Board ID change for PT	Change RE5 from 8.2k_0402(SD028820180) to 33k_0402(SD028330280)	0.2
6	21,39	Touch Screen	2012/05/30	HW	Add touch screen function power control	Add NET "TOUCH_ON#" from JTOUCH to UE1.82(KB9012) for TOUCH SCREEN PANEL power control	0.2
7	33	Audio codec	2012/05/30	HW	Follow RealTek suggestion remove, delete reserve MUTE circuit	Delete D1,QA1,QA2,QA3,RA24,RA26,RA60,RA62,RA68,RA109,CA72,CA73	0.2
8	15,16, 39,41	ESD	2012/05/30	ESD	ESD ask CAP for reserve	Reserve 0.1u/0402 CH104,CZ23,CH105,CE27,CE29	0.2
9	14	Green CLK	2012/05/30	HW	For Green CLK test	Change RH31,RH41,RV232 0ohm form "GCLK@" to "@" for break the clock signal to device	0.2
10	10,26,41	DC/DC	2012/05/31	HW	Change "+1.5V_CPU_VDDQ", "+1.5VS", "+1.5VGS" derating	Change RC150 330K/0402 to 2M/0402, RC151 100K/0402 to 470K/0402, RZ18 100K/0402 to 470K/0402, RV115 0/0402 to 2M/0403	0.2
11	41	DC/DC	2012/05/31	HW	For power sequence trunning	Change RZ15 to DE-POP	0.2
12	06,15,16, 39,41	ESD	2012/05/31	ESD	Follow ESD team request	Change 0.1u/0402 from "@" to POP	0.2
13	32	Green CLK	2012/06/15	HW	Change for Green CLK bom control	Change RL21,RL30 from "@" to "GCLK@"	0.2
14	41	DC/DC	2012/06/15	HW	For WLAN card power sequence issue	Change RZ4,RZ13 from 470K/0402 56K/0403	0.2
15	35,41	Schematic page modify	2012/06/18	HW	Schematic page modify for easily maintain.	Swap Page. 35 & Page 41.	0.2
16	41	ODD	2012/06/18	HW	Change component location for easily maintain.	Move CH9,CH10 from Page.13 to Page.41	0.2
17	39	FAN	2012/06/29	HW	Fan speed noise issue	Reserve 220p/0402 CE24	0.2
18	6	CPU	2012/06/29	ESD	System boot-up shot down issue.	Change CC151 from POP to "@"	0.2
19	21,35, 39,40,41	Circuit adjuest	2012/07/01	HW	Circuit & page adjust for OAK 15" & OAK 17"	1. Swap P.35 & P.41and move touch screen circuit from P.21 to P.41. 2. Swap P.39 & P.40 page no	0.2
20	40	LID SW	2012/07/01	HW	LID SW need a trace for debug and switch.	Add RE81 for LID SW.	0.2
21	25	GPU	2012/07/01	HW	Follow AMD request, MarsPro will used MPLs.	Change RV75,RV76,RV81 from "DIS@" to "TH@"	0.2
22	29	GPU	2012/07/01	HW	Follow AMD request, MEM_CALRP2 is not need for Mars ASIC now.	Change RV205 from "MS@" to "@"	0.2
23	38	MINI card	2012/07/03	HW	Power Control for Mini card didn't need	Change R17 to "@"	0.2
24	6	XDP	2012/07/06	HW	S3 return hang issue	Change RC89 from "@" to POP	0.2
25	23	GREEN CLK	2012/07/09	HW	Follow Green CLK FAE suggestion	1. Change UG1.2(+3VLP) & UG1.8(+3VALW) connect to +LAN_IO 2. Add R787 connect from +RTCBATT to C5.2 & UG1.10 3. Change C14 from 0.1u to 5p/0402 4. Change C8 connect from +3V_ALW to +LAN_IO 5. Add R788 0ohm/0402 from +RTCVCC to UG1 for GCLK & DH1 select	0.2
26	35	MOAT	2012/07/09	ESD	For ESD request reserve CAP.	Reserve those CAP for ESD MOAT.	0.2
27	18	LVDS	2012/07/10	HW	Change RES and reserve CAP for LVDS issue	Change RH185 from 0ohm-short to 0ohm/0805, and reserve CH106 1U/0402	0.2
28	13	PCH	2012/07/11	ESD	Follow ESD team request	Add RH44,RH48,RH70 & NET PCH_JTAG_TMS_R, PCH_JTAG_TDI_R, PCH_JTAG_TDO_R for break signal trace	0.2
29	40	PCH	2012/07/11	ESD	Follow ESD team request	1.Change NET NAME "N59110727" to "WL_BT_LED#_R" 2. Reserve 0.1u/0402 on "WL_BT_LED#_R" for ESD	0.2
30	21	LVDS	2012/07/11	HW	Reserve for CE function for LVDS connector	Change CE_EN_R from dummy to JLVDS.18	0.2
31	32	Connector	2012/07/12	ME	For ME request	Change JLAN CPN from "DC234004V00" to "SP011207090"	0.2
32	40	FAN	2012/07/16	HW	For FAN_SPEED1 noise issue	Change CE29 from "@" to POP	0.2
33	14	Touch PAD	2012/07/17	SED	Change Touch PAD SMBUS port for SMBUS issue	Change Touch PAD SMBUS port for SMB0 to SMB	1.0
34	32	GREEN CLK	2012/07/19	HW	Follow Silego FAE request	Change RL21 from 510 ohm to 0 ohm/0402	1.0
35	41	Touch Screen	2012/08/07	SED	Follow SED team request change JTOUCH USB signal conatct.	Change JTOUCH Pin define.	1.0
36	34	Card Reader	2012/08/14	ESD	Follow ESD team request	Reserve CR11 100p/0402 close to JREAD	1.0
37	23	GREEN CLK	2012/08/16	HW	Fixed GCLK output abnormal issue	Change UG1.2(UG1/VDD) from +LAN_IO to+3VALW	1.0
38	33	CODEC	2012/08/16	HW	The issue already fixed by new CODEC.	Remove delay circuit and POP RA4	1.0
39	23	GREEN CLK	2012/08/17	HW	For RTC discharge issue	De-pop R788	1.0
40	32,34	LAN	2012/08/17	HW	For LAN Chip abnormal leakage issue	Pop RL34 and de-pop RE21	1.0
41	34	Card Reader	2012/08/20	ESD	Follow ESD team request	Change CR11 from 100p/0402 to 10p/0402 and POP	1.0

Compal Electronics, Inc.

Title: HW-PIR

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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
42	41	Touch Screen	2012/08/20	SED	Follow SED team request	Change Touch screen power rail for +3VS to +5VS	1.0
43	38	LED	2012/08/20	HW	Change LED light	Change LED1,LED2,LED4 CPN from SC500006O00 to SC50000DC00	1.0
44	38	WLAN	2012/08/20	HW	Remove AOAC function power control	Change R18,R19,R20,R21,C13,Q2,Q4 component BOM structure to "@"	1.0
45	41	Touch Screen	2012/08/20	HW	Add EC control for Touch Screen function	Add RN15 & QN6 and relative circuit connect	1.0
46	40	BATMAN2	2012/08/21	HW	For BATMAN2	Add RE82 0ohm/0402 between trace SUSCLK_R & EC_CRY2	1.0
47	14,17	PCH	2012/08/21	HW	For SYSTEM S3 leakage issue	Change RH79.2 & RH245.2 connect from +3V_PCH to +3VS	1.0

Compal Electronics, Inc.

Title: HW-PIR

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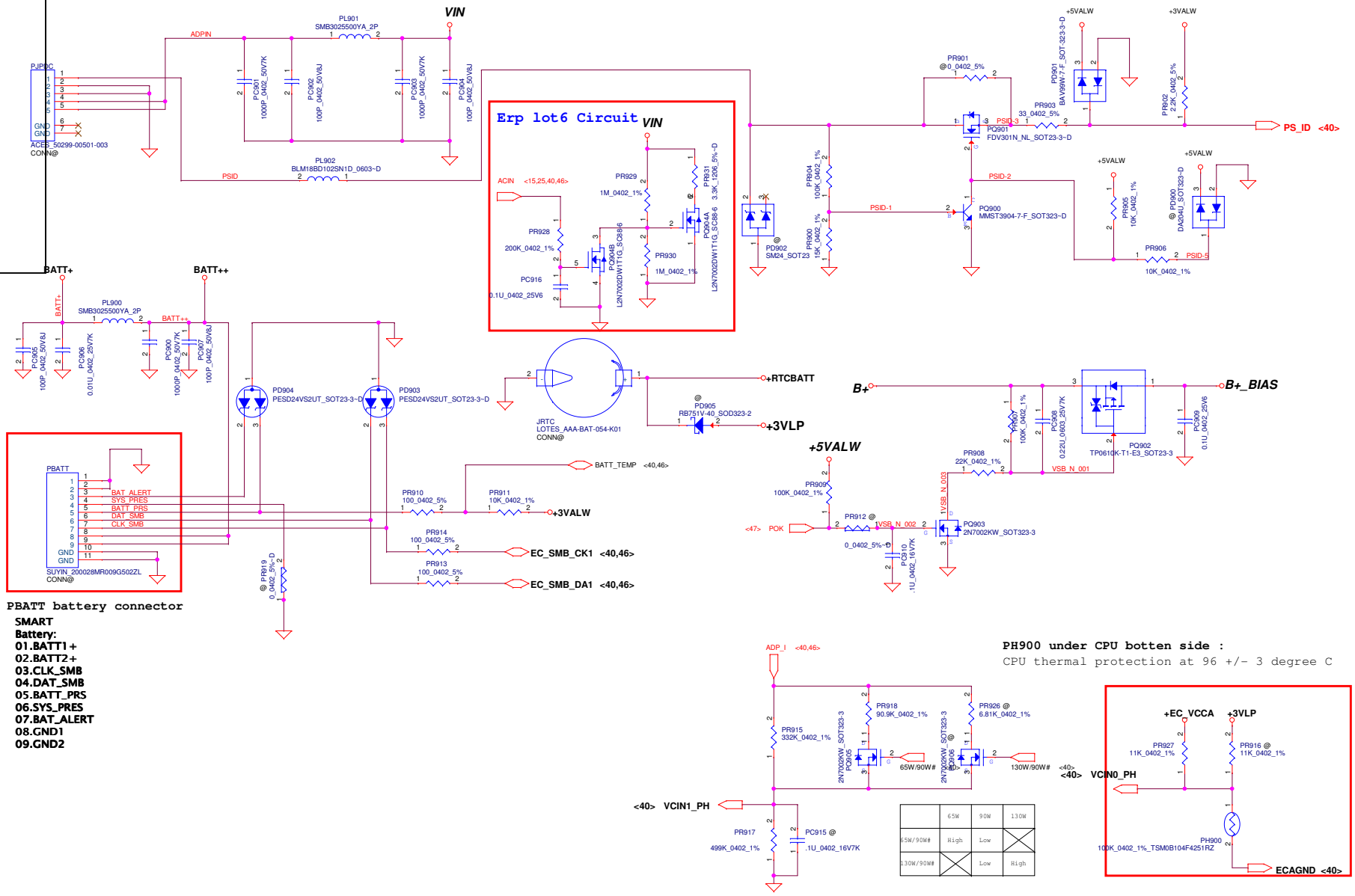

	65W	90W	130W
65W/90W#	High	Low	
130W/90W#		Low	High

Compal Electronics, Inc.

Title: PWR_DCIN/BATT CONN/OTP

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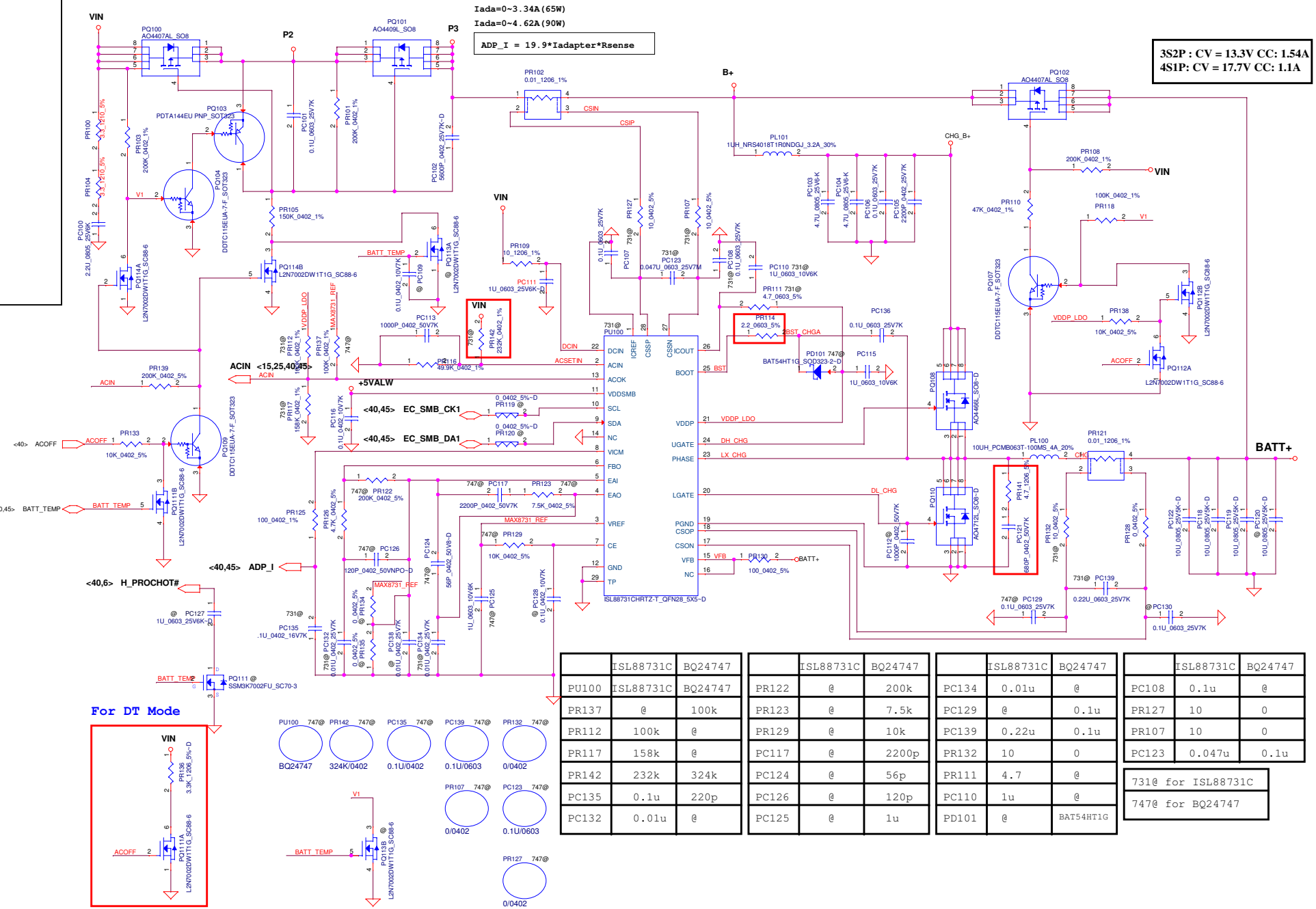

	ISL88731C	BQ24747
PU100	ISL88731C	BQ24747
PR137	@	100k
PR112	100k	@
PR117	158k	@
PR142	232k	324k
PC135	0.1u	220p
PC132	0.01u	@

	ISL88731C	BQ24747
PR122	@	200k
PR123	@	7.5k
PR129	@	10k
PC117	@	2200p
PC124	@	56p
PC126	@	120p
PC125	@	1u

	ISL88731C	BQ24747
PC134	0.01u	@
PC129	@	0.1u
PC139	0.22u	0.1u
PR132	10	0
PR111	4.7	@
PC110	1u	@
PD101	@	BAT54HT1G

	ISL88731C	BQ24747
PC108	0.1u	@
PR127	10	0
PR107	10	0
PC123	0.047u	0.1u

731@ for ISL88731C
747@ for BQ24747

PU100	747@	PR142	747@	PC135	747@
BQ24747		324K/0402		0.1U/0402	

PC139	747@	PR132	747@	PR107	747@
0.1U/0603		0/0402		0/0402	

PC123	747@	PR127	747@
0.1U/0603		0/0402	

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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Compal Electronics, Inc.	
Title	PWR_CHARGER
Size	Document Number: LA-9104P
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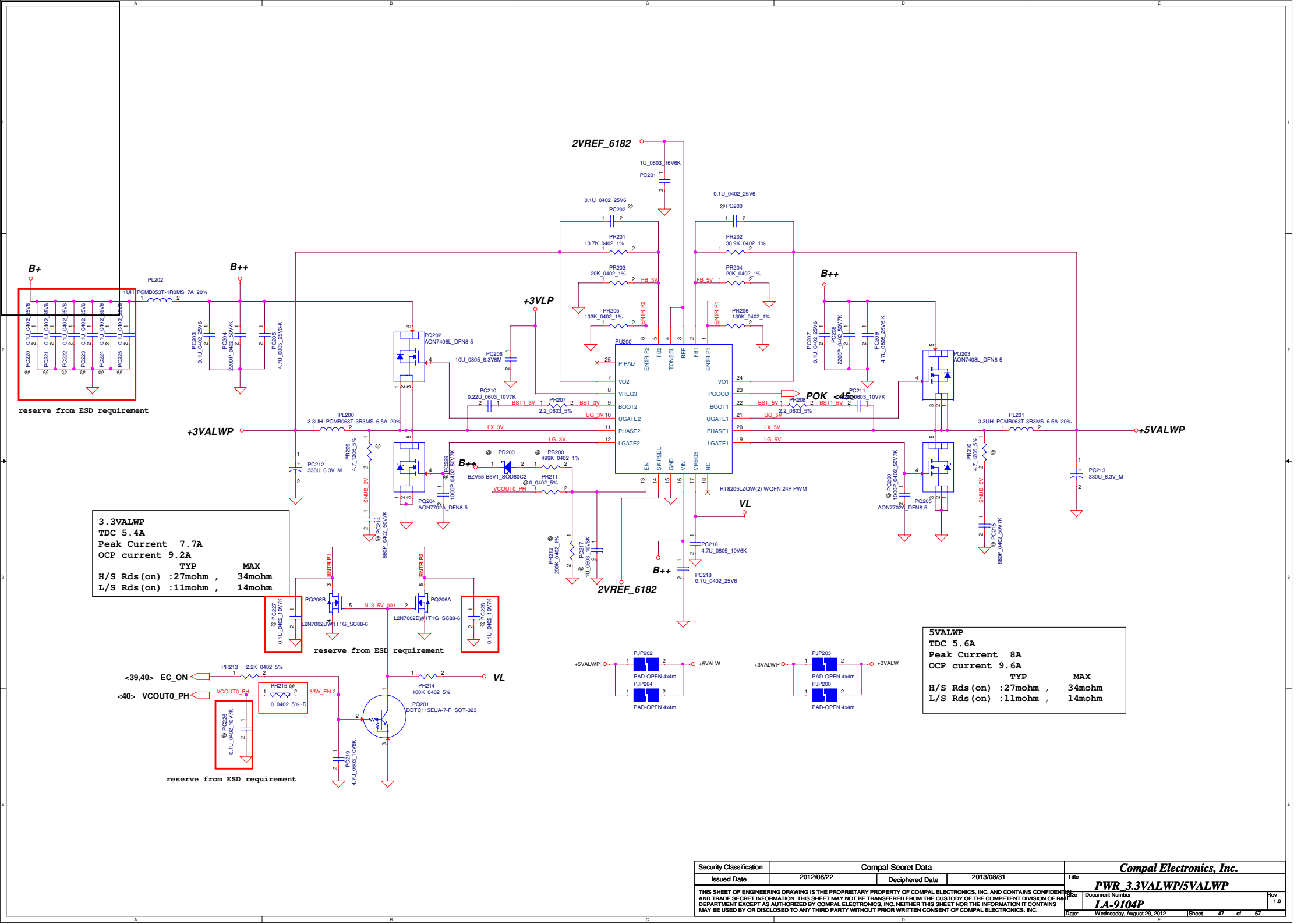
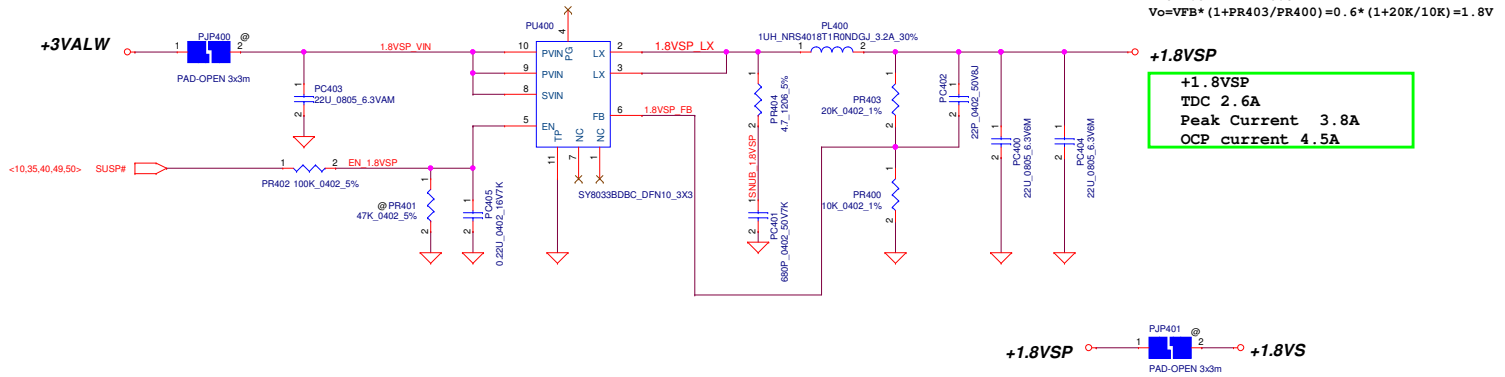
Sheet	46 of 57

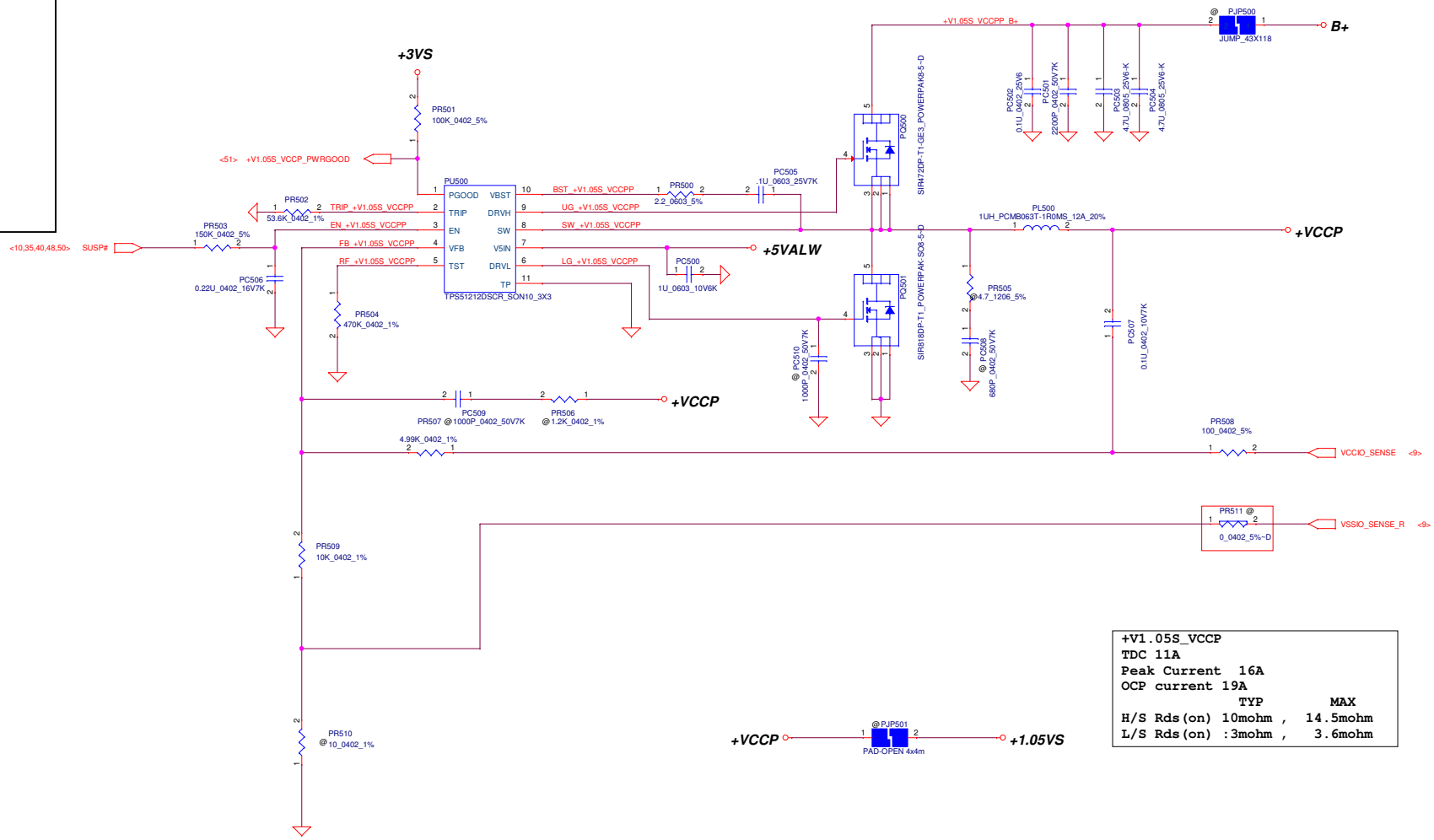


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title: PWR_3.3VALWP/5VALWP
				Size: Document Number: LA-9104P Rev: 1.0
				Date: Wednesday, August 29, 2012 Sheet 47 of 57



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Title	PWR_1.8VSP		
Size	Document Number		Rev
	LA-9104P		1.0
Date:	Wednesday, August 29, 2012	Sheet 48 of 57	



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PWR_+VCCIO

Size: | Document Number: LA-9104P | Rev: 1.0

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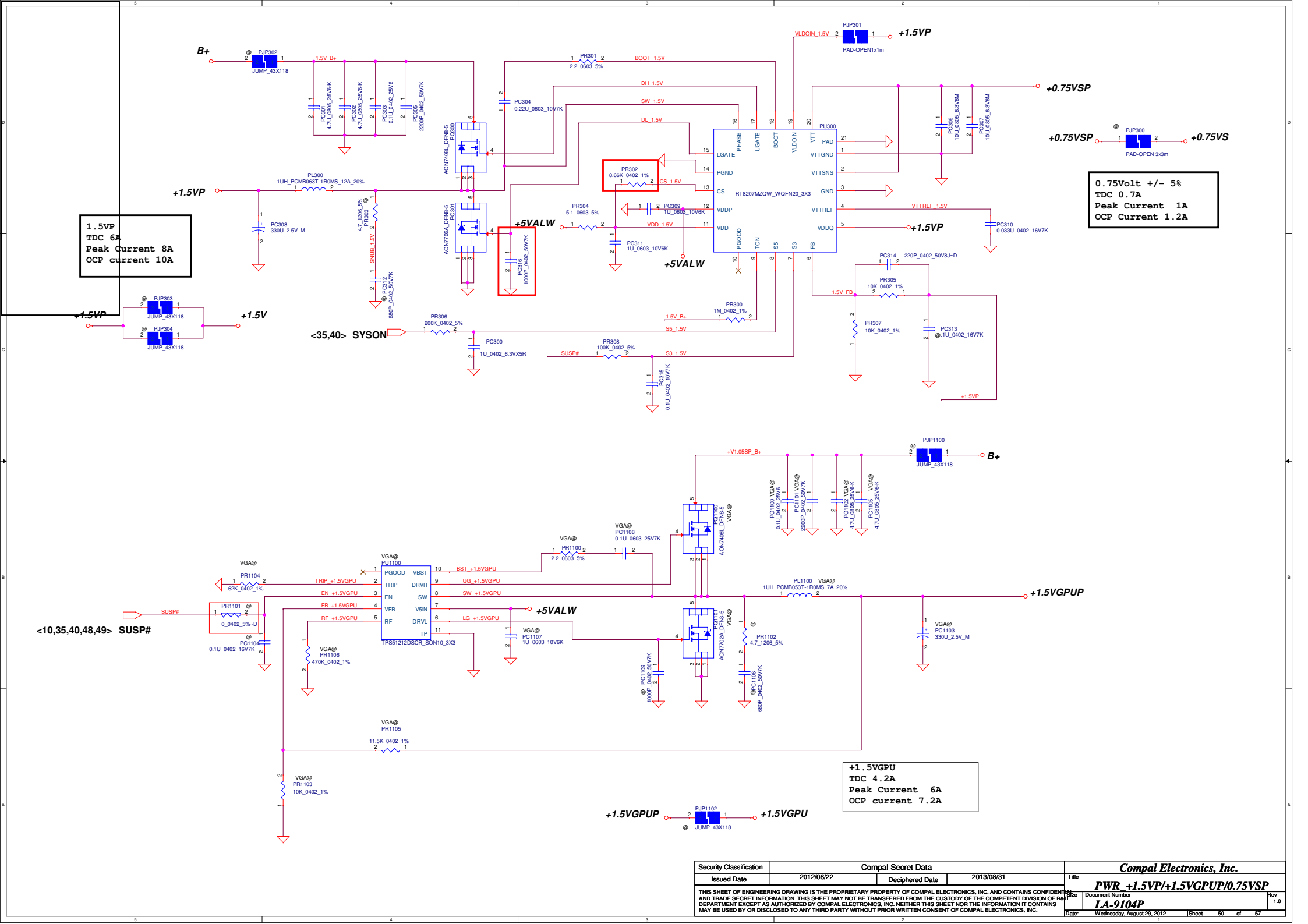

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PWR_+1.5VP/+1.5VGPUP/0.75VSP

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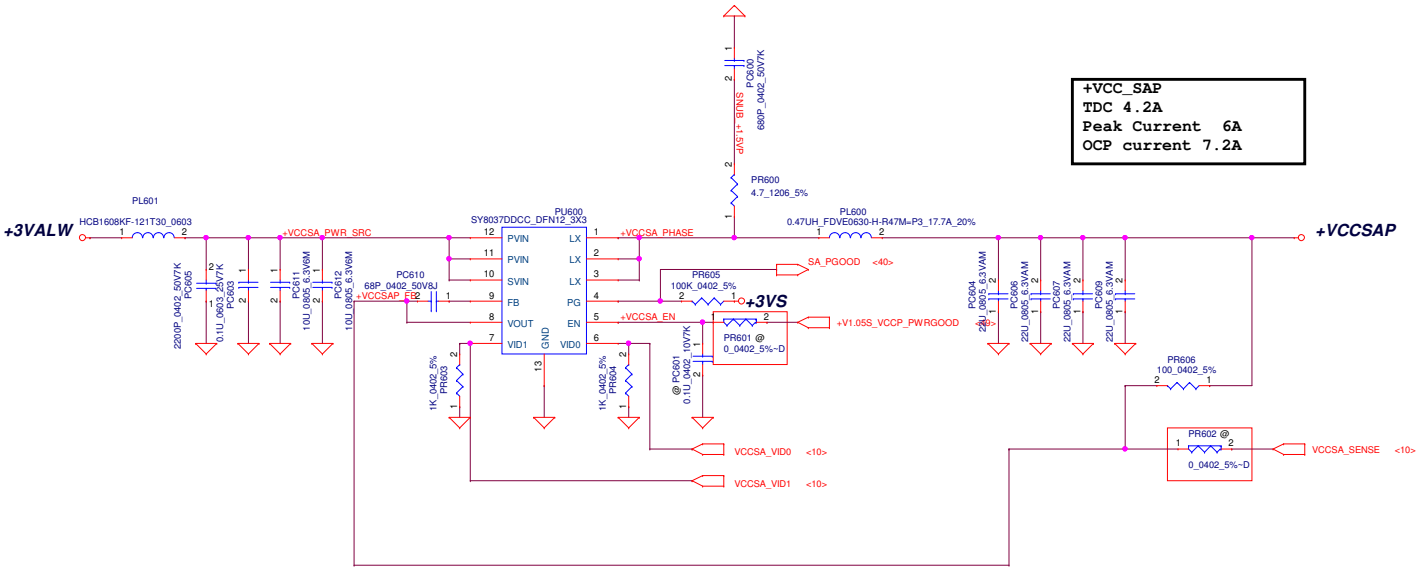
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

reserve for Pentium and Celeron only

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PWR_+VCCSAP

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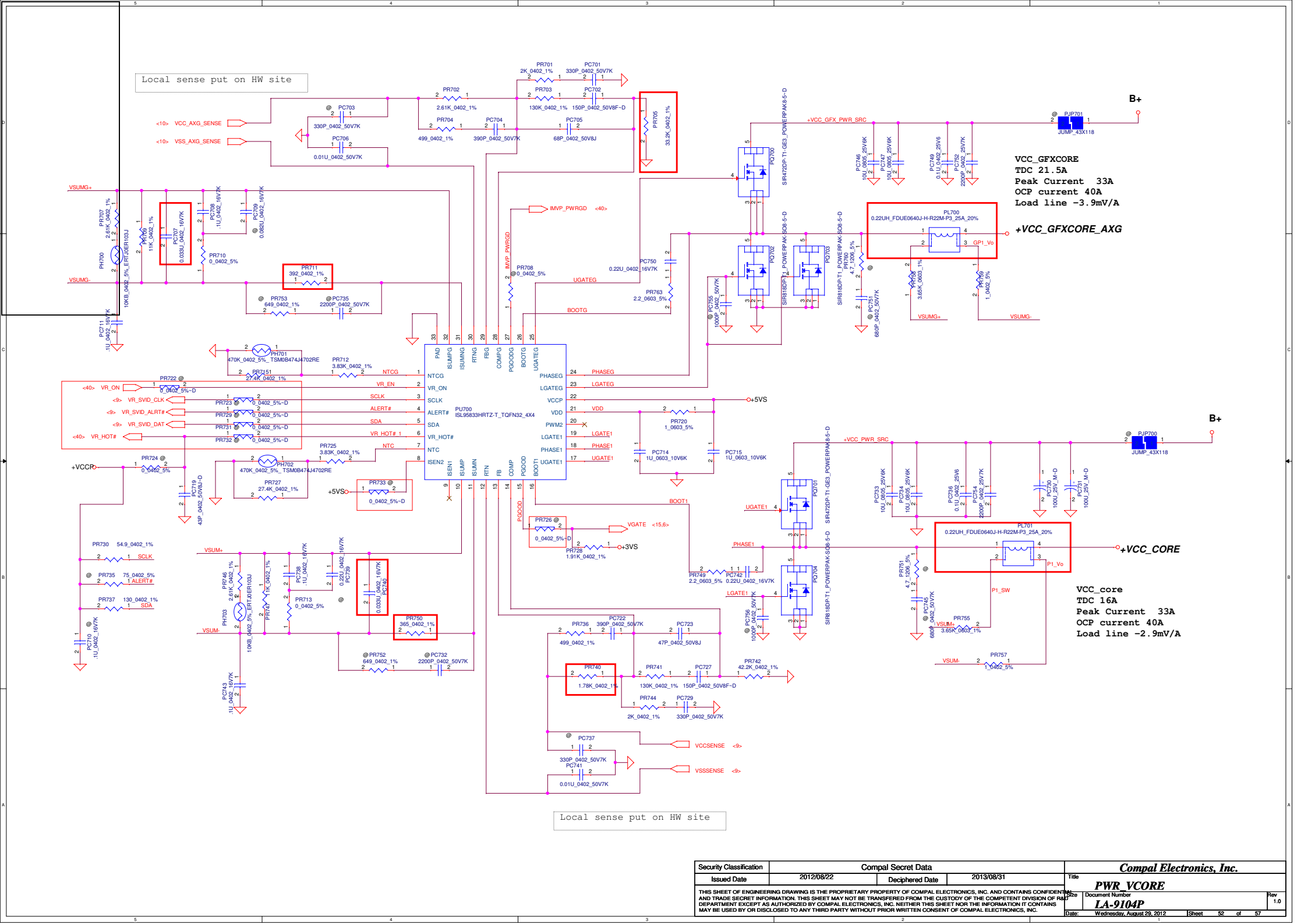

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PWR_VCORE

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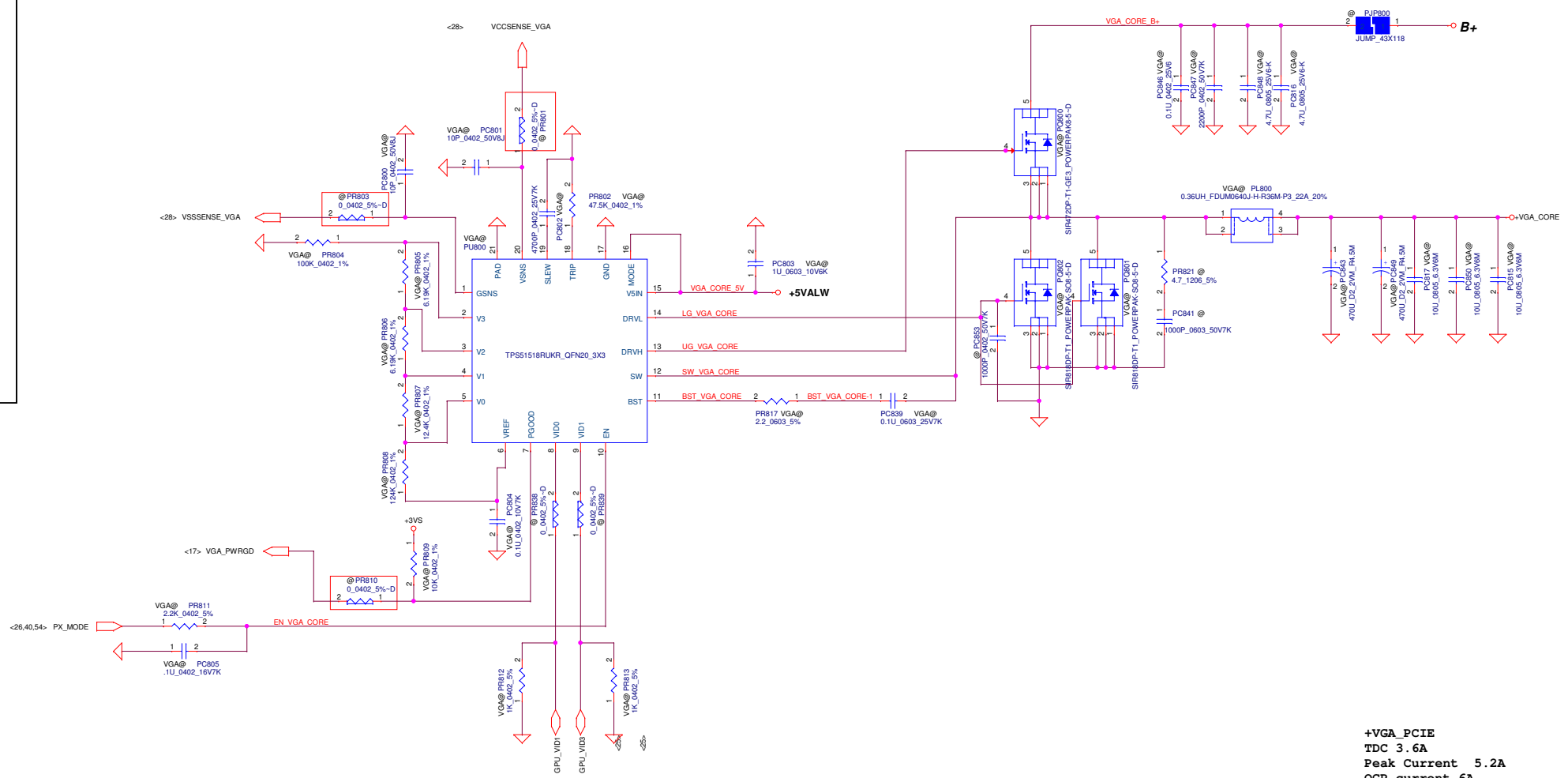
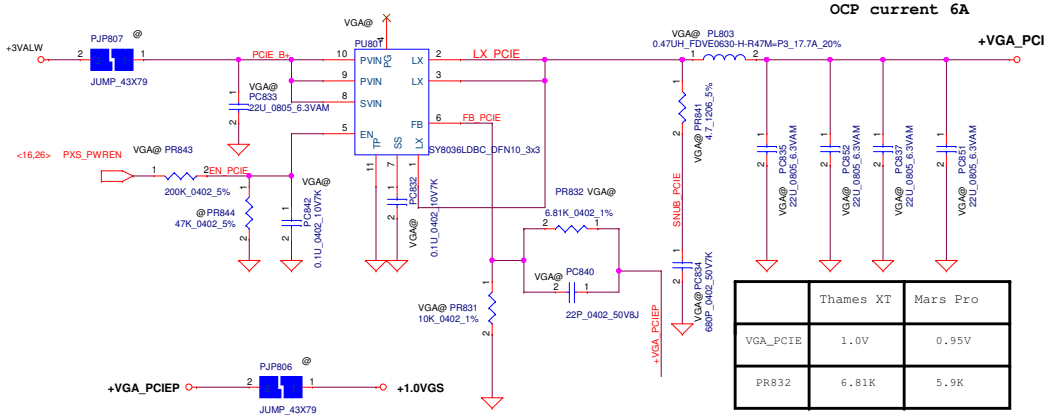


Thames XT

GPU_VID3 (GPIO15)	GPU_VID1 (GPIO20)	Core Voltage Level
1	1	0.8V
1	0	0.85V
0	1	0.9V
0	0	1.0V

+VGA_CORE
TDC 20A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.4mohm +/-5%

+VGA_PCIE
TDC 3.6A
Peak Current 5.2A
OCP current 6A



	Thames XT	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PWR_VGA_CORE/VGA_PCIE

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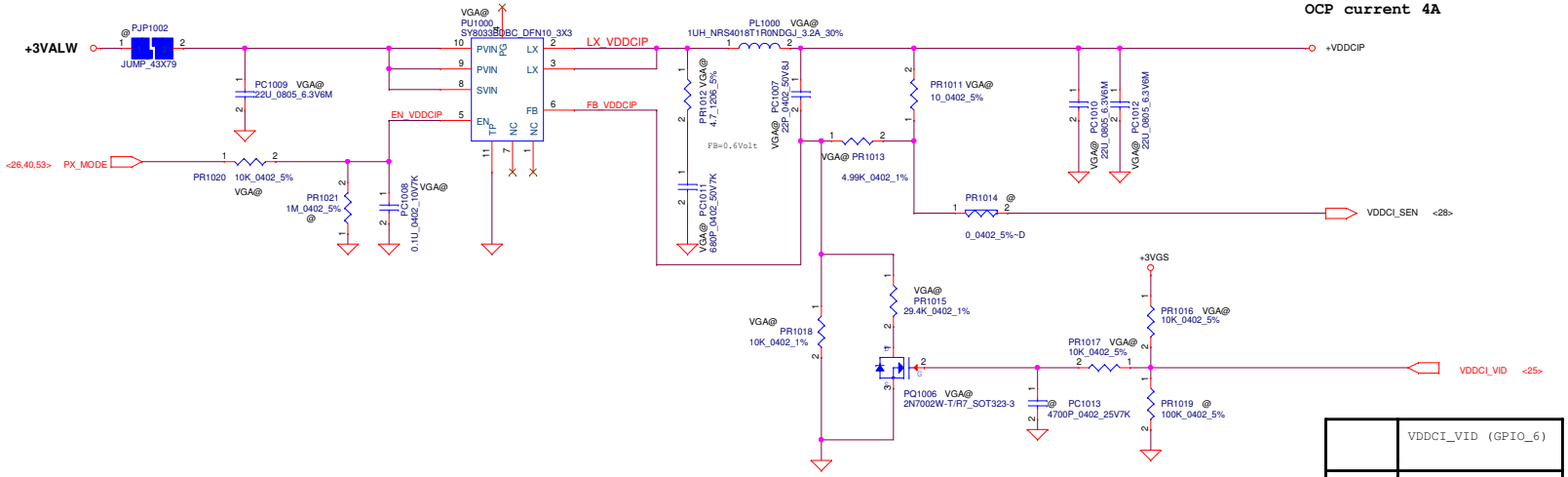
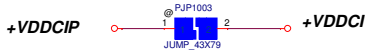
+VDDCI
TDC 2.2A
Peak Current 2.2A
OCP current 4A



	VDDCI_VID (GPIO_6)
High	1V
Low	0.9V



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: PWR_+VDDCIP

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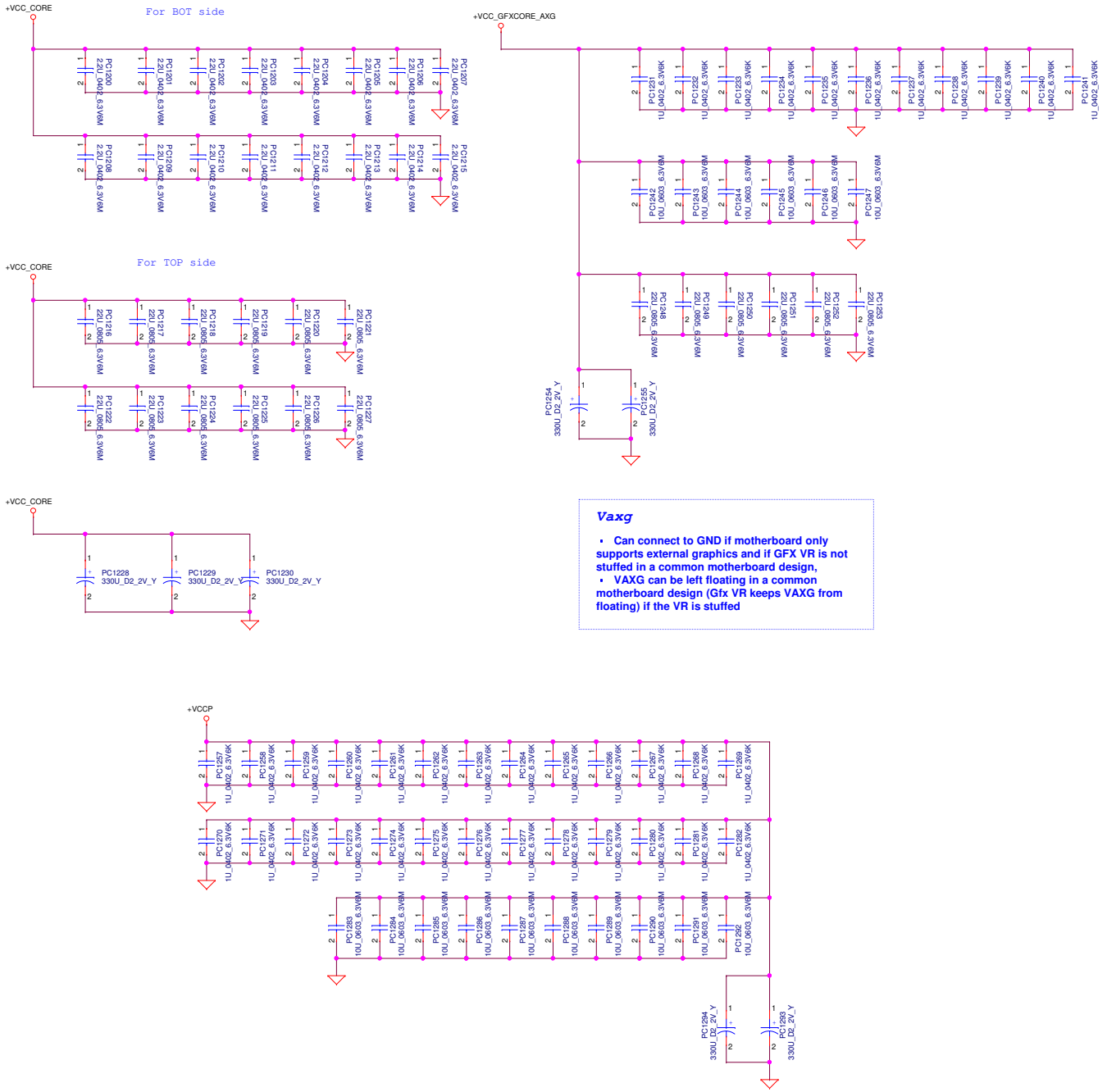

Vaxg

- **Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,**
- **VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed**

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.

Title: **PWR_PROCESSOR DECOUPLING**

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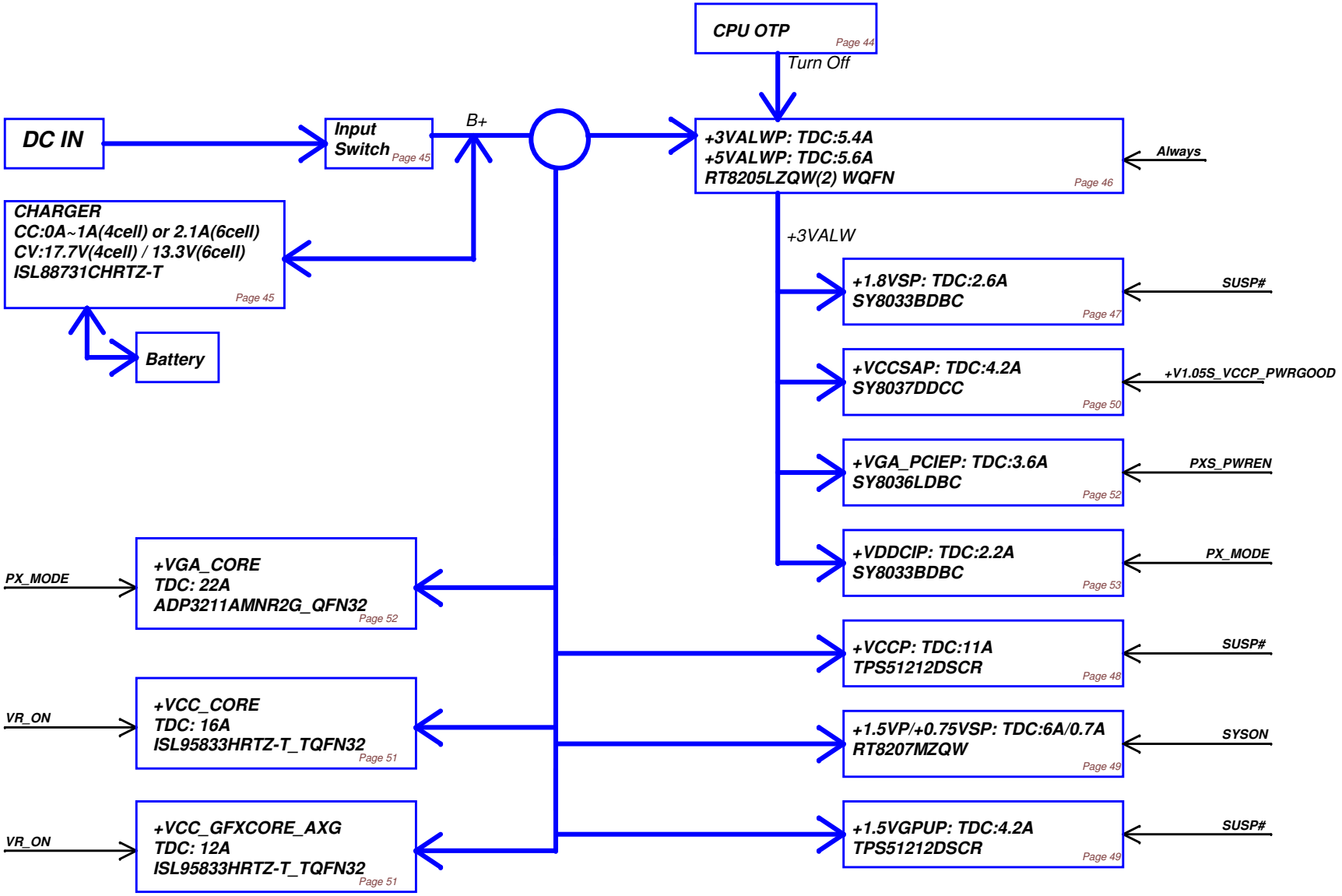
Power block



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

Compal Electronics, Inc.			
Title: PWR_POWER BLOCK DIAGRAM			
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Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	51	VCORE	12/05/11	Morris	adjust VR parameter	change PL700 and PL701 from 0.36u to 0.22u change PC707 and PC740 from 0.047u to 0.033u change PR750 from 649 to 365 change PR711 from 649 to 392 change PR740 from 1.91k to 1.78k change PR705 from 150k to 33.2k	X00
2	44 45 46	DCIN/BATT CONN/OTP CHARGER 3.3VALWP/5VALWP	12/05/11	Morris	follow SSI memo for part shortage issue	change PQ112,PQ114,PQ1111,PQ206,PQ904 from SB00000CQ00 to SB00000PV00	X00
3	49	+1.5VP/1.5VDGPU/0.75VSP	12/05/15	Morris	design change	change PR302 from 12k to 8.66k	X00
4	50	+VCCSAP	12/05/23	Morris	for Pentium and Celeron special BOM	add PR607 and reserve	X00
5	49	+1.5VP/1.5VDGPU/0.75VSP	12/07/06	Morris	design change to reduce low-side mosfet induce	add PC316 1000pf	X01
6	45	CHARGER	12/07/17	Morris	from EMI request	change PR114 from 0 to 2.2 add PR141 and PC121	X01
7	45	CHARGER	12/07/17	Morris	design change to solve Battery LED is still on after unplug AC when SUT in S3S4S5 issue	change PR142 from 210k to 232k for ISL88731C (X76) change PR142 from 309k to 324k for BQ24747 (X76)	X01
8	44	DCIN/BATT CONN/OTP	12/07/17	Morris	revise OTP setting to 96C from thermal request	change PR927 from 12.1k to 11k	X01

Compal Electronics, Inc.		
Title: PWR-PIR		
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