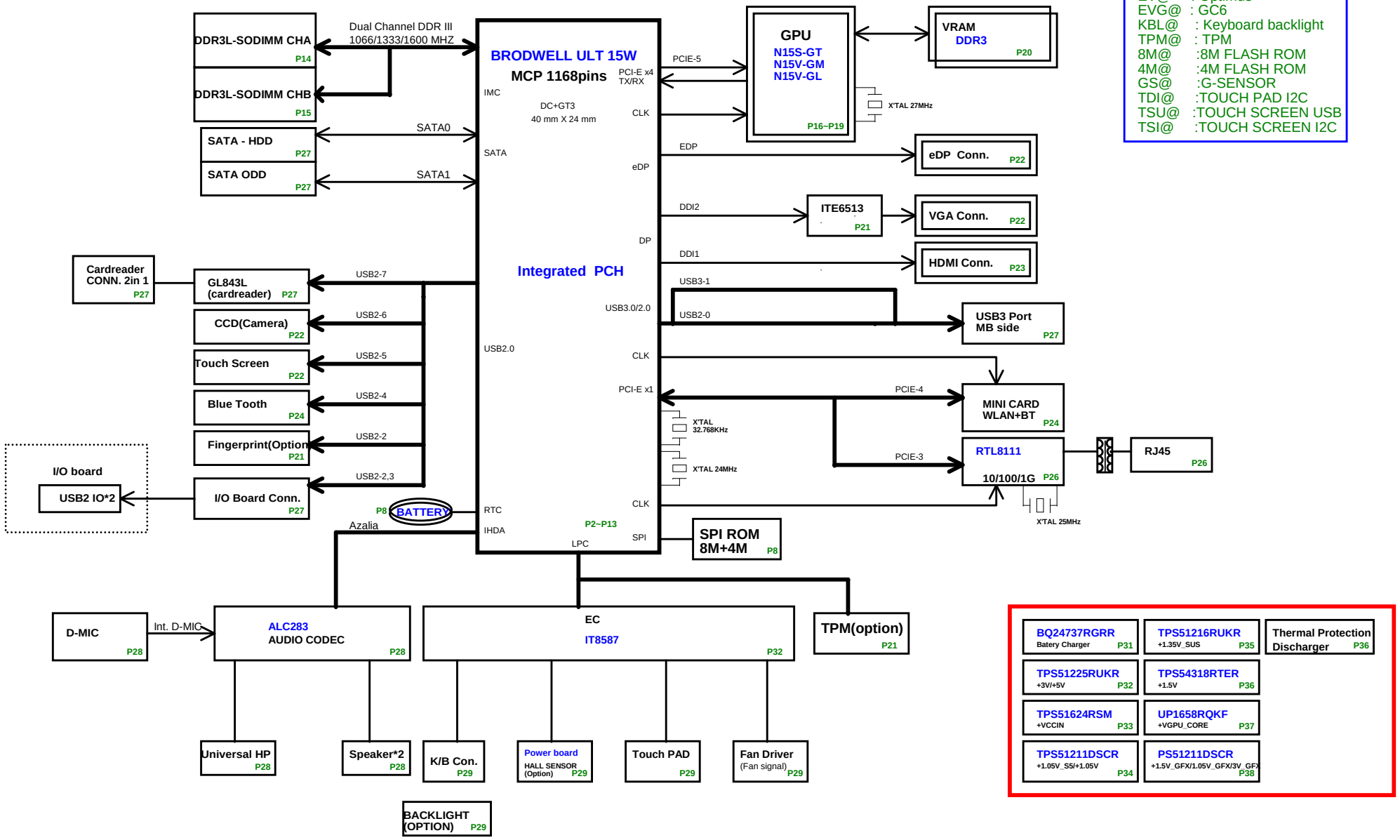
ZQ0_GDDR3 BWD ULT SYSTEM BLOCK DIAGRAM

01

BOM

IV@ : iGPU
EV@ : Optimus
EVG@ : GC6
KBL@ : Keyboard backlight
TPM@ : TPM
8M@ :8M FLASH ROM
4M@ :4M FLASH ROM
GS@ :G-SENSOR
TDI@ :TOUCH PAD I2C
TSU@ :TOUCH SCREEN USB
TSI@ :TOUCH SCREEN I2C



BQ24737RGRR Batery Charger P31	TPS51216RUKR +1.35V_SUS P35	Thermal Protection Discharger P36
TPS51225RUKR +3V/+5V P32	TPS54318RTER +1.5V P36	
TPS51624RSM +VCCIN P33	UP1658RQKF +VGPU_CORE P37	
TPS51211DSCR +1.05V_S5/+1.05V P34	PS51211DSCR +1.5V_GFX/1.05V_GFX/3V_GFX P38	

Quanta Computer Inc.
PROJECT : ZQ0
Block Diagram
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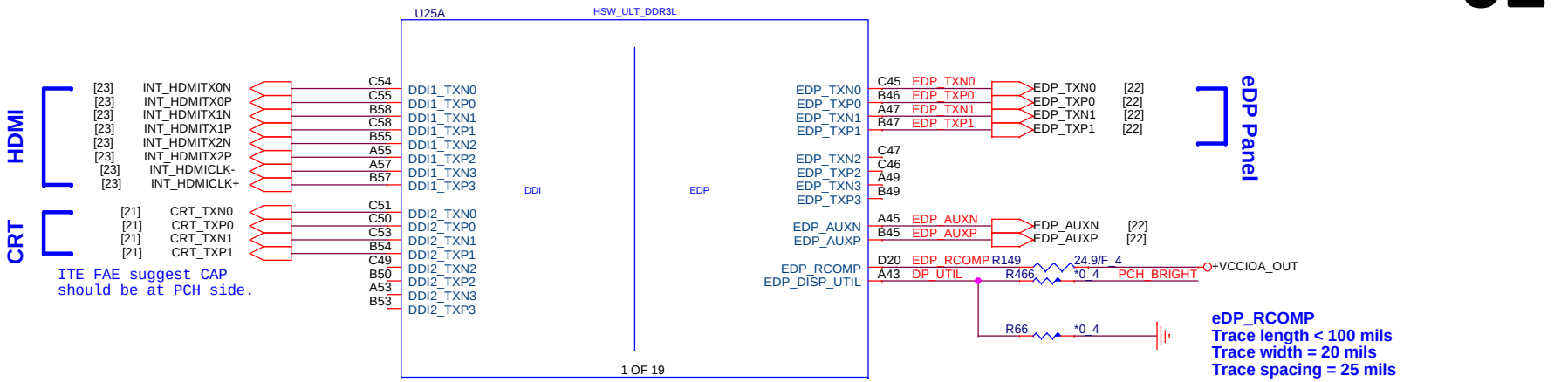
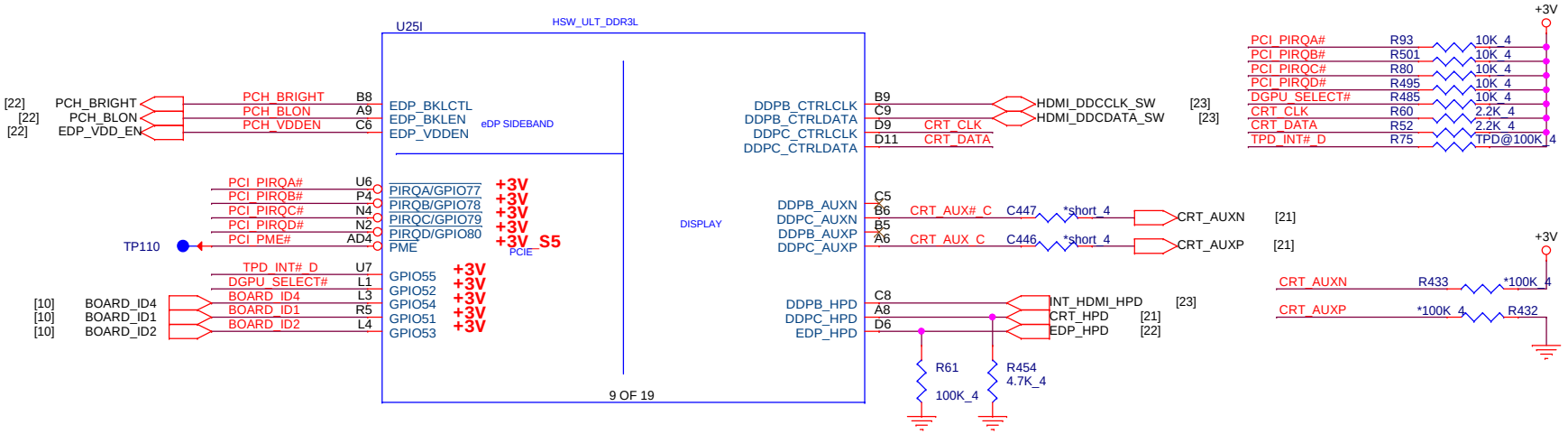
Date: Monday, April 07, 2014 Sheet 1 of 46

Haswell ULT (DISPLAY,eDP)

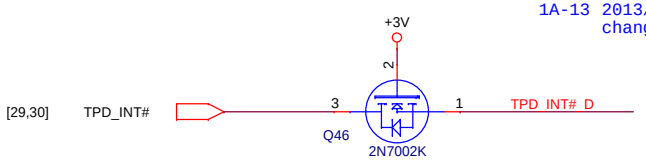
02



eDP_RCOMP
Trace length < 100 mils
Trace width = 20 mils
Trace spacing = 25 mils



1A-13 2013/10/30 move Q42 to page02
change U24.U7 net name.



Quanta Computer Inc.		
PROJECT : ZQ0		
Size	Document Number: Haswell 3/5 (DDI/eDP)	Rev 3A
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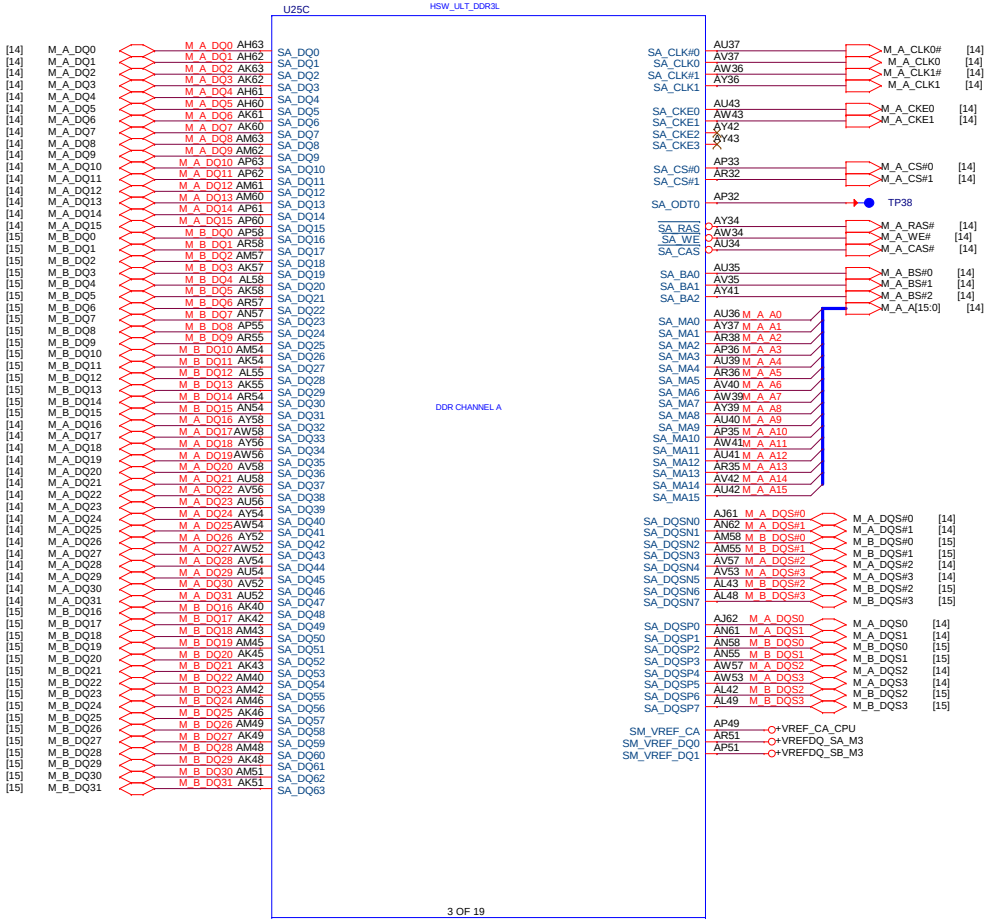
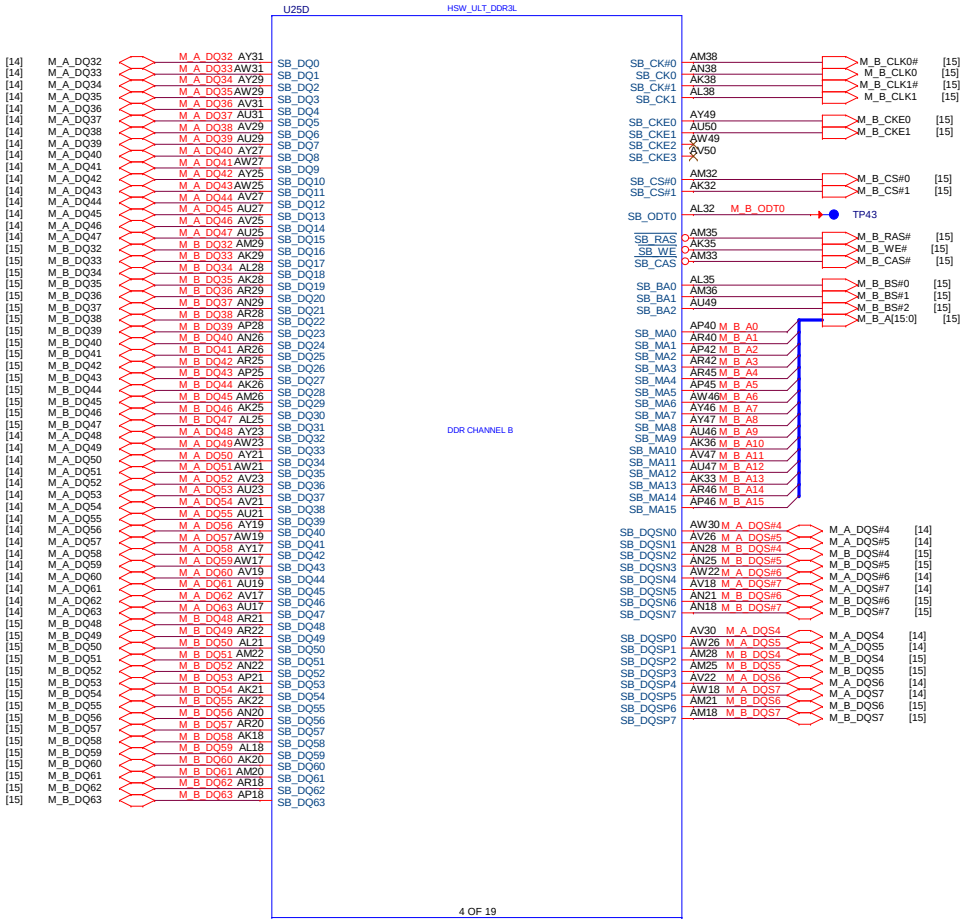
Change Data and DQS to interleave.

Haswell ULT (DDR3L)



Haswell Processor (DDR3)



03

Quanta Computer Inc.		
PROJECT : ZQ0		
Size	Document Number: Haswell 2/5 (DDR3 I/F)	Rev 3A
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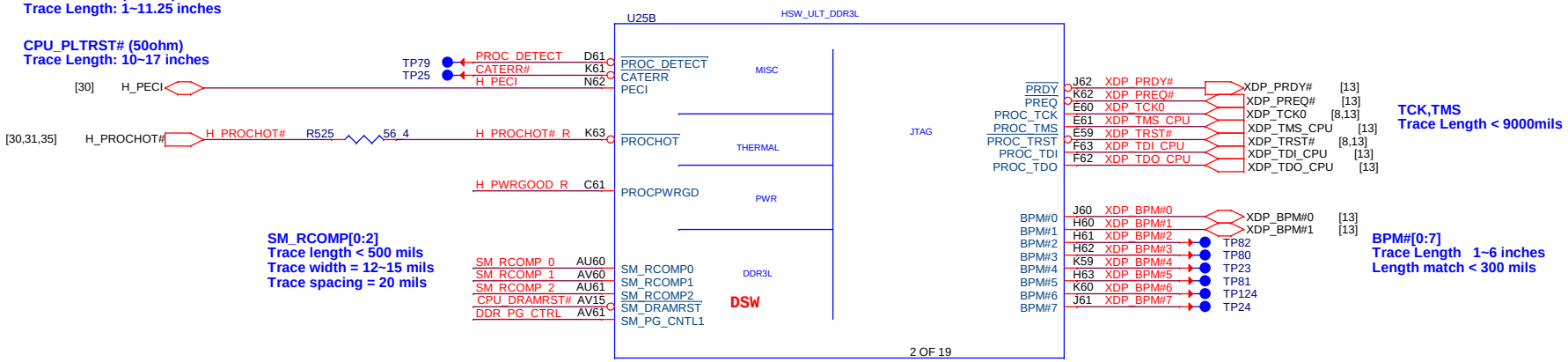
Haswell ULT (SIDEBAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

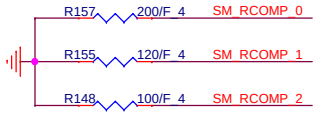


TCK,TMS
Trace Length < 9000mils

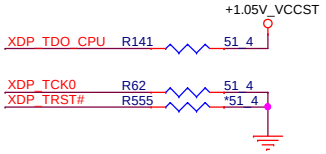
SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

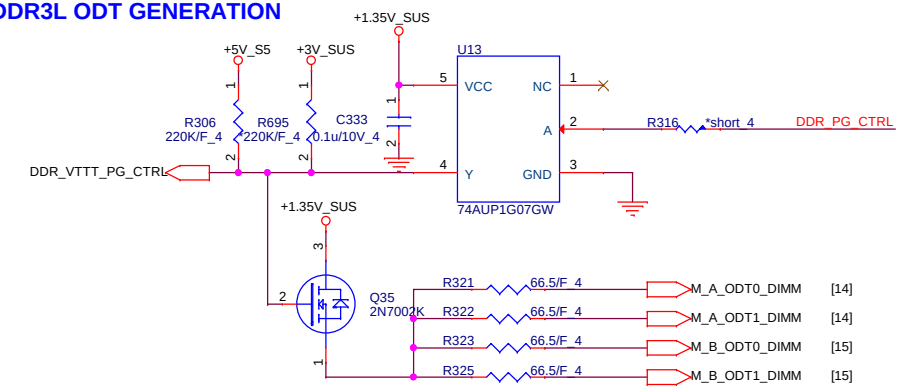
DRAM COMP



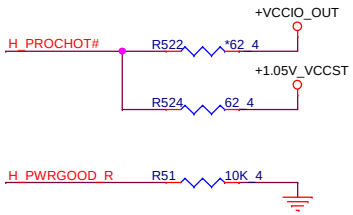
XDP PU/PD



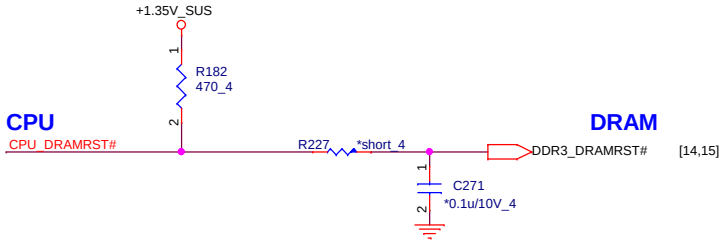
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST



Quanta Computer Inc.
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	Haswell 1/5 (PEG/DMI/FDI)	3A
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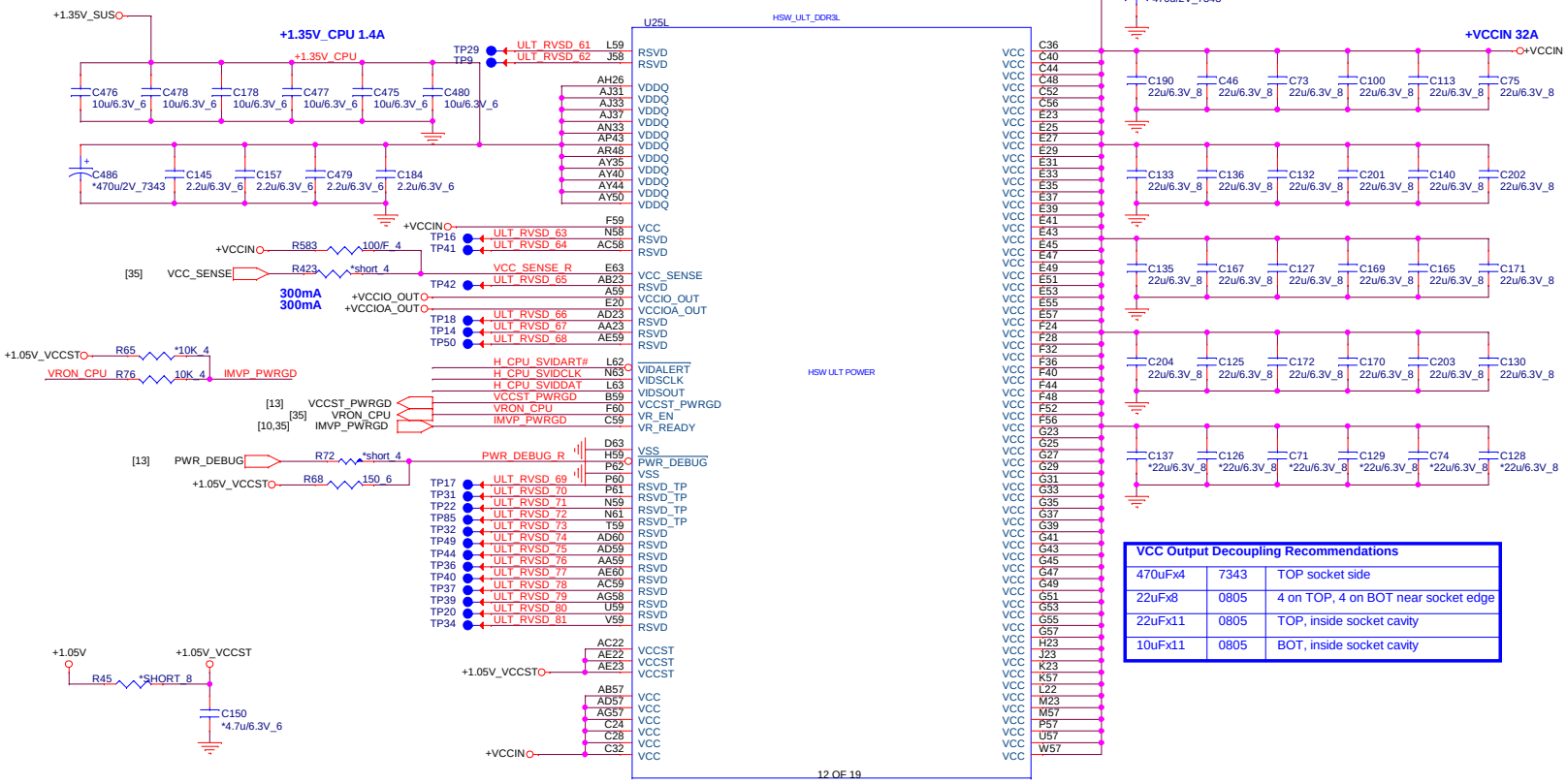
Haswell ULT (POWER)

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

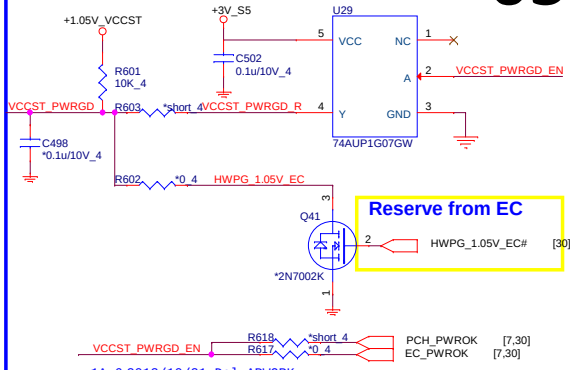


VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

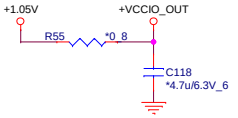
VCCST PWRGD

CRB is via +1.05V PG

05

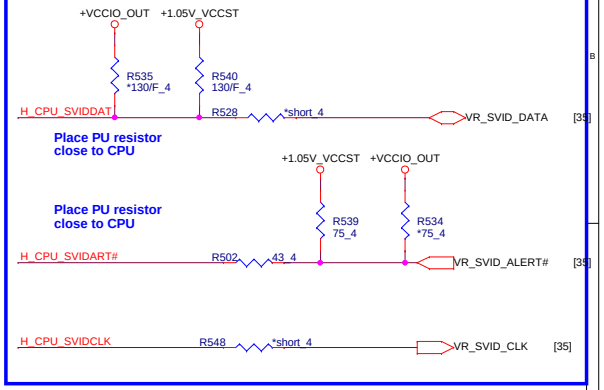


1A-6 2013/10/21 Del APWORK.

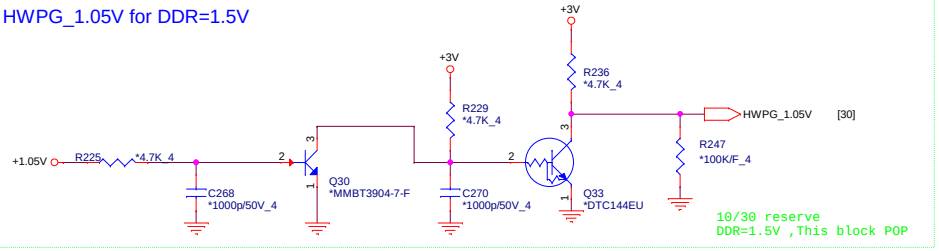


SVID

Layout note: need routing together and ALERT need between CLK and DATA.



HWPG_1.05V for DDR=1.5V



Quanta Computer Inc.		
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Size	Document Number: Haswell 4/5 (POWER)	Rev: 3A
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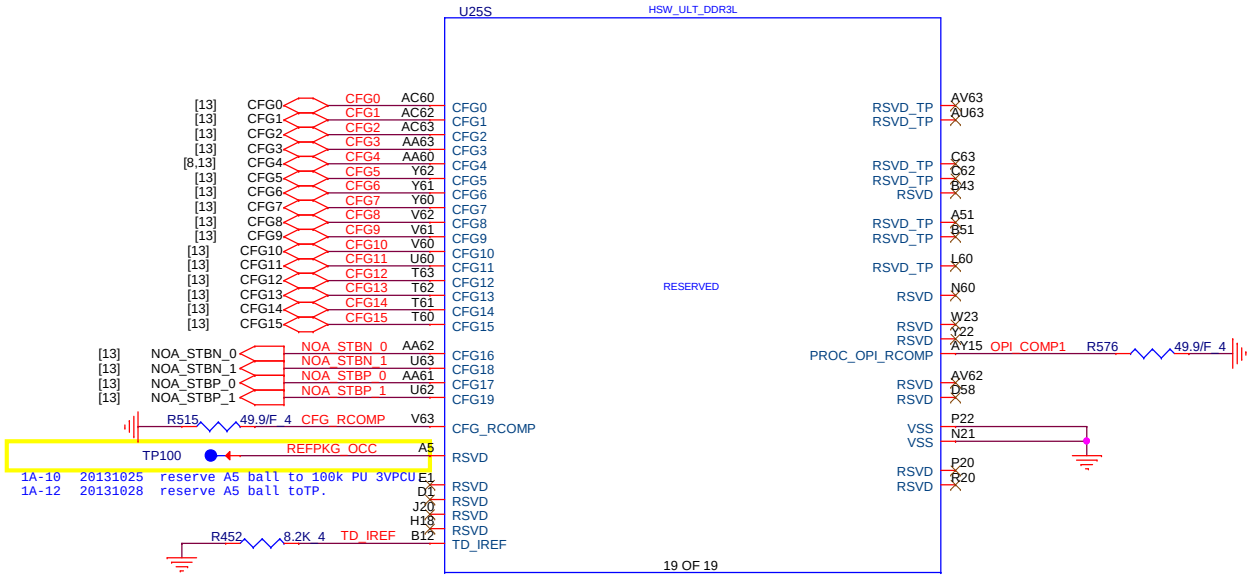
Haswell ULT (CFG,RSVD)

06



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R134 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R552 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R549 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R537 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R532 *1K_4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R126 *1K_4

Quanta Computer Inc.
PROJECT : ZQ0

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	Haswell 5/5 (CFG/GND)	3A

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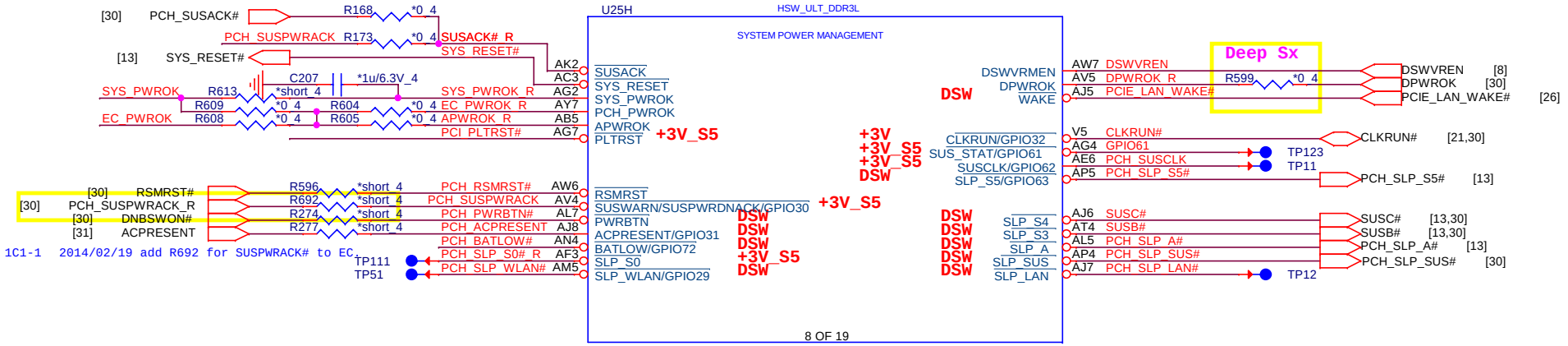
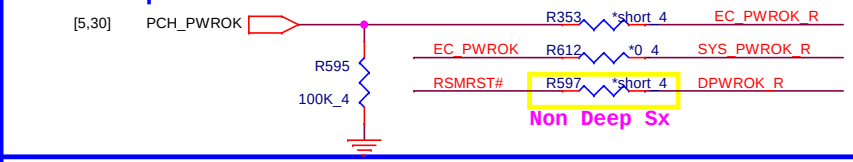
Haswell ULT PCH (PM)

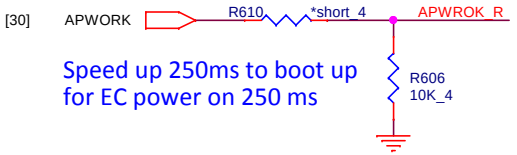
07



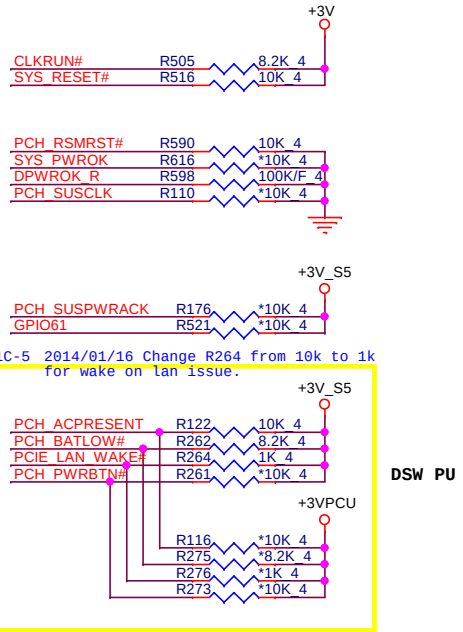
1C1-1 2014/02/19 add R692 for SUSPWRACK# to EC.

Power Sequence

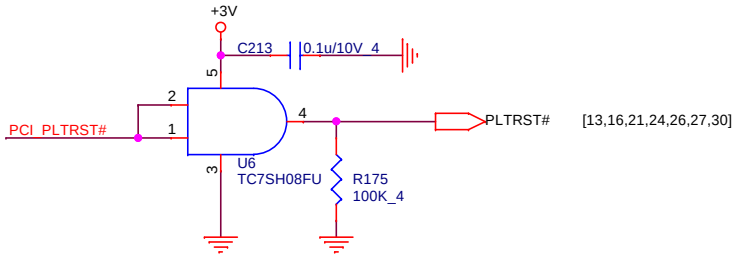




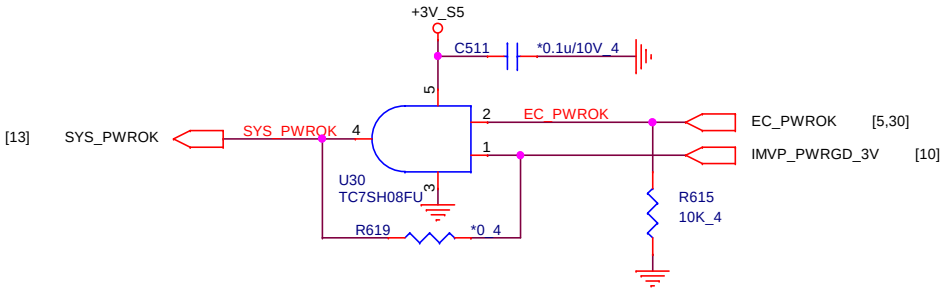
PCH PM PU/PD



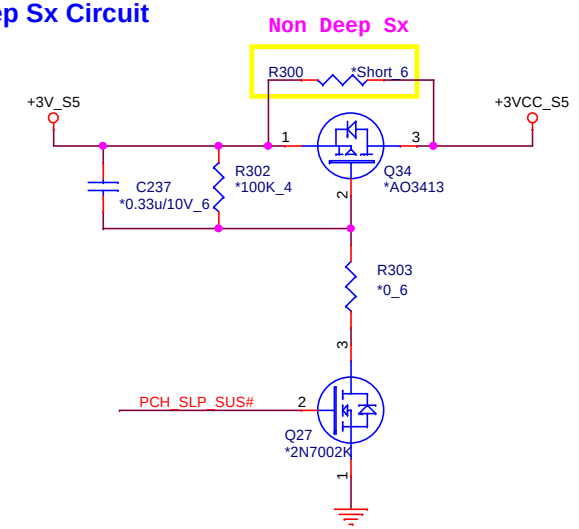
PLTRST# Buffer



SYSPWOK



Deep Sx Circuit



Quanta Computer Inc.		
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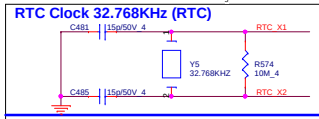
Haswell ULT PCH (RTC/HDA/SATA/SPI)

Haswell ULT PCH(LPC,SPI,SMBUS,C-LINK,THERMAL)

08

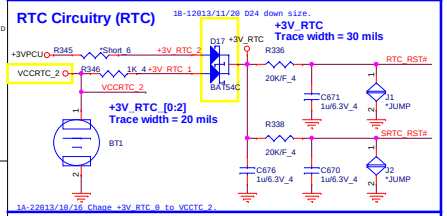
RTC Clock 32.768KHz (RTC)



RTC Circuitry (RTC)

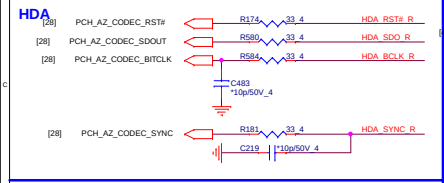
1B-12013/11/20 D24 down size.

+3V_RTC
Trace width = 30 mils



1A-22013/10/16 Change +3V_RTC_0 to VCCTC_2.

HDA

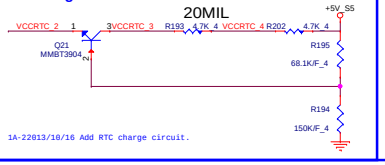


PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

MP remove(Intel)

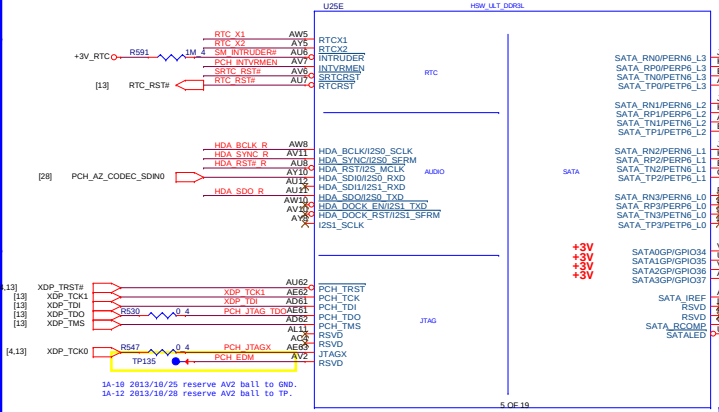
RTC charge circuit

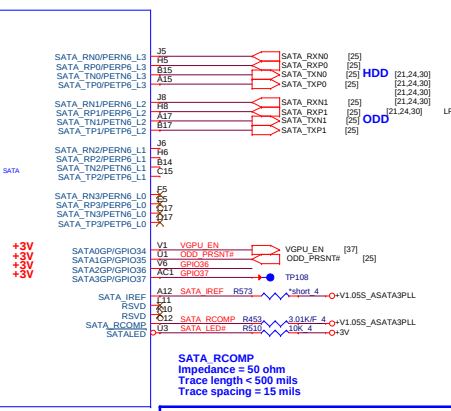


1A-22013/10/16 Add RTC charge circuit.

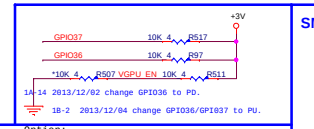
ULT Strapping Table

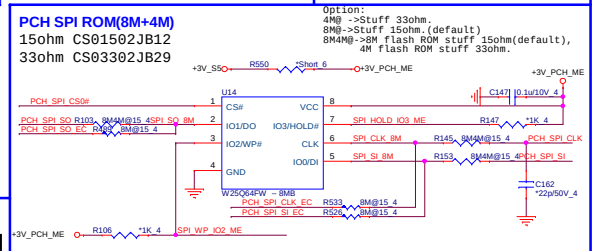
Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (iPD 20K) 1 =Disable No-Reboot mode	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (iPD 20K) 1 =can't program ME	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (iPD 20K) 1 =LPC	
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 =disable	
DSWVREN	Deep Sx well on die VR enable		1=Should be always pull-up	

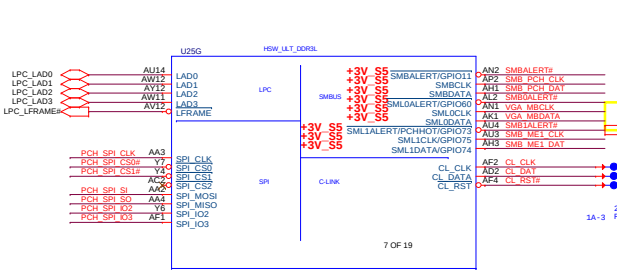




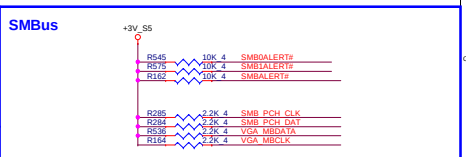
SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils



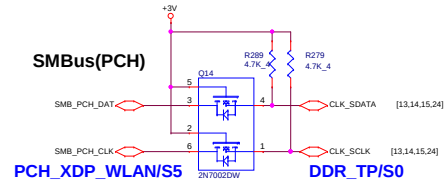




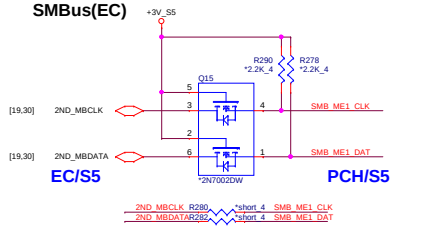
SMBus



SMBus(PCH)



SMBus(EC)



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Haswell ULT PCH (PCIE,USB3.0,USB2.0)

Haswell ULT PCH (CLOCK)

09

1A-6 2013/10/21 reversal PEG lan for layout.
1A-8 2013/10/21 Swap PEG to nomroal mode.

PEG x4

WLAN LAN

U25K HSW_ULT_DDR3L

PCIE

11 OF 19

1A-1 2013/10/15 following up acer define and swap USB3 and USB2 USB2 port.

MB USB3.0
DB USB2.0
DB FingerPrint
DB USB2.0
BT
Touch screen
CCD
Card reader
MB USB3.0

USB

WLAN LAN

VGA

1B-2 2013/11/15 Swap LAN and WLAN Request clk port base on DG.

USBCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

MB U3
DB U2

USB Overcurrent

U25F HSW_ULT_DDR3L

CLOCK SIGNALS

6 OF 19

XTAL24_IN
XTAL24_OUT
C443 12p/50V_4
C442 12p/50V_4
R446 1M_4
Y4 24MHz

CLK_PCI_EC
CLK_PCI_LPC
PCLK_TPM

C221 *18p/50V_4
C226 *18p/50V_4
C222 *TPM@18p/50V_4

Quanta Computer Inc.
PROJECT : ZQ0

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	LPT 3/6 (PCIE/USB/CLK)	3A
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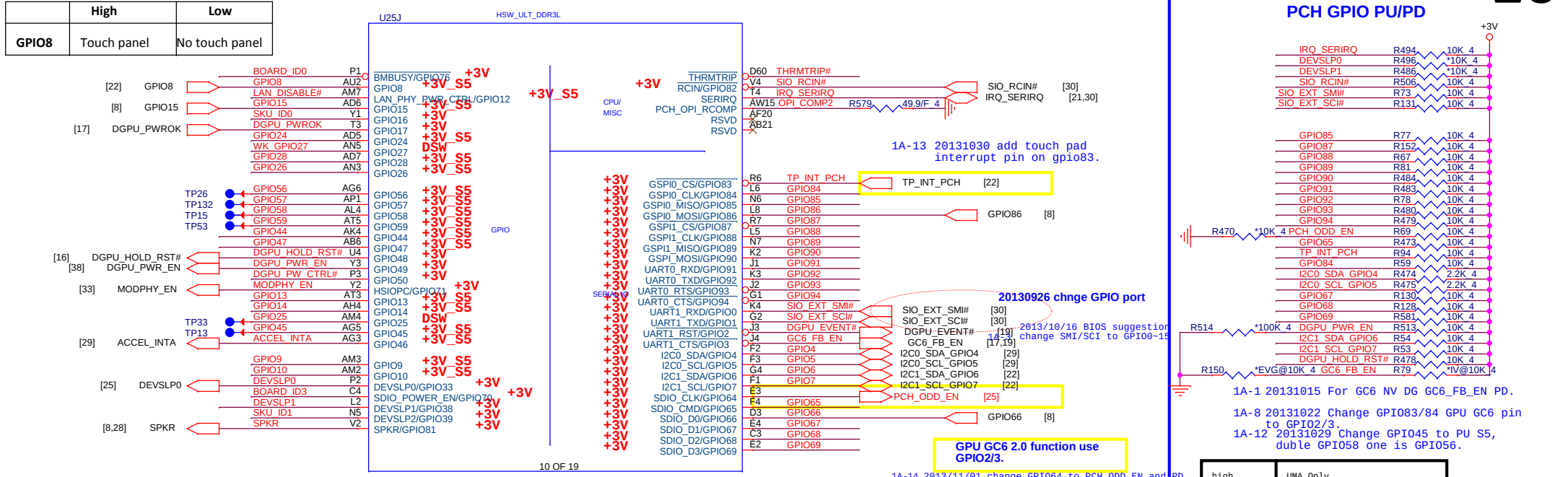
Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

	High	Low
GPIO8	Touch panel	No touch panel



1A-13 20131030 add touch pad interrupt pin on gpio83.

20130926 chnge GPIO port

2013/10/16 BIOS suggestion change SMI/SCI to GPIO0~15

GPU GC6 2.0 function use GPIO2/3.

1A-14 2013/11/01 change GPIO64 to PCH_ODD_EN and PD.

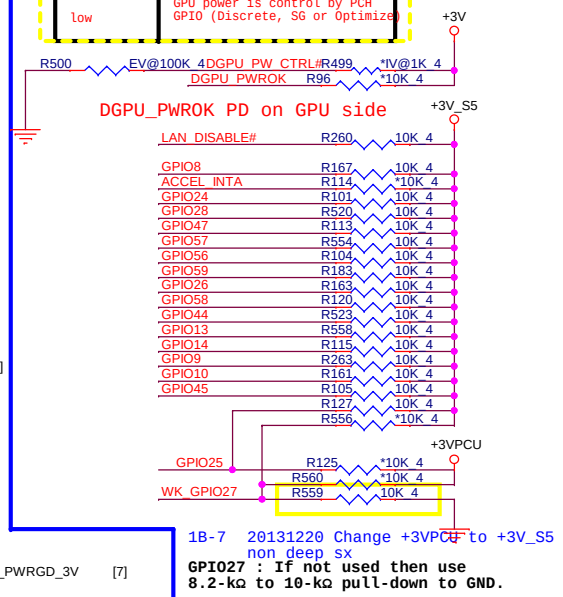
PCH GPIO PU/PD

1A-1 20131015 For GC6 NV DG GC6_FB_EN PD.

1A-8 20131022 Change GPIO83/84 GPU GC6 pin to GPIO2/3.

1A-12 20131029 Change GPIO45 to PU S5, duble GPIO58 one is GPIO56.

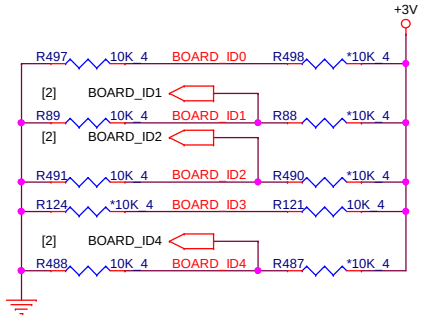
high	UMA Only
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)



1B-7 20131220 Change +3VPCU to +3V_S5 non deep sx

GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

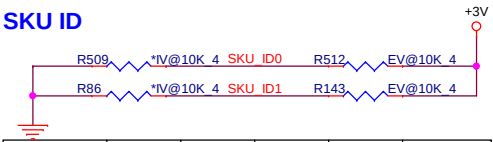
Board ID



	Low	High
BOARD_ID0	N15V-GL-B	N15V-GM-B
BOARD_ID1	Reserved (Default)	Reserve
BOARD_ID2	Reserve for Touch pad, default(low)	
BOARD_ID3	DTPM	No DTPM
BOARD_ID4	Non-Dolly (Default)	Dolly

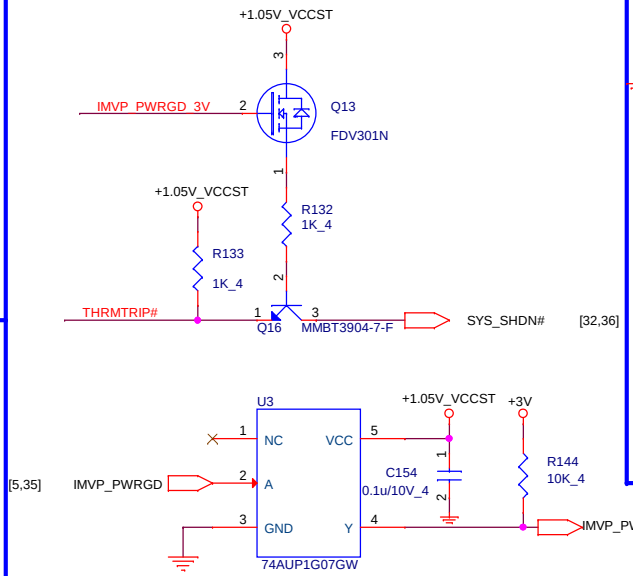
RAM ID

SKU ID



	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

CPU thermal trip



Quanta Computer Inc.
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	LPT 4/6 (GPIO/MISC)	3A
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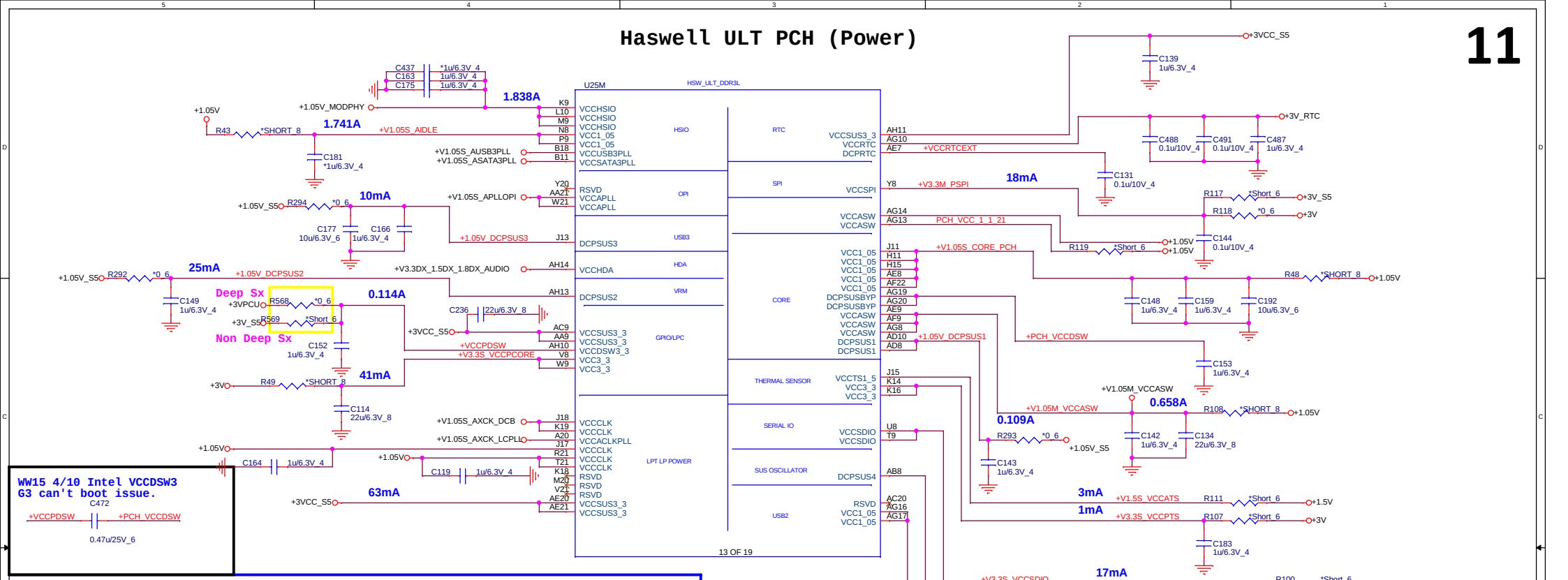
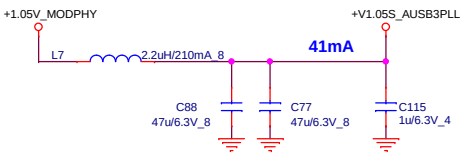
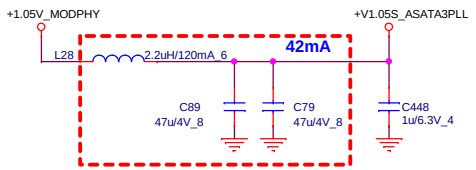
Haswell ULT PCH (Power)



PCH VCCHSIO Power

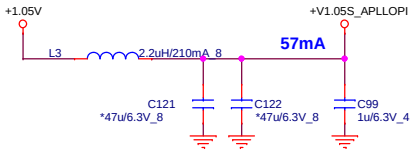
1A-1 2013/10/11 del LDO change to MOS.

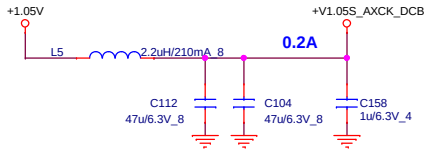




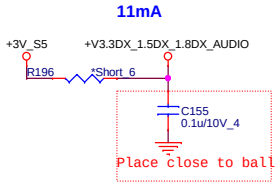
2013/10/31 PN change to H=0.85.L17 H=0.9

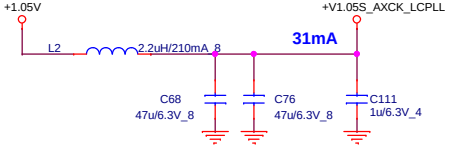
VCCAPLL power





PCH HDA Power





Quanta Computer Inc.
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	LPT 5/6 (POWER)	3A

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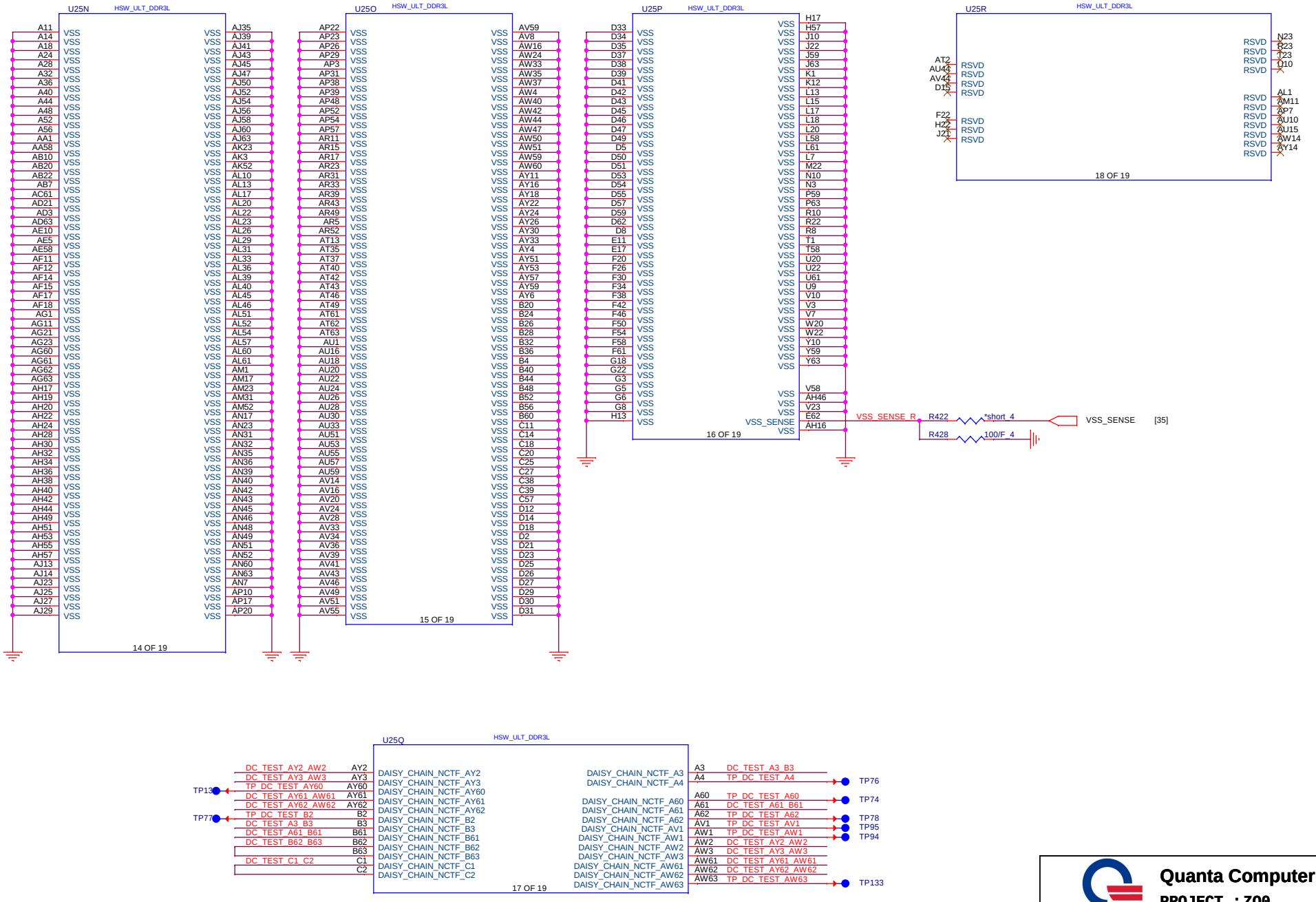
Haswell ULT (GND)



Quanta Computer Inc.

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Size	Document Number	Rev
	LPT 6/6 (GND)	3A

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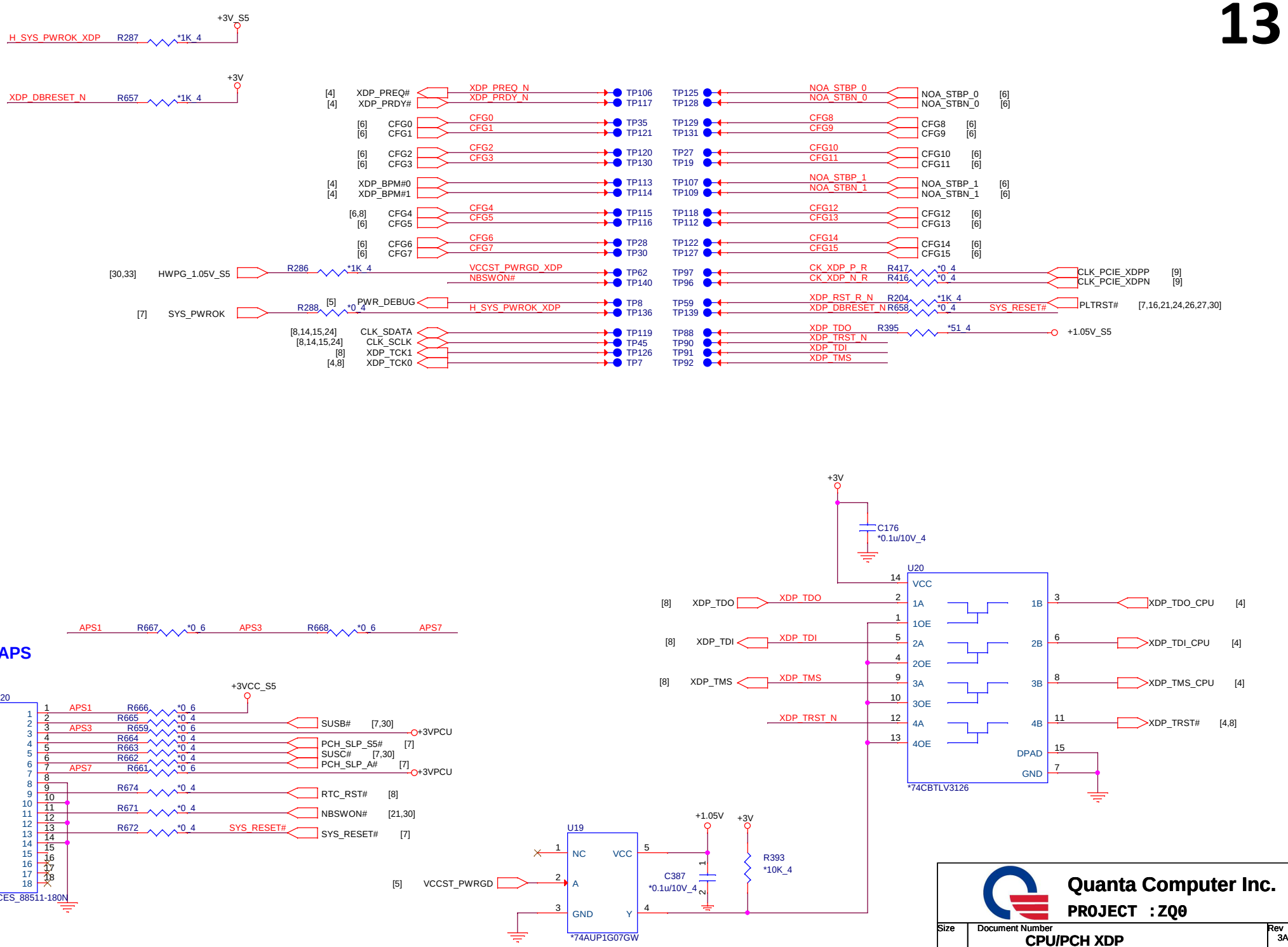

APS

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	CPU/PCH XDP	3A
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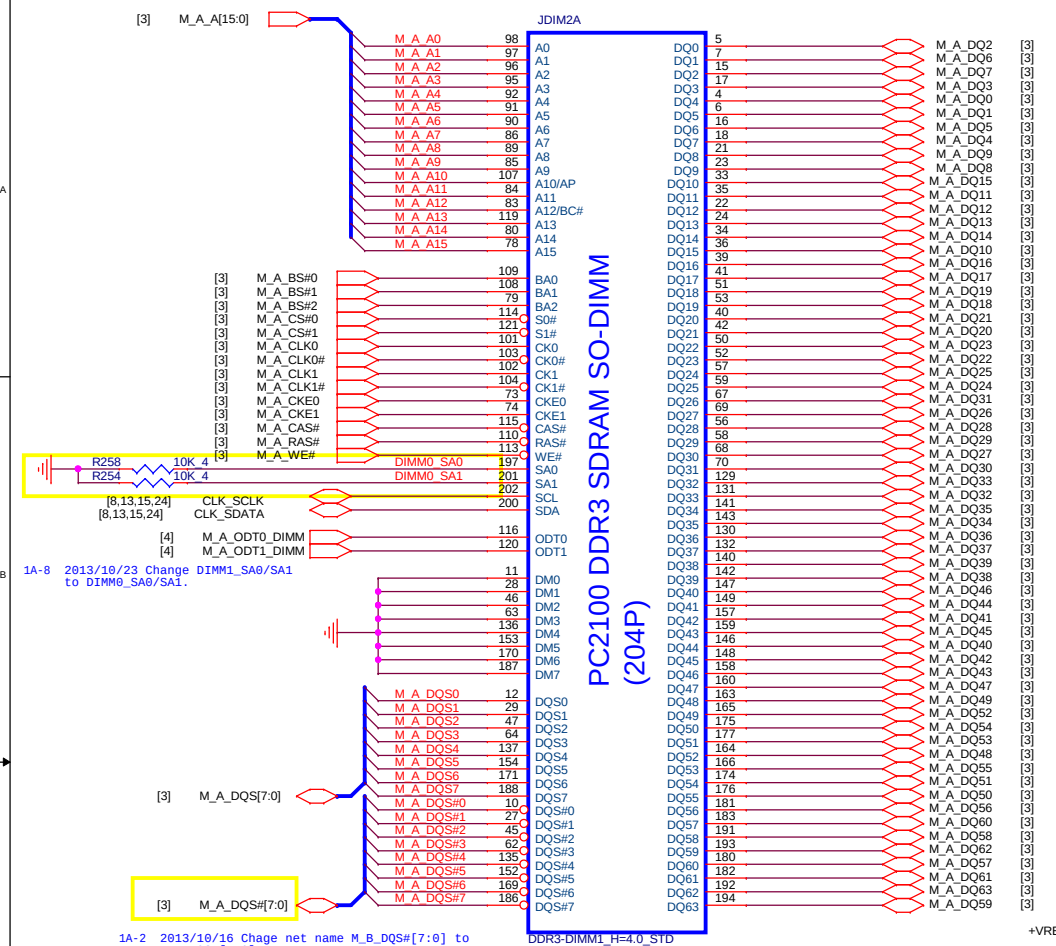
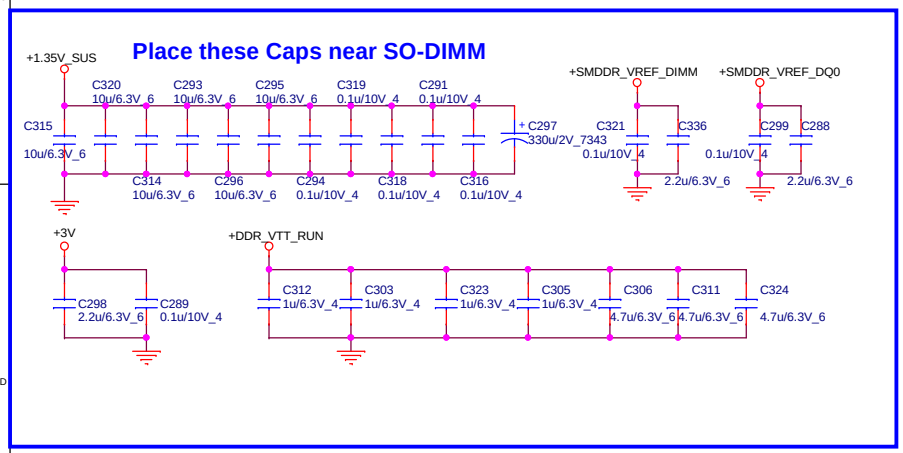
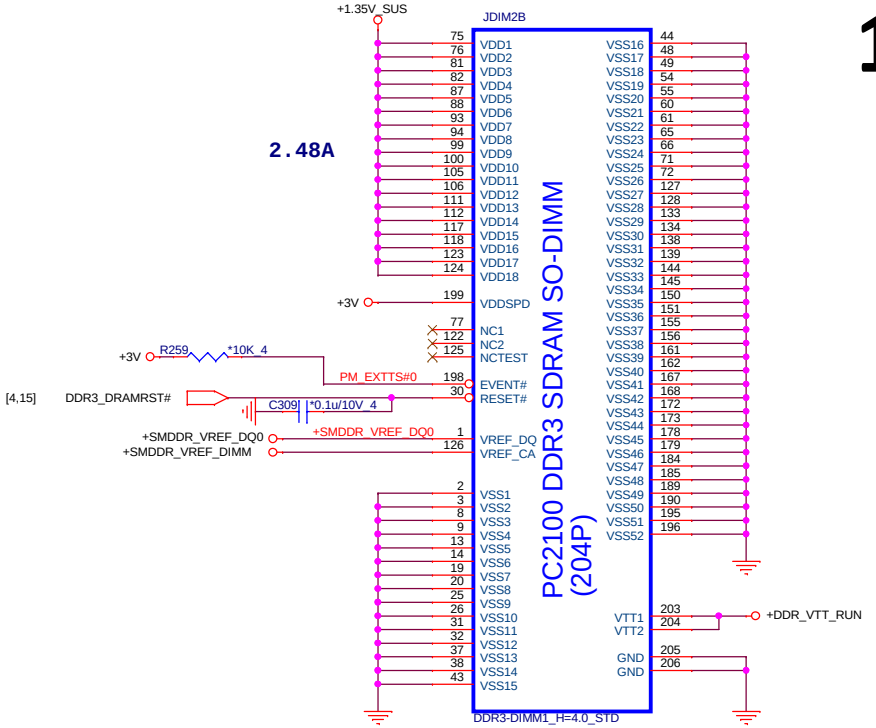
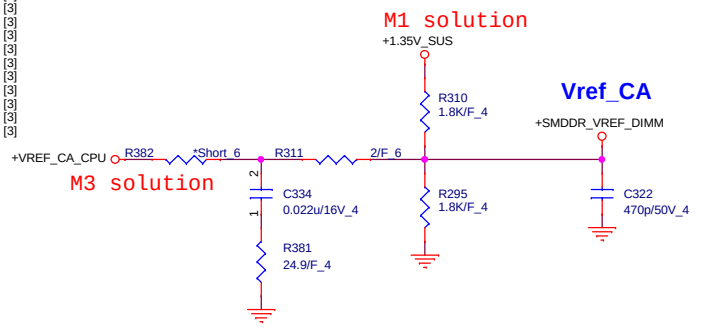


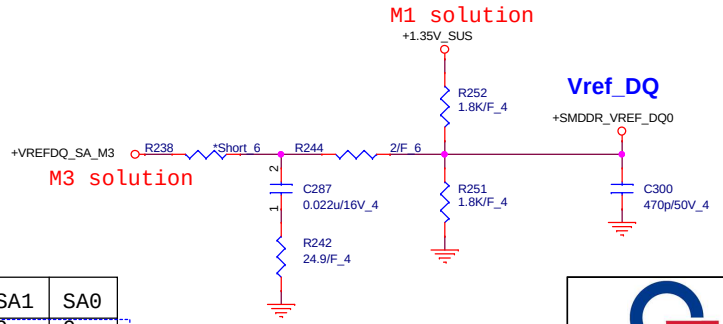
1A-8 2013/10/23 Change DIMM1_SA0/SA1 to DIMM0_SA0/SA1.

1A-2 2013/10/16 Chage net name M_B_DQS#[7:0] to M_A_DQS#[7:0].









	SA1	SA0
CHA	0	0
CHB	1	0

Quanta Computer Inc.

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Size	Document Number	Rev
	DDR3 MEMORY SO-DIMM A	3A

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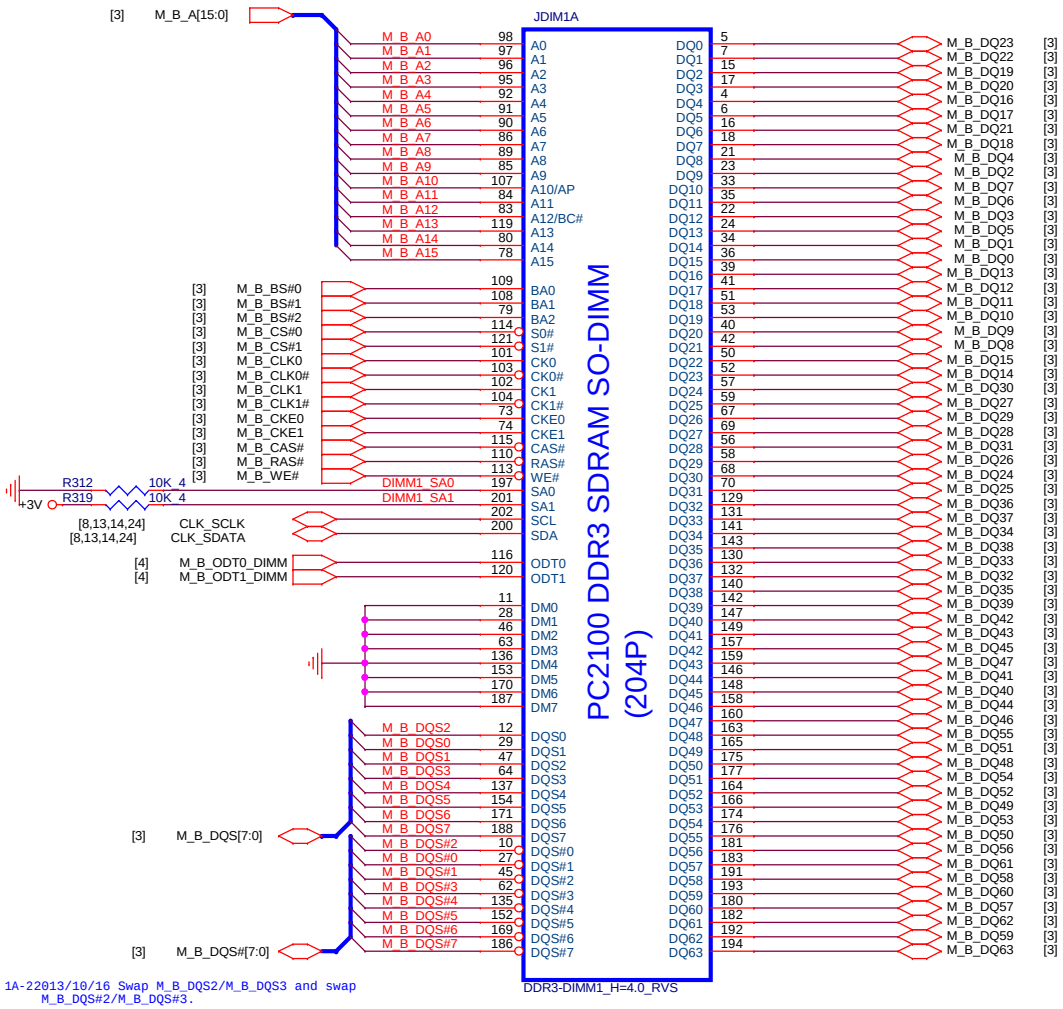
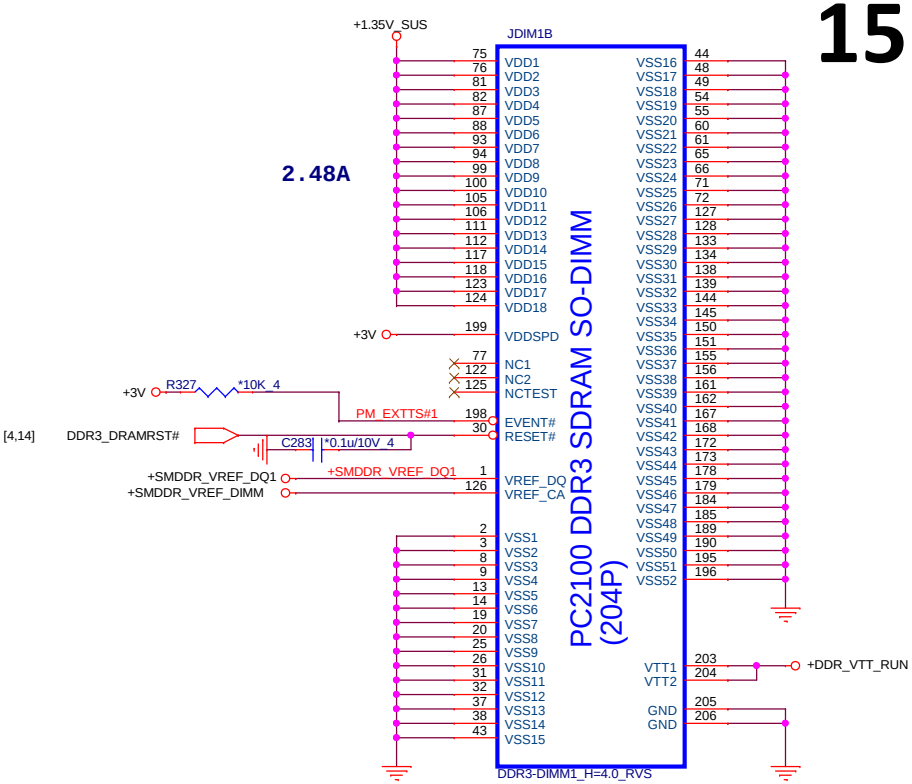
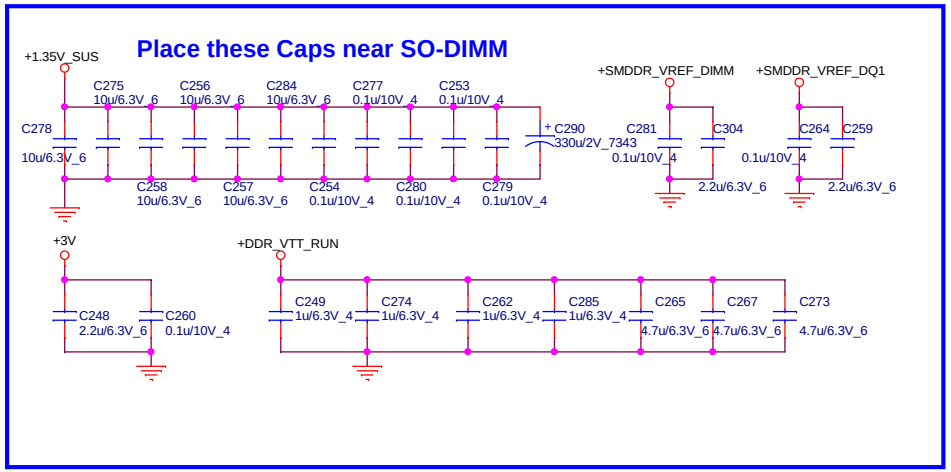
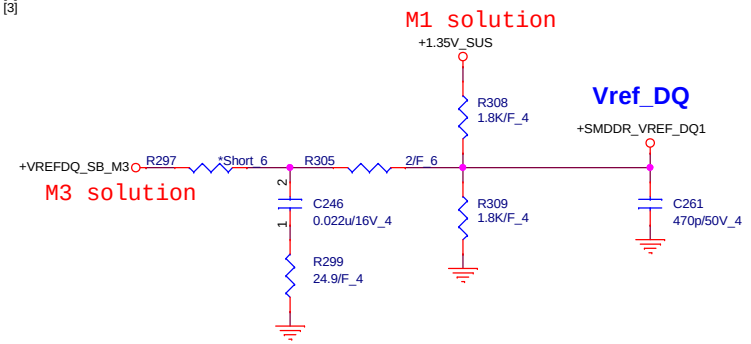


1A-22013/10/16 Swap M_B_DQS2/M_B_DQS3 and swap M_B_DQS#2/M_B_DQS#3.







	SA1	SA0
CHA	0	0
CHB	1	0

Quanta Computer Inc.

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Size	Document Number	Rev
	DDRIII Memory SO-DIMM B	3A
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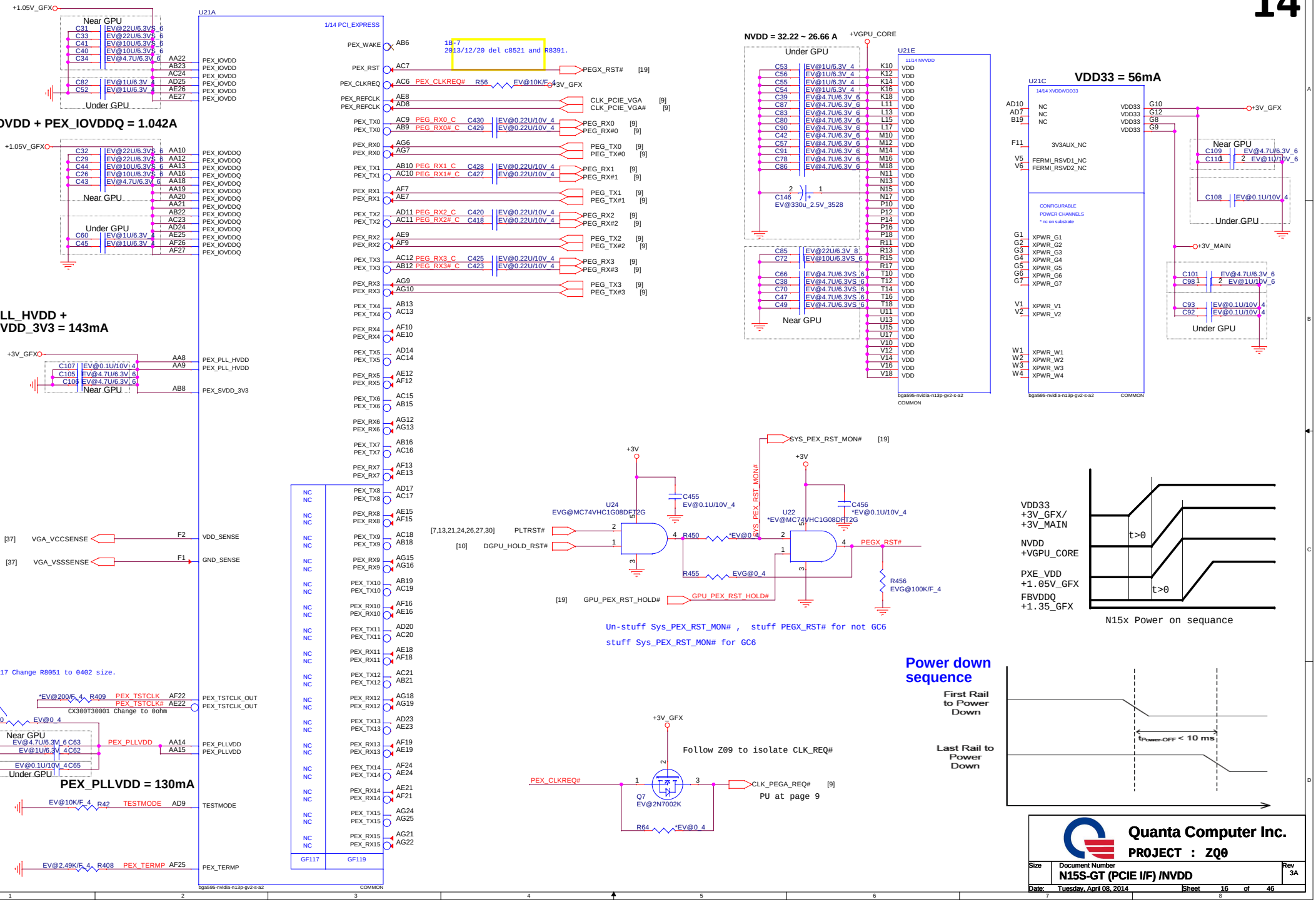
PEX_IOVDD + PEX_IOVDDQ = 1.042A
PEX_PLL_HVDD +
PEX_SVDD_3V3 = 143mA
PEX_PLLVDD = 130mA
8mils width
(0.2MM)
NVDD = 32.22 ~ 26.66 A
VDD33 = 56mA
Power down sequence
First Rail to Power Down
Last Rail to Power Down
Un-stuff Sys_PEX_RST_MON# , stuff PEGX_RST# for not GC6
stuff Sys_PEX_RST_MON# for GC6
Follow Z09 to isolate CLK_REQ#
PU at page 9
VDD33
+3V_GFX/
+3V_MAIN
NVDD
+VGPU_CORE
PXE_VDD
+1.05V_GFX
FBVDDQ
+1.35_GFX
t>0
N15x Power on sequance
Quanta Computer Inc.
PROJECT : ZQ0
N15S-GT (PCIE I/F) /NVDD
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[17,19,30] EC_FB_CLAMP — R459 *EV@0_4 — R444 EV@10K/F_4 — FB_CLAMP F3

For GC6 2.0 and 1.0 stuff EC_FB_CLAMP

PV modify

FBA_ODT_L — FBA_CMD2 — R27 EV@10K/F_4
FBA_ODT_H — FBA_CMD18 — R10 EV@10K/F_4
FBA_RST# — FBA_CMD5 — R23 EV@10K/F_4
FBA_CKE_L — FBA_CMD3 — R28 EV@10K/F_4
FBA_CKE_H — FBA_CMD19 — R11 EV@10K/F_4

U21B

NC	GF119
FB_CLAMP	GF117

2/14 FBA

FBA_D0	E18	VMA_DQ0
FBA_D1	F18	VMA_DQ1
FBA_D2	E16	VMA_DQ2
FBA_D3	F17	VMA_DQ3
FBA_D4	D20	VMA_DQ4
FBA_D5	D21	VMA_DQ5
FBA_D6	F20	VMA_DQ6
FBA_D7	E21	VMA_DQ7
FBA_D8	E15	VMA_DQ8
FBA_D9	D15	VMA_DQ9
FBA_D10	F15	VMA_DQ10
FBA_D11	F13	VMA_DQ11
FBA_D12	C13	VMA_DQ12
FBA_D13	B13	VMA_DQ13
FBA_D14	E13	VMA_DQ14
FBA_D15	D13	VMA_DQ15
FBA_D16	B15	VMA_DQ16
FBA_D17	C16	VMA_DQ17
FBA_D18	A13	VMA_DQ18
FBA_D19	A15	VMA_DQ19
FBA_D20	B18	VMA_DQ20
FBA_D21	A18	VMA_DQ21
FBA_D22	A19	VMA_DQ22
FBA_D23	C19	VMA_DQ23
FBA_D24	B24	VMA_DQ24
FBA_D25	C23	VMA_DQ25
FBA_D26	A25	VMA_DQ26
FBA_D27	A24	VMA_DQ27
FBA_D28	A21	VMA_DQ28
FBA_D29	B21	VMA_DQ29
FBA_D30	C20	VMA_DQ30
FBA_D31	C21	VMA_DQ31
FBA_D32	R22	VMA_DQ32
FBA_D33	R24	VMA_DQ33
FBA_D34	T22	VMA_DQ34
FBA_D35	R23	VMA_DQ35
FBA_D36	N25	VMA_DQ36
FBA_D37	N26	VMA_DQ37
FBA_D38	N23	VMA_DQ38
FBA_D39	N24	VMA_DQ39
FBA_D40	V23	VMA_DQ40
FBA_D41	V22	VMA_DQ41
FBA_D42	T23	VMA_DQ42
FBA_D43	U22	VMA_DQ43
FBA_D44	Y24	VMA_DQ44
FBA_D45	AA24	VMA_DQ45
FBA_D46	Y22	VMA_DQ46
FBA_D47	AA23	VMA_DQ47
FBA_D48	AD27	VMA_DQ48
FBA_D49	AB25	VMA_DQ49
FBA_D50	AD26	VMA_DQ50
FBA_D51	AC25	VMA_DQ51
FBA_D52	AA27	VMA_DQ52
FBA_D53	AA26	VMA_DQ53
FBA_D54	W26	VMA_DQ54
FBA_D55	Y25	VMA_DQ55
FBA_D56	R26	VMA_DQ56
FBA_D57	T25	VMA_DQ57
FBA_D58	N27	VMA_DQ58
FBA_D59	R27	VMA_DQ59
FBA_D60	V26	VMA_DQ60
FBA_D61	V27	VMA_DQ61
FBA_D62	W27	VMA_DQ62
FBA_D63	W25	VMA_DQ63

TP93 — FBA_CMD1 — [20] FBA_CMD0 — C27 — FBA_CMD0
[20] FBA_CMD2 — C26 — FBA_CMD1
[20] FBA_CMD3 — E24 — FBA_CMD2
[20] FBA_CMD4 — F24 — FBA_CMD3
[20] FBA_CMD5 — D27 — FBA_CMD4
[20] FBA_CMD6 — D26 — FBA_CMD5
[20] FBA_CMD7 — F25 — FBA_CMD6
[20] FBA_CMD8 — F26 — FBA_CMD7
[20] FBA_CMD9 — F23 — FBA_CMD8
[20] FBA_CMD10 — G22 — FBA_CMD9
[20] FBA_CMD11 — G23 — FBA_CMD10
[20] FBA_CMD12 — G24 — FBA_CMD11
[20] FBA_CMD13 — F27 — FBA_CMD12
[20] FBA_CMD14 — G25 — FBA_CMD13
[20] FBA_CMD15 — G27 — FBA_CMD14
[20] FBA_CMD16 — G26 — FBA_CMD15
TP2 — FBA_CMD17 — M24 — FBA_CMD16
[20] FBA_CMD18 — M23 — FBA_CMD17
[20] FBA_CMD19 — K24 — FBA_CMD18
[20] FBA_CMD20 — K23 — FBA_CMD19
[20] FBA_CMD21 — M27 — FBA_CMD20
[20] FBA_CMD22 — M26 — FBA_CMD21
[20] FBA_CMD23 — M25 — FBA_CMD22
[20] FBA_CMD24 — K26 — FBA_CMD23
[20] FBA_CMD25 — K22 — FBA_CMD24
[20] FBA_CMD26 — J23 — FBA_CMD25
[20] FBA_CMD27 — J25 — FBA_CMD26
[20] FBA_CMD28 — J24 — FBA_CMD27
[20] FBA_CMD29 — K27 — FBA_CMD28
[20] FBA_CMD30 — K25 — FBA_CMD29
TP1 — FBA_CMD31 — J27 — FBA_CMD30
J26 — FBA_CMD31

+1.35V_GFX — R33 *EV@60.4_4 — F22 — FBA_DEBUG0
R39 *EV@60.4_4 — D22 — FBA_DEBUG1

[20] VMA_CLK0 — D24 — FBA_CLK0
[20] VMA_CLK0# — D25 — FBA_CLK0
[20] VMA_CLK1 — N22 — FBA_CLK1
[20] VMA_CLK1# — M22 — FBA_CLK1

D18 FBA_WCK01
C18 FBA_WCK01
D17 FBA_WCK23
D16 FBA_WCK23
T24 FBA_WCK45
U24 FBA_WCK45
V24 FBA_WCK67
V25 FBA_WCK67

FB_PLLAVDD = 55mA

+1.05V_GFX — L1 EV@BLM15PX331SN1D — +FB_PLLAVDD — F16 — FB_PLLAVDD
P22 FB_PLLAVDD
H22 FB_PLLAVDD

C59 EV@22U/6.3VS_6
C67 EV@0.1U/10V_4
C81 EV@0.1U/10V_4
C84 EV@0.1U/10V_4

FB_DLLAVDD	GF119
FB_PLLAVDD	GF117

FB_DLLAVDD = 15mA

INT

bga595-nvidia-n13p-gv2-s-a2 COMMON

FB_VREF_PROBE — D23

FBA_DQM0 D19 VMA_DM0
FBA_DQM1 D14 VMA_DM1
FBA_DQM2 C17 VMA_DM2
FBA_DQM3 C22 VMA_DM3
FBA_DQM4 P24 VMA_DM4
FBA_DQM5 W24 VMA_DM5
FBA_DQM6 AA25 VMA_DM6
FBA_DQM7 U25 VMA_DM7
VMA_DM[7:0] [20]

FBA_DQS_WP0 E19 VMA_WDQS0
FBA_DQS_WP1 C15 VMA_WDQS1
FBA_DQS_WP2 B16 VMA_WDQS2
FBA_DQS_WP3 B22 VMA_WDQS3
FBA_DQS_WP4 R25 VMA_WDQS4
FBA_DQS_WP5 W23 VMA_WDQS5
FBA_DQS_WP6 AB26 VMA_WDQS6
FBA_DQS_WP7 T26 VMA_WDQS7
VMA_WDQS[7:0] [20]

FBA_DQS_RN0 F19 VMA_RDQS0
FBA_DQS_RN1 C14 VMA_RDQS1
FBA_DQS_RN2 A16 VMA_RDQS2
FBA_DQS_RN3 A22 VMA_RDQS3
FBA_DQS_RN4 P25 VMA_RDQS4
FBA_DQS_RN5 W22 VMA_RDQS5
FBA_DQS_RN6 AB27 VMA_RDQS6
FBA_DQS_RN7 T27 VMA_RDQS7
VMA_RDQS[7:0] [20]

VMA_DQ[63:0] — VMA_DQ[63:0] [20]

FBVDDQ + FBVDD = 3.116A

+1.35V_GFX

C4 EV@0.1U/10V_4
C2 EV@0.1U/10V_4
C301 EV@0.1U/10V_6
C394 EV@0.1U/10V_6
C12 EV@4.7U/6.3V_6
C426 EV@10U/6.3V_6
C395 EV@22U/6.3V5_6
C424 EV@4.7U/6.3V_6

U21D

B26	FBVDDQ
C25	FBVDDQ
E23	FBVDDQ
E26	FBVDDQ
F14	FBVDDQ
F21	FBVDDQ
G13	FBVDDQ
G14	FBVDDQ
G15	FBVDDQ
G16	FBVDDQ
G18	FBVDDQ
G19	FBVDDQ
G20	FBVDDQ
G21	FBVDDQ
H24	FBVDDQ
H26	FBVDDQ
J21	FBVDDQ
K21	FBVDDQ
L22	FBVDDQ
L24	FBVDDQ
L26	FBVDDQ
M21	FBVDDQ
N21	FBVDDQ
R21	FBVDDQ
T21	FBVDDQ
V21	FBVDDQ
W21	FBVDDQ

12/14 FBVDDQ

bga595-nvidia-n13p-gv2-s-a2 COMMON

FB_CAL_PD_VDDQ — D22 FB_CAL_PD_VDDQ — R38 EV@40.2/F_4 — +1.35V_GFX
FB_CAL_PU_GND — C24 FB_CAL_PU_GND — R35 EV@42.2/F_4
FB_CALTERM_GND — B25 FB_CAL_TERM_GND — R36 EV@51.1/F_4

U21F

13/14 GND

A2	GND	GND	M13
AB17	GND	GND	M15
AB20	GND	GND	M17
AB24	GND	GND	N10
AC2	GND	GND	N12
AC22	GND	GND	N14
AC26	GND	GND	N16
AC5	GND	GND	N18
AC8	GND	GND	P11
AD12	GND	GND	P13
AD13	GND	GND	P15
A26	GND	GND	P17
AD15	GND	GND	P2
AD16	GND	GND	P23
AD18	GND	GND	P26
AD19	GND	GND	P5
AD21	GND	GND	R10
AD22	GND	GND	R12
AE11	GND	GND	R14
AE14	GND	GND	R16
AE17	GND	GND	R18
AE20	GND	GND	T11
AB11	GND	GND	T13
AF1	GND	GND	T15
AF11	GND	GND	T17
AF14	GND	GND	U10
AF17	GND	GND	U12
AF20	GND	GND	U14
AF23	GND	GND	U16
AF5	GND	GND	U18
AF8	GND	GND	U2
AG2	GND	GND	U23
AG26	GND	GND	U26
AB14	GND	GND	U5
B1	GND	GND	V11
B11	GND	GND	V13
B14	GND	GND	V15
B17	GND	GND	V17
B20	GND	GND	Y2
B23	GND	GND	Y23
B27	GND	GND	Y26
B5	GND	GND	Y5
B8	GND	GND	
E11	GND	GND	
E14	GND	GND	
E17	GND	GND	
E2	GND	GND	
E20	GND	GND	
E22	GND	GND	
E25	GND	GND	
E5	GND	GND	
E8	GND	GND	
H2	GND	GND	
H23	GND	GND	
H25	GND	GND	
H5	GND	GND	
K11	GND	GND	
K13	GND	GND	
K15	GND	GND	
K17	GND	GND	
L10	GND	GND	
L12	GND	GND	
L14	GND	GND	
L16	GND	GND	
L18	GND	GND	
L2	GND	GND	
L23	GND	GND	
L25	GND	GND	
L5	GND	GND	AA7
M11	GND	GND	AB7

bga595-nvidia-n13p-gv2-s-a2 COMMON

[38] HWPG_1.5VGFX — R58 EV@4.7K_4 — DGPU_POK-1 — Q8 EV@METR3904-G — C120 *EV@1000P/50V_4

+3V_GFX — R70 EV@4.7K_4 — DGPU_PWROK [10]
+3V — R74 EV@4.7K_4 — Q9 EV@DTC144EUA — R71 EV@100K/F_4 — C123 EV@1000P/50V_4

*EV@0.1u/10V_4 C454
C453 EV@0.1U/10V_4

GPU_PWR_GD ,PD at GPU power side

[37] GPU_PWR_GD — R477 EV@0_4
[10,19] GC6_FB_EN — R469 EV@0_4
[17,19,30] EC_FB_CLAMP — R471 *EV@0_4

EV@SN74AHC1G32DCKR U23

FBVDDQ_EN [38]
R476 EV@100K/F_4

stuff EC_FB_CLAMP for GC6 1.0
stuff GC6_FB_EN for GC6 2.0

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	N15S-GT (MEMEORY/GND)	3A

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U21G
4/14 IFPAB

IFPAB

U21J
7/14 IFPEF

IFPE

IFPF

U21K
3/14 DACA

1B-7
2013/12/20 Change resistor to 2.2k.

U21M
9/14 XTAL_PLL

PLLVDD = 38mA

SP_PLLVDD = 17mA

VID_PLLVDD = 41mA

U21H
5/14 IFPC

IFPC

U21I
6/14 IFPD

IFPD

3V MAIN POWER

N15V stuff not support GC6.
1A-7 2013/10/21 add R5331 for not GC6 support.

+1.05V_GFX and GPU core power EN

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	N15S-GT (DISPALY)	3A

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For N15S-GT sku
N15S-GT device ID=0x0FE4
R3=40.3k pull down.
1.ROM_SCLK =4.99K pull down
2.ROM_SO = 4.99K pull down
3.ROM_SI= Memory strap setting
3.STRAP0 = 50k Pull pu.
4.Strap4~1 = reserve Pull pu and Pull down

For N15V-GL-B and N15V-GM-B sku
Board_ID0=
H=N15V-GM,L=N15V-GL
Device ID=0x1140
R3= N.C.
1.ROM_SCLK =10K pull down.
2.ROM_SI= 10k pull down
3.ROM_SO= 10k pull down
4.Strap3~0 = RVL memory binary mode setting.
5.Strap4 =10k pull down

R3

U21L
10/14 MISC2
bga595-nvidia-n13p-gv2-s-a2
COMMON

GF119	GF117
STRAP5_NC	NC
MULTISTRAP_REF1_GND	NC
MULTISTRAP_REF2_GND	NC

R442 EV@40.2K_4

N15S Based on RVL.
N15V pull down10k.

Pull Down 4.99k for N15S-GT.
Pull Down 10k for N15V.

	CS24992FB26
4.99k	CS31002FB26
10k	CS31502FB24
15k	CS32002FB29
20k	CS32492FB16
24.9k	CS33012FB18
30.1k	CS33482FB22
34.8k	CS34532FB18
45.3k	

N15S-GT
STRAP1---> 50k PU
N15V-GM\GL
STRAP4---> 10k PD

Default: HYNIX

N15S Strap0 pull up 50k, strap1~4 reverve only.
N15V Strap4 pull down 10k, strap0~3 based on RVL binary setting.

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

U21N
8/14 MISC1
bga595-nvidia-n13p-gv2-s-a2
COMMON

1B-7
2013/12/20 Change resistor to 2.2k.

GF117	GF119
NC	I2CB_SCL
NC	I2CB_SDA

GF117	GF119
NC	GPIO16
NC	GPIO20
NC	GPIO21

EC/S5 VGA/VGA
EV@2N7002DW

EC_FB_CLAMP [17,30]
GC6_FB_EN [10,17]

N15S -> GPIO0 un-stuff Q24 and EC_FB_CLAMP.
GPIO6 Un-stuff Q26\R70 and FB_CLAMP_REQ#.

N15V -> GPIO0 stuff Q24 and EC_FB_CLAMP, un-stuff R75 GC6_FB_EN.
GPIO6 stuff Q26\R70 and FB_CLAMP_REQ#, un-stuff R76,FB_Clamp_req#.

dGPU_OPP# = EC control
GPIO12 AC detect
AC high
DC low

1C1-1 2014/02/6 add VGA_ALERT# PU 10K for FAE request.

1C-2 2014/01/13 add R678\R677 PU and R679 PD for ICT.

VRAM Configuration Table

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	STN P/N
0000	DDR3(L) 256MBx16x4, 64bit,1000MHz(	HYNIX	H5TC4G63AFR-11C	AKD5PGWTW05	AKD5PGWTW13
0010(0101)	DDR3(L) 256MBx16x4, 64bit,,1000MHz(900MHz)	SAMSUNG	K4W4G1646D-BC1A		
0110(1001)	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	HYNIX	H5TC2G63FFR-11C		
0111(1010)	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J128M16JT-093G:K		
1000(1011)	DDR3(L) 128MBx16x4, 64bit,,1000MHz(900MHz)	SAMSUNG	K4W2G1646Q-BC1A		
0001(0100)	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J256M16HA-093G:E		

Strap [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N		Note
0100	DDR3(L) 256MBx16x4, 64bit,1000MHz(900MHz)	HYNIX	H5TC4G63AFR-11C			
1100	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	HYNIX	H5TC2G63FFR-11C			
0001	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J128M16JT-093G:K			
1101	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J256M16HA-093G:E			

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

GPIO ASSIGNMENTS

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	N15S-GT (GPIO/STRAPS)	3A

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MP-1 20140401 update Footprint like as ZQN.

CHANNEL A: 256MB/512MB DDR3

HYU 256Mx16, PN : AKD5PGWTW08---AKD5PGWTW07
HYU 128Mx16, PN : AKD5MZDTW03---AKD5MZDTW02
QBC TOP B/S
SAM 256Mx16, PN : AKD5PZDT501---AKD5PZDT500
SAM 128Mx16, PN : AKD5MGGT535---AKD5MGGT534

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[17] VMA_DQ[63..0]
[17] VMA_DM[7..0]
[17] VMA_WDQS[7..0]
[17] VMA_RDQS[7..0]

VRAM2 — EV@VRAM _DDR3_HYNIX_256MX16
VRAM4 — EV@VRAM _DDR3_HYNIX_256MX16
VRAM1 — EV@VRAM _DDR3_HYNIX_256MX16
VRAM3 — EV@VRAM _DDR3_HYNIX_256MX16

Should be 240 Ohms +-1% R32 EV@243/F_4
Should be 240 Ohms +-1% R407 EV@243/F_4
Should be 240 Ohms +-1% R7 EV@243/F_4
Should be 240 Ohms +-1% R404 EV@243/F_4

R31 EV@160/F_4
R405 EV@1.33K/F_4
R406 EV@1.33K/F_4
C413 EV@0.1U/10V_4
R37 EV@1.33K/F_4
R34 EV@1.33K/F_4
C28 EV@0.1U/10V_4
R9 EV@160/F_4
R12 EV@1.33K/F_4
R8 EV@1.33K/F_4
C1 EV@0.1U/10V_4
R401 EV@1.33K/F_4
R400 EV@1.33K/F_4
C400 EV@0.1U/10V_4

C25 C416 C37 C50 EV@1U/6.3V_4
C69 C419 C411 C402 C417 C8 EV@1U/6.3V_6
C412 C401 C35 C22 EV@10U/6.3V_6
C36 C398 C5 C11 EV@1U/6.3V_4
C393 C392 EV@10U/6.3V_6
C23 C415 C48 EV@0.1U/10V_4
C27 C396 EV@0.1U/10V_4
C421 C58 EV@10U/6.3V_6
C414 C3 C6 EV@0.1U/10V_4

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	DGPU Memory (DDR3)	3A

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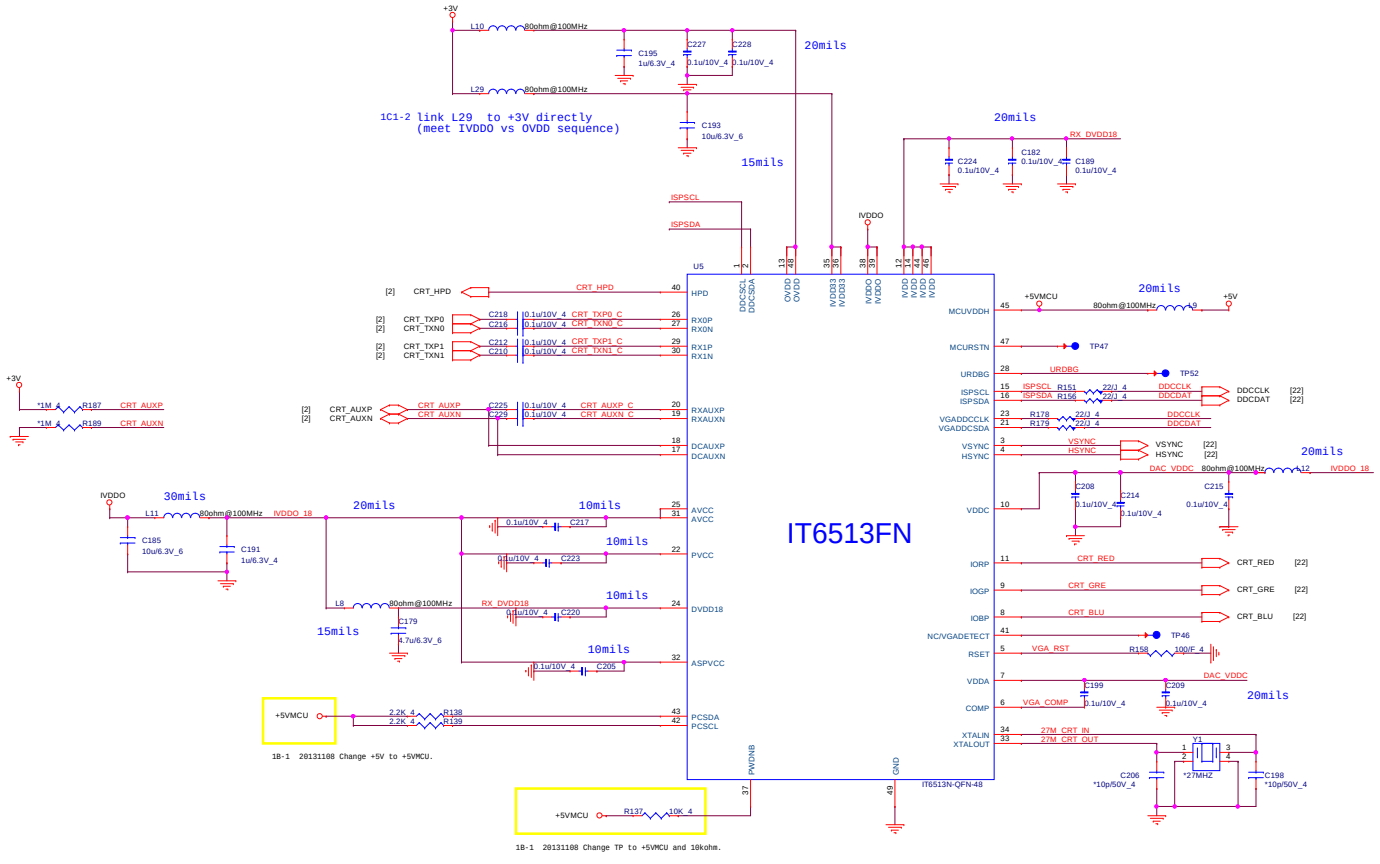
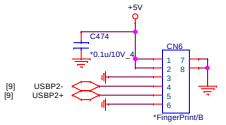
DP TO VGA

1A-1 2013/10/15 Change VGA ITE soltion to NXP.

1A-5 2013/10/18 Change VGA NXP soltion to ITE.



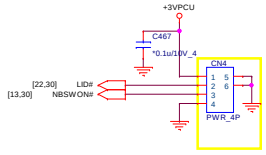
FingerPrint Conn



1A-7 2013/10/22 Change CN4 to 6pin.

1B-6 2013/12/18 Change CN5 USB port to port2.

Power Button/Conn

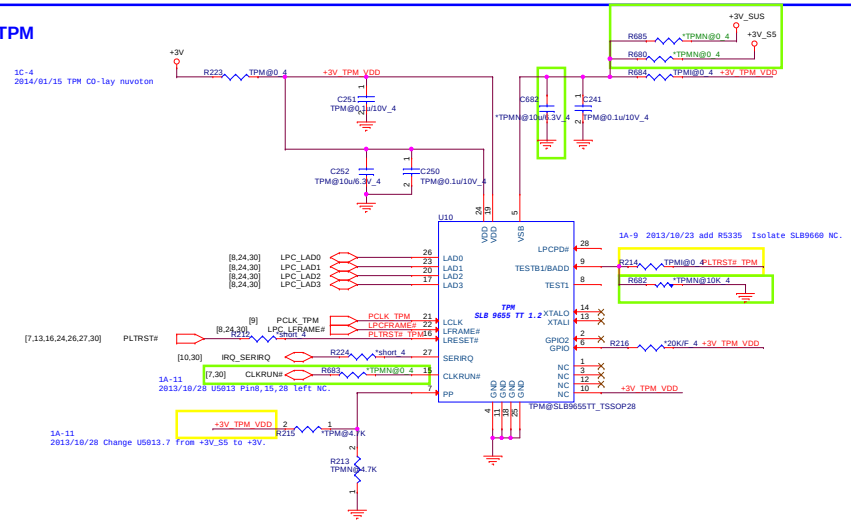


1A-1 2013/10/15 change to 6pin.

1B-2 2013/12/3 change to 4pin.

1B-3 2013/12/10 change CN6 footprint.

TPM



TPMI@-->for SLB9655 TPMN@-->for Nuvoton		
	SLB 9655	NPCT620
R685	Un-stuff	stuff
C682	Un-stuff	stuff
R683	Un-stuff	stuff
R213	stuff	Un-stuff
R682	Un-stuff	stuff
R214	stuff	Un-stuff
R684	stuff	Un-stuff

Green CLK Gen

1B-4 2013/12/13 remove Green GLK U9

Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	Mini DP/HD3SS2521	3A

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CRT

1C-1 2014/01/10 Remove U29 and add U40 and U41.

U40 M74VHC1GT125DF2G

U41 M74VHC1GT125DF2G

[21] HSYNC — HSYNC — CRTHSYNC

[21] VSYNC — VSYNC — CRTVSYNC

[21] CRT_RED

[21] CRT_GRE

[21] CRT_BLU

Q10 AP2331SA-7

CRTVDD5

CN3 CRT CONN

CRT_R1 CRT_G1 CRT_B1

DDCDAT [21]

DDCCLK [21]

TP48

U26 *RClamp0524P

U4 *RClamp0524P

Power trace tracking

[2,5,7,8,9,10,11,13,14,15,16,17,18,21,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38]
[21,23,25,28,29,32,36]
[7,8,10,11,13,21,25,27,28,29,30,31,32,36,37,38]
[31,32,33,34,35,36,37,38]

+3V +5V +3VPCU VIN

LCD CONNECTOR

Touch Panel interrupt

Q1 *2N7002K

1A-5 2013/10/18 add 0ohm short TP interrap pin.

MAX 1.5A

1A-5 2013/10/17 Change Touch screen power rail from 5V to 3V.

MP-1 20140328 Change Touch screen power rail from 3V to 5V.

MP-1 20140408 reserve 3V TP_PWR.

eDP

CCD-USB

Touch Panel

1A-13 2013/10/30 CN5002.6 add USB touch screen on/off pin to EC.

50398-04071-001

1C1-2 2014/03/11 Add R698 for TS_EN short TP_INT, for issue debug.

LCD Power

U1 G5243AT11U

Touch screen level shift I2C(reserve)

Q2 *TSI@2N7002DW

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.

Backlight Control

LID591#,EC intrnal PU

D1 1N4148WS

Q3 2N7002DW

Q4 DTC144EUA

1B-1 2013/11/28 Add BLON pin from PCH to lison.

1B-3 2013/12/10 change Q3.3 from +3V to +3VPCU.

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A

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HDMI

From PCH

[2] INT_HDMITX2N
[2] INT_HDMITX2P
[2] INT_HDMITX1N
[2] INT_HDMITX1P
[2] INT_HDMITX0N
[2] INT_HDMITX0P
[2] INT_HDMICLK+
[2] INT_HDMICLK-

C527 0.1u/10V_4 INT_HDMITX2N_C
C528 0.1u/10V_4 INT_HDMITX2P_C
C525 0.1u/10V_4 INT_HDMITX1N_C
C526 0.1u/10V_4 INT_HDMITX1P_C
C530 0.1u/10V_4 INT_HDMITX0N_C
C533 0.1u/10V_4 INT_HDMITX0P_C
C524 0.1u/10V_4 INT_HDMICLK+_C
C523 0.1u/10V_4 INT_HDMICLK-_C

R639 470_4
R641 470_4
R255 470_4
R249 470_4
R241 470_4
R239 470_4
R248 470_4
R245 470_4

R235 *680_4 INT_HDMICLK+_CONN
R231 *680_4 INT_HDMICLK-_CONN

1B-1 20131108 Change +5V to +3V for DG.

+5V
Q31
2N7002E
R226 *100K/F_4

INT_HDMICLK+_CONN R234 *short_4 INT_HDMICLK+_C
INT_HDMICLK-_CONN R230 *short_4 INT_HDMICLK-_C

HDMI connector

CN10
SHELL1 20
D2+ 1
D2 Shield 2
D2- 3
D1+ 4
D1 Shield 5
D1- 6
D0+ 7
D0 Shield 8
D0- 9
CK+ 10
CK Shield 11
CK- 12
CE Remote 13
NC 14
DDC CLK 15
DDC DATA 16
GND 17
+5V 18
HP DET 19
SHELL2 21
GND 23
GND 22

INT_HDMITX0P_C
INT_HDMITX0N_C
INT_HDMITX1P_C
INT_HDMITX1N_C
INT_HDMITX2P_C
INT_HDMITX2N_C
INT_HDMICLK+_C
INT_HDMICLK-_C
HDMI_DDCCLK_MB
HDMI_DDCDATA_MB
HDMI_5V
HDMI_MB_HPD
R218 *short_4
HP_DET_CN
HDMI connector

+5V
Q29
IN OUT GND
AP2331SA-7
C247 *220p/50V_4
D5 *AZ5125-01J
R221 20K_4

HDMI-detect

+3V
R63 1M_4
[2] INT_HDMI_HPD
Q20 2N7002K
HDMI_MB_HPD

I2C

From PCH
[2] HDMI_DDCCLK_SW
[2] HDMI_DDCDATA_SW

+3V
R165 2.2K_4
Q19 2N7002K
D2 RB501V-40
R184 2.2K_4
HDMI_DDCCLK_MB

R166 2.2K_4
Q18 2N7002K
D3 RB501V-40
R186 2.2K_4
HDMI_DDCDATA_MB

EMI

INT_HDMITX2P_C R246 *120/F_4 INT_HDMITX2N_C
INT_HDMITX1P_C R240 *120/F_4 INT_HDMITX1N_C
INT_HDMITX0P_C R253 *120/F_4 INT_HDMITX0N_C
INT_HDMICLK+_C R640 *120/F_4 INT_HDMICLK-_C

Power trace tracking

[2,5,7,8,9,10,11,13,14,15,16,17,18,21,22,24,25,26,27,28,29,30,32,33,34,35,36,37,38] +3V
[21,22,25,28,29,32,36] +5V

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	HDMI (PS8101)	1A
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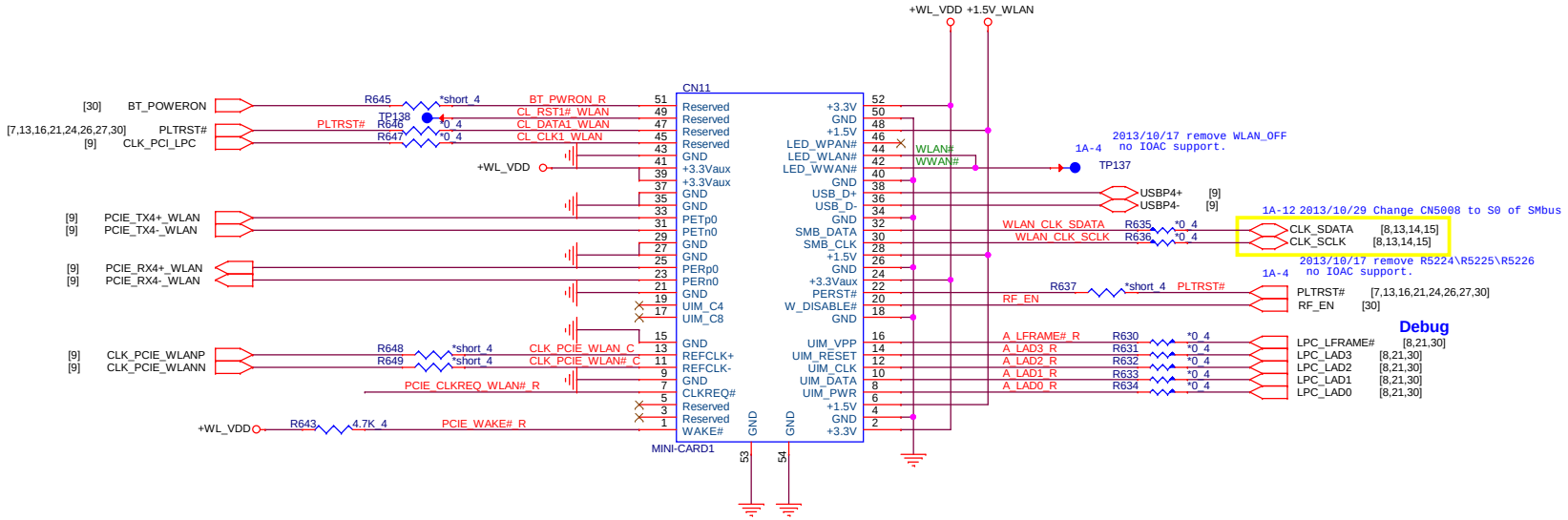
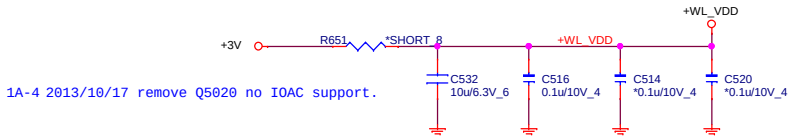
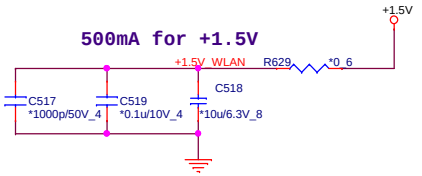
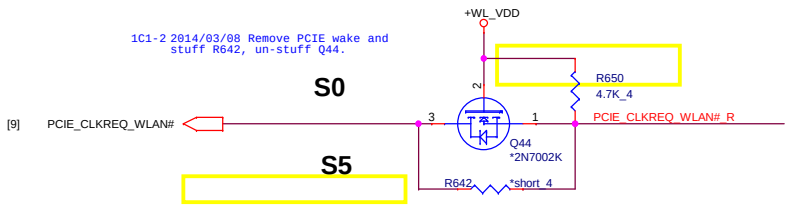
Mini Card 1 (MPC)









1A-4 2013/10/17 remove Q5019 no IOAC support.

Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1A

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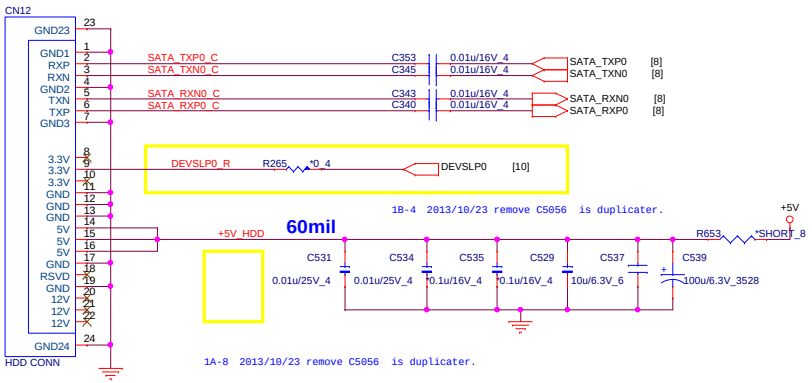
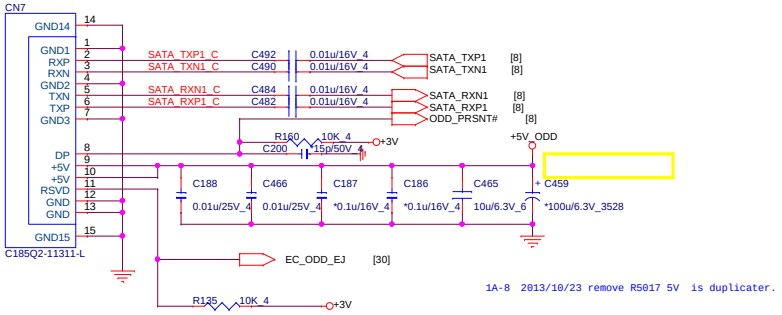
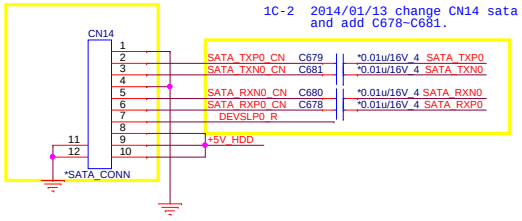
2.5" SATA HDD (HDD)



SATA ODD Connector



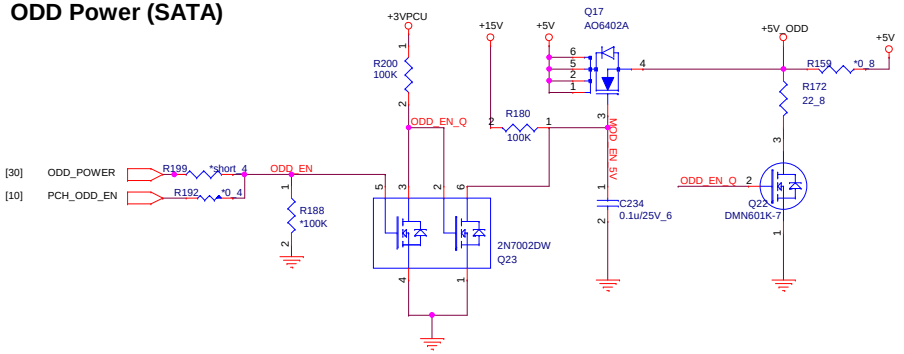
FFC Type SATA HDD CON



1C-2 2014/01/13 change CN14 sata net name and add C678~C681.

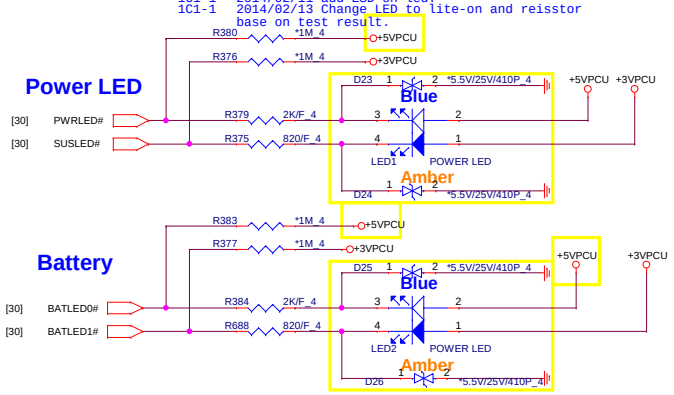
1B-3 2013/12/10 change Cn20 Pin define.

ODD Power (SATA)



POWER LED

1A-9 2013/10/17 Change power LED from +3VPCU to +3V_S5.
1A-10 2013/10/25 change LED from 3pin to 4pin. for acer reqeust.
1A-11 2013/10/28 change LED from 4pin to 3pin. and power LED to +3VPCU.
1B-2 2013/12/03 change LED from 3pin to 4pin.
1C1-1 2014/02/06 change Blue LED power rail to +5VPCU.
1C1-1 2014/02/11 add ESD on led.
1C1-1 2014/02/13 Change LED to lite-on and reisstor base on test result.



Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	SATA HDD/LED/SW	1A
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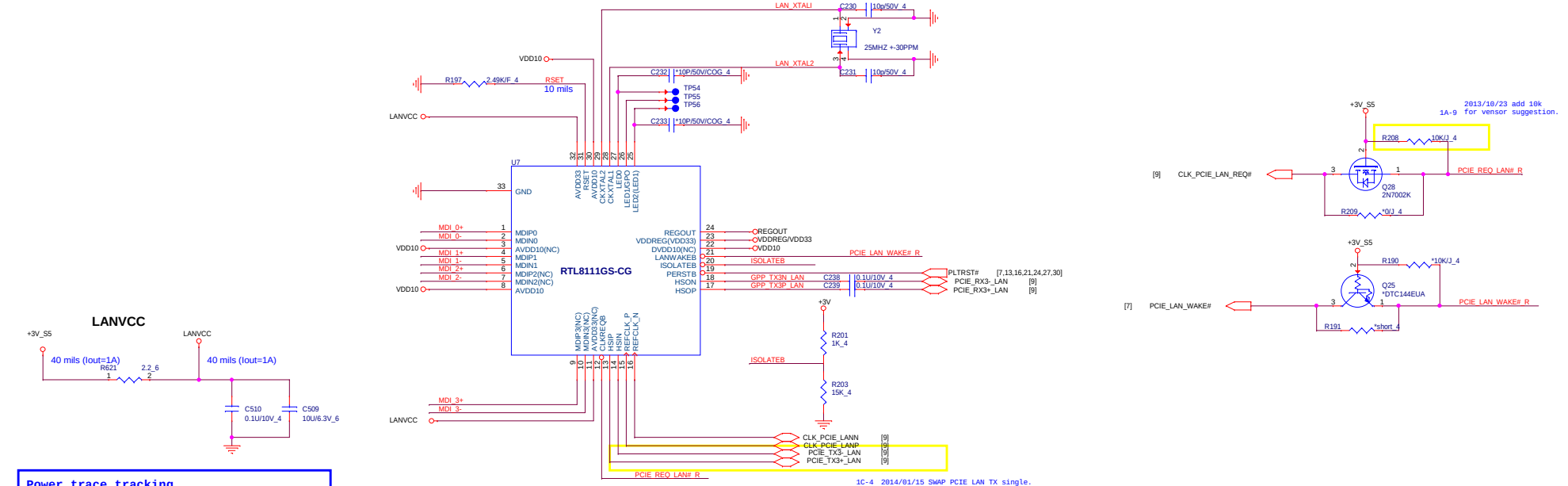
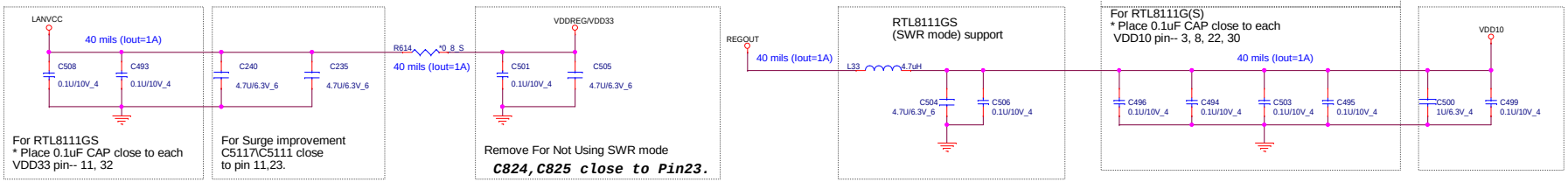
LAN

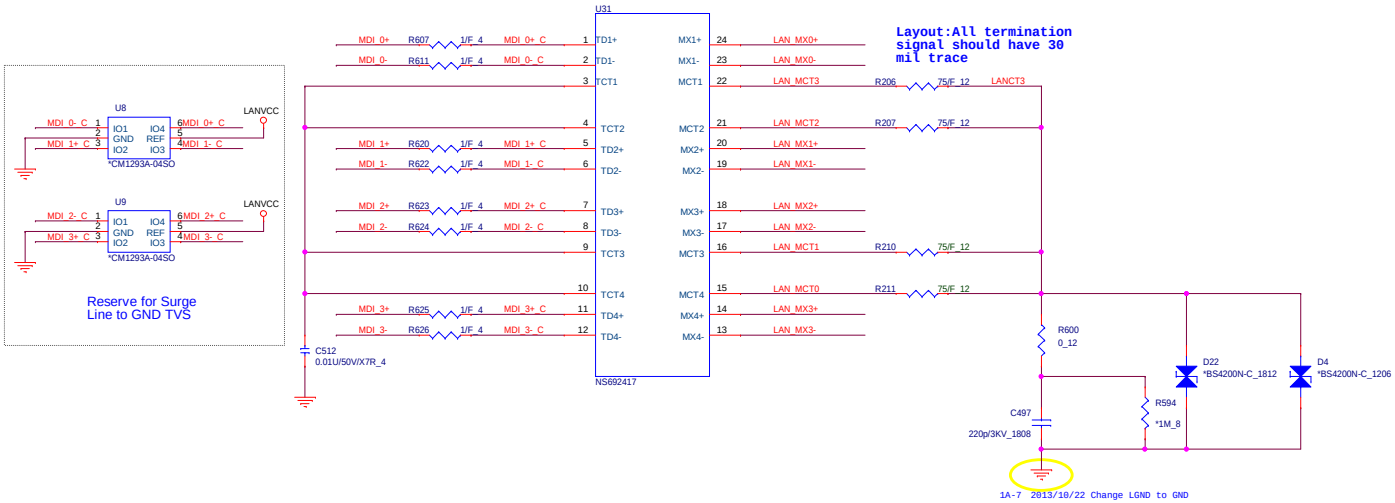


Power trace tracking

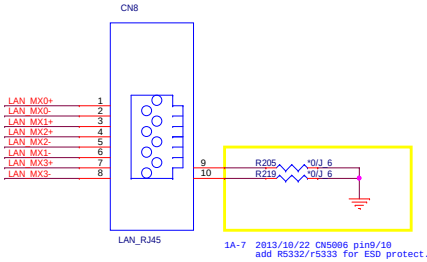
[5,7,8,9,10,11,13,21,27,29,30,32,35,37] +3V_S5
8,21,22,23,24,25,27,28,29,30,32,33,34,35,36,37,38] +3V



Tramsformer



RJ45 Connector



Quanta Computer Inc.		
PROJECT : ZQ0		
Size	Document Number: LAN (RTL8111GS)	Rev: 1A
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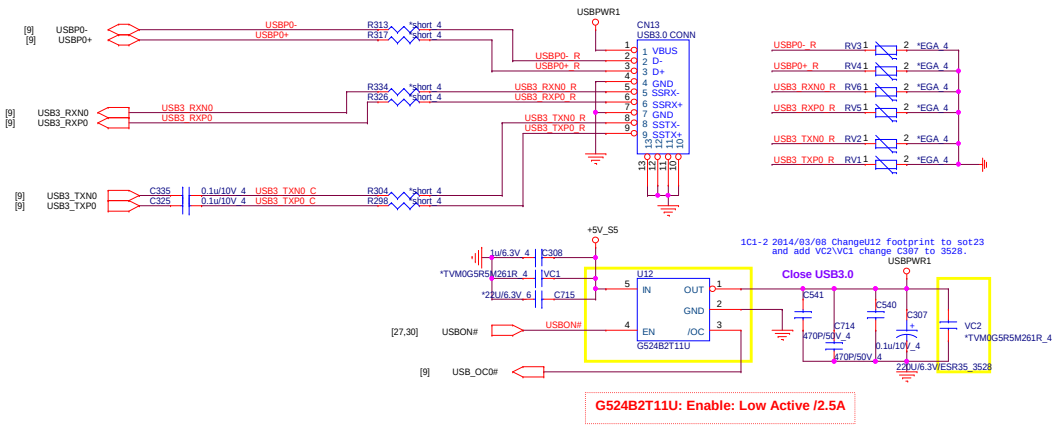
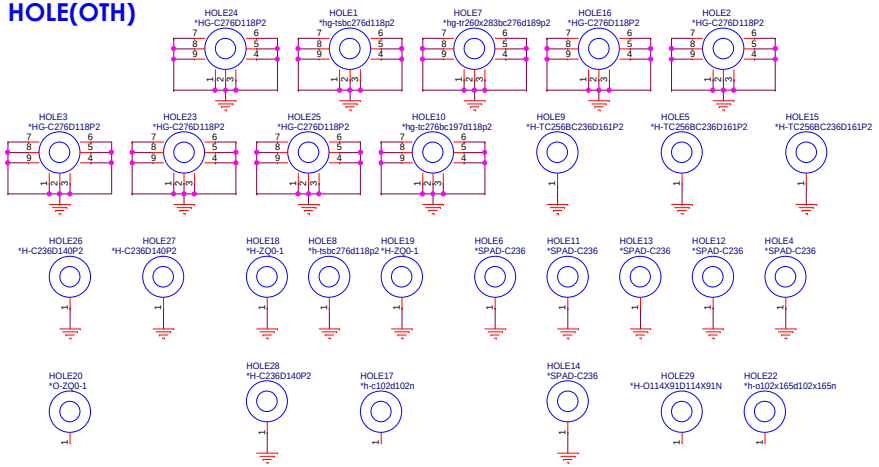
USB 3.0 Connector

1B-6 2013/12/18 Change CN12 USB2.0 port to port0.

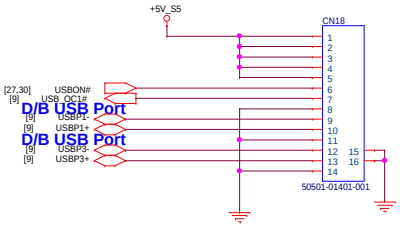


G524B2T11U: Enable: Low Active /2.5A

HOLE(OTH)

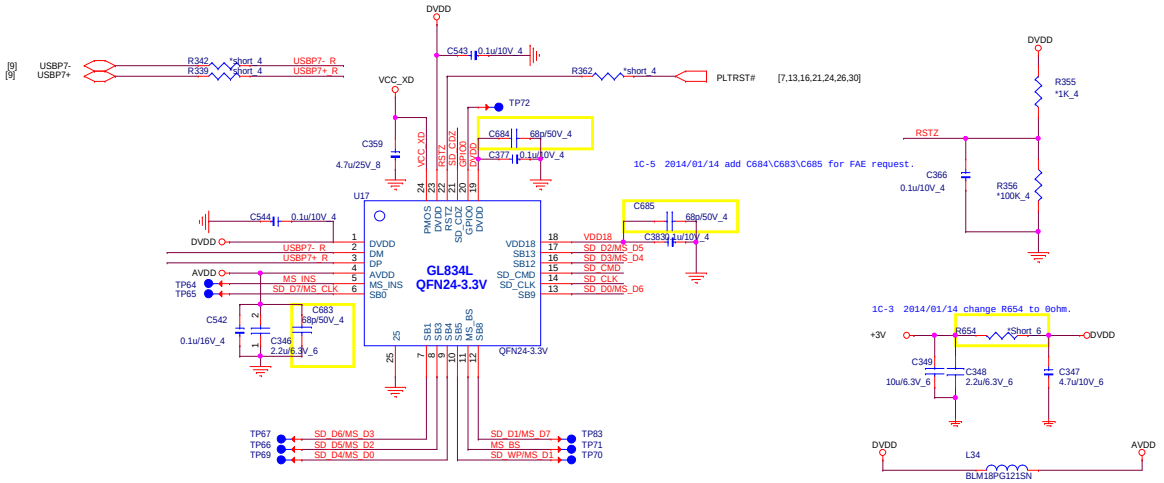


USB IO D/B

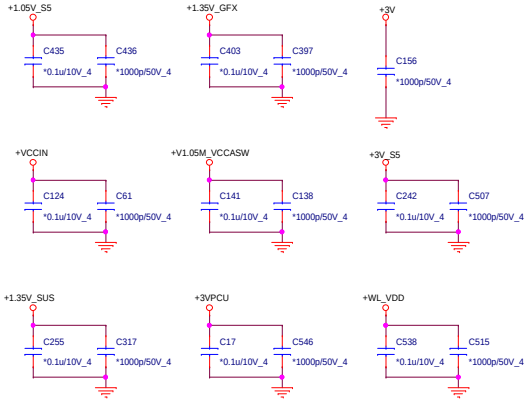


1B-6 2013/12/18 Change CN16 USB2.0 port to port1\port2 for DB.

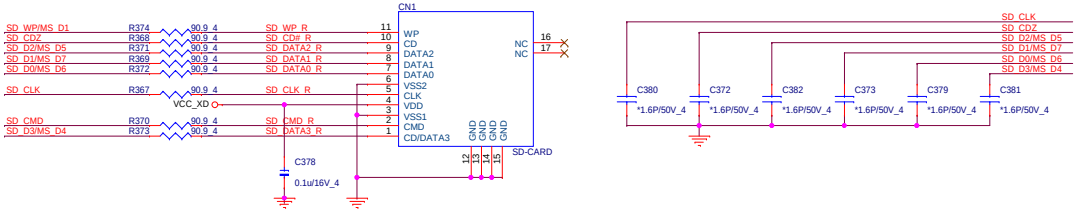
Card Reader and Connector



EMI



SD/MMC CARD READER (MMC)



Quanta Computer Inc.

PROJECT : ZQ0

Size	Document Number	Rev
	USB Port/ DB	1A
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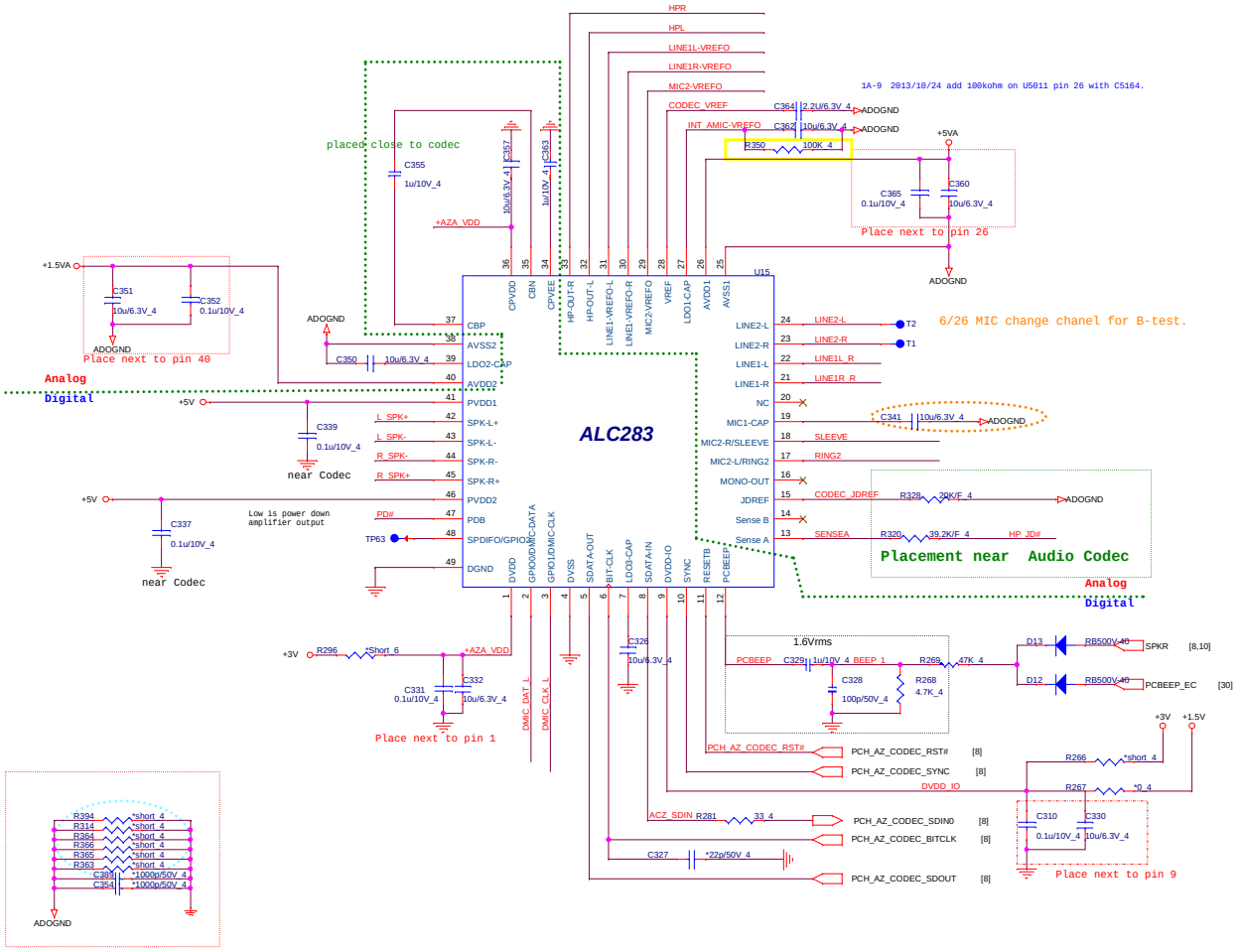
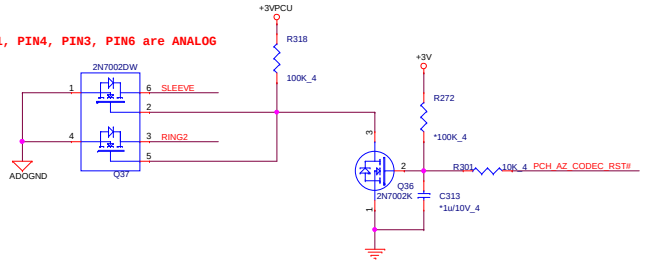
Codec(ADO)

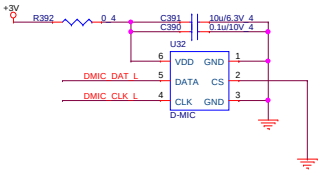


Grounding circuit(ADO)



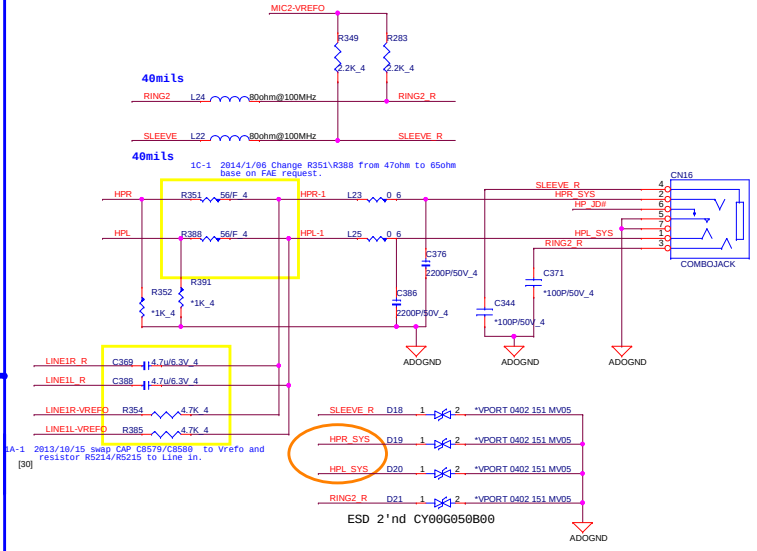
D-Mic

1B-5 2013/12/18 U34 pin6 reserve 0402 resistor for power noise issue.

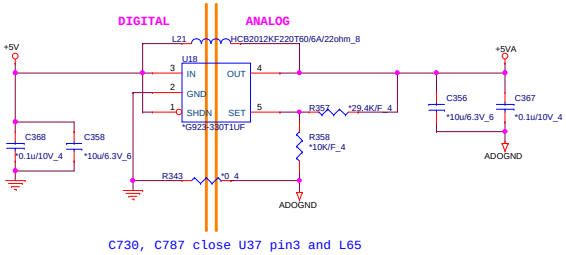


1A-7 2013/10/22 del C5079.

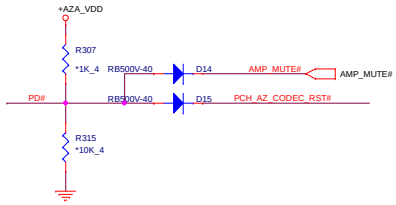
Universal Audio Jack



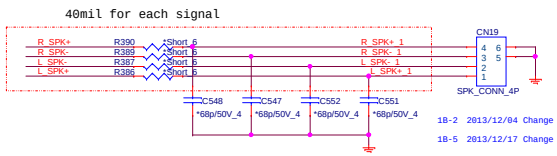
Codec PWR 5V(ADO)



Mute(ADO)



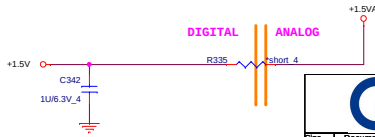
Internal Speaker



1B-2 2013/12/04 Change PK and footprint.

1B-5 2013/12/17 Change C414 pin define

Codec PWR 3V/1.5V(ADO)



Quanta Computer Inc.		
PROJECT : ZQ0		
Size	Document Number: ALC283/HP/SPK	Rev: 3B
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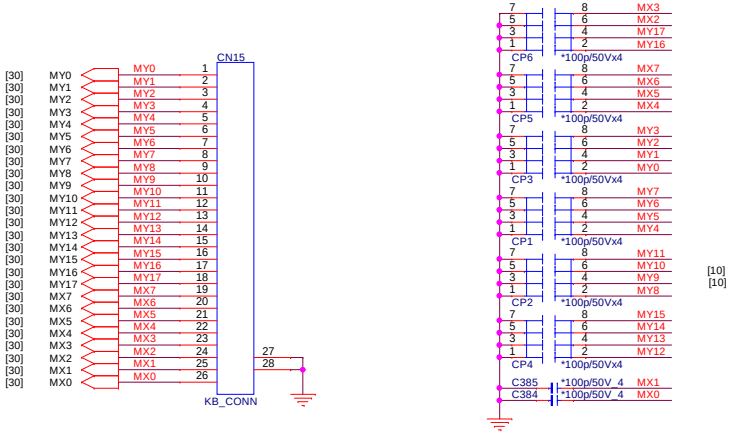
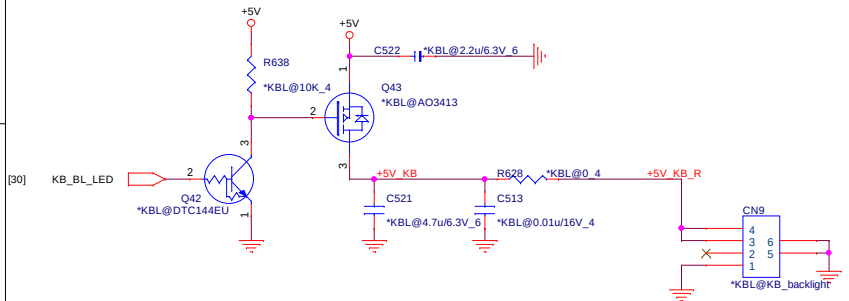
K/B (KBC)



1A-7 2013/10/22 change CN24 pin define based on spec.
1A-8 2013/10/22 change CN24 pin define based on spec based on ZRQ.

KB_BL LED (KBC)



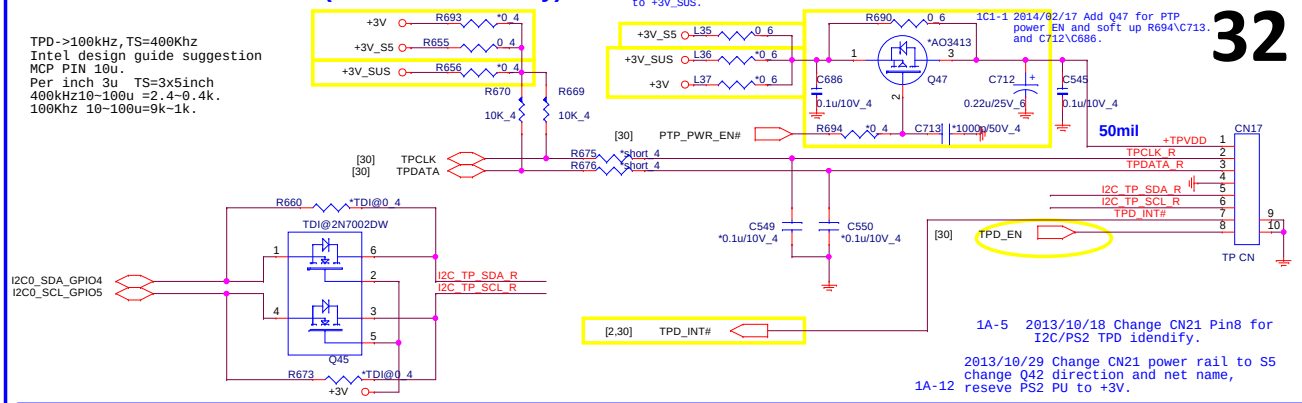
1A-7 2013/10/22 change CN25 pin define for spec.

1A-8 2013/10/23 change CN25 footprint.

TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

1C-2 2014/01/13 Change TP power rail from +3V_S5 to +3V_SUS.
1C-4 2014/01/15 reserve TP power rail +3V_S5.
1C1-1 2014/02/17 Add Q47 for PTP power EN and soft up R694\C713. and C712\C686.

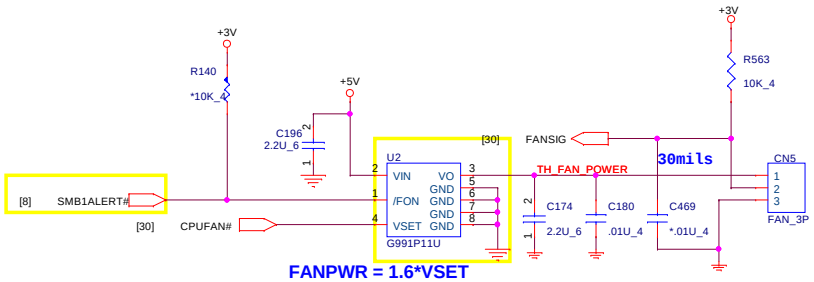
TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.



1A-5 2013/10/18 Change CN21 Pin8 for I2C/PS2 TPD idendify.

2013/10/29 Change CN21 power rail to S5 change Q42 direction and net name,
1A-12 reseve PS2 PU to +3V.

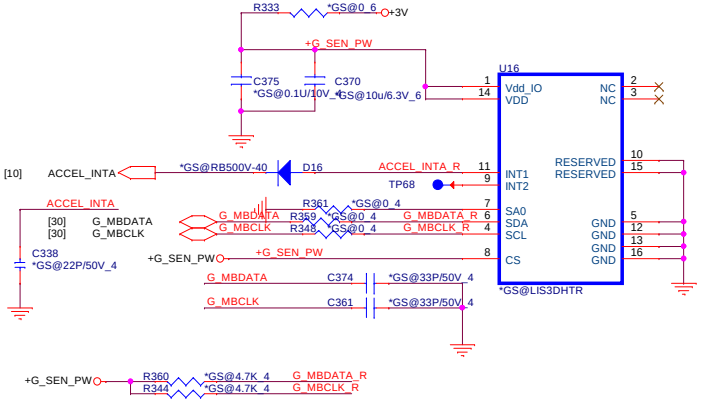
CPU FAN (THM)



FANPWR = 1.6*VSET

1A-12013/10/15 change pin define and add pwm IC U17.
1A-42013/10/17 Change U17 to G991P11U and PU U17 pin1.
1A-92013/10/24 Add alert on U17.1 for CPU themal tempture.
1A-13 2013/10/31CN15 Pin2/3 swap.

Accelerometer Sensor(reserve only)



Quanta Computer Inc.
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Size	Document Number	Rev
	KB/TP/FAN	3A
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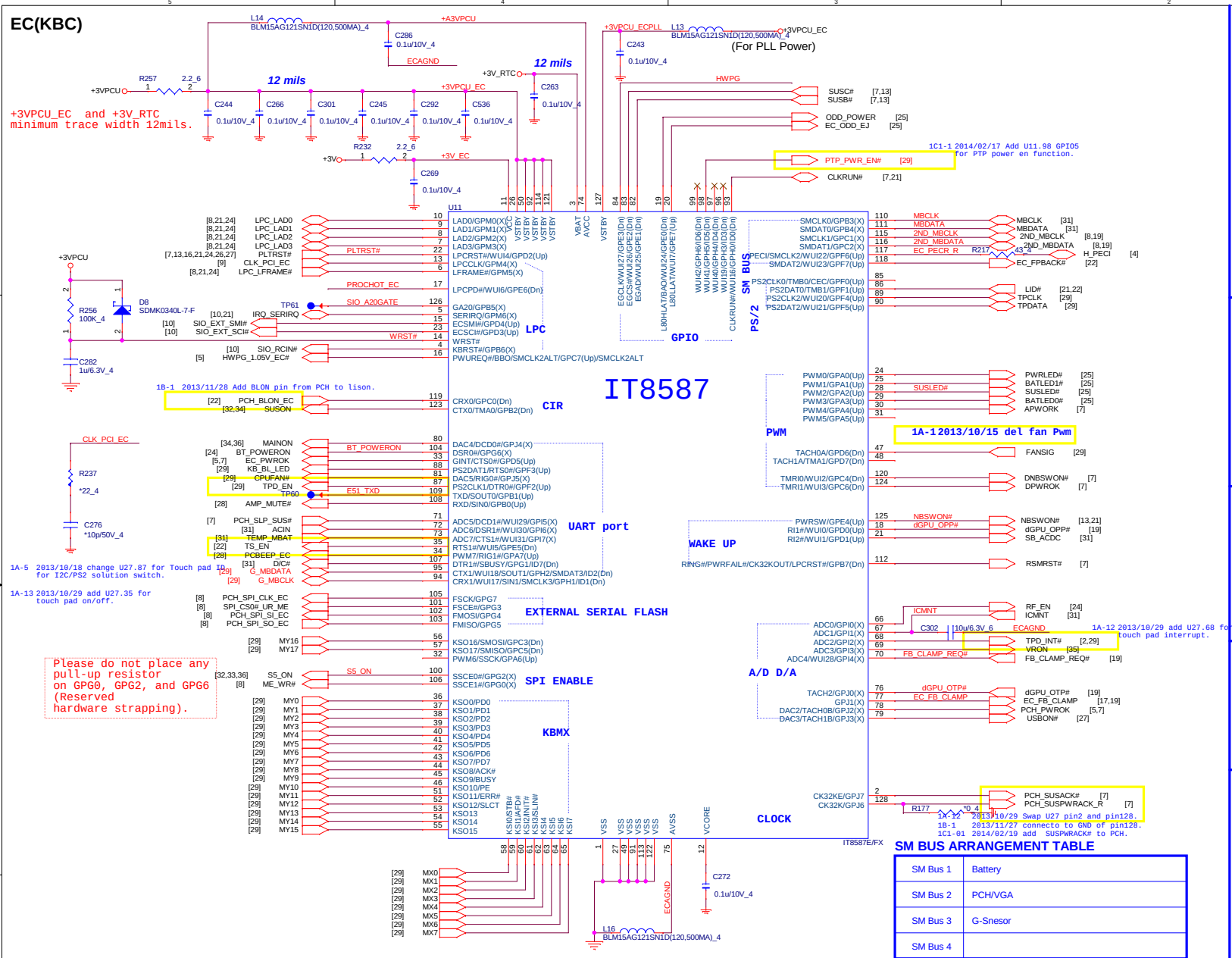
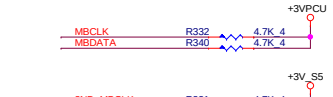
EC(KBC)

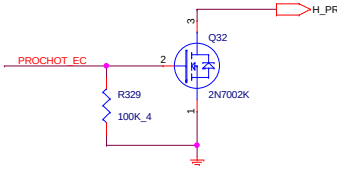


SM BUS ARRANGEMENT TABLE

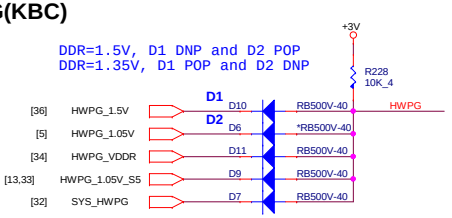
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	G-Snesor
SM Bus 4	

SM BUS PU(KBC)

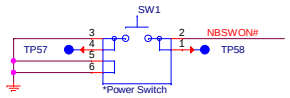




HWPG(KBC)



For test only



iRST

1A-4 2013/10/17 Del U22 becuse no support IOAC

Quanta Computer Inc.
PROJECT : ZQ0
Size | Document Number: KBC IT8587 | Rev 3A
Date: Tuesday, April 08, 2014 | Sheet 30 of 47

1A-7 2013/10/22 change PJ1 Pin define same as ZQN.

1A-14 2013/10/30 change Pin define revers.

20131024 Modify PN for low H.

recommend 200mA at least.

20140304 Short Pad

20140328 EMI add.

No need batt en pin

12/23 Change to avoid revise BATT

20131009 CHANGE

1A-7 2013/10/22 change PJ2 Pin define same as ZQN.

1A-10 2013/10/25 modify PJ2 footprint.

Add ESD diode base on EC FAE suggestion

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

Pin10 ILIM=0.793V
Rsr = 0.01ohm

Limit set on 60W/3.16A

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	Charger(BQ24737RGRR)	2A
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MAIND → MAIND [33,36]

SYS_SHDN# → SYS_SHDN# [10,36]

20140304 C1-Stage Remove Jumper

20140304 Short Pad

+5VPCU
5 Volt +/- 5%
TDC : 6.8A
PEAK : 9A
OCP : 11A
Width : 280mil

+3VPCU
3.3 Volt +/- 5%
TDC : 3A
PEAK : 4A
OCP : 5A
Width : 120mil

PU3 TPS51225RUKR

OCP:11A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=11-(3.367/2)=9.316A
Vth=9.316A*14mOhm+1mV=131.43mV
R(Ilim)=(131.43mV*8)/10uA
=105.14K

OCP:5A
L(ripple current)
=(9-3.3)*3.3/(6.8u*0.355M*9)
~0.865A
Iocp=5-(0.865/2)=4.57A
Vth=4.57A*14mOhm+1mV=64.94mV
R(Ilim)=(64.94mV*8)/10uA
~51.95K

1/13 Adding +3V_SUS power for touch pad
(By acer request)

TDC : 0.038A
PEAK : 0.05A
Width : 20mil

TDC : 3A
PEAK : 4A
Width : 120mil

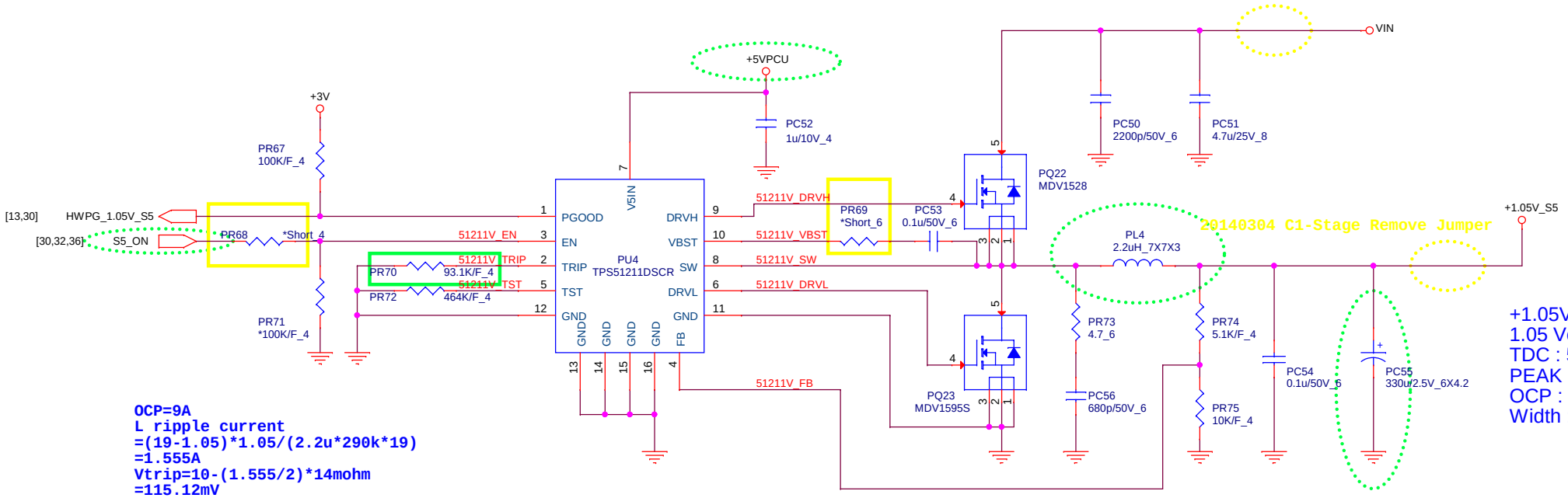
TDC : 3.77A
PEAK : 5.02A
Width : 160mil

TDC : 0.69A
PEAK : 0.92A
Width : 40mil

TDC : 0.6A
PEAK : 0.81A
Width : 40mil

Quanta Computer Inc.		
PROJECT : ZQ0		
Size	Document Number: SYSTEM 5V/3V (TPS51225)	Rev 2A
Date: Tuesday, April 08, 2014	Sheet 32 of 47	

20140304 C1-Stage Remove Jumper

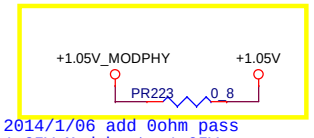


20140304 C1-Stage Remove Jumper

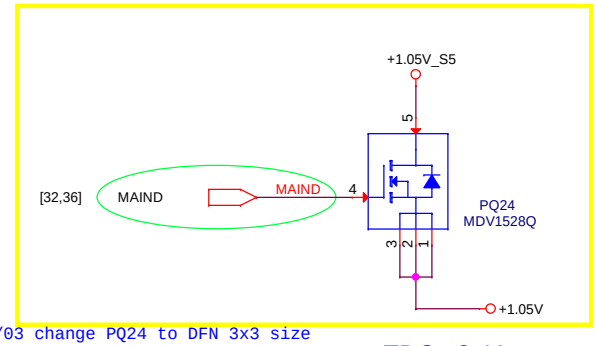
+1.05V
1.05 Volt +/- 5%
TDC : 5.7A
PEAK : 7.2A
OCP : 9A
Width : 240mil

OCP=9A
L ripple current
=(19-1.05)*1.05/(2.2u*290k*19)
=1.555A
Vtrip=10-(1.555/2)*14mohm
=115.12mV
Rlimit=115.12mV/10uA*8=92.09Kohm

VFB=0.7V



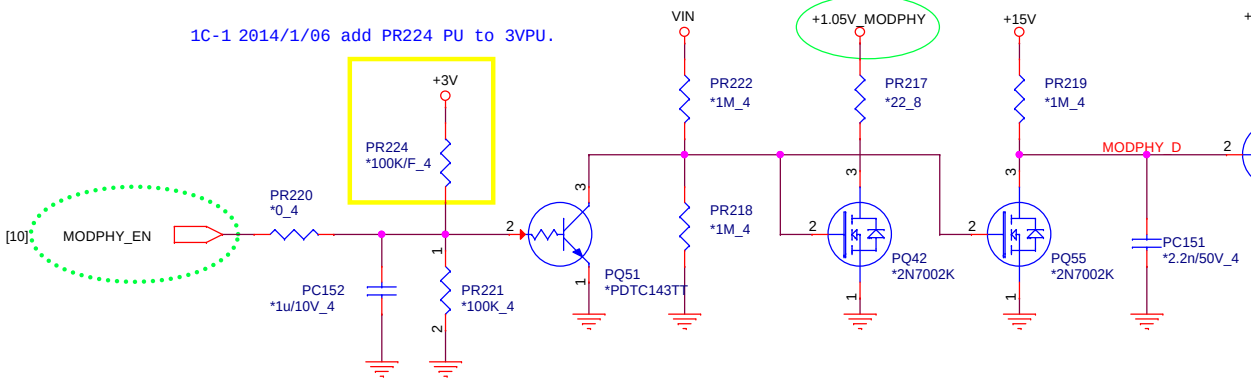
1C-1 2014/1/06 add 0ohm pass 1.05V_Modphy to 1.05V.



1B-2 2013/12/03 change PQ24 to DFN 3x3 size

TDC : 2.4A
PEAK : 3.2A
Width : 100mil

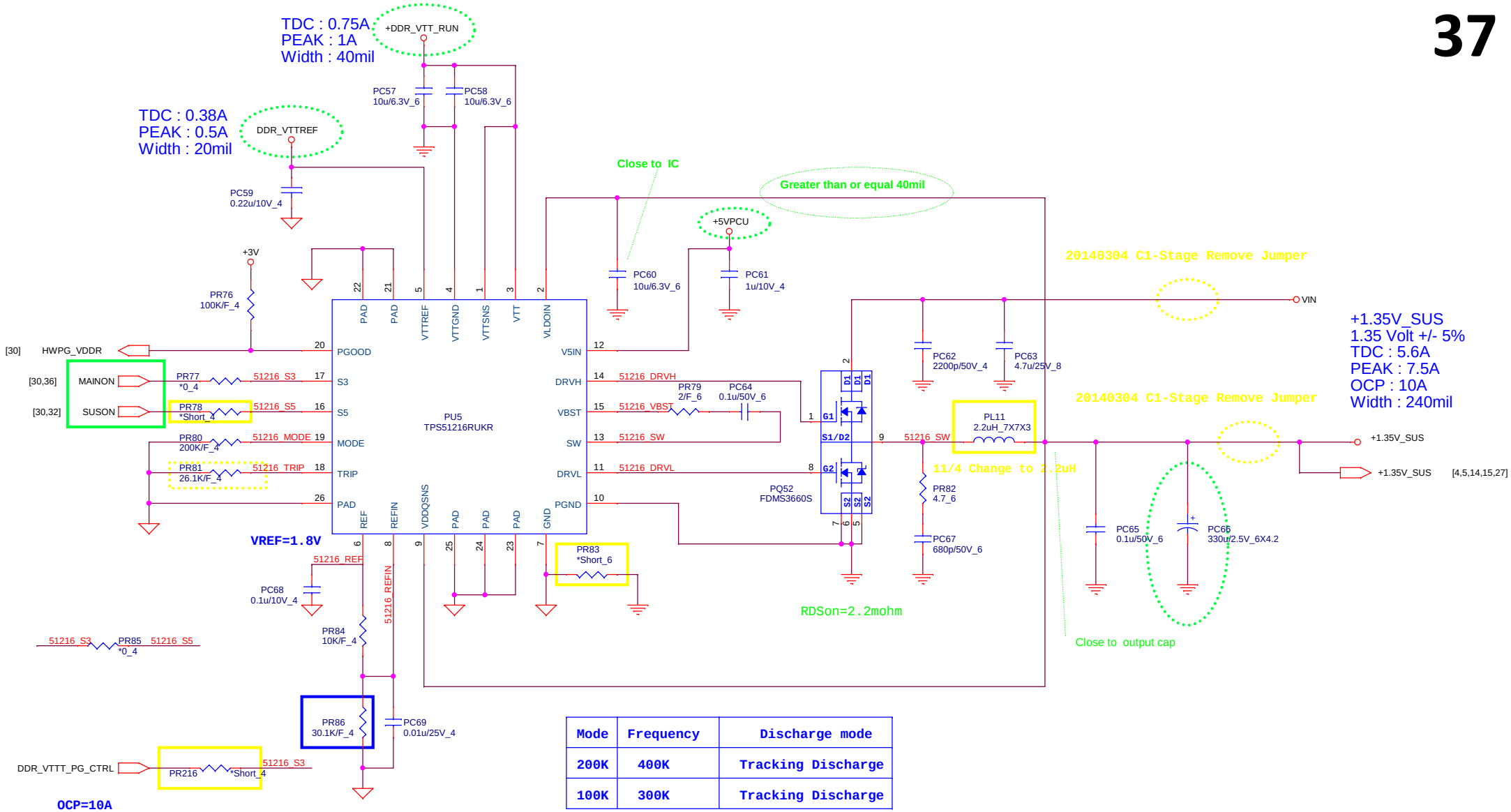
1C-1 2014/1/06 add PR224 PU to 3VPU.



+1.05V_MODPHY
TDC : 1.43A
PEAK : 1.9A
Width : 80mil

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	+1.05V_S5 (TPS51211)	2A
Date: Tuesday, April 08, 2014	Sheet 33 of 47	



Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	2A

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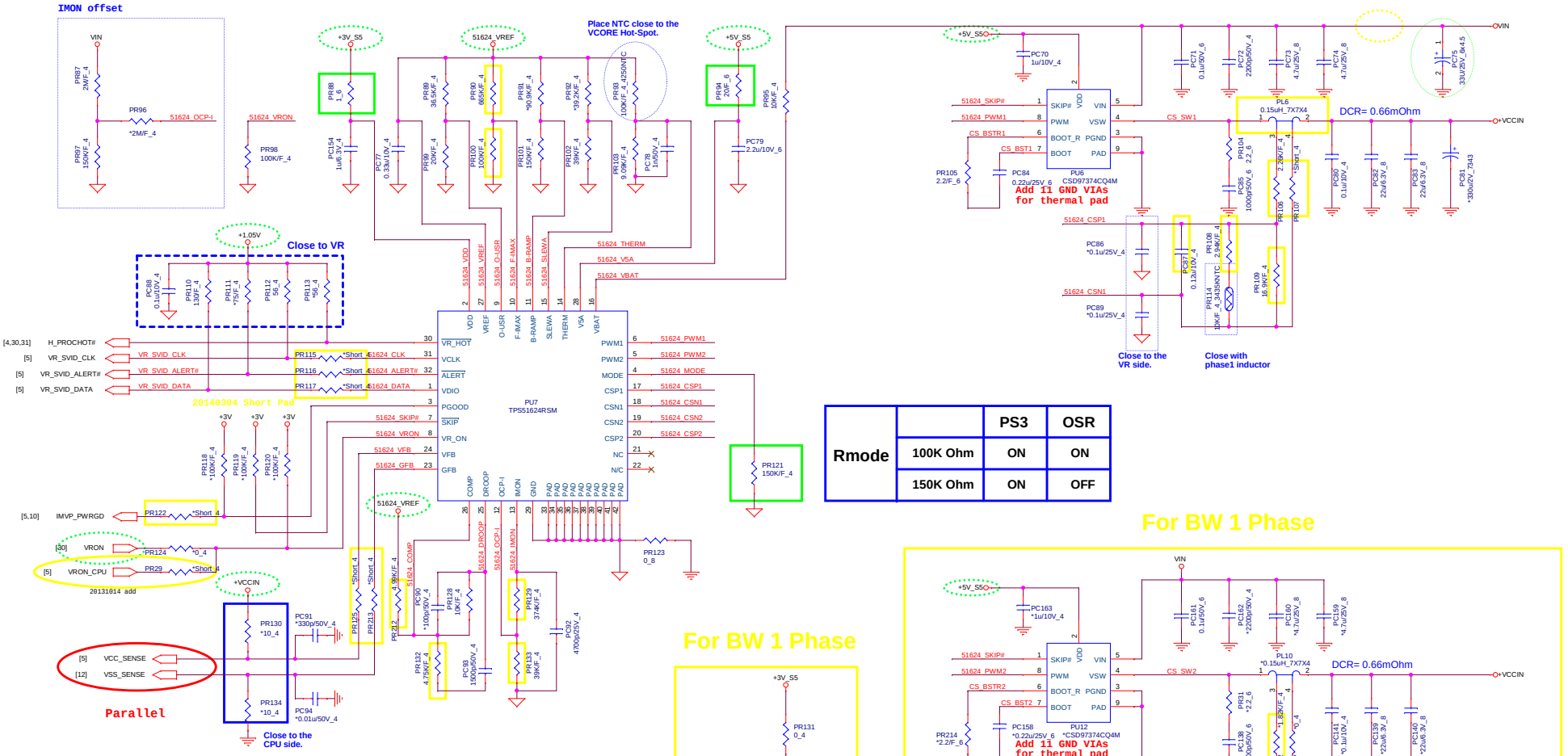
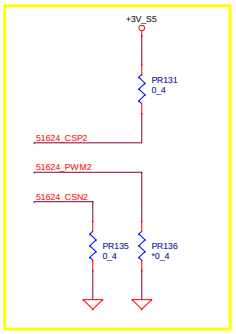
1C-2 20140113 PU6\PU12
change footprint for SMT request.

20140304 C1-Stage Remove Jumper



Rmode		PS3	OSR
	100K Ohm	ON	ON
	150K Ohm	ON	OFF

For BW 1 Phase



For BW 1 Phase

BW-U 15W (1 phase)

Icc TDC PL2：14A

Icc Max：32A

OCP：37A

Fsw：1.2MHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

BW-U 28W (1 phase)

Icc TDC PL2：19A

Icc Max：40A

OCP：47A

Fsw：800KHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

Quanta Computer Inc.

PROJECT ：ZQ0

Size	Document Number	Rev
	+VCCIN(TPS51624)	2A
Date: Tuesday, April 08, 2014	Sheet 35 of 47	

20140304 C1-Stage Remove Jumper

+1.5V
1.5Volt +/- 5%
TDC : 0.6A
PEAK : 0.8A
Width : 40mil

20140304 C1-Stage Remove Jumper

VFB=0.8V

V0=0.8*(R1+R2)/R2

Thermal protection

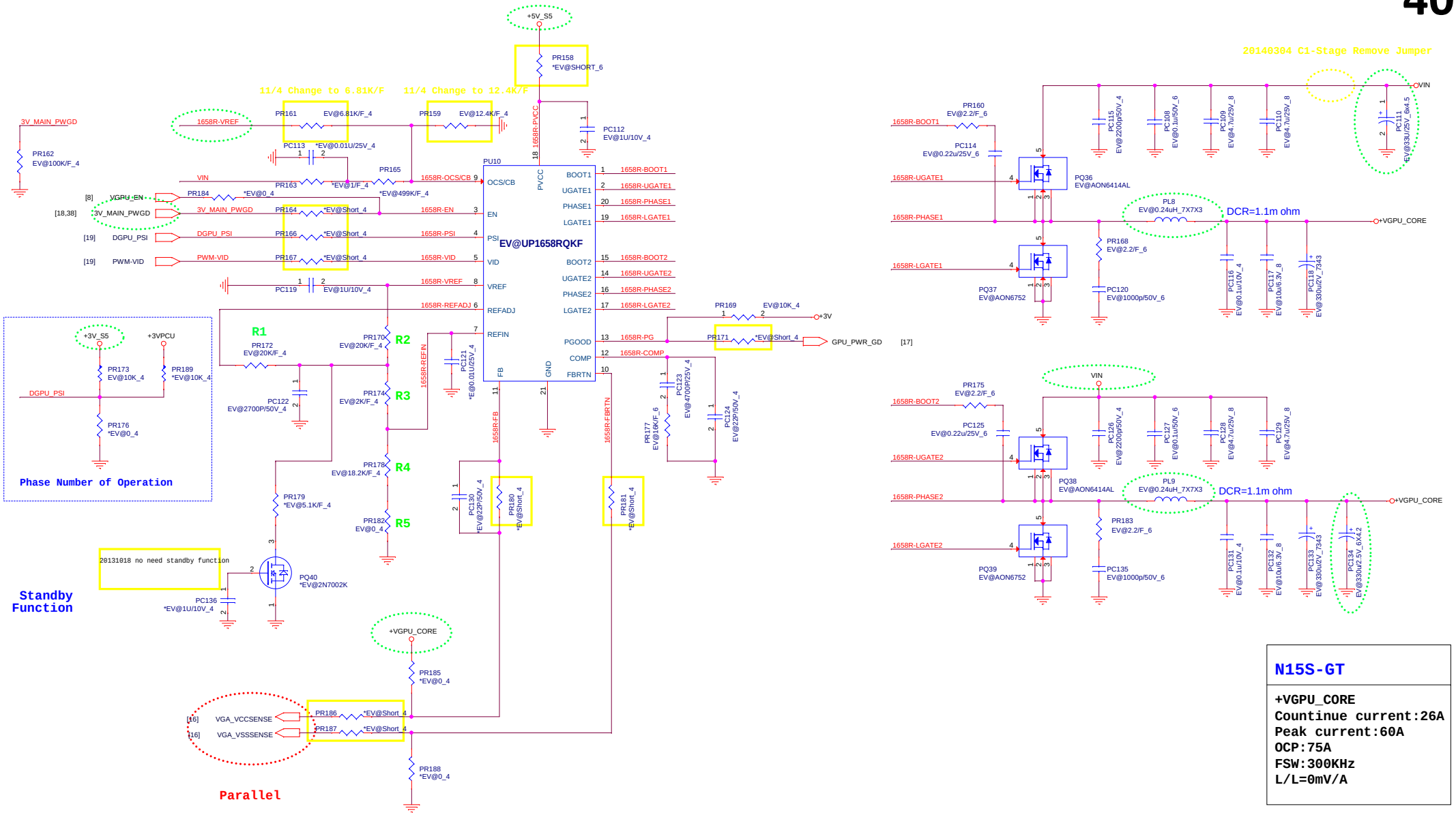
Need fine tune
for thermal protect point
Note placement position
TEMP=85C

11/4 Change to 1.47K/F

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.			
PROJECT : ZQ0			
Size	Document Number		Rev
	+1.5V/Thermal Protect		2A
Date: Tuesday, April 08, 2014	Sheet 36 of 47		

20140304 C1-Stage Remove Jumper



N15S-GT

+VGPU_CORE
Countinue current:26A
Peak current:60A
OCP:75A
FSW:300KHz
L/L=0mV/A

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	2A
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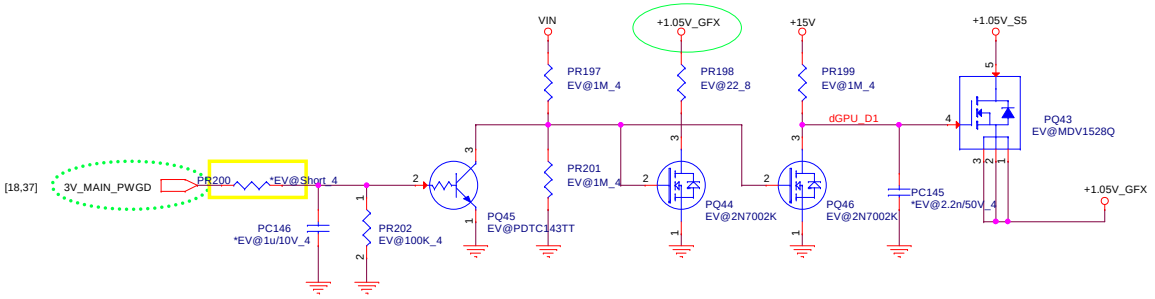
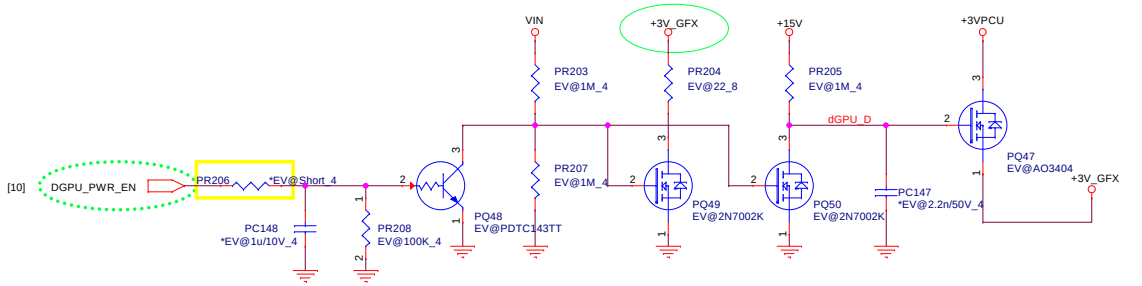
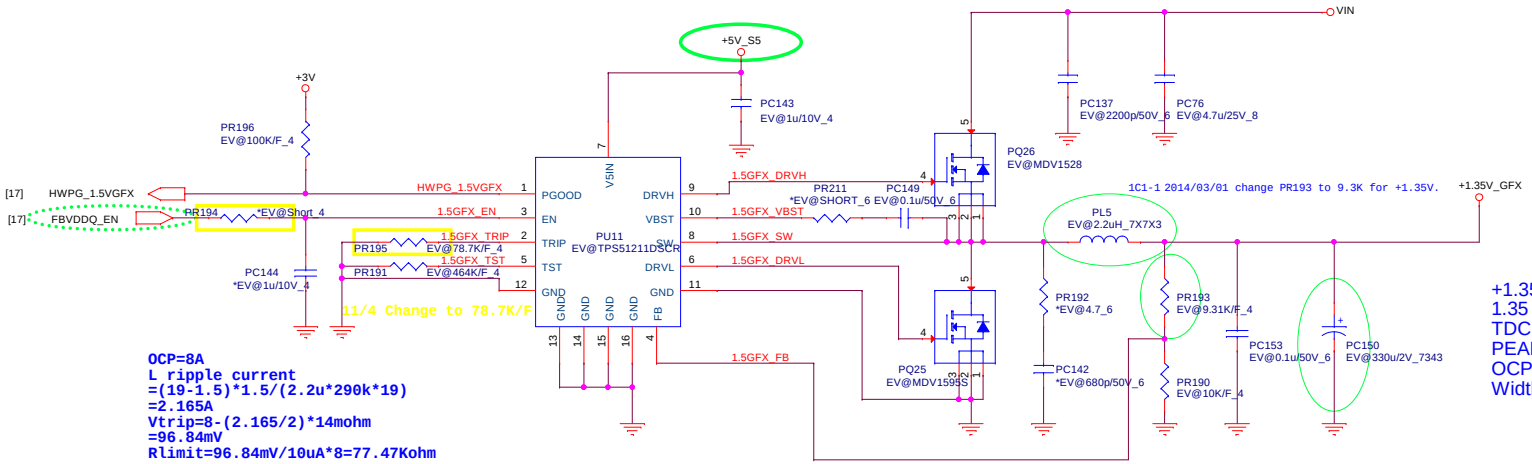
[16,17,18] +1.05V_GFX
[17,20,27] +1.35V_GFX
[16,17,18,19,30] +3V_GFX



+1.05V_GFX
TDC : 1.73A
PEAK : 2.3A
Width : 80mil



+3V_GFX
TDC : 0.17A
PEAK : 0.23A
Width : 20mil



OCP=8A
L ripple current
=(19-1.5)*1.5/(2.2u*290k*19)
=2.165A
Vtrip=8-(2.165/2)*14mohm
=96.84mV
Rlimit=96.84mV/10uA*8=77.47Kohm

VFB=0.704V

+1.35V_GFX
1.35 Volt +/- 5%
TDC : 3.3A
PEAK : 4.3A
OCP : 8A
Width : 160mil

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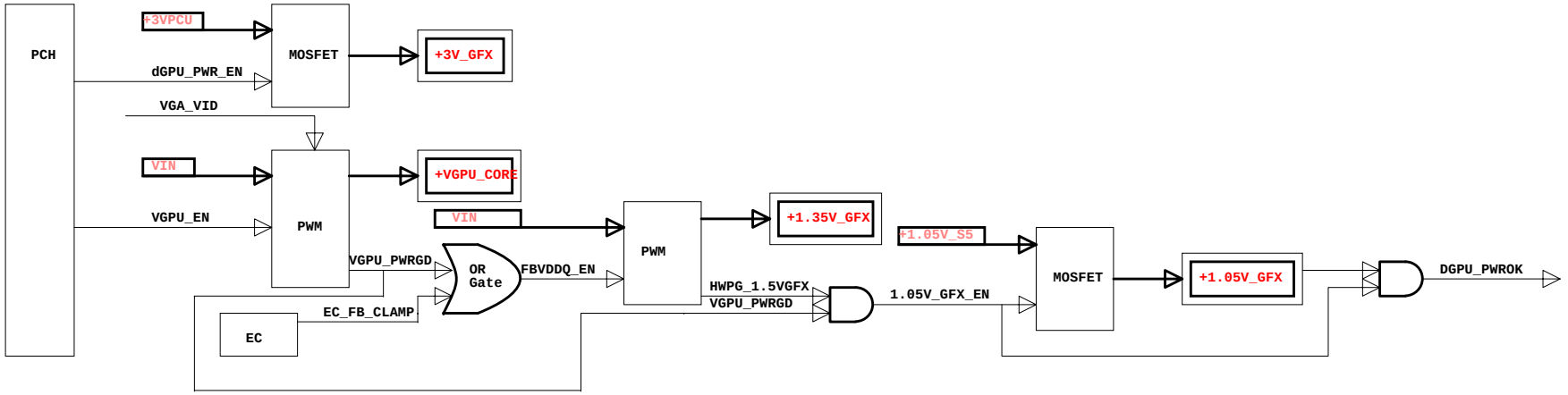
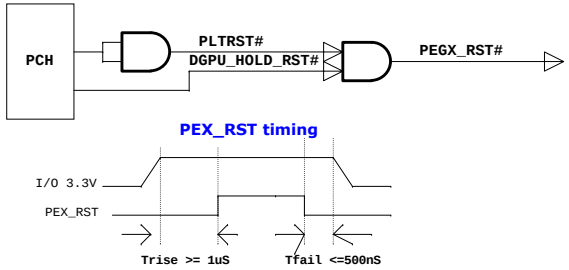
VGA power up sequence



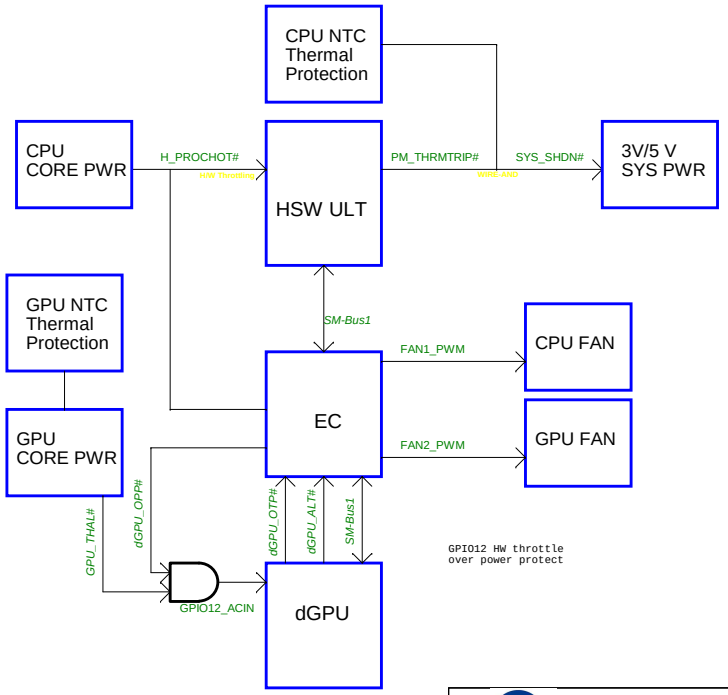
VGA Reset



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+VGPU_CORE	variation	External GPU POWER	VGPU_EN	S0
+3V_GFX	+3.3V	External GPU POWER	dGPU_PWR_EN	S0
+1.35V_GFX	+1.35V	External GPU POWER	FBVDDQ_EN	S0
+1.05V_GFX	+1.05V	External GPU POWER	1.05V_GFX_EN	S0

Thermal Follow Chart



dGPU_OPP# EC notify HW throttle over power protect
dGPU_ALT# for ADPS circuit to infrom EC NV dGPU VPS Alert
dGPU_OTP# VGA thrmtrip# => inform EC over temperature protect

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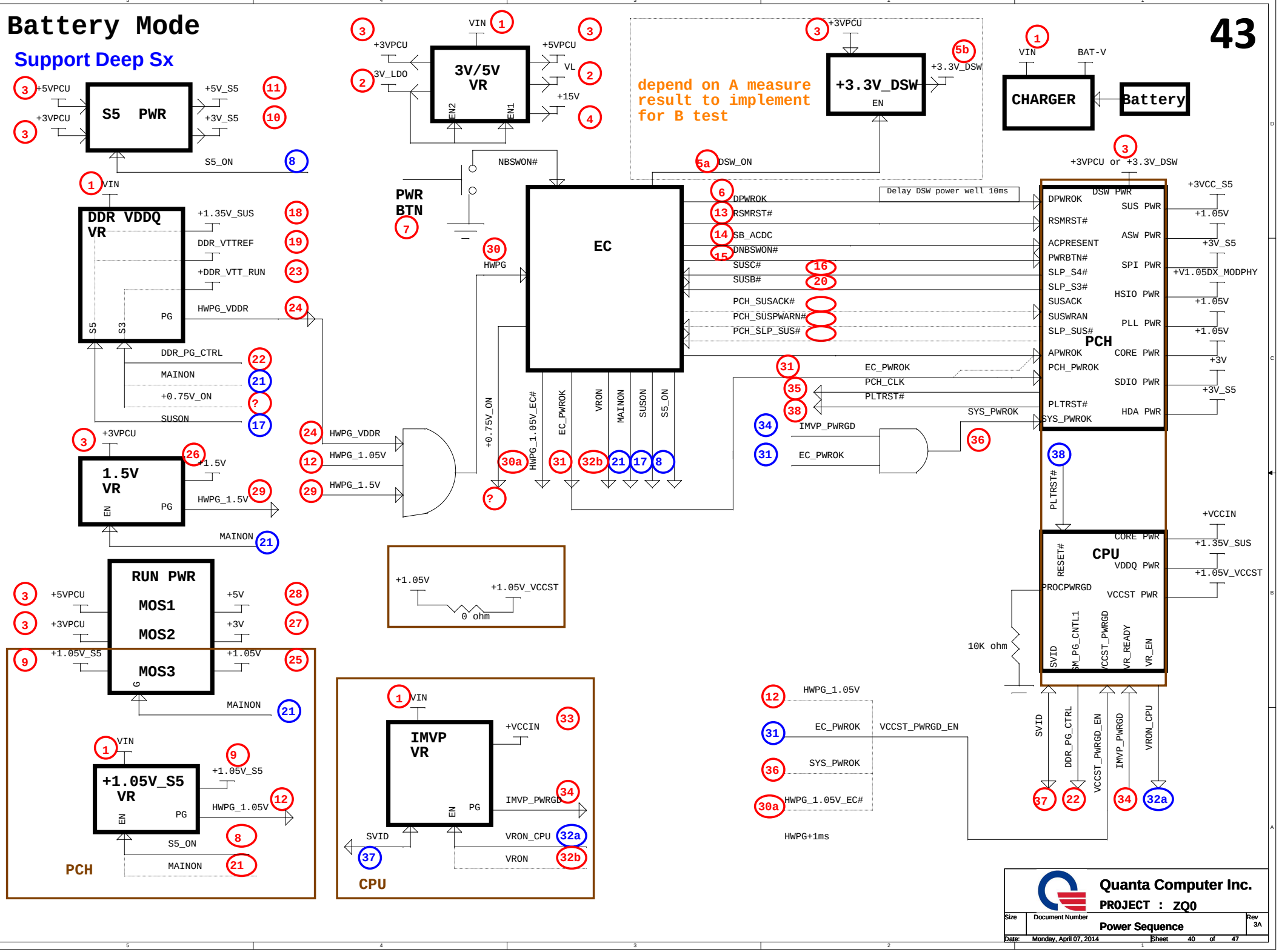
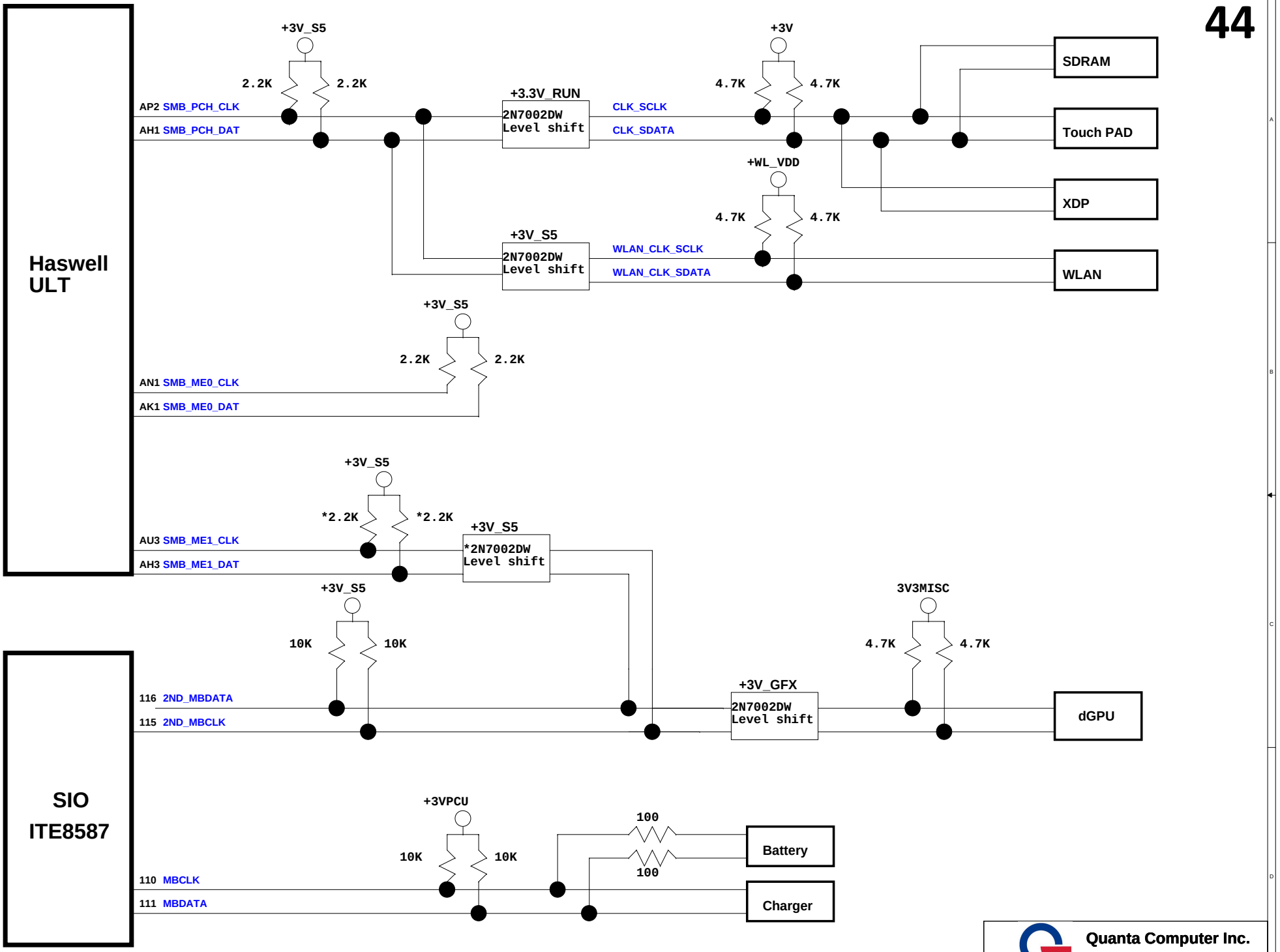
Battery Mode

Support Deep Sx





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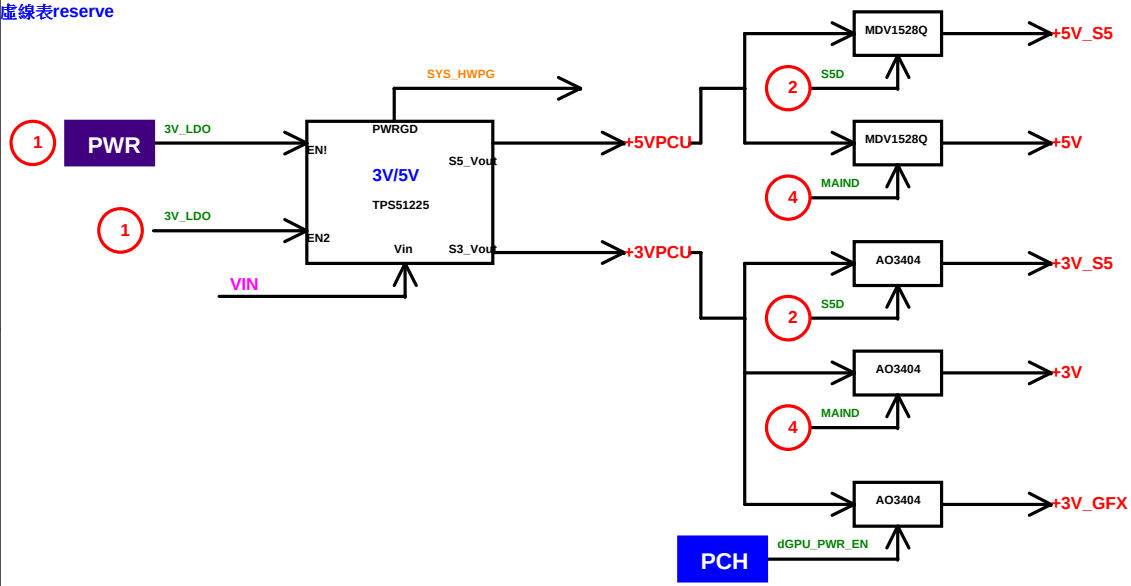
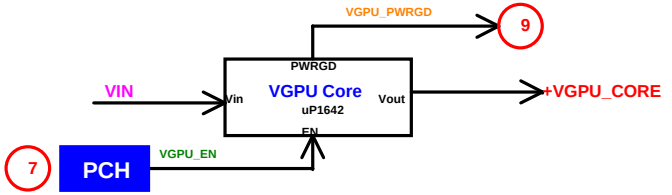
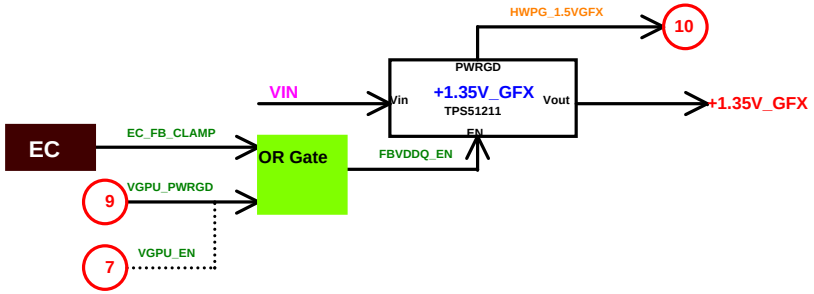
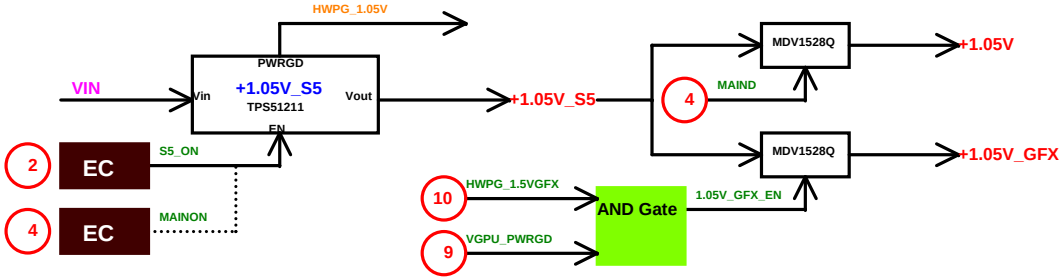
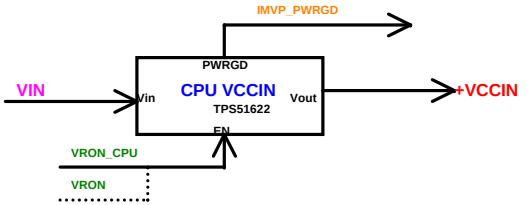
實線表defult
虛線表reserve

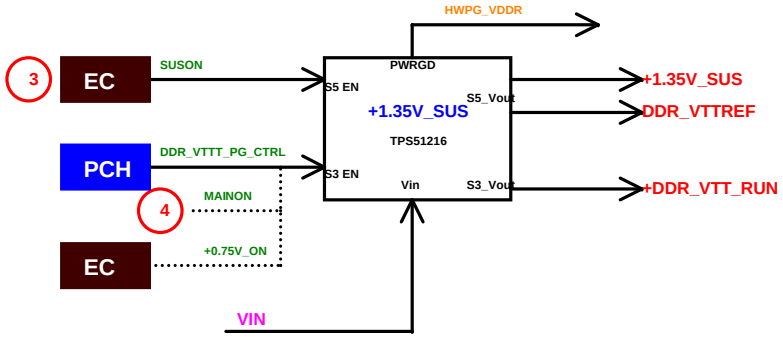


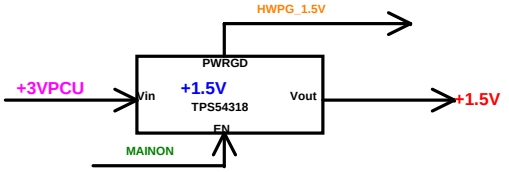












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	ULT PWR CONTROL	3A

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Model	Version		CHANGE LIST
ZQ0	1A-1	1	2013/10/15 change pin define and add pwm IC.(page31)
		2	2013/10/15 Change VGA ITE solution to NXP.(page 23)
		3	2013/10/15 power board CN change to 6pin.(Page 23)
		4	2013/10/15 U5017.12 change 27M crystal to VGA IC.(Page 23)
		5	2013/10/15 U5017.14 add power rail +3V_RTC(page23)
		6	2013/10/15 strap0 R672 DG 50k PU.(Page 19)
		7	2013/10/15 Change AND gat to Q63 D-MOS.(Page 19)
		8	2013/10/15 change pin define and add pwm IC U17.(Page 46)
		9	2013/10/15 for GC6 stuff R228\R1013\R226\R1012.un-stuff Q24\Q26\R227\R1011. (Page19)
		10	20131015 For GC6 NV DG GC6_FB_EN PD.(Page10)
		11	2013/10/15 following up acer define and swap USB3 and USB2 port.(Page9)
		12	2013/10/15 swap CAP C8579/C8580 to Vrefo and resistor R5214/R5215 to Line in.(Page30)
		13	2013/10/15 U27.30/U27.31 del fan Pwm signal.(Page32)
		14	20131015 change LVDS\USB3\RJ45\FAN\TPD\USB DB CN\DC-IN CN\Power Button\Cardreader\KB BLK CN\Power board, footprint.
	1A-2	1	2013/10/16 JDIM5 Swap M_B_DQS2/M_B_DQS3 and swap M_B_DQS#2/M_B_DQS#3.(page15)
		2	2013/10/16 JDIM6 Chage net name M_B_DQS#[7:0] to M_A_DQS#[7:0].(page14)
		3	2013/10/16 Add RTC charge circuit.(page8)
		4	2013/10/16 BT1.1 Chage +3V_RTC_0 to VCCTC_2.(page8)
		5	2013/10/15 change power rail from +3V_RTC_0 to VCCRTC_2.(page23)
	1A-3	1	2013/10/16 change R5285 from 330 to 100ohm for charge RTC battery.(page23)
		2	2013/10/16 2013/10/16 U58 add 0ohm R5322/R5323 for SMBus reserve for FW burnning.(page 23)
		3	2013/10/16 U58 pin24/25 add 33ohm for HSYNC/VSYNC.(page23)
		4	2013/10/16 U58.37 add 10 ohm for test pin avide i2c impact.(page 23)
		5	2013/10/16 U24 ball K4/G2 BIOS suggestion change SMI/SCI to GPIO~15.(page 10)
		6	2013/10/16 Add U34 flash 4M ROM reserve for ZQ0D.(page8)
		7	2013/10/16 change SMbus VGA to PCH SML0CLK/SML0DATA.(page 8)
	1A-4	1	2013/10/17 Change EC pin define for 2014 GPIO table.(page32)
		2	2013/10/17 Change All short pad to resistor.(All)
		3	2013/10/17 Change U17 to G991P11U and PU U17 pin1.(page31)
		4	2013/10/17 Remove Q25\R231\R232 because not support GPIO9 for ADPS circuit to infrom EC NV dGPU VPS Alert.(page19)
		5	2013/10/17 remove Q5020 no IOAC support.(page26)
		6	2013/10/17 remove R5224\R5225\R5226 no IOAC support.(page26)
		7	2013/10/17 remove WLAN_OFF no IOAC support.(page26)
		8	2013/10/17 Del U22 becuse no support IOAC.(page32)
	1A-5	1	2013/10/18 Change CN21 Pin8 for I2C/PS2 TPD idendify.(Page31)
		2	2013/10/18 Change VGA NXP soltion to ITE.(page23)
		3	2013/10/18 design change R5293 from 22ohm to 33ohm.(page23)
		4	2013/10/18 Change Touch screen power rail from 5V to 3V.(page24)
		5	2013/10/18 add 0ohm short TP interrap pin.(page24)
		6	2013/10/18 change U27.87 for Touch pad ID for I2C/PS2 solution switch.(page 32)
	1A-6	1	2013/10/18 Change Q63 to MOS.(page19).
		2	2013/10/21 reversal PEG lan for layout.(page9).
		3	2013/10/21 Del APWORK.(page5)
		4	2013/10/19 Swap DDR so-ddim pin for layout request.(page14,15)
	1A-7	1	2013/10/22 change CN24 pin define based on spec.(page31)
		2	2013/10/22 change CN25 pin define for spec.(page31)
		3	2013/10/22 Change CN4 to 6pin.(page23)
		4	2013/10/22 change Y5004 to +/-10PPM(page23)
		5	2013/10/21 add R5331 between 3V_GFX and 3V_MIN for not GC6 support.(page20)
		6	2013/10/22 change PJ1 Pin define same as ZQN.(page33)
		7	2013/10/22 Change LGND to GND.(page28)
		8	2013/10/22 CN5006 pin9/10 add R5332/r5333 for ESD protect.(page28)
		9	2013/10/22 Change CN5009\CN5013\Y7 footprint.
	1A-8	1	2013/10/22 change CN24 pin define based on spec based on ZRQ.(page31)
		2	2013/10/23 change CN25 footprint.(page31)
		3	2013/10/23 Change DIMM1_SA0/SA1 to DIMM0_SA0/SA1.(page14)
		4	20131022 Change GPIO83/84 GPU GC6 pin to GPIO2/3.(page10)
		5	2013/10/21 Swap PEG to nomroal mode.(page9)
		6	2013/10/23 remove R5017 5V is duplicater.(page27).
		7	2013/10/23 remove C5056 is duplicater.(page27)
		8	2013/10/23 change CN5008\CN25 footprint to match DXF.
		9	2013/10/23 add screw Hole footprint.
	1A-9	1	2013/10/17 Change power LED from +3VPCU to +3V_S5.(page27)
		2	2013/10/24 add 100kohm on U5011 pin 26 with C5164 for discharge(page30)
		3	2013/10/23 add 10k for vendor suggestion.(page28)
		4	2013/10/23 add R5335 Isolate SLB9660 NC.(page23).
		5	2013/10/24 Add alert on U17.1 for CPU themal tempture.(page31).
	1A-10	1	2013/10/25 remove 1.35GFX_PDG NET.(page20)
		2	2013/10/25 remove 1.35GFX_PDG (page20)
		3	2013/10/25 remove 1.35GFX POWER(page20)
		4	2013/10/25 reserve AV2 ball to GND.(page6)
		5	20131025 reserve A5 ball to 100k PU 3VPCU.(page6)
		6	2013/10/25 modify PJ2 footprint.(page33)
		7	2013/10/25 change LED from 3pin to 4pin for acer reqeust.(page27)
	1A-11	1	2013/10/28 Change U5013.7 from +3V_S5 to +3V.(page23)
		2	2013/10/28 change LED from 4pin to 3pin and power LED to +3VPCU.(page27)
		3	2013/10/28 U5013 Pin8,15,28 left NC.(page23)
	1A-12	1	2013/10/29 Change CN21 power rail to S5,change Q42 direction and net name reseve PS2 PU to +3V.(page31)
		2	20131029 Change GPIO45 to PU S5,duble GPIO58 one is GPIO56.(page10).
		3	2013/10/28 reserve AV2 ball to TP.(page8)
		4	20131028 reserve A5 ball toTP.(page6)
		5	2013/10/29 Change CN5008 to S0 of SMbus(page26)
		6	2013/10/29 Swap U27 pin2 and pin128,add U27.68 for touch pad interrupt.(page32)
	1A-13	1	20131030 add touch pad interrupt pin on ggio83.(page10)
		2	2013/10/30 move Q42 to page02 change U24.U7 net name.(page2).
		3	2013/10/30 CN5002.6 add USB touch screen on/off pin to EC.(page24)
		4	2013/10/29 add U27.35 for touch pad on/off.(page32)

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	PART NUMBER:		DRAWING BY:		REVISON:	

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Model	Version	CHANGE LIST
ZQ0	1B-2	1 2013/12/04 change PQ24 to DFN 3x3 size.(page35) 2 2013/12/04 Change Cn14 PN and footprint.(page30). 3 2013/12/04 change LED from 3pin to 4pin..(page27) 4 2013/12/4 change cN6 to 4pin.(page23) 5 2013/12/04 change GPIO36/GPI037 to PU..(page9)
	1B-3	1 2013/12/10 change Cn20 Pin define.(page25) 2 2013/12/10 change Q3.3 from +3V to +3VPCU.(page22). 3 2013/12/10 change CN6 footprint..(page21)
	1B-4	1 2013/12/12 Remove U9 Green CLK circuit.(page21)
	1B-5	1 2013/12/17 Change CN14 pin define.(page28) 2 2013/12/17 Change R8051 to 0402 size.(page16)
	1B-6	1 2013/12/18 Change USB port USB3.0 to port0,USB2.0 to port1 and port3,Fingerprint to usb port2. 2 2013/12/17 Change R8051 to 0402 size.(page16) 3 2013/12/18 U34 pin6 reserve 0402 resistor for power noise issue.(page28)
	1B-7	1 2013/12/20 add U29 VSYNC and HSYNC by pass resistor.(page22) 2 20131220 Change +3VPCU to +3V_S5 non deep sx(page10). 3 2013/12/20 del c8521 and R8391..(page16)
	1C-1	1 2014/1/06 add 0ohm pass 1.05V_Modphy to 1.05V.(page33) 2 2014/1/06 add PR224 PU to 3V.(page33). 3 2014/1/06 Change R351\R388 from 47ohm to 65ohm base on FAE request..(page28) 4 2014/01/10 Remove U29 and add U40 and U41..(page22)
	1C-2	1 2014/01/13 Change TP power rail from +3V_S5 to +3V_SUS.(page29) 2 20140113 PU6\PU12 change footprint for SMT request.(page35). 3 2014/01/13 change CN14 sata net name and add C678~C681.(page25) 4 2014/01/13 add R678\R677 PU and R679 PD for ICT..(page19) 5 2014/01/131/13 Adding +3V_SUS power for touch pad (acer request).(page32)
	1C-3	1 2014/01/14 change R654 to 0ohm.(page27) 2 2014/01/14 Change Cn11 Footprint.(page24).
	1C-4	1 2014/01/15 reserve TP power rail +3V_S5..(page29) 2 2014/01/15 TPM CO-lay nuvoton(page21). 3 2014/01/15 SWAP PCIE LAN TX single.(page26).
	1C1-1	1 2014/03/01 change PR193 to 9.3K for +1.35V.(page38) 2 2014/02/17 Add U11.98 GPIO5 for PTP power en function.(page30). 3 2014/02/17 Add Q47 for PTP power EN and soft start R694\C713 and C712\C686.(page29) 4 2014/02/06 change Blue LED power rail to +5VPCU and add ESD and Change LED to lite-on and R379=820,R375=680 base on test result.(page25) 5 2014/02/6 add VGA_ALERT# PU 10K for FAE request.(page19) 6 2014/02/19 add R692 for SUSPWRACK# to EC.(page07) 7 2014/03/01 Change 0ohm to short pad. 8 2014/03/01 link L29 to +3V directly(meet IVDDO vs OVDD sequence)(page 21)
	1C1-2	1 2014/03/08 add R696\R697 PU..(page30) 2 2014/03/08 ChangeU12 footprint to sot23 and add VC2\VC1 change C307 to 3528.(page27). 3 2014/03/08 Remove PCIE wake and stuff R642, un-stuff Q44..(page24) 4 2014/03/11 Add R698 for TS_EN short TP_INT,for issue debug.(page22)

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