Cedar Schematic
Beema

2014-03-05

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE SG installed

Cedar UMA 14

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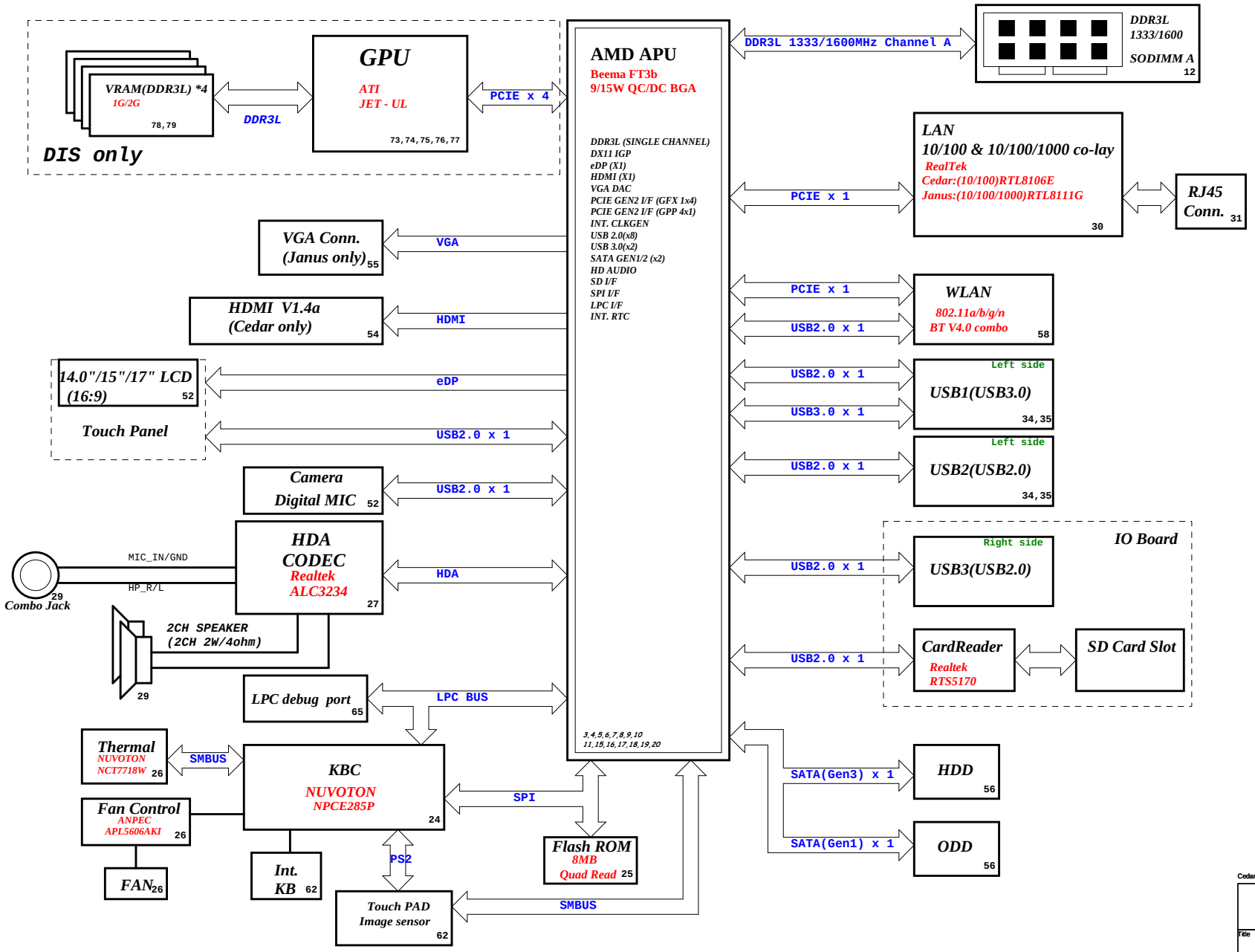
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
Size: A3	Document Number: Cedar AMD BEEMA	Rev: A00
Date: Wednesday, March 05, 2014	Sheet 1 of 104	

Cedar Block Diagram

Project code:4PD00G010001
PCB P/N: 13283-1
Revision: A00



CHARGER		
BQ24727RGRR		44
INPUTS	OUTPUTS	
AD+ BT+	DCBATOUT	

SYSTEM DC/DC		
TPS51225RUKR-GP		45
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5	

CPU Core Power		
ISL95813HRZ-GP		46,47
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	

DDR3L SUS		
TPS51716RUKR-GP		49
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3 0D65V_S0	

CPU 1.05V		
RT8237CZQW-2-GP		48
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0	

VDDIO_AZ		
TLV70215DBVR		36
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	

Switches 36 83

INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
0D95V_S5	0D95V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D35V_S3	1D35V_VGA_S0
1D8V_S5	1D8V_VGA_S0

PCB LAYER

L1:TOP
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:BOT

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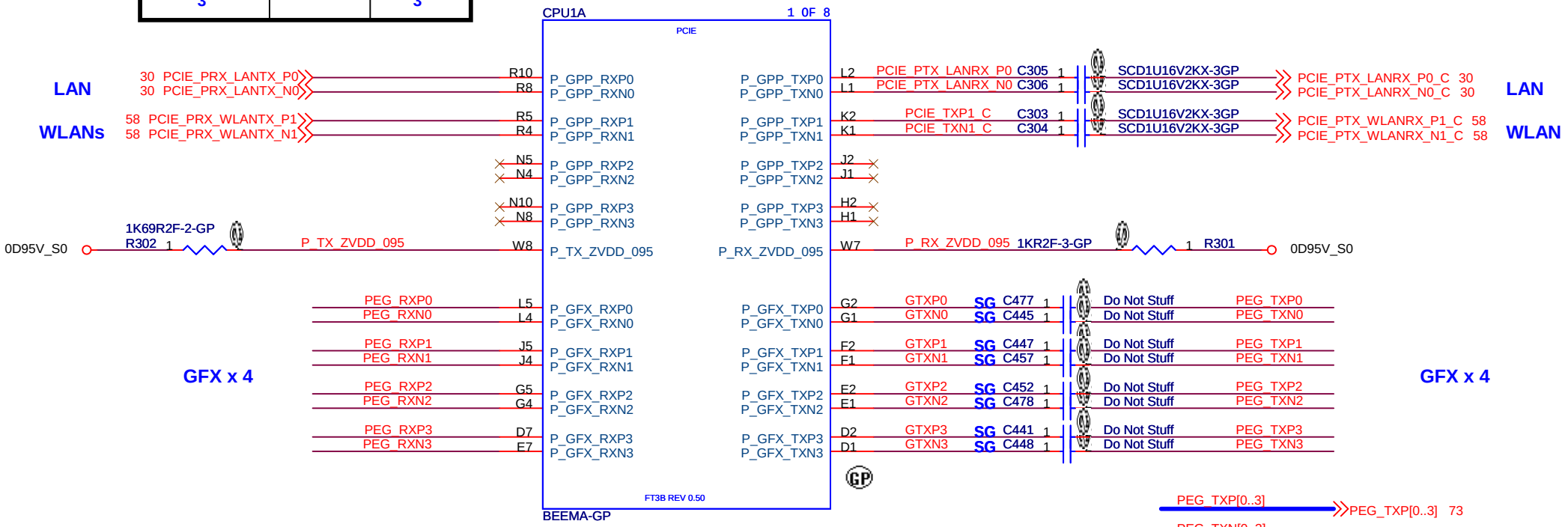
Title: Block Diagram
Size: C
Document Number: Cedar AMD BEEMA
Rev: A00
Date: Wednesday, March 05, 2014
Sheet 2 of 104

GPP CLK port	Device	CLKREQ#
0	LAN	0
1	WLAN	1
2		2
3		3



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Title: ***CPU (PCIE)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 3 of 104

Pre-PWROK METAL VID CODES

SVD	SVC	Output Voltage
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8

HDMI

eDP

SMB1

APU core Control

HDT+ Connectors

Close to APU

Follow Larne

DP_STEREOSYNC & APU_HSYNC PU FOR INTERNAL

[AMD HDMI design guidance]
Strap define PU :Enable HDMI
PD:Disable HDMI

2ND = 83.00016.F11
83.00016.K11

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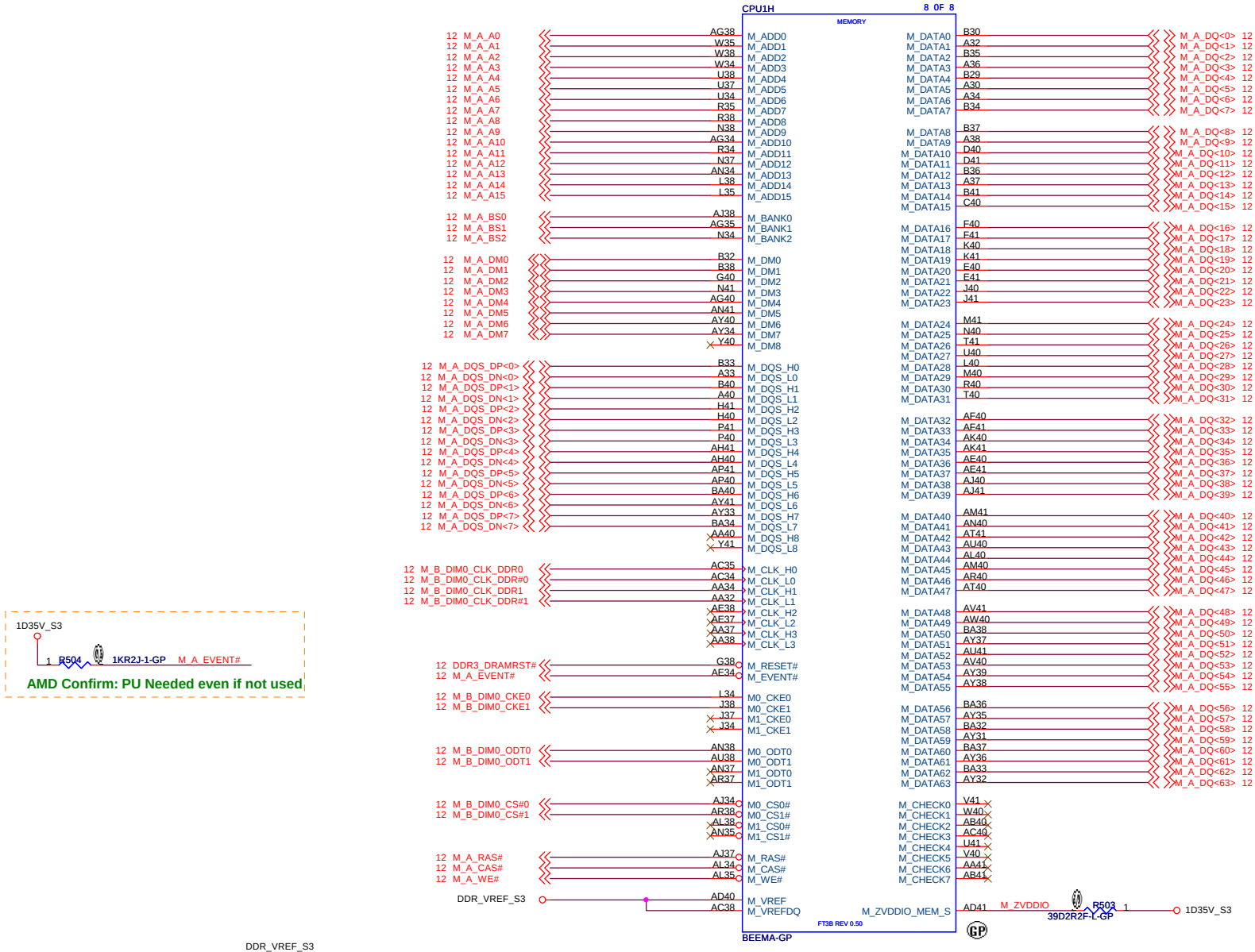
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DISPLAY/SVI2/JTAG/TES)

Size: A3 | Document Number: Cedar AMD BEEMA | Rev: A00

Date: Wednesday, March 05, 2014 | Sheet 4 of 104



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Title: **CPU (DDR)**

Size	Document Number	Rev
A3	Cedar AMD BEEMA	A00

Date: Wednesday, March 05, 2014 Sheet 5 of 104

Follow AMD Checklist

There are integrated pull-up.

R635	10KR2J-3-GP	BLUETOOTH_EN	
R603	Do Not Stuff	H_A20GATE	DY
R604	10KR2J-3-GP	KB_DET#	
R601	10KR2J-3-GP	DBC_EN	

KBC need to use OD Type

1D8V_S5		
R627	10KR2J-3-GP	S0_PWR_GOOD_R

4,30,52,58,73 PLT_RST#	R618 Do Not Stuff	PCIE_RST#_C	
	DY C601 Do Not Stuff		
24,65 LPC_RST#	R602 Do Not Stuff	LPC_RST#_C	

VRAM_SIZE1	
1	1G
0	2G

CEDAR_JANUS_ID	
1	CEDAR
0	JANUS

CPU1C — ACPI/SD/AZ/GPIO/RTC/MISC — 3 OF 8

LPC_RST# C	AY4	LPC_RST#	
PCIE_RST# C	AY9	PCIE_RST#	
PM_RSMRST# R	AY5	RSMRST#	
24 PM_PWRBTN#	BA8	PWR_BTN#	
24,36 SYS_PWRGD	AM19	PWR_GOOD	
19 SYS_RESET#	AY7	SYS_RESET#/GEVENT19#	
24,30 PCIE_WAKE#	AW11	WAKE#/GEVENT8#	
24,36,49,83 PM_SLP_S3#	AY3	SLP_S3#	
24,49 PM_SLP_S5#	BA5	SLP_S5#	
APU_TEST0	AU13	TEST0	
APU_TEST1	AY10	TEST1/TMS	
APU_TEST2	AY6	TEST2	
24 H_RCIN#	AR23	KBRST#	
24 H_A20GATE	AR31	GA20IN/GEVENT0#	
24 EC_SCI#	AN5	LPC_PME#/GEVENT3#	
24 EC_SMI#	AL7	LPC_SMI#/GEVENT23#	
24 AC_PRESENT	AP15	AC_PRES/IR_RX0/GEVENT16#	
24 EC_SW1#	AV13	IR_TX0/GEVENT21#	
25 RTC_DET#	BA9	IR_TX1/GEVENT6#	
	BA10	IR_RX1/GEVENT20#	
	AV15	IR_LED#/LLB#/GPIO184	
30 CLK_PCIE_LAN_REQ0#	AU29	CLK_REQ0#/SATA_ISI0#/SATA_ZP0#/GPIO60	
58 CLK_PCIE_WLAN_REQ1#	AW29	CLK_REQ1#/GPIO61	
	AR27	CLK_REQ2#/GPIO62	
	AV27	CLK_REQ3#/SATA_IS1#/SATA_ZP1#/GPIO63	
75 PEG_CLKREQ#	AY29	CLK_REQ0#/GPIO65/OSCIN	
35 USB_OC#0	AY8	USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#	
35 USB_OC#1	AW1	USB_OC1#/TDI/GEVENT13#	
56 SATA_ODD_PRSNT#	AV1	USB_OC2#/TCK/GEVENT14#	
35 USB_OC#3	AY1	USB_OC3_L/TDO/GEVENT15_L	
HDA_CODEC_BITCLK_R	AN2	AZ_BITCLK	
HDA_CODEC_SDOUT_R	AN1	AZ_SDOUT	
27 HDA_SDIN0	AK2	AZ_SDIN0/GPIO167	
27 HDA_CODEC_BITCLK	AK1	AZ_SDIN1/GPIO168	
27 HDA_CODEC_SDOUT	AM1	AZ_SDIN2/GPIO169	
27 HDA_CODEC_SYNC	AL2	AZ_SDIN3/GPIO170	
27,29 HDA_CODEC_RST#	AM2	AZ_SYNC	
	AL1	AZ_RST#	
32K_X1	AJ2	X32K_X1	
32K_X2	AJ1	X32K_X2	
		FT3B REV 0.50	

BEEMA-GP

	SD_PWR_CTRL	BA23	
	SD_CLK/GPIO73	AY22	
	SD_CMD/GPIO74	AY23	
	SD_CD/GPIO75	AY20	
	SD_WP/GPIO76	BA20	
VRAM_SIZE1	SD_DATA0/GPIO77	BA22	
CEDAR_JANUS_ID	SD_DATA1/GPIO78	AY21	
	SD_DATA2/GPIO79	AY24	
	SD_DATA3/GPIO80	BA24	
	SD_LED/GPIO45	AY25	
SMB0_CLK 12	SCL0/GPIO43	AU25	
SMB0_DATA 12	SDA0/GPIO47	AV25	
SMB1_CLK 62	SCL1/GPIO227	AY11	
SMB1_DATA 62	SDA1/GPIO228	BA11	
BLUETOOTH_EN 58	GPIO49	AP27	
DBC_EN 52	GPIO50	AY28	
KB_DET# 62	GPIO51	BA28	
	DEVSLP0/GPIO55	AY23	
	GPIO57	AP21	
DGPU_PRESENT#	GPIO58	BA26	
	DEVSLP1/GPIO59	AV19	
	GPIO64	AY27	
HDA_SPKR 27	SPKR/GPIO66	BA27	
	GPIO68	AU21	
PANEL_SIZE_ID 52	GPIO69	AY26	
KB_LED_BL_DET 62	GPIO70	AY21	
GPIO71	GPIO71	AM21	
MEM_1V5	GPIO174	BA3	
SPI_SW 19	GEVENT2#	AV17	
GEVENT4#	GEVENT4#	BA4	
GEVENT7#	GEVENT7#	AR15	
	GEVENT10#	AP17	
	GEVENT11#	AP11	
SATA_ODD_DA# 56	GEVENT17#	AN8	
BLINK 19	BLINK/GEVENT18#	AU17	
	GEVENT22#	BA6	
DGPU_PWROK_R	GENINT1#/GPIO32	BA29	
	GENINT2#/GPIO33	AP23	
SATA_ODD_PWRGT 56	FANOUT0/GPIO52	AV31	
	FANIN0/GPIO56	AU31	
PCH_SUSCLK_KBC 24	RTCCLK	AV11	
RTC_CLK 19			

SODIMM

TP

R638 Do Not Stuff	VRAM_1G	R639 10KR2J-3-GP	CEDAR
R641 Do Not Stuff	VRAM_2G	R640 Do Not Stuff	JANUS

R637	DY	Do Not Stuff	
R636	DY	Do Not Stuff	
PE_GPIO0	73		
PE_GPIO1	82,83		

PX support
PE_GPIO0: VGA_RESET
PE_GPIO1: VGA_PowerEnable

R631	Do Not Stuff	DGPU_PWROK	24,82,83
C605	DY	Do Not Stuff	

R609	Do Not Stuff	PCH_SUSCLK_KBC	24
		RTC_CLK	19

3D3V_S5

R630	10KR2J-3-GP	PM_PWRBTN# R	
R634	10KR2J-3-GP	RTC_DET#	
R617	10KR2J-3-GP	AC_PRESENT	
R626	100KR2J-1-GP	PCIE_WAKE# R	

X02 0206

RN604		USB_OC#1	
		USB_OC#3	
		USB_OC#0	
SRN10KJ-6-GP			
R608	DY Do Not Stuff	EC_SWI#	

R629	100KR2J-1-GP	PM_RSMRST#	
R633	DY Do Not Stuff	HDA_SDIN0	
R607	DY Do Not Stuff	PE_GPIO0	
R620	10KR2J-3-GP	GEVENT4#	
R621	10KR2J-3-GP	GEVENT7#	
R647	15KR2J-1-GP	APU_TEST0	
R646	15KR2J-1-GP	APU_TEST1	
R645	15KR2J-1-GP	APU_TEST2	
R632	10KR2J-3-GP	GPIO71	
R644	10KR2J-3-GP	MEM_1V5	

X02 0127

C603	SC8P50V2DN-1GP	32K_X1	
X601	XTAL-32D768KHZ-17-GP		
R623	20MR3-GP		
C604	SC10P50V2JN-4GP	32K_X2	

AMD suggests Xtal ESR must be less than 65R

	XTAL	CLK, Hz
0	System & USB	48M
1	RTC	32.768K
2	LAN	25M
3	VGA	27M

R612	Do Not Stuff	HDA_CODEC_SYNC_R	
R613	Do Not Stuff	HDA_CODEC_RST#_R	
R614	Do Not Stuff		

33R2J-2-GP R616

Report APU
H=UMA L=DISCRETE

UMA	R642	100KR2J-1-GP	
DGPU_PRESENT#			
SG	R643	Do Not Stuff	

RN601		SMB0_CLK	
		SMB0_DATA	
SRN2KJ-1-GP			
RN603		SMB1_CLK	
		SMB1_DATA	
SRN10KJ-5-GP			

RN602	SRN100KJ-6-GP		
Q601	2N7002KDW-GP		
R628	1KR2J-1-GP	PM_RSMRST#	
		RSMRST#_KBC	24
		3V_5V_POK	45,50
		51123_PGOOD	

R649	10KR2J-3-GP	PM_RSMRST#_R	
Q603	2N7002KDW-GP	PM_RSMRST#	
R648	100KR2J-1-GP	Q603_2	

Cedar UMA 14

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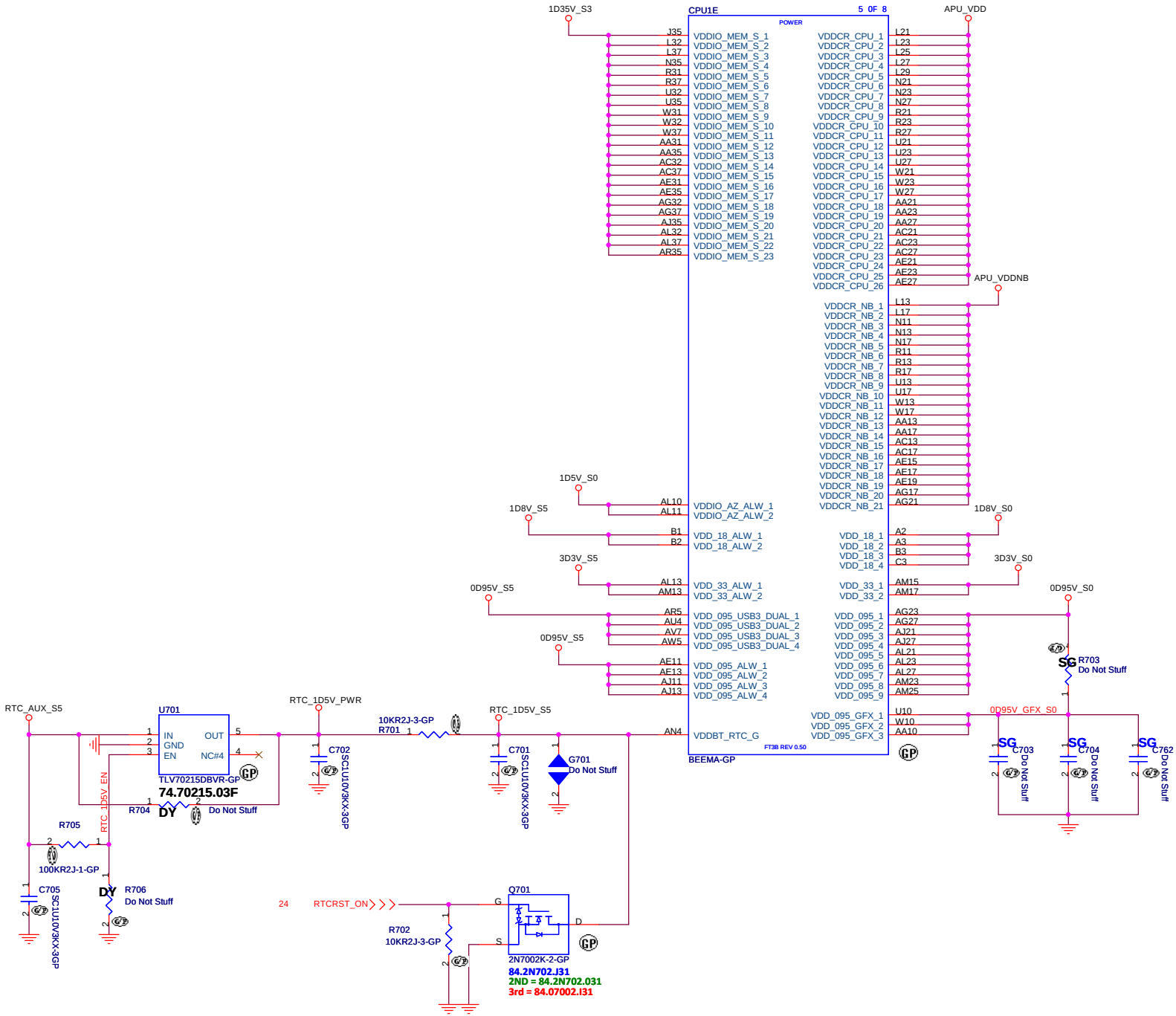
Title: CPU (ACPI/SD/AZ/GPIO/RTC)

Size: Custom | Document Number: Cedar AMD BEEMA | Rev: A00

Date: Wednesday, March 05, 2014 | Sheet 6 of 104



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***007_CPU (VCC_CORE)***	
Size A3	Document Number **Cedar AMD BEEMA**	Rev **A00**
Date: Wednesday, March 05, 2014	Sheet 7 of 104	

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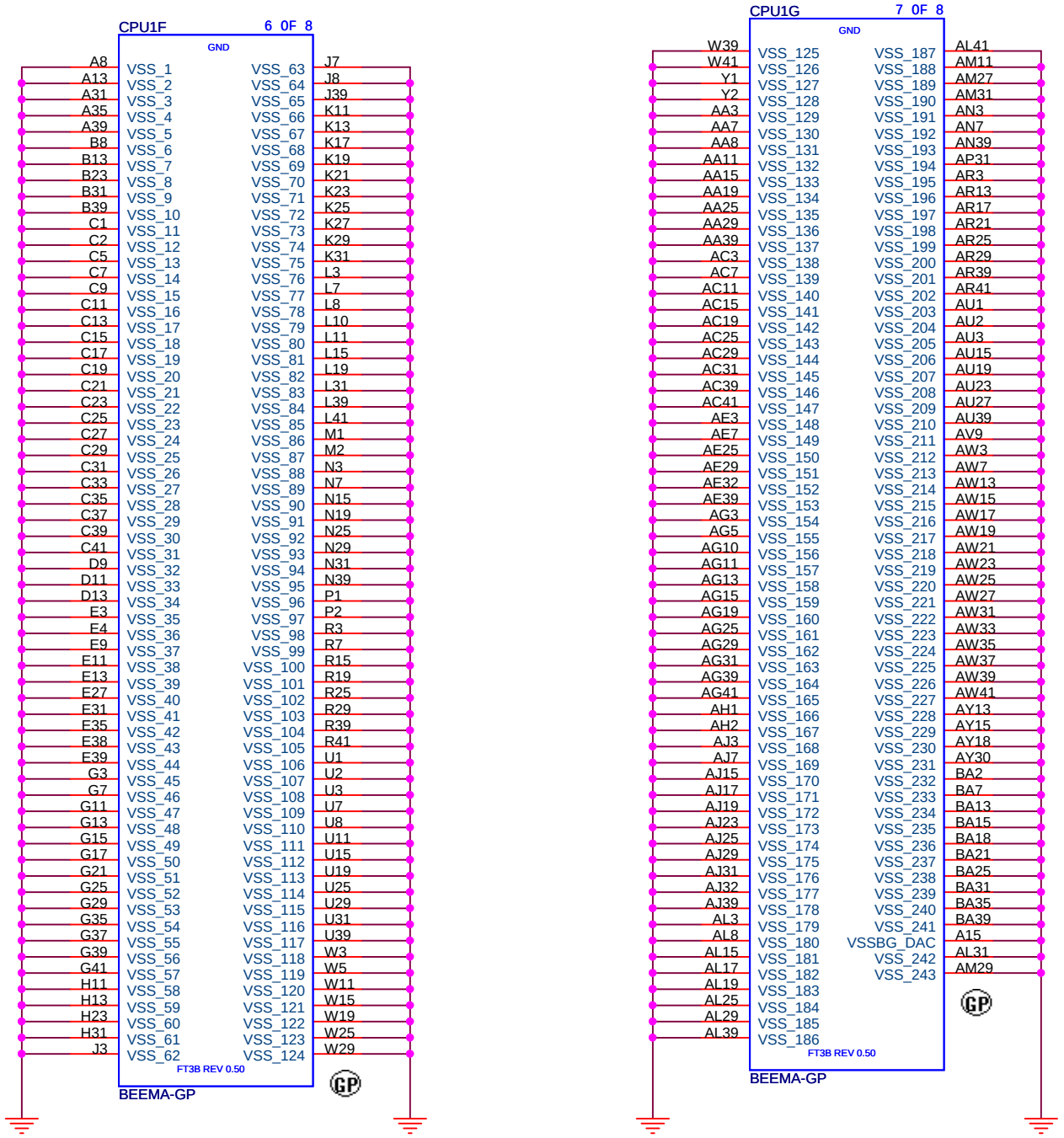
Title: ***Reserved***

Size	Document Number	Rev
A3	Cedar AMD BEEMA	A00

Date: Wednesday, March 05, 2014 Sheet 8 of 104



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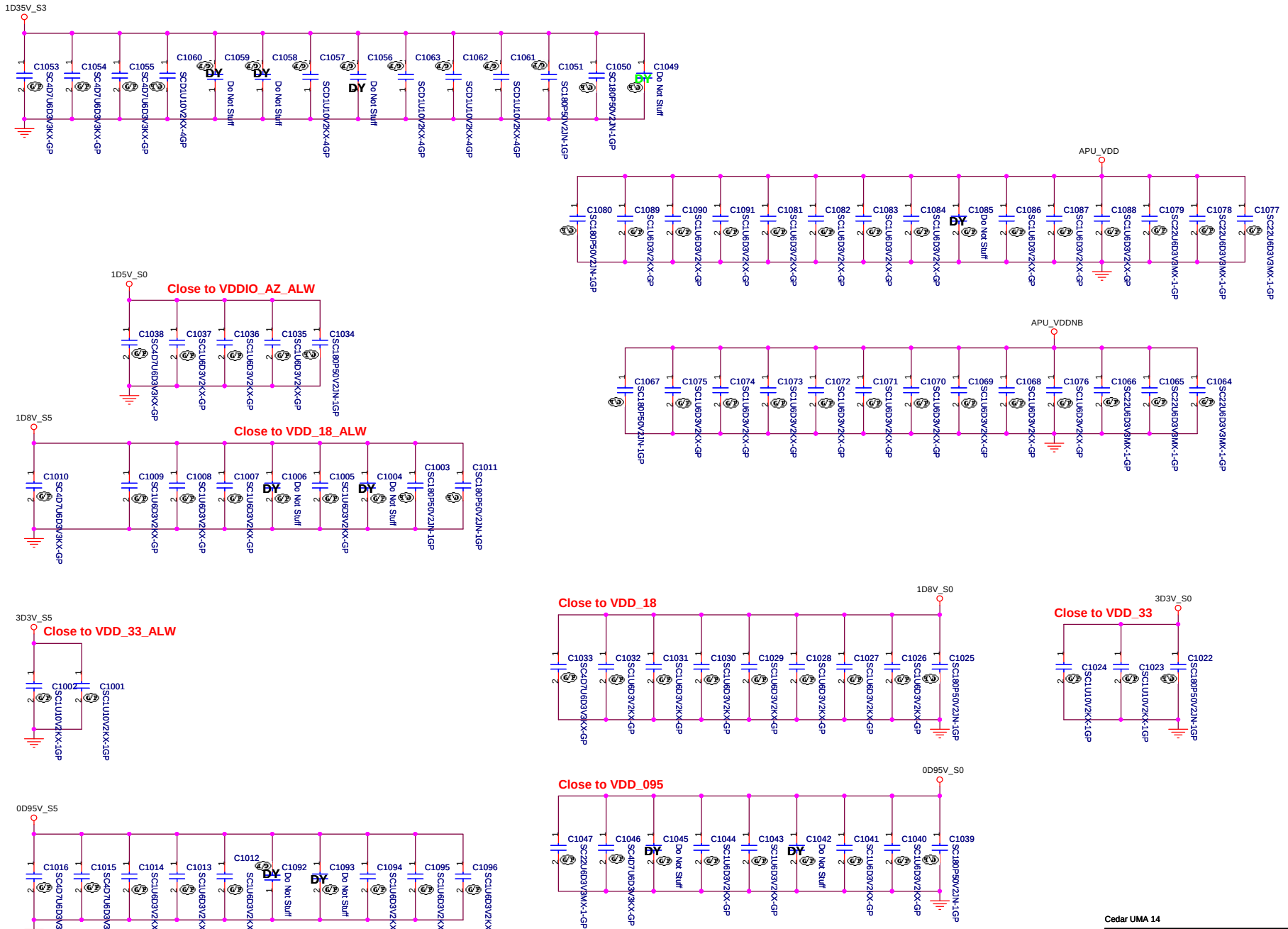
Title

CPU (VSS)

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	A00

Date: Wednesday, March 05, 2014 Sheet 9 of 104



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A3	Cedar AMD BEEMA	A00

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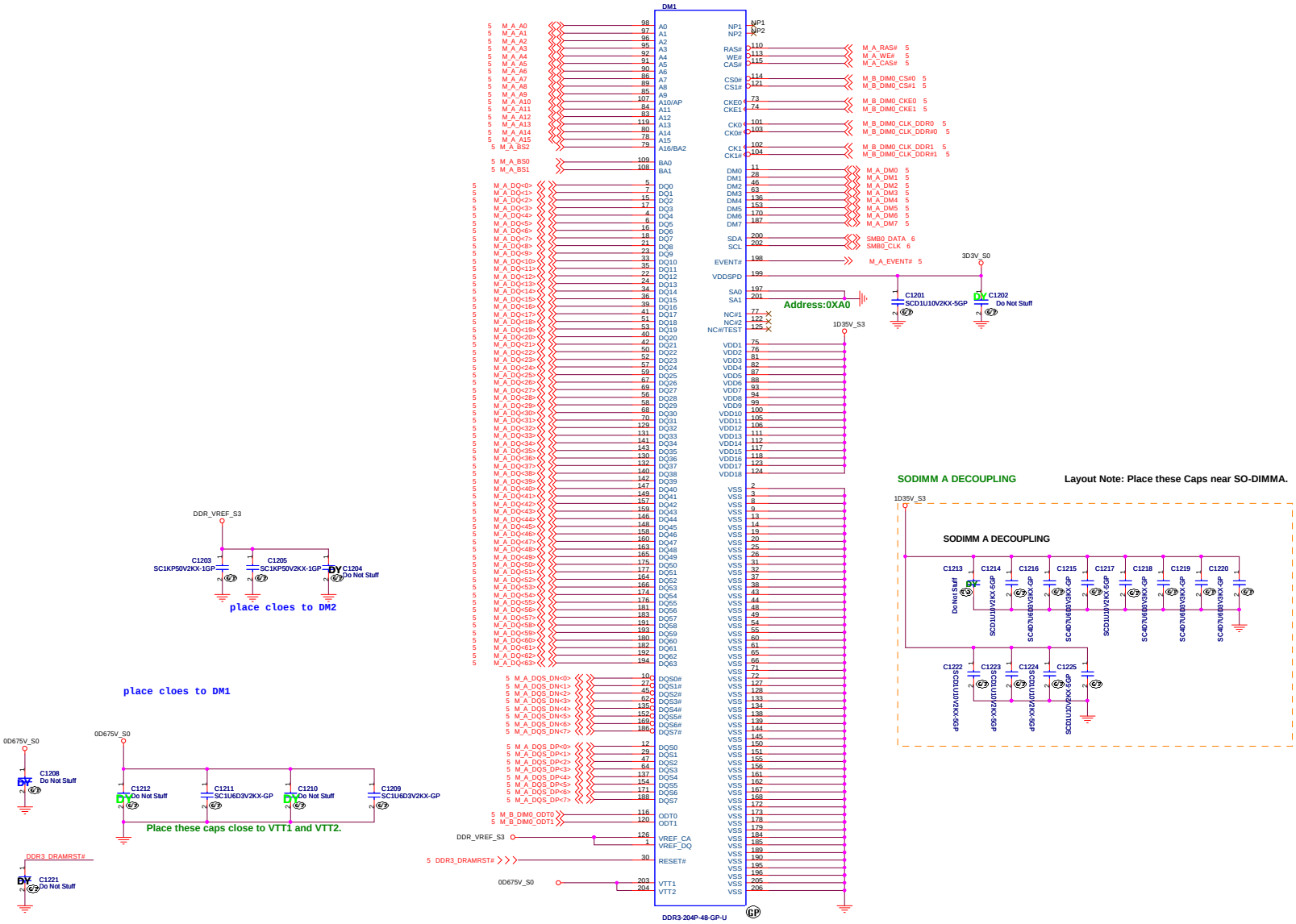
SSID = MEMORY



62.10017.P41

Cedar UMA 14

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Title: *DDR3-SODIMM1*		
Size: A2	Document Number: Cedar AMD BEEMA	Rev: A00
Date: Wednesday, March 05, 2014	Sheet 12 of 104	

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Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	A00

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Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

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A4	**Cedar AMD BEEMA**	**A00**

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A4	**Cedar AMD BEEMA**	**A00**

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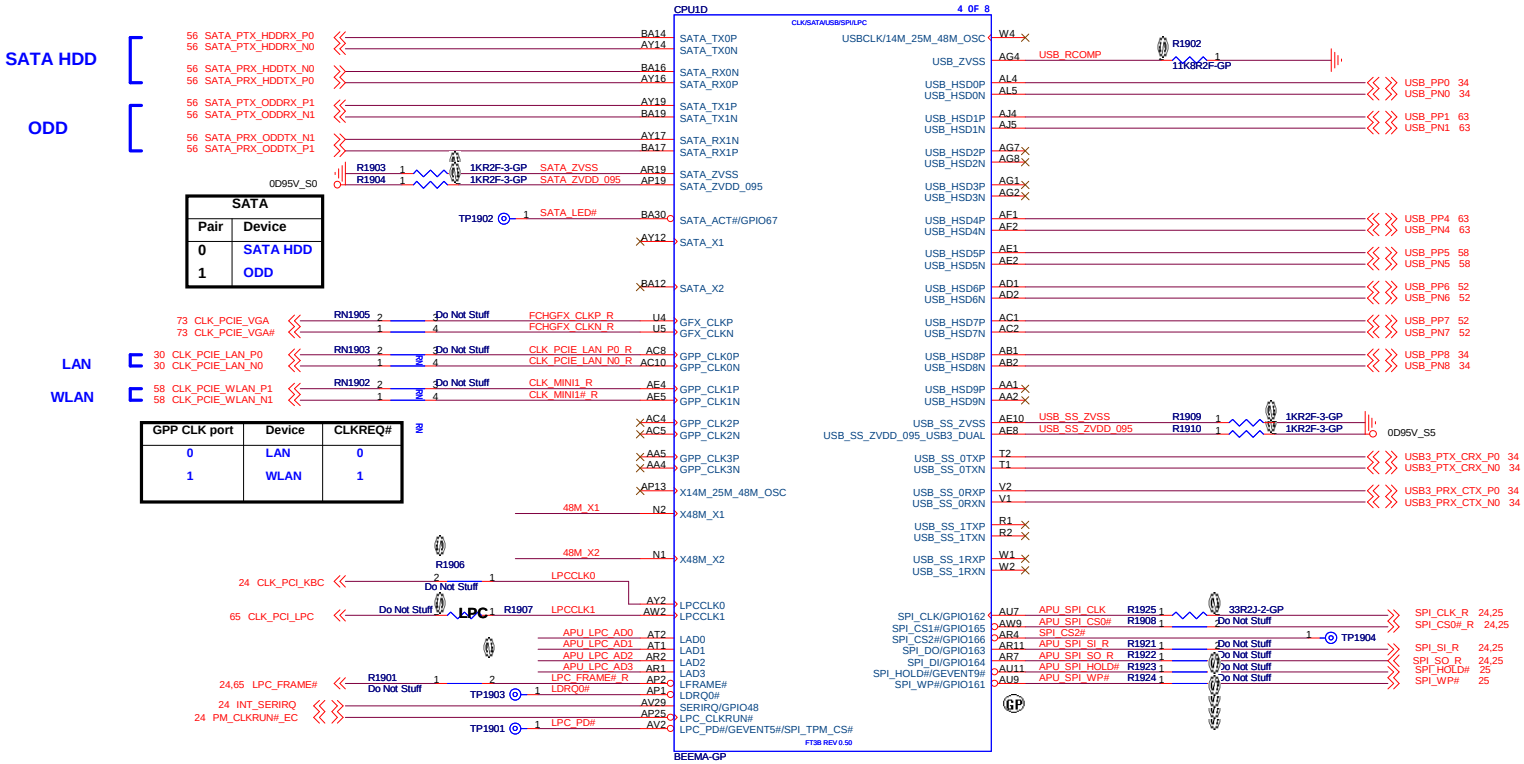
A4	**Cedar AMD BEEMA**	**A00**

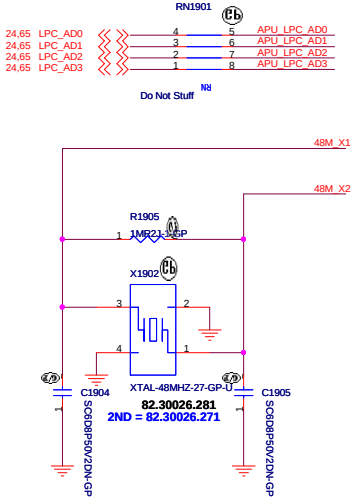
Date: Wednesday, March 05, 2014 Sheet 18 of 104



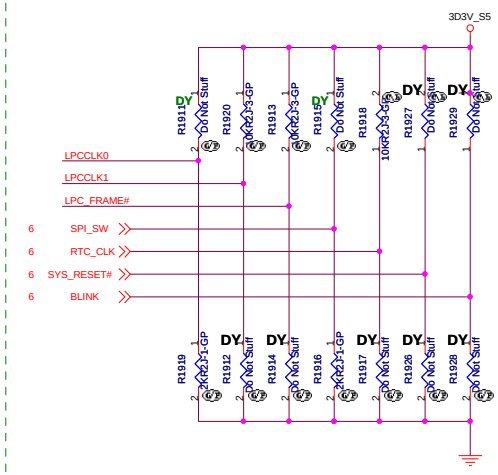
USB Table

Pair	Device
0	USB2.0 PORT1 Debug
1	USB2.0 PORT3 (DB Conn)
2	
3	NA
4	Card Reader
5	WLAN + BT (Mini PCI-E)
6	Touch Panel
7	CCD (CCD Conn)
0/8	USB3.0 & USB 2.0 (MB port2)
1/9	

	XTAL	CLK, Hz
0	System & USB	48M
1	RTC	32.768K
2	LAN	25M
3	VGA	27M

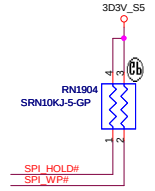


SYSTEM STRAPPINGS



REQUIRED SYSTEM STRAPS

	LPC_CLK0	LPC_CLK1	LPC_FRAME#	SPI_SELECT	RTC_CLK	SYS_RESET#	BLINK
PULL HIGH	Boot Fail Timer Enabled	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM DEFAULT	Coin Battery DEFAULT	NORMAL POWR UP /RESET TIMING DEFAULT	PWROK and RST_L pin routed to APU DEFAULT
PULL LOW	Boot Fail Timer Disabled DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM	Direct DC	Reserved	Reserved



Cedar UMA 14

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CLK/SATA/USB/SPI/LPC)

Size: Custom | Document Number: Cedar AMD BEEMA | Rev: A00

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Title: ***Reserved***

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A4	**Cedar AMD BEEMA**	**A00**

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Title: ***Reserved***

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Title: ***Reserved***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 22 of 104

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Title: ***Reserved***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 23 of 104

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

TBD

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Jamus_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
TBD	100.0K	13.7K(64.13725.6DL)	2.902V
TBD	100.0K	17.8K(64.17825.6DL)	2.801V
TBD	100.0K	22.1K(64.22125.6DL)	2.702V
Cedar_UMA	100.0K	27.0K(64.27025.6DL)	2.598V
TBD	100.0K	32.4K(64.32425.6DL)	2.492V
TBD	100.0K	37.4K(64.37425.6DL)	2.402V
Jamus_DIS	100.0K	43.2K(64.43225.6DL)	2.304V
TBD	100.0K	49.9K(64.49925.6DL)	2.201V
TBD	100.0K	57.6K(64.57625.6DL)	2.093V
Cedar_DIS	100.0K	64.9K(64.64925.6DL)	2.001V
TBD	100.0K	73.2K(64.73225.6DL)	1.905V
TBD	100.0K	82.5K(64.82525.6DL)	1.808V
TBD	100.0K	93.1K(64.93125.6DL)	1.709V
TBD	100.0K	107K(64.10735.6DL)	1.584V
TBD	100.0K	120K(64.12035.6DL)	1.499V
TBD	100.0K	137K(64.13735.6DL)	1.392V
TBD	100.0K	154K(64.15435.6DL)	1.299V
TBD	100.0K	200K(64.20035.6DL)	1.099V
TBD	100.0K	232K(64.23236.6DL)	0.994V

Don't PD
ALL_SYS_PWRGD assert,
delay 10ms; SYS_PWRGD assert.

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Connect GND and AGND planes via either
0R resistor or connect directly.

Do Not Stuff
2nd = 83.R2004.C8F

Power Switch Logic(PSL)

EC_GPIO47 Low Active

071.00285.000G

Cedar UMA 14

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

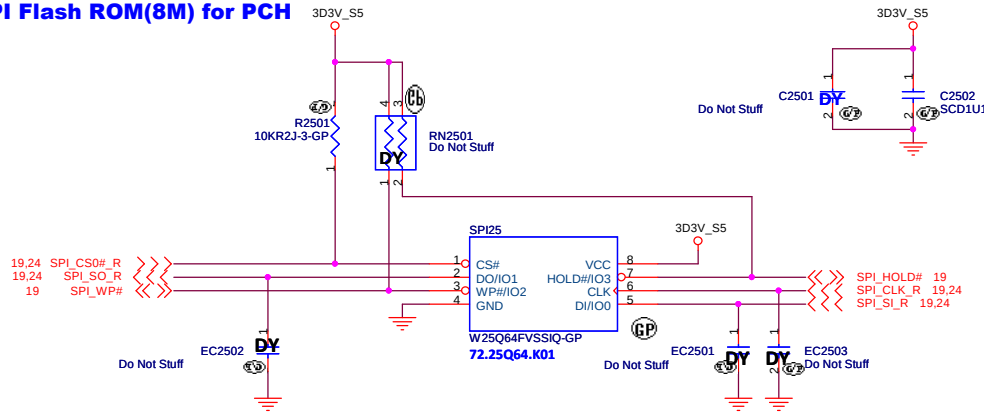
Title: KBC Nuvoton NPCE885

Size: Custom | Document Number: Cedar AMD BEEMA | Rev: A00

Date: Wednesday, March 05, 2014 | Sheet 24 of 104

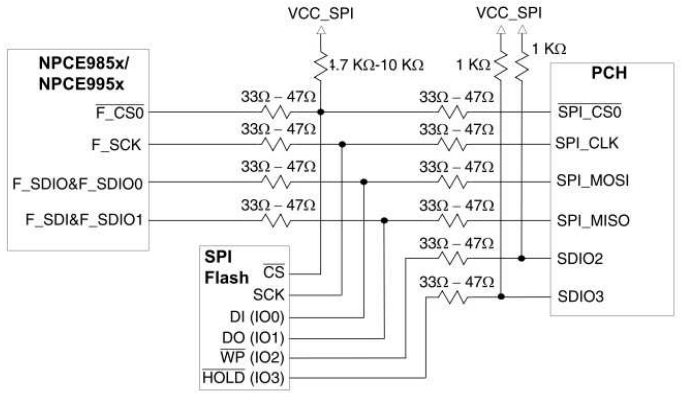
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



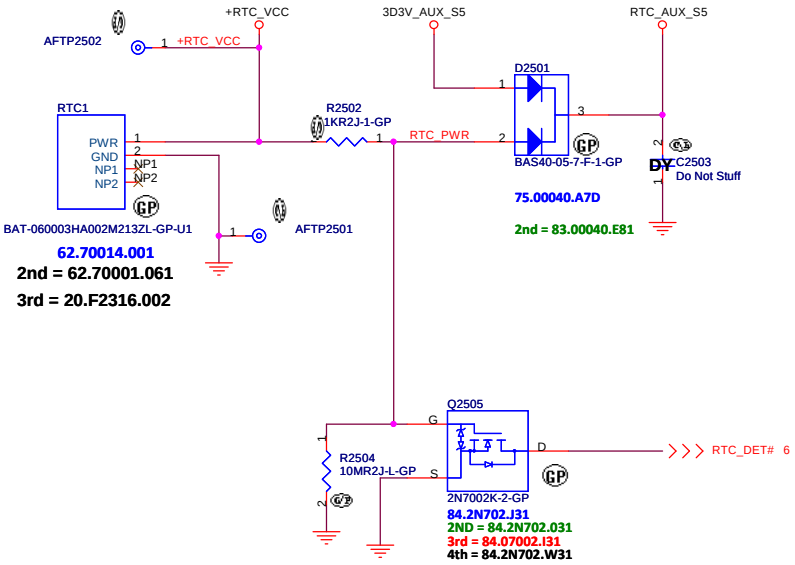
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT



Cedar UMA 14

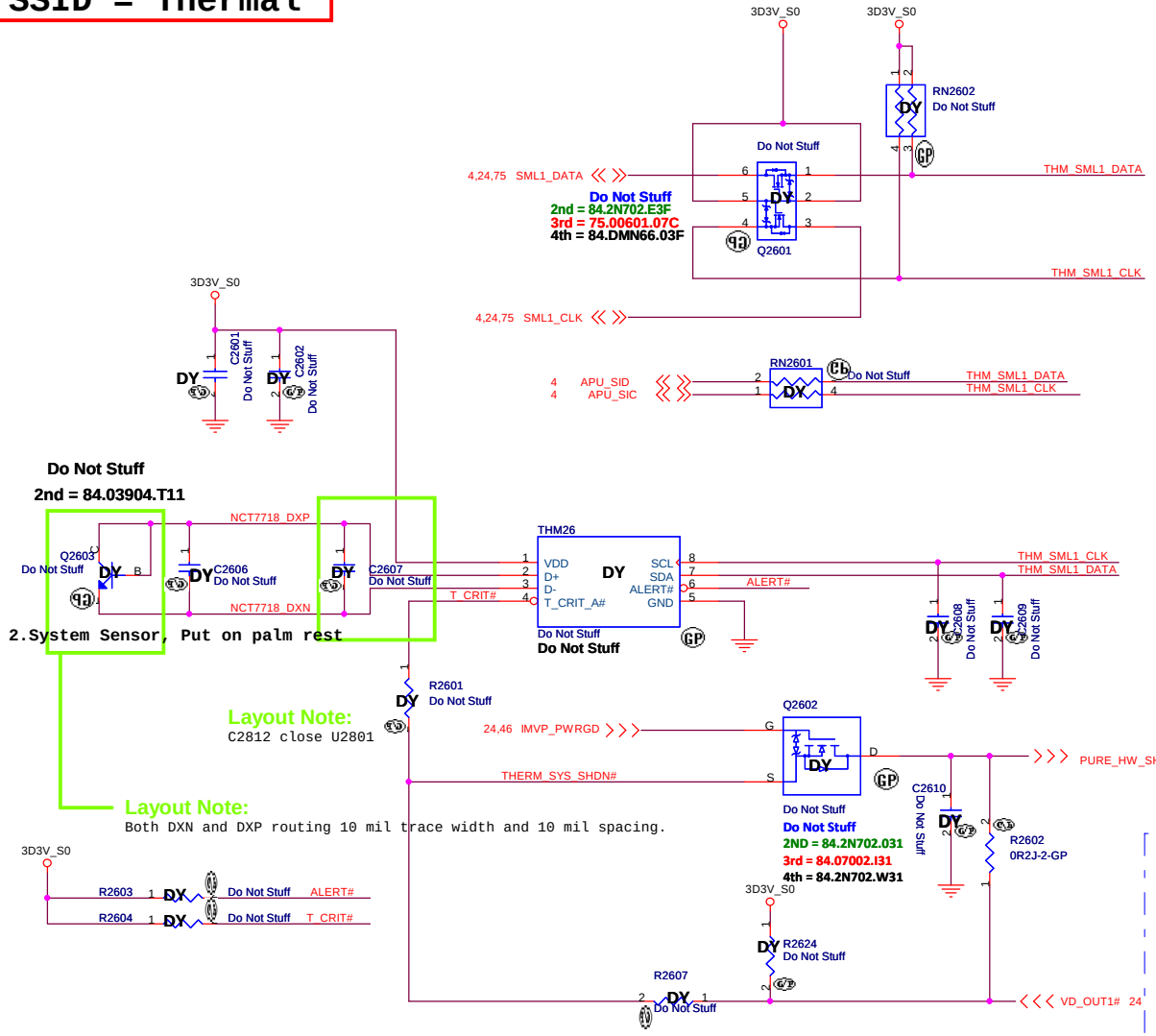
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Flash/RTC**

Size	Document Number	Rev
A3	Cedar AMD BEEMA	A00

Date: Wednesday, March 05, 2014 Sheet 25 of 104

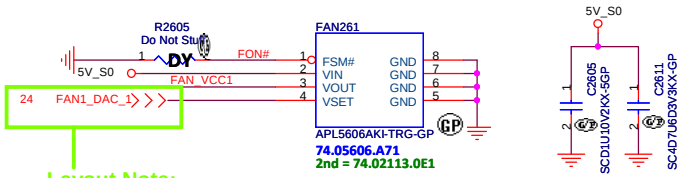
SSID = Thermal



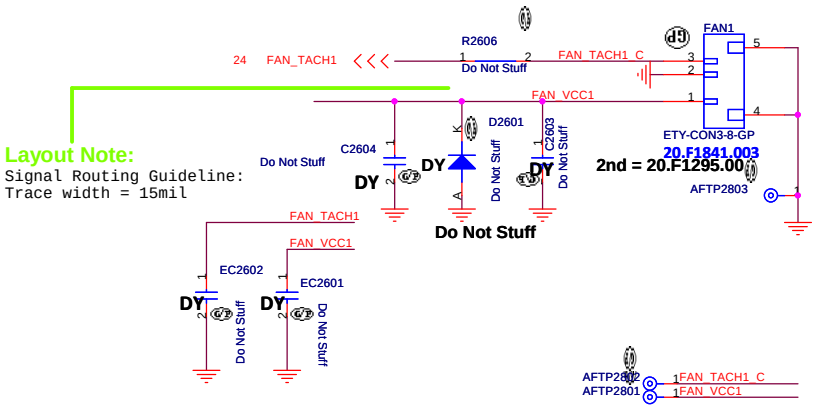
Layout Note:
C2812 close U2801

Layout Note:
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Fan controller1

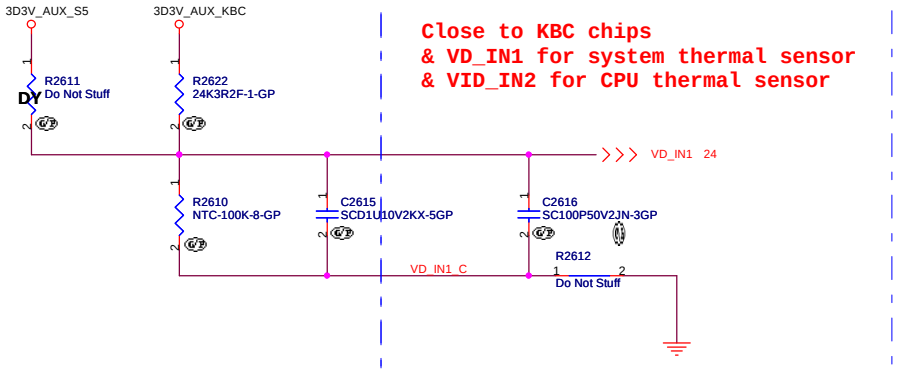


Layout Note:
Need 10 mil trace width.



Layout Note:
Signal Routing Guideline:
Trace width = 15mil

Close to Thermal sensor



Close to KBC chips
& VD_IN1 for system thermal sensor
& VID_IN2 for CPU thermal sensor

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Cedar UMA 14

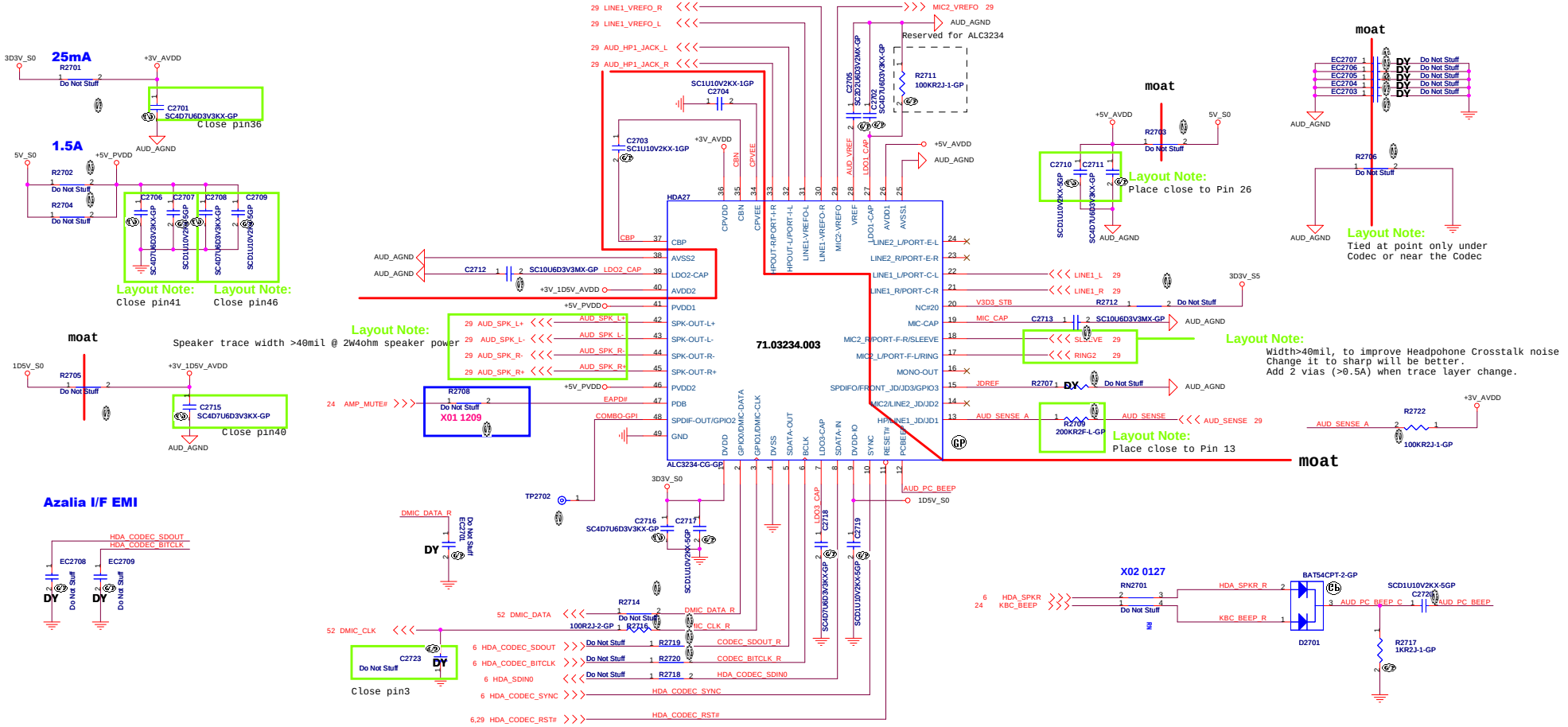
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size: A3 | Document Number: Cedar AMD BEEMA | Rev: A00

Date: Wednesday, March 05, 2014 | Sheet 26 of 104

SSID = AUDIO



Cedar UMA 14

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3223

Size: Custom | Document Number: Cedar AMD BEEMA | Rev: A00

Date: Wednesday, March 05, 2014 | Sheet 27 of 104

(Blanking)

Cedar UMA 14

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

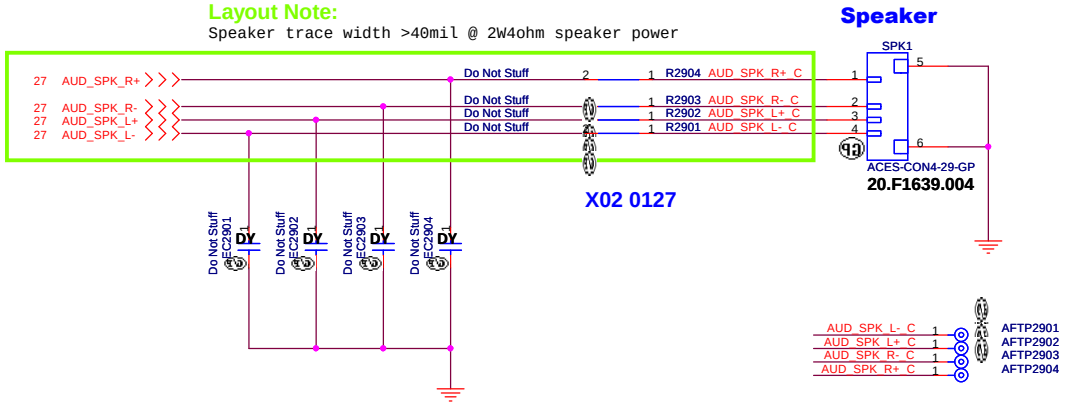
Title: ***Reserved***

Size	Document Number	Rev
A4	***Cedar AMD BEEMA***	***A00***

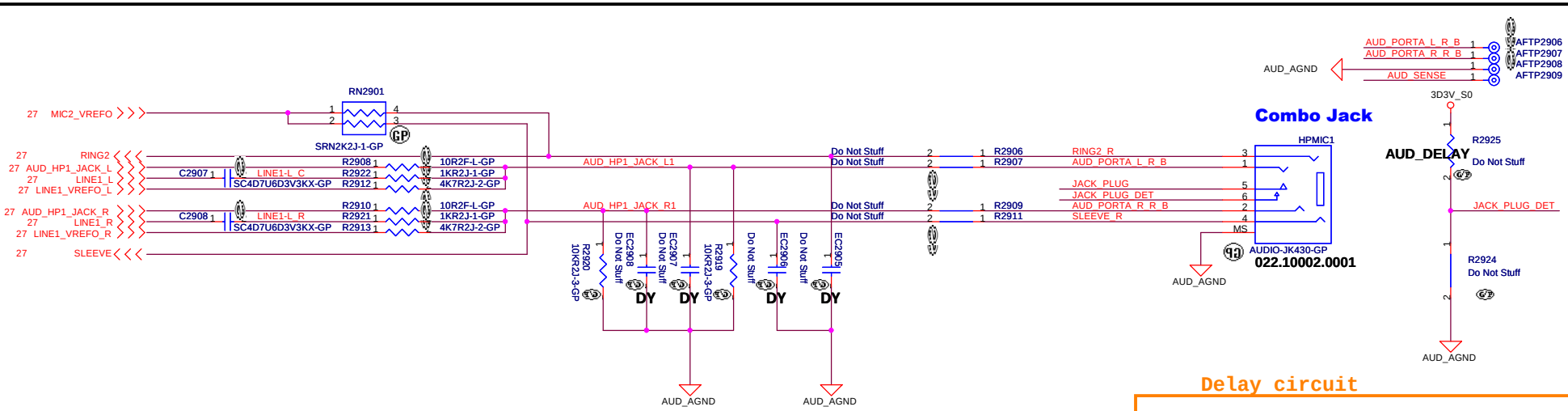
Date: Wednesday, March 05, 2014 Sheet 28 of 104

SSID = AUDIO

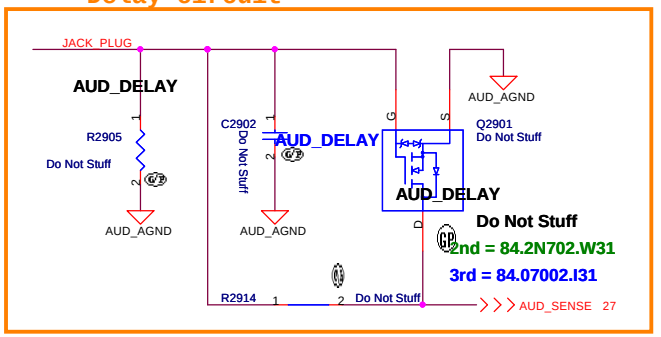
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

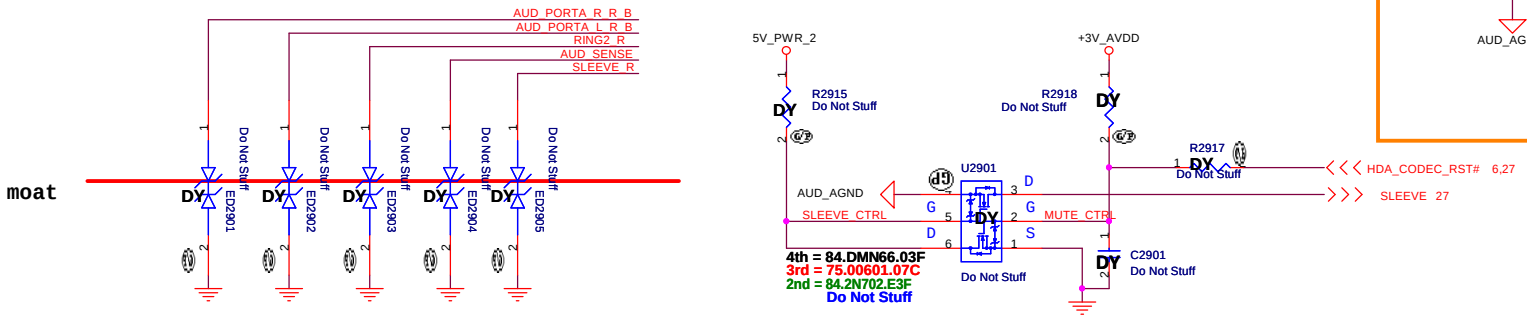


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L_



Delay circuit





Cedar UMA 14

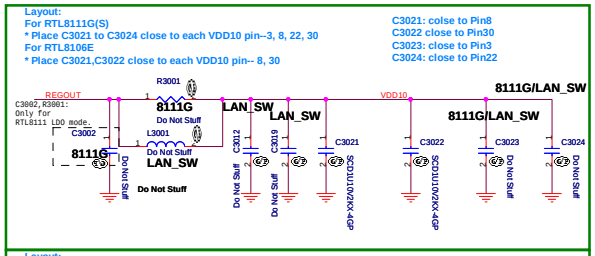
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

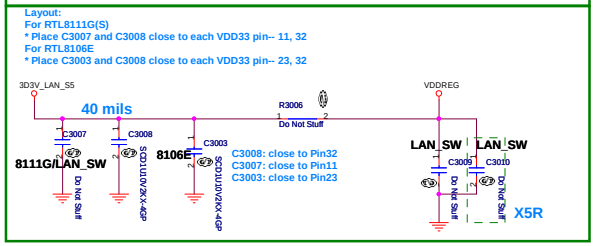
Title: Thermal NCT7718W/Fan Controllor P2793

Size: A3 | Document Number: Cedar AMD BEEMA | Rev: A00

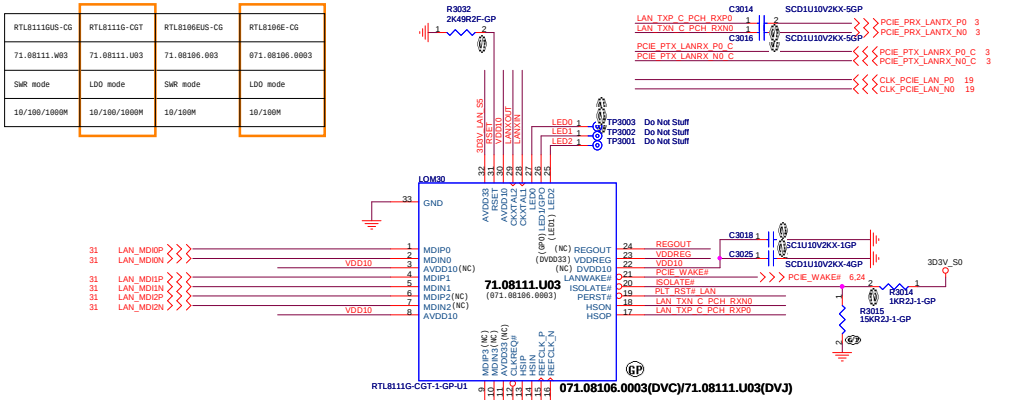
Date: Wednesday, March 05, 2014 | Sheet 29 of 104

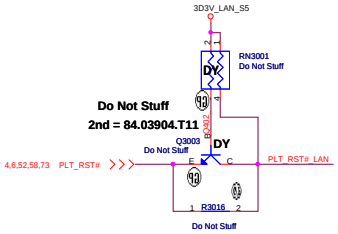
LAN CHIP (10/100/1000M & 10/100M co-lay)

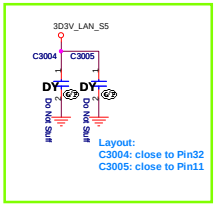




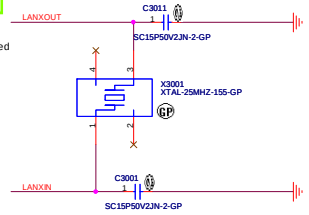
RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CG
71.08111.W03	71.08111.U03	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

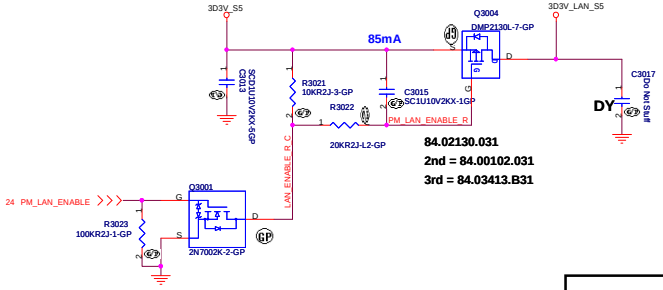


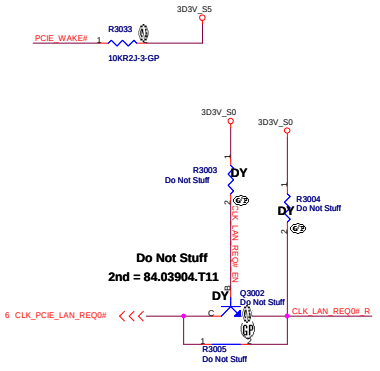




3D3V_LAN_S5 rise time must be controlled between 0.5 mS and 100 mS.







	1.0V Source	R3001	C3002	C3023	C3024	C3007	L3001	C3012	C3019	C3009	C3010	C3003
RTL8111G-CGT (71.08111.U03)	LDO	0	0	0	0	0	X	X	X	X	X	X
RTL8111GUS-CG (71.08111.W03)/ RTL8106EUS-CG (71.08106.003)	SWR	X	X	0	0	0	0	0	0	0	0	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	X	X	X	X	X	0

Cedar UMA 14

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8111/RTL8106

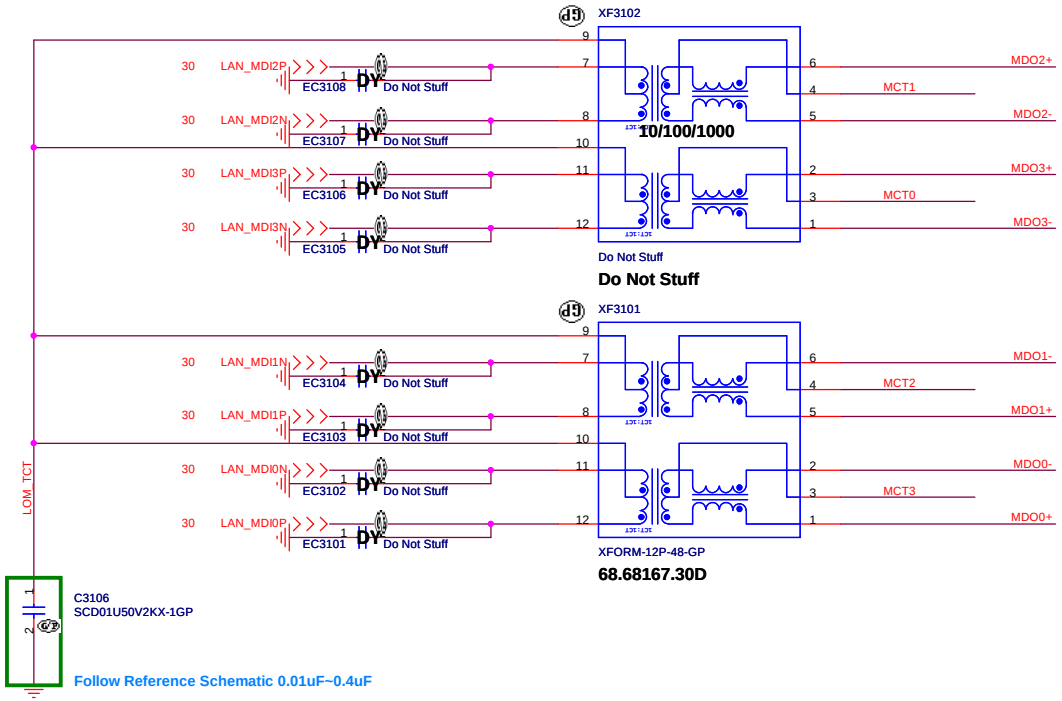
Size: A2 | Document Number: Cedar AMD BEEMA | Rev: A00

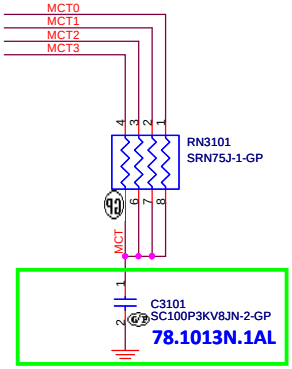
Date: Wednesday, March 05, 2014 | Sheet 30 of 104

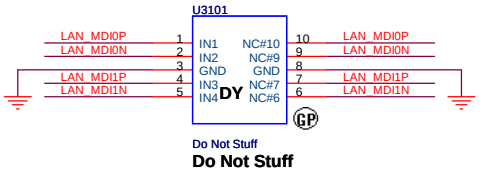
SSID = LOM

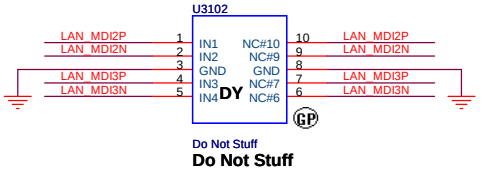
LAN TransFormer (10/100/1000M & 10/100M co-lay)

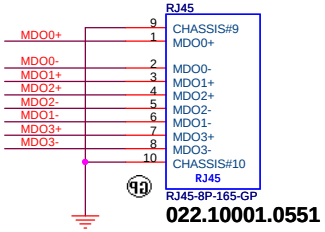
Layout note:
30 mil spacing between MDI differential pairs.



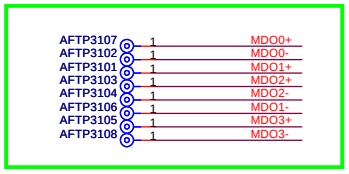








Layout:
Place near RJ45



Cedar UMA 14

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	XFOM&RJ45	
Size: A3	Document Number: Cedar AMD BEEMA	Rev: A00
Date: Wednesday, March 05, 2014	Sheet 31 of 104	

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Cedar UMA 14

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)Card Reader***

Size	Document Number	Rev
A4	***Cedar AMD BEEMA***	***A00***

Date: Wednesday, March 05, 2014 Sheet 32 of 104

(Blanking)

Cedar UMA 14

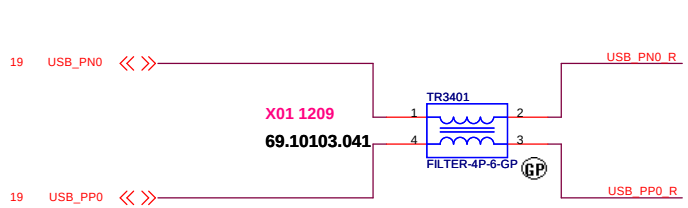
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

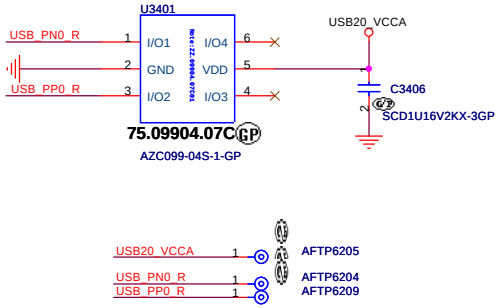
Title: *(Reserved)*

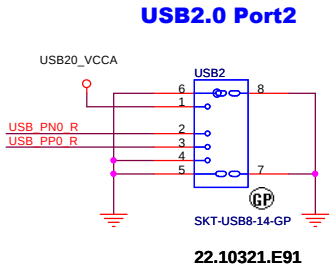
Size	Document Number	Rev
A4	*Cedar AMD BEEMA*	*A00*

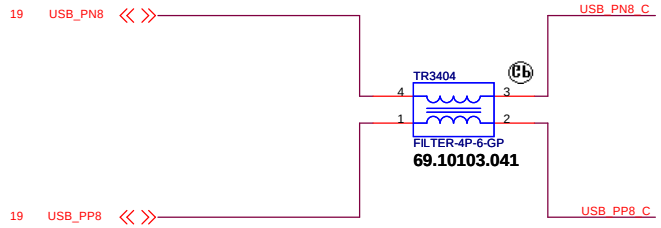
Date: Wednesday, March 05, 2014 Sheet 33 of 104

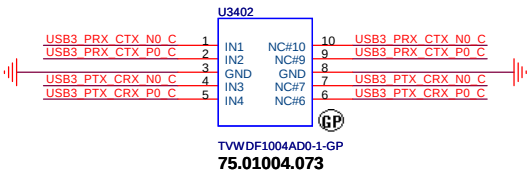
SSID = USB

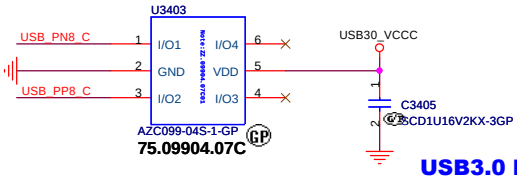


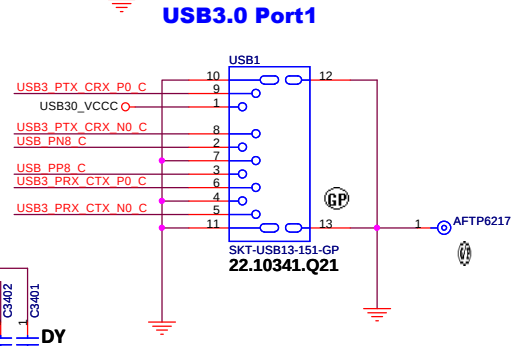


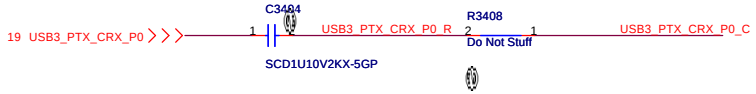


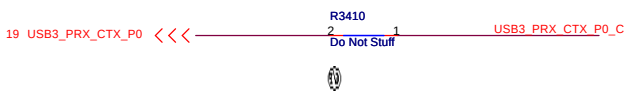


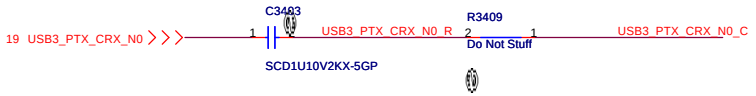


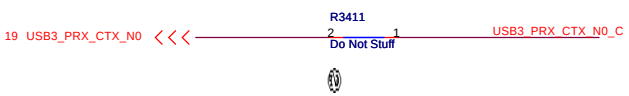


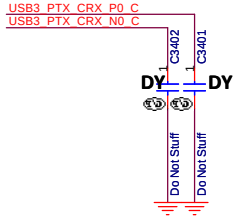












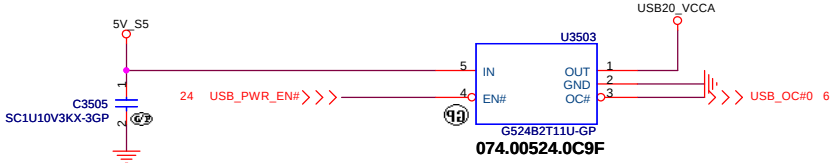
Cedar UMA 14

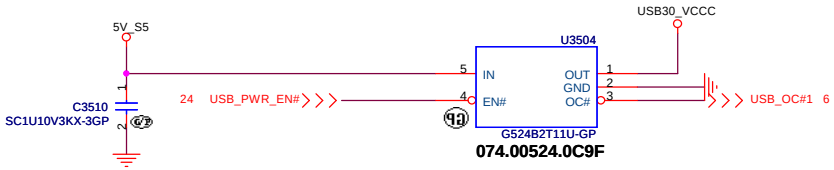
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

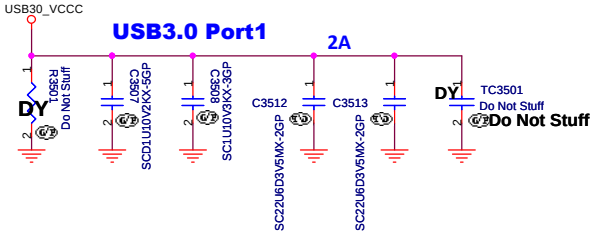
Title: **USB 3.0**

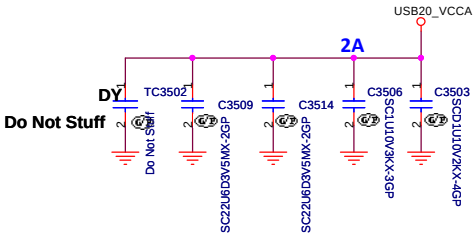
Size	Document Number	Rev
A3	Cedar AMD BEEMA	A00

Date: Wednesday, March 05, 2014 Sheet 34 of 104

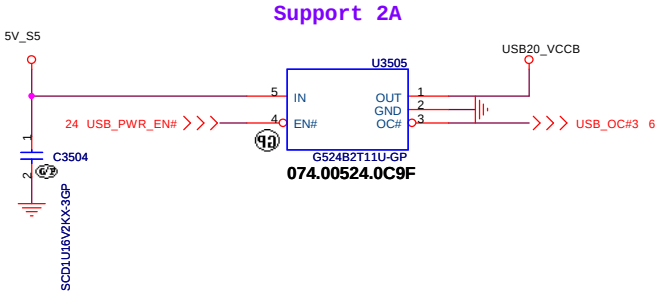


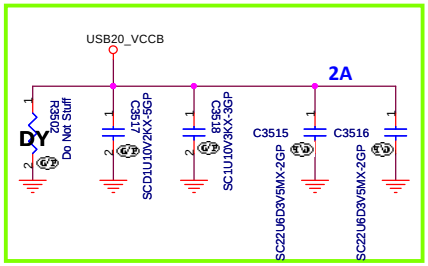






Layout Note: Close CON1





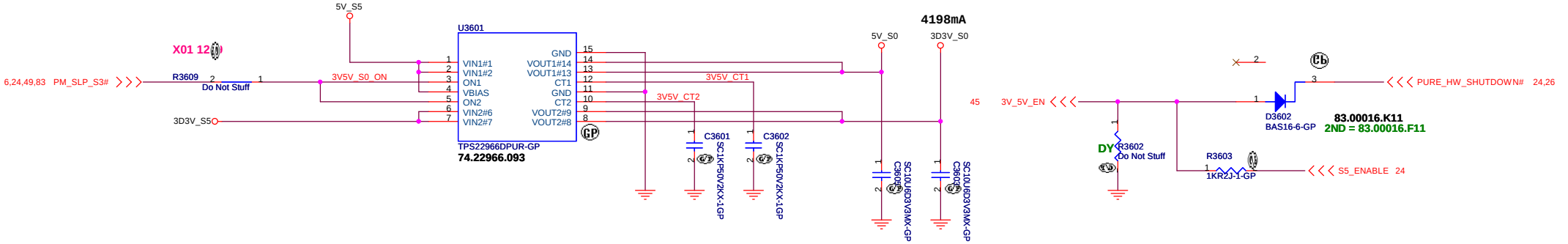
USB2.0 Port3 (IO Board)

Cedar UMA 14

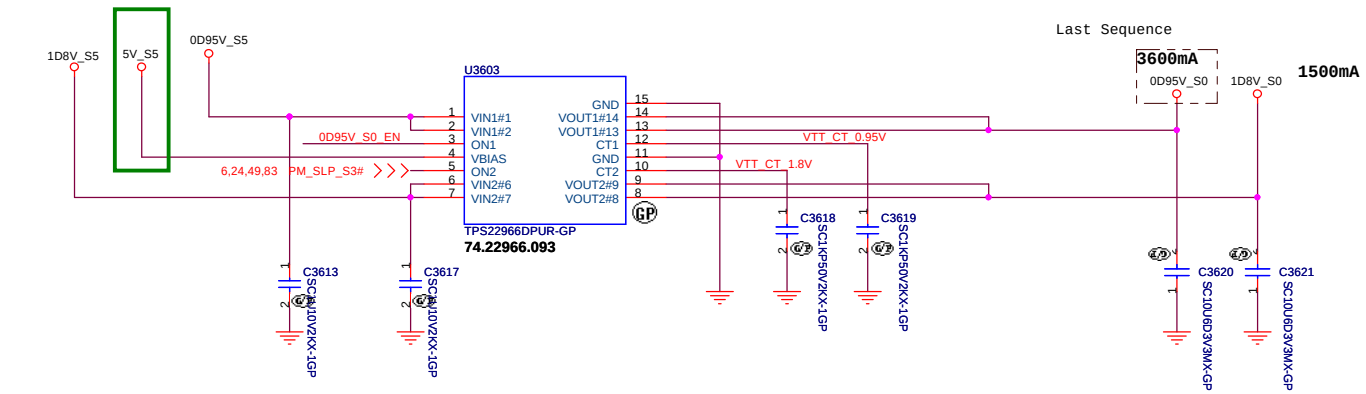
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

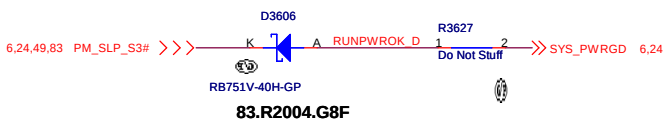
Title	USB Power SW	
Size	Document Number: Cedar AMD BEEMA	Rev: A00
Date: Wednesday, March 05, 2014	Sheet 35 of 104	

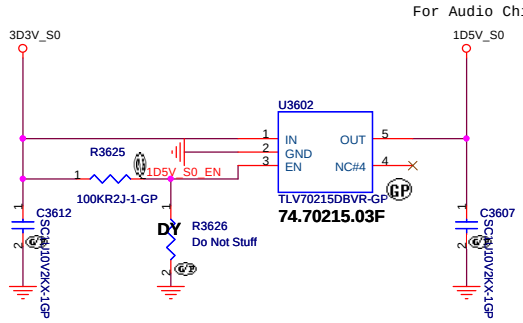
Power Sequence

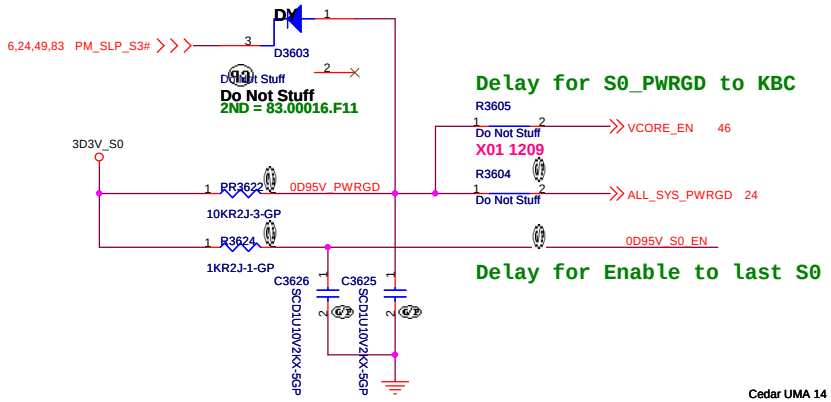


10/16 TI recommend









Cedar UMA 14

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	Cedar AMD BEEMA	A00

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SSID = Reset.Suspend

(Blanking)

Cedar UMA 14

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Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size: A3 | Document Number: Cedar AMD BEEMA | Rev: A00

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(Blanking)

Cedar UMA 14

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***(Reserved)***

Size	Document Number	Rev
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Cedar UMA 14

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved) 1D05_M***

Size	Document Number	Rev
A4	***Cedar AMD BEEMA***	***A00***

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(Blanking)

Cedar UMA 14

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Reserved***		
Size: A4	Document Number: ***Cedar AMD BEEMA***	Rev: ***A00***
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(Blanking)

Cedar UMA 14

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Title: ***Reserved***

Size	Document Number	Rev
A4	***Cedar AMD BEEMA***	***A00***

Date: Wednesday, March 05, 2014 Sheet 41 of 104

SSID = PWR.Support

Layout Note:
PSID Layout width > 25mil

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

DT MODE

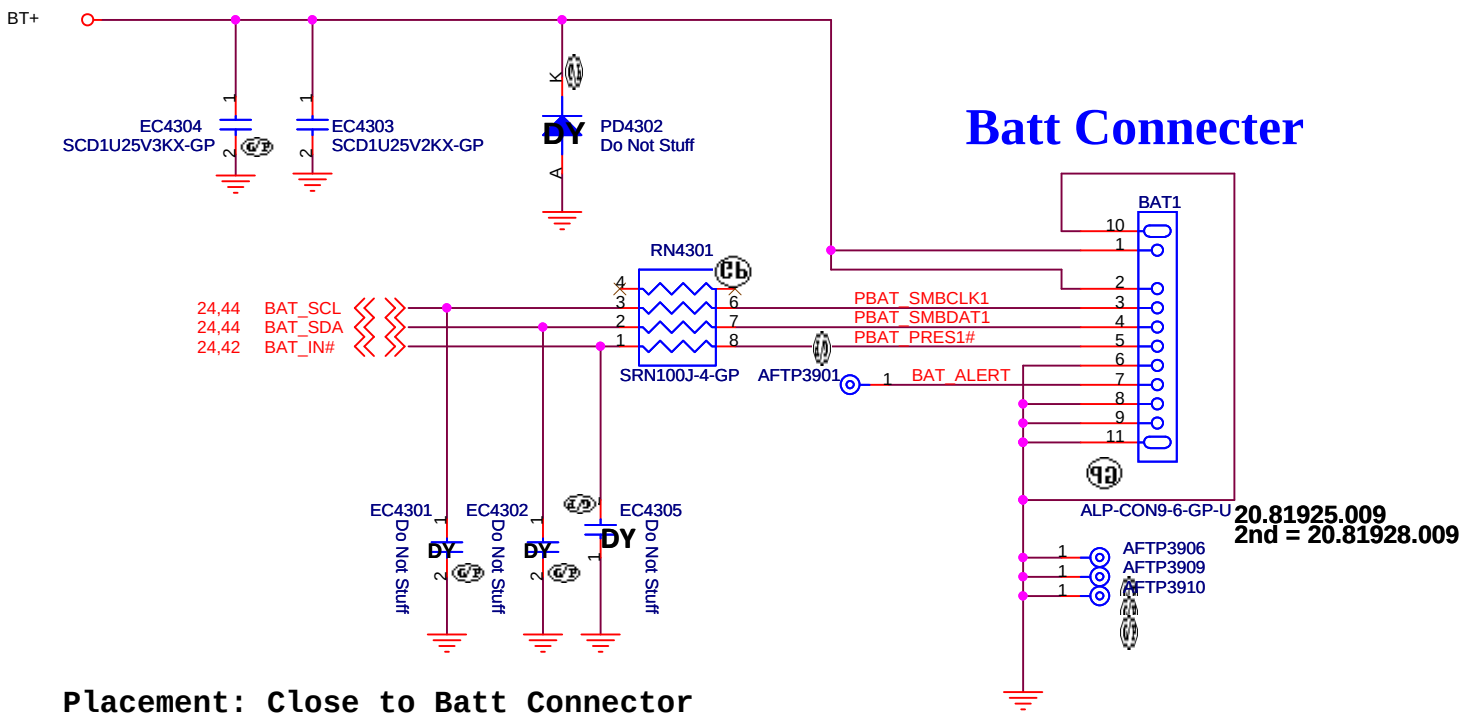
Id=-9.6A
Qg=-25nC
Rdson=18~30mohm

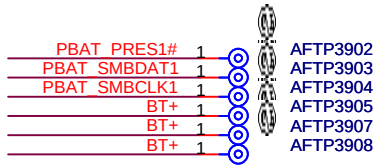
Cedar UMA 14

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

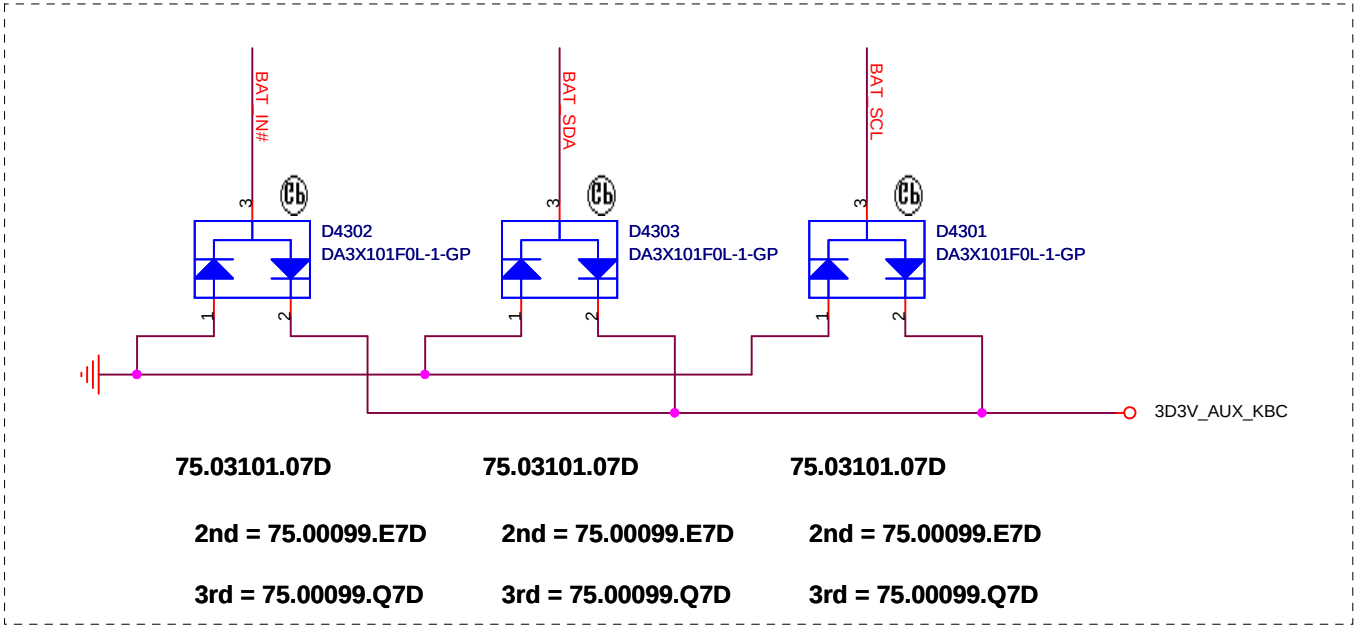
Title: DCIN
Size: A3 | Document Number: Cedar AMD BEEMA | Rev: A00
Date: Wednesday, March 05, 2014 | Sheet 42 of 104

SSID = PWR.Support





Placement: Close to Batt Connector



75.03101.07D	75.03101.07D	75.03101.07D
2nd = 75.00099.E7D	2nd = 75.00099.E7D	2nd = 75.00099.E7D
3rd = 75.00099.Q7D	3rd = 75.00099.Q7D	3rd = 75.00099.Q7D

Cedar UMA 14

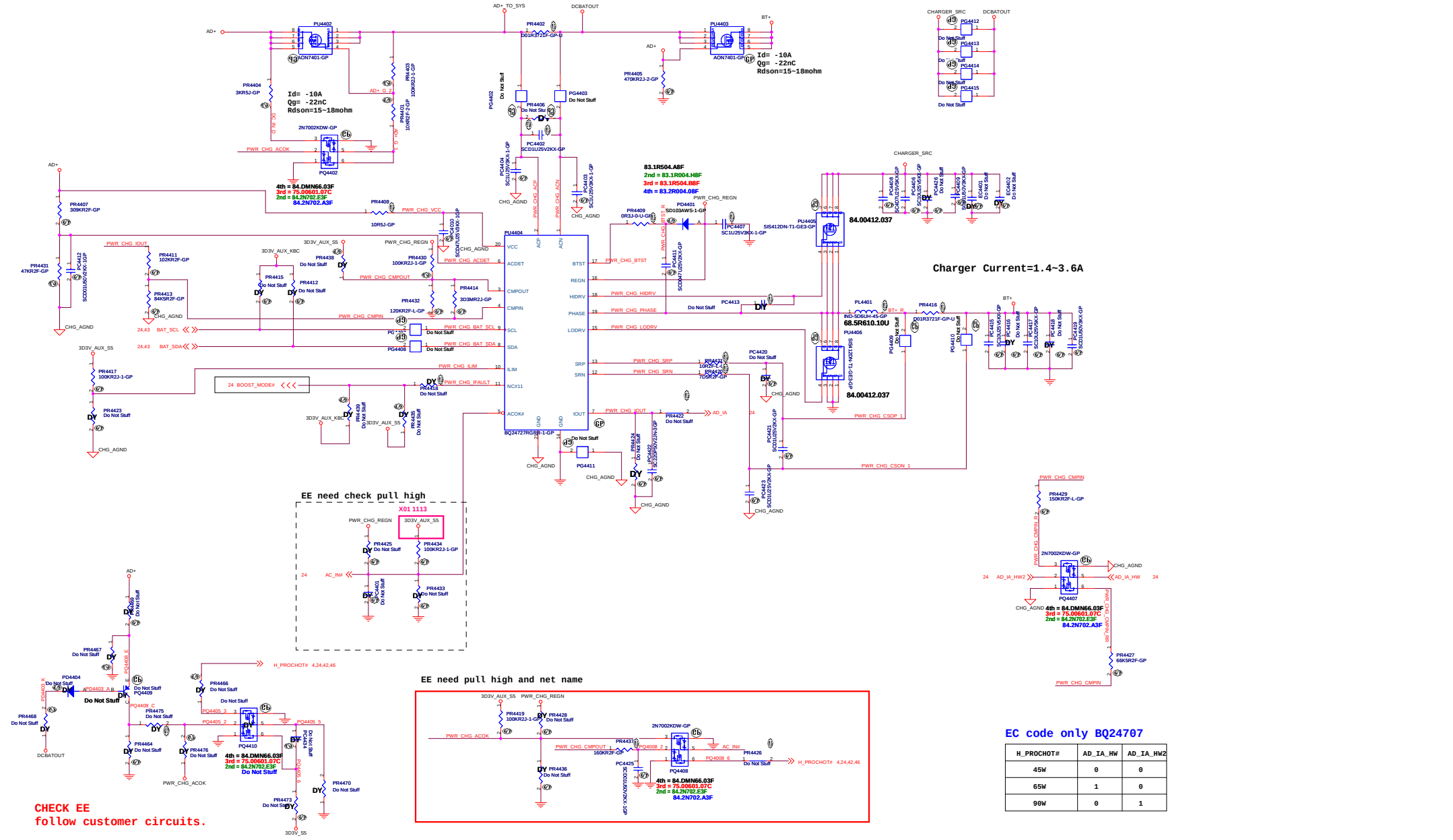
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

Size	Document Number	Rev
A4	Cedar AMD BEEMA	A00

Date: Wednesday, March 05, 2014 Sheet 43 of 104

SSID = Charger



EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
45W	0	0
65W	1	0
90W	0	1

Cedar UMA 14

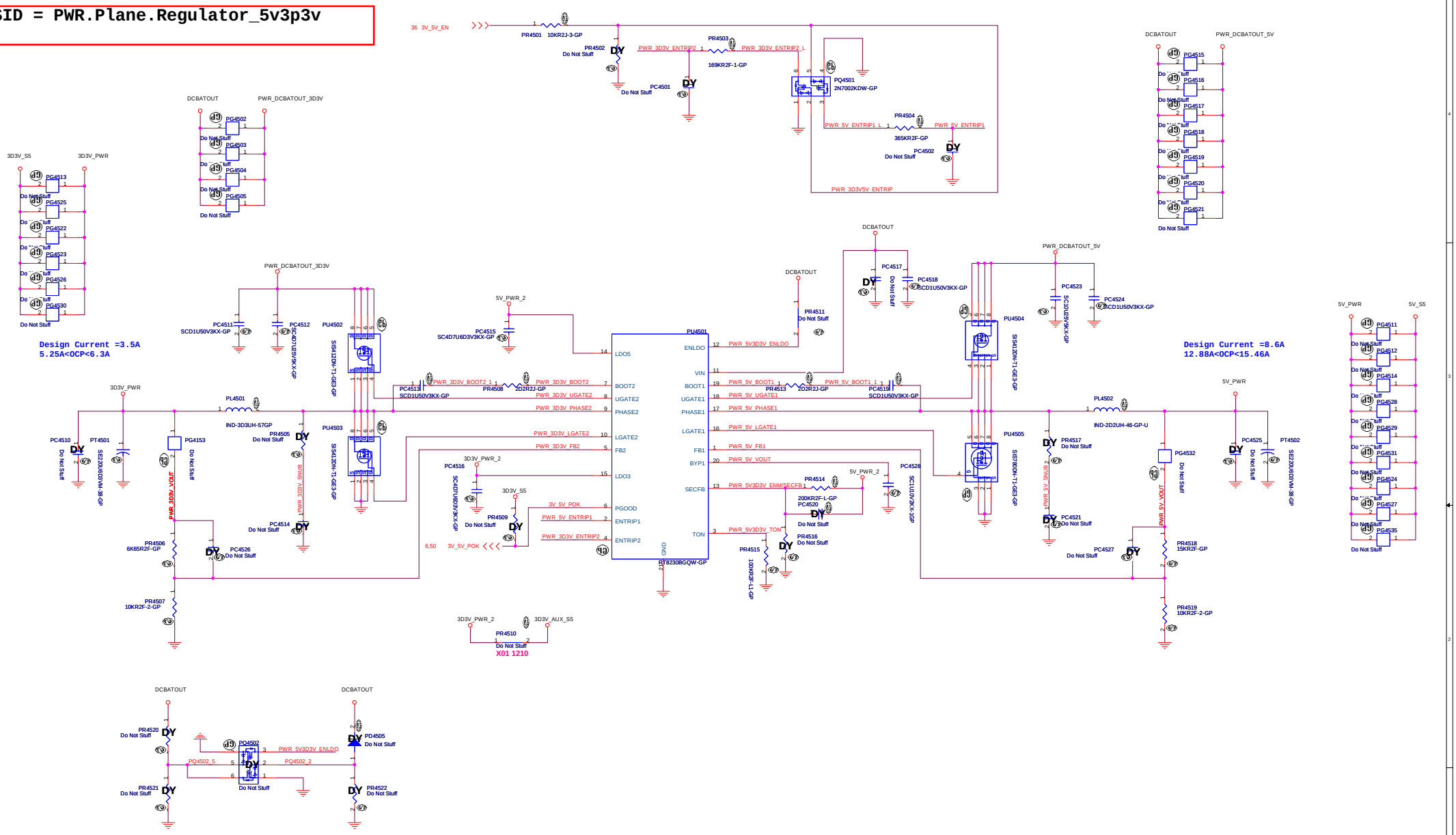
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24727RGRR

Size: Custom | Document Number: Cedar AMD BEEMA | Rev: A00

Date: Wednesday, March 05, 2014 | Sheet 44 of 104

SSID = PWR.Plane.Regulator_5v3p3v



Cedar UMA 14

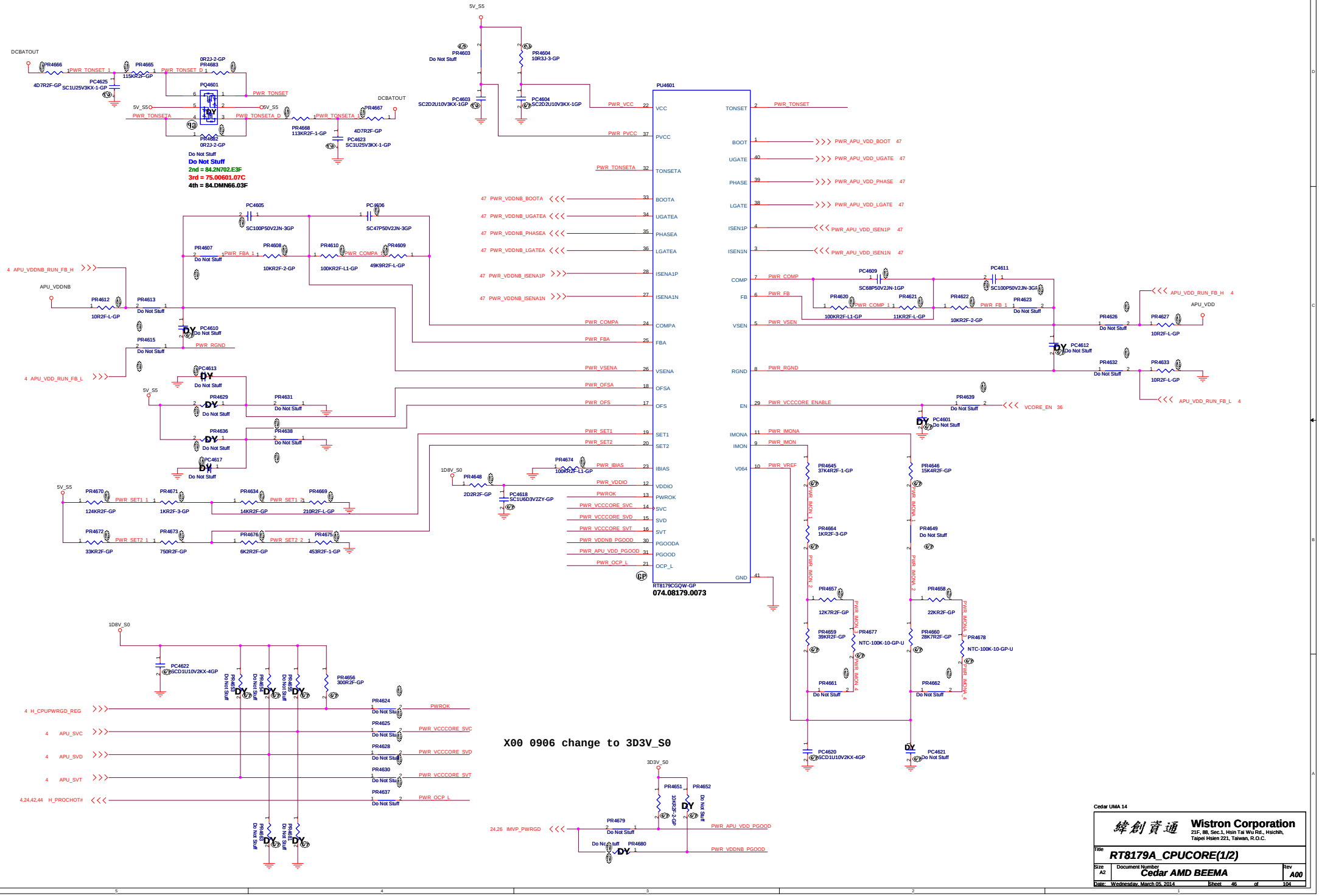
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3V/5V RT8230BGQW

Size: A2 | Document Number: Cedar AMD BEEMA | Rev: A00

Date: Wednesday, March 05, 2014 | Sheet 45 of 104

SSID = CPU.Regulator



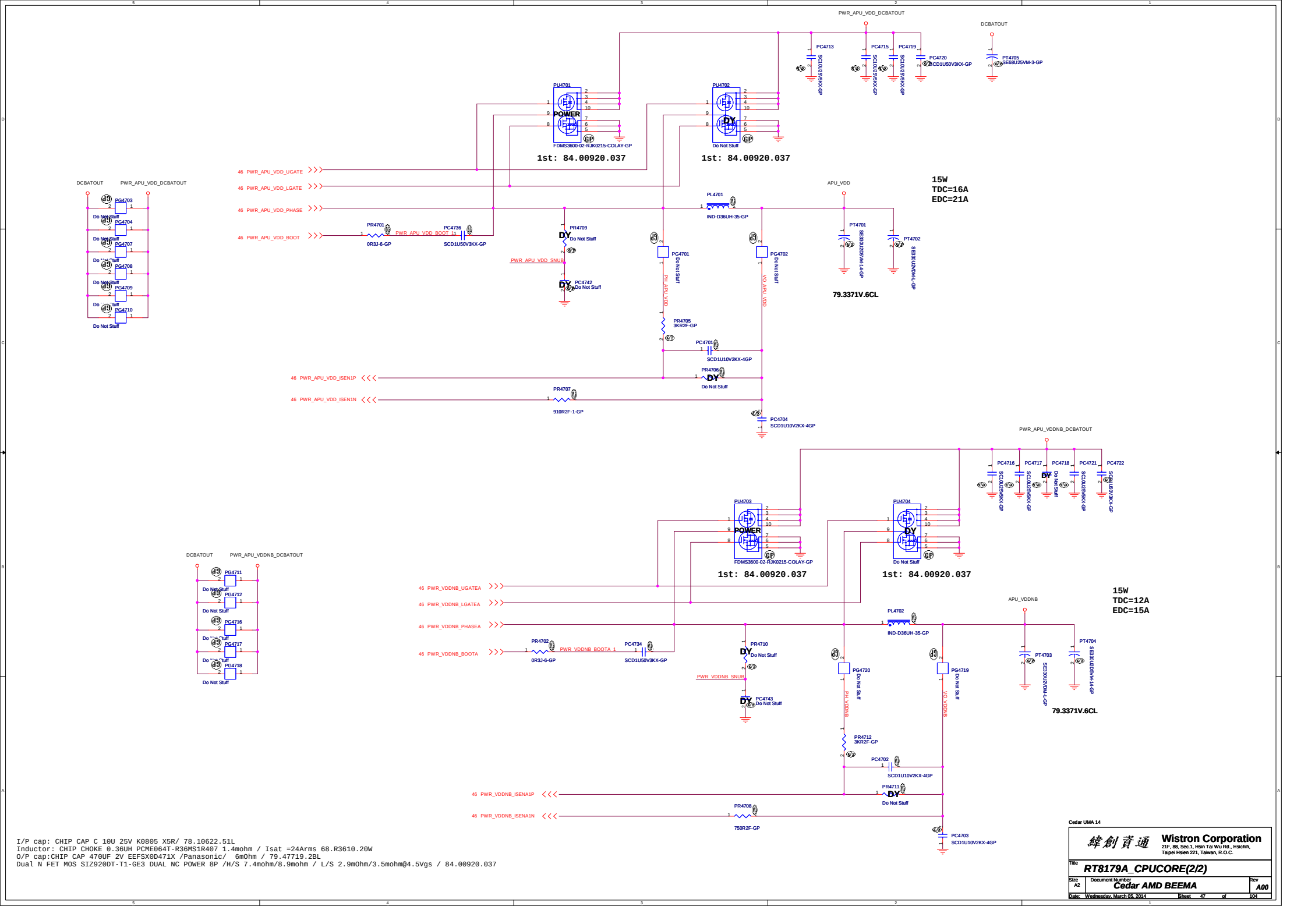
Cedar UMA 14

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8179A_CPUCORE(1/2)

Size	Document Number	Rev
A2	Cedar AMD BEEMA	A00

Date: Wednesday, March 05, 2014 Sheet 46 of 104



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 0.36UH PCME064T-R36MS1R407 1.4mohm / Isat =24Arms 68.R3610.20W
O/P cap:CHIP CAP 470UF 2V EEFSX0D471X /Panasonic/ 6mOhm / 79.47719.2BL
Dual N FET MOS SIZ920DT-T1-GE3 DUAL NC POWER 8P /H/S 7.4mohm/8.9mohm / L/S 2.9mOhm/3.5mohm@4.5Vgs / 84.00920.037

Cedar UMA 14

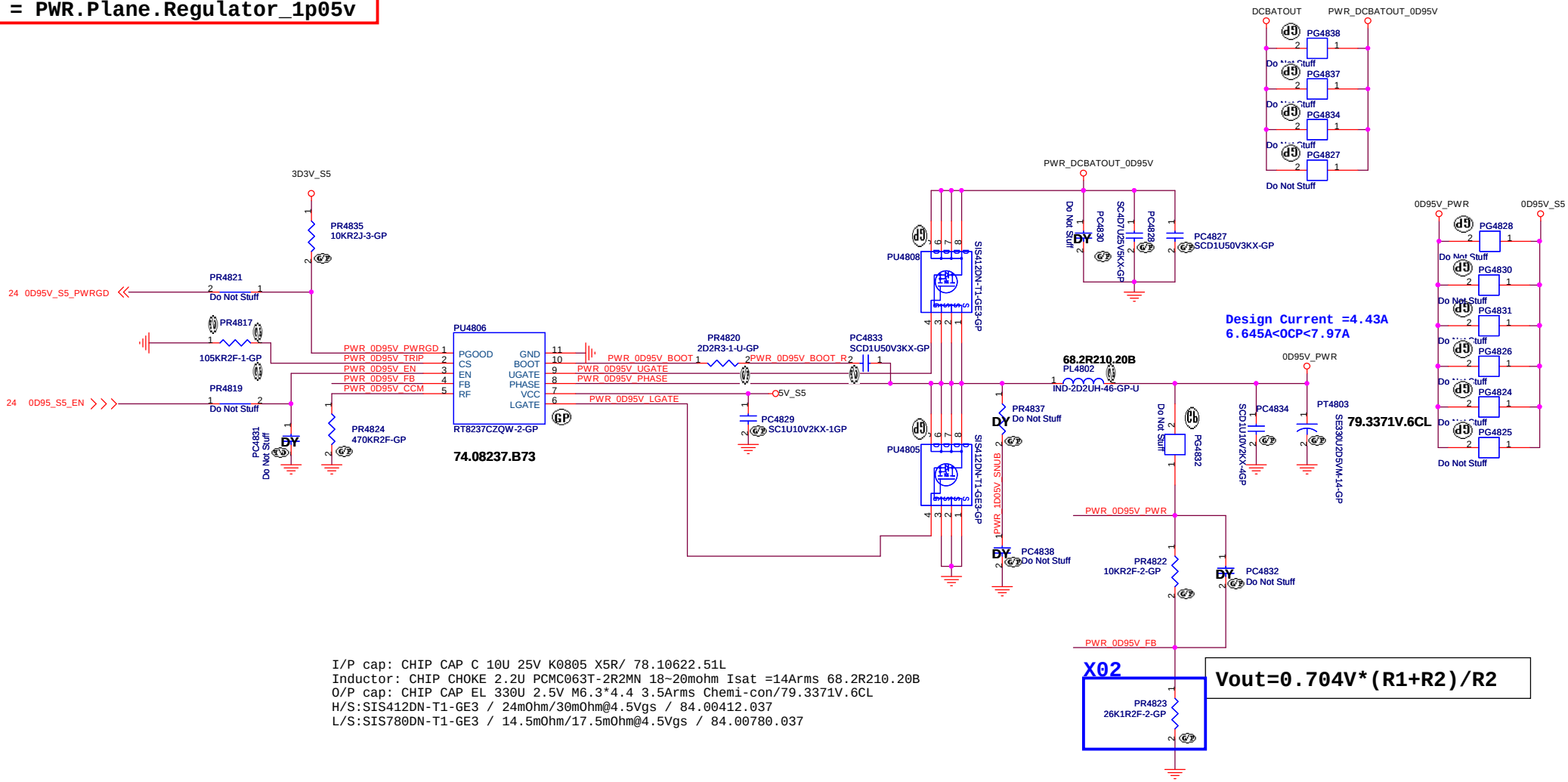
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8179A_CPUCORE(2/2)

Size: A2 | Document Number: Cedar AMD BEEMA | Rev: A00

Date: Wednesday, March 05, 2014 | Sheet 47 of 104

SSID = PWR.Plane.Regulator_1p05v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 3.5Arms Chemi-con/79.3371V.6CL
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

Cedar UMA 14

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RT8237_0D95V***

Size	Document Number	Rev
A3	***Cedar AMD BEEMA***	***A00***

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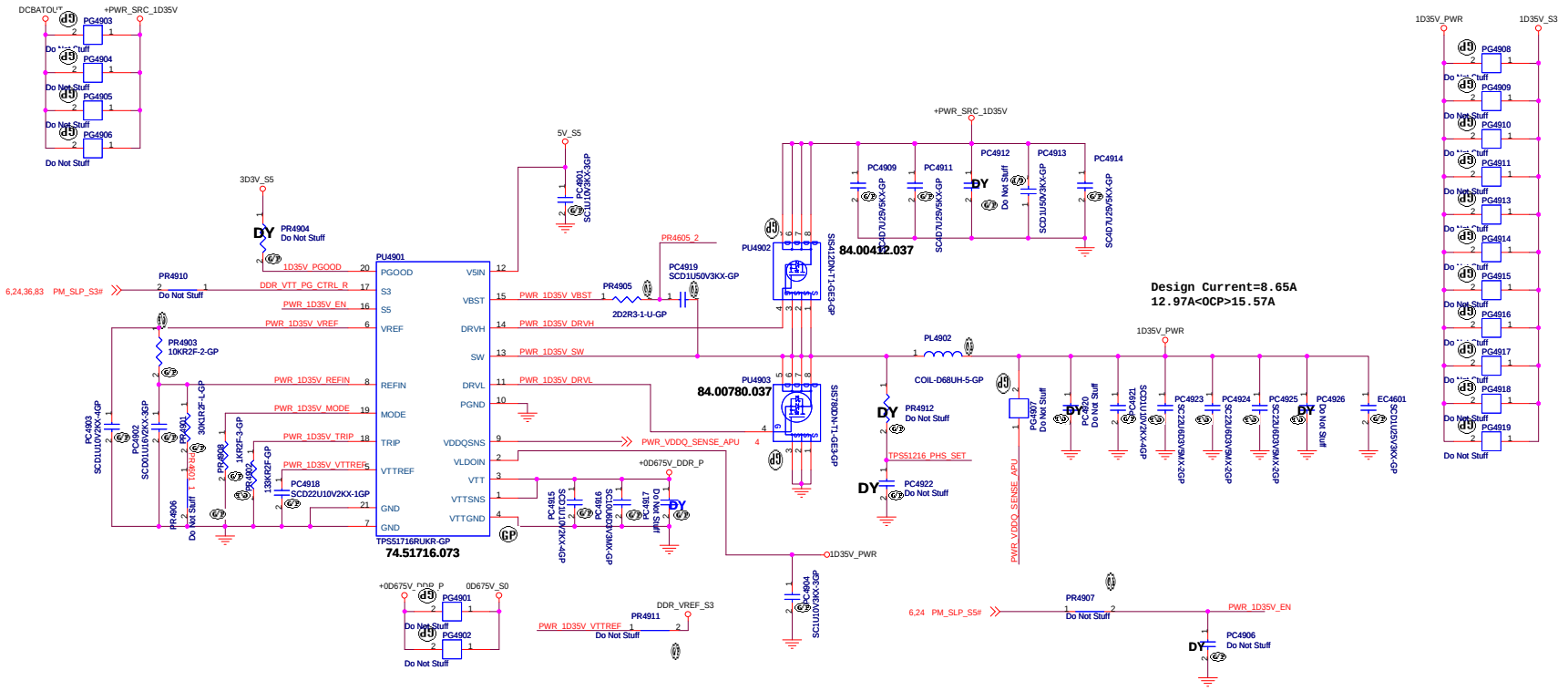
SSID = PWR.Plane.Regulator_1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

TPS51716 MODE

PR4608	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.1UH M PCMC063T-R10MN 1.5~1.7mohm Isat =60Arms 68.R1010.10T
O/P cap: CHIP CAP C 22U 6.3V M0805 X5R /78.22610.51L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

Cedar UMA 14

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51716_1D35V_S3

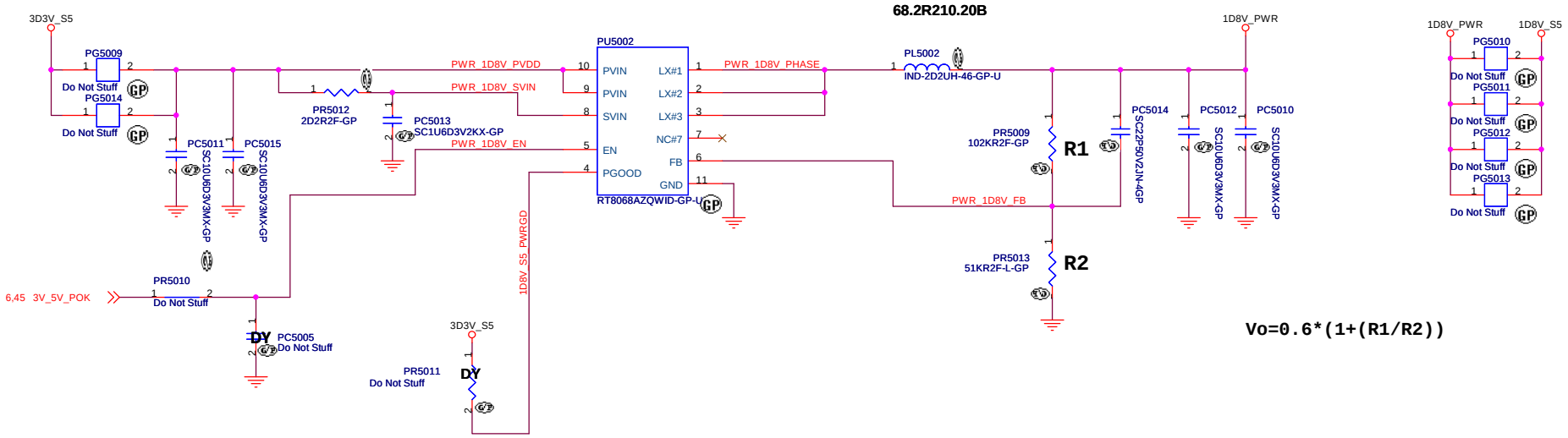
Size: C | Document Number: Cedar AMD BEEMA | Rev: A00

Date: Wednesday, March 05, 2014 | Sheet 49 of 104

SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S5

Design Current=1.62A



$$Vo=0.6*(1+(R1/R2))$$

Cedar UMA 14

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
RT8068A_1D8V_S5		
Size: A3	Document Number: Cedar AMD BEEMA	Rev: A00
Date: Wednesday, March 05, 2014	Sheet 50 of 104	

SSID = PWR.Plane.Regulator_1p5v

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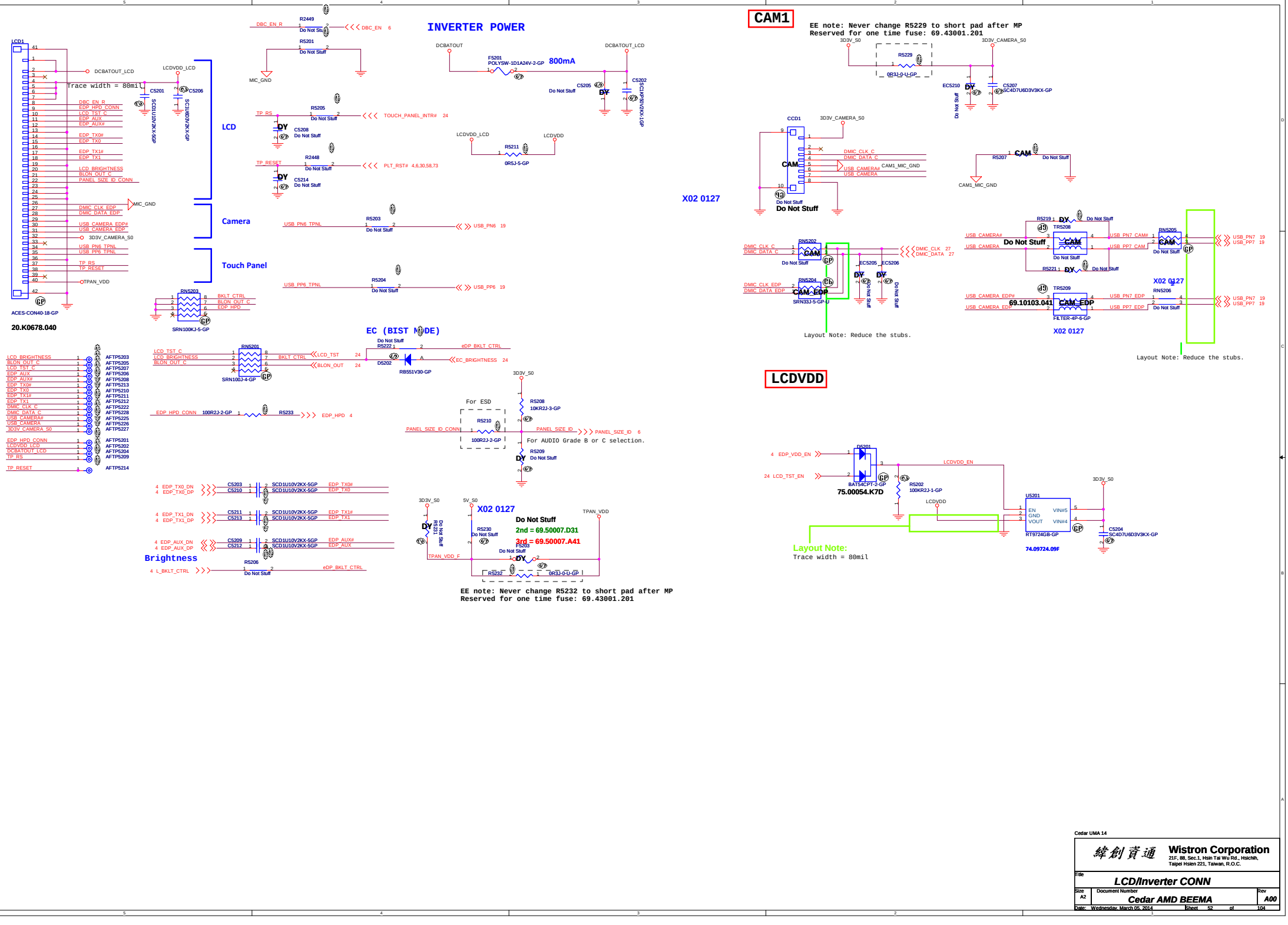
Cedar UMA 14

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TLV70215_1D5*		
Size: A3	Document Number: *Cedar AMD BEEMA*	Rev: *A00*
Date: Wednesday, March 05, 2014	Sheet 51 of 104	


INVERTER POWER
LCD
Camera
Touch Panel
EC (BIST MODE)
Brightness
CAM1
LCDVDD
X02 0127
Do Not Stuff
800mA
Trace width = 80mil
Layout Note: Reduce the stubs.
Layout Note:
Trace width = 80mil
For AUDIO Grade B or C selection.
EE note: Never change R5229 to short pad after MP
Reserved for one time fuse: 69.43001.201
EE note: Never change R5232 to short pad after MP
Reserved for one time fuse: 69.43001.201
2nd = 69.50007.D31
3rd = 69.50007.A41
20.K0678.040
75.00054.K7D
69.10103.041
74.09724.09F
Cedar UMA 14
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LCD/Inverter CONN
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Cedar UMA 14

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *(Reserved)*

Size	Document Number	Rev
A3	*Cedar AMD BEEMA*	*A00*

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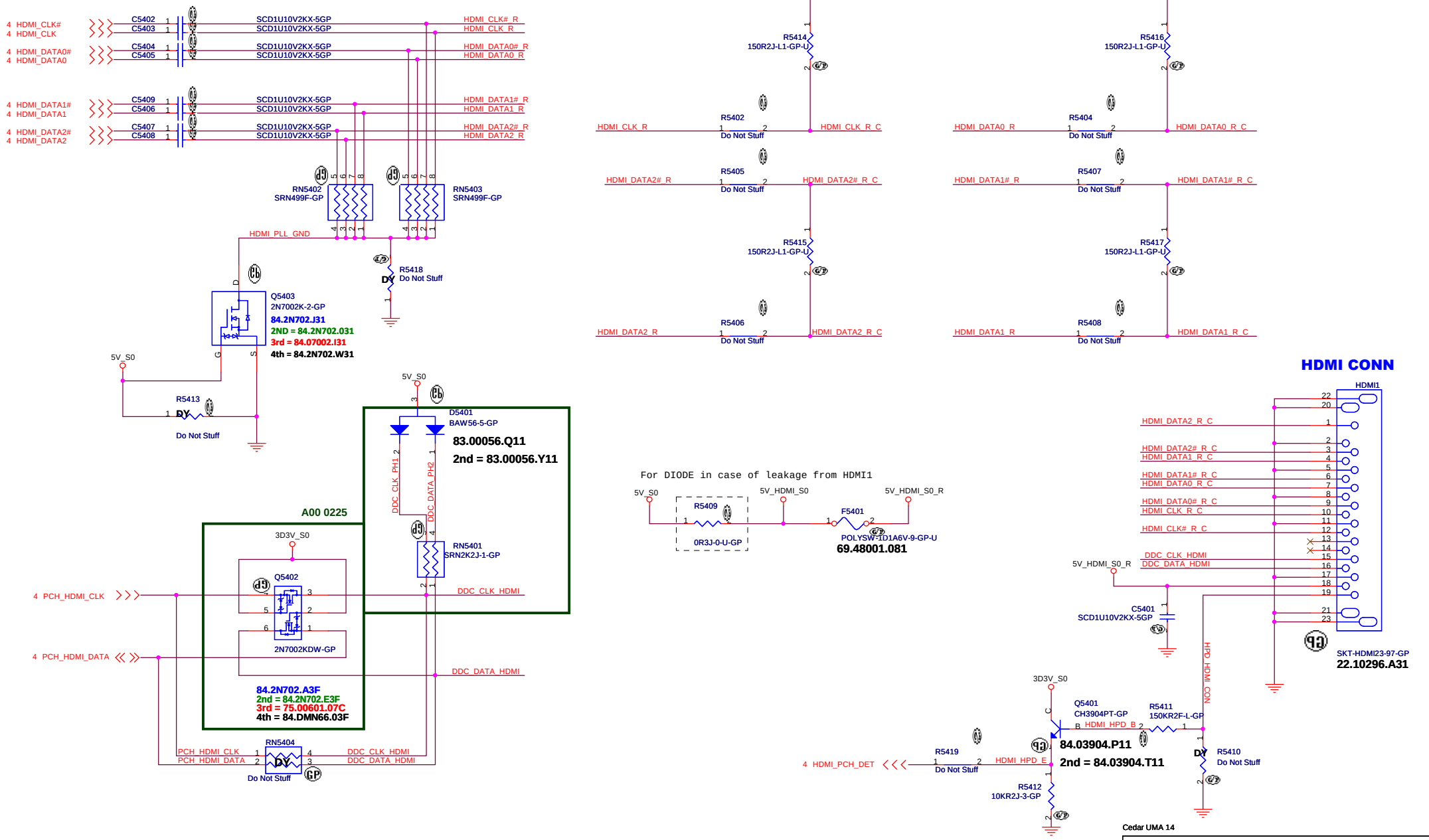
SSID = VIDEO



Cedar UMA 14

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDMI Level Shifter/Connector***

Size	Document Number	Rev
A3	***Cedar AMD BEEMA***	***A00***

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(Blanking)

Cedar UMA 14

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VGA Con.(Reserve)*

Size	Document Number	Rev
A3	*Cedar AMD BEEMA*	*A00*

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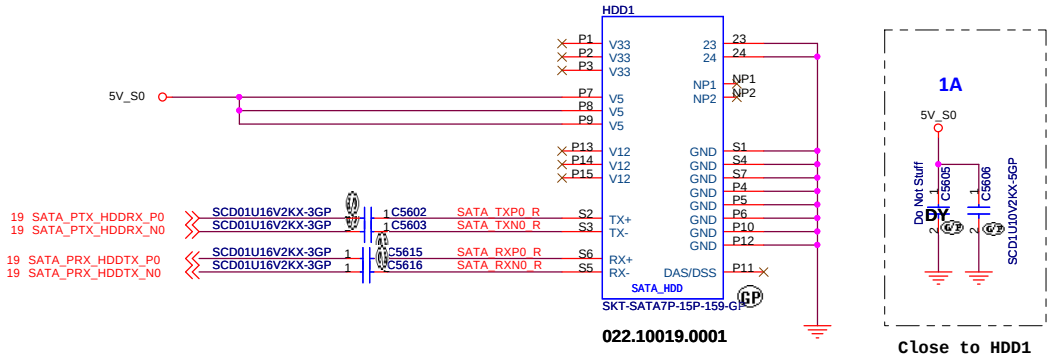
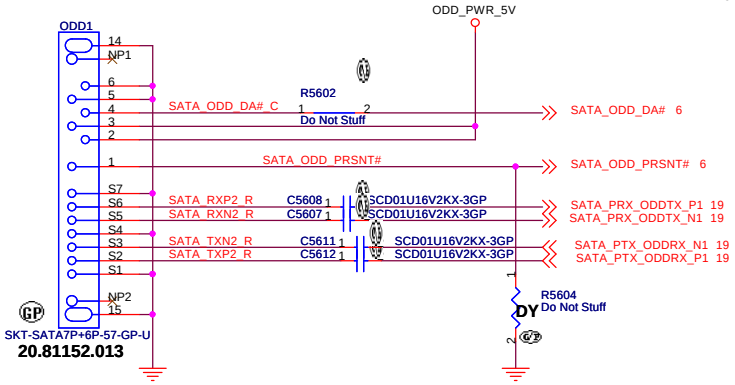
SSID = SATA

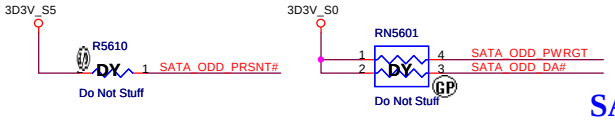
SATA HDD Connector



ME Note: New HDD conn symbol is not ready,
we will use original OAK HDD conn (22.10300.991) and shift to the correct position.

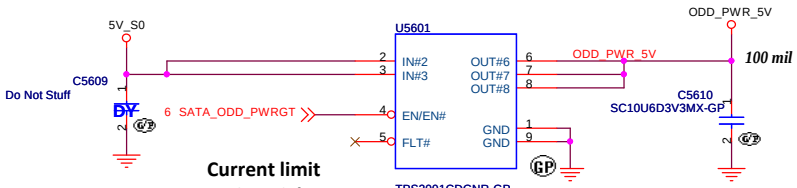
ODD Connector

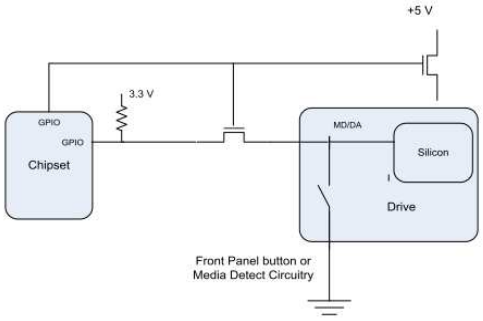




SATA Zero Power ODD

2.5A





Cedar UMA 14

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD/ODD		
Size: A3	Document Number: Cedar AMD BEEMA	Rev: A00
Date: Wednesday, March 05, 2014	Sheet 56 of 104	

SSID = ESATA

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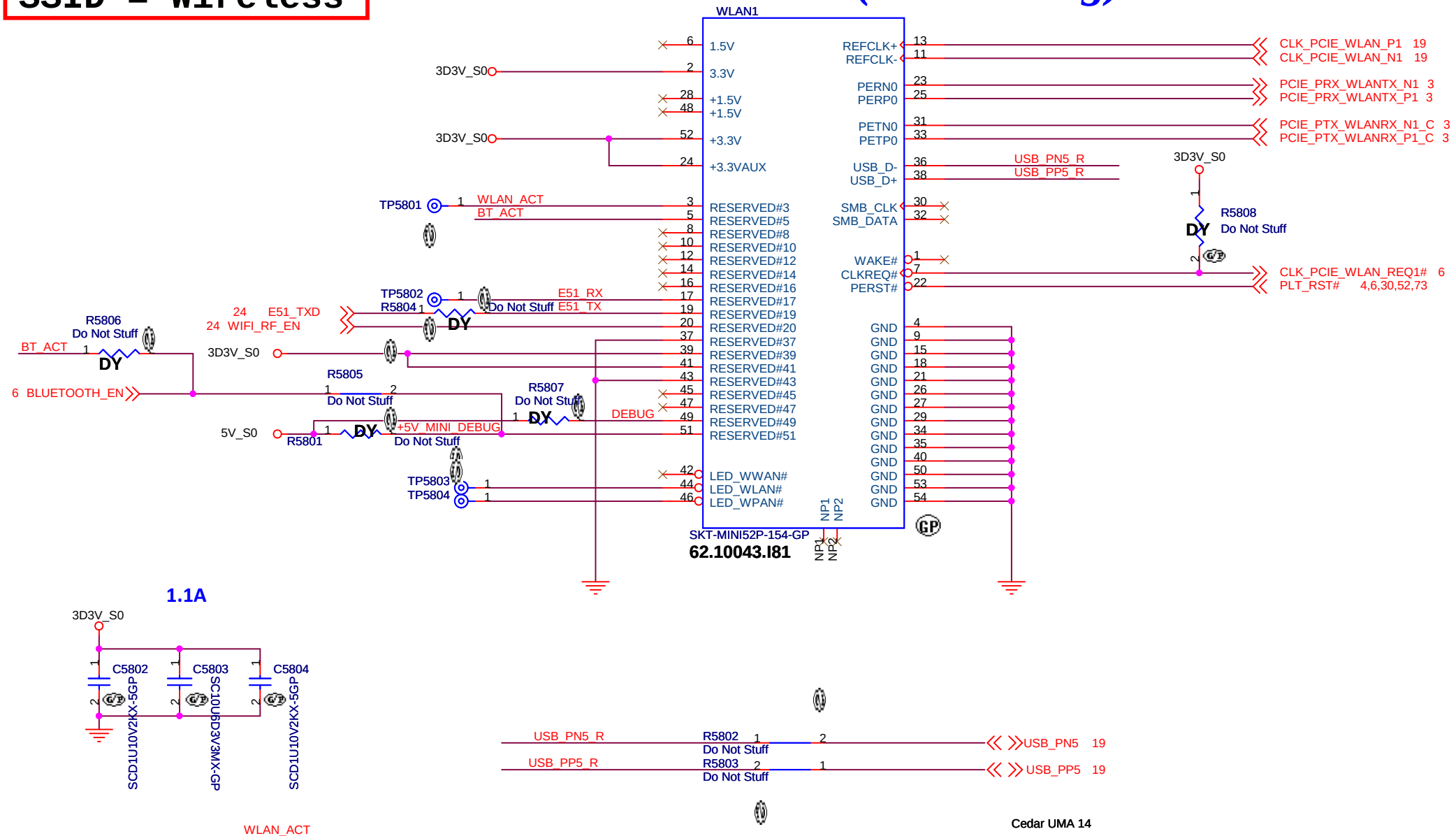
Cedar UMA 14

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA		
Size: A3	Document Number: Cedar AMD BEEMA	Rev: A00
Date: Wednesday, March 05, 2014	Sheet 57 of 104	

Mini Card Connector(802.11a/b/g)

SSID = Wireless



Cedar UMA 14

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**WLAN CONN**	
Size A4	Document Number **Cedar AMD BEEMA**	Rev **A00**
Date: Wednesday, March 05, 2014	Sheet 58 of 104	

(Blanking)

Cedar UMA 14

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Title: ***Reserved***		
Size: A4	Document Number: ***Cedar AMD BEEMA***	Rev: ***A00***
Date: Wednesday, March 05, 2014	Sheet 59 of 104	

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Cedar UMA 14

緯創資通 **Wistron Corporation**
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Title: ***(Reserved)***

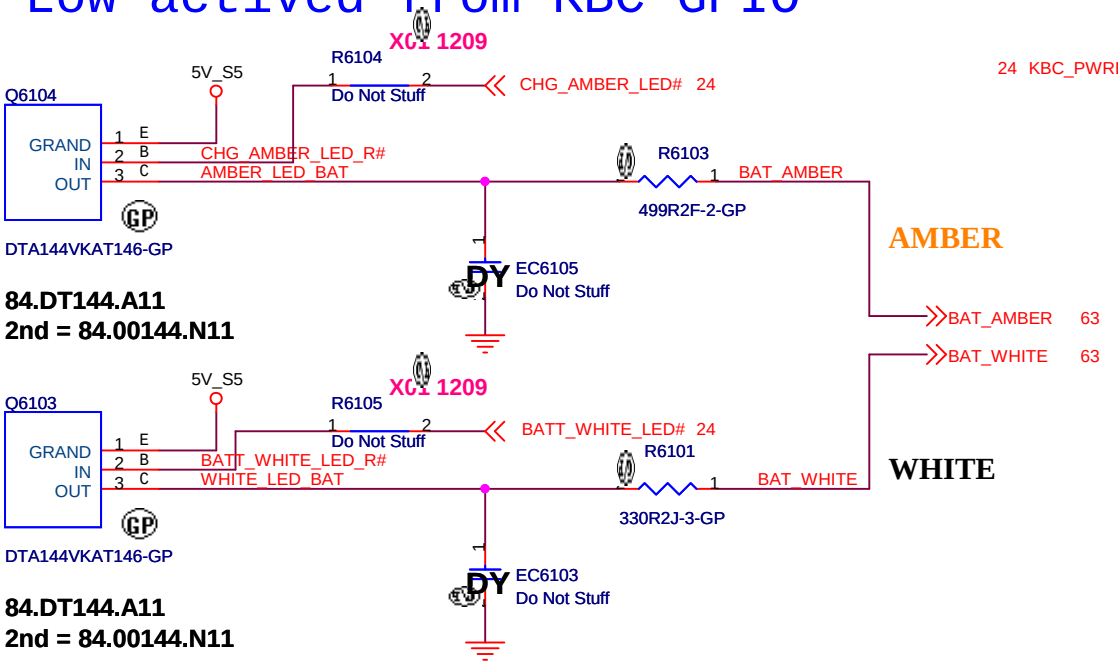
Size	Document Number	Rev
A4	***Cedar AMD BEEMA***	***A00***

Date: Wednesday, March 05, 2014 Sheet 60 of 104

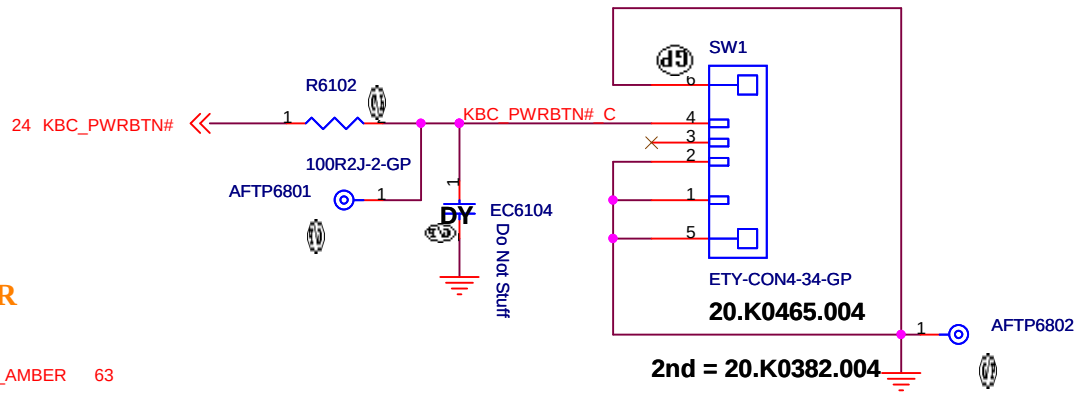
SSID = User.Interface

Battery LED1 (AMBER_LED)

Low actived from KBC GPIO



Power button



Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

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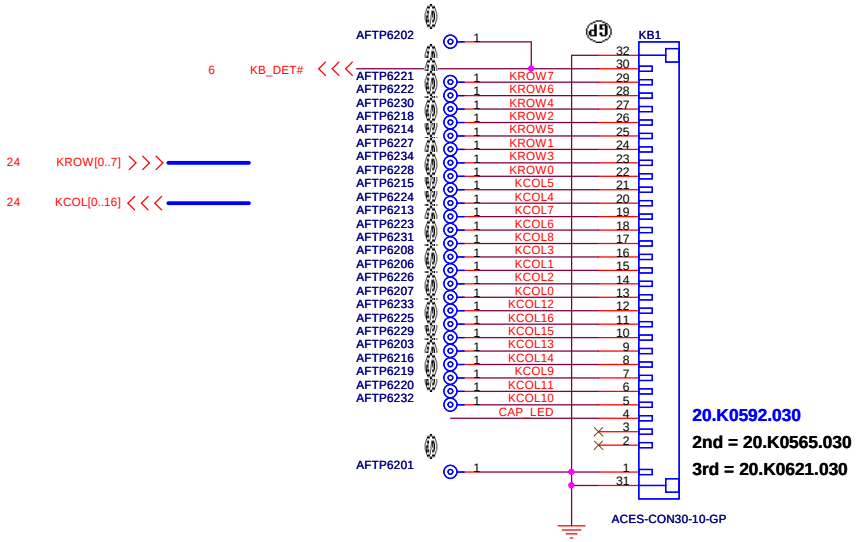
Title: *LED Bard/Power Button*		
Size: A4	Document Number: Cedar AMD BEEMA	Rev: A00
Date: Wednesday, March 05, 2014	Sheet 61 of 104	

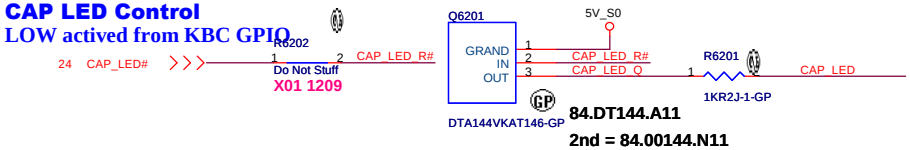
SSID = KBC

Internal Keyboard Connector (DVC40)

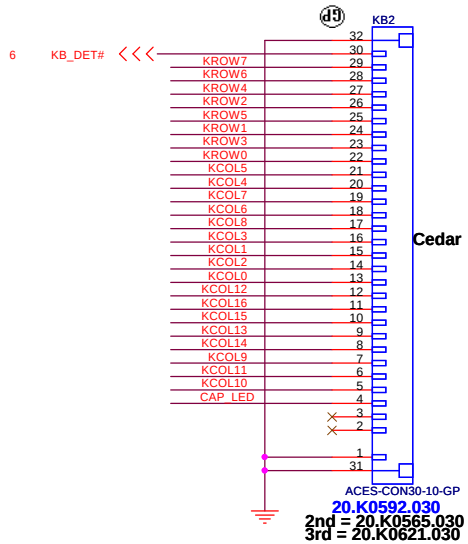


CAP LED Control

LOW actived from KBC GPIO



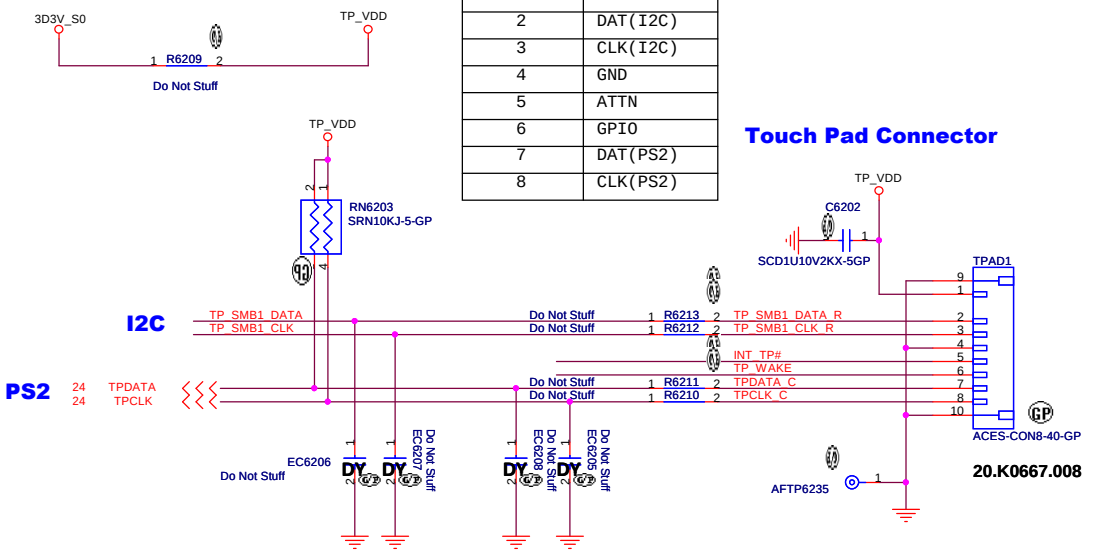
Internal Keyboard Connector (DVC50)

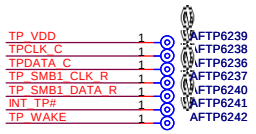


SSID = Touch.Pad

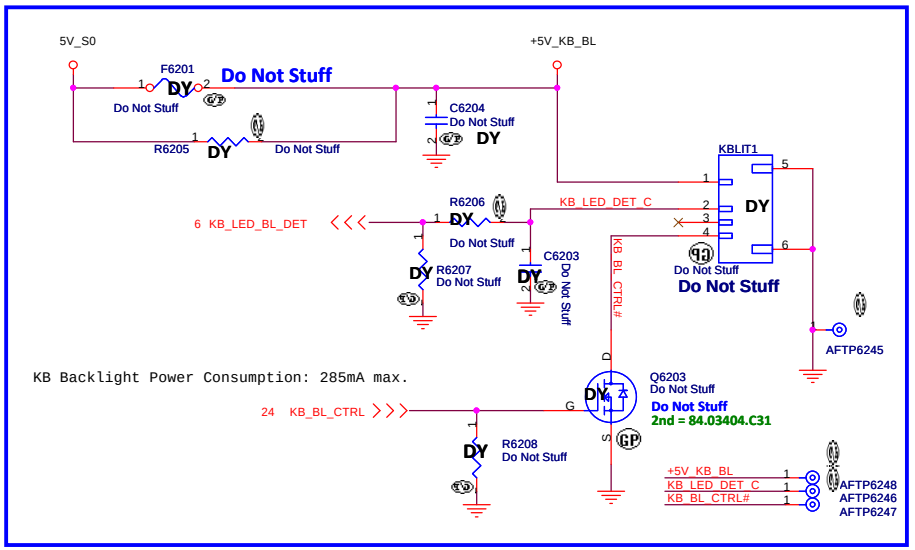
Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

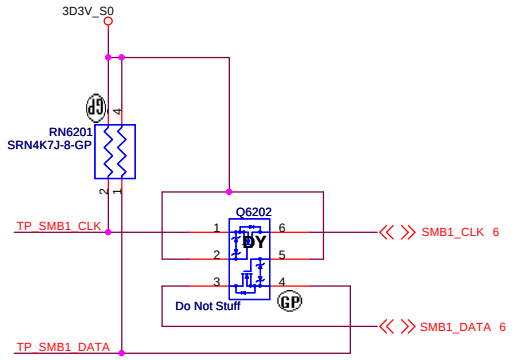
Touch Pad Connector





Keyboard Backlight





Cedar UMA 14

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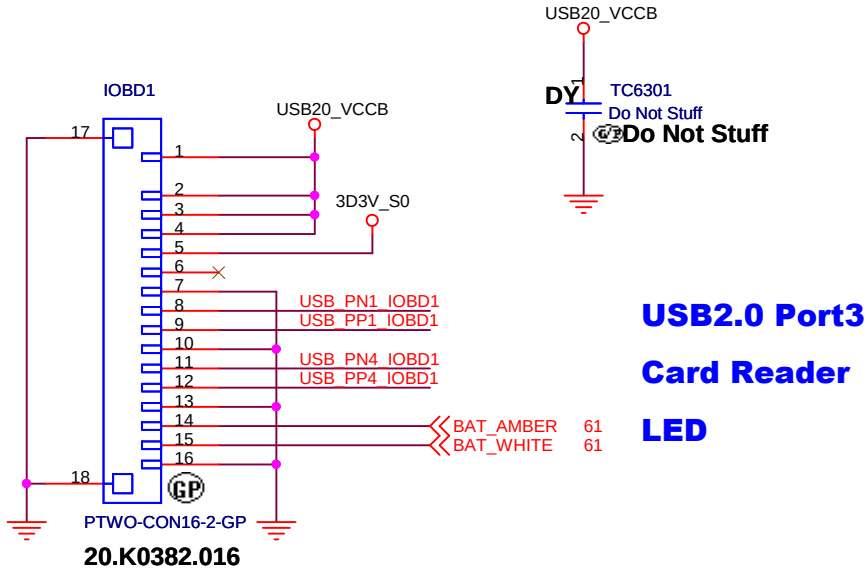
Title: Key Board/Touch Pad

Size: A3 | Document Number: Cedar AMD BEEMA | Rev: A00

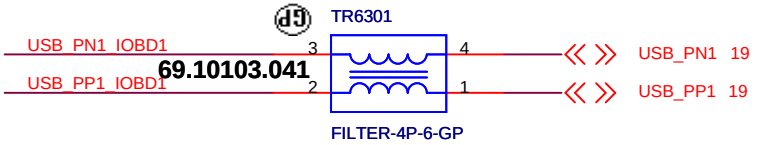
Date: Wednesday, March 05, 2014 | Sheet 62 of 104

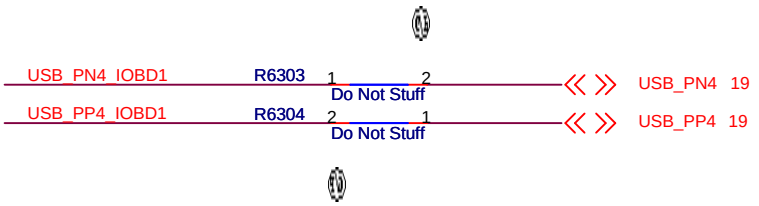


USB2.0 Port3

Card Reader

LED





The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA

Cedar UMA 14

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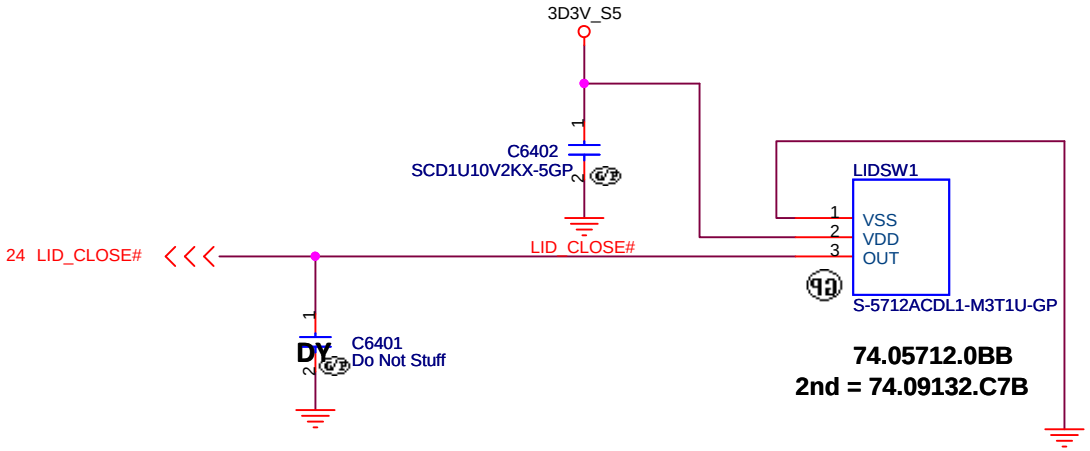
Title: ***IO Board Connector***

Size	Document Number	Rev
A4	***Cedar AMD BEEMA***	***A00***

Date: Wednesday, March 05, 2014 Sheet 63 of 104

SSID = User.Interface



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Title: ***Hall Sensor***

Size	Document Number	Rev
A4	***Cedar AMD BEEMA***	***A00***

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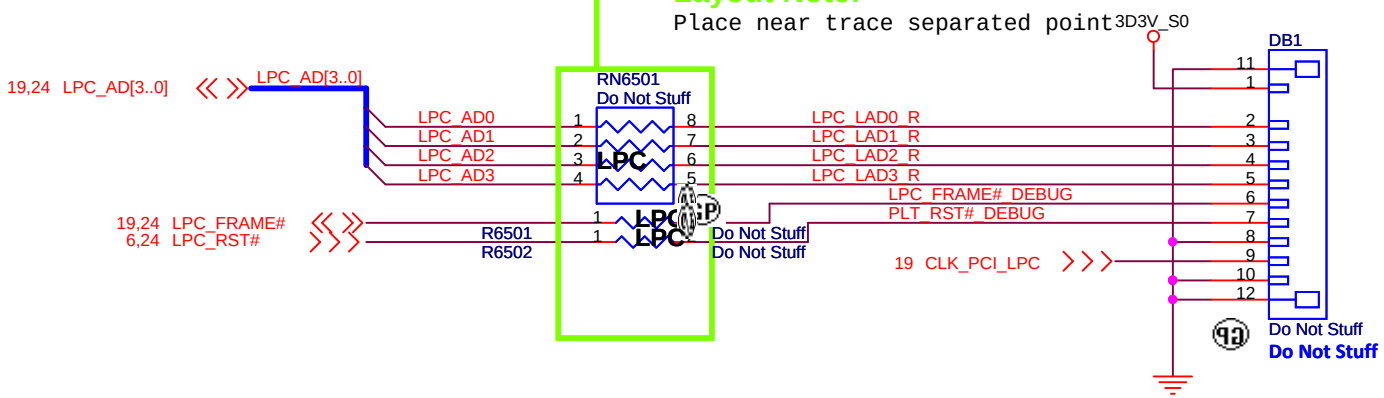
SSID = DEBUG PORT

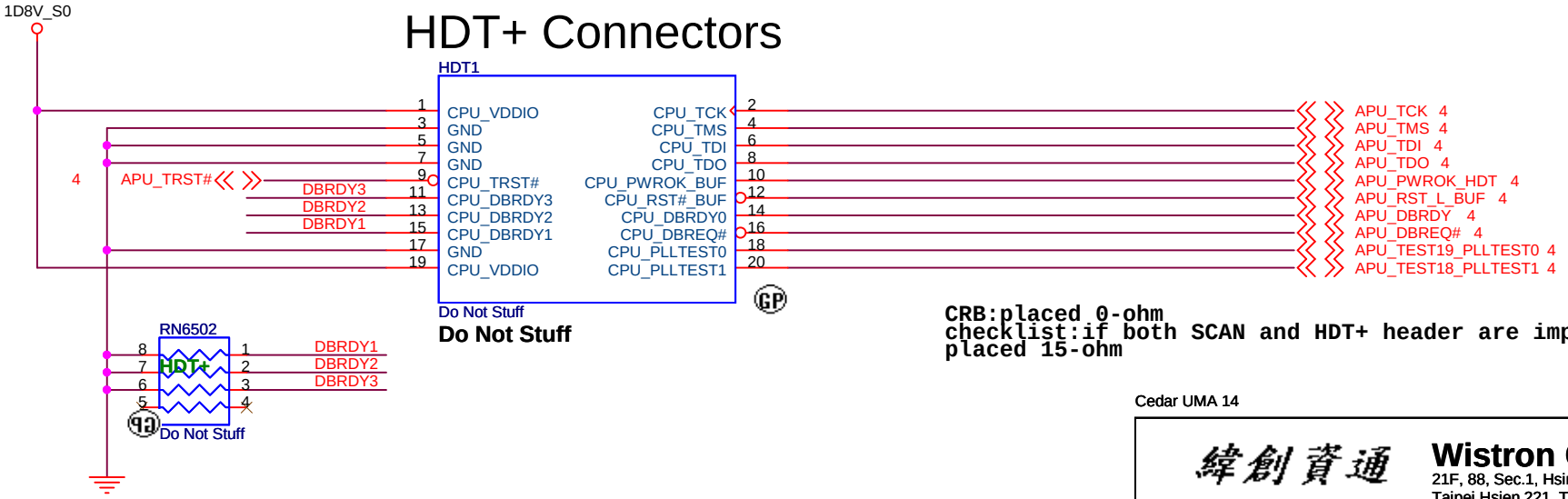
Debug Connector

Layout Note:
Place near trace separated point



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

HDT+ Connectors



CRB:placed 0-ohm
checklist:if both SCAN and HDT+ header are implement placed 15-ohm

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Title	Dubug connector	
Size A4	Document Number Cedar AMD BEEMA	Rev A00
Date: Wednesday, March 05, 2014	Sheet 65 of 104	

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Title: ***Reserved***

Size	Document Number	Rev
A4	***Cedar AMD BEEMA***	***A00***

Date: Wednesday, March 05, 2014 Sheet 66 of 104

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Cedar UMA 14

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Title: ***Reserved***

Size	Document Number	Rev
A3	***Cedar AMD BEEMA***	***A00***

Date: Wednesday, March 05, 2014 Sheet 67 of 104

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Title: ***Thunderbolt (1/5)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 68 of 104

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Cedar UMA 14

緯創資通 **Wistron Corporation**
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Title: ***Thunderbolt (2/5)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 69 of 104

(Blanking)

Cedar UMA 14

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Title: ***Thunderbolt (3/5)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 70 of 104

(Blanking)

Cedar UMA 14

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Title: ***Thunderbolt (4/5)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 71 of 104

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Cedar UMA 14

緯創資通 **Wistron Corporation**
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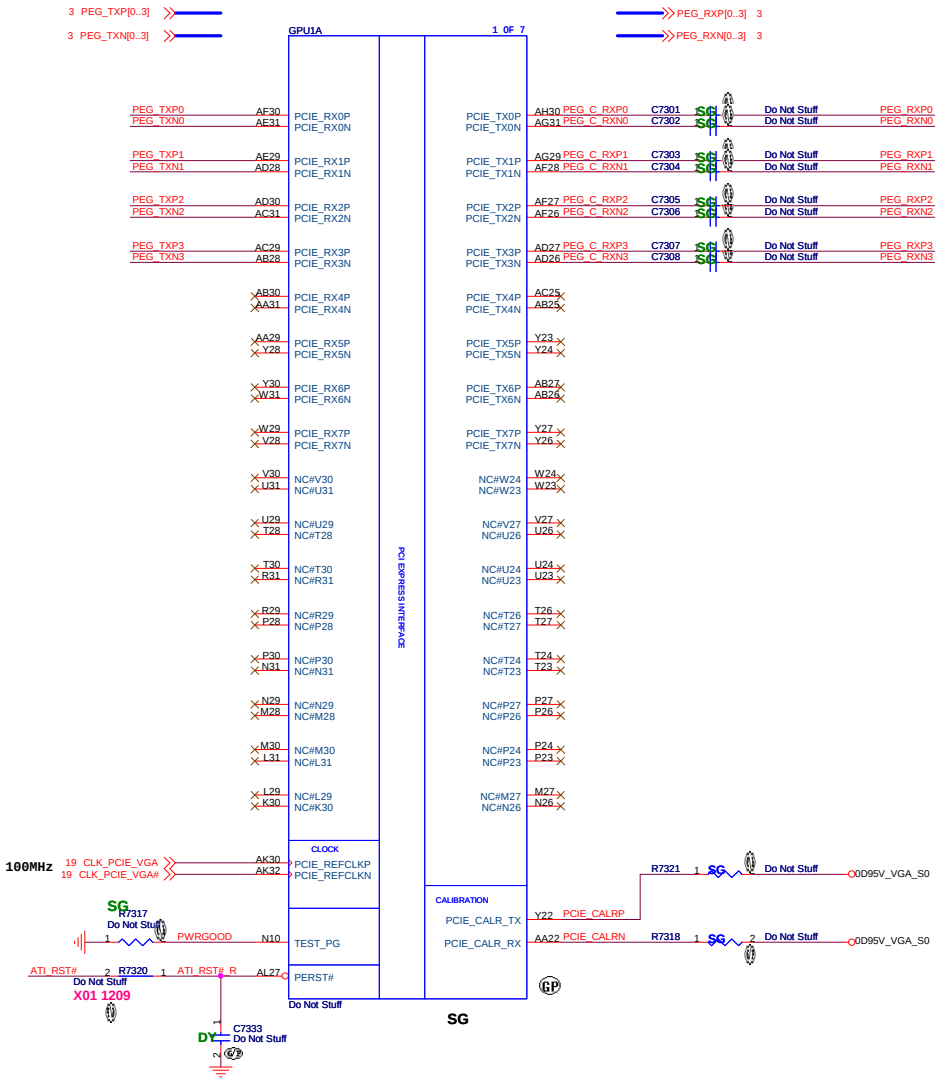
Title: ***Thunderbolt (5/5)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 72 of 104



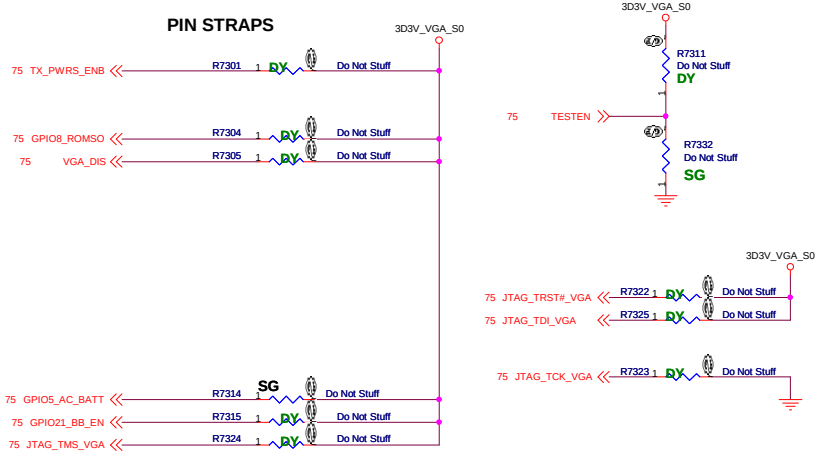
CONFIGURATION STRAPS

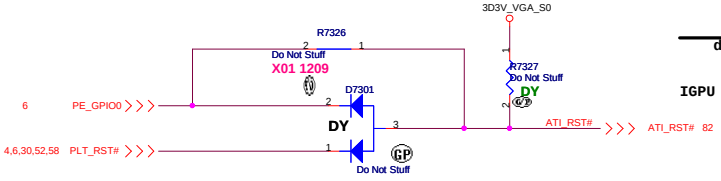
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS





	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACO	H

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

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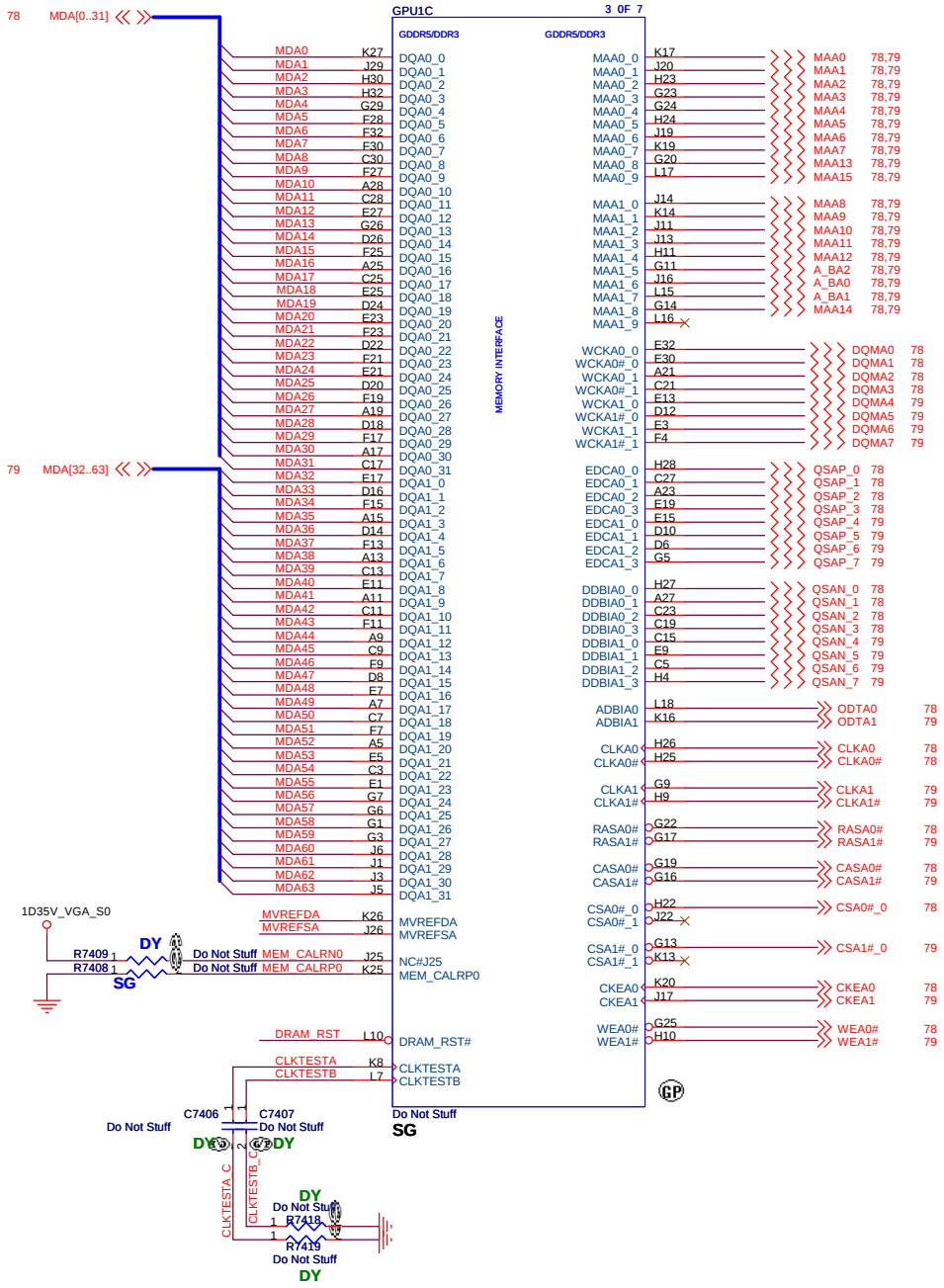
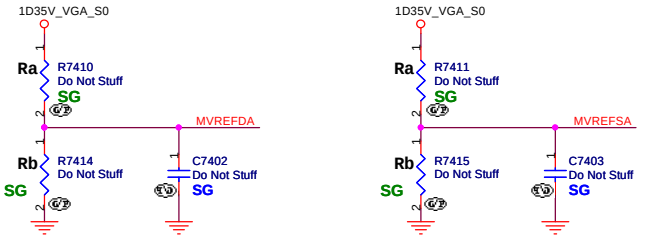
Title: GPU PCIE/STRAPPING

Size: Custom | Document Number: Cedar AMD BEEMA | Rev: A00

Date: Wednesday, March 05, 2014 | Sheet 73 of 104

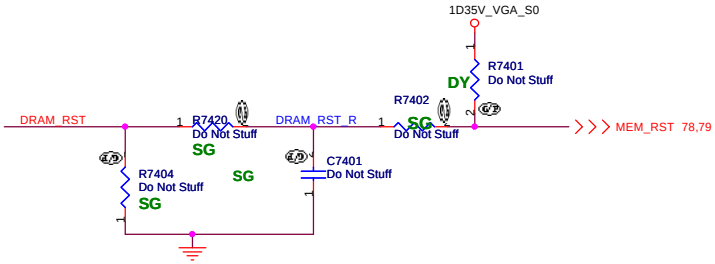


PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



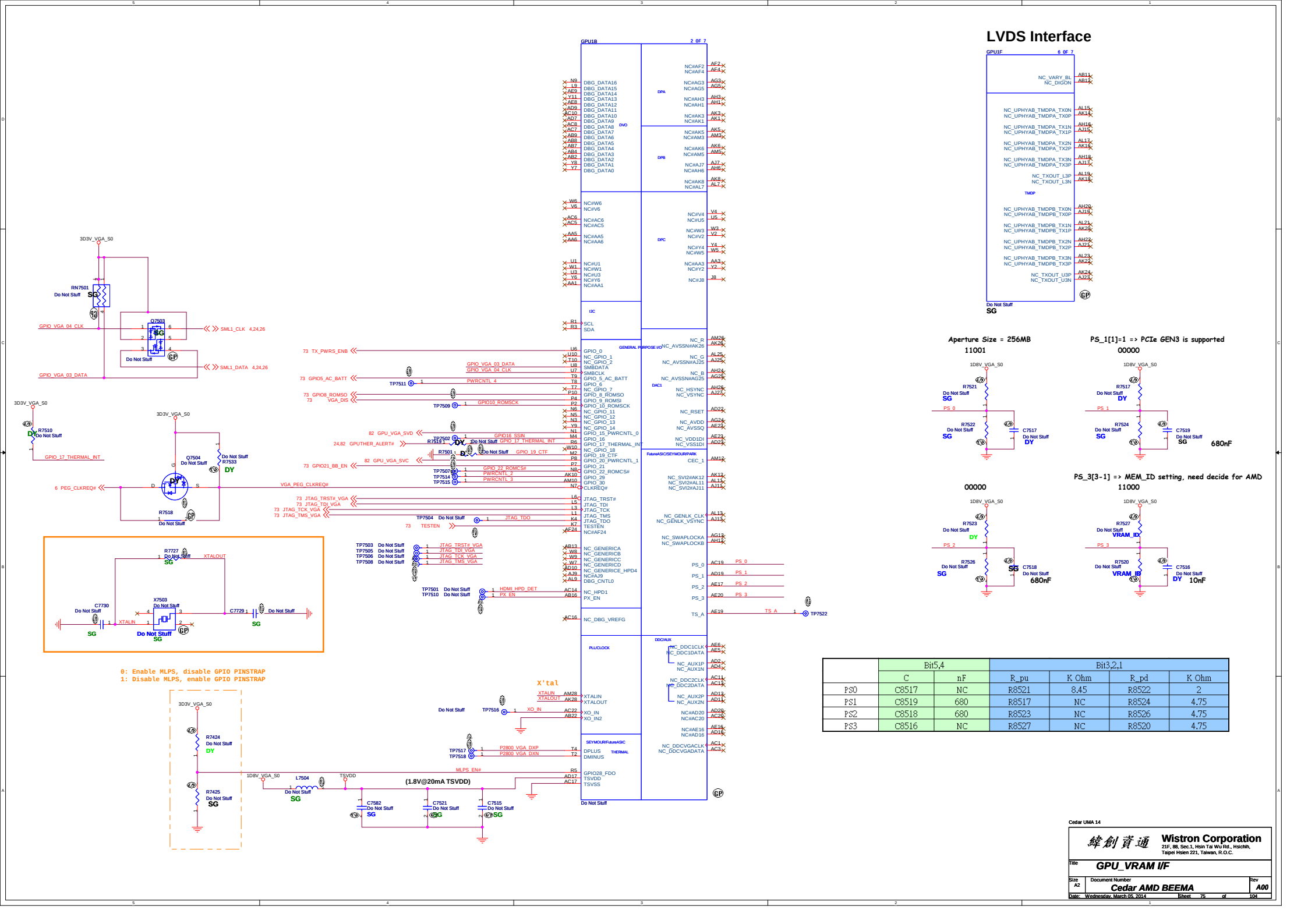
DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.35V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



Cedar UMA 14

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***GPU_Digitalout***		
Size: A3	Document Number: ***Cedar AMD BEEMA***	Rev: ***A00***
Date: Wednesday, March 05, 2014	Sheet 74 of 104	



	Bit5,4		Bit3,2,1			
	C	nF	R_pu	K Ohm	R_pd	K Ohm
PS0	C8517	NC	R8521	8.45	R8522	2
PS1	C8519	680	R8517	NC	R8524	4.75
PS2	C8518	680	R8523	NC	R8526	4.75
PS3	C8516	NC	R8527	NC	R8520	4.75

Cedar UMA 14

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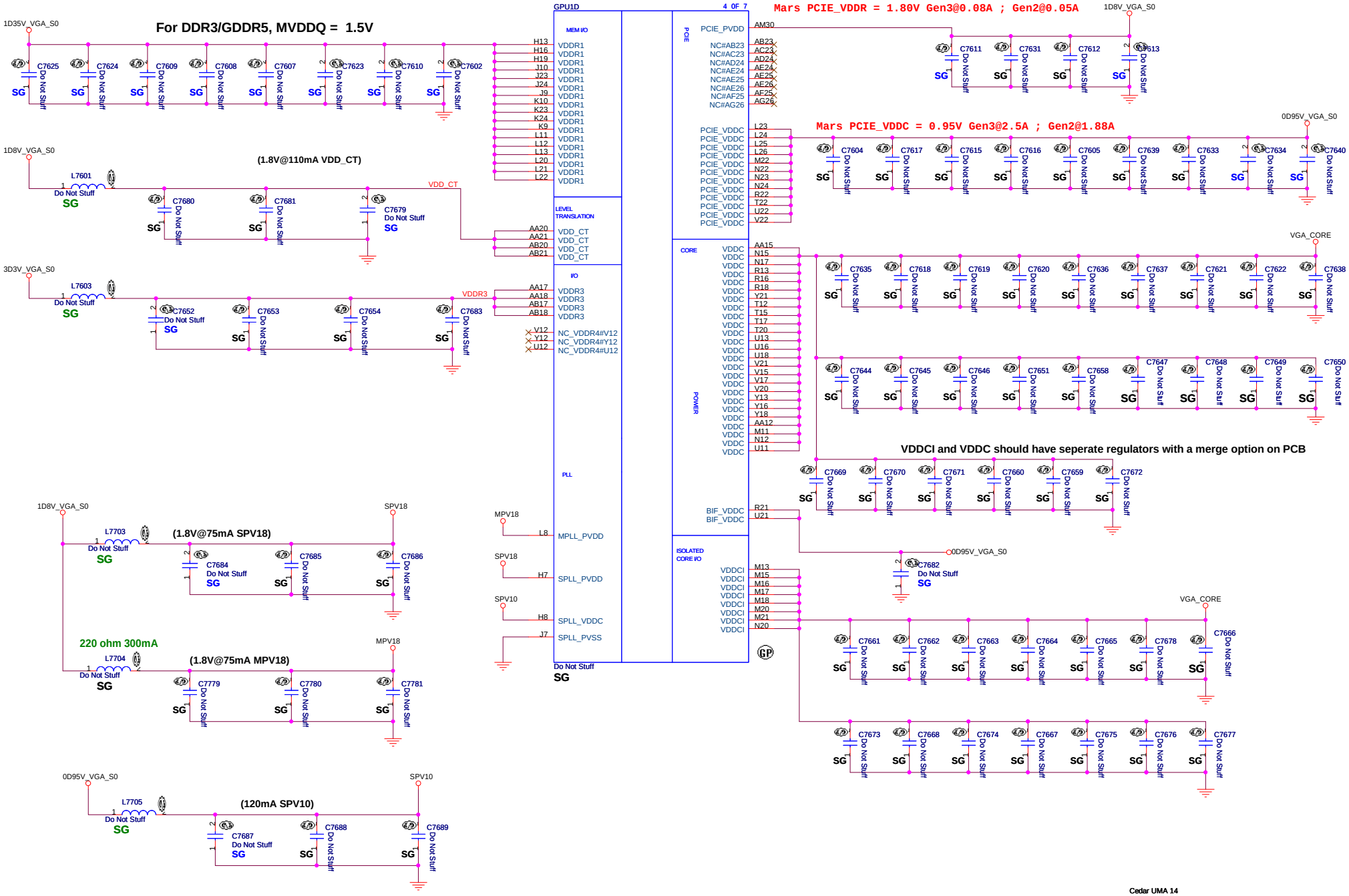
Title: **GPU_VRAM I/F**

Size: A2 | Document Number: **Cedar AMD BEEMA** | Rev: **A00**

Date: Wednesday, March 05, 2014 | Sheet 75 of 104


For DDR3/GDDR5, MVDDQ = 1.5V
Mars PCIE_VDDR = 1.80V Gen3@0.08A ; Gen2@0.05A
Mars PCIE_VDDC = 0.95V Gen3@2.5A ; Gen2@1.88A
(1.8V@110mA VDD_CT)
(1.8V@75mA SPV18)
(1.8V@75mA MPV18)
(120mA SPV10)
220 ohm 300mA
VDDCI and VDDC should have seperate regulators with a merge option on PCB
GPU1D
4 OF 7
1D35V_VGA_S0
1D8V_VGA_S0
0D95V_VGA_S0
3D3V_VGA_S0
VGA_CORE
VDD_CT
VDDR3
SPV18
MPV18
SPV10
Do Not Stuff
SG
Cedar UMA 14
Wistron Corporation
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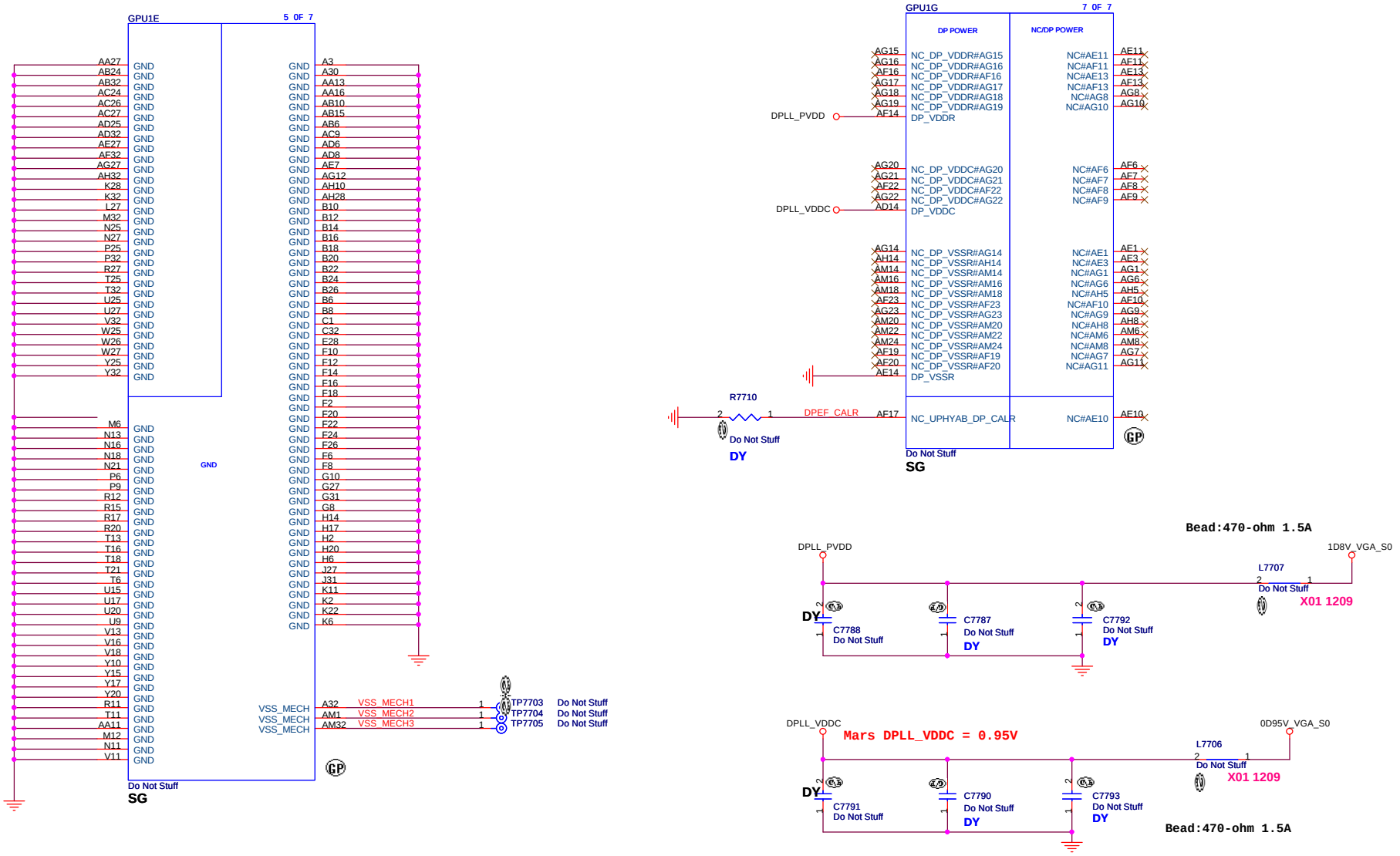
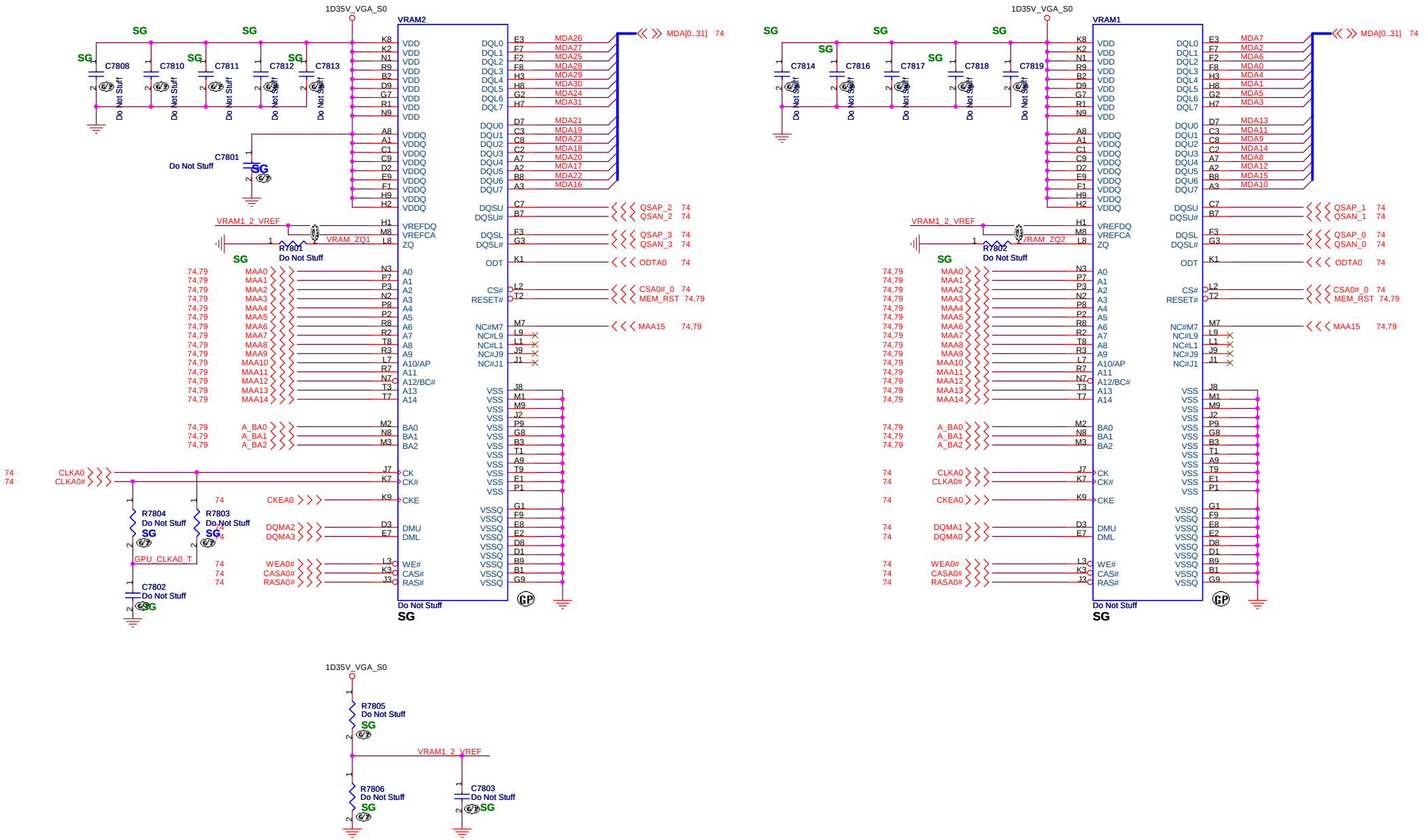
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU_GPIO/STRAP
Size
Custom
Document Number
Cedar AMD BEEMA
Rev
A00
Date: Wednesday, March 05, 2014
Sheet 76 of 104



Cedar UMA 14

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU_POWER/GND	
Size	Project Name: <Project Name>	Rev: <Rev>
Date: Wednesday, March 05, 2014	Sheet 77 of 104	



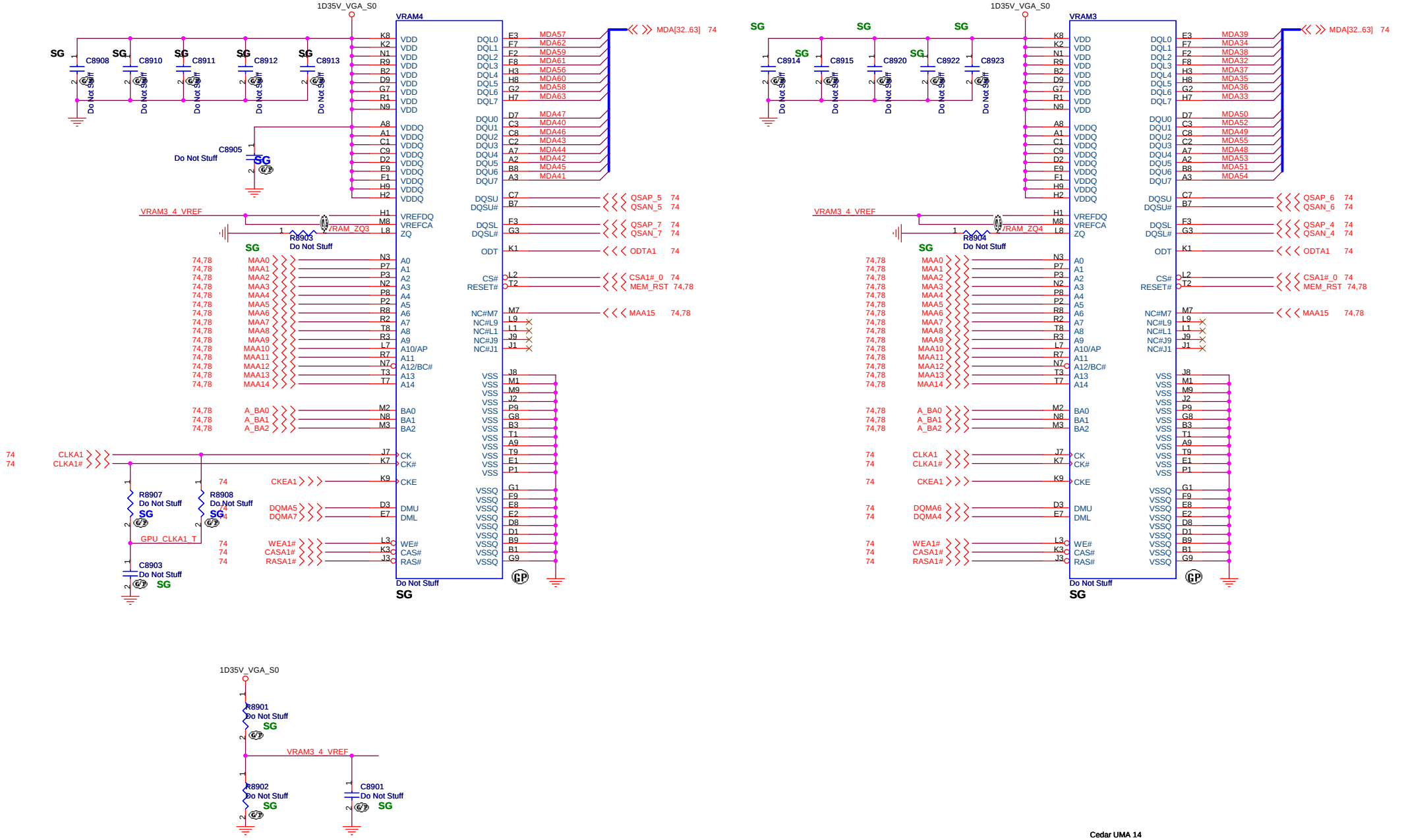
Cedar UMA 14

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
A3	Cedar AMD BEEMA	A00

Date: Wednesday, March 05, 2014 Sheet 78 of 104



Cedar UMA 14

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A3	Cedar AMD BEEMA	A00

Date: Wednesday, March 05, 2014 Sheet 79 of 104

Cedar UMA 14

緯創資通 **Wistron Corporation**
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Title

Reserved

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 80 of 104

Cedar UMA 14

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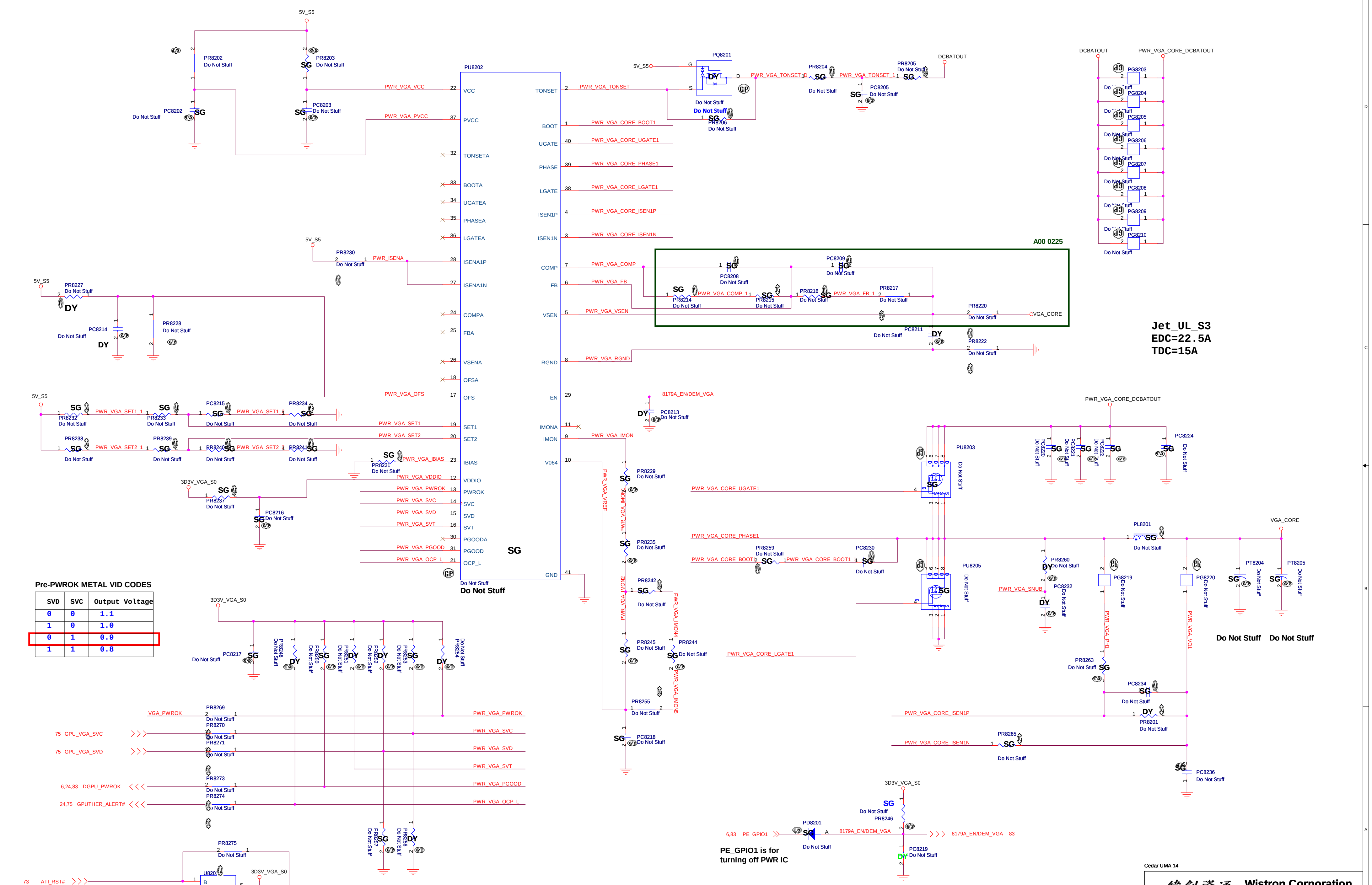
Title

Reserved

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 81 of 104



Pre-PWROK METAL VID CODES

SVD	SVC	Output Voltage
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8

PE_GPIO1 is for turning off PWR IC

```
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 0.36UH PCME064T-R36MS1R407 1.4mohm / Isat =24Arms 68.R3610.20W
O/P cap:CHIP CAP 470UF 2V EEFSX0D471X /Panasonic/  6mOhm / 79.47719.2BL
        CHIP CAP EL 330U 2.5V M6.3*4.4 3.5Arms Chemi-con/79.3371V.6CL
FET MOS /H/S: SIRA14DP /6.8mohm/8.5mohm / 2.9mOhm/3.5mohm@4.5Vgs / 84.A14DP.037
         L/S: SIRA06DP /6.8mohm/8.5mohm / 2.75mOhm/3.5mohm@4.5Vgs / 84.SRA06.037
```

Cedar UMA 14

緯創資通 Wistron Corporation
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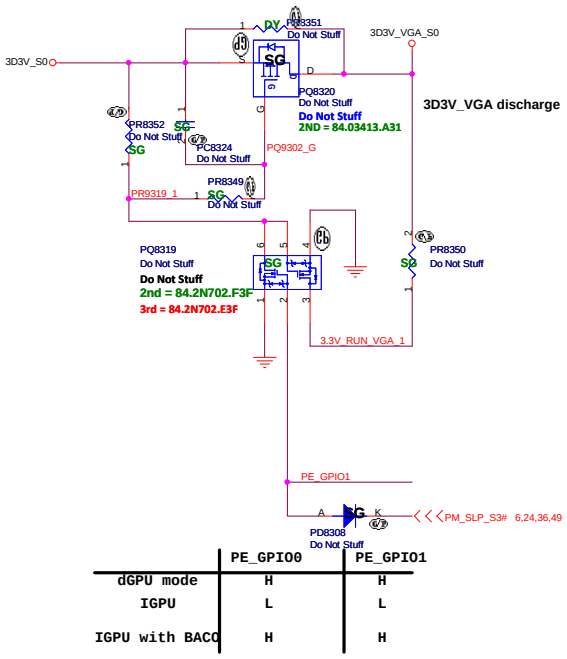
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8179A_VGACORE

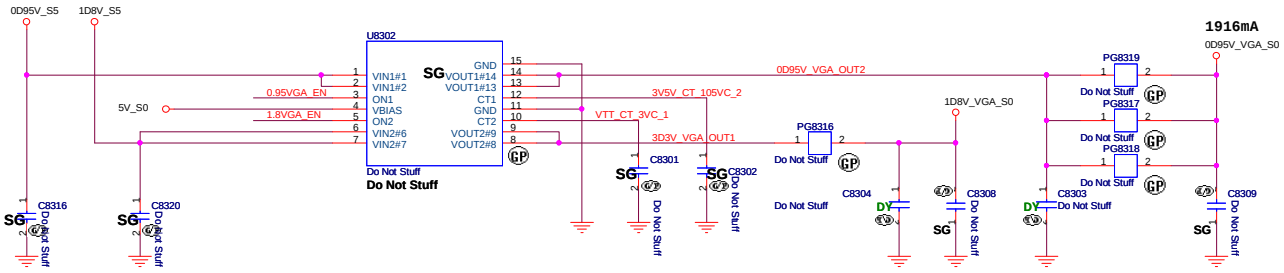
Size: A2 | Document Number: Cedar AMD BEEMA | Rev: A00

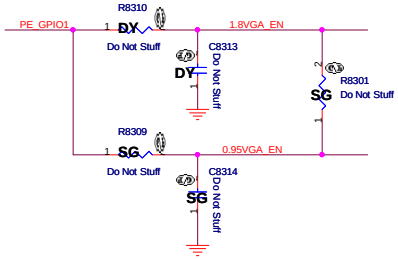
3D3V_S0 to 3D3V_VGA_S0 Transfer

Change DUMMY Reference Name to PX_BACO



	PE_GPIO0	PE_GPIO1
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H





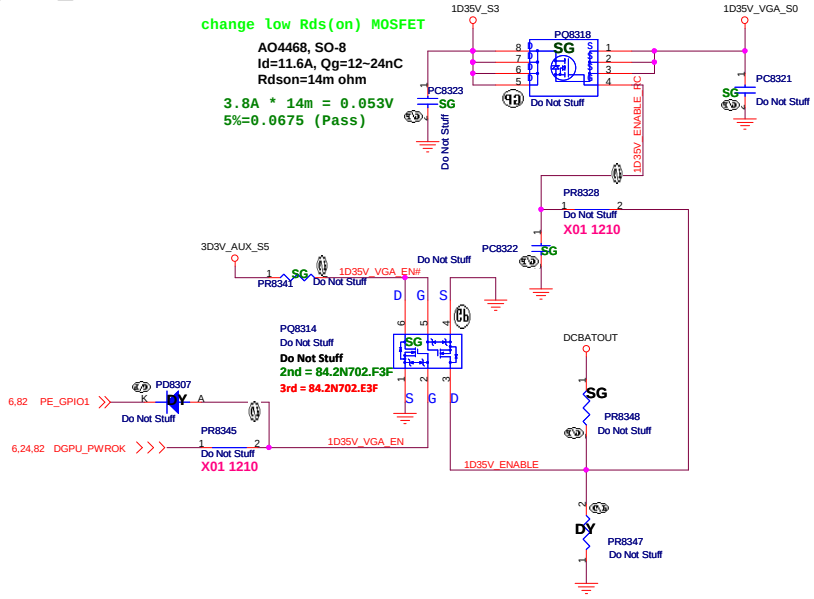
finally rising of 1.8_VGA_S0

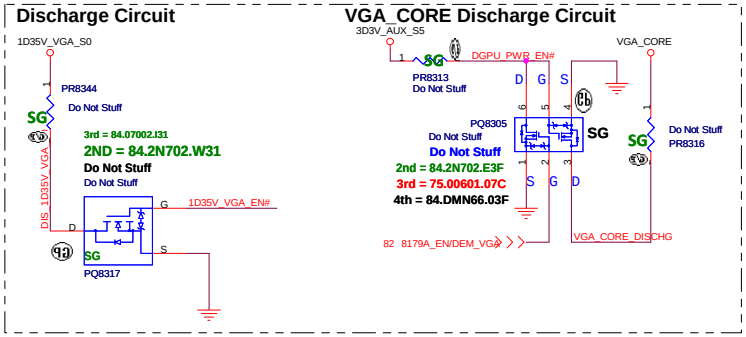
1D5V_VGA_S0

change low Rds(on) MOSFET

AO4468, SO-8
Id=11.6A, Qg=12~24nC
Rdson=14m ohm

3.8A * 14m = 0.053V
5%=0.0675 (Pass)





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Title: DISCRETE VGA POWER

Size: Custom | Document Number: Cedar AMD BEEMA | Rev: A00

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Cedar UMA 14

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 84 of 104

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Cedar UMA 14

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Title: ***(Reserved)***

Size	Document Number	Rev
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Date: Wednesday, March 05, 2014 Sheet 85 of 104

SSID = Mechanical

S1
Do Not Stuff
SG
Do Not Stuff
2nd = 34.4CK01.601
3rd = 34.4CK01.501

S2
Do Not Stuff
SG
Do Not Stuff
2nd = 34.4CK01.601
3rd = 34.4CK01.501

H2
Do Not Stuff
GP
Do Not Stuff

H5
Do Not Stuff
Do Not Stuff

H6
Do Not Stuff
Do Not Stuff

H1
Do Not Stuff
GP
Do Not Stuff

H3
Do Not Stuff
GP
Do Not Stuff

H4
Do Not Stuff
GP
Do Not Stuff

SPR2
SPRING-102-GP
34.41V01.001

SPR5
SPRING-102-GP
34.41V01.001

X02 0206
SPR4
SPRING-43-GP-U
34.15J03.001

SPR6
SPRING-57-GP
34.42T14.002

C1
Do Not Stuff
Do Not Stuff

C2
Do Not Stuff
Do Not Stuff

C3
Do Not Stuff
Do Not Stuff

SSID = EMI

DCBATOUT
DY EC9701 Do Not Stuff
DY EC9703 Do Not Stuff
EC9704 SCD1U25V2KX-GP
EC9708 SCD1U25V2KX-GP
EC9705 SCD1U25V2KX-GP
EC9707 DY Do Not Stuff
EC9709 DY Do Not Stuff
EC9710 DY Do Not Stuff
EC9717 SCD1U25V2KX-GP
DY EC9711 Do Not Stuff
EC9712 SCD1U25V2KX-GP
DY EC9713 Do Not Stuff
DY EC9716 Do Not Stuff
DY EC9715 Do Not Stuff
EC9714 DY Do Not Stuff

1D35V_VGA_S0
EC9727 DY Do Not Stuff
EC9725 DY Do Not Stuff
EC9726 DY Do Not Stuff
EC9730 DY Do Not Stuff
EC9728 DY Do Not Stuff
EC9729 DY Do Not Stuff
EC9731 DY Do Not Stuff

AUD_AGND
EC9739 DY Do Not Stuff
EC9744 DY Do Not Stuff
EC9743 DY Do Not Stuff
EC9745 DY Do Not Stuff

DCBATOUT
EC9740 SCD1U25V2KX-GP
EC9741 SCD1U25V2KX-GP
DY EC9742 Do Not Stuff
DY EC9747 Do Not Stuff
EC9748 SCD1U25V2KX-GP
EC9749 SCD1U25V2KX-GP

5V_S0
EC9720 DY Do Not Stuff
EC9719 DY Do Not Stuff
EC9718 DY Do Not Stuff
EC9723 DY Do Not Stuff
EC9721 DY Do Not Stuff
EC9722 DY Do Not Stuff
EC9724 DY Do Not Stuff

3D3V_S0
EC9737 DY Do Not Stuff
EC9735 DY Do Not Stuff
EC9736 DY Do Not Stuff
EC9738 DY Do Not Stuff

5V_S5
EC9734 DY Do Not Stuff
EC9732 DY Do Not Stuff
EC9733 DY Do Not Stuff

Cedar UMA 14

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Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	Cedar AMD BEEMA	A00

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Cedar UMA 14

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Title: ***NFC(Reserved)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 87 of 104

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Cedar UMA 14

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPM/TCM***

Size: A3 | Document Number: **Cedar AMD BEEMA** | Rev: **A00**

Date: Wednesday, March 05, 2014 | Sheet 88 of 104

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Cedar UMA 14

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TEST PAD

Size: C | Document Number: Cedar AMD BEEMA | Rev: A00

Date: Wednesday, March 05, 2014 | Sheet 90 of 104

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Cedar UMA 14

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 91 of 104

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Cedar UMA 14

緯創資通 **Wistron Corporation**
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Title: ***(Reserved)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

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Cedar UMA 14

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

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Cedar UMA 14

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

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Cedar UMA 14

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 95 of 104

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Cedar UMA 14

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Wistron Corporation
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Title: ***MCP CPU XDP HDT+***

Size	Document Number	Rev
A3	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 96 of 104

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4

3

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2

1

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Title: ***Table of Content***

Size	Document Number	Rev
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Cedar UMA 14

緯創資通

Wistron Corporation
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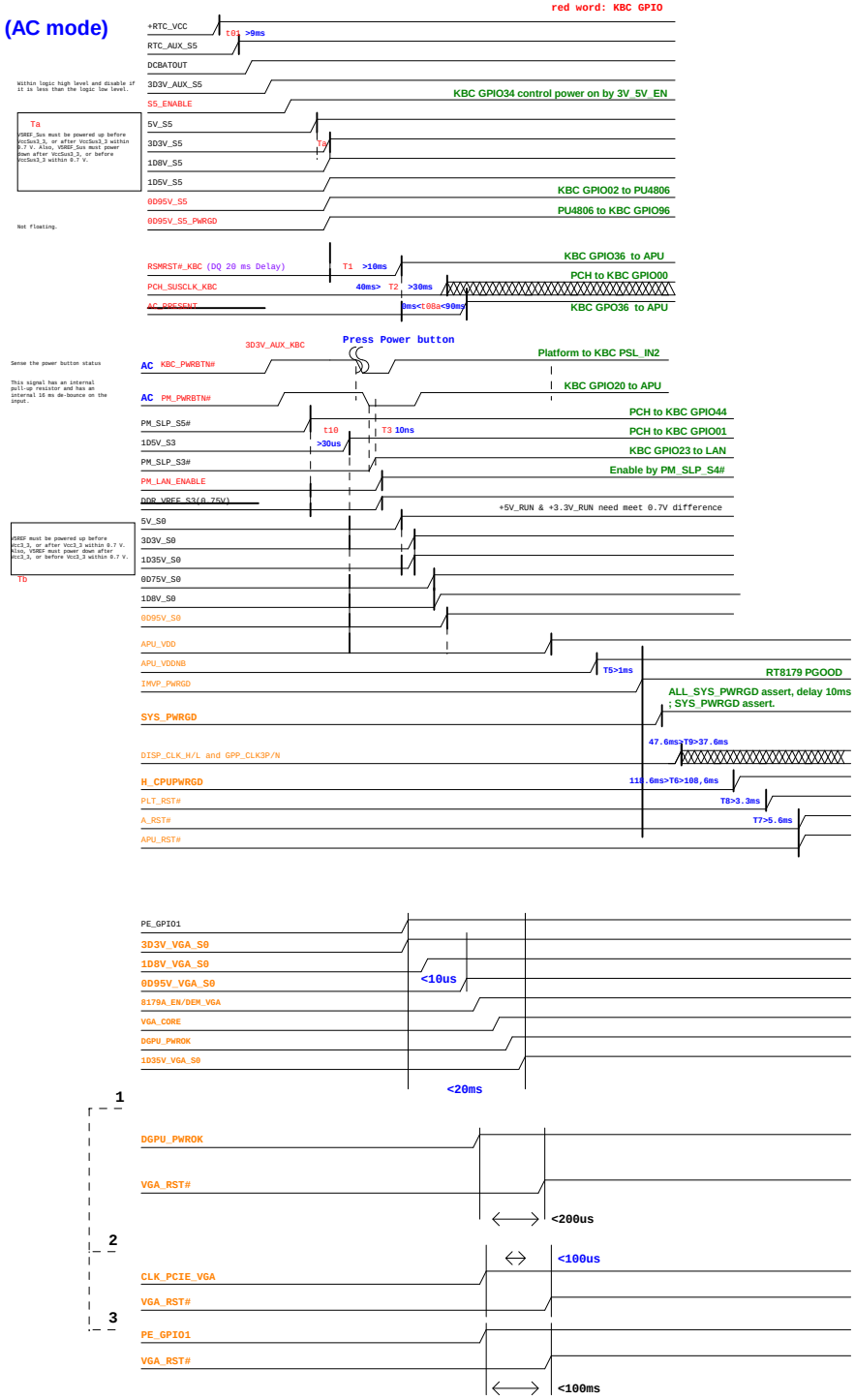
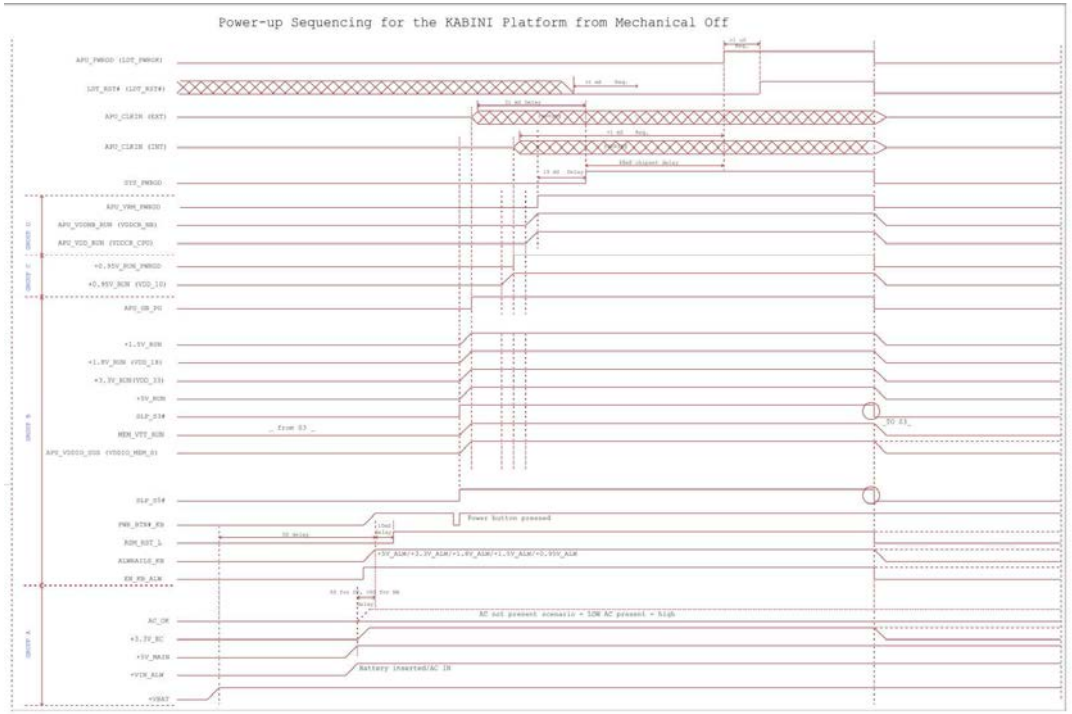
Title: ***Change History***

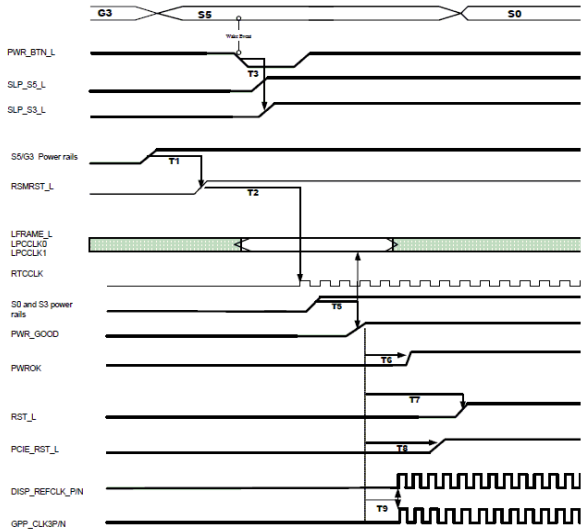
Size	Document Number	Rev
A3	**Cedar AMD BEEMA**	**A00**

Date: Wednesday, March 05, 2014 Sheet 98 of 104

Beema Platform Power Sequence

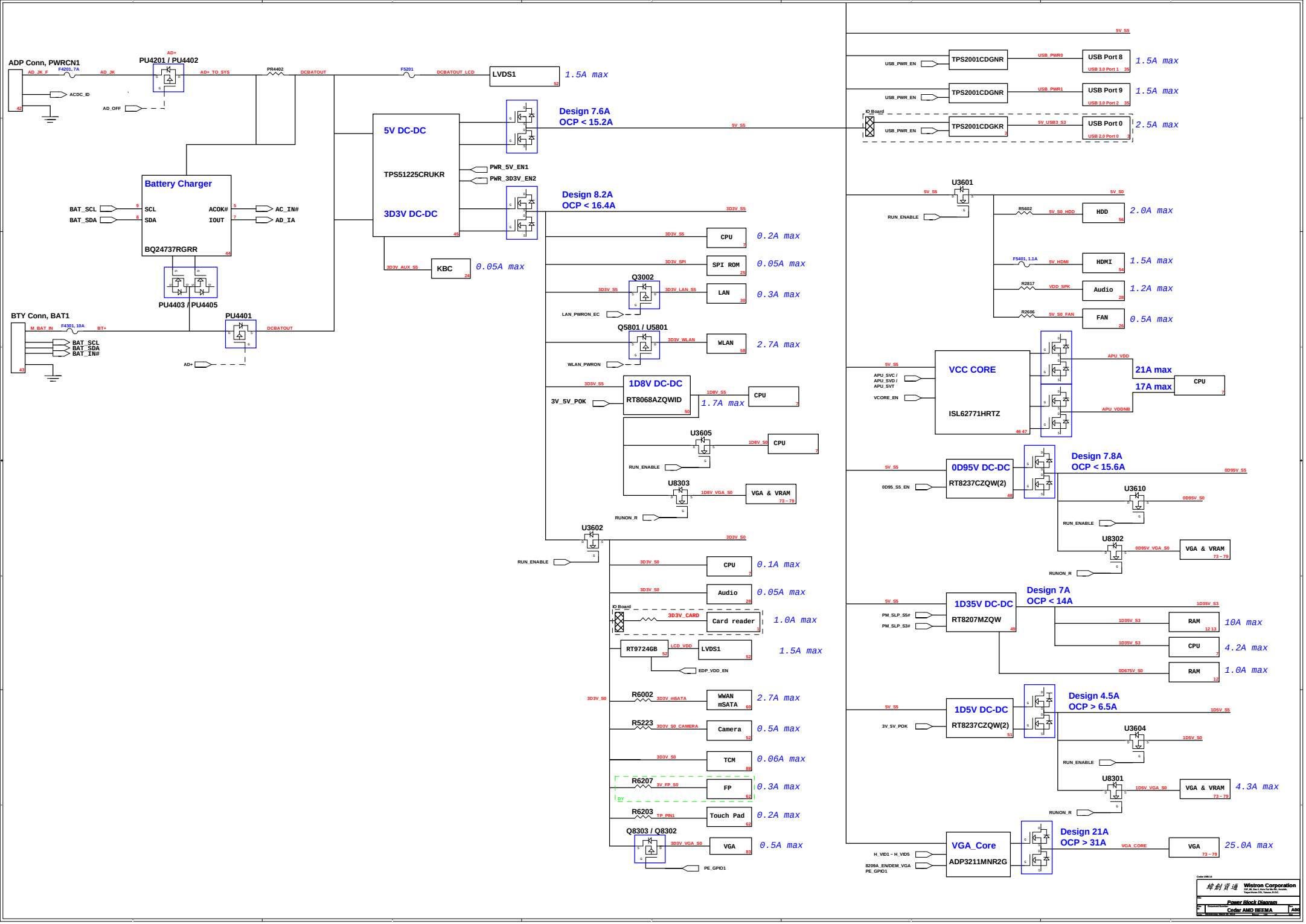




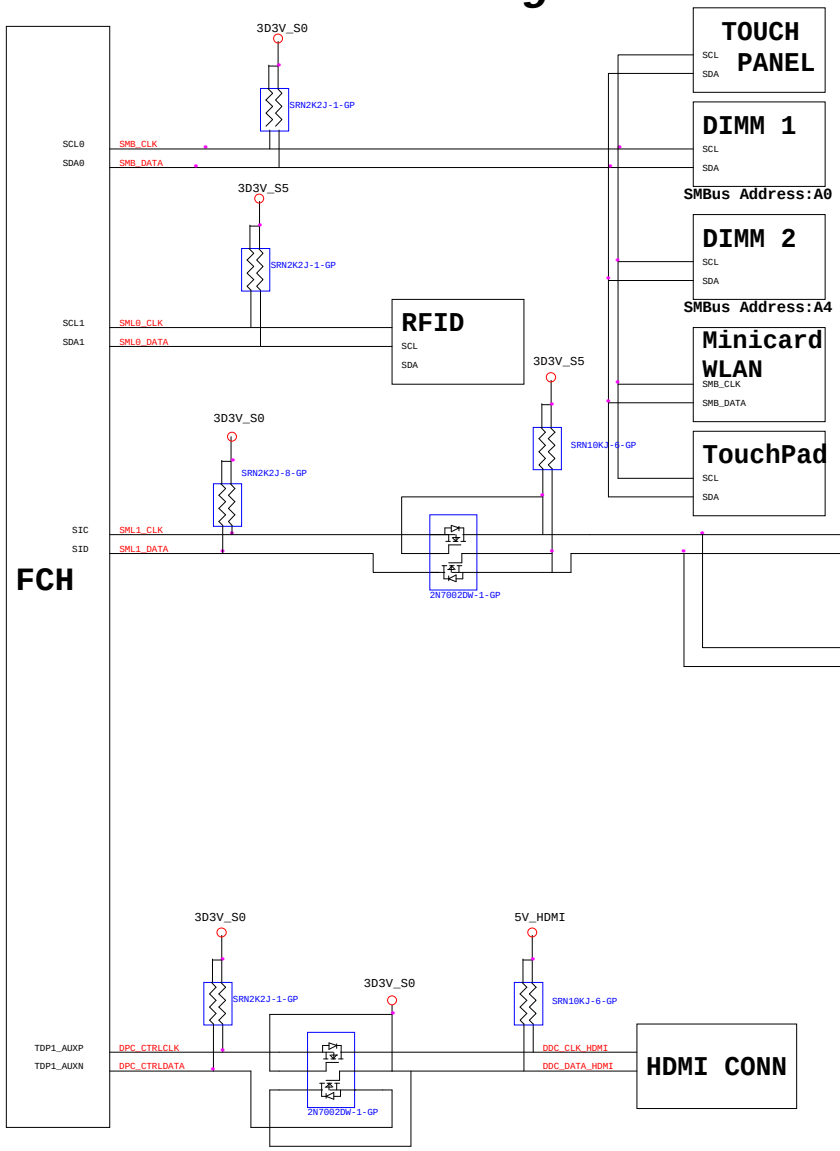


Cedar UMA 14

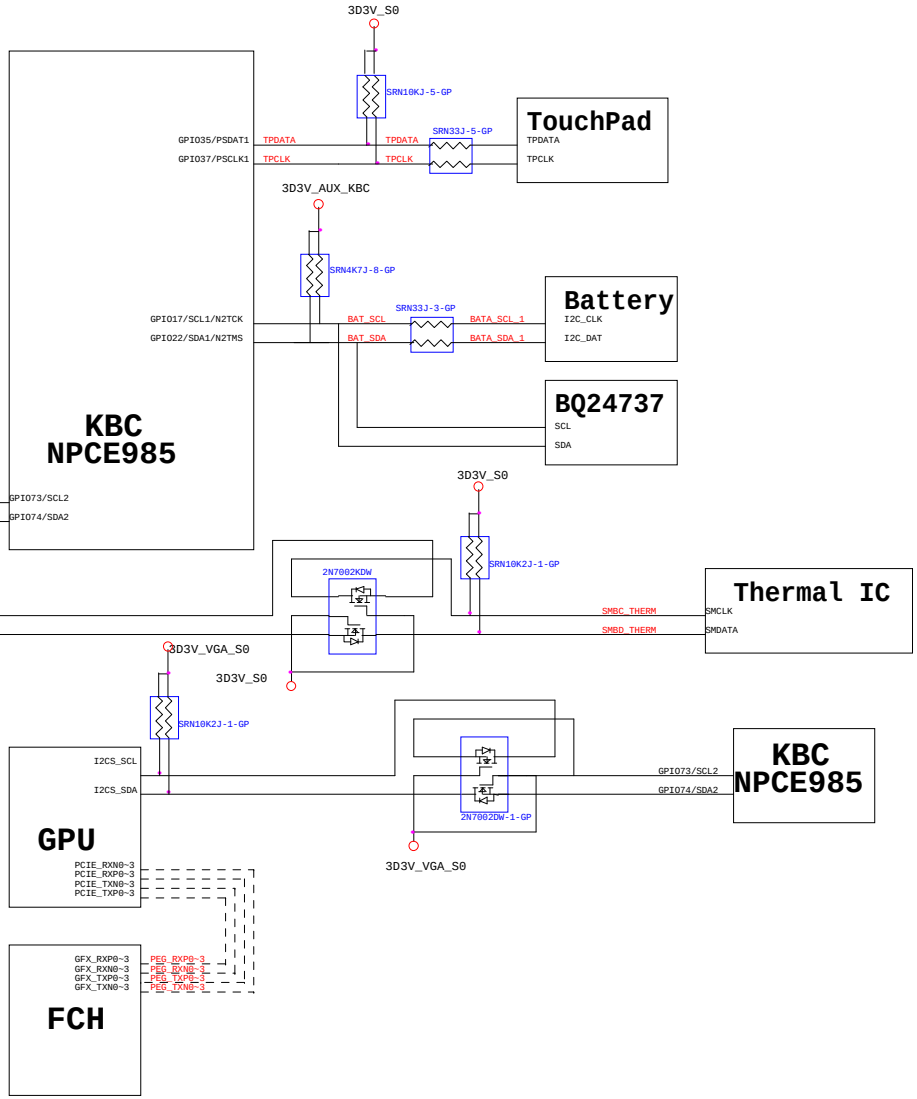
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Power Sequence		
Size: A1	Document Number: Cedar AMD BEEMA	Rev: A00
Date: Wednesday, March 05, 2014	Sheet 99 of 104	


ADP Conn, PWRCN1
PU4201 / PU4402
AD_JK_F
F4201, 7A
AD_JK
AD+_TO_SYS
PR4402
DCBATOUT
FS201
DCBATOUT_LCD
LVDS1
1.5A max
ACDC_ID
AD_OFF
Battery Charger
BAT_SCL
BAT_SDA
SCL
SDA
ACOK#
IOUT
AC_IN#
AD_IA
BQ24737RGRR
PU4403 / PU4405
BTY Conn, BAT1
M_BAT_IN
F4301, 10A
BT+
BAT_SCL
BAT_SDA
BAT_1N#
PU4401
5V DC-DC
TPS51225CRUKR
3D3V DC-DC
PWR_5V_EN1
PWR_3D3V_EN2
Design 7.6A
OCP < 15.2A
Design 8.2A
OCP < 16.4A
3D3V_AUX_S5
KBC
0.05A max
CPU
0.2A max
SPI ROM
0.05A max
Q3002
LAN
0.3A max
LAN_PWRON_EC
Q5801 / U5801
WLAN
2.7A max
WLAN_PWRON
1D8V DC-DC
RT8068AZQWID
3V_5V_POK
1.7A max
U3605
RUN_ENABLE
U8303
VGA & VRAM
RUNON_R
U3602
0.1A max
Audio
0.05A max
IO Board
Card reader
1.0A max
RT9724GB
LVDS1
1.5A max
EDP_VDD_EN
R6002
WWAN mSATA
2.7A max
R5223
Camera
0.5A max
TCM
0.06A max
R6207
FP
0.3A max
DY
R6203
Touch Pad
0.2A max
Q8303 / Q8302
VGA
0.5A max
PE_GPIO1
TPS2001CDGNR
USB Port 8
1.5A max
USB Port 9
1.5A max
TPS2001CDGKR
USB Port 0
2.5A max
U3601
RUN_ENABLE
RS602
HDD
2.0A max
F5401, 1.1A
HDMI
1.5A max
R2817
Audio
1.2A max
R2606
FAN
0.5A max
VCC CORE
ISL62771HRTZ
APU_SVC / APU_SVD / APU_SVT
VCORE_EN
APU_VDD
APU_VDDNB
21A max
17A max
0D95V DC-DC
RT8237CZQW(2)
0D95_S5_EN
Design 7.8A
OCP < 15.6A
U3610
U8302
1D35V DC-DC
RT8207MZQW
PM_SLP_S5#
PM_SLP_S3#
Design 7A
OCP < 14A
RAM
10A max
CPU
4.2A max
1.0A max
1D5V DC-DC
RT8237CZQW(2)
Design 4.5A
OCP > 6.5A
U3604
U8301
4.3A max
VGA_Core
ADP3211MNR2G
H_VID1 ~ H_VID5
8209A_EN/DEM_VGA
Design 21A
OCP > 31A
VGA_CORE
25.0A max
Wistron Corporation
Power Block Diagram
Cedar AMD BEEMA

PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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Custom	Cedar AMD BEEMA	A00

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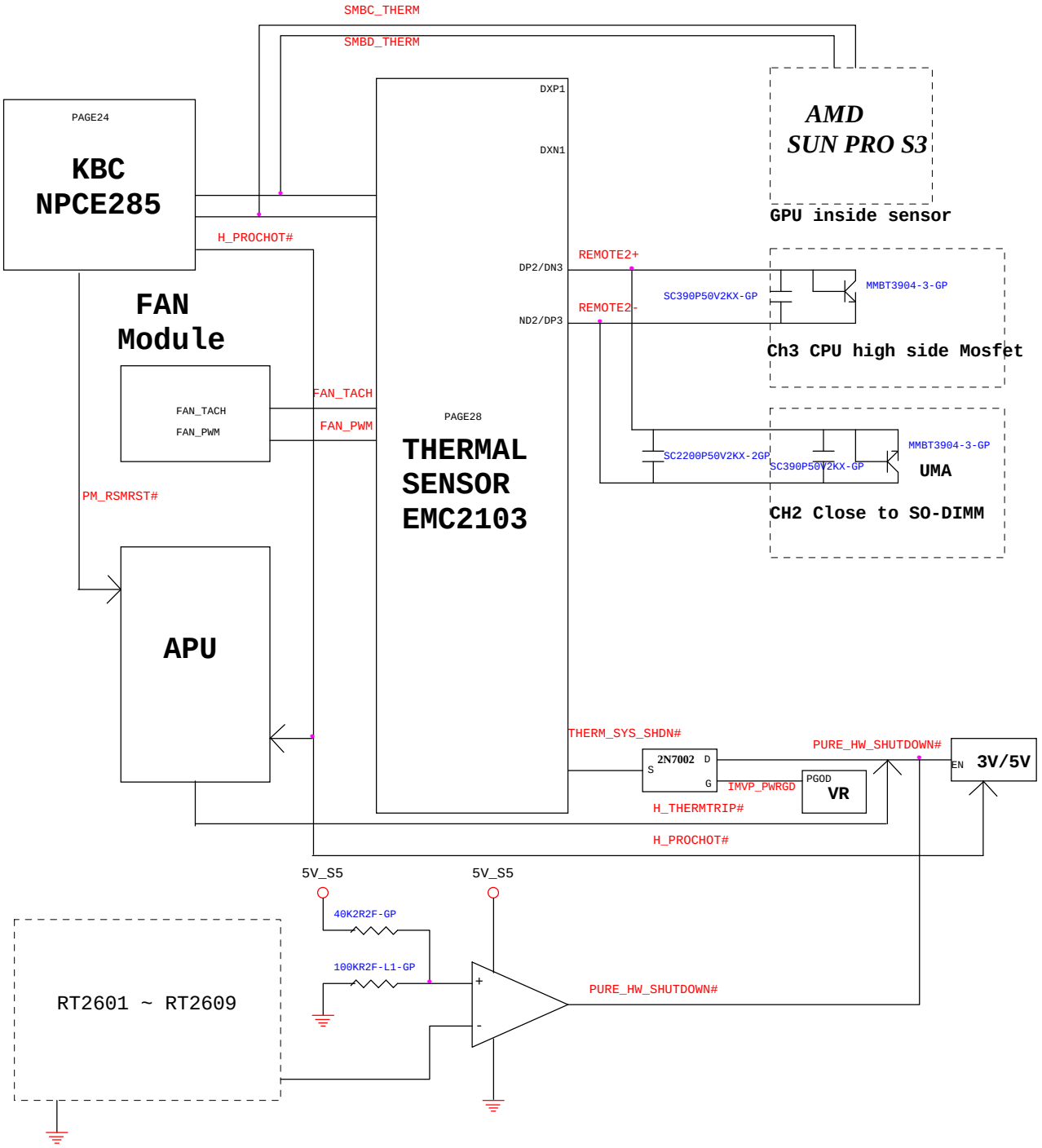
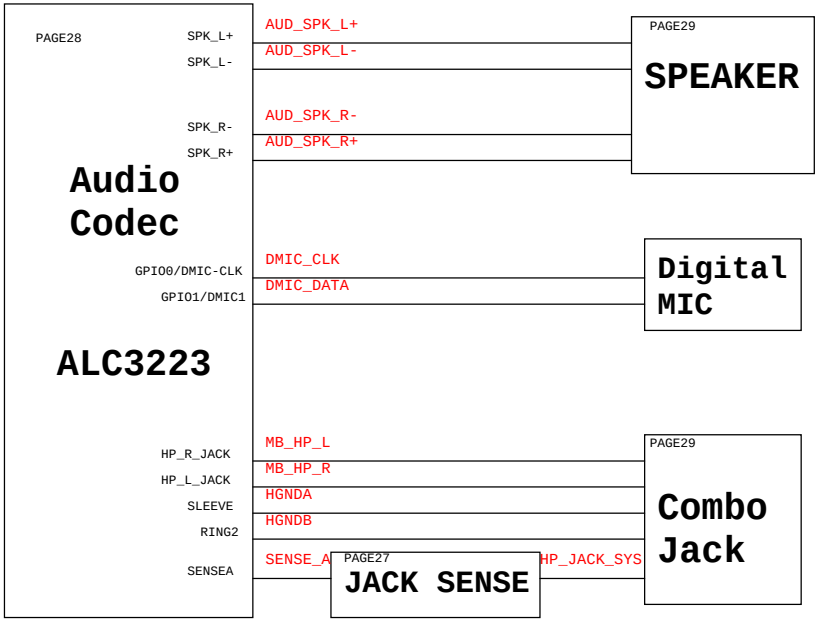
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram		
Size: Custom	Document Number: Cedar AMD BEEMA	Rev: A00
Date: Wednesday, March 05, 2014	Sheet 102 of 104	

Change notes -

	VERSON	DATE	Page	Modify List	OWNER
	X01	2013/12/3	83	R8309 = 15Kohm ,C8301/C8313 = DY,C8302 = 1000pF	
	X01	2013/12/3	43 44	RN4301 to 100ohm, AC_IN# change to Pull-H 3D3V_AUX_S5(PR4434)	
	X01	2013/12/3	27	HDA27 change from ALS3223 to ALC3234	
	X01	2013/12/3	24 25	Swap BATT_WHITE_LED# and EC_BRIGHTNESS. BATT_WHITE_LED# to GPIO13 and EC_BRIGHTNESS to GPIO15. Change R2404 from 10K to 20K ohm for PCB VERSION strap , Del SKT25	
	X01	2013/12/3	52	Reserve 0805 0 ohm R5211 between LCDVDD and LCD1.F5201 change from 69.50007.A31 to 69.60040.001	
	X01	2013/12/3	Power	Change C5205,EC4304,EC4601,PC4409,PC4419,PC4511.PC4518,PC4524,PC4720,PC4722,PC4827, PC4913 to 78.10422.2BL (0.1U 25V K0603 X7R) from 78.10424.2BL (0.1U 50V K0603 X7R).	
	X01	2013/12/3	54 55	Add HDMI SMBUS use 0 ohm DUMMY co-lay ,Add Hsync Vsync 0ohm DUMMY co-lay	
	X01	2013/12/3	29	Change HPMIC1 to 022.10002.0001 from 22.10270.G61 SPK1 change to 20.F1639.004	
	X01	2013/12/3	34 63	Change USB1 to 22.10341.Q21 / Change KBLIT1 to 20.K0800.004	
	X01	2013/12/3	19 26	Change C1904 and C1905 from 10pf to 6.8pf / Q2601 RN2602 DUMMY, RN2601 install	
	X01	2013/12/3	30	R3004 CLK_LAN_REQ0#_R change pull high to 3D3V_S0	
	X01	2013/12/3	EMI	DMIC_CLK mount R2716 100ohm resistance,Mount EC9749,Mount EC4304	
	X01	2013/12/3	58	CARD_WLAN_OUT# and CARD_WPAN_OUT# modify to TP change WLAN1 to 62.10043.I81	
	X01	2013/12/3	42 51	DCIN1 change to 20.F1783.007,Del 1D5V_S5 circuit	
	X01	2013/12/4	24 34 35	R2447 change to 63.10334.1DL,Del U3502 and U3501,swap the net U3403.1 and U3403.3	
	X01	2013/12/5	42 46 24 26	Del AFTP3804 AFTP3807, Modify AFTP6241 Add AFTP6242,Change R2447 to 1K , R2622 change to 24.3K	
	X01	2013/12/6	24	R2411 DY D2401 install	
	X01	2013/12/9	31 47 82	RJ45 connector change to 022.10001.0551, PT4701 /PT4704/PT8204 change to 79.3371V.6CL	
	X01	2013/12/10	EMI	Mount EC4303 and change to 0.1u Mount EC9705 EC9748 EC9717 EC9740 EC9741 EC9712 EC9704 EC9708 and change to 0.1u Mount R5415、R5417、R5416、R5414 150ohm resistance Mount TR3401、TR3404、TR6301(69.10103.041、69.10080.011) Mount TR5208、TR5209(69.10103.041、69.10080.011) Mount EC2705、EC2703、EC9739、EC9743、EC9744 0.1u cap Mount SPR2、SPR5、SPR6	
	X01	2013/12/10	0 ohm	change 0 ohm to short pad	
	X01	2013/12/10	54 55	R5501/R5502 change to 33 ohm / Del D5402	
	X01	2013/12/10	24 52 62	R2411 Install D2401 DUMMY ,R5207 BOM control ,BOM control DVC50 to Janus	
	X01	2013/12/12	46 86 62	PR4609 change to 44.2K (64.44225.6DL) from short pad, EMI:Add SPR6(34.42T14.002),KBLIT DUMMY	
	X01	2013/12/16	55 Power	Del CRT circuit / Modify power schematic BOM	
	X01	2013/12/18	Power	PR8214 change to 499K (64.49935.6DL) / PR8215 change to 9.76K (64.97615.6DL)	

Cedar UMA 14

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Title: **Change List**

Size: A3 | Document Number: **Cedar AMD BEEMA** | Rev: **A00**

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Change notes -

	VERSON	DATE	Page	Modify List	OWNER
	X02	2014/01/21	48	Change PR4823 to 26.1K. The voltage about 0.97V	
	X02	2014/01/21	83	R8310 change 15Kohm /C8313 change 0.1uF /C8301 change 470pF Add R8301 for power sequence	
	X02	2014/01/27	12,46	EMC request:change EC4601,C1217,C1225,C1214 to 0.1u	
	X02	2014/01/27		Change 0 ohm to short pad	
	X02	2014/01/27	6	DGPU_PRESENT# pull hi to 3D3V_S0	
	X02	2014/01/28	power	1. PD4201 change 1st source to 83.P6SBM.AAG and 2nd source to 83.P6SBM.DAG . 2. PC4202 PC4409 PC4419 PC4519 PC4524 PC4511 PC4513 PC4518 PC4734 PC4720 PC4722 PC4736 PC4833 PC4827 PC4919 PC4913 PC8230 change to 78.10424.2BL. 3. PC4201 change to 78.10594.41L. 4. PC4916,PC4917 change to 78.10610.5BL. 5. PC4408 change to 78.47522.51L (4.7U 25V K0805 X5R). 6. PC4425 change to 78.10324.2FL (0.01U 50V K0402 X7R). 7. PC4512 change to 78.47522.51L (4.7U 25V K0805 X5R). 8. Delete PC4814/PC4714. 9. Dummy PC4718/PC4912/PC4920/PC4204/PC4205/ PC4426/PC4416/PC4830 10.PC4828 change to 78.47522.51L (4.7U 25V K0805 X5R). 11.PC4909 and PC4911 change to 78.47522.51L (4.7U 25V K0805 X5R).	
	X02	2014/01/28	31	change XF3101 and XF3102 to 68.68167.30D and Swap net	
	X02	2014/02/06	06 19	Change RN1901 R1901 from short pad to 0 ohm Change RN604 to 66.10336.08L	
	X02	2014/02/06	86	Change SPR4 P/N to 34.15J03.001	
	X02	2014/02/07	26	THM26 DUMMY, Add R2602 for VD_OUT1# connect PURE_HW_SHUTDOWN#	
	A00	2014/02/25		Change PR4911 PR4649 R3016 R6209 R1901 RN5404 RN1901 to short pad	
	A00	2014/02/25	82	Modify schematic PWR_VGA_COMP connecte to PWR_VGA_FB	
	A00	2014/02/25	24	PCB VERSION A/D(PIN98) R2404 change to 64.64925.6DL	
	A00	2014/02/25	54	Install D5401 RN5401 Q5402, Dummy RN5404	

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Title: Change List

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