Compal Confidential

G400S/G500S DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

nVIDIA N14X

LA-9901P

2013-03-20

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Title: Cover Page

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

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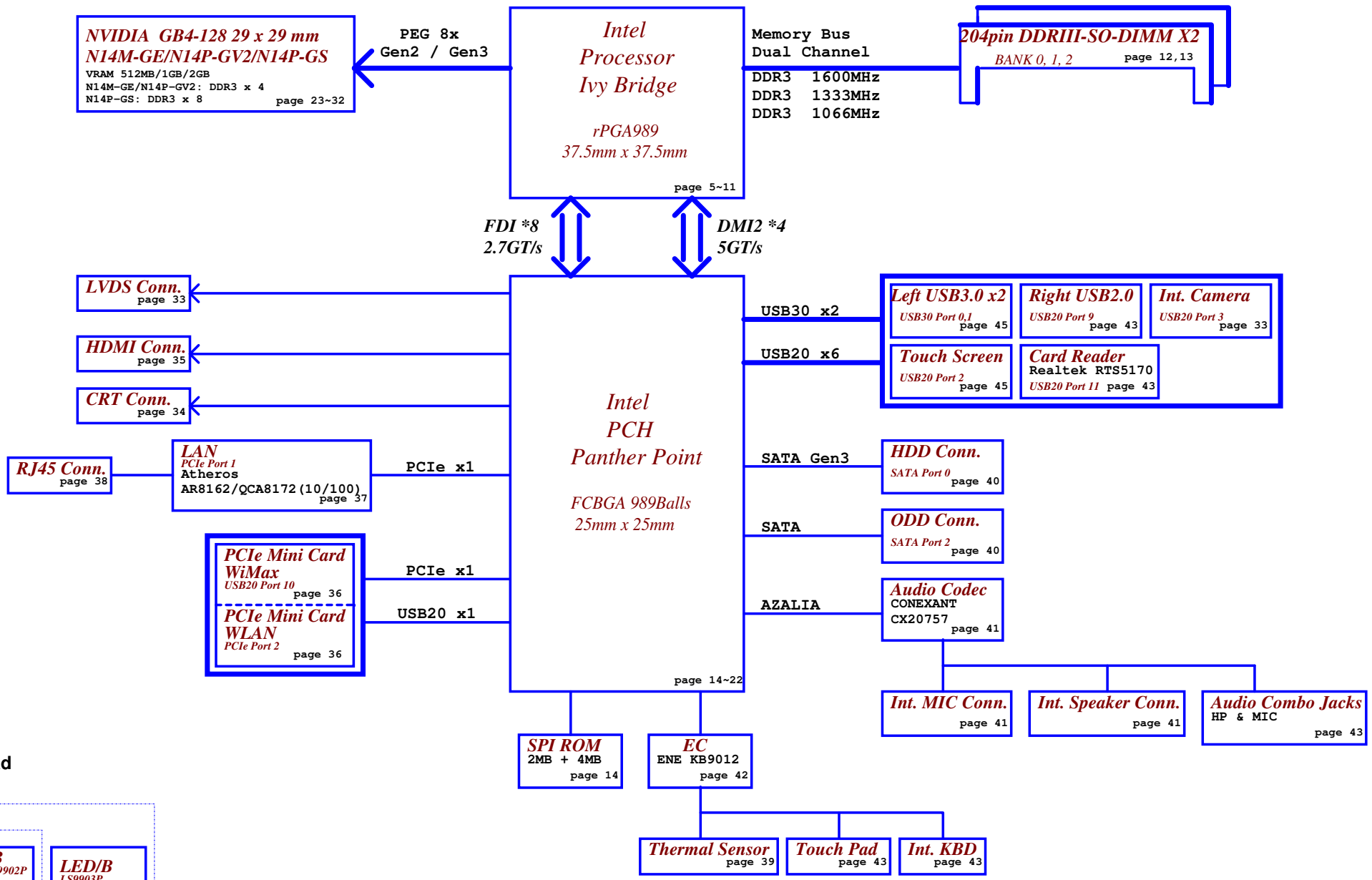
Chief River



Sub-borad

15"

14"

- Power/B LS9902P page 43
- LED/B LS9903P page 43
- IO/B LS9901P page 43
- ODD/B LS9904P page 40

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Title: MB Block Diagram

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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	1.0
1	0.3
2	0.2
3	0.1
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID table for AD channel

Vcc	3.3V
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0.300 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30	EVT

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001 100xb

PCH SM Bus address

Device	Address
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	V +3VS_VGA	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS_VGA	X	V +3VS	X	X	V +3VS	X

USB Port Table

	USB 2.0 Port		3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Touch Screen
		3	USB Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB/B (Right Side USB2.0)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
45 LEVEL	45@
Connector	ME@
For VILG2 (14")	14@
For VILG1 (15")	15@
GPU:N14M-GE	N14@
HDMI	HDMI@
Camera	CMOS@
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
10/100 LAN(AR8162L)	8162@
10/100 LAN(QCA8172)	8172@
N14M-GE SKU	GE@
N14P-GS SKU	GS@
N14P-GV2 SKU	GV2@
N14P-GV2&N14P-GS SKU	GVGS@
Green clock(DIS sku)	GCLK304@
Green clock(UMA sku)	GCLK244@
Green clk support	GCLK@
No Green clk support	NOGCLK@
Nvidia GC6 state	GC6@
Touch Screen SKU	TS@
Optimus SKU	OPT@
UMA SKU	UMA@
PCH(NM70 sku)	NM70@
PCH(HM70 sku)	HM70@
PCH(HM76 sku)	HM76@
VRAM(1000MHz)	1000M@
VRAM(900MHz)	900M@
Unpop	@

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Title: Notes List

Size: B | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

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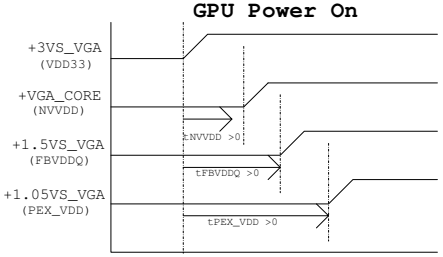
N14x GPIO Pin Definition Table

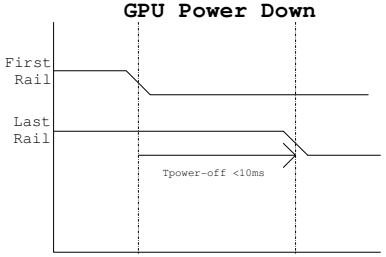
Pin Name	Normal Function	I/O	Functional Description	Default PU/PD
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID:Strap to boot FBVDD/Q
GPIO2~4	Non-support for LCD	O	Panel	100k PD
GPIO5	Reserve			
GPIO6	FB_CLAMP_TGL_REQ#	O	Active low FB Clamp toggle request	
GPIO7	3DVision	O	3D Vision L/R signal	100k PD
GPIO8	OVERT	IO	Active Low Thermal Catastrophic Over Temperature	100k PU
GPIO9	ALERT	IO	Active Low Thermal Alert	100k PU
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100k PD
GPIO11	PWM_VID	O	GPU Core VDD PWM control supply overdraw input	
GPIO12	PWR_LEVEL	I	AC power detact or control signal	100k PU
GPIO13	PSI	O	Phase Shedding	PSI:100k PU to enable two phase
GPIO14~19	Non-support for HDA	I	Hot Plug	
GPIO20~21	Reserve			

GPU Power On



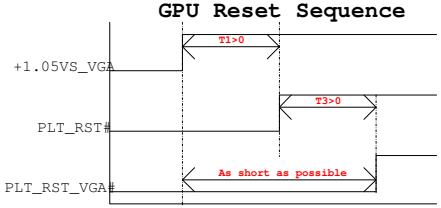
1. all power rail ramp up time should be larger than 40us
2. The total time for all rails to ramp should be within 6ms.
3. A power rail has to ramp up 90% before the next power rail in sequence can start ramping up.
4. No signal should be applied to the GPU before the power rail are fully ramped.

GPU Power Down

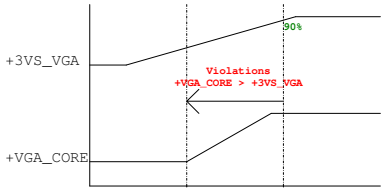


1.All GPU power rails should be turned off within 10ms

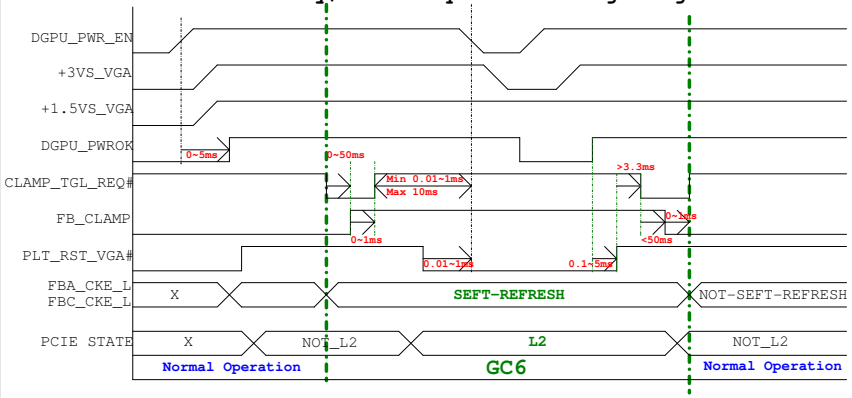
GPU Reset Sequence



Power sequencing violations



GC6 Entry/Exit Sequence Timing Diagram



For N14P-GV2 strap table X76

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GV2	1 GHz	128M* 16* 4 1GB	Samsung K4W2G1646E-BC1A	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 45K	R PU 5K	R PU 5K
N14P-GV2	1 GHz	128M* 16* 4 1GB	Micron MT41J128M16JT-093G:K	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 30K	R PU 5K	R PU 5K
N14P-GV2	1 GHz	128M* 16* 4 1GB	Hynix H5TC2G63FFR-11C	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 25K	R PU 5K	R PU 5K
N14P-GV2	900 MHz	256M* 16* 4 2GB	Samsung K4W4G1646B-HC11	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 20K	R PU 5K	R PU 5K
N14P-GV2	900 MHz	256M* 16* 4 2GB	Micron MT41K256M16HA-107G:E	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 10K	R PU 5K	R PU 5K

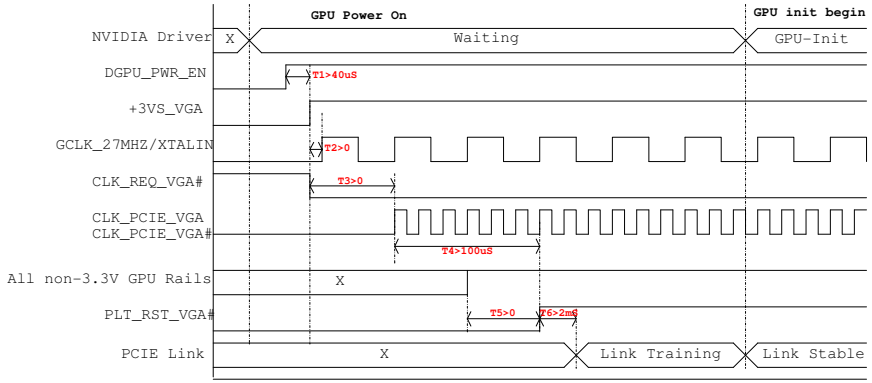
For N14P-GS strap table X76

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GS	1 GHz	128M* 16* 8 2GB	Samsung K4W2G1646E-BC1A	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 45K	R PU 5K	R PD 15K
N14P-GS	1 GHz	128M* 16* 8 2GB	Micron MT41J128M16JT-093G:K	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 30K	R PU 5K	R PD 15K
N14P-GS	1 GHz	128M* 16* 8 2GB	Hynix H5TC2G63FFR-11C	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 25K	R PU 5K	R PD 15K
N14P-GS	900 MHz	256M* 16* 8 4GB	Samsung K4W4G1646B-HC11	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 20K	R PU 5K	R PD 15K
N14P-GS	900 MHz	256M* 16* 8 4GB	Micron MT41K256M16HA-107G:E	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 10K	R PU 5K	R PD 15K

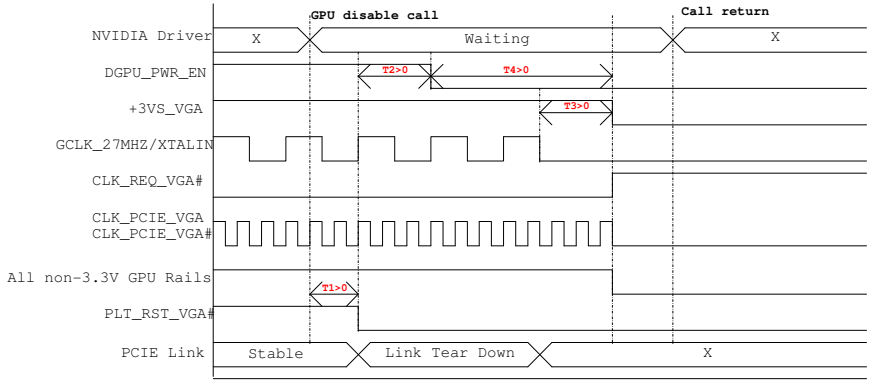
For N14M-GE strap table X76

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14M-GE	1 GHz	128M* 16* 4 1GB	Samsung K4W2G1646E-BC1A	R PU 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	1 GHz	128M* 16* 4 1GB	Micron MT41J128M16JT-093G:K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	1 GHz	128M* 16* 4 1GB	Hynix H5TC2G63FFR-11C	R PD 10K	R PD 10K	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	900 MHz	256M* 16* 4 2GB	Samsung K4W4G1646B-HC11	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	900 MHz	256M* 16* 4 2GB	Micron MT41K256M16HA-107G:E	R PU 10K	R PD 10K	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K

Optimus Typical Power-Up Sequence



Optimus Typical Power-Down Sequence



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Title: VGA Notes List

Size: Custom | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

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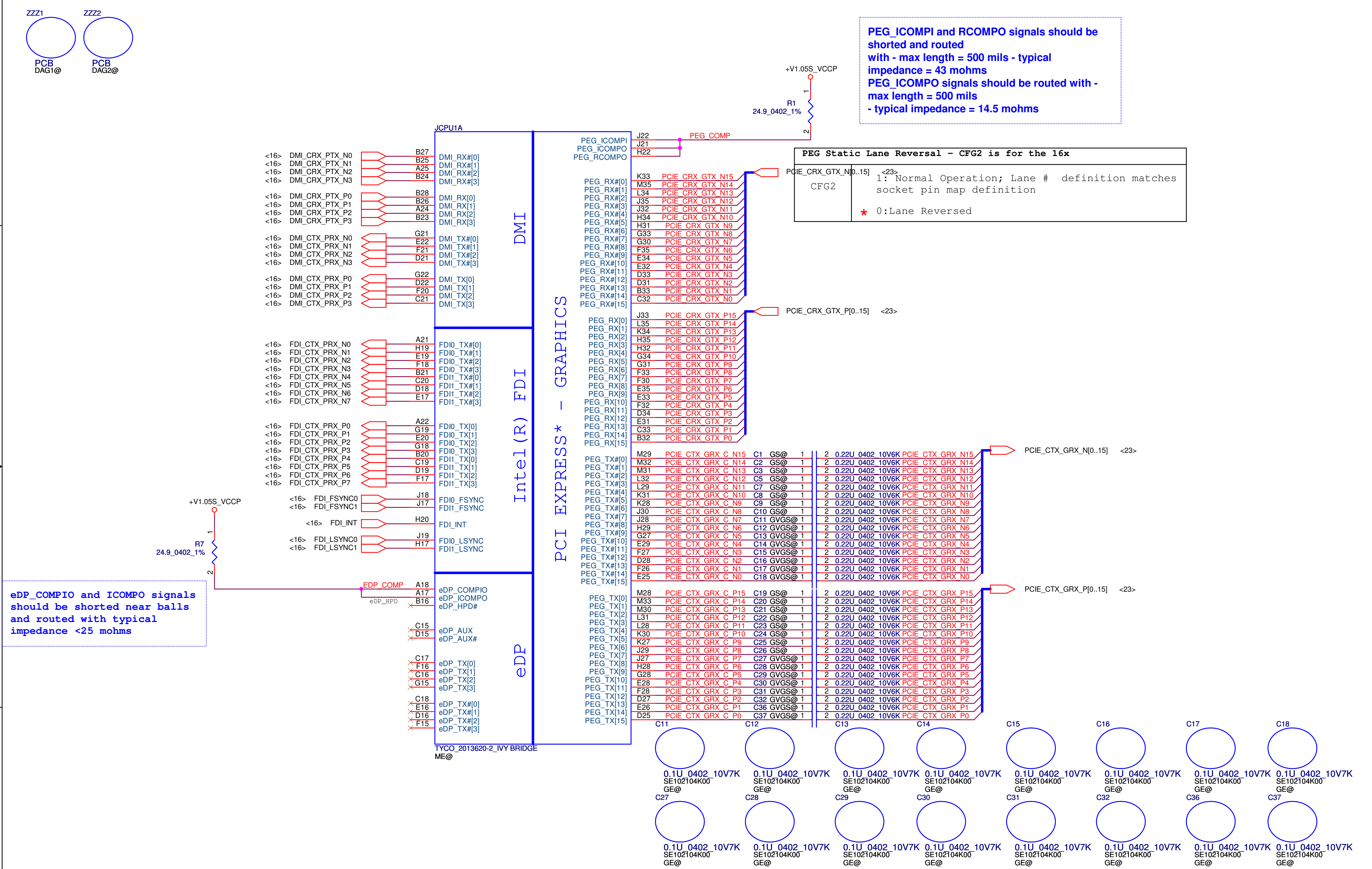

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title: PROCESSOR(1/7) DMI,FDI,PEG
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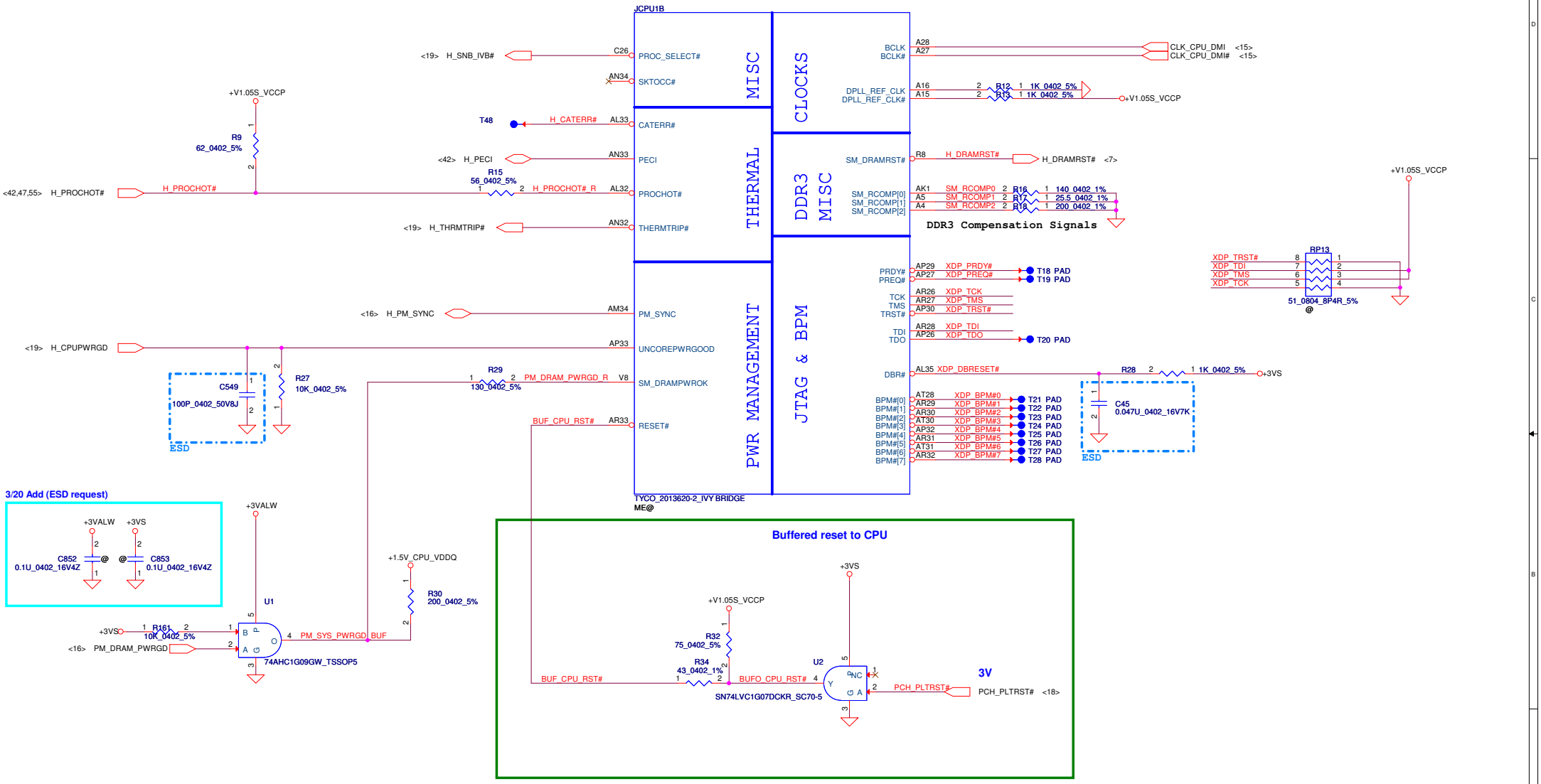
				Date: Wednesday, March 20, 2013; Sheet 5 of 63



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Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

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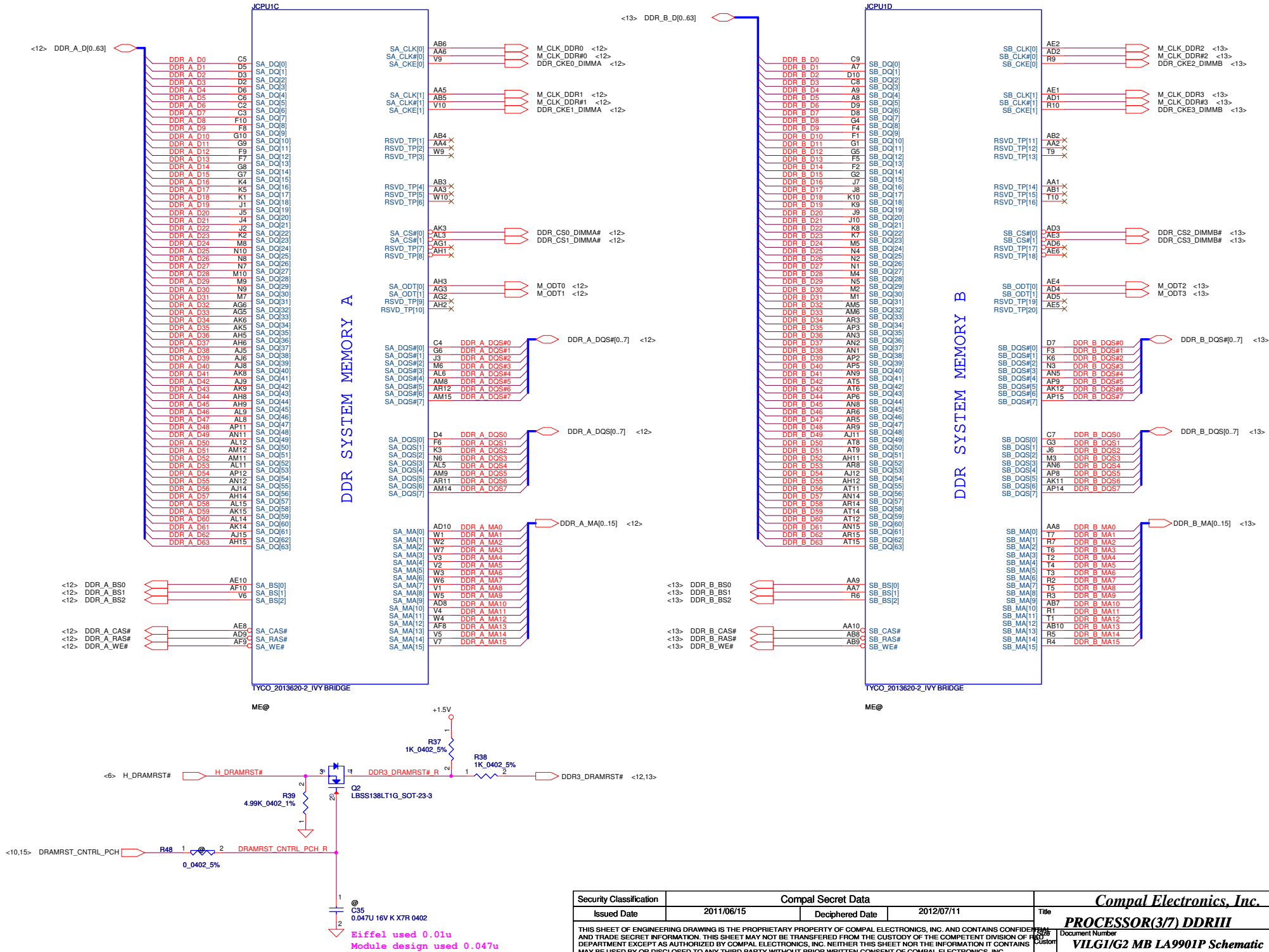

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Title: PROCESSOR(3/7) DDRIII

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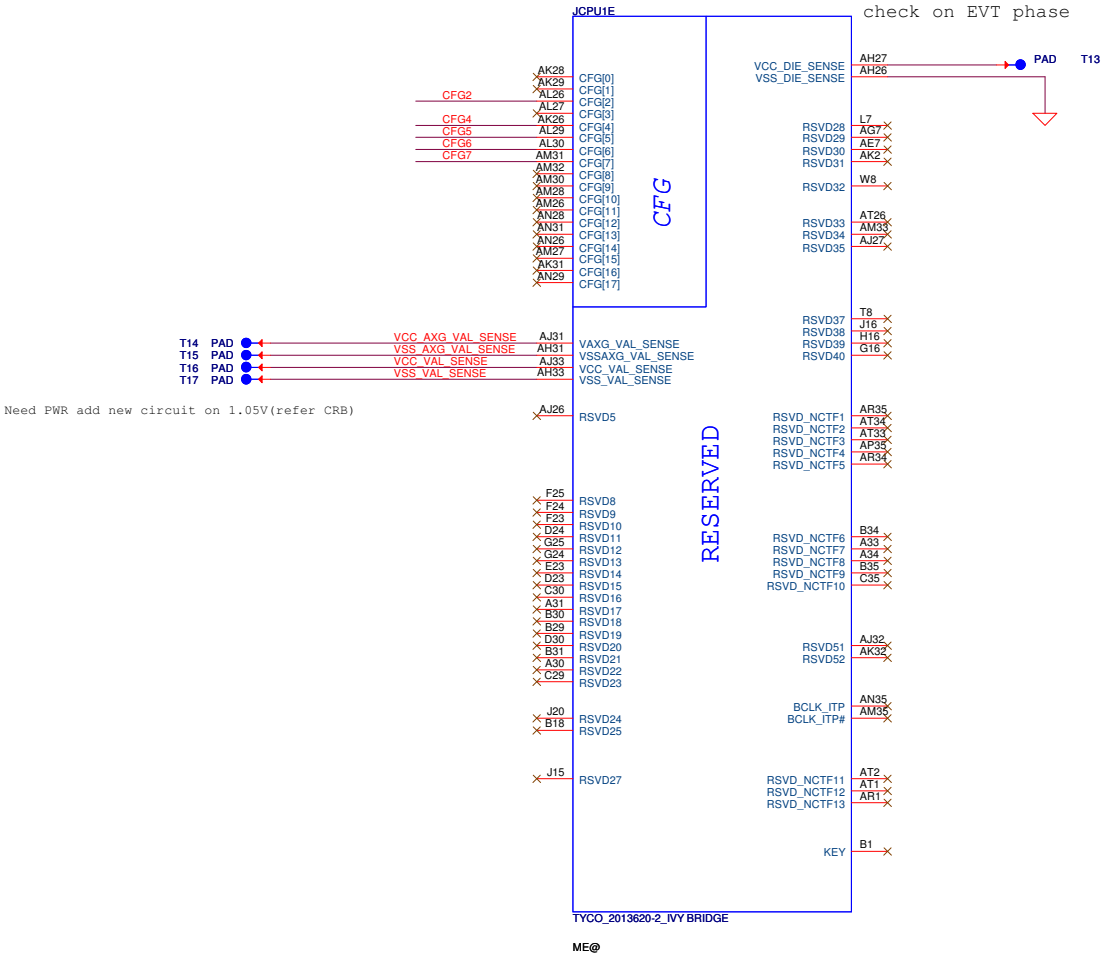
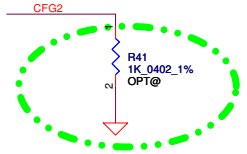
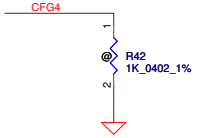
CFG Straps for Processor

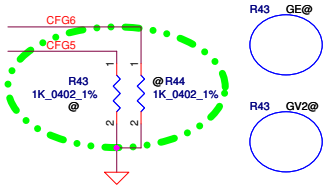




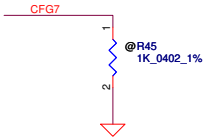
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled *10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

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POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

+V1.05S_VCCP

8.5A

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

AG35	VCC1	VCCIO1	AH13
AG34	VCC2	VCCIO2	AH10
AG33	VCC3	VCCIO3	AG10
AG32	VCC4	VCCIO4	AC10
AG31	VCC5	VCCIO5	Y10
AG30	VCC6	VCCIO6	U10
AG29	VCC7	VCCIO7	P10
AG28	VCC8	VCCIO8	L10
AG27	VCC9	VCCIO9	J14
AG26	VCC10	VCCIO10	J13
AF35	VCC11	VCCIO11	J12
AF34	VCC12	VCCIO12	J11
AF33	VCC13	VCCIO13	H14
AF32	VCC14	VCCIO14	H12
AF31	VCC15	VCCIO15	H11
AF30	VCC16	VCCIO16	G14
AF29	VCC17	VCCIO17	G13
AF28	VCC18	VCCIO18	G12
AF27	VCC19	VCCIO19	F14
AF26	VCC20	VCCIO20	F13
AD35	VCC21	VCCIO21	F12
AD34	VCC22	VCCIO22	F11
AD33	VCC23	VCCIO23	E14
AD32	VCC24	VCCIO24	E12
AD31	VCC25		
AD30	VCC26	VCCIO25	E11
AD29	VCC27	VCCIO26	D14
AD28	VCC28	VCCIO27	D13
AD27	VCC29	VCCIO28	D12
AD26	VCC30	VCCIO29	D11
AC35	VCC31	VCCIO30	C14
AC34	VCC32	VCCIO31	C13
AC33	VCC33	VCCIO32	C12
AC32	VCC34	VCCIO33	C11
AC31	VCC35	VCCIO34	B14
AC30	VCC36	VCCIO35	B12
AC29	VCC37	VCCIO36	A14
AC28	VCC38	VCCIO37	A13
AC27	VCC39	VCCIO38	A12
AC26	VCC40	VCCIO39	A11
AA35	VCC41		
AA34	VCC42	VCCIO40	J23
AA33	VCC43		
AA32	VCC44		
AA31	VCC45		
AA30	VCC46		
AA29	VCC47		
AA28	VCC48		
AA27	VCC49		
AA26	VCC50		
Y35	VCC51		
Y34	VCC52		
Y33	VCC53		
Y32	VCC54		
Y31	VCC55		
Y30	VCC56		
Y29	VCC57		
Y28	VCC58		
Y27	VCC59		
Y26	VCC60		
V35	VCC61		
V34	VCC62		
V33	VCC63		
V32	VCC64		
V31	VCC65		
V30	VCC66		
V29	VCC67		
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V27	VCC69		
V26	VCC70		
U35	VCC71		
U34	VCC72		
U33	VCC73		
U32	VCC74		
U31	VCC75		
U30	VCC76		
U29	VCC77		
U28	VCC78		
U27	VCC79		
U26	VCC80		
R35	VCC81		
R34	VCC82		
R33	VCC83		
R32	VCC84		
R31	VCC85		
R30	VCC86		
R29	VCC87		
R28	VCC88		
R27	VCC89		
R26	VCC90		
P35	VCC91		
P34	VCC92		
P33	VCC93		
P32	VCC94		
P31	VCC95		
P30	VCC96		
P29	VCC97		
P28	VCC98		
P27	VCC99		
P26	VCC100		

TYCO_2013620-2_IVY BRIDGE

ME@

+V1.05S_VCCP

R46 75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT# AJ29 H_CPU_SVIDALRT# — R47 43_0402_5% — VR_SVID_ALRT# <55>
VIDSCLK AJ30 — VR_SVID_CLK <55>
VIDSOUT AJ28 — VR_SVID_DAT <55>

R50 130_0402_5% +V1.05S_VCCP 0.1uF on power side

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

+VCC_CORE

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

R51 100_0402_1%

VCC_SENSE AJ35 — VCCSENSE <55>
VSS_SENSE AJ34 — VSSSENSE <55>

R54 100_0402_1%

VCCIO_SENSE B10
VSS_SENSE_VCCIO A10 VSSIO_SENSE_L — R74 10_0402_1%

VCCIO_SENSE <53>

R74 & R79 put together

+V1.05S_VCCP

R79 10_0402_1%

VSSIO_SENSE_L <53>

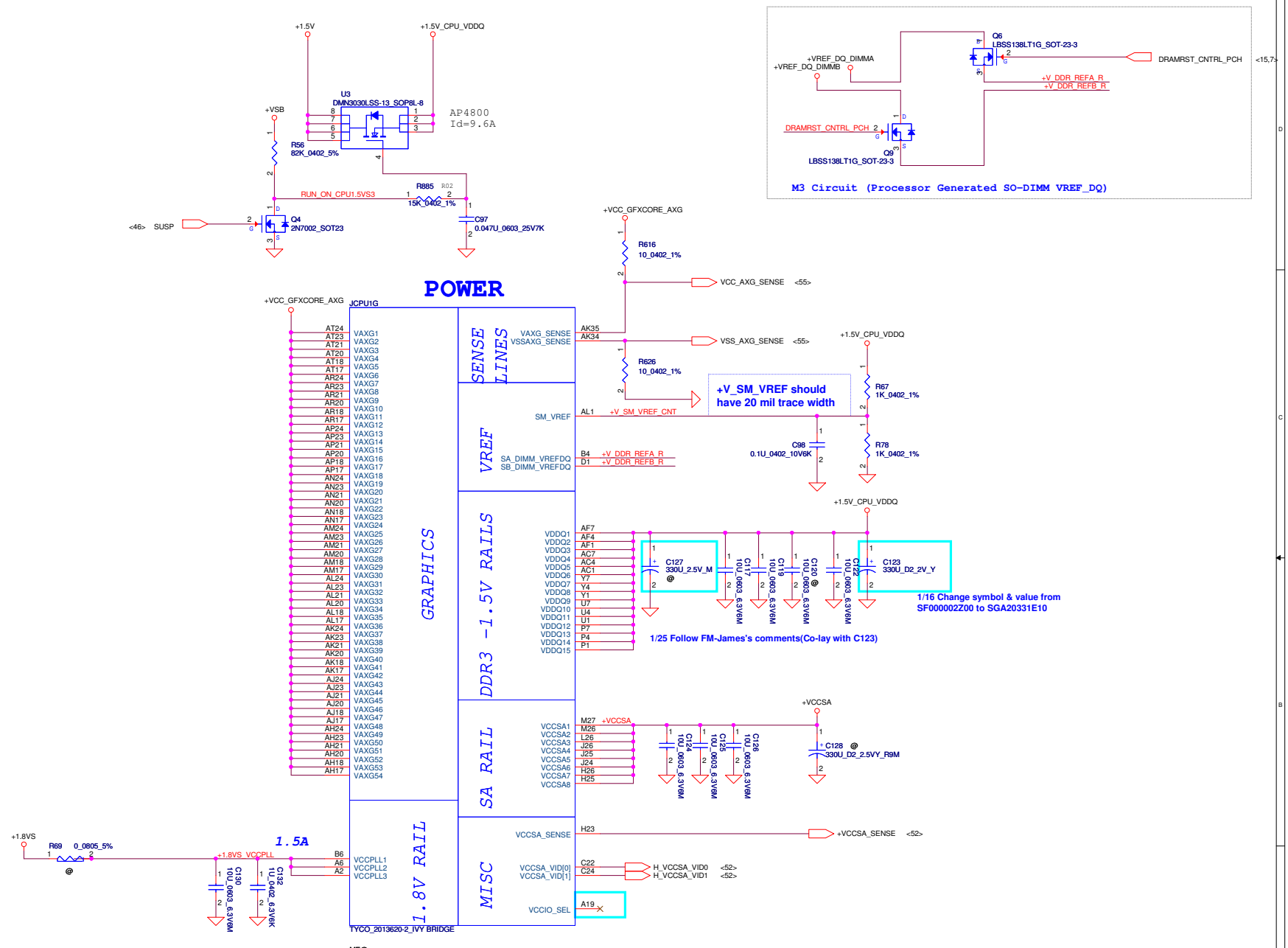
VSS_SENCE 100ohm +-1% pull-down to GND near processor

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PROCESSOR(5/7) PWR,BYPASS

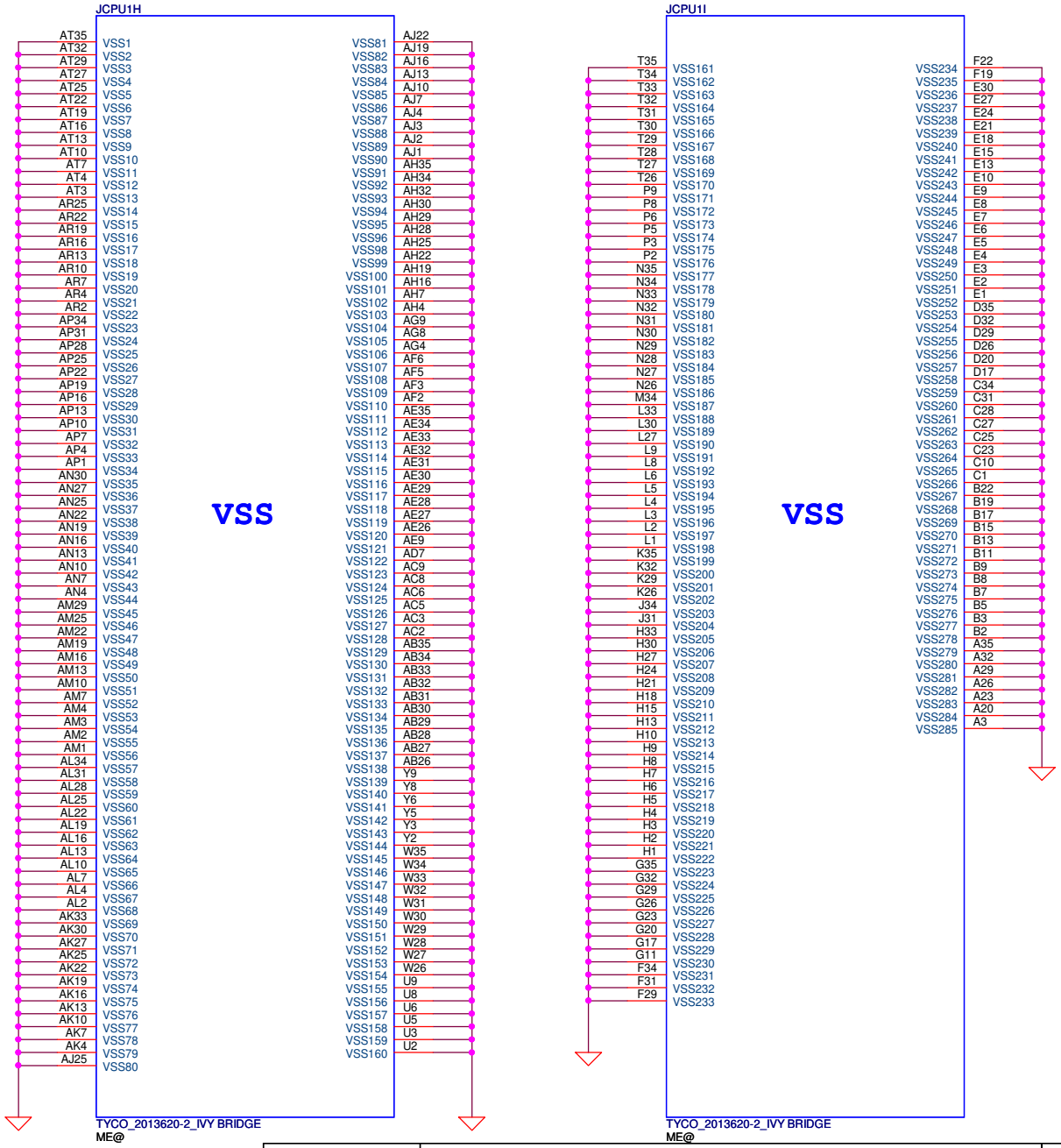
Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 9 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	PROCESSOR(6/7) PWR		
Size: Custom	Document Number: VILG1/G2 MB LA9901P Schematic		Rev: 1.0
Date: Wednesday, March 20, 2013	Sheet 10 of 63		



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	VILG1/G2 MB LA9901P Schematic	1.0

Date: Wednesday, March 20, 2013 Sheet 11 of 63

DDR3 SO-DIMM A

JDIMM1

LCN_DAN06-K4806-0103
ME@

<7> DDR_A_D[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_MA[0..15]

RP15 1K_0804_8P4R_1%
RP16 1K_0804_8P4R_1%

Layout Note: Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note: Place near DIMM

```
VDDQ(1.5V) =
  3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
  6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
  3*0805 10uf  4*0402 1uf
VREF =
  1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
  1*0402 0.1uf  1*0402 2.2uf
```

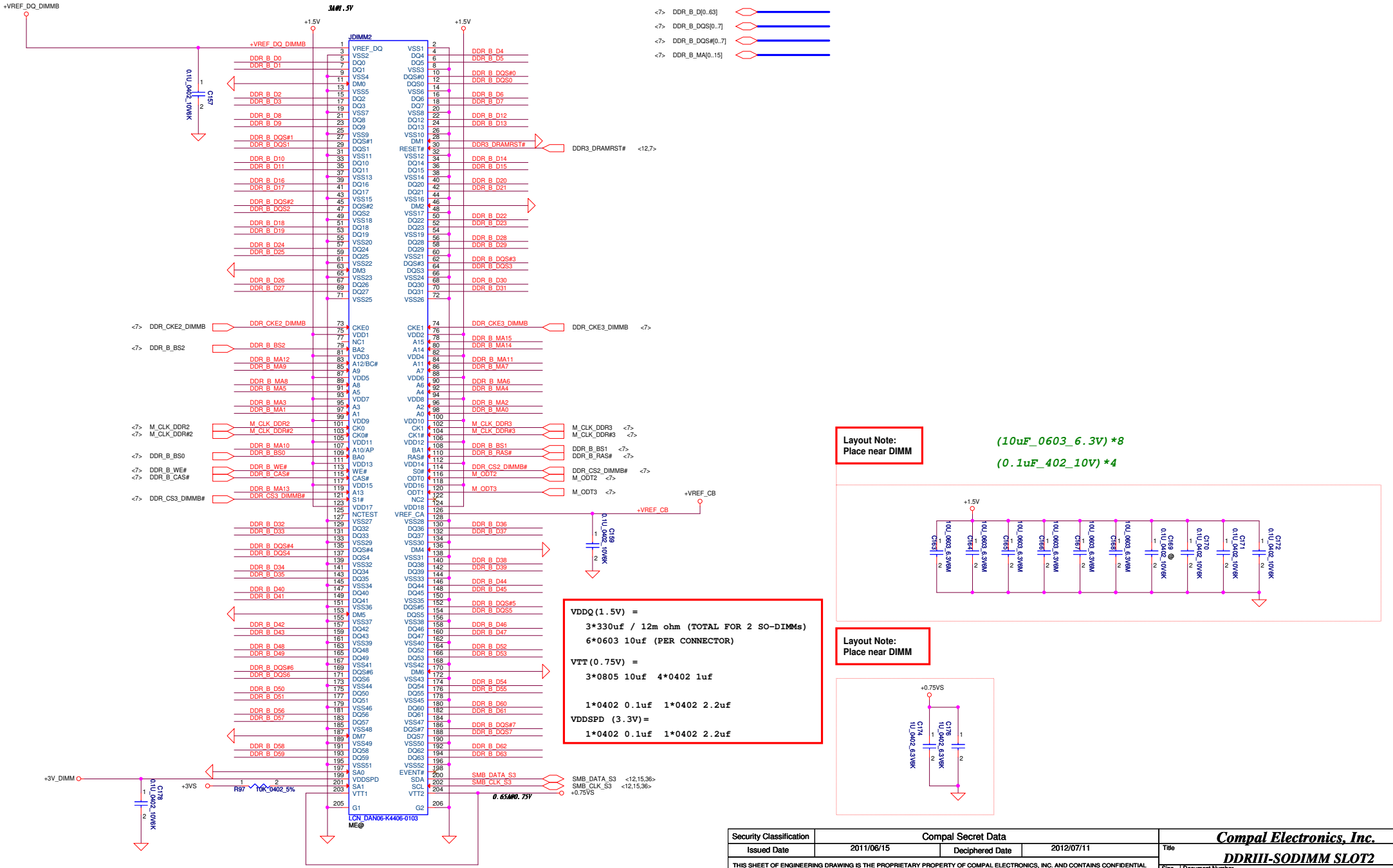
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 12 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size: | Document Number: **VILG1/G2 MB LA9901P Schematic** | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 13 of 63

W=20mils +RTCVCC — R99 1K_0402_5% — C179 1U_0603_10V4Z

W=20mils +RTCBATT

PCH_RTCX1 — R98 10M_0402_5% NOGCLK@ — PCH_RTCX2

Y1 32.768KHZ_12.5PF_CM31532768DZFT NOGCLK@

C180 12P_0402_50V8J NOGCLK@

C181 12P_0402_50V8J NOGCLK@

R187 0_0402_5% @ GCLK_32K — GCLK_32K <44>

+RTCVCC

R101 1M_0402_5% SM_INTRUDER#

R102 330K_0402_5% PCH_INTVRMEN

INTVRMEN

★ H : Integrated VRM enable
L : Integrated VRM disable

(INTVRMEN should always be pull high.)

+3VS — R105 @ 1K_0402_5% HDA_SPKR

HIGH= Enable (No Reboot)
★ LOW= Disable (Default)

+3V_PCH — R106 @ 1K_0402_5% ME_FLASH

★ Low = Disable (Default)
High = Enabled [Flash Descriptor Security Overide]

+3V_PCH — R108 1K_0402_5% HDA_SYNC

This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high(For mobile only)
★ 1.8V when sampled low (For Desktop only)
Needs to be pulled High for Chief River platfrom

DPDG1.1

CMOS

+RTCVCC — C183 1U_0603_10V4Z — R103 20K_0402_5% — R100 20K_0402_5% — C182 1U_0603_10V4Z

CLRP2 SHORT PADS

CLRP3 SHORT PADS

U4A

PCH_RTCX1	A20	RTCX1	RTC	
PCH_RTCX2	C20	RTCX2		
PCH_RTCRST#	D20	RTCRST#		
PCH_SRTCRST#	G22	SRTCRST#		
SM_INTRUDER#	K22	INTRUDER#		
PCH_INTVRMEN	C17	INTVRMEN		
HDA_BIT_CLK	N34	HDA_BCLK	IHDA	
HDA_SYNC	L34	HDA_SYNC		
<41> HDA_SPKR — HDA_SPKR	T10	SPKR		
HDA_RST#	K34	HDA_RST#		
<41> HDA_SDIN0 — HDA_SDIN0	E34	HDA_SDIN0		
	G34	HDA_SDIN1		
	C34	HDA_SDIN2		
	A34	HDA_SDIN3		
<42> ME_FLASH — ME_FLASH	A36	HDA_SDO		
	C36	HDA_DOCK_EN# / GPIO33		
	N32	HDA_DOCK_RST# / GPIO13		
PCH_JTAG_TCK	J3	JTAG_TCK	JTAG	
PCH_JTAG_TMS	H7	JTAG_TMS		
PCH_JTAG_TDI	K5	JTAG_TDI		
PCH_JTAG_TDO	H1	JTAG_TDO		
SPI_CLK_PCH_R	T3	SPI_CLK	SPI	
SPI_SB_CS0#	Y14	SPI_CS0#		
SPI_SB_CS1#	T1	SPI_CS1#		
SPI_SI	V4	SPI_MOSI		
SPI_SO_R	U3	SPI_MISO		

PANTHER-POINT_FCBGA989
HM76@

T41 PAD — PCH_JTAG_TCK
T35 PAD — PCH_JTAG_TMS
T36 PAD — PCH_JTAG_TDI
T37 PAD — PCH_JTAG_TDO

LPC	C38	LPC_AD0	LPC_AD0 <42>
	A38	LPC_AD1	LPC_AD1 <42>
	B37	LPC_AD2	LPC_AD2 <42>
	C37	LPC_AD3	LPC_AD3 <42>
	D36	LPC_FRAME#	LPC_FRAME# <42>
	E36	LDRQ0#	
	K36	LDRQ1# / GPIO23	
	V5	SERIRQ	SERIRQ <42>
SATA 6G	AM3	SATA_DTX_C_IRX_N0	SATA_DTX_C_IRX_N0 <40>
	AM1	SATA_DTX_C_IRX_P0	SATA_DTX_C_IRX_P0 <40>
	AP7	SATA_ITX_C_DRX_N0	SATA_ITX_C_DRX_N0 <40>
	AP5	SATA_ITX_C_DRX_P0	SATA_ITX_C_DRX_P0 <40>
	AM10	SATA1RXN	
	AM8	SATA1RXP	
	AP11	SATA1TXN	
	AP10	SATA1TXP	
	AD7	SATA_DTX_C_IRX_N2	SATA_DTX_C_IRX_N2 <40>
	AD5	SATA_DTX_C_IRX_P2	SATA_DTX_C_IRX_P2 <40>
	AH5	SATA_ITX_C_DRX_N2	SATA_ITX_C_DRX_N2 <40>
	AH4	SATA_ITX_C_DRX_P2	SATA_ITX_C_DRX_P2 <40>
	AB8	SATA3RXN	
	AB10	SATA3RXP	
	AF3	SATA3TXN	
	AF1	SATA3TXP	
	Y7	SATA4RXN	
	Y5	SATA4RXP	
	AD3	SATA4TXN	
	AD1	SATA4TXP	
	Y3	SATA5RXN	
	Y1	SATA5RXP	
	AB3	SATA5TXN	
	AB1	SATA5TXP	
	Y11	SATAICOMPO	
	Y10	SATAICOMPI	SATA_COMP
	AB12	SATA3RCOMPO	
	AB13	SATA3COMPI	SATA3_COMP
	AH1	SATA3RBIAS	RBIAS_SATA3
	P3	SATALED#	SATALED#
	V14	SATA0GP / GPIO21	
	P1	SATA1GP / GPIO19	BBS_BIT0_R

EC and Mini card debug port

HDD

ODD

GPIO19 has internal Pull UP

R111 37.4_0402_1% +V1.05S_VCCP

R113 49.9_0402_1% +V1.05S_VCCP

RT15 750_0402_1%

11/30 Add(Share ROM)

Near U5

RP27 0_0804_8P4R_5%

<42> EC_SPI_SO — EC_SPI_SO — SPI_SO_L
<42> EC_SPI_SI — EC_SPI_SI — SPI_SI_R
<42> EC_SPI_CLK — EC_SPI_CLK — SPI_CLK_PCH_0
<42> EC_SPI_CS# — EC_SPI_CS# — SPI_SB_CS0#

8MB SPI ROM FOR ME & Non-share ROM.

+3V_ROM

U6 64M W25Q64FVSSIQ SOIC 8P @

SPI_SB_CS1# — R188 0_0402_5% For EMI — SPI_SO1

R198 0_0402_5% SPI_CLK_PCH_R

R196 0_0402_5% SPI_SI

For EMI

U6 Rersver 4M+2M Solution

U5 64M W25Q64FVSSIQ SOIC 8P

SPI_SB_CS0# — R131 0_0402_5% For EMI — SPI_SO_L

R135 0_0402_5% SPI_CLK_PCH_R

R133 0_0402_5% SPI_SI

For EMI

+5VS — Q10 LBSS138LT1G_SOT-23-3 @

<41> HDA_BITCLK_AUDIO — HDA_BIT_CLK
<41> HDA_SYNC_AUDIO — HDA_SYNC_R
<41> HDA_RST_AUDIO# — HDA_RST#
<41> HDA_SDOUT_AUDIO — ME_FLASH

For EMI — RP12 33_0804_8P4R_5%

R878 1M_0402_5% — HDA_SYNC — R175 0_0402_5%

check with vender
Del Q10 check with codec
VDDIO using 3VALW

SPI_CLK_PCH_R — R124 33_0402_5% @ — C190 22P_0402_50V8J @ For EMI

R124;c190 close to U4.T3 pin

U4 HM70@

SA00005MQ80
S IC BD82HM70 SJTNV C1 BGA 989P PCH C38!

+3V_ROM

R266 3.3K_0402_5% SPI_WP#1
R221 3.3K_0402_5% SPI_HOLD#1
R127 3.3K_0402_5% SPI_WP#
R129 3.3K_0402_5% SPI_HOLD#

+3VS

RP17 10K_0804_8P4R_5%

<19> PCH_GPIO16 — PCH_GPIO16
BBS_BIT0_R
SATALED#
SERIRQ

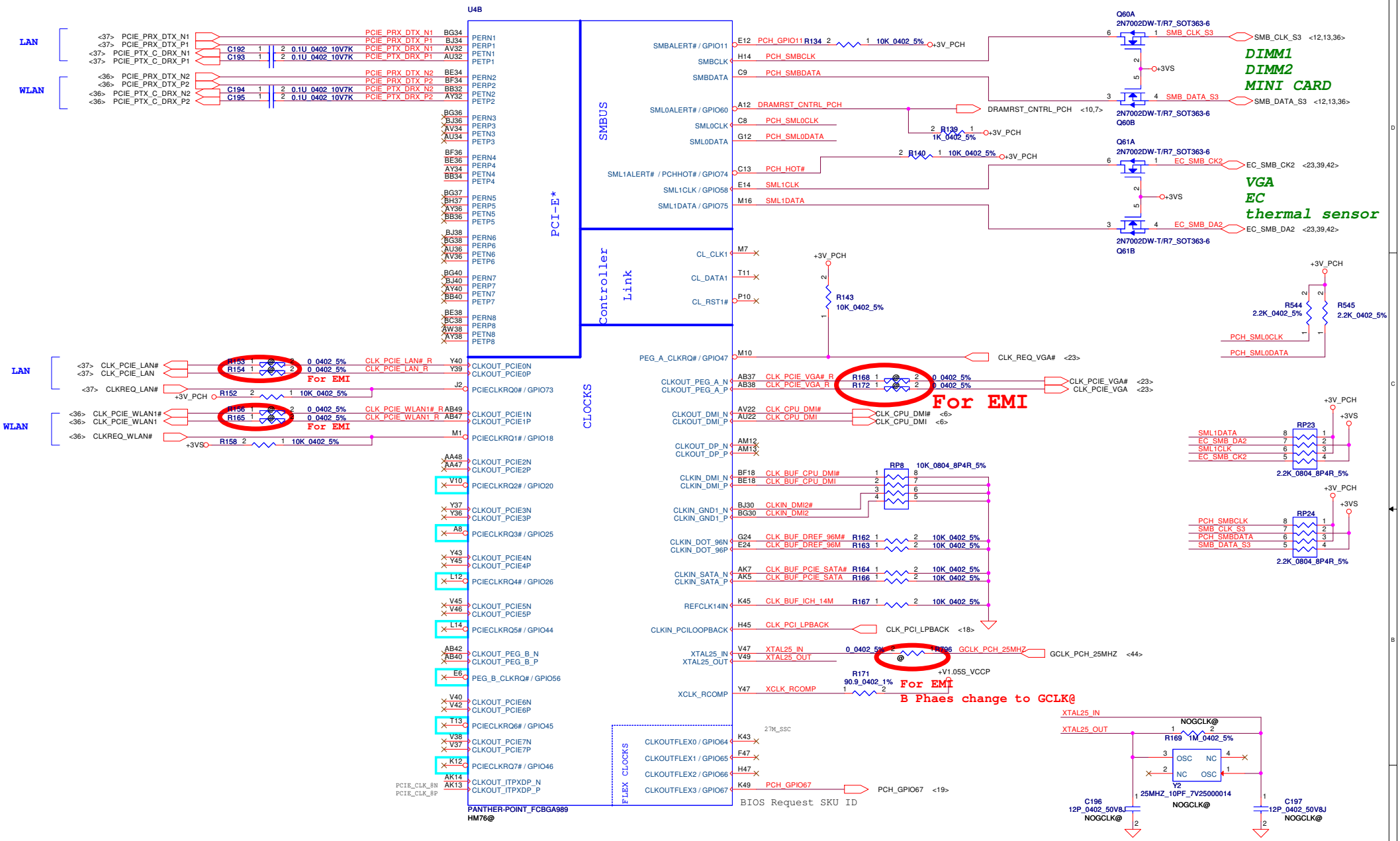
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 14 of 63



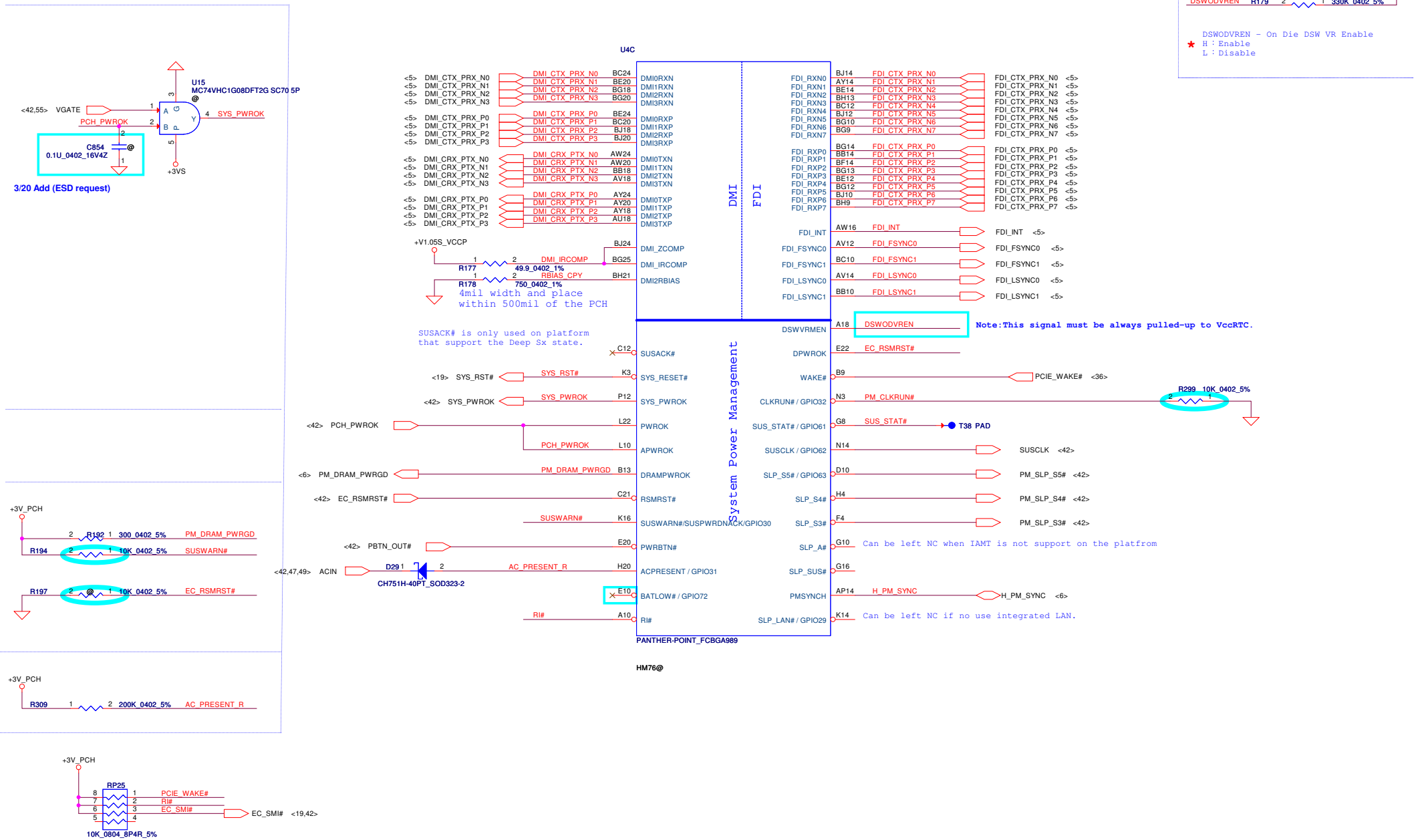
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	VILG1/G2 MB LA9901P Schematic	1.0

Date: Wednesday, March 20, 2013 Sheet 15 of 63



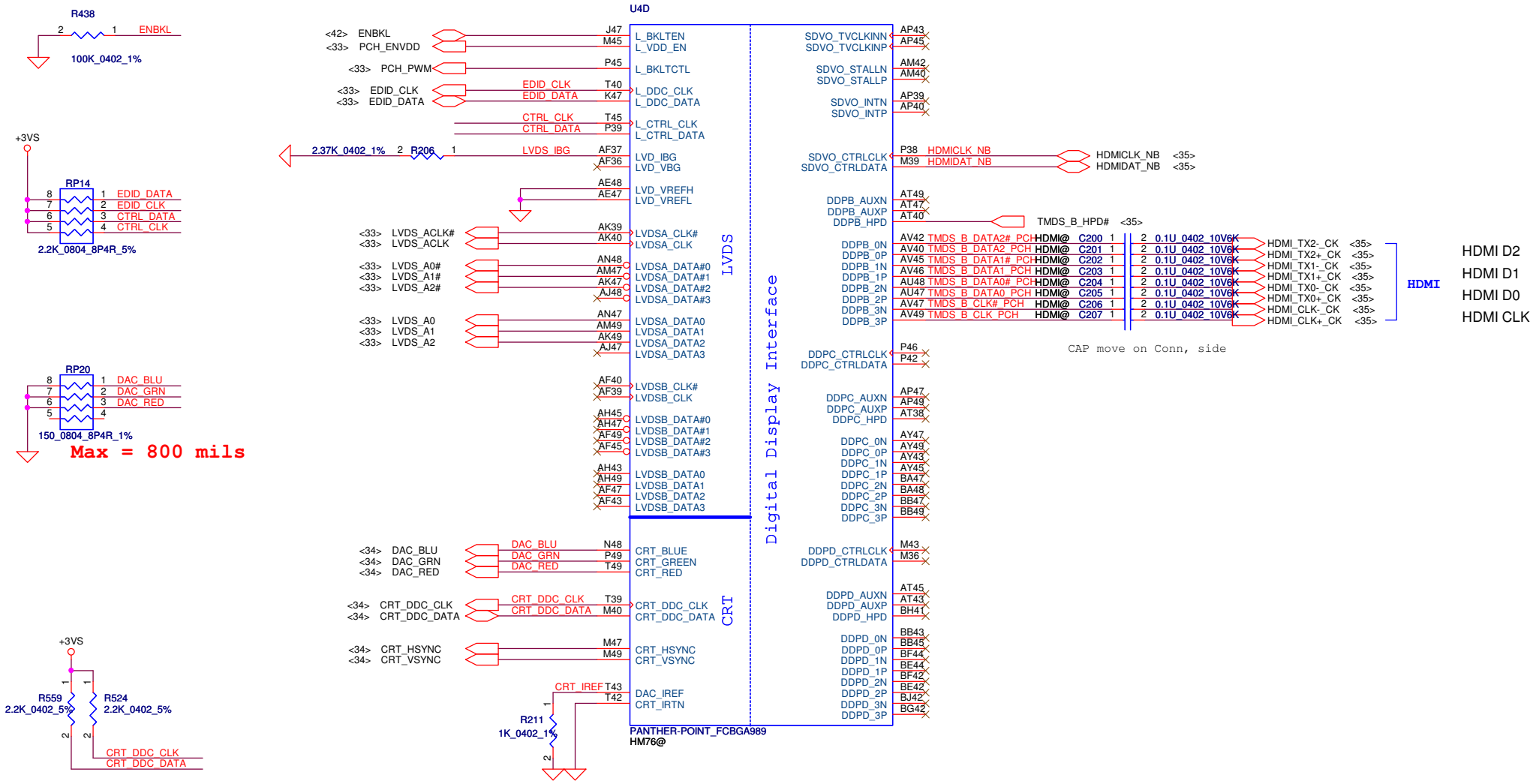
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 16 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size: B | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

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RP1
+3VS
PCI_PIRQA# 1
PCI_PIRQD# 2
PCI_PIRQC# 3
PCI_PIRQB# 4
5
10
9 PCH_GPIO2
8 DGPU_PWR_EN
7 PCH_GPIO4
6 PCH_GPIO3
+3VS
8.2K_1206_10P8R_5%

RP7
+3VS
8 1 DGPU_HOLD_RST#
7 2 PCH_WL_OFF#
6 3 PCH_GPIO5
5 4 NVDD_PWR_EN
8.2K_0804_8P4R_5%

Pull-up resistors are not required on these signals

R292 1 @ 2 8.2K_0402_5% PCH_GPIO51
R557 1 @ 2 8.2K_0402_5% PCH_GPIO53

Boot BIOS Strap			
	GPIO51 Bit11	GPIO19 Bit10	Boot BIOS Destination
GNT1#/ GPIO51			
SATA1GP/ GPIO19	0	1	Reserved
Internal PH	1	0	PCI
	1	1 *	SPI (Default)
	0	0	LPC

GPIO55
PCH_WL_OFF# R215 1 @ 2 1K_0402_5%

A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default *

U4E

RSVD: TP1 BG26, TP2 BJ26, TP3 BH25, TP4 BJ16, TP5 BG16, TP6 AH38, TP7 AH37, TP8 AK43, TP9 AK45, TP10 C18, TP11 N30, TP12 H3, TP13 AH12, TP14 AM4, TP15 AM5, TP16 Y13, TP17 K24, TP18 L24, TP19 AB46, TP20 AB45, TP21 B21, TP22 M20, TP23 AY16, TP24 BG46
RSVD1 AY7, RSVD2 AV7, RSVD3 AU3, RSVD4 BG4, RSVD5 AT10, RSVD6 BC8, RSVD7 AU2, RSVD8 AT4, RSVD9 AT3, RSVD10 AT1, RSVD11 AY3, RSVD12 AT5, RSVD13 AV3, RSVD14 AV1, RSVD15 BB1, RSVD16 BA3, RSVD17 BB5, RSVD18 BB3, RSVD19 BB7, RSVD20 BE8, RSVD21 BD4, RSVD22 BF6, RSVD23 AV5, RSVD24 AV10, RSVD25 AT8, RSVD26 AY5, RSVD27 BA2, RSVD28 AT12, RSVD29 BF3

USB3: USB3Rn1 BE28, USB3Rn2 BC30, USB3Rn3 BE32, USB3Rn4 BJ32, USB3Rp1 BC28, USB3Rp2 BE30, USB3Rp3 BF32, USB3Rp4 BG32, USB3Tn1 AV26, USB3Tn2 BB26, USB3Tn3 AU28, USB3Tn4 AY30, USB3Tp1 AU26, USB3Tp2 AY26, USB3Tp3 AV28, USB3Tp4 AW30
<45> USB3_RX1_N, USB3_RX2_N
<45> USB3_RX1_P, USB3_RX2_P
<45> USB3_TX1_N, USB3_TX2_N
<45> USB3_TX1_P, USB3_TX2_P

PCI: PIRQA# K40, PIRQB# K38, PIRQC# H38, PIRQD# G38, REQ1# / GPIO50 C46, REQ2# / GPIO52 C44, REQ3# / GPIO54 E40, GNT1# / GPIO51 D47, GNT2# / GPIO53 E42, GNT3# / GPIO55 F46, PIRQE# / GPIO2 G42, PIRQF# / GPIO3 G40, PIRQG# / GPIO4 C42, PIRQH# / GPIO5 D44, PME# K10, PLTRST# C6, CLKOUT_PCI0 H49, CLKOUT_PCI1 H43, CLKOUT_PCI2 J48, CLKOUT_PCI3 K42, CLKOUT_PCI4 H40

USB: USBP0N C24, USBP0P A24, USBP1N C25, USBP1P B25, USBP2N C26, USBP2P A26, USBP3N K28, USBP3P H28, USBP4N E28, USBP4P D28, USBP5N C28, USBP5P A28, USBP6N C29, USBP6P B29, USBP7N N28, USBP7P M28, USBP8N L30, USBP8P K30, USBP9N G30, USBP9P E30, USBP10N C30, USBP10P A30, USBP11N L32, USBP11P K32, USBP12N G32, USBP12P E32, USBP12N C32, USBP13P A32
USBRBIAS# C33, USBRBIAS B33
OC0# / GPIO59 A14, OC1# / GPIO40 K20, OC2# / GPIO41 B17, OC3# / GPIO42 C16, OC4# / GPIO43 L16, OC5# / GPIO9 A16, OC6# / GPIO10 D14, OC7# / GPIO14 C14

PANTHER-POINT_FCBGA989
HM76@

USB DEBUG=PORT1 AND PORT9

USBP0N C24	USB20_N0	USB20_N0 <45>	LEFT USB (USB 3.0)
USBP0P A24	USB20_P0	USB20_P0 <45>	LEFT USB
USBP1N C25	USB20_N1	USB20_N1 <45>	Touch Screen
USBP1P B25	USB20_P1	USB20_P1 <45>	USB Camera
USBP2N C26	USB20_N2	USB20_N2 <45>	
USBP2P A26	USB20_P2	USB20_P2 <45>	
USBP3N K28	USB20_N3	USB20_N3 <33>	
USBP3P H28	USB20_P3	USB20_P3 <33>	
USBP9N G30	USB20_N9	USB20_N9 <43>	USB2.0
USBP9P E30	USB20_P9	USB20_P9 <43>	WLAN
USBP10N C30	USB20_N10	USB20_N10 <36>	CARD READER
USBP10P A30	USB20_P10	USB20_P10 <36>	
USBP11N L32	USB20_N11	USB20_N11 <43>	
USBP11P K32	USB20_P11	USB20_P11 <43>	

HM76 not support USB2.0 for port 6-7
HM70 not support USB2.0 for port 4-7 &12 &13
NM70 not support USB2.0 for port 4-7 &12 &13

USBRBIAS C33 — R218 1 2 22.6_0402_1% — Within 500 mils

For LEFT USB3.0 Port: USB_OC0# <45>
For RIGHT USB2.0 Port: USB_OC4# <43>

RP18
+3V_PCH
USB_OC0# 1
USB_OC1# 2
USB_OC2# 3
USB_OC3# 4
5
10
9 USB_OC4#
8 USB_OC5#
7 USB_OC6#
6 USB_OC7#
+3V_PCH
10K_1206_10P8R_5%

T39 PAD
<6> PCH_PLTRST#
For EMI
<15> CLK_PCI_LPBACK — 22_0402_5% — R219 — CLK_PCI_LPBACK_R
<42> CLK_PCI_EC — 22_0402_5% — R220 — CLK_PCI_EC_R

<23,36,37,42> PLT_RST#
R222 1 2 0_0402_5% @ PCH_PLTRST#
R223 100K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PCH (5/9) PCI, USB
Size: Custom
Document Number: VILG1/G2 MB LA9901P Schematic
Rev: 1.0
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PCH_GPIO69	PCH_GPIO70	Function
-	-	NM70
-	-	Reserved
-	1	HM70
-	0	HM76

PCH_GPIO71	Function
1	N14M-GE 1000MHz
0	N14M-GE 900MH

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R240 1 @ 2 1K_0402_5% PCH_GPIO28

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R245 1 @ 2 10K_0402_5% PCH_GPIO27

GPIO36, 37
When Unused as GPIO or SATA*GP
Use 8.2K-10K pull-down to ground.

R244 @ 10K_0402_5% PCH_GPIO37
R250 @ 10K_0402_5% PCH_GPIO36
R881 10K_0402_5% @
R547 @ 10K_0402_5%

BIOS Request SKU ID

R711 UMA@ 10K_0402_5%
R246 UMA@ 10K_0402_5%
PCH_GPIO38
PCH_GPIO67 PCH_GPIO67 <15>
R708 OPT@ 10K_0402_5%
R298 OPT@ 10K_0402_5%

RP10 10K_0804_8P4R_5%
8 PCH_GPIO39
7 SYS_RST#
6 PCH_BT_ON#
5 PCH_GPIO35
SYS_RST# <16>

PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA

R702 @ 10K_0402_5% PCH_GPIO69
R707 @ 10K_0402_5%
R703 HM70@ 10K_0402_5% PCH_GPIO70
R705 HM76@ 10K_0402_5%
R704 1000M@ 10K_0402_5% PCH_GPIO71
R706 900M@ 10K_0402_5%

U4F

GPIO:
T7 BMBUSY# / GPIO0
A42 TACH1 / GPIO1
H36 TACH2 / GPIO6
E38 TACH3 / GPIO7
C10 GPIO8
C4 LAN_PHY_PWR_CTRL / GPIO12
G2 GPIO15
U2 SATA4GP / GPIO16
D40 TACH0 / GPIO17
T5 SCLOCK / GPIO22
E8 GPIO24
E16 GPIO27
P8 GPIO28
K1 STP_PCI# / GPIO34
K4 GPIO35
V8 SATA2GP / GPIO36
M5 SATA3GP / GPIO37
N2 SLOAD / GPIO38
M3 SDATAOUT0 / GPIO39
V13 SDATAOUT1 / GPIO48
V3 SATA5GP / GPIO49 / TEMP_ALERT#
D6 GPIO57

CPU/MISC:
C40 TACH4 / GPIO68
B41 TACH5 / GPIO69 PCH_GPIO69
C41 TACH6 / GPIO70 PCH_GPIO70
A40 TACH7 / GPIO71 PCH_GPIO71
P4 A20GATE
AU16 PECI
P5 RCIN#
AY11 PROCPWRGD
AY10 THRMTRIP#
T14 INIT3_3V#
AY1 DF_TVS
AH8 TS_VSS1
AK11 TS_VSS2
AH10 TS_VSS3
AK10 TS_VSS4
P37 NC_1

NCTF:
A4 VSS_NCTF_1
A44 VSS_NCTF_2
A45 VSS_NCTF_3
A46 VSS_NCTF_4
A5 VSS_NCTF_5
A6 VSS_NCTF_6
B3 VSS_NCTF_7
B47 VSS_NCTF_8
BD1 VSS_NCTF_9
BD49 VSS_NCTF_10
BE1 VSS_NCTF_11
BE49 VSS_NCTF_12
BF1 VSS_NCTF_13
BF49 VSS_NCTF_14
BG2 VSS_NCTF_15
BG48 VSS_NCTF_16
BH3 VSS_NCTF_17
BH47 VSS_NCTF_18
BJ4 VSS_NCTF_19
BJ44 VSS_NCTF_20
BJ45 VSS_NCTF_21
BJ46 VSS_NCTF_22
BJ5 VSS_NCTF_23
BJ6 VSS_NCTF_24
C2 VSS_NCTF_25
C48 VSS_NCTF_26
D1 VSS_NCTF_27
D49 VSS_NCTF_28
E1 VSS_NCTF_29
E49 VSS_NCTF_30
F1 VSS_NCTF_31
F49 VSS_NCTF_32

PANTHER-POINT_FCBGA989
HM76@

<42> EC_SCI# EC_SCI#
<16,42> EC_SMI# EC_SMI#
+3V_PCH R230 1K_0402_5% EC_LID_OUT#
<42> EC_LID_OUT#
<14> PCH_GPIO16 PCH_GPIO16
<26,27,54> DGPU_PWROK
PU on power side
<36> PCH_BT_ON# PCH_BT_ON#
+3V_PCH <40> ODD_EN ODD_EN
+3V_PCH R241 10K_0402_5% PCH_GPIO27
PCH_GPIO28
<36> INTEL_BT_OFF# INTEL_BT_OFF#
+3VS R242 10K_0402_5%
PCH_GPIO35
PCH_GPIO36
PCH_GPIO37
PCH_GPIO38
PCH_GPIO39

+3VS R236 10K_0402_5%
A20GATE GATEA20 <42>
KBRST# R226 10K_0402_5%
PECI
RCIN# KBRST# KBRST# <42>
PROCPWRGD H_CPUPWRGD <6>
THRMTRIP# PCH_THRMTRIP#_R R239 390_0402_5% H_THRMTRIP# H_THRMTRIP# <6>
INIT3_3V#
DF_TVS
INIT3_3V
This signal has weak internal PU,can't pull low
NV_CLE
Weak internal PU,Do not pull low

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

+1.8VS R216 2.2K_0402_5%
R217 1K_0402_5% H_SNB_IVB# <6>
CLOSE TO THE BRANCHING POINT

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.
Title: PCH (6/9) GPIO, CPU, MISC
Size: Custom
Document Number: VILG1/G2 MB LA9901P Schematic
Rev: 1.0
Date: Wednesday, March 20, 2013
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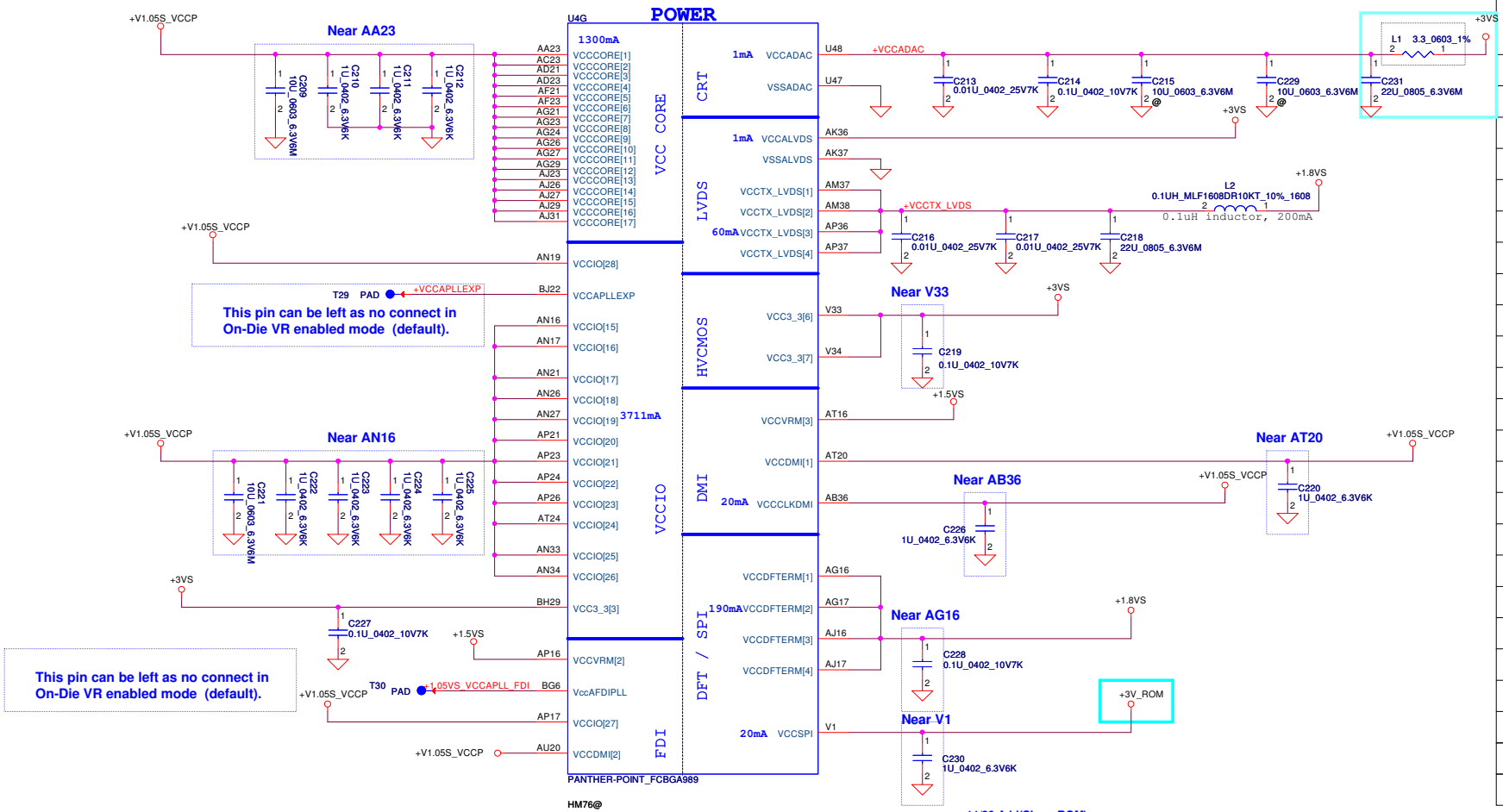
L1 Change to 1 ohm P/N
S RES 1/10W 1 +-1% 0603



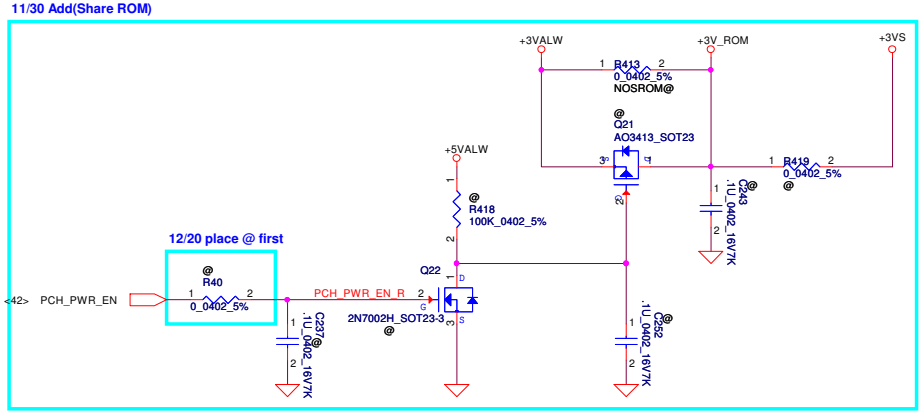
PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Intel recommand stuff R265 and unstuff R266

VCCVRM==>1.5V FOR MOBILE
VCCVRM==>1.8V FOR DESKTOP

VCCVRM = 160mA detal waiting for newest spec

11/30 Add(Share ROM)



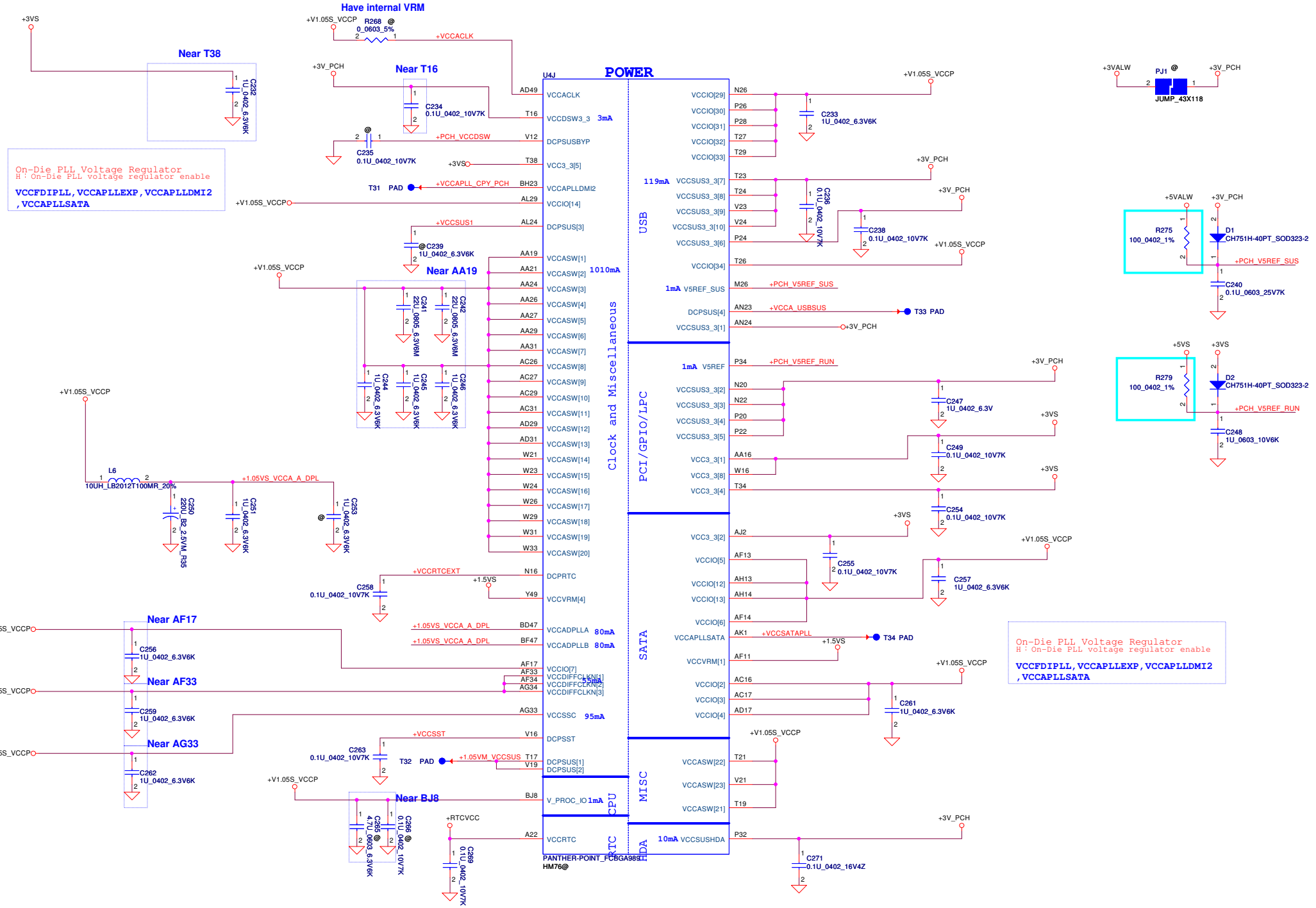
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 20 of 63


Have internal VRM
POWER
U4J
Near T38
Near T16
Near AA19
Near AF17
Near AF33
Near AG33
Near BJ8
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2 , VCCAPLLSATA
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
PANTHER-POINT_FCBGA989
HM76@
JUMP_43X118
T33 PAD
T34 PAD
T31 PAD
T32 PAD
Compal Secret Data
2011/06/15
2012/07/11
Compal Electronics, Inc.
PCH (8/9) PWR
VILG1/G2 MB LA9901P Schematic
Rev 1.0
Wednesday, March 20, 2013
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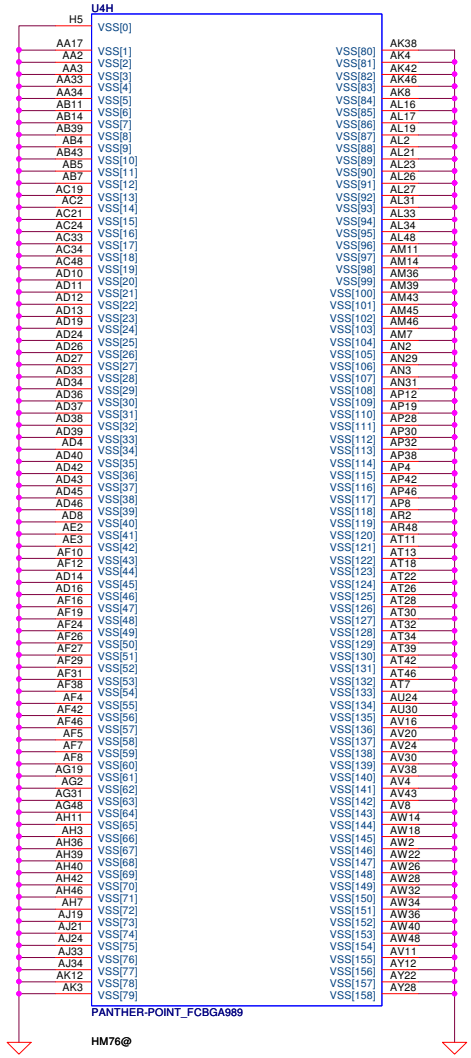
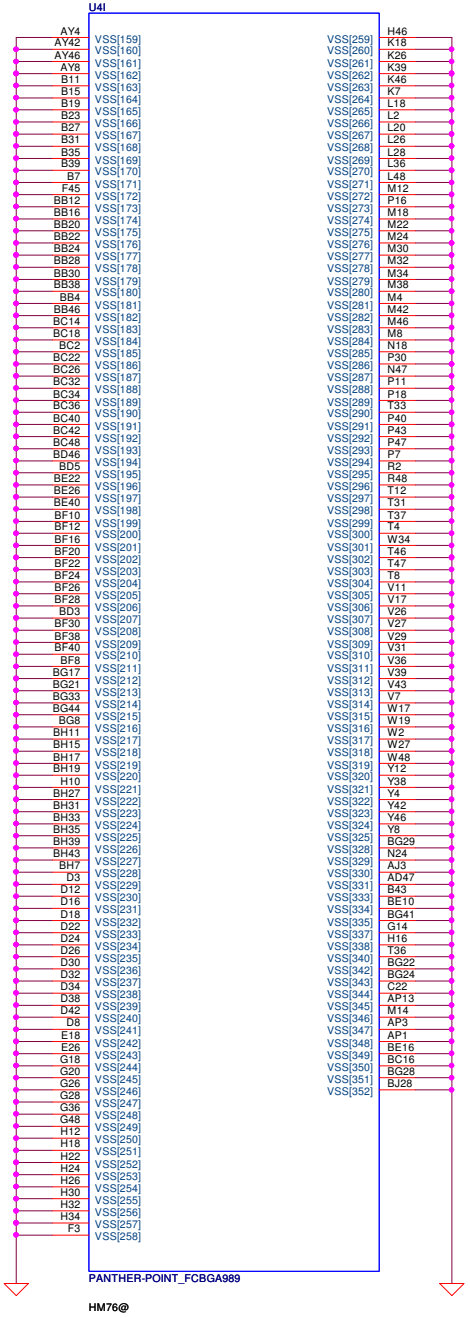




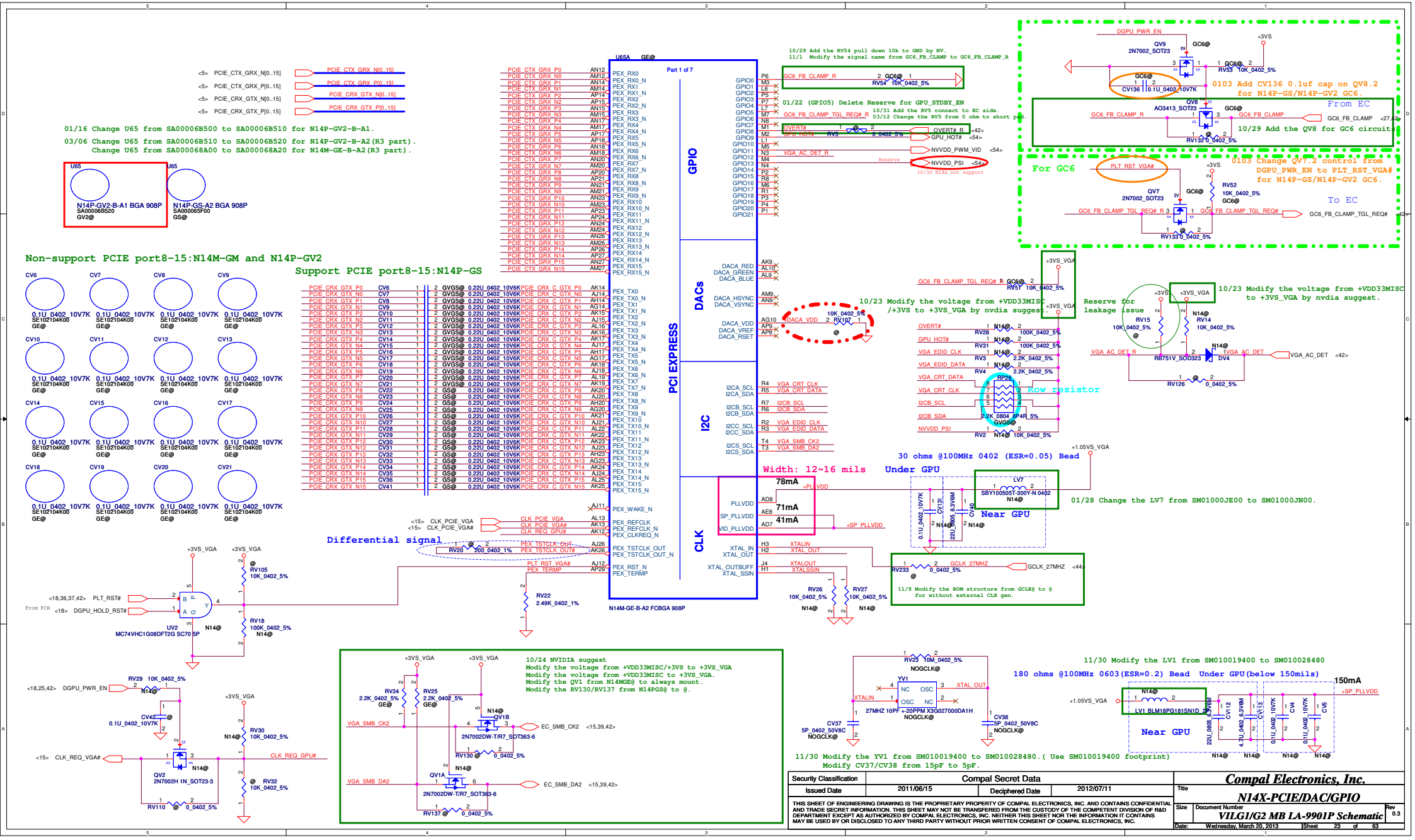
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 22 of 63


01/16 Change U65 from SA00006B500 to SA00006B510 for N14P-GV2-B-A1.
03/06 Change U65 from SA00006B510 to SA00006B520 for N14P-GV2-B-A2(R3 part).
Change U65 from SA000068A00 to SA000068A20 for N14M-GE-B-A2(R3 part).
U65
N14P-GV2-B-A1 BGA 908P
SA00006B520
GV2@
U65
N14P-GS-A2 BGA 908P
SA000065F00
GS@
Non-support PCIE port8-15:N14M-GM and N14P-GV2
Support PCIE port8-15:N14P-GS
U65A GE@
Part 1 of 7
PCI EXPRESS
GPIO
DACs
I2C
CLK
N14M-GE-B-A2 FCBGA 908P
10/29 Add the RV54 pull down 10k to GND by NV.
11/1 Modify the signal name from GC6_FB_CLAMP to GC6_FB_CLAMP_R
01/22 (GPIO5) Delete Reserve for GPU_STDBY_EN
10/31 Add the RV5 connect to EC side.
03/12 Change the RV5 from 0 ohm to short pad.
10/23 Modify the voltage from +VDD33MISC /+3VS to +3VS_VGA by nvdia suggest.
10/23 Modify the voltage from +VDD33MISC to +3VS_VGA by nvdia suggest.
Reserve for leakage issue
Row resistor
Width: 12~16 mils
Under GPU
30 ohms @100MHz 0402 (ESR=0.05) Bead
78mA
71mA
41mA
Near GPU
01/28 Change the LV7 from SM01000JE00 to SM01000JN00.
11/8 Modify the BOM structure from GCLK@ to @ for without external CLK gen.
Differential signal
0103 Add CV136 0.1uf cap on QV8.2 for N14P-GS/N14P-GV2 GC6.
From EC
10/29 Add the QV8 for GC6 circuit.
0103 Change QV7.2 control from DGPU_PWR_EN to PLT_RST_VGA# for N14P-GS/N14P-GV2 GC6.
For GC6
To EC
10/24 NVIDIA suggest
Modify the voltage from +VDD33MISC/+3VS to +3VS_VGA
Modify the voltage from +VDD33MISC to +3VS_VGA.
Modify the QV1 from N14MGE@ to always mount.
Modify the RV130/RV137 from N14PGS@ to @.
11/30 Modify the LV1 from SM010019400 to SM010028480
180 ohms @100MHz 0603(ESR=0.2) Bead Under GPU(below 150mils)
150mA
11/30 Modify the YV1 from SM010019400 to SM010028480.(Use SM010019400 footprint)
Modify CV37/CV38 from 15pF to 5pF.
Security Classification
Compal Secret Data
Issued Date
2011/06/15
Deciphered Date
2012/07/11
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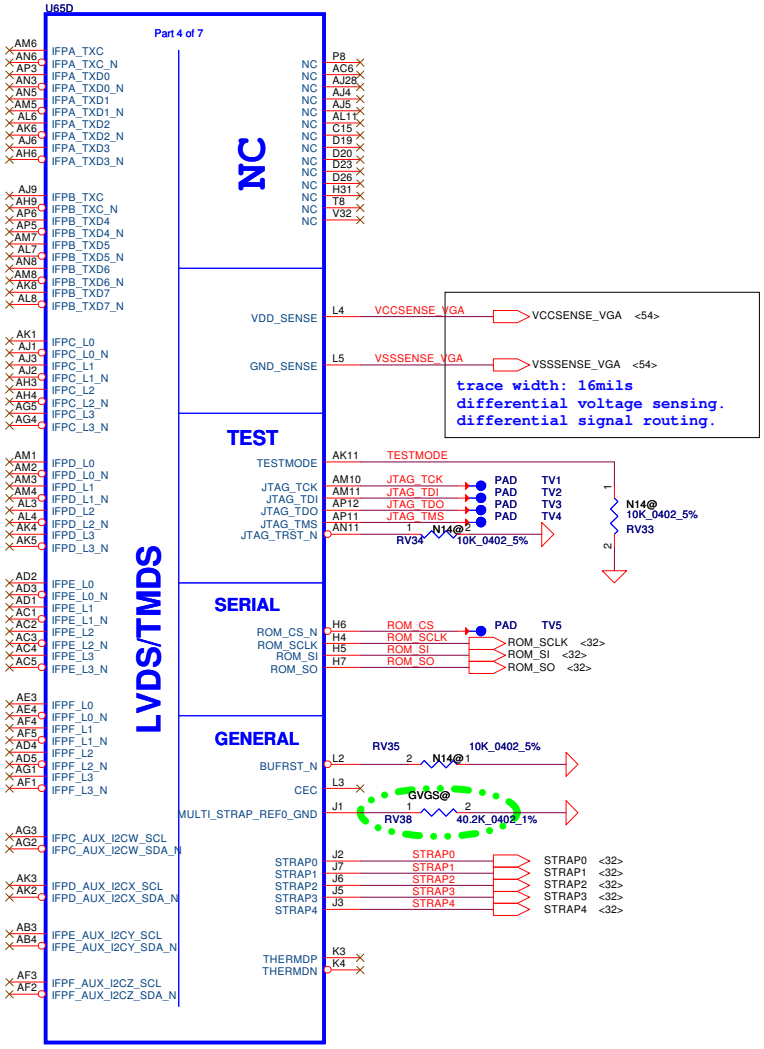
Compal Electronics, Inc.
Title
N14X-PCIE/DAC/GPIO
Size
Document Number
VILG1/G2 MB LA-9901P Schematic
Rev
0.3
Date: Wednesday, March 20, 2013
Sheet 23 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	N14X-LVDS/HDMI/DP/THM		
Size	Document Number	VILG1/G2 MB LA-9901P Schematic	Rev 0.3
Date: Wednesday, March 20, 2013	Sheet 24 of 63		

0128: Change the BOM structure of CV58/CV59/CV278/CV282 from N14@ to GS@.

rise 1.5v system source voltage to 1.55-1.57V

CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

+3VS to +3VS_VGA

Row resistor

+1.5V to +1.5VS_VGA

11/29 Modify the RV138 from 0ohm to short pad.

10/24 Delete QV8/CV72/CV105 and mount RV140.
11/29 Modify the RV140 from 0ohm to short pad.

120 ohms @100MHz 0603 (ESR=0.18) Bead

11/30 Modify the CV63 from 0.01uF to 1uF.
01/28 Change the RV41 from 1k to 150k.
Change the CV63 to SE00000OU00.

11.27 Add the QV4 and RV42.
Modify the RV41 from 200k to 1K for EVT test.
Modify the QV3 from SB00000QP00 to SB00000EN00.
Modify the UV11 from SB00000RV00 to SB548000210.

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

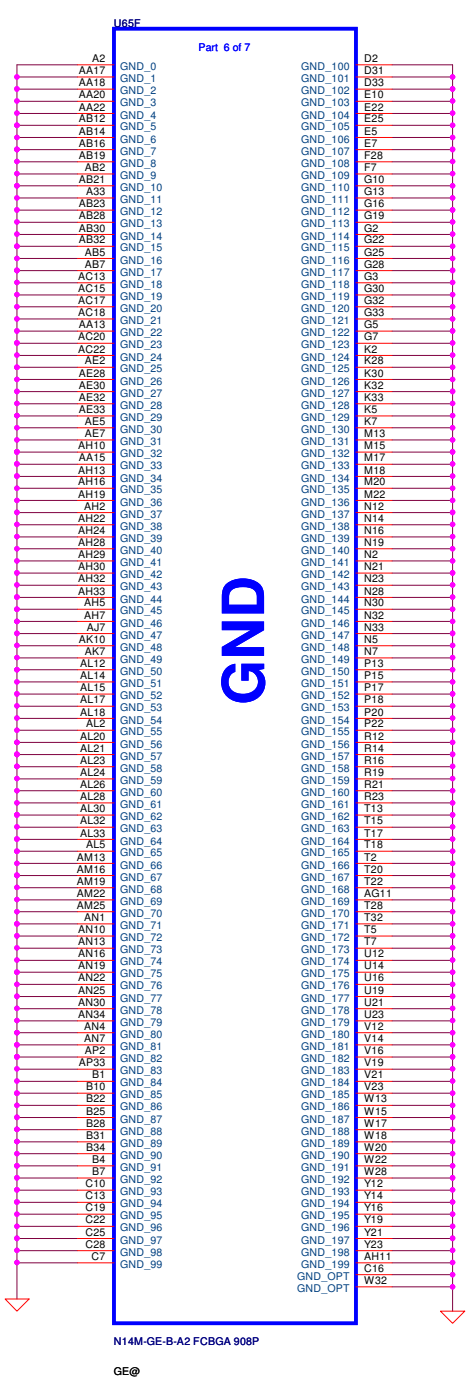
Compal Electronics, Inc.

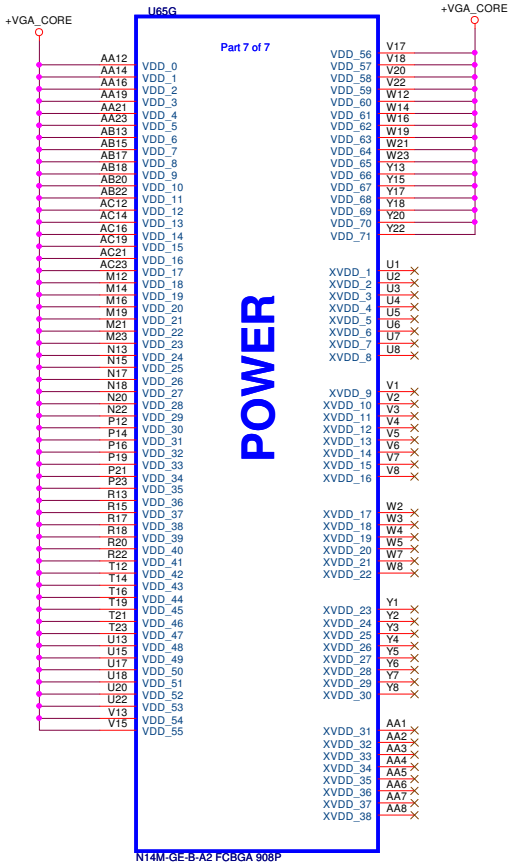
Title: N14X-POWER

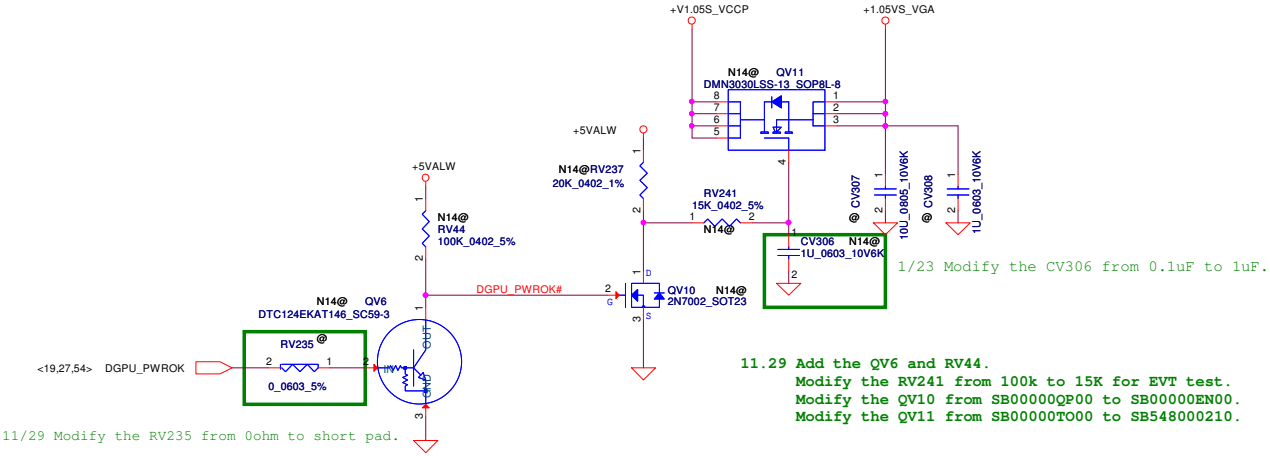
Document Number: VILG1/G2 MB LA-9901P Schematic

Rev: 0.3

Date: Wednesday, March 20, 2013 | Sheet 25 of 63

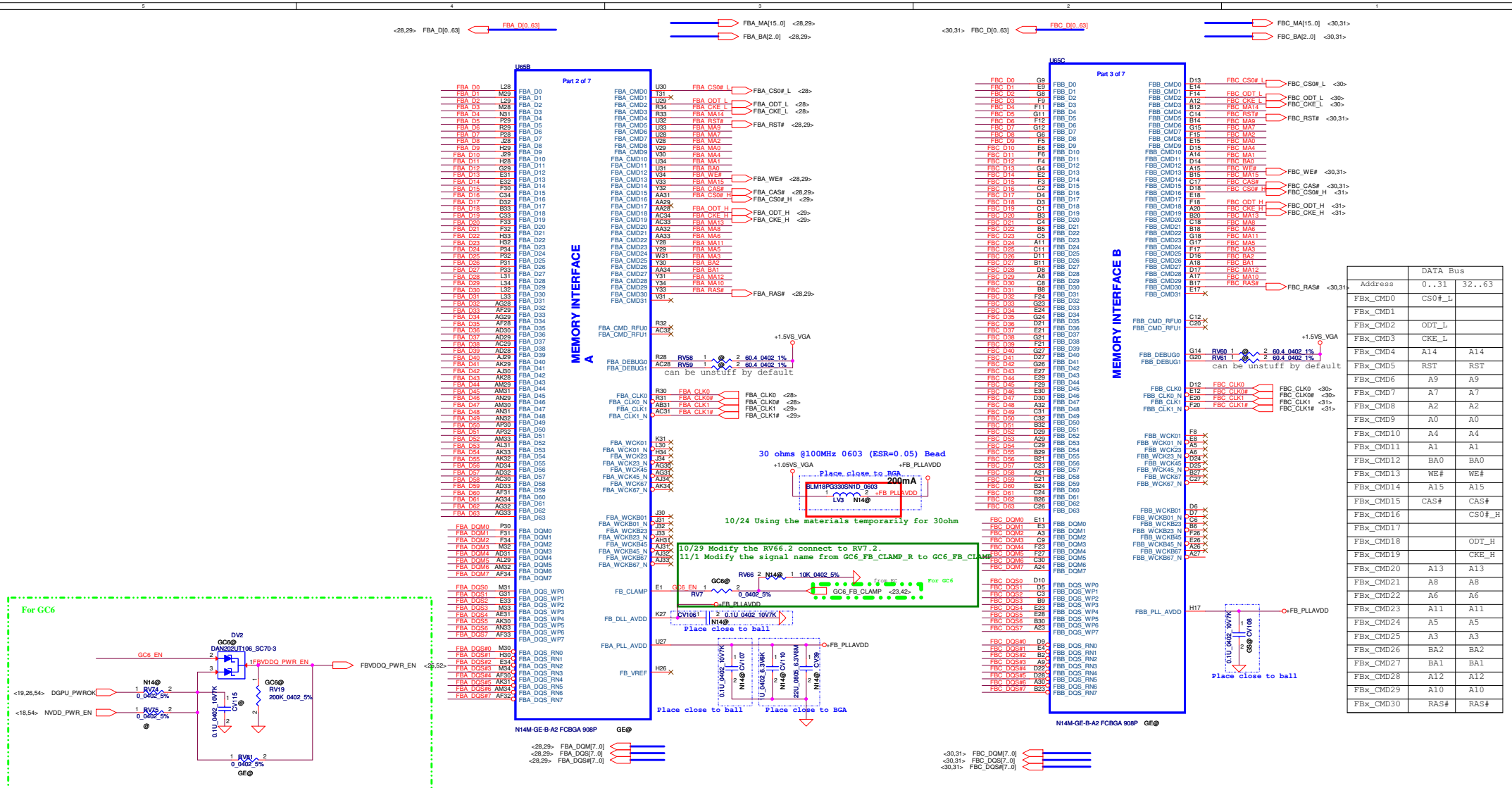






Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.	
Title	N14X-VGA CORE, GND
Size	Document Number: VILG1/G2 MB LA-9901P Schematic
Rev	0.3
Date: Wednesday, March 20, 2013	Sheet 26 of 63



	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: N14X-MEM Interface

Size: A3 | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

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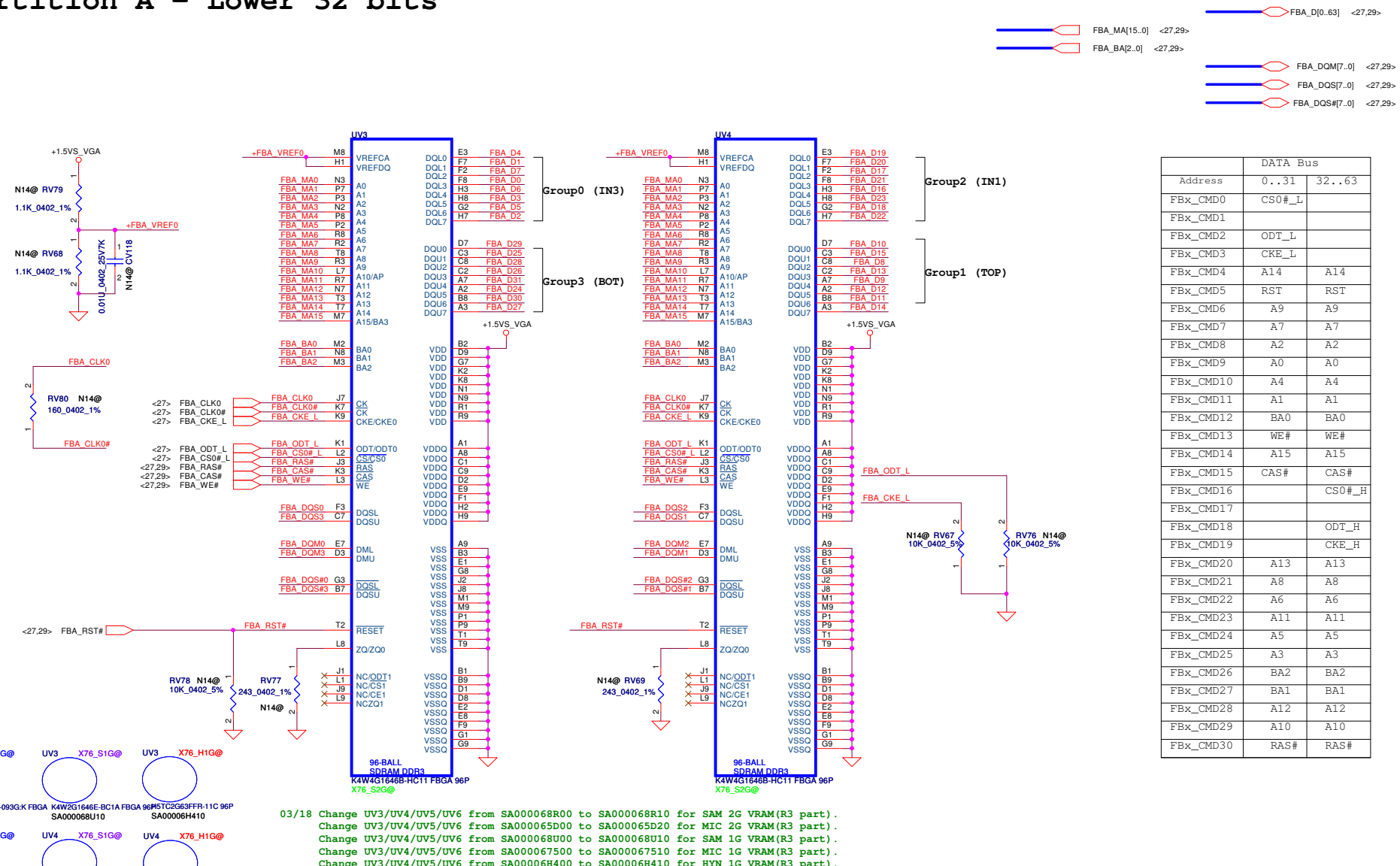
Memory Partition A - Lower 32 bits

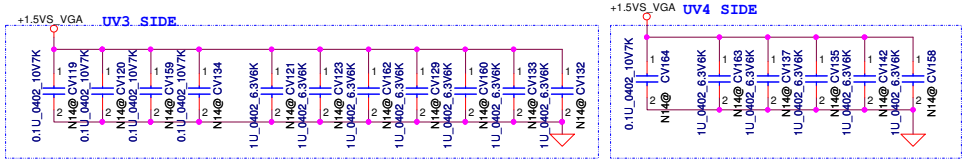


	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

UV3 X76_M2G@ / UV3 X76_M1G@ / UV3 X76_S1G@ / UV3 X76_H1G@
MT41K256M16HA-107G:E SA000065D20 | MT41J128M16JT-093G:K FBGA SA000067510 | K4W2G1646E-BC1A FBGA 96P SA000068U10 | H5TC2G63FFR-11C 96P SA00006H410

UV4 X76_M2G@ / UV4 X76_M1G@ / UV4 X76_S1G@ / UV4 X76_H1G@
MT41K256M16HA-107G:E SA000065D20 | MT41J128M16JT-093G:K FBGA SA000067510 | K4W2G1646E-BC1A FBGA 96P SA000068U10 | H5TC2G63FFR-11C 96P SA00006H410

03/18 Change UV3/UV4/UV5/UV6 from SA000068R00 to SA000068R10 for SAM 2G VRAM(R3 part).
Change UV3/UV4/UV5/UV6 from SA000065D00 to SA000065D20 for MIC 2G VRAM(R3 part).
Change UV3/UV4/UV5/UV6 from SA000068U00 to SA000068U10 for SAM 1G VRAM(R3 part).
Change UV3/UV4/UV5/UV6 from SA000067500 to SA000067510 for MIC 1G VRAM(R3 part).
Change UV3/UV4/UV5/UV6 from SA00006H400 to SA00006H410 for HYN 1G VRAM(R3 part).



0111 Change UV3/UV4/UV5/UV6
from SA000065300 to SA00006H400 for Hynix VRAM

UV3 GV2_M2G@ / UV3 GV2_M1G@ / UV3 GV2_S1G@ / UV3 GV2_H1G@ / UV3 GV2_S2G@
MT41K256M16HA-107G:E SA000065D20 | MT41J128M16JT-093G:K FBGA SA000067510 | K4W2G1646E-BC1A FBGA 96P SA000068U10 | H5TC2G63FFR-11C 96P SA00006H410 | K4W4G1646B-HC11 FBGA 96P SA000068R10

UV4 GV2_M2G@ / UV4 GV2_M1G@ / UV4 GV2_S1G@ / UV4 GV2_H1G@ / UV4 GV2_S2G@
MT41K256M16HA-107G:E SA000065D20 | MT41J128M16JT-093G:K FBGA SA000067510 | K4W2G1646E-BC1A FBGA 96P SA000068U10 | H5TC2G63FFR-11C 96P SA00006H410 | K4W4G1646B-HC11 FBGA 96P SA000068R10

0206 Add UV3/UV4/UV5/UV6 BOM structure for N14P-GV2.

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: N14X-VRAM A Lower

Document Number: VILG1/G2 MB LA-9901P Schematic

Rev: 0.3

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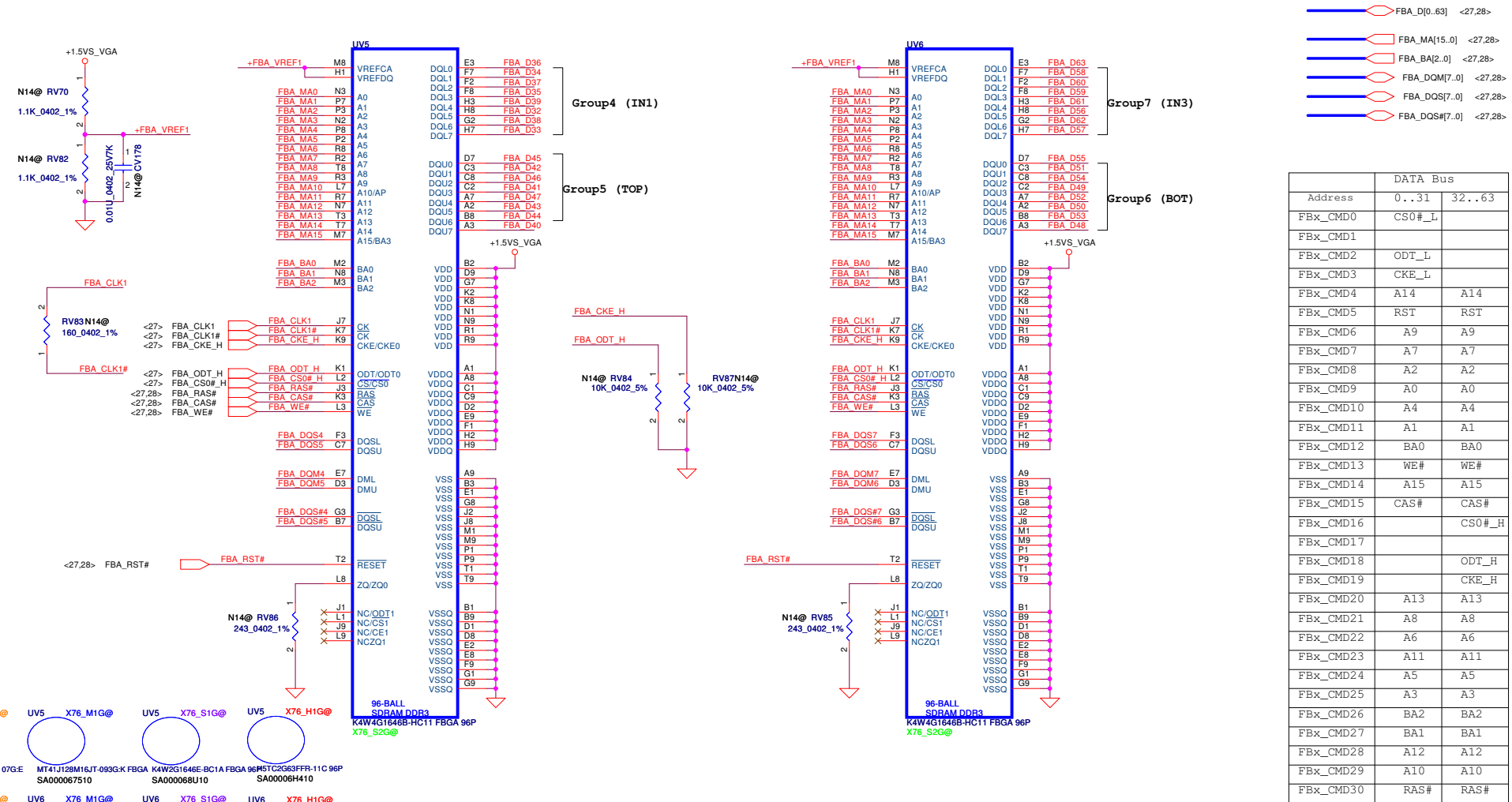
Memory Partition A – Upper 32 bits



FBA_D[0..63] <27,28>
FBA_MA[15..0] <27,28>
FBA_BA[2..0] <27,28>
FBA_DQM[7..0] <27,28>
FBA_DQS[7..0] <27,28>
FBA_DQS#[7..0] <27,28>

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

UV5 X76_M2G@ — MT41K256M16HA-107G:E — SA000065D20
UV5 X76_M1G@ — MT41J128M16JT-093G:K FBGA — SA000067510
UV5 X76_S1G@ — K4W2G1646E-BC1A FBGA 96P — SA000068U10
UV5 X76_H1G@ — H5TC2G63FFR-11C 96P — SA00006H410

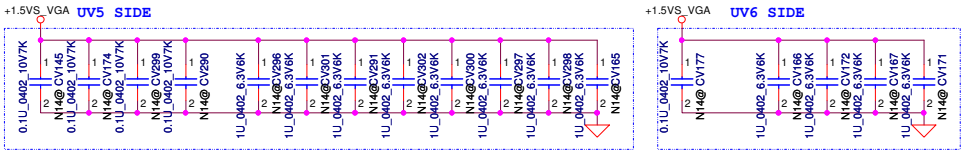
UV6 X76_M2G@ — MT41K256M16HA-107G:E — SA000065D20
UV6 X76_M1G@ — MT41J128M16JT-093G:K FBGA — SA000067510
UV6 X76_S1G@ — K4W2G1646E-BC1A FBGA 96P — SA000068U10
UV6 X76_H1G@ — H5TC2G63FFR-11C 96P — SA00006H410

0111 Change UV3/UV4/UV5/UV6
from SA000065300 to SA00006H400 for Hynix VRAM

UV5 GV2_M2G@ — MT41K256M16HA-107G:E — SA000065D20
UV5 GV2_M1G@ — MT41J128M16JT-093G:K FBGA — SA000067510
UV5 GV2_S1G@ — K4W2G1646E-BC1A FBGA 96P — SA000068U10
UV5 GV2_H1G@ — H5TC2G63FFR-11C 96P — SA00006H410
UV5 GV2_S2G@ — K4W4G1646B-HC11 FBGA 96P — SA000068R10

UV6 GV2_M2G@ — MT41K256M16HA-107G:E — SA000065D20
UV6 GV2_M1G@ — MT41J128M16JT-093G:K FBGA — SA000067510
UV6 GV2_S1G@ — K4W2G1646E-BC1A FBGA 96P — SA000068U10
UV6 GV2_H1G@ — H5TC2G63FFR-11C 96P — SA00006H410
UV6 GV2_S2G@ — K4W4G1646B-HC11 FBGA 96P — SA000068R10

0206 Add UV3/UV4/UV5/UV6 BOM structure for N14P-GV2.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

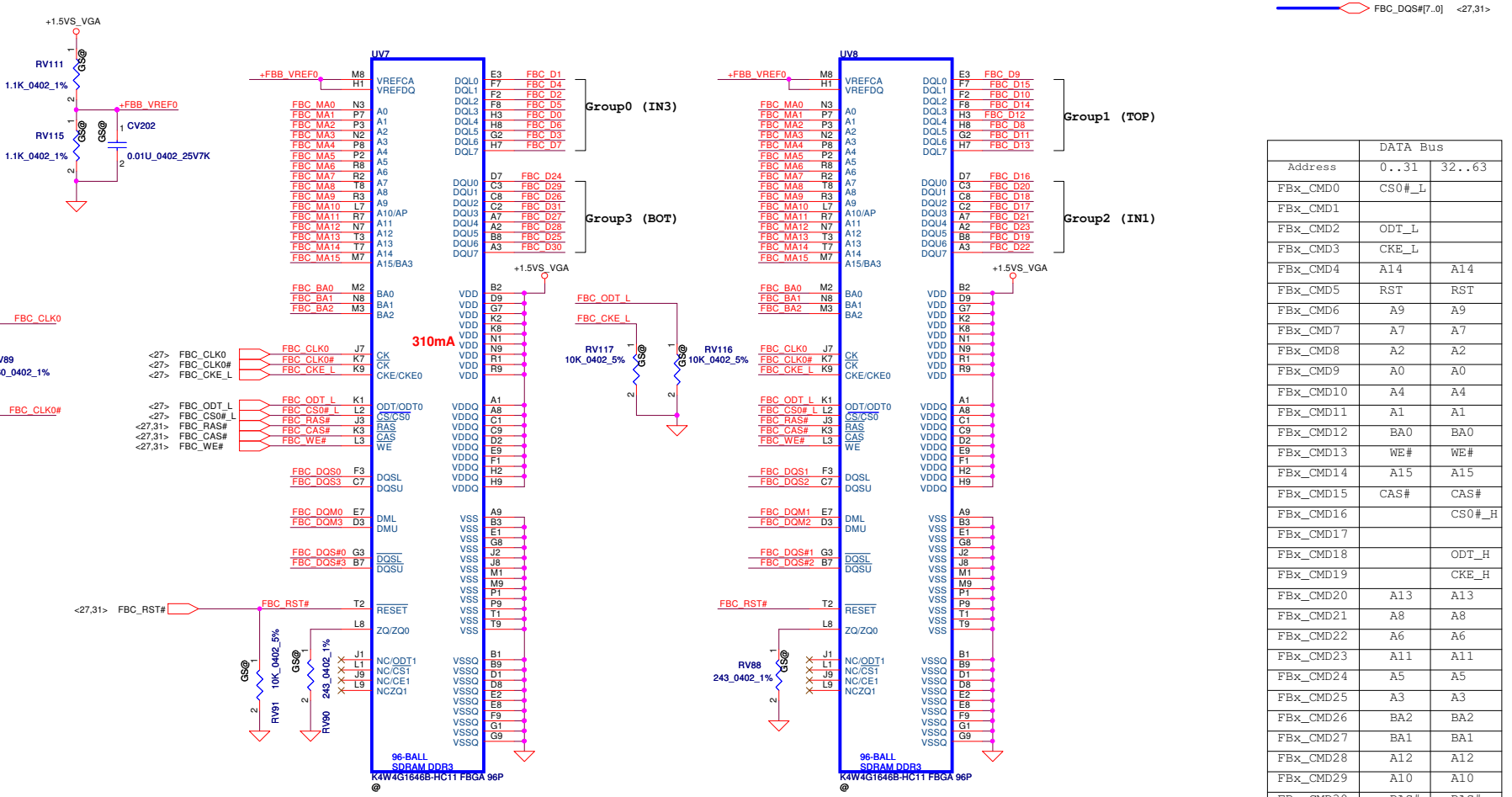
Compal Electronics, Inc.

Title: N14X-VRAM A Upper

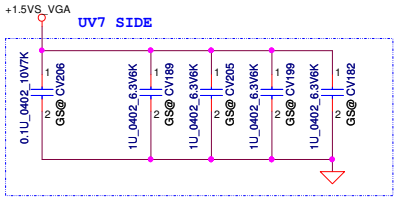
Size: C | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

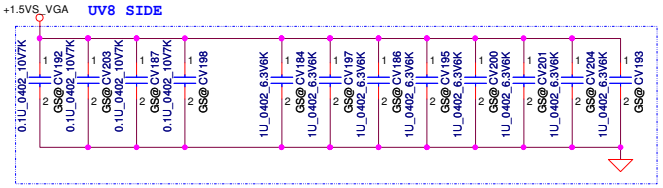
Date: Wednesday, March 20, 2013 | Sheet 29 of 63

Memory Partition C – Lower 32 bits



	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

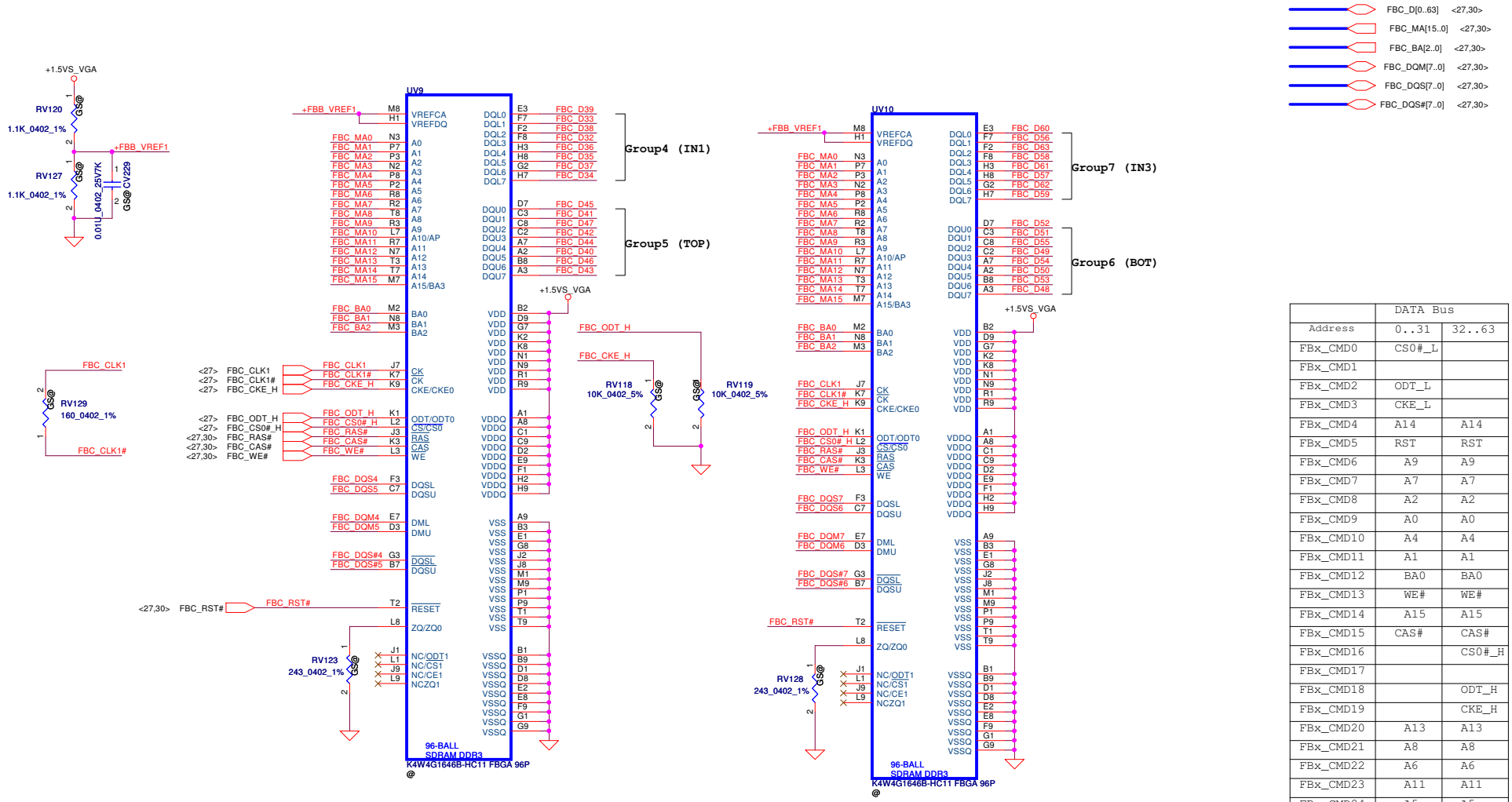
Compal Electronics, Inc.

Title: N14X-VRAM C Lower

Size: Custom | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

Date: Wednesday, March 20, 2013 | Sheet 30 of 63

Memory Partition C – Upper 32 bits



	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: N14X-VRAM C Upper

Size: Custom | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

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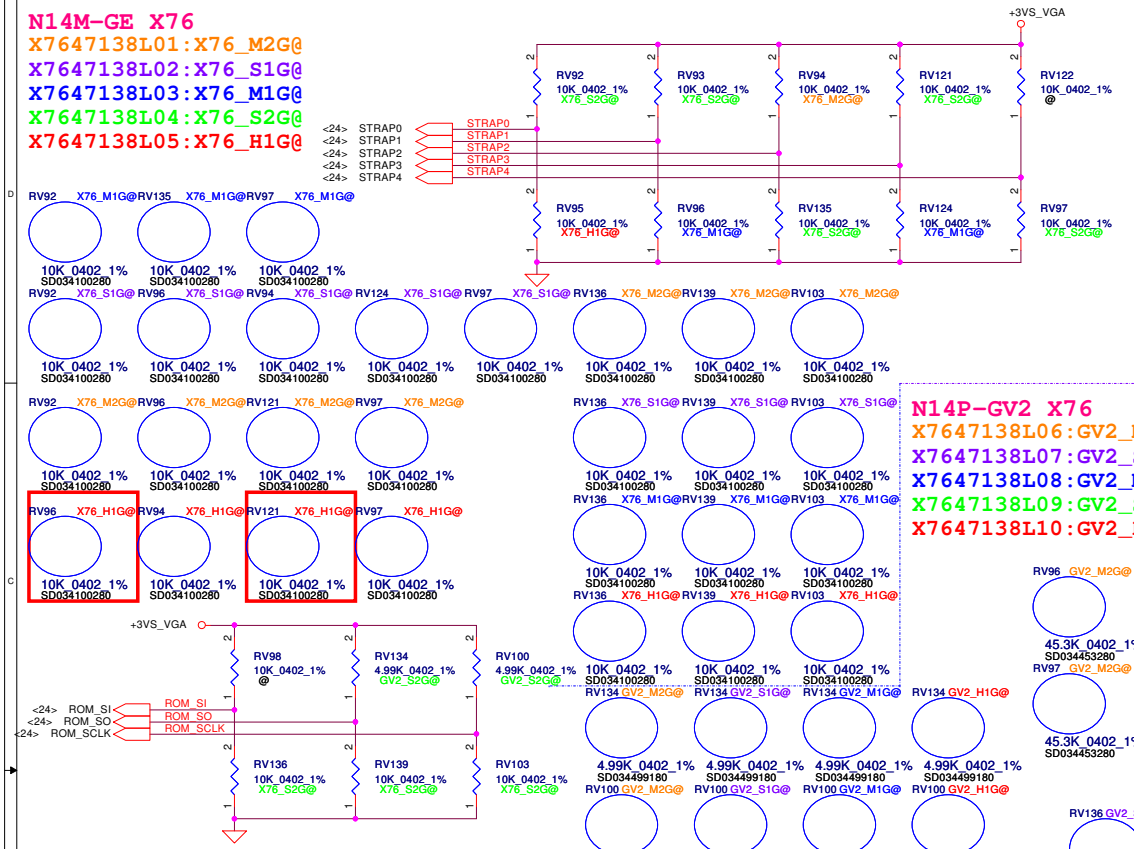
N14M-GE X76
X7647138L01:X76_M2G@
X7647138L02:X76_S1G@
X7647138L03:X76_M1G@
X7647138L04:X76_S2G@
X7647138L05:X76_H1G@



Multi-Level Mode

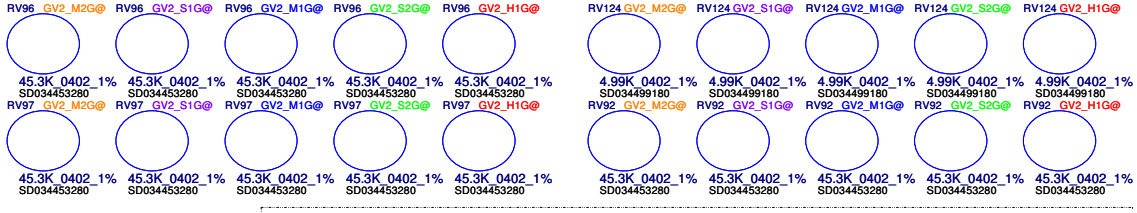
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

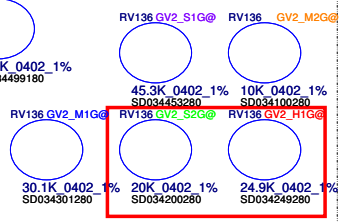
Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Binary-Level Mode

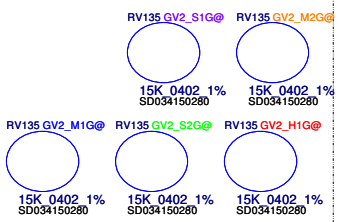
Physical Strapping pin	Strapping Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10K	PD
ROM_SI	SUB_VENDOR	10K	PU(VBIOS ROM) PD(Non-VBIOS ROM)
ROM_SO	VGA_DEVICE	10K	PD(No display)
STRAP0	RAM_CFG[0]	10K	PU (Binary=1) PD (Binary=0)
STRAP1	RAM_CFG[1]	10K	
STRAP2	RAM_CFG[2]	10K	
STRAP3	RAM_CFG[3]	10K	
STRAP4	PCIE_MAX_SPEED	10K	PD

N14P-GV2 X76
X7647138L06:GV2_M2G@
X7647138L07:GV2_S1G@
X7647138L08:GV2_M1G@
X7647138L09:GV2_S2G@
X7647138L10:GV2_H1G@





0206 Change R136 from SD034200200 to SD034200280 for GV2_S2G.
0206 Change R136 from SD034249200 to SD034249280 for GV2_H1G.



For N14P-GV2 strap table X76

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GV2	1 GHz	128M* 16* 4 1GB	Samsung K4W2G1646E-BC1A	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 45K	R PU 5K	R PU 5K
N14P-GV2	1 GHz	128M* 16* 4 1GB	Micron MT41J128M16JT-093G:K	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 30K	R PU 5K	R PU 5K
N14P-GV2	1 GHz	128M* 16* 4 1GB	Hynix H5TC2G63FFR-11C	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 25K	R PU 5K	R PU 5K
N14P-GV2	900 MHz	256M* 16* 4 2GB	Samsung K4W4G1646B-HC11	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 20K	R PU 5K	R PU 5K
N14P-GV2	900 MHz	256M* 16* 4 2GB	Micron MT41K256M16HA-107G:E	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 10K	R PU 5K	R PU 5K

For N14P-GS strap table X76

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GS	1 GHz	128M* 16* 8 2GB	Samsung K4W2G1646E-BC1A	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 45K	R PU 5K	R PD 15K
N14P-GS	1 GHz	128M* 16* 8 2GB	Micron MT41J128M16JT-093G:K	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 30K	R PU 5K	R PD 15K
N14P-GS	1 GHz	128M* 16* 8 2GB	Hynix H5TC2G63FFR-11C	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 25K	R PU 5K	R PD 15K
N14P-GS	900 MHz	256M* 16* 8 4GB	Samsung K4W4G1646B-HC11	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 20K	R PU 5K	R PD 15K
N14P-GS	900 MHz	256M* 16* 8 4GB	Micron MT41K256M16HA-107G:E	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 10K	R PU 5K	R PD 15K

For N14M-GE strap table X76

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14M-GE	1 GHz	128M* 16* 4 1GB	Samsung K4W2G1646E-BC1A	R PU 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	1 GHz	128M* 16* 4 1GB	Micron MT41J128M16JT-093G:K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	1 GHz	128M* 16* 4 1GB	Hynix H5TC2G63FFR-11C	R PU 10K	R PD 10K	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	900 MHz	256M* 16* 4 2GB	Samsung K4W4G1646B-HC11	R PU 10K	R PU 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	900 MHz	256M* 16* 4 2GB	Micron MT41K256M16HA-107G:E	R PU 10K	R PD 10K	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K

VRAM Part Number

Frenq.	Memory Size	Samsung K4W2G1646E-BC1A	Micron MT41J128M16JT-093G:K	Hynix H5TC2G63FFR-11C	Samsung K4W4G1646B-HC11	Micron MT41K256M16HA-107G:E
1 GHz	128M* 16* 8 2GB	SA000068U10	SA000067510	SA00006H410		
900 MHz	256M* 16* 8 4GB				SA000068R10	SA000065D20

SUB_VENDOR

0	No VBIOS ROM
1	BIOS ROM is present (Default)

PEX_PLL_EN_TERM

0	Disable (Default)
1	Enable

XCLK_417

0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE

0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG

0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE

0	Non-Primary 3D Acceleration Device (Class Code 302h)
1	Primary Display or VGA Device (Class Code 300h)

USER Straps

User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG

[3:0]	Description
0110	Gen 1 / Gen 2 Support only
0000	Gen 3 Support

NV update PUN doc for the definition of 3GIO_CONFIG.

PCI_DEVID

GPU Type	DEVID[5]	DEVID[4]	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
N14P-GV2	0	1	0	0	1	0
N14P-GS	1	0	0	0	1	1

PCIE_SPEED_CHANGE_GEN3 / PCIE_MAX_SPEED

	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED
N14P-GV2	1	1
N14P-GS	1	1
	0: Disable PCIE Gen3 operation 1: Enable PCIE Gen3 operation	0: Limit to PCIE Gen1 1: PCIE Gen 2/3 Capable

3GIO_PADCFG[3:0]

Strap1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[2]	3GIO_PADCFG[1]
N14P-GV2	0	1	1	1
N14P-GS	0	0	0	0

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

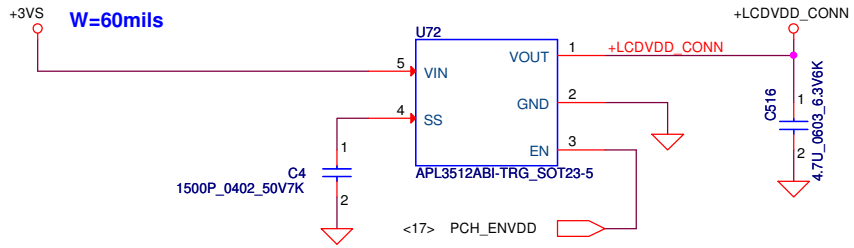
Compal Electronics, Inc.

Title: N14X-MISC

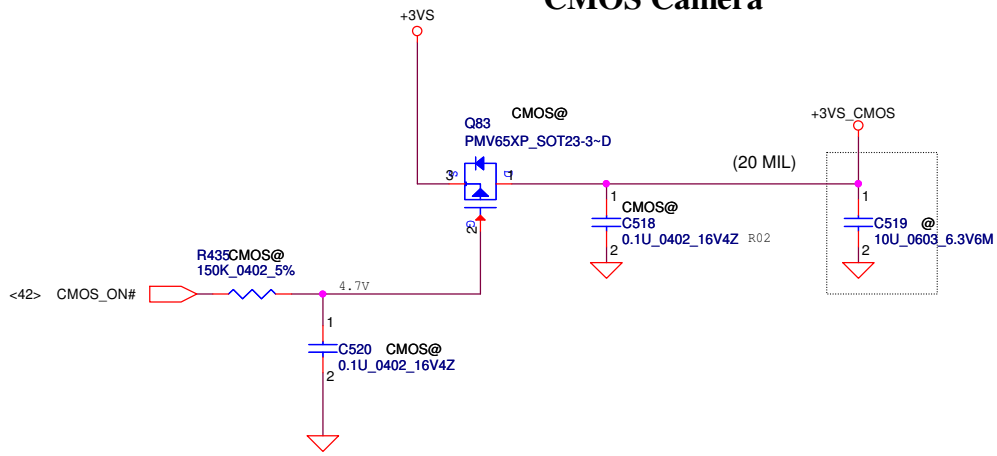
Size: Custom | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

Date: Wednesday, March 20, 2013 | Sheet 32 of 63

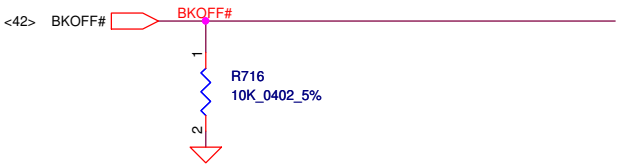
LCD POWER CIRCUIT

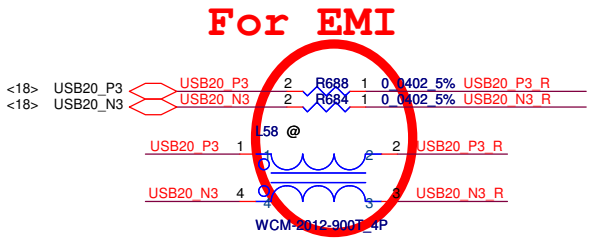


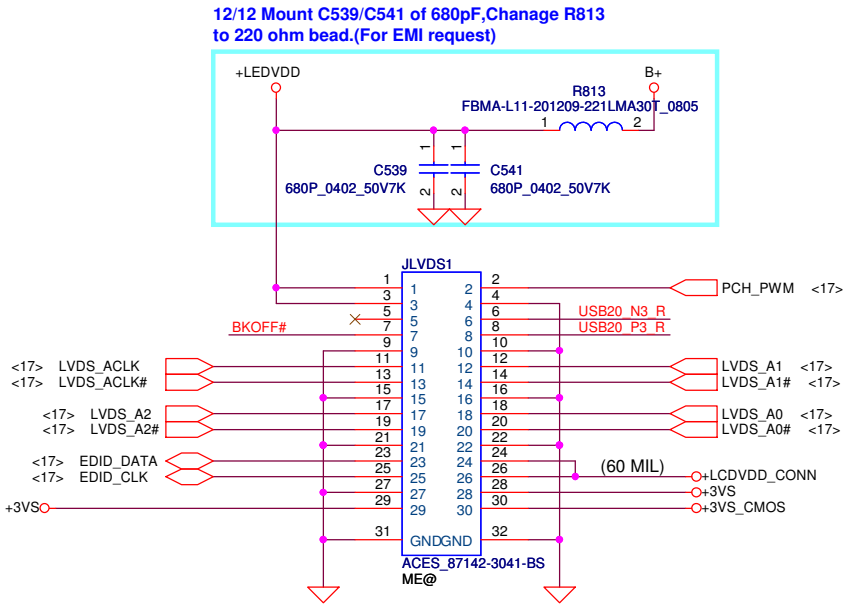
CMOS Camera



VGA LCD/PANEL BD. Conn.







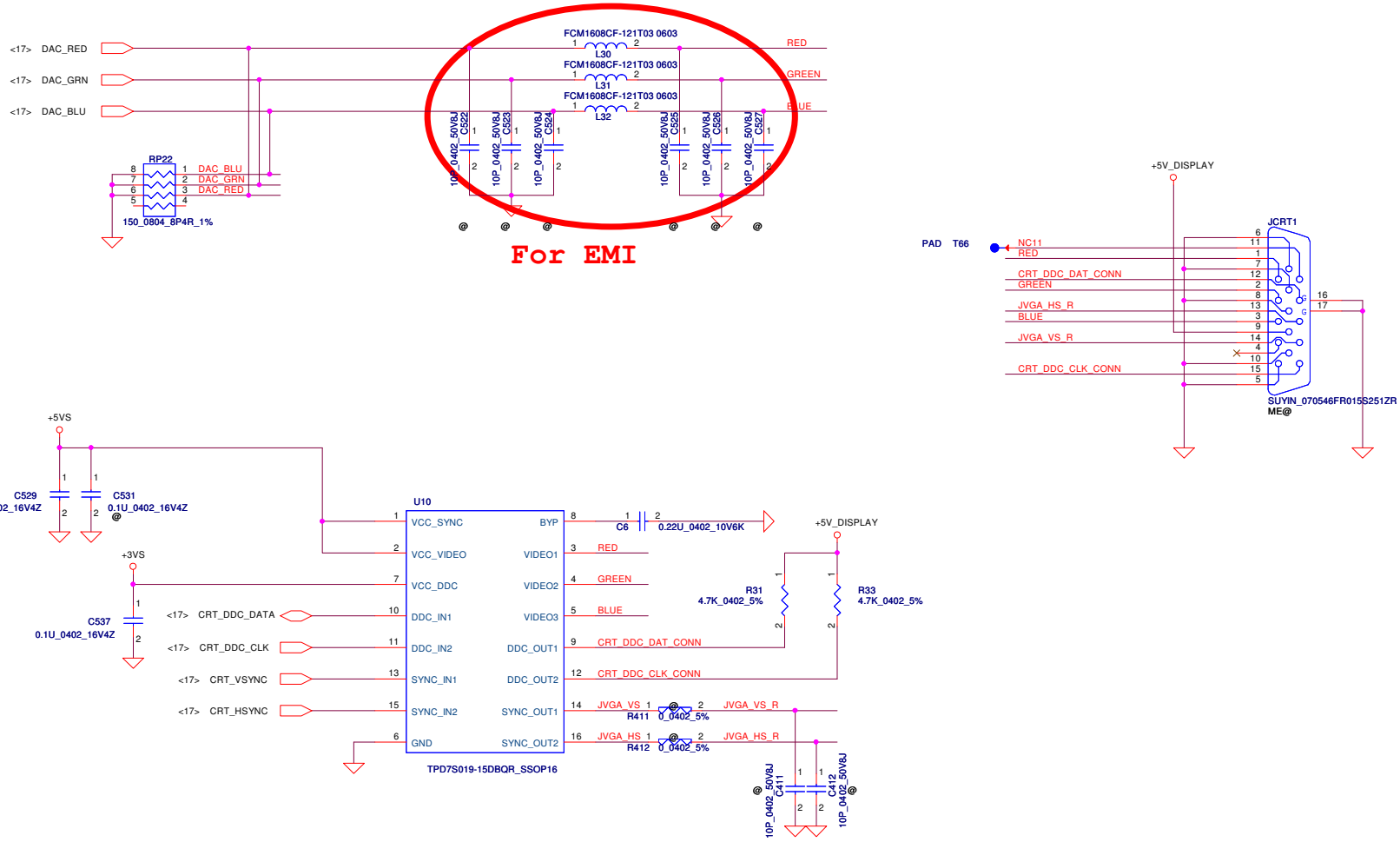
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LVDS/CAMERA

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 33 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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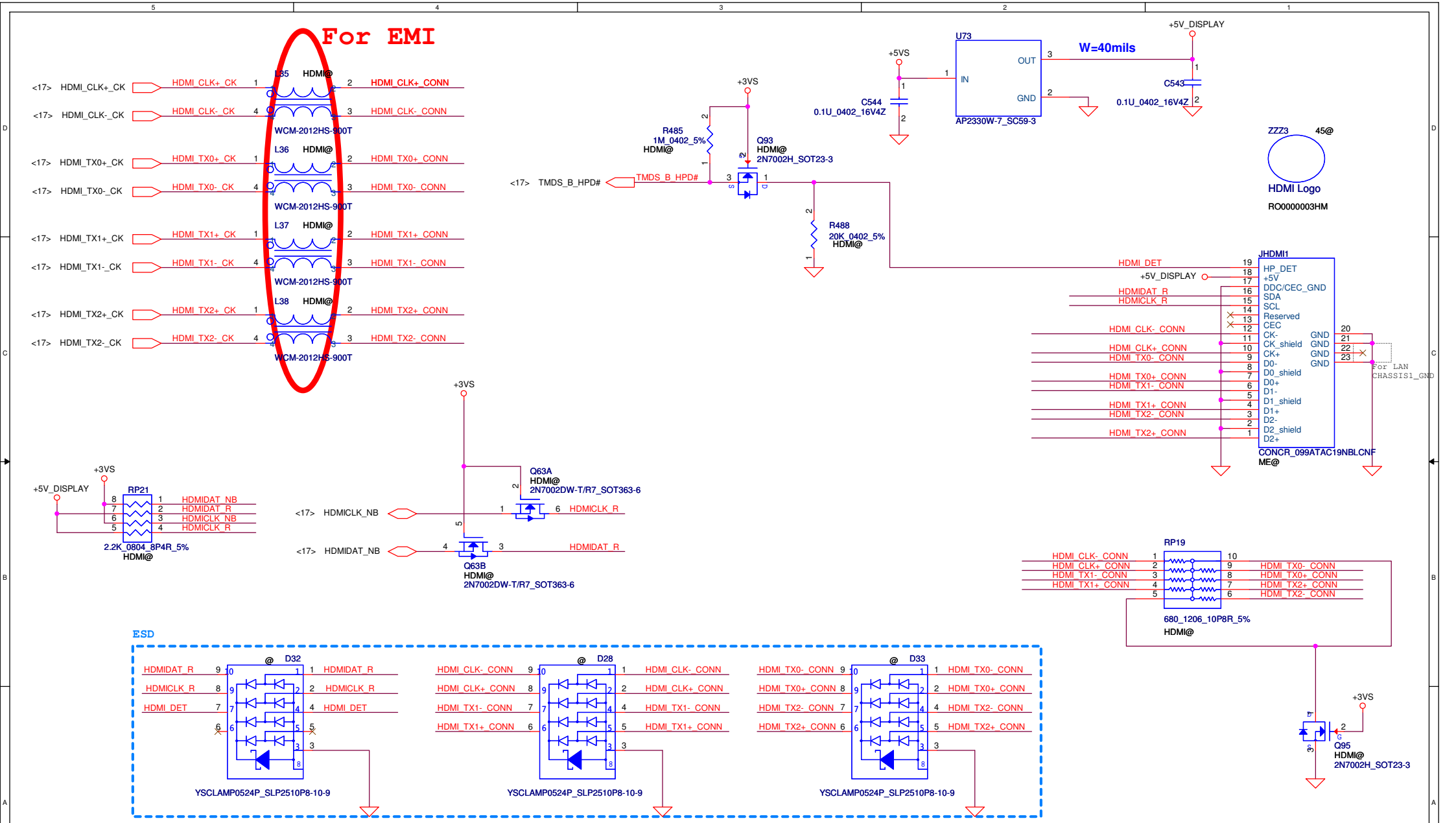
Compal Electronics, Inc.

Title: **CRT Connector**

Size: Custom | Document Number: **VILG1/G2 MB LA9901P Schematic** | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 34 of 63



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

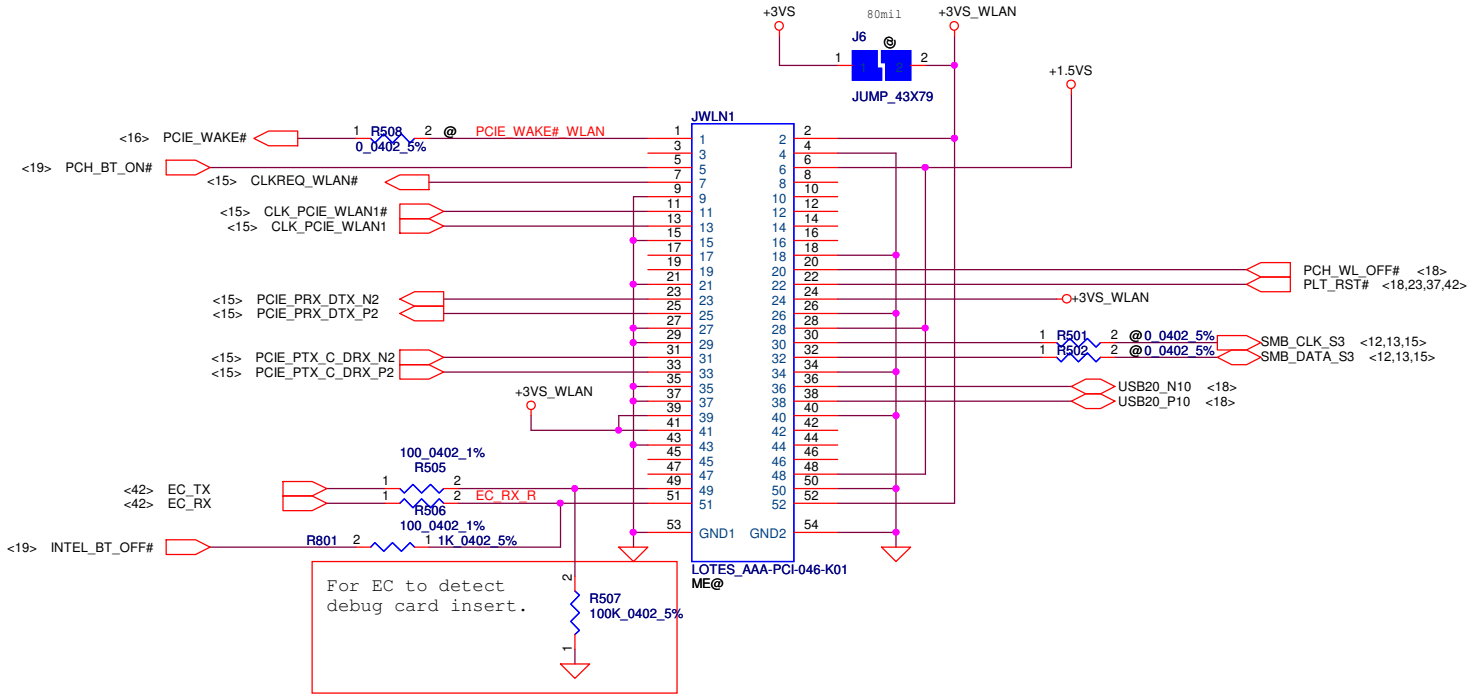
Compal Electronics, Inc.

Title: **HDMI CONN**

Size	Document Number	Rev
B	VILG1/G2 MB LA9901P Schematic	1.0

Date: Wednesday, March 20, 2013 Sheet 35 of 63

Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: Mini-Card/NEW Card/SIM

Size | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 36 of 63

For LAN & Green CLK

+3VALW, +3V_LAN

J12 @ JUMP_43X79

QL1 LP2301ALT1G-SOT23-3

<42> LAN_PWR_ON# — LAN_PWR_ON# — RL3 @ — 10K_0402_5% — CL7 @ 0.1U_0402_16V7K

Vendor recommand reseve the PU resistor close LAN chip

+3V_LAN — RL4 @ 4.7K_0402_5% — PLT_RST#

<18,23,36,42> PLT_RST#

UL1 8172@ QCA8172-BL3A-R

Close together

+LX — LL1 SWR@ 4.7UH_SIA4012-4R7M_20% — +LX_R

CL1 1000P_0402_50V7K, CL2 0.1U_0402_16V4Z, CL3 10U_0603_6.3V6M

SWR@SWR@SWR@

Note: Place Close to LAN chip
LL1 DCR< 0.15 ohm
Rate current > 1A

Close to Pin40

+1.1_AVDDL_L — LL2 FBMA-L11160808601LMA10T_2P — +1.1_AVDDL — LL3 SWR@ FBMA-L11160808601LMA10T_2P — +LX_R

CL4 0.1U_0402_16V4Z, CL5 1U_0402_6.3V4Z, CL6 4.7U_0603_6.3V6K

Place close to Pin34

Pin	Configure signal	Description	
LED[1]	Regulator select	1	Switch mode regulator(SWR) mode
		0	Linear regulator (LDO) mode *

Place Close to Chip

UL1 Atheros AR8151/AR8161

<15> PCIE_PRX_DTX_N1 — CL9 0.1U_0402_16V7K — PCIE_PRX_C_DTX_N1 — TX_N
<15> PCIE_PRX_DTX_P1 — CL11 0.1U_0402_16V7K — PCIE_PRX_C_DTX_P1 — TX_P
<15> PCIE_PTX_C_DRX_N1 — RX_N
<15> PCIE_PTX_C_DRX_P1 — RX_P
<15> CLK_PCIE_LAN# — REFCLK_N
<15> CLK_PCIE_LAN — REFCLK_P
PLT_RST# — PERST#
PCIE_WAKE#_R — WAKE#
<42> LAN_WAKE# — RL7 0 0402 5%
+3V_LAN — RL9 @ 4.7K_0402_5%
SMCLK, SMDATA
NC, TESTMODE

Vendor recommand reseve the PU resistor close LAN chip

LAN_XTALO — XTLO
LAN_XTALI — XTLI
+3V_LAN — RL11 @ 4.7K_0402_5%
<15> CLKREQ_LAN# — CLKREQ#

+1.1_AVDDL ×5, +1.1_AVDDL_L — AVDDL ×5, AVDDL_REG/AVDDL

GND

AR8162-BL3A-R_QFN40_5X5
8162@

LED_0, LED_1, LED_2 — RL12 @ 10K_0402_5% — LDO@ — mount RL12 if use LDO modue

TRXN0 MDI0- <38>, TRXP0 MDI0+ <38>, TRXN1 MDI1- <38>, TRXP1 MDI1+ <38>, TRXN2, TRXP2, TRXN3, TRXP3

RBIAS — LAN_RBIAS — RL8 2.37K_0402_1% — Place Close to PIN1

VDD33 — +3V_LAN

LX — +LX — RL10 30K_0402_5% — +3V_LAN

VDDCT/ISOLAN — +1.7_VDDCT

DVDDL/PPS, DVDDL_REG/DVDDL — +LX_R

AVDDH/AVDD33, AVDDH, AVDDH_REG — +3V_LAN, +2.7_AVDDH ×2

Place Close to PIN1

+3V_LAN — CL12 1000P_0402_50V7K, CL13 0.1U_0402_16V4Z, CL14 1U_0402_6.3V4Z, CL15 10U_0603_6.3V6M, CL16 10U_0603_6.3V6M

don't @ (could be B C cost done)

+3V_LAN — CL10 0.1U_0402_16V4Z, CL8 1U_0402_6.3V4Z

Place close to Pin16

CL17 0.1U_0402_16V4Z — Near Pin13
CL18 0.1U_0402_16V4Z — Near Pin19
CL19 0.1U_0402_16V4Z — Near Pin31
CL20 1U_0402_6.3V4Z, CL21 0.1U_0402_16V4Z — Near Pin6
CL22 0.1U_0402_16V4Z, CL23 1U_0402_6.3V4Z — Near Pin9
CL24 0.1U_0402_16V4Z — Near Pin22
CL25 0.1U_0402_16V4Z, CL26 1U_0402_6.3V4Z — Near Pin37

For EMI
B Phaes change to GCLK@

<44> GCLK_LAN_25MHZ — RL13 @ 0 0402 5%

value shoud be discuss
ORB 5P

CL27 5P_0402_50V8C @ — LAN_XTALI

YL1 NC OSC OSC NC 25MHZ_10PF_7V25000014 — LAN_XTALO

CL28 15P_0402_50V8J NOGCLK@
CL29 15P_0402_50V8J NOGCLK@

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN-AR8162/8172

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 37 of 63

ESD

Place Close to TL1

DL1
1'S PN:SC300001G00
2'S PN:SC300002E00

@
DL1
AZC099-04S.R7G_SOT23-6

Reserve gas tube for EMI go rural solution

For EMI

RL14
75_0805_5%

CL30
10P_0603_50V

CHASSIS1_GND

DL1
BS4200N-C-LV_SMB-F2
GAS@

Place Close to TL1

TL1
MHPC_NS681612A

For EMI

12/12 Change BOM Structure of CL31 from @ to mount(EMI request)

CL31
0.01U_0402_16V7K

For EMI

CL63 1 2 0.1U_0603_50V7K

CHASSIS1_GND

JLAN1
PS_HPKR0125-08A1A0R
ME@

CHASSIS1_GND

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

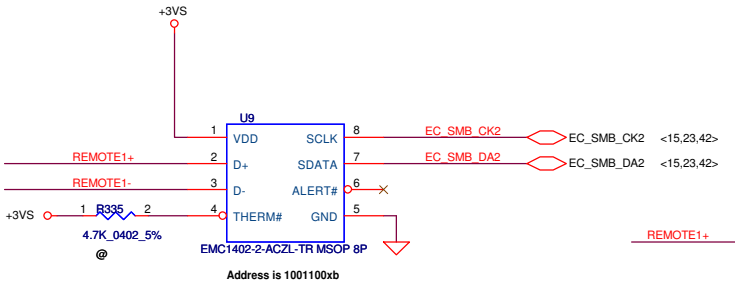
Title: LAN_Transformer

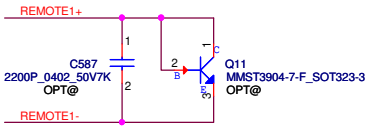
Size: B | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 38 of 63

2 Channel

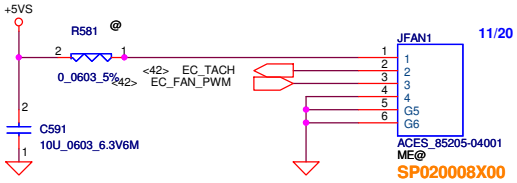
SMSC thermal sensor placed near VRAM





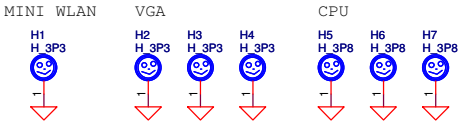
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

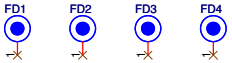
FAN1 Conn

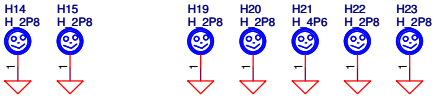


11/20 Change symbol of JFAN1 to SP020008X00

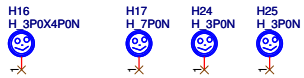
MINI WLAN VGA CPU







R



E

M/B 橢圓孔

M/B 圓孔

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **Fintek-Thermal IC/FAN/screw**

Size: Custom | Document Number: **VILG1/G2 MB LA9901P Schematic** | Rev: 1.0

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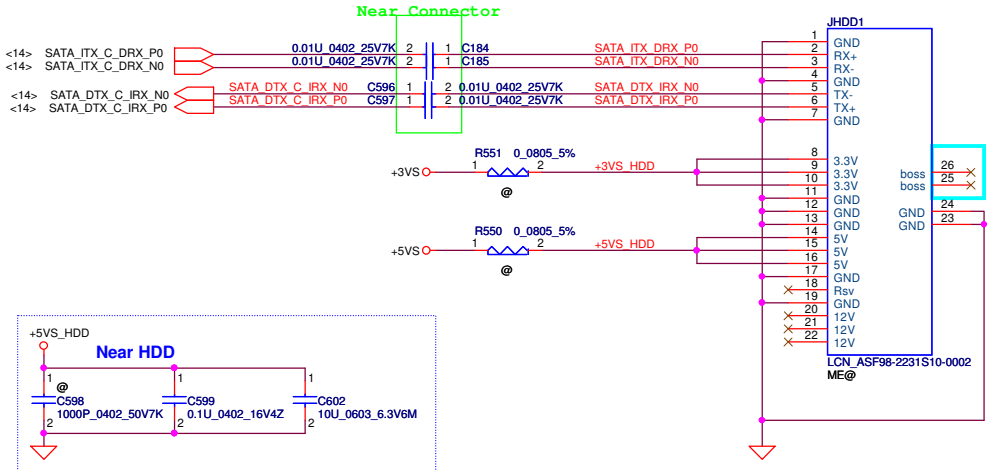
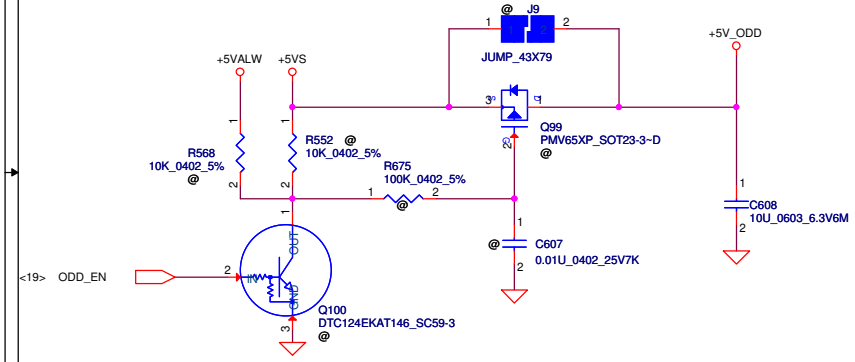
SATA HDD Conn.



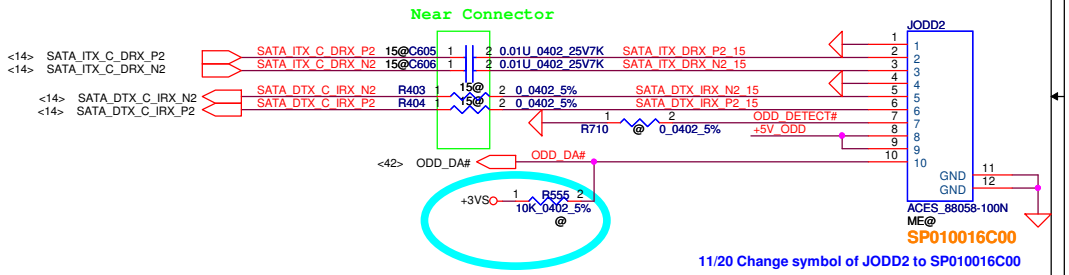
1/16 Change footprint of JHDD1 from SANTA_191501-1_22P to LCN_ASF98-2231S10-0002_22P (DC010005W00 toDC010009C00)

ODD Power Control



FOR 15"

SATA ODD FFC Conn.

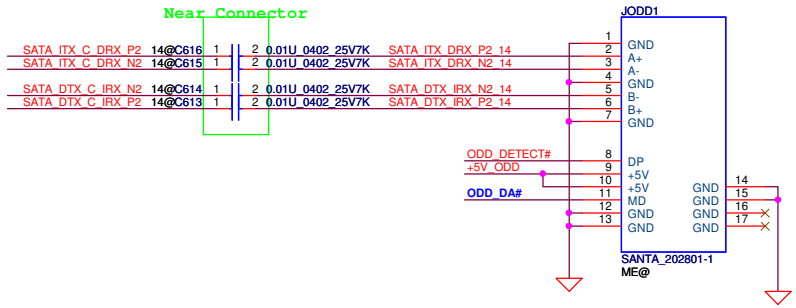


11/20 Change symbol of JODD2 to SP010016C00

Co-lay

FOR 14"

SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **HDD/ODD/BT Connector**

Size: Custom | Document Number: **VILG1/G2 MB LA9901P Schematic** | Rev: 1.0

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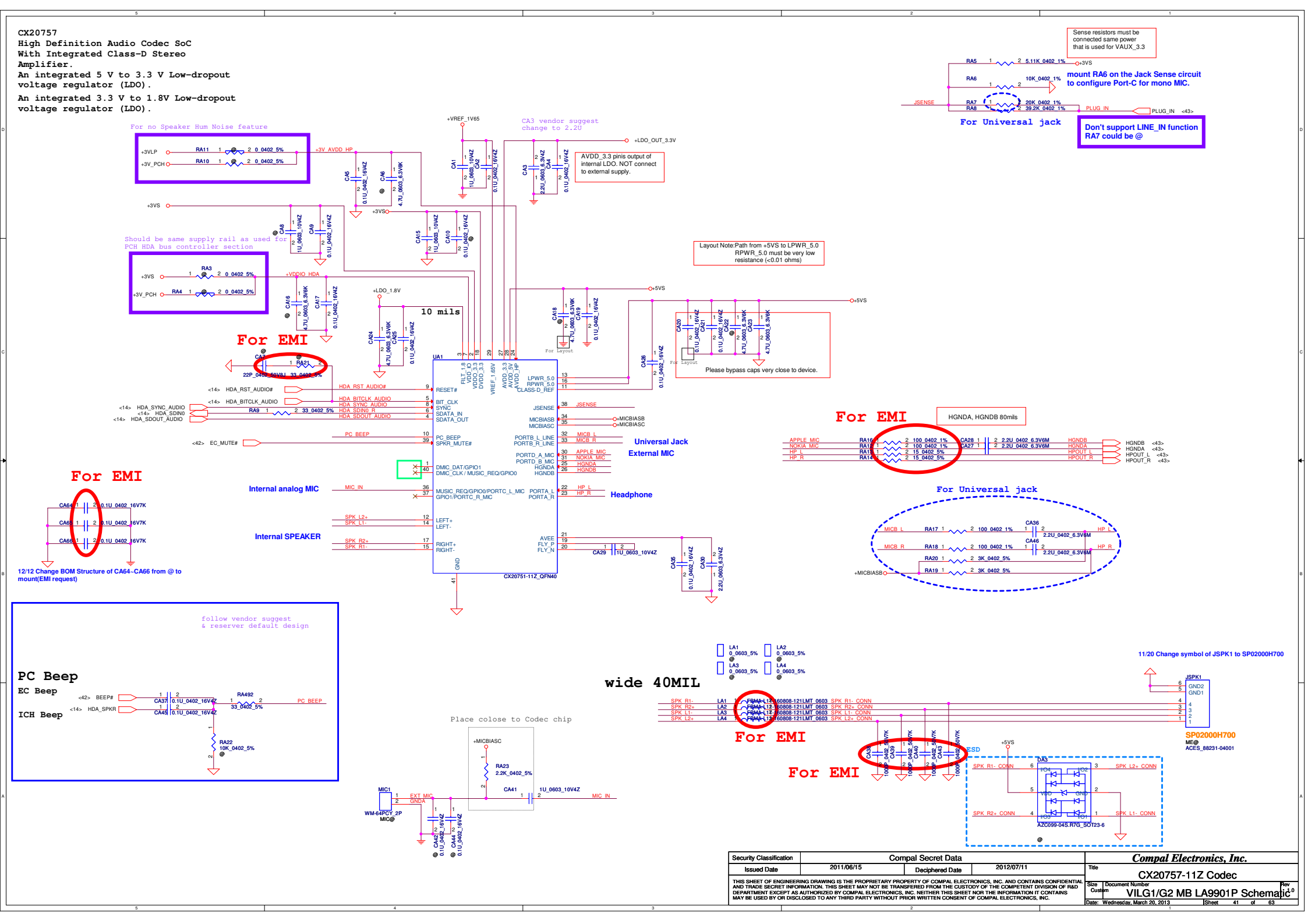
CX20757
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CX20757-11Z Codec

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

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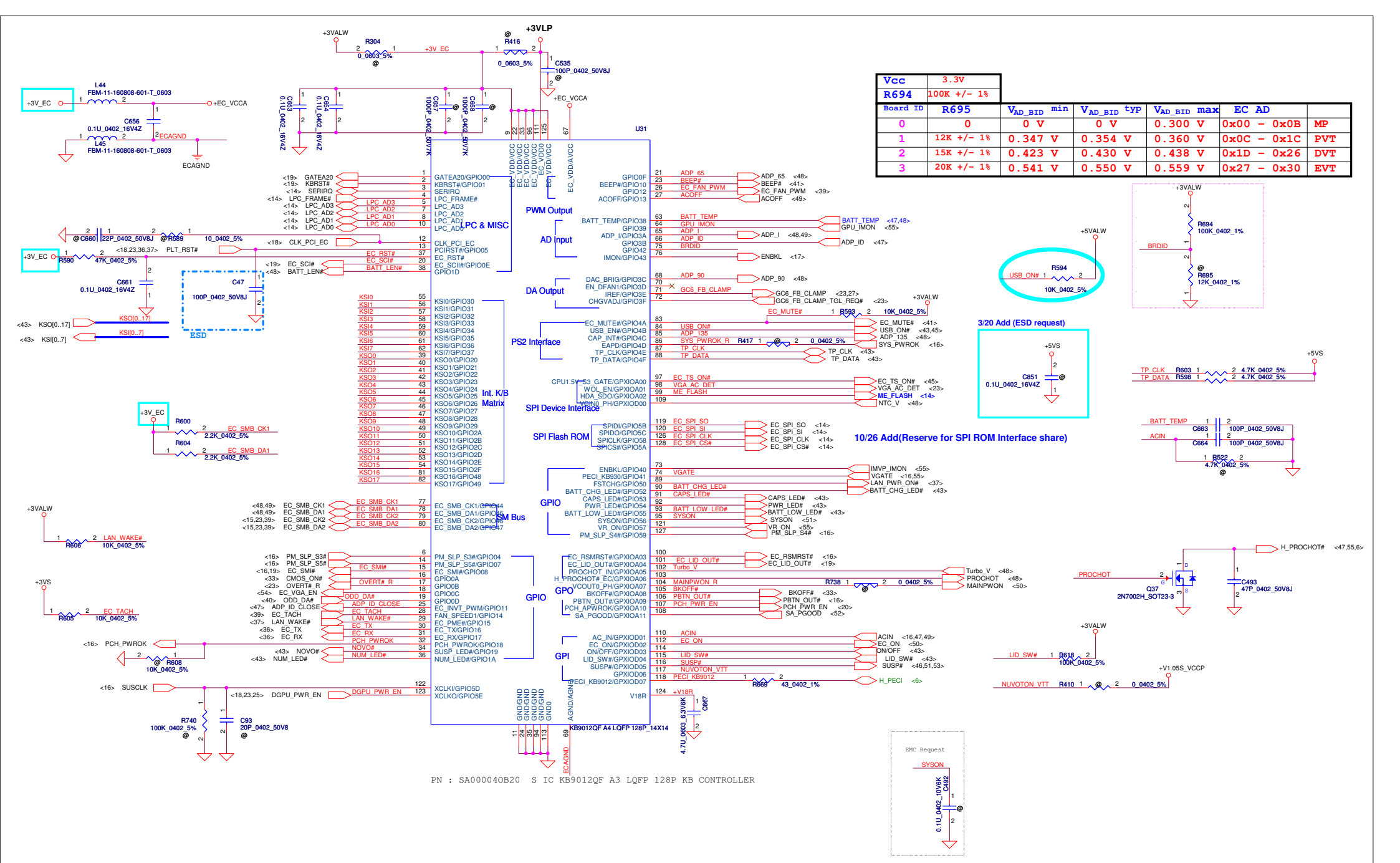


Vcc	3.3V					
R694	100K +/- 1%					
Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0.300 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30	EVT

PN : SA00004OB20 S IC KB9012QF A3 LQFP 128P KB CONTROLLER

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

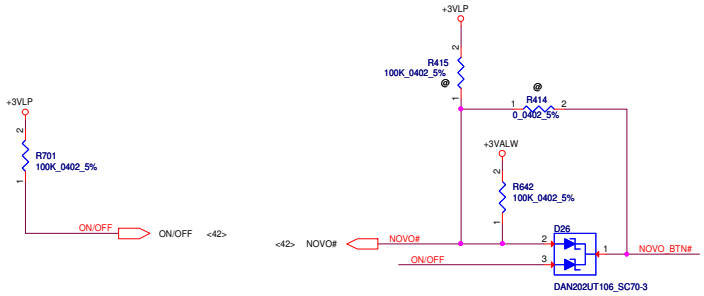
Compal Electronics, Inc.

Title: BIOS & EC I/O Port

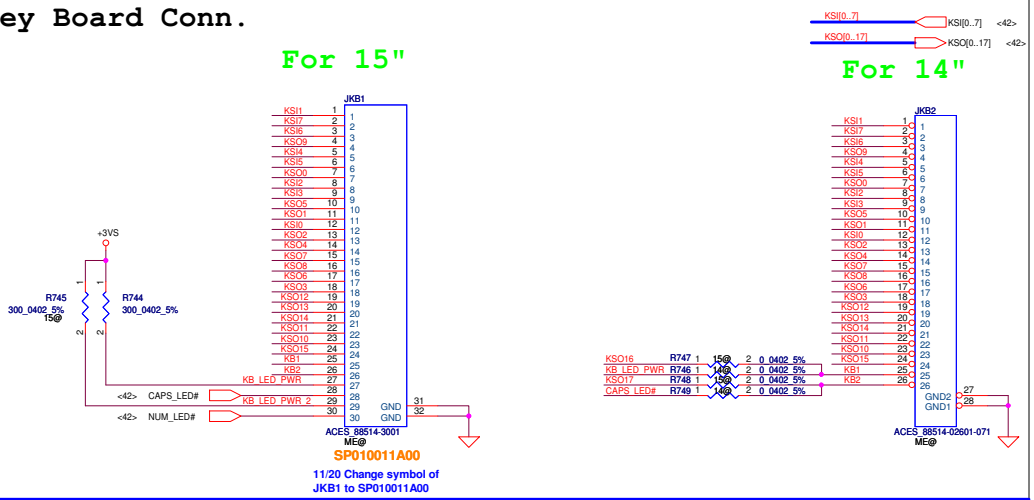
Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 42 of 63

PWR Button For Debug

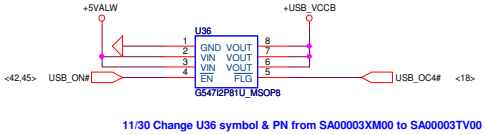


Key Board Conn.

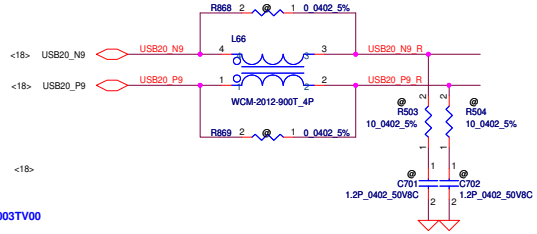


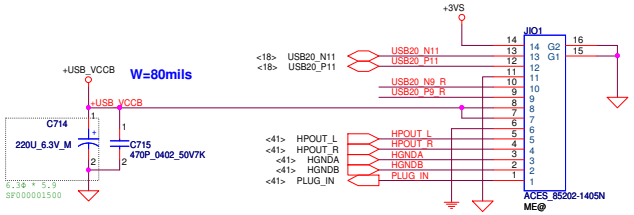
IO/B Conn.

Ext. USB2.0

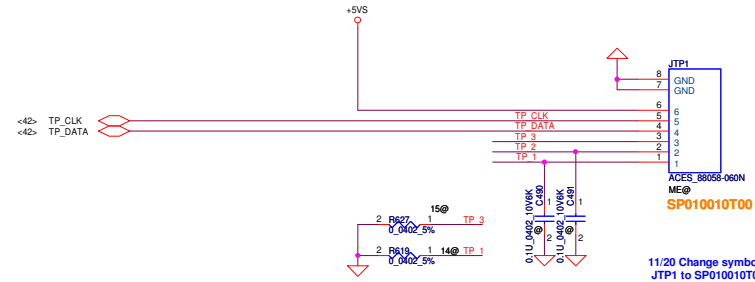


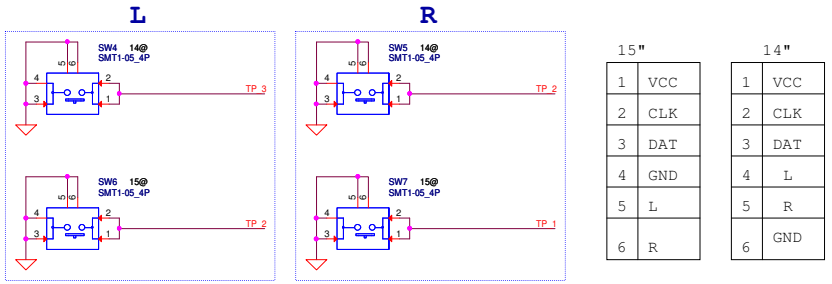
For EMI





TP Switch & TP Conn.





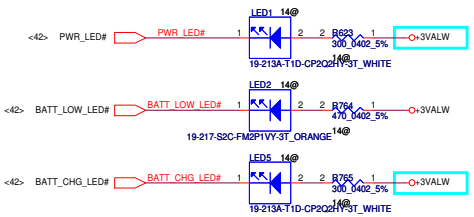
15"

1	VCC
2	CLK
3	DAT
4	GND
5	L
6	R

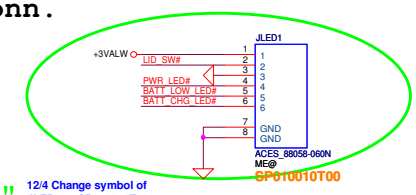
14"

1	VCC
2	CLK
3	DAT
4	L
5	R
6	GND

LED



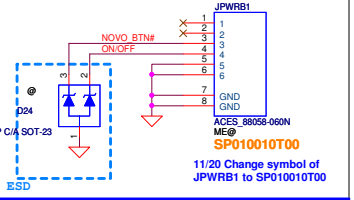
LED/B Conn.



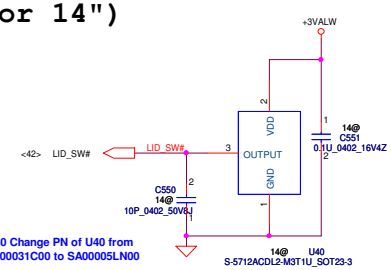
For 15"

12/4 Change symbol of
JLED1 to SP010010T00

PWR/B Conn.



Lid SW(For 14")



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: ROM/KBD/PWR/CR/LED/TP Conn.

Size: C | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

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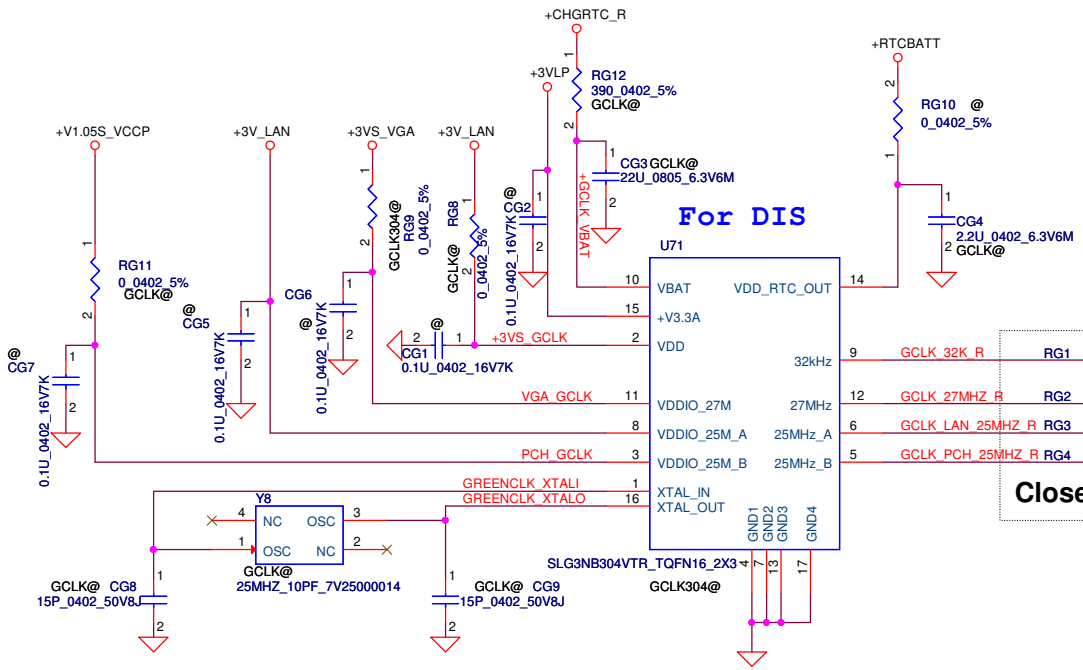
For UMA

U71 GCLK244@

SLG3NB244VTR_TQFN16_2X3

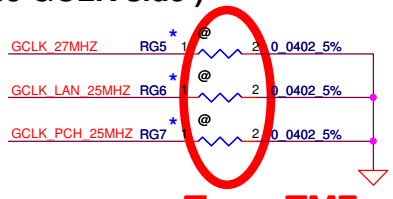
Every power trace need:
W=20mils

For GreenCLK generate CLK:
Mount: All parts in this page except Swing Level RES (Marked "*")
NA: PD108,
Y1,R98,C180,C181,
Y2,R169,C196,C197,
Y6,C968,C969



PCH_32.768K
NV_GPU
LAN
PCH_25M

Reserved for Swing Level adjustment
(Close GCLK side)



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: USB ext. ports

Size: B | Document Number: **VILG1/G2 MB LA9901P Schematic** | Rev: 1.0

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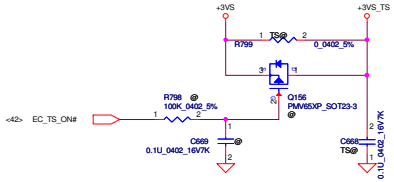
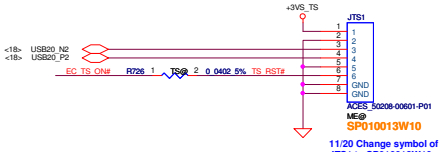
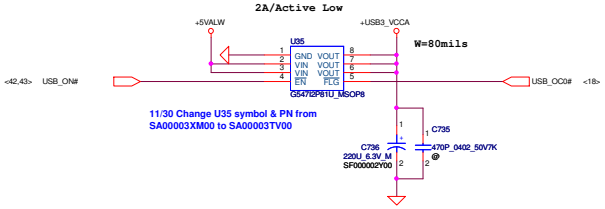
Touch Screen





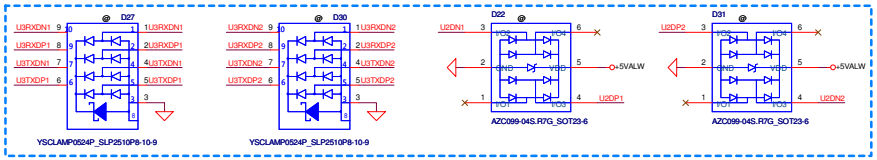
11/20 Change symbol of JTS1 to SP010013W10

USB3.0

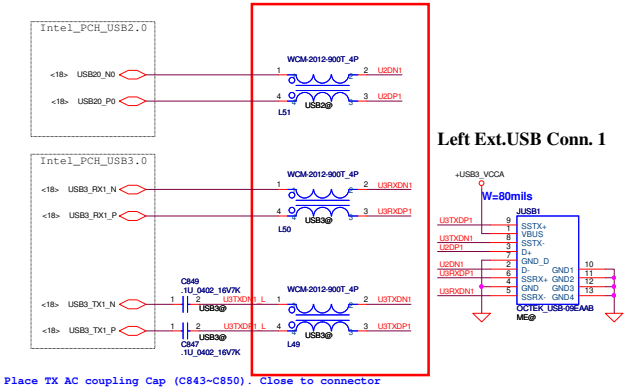


11/30 Change U35 symbol & PN from SA00003XM00 to SA00003TV00

ESD



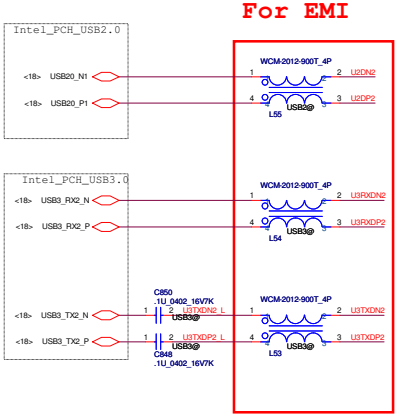
For EMI



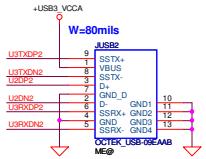
Place TX AC coupling Cap (C843~C850). Close to connector

Left Ext.USB Conn. 1

For EMI



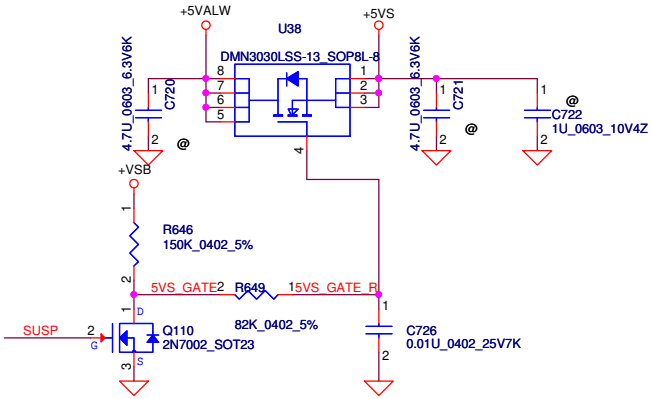
Left Ext.USB Conn. 2



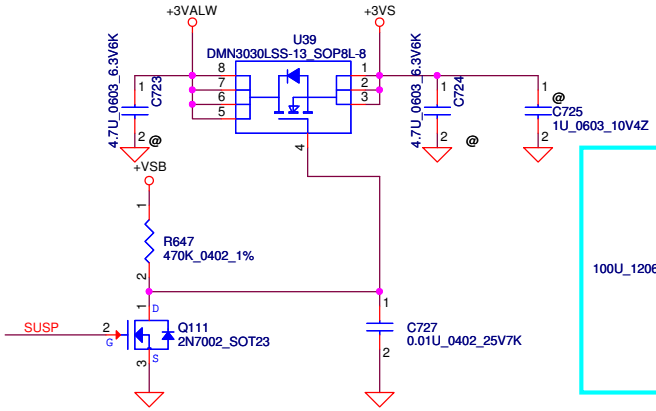
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

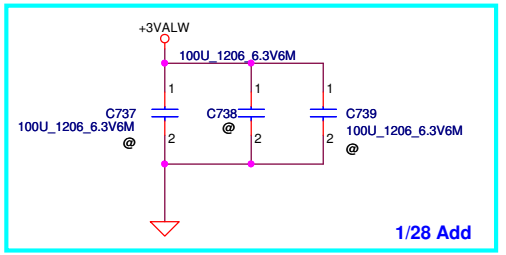
Compal Electronics, Inc.			
Title	USB3.0/Left USB Ports		
Size	Document Number		Rev
B	VILG1/G2 MB LA9901P Schematic		1.0
Date:	Wednesday, March 20, 2013	Sheet	45 of 63

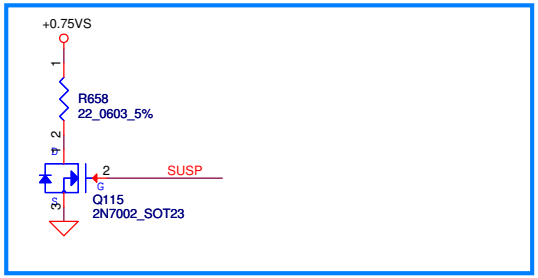
+5VALW to +5VS



+3VALW to +3VS

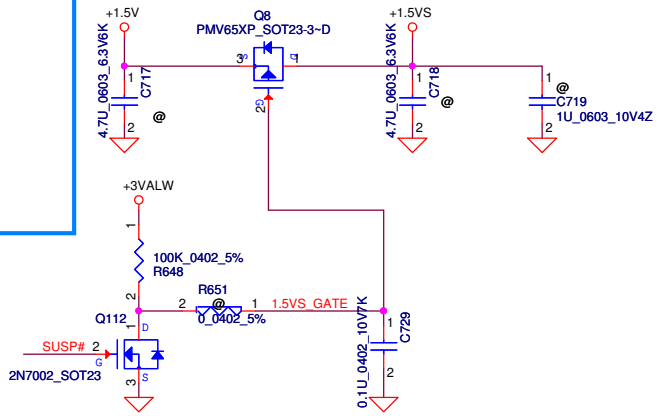


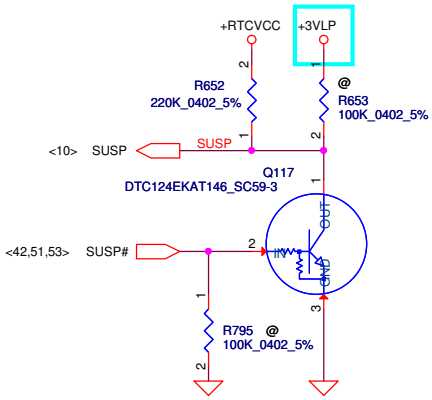




For Intel S3 Power Reduction.

+1.5V to +1.5VS





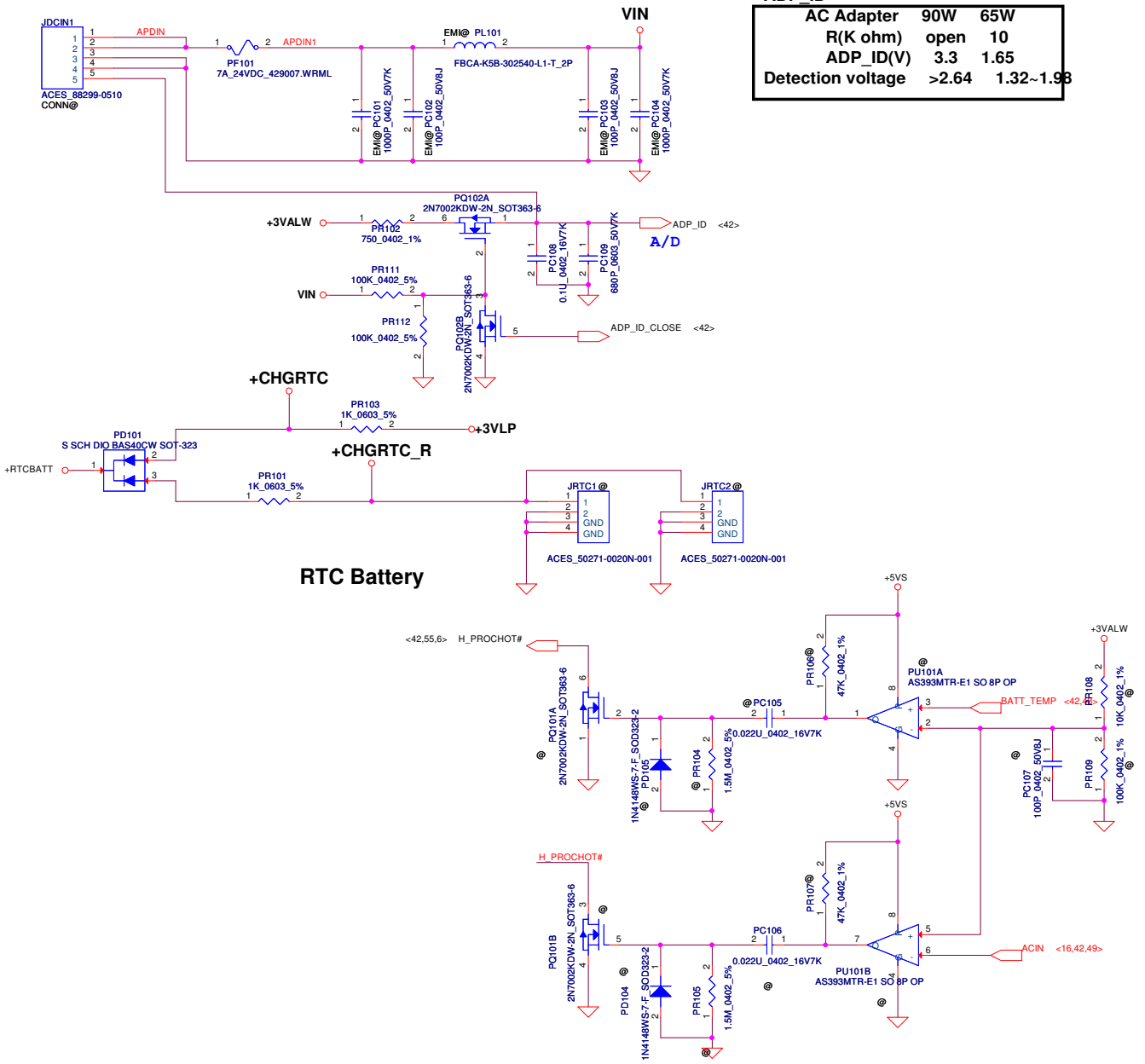
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 46 of 63



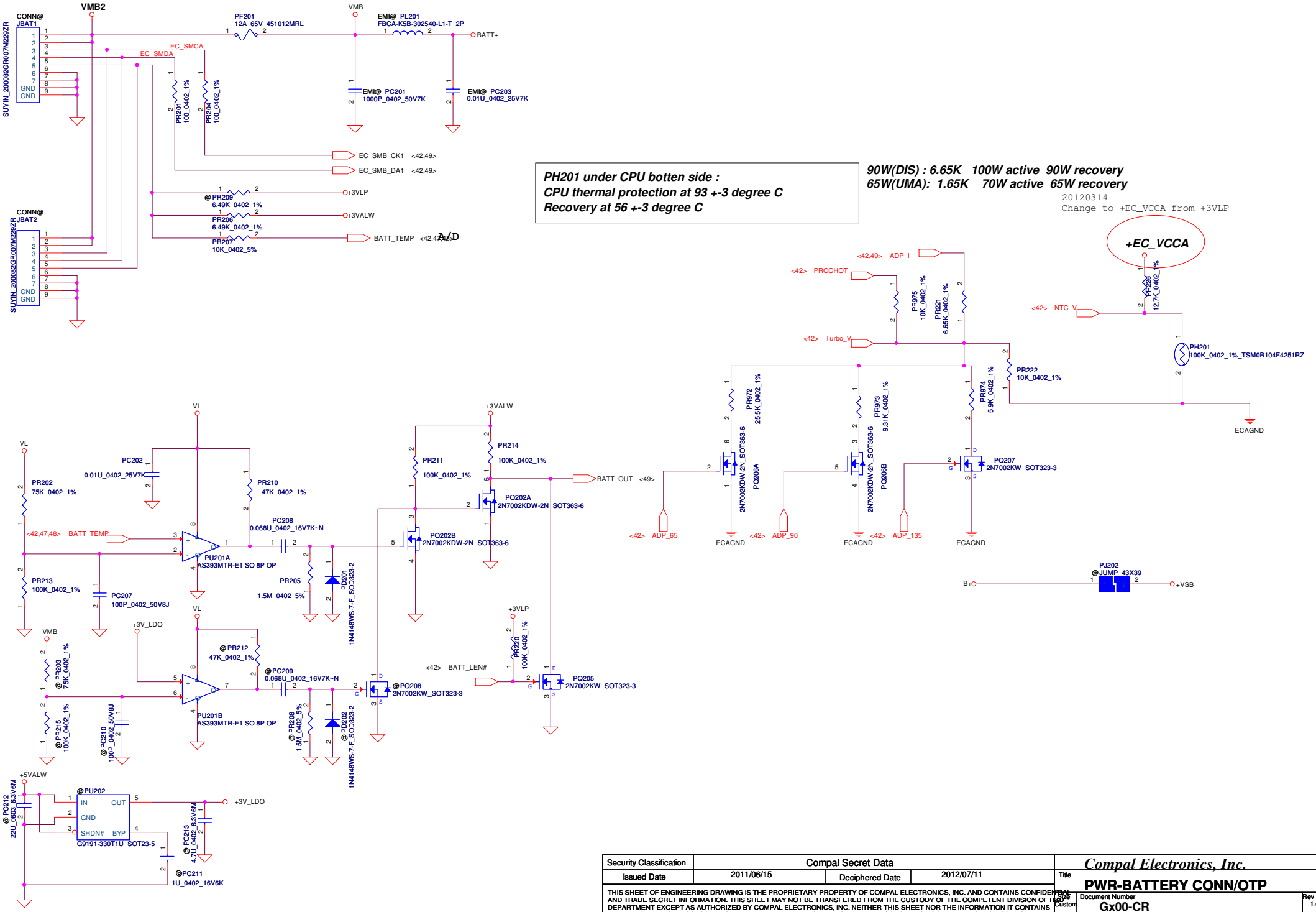
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR DCIN / RTC Battery

Size: Custom | Document Number: Gx00 | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 47 of 63



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

90W(DIS) : 6.65K 100W active 90W recovery
65W(UMA): 1.65K 70W active 65W recovery

20120314
Change to +EC_VCCA from +3VLP

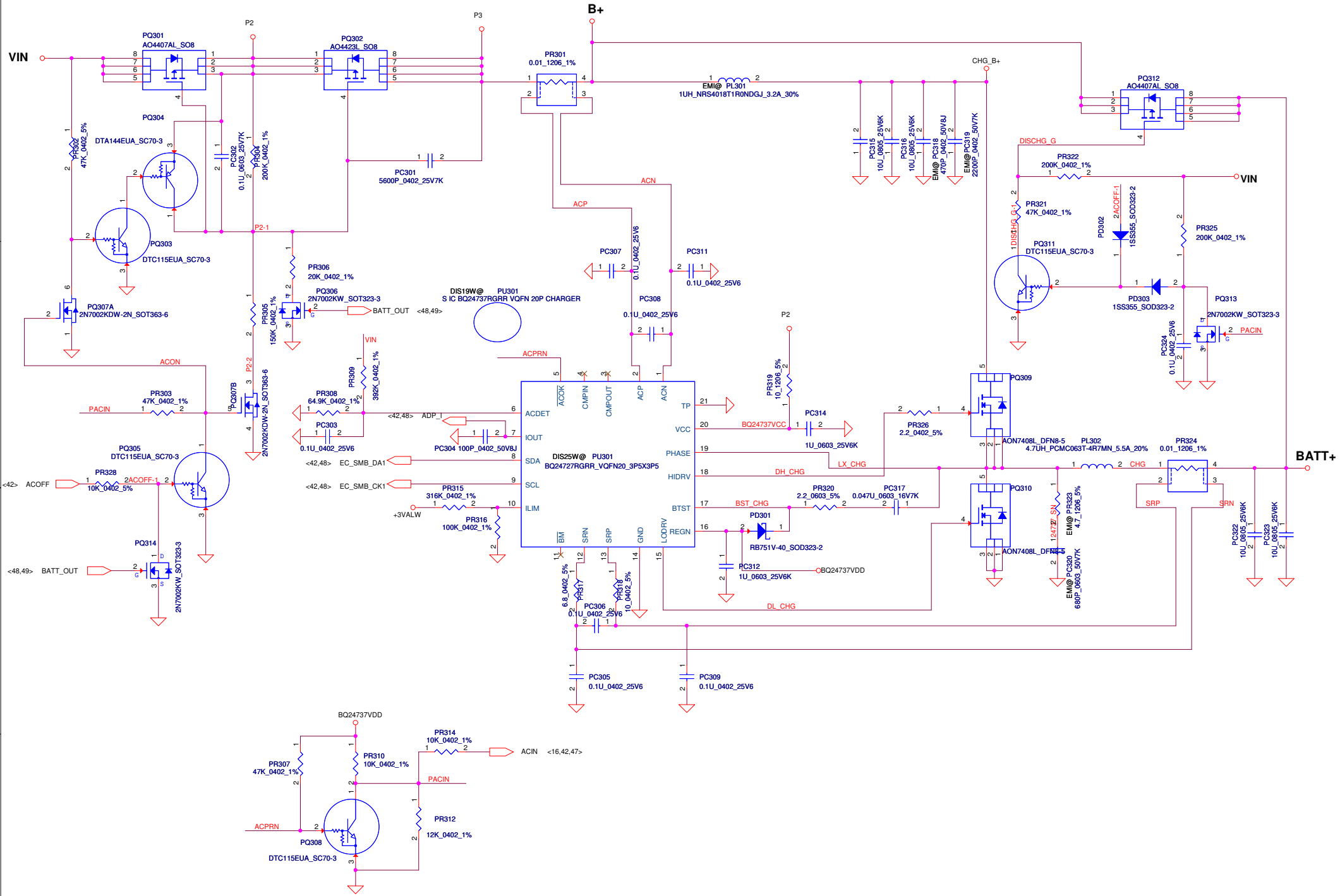
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 48 of 63



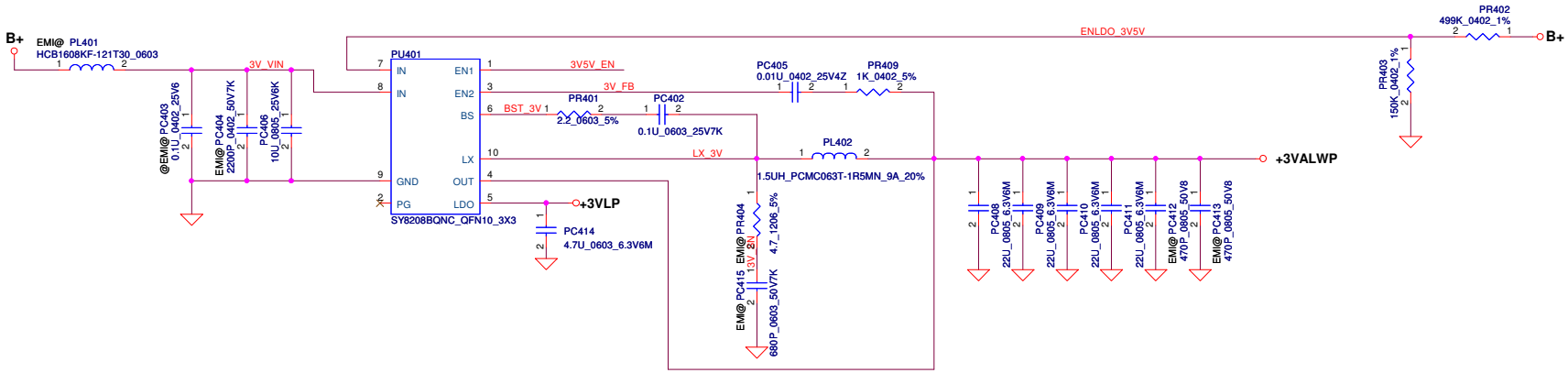
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

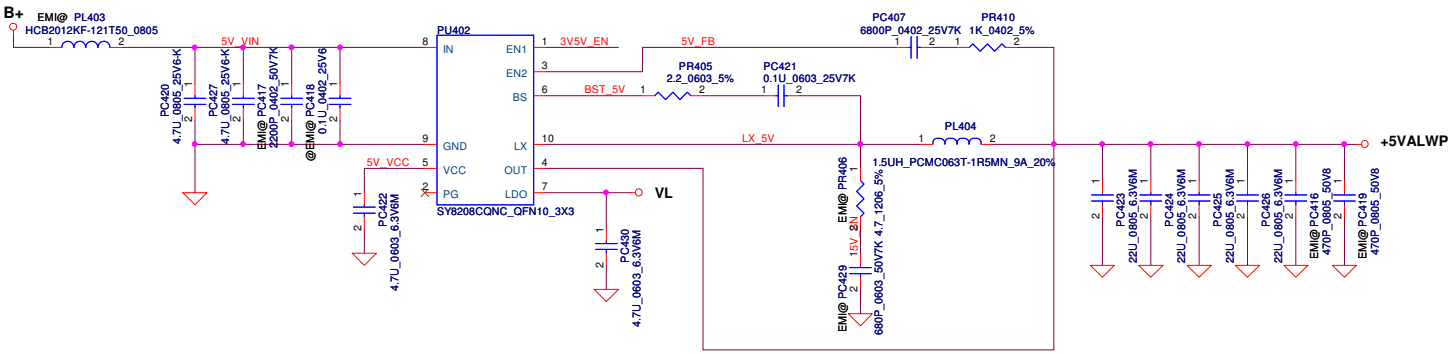
Compal Electronics, Inc.

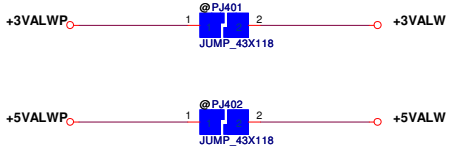
Title: **CHARGER**

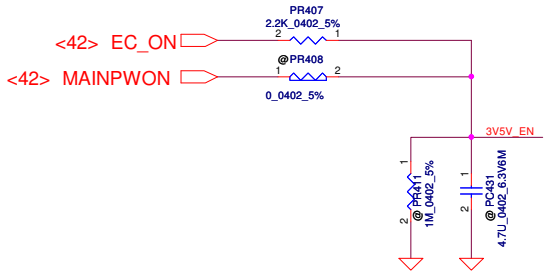
Size	Document Number	Rev
	Gx00-CR	1.0

Date: Wednesday, March 20, 2013 | Sheet 49 of 63









Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

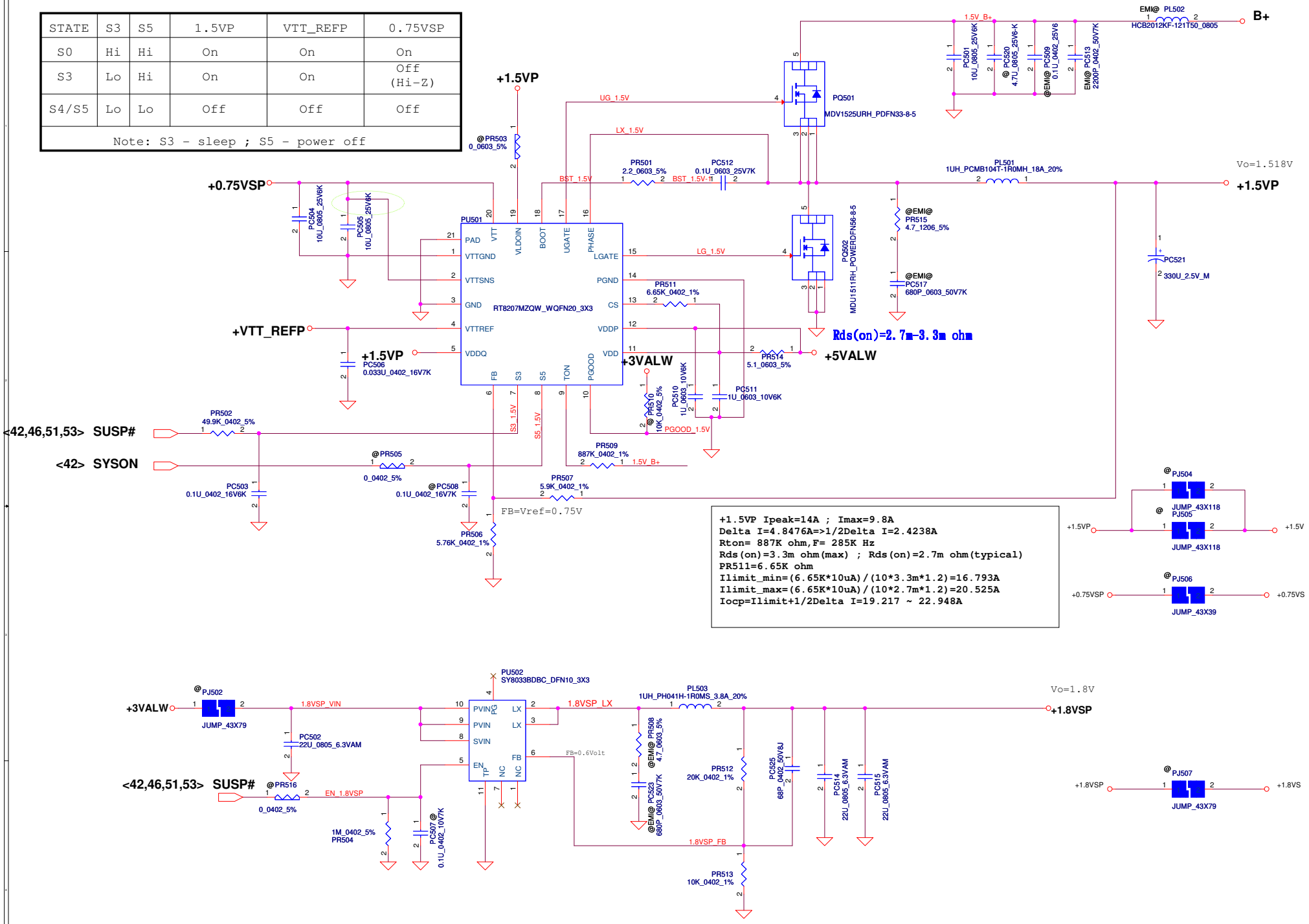
Title: +3VALW/+5VALW

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 50 of 63

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +1.5VP/+1.8VSP

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 51 of 63

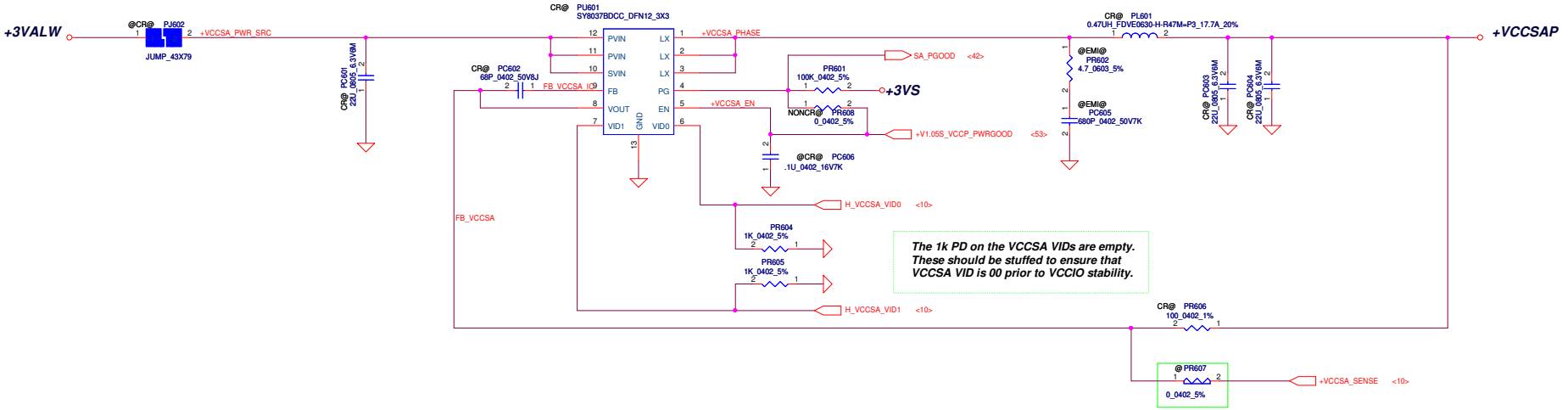
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

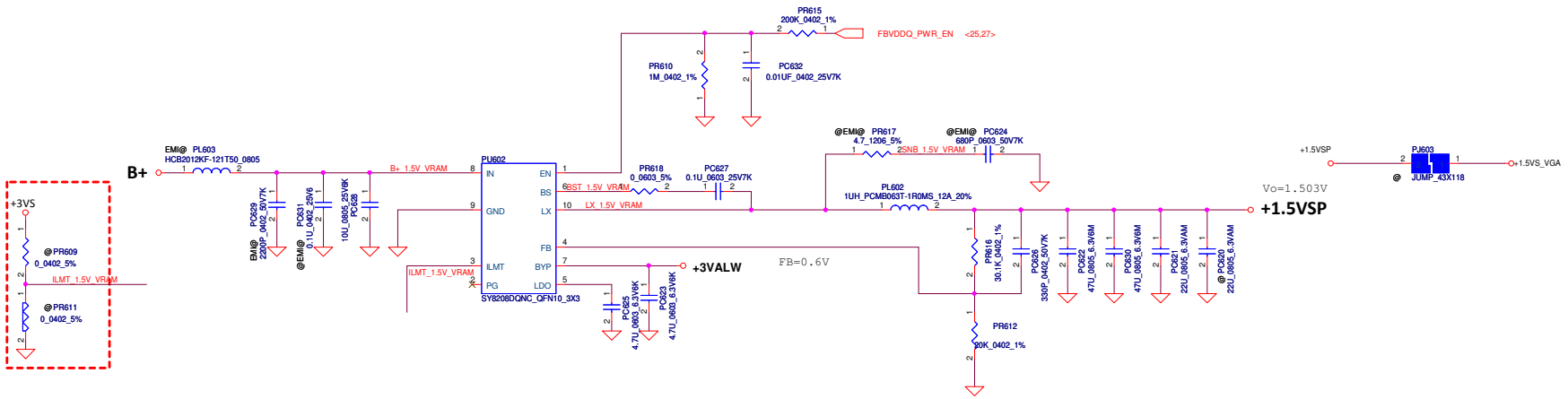
output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
OVP 1.06V

+V1.05S_VCCP — NONCR@ PR603 0.001_1206_1% — +VCCSA

+VCCSAP — @CR@ PJ601 JUMP_43X118 — +VCCSA





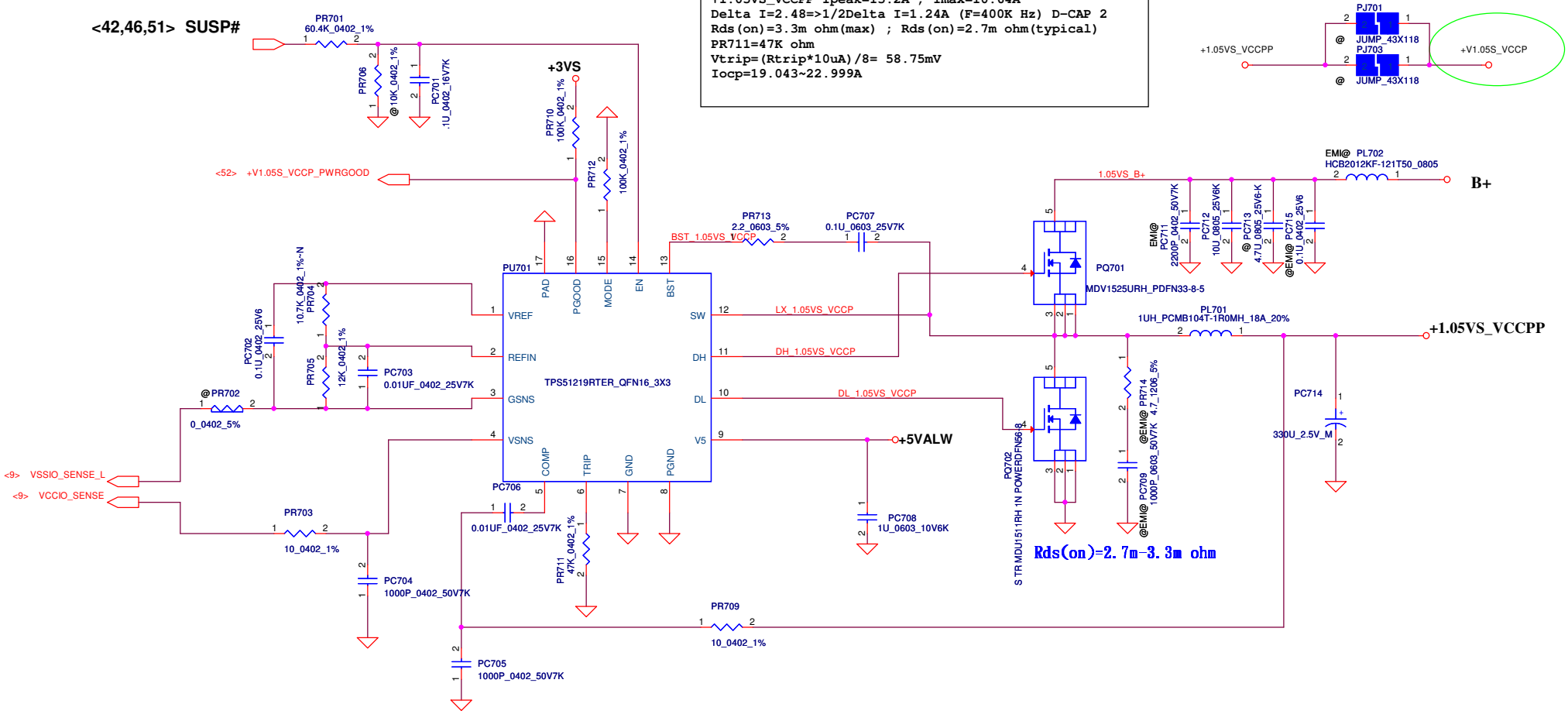
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +VCCSAP/+1.5VSP(VRAM)

Size	Document Number	Rev
C	Gx00-CR	1.0

Date: Wednesday, March 20, 2013 Sheet 52 of 63



Title	+1.05VS_VCCP	
Size: Custom	Document Number	Rev: 1.0
Date: Wednesday, March 20, 2013	Sheet 53 of 63	

	GSGV2(25W)	GE(19W)	
PR842	20	39	(kohm)
PR845	20	30	(kohm)
PR831	2	3	(kohm)
PR816	18	24	(kohm)
PR832	0	3	(kohm)
PC863	2.7	1.8	(nF)

If fix to one phase, PR838 and PR836 must mount.

1phase CCM=>1.2V<PSI<1.8V

PR853=18K ohm,OCP=103A
PR853=15K ohm,OCP=83A
PR853=12K ohm,OCP=63A

PR822=499K ohm,F=300Khz
PR822=360K ohm,F=450Khz

Rds(on)=2.6m-3.1m ohm

Rds(on)=2.6m-3.1m ohm

+VGA_CORE Under VGA Core

+VGA_CORE Near VGA Core

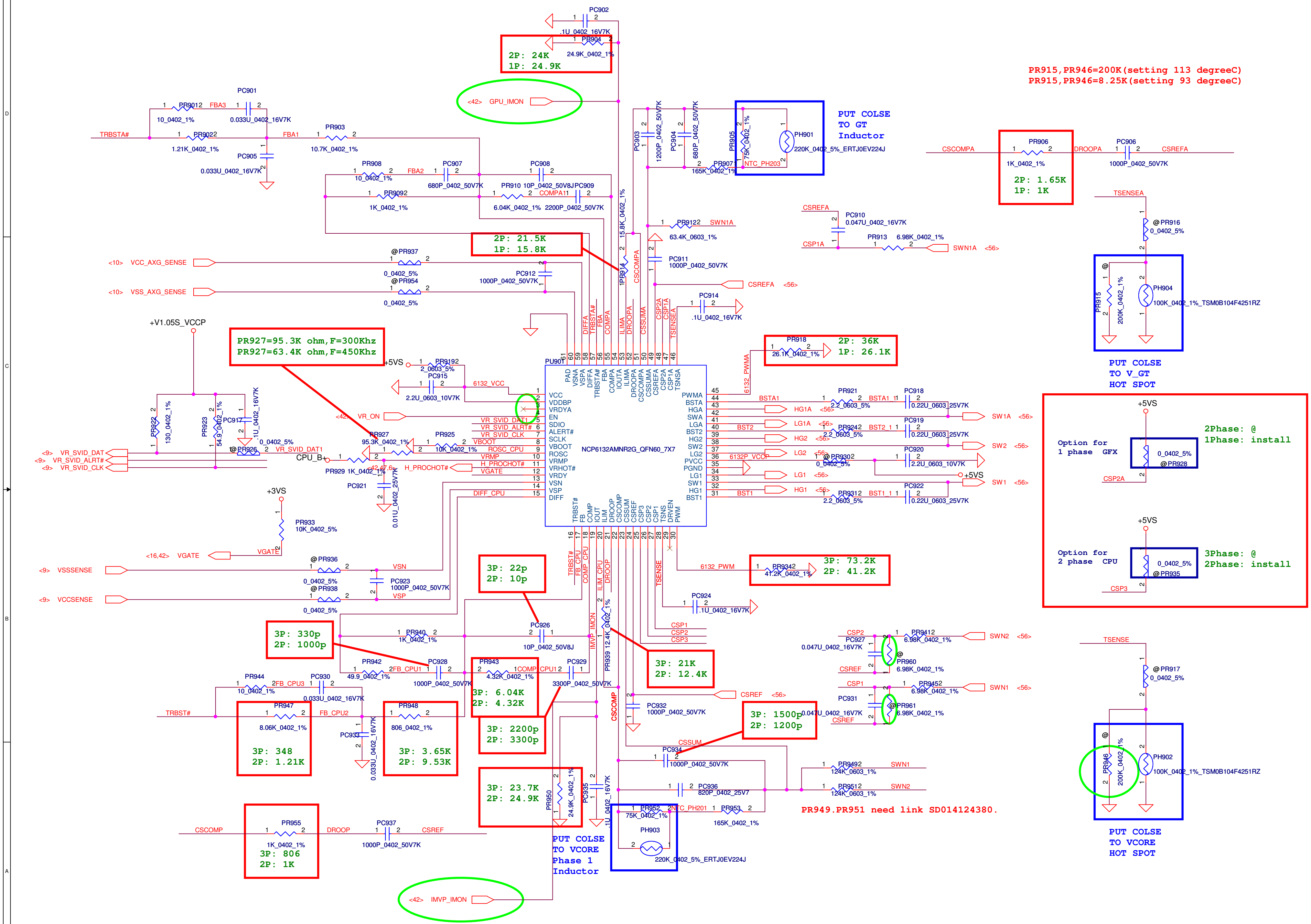
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: VGA_CORE

Size: C | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 54 of 63



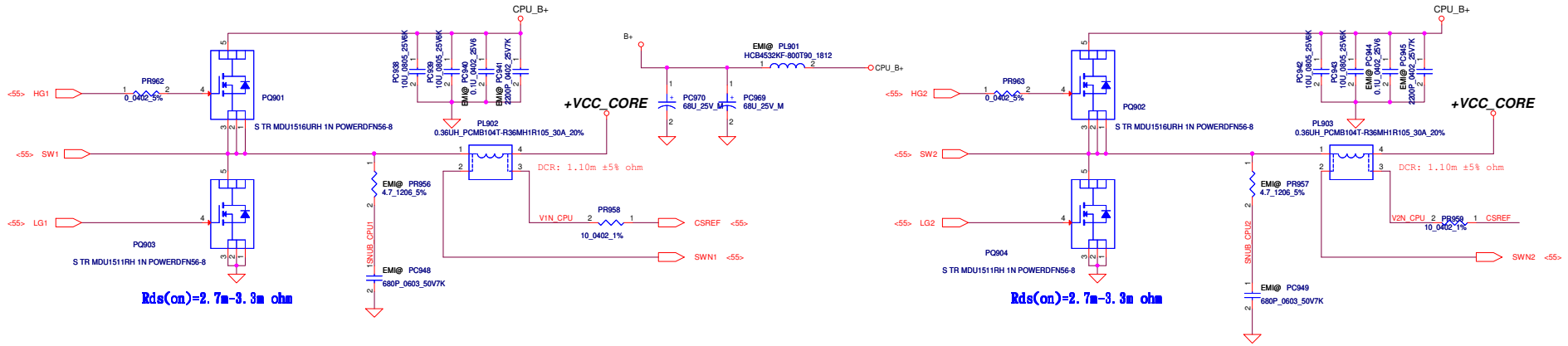
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **PWR-CPU_CORE**

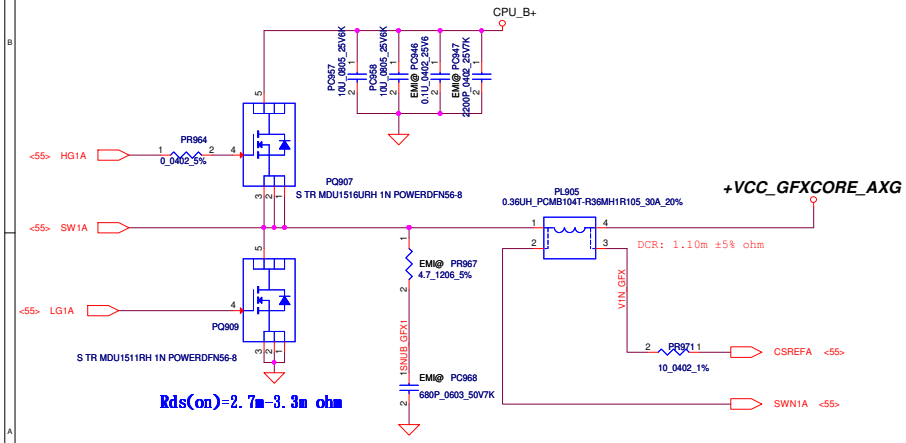
Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 55 of 63



QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

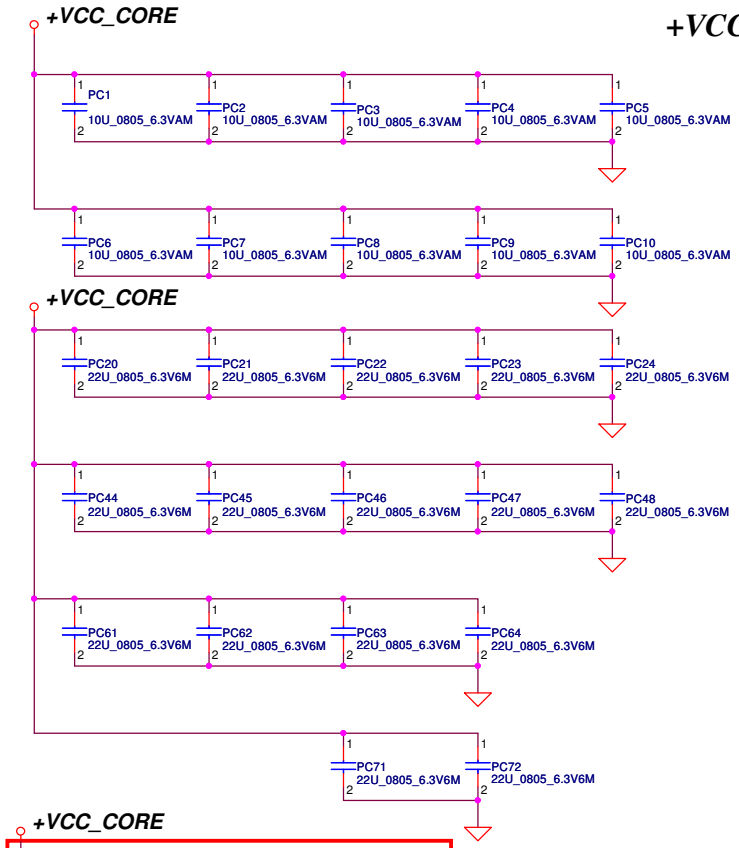
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

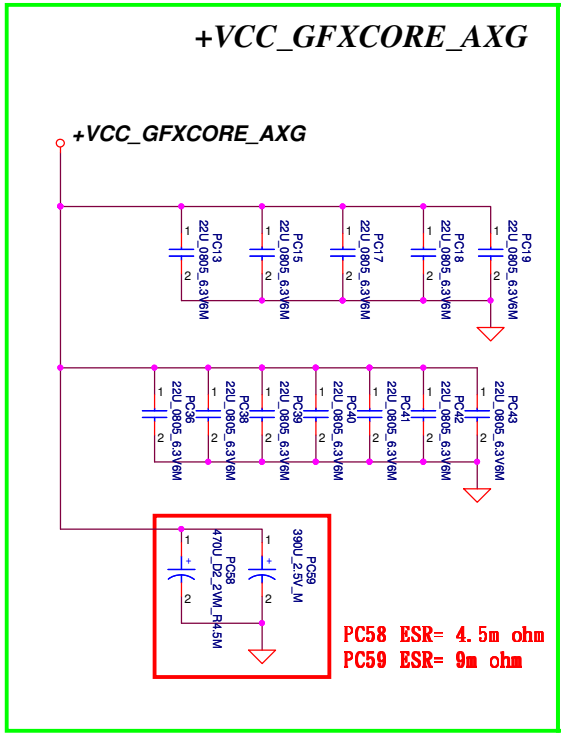
Compal Electronics, Inc.

Title: PWR-CPU_CORE

Size: C | Document Number: Gx00-CR | Rev: 1.0

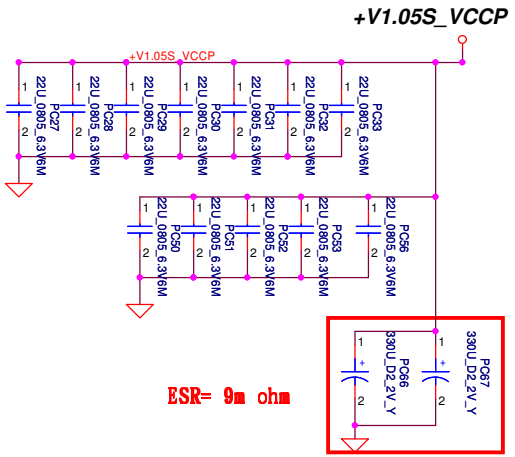
Date: Wednesday, March 20, 2013 | Sheet 56 of 63





Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	LA-9631P	1.0

Date: Wednesday, March 20, 2013 Sheet 57 of 63

Version change list (P.I.R. List)

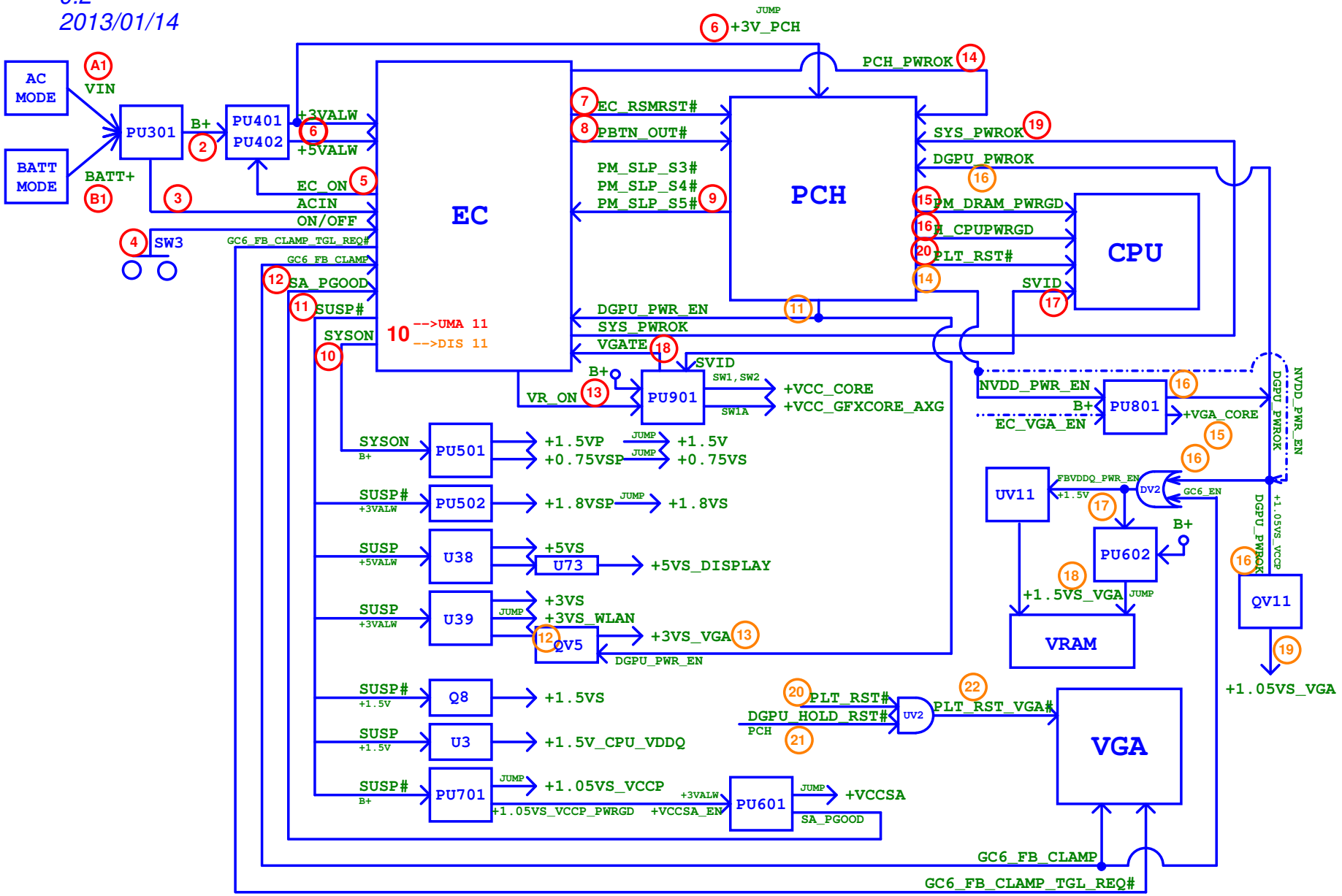
Item	Reason for change	PG#	Modify List	Date	Phase
1	Design Change of IC Package.	50	Change PU401 to SA000061M00(S IC SY8208BQNC QFN 10P PWM)	2012/11/22	DVT
2	Design Change of IC Package.	50	Change PU402 to SA000061N00(S IC SY8208CQNC QFN 10P PWM)	2012/11/22	DVT
3	Design Change of IC Package.	52	Change PU602 to SA000061Q00(S IC SY8208DQNC QFN 10P PWM)	2012/11/22	DVT
4	Add ADP_ID Circuit.	47	Add PQ102 to SB00000EO10(S TR 2N7002KDW 2N SOT-363-6 PANJIT) Add PR111.PR112 to SD028100380(S RES 1/16W 100K +-5% 0402)	2012/12/03	DVT
5	Factory lack of material.	52	Change PC521 to SF000003H00(S_A-P_CAP 330U 2.5V M 6.3X4.2 LESR16M SL)	2012/12/06	DVT
6	Factory lack of material.	56	Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE)	2012/12/06	DVT
7	EMI request adjust +3VALWP/+5VALWP snubber function.	50	Change @PR404.@PC415.@PR406.@PC429 to PR404.PC415.PR406.PC429.	2012/12/06	DVT
8	EMI request adjust +3VALWP/+5VALWP boost resistor.	50	Change PR401.PR405 to SD013220B80(S RES 1/10W 2.2 +-5% 0603).	2012/12/06	DVT
9	EMI request add bypass capacitor.	50	Add PC412.PC413.PC416.PC419 to SE001471J80(S CER CAP 470P 50V J NPO 0805 H0.6)	2012/12/06	DVT
10	EMI request adjust CPU/GFX CORE snubber function.	56	Change @PR956.@PC948.@PR957.@PC949.@PR967.@PC968 to PR956.PC948.PR957.PC949.PR967.PC968.	2012/12/06	DVT
11	EMI request adjust bypass capacitor.	56	Change @PC940 to PC940.	2012/12/06	DVT
12	EMI request add bypass capacitor.	56	Add PC944.PC946 to SE00000G880(S CER CAP 0.1U 25V K X5R 0402) Add PC945.PC947 to SE075222K80(S CER CAP 2200P 25V K X7R 0402)	2012/12/06	DVT
13	Design Change of input capacitor.	50	Change PC420 to SE00000OF80(S CER CAP 4.7U 25V K X6S 0805 H1.25) Add PC427 to SE00000OF80(S CER CAP 4.7U 25V K X6S 0805 H1.25)	2012/12/07	DVT
14	Design Change of IC Application.	50	Add @PR409.@PR410 to SD028100180(S RES 1/16W 1K +-5% 0402) Add @PC405 to SE075472K80(S CER CAP 4700P 25V K X7R 0402) Add @PC407 to SE075472K80(S CER CAP 0.047U 25V K X7R 0402) Add PR411 to SD028000080(S RES 1/16W 0 +-5% 0402)	2012/12/10	DVT
15	Design Change of IC Application.	55	Change PC936 to SE000008980(S CER CAP 820P 25V K X7R 0402) Change PC929 to SE074332K80(S CER CAP 3300P 50V K X7R 0402) Change PC926 to SE071100J80(S CER CAP 10P 50V J NPO 0402) Change PC928 to SE074102K80(S CER CAP 1000P 50V K X7R 0402) Change PR943 to SD00000J280(S RES 1/16W 4.32K +-1% 0402) Change PR949.PR951 to SD014124380(S RES 1/10W 124K +-1% 0603 YAGEO)	2012/12/17	DVT
16	Design Change of CPU/GFX CORE Choke.	56	Change PL902.PL903.PL905 to SH00000NM00(S COIL 0.22UH +-20% PCMB104T-R22MS 35A)	2012/12/21	DVT
17	Design Change of VGA CORE(Standby mode Circuit).	54	Delete PC864.PQ810.PR802.PR803.PR805	2012/12/21	DVT
18	Reduction Part Count.	47	Delete PR110.	2013/01/18	PVT
19	Reduction Part Count.	52	Delete PR603.	2013/01/18	PVT
20	Reduction Part Count.	54	Delete PR814.PC849.PR825.PR835.PR850.PD802.PD801.	2013/01/18	PVT

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
21	Reduction Part Count.	55	Delete PC916.	2013/01/18	PVT
22	Design Change of IC Application.	50	Change @PC405.@PR490.@PC407.@PR410 to PC405.PR490.PC407.PR410. Change PR411 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
23	Reduction Part Count.	51	Change PR505.PR516 to SD028000080(S RES 1/16W 0 +-5% 0402) Change PR503 to SD013000080(S RES 1/10W 0 +-5% 0603)	2013/01/18	PVT
24	Design Change of Thermal Application.	51	Change PC521 to SGA20331E10(S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	2013/01/18	PVT
25	Reduction Part Count.	52	Change PR611 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
26	Reduction Part Count.	53	Change PR702 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
27	Reduction Part Count.	54	Change PR823.PR824 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
28	Reduction Part Count.	55	Change PR926.PR916.PR917 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
29	Design Change of CPU/GFX CORE Choke.	56	Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE)	2013/01/18	PVT
30	Design Change of CPU/GFX CORE Frequence.	55	Change PR927 to SD034953280(S RES 1/16W 95.3K +-1% 0402)	2013/01/18	PVT
31	Factory lack of material.	50	Change PC420.PC427 to SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25)	2013/01/18	PVT
32	Reduction Part Count.	50	Delete PR411.	2013/01/21	PVT
33	Design Change of Power Circuit Application.	48	Change PC208 to SE000003J80(S CER CAP 0.068U 16V K X7R 0402)	2013/01/23	PVT
34	Design Change of Power Circuit Application.	49	Add PR328 to SD028100280(S RES 1/16W 0 +-5% 0402) Add PR327 to SD028000080(S RES 1/16W 0 +-5% 0402) Add PQ314 to SB000009Q80(S TR 2N7002KW 1N SOT323-3)	2013/01/23	PVT
35	Design Change of Power Circuit Application.	50	Change PC405 to SE072103Z80(S CER CAP .01U 25V Z Y5V 0402) Change PC407 to SE075682K80(S CER CAP 6800P 25V K X7R 0402)	2013/03/04	PVT

COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-9901P*
REVISION: *0.2*
DATE: *2013/01/14*



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: *Power sequence*

Size: Custom | Document Number: *VILG1/G2 MB LA-9901P Schematic* | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 60 of 63

VILG1/G2 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			EVT TO DVT
1	P.5~11	Change footprint of JCPU1	For Lenovo rule
2	P.14	Add R406, R407, R408, R409	Reserve for improvement factory processes
3	P.42	Add EC_SPI_SO, EC_SPI_SI, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes
4	P.42	Add PCH_PWR_EN to EC Pin.107	Reserve for improvement factory processes
5	P.42	Reserve R410	Reserve Pull-high for GPIO use
6	P.42	Change EC_FAN_PWM from EC Pin.34 to EC Pin.26	For common design
7	P.42	Change NOVO# from EC Pin.26 to EC Pin.34	For common design
8	P.42	Change ENBKL from EC Pin.73 to EC Pin.76	For common design
9	P.42	Change IMVP_IMON from EC Pin.76 to EC Pin.73	For common design
10	P.42	Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123	For common design
11	P.42	Change OVERT#_R from EC Pin.117 to EC Pin.17	For common design
12	P.34	Add R411, R412, C411, C412	Reserve for EMI
13	P.20	Add Q21, R40, C237, Q22,R418, C243,C252,R413	Reserve for power consumption
14	P.25	Change RV41 to 1K ohm, CV63 to 1uF	For VGA Sequence
15	P.25	Add QV4/RV42	For VGA Sequence
16	P.25	Change QV3/UV11	For VGA Sequence
17	P.26	Change RV241 to 15K ohm	For VGA Sequence
18	P.26	Add QV6 and RV44.	For VGA Sequence
19	P.26	Change QV10/QV11	For VGA Sequence
20	P.43	Del Q12/R806	For Change Audio Jack type from Normal close to Normal open

Compal Electronics, Inc.

Title: HW-PIR1

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 61 of 63

VILG1/G2 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			DVT TO PVT
1	P.36	Reserve R508	For leakage current issue of Atheros WLAN
2	P.41	Change RA22 to reserve	For PC Beep issue(can't heard sound of "di" on BIOS setup menu)
3	P.41	Reserve RA10/RA11	For solve Codec speaker Hum noise issue(Zizi)
4	P.42	Reserve R416	Reserve +3VLP power rail to EC
5	P.42	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC
6	P.42	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC	Using power rail which the same with EC
7	P.14	Change U5 from 4MB to 8MB ROM	Follow common design
			PVT TO Pre-MP
1	P.23	Change RV5 to shortpad	
2	P.42	Chagne R416 to shortpad	
3	P.52	Reserve +1.05S_VCCP_PWRGOOD of +V1.05S_VCCP to connect to SA_PGOOD	For Celeron/Pentium CPU

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.		
Title: HW-PIR2		
Size: Custom	Document Number: VILG1/G2 MB LA9901P Schematic	Rev: 1.0
Date: Wednesday, March 20, 2013	Sheet 62 of 63	

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
44					
45					
46					
47					
48					
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53					

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