E440

NM-A151 Rev1.0 Schematic

Intel Haswell Processor with DDRIII + Lynx point PCH
nVIDIA N14P-GV2/ N14M-GL

2013-07-11 Rev 1.0

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Title: Cover Page

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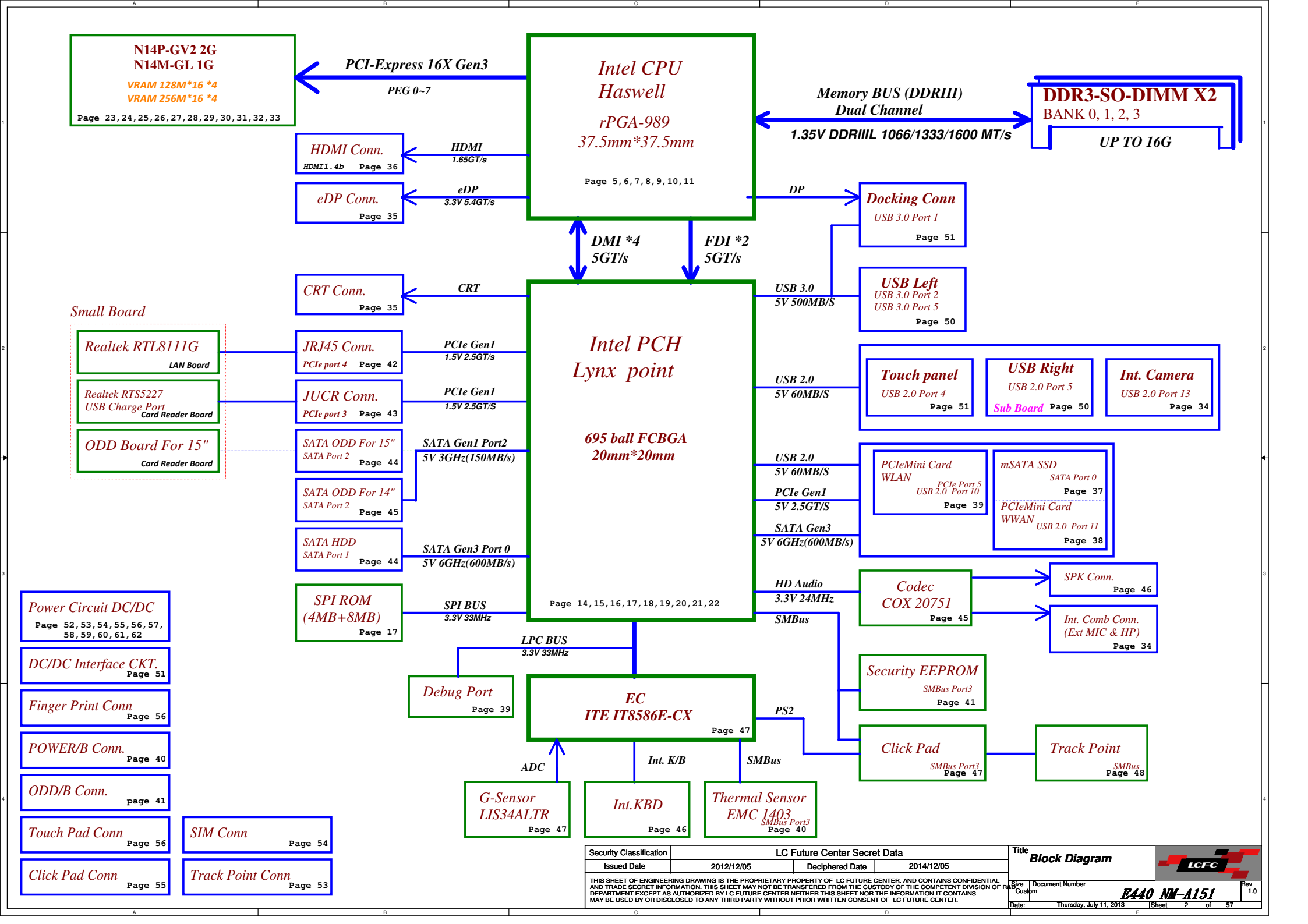

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Title: **Block Diagram**

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW / +5VALW	+1.5V	+5VS / +3VS / +1.5VS / +VCCSA / +V1.5S_VCCP / +CPU_CORE / +VGA_CORE / +GFX_CORE / +1.8VS / +1.05VS / +0.75VS / +3.3VS_VGA / +1.5VS_VGA / +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
EHCI1	XHCI 1	0	Camera
	2	1	USB Port (Right Side)
		2	USB Port (Left Side)
	3	3	
	4	4	
		5	USB Port (Right Side)
		6	
		7	
EHCI2		8	
		9	
		10	Mini Card(WLAN)
		11	
		12	
		13	Blue Tooth

BOM Structure Table

BOM Structure	BTO Item
HDMI@	HDMI part
CHG@	USB charger part
NOCHG@	No USB charger part
CMOS@	CMOS camera support part
8171@	QCA8171 LAN part
8171S@	QCA8171 LAN surge part
SURGE@	QCA8171&8172 LAN surge part
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
SLI@	For SLI function part
DS3@	Deep S3 support part
S3@	For S3 function part
GT@	NV chip part
@	Unpop
EDP@	Support EDP panel function
daul@	Support daul channel panel function

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
PM_SMBCLK PM_SMBDATA	PCH +3V_PCH	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	Card Reader
5	
6	
7	
8	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

ZZZ1

DA80000TV00

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Title: Notes List

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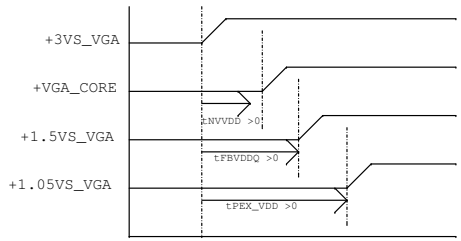
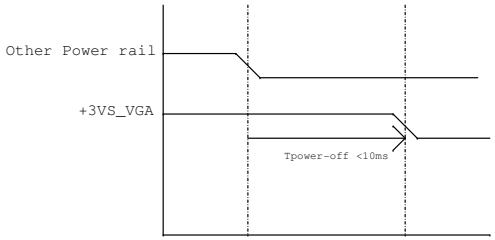
Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	_	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	_	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	_	HPD_IRQ



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GT (28nm)	0x0FDB

	setting	I2C Slave addrees ID
SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
	1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU		N13P-GT		
FB Memory (GDDR5)		ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K		

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Title: VGA Notes List

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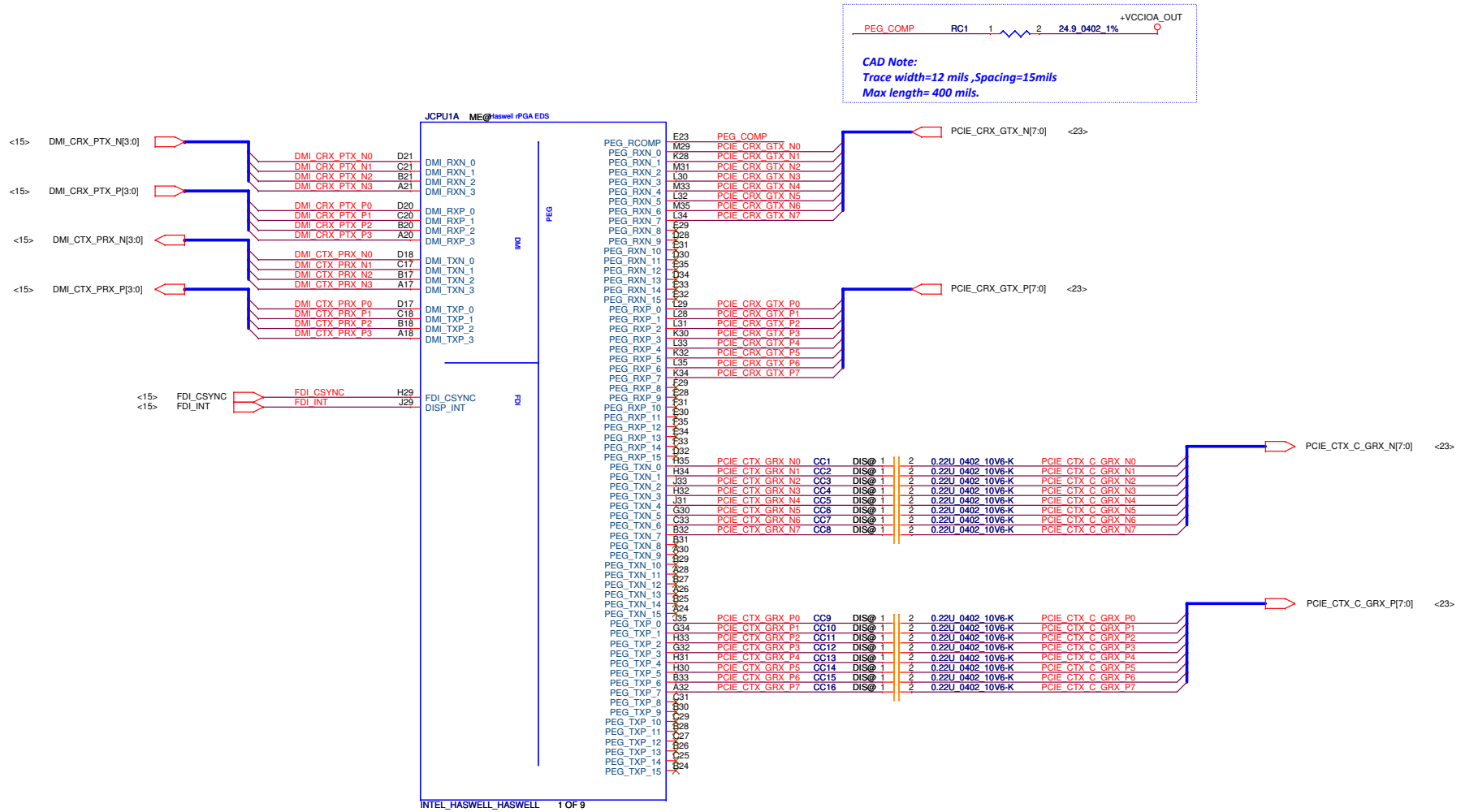

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Title: CPU_DMI/PEG/FDI

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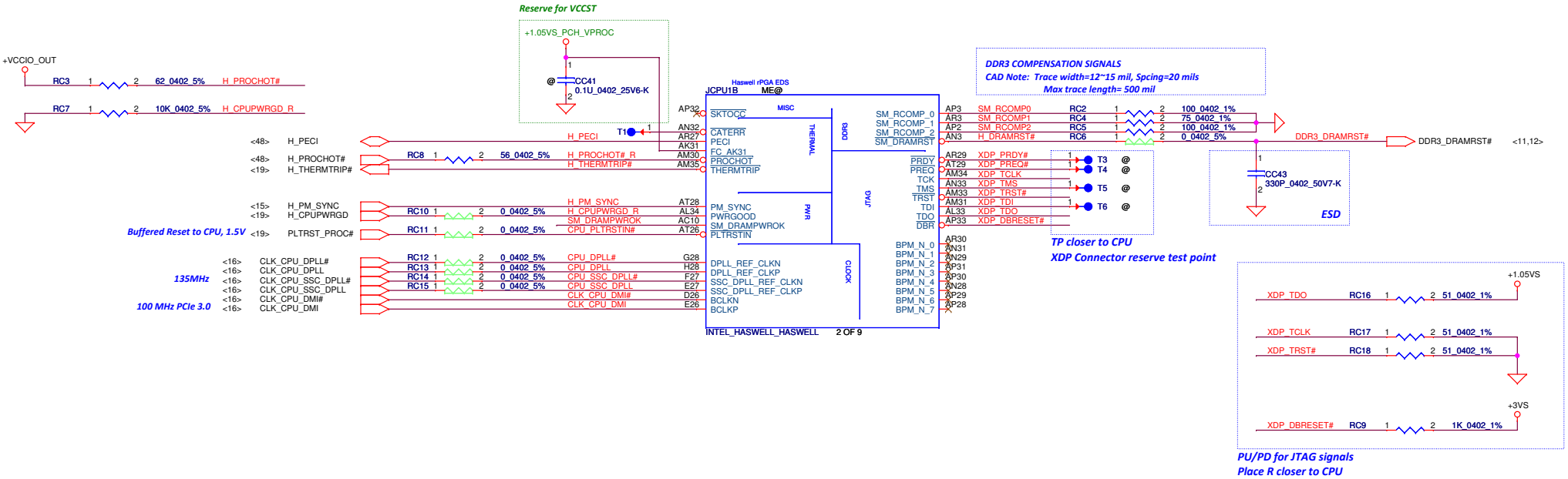
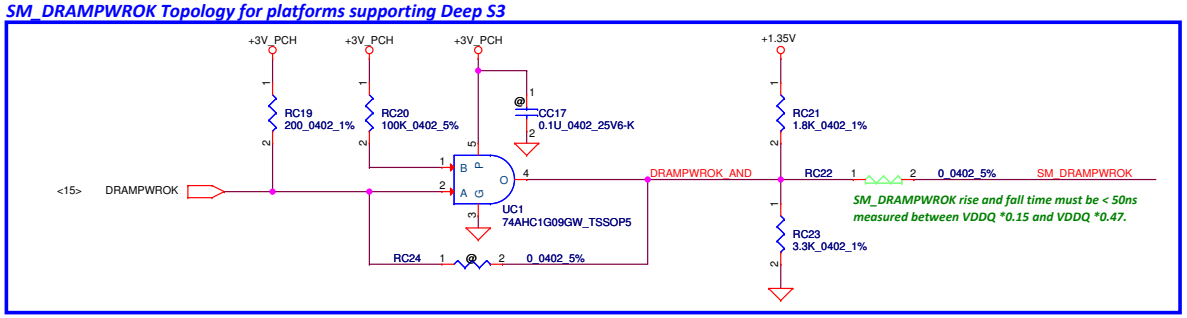
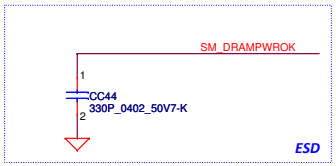


SM_DRAMPWROK Topology for platforms supporting Deep S3



Close to JCPU. AC10



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Title: CPU_JTAG/XDP/CLK

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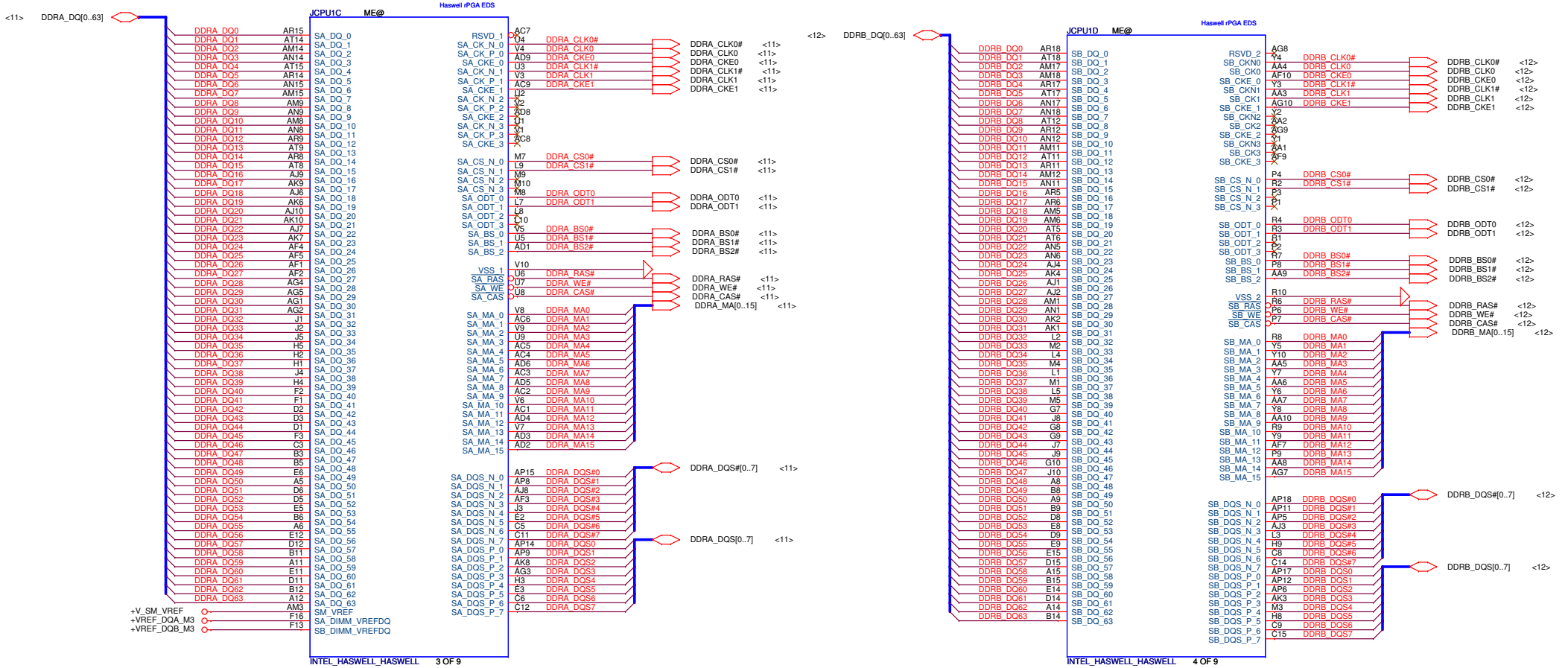

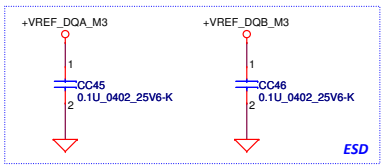

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Title: CPU_DDR3 INTERFACE

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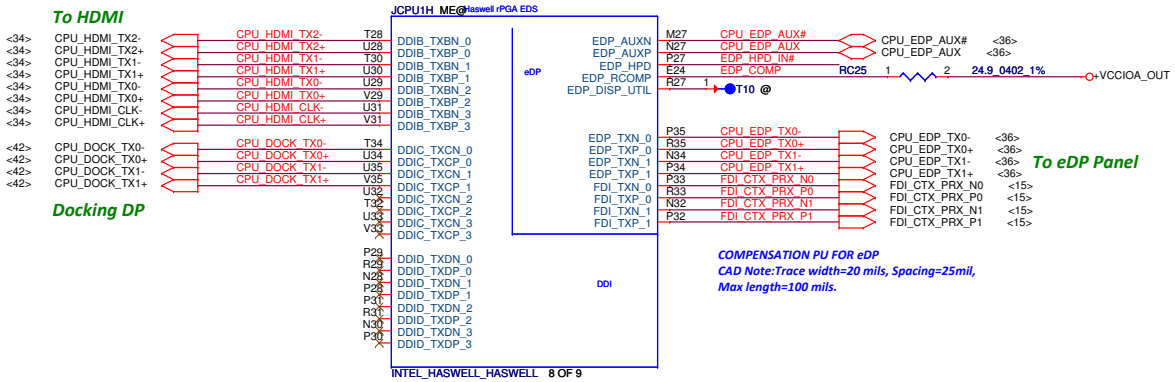

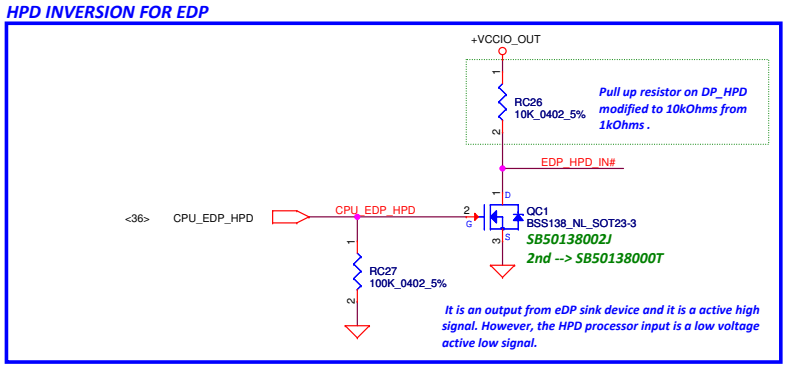

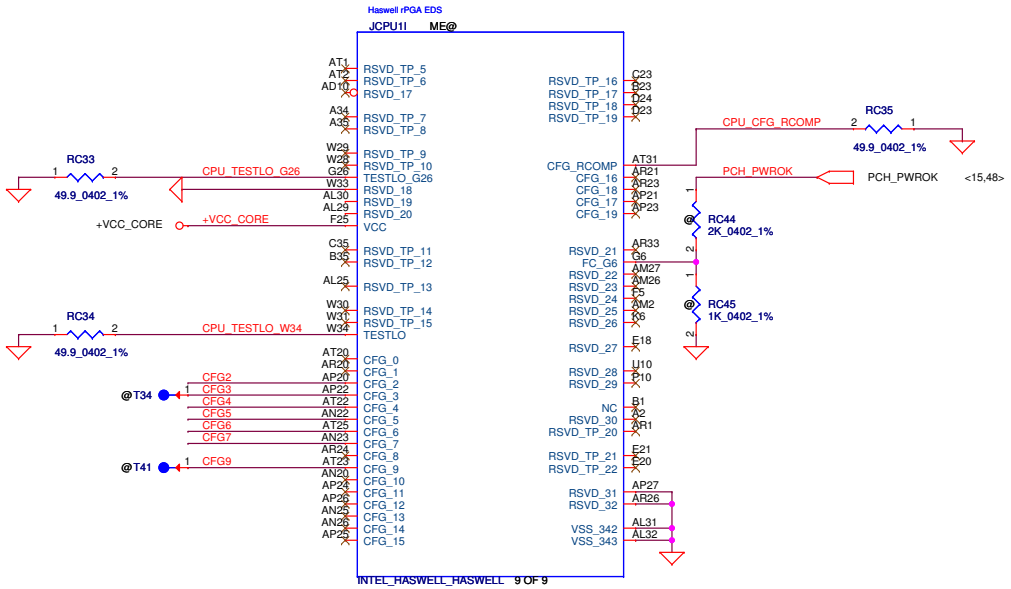

CFG STRAPS For CPU
(CFG[17:0] internal pull high 5 ~15K to VCCIO)

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: (Default) Normal Operation; Lane# definition matches socket pin map definition 0: Lane Reversed

CFG2 RC28 1 @ 2 1K_0402_1%

Display Port Presence Strap	
CFG4	1 : Disabled No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4 RC29 1 @ 2 1K_0402_1%

PCIE Port Bifurcation Straps	
CFG[6:5]	11 : Func 1 Disabled, Func 2 Disabled (x16,---,---) * 10 : Func 1 Enabled, Func 2 Disabled (x8,x8,---) 01 : Func 1 Disabled, Func 2 Enabled 00 : Func 1 Enabled, Func 2 Enabled (x8,x4,x4)

CFG5 RC30 1 @ 2 1K_0402_1%
CFG6 RC31 1 @ 2 1K_0402_1%

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train Immediately Following XXRESETB Deassertion 0 : PEG Wait for BIOS for Training

CFG7 RC32 1 @ 2 1K_0402_1%

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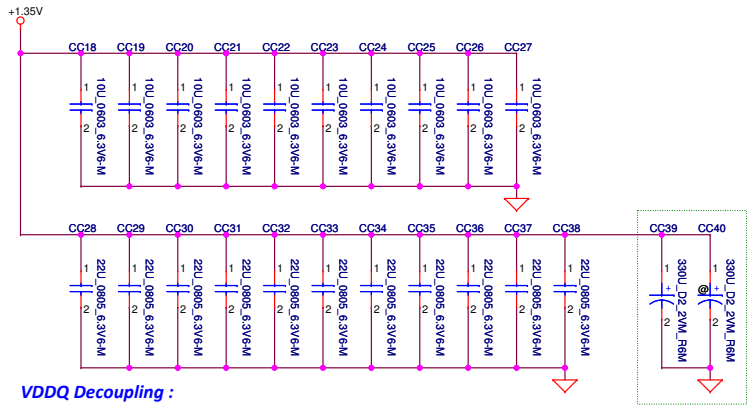
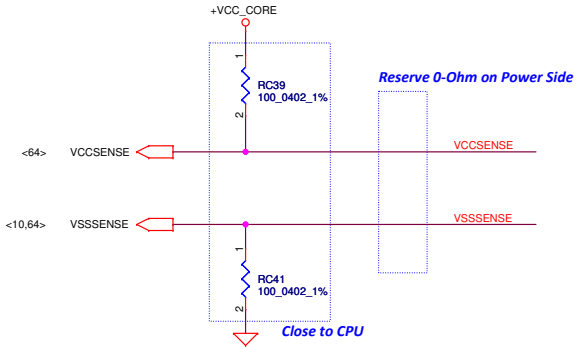
CPU VDDQ DECOUPLING

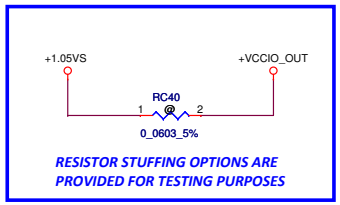


VDDQ Decoupling :

1. *MB Bottom Socket Edge --> 2* 330uf, 6mΩ*
2. *6x MB Bottom Socket Cavity --> 11* 22 µF (0805), 3mΩ*
   5x MB Top Socket Cavity
3. *5x MB Bottom Socket Cavity --> 10 x 10 µF (0805), 3mΩ*
   5x MB Top Socket Cavity

VCC/VSS SENSE





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Title: CPU_POWER

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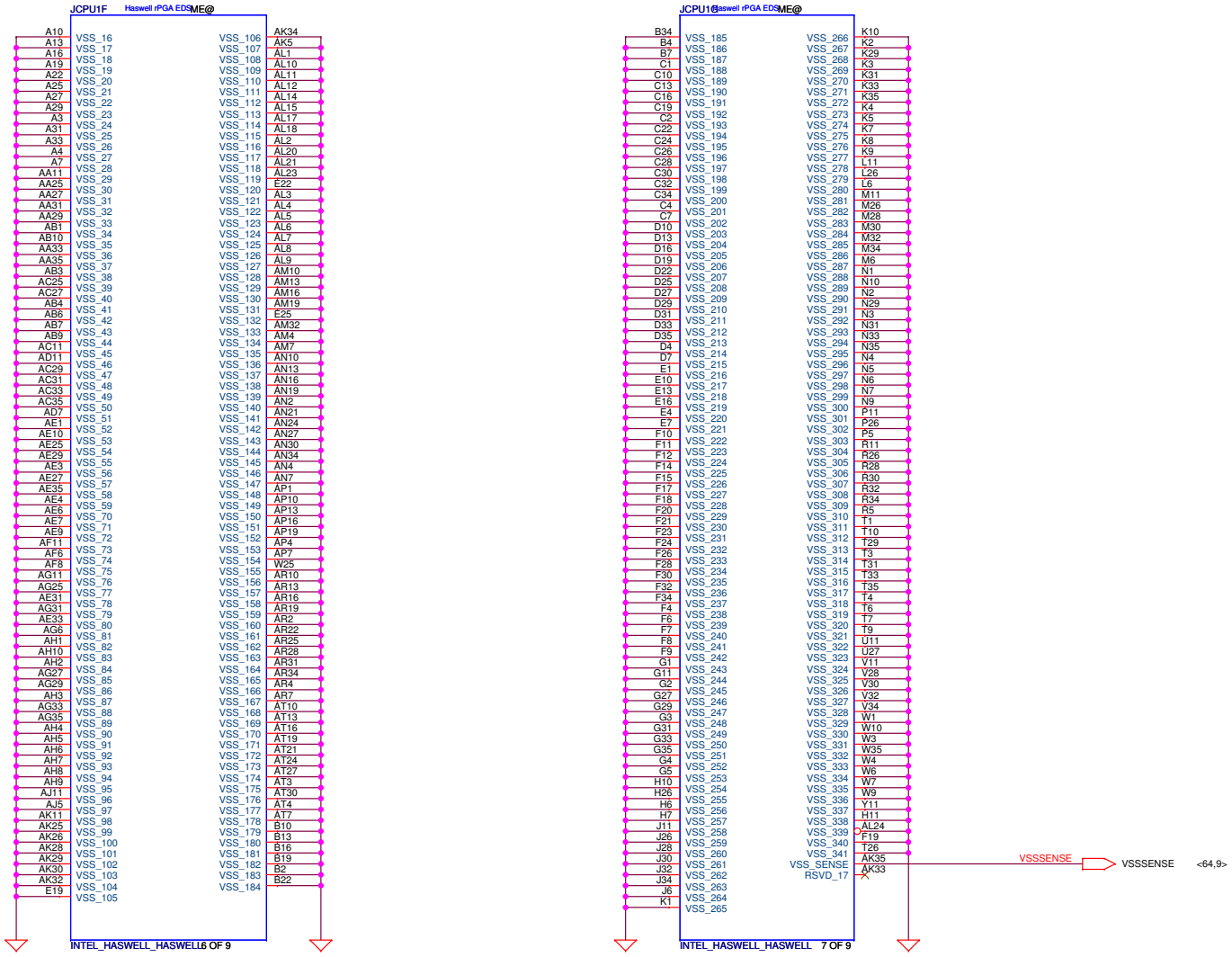

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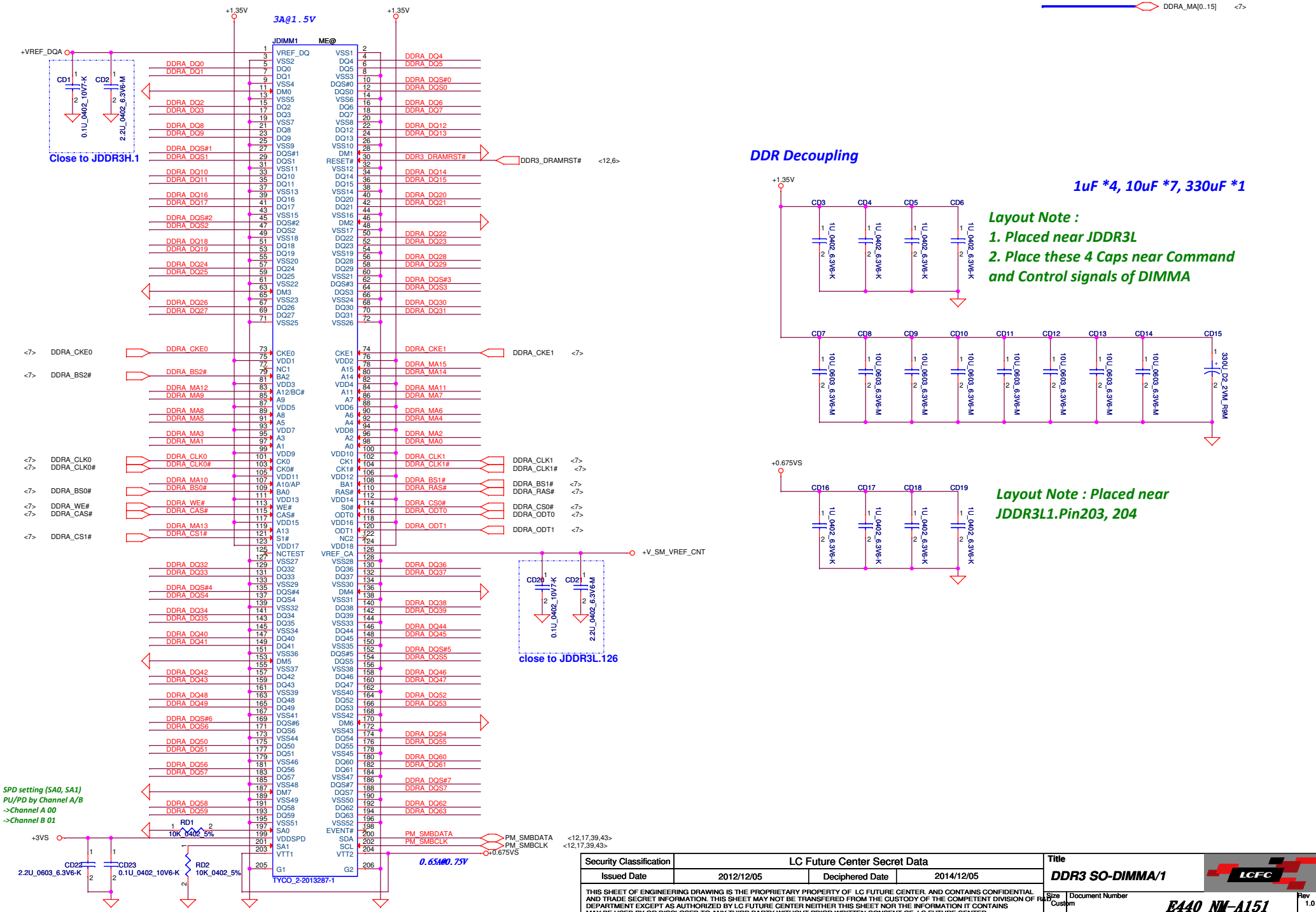
DDR3 SO-DIMM A



DDR Decoupling

1uF *4, 10uF *7, 330uF *1

Layout Note :
1. Placed near JDDR3L
2. Place these 4 Caps near Command and Control signals of DIMMA

Layout Note : Placed near JDDR3L1.Pin203, 204

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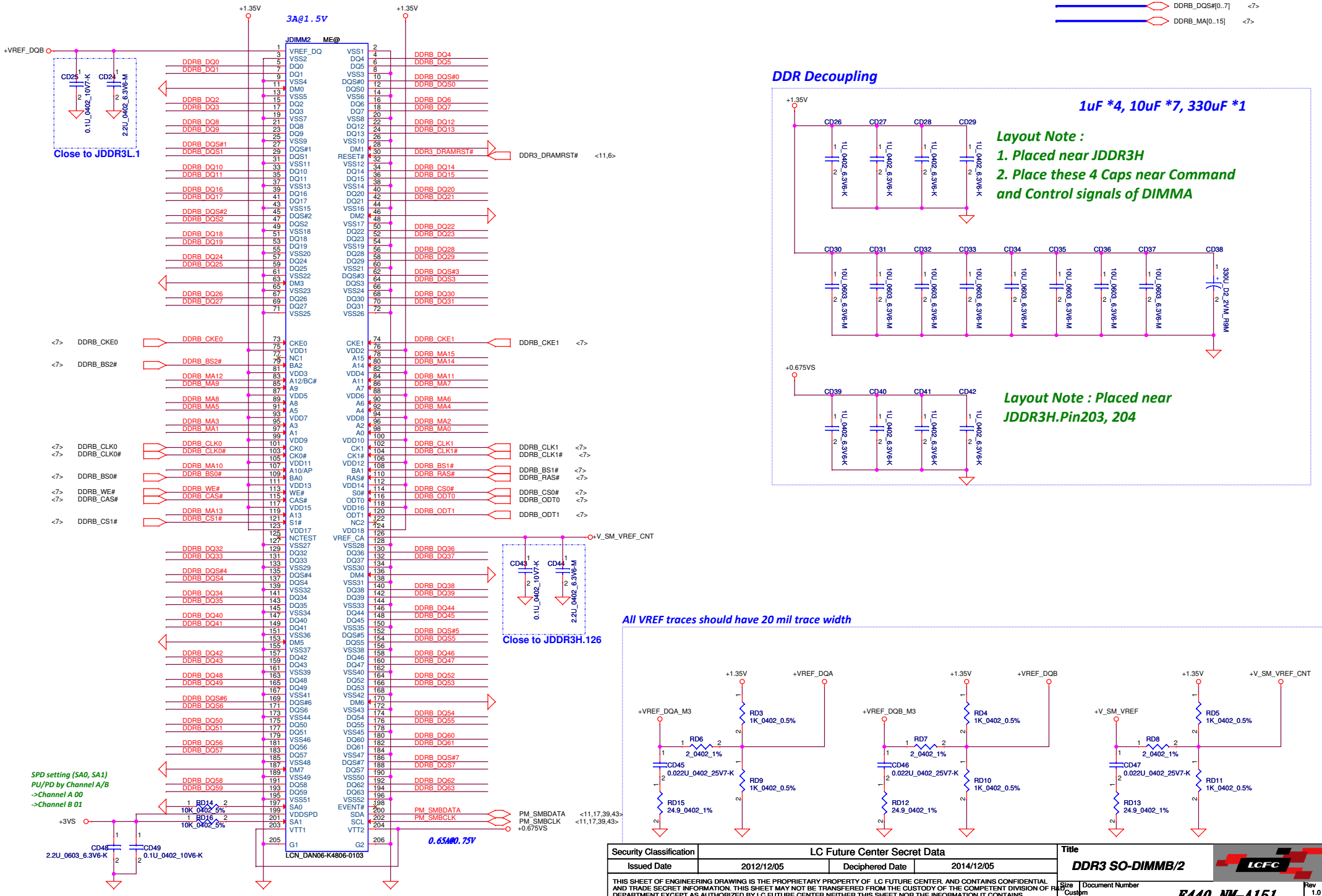
DDR3 SO-DIMM B



DDR Decoupling

All VREF traces should have 20 mil trace width

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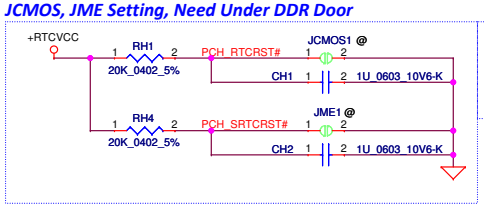
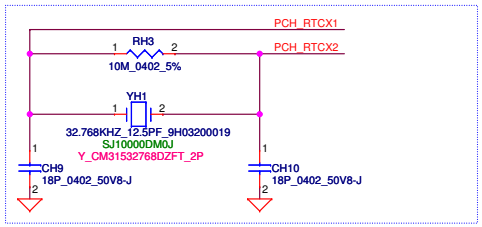
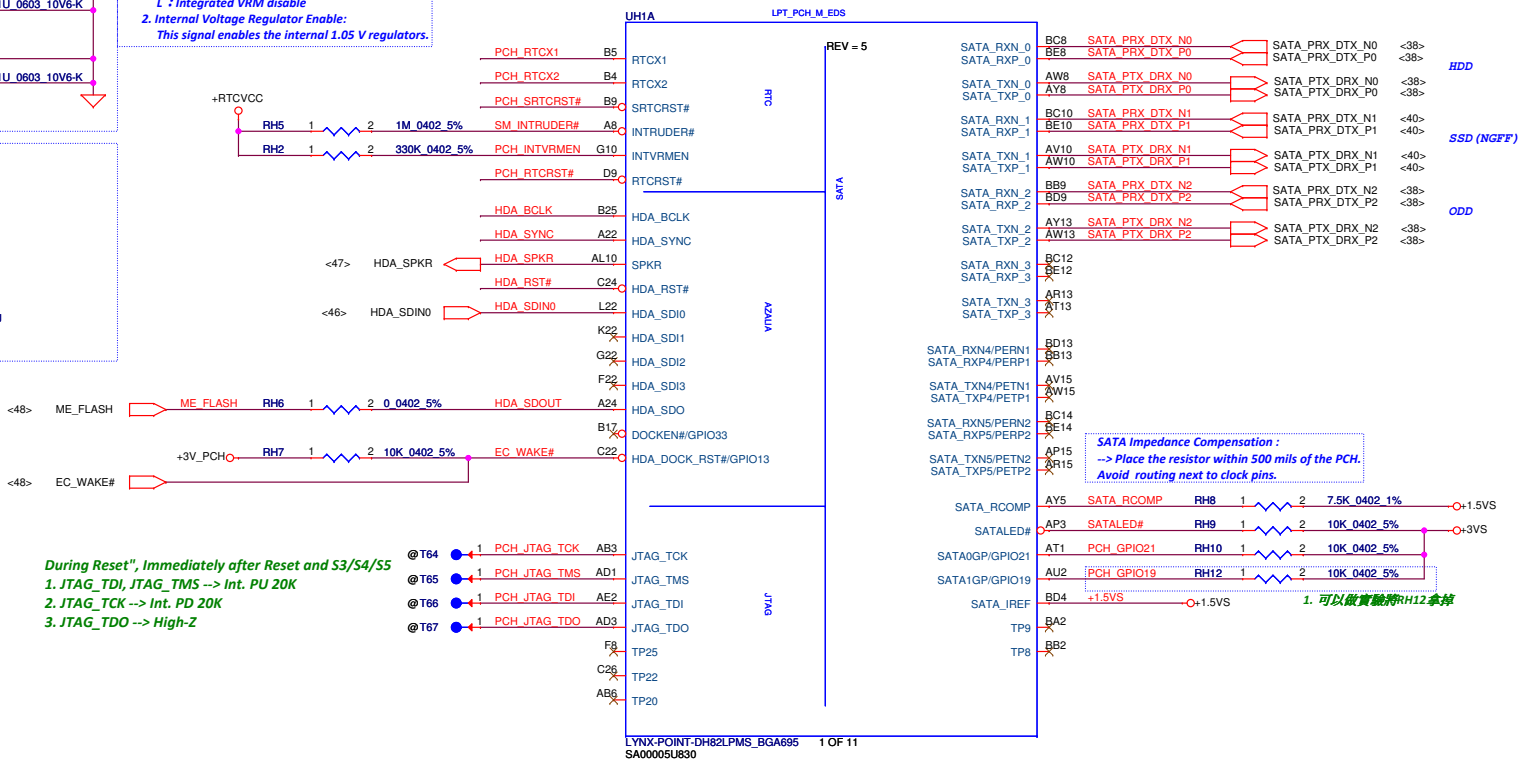
JCMOS, JME Setting, Need Under DDR Door



★ 1. INTVRMEN, should always be pull high
H : Integrated VRM enable (Default)
L : Integrated VRM disable
2. Internal Voltage Regulator Enable:
This signal enables the internal 1.05 V regulators.

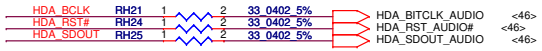




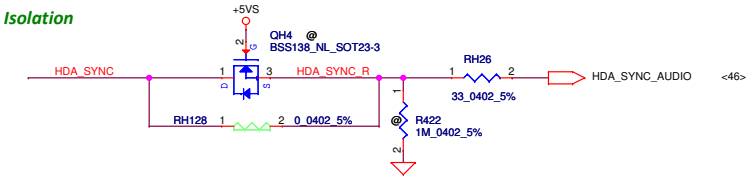
During Reset", Immediately after Reset and S3/S4/S5
1. JTAG_TDI, JTAG_TMS --> Int. PU 20K
2. JTAG_TCK --> Int. PD 20K
3. JTAG_TDO --> High-Z

HDA AUDIO SIGNAL

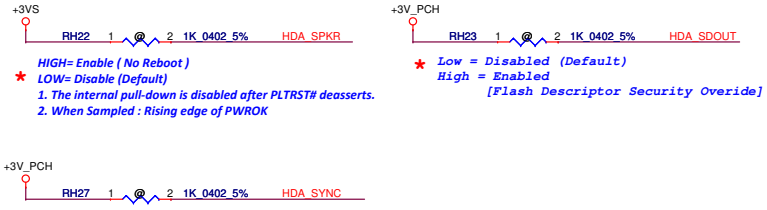
HDA AUDIO For Codec



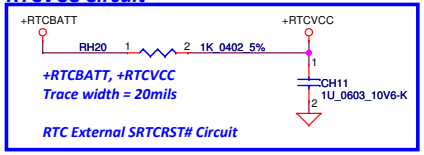
Isolation



HDA STRAP



RTCVCC Circuit



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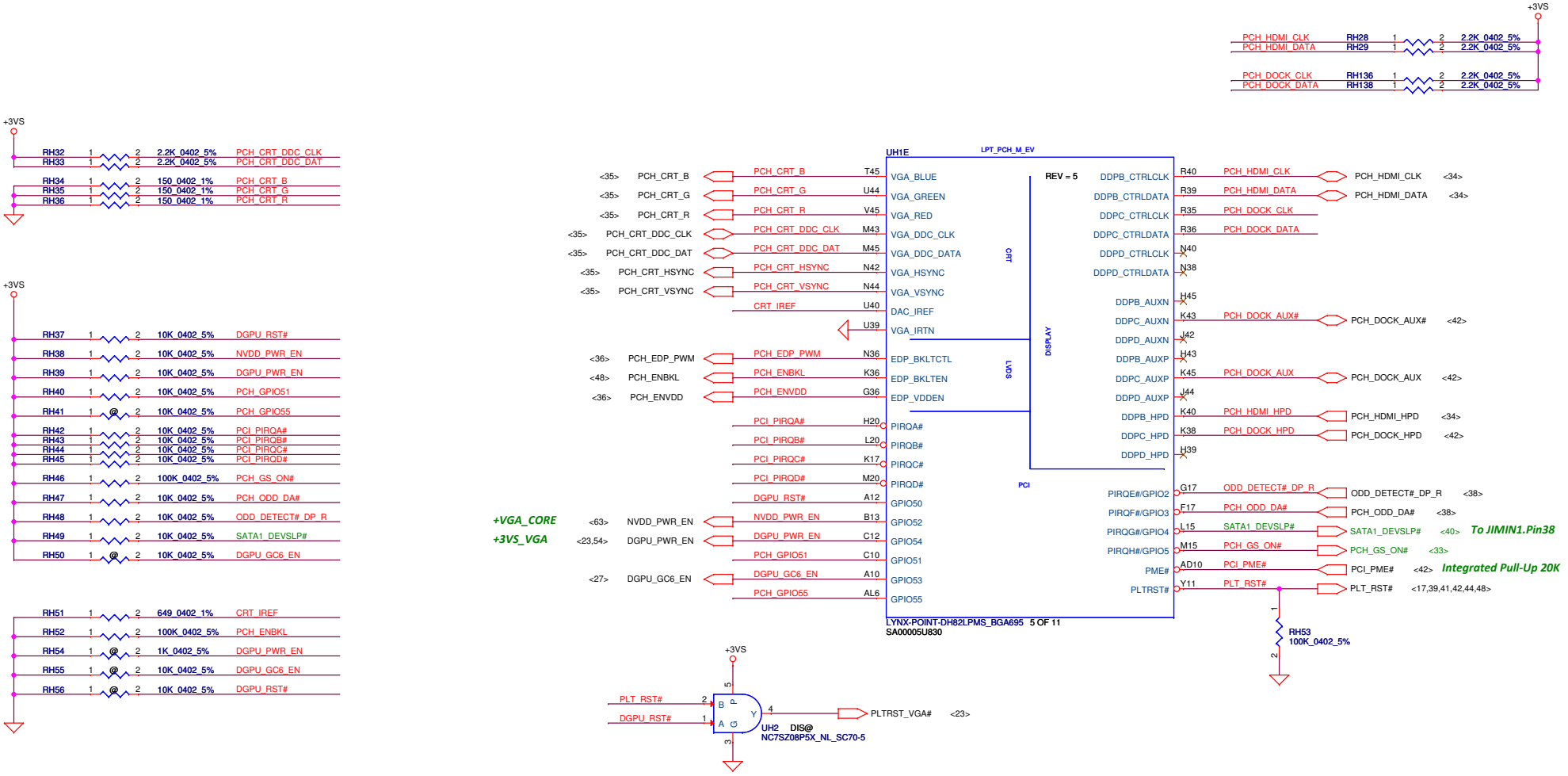
Title	PCH_RTC/HDA/SATA		
Size	Document Number		Rev
Custom	E440 NM-A151		1.0
Date:	Thursday, July 11, 2013	Sheet	13 of 57



A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled ★ **High=Default

1. The signal has a weak internal pull-up, which is disabled after PLTRST# deasserts.
2. When sampled : Rising edge of PWROK

Boot BIOS Straps (BBS)

BBS_BIT1 (GPIO51)	BBS_BIT0 (GPIO19)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI ★

1. GPIO51/19 has weak internal pull-up via 20kohm
2. The internal pull-up is disabled after PLTRST# deasserts.
3. GPIO51 (bit 11) at the rising edge of PWROK
   SATA1GP/GPIO19 (bit 10) at the rising edge of PWROK.

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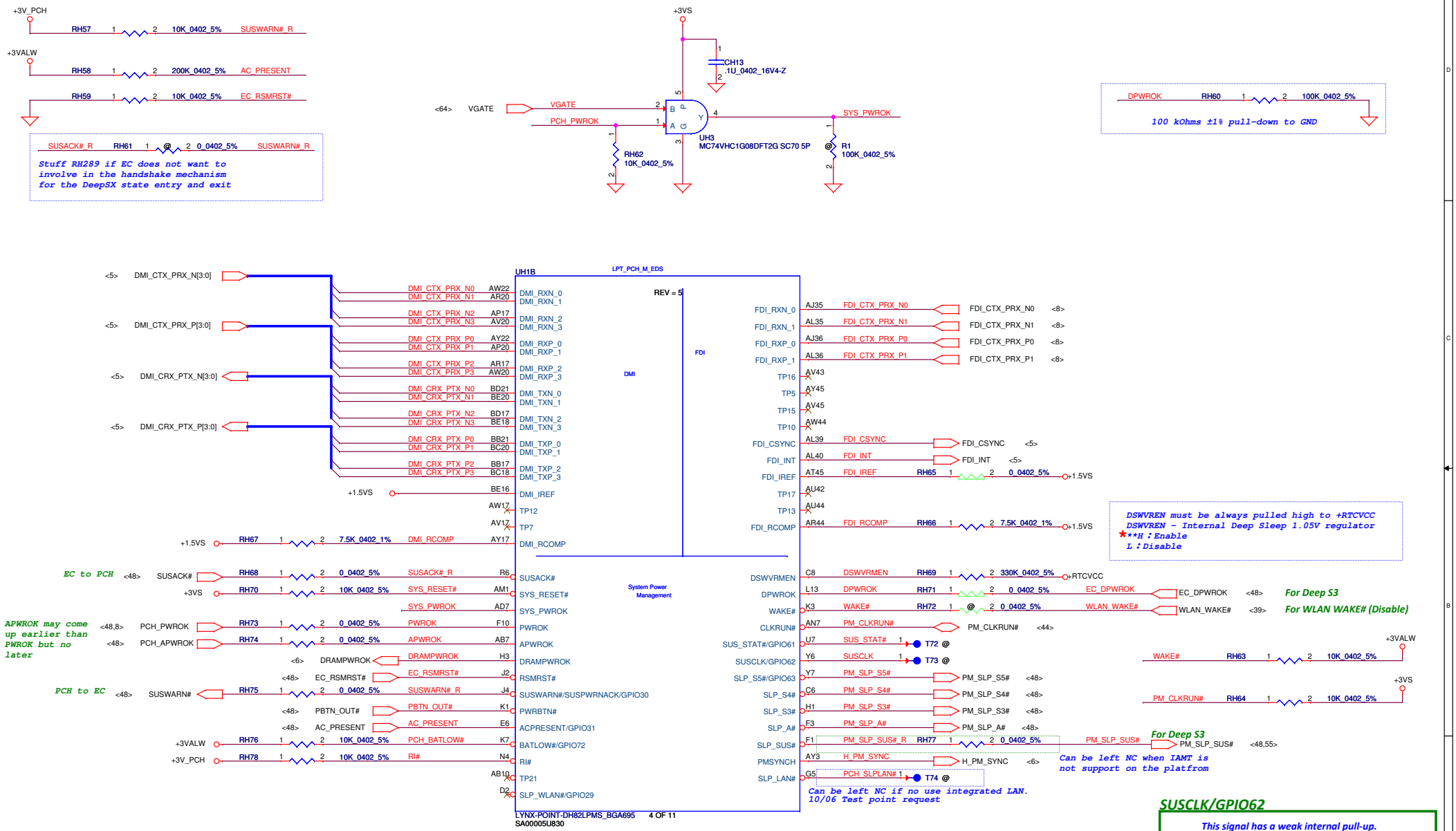
Title			
PCH_CRT/EDP/DDP			
Size: Custom	Document Number: E440 NM-A151		Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 14 of 57		



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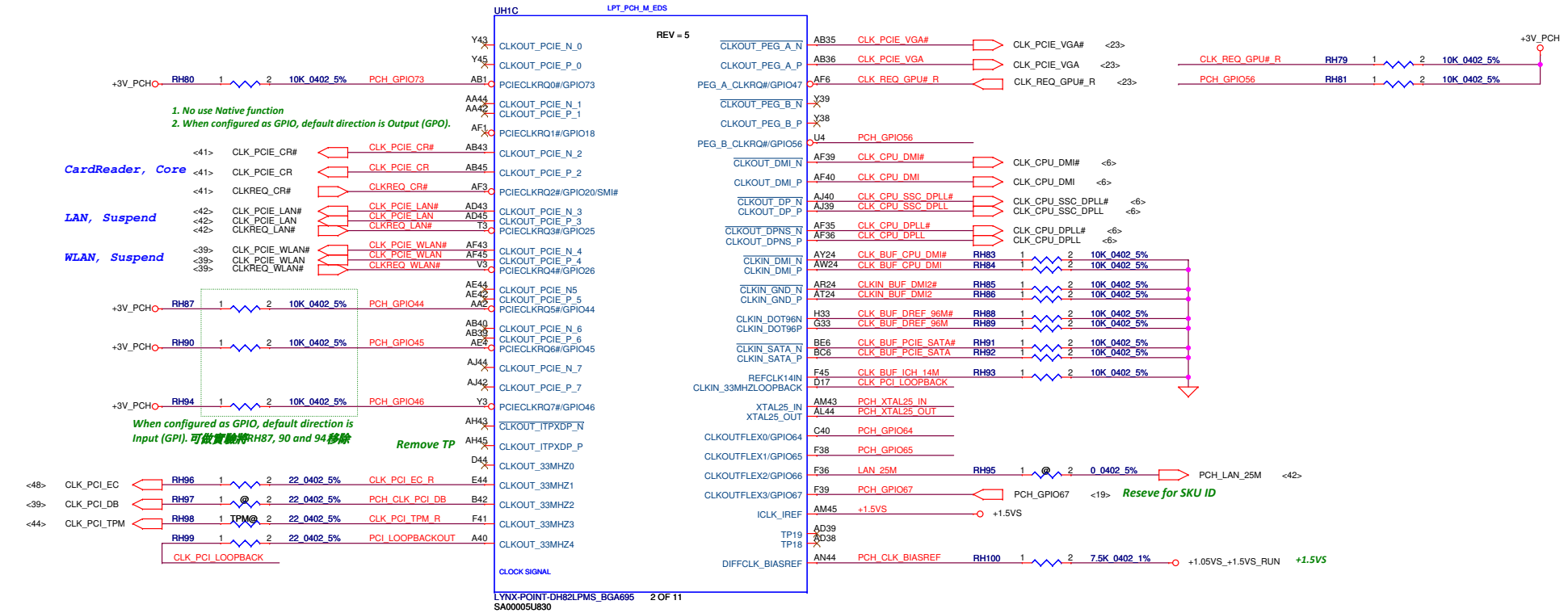
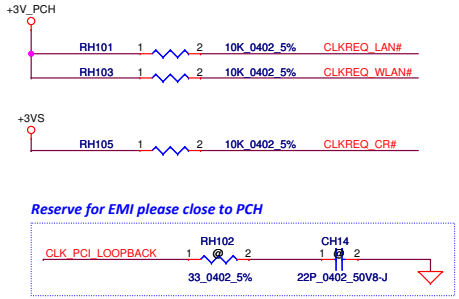
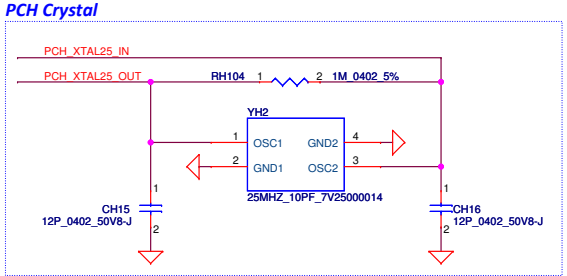
Title: PCH_DMI/FDI/PM

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 15 of 57

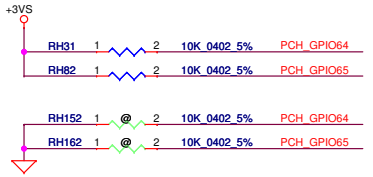






Project Phase ID

Project Phase	PCH_GPIO64	PCH_GPIO65
SDV, FVT	0	0
SIT2 (R 0.5)	0	1
SIT (R 0.4)	1	0
*SVT	1	1



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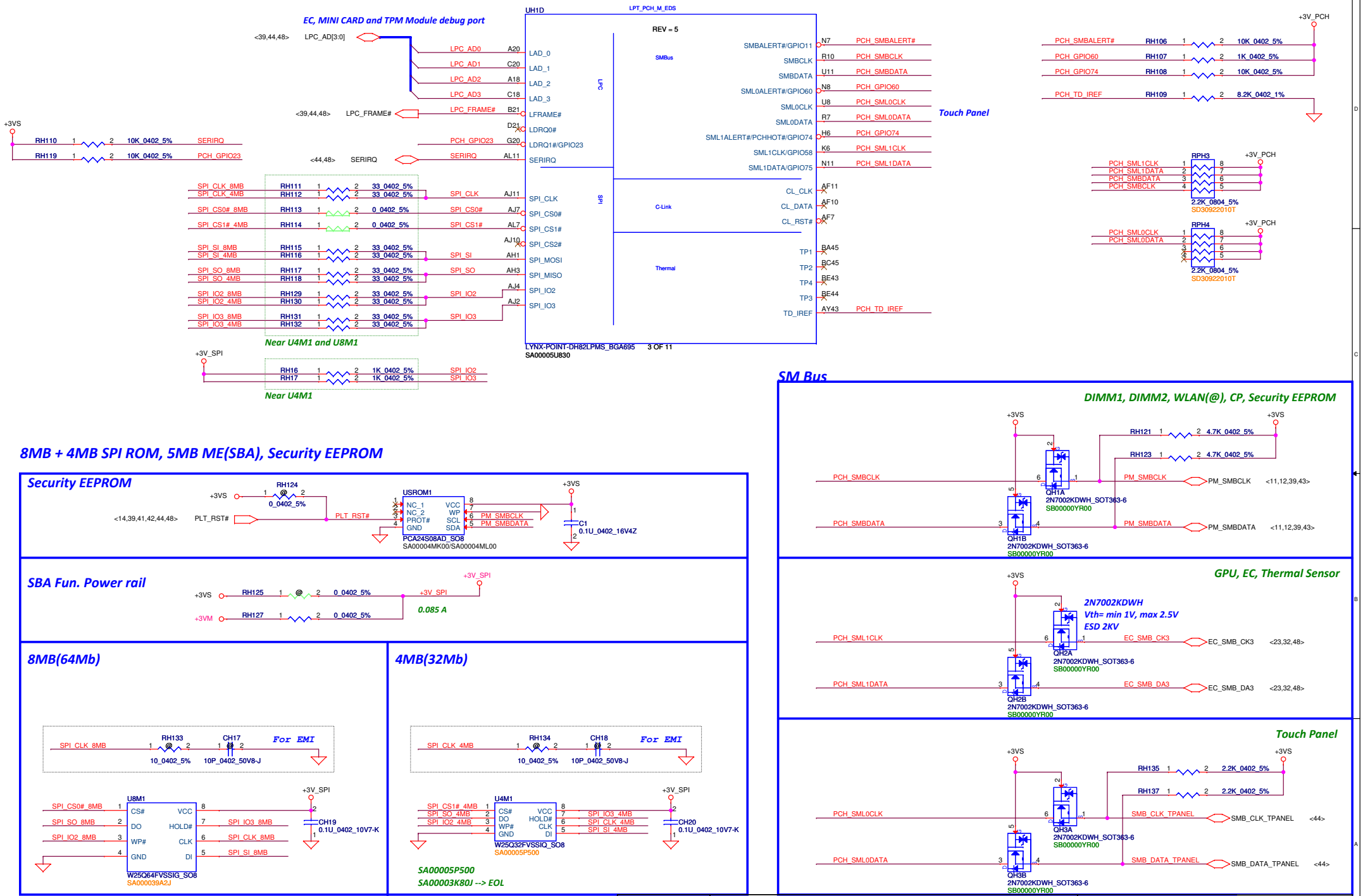
Title	PCH_PCIE/CLK		
Size	Document Number		Rev
Custom	E440 NM-A151		1.0
Date:	Thursday, July 11, 2013	Sheet	16 of 57



SM Bus

DIMM1, DIMM2, WLAN(@), CP, Security EEPROM

GPU, EC, Thermal Sensor

Touch Panel

8MB + 4MB SPI ROM, 5MB ME(SBA), Security EEPROM

Security EEPROM

SBA Fun. Power rail

8MB(64Mb)

4MB(32Mb)

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Title: PCH_LPC/SPI/SM BUS

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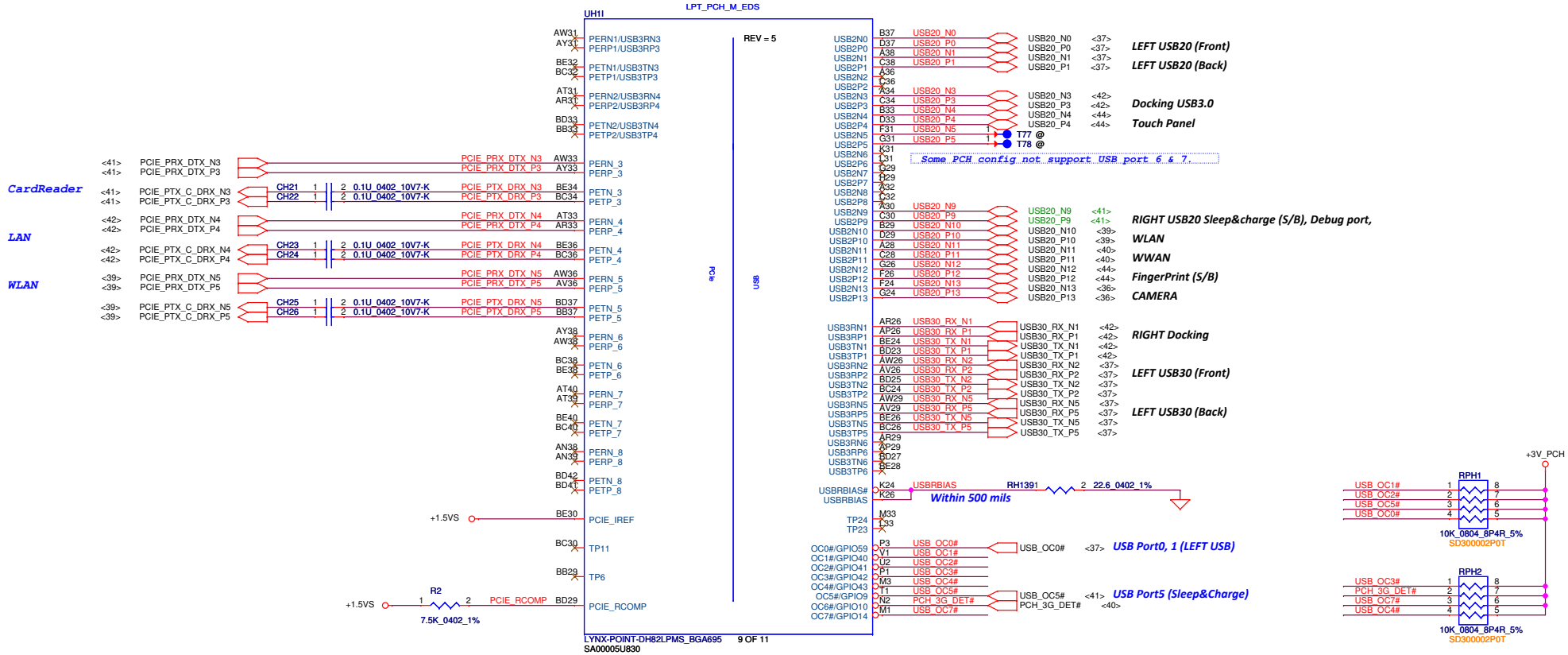
Date: Thursday, July 11, 2013 | Sheet 17 of 57



USB2.0 :
OC#0-3 --> Port 0-7
OC#4-7 --> Port 8-13

OC[3:0]# should be connected with USB 2.0 ports 0 - 7 and any 4 of USB 3.0 ports 1 - 6.

USB3.0	USB2.0	OC#	Note
Port1	Port3	X	Docking (Right)
Port2	Port0	OC0#	LEFT USB (Front)
Port5	Port1	OC0#	LEFT USB (Back)
X	Port9	OC5#	Sleep&Charge (Right)

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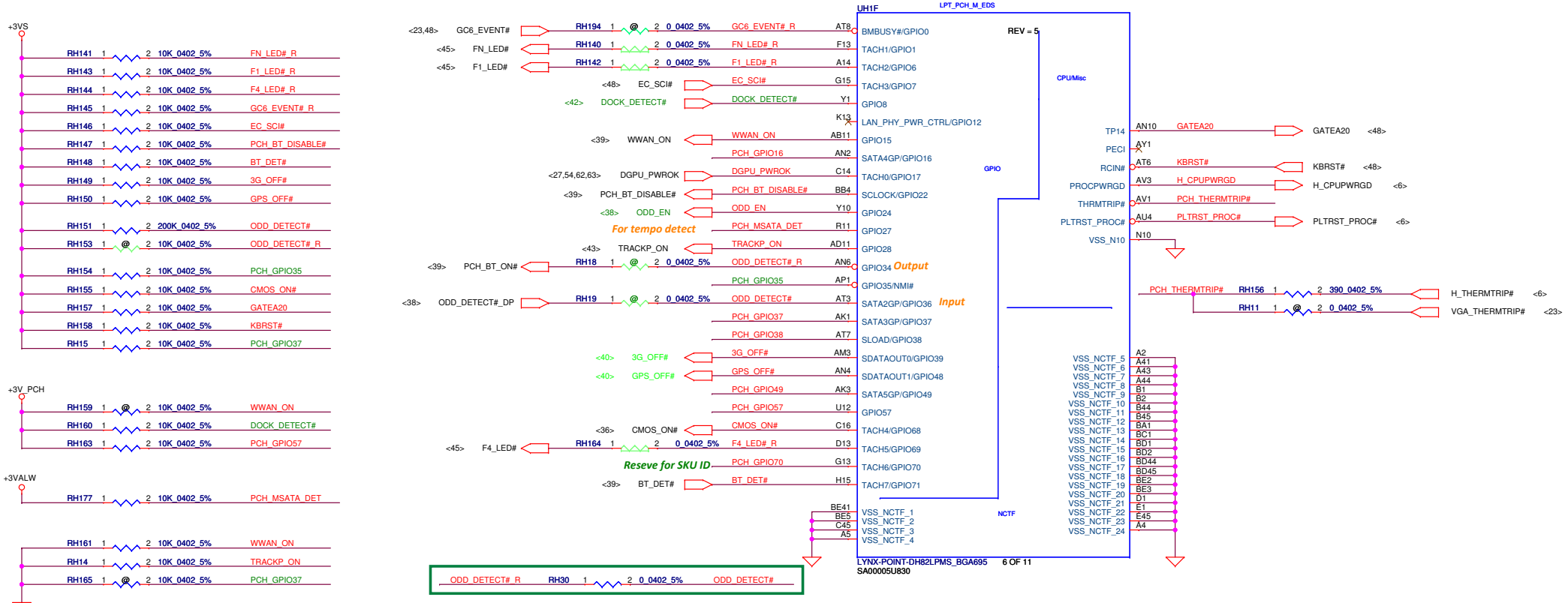
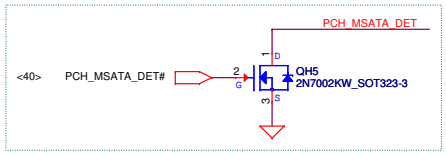
Title: PCH_PCIE/USB/OC#

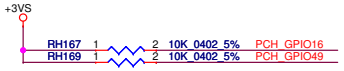
Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 18 of 57





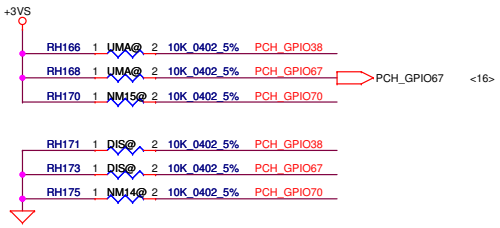
CONFIG	GPIO16, 49
* USB X4,PCIEX8,SATAX6	11
USB X6,PCIEX8,SATAX4	01



No use Flexible I/O pin, delete RH172, RH174

SKU ID

Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
* Optimus	0	0	
Reserve	0	1	
DIS	1	0	
* UMA	1	1	
* 14"			0
* 15"			1



Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1 (00)	PCIE 2 (00)	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4 (00)	SATA 5 (00)	SATA 0	SATA 1	SATA 2	SATA 3
				USB3 3 (01)	USB3 4 (01)							PCIE 1 (01)	PCIE 2 (01)				

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Title: PCH_GPIO/CPU-MISC

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

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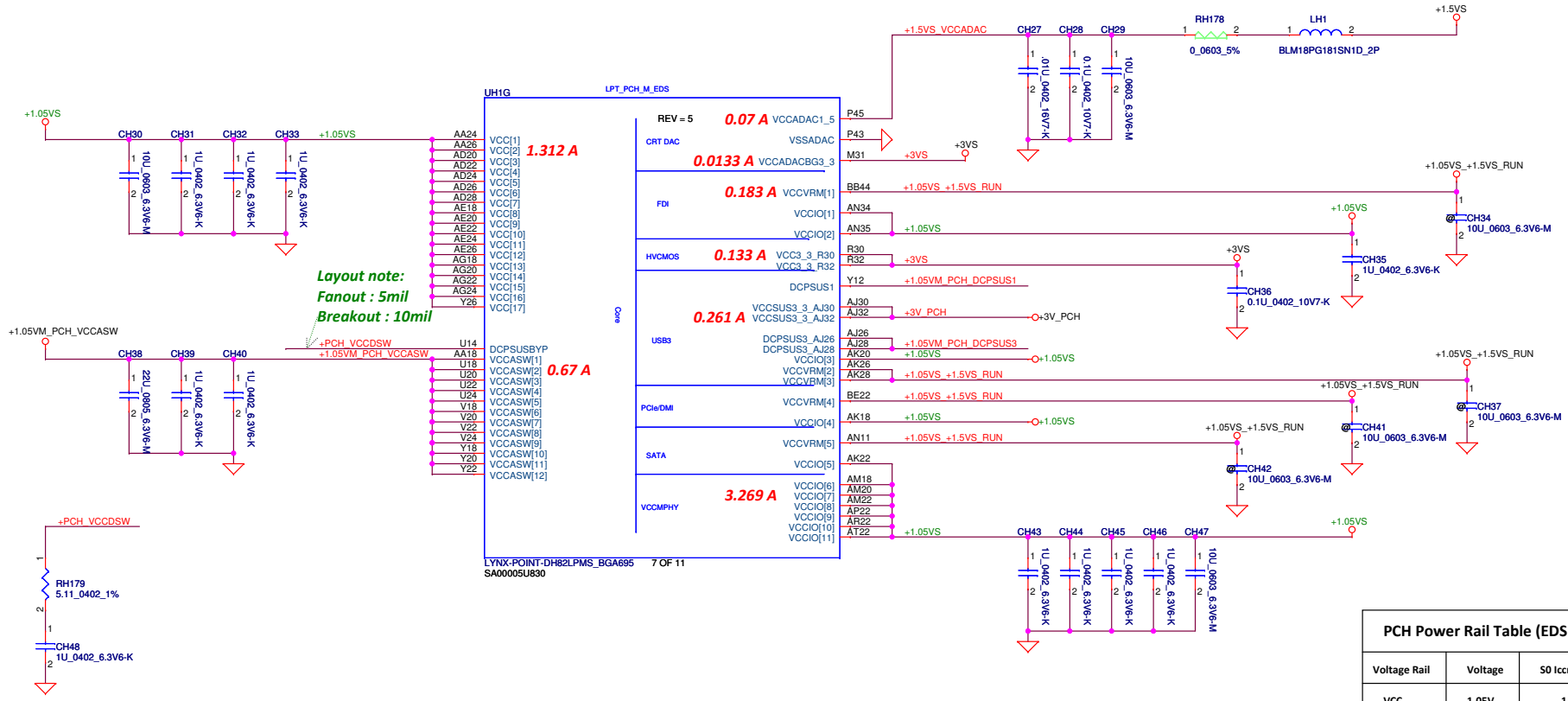

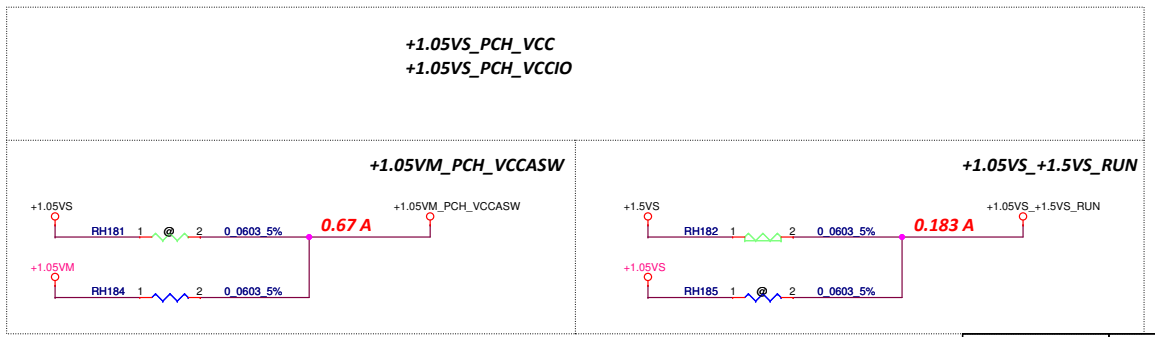

PCH Power Rail Table (EDS Rev1.0)		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.312 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.07 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.183 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

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Title: PCH_POWER-1

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

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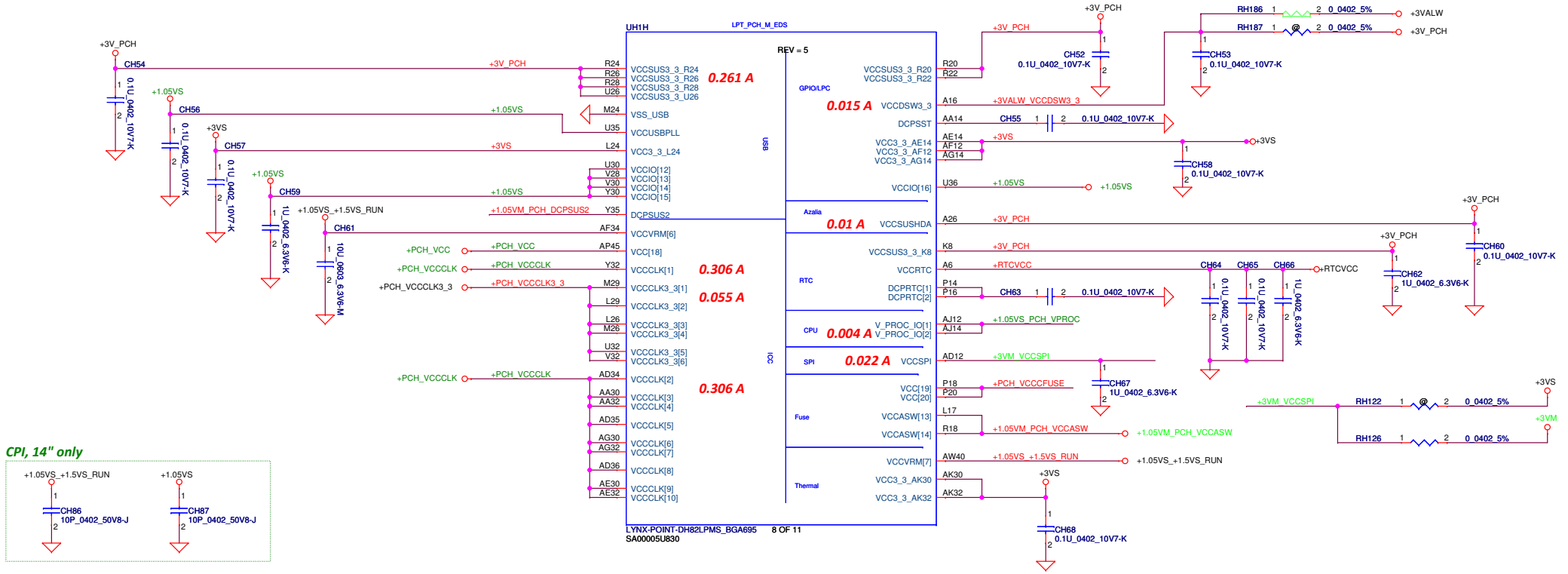
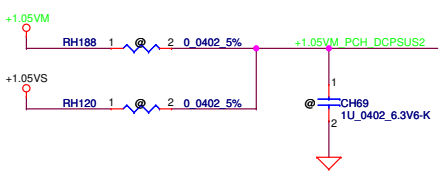
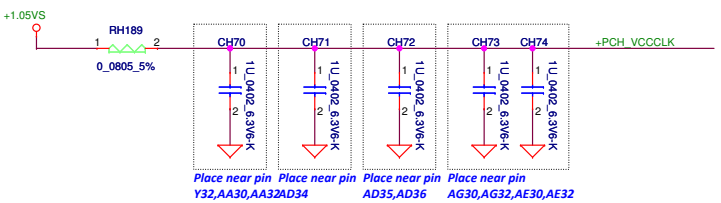


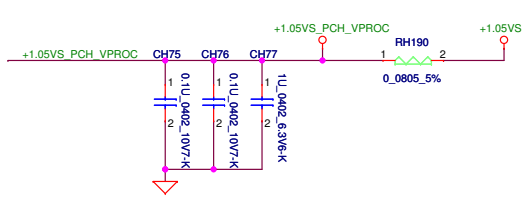
+1.05VM_PCH_DCPSUS2



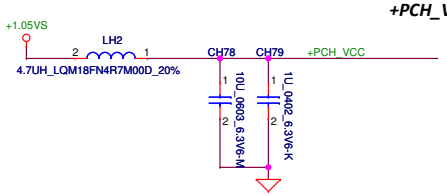
+PCH_VCCCLK



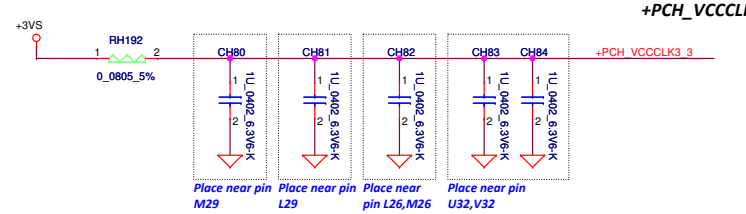
+V_VPROC



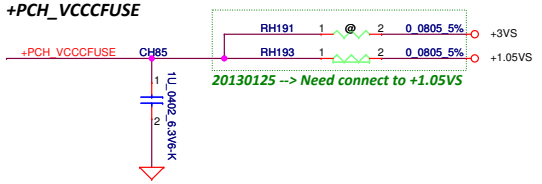
+PCH_VCC



+PCH_VCCCLK3_3



+PCH_VCCCFUSE



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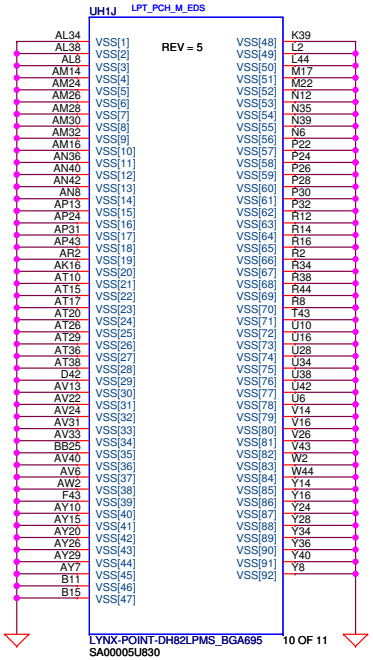
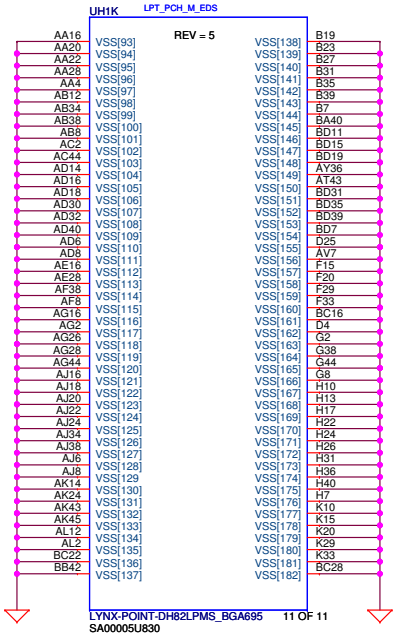
Title: PCH_POWER-2

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 21 of 57





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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: PCH_GND

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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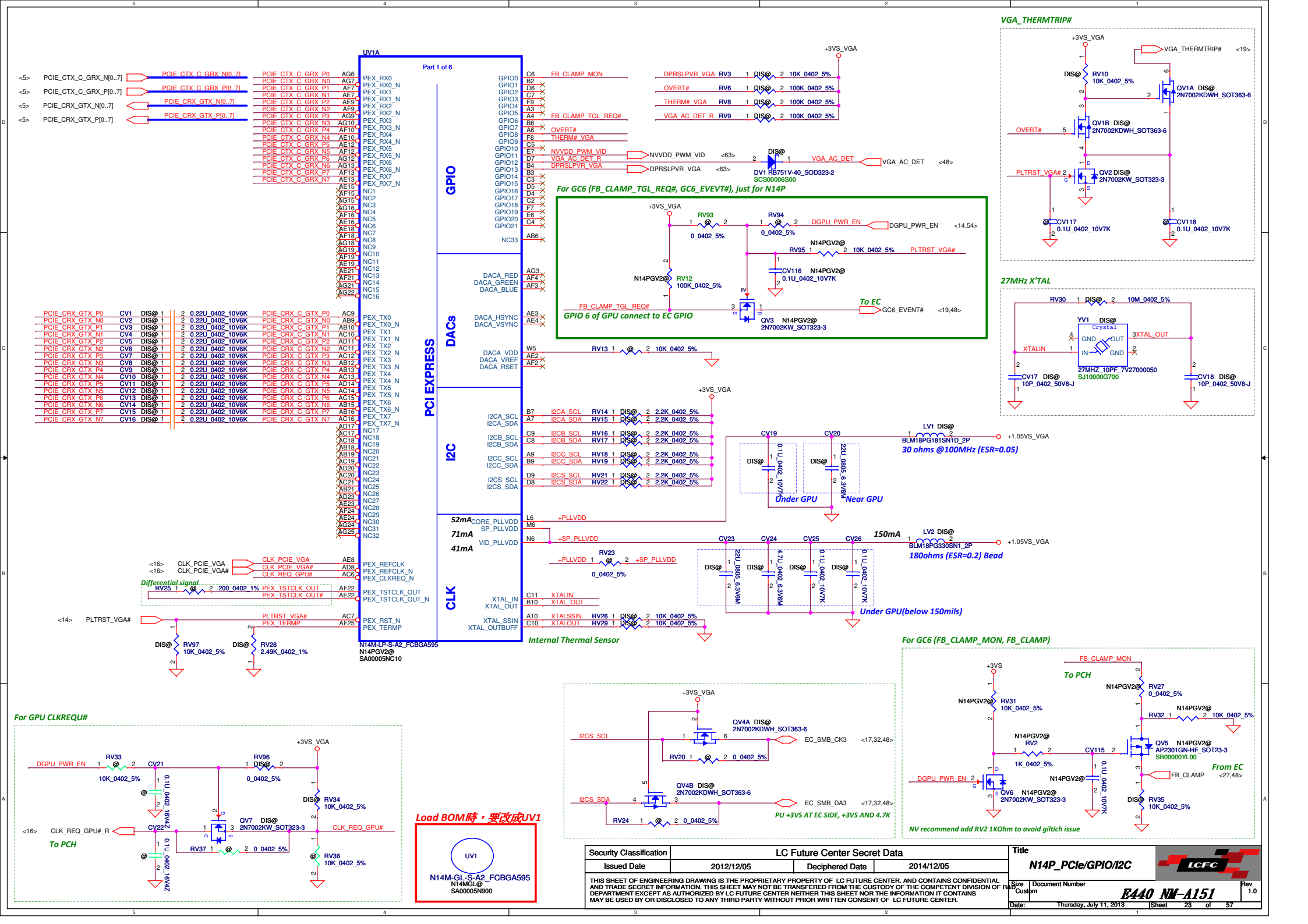

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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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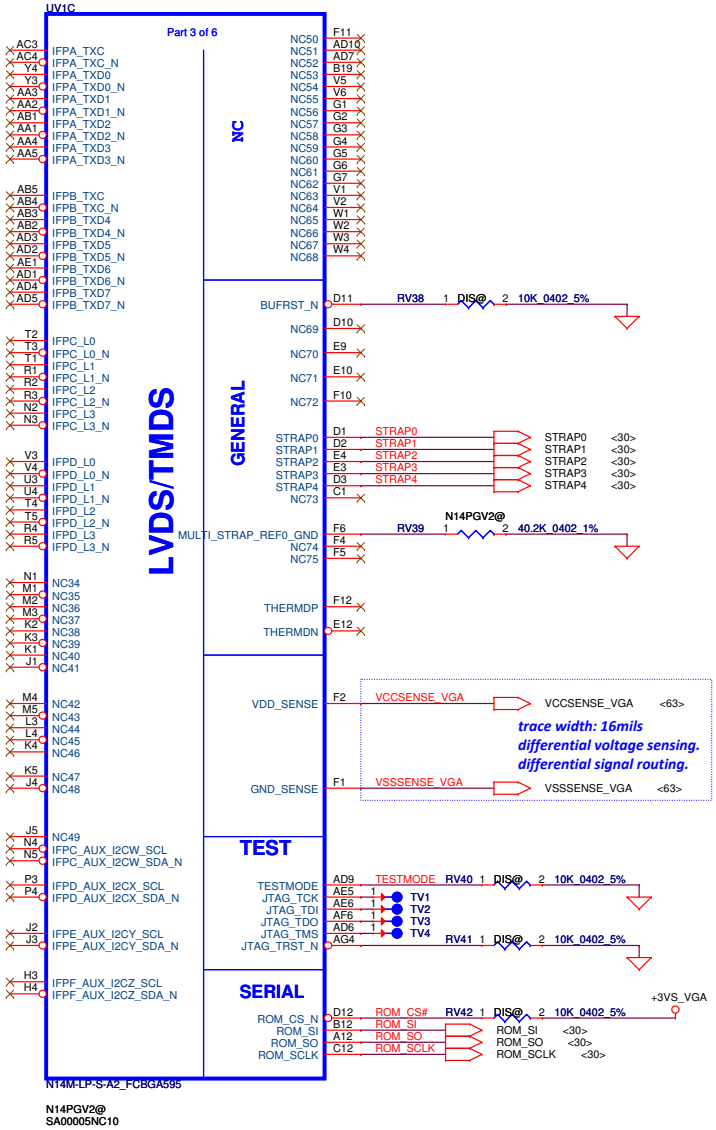
Title	N14P_PCIe/GPIO/I2C		
Size	Document Number		Rev
Custom	E440 NM-A151		1.0
Date:	Thursday, July 11, 2013	Sheet	23 of 57



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Title: N14P_SPI ROM/SENSE

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

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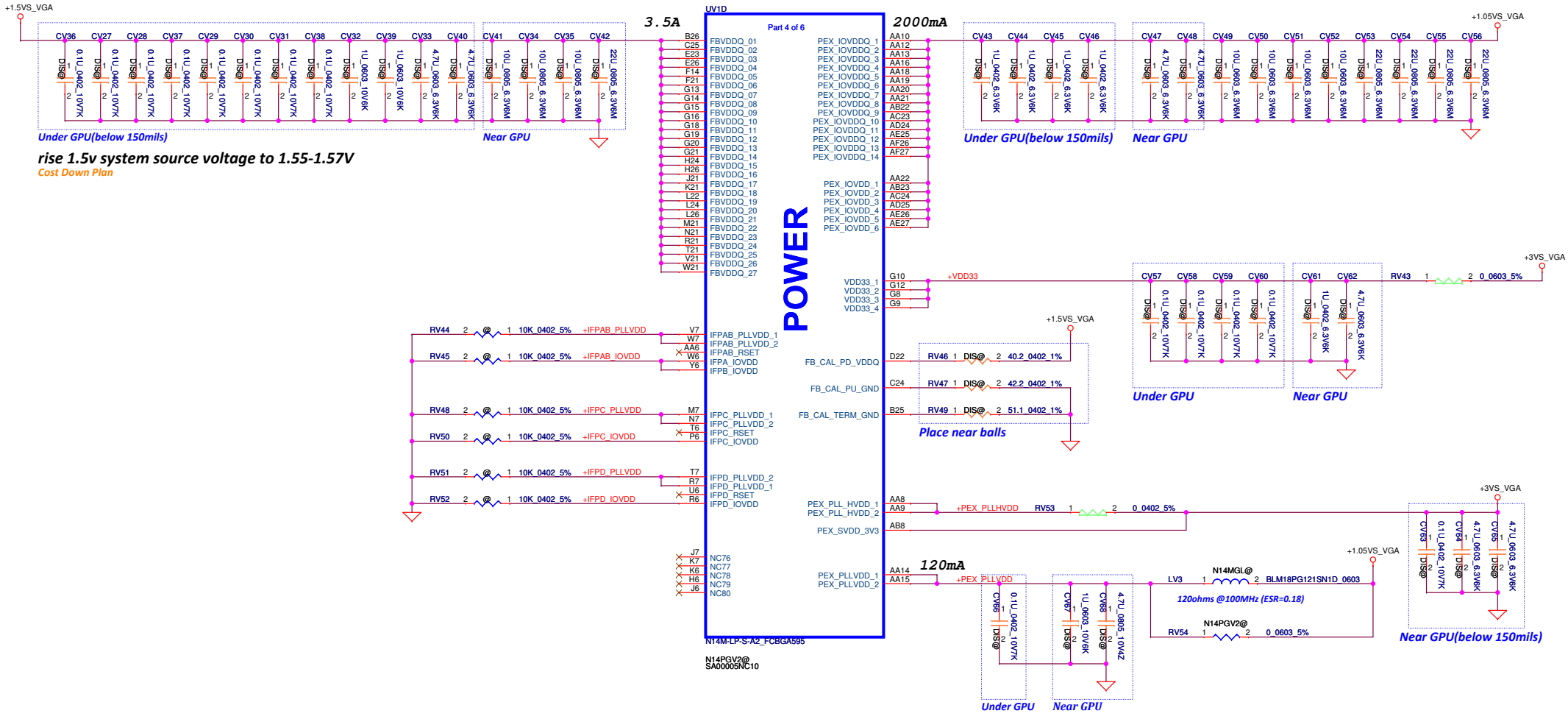

CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: N14P_POWER

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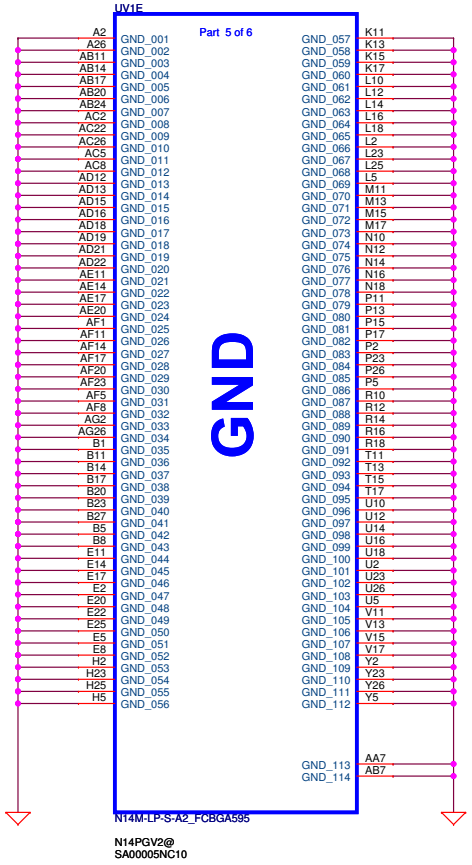

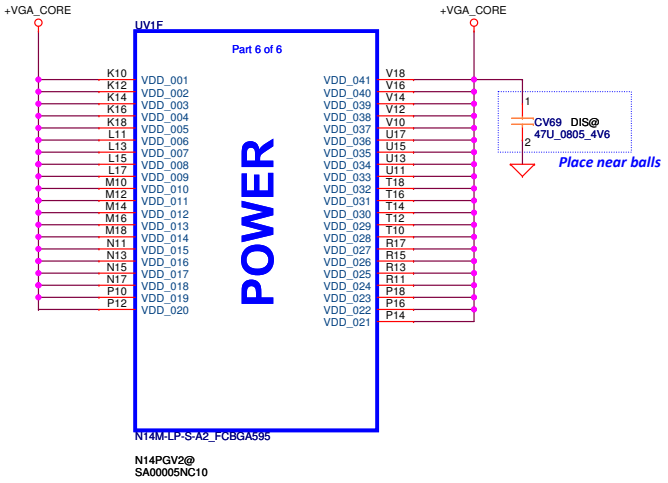

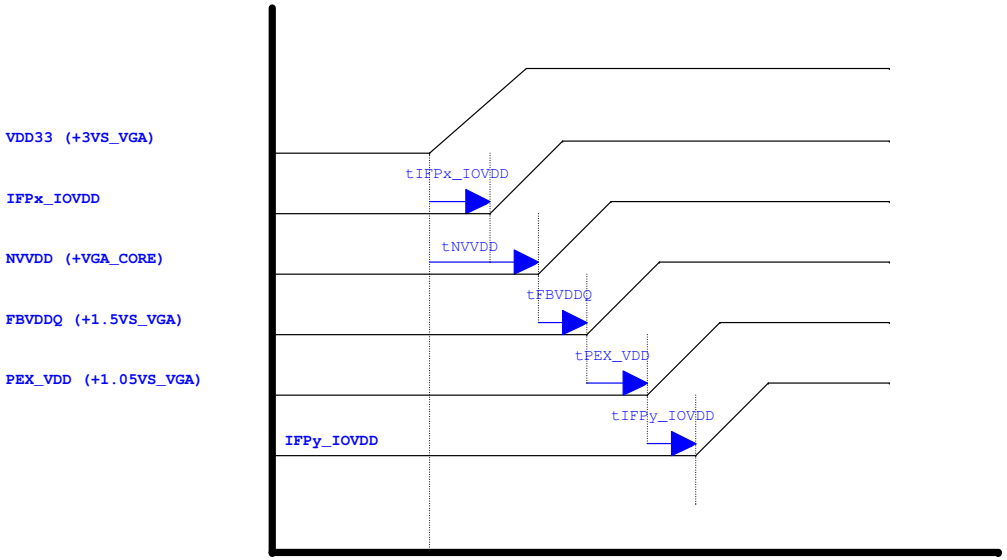

NV Recommended Power On Sequencing Order

X=A and B
Y=C,D,E and F

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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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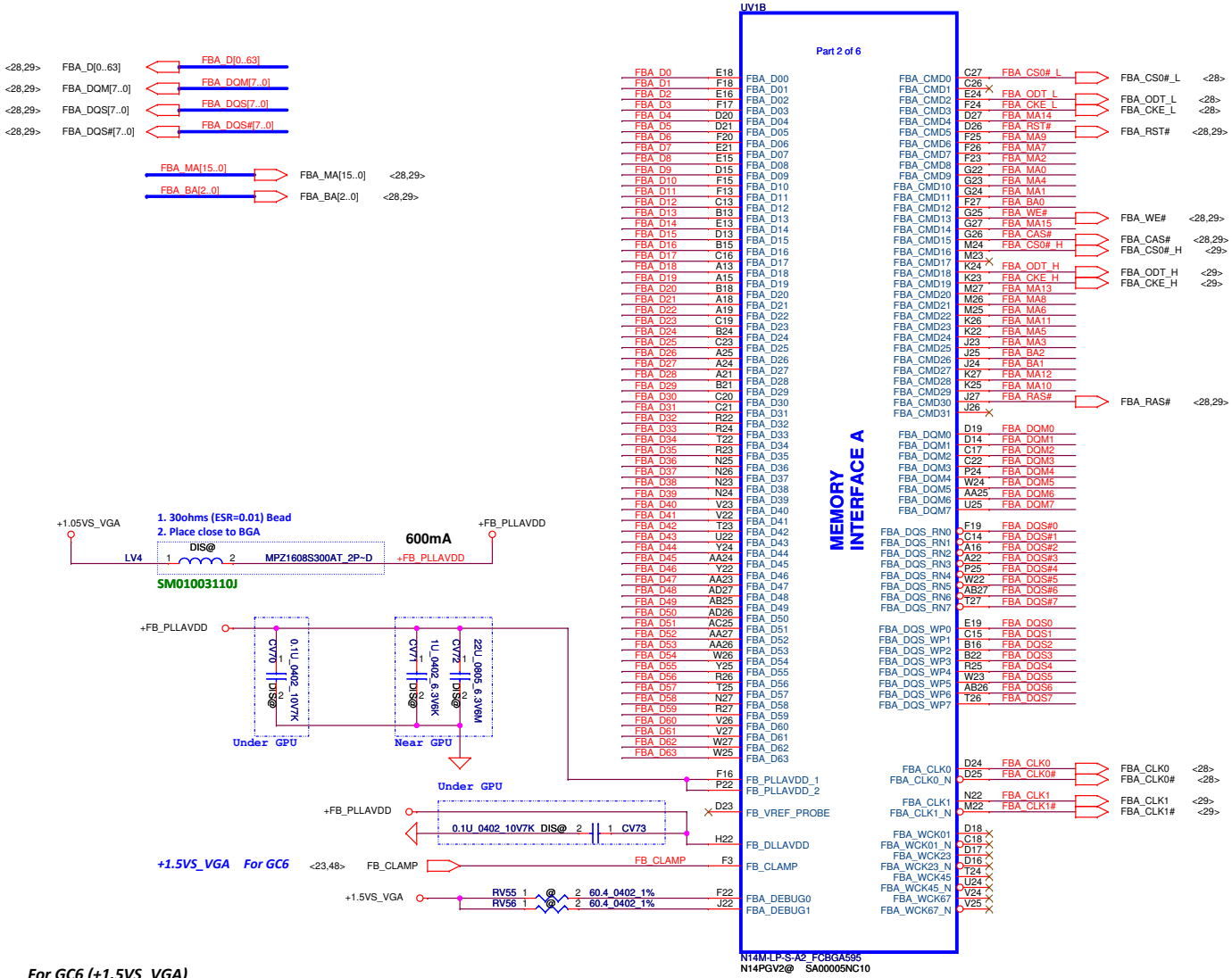
Title: N14P_VDD/GND

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

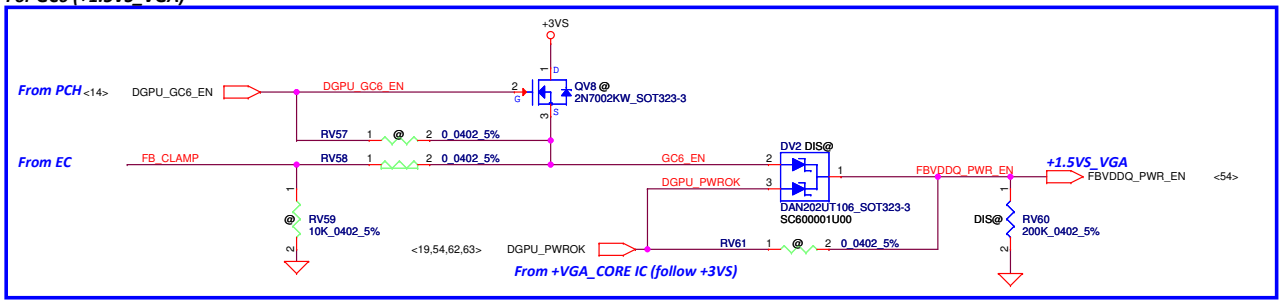
Date: Thursday, July 11, 2013 Sheet 26 of 57



Mode D – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

For GC6 (+1.5VS_VGA)



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Title: N14P_MEM IF/FB CLAMP

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

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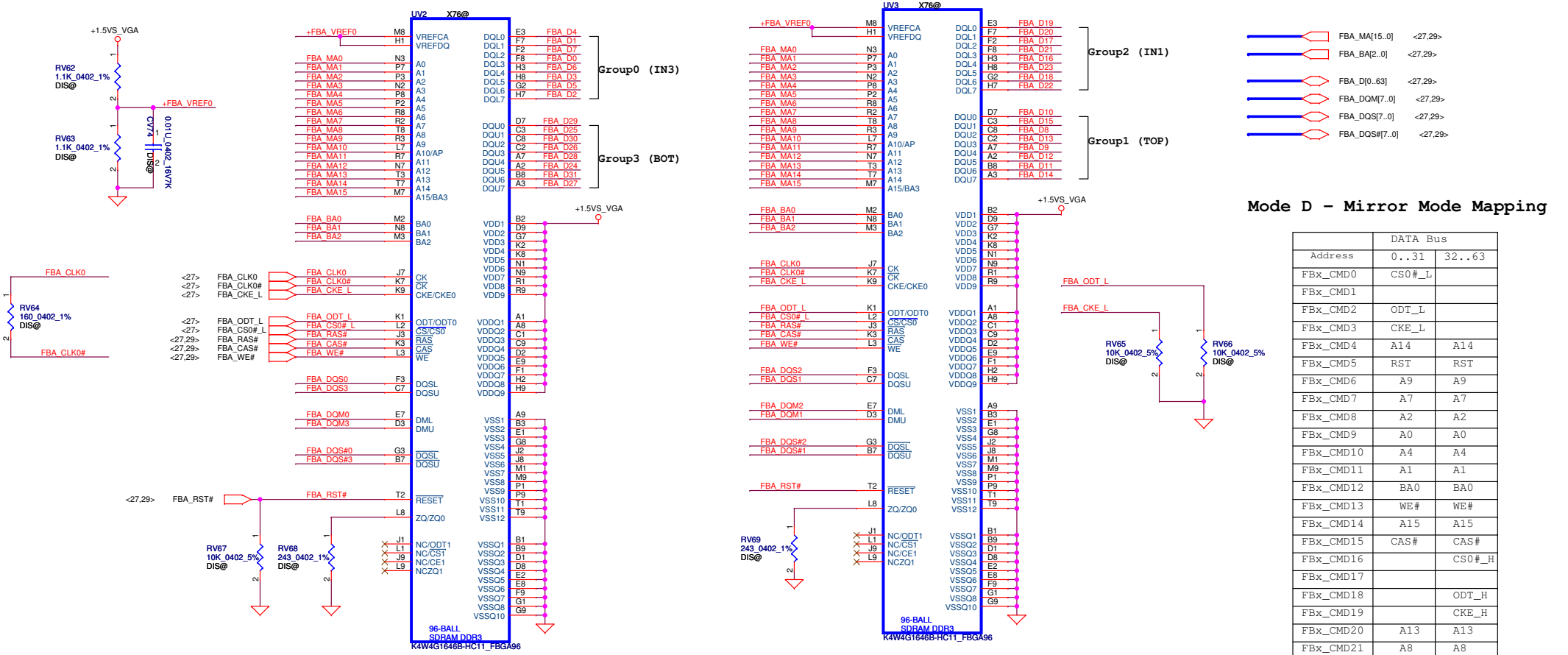
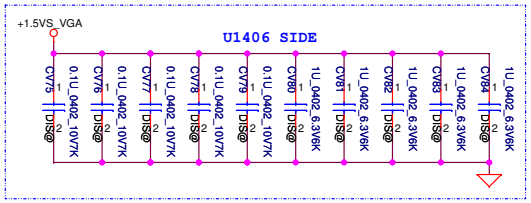
Memory Partition A - Lower 32 bits

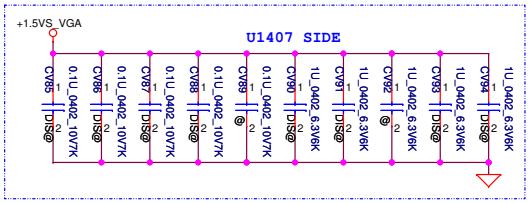


FBA_MA[15..0] <27,29>
FBA_BA[2..0] <27,29>
FBA_D[0..63] <27,29>
FBA_DQM[7..0] <27,29>
FBA_DQS[7..0] <27,29>
FBA_DQS#[7..0] <27,29>

Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#





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Title: N14P_DDR3-A LOWER

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

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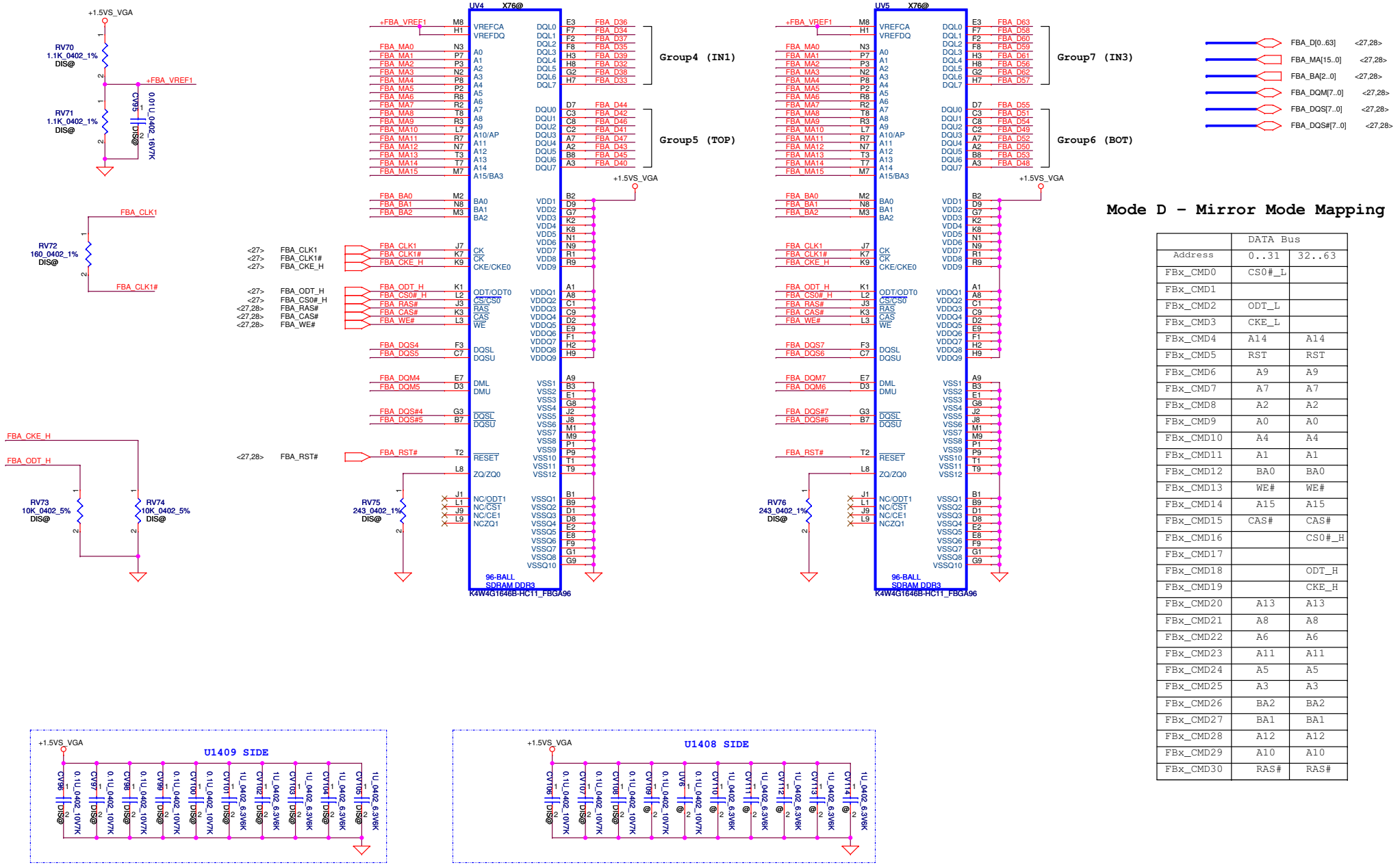
Memory Partition A – Upper 32 bits



Mode D – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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Title: N14P_DDR3-A UPPER

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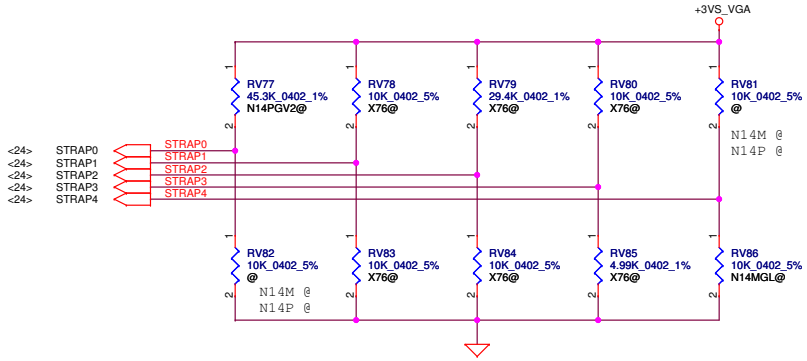
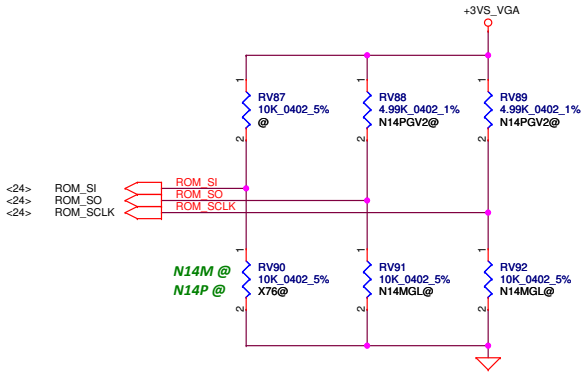
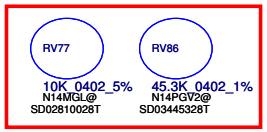
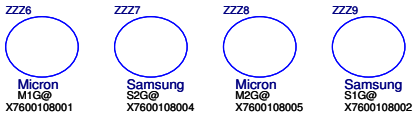




For N14P-GV2 QS Sample
ROM_SO change from PU 10K to PU 5K
ROM_SCLK change from PD 15K to PU 5K
STRAP1 change from PD 5K to PD 45K
STRAP2 change from PU 30K to PD 15K
STRAP4 change from PD 5K to PD 45K



Load BOM時，要改成RV86, RV77



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG[3:0]	
0110	Gen1/Gen2 support only
0000	Gen3 support

FB[1:0]	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

PCIE_MAX_SPEED	
0	Limit booting to PCIE Gen1
1	Allow booting to PCIE Gen 2/3

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_SPEED_CHANGE_GEN3	
0	Disable PCIE Gen3 operation
1	Enable PCIE Gen3 operation

DP_PLL_VDD33V	
0	Reserved
1	Default

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Title: N14P_MISC(1/2)

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						X76 RV90	RV77	PU, RV78 PD, RV83	PU, RV79 PD, RV84	PU, RV80 PD, RV85	PD, RV86
	GPU	FB Memory GDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
S2G, X76~04 SA00005OM00 M2G, X76~05 SA00005ON00	N14P-GV2	Samsung 1000MHz	K4W2G1646E-BC1A 128Mx16	PU 5K		PD 45K PD 30K PD 20K PD 10K	PU 45.3K	PD 45.3K	PD 15K	PD 5K	PD 45.3K
		Micron 1000MHz	MT41J128M16JT-093G 128Mx16								
		*Samsung 900MHz	K4W4G1646B-HC11 256Mx16								
		*Micron 900MHz	MT41K256M16HA-107G 256Mx16								

							RV77	PU, RV78 PD, RV83	PU, RV79 PD, RV84	PU, RV80 PD, RV85	PD, RV86
	GPU	FB Memory GDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
S1G, X76~02 SA00005SH20	N14M-GL	*Samsung 1000MHz	K4W2G1646E-BC1A 128Mx16	PD 10K			PU 10K	PD 10K	PU 10K	PD 10K	PD 10K
		Hynix 1000MHz	H5TQ2G63DFR-N0C 128Mx16				PD 10K	PU 10K	PU 10K	PD 10K	
M1G, X76~01 SA00005M110		*Micron 1000MHz	MT41J128M16JT-093G 128Mx16				PU 10K	PD 10K	PD 10K	PD 10K	
		Samsung 900MHz	K4W4G1646B-HC11 256Mx16				PU 10K	PU 10K	PU 10K	PU 10K	
		Hynix 900MHz	H5TQ4G63MFR-11C 256Mx16				PU 10K	PU 10K	PD 10K	PD 10K	
		Micron 900MHz	MT41K256M16HA-107G 256Mx16				PD 10K	PD 10K	PU 10K	PU 10K	

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: N14P_MISC(2/2)

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

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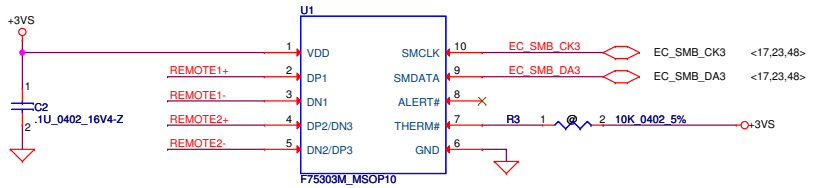
Thermal Sensor

Thermal Sensor
placed near by VRAM

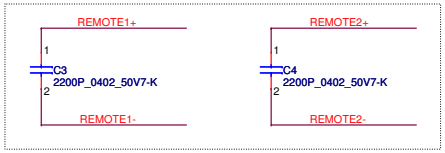


Address 1001_101xb

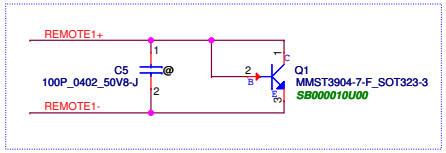
Internal pull up 1.2K to 1.5V

R for initial thermal shutdown temp

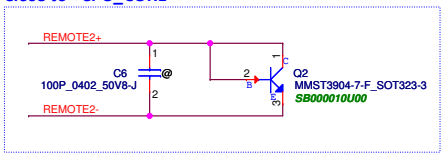
Close to U2



Close to BOTTOM DDR3



Close to +CPU_CORE



REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: THERMAL SENSOR

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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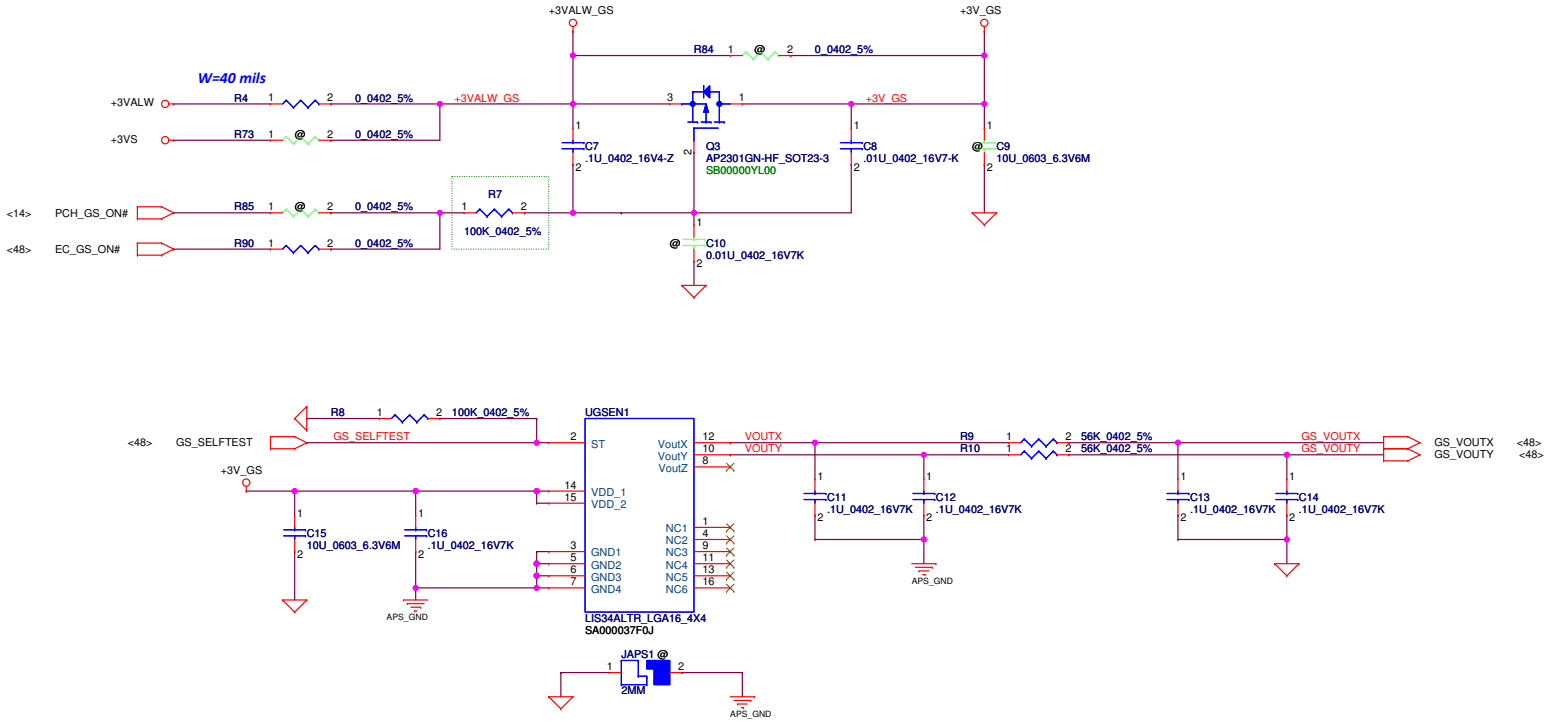
APS G-Sensor



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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: APS G-SENSOR

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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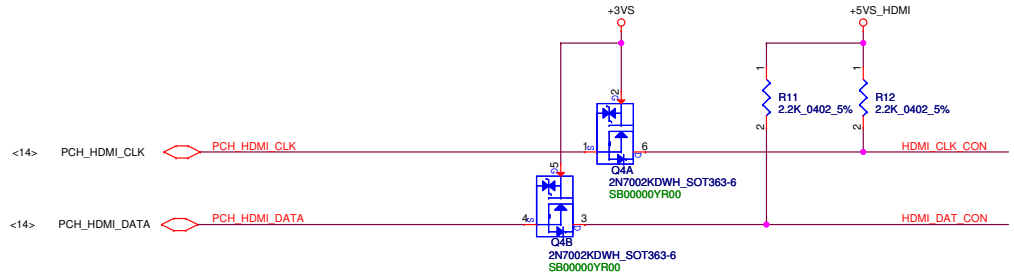
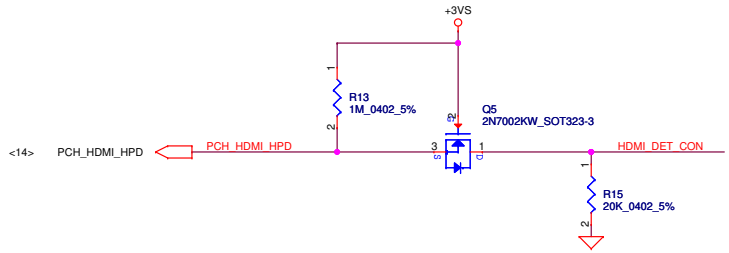
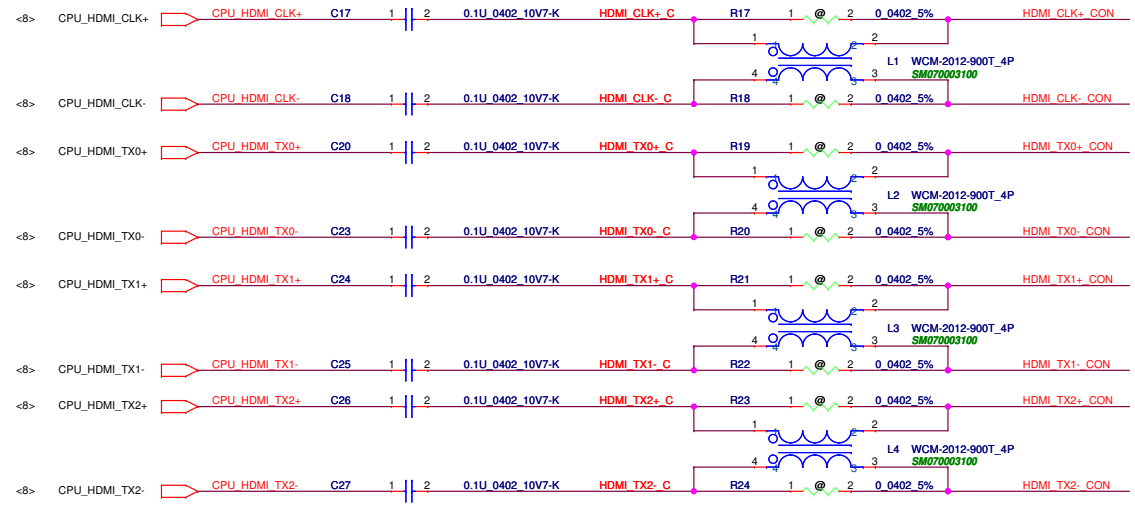
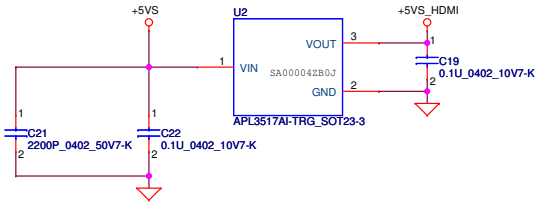
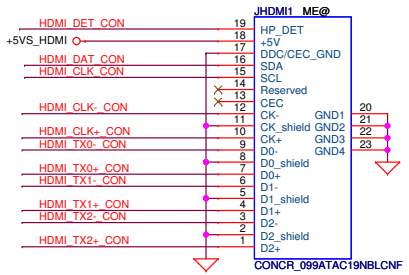


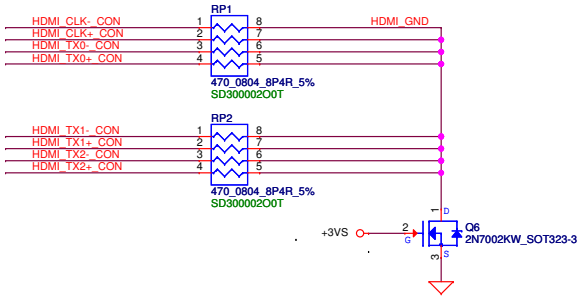




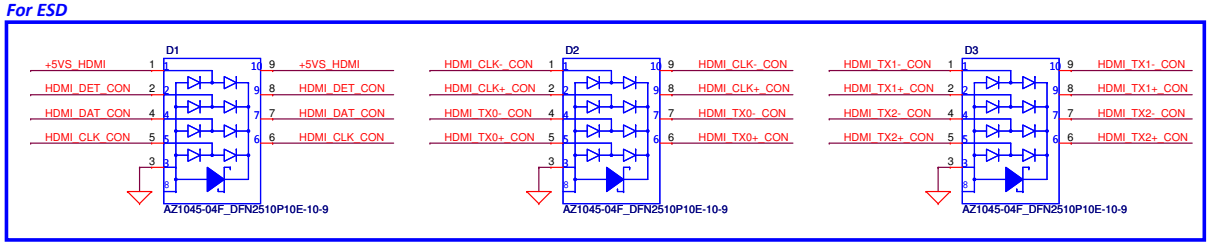


HDMI CONN.





For ESD



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Title: HDMI CONN.

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Custom	E440 NM-A151	1.0

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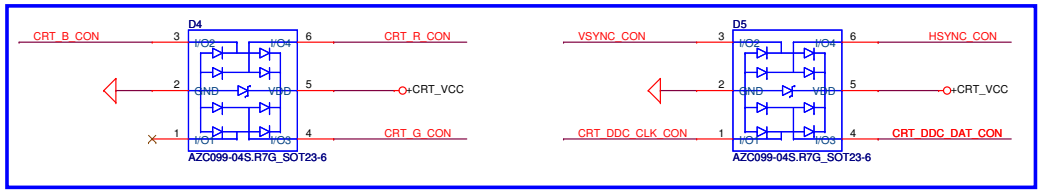
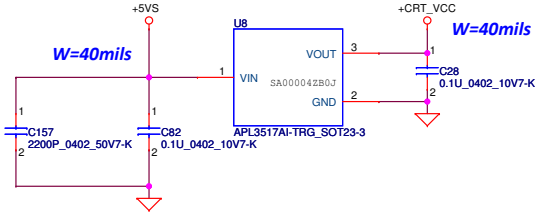


closer to JCRT



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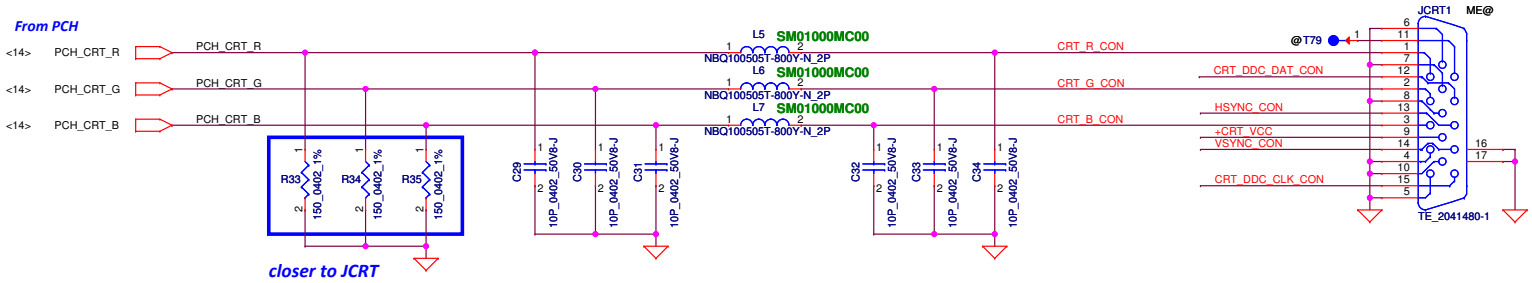
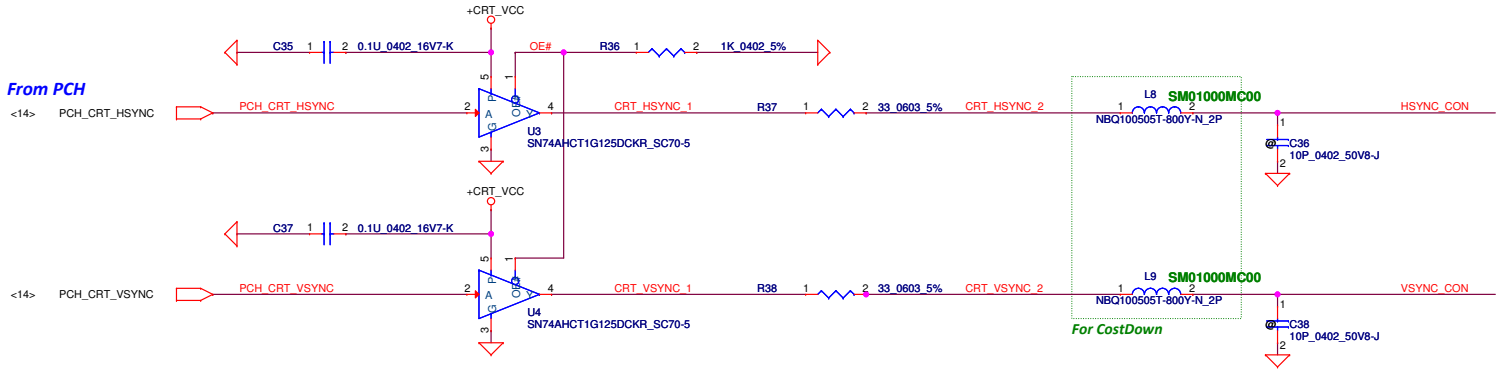
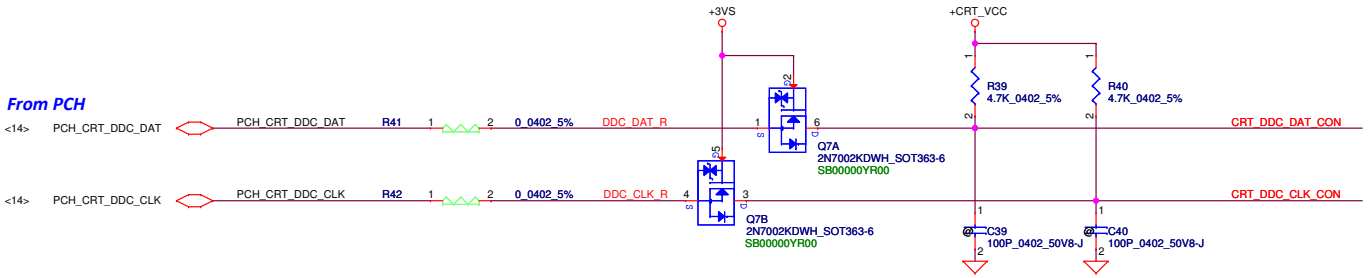


closer to JCRT





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Title: CRT CONN.

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

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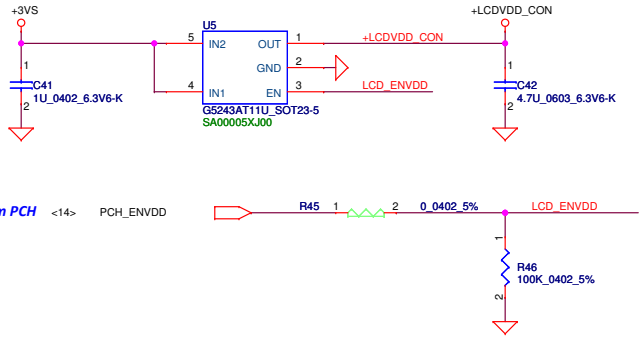
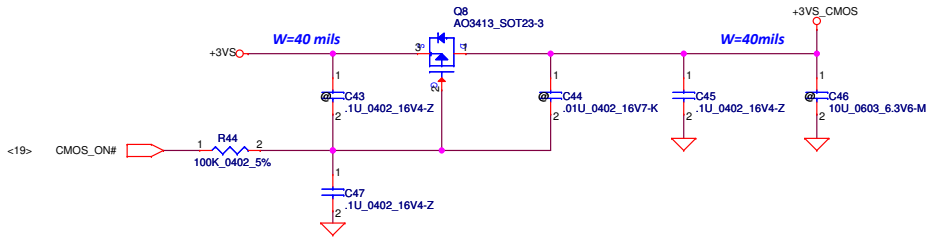
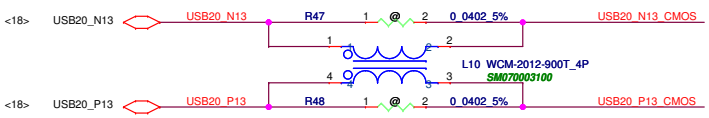
LCDVDD Circuit

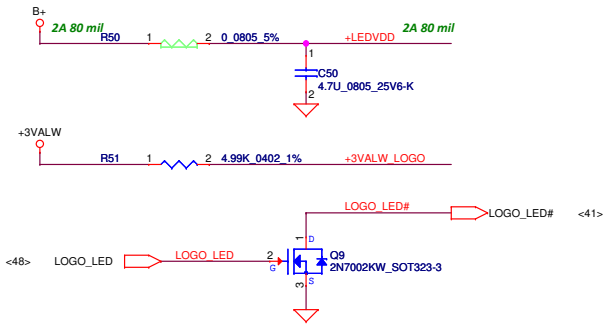


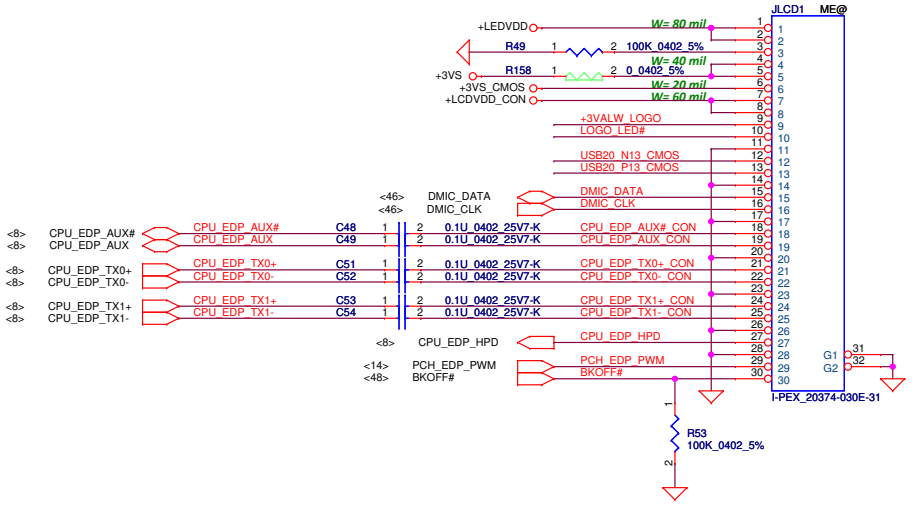
CMOS Camera



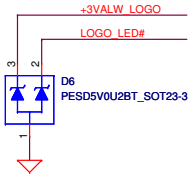
CMOS USB Port10



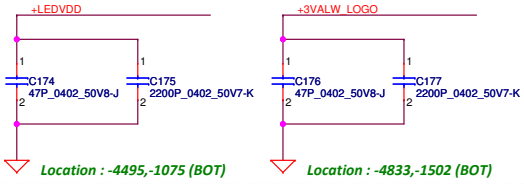




ESD request



EMI



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Title: LCD/CMOS CONN.

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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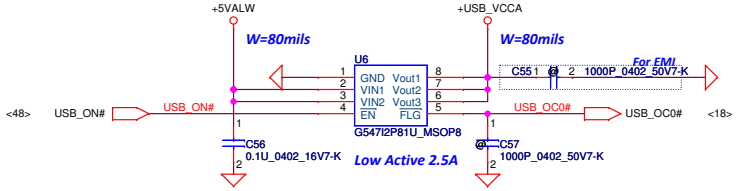
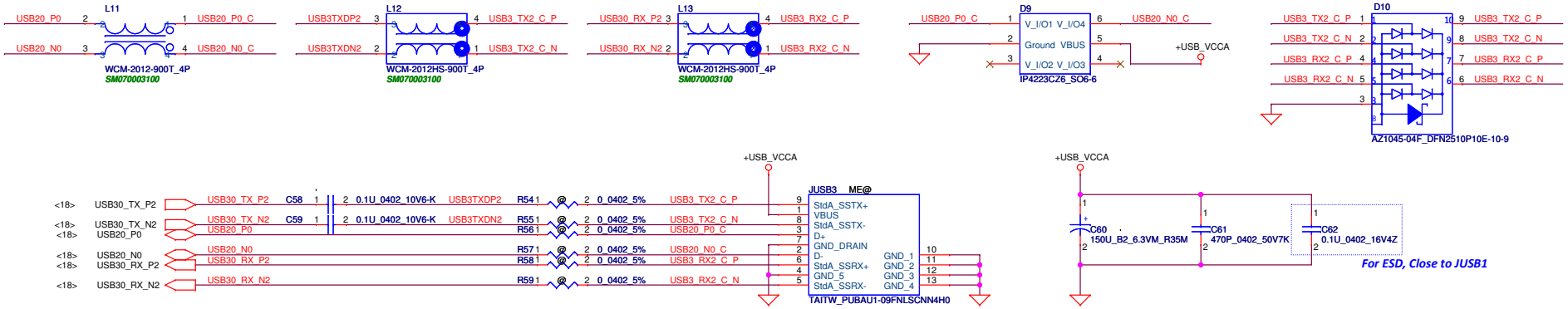
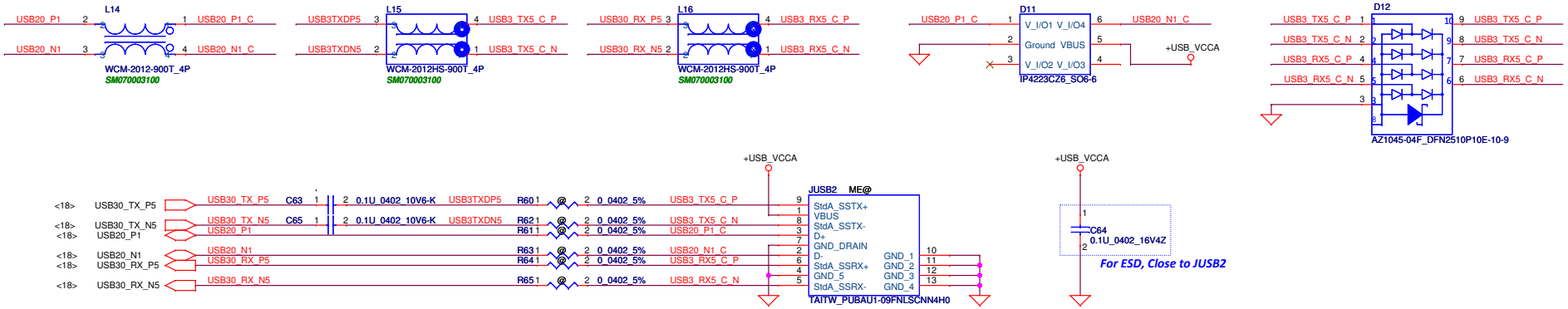


USB30 Front



USB30 Back



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Title: USB30 PORT CONN.

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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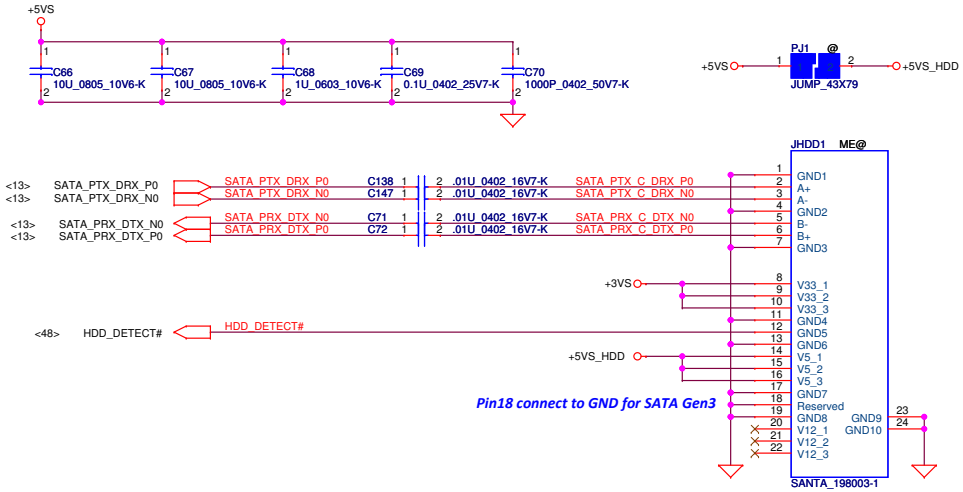
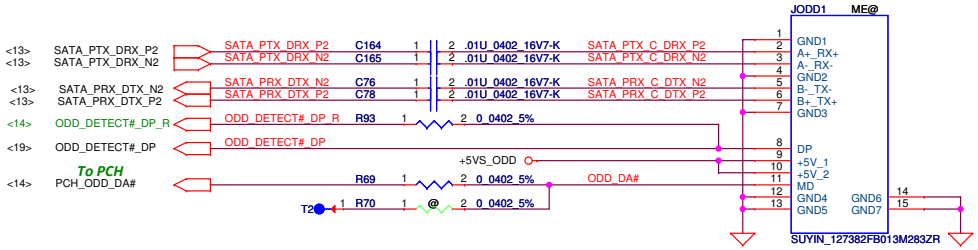
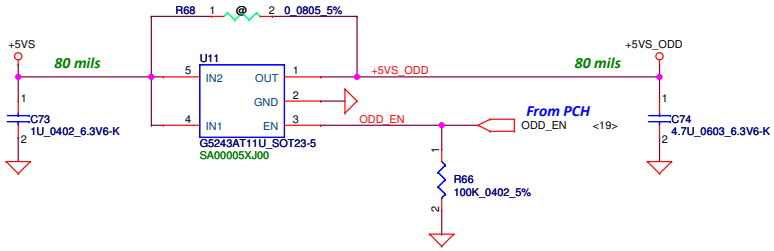
SATA HDD CONN.

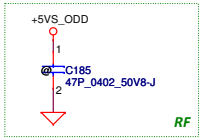


SATA ODD CONN & ODD Power Control



+5VS TO +5VS_ODD





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Title: SATA HDD/ODD CONN.

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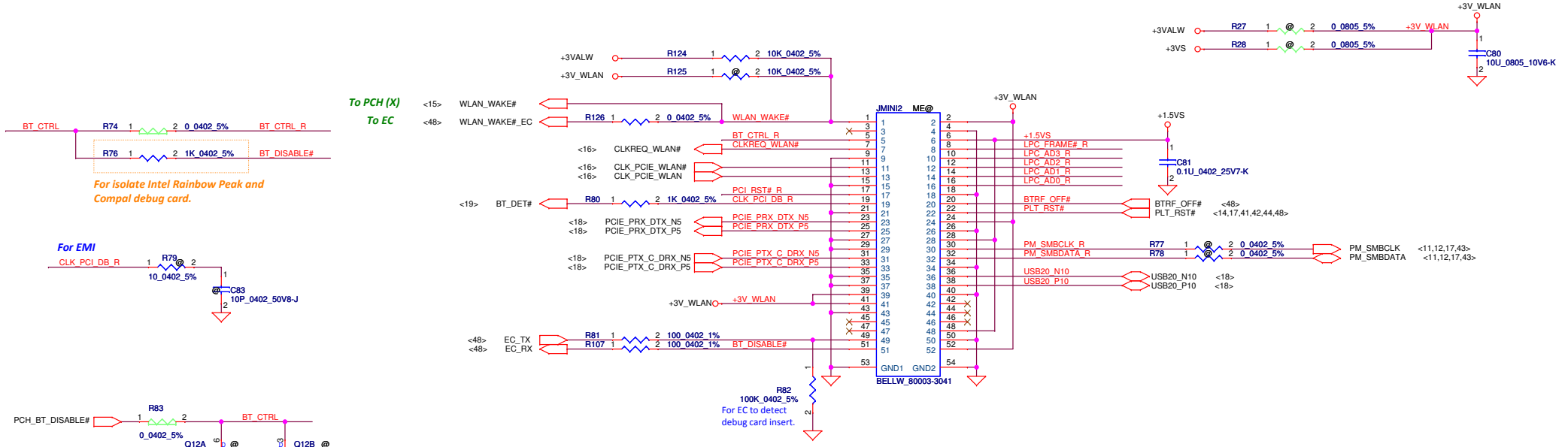
Mini-Express Card(WLAN/WiMAX)



WLAN&BT Combo module circuits

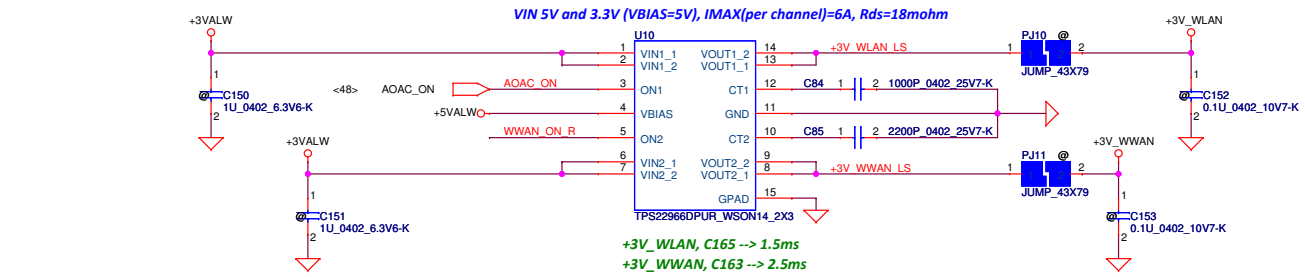
	BT on module Enable	BT on module Disable
* PCH_BT_DISABLE#	H	L
PCH_BT_ON#	L	H

Load Switch

+3VALW To +3V_LAN

+3VALW To +3V_WWAN

1. softstart (RC) will check on EVT PCB
2. if AOAC enable +3V_WLAN always ON
   if AOAC disable +3V_WLAN is same as +3VS



<48,55,61,62> SUSP# — SUSP# R29 0_0402_5%

<19> WWAN_ON — WWAN_ON R30 0_0402_5% — WWAN_ON_R

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME#_R	R86	0_0402_5%	LPC_FRAME#	LPC_FRAME# <17,44,48>
LPC_AD3_R	R87	0_0402_5%	LPC_AD3	LPC_AD3 <17,44,48>
LPC_AD2_R	R88	0_0402_5%	LPC_AD2	LPC_AD2 <17,44,48>
LPC_AD1_R	R89	0_0402_5%	LPC_AD1	LPC_AD1 <17,44,48>
LPC_AD0_R	R91	0_0402_5%	LPC_AD0	LPC_AD0 <17,44,48>
PCI_RST#_R	R92	0_0402_5%	PLT_RST#	
CLK_PCI_DB_R	R106	0_0402_5%	CLK_PCI_DB	CLK_PCI_DB <16>

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Title: **PCIe-WLAN SLOT**

LCFC

Size: Custom | Document Number: **E440 NM-A151** | Rev: 1.0

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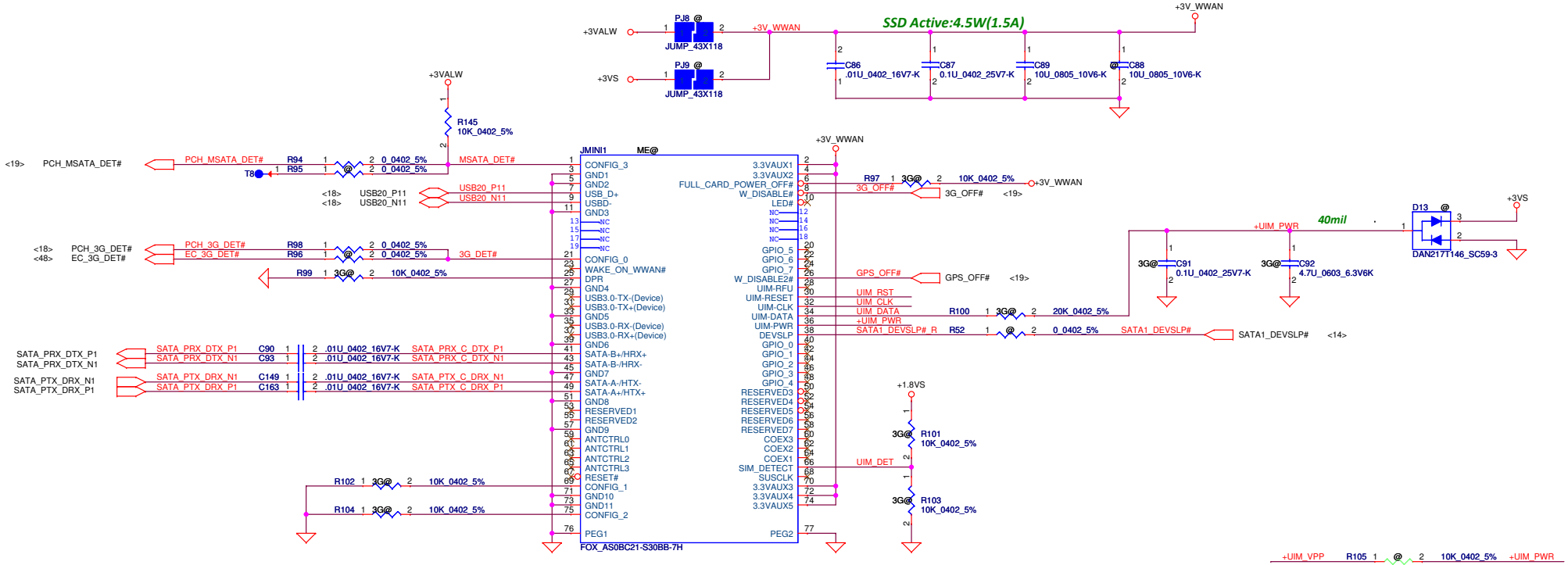
NGFF(SSD) & SIM CARD CONN.



Only for 15"

1. PCH_MSATA_DET# --> +3V_PCH
   EC_MSATA_DET# --> +3VL
2. PCH_3G_DET# --> +3VS
   EC_3G_DET# --> +3VL
   需小心EC漏電到PCH
3. EC don't have GPIO pin for DET# pin as below
   a. PCH_3G_DET#
   b. PCH_MSATA_DET#

NGFF Detect Desc.

	MSATA_DET#	3G_DET#
No Card	1	1
WWAN CARD	1	0
SSD CARD	0	0

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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title	PCIe-WWAN/SIM SLOT		
Size	Document Number		Rev
Custom	E440 NM-A151		1.0
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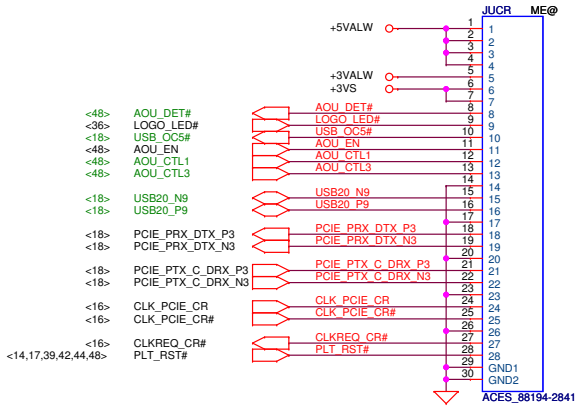
USB2.0, CR & LOGO Board



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Title: PCIe-CR/USB-Charge CONN.

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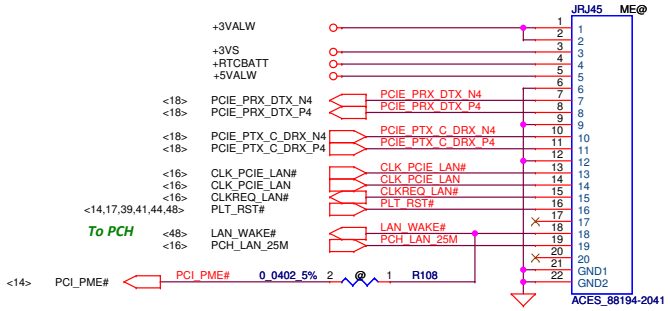
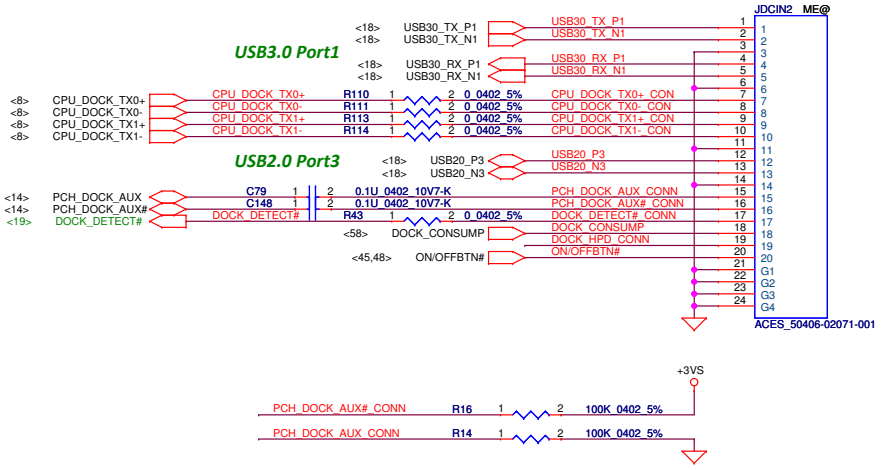
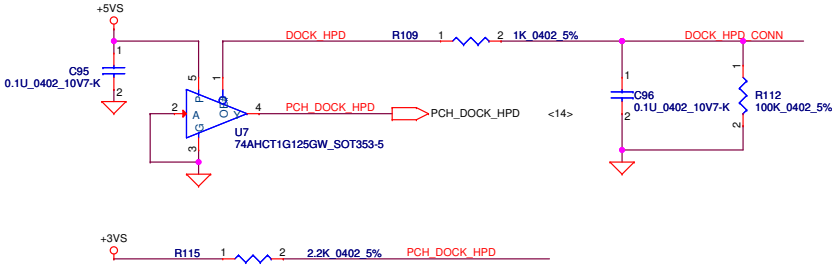
LAN (Port4)
USB3.0/2.0 (Port1/3)
DP(DDIC)

LAN CONN. (FFC)



DCIN CONN. (Coaxial)





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Title: PCIe-RJ45/RTC/Docking CON

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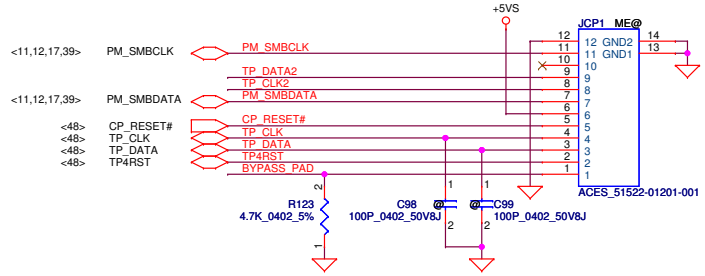
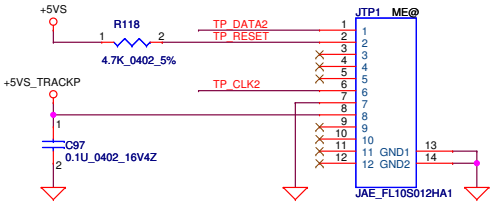
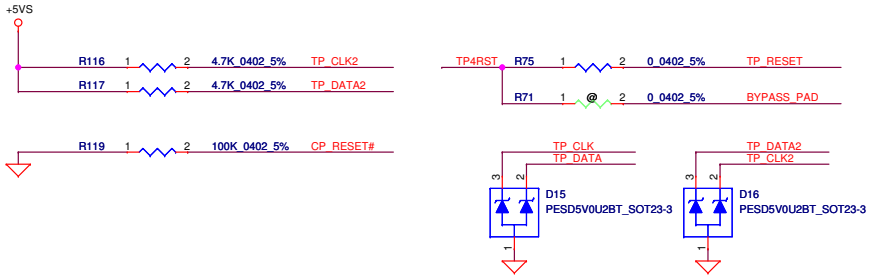
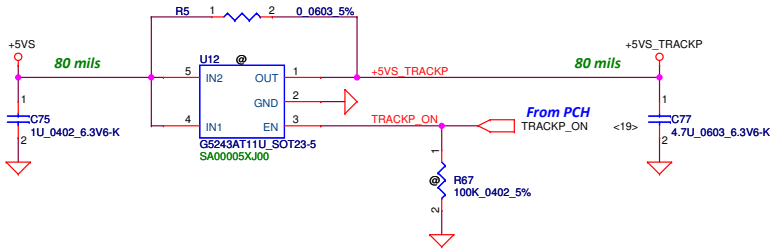
Click Pad



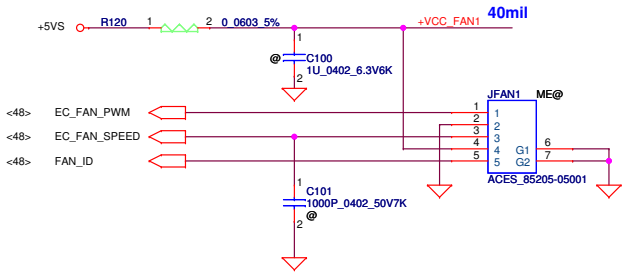
Track point







FAN CONN.



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Title: CP/TP/FAN CONN.

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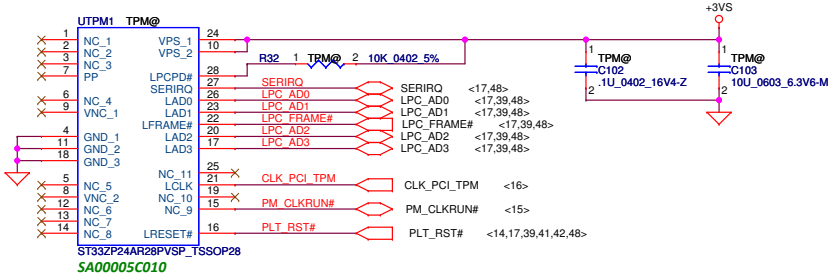
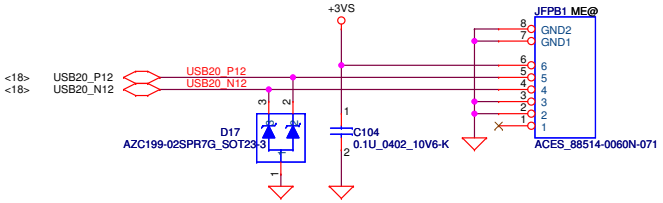
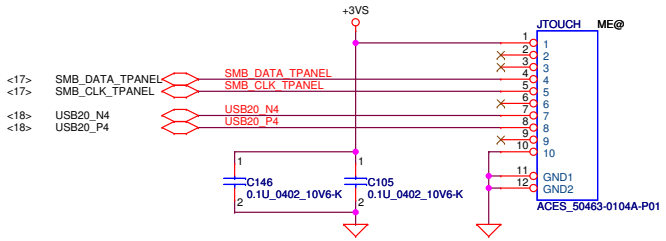
TPM IC



FingerPrint CONN.



Touch Panel CONN.



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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: TPM/TPanel/FP CONN.

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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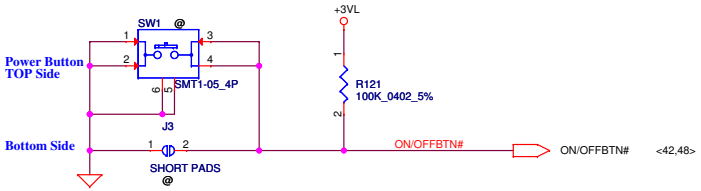
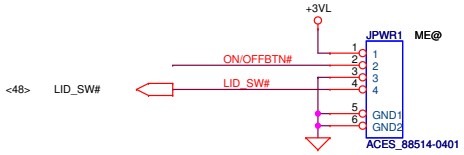
PWR BTN/LID SW CONN.

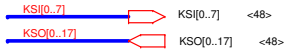
1. Power Button/B link to Function/B Conn. 10pin
2. Lid Switch

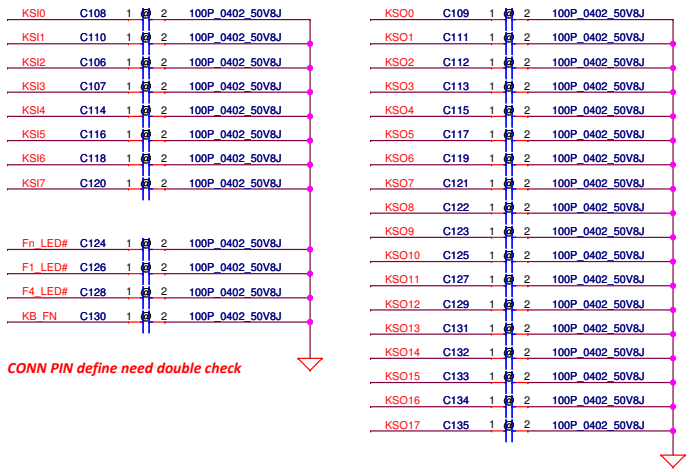
ON/OFF switch



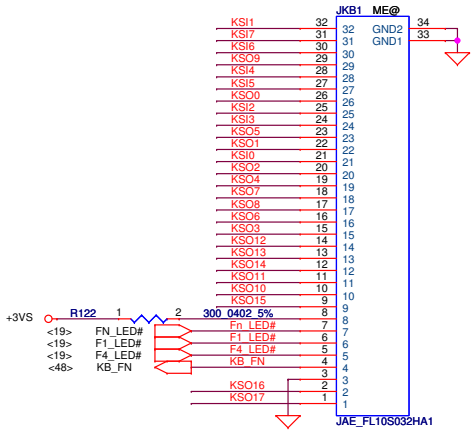


KeyBoard CONN.(14")





CONN PIN define need double check



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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: KB/PWR BTN CONN.

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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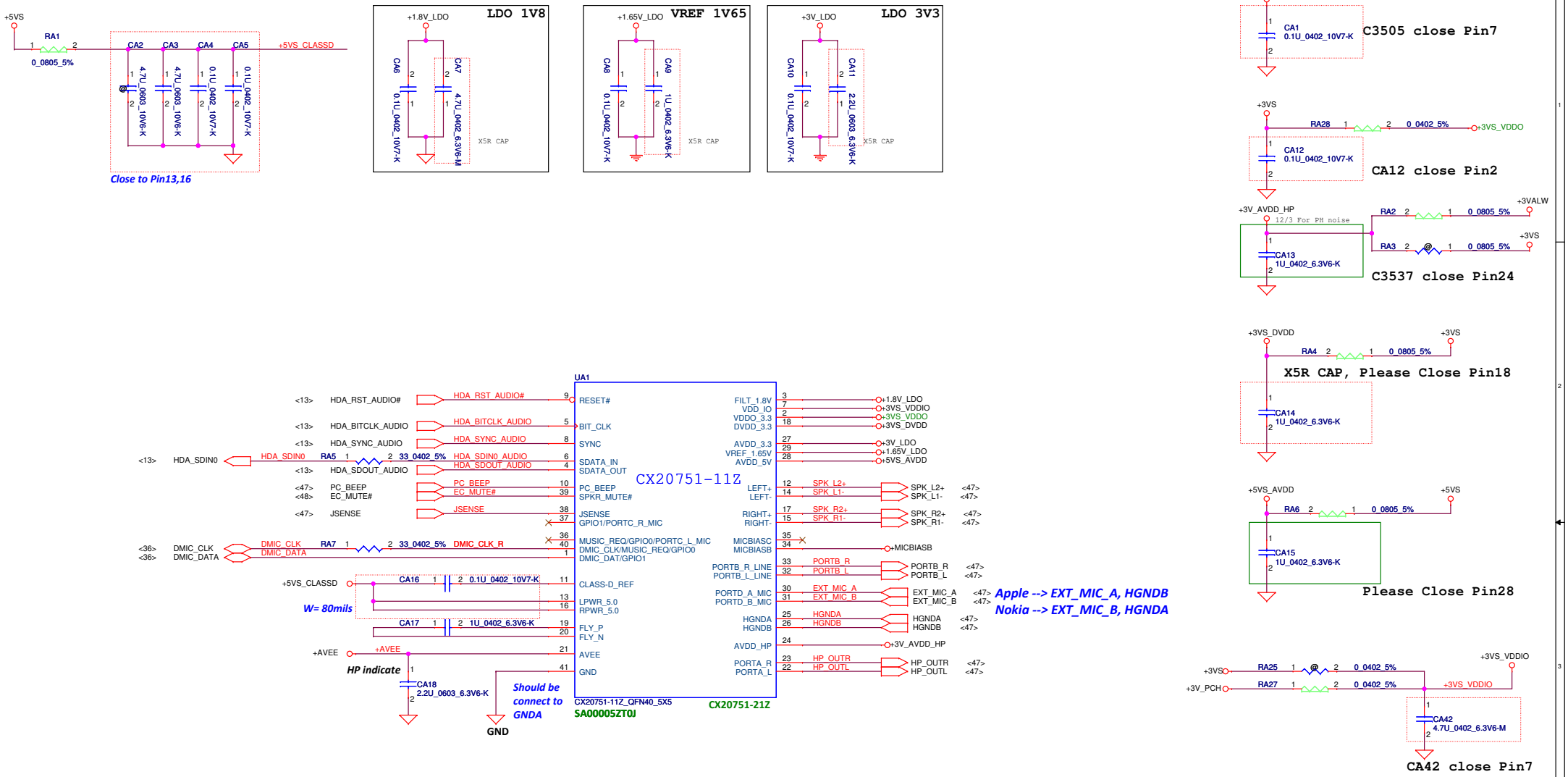

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: HDA-CX20751-CX

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

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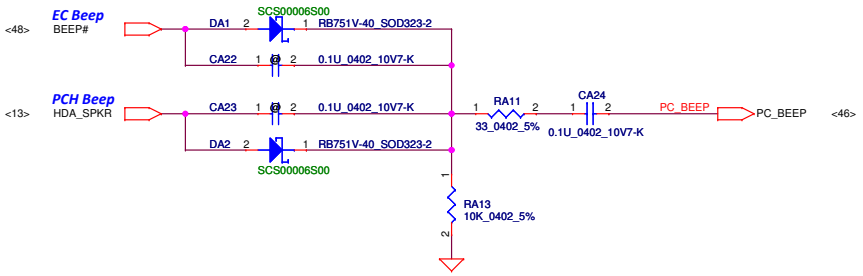
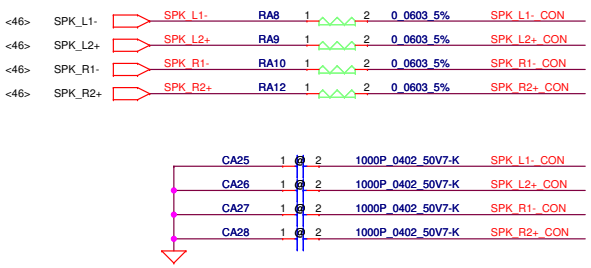
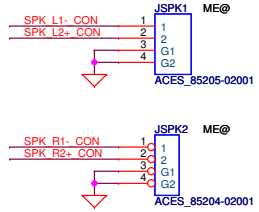
PC Beep



Speaker OUT

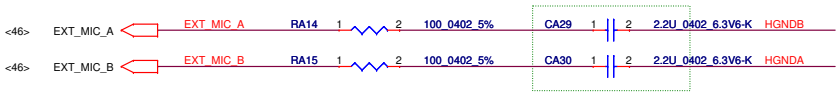


SPK CONN.



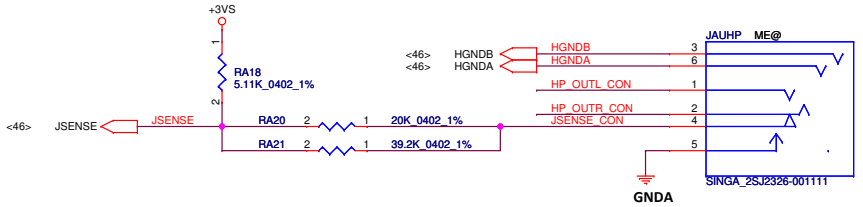
EXT. MIC/LINE IN

Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA

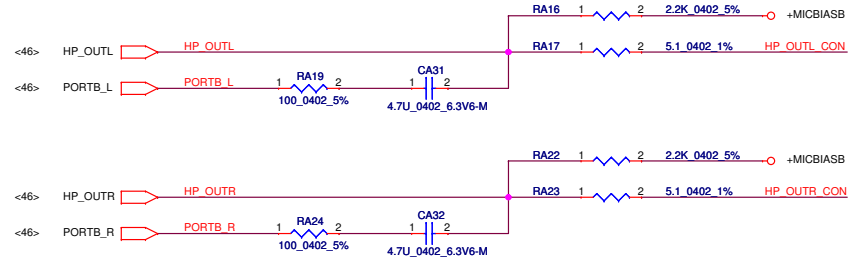


Changed CA29 & CA30 from 1uF to 2.2uF/X5R to meet Port-D(headset-Mic) THD+N <= -65 dB

Audio Jack

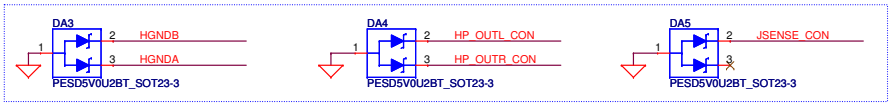


HeadPhone/LINE OUT

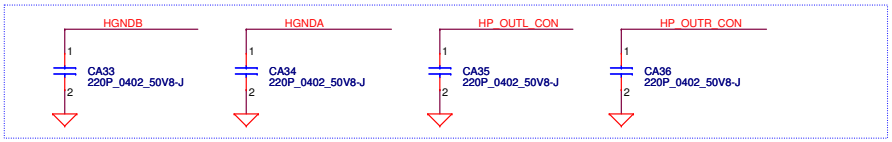


CA31, CA32 change to 4.7U for Quality requirement

ESD Diode, close to JAUHP



EMI, close to JAUHP



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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: HDA-HP/EXT MIC/SPK CO

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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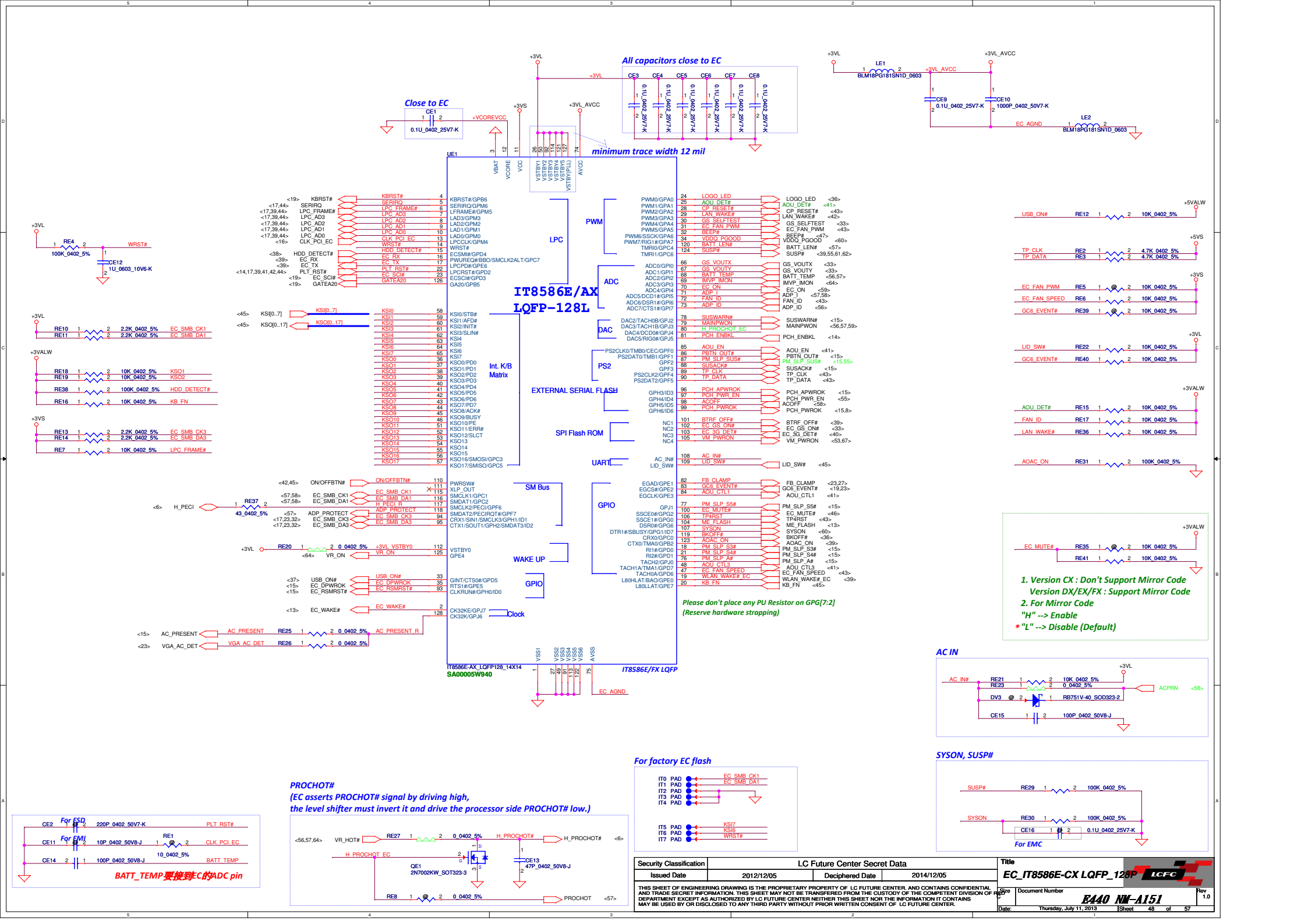

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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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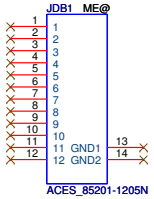
Title: EC_IT8586E-CX LQFP_128P

Size: C | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 48 of 57



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

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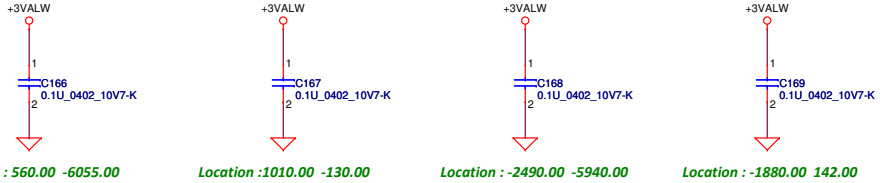
Title: **BLANK**

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

Date: Thursday, July 11, 2013 Sheet 49 of 57

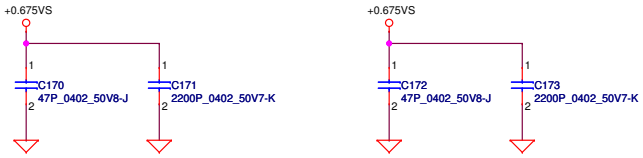


Location : 560.00 -6055.00

Location :1010.00 -130.00

Location : -2490.00 -5940.00

Location : -1880.00 142.00



close to JDDR3L and Pin .203/.204
1. 47P --> Location : -3885,-5914 (BOT)
2. 2200P --> Location : -3885,-5877 (BOT)

close to JDDR3H and Pin .203/.204
1. 47P --> Location : -4198,-5416 (TOP)
2. 2200P --> Location : -4204,-5384 (Top)

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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: **BLANK**

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: ***BLANK***

LCFC

Size	Document Number	Rev
Custom	*E440 NM-A151*	1.0

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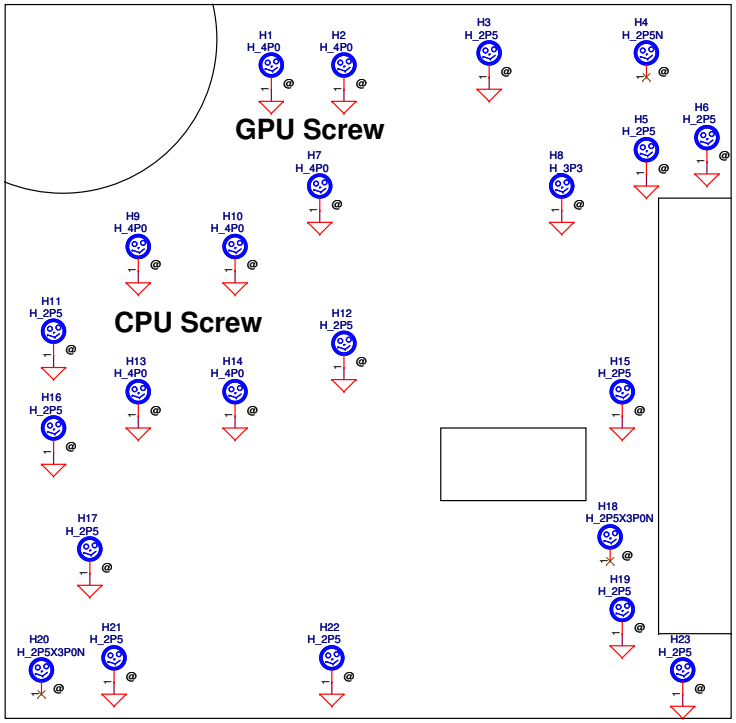
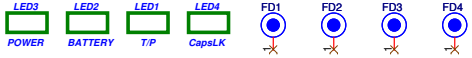
Screw Hole



PCB Fedical Mark PAD



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: *LED*

Size	Document Number	Rev
Custom	*E440 NM-A151*	1.0

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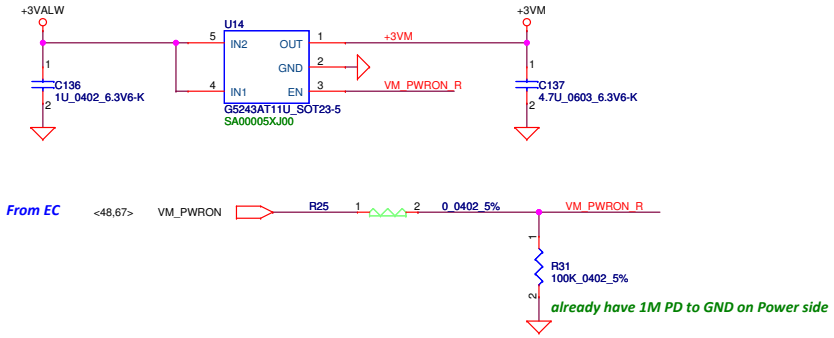
+3VALW to +3VM

FOR SBA Function POWER(always mount)



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

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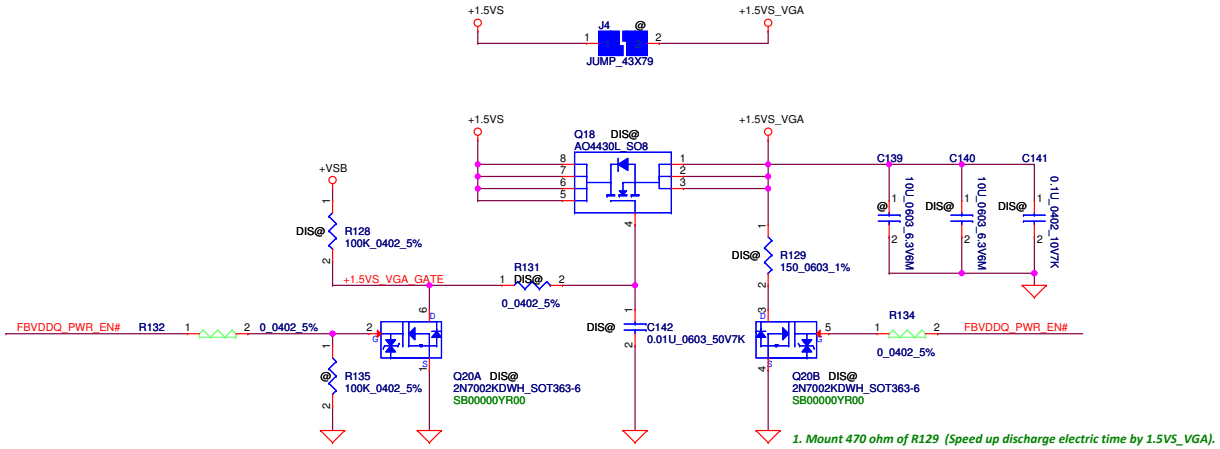
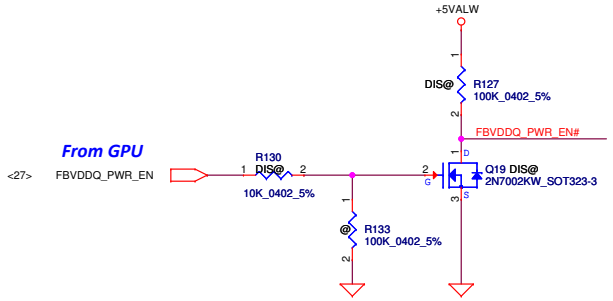
Title: ONOFF SW/ PWR-B CONN/ ISPD

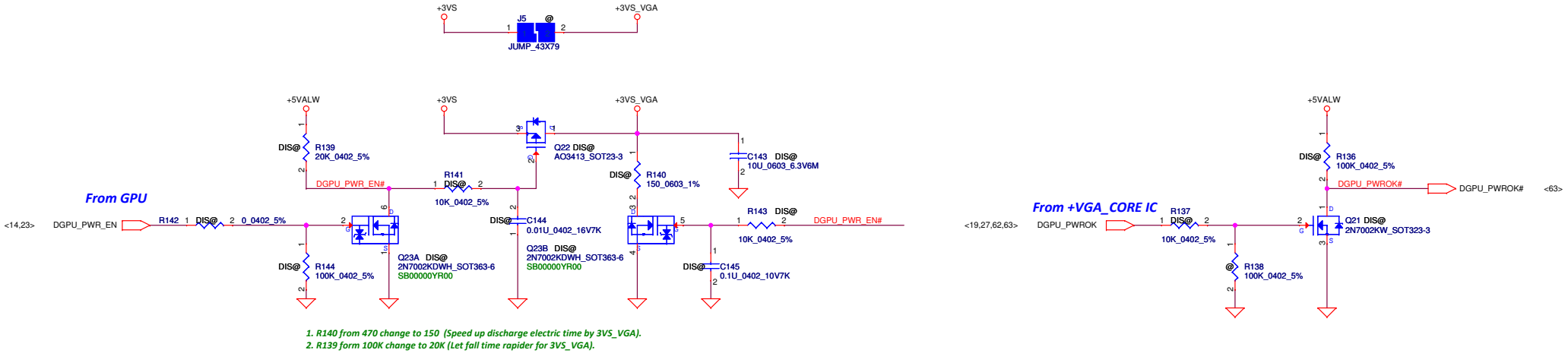
Size: Custom	Document Number: JITR1_LA-4141P E540 NM-A161	Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 53 of 57	

+1.5V to +1.5VS_VGA





+3VS to +3VS_VGA



Power Up -->

+3VS_VGA (En:DGPU_PWR_EN)

+VGA_CORE (En:NVDD_PWR_EN, POK:DGPU_PWROK)

+1.5VS_VGA (En:FBVDDQ_PWR_EN# = FB_CLAMP and DGPU_PWROK)

+1.05VS_VGA (En:DGPU_PWROK#)

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Issued Date	2012/12/05	Deciphered Date	2014/12/05

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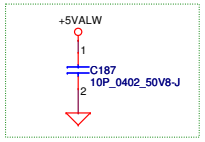
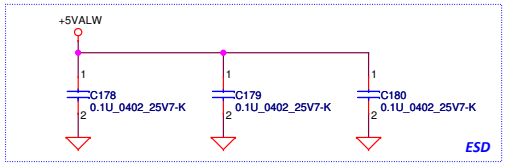
Title	DOCKING USB30/DP		
Size	Document Number		Rev
Custom	E440 NM-A151		1.0
Date:	Thursday, July 11, 2013	Sheet	54 of 57

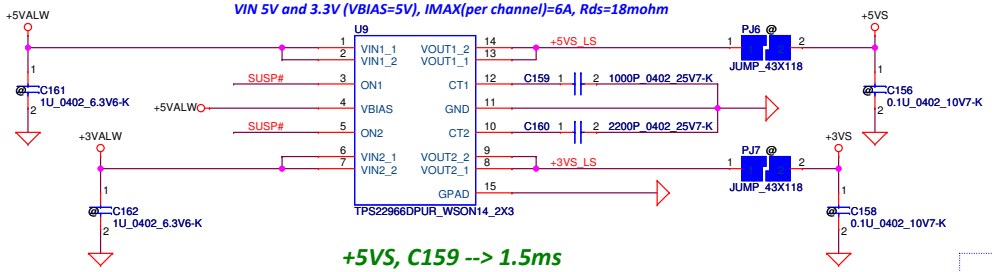
Load Switch
+5VALW To +5VS
+3VALW To +3VS

CPI, 14" only

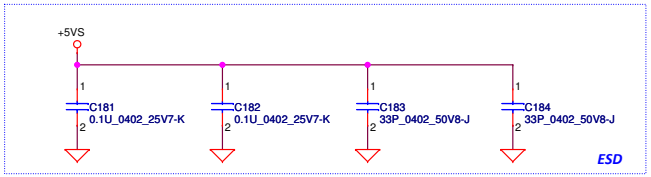




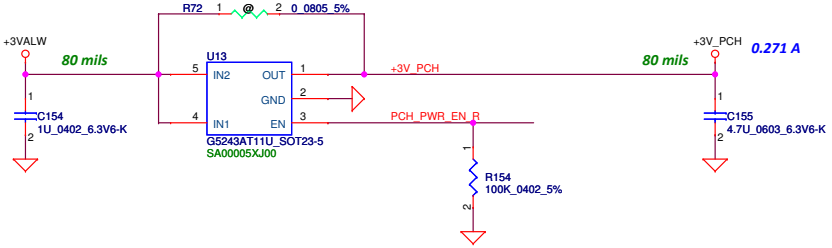
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=18mohm



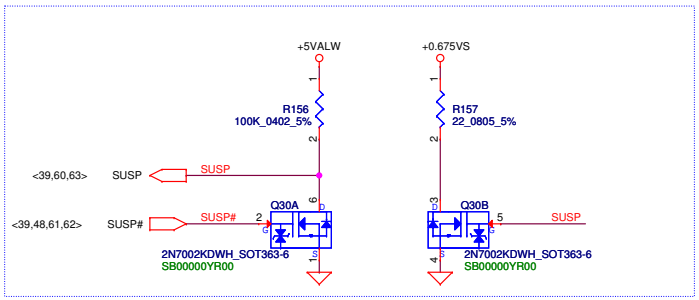
+5VS, C159 --> 1.5ms
+3VS, C160 --> 2.5ms



+3VALW To +3V_PCH



For DisCharge



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: DC V TO V/VS INTERFACE

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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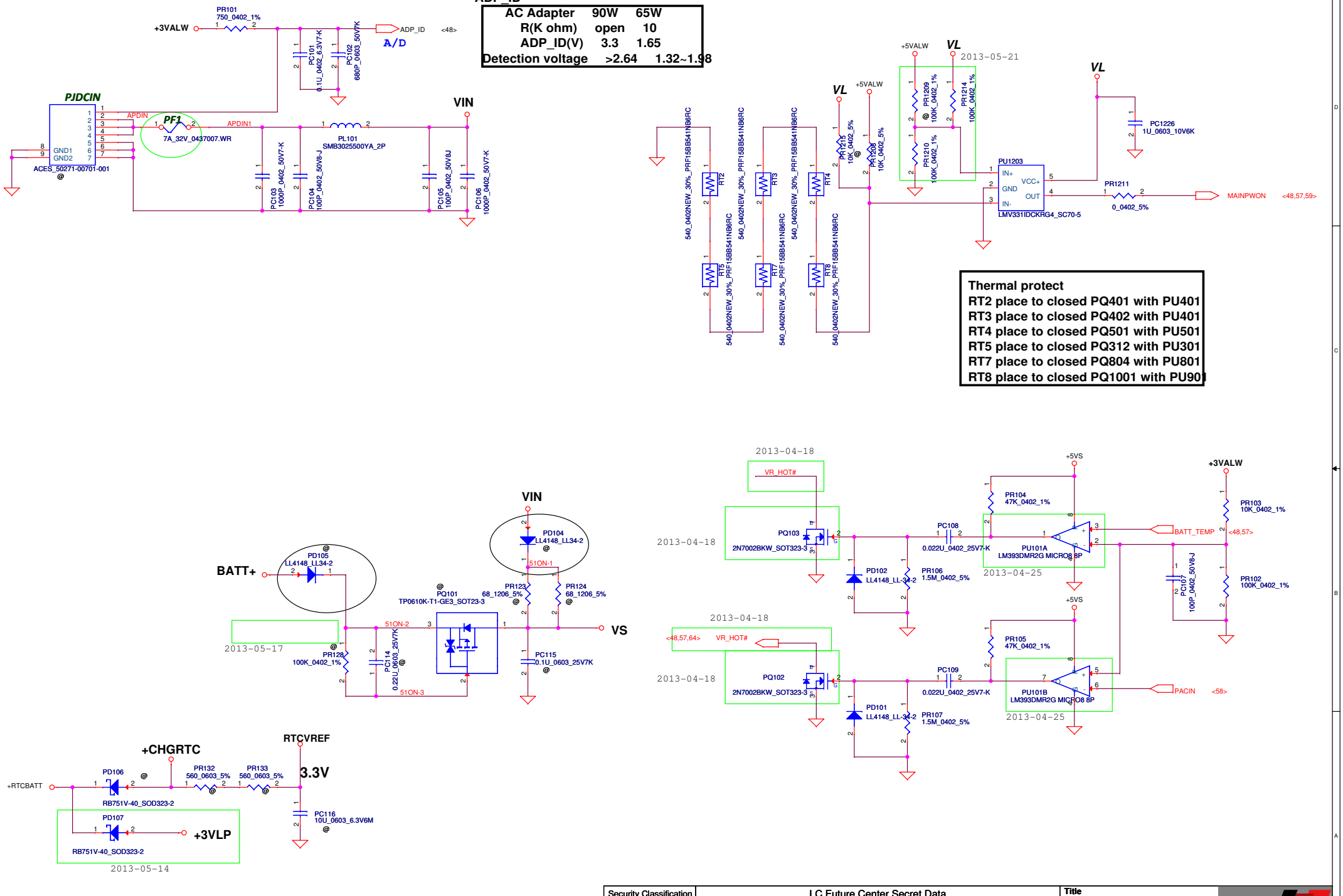

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: PWR-DCIN / Vin Detector

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

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PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

JBATT1
SUYIN_200082GR007M211ZR
2011_0823
change 9P JBATT1

VMB2
PF201 12A_65V_451012MRL
EC_SMCA
EC_SMDA
VMB
PL201 SMB3025500YA_2P
PC201 1000P_0402_50V7K
PC202 0.01U_0402_25V7K
PR223 0.01_1206_1%
BATT+
DCP
DCN
PR202 100_0402_1%
PR201 100_0402_1%
PESD5V0U2BT_SOT23-3 PD805
EC_SMB_CK1 <48,58>
EC_SMB_DA1 <48,58>
PR203 100K_0402_1%
+3VALW
A/D
PR204 750_0402_5% <BOM Structure>
BATT_TEMP <48,56>
PESD5V0U2BT_SOT23-3 PD806

VL
PC203 0.1U_0603_16V7K
+3VS
PR209 100K_0402_1%
<48,56,64> VR_HOT#
PQ201 2N7002BKW_SOT323-3
ADP_OCP_1
PR212 @ 0_0402_5%
<48> PROCHOT
OTP_N_003
PU201 G718TM1U_SOT23-8
VCC TMSNS1
GND RHYST1
OT1 TMSNS2
OT2 RHYST2
OTP_N_002
ADP_OCP_2
Turbo_V_1
PR210 27.4K_0402_1%
PR213 0_0402_5%
MAINPWON <48,56,59>
<48,58> ADP_I
PR205 4.42K_0402_1%
PR227 2.1K_0402_1%
PQ206 2N7002BKW_SOT323-3
ADP_PROTECT <48>
PR206 12.7K_0402_1%
PR207 30K_0402_1%
NTC_V_1
+3VLP
PR208 499K_0402_1%
PR230 0_0402_5%
+3VALW
PR228 0_0402_5%
PR229
PR211 10K_0402_1%
PR231 47K_0402_1%
PR232 47K_0402_1%
PH201 NCP15WF104J03RC
100K_0402_1%
@ T135 Turbo_V
@ T136 NTC_V

2013-04-18
2013-05-23
2013-07-08
2013-07-08
2013-07-08

PR248 0_0402_5%
VCP
PU102 INA199A1DCKR_SC70-6
REF OUT
GND IN-
V+ IN+
PR247 150K_0402_1%
PR246 100K_0402_1%

2011_0731 add circuit for battery learning function
2011_1119 change circuit to unmount from mount

P2
VMB2
PR224 255K_0402_1%
PR219 10K_0402_1%
PR221 150K_0402_1%<BOM Structure>
PC207 .01U_0402_25V7-K
PR218 10M_0402_5%
PU202A LM393DMR2G MICRO8 8P
2013-04-25
+3VLP
PR222 100K_0402_1%
+3VALW
PR220 100K_0402_1%
PQ204 2N7002BKW_SOT323-3
BATT_OUT <58>
PR225 10K_0402_1%
PR226 100K_0402_1%
<48> BATT_LEN#
PQ205 2N7002BKW_SOT323-3
2013-04-18
2013-04-18

+1.05VS
PC214 0.1U_0402_25V6
PR250 1K_0402_1%
PR251 1K_0402_1%
PC212 0.1U_0402_25V6
PC213 0.1U_0402_25V6
PR249 10K_0402_1%
PC215 0.1U_0402_25V6
2013-05-15
PR255 0_0402_5%
PR254 0_0402_5%
VR_HOT#
MAINPWON
PVIN2 PVIN1 SVIN1 PGND LX1 LX2 LX3 FB NC
PU203 RT9553
PR257 13K_0402_1%
PR260 20K_0402_1%
PR261 374K_0402_1%
PR252 10K_0402_1%
PR253 10K_0402_1%
PR259 20K_0402_1%
PR258 10K_0402_1%
+5VALW
PR256 2.2_0402_5%
PC218 1U_0402_25V6

+3VS
PR237 100K_0402_1%
PR238 100K_0402_1%
100P_0402_50V8-J PC209
+5VS
PR234 221K_0402_1%
PR235 1.78M_0402_1%
PR236 20K_0402_1%
VCP
PU1204A LM393DMR2G MICRO8 8P
220P_0402_50V7-K PC208
2013-04-25
PR233 0_0402_5% VR_HOT#
2013-04-18
PQ207 2N7002BKW_SOT323-3

Battery Protection Circuit for Turbo Mode

+3VS
PR243 150K_0402_1%
PR244 84.5K_0402_1%
100P_0402_50V8-J PC211
Turbo_V_1
+5VS
PR242 221K_0402_1%
PR239 1.78M_0402_1%
PR240 20K_0402_1%
PR245 10K_0402_1%
PU1204B LM393DMR2G MICRO8 8P
220P_0402_50V7-K PC210
2013-04-25
PR241 0_0402_5% VR_HOT#
2013-04-18
PQ208 2N7002BKW_SOT323-3
2013-07-01

Adaptor Protection Circuit for Turbo Mode

PQ202 TP0610K-T1-GE3_SOT23-3
B+
+VSBP
PC205 0.1U_0603_25V7K
PR214 100K_0402_1%
PC204 0.22U_0603_25V7K
PR215 22K_0402_1%
PJ201 @JUMP_43X39
+VSBP
+VSB
VL
PR216 100K_0402_1%
PR217 1K_0402_1%
<59> SPOK
PQ203 2N7002BKW_SOT323-3
2013-04-18
PC206 1U_0402_10V6K

2011_1005 PQ105 change
form SB000006800(2N7002W T/R7 1N SOT-323)
to SB000009Q80(2N7002KW 1N SOT323-3)

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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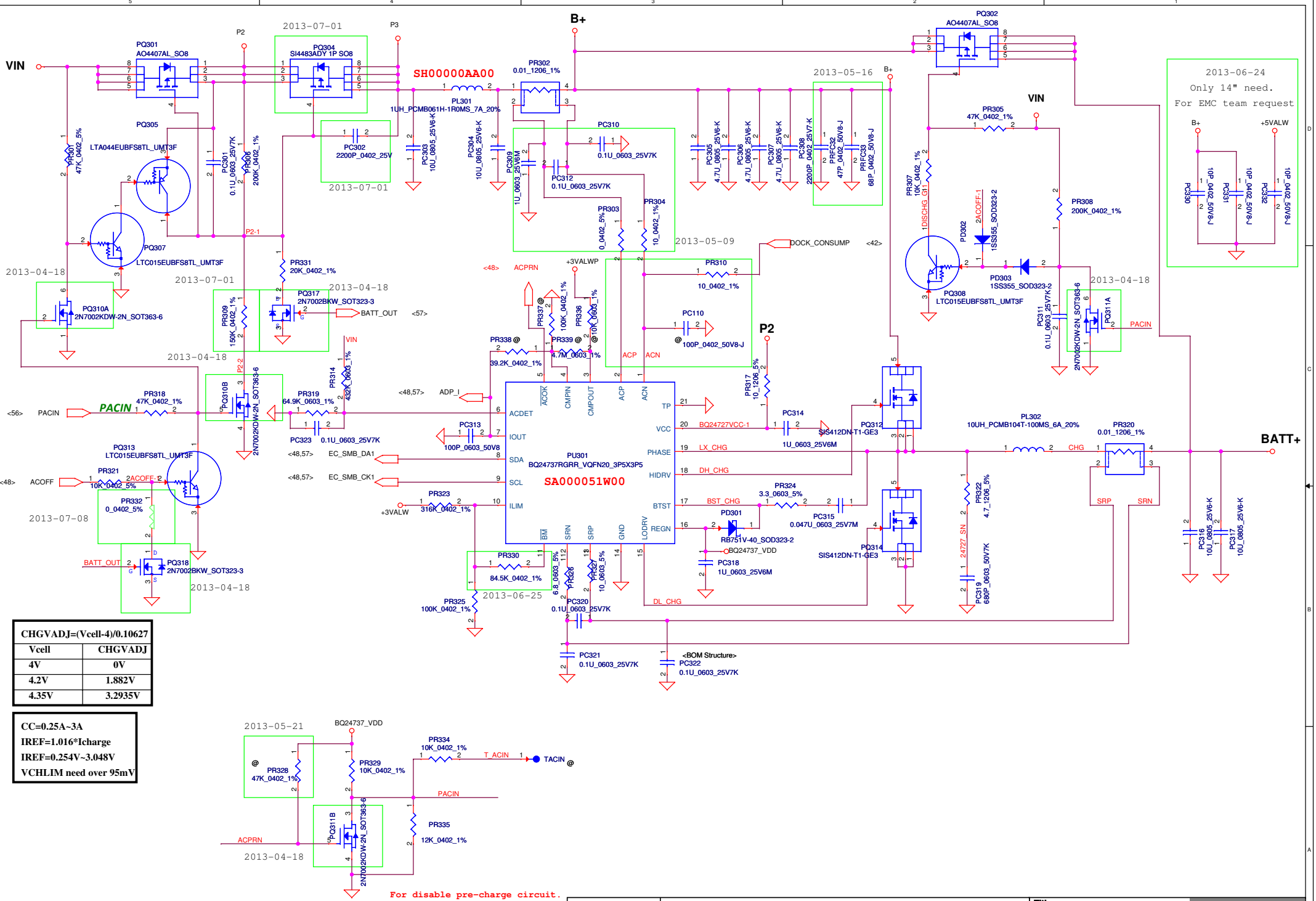
Title: PWR-BATTERY CONN/OTP
Size: Custom
Document Number: E440 NM-A151
Rev: 1.0
Date: Thursday, July 11, 2013
Sheet 57 of 69



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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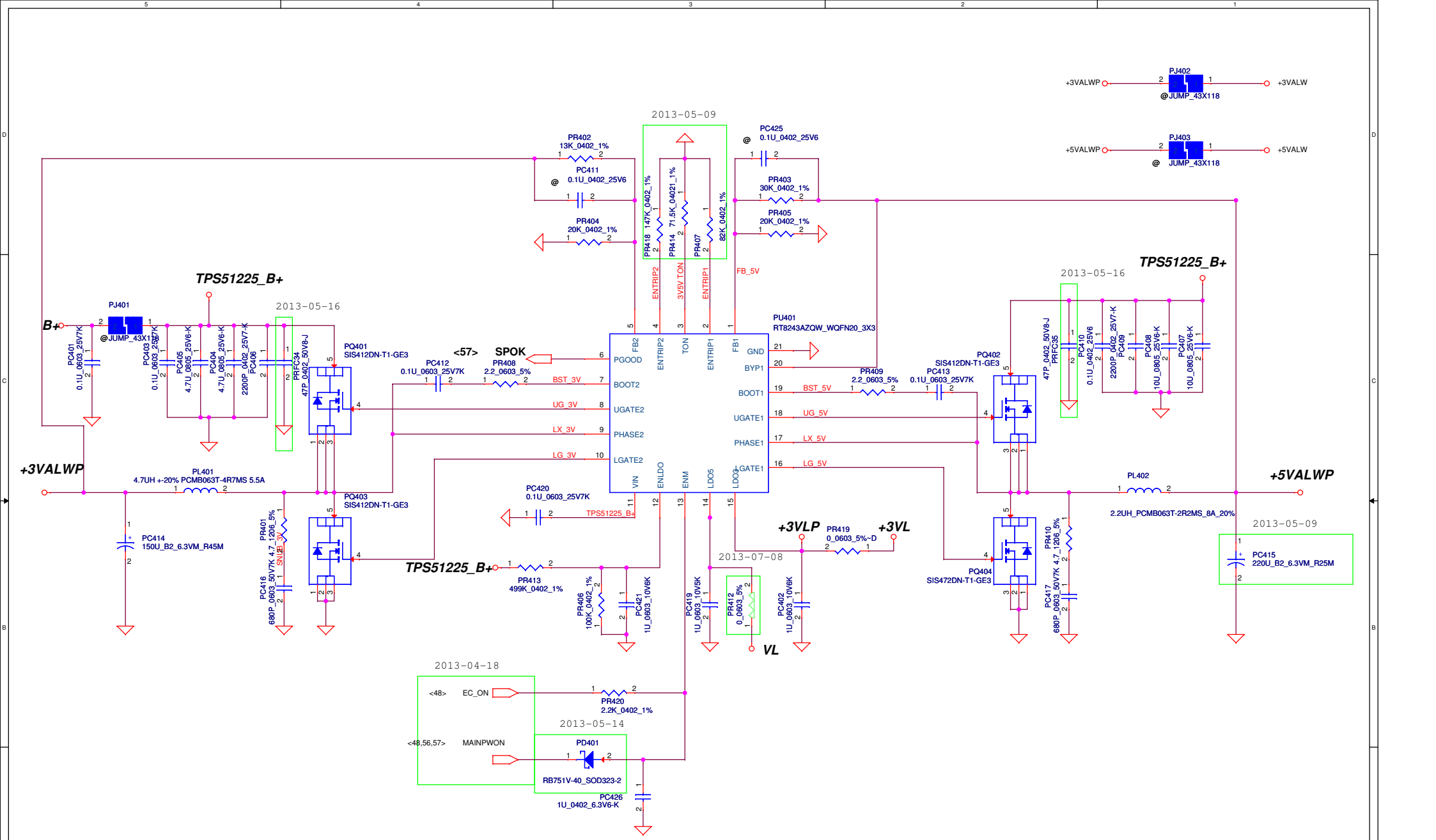
Title: PWR-CHARGER-BQ24737

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 58 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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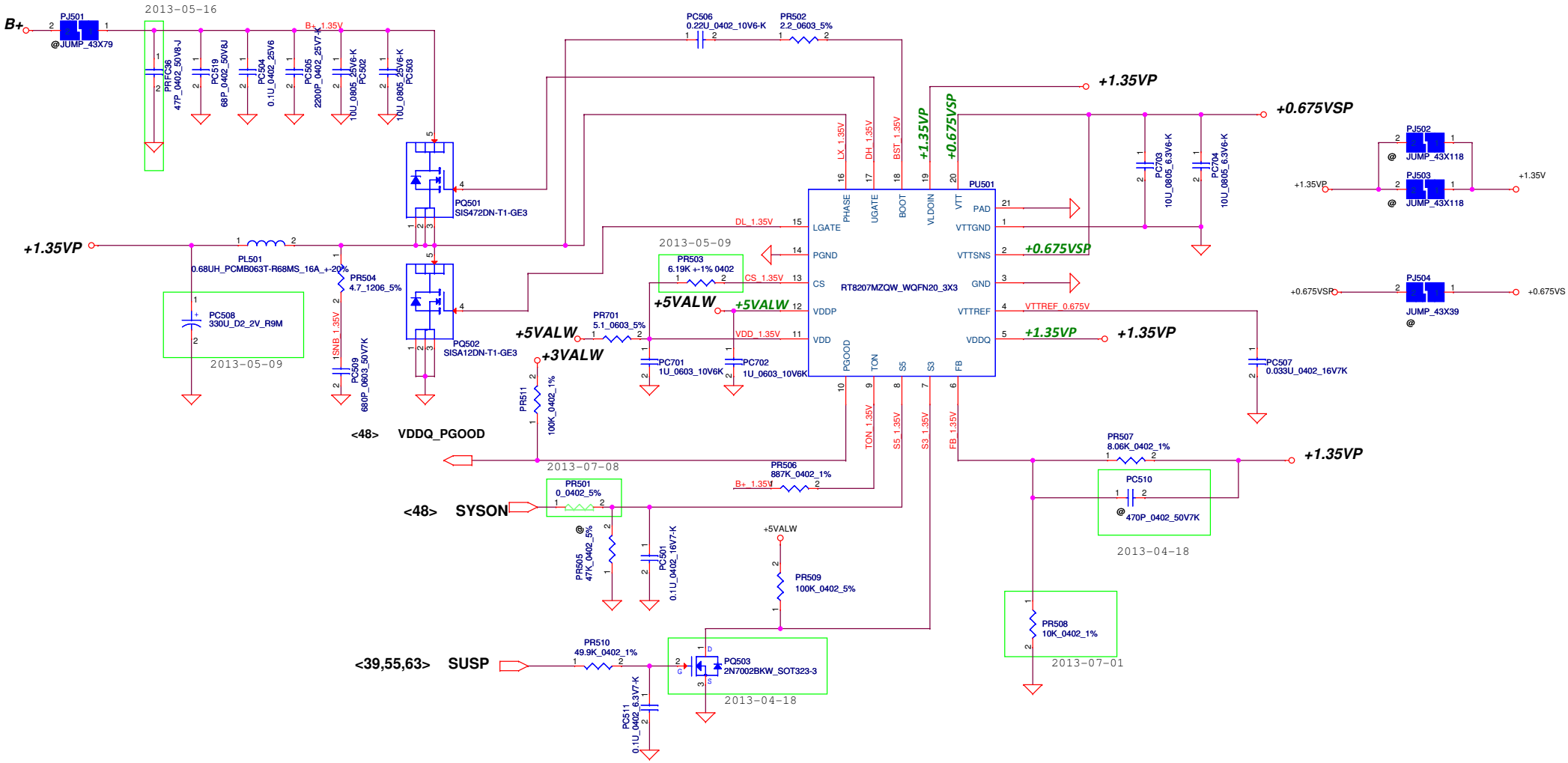
Title	PWR-3VALWP/5VALWP		
Size: Custom	Document Number: E440 NM-A151		Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 59 of 69		



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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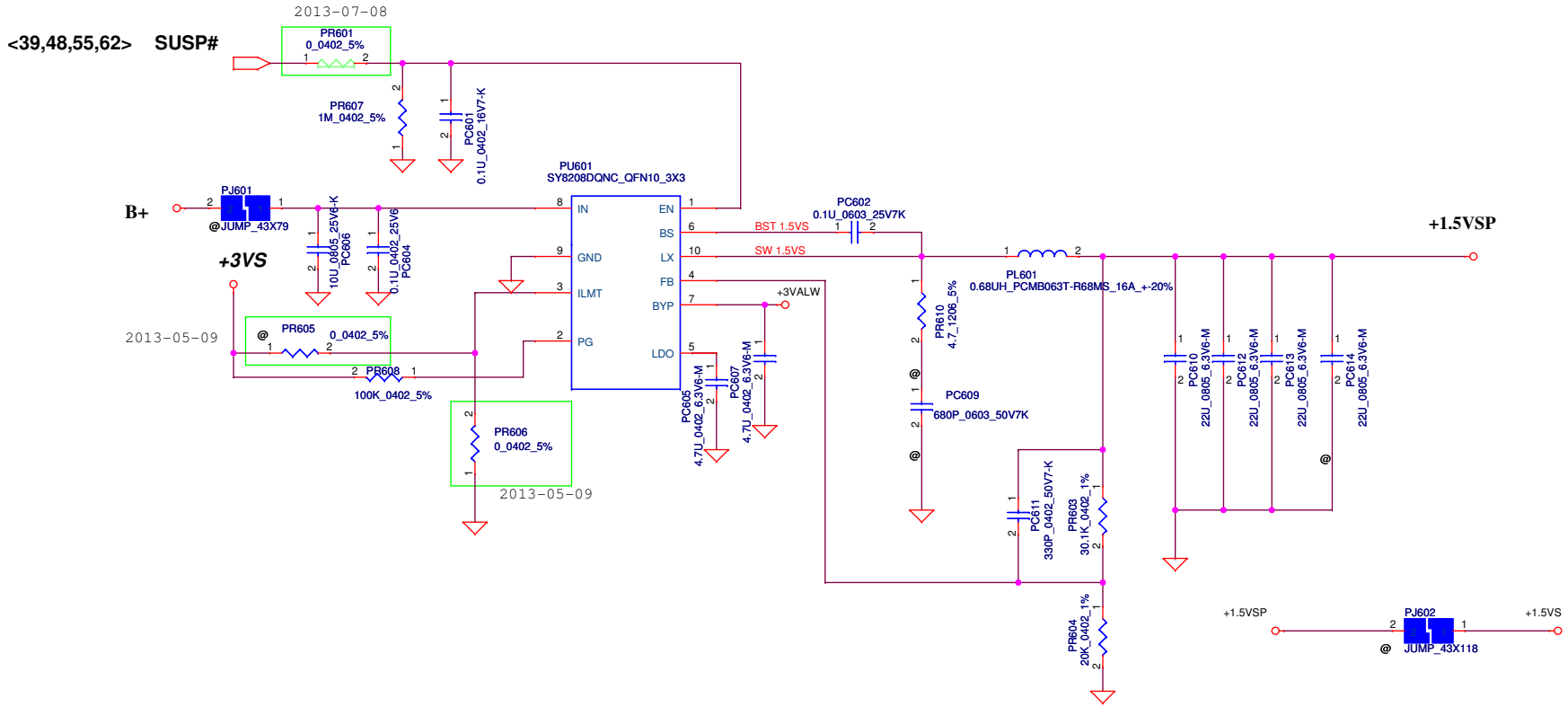
Title	PWR-+1.35VP/+0.675VSP		
Size: Custom	Document Number: E440 NM-A151		Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 60 of 69		



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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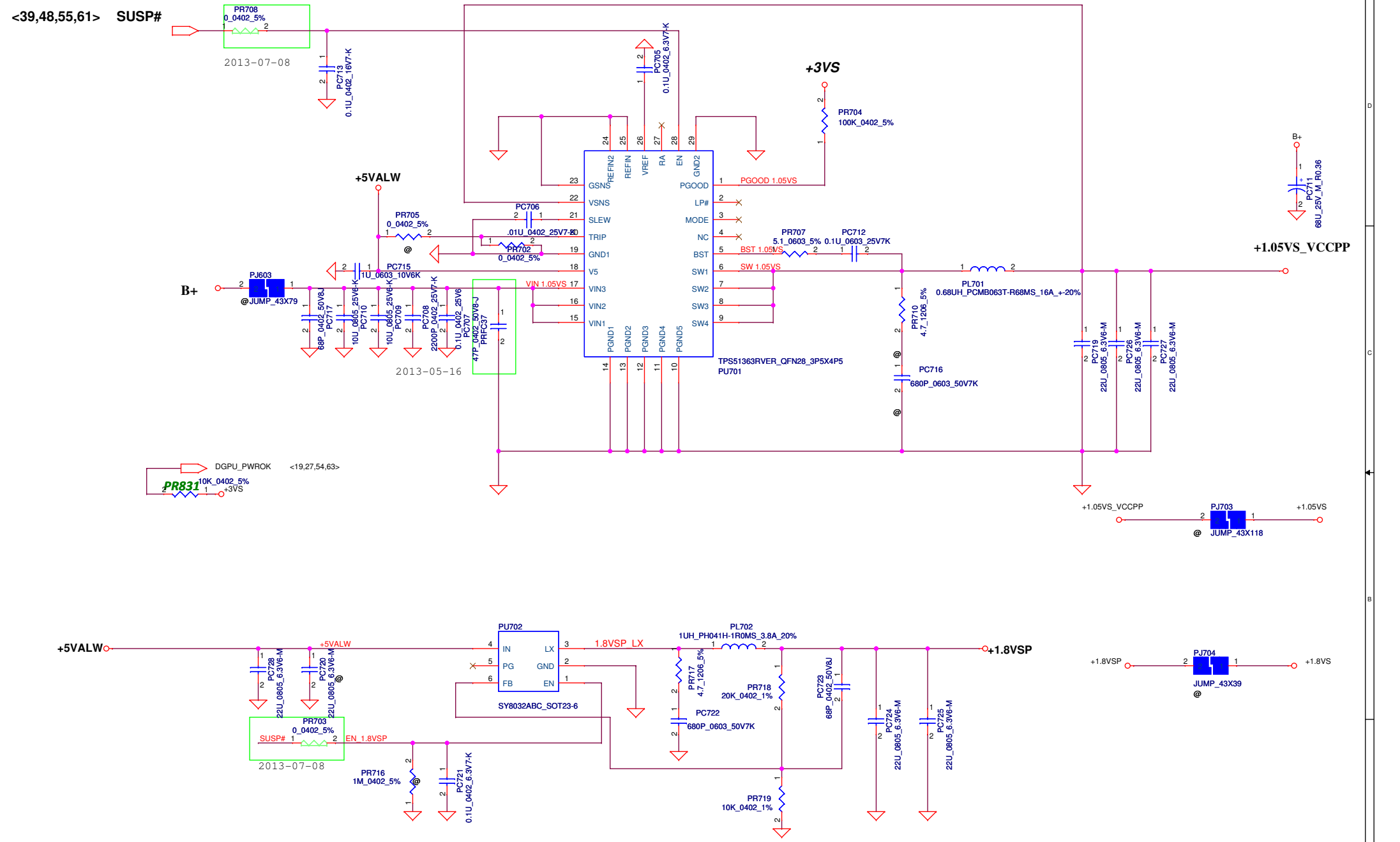
Title: PWR-+1.5VSP

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

Date: Thursday, July 11, 2013 Sheet 61 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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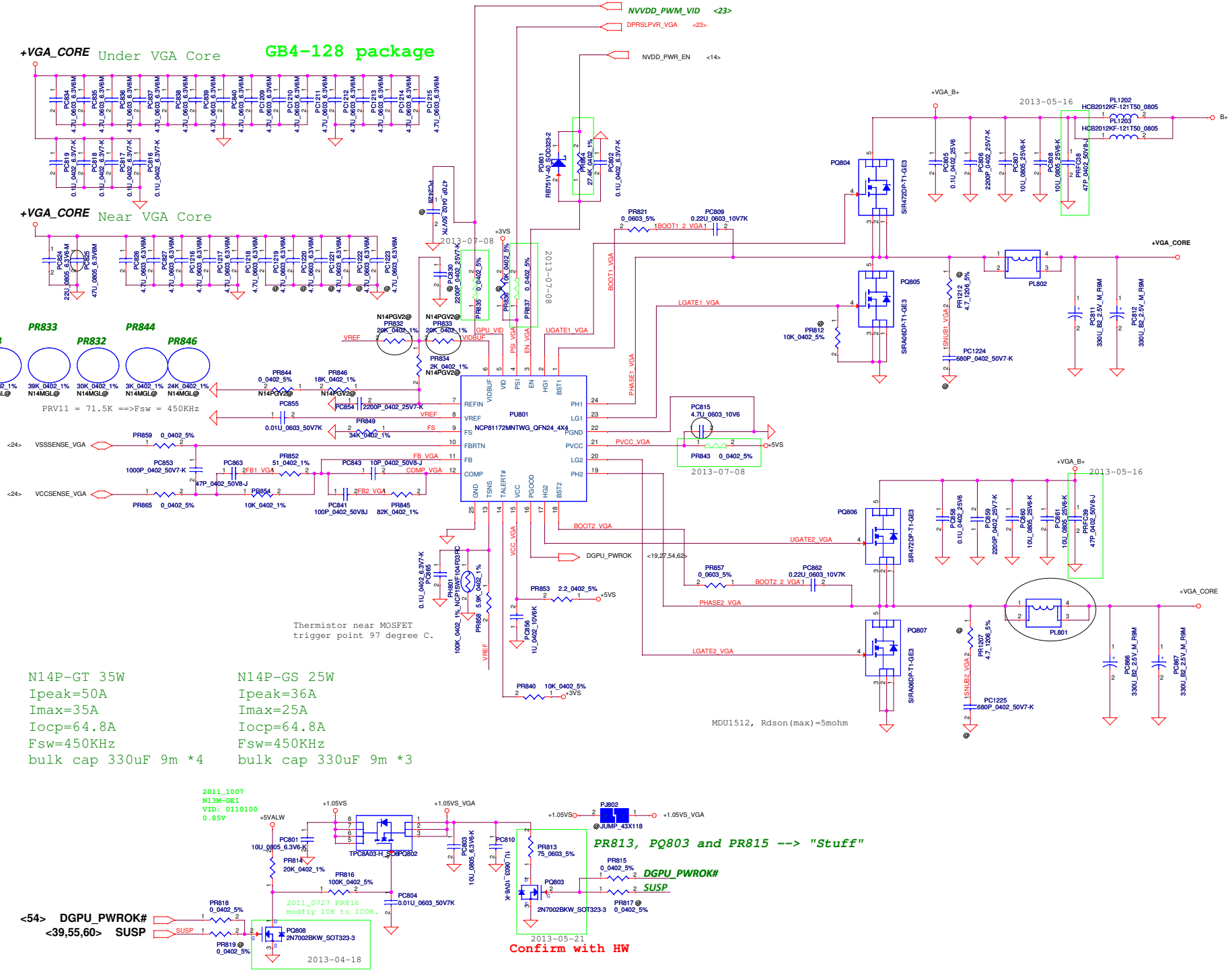
Title: PWR-+1.05VS_VCCPP/+1.8VSP

Size	Document Number	Rev
Custom	E440 NM-A151	1.0
Date: Thursday, July 11, 2013	Sheet 62 of 69	



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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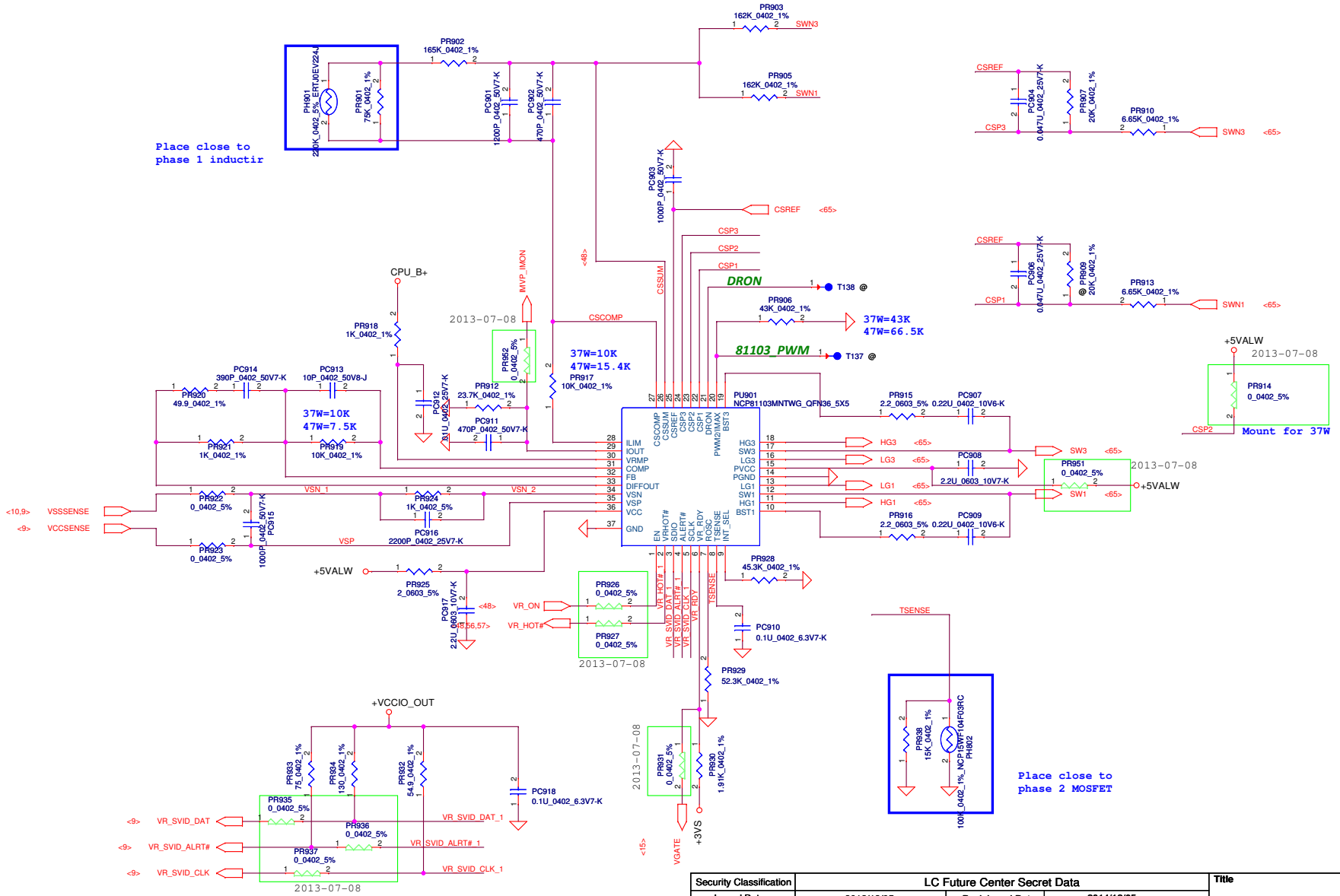
Title: PWR-VGA_COREP-ISL62883

Size: | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 63 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

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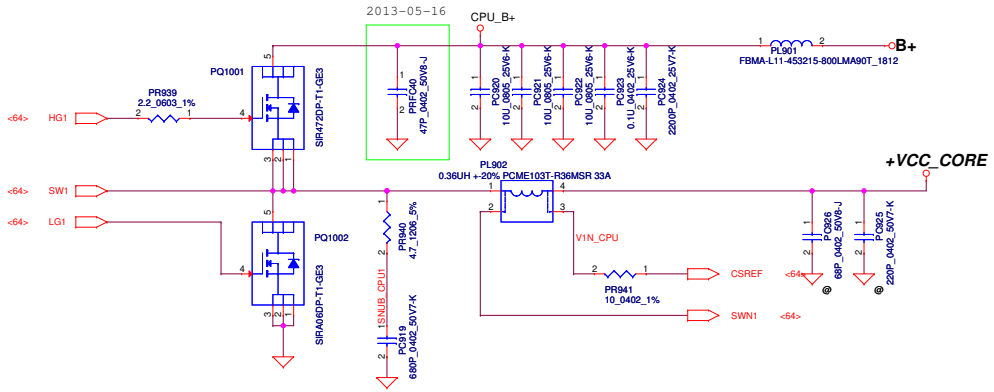
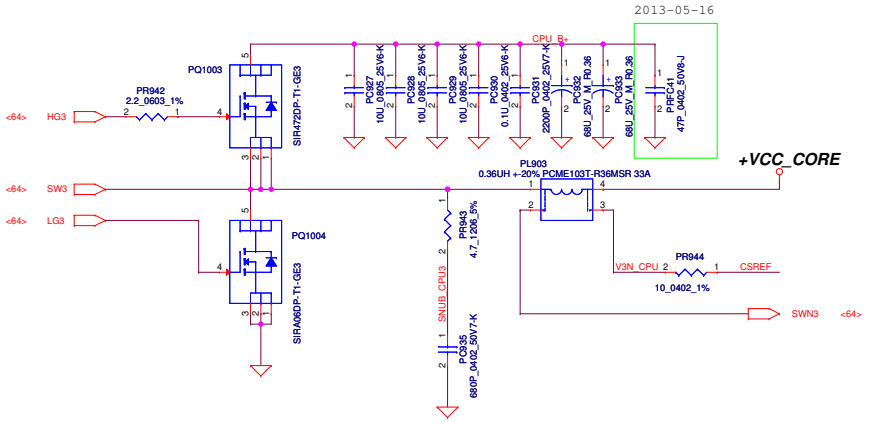
Title: CPU_CORE

Size	Document Number	Rev
Custom	E440 NM-A151	1.0

Date: Thursday, July 11, 2013 Sheet 64 of 69





Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

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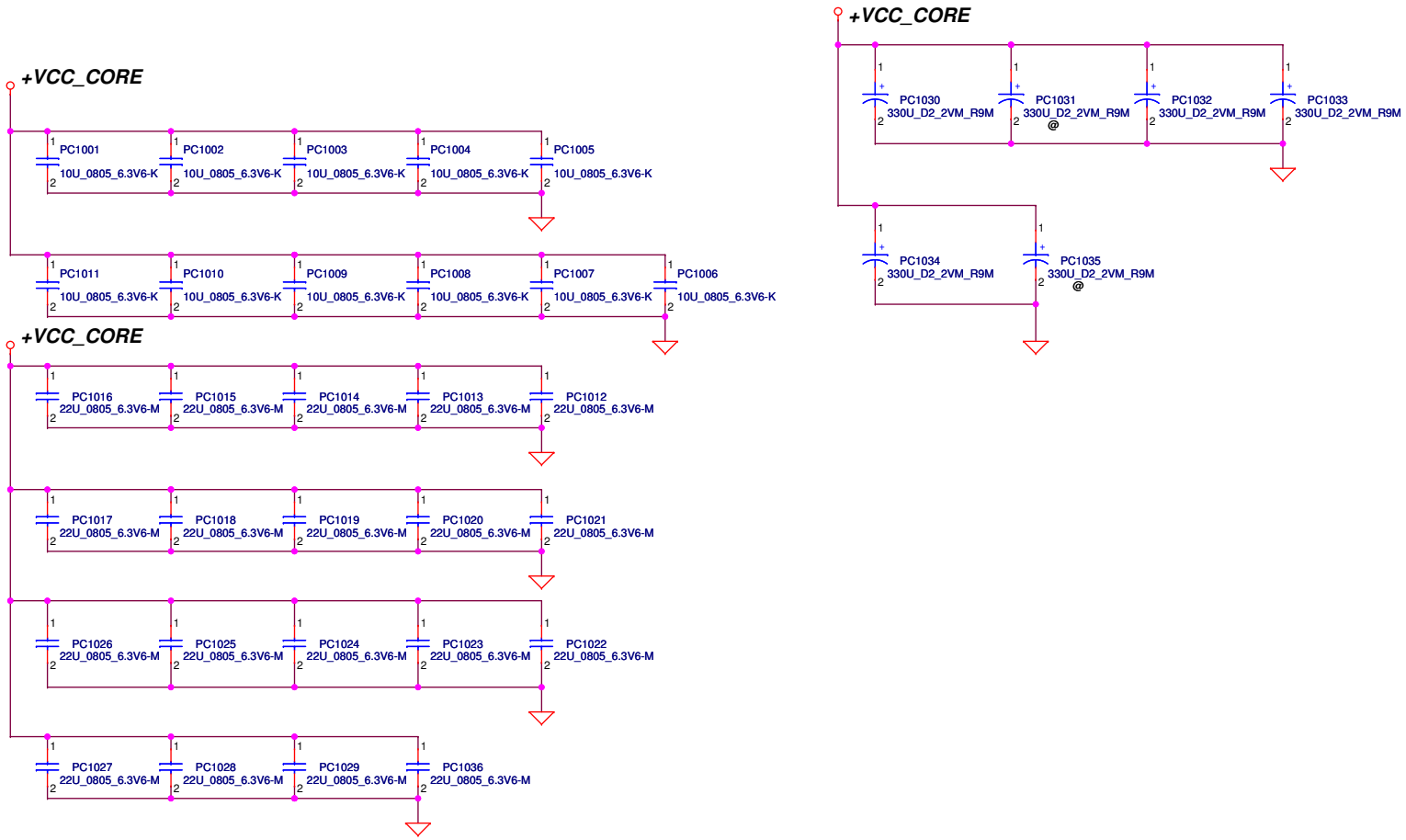
Title	CPU_CORE		
Size	Document Number		Rev
D	E440 NM-A151		1.0
Date:	Thursday, July 11, 2013	Sheet	65 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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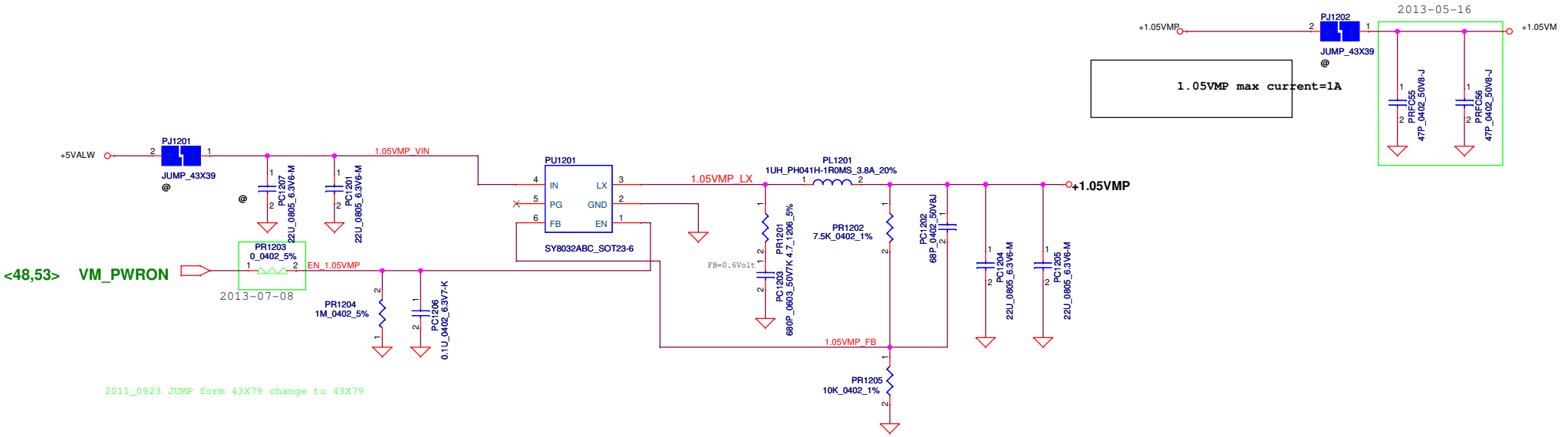
Title: PWR-PROCESSOR DECOUPLING

Size: Custom	Document Number: E440 NM-A151	Rev: 1.0
Date: Thursday, July 11, 2013	Sheet 66 of 69	



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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Title: PWR-+1.05VMP

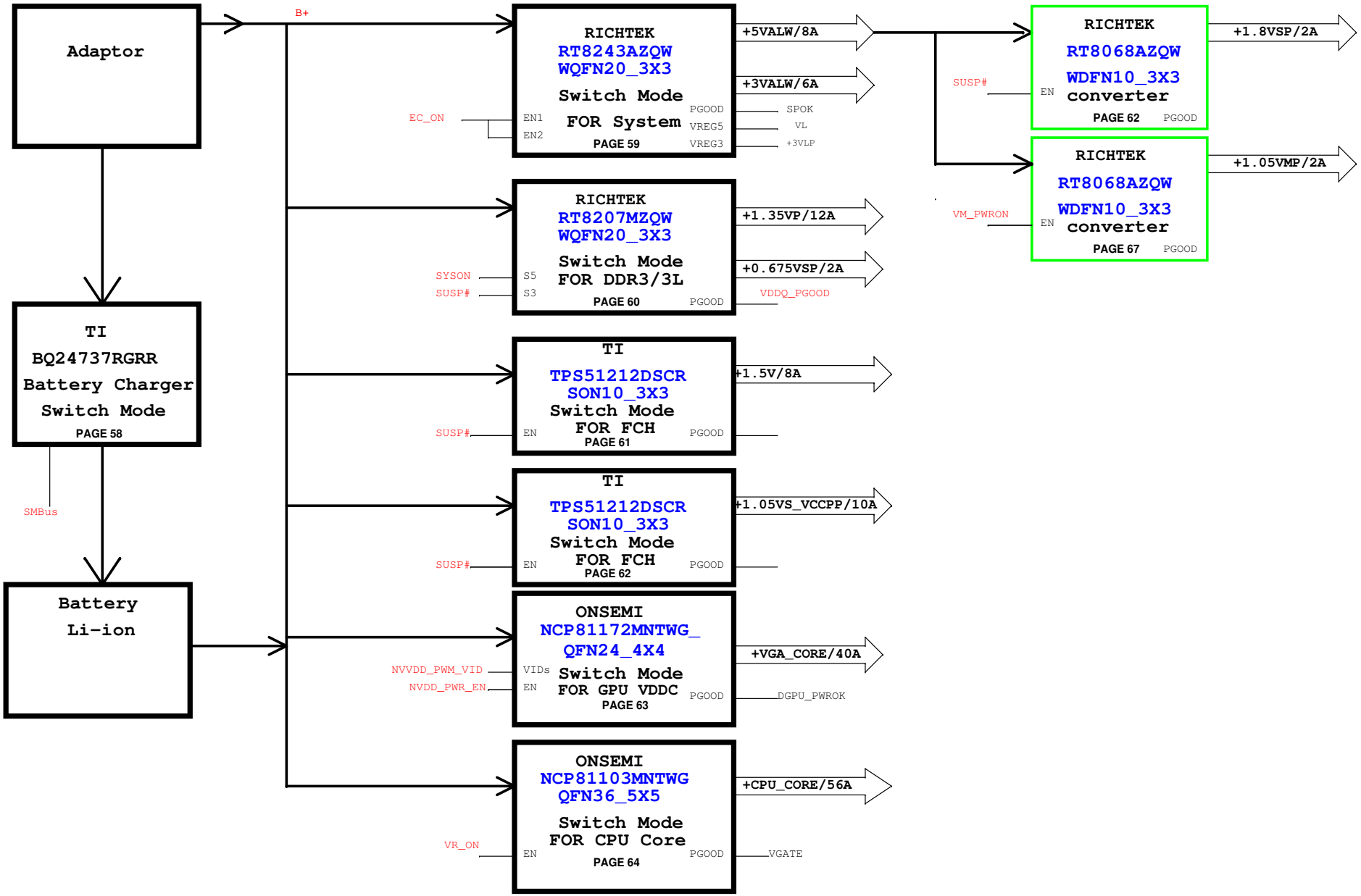
Size	Document Number	Rev
Custom	E440 NM-A151	1.0

Date: Thursday, July 11, 2013 Sheet 67 of 69

POWER PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/01/16

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Title: HW-PIR

Size: Custom | Document Number: E440 NM-A151 | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 68 of 69

HW PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/01/16

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01)	03/14	10	R64 Change R64 BOM structure from "@" to "DS3@"	For Deep S3 Function

Security Classification	Compal Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

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Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: Y490-LA8691P | Rev: 1.0

Date: Thursday, July 11, 2013 | Sheet 69 of 69