R33 INTEL UMA/DISCRETE SYSTEM DIAGRAM 01

+3V/+5V S5 PG.35
+1.05V_VTT PG.38
CPU Core PG.40~41
DDR3 PG.37
VCCSA PG.36
Charge PG.34
Dis-Charge PG.39
+VGACORE PG.42
+1.0V_VGA PG.43

SODIMM1 Max. 4GB PG.12 — DDR3 Channel A
SODIMM2 Max. 4GB PG.13 — DDR3 Channel B

INTEL IVY
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.2~5

PCI-E x8

AMD Thames XT
29mm X 29mm
TDP 25W
PG.14~20

DDR3 900MHz
VRAM 128Mx16x8,128bit PG.21~22

FDI DMI

INTEL PCH Panther Point
PG.6~11

HDMI PG.25
CRT PG.24
LVDS PG.23

HDD PG.32 — SATA0
ODD PG.32 — SATA1

DP Port B
CRT
LVDS

PCI-E x 1 — LANE2 / LANE1
LAN RTL8105EH 10/100 PG.29
WLAN BT COMBO PG.33 — USB 2.0 PORT10

PCI-E x 1 — LANE3
Accelerometer PG.33 — SMBUS
Card Reader RTS5229 PG.26

KBC EnE KB3930QF A2 PG.30 — LPC
KB PG.31
TP PG.31
ROM PG.30
FAN PG.32

USB 3.0
USB3.0 Ports X2 PG.28 — PORT1,2
Webcam PG.23 — PORT4
USB 2.0 — PORT0,1
USB2.0 Ports PG.28

AUDIO CODEC
IDT 92HD87
ICT PG.27

Speaker PG.27
HP/MIC PG.28
Analog MIC PG.28

Stackup
TOP
GND
IN1
IN2
VCC
BOT

NB5

PROJECT : R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Wednesday, September 07, 2011 Sheet 1 of 43

Ivy Bridge Processor (DMI,PEG,FDI)

Ivy Bridge Processor (CLK,MISC,JTAG)

02

U22A

DMI

Intel(R) FDI

PCI EXPRESS* - GRAPHICS

eDP

Ivy Bridge_rPGA_2DPC_Rev0p61

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

U22B

MISC

THERMAL

PWR MANAGEMENT

CLOCKS

DDR3 MISC

JTAG & BPM

Ivy Bridge_rPGA_2DPC_Rev0p61

SNB_IVB# N.A at SNB EDS #27637 0.7v1

Placement close to EC.

close to VR side

reserved for "boot hang 47" issue

CPU RESET#

SM_DRAMPWROK Processor Input.

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

CPU XDP

DDR3 DRAM RESET

FDI disable (DIS only stuff)

DEL

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

check

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

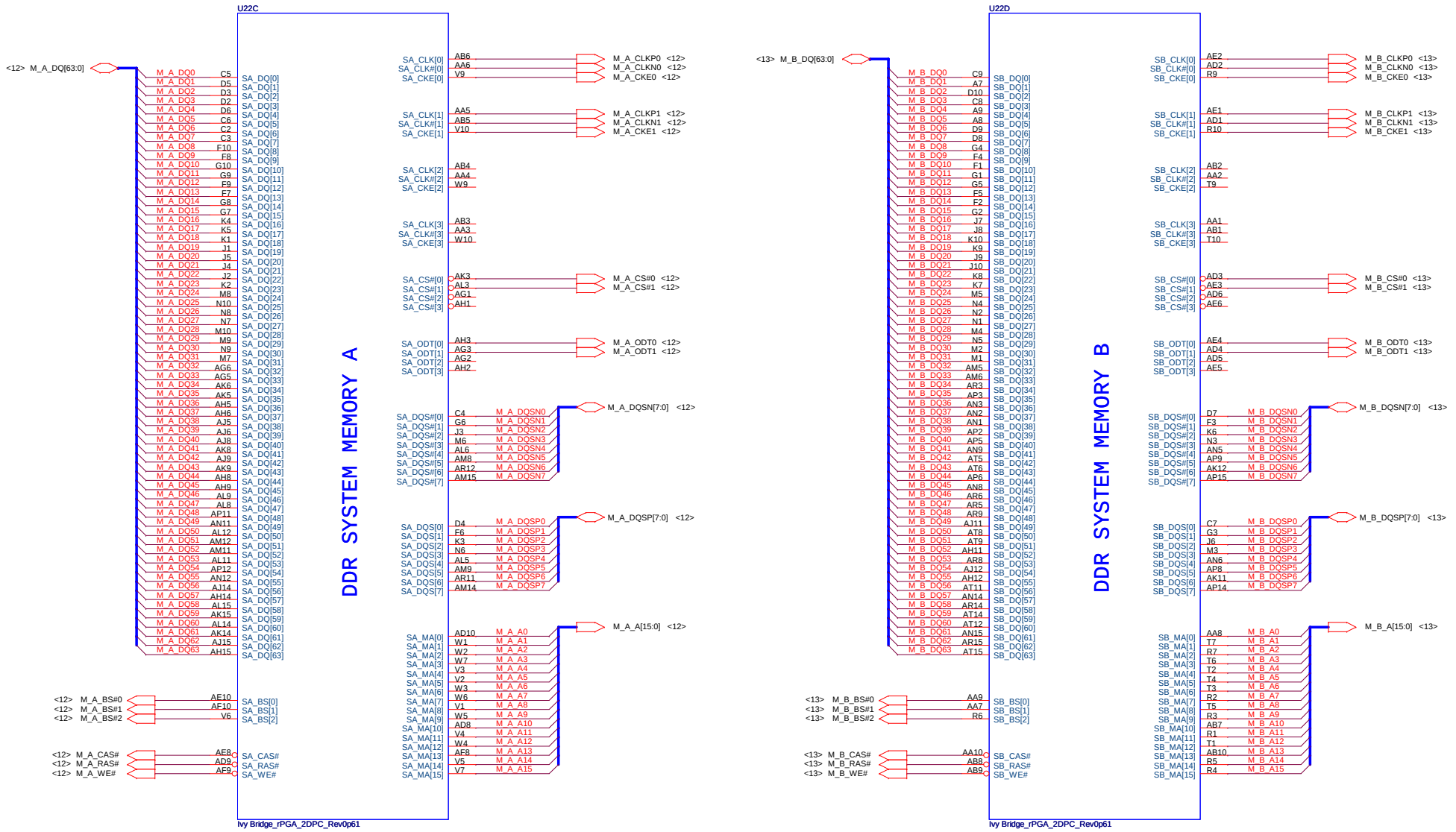
NB5

PROJECT : R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A

Date: Wednesday, August 31, 2011 Sheet 2 of 43

Ivy Bridge Processor (DDR3)



PROJECT : R33
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	1A

Date: Wednesday, August 31, 2011 | Sheet 3 of 43

Ivy Bridge Processor (POWER)

04

POWER

U22F

SNB: 55A
IVY: 55A

+VCC_CORE

C638 22U/6.3VS_8 C682 10U/6.3VS_6 C637 22U/6.3VS_8
C80 22U/6.3VS_8 C67 22U/6.3VS_8 C193 22U/6.3VS_8
C664 22U/6.3VS_8 C196 22U/6.3VS_8 C272 22U/6.3VS_8
C699 22U/6.3VS_8 C53 22U/6.3VS_8 C639 22U/6.3VS_8
C199 22U/6.3VS_8 C691 *10U/6.3V_6S C58 22U/6.3VS_8
C160 22U/6.3VS_8 C277 22U/6.3VS_8 C303 22U/6.3VS_8
C248 22U/6.3VS_8 C233 22U/6.3VS_8 C179 22U/6.3VS_8
C684 *22U/6.3VS_8 C222 *22U/6.3VS_8 C576 22U/6.3VS_8
C192 22U/6.3VS_8 C678 10U/6.3VS_6 C253 22U/6.3VS_8
C573 22U/6.3VS_8 C572 22U/6.3VS_8 C695 *10U/6.3V_6S

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CORE SUPPLY

PEG AND DDR

SNB: 8.5A
IVY: 8.5A

+1.05V_VTT

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C165 22U/6.3VS_8 C156 22U/6.3VS_8 C626 22U/6.3VS_8
C271 22U/6.3VS_8 C207 22U/6.3VS_8 C184 22U/6.3VS_8
C155 *22U/6.3VS_8 C227 22U/6.3VS_8 C666 22U/6.3VS_8
C677 *22U/6.3VS_8 C218 *22U/6.3VS_8 C88 *22U/6.3VS_8
C635 22U/6.3VS_8 C94 *22U/6.3VS_8 C302 *22U/6.3VS_8
C188 *22U/6.3VS_8 C652 22U/6.3VS_8 C247 *22U/6.3VS_8
C657 *22U/6.3VS_8 C645 22U/6.3VS_8 C168 22U/6.3VS_8

5/14 modify

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

+1.05V_VTT

J23

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

SENSE LINES

VCC_SENSE AJ35
VSS_SENSE AJ34

R157 100_4 +VCC_CORE
VCC_SENSE <40>
VSS_SENSE <40>
R160 100_4

VCCIO_SENSE B10
VSS_SENSE_VCCIO A10

VCCP_SENSE
VSSP_SENSE

VCCP_SENSE <38>
VSSP_SENSE <38>

Trace Route to Power IC area.

+1.05V_VTT
VCCP_SENSE R394 10/F_4
VSSP_SENSE R390 10/F_4

+1.5V <10,12,33>
+1.8V <7,10,38,43>
+VCCSA <36>
+1.5VSUS <2,10,12,13,37,43>
+1.5V_CPU <2>
+VCC_GFX <41>
+1.05V_VTT <2,10,30,38,40>
+VCC_CORE <41>

Ivy Bridge_rPGA_2DPC_Rev0p61

POWER

U22G

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

+VCC_GFX SNB: 21.5A

C669 22U/6.3V_8 C273 22U/6.3V_8
C305 22U/6.3V_8 C324 22U/6.3V_8
C304 22U/6.3V_8 C670 22U/6.3V_8
C325 22U/6.3V_8 C249 22U/6.3V_8
C668 22U/6.3V_8 C250 22U/6.3V_8
C274 22U/6.3V_8 C671 22U/6.3V_8

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

GRAPHICS

SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34

R162 100/F_4 +VCC_GFX
VCC_AXG_SENSE <40>
VSS_AXG_SENSE <40>
R166 100/F_4

VREF

SM_VREF AL1

+VDDR_REF_CPU
CAD Note: +VDDR_REF_CPU should have 10 mil trace width

R192 100K_4
Q18 2N7002
DDR_VTTREF <12,13,37>
MAIND
MAIND <39>

SA_DIMM_VREFDQ B4
SB_DIMM_VREFDQ D1

SMDDR_VREF_DQ0_M3 <12>
SMDDR_VREF_DQ1_M3 <13>

R391 *1K_4 R386 *1K_4

DDR3 -1.5V RAILS

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

SNB: 5A
+1.5V_CPU

C320 10U/6.3V_6 C226 10U/6.3V_8 C310 10U/6.3V_6 C275 10U/6.3V_6
C209 10U/6.3V_6 C341 10U/6.3V_6 C737 *330U_2.5V_5.0x5.9_ESR10m

330uF x1, 10uF_8 x6 Socket BOT edge.

SA RAIL

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

SNB: 6A
+VCCSA

C625 10U/6.3V_8 C579 10U/6.3V_8 C630 10U/6.3V_8 C571 *10U/6.3V_8

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

1.8V RAIL

+1.8V SNB: 1.5A

C55 10U/6.3V_8 C51 1U/6.3V_4 C50 1U/6.3V_4 C65 *330u_2.5V_3528

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

Ivy Bridge_rPGA_2DPC_Rev0p61

MISC

VCCSA_SENSE H23
VCCSA_VID[0] C22
VCCSA_VID[1] C24
VCCIO_SEL A19

VCCUSA_SENSE_R R85 *0_4/S
VCCUSA_SENSE <36>
VCCSA_SEL0 <36>
VCCSA_SEL <36>
R71 10K_4
R73 10K_4
V_TVID1
R389 0_4
H_VTTVID1 <38>

+1.5V_CPU R50 *0_8/S +1.5V
40mile routing

Layout note: need routing together and ALERT need between CLK and DATA.

SVID CLK

H_CPU_SVIDCLK
VR_SVID_CLK <40>

SVID DATA

+1.05V_VTT +1.05V_VTT
Place PU resistor close to CPU
R172 130/F_4
R175 *130/F_4
Place PU resistor close to VR
H_CPU_SVIDDAT
VR_SVID_DATA <40>

Place PU resistor close to CPU

SVID ALERT

C352 0.1U/10V_4
+1.05V_VTT R170 75/F_4
H_CPU_SVIDALRT# R171 43_4
VR_SVID_ALERT# <40>

CPU VDDQ

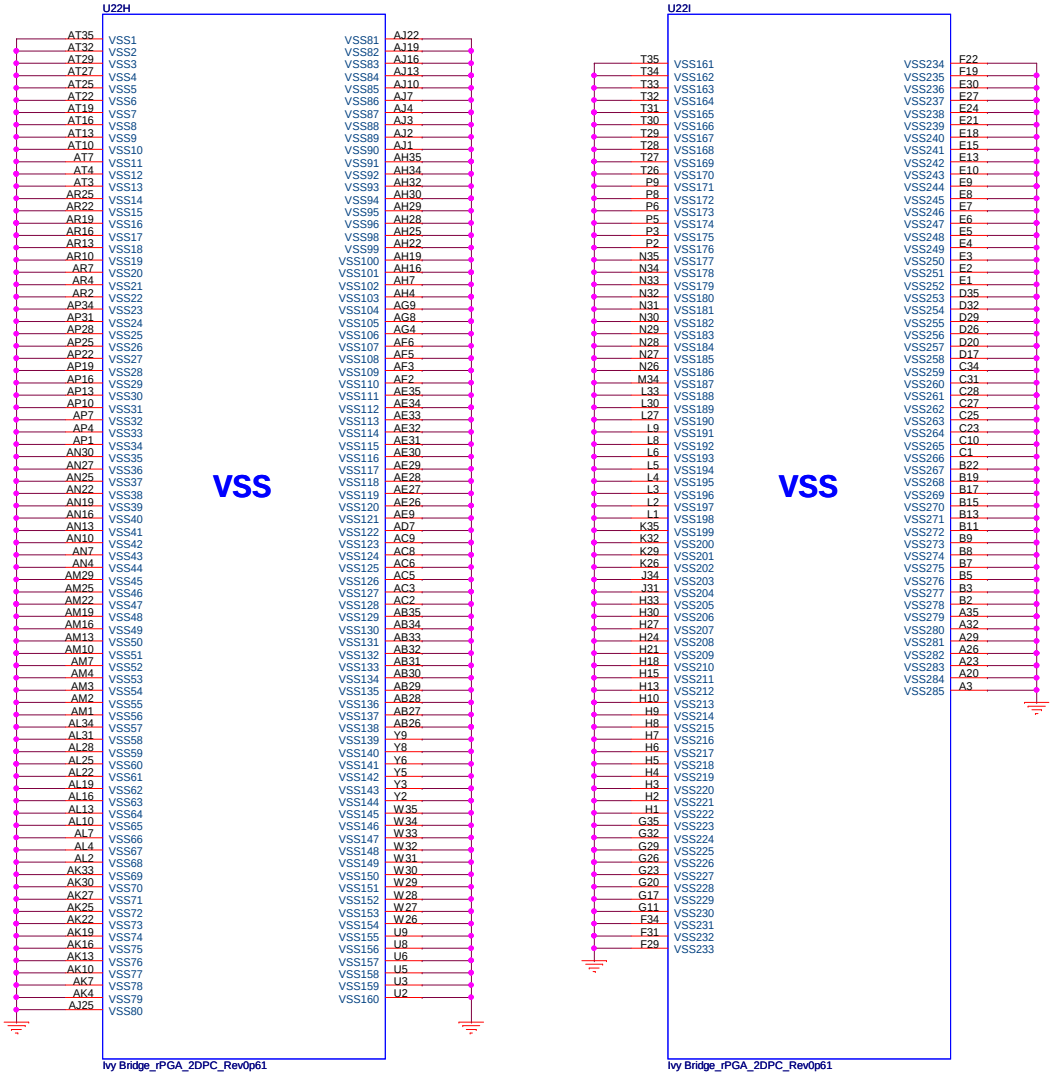
+1.5VSUS +1.5V_CPU +1.5VSUS
Q10 AON7410
R229 220_8
C582 0.1U/10V_4
C580 0.1U/10V_4
C574 0.1U/10V_4
C577 0.1U/10V_4
Placement close to CPU.
MAIND
C54 *470P/50V_4
Q22 2N7002
MAIN_ONG <2,39>

NB5

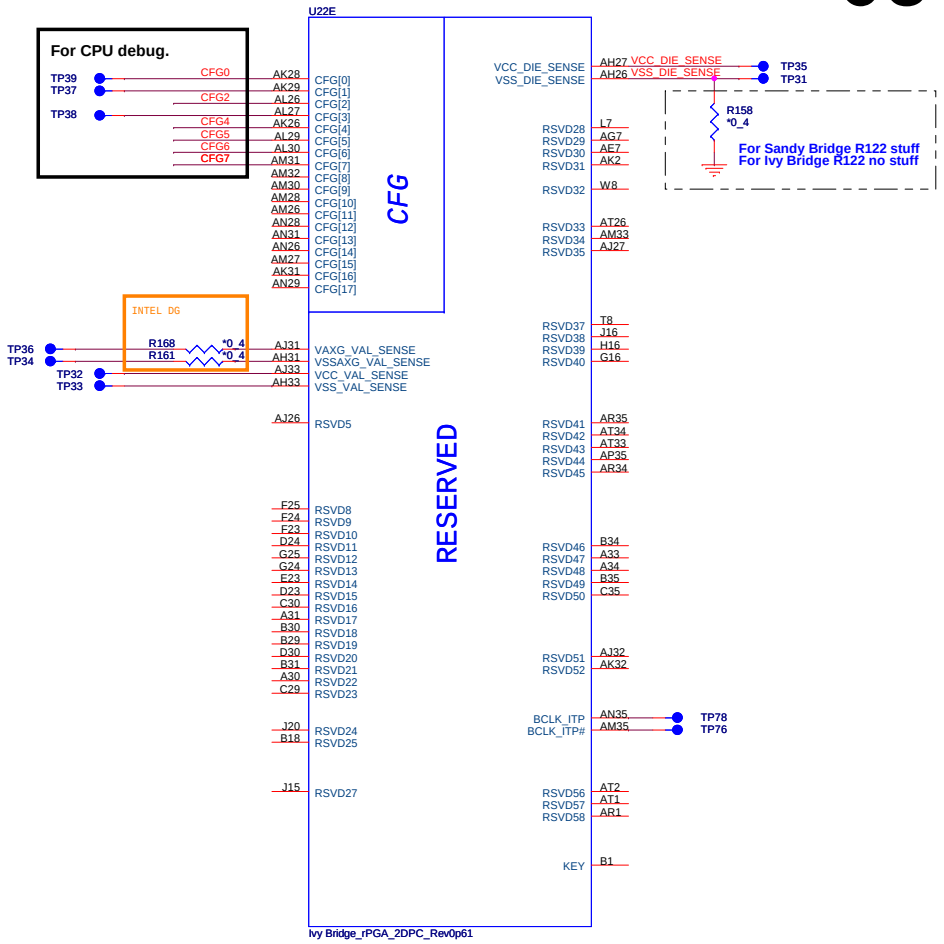
PROJECT : R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	1A
Date: Wednesday, August 31, 2011	Sheet 4 of 43	

Ivy Bridge Processor (GND)



Ivy Bridge Processor (RESERVED, CFG)



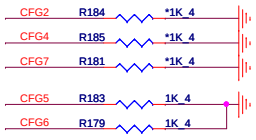
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PROJECT : R33
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A

Date: Wednesday, August 31, 2011 Sheet 5 of 43

Cougar Point/Panther Point (DMI,FDI,PM)

Cougar Point/Panther Point (LVDS,DDI)

06

U32C

U32D

PD Res place close to PCH

PCH to Res routeing 37.5 ohm Impedance.

Res to connector filter routeing 50ohm Impedance.

Reserve from EMI request

Reserve for power on sequence

PCH Pull-high/low(CLG)

INT HDMI disable (DIS only remove)

INT HDMI Detect Function

System PWR_OK(CLG)

DPWROK FOR DSW

Remove DSW power rail

On Die DSW VR Enable

High = Enable (Default)
Low = Disable

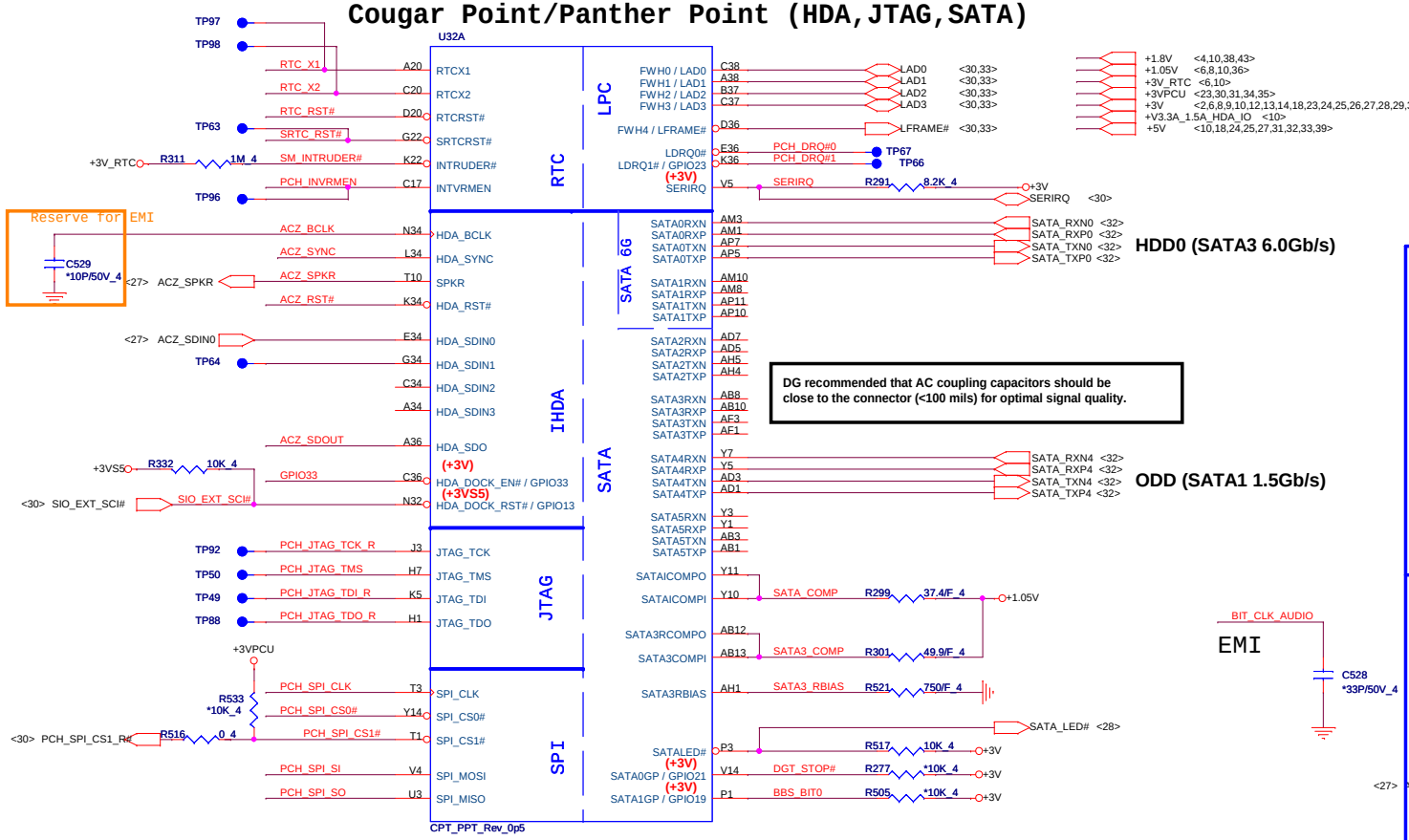
PROJECT : R33
Quanta Computer Inc.

NB5

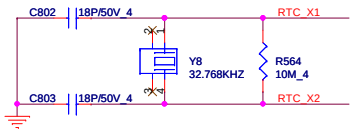
Size: Custom | Document Number: PCH 1/6 (DMI/FDI/VIDEO) | Rev: 1A

Date: Wednesday, August 31, 2011 | Sheet 6 of 43

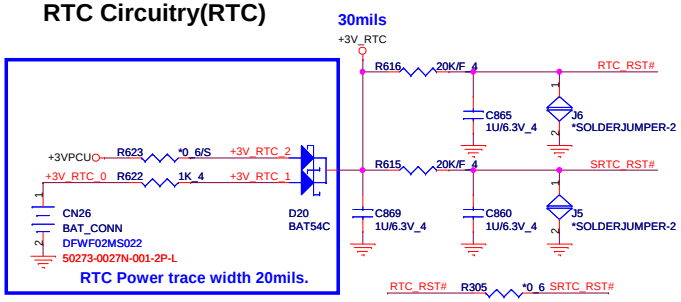
Cougar Point/Panther Point (HDA,JTAG,SATA)



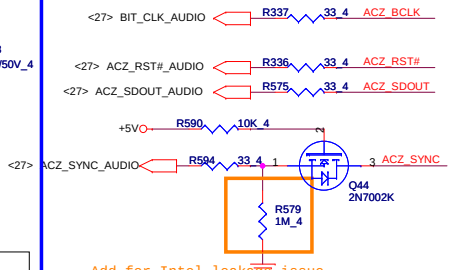
RTC Clock 32.768KHz



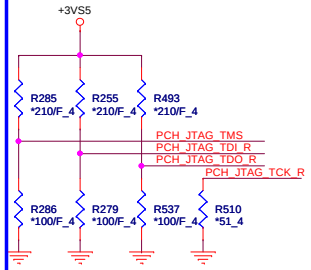
RTC Circuitry(RTC)



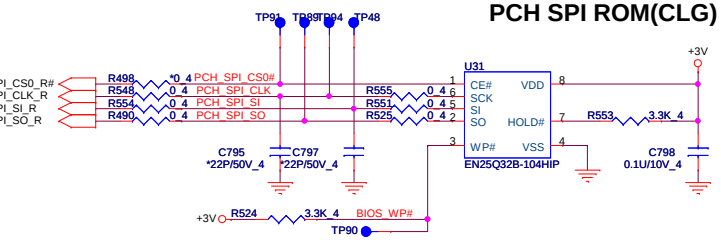
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
Max	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
Socket		DFHS08FS023

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R500 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R584 *1K_4 R595 10K_4 PCI_GNT3# <8>
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R563 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R572 0_4 BIOS_WP#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# GNT0# Boot Location: 1 1 SPI; 1 0 LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		R534 *1K_4 BBS_BIT0 R585 *1K_4 BBS_BIT1 <8>
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R547 *1K_4 NV_ALE <8>
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R526 2.2K_4 R546 1K_4 NV_CLE <9> H_SNB_IVB# <2> sandy/Ivy bridge
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R334 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Overridden	GPIO33_E ACZ_SDOUT R573 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R492 *1K_4 PLL_ODVR_EN <9>
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R292 1K_4 +3V

PROJECT : R33
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

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07

Cougar Point/Panther Point (PCI,USB,NVRAM)

Cougar Point/Panther Point(PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

USB3.0

EMI

change 25M to small size

RF

PLTRST#(CLG)

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

PCIE Clock

SMBus/Pull-up(CLG)

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

Remove Ra, Rb for UMA &
SG. 27MHz support DIS only.

Remove for UMA only.

CLOCK TERMINATION for FCIM

SG : Rb ; UMA : Ra

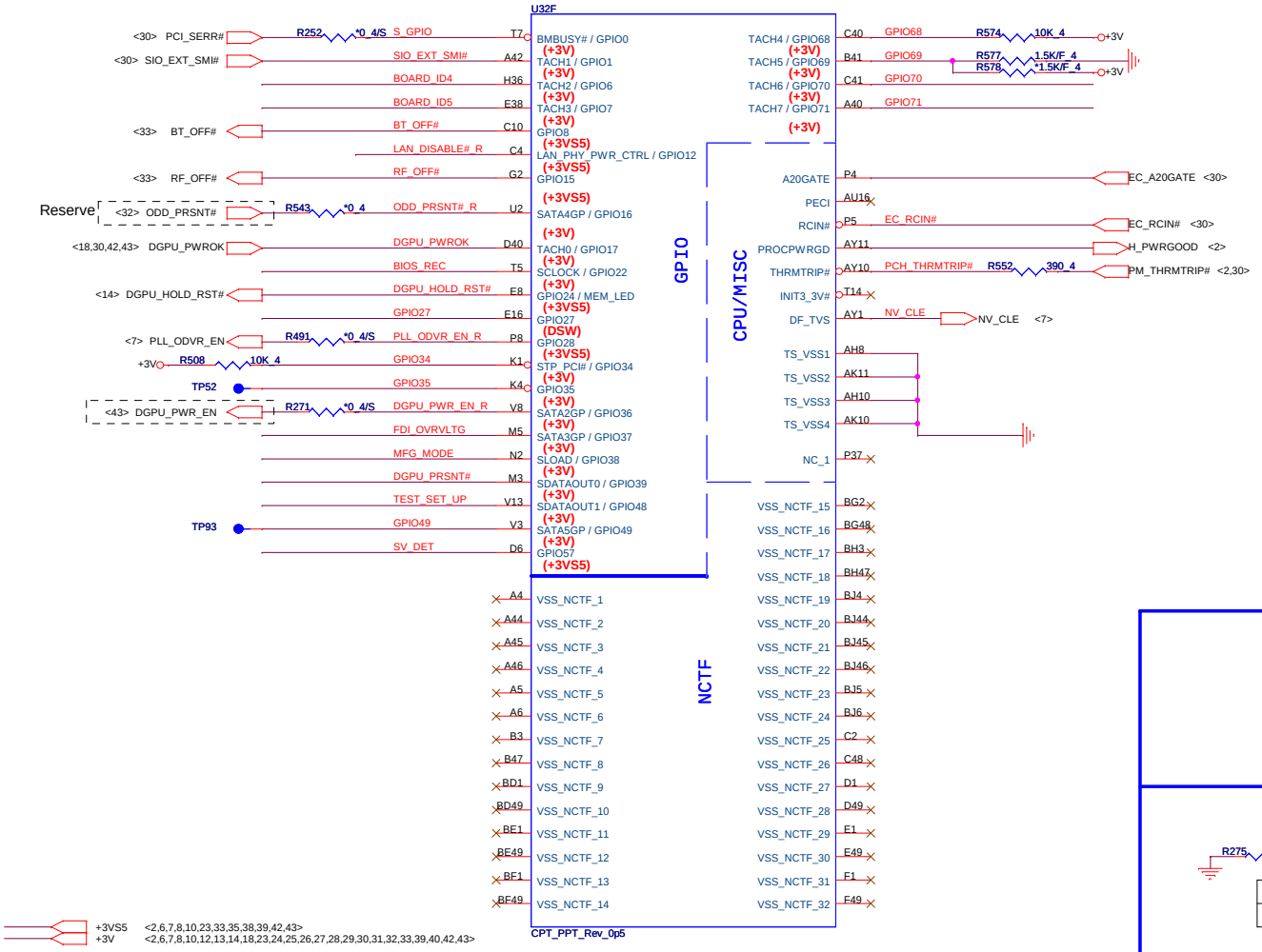
PROJECT : R33
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	1A

Date: Wednesday, August 31, 2011 | Sheet 8 of 43

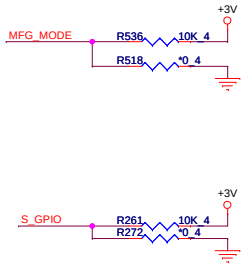
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



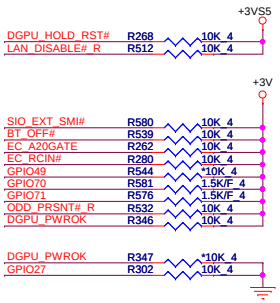
Clock Gen Power OK (CLG)

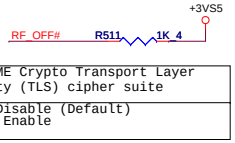
09

MFG-TEST

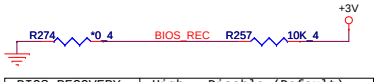


GPIO Pull-up/Pull-down(CLG)

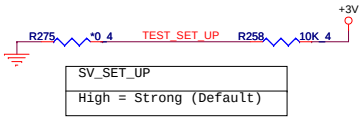




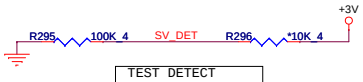
Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable



BIOS RECOVERY	High = Disable (Default) Low = Enable

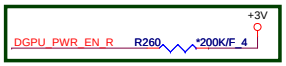


SV_SET_UP
High = Strong (Default)

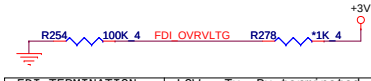


TEST DETECT
Low = Default

9/3 SI for H/W.

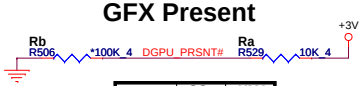


DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



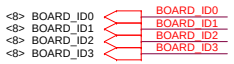
FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

GFX Present

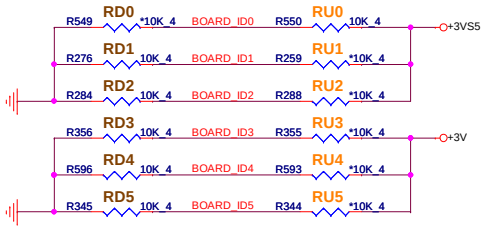


	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

BOARD ID SETTING



Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R33 UMA	0	0	0	0	0	0
R33 DIS	0	0	0	0	0	1
	0	0	0	0	1	1
	0	0	0	1	1	1
	0	0	0	0	0	0

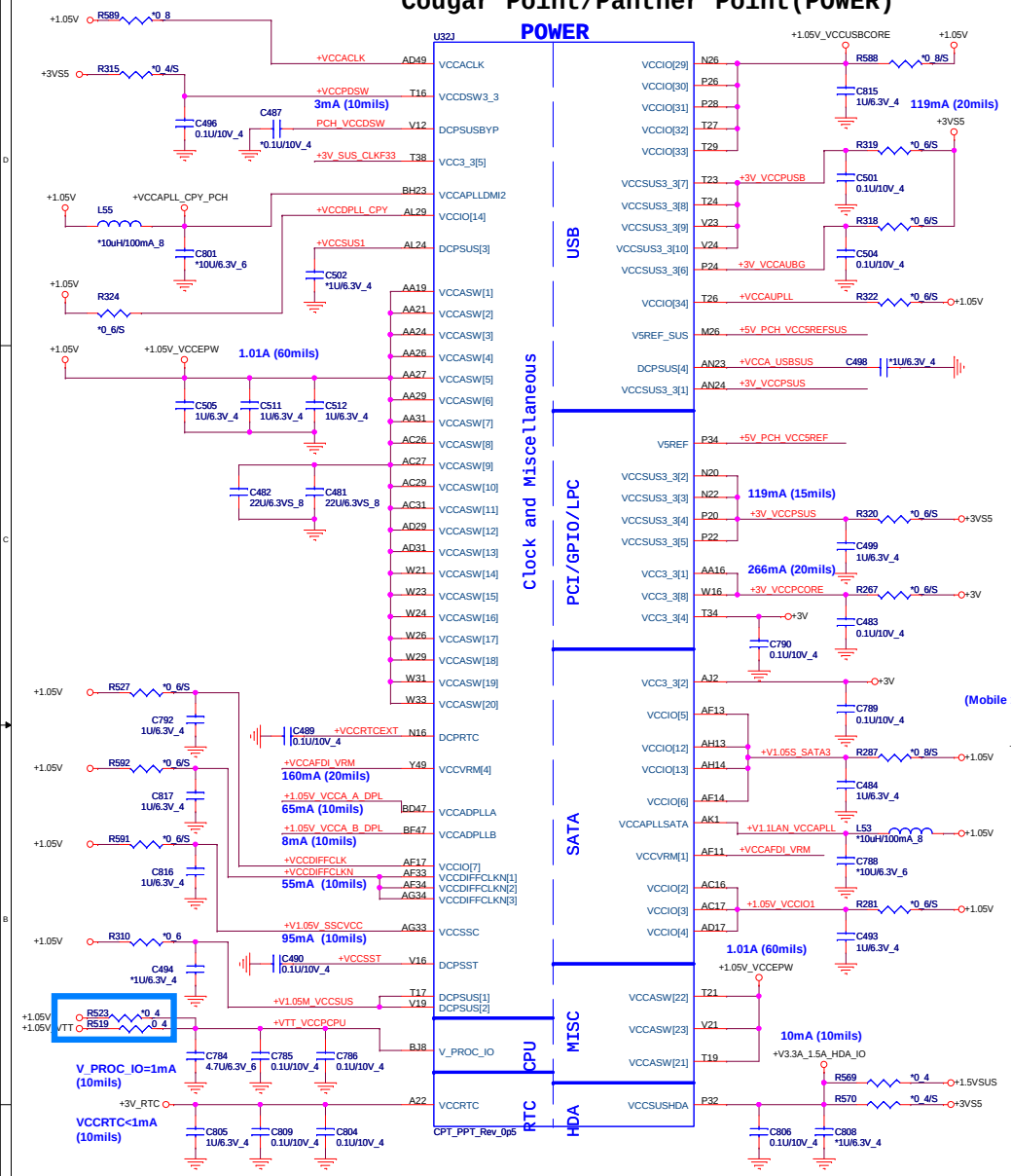


NB5

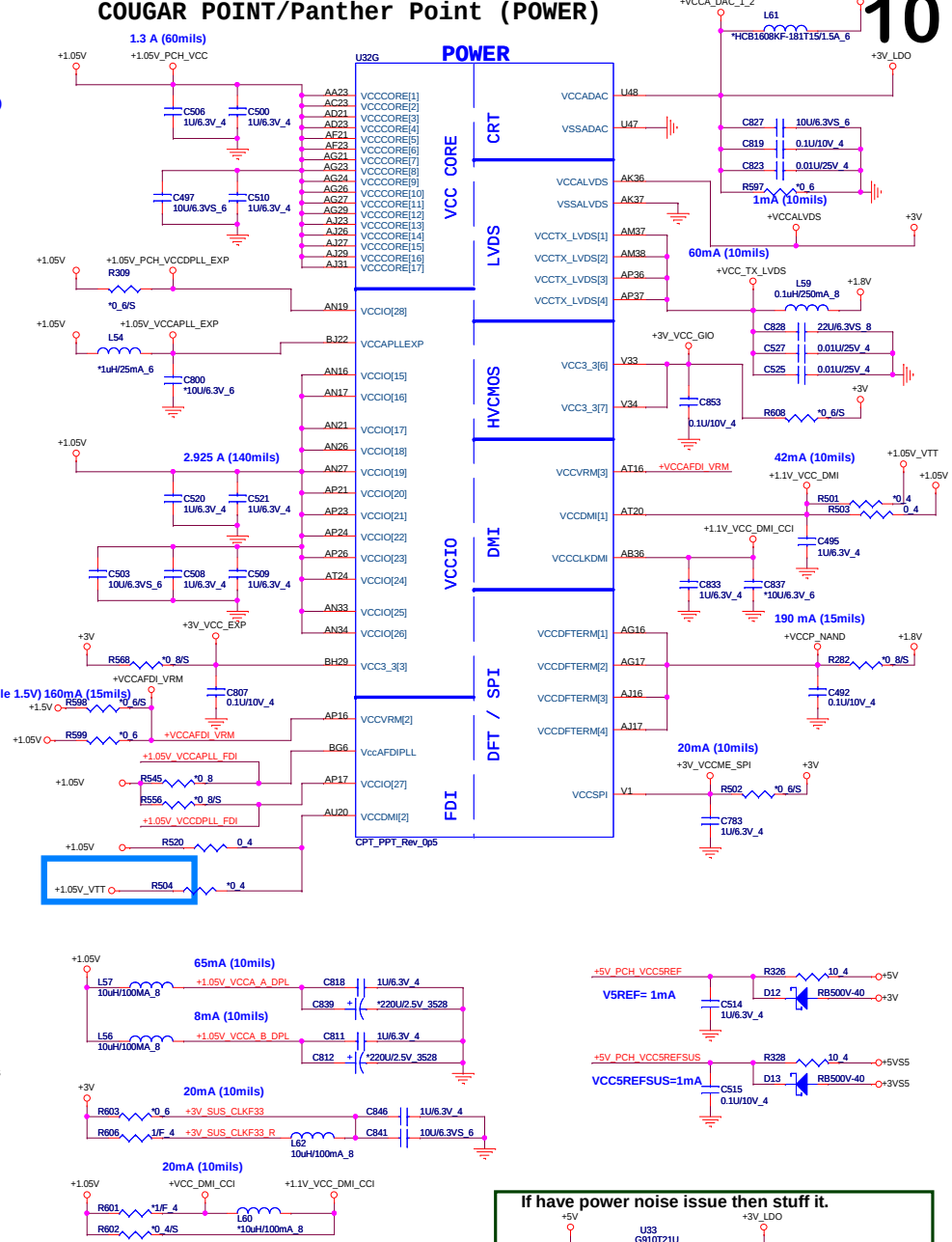
PROJECT : R33
Quanta Computer Inc.

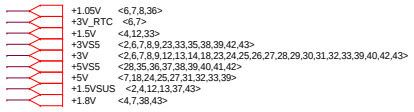
Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A
Date: Wednesday, August 31, 2011	Sheet 9 of 43	

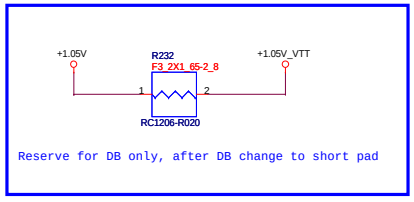
Cougar Point/Panther Point(POWER)

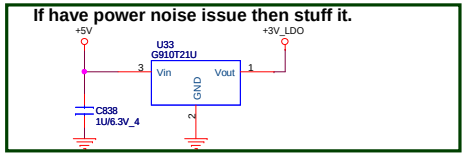


COUGAR POINT/Panther Point (POWER)









NB5	PROJECT : R33 Quanta Computer Inc.		
Size: Custom	Document Number: PCH 5/6 (POWER)		Rev: 1A
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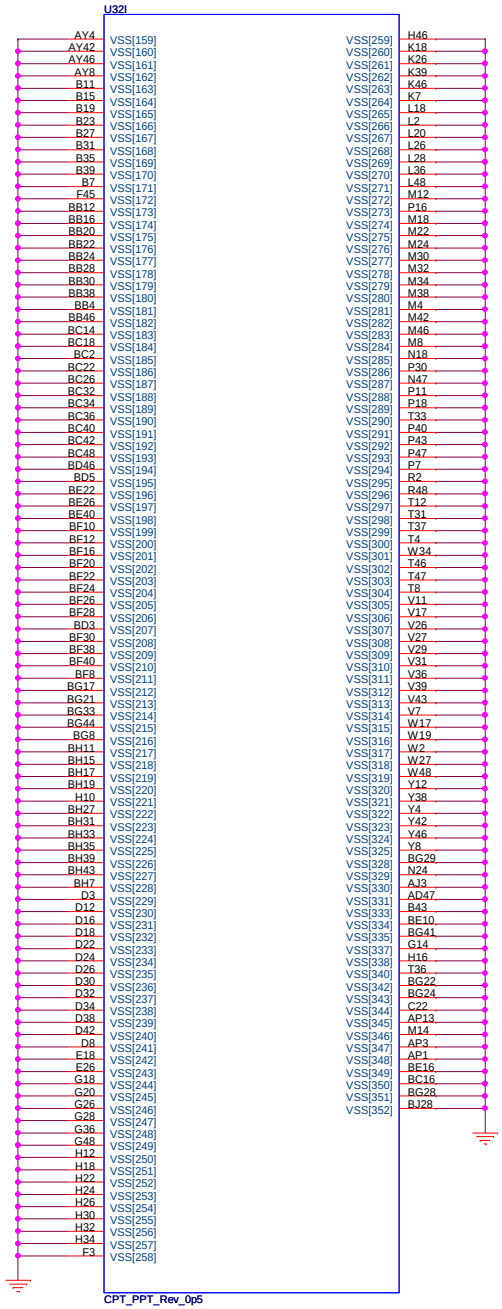
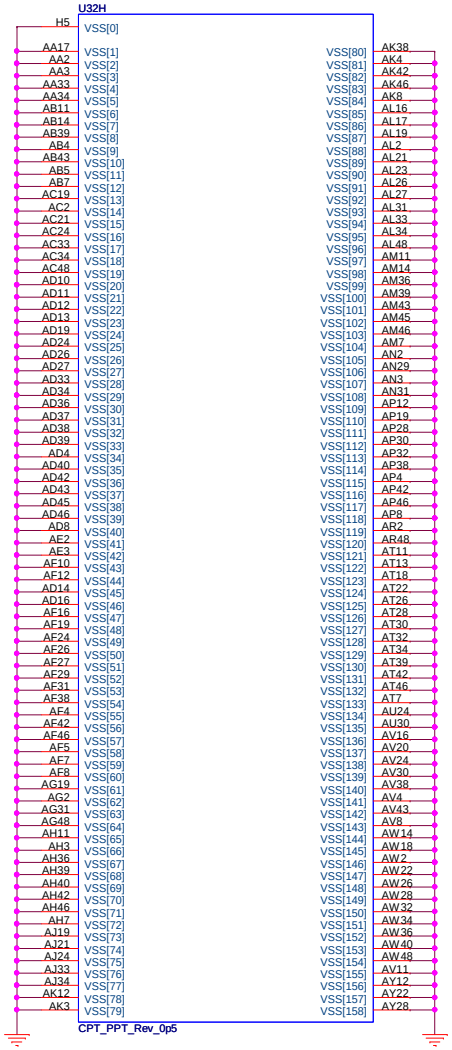
Cougar Point/Panther Point (GND)



Cougar Point/Panther Point (GND)



NB5

PROJECT : R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A
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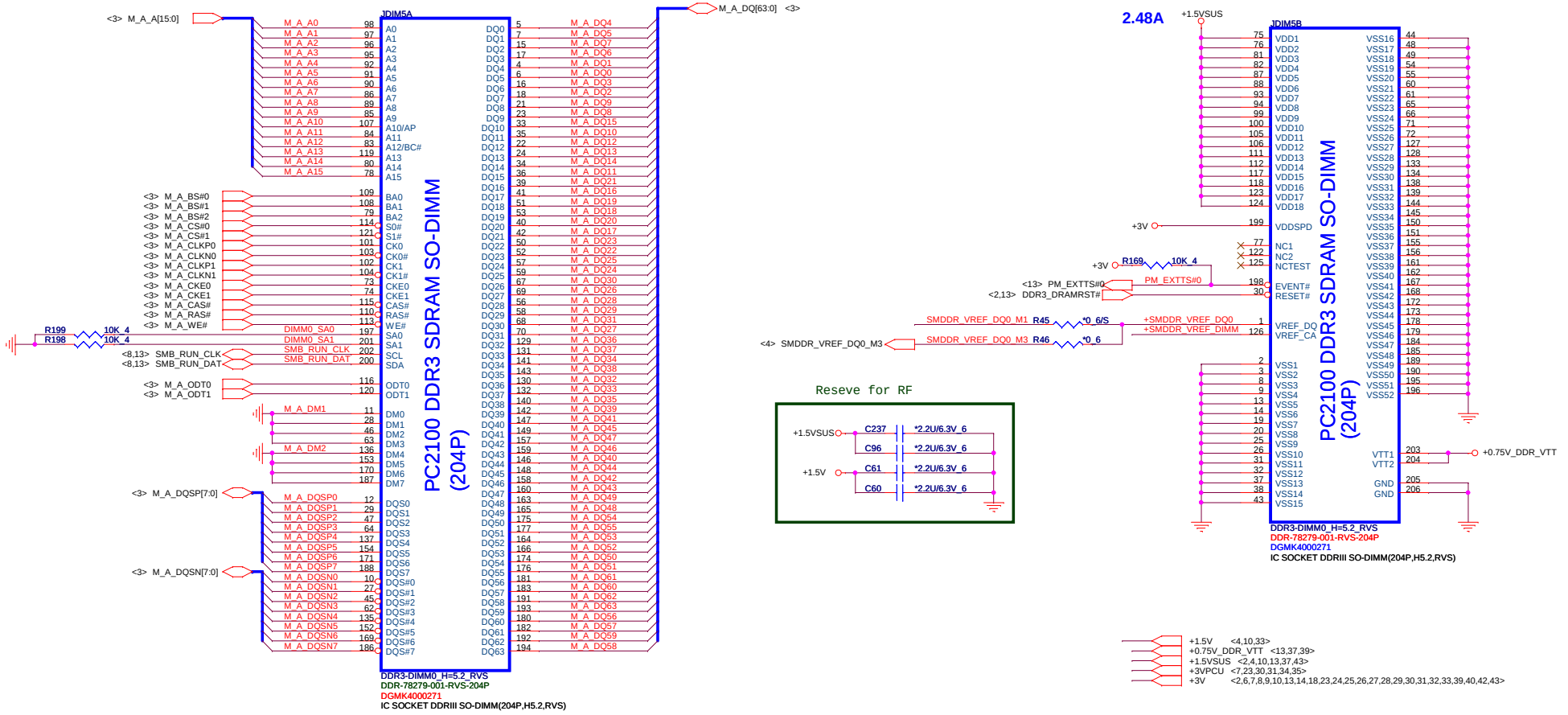
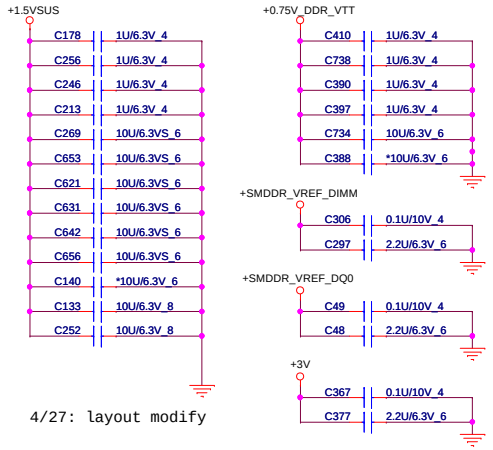


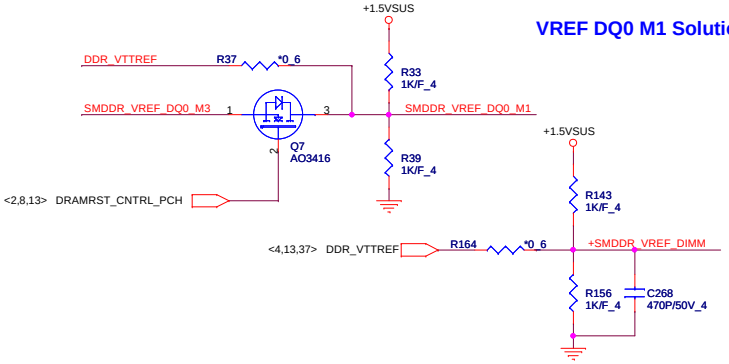
VREF DQ0 M2 Solution

del M2 solution

Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution

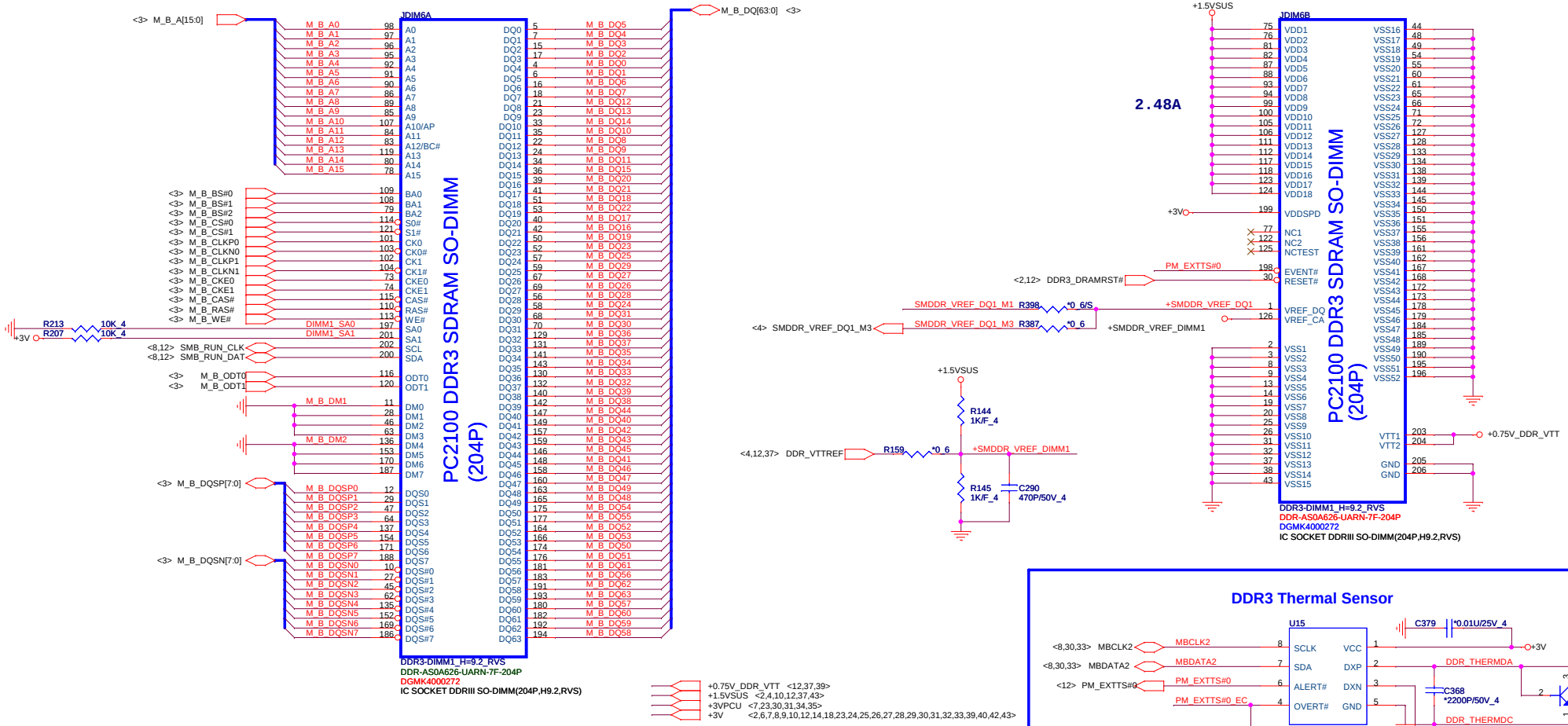


NB5

PROJECT : R33
Quanta Computer Inc.

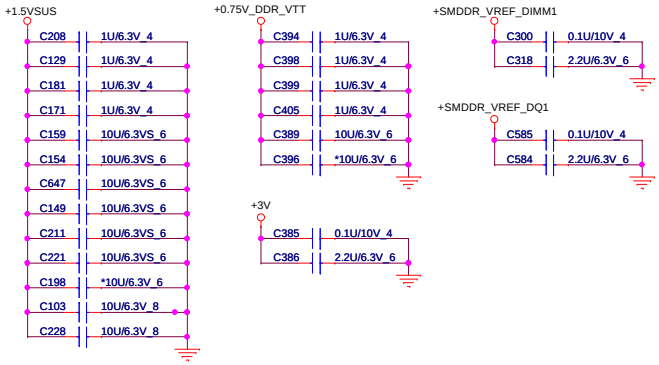
Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A

Date: Wednesday, August 31, 2011 Sheet 12 of 43

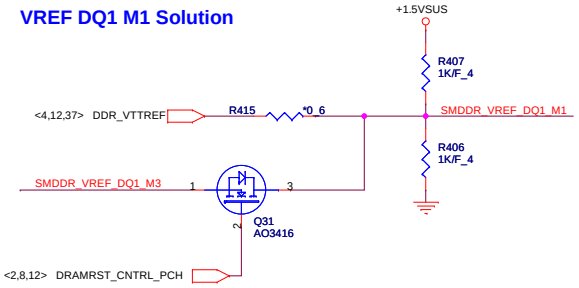


DDR3 Thermal Sensor

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



del M2 solution

NB5	PROJECT : R33 Quanta Computer Inc.		
	Size: Custom	Document Number: DDR3 DIMM1-RVS (9.2H)	Rev: 1A
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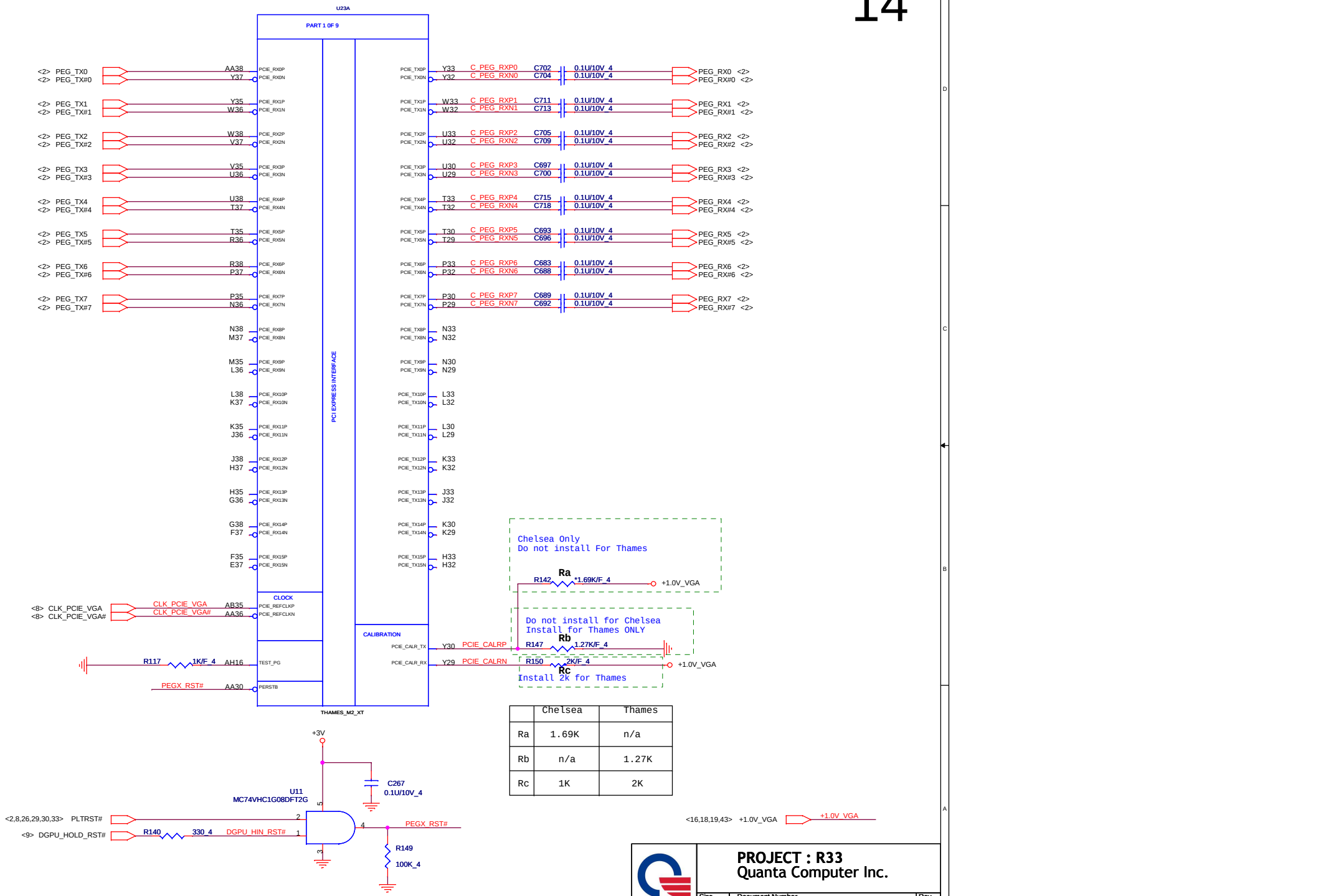

	Chelsea	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K

NB5

PROJECT : R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_PCIE_Interface	1A

Date: Wednesday, August 31, 2011 Sheet 14 of 43

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix- D (VEGA)	64Mx16 *8, 900Mhz	H5TQ1G63DFR-11C
0001	Micron- G die	64Mx16 *8, 900Mhz	MT41J64M16JT-107G:G
0010	Samsung- G die	64Mx16 *8, 900Mhz	K4W1G1646G-BC11
0011	Hynix- B (VEGA)	128Mx16 *8, 900Mhz	H5TQ2G63BFR-11C
0100	Micron- D die	128Mx16 *8, 900Mhz	MT41J128M16HA-107G:D
0101	Samsung- C die	128Mx16 *8, 900Mhz	K4W2G1646C-HC11
0110	Hynix- B (VEGA)	128Mx16 *4, 900Mhz	H5TQ2G63BFR-11C
0111	Micron- D die	128Mx16 *4, 900Mhz	MT41J128M16HA-107G:D
1000	Samsung- C die	128Mx16 *4, 900Mhz	K4W2G1646C-HC11
1001			
1010			
1011			
1100			
1101			
1110			
1111			

GPIO16 GPIO20 GPIO15

Thames XT	PWRCNTL2	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

Memory ID

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

A 3-k external pull up (3.3 V) is required if an external BIOS ROM chip is used.

Reserve for Power Play

Thames INSTALL, do not install for Chelsea
PS_0 should be tied to GND on Thames

PS_1,PS_2, PS_3 are NC on Thames
Do not install for Thames

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NB5

Size: Custom | Document Number: THAMES_Main & GND | Rev: 1A

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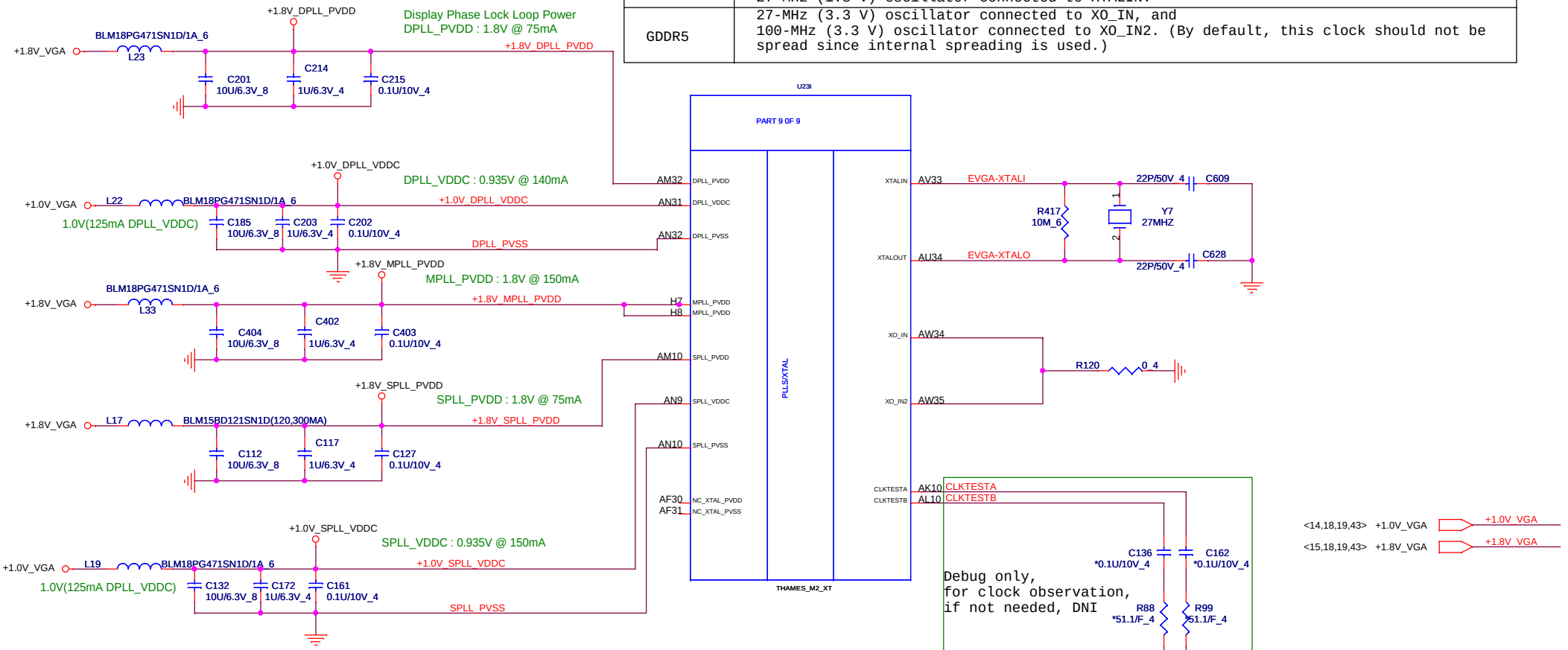
Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)



NB5

PROJECT : R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_XTAL	1A

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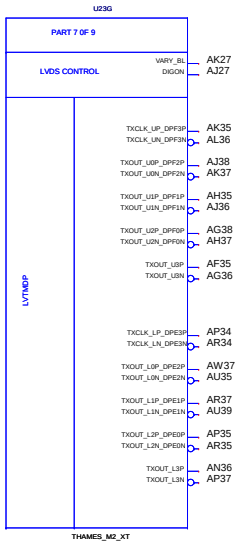
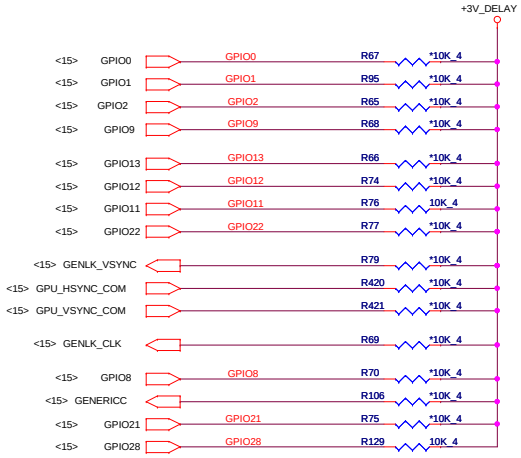




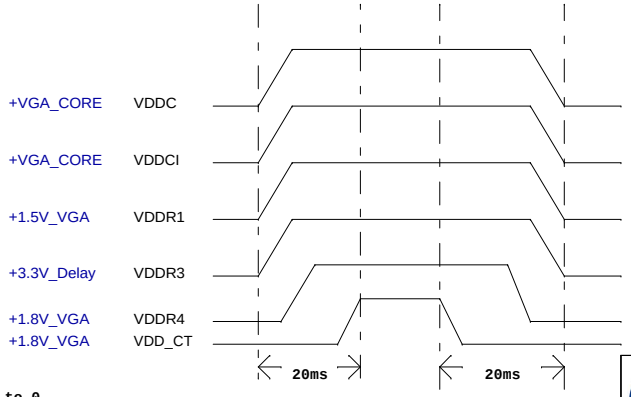
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence



NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_LVDS / STRAP	1A

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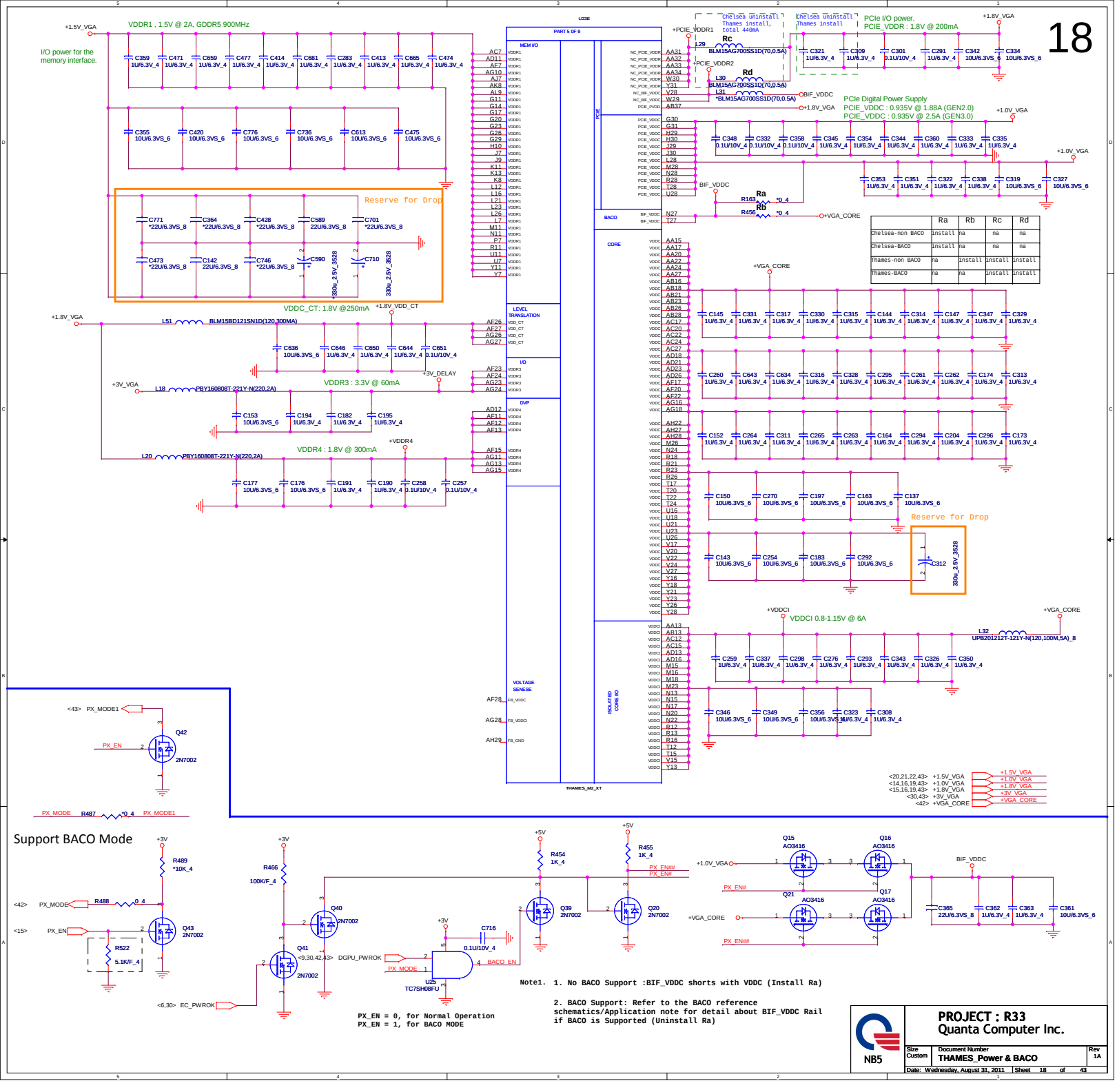

	Ra	Rb	Rc	Rd
Chelsea-non BACO	install	na	na	na
Chelsea-BACO	install	na	na	na
Thames-non BACO	na	install	install	install
Thames-BACO	na	na	install	install

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NB5	
Size	Custom
Document Number	THAMES_Power & BACO
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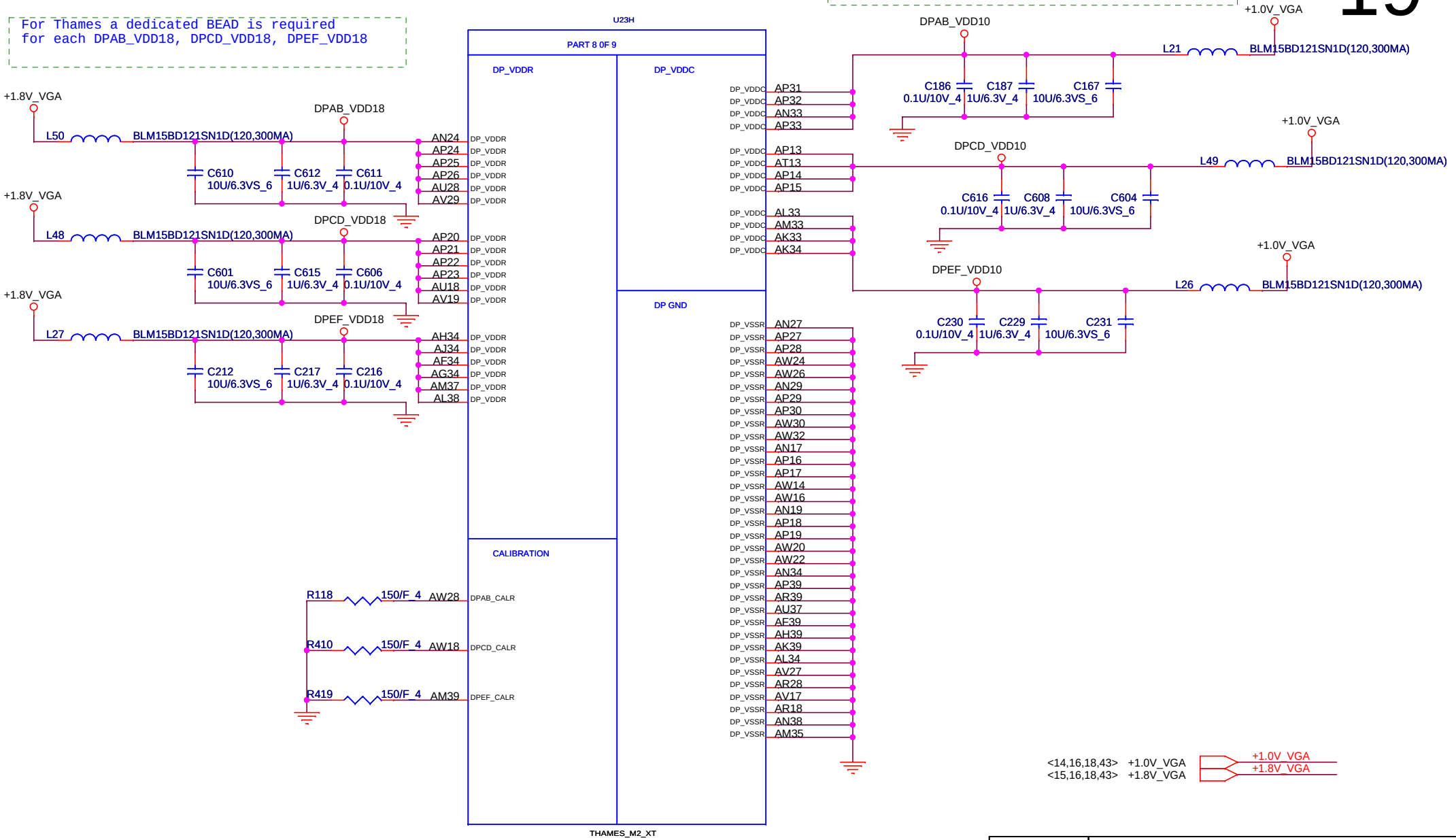
For Thames a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

For Thames a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10



NB5

PROJECT : R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**THAMES_DP Powers**	1A

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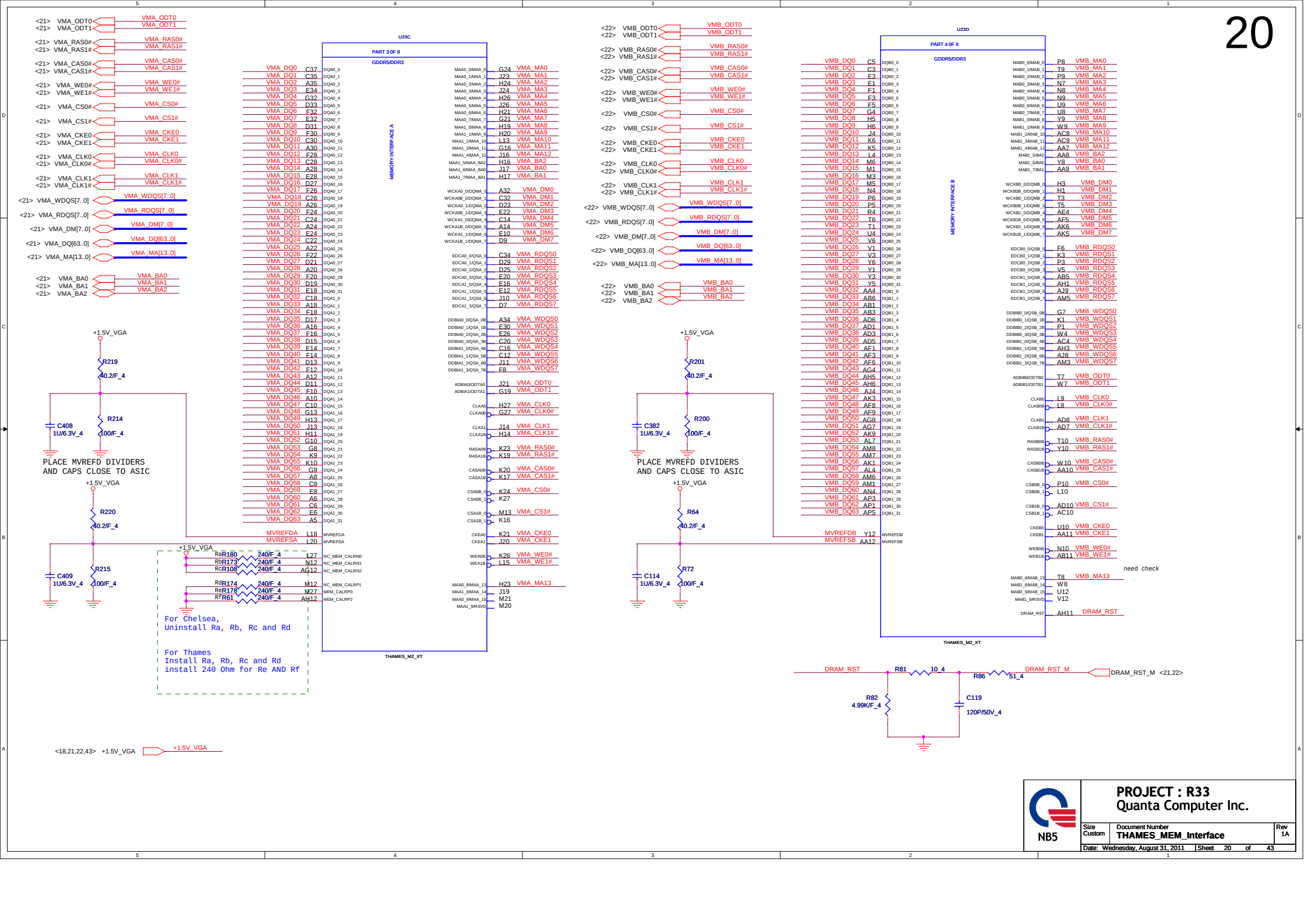
U23C
PART 3 OF 9
GDDR5/DDR3
MEMORY INTERFACE A
THAMES_M2_XT
U23D
PART 4 OF 9
GDDR5/DDR3
MEMORY INTERFACE B
THAMES_M2_XT
+1.5V_VGA
PLACE MVREFD DIVIDERS
AND CAPS CLOSE TO ASIC
For Chelsea,
Uninstall Ra, Rb, Rc and Rd
For Thames
Install Ra, Rb, Rc and Rd
install 240 Ohm for Re AND Rf
need check
DRAM_RST
DRAM_RST_M
NB5
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Quanta Computer Inc.
THAMES_MEM_Interface
Size Custom
Document Number
Rev 1A
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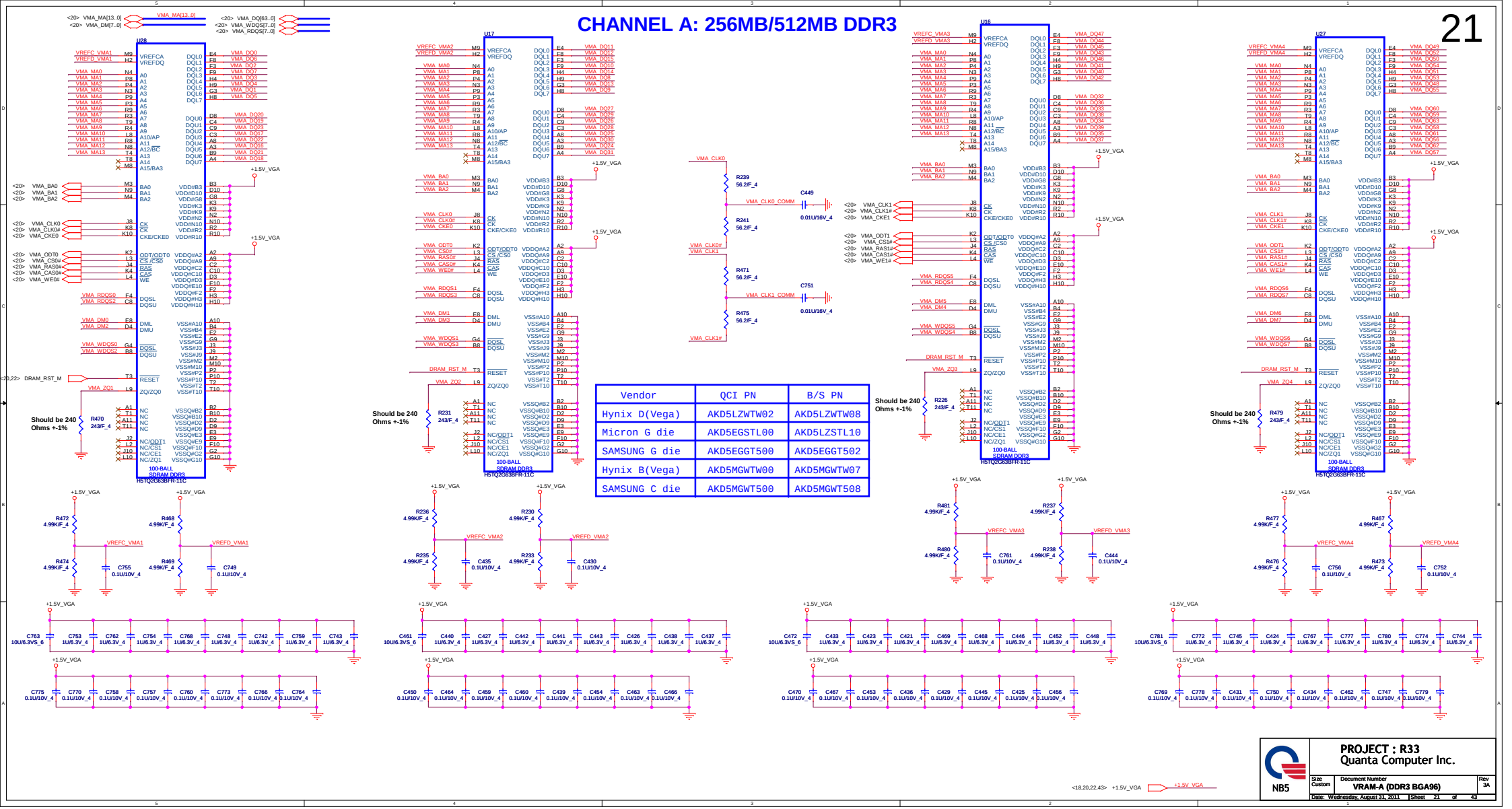
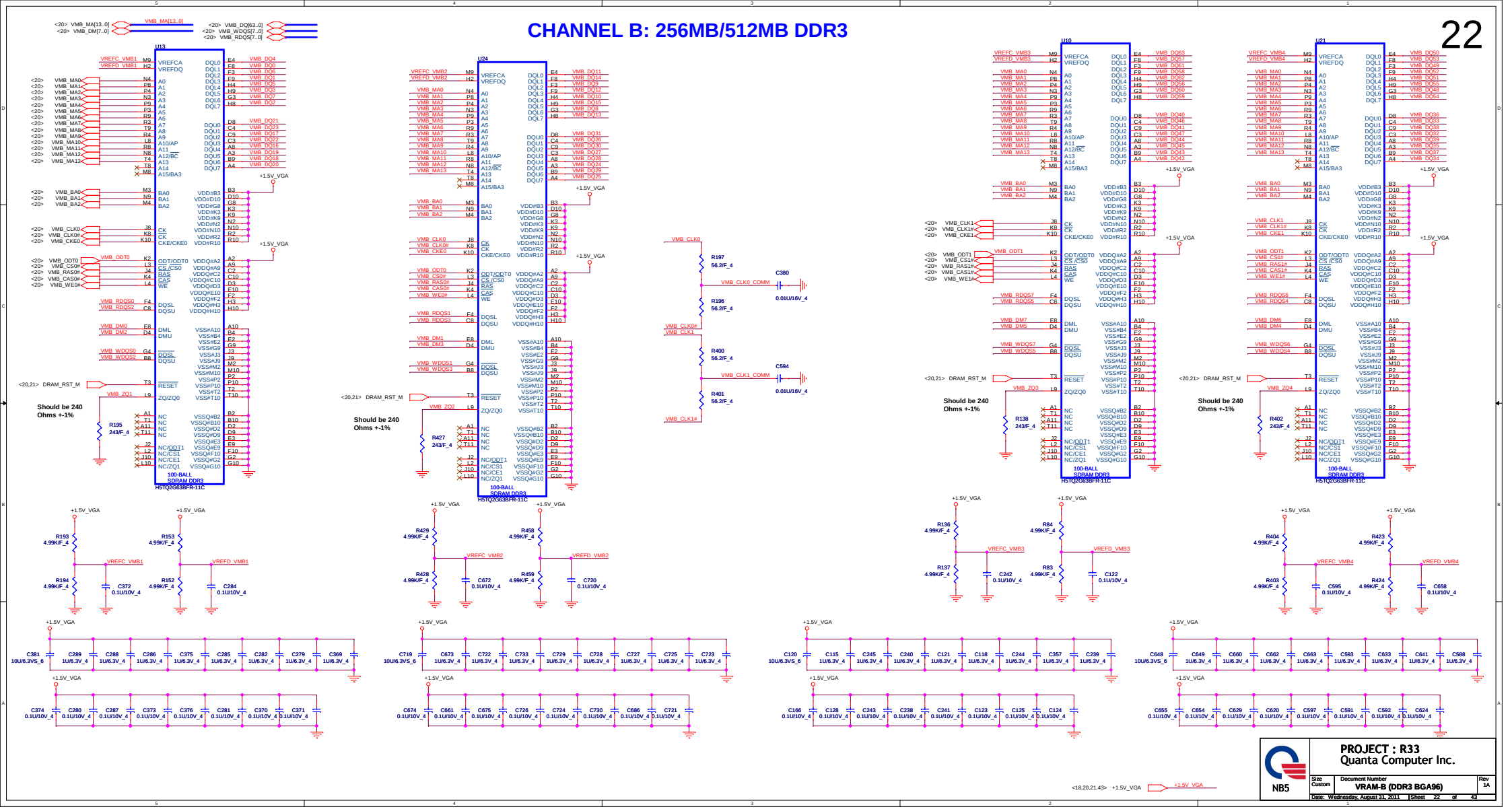
CHANNEL A: 256MB/512MB DDR3



Vendor	QCI PN	B/S PN
Hynix D(Vega)	AKD5LZWTW02	AKD5LZWTW08
Micron G die	AKD5EGSTL00	AKD5LZSTL10
SAMSUNG G die	AKD5EGGT500	AKD5EGGT502
Hynix B(Vega)	AKD5MGWTW00	AKD5MGWTW07
SAMSUNG C die	AKD5MGWT500	AKD5MGWT508

CHANNEL B: 256MB/512MB DDR3



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Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	VRAM-B (DDR3 BGA96)	1A

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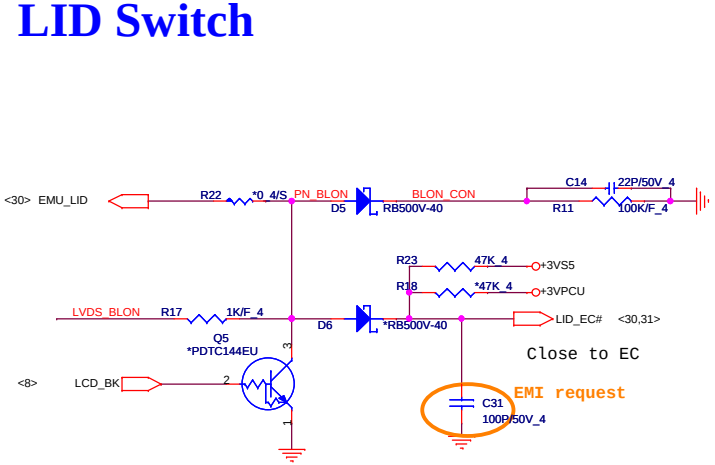
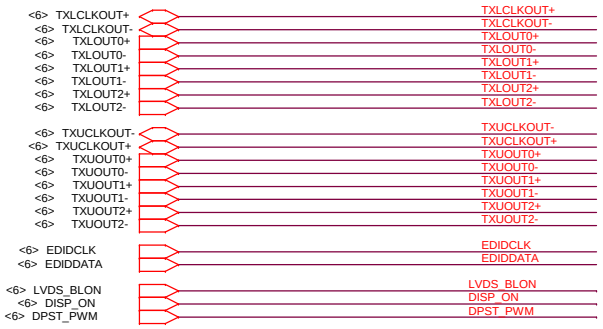
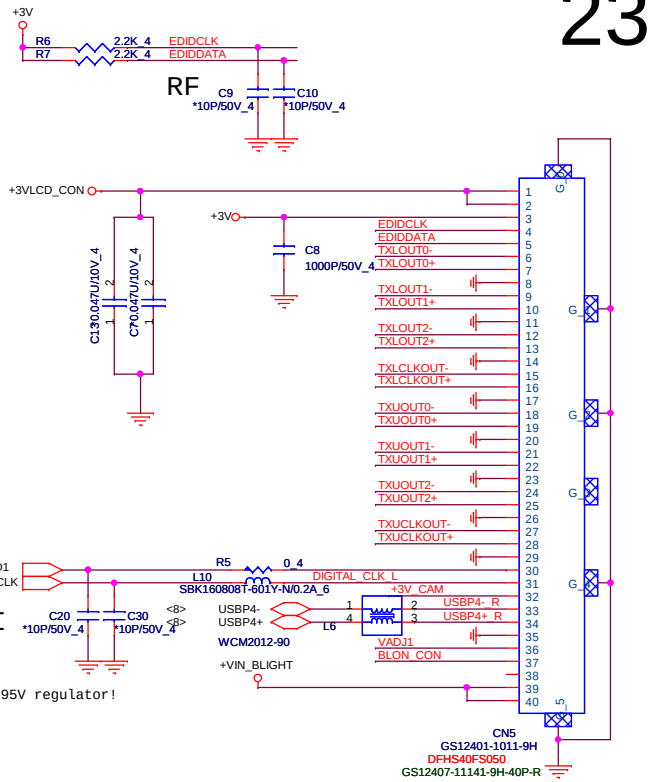
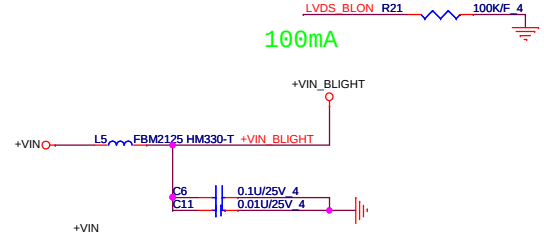
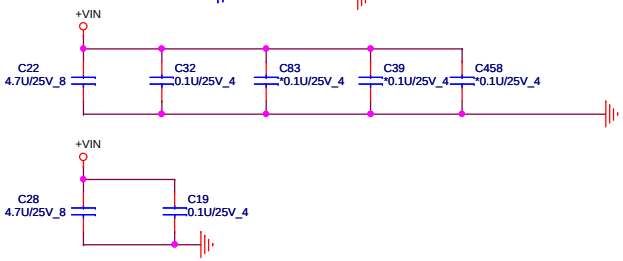
LID Switch

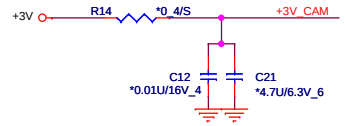








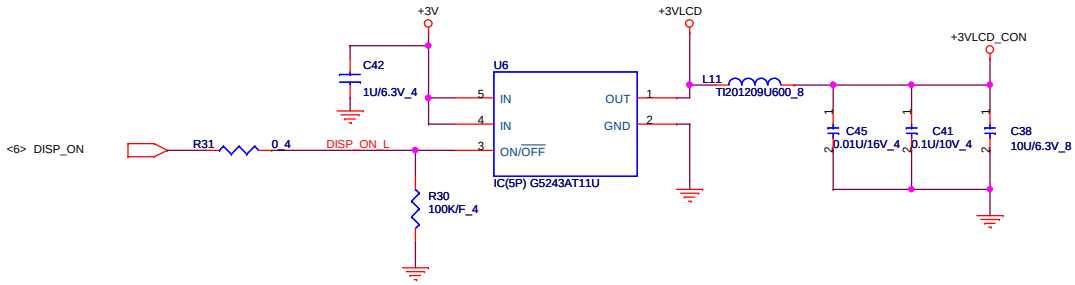




Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

follow L6 location

USBP4- R8 *0_4 USBP4- R
USBP4+ R9 *0_4 USBP4+ R



<2,6,7,8,9,10,12,13,14,18,24,25,26,27,28,29,30,31,32,33,39,40,42,43> +3V
<7,30,31,34,35> +3VPCU
<7,10,18,24,25,27,31,32,33,39> +5V
<32,34,39,43> +12VALW
<34,35,36,37,38,39,41,42,43> +VIN

NB5

PROJECT : R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

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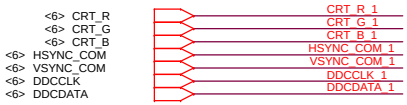
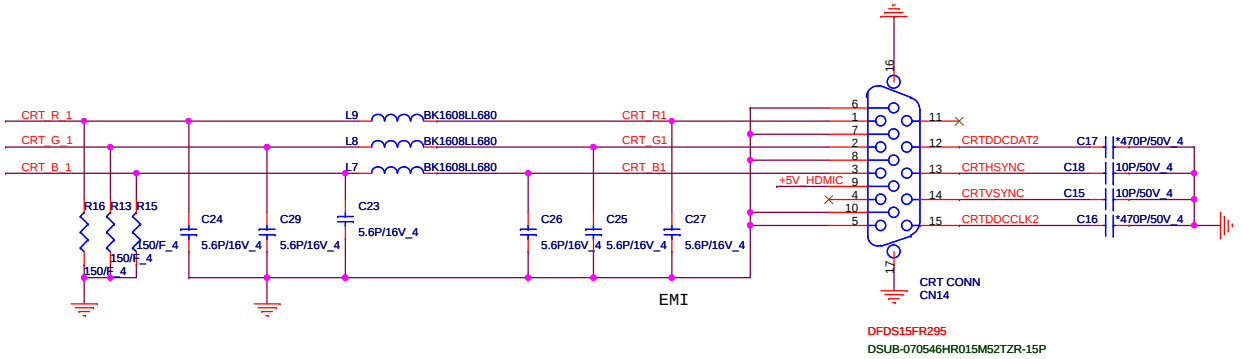
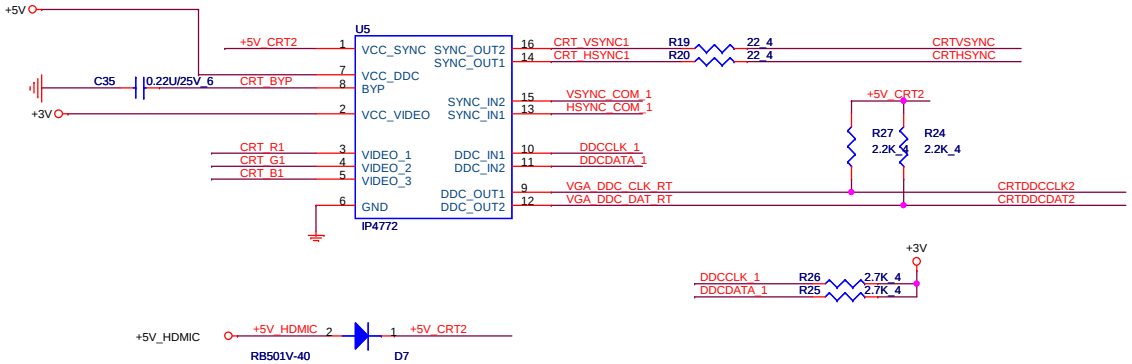
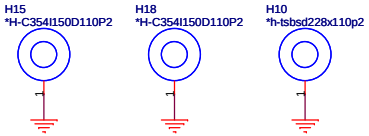
CRT PORT

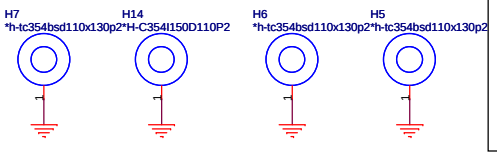


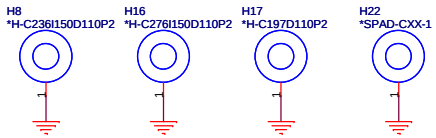


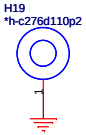


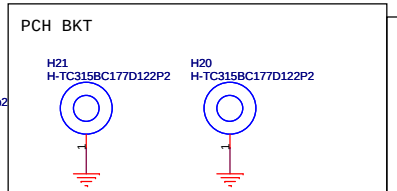
HOLE

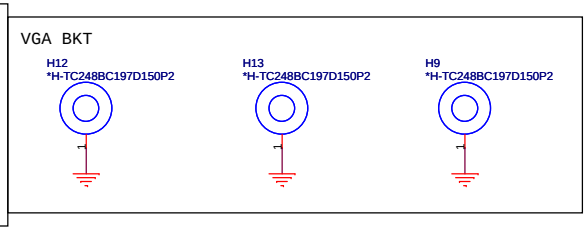


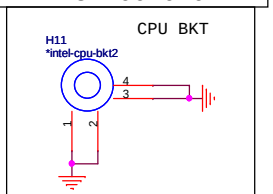












PROJECT : R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT,Hole	1A

NB5

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EMI request

+3V

C586
0.1U/10V_4

EMI request

+5V_HDMIC

C164
0.1U/10V_4

Add for EMI

+5V_HDMIC

C101
220P/50V_4

close to HDMI conn

<6> IN_CLK#
<6> IN_CLK
<6> IN_D0#
<6> IN_D0
<6> IN_D1#
<6> IN_D1
<6> IN_D2#
<6> IN_D2

IN_CLK# C141 0.1U/10V_4 C_TXC_HDMI-
IN_CLK C148 0.1U/10V_4 C_TXC_HDMI+
IN_D0# C180 0.1U/10V_4 C_TX0_HDMI-
IN_D0 C189 0.1U/10V_4 C_TX0_HDMI+
IN_D1# C157 0.1U/10V_4 C_TX1_HDMI-
IN_D1 C169 0.1U/10V_4 C_TX1_HDMI+
IN_D2# C200 0.1U/10V_4 C_TX2_HDMI-
IN_D2 C210 0.1U/10V_4 C_TX2_HDMI+

<6> SDVO_CLK
<6> SDVO_DATA

SDVO_CLK HDMI_SCL_R
SDVO_DATA HDMI_SDA_R

<6> HDMI_HPD_CON

HDMI_HPD_CON HDMI_HPD_3V

DISCRETE HDMI I2C SELECT
Close to HDMI Connector

+3V
R418 2.2K_4
HDMI_SCL_R
HDMI_SCLK
Q36 2N7002

+3V
R408 2.2K_4
HDMI_SDA_R
HDMI_SDATA
Q35 2N7002

reserve for Intel DG

+3V
R38 *1M_4
HDMI_HPD_3V
HDMI_HPD
Q9 *2N7002

+5V
R132 *0_4/S
Q13 2N7002K
R139 100K_4
C255 0.1U/10V_4

R127 680_4/F C_TX2_HDMI+
R123 680_4/F C_TX2_HDMI-
R109 680_4/F C_TX1_HDMI+
R105 680_4/F C_TX1_HDMI-
R119 680_4/F C_TX0_HDMI+
R115 680_4/F C_TX0_HDMI-
R102 680_4/F C_TXC_HDMI+
R94 680_4/F C_TXC_HDMI-

+3V
Q6 MMBT3904-7-F
HDMI_DET_R
R32 200K/F_4
HDMI_HPD
HDMI_HPD_3V
R34 10K/F_4
R399 *200K/F_4

EMI request

C_TX2_HDMI+ R126 150/F_4 C_TX2_HDMI-
C_TX1_HDMI+ R107 150/F_4 C_TX1_HDMI-
C_TX0_HDMI+ R116 150/F_4 C_TX0_HDMI-

C_TXC_HDMI+ R98 150/F_4 C_TXC_HDMI-

C_TX2_HDMI+
C_TX2_HDMI-
C_TX1_HDMI+
C_TX1_HDMI-
C_TX0_HDMI+
C_TX0_HDMI-
C_TXC_HDMI+
C_TXC_HDMI-

CN19
D2+ D2- D1+ D1- D0+ D0-
D2 Shield D1 Shield D0 Shield CK Shield GND
CK+ CK-
DDC CLK CE Remote DDC DATA NC
+5V
HP DET
SHELL1 SHELL2 SHELL2 SHELL2
HDMI CONN

HDMI_SCLK
HDMI_SDATA
1A +5V_HDMIC
FUSE1.1A8V_POLY F5
+5V
HDMI_HPD HDMI_HPD_L
*0_6/S L47
C598 220P/50V_4
VC5 *AVLC5S_4
DFHD19MR191
hdmi-2he1608-000111f-19p-ldv

reserved for EMI

C131 *10P/50V_4
HDMI_SDATA
C135 *10P/50V_4
HDMI_SCLK

+5V_HDMIC +5V_HDMIC
D10 RB501V-40
D9 RB501V-40
R90 2.2K_4
R87 2.2K_4
HDMI_SCLK
HDMI_SDATA

NB5

PROJECT : R33
Quanta Computer Inc.

Size: Custom
Document Number: HDMI CONN
Rev: 1A
Date: Wednesday, August 24, 2011
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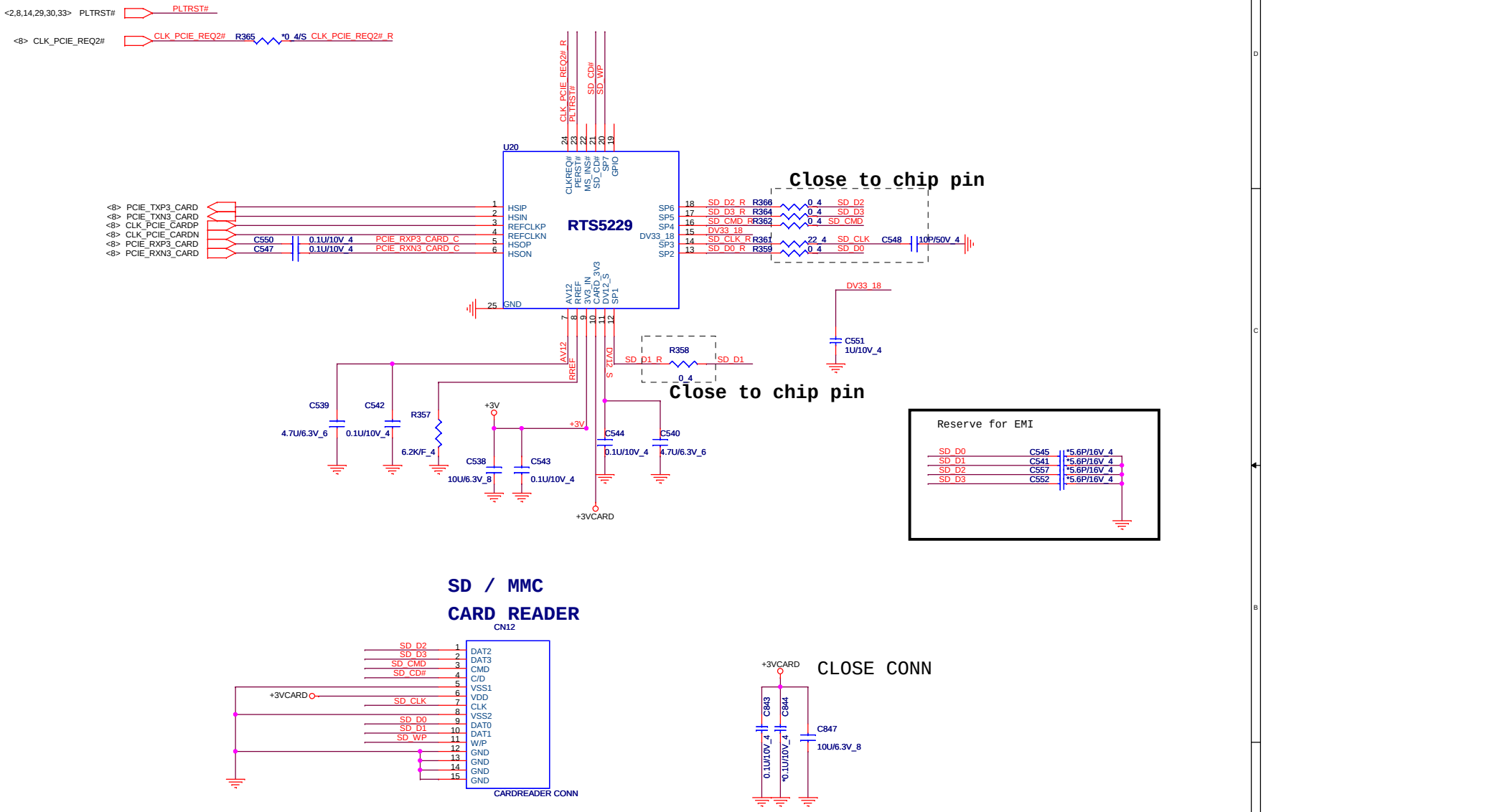
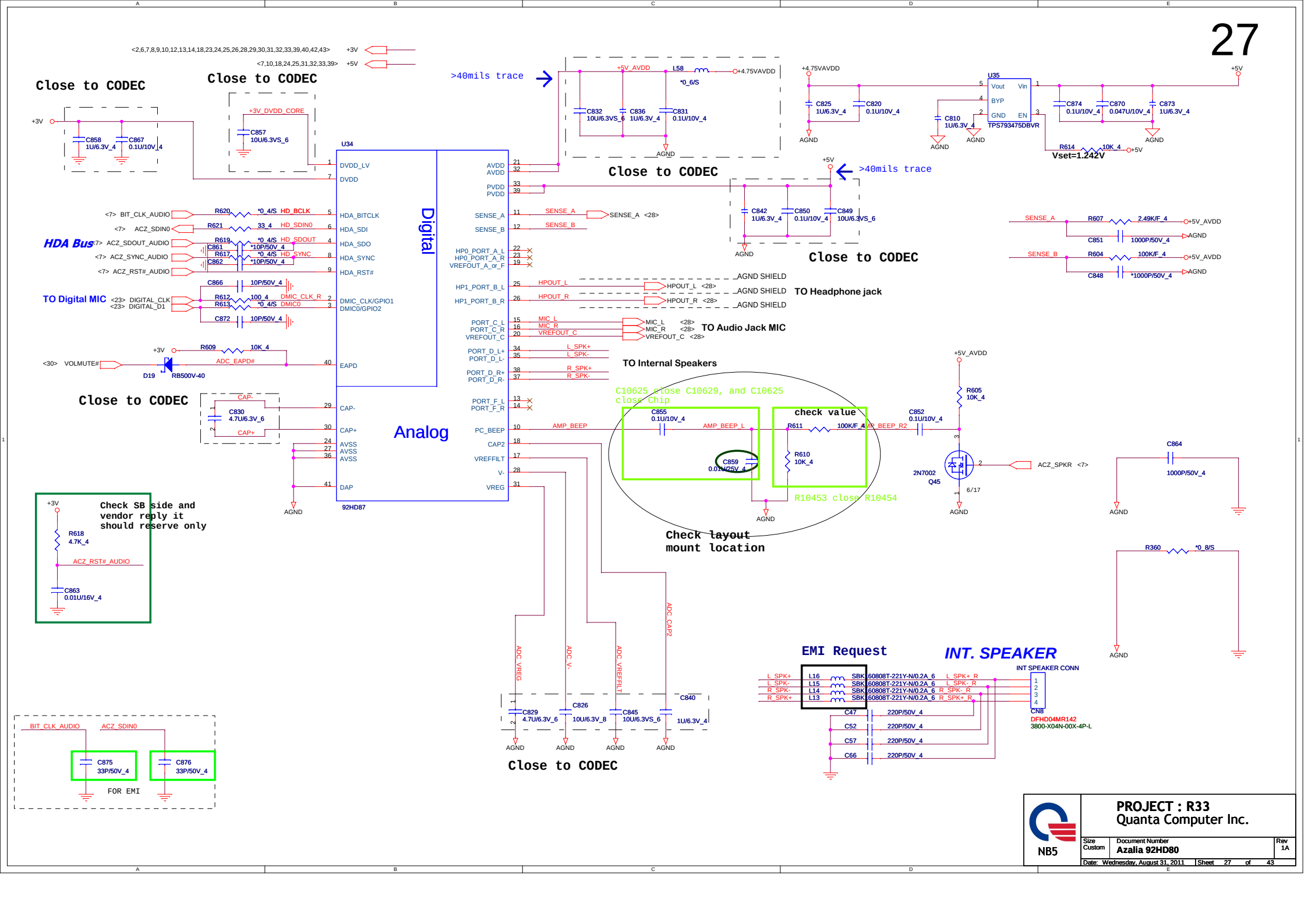


NB5	PROJECT : R33 Quanta Computer Inc.	
Size: Custom	Document Number: RTS5229 & CR SOCKET	Rev: 1A
Date: Thursday, August 25, 2011	Sheet 26 of 43	


Close to CODEC
Close to CODEC
>40mils trace
Close to CODEC
>40mils trace
Close to CODEC
Close to CODEC
Close to CODEC
Close to CODEC
HDA Bus
TO Digital MIC
TO Headphone jack
TO Audio Jack MIC
TO Internal Speakers
Digital
Analog
92HD87
U34
U35
TPS793475DBVR
Vset=1.242V
C10625 close C10629, and C10625 close Chip
check value
R10453 close R10454
Check layout mount location
Check SB side and vendor reply it should reserve only
EMI Request
INT. SPEAKER
INT SPEAKER CONN
CN8
DFHD04MR142
3800-X04N-00X-4P-L
FOR EMI
NB5
PROJECT : R33
Quanta Computer Inc.
Azalia 92HD80
Wednesday, August 31, 2011

USB3.0 X 2/USB2.0 COMBO

28

USB 3.0

EMI request

1A C739 1000P/50V_4

CN21 USB3.0 CONN

1 VBUS
2 D-
3 D+
4 GND
5 SSRX-
6 SSRX+
7 GND
8 SSTX-
9 SSTX+

+5V_USBP0

USBP0- C C407 *Clamp-Diode
USBP0+ C C412 *Clamp-Diode
USB30_TX1- C C401 *Clamp-Diode
USB30_TX1+ C C383 *Clamp-Diode
USB30_RX1- C C422 *Clamp-Diode
USB30_RX1+ C C419 *Clamp-Diode

<8> USBP0-
<8> USBP0+
R218 0_4
L36 *WCM2012-90
R221 0_4
USBP0- C
USBP0+ C

<8> USB30_RX1-
<8> USB30_RX1+
R227 0_4
L38 *WCM2012-90
R225 0_4
USB30_RX1- C
USB30_RX1+ C

<8> USB30_TX1-
<8> USB30_TX1+
C395 0.1U/10V_4
C387 0.1U/10V_4
R208 0_4
L35 *WCM2012-90
R203 0_4
USB30_TX1- R
USB30_TX1+ R
USB30_TX1- C
USB30_TX1+ C

USB 3.0

EMI request

1A C765 1000P/50V_4

CN22 USB3.0 CONN

1 VBUS
2 D-
3 D+
4 GND
5 SSRX-
6 SSRX+
7 GND
8 SSTX-
9 SSTX+

+5V_USBP0

USB30_TX2- C C457 *Clamp-Diode
USB30_TX2+ C C447 *Clamp-Diode
USBP1- C C465 *Clamp-Diode
USBP1+ C C476 *Clamp-Diode
USB30_RX2- C C479 *Clamp-Diode
USB30_RX2+ C C478 *Clamp-Diode

<8> USBP1-
<8> USBP1+
R244 0_4
L41 *WCM2012-90
R245 0_4
USBP1- C
USBP1+ C

<8> USB30_RX2-
<8> USB30_RX2+
R249 0_4
L42 *WCM2012-90
R247 0_4
USB30_RX2- C
USB30_RX2+ C

<8> USB30_TX2-
<8> USB30_TX2+
C455 0.1U/10V_4
C451 0.1U/10V_4
R243 0_4
L40 *WCM2012-90
R242 0_4
USB30_TX2- R
USB30_TX2+ R
USB30_TX2- C
USB30_TX2+ C

+5VS5
U30 80 mils (Iout=2A)
+5V_USBP0
VIN1 VIN2 EN GND
OUT3 OUT2 OUT1 OC
G547N2P81U
<30> USBPW_ON#
C793 1U/6.3V_4
C741 470P/50V_4
C740 0.1U/10V_4
C791 470P/50V_4
C787 0.1U/10V_4
C782 100U/25V

Right SIDE USBX1

USBP9- R29 *0_4 USBP9- R
USBP9+ R28 *0_4 USBP9+ R
C43 0.1U/10V_4
+5VS5
<8> USBP9-
<8> USBP9+
L12 WCM2012-90
USBPW_ON#
USBP9- R
USBP9+ R
<7> SATA_LED#
<30> PWRLED_RIGHT
+3V
SATA_LED#
C37 1000P/50V_4
PWRLED_RIGHT
C36 1000P/50V_4
<8> ACC_LED#
CN6 USB CONN
EMI request
USBPW_ON# C40 220P/50V_4

Line out

AGND SHIELD
<27> HPOUT_L
HPOUT_L
R327 16/F_4
HPOUT_L1
AGND SHIELD
<27> HPOUT_R
HPOUT_R
R313 16/F_4
HPOUT_R1
BLM18BD601SN1D L46
BLM18BD601SN1D L45
HPOUT_L2
HPOUT_R2
CN24
HP-JACK-BLACK
Normal Open
SENSE_PHONE
R317 *20K/F_4
R333 *20K/F_4
C507 1000P/50V_4
C522 1000P/50V_4
AGND
VC11 *AVLC5S_4
VC9 *AVLC5S_4
C526 0.1U/10V_4
C518 0.1U/10V_4
AGND
VC10 *AVLC5S_4
AGND
SENSE_PHONE
R312 20K/F_4
SENSE_A
SENSE_A <27>
SENSE_MIC
R283 10K/F_4
SENSE_A
VC6 *AVLC5S_4
AGND

MIC

<27> VREFOUT_C
VREFOUT_C
C486 1U/6.3V_4
AGND
R297 3.9K/F_4
R300 3.9K/F_4
<27> MIC_L
<27> MIC_R
MIC_L
MIC_R
C799 2.2U/6.3V_6
C794 2.2U/6.3V_6
MIC_L1
MIC_R1
BLM18BD601SN1D L44
BLM18BD601SN1D L43
MIC_IN_L
MIC_IN_R
C485 220P/50V_4
C491 220P/50V_4
AGND
VC7 *AVLC5S_4
VC8 *AVLC5S_4
AGND
CN23
HP-JACK-BLACK
Normal Open
SENSE_MIC

COMPONENT CHOICES:
The selection of ferrite beads can have a large effect on THD+N, causing failures versus the WLP requirements.
At this time, IDT has verified three ferrite beads that will meet the WLP performance requirements:
Murata: BLM18BD601SN1
TDK: MMZ1608Y601BTA
Taiyo Yuden: LF BK 1608HM601-T

NB5

PROJECT : R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB/BT/Audio JacK	1A
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For EMI 0 ~ 22 ohm

R54 10_4
LAN_XTAL1
XTAL1
Y5
25MHz
XTAL2
C70 33P/50V_4
C71 33P/50V_4

+3VLANVCC
+3V_LAN
C79 0.1U/10V_4
C76 0.1U/10V_4
C97 0.1U/10V_4
C85 0.1U/10V_4

GND VIA x 9 Pcs

+1.05V_LAN
R55 2.49K/F_4
LANRSET
+3V_LAN
LAN_TX#
LAN_GPIOS
R56 1K/F_4
+3V_LAN
LAN_GLINK100#

U9
RTL8105E
GND
AVDD33
AVDD33
RSET
AVDD10
CKXTAL2
CKXTAL1
AVDD33
DVDD10(NC)
DVDD33
DVDD33
GPO/SMBALERT
LED1/EESK
XTAL2
XTAL1
MDIP0
MDIN0
AVDD10
MDIP1
MDIN1
AVDD10(NC)
MDIP2(NC)
MDIN2(NC)
AVDD10(NC)
MDIP3(NC)
MDIN3(NC)
AVDD33(NC)
REGOUT
VDDREG
VDDREG
ENSWREG
EEDI
LED3/EEDO
EECS
DVDD10
LANWAKEB
DVDD33
ISOLATEB
PERSTB
DVDD10
SMBCLK(NC)
SMBDATA(NC)
CLKREQB
HSIP
HSIN
REFCLK_P
REFCLK_N
EVDD10
HSOP
HSON
GND

MDI0+
MDI0-
MDI1+
MDI1-
LAN_GLINK10# R57 10K/F_4
LAN_ECS_SCL R58 10K/F_4
PCIE_WAKE# +1.05V_LAN
PCIE_WAKE# <6,33>
+3V_LAN
ISOLATEB
PLTRST#
PLTRST# <2,8,14,26,30,33>

+3V
R62 1K_4
ISOLATEB
R60 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

U8
NS681684
LAN_MX0+
LAN_MX0-
LAN_MCT1
LAN_MX1+
LAN_MX1-
LAN_MCT0
TD+
TD-
CT
RD+
RD-
CT
TX+
CMT
TX-
RX-
CT
RX+
MDI0+
V_DAC2
MDI0-
MDI1-
V_DAC1
MDI1+

75_4 R51
C64 0.01U/100V_0603
75_4 R53
C77 0.01U/100V_0603
C46 10P/3KV_1808
C72 0.01U/25V_4

+1.05V_LAN
LAN_CLKRQ
EVDD10
PCIE_RXN2_LAN_L C107 0.1U/10V_4
PCIE_RXN2_LAN <8>
PCIE_RXP2_LAN_L C110 0.1U/10V_4
PCIE_RXP2_LAN <8>
<8> PCIE_CLKREQ_LAN#
PCIE_CLKREQ_LAN# R63 *0_4/S
<8> PCIE_TXP2_LAN
<8> PCIE_TXN2_LAN
PCIE_TXP2_LAN
PCIE_TXN2_LAN
<8> CLK_PCIE_LANP
<8> CLK_PCIE_LANN
CLK_PCIE_LANP
CLK_PCIE_LANN

+1.05V_LAN
C106 0.1U/10V_4
C78 0.1U/10V_4
C105 0.1U/10V_4
EVDD10
C90 1U/6.3V_4
C98 0.1U/10V_4

+1.05V_LAN
C93 0.1U/10V_4
C92 0.1U/10V_4
C109 0.1U/10V_4
C108 0.1U/10V_4

LAN_GLINK100#
LAN_TX#
LAN_GLED#
LAN_YLED#
C234 *1000P/50V_4
C366 *1000P/50V_4
Link

RJ45
+3V_LAN
R444 330_4
C707 1000P/50V_4
CN20
LAN_YLED
LAN_YLED#
LED_AMBER_P
LED_AMBER_N
LAN_MX1-
LAN_MX0-
LAN_MX1+
LAN_MX0+
RX1-
RX1+
RX0-
TX1-
TX1+
RX0+
TX0-
TX0+
GND1
GND
FOR EMI
R452 0_4
R422 0_4
+3V_LAN
R425 330_4
LAN_GLED
LAN_GLED#
LED_WHITE_P
LED_WHITE_N
C667 1000P/50V_4
C690 1000P/50V_4
RJ45_CONN

NB5

PROJECT : R33
Quanta Computer Inc.

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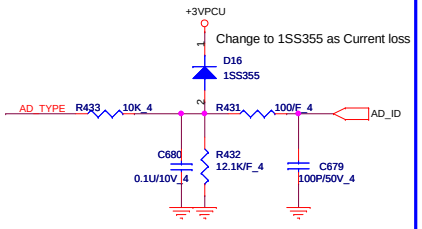
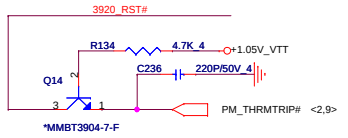
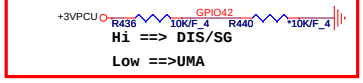
adapter Type check



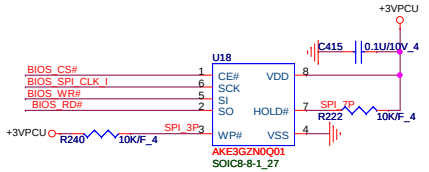


adapter select for EC

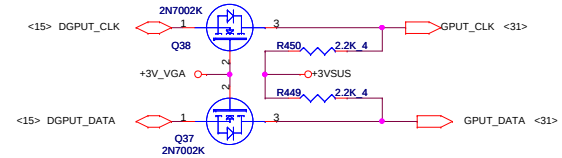


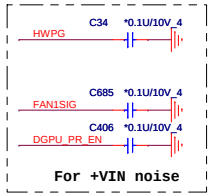
Socket: DFHS08FS023
AMIC AKE3GZP0801
EON AKE3GZN0Q01

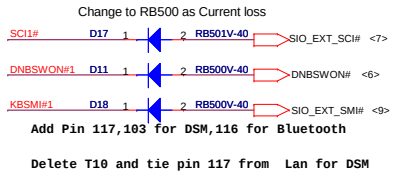
1M byte SPI EC ROM

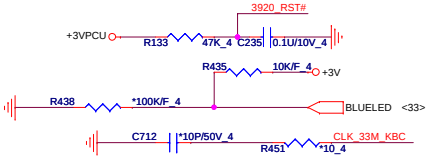


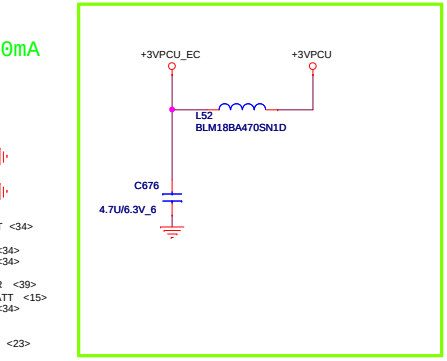
TP SM bus



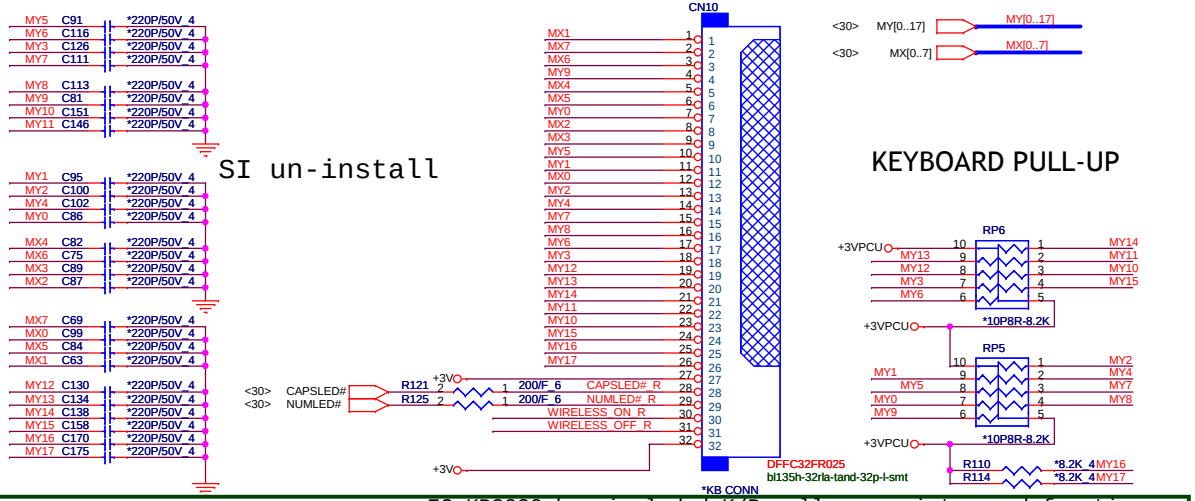




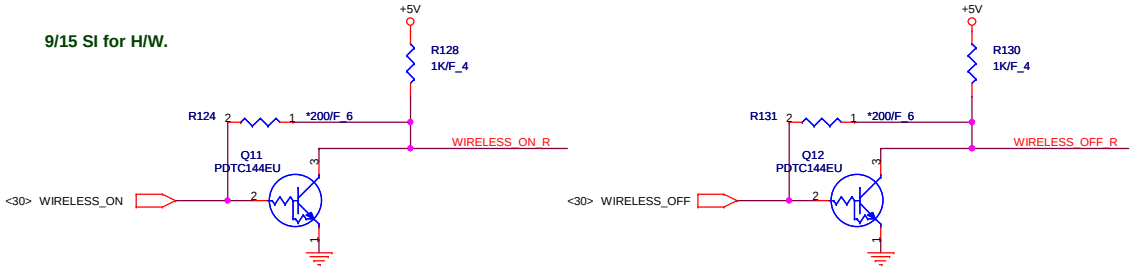




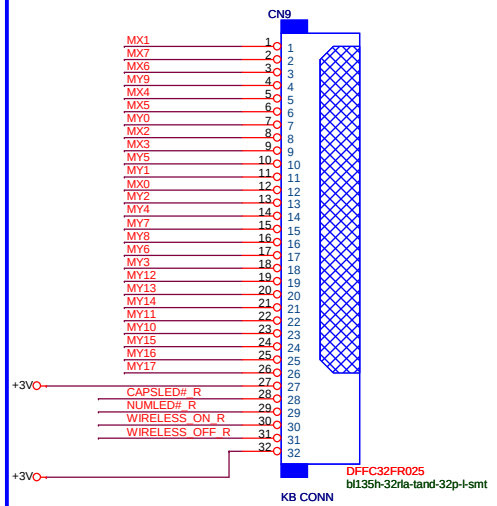
KEYBOARD Con.



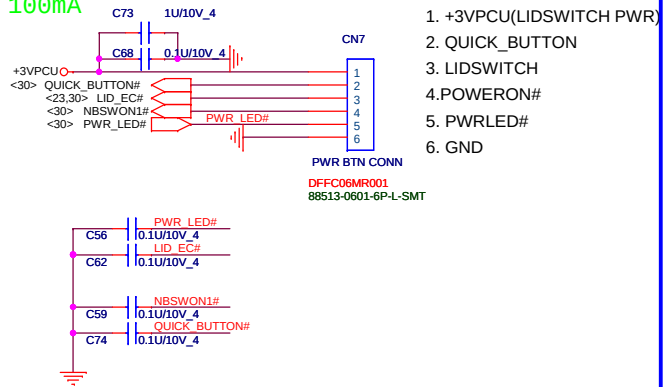
EC KB3930 has included K/B pull-up resistor and function



KEYBOARD Con.
Co-layout for 17" only



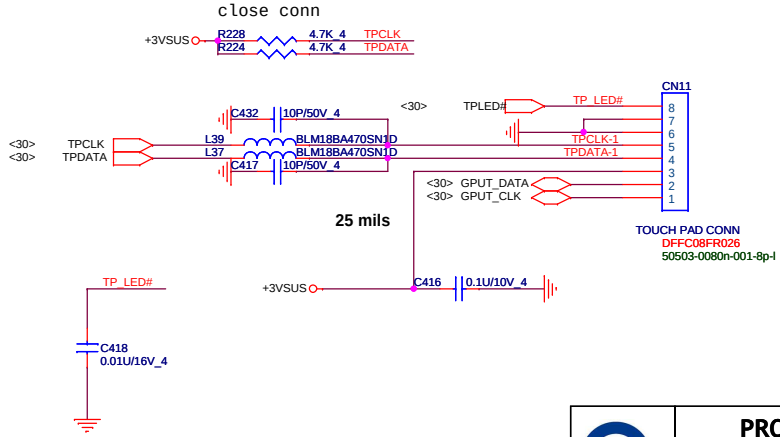
POWER BOTTON CONNECT

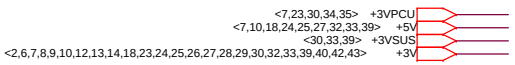


1. +3VPCU(LIDSWITCH PWR)
2. QUICK_BUTTON
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

TOUCH PAD Con.

change to +3VSUS
close conn





NB5	PROJECT : R33 Quanta Computer Inc.	
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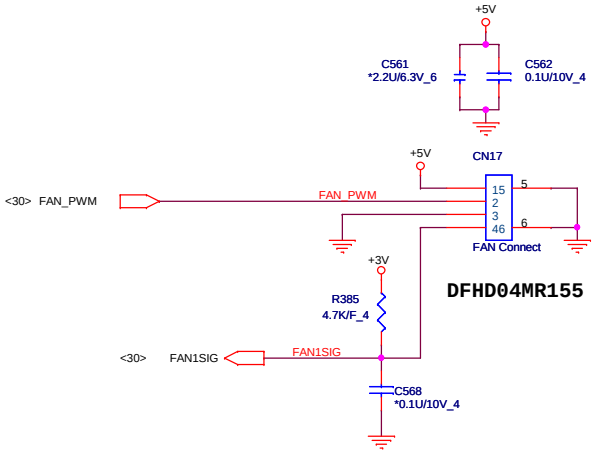
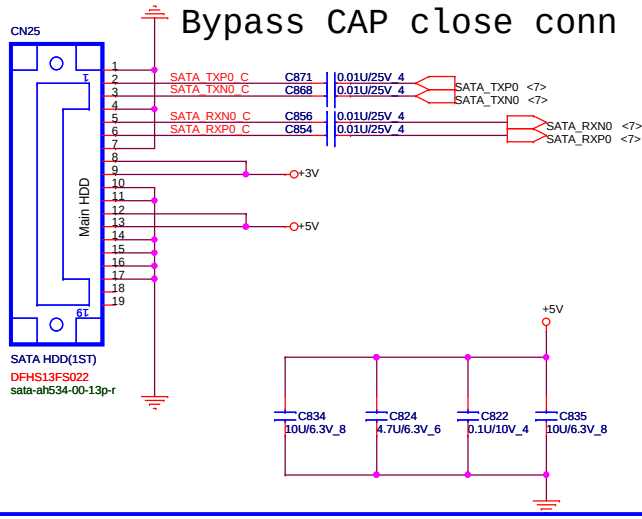
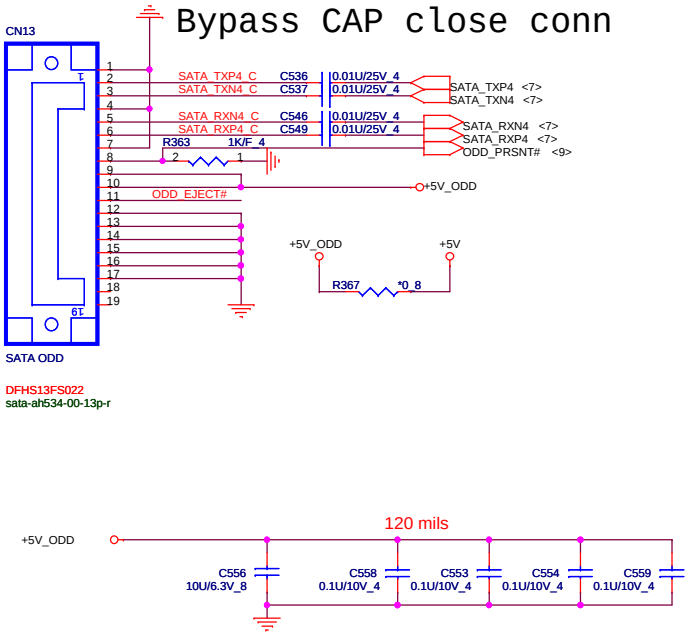
CPU FAN



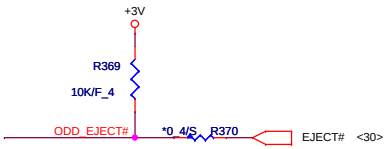
SATA HDD CONNECTOR



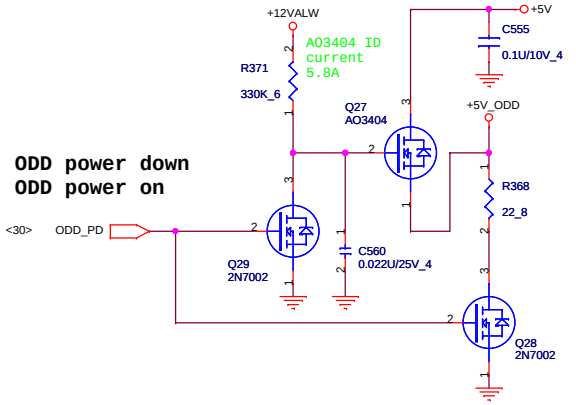
SATA ODD CONNECTOR



follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on



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	Size: Custom Document Number: HDD/ODD/FAN	Rev: 1A
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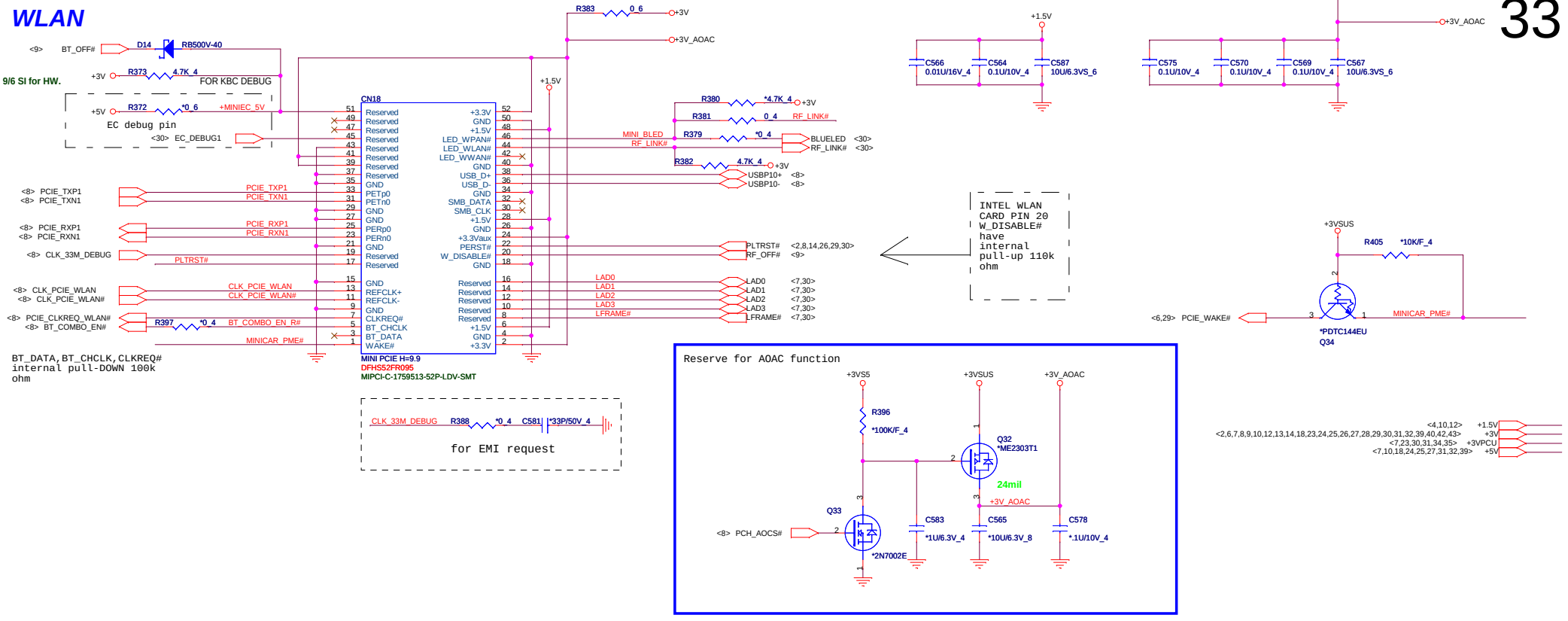
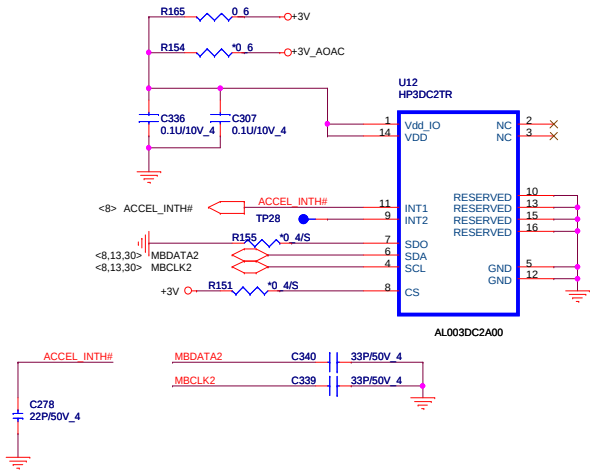
Mini PCI-E Card 1
WLAN



Accelerometer Sensor



NB5	PROJECT : R33 Quanta Computer Inc.		
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DC_JACK
90W

CN16
DC-IN CONN

To PWR LED

Do Not add test pad on BATDIS_G signal

Place this ZVS close to
Diode away +VIN

Place this ZVS close to
Far-Far away +VIN

Place this cap
close to EC

Place this cap
close to EC

Place this cap
close to EC

PU9
BQ24738

ACDET=13V

MIN. BATV=7.2V

CN15
200045MR008G10JZR
DFHD08MR175
bat-bp02081-b82d5-7h-8p-l-v

+VA
+VH28 <39>
+VAD_1 <39>
+3VPCU <7,23,30,31,35>
+5VPCU <35>
+BATCHG

NB5

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Quanta Computer Inc.

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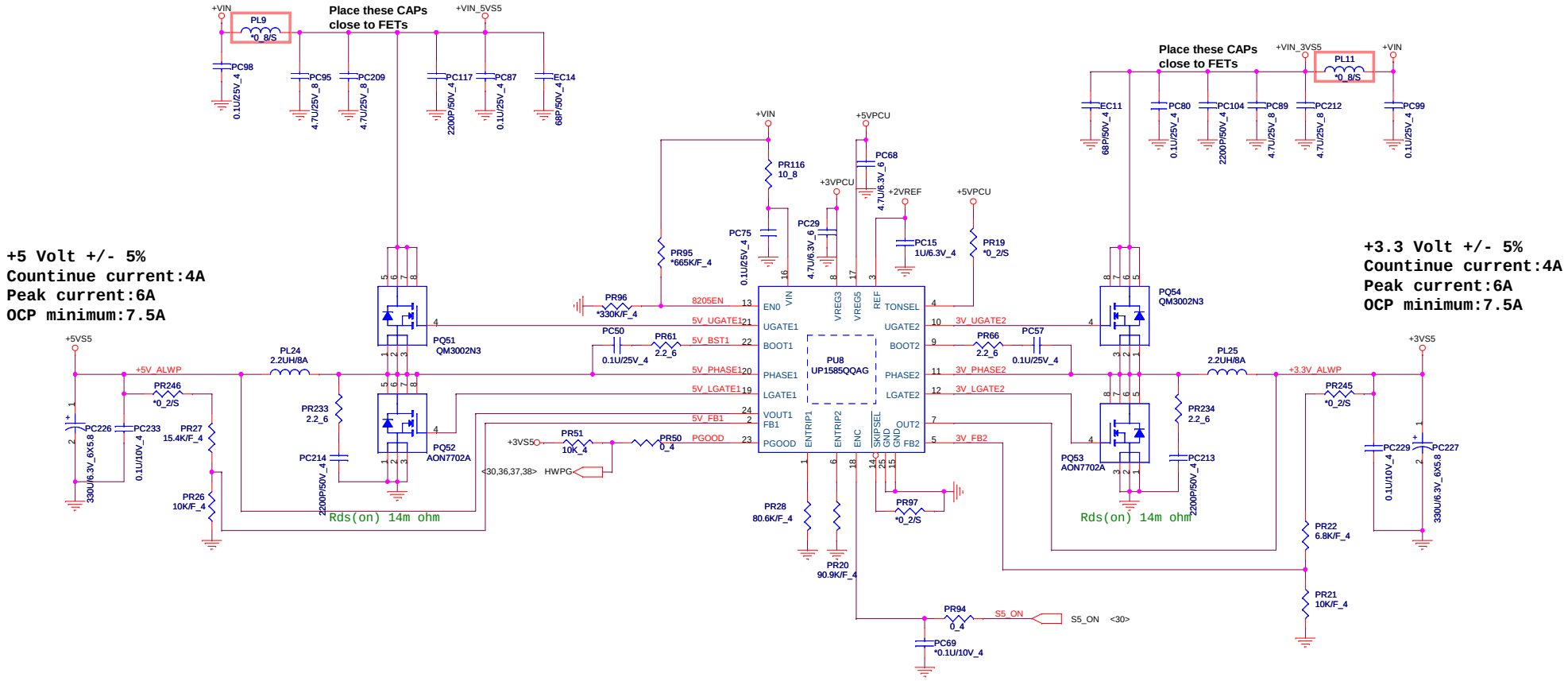

NB5	PROJECT : R33 Quanta Computer Inc.	
Size: Custom	Document Number: 3/5VPCU(RT8223P)	Rev: 1A
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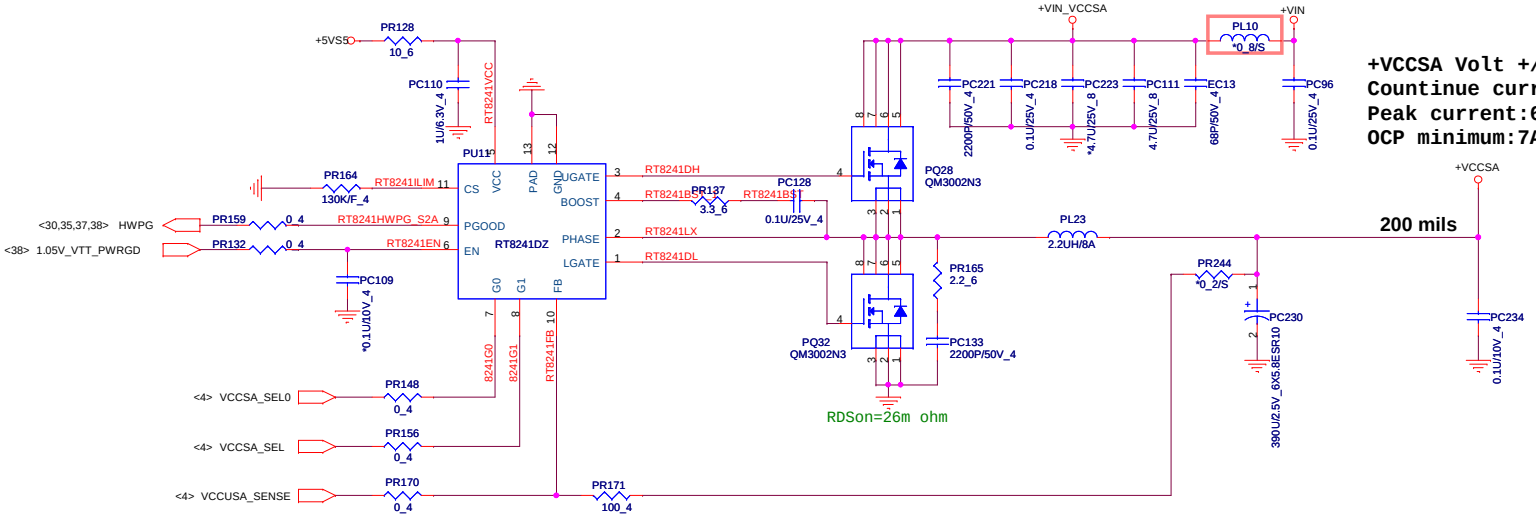
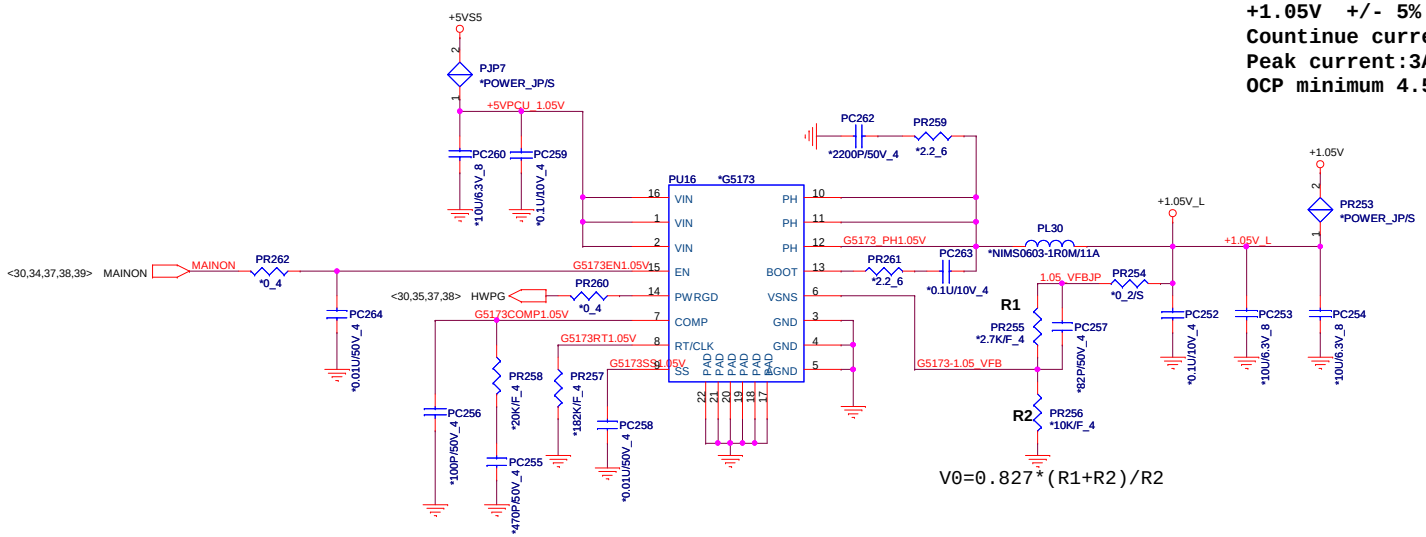


+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A

CPU system agent
voltage slew rate of 0.5 -10 mV/µs

H_FC_C22 VID0	VCCSA_SEL VID1	Vout
0	0	0.9V
0	1	0.80V (SV-RT8241DZGQW) 0.85V (LV-RT8241EZGQW)
1	0	0.725V
1	1	0.675V



+1.05V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

NB5

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Quanta Computer Inc.

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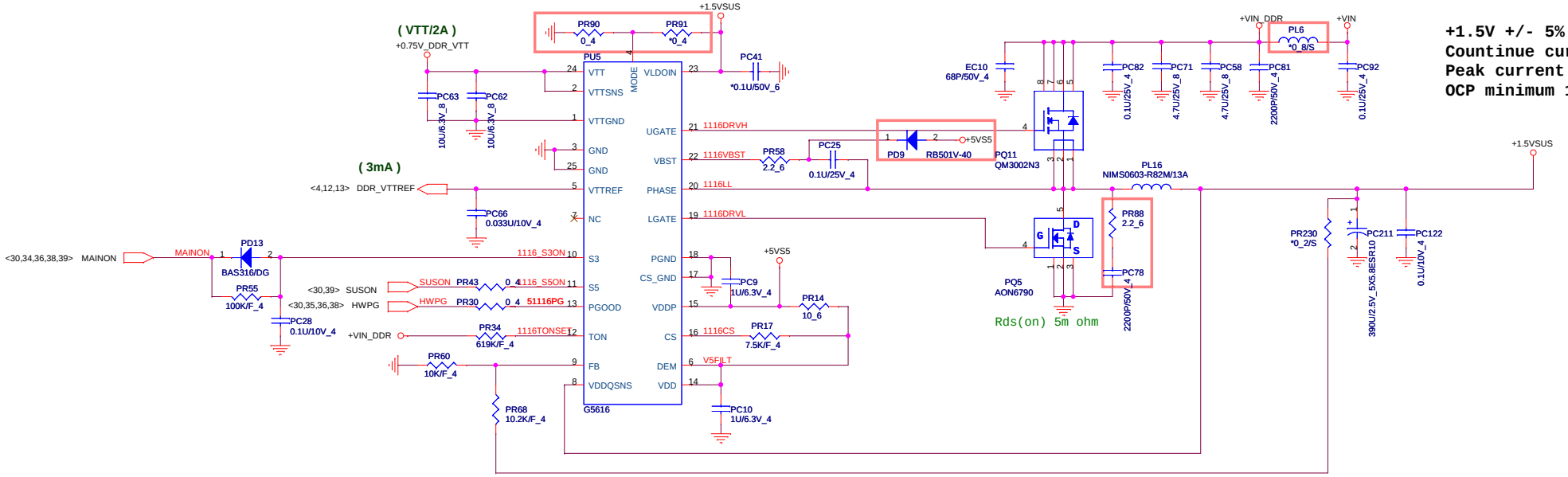

+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum 15A

NB5	**PROJECT : R33** Quanta Computer Inc.	
Size: Custom	Document Number: DDRIII(RT8207LGQW)	Rev: 1A
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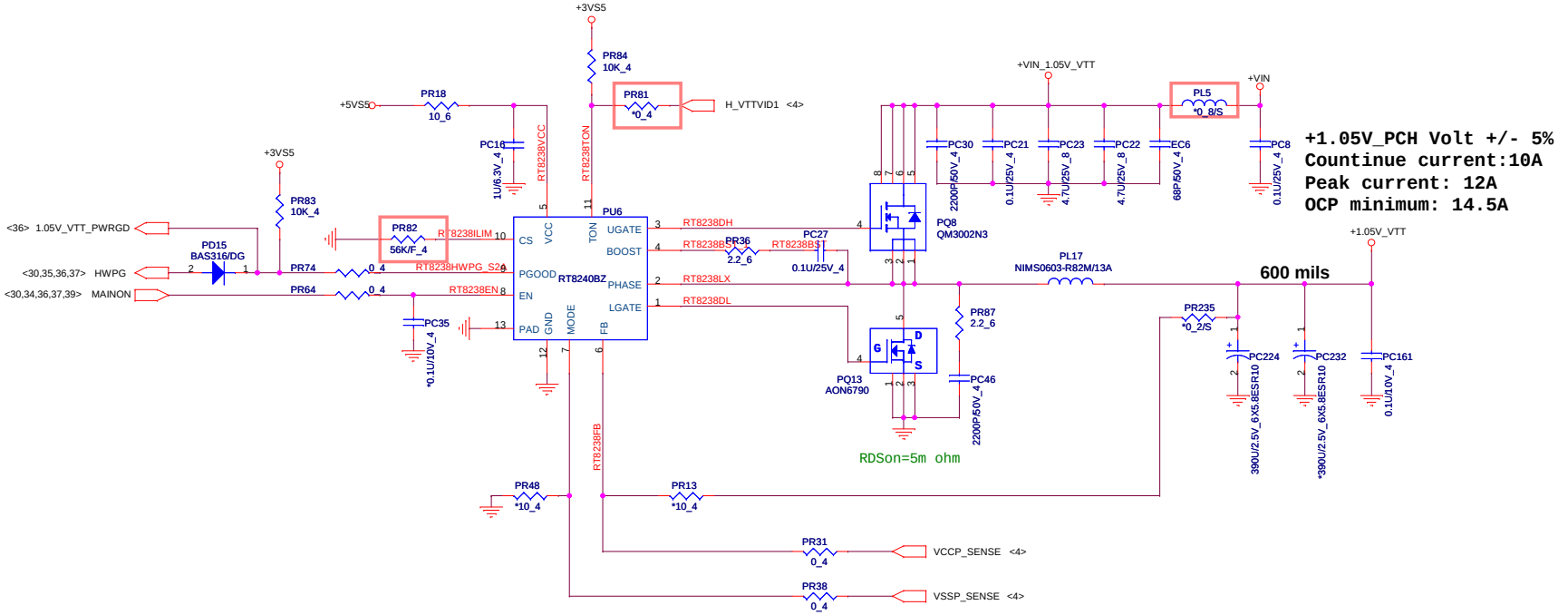
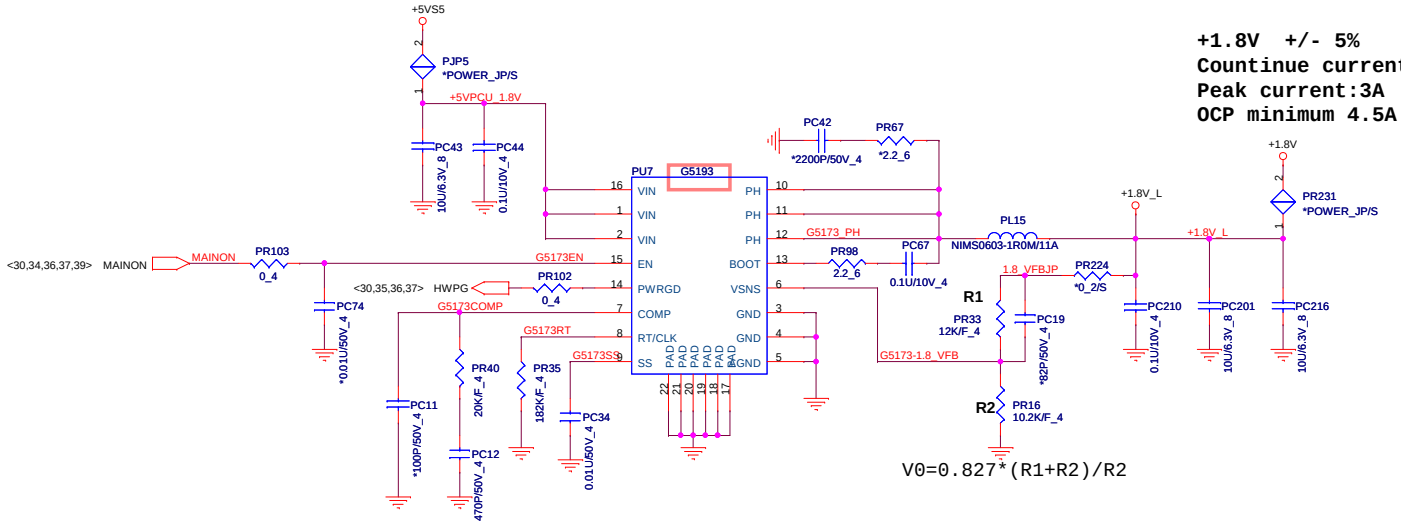
1.05V_VTT





NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.0V(RT8228BZ)/1.8V(G5173)	1A
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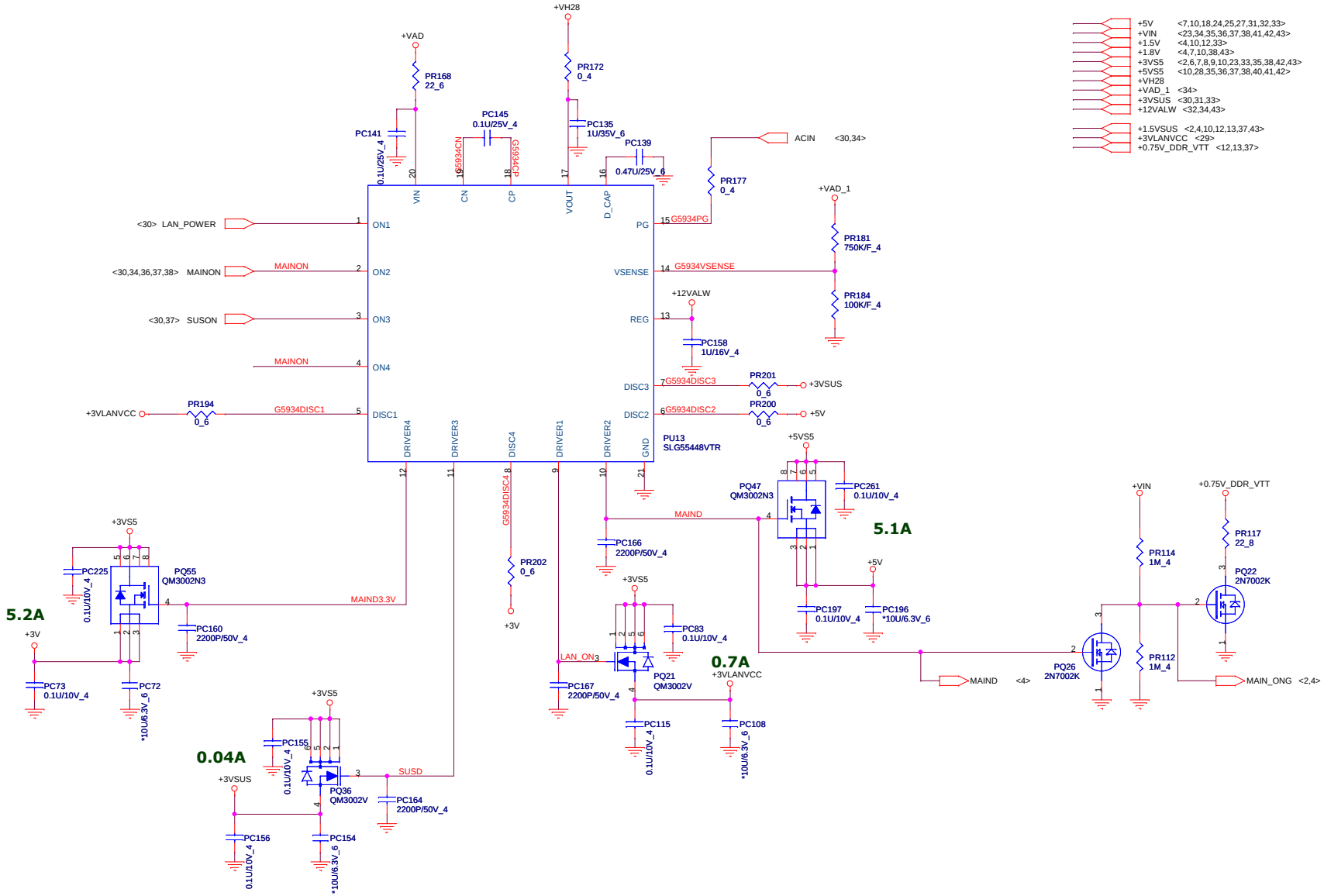

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A

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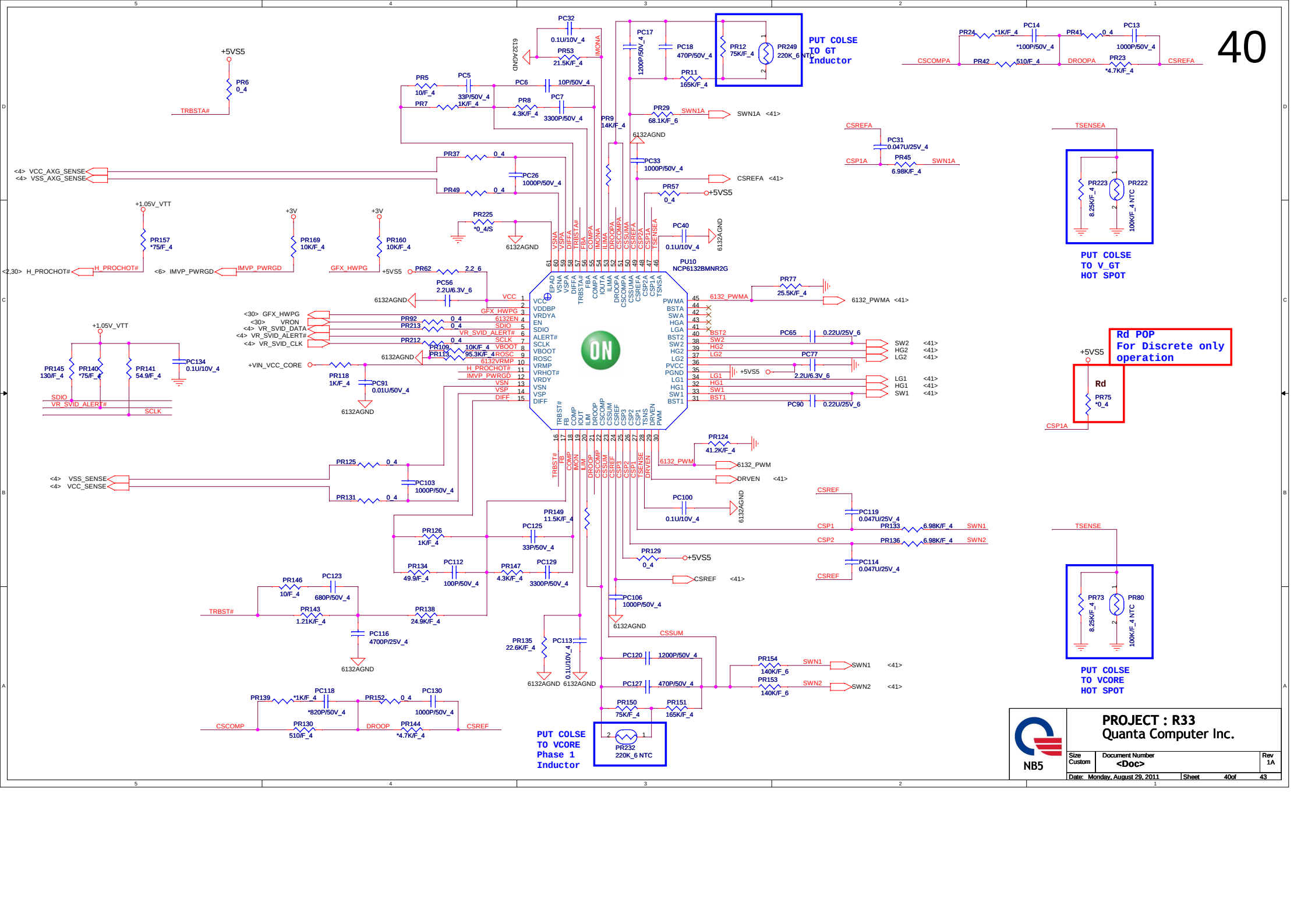
40
PU10
NCP6132BMNR2G
PUT COLSE TO GT Inductor
PUT COLSE TO V_GT HOT SPOT
PUT COLSE TO VCORE HOT Phase 1 Inductor
PUT COLSE TO VCORE HOT SPOT
Rd POP For Discrete only operation
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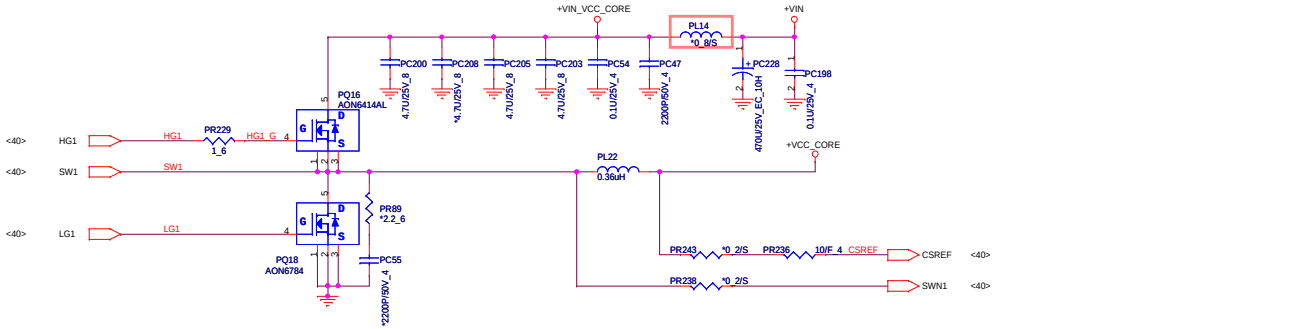
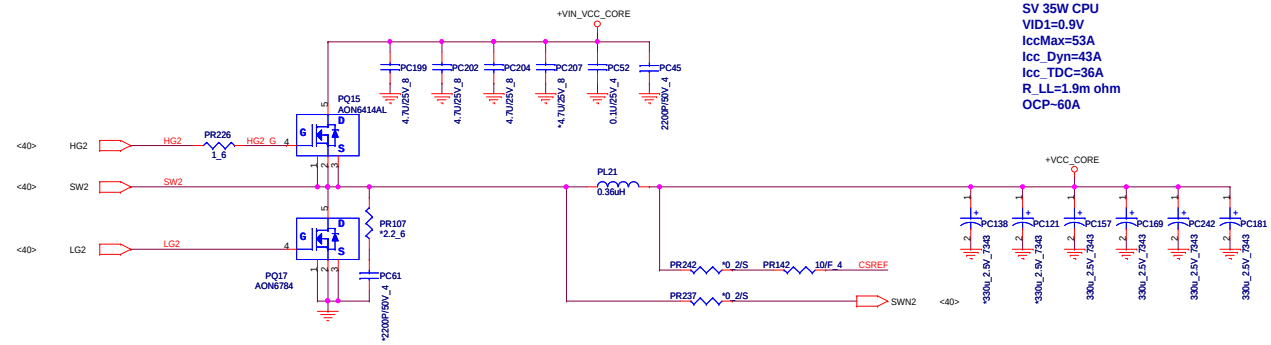
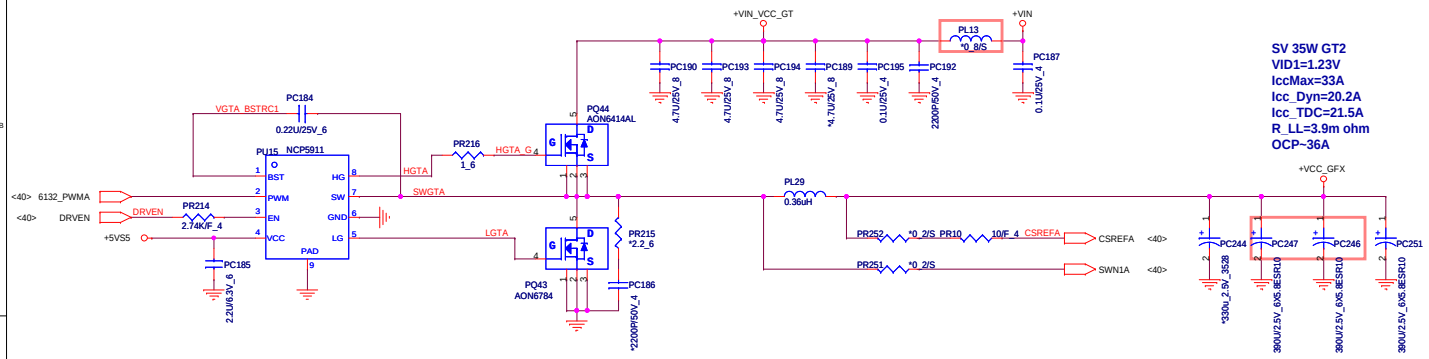




SV 35W CPU
VID1=0.9V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~60A



SV 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~36A

NB5	PROJECT : R33 Quanta Computer Inc.		
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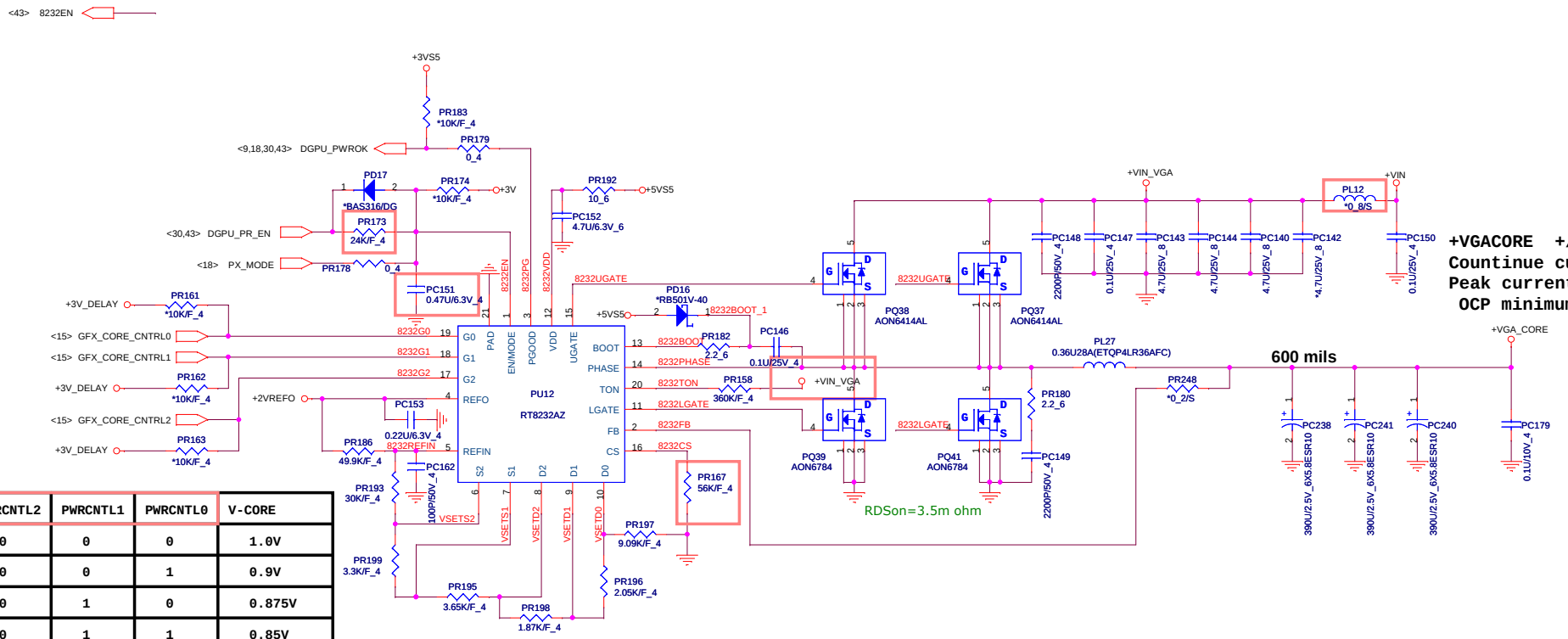
VGA Core



thames xt	PWRCNTL2	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

NB5	PROJECT : R33 Quanta Computer Inc.	
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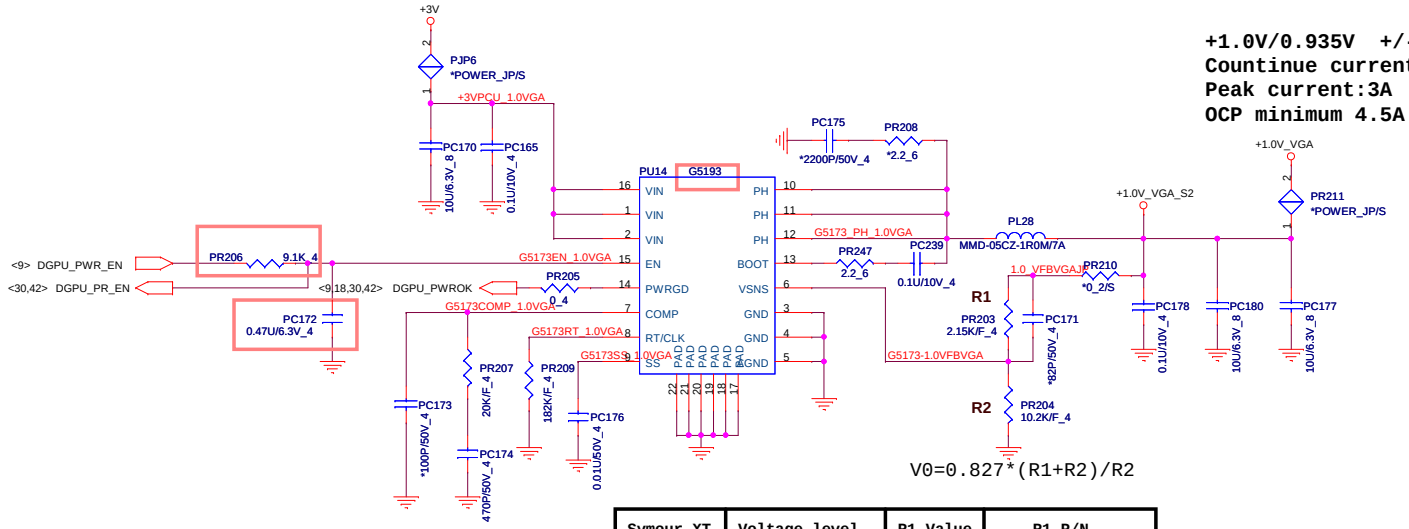
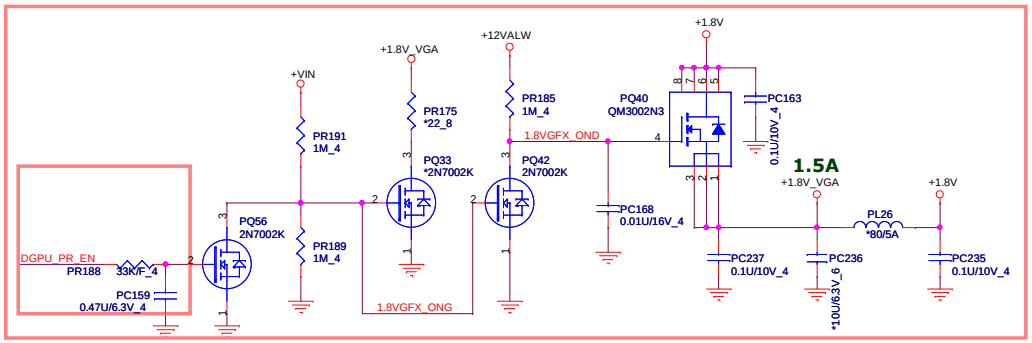
+1.0V/0.935V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

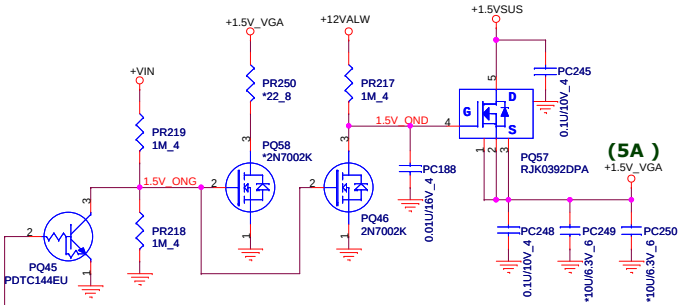
+3V <2,6,7,8,9,10,12,13,14,18,23,24,25,27,28,29,30,31,32,33,39,40,42>
+VIN <23,34,35,36,37,38,39,41,42>
+1.8V <4,7,10,38>
+3VS5 <2,6,7,8,9,10,23,33,35,38,39,42>
+5VS5 <10,28,35,36,37,38,39,40,41,42>
+3V_VGA <18>
+12VALW <32,34,39>
+1.5VSUS <2,4,10,12,13,37>
+1.5V_VGA <18,20,21,22>
+1.8V_VGA <15,16,18,19>
+3V_DELAY <15,17,18,42>
+VGA_CORE <18,42>

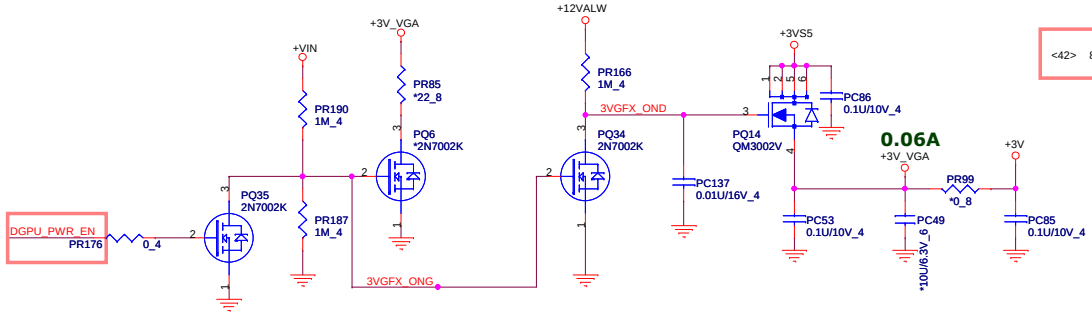


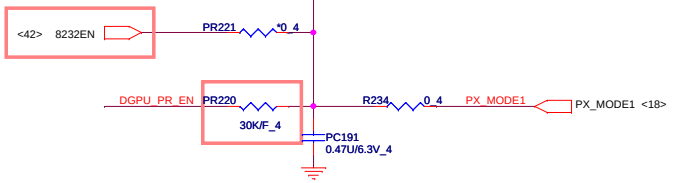
V0=0.827*(R1+R2)/R2

Symour-XT	Voltage level	R1 Value	R1 P/N
17W	1.0V	2.15K	CS22152FB07
25W	0.935V	1.37K	CS21372FB19









NB5

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Quanta Computer Inc.

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