Compal Confidential

QIWG5/QIWG6 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

nVIDIA N13X

2012-02-01

LA-7981P

REV:1.0

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: LA-7981P	Rev: 1.0
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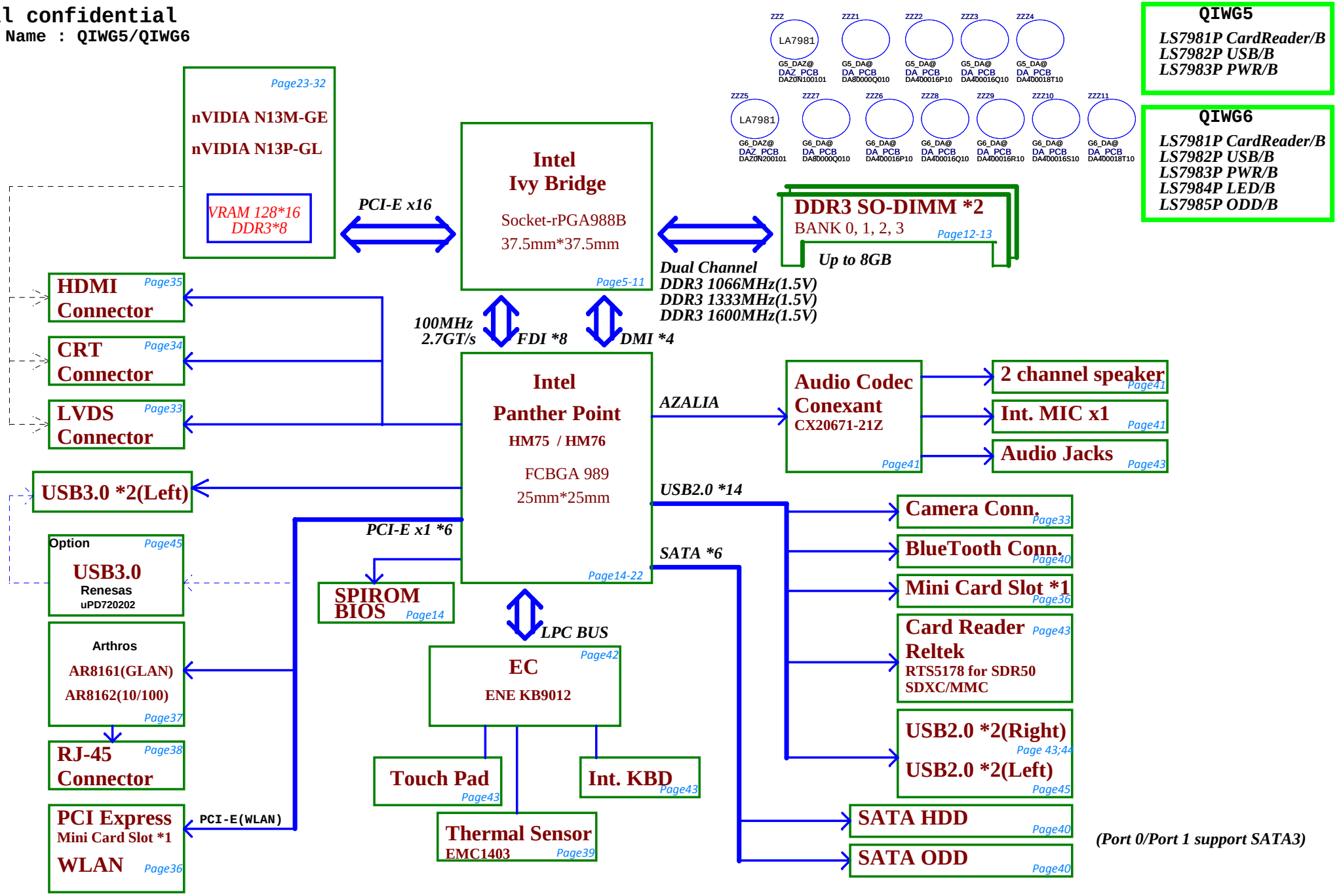
Compal confidential
File Name : QIWG5/QIWG6



Security Classification	Compal Secret Data		
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Title	Block Diagram		
Size Custom	Document Number LA-7981P		Rev 1.0
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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB Port (Right Side CR-BD)
	UHCI1	2	USB Port (Left Side) USB3.0
		3	USB Port (Left Side) USB3.0
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB/B (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
GPU:N13P-GL	N13P@
GPU:N13M-GE	N13M@
HDMI	HDMI@
Interna-Intel-USB3.0	IU3@
External-NEC-USB3.0	EU3@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8162@
GIGA LAN	GIGA@
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
Cameara	CMOS@
For QIWG5 (14")	14@
For QIWG6 (15")	15@
Unpop	@
G5/G6/G9(Low/Mid END)	nonBBH@
G9 High-END	BBH@
G9	G9 @
G5/G6/G9(Low/Mid END)	15_nonBBH@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

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Title: Notes List

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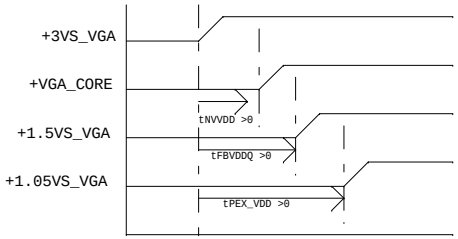
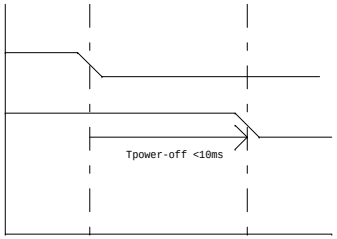
Hot plug detect for IFP link C

VGA and GDDR3 Voltage Rails (N13x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN		Hot plug detect for IFP link C
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		Hot Plug Detect for IFPE
GPIO19	IN	N/A	



1. all power rail ramp up time should be larger than 40us
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ



1.all GPU power rails should be turned off within 10ms

Performance Mode P0 TDP at Tj = 102 C* (GDDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13P-GL 64bit 1GB GDDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GL (28nm)	??
N13M-GE (28nm)	???

GPU	FB Memory (GDDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N13P-GL N13M-GE	Samsung 2500MHz	K4G10325FG-HC04						
		32Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 2500MHz	H5GQ1H24BFR-T2C						
		32Mx32	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
	Samsung 2500MHz	K4G20325FG-HC04						
		64Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 2500MHz	H5GQ2H24MFR-T2C						
		64Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K

X76

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Title: VGA Notes List

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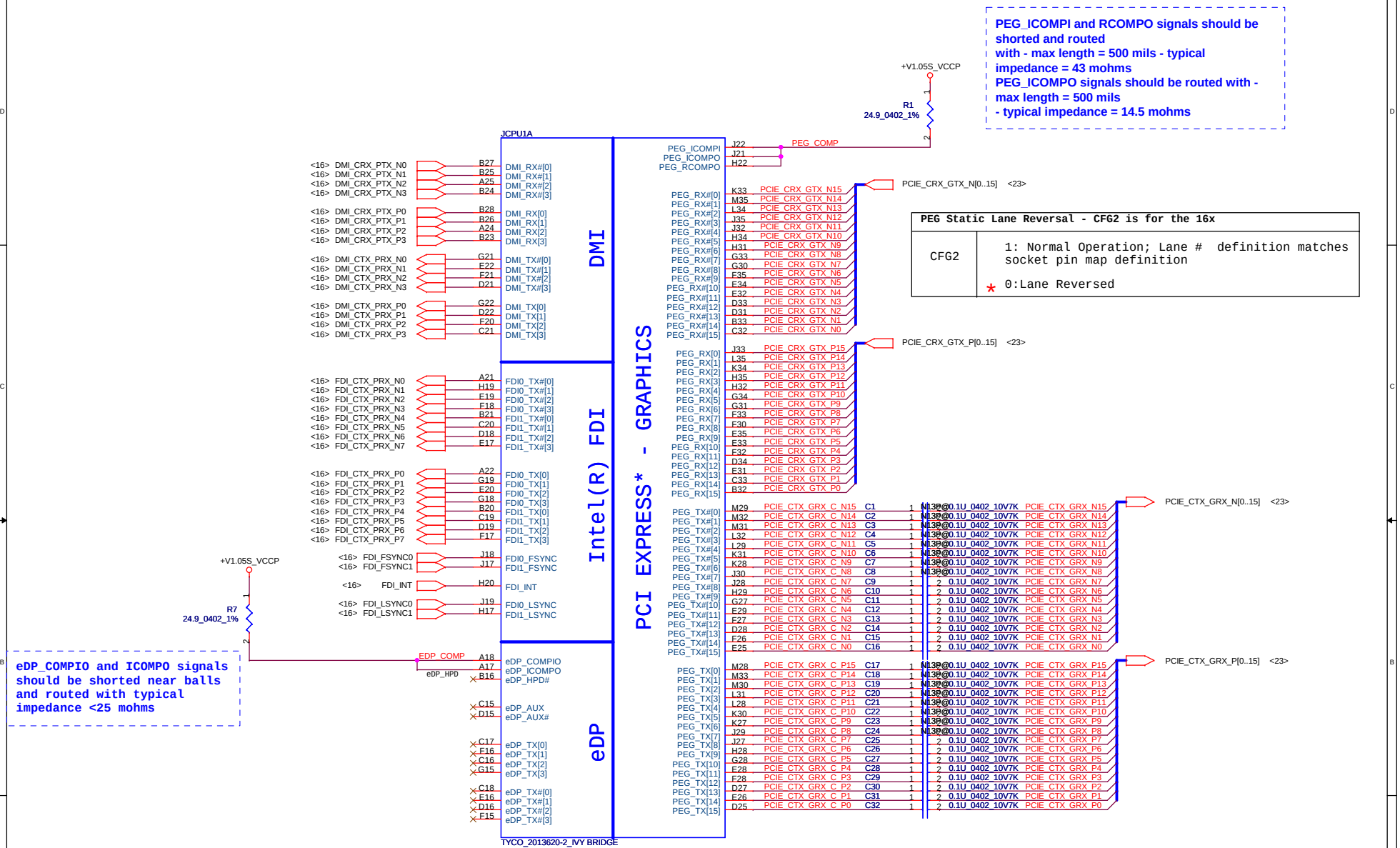

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Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
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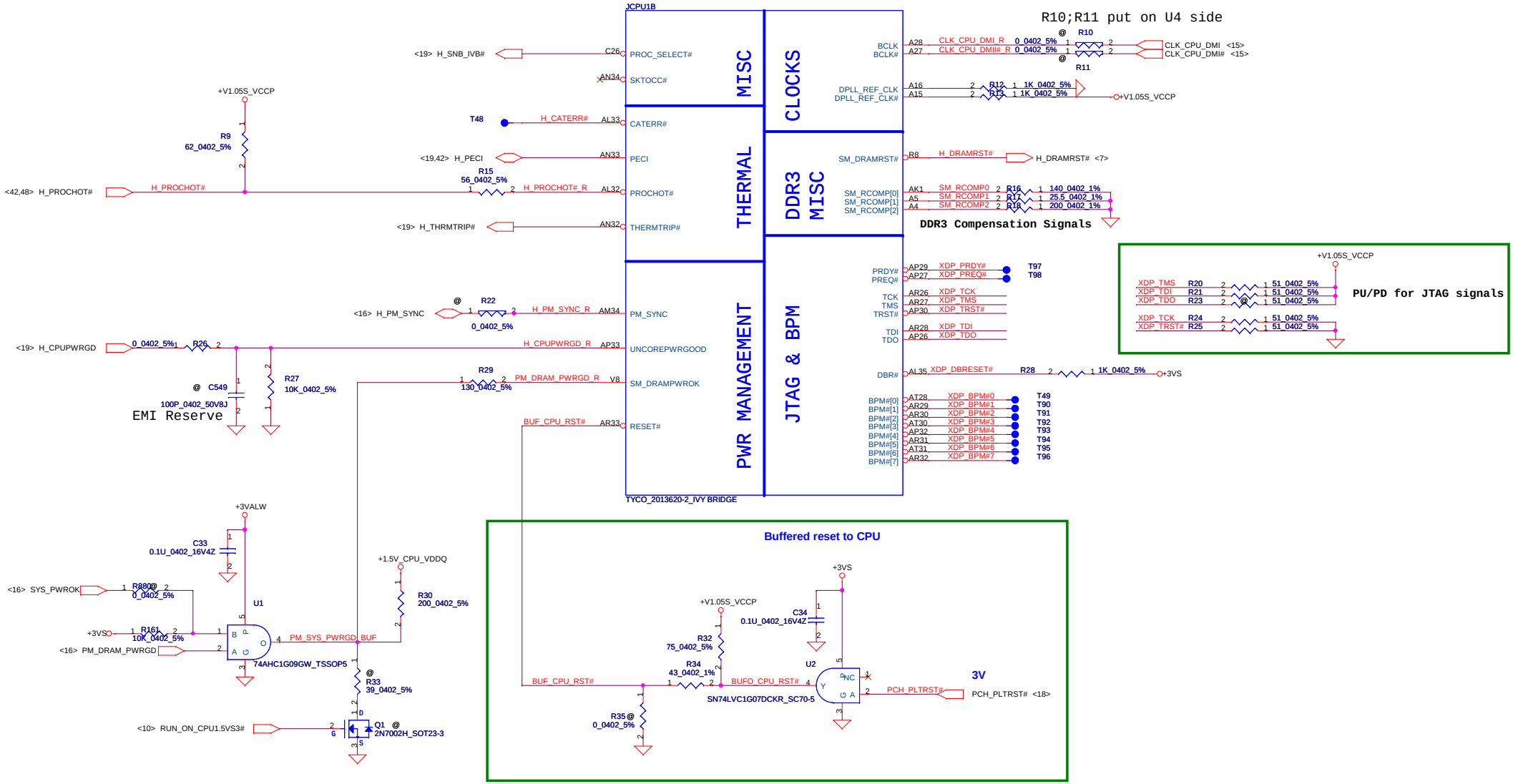

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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Title	PROCESSOR(2/7) PM,XDP,CLK		
Size: Custom	Document Number: LA-7981P		Rev: 0.2
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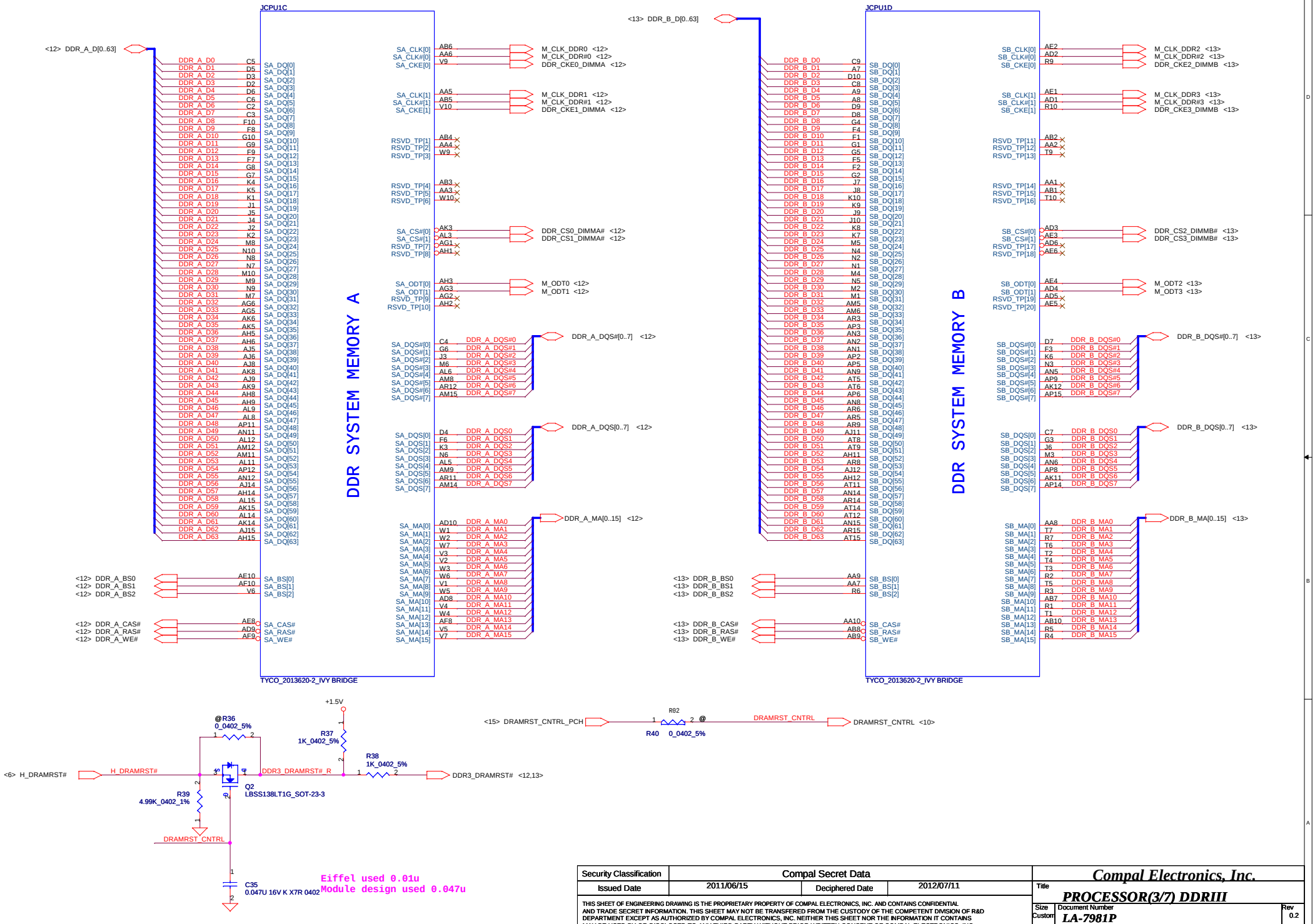

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Title: PROCESSOR(3/7) DDRIII

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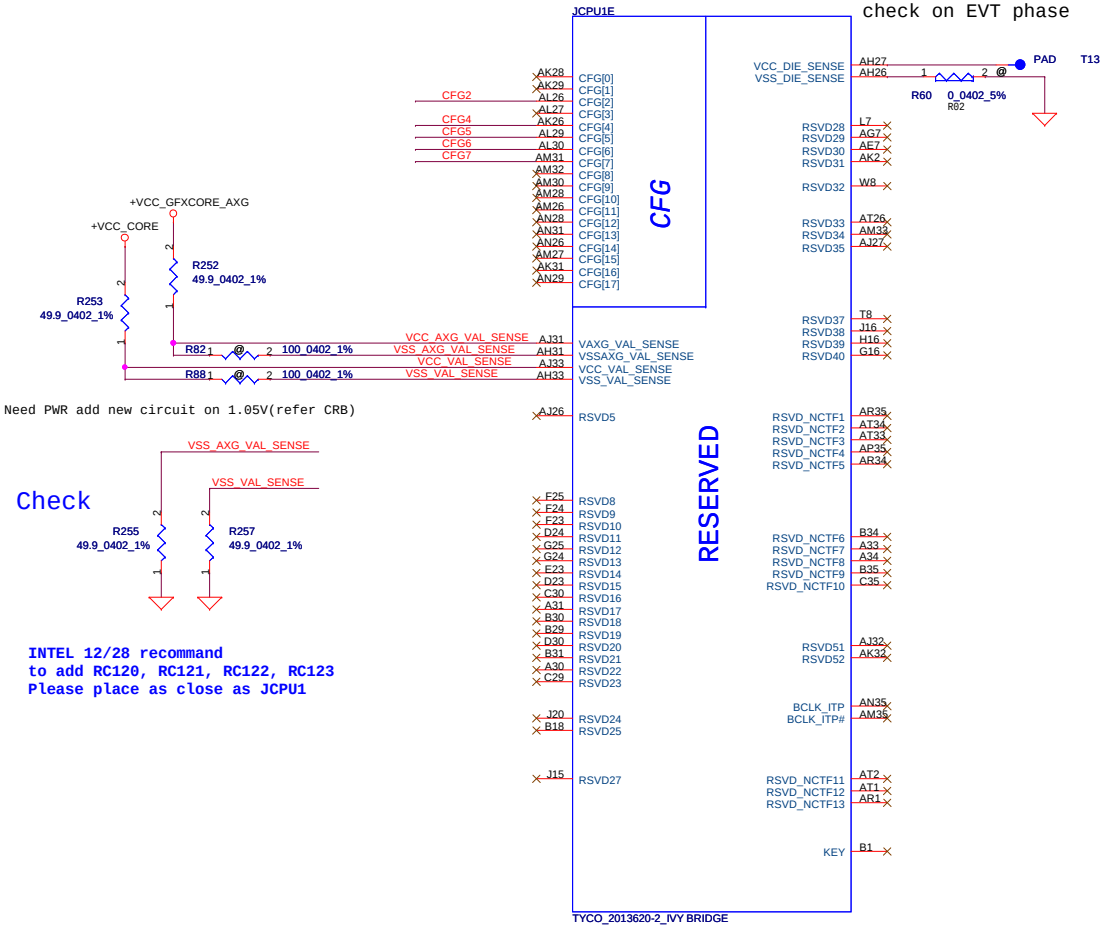
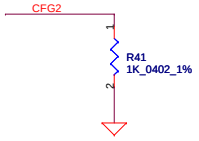
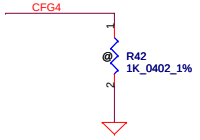
CFG Straps for Processor



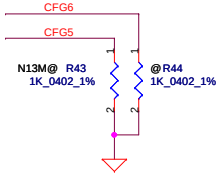
Interl request AH26 short GND
check on EVT phase



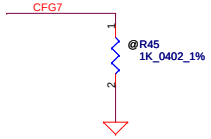
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

+V1.05S_VCCP

8.5A

CORE SUPPLY

VCC1 AG35, VCC2 AG34, VCC3 AG33, VCC4 AG32, VCC5 AG31, VCC6 AG30, VCC7 AG29, VCC8 AG28, VCC9 AG27, VCC10 AG26, VCC11 AF35, VCC12 AF34, VCC13 AF33, VCC14 AF32, VCC15 AF31, VCC16 AF30, VCC17 AF29, VCC18 AF28, VCC19 AF27, VCC20 AF26, VCC21 AD35, VCC22 AD34, VCC23 AD33, VCC24 AD32, VCC25 AD31, VCC26 AD30, VCC27 AD29, VCC28 AD28, VCC29 AD27, VCC30 AD26, VCC31 AC35, VCC32 AC34, VCC33 AC33, VCC34 AC32, VCC35 AC31, VCC36 AC30, VCC37 AC29, VCC38 AC28, VCC39 AC27, VCC40 AC26, VCC41 AA35, VCC42 AA34, VCC43 AA33, VCC44 AA32, VCC45 AA31, VCC46 AA30, VCC47 AA29, VCC48 AA28, VCC49 AA27, VCC50 AA26, VCC51 V35, VCC52 Y34, VCC53 Y33, VCC54 Y32, VCC55 Y31, VCC56 Y30, VCC57 Y29, VCC58 Y28, VCC59 Y27, VCC60 Y26, VCC61 V35, VCC62 V34, VCC63 V33, VCC64 V32, VCC65 V31, VCC66 V30, VCC67 V29, VCC68 V28, VCC69 V27, VCC70 V26, VCC71 U35, VCC72 U34, VCC73 U33, VCC74 U32, VCC75 U31, VCC76 U30, VCC77 U29, VCC78 U28, VCC79 U27, VCC80 U26, VCC81 R35, VCC82 R34, VCC83 R33, VCC84 R32, VCC85 R31, VCC86 R30, VCC87 R29, VCC88 R28, VCC89 R27, VCC90 R26, VCC91 P35, VCC92 P34, VCC93 P33, VCC94 P32, VCC95 P31, VCC96 P30, VCC97 P29, VCC98 P28, VCC99 P27, VCC100 P26

PEG AND DDR

VCCIO1 AH13, VCCIO2 AH10, VCCIO3 AG10, VCCIO4 AC10, VCCIO5 Y10, VCCIO6 U10, VCCIO7 P10, VCCIO8 L10, VCCIO9 J14, VCCIO10 J13, VCCIO11 J12, VCCIO12 J11, VCCIO13 H14, VCCIO14 H12, VCCIO15 H11, VCCIO16 G14, VCCIO17 G13, VCCIO18 G12, VCCIO19 F14, VCCIO20 F13, VCCIO21 F12, VCCIO22 F11, VCCIO23 E14, VCCIO24 E12, VCCIO25 E11, VCCIO26 D14, VCCIO27 D13, VCCIO28 D12, VCCIO29 D11, VCCIO30 C14, VCCIO31 C13, VCCIO32 C12, VCCIO33 C11, VCCIO34 B14, VCCIO35 B12, VCCIO36 A14, VCCIO37 A13, VCCIO38 A12, VCCIO39 A11, VCCIO40 J23

SVID

+V1.05S_VCCP

C99 0.1U_0402_10V6K

R46 75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT# AJ29 H_CPU_SVIDALRT# — R47 43_0402_5% — VR_SVID_ALRT# <55>
VIDSCLK AJ30 H_CPU_SVIDCLK — 0_0402_5% — R48 @ — VR_SVID_CLK <55>
VIDSOUT AJ28 H_CPU_SVIDDAT — 0_0402_5% — R49 @ — VR_SVID_DAT <55>

R50 130_0402_5% +V1.05S_VCCP

0.1uF on power side

SENSE LINES

VCC_SENSE AJ35 VCCSENSE_R — R52 @0_0402_5% — VCCSENSE <55>
VSS_SENSE AJ34 VSSSENSE_R — R53 @0_0402_5% — VSSSENSE <55>

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

+VCC_CORE

R51 100_0402_1%

R54 100_0402_1%

R66 @ 100_0402_1%

VCCIO_SENSE B10
VSS_SENSE_VCCIO A10
VSSIO_SENSE_L — R74 10_0402_1% @ — VSSIO_SENSE
VCCIO_SENSE <52,53>

R74 & R79 put together

R79 10_0402_1% +V1.05S_VCCP

VSSIO_SENSE_L <53>

VSS_SENCE 100ohm +-1% pull-down to GND near processor

TYCO_2013620-2_IVY BRIDGE

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Title: PROCESSOR(5/7) PWR,BYPASS

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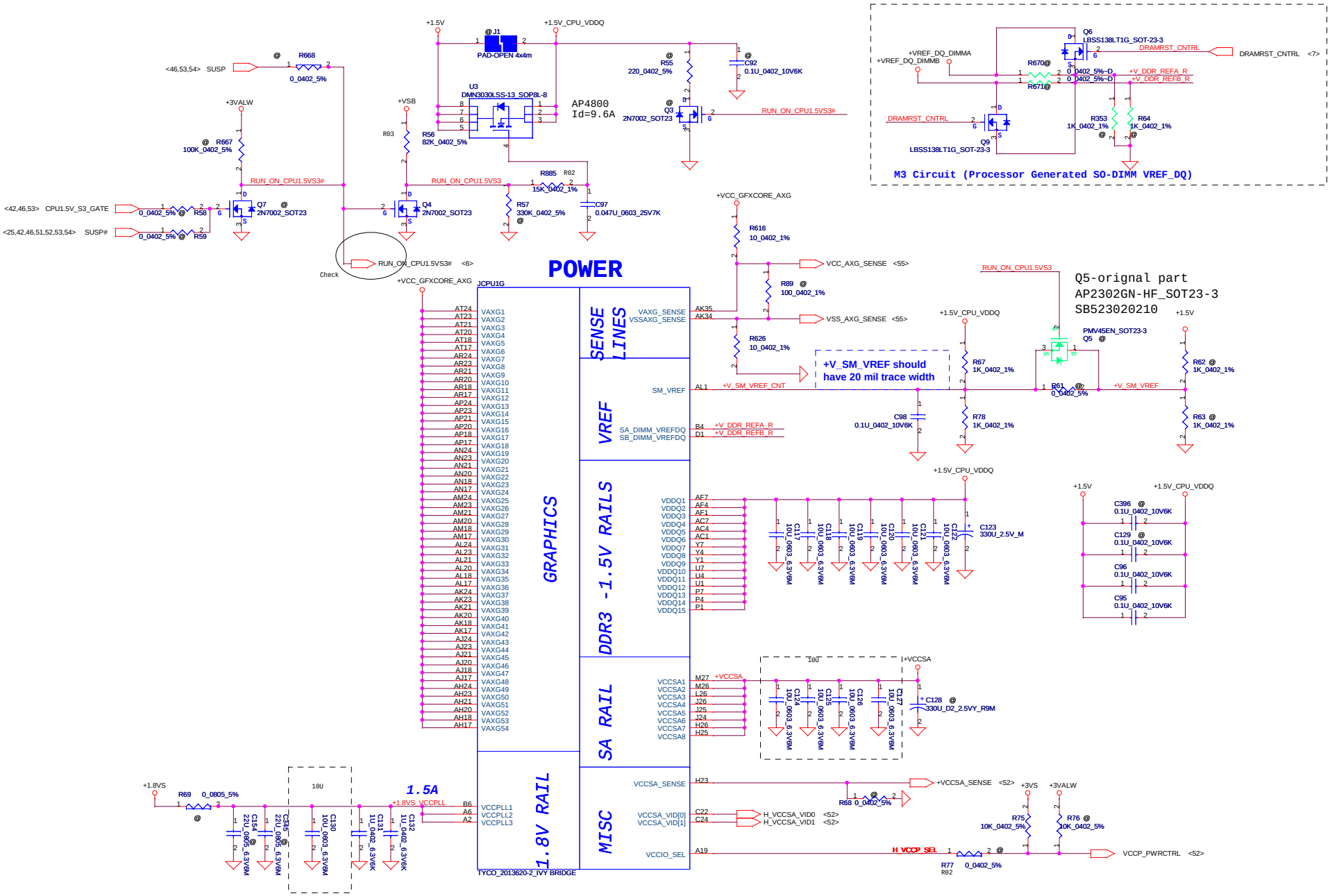

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Title	PROCESSOR(6/7) PWR		
Size: Custom	Document Number: LA-7981P		Rev: 0.2
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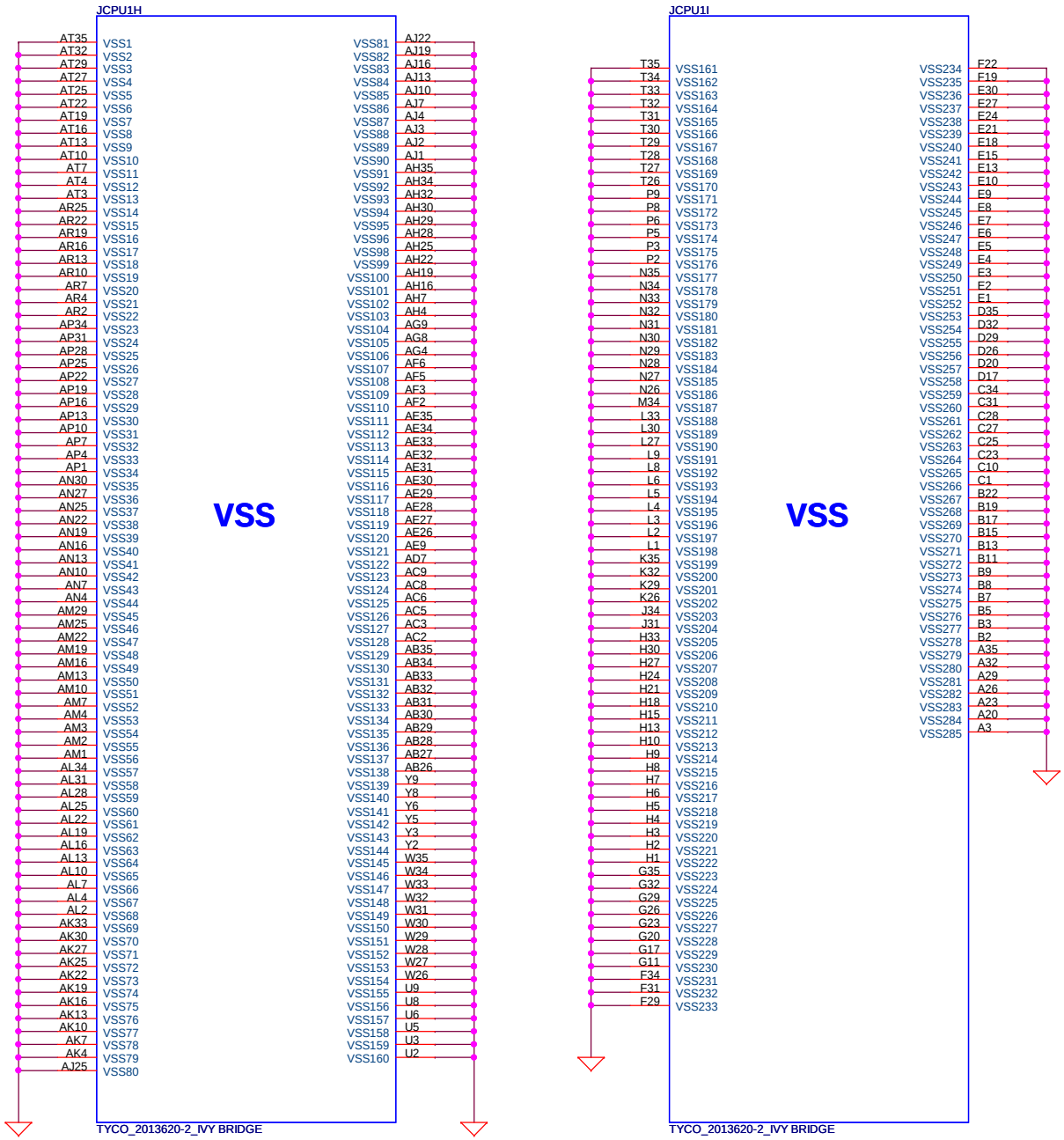

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Title: PROCESSOR(7/7) VSS

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DDR3 SO-DIMM A

JDIMM1

FOX_AS0A626-U4SN-7F

ME@

<7> DDR_A_D[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_MA[0..15]

DDR3_DRAMRST# <7,13>

<7> DDR_CKE0_DIMMA
DDR_CKE1_DIMMA <7>
<7> DDR_A_BS2
<7> M_CLK_DDR0
<7> M_CLK_DDR#0
<7> DDR_A_BS0
<7> DDR_A_WE#
<7> DDR_A_CAS#
<7> DDR_CS1_DIMMA#
M_CLK_DDR1 <7>
M_CLK_DDR#1 <7>
DDR_A_BS1 <7>
DDR_A_RAS# <7>
DDR_CS0_DIMMA# <7>
M_ODT0 <7>
M_ODT1 <7>

SMB_DATA_S3 <13,15,36>
SMB_CLK_S3 <13,15,36>

+0.75VS

0.65MIL 75V

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

EVT Check

7/28 Update connect GND directly

Security Classification	Compal Secret Data		
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Title: **DDRIII-SODIMM SLOT1**

Size: Custom | Document Number: **LA-7981P** | Rev: 0.2

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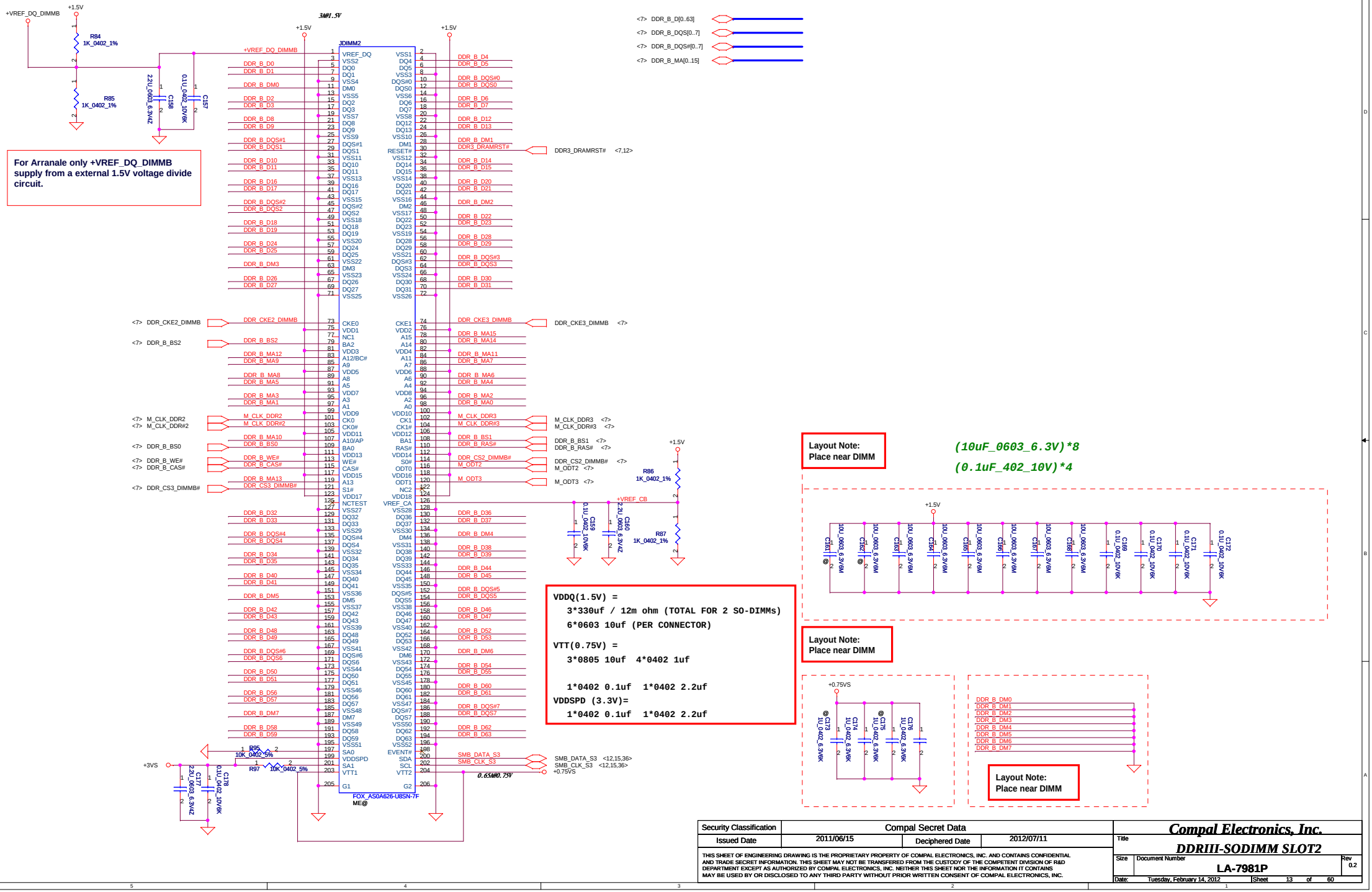


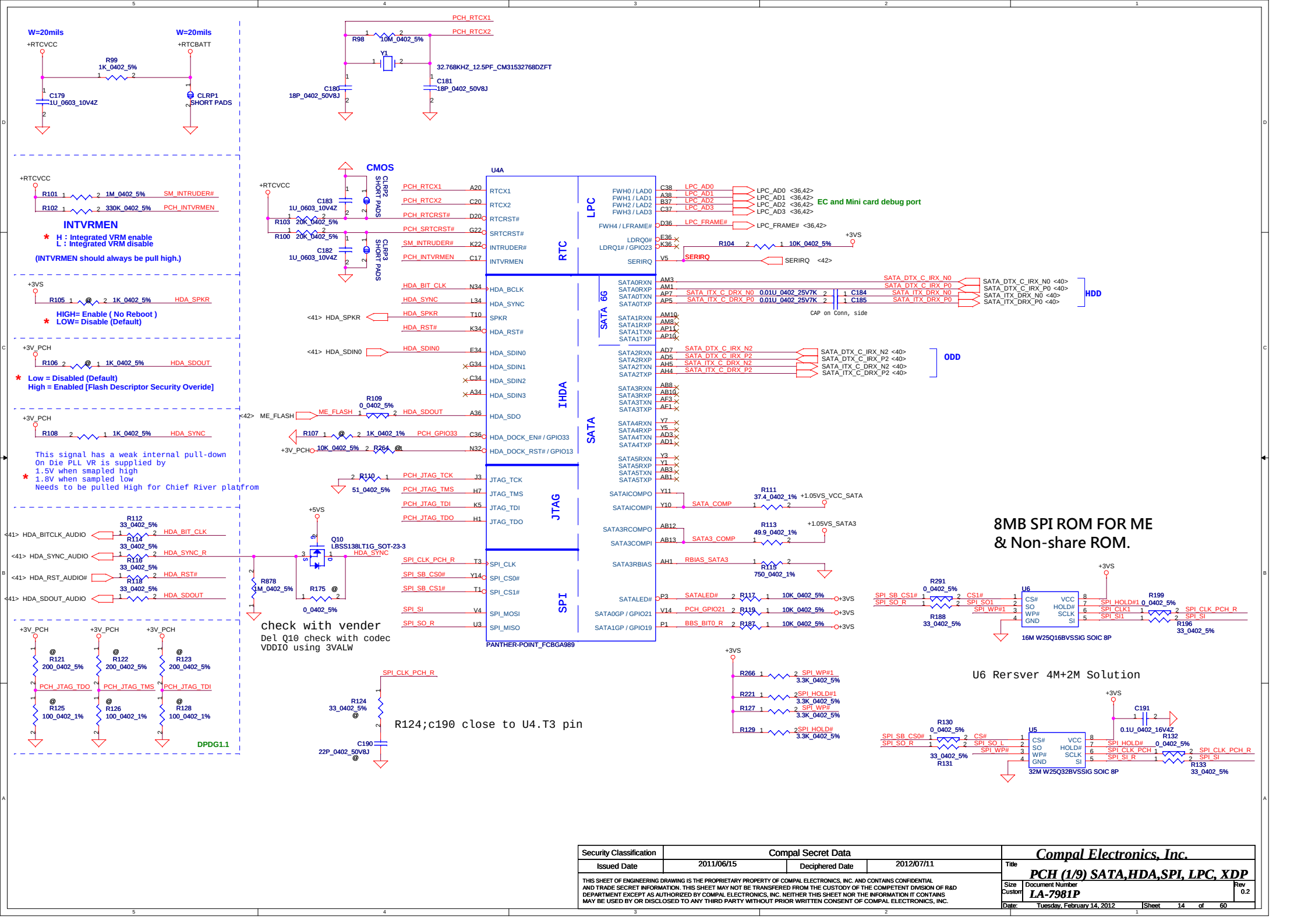
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

Size	Document Number	Rev
	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 13 of 60



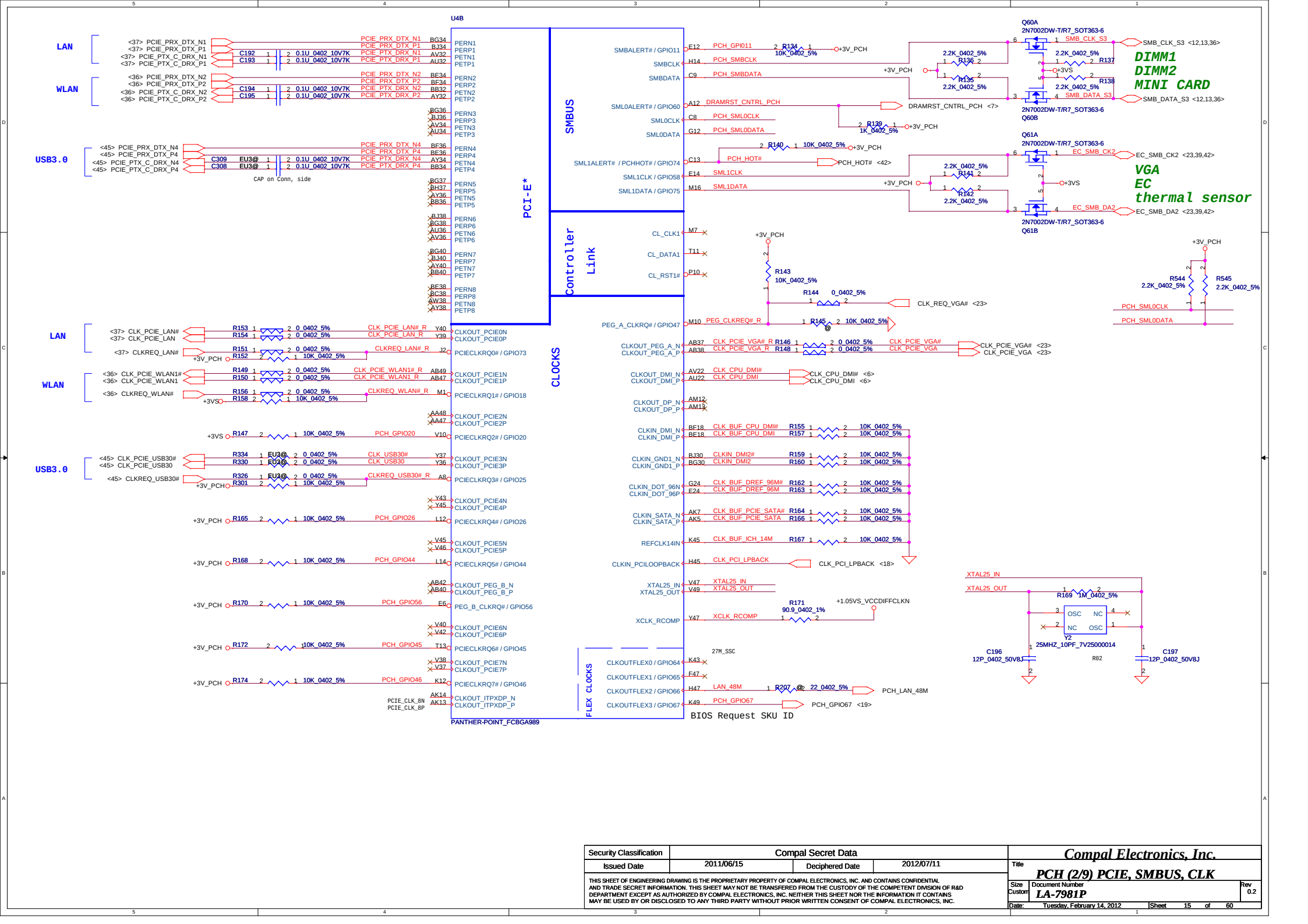
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 14 of 60



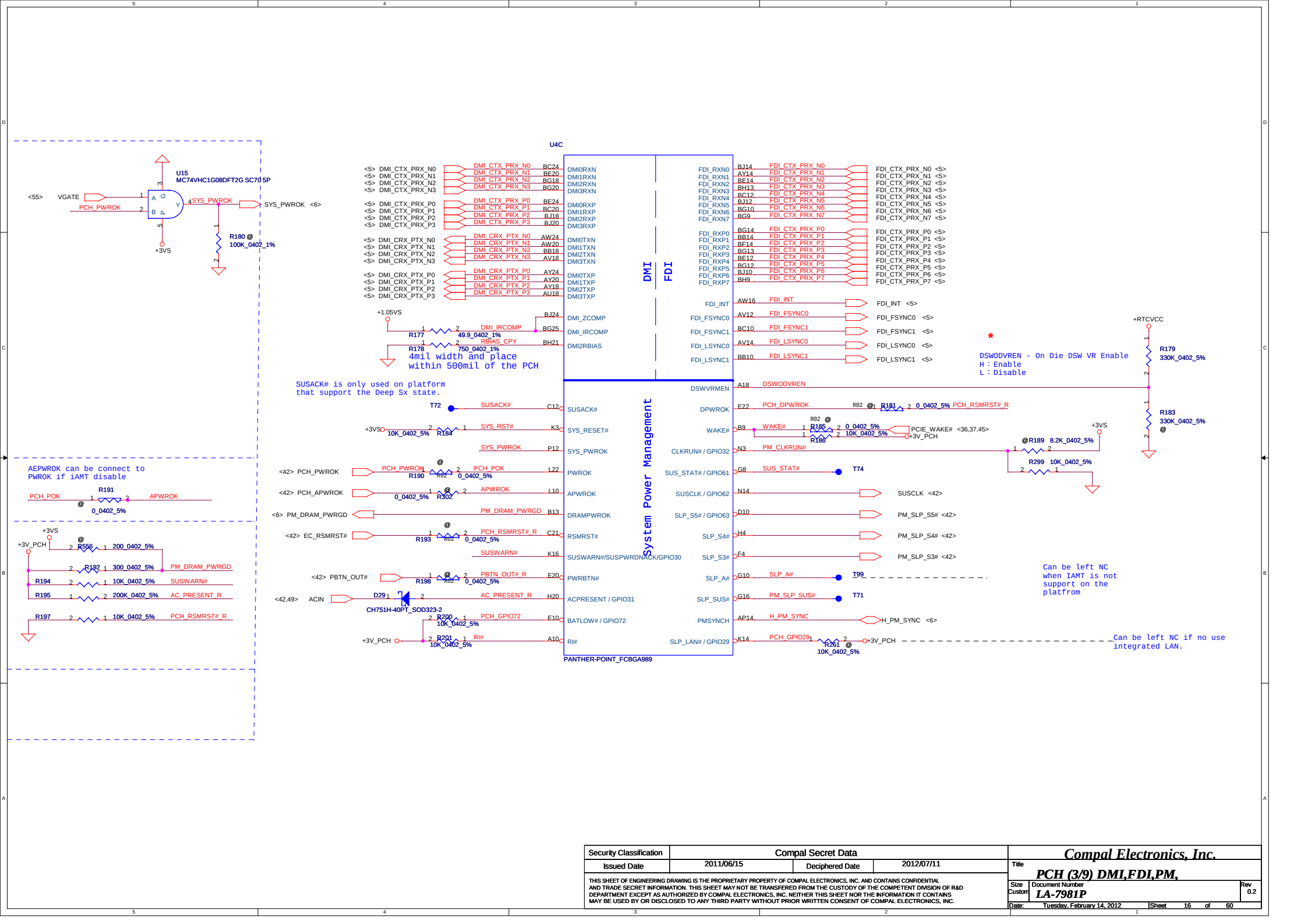
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 15 of 60



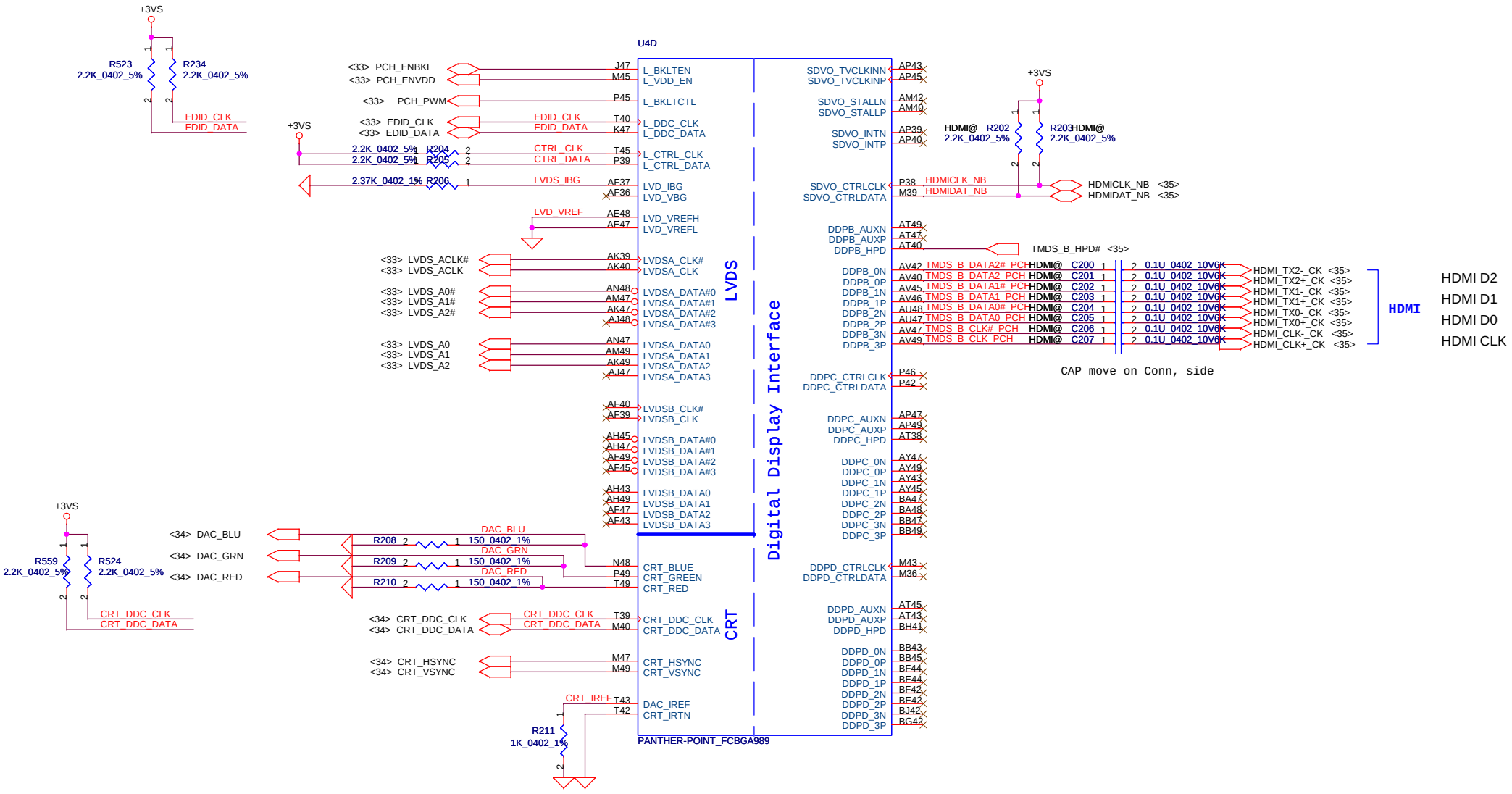
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

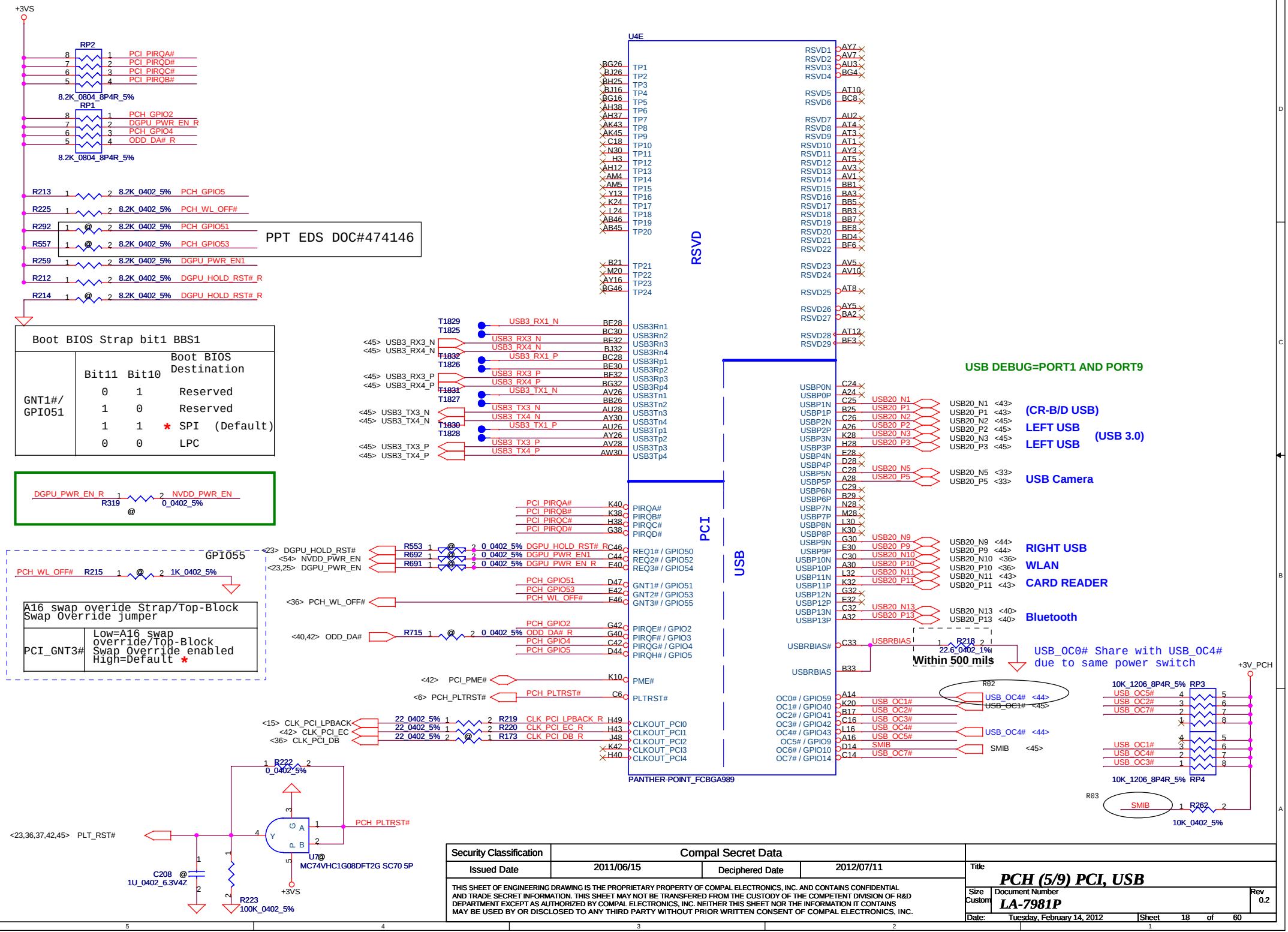
Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 16 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	PCH (4/9) LVDS,CRT,DP,HDMI		
Size B	Document Number LA-7981P		Rev 0.2
Date: Tuesday, February 14, 2012	Sheet 17 of 60		



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: **PCH (5/9) PCI, USB**

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 18 of 60

PCH_GPIO69	Function
0	HM76 by PCH
1	HM70 by PCH

PCH_GPIO70	Function
0	14/15"
1	17"
PCH_GPIO71	
0	USB3.0 by PCH
1	USB3.0 by NEC

+3V_PCH — Weak internal pull-high — R235 10K_0402_5% — EC_SMI#

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R240 @ 1K_0402_5% — PCH_GPIO28

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R245 @ 10K_0402_5% — PCH_GPIO27

<46,54> DGPU_PWROK — PU on power side — R297 0_0402_5% — DGPU_PWROK_R

<36> BT_DISABLE — R238 10K_0402_5% — BT_DISABLE

<40> ODD_EN — ODD_EN

<36,40> PCH_BT_ON# — R242 10K_0402_5% — PCH_BT_ON#

R241 10K_0402_5% — PCH_GPIO28

R243 10K_0402_5% — PCH_GPIO35

R244 @ 10K_0402_5% — PCH_GPIO37 — R881 10K_0402_5%

R250 @ 10K_0402_5% — PCH_GPIO36 — R547 10K_0402_5%

R233 10K_0402_5% — T7
R227 10K_0402_5% — PCH_GPIO1 — A42
R228 10K_0402_5% — PCH_GPIO6 — H36
<42> EC_SCI# — EC_SCI# — E38
<42> EC_SMI# — EC_SMI# — C10
R229 @ 10K_0402_5% — PCH_GPIO12 — C4
R230 1K_0402_5% — EC_LID_OUT# — G2
<42> EC_LID_OUT#
R231 10K_0402_5% — PCH_GPIO16 — U2
R232 @ 10K_0402_1% — DGPU_PWROK_R — D40
R247 10K_0402_5% — PCH_GPIO39 — M3
R248 10K_0402_5% — PCH_GPIO48 — V13
R249 10K_0402_5% — PCH_GPIO49 — V3
R251 10K_0402_5% — PCH_GPIO57 — D6

U4F

GPIO:
BMBUSY# / GPIO0
TACH1 / GPIO1
TACH2 / GPIO6
TACH3 / GPIO7
GPIO8
LAN_PHY_PWR_CTRL / GPIO12
GPIO15
SATA4GP / GPIO16
TACH0 / GPIO17
SCLOCK / GPIO22
GPIO24
GPIO27
GPIO28
STP_PCI# / GPIO34
GPIO35
SATA2GP / GPIO36
SATA3GP / GPIO37
SLOAD / GPIO38
SDATAOUT0 / GPIO39
SDATAOUT1 / GPIO48
SATA5GP / GPIO49 / TEMP_ALERT#
GPIO57

CPU/MISC:
TACH4 / GPIO68 — C40 — PCH_GPIO68 — 10K_0402_5% — R224
TACH5 / GPIO69 — B41 — PCH_GPIO69
TACH6 / GPIO70 — C41 — PCH_GPIO70
TACH7 / GPIO71 — A40 — PCH_GPIO71
A20GATE — P4 — R236 10K_0402_5% — GATEA20 <42>
PECI — AU16 — PCH_PECI_R — @ R237 0_0402_5% — H_PECI <6,42>
RCIN# — P5 — KBRST# — KBRST# <42>
PROCPWRGD — AY11 — H_CPUPWRGD <6>
THRMTRIP# — AY10 — PCH_THRMTRIP#_R — R239 390_0402_5% — H_THRMTRIP# <6>
PCH_THRMTRIP#_R <23>
INIT3_3V — T14
DF_TVS — AY1
TS_VSS1 — AH8
TS_VSS2 — AK11
TS_VSS3 — AH10
TS_VSS4 — AK10
NC_1 — P37

KBRST# — R226 10K_0402_5%

INIT3_3V
This signal has weak internal PU,can't pull low

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

NV_CLE — R217 1K_0402_5% — R216 2.2K_0402_5% — H_SNB_IVB# <6>
CLOSE TO THE BRANCHING POINT

Weak internal PU,Do not pull low

NCTF:
VSS_NCTF_1 … VSS_NCTF_14 (A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49)
VSS_NCTF_15 … VSS_NCTF_32 (BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48, D1, D49, E1, E49, F1, F49)

PANTHER-POINT_FCBGA989

BIOS Request SKU ID

R711 @ 10K_0402_5% — PCH_GPIO38
R246 @ 10K_0402_5%
PCH_GPIO67 — PCH_GPIO67 <15>
R708 10K_0402_5%
R293 10K_0402_5%

PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PCH (6/9) GPIO, CPU, MISC
Size: Custom | Document Number: LA-7981P | Rev: 0.2
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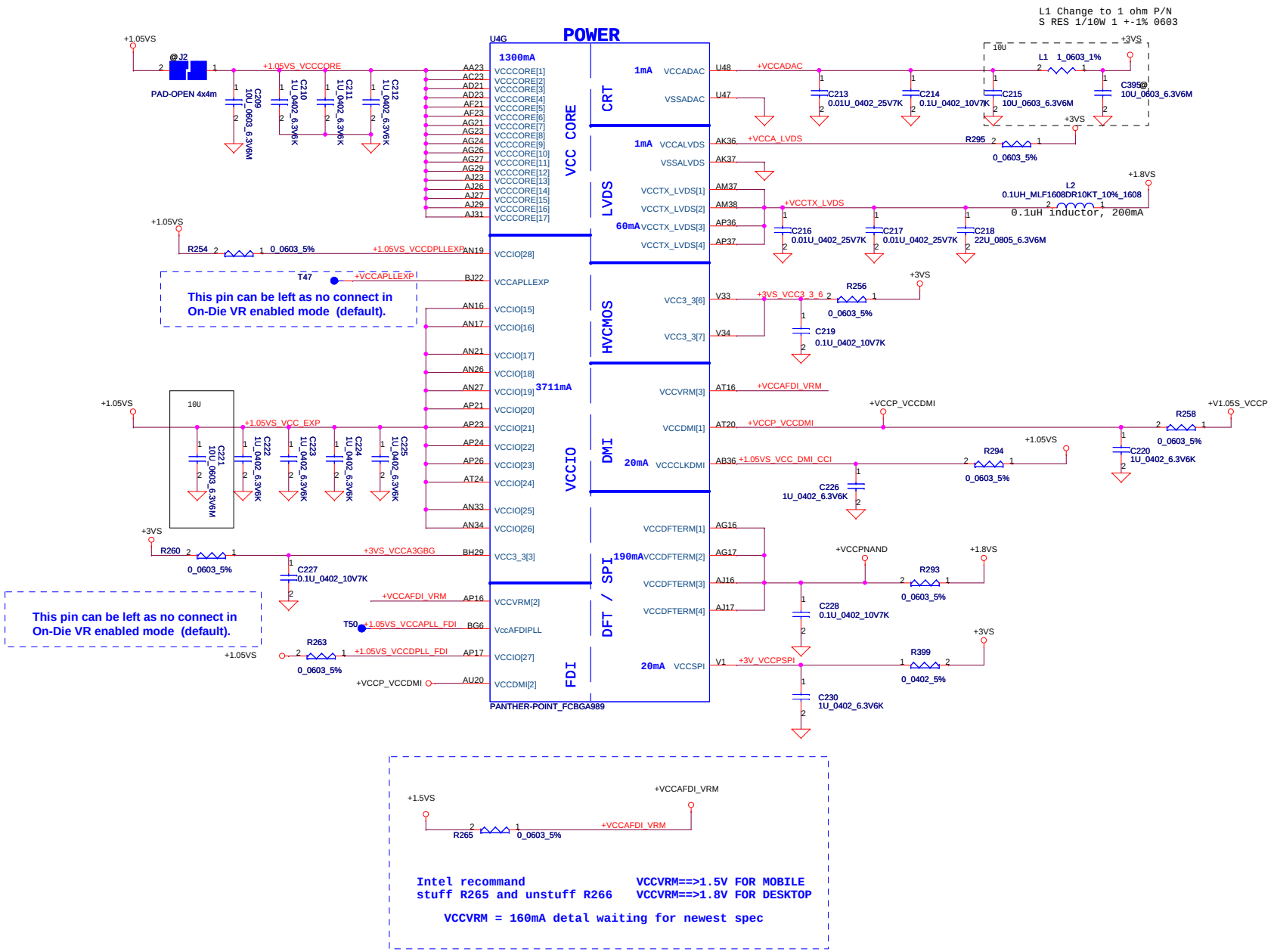
Compal Electronics, Inc.



PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

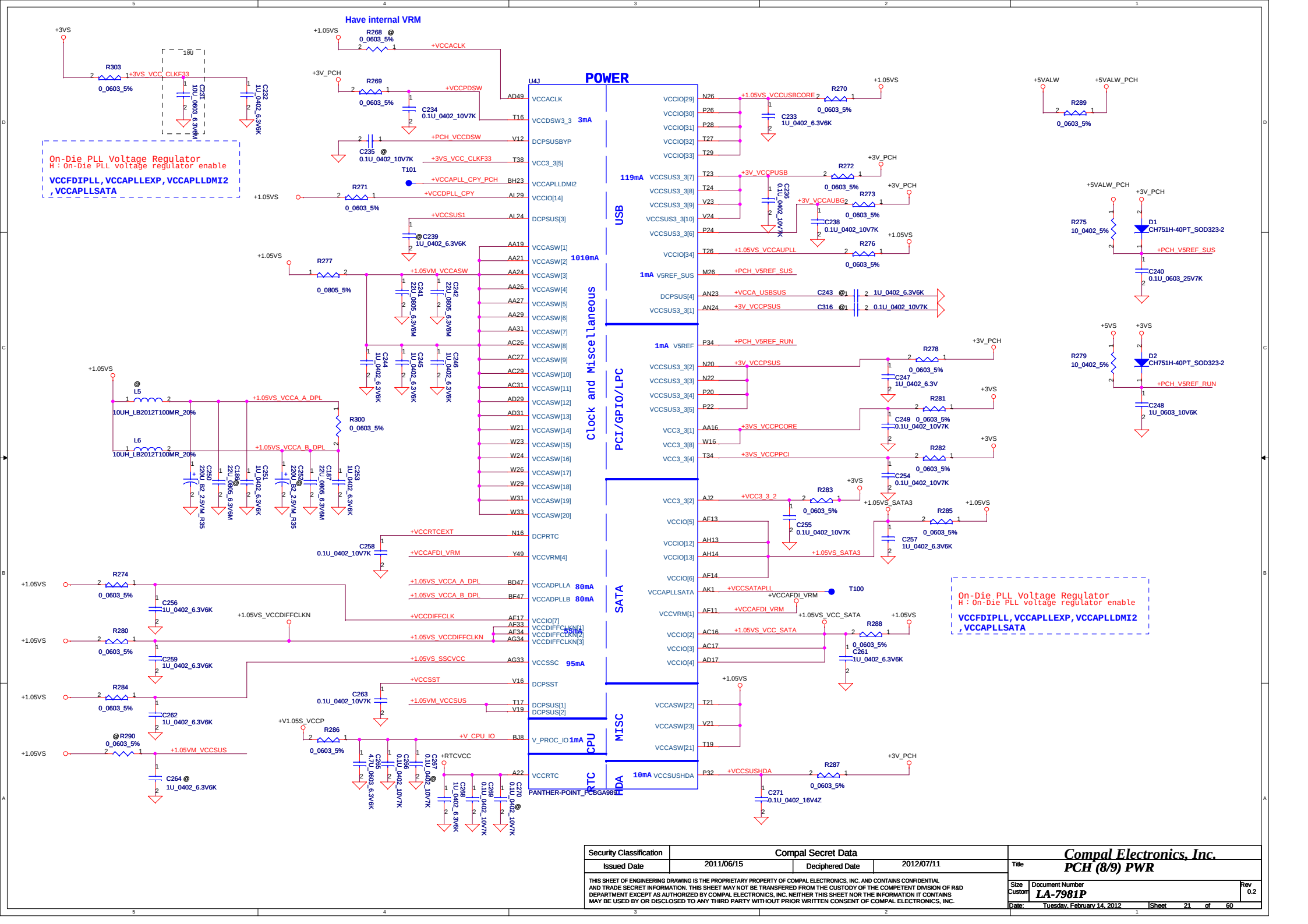
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-7981P | Rev: 0.2

Date: Tuesday, February 14, 2012 | Sheet 20 of 60



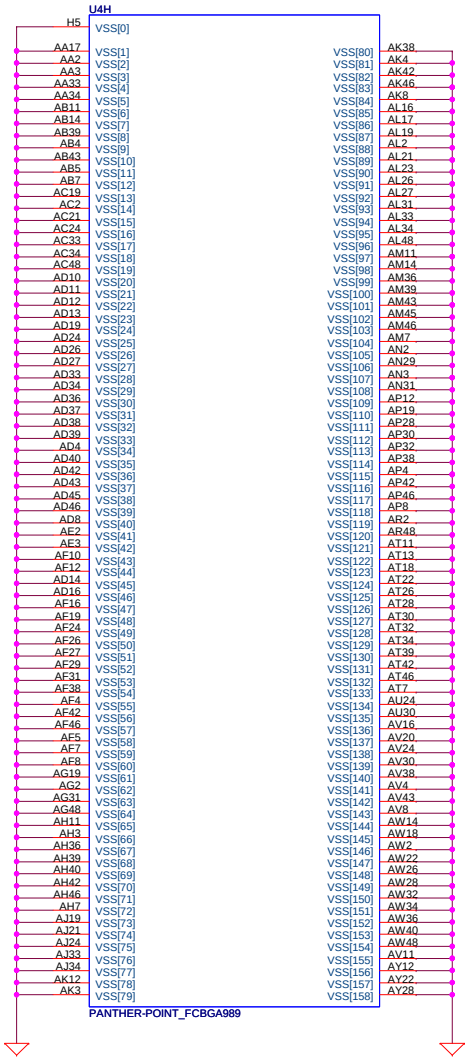
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

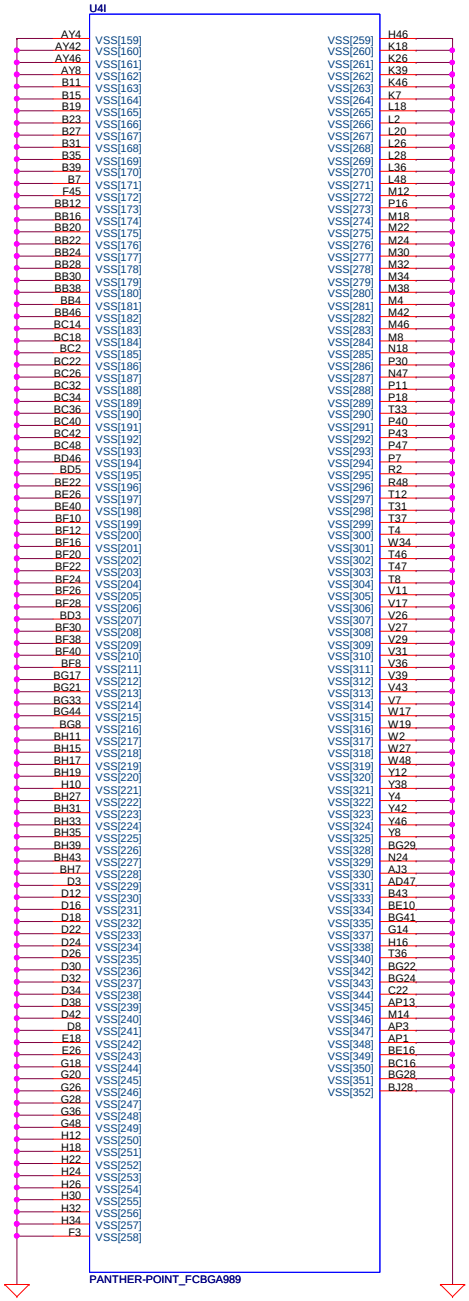
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 21 of 60





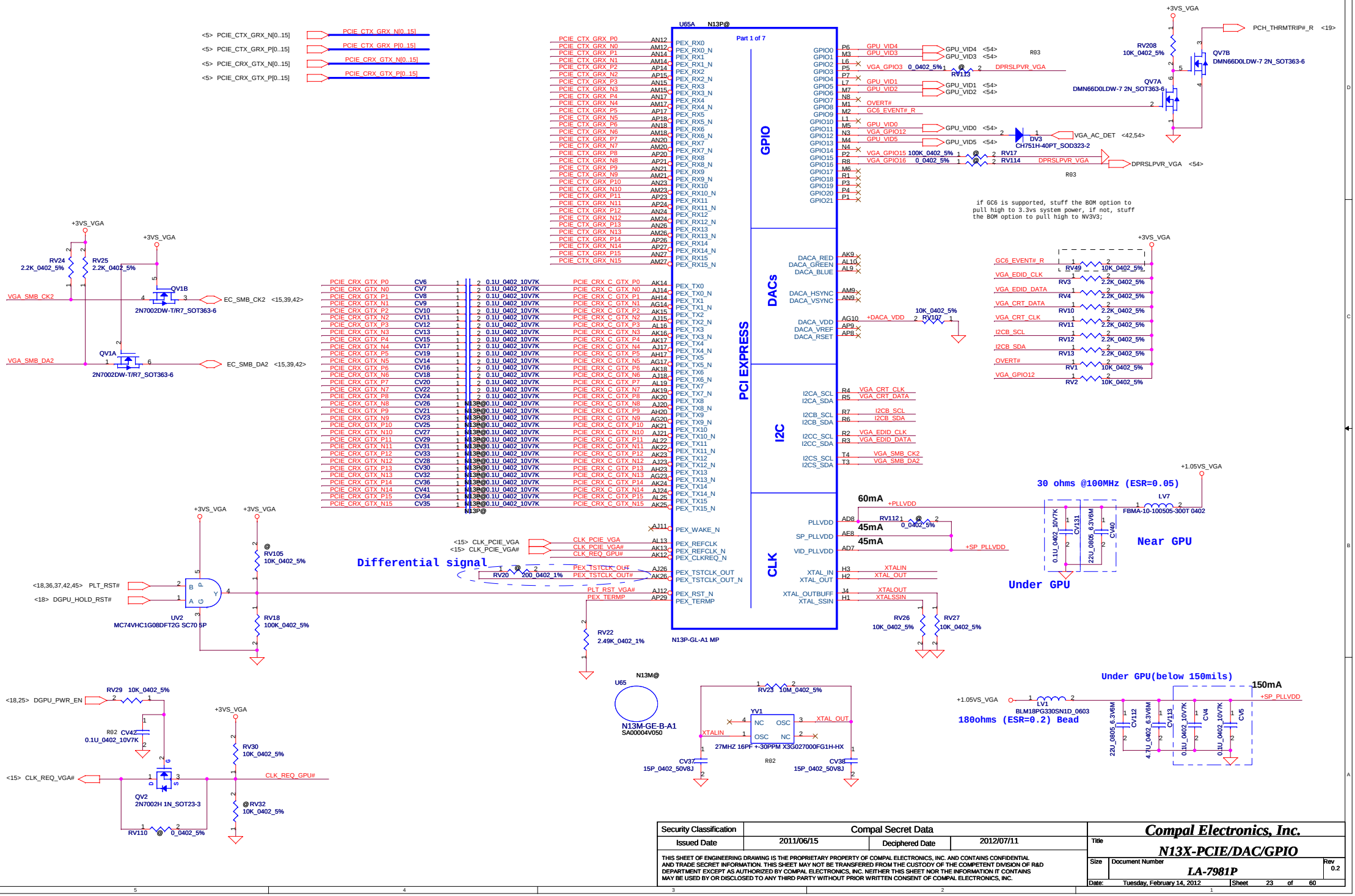
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **PCH (9/9) VSS**

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 22 of 60



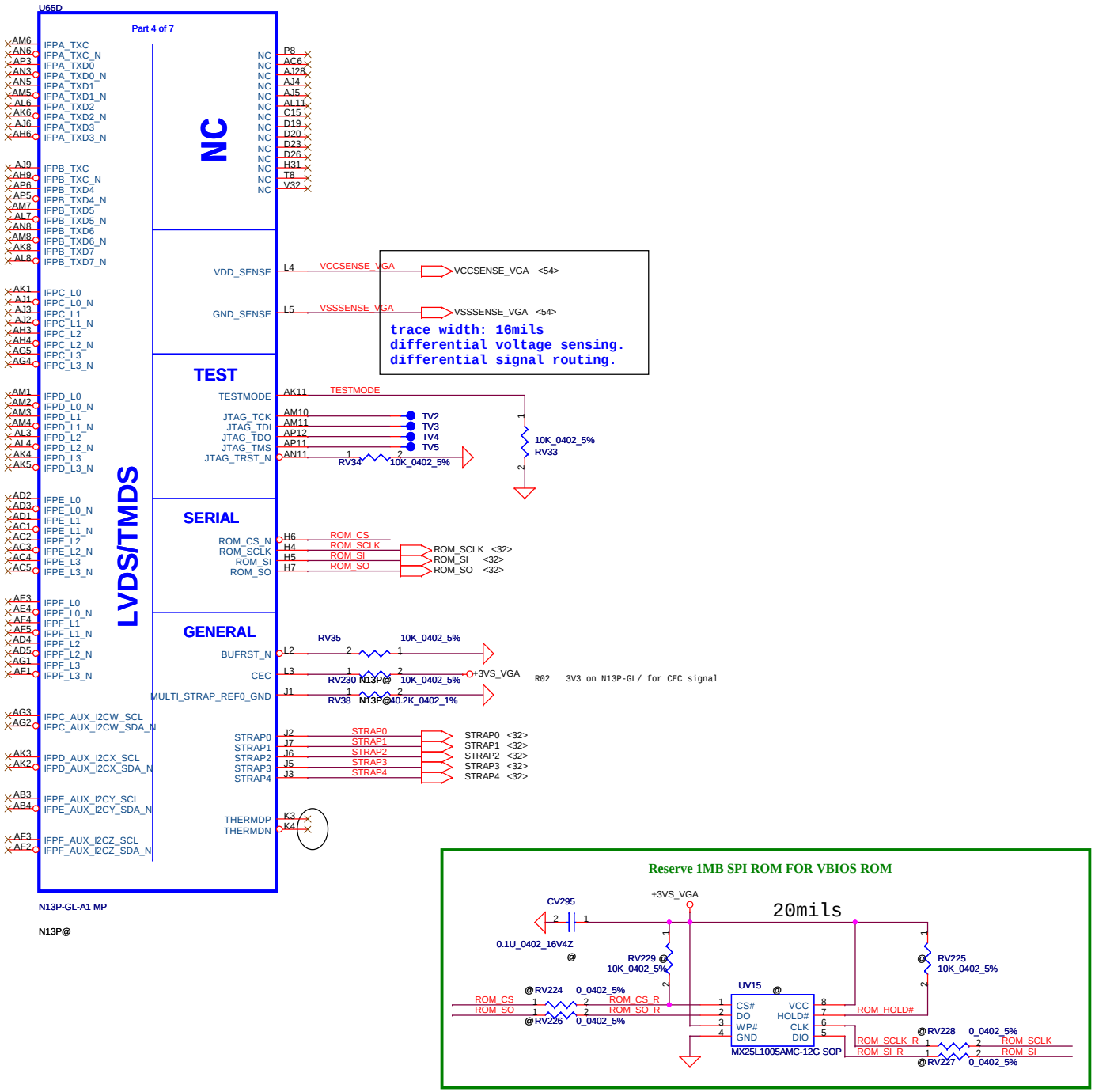
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **N13X-PCIE/DAC/GPIO**

Size	Document Number	Rev
	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 23 of 60



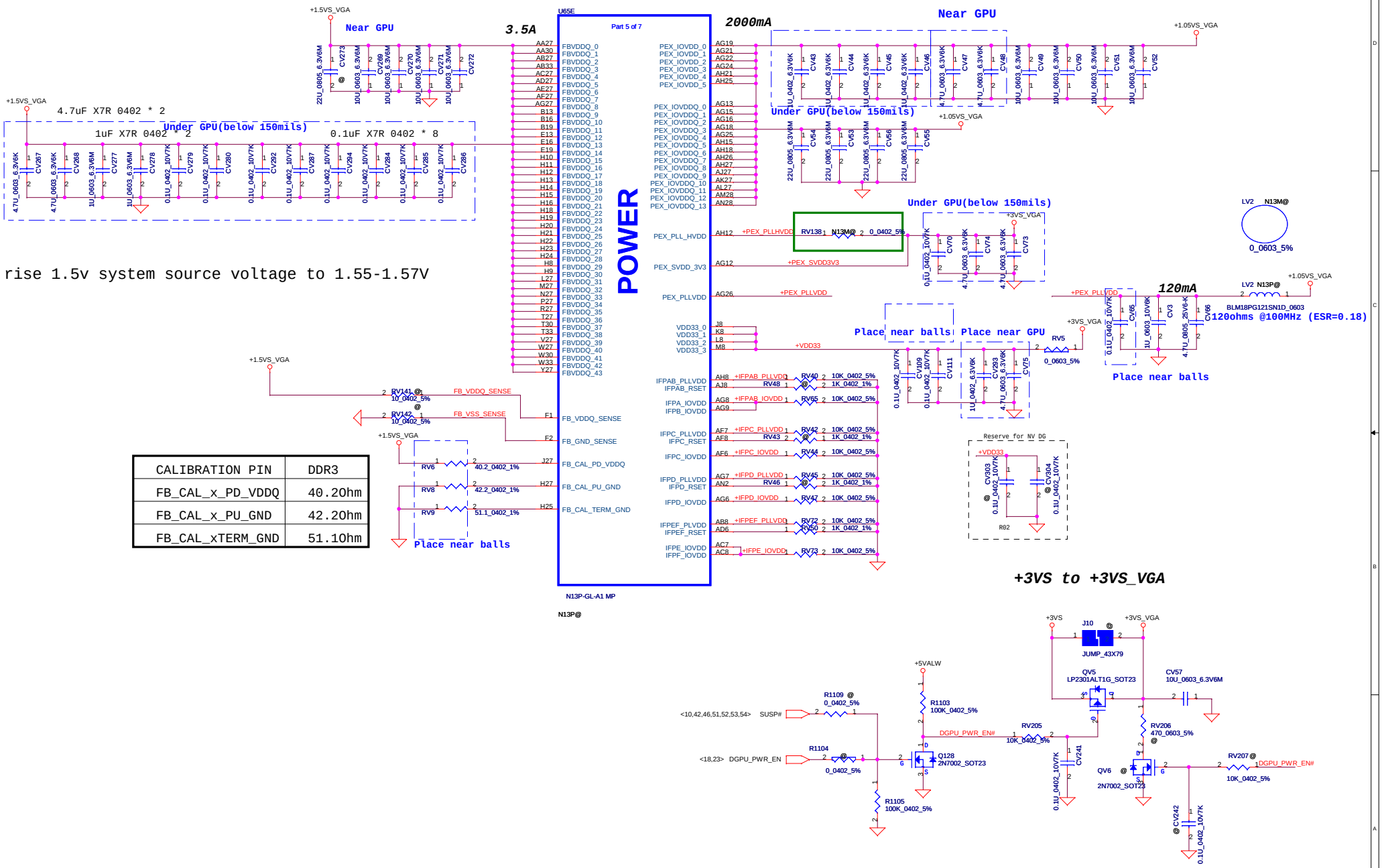
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **N13X-LVDS/HDMI/DP/THM**

Size	Document Number	Rev
	LA-7981P	0.2

Date: Tuesday, February 14, 2012 Sheet 24 of 60



CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

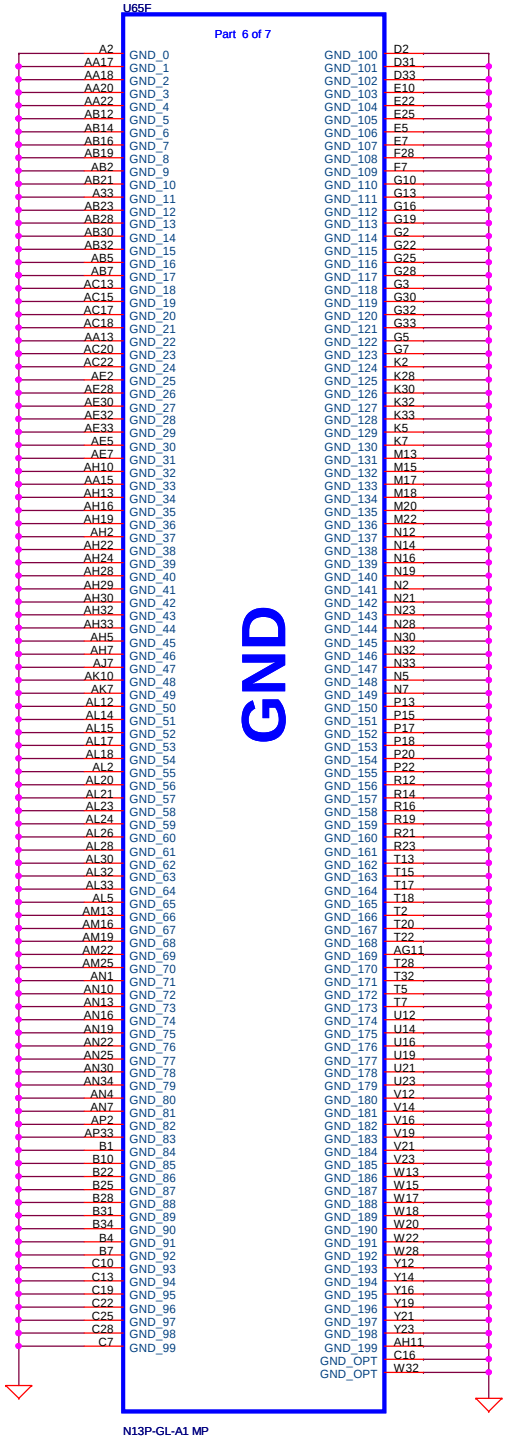
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

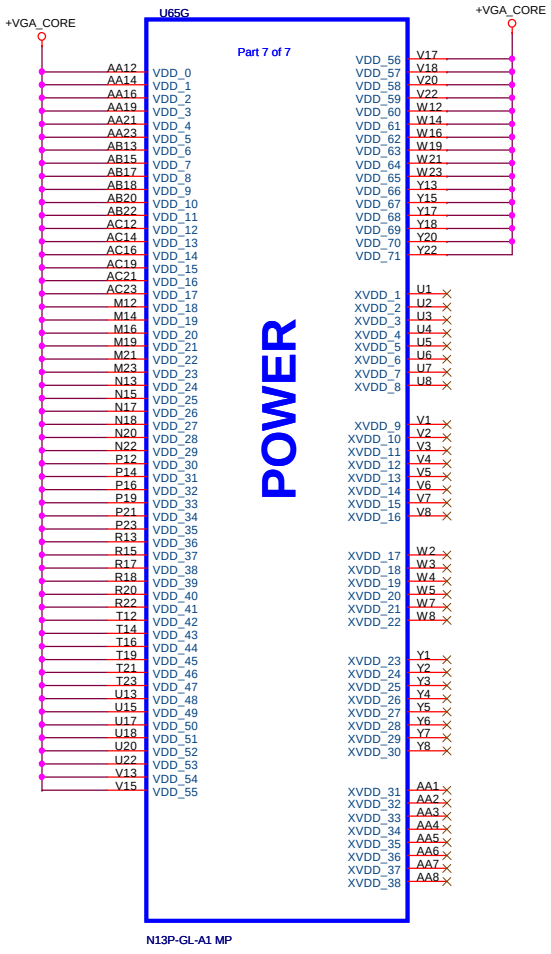
Compal Electronics, Inc.

Title: *N13X-POWER*

Size	Document Number	Rev
	LA-7981P	0.2

Date: Tuesday, February 14, 2012 | Sheet 25 of 60





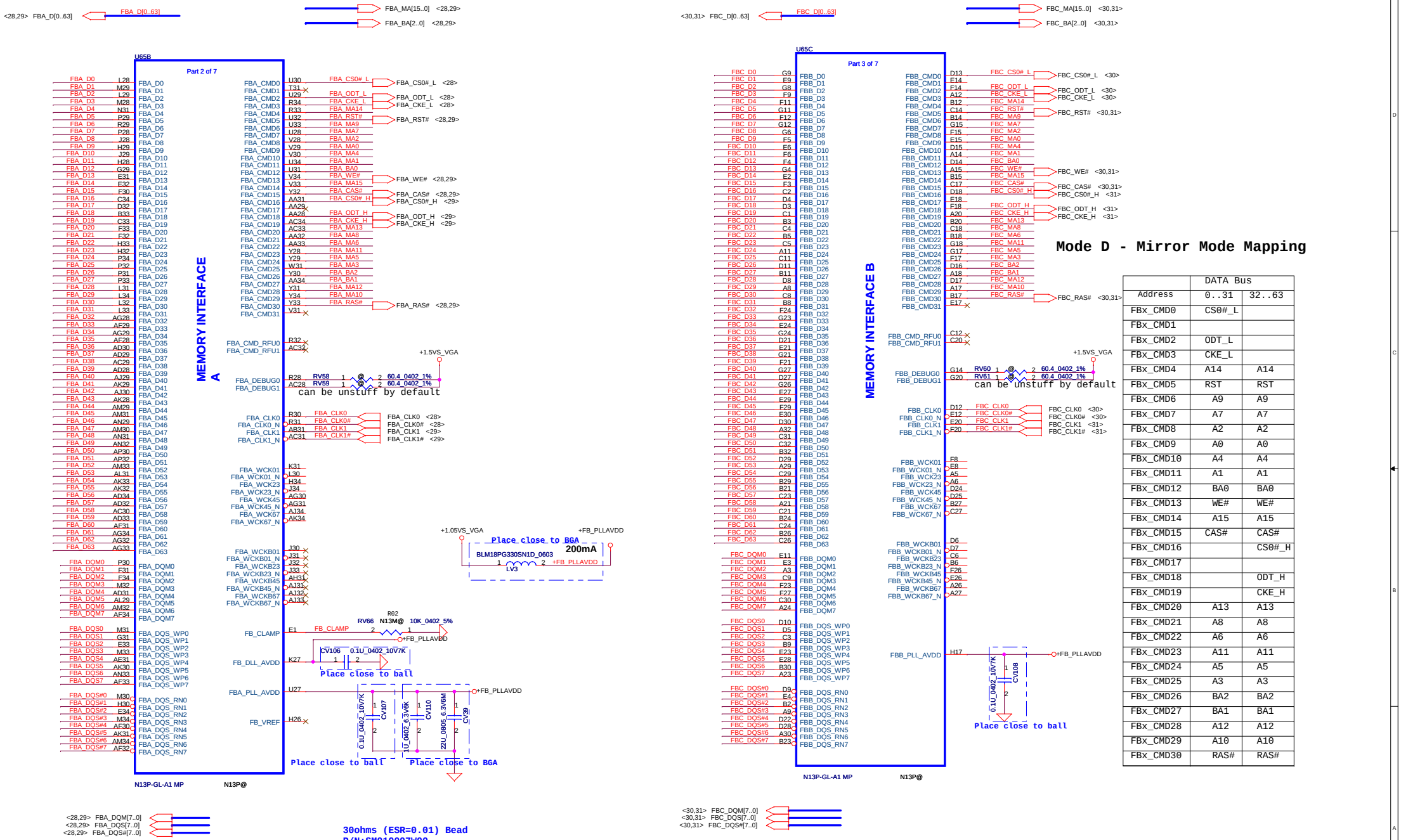
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **N13-VGA CORE, GND**

Size	Document Number	Rev
	LA-7981P	0.2

Date: Tuesday, February 14, 2012 | Sheet 26 of 60



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

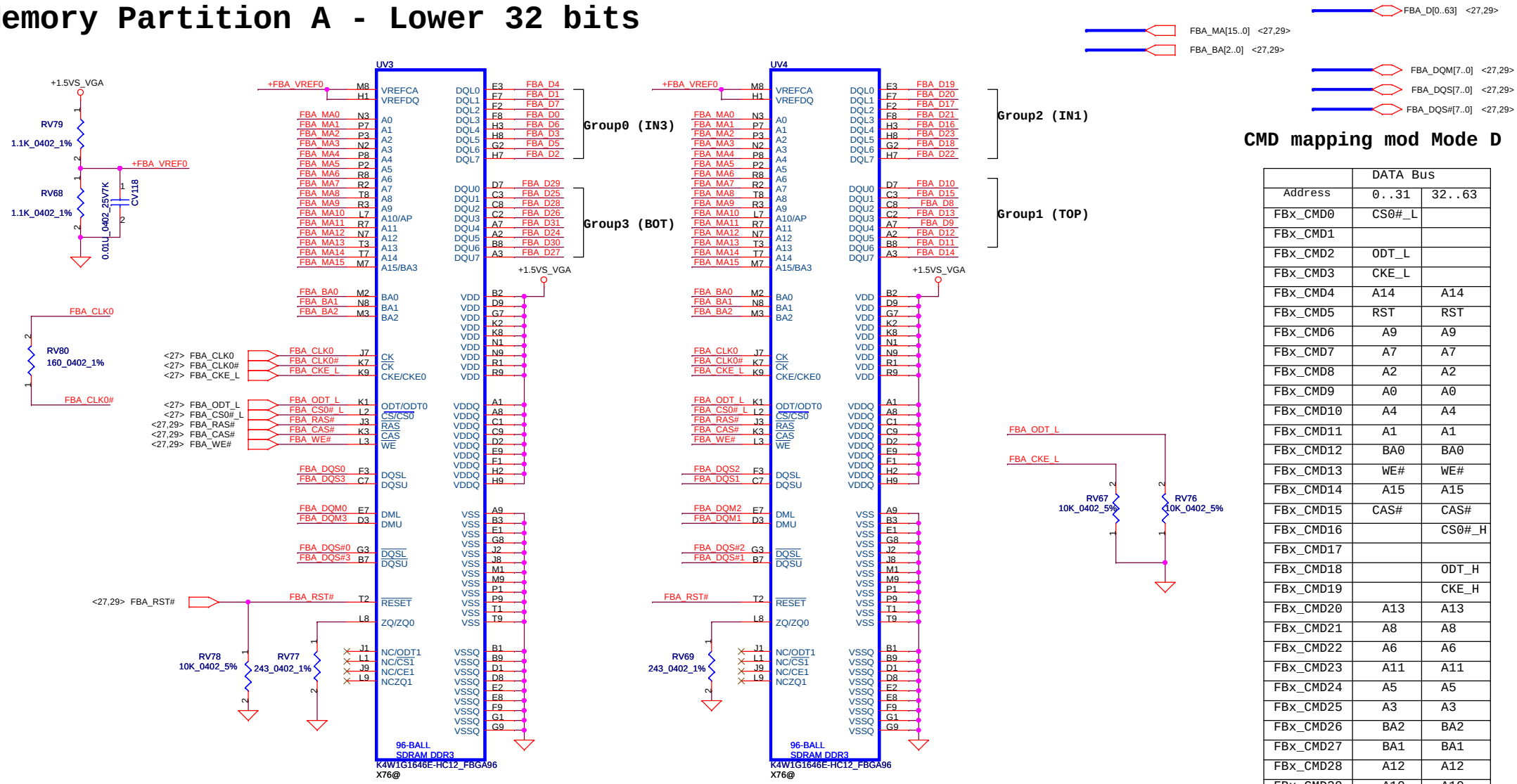
Compal Electronics, Inc.

Title: **N13X-MEM Interface**

Size	Document Number	Rev
	LA-7981P	0.2

Date: Tuesday, February 14, 2012 | Sheet 27 of 60

Memory Partition A - Lower 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: N13X-VRAM A Lower

Size | Document Number: LA-7981P | Rev: 0.2

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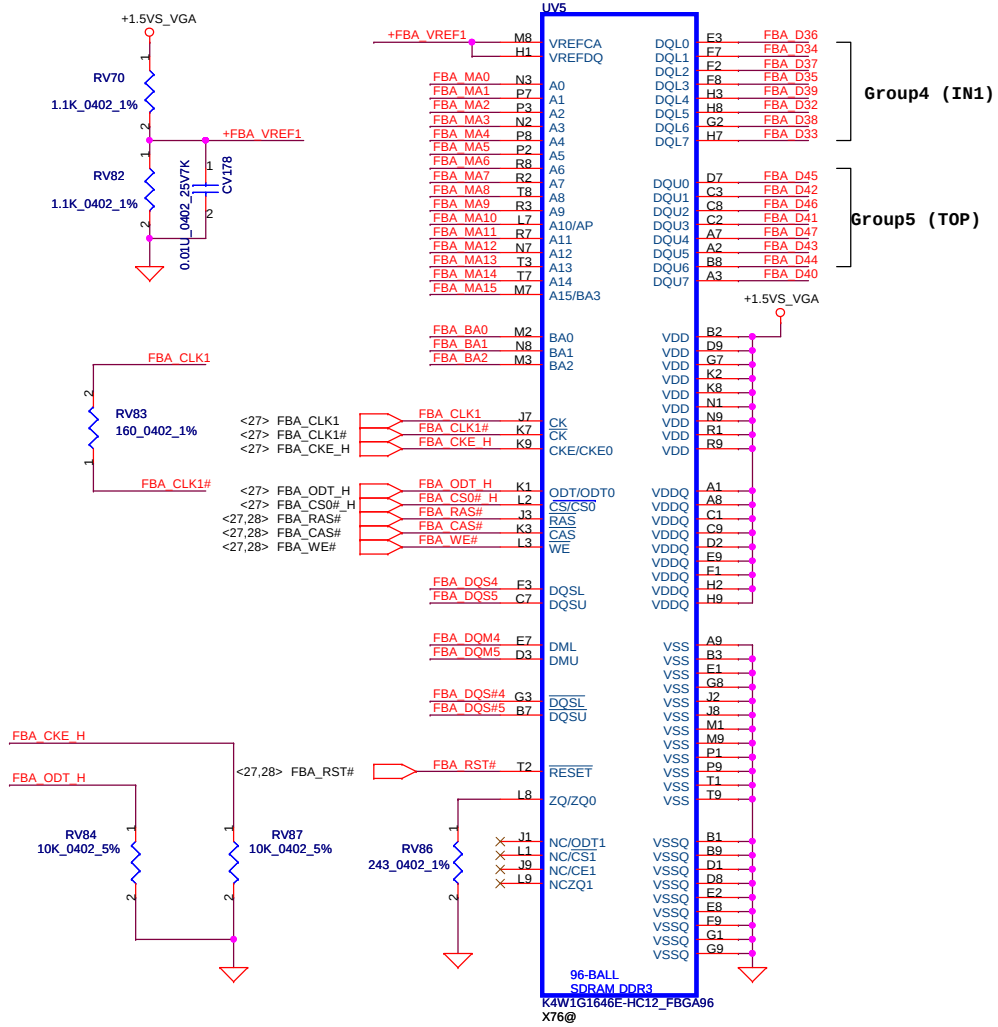
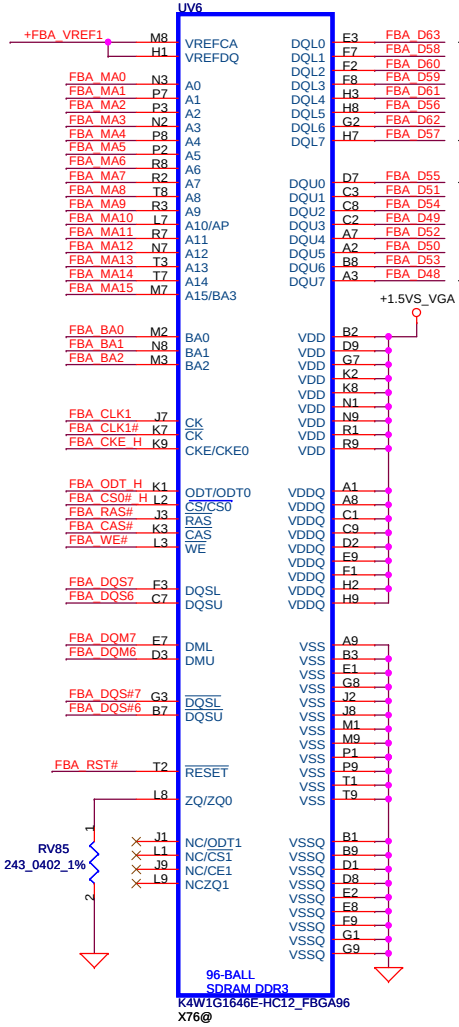
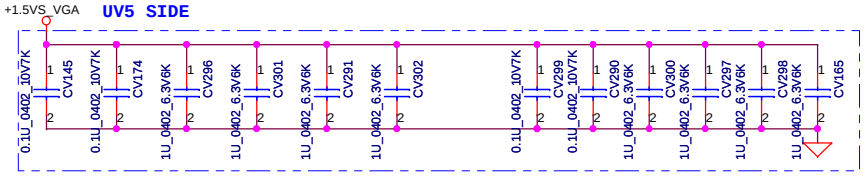
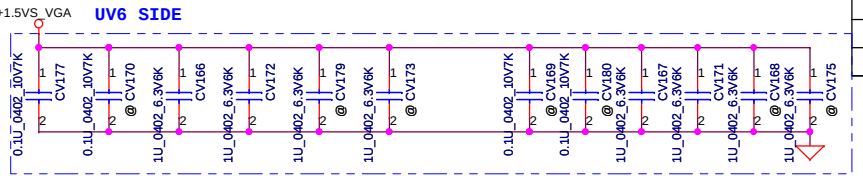
Memory Partition A - Upper 32 bits









FBA_D[0..63] <27,28>
FBA_MA[15..0] <27,28>
FBA_BA[2..0] <27,28>
FBA_DQM[7..0] <27,28>
FBA_DQS[7..0] <27,28>
FBA_DQS#[7..0] <27,28>

CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: N13X-VRAM A Upper

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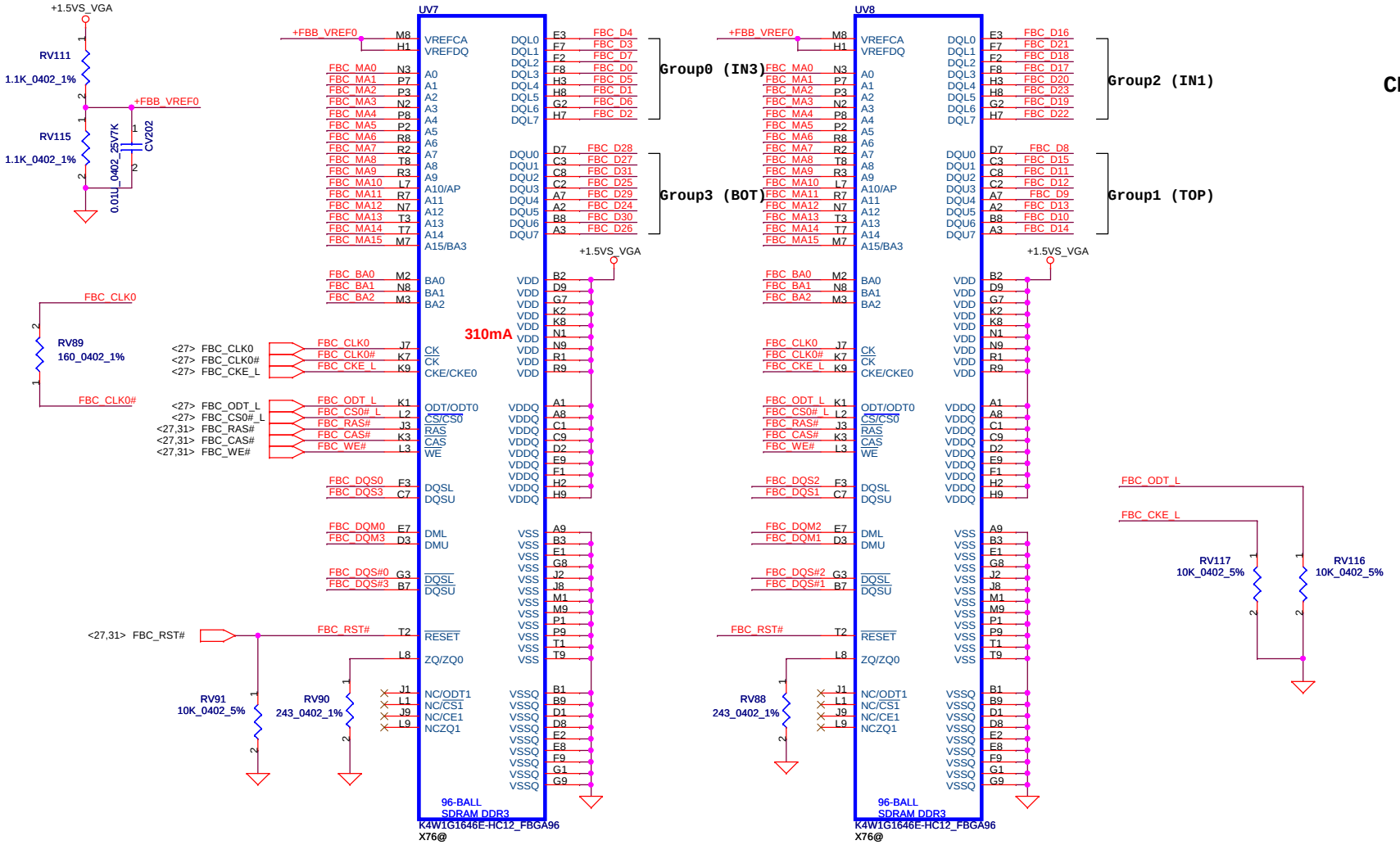
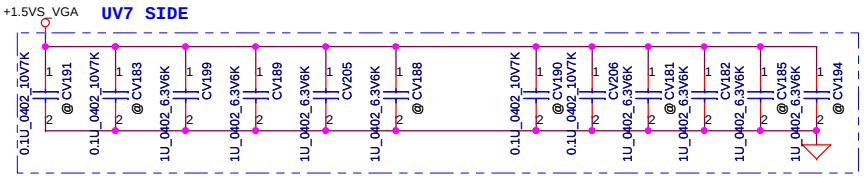
Memory Partition C - Lower 32 bits

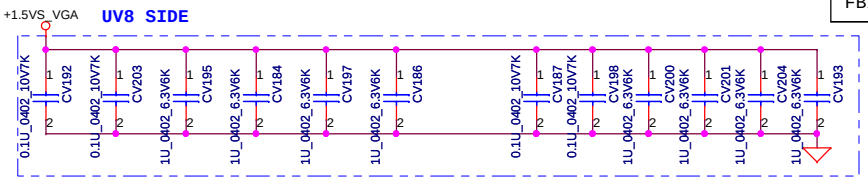
FBC_D[0..63] <27,31>
FBC_MA[15..0] <27,31>
FBC_BA[2..0] <27,31>
FBC_DQM[7..0] <27,31>
FBC_DQS[7..0] <27,31>
FBC_DQS#[7..0] <27,31>



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **N13X-VRAM C Lower**

Size: Custom | Document Number: **LA-7981P** | Rev: 0.2

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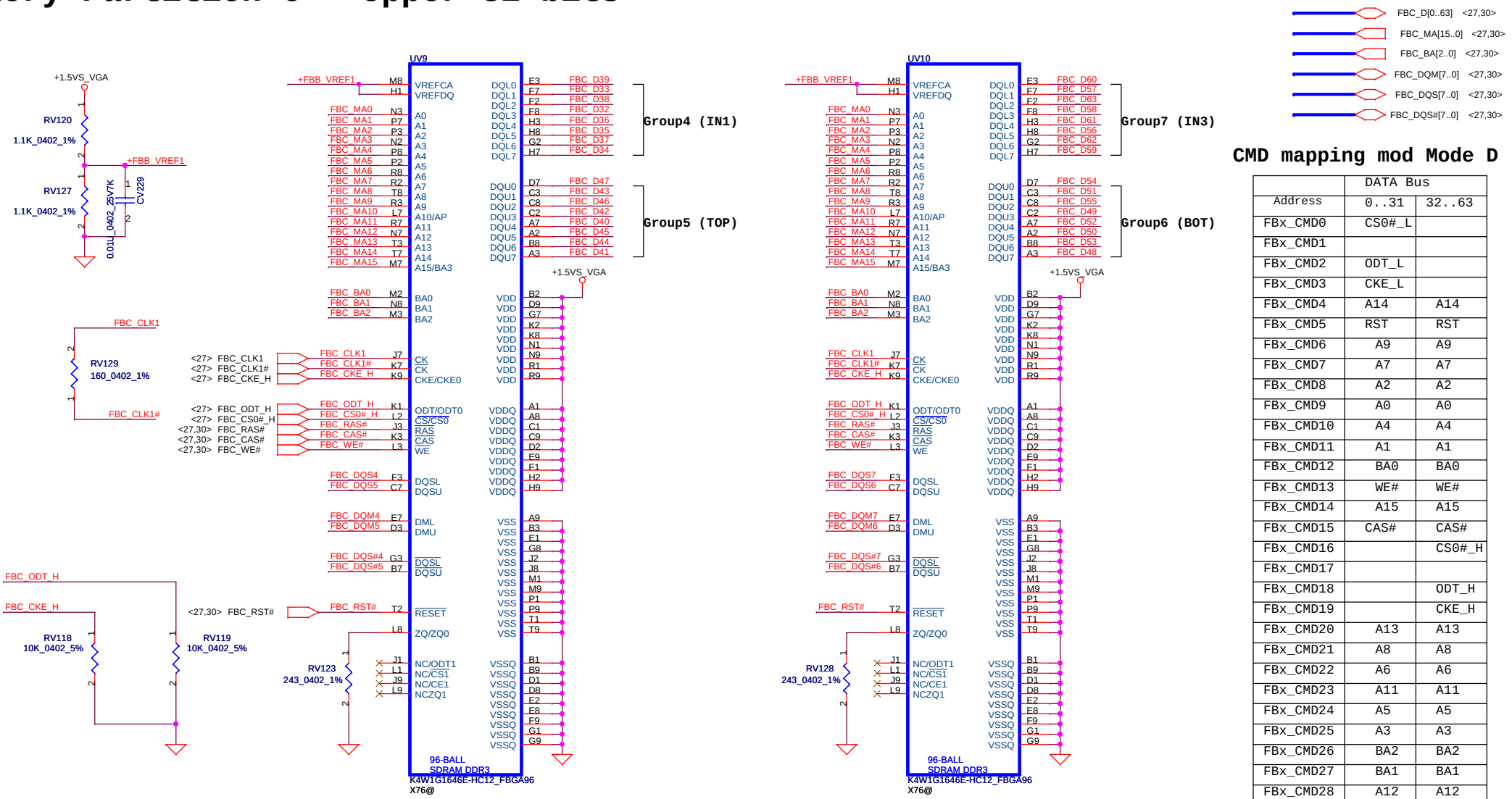
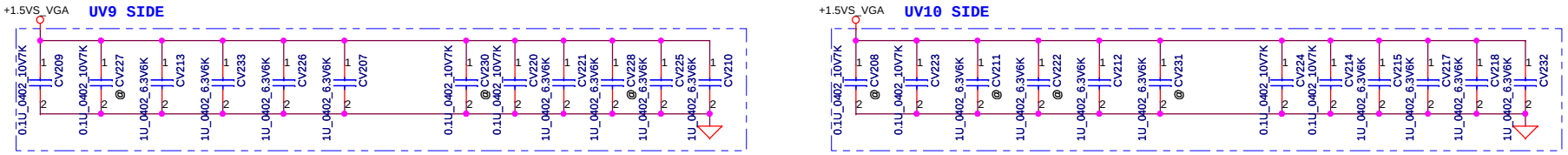
Memory Partition C - Upper 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **N13X-VRAM C Upper**

Size: Custom | Document Number: **LA-7981P** | Rev: 0.2

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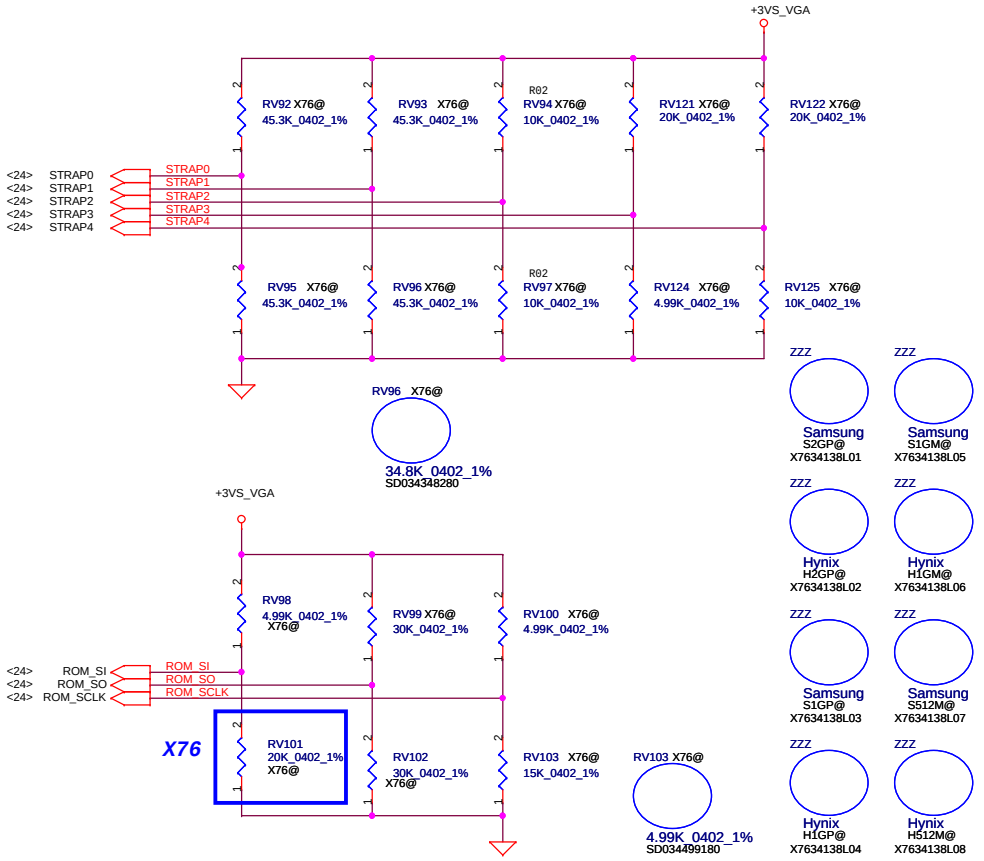

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR

0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG

3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417

0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE

0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG

0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

USER Straps

User[3:0]	
1000-1100	Customer defined

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE

0	3D Device (Class Code 302h)
1	VGA Device (Default)

PEX_PLL_EN_TERM

0	Disable (Default)
1	Enable

PCIE_MAX_SPEED

0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

For N13P-GL strap table

X76

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16* 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 45K	R PD 10K	R PD 15K
N13P-GL	900 MHz	128M* 16* 8 2GB	Hynix (2Gb) H5TQ1G63DFR-11C	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 35K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Samsung (1Gb) K4W1G1646G-BC11	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 20K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Hynix (1Gb) H5TQ1G63DFR-11C	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 15K	R PD 10K	R PD 15K

For N13M-GE strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE	900 MHz	128M* 16* 4 1GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N13M-GE	900 MHz	128M* 16* 4 1GB	Hynix (2Gb) H5TQ1G63DFR-11C	R PD 10K	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N13M-GE	900 MHz	64M* 16* 4 512MB	Samsung (1Gb) K4W1G1646G-BC11	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N13M-GE	900 MHz	64M* 16* 4 512MB	Hynix (1Gb) H5TQ1G63DFR-11C	R PD 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: N13X_MISC

Size: Custom | Document Number: LA-7981P | Rev: 0.2

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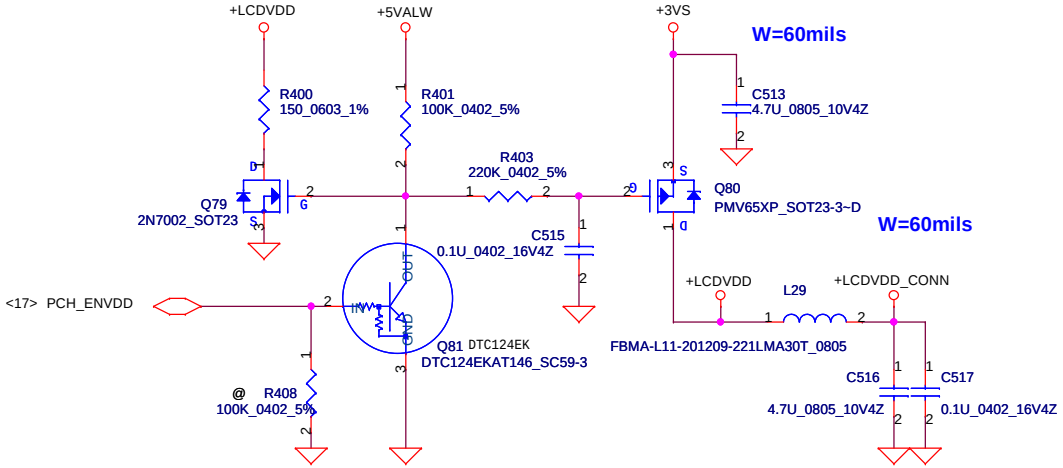
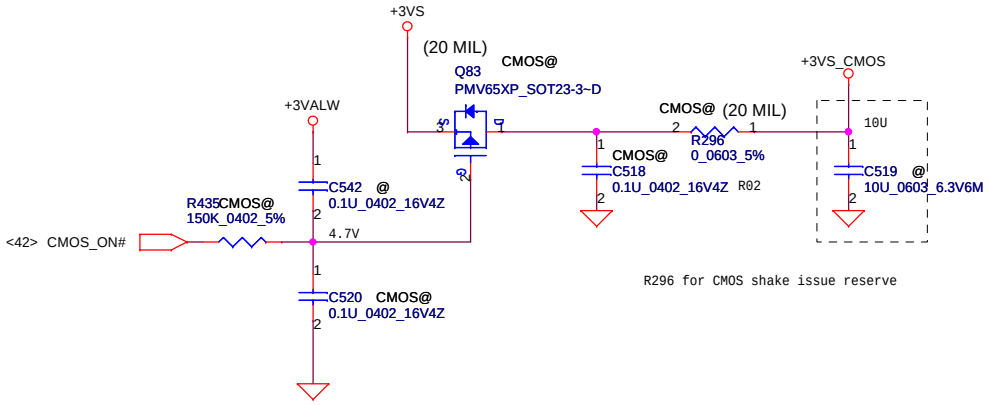
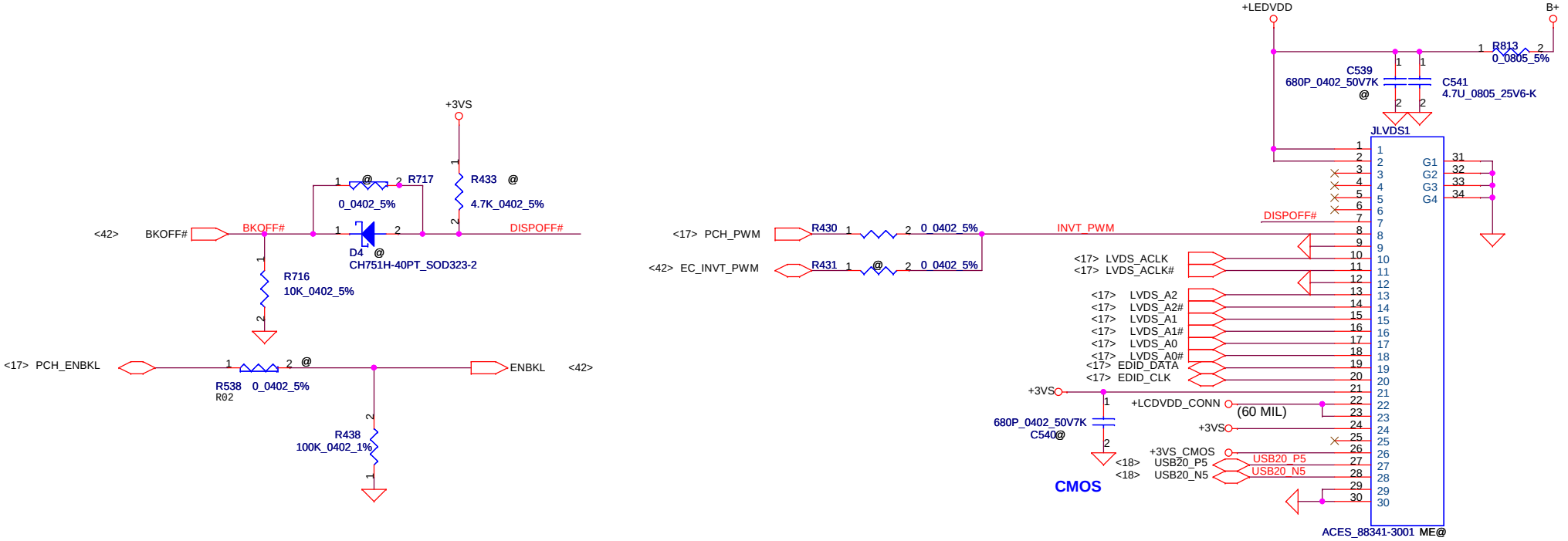
LCD POWER CIRCUIT



CMOS Camera



VGA LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size	Document Number	Rev
Custom	LA-7981P	0.2

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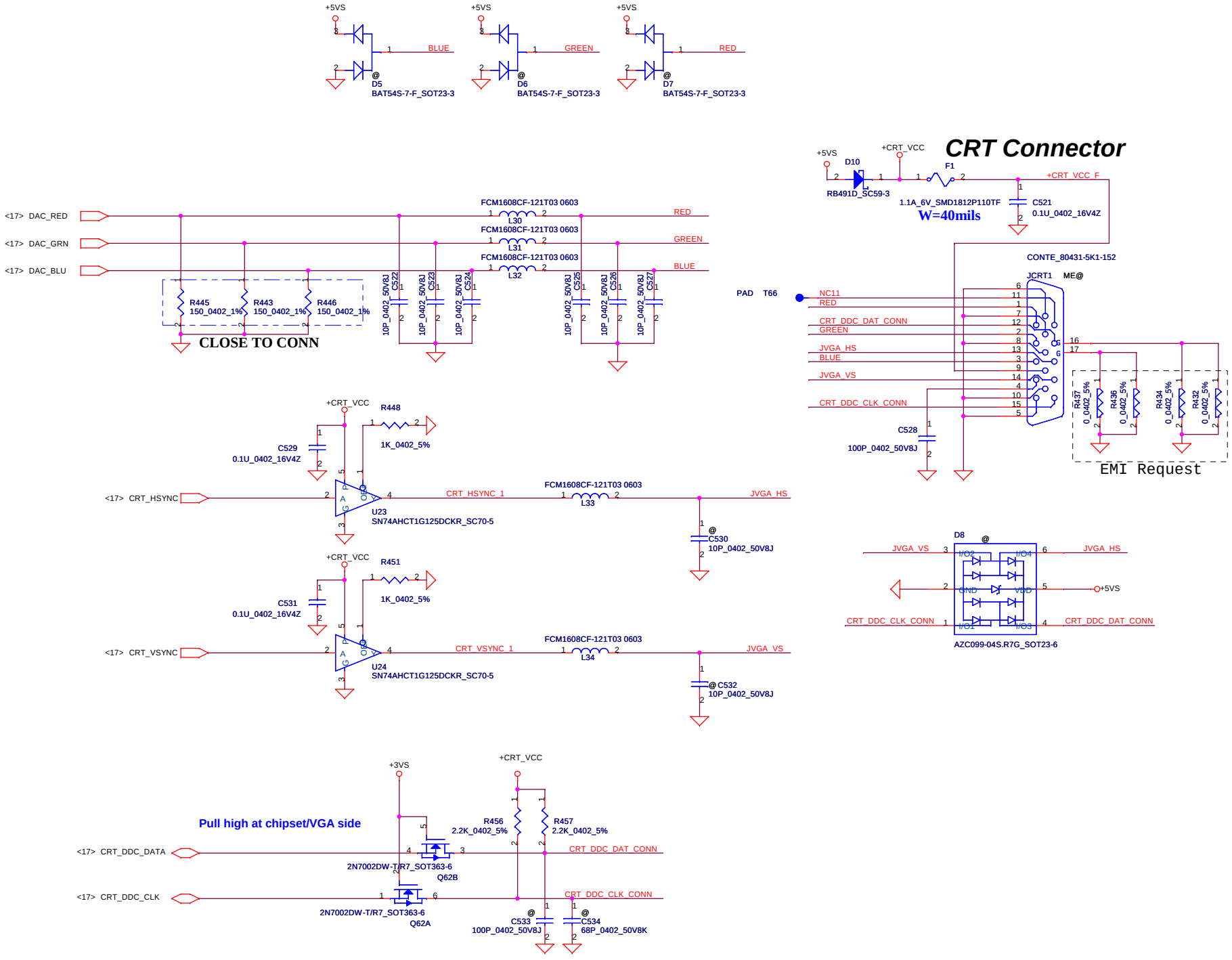

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **CRT Connector**

Size	Document Number	Rev
Custom	LA-7981P	0.2

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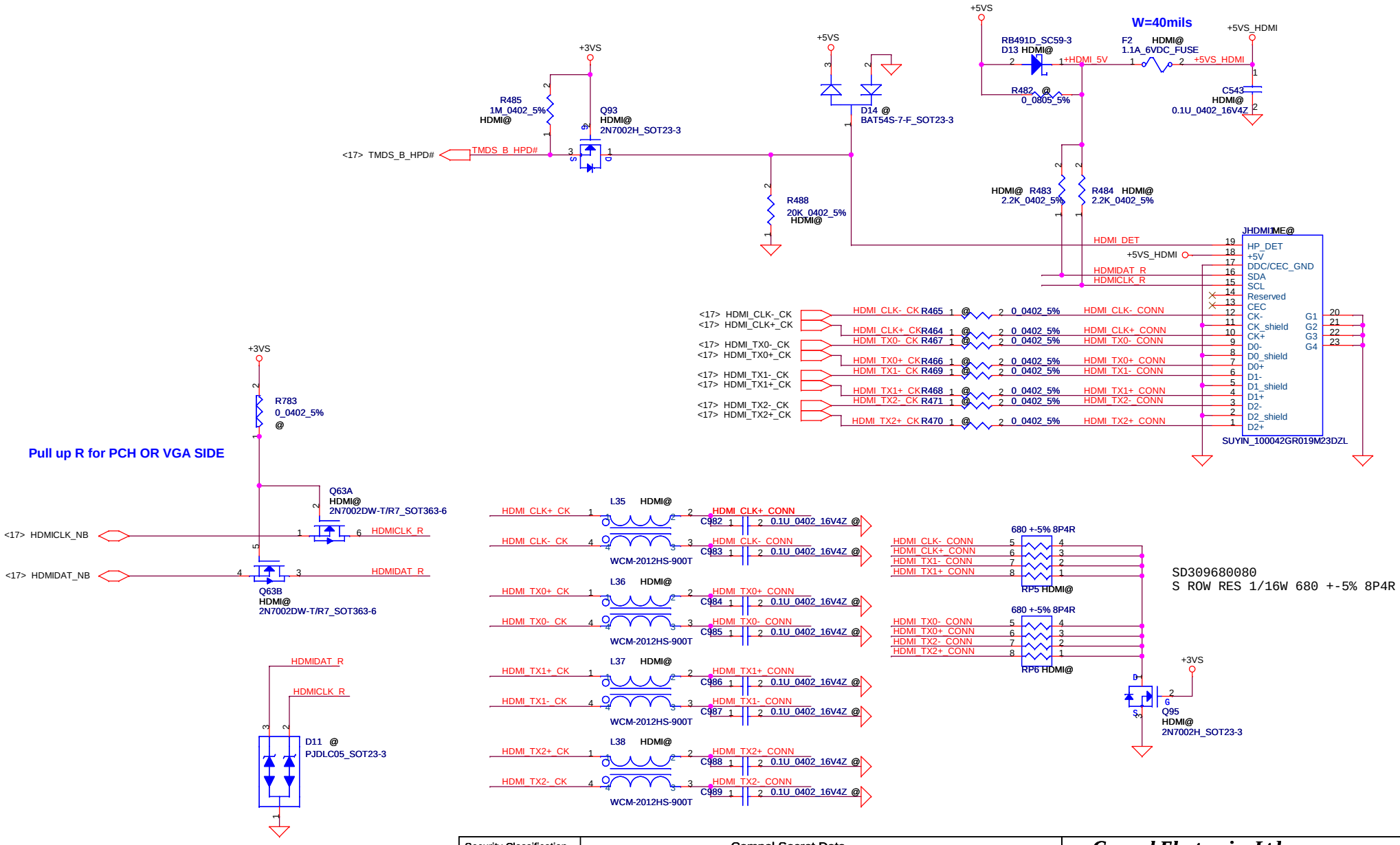

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics,Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
B	LA-7981P	0.2

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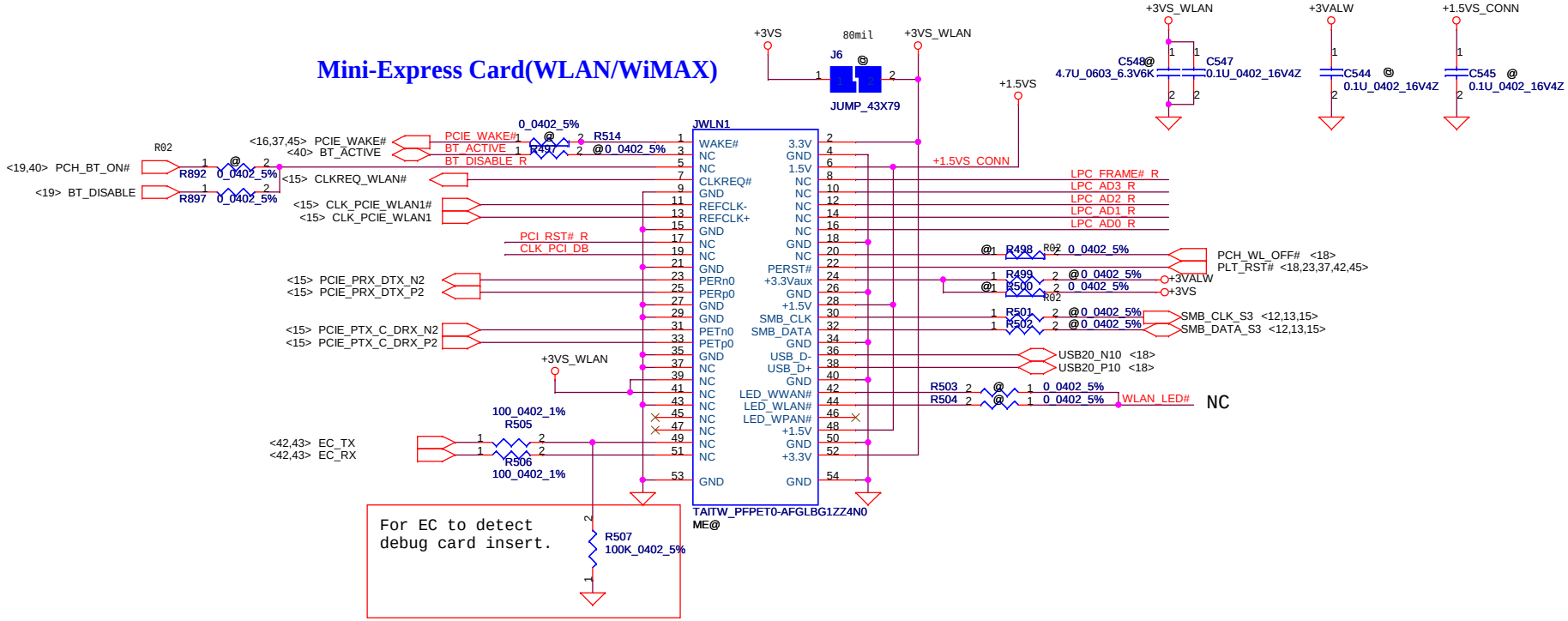
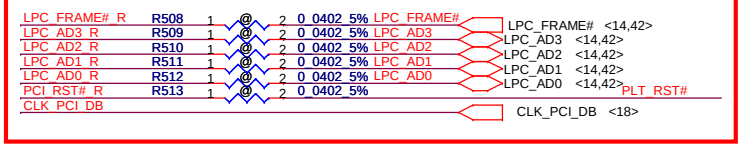
Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **Mini-Card/NEW Card/SIM**

Size	Document Number	Rev
	LA-7981P	0.2

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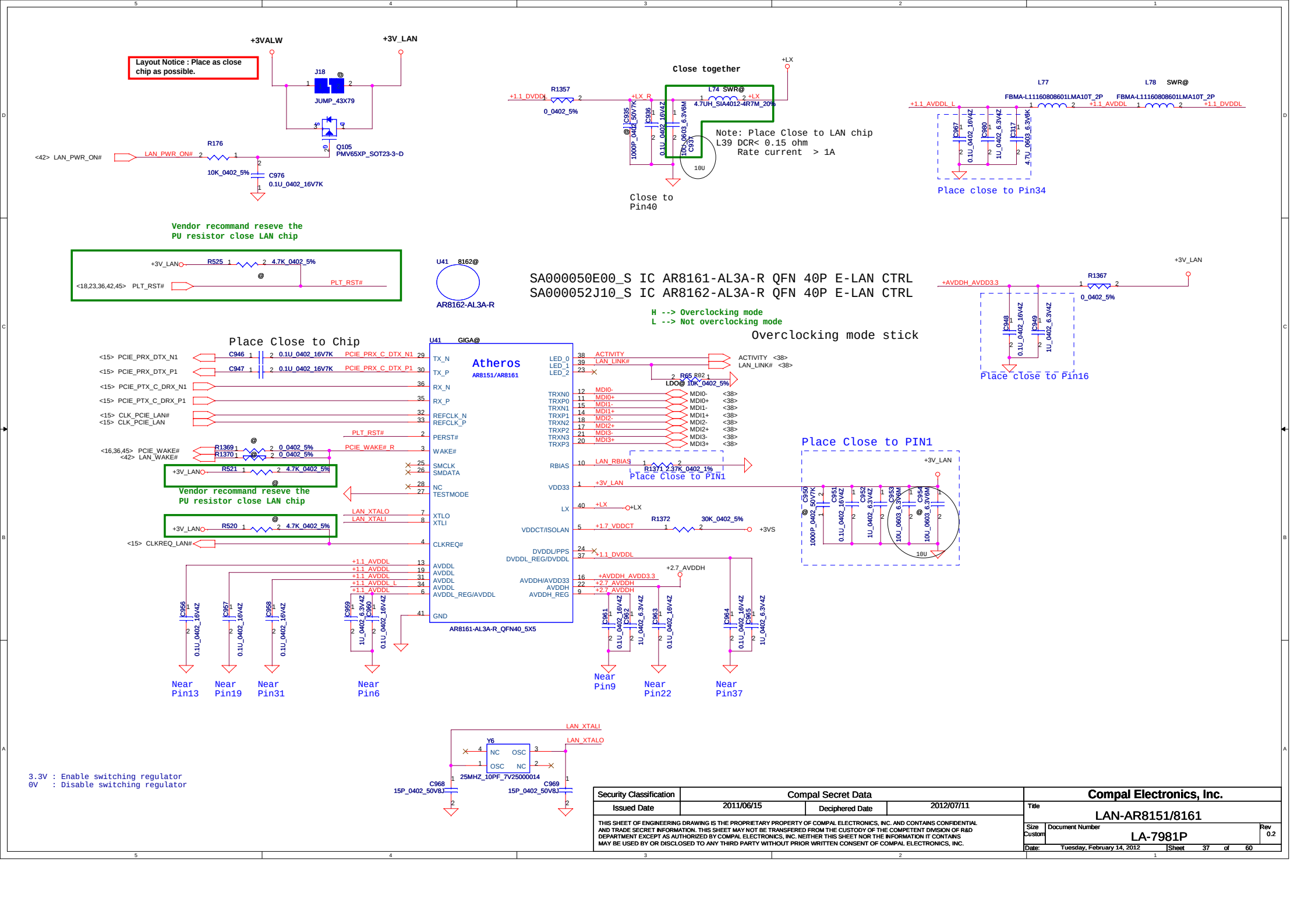

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN-AR8151/8161

Size	Document Number	Rev
Custom	LA-7981P	0.2

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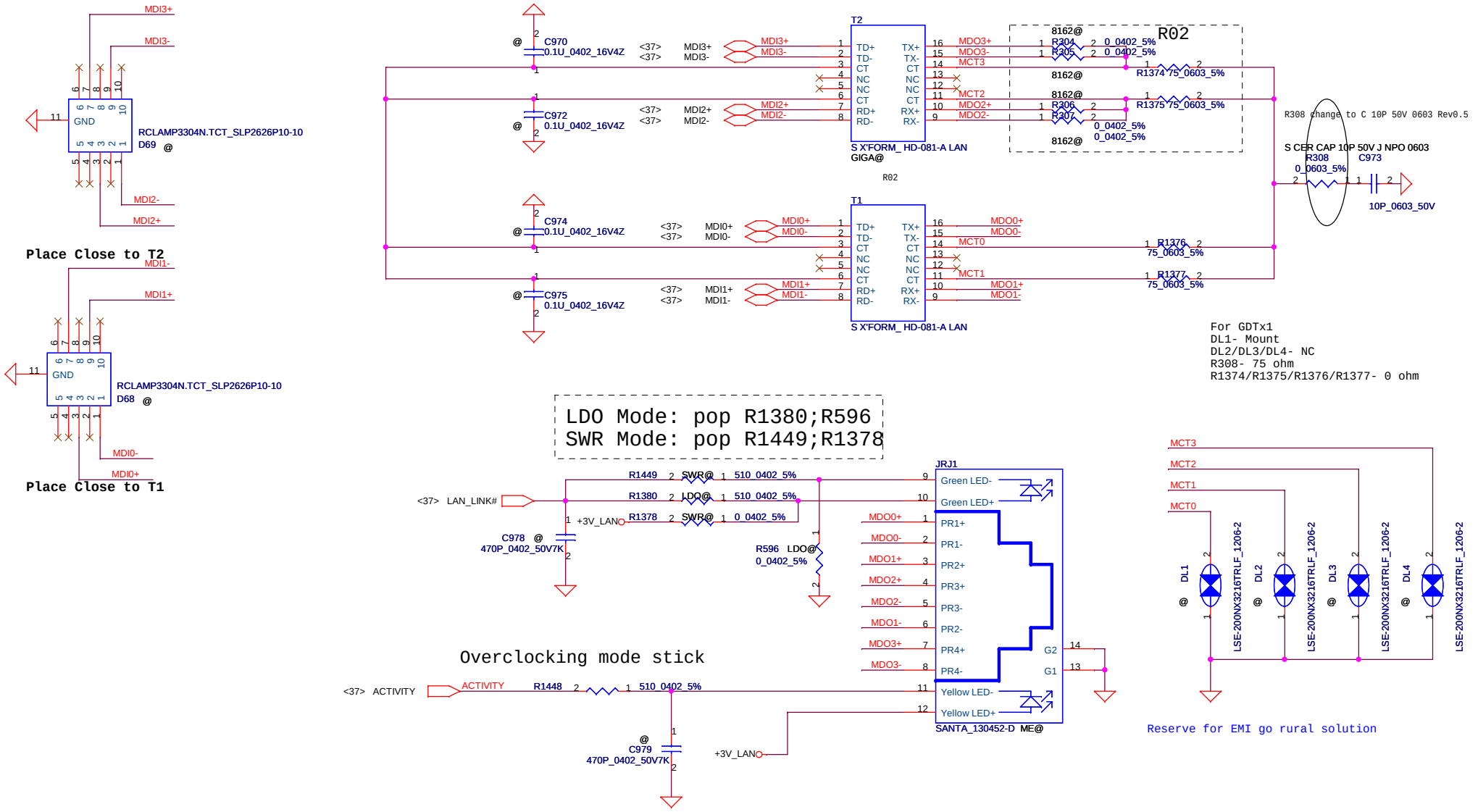

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN_Transformer

Size	Document Number	Rev
B	LA-7981P	0.2

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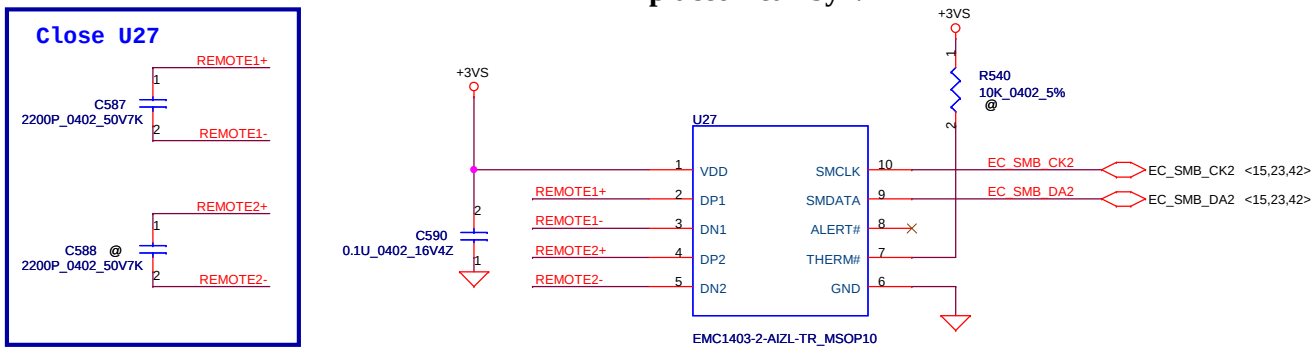
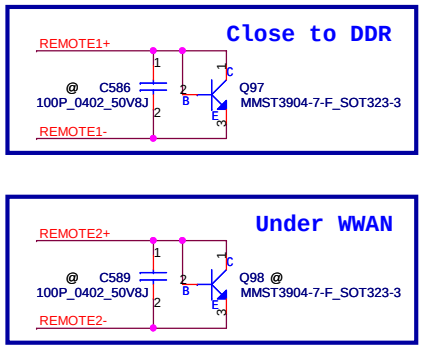
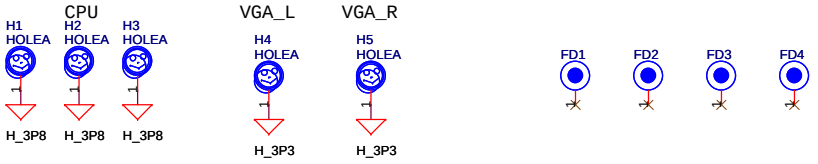
SMSC thermal sensor placed near by VRAM



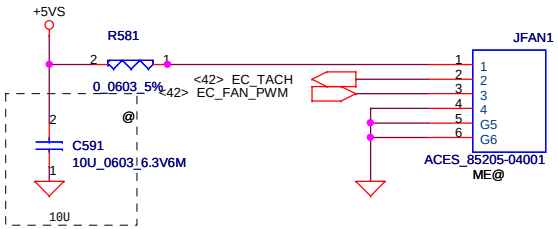
Address 1001_101xb

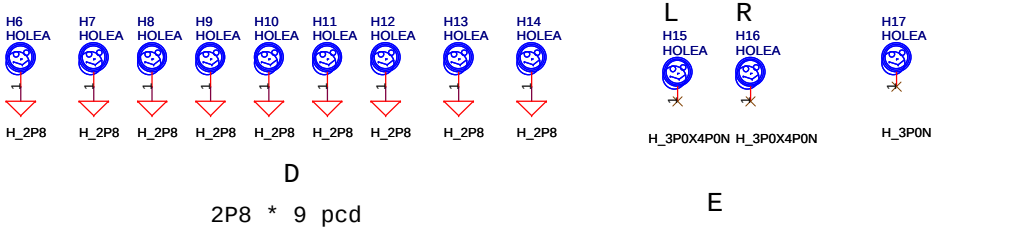


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics,Ltd.	
Title	Fintek-Thermal IC/FAN/screw
Size B	Document Number LA-7981P
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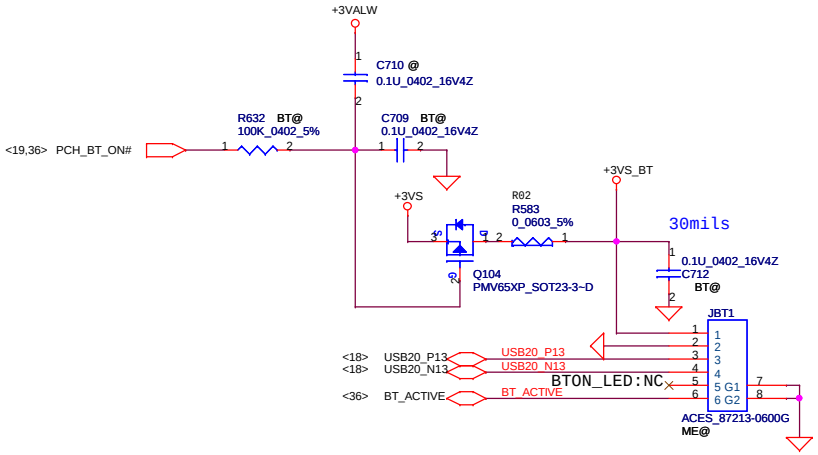
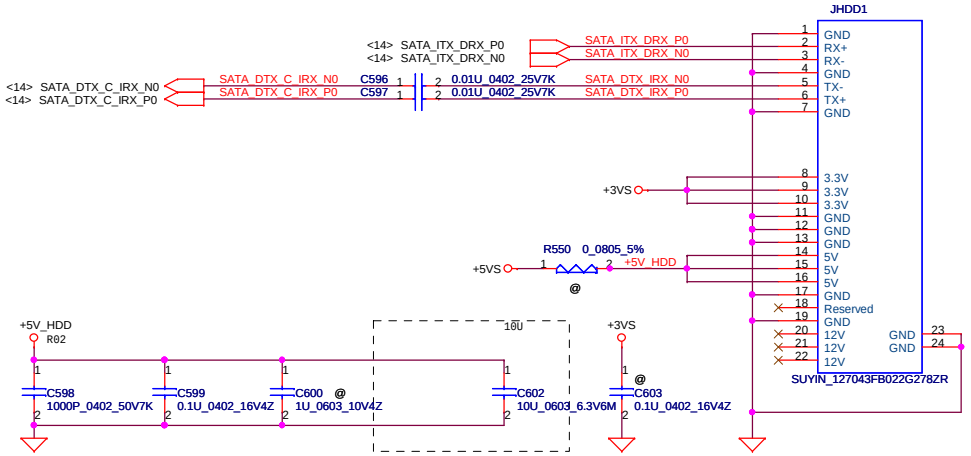
Date: Tuesday, February 14, 2012	Sheet 39 of 60

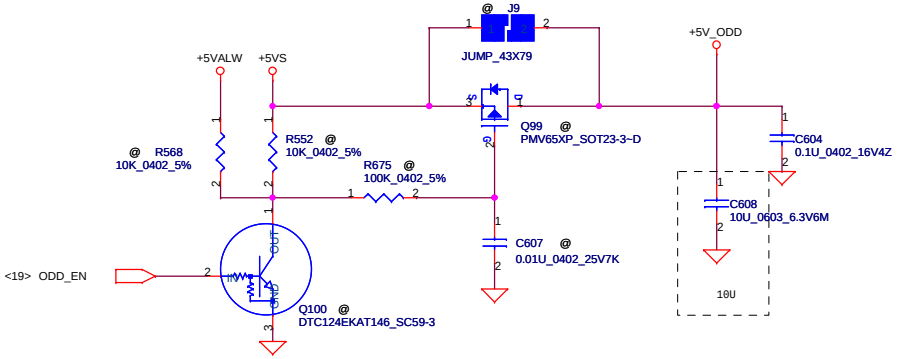
BT MODULE CONN



SATA HDD Conn.

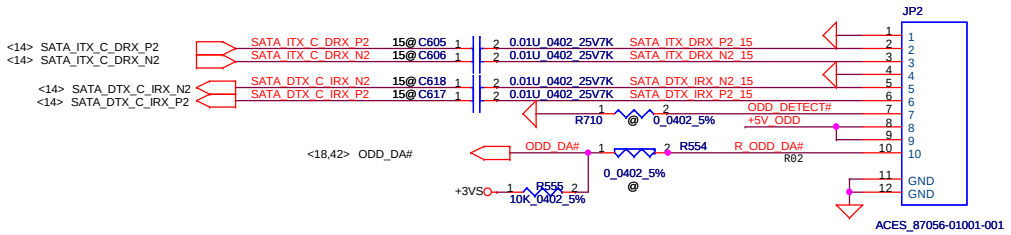


ODD Power Control



FOR 15"

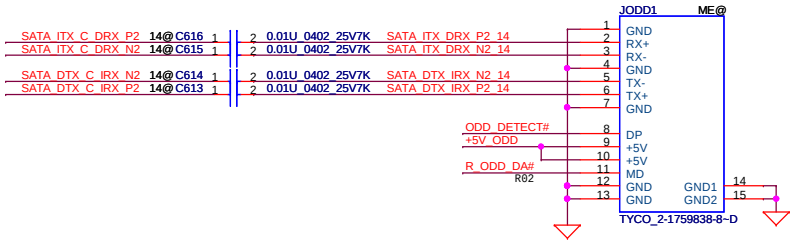
SATA ODD FFC Conn.



Co-lay

FOR 14"

SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **HDD/ODD/BT Connector**

Size	Document Number	Rev
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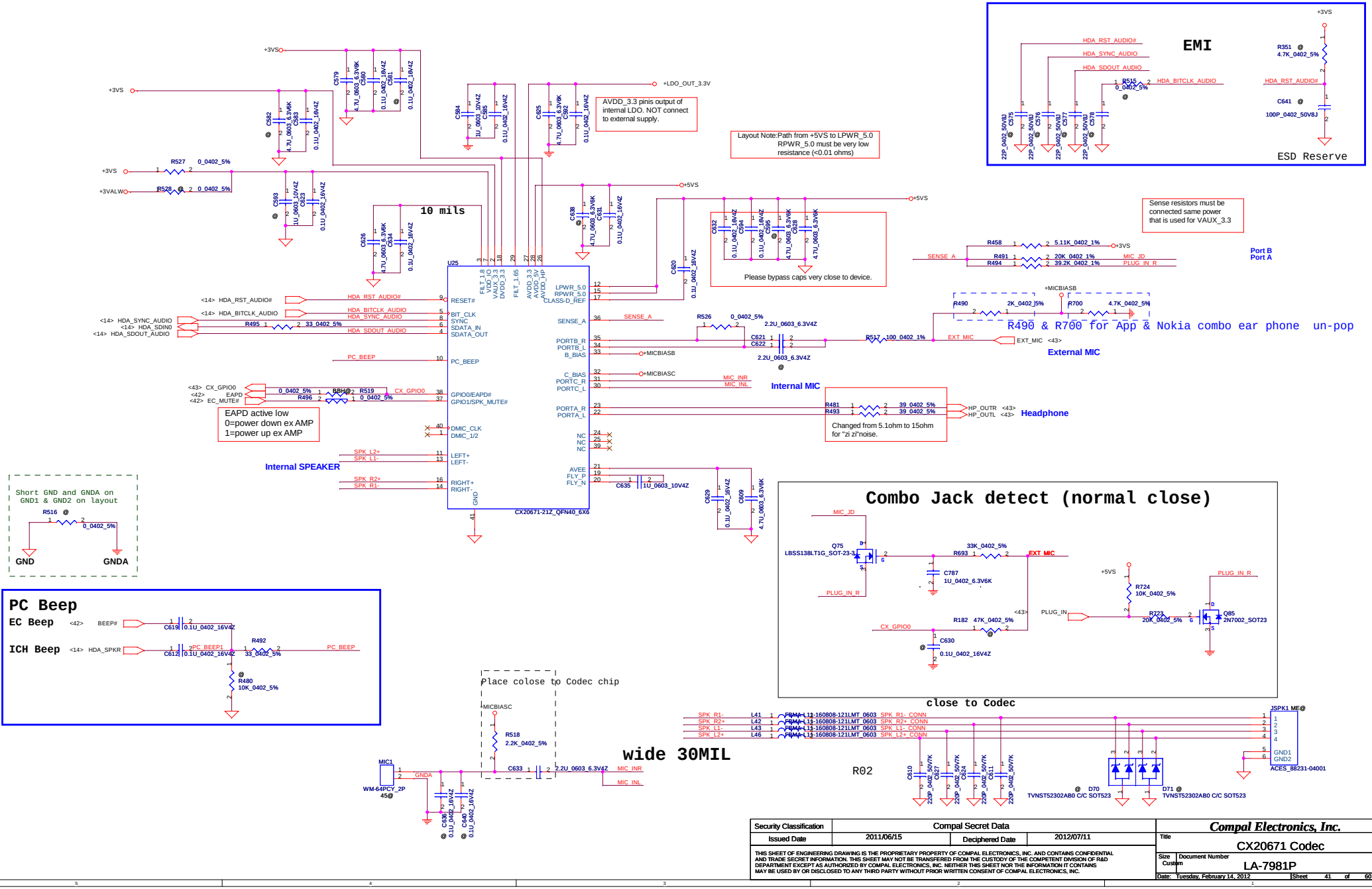
CX20671
High Definition Audio Codec SoC With Integrated Class-D Stereo Amplifier.
An integrated 5 V to 3.3 V Low-dropout voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CX20671 Codec

Size: Custom | Document Number: LA-7981P | Rev: 0.2

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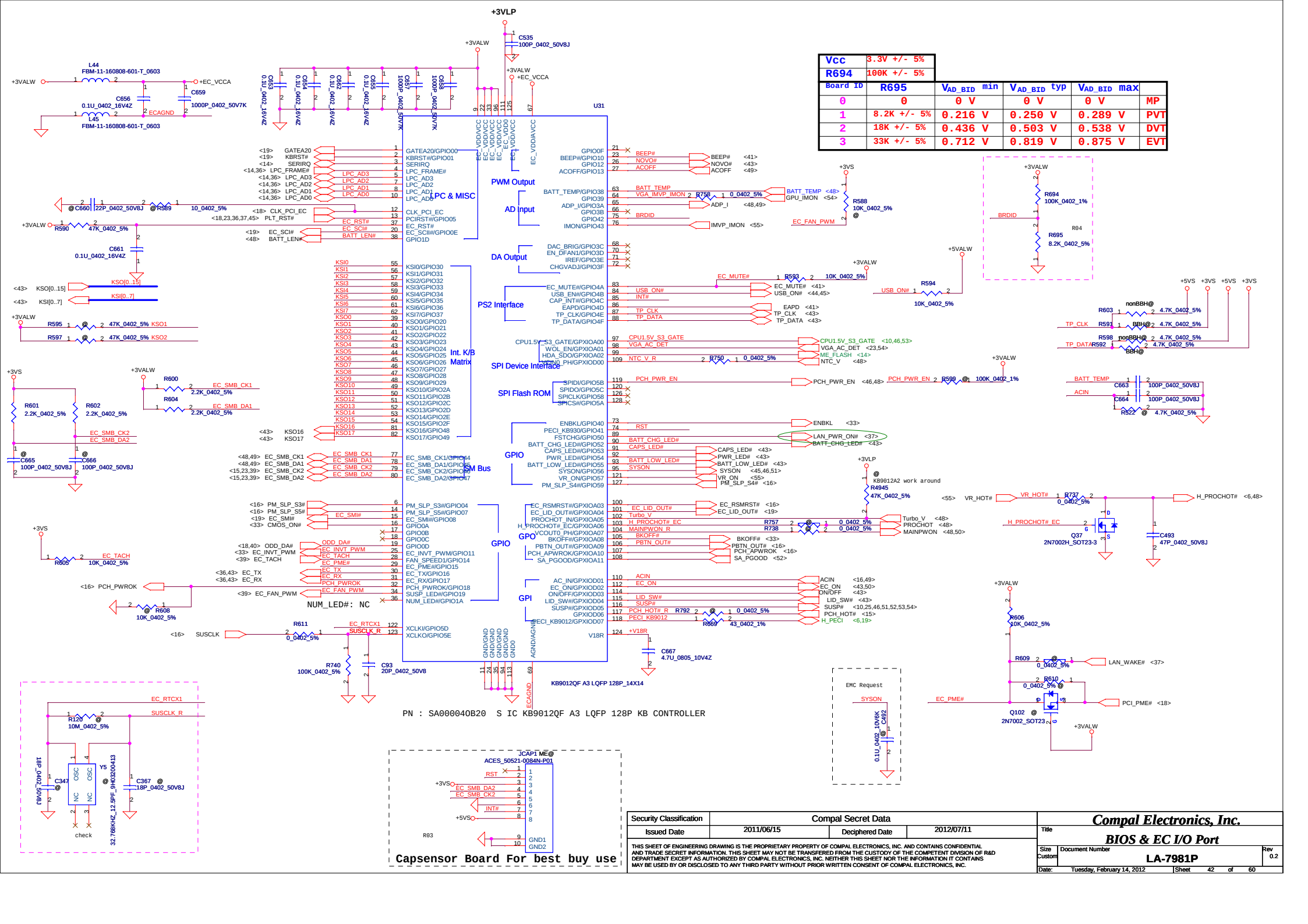
+3VLP
U31
KB9012QF A3 LQFP 128P_14X14
PN : SA00004OB20 S IC KB9012QF A3 LQFP 128P KB CONTROLLER
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
NUM_LED#: NC
Capsensor Board For best buy use
EMC Request
KB9012A2 work around
Vcc 3.3V +/- 5%
R694 100K +/- 5%
Board ID | R695 | VAD_BID min | VAD_BID typ | VAD_BID max
0 | 0 | 0 V | 0 V | 0 V | MP
1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | PVT
2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | DVT
3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | EVT
Security Classification
Compal Secret Data
Issued Date
2011/06/15
Deciphered Date
2012/07/11
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Compal Electronics, Inc.
Title
BIOS & EC I/O Port
Size Custom
Document Number
LA-7981P
Rev 0.2
Date: Tuesday, February 14, 2012
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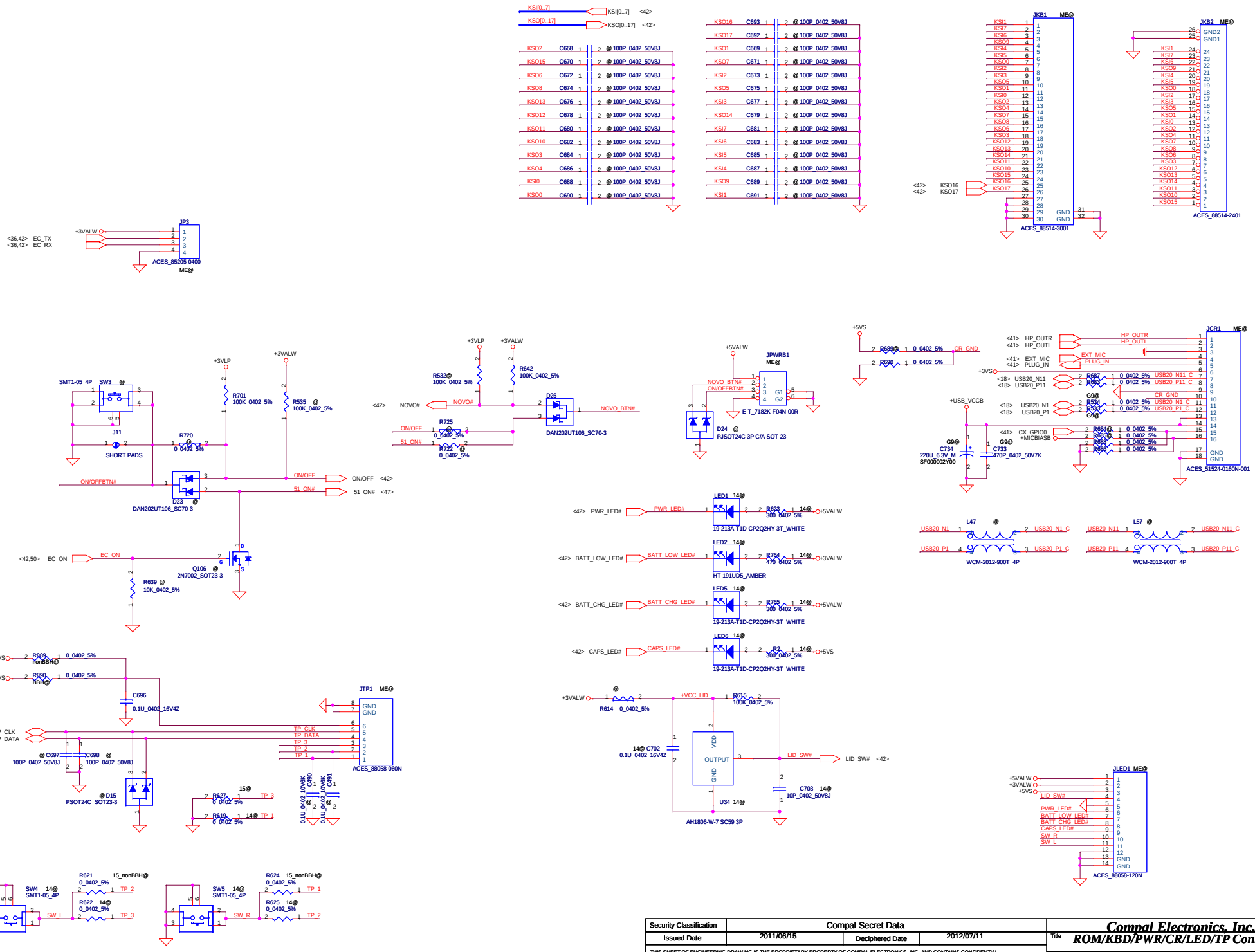

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	Compal Electronics, Inc. ROM/KBD/PWR/CR/LED/TP Conn.		
Size C	Document Number LA-7981P		Rev 0.2
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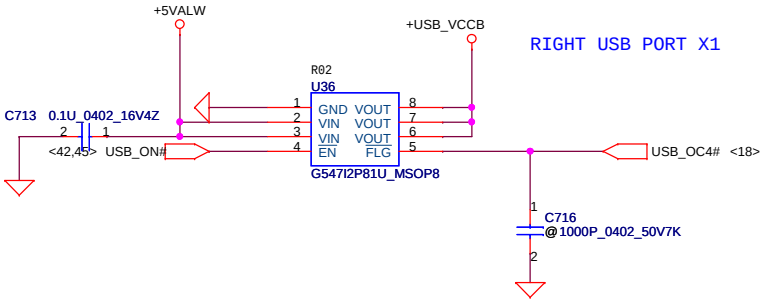
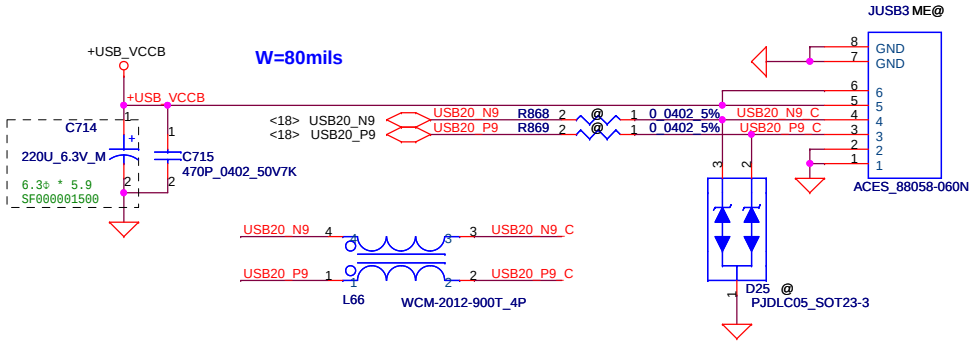
Right Ext.USB Conn.





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: USB ext. ports

Size	Document Number	Rev
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+1.5V to +1.05V Transfer

Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

+3VALW to +3V Transfer

For EMI request

Place TX AC coupling Cap (C843~C850). Close to connector

2A/Active Low

W=80mils

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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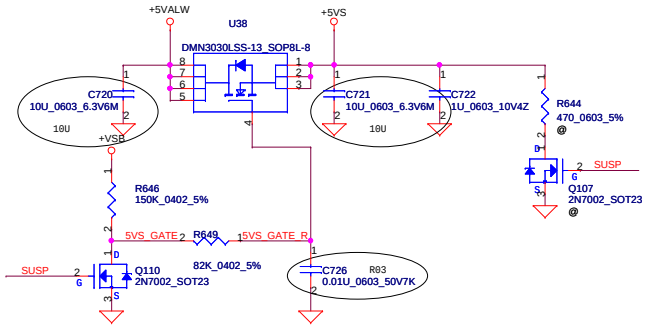
Compal Electronics, Inc.

Title: USB3.0/Left USB Ports

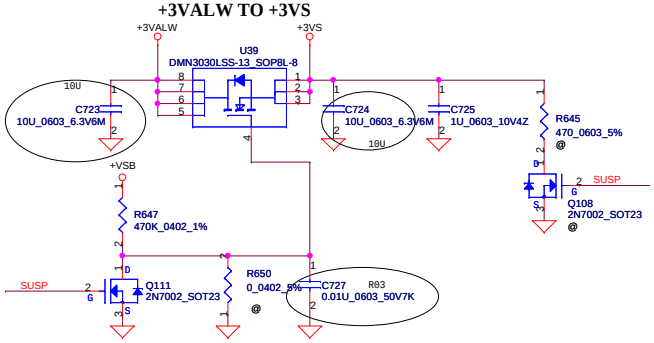
Size	Document Number	Rev
Custom		0.2

Date: Tuesday, February 14, 2012 Sheet 45 of 60

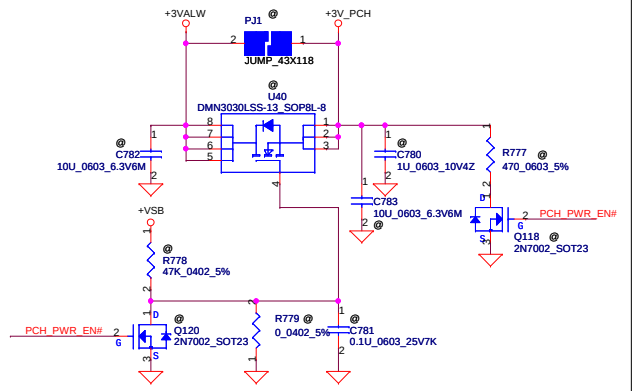
+5VALW TO +5VS

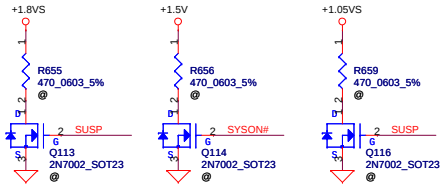


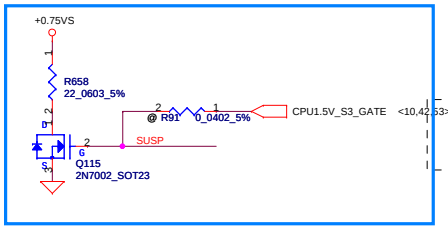
+3VALW TO +3VS



+3VALW TO +3VALW(PCH AUX Power)

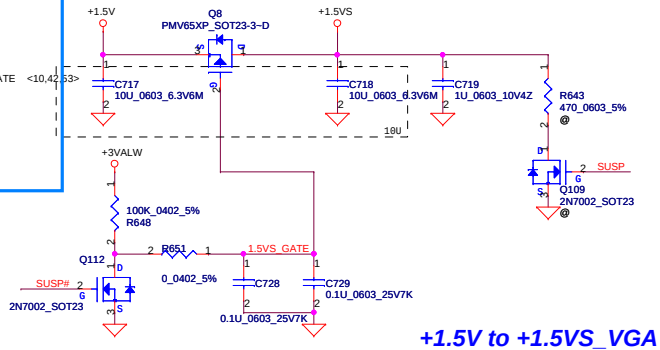


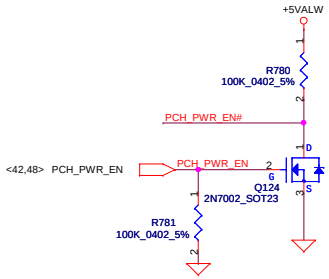


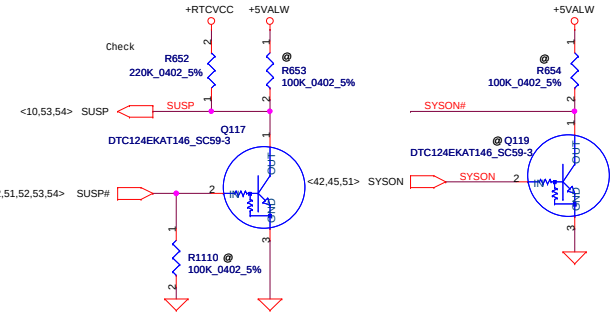


For Intel S3 Power Reduction.

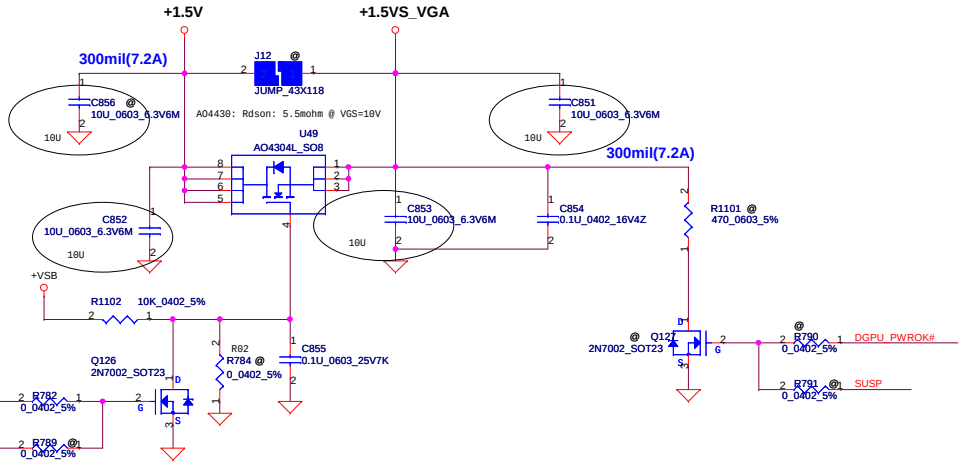
+1.5V to +1.5VS

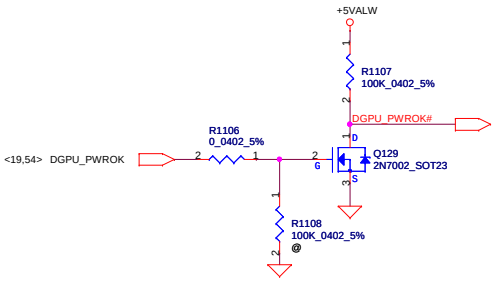






+1.5V to +1.5VS_VGA Transfer





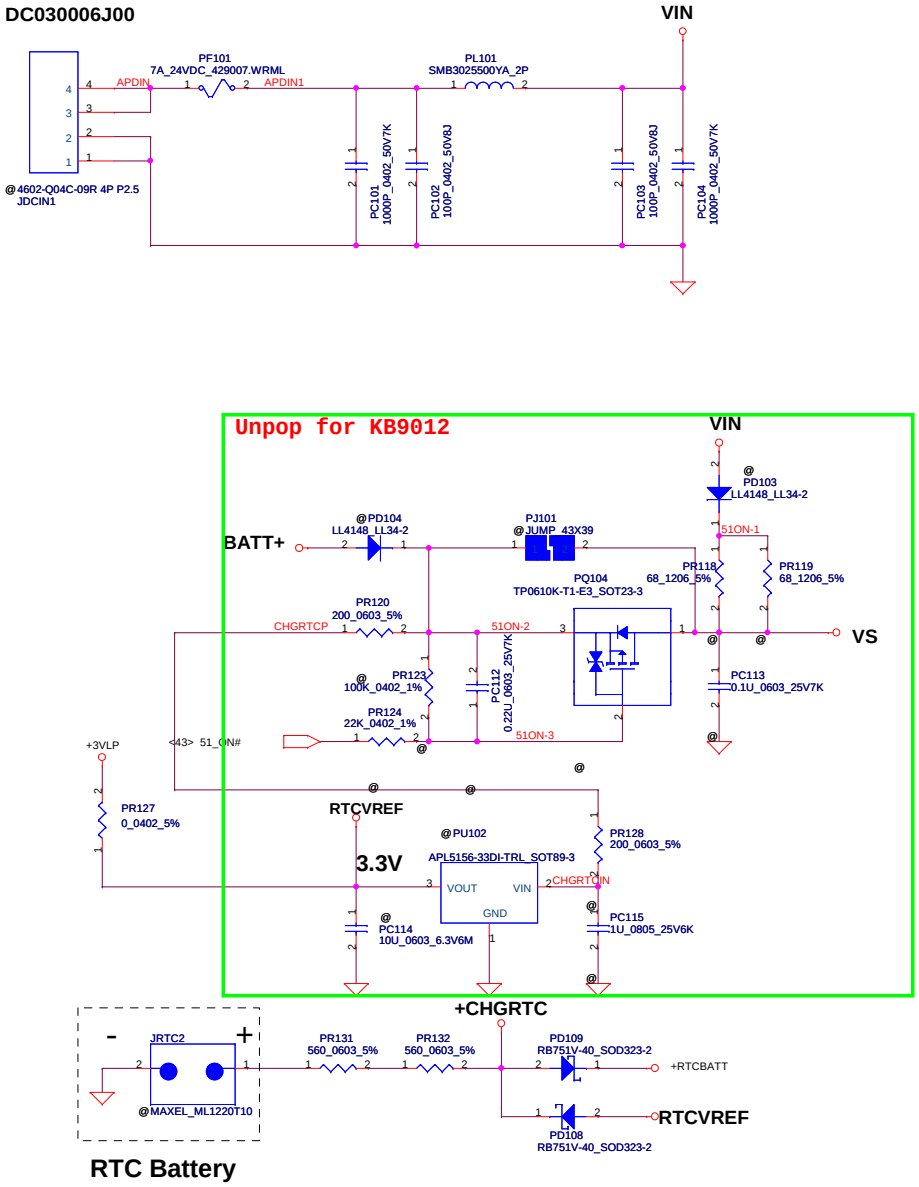
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-7981P	0.2

Date: Tuesday, February 14, 2012 | Sheet 46 of 60



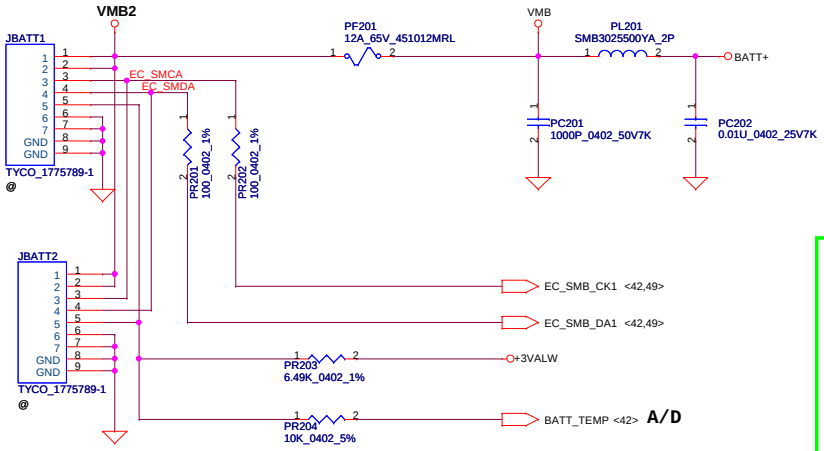
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR DCIN / Vin Detector /Pre-charge

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Tuesday, February 14, 2012 | Sheet 47 of 60

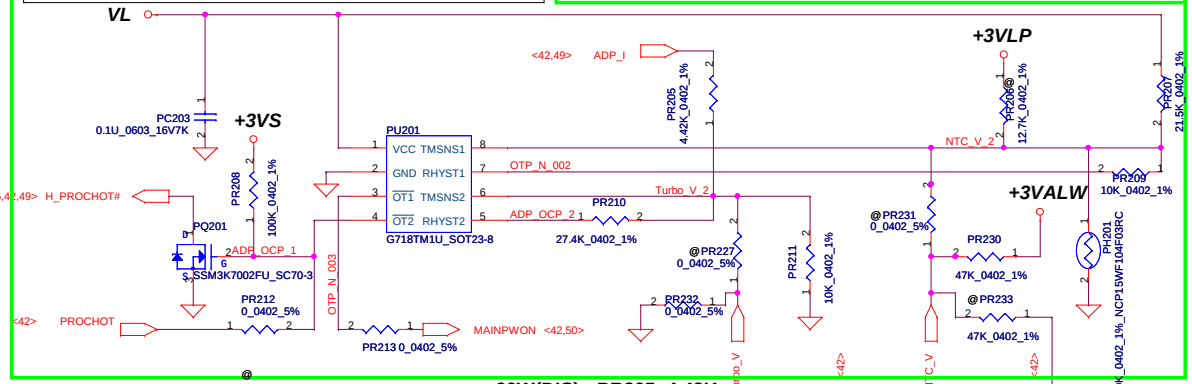


ADP_I need to write Charge Options Register (0x12H)=> bit6=1

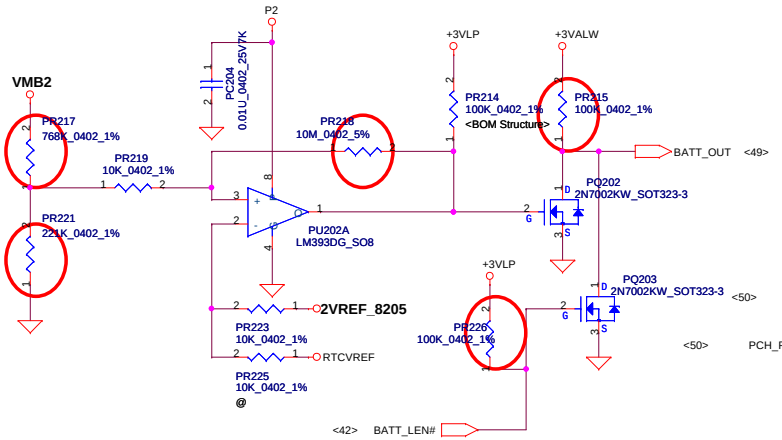
0: IOUT is the 20x current amplifier output <default @ POR>
1: IOUT is the 40x current amplifier output

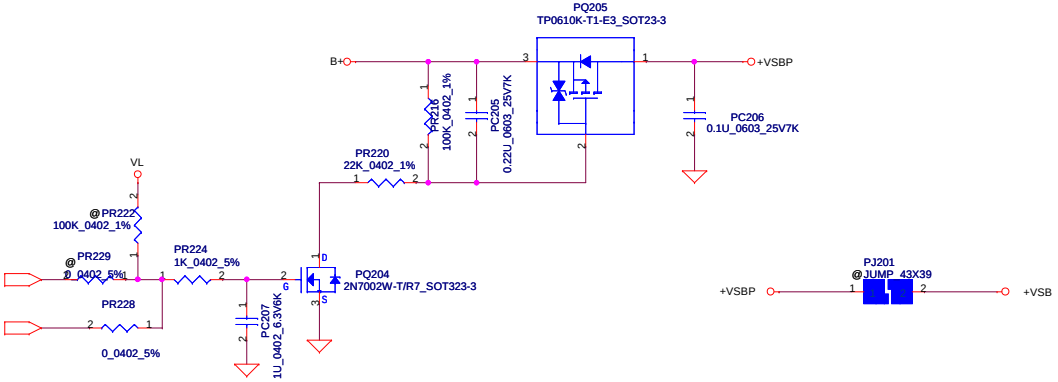
PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU201 circuit
(Vth = 1.25V)
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211,PQ201,PR208,PR212



90W(DIS) : PR205=4.42K
PR210=27.4K
65W(UMA) : PR205=402(SD034020080)
PR210=5.11K





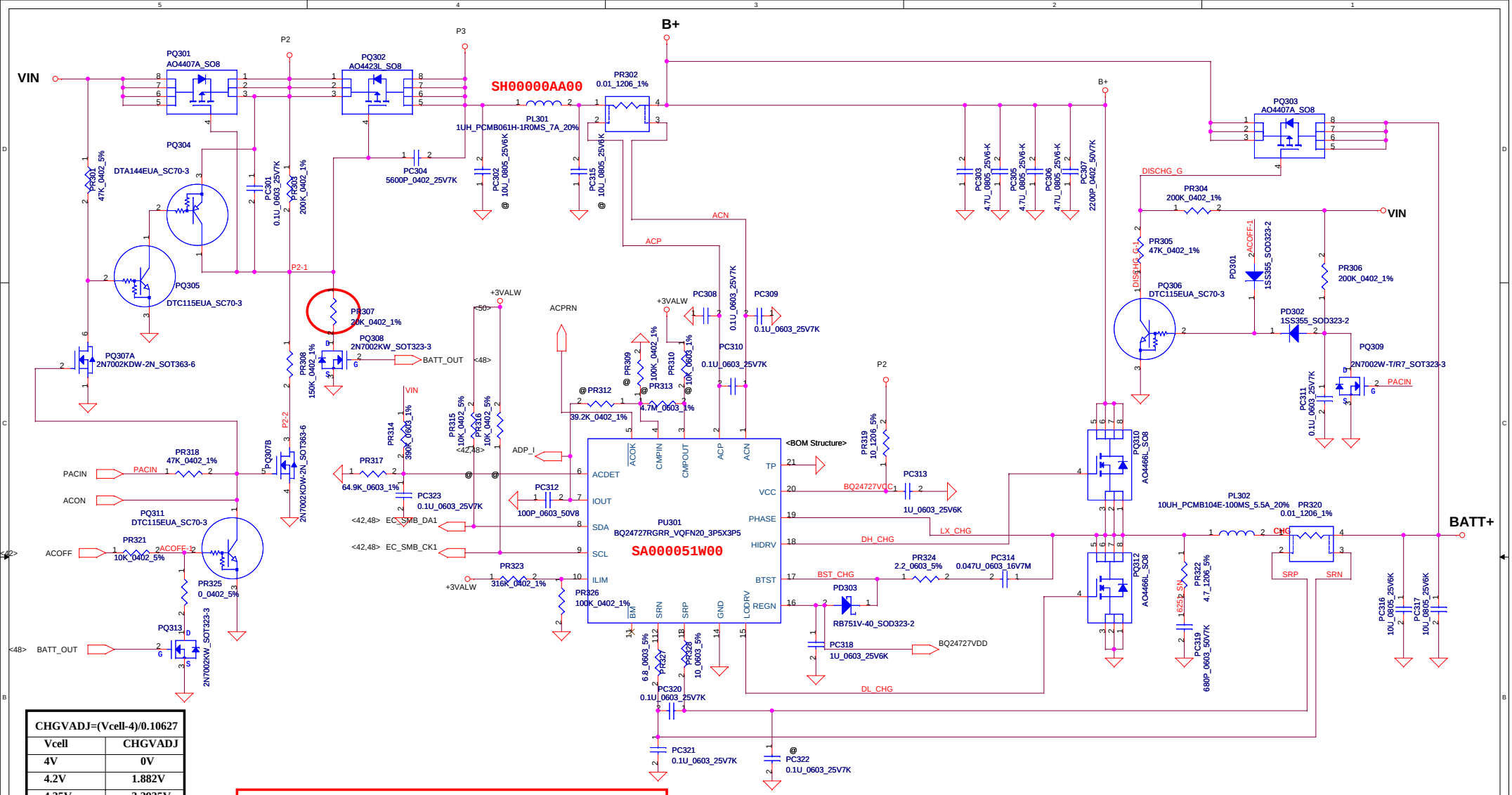
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Tuesday, February 14, 2012 | Sheet 48 of 60



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2012/07/11

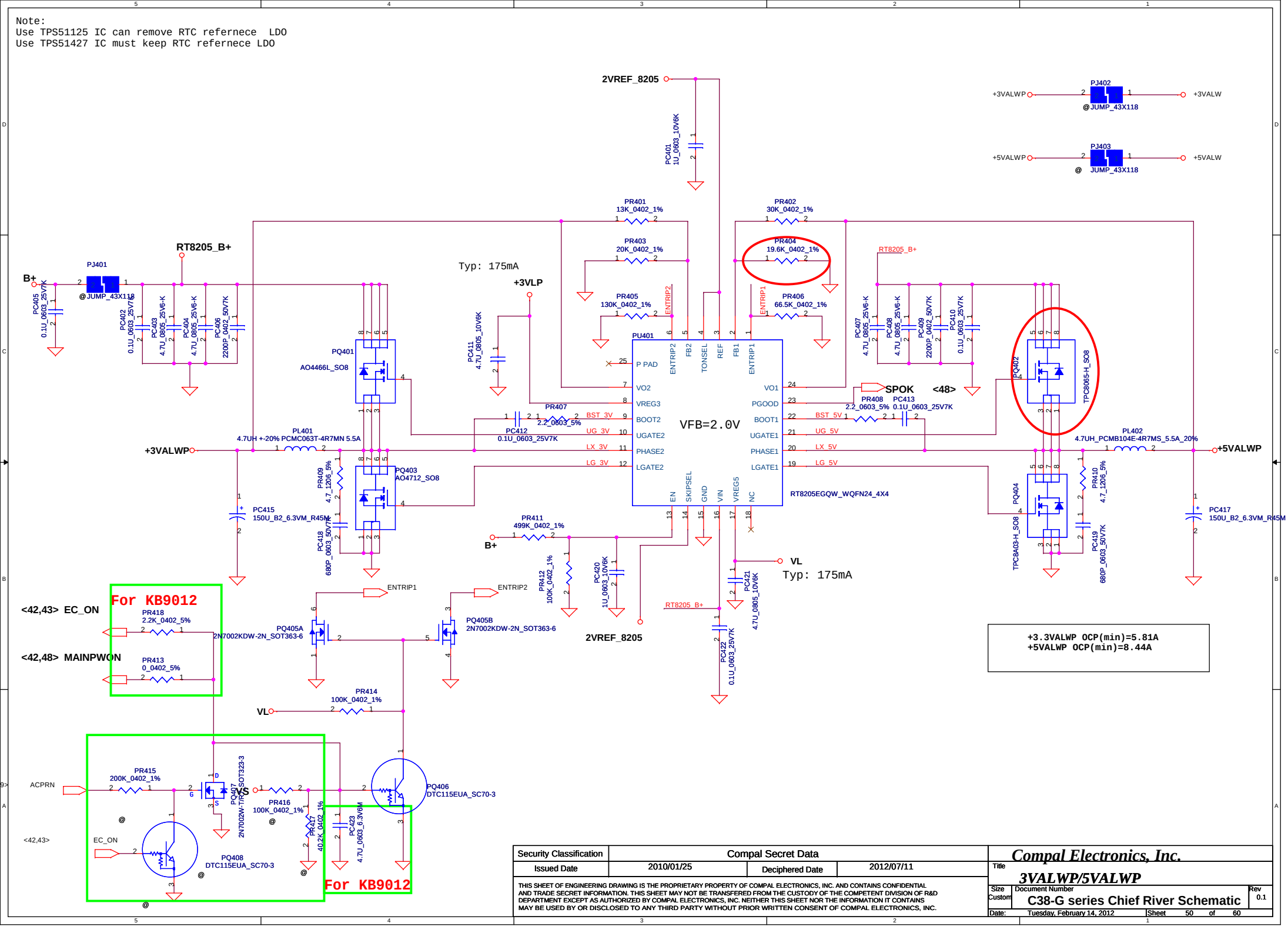
Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Tuesday, February 14, 2012 | Sheet 49 of 60

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



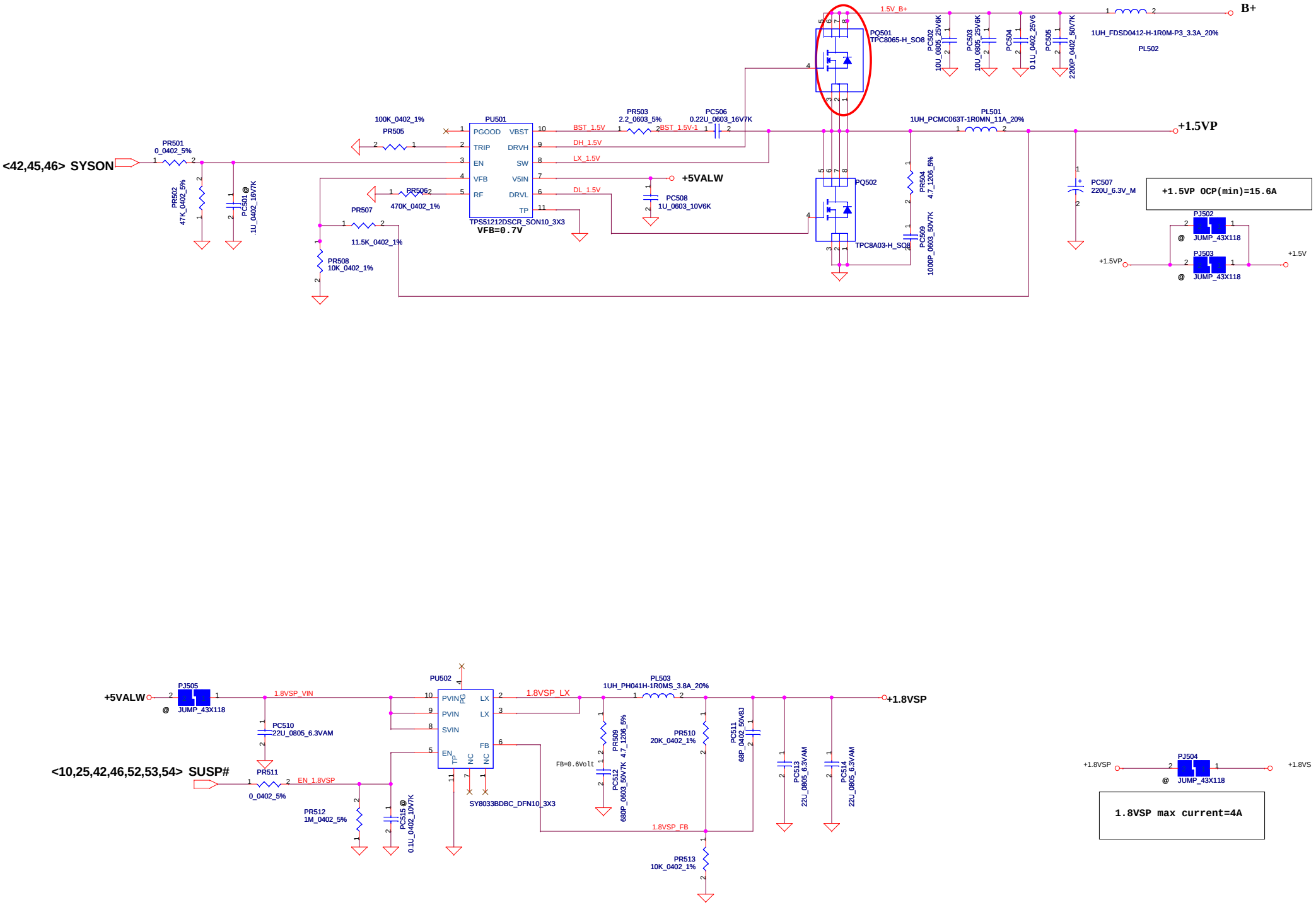
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	C38-G series Chief River Schematic	0.1

Date: Tuesday, February 14, 2012 | Sheet 50 of 60



Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.8VSP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Tuesday, February 14, 2012 | Sheet 51 of 60

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

+VCCSAP PJ602 JUMP_43X118 +VCCSA

+3VS PR601 1K_0402_5% H_VCCSA_VID1 <10>
PR602 100K_0402_5% VCCSA_PWRGD
H_VCCSA_VID0 <10>
PR603 1K_0402_5%
<42> SA_PGOOD

+5VALW PR604 10_0402_1% PC601 1U_0603_10V6K PC602 2.2U_0603_10V7K
+VCCSA_EN PR605 0_0402_5% +V1.05S_VCCP_PWRGOOD <53>

PU601 TPS51461RGER_QFN24_4X4
V5DRV V5FILT PGOOD VID1 VID0 EN
PGND PGND PGND VIN VIN VIN
BST SW SW SW SW SW TP
GND VREF COMP SLEW VOUT MODE

+VCCSA_BT PR606 0_0603_5% PC603 0.22U_0603_16V7K
+VCCSA_PHASE PL601 0.47UH_FDVE0630-H-R47M=P3_17.7A_20%
PR607 4.7_1206_5% PC604 1000P_0603_50V7K
PR608 33K_0402_5%
PC605 22U_0805_6.3V6M PC608 22U_0805_6.3V6M PC607 0.1U_0402_10V7K PC608 22U_0805_6.3V6M PC609 22U_0805_6.3V6M PC610 2200P_0402_50V7K PC611 22U_0805_6.3V6M PC612 22U_0805_6.3V6M
+VCCSAP

+3VALW PJ601 JUMP_43X118 +VCCSA_PWR_SRC
2200P_0402_50V7K PC613 0.1U_0603_25V7K PC614 10U_0805_6.3V6M PC615 10U_0805_6.3V6M PC616

PC617 0.22U_0402_10V6K
PC618 3300P_0402_50V7K
PR610 5.1K_0402_1%
PC619 0.01U_0402_25V7K
PR609 100_0402_5%
PR611 0_0402_5% +VCCSA_SENSE <10>

+3VS PR612 100K_0402_5%
<53> +V1.05S_VCCP_PWRGOOD
PR613 0_0603_5% PC624 0.22U_0603_16V7K
PR614 66.5K_0402_1%
PR615 0_0402_5% <10,25,42,46,51,53,54> SUSP#
PC625 0.1U_0402_16V7K
PR616 470K_0402_1%

PU602 TPS51212DSCR_SON10_3X3
PGOOD VBST BST_+V1.05S_VCCPP
TRIP DRVH UG_+V1.05S_VCCPP
EN SW SW_+V1.05S_VCCPP
VFB VSIN +V1.05S_VCCP_5V
RF DRVL LG_+V1.05S_VCCPP
TP
TRIP_+V1.05S_VCCPP
EN_+V1.05S_VCCPP
FB_+V1.05S_VCCPP
RF_+V1.05S_VCCPP

+5VALW PC626 1U_0603_6.3V6M

PQ601 TPC8037-H_SO8
PC620 0.1U_0402_25V6 PC621 2200P_0402_50V7K PC622 4.7U_0805_25V6K PC623 4.7U_0805_25V6K
+V1.05S_VCCPP_B+ PJ603 JUMP_43X118 B+
PL602 1UH_PCMC063T-1R0MN_11A_20%
+V1.05S_VCCPP
PQ602 TPC8A03-H_SO8
PR617 4.7_1206_5% PC628 1000P_0603_50V7K
PC627 0.1U_0402_10V7K

+V1.05S_VCCPP PJ604 JUMP_43X118 +V1.05S_VCCP
PC631 150U_B2_6.3VM_R45M

PC629 1000P_0402_50V7K PR618 1.2K_0402_1%
PR619 4.32K_0402_1%
PR620 0_0402_5% VCCIO_SENSE <9,53>

+3VS PR621 10K_0402_1% PR622 71.5K_0402_1%
PQ603 SSM3K702FU_SC70-3
PR623 100K_0402_5% PR624 0_0402_5% VCCP_PWRCTRL <10>
PC630 .01U_0402_16V7K PR625 100K_0402_5%

VCCP_PWRCTRL = "High" , Vo = 1.05V (SNB)
VCCP_PWRCTRL = "Low" , Vo = 1V (IVB)

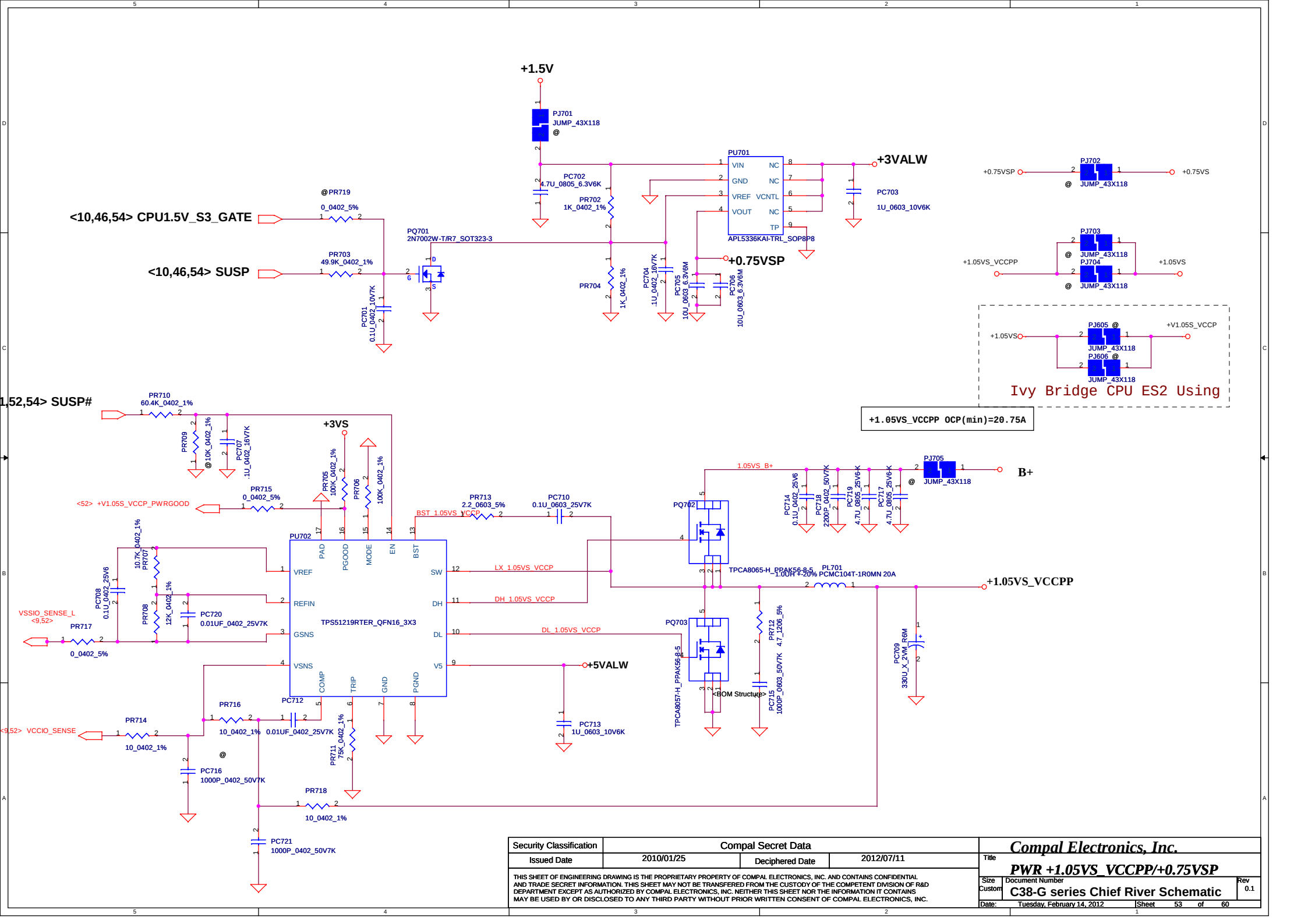
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR +VCCSAP/1.0

Size: C | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Tuesday, February 14, 2012 | Sheet 52 of 60



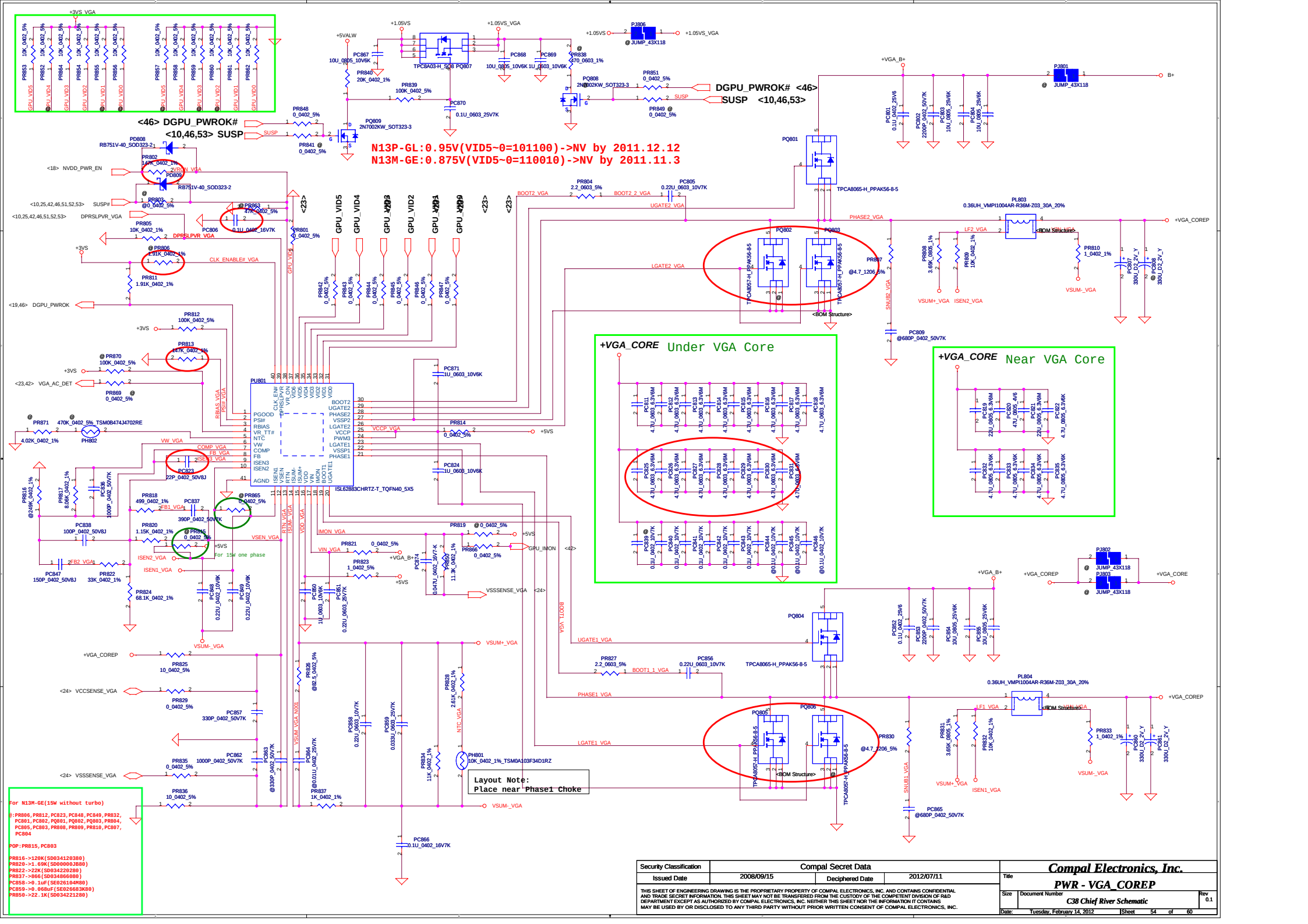
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size	Document Number	Rev
Custom	C38-G series Chief River Schematic	0.1

Date: Tuesday, February 14, 2012 Sheet 53 of 60


N13P-GL:0.95V(VID5~0=101100)->NV by 2011.12.12
N13M-GE:0.875V(VID5~0=110010)->NV by 2011.11.3
<46> DGPU_PWROK#
<10,46,53> SUSP
DGPU_PWROK# <46>
SUSP <10,46,53>
+VGA_CORE Under VGA Core
+VGA_CORE Near VGA Core
PU801
ISL62883CHRTZ-T_TQFN40_5X5
PQ801
PQ802
PQ803
PQ804
PQ805
PQ806
TPCA8065-H_PPAK56-8-5
TPCA8057-H_PPAK56-8-5
PL803
0.36UH_VMPI1004AR-R36M-Z03_30A_20%
PL804
0.36UH_VMPI1004AR-R36M-Z03_30A_20%
PH801
10K_0402_1%_TSM0A103F34D1RZ
PH802
470K_0402_5%_TSM0B474J4702RE
Layout Note:
Place near Phase1 Choke
For N13M-GE(15W without turbo)
R:PR806,PR812,PC823,PC848,PC849,PR832,
PC801,PC802,PQ801,PQ802,PQ803,PR804,
PC805,PC803,PR808,PR809,PR810,PC807,
PC804
POP:PR815,PC803
PR816->120K(SD034120380)
PR820->1.69K(SD00000JB80)
PR822->22K(SD034220280)
PR837->866(SD034866080)
PC858->0.1uF(SE026104M80)
PC859->0.068uF(SE026683K80)
PR856->22.1K(SD034221280)
Security Classification
Compal Secret Data
Issued Date
2008/09/15
Deciphered Date
2012/07/11
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Compal Electronics, Inc.
Title
PWR - VGA_COREP
Size
Document Number
C38 Chief River Schematic
Rev
0.1
Date: Tuesday, February 14, 2012
Sheet 54 of 60

PR915,PR946=200K(setting 113 degreeC)
PR915,PR946=8.25K(setting 93 degreeC)

PUT COLSE TO GT Inductor

PUT COLSE TO V_GT HOT SPOT

PUT COLSE TO VCORE Phase 1 Inductor

PUT COLSE TO VCORE HOT SPOT

2P: 24K
1P: 24.9K

2P: 21.5K
1P: 15.8K

2P: 1.65K
1P: 1K

2P: 36K
1P: 26.1K

Option for 1 phase GFX
2Phase: @
1Phase: install

Option for 2 phase CPU
3Phase: @
2Phase: install

3P: 73.2K
2P: 41.2K

3P: 22p
2P: 10p

3P: 330p
2P: 1000p

3P: 21K
2P: 12.4K

3P: 6.04K
2P: 4.32K

3P: 1500p
2P: 1200p

3P: 2200p
2P: 3300p

3P: 348
2P: 1.21K

3P: 3.65K
2P: 9.53K

3P: 23.7K
2P: 24.9K

3P: 806
2P: 1K

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2012/07/11

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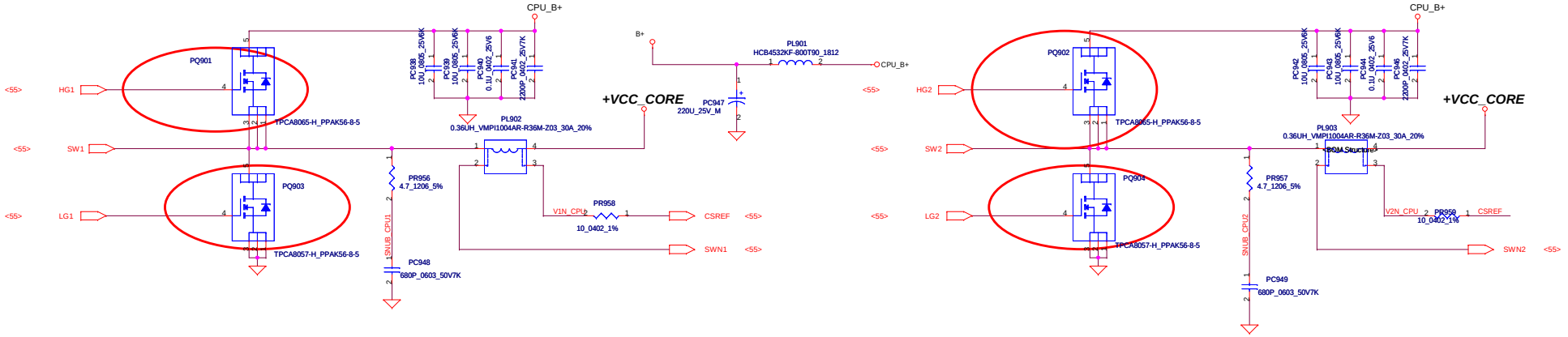
Compal Electronics, Inc.

Title: PWR-CPU_CORE

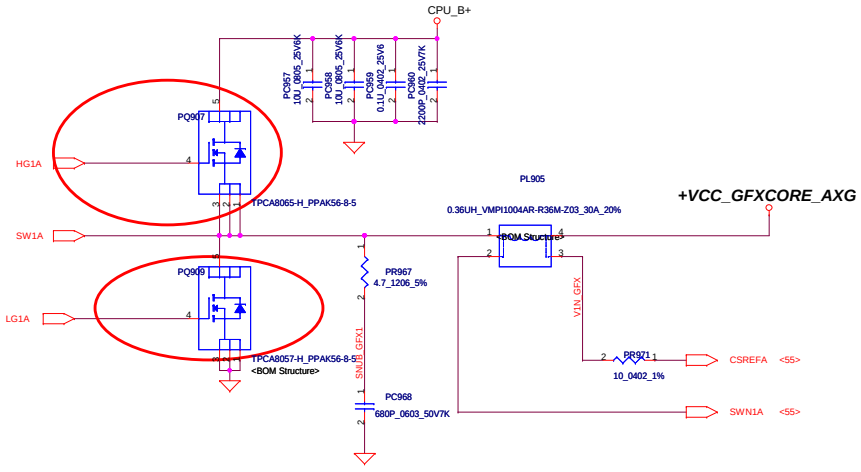
Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Tuesday, February 14, 2012 | Sheet 55 of 60



QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

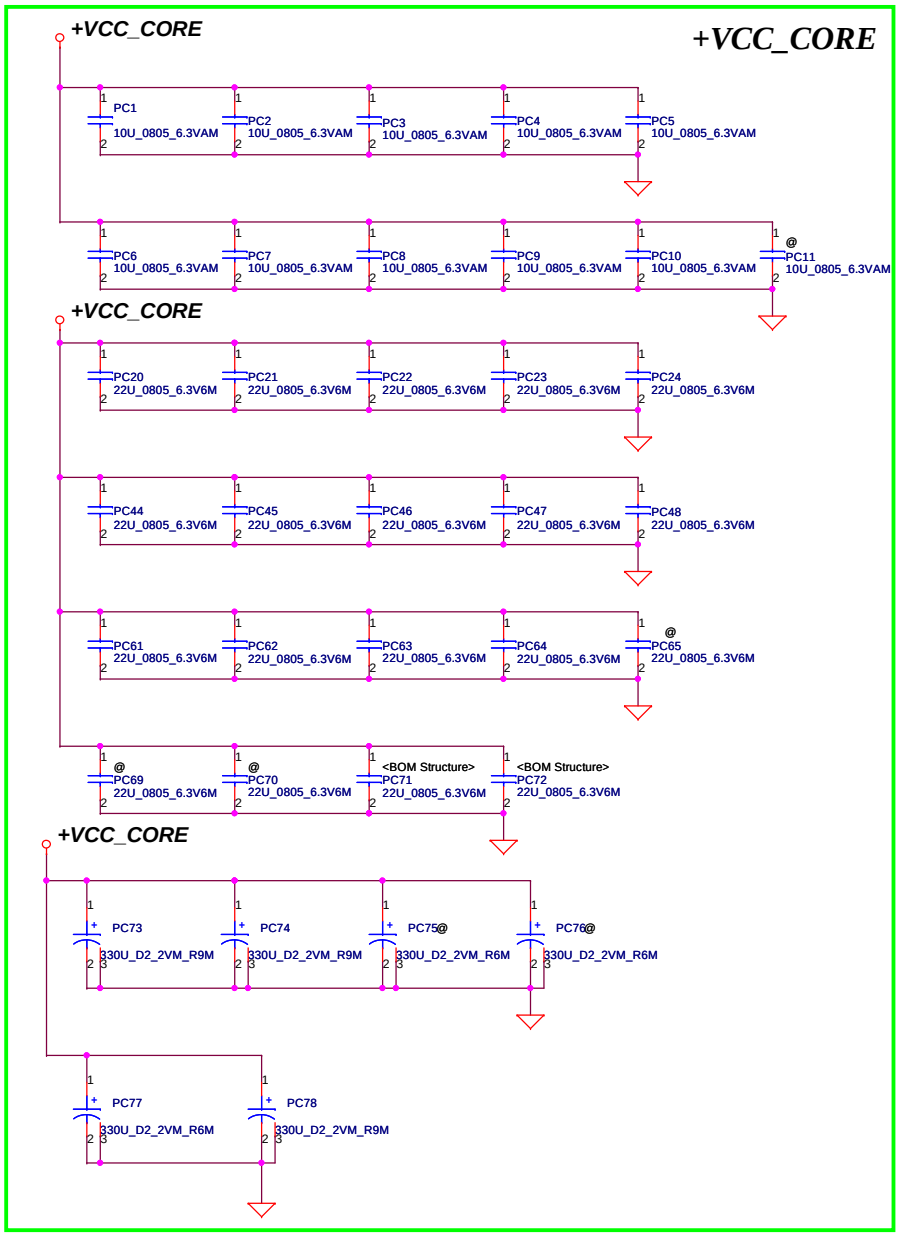
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2012/07/11

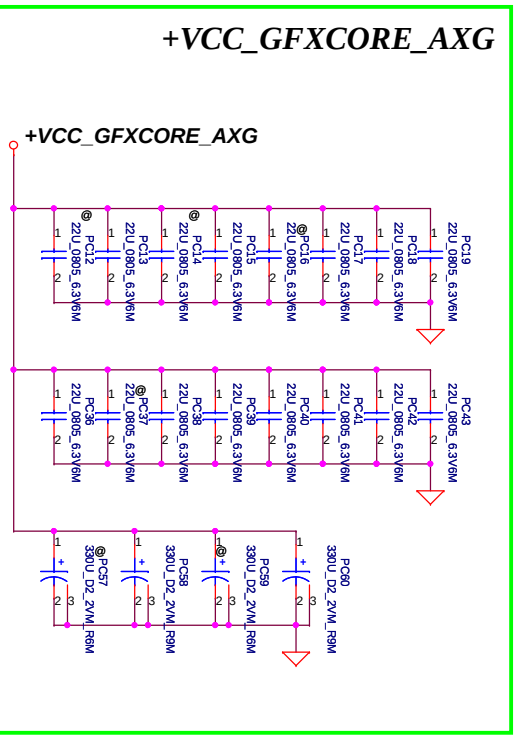
Compal Electronics, Inc.

Title: **PWR-CPU_CORE**

Size	Document Number	Rev
C	C38-G series Chief River Schematic	0.1

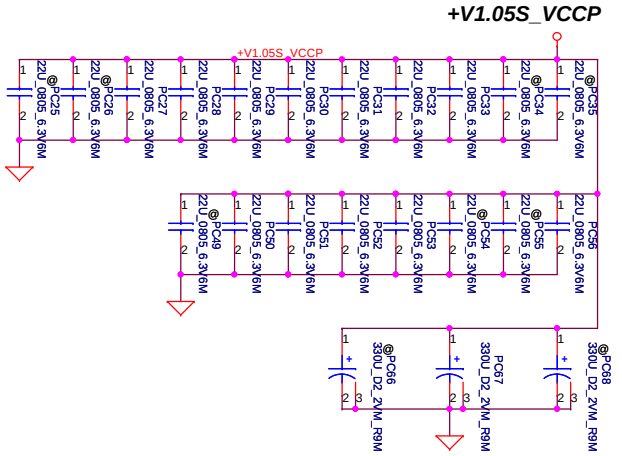
Date: Tuesday, February 14, 2012 | Sheet 56 of 60





Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	C38-G series Chief River Schematic	0.1

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	add PR865 for ISL62883 one phase solution and unpop for two phase solution.	P54	add PR865	2011.08.29	DVT
2	unpop PR315,PR316 for SMBus SPEC.	P49	unpop PR315,PR316	2011.08.29	DVT
3	delet PSI#_VGA for NV chip.	P54		2011.10.14	DVT2
4	change NTC_V pull high voltage from +3VLP to +3VALW	P48			
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

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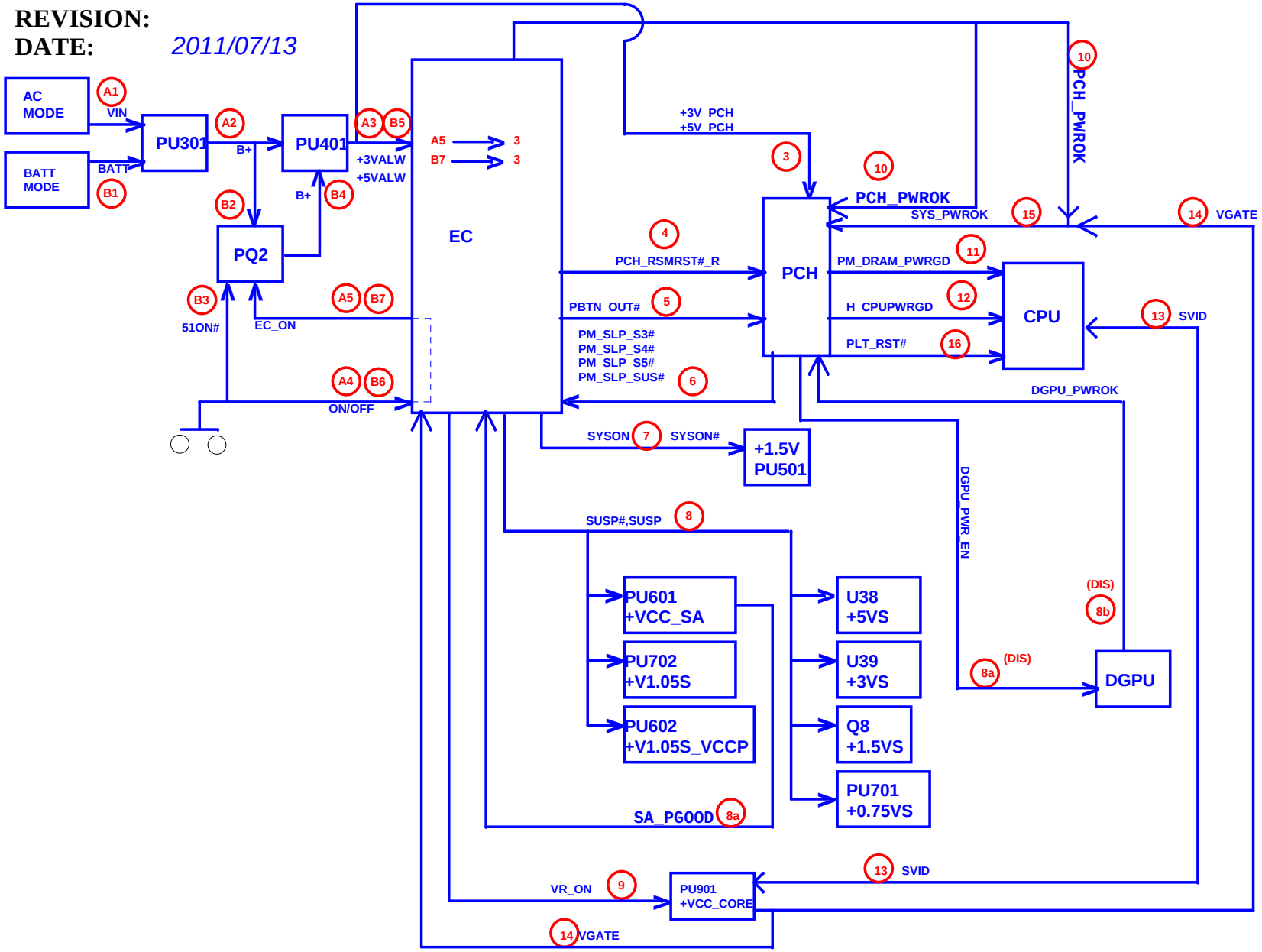
COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-7981P*
REVISION:
DATE: *2011/07/13*



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Title: ***Power sequence***

Size	Document Number	Rev
Custom	*LA-7981P*	0.2

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	GPU 13M GPU Device loss (Pcie lan x8 issue)	8	Add R43		DVT
2	HDD no function	40	Add R550		DVT
3	10/100 lan no function & change to overclocking mode	37	ADD R1372 ; DEL R31		DVT
4	For DGPU_PWROK leakage issue.(Let timing +5VS > +3VS)	46	Change C726 from 0.1uF to 0.01uF		DVT
5	For S3 can't wake up	10	Change R56 from 15K to 4.7K change R885 from 0 ohm to 15K		DVT
6	Can unstuff RV66 for N13P-GL & as NV DG	27	RV66 change to N13M@		DVT
7	GPU N13P-GL QS sample change strap	32	RV94 change from 45.3K to 10K		DVT
8	PCH 25Mhz for vender crystal test report change CL to 12pF	15	C196;C197		DVT
9	GPU 27Mhz for vender crystal test report change CL to 15pF	23	CV37;CV38		DVT
10	EC_LID_OUT# internal PD 20K, follow ORB change R230 from 10k to 1K	19	R230		DVT
11	For GPIO70;GPIO71 voltage level issue (internal Pull High 20k)	19	R705;R706 Change from 10K to 200K		DVT
12	for DVT board ID Change R695 from 33k to 18k	42	R695		DVT
13	LAN Surge test fail change P/N from SP050006E00 to SP050006W00	27	T1;T2		DVT
14	Del ODD Power Control function component	40	R568;Q100;R675;C607;Q99		DVT
15	AO4430L(SB000007O10)EOL Change to AO4304 (SB00000RV00)	46	U49		DVT
16	Del (PCH AUX Power) Reserve component no use	46	C780;C781;C782;C783;R778;Q120;U40		DVT
17	PCH(U4) P/N Change from SA00004NQ30 to SA00004NQ80	14	U4		DVT
18	NV-GPU (U65)P/N change N13M from SA00004V000 to SA00004V010 N13P Keep SA000051A00	23	U65		DVT
19	EXT USB 3.0 IC PCIE_WAKE# ; CLKREQ_USB30# leakage on S4	45	Swap Q125;Q121 pin1 & pin3		DVT
20	No function	45	DEL R769		DVT
21	add LAN LDO mode function	37;38	ADD R65;R596;R1449;R1380		DVT
22	USB_OC0# Share with USB_OC4# due to same power switch	18	short USB_OC0#;USB_OC4# ; del R267		DVT
23	Add Capsensor B/D Conn. For best buy use	42	ADD JCAP1 Conn.		DVT

Compal Electronics, Inc.

Title: *HW-PIR1*

Size: Custom | Document Number: LA-7981P | Rev: 0.1

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Item	Reason for change	PG#	Modify List	Date	Phase
24	L1 change to 1 ohm R	20	L1 change to R footprint		DVT
25	Reserve 0 ohm for CMOS Camera shake	33	add R296 0 ohm		DVT
26	Reserve 0 ohm for U49 MOS VGS 20V will burn out issue	46	add R784 0 ohm		DVT
27	For HDD +5VS Power plant del C601; change C598 pin1 power name for good power plant	40	change from +5VS to +5V_HDD ;DEL C601		DVT
28	For Audio jack support APPLE and NOKIA function Reserve	43	add R684;R685;R688;R686 0ohm R		DVT DVT
29	For standard part cost down change 10uF 0805 type to 0603 type	10,20 21,33 37,39 40,46	C124;C125;C126;C127;C130;C221;C215;C395; C231;C519;C937;C953;C954;C591;C608;C602; C720;C721;C723;C724;C782;C783;C717;C718; C856;C852;C851;C853		DVT DVT
30	change Crystal foot print follow standard parts from 5032 to 3225 package	15;23; 37	Y2;Y6;YV1		DVT
31	change 0ohm to short-pad (R0402_0ohm)	7;8; 10;15 16;20; 33;36; 40;43	R40;R60;R77;R144;R190;R193;R198;R181;R185; R265;R538;R498;R500;R583;R614		DVT DVT DVT
32	Reserve BT_DISABLE (GPI022) for combo card(BT+WLAN)	19	ADD R892;R897		DVT
33	U35;U36 Change footprint without thermal PAD type	44;45	U35;U36		DVT
34	PU 10K with 3V3 on N13P-GL/ for CEC signal	24	RV230		DVT
35	VGA_GPIO3;VGA_GPIO16 change connect DPRSLPVR_VGA to PSI#_VGA	23;54	RV113;RV114		DVT
36	Fix VGA power on CLKREQ has drop (QV2 gate add 0.1uF)	23	CV42		DVT
37	LED5 和LED2 Location sawp ; Location name D9 change to LED6	43	LED2;LED5;LED6		DVT
38	For Lan surge fail add 0 ohm on MDO2-;MDO2+;MDO3-;MDO3+	38	R304;R305;R306;R307		DVT
39	Change UV2 PN from SA007080B90 to SA00000OH00	23	UV2	09/28	DVT
40	Change 2M BIOS ROM from SA00003FO00 to SA00003FO10	14	U6	09/29	DVT
41	Correct PCIE_PRX_DTX_P4/N4 of U32 (SWAP)	45	U32	10/03	DVT
42	Reserve +5VS to JCR1, add R689 ,R690	43	R689 (@),R690	10/03	DVT
43	Update Power sheet of 1003 version	47~58		10/04	

Item	Reason for change	PG#	Modify List	Date	Phase
44	CPU Symbol Update	5,6,7, 8,9,10,11	Location : Jcpu1		PVT
45	Change 10P 50V Cap from 1206 to 0603	38	Location : C973		PVT
46	S3 Reduction	53	Reserve PR719 for 0.75V		PVT
47	LAN CO-lay x1 GDT & 75ohm	38	Location : R308,R304,R305,R306,R307,DL1,DL2,DL3,DL4		PVT
48	R750 for Power request	42	Location :R750		PVT
49	JUSB3 From 4PIN TO 6 PIN FOR VOLTAGE DROP	44	Location : JUSB3		PVT
50	Add C535 100pF on +3VLP for ESD request - Pony	42	Location : C535		PVT
51	FOR TP POWER SOLUTION	42	Location : R598.R603		PVT2
52	FOR POWER REQUEST	42	Location : R738		PVT2
52	Change C from 0.22Uf to 0.11uF	5 23	Location : C1,C2,C3,C4,C5,C6,C7,C8,C9,C10, C11,C12,C13,C14,C15,C16,C17,C18,C19,C20, C21,C22,C23,C24,C25,C26,C27,C28,C29,C30, C31,C32, CV6,CV7,CV8,CV9,CV10,CV11,CV12,CV13,CV15, CV17,CV19,CV14,CV16,CV18,CV20,CV22,CV24, CV26,CV21,CV23,CV25,CV27,CV29,CV31,CV33, CV28,CV30,CV32,CV36,CV41,CV34,CV35,		SVT