

Compal Confidential

Model Name : Z5WAH

File Name : LA-B162P

# Compal Confidential

## EA50\_HB M/B Schematics Document

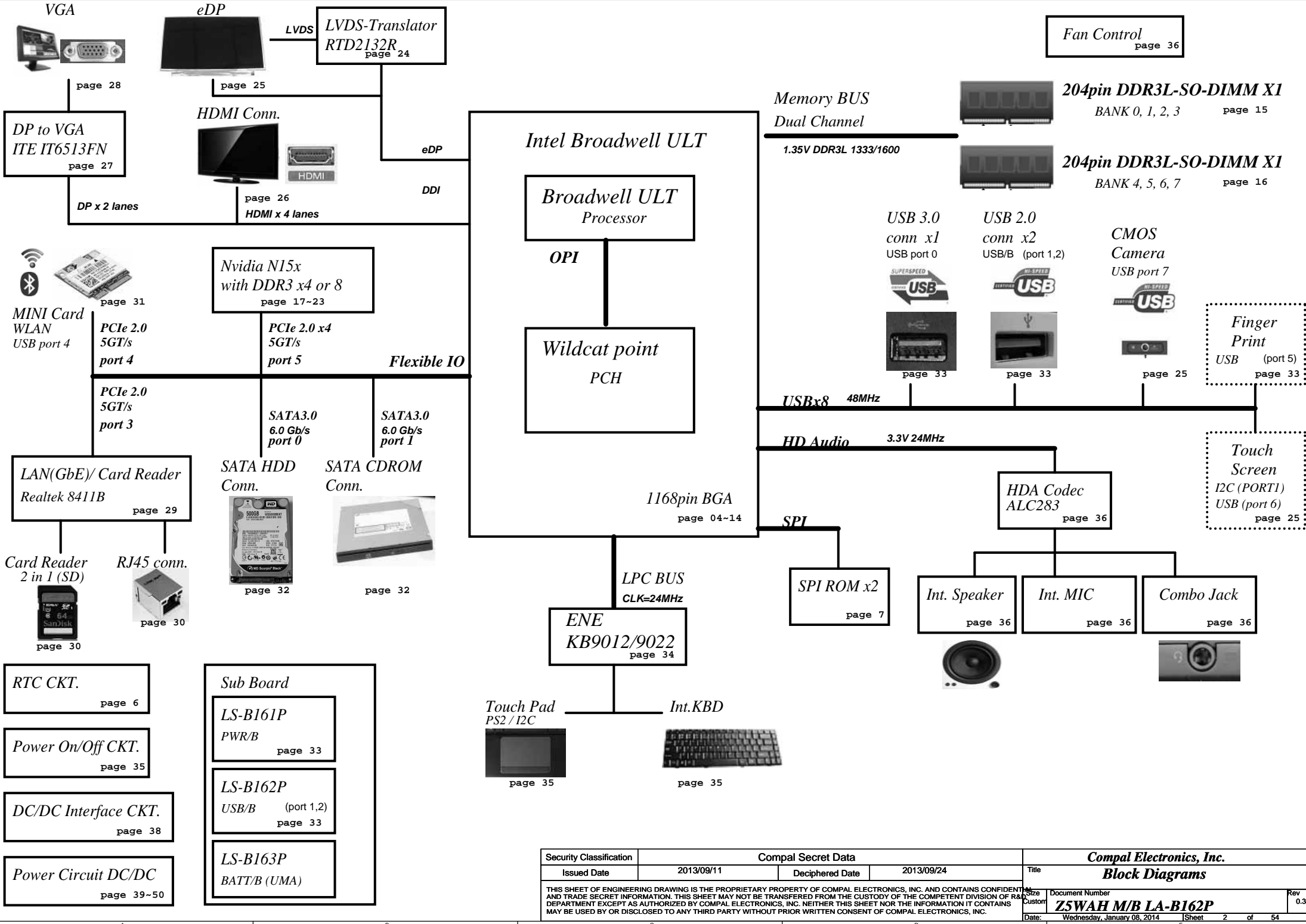
Intel Broadwell ULT (Broadwell + Wildcat point)

Nvidia N15S-GT / N15V-GM / N15V-GL

2013-12-24

REV: 0.2

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/09/11	Deciphered Date	2013/09/24	Title	Cover Page
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				Block Diagrams	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.675VS	+0.675VS power rail for DDR3L terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05V power rail for CPU	ON	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+1.5VSDGPU	+1.5VSDGPU power rail for GPU	ON	OFF	OFF
+1.5VS	+1.5V power rail for CPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X	On Board Thermal Sensor	0100 110x
		VGA Internal Thermal Sensor	0100 000x
		G Sensor	0011 000x

EC SM Bus2 address

PCH SM Bus address

Device	Address	
ChannelA DIMM0	1010 0000	JDIMM1
ChannelB DIMM1	1010 0010	JDIMM2

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	12K +/- 5%	0.347 V	0.354 V	0.360 V
2	15K +/- 5%	0.423 V	0.430 V	0.438 V
3	20K +/- 5%	0.541 V	0.550 V	0.559 V
4	27K +/- 5%	0.691 V	0.702 V	0.713 V
5	33K +/- 5%	0.807 V	0.819 V	0.831 V
6	43K +/- 5%	0.978 V	0.992 V	1.006 V
7	56K +/- 5%	1.169 V	1.185 V	1.200 V
8	75K +/- 5%	1.398 V	1.414 V	1.430 V
9	100K +/- 5%	1.634 V	1.650 V	1.667 V
10	130K +/- 5%	1.849 V	1.865 V	1.881 V
11	160K +/- 5%	2.015 V	2.031 V	2.046 V
12	200K +/- 5%	2.185 V	2.200 V	2.215 V
13	240K +/- 5%	2.316 V	2.329 V	2.343 V

USB Port Table

USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port(Left 3.0)
	1	USB Port(Right 2.0)
	2	USB Port(Right 2.0)
	3	
	4	Mini Card (WLAN+BT)
	5	Touch Screen
	6	Camera
	7	Finger Print
USB 3.0	Port	
XHCI	0	USB Port(Left 3.0)
	1	
	2	
	3	

BOARD ID Table

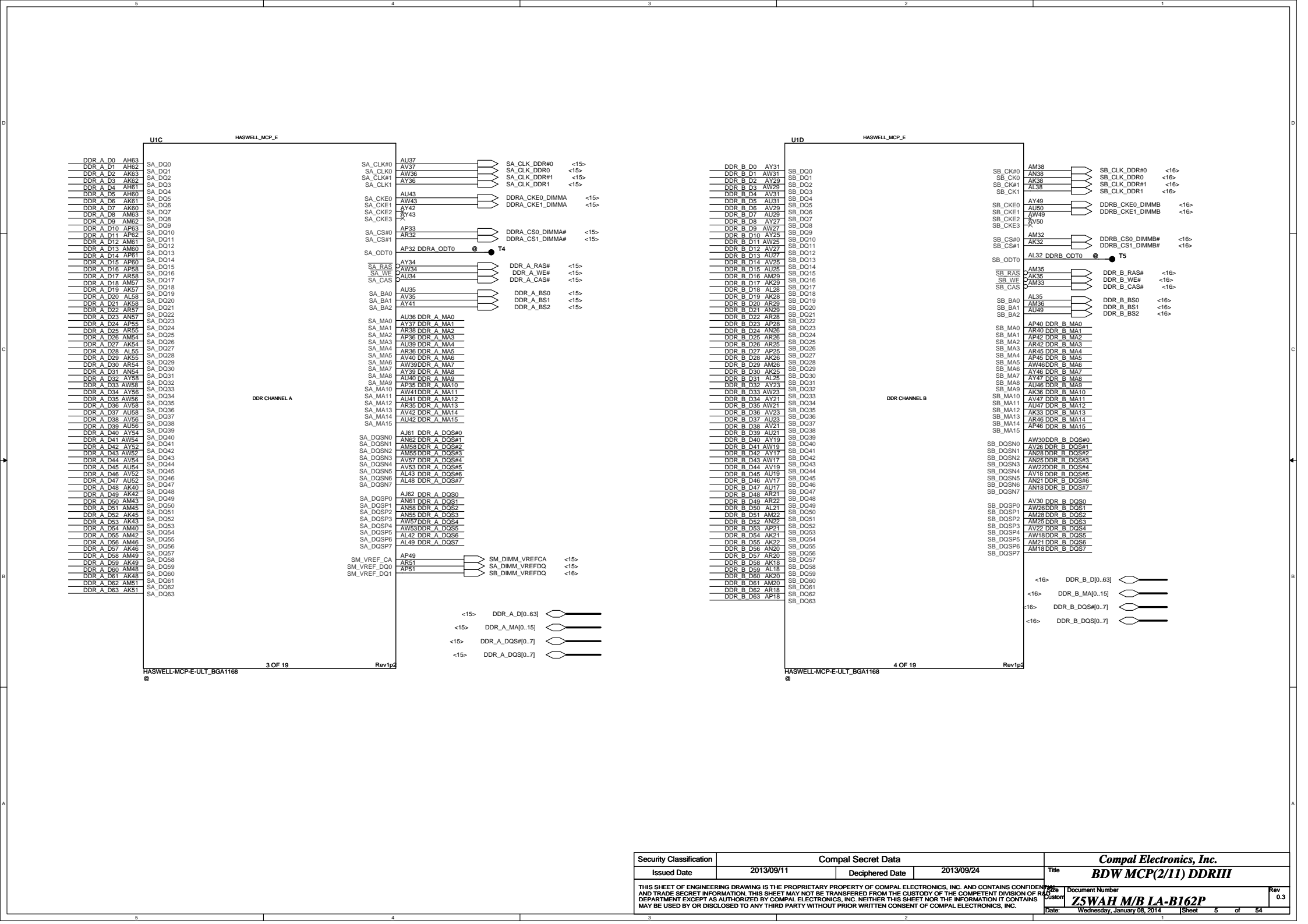
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2	0.3
3	0.4
4	0.5
5	1.0
6	
7	

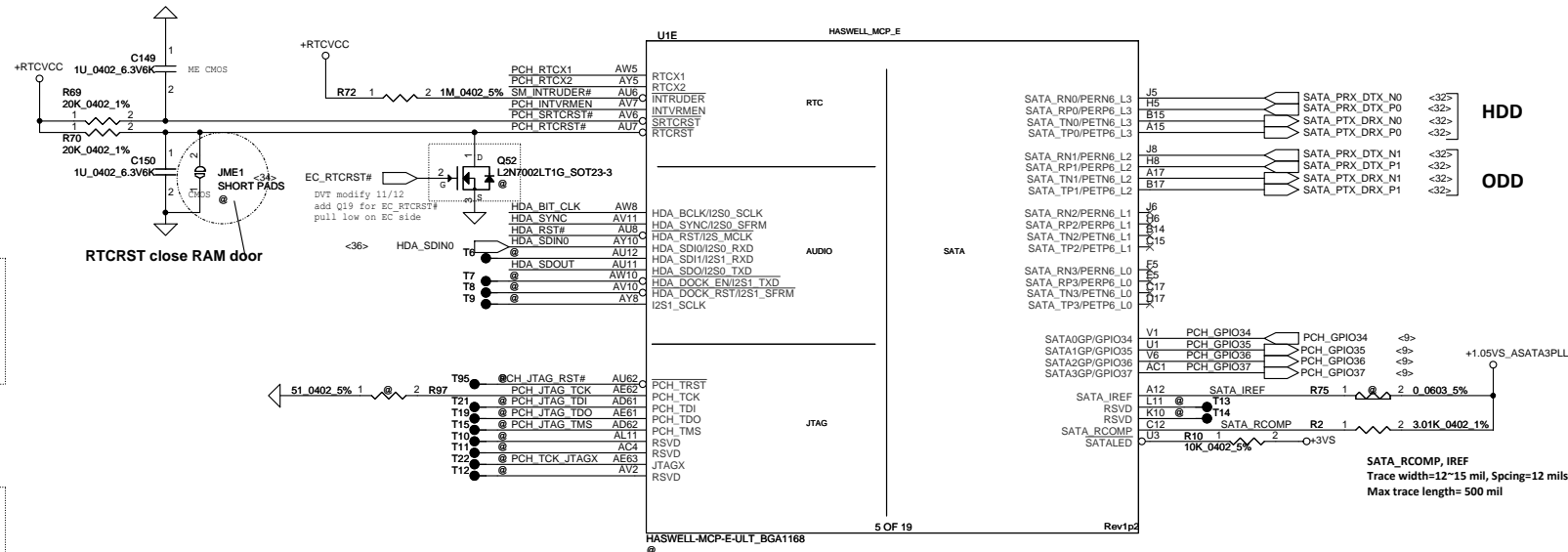
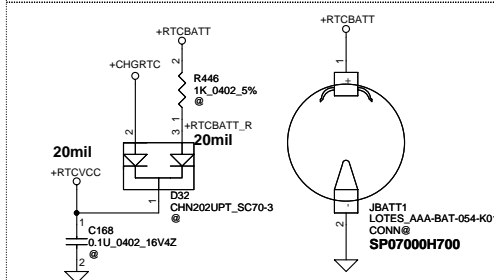
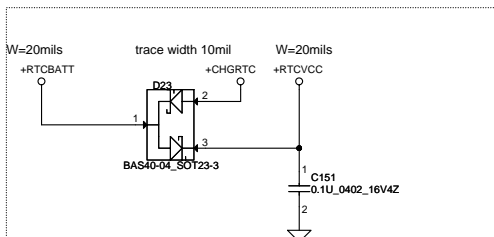
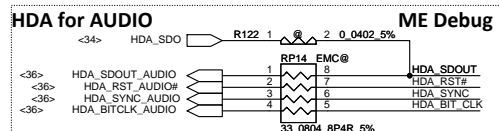
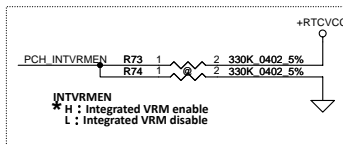
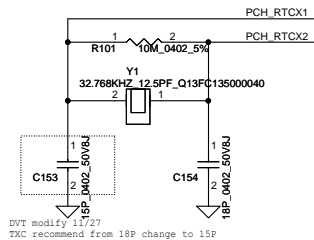
BTO Option Table

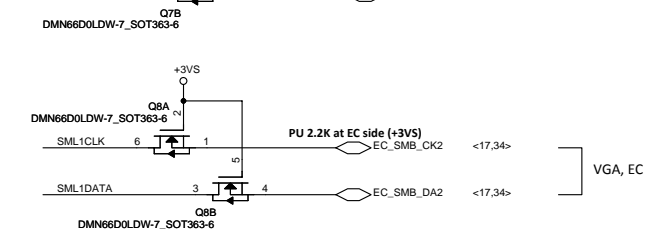
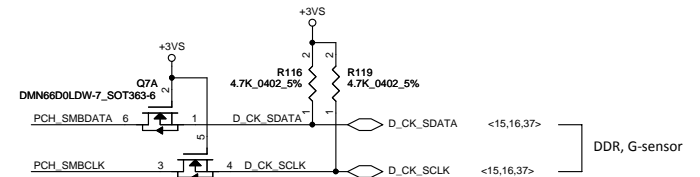
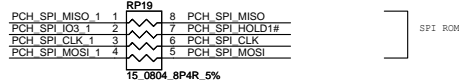
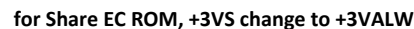
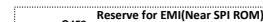
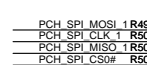
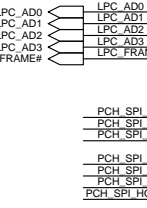
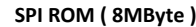
BTO Item	BOM Structure
Unpop	@
Connector	CONN@
EC 9022	9022@
EC 9012	9012@
UMA Component	UMA@
GPU	VGA@
VRAM x 8pcs	128@
EDP panel	EDP@
eDP to LVDS	LVDS@
EMC Component	EMC@
EMC Reserve	XEMC@
On Board HDD	HDD@
G-Sensor	BA@
TPM Module	BA@
Redriver HDD	BA@
Touch Screen	TS@
DGPU_IDEN	VGL@, VGME@, SGT@
CPU_IDEN	HW@, BW@
GC6 2.0	GC6@
non GC6	NGC6@
One DMIC	EA50@
Two DMIC	EA54@
VRAM Selection	X76@

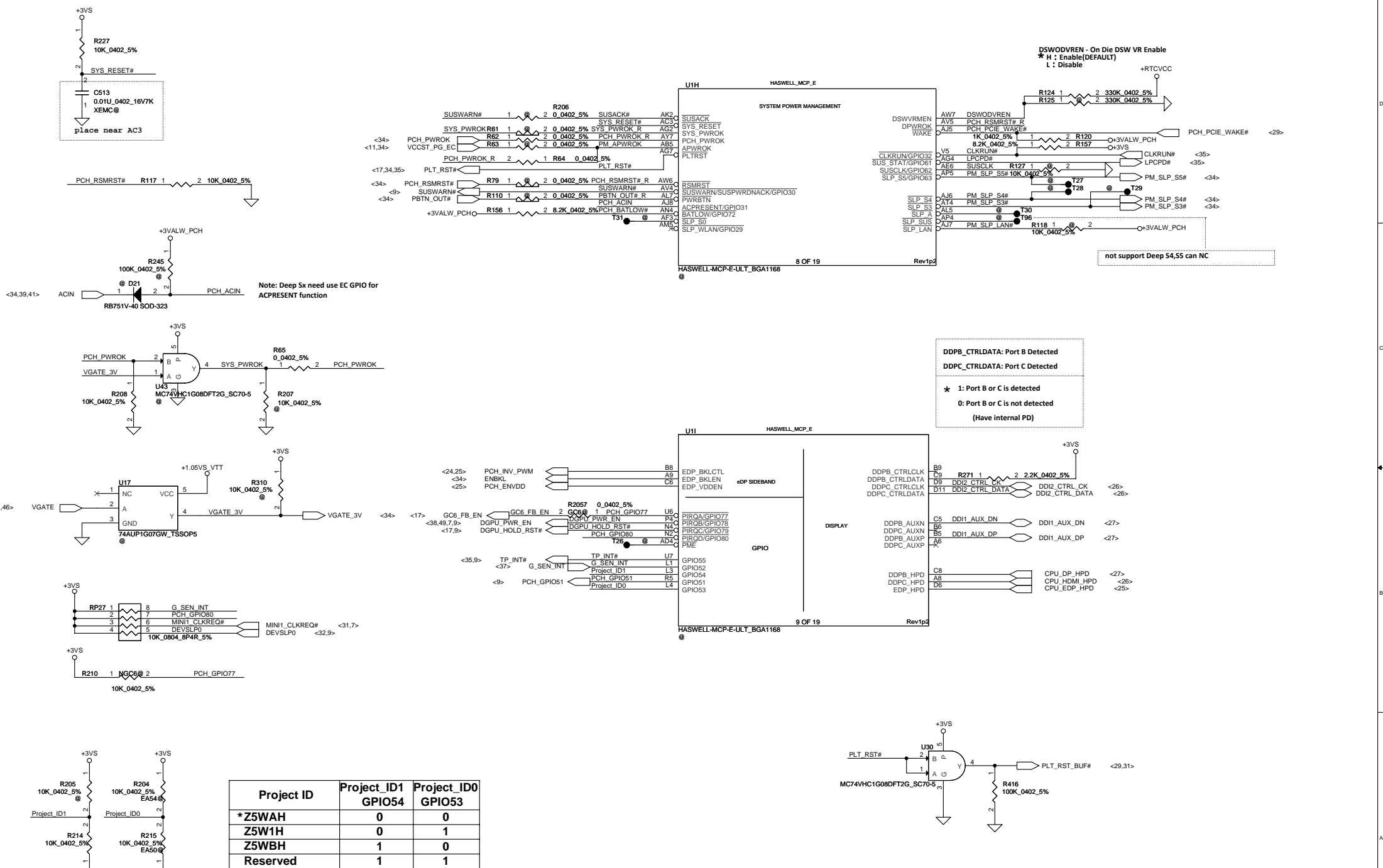
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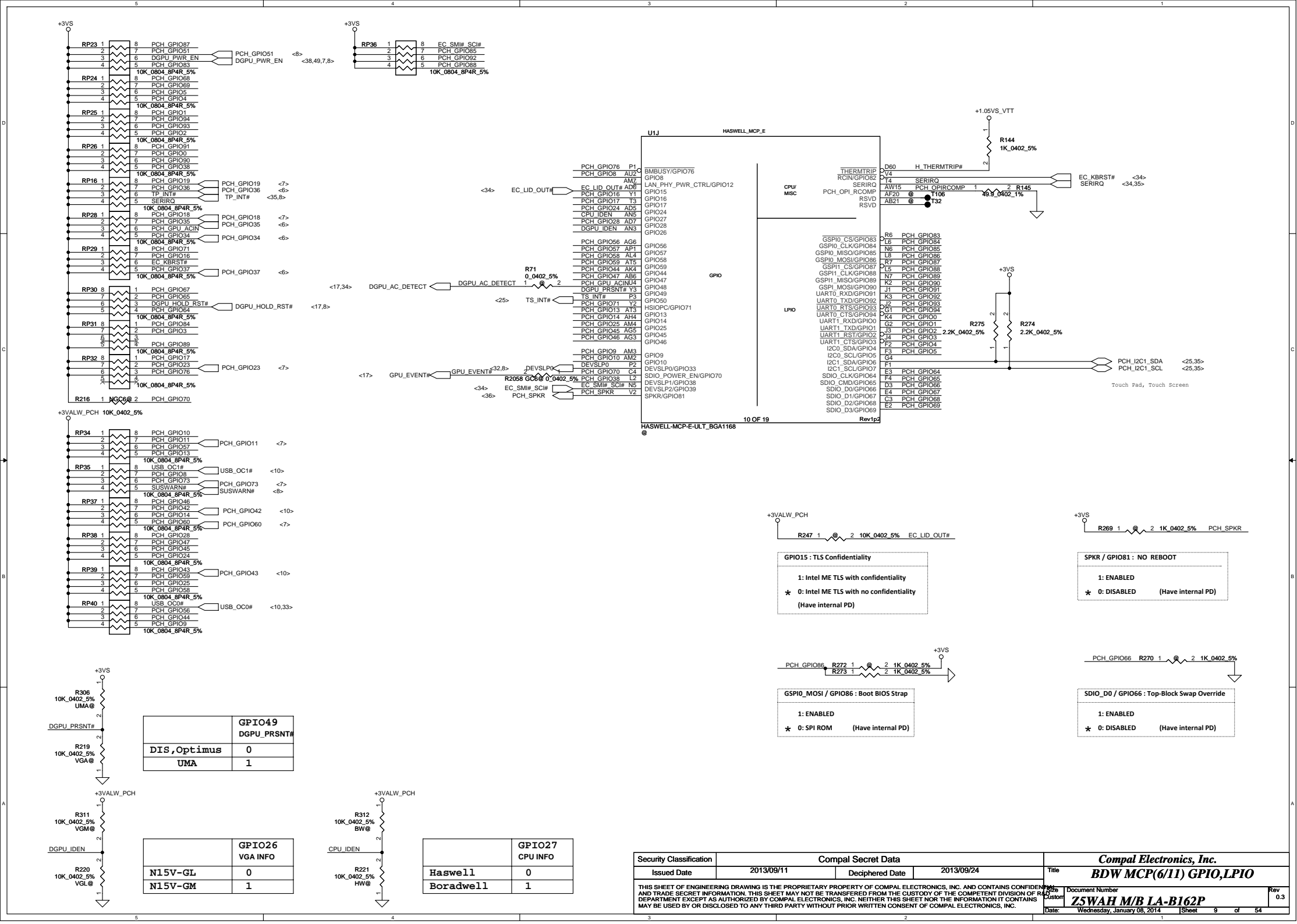


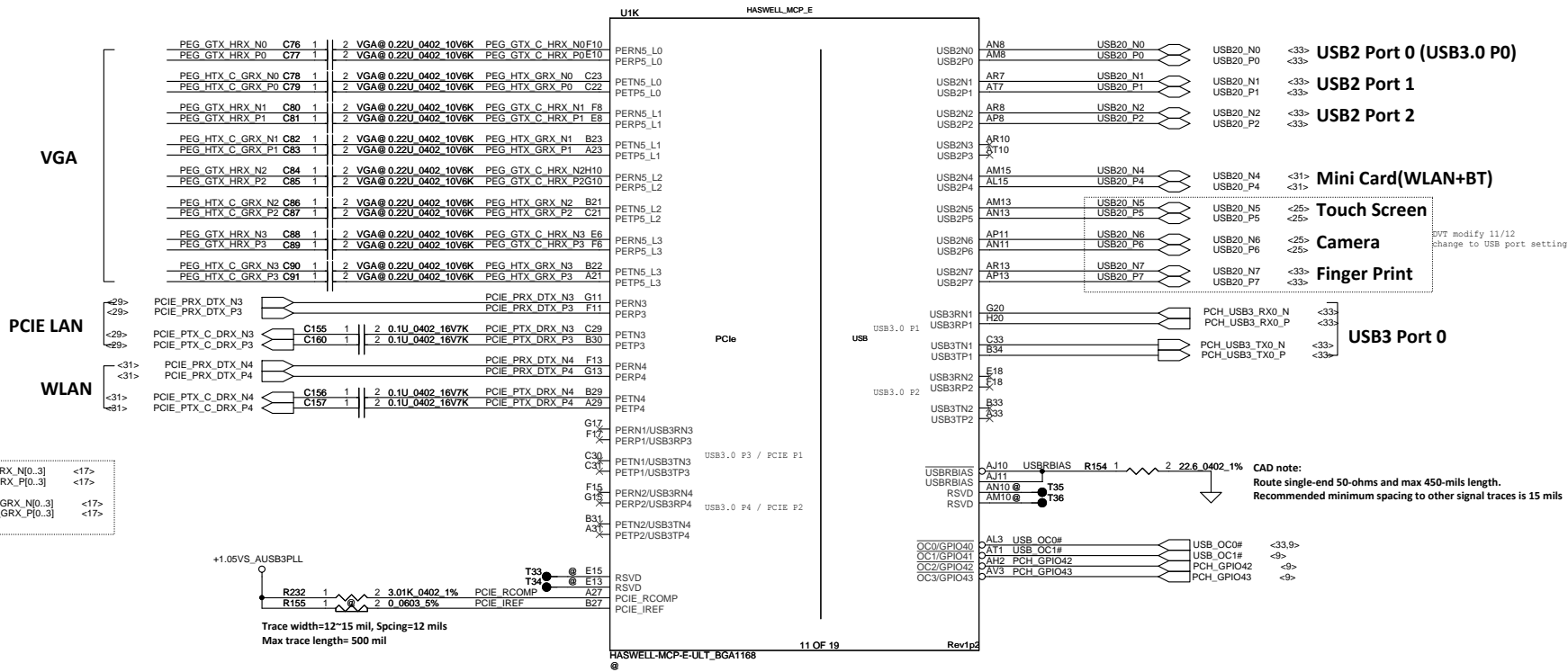
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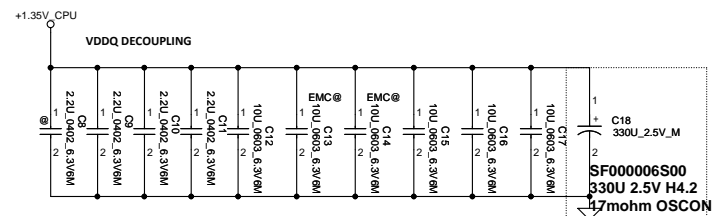
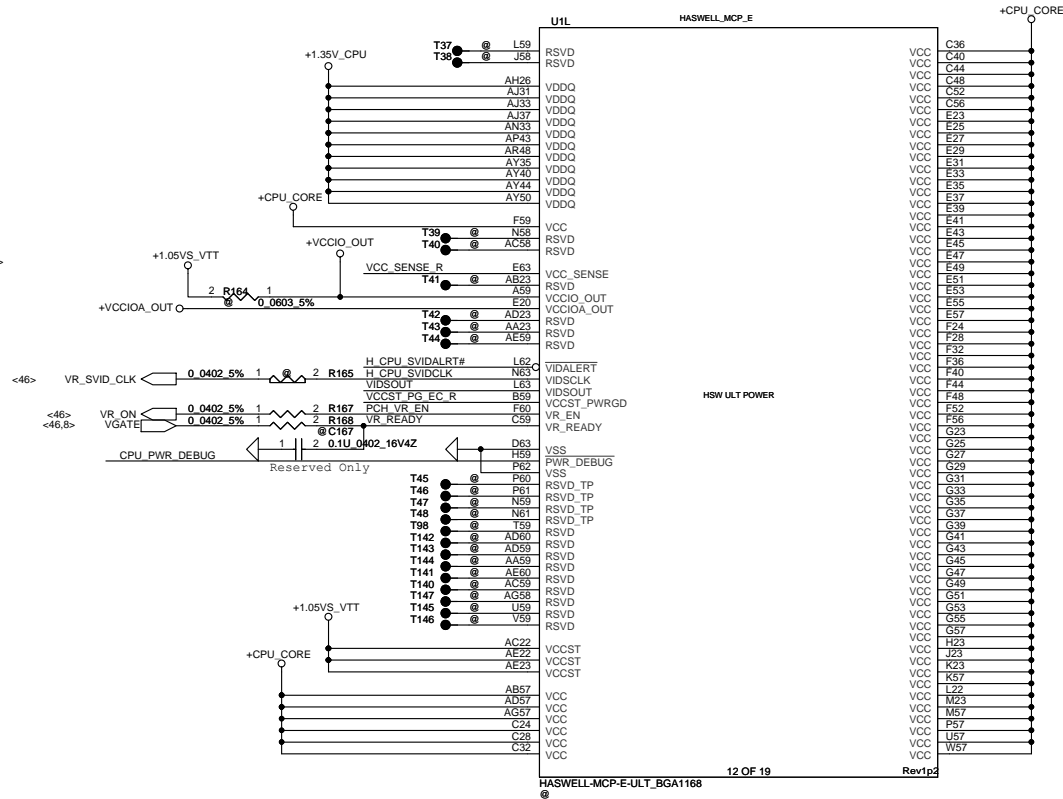
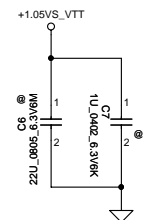
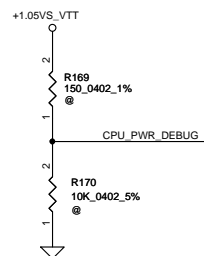
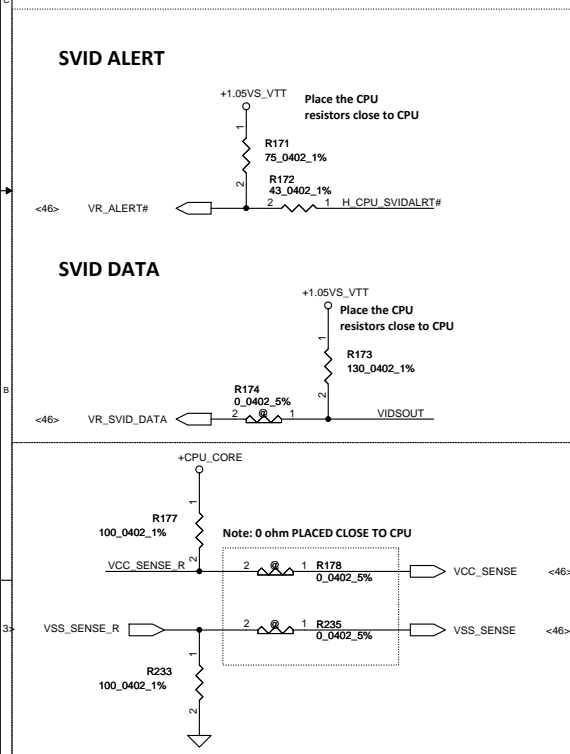


Project ID	Project ID1 GPIO54	Project_ID0 GPIO53
*Z5WAH	0	0
Z5W1H	0	1
Z5WBH	1	0
Reserved	1	1



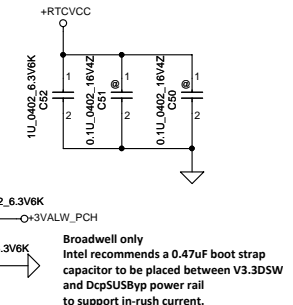
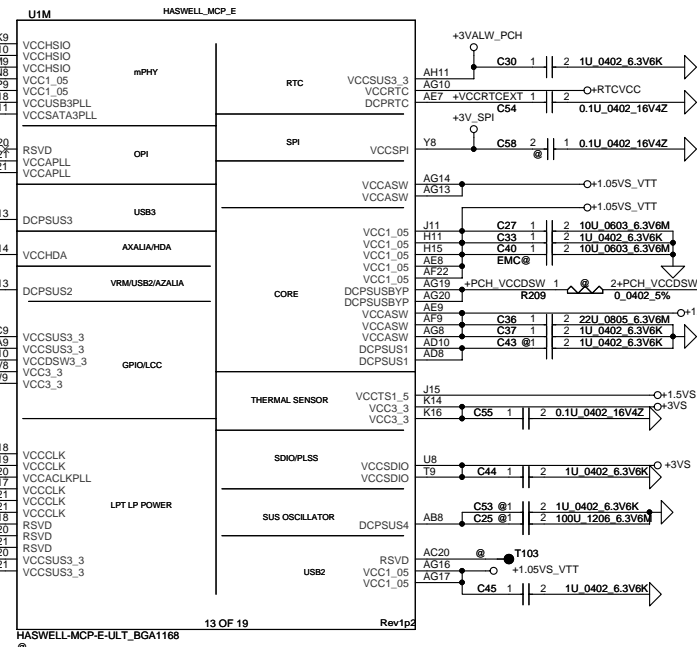
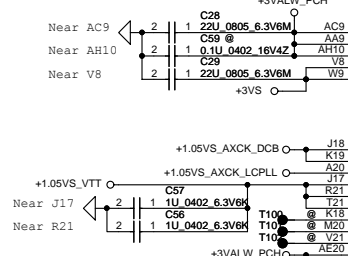
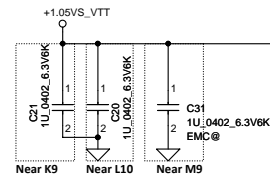






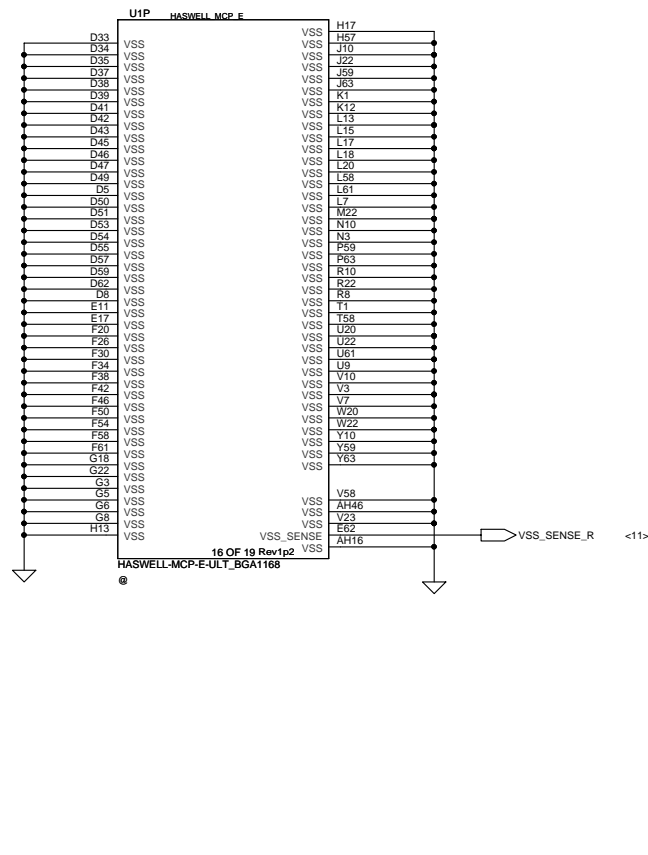
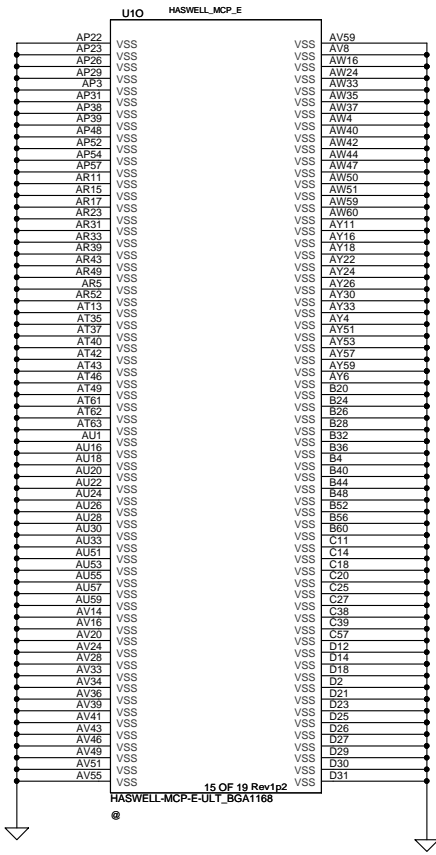
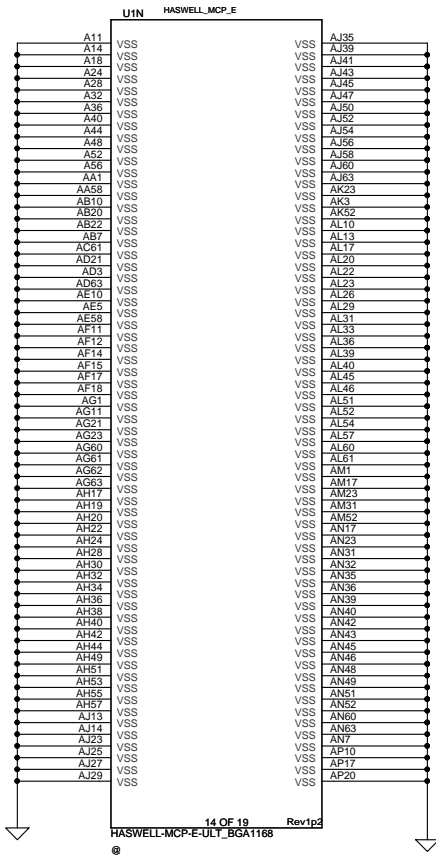
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+1.35V : 470UF/2V/7343 *2
          10UF/6.3V/0603 * 6
          2.2UF/6.3V/0402 * 4
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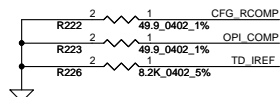
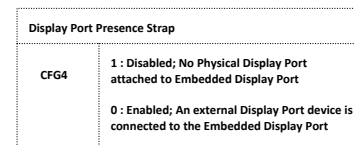
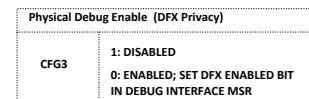
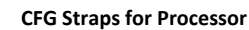
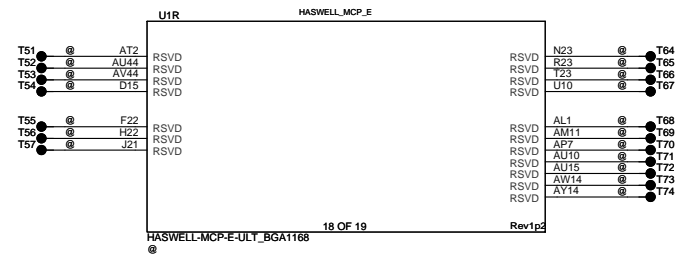
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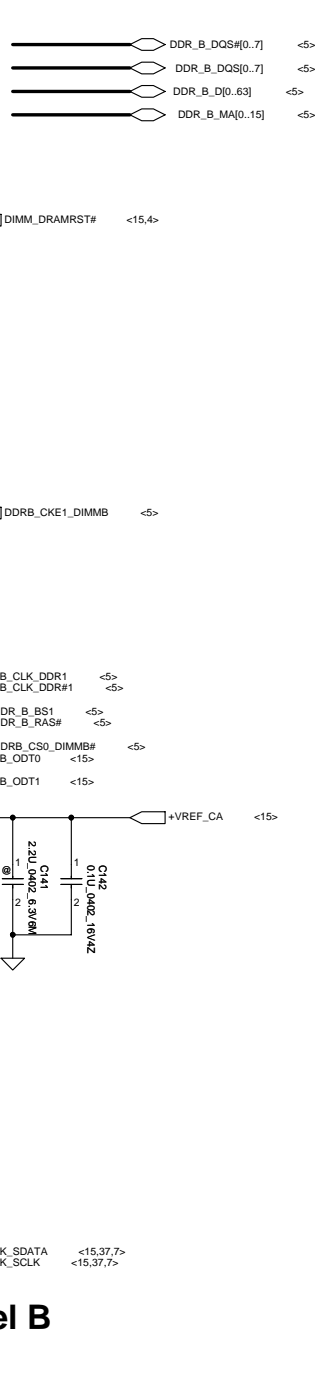
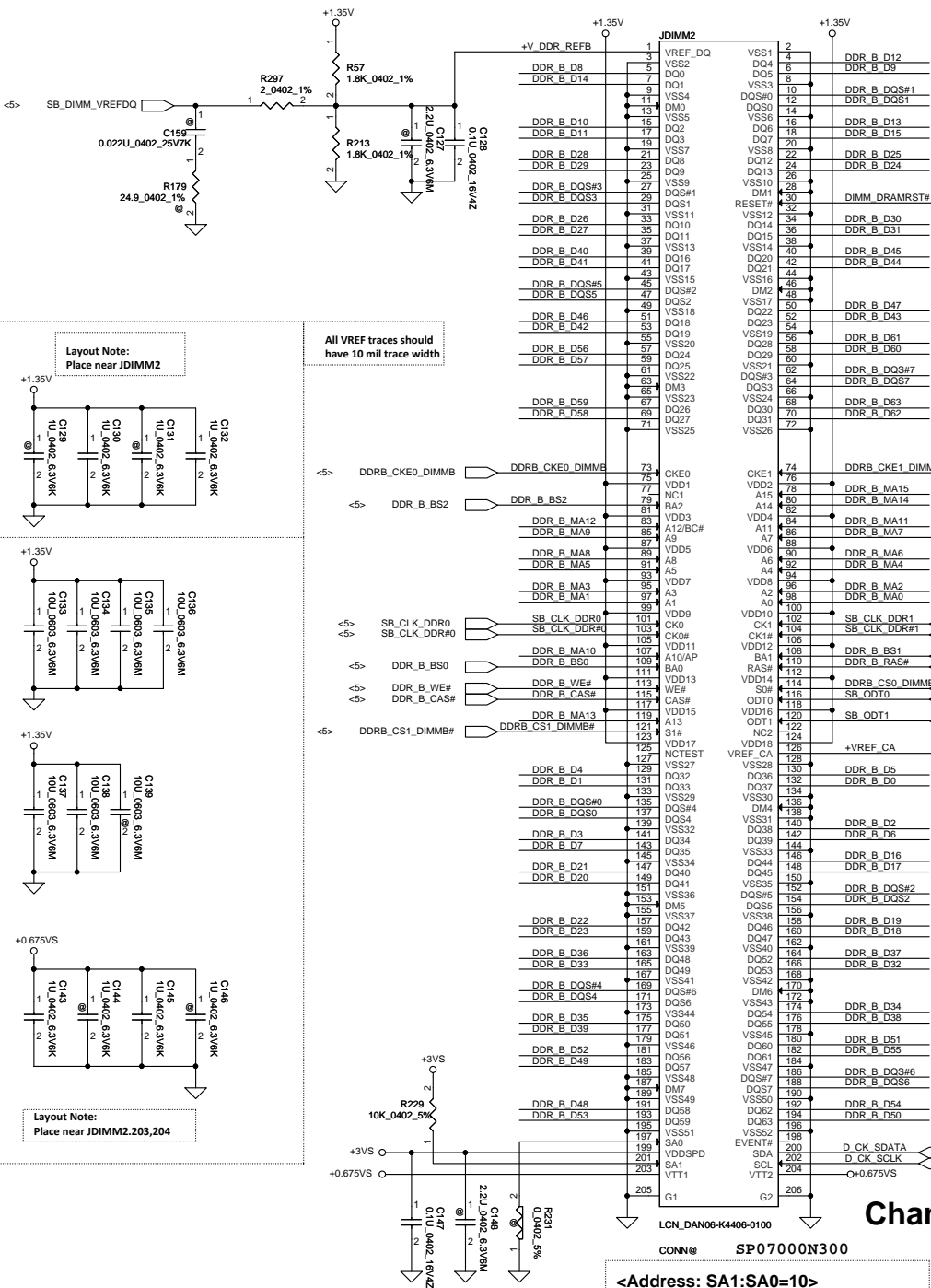
+3VALW J8 @ +3VALW\_PCH  
 JUMP 43X39  
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				Date:	Wednesday, January 08 2014	Issue 12 of 54









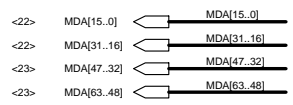
Channel B

<Address: SA1:SA0=10>  
**DIMM\_2 H:4mm**  
**DIS for Standard type**  
**UMA for Reverse type**



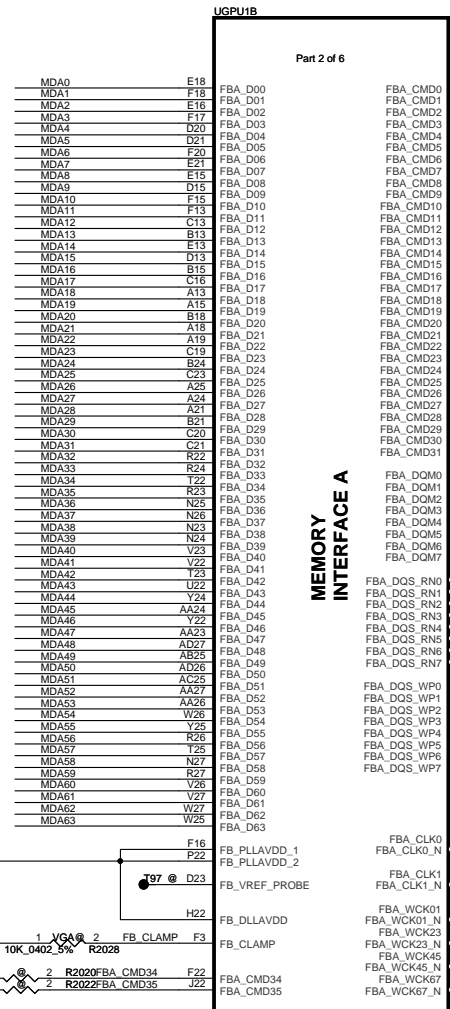
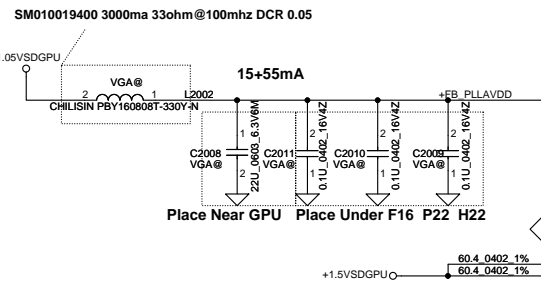


VRAM Interface

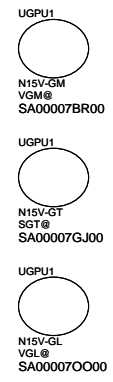


NV 15x DG-06803-V03

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2
		22 µF	X5R	0805	1
		Bead Type			
		30 Ω (ESR=0.010 Ω)		0603	1
					Near GPU



MEMORY INTERFACE A

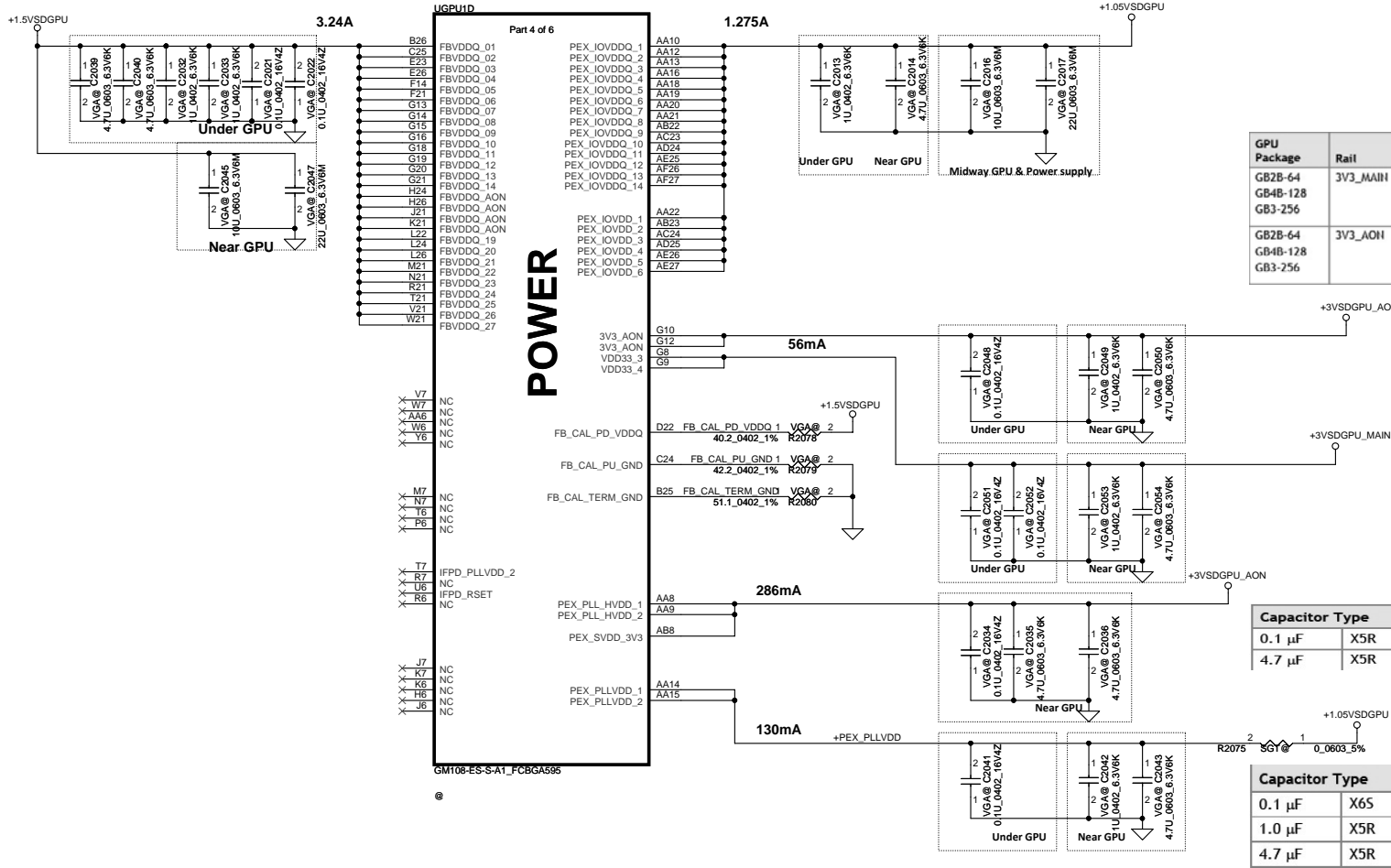




NV 15x DG-06803-V03

GPU Package Type	Capacitor Type	Footprint	Population	Location		
GB2B-64 DDR3	0.1 µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

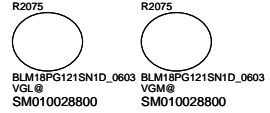
GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 μF	X6S	0402	1	Under GPU
	4.7 μF	X6S	0603	1	Near GPU
	10 μF	X5R	0805	1	Midway between GPU and Power Supply
	22 μF	X5R	0805	1	Midway between GPU and Power Supply



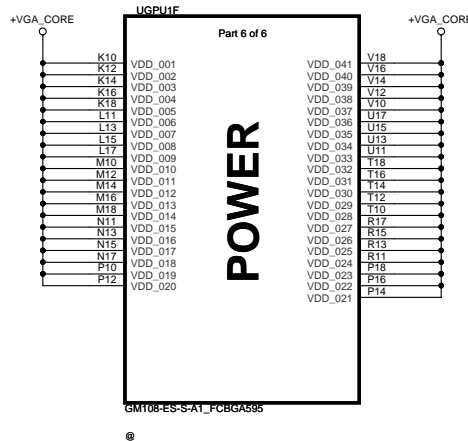
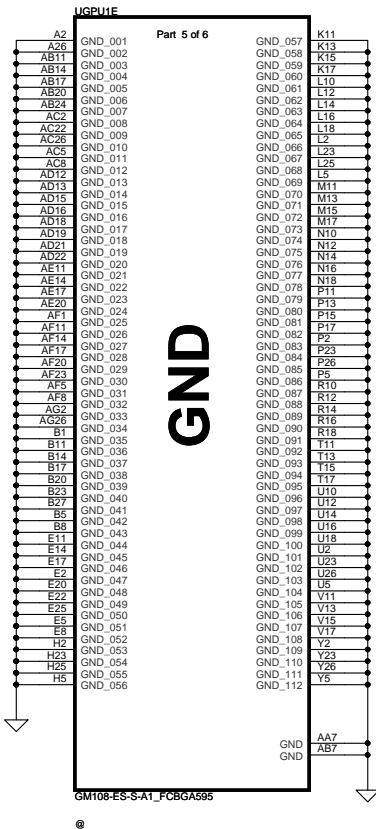
GPU Package	Rail	Capacitor Type		Footprint	Population		Location
GB2B-64	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
GB4B-128		1 µF	X5R	0603	1	1	Hear GPU
GB3-256		4.7 µF	X5R	0603	1	1	Hear GPU
GB2B-64	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
GB4B-128		1 µF	X5R	0603	1	1	Hear GPU
GB3-256		4.7 µF	X5R	0603	1	1	Hear GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X5R	0402	1	Near GPU
4.7 μF	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 µF	X6S	0402	1	Under GPU
1.0 µF	X5R	0603	1	Near GPU
4.7 µF	X5R	0805	1	Near GPU



SM010028800 2000ma 120ohm @100mhz DCR 0.1



## NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint	Population	Location	Comments
GB2B-64	4.7 $\mu$ F	X65	0603	10	10	Under GPU
	1 $\mu$ F	X65	0402	4	4	Under GPU
	47 $\mu$ F	X5R	0805	1	1	Near GPU
	22 $\mu$ F	X5R	0805	1	1	Near GPU
	4.7 $\mu$ F	X5R	0805	5	5	Near GPU
	330 $\mu$ F	POS	7343	1	1	Near GPU ESR $\leq$ 6 m $\Omega$

## DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core	FB Total	1.05V Total
		—	1.5/1.35V	1.05V
N155-GM	DDR3/L	48.11	4.23	0.91
N155-GT	DDR3/L	60.07	4.26	0.91

## DA-06925-V05

Table 6. EDP-Peak at  $T_j = 102^\circ\text{C}$

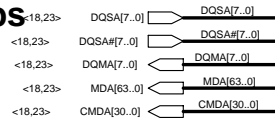
Power Supply Rail (V)	N15V-GM-S DDR3/L
	(A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

## DA07075-V01

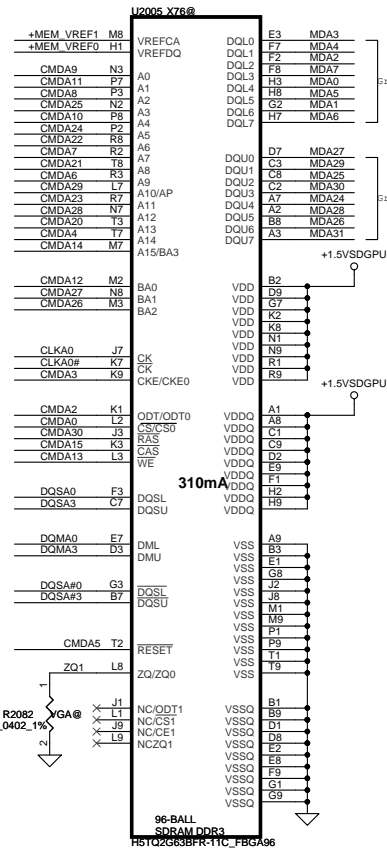
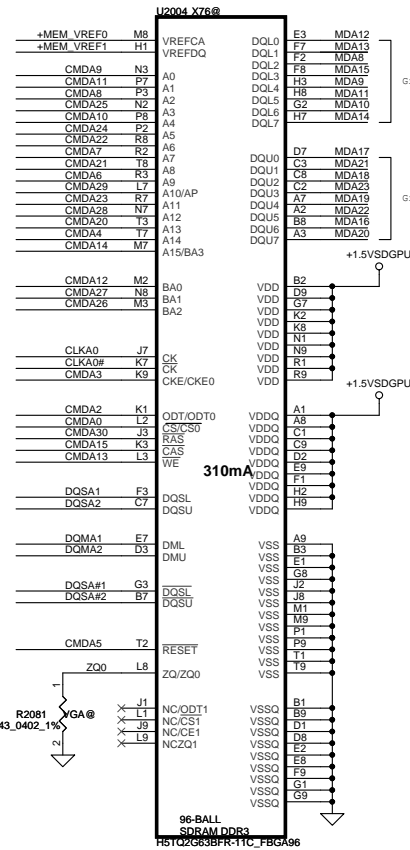
Table 7. EDP-Peak at  $T_j = 102^\circ\text{C}$

Power Supply Rail (V)	N15V-GL DDR3
	(A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

## VRAM DDR3 chips



**Low 32**



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

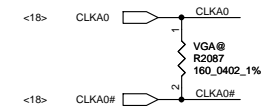
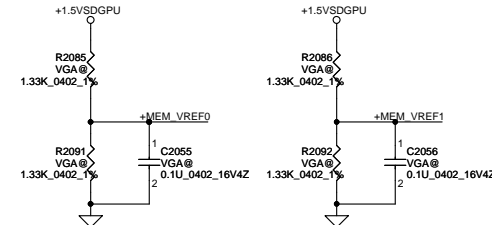
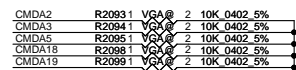
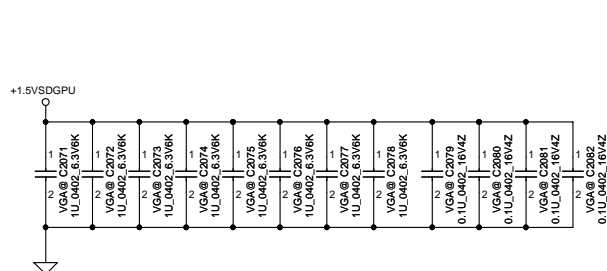
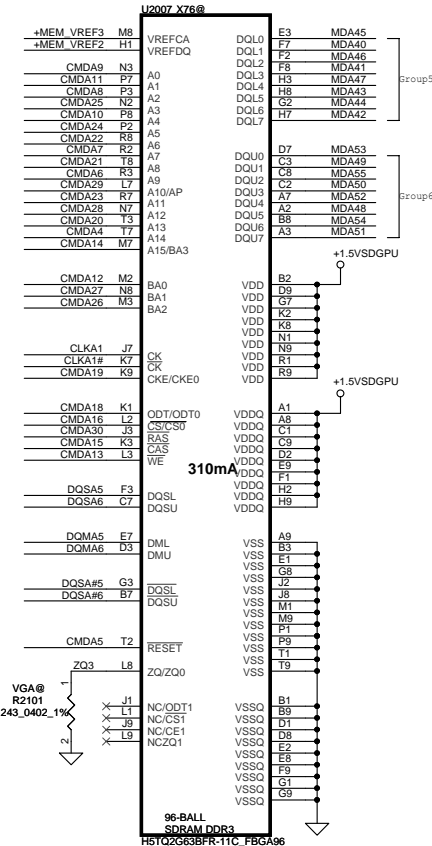
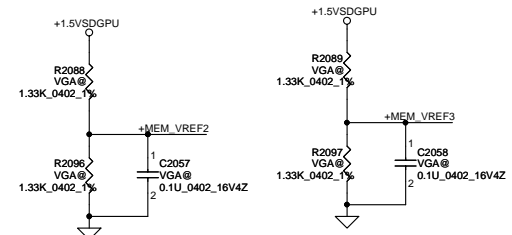
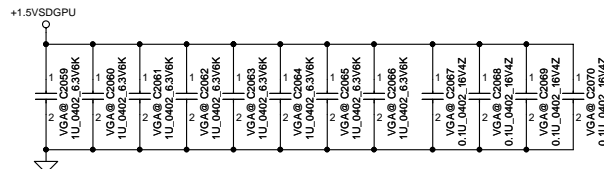
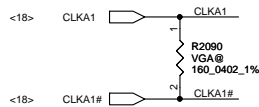


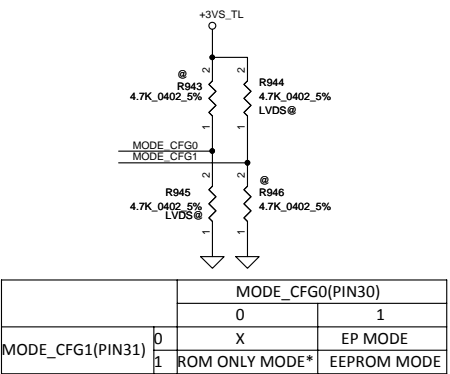
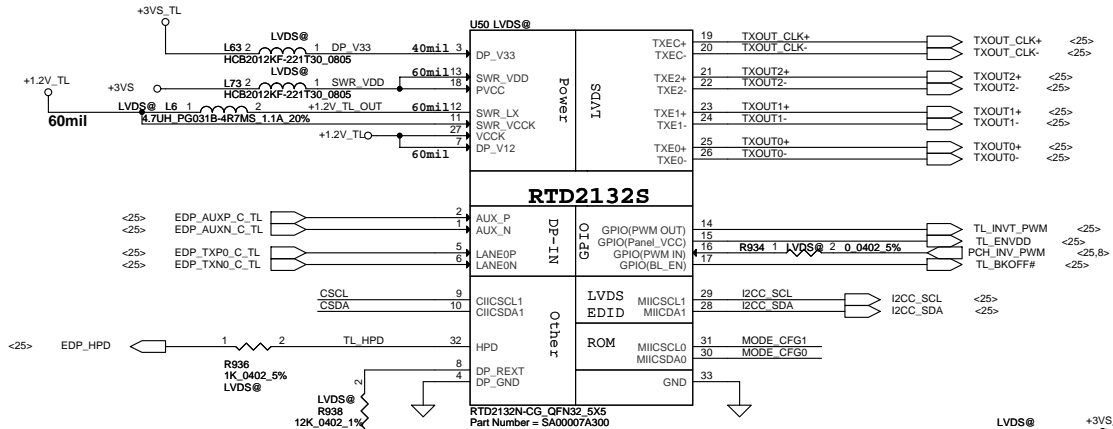
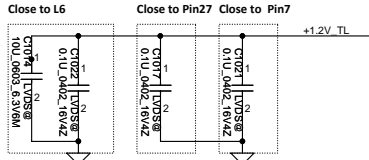
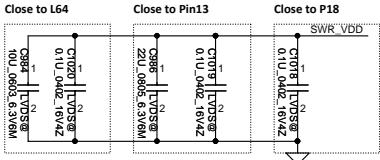
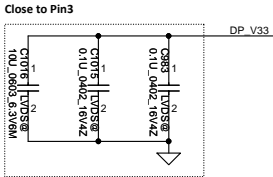
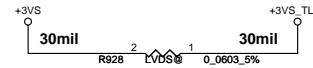
Figure 1 illustrates five data access methods. Each method is represented by a row with a label, a data source, and a data destination. The labels are all <18,22>. The data sources are DQSA[7..0], DQSA#[7..0], DQMA[7..0], MDA[63..0], and CMDA[30..0]. The data destinations are DQSA[7..0], DQSA#[7..0], DQMA[7..0], MDA[63..0], and CMDA[30..0]. Arrows indicate the direction of data flow from the source to the destination.

[illegible]

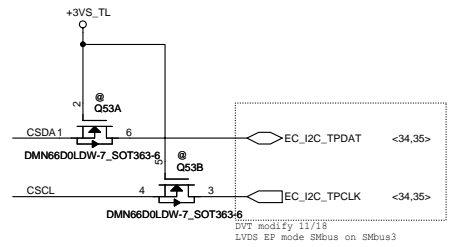
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



LVDS Translator - RTD2132R



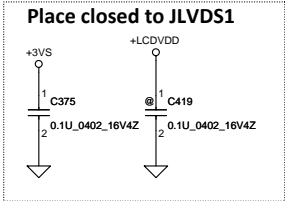
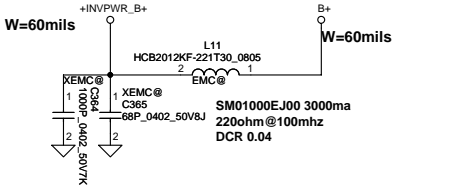
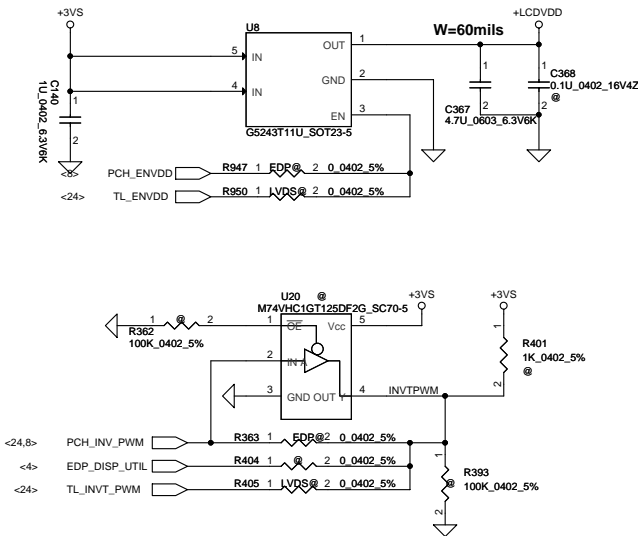
MODE_CFG0(PIN30)		
	0	1
MODE_CFG1(PIN31)	X	EP MODE
	ROM ONLY MODE*	EEPROM MODE



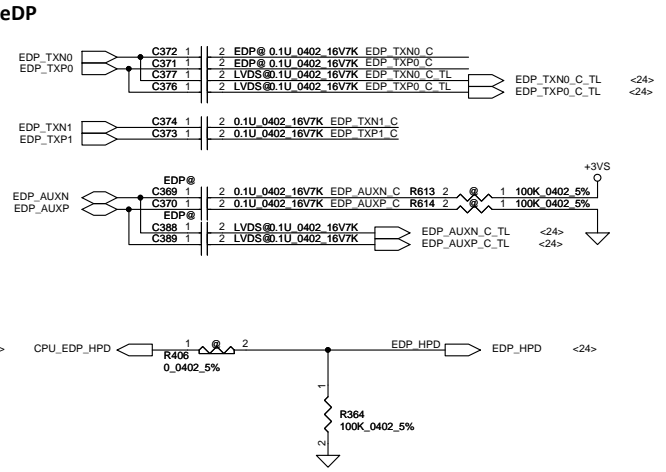
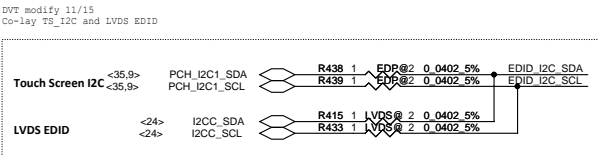
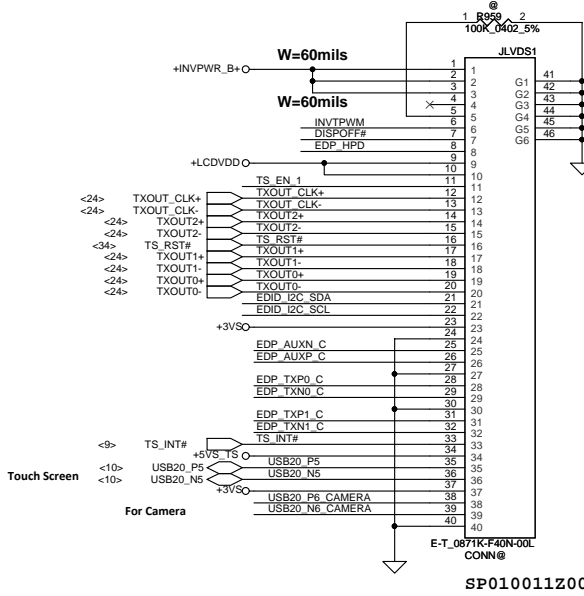
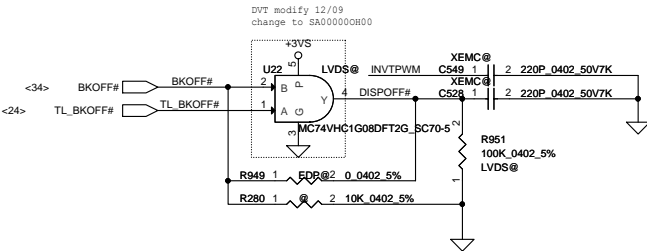


EDP / LVDS conn.

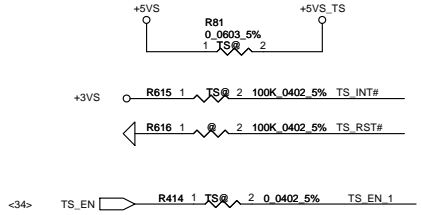
LCD POWER CIRCUIT



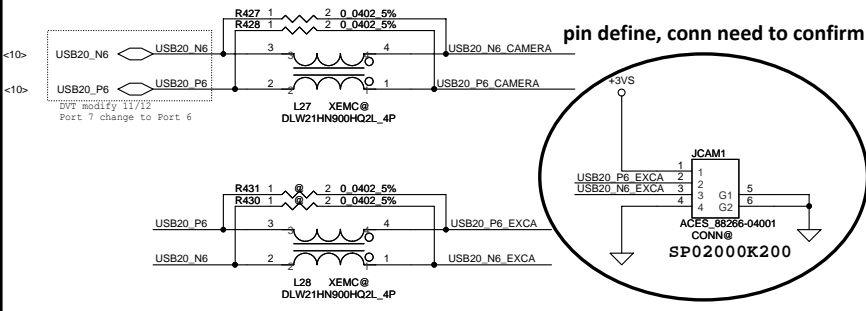
LCD/ LED PANEL Conn.



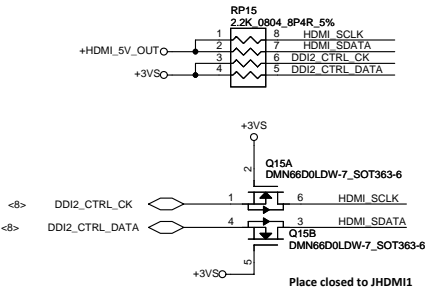
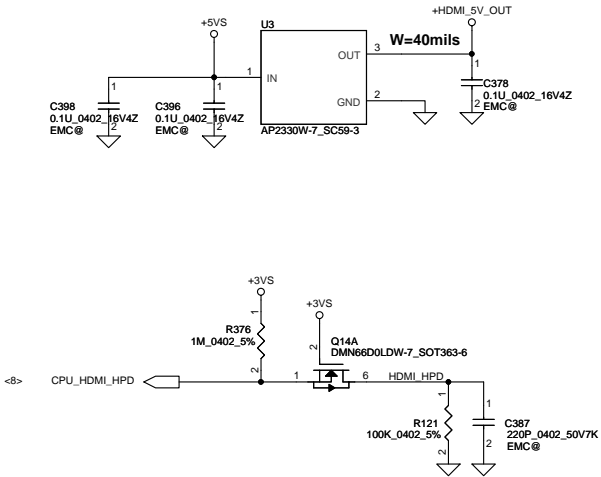
Touch Screen



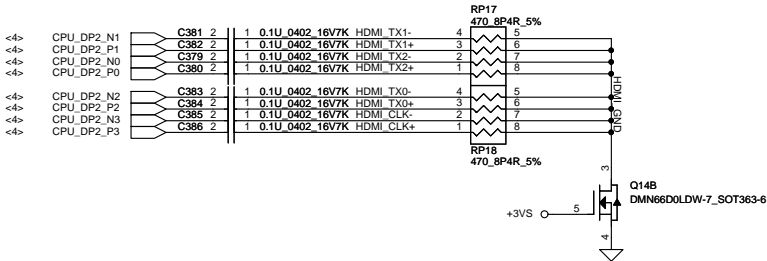
Camera



HDMI conn.

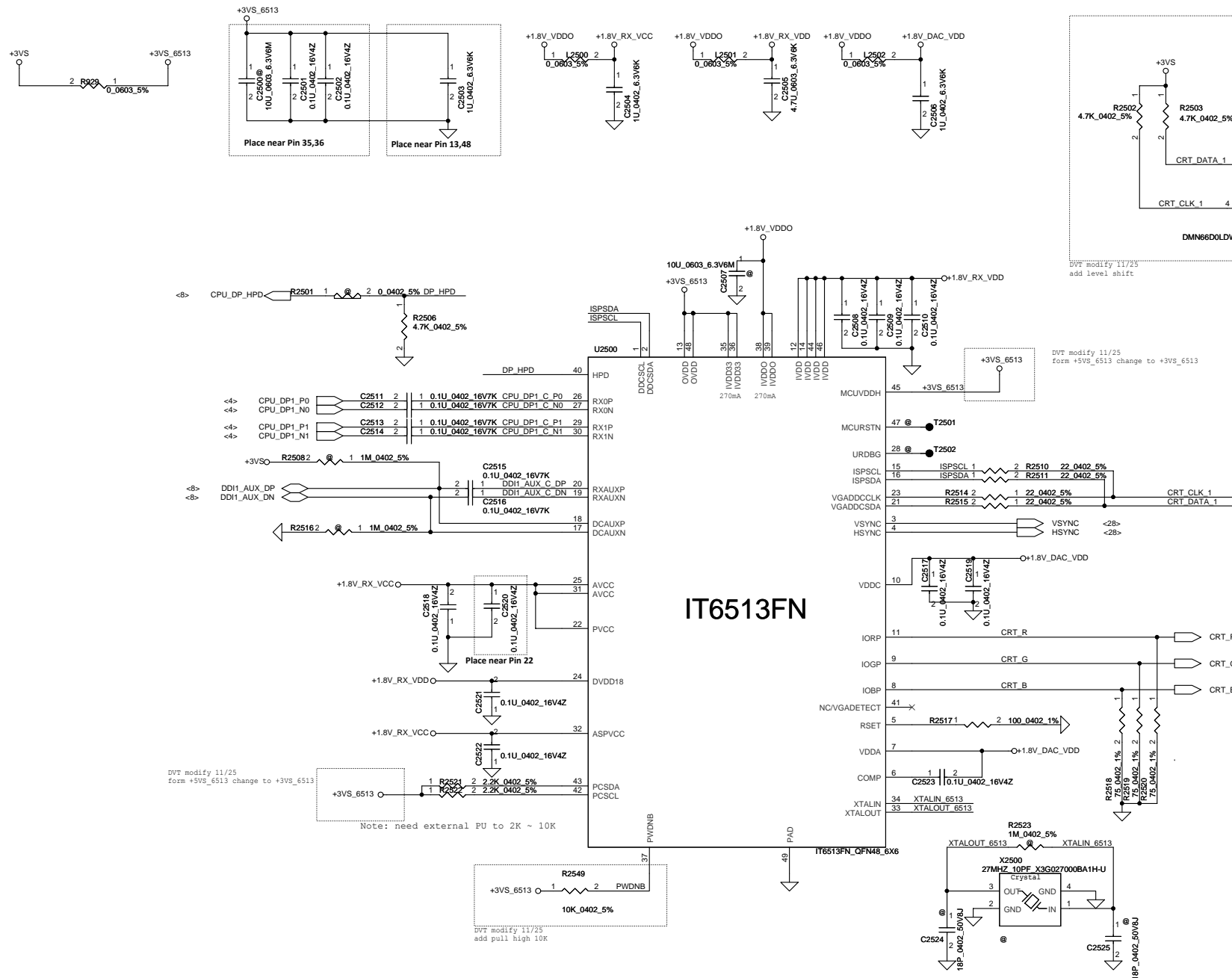


SM070001310 400ma 90ohm @100mhz DCR 0.3					
HDMI_CLK-	R368	1	XEMC@ 2	0.0402_5%	HDMI_R_CLK-
HDMI_CLK+	R369	1	XEMC@ 2	0.0402_5%	HDMI_R_CLK+
HDMI_TX0-	R370	1	XEMC@ 2	0.0402_5%	HDMI_R_D0-
HDMI_TX0+	R371	1	XEMC@ 2	0.0402_5%	HDMI_R_D0+
HDMI_TX1-	R372	1	XEMC@ 2	0.0402_5%	HDMI_R_D1-
HDMI_TX1+	R373	1	XEMC@ 2	0.0402_5%	HDMI_R_D1+
HDMI_TX2-	R374	1	XEMC@ 2	0.0402_5%	HDMI_R_D2-
HDMI_TX2+	R375	1	XEMC@ 2	0.0402_5%	HDMI_R_D2+



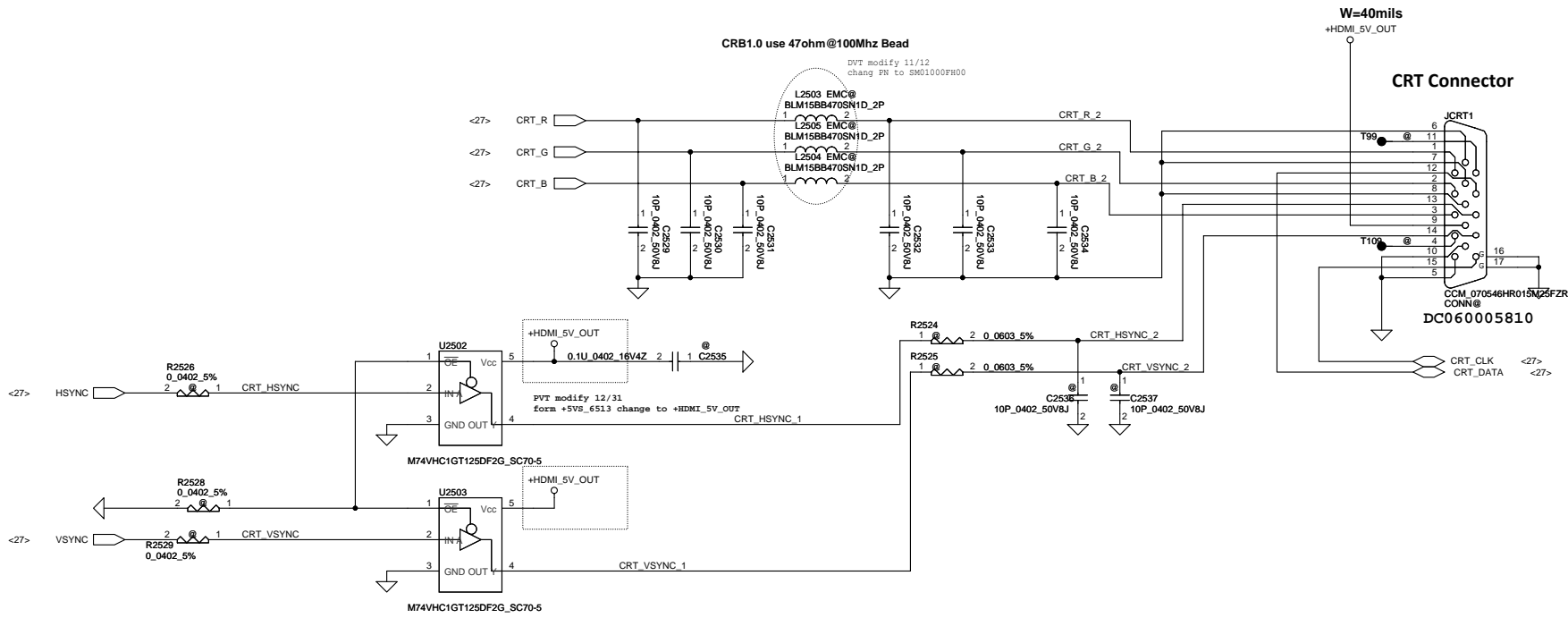
HDMI connector

## DP to VGA-IT6513



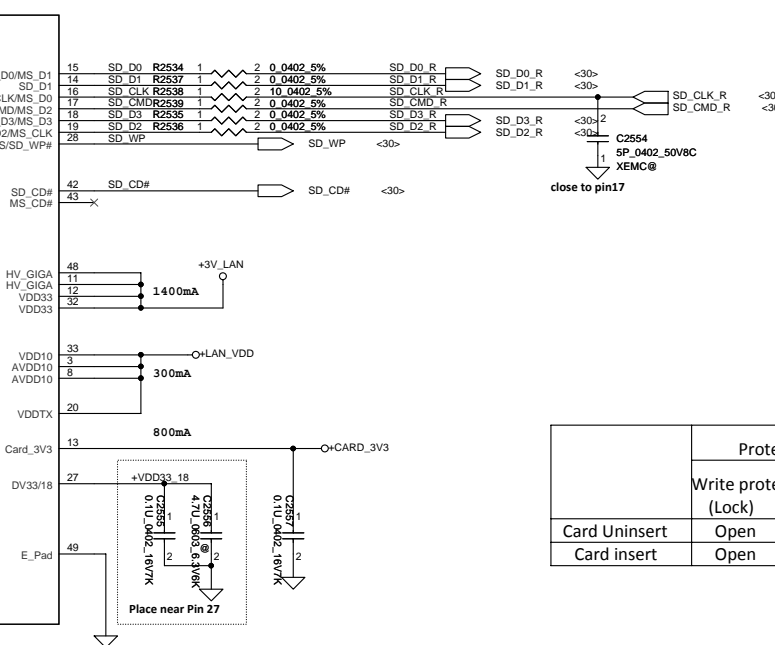
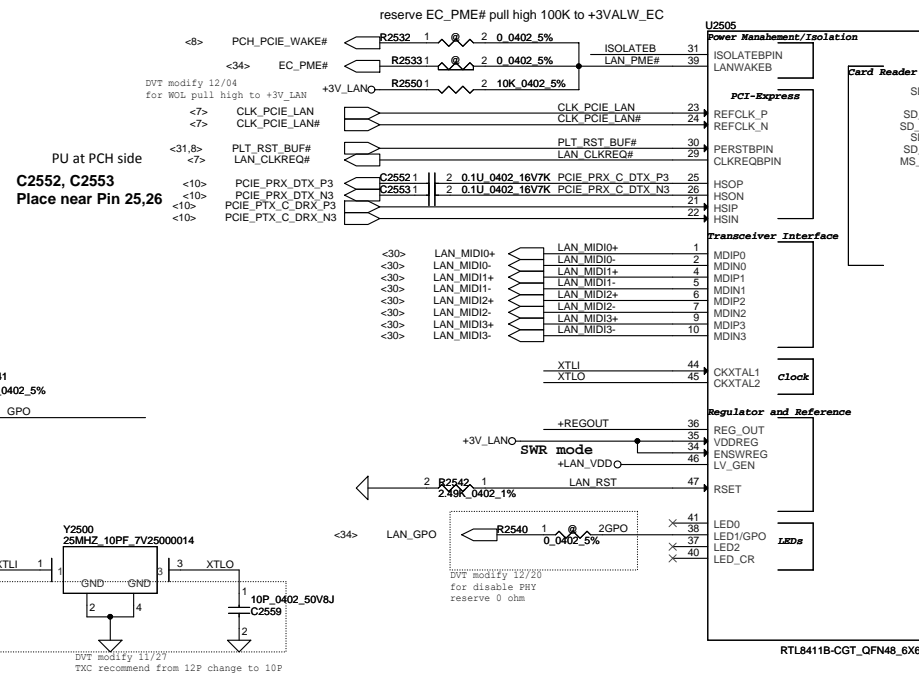
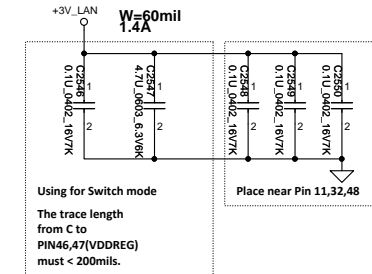
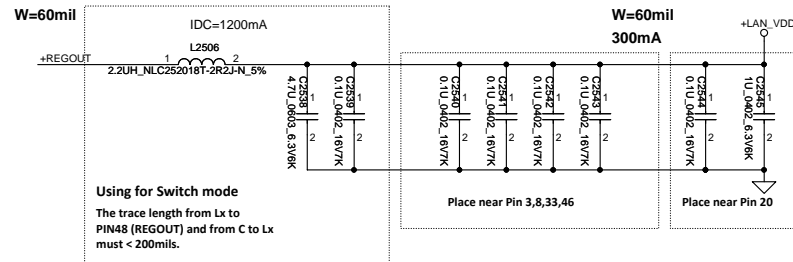
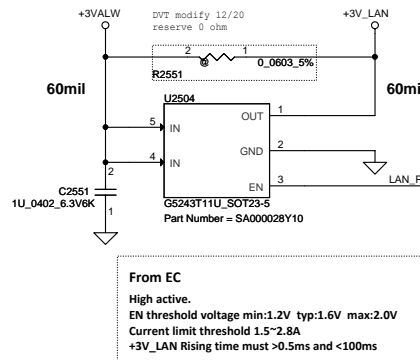
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CRT conn.



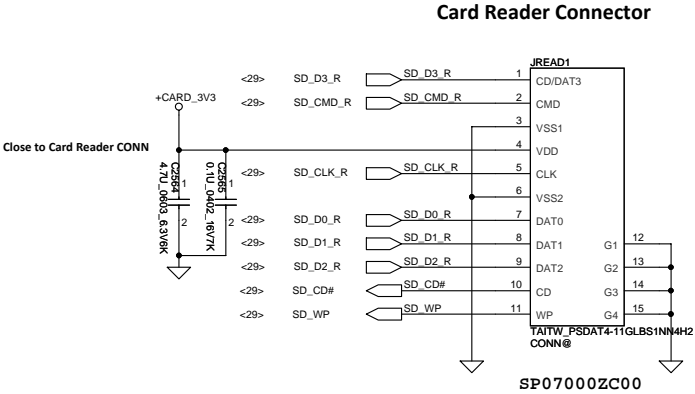
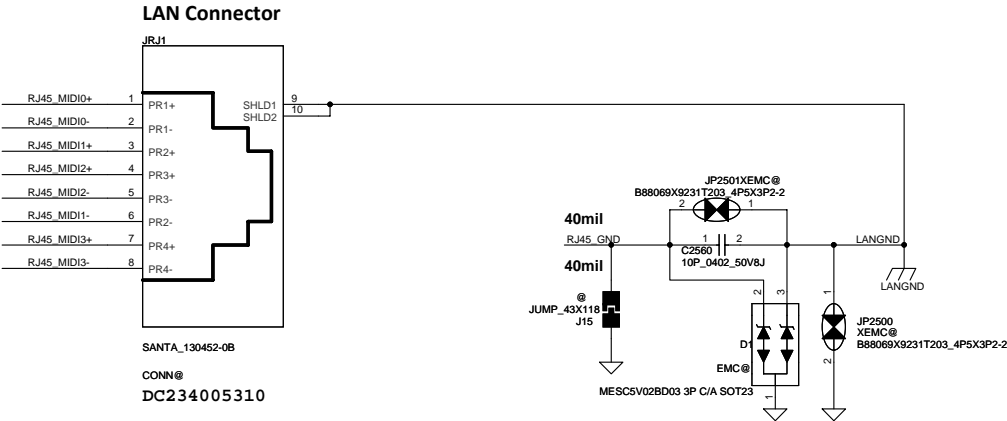
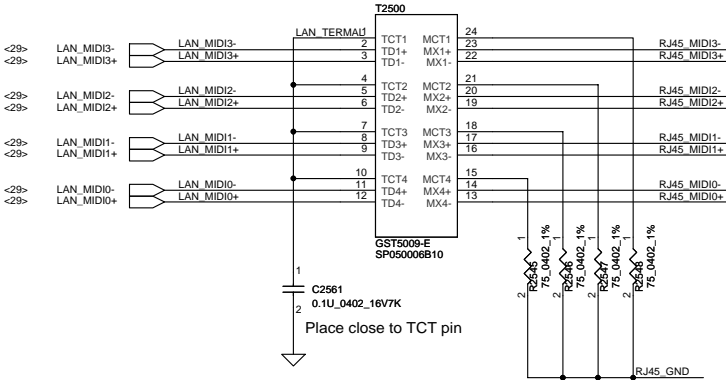
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# LAN-RTL8411B

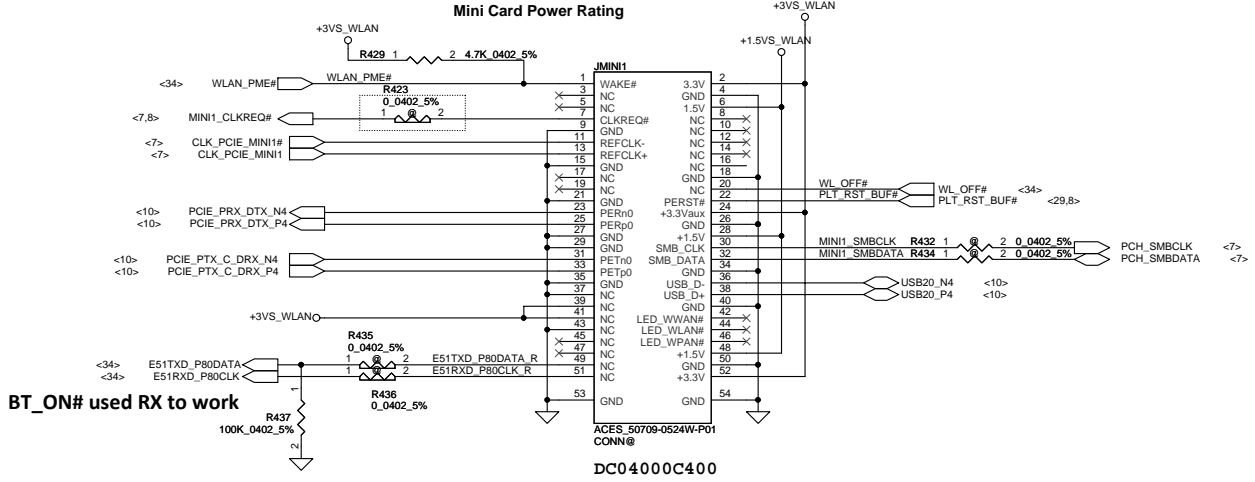
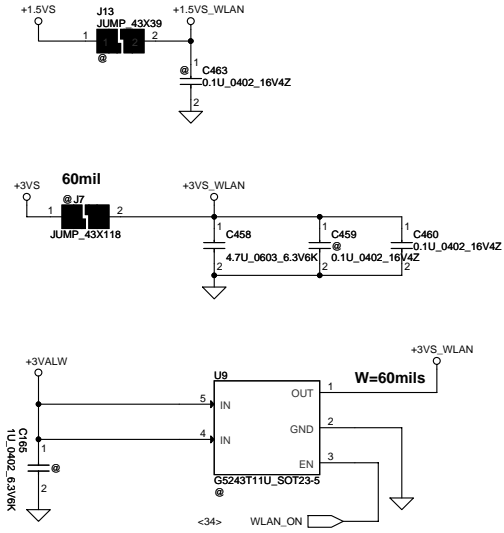


	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

RJ45 / Card Reader conn.

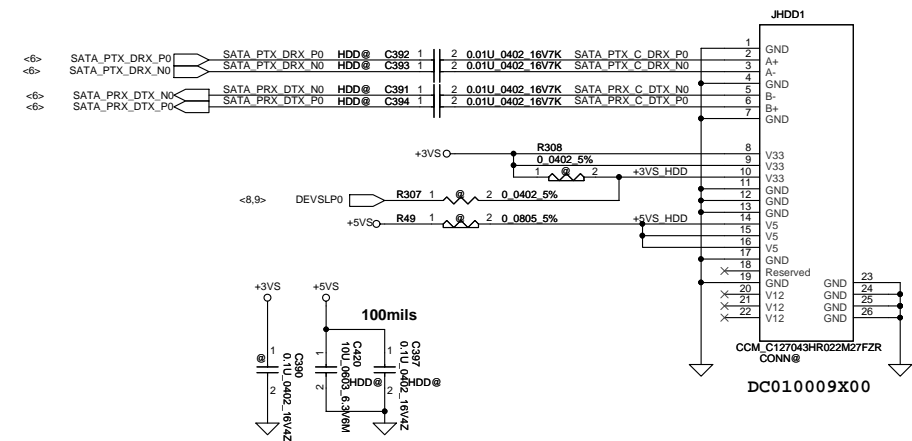


# Wireless LAN

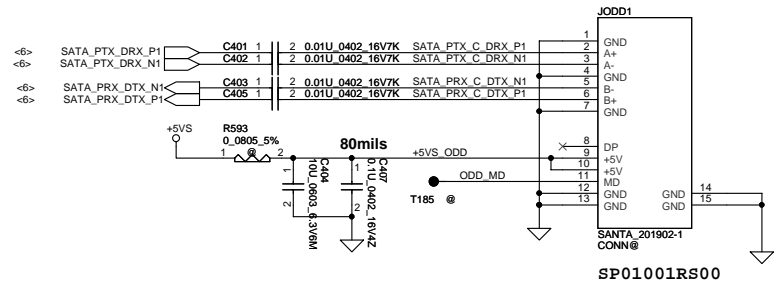


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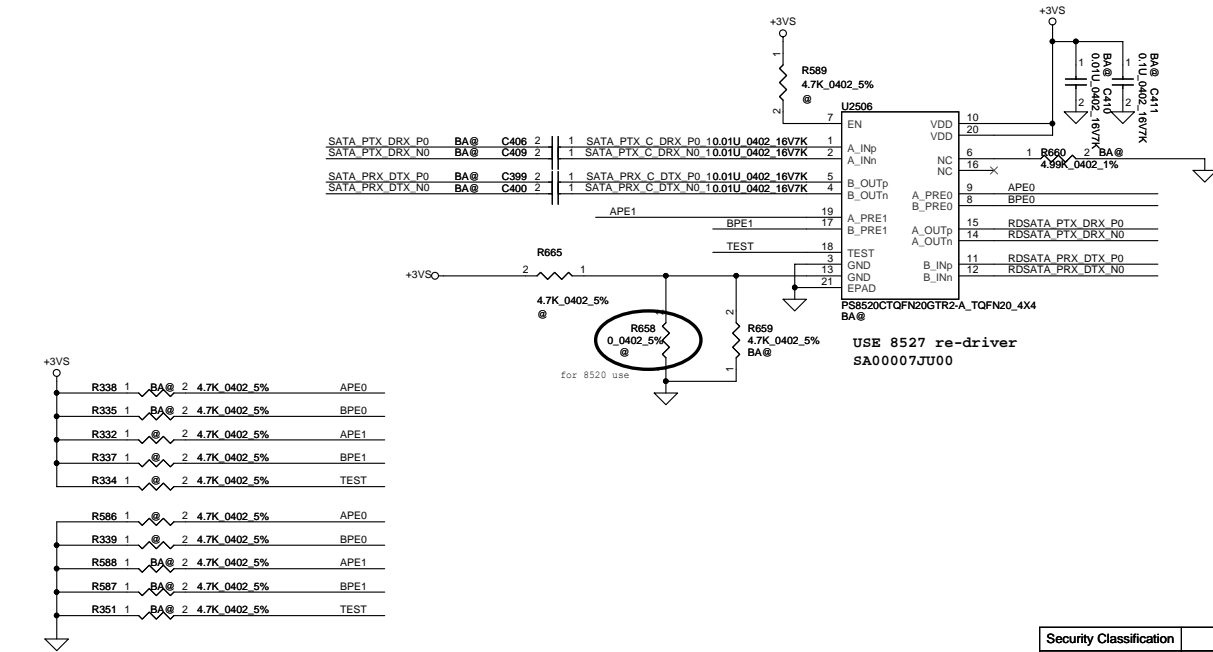
SATA HDD1 Conn.



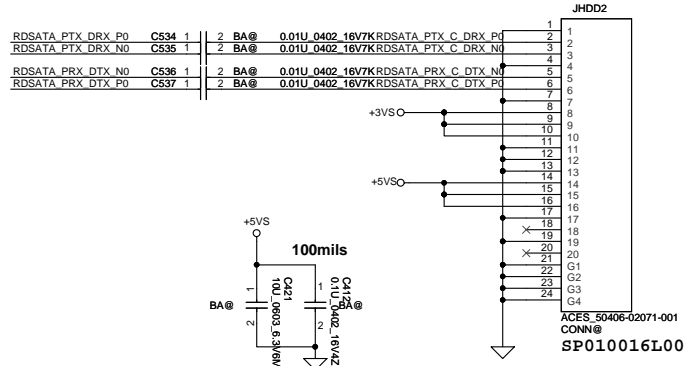
SATA ODD Conn.



SATA Re-Driver HDD Conn. for BA50

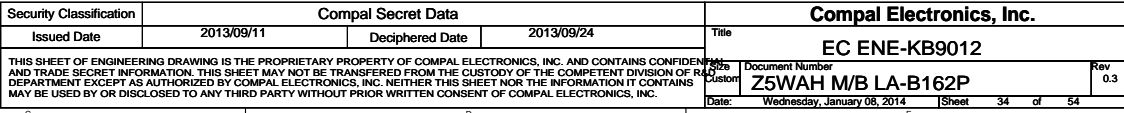


SATA HDD1 Conn.

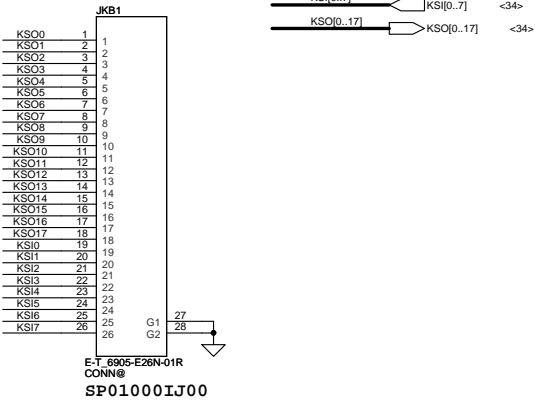




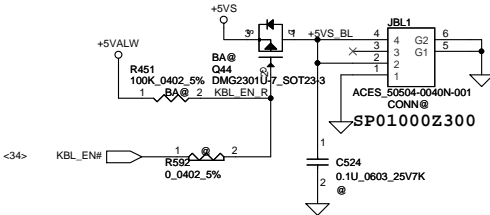




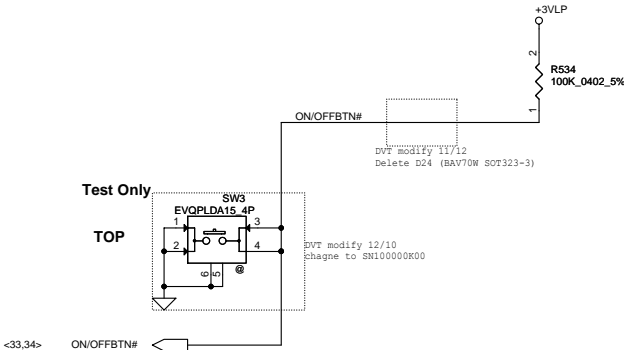
KB Conn.



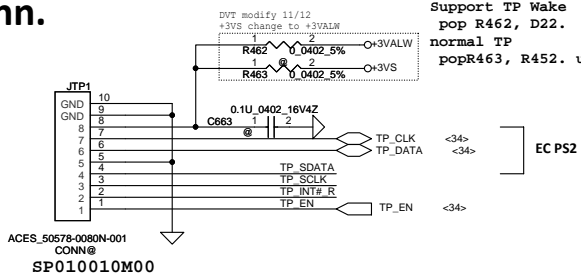
KB BackLight Conn. Reserve



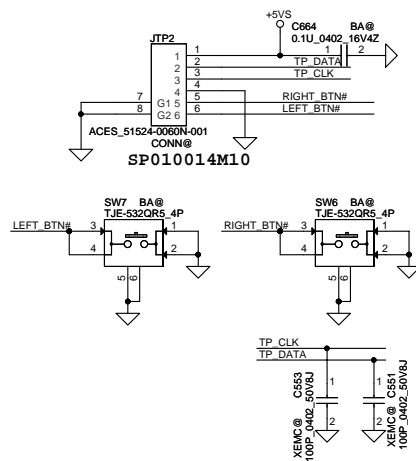
ON/OFF BTN



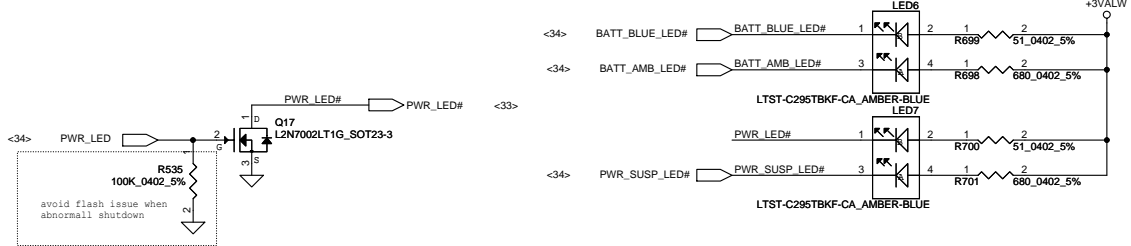
TP/B Conn.



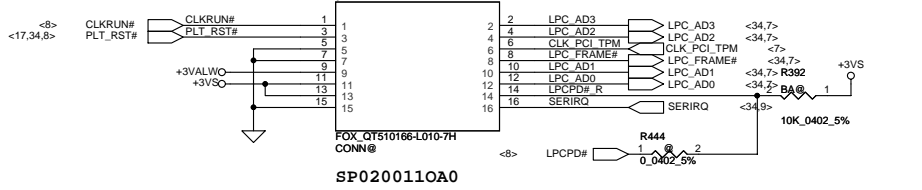
To BA50 TP/B Conn.



LED

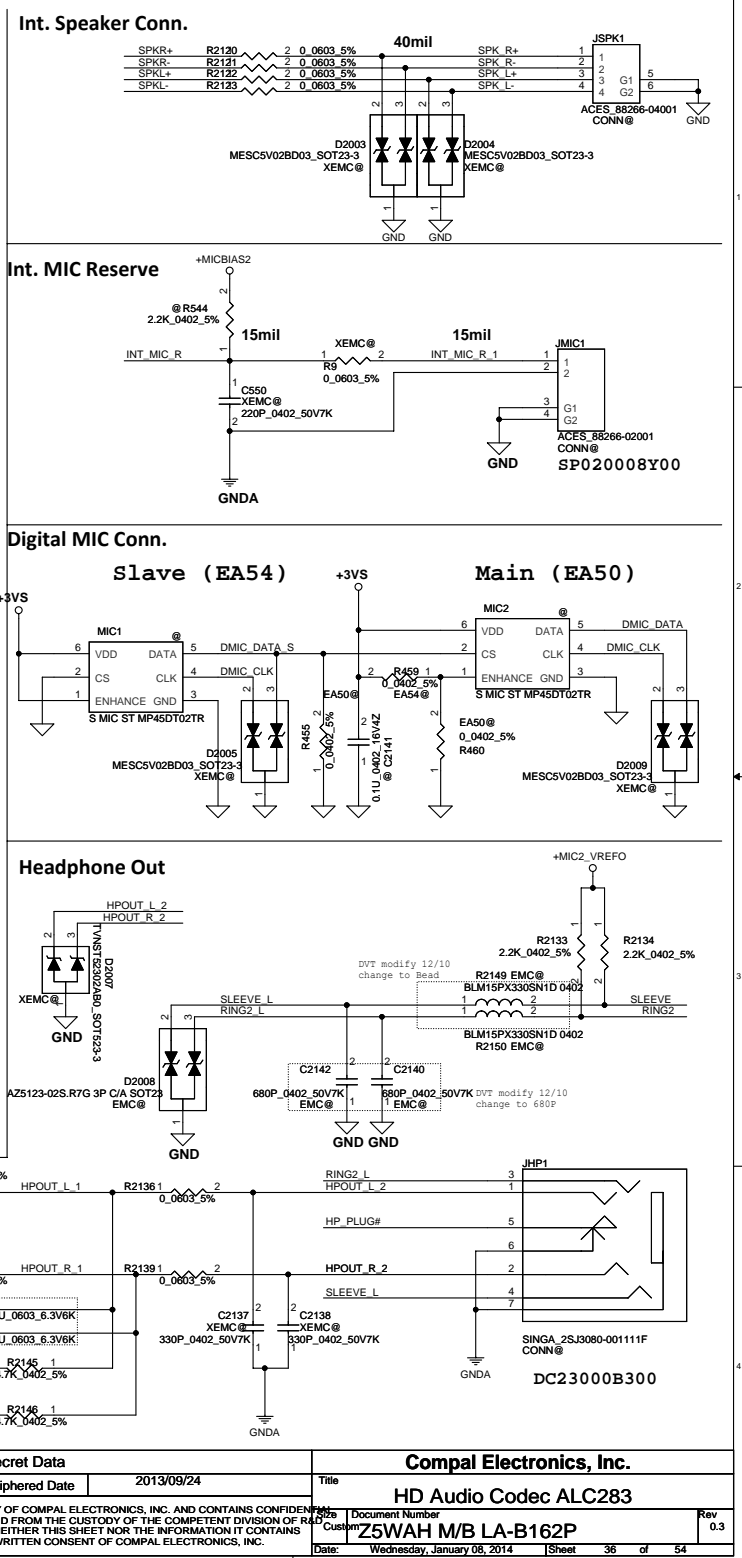
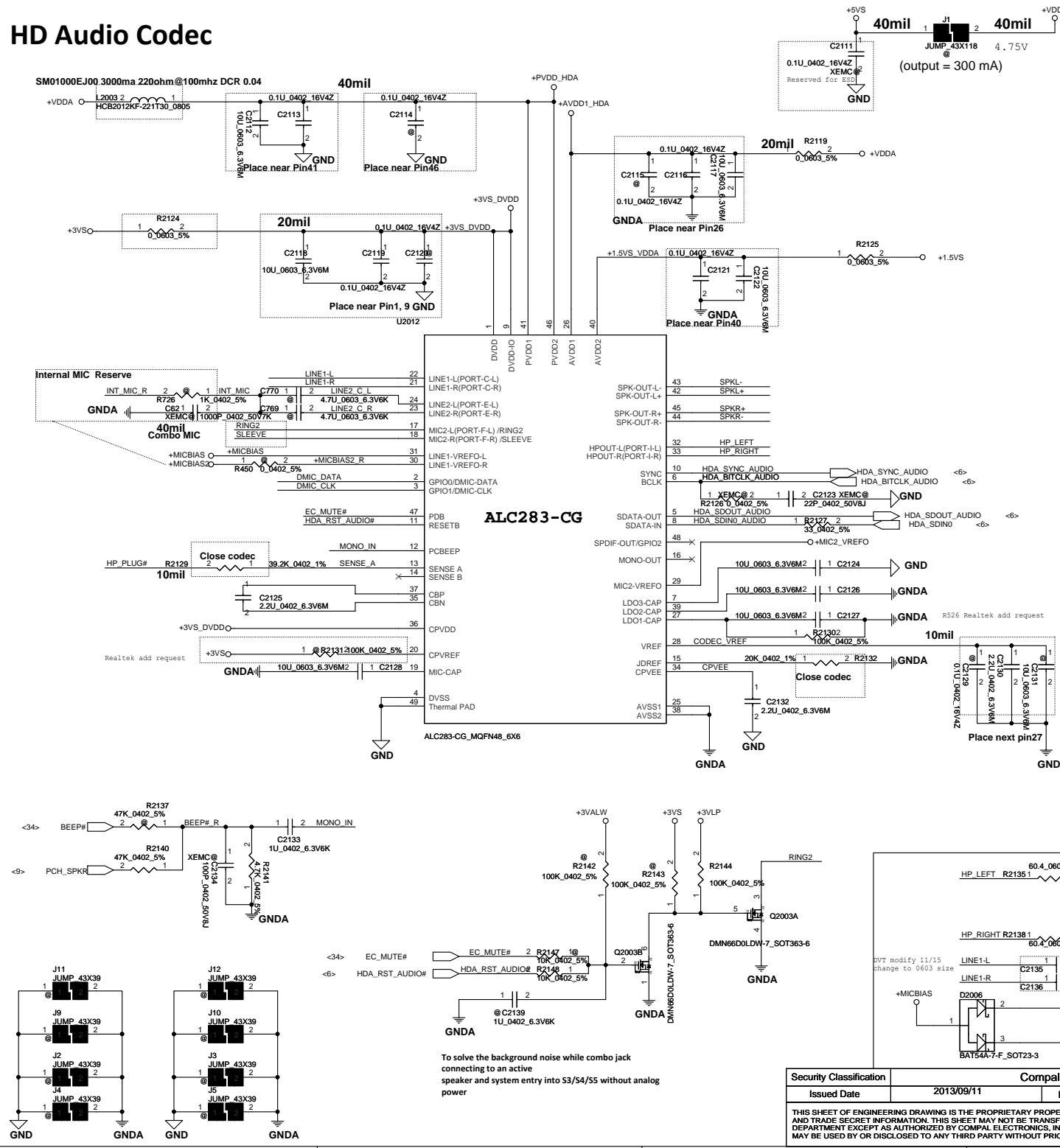


TPM Board for BA50



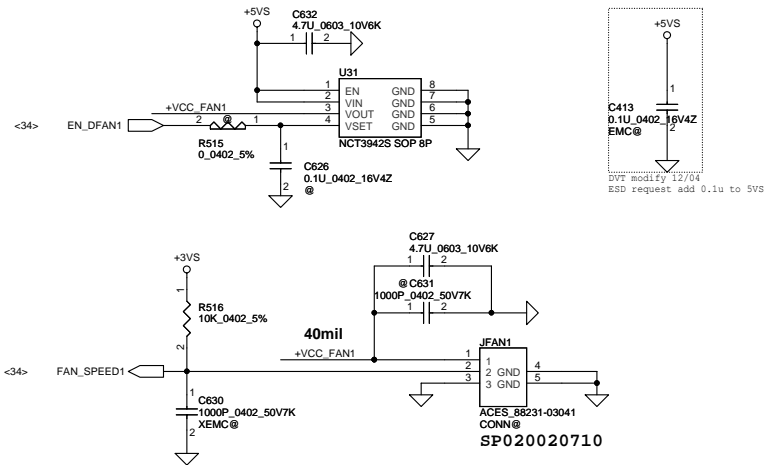
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## HD Audio Codec

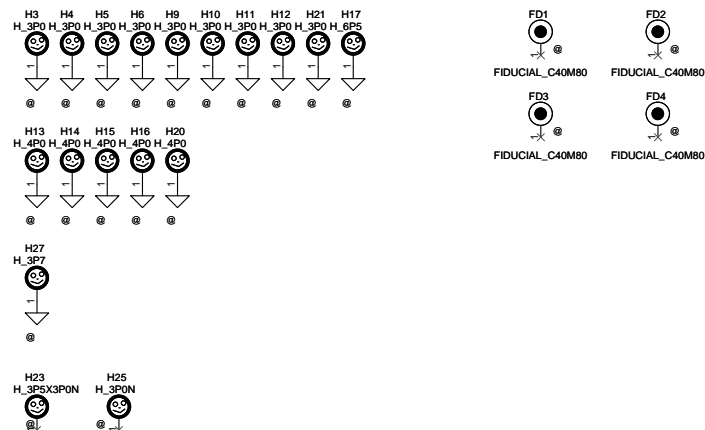


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				Doc Number		Rev	
				Customer		0.3	
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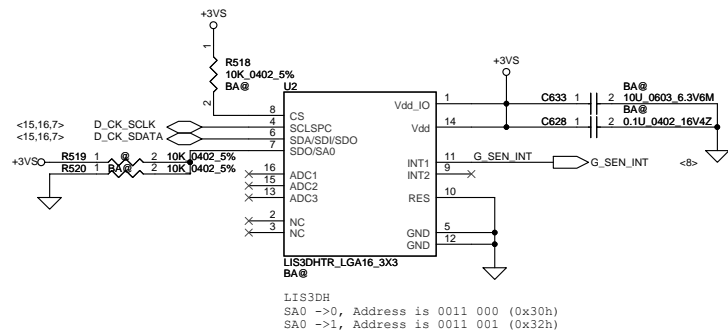
FAN1 Conn



Screw Hole

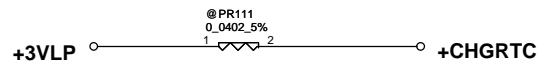
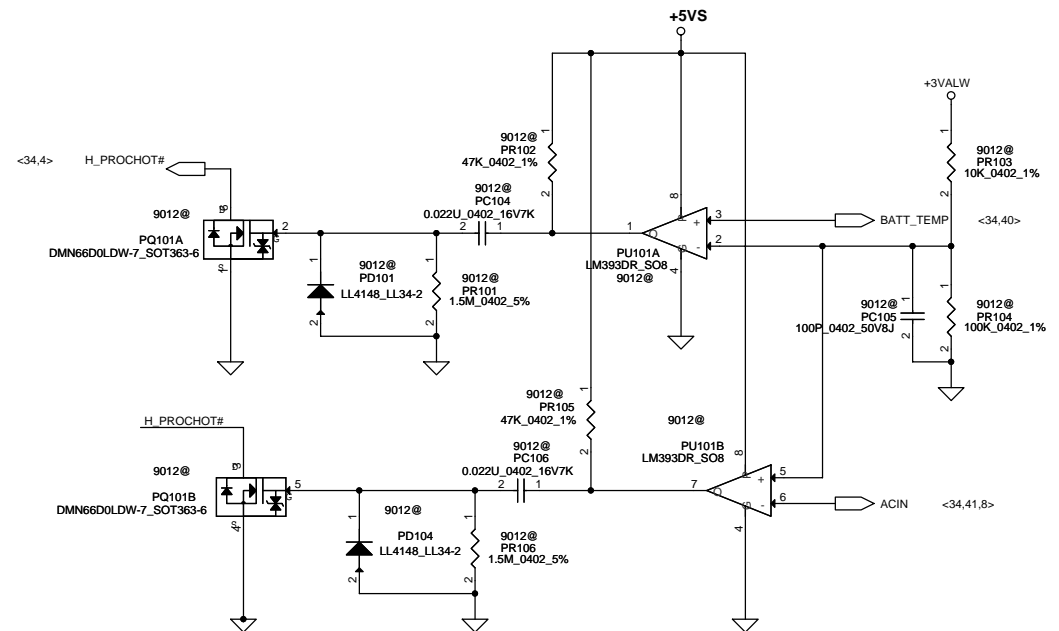
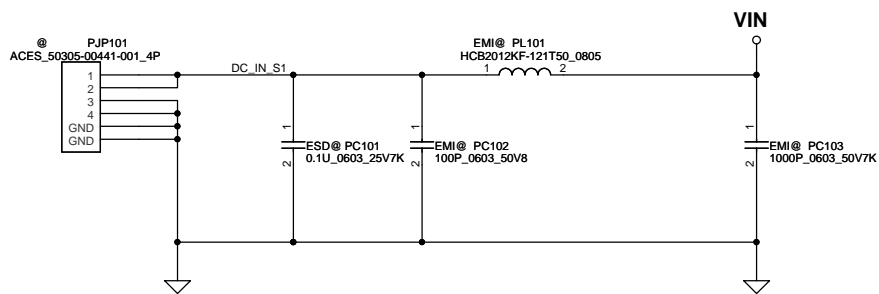


G-Sensor for BA50

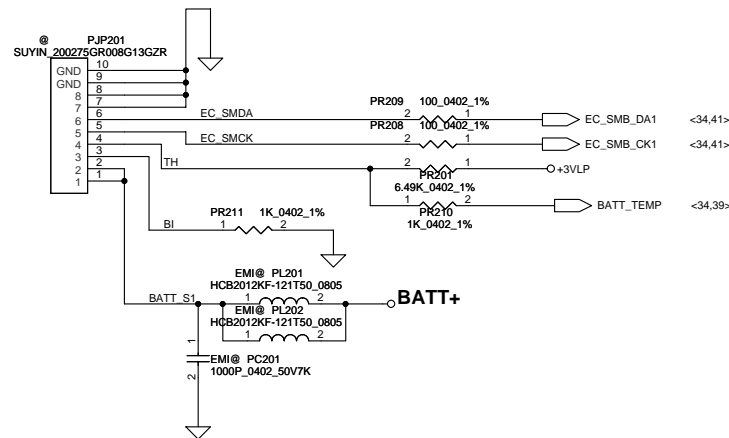


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Date:	Wednesday, January 08, 2014	Sheet	39	of	54



---Battery\_pin define---

PIN1 GND  
PIN2 GND  
PIN3 SMD  
PIN4 SMC  
PIN5 TS  
PIN6 B/I  
PIN7 Batt+  
PIN8 Batt+

---Battery Con\_pin define---

PIN8 GND  
PIN7 GND  
PIN6 SMD  
PIN5 SMC  
PIN4 TS  
PIN3 B/I  
PIN2 Batt+  
PIN1 Batt+

	For KB9012 OTP	For KB9022 OTP
92	1.2V	1.0V
56	1.2V	1.0V
PR216	22.6K ohm	32.4K ohm
PR227	26.1K ohm	30K ohm

2013/10/14 update

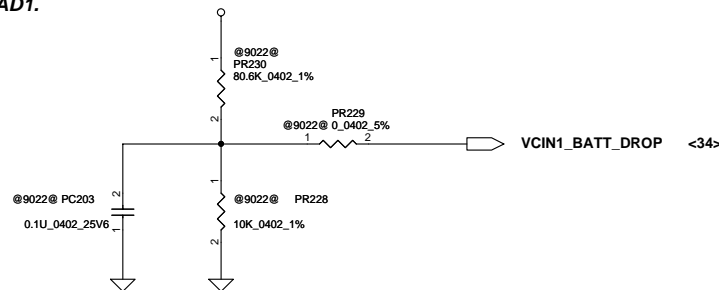
For KB9022 sense 20ms	Active	Recovery
40W	52W, 0.51V	40W, 0.51V
65W	84.5W, 0.82V	65W, 0.82V

PH201 under CPU bottom side :  
CPU thermal protection at 92 degree C ( shutdown )  
Recovery at 56 degree C

2013/10/02

Add for ENE9022 Battery Voltage drop detection. B+  
Connect to ENE9022 pin64 AD1.

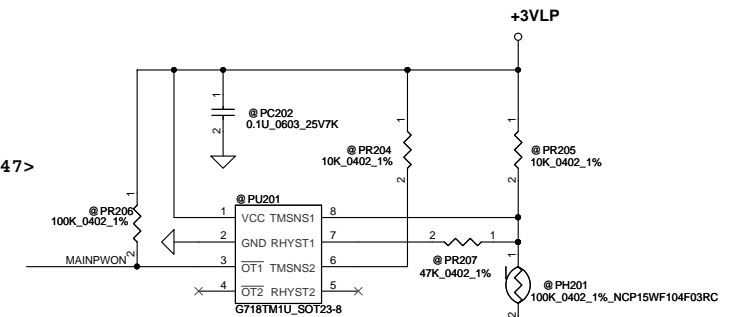
Battery is 3-cell design.  
B+=9V



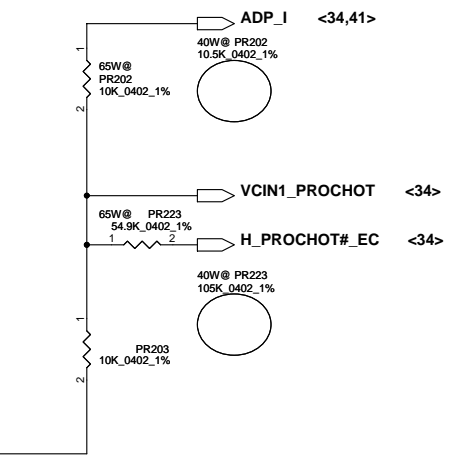
2013/10/28 update PH202 chang  
Common part SL200002H00

For 65W adapter==>action 70W , Recovery 54W  
For 40W adapter==>action 52W , Recovery 40W

<34> ECAGND



2013/10/28 update PH201 chang  
Common part SL200002H00



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				Size	Document Number	Rev
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Date:				Wednesday, January 08, 2014	ISheet	40 of 54



Protection for reverse input

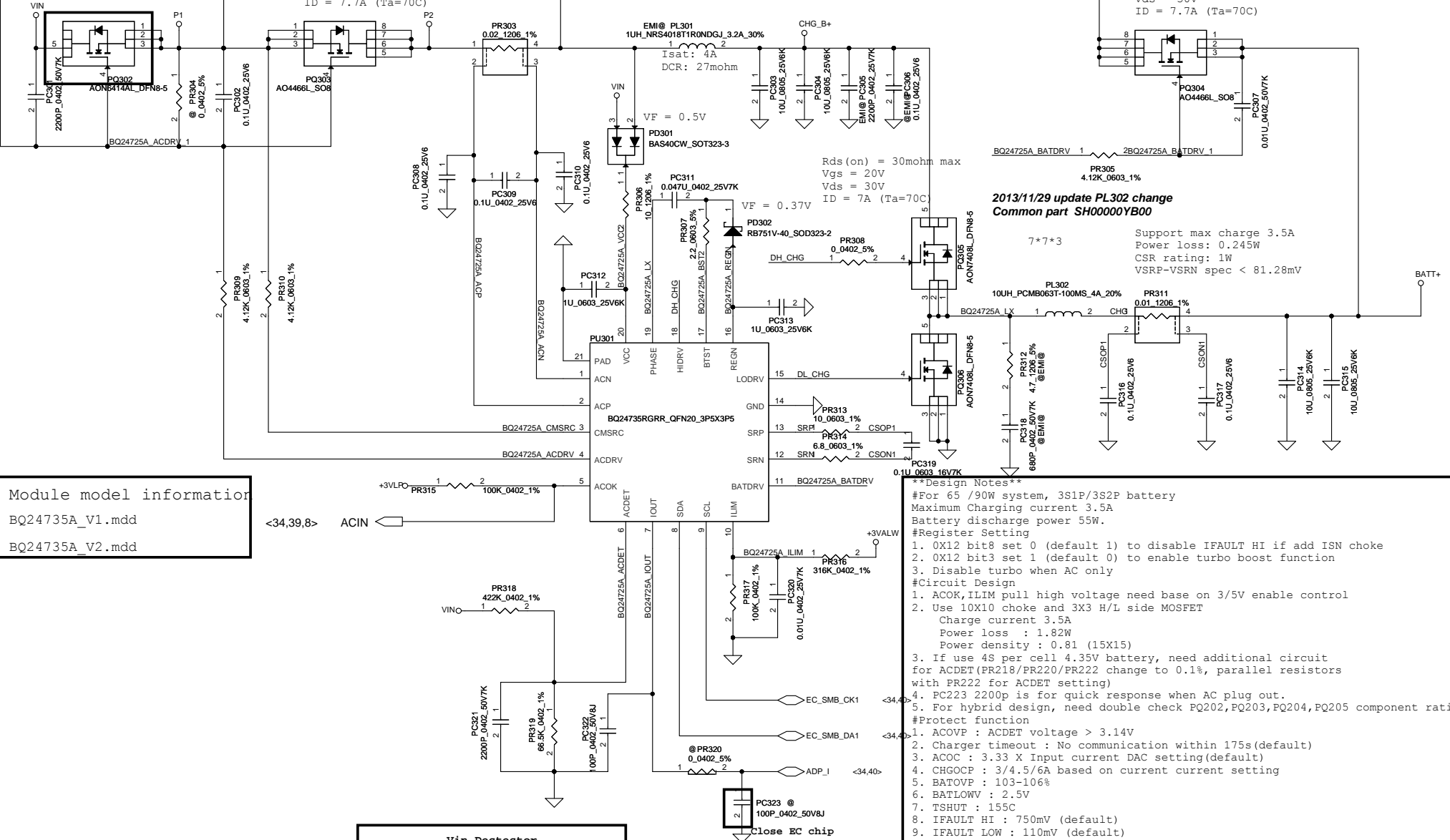
2013/10/14

PR303 10m ohm chang -->20m ohm  
SD00000S120

Rds(on) typ = 35mohm max  
Vgs = 20V  
Vds = 30V  
ID = 7.7A (Ta=70C)

Need check the SOA for inrush

Rds(on) = 35mohm max  
Vgs = 20V  
Vds = 30V  
ID = 7.7A (Ta=70C)



Module model information

BQ24735A\_V1.mdd

BQ24735A\_V2.mdd

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				Date	Wednesday, January 08, 2014
				Sheet	41 of 54
				Rev	0.3

SY8208B\_V2.mdd  
SY8208C\_V2.mdd

ENLDO\_3V5V

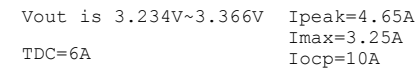
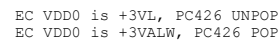
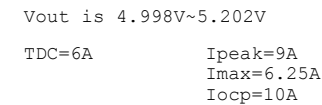


Diagram illustrating the JUMP 43X118 component. The component is represented by two rectangular blocks labeled 1 and 2. Block 1 is connected to the +5VALWP terminal, and Block 2 is connected to the +5VALW terminal. The component is identified as JUMP 43X118, with a reference to @PJ402.

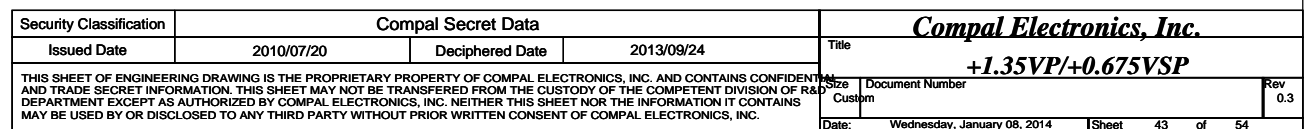


Compal Electronics, Inc.

+3VALW/+5VALW

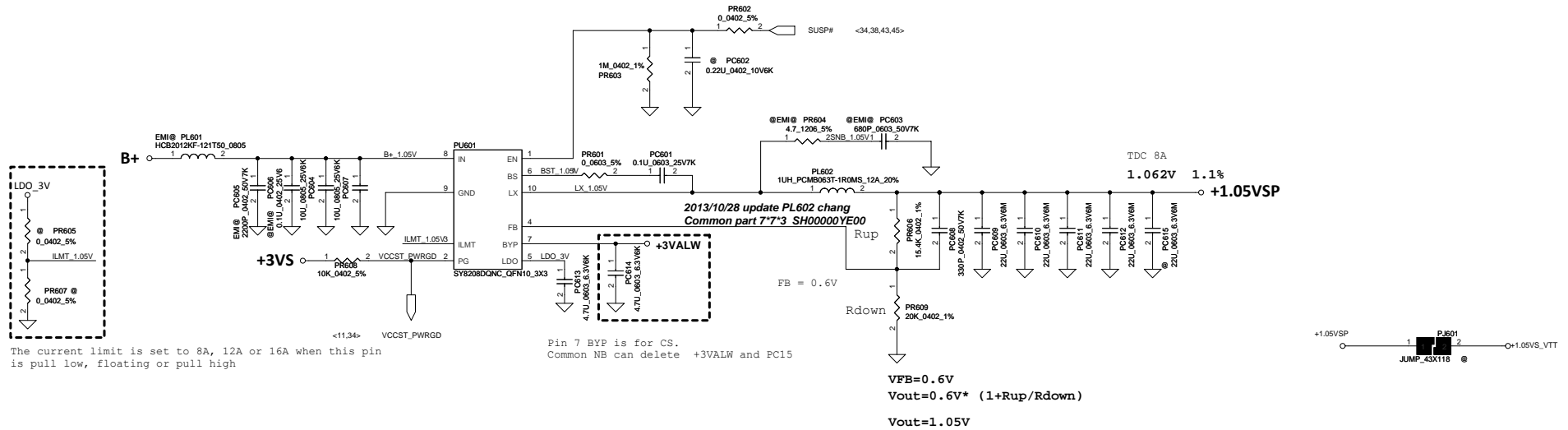
IDENTIFICATION OF RECORD NUMBER	Document Number Custom	Rev 0.3
Date: Wednesday, January 08, 2014		Sheet 42 of 54

RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

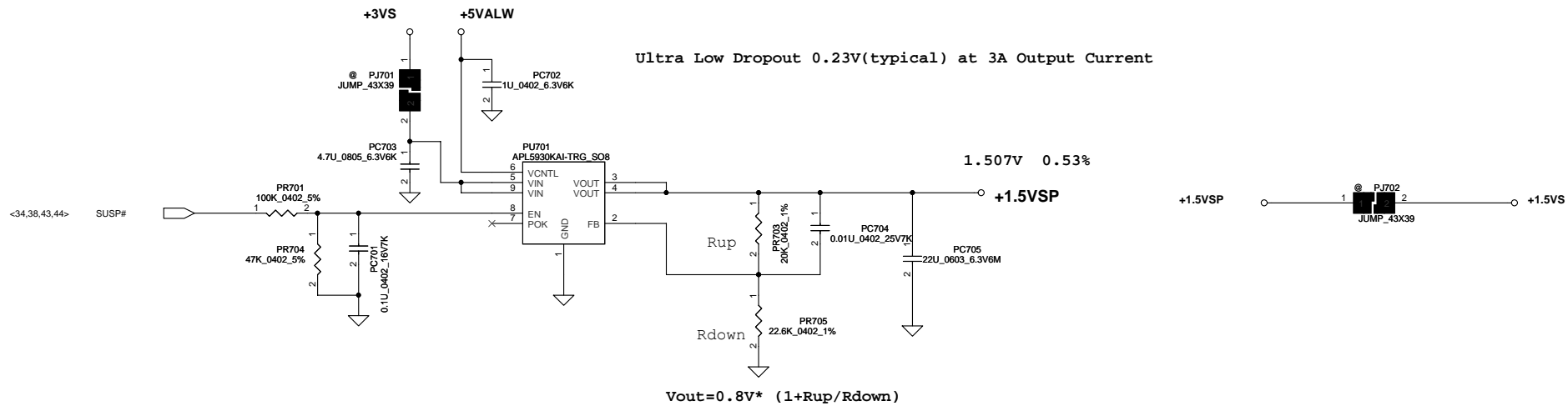


Module model information  
SY8208D\_V1.mdd

EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



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				Date:	Wednesday, January 08, 2014
				Sheet	44 of 54



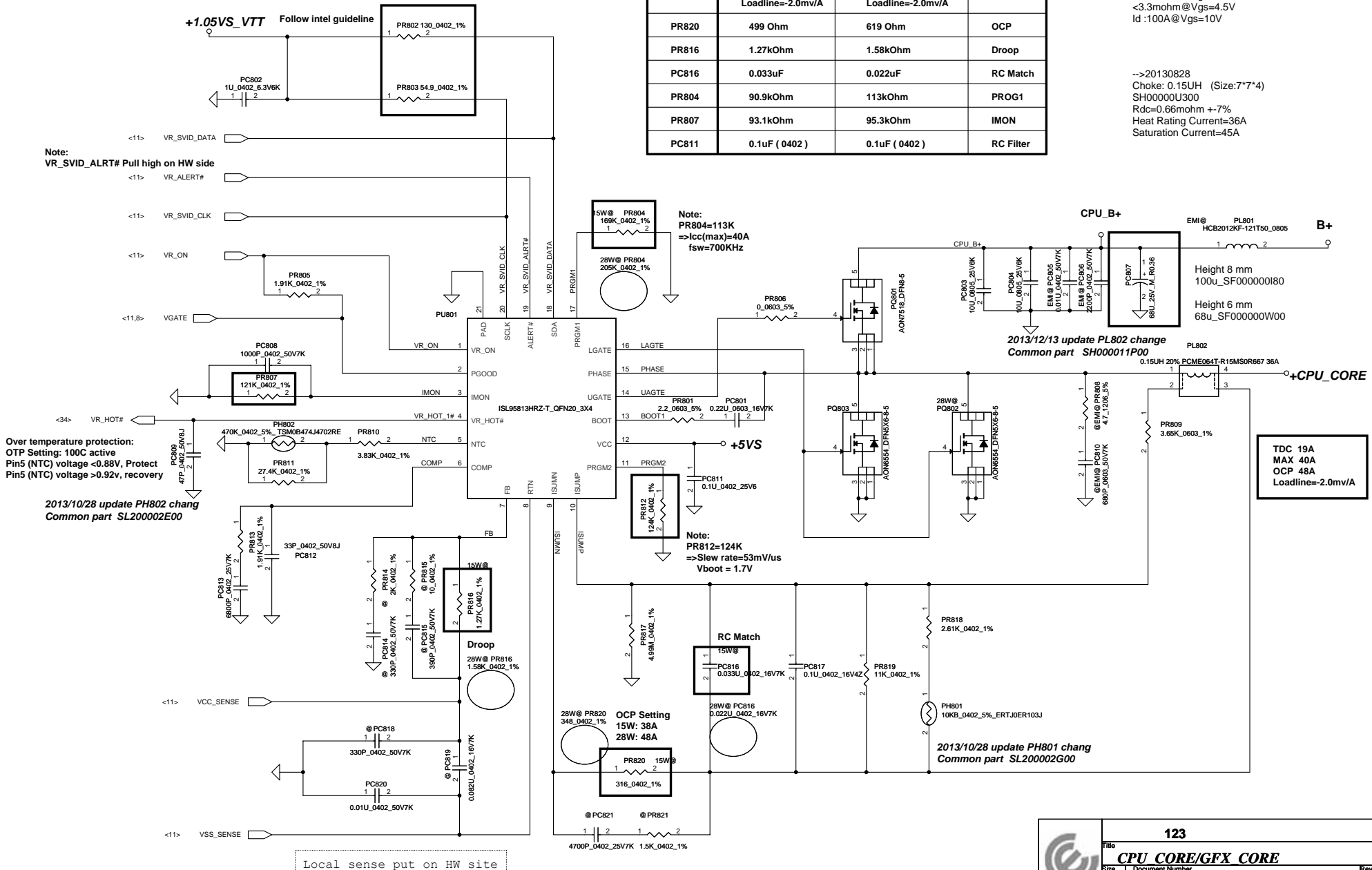
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/13	Deciphered Date	2013/09/24	Title	<b>+1.5VSP</b>	
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				Custom		0.3
				Date:	Wednesday, January 08, 2014	Sheet 45 of 54

**Module model information:**  
ISL95813 (for 15W & 28W CPU)

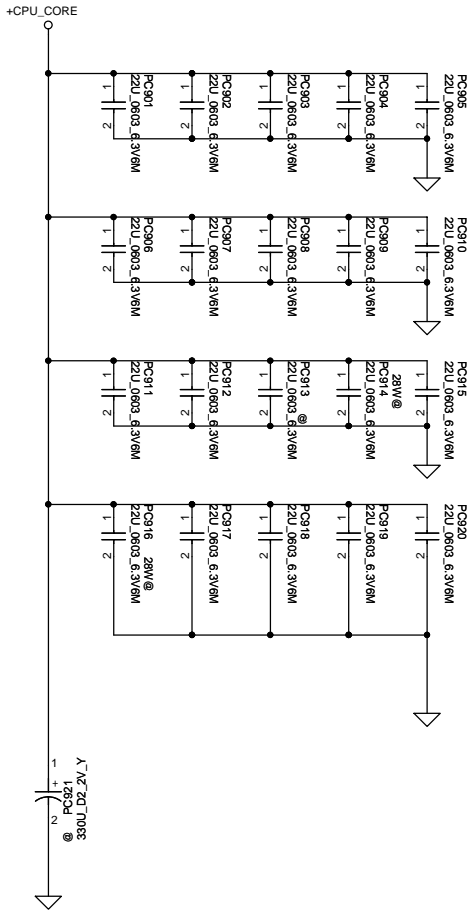
Base on BDW PDDG Rev_0_73			
Location	15W	28W	Note
	TDC 14A	TDC 19A	
	MAX 32A	MAX 40A	
	OCp 38.4A	OCp 48A	
	Loadline=-2.0mv/A	Loadline=-2.0mv/A	
PR820	499 Ohm	619 Ohm	OCp
PR816	1.27kOhm	1.58kOhm	Droop
PC816	0.033uF	0.022uF	RC Match
PR804	90.9kOhm	113kOhm	PROG1
PR807	93.1kOhm	95.3kOhm	IMON
PC811	0.1uF ( 0402 )	0.1uF ( 0402 )	RC Filter

L-side MOS: MDU1511RH  
Rds(on):  
<2.4mohm@Vgs=10V  
<3.3mohm@Vgs=4.5V  
Id :100A@Vgs=10V

-->20130828  
Choke: 0.15UH (Size:7\*7\*4)  
SH00000U300  
Rdc=0.66mohm +-7%  
Heat Rating Current=36A  
Saturation Current=45A



PWR Rule  
需確認最新SPEC.  
Modify 8/6.

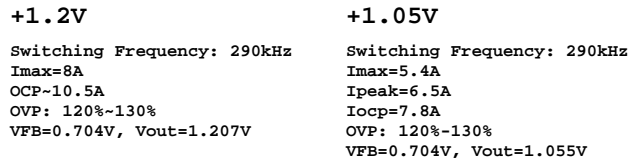


30 X 22uF 0805  
2012/10/23  
check the output cap Qty!!!  
2012/10/24  
23 pcs 22uF and reserve 7 pcs  
2013/01/14  
22uF\*17 unpop:22uF\*3

20130828  
15W: 22uF\*14  
28W: 22uF\*16

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								Size		Document Number		Rev	
								Custom				0.3	
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TPS51212\_V1.mdd for Single layer  
TPS51212\_V2.mdd for Dual layer



Vout	PR1007	PR1008	PR1003
+1.5V	11.5k	10k	
+1.35V	9.31k	10k	
+1.2V	7.15K	10k	105K
+1.05V	4.99k	10k	93.1k

The diagram illustrates the JUMP @PJ002 instruction. It shows a +1.5VSDGPUP input connected to pin 1 of a 2-to-1 multiplexer. The output of the multiplexer is connected to pin 1 of another 2-to-1 multiplexer, which is also connected to a +1.5VSDGPU output. Both multiplexers are controlled by a JUMP @PJ002 instruction, with pin 2 of the first multiplexer and pin 2 of the second multiplexer both connected to the JUMP @PJ002 instruction.

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Issued Date	2011/07/29	Deciphered Date		Title	<b>1.5VSDGPUP</b>	
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Module model information:  
RT8813A\_V1A for IC module  
RT8813A\_V1B for SW module

$V_{boot} = V_{vref} * R_{ref1} / (R_{ref1} + R_{boot})$   
 $R_t = R_{refadj} // (R_{boot} + R_{ref2})$   
 $V_{min} = V_{vref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R_t / (R_{ref1} + R_t)]$   
 $V_{max} = V_{vref} * R_{ref2} / (R_{ref1} // R_{refadj} + R_{boot} + R_{ref2})$   
 $V_{out} = V_{min} + N * V_{step}$   
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

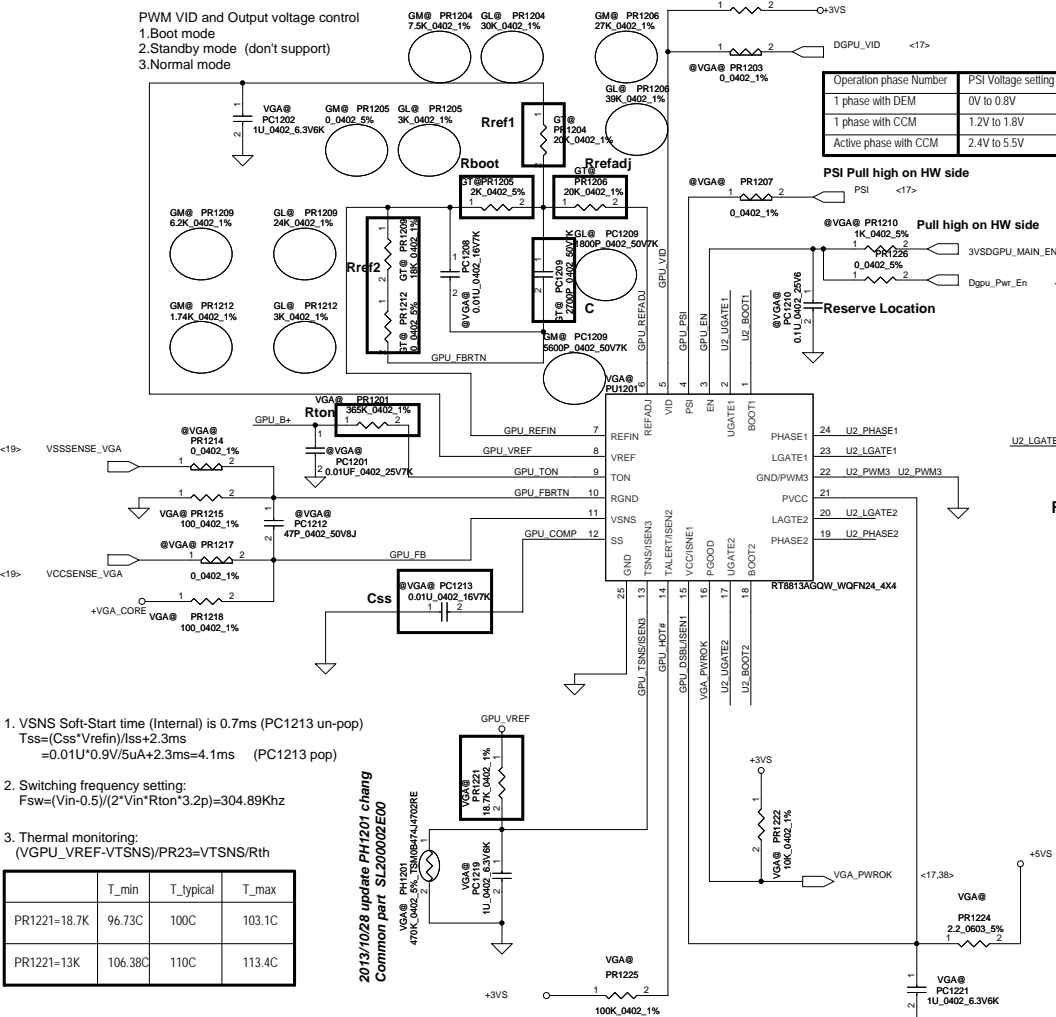
PWM-VID Spec and component Values

PWM-VID Spec		Config B	Config C	Config D
Vmin		0.6V	0.65V	0.9V
Vmax		1.2V	1.15V	1.15V
Vboot		0.9V	0.9V	1.028V
Voltage step		6.25mV	25mV	12.5mV
N of Voltage level		96	20	20
Rrefadj	PR1204	20K	39K	27K
Rref1	PR1204	20K	30K	7.5K
Rboot	PR1205	2K	3K	0
Rref2=PR1209 +PR1212	PR1209	18K	24K	6.2K
	PR1212	0	3K	1.74K
C	PC1209	2.7nF	1.8nF	5.6nF

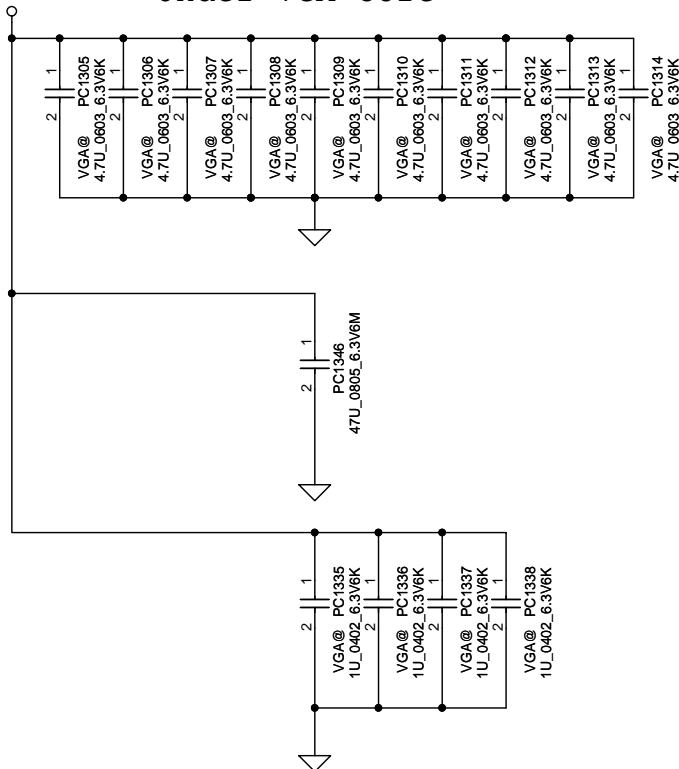
Current Limit threshold setting  
 $R_{ocset} = (I_{valley} * R_{ds(on)} + 40 \text{ mV}) / 10uA$   
 $I_{ripple} = (19.0.9) * 0.9 / (304.89KHz * 0.36u * 19) = 7.811A$   
OCp=54A/2=27A per phase  
 $I_{valley} = 27A * 7.811A / 2 = 23.1A$   
H-side MOS:AON6552  
Rds(on): 5.6mohm @ Vgs=10V  
6.7mohm @ Vgs=4.5V  
Id :20A @ Ta=25 degC  
L-side MOS:AON6554  
Rds(on): 3.2mohm @ Vgs=10V  
3-3.8mohm @ Vgs=4.5V  
Id :85A @ Ta=25 degC  
Choke: 0.22uH (Size:7\*7\*4)  
Rdc=0.97mohm +5%  
Heat Rating Current=34A  
Saturation Current=25A  
C=3\*330uF (9mohm)=990uF  
 $V_{ripple} = I_{ripple} * ESR(\text{min}) = 7.811A * 3mohm = 23.4mV$

Different VGA Chip (different EDP-Peak M) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT	N15S-GT	N15V-GM
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config C
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W	18W	18.16W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W	25W	24.72W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A	31A	29.2A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A	60A	44.3A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A		
OCp Setting Current	42A	66A	54A	42A	42A	48A	72A	90A	72A	54A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K	13K	10.2K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L	2phase 1H1L	2phase 1H1L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)		
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL	GT@	GM@



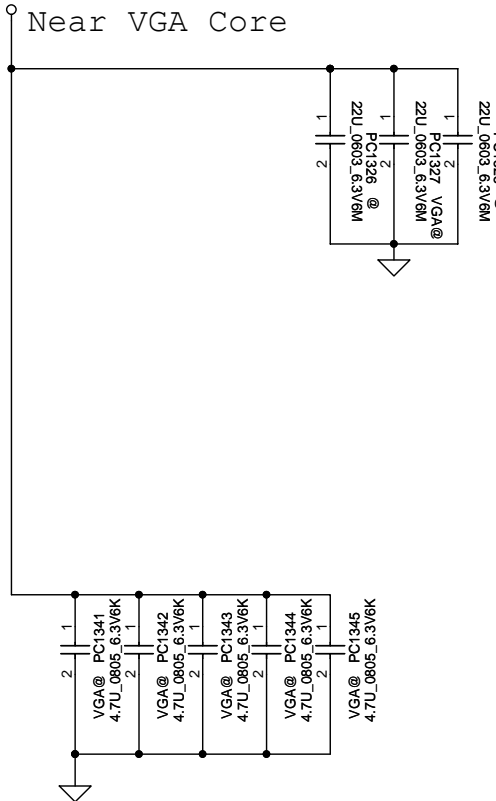
# **+VGA\_CORE** Under VGA Core



# **+VGA\_CORE**

## **+VGA\_CORE**

### Near VGA Core



N15x 2013/12/10  
Under  
4.7uF\_0603\_10pcs  
1uF\_0402\_4pcs  
Near  
47uF\_0805\_1pcs  
22uF\_0603\_1pcs(2PCS unpop)  
4.7uF\_0805\_5pcs

N15x2013/10/17  
Under  
4.7uF\_0603\_15pcs  
1uF\_0402\_8pcs  
Near  
47uF\_0805\_0pcs  
22uF\_0603\_9pcs(2PCS unpop)  
4.7uF\_0805\_5pcs

N15x2013/10/07  
Under  
4.7uF\_0603\_15pcs  
1uF\_0402\_8pcs  
Near  
47uF\_0805\_0pcs  
22uF\_0805\_9pcs(2PCS unpop)  
4.7uF\_0805\_5pcs

N15x2013/10/02  
Under  
4.7uF\_0603\_15pcs  
1uF\_0402\_8pcs  
Near  
47uF\_0805\_0pcs  
22uF\_0805\_14pcs  
4.7uF\_0805\_5pcs

N14x  
Under  
4.7uF\_0603\_10pcs  
0.1uF\_0402\_4pcs  
Near  
47uF\_0805\_1pcs  
22uF\_0805\_1pcs  
4.7uF\_0805\_5pcs

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				Size	Rev
				Custom	0.3
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				Docu- ment Number	Rev	0.3
Date:	Wednesday, January 08, 2014	Sheet	51	of	54	

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	Module Design	Module Design change 3/5V solution	3/5V	Un-pop PR1	11/13	DVT
2						
12						
13						
14						
15						
16						
17						

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Issued Date	2012/07/10	Deciphered Date	2013/09/24	Title		
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				Date Customer		Document Number Rev
				Date: Wednesday, January 08, 2014		Sheet 52 of 54

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	material update		P28	L2503/2504/2505 Change P/N from SM01000GA00 to SM01000FH00	11/12	DVT
2	material update		P34	L31/L32 Change P/N from SM010030010 to SM010009U00	11/12	DVT
3	design update		P35	Delete D24, ON/OFF change to ON/OFFBTN#	11/12	DVT
4	schematics update	for TP_INT# wake function	P35	TP PIN1 VCC Connect to +3VALW, add R462, R463@, pop D22, R633, R453	11/12	DVT
5	design change		P10	Change USB port 5 for TS/port 6 for CCD / port 7 for CR(USB)_FP	11/12	DVT
6	design update		P6	reserve RTCRST# to EC pin 27 for clear CMOS add R490, and Q52 reserve to EC_RTCRST#	11/12	DVT
7	design update	EC board ID	P34	Pop R503(100K), R506(12K)	11/15	DVT
8	material update		P36	change C2135, C2136 to 0603 size	11/15	DVT
9	material update		P33	L24, L25 form SM070003Y00 to SM070003K00	11/15	DVT
10	material update		P7	pop share rom	11/15	DVT
11	design update	Co-lay TS_I2C and LVDS EDID	P25	R415, R433 for LVDS EDID R438, R439 for TS I2C	11/15	DVT
12	design update	for LVDS EP mode SMBus2 change to SMBus3	P24	Add R491 reserve for RTD2132 EP_MODE	11/18	DVT
13	design update	<del>for TP_INT# wake function</del>	P34	<del>GPI055 change to GPI013</del>	11/18	DVT
14	design update	for GC62.0 function	P17	R2055 change to Pull high +3VSDGPU_AON	11/20	DVT
15	design update	for +1.05VS_VTT leakage issue	P38	+5VALW change to +3VLP add level shift(Q2501)、R2503, R2502、R2549 Del R930	11/20	DVT
16	design update	for IT 6513 leakage issue	P27	IT6513 change to use 3VS	11/26	DVT
17	material update	for TXC recommend	P6	C153, C2, C3 to 15PF, C2004, C2005, C2558, C2559 to 10PF	11/27	DVT
18	design update	for wake on LAN function	P29	add R2550 10K pull high to +3V_LAN , PCH side pull high reserve	12/04	DVT
19	design update	for ESD request	P37	add C413 0.1u to +5VS	12/04	DVT
20	design update	<del>for EMI request</del>	P33	<del>add choke(L29,L30) and R(R456, R457,R462,R463) co-lay for USB/B comm</del>	12/04	DVT
21	design update	for ESD request	P36	add R2149, R2150( SM01000NH00), C2140, C2142(680PF) D2008(SCA00001B00) change to SOT23 R2135,R2138 chagne to 60 ohm	12/10	DVT
22	material update			SW3 SN100007700 chagne to SN100000K00 C408, C486 SF000002Y00 change to SF000006R00 C18, C118 SF000002Z00 change to SF000006S00	12/13	DVT
23	design update		P37	reserve R2551 0 ohm +3VALW to +3VLAN reserve R2540 for disable PHY	12/20	DVT

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Issued Date	2012/07/10	Deciphered Date	2013/09/24	Title PIR-HW	
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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	design issue		P28	U2052, U2503 change power rail to +HDMI_5V_OUT	12/31	PVT
2	material update	PVT board ID	P34	R506 change to 15K	12/31	PVT
3	design update	modify DQS P/N pin	P18		01/08	PVT
4	schematics update					
5	design change					
6	design update					
7	design update					
8	material update					
9	material update					
10	material update					
11	design update					
12	design update					
13	design update					
14	design update					
15	design update					
16	design update					
17	material update					
18	design update					
19	design update					
20	design update					
21	design update					
22	material update					
23	design update					

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