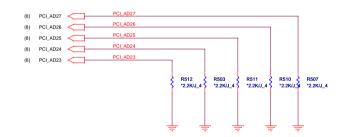


REQUIRED STRAPS

	 PCI_CLK1	 PCI_CLK3	RCI CK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	 ALLOW PCIE Gen2 DEFAULT	 USE DEBUG STRAP	non_Fusion CLOCK MODE	ENADVED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	 FORCE PCIE Gen1	 IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKCEN DISABLED	SPIROM	S5 PLUS MODE ENABLED

DEBUG STRAPS

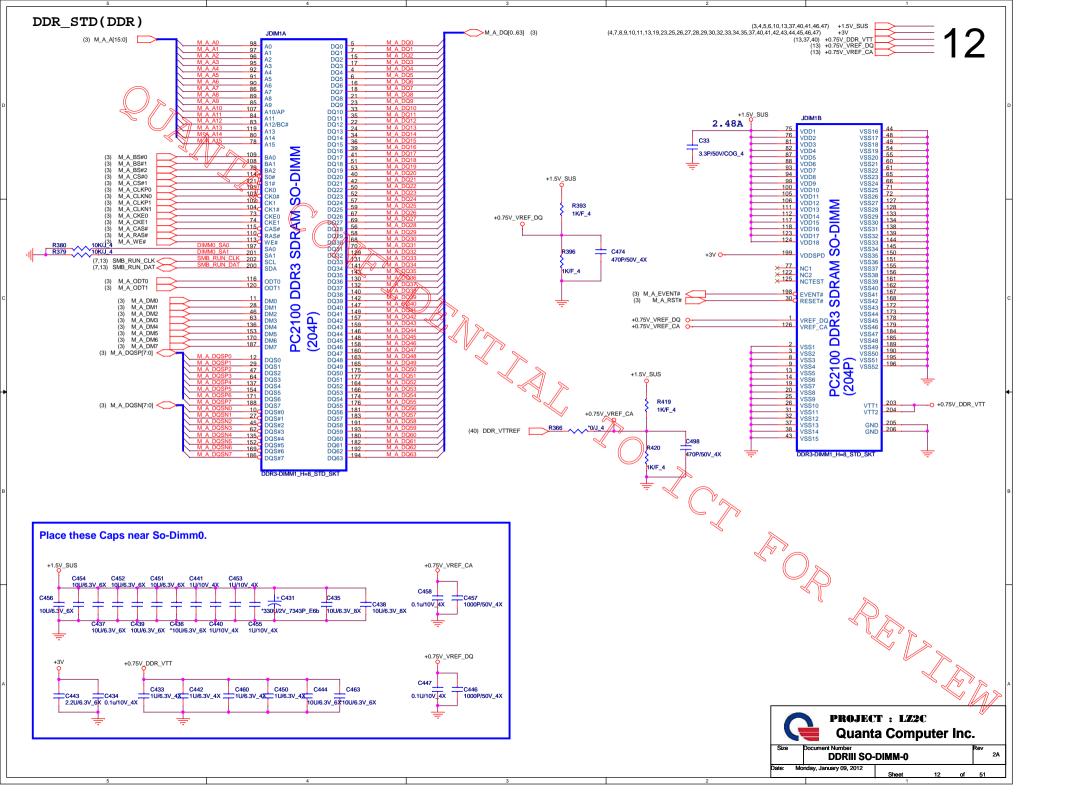
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

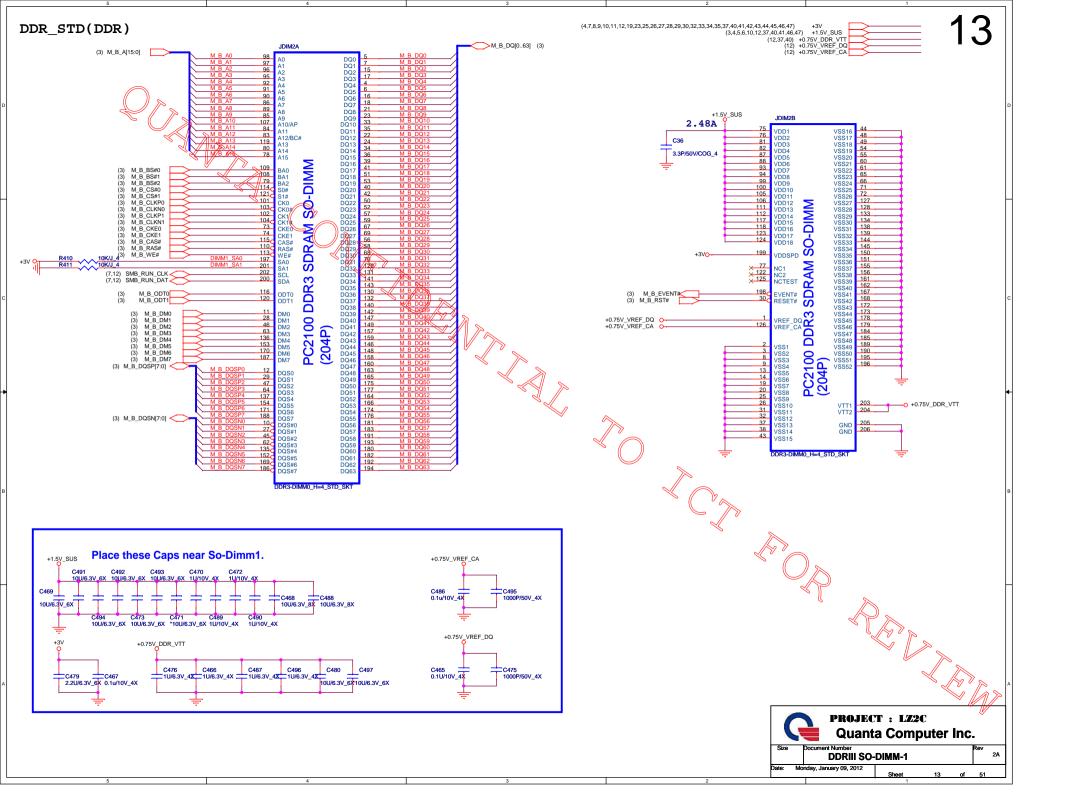


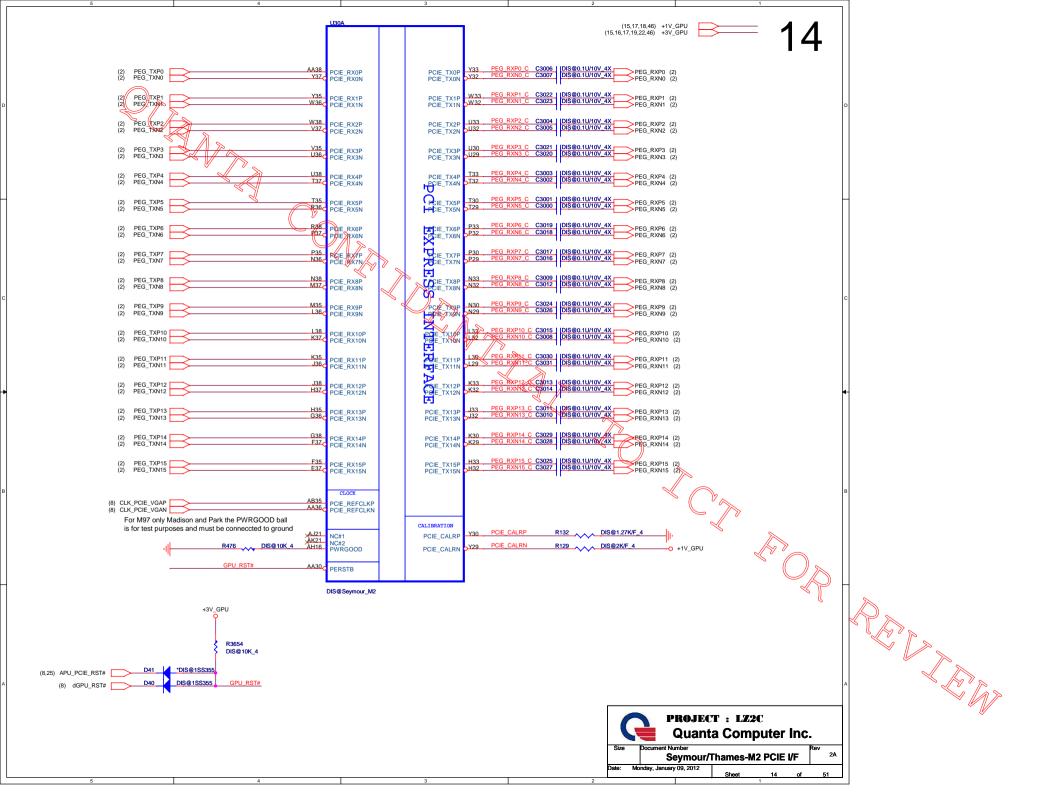
	PCI_AD27	PCI AD26	PCI_AD25	PCI_AD24	PCI_AD23	
PULL HIGH	USE PCI PLL	DISABLE LA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT	

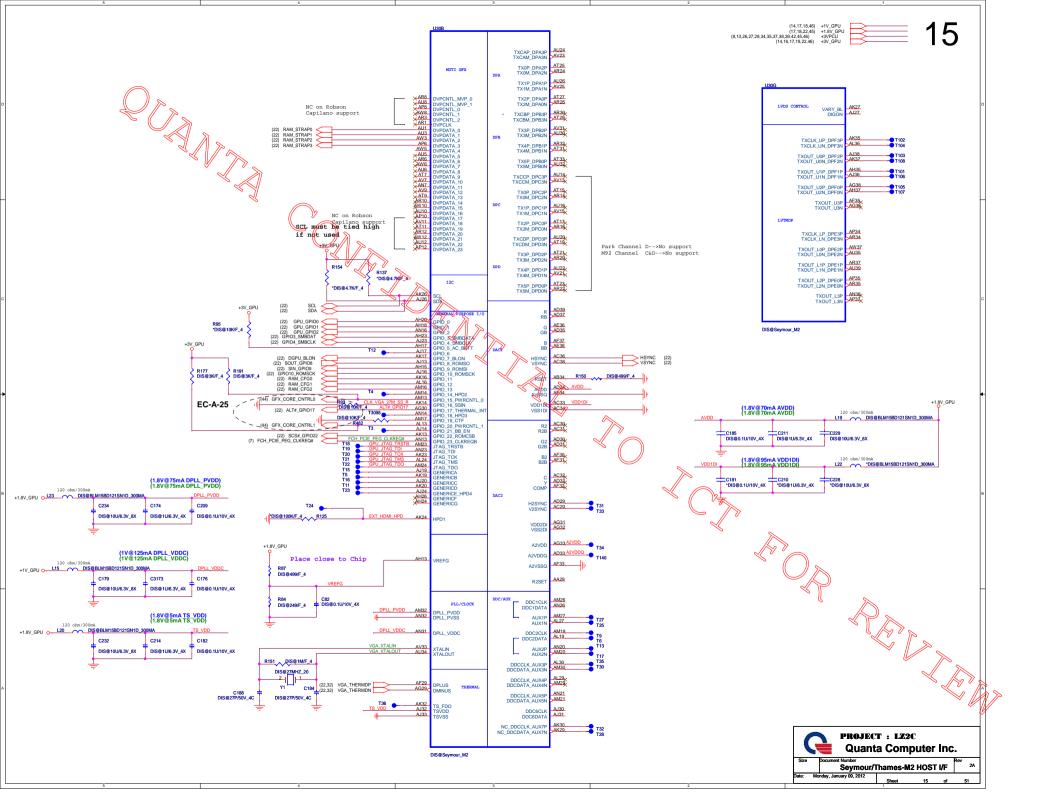
FCH PWRGD CKT

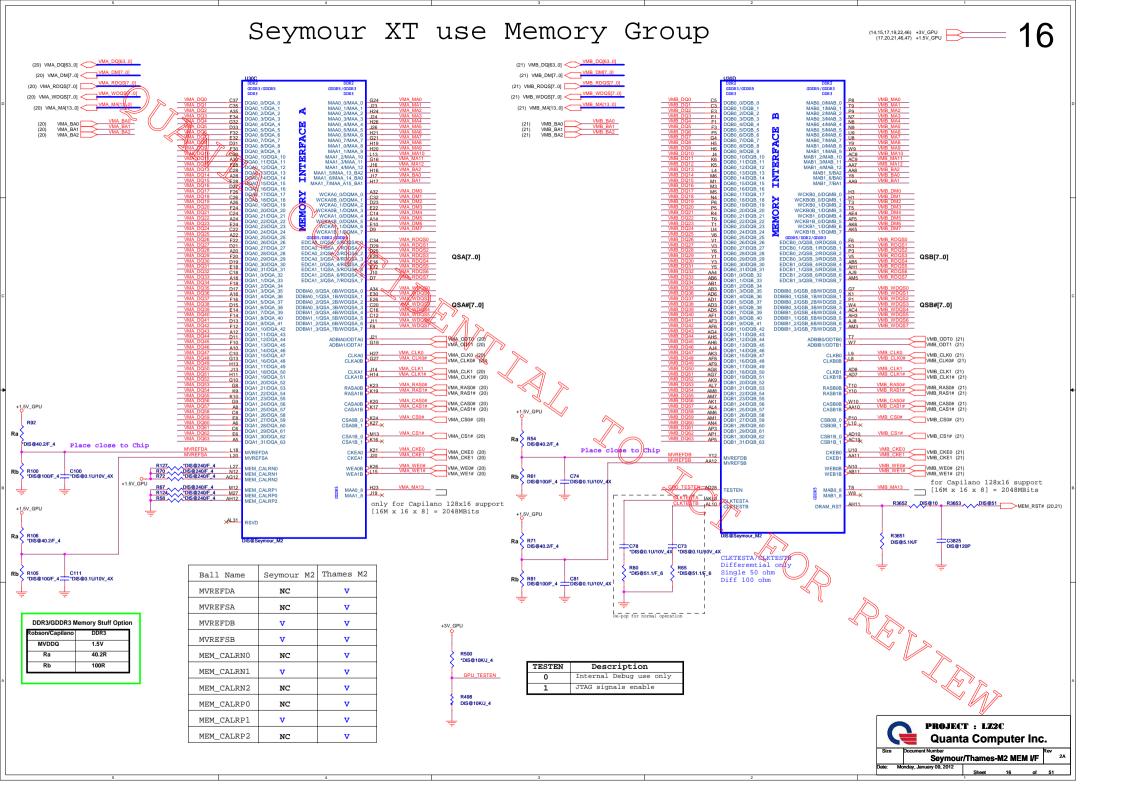


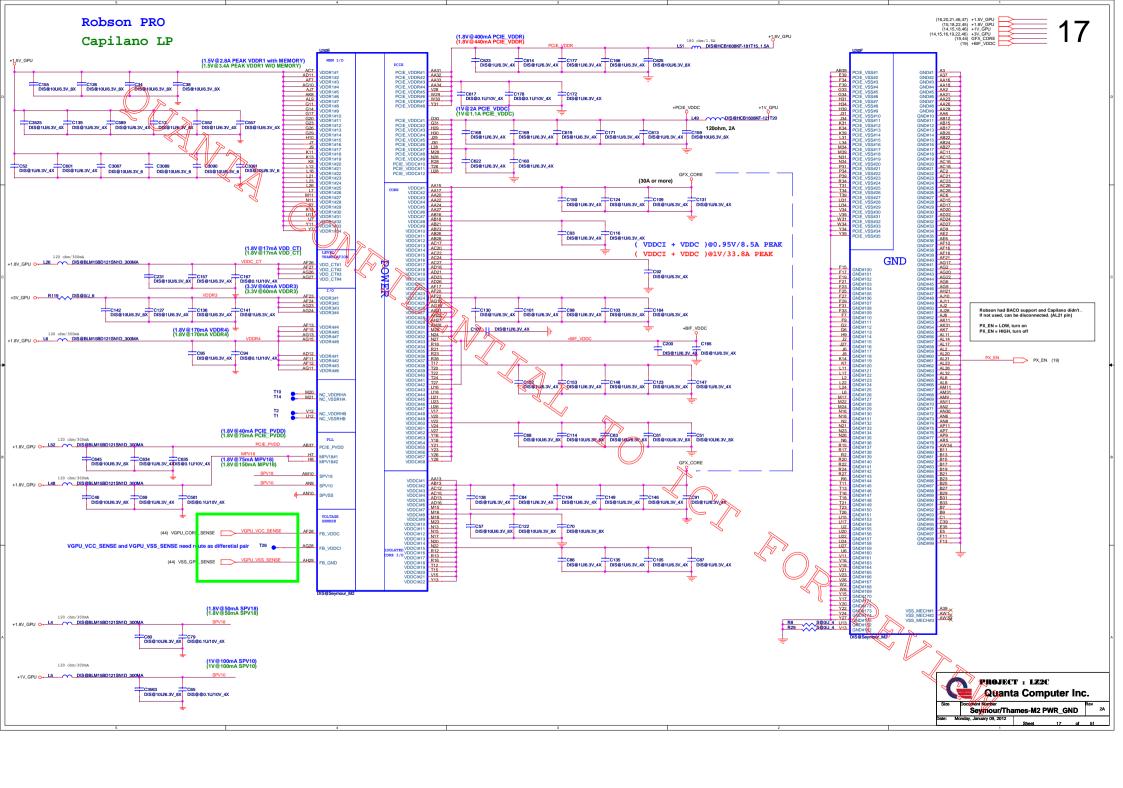


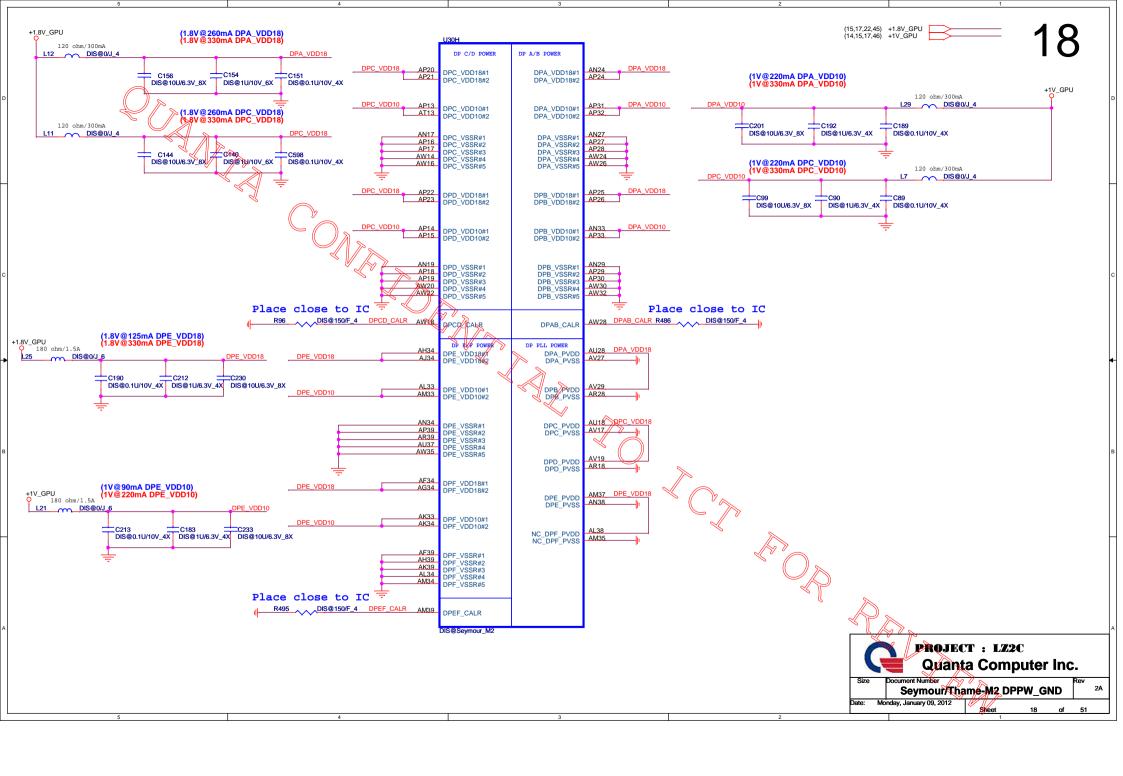


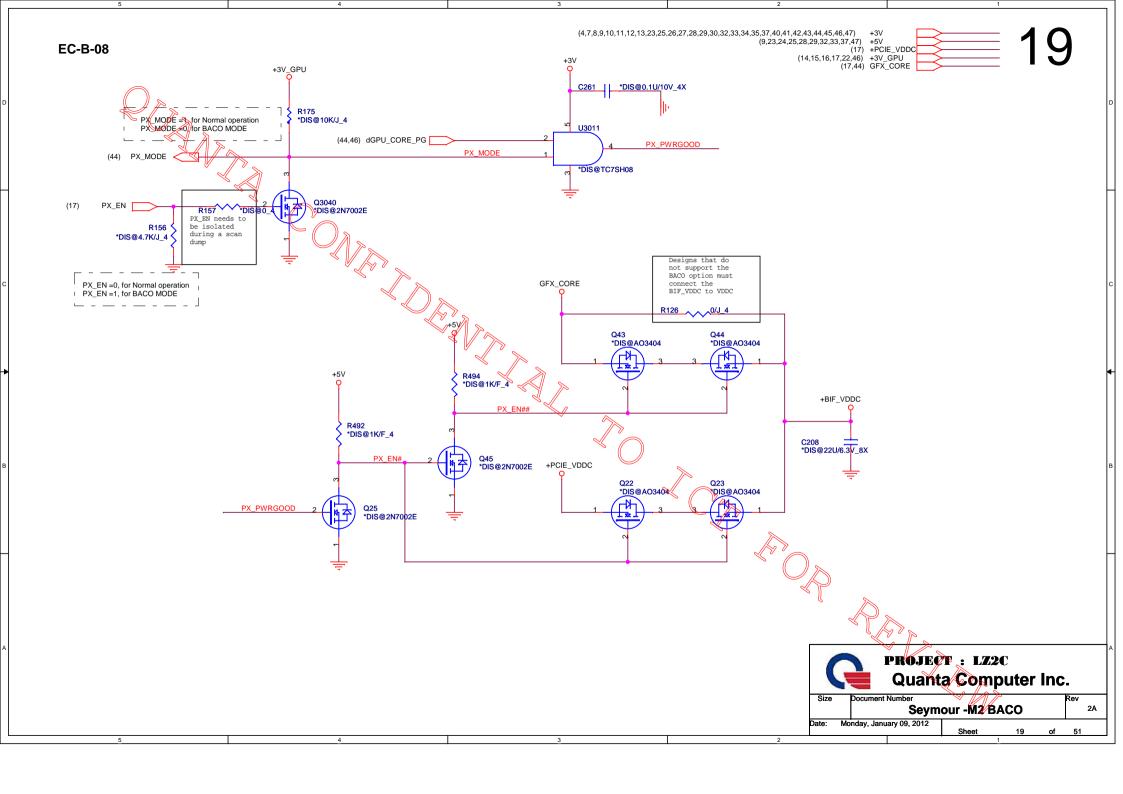


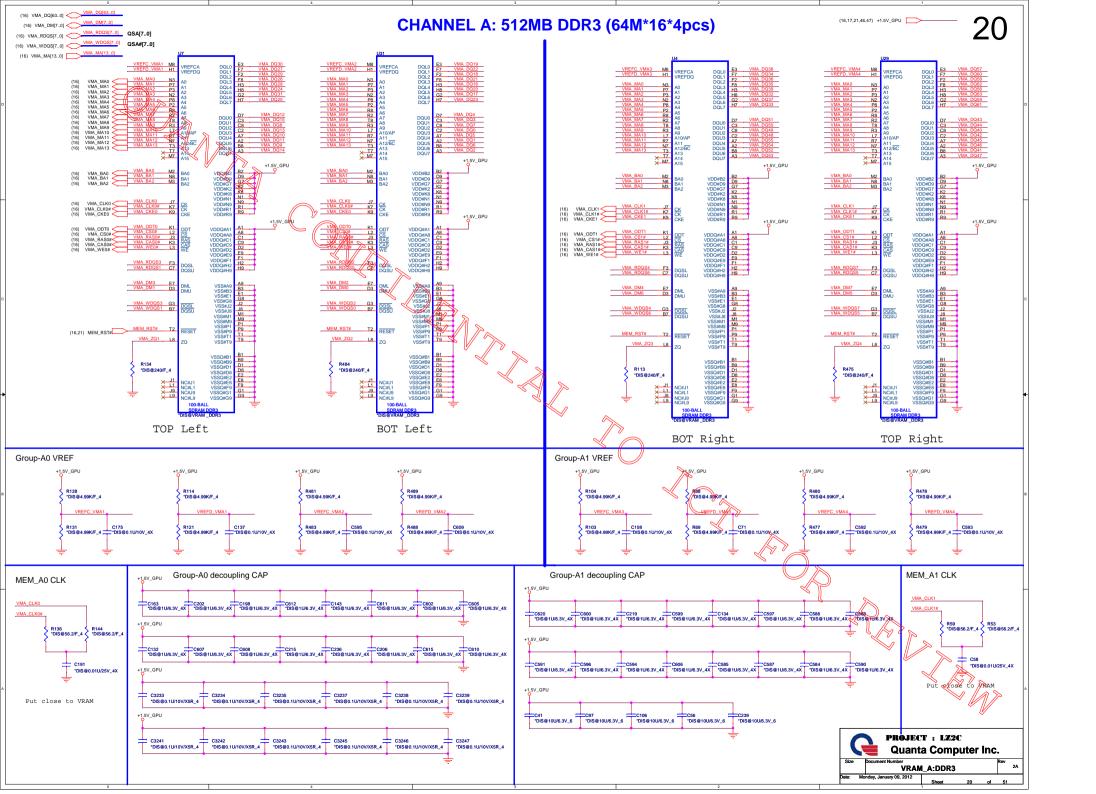


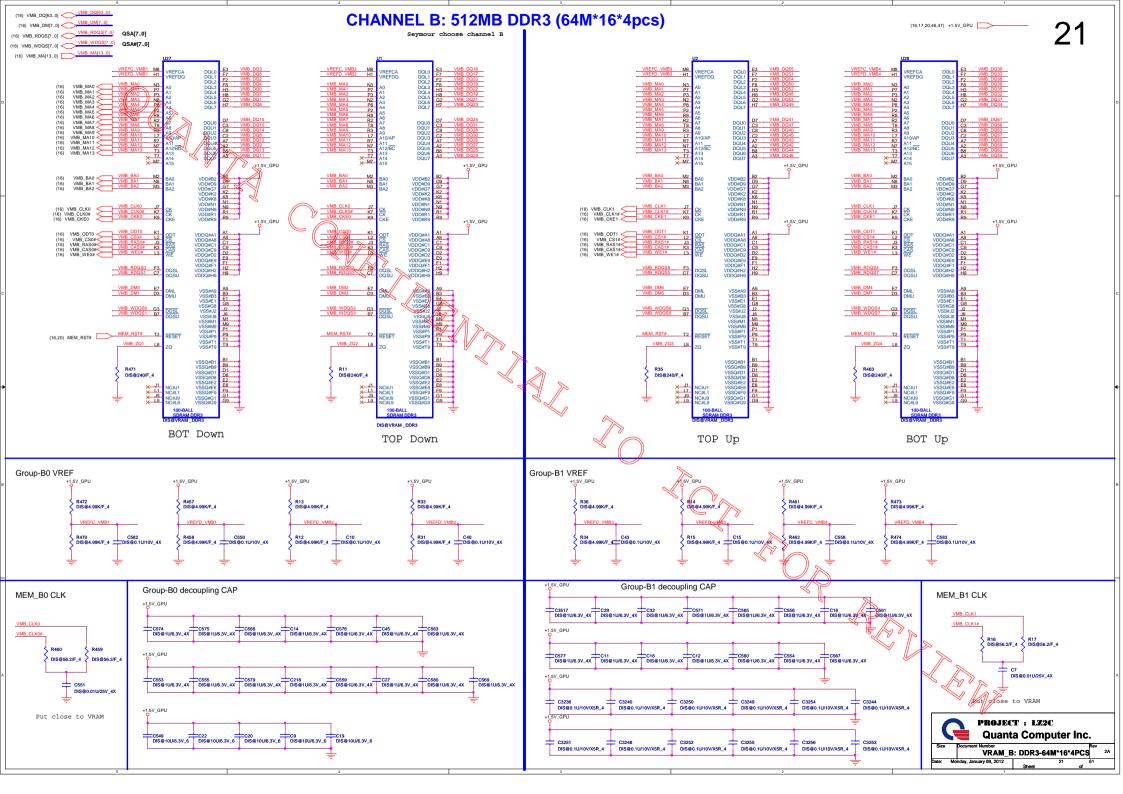


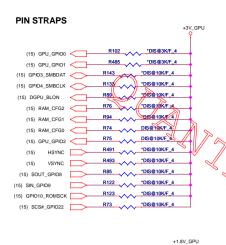












R57 *DIS@10K/F_4

R56 DIS@10K/F_4

R44 DIS@10K/F_4

R40 DIS@10K/F_4

R40 DIS@10K/F_4

R39 DIS@10K/F_4

(15) RAM_STRAP3

(15) RAM_STRAP2

(15) RAM_STRAP1

(15) RAM_STRAP0

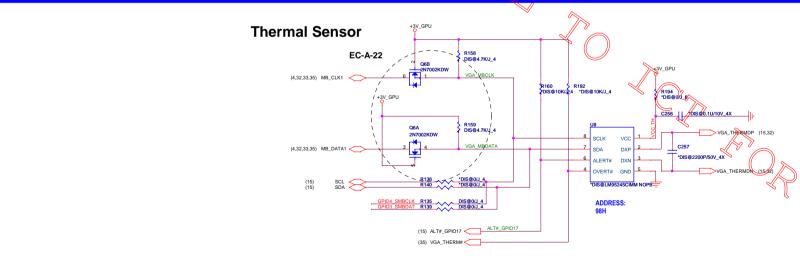
Memory Aperture size						
RAM_CFG[2:0]	Size					
000	128MB					
001	256MB					
010	64MB					
011	32MB					

ROM Table						
HSYNC	VSYNC	Discription				
0	0	No Audio				
0	1	Any one by dectec				
1	0	DP only				
1	1	Both DP & HDMI				

VRAM Memory TYPE

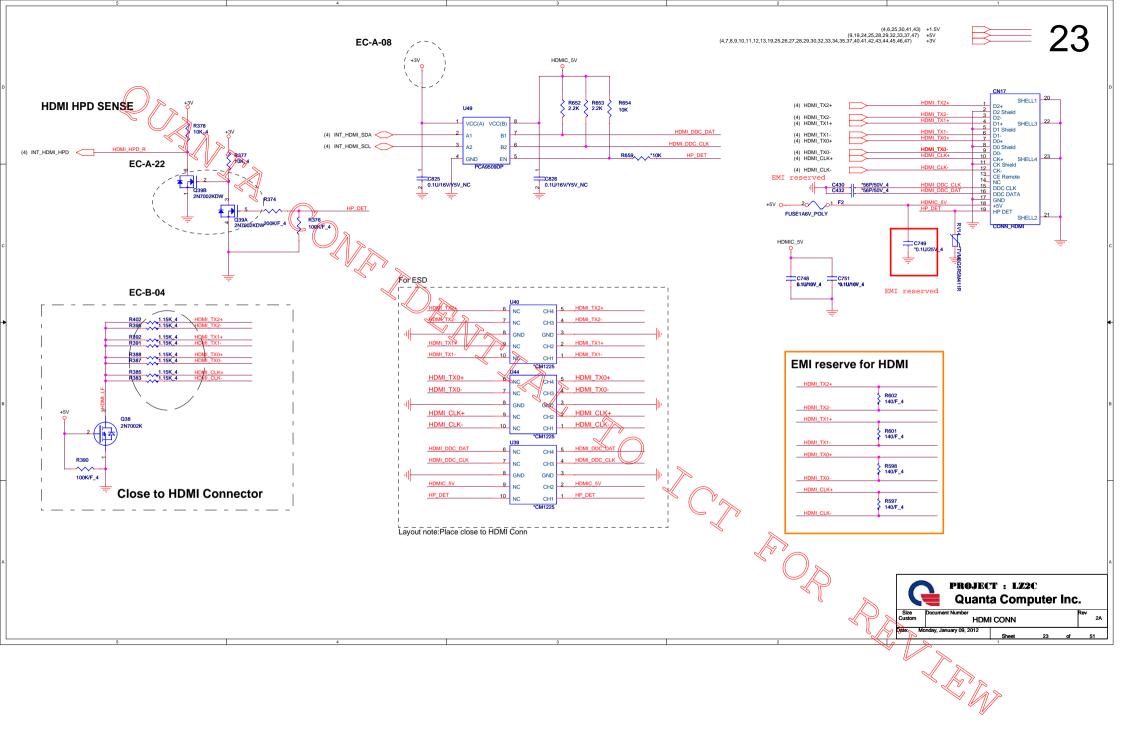
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	_	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
	H5TQ1G63DFR -11C	AKD5LZWTW02 (64M*16-1Gb)	1GB	0	0	1	0
Hynix	H5TQ2G63BFR -11C	AKD5MGWTW00 (128M*16-1GB)	2GB	0	0	0	0
	H5TQ2G63DFR -11C	AKD5MGWTW16 (128M*16-1Gb)	2GB	0 %	1	0	0
Samsung	K4W1G1646G -BC11	AKD5EGGT500 (64M*16-1Gb)	1GB		>> °	1	1
	K4W2G1646C -HC11	AKD5MGWT500 (128M*16-1Gb)	2GB	0	0	» 0	1

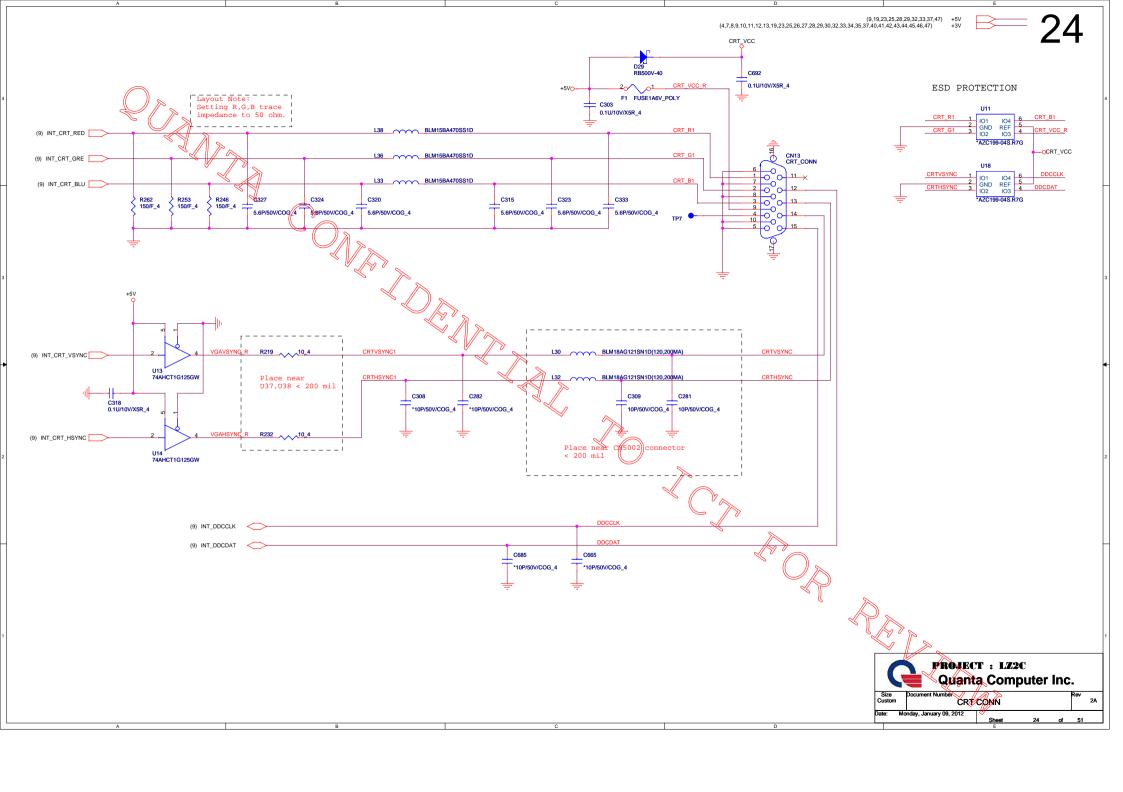
С				
ALLOW FOR PULLUP I				
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A: 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	1	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUDI: 0) 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

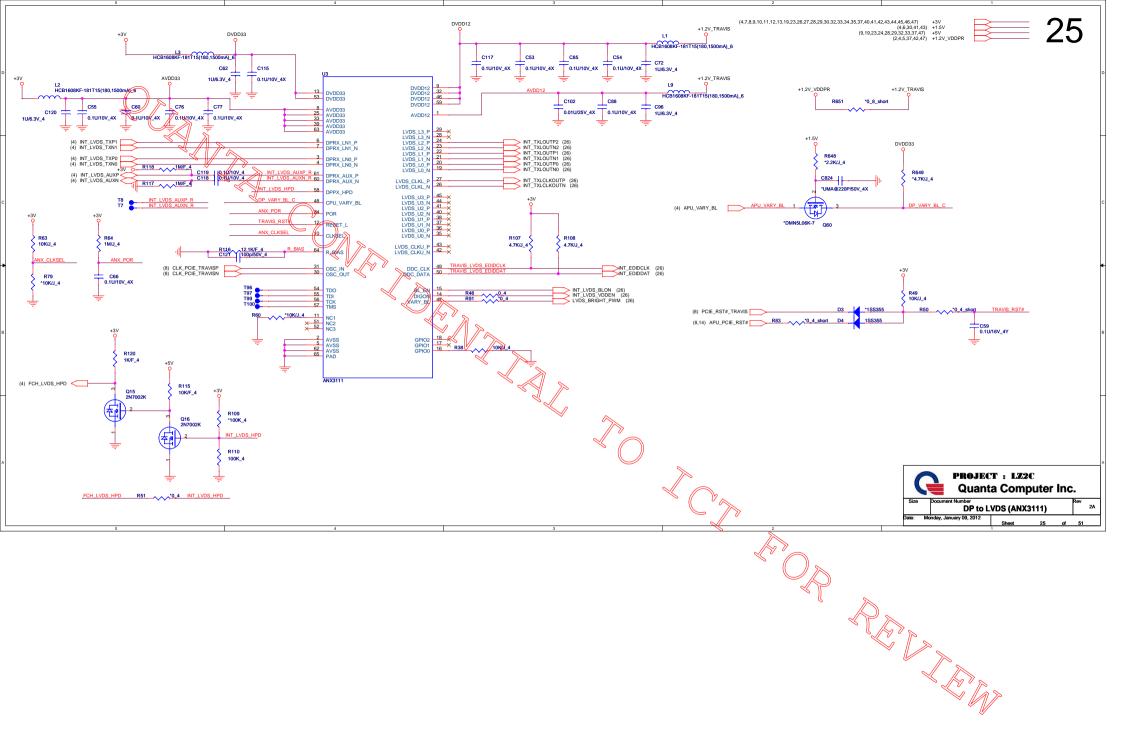


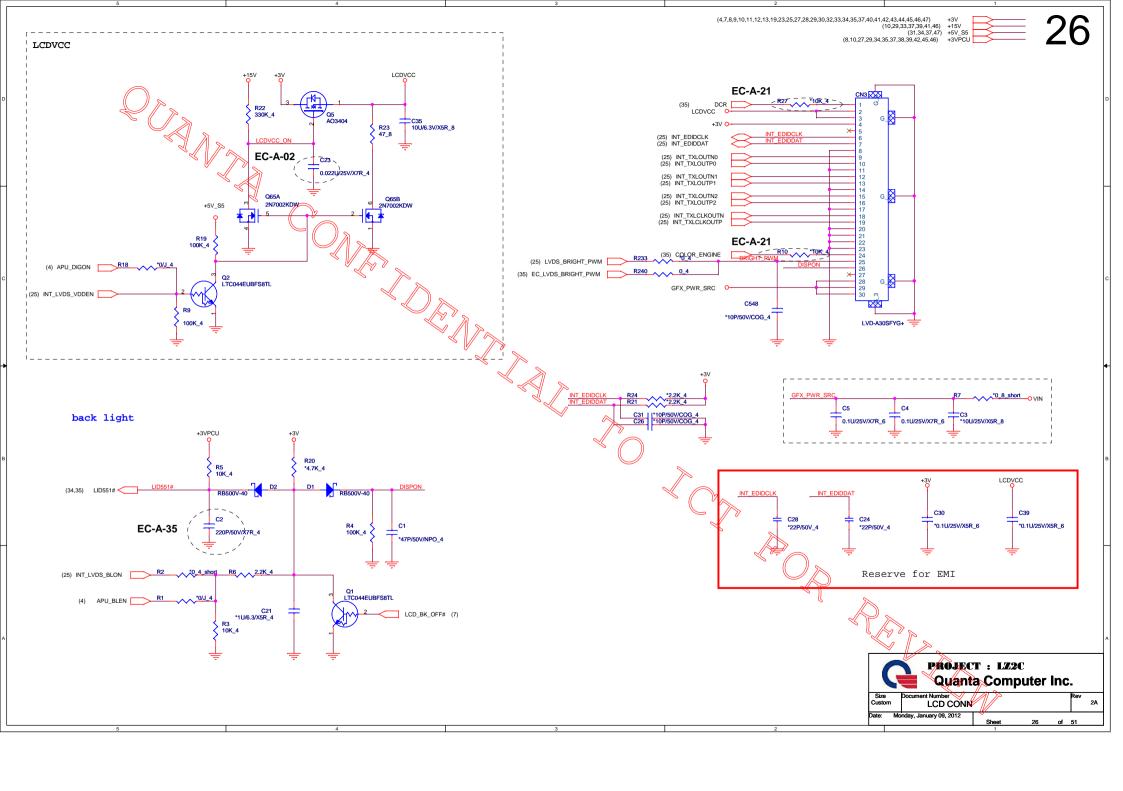
PROJECT : LZ2C
Quanta Computer Inc.

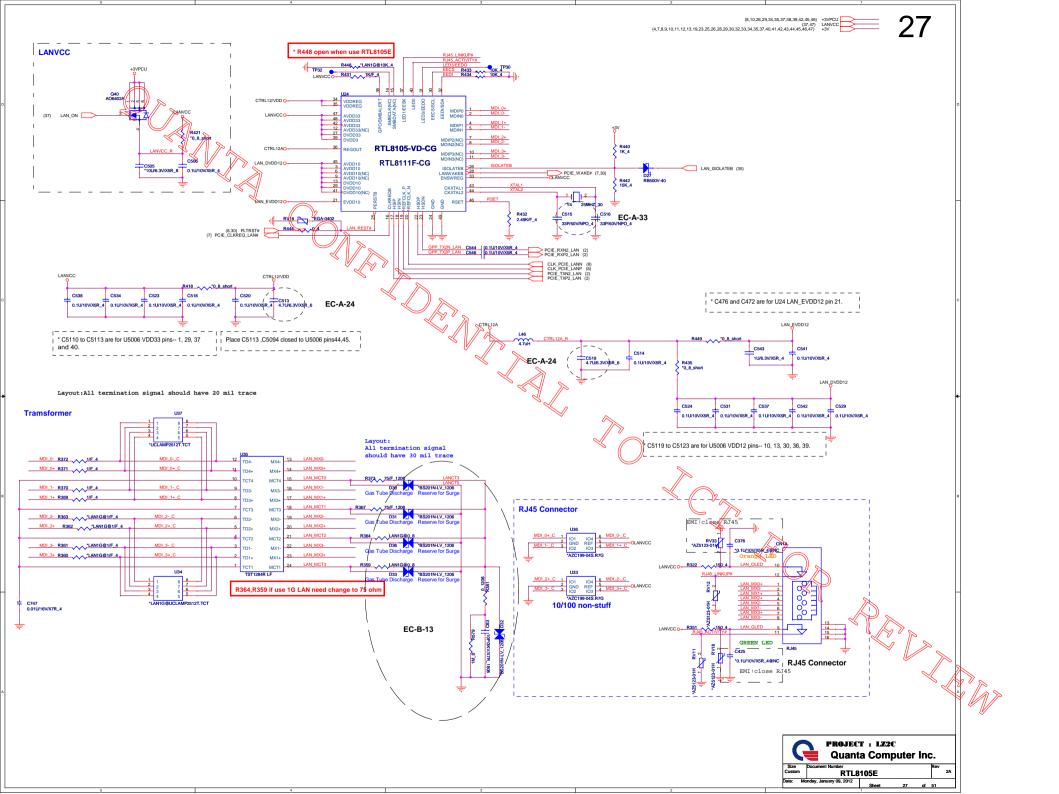
Size Downey Nayiber
Memory strip/Thermal
Date: Monday, January 09, 2017
Sheet 22 of 51

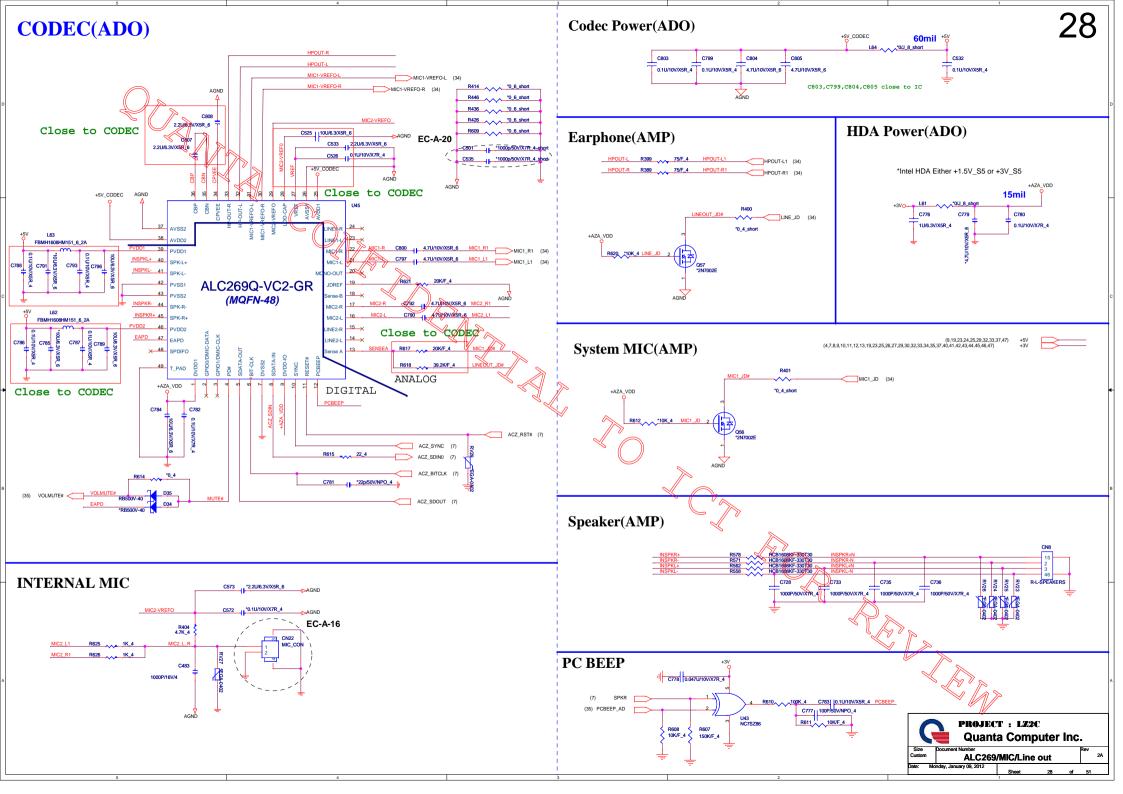


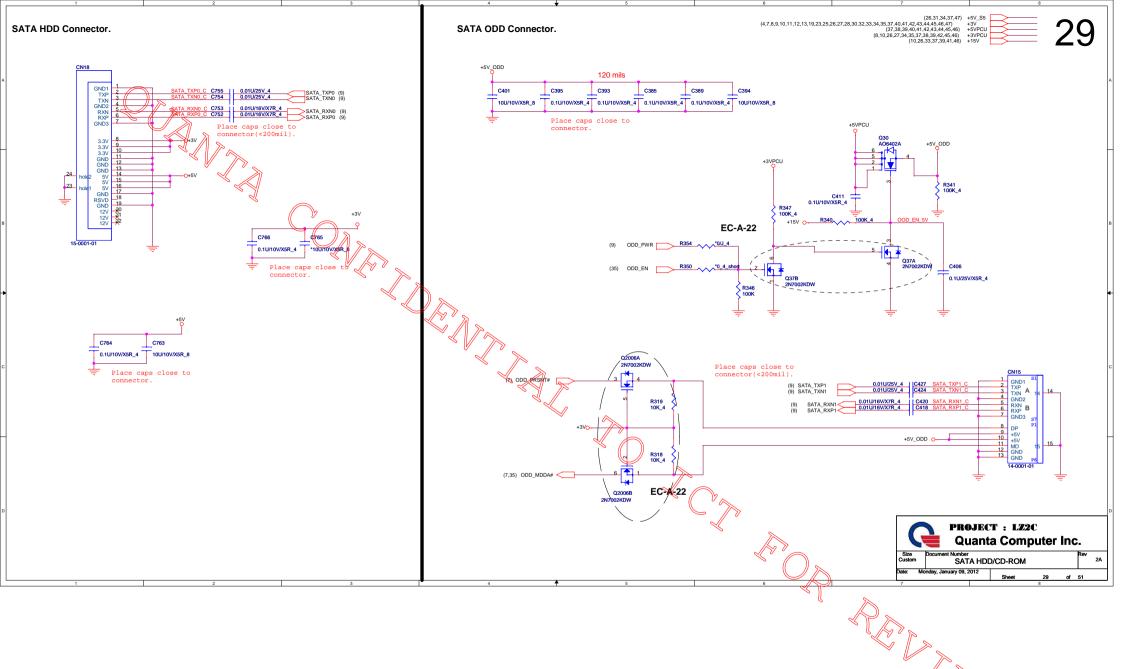


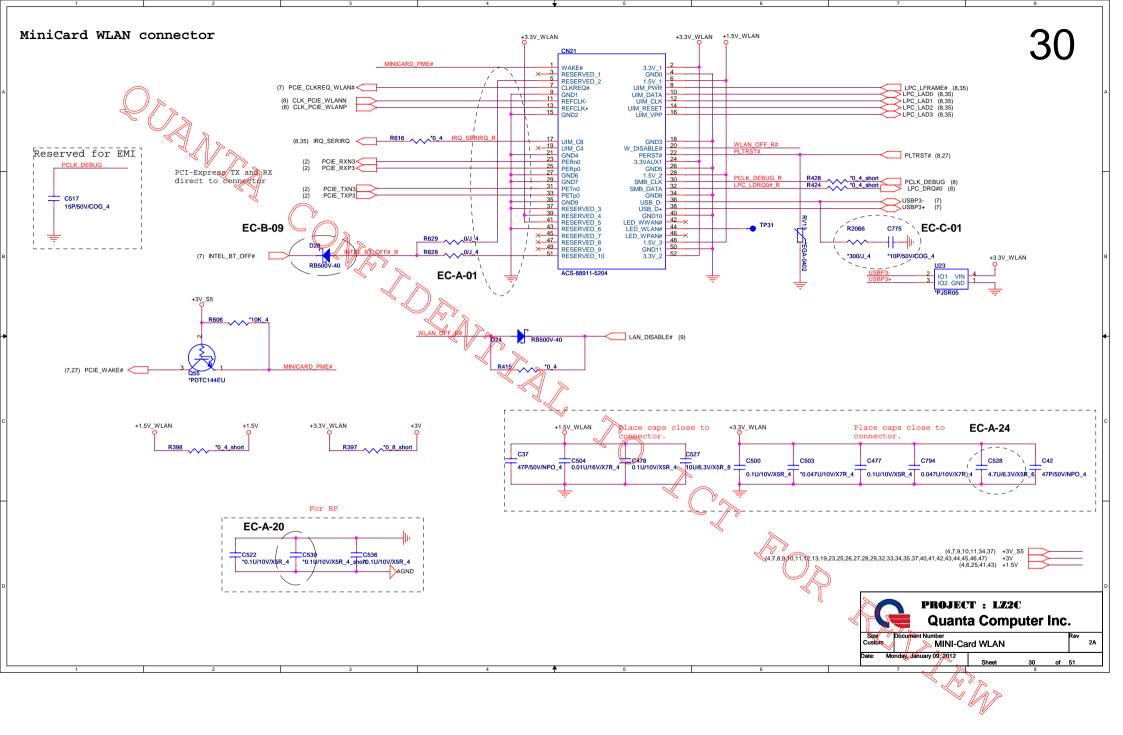


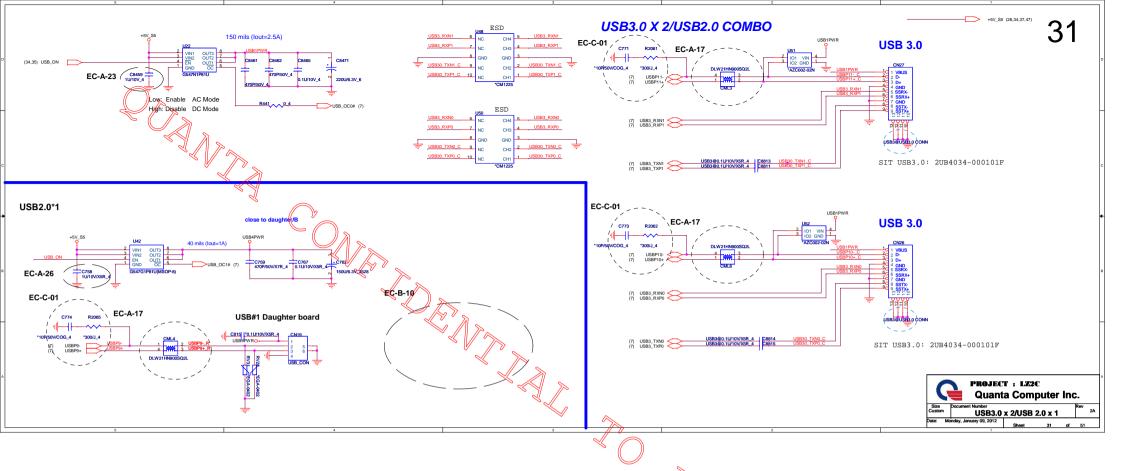


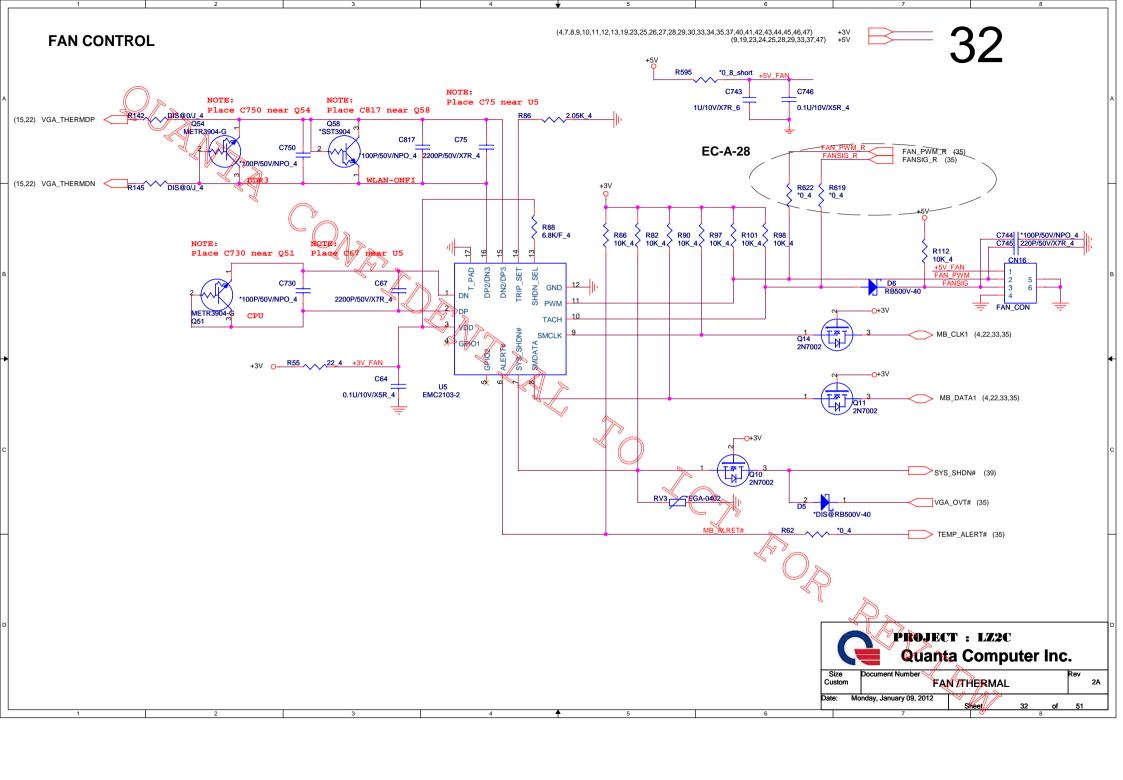


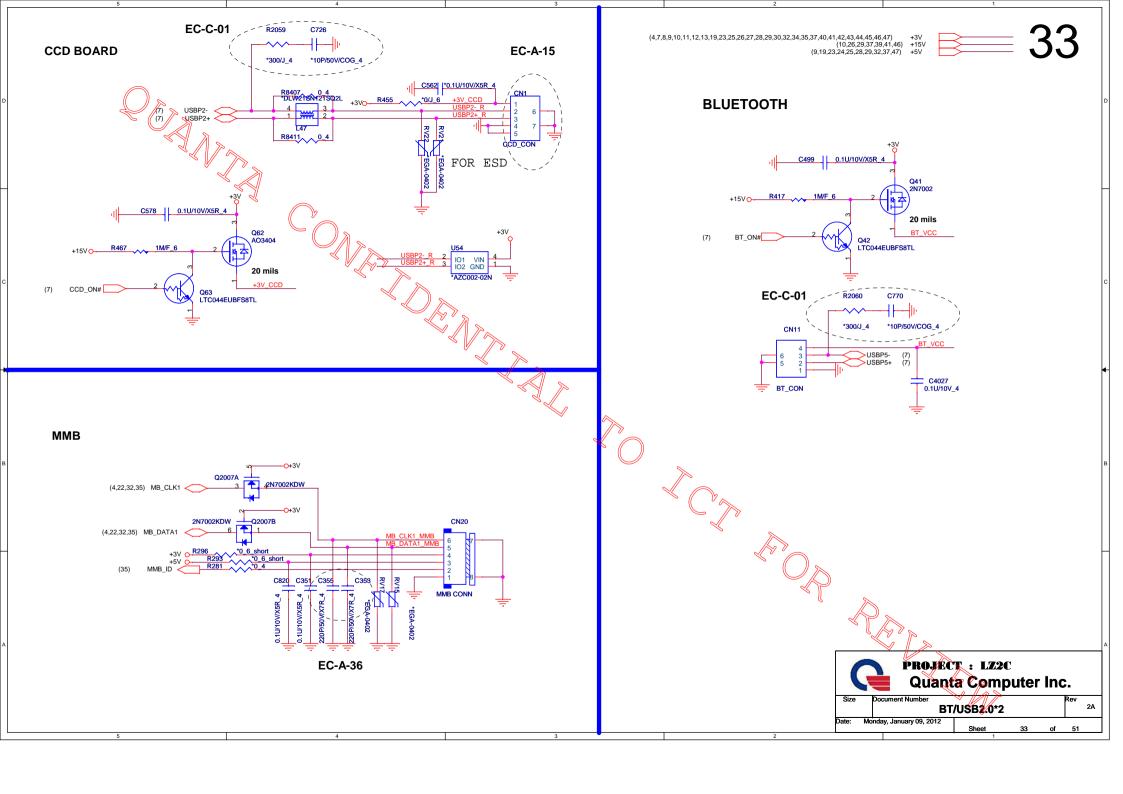


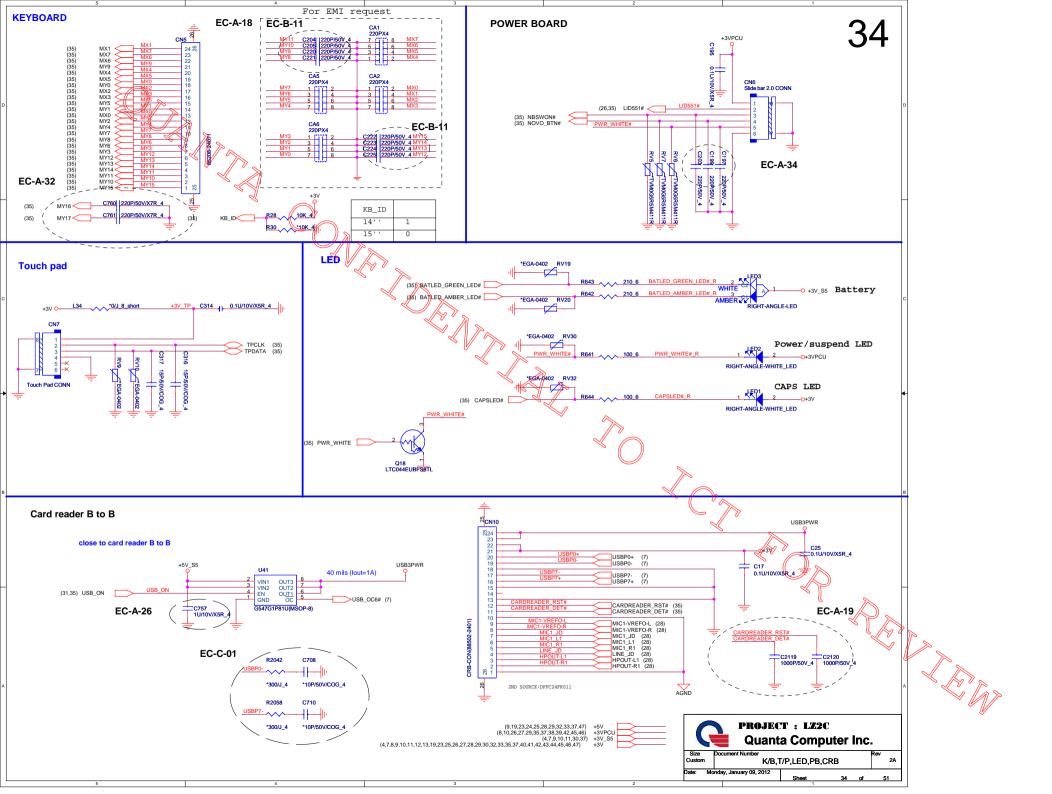


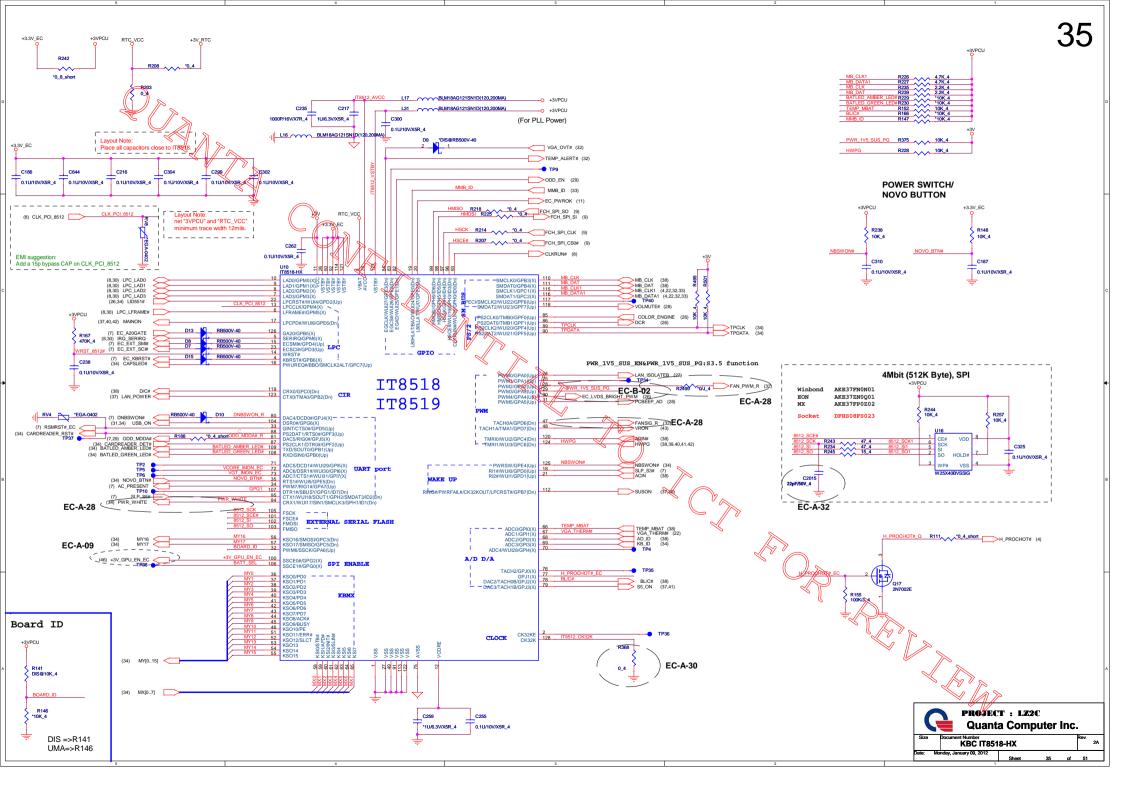


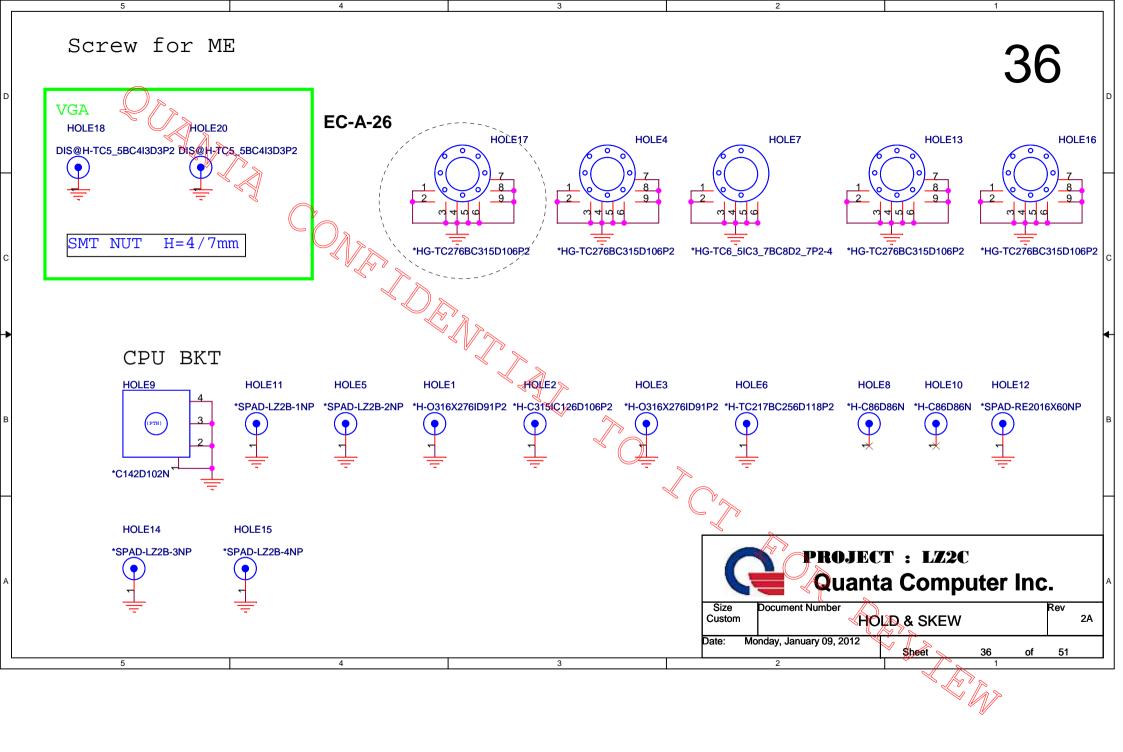


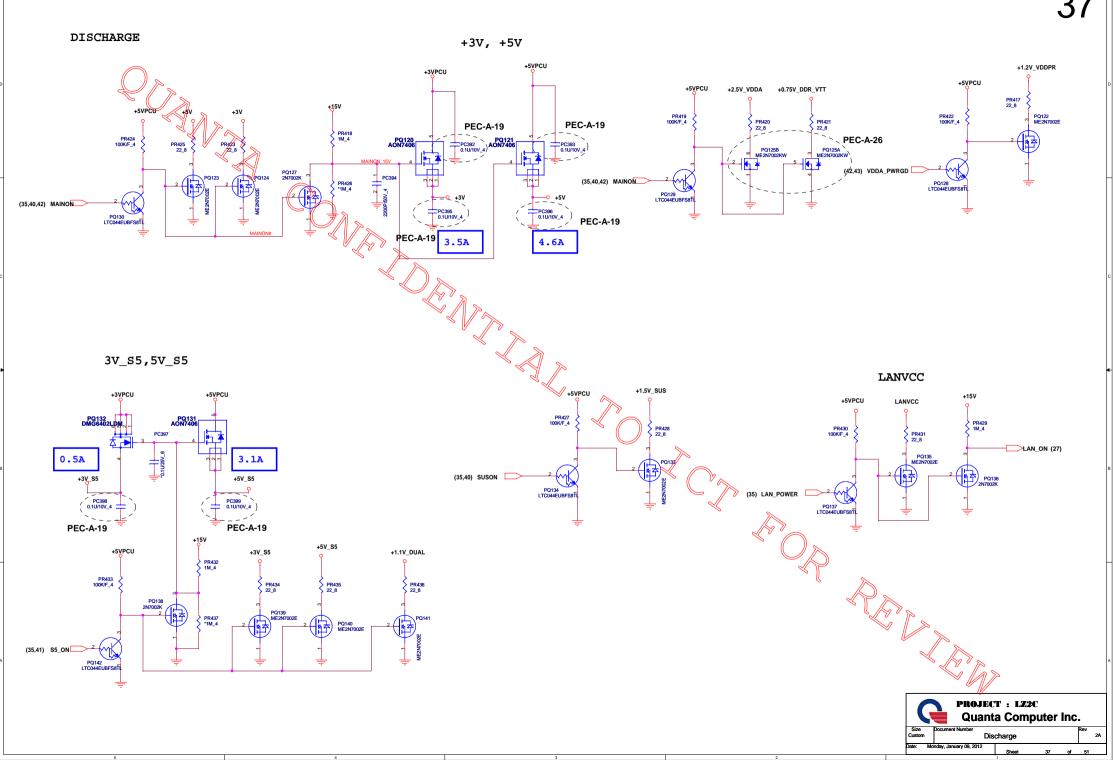


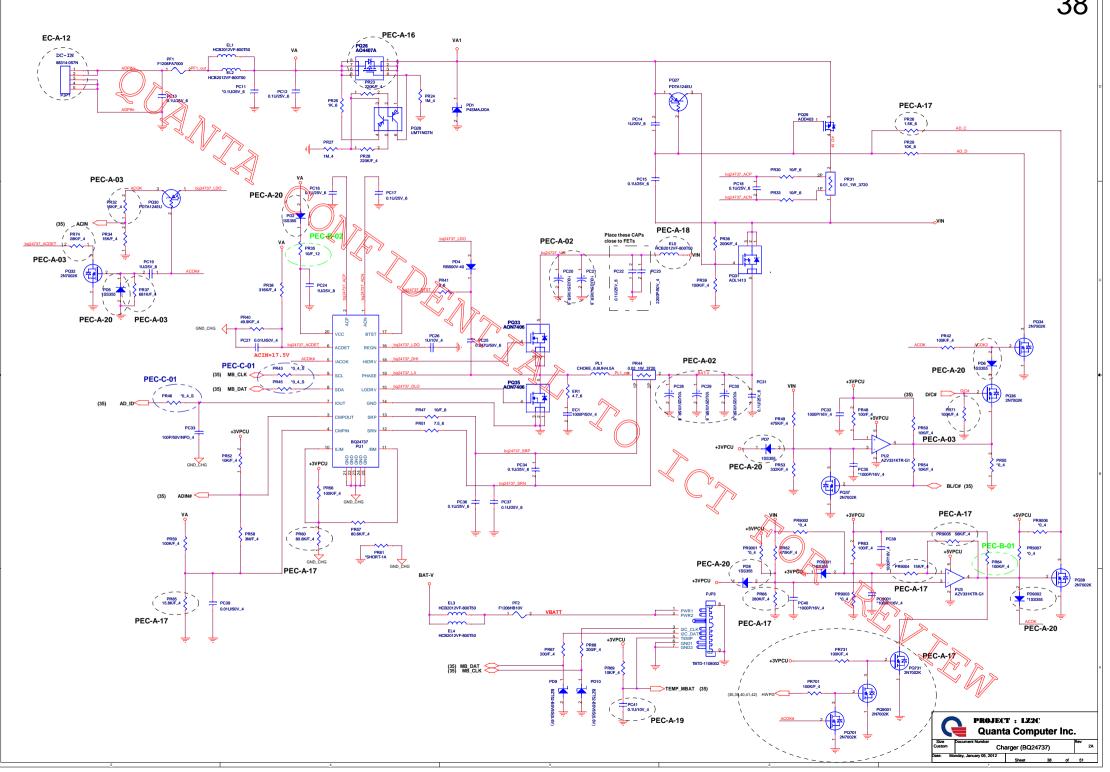


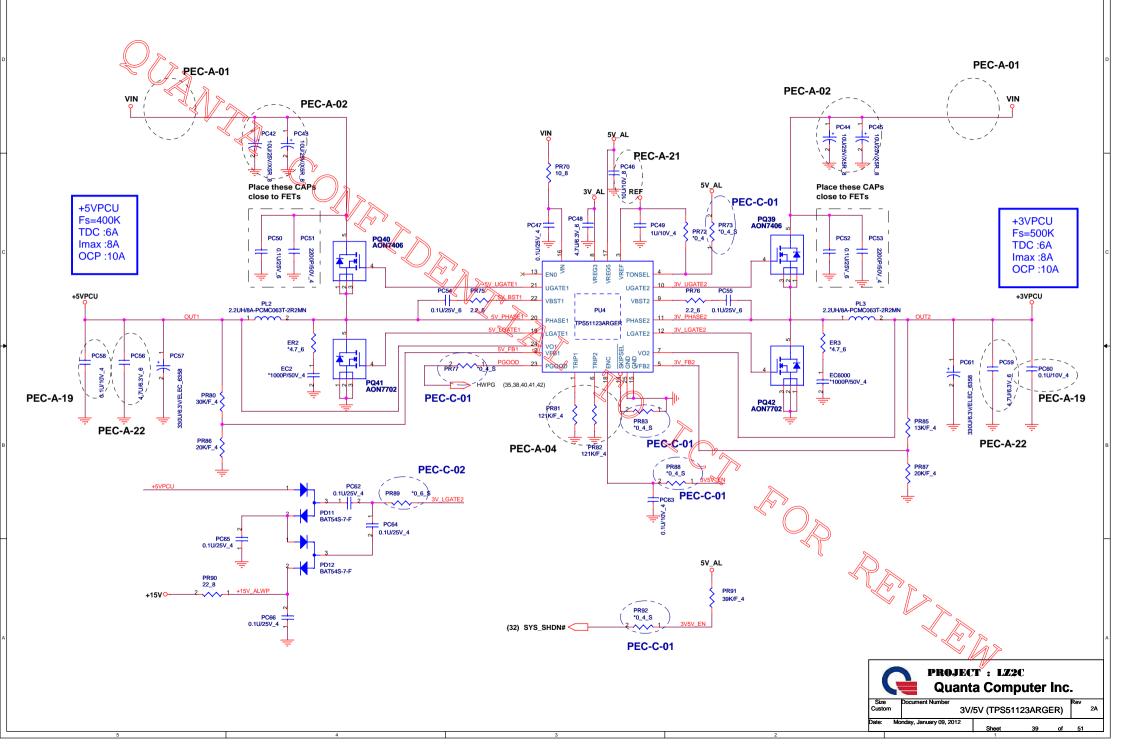


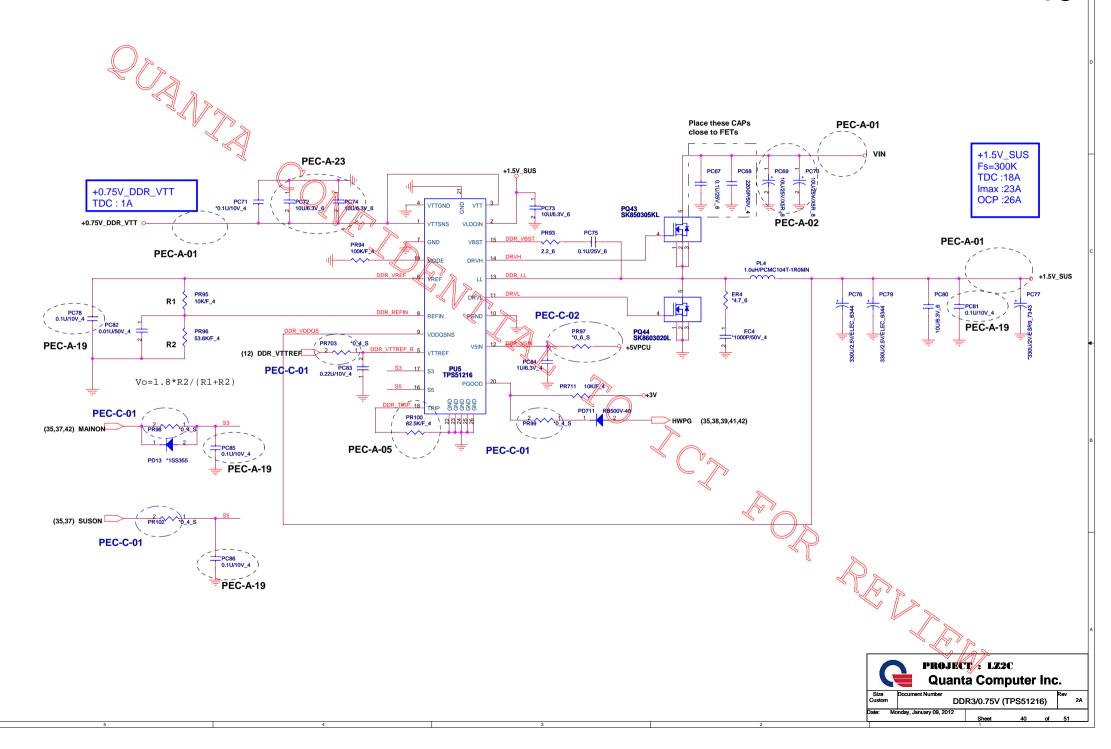


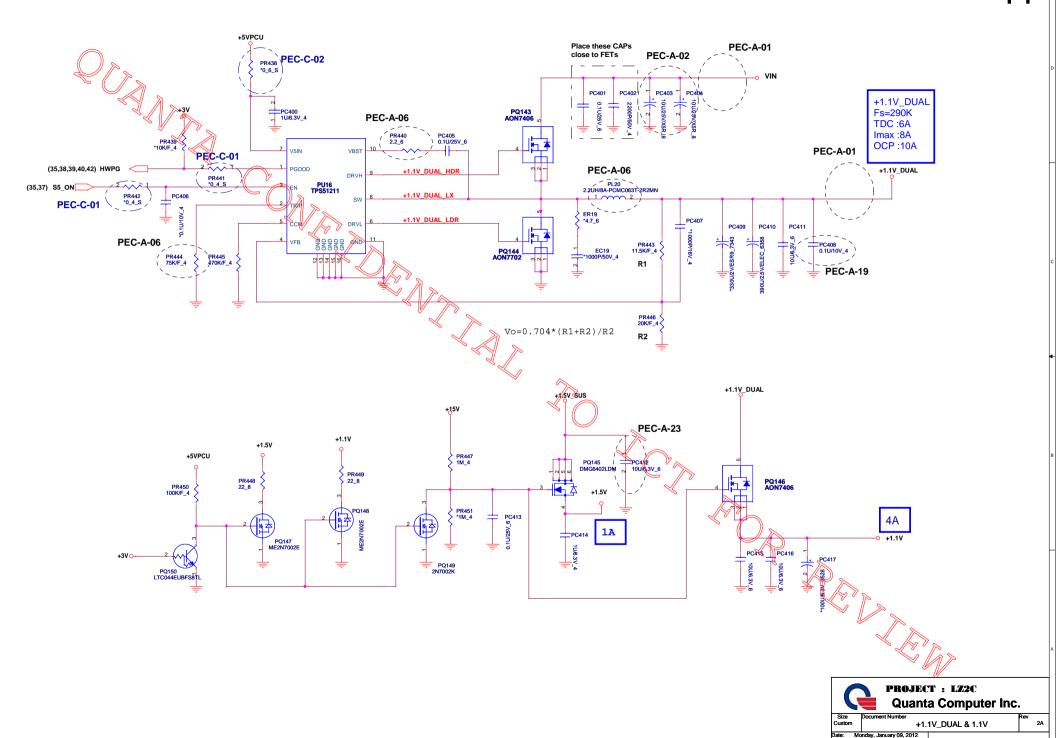


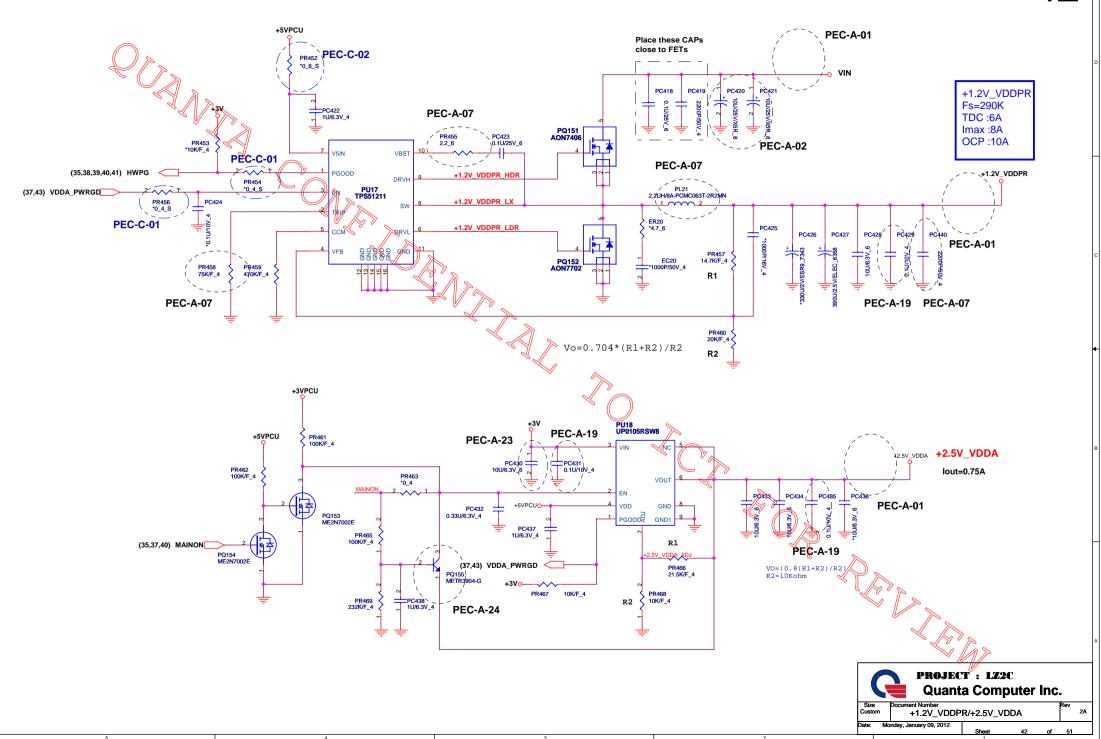


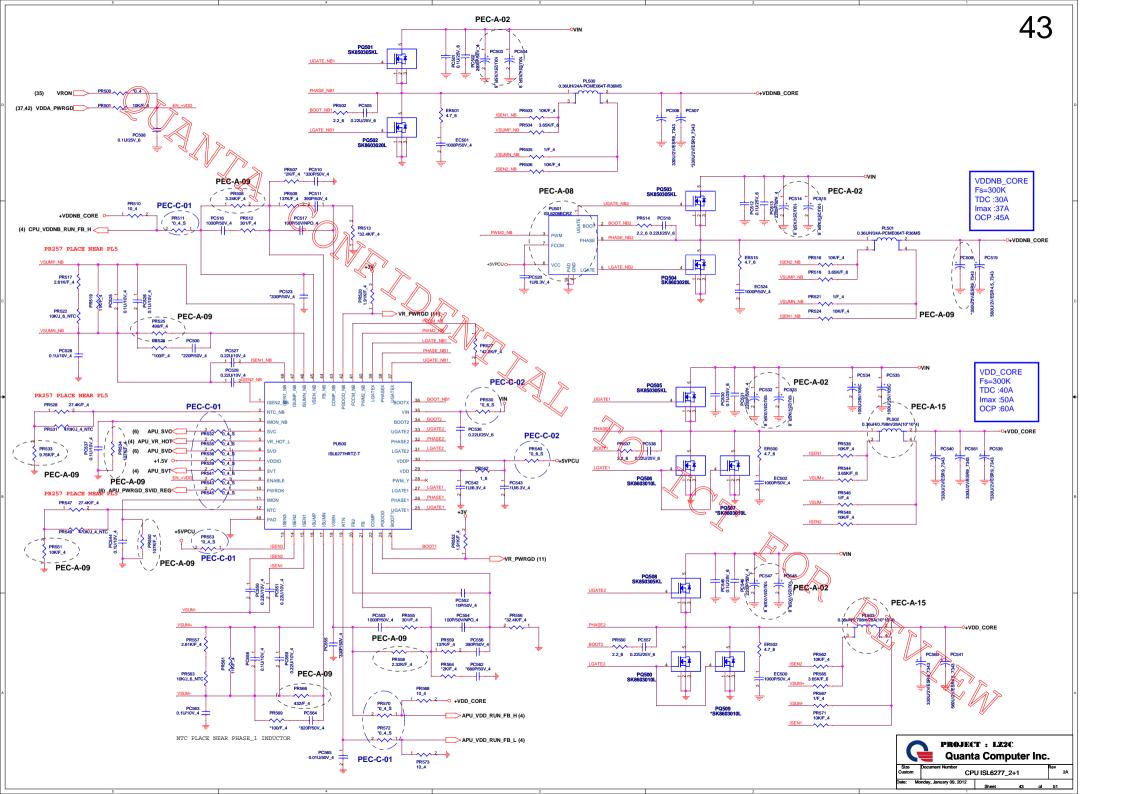


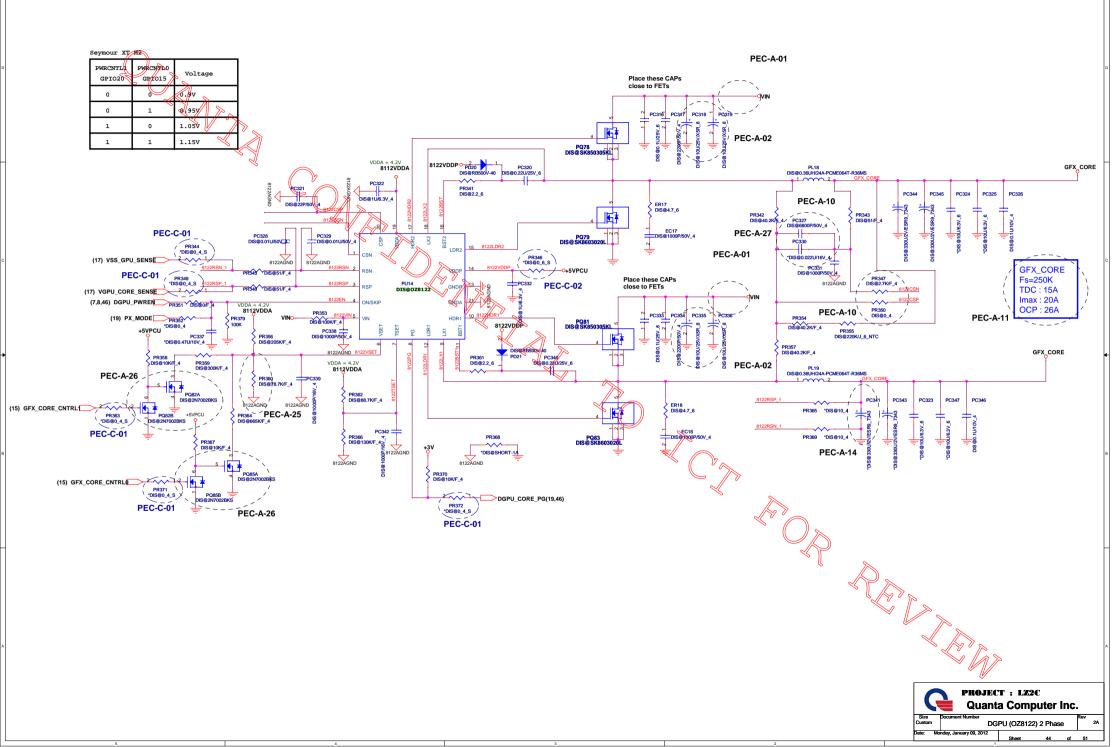


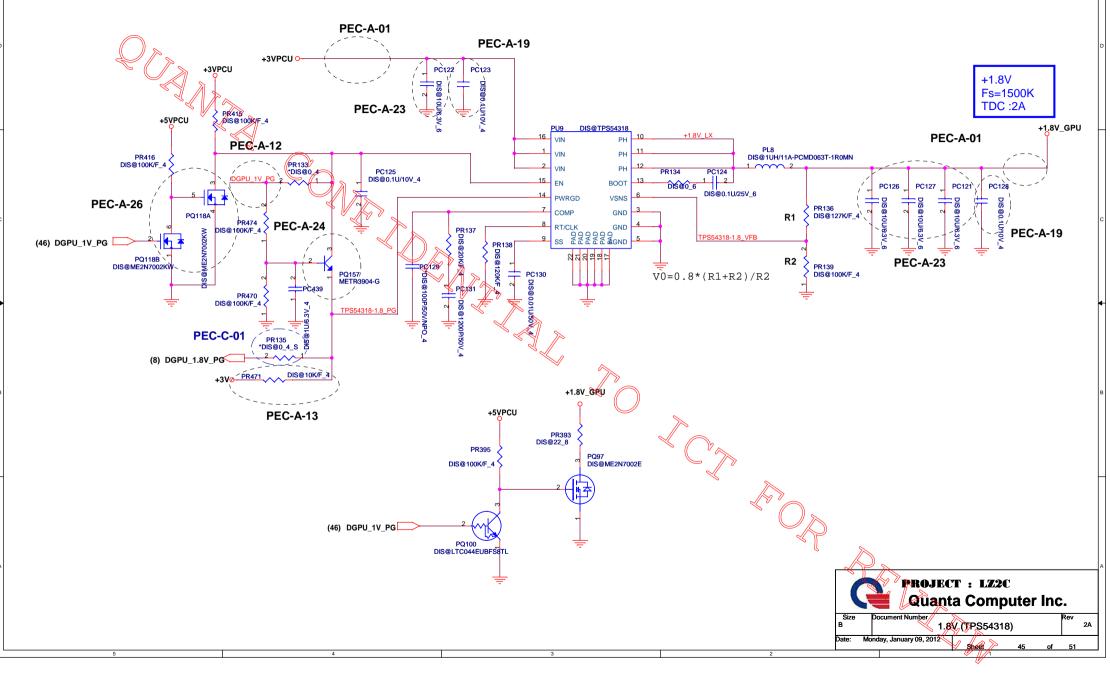


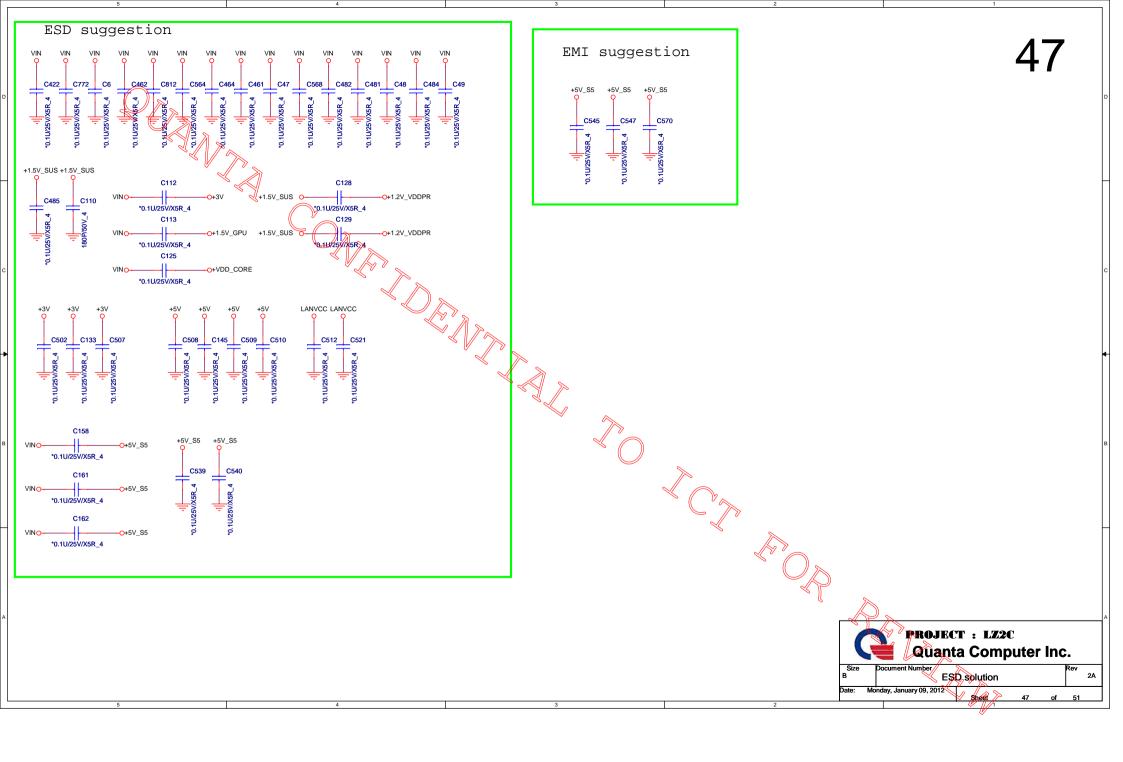












	EC NO.	ÞG.	DATE	PART REFERENCE	DESCRIPTION	48
2011	EC-A-01	30	08/23	CN21	Change connection form pin19 to pin 5 due to module choose as below #5: Liteon #53: Cyber TAN POP R628 & R629	
	EG-A-02	2 6	08/23	C23	C23 change from 0603 to 0402	
	EC-A-03	4,8	_{>} 08/23	U2001,U15	DELETE SOME TPS	
	EC-A-04	4	08/24	U2001	add pull high resistor R2053~R2057 for JTAG signals.	
S	EC-A-05	4	08/24	R2033	reserve R2033 for Test35	
>	EC-A-06	8	08/25	₹ 189	change R189 to 0 ohm	
Ü	EC-A-07	9	08/25	R280,R286,R292	pull up resistor from +3V to +3V_S5	
ဟ	EC-A-08	23	09/02	U49	U49.1 need connect to +3V to meet D.G.	_
	EC-A-09	35	09/06	U35 🗸	move net +3V_GPU_EN_EC to pin 100	
	EC-A-10	5	09/06	U2001	add C21/77 & C2116 & C2118 to improve +VDDNB_CORE ripple	_
	EC-A-11	7	09/06	U15	change port & and port 8 setting	
	EC-A-12	38	09/06	PJP1	change pin derine/for PUP1	
	EC-A-13	34	09/06	R28	Pop R28 for K/B ID setting	_
	EC-A-14	8	09/07	G3	Add short pad for RTC	
	EC-A-15	33	09/26	CN1	add pin5 for CN1	_
	EC-A-16	34	09/26	CN9	change CN9 footprint	
	EC-A-17	31	10/05	CML3/CML4/CML6/R8406 R8410/R8405/R8409/R8198 R8200	add CML4(CX21SQ2L000) and delete R8406/R8410 for EM request and CML3/4/6 change footprint to choke-dlw21s-4p add CML3&CML6(CX21SQ2L000) and delete R8405/R8409/R8198/R8200 for EMI request	
	EC-A-18	34	10/05	CA1~CA6	POP for EMI request	brack I
	EC-A-19	34	10/05	C2119,C2120	add C2119 for CARDREADER_DET# and C2120 for CARDREADER_RST# from EMPrequest	I
	EC-A-20	28 30	10/05	C501,C535 C530	change footprint to short pad from EMI request	
	5			4	PROJECT : LZ2C Quanta Compute Size Document Number Ecclist Date: Monday, January 09, 2012 A8	er Inc. Rev 2A of 51

EC pg.	DATE	PART REFERENCE	DESCRIPTION
C-A-21 26	10/05	R10/R27	Not support DCR & COLOR_ENGINE from customer request
C-A-22 23 29 29	10/05	Q19,Q20,Q6 Q34,Q35,Q39 Q31,Q36,Q37 >>Q27,Q28,Q2006	change to dual mosfet Q6 change to dual mosfet Q39 change to dual mosfet Q37 change to dual mosfet Q2006
C-A-23 31	10/05	C8459	C8459 change to 1uF/10V/0402
C-A-24 27 30	10/05	C513,C519 C528	change to 4.7uF/6.3V/0603
C-A-25 15	10/05	U30 🧪	shange GFX_CORE_CNTRL0/GFX_CORE_CNTRL1 for VBIOS setting
C-A-26 31 34	10/05	C758 C757	dhange to 1U/10V/X5R_4
C-A-27 36	10/06	hloe17	add hole to the second
C-A-28 32/35	10/06	R2498/R2499/R619/R622	reserve R2498/R2499/R619/R622 for EC control FAN
C-A-29 8	10/06	U15	change dGPU_1.8V_PG to GPIO46
C-A-30 35	10/06	R368	reserve for GPIO pin 🥢 \iint 🐆
C-A-31			
C-A-31			
C-A-32 34	10/07	C760,C761	POP for EMI request
C-A-32 35	10/7	C2015	Change from 220p to 22p, POP for EMI request
C-A-33 27	10/14	C515,C516	Change from 27p to 33p, vendor test result.
C-A-34 34	10/14	C197,C199,C203	Change from 1000p to 220p, POP for EMI request
C-A-35 26	10/18	C2	Change from 0.1U to 220p, POP for EMI request
C-A-36 33	10/14	C353,C355	Change from 10p to 220p, POP for EMI request
C-B-01 10	11/04	R343	change R343 to power rail from Vin to +15V
C-B-02 35	11/14	U10	reserve PWR_1V5_SUS_EN&PWR_1V5_SUS_PG:S3.5 funstion
C-B-03 04	11/18	R2496,R2497	pop for EC can read graphic temp.
C-B-04 23	11/18	R383,R385 R387,R388 R391,R392 R395,R402	tune resistor to meet AMD spec.
C-B-04 23	11/18	R387,R388 R391,R392	tune resistor to meet AMD spec.



EC NO.	PG.	DATE	DART REFERENCE	DESCRIPTION
EC-B-06	26	11/18	Q3,Q4,Q65,R23	Delete Q3,Q4 add Q65 and R23 change to 47 ohm
EC-B-07	8	11/18	R309,R312	change to 0 ohm due to non pci device.
EC-B-08	19	11/18		R126 pop & depop C208,C261,Q22,Q23,Q25,Q43,Q44,Q45,Q3040,R156,R157,R175,R492,R494,U3011 for PX5 implement
EC-B-09	30 🔇	1/2/06	D28	reserve to prevent leakage
EC-B-10	31	12/06	1 053	remove
EC-B-11	34	12/06	CA3/CA4/C204/C205 C220/C221/C222 C223/C224/C225	CA3,CA4 change to 0402*8(C204,C205,C220,C221,C222,C223,C224,C225)
EC-B-12	7	12/06	R527	reserve for dgpu_pwr_en
EC-B-13	27	12/06		Reserve for Surge Line to GND Gas Tube Discharge
EC-C-01	30 31 33 34	01/03	R2066,C775 R2065,C774 R2061,C771 R2062,C773 R2059,C726 R2060,C770 R2042,C708 R2058,C710	Add resistor(3000bm) and CAP(10PF) to meet AMD spec.

	PROJECT : LZ3C Quanta Computer Inc).	
Size Custom	Document Number EG/list-3	Rev	2A
Date: Mo	onday, January 09, 2012 Sheet 50 of	51	

		EC	DG. DA	JE DART	· •	DESCRIPTION	50
The color of the	2011	NO.	38.39.	D ID4 D ID5 D ID6	NCE		
The content of the		EC-A-01	40,41, 09/2 42	21 PJP33,PJP8,PJP9 PJP33,PJP34,PJ PJP36,PJP26,PJ PJP16,PJP17.PJ	UP35, UP29, UP31	Change open paid to short pad.	
The column The			38,39,	PC30.PC42.PC4	43.PC44.		
Section Sect	≥	EC-A-02	40,41, 43,44	22 PC404 PC420 P	PC421.	Change MLCC 10UF size from 1206 to 0805.	
March Marc	₹			PC532,PC533,P PC548,PC318,P	PC547, PC319,		
March Marc	Ö	EC-A-03	38 09/2			udjust AC plug-in detect function.	
Section Text					// F	R8Z-PR82 change from 140K to 121K for 3V/5V OCP.	
From 2							
From 2		EC-A-06	41 09/2	PR440,PR444	4,PL20	200 Acquire promise the Control of Link_DAUL COPY. Add Octable from 0.2 Down to 2.2 Down for improve ringing voltage. L20 change from 1/4 to 2.2 Dot for improve ripple.	
No. 10 1 1 1 1 1 1 1 1 1		EC-A-07	42 09/3	PR455,PR458	8,PL21,	R458 change from 100k te/5K fo/C 1V_DAUL OCP. R455 change from 0 gray/to 2.2 chm or improve ringing voltage.	
No. 10 1 1 1 1 1 1 1 1 1					a la	Les trainings mont un payez-dust for improva papes. del PC4do 200P cag fur improva papes. del PC4do 200P cag fur improva papes. honos DIRIOI délaur l'C sina prova page 1/3 to 2/2	
Person 1	1			PR508,PR525,PF PR534,PR551,PF	PR533, PR550,		
Test					_		}
Section Sect				PC327,PR350	i0 ′		
Section 2	Ī	PEC-A-12	45 09/	08 PU9		Change from MAINON to DGPU_1V_PG	
Fig. 2 1	- 1	EC-A-14	44 09/	26 PC341	R	reduce 1pcs GFX core 7343 size output Cap for ATI Seymojr XT(15w).	}
Part	i	EC-A-15	43 09/	26 PL502,PL503			
Proceedings	1			PQ701 PR701 P	PQ731.		
Miles 10 10 10 10 10 10 10 1	L			/29 EL5	а		
Mark			37,38,				
1		ľ	41,42,	PC85,PC58,PC76 PC359,PC353,PC	398,PC395 78,PC86 PC128	hange P/N from CH4104K9B03 to CH41002KB93.	
Michael 10 10 10 10 10 10 10 1	-			PC123	- 1	Channe PIN from RC1SS365707 in RC1SS365721	/ M _
Part	İ	EC-A-21	39 10/	04 PC46	c	· · · · · · · · · · · · · · · · · · ·	
Fig. Apr 1 1 1 1 1 1 1 1 1		EC-A-22	39 10/	PC56,PC59 PC74,PC72,PC1	127	Change PiN from CH5472K9A02 to CH5472M9901.	, N
Fig. Apr 1		EC-A-23	40,41, 42,45. 10/	PC122,PC126,P0 PC412,PC351,P0 PC348,PC350,P0	C121 C430 C365	Change P/N from CH61001ME96 to CH6101M9905.	9
PRINTY LIDE CONTROL INC.			46	PC358,PC349,P0 PC352,PC366	PC357		
PRANTY - LEET -							
PRANTY - LEET -	ĺ			PQ123.PQ124.P	PQ125.	hange PIN from CS37682FB00 to CS37872FB15.	} [
PRANTY - LEET -		EC-A-26	37,44, 45,46 10	/17 PQ82,PQ102,PQ	Q101, Q119	rhange to dual mosfet.	
PRANTY CERT CONTROL OF	,	A	4 4	PQ94,PQ95		00 (64 annual formation)	
PRANTY - LEET -	- [EC-B-01	38 11/	18 PR64	А	djust Battery discharge function.	
PROJECT 1 LEST Quanta Computer Inc.	}	EC-B-02	38 11/	/22 PR35	C	hange footprint from RC0603 to RC1206.	
PROJECT 1 LEST Quanta Computer Inc.							
PROJECT 1 LEST Quanta Computer Inc.							
PROJECT 1 LESC Quanta Computer Inc.							
PROJECT 1 LEST Quanta Computer Inc.							
PROJECT 1 LESC Quanta Computer Inc.							
PROJECT 1 LESC Quanta Computer Inc.							
PROJECT 1 LEST Quanta Computer Inc.							
PROJECT 1 LEST Quanta Computer Inc.							
PROJECT : LEXT: Quantitative for control inc.							
PROJECT : LEXT: Quantitative for control inc.							
PROJECT : LESC Quanta Computer Inc.							
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PROJECT : LESC Quanta Computer Inc.							
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PROJECT : LESC Quanta for Computer Inc.							
PROJECT : LEXC Quanta for Computer Inc.							
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Sia Doursel Norder We 3.4.						Quanta Computer	Inc.
						Size Pocurent Number Outer Open DEC Next	8w 2A

