VULCAIN Discrete

SI Build

2008.12.26

DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE = 3 VER :

FILE NAME : XXXX-XXXXXX-XX

P/N XXXXXXXXXXX

INVENTEC

TITLE *VV Discrete*

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

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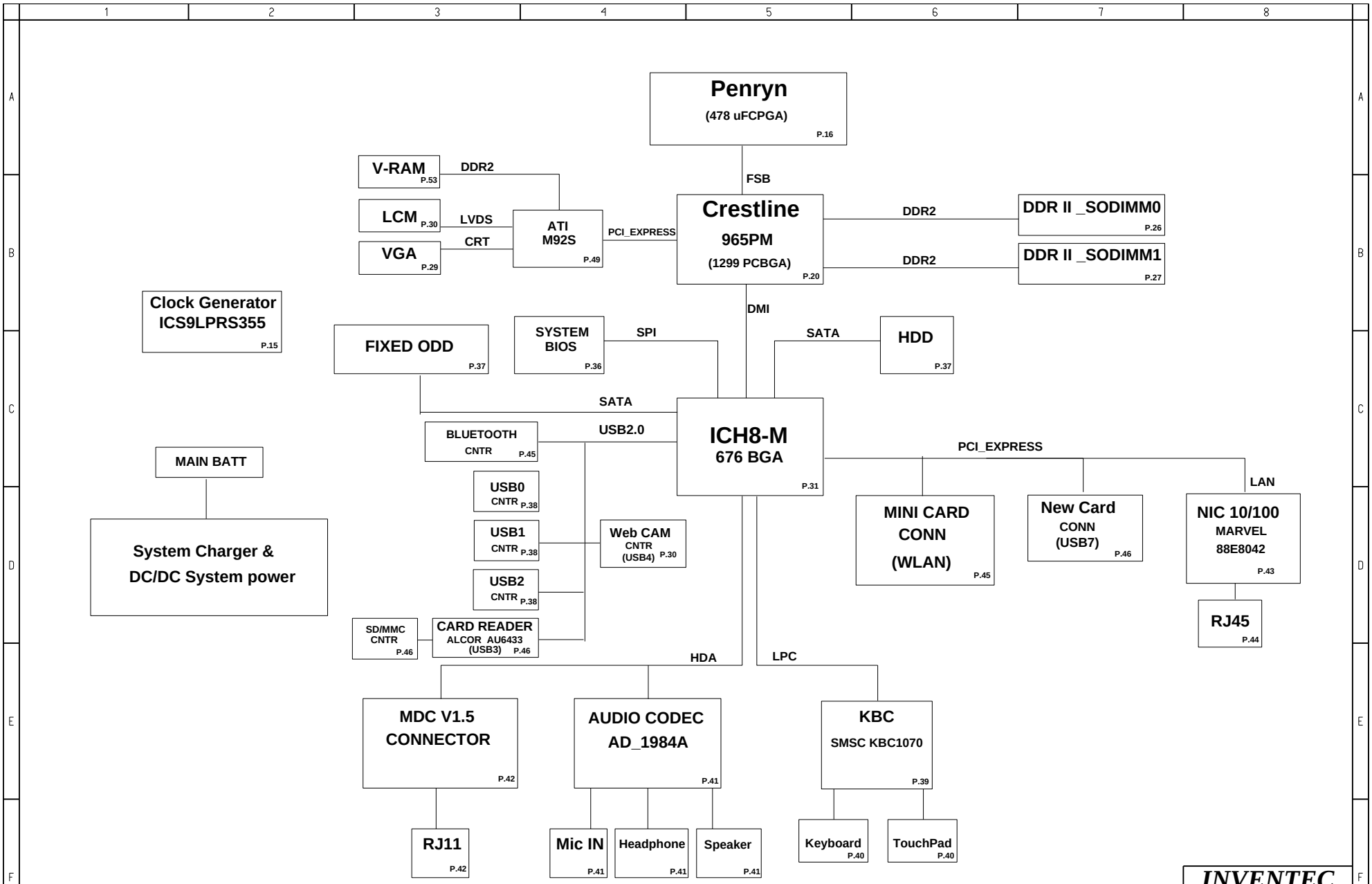
CHANGE by		
Chang, Roger		*30-Nov-2008*

INVENTEC			
TITLE: *VV Discrete*			
SIZE: A3	CODE: CS	DOC. NUMBER: *1310A22294-0-MTR*	REV: *A01*
SHEET 2 OF 54			



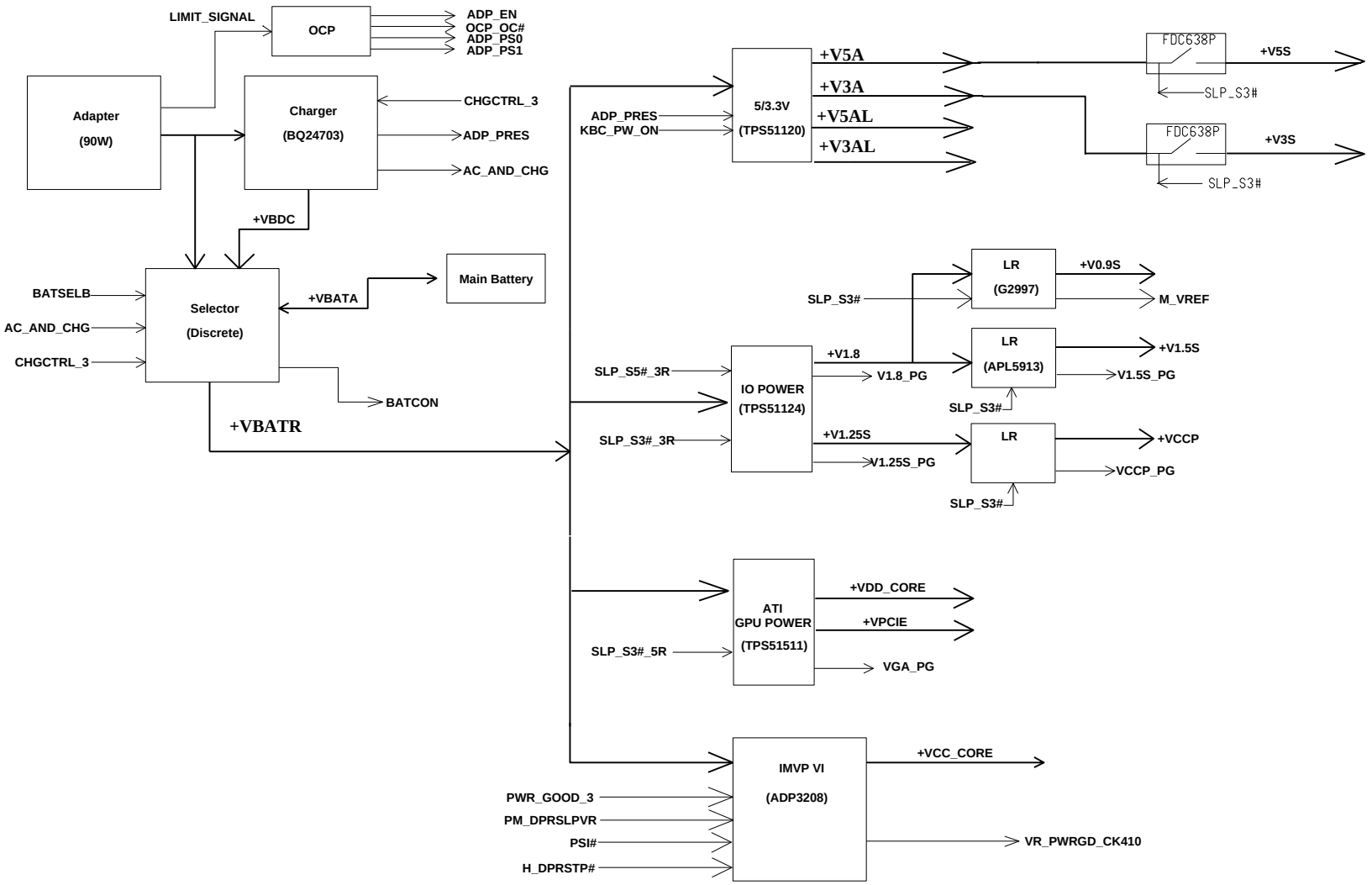
CHANGE by	Chang, Roger	30-Nov-2008	

INVENTEC

TITLE: *VV Discrete*

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 3 OF 54



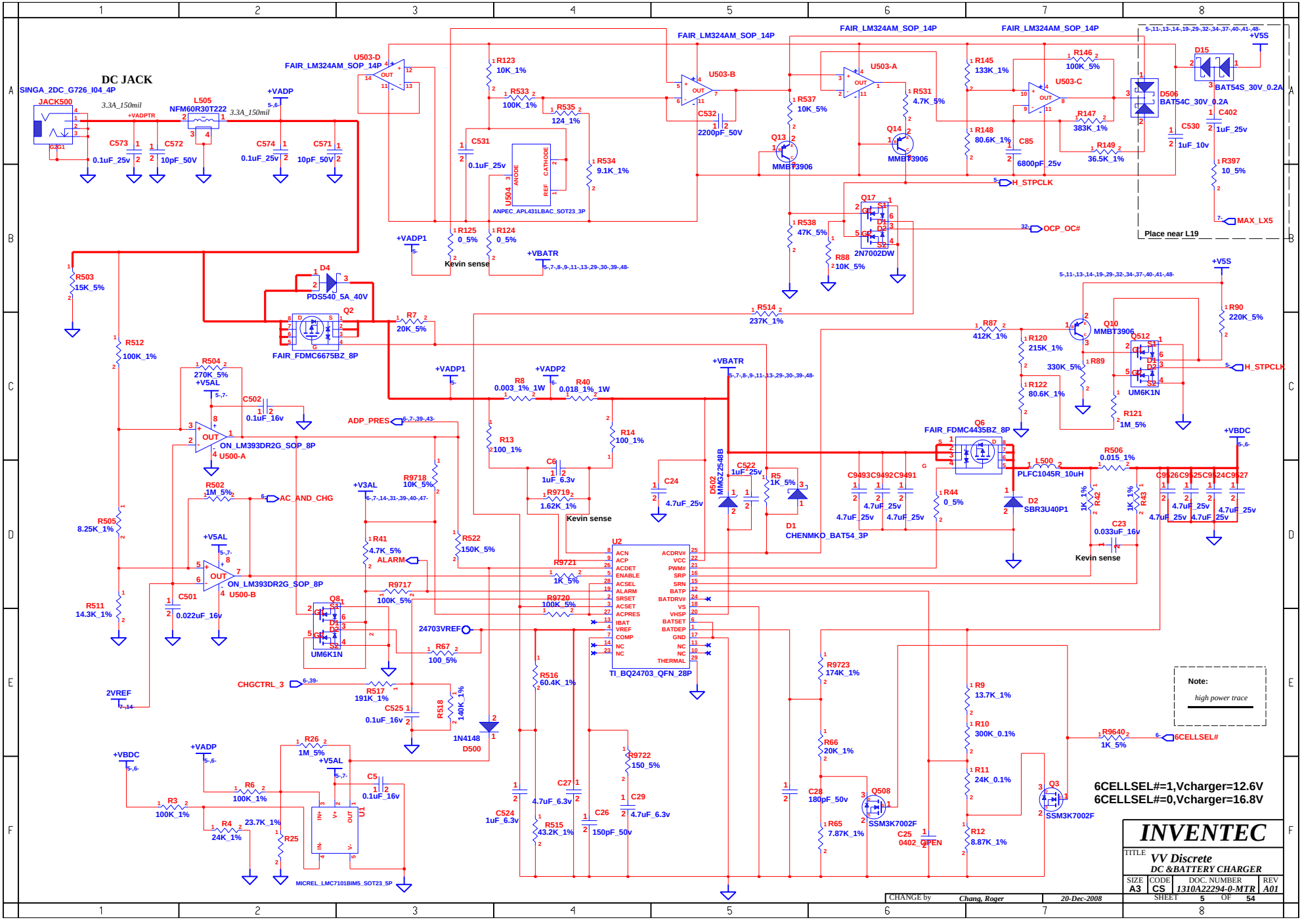
CHANGE by	Chang, Roger	4-Sep-2008

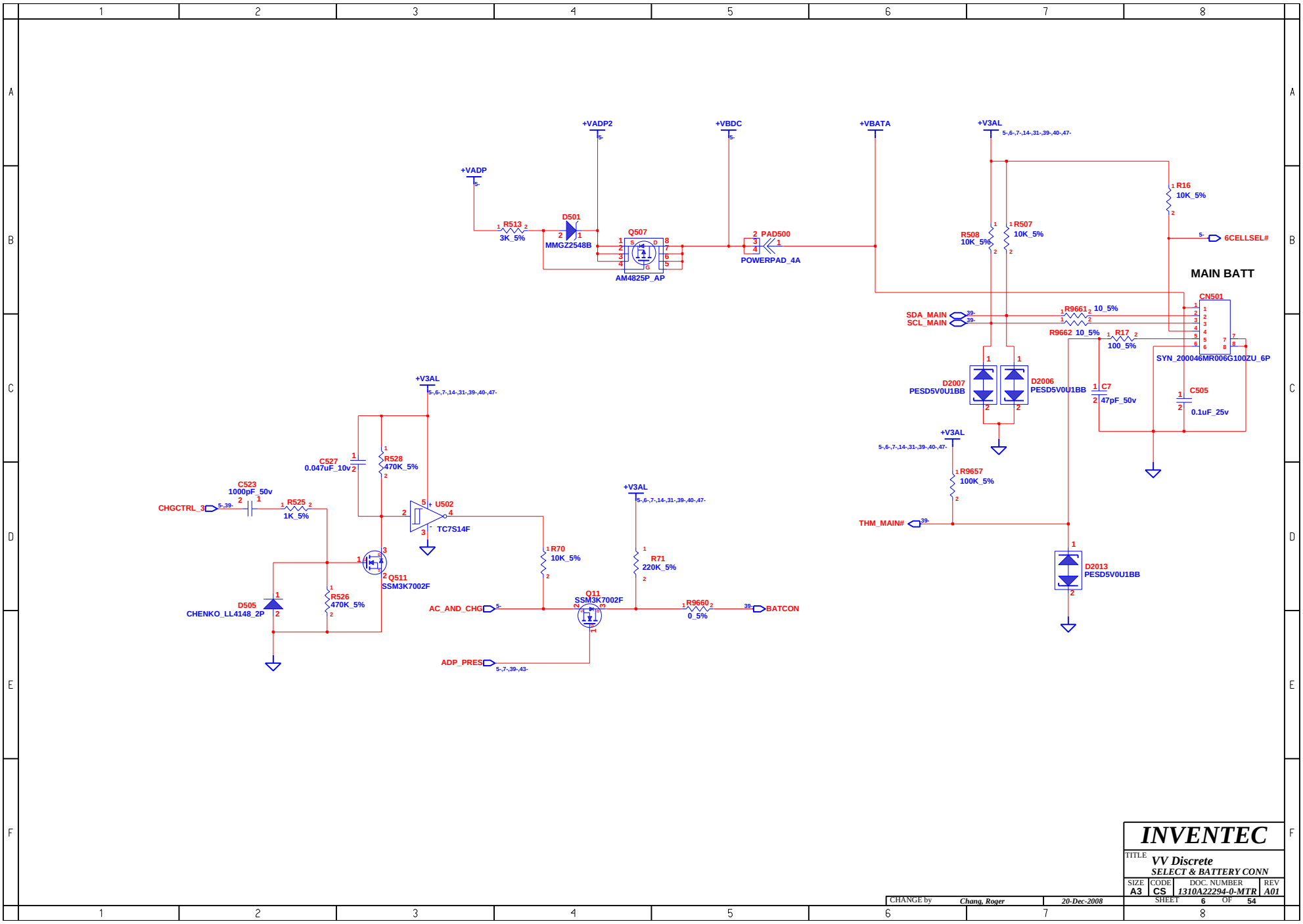
INVENTEC

TITLE: *VV Discrete*

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 4 OF 54


DC JACK
SINGA_2DC_G726_I04_4P
JACK500
3.3A_150mil
L505
NFM60R30T222
+VADP
+VADPTR
C573 0.1uF_25v
C572 10pF_50V
C574 0.1uF_25v
C571 10pF_50V
U503-D
FAIR_LM324AM_SOP_14P
R123 10K_1%
R533 100K_1%
R535 124_1%
C531 0.1uF_25v
U504
ANPEC_APL431LBAC_SOT23_3P
R534 9.1K_1%
R125 0_5%
R124 0_5%
Kevin sense
+VADP1
+VBATR
U503-B
C532 2200pF_50V
U503-A
R537 10K_5%
R531 4.7K_5%
Q13
MMBT3906
Q14
MMBT3906
R145 133K_1%
R146 100K_5%
U503-C
R147 383K_1%
R148 80.6K_1%
C85 6800pF_25v
R149 36.5K_1%
D15
BAT54S_30V_0.2A
D506
BAT54C_30V_0.2A
C530 1uF_10v
C402 1uF_25v
R397 10_5%
MAX_LX5
H_STPCLK
OCP_OC#
Q17
2N7002DW
R538 47K_5%
R88 10K_5%
Place near L19
+V5S
R503 15K_5%
D4
PDS540_5A_40V
Q2
FAIR_FDMC6675BZ_8P
R7 20K_5%
R514 237K_1%
R512 100K_1%
R504 270K_5%
+V5AL
C502 0.1uF_16v
ON_LM393DR2G_SOP_8P
U500-A
ADP_PRES
R8 0.003_1%_1W
R40 0.018_1%_1W
R13 100_1%
R14 100_1%
C6 1uF_6.3v
R9719 1.62K_1%
Kevin sense
C24 4.7uF_25v
D502
MMBZ5248B
C522 1uF_25v
R5 1K_5%
D1
CHENMKO_BAT54_3P
R87 412K_1%
R120 215K_1%
330K_5%
R89
R122 80.6K_1%
Q10
MMBT3906
Q512
UM6K1N
R90 220K_5%
R121 1M_5%
Q6
FAIR_FDMC4435BZ_8P
L500
PLFC1045R_10uH
D2
SBR3U40P1
R506 0.015_1%
C9493 C9492 C9491 4.7uF_25v
C9526 C9525 C9524 C9527 4.7uF_25v
C23 0.033uF_16v
Kevin sense
+VBDC
R502 1M_5%
AC_AND_CHG
+V3AL
R9718 10K_5%
R505 8.25K_1%
R511 14.3K_1%
C501 0.022uF_16v
R41 4.7K_5%
ALARM
R522 150K_5%
U2
TI_BQ24703_QFN_28P
R9721 1K_5%
R9720 100K_5%
R9717 100K_5%
Q8
UM6K1N
24703VREF
R67 100_5%
CHGCTRL_3
R517 191K_1%
C525 0.1uF_16v
R518 2.40K_1%
D500
1N4148
2VREF
R516 60.4K_1%
R9723 174K_1%
R66 20K_1%
R65 7.87K_1%
C28 180pF_50v
Q508
SSM3K7002F
C25 0402_OPEN
R9 13.7K_1%
R10 300K_0.1%
R11 24K_0.1%
R12 8.87K_1%
Q3
SSM3K7002F
R9640 1K_5%
6CELLSEL#
Note:
high power trace
6CELLSEL#=1,Vcharger=12.6V
6CELLSEL#=0,Vcharger=16.8V
+VADP
R26 1M_5%
R6 100K_1%
R3 100K_1%
R4 23.7K_1%
24K_1%
R25
C5 0.1uF_16v
U1
MICREL_LMC7101BIM5_SOT23_5P
C524 1uF_6.3v
C27 4.7uF_6.3v
R515 43.2K_1%
C26 150pF_50v
R9722 150_5%
C29 4.7uF_6.3v
INVENTEC
TITLE
VV Discrete
DC &BATTERY CHARGER
SIZE A3
CODE CS
DOC. NUMBER 1310A22294-0-MTR
REV A01
SHEET 5 OF 54
CHANGE by Chang, Roger 20-Dec-2008



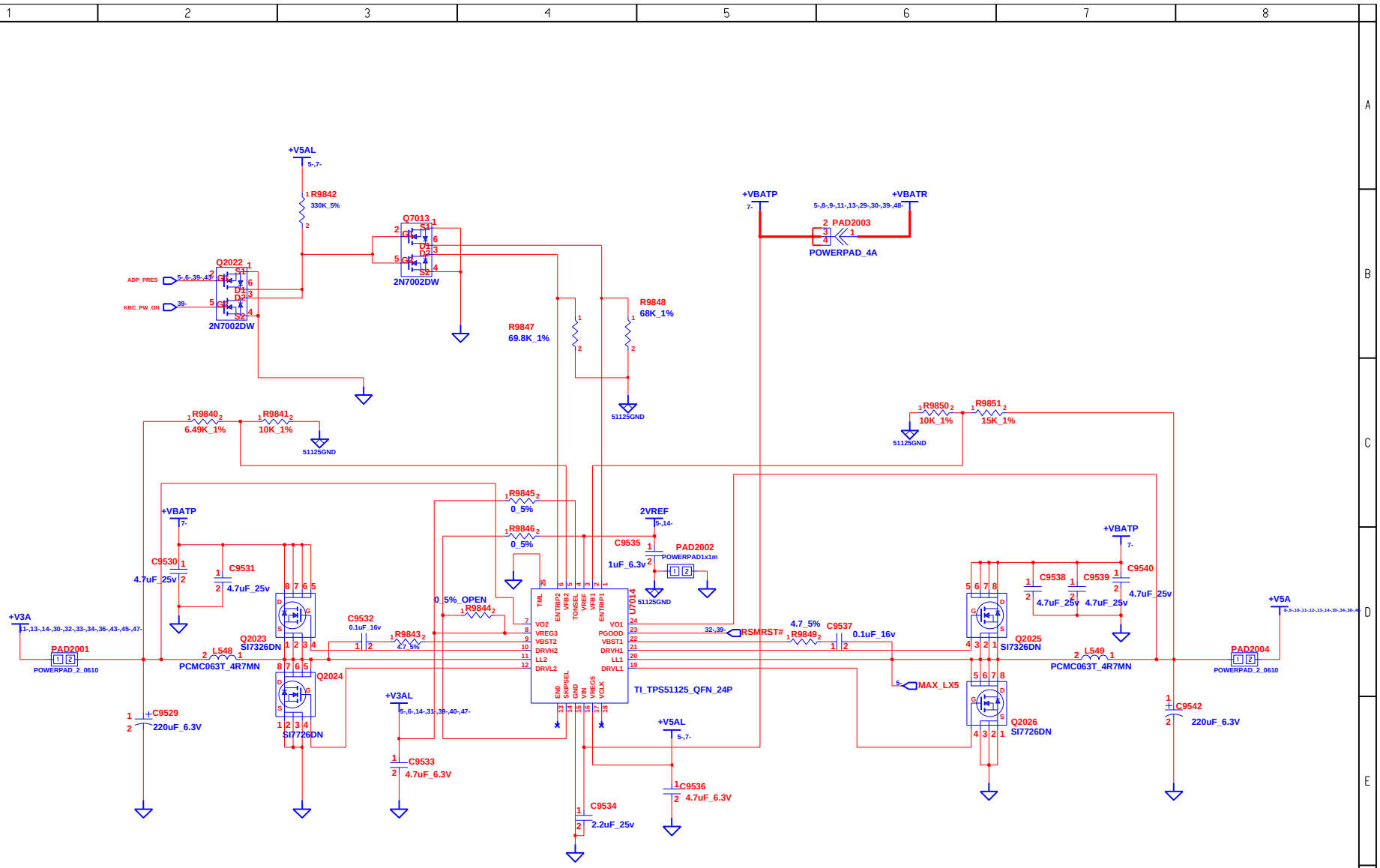
INVENTEC

TITLE: *VV Discrete*
SELECT & BATTERY CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 6 OF 54

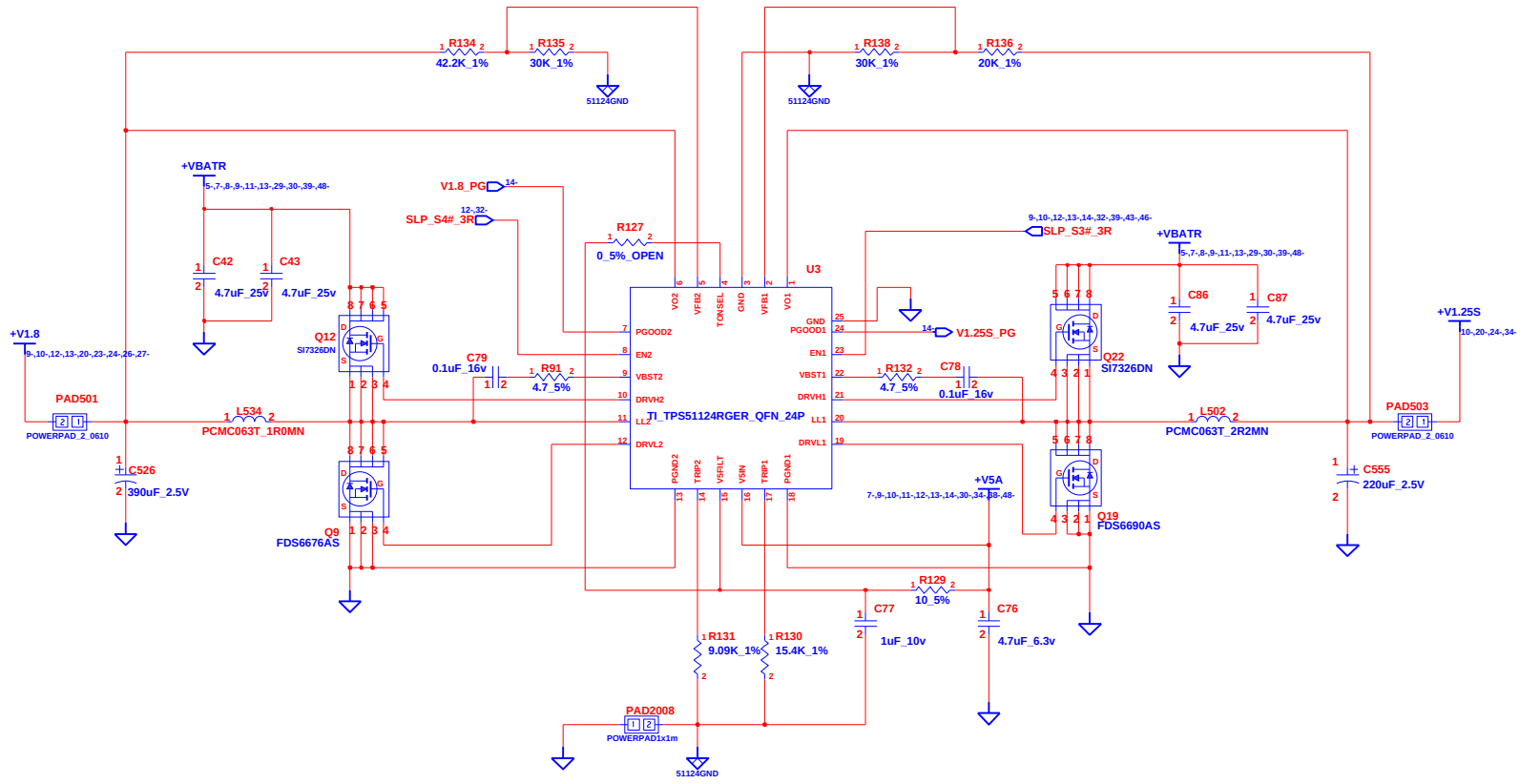
CHANGE by		
	Chang, Roger	*20-Dec-2008*



CHANGE by	*Chang, Roger*	*4-Sep-2008*	

INVENTEC

TITLE	*VV Discrete* *SYSTEM POWER(3V/5V/12V)*		
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*
SHEET	7	OF	54



CHANGE by	Chang, Roger	20-Dec-2008	

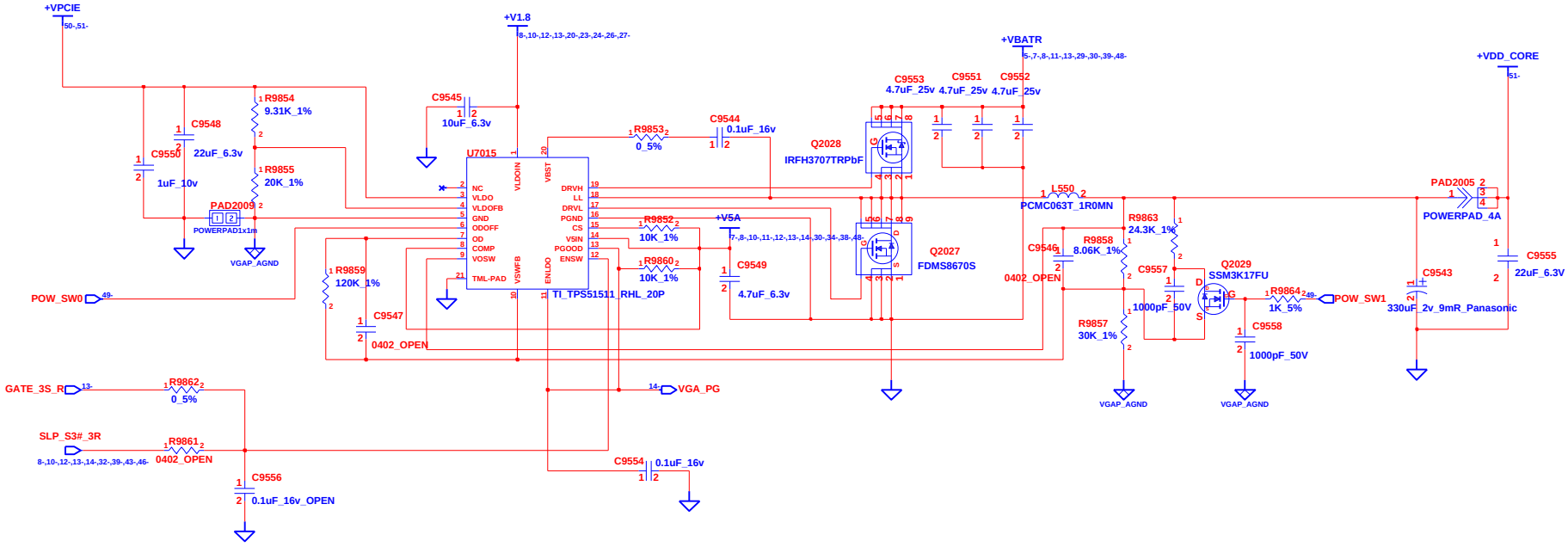
INVENTEC

TITLE: *VV Discrete*
SYSTEM POWER(+V1.8/+V1.25S)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 8 OF 54

POW_SW1	POW_SW0	+VDD_CORE
0	0	1V
0	1	0.95V
1	0	0.9V



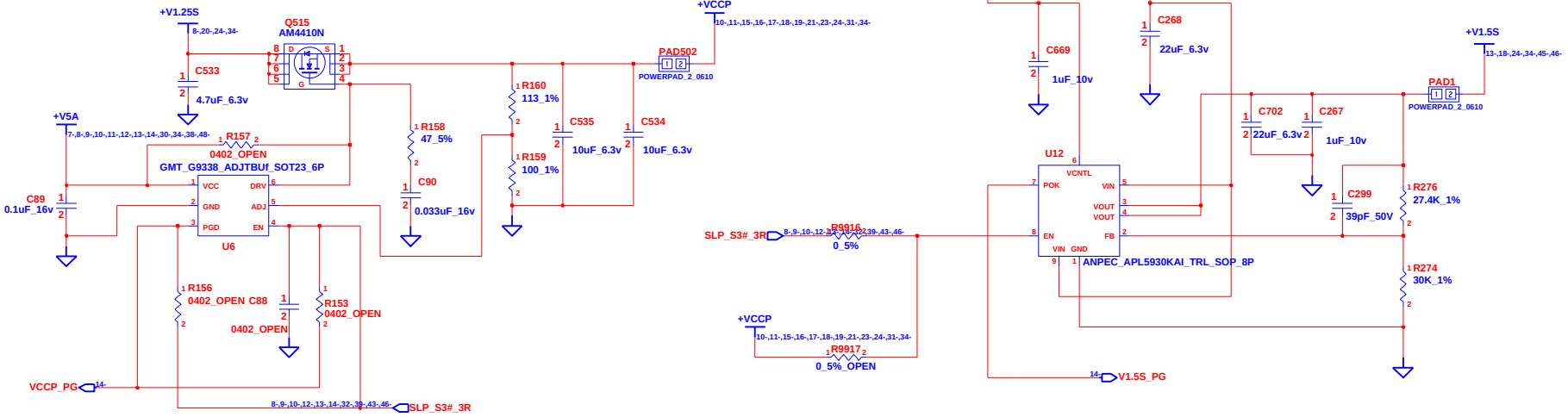
CHANGE by		
Chang, Roger		*4-Sep-2008*

INVENTEC

TITLE: *VV Discrete*
GRAPHIC POWER (+VGFX_CORE)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 9 OF 54



	R579	R576	R578	R577
G9338	0 ohm	OPEN	OPEN	0 ohm
SC339	OPEN	0 ohm	0 ohm	OPEN

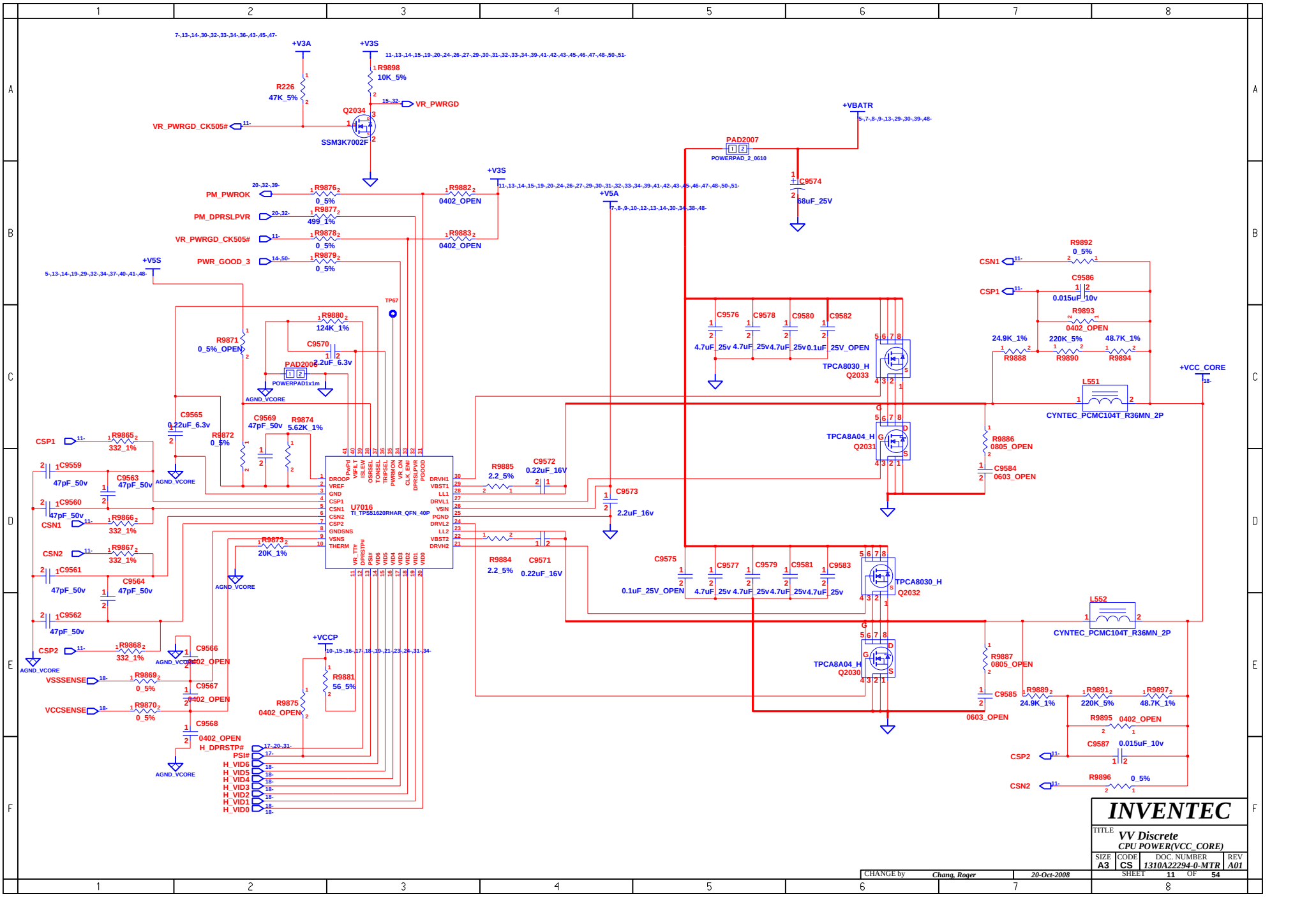
CHANGE by *Chang, Roger* *20-Dec-2008*

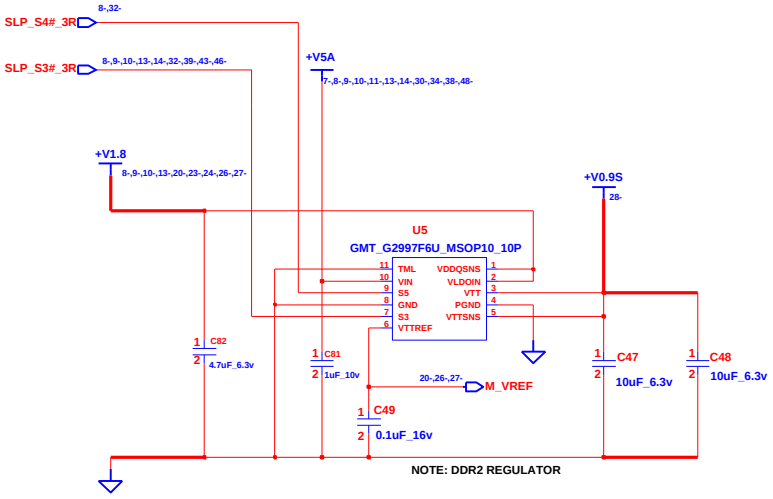
INVENTEC

TITLE *VV Discrete*
SYSTEM POWER(+VCCP/+V1.5S)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 10 OF 54


+V3A
+V3S
R226
47K_5%
R9898
10K_5%
VR_PWRGD
VR_PWRGD_CK505#
Q2034
SSM3K7002F
+VBATR
PAD2007
POWERPAD_2_0610
C9574
68uF_25V
+V5A
PM_PWROK
PM_DPRSLPVR
VR_PWRGD_CK505#
PWR_GOOD_3
R9876
R9877
R9878
R9879
0_5%
499_1%
R9882
R9883
0402_OPEN
+V5S
TP67
R9880
124K_1%
R9871
0_5%_OPEN
C9570
2.2uF_6.3v
PAD2006
POWERPAD1x1m
AGND_VCORE
C9565
0.22uF_6.3v
C9569
47pF_50v
R9874
5.62K_1%
R9872
0_5%
CSP1
CSN1
CSN2
CSP2
R9865
R9866
R9867
R9868
332_1%
C9559
C9560
C9561
C9562
C9563
C9564
47pF_50v
U7016
TI_TPS51620RHAR_QFN_40P
DROOP
VREF
GND
CSP1
CSN1
CSP2
GNDSNS
VSNS
THERM
PwrPd
VSFLT
ISLEW
OSNSEL
TONSEL
TRIPSEL
PWRMON
VR_ON
CLK_EN#
DPRSLPVR
PGOOD
DRVH1
VBST1
LL1
DRVL1
VSIN
PGND
DRVL2
LL2
VBST2
DRVH2
VR_TT#
DPRSTP#
PSI#
VID6
VID5
VID4
VID3
VID2
VID1
VID0
R9873
20K_1%
R9885
2.2_5%
C9572
0.22uF_16V
C9573
2.2uF_16v
R9884
2.2_5%
C9571
0.22uF_16V
+VCCP
R9881
56_5%
R9875
0402_OPEN
C9566
C9567
C9568
VSSSENSE
VCCSENSE
R9869
R9870
0_5%
H_DPRSTP#
PSI#
H_VID6
H_VID5
H_VID4
H_VID3
H_VID2
H_VID1
H_VID0
C9575
0.1uF_25V_OPEN
C9576
C9578
C9580
C9582
4.7uF_25v
0.1uF_25V_OPEN
TPCA8030_H
Q2033
TPCA8A04_H
Q2031
C9577
C9579
C9581
C9583
TPCA8030_H
Q2032
TPCA8A04_H
Q2030
R9892
0_5%
C9586
0.015uF_10v
R9893
0402_OPEN
24.9K_1%
220K_5%
48.7K_1%
R9888
R9890
R9894
+VCC_CORE
L551
CYNTEC_PCMC104T_R36MN_2P
R9886
0805_OPEN
C9584
0603_OPEN
L552
R9887
0805_OPEN
C9585
0603_OPEN
R9889
R9891
R9897
R9895
0402_OPEN
C9587
0.015uF_10v
R9896
INVENTEC
TITLE
VV Discrete
CPU POWER(VCC_CORE)
SIZE A3
CODE CS
DOC. NUMBER 1310A22294-0-MTR
REV A01
CHANGE by Chang, Roger 20-Oct-2008
SHEET 11 OF 54



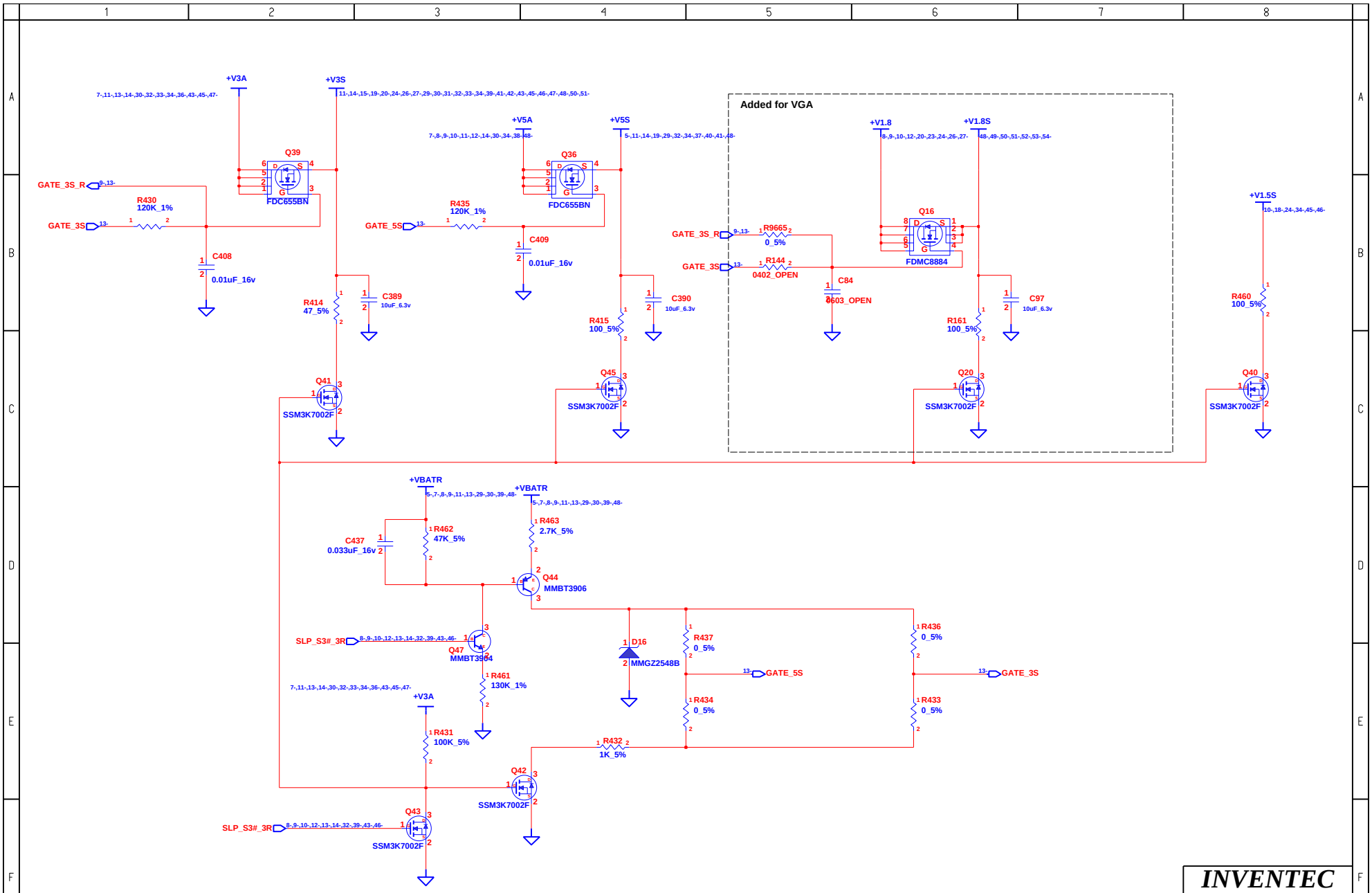
CHANGE by	Chang, Roger	4-Sep-2008	

INVENTEC

TITLE: *VV Discrete*
DDR TERMINATION VOLTAGE

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 12 OF 54



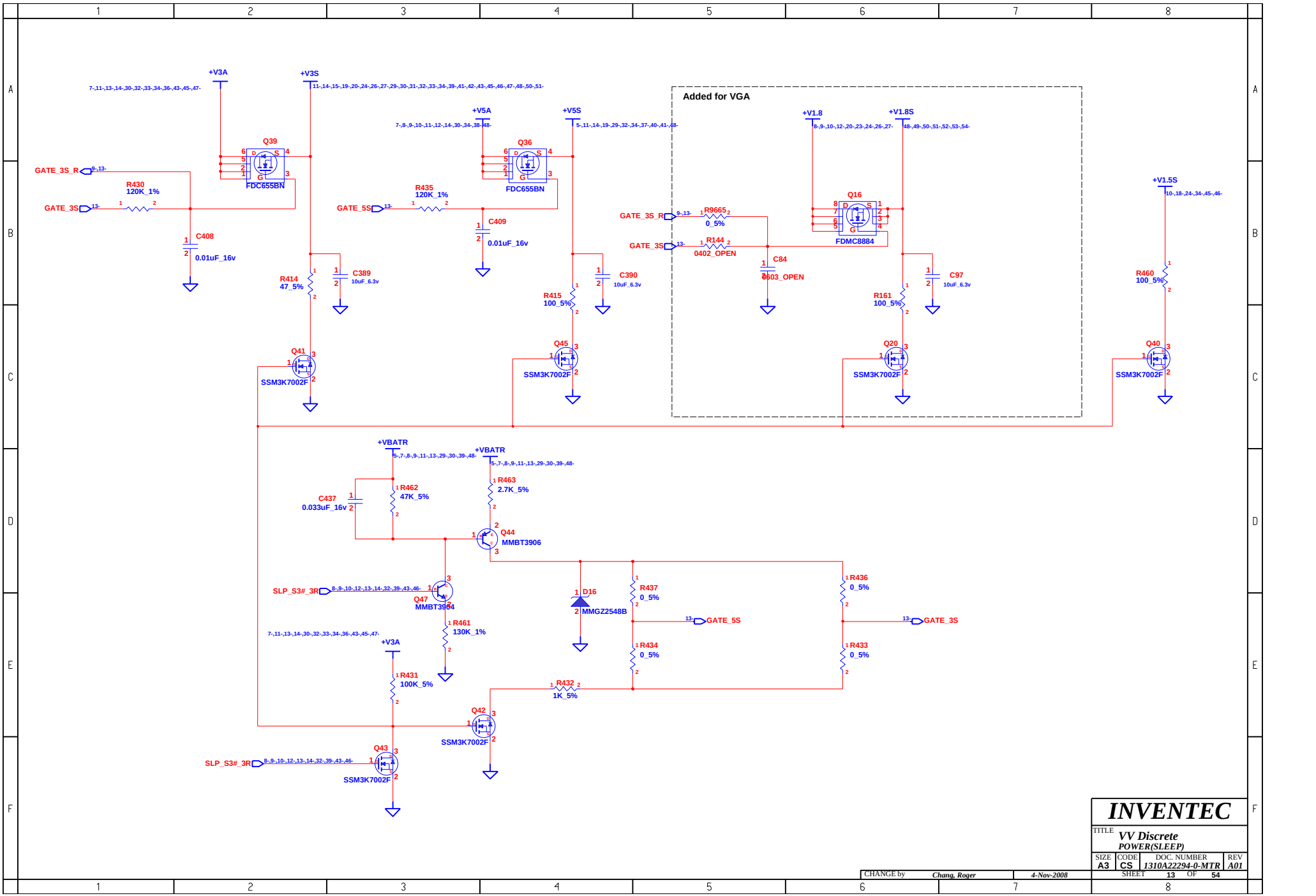
CHANGE by	*Chang, Roger*	*4-Nov-2008*		

INVENTEC

TITLE: ***VV Discrete***
POWER(SLEEP)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 13 OF 54



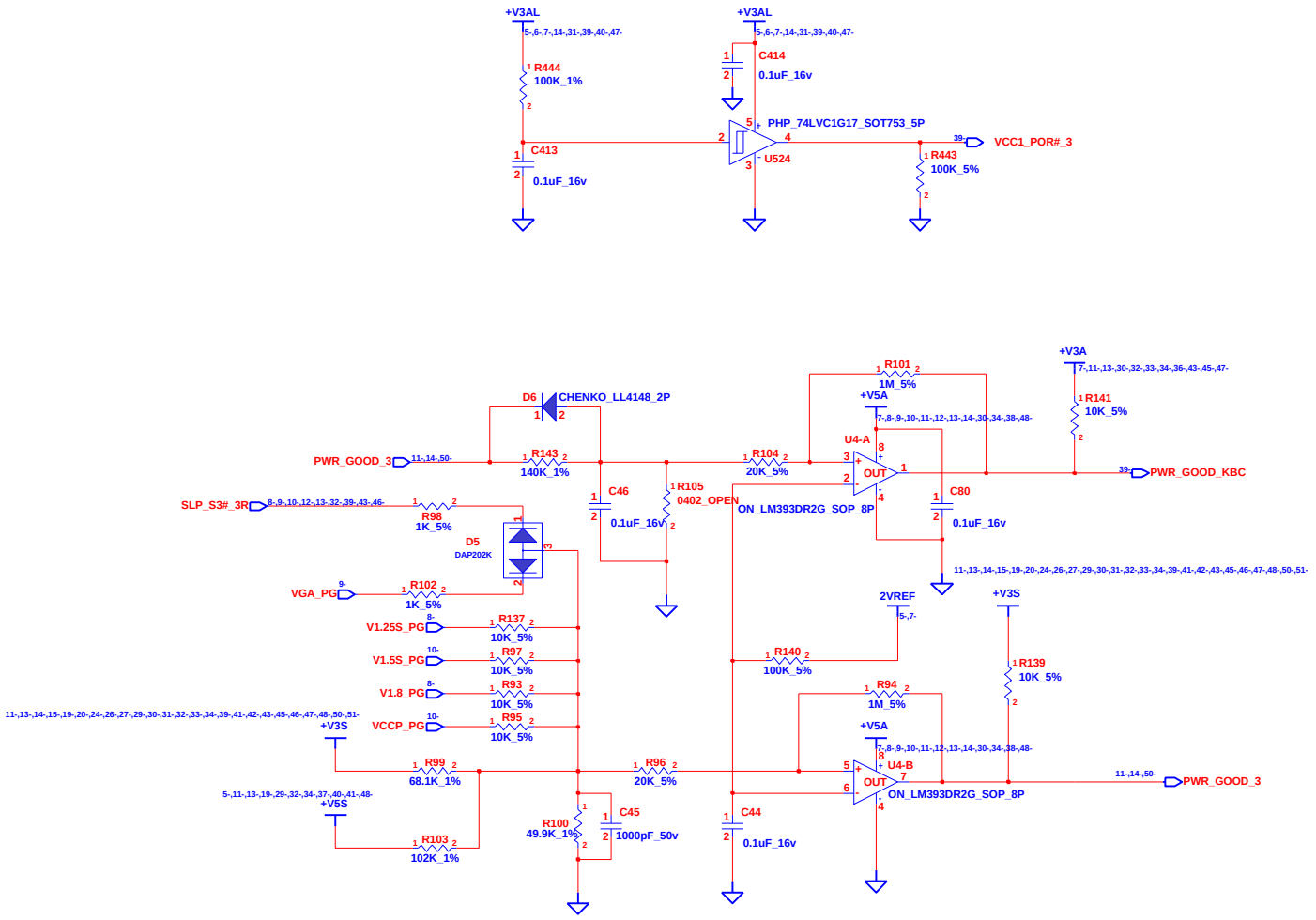
CHANGE by		
Chang, Roger	4-Nov-2008	

INVENTEC

TITLE: *VV Discrete*
POWER(SLEEP)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 13 OF 54



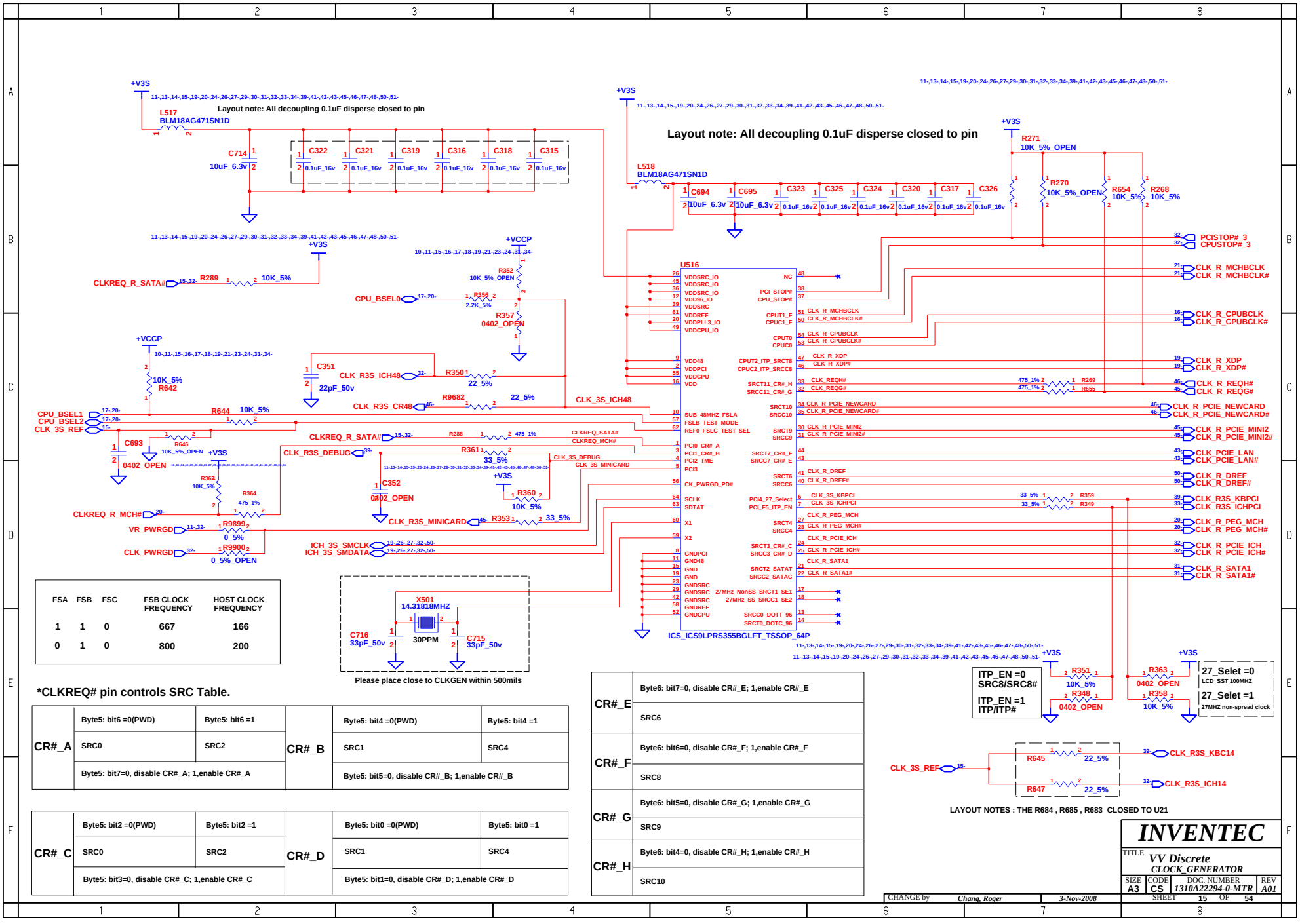
CHANGE by	*Chang, Roger*	*4-Nov-2008*	

INVENTEC

TITLE: ***VV Discrete***
POWER(SEQUENCE)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 14 OF 54



FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200

***CLKREQ# pin controls SRC Table.**

CR#_A	Byte5: bit6 =0(PWD)	Byte5: bit6 =1	CR#_B	Byte5: bit4 =0(PWD)	Byte5: bit4 =1
	SRC0	SRC2		SRC1	SRC4
	Byte5: bit7=0, disable CR#_A; 1,enable CR#_A			Byte5: bit5=0, disable CR#_B; 1,enable CR#_B	

CR#_C	Byte5: bit2 =0(PWD)	Byte5: bit2 =1	CR#_D	Byte5: bit0 =0(PWD)	Byte5: bit0 =1
	SRC0	SRC2		SRC1	SRC4
	Byte5: bit3=0, disable CR#_C; 1,enable CR#_C			Byte5: bit1=0, disable CR#_D; 1,enable CR#_D	

CR#_E	Byte6: bit7=0, disable CR#_E; 1,enable CR#_E
	SRC6
CR#_F	Byte6: bit6=0, disable CR#_F; 1,enable CR#_F
	SRC8
CR#_G	Byte6: bit5=0, disable CR#_G; 1,enable CR#_G
	SRC9
CR#_H	Byte6: bit4=0, disable CR#_H; 1,enable CR#_H
	SRC10

LAYOUT NOTES : THE R684 , R685 , R683 CLOSED TO U21

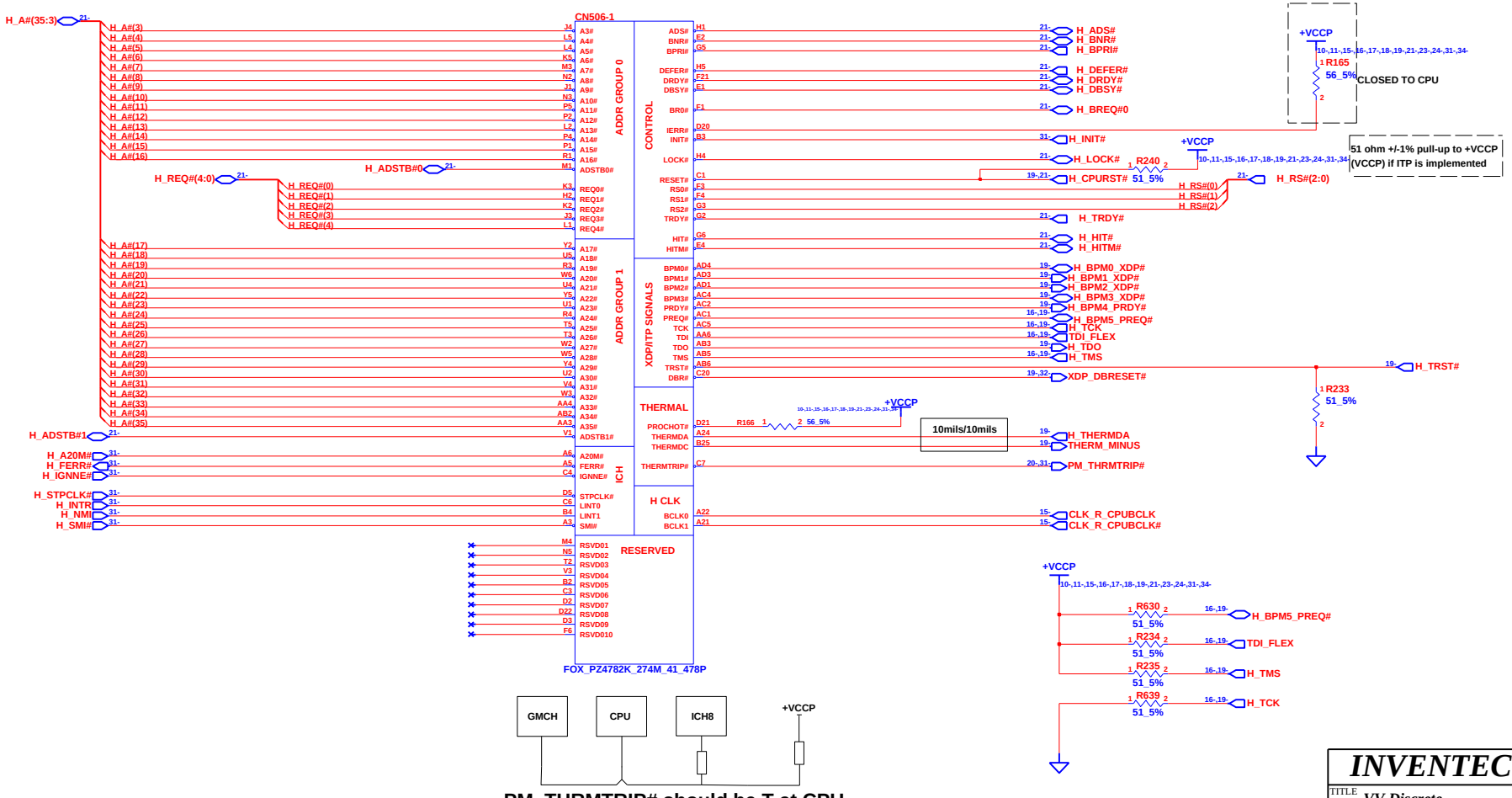
CHANGE by: Chang, Roger 3-Nov-2008

INVENTEC

TITLE: VV Discrete CLOCK_GENERATOR

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 15 OF 54



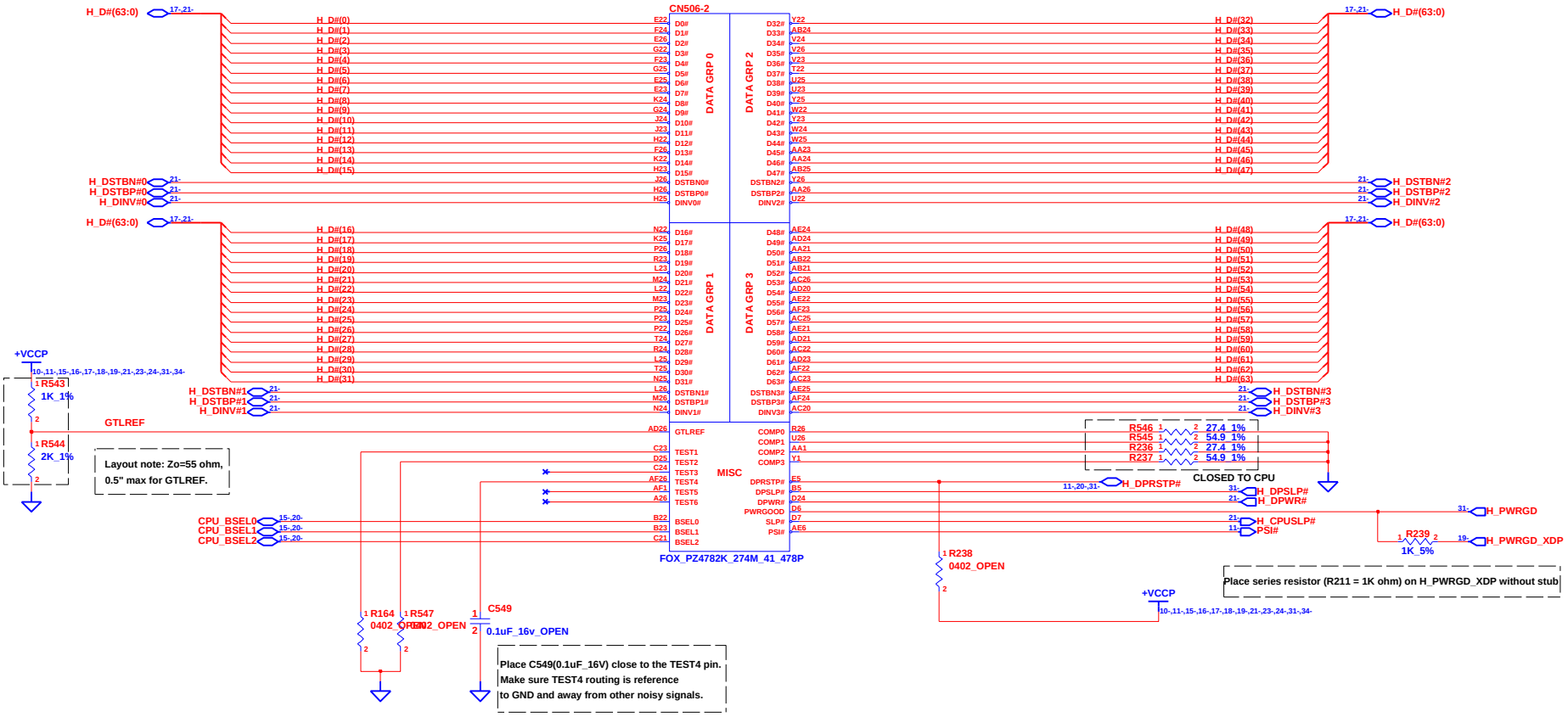
CHANGE by	Chang, Roger	3-Nov-2008	

INVENTEC

TITLE: *VV Discrete*
MEROM-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 16 OF 54



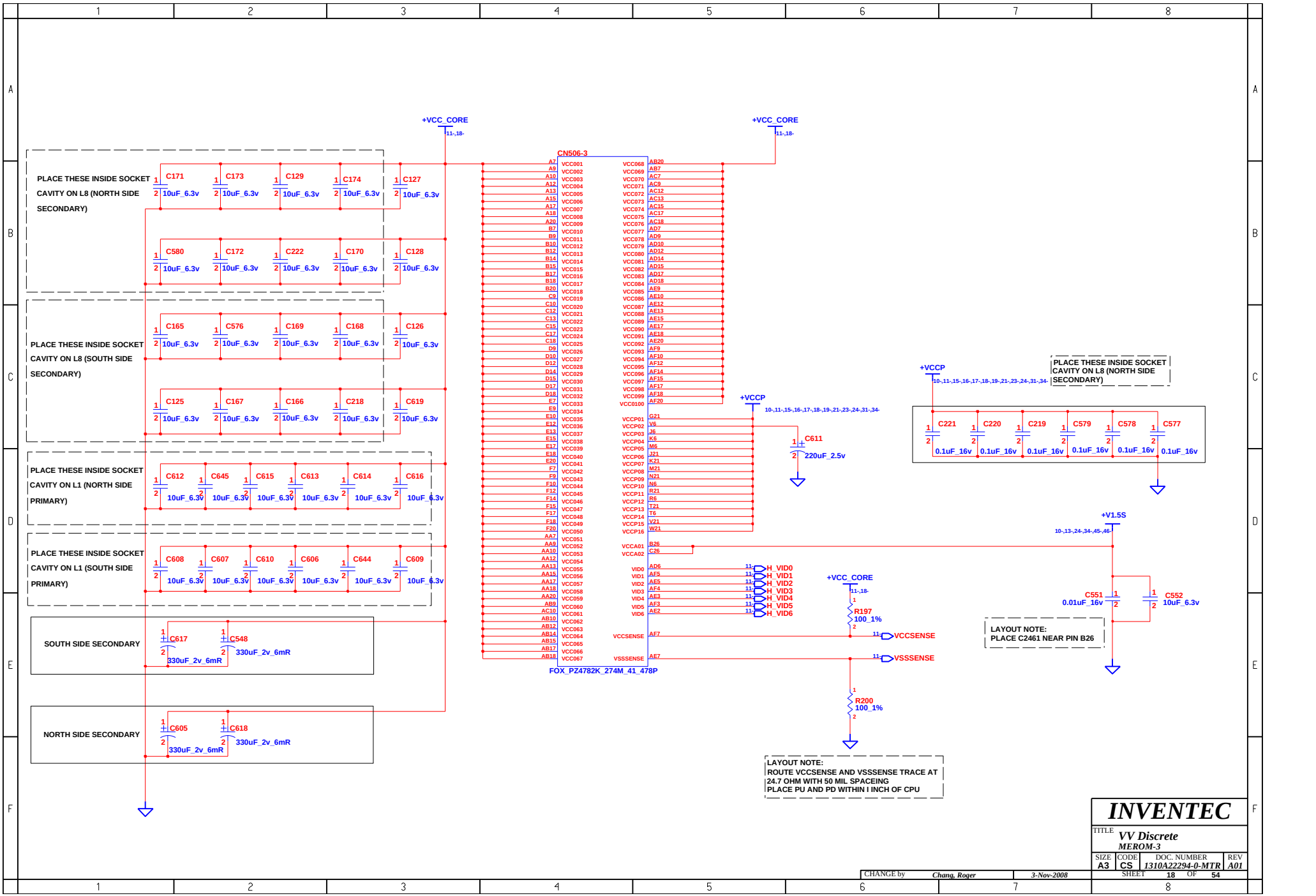
CHANGE by	Chang, Roger	3-Nov-2008		

INVENTEC

TITLE: *VV Discrete*
MEROM-2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 17 OF 54



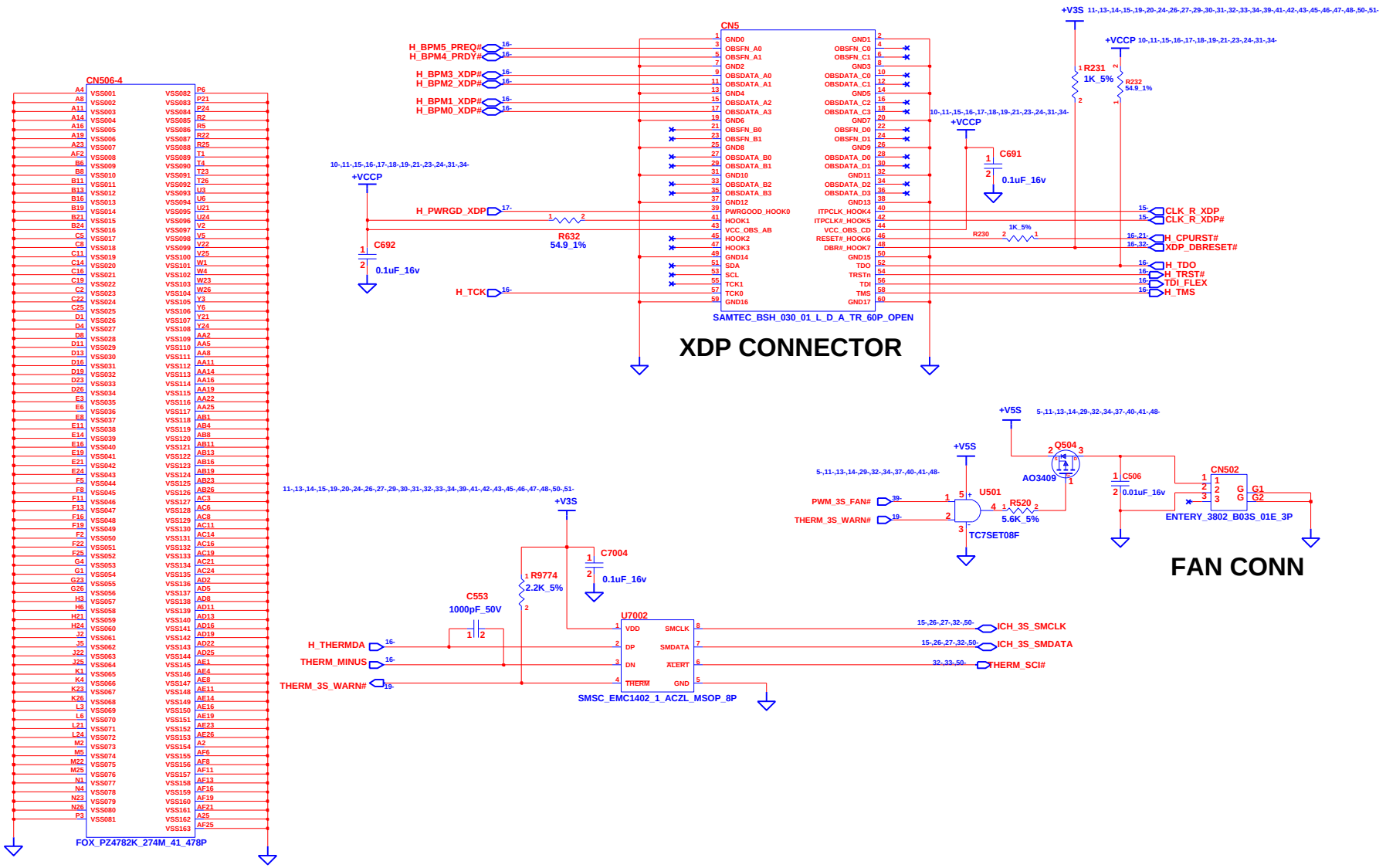
CHANGE by	*Chang, Roger*	*3-Nov-2008*			

INVENTEC

TITLE: *VV Discrete*
MEROM-3

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 18 OF 54



CHANGE by	Chang, Roger
	3-Nov-2008

INVENTEC

TITLE: VV Discrete
THERMAL&FAN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 19 OF 54

MCH_CFG(5)	LOW=DMIx2 HIGH=DMIx4

MCH_CFG(7) (CPU Strap)	LOW=RSVD HIGH=Mobile CPU

MCH_CFG(9) PCIE Graphics Lane	LOW=Reverse Lane HIGH=Normal operation

NOTE : USE 4K-OHM RESISTOR WHEN INSTALLING PULL-UP/PULL-DOWN RESISTOR ON ANY MCH-CFG CONNECTION/PINS.

MCH_CFG(16) 20-
MCH_CFG(9) 20-
MCH_CFG(7) 20-
MCH_CFG(5) 20-

R203 0402_OPEN 2
R204 0402_OPEN 2
R201 0402_OPEN 2
R202 0402_OPEN 2

MCH_CFG(13:12) XOR/ALLZ	00=PARTIAL CLOCK GATING DISABLE 01=XOR MODE ENABLE 10=ALL-Z MODE ENABLE 11=NORMAL OPERATION

MCH_CFG(16) (FSB Dynamic ODT)	LOW=Dynamic ODT Disable HIGH=Dynamic ODT Enable

MCH_CFG(11) PSB 4X CLK ENABLE	LOW=CALISTOGA HIGH=RESERVED

NOTE: CFG[2:0] STRP : 001b : 533 MT/S
011b : 667 MT/S

+V1.8
8-,9-,10-,12-,13-,20-,23-,24-,26-,27-

R540 20_1% 2
20- SM_RCOMP
20- SM_RCOMP#

R554 20_1% 2

Note: R1351,R1352
For Calero : 80.6 ohm
For Crestline : 20 ohm

+V3S
11-,13-,14-,15-,19-,20-,24-,26-,27-,29-,30-,31-,32-,33-,34-,39-,41-,42-,43-,45-,46-,47-,48-,50-,51-

R250 10K_5% 15-,20- CLKREQ_R_MCH#
R246 10K_5% 20-,26- PM_EXTTS#0
R248 10K_5% 20-,27- PM_EXTTS#1

CPU_BSEL0 15-,17-
CPU_BSEL2 15-,17-
R205 1K_5%
R173 1K_5%
CPU_BSEL1 15-,17-
MCH_CFG(17:3) 20-

+V3S
11-,13-,14-,15-,19-,20-,24-,26-,27-,29-,30-,31-,32-,33-,34-,39-,41-,42-,43-,45-,46-,47-,48-,50-,51-

R206 0402_OPEN
R244 0402_OPEN
R245 0402_OPEN

MCH_CFG(18) 20-
MCH_CFG(19) 20-
MCH_CFG(20) 20-

PM_PWROK 11-,20-,32-,39-
R167 100_5%
BM_BUSY# 32-
H_DPRSTP# 11-,17-,31-
PM_EXTTS#0 20-,26-
PM_EXTTS#1 20-,27-
PLT_RST# 33-,46-
PM_THRMTRIP# 16-,31-
PM_DPRSLPVR 11-,32-

U510-2

RSVD: P36 P37 R35 N35 AR12 AR13 AM12 AN13 J12 AR37 AM36 AL36 AM37 D20 H10 B51 BJ20 BK22 BF19 BH20 BK18 BJ18 BF23 BG23 BC23 BD24 BJ29 BE24 BH39 AW20 BK20 C48 D47 B44 C44 A35 B37 B36 B34 C34

MA_A(14) 26-,28-
MB_A(14) 27-,28-

DDR MUXING:
SM_CK_0 AV29 26- M_CLK_DDR0
SM_CK_1 BB23 26- M_CLK_DDR1
SM_CK_3 BA25 27- M_CLK_DDR2
SM_CK_4 AV23 27- M_CLK_DDR3
SM_CK#_0 AW30 26- M_CLK_DDR0#
SM_CK#_1 BA23 26- M_CLK_DDR1#
SM_CK#_3 AW25 27- M_CLK_DDR2#
SM_CK#_4 AW23 27- M_CLK_DDR3#
SM_CKE_0 BE29 26-,28- M_CKE0
SM_CKE_1 AY32 26-,28- M_CKE1
SM_CKE_3 BD39 27-,28- M_CKE2
SM_CKE_4 BG37 27-,28- M_CKE3
SM_CS#_0 BG20 26-,28- M_CS0#
SM_CS#_1 BK16 26-,28- M_CS1#
SM_CS#_2 BG16 27-,28- M_CS2#
SM_CS#_3 BE13 27-,28- M_CS3#
SM_ODT_0 BH18 26-,28- M_ODT0
SM_ODT_1 BJ15 26-,28- M_ODT1
SM_ODT_2 BJ14 27-,28- M_ODT2
SM_ODT_3 BE16 27-,28- M_ODT3
SM_RCOMP BL15 20- SM_RCOMP
SM_RCOMP# BK14 20- SM_RCOMP#
SM_RCOMP_VOH BK31 20- SM_RCOMP_VOH
SM_RCOMP_VOL BL31 20- SM_RCOMP_VOL
SM_VREF_0 AR49
SM_VREF_1 AW4 12-,26-,27- M_VREF

C145 0.1uF_16v

CLK:
DPLL_REF_CLK B42 C42
DPLL_REF_SSCLK H48 H47
PEG_CLK K44 15- CLK_R_PEG_MCH
PEG_CLK# K45 15- CLK_R_PEG_MCH#

DMI:
DMI_RXN_0 AN47 DMI_TXN(0)
DMI_RXN_1 AJ38 DMI_TXN(1)
DMI_RXN_2 AN42 DMI_TXN(2)
DMI_RXN_3 AN46 DMI_TXN(3)
DMI_TXN(3:0) 32-
DMI_RXP_0 AM47 DMI_TXP(0)
DMI_RXP_1 AJ39 DMI_TXP(1)
DMI_RXP_2 AN41 DMI_TXP(2)
DMI_RXP_3 AN45 DMI_TXP(3)
DMI_TXP(3:0) 32-
DMI_TXN_0 AJ46 DMI_RXN(0)
DMI_TXN_1 AJ41 DMI_RXN(1)
DMI_TXN_2 AM40 DMI_RXN(2)
DMI_TXN_3 AM44 DMI_RXN(3)
DMI_RXN(3:0) 32-
DMI_TXP_0 AJ47 DMI_RXP(0)
DMI_TXP_1 AJ42 DMI_RXP(1)
DMI_TXP_2 AM39 DMI_RXP(2)
DMI_TXP_3 AM43 DMI_RXP(3)
DMI_RXP(3:0) 32-

CFG: P27 N27 N24 C21 C23 F23 N23 G23 J20 C20 R24 L23 J21 E23 E20 K23 M20 M24 L32 N33 L35
MCH_CFG(3) MCH_CFG(4) MCH_CFG(5) MCH_CFG(6) MCH_CFG(7) MCH_CFG(8) MCH_CFG(9) MCH_CFG(10) MCH_CFG(11) MCH_CFG(12) MCH_CFG(13) MCH_CFG(14) MCH_CFG(15) MCH_CFG(16) MCH_CFG(17)
MCH_CFG(18) 20-
MCH_CFG(19) 20-
MCH_CFG(20) 20-

GRAPHICS VID:
GFX_VID_0 E35 TP39
GFX_VID_1 A39 TP40
GFX_VID_2 C38 TP41
GFX_VID_3 B39 TP42
DFGT_VR_EN E36 TP43

PM: G41 L39 L36 J36 AW49 AV20 N20 G36
PM_BM_BUSY#
PM_DPRSTP#
PM_EXT_TS#_0
PM_EXT_TS#_1
PWROK
RSTIN#
THRMTRIP#
DPRSLPVR

ME:
CL_CLK AM49 32- CL_CLK0
CL_DATA AK50 32- CL_DATA0
CL_PWROK AT43 11-,20-,32-,39- PM_PWROK
CL_RST# AN49 32- CL_RST#0
CL_VREF AM50

NC: BJ51 BK51 BK50 BL50 BL49 BL3 BL2 BK1 BJ1 E1 A5 C51 B50 A50 A49 BK2
NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13 NC14 NC15 NC16

MISC:
SDVO_CTRL_CLK H35
SDVO_CTRL_DATA K36
CLK_REQ# G39 15-,20- CLKREQ_R_MCH#
ICH_SYNC# G40 32- MCH_ICH_SYNC#
TEST_1 A37
TEST_2 R32
R177 20K_5%
R607 0_5%

ITL_CRESTLINE_DIS_FCBGA_1299P

+V1.8
8-,9-,10-,12-,13-,20-,23-,24-,26-,27-

R555 1K_1%
R541 3K_1% C558 0.01uF_16v C536 2.2uF_16V 20- SM_RCOMP_VOH
R556 1K_1% C559 0.01uF_16v C537 2.2uF_16V 20- SM_RCOMP_VOL

+V1.25S
8-,10-,24-,34-

R573 1K_1%
C588 0.1uF_16v
R572 392_1%

MCH_CFG(18) VCC SELECT	LOW=1.05V HIGH=1.5V

MCH_CFG(19) (DMI LANE REVERSAL)	LOW=NORMAL HIGH=LANES REVERSED

MCH_CFG(20) (PCIE BACKWARD INTERPOERABILITY MODE	LOW=ONLY SDVO OR PCIE X1 IS OPERATIONAL HIGH=SDVO AND PCIE X1 ARE OPERATING SIMULTANEOUSLY VIA THE PEG PORT

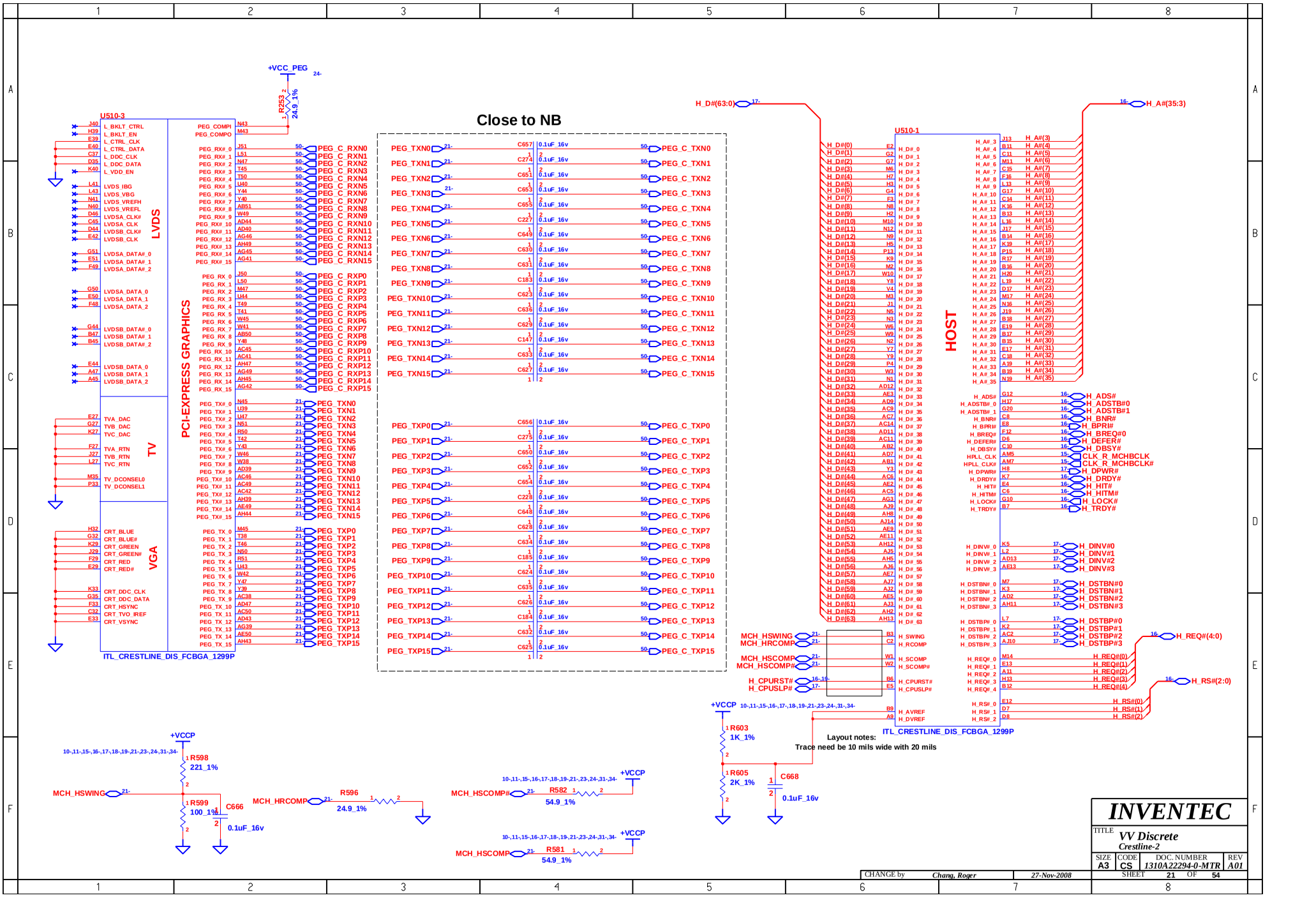
CHANGE by Chang, Roger 27-Nov-2008

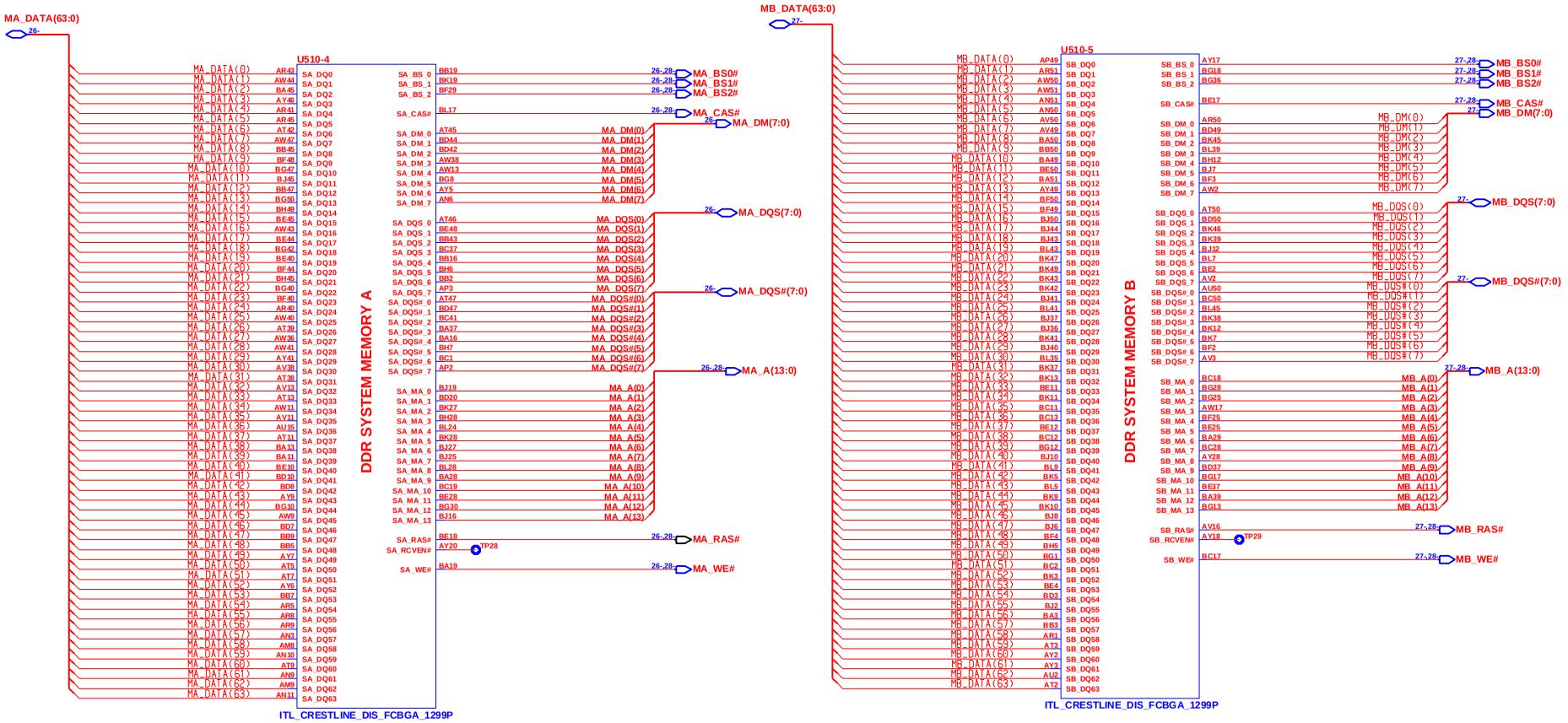
INVENTEC

TITLE VV Discrete
CRESTLINE-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 20 OF 54


Close to NB
U510-3
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
ITL_CRESTLINE_DIS_FCBGA_1299P
U510-1
HOST
ITL_CRESTLINE_DIS_FCBGA_1299P
+VCC_PEG
R253
24.9_1%
H_D#(63:0)
H_A#(35:3)
Layout notes:
Trace need be 10 mils wide with 20 mils
+VCCP
R603
1K_1%
R605
2K_1%
C668
0.1uF_16v
R598
221_1%
R599
100_1%
C666
0.1uF_16v
R596
24.9_1%
R582
54.9_1%
R581
54.9_1%
INVENTEC
VV Discrete
Crestline-2
SIZE A3
CODE CS
DOC. NUMBER 1310A22294-0-MTR
REV A01
CHANGE by Chang, Roger
27-Nov-2008
SHEET 21 OF 54



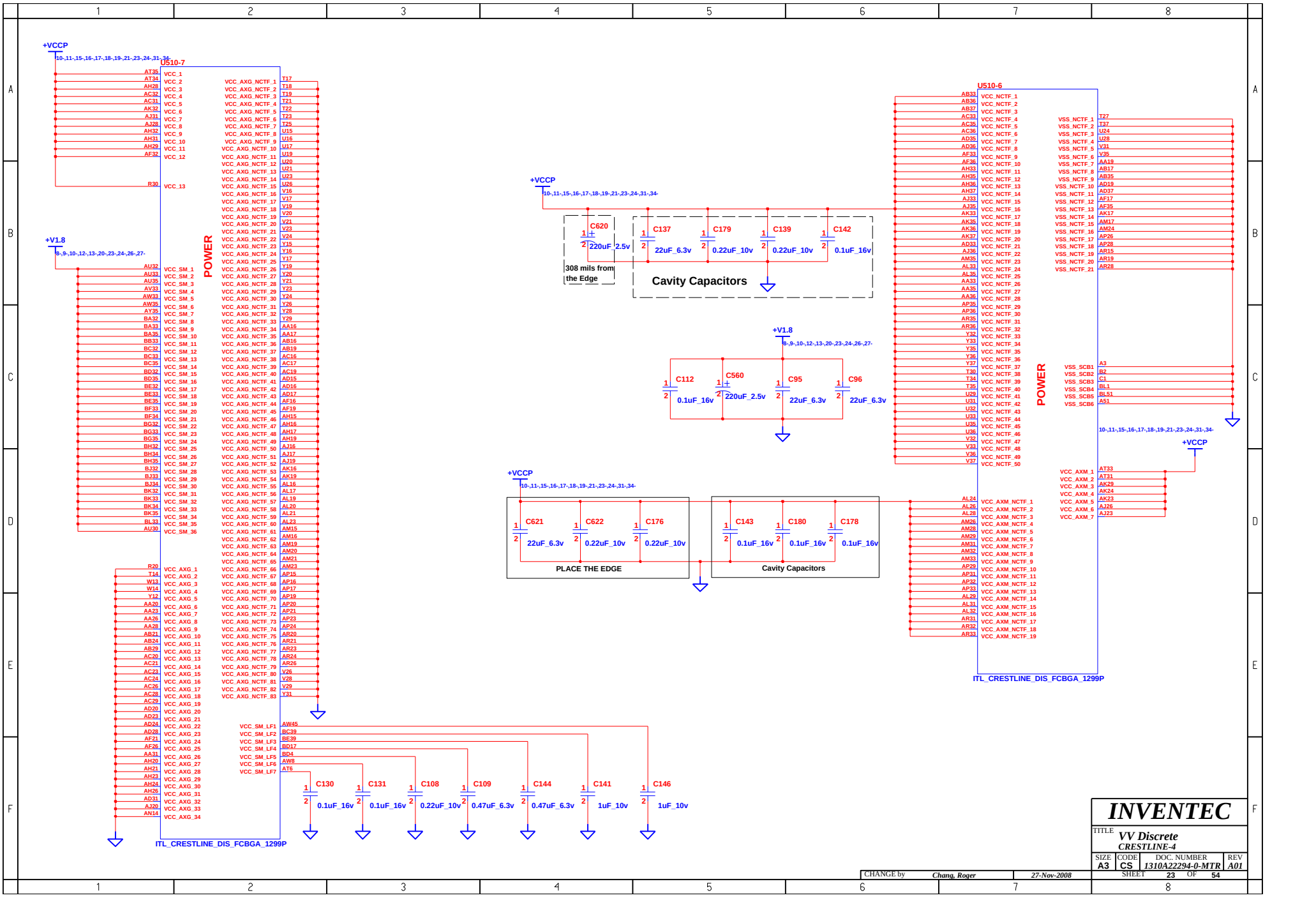
CHANGE by	Chang, Roger	27-Nov-2008

INVENTEC

TITLE: *VV Discrete*
CRESTLINE-3

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 22 OF 54



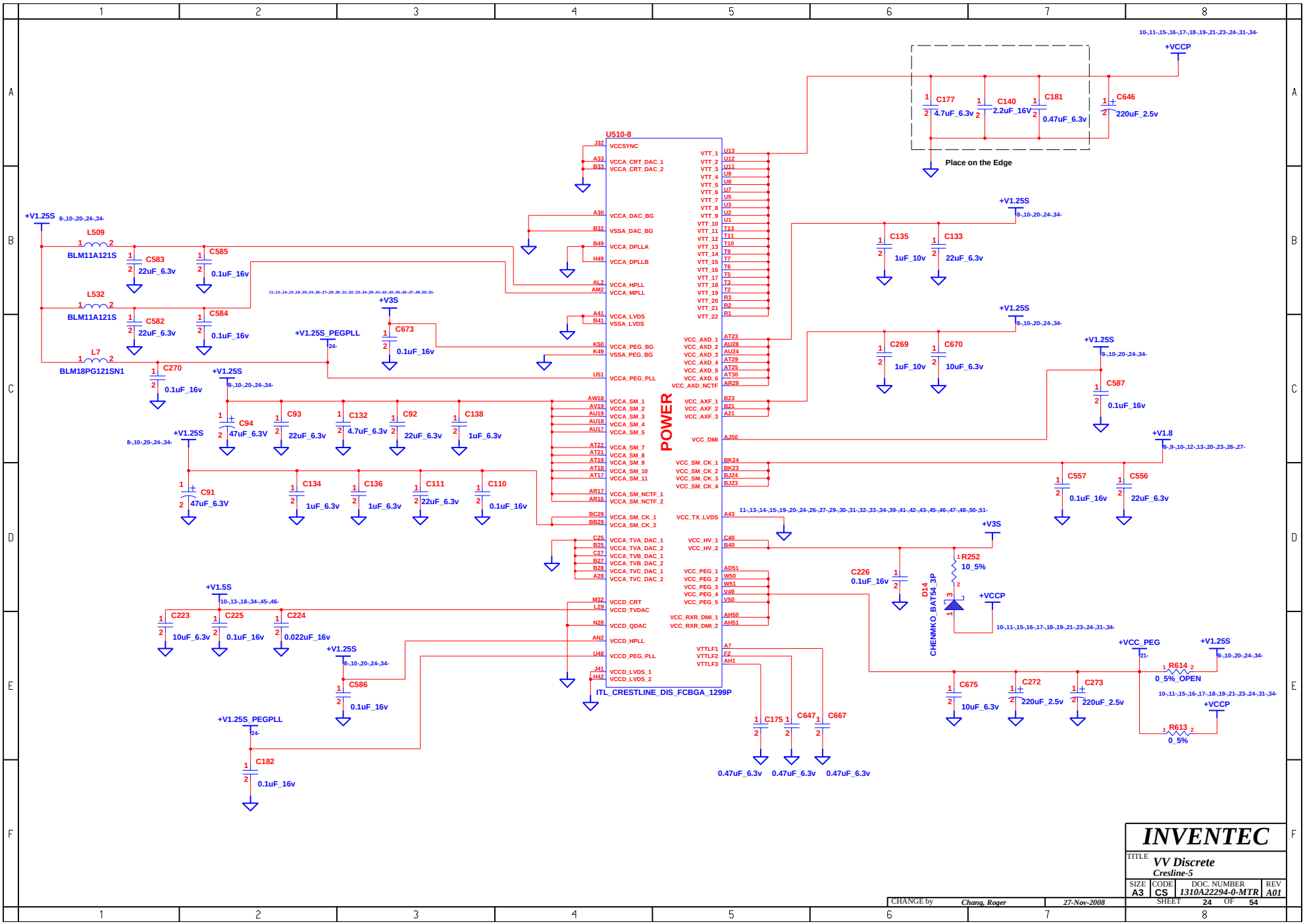
CHANGE by		
Chang, Roger	27-Nov-2008	

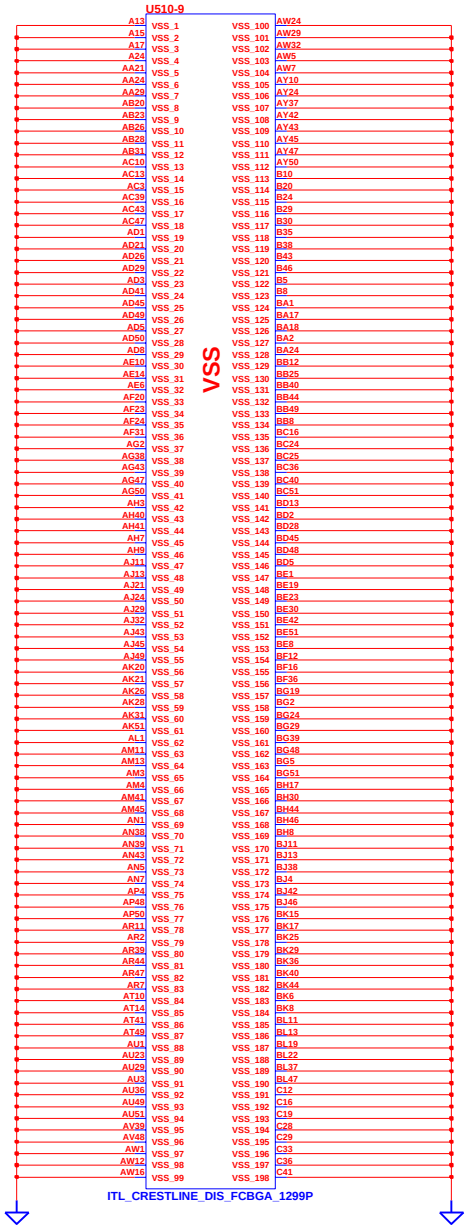
INVENTEC

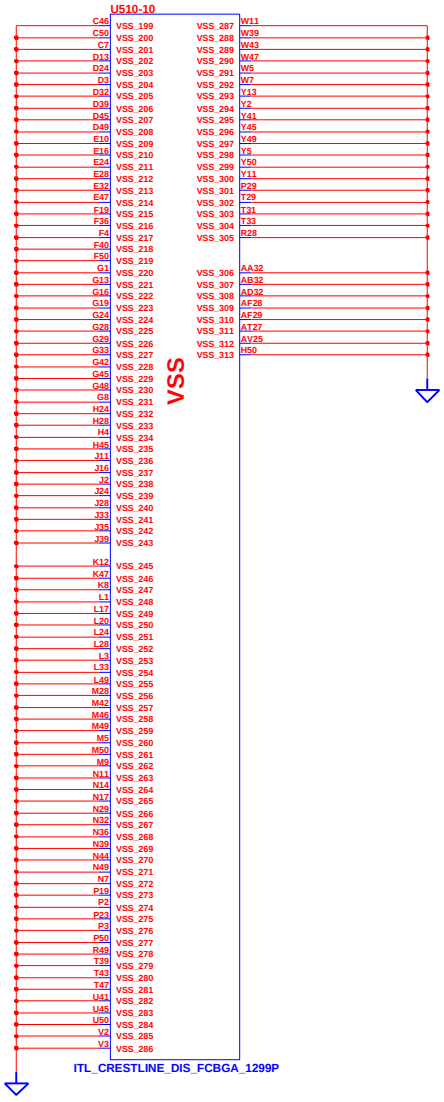
TITLE: *VV Discrete*
CRESTLINE-4

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 23 OF 54


U510-8
POWER
ITL_CRESTLINE_DIS_FCBGA_1299P
Place on the Edge
+V1.25S
+V3S
+VCCP
+V1.8
+V1.5S
+V1.25S_PEGPLL
+VCC_PEG
L509
BLM11A121S
L532
BLM11A121S
L7
BLM18PG121SN1
C583 22uF_6.3v
C585 0.1uF_16v
C582 22uF_6.3v
C584 0.1uF_16v
C270 0.1uF_16v
C673 0.1uF_16v
C94 47uF_6.3V
C93 22uF_6.3v
C132 4.7uF_6.3v
C92 22uF_6.3v
C138 1uF_6.3v
C91 47uF_6.3V
C134 1uF_6.3v
C136 1uF_6.3v
C111 22uF_6.3v
C110 0.1uF_16v
C177 4.7uF_6.3v
C140 2.2uF_16V
C181 0.47uF_6.3v
C646 220uF_2.5v
C135 1uF_10v
C133 22uF_6.3v
C269 1uF_10v
C670 10uF_6.3v
C587 0.1uF_16v
C557 0.1uF_16v
C556 22uF_6.3v
C226 0.1uF_16v
R252 10_5%
D14 CHENMKO_BAT54_3P
C675 10uF_6.3v
C272 220uF_2.5v
C273 220uF_2.5v
R614 0_5%_OPEN
R613 0_5%
C223 10uF_6.3v
C225 0.1uF_16v
C224 0.022uF_16v
C586 0.1uF_16v
C182 0.1uF_16v
C175 0.47uF_6.3v
C647 0.47uF_6.3v
C667 0.47uF_6.3v
INVENTEC
TITLE VV Discrete
Cresline-5
SIZE A3
CODE CS
DOC. NUMBER 1310A22294-0-MTR
REV A01
SHEET 24 OF 54
CHANGE by Chang, Roger 27-Nov-2008





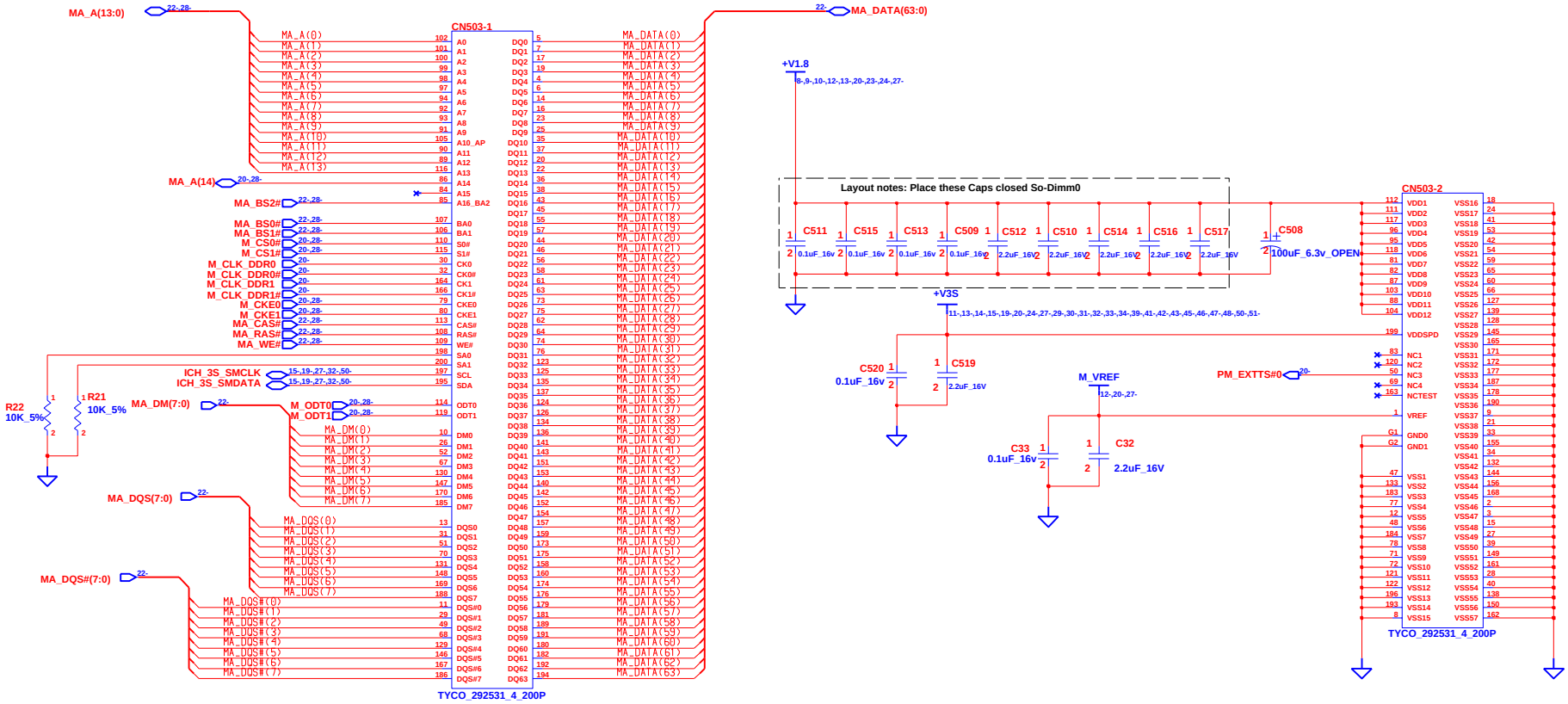
CHANGE by	Chang, Roger	27-Nov-2008

INVENTEC

TITLE: *VV Discrete*
CRESTLINE-6

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 25 OF 54



SO DIMM0_9.2mm

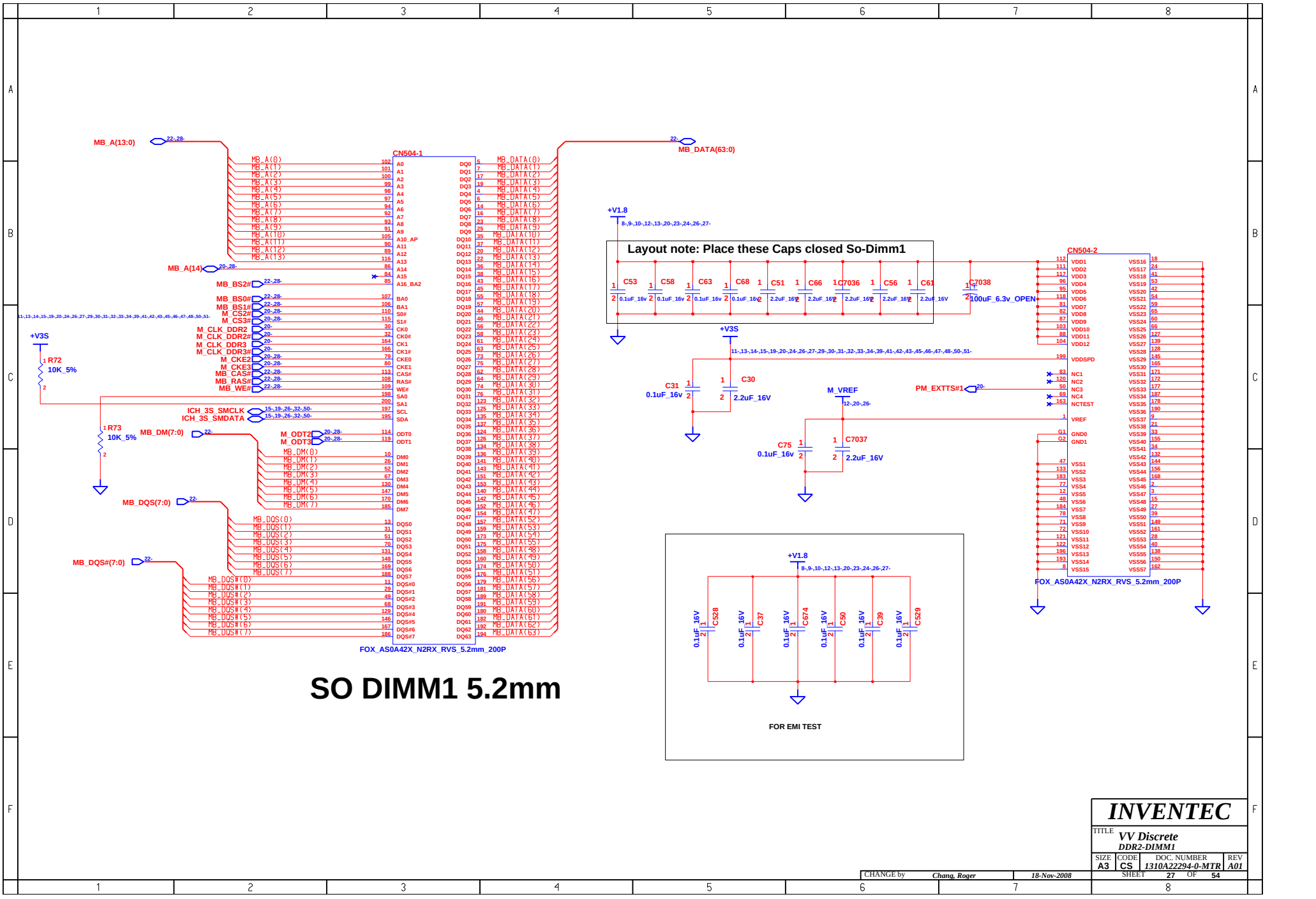
CHANGE by	Chang, Roger	25-Nov-2008	

INVENTEC

TITLE: *VV Discrete*
DDR2-DIMM-0

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 26 OF 54



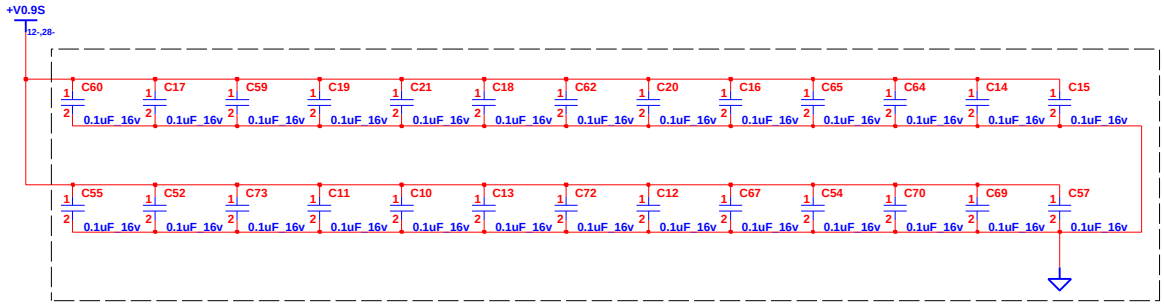
CHANGE by	Chang, Roger	18-Nov-2008	

INVENTEC

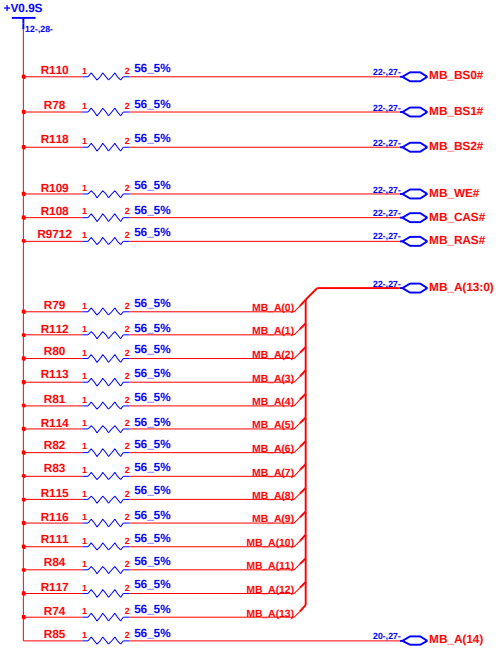
TITLE: *VV Discrete*
DDR2-DIMM1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 27 OF 54



LAYOUT NOTES : PLACE ONE CAP CLOSE TO EVERY 2 PULL UP RESISTOR TERMINATED TO +V0.9S



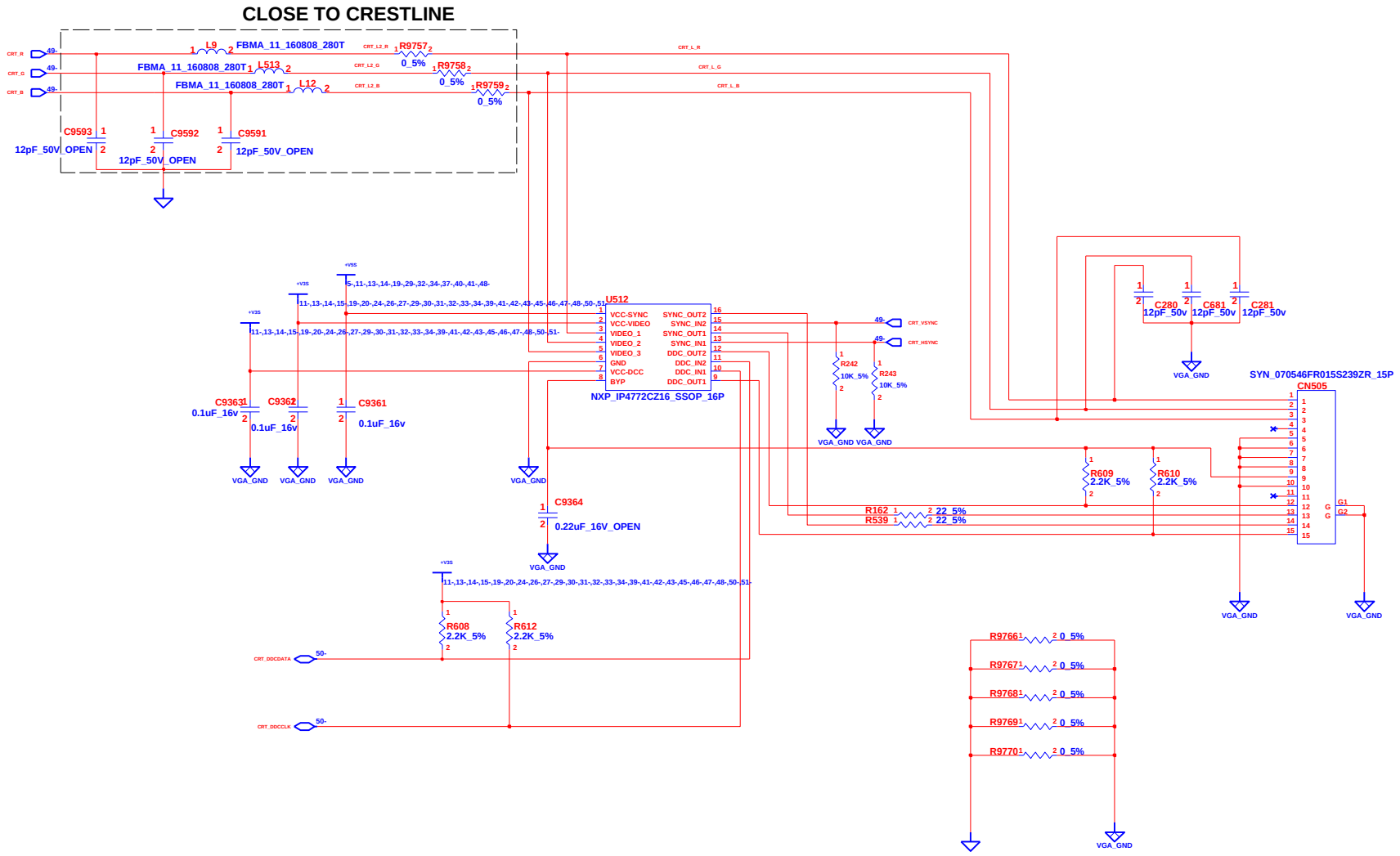
CHANGE by		
Chang, Roger		27-Sep-2003

INVENTEC

TITLE: ***VV Discrete***
DDR2-DAMPING

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTRA01*	

SHEET 28 OF 54



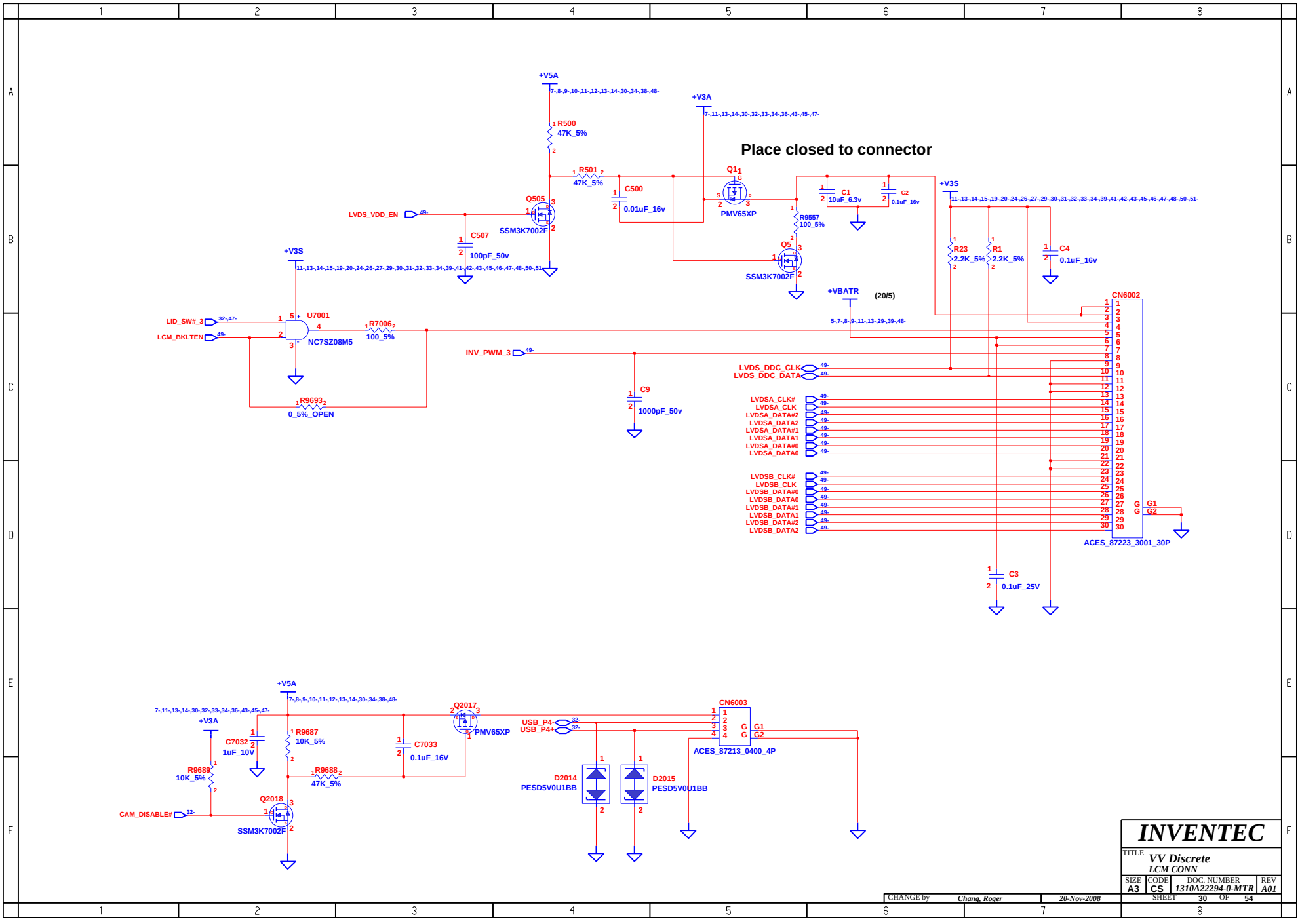
CHANGE by	Chang, Roger	25-Dec-2008

INVENTEC

TITLE: VV Discrete
VGA CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 29 OF 54



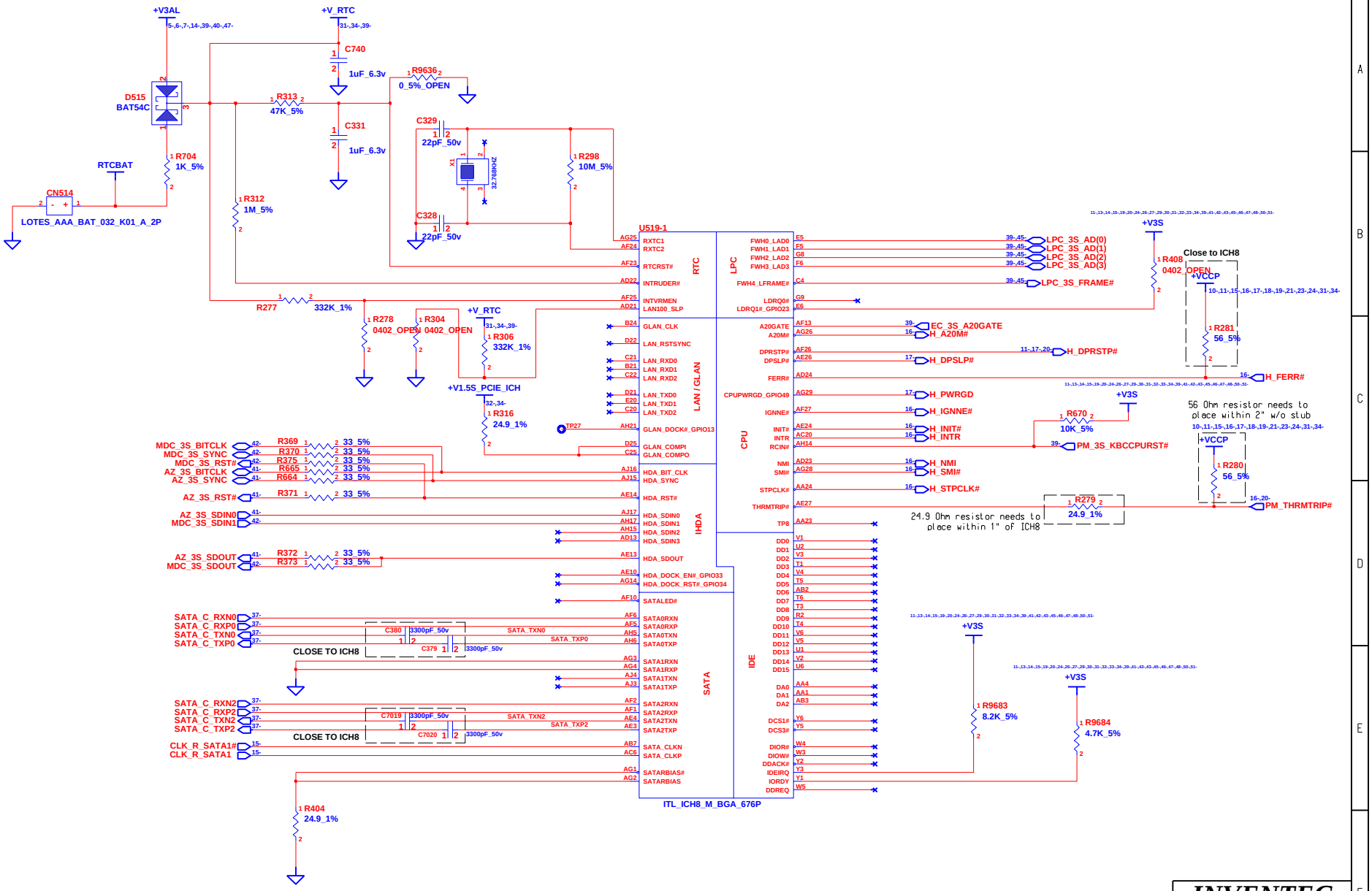
CHANGE by Chang, Roger 20-Nov-2008

INVENTEC

TITLE: *VV Discrete*
LCM CONN

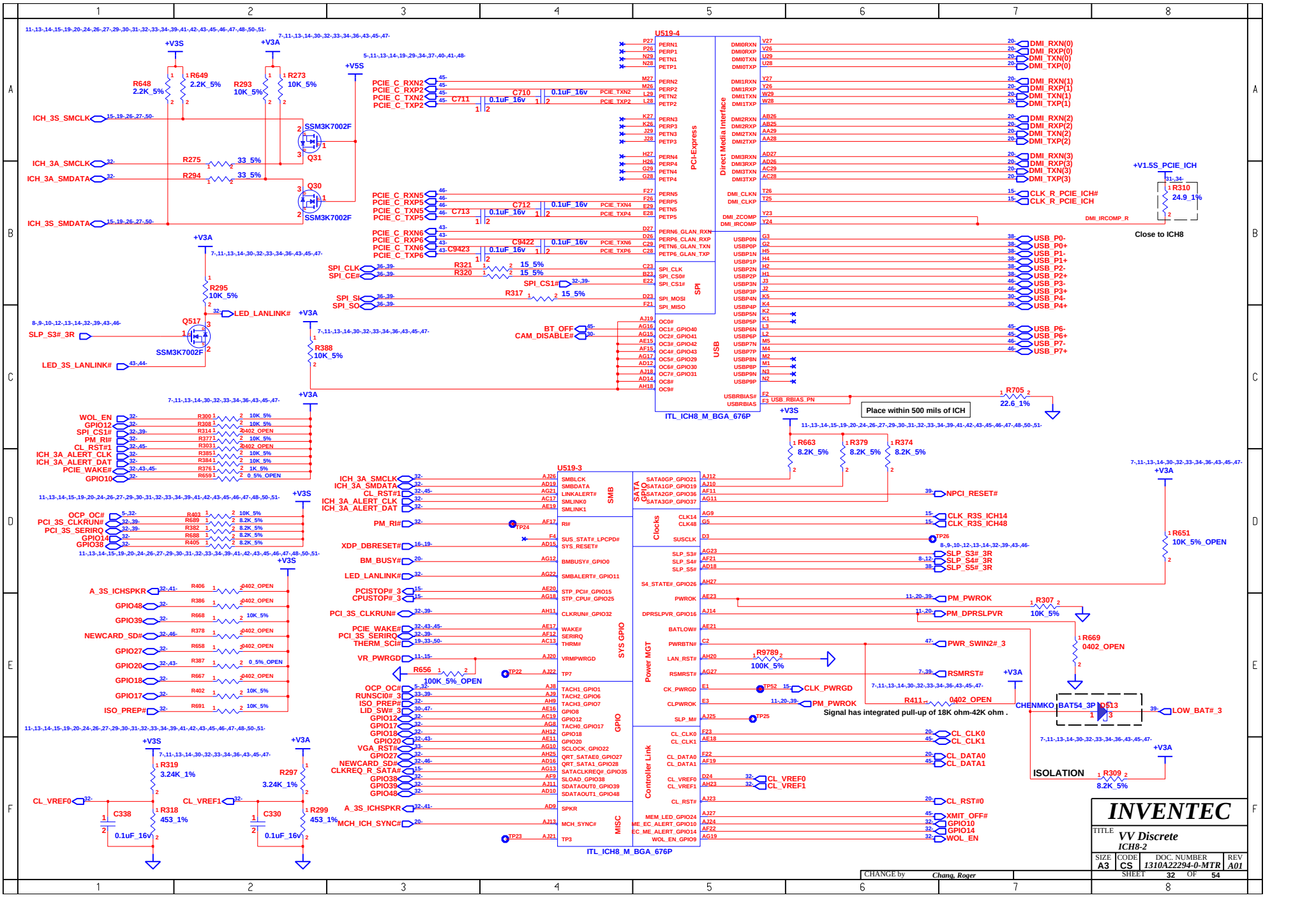
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

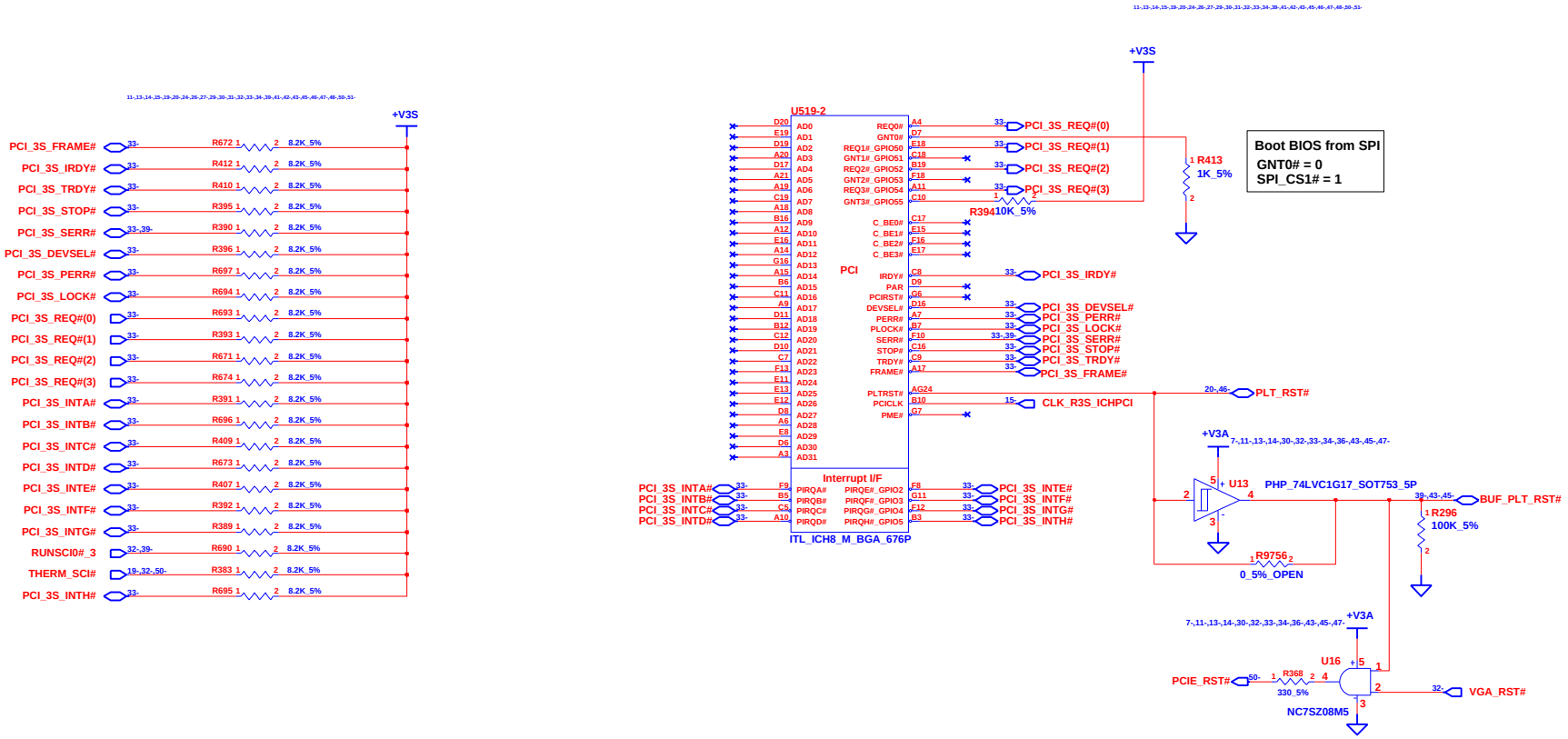
SHEET 30 OF 54



INVENTEC			
TITLE: *VV Discrete* *ICH8-1*			
SIZE: A3	CODE: CS	DOC. NUMBER: *1310A22294-0-MTR*	REV: *A01*
		SHEET 31 OF 54	

CHANGE by		
Chang, Roger	*27-Nov-2008*	


U519-4
PCI-Express
Direct Media Interface
SPI
USB
ITL_ICH8_M_BGA_676P
U519-3
SMB
SATA GPIO
Clocks
Power MGT
SYS GPIO
GPIO
Controller Link
MISC
ITL_ICH8_M_BGA_676P
Place within 500 mils of ICH
Signal has integrated pull-up of 18K ohm-42K ohm .
Close to ICH8
ISOLATION
CHENMKO BAT54_3P SD13
INVENTEC
VV Discrete
ICH8-2
SIZE A3
CODE CS
DOC. NUMBER 1310A22294-0-MTR
REV A01
SHEET 32 OF 54
CHANGE by Chang, Roger



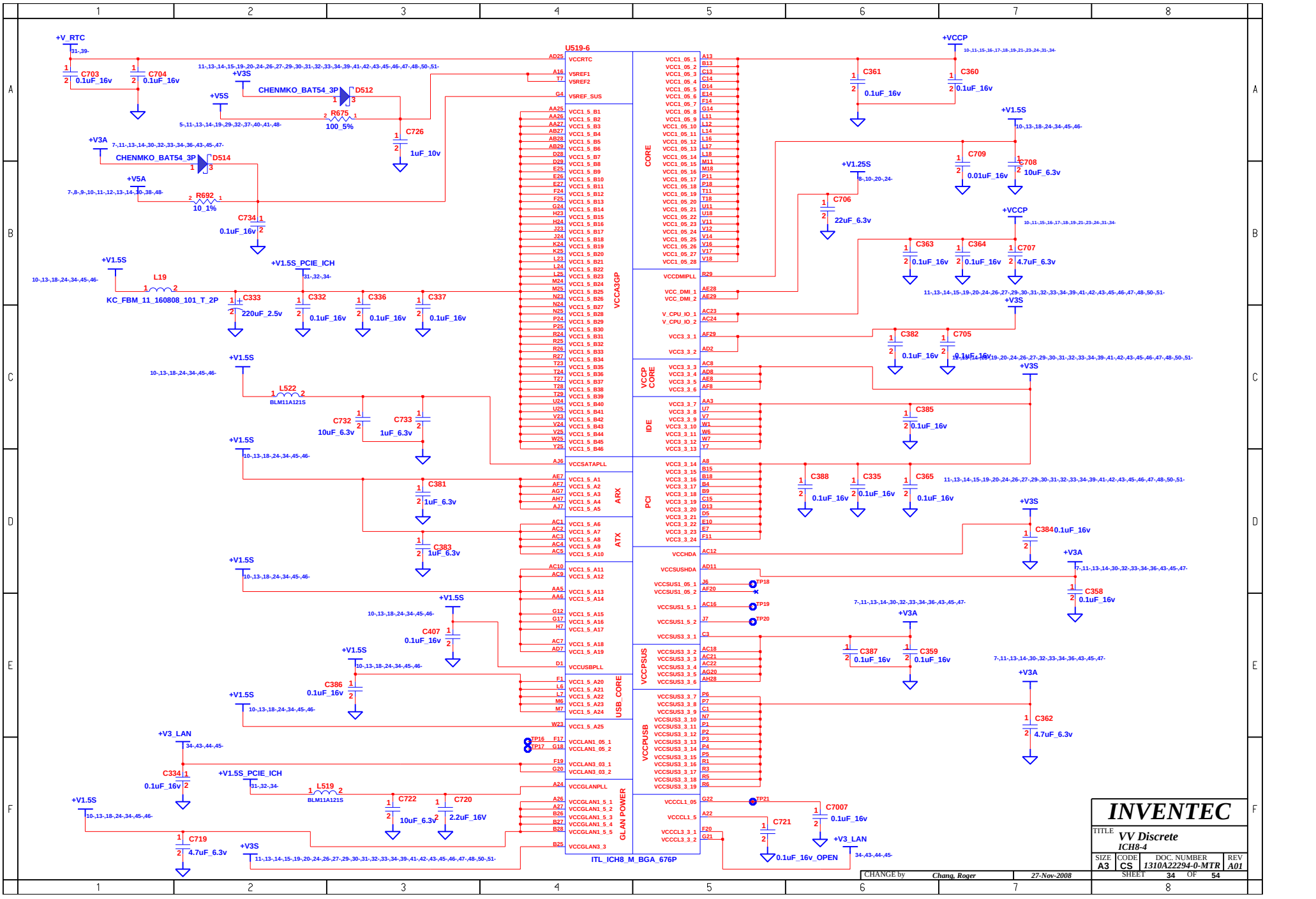
CHANGE by		
Chang, Roger		*27-Nov-2008*

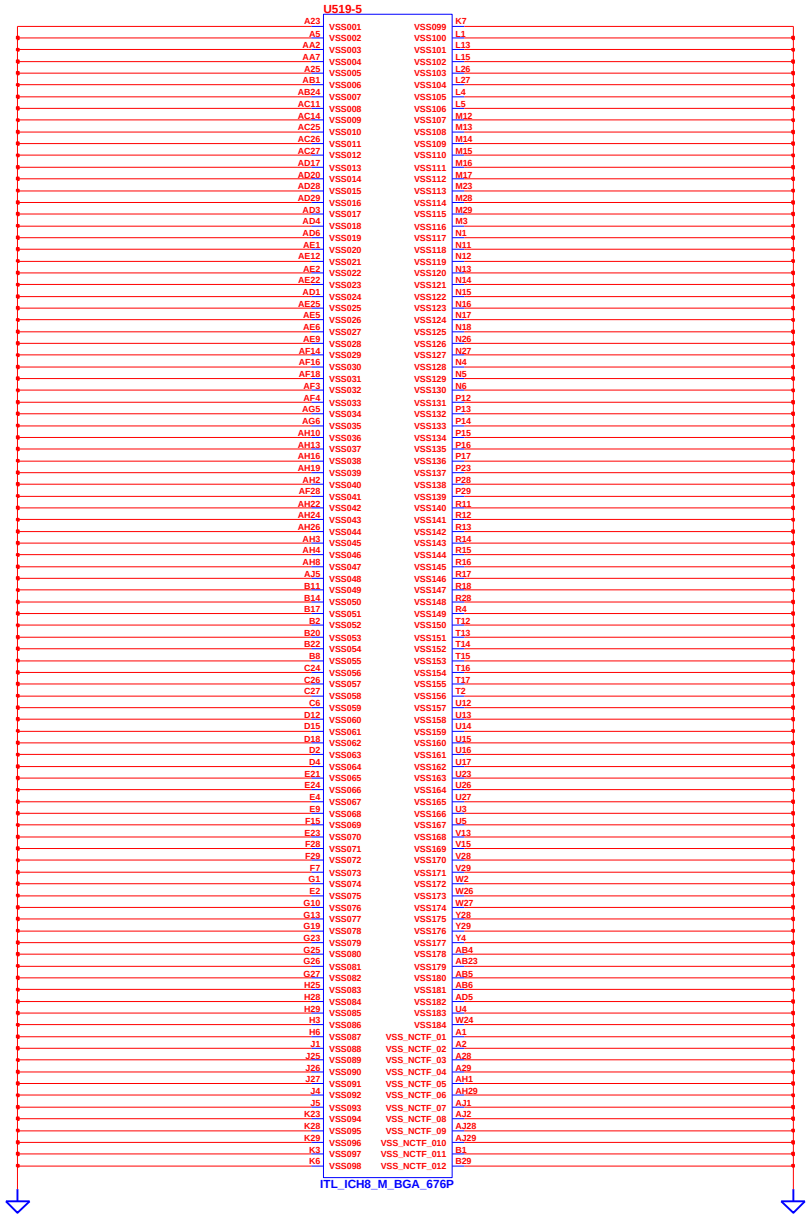
INVENTEC

TITLE: *VV Discrete*
ICH8-3

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 33 OF 54


U519-6
ITL_ICH8_M_BGA_676P
CORE
VCCA3GP
VCCP CORE
IDE
PCI
ARX
ATX
USB_CORE
VCCPSUS
VCCPLSB
GLAN POWER
+V_RTC
+V3S
+V5S
+V3A
+V5A
+V1.5S
+V1.5S_PCIE_ICH
+V3_LAN
+VCCP
+V1.25S
CHENMKO_BAT54_3P
D512
D514
R675
100_5%
R692
10_1%
L19
KC_FBM_11_160808_101_T_2P
L522
BLM11A121S
L519
C703 0.1uF_16v
C704 0.1uF_16v
C726 1uF_10v
C734 0.1uF_16v
C333 220uF_2.5v
C332 0.1uF_16v
C336 0.1uF_16v
C337 0.1uF_16v
C732 10uF_6.3v
C733 1uF_6.3v
C381 1uF_6.3v
C383 1uF_6.3v
C407 0.1uF_16v
C386 0.1uF_16v
C334 0.1uF_16v
C722 10uF_6.3v
C720 2.2uF_16v
C719 4.7uF_6.3v
C361 0.1uF_16v
C360 0.1uF_16v
C709 0.01uF_16v
C708 10uF_6.3v
C706 22uF_6.3v
C363 0.1uF_16v
C364 0.1uF_16v
C707 4.7uF_6.3v
C382 0.1uF_16v
C705 0.1uF_16v
C385 0.1uF_16v
C388 0.1uF_16v
C335 0.1uF_16v
C365 0.1uF_16v
C384 0.1uF_16v
C358 0.1uF_16v
C387 0.1uF_16v
C359 0.1uF_16v
C362 4.7uF_6.3v
C7007 0.1uF_16v
C721 0.1uF_16v_OPEN
TP16
TP17
TP18
TP19
TP20
TP21
INVENTEC
TITLE
VV Discrete
ICH8-4
SIZE A3
CODE CS
DOC. NUMBER 1310A22294-0-MTR
REV A01
SHEET 34 OF 54
CHANGE by Chang, Roger
27-Nov-2008



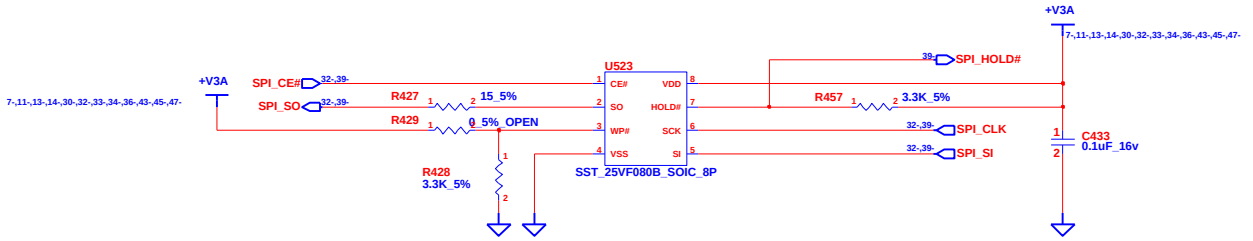
CHANGE by		
Chang, Roger		*27-Nov-2008*

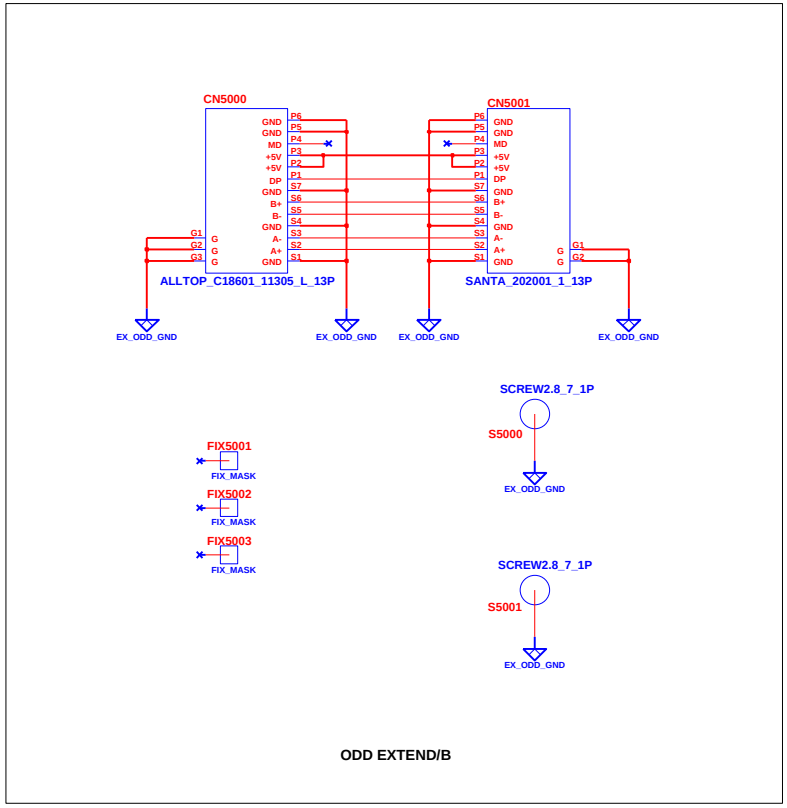
INVENTEC

TITLE: ***VV Discrete***
ICH8-5

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 35 OF 54





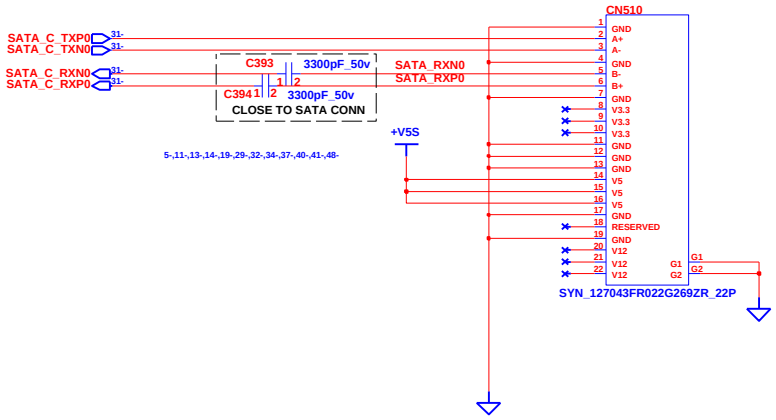
CHANGE by	Chang, Roger	27-Nov-2008	

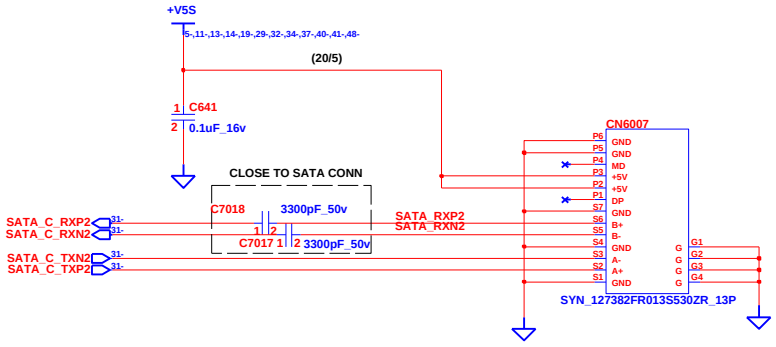
INVENTEC

TITLE: *VV Discrete*
SYSTEM BIOS

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 36 OF 54





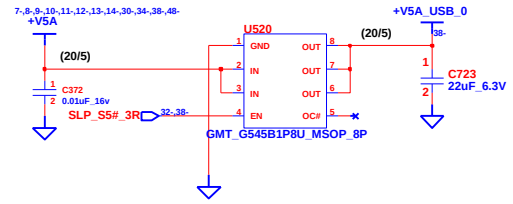
CHANGE by	*Chang, Roger*	*18-Nov-2008*		

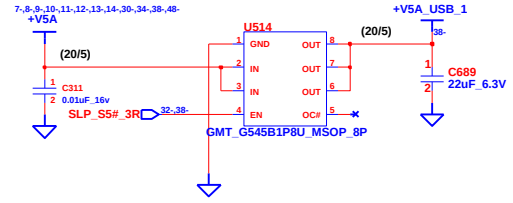
INVENTEC

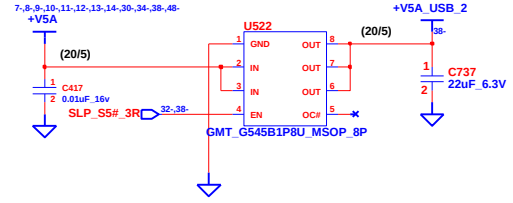
TITLE: ***VV Discrete***
HDD & ODD CONN

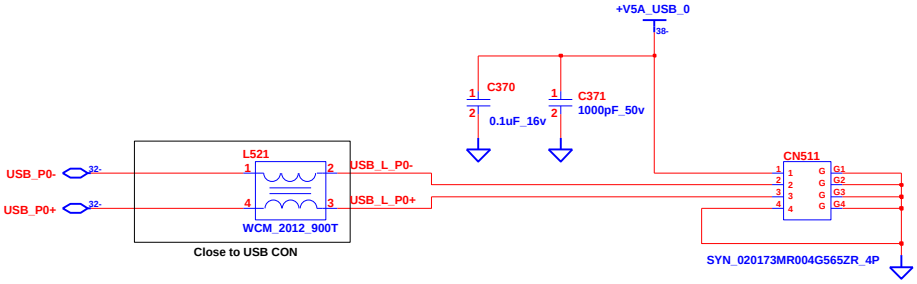
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

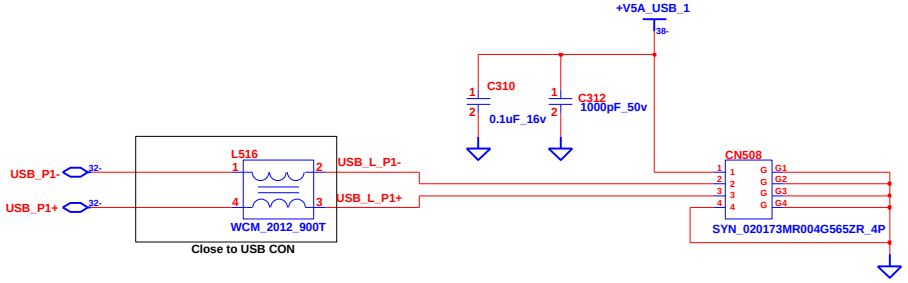
SHEET 37 OF 54

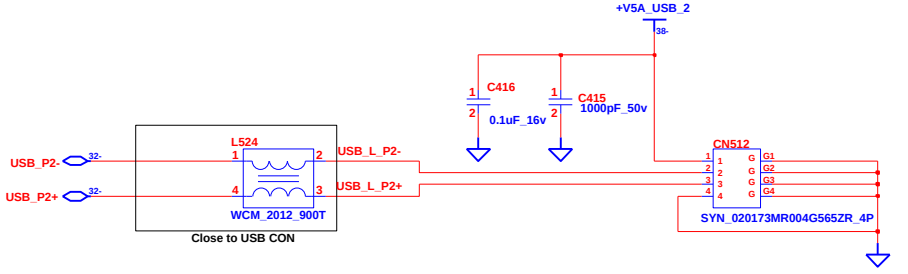












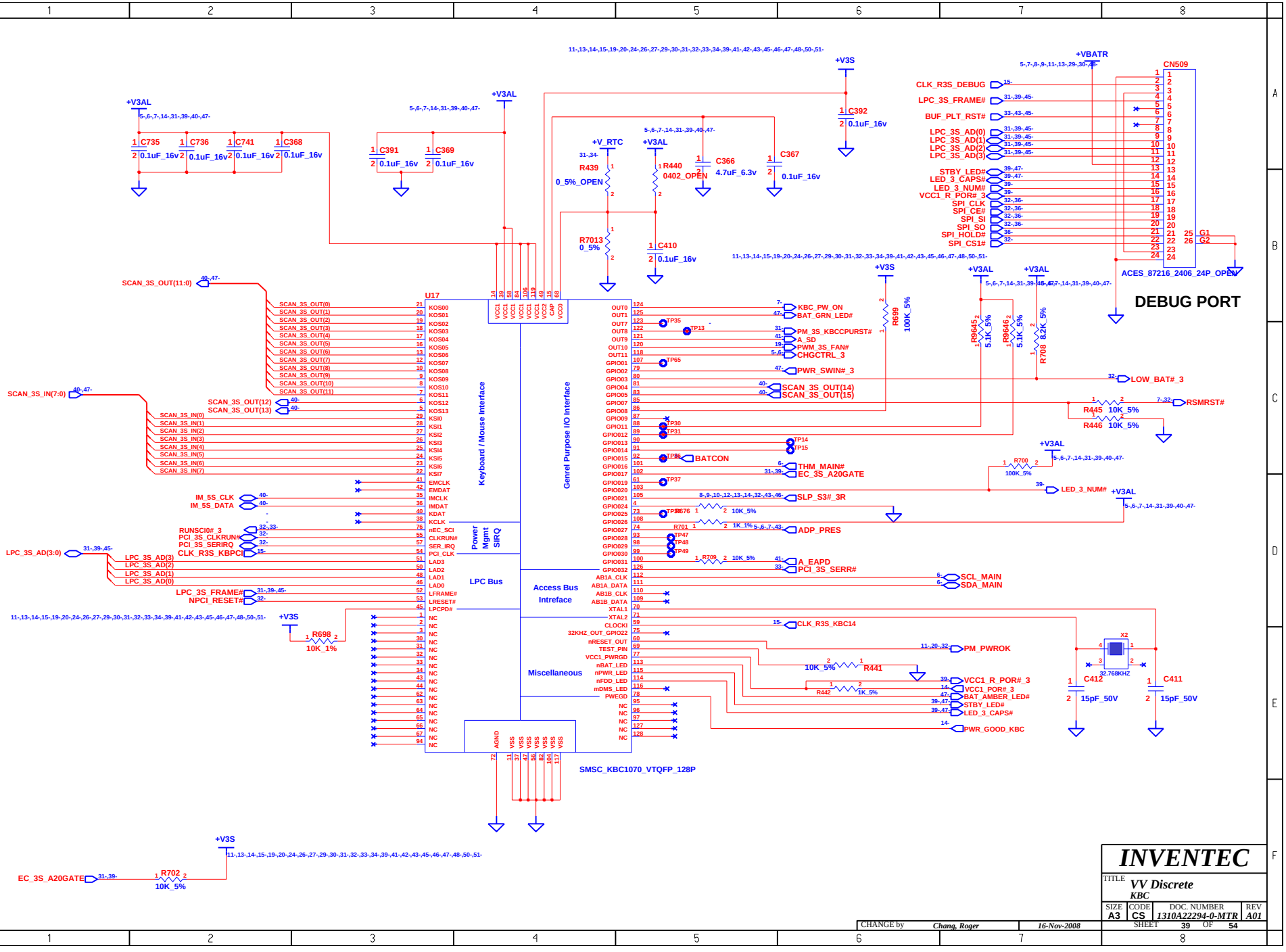
CHANGE by	Chang, Roger	4-Nov-2008

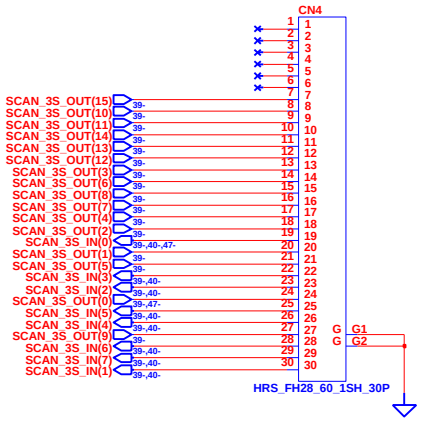
INVENTEC

TITLE: *VV Discrete*
USB CONN

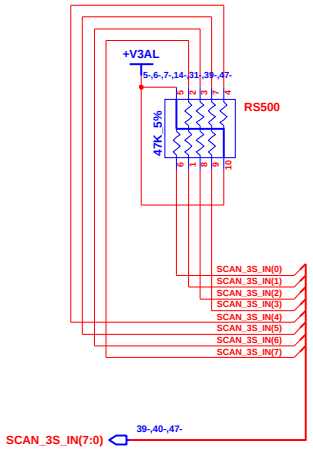
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

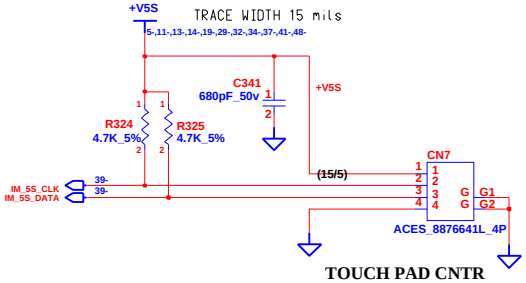
SHEET 38 OF 54


DEBUG PORT
U17
SMSC_KBC1070_VTQFP_128P
Keyboard / Mouse Interface
Genrel Purpose I/O Interface
Power Mgmt SIRQ
LPC Bus
Access Bus Intreface
Miscellaneous
ACES_87216_2406_24P_OPEN
CN509
BATCON
SLP_S3#_3R
ADP_PRES
PM_PWROK
PWR_GOOD_KBC
RSMRST#
LOW_BAT#_3
SCL_MAIN
SDA_MAIN
INVENTEC
VV Discrete
KBC
1310A22294-0-MTR
A01
A3
CS
Chang, Roger
16-Nov-2008
SHEET 39 OF 54



KEYBOARD CONN





TOUCH PAD CNTR

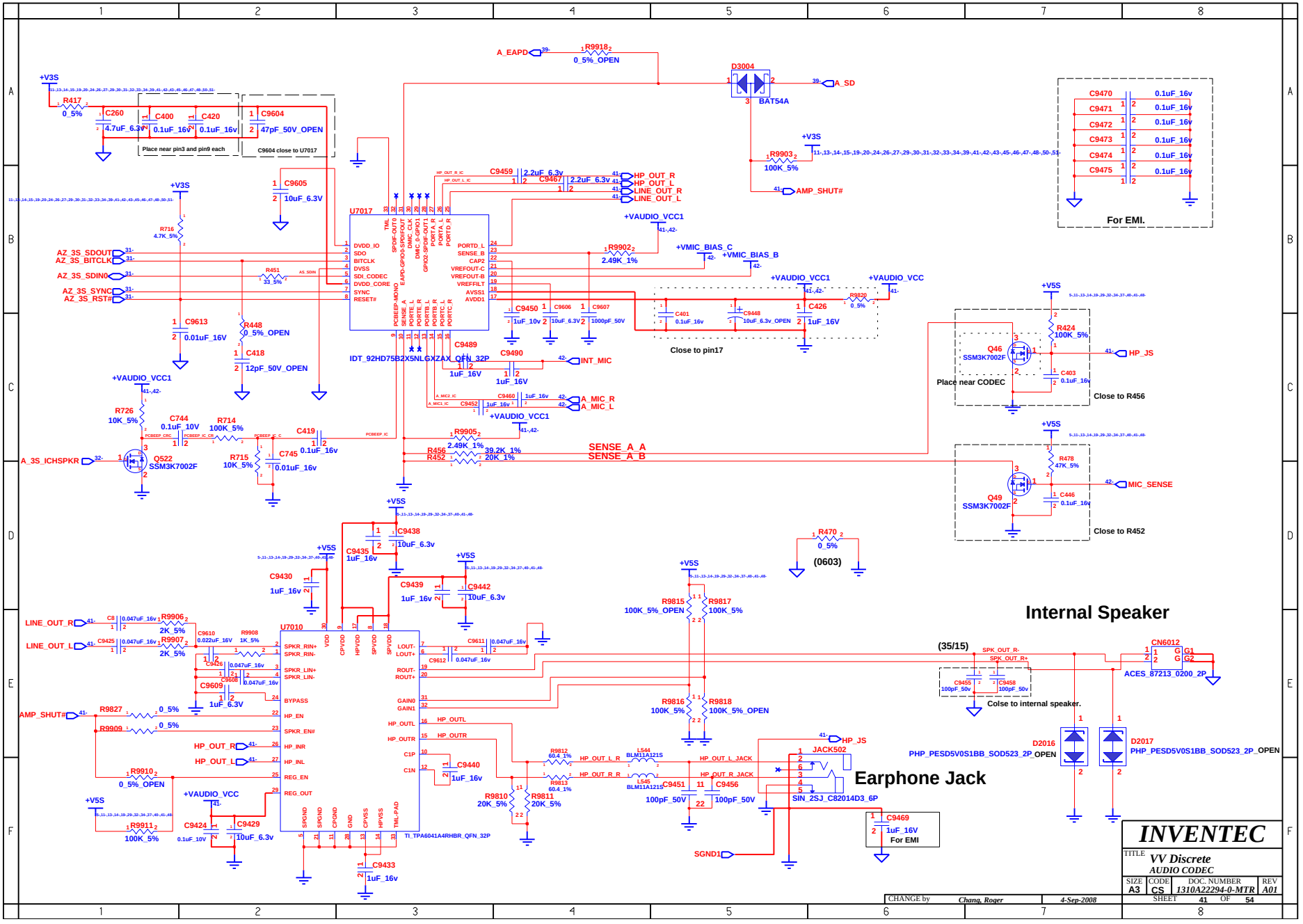
CHANGE by	*Chang, Roger*	*15-Dec-2008*	

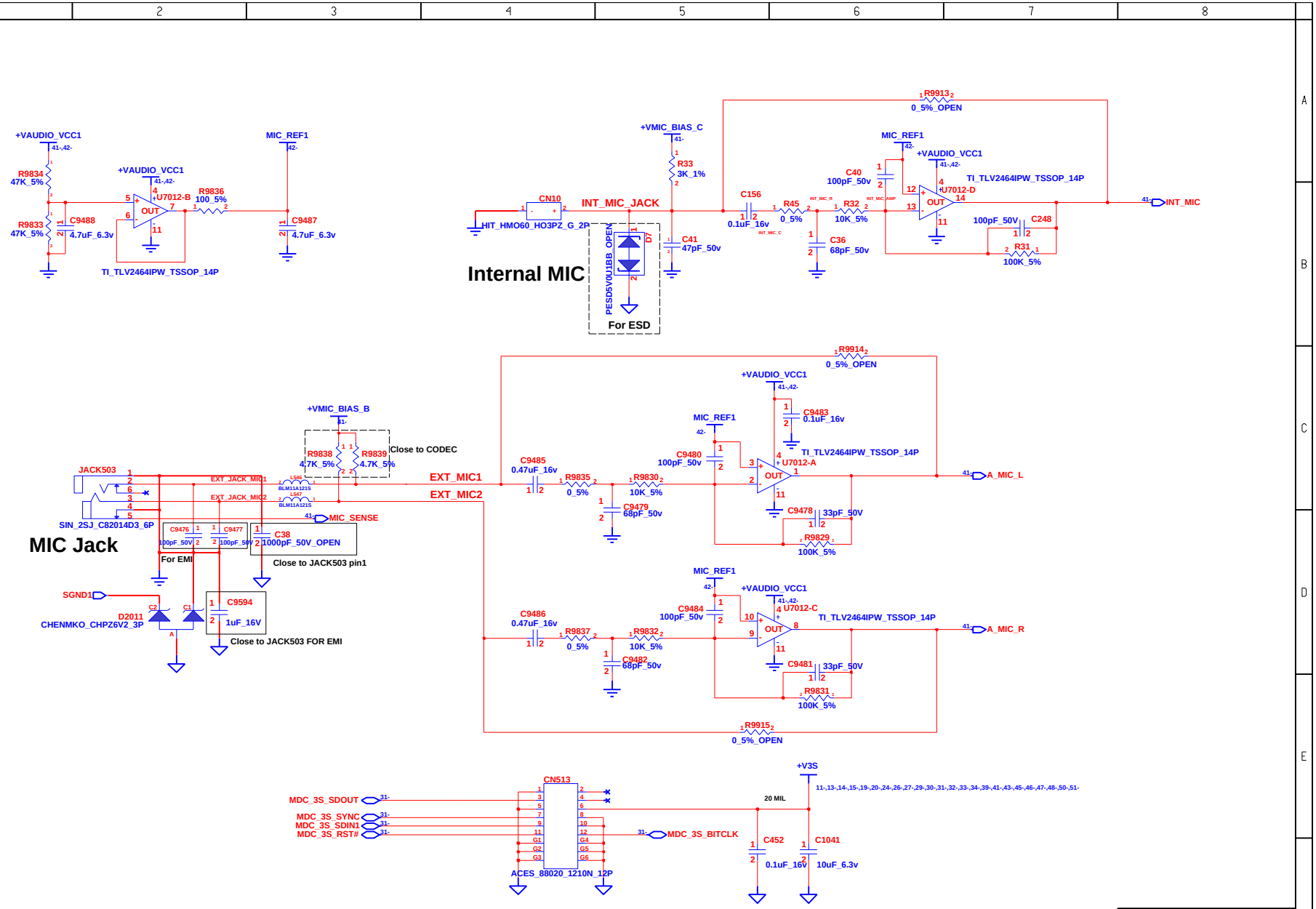
INVENTEC

TITLE: ***VV Discrete***
KB & TP CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

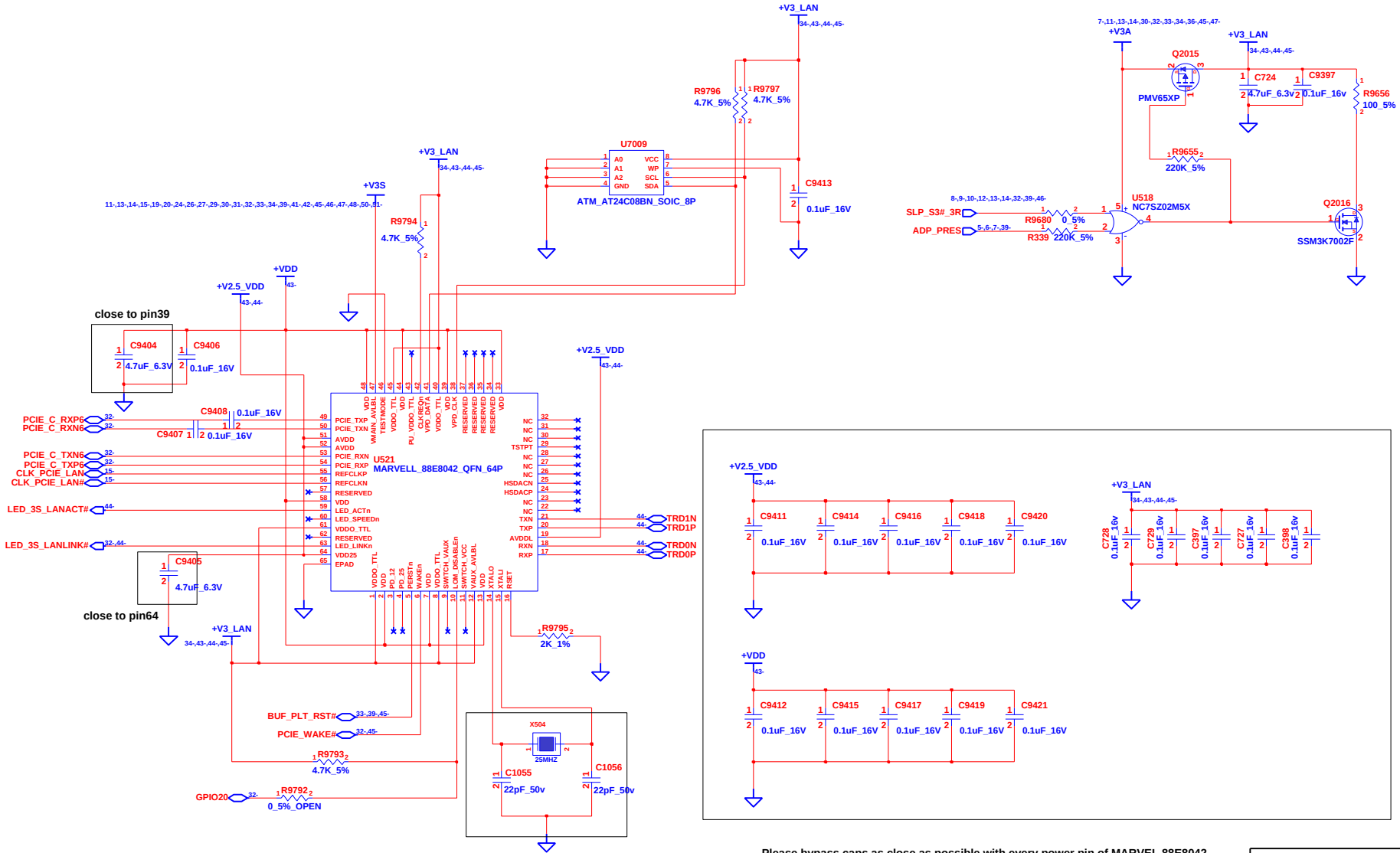
SHEET 40 OF 54


U7017
IDT_92HD75B2X5NLGXZAX_QFN_32P
U7010
TI_TPA6041A4RHBR_QFN_32P
Q522
SSM3K7002F
Q46
SSM3K7002F
Q49
SSM3K7002F
D3004
BAT54A
JACK502
SIN_2SJ_C82014D3_6P
CN6012
ACES_87213_0200_2P
D2016
PHP_PESD5V0S1BB_SOD523_2P_OPEN
D2017
PHP_PESD5V0S1BB_SOD523_2P_OPEN
Internal Speaker
Earphone Jack
For EMI.
Place near pin3 and pin9 each
C9604 close to U7017
Close to pin17
Place near CODEC
Close to R456
Close to R452
Colse to internal speaker.
A_EAPD
A_SD
AMP_SHUT#
HP_OUT_R
HP_OUT_L
LINE_OUT_R
LINE_OUT_L
INT_MIC
A_MIC_R
A_MIC_L
HP_JS
MIC_SENSE
SENSE_A_A
SENSE_A_B
AZ_3S_SDOUT
AZ_3S_BITCLK
AZ_3S_SDIN0
AZ_3S_SYNC
AZ_3S_RST#
A_3S_ICHSPKR
+V3S
+V5S
+VAUDIO_VCC
+VAUDIO_VCC1
+VMIC_BIAS_C
+VMIC_BIAS_B
SGND1
INVENTEC
VV Discrete
AUDIO CODEC
1310A22294-0-MTR
A01
Chang, Roger
4-Sep-2008
41
54



INVENTEC			
TITLE	VV Discrete MDC CNTR		
SIZE A3	CODE CS	DOC. NUMBER 1310A22294-0-MTR	REV A01
		SHEET 42 OF 54	

CHANGE by Chang, Roger 14-Oct-2008



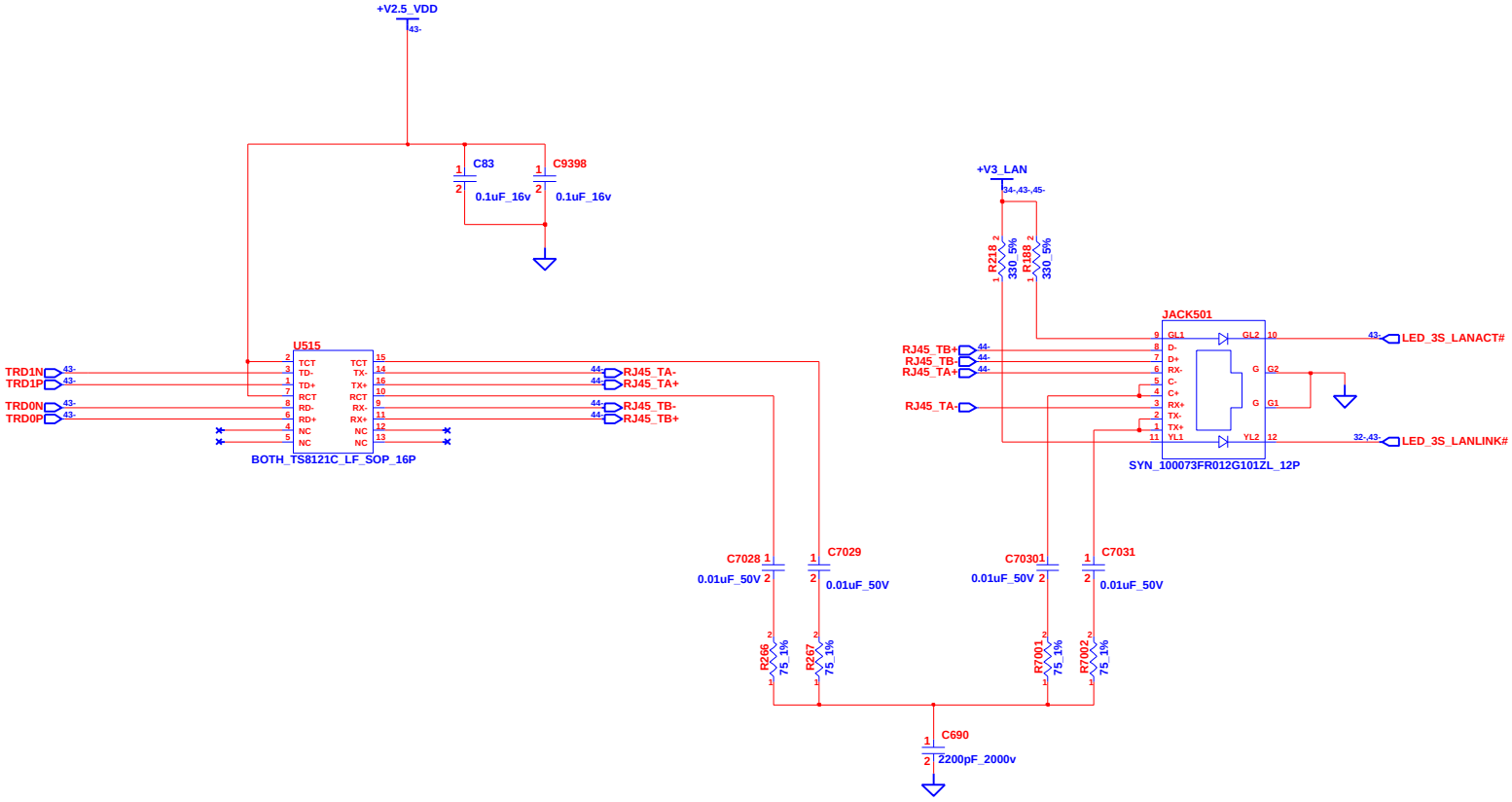
CHANGE by		
Chang, Roger		16-Nov-2008

INVENTEC

TITLE: *VV Discrete*
NIC 10/100- CONTROLLER

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 43 OF 54



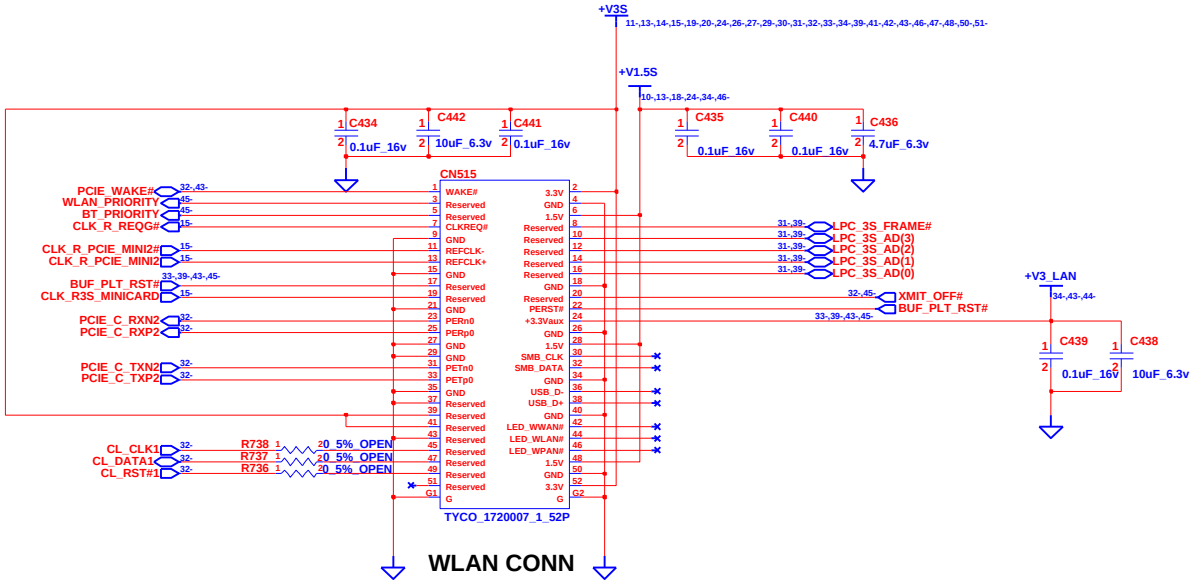
CHANGE by		
Chang, Roger	4-Nov-2008	

INVENTEC

TITLE: *VV Discrete*
NIC 10/100- RJ45

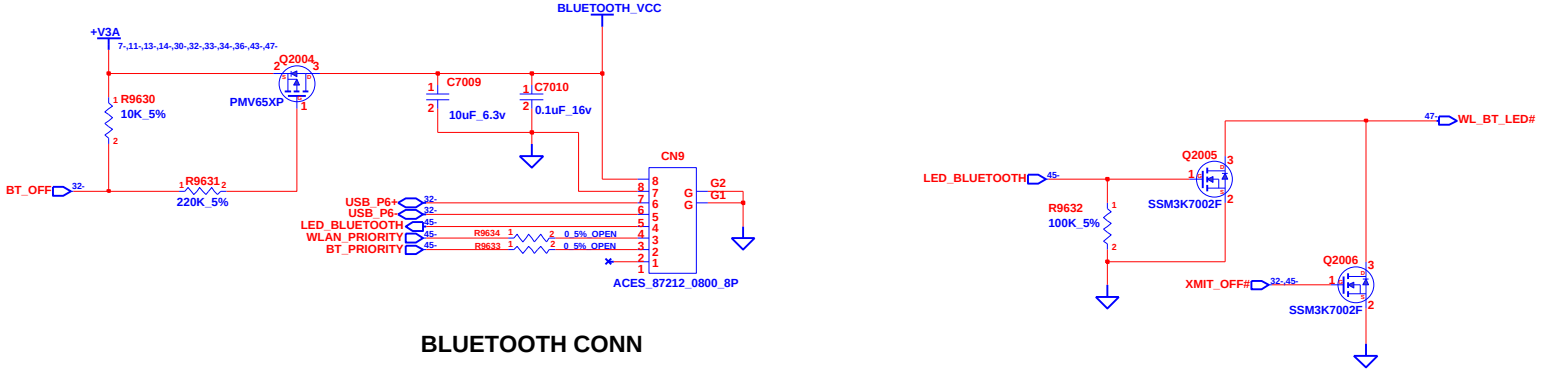
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 44 OF 54



WLAN CONN

R261,R262,R263,R264,R265 place as close to LPC signal as possible to minimize stub length for LPC bus (will be NI for FCS)



BLUETOOTH CONN

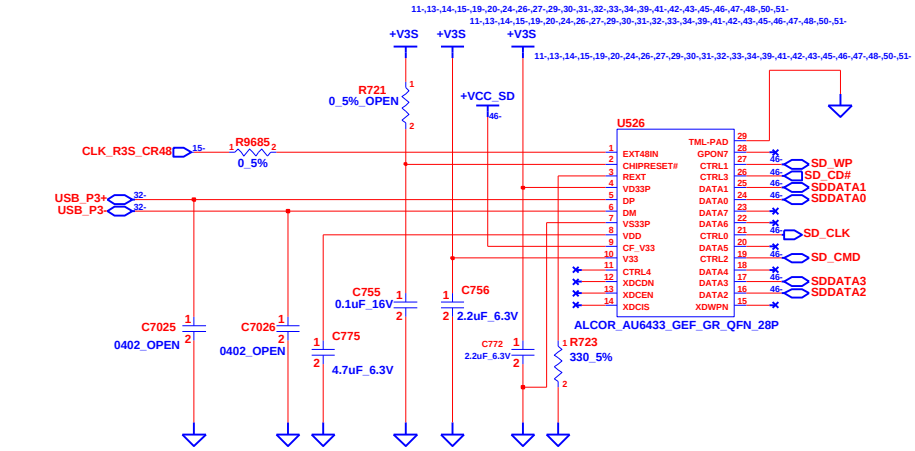
CHANGE by	Chang, Roger
	5-Nov-2008

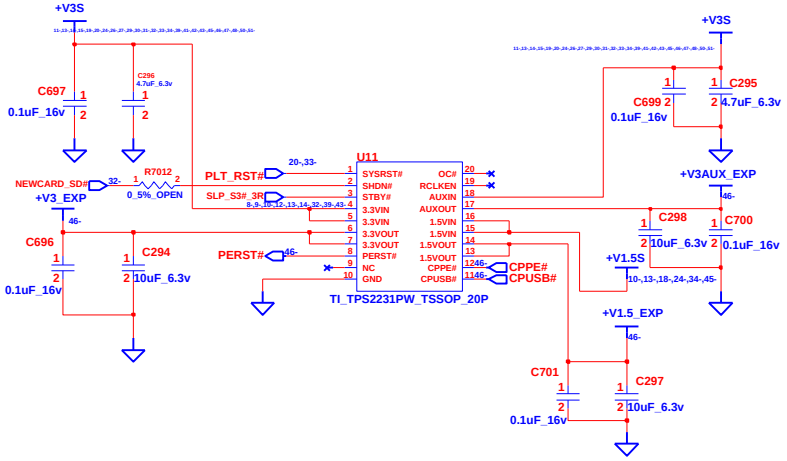
INVENTEC

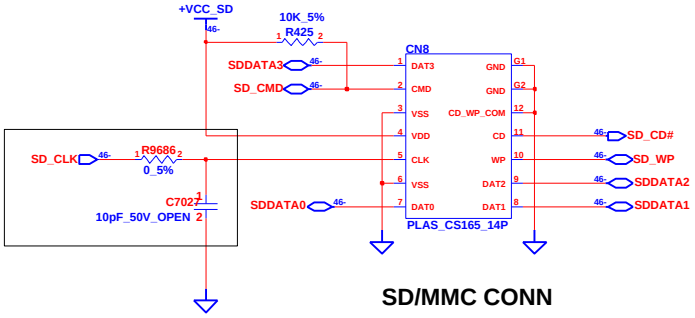
TITLE: *VV Discrete*
MINICARD CONN & BLUETOOTH

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

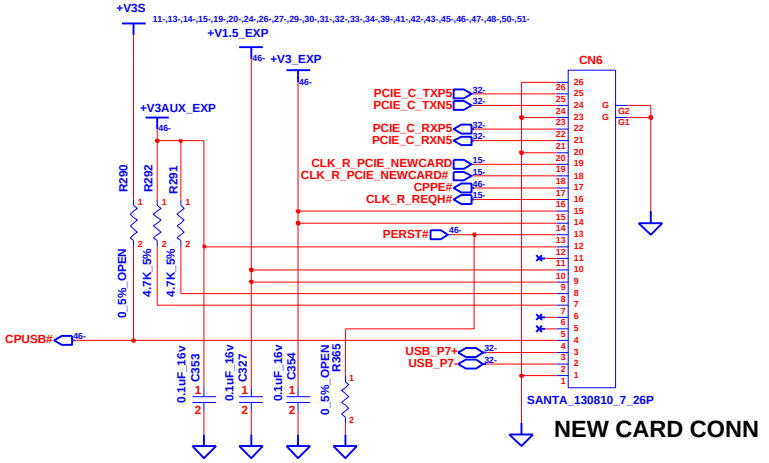
SHEET 45 OF 54



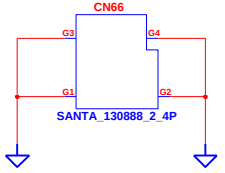




SD/MMC CONN



NEW CARD CONN



NEW CARD HOUSING

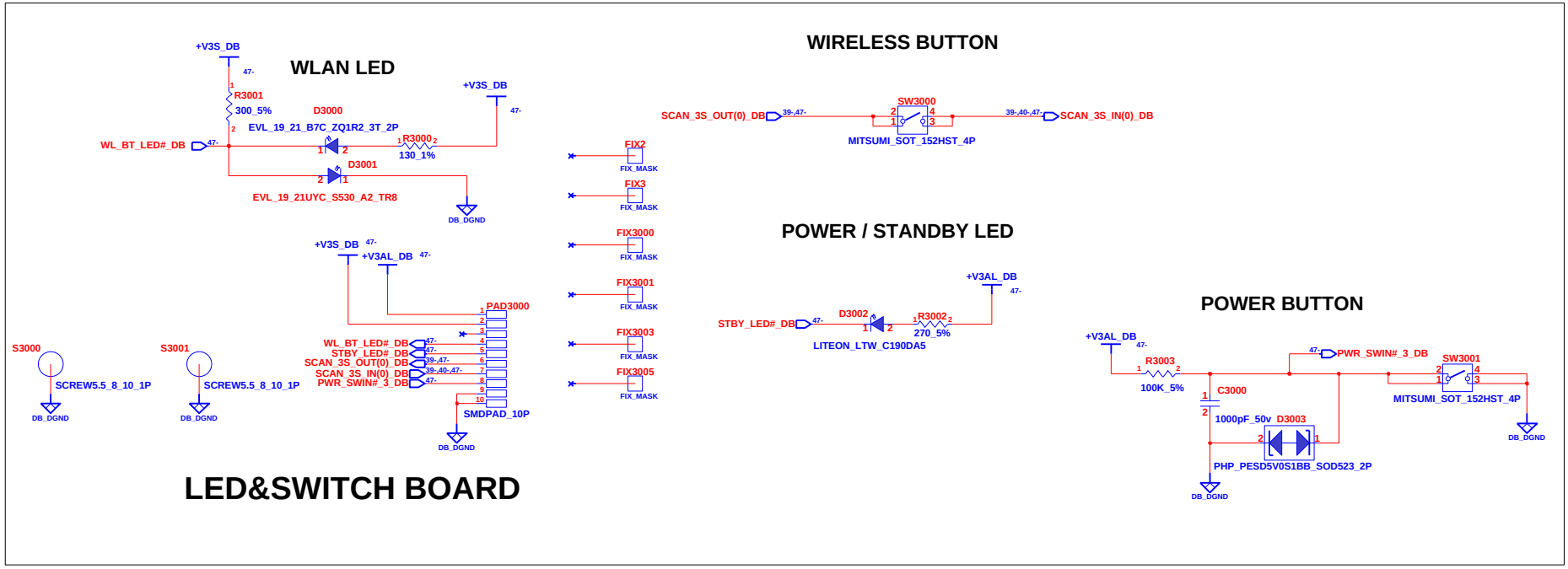
CHANGE by	Chang, Roger	20-Nov-2008	

INVENTEC

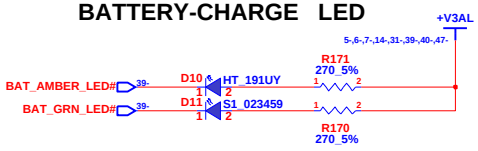
TITLE: *VV Discrete*
NEW CARD & SD/MMC

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

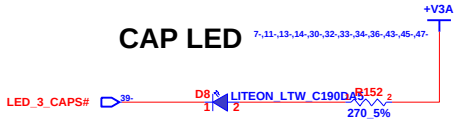
SHEET 46 OF 54



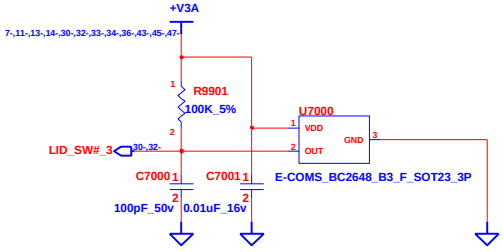
BATTERY-CHARGE LED

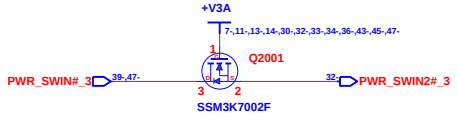


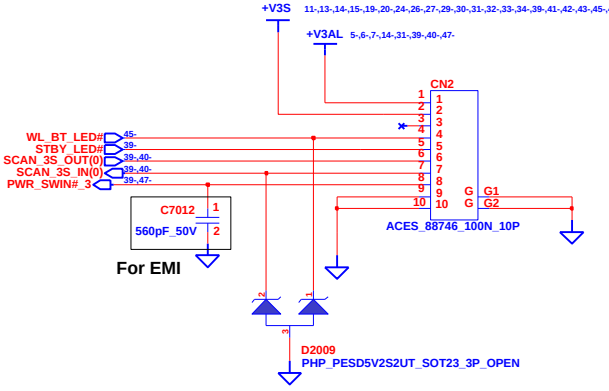
CAP LED



LID SWITCH







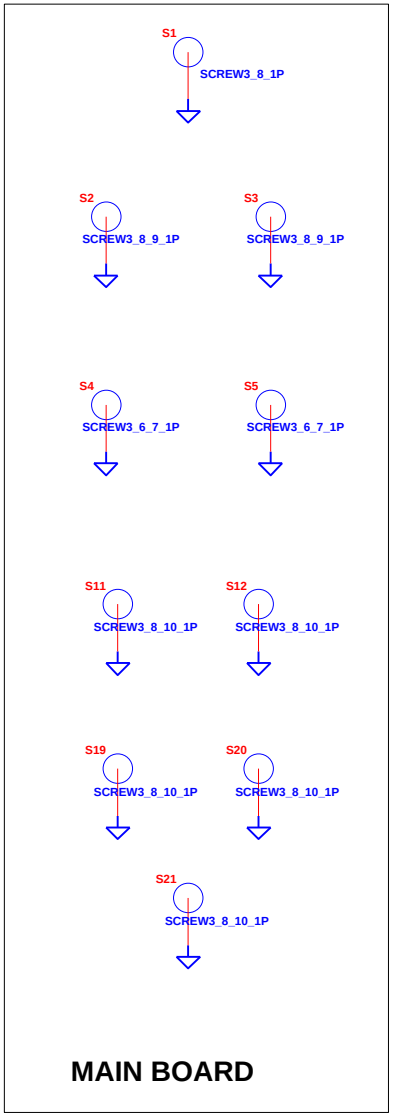
CHANGE by		
Chang, Roger		25-Dec-2008

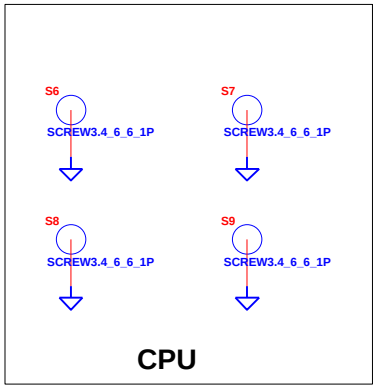
INVENTEC

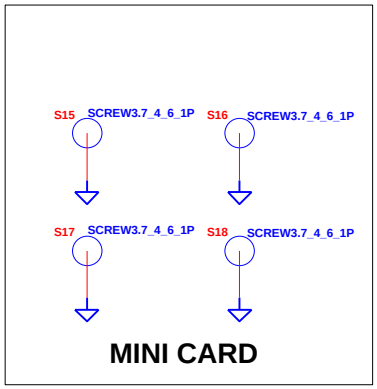
TITLE: *VV Discrete*
BUTTON & LED

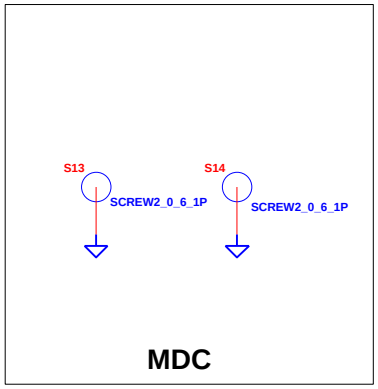
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

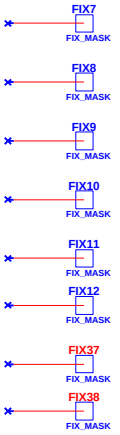
SHEET 47 OF 54

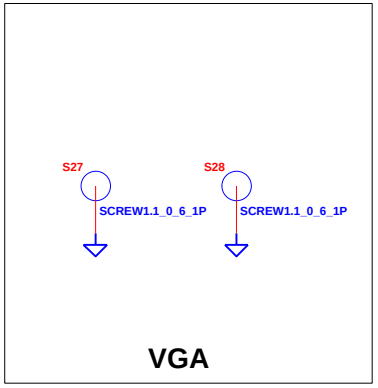


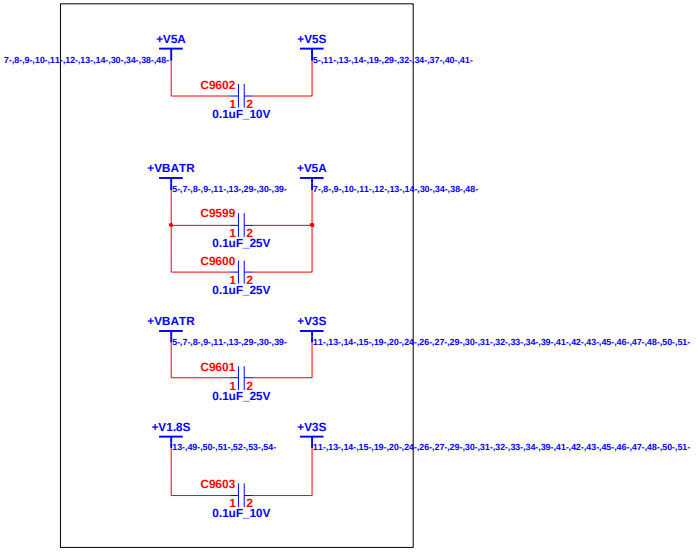












CHANGE by	Chang, Roger	25-Nov-2008	

INVENTEC

TITLE: *VV Discrete*
SCREW

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 48 OF 54

STRAPS	PIN	Description of default settings	
TX_PWRS_ENB	GPIO0	PCIE full TX output swing.	0
TX_DEEMPH_EN	GPIO1	PCIE transmitter de-emphasis enabled.	0
BIF_DEBUG_ACCESS	GPIO4	Debug signals muxed out.	0
ROMIDCFG(0:3)	GPIO[11:13,9]	Memory aperture type	X X X X

X = DESIGN DEPENDANT

0 = DO NOT INSTALL RESISTOR

1 = INSTALL 10K RESISTOR

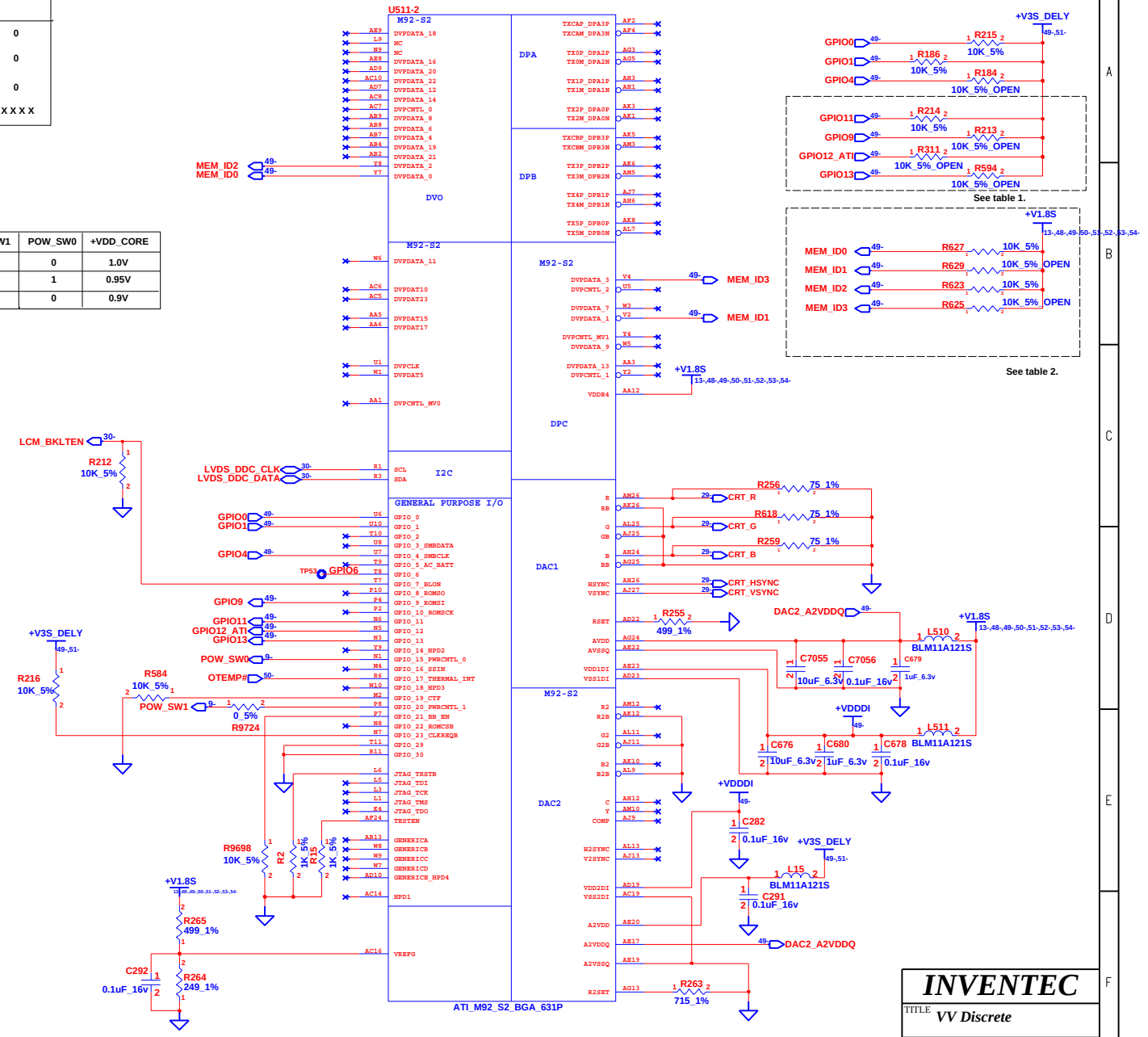
Table 1

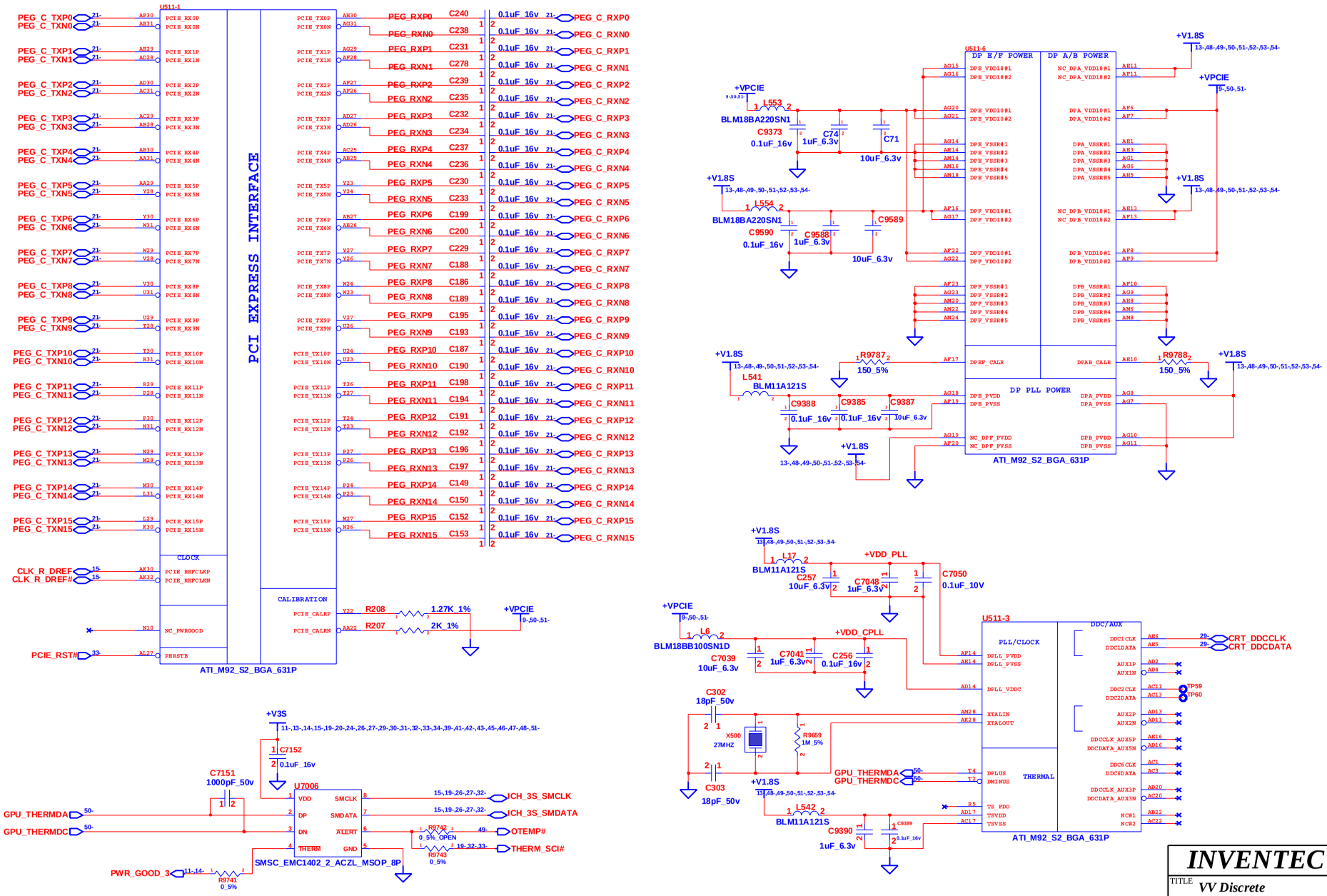
GPIO_13	GPIO_12	GPIO_11	For DIS-GDDR2	
0	0	0	128M memory aperture	
0	0	1	256M memory aperture	(Default)
1	1	0	reserved	

POW_SW1	POW_SW0	+VDD_CORE
0	0	1.0V
0	1	0.95V
1	0	0.9V

Table 2

For DIS-GDDR2					
MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	vendor	
0	1	0	1	samsung (256MB)	
0	1	1	0	Qimonda(256M)	(Default)
0	1	1	1	hynix (256MB)	





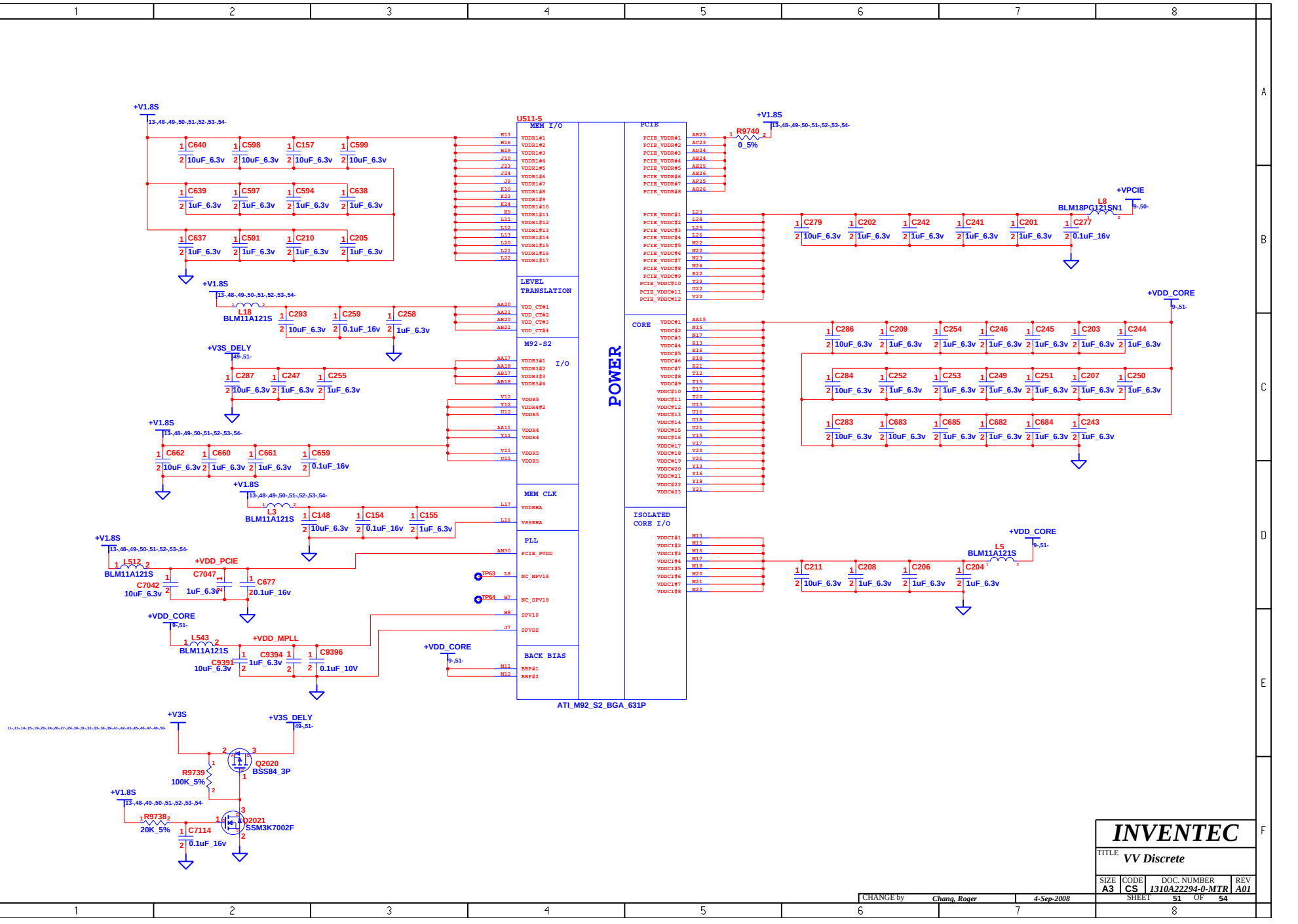
CHANGE by	*Chang, Roger*	*4-Sep-2008*	

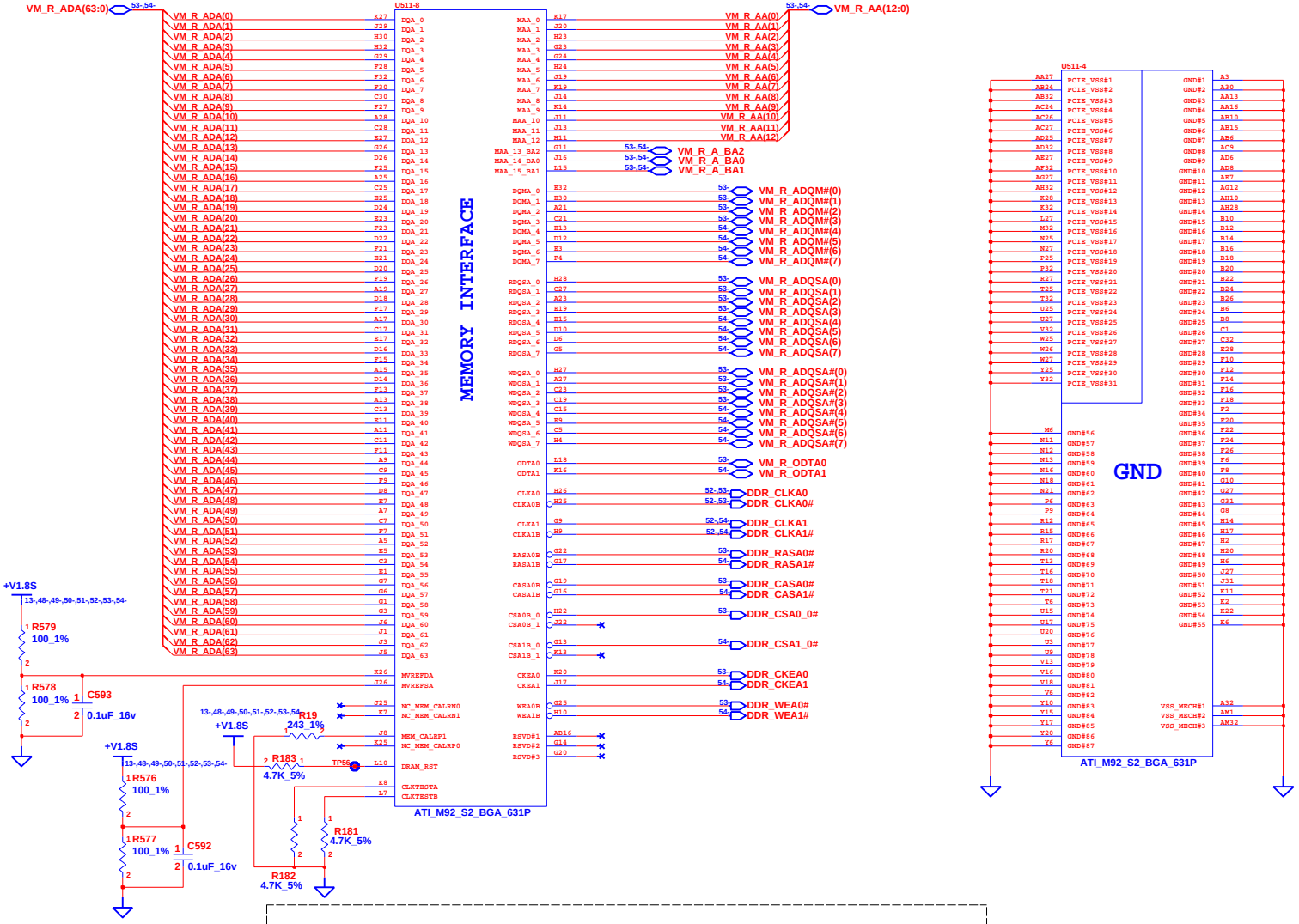
INVENTEC

TITLE: *VV Discrete*

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 50 OF 54


U511-5
MEM I/O
LEVEL TRANSLATION
M92-S2
I/O
MEM CLK
PLL
BACK BIAS
PCIE
CORE
ISOLATED CORE I/O
POWER
ATI_M92_S2_BGA_631P
+V1.8S
+V3S_DELY
+VDD_PCIE
+VDD_CORE
+VDD_MPLL
+VPCIE
+V3S
R9740
0_5%
L8
BLM18PG121SN1
L18
BLM11A121S
L3
BLM11A121S
L512
BLM11A121S
L543
BLM11A121S
L5
BLM11A121S
R9739
100K_5%
R9738
20K_5%
Q2020
BSS84_3P
Q2021
SSM3K7002F
C7114
0.1uF_16v
INVENTEC
VV Discrete
SIZE A3
CODE CS
DOC. NUMBER 1310A22294-0-MTR
REV A01
SHEET 51 OF 54
CHANGE by Chang, Roger 4-Sep-2008



Layou Note: Put these resisters close to V-RAM.

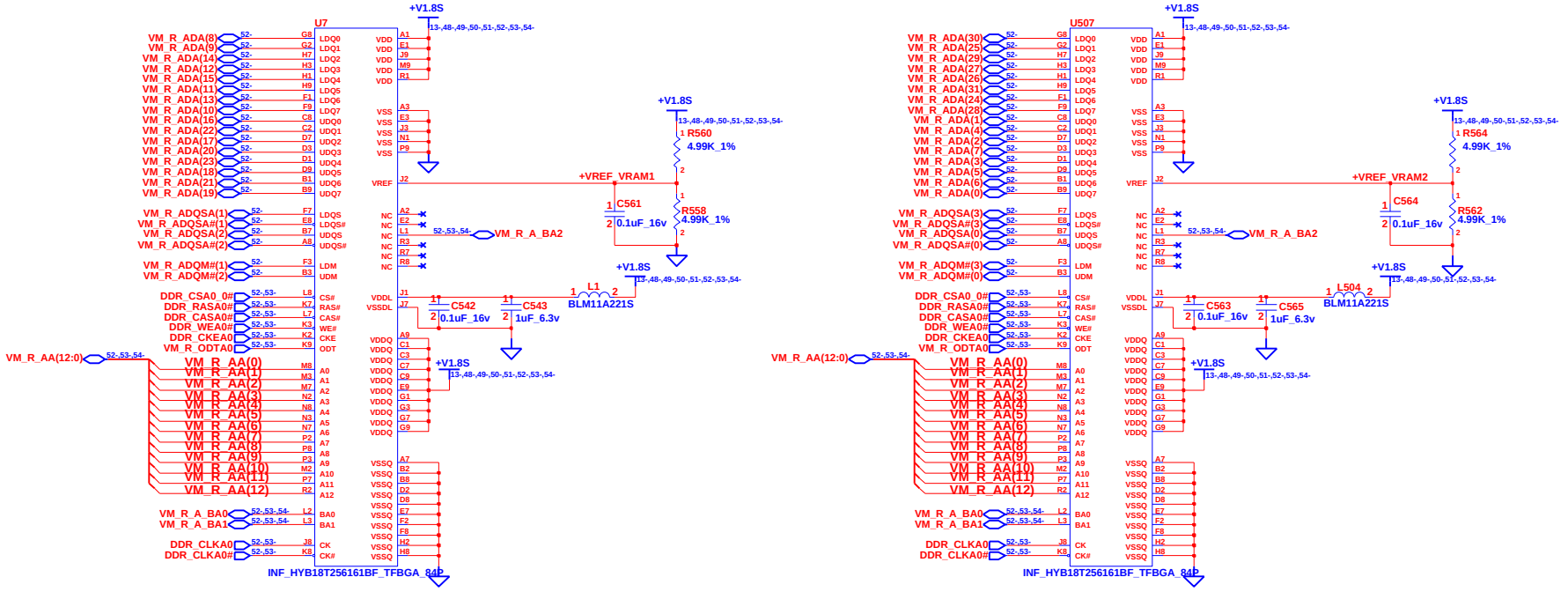
CHANGE by	Chang, Roger	4-Sep-2008	

INVENTEC

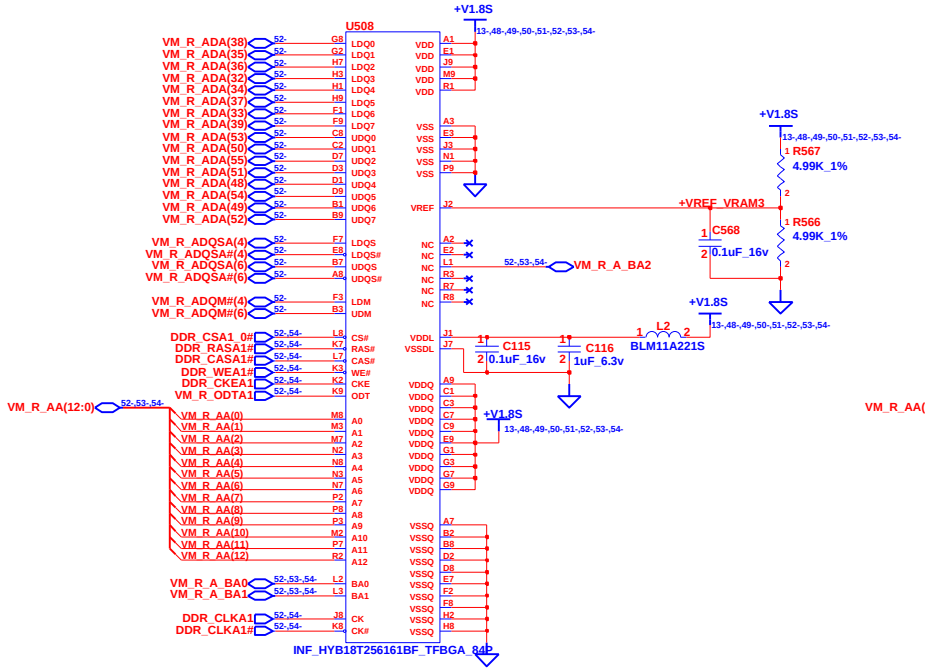
TITLE: *VV Discrete*

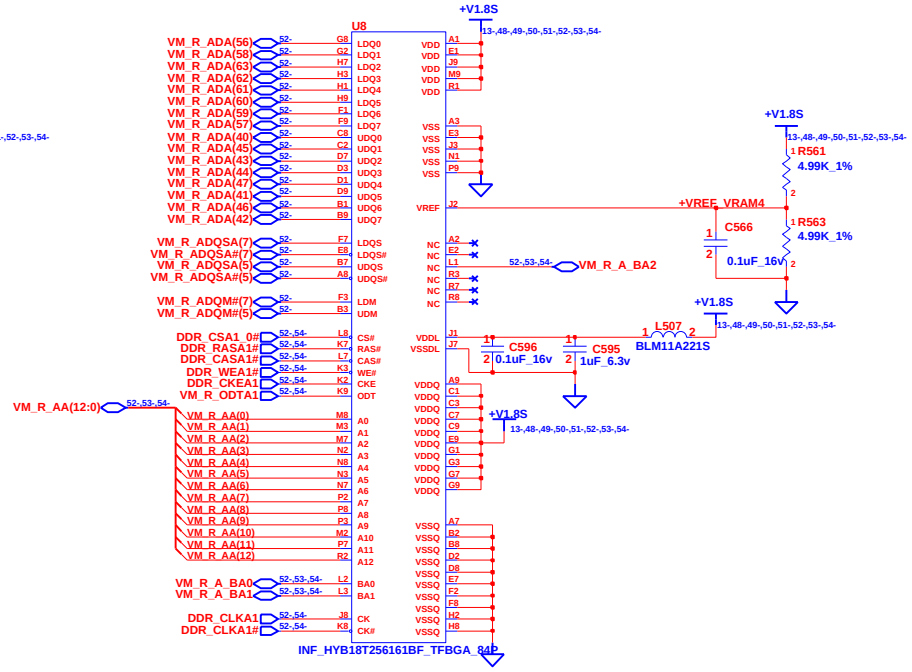
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

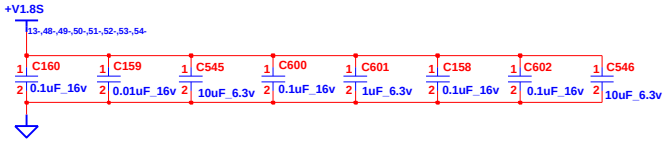
SHEET 52 OF 54

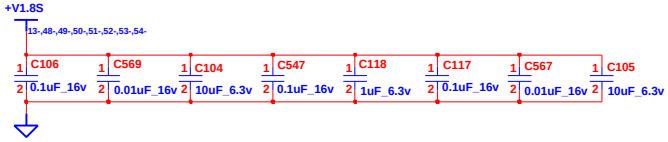


INVENTEC			
TITLE: VV Discrete			
SIZE: A3	CODE: CS	DOC. NUMBER: 1310A22294-0-MTR	REV: A01
CHANGE by: Chang, Roger	4-Sep-2008	SHEET 53 OF 54	









INVENTEC

TITLE: *VV Discrete*

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22294-0-MTR*	*A01*

SHEET 54 OF 54

CHANGE by	*Chang, Roger*	*4-Sep-2008*