# LCFC Confidential

## SKYWALKER NM-A831 Rev2.0 Schematic

### *Intel KabyLake Processor with DDR4 + PCH-LP*

### *NVIDIA N16S-GTR GDDR5 2GB*
### *NVIDIA N16P-GT GDDR5 2GB*

**2016-08-24 Rev2.0**



| | | | |
|---|---|---|---|
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Title: COVER PAGE

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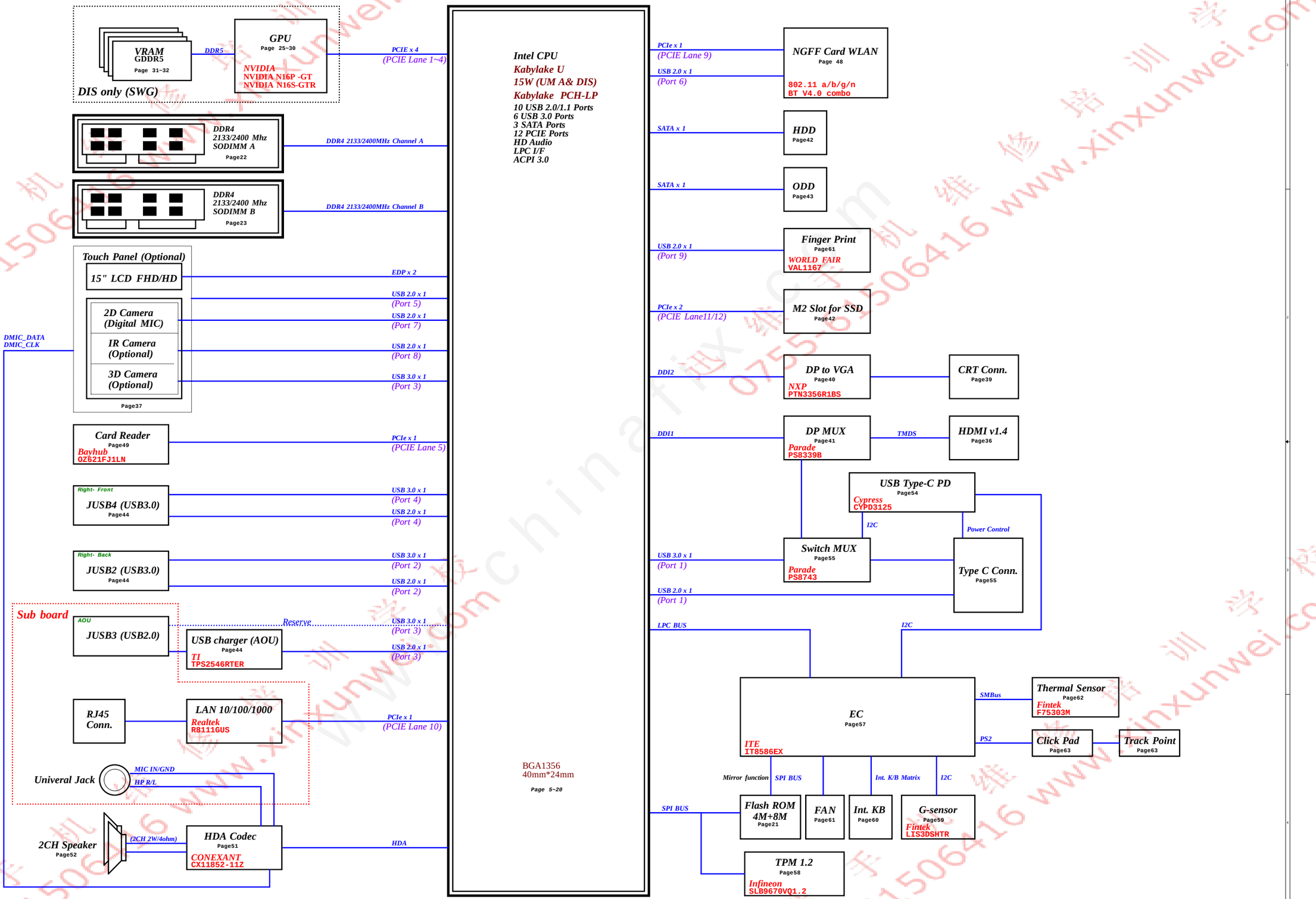
# Skywalker KBL U Block Diagram

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| | | | |
|---|---|---|---|
| Title | BLOCK DIAGRAM | | |
| Size A1 | Document Number | SKYWALKER | Rev 2.0 |
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## Voltage Rails ( O --> Means ON , X --> Means OFF )

| Power Plane / State | B+ +3VL | +3VALW +5VALW +1VALW +1.8VALW | +2.5V +1.2V +VCC_STG | +5VS +3VS +VCC_CORE +VCC_IO +VCC_SA +VCC_ST +VGA_CORE +3VS_VGA +1.35VS_VGA +3VS_AON +1VS_VGA +0.6VS |
|---|---|---|---|---|
| S0 | 0 | 0 | 0 | 0 |
| S3 | 0 | 0 | 0 | X |
| S5 S4/AC Only | 0 | 0 | X | X |
| S5 S4 Battery only | 0 | X | X | X |
| S5 S4 AC & Battery don't exist | X | X | X | X |

| STATE / SIGNAL | SLP_A# | SLP_S3# | SLP_S4# | SLP_S5# | EC_ON2 | EC_ON | SUSP# | SYSON |
|---|---|---|---|---|---|---|---|---|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | HIGH |
| S1(Power On Suspend) | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | HIGH |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | HIGH |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | ON | OFF | LOW |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | ON | OFF | LOW |

## SMBUS Control Table

| | SOURCE | Main VGA | BATT (Charger) | SODIMM | WLAN WiMAX | Thermal Sensor | PCH | CP Module | LAN PHY | G sensor | USB Type-C |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EC_SMB_CK1 EC_SMB_DA1 | IT8580F +3VL | X | V +3VALW | X | X | X | X | X | X | X | X |
| EC_SMB_CK2 EC_SMB_DA2 | IT8580F +3VL | X | X | X | X | X | X | X | X | X | V +3VPD_VDD |
| EC_SMB_CK3 EC_SMB_DA3 | IT8580F +3VS | V +3VS_VGA | X | X | X | V +3VS | V +3V_PCH | X | X | V +3VS_GS | X |
| PCH_SMB_CLK PCH_SMB_DATA | PCH +3V_PCH | X | X | X | X | X | X | V +5VS | X | X | X |
| PCH_SML1CLK PCH_SML1DAT | PCH +3V_PCH | X | X | X | X | X | X | X | X | X | X |

## BOM Structure Table

| BOM Structure | NOTE |
|---|---|
| PCB@ | For PCB load BOM |
| XDP@ | Debug port |
| UMA@ | UMA SKU ID |
| DIS@ | Optimus SKU ID |
| DIMM2@ | For DIMM2 function |
| DIMM1@ | For DIMM1 function |
| TYPEC@ | For USB Type-C function |
| ME@ | ME Connector |
| EMC@ | For EMC function |
| EMC_2D@ | For EMC function |
| EMC_NS@ | For EMC function |
| RF_NS@ | For RF function |
| S2G@ | For VRAM Strap |
| CHA@ | For VRAMA function |
| CHB@ | For VRAMB function |
| RANKA@ | GPU DDR5 Setting |
| X76@ | GPU VRAM Setting |
| 3DCCD@ | 3D Camera Setting |
| VGA@ | VGA Setting |
| MUX@ | MUX Setting |
| ODD@ | ODD Setting |
| TPM@ | Trusted Platform Module (TPM) |
| MIRROR@ | For mirror function |
| NGC6@ | For VGA Non GC6 function |
| GC6@ | For VGA GC6 function |

## USB2 Port

| Port | Device |
|---|---|
| 1 | JUSB1 TYPE-C |
| 2 | JUSB2 |
| 3 | JUSB3 Sub board |
| 4 | JUSB4 |
| 5 | Touch Panel |
| 6 | BT |
| 7 | CMOS |
| 8 | IR CAMERA |
| 9 | FP/Smart |

## USB3 Port

| Port | Device |
|---|---|
| 1 | JUSB1 TYPE-C |
| 2 | JUSB2 |
| 3 | 3D CCD |
| 4 | JUSB4 |

## PCIE Port

| Port | Device |
|---|---|
| 1 | GPU |
| 2 | GPU |
| 3 | GPU |
| 4 | GPU |
| 5 | CardReader |
| 6 | X |
| 7 | X |
| 8 | X |
| 9 | WLAN |
| 10 | LAN |
| 11 | M.2 SSD |
| 12 | M.2 SSD |

## SATA Port

| Port | Device |
|---|---|
| 1 | HDD |
| 2 | ODD |
| 3 | X |
| 4 | X |

| | | | |
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Title: NOTE LIST

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|---|---|---|
| Custom | SKYWALKER | 2.0 |

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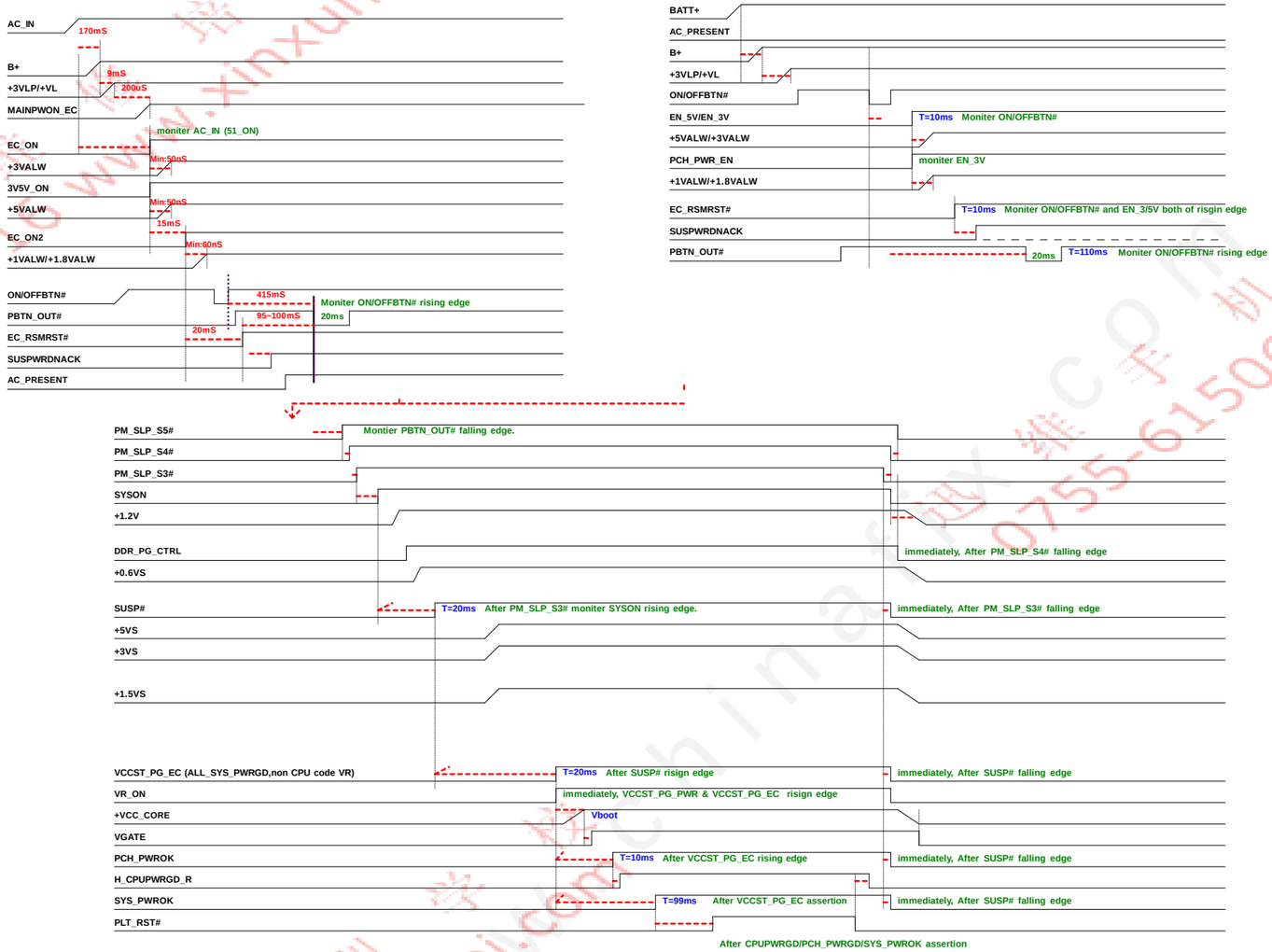
# Skywalker PWR Sequence_SKL-U_DDR4_Non-Deep Sx]

## [AC Mode]




## [DC Mode]




| | | | |
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| | | | |
|---|---|---|---|
| Title | Power Sequence | | |
| Size | Document Number | | Rev |
| D | SKYWALKER | | 2.0 |
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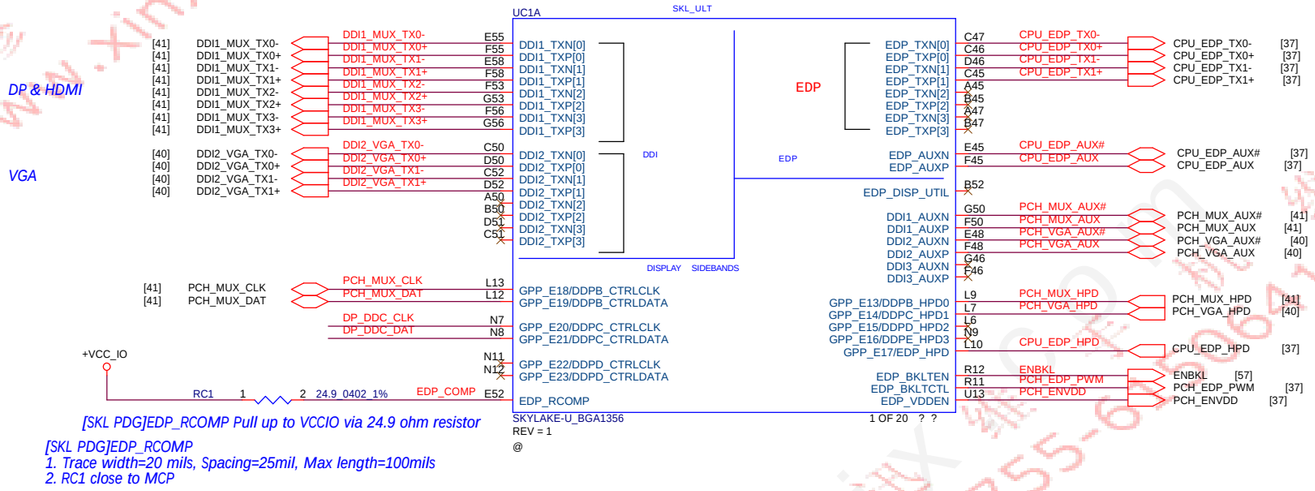
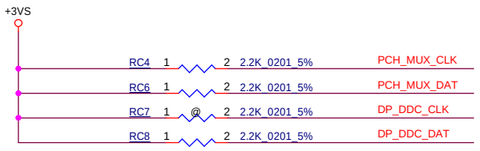
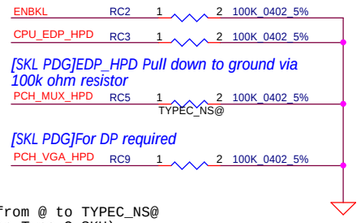



**DDPB_CTRLDATA, DDPC_CTRLDATA Internal PD 20K**




**20160202**
**Install RC4,RC6 to fix dual display issue**

| | | |
|---|---|---|
| DDPB_CTRLDATA | Port B Detected | This signal has an integrated weak pull-down (20 KΩ nominal) resistor.<br>When this signal is pulled up to VCC3_3 through a 1−3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port B will be detected. |
| DDPC_CTRLDATA | Port C Detected | This signal has an integrated weak pull-down (20 KΩ nominal) resistor.<br>When this signal is pulled up to VCC3_3 through a 1−3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port C will be detected. |




20160824
Change RC5 from @ to TYPEC_NS@
(Only for Non Type-C SKU)

| | | | |
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Title: **KBL(1/16):DDI/EDP**

| Size | Document Number | Rev |
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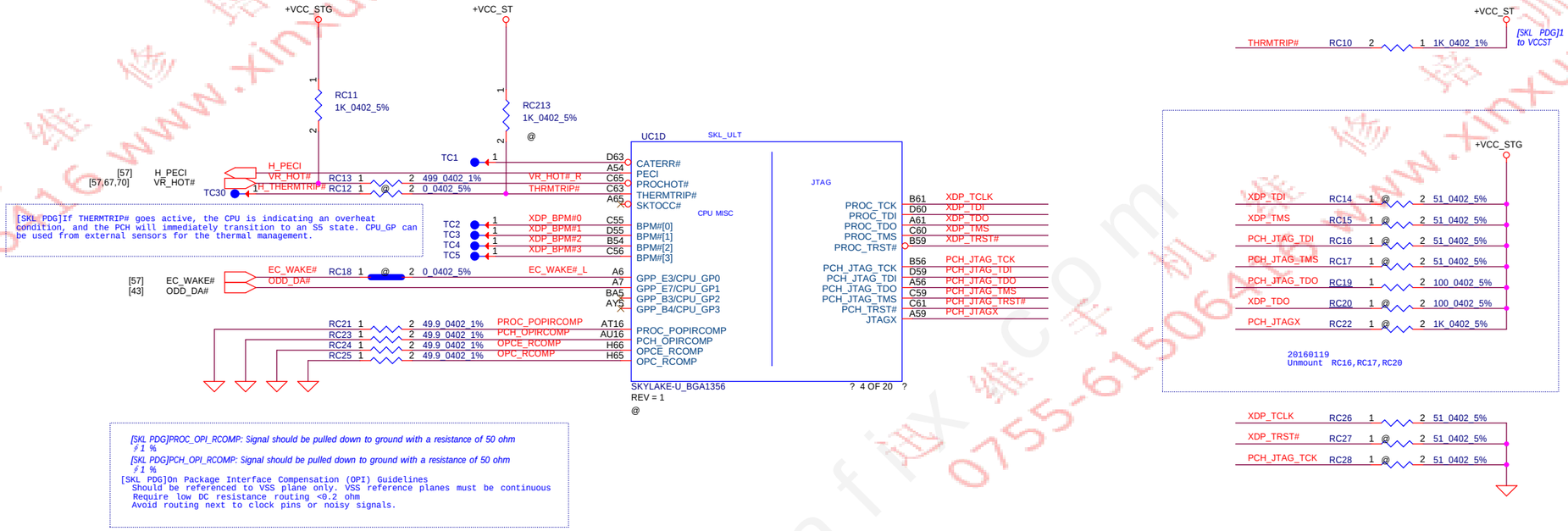


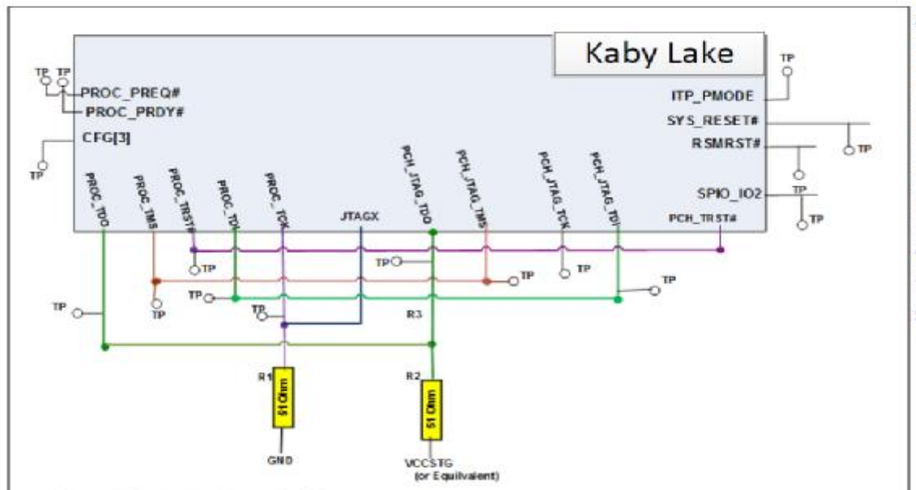


Figure 44-6. Connector Less Routing Topology

– Stubs on JTAG nets should not more than 200ps
– R1, R2 should be placed to within 200ps of PROC_TCK pin, PCH_JTAG_TDO, respectively
– Place Test point pads on Secondary side
– Route These Signals to Test Points: JTAG pins, ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[3], SPIO_IO2 VCCOBS_AB (PCH V1.0 A), GND pins (2)
– TP should be placed to within 250ps of the respetive Skylake pins, and the distance between TP and termination (for JTAG, if any) must be within 200ps.
– TP = Test Point Pad (size – 18 mil min, 25 mil preferred) The pad side must meet the industrial standard of Boundary Scan Test.

XDP_TCLK RC29 1 DCI@ 2 0_0402_5% PCH_JTAGX
XDP_TDI RC30 1 DCI@ 2 0_0402_5% PCH_JTAG_TDI
XDP_TDO RC31 1 DCI@ 2 0_0402_5% PCH_JTAG_TDO
XDP_TMS RC32 1 DCI@ 2 0_0402_5% PCH_JTAG_TMS
XDP_TRST# RC33 1 DCI@ 2 0_0402_5% PCH_JTAG_TRST#

Close to UC1

## Termination option

**XDP_TCLK**

PROC_TCK Termination:
51 ohm +/- 5% pull down to GNG (Ground)
Placed to within 200ps (1100 mil) or PROC_TCK pin

**PCH_JTAG_TDO**

PCH_JTAG_TDO Termination:
51ohm +/- 5% pull up to VccSTG or equivalent.
Placed to within 200ps (1100 mil) or PCH_JTAG_TDO pin



| | | | |
|---|---|---|---|
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Title: KBL(2/16):MISC/JTAG

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TABLE

| | Pin | Interleave | Non-Interleave |
|---|---|---|---|
| Block 0 | AL71 | DDR0_DQ[0] | DDR0_DQ[0] |
| | AL68 | DDR0_DQ[1] | DDR0_DQ[1] |
| | AN68 | DDR0_DQ[2] | DDR0_DQ[2] |
| | AN69 | DDR0_DQ[3] | DDR0_DQ[3] |
| | AL70 | DDR0_DQ[4] | DDR0_DQ[4] |
| | AL69 | DDR0_DQ[5] | DDR0_DQ[5] |
| | AN70 | DDR0_DQ[6] | DDR0_DQ[6] |
| | AN71 | DDR0_DQ[7] | DDR0_DQ[7] |
| | AR70 | DDR0_DQ[8] | DDR0_DQ[8] |
| | AR68 | DDR0_DQ[9] | DDR0_DQ[9] |
| | AU71 | DDR0_DQ[10] | DDR0_DQ[10] |
| | AU68 | DDR0_DQ[11] | DDR0_DQ[11] |
| | AR71 | DDR0_DQ[12] | DDR0_DQ[12] |
| | AR69 | DDR0_DQ[13] | DDR0_DQ[13] |
| | AU70 | DDR0_DQ[14] | DDR0_DQ[14] |
| | AU69 | DDR0_DQ[15] | DDR0_DQ[15] |
| Block 2 | BB65 | DDR0_DQ[16] | DDR0_DQ[32] |
| | AW65 | DDR0_DQ[17] | DDR0_DQ[33] |
| | AW63 | DDR0_DQ[18] | DDR0_DQ[34] |
| | AY63 | DDR0_DQ[19] | DDR0_DQ[35] |
| | BA65 | DDR0_DQ[20] | DDR0_DQ[36] |
| | AY65 | DDR0_DQ[21] | DDR0_DQ[37] |
| | BA63 | DDR0_DQ[22] | DDR0_DQ[38] |
| | BB63 | DDR0_DQ[23] | DDR0_DQ[39] |
| | BA61 | DDR0_DQ[24] | DDR0_DQ[40] |
| | AW61 | DDR0_DQ[25] | DDR0_DQ[41] |
| | BB59 | DDR0_DQ[26] | DDR0_DQ[42] |
| | AW59 | DDR0_DQ[27] | DDR0_DQ[43] |
| | BB61 | DDR0_DQ[28] | DDR0_DQ[44] |
| | AY61 | DDR0_DQ[29] | DDR0_DQ[45] |
| | BA59 | DDR0_DQ[30] | DDR0_DQ[46] |
| | AY59 | DDR0_DQ[31] | DDR0_DQ[47] |
| Block 4 | AY39 | DDR0_DQ[32] | DDR1_DQ[0] |
| | AW39 | DDR0_DQ[33] | DDR1_DQ[1] |
| | AY37 | DDR0_DQ[34] | DDR1_DQ[2] |
| | AW37 | DDR0_DQ[35] | DDR1_DQ[3] |
| | BB39 | DDR0_DQ[36] | DDR1_DQ[4] |
| | BA39 | DDR0_DQ[37] | DDR1_DQ[5] |
| | BA37 | DDR0_DQ[38] | DDR1_DQ[6] |
| | BB37 | DDR0_DQ[39] | DDR1_DQ[7] |
| | AY35 | DDR0_DQ[40] | DDR1_DQ[8] |
| | AW35 | DDR0_DQ[41] | DDR1_DQ[9] |
| | AY33 | DDR0_DQ[42] | DDR1_DQ[10] |
| | AW33 | DDR0_DQ[43] | DDR1_DQ[11] |
| | BB35 | DDR0_DQ[44] | DDR1_DQ[12] |
| | BA35 | DDR0_DQ[45] | DDR1_DQ[13] |
| | BA33 | DDR0_DQ[46] | DDR1_DQ[14] |
| | BB33 | DDR0_DQ[47] | DDR1_DQ[15] |
| Block 6 | AY31 | DDR0_DQ[48] | DDR1_DQ[32] |
| | AW31 | DDR0_DQ[49] | DDR1_DQ[33] |
| | AY29 | DDR0_DQ[50] | DDR1_DQ[34] |
| | AW29 | DDR0_DQ[51] | DDR1_DQ[35] |
| | BB31 | DDR0_DQ[52] | DDR1_DQ[36] |
| | BA31 | DDR0_DQ[53] | DDR1_DQ[37] |
| | BA29 | DDR0_DQ[54] | DDR1_DQ[38] |
| | BB29 | DDR0_DQ[55] | DDR1_DQ[39] |
| | AY27 | DDR0_DQ[56] | DDR1_DQ[40] |
| | AW27 | DDR0_DQ[57] | DDR1_DQ[41] |
| | AY25 | DDR0_DQ[58] | DDR1_DQ[42] |
| | AW25 | DDR0_DQ[59] | DDR1_DQ[43] |
| | BB27 | DDR0_DQ[60] | DDR1_DQ[44] |
| | BA27 | DDR0_DQ[61] | DDR1_DQ[45] |
| | BA25 | DDR0_DQ[62] | DDR1_DQ[46] |
| | BB25 | DDR0_DQ[63] | DDR1_DQ[47] |

TABLE

| | Pin | Interleave | Non-Interleave |
|---|---|---|---|
| Block 0 | AM70 | DDR0_DQSN[0] | DDR0_DQSN[0] |
| | AM69 | DDR0_DQSP[0] | DDR0_DQSP[0] |
| | AT69 | DDR0_DQSN[1] | DDR0_DQSN[1] |
| | AT70 | DDR0_DQSP[1] | DDR0_DQSP[1] |
| Block 2 | BA64 | DDR0_DQSN[2] | DDR0_DQSN[4] |
| | AY64 | DDR0_DQSP[2] | DDR0_DQSP[4] |
| | AY60 | DDR0_DQSN[3] | DDR0_DQSN[5] |
| | BA60 | DDR0_DQSP[3] | DDR0_DQSP[5] |
| Block 4 | BA38 | DDR0_DQSN[4] | DDR1_DQSN[0] |
| | AY38 | DDR0_DQSP[4] | DDR1_DQSP[0] |
| | AY34 | DDR0_DQSN[5] | DDR1_DQSN[1] |
| | BA34 | DDR0_DQSP[5] | DDR1_DQSP[1] |
| Block 6 | BA30 | DDR0_DQSN[6] | DDR1_DQSN[4] |
| | AY30 | DDR0_DQSP[6] | DDR1_DQSP[4] |
| | AY26 | DDR0_DQSN[7] | DDR1_DQSN[5] |
| | BA26 | DDR0_DQSP[7] | DDR1_DQSP[5] |

TABLE

| Pin | DDR3L | LPDDR3 | DDR4 |
|---|---|---|---|
| BA51 | DDR0_MA[5] | DDR0_CAA[0] | DDR0_MA[5] |
| BB54 | DDR0_MA[9] | DDR0_CAA[1] | DDR0_MA[9] |
| BA52 | DDR0_MA[6] | DDR0_CAA[2] | DDR0_MA[6] |
| AY52 | DDR0_MA[8] | DDR0_CAA[3] | DDR0_MA[8] |
| AW52 | DDR0_MA[7] | DDR0_CAA[4] | DDR0_MA[7] |
| AY55 | DDR0_BA[2] | DDR0_CAA[5] | DDR0_BG[0] |
| AW54 | DDR0_MA[12] | DDR0_CAA[6] | DDR0_MA[12] |
| BA54 | DDR0_MA[11] | DDR0_CAA[7] | DDR0_MA[11] |
| BA55 | DDR0_MA[15] | DDR0_CAA[8] | DDR0_ACT# |
| AY54 | DDR0_MA[14] | DDR0_CAA[9] | DDR0_BG[1] |
| AU46 | DDR0_MA[13] | DDR0_CAB[0] | DDR0_MA[13] |
| AU48 | DDR0_CAS# | DDR0_CAB[1] | DDR0_MA[15] |
| AT46 | DDR0_WE# | DDR0_CAB[2] | DDR0_MA[14] |
| AU50 | DDR0_RAS# | DDR0_CAB[3] | DDR0_MA[16] |
| AU52 | DDR0_BA[0] | DDR0_CAB[4] | DDR0_BA[0] |
| AY51 | DDR0_MA[2] | DDR0_CAB[5] | DDR0_MA[2] |
| AT48 | DDR0_BA[1] | DDR0_CAB[6] | DDR0_BA[1] |
| AT50 | DDR0_MA[10] | DDR0_CAB[7] | DDR0_MA[10] |
| BB50 | DDR0_MA[1] | DDR0_CAB[8] | DDR0_MA[1] |
| AY50 | DDR0_MA[0] | DDR0_CAB[9] | DDR0_MA[0] |
| BA50 | DDR0_MA[3] | Not Used | DDR0_MA[3] |
| BB52 | DDR0_MA[4] | Not Used | DDR0_MA[4] |

[22] DDR_A_D[63..0]

UC1B — SKL_ULT — DDR CH - A — SKYLAKE-U_BGA1356 — REV = 1 — @ — 2 OF 20 ?

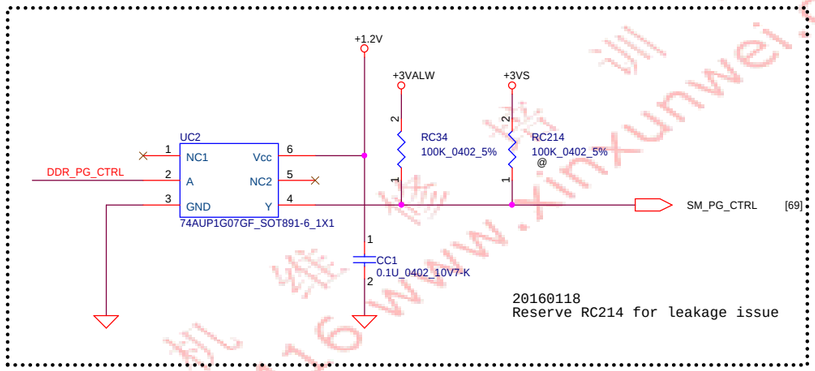
| | | | |
|---|---|---|---|
| DDR_A_D0 | AL71 | DDR0_DQ[0] | |
| DDR_A_D1 | AL68 | DDR0_DQ[1] | |
| DDR_A_D2 | AN68 | DDR0_DQ[2] | |
| DDR_A_D3 | AN69 | DDR0_DQ[3] | |
| DDR_A_D4 | AL70 | DDR0_DQ[4] | |
| DDR_A_D5 | AL69 | DDR0_DQ[5] | |
| DDR_A_D6 | AN70 | DDR0_DQ[6] | |
| DDR_A_D7 | AN71 | DDR0_DQ[7] | |
| DDR_A_D8 | AR70 | DDR0_DQ[8] | |
| DDR_A_D9 | AR68 | DDR0_DQ[9] | |
| DDR_A_D10 | AU71 | DDR0_DQ[10] | |
| DDR_A_D11 | AU68 | DDR0_DQ[11] | |
| DDR_A_D12 | AR71 | DDR0_DQ[12] | |
| DDR_A_D13 | AR69 | DDR0_DQ[13] | |
| DDR_A_D14 | AU70 | DDR0_DQ[14] | |
| DDR_A_D15 | AU69 | DDR0_DQ[15] | |
| DDR_A_D16 | BB65 | DDR0_DQ[16]/DDR0_DQ[32] | |
| DDR_A_D17 | AW65 | DDR0_DQ[17]/DDR0_DQ[33] | |
| DDR_A_D18 | AW63 | DDR0_DQ[18]/DDR0_DQ[34] | |
| DDR_A_D19 | AY63 | DDR0_DQ[19]/DDR0_DQ[35] | |
| DDR_A_D20 | BA65 | DDR0_DQ[20]/DDR0_DQ[36] | |
| DDR_A_D21 | AY65 | DDR0_DQ[21]/DDR0_DQ[37] | |
| DDR_A_D22 | BA63 | DDR0_DQ[22]/DDR0_DQ[38] | |
| DDR_A_D23 | BB63 | DDR0_DQ[23]/DDR0_DQ[39] | |
| DDR_A_D24 | BA61 | DDR0_DQ[24]/DDR0_DQ[40] | |
| DDR_A_D25 | AW61 | DDR0_DQ[25]/DDR0_DQ[41] | |
| DDR_A_D26 | BB59 | DDR0_DQ[26]/DDR0_DQ[42] | |
| DDR_A_D27 | AW59 | DDR0_DQ[27]/DDR0_DQ[43] | |
| DDR_A_D28 | BB61 | DDR0_DQ[28]/DDR0_DQ[44] | |
| DDR_A_D29 | AY61 | DDR0_DQ[29]/DDR0_DQ[45] | |
| DDR_A_D30 | BA59 | DDR0_DQ[30]/DDR0_DQ[46] | |
| DDR_A_D31 | AY59 | DDR0_DQ[31]/DDR0_DQ[47] | |
| DDR_A_D32 | AY39 | DDR0_DQ[32]/DDR1_DQ[0] | |
| DDR_A_D33 | AW39 | DDR0_DQ[33]/DDR1_DQ[1] | |
| DDR_A_D34 | AY37 | DDR0_DQ[34]/DDR1_DQ[2] | |
| DDR_A_D35 | AW37 | DDR0_DQ[35]/DDR1_DQ[3] | |
| DDR_A_D36 | BB39 | DDR0_DQ[36]/DDR1_DQ[4] | |
| DDR_A_D37 | BA39 | DDR0_DQ[37]/DDR1_DQ[5] | |
| DDR_A_D38 | BA37 | DDR0_DQ[38]/DDR1_DQ[6] | |
| DDR_A_D39 | BB37 | DDR0_DQ[39]/DDR1_DQ[7] | |
| DDR_A_D40 | AY35 | DDR0_DQ[40]/DDR1_DQ[8] | |
| DDR_A_D41 | AW35 | DDR0_DQ[41]/DDR1_DQ[9] | |
| DDR_A_D42 | AY33 | DDR0_DQ[42]/DDR1_DQ[10] | |
| DDR_A_D43 | AW33 | DDR0_DQ[43]/DDR1_DQ[11] | |
| DDR_A_D44 | BB35 | DDR0_DQ[44]/DDR1_DQ[12] | |
| DDR_A_D45 | BA35 | DDR0_DQ[45]/DDR1_DQ[13] | |
| DDR_A_D46 | BA33 | DDR0_DQ[46]/DDR1_DQ[14] | |
| DDR_A_D47 | BB33 | DDR0_DQ[47]/DDR1_DQ[15] | |
| DDR_A_D48 | AY31 | DDR0_DQ[48]/DDR1_DQ[32] | |
| DDR_A_D49 | AW31 | DDR0_DQ[49]/DDR1_DQ[33] | |
| DDR_A_D50 | AY29 | DDR0_DQ[50]/DDR1_DQ[34] | |
| DDR_A_D51 | AW29 | DDR0_DQ[51]/DDR1_DQ[35] | |
| DDR_A_D52 | BB31 | DDR0_DQ[52]/DDR1_DQ[36] | |
| DDR_A_D53 | BA31 | DDR0_DQ[53]/DDR1_DQ[37] | |
| DDR_A_D54 | BA29 | DDR0_DQ[54]/DDR1_DQ[38] | |
| DDR_A_D55 | BB29 | DDR0_DQ[55]/DDR1_DQ[39] | |
| DDR_A_D56 | AY27 | DDR0_DQ[56]/DDR1_DQ[40] | |
| DDR_A_D57 | AW27 | DDR0_DQ[57]/DDR1_DQ[41] | |
| DDR_A_D58 | AY25 | DDR0_DQ[58]/DDR1_DQ[42] | |
| DDR_A_D59 | AW25 | DDR0_DQ[59]/DDR1_DQ[43] | |
| DDR_A_D60 | BB27 | DDR0_DQ[60]/DDR1_DQ[44] | |
| DDR_A_D61 | BA27 | DDR0_DQ[61]/DDR1_DQ[45] | |
| DDR_A_D62 | BA25 | DDR0_DQ[62]/DDR1_DQ[46] | |
| DDR_A_D63 | BB25 | DDR0_DQ[63]/DDR1_DQ[47] | |

| | | | |
|---|---|---|---|
| DDR0_CKN[0] | AU53 | DDR_A_DDRCLK0_1866M# | DDR_A_DDRCLK0_1866M# [22] |
| DDR0_CKP[0] | AT53 | DDR_A_DDRCLK0_1866M | DDR_A_DDRCLK0_1866M [22] |
| DDR0_CKN[1] | AU55 | DDR_A_DDRCLK1_1866M# | DDR_A_DDRCLK1_1866M# [22] |
| DDR0_CKP[1] | AT55 | DDR_A_DDRCLK1_1866M | DDR_A_DDRCLK1_1866M [22] |
| DDR0_CKE[0] | BA56 | DDR_A_CKE0 | DDR_A_CKE0 [22] |
| DDR0_CKE[1] | BB56 | DDR_A_CKE1 | DDR_A_CKE1 [22] |
| DDR0_CKE[2] | AW56 | | |
| DDR0_CKE[3] | AY56 | | |
| DDR0_CS#[0] | AU45 | DDR_A_CS0# | DDR_A_CS0# [22] |
| DDR0_CS#[1] | AU43 | DDR_A_CS1# | DDR_A_CS1# [22] |
| DDR0_ODT[0] | AT45 | DDR_A_ODT0 | DDR_A_ODT0 [22] |
| DDR0_ODT[1] | AT43 | DDR_A_ODT1 | DDR_A_ODT1 [22] |
| DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5] | BA51 | DDR_A_MA5 | |
| DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9] | BB54 | DDR_A_MA9 | |
| DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6] | BA52 | DDR_A_MA6 | |
| DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8] | AY52 | DDR_A_MA8 | |
| DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7] | AW52 | DDR_A_MA7 | |
| DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0] | AY55 | DDR_A_BG0 | DDR_A_BG0 [22] |
| DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12] | AW54 | DDR_A_MA12 | |
| DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11] | BA54 | DDR_A_MA11 | |
| DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT# | BA55 | DDR_A_ACT_N | DDR_A_ACT_N [22] |
| DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1] | AY54 | DDR_A_BG1 | DDR_A_BG1 [22] |
| DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13] | AU46 | DDR_A_MA13 | |
| DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15] | AU48 | DDR_A_MA15 | |
| DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14] | AT46 | DDR_A_MA14 | |
| DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16] | AU50 | DDR_A_MA16 | |
| DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0] | AU52 | DDR_A_BA0 | DDR_A_BA0 [22] |
| DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2] | AY51 | DDR_A_MA2 | |
| DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1] | AT48 | DDR_A_BA1 | DDR_A_BA1 [22] |
| DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10] | AT50 | DDR_A_MA10 | |
| DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1] | BB50 | DDR_A_MA1 | |
| DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0] | AY50 | DDR_A_MA0 | |
| DDR0_MA[3] | BA50 | DDR_A_MA3 | |
| DDR0_MA[4] | BB52 | DDR_A_MA4 | |
| DDR0_DQSN[0] | AM70 | DDR_A_DQS#0 | |
| DDR0_DQSP[0] | AM69 | DDR_A_DQS0 | |
| DDR0_DQSN[1] | AT69 | DDR_A_DQS#1 | |
| DDR0_DQSP[1] | AT70 | DDR_A_DQS1 | |
| DDR0_DQSN[2]/DDR0_DQSN[4] | BA64 | DDR_A_DQS#2 | |
| DDR0_DQSP[2]/DDR0_DQSP[4] | AY64 | DDR_A_DQS2 | |
| DDR0_DQSN[3]/DDR0_DQSN[5] | AY60 | DDR_A_DQS#3 | |
| DDR0_DQSP[3]/DDR0_DQSP[5] | BA60 | DDR_A_DQS3 | |
| DDR0_DQSN[4]/DDR1_DQSN[0] | BA38 | DDR_A_DQS#4 | |
| DDR0_DQSP[4]/DDR1_DQSP[0] | AY38 | DDR_A_DQS4 | |
| DDR0_DQSN[5]/DDR1_DQSN[1] | AY34 | DDR_A_DQS#5 | |
| DDR0_DQSP[5]/DDR1_DQSP[1] | BA34 | DDR_A_DQS5 | |
| DDR0_DQSN[6]/DDR1_DQSN[4] | BA30 | DDR_A_DQS#6 | |
| DDR0_DQSP[6]/DDR1_DQSP[4] | AY30 | DDR_A_DQS6 | |
| DDR0_DQSN[7]/DDR1_DQSN[5] | AY26 | DDR_A_DQS#7 | |
| DDR0_DQSP[7]/DDR1_DQSP[5] | BA26 | DDR_A_DQS7 | |
| DDR0_ALERT# | AW50 | DDR_A_ALERT_N | DDR_A_ALERT_N [22] |
| DDR0_PAR | AT52 | DDR_A_PARITY | DDR_A_PARITY [22] |
| DDR_VREF_CA | AY67 | DDR4_VREF_CA_CPU_A | DDR4_VREF_CA_CPU_A [22] |
| DDR0_VREF_DQ | AY68 | DDR4_VREF_DQ_CPU_A | TC31 |
| DDR1_VREF_DQ | BA67 | DDR4_VREF_DQ_CPU_B | DDR4_VREF_DQ_CPU_B [23] |
| DDR_VTT_CNTL | AW67 | DDR_PG_CTRL | |

DDR_A_MA0 … DDR_A_MA16 → DDR_A_MA[0..16] [22]

DDR_A_DQS#0 … DDR_A_DQS#7 → DDR_A_DQS#[0..7] [22]

DDR_A_DQS0 … DDR_A_DQS7 → DDR_A_DQS[0..7] [22]

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|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **KBL(3/16):DDR4 CH.A**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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TABLE

| | Pin | Interleave | Non-Interleave |
|---|---|---|---|
| Block 1 | AF85 | DDR1_DQ[0] | DDR0_DQ[16] |
| | AF84 | DDR1_DQ[1] | DDR0_DQ[17] |
| | AK85 | DDR1_DQ[2] | DDR0_DQ[18] |
| | AK84 | DDR1_DQ[3] | DDR0_DQ[19] |
| | AF86 | DDR1_DQ[4] | DDR0_DQ[20] |
| | AF87 | DDR1_DQ[5] | DDR0_DQ[21] |
| | AK87 | DDR1_DQ[6] | DDR0_DQ[22] |
| | AK86 | DDR1_DQ[7] | DDR0_DQ[23] |
| | AF70 | DDR1_DQ[8] | DDR0_DQ[24] |
| | AF68 | DDR1_DQ[9] | DDR0_DQ[25] |
| | AH71 | DDR1_DQ[10] | DDR0_DQ[26] |
| | AH68 | DDR1_DQ[11] | DDR0_DQ[27] |
| | AF71 | DDR1_DQ[12] | DDR0_DQ[28] |
| | AF69 | DDR1_DQ[13] | DDR0_DQ[29] |
| | AH70 | DDR1_DQ[14] | DDR0_DQ[30] |
| | AH69 | DDR1_DQ[15] | DDR0_DQ[31] |
| Block 3 | AT86 | DDR1_DQ[16] | DDR0_DQ[48] |
| | AU86 | DDR1_DQ[17] | DDR0_DQ[49] |
| | AP85 | DDR1_DQ[18] | DDR0_DQ[50] |
| | AN85 | DDR1_DQ[19] | DDR0_DQ[51] |
| | AN86 | DDR1_DQ[20] | DDR0_DQ[52] |
| | AP86 | DDR1_DQ[21] | DDR0_DQ[53] |
| | AT85 | DDR1_DQ[22] | DDR0_DQ[54] |
| | AU85 | DDR1_DQ[23] | DDR0_DQ[55] |
| | AT81 | DDR1_DQ[24] | DDR0_DQ[56] |
| | AU81 | DDR1_DQ[25] | DDR0_DQ[57] |
| | AP80 | DDR1_DQ[26] | DDR0_DQ[58] |
| | AN80 | DDR1_DQ[27] | DDR0_DQ[59] |
| | AN81 | DDR1_DQ[28] | DDR0_DQ[60] |
| | AP81 | DDR1_DQ[29] | DDR0_DQ[61] |
| | AT80 | DDR1_DQ[30] | DDR0_DQ[62] |
| | AU80 | DDR1_DQ[31] | DDR0_DQ[63] |
| Block 5 | AU40 | DDR1_DQ[32] | DDR1_DQ[16] |
| | AT40 | DDR1_DQ[33] | DDR1_DQ[17] |
| | AT37 | DDR1_DQ[34] | DDR1_DQ[18] |
| | AU37 | DDR1_DQ[35] | DDR1_DQ[19] |
| | AR40 | DDR1_DQ[36] | DDR1_DQ[20] |
| | AP40 | DDR1_DQ[37] | DDR1_DQ[21] |
| | AR37 | DDR1_DQ[38] | DDR1_DQ[22] |
| | AT33 | DDR1_DQ[39] | DDR1_DQ[23] |
| | AU33 | DDR1_DQ[40] | DDR1_DQ[24] |
| | AU30 | DDR1_DQ[41] | DDR1_DQ[25] |
| | AT30 | DDR1_DQ[42] | DDR1_DQ[26] |
| | AR33 | DDR1_DQ[43] | DDR1_DQ[27] |
| | AP33 | DDR1_DQ[44] | DDR1_DQ[28] |
| | AR30 | DDR1_DQ[45] | DDR1_DQ[29] |
| | AP30 | DDR1_DQ[46] | DDR1_DQ[30] |
| | | DDR1_DQ[47] | DDR1_DQ[31] |
| Block 7 | AU27 | DDR1_DQ[48] | DDR1_DQ[48] |
| | AT27 | DDR1_DQ[49] | DDR1_DQ[49] |
| | AT25 | DDR1_DQ[50] | DDR1_DQ[50] |
| | AU25 | DDR1_DQ[51] | DDR1_DQ[51] |
| | AP27 | DDR1_DQ[52] | DDR1_DQ[52] |
| | AN27 | DDR1_DQ[53] | DDR1_DQ[53] |
| | AP25 | DDR1_DQ[54] | DDR1_DQ[54] |
| | AN25 | DDR1_DQ[55] | DDR1_DQ[55] |
| | AT22 | DDR1_DQ[56] | DDR1_DQ[56] |
| | AU22 | DDR1_DQ[57] | DDR1_DQ[57] |
| | AU21 | DDR1_DQ[58] | DDR1_DQ[58] |
| | AT21 | DDR1_DQ[59] | DDR1_DQ[59] |
| | AN22 | DDR1_DQ[60] | DDR1_DQ[60] |
| | AP22 | DDR1_DQ[61] | DDR1_DQ[61] |
| | AP21 | DDR1_DQ[62] | DDR1_DQ[62] |
| | AN21 | DDR1_DQ[63] | DDR1_DQ[63] |

TABLE

| | Pin | Interleave | Non-Interleave |
|---|---|---|---|
| Block 1 | AH66 | DDR1_DQSN[0] | DDR0_DQSN[2] |
| | AH65 | DDR1_DQSP[0] | DDR0_DQSP[2] |
| | AG69 | DDR1_DQSN[1] | DDR0_DQSN[3] |
| | AG70 | DDR1_DQSP[1] | DDR0_DQSP[3] |
| Block 3 | AR66 | DDR1_DQSN[2] | DDR0_DQSN[6] |
| | AR65 | DDR1_DQSP[2] | DDR0_DQSP[6] |
| | AR61 | DDR1_DQSN[3] | DDR0_DQSN[7] |
| | AR60 | DDR1_DQSP[3] | DDR0_DQSP[7] |
| Block 5 | AT38 | DDR1_DQSN[4] | DDR1_DQSN[2] |
| | AR38 | DDR1_DQSP[4] | DDR1_DQSP[2] |
| | AT32 | DDR1_DQSN[5] | DDR1_DQSN[3] |
| | AR32 | DDR1_DQSP[5] | DDR1_DQSP[3] |
| Block 7 | AR25 | DDR1_DQSN[6] | DDR1_DQSN[6] |
| | AR27 | DDR1_DQSP[6] | DDR1_DQSP[6] |
| | AR22 | DDR1_DQSN[7] | DDR1_DQSN[7] |
| | AR21 | DDR1_DQSP[7] | DDR1_DQSP[7] |

TABLE

| Pin | DDR3L | LPDDR3 | DDR4 |
|---|---|---|---|
| AY45 | DDR1_MA[5] | DDR1_CAA[0] | DDR1_MA[5] |
| AP50 | DDR1_MA[9] | DDR1_CAA[1] | DDR1_MA[9] |
| BA48 | DDR1_MA[6] | DDR1_CAA[2] | DDR1_MA[6] |
| BB48 | DDR1_MA[8] | DDR1_CAA[3] | DDR1_MA[8] |
| AP48 | DDR1_MA[7] | DDR1_CAA[4] | DDR1_MA[7] |
| AP52 | DDR1_BA[2] | DDR1_CAA[5] | DDR1_BG[0] |
| AN50 | DDR1_MA[12] | DDR1_CAA[6] | DDR1_MA[12] |
| AN48 | DDR1_MA[11] | DDR1_CAA[7] | DDR1_MA[11] |
| AN53 | DDR1_MA[15] | DDR1_CAA[8] | DDR1_ACT# |
| AN52 | DDR1_MA[14] | DDR1_CAA[9] | DDR1_BG[1] |
| BA43 | DDR1_MA[13] | DDR1_CAB[0] | DDR1_MA[13] |
| AY43 | DDR1_CAS# | DDR1_CAB[1] | DDR1_MA[15] |
| AY44 | DDR1_WE# | DDR1_CAB[2] | DDR1_MA[14] |
| AW44 | DDR1_RAS# | DDR1_CAB[3] | DDR1_MA[16] |
| BB44 | DDR1_BA[0] | DDR1_CAB[4] | DDR1_BA[0] |
| AY47 | DDR1_MA[2] | DDR1_CAB[5] | DDR1_MA[2] |
| BA44 | DDR1_BA[1] | DDR1_CAB[6] | DDR1_BA[1] |
| AW46 | DDR1_MA[10] | DDR1_CAB[7] | DDR1_MA[10] |
| AY46 | DDR1_MA[1] | DDR1_CAB[8] | DDR1_MA[1] |
| BA46 | DDR1_MA[0] | DDR1_CAB[9] | DDR1_MA[0] |
| BB46 | DDR1_MA[3] | Not Used | DDR1_MA[3] |
| BA47 | DDR1_MA[4] | Not Used | DDR1_MA[4] |

[23] DDR_B_D[0..63]

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DDR_B_D0 AF65 — DDR1_DQ[0]/DDR0_DQ[16]
DDR_B_D1 AK64 — DDR1_DQ[1]/DDR0_DQ[17]
DDR_B_D2 AK65 — DDR1_DQ[2]/DDR0_DQ[18]
DDR_B_D3 AK64 — DDR1_DQ[3]/DDR0_DQ[19]
DDR_B_D4 AF66 — DDR1_DQ[4]/DDR0_DQ[20]
DDR_B_D5 AF67 — DDR1_DQ[5]/DDR0_DQ[21]
DDR_B_D6 AK67 — DDR1_DQ[6]/DDR0_DQ[22]
DDR_B_D7 AK66 — DDR1_DQ[7]/DDR0_DQ[23]
DDR_B_D8 AF70 — DDR1_DQ[8]/DDR0_DQ[24]
DDR_B_D9 AF68 — DDR1_DQ[9]/DDR0_DQ[25]
DDR_B_D10 AH71 — DDR1_DQ[10]/DDR0_DQ[26]
DDR_B_D11 AH68 — DDR1_DQ[11]/DDR0_DQ[27]
DDR_B_D12 AF71 — DDR1_DQ[12]/DDR0_DQ[28]
DDR_B_D13 AF69 — DDR1_DQ[13]/DDR0_DQ[29]
DDR_B_D14 AH70 — DDR1_DQ[14]/DDR0_DQ[30]
DDR_B_D15 AH69 — DDR1_DQ[15]/DDR0_DQ[31]
DDR_B_D16 AT66 — DDR1_DQ[16]/DDR0_DQ[48]
DDR_B_D17 AU66 — DDR1_DQ[17]/DDR0_DQ[49]
DDR_B_D18 AP65 — DDR1_DQ[18]/DDR0_DQ[50]
DDR_B_D19 AN65 — DDR1_DQ[19]/DDR0_DQ[51]
DDR_B_D20 AN66 — DDR1_DQ[20]/DDR0_DQ[52]
DDR_B_D21 AP66 — DDR1_DQ[21]/DDR0_DQ[53]
DDR_B_D22 AT65 — DDR1_DQ[22]/DDR0_DQ[54]
DDR_B_D23 AU65 — DDR1_DQ[23]/DDR0_DQ[55]
DDR_B_D24 AT61 — DDR1_DQ[24]/DDR0_DQ[56]
DDR_B_D25 AU61 — DDR1_DQ[25]/DDR0_DQ[57]
DDR_B_D26 AP60 — DDR1_DQ[26]/DDR0_DQ[58]
DDR_B_D27 AN60 — DDR1_DQ[27]/DDR0_DQ[59]
DDR_B_D28 AN61 — DDR1_DQ[28]/DDR0_DQ[60]
DDR_B_D29 AP61 — DDR1_DQ[29]/DDR0_DQ[61]
DDR_B_D30 AT60 — DDR1_DQ[30]/DDR0_DQ[62]
DDR_B_D31 AU60 — DDR1_DQ[31]/DDR0_DQ[63]
DDR_B_D32 AU40 — DDR1_DQ[32]/DDR1_DQ[16]
DDR_B_D33 AT40 — DDR1_DQ[33]/DDR1_DQ[17]
DDR_B_D34 AT37 — DDR1_DQ[34]/DDR1_DQ[18]
DDR_B_D35 AU37 — DDR1_DQ[35]/DDR1_DQ[19]
DDR_B_D36 AR40 — DDR1_DQ[36]/DDR1_DQ[20]
DDR_B_D37 AP40 — DDR1_DQ[37]/DDR1_DQ[21]
DDR_B_D38 AP37 — DDR1_DQ[38]/DDR1_DQ[22]
DDR_B_D39 AR37 — DDR1_DQ[39]/DDR1_DQ[23]
DDR_B_D40 AT33 — DDR1_DQ[40]/DDR1_DQ[24]
DDR_B_D41 AU33 — DDR1_DQ[41]/DDR1_DQ[25]
DDR_B_D42 AU30 — DDR1_DQ[42]/DDR1_DQ[26]
DDR_B_D43 AT30 — DDR1_DQ[43]/DDR1_DQ[27]
DDR_B_D44 AR33 — DDR1_DQ[44]/DDR1_DQ[28]
DDR_B_D45 AP33 — DDR1_DQ[45]/DDR1_DQ[29]
DDR_B_D46 AR30 — DDR1_DQ[46]/DDR1_DQ[30]
DDR_B_D47 AP30 — DDR1_DQ[47]/DDR1_DQ[31]
DDR_B_D48 AU27 — DDR1_DQ[48]
DDR_B_D49 AT27 — DDR1_DQ[49]
DDR_B_D50 AT25 — DDR1_DQ[50]
DDR_B_D51 AU25 — DDR1_DQ[51]
DDR_B_D52 AP27 — DDR1_DQ[52]
DDR_B_D53 AN27 — DDR1_DQ[53]
DDR_B_D54 AN25 — DDR1_DQ[54]
DDR_B_D55 AP25 — DDR1_DQ[55]
DDR_B_D56 AT22 — DDR1_DQ[56]
DDR_B_D57 AU22 — DDR1_DQ[57]
DDR_B_D58 AU21 — DDR1_DQ[58]
DDR_B_D59 AT21 — DDR1_DQ[59]
DDR_B_D60 AN22 — DDR1_DQ[60]
DDR_B_D61 AP22 — DDR1_DQ[61]
DDR_B_D62 AP21 — DDR1_DQ[62]
DDR_B_D63 AN21 — DDR1_DQ[63]

DDR CH - B

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DDR1_CKN[0] AN45 — DDR_B_DDRCLK0_1866M# — DDR_B_DDRCLK0_1866M# [23]
DDR1_CKN[1] AN46 — DDR_B_DDRCLK1_1866M# — DDR_B_DDRCLK1_1866M# [23]
DDR1_CKP[0] AP45 — DDR_B_DDRCLK0_1866M — DDR_B_DDRCLK0_1866M [23]
DDR1_CKP[1] AP46 — DDR_B_DDRCLK1_1866M — DDR_B_DDRCLK1_1866M [23]

DDR1_CKE[0] AN56 — DDR_B_CKE0 — DDR_B_CKE0 [23]
DDR1_CKE[1] AP55 — DDR_B_CKE1 — DDR_B_CKE1 [23]
DDR1_CKE[2] AN55
DDR1_CKE[3] AP53

DDR1_CS#[0] BB42 — DDR_B_CS0# — DDR_B_CS0# [23]
DDR1_CS#[1] AY42 — DDR_B_CS1# — DDR_B_CS1# [23]
DDR1_ODT[0] BA42 — DDR_B_ODT0 — DDR_B_ODT0 [23]
DDR1_ODT[1] AW42 — DDR_B_ODT1 — DDR_B_ODT1 [23]

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5] AY48 — DDR_B_MA5
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9] AP50 — DDR_B_MA9
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6] BA48 — DDR_B_MA6
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8] BB48 — DDR_B_MA8
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7] AP48 — DDR_B_MA7
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0] AP52 — DDR_B_BG0 — DDR_B_BG0 [23]
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12] AN50 — DDR_B_MA12
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11] AN48 — DDR_B_MA11
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT# AN53 — DDR_B_ACT_N — DDR_B_ACT_N [23]
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1] AN52 — DDR_B_BG1 — DDR_B_BG1 [23]

DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13] BA43 — DDR_B_MA13
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15] AY43 — DDR_B_MA15
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14] AY44 — DDR_B_MA14
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16] AW44 — DDR_B_MA16
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0] BB44 — DDR_B_BA0 — DDR_B_BA0 [23]
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2] AY47 — DDR_B_MA2
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1] BA44 — DDR_B_BA1 — DDR_B_BA1 [23]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10] AW46 — DDR_B_MA10
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1] AY46 — DDR_B_MA1
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0] BA46 — DDR_B_MA0
DDR1_MA[3] BB46 — DDR_B_MA3
DDR1_MA[4] BA47 — DDR_B_MA4

DDR1_DQSN[0]/DDR0_DQSN[2] AH66 — DDR_B_DQS#0
DDR1_DQSP[0]/DDR0_DQSP[2] AH65 — DDR_B_DQS0
DDR1_DQSN[1]/DDR0_DQSN[3] AG69 — DDR_B_DQS#1
DDR1_DQSP[1]/DDR0_DQSP[3] AG70 — DDR_B_DQS1
DDR1_DQSN[2]/DDR0_DQSN[6] AR66 — DDR_B_DQS#2
DDR1_DQSP[2]/DDR0_DQSP[6] AR65 — DDR_B_DQS2
DDR1_DQSN[3]/DDR0_DQSN[7] AR61 — DDR_B_DQS#3
DDR1_DQSP[3]/DDR0_DQSP[7] AR60 — DDR_B_DQS3
DDR1_DQSN[4]/DDR1_DQSN[2] AT38 — DDR_B_DQS#4
DDR1_DQSP[4]/DDR1_DQSP[2] AR38 — DDR_B_DQS4
DDR1_DQSN[5]/DDR1_DQSN[3] AT32 — DDR_B_DQS#5
DDR1_DQSP[5]/DDR1_DQSP[3] AR32 — DDR_B_DQS5
DDR1_DQSN[6] AR25 — DDR_B_DQS#6
DDR1_DQSP[6] AR27 — DDR_B_DQS6
DDR1_DQSN[7] AR22 — DDR_B_DQS#7
DDR1_DQSP[7] AR21 — DDR_B_DQS7

DDR1_ALERT# AN43 — DDR_B_ALERT_N — DDR_B_ALERT_N [23]
DDR1_PAR AP43 — DDR_B_PARITY — DDR_B_PARITY [23]
DRAM_RESET# AT13 — DDR4_DRAMRST_N
DDR_RCOMP[0] AR18 — SM_RCOMP0 — RC36 1 2 121_0402_1%
DDR_RCOMP[1] AT18 — SM_RCOMP1 — RC38 1 2 80.6_0402_1%
DDR_RCOMP[2] AU18 — SM_RCOMP2 — RC39 1 2 100_0402_1%

*[KBL PDG]for DDR4 COMPENSATION*
*DDR_RCOMP[0] Pull down 121 ohm resistor*
*DDR_RCOMP[1] Pull down 80.6 ohm resistor*
*DDR_RCOMP[2] Pull down 100 ohm resistor*

DDR_B_MA0 DDR_B_MA1 DDR_B_MA2 DDR_B_MA3 DDR_B_MA4 DDR_B_MA5 DDR_B_MA6 DDR_B_MA7 DDR_B_MA8 DDR_B_MA9 DDR_B_MA10 DDR_B_MA11 DDR_B_MA12 DDR_B_MA13 DDR_B_MA14 DDR_B_MA15 DDR_B_MA16 → DDR_B_MA[0..16] [23]

DDR_B_DQS#0 DDR_B_DQS#1 DDR_B_DQS#2 DDR_B_DQS#3 DDR_B_DQS#4 DDR_B_DQS#5 DDR_B_DQS#6 DDR_B_DQS#7 → DDR_B_DQS#[0..7] [23]

DDR_B_DQS0 DDR_B_DQS1 DDR_B_DQS2 DDR_B_DQS3 DDR_B_DQS4 DDR_B_DQS5 DDR_B_DQS6 DDR_B_DQS7 → DDR_B_DQS[0..7] [23]

+1.2V
RC35 2 1 470_0402_5%
DDR4_DRAMRST_N — RC37 1 @ 2 0_0402_5% — DDR4_DRAMRST# [22,23]

| | | | |
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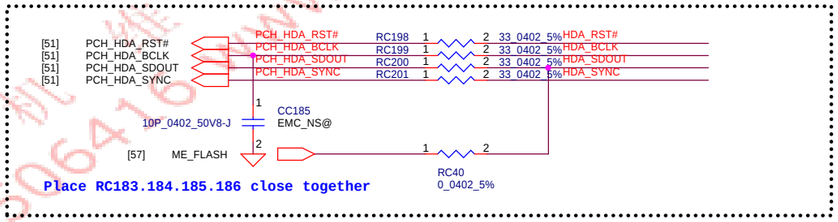
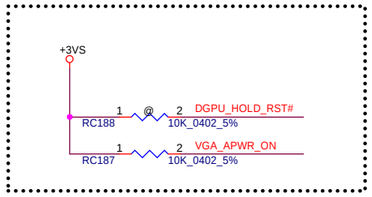
Title: KBL(4/16):DDR4 CH.B

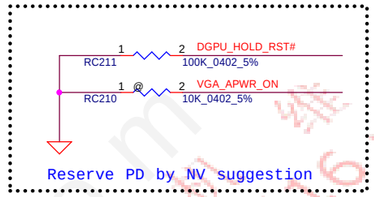
Size: Custom | Document Number: SKYWALKER | Rev: 2.0

Date: Thursday, August 25, 2016 | Sheet 8 of 82

[KBL PDG]Manufacturing Mode Jumper
1. If strap is sampled low, the security measures defined in
the Flash Descriptor will be in effect (default)
2. If sampled high, the Flash Descriptor Security will be overridden.

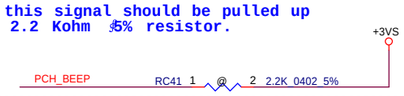


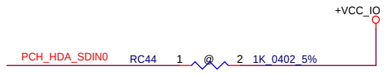




**Note:**
**SPKR (PC_BEEP) has an integrated weak pull-down resistor (20 K ohm nominal) to disable Top-Block Sway by default.**

**To enable Top-Block Swap, this signal should be pulled up to V3.3S through a 1k to 2.2 Kohm ±5% resistor.**

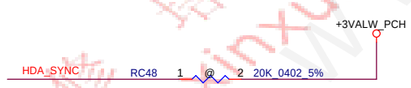


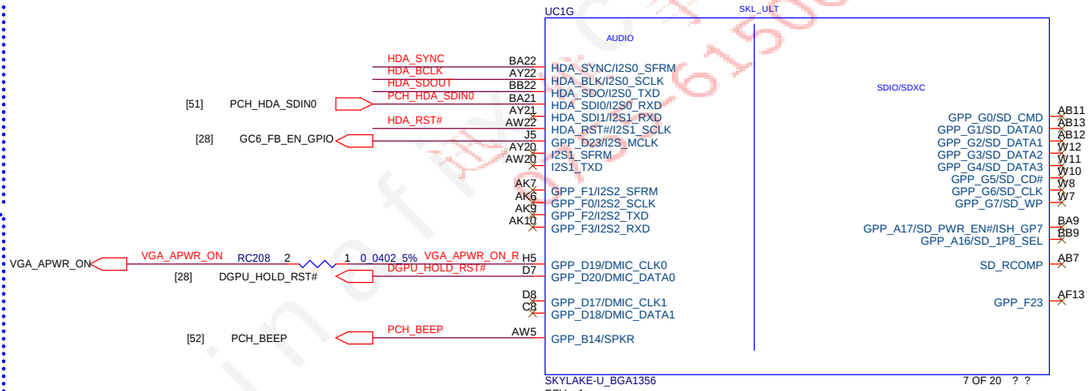

**Note:**
**Internal PD 20K**




**Note:**
**HDA_SDO should only be asserted high via external pull-up to 3.3A rail in manufacturing/debug environments ONLY.**


**Note:**
**Internal PD 20K**




*[SKL PDG] internal SD Card*

**Not support internal SD card. Remove SD_RCOMP**

| | | | |
|---|---|---|---|
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Title: **KBL(5/16):HDA/SDIO**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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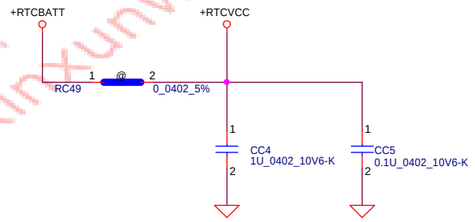
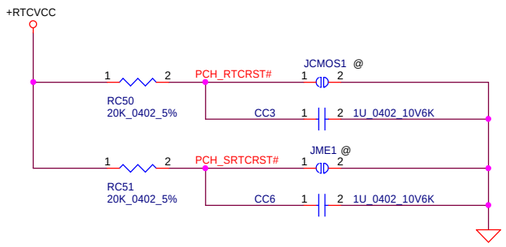
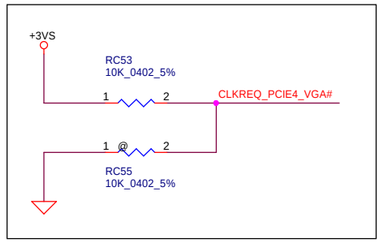
## RTC External Circuit

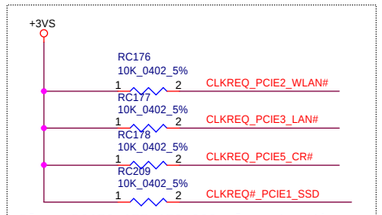
*+RTCBATT, +RTCVCC*
*Trace width = 20mils*




## JCMOS, JME Setting, Need Under DDR Door




**Place RC176,177,178,209 close together**

**M.2 SSD**
[42] CLK_PCIE_SSD#
[42] CLK_PCIE_SSD
[42] CLKREQ#_PCIE1_SSD

**WLAN**
[48] CLK_PCIE_WLAN#
[48] CLK_PCIE_WLAN
[48] CLKREQ_PCIE2_WLAN#

**LAN**
[56] CLK_PCIE_LAN#
[56] CLK_PCIE_LAN
[56] CLKREQ_PCIE3_LAN#

**VGA**
[25] CLK_PCIE_VGA#
[25] CLK_PCIE_VGA
[25] CLKREQ_PCIE4_VGA#

**CR**
[49] CLK_PCIE_CR#
[49] CLK_PCIE_CR
[49] CLKREQ_PCIE5_CR#

UC1J — SKL_ULT — CLOCK SIGNALS

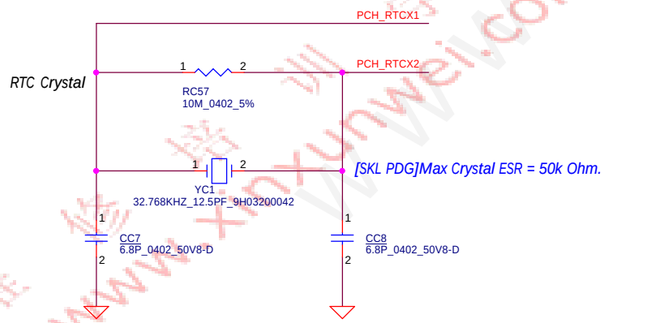
| | | | |
|---|---|---|---|
| | CLK_PCIE_SSD# | B42 | CLKOUT_PCIE_N0 |
| | CLK_PCIE_SSD | A42 | CLKOUT_PCIE_P0 |
| | CLKREQ#_PCIE1_SSD | AT7 | GPP_B5/SRCCLKREQ0# |
| | CLK_PCIE_WLAN# | D41 | CLKOUT_PCIE_N1 |
| | CLK_PCIE_WLAN | C41 | CLKOUT_PCIE_P1 |
| | CLKREQ_PCIE2_WLAN# | AT8 | GPP_B6/SRCCLKREQ1# |
| | CLK_PCIE_LAN# | D40 | CLKOUT_PCIE_N2 |
| | CLK_PCIE_LAN | C40 | CLKOUT_PCIE_P2 |
| | CLKREQ_PCIE3_LAN# | AT10 | GPP_B7/SRCCLKREQ2# |
| | CLK_PCIE_VGA# | B40 | CLKOUT_PCIE_N3 |
| | CLK_PCIE_VGA | A40 | CLKOUT_PCIE_P3 |
| | CLKREQ_PCIE4_VGA# | AU8 | GPP_B8/SRCCLKREQ3# |
| | CLK_PCIE_CR# | E40 | CLKOUT_PCIE_N4 |
| | CLK_PCIE_CR | E38 | CLKOUT_PCIE_P4 |
| | CLKREQ_PCIE5_CR# | AU7 | GPP_B9/SRCCLKREQ4# |
| | | | CLKOUT_PCIE_N5 |
| | | | CLKOUT_PCIE_P5 |
| | | | GPP_B10/SRCCLKREQ5# |
| | | E43 | CLKOUT_ITPXDP_N |
| | | E43 | CLKOUT_ITPXDP_P |
| | | BA17 | GPD8/SUSCLK |
| | | E37 | XTAL24_IN |
| | | E35 | XTAL24_OUT |
| | | E42 | XCLK_BIASREF |
| | | AM18 | RTCX1 |
| | | AM20 | RTCX2 |
| | | AN18 | SRTCRST# |
| | | AM16 | RTCRST# |

SUSCLK_32K → SUSCLK_32K [48]
DIFFCLK_BIASREF → RC56 2.7K_0402_1% → +1VALW
PCH_RTCX1, PCH_RTCX2, PCH_XTAL24_IN, PCH_XTAL24_OUT, PCH_SRTCRST#, PCH_RTCRST#

SKYLAKE-U_BGA1356
10 OF 20 ? ?
REV = 1
@

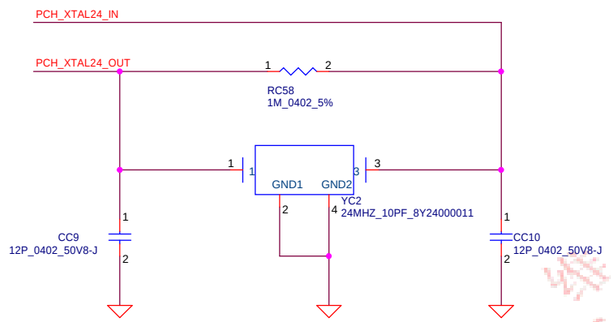
**[SKL PDG]External pull-up resistor required if used for CLKREQ# functionality.**

[SKL PDG]
1.Space > 15mils
2.No trace under crystal
3.Place on oppsosit side of MCP for temp inf l uence
4.The exact capacitor values forC1 and C2 must be based on the crystal maker recommendat i ons
Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.




20160127
Change CC7/CC8 to 6.8p by vender suggestion

[SKL PDG]
1.A 24 MHz crystal with crystal frequency tolerance and stability of +/-30 ppm
2.Two External Load Capacitors (Ce1 and Ce2)
3.A 1-Mohm bias resistor (Rf)

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Title: **KBL(6/16):CLOCK SIGNALS**
Size: Custom | Document Number: **SKYWALKER** | Rev: 2.0
Date: Thursday, August 25, 2016 | Sheet 10 of 82

## Functional Strap Definitions

L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
*H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).Support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

+3VALW_PCH
SMBALERT# — RC59 1 — 2 — 1K_0402_5%

**GPP_C2, Internal PD 20K**

JTAG ODT

**SPI0_MOSI**

+3VALW_PCH
SPI_SI — RC62 1 — @ — 2 — 8.2K_0402_5%

+3VALW_PCH
SPI_SO — RC65 1 — @ — 2 — 8.2K_0402_5%

**GPP_C5, Internal PD 20K**

*L: LPC
H: eSPI

+3VALW_PCH
SML0ALERT# — RC67 1 — @ — 2 — 1K_0402_5%

+3VS
**Place RC179,180,181 close together**
+3VALW_PCH

RC179 1 — 2 10K_0402_5% SERIRQ
RC180 1 — 2 10K_0402_5% EC_SCI#
RC181 1 — 2 10K_0402_5% KBRST#
RC72 1 — 2 4.7K_0402_5% CP_SMB_CLK
RC76 1 — 2 4.7K_0402_5% CP_SMB_DAT
RC212 1 — 2 10K_0402_5% GPU_EVENT#

PCH_SMB_CLK — RC71 1 — 2 2.2K_0402_1%
PCH_SMB_DATA — RC73 1 — 2 2.2K_0402_1%
PCH_SML1CLK — RC74 1 — 2 2.2K_0402_1%
PCH_SML1DATA — RC75 1 — 2 2.2K_0402_1%

SML1ALERT# — RC77 1 — @ — 2 — 1K_0402_5%

Add RC212 PU by NV suggestion

**close to CPU**

UC1E — SKL_ULT

SPI - FLASH
[21,58] SPI_CLK — SPI_CLK — AV2
[21,58] SPI_SO — SPI_SO — AW3
[21,58] SPI_SI — SPI_SI — AV3
[21] SPI_IO2 — SPI_IO2 — AW2
[21] SPI_IO3 — SPI_IO3 — AU4
[21] SPI_CS0#_8MB — SPI_CS0#_8MB — AU3
[21] SPI_CS1#_4MB — SPI_CS1#_4MB — AU2
[58] SPI_CS2#_TPM — SPI_CS2#_TPM — AU1

SPI - TOUCH
M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

[25] All_GPU_PWRGD — RC107 1 — 2 0_0402_5% — All_GPU_PWRGD_R
[28] GPU_EVENT# — GPU_EVENT#
[57] EC_SCI# — EC_SCI#

C LINK
[48] CL_CLK_WLAN — G3 CL_CLK
[48] CL_DATA_WLAN — G2 CL_DATA
[48] CL_RST_WLAN# — G1 CL_RST#

[57] KBRST# — KBRST# — AW13 GPP_A0/RCIN#
1 — CC183 EMC_NS@ — 2
10P_0402_50V8-J
[57,58] SERIRQ — SERIRQ — AY11 GPP_A6/SERIRQ

SMBUS, SMLINK
R7 GPP_C0/SMBCLK — PCH_SMB_CLK
R8 GPP_C1/SMBDATA — PCH_SMB_DATA
R10 GPP_C2/SMBALERT# — SMBALERT#
R9 GPP_C3/SML0CLK
W2 GPP_C4/SML0DATA
W1 GPP_C5/SML0ALERT# — SML0ALERT#
W3 GPP_C6/SML1CLK — PCH_SML1CLK
V3 GPP_C7/SML1DATA — PCH_SML1DATA
AM7 GPP_B23/SML1ALERT#/PCHHOT# — SML1ALERT#

LPC
AY13 GPP_A1/LAD0/ESPI_IO0 — LPC_AD0 [57]
BA13 GPP_A2/LAD1/ESPI_IO1 — LPC_AD1 [57]
BB13 GPP_A3/LAD2/ESPI_IO2 — LPC_AD2 [57]
AY12 GPP_A4/LAD3/ESPI_IO3 — LPC_AD3 [57]
BA12 GPP_A5/LFRAME#/ESPI_CS# — LPC_FRAME# [57]
BA11 GPP_A14/SUS_STAT#/ESPI_RESET# — SUS_STAT#

AW9 GPP_A9/CLKOUT_LPC0/ESPI_CLK — PCH_PCI_CLK_R
AY9 GPP_A10/CLKOUT_LPC1
AW11 GPP_A8/CLKRUN# — CLKRUN#

SKYLAKE-U_BGA1356
REV = 1
@
5 OF 20 ? ?

RC63 0_0402_5% — 1 — @ — 2 — 1 — TC7
RC64 22_0402_5% — 1 EMC@ 2 — CLK_PCI_EC [57]
RC66 8.2K_0402_5% — +3VS
1 — CC184 EMC_NS@ — 2
10P_0402_50V8-J
Close to UC1

DIMM1, DIMM2, Security EEPROM, Click Pad

EC,dGPU,Thermal Sensor

SB00000YS00 2N7002KDWH_SOT363-6 QC1A
PCH_SMB_CLK — CP_SMB_CLK [22,23,63]
+3VS
Plan to remove QC1 after SDV
PCH_SMB_DATA — CP_SMB_DAT [22,23,63]
QC1B 2N7002KDWH_SOT363-6 SB00000YS00

SB00000YS00 2N7002KDWH_SOT363-6 QC2A
+3VS PCH_SML1CLK — EC_SMB_CK3 [28,57,59,62]
PCH_SML1DATA — EC_SMB_DA3 [28,57,59,62]
QC2B 2N7002KDWH_SOT363-6 SB00000YS00

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| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |

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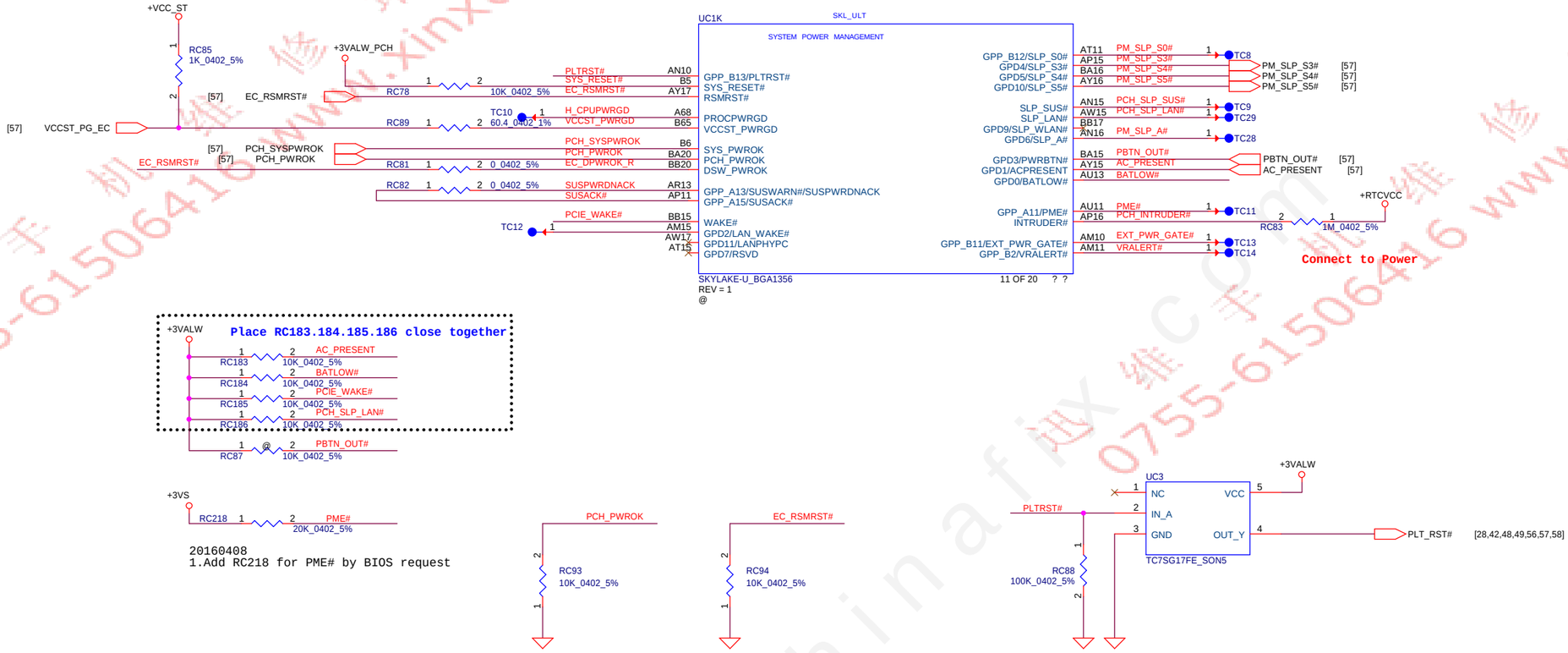
Title: KBL(7/16):LPC/SPI/SMBUS/CL
Size: Custom | Document Number: SKYWALKER | Rev: 2.0
Date: Thursday, August 25, 2016 | Sheet 11 of 82










20160408
1.Add RC218 for PME# by BIOS request







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|---|---|---|---|
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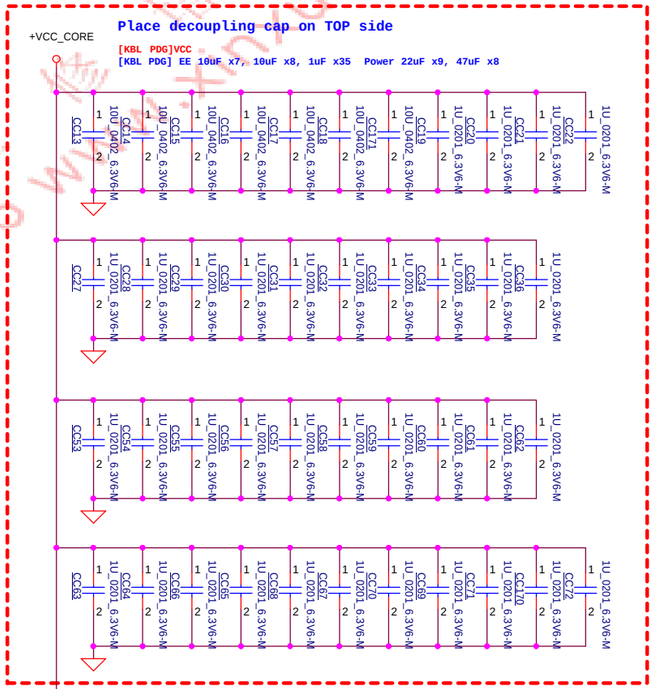
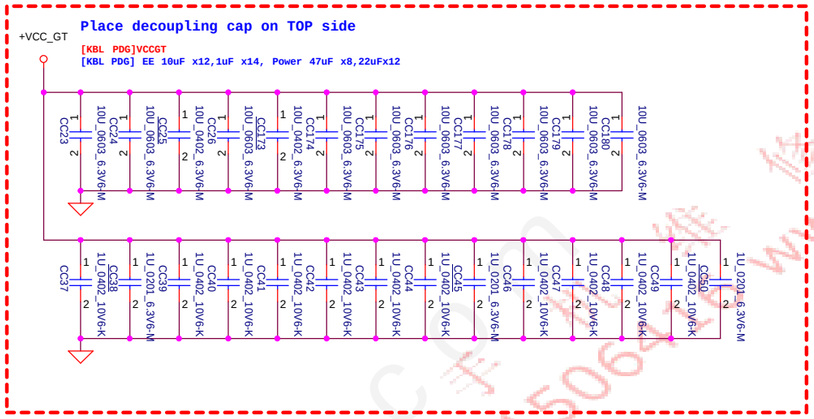
Title: KBL(8/16):SYSTEM PM

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

Date: Thursday, August 25, 2016 Sheet 12 of 82

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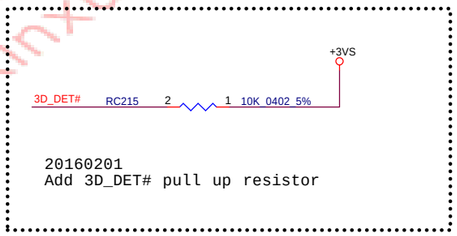
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **KBL(9/16):Decoupling**

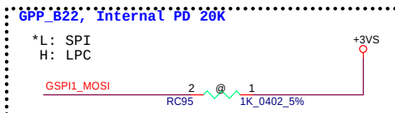
Size: Custom | Document Number: **SKYWALKER** | Rev: 2.0

Date: Thursday, August 25, 2016 | Sheet 13 of 82



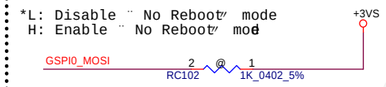

20160201
Add 3D_DET# pull up resistor

**GPP_B22, Internal PD 20K**




To enable boot to LPC, this signal should be pulled up to V3.3S through a 1k to 2.2 K ±5 % resistor

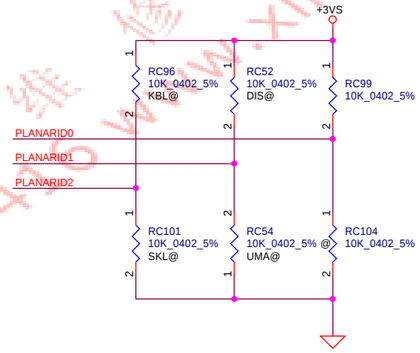
**GPP_B18, Internal PD 20K**

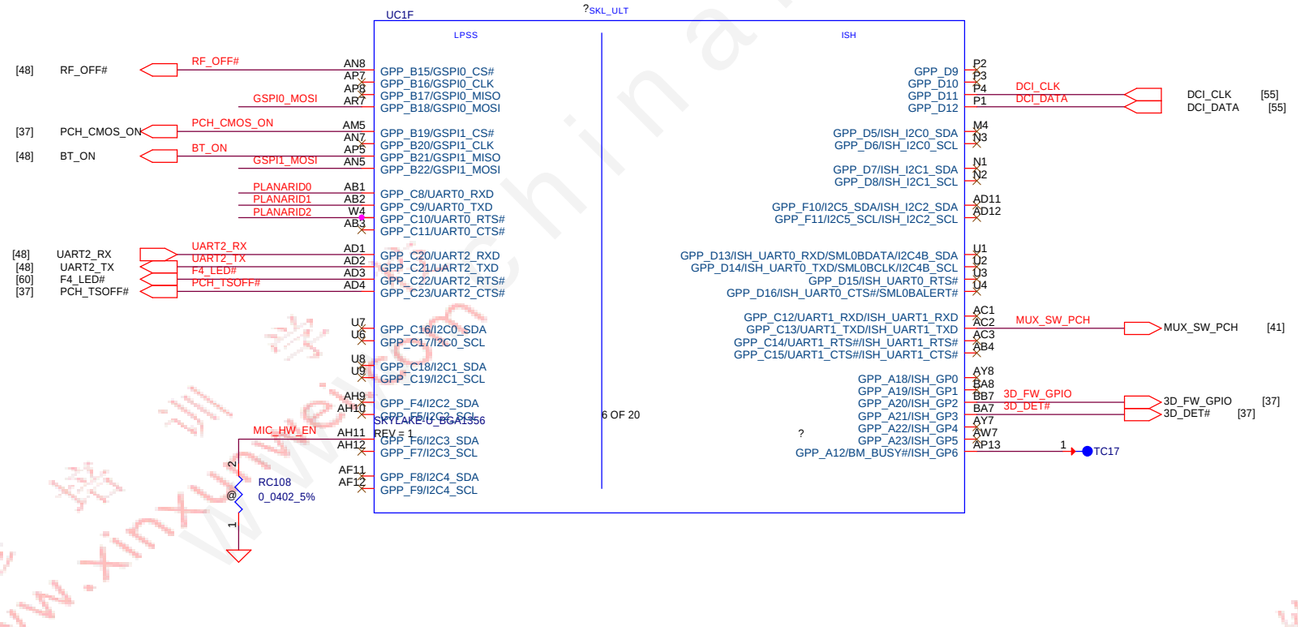



To enable no reboot on TCO Timer expiration, this signal should be pulled-up to V3.3S through a 1k to 2.2 K ±5 % resistor

Project ID

| | PLANARID0 (GPP_C8) | PLANARID1 (GPP_C9) | PLANARID2 (GPP_C10) | |
|---|---|---|---|---|
| L | 14" | UMA | Skylake | |
| H | 15" | DIS | Kabylake | |




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: KBL(10/16):GPIO/CPU/MISC

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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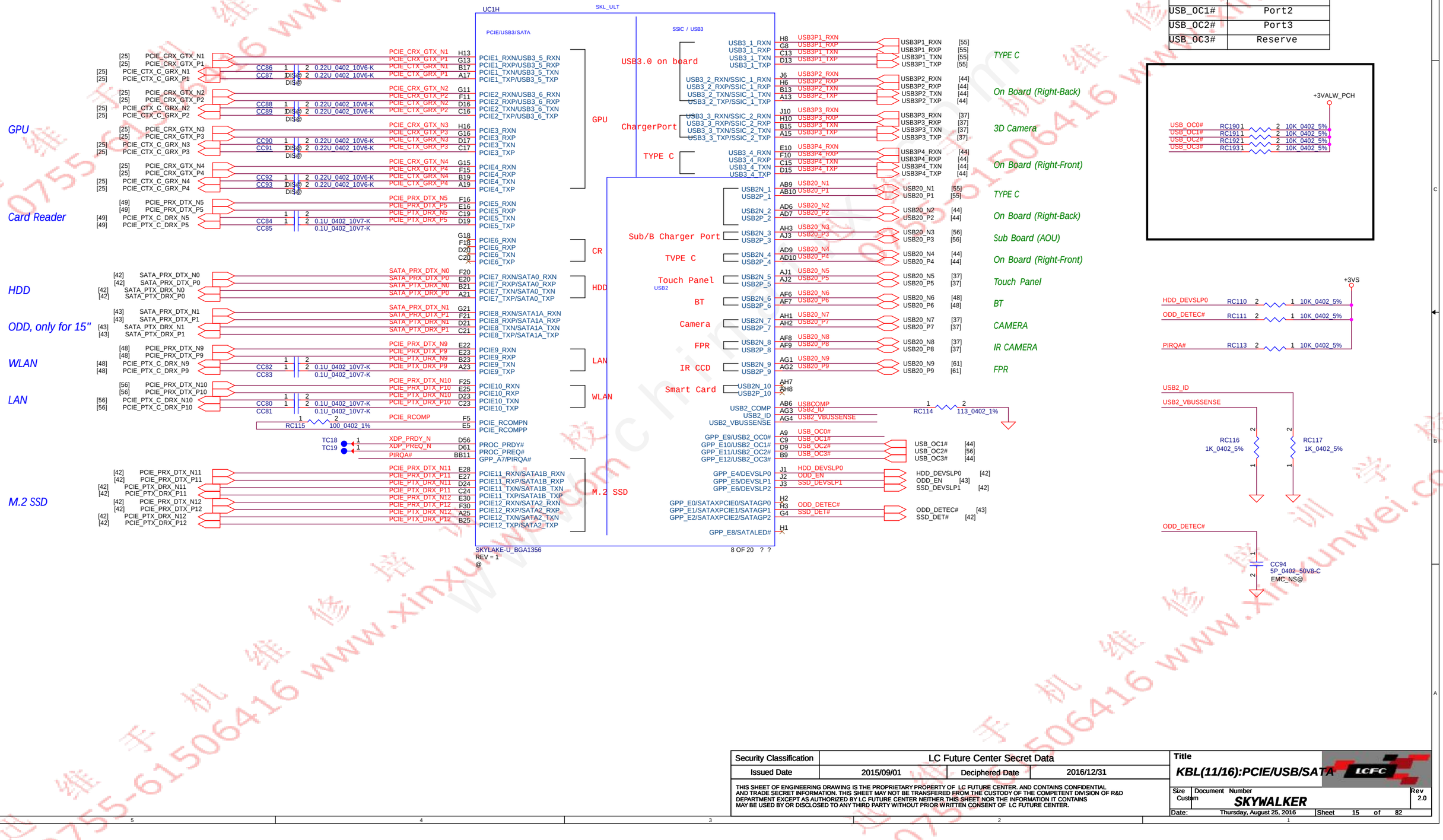


| | USB Port Number |
|---|---|
| USB_OC0# | Port1 |
| USB_OC1# | Port2 |
| USB_OC2# | Port3 |
| USB_OC3# | Reserve |

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **KBL(11/16):PCIE/USB/SATA**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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## Table 10-10. SVID Bus Routing Guidelines

| Signal | W1 [inches] | W2 [inches] | W3/4/5 [inches] | W2+W3+W4+W5 [inches] | W51 [inches] | W52 [inches] | $R_{PU1}$ [Ω] | $R_{PU2}$ [Ω] | $R_{S1}$ [Ω] | $R_{S2}$ [Ω] | $VCC_{ST}$ [V] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VIDSOUT | 0.5-3 | 1-15 | 0.5-4 | 3-17 | <0.1 | <0.1 | 100 | 100 | 0 | 10 | 1.0 |
| VIDSCK | | | | | | | Empty | 45 | 0 | 50 | |
| VIDALERT# | | | | | | | 56 | Empty | 220 | 0 | |

UC1L SKL_ULT
CPU POWER 1 OF 4
SKYLAKE-U_BGA1356 12 OF 20 ? ?
REV = 1
@

+VCC_CORE
VCC_A30 A30
VCC_A34 A34
VCC_A39 A39
VCC_A44 A44
VCC_AK33 AK33
VCC_AK35 AK35
VCC_AK37 AK37
VCC_AK38 AK38
VCC_AK40 AK40
VCC_AL33 AL33
VCC_AL37 AL37
VCC_AL40 AL40
VCC_AM32 AM32
VCC_AM33 AM33
VCC_AM35 AM35
VCC_AM37 AM37
VCC_AM38 AM38
VCC_G30 G30
RSVD_K32 K32
RSVD_AK32 AK32
VCCOPC_AB62 AB62
VCCOPC_P62 P62
VCCOPC_V62 V62
VCC_OPC_1P8_H63 H63
VCC_OPC_1P8_G61 G61
VCCOPC_SENSE AC63
VSSOPC_SENSE AE63
VCCEOPIO_AE62 AE62
VCCEOPIO_AG62 AG62
VCCEOPIO_SENSE AL63
VSSEOPIO_SENSE AJ62

+VCC_CORE
VCC_G32 G32
VCC_G33 G33
VCC_G35 G35
VCC_G37 G37
VCC_G38 G38
VCC_G40 G40
VCC_G42 G42
VCC_J30 J30
VCC_J33 J33
VCC_J37 J37
VCC_J40 J40
VCC_K33 K33
VCC_K35 K35
VCC_K37 K37
VCC_K38 K38
VCC_K40 K40
VCC_K42 K42
VCC_K43 K43
VCC_SENSE
VSS_SENSE
VIDALERT#
VIDSCK
VIDSOUT
VCCSTG_G20 G20

E32 VCC_SENSE_R 1 @ 2 RC121 0_0402_5%
E33 VSS_SENSE_R 1 @ 2 RC122 0_0402_5%
VCC_SENSE [70]
VSS_SENSE [70]
B63 VR_SVID_ALRT#_R
A63 VR_SVID_CLK
D64 VR_SVID_DAT
+VCC_STG

+VCC_CORE
RC120 100_0402_1%
RC123 100_0402_1%

+VCC_ST [KBL PDG]VIDSOUT
Rpu2
RC119 100_0402_1%
VR_SVID_DAT
VR_SVID_DAT [70]

+VCC_ST [KBL PDG]VIDSCK
Rpu1
RC124 100_0402_1%
VR_SVID_CLK
VR_SVID_CLK [70]

+VCC_ST [KBL PDG]VIDALERT#
Rpu1
RC125 56_0402_1%
Rs1
VR_SVID_ALRT#_R
RC126 220_0402_1%
VR_SVID_ALRT#
VR_SVID_ALRT# [70]

+VCC_GT
UC1M SKL_ULT
CPU POWER 2 OF 4
SKYLAKE-U_BGA1356 13 OF 20 ? ?
REV = 1
@

+VCC_GT
VCCGT_A48 A48
VCCGT_A53 A53
VCCGT_A58 A58
VCCGT_A62 A62
VCCGT_A66 A66
VCCGT_AA63 AA63
VCCGT_AA64 AA64
VCCGT_AA66 AA66
VCCGT_AA67 AA67
VCCGT_AA69 AA69
VCCGT_AA70 AA70
VCCGT_AA71 AA71
VCCGT_AC64 AC64
VCCGT_AC65 AC65
VCCGT_AC66 AC66
VCCGT_AC67 AC67
VCCGT_AC68 AC68
VCCGT_AC69 AC69
VCCGT_AC70 AC70
VCCGT_AC71 AC71
VCCGT_J43 J43
VCCGT_J45 J45
VCCGT_J46 J46
VCCGT_J48 J48
VCCGT_J50 J50
VCCGT_J52 J52
VCCGT_J53 J53
VCCGT_J55 J55
VCCGT_J56 J56
VCCGT_J58 J58
VCCGT_J60 J60
VCCGT_K48 K48
VCCGT_K50 K50
VCCGT_K52 K52
VCCGT_K53 K53
VCCGT_K55 K55
VCCGT_K56 K56
VCCGT_K58 K58
VCCGT_K60 K60
VCCGT_L62 L62
VCCGT_L63 L63
VCCGT_L64 L64
VCCGT_L65 L65
VCCGT_L66 L66
VCCGT_L67 L67
VCCGT_L68 L68
VCCGT_L69 L69
VCCGT_L70 L70
VCCGT_L71 L71
VCCGT_M62 M62
VCCGT_N63 N63
VCCGT_N64 N64
VCCGT_N66 N66
VCCGT_N67 N67
VCCGT_N69 N69
VCCGT_SENSE
VSSGT_SENSE

VCCGT_N70 N70
VCCGT_N71 N71
VCCGT_R63 R63
VCCGT_R64 R64
VCCGT_R65 R65
VCCGT_R66 R66
VCCGT_R67 R67
VCCGT_R68 R68
VCCGT_R69 R69
VCCGT_R70 R70
VCCGT_R71 R71
VCCGT_T62 T62
VCCGT_U65 U65
VCCGT_U65 U68
VCCGT_U68 U71
VCCGT_U71 W63
VCCGT_W63 W64
VCCGT_W64 W65
VCCGT_W65 W66
VCCGT_W66 W67
VCCGT_W67 W68
VCCGT_W68 W69
VCCGT_W69 W70
VCCGT_W70 W71
VCCGT_W71 Y62
VCCGT_Y62
VCCGTX_AK42 AK42
VCCGTX_AK43 AK43
VCCGTX_AK45 AK45
VCCGTX_AK46 AK46
VCCGTX_AK48 AK48
VCCGTX_AK50 AK50
VCCGTX_AK52 AK52
VCCGTX_AK53 AK53
VCCGTX_AK55 AK55
VCCGTX_AK56 AK56
VCCGTX_AK58 AK58
VCCGTX_AK60 AK60
VCCGTX_AK70 AK70
VCCGTX_AL43 AL43
VCCGTX_AL46 AL46
VCCGTX_AL50 AL50
VCCGTX_AL53 AL53
VCCGTX_AL56 AL56
VCCGTX_AL60 AL60
VCCGTX_AM48 AM48
VCCGTX_AM50 AM50
VCCGTX_AM52 AM52
VCCGTX_AM53 AM53
VCCGTX_AM56 AM56
VCCGTX_AM58 AM58
VCCGTX_AU58 AU58
VCCGTX_AU63 AU63
VCCGTX_BB57 BB57
VCCGTX_BB66 BB66
VCCGTX_SENSE AK62
VSSGTX_SENSE AL61

[70] VCCGT_SENSE
[70] VSSGT_SENSE
RC136 1 @ 2 0_0402_5% J70
RC137 1 @ 2 0_0402_5% J69
+VCC_GT
RC134 100_0402_1%
RC138 100_0402_1%

Place CC109 on bottom side
[SKL PDG]VCCSTG
[SKL PDG]1uF x1
Place CC110 on bottom side
[SKL PDG]VCCST
[SKL PDG]1uF x1
Place CC129 on bottom side
[SKL PDG]VDDQC
[SKL PDG]10uF x1
Place CC130 on bottom side
[SKL PDG]VCCPLL
[SKL PDG]1uF x1
+VCC_SFROC should be sourced from the VDDQ VR
Preferred to place the 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape

Place CC109 on bottom side
+1.2V
[KBL PDG]VDDQ
[KBL PDG]10uF x4

UC1N SKL_ULT
CPU POWER 3 OF 4
SKYLAKE-U_BGA1356 14 OF 20 ? ?
REV = 1
@

VDDQ_AU23 AU23
VDDQ_AU28 AU28
VDDQ_AU35 AU35
VDDQ_AU42 AU42
VDDQ_BB23 BB23
VDDQ_BB32 BB32
VDDQ_BB41 BB41
VDDQ_BB47 BB47
VDDQ_BB51 BB51
VDDQC AM40
VCCST A18
VCCSTG_A22 A22
VCCPLL_OC AL23
VCCPLL_K20 K20
VCCPLL_K21 K21
+1.2V
+VCC_ST
+VCC_STG
+VCC_SFROC
+VCC_SFR

VCCIO_AK28 AK28
VCCIO_AK30 AK30
VCCIO_AL30 AL30
VCCIO_AL42 AL42
VCCIO_AM28 AM28
VCCIO_AM30 AM30
VCCIO_AM42 AM42
VCCSA_AK23 AK23
VCCSA_AK25 AK25
VCCSA_G23 G23
VCCSA_G25 G25
VCCSA_G27 G27
VCCSA_G28 G28
VCCSA_J22 J22
VCCSA_J23 J23
VCCSA_J27 J27
VCCSA_K23 K23
VCCSA_K25 K25
VCCSA_K27 K27
VCCSA_K28 K28
VCCSA_K30 K30
VCCIO_SENSE AM23
VSSIO_SENSE AM22
VSSSA_SENSE H21
VCCSA_SENSE H20

+VCC_IO
[KBL PDG]VCCIO
[KBL PDG]1uF x4
Place decoupling cap on TOP side
CC102 CC104 CC103 CC105 1U_0402_10V6K

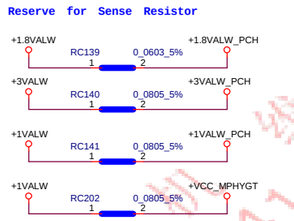
+VCC_SA
[KBL PDG]VCCSA
[KBL PDG]10uF x13, 1uF x7
Place decoupling cap on TOP side
CC114 CC115 CC116 CC117 CC118 CC119 10U_0603_6.3V6-M
CC120 CC121 CC122 CC124 CC123 CC126 CC125 CC127 1U_0402_10V6K

VCCIO_SENSE VCCIO_SENSE [70]
VSSIO_SENSE RC129 1 2 100_0402_1% +VCC_IO
RC130 1 2 100_0402_1%
RC131
VSSSA_SENSE_R 1 @ 2 0_0402_5%
VCCSA_SENSE_R 1 @ 2
0_0402_5% RC132
+VCC_SA
RC133 100_0402_1%
VSSSA_SENSE [70]
VCCSA_SENSE [70]
RC135 100_0402_1%

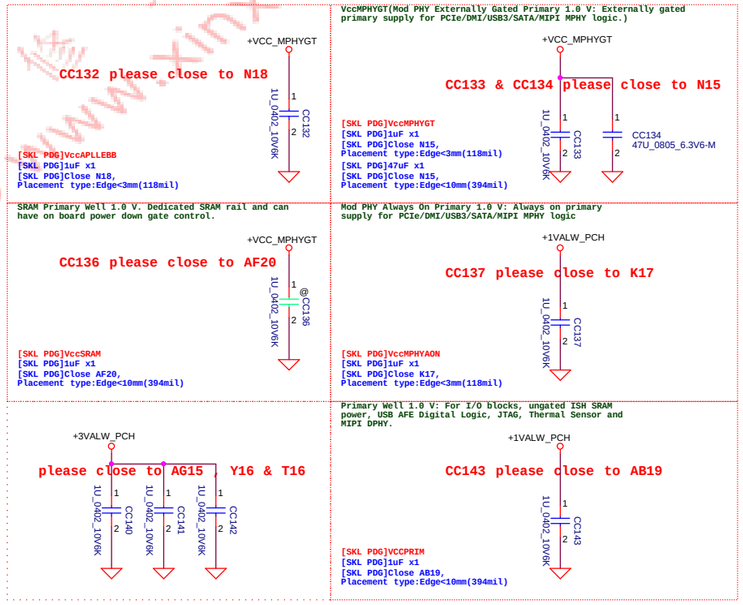
| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |

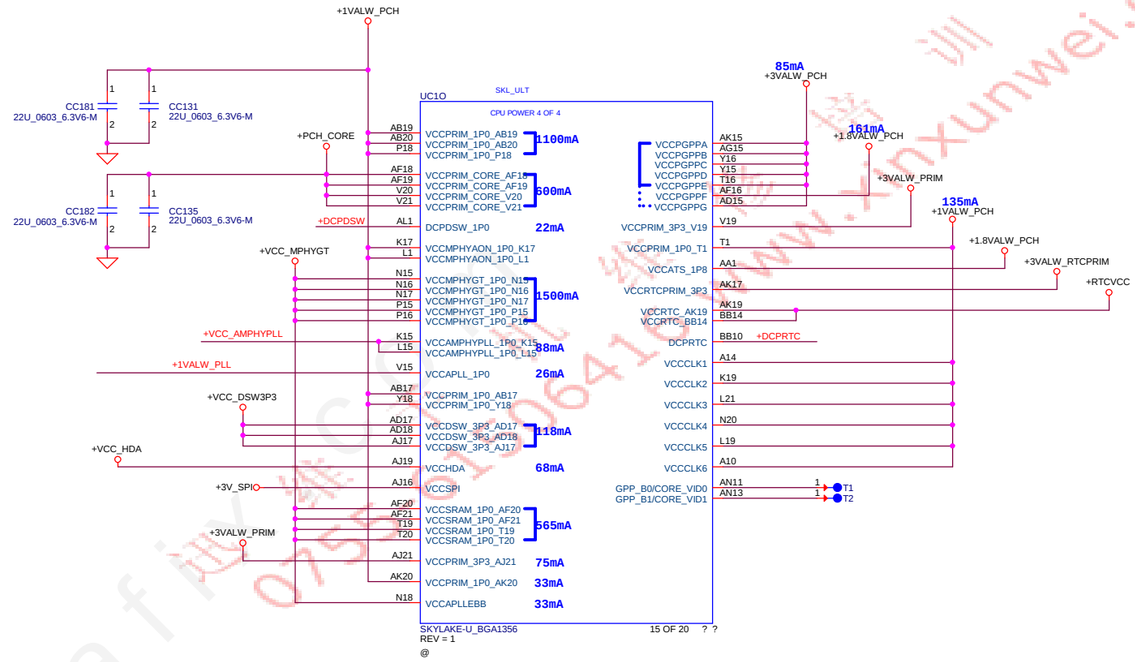


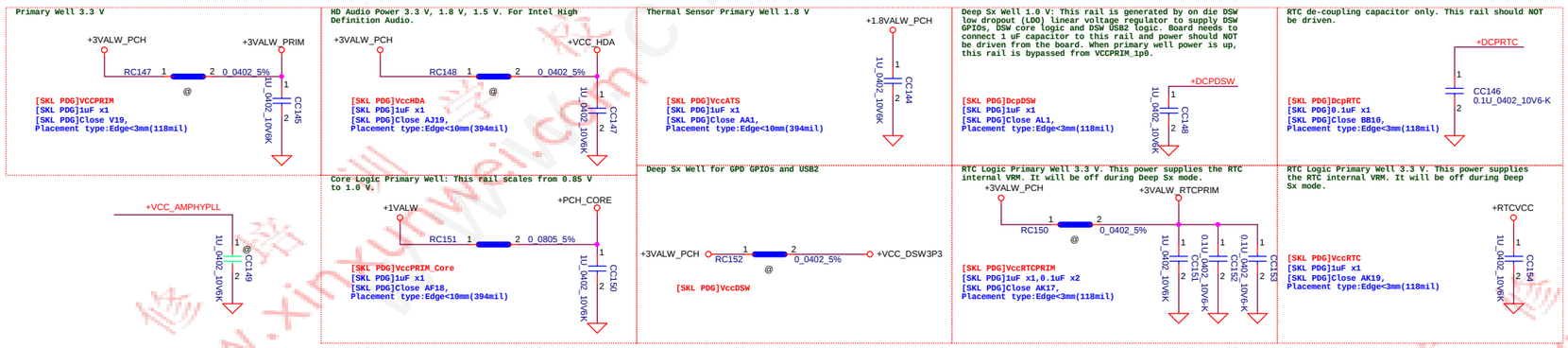
Title: KBL(12/16):POWER
Size: Custom | Document Number: SKYWALKER | Rev: 2.0
Date: Thursday, August 25, 2016 | Sheet 16 of 82





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| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



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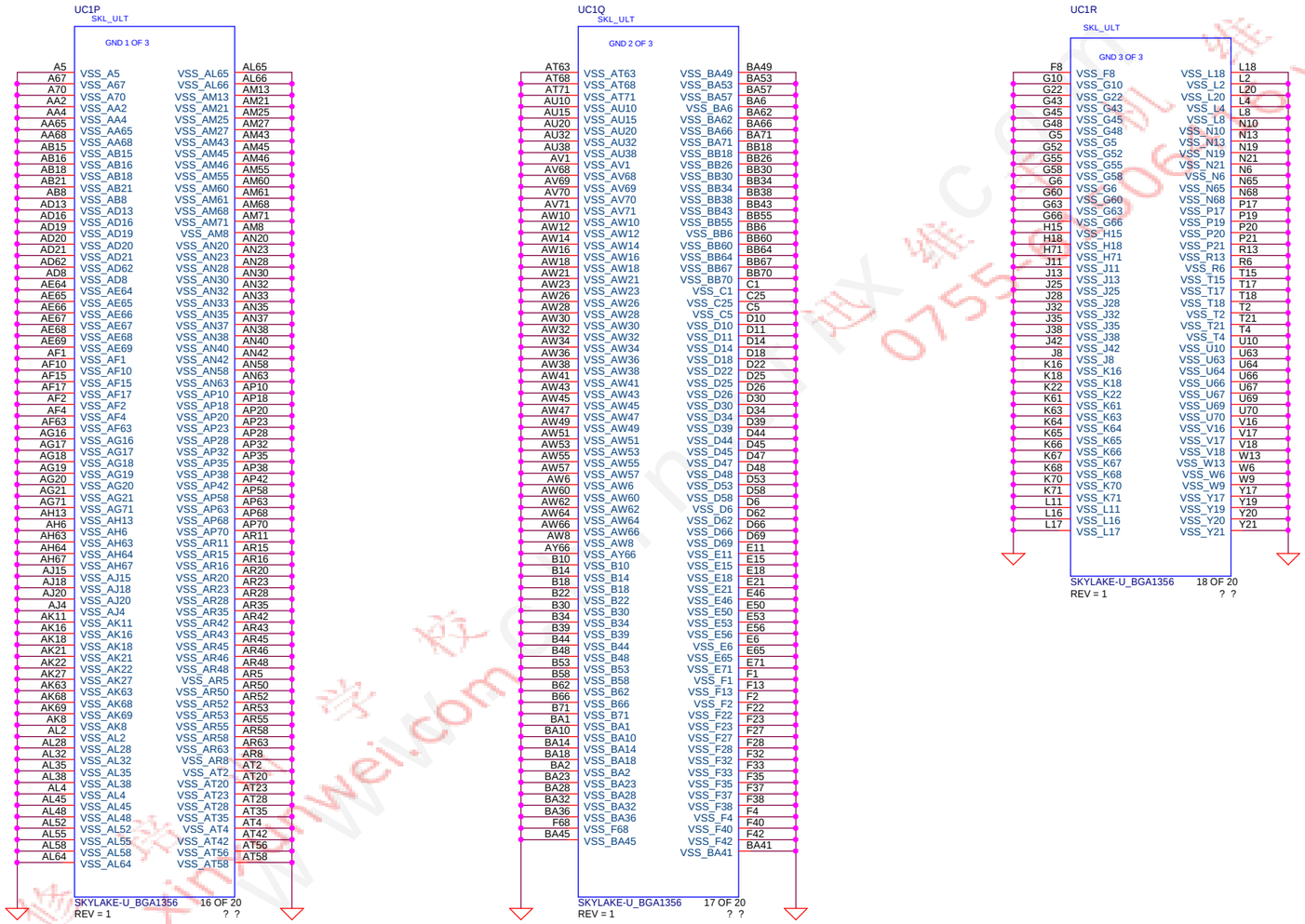


| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **KBL(14/16):GND**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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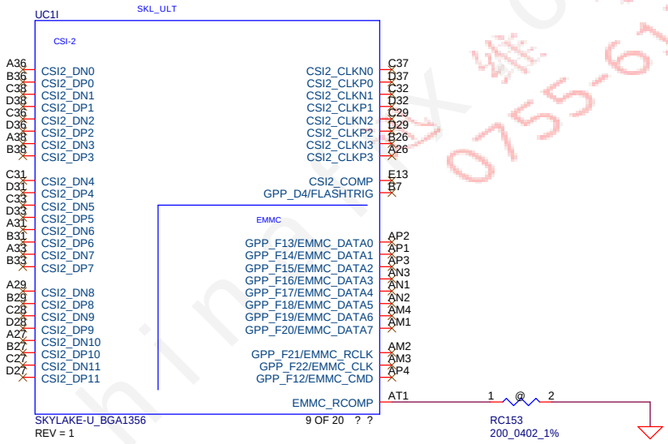


| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **KBL(15/16):CSI-2/EMMC**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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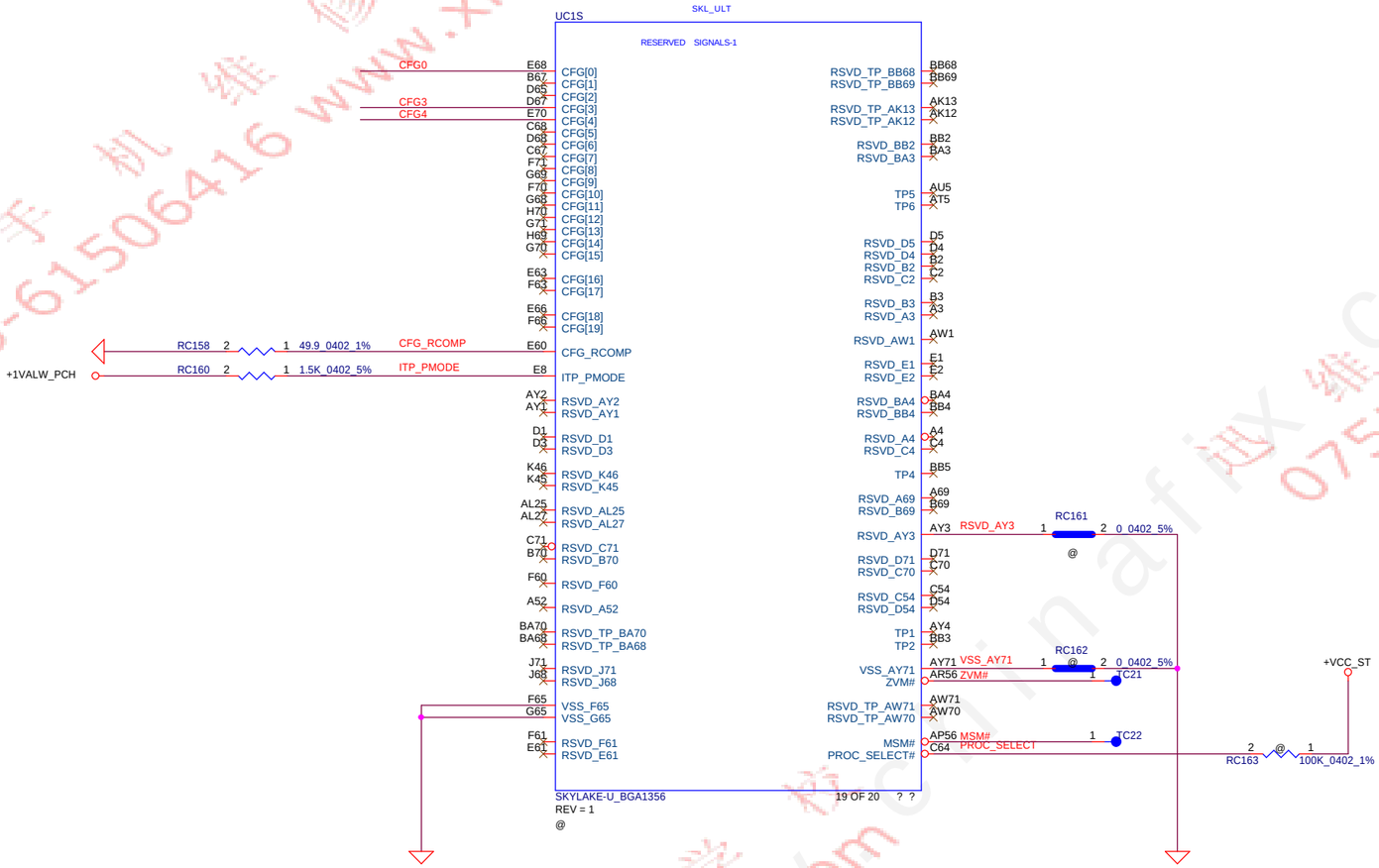
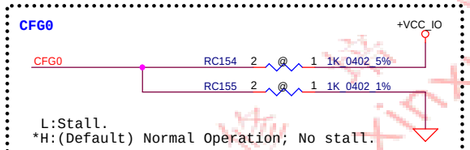


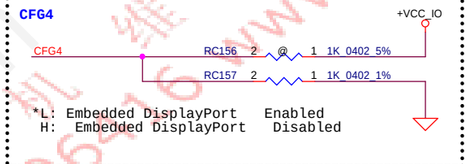

[SKL EDS]

**CFG0**



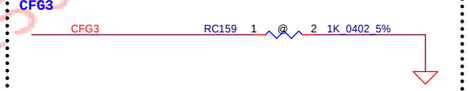

L:Stall.
*H:(Default) Normal Operation; No stall.

**CFG4**




*L: Embedded DisplayPort Enabled
H: Embedded DisplayPort Disabled

**CFG3**




CFG3 require >= 0.5"
CPU Debug Consent Strap

**TABLE**

| |
|---|
| **CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted**<br>**1 : No Stall**<br>**0 : Stall** |
| **CFG4 : eDP Enable**<br>**1 : Disabled**<br>**0 : Enabled** |

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: KBL(16/16):CFG/RESERVED

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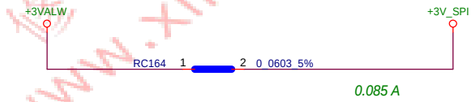
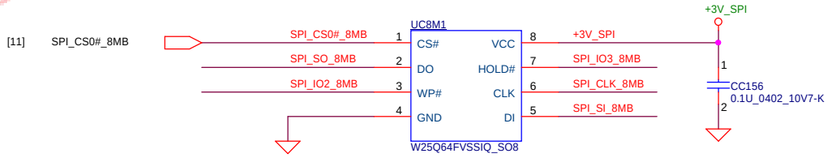
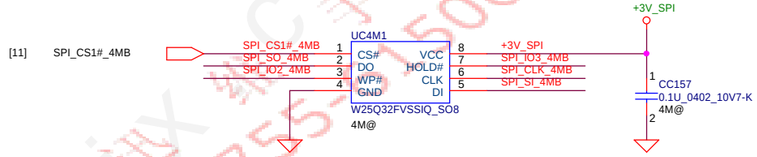



8MB(64Mb)

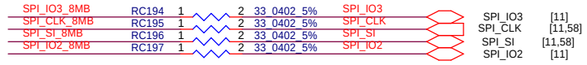
[SKL]SPI0_CS0#: SPI FLASH
SPI0_CS1#: SPI FLASH
SPI0_CS2#: SPI TPM




4MB(32Mb) Reserve



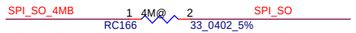

**Place RC194,195,196,197 close together**



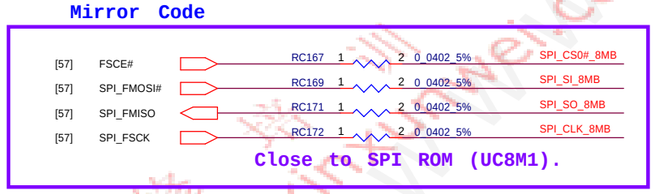

**Place RC203,204,205,206 close together**

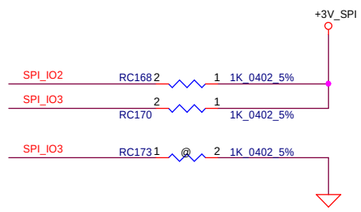

*Near SPI ROM*


*Near SPI ROM*




**Mirror Code**




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **SPI ROM**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins.
330uF placeholder

[KBL PDG]VDDQ
[KBL PDG] EE 10uF x16, 1uF x16. 330uF x1

+1.2V

CD1 10U_0603_6.3V6-M
CD2 10U_0603_6.3V6-M
CD3 10U_0603_6.3V6-M
CD4 10U_0603_6.3V6-M
CD5 10U_0603_6.3V6-M
CD6 10U_0603_6.3V6-M
CD7 10U_0603_6.3V6-M
CD8 10U_0603_6.3V6-M

+1.2V

CD14 1U_0402_6.3V6-K
CD15 1U_0402_6.3V6-K
CD16 1U_0402_6.3V6-K
CD17 1U_0402_6.3V6-K
CD18 1U_0402_6.3V6-K
CD19 1U_0402_6.3V6-K
CD20 1U_0402_6.3V6-K
CD21 1U_0402_6.3V6-K
CD26 330U_D2_2VM_R9M @

Place decoupling cap on DRAM side.

[KBL PDG]VPP
[KBL PDG] EE 10uF x2, 1uF x2.

+2.5V

CD9 10U_0603_6.3V6-M
CD10 10U_0603_6.3V6-M
CD11 1U_0402_6.3V6-K
CD12 1U_0402_6.3V6-K

Place decoupling on the VTT plane close to SODIMM

[KBL PDG]VTT
[KBL PDG] EE 10uF x2, 1uF x4.

+0.6VS

CD22 10U_0603_6.3V6-M
CD23 10U_0603_6.3V6-M
CD24 1U_0402_6.3V6-K
CD63 1U_0402_6.3V6-K
CD64 1U_0402_6.3V6-K
CD65 1U_0402_6.3V6-K

DDR_A_D[0..63] [7]
DDR_A_MA[0..16] [7]
DDR_A_DQS#[0..7] [7]
DDR_A_DQS[0..7] [7]

JDIMM1A ME@

| | | | | | |
|---|---|---|---|---|---|
| DDR_A_D5 | 1 | VSS_1 | VSS_2 | 2 | |
| | 3 | DQ5 | DQ4 | 4 | DDR_A_D0 |
| DDR_A_D1 | 5 | VSS_3 | VSS_4 | 6 | |
| | 7 | DQ1 | DQ0 | 8 | DDR_A_D4 |
| DDR_A_DQS#0 | 9 | VSS_5 | VSS_6 | 10 | |
| DDR_A_DQS0 | 11 | DQS0_C | DM0_n/DBI0_n | 12 | |
| | 13 | DQS0_t | VSS_7 | 14 | |
| DDR_A_D2 | 15 | VSS_8 | DQ6 | 16 | DDR_A_D6 |
| | 17 | DQ7 | VSS_9 | 18 | |
| DDR_A_D7 | 19 | VSS_10 | DQ2 | 20 | DDR_A_D3 |
| | 21 | DQ3 | VSS_11 | 22 | |
| DDR_A_D9 | 23 | VSS_12 | DQ12 | 24 | DDR_A_D8 |
| | 25 | DQ13 | VSS_13 | 26 | |
| DDR_A_D12 | 27 | VSS_14 | DQ8 | 28 | DDR_A_D13 |
| | 29 | DQ9 | VSS_15 | 30 | |
| | 31 | VSS_16 | DQS1_c | 32 | DDR_A_DQS#1 |
| | 33 | DM1_n/DBI1_n | DQS1_t | 34 | DDR_A_DQS1 |
| DDR_A_D10 | 35 | VSS_17 | VSS_18 | 36 | |
| | 37 | DQ15 | DQ14 | 38 | DDR_A_D11 |
| DDR_A_D15 | 39 | VSS_19 | VSS_20 | 40 | |
| | 41 | DQ10 | DQ11 | 42 | DDR_A_D14 |
| DDR_A_D16 | 43 | VSS_21 | VSS_22 | 44 | |
| | 45 | DQ21 | DQ20 | 46 | DDR_A_D17 |
| DDR_A_D20 | 47 | VSS_23 | VSS_24 | 48 | |
| | 49 | DQ17 | DQ16 | 50 | DDR_A_D21 |
| DDR_A_DQS#2 | 51 | VSS_25 | VSS_26 | 52 | |
| DDR_A_DQS2 | 53 | DQS2_c | DM2_n/DBI2_n | 54 | |
| | 55 | DQS2_t | VSS_27 | 56 | |
| DDR_A_D23 | 57 | VSS_28 | DQ22 | 58 | DDR_A_D22 |
| | 59 | DQ23 | VSS_29 | 60 | |
| DDR_A_D18 | 61 | VSS_30 | DQ18 | 62 | DDR_A_D19 |
| | 63 | DQ19 | VSS_31 | 64 | |
| DDR_A_D25 | 65 | VSS_32 | DQ28 | 66 | DDR_A_D29 |
| | 67 | DQ29 | VSS_33 | 68 | |
| DDR_A_D24 | 69 | VSS_34 | DQ24 | 70 | DDR_A_D28 |
| | 71 | DQ25 | VSS_35 | 72 | |
| | 73 | VSS_36 | DQS3_c | 74 | DDR_A_DQS#3 |
| | 75 | DM3_n/DBI3_n | DQS3_t | 76 | DDR_A_DQS3 |
| DDR_A_D30 | 77 | VSS_37 | VSS_38 | 78 | |
| | 79 | DQ30 | DQ31 | 80 | DDR_A_D31 |
| DDR_A_D26 | 81 | VSS_39 | VSS_40 | 82 | |
| | 83 | DQ26 | DQ27 | 84 | DDR_A_D27 |
| | 85 | VSS_41 | VSS_42 | 86 | |
| | 87 | CB5/NC | CB4/NC | 88 | |
| | 89 | VSS_43 | VSS_44 | 90 | |
| | 91 | CB1/NC | CB0/NC | 92 | |
| | 93 | VSS_45 | VSS_46 | 94 | |
| DDR_A_DQS#8 | 95 | DQS8_c | DM8_n/DBI8_n/NC | 96 | |
| DDR_A_DQS8 | 97 | DQS8_t | VSS_47 | 98 | |
| | 99 | VSS_48 | CB6/NC | 100 | |
| | 101 | CB2/NC | VSS_49 | 102 | |
| | 103 | VSS_50 | CB7/NC | 104 | |
| | 105 | CB3/NC | VSS_51 | 106 | |
| DDR_A_CKE0 | 107 | VSS_52 | RESET_n | 108 | DDR4_DRAMRST# [8,23] |
| | 109 | CKE0 | CKE1 | 110 | DDR_A_CKE1 [7] |
| DDR_A_BG1 | 111 | VDD_1 | VDD_2 | 112 | |
| [7] DDR_A_BG1 | 113 | BG1 | ACT_n | 114 | DDR_A_ACT_N |
| DDR_A_BG0 | 115 | BG0 | ALERT_n | 116 | DDR_A_ACT_N [7] |
| [7] DDR_A_BG0 | 117 | VDD_3 | VDD_4 | 118 | DDR_A_ALERT_N [7] |
| DDR_A_MA12 | 119 | A12 | A11 | 120 | DDR_A_MA11 |
| DDR_A_MA9 | 121 | A9 | A7 | 122 | DDR_A_MA7 |
| | 123 | A8 | A6 | 124 | |
| DDR_A_MA8 | 125 | VDD_5 | VDD_6 | 126 | DDR_A_MA5 |
| DDR_A_MA6 | 127 | A8 | A5 | 128 | DDR_A_MA4 |
| | 129 | A6 | A4 | 130 | |
| | | VDD_7 | VDD_8 | | |

FOX_AS0A826-H4RB-7H

+3VS

RD6 10K_0402_5% @ — SA0_CHA_P — RD9 0_0402_5%
RD7 10K_0402_5% @ — SA1_CHA_P — RD10 0_0402_5%
RD8 10K_0402_5% @ — SA2_CHA_P — RD11 0_0402_5%

SPD Address = 0H

[7] DDR_A_DDRCLK0_1866M
[7] DDR_A_DDRCLK0_1866M#
[7] DDR_A_PARITY
[7] DDR_A_BA1
[7] DDR_A_CS0#
[7] DDR_A_ODT0
[7] DDR_A_CS1#
[7] DDR_A_ODT1

JDIMM1B ME@

| | | | | | |
|---|---|---|---|---|---|
| DDR_A_MA3 | 131 | A3 | A2 | 132 | DDR_A_MA2 |
| DDR_A_MA1 | 133 | A1 | EVENT_n/NF | 134 | EVENT_n_1 |
| | 135 | VDD_9 | VDD_10 | 136 | |
| DDR_A_DDRCLK0_1866M | 137 | CK0_t | CK1_t/NF | 138 | DDR_A_DDRCLK1_1866M |
| DDR_A_DDRCLK0_1866M# | 139 | CK0_c | CK1_c/NF | 140 | DDR_A_DDRCLK1_1866M# |
| | 141 | VDD_11 | VDD_12 | 142 | |
| DDR_A_PARITY | 143 | Parity | A0 | 144 | DDR_A_MA0 |
| DDR_A_BA1 | 145 | BA1 | A10/AP | 146 | DDR_A_MA10 |
| | 147 | VDD_13 | VDD_14 | 148 | |
| DDR_A_CS0# | 149 | CS0_n | BA0 | 150 | DDR_A_BA0 |
| DDR_A_MA14 | 151 | A14/WE_n | A16/RAS_n | 152 | DDR_A_MA16 |
| | 153 | VDD_15 | VDD_16 | 154 | |
| DDR_A_ODT0 | 155 | ODT0 | A15/CAS_n | 156 | DDR_A_MA15 |
| DDR_A_CS1# | 157 | CS1_n | A13 | 158 | DDR_A_MA13 |
| | 159 | VDD_17 | VDD_18 | 160 | |
| DDR_A_ODT1 | 161 | ODT1 | C0/CS2_n/NC | 162 | |
| | 163 | VDD_19 | VREFCA | 164 | M_VREF_CA_DIMMA |
| | 165 | C1/CS3_n/NC | SA2 | 166 | SA2_CHA_P |
| DDR_A_D37 | 167 | VSS_53 | VSS_54 | 168 | |
| | 169 | DQ37 | DQ36 | 170 | DDR_A_D33 |
| DDR_A_D32 | 171 | VSS_55 | VSS_56 | 172 | |
| | 173 | DQ33 | DQ32 | 174 | DDR_A_D36 |
| DDR_A_DQS#4 | 175 | VSS_57 | VSS_58 | 176 | |
| DDR_A_DQS4 | 177 | DQS4_c | DM4_n/DBI4_n | 178 | |
| | 179 | DQS4_t | VSS_59 | 180 | |
| DDR_A_D38 | 181 | VSS_60 | DQ39 | 182 | DDR_A_D35 |
| | 183 | DQ38 | VSS_61 | 184 | |
| DDR_A_D39 | 185 | VSS_62 | DQ35 | 186 | DDR_A_D34 |
| | 187 | DQ34 | VSS_63 | 188 | |
| DDR_A_D40 | 189 | VSS_64 | DQ45 | 190 | DDR_A_D41 |
| | 191 | DQ44 | VSS_65 | 192 | |
| DDR_A_D44 | 193 | VSS_66 | DQ41 | 194 | DDR_A_D45 |
| | 195 | DQ40 | VSS_67 | 196 | |
| | 197 | VSS_68 | DQS5_c | 198 | DDR_A_DQS#5 |
| | 199 | DM5_n/DBI5_n | DQS5_t | 200 | DDR_A_DQS5 |
| DDR_A_D43 | 201 | VSS_69 | VSS_70 | 202 | |
| | 203 | DQ46 | DQ47 | 204 | DDR_A_D42 |
| DDR_A_D46 | 205 | VSS_71 | VSS_72 | 206 | |
| | 207 | DQ42 | DQ43 | 208 | DDR_A_D47 |
| DDR_A_D49 | 209 | VSS_73 | VSS_74 | 210 | |
| | 211 | DQ52 | DQ53 | 212 | DDR_A_D48 |
| DDR_A_D52 | 213 | VSS_75 | VSS_76 | 214 | |
| | 215 | DQ49 | DQ48 | 216 | DDR_A_D53 |
| DDR_A_DQS#6 | 217 | VSS_77 | VSS_78 | 218 | |
| DDR_A_DQS6 | 219 | DQS6_c | DM6_n/DBI6_n | 220 | |
| DDR_A_D50 | 221 | DQS6_t | VSS_79 | 222 | |
| | 223 | VSS_80 | DQ54 | 224 | DDR_A_D54 |
| DDR_A_D55 | 225 | DQS5 | VSS_81 | 226 | |
| | 227 | VSS_82 | DQ50 | 228 | DDR_A_D51 |
| DDR_A_D56 | 229 | DQ51 | VSS_83 | 230 | |
| | 231 | VSS_84 | DQ60 | 232 | DDR_A_D57 |
| DDR_A_D60 | 233 | DQ61 | VSS_85 | 234 | |
| | 235 | VSS_86 | DQ57 | 236 | DDR_A_D61 |
| | 237 | DQ56 | VSS_87 | 238 | |
| | 239 | VSS_88 | DQS7_c | 240 | DDR_A_DQS#7 |
| | 241 | DM7_n/DBI7_n | DQS7_t | 242 | DDR_A_DQS7 |
| DDR_A_D59 | 243 | VSS_89 | VSS_90 | 244 | |
| | 245 | DQ62 | DQ63 | 246 | DDR_A_D63 |
| DDR_A_D58 | 247 | VSS_91 | VSS_92 | 248 | |
| | 249 | DQ58 | DQ59 | 250 | DDR_A_D62 |
| CP_SMB_CLK | 251 | VSS_93 | VSS_94 | 252 | |
| | 253 | SCL | SDA | 254 | CP_SMB_DAT |
| | 255 | VDDSPD | SA0 | 256 | SA0_CHA_P |
| | 257 | VPP_1 | VTT | 258 | |
| | 259 | VPP_2 | SA1 | 260 | SA1_CHA_P |
| | 261 | GND_1 | GND_2 | 262 | |

FOX_AS0A826-H4RB-7H

RF

+1.2V — RD5 240_0402_1%

[11,23,63] CP_SMB_CLK — CP_SMB_DAT [11,23,63]

+3VS — RD12 0_0402_5%

[KBL PDG]VDDSPD
[KBL PDG] EE 0.1uF x1, 2.2uF x1.

CD29 0.1U_0402_10V7-K
CD30 2.2U_0402_6.3V6-M

Place decoupling cap close to DIMM

+1.2V — CD27 2.2U_0402_6.3V6-M @ — CD28 0.1U_0402_10V7-K @

+1.2V — RD1 1K_0402_1%

[7] DDR4_VREF_CA_CPU_A — RD2 2_0402_1% — M_VREF_CA_DIMMA

CD13 0.022U_0402_25V7-K
RD3 1K_0402_1%
RD4 24.9_0402_1%
CD25 0.1U_0402_16V7-K @

+1.2V — RD13 240_0402_1% — RD14 240_0402_1%

DDR_A_DQS#8
DDR_A_DQS8

| Signal Name | Description | Dir. | Buffer Type | Link Type | Availability |
|---|---|---|---|---|---|
| DDR0_DQSP[8:0]<br>DDR0_DQSN[8:0]<br>DDR1_DQSP[8:0]<br>DDR1_DQSN[8:0] | **Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions. | I/O | DDR4/-R5 | Diff | The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors |

| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |

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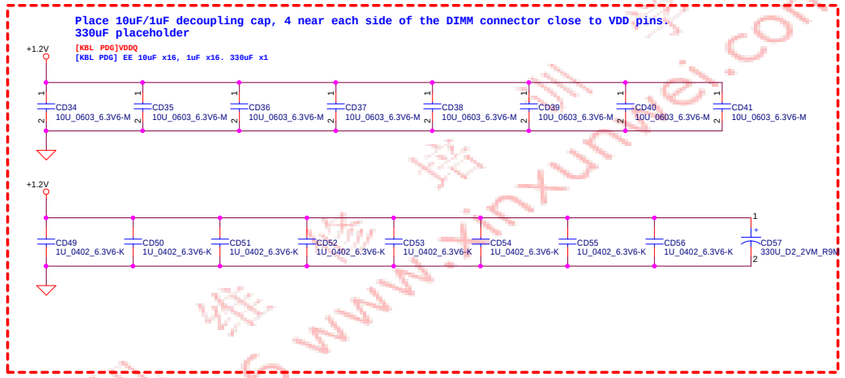
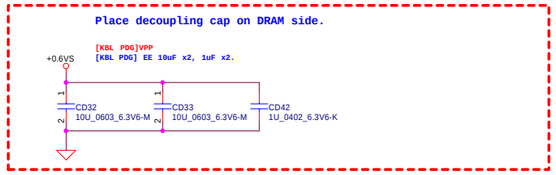
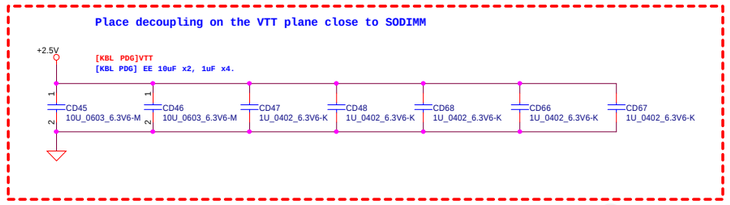
Title: DDR4 CH-A PRIMARY

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

Date: Thursday, August 25, 2016 | Sheet 22 of 82

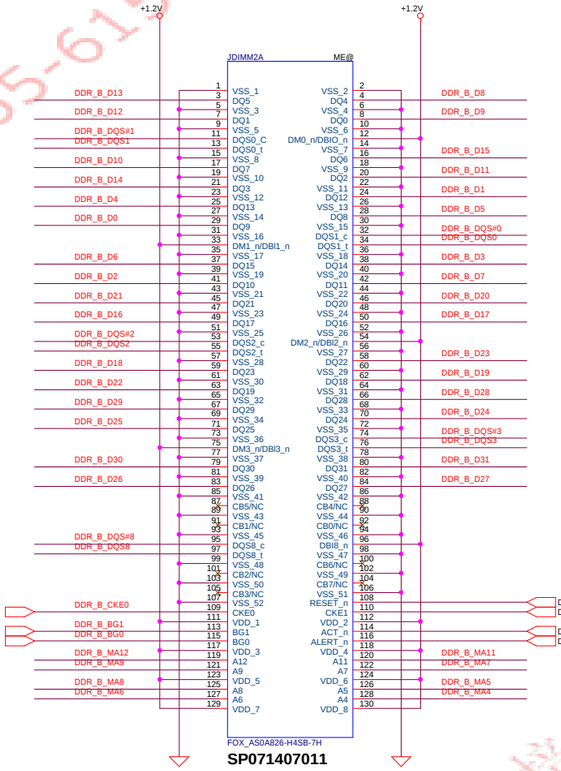


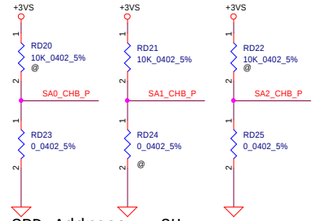




Layout Node:
Place Close DIMMs

DDR_B_D[0..63] [8]
DDR_B_MA[0..16] [8]
DDR_B_DQS#[0..7] [8]
DDR_B_DQS[0..7] [8]

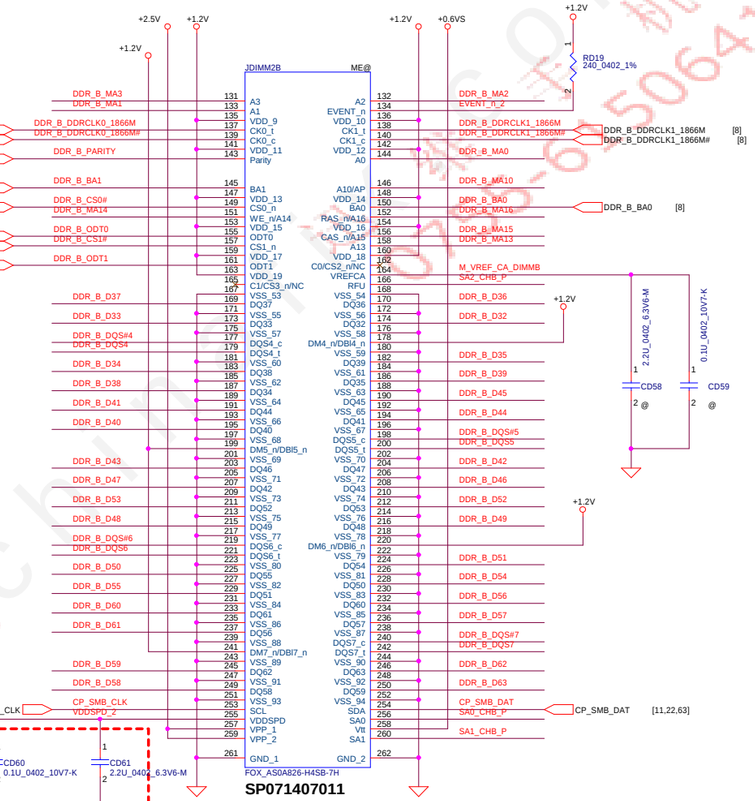


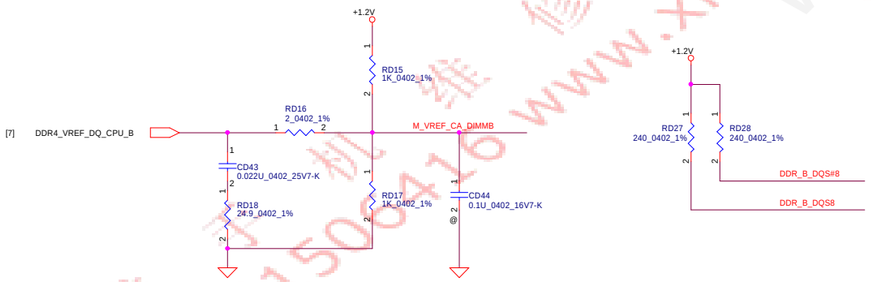













| Signal Name | Description | Dir. | Buffer Type | Link Type | Availability |
|---|---|---|---|---|---|
| DDR0_DQSP[8:0]<br>DDR0_DQSN[8:0]<br>DDR1_DQSP[8:0]<br>DDR1_DQSN[8:0] | **Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions. | I/O | DDR4/-R5 | Diff | The 9th signals[8] are applicable for UDIMM/ SODIMM module with ECC in S and H-processor line processors |

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: DDR4 CH-B PRIMARY

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |
| Date: Thursday, August 25, 2016 | Sheet 23 of 82 | |

| Physical Strapping pin | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|---|---|---|---|---|---|
| ROM_SCLK | +3VS_AON | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| ROM_SI | +3VS_AON | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] |
| ROM_SO | +3VS_AON | DEVID_SEL | PCIE_CFG | SMB_ALT_ADDR | VGA_DEVICE |
| STRAP0 | +3VS_AON | Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up) | | | |
| STRAP1 | +3VS_AON | Reserved(keep pull-up and pull-down footprint and not stuff by default) | | | |
| STRAP2 | +3VS_AON | | | | |
| STRAP3 | +3VS_AON | | | | |
| STRAP4 | +3VS_AON | | | | |

| DEVID_SEL | |
|---|---|
| 0 | (Default) |
| 1 | |

| SMBUS_ALT_ADDR | |
|---|---|
| 0 | 0x9E (Default) |
| 1 | 0x9C (Multi-GPU usage) |

| PCIE_CFG | |
|---|---|
| 0 | (Default) |
| 1 | |

| VGA_DEVICE | |
|---|---|
| 0 | 3D Device (Class Code 302h) |
| 1 | VGA Device (Default) |

*X76*

| GPU | FB Memory (GDDR5) | | ROM_SI | ROM_SO | ROM_SCLK | STRAP0 | STRAP1 | STRAP2 | STRAP3 | STRAP4 |
|---|---|---|---|---|---|---|---|---|---|---|
| N16P-GT | Samsung | K4G41325FE-HC28 | PD 45.3K | PD 5K | PD 5K | PU 50K | NC | NC | NC | NC |
| | Hynix | H5GC4H24AJR-T2C 256X16 | PD 34.8K | | | | | | | |
| | Micron | EDW4032BABG-60-F 256X16 | PD 24.9K | | | | | | | |

| Resistor Values | Pull-up to +3VGS | Pull-down to Gnd |
|---|---|---|
| 4.99K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 24.9K | 1100 | 0100 |
| 30.1K | 1101 | 0101 |
| 34.8K | 1110 | 0110 |
| 45.3K | 1111 | 0111 |

| GPU | FB Memory (GDDR5) | | ROM_SI | ROM_SO | ROM_SCLK | STRAP0 | STRAP1 | STRAP2 | STRAP3 | STRAP4 |
|---|---|---|---|---|---|---|---|---|---|---|
| N16S-GTR | Samsung | K4G80325FB-HC03 | PD 4.99K | PD 5K | PD 5K | PU 50K | NC | NC | NC | NC |
| | Hynix | H5GC8H24MJR-T2C | PD 30.1K | | | | | | | |
| | Micron | MT51J256M32HF-60:A | PD 10K | | | | | | | |



| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2015/10/5 | Deciphered Date | 2016/12/31 |

Title: VGA NOTE

| Size | Document Number | Rev |
|---|---|---|
| B | SKYWALKER | 2.0 |

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[15] PCIE_CTX_C_GRX_N[1..4]
[15] PCIE_CTX_C_GRX_P[1..4]
PCIE_CTX_C_GRX_N[1..4]
PCIE_CTX_C_GRX_P[1..4]
[15] PCIE_CRX_GTX_N[1..4]
[15] PCIE_CRX_GTX_P[1..4]
PCIE_CRX_GTX_N[1..4]
PCIE_CRX_GTX_P[1..4]

+3VS_AON
RV1 @ 1 2 10K_0402_5%

UV1A
1/18 PCI_EXPRESS
GM107/GM108 GK107/GK208 GF117
PEX_WAKE_N AJ11 | NC
PEX_RST_N AJ12
PEX_CLKREQ_N AK12
PEX_REFCLK AL13
PEX_REFCLK_N AK13
PEX_TX0 AK14
PEX_TX0_N AJ14
PEX_RX0 AN12
PEX_RX0_N AM12
PEX_TX1 AH14
PEX_TX1_N AG14
PEX_RX1 AN14
PEX_RX1_N AM14
PEX_TX2 AK15
PEX_TX2_N AJ15
PEX_RX2 AP14
PEX_RX2_N AP15
PEX_TX3 AL16
PEX_TX3_N AK16
PEX_RX3 AN15
PEX_RX3_N AM15
PEX_TX4 AK17
PEX_TX4_N AJ17
PEX_RX4 AN17
PEX_RX4_N AM17
PEX_TX5 AH17
PEX_TX5_N AG17
PEX_RX5 AP17
PEX_RX5_N AP18
PEX_TX6 AK18
PEX_TX6_N AJ18
PEX_RX6 AN18
PEX_RX6_N AM18
PEX_TX7 AL19
PEX_TX7_N AK19
PEX_RX7 AN20
PEX_RX7_N AM20
PEX_TX8 AK20
PEX_TX8_N AJ20
PEX_RX8 AP20
PEX_RX8_N AP21
PEX_TX9 AH20
PEX_TX9_N AG20
PEX_RX9 AN21
PEX_RX9_N AM21
PEX_TX10 AK21
PEX_TX10_N AJ21
PEX_RX10 AN23
PEX_RX10_N AM23
PEX_TX11 AL22
PEX_TX11_N AK22
PEX_RX11 AP23
PEX_RX11_N AP24
PEX_TX12 AK23
PEX_TX12_N AJ23
PEX_RX12 AN24
PEX_RX12_N AM24
PEX_TX13 AH23
PEX_TX13_N AG23
PEX_RX13 AN26
PEX_RX13_N AM26
PEX_TX14 AK24
PEX_TX14_N AJ24
PEX_RX14 AP26
PEX_RX14_N AP27
PEX_TX15 AL25
PEX_TX15_N AK25
PEX_RX15 AN27
PEX_RX15_N AM27
PEX LANES 4 TO 15 NC FOR GM108
PEX LANES 8 TO 15 NC FOR GK208/GF117
N16P-GX_BGA908

[28] VGA_PEX_RST# → VGA_PEX_RST#
RV11 DIS@ 2 1 0_0402_5%
CLKREQ_VGA#
[10] CLK_PCIE_VGA → CLK_PCIE_VGA
[10] CLK_PCIE_VGA# → CLK_PCIE_VGA#

PCIE_CRX_GTX_P1 — CV8 1 2 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_P1
PCIE_CRX_GTX_N1 — CV9 1 2 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_N1
PCIE_CRX_GTX_P2 — CV10 1 2 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_P2
PCIE_CRX_GTX_N2 — CV11 1 2 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_N2
PCIE_CRX_GTX_P3 — CV12 1 2 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_P3
PCIE_CRX_GTX_N3 — CV13 1 2 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_N3
PCIE_CRX_GTX_P4 — CV21 1 2 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_P4
PCIE_CRX_GTX_N4 — CV22 1 2 DIS@ 0.22U_0402_10V6-K — PCIE_CRX_C_GTX_N4

PCIE_CTX_C_GRX_P1 / PCIE_CTX_C_GRX_N1
PCIE_CTX_C_GRX_P2 / PCIE_CTX_C_GRX_N2
PCIE_CTX_C_GRX_P3 / PCIE_CTX_C_GRX_N3
PCIE_CTX_C_GRX_P4 / PCIE_CTX_C_GRX_N4

+3VS_AON
RV13 10K_0402_5% DIS@
DV1
[80] dgpu_pwrgd → dgpu_pwrgd
[79] VDDQPWRGD → VDDQPWRGD
All_GPU_PWRGD → All_GPU_PWRGD [11]
BAT54AW_SOT323-3
DIS@

+3VS
RV9212 DIS@ 10K_0402_5% dgpu_pwrgd
RV9222 DIS@ 10K_0402_5% VDDQPWRGD

+1.05VS_VGA

Under GPU
Near GPU
Midway between GPU and power supply

PEX_IOVDD_1 AG19
PEX_IOVDD_2 AG21
PEX_IOVDD_3 AG22
PEX_IOVDD_4 AG24
PEX_IOVDD_5 AH21
PEX_IOVDD_6 AH25
1UF_0402_6.3V6-K CV54 DIS@ | 1UF_0402_6.3V6-K CV55 DIS@
4.7U_0603_6.3VAK CV3 DIS@
10U_0603_6.3V6M CV4 DIS@ | 10U_0603_6.3V6M CV67 DIS@ | 22U_0603_6.3V6-M CV64 DIS@ | 22U_0603_6.3V6-M CV7 DIS@

PEX_IOVDDQ_01 AG13
PEX_IOVDDQ_02 AG15
PEX_IOVDDQ_03 AG16
PEX_IOVDDQ_04 AG18
PEX_IOVDDQ_05 AG25
PEX_IOVDDQ_06 AH15
PEX_IOVDDQ_07 AH18
PEX_IOVDDQ_08 AH26
PEX_IOVDDQ_09 AH27
PEX_IOVDDQ_10 AJ27
PEX_IOVDDQ_11 AK27
PEX_IOVDDQ_12 AL27
PEX_IOVDDQ_13 AM28
PEX_IOVDDQ_14 AN28
1UF_0402_6.3V6-K CV56 DIS@ | 1UF_0402_6.3V6-K CV57 DIS@
4.7U_0603_6.3VAK CV16 DIS@
10U_0603_6.3V6M CV17 DIS@ | 10U_0603_6.3V6M CV61 DIS@ | 22U_0603_6.3V6-M CV58 DIS@ | 22U_0603_6.3V6-M CV20 DIS@

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
+3VS_AON
0.1U_0402_10V7-K CV23 DIS@ | 4.7U_0402_6.3V6M CV24 DIS@ | 4.7U_0402_6.3V6M CV25 DIS@

+VGA_CORE
100_0402_1% RV2 DIS@
VDD_SENSE L4 → GFXCORE_VDD_SENSE_D [75]
GND_SENSE L5 → GFXCORE_GND_SENSE_D [75]
100_0402_1% RV3 DIS@

3V3AUX_NC P8

PEX_TSTCLK_OUT AJ26
PEX_TSTCLK_OUT_N AK26
RV6 @1 2 200_0402_1%

+1.05VS_VGA
0_0402_5% RV7 DIS@

PEX_PLLVDD AG26
Under GPU: CV26 DIS@ 0.1U_0402_25V7K
Near GPU: CV27 DIS@ 1UF_0402_6.3V6-K; CV28 DIS@ 4.7U_0402_6.3V6M

TESTMODE AK11

PEX_TERMP AP29
RV10 DIS@ 2.49K_0402_1%
RV8 DIS@ 10K_0402_5%

+3VS_AON
RV5 10K_0402_5% DIS@
QV1 DIS@ 2N7002KW_SOT323-3
[10] CLKREQ_PCIE4_VGA# → CLKREQ_VGA#
RV9 10K_0402_5% @
RV14 @ 1 2 0_0402_5%

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| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |

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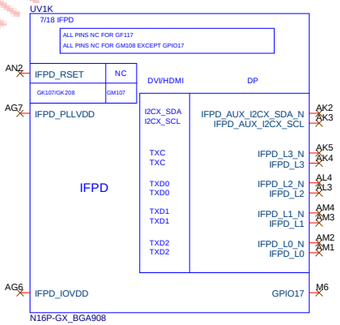
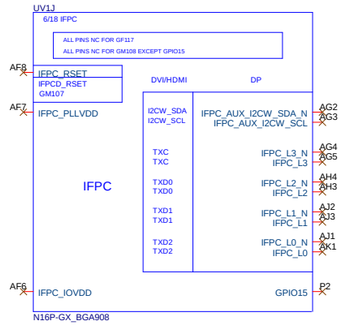
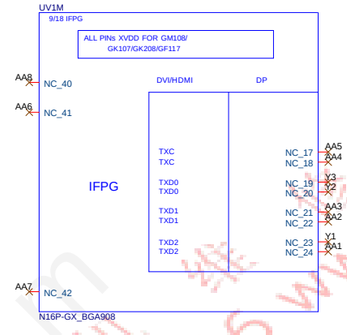
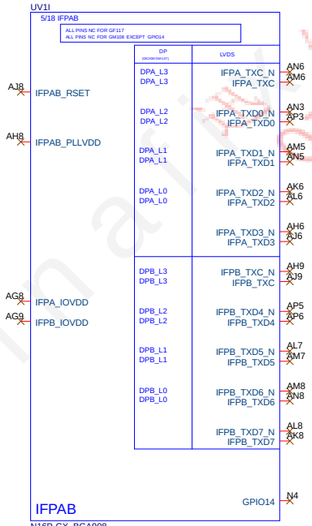
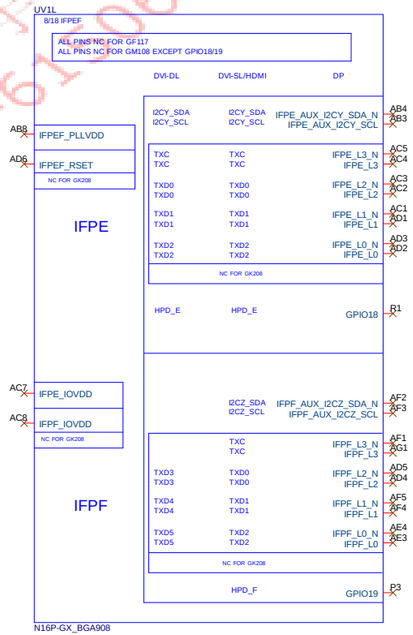
Title: N16P-Q1/Q3(1/6): PEG I/F
Size C | Document Number: SKYWALKER | Rev 2.0
Date: Thursday, August 25, 2016 | Sheet 25 of 82

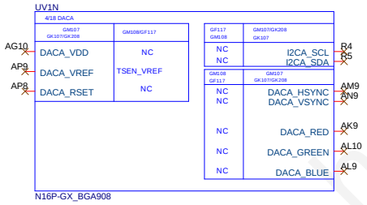
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Title: **N16P-Q1/Q3(2/6): DIGITAL OUT**

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|---|---|---|
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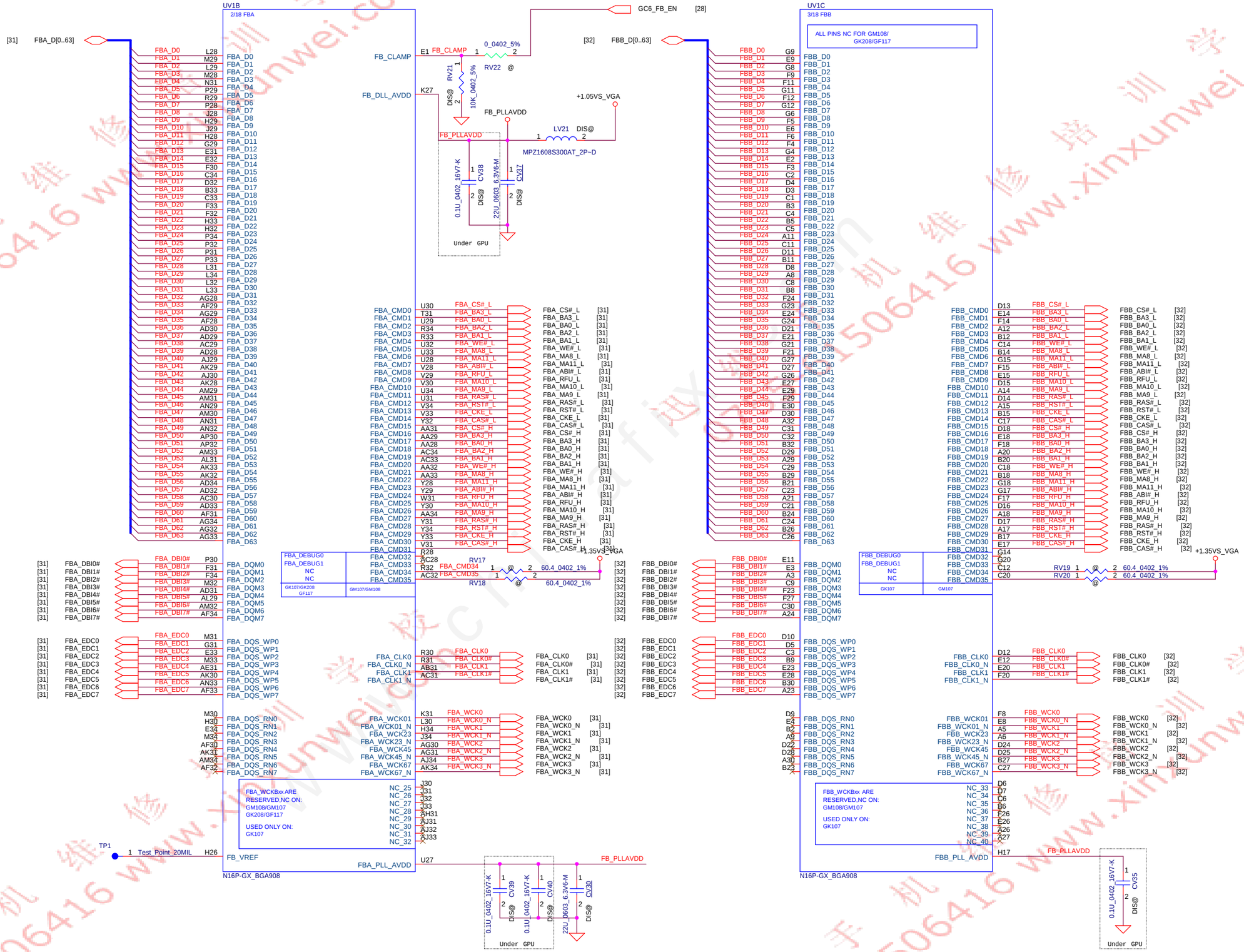


| FBx_PLL_AVDD | | |
|---|---|---|
| Capactior Type | GB4B-128/GDDR5 NV_DG | Actual |
| 0.1uF_0402 | 3 | 3 |
| 22uF_0805 | 1 | 1 |

| | | | |
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Title: 033_N16P-Q1/Q3(3/6): MEM I/F

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30ohm@100MHz ESR=0.01

+1.05VS_VGA

LV1 DIS@ MPZ1608S300AT_2P~D NEAR BALL

CV107 22U_0603_6.3V6-M DIS@

CV108 0.1U_0402_25V7K DIS@

112mA

LV2 PBY160808T-301Y-N_2P DIS@

CV101 22U_0603_6.3V6-M DIS@

CV102 10U_0603_6.3V6-M DIS@

CV103 0.1U_0402_25V7K DIS@

CV104 0.1U_0402_25V7K DIS@

UNDER GPU

RV104 DIS@ 0_0402_5%

VIDEO_CLK_XTAL_SS

50-ohm TRACE

RV108 10K_0402_5% DIS@

UV1P 12/18 XTAL_PLL

AD8 PLLVDD
AE8 SP_PLLVDD
AD7 VID_PLLVDD
H1 XTAL_SSIN
H3 XTAL_IN
J4 XTAL_OUTBUFF
H2 XTAL_OUT

GM107 GK107/GK208 GM108 GF117

N16P-GX_BGA908

+3VS_AON

RV125 10K_0402_5% @

RV109 10K_0402_5% DIS@

XTAL_OUTBUFF_GPU

@ RV110 1M_0402_5% 27MHZ_OUT

RV970 0_0201_5% DIS@

Crystal GND2 OUT IN GND1

27MHZ_IN GPU_XTAL_OUT_R

YV1 27MHZ_7PF_8Y27000005 DIS@

CV105 6.8P_0402_50V8-D DIS@

CV106 6.8P_0402_50V8-D DIS@

20160419
Add RV970 to reduce crystal driving level

+3VS_AON

RV129 RV111 RV112 RV113 RV114 10K_0402_1% @ DIS@ 493K_0402_1%

Strap0 = H
GC6 enable

RV115 RV116 RV117 RV118 RV119 10K_0402_1% @

STRAP0 STRAP1 STRAP2 STRAP3 STRAP4

UV1Q 13/18 MISC2

ROM_CS_N H6
ROM_SI H5
ROM_SO H7
ROM_SCLK H4
BUFRST_N L2

+3VS_VGA

RV101 RV102 RV106 4.99K_0402_1% @ 10K_0402_5%

RV105 RV103 RV107 4.99K_0402_1% X76@ DIS@

STRAP0 J2
STRAP1 J7
STRAP2 J6
STRAP3 J5
STRAP4 J3

STRAP0 STRAP1 STRAP2 STRAP3 STRAP4 NC NC NC NC

GK107/GK208 GF117 GM107 GM108

+3VS_AON

RV920 10K_0402_1% @

MULTI_STRAP_REF0_GND_GPU J1

MULTI_STRAP_REF0_GND

RV124 DIS@ 40.2K_0402_1%

N16P-GX_BGA908

UV1R 11/18 MISC1

VGA_OVERT# M1 OVERT GPIO8

THERMDN K4
THERMDP K3

I2CS_SCL I2CS_SDA T4 T3
I2CC_SCL I2CC_SDA R2 R3
I2CB_SCL I2CB_SDA R7 R6

NC NC GF117 GM107/GM108 GK107/GK208

Test_Point_20MIL TP2 AM10
Test_Point_20MIL TP3 AP11
Test_Point_20MIL TP4 AM11
Test_Point_20MIL TP5 AP12
AN11

JTAG_TCK JTAG_TMS JTAG_TDI JTAG_TDO JTAG_TRST_N

RV144 DIS@ 10K_0402_5%

GPIO0 P6 GC6_FB_EN
GPIO1 M3
GPIO2 L6
GPIO3 P5
GPIO4 P7
GPIO5 L7 VGA_MPWR_ON
GPIO6 M7 VGA_EVENT#
GPIO7 N8
GPIO8 L5 SYS_PEX_RST_MON
GPIO9 M2 VGA_ALERT#
GPIO10 L1 MEM_VREF
GPIO11 M5 VGA_PWM_VID
GPIO12 N3 VGA_PWR_LIM_D
GPIO13 M4 VGA_PSI
GPIO16 R8
GPIO20 P4
GPIO21 P1 GPU_PEX_RST_HOLD

GK107/GK208/GF117 NC

GPIO10 NC GPIO16
GPIO20 NC NC
GPIO8 NC NC
GK208 GF117 GK107 GM107 GM108

N16P-GX_BGA908

GC6_FB_EN [27]
VGA_MPWR_ON [33]
SYS_PEX_RST_MON
VGA_ALERT#
MEM_VREF [31,32]
VGA_PWM_VID [75]
VGA_PWR_LIM_D [67]
VGA_PSI [75]
GPU_PEX_RST_HOLD

VGA_PWR_LIM_D DIS@ DV102 RB751V-40_SOD323-2 VGA_PWR_LIM VGA_PWR_LIM [57]

VGA_ALERT# DV103 RB751V-40_SOD323-2 @

+3VS_AON

RV120 RV121 2.2K_0402_5% DIS@

QV21B QV21A 2N7002KDWH_SOT363-6 DIS@

EC_SMB_CK3 [11,57,59,62]
EC_SMB_DA3 [11,57,59,62]

SMBUS to EC for Thermal

+3VS_AON

RV127 @ 10K_0402_1%

[75] DGFX_PWRGD DGFX_PWRGD RV925 @ 0_0402_5%

[33,75,80] VGA_ON VGA_ON RV143 DIS@ 0_0402_5%

GC6_FB_EN RV138 GC6@ 0_0402_5%

RV200 NGC6@ 0_0402_5%

DV101 GC6@ DAN222MGT2L_VMD3

FB_PWR_EN

FB_PWR_EN [79]

RV926 200K_0402_5% @

GC6_FB_EN_GPIO GC6_FB_EN_GPIO [9]

Connect to EC or PCH to indicate the GC6 status of GPU to the system

+3VS_AON

CV109 @ 0.1U_0402_10V6-K

GC6_FB_EN GC6_FB_EN_D RV141 DIS@ 0_0402_5% GC6_FB_EN_GPIO

QV102 @ 2N7002KW_SOT323-3

VGA_PEX_RST#

GPU Thermal shut down pin, sent to EC to control SLP_S3#

[57] WRST# WRST#

VGA_OVERT#

QV22 @ 2N7002W-T/R7_SOT323-3

CV112 @ 0.01U_0402_25V7-K

20160303
Correct VGA_OVERT# netname and unstuff QV22

+3VS_AON

RV130 DIS@ 10K_0402_1% VGA_MPWR_ON

RV123 @ 10K_0402_1% SYS_PEX_RST_MON

RV122 DIS@ 10K_0402_1% VGA_OVERT#

RV131 DIS@ 10K_0402_1% VGA_ALERT#

RV132 DIS@ 100K_0402_5% VGA_PWR_LIM_D

RV133 DIS@ 10K_0402_1% VGA_PSI

RV134 DIS@ 10K_0402_1% GPU_PEX_RST_HOLD

RV135 DIS@ 10K_0402_1% VGA_EVENT#

RV146 DIS@ 10K_0402_1% GC6_FB_EN

RV136 DIS@ 100K_0402_5% MEM_VREF

+3VS_AON

UV101 GC6@ 74LVC1G08GW_SOT353-1-5

SYS_PEX_RST_MON

VGA_PEX_RST# [25]

RV128 GC6@ 0_0402_5%

RV140 NGC6@ 0_0402_5% SYS_PEX_RST_MON_R

SYS_PEX_RST_MON_L

+3VS_AON

UV102 DIS@ 74LVC1G08GW_SOT353-1-5

DGPU_HOLD_RST# [9]

PLT_RST# [12,42,48,49,56,57,58]

GPIO from PCH

+3VS_AON

CV110 DIS@ 0.1U_0402_10V6-K

VGA_EVENT# GPU_EVENT#_R RV147 DIS@ 0_0402_5% GPU_EVENT#

QV101 DIS@ 2N7002KW_SOT323-3

RV145 @ 0_0402_5%

GPU_EVENT# [11]

PCH GPIO Pin to wake up GPU from GC6

X76

| GPU | FB Memory (GDDR5) | | ROM_SI | ROM_SO | ROM_SCLK | STRAP0 | STRAP1 | STRAP2 | STRAP3 | STRAP4 |
|---|---|---|---|---|---|---|---|---|---|---|
| N16P-GT | Samsung | K4G41325FE-HC28 | PD 45.3K | PD 5K | PD 5K | PU 50K | NC | NC | NC | NC |
| | Hynix | H5GC4H24AJR-T2C 256X16 | PD 34.8K | | | | | | | |
| | Micron | EDW4032BABG-60-F 256X16 | PD 24.9K | | | | | | | |

| GPU | FB Memory (GDDR5) | | ROM_SI | ROM_SO | ROM_SCLK | STRAP0 | STRAP1 | STRAP2 | STRAP3 | STRAP4 |
|---|---|---|---|---|---|---|---|---|---|---|
| N16S-GTR | Samsung | K4G80325FB-HC03 | PD 4.99K | PD 5K | PD 5K | PU 50K | NC | NC | NC | NC |
| | Hynix | H5GC8H24MJR-T2C | PD 30.1K | | | | | | | |
| | Micron | MT51J256M32HF-60:A | PD 10K | | | | | | | |

| | | |
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Title: 034_N16P-Q1/Q3(4/6): GPIO

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

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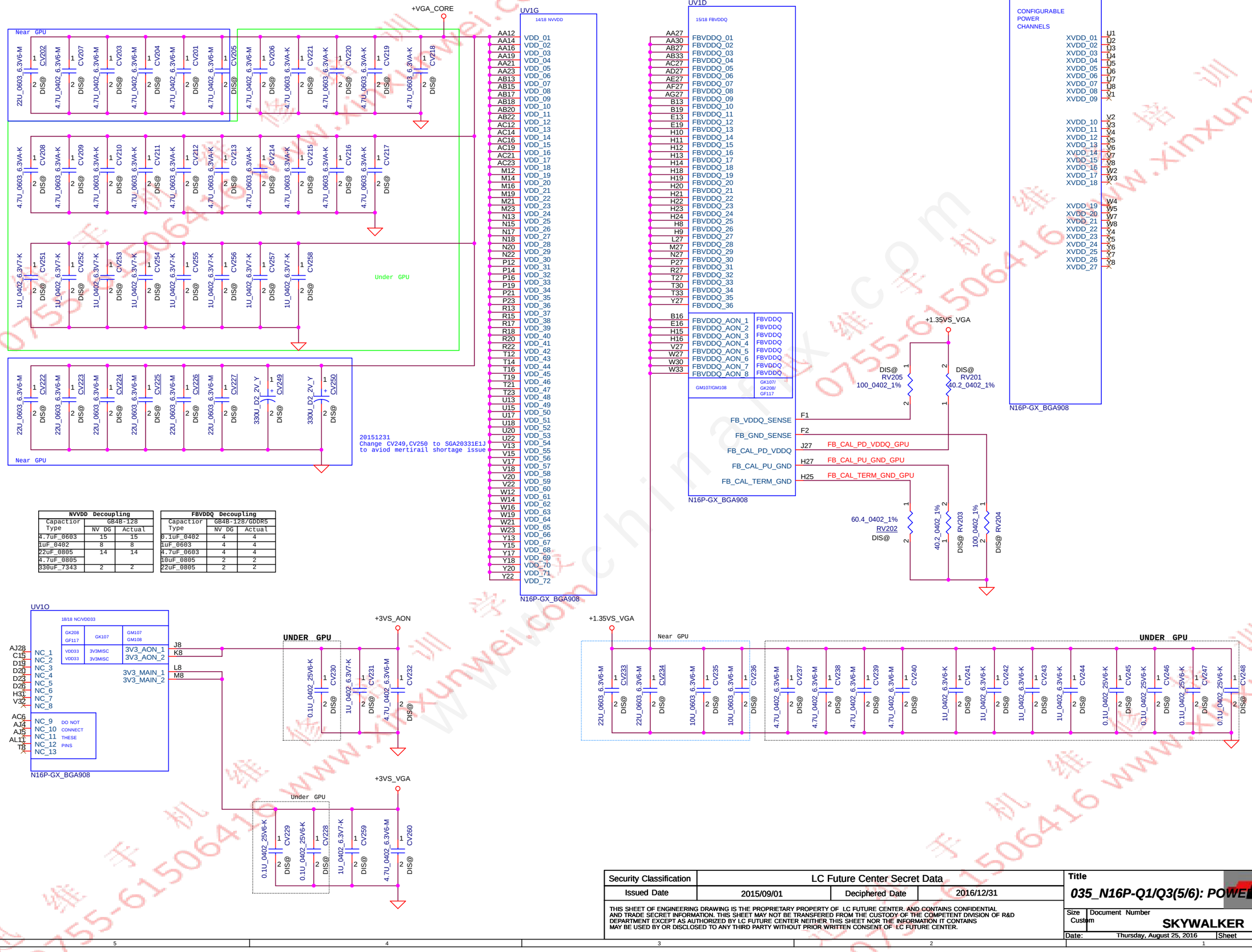


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| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: 035_N16P-Q1/Q3(5/6): POWER

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|---|---|---|
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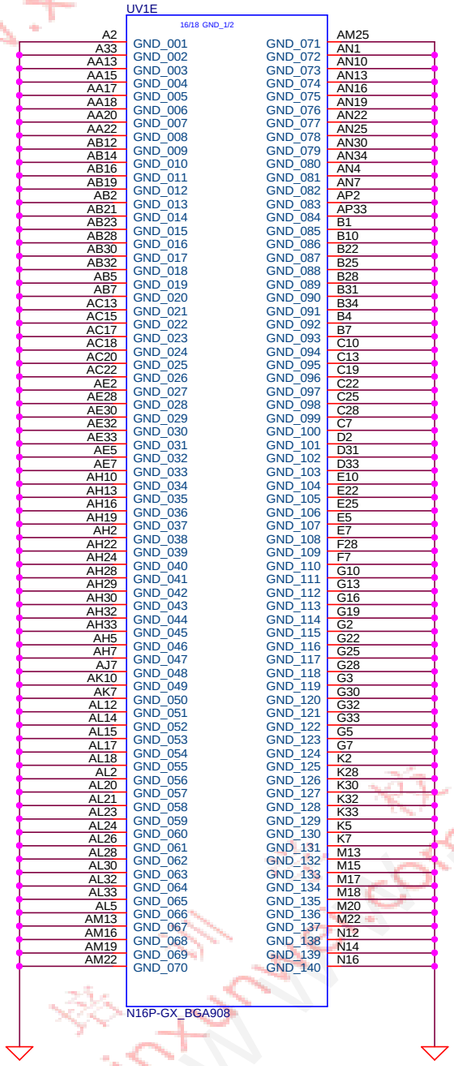


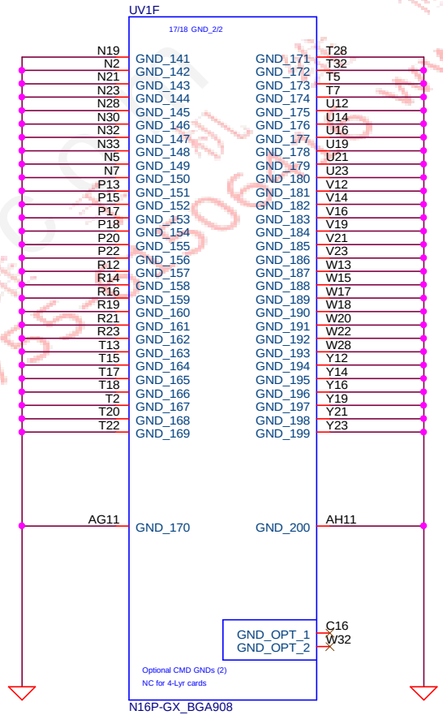


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Title: *036_N16P-Q1/Q3(6/6): GND*

| Size | Document Number | Rev |
|---|---|---|
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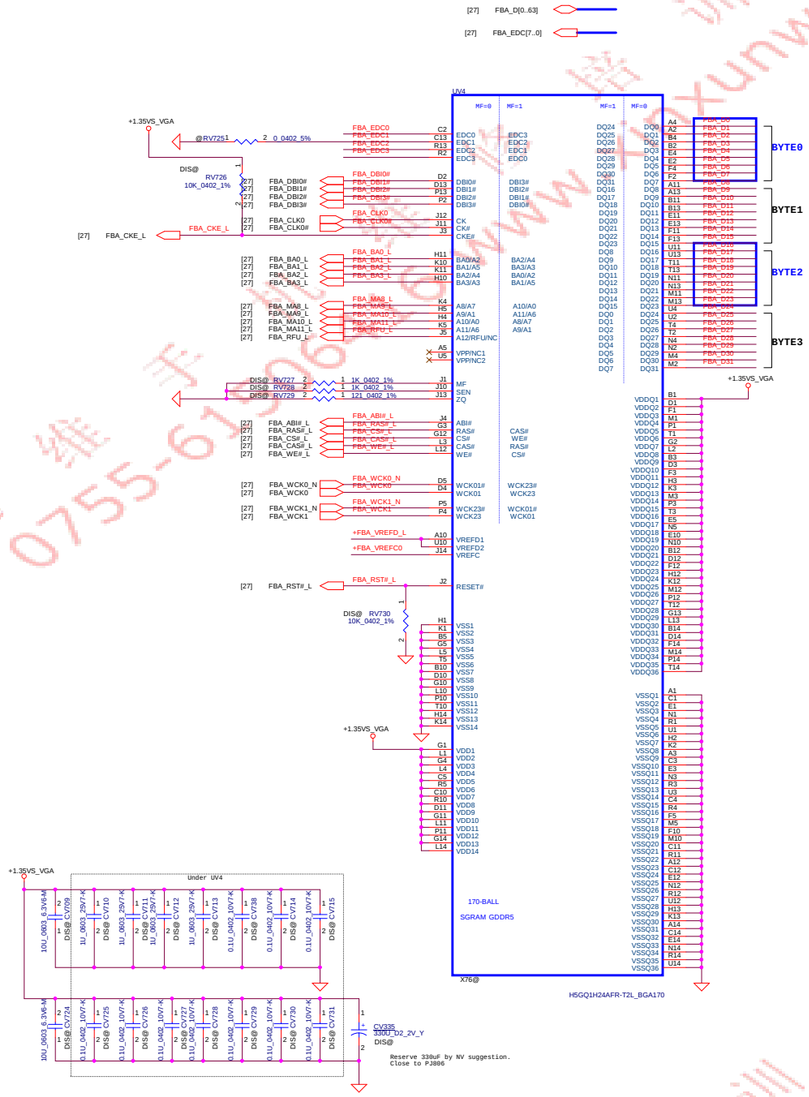


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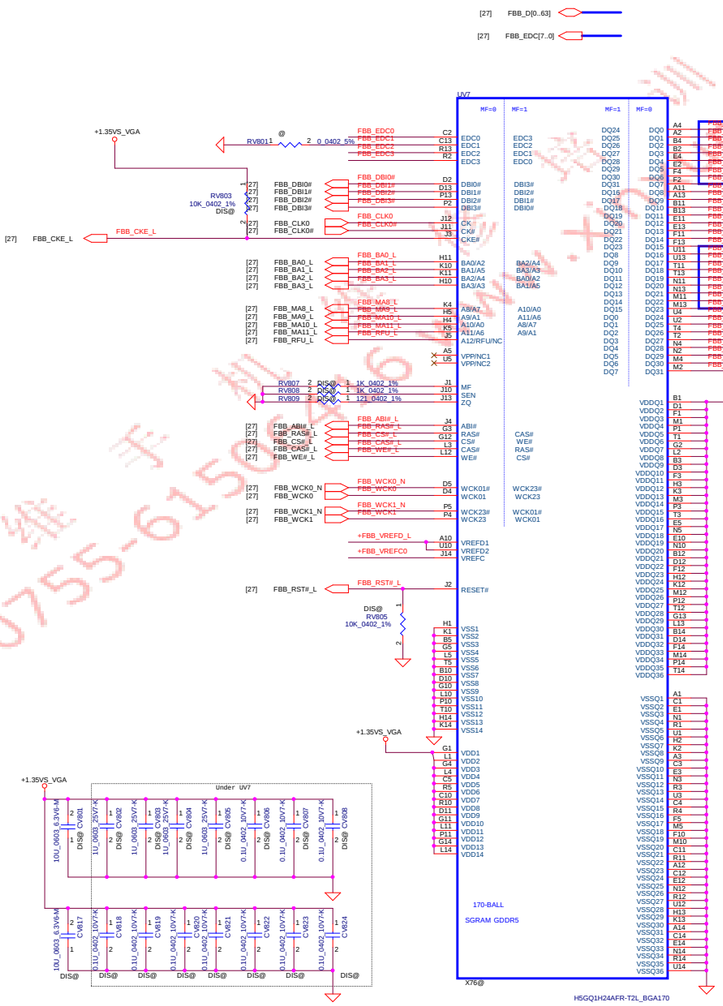
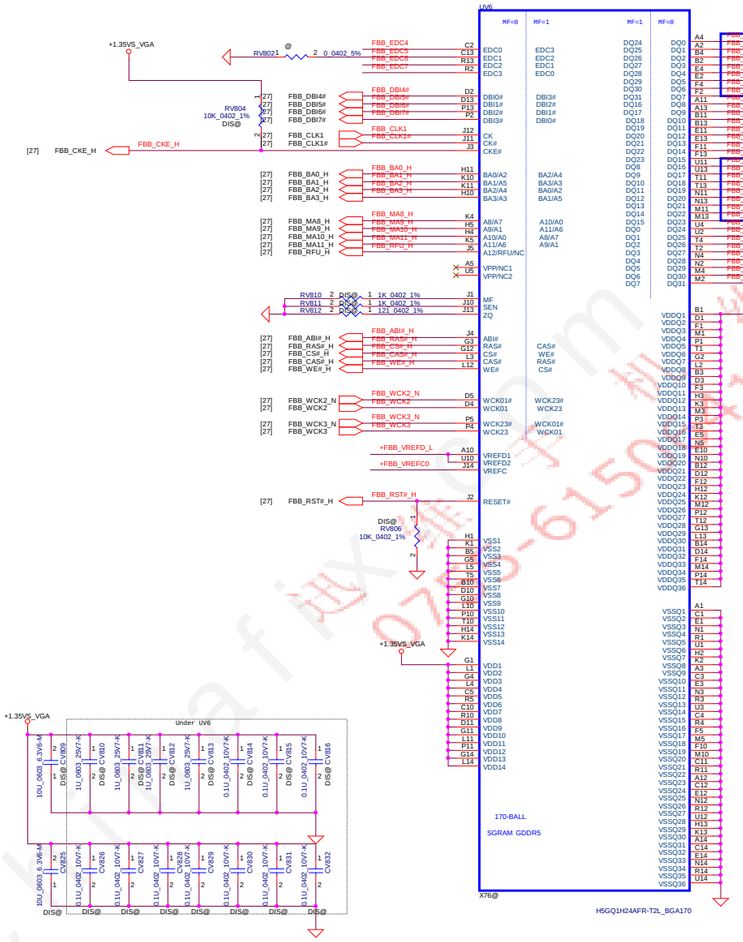
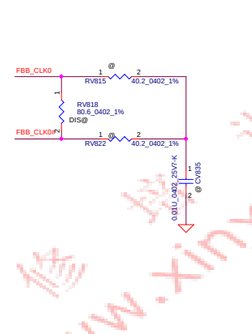
Title: VRAM CH_A

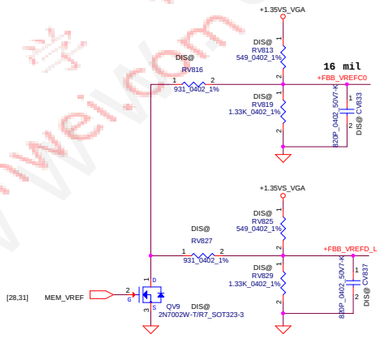
Size: Custom | Document Number: SKYWALKER | Rev: 2.0

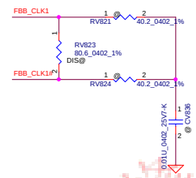
Date: Thursday, August 25, 2016 | Sheet 31 of 82

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Title: VRAM CH_B

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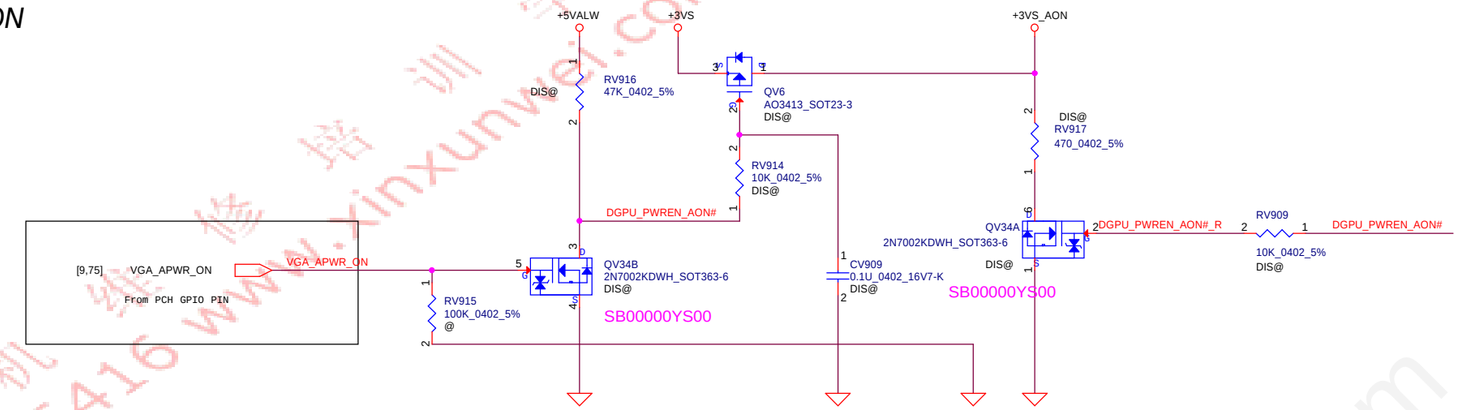
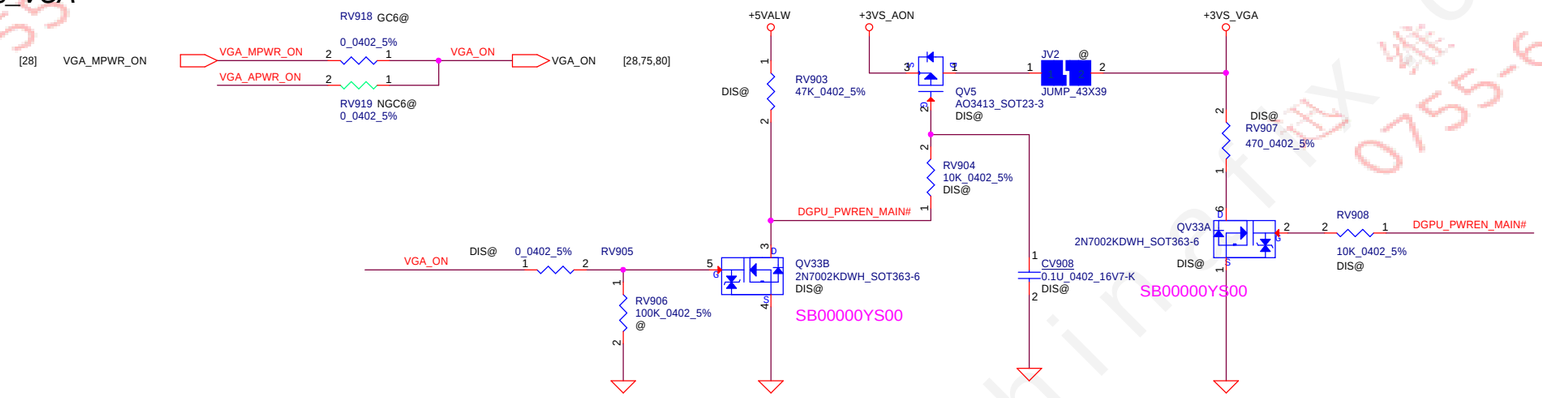
## +3VS to +3VS_AON

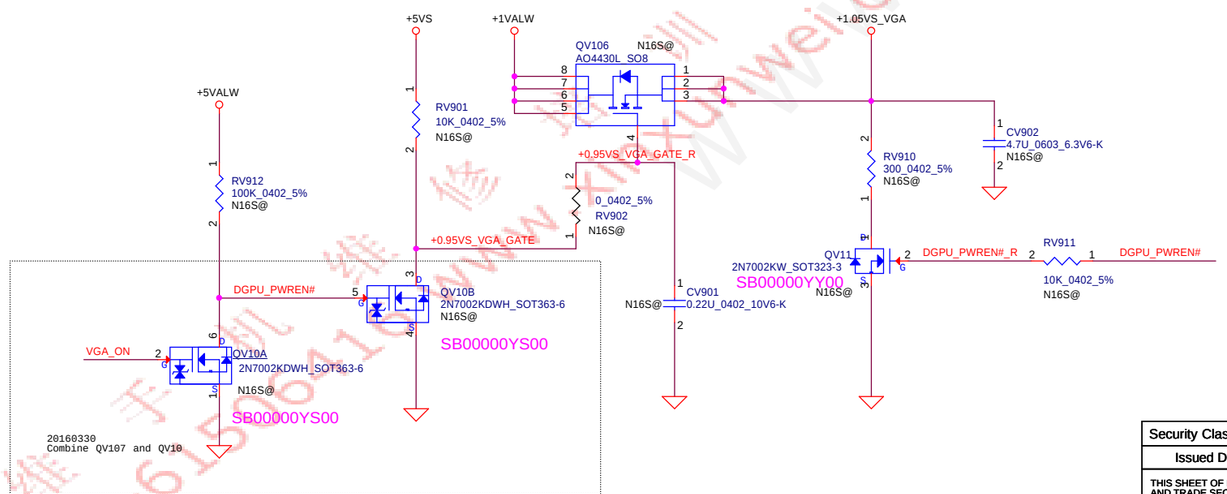


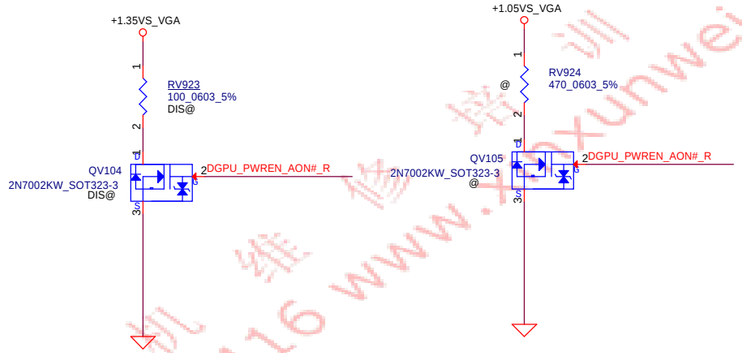

## +3VS_VGA




20160310
Add 1.05VS_VGA circuit for N16S GPU

## +1VALW to +1.05VS_VGA

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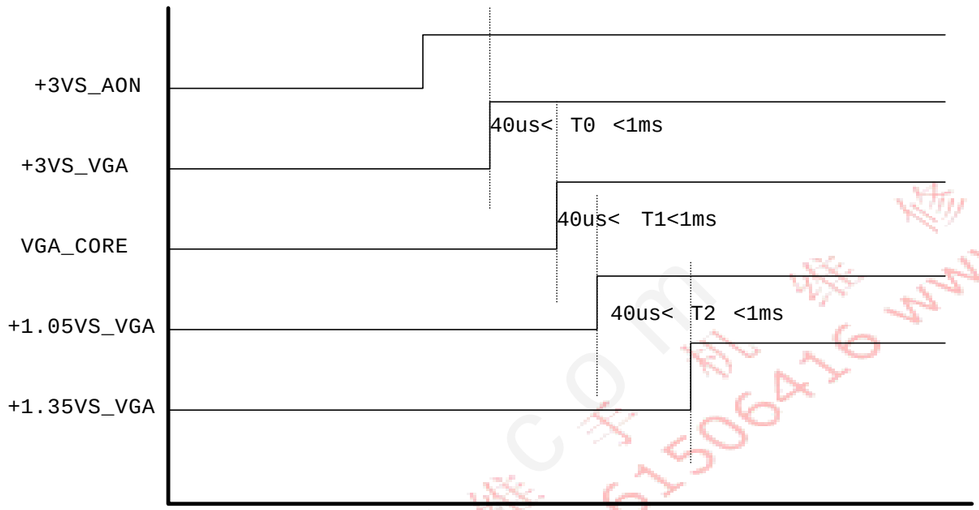
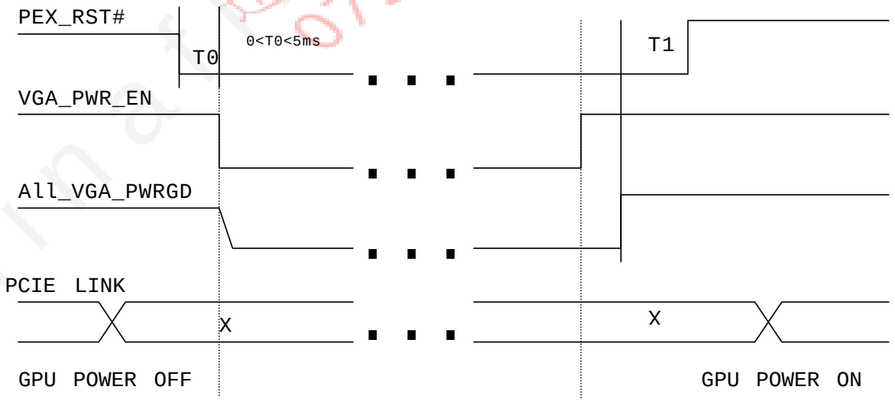
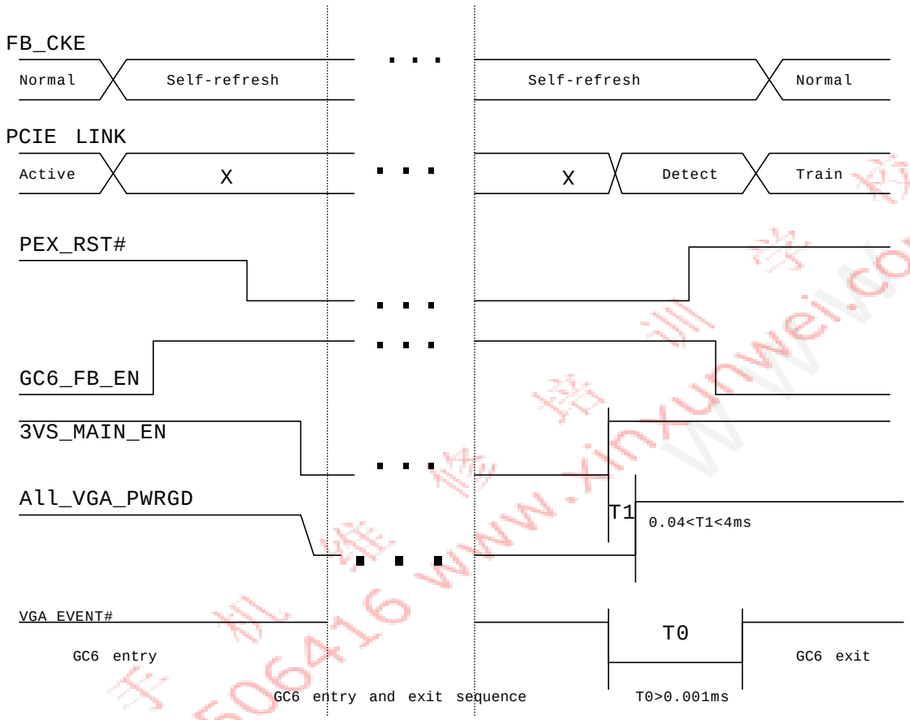
| GPIO | I/O | Functional Description | I/O Termination |
|---|---|---|---|
| GPIO0 | O | FB Enable for GC6 2.0, Open source | 10K pull-down |
| GPIO1 | O | Memory voltage control | Pull-up/pull down to set the FBVDD/Q boot voltage |
| GPIO2 | O | Panel Backlight PWM Brightness Control | 100K pull down |
| GPIO3 | O | Panel Power Enable | 100K pull down |
| GPIO4 | O | Panel Backlight Enable | 100K pull down |
| GPIO5 | O | GPU Power Sequence for GC6 2.0, Open Drain | 10k pull-up to 3V3_AON |
| GPIO6 | I | GPU wake signal for GC6 2.0 | 10k pull-up to 3V3_AON |
| GPIO7 | O | 3D Vision L/R signal | 100K pull down |
| GPIO8 | O | System side PCIe rest monitor | 10k pull-up to 3V3_AON |
| GPIO9 | I/O | Active low thermal alert, open drain | 10k pull-up to 3V3_AON |
| GPIO10 | O | Memory VREF Control | 100K pull down |
| GPIO11 | O | GPU Core VDD PWM control signal | |
| GPIO12 | I | AC power detect or power supply overdraw input | 100k pull-up to 3V3_AON |
| GPIO13 | O | Phase Shedding | 10K pull-up to 3V3_AON to enable two phase |
| GPIO14 | I | Hot Plug Detect for IFPA used as DisplayPort for IFPAB when used as Dual Link DVI | |
| GPIO15 | I | Hot Plug Detect for IFPC | |
| GPIO16 | I | Active Low Frame Lock, Open Drain | 10k pull-up to 3V3_AON |
| GPIO17 | I | Hot Plug Detect for IFPD | |
| GPIO18 | I | Hot Plug Detect for IFPE | |
| GPIO19 | I | Hot Plug Detect for IFPF or for IPFB when used as DisplayPort | |
| GPIO20 | O | Reserved | |
| GPIO21 | O | GPU PCIe self-reset control, Open Drain | 10k pull-up to 3V3_AON |
| OVERT | I/O | Catastrophic Over Temperature | 100k pull-up to 3V3_AON |




Optimus entry and exit sequence




GC6 entry and exit sequence

| | | | |
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Title: *P35-GPU GPIO table & sequence*

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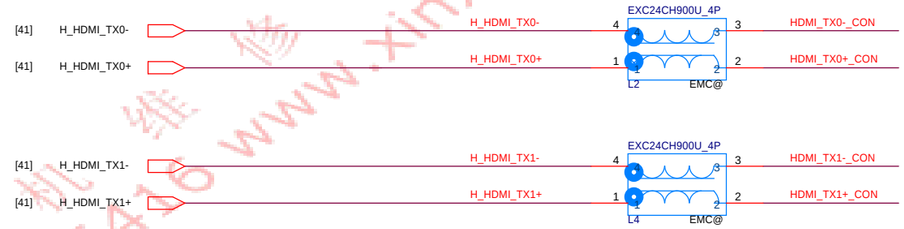


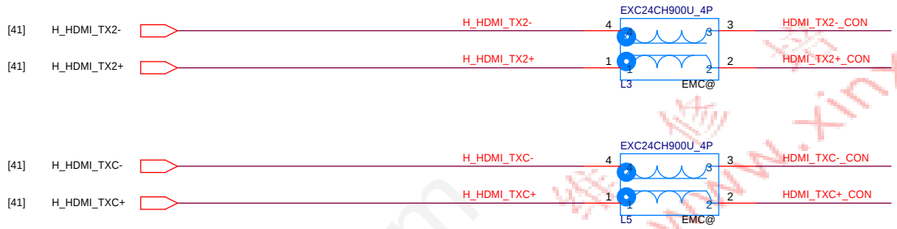


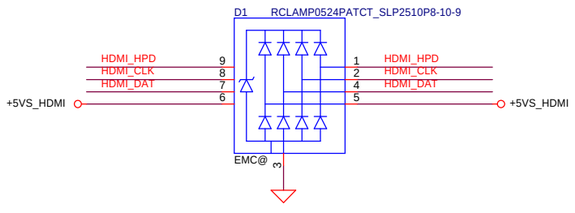


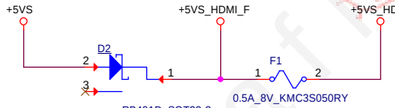


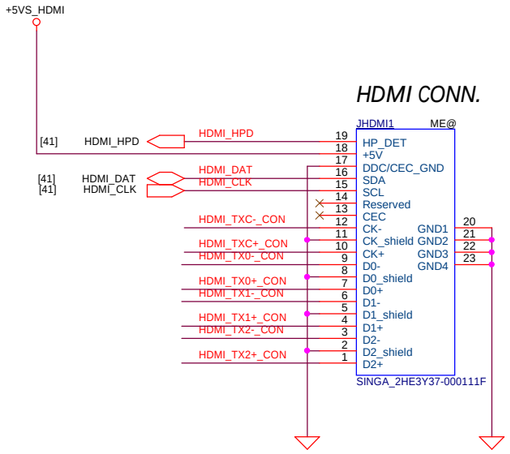


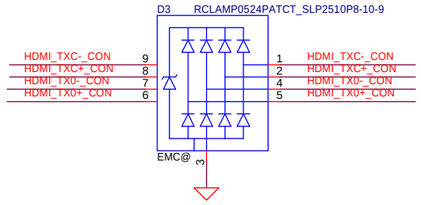


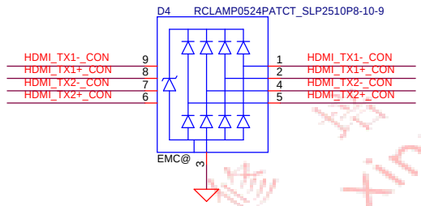


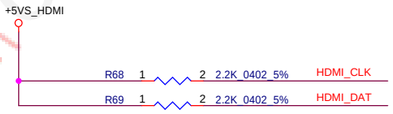


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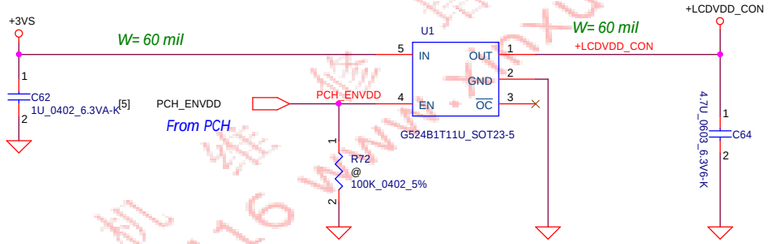
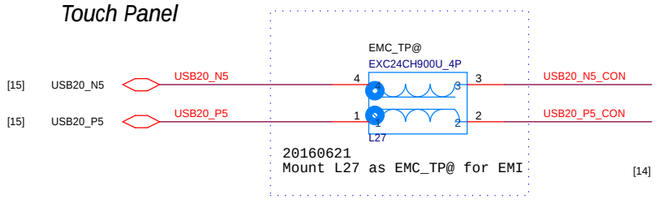
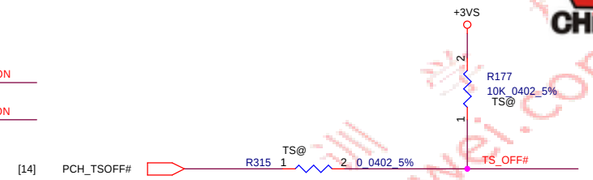
## LCDVDD Circuit

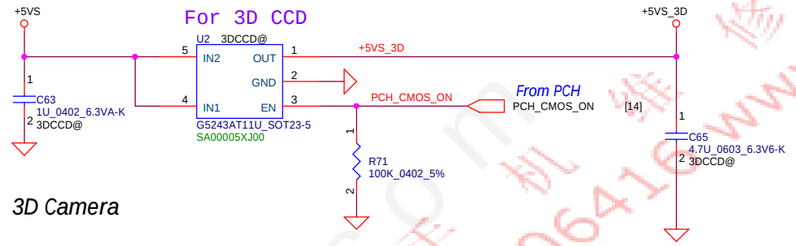



## Touch Panel



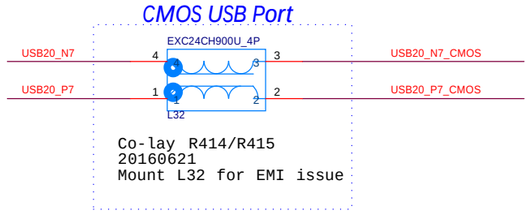



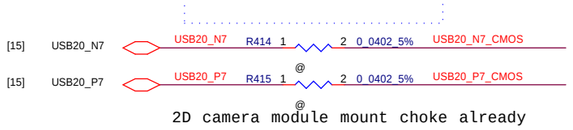

## 3D Camera



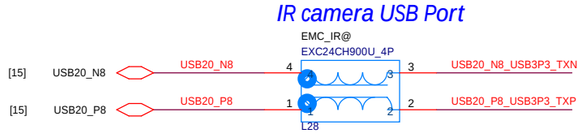

## CMOS Camera


## CMOS USB Port

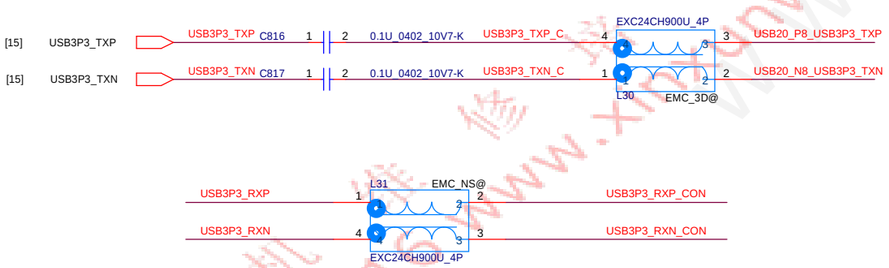


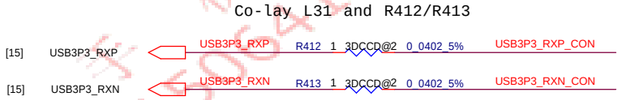



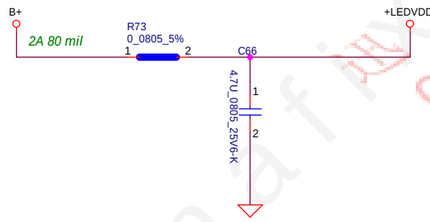

## IR camera USB Port

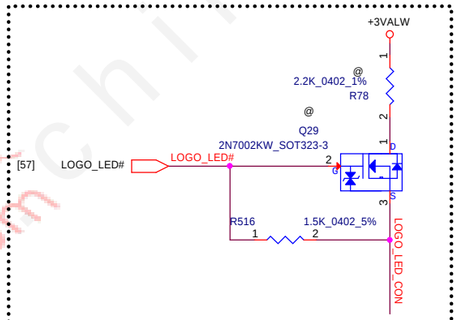



## 3D CCD USB Port

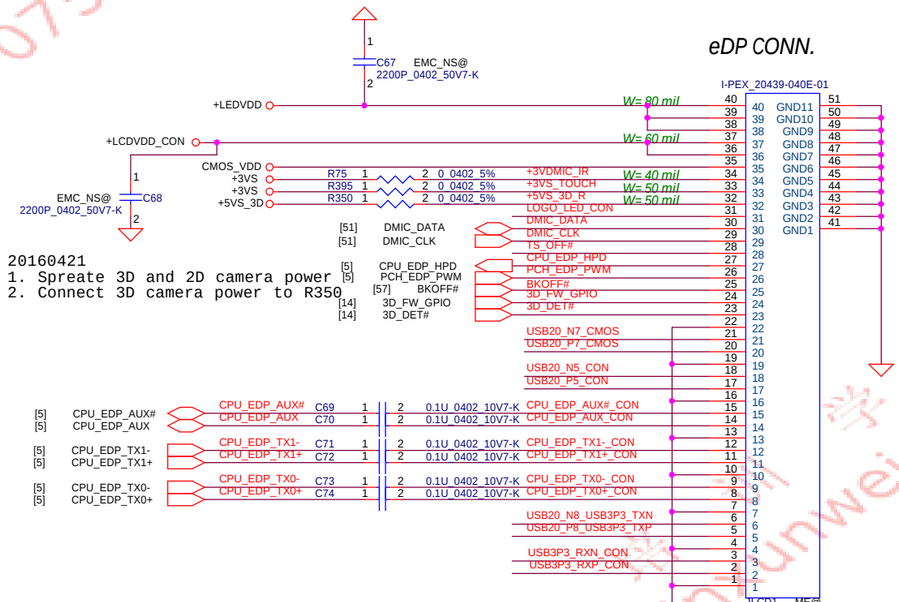


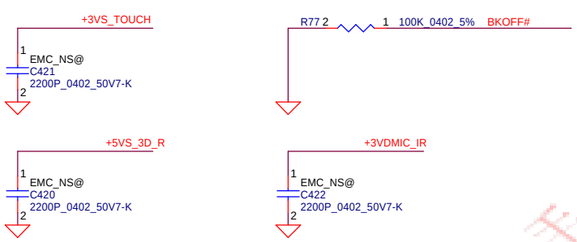



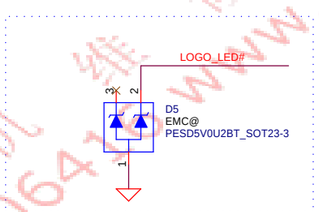




## eDP CONN.

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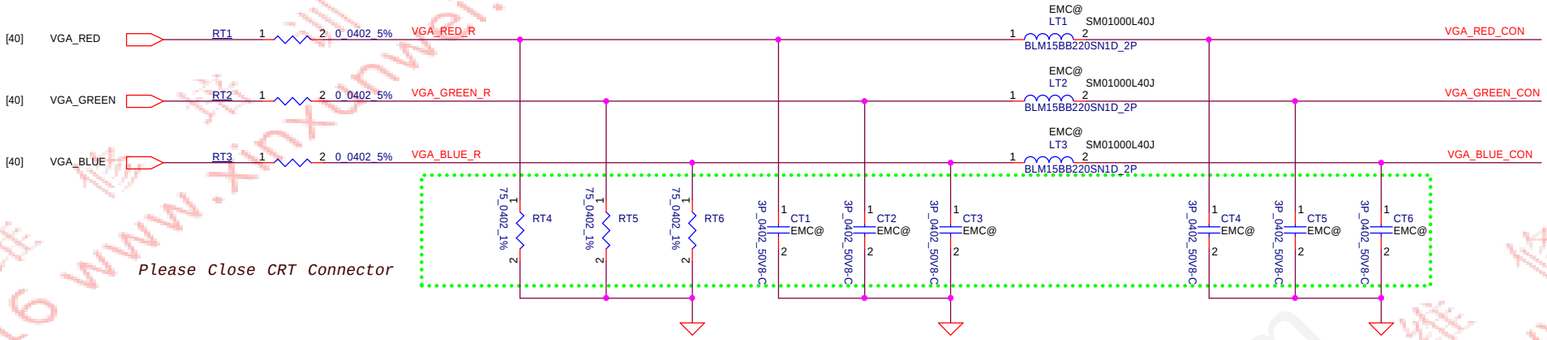
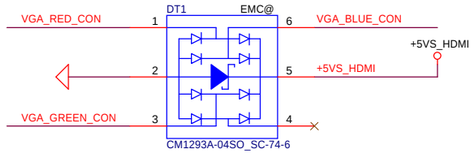
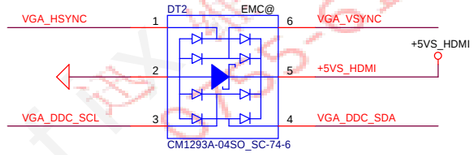
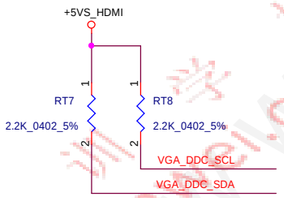


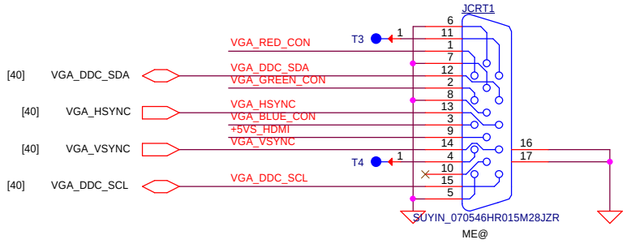




Only for 15'

## CRT Connector

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Title: **CRT CONN**

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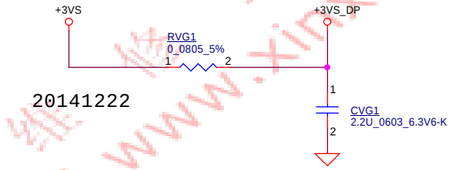
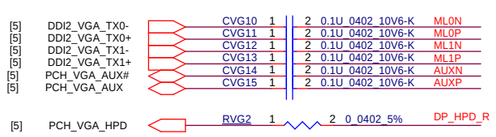
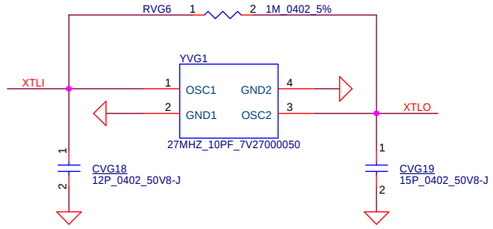
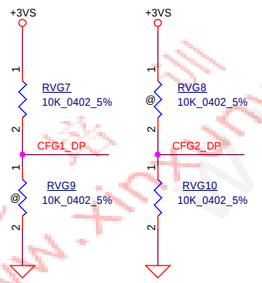



20160127
Change CVG19 to 15p by vender suggestion



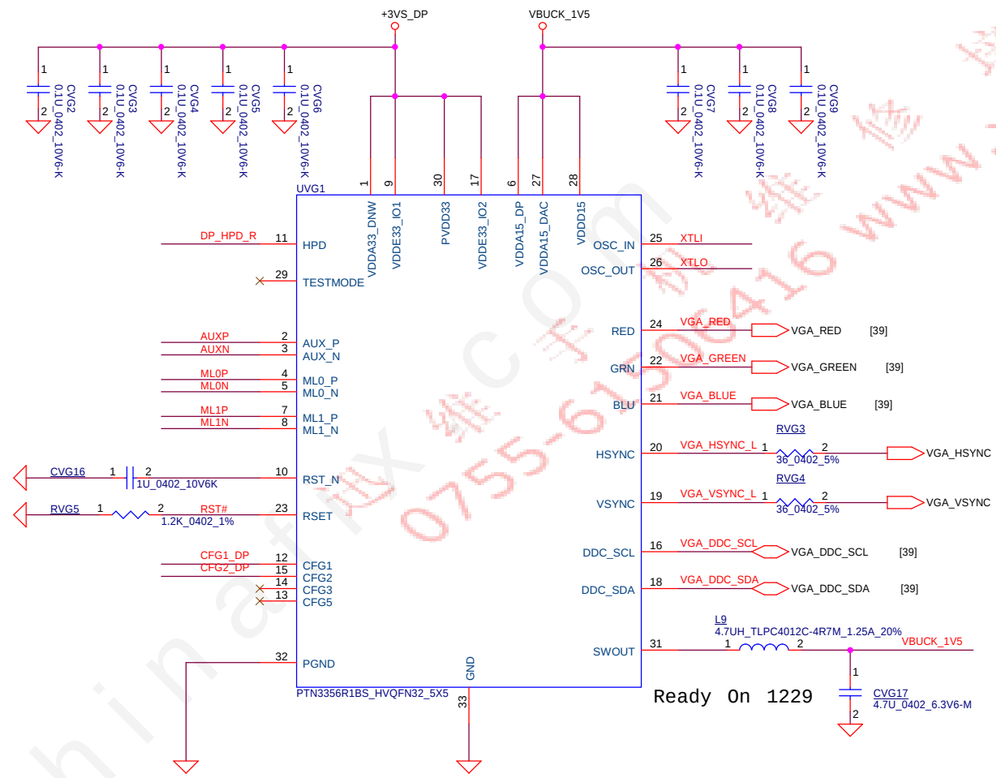




**Table 7. CFG1/CFG2 pin definitions**

| Pin value | System behavior |
|---|---|
| 00 | Compliant HPD behavior |
| 01 | Most interoperable (non-compliant) HPD behavior |
| 10 | Most interoperable (non-compliant) HPD behavior |
| 11 | (Default) Compliant behavior |

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Title: *DP to VGA*

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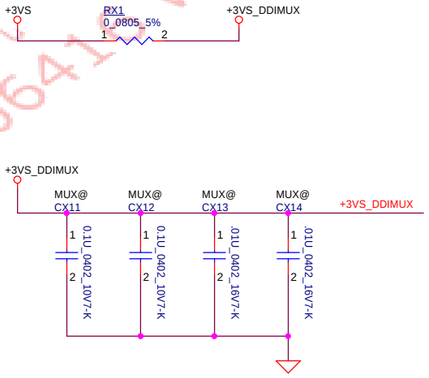


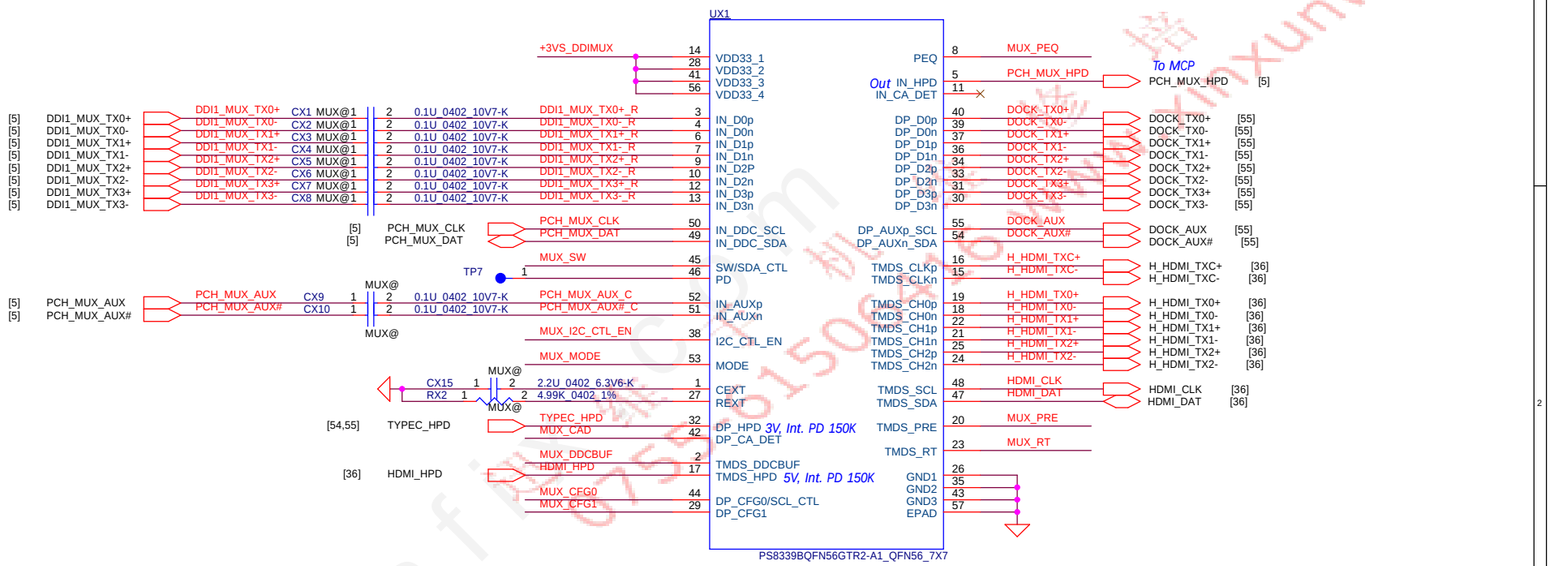


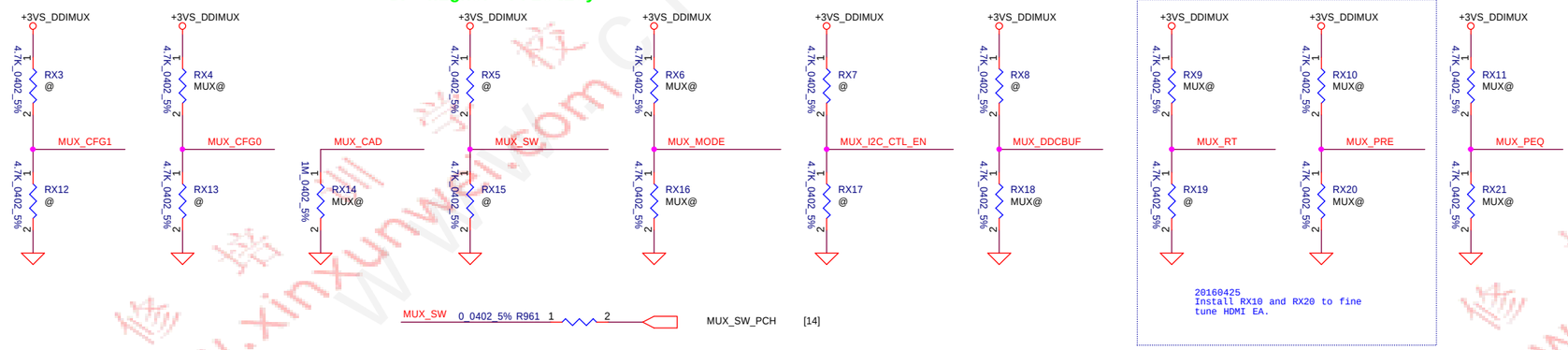


20160419
1. Connect MUX_SW to PCH, display priolity control by BIOS
2. Add R961 0 ohm and unstaff RX15.

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Title: **Mux IC**

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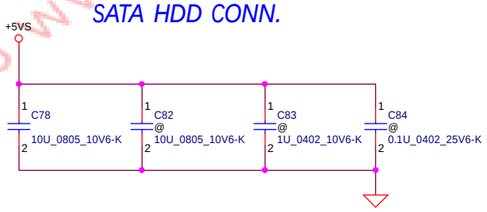
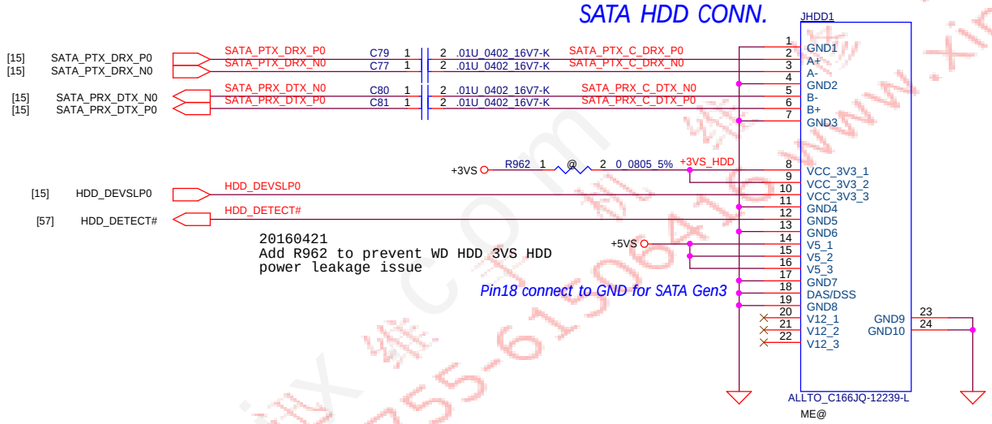
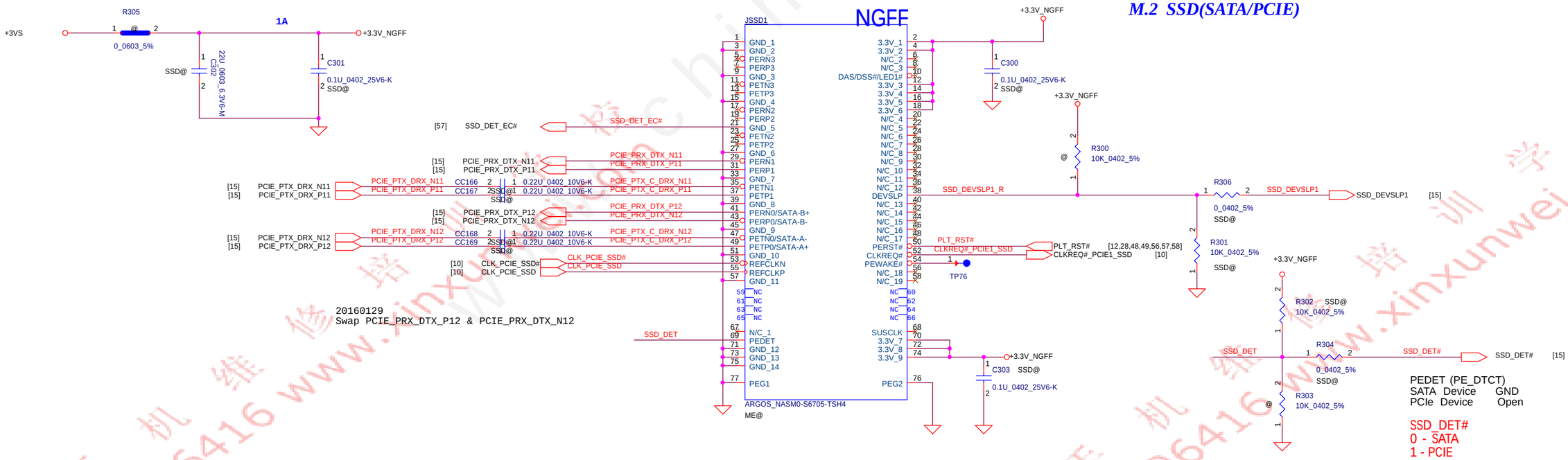
## SATA HDD CONN.




## SATA HDD CONN.




## M.2 SSD(SATA/PCIE)




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **SATA HDD**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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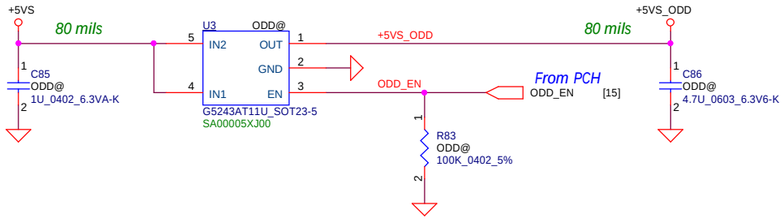
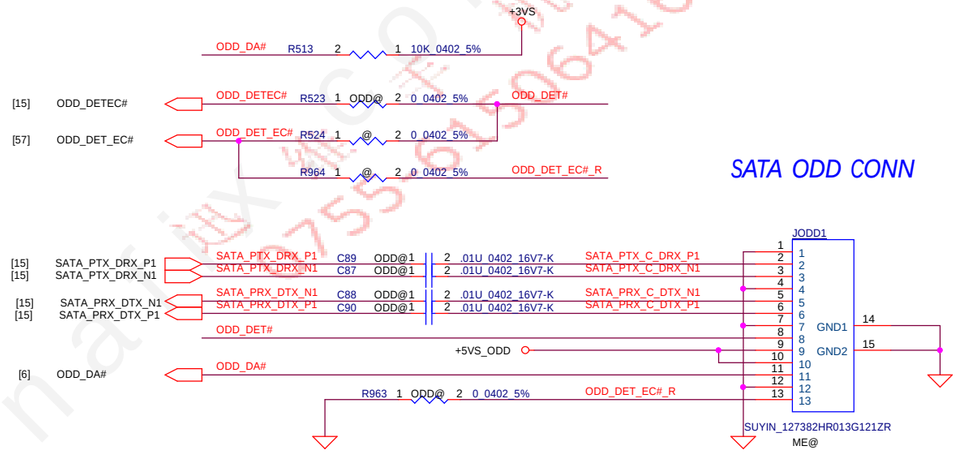
## +5VS TO +5VS_ODD




20160421
Add R963 and reserve R964 for tember function

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: ODD

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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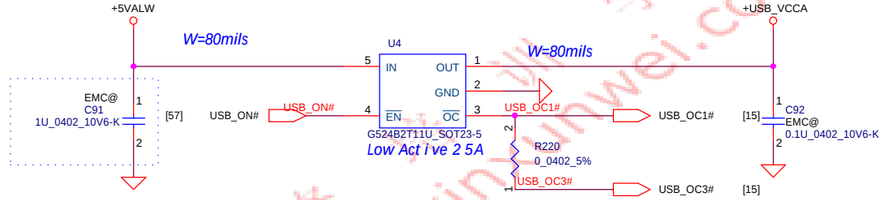
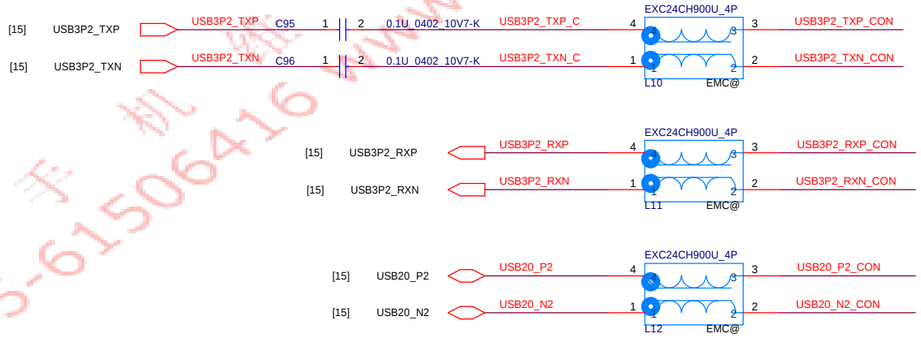
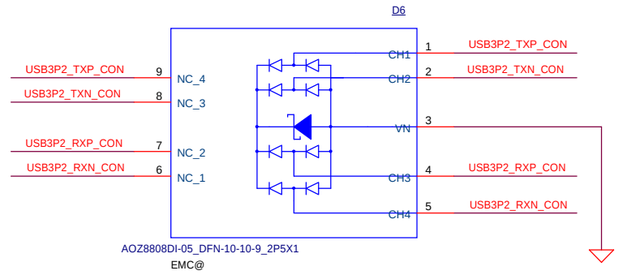
# USB3 PORT2

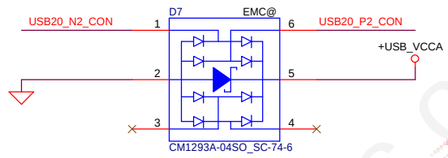
## POWER SWITCH

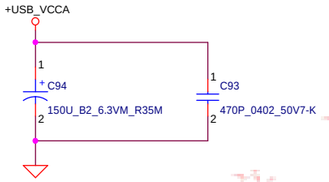


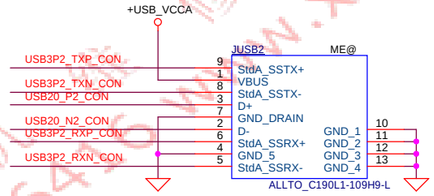

20160616
Change C91 for 0.1U_0402_10V6-K to 1U_0402_10V6-K EMC@



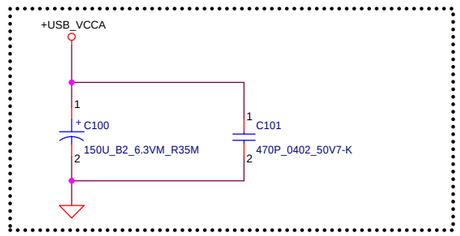



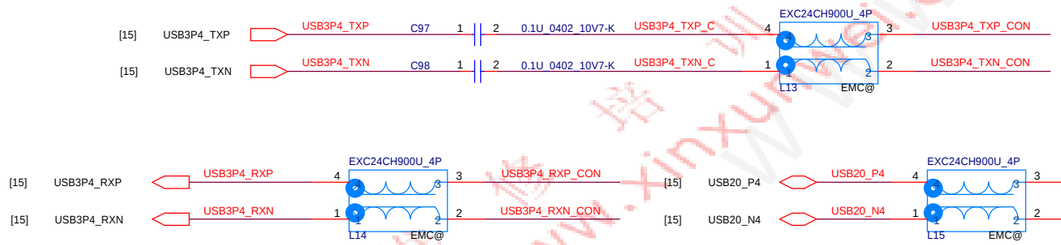

# PORT4

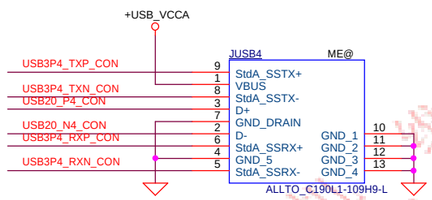









| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **USB3 PORT1/PORT2(AOU)**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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# BLANK



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|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: BLANK

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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# BLANK



| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **GBE LAN PHY**

| Size | Document Number | Rev |
|---|---|---|
| Custom | **SKYWALKER** | 2.0 |

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# BLANK



| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |

Title: *RJ45 CONN*

Size: Custom | Document Number: **SKYWALKER** | Rev: 2.0

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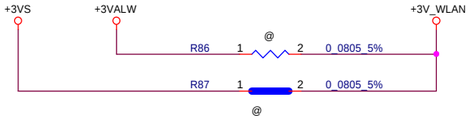
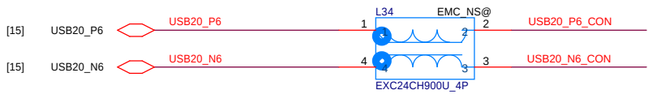
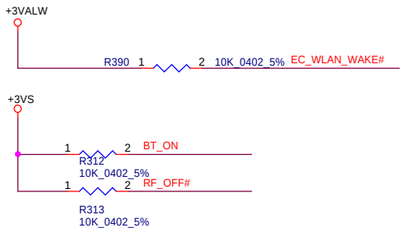
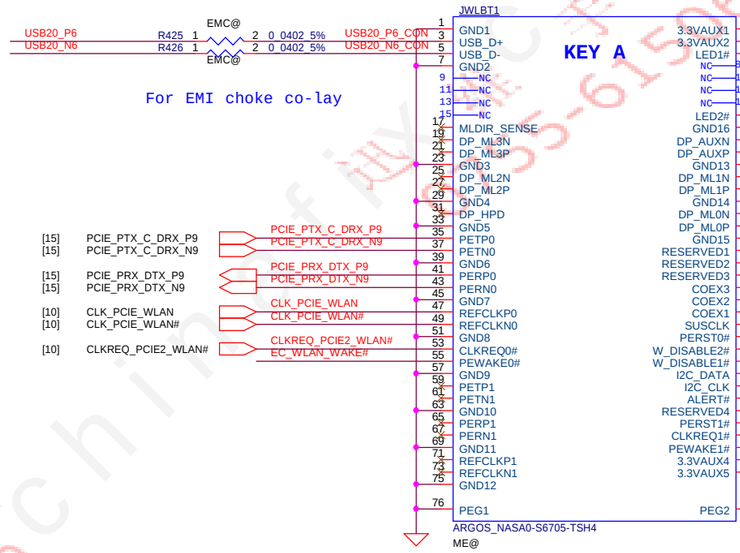
# TYPE-A NGFF SLOT FOR WLAN
# 3.2H CONNECTOR




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: *WWAN/WLAN NGFF CONN.*

| Size | Document Number | Rev |
|---|---|---|
| Custom | *SKYWALKER* | 2.0 |

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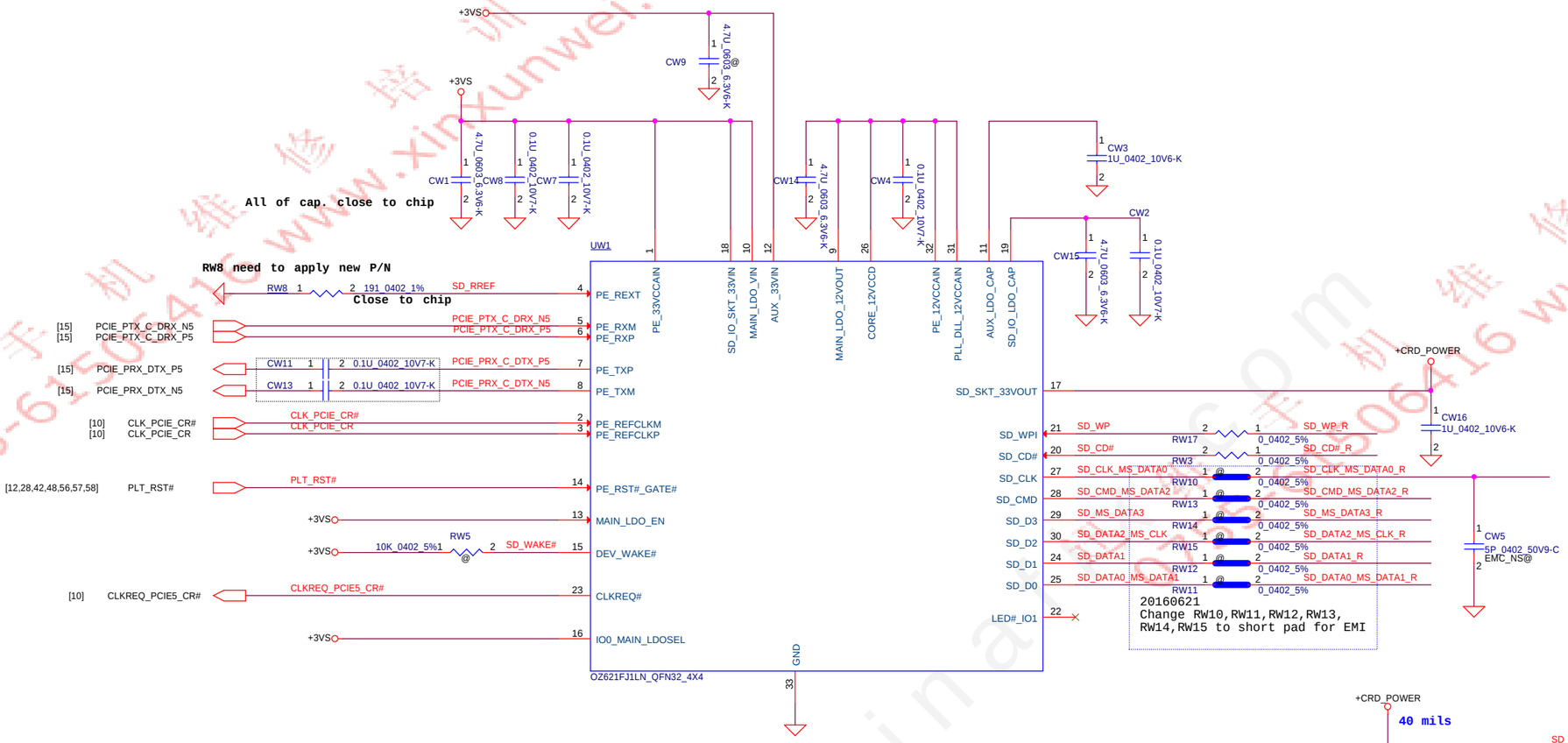


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Title: **Card Reader**

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|---|---|---|
| Custom | SKYWALKER | 2.0 |

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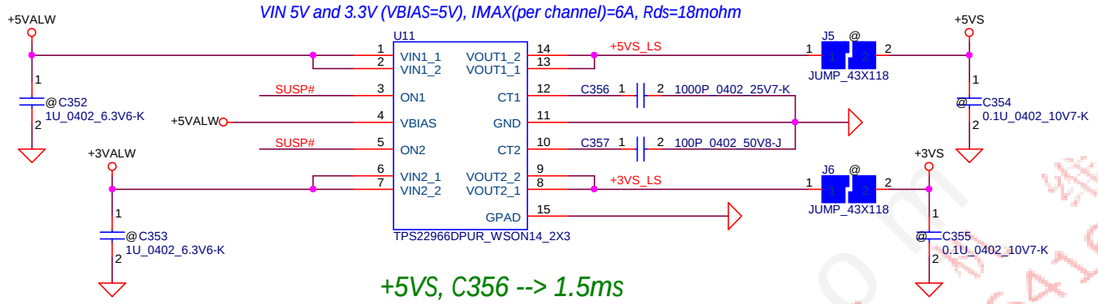
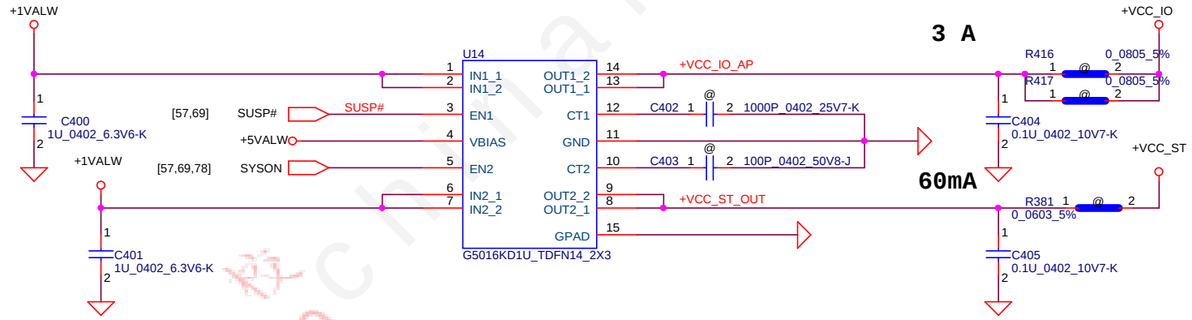
*Load Switch*
*+5VALW To +5VS*
*+3VALW To +3VS*

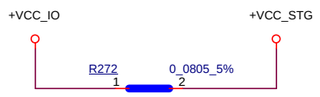



*+5VS, C356 --> 1.5ms*
*+3VS, C357 --> 2.5ms*

*+1VALW to +VCC_IO_AP & +VCC_ST*

Unstaff C402 and C403 for the fastest sequence.




Slew Rate=10uS<TR<65us

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: *DC V TO VS/ V-PCH/VM*

| Size | Document Number | Rev |
|---|---|---|
| Custom | *SKYWALKER* | 2.0 |

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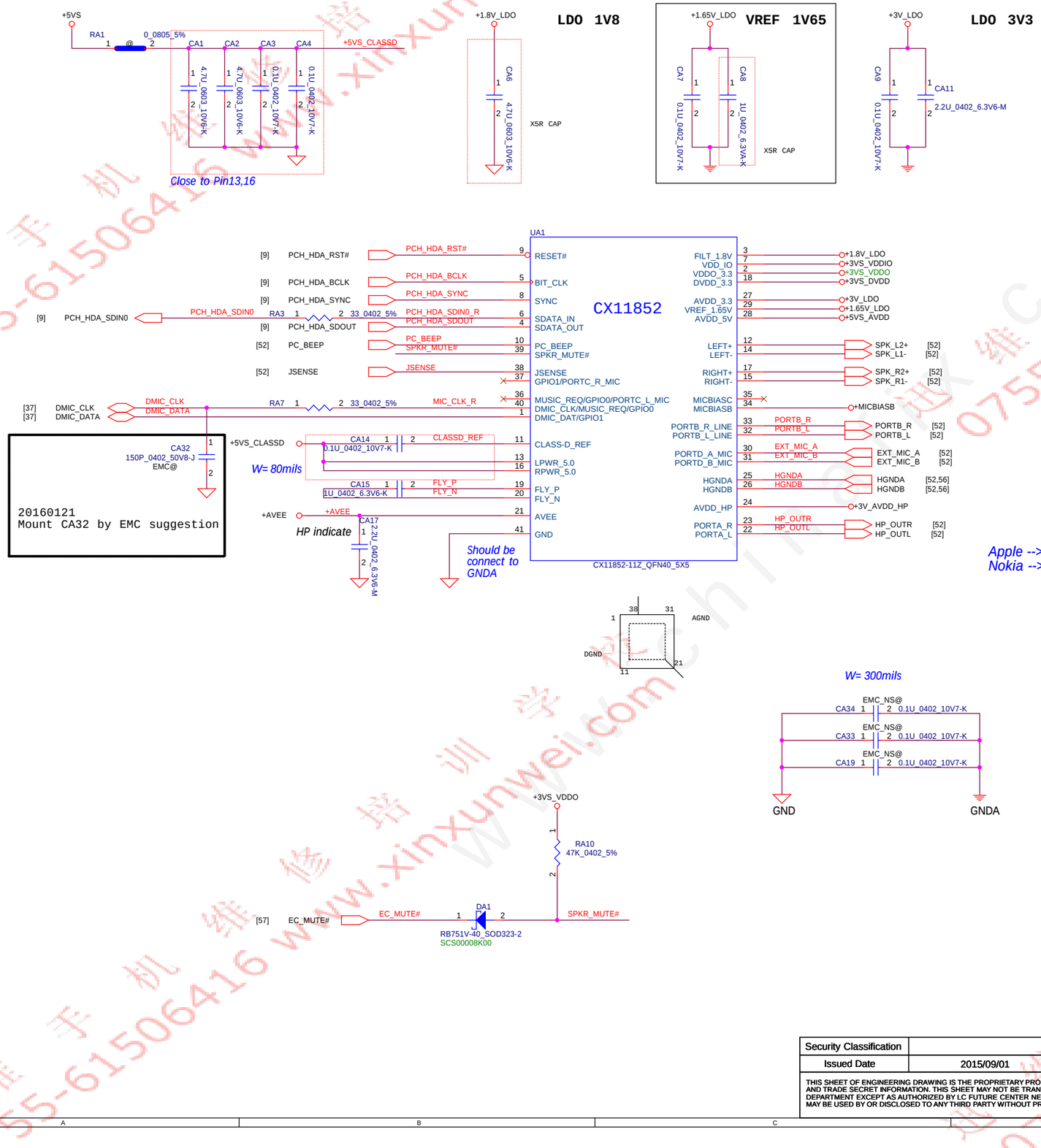


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Title: **Audio Codec**

Size: Custom | Document Number: **SKYWALKER** | Rev: 2.0

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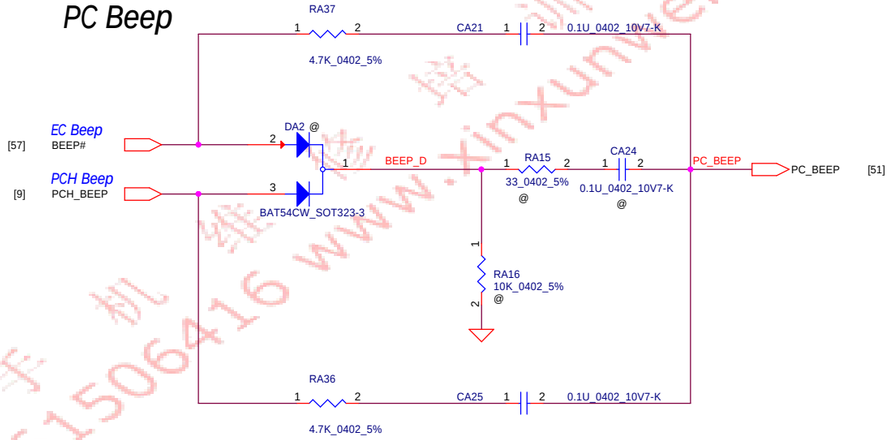
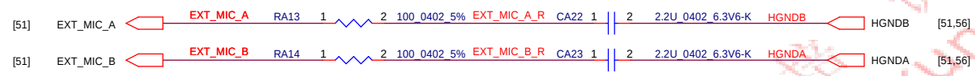
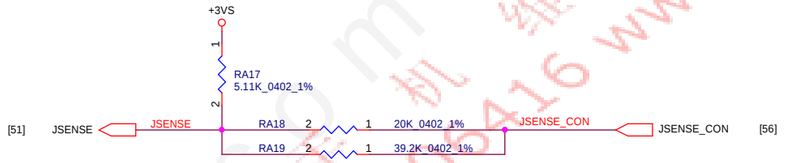
## PC Beep



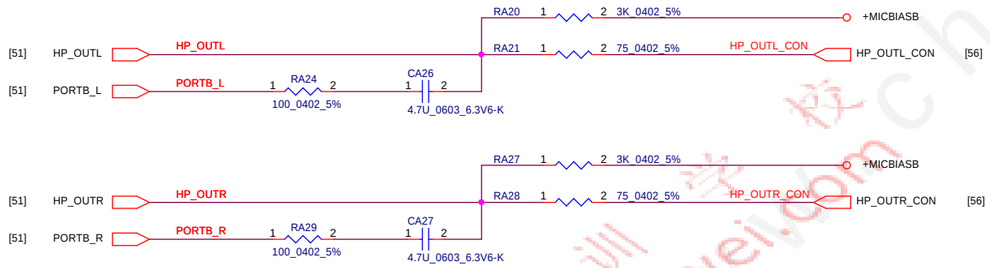

## EXT. MIC/LINE IN

*Apple --> EXT_MIC_A, HGNDB*
*Nokia --> EXT_MIC_B, HGNDA*



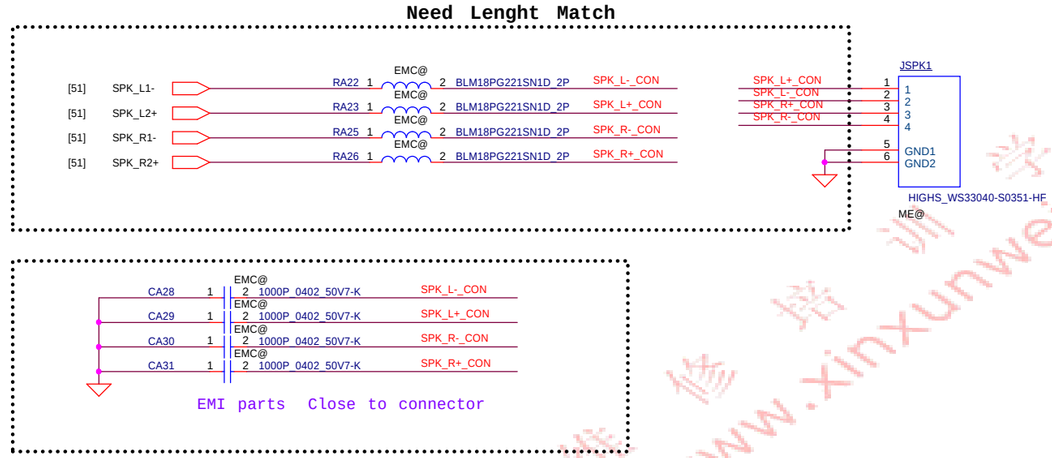

## HeadPhone/LINE OUT




## Speaker OUT

## SPK CONN.

**Need Lenght Match**




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **HP/MIC JACK/Speaker**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |
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|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
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Title: BLANK

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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+3VPD
+3VPD_VDD
+3VPD_VDDIO
TYPEC@
R98 1 2 0_0402_5%
R99 1 2 0_0402_5%
20160624
Change R99 Pin1 to +3VPD_VDD

USBC1_CC1_CONN
USBC1_CC2_CONN
TYPEC@ C108 330P_0402_50V8-J
TYPEC@ C109 330P_0402_50V8-J
20160426
1.Change C108,C109 to 150P
by vender suggestion
20160505
Change C108,109 to 390P
due to U20 material shortage

+3VPD_VDD
R110 @ 4.7K_0402_5%
PD_XRES
C110 TYPEC@ 0.1U_0402_16V7-K

+3VPD_VDD
C103 TYPEC@ 0.1U_0402_16V7-K
C104 TYPEC@ 1U_0402_10V6-K
C105 TYPEC@ 10U_0603_6.3V6-M

+3VPD_VDDIO
C902 TYPEC@ 0.1U_0402_16V7-K
C903 TYPEC@ 1U_0402_10V6-K

+3VPD_VDDIO
CCG2_I2C_CLK_PD R400 1 TYPEC@2 10K_0402_5%
CCG2_I2C_DATA_PD R399 1 TYPEC@2 10K_0402_5%
20160624
Change pull up from +3VPD to +3VALW
20160627
Change pull up from +3VALW to +3VPD_VDDIO

+3VALW
2.2K_0402_5% R393 EC_SMB_CK2
2.2K_0402_5% R394 EC_SMB_DA2
+3VALW
2.2K_0402_5% R370 INT#_TYPEC
10K_0402_1% R371 TYPEC_HPD
20160414
1.Change pull up from +3VPD to +3VALW
by vender suggestion.

20160615
Add VBUS_C_CTRL0 due to Type-C
Add R961 0_0402_5%

VCCPD_VBUS
+3VALW
+3VPD_VDDIO
+5VALW
TC32
U5
VBUS 31
VSYS 20
VDDD 18
VBUS_P 40

[55] CCG2_I2C_CLK_PD R215 1 TYPEC@2 0_0402_5% CCG2_I2C_CLK_PD_R 9
[55] CCG2_I2C_DATA_PD R216 1 TYPEC@2 0_0402_5% CCG2_I2C_DATA_PD_R 10
[55] USBC1_CC1_CONN R108 1 TYPEC@2 0_0402_5% USBC1_CC1 5
[55] USBC1_CC2_CONN R109 1 TYPEC@2 0_0402_5% USBC1_CC2 3
+5VALW 4
[65] VBUS_C_CTRL0 R965 1 TYPEC@2 0_0402_5% VBUS_C_CTRL0_R 30
PD_VBUS_DISCHG 32
29
[41,55] TYPEC_HPD TP17 R105 1 TYPEC@2 0_0201_5% TYPEC_HPD_PD 6
VSEL1 35
[65] PD_VBUS_C_CTRL1 PD_VBUS_C_CTRL1 28
27
[57] EC_SMB_DA2 R214 1 TYPEC@2 0_0201_5% EC_SMB_DA2_R 36
[57] EC_SMB_CK2 R213 1 TYPEC@2 0_0201_5% EC_SMB_CK2_R 37
[57] INT#_TYPEC R101 1 TYPEC@2 0_0201_5% INT#_TYPEC_R 34
[55] 3V_TPD8S300_FLT# R972 1 TYPEC@2 0_0402_5% OS_SENSE# 38
VBUS_OVP_ACOK# R973 1 TYPEC@2 0_0402_5%

[55] USB_OE# USB_OE# 25
[55] USB_SEL USB_SEL 24
[55] USBC_DPAUX1_MUX R889 1 @ 2 0_0402_5% USBC_DPAUX1_PD 11
[55] USBC_DPAUX2_MUX R890 1 @ 2 0_0402_5% USBC_DPAUX2_PD 14
[55] USBC_DPAUX1 R891 1 @ 2 0_0402_5% USBC_SBU1 12
[55] USBC_DPAUX2 R892 1 @ 2 0_0402_5% USBC_SBU2 13
TC34 1 PD_XRES 26
XRES

GPIO/UART_0_RX/UART_3_CTS/SPI_3_MOSI/I2C_3_SCL/HPD
GPIO/UART_0_TX/UART_3_RTS/SPI_3_CLK/I2C_3_SDA
CC1
CC2
VSY
VBUS_DISCHARGE
VBUS_C_CTRL0
VBUS_C_CTRL1
VCONN
GPIO/P3.3
I2C_0_SCL/GPIO_OVT/UART_0_RTS/SPI_0_MISO
I2C_0_SDA/GPIO_OVT/UART_0_CTS/SPI_0_SEL
GPIO/UART_2_CTS/SPI_2_MOSI/I2C_2_SDA
GPIO/UART_2_RTS/SPI_2_CLK/I2C_2_SCL
GPIO/P3.2
GPIO/P3.6
GPIO/P2.4
GPIO/UART_1_CTS/SPI_1_CLK/I2C_1_SCL/SWD_0_DAT/P2.0
GPIO/UART_1_RTS/SPI_1_MOSI/I2C_1_SDA/SWD_0_CLK/P2.1
GPIO/UART_2_TX/SPI_2_MISO
GPIO/UART_2_RX/SPI_2_SEL
GPIO/UART_0_RX/SPI_0_CLK
GPIO/UART_0_TX/SPI_0_MOSI
AUX_P_signal/GPIO/UART_1_TX/SPI_1_MISO
AUX_N_signal/GPIO/UART_1_RX/SPI_1_SEL
SBU1_signal/GPIO/UART_3_TX/SPI_3_MISO/SWD_1_CLK
SBU2_signal/GPIO/UART_3_RX/SPI_3_SEL/SWD_1_DAT
DMINUS
DPLUS
GND
EPAD
TYPEC@
CYPD3125-40LQXIT_QFN40_6X6

VCCD 19
VCCD
USB_P_PWR_SENSE 39
OC
+3VPD_VDD
VDDD 17
20160414
1.Change net name from +3VPD_VDDIO
to +3VPD_VDD
TYPEC@ C900 0.1U_0402_16V7-K
TYPEC@ C901 1U_0402_10V6-K

PD_VBUS_P_CTRL1 1
PD_VBUS_P_CTRL0 2
VBUS_P_CTRL1
VBUS_P_CTRL0
PD_MUX_EN 23
PD_SWD_IO 15
PD_SWD_CLK 16
TC23 1
TC24 1
7
8
TC33 33 1
41

+5VALW
+3VALW
TYPEC@ R521 0_0805_5%
+3V_MUX
@ R969 47K_0402_5%
Q31 AO3413_SOT23-3
@ R971 10K_0402_5%
PD_MUX_EN#
@ Q30 2N7002KW_SOT323-3
@ R970 100K_0402_5%
@ C961 0.1U_0402_16V7-K
20160616
Add soft stop

VBUS_P_CTRL = 1 (Consumer Path ON)
VBUS_P_CTRL = 0/Z (Consumer Path OFF)
FROM SYSTEM

VCCPD_VBUS
TYPEC@ C180 1U_0402_25V6-K
R156 100_0805_5% TYPEC@
R896 100_0805_5% @
PD_VBUS_DISCHG
Discharge Circuit
20160309
1. Reserve R896 for discharge circuit.

TYPEC@ Q27 AON7380
TYPEC@ Q28 AON7380
VCCSM_Q_VBUS
USB_P_PWR_SENSE
TYPEC@ 0.01_1206_1%
R533
+5VALW
TYPEC@ C181 1U_0402_25V6-K
C460 @
C461 470P_0402_50V7-K
150U_B2_6.3VM_R35M

PD_VBUS_P_CTRL1
R974 10K_0201_5%
TYPEC@
C8622 TYPEC@ 0.1U_0201_25V6-K
R537 10M_0201_5% TYPEC@
R536 10M_0201_5% TYPEC@
C8623 TYPEC@ 0.1U_0201_25V6-K
R975 10K_0201_5% TYPEC@
PD_VBUS_P_CTRL0
20160624
Type-C solution for inrush current
Change R536/R537 to 10M_0201_5% TYPEC@ for layout place
Change R974/R975 to 100K_0201_5% TYPEC@ for layout place
Change C8622/C8623 to 0.0.1U_0201_25V6-K TYPEC@ for layout place
20160627
Change R974/R975 to 10K_0201_5% TYPEC@

VCCPD_VBUS_CONN
20160824
Due to EMI fail with Acbel typeC adapter
EMI suggest add -filter
PL5 EMC_NS@ BLM18KG300TN1D_2P
PL6 EMC_NS@ BLM18KG300TN1D_2P
EMC_NS@ C200 1000P_0402_50V7-K
EMC_NS@ C201 100P_0402_50V8J
EMC_NS@ C202 100P_0402_50V8J
EMC_NS@ C203 1000P_0402_50V7-K
TYPEC@ C502 0.1U_0603_50V7-K
TYPEC@ R508 1 2 1M_0201_5%
TYPEC@ R902 51.1K_0201_1%
U30
B3 IN1
C2 IN2
C3 IN3
EN# A1
OVLO C1
OUT1 A2
OUT2 A3
OUT3 B2
ACOK# B1
GND_1 A4
GND_2 B3
GND_3
FPF2281BUCX-F130_WLCSP12
TYPEC@
20160624
Change F10 connect to VCCPD_VBUS
VCCPD_VBUS_F
F10 5A_35V_T0603FF5000TM
TYPEC@
VCCPD_VBUS
TYPEC@ C960 1U_0603_25V6-K
20160616
Change +3VAWL to +3V_MUX
+3V_MUX
TYPEC@ R960 10K_0201_5%
VBUS_OVP_ACOK#

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |

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Title: TYPE-C_Controller
Size: Custom | Document Number: KENOBI | Rev: 2.0
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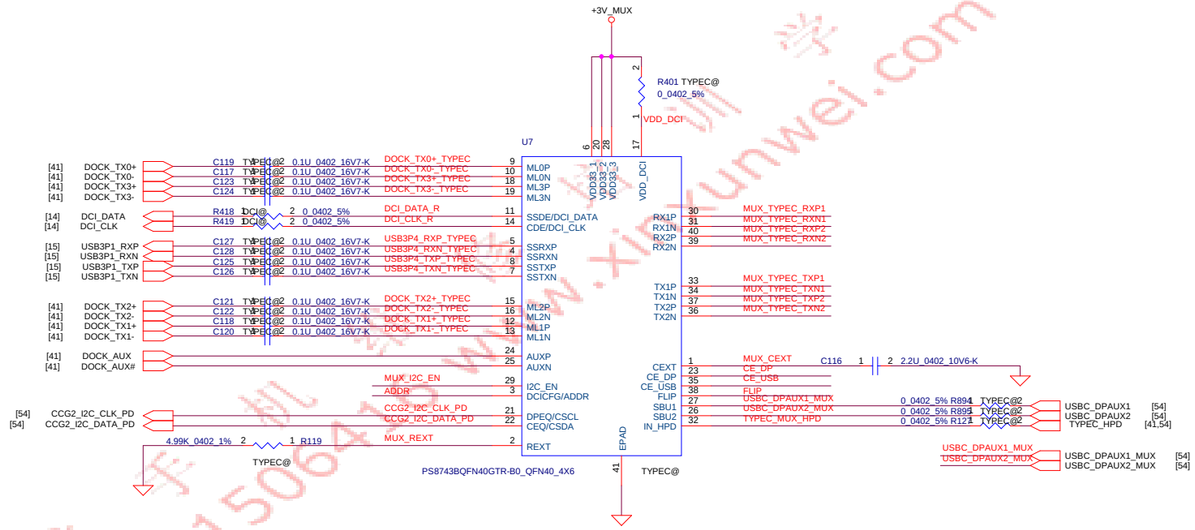


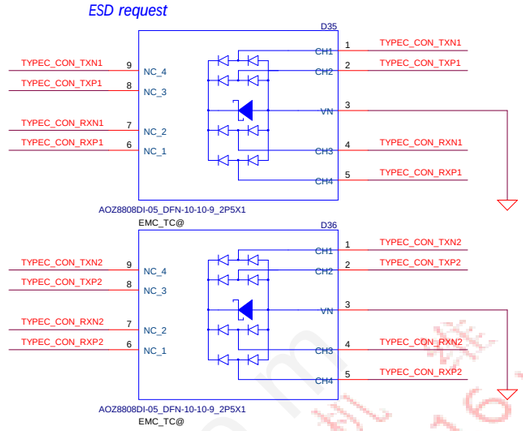


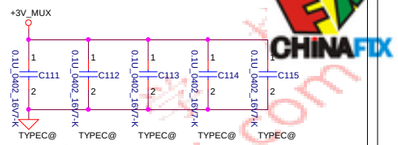


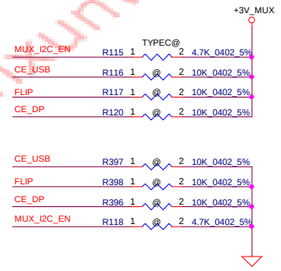


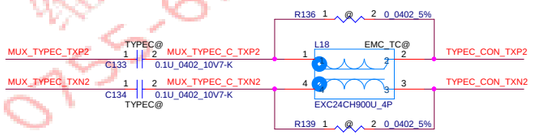


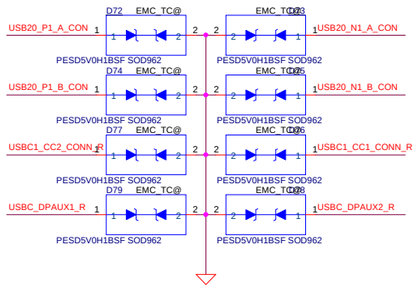


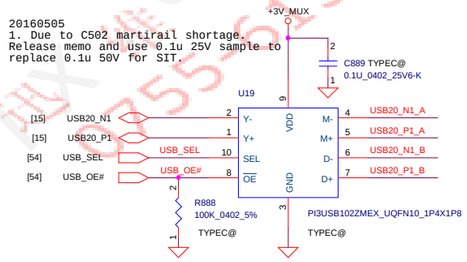


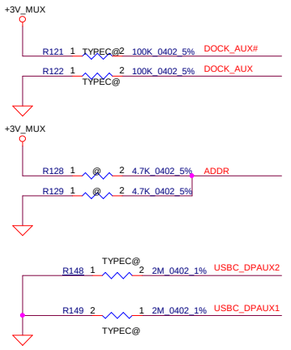


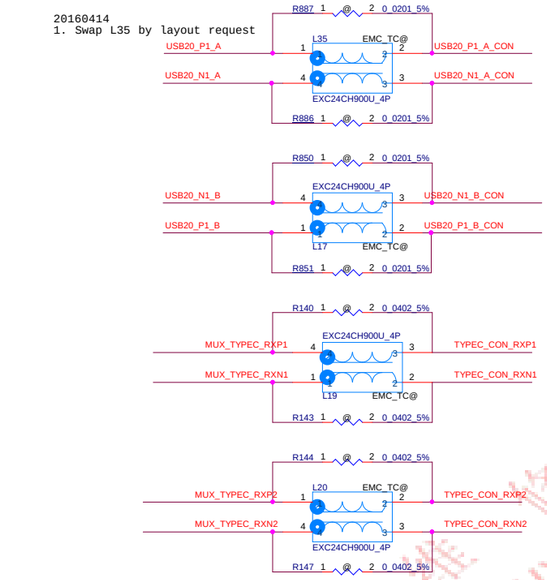


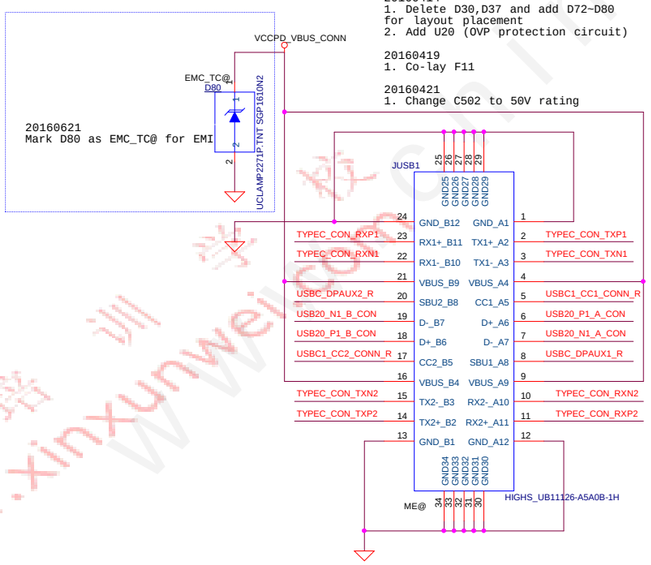


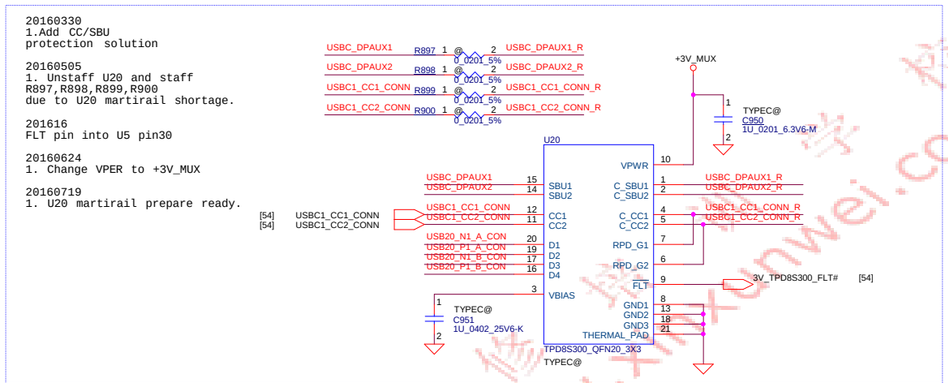


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Title: TYPE-C_MUX

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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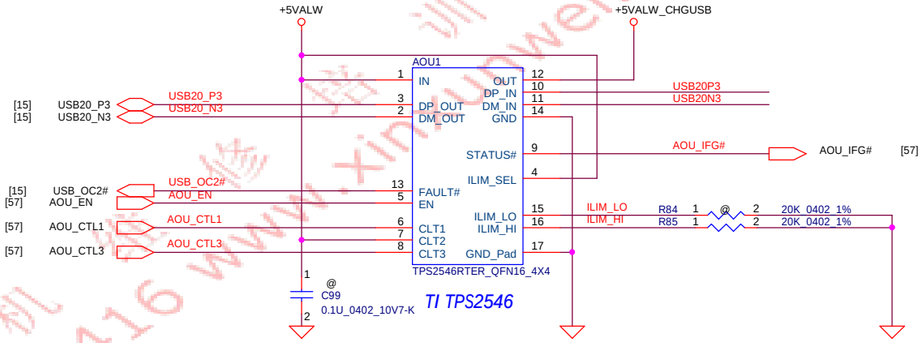
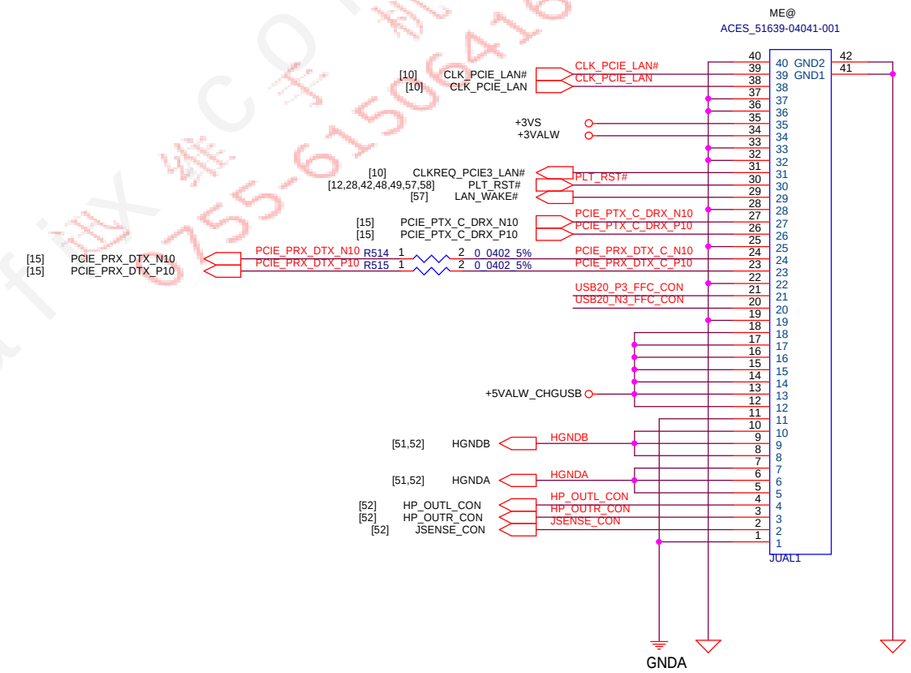



| | CLT1 | CLT2 | CLT3 | ILIM_SEL | MOD | |
|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | X | **DCH** | OUT held low |
| * | 1 | 1 | 1 | 1 | **CDP** | Data Connected and Port Power Mgt. Function Active |
| * | 1 | 1 | 1 | 0 | **SDP2** | Data Connected |
| * | 1 | 1 | 0 | X | **SDP1** | Data Connected |
| * | 0 | 1 | 0 | X | **SDP1** | Data Connected |
| | 1 | 0 | 0 | X | **DCP_Short** | Device Forced to stay in DCP BC 1.2 charging mode |
| | 1 | 0 | 1 | X | **DCP_Divider** | Device Forced to stay in DCP Divider 1 Charging Mode |
| * | 0 | 1 | 1 | X | **DCP_Auto** | Data Disconnected and Port Power Mgt. Function Active |
| | 0 | 0 | 1 | X | **DCP_Auto** | Data Disconnected and Power Wake Function Active |




1. AC Capacitor place on Sub/B

| | | | |
|---|---|---|---|
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| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **DOCKING/ DCIN CONN**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |
| Date: Thursday, August 25, 2016 | Sheet 56 of 82 | |

| Vcc | 3.3V +/- 5% |
|---|---|
| RE1 | 100K +/- 1% |

| Board ID | RE2 | $V_{AD\_BID}$ min | $V_{AD\_BID}$ typ | $V_{AD\_BID}$ max | Phase |
|---|---|---|---|---|---|
| 0 | 0K +/- 5% | 0 V | 0 V | 0 V | SDV |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | FVT |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | SIT |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | SVT |
| 4 | 4.7K +/- 5% | 0.141 V | 0.148 V | 0.155 V | |
| 5 | 24K +/- 5% | 0.612 V | 0.638 V | 0.664 V | |

20160127
Add TEMBER_DETECT# circuit

20160419
Change RE2 to 18K
for SIT board ID

20160307
Stuff CE11 for WRST singal

All capacitors close to EC

Close to EC

minimum trace width 12 mil

IT8586E/AX
LQFP-128L

Un-stuff if not necessary.

1. Version CX : Don't Support Mirror Code
Version DX/EX/FX : Support Mirror Code
2. For Mirror Code
"H" --> Enable
"L" --> Disable (Default)
*

Please don't place any PU Resistor on GPG[7:2]
(Reserve hardware strapping)

IT8586E-AX_LQFP128_14X14
SA00005W940

IT8586E/FX LQFP

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Title: EC

Size: A2 | Document Number: SKYWALKER | Rev: 2.0

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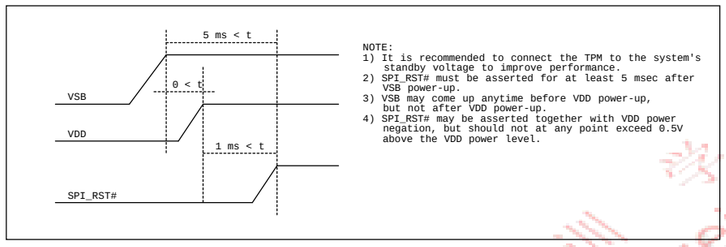
# TPM IC

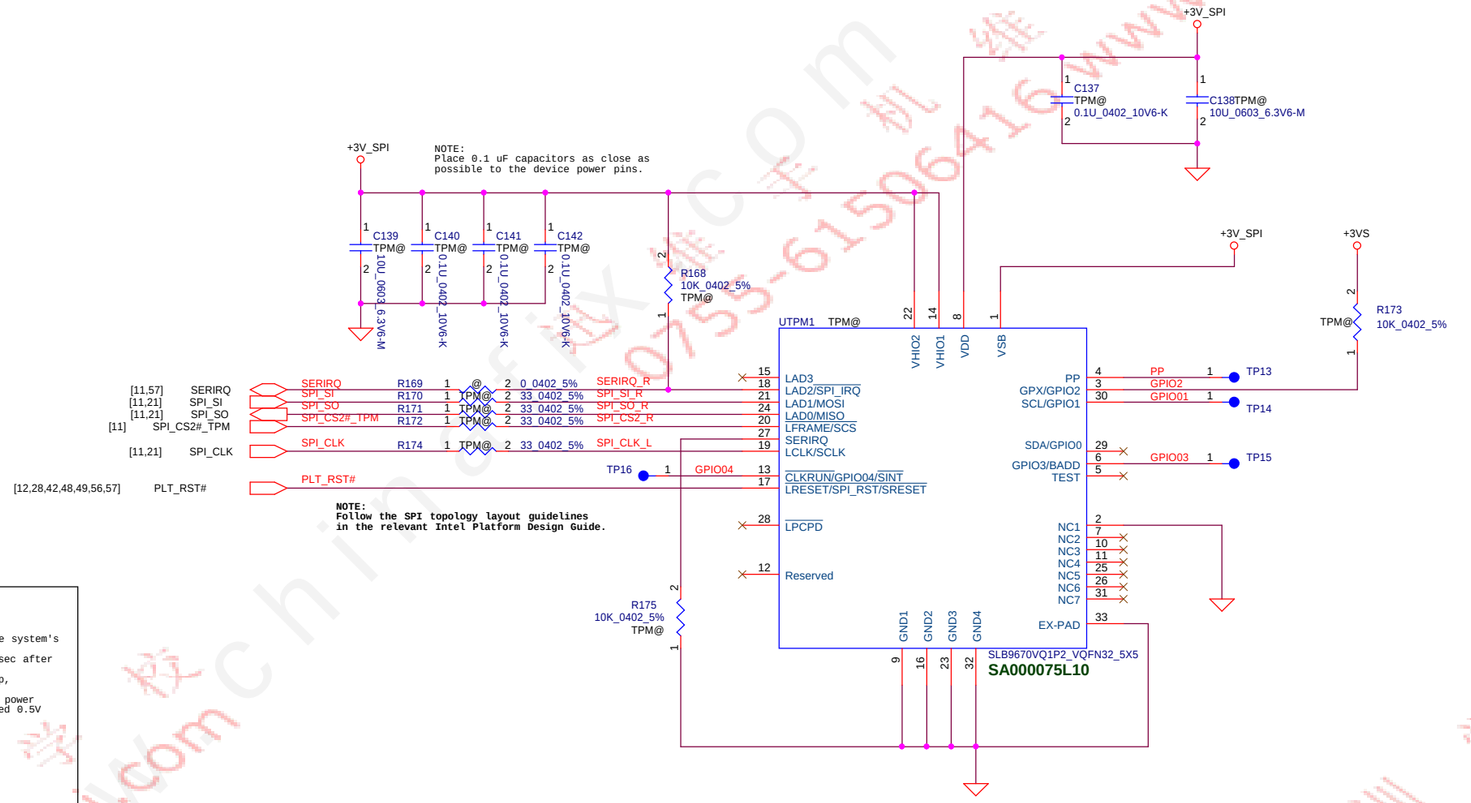
TABLE

| Pin No | TCG PTP Spec (x38) | Infineon SLB9670VQ1.2 FW 6.10 | ST Micro ST33HTPM2E33AAB9 | Nuvoton NPCT653LB0YX |
|---|---|---|---|---|
| 1 | VDD | VDD | NC | VSB |
| 2 | GND | GND | GND | NC |
| 3 | GPIO | NC | NC | GPX/GPIO2 |
| 4 | GPIO | NC | PP | PP |
| 5 | NC | NC | NC | TEST |
| 6 | VNC/GPIO | GPIO | NC | GPIO3 |
| 7 | GPIO/VDD | PP | GPIO | NC |
| 8 | VDD | VDD | NC | VDD |
| 9 | GND | GND | NC | GND |
| 10 | VNC | NC | NC | NC |
| 11 | NC | NC | NC | NC |
| 12 | NC | NC | NC | Reserved |
| 13 | VNC/GPIO | NC | NC | GPIO4 |
| 14 | VDD | NC | NC | VDD |
| 15 | NC | NC | NC | DNC |
| 16 | GND | NC | NC | GND |
| 17 | SPI_RST# | RST# | SPI_RST# | SPI_RST# |
| 18 | SPI_PIRQ# | PIRQ# | SPI_PIRQ# | SPI_IRQ# |
| 19 | SPI_CLK | SCLK | SPI_CLK | SCLK |
| 20 | SPI_CS# | CS# | SPI_CS# | SCS# |
| 21 | MOSI | MOSI | MOSI | MOSI |
| 22 | VDD | VDD | VPS | VDD |
| 23 | GND | GND | NC | GND |
| 24 | MISO | MISO | MISO | MISO |
| 25 | NC | NC | NC | NC |
| 26 | NC | NC | NC | NC |
| 27 | NC | NC | NC | (SERIRQ) |
| 28 | NC | NC | NC | DNC |
| 29 | VNC/GPIO | NC | NC | GPIO0 |
| 30 | VNC/GPIO | NC | NC | GPIO1 |
| 31 | VNC | NC | NC | NC |
| 32 | GND | GND | NC | GND |

Follow THP1_SWG_SIT_EC005, update TPM table

**NOTE:**
**Check timing sequence in SDV phase.**




| | | | |
|---|---|---|---|
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| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: TPM

Size: Custom | Document Number: SKYWALKER | Rev: 2.0

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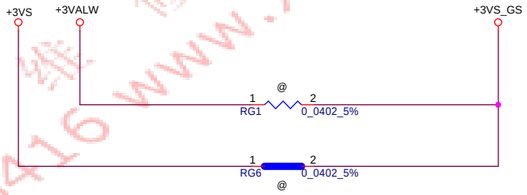


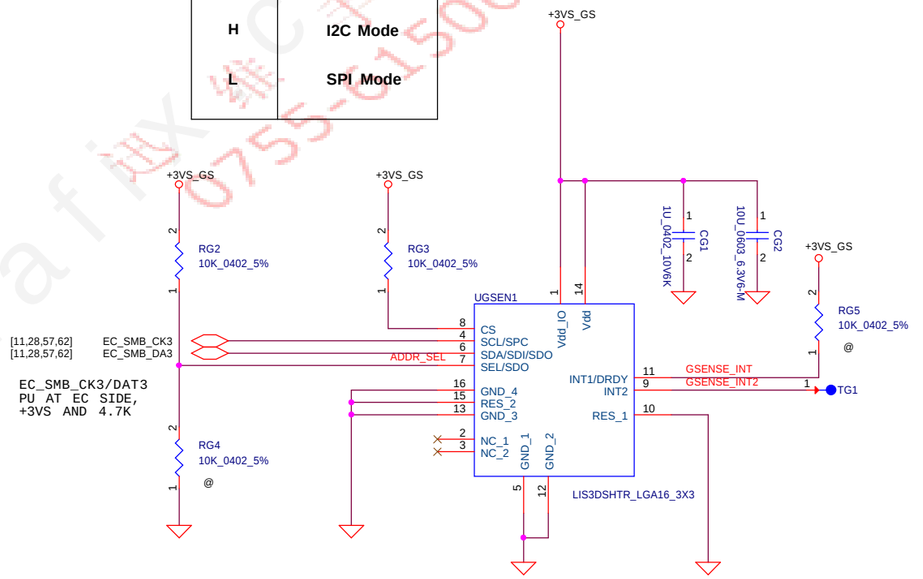

# APS G-Sensor

**TABLE**

| P/N | ADDR_SEL | Address |
|---|---|---|
| LIS3DSHTR | H | 32h (W) & 33h (R) |
| | L | 30h (W) & 31h (R) |
| KX023-1025 | H | 3Eh (W) & 3Fh (R) |
| | L | 3Ch (W) & 3Dh (R) |

**TABLE**

| P/N | Mode Selection |
|---|---|
| H | I2C Mode |
| L | SPI Mode |




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |

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Title: *G SENSOR*

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |
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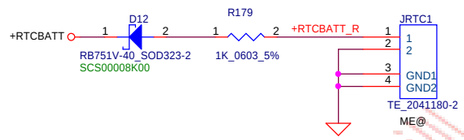
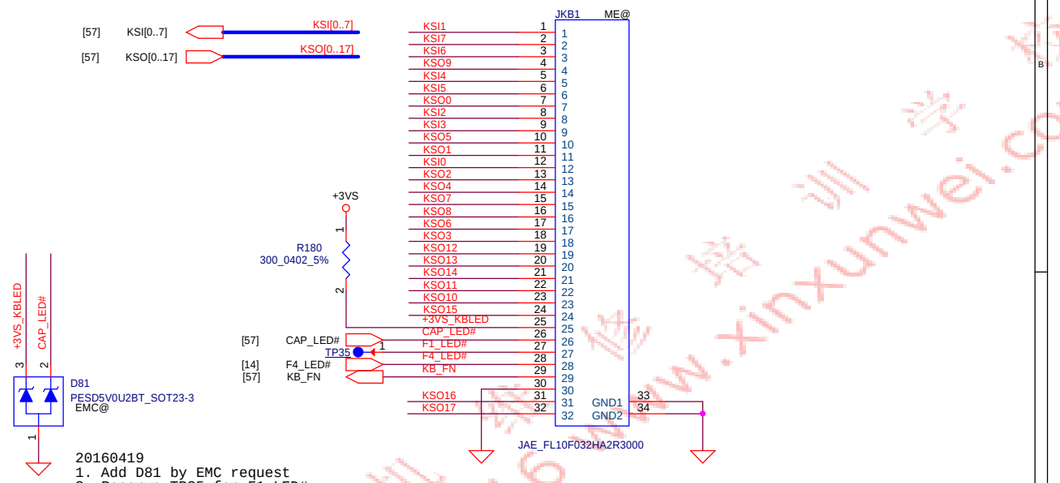
## RTC CONN.




## KB CONN




20160419
1. Add D81 by EMC request
2. Reserve TP35 for F1_LED#

| | | | |
|---|---|---|---|
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Title: **KB/RTC/TOUCH PAN CONN.**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |
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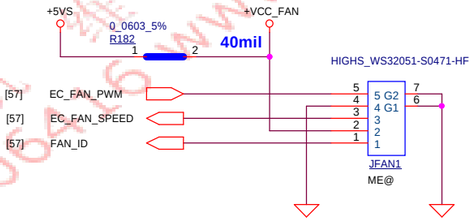
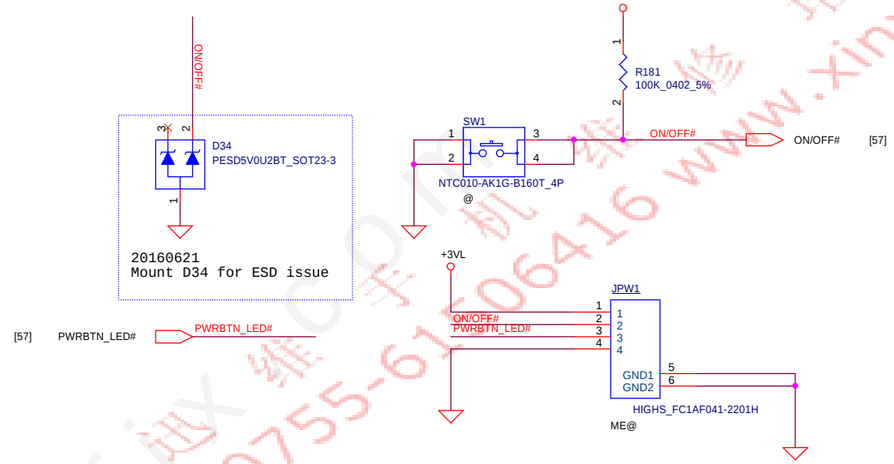
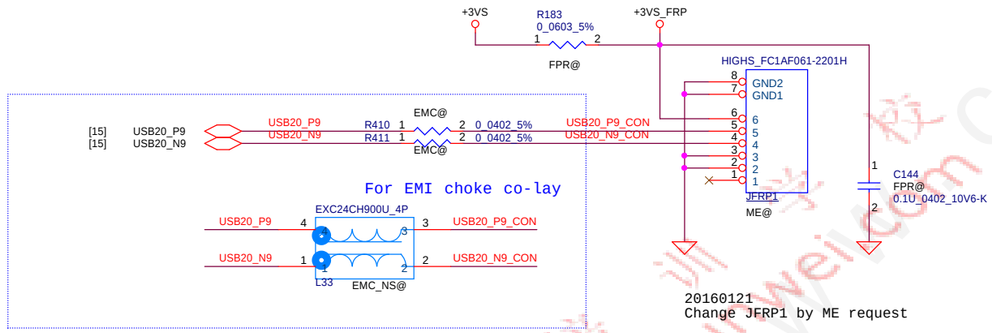
## FAN CONN.



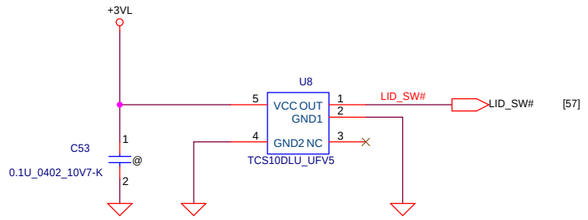

## PWR BTN



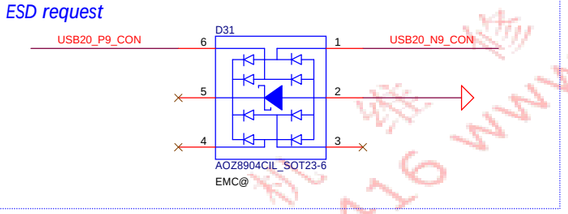

## FingerPrint CONN.




## Lid Switch




## ESD request




| | | | |
|---|---|---|---|
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| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **PBTN/LID/FP/FAN CONN.**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

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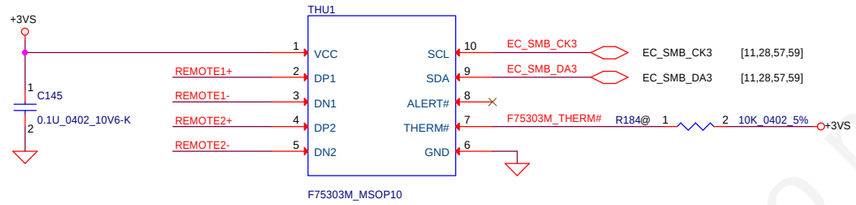
*Thermal Sensor*
*placed near by VRAM*

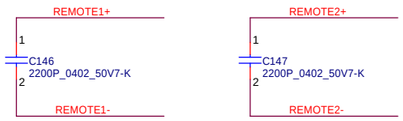



**Address 1001_101xb**

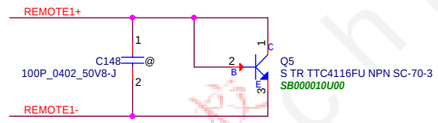
*Internal pull up 1.2K to 1.5V*
*R for initial thermal shutdown temp*

*REMOTE2+/-:*
*Trace width/space:10/10 mil*
*Trace length:<8"*

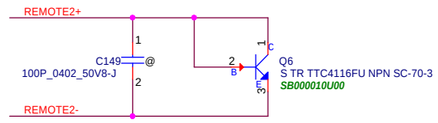
*Close to U1*

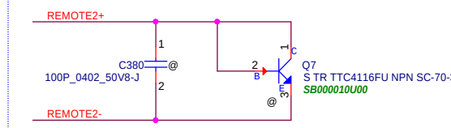



*Close to +VCC_CORE*




*Close JDIMM1&JDIMM2*




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: ***Thermal Sensor***

| Size | Document Number | Rev |
|---|---|---|
| Custom | ***SKYWALKER*** | 2.0 |

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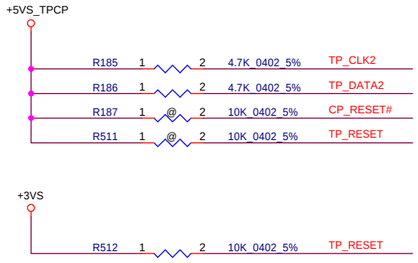
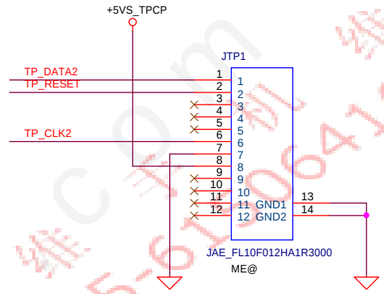
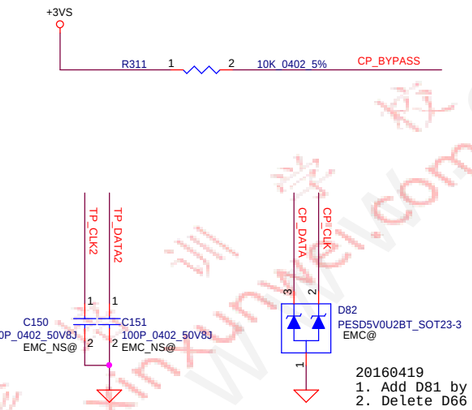


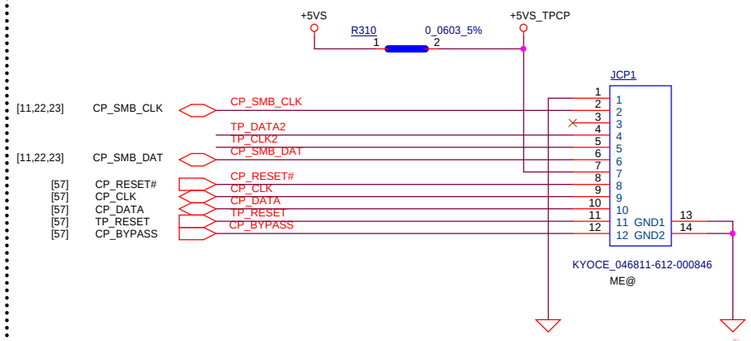

## Track point




20160419
1. Add D81 by EMC request
2. Delete D66 and connect to C150/C151

## Click Pad




20160417
Change JCP1 to KYOCE_046811-612-000846

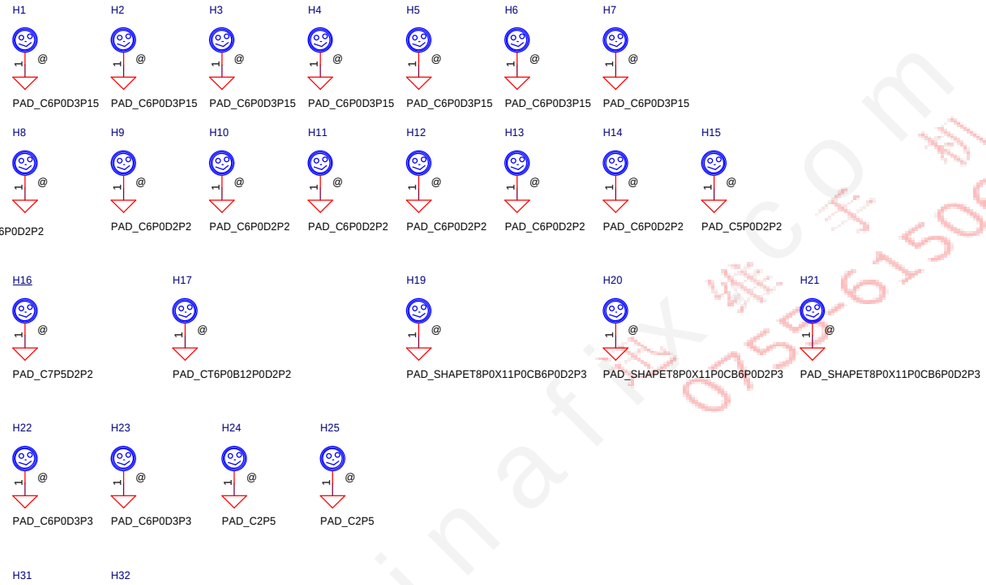
| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: CP/TPOINTCONN.

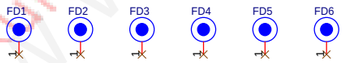
| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |
| Date: Thursday, August 25, 2016 | Sheet 63 of 82 | |

# Screw Hole




Center Zero

## PCB Fedical Mark PAD



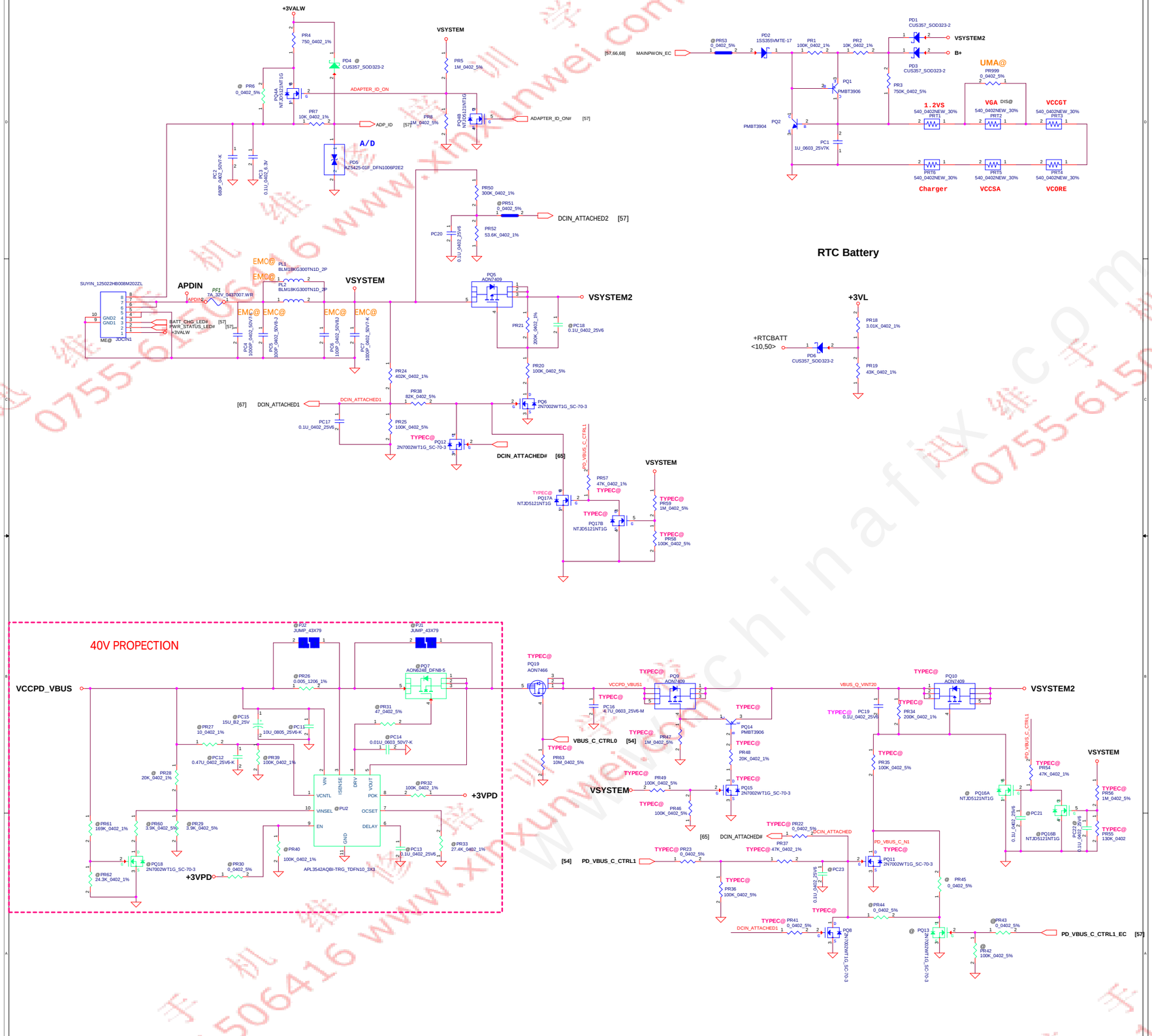

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2015/09/01 | Deciphered Date | 2016/12/31 |



Title: **P68-PLM/SCREW HOLE**

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKYWALKER | 2.0 |

Date: Thursday, August 25, 2016 Sheet 64 of 82




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
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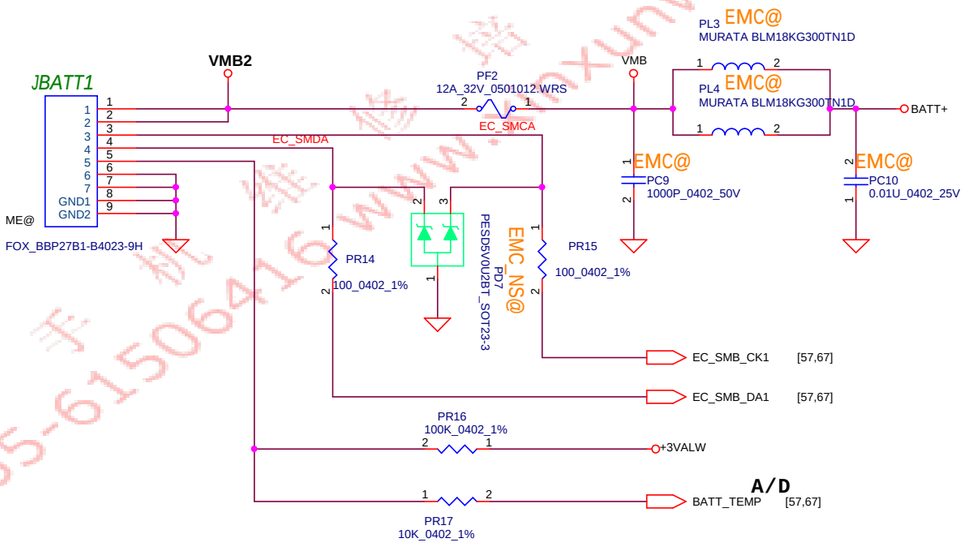
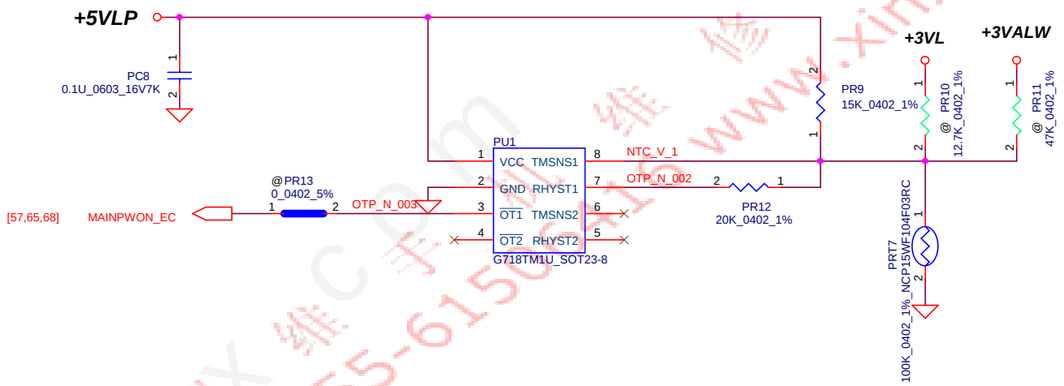
Title: *DCIN / VIN Detector*

Size: Custom | Document Number: **KENOBI** | Rev: 2.0

Date: Thursday, August 25, 2016 | Sheet 65 of 82




***PRT7 under CPU bottom side for CPU thermal protection***
***This is fot thermal team request***



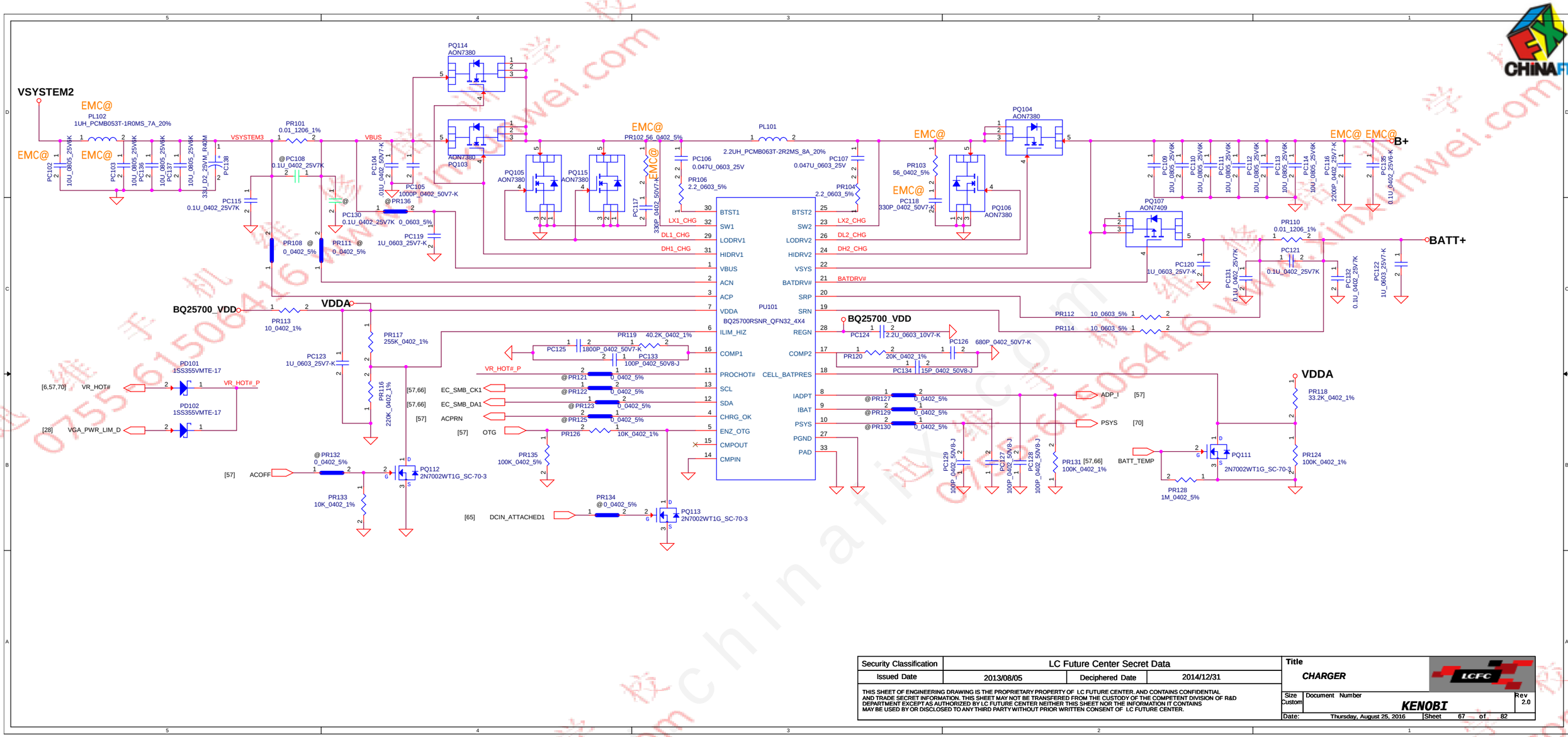

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 |



Title: ***BATTERY CONN/OTP***

| Size | Document Number | Rev |
|---|---|---|
| Custom | ***Skywalker*** | 2.0 |

Date: Thursday, August 25, 2016 Sheet 66 of 83




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 |



Title: CHARGER

| Size | Document Number | Rev |
|---|---|---|
| Custom | KENOBI | 2.0 |

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+3VALW
FSW=750 KHz
TDC:8A
OCP:11A

+5VALW
FSW=750 KHz
TDC:8A
OCP:11A

6800pf soft start 2ms
47nf soft start 7ms

| | | | |
|---|---|---|---|
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| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 |

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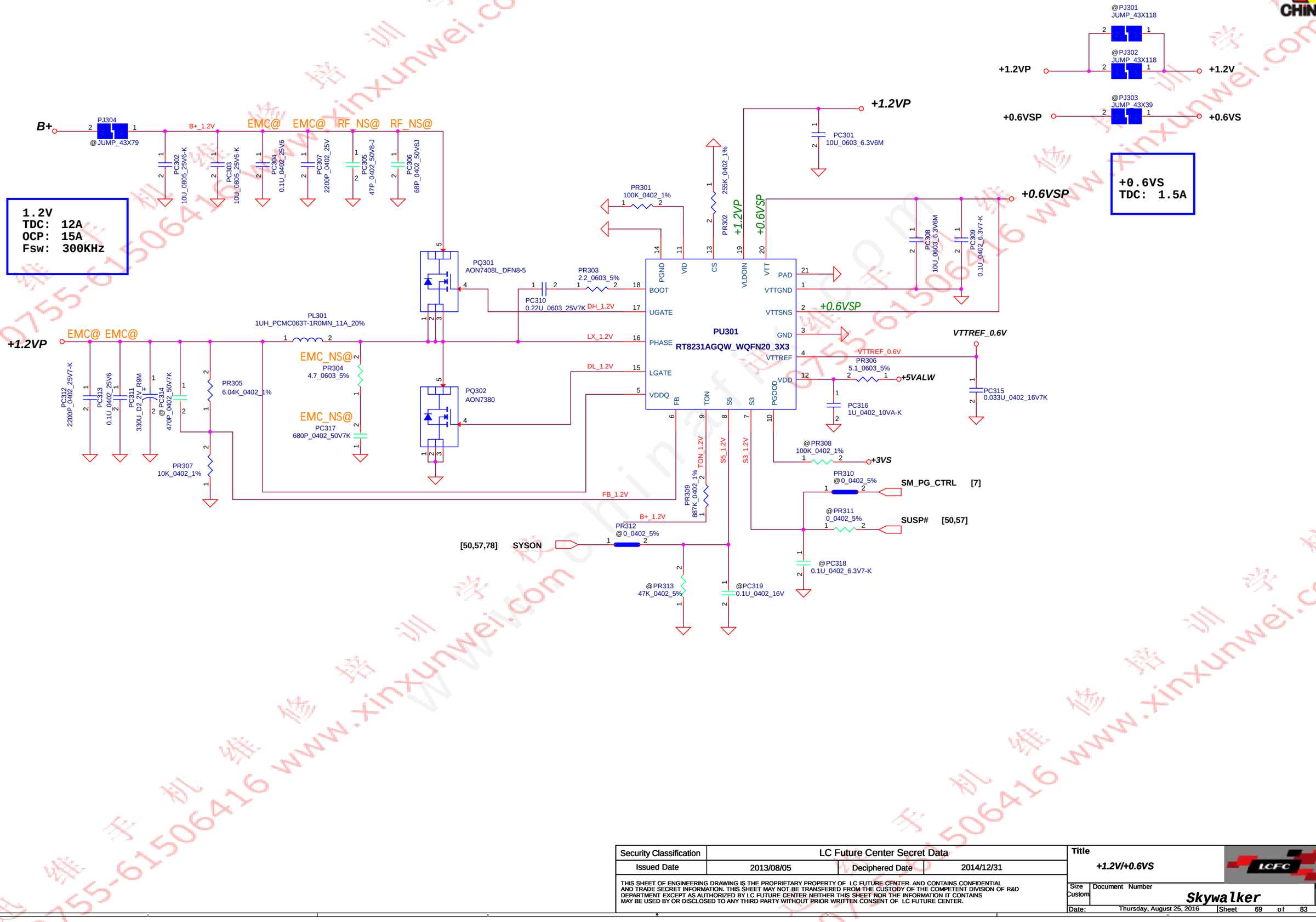
Title: +3VALW/+5VALW

Size: Custom | Document Number: Skywalker | Rev: 2.0

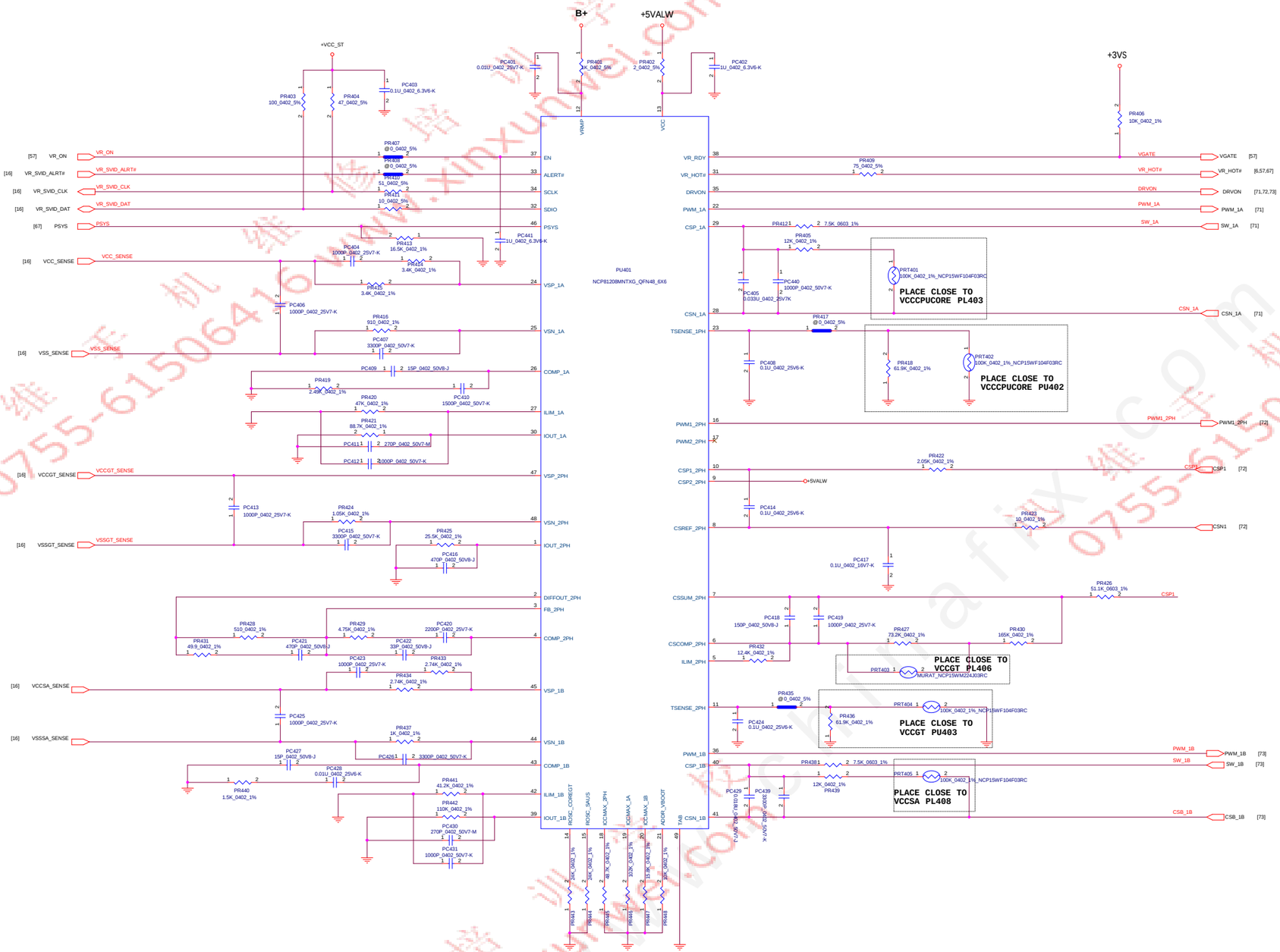
Date: Thursday, August 25, 2016 | Sheet 68 of 83




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 |



| | | | |
|---|---|---|---|
| Title | +1.2V/+0.6VS | | |
| Size Custom | Document Number | Skywalker | Rev 2.0 |
| Date: Thursday, August 25, 2016 | Sheet 69 of 83 | | |




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 |

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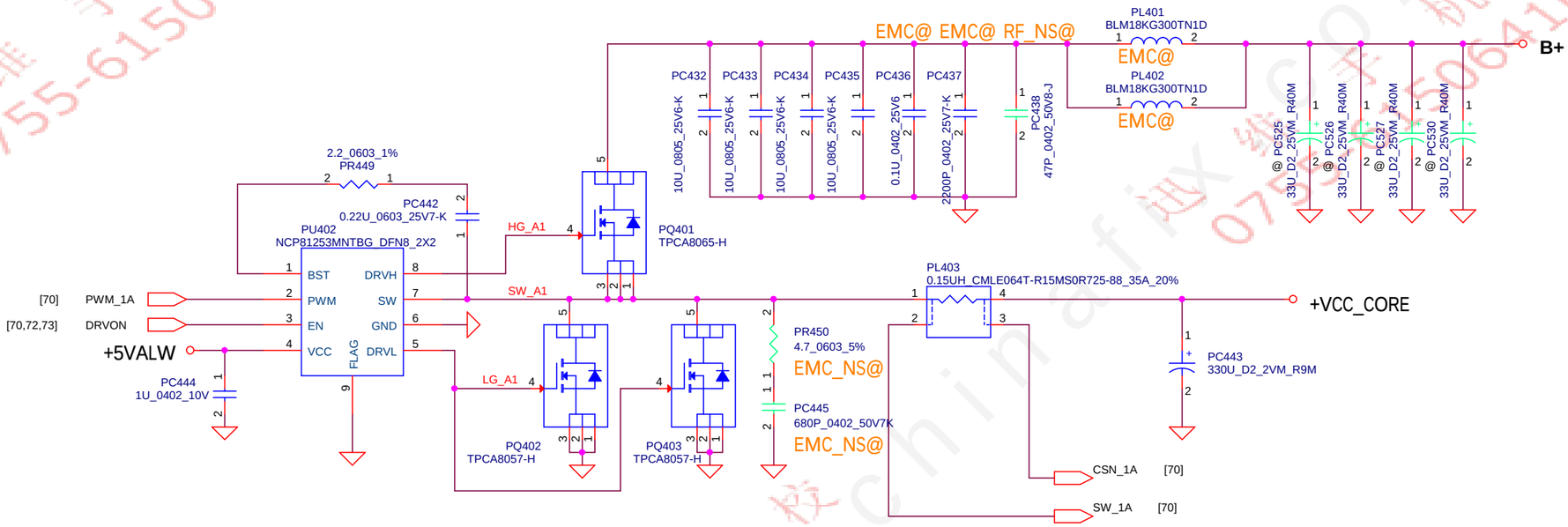
| | | | |
|---|---|---|---|
| Title | IMVP8 | | |
| Size | Document Number | | Rev |
| D | Skywalker | | 2.0 |
| Date: | Thursday, August 25, 2016 | Sheet 70 of 83 | |




+VCC_CORE
TDC= 21A
IccMAX=31A
OCP = 36A

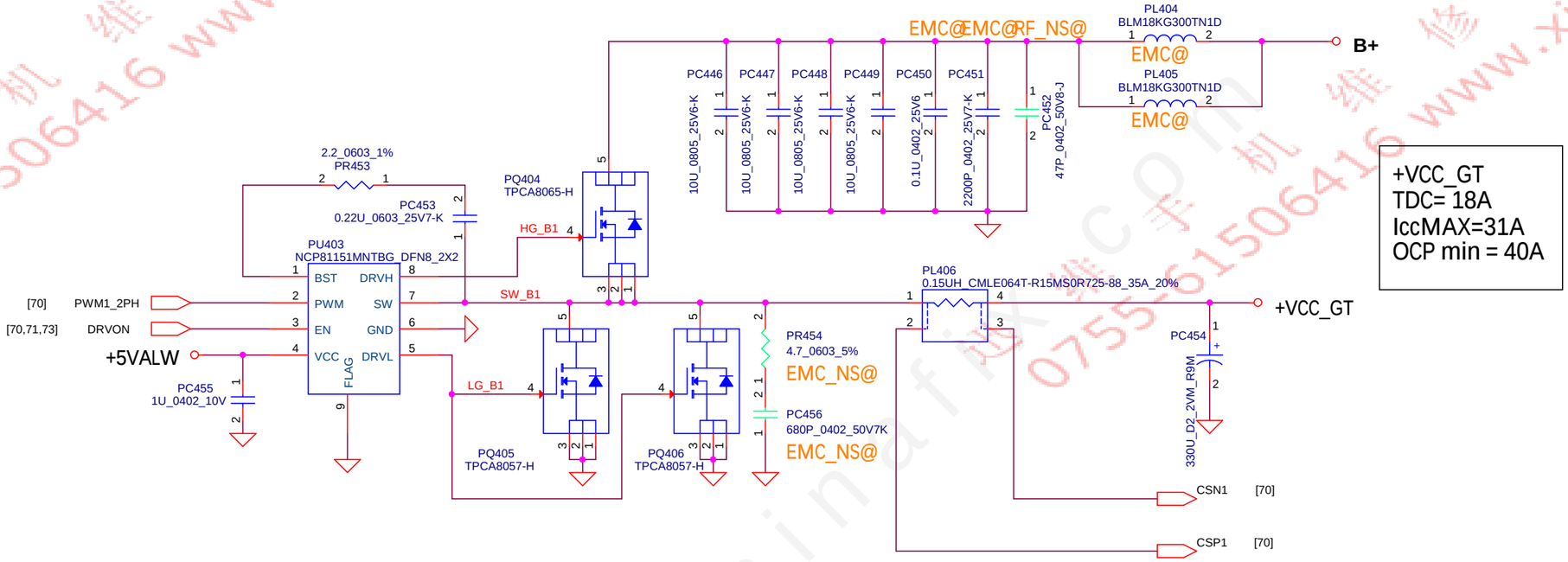
| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 |



Title: *+VCC_CORE*

| Size | Document Number | Rev |
|---|---|---|
| Custom | *Skywalker* | 2.0 |

Date: Thursday, August 25, 2016 Sheet 71 of 83



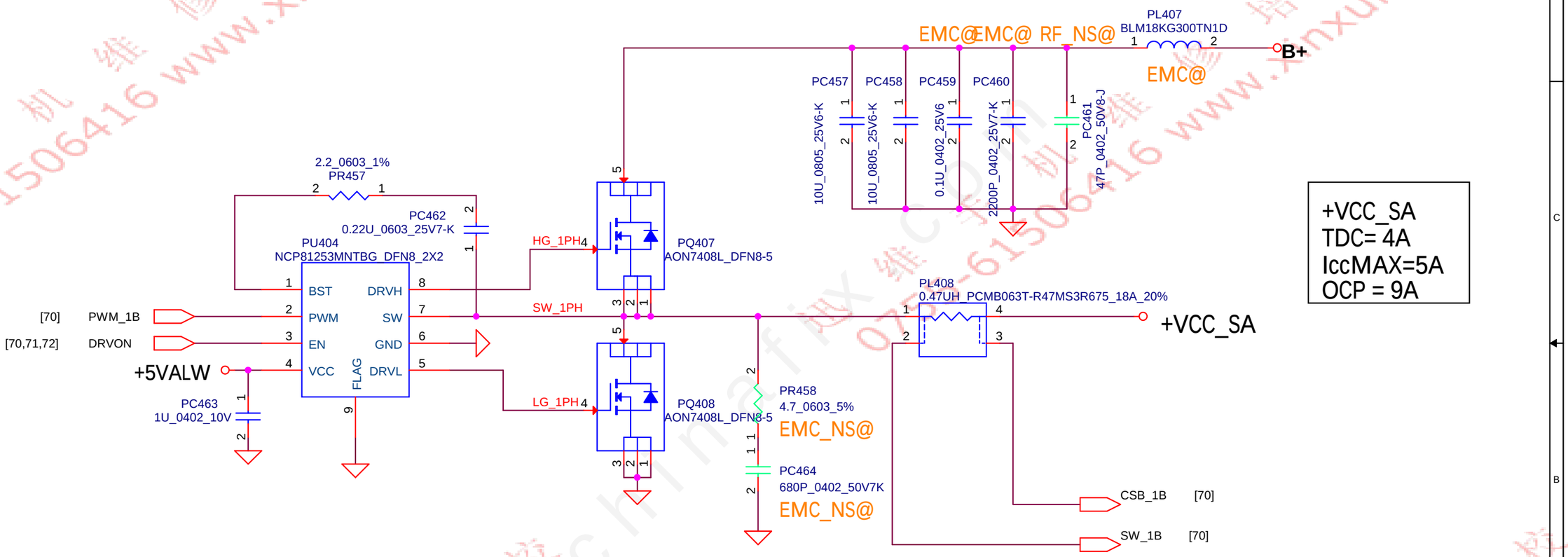

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 |



Title: +VCC_GT

Size: Custom | Document Number: Skywalker | Rev: 2.0

Date: Thursday, August 25, 2016 | Sheet 72 of 83




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 |



Title: *+VCC_SA*

Size: Custom | Document Number: ***Skywalker*** | Rev: 2.0

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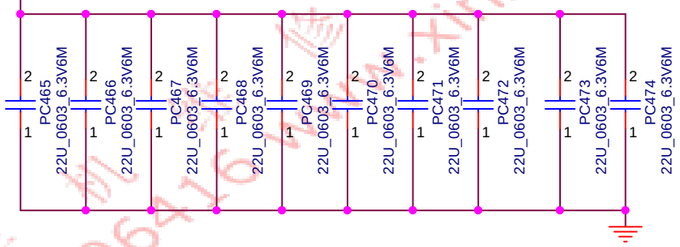
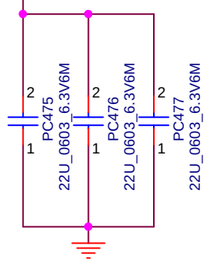
**Based on PDDG rev 0.7 Table 5-1.**

+VCC_CORE

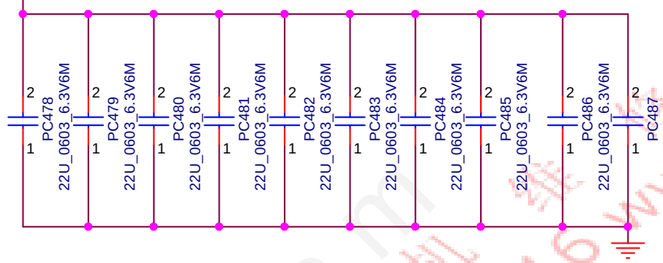
23pcs 22uF for +VCC_CORE




+VCC_CORE

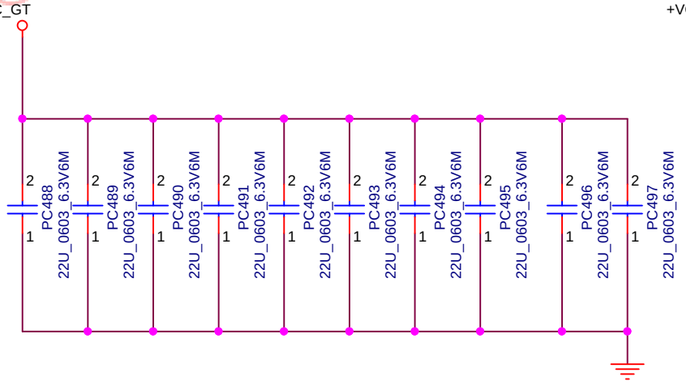



+VCC_CORE

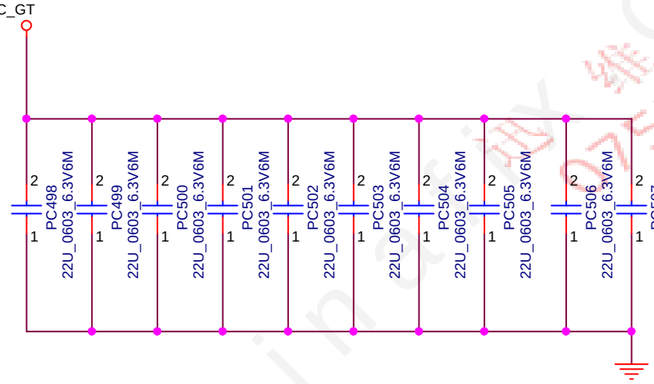



25pcs 22uF for +VCC_GT

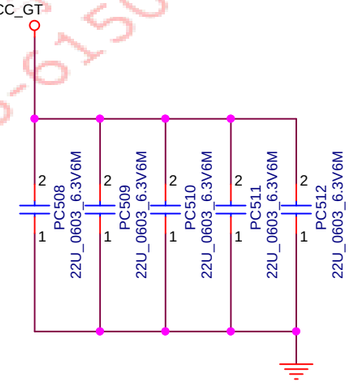
+VCC_GT




+VCC_GT

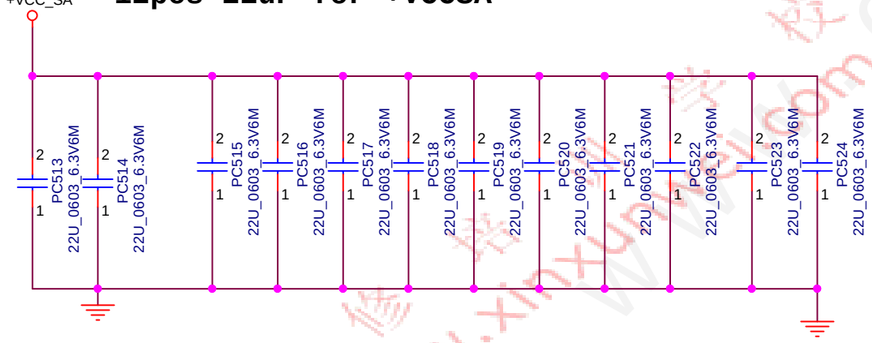



+VCC_GT




+VCC_SA

12pcs 22uF for +VCCSA




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 |



Title: **PROCESSOR DECOUPLING**

| Size | Document Number | Rev |
|---|---|---|
| B | Skywalker | 2.0 |

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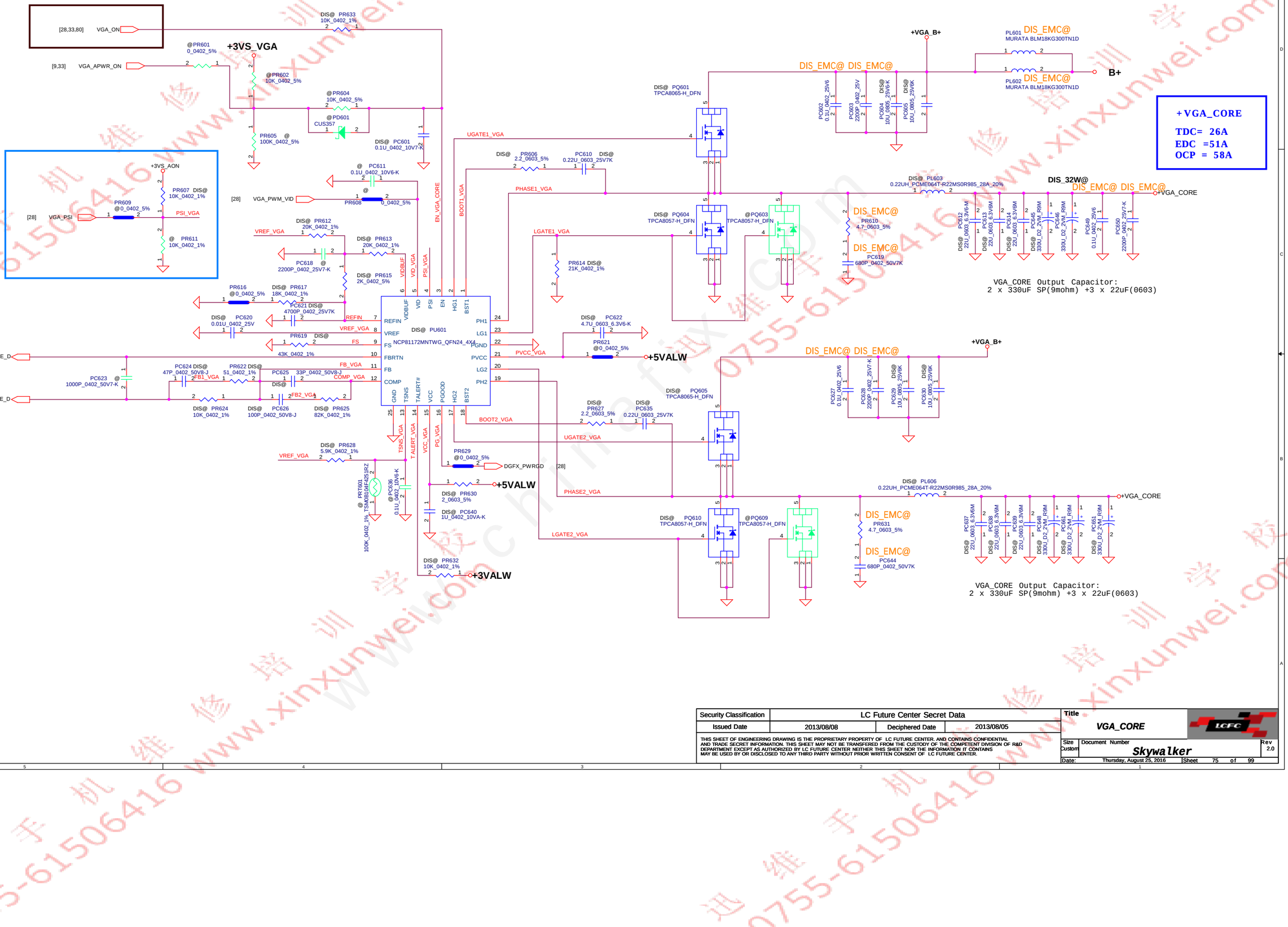


| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/08 | Deciphered Date | 2013/08/05 |



Title: VGA_CORE

| Size | Document Number | Rev |
|---|---|---|
| Custom | Skywalker | 2.0 |

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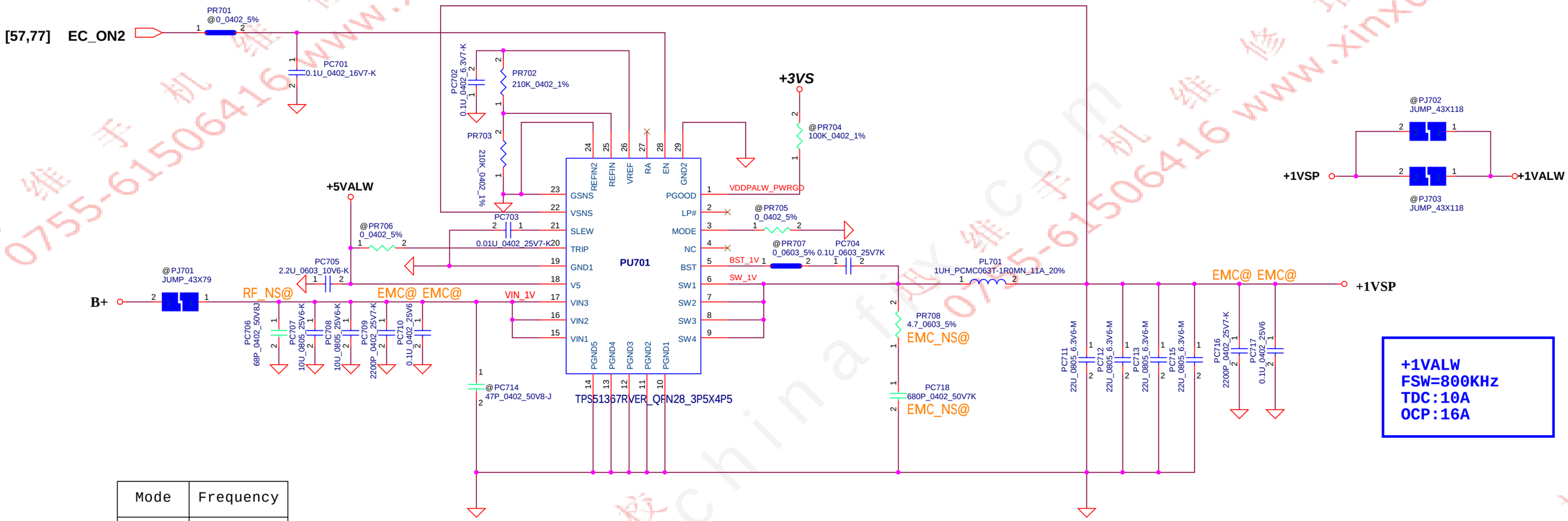


| Mode | Frequency |
|---|---|
| GND | 400KHz |
| Float | 800KHz |

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/01 | Deciphered Date | 2014/08/01 |



Title: +1VALW

| Size | Document Number | Rev |
|---|---|---|
| Custom | Skywalker | 2.0 |

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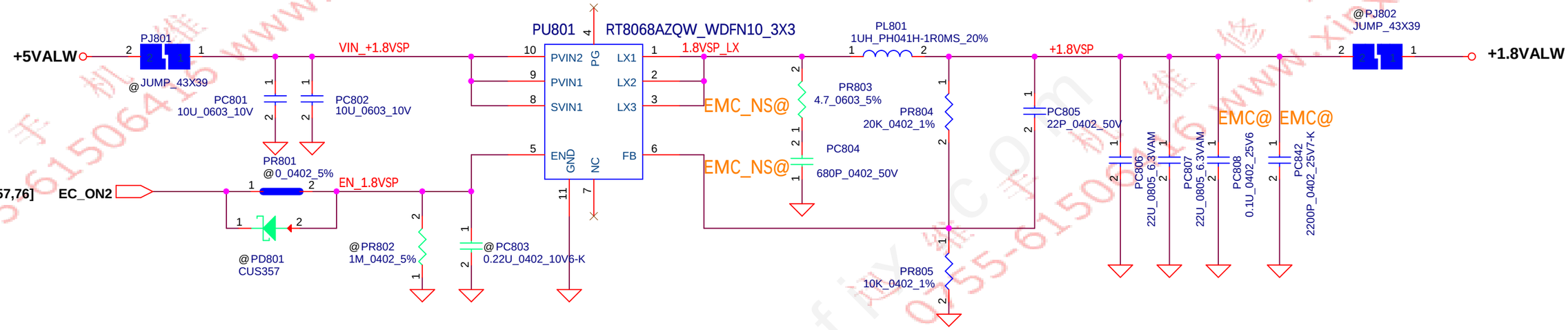


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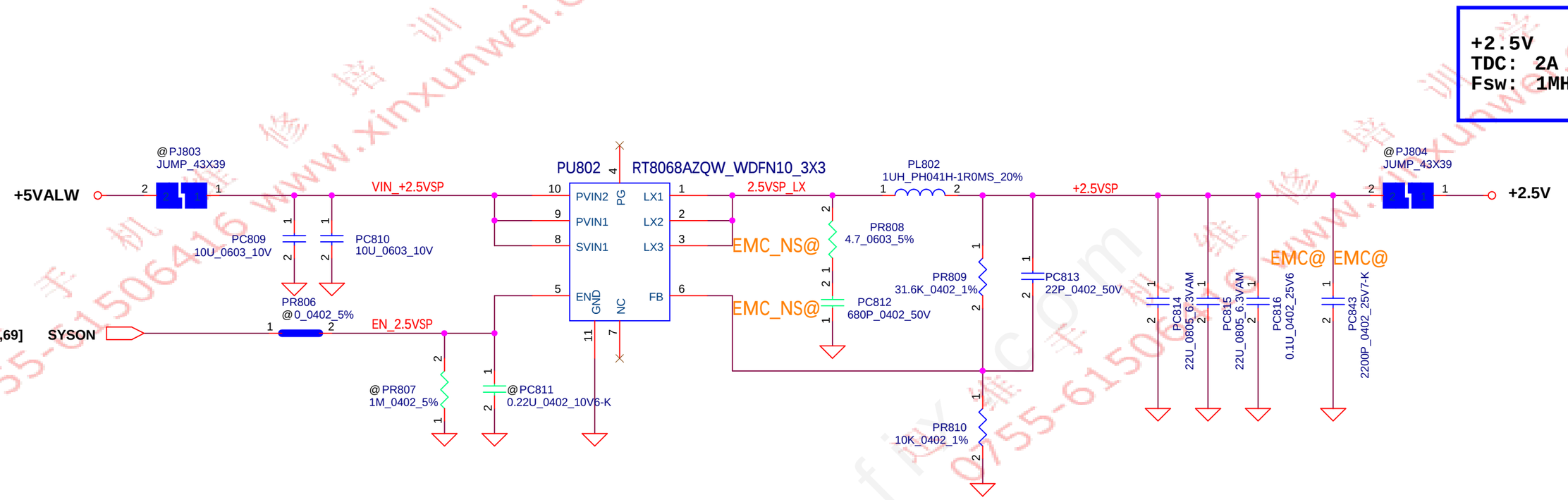
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 |



| | | | |
|---|---|---|---|
| Title | +1.8VALW | | |
| Size | Custom | Document Number | Rev 2.0 |
| | | Skywalker | |
| Date: | Thursday, August 25, 2016 | Sheet 77 of 83 | |




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 |



| | | | |
|---|---|---|---|
| Title | +2.5V | | |
| Size | Document Number | | Rev |
| Custom | Skywalker | | 2.0 |
| Date: | Thursday, August 25, 2016 | Sheet | 78 of 83 |

+1.35VS_VGA
TDC: 8A
OCP: 16A
Fsw: 650KHz

@PD802
CUS357

DIS@ PR811
100K_0402_1%

[28] FB_PWR_EN

DIS@ PR812
200K_0402_1%

DIS@ PC817
0.1U_0402_16V

@PJ805
JUMP_43X79

B+

DIS_32W@

DIS_EMC@ DIS_EMC@

DIS@ PC818 10U_0805_25V
DIS@ PC841 10U_0805_25V
DIS@ PC819 0.1U_0402_25V
DIS@ PC844 2200P_0402_25V7-K

DIS@ PU803

IN
GND
ILMT
PG
EN
BS
LX
FB
BYP
LDO

SYX198DQNC_QFN10_3X3

+3VS

PR814
@0_0402_5%

@PR815
100K_0402_1%

PR827
0_0402_5%

@PR816
0_0402_5%

[25] VDDQPWRGD

DIS@ PC820 4.7U_0402_6.3V6-M
DIS@ PC821 4.7U_0402_6.3V6-M

+3VALW

BS_1.35VSP
SW_1.35VSP
FB_1.35VSP

@PR813 0_0603_5%
DIS@ PC822 0.1U_0603_25V7K

DIS@ PL803
1UH_PCMC063T-1R0MN_11A_20%

DIS_EMC_NS@
PR820
4.7_0603_5%

DIS_EMC_NS@
PC823
680P_0402_50V

DIS@ PC824
330P_0402_50V

DIS@ PR817
1K_0402_1%

DIS@ PR818
30.1K_0402_1%

DIS_32W@
+1.35VSP

DIS@ PC825 22U_0805_6.3V6-M
DIS@ PC826 22U_0805_6.3V6-M
DIS@ PC827 22U_0805_6.3V6-M
DIS@ PC828 22U_0805_6.3V6-M
DIS@ PC839 22U_0805_6.3V6-M
DIS@ PC840 22U_0805_6.3V6-M
DIS@ PC829 2200P_0402_25V
DIS@ PC830 0.1U_0402_25V6

DIS_EMC@
DIS_EMC@

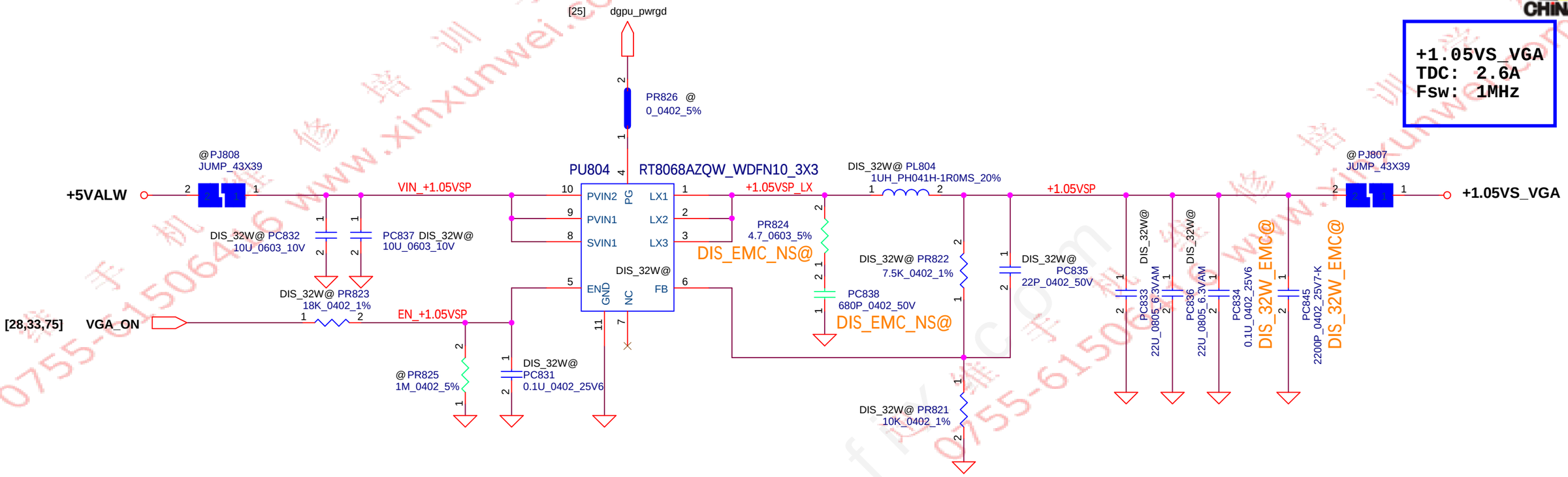
@PJ806
JUMP_43X118

+1.35VS_VGA

DIS@ PR819
24K_0402_1%



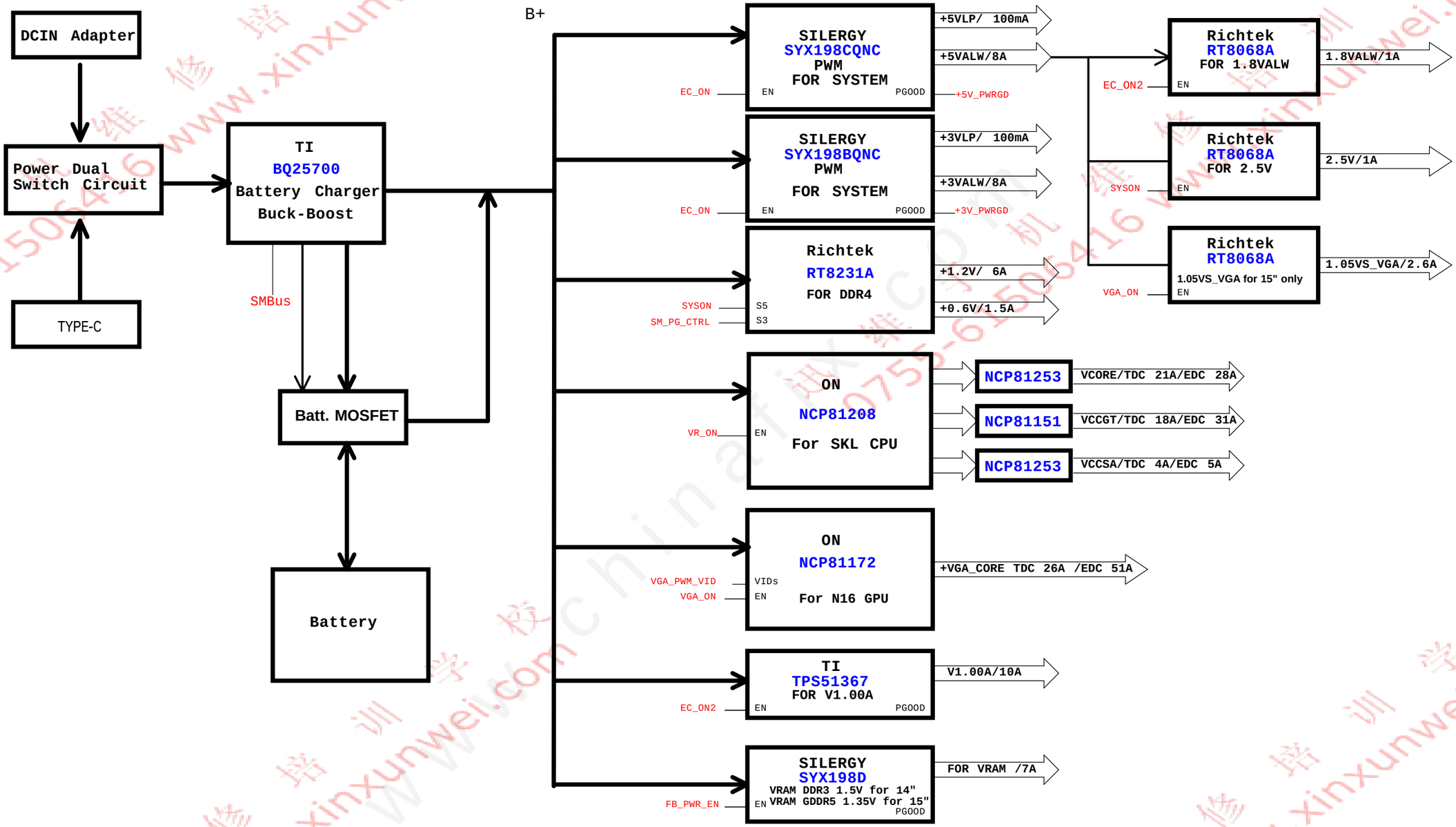
| Title | | |
|---|---|---|
| +1.35VS_VGA | | |
| Size: Custom | Document Number: Skywalker | Rev: 2.0 |
| Date: Thursday, August 25, 2016 | Sheet 79 of 99 | |




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2013/08/05 | Deciphered Date | 2014/12/31 |



| | | | |
|---|---|---|---|
| Title | +1.05VS_VGA | | |
| Size: Custom | Document Number: Skywalker | | Rev: 2.0 |
| Date: Thursday, August 25, 2016 | Sheet 80 of 99 | | |

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|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | | Deciphered Date | |



Title: *Power Block Diagram*

| Size | Document Number | Rev |
|---|---|---|
| Custom | *Skywalker* | 2.0 |
| Date: Thursday, August 25, 2016 | Sheet 81 of 99 | |

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|---|---|---|---|
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Title: *XXXX*

| Size | Document Number | Rev |
|---|---|---|
| Custom | *SKYWALKER* | 2.0 |

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