

CB-3 LOGIC SCHEMATICS

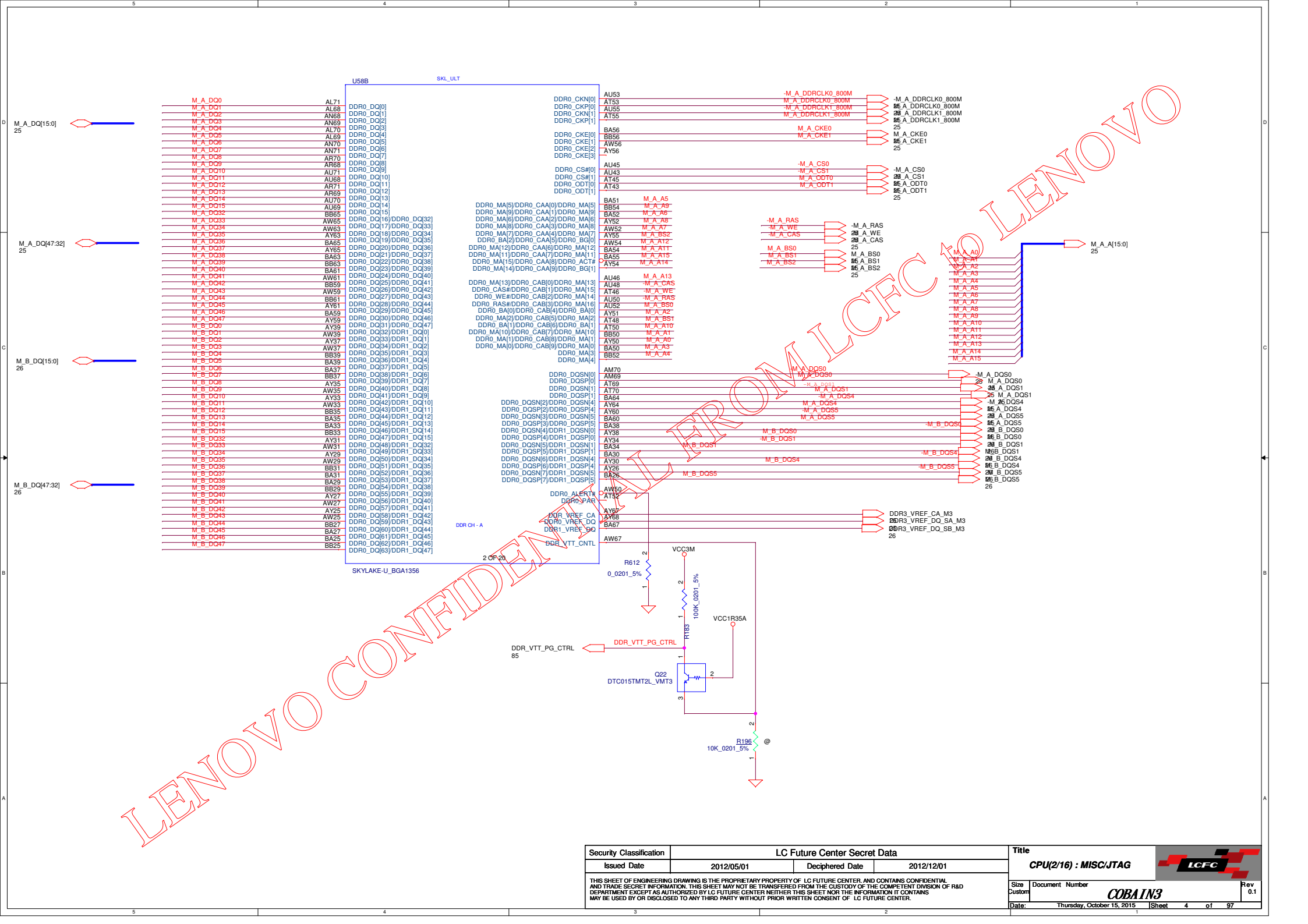
001.TITLE PAGE	36.MEMORY TERMINATION	
002.EC HISTORY	37.BLANK	
003.CPU(1/16) : DDI/EDP	38.LCD CONNECTOR	
004.CPU(2/16) : MISC/JTAG	39.BLANK	
005.CPU(3/16) : DDR3L CHANNEL-A	40.EXT CRT INTERFACE	
006.CPU(4/16) : DDR3L CHANNEL-B	41.DISPLAY PORT CONNECTOR	71.THINK ENGINE(1/2)
007.CPU(5/16) : RTC/HDA/SATA/JTAG	42.BLANK	72.THINK ENGINE(2/2)
008.CPU(6/16) : CLOCK SIGNALS	43.SATA HDD CONN	73.DC-IN
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010.CPU(8/16) : SYSTEM PM	45.USB POWER/CONN	75.BATTERY CHARGER(BQ24760)
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012.CPU(10/16) : GPIO/CPU/MISC/LPIO	47.BLANK	77.BATTERY MONITOR
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014.CPU(12/16) : POWER	49.RJ45 CONNECTOR	79.DC/DC VCCCPUCORE(VT1328M)
015.CPU(13/16) : POWER	50.PCIE MINI CARD SLOT	80.DC/DC VCCCPUCORE(VT1334S)
016.CPU(14/16) : GND	51.MEDIA CARD CONTROLLER	81.BLANK
017.CPU(15/16) : NCTF	52.MEDIA CARD INTERFACE	82.VCCCPUCORE DECOUPLING
018.CPU(16/16) : CFG/RESERVED	53.SMART CARD I/F	83.DC/DC VCCGFXCORE_D (TPS51728)
019.DDI-VGA CONVERTER	54.AUDIO ALC3232-GR	84.BLANK
020.BLANK	55.AUDIO CONNECTOR	85.DC/DC VCC1R05AMT(VT356)
021.XDP CONNECTOR	56.AUDIO JACK SENSE	86.DC/DC VCC1R35A(VT357)
022.RTC BATTERY	57.AUDIO EXT MIC I/F	87.DC/DC VCC0R675B(TPS51200)
023.SPI FLASH	58.AUDIO SPEAKER	88.DC/DC VCC1R5VIDEO(VT356)
024.DDR3L SO DIMM CHANNEL-A	59.AUDIO BEEP	89.DC/DC VCC1R05VIDEO_PLL(BD3551HFN)
025.BLANK	60.BLANK	90.DC/DC VCC1R8B(BD9139)
026.DDR3L SO DIMM CHANNEL-B	61.MEC1619(1/3)	91.BLANK
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028.N15S-GM(1/6) : PEG I/F	63.MEC1619(3/3)	93.LOAD SW PCH SUS
029.N15S-GM(2/6) : DIGITAL OUT I/F	64.KEYBOARD CONNECTOR	94.LOAD SW LAN
030.N15S-GM(3/6) : VRAM I/F	65.TOUCH PAD CONNECTOR	95.LOAD SW VIDEO
031.N15S-GM(4/6) : GPIO	66.BLANK	96.LOAD SW B
032.N15S-GM(5/6) : POWER	67.FAN CONNECTOR	97.BLANK
033.N15S-GM(6/6) : GND	68.G-SENSOR	98.LOAD SW WWAN & WLAN
034.VRAM CHANNEL-A	69.TPM	99.PTH FOR SCREW HOLES
035.BLANK	70.EEPROM/SMBUS SW	100.3rd USB

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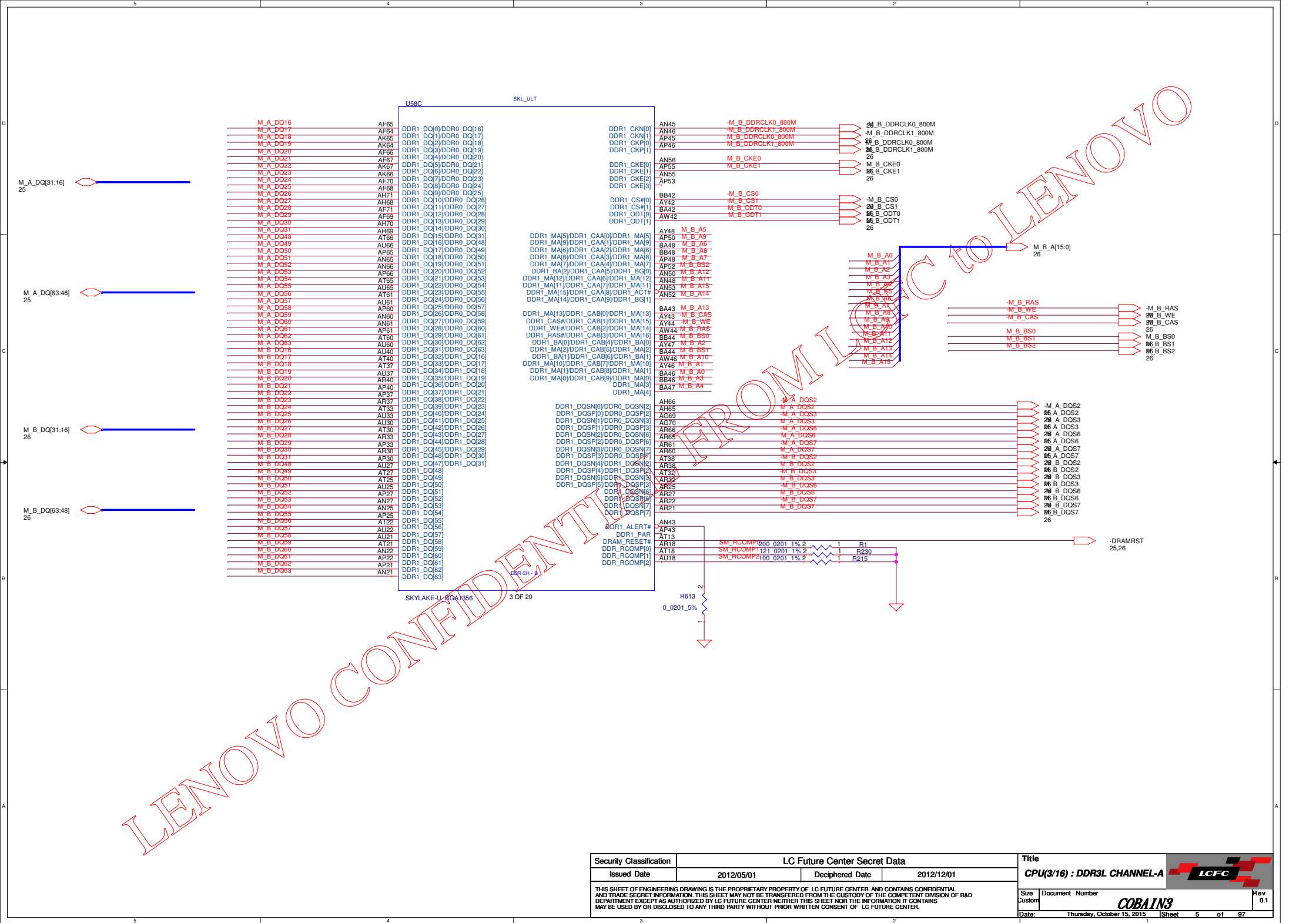
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2012/10/09	CB_1_SWG_SDV_EC011	JV_CB-1_SWG_SDV1_SCH_EC009-010_100801.pdf
2012/10/12	CB_1_SWG_SDV_EC012	JV_CB-1_SWG_SDV1_SCH_EC010-011_101101.pdf
2012/10/13	CB_1_SWG_SDV_EC013	JV_CB-1_SWG_SDV1_SCH_EC011-012_101201.pdf
2012/10/16	CB_1_SWG_SDV_EC014	JV_CB-1_SWG_SDV1_SCH_EC013_101501.pdf
2012/10/17	CB_1_SWG_SDV_EC015	JV_CB-1_SWG_SDV1_SCH_EC014_101601.pdf
2012/10/18	CB_1_SWG_SDV_EC016	JV_CB-1_SWG_SDV1_SCH_EC015_101701.pdf
2012/10/19	CB_1_SWG_SDV_EC017	JV_CB-1_SWG_SDV1_SCH_EC016_101801.pdf
2012/10/20	CB_1_SWG_SDV_EC018	JV_CB-1_SWG_SDV1_SCH_EC017_101901.pdf
2012/10/25	CB_1_SWG_SDV_EC018-022	JV_CB-1_SWG_SDV1_SCH_EC018-021_102401.pdf
2012/10/31	CB_1_SWG_SDV_EC023	JV_CB-1_SWG_SDV1_SCH_EC022_103001.pdf
2012/10/32	CB_1_SWG_SDV_EC023-025	JV_CB-1_SWG_SDV1_SCH_EC023-024_103101.pdf
2012/11/15	CB_1_SWG_SDV_EC025-033	JV_CB-1_SWG_SDV1_SCH_EC025-032_111401.pdf
2012/11/23	CB_1_SWG_SDV_EC033-036	JV_CB-1_SWG_SDV1_SCH_EC025-035_112201.pdf
2012/11/27	CB_1_SWG_SDV_EC037	JV_CB-1_SWG_SDV1_SCH_EC036_112601.pdf
2012/12/05	CB_1_SWG_SDV_EC037-039	JV_CB-1_SWG_SDV_SCH_EC037-038_120401.pdf


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				Quoted	COBAIN2 SWG
				Date:	Thursday, October 16, 2015 (Sheet 2 of 97)

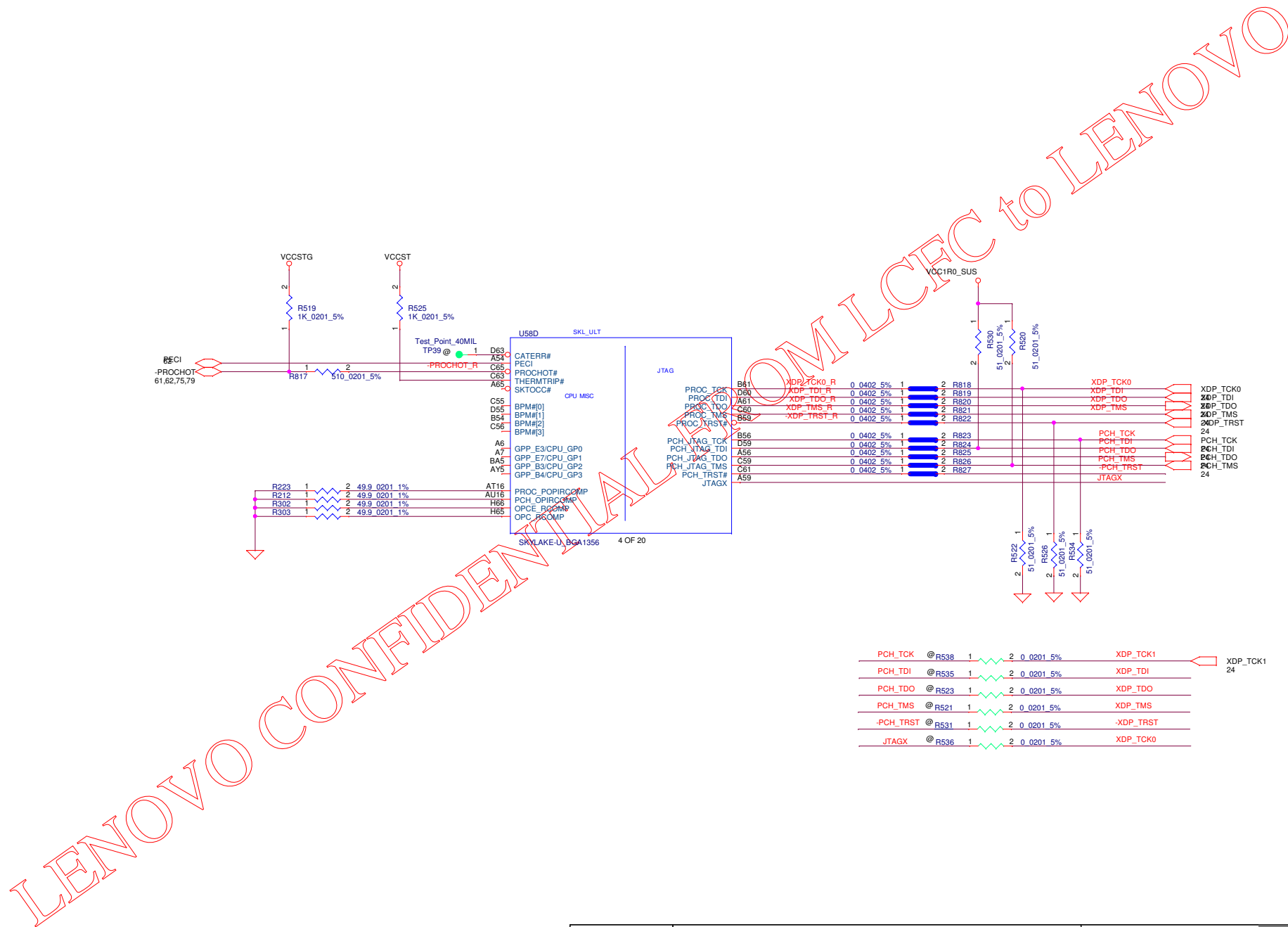




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Size Custom		Document Number		COBATN3		Rev 0.1	
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PCH_TCK	@ R538	1	2	0.0201 5%	XDP_TCK1	XDP_TCK1
PCH_TDI	@ R535	1	2	0.0201 5%	XDP_TDI	24
PCH_TDO	@ R523	1	2	0.0201 5%	XDP_TDO	
PCH_TMS	@ R521	1	2	0.0201 5%	XDP_TMS	
-PCH_TRST	@ R531	1	2	0.0201 5%	-XDP_TRST	
JTAGX	@ R536	1	2	0.0201 5%	XDP_TCK0	

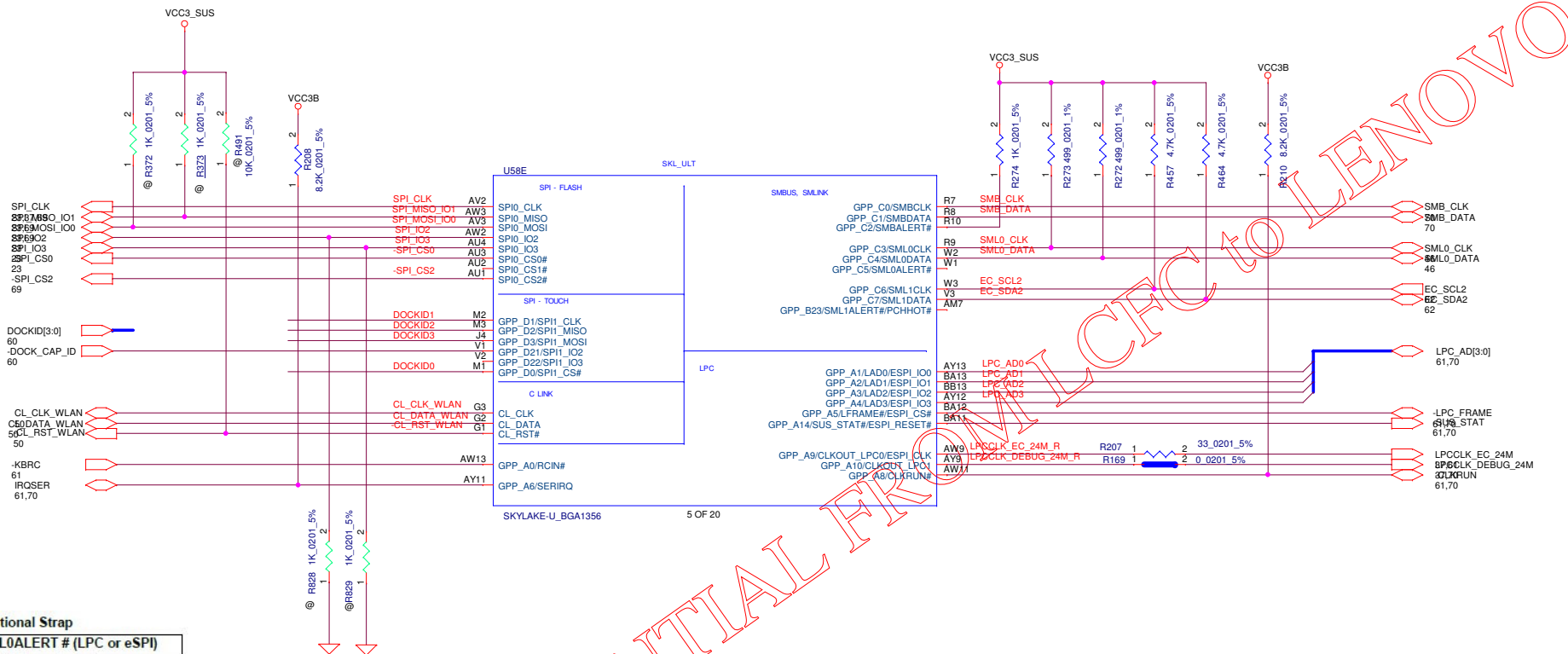


TABLE : Functional Strap

GPP_C5/SML0ALERT# (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

TABLE : Functional Strap

GPP_B22/GSPI0_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

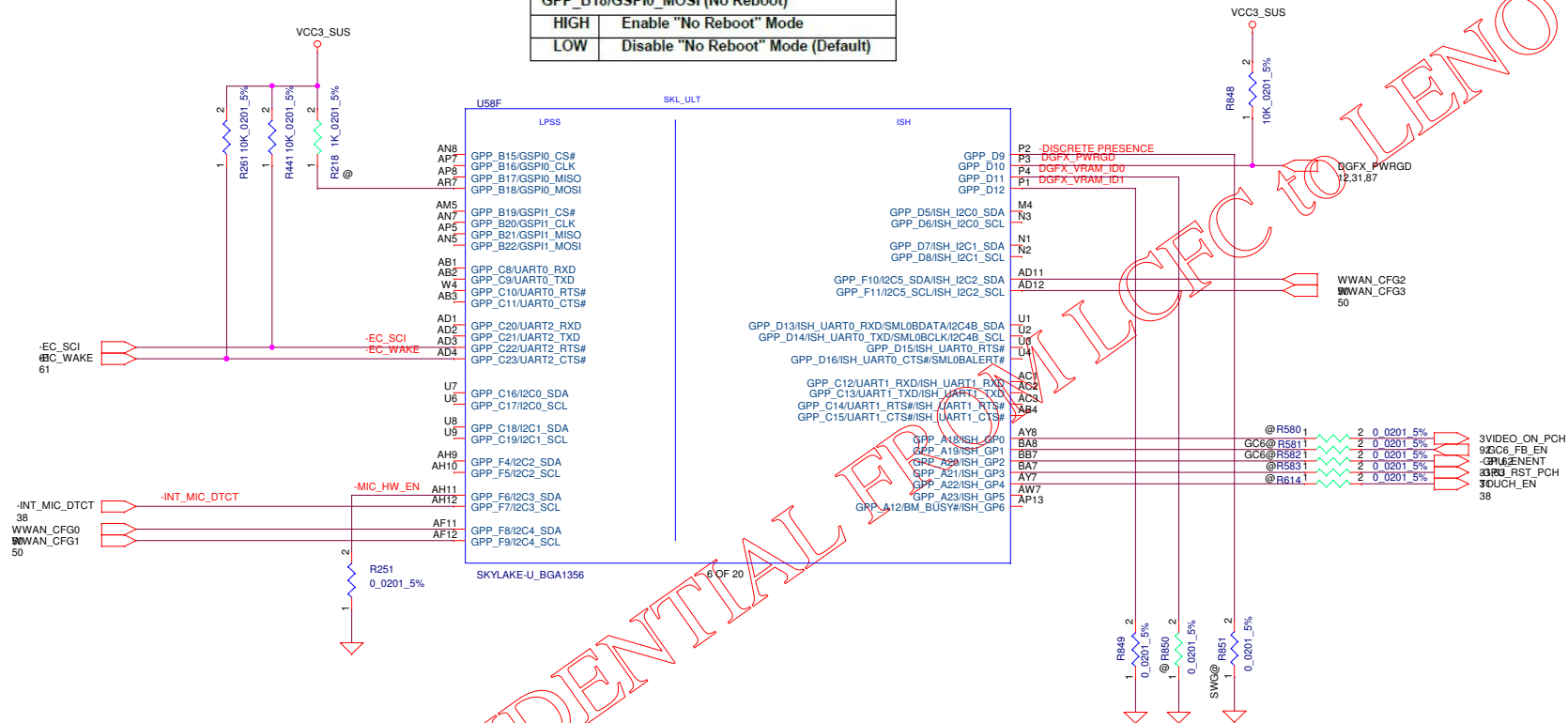
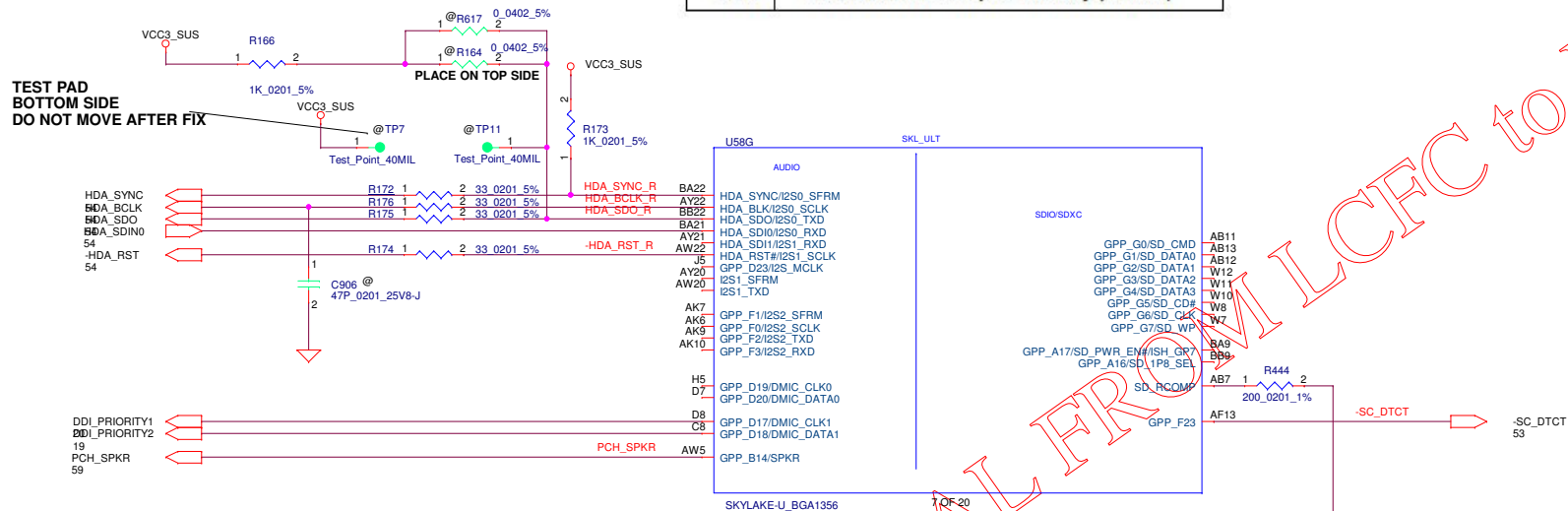


TABLE : Functional Strap

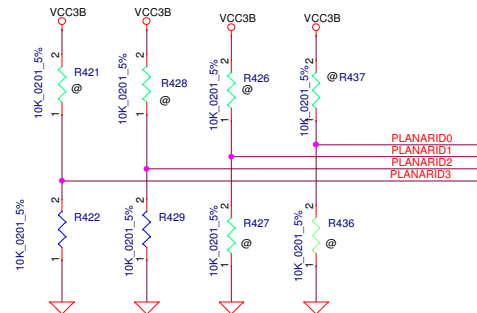
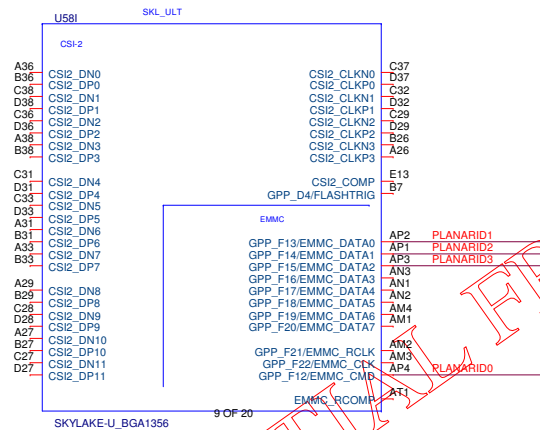
HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)



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		2015/08/10
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Title		LCFC	
CPU(7/16) : AUDIO/SDXC			
Size	Document Number	Rev	
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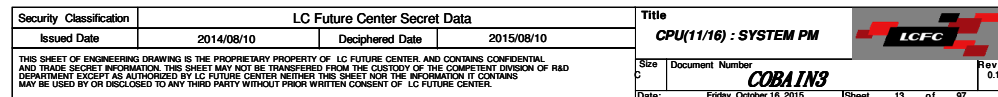
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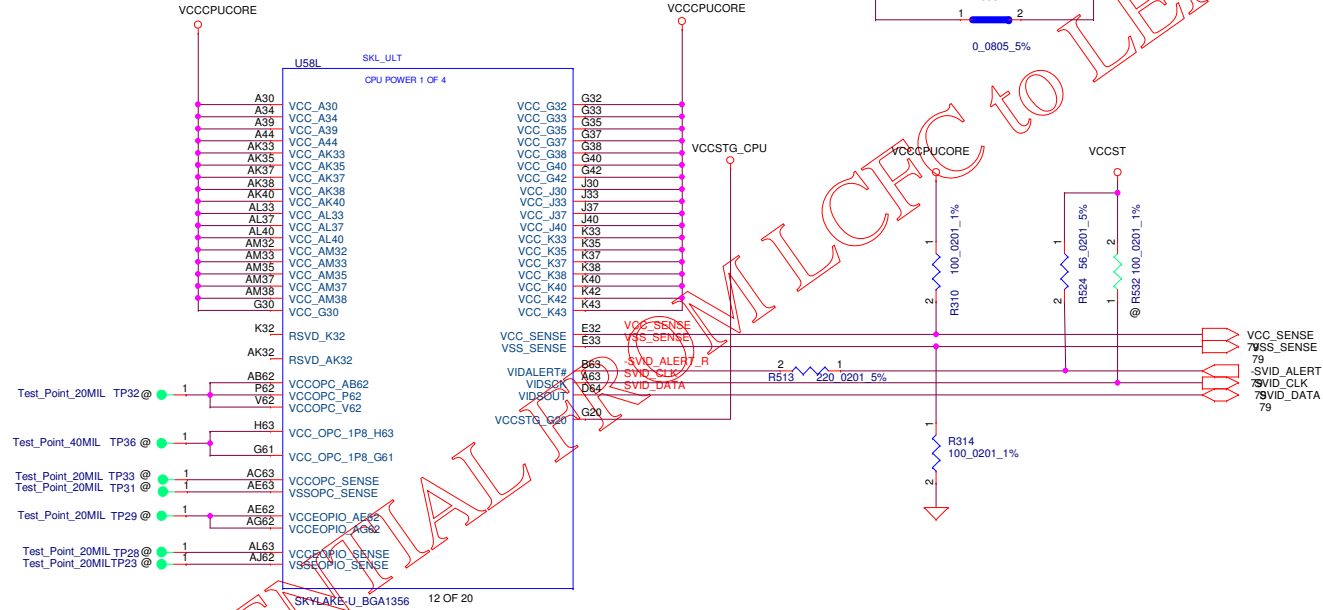
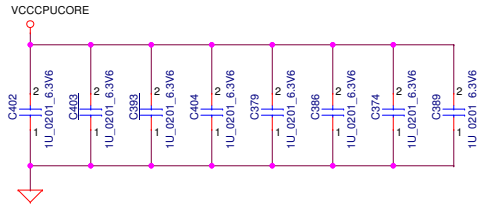


PLANAR ID TABLE		
LEVEL		PLANARID[3..0]
UMA	SWG	
SDV		0000B
FVT		0001B
SIT	FVT	0010B
SVT	SIT	0011B
	SVT	0100B

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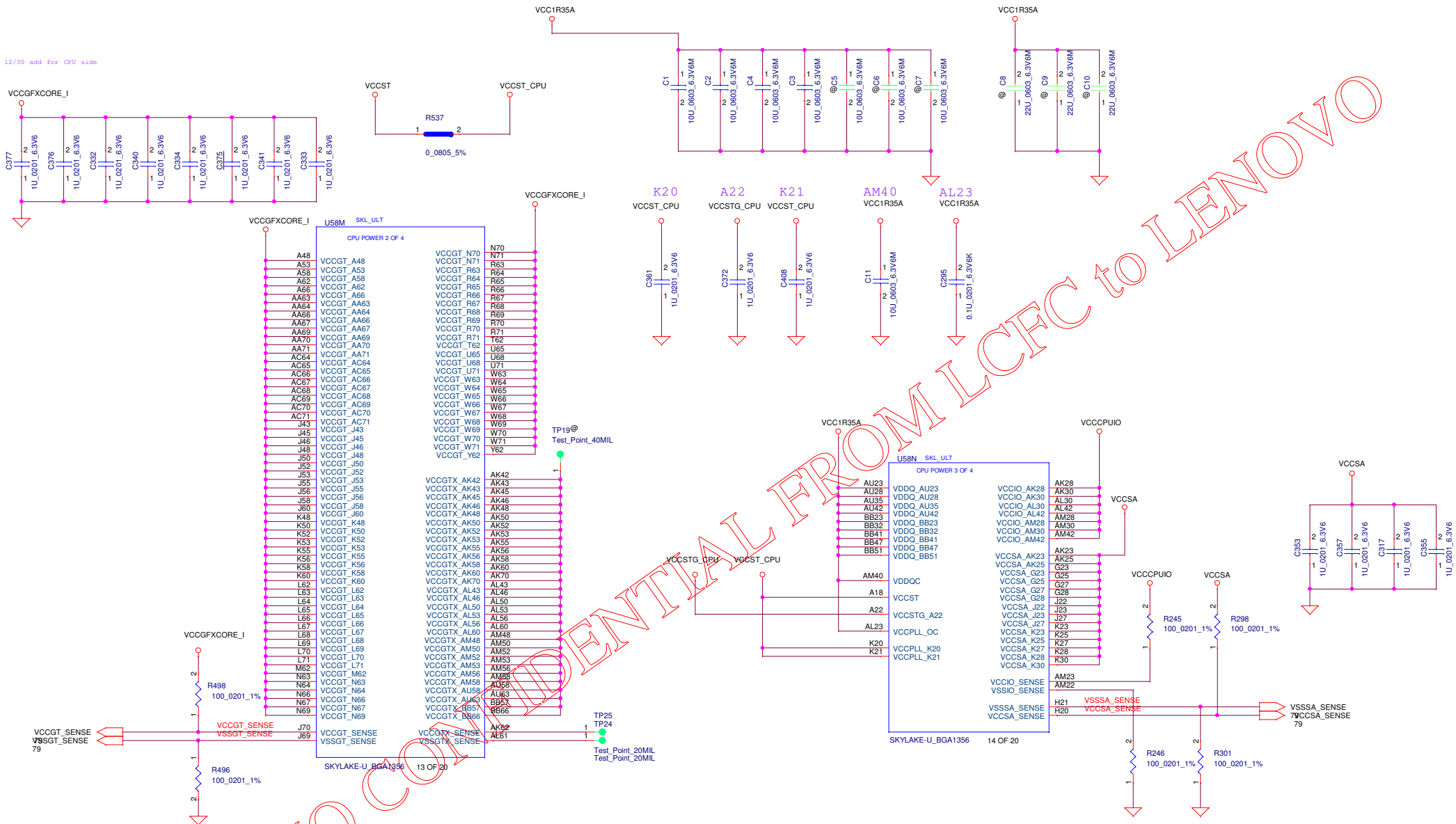
Title			
CPU(9/16) : CSI-2/EMMC			
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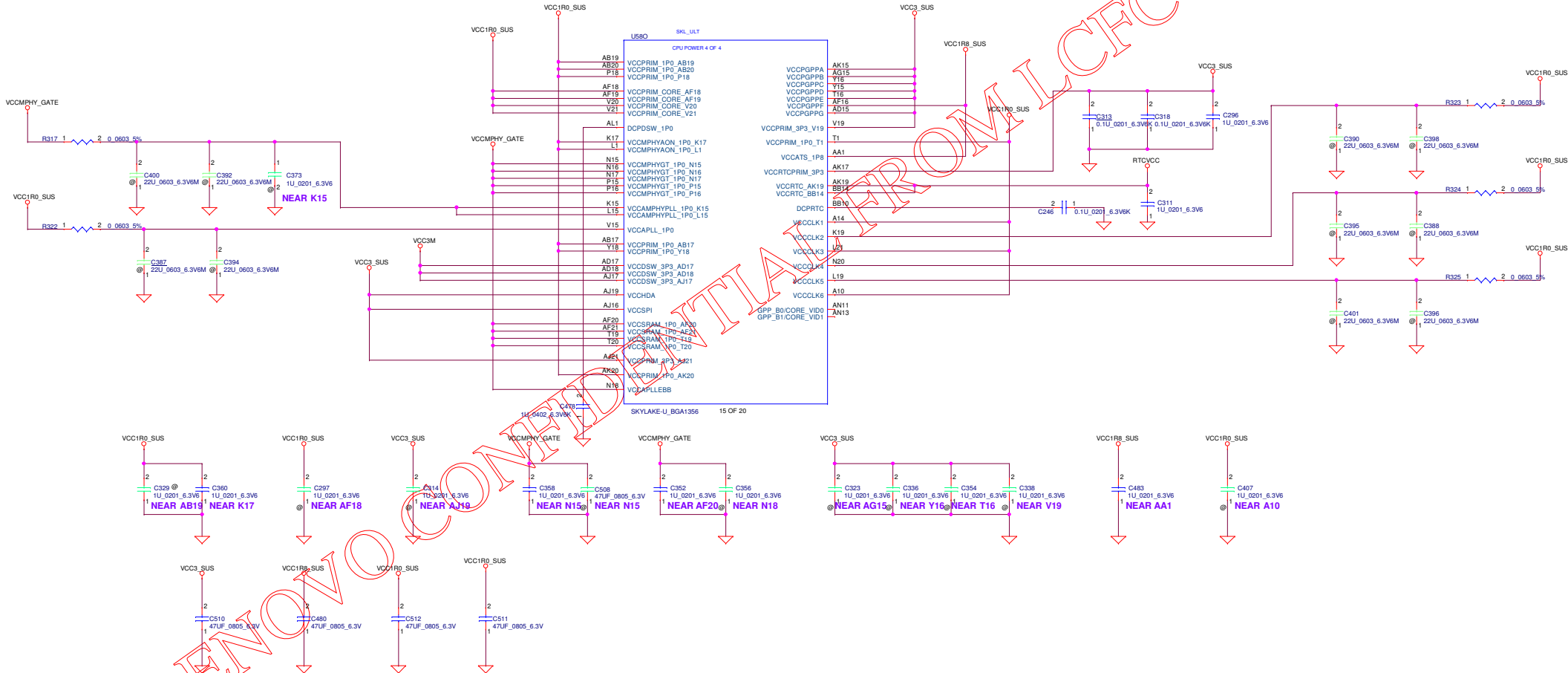
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12/30 add for CPU side

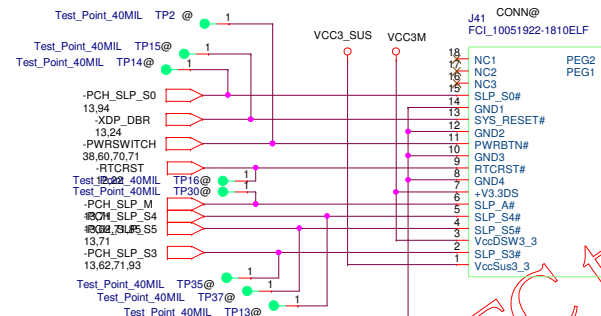
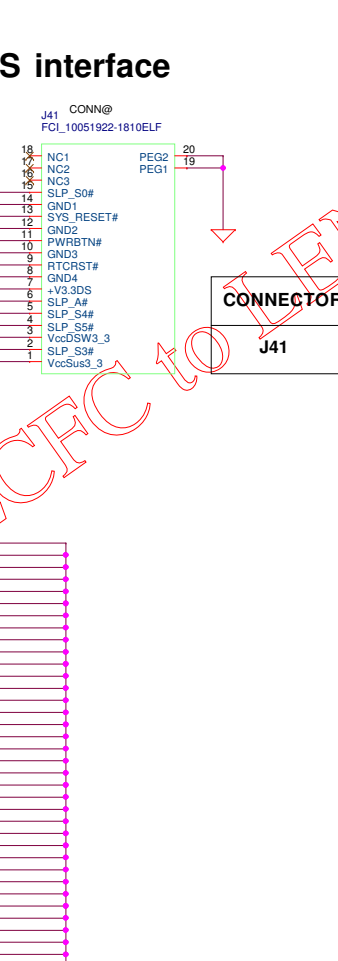
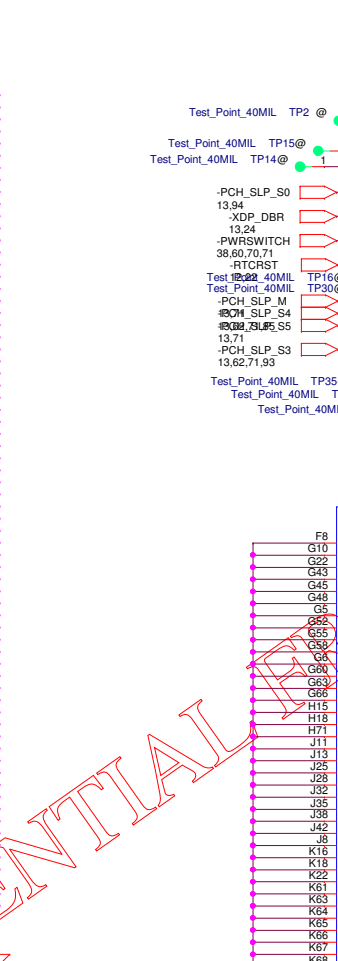
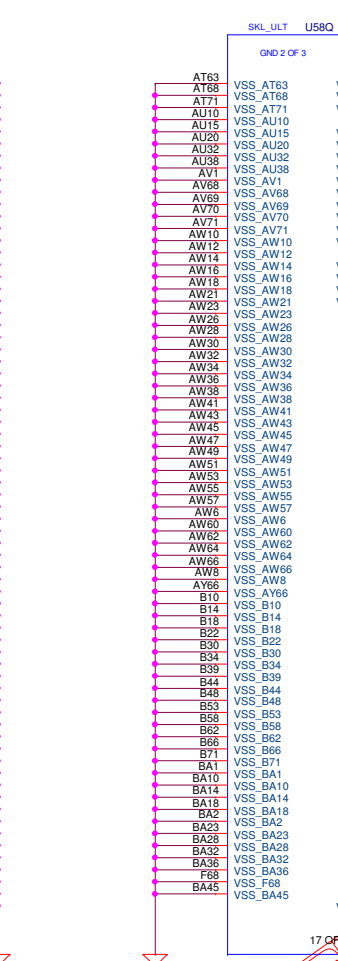


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Title		CPU(13/16) : CPU POWER		LCFC	
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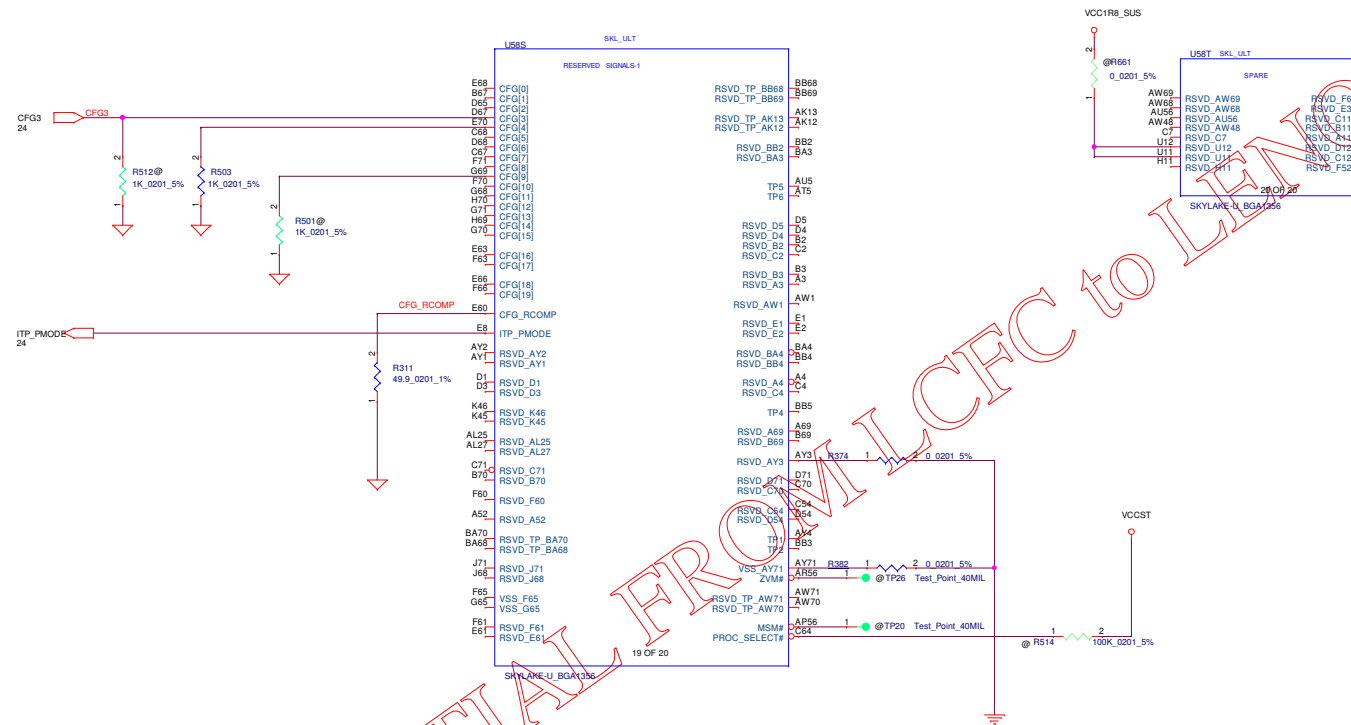


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				Date:	Friday, October 16, 2015	Sheet 16 of 97

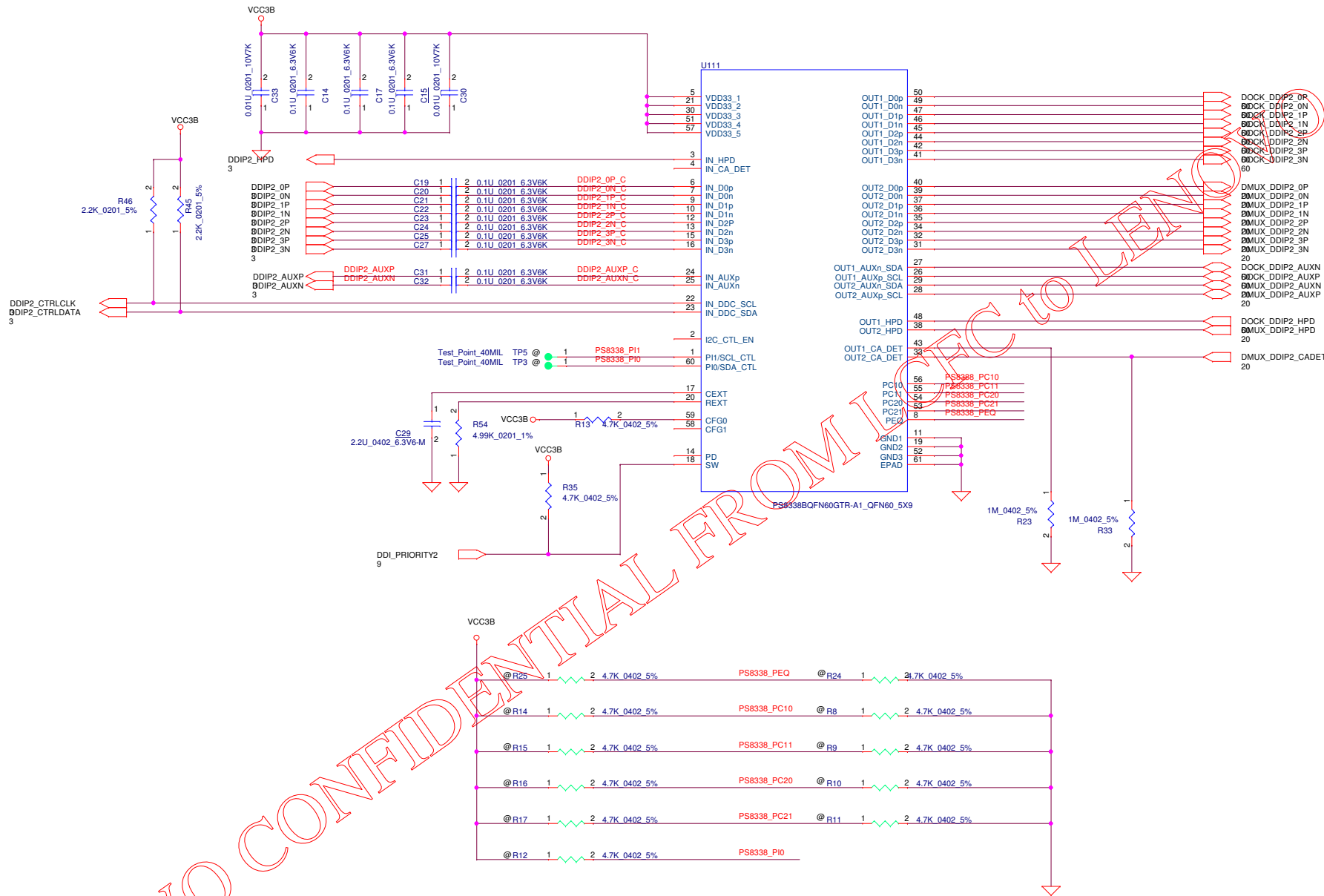


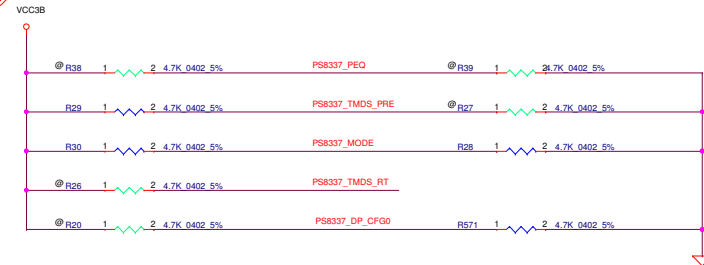
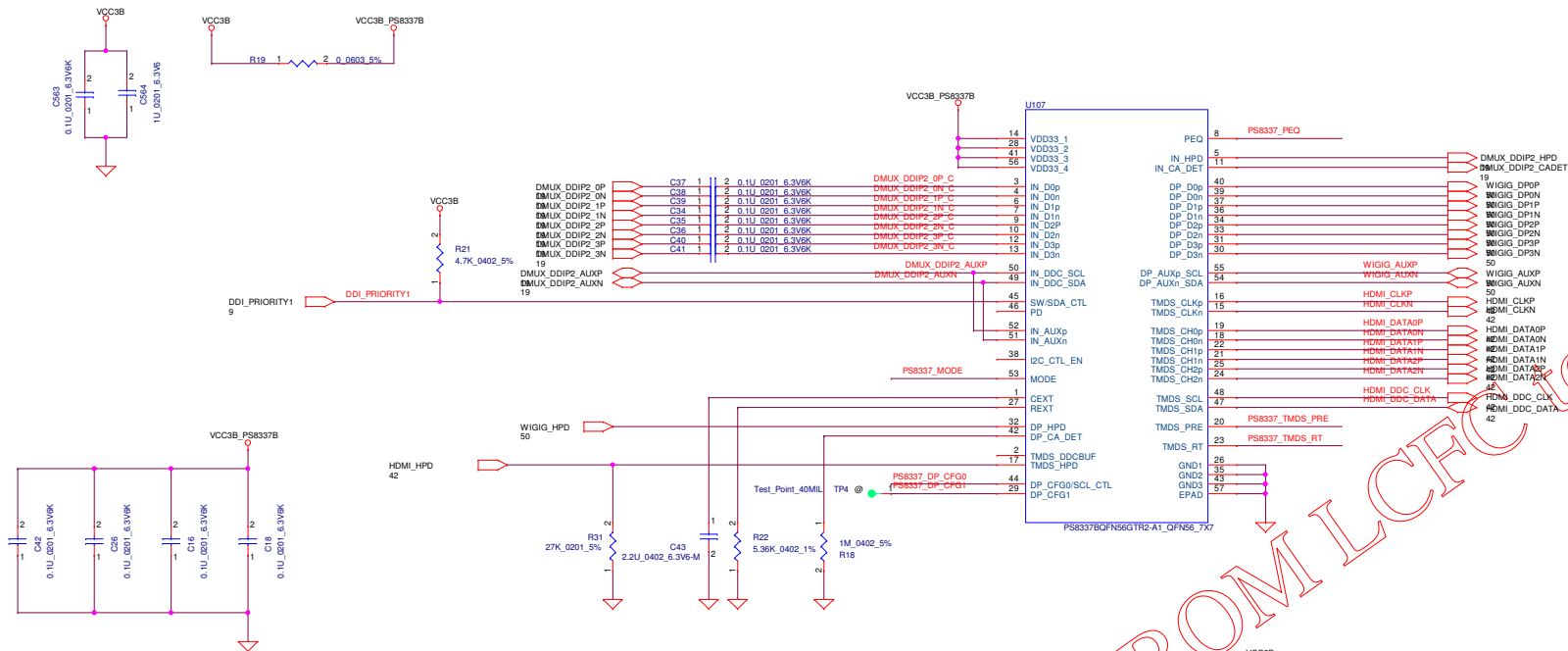
CONNECTOR	Planar Only	BOX
J41	ASM	NO ASM

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall
CFG4 : eDP Enable 1 : Disabled 0 : Enabled
CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled




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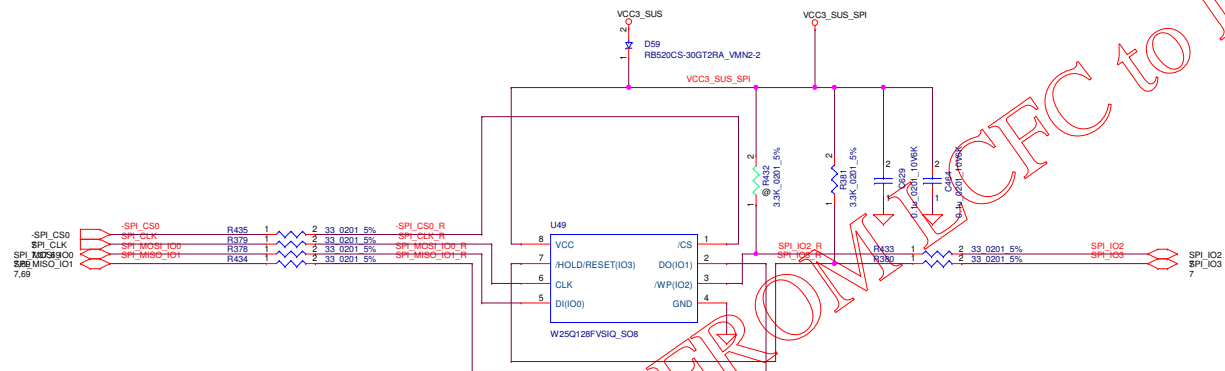




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TABLE

SPI ROM HEADER INTERFACE (TOP VIEW)					
1	VCC	D12.1	GND	GND	2
3	CS	R322.2	R681.2	CLK	4
5	MISO	R694.2	R674.2	MOSI	6
7	RESET	N/A	N/A	(RESET)	8

U49 SPI ROM

vPro/non-vPro Model (16MB)	
WINBOND	W25Q128FVSIQ
MACRONIX	MX25L12875FM2I-10G

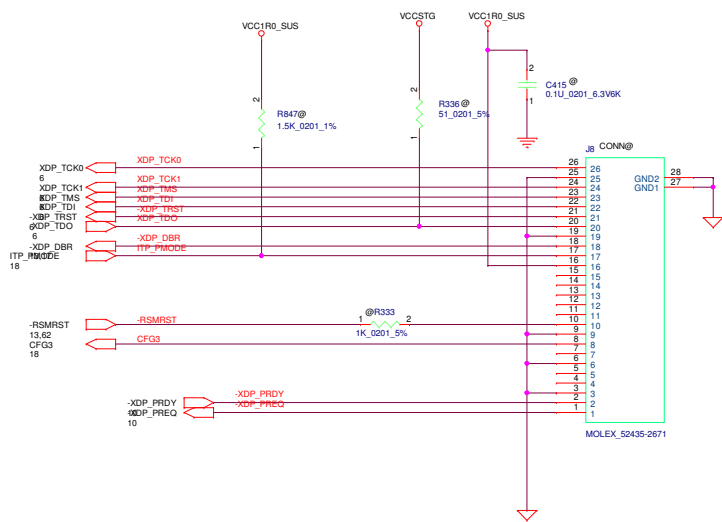
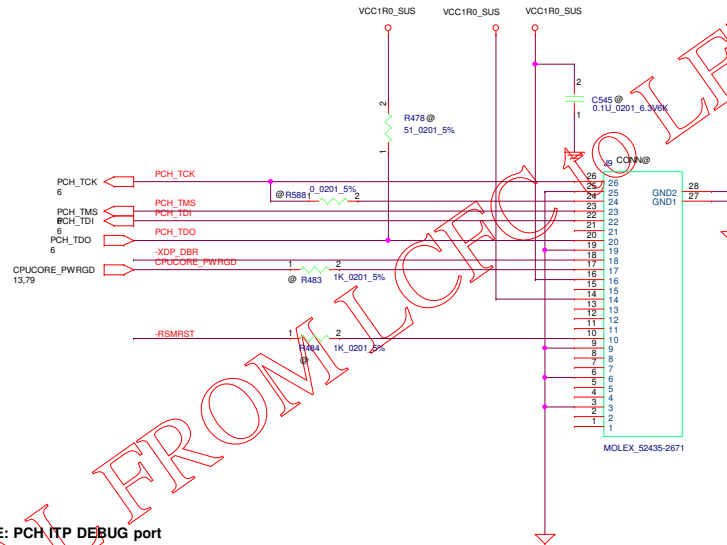
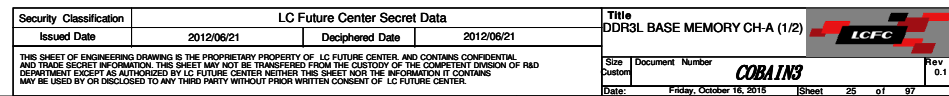


TABLE: PCH ITP DEBUG port

SIGNAL	REF DES	Planar only	BOX
TDO	R478 R523	ASM	ASM
TMS	R521	ASM	ASM
TDI	R535	ASM	ASM
TCK	R588 R538	ASM	ASM
CPUCORE_PWRGD	R483	ASM	ASM
-RSMRST	R484	ASM	ASM
CONNECTOR	J9	ASM	NO ASM


NOTE: APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV

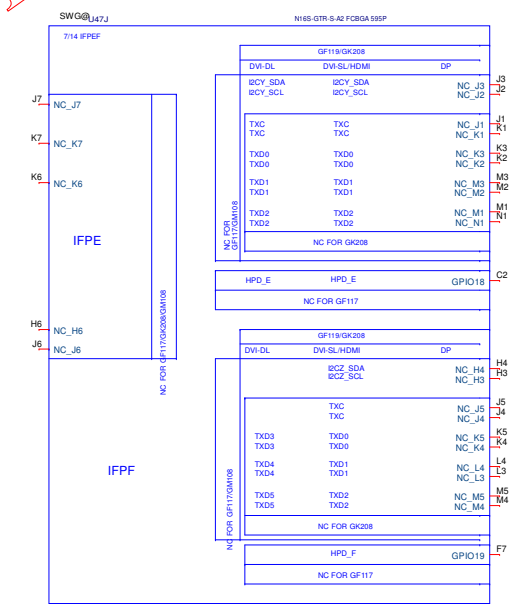
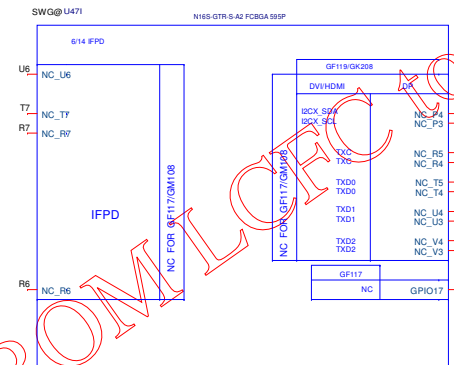
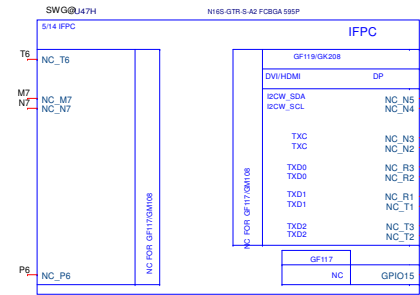
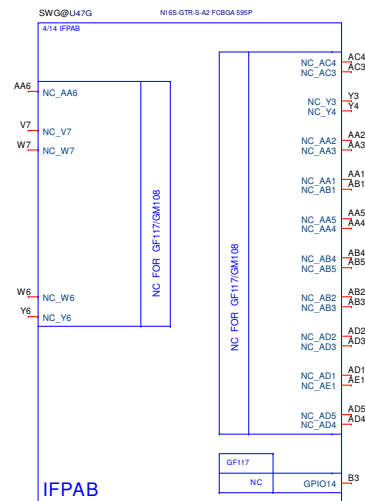


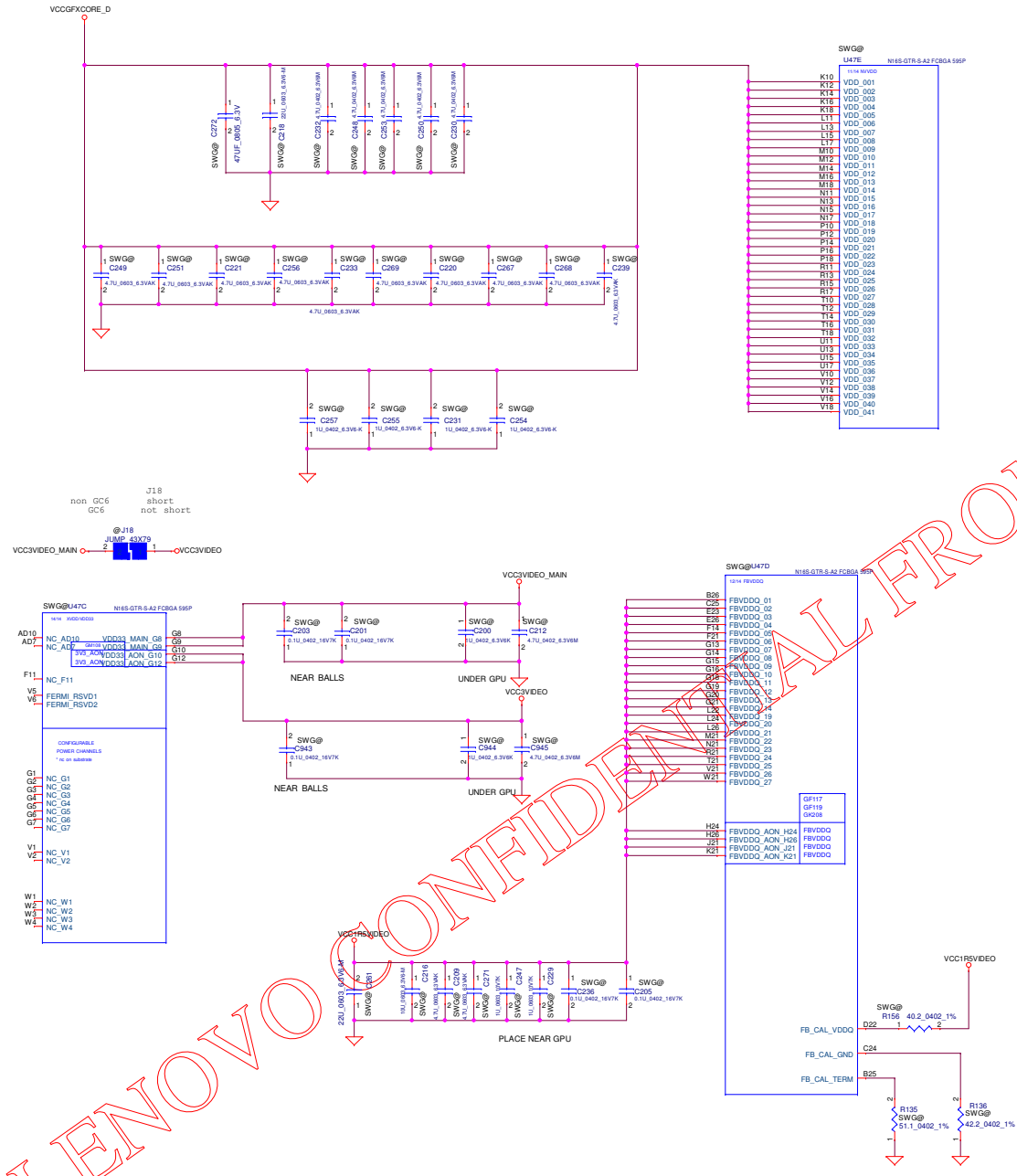


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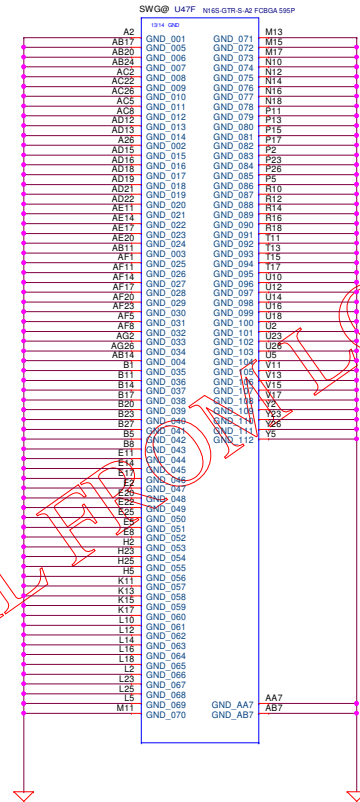


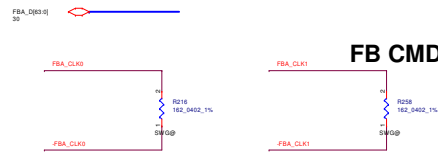


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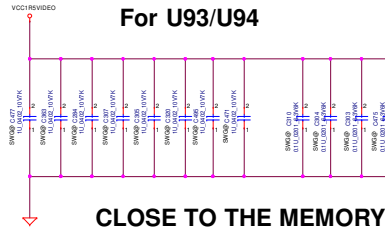
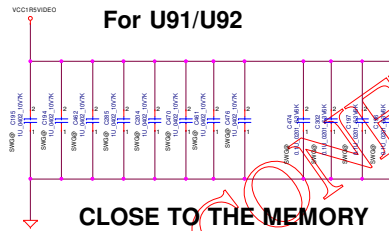
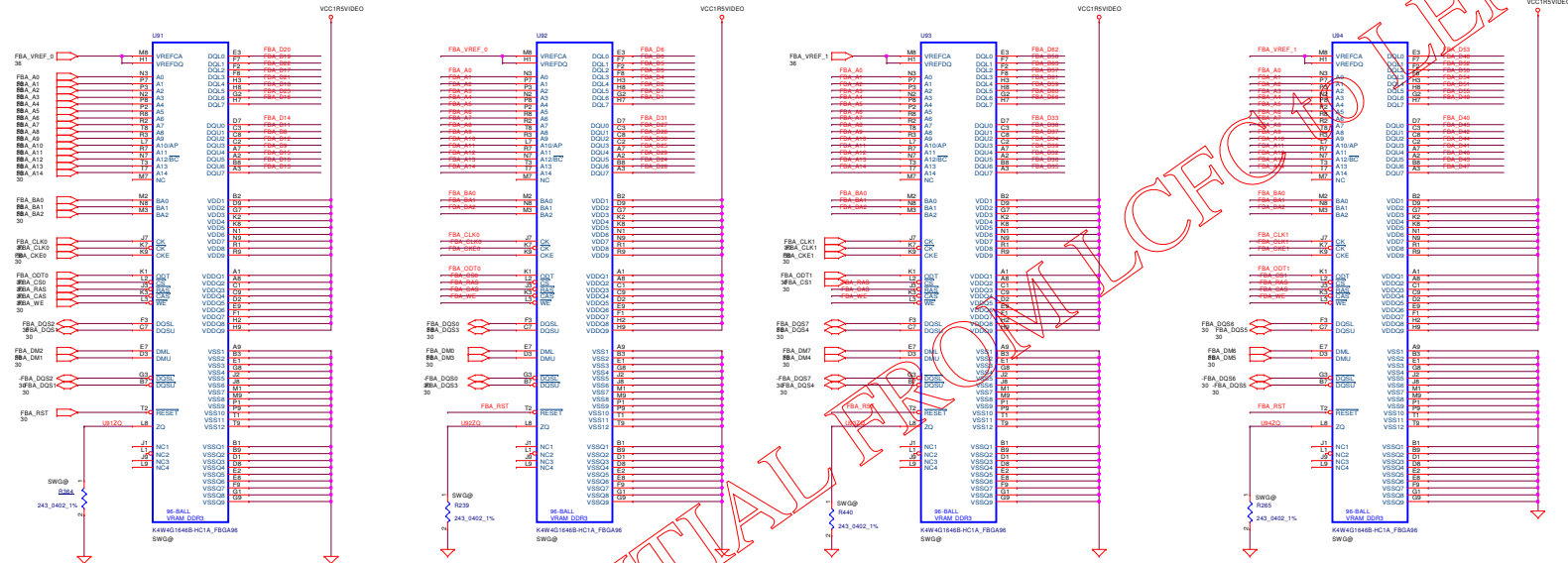




FB CMD mapping Mode D-N14x

TABLE D0R3 VIDEO MEMORY

	Micron 2GBITS (128Mx16)	HYNIX 2GBITS(128Mx16)	SAMSUNG 2GBITS(128Mx16)	SAMSUNG 4GBITS(256Mx16)	HYNIX 4GBITS(256Mx16)
U91 U92 U93 U94				K4W4G1646E-BC1A	H5TC4G63CFR-N0C
BOM Structure				S2G@	H2G@

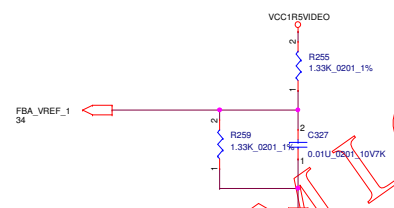
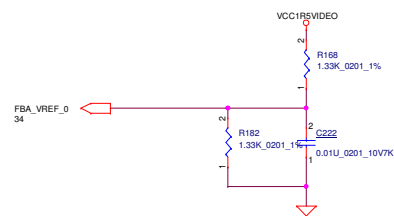


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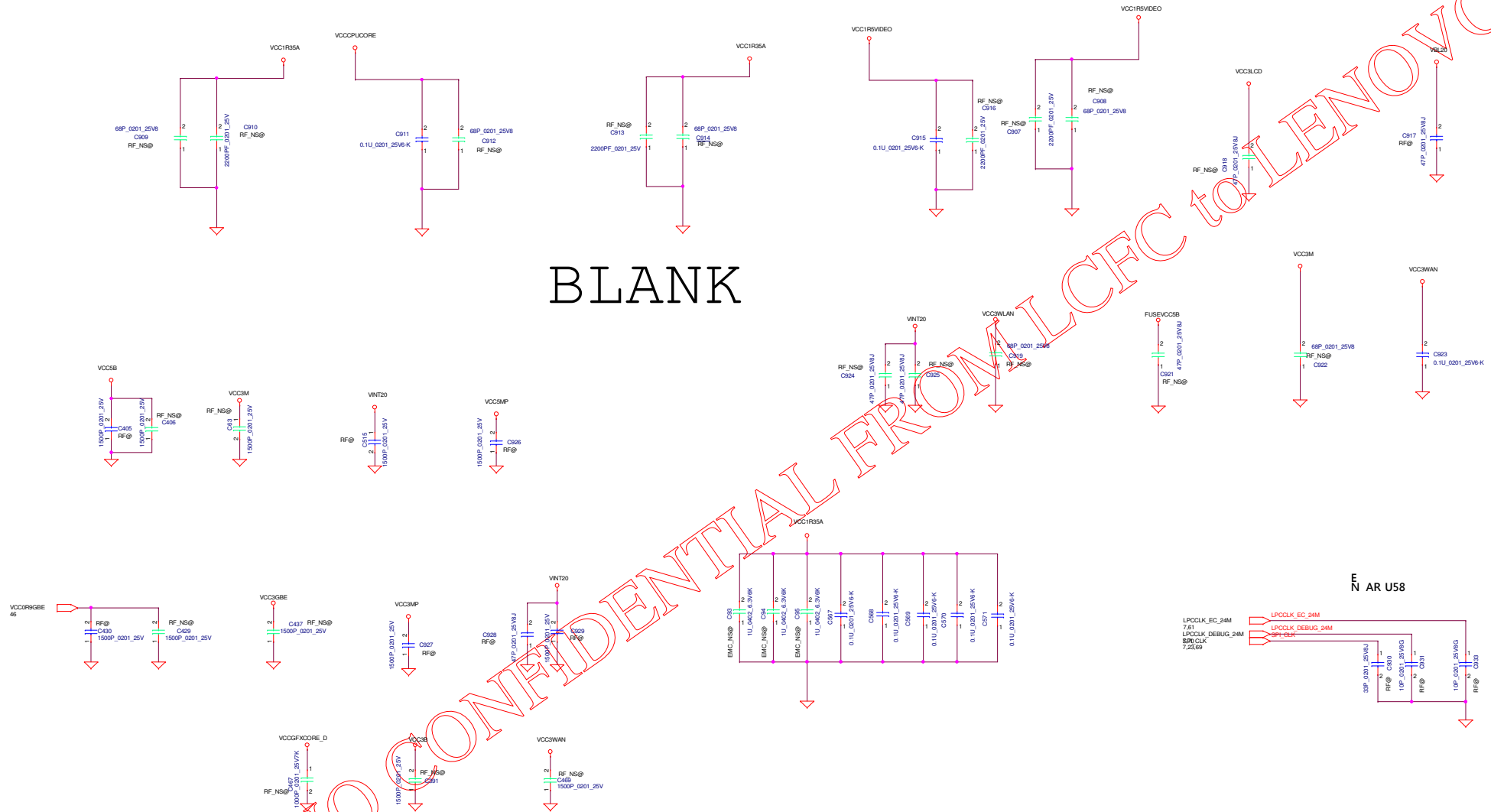
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				Sheet	37	of 67

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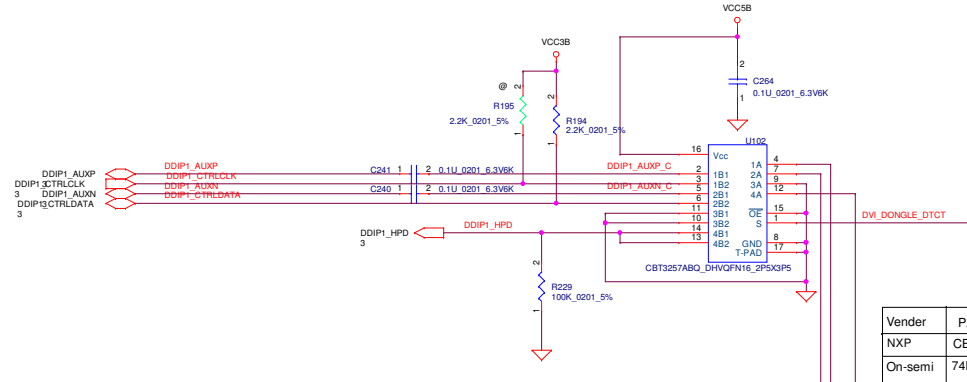
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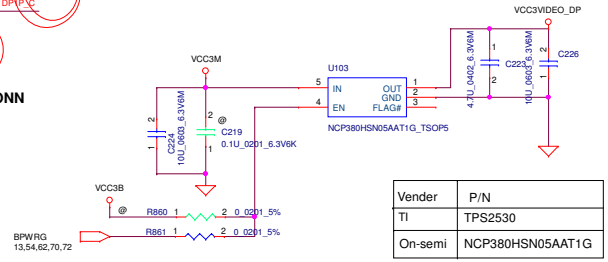
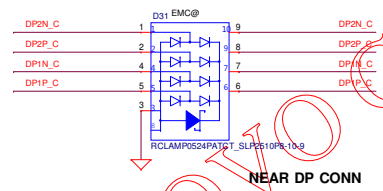
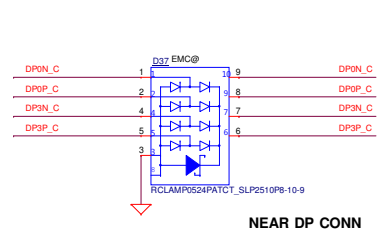
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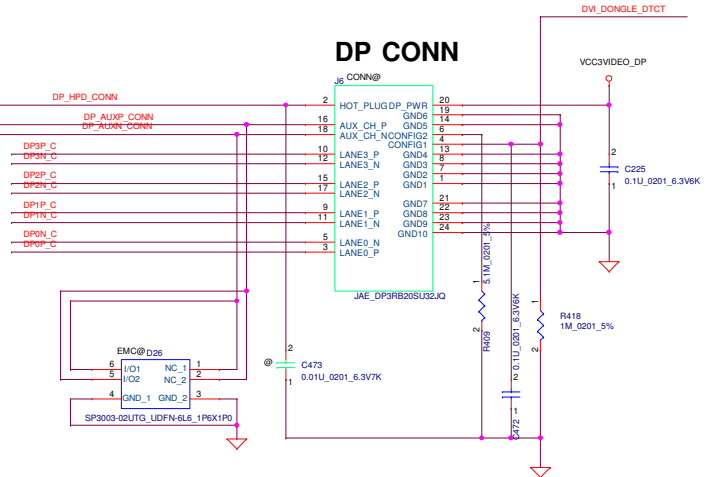


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NXP	CBT3257ABQ
On-semi	74FST3257MNTWG



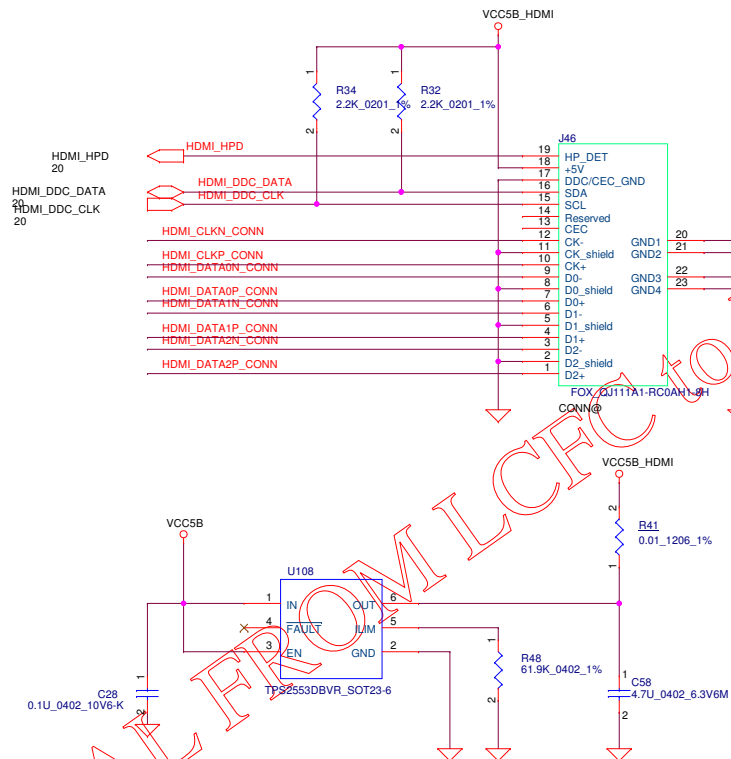
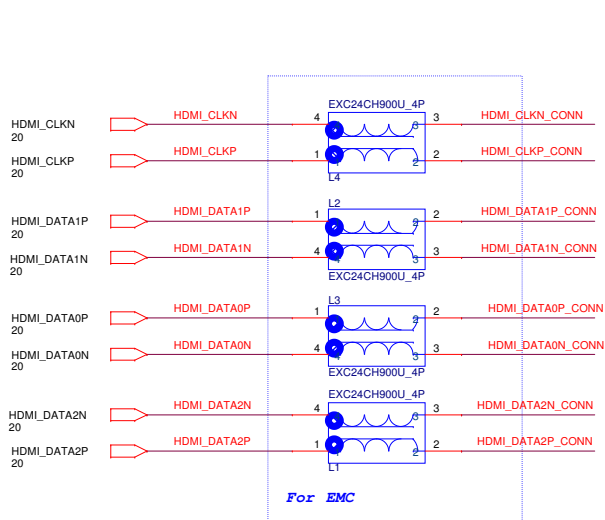
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TI	TPS2530
On-semi	NCP380HSN05AAT1G

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DDIP1_3P	C319 1	2	0.1U 0201 6.3V6K	DP3P_C
DDIP1_2N	C263 1	2	0.1U 0201 6.3V6K	DP2N_C
DDIP1_2P	C265 1	2	0.1U 0201 6.3V6K	DP2P_C
DDIP1_1N	C266 1	2	0.1U 0201 6.3V6K	DP1N_C
DDIP1_1P	C276 1	2	0.1U 0201 6.3V6K	DP1P_C
DDIP1_0N	C280 1	2	0.1U 0201 6.3V6K	DP0N_C
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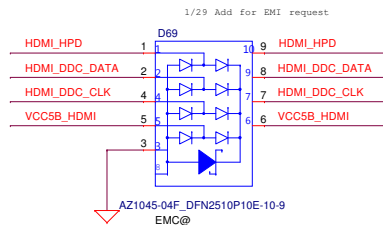
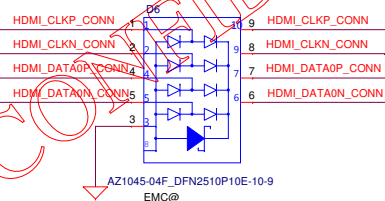
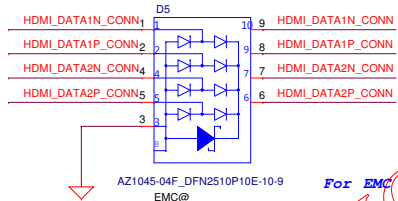



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Close to J46



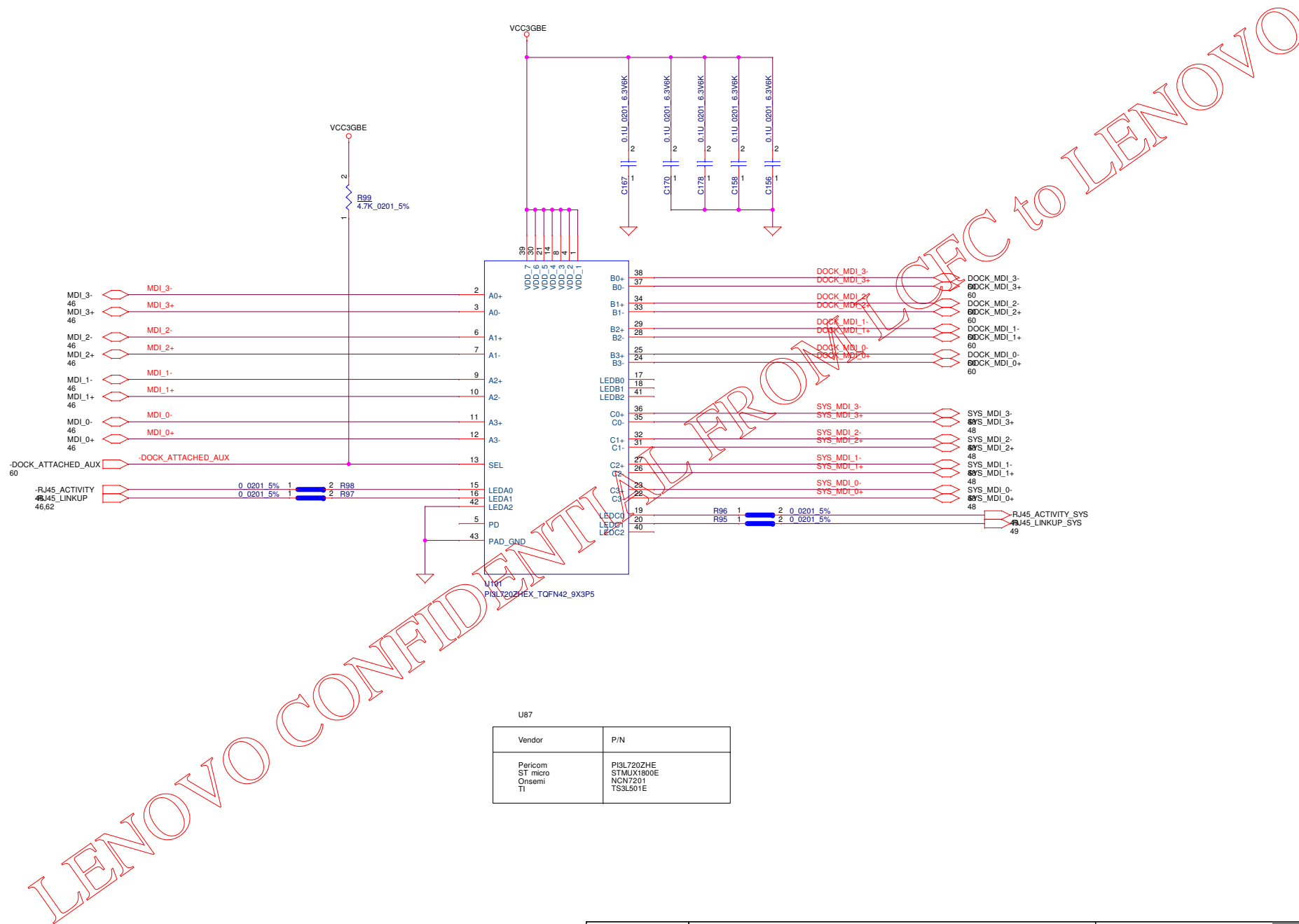
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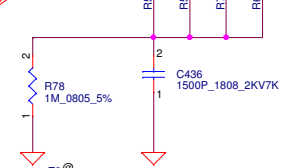
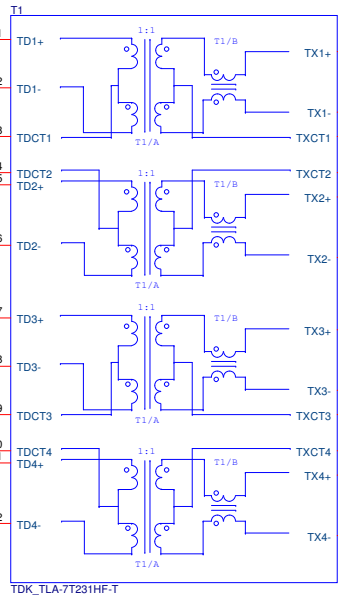
U87	
Vendor	P/N
Pericom ST micro Onsemi TI	PI3L720ZHE STMUX1800E NCH7201 TS3L501E

THE WIDTH OF THESE TRACE SHOULD BE WIDER THAN 35MIL TO PREVENT VOLTAGE DROP.

C303 SHOULD BE PLACED AS CLOSE TO MAGNETICS AS POSSIBLE.

ESD REASON

Vendor	P/N
TDK	TLA-7T231HF-T
Timag	IH-115-F
Bothand	NA69LF

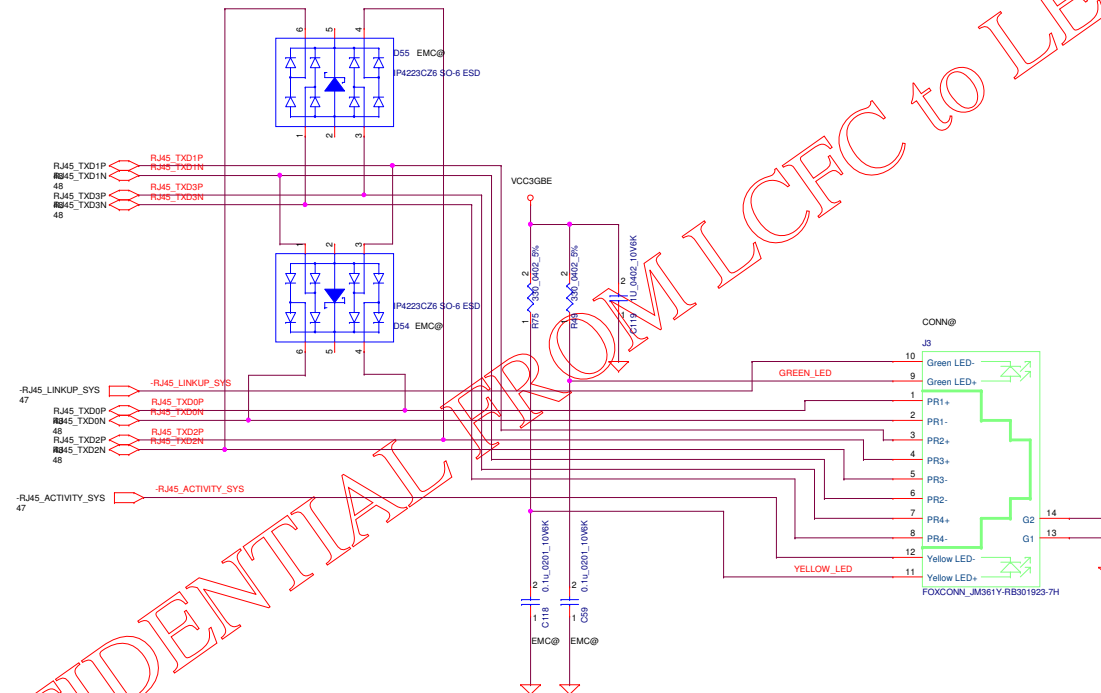



PATTERN MUST BE SHORT AND WIDE.
HIGH VOLTAGE 1500PF CAP IS OPTIONAL

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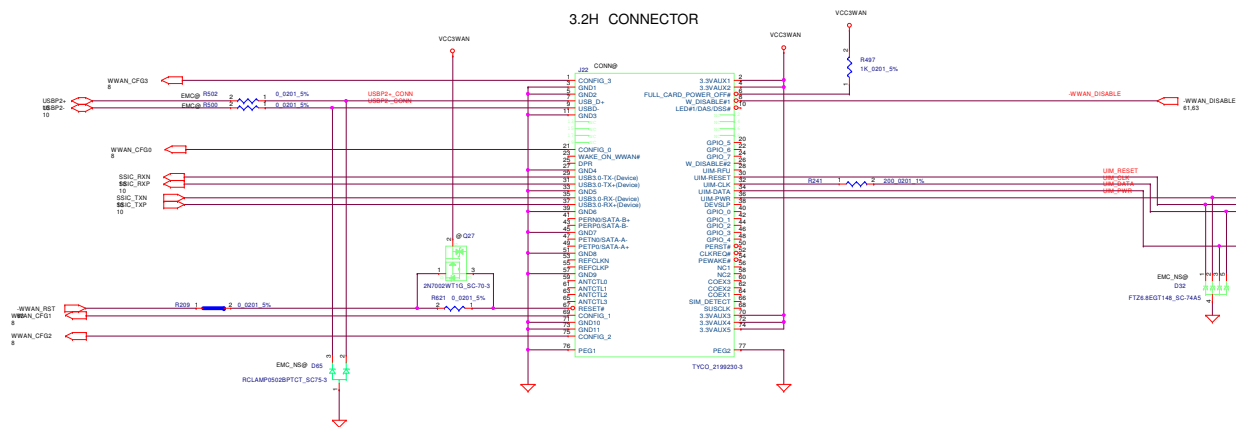
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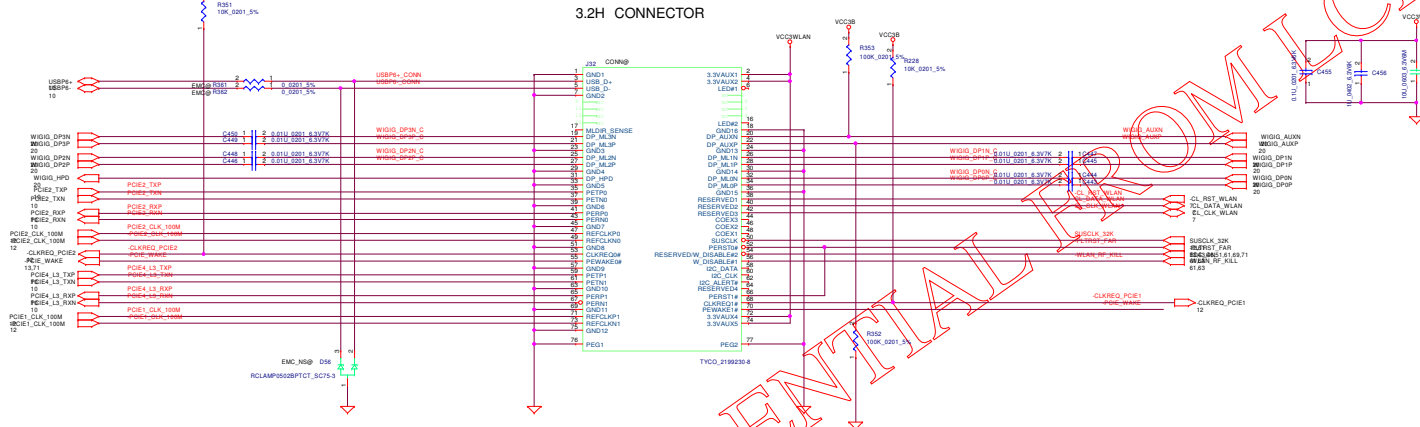


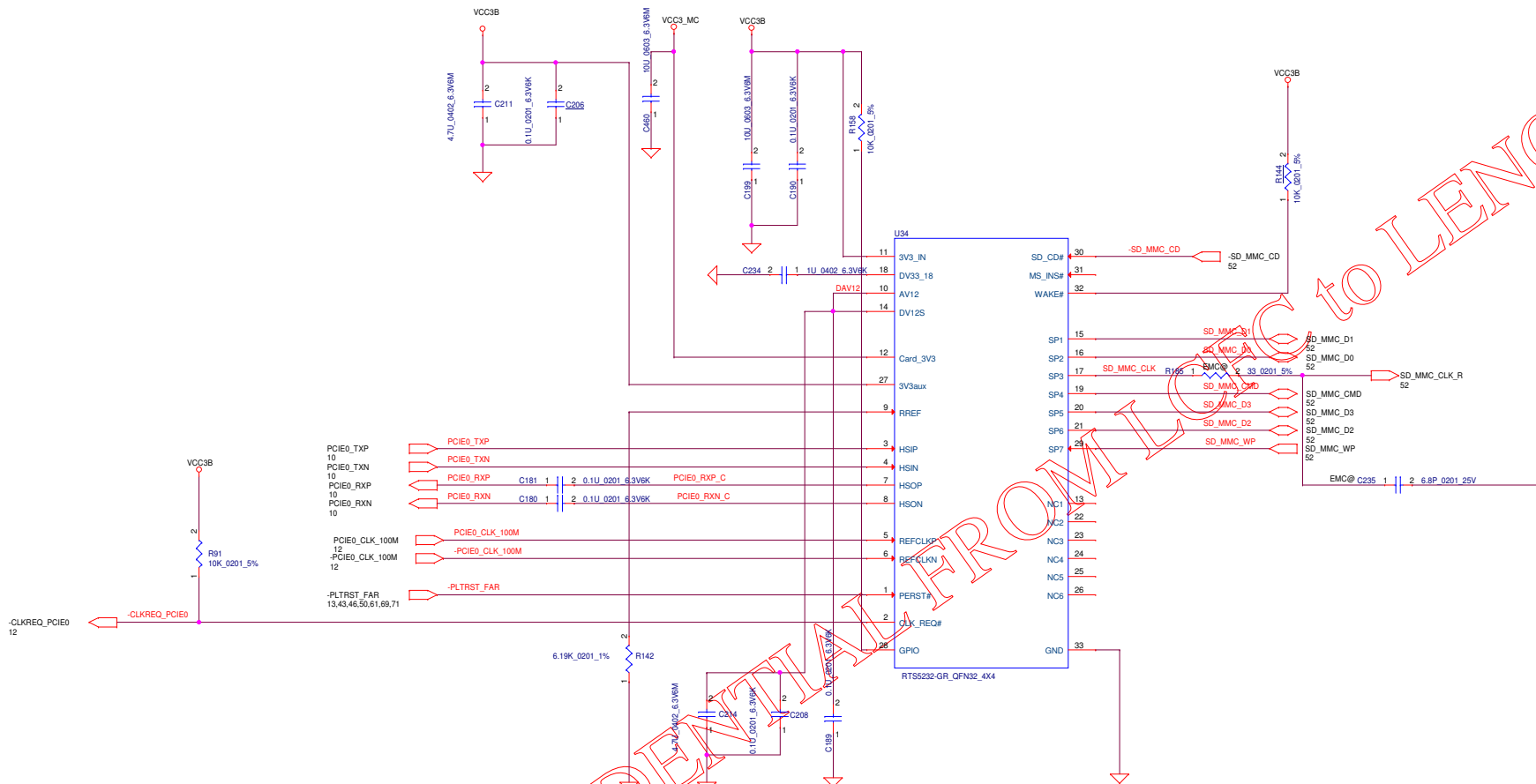
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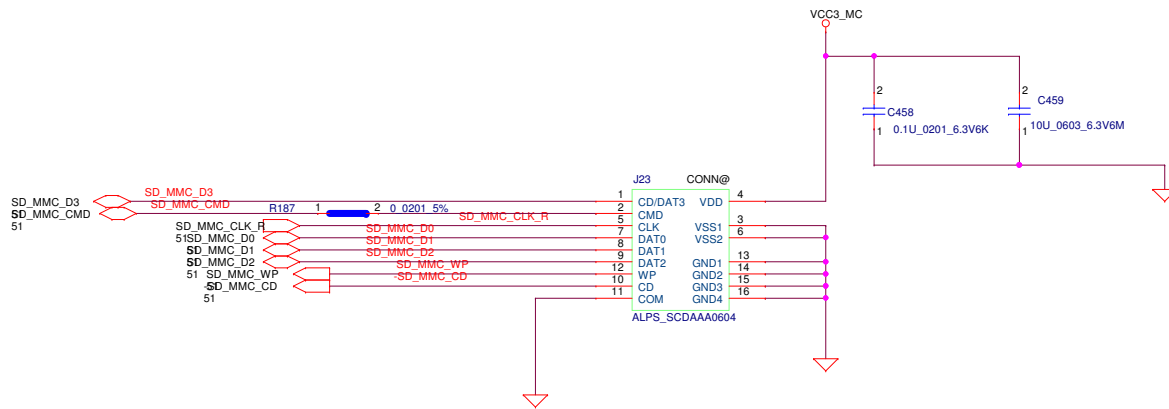
3.2H CONNECTOR




3.2H CONNECTOR



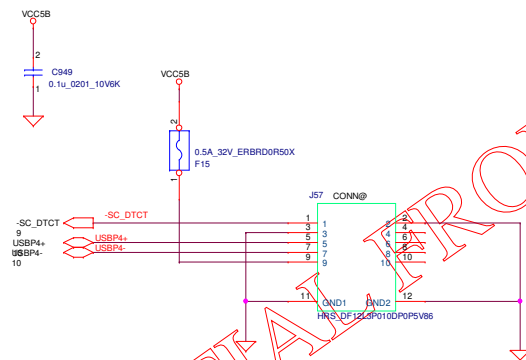




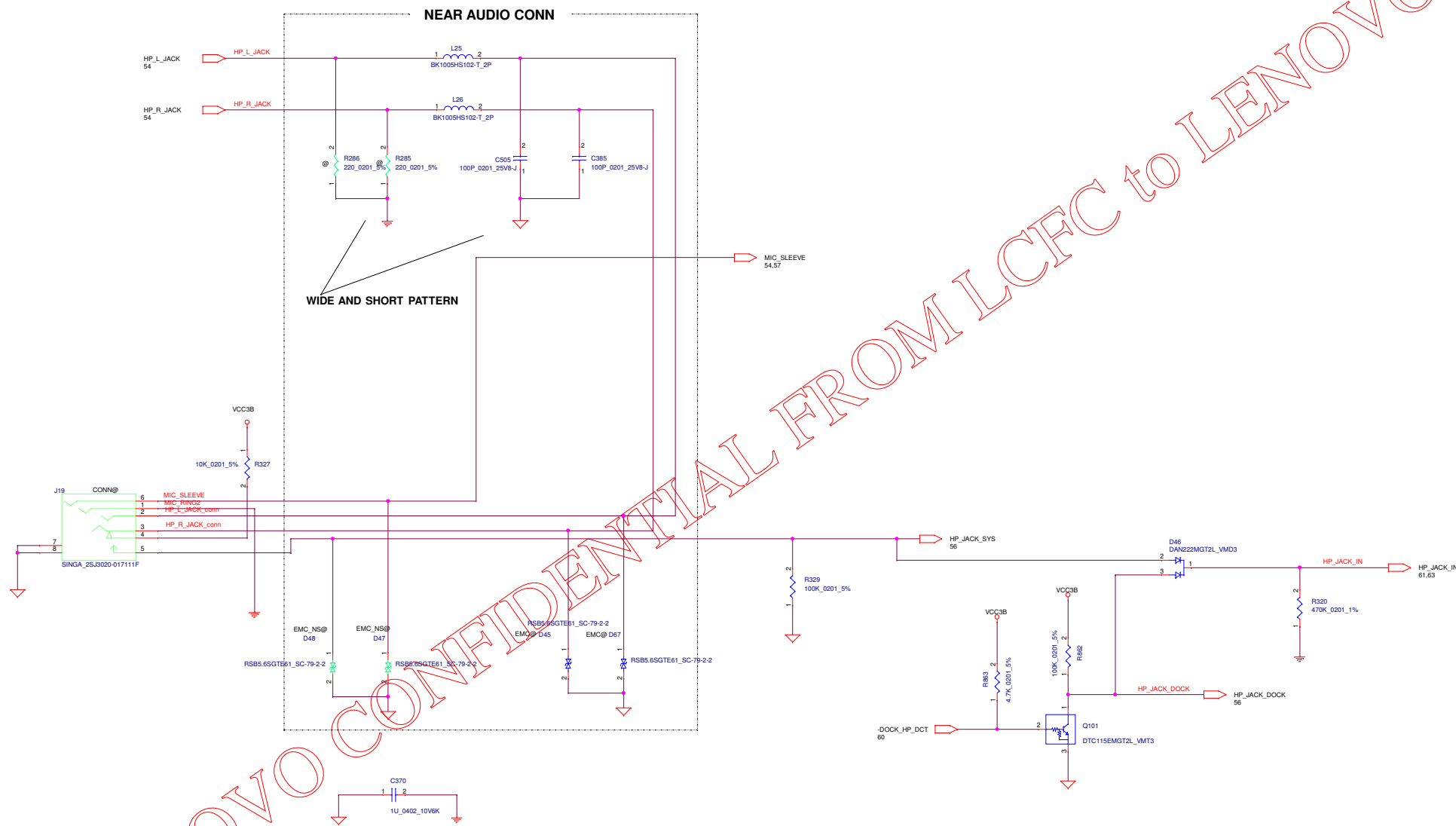
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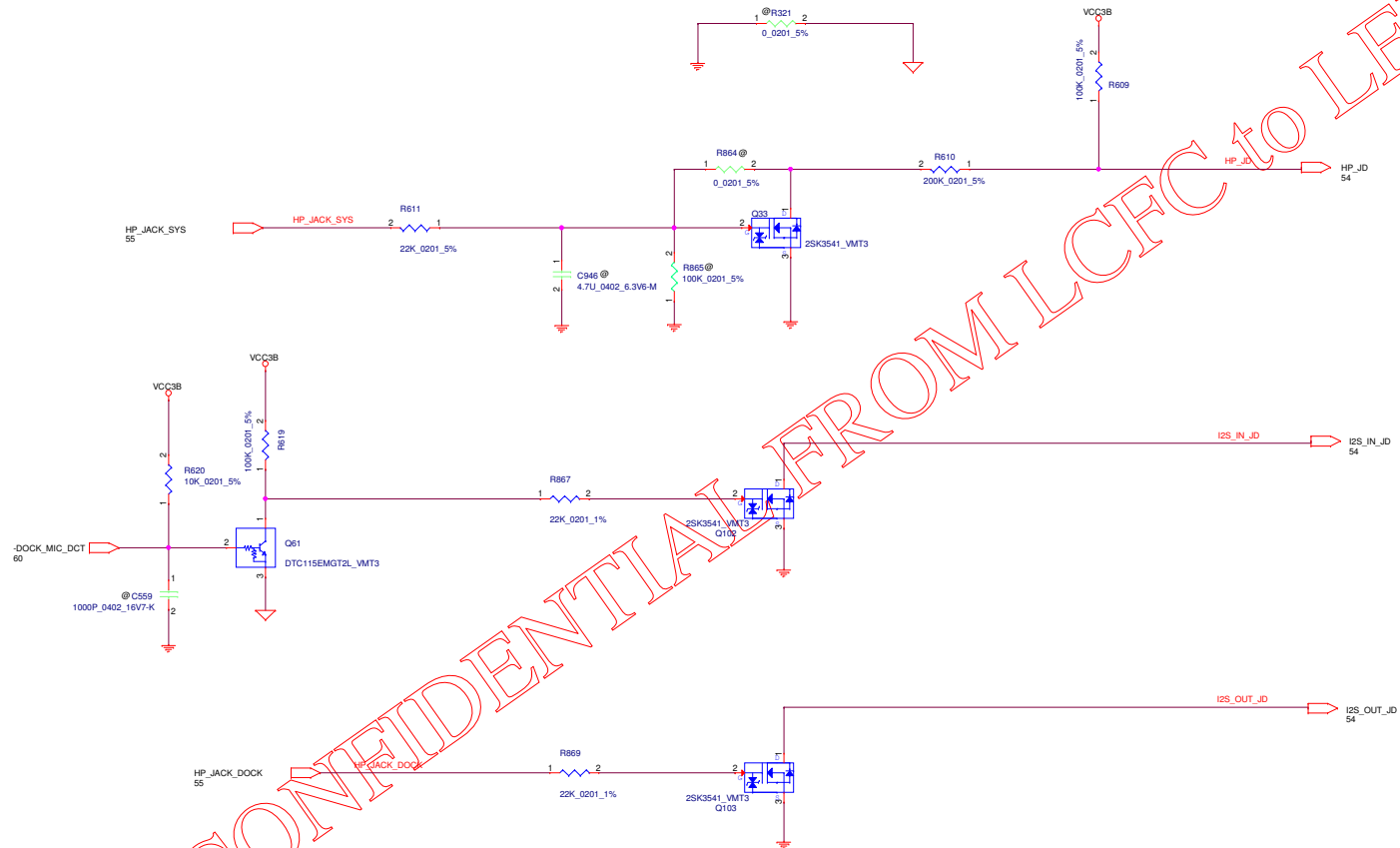


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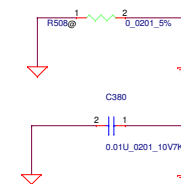



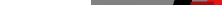
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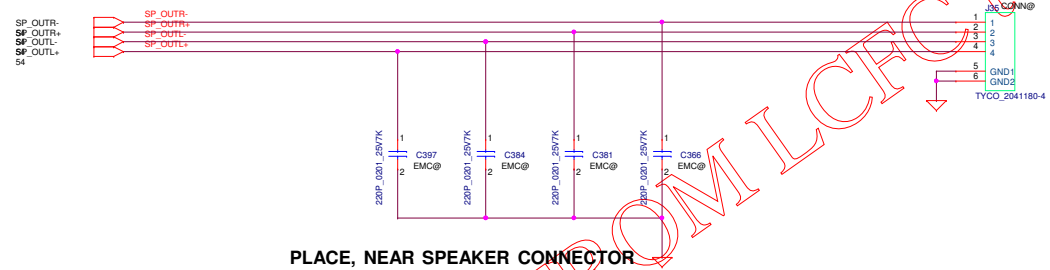


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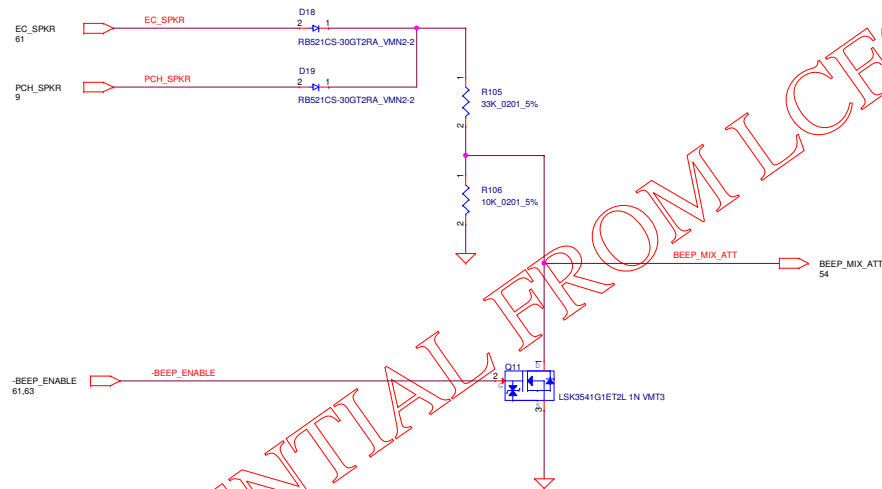
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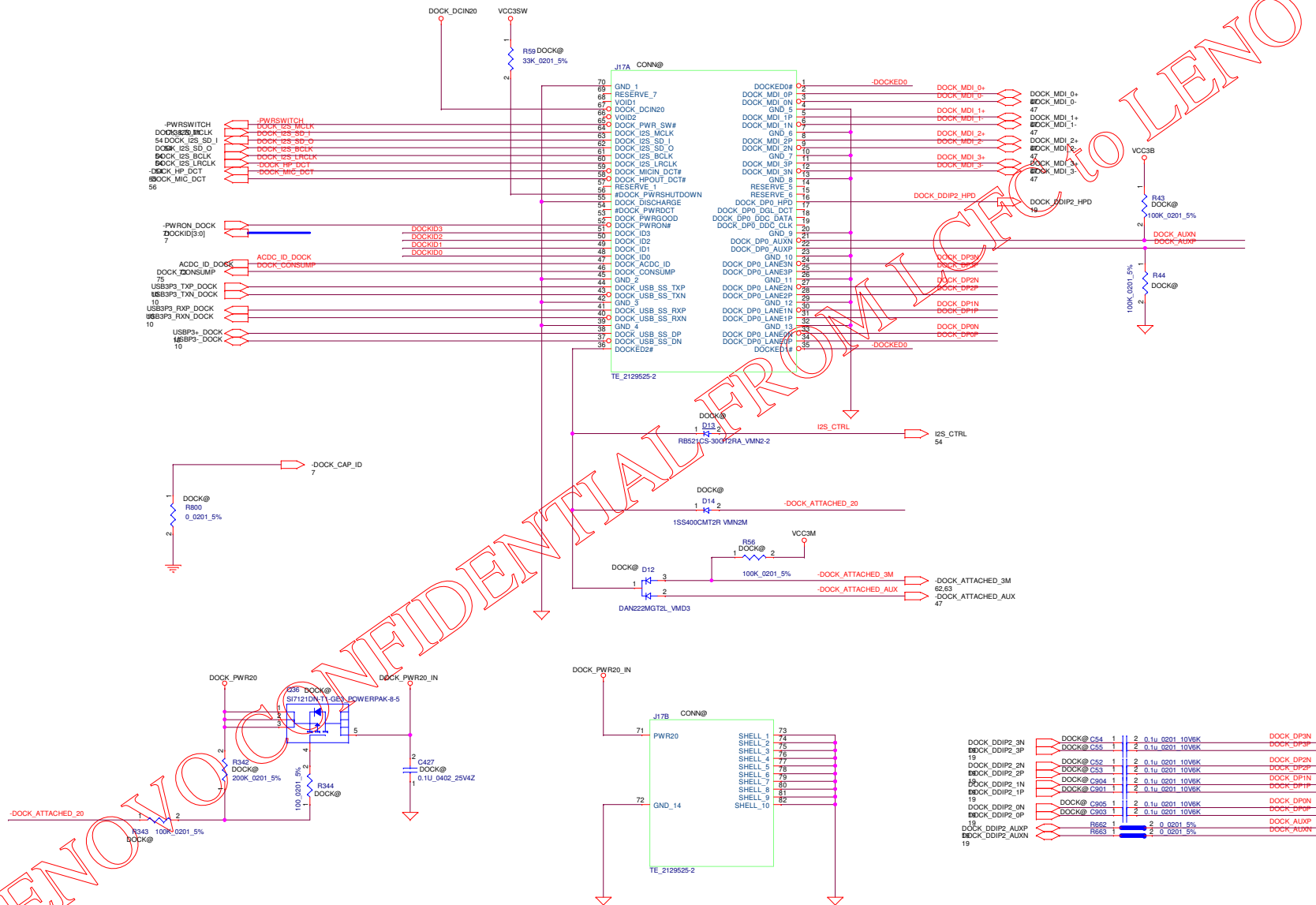


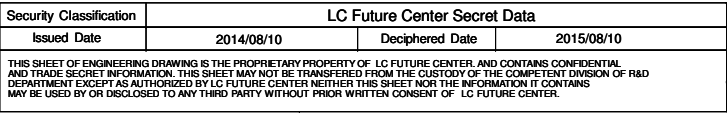
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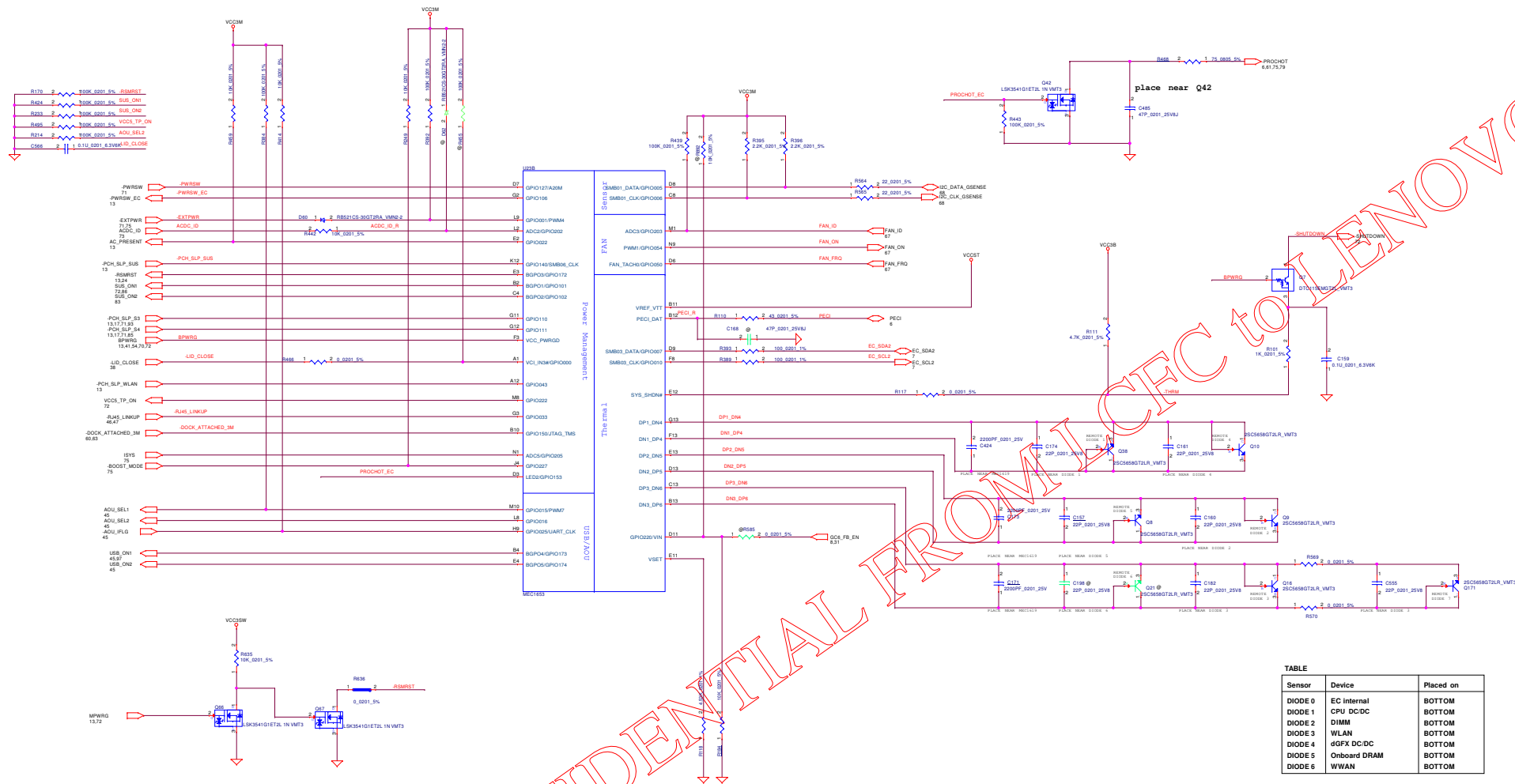
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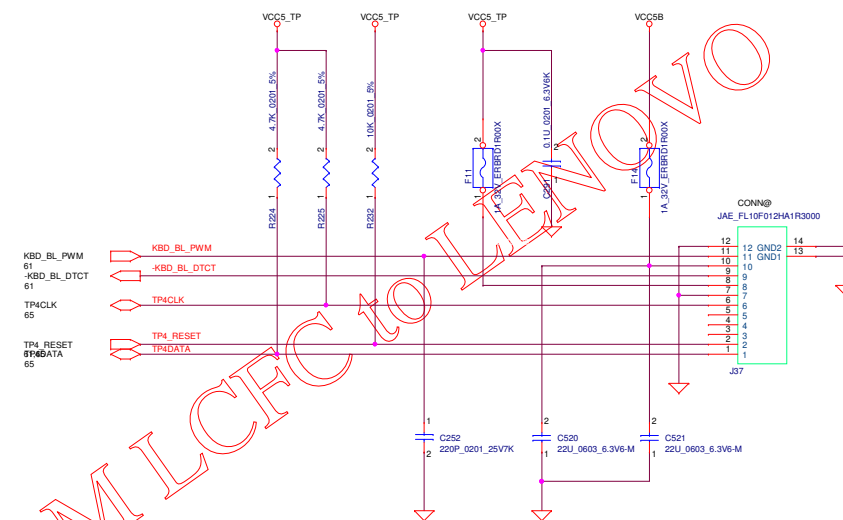
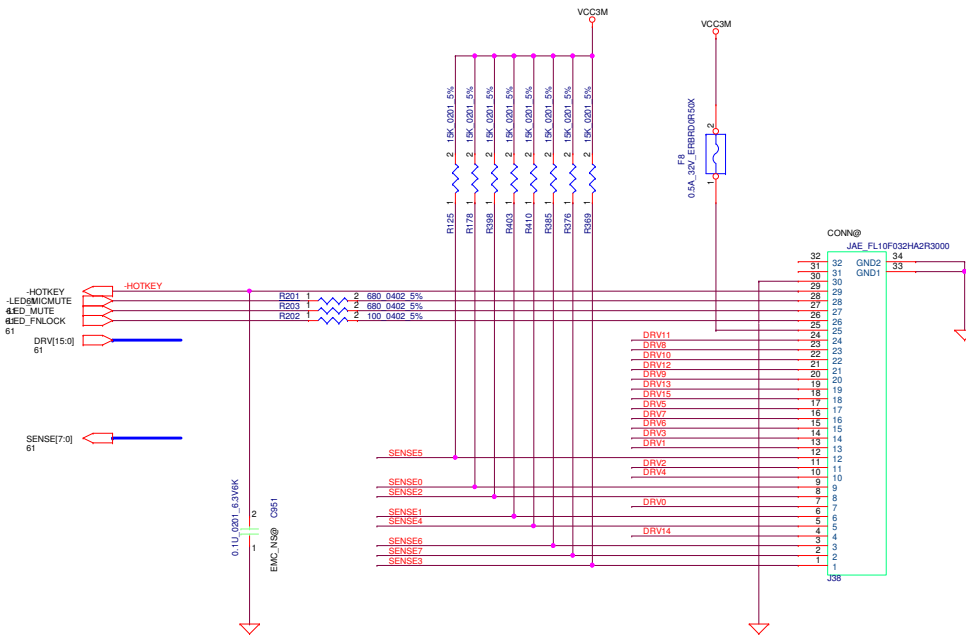




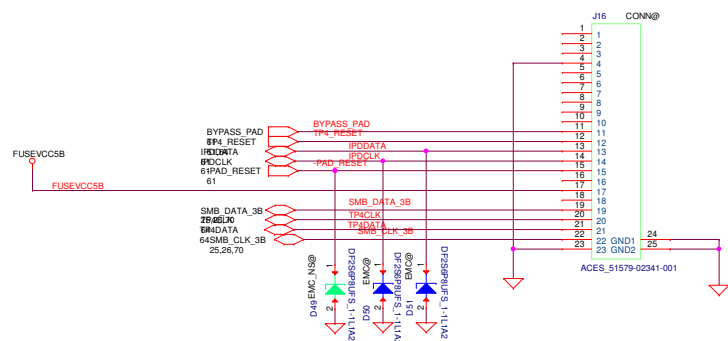
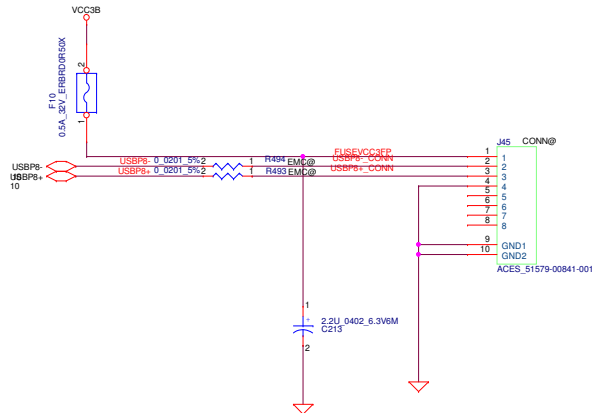



TABLE

Sensor	Device	Placed on
DIODE 0	EC Internal	BOTTOM
DIODE 1	CPU DC-DC	BOTTOM
DIODE 2	DIIMM	BOTTOM
DIODE 3	WLAM	BOTTOM
DIODE 4	#GFX DC-DC	BOTTOM
DIODE 5	Onboard DRAM	BOTTOM
DIODE 6	WWAN	BOTTOM



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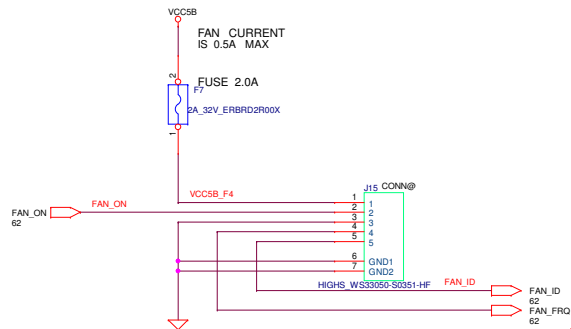
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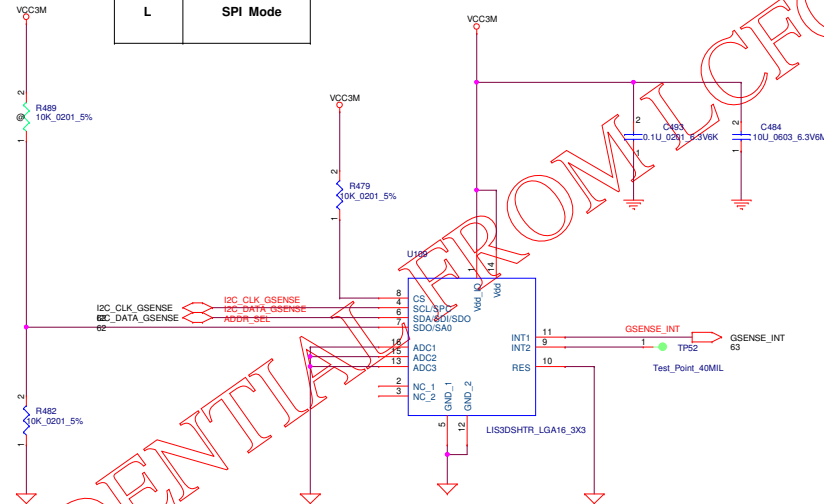
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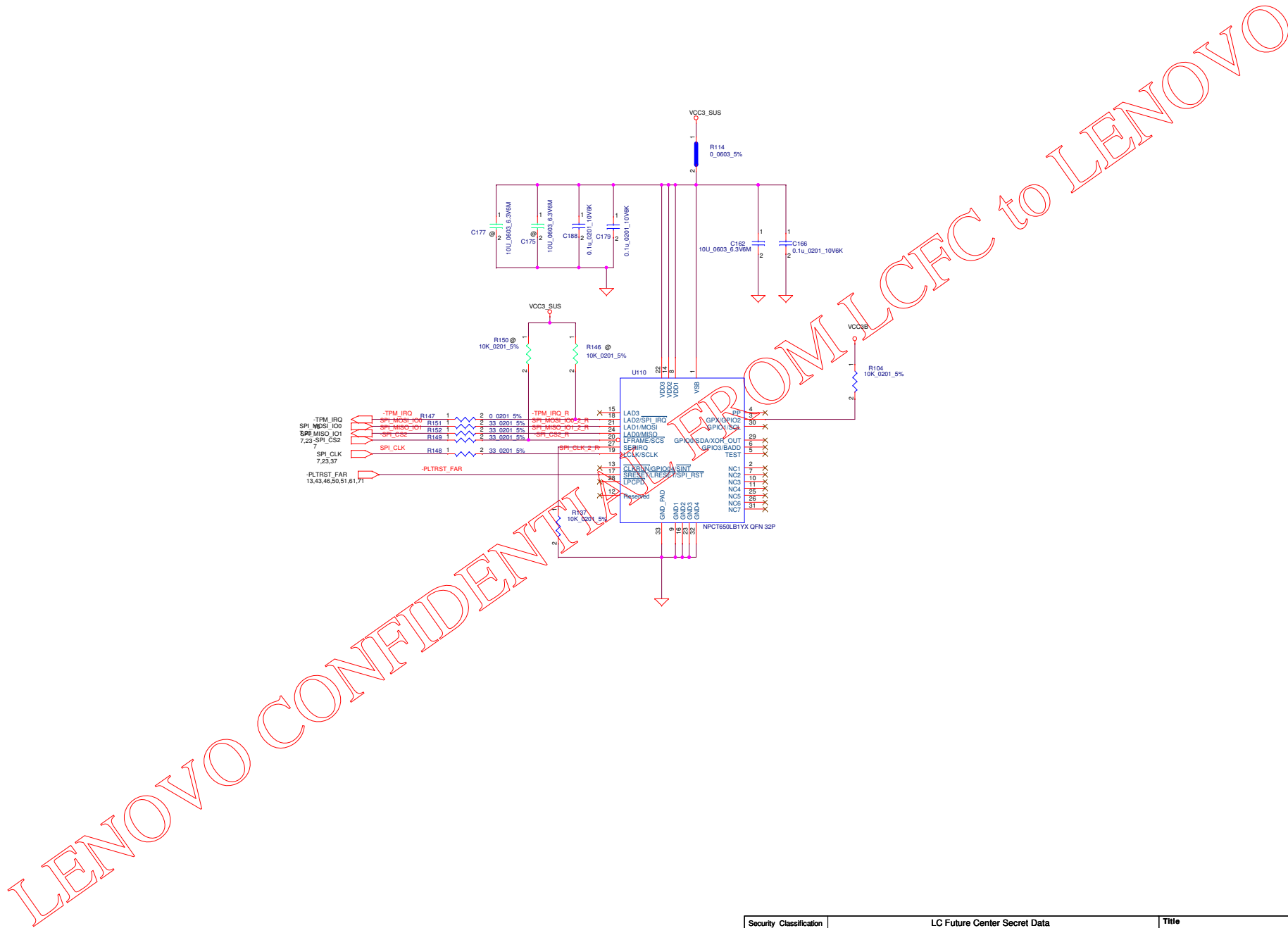
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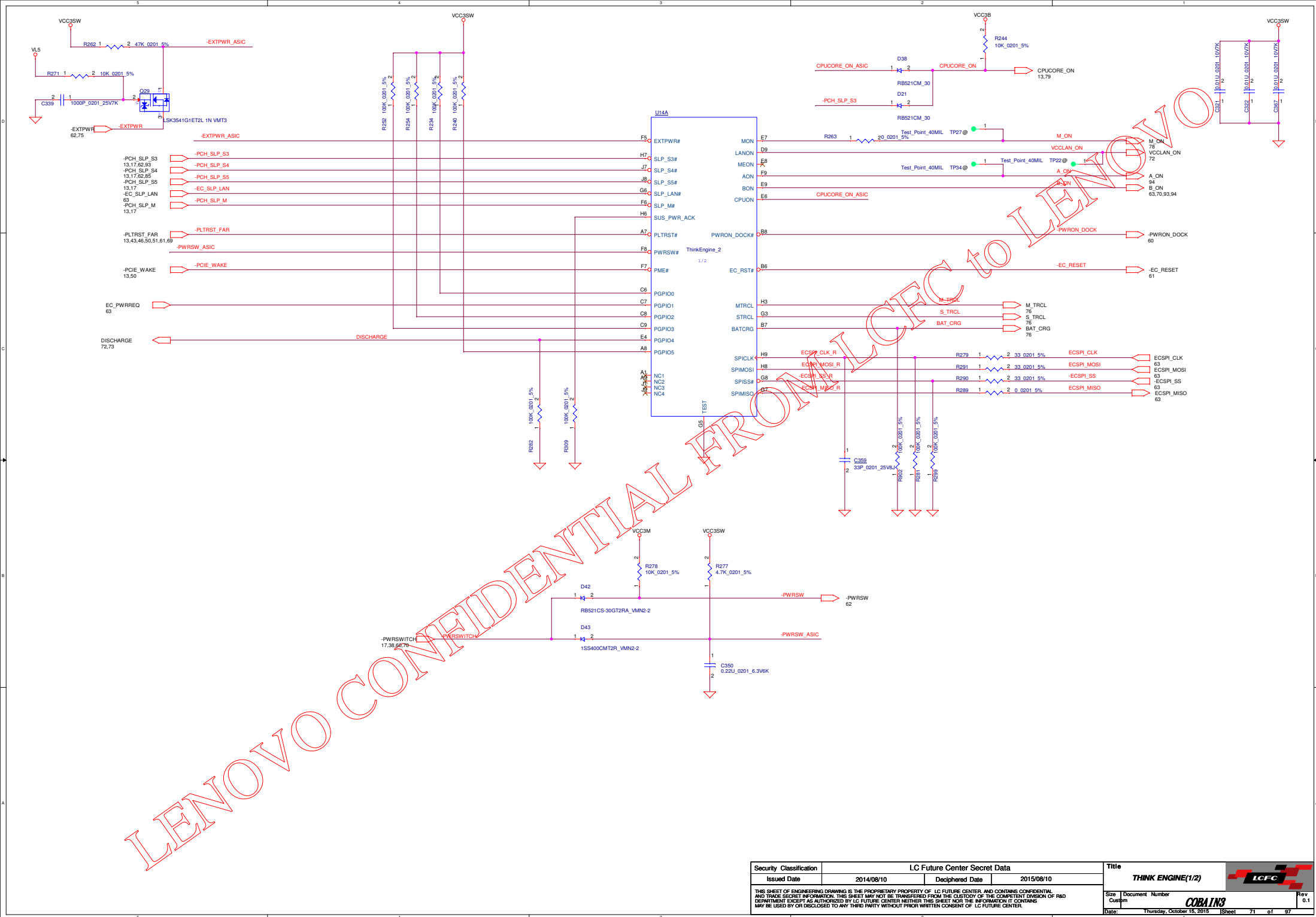
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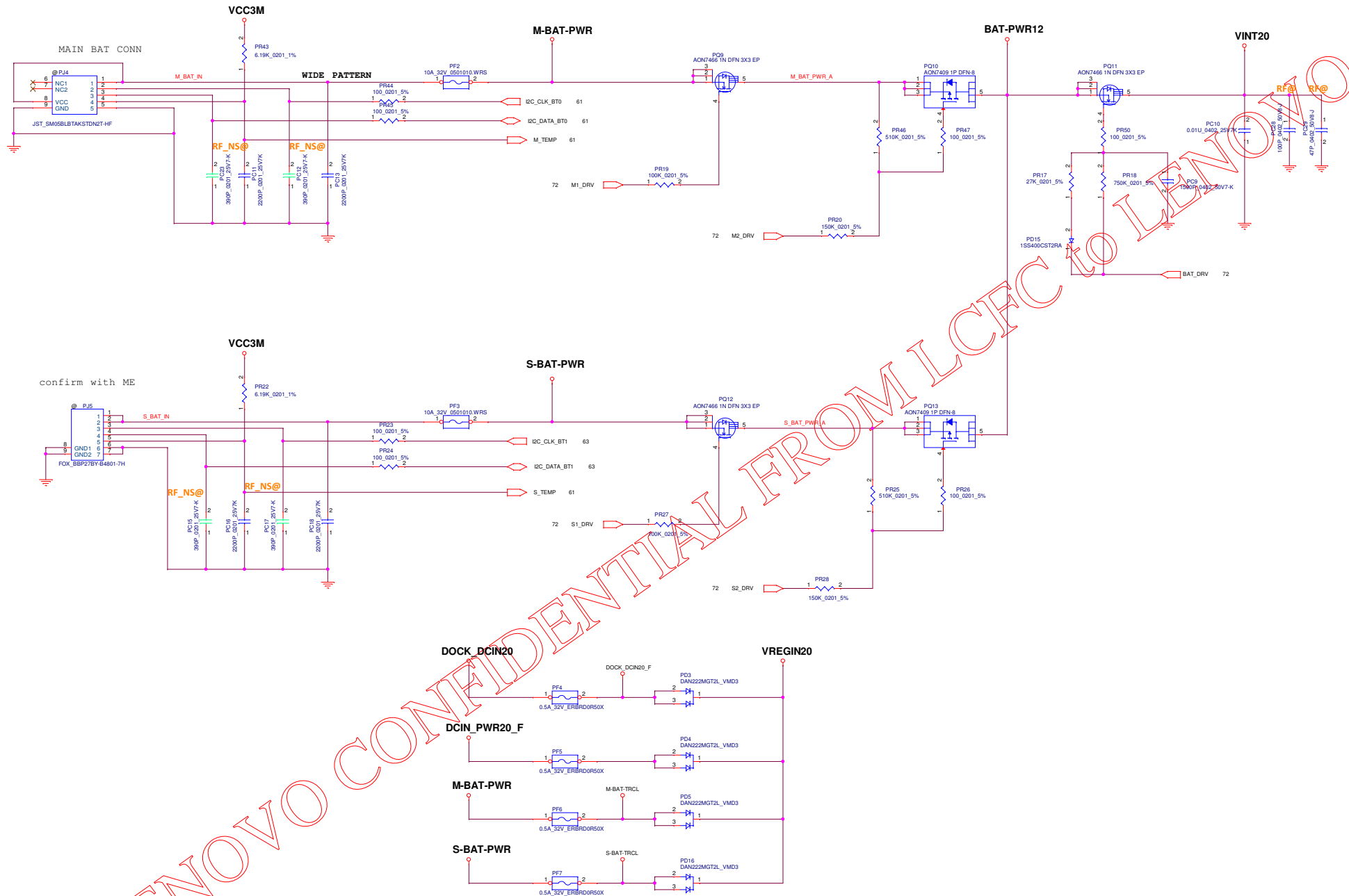
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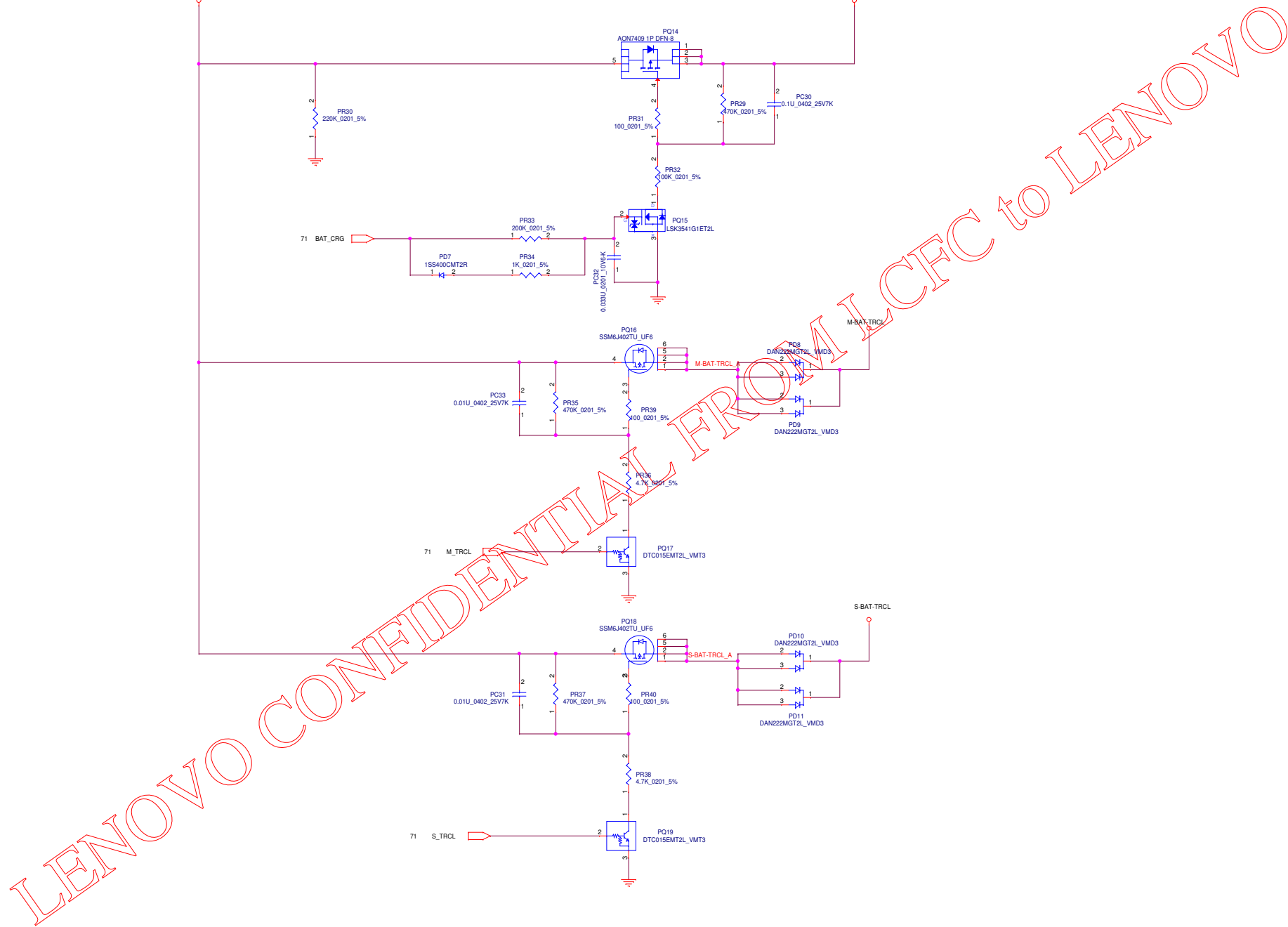



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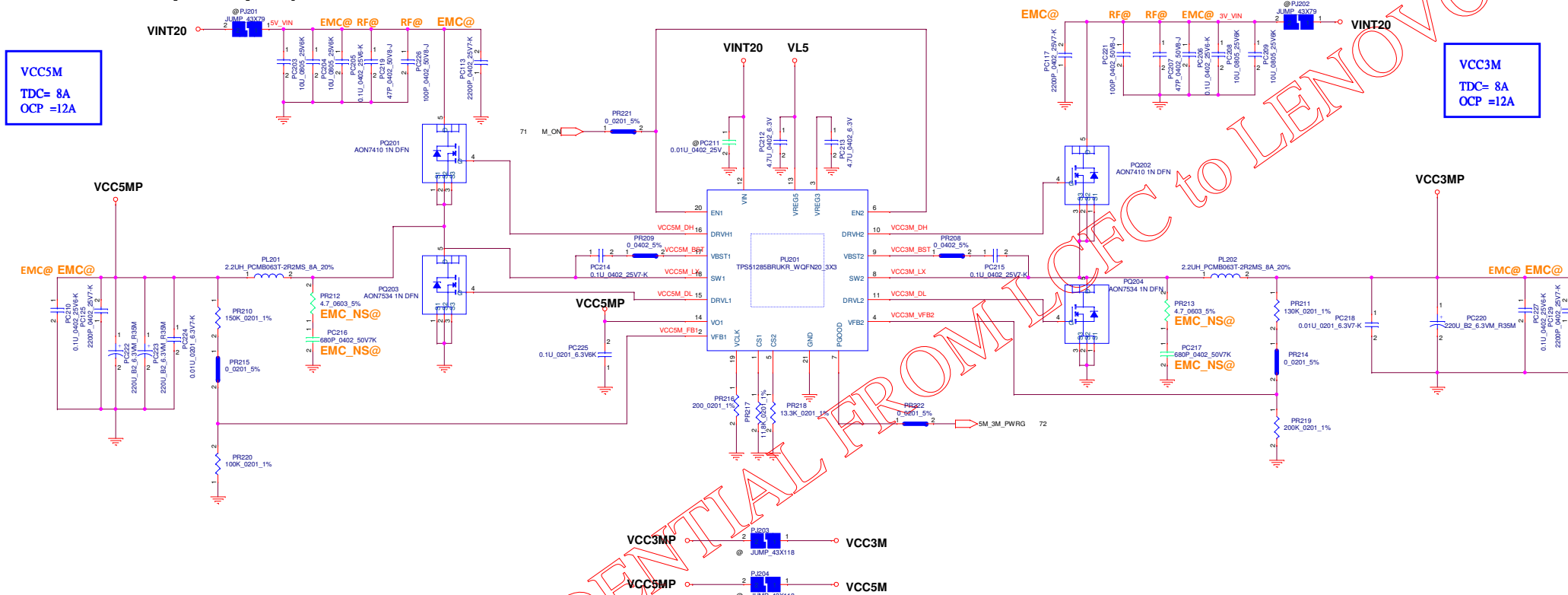
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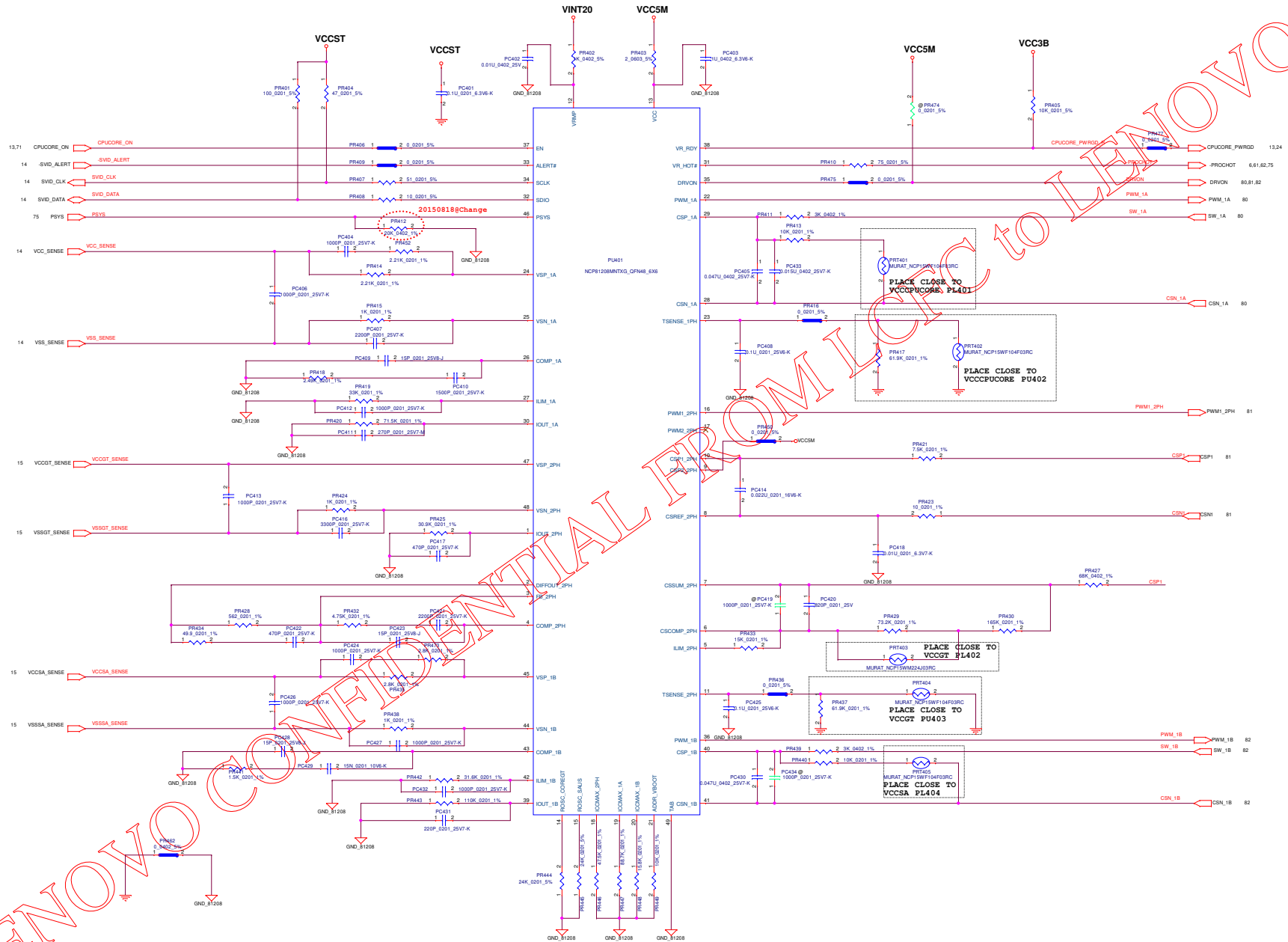
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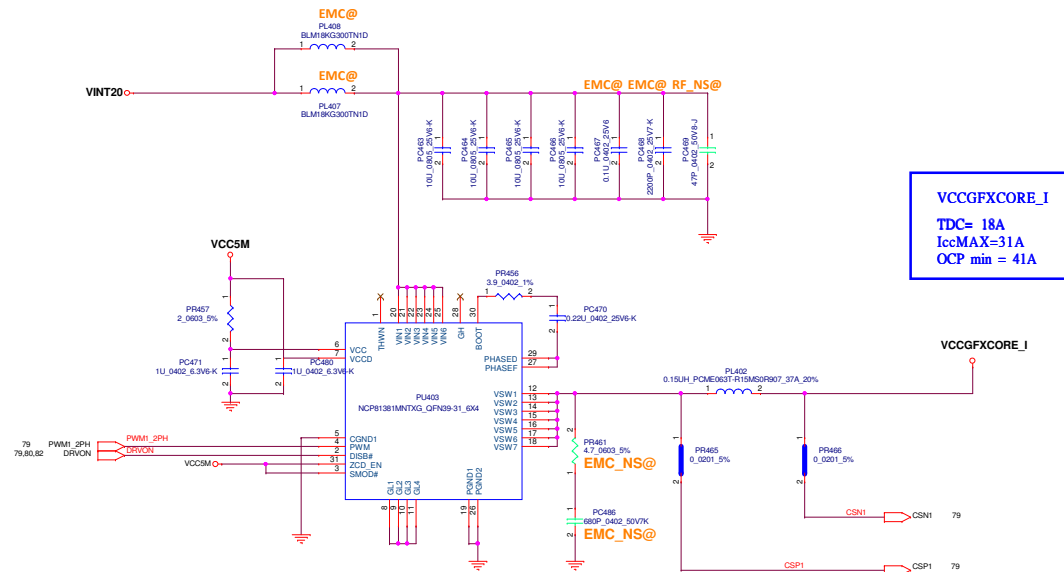
All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.



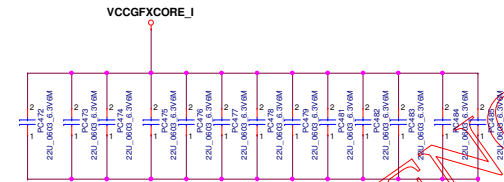
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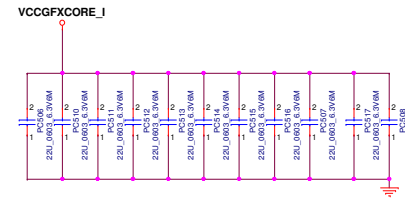
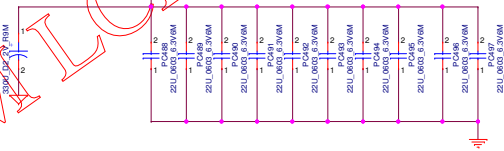




VCCGFXCORE_I
TDC= 18A
IccMAX=31A
OCP min = 41A

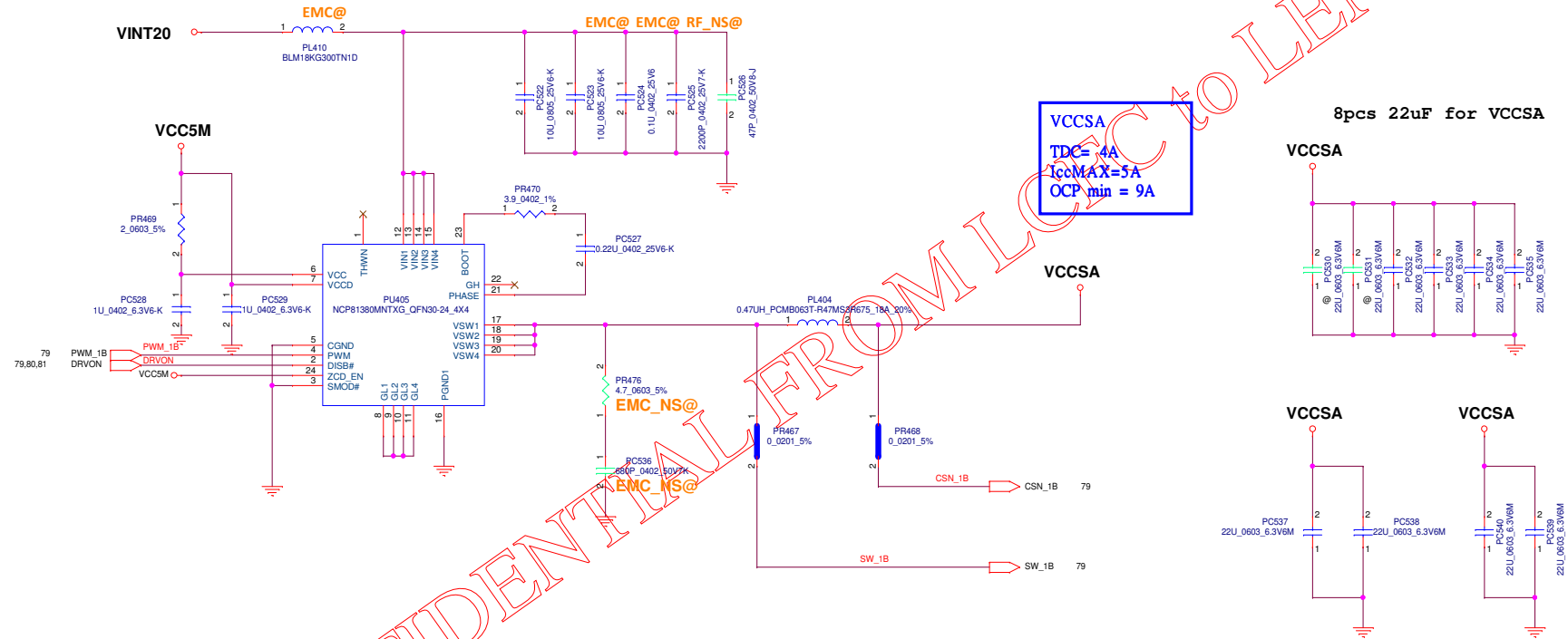



VCCGFXCORE_I 34pcs 22uF for VCCGFXCORE_I

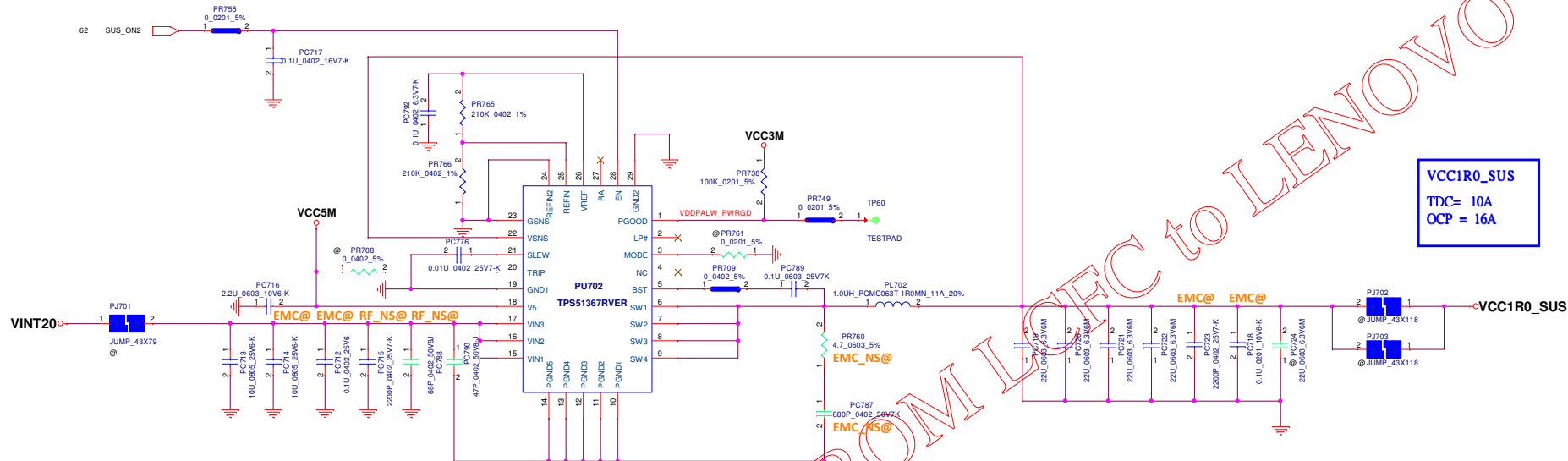


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Mode	Frequency
GND	400KHz
Float	800KHz

VCC1R0_SUS
TDC= 10A
OCP = 16A

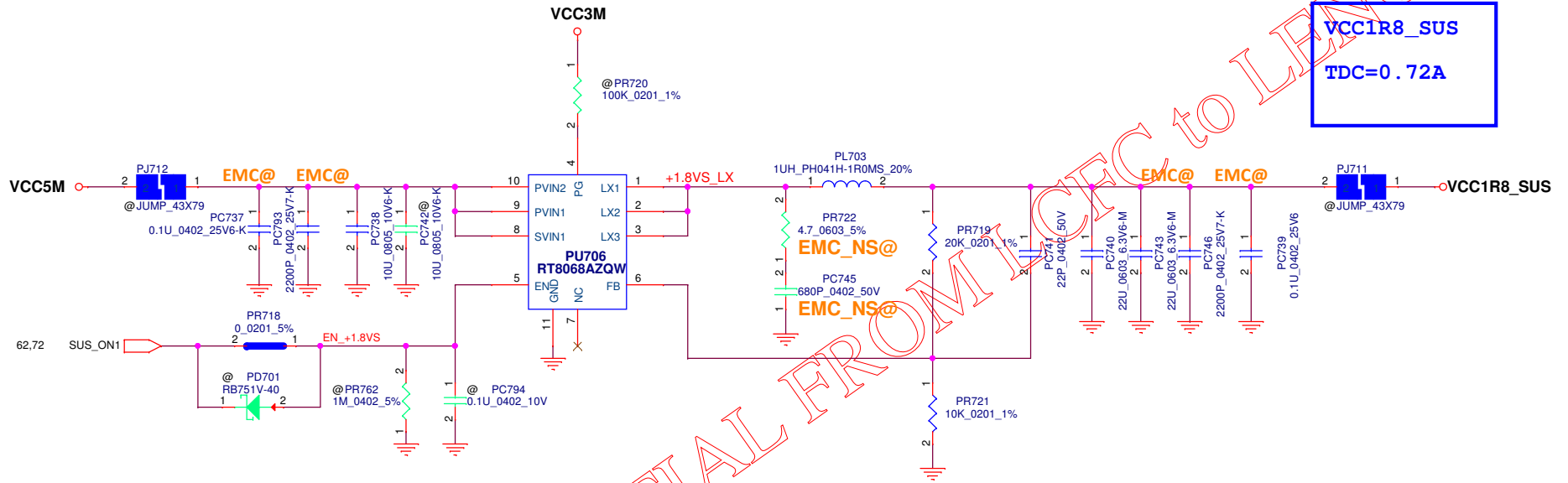
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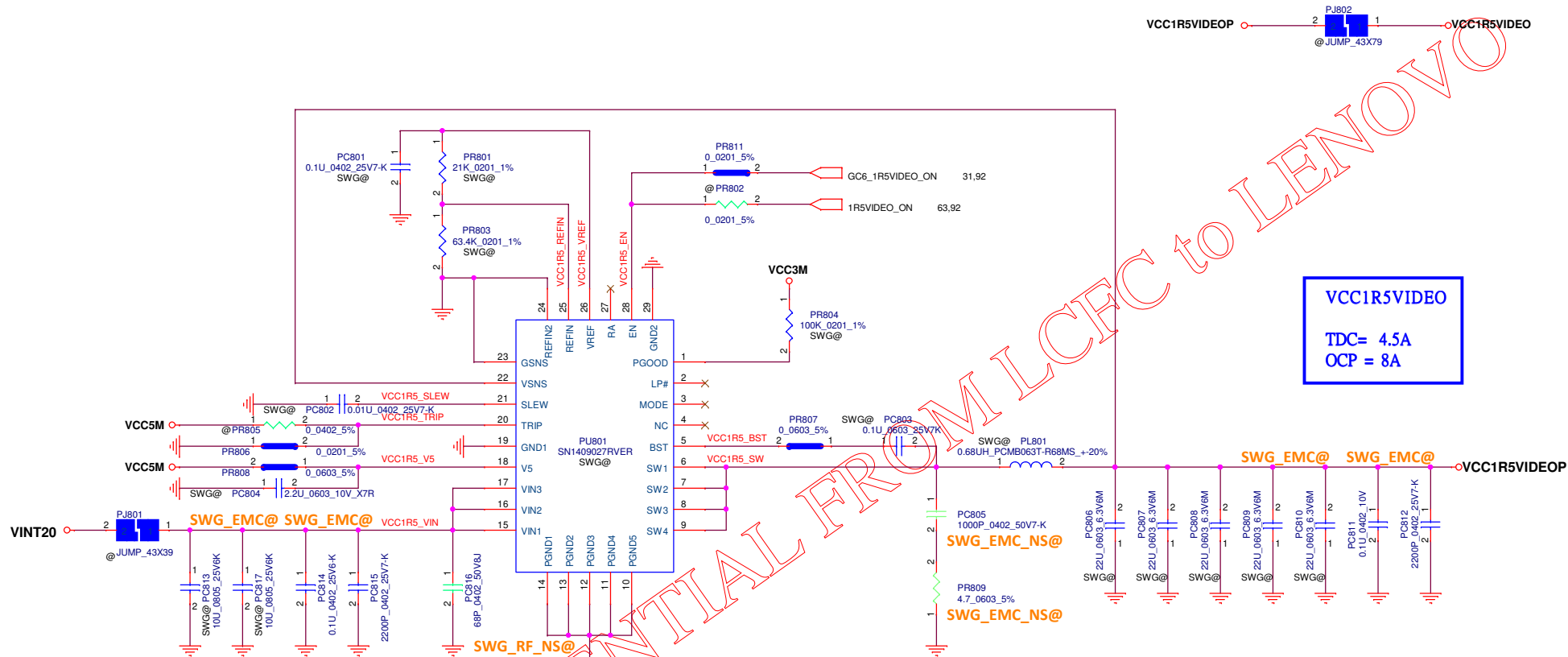




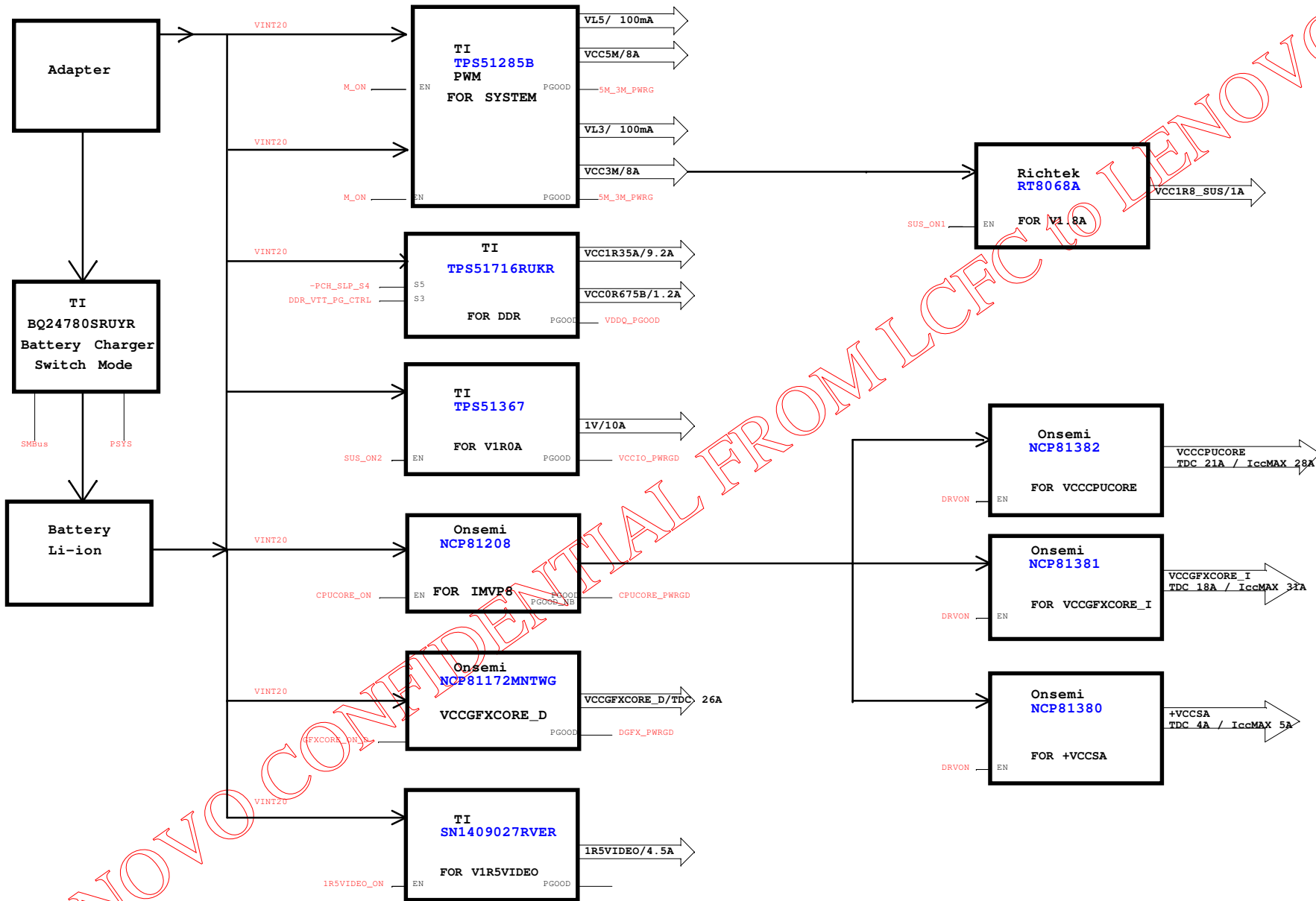
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VCCGFXCORE_D
TDC= 26A
EDR-PEAK=51A
OCP = 58A

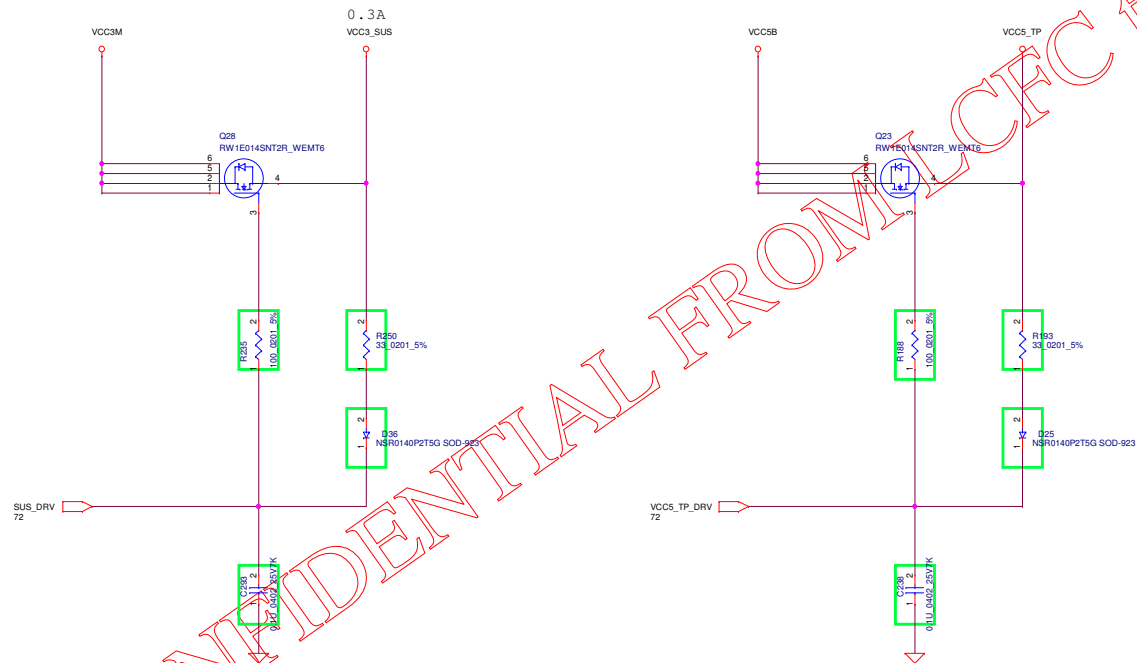
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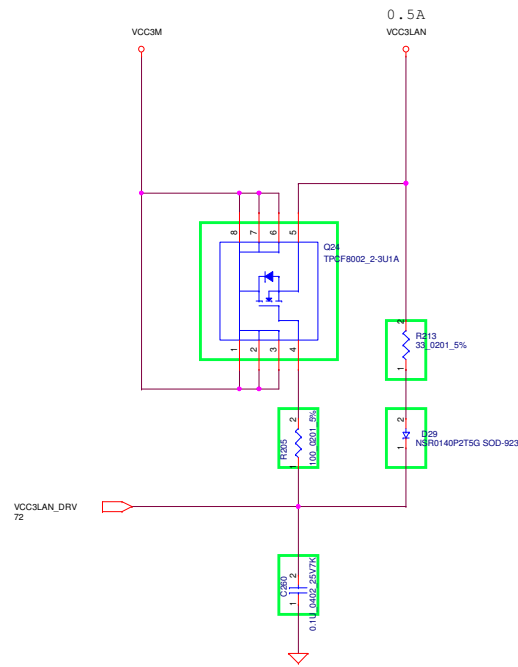
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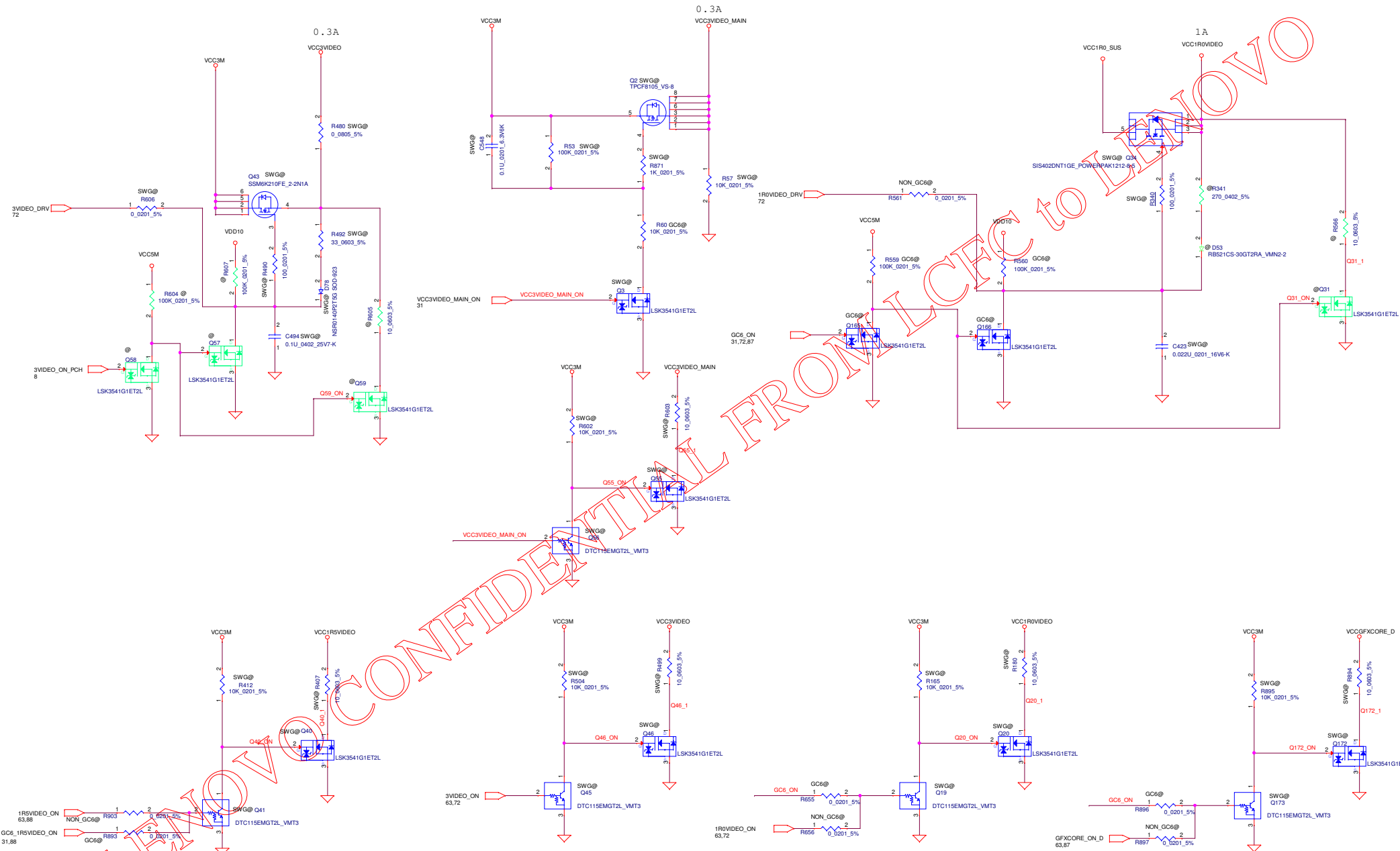



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0.24					
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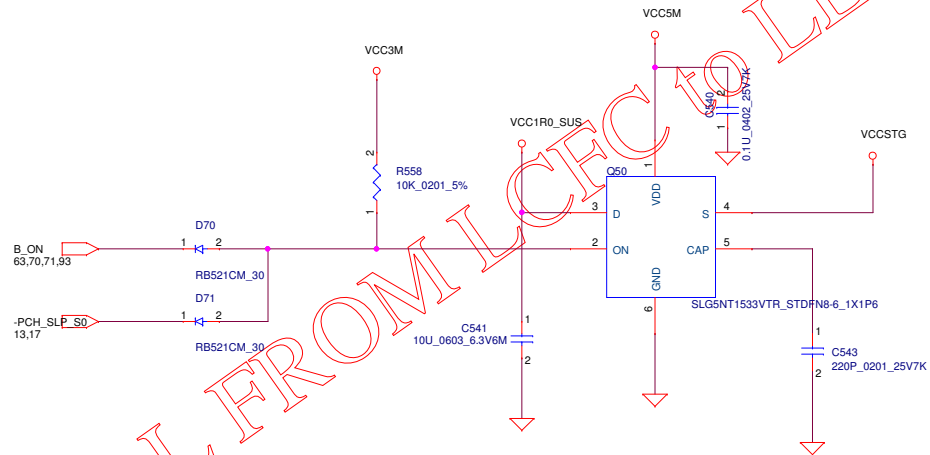
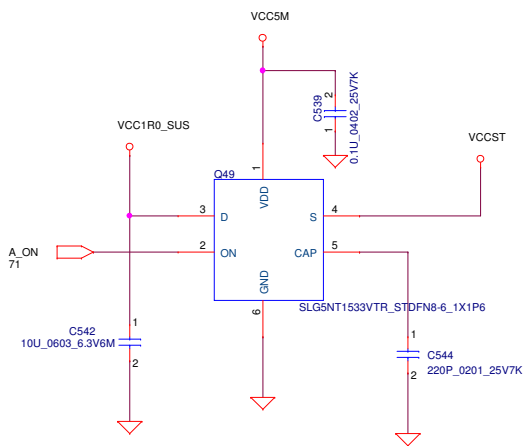


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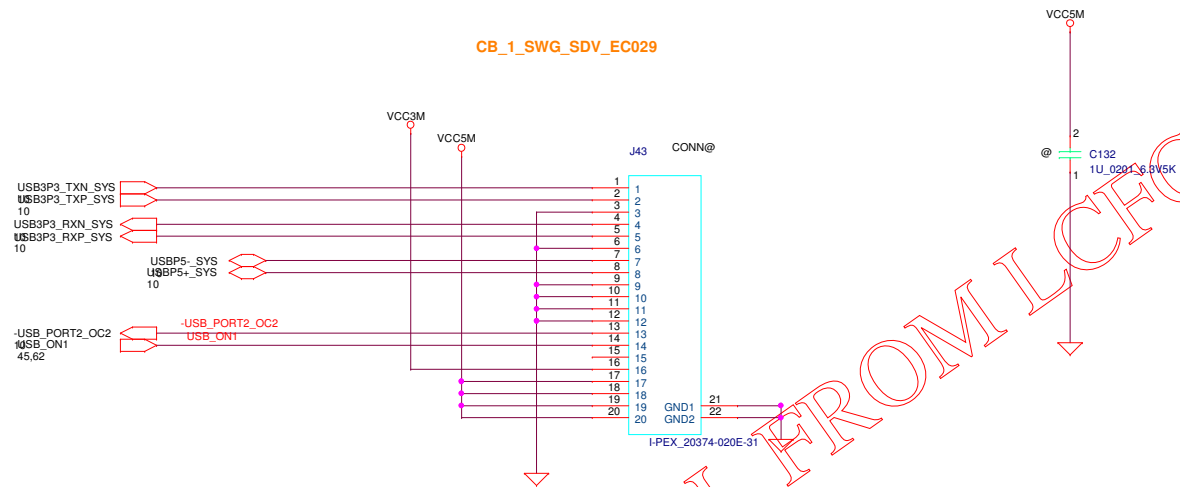



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