UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :NotInstalled
UMA:UMA platform installed
OPS:Optimus
CR:Chief River
V: V-Series installed

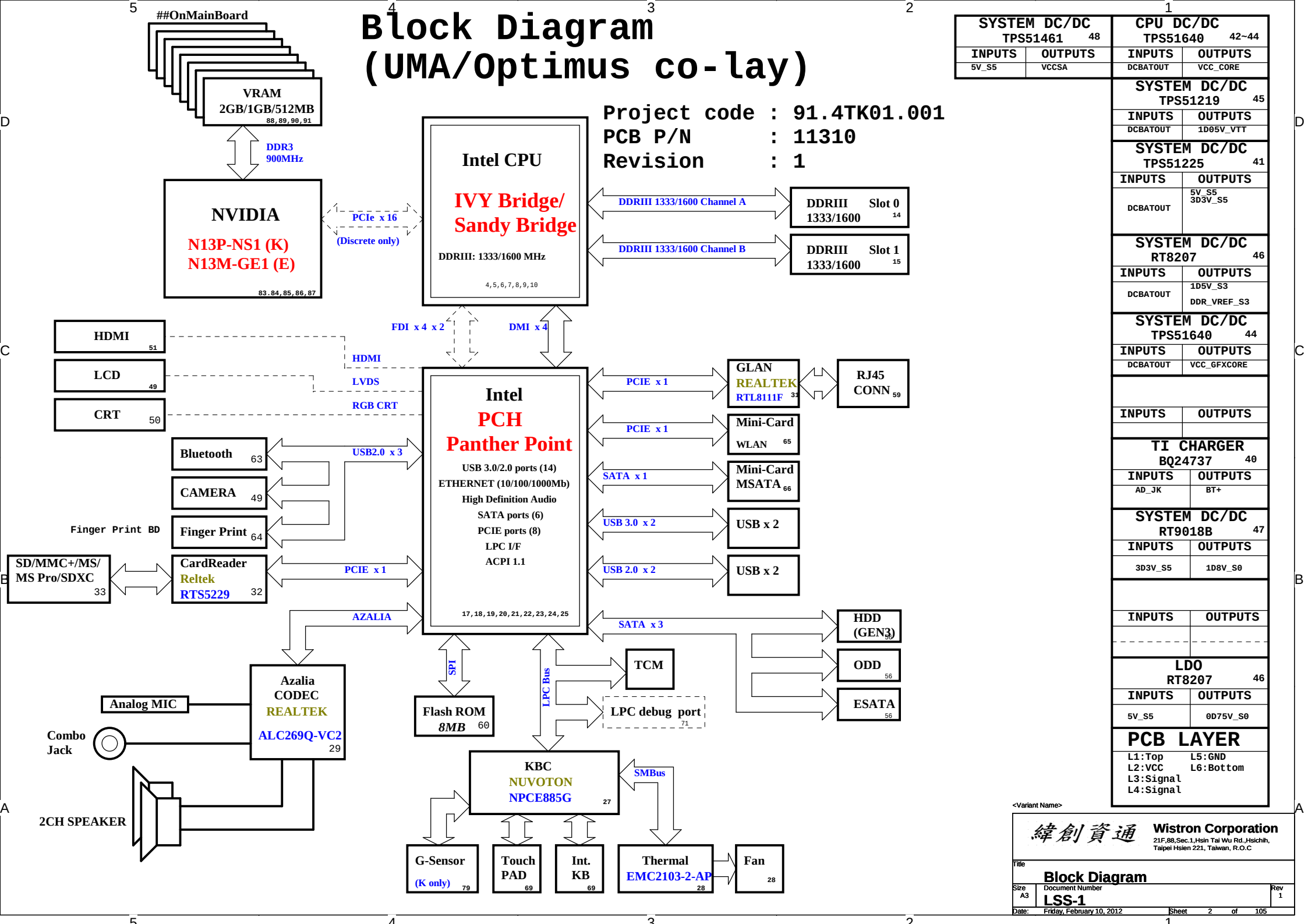
<Variant Name>

緯創資通
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: **Cover Page**		
Size: A4	Document Number: **LSS-1**	Rev: 1
Date: Friday, February 10, 2012	Sheet 1 of 105	

Block Diagram (UMA/Optimus co-lay)

Project code : 91.4TK01.001
PCB P/N : 11310
Revision : 1



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
5V_S5	VCCSA

CPU DC/DC TPS51640 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51219 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51225 41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC RT8207 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC TPS51640 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

INPUTS	OUTPUTS

TI CHARGER BQ24737 40	
INPUTS	OUTPUTS
AD_JK	BT+

SYSTEM DC/DC RT9018B 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

INPUTS	OUTPUTS

LDO RT8207 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:GND
L2:VCC	L6:Bottom
L3:Signal	
L4:Signal	

<Variant Name>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: Block Diagram

Size: A3 | Document Number: LSS-1 | Rev: 1

Date: Friday, February 10, 2012 | Sheet 2 of 105

PCH Strapping

Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1D0V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

PCIe Routing

LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN / LAN
LANE7	X
LANE8	Express Card

USB Table

port9 is debug port

Pair	Device
0	USB3.0 ext port 1
1	USB3.0 ext port 2
2	USB3.0 ext port 3
3	USB3.0 ext port 4
4	BLUETOOTH (USB1.1)
5	Fingerprint (USB1.1)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB ext. port 4 / E-SATA /USB CHARGER
10	CARD READER
11	Mini Card1 (WLAN)
12	CCD
13	New Card

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

SATA Table

SATA Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

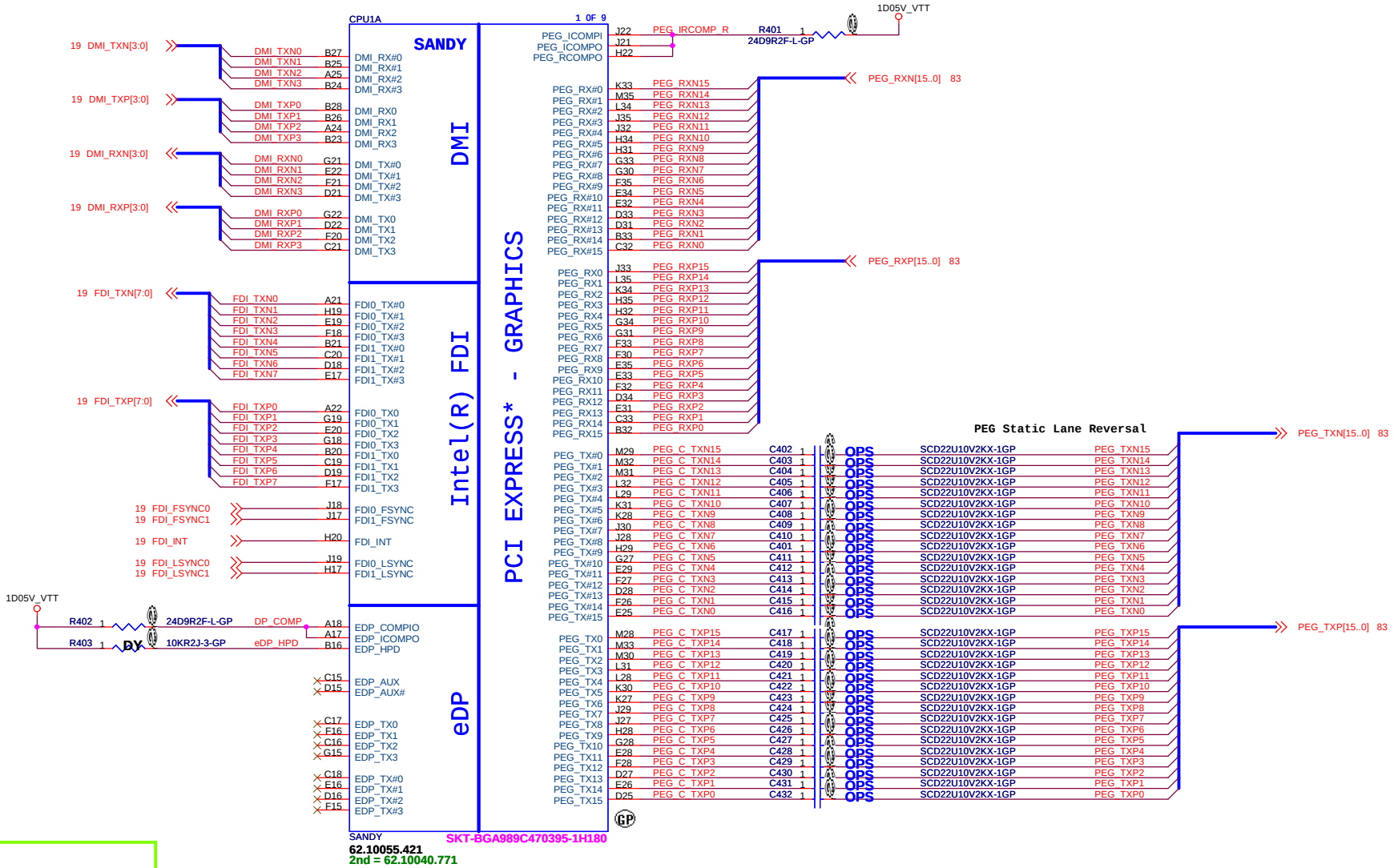
Title: Table of Content

Size: A3 | Document Number: LSS-1 | Rev: 1

Date: Friday, February 10, 2012 | Sheet 3 of 105

SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

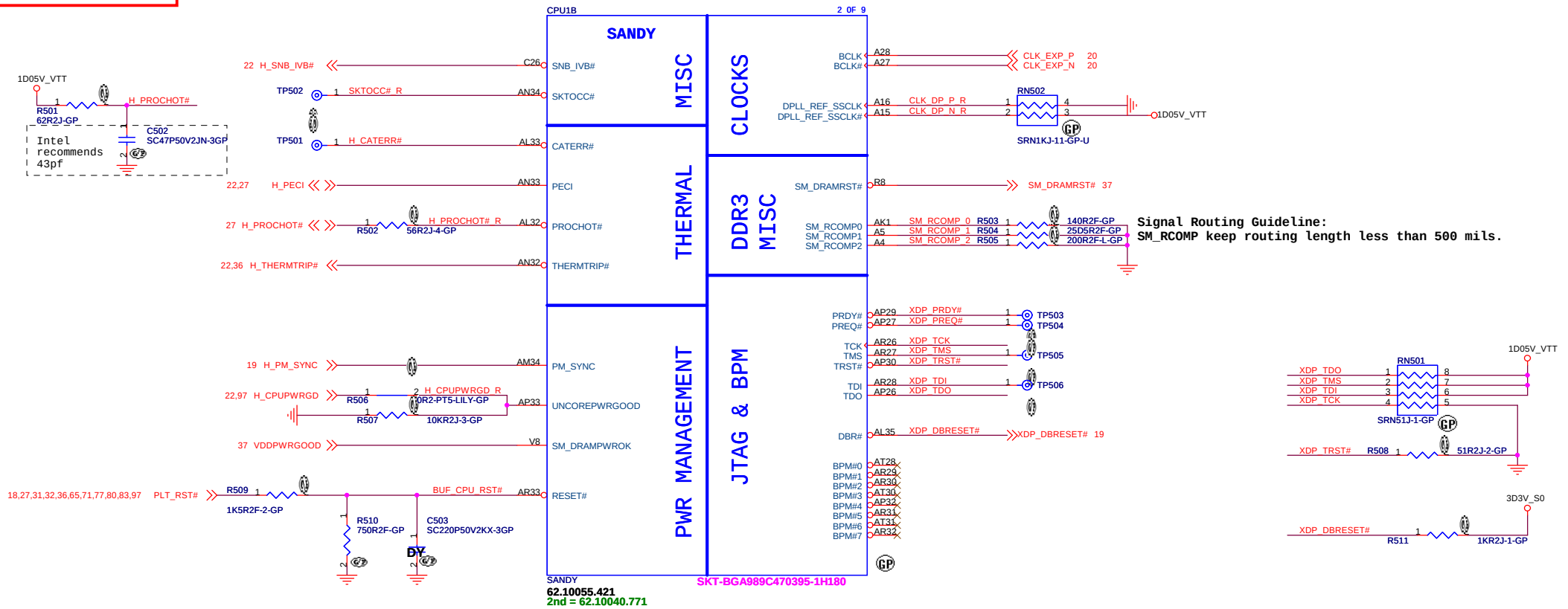
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

<Variant Name>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

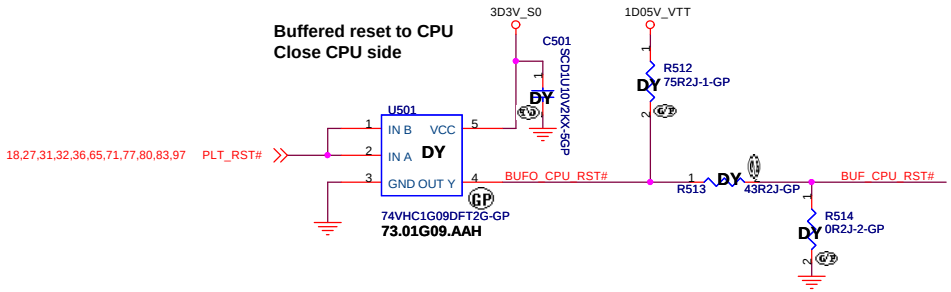
Title: CPU (PCIE/DMI/FDI)
Size: A3
Document Number: LSS-1
Rev: 1
Date: Wednesday, February 22, 2012
Sheet 4 of 105

SSID = CPU



Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

Buffered reset to CPU
Close CPU side



<Variant Name>

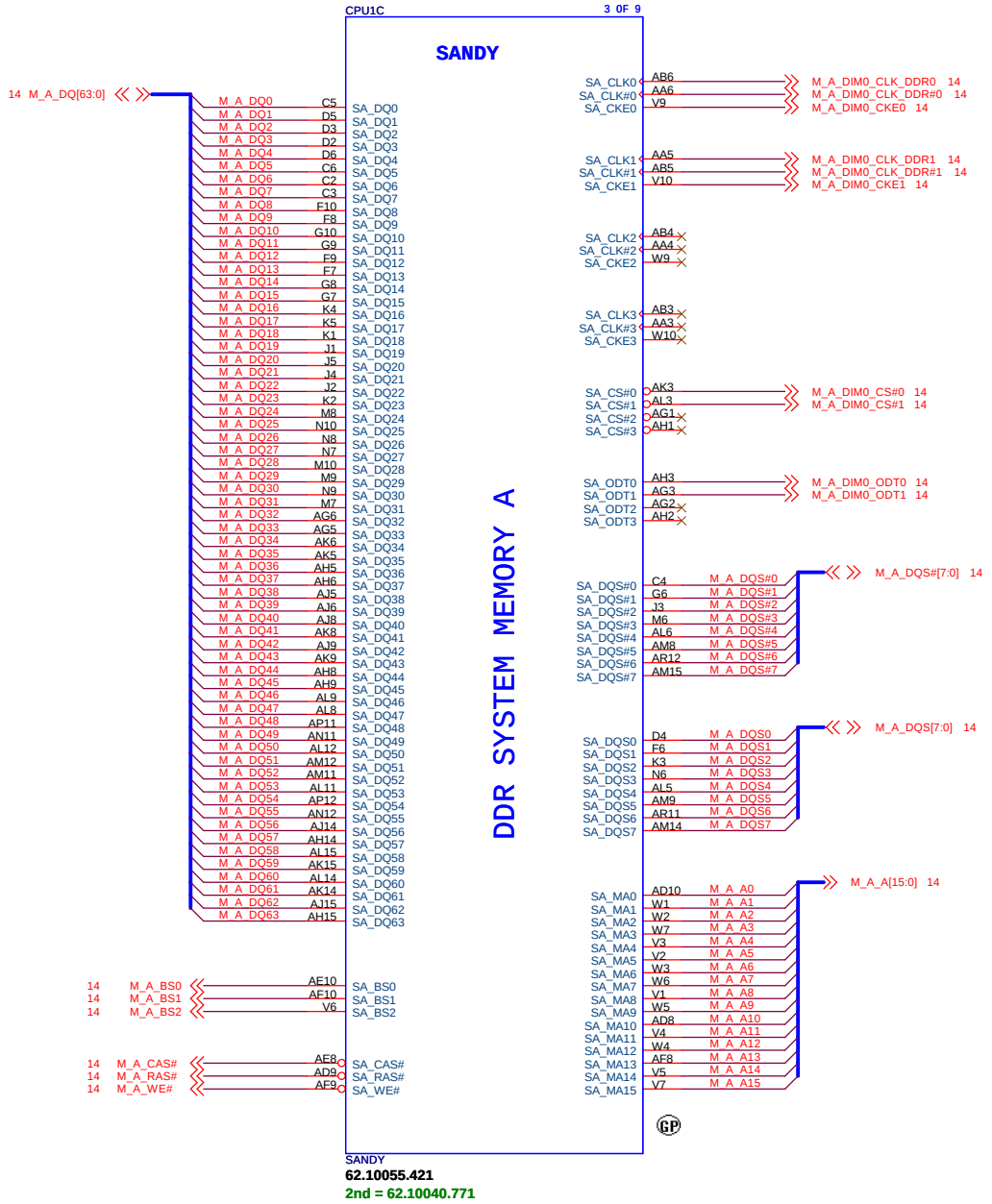
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

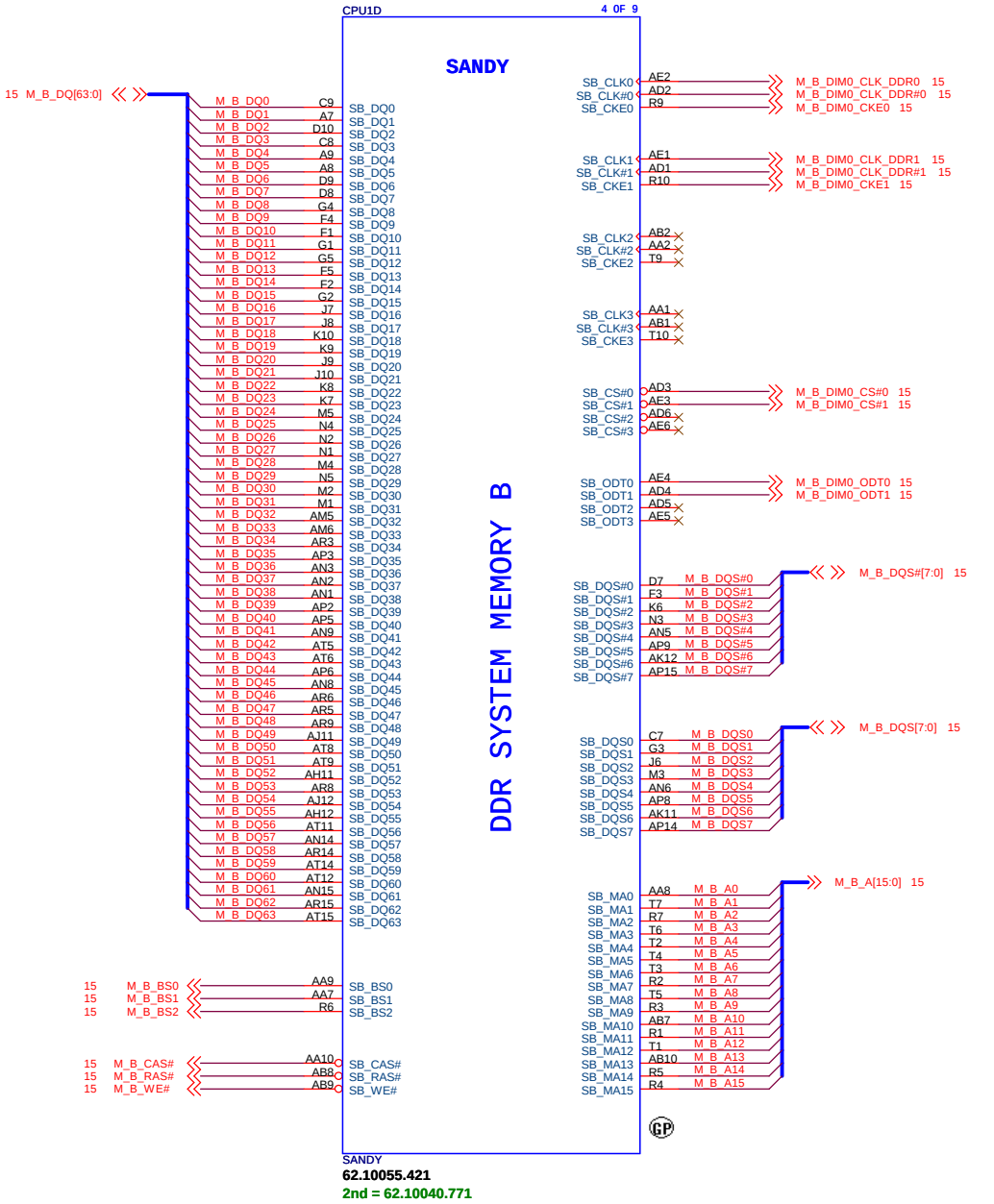
Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A3	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 5 of 105

SSID = CPU





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (DDR)***

Size	Document Number	Rev
A3	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 6 of 105

SSID = CPU

CFG2 — R702 1KR2J-1-GP — QPS

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

CFG4 — R703 1KR2J-1-GP — DY

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG0 — R706 1KR2J-1-GP — DY

CFG5 — R704 1KR2J-1-GP — DY

CFG6 — R705 1KR2J-1-GP — DY

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG7 — R701 1KR2J-1-GP — DY

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CPU1E — 5 OF 9

SANDY

RESERVED

TP702	CFG0	AK28	CFG0
	CFG1	AK29	CFG1
TP704	CFG2	AL26	CFG2
	CFG3	AL27	CFG3
	CFG4	AK26	CFG4
	CFG5	AL29	CFG5
	CFG6	AL30	CFG6
	CFG7	AM31	CFG7
		AM32	CFG8
		AM30	CFG9
		AM28	CFG10
		AM26	CFG11
		AN28	CFG12
		AN31	CFG13
		AN26	CFG14
		AM27	CFG15
TP705	CFG16	AK31	CFG16
		AN29	CFG17
		AJ31	RSVD#AJ31
		AH31	RSVD#AH31
		AJ33	RSVD#AJ33
		AH33	RSVD#AH33
		AJ26	RSVD#AJ26
12 DDR_WR_VREF01		B4	RSVD#B4
12 DDR_WR_VREF02		D1	RSVD#D1
		F25	RSVD#F25
		F24	RSVD#F24
		F23	RSVD#F23
		D24	RSVD#D24
		G25	RSVD#G25
		G24	RSVD#G24
		F23	RSVD#E23
		D23	RSVD#D23
		C30	RSVD#C30
		A31	RSVD#A31
		B30	RSVD#B30
		B29	RSVD#B29
		D30	RSVD#D30
		B31	RSVD#B31
		A30	RSVD#A30
		C29	RSVD#C29
TP708	H_VCCP_SEL	J20	RSVD#J20
		B18	RSVD#B18
		A19	RSVD#A19
		J15	RSVD#J15

		L7	RSVD#L7
		AG7	RSVD#AG7
		AE7	RSVD#AE7
		AK2	RSVD#AK2
		W8	RSVD#W8
		AT26	RSVD#AT26
		AM33	RSVD#AM33
		AJ27	RSVD#AJ27
		T8	RSVD#T8
		J16	RSVD#J16
		H16	RSVD#H16
		G16	RSVD#G16
		AR35	RSVD#AR35
		AT34	RSVD#AT34
		AT33	RSVD#AT33
		AP35	RSVD#AP35
		AR34	RSVD#AR34
		B34	RSVD#B34
		A33	RSVD#A33
		A34	RSVD#A34
		B35	RSVD#B35
		C35	RSVD#C35
		AJ32	RSVD#AJ32
		AK32	RSVD#AK32
	AH27	TP705	TP706
	AN35	TP706	TP701
	AM35	TP707	TP707
		AT2	RSVD#AT2
		AT1	RSVD#AT1
		AR1	RSVD#AR1

SANDY SKT-BGA989C470395-1H180

62.10055.421

2nd = 62.10040.771

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RESERVED)

Size: A3 | Document Number: LSS-1 | Rev: 1

Date: Wednesday, February 22, 2012 | Sheet 7 of 105

POWER

VCC CORE:53A

VCCIO:8.5A

CPU1F

6 OF 9

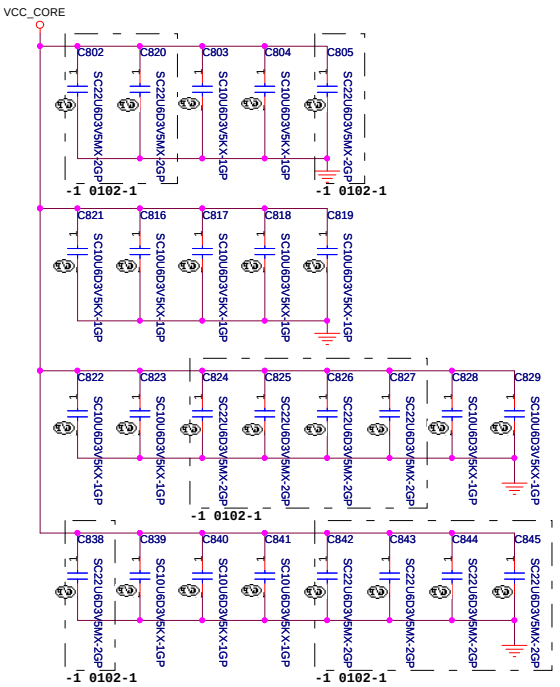
SANDY

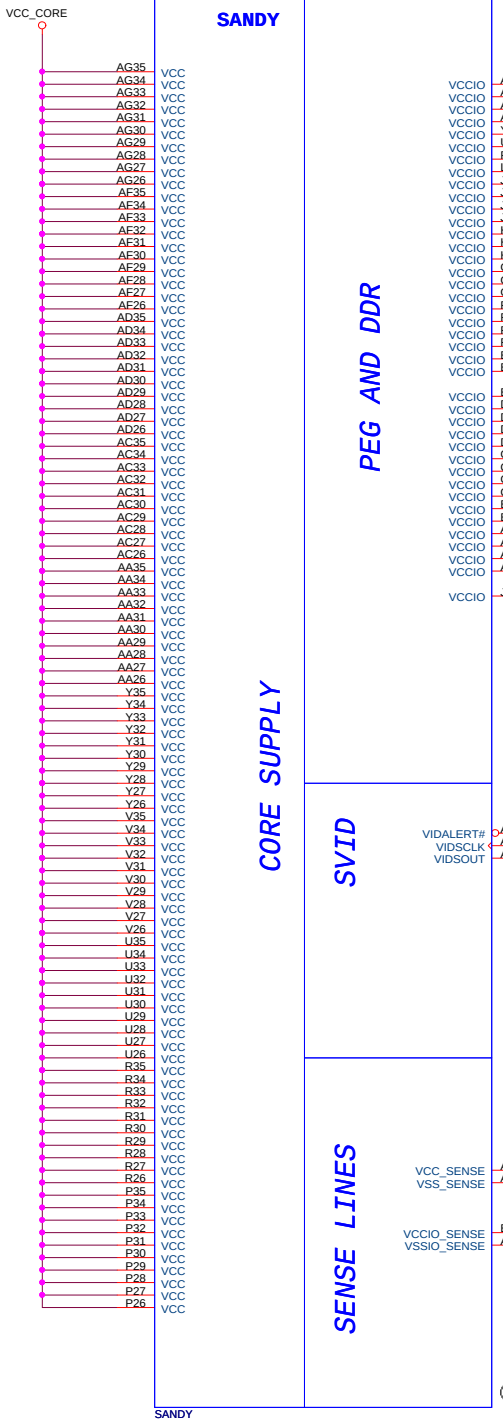
PEG AND DDR

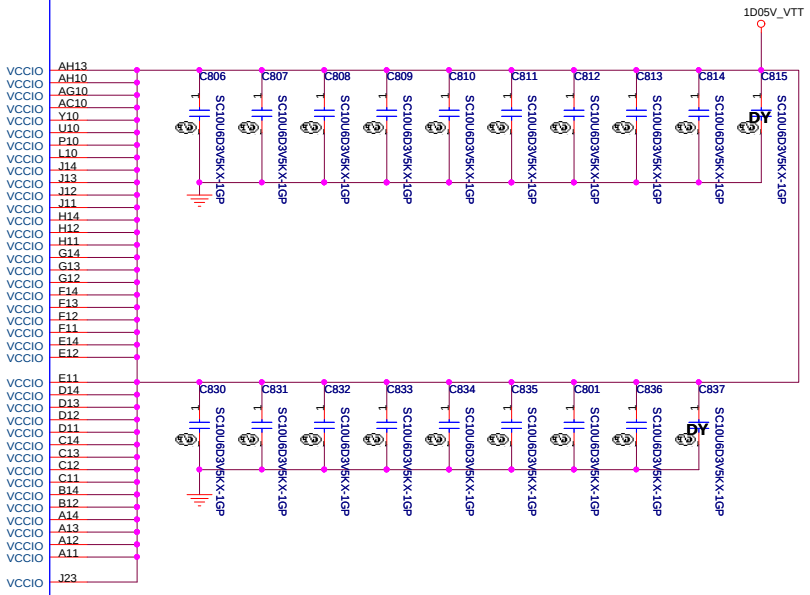
CORE SUPPLY

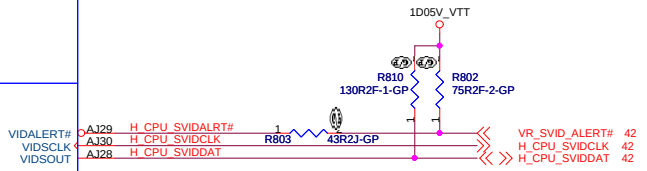
SVID

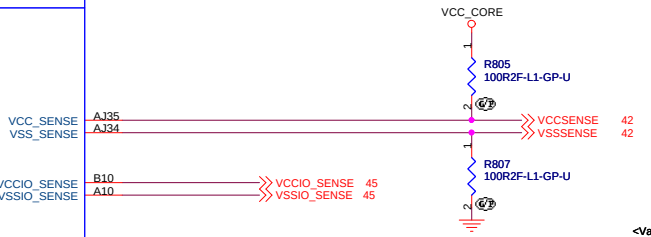
SENSE LINES

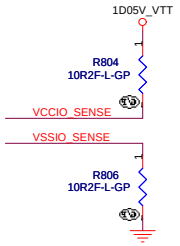












SANDY

62.10055.421

2nd = 62.10040.771

<Variant Name>

緯創資通 Wistron Corporation

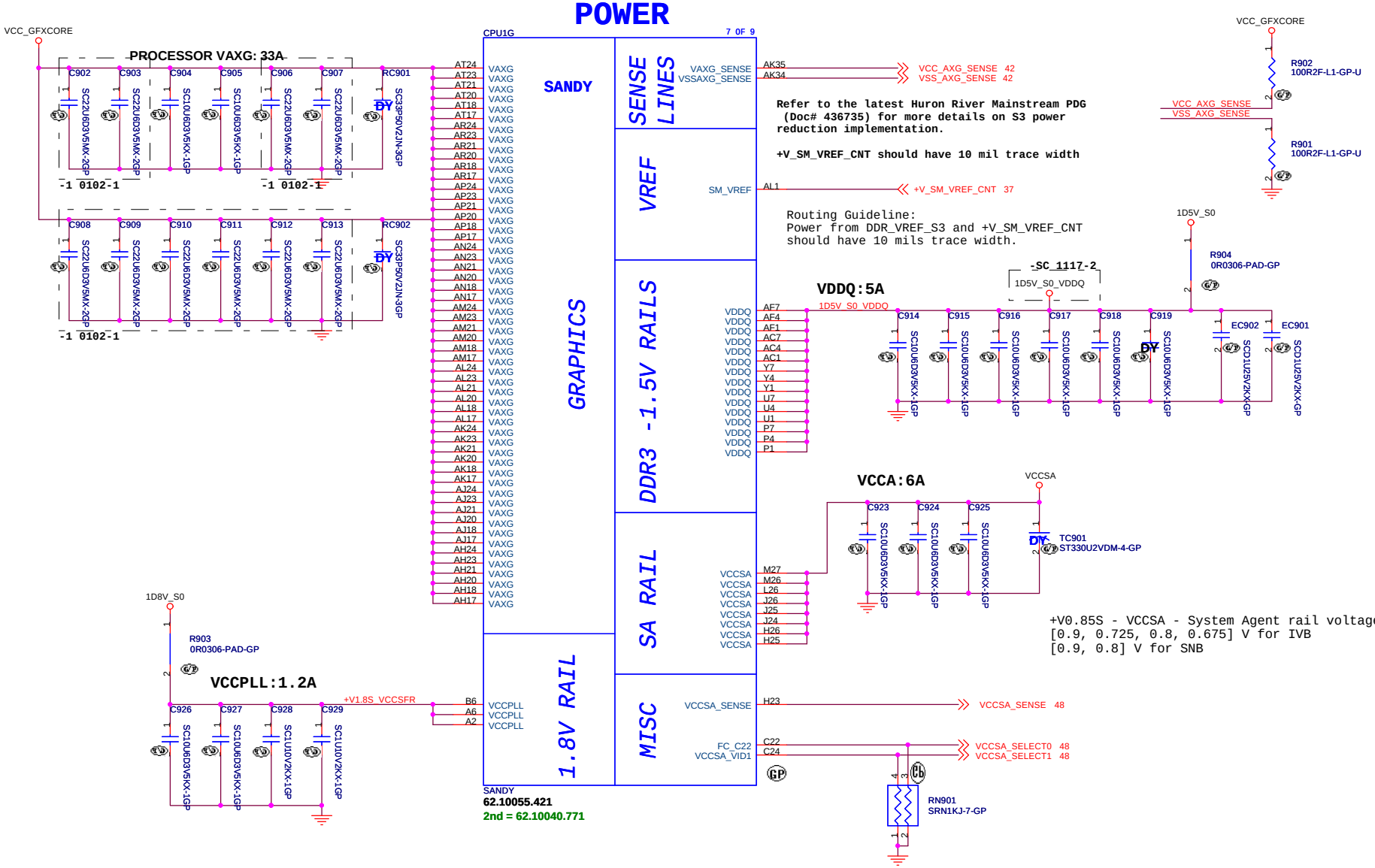
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size: Custom | Document Number: LSS-1 | Rev: 1

Date: Wednesday, February 22, 2012 | Sheet 8 of 105

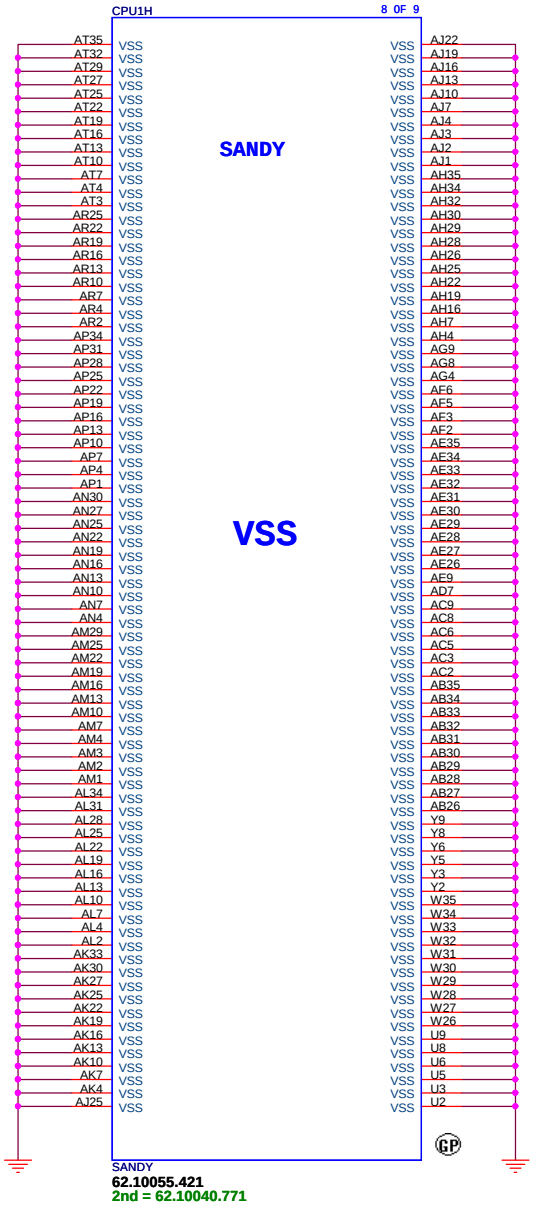
POWER

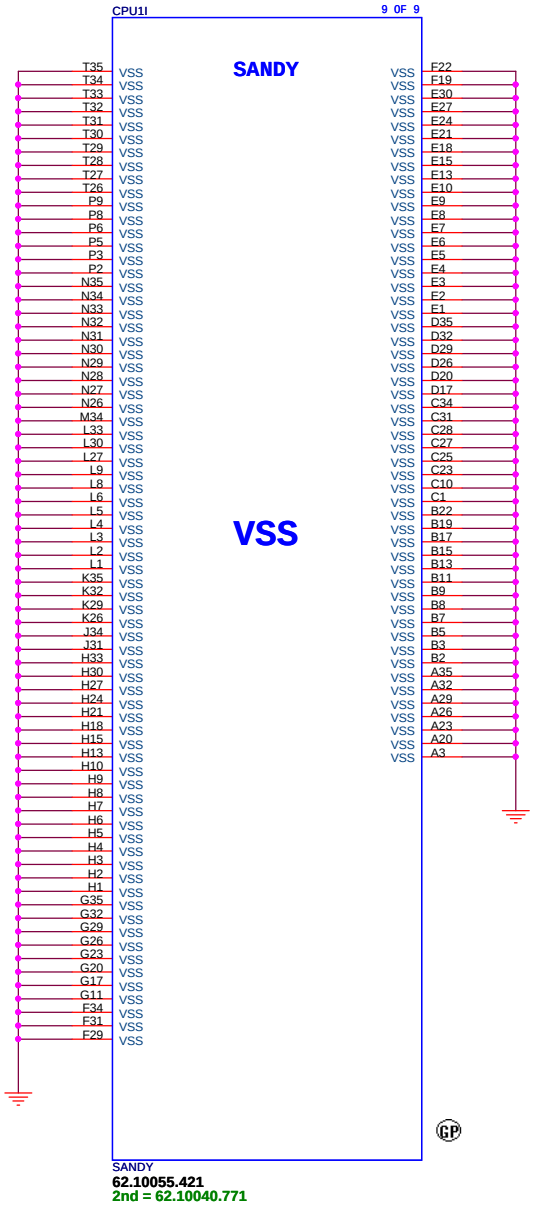


<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU (VCC_GFXCORE)	
Size: A3	Document Number: LSS-1	Rev: 1
Date: Wednesday, February 22, 2012	Sheet 9 of 105	

SSID = CPU





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	LSS-1	1

Date: Friday, February 10, 2012 Sheet 10 of 105

5 4 3 2 1

D

C

BLANK

B

A

<Variant Name>

緯創資通

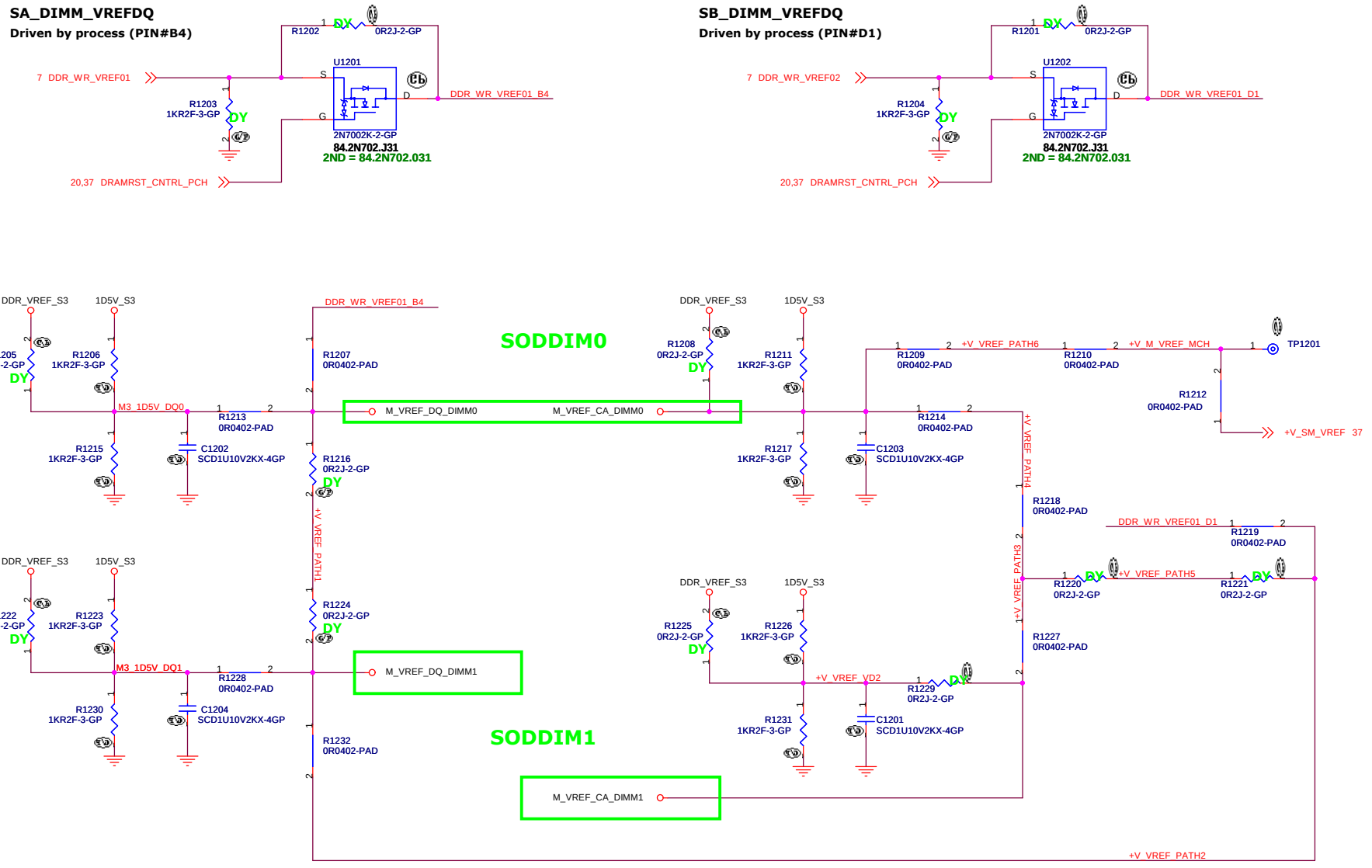
Wistron Corporation

21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: <Title>		
Size: A4	Document Number: LSS-1	Rev: 1
Date: Friday, February 10, 2012	Sheet 11 of 105	

VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

CAD Note: All VREF traces should have 20:20 mil trace geometry

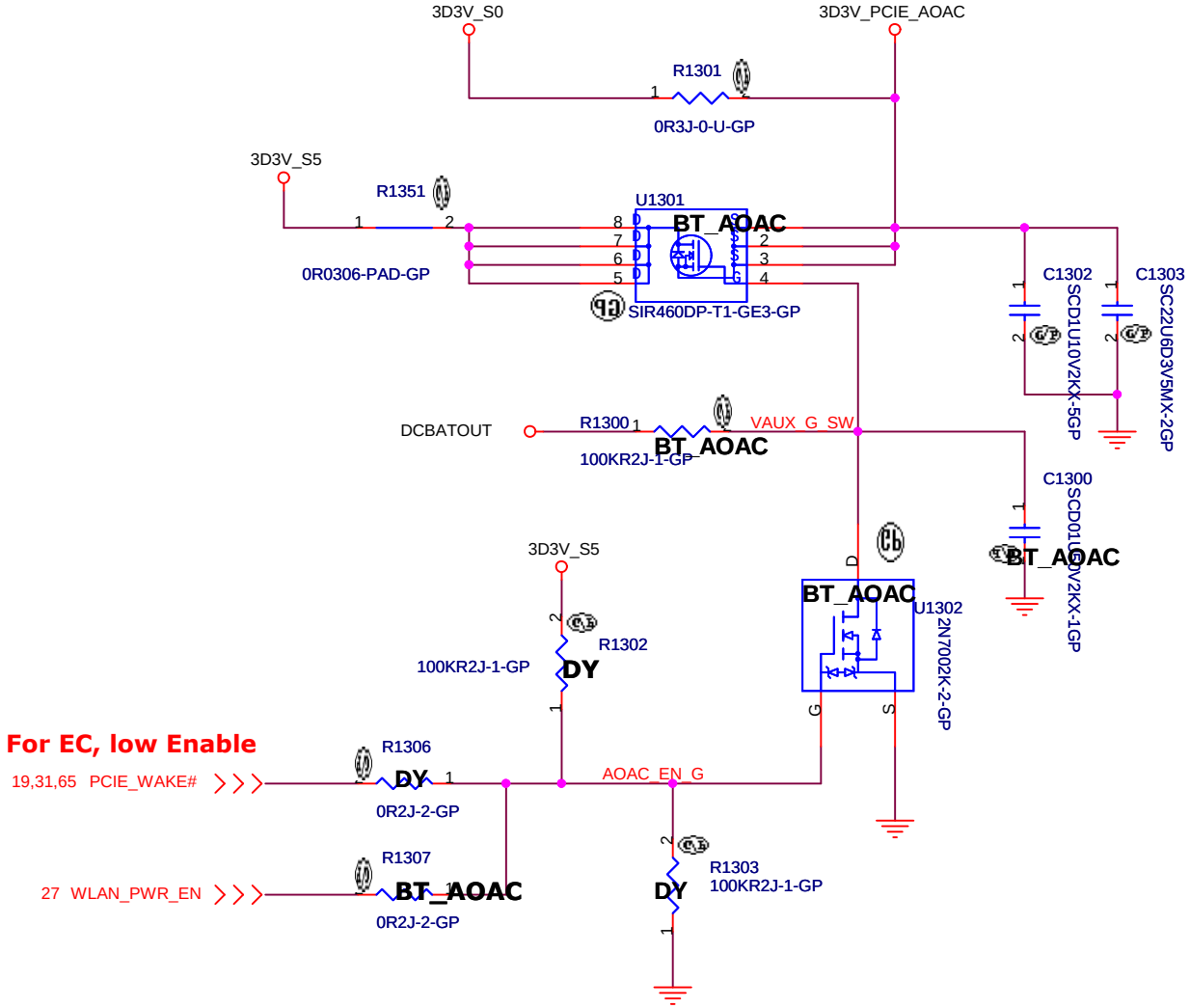


<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
M3		
Size: A3	Document Number: LSS-1	Rev: 1
Date: Wednesday, February 22, 2012	Sheet 12 of 105	

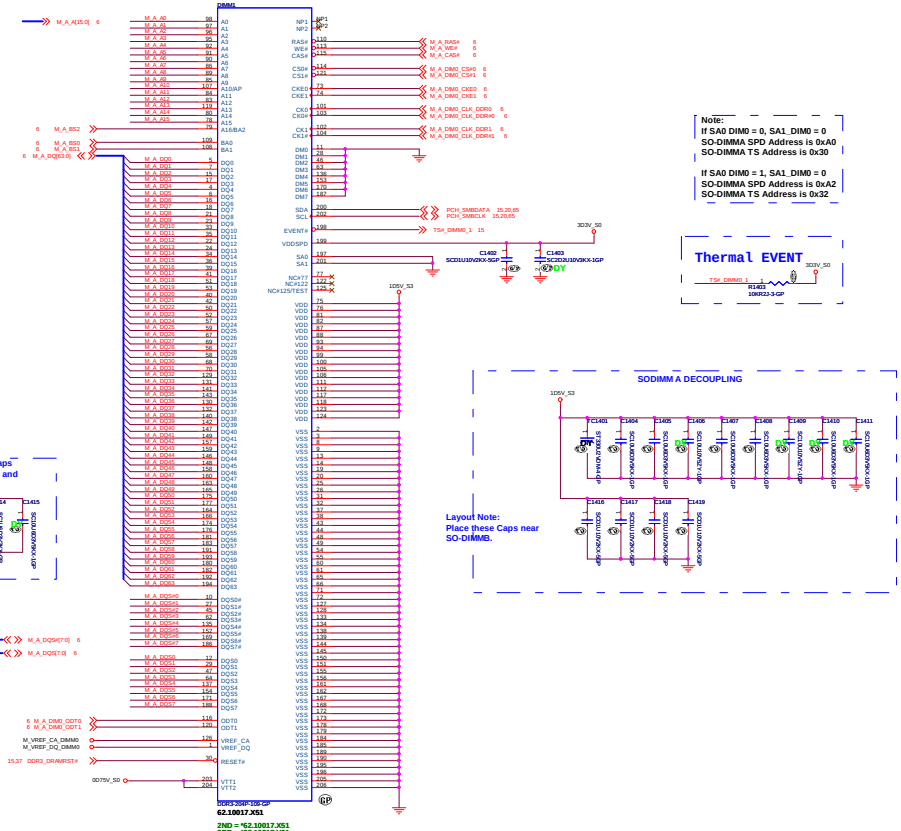
3D3V_PCIE_AOAC tie to I/O board WLAN, WWAN



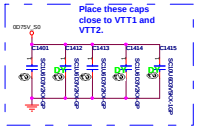
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AOAC***	
Size A4	Document Number **LSS-1**	Rev **1**
Date: Wednesday, February 22, 2012	Sheet 13 of 105	

SSID = MEMORY



Place these caps close to VTT1 and VTT2.



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

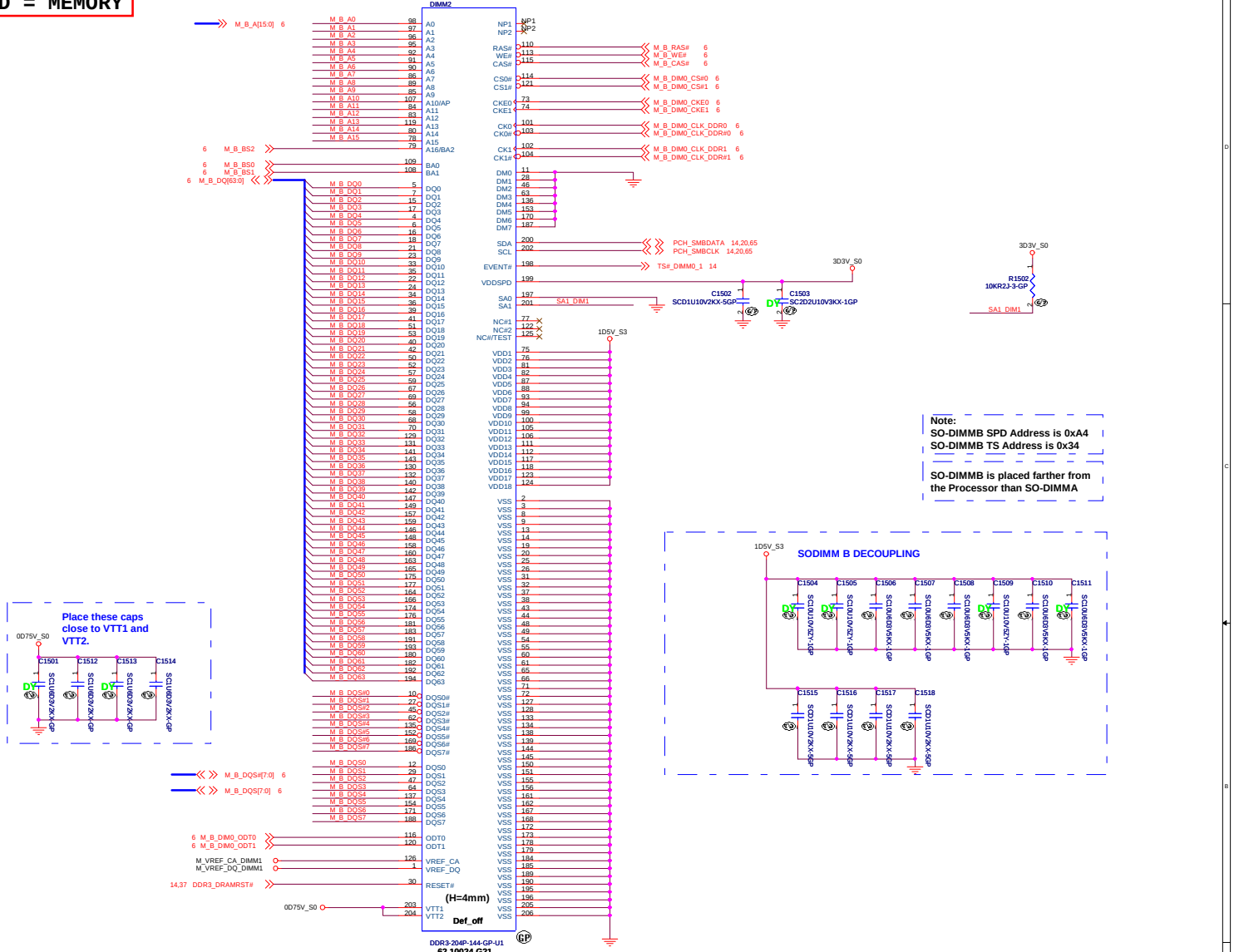
SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMM0.

<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR3-SODIMM1		
Size: C (Custom)	Document Number: LSS-1	Rev: 1
Date: Wednesday, February 22, 2012	Sheet 14 of 36	

SSID = MEMORY



Place these caps close to VTT1 and VTT2.

C1501 C1512 C1513 C1514

C1502 SCD1U10V2KX-5GP

C1503 SC2D2U10V3KX-1GP

R1502 10KR2J-3-GP

SODIMM B DECOUPLING

C1504 C1505 C1506 C1507 C1508 C1509 C1510 C1511

C1515 C1516 C1517 C1518

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: Custom | Document Number: LSS-1 | Rev: 1

Date: Wednesday, February 22, 2012 | Sheet 15 of 105

BLANK

<Variant Name>

緯創資通

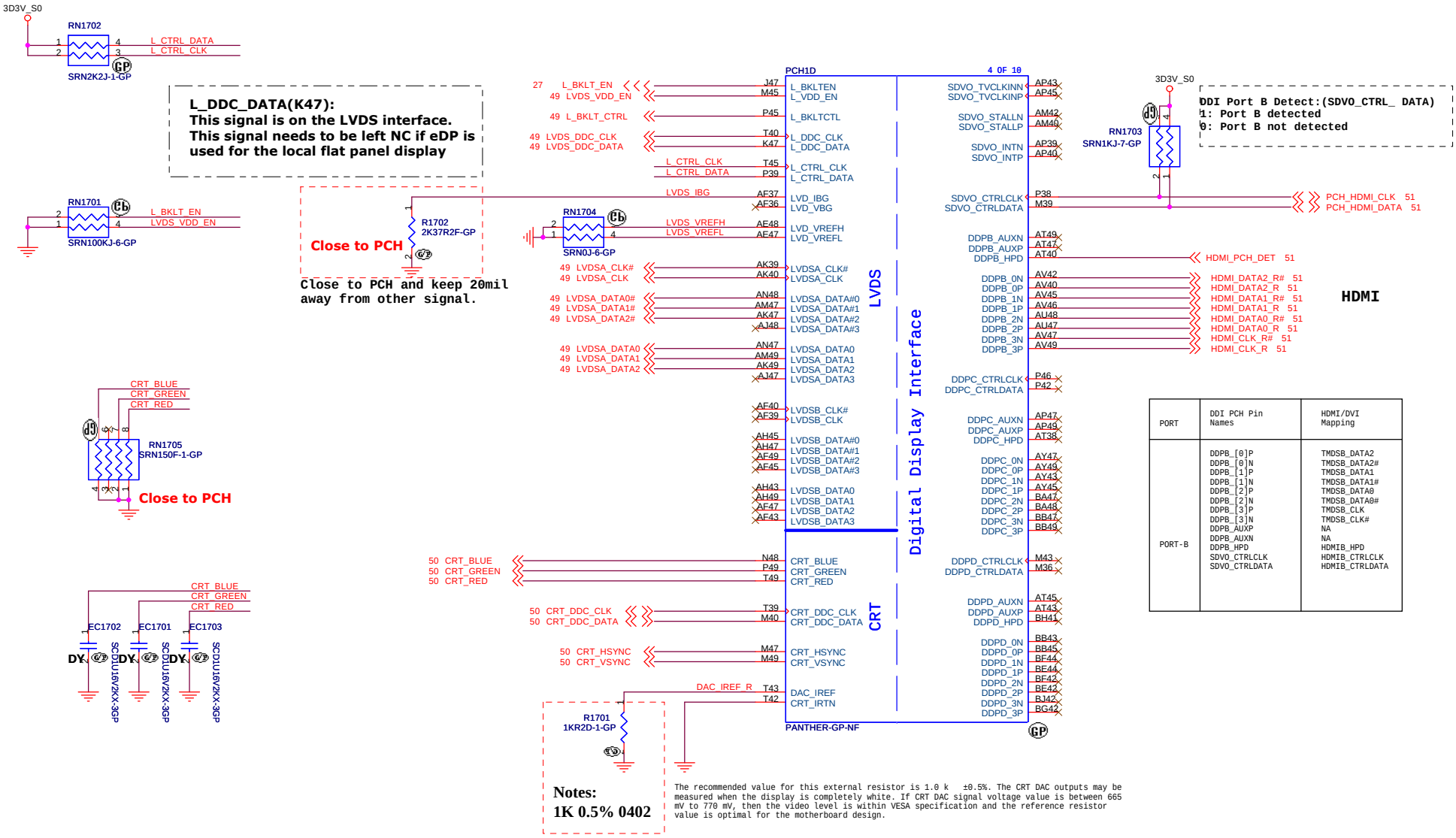
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DDR3-SODIMM2

Size	Document Number	Rev
A4	**LSS-1**	**1**

Date: Friday, February 10, 2012 Sheet 16 of 105



PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-B	DDPB_[0]P DDPB_[0]N DDPB_[1]P DDPB_[1]N DDPB_[2]P DDPB_[2]N DDPB_[3]P DDPB_[3]N DDPB_AUXP DDPB_AUXN DDPB_HPD SDVO_CTRLCLK SDVO_CTRLDATA	TMDSB_DATA2 TMDSB_DATA2# TMDSB_DATA1 TMDSB_DATA1# TMDSB_DATA0 TMDSB_DATA0# TMDSB_CLK TMDSB_CLK# NA NA HDMIB_HPD HDMIB_CTRLCLK HDMIB_CTRLDATA

<Variant Name>

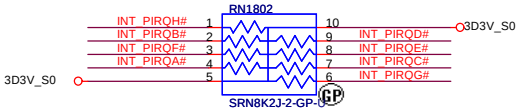
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

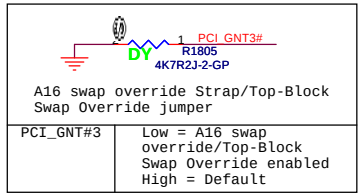
Title: PCH : LVDS/CRT/DDI

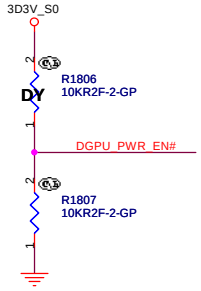
Size	Document Number	Rev
A3	LSS-1	1

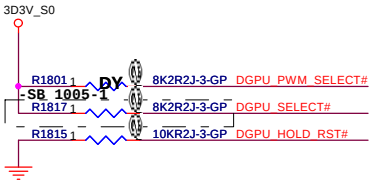
Date: Wednesday, February 22, 2012 Sheet 17 of 105

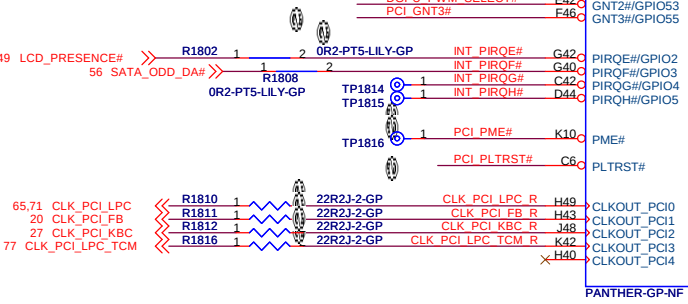
SSID = PCH

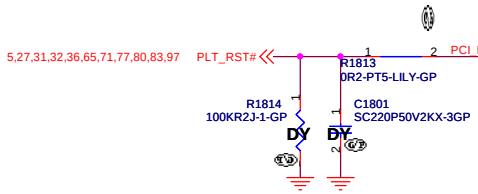


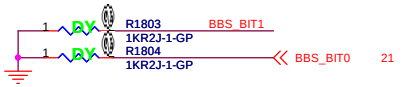












BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

Gx8 USB Table

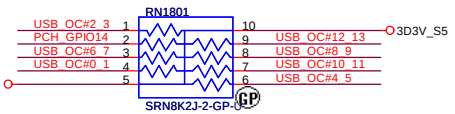
Pair	Device
0	X
1	USB3.0, ext port1
2	USB2.0, ext port4
3	USB3.0, ext port2
4	Bluetooth
5	X
6	X
7	X
8	X
9	USB2.0, ext port3
10	Finger Print
11	Mini Card1 (Bluetooth)
12	CAMERA
13	X

USB3.0 ext port 1 (OC0#)
USB2.0 ext port 4 (OC1#)
USB3.0 ext port 2 (OC2#)
Bluetooth

USB2.0 ext port 3 (OC4#)
Fingerprint
Mini Card1 (Bluetooth)
CAMERA

USB 2.0 Overcurrent Pin Default Usage			
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0# OC1# OC2# OC3#	Port 0, Port 1 Port 2, Port 3 Port 4, Port 5 Port 6, Port 7	OC4# OC5# OC6# OC7#	Port 8, Port 9 Port 10, Port 11 Port 12, Port 13 Not Used

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : PCI/USB/NVRAM/RSVD

Size	Document Number	Rev
A3	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 18 of 105

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

PCH1C — 3 OF 10

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

Platforms supporting Deep S4/S5, but not wishing to participate in the handshake during wake and Deep S4/S5 entry may tie SUSACK# to SUSWARN#.

SUS_ACK#: For non-DWS platforms, this signal can be left unconnected. Due to the internal pull-up on this signal it will be pulled high in order for the boot sequence to proceed.

SYS_PWROK: the system is ready to start the exit from reset (de-asserts PLT_RST# to the processor)

PWROK: it indicates to PCH that its CORE well power is stable.

Active Sleep Well (ASW) Power OK

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

-SB 1004-1

84.2N702.A3F
2nd = 84.DM601.03F

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : DMI/FDI/PM

Size	Document Number	Rev
A3	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 19 of 105

SSID = PCH

If PCIE port 1 is disabled, it will cause all PCIE port disabled

PCH1B — 2 OF 10

PCI-E*: PERN1/PERP1 WWAN; PERN2/PERP2 WLAN; PERN3/PERP3 Card Reader; PERN4/PERP4 LAN; PERN5/PERP5; PERN6/PERP6; PERN7/PERP7; PERN8/PERP8; PETN1/PETP1; PETN2/PETP2; PETN3/PETP3; PETN4/PETP4; PETN5/PETP5; PETN6/PETP6; PETN7/PETP7; PETN8/PETP8

SMBUS: SMBALERT#/GPIO11 (E12) EC_SW# → EC_SWI# 27; SMBCLK (H14) SMB_CLK → SMB_CLK 80; SMBDATA (C9) SMB_DATA → SMB_DATA 80; SML0ALERT#/GPIO60 (A12) DRAMRST_CNTRL_PCH → DRAMRST_CNTRL_PCH 12,37; SML0CLK (C8) SML0_CLK; SML0DATA (G12) SML0_DATA; SML1ALERT#/PCHHOT#/GPIO74 (C13) PCH_GPIO74; SML1CLK/GPIO58 (E14) SML1_CLK → SML1_CLK 27,86; SML1DATA/GPIO75 (M16) SML1_DATA → SML1_DATA 27,86

Controller Link: CL_CLK1 (M7) CL_CLK → TP2002; CL_DATA1 (T11) CL_DATA → TP2003; CL_RST1# (P10) CL_RST# → TP2001

CLOCKS: CLKOUT_PCIE0N/P; PCIECLKRQ0#/GPIO73; CLKOUT_PCIE1N/P; PCIECLKRQ1#/GPIO18; CLKOUT_PCIE2N/P; PCIECLKRQ2#/GPIO20; CLKOUT_PCIE3N/P; PCIECLKRQ3#/GPIO25; CLKOUT_PCIE4N/P; PCIECLKRQ4#/GPIO26; CLKOUT_PCIE5N/P; PCIECLKRQ5#/GPIO44; CLKOUT_PEG_B_N/P; PEG_B_CLKRQ#/GPIO56; CLKOUT_PCIE6N/P; PCIECLKRQ6#/GPIO45; CLKOUT_PCIE7N/P; PCIECLKRQ7#/GPIO46; CLKOUT_ITPXDP_N/P

FLEX CLOCKS: CLKOUTFLEX0/GPIO64 (K43) PCH_GPIO64; CLKOUTFLEX1/GPIO65 (F47) PCH_GPIO65; CLKOUTFLEX2/GPIO66 (H47) PCH_GPIO66; CLKOUTFLEX3/GPIO67 (K49) DGPU_PRSNT#

PEG_A_CLKRQ#/GPIO47 (M10) PEG_CLKREQ# → PEG_CLKREQ# 83

CLKOUT_PEG_A_N/P (AB37/AB38) → RN2017 OPS SRN0J-6-GP → CLK_PCIE_VGA# 83, CLK_PCIE_VGA 83

CLKOUT_DMI_N/P (AV22/AU22) → CLK_EXP_N 5, CLK_EXP_P 5

CLKOUT_DP_N/P (AM12/AM13)

CLKIN_DMI_N/P (BF18/BE18) CLK_BUF_EXP_N/P → RN2001 SRN10KJ-5-GP

CLKIN_GND1_N/P (BJ30/BG30) CLK_BUF_CPYCLK_N/P → RN2010 SRN10KJ-5-GP

CLKIN_DOT_96N/P (G24/E24) CLK_BUF_DOT96_N/P → RN2011 SRN10KJ-5-GP

CLKIN_SATA_N/P (AK7/AK5) CLK_BUF_CKSSCD_N/P → RN2012 SRN10KJ-5-GP

REFCLK14IN (K45) CLK_BUF_REF14

CLKIN_PCILOOPBACK (H45) CLK_PCI_FB → CLK_PCI_FB 18

XTAL25_IN (V47) / XTAL25_OUT (V49)

XCLK_RCOMP (Y47) XCLK_RCOMP → R2011 90D9R2F-1-GP → 1D05V_VTT

PANTHER-GP-NF

WLAN CLK

65 PCIE_RXN2 / 65 PCIE_RXP2 / 65 PCIE_TXN2 / 65 PCIE_TXP2 → C2006 / C2002 SCD1U10V2KX-5GP → PCIE_TXN2_C / PCIE_TXP2_C

Card Reader CLK

32 PCIE_RXN3 / 32 PCIE_RXP3 / 32 PCIE_TXN3 / 32 PCIE_TXP3 → C2003 / C2009 SCD1U10V2KX-5GP → PCIE_TXN3_C / PCIE_TXP3_C

LAN CLK

31 PCIE_RXN4 / 31 PCIE_RXP4 / 31 PCIE_TXN4 / 31 PCIE_TXP4 → C2001 / C2005 SCD1U10V2KX-5GP → PCIE_TXN4_C / PCIE_TXP4_C

3D3V_S0 — RN2015 SRN10KJ-5-GP: CLKREQ_MCC# / PCIE_CLK_WLAN_REQ#

PCIECLKRQ1# and PCIECLKRQ2# Support S0 power only

PCIE_CLK_RQ0# → J2

RN2007 SRN0J-6-GP: 65 CLK_PCIE_WLAN# / 65 CLK_PCIE_WLAN → CLK_PCH_SRC1_N (AB49) / CLK_PCH_SRC1_P (AB47)

65 PCIE_CLK_WLAN_REQ# → M1

RN2008 SRN0J-6-GP: 32 CLK_PCIE_MCC# / 32 CLK_PCIE_MCC → CLK_PCH_SRC2_N (AA48) / CLK_PCH_SRC2_P (AA47)

32 CLKREQ_MCC# → V10

RN2009 SRN0J-6-GP: 31 CLK_PCIE_LAN# / 31 CLK_PCIE_LAN → CLK_PCH_SRC3_N (Y37) / CLK_PCH_SRC3_P (Y36)

31 PCIE_CLK_LAN_REQ# → A8

3D3V_S5 — RN2013 SRN10KJ-5-GP: CLK_PCIE_NEW_REQ# / PCIE_CLK_LAN_REQ# / PCIE_CLK_RQ5# / PCIE_CLK_RQ4#

RN2014 SRN10KJ-5-GP: EC_SWI# / PCIE_CLK_RQ0# / PEG_B_CLKRQ#

3D3V_S0 — RN2016 SRN10KJ-5-GP: PCH_GPIO64 / PCH_GPIO65 / PCH_GPIO66

-SB 1013-3

PCIE_CLK_RQ4# → L12

PCIE_CLK_RQ5# → L14

PEG_B_CLKRQ# → E6

PCIE_CLK_RQ6# → T13

CLK_PCIE_NEW_REQ# → K12

TP2015 / TP2016: PCIE_CLK_XDP_N (AK14) / PCIE_CLK_XDP_P (AK13) → CLKOUT_ITPXDP_N/P

3D3V_S5 — RN2002 SRN2K2J-1-GP: SMB_CLK / SMB_DATA

RN2003 SRN2K2J-1-GP: SML0_DATA / SML0_CLK

RN2004 SRN2K2J-1-GP: SML1_CLK / SML1_DATA

RN2005 SRN10KJ-5-GP: PCIE_CLK_RQ6# / PCH_GPIO74

DRAMRST_CNTRL_PCH → R2001 1KR2J-1-GP

3D3V_S0 — RN2006 SRN2K2J-1-GP

Q2001 2N7002KDW-GP — SMB_DATA → PCH_SMBDATA 14,15,65; SMB_CLK → PCH_SMBCLK 14,15,65

84.2N702.A3F

2nd = 84.DM601.03F

XTAL25_IN / XTAL25_OUT — X2001 XTAL 25MHZ-155-GP — C2007 / C2008 SC15P50V2JN-2-GP — R2005 1M1R2J-GP

82.30020.D41

2nd = 82.30020.G71

3rd = 82.30020.G61

-SC 1209-2

R2004 0R2-PT5-LILY-GP

3D3V_S5 — R2002 10KR2J-3-GP; PEG_CLKREQ# R — R2003 10KR2J-3-GP DY

UMA_DISCRETE#

UMA: 1 1

DIS :0 1

SG(PX) : 0 0

Optimus(Muxless) : 1 0

3D3V_S0 — R2006 10KR2J-3-GP UMA; R2007 10KR2J-3-GP — UMA_DIS# / DGPU_PRSNT# → UMA_DIS# 22

R2008 10KR2J-3-GP DY; R2009 10KR2J-3-GP OPS

CLK_BUF_REF14 → R2010 10KR2J-3-GP

<Variant Name>

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

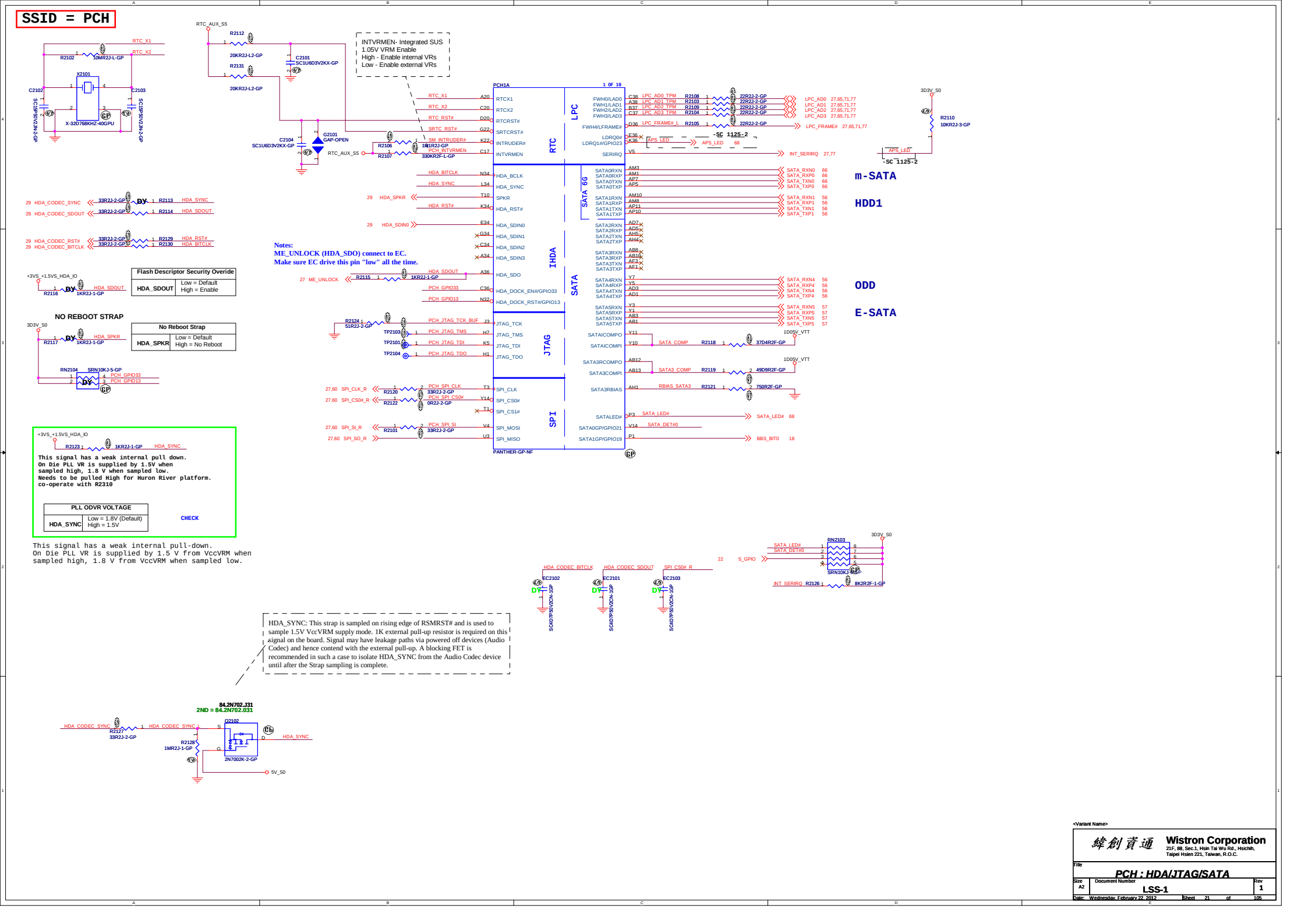
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : PCIE/SMBUS/CLK

Size: A3 | Document Number: LSS-1 | Rev: 1

Date: Wednesday, February 22, 2012 | Sheet 20 of 105

SSID = PCH



Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

CHECK

This signal has a weak internal pull-down.
On Die PLL VR is supplied by 1.5 V from VccVRM when sampled high, 1.8 V from VccVRM when sampled low.

Notes:
ME_UNLOCK (HDA_SDO) connect to EC.
Make sure EC drive this pin "low" all the time.

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<variant_name>

Title: PCH : HDA/JTAG/SATA

Size: A2 | Document Number: LSS-1 | Rev: 1

Date: Wednesday, February 22, 2012 | Sheet 21 of 105

Note:
For PCH debug with XDP, need to NO STUFF R2218

PCH1F

PANTHER-GP-NF

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2229 UNSTUFFED) DEFAULT DISABLED -- LOW (R2229 STUFFED)

GPIO28 has a weak[20K] internal pull up. To enable on-die PLL Voltage regurator, should not place external pull down.

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2225 DY)- DISABLED [DEFAULT] LOW (R2225)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

R2211 BOM CTRL
HR:1K
CRV:DY

PROCPWRGD (PCH) --> UNCOREPOWRGOOD (CPU)
Indicates that VccSA, VDDQ, VccA (1.0V) and VccIO power supplies are stable. This signal will be asserted only after PWROK assertion.

<Variant Name>

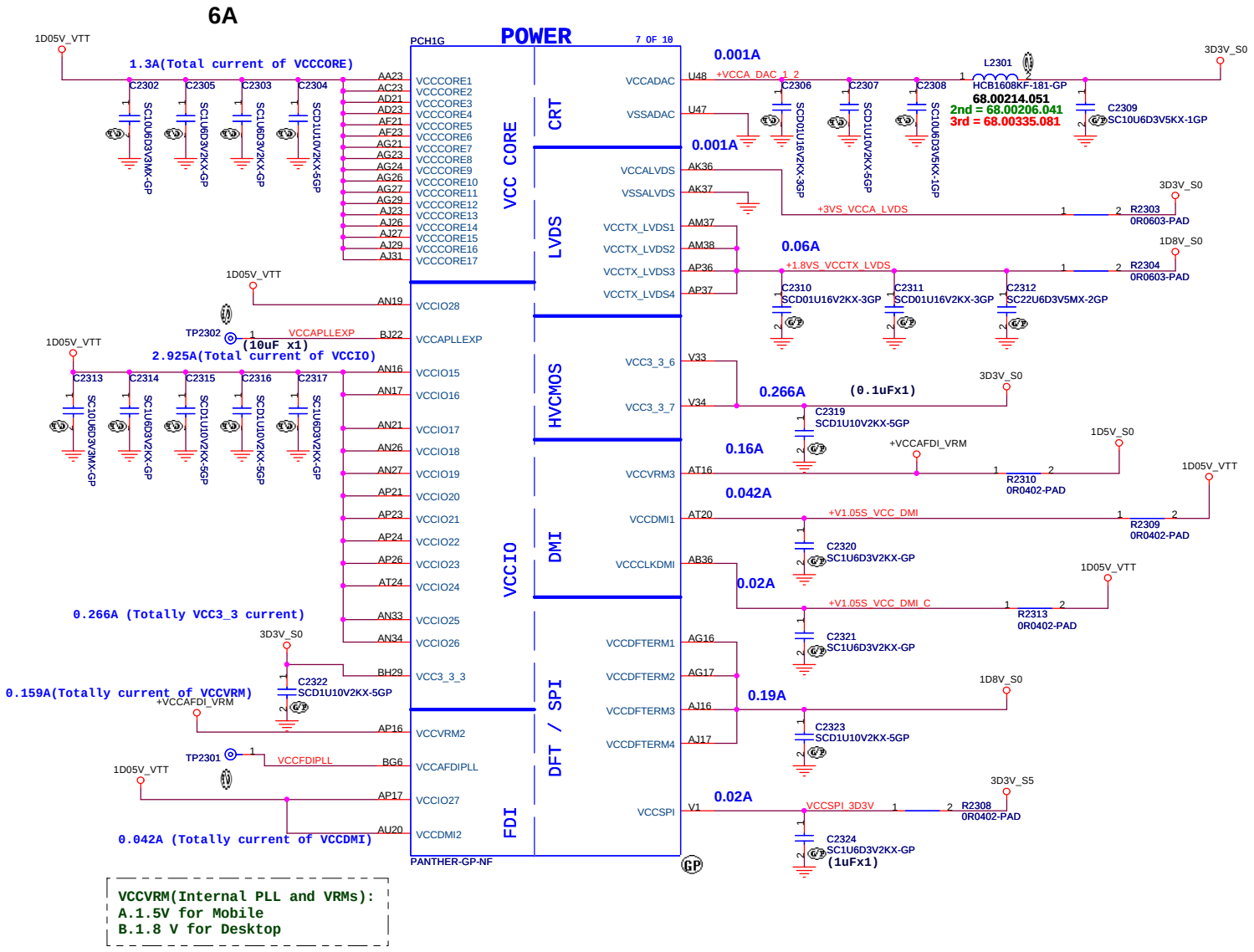
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : GPIO/NTCF/MISC

Size	Document Number	Rev
A2	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 22 of 105

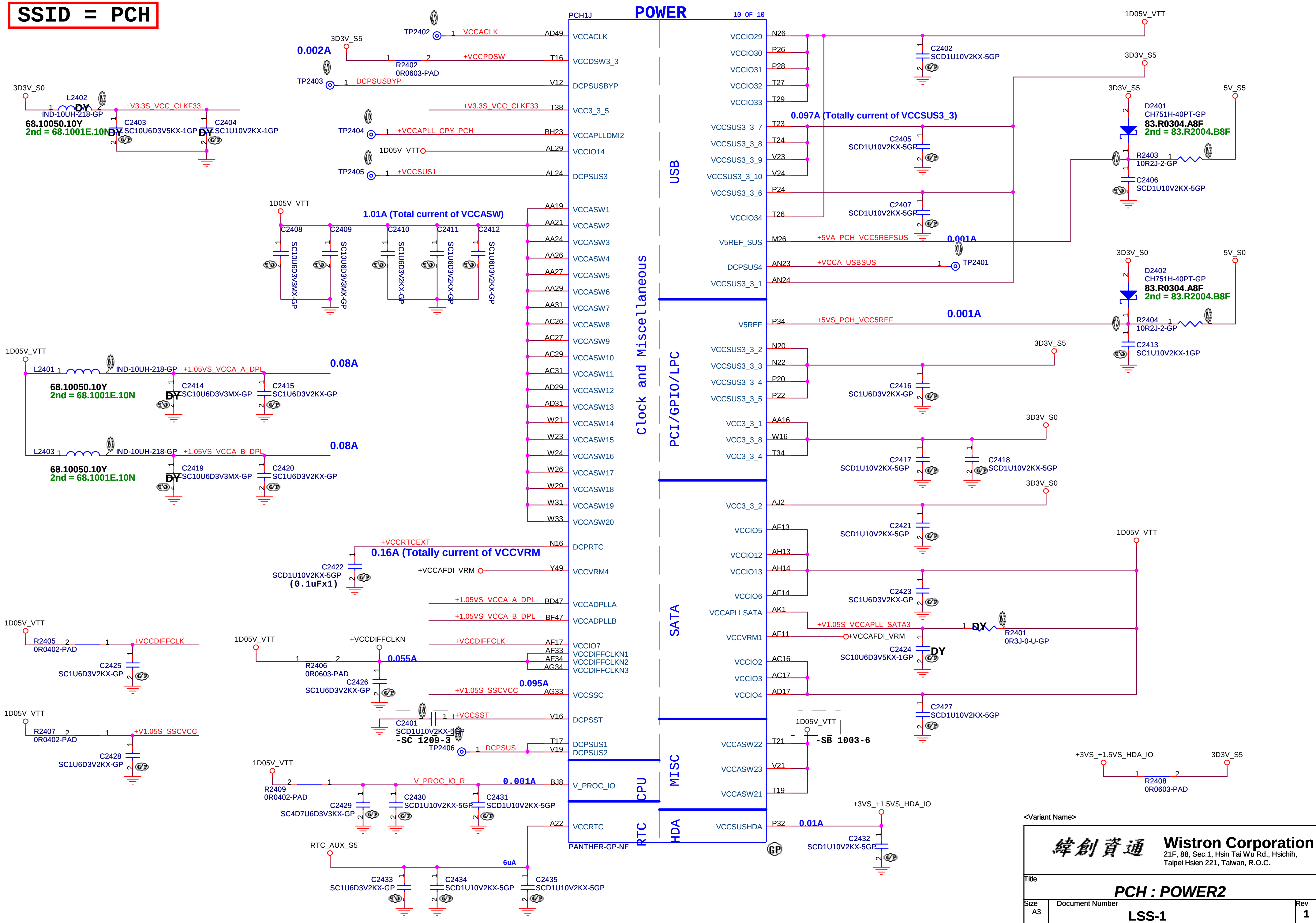
SSID = PCH



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**PCH : POWER1**	
Size A3	Document Number **LSS-1**	Rev 1
Date: Tuesday, February 14, 2012	Sheet 23 of 105	

SSID = PCH



<Variant Name>

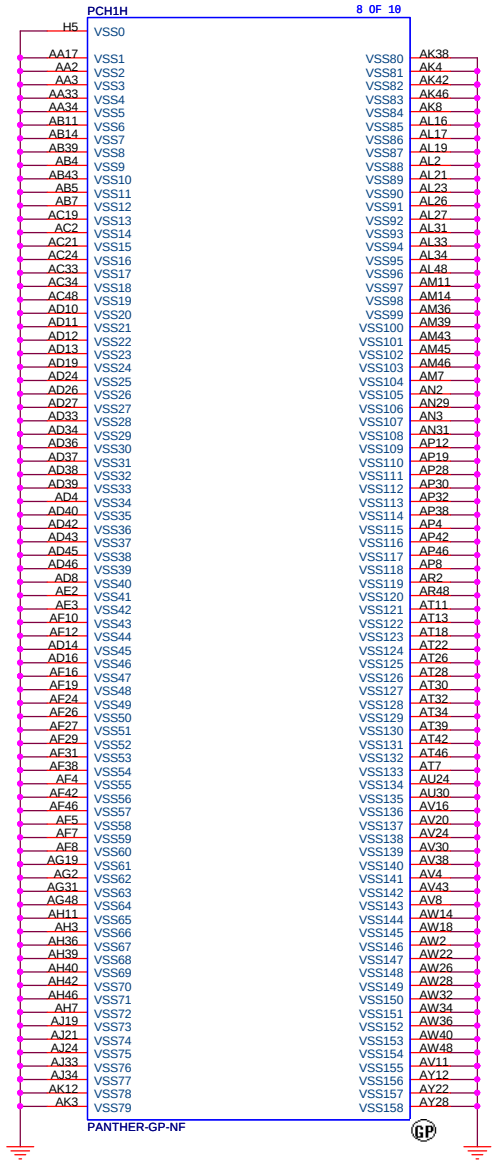
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

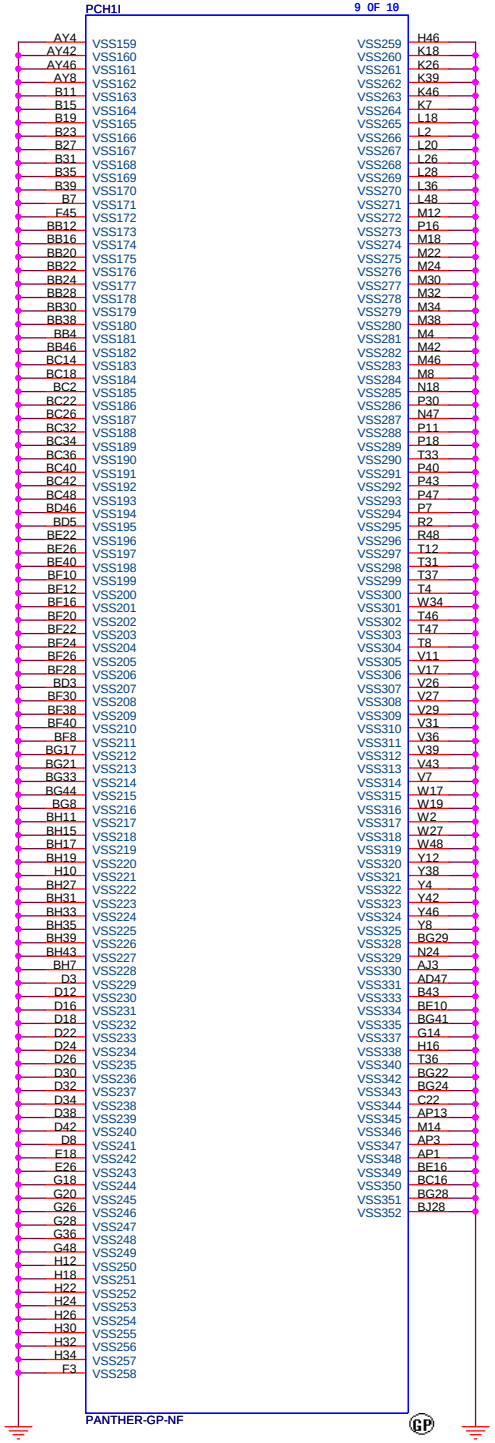
Title: **PCH : POWER2**

Size	Document Number	Rev
A3	LSS-1	1

Date: Tuesday, February 14, 2012 Sheet 24 of 105

SSID = PCH





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH : VSS***

Size	Document Number	Rev
A3	LSS-1	1

Date: Friday, February 10, 2012 Sheet 25 of 105

BLANK

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LSS-1	1

Date: Friday, February 10, 2012 Sheet 26 of 105

SSID = KBC

65W_90W#
High: 65W / Low 90W

SC 1205-6
For LED issue

SC 1205-7
For AD_OFF issue

SC 1125-5

SC 1125-3

SC 1125-4

R2720 and C2716
Need very close to EC

<------ TP
<------ BATTERY / CHARGER
<------PCH / eDP

EC_GPIO47 High Active

Reset IC: Prevent BIOS data loss solution

EC GPIO standard PH/PL

MODEL_ID_AD (Pin100)	Pull Down	Pull High	Voltage
UMA (LGN-1)	100.0K	10.0K	3.0V
UMA (LLP-1)	100.0K	20.0K	2.75V
OPTIMUS (LLP-1)	100.0K	33.0K	2.48V
UMA (LSS-1)	100.0K	47.0K	2.24V
OPTIMUS (LSS-1)	100.0K	64.9K	2.0V

PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

71.00885.A0G
IC EMB CTRL NPCE885PA0DX LQFP 128P

<Variant Name>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

<Title>

Size: A1 | Document Number: LSS-1 | Rev: 1

Date: Wednesday, February 22, 2012 | Sheet 27 of 185

SSID = Thermal

Thermal sensor

Close to SO-DIMM on top side.

SA 0905 change to 390p

3
Q2801
MMBT3904WT1G-GP
C2804
SC390P50V2KX-GP

2200p close to smsc2103 chip

2
Q2803
MMBT3904WT1G-GP
C2805
SC390P50V2KX-GP DY
C2806
SC2200P50V2KX-2GP
REMOTE2-
REMOTE2+

LK430 : Close to GPU
LK230 : Close to PCH

T8

1
Q2802
MMBT3904WT1G-GP
C2802
SC390P50V2KX-GP
2200p close to smsc2103 chip
C2803
SC2200P50V2KX-2GP
H_THERMDA
H_THERMDC

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width
and spacing. Locate Capacity near Thermal diode.

20110718_Carrey:
For Vendor suggestion, add 10k pull high to 3D3V_S0

3D3V_S0
R2801
10KR2J-3-GP
THERM_SCI#

3D3V_S0
R2804
6K8R2J-GP
SHDN_SEL

SHDN --> 2N3904 ON External diode

3D3V_S0
R2806
68R2-GP
U2801
C2808
SCD1U10V2KX-4GP
2103_VDD
VDD
DP1
DN1
DP2/DN3
ND2/DP3
SYS_SHDN#
ALERT#
SMCLK
SMDATA
GPIO1
GPIO2
TACH
PWM
TRIP_SET
SHDN_SEL
GND
GND
EMC2103-2-AP-GP
H_THERMDA
H_THERMDC
REMOTE2+
REMOTE2-
THERM_SYS_SHDN#
THERM_SCI# R
THERM_SCI#
TP2804
R2808
0R2-PT5-LILY-GP
27 SMBC_THERM
27 SMBD_THERM
2103_4
2103_5
TP2802
TP2803
RN2801
SRN10KJ-5-GP
3D3V_S0
FAN_TACH_1
D2801
FAN_TACH
FAN_PWM
TRIP_SET R2807
649R2F-GP
SHDN_SEL
T8 = 98
TRIP_SET: 649 ohm => 87 dgree C
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.5R003.08F
3rd = 83.R5003.G8F

pin6, ALERT# OD
pin7, SYS_SHDN# OD

4 WIRE PWM Fan Control circuit

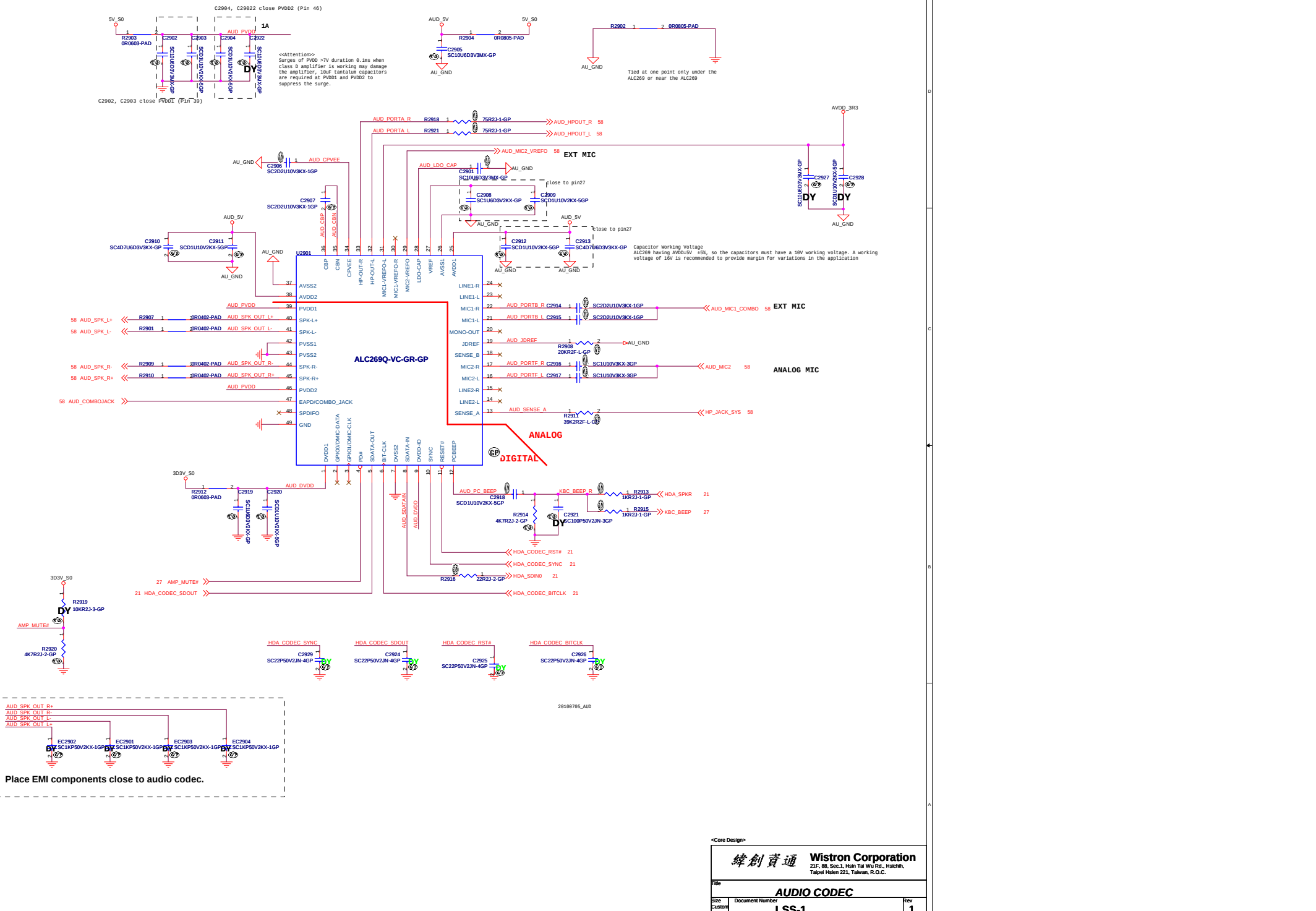
5V_S0
C2807
SC4D7U6D3V3KX-GP
R2802
10KR2J-3-GP
R2803
0R0603-PAD
FAN_TACH
FAN_PWM
5V_S0_FAN
FAN_PWM_C
R2805
0R2-PT5-LILY-GP
EC2801
SC1KP50V2KX-1GP
EC2802
SC1KP50V2KX-1GP
20100707_EMI
20.F0714.004
ACES-CON4-GP-U1
FAN1
TP2801
TP2805
TP2806
TP2807
FAN_PWM_C
FAN_TACH
5V_S0_FAN
GND

3D3V_AUX_S5
D2802
BAT54PT-GP
83.00054.T81
2ND = 83.BAT54.D81
3rd = 83.BAT54.S81
Q2804
2N7002K-2-GP
84.2N702.031
2ND = 84.2N702.J31
27,36 PURE_HW_SHUTDOWN#
R2812
10KR2J-3-GP
C2801
SCD1U10V2KX-5GP
THERM_SYS_SHDN#
IMVP_PWRGD_T
3D3V_S0
R2809
100KR2J-1-GP
R2810
0R2-PT5-LILY-GP
R2811
0R2J-2-GP
IMVP_PWRGD 36,42

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL SENSOR SMSC EMC2103
Size: A3
Document Number: LSS-1
Rev: 1
Date: Wednesday, February 22, 2012
Sheet 28 of 105


C2904, C29022 close PVDD2 (Pin 46)
C2902, C2903 close PVDD1 (Pin 39)
<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.
Tied at one point only under the ALC269 or near the ALC269
EXT MIC
ANALOG MIC
ALC269Q-VC-GR-GP
ANALOG
DIGITAL
Capacitor Working Voltage
ALC269 having AVDD=5V ±5%, so the capacitors must have a 10V working voltage. A working voltage of 10V is recommended to provide margin for variations in the application
Place EMI components close to audio codec.
20100705_AUD
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CODEC
LSS-1
Wednesday, February 22, 2012
29
105

BLANK

<Variant Name>

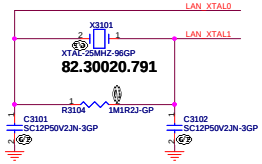
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

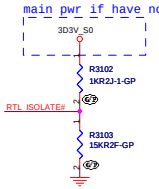
Title: ***Reserved***

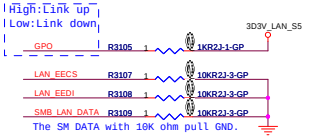
Size	Document Number	Rev
A4	LSS-1	1

Date: Friday, February 10, 2012 Sheet 30 of 105

25MHz XTAL



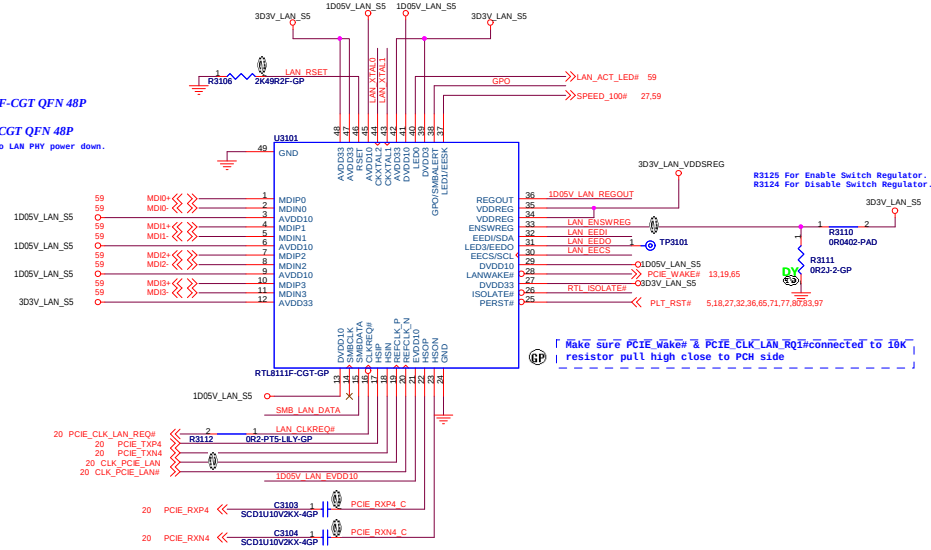


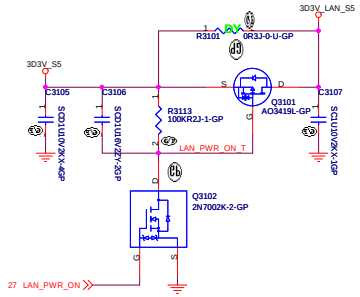


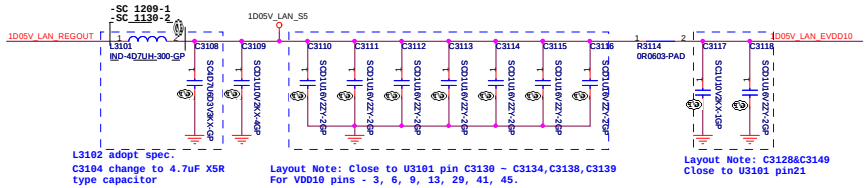
71.08111.N03, IC PCIE CTRL RTL8111F-CGT QFN 48P

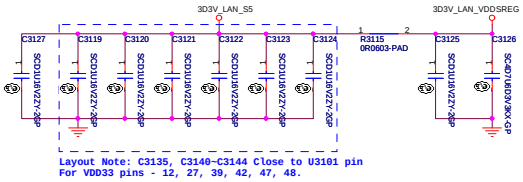
71.08111.J03, IC PCI-E RTL8111E-VL-CGT QFN 48P

8111F can use GPIO to inform system to do LAN PHY power down.









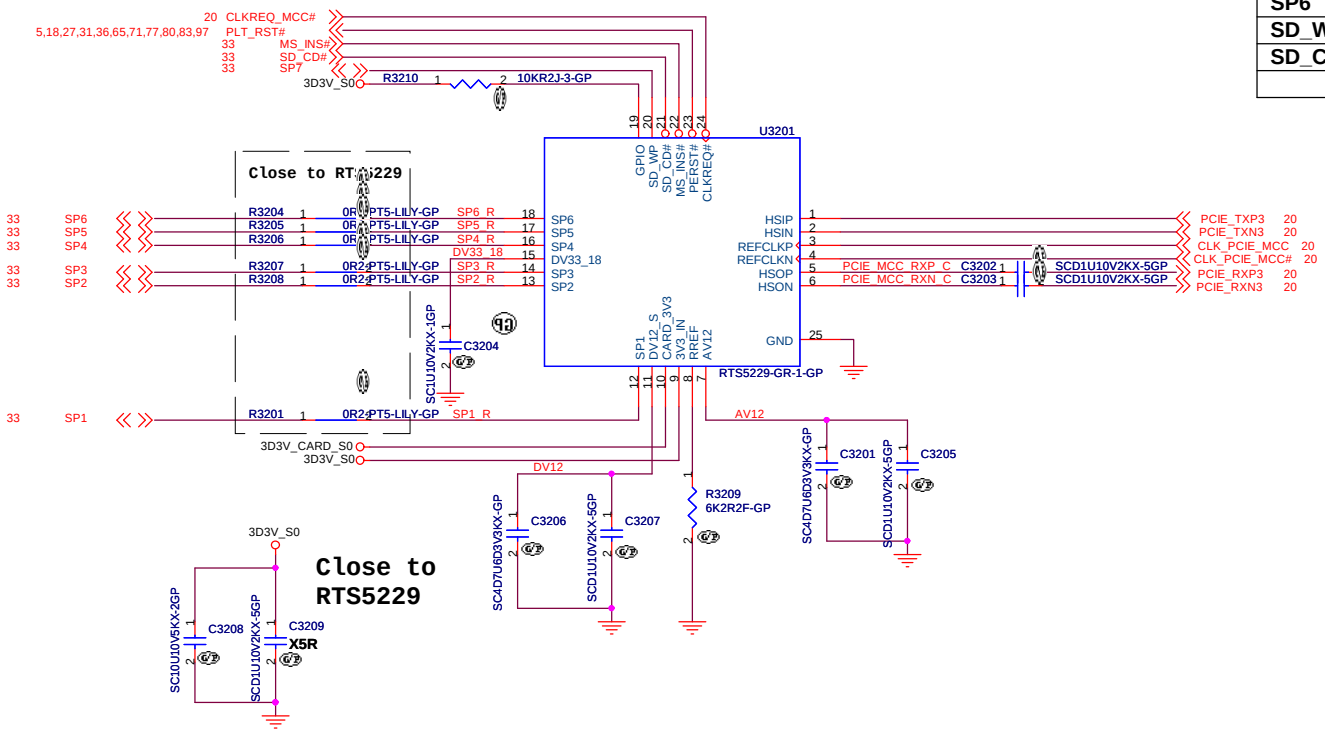
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Customer Name

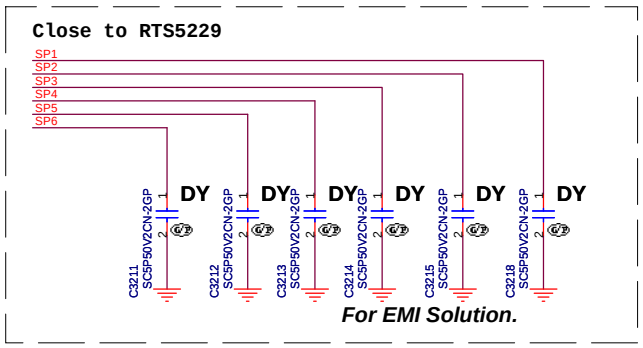
Title: LAN_RTL8111F

Size: A2 | Document Number: LSS-1 | Rev: 1

Date: Wednesday, February 22, 2012 | Sheet 31 of 105

SP_IO	SD/MMC	MS
SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SD_WP	SD_WP	MS_BS
SD_CD#		SD_CD#
	MS_INS#	MS_INS#





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

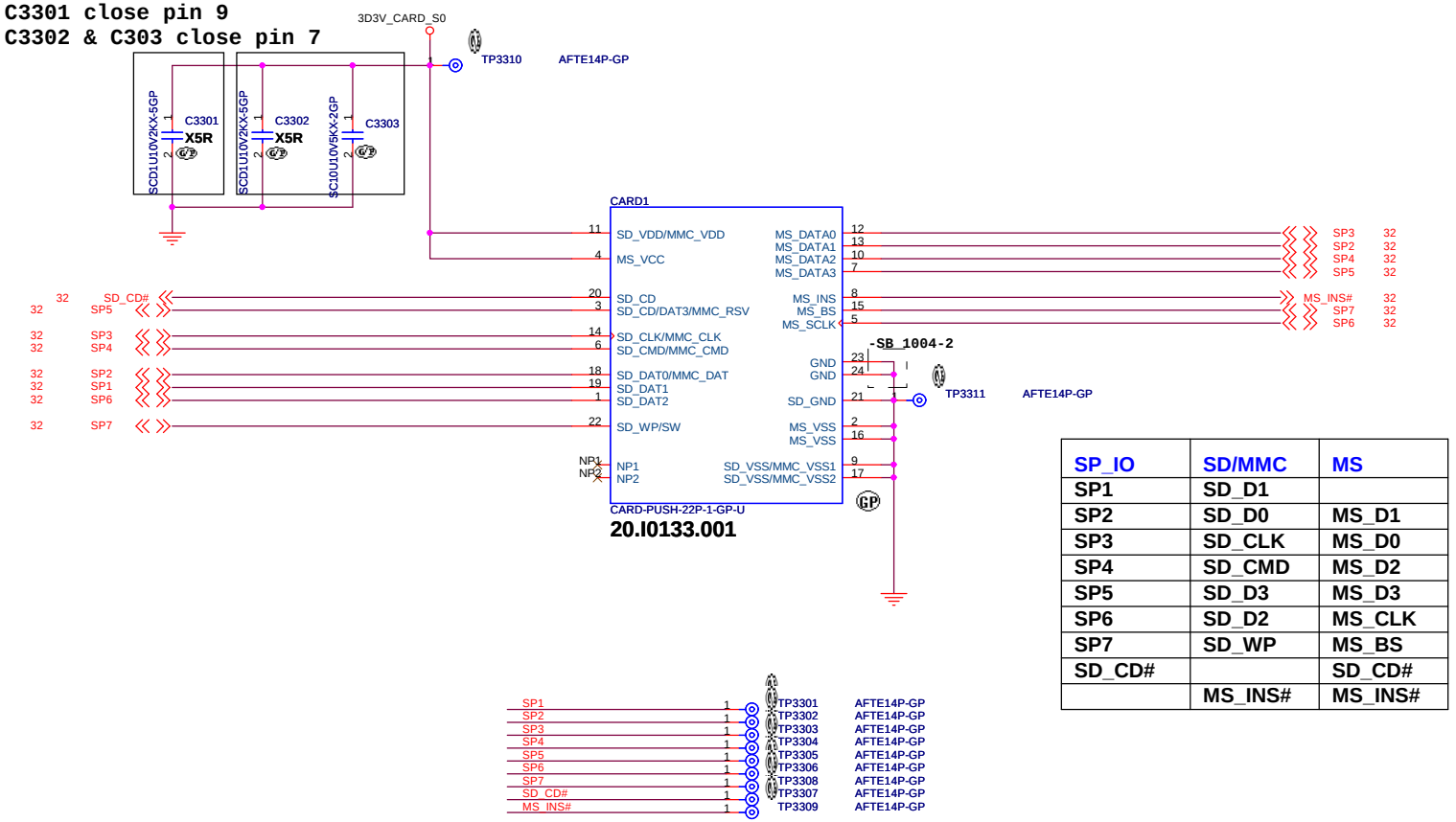
Title: Card Reader-RTS5229

Size	Document Number	Rev
A3	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 32 of 105

SD/MMC/MMC+ Card Reader

C3301 close pin 9
C3302 & C303 close pin 7



SP_IO	SD/MMC	MS
SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS
SD_CD#		SD_CD#
	MS_INS#	MS_INS#

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SD/MMC/MMC+ Card CONN***

Size	Document Number	Rev
A3	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 33 of 105

BLANK

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LSS-1	1

Date: Friday, February 10, 2012 Sheet 34 of 105

BLANK

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

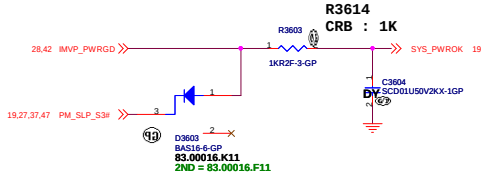
Title

USB 3.0 Controller

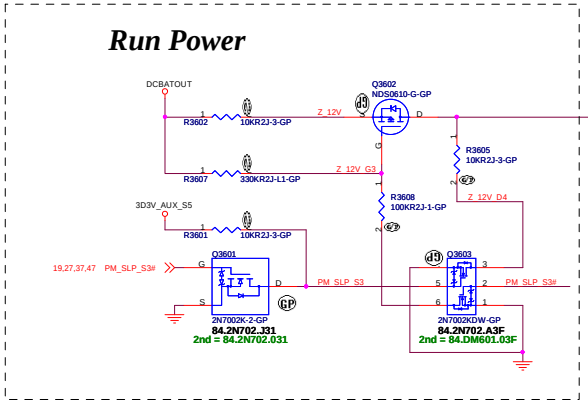
Size	Document Number	Rev
A4	LSS-1	1

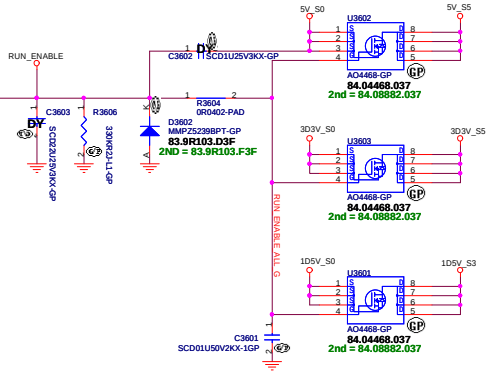
Date: Friday, February 10, 2012 Sheet 35 of 105

Power Sequence



Run Power

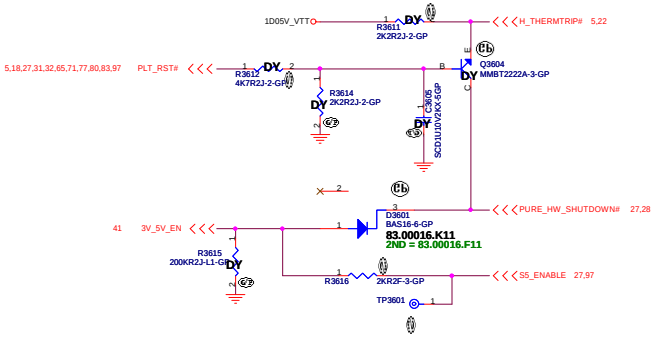


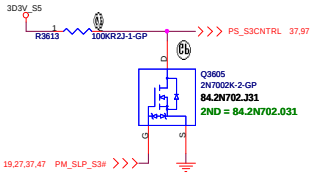


1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

-SB 1003-2





<Variant Name>

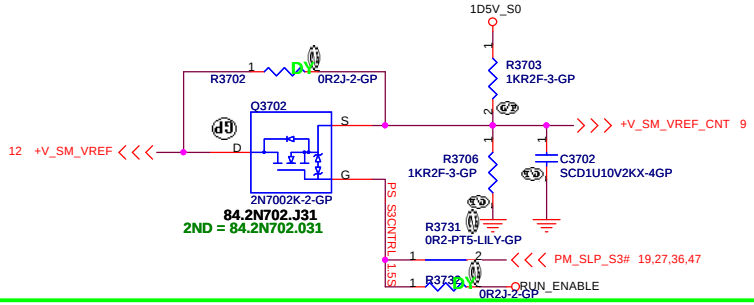
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Plane Enable***

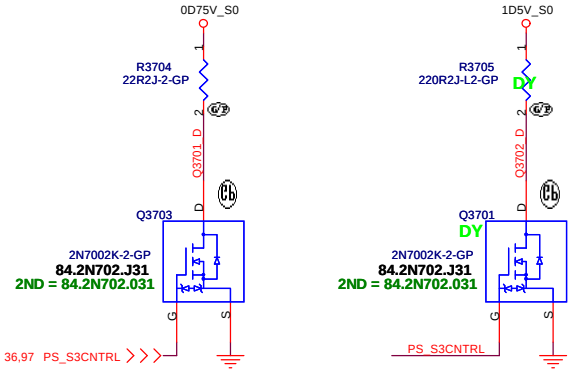
Size	Document Number	Rev
A2	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 36 of 105

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

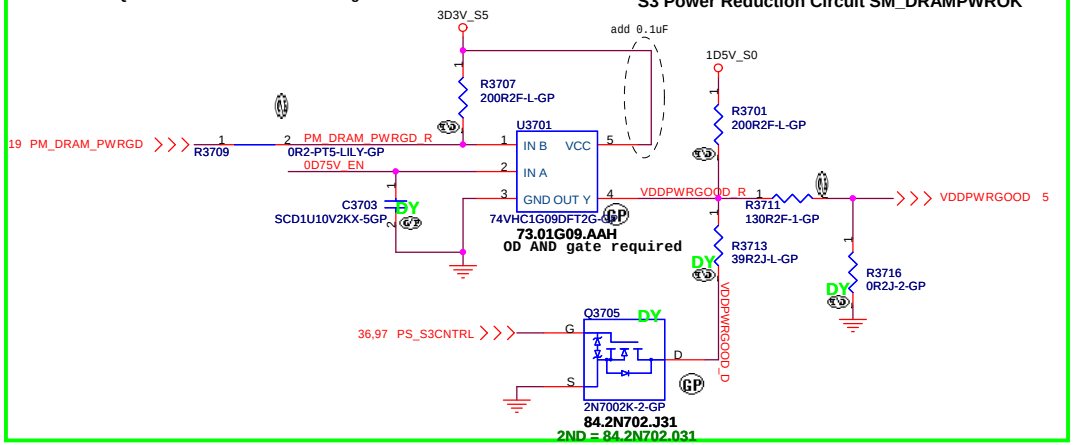


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

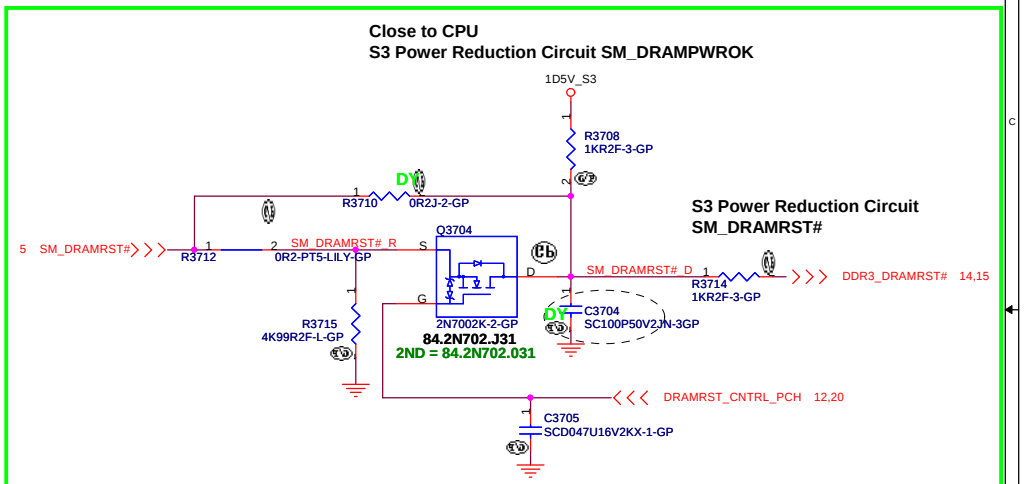


SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

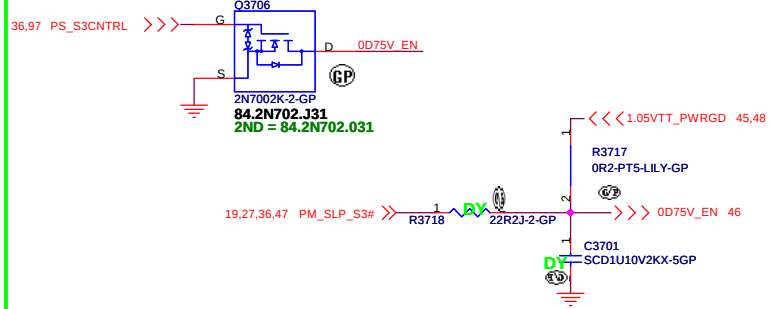


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



S3 Power Reduction Circuit
SM_DRAMRST#

5 S3 Power Reduction



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

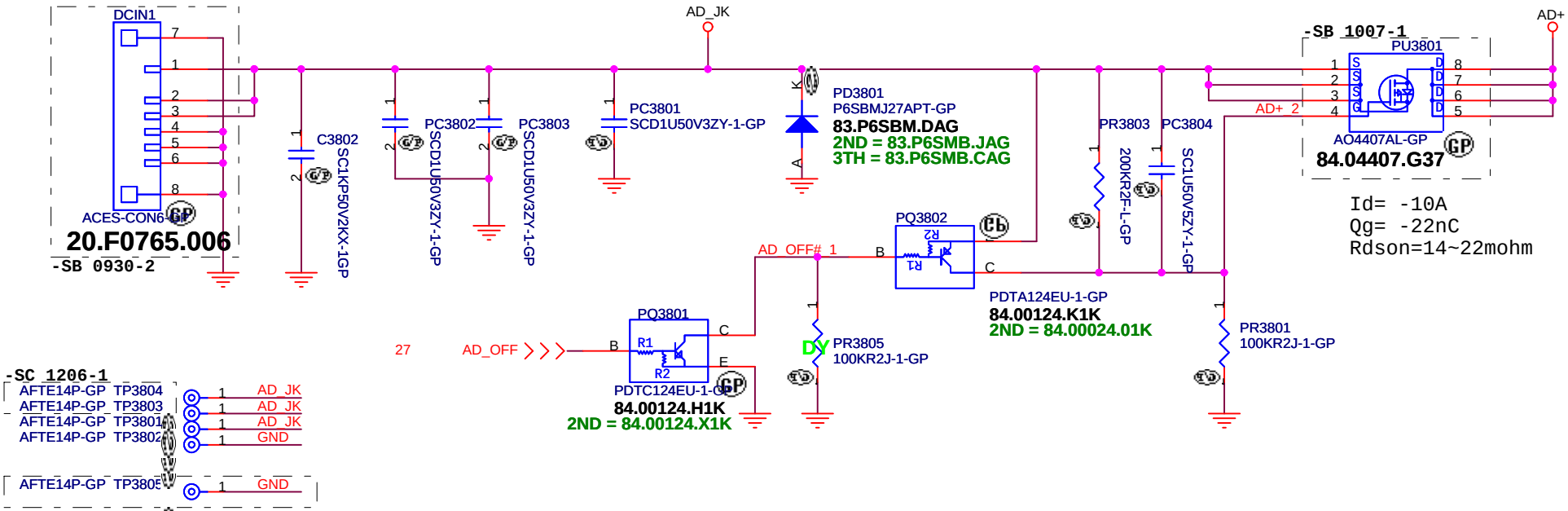
Title: ADAPTER

Size	Document Number	Rev
A3	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 37 of 105

CHECK Adaptor ID PIN

Adaptor in to generate DCBATOUT

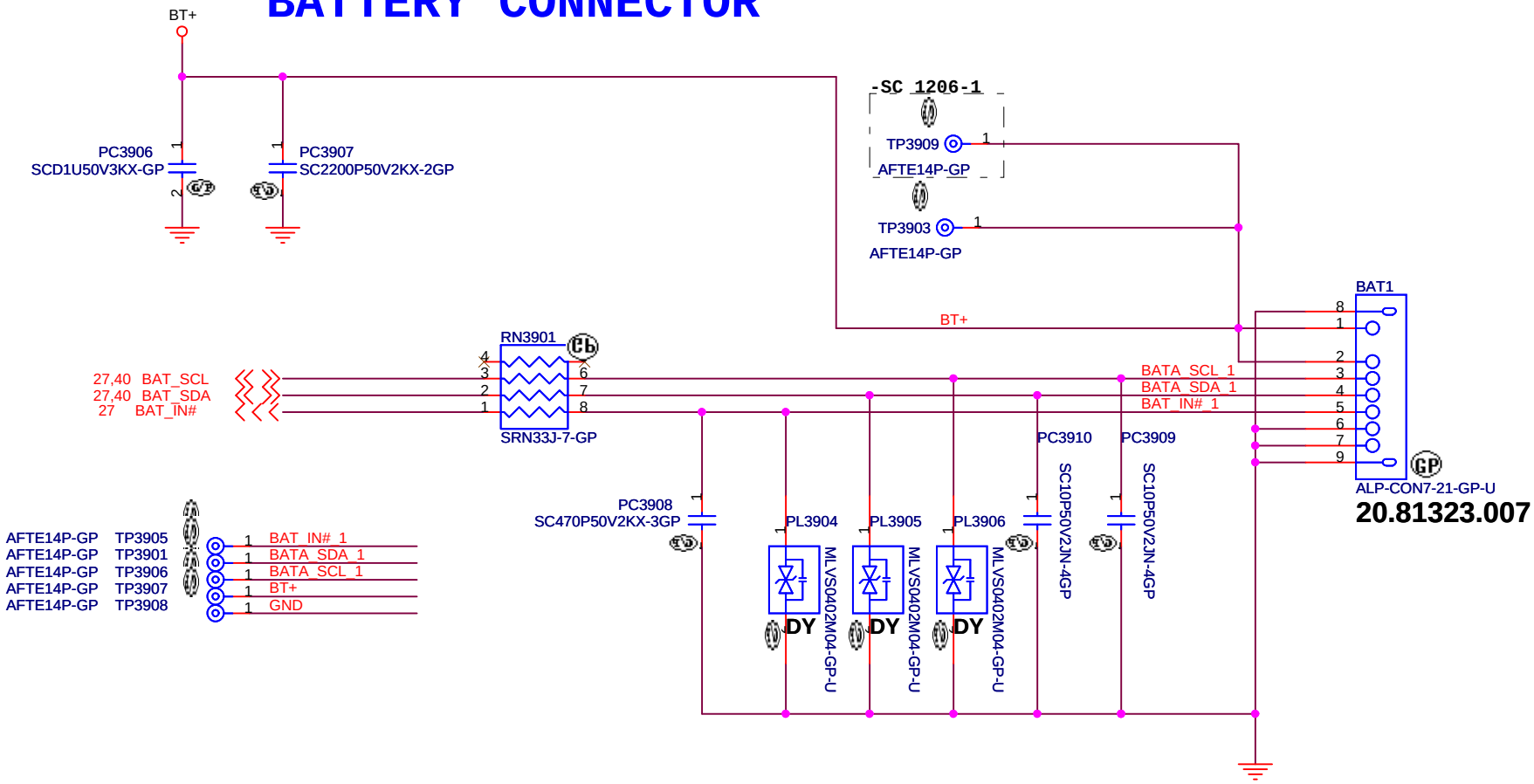


test point at bottom side

JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN_JACK*		
Size: A4	Document Number: LSS-1	Rev: 1
Date: Wednesday, February 22, 2012	Sheet 38 of 105	

BATTERY CONNECTOR



JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***BATT_CONN***	
Size	Document Number **LSS-1**	Rev **1**
Date: Wednesday, February 22, 2012	Sheet 39 of 105	

SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4008 R1:
UMA:64.12425.6DL
DIS:64.60425.6DL

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118K	100K

STOP_CHG# connects to KBC

Charger Current=1.4~3.6A

Cyntec.5.6uH 7*6.6*3mm
DCR=39~42mohm
Idc=5.5A, Isat=6.0A

PU4001 AO4407AL-GP 84.04407.G37
Id= -10A
Qg= -22nC
Rdson=14~22mohm

PU4002 AO4407AL-GP 84.04407.G37
Id= -10A
Qg= -22nC
Rdson=14~22mohm

PU4004 SIS412DN-T1-GE3-GP 84.00412.037
Id= -10A
Qg= -4.4nC
Rdson=23~31mohm

PU4005 SIS412DN-T1-GE3-GP 84.00412.037

PQ4001 2N7002KDW-GP 84.2N702.A3F
2nd = 84.DM601.03F

PU4003 BQ24737RGRR-GP

PL4001 IND-5D6UH-48-GP-U1 68.5R610.10L

PR4019 0R0402-PAD 83.R0203.08F
2nd = 83.1R003.I8F

PD4003 CH520S-30PT-GP

PQ4005 2N7002K-2-GP

PQ4007 2N7002K-2-GP

PQ4008 2N7002K-2-GP

<Variant Name>

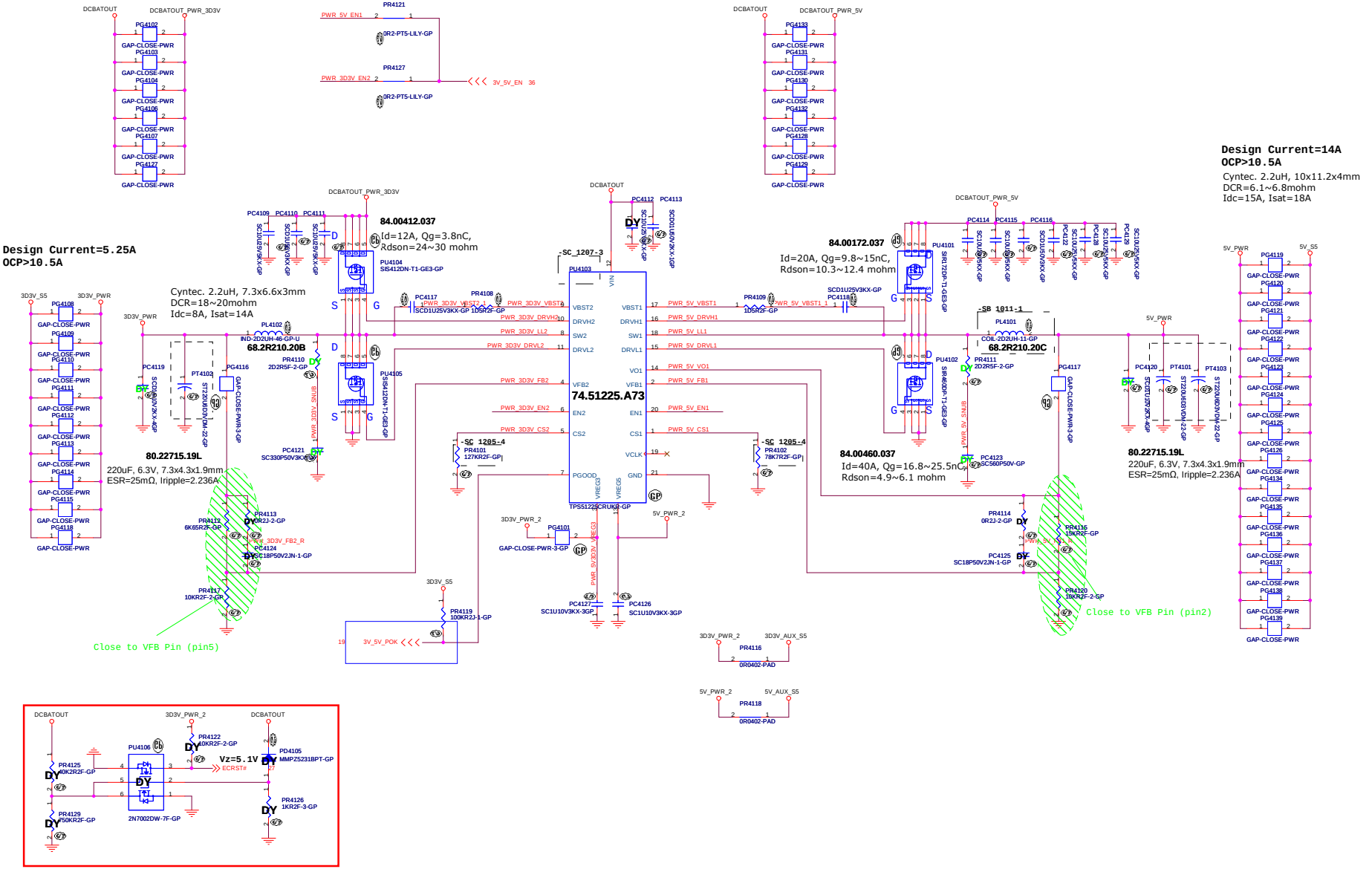
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: BQ24737_Charger

Size | Document Number: LSS-1 | Rev: 1

Date: Wednesday, February 22, 2012 | Sheet 40 of 105

SSID = PWR.Plane.Regulator_5v3p3v



JV10-CS

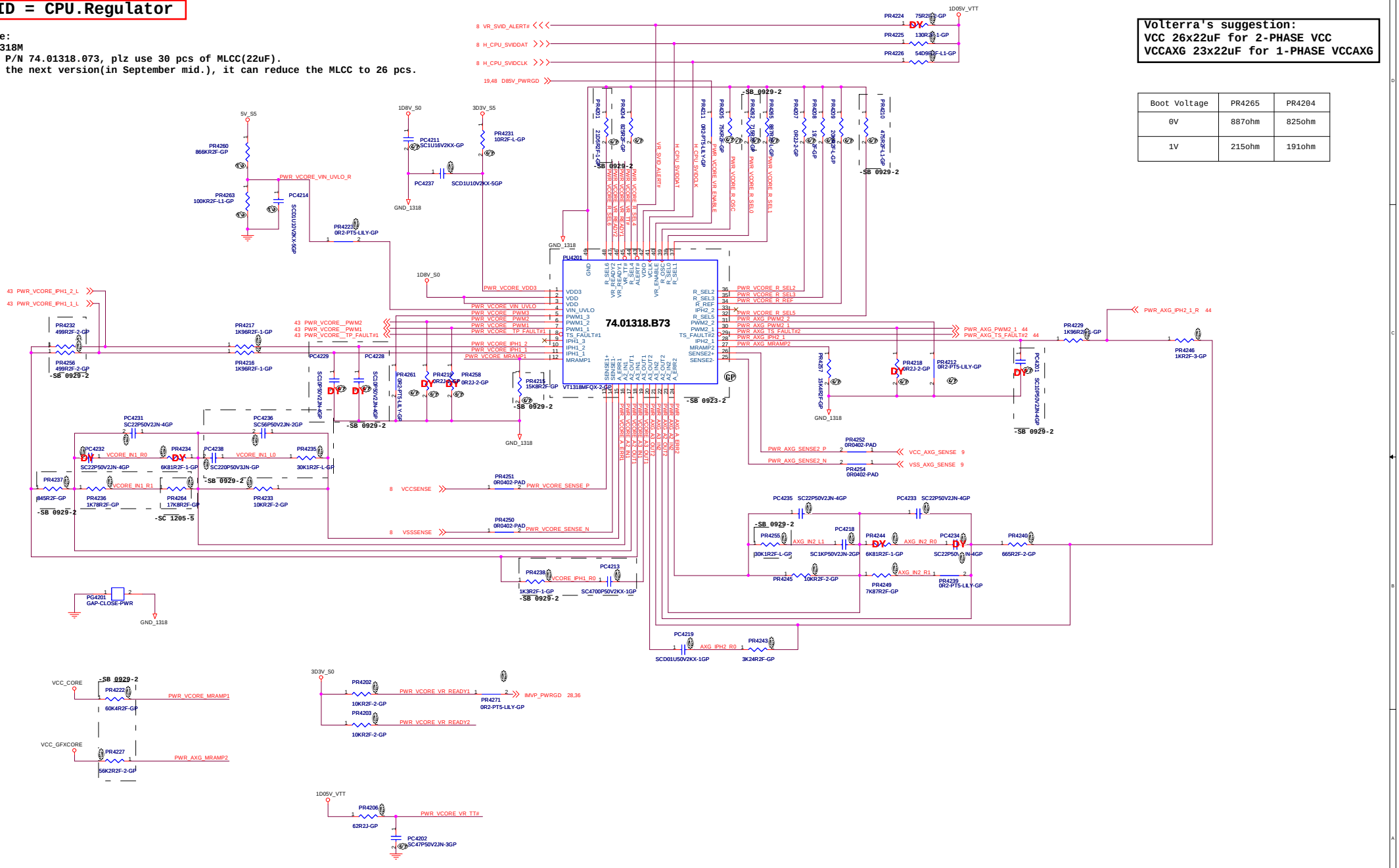
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TPS51225_5V_3D3V		
Size	Document Number: LSS-1	Rev: 1
Date: Wednesday, February 22, 2012	Sheet 41 of 105	

SSID = CPU.Regulator

Note:
VT1318M
For P/N 74.01318.073, plz use 30 pcs of MLCC(22uF).
For the next version(in September mid.), it can reduce the MLCC to 26 pcs.

Volterra's suggestion:
VCC 26x22uF for 2-PHASE VCC
VCCAXG 23x22uF for 1-PHASE VCCAXG

Boot Voltage	PR4265	PR4204
0V	887ohm	825ohm
1V	215ohm	191ohm



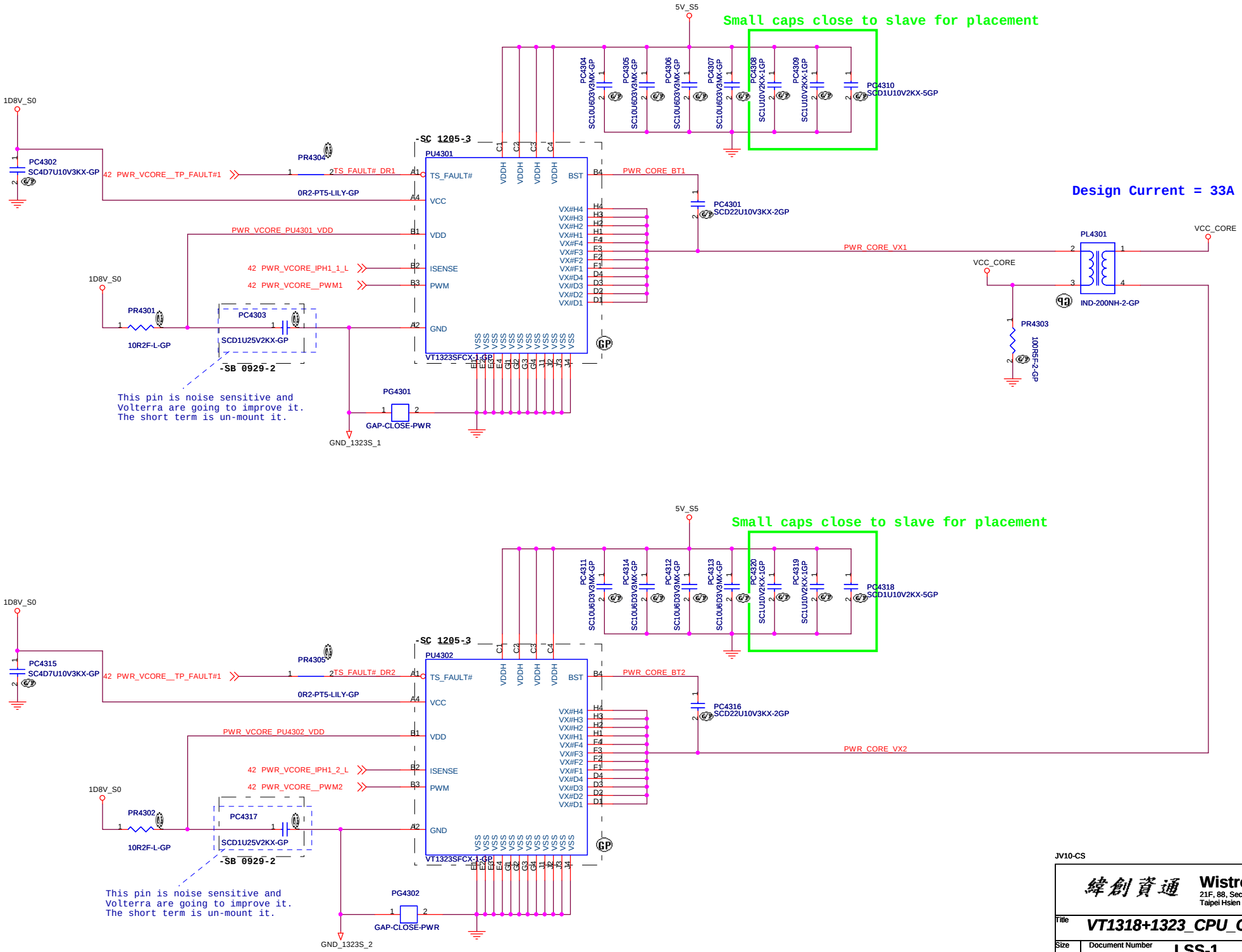
JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1318+1323_CPU_CORE2+1(1/3)

Size | Document Number: LSS-1 | Rev: 1

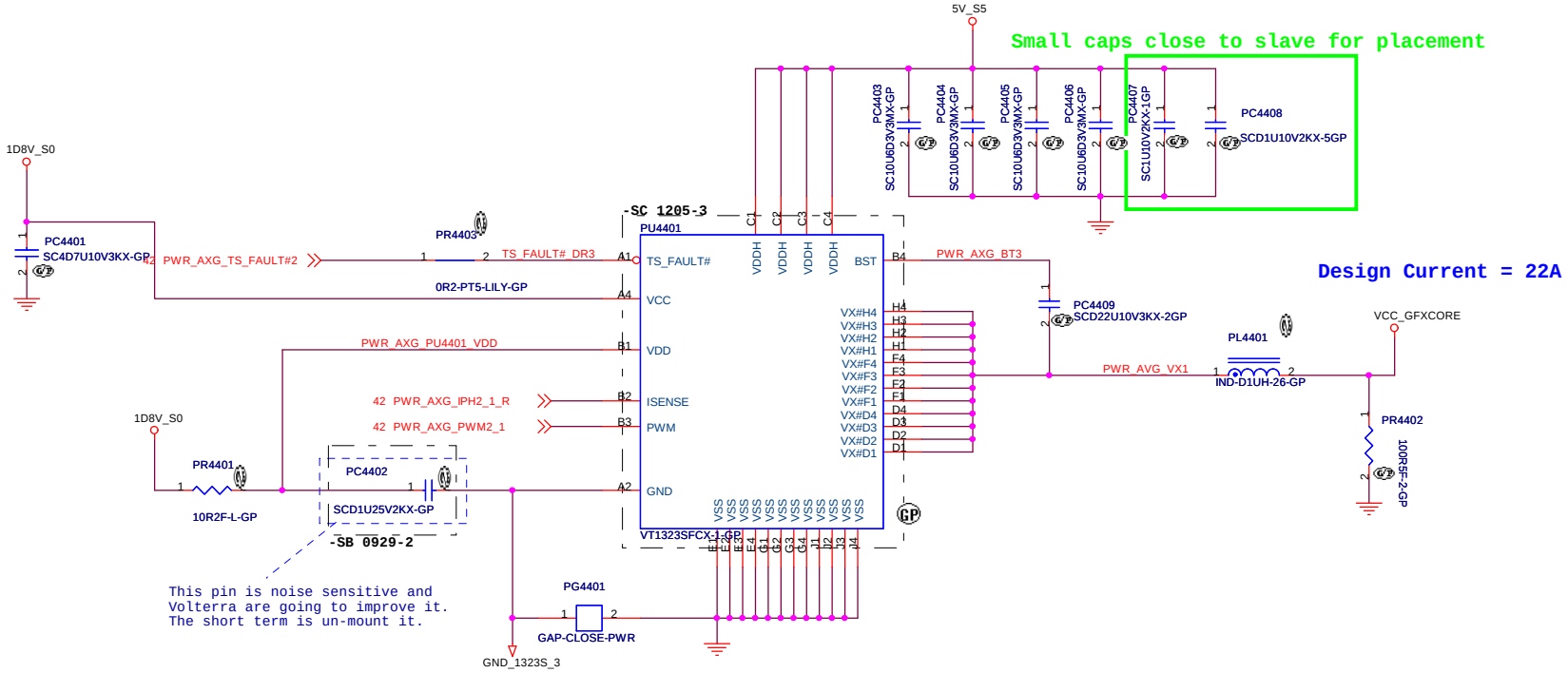
Date: Wednesday, February 22, 2012 | Sheet 42 of 105



JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

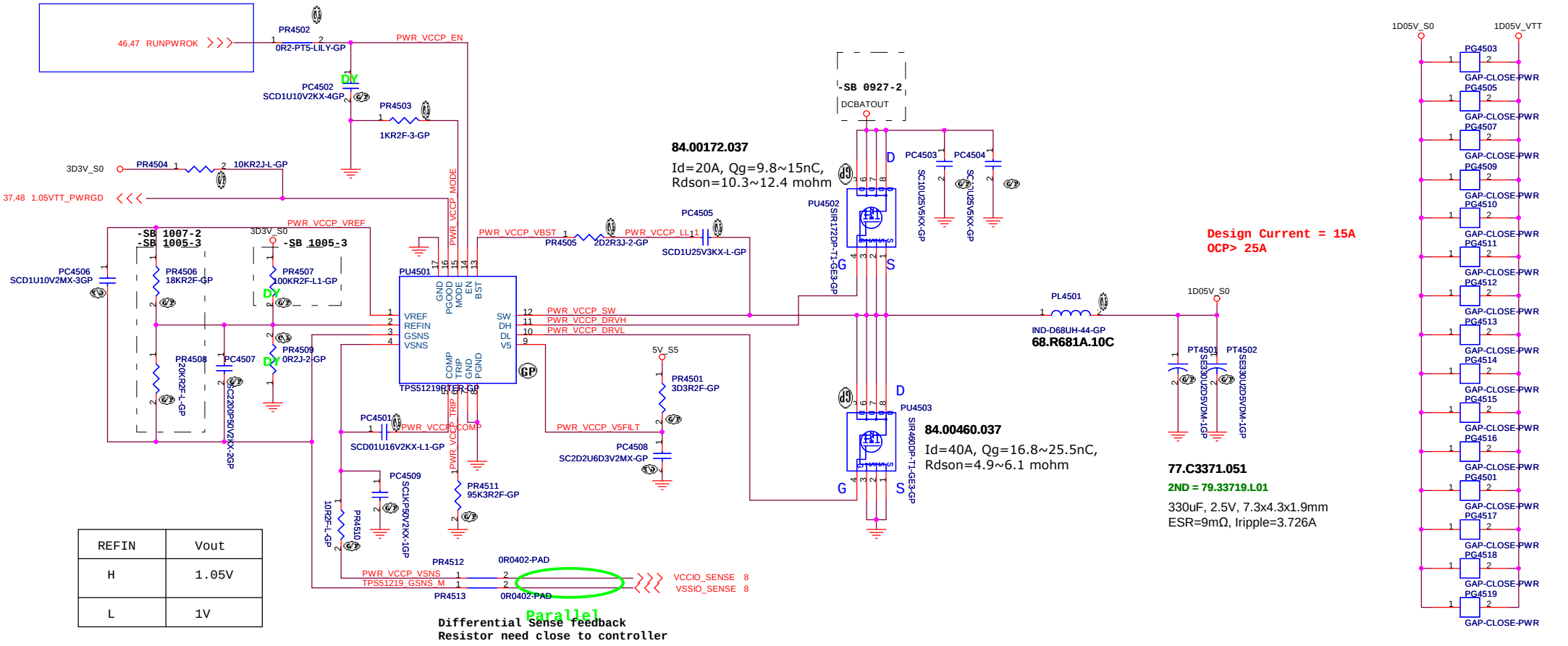
Title	VT1318+1323_CPU_CORE2+1(2/3)	
Size	Document Number LSS-1	Rev 1
Date: Wednesday, February 22, 2012	Sheet 43 of 105	



JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VT1318+1323_CPU_CORE2+1(3/3)***	
Size	Document Number **LSS-1**	Rev **1**
Date: Wednesday, February 22, 2012	Sheet 44 of 105	

TPS51219 for 1D05V



REFIN	Vout
H	1.05V
L	1V

Parallel

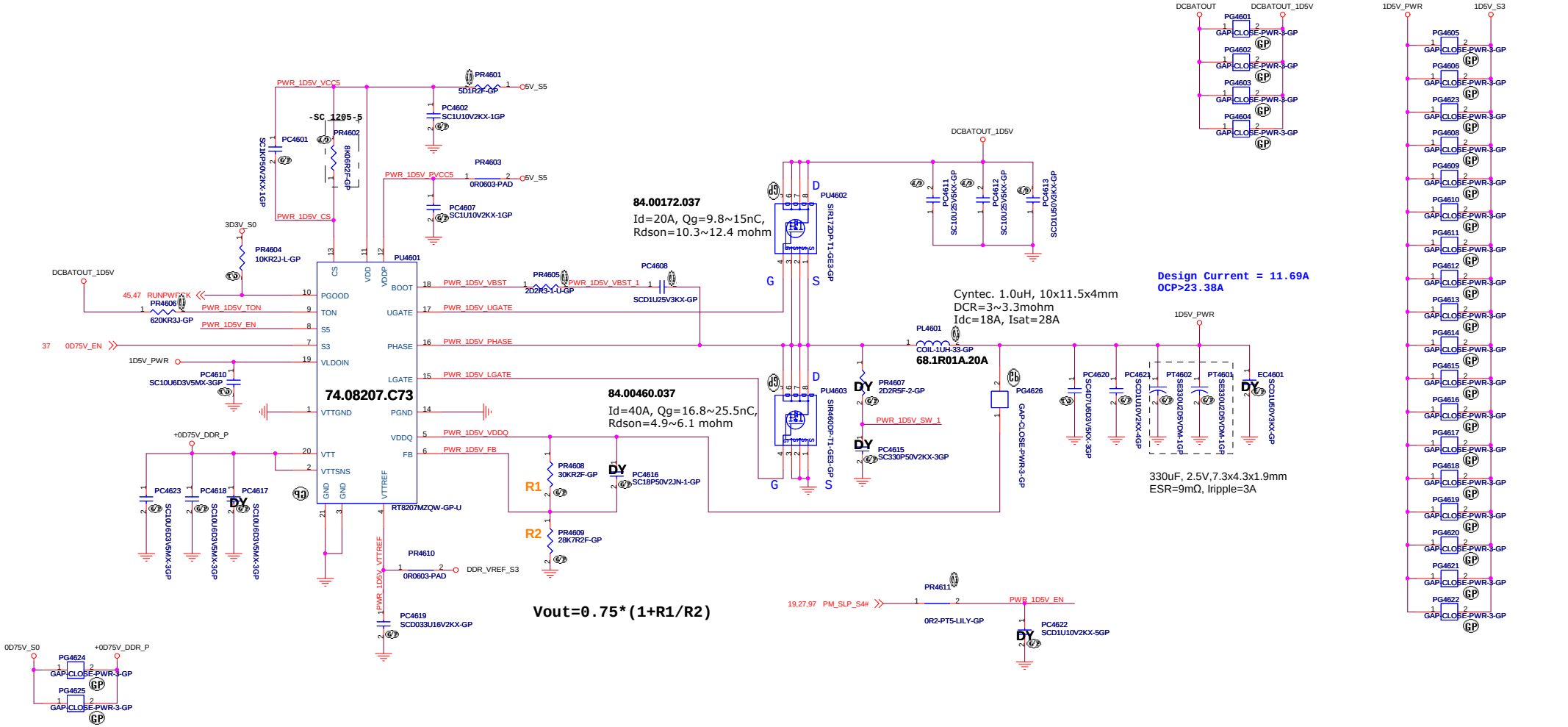
Differential Sense feedback
Resistor need close to controller

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51219_1D05V	
Size	Document Number: LSS-1	Rev: 1
Date: Wednesday, February 22, 2012	Sheet 45 of 105	

SSID = PWR.Plane.Regulator_1p5v0p75v



JV10-CS

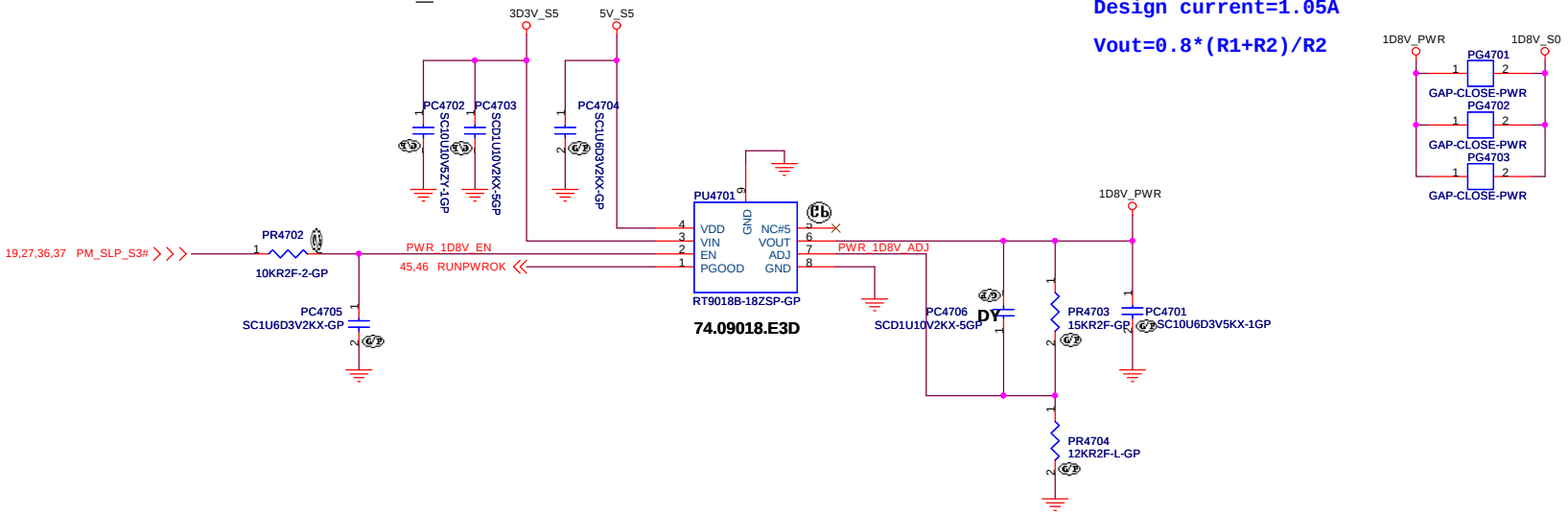
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RT8207M_1D5V_0D75V	
Size	Document Number LSS-1	Rev 1
Date: Wednesday, February 22, 2012	Sheet 46 of 105	

SSID = PWR.Plane.Regulator_1p8v

RT9018B-18ZSP for 1D8V_S0

Design current=1.05A

Vout=0.8*(R1+R2)/R2

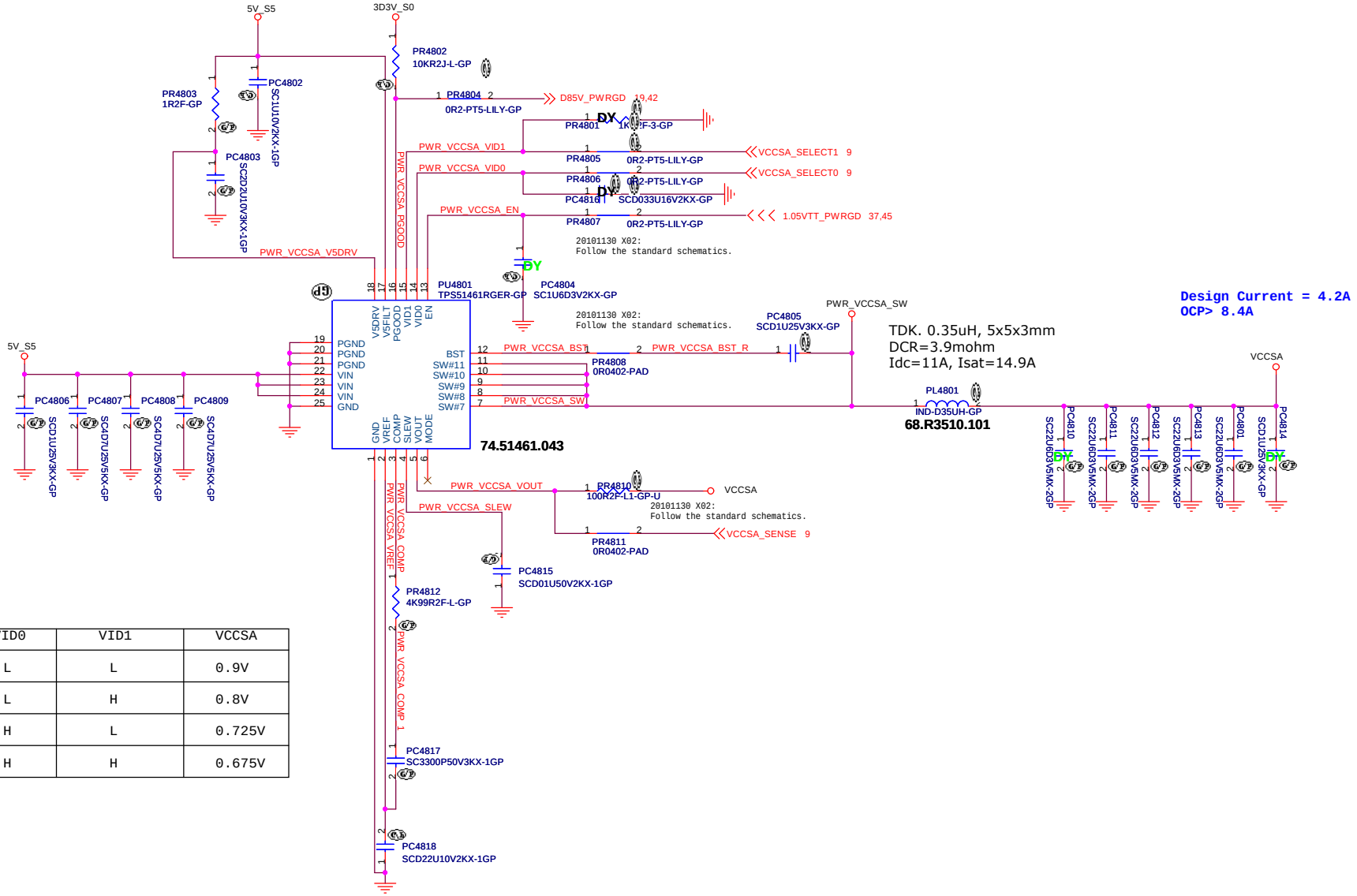


JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PWM_1D8V_RT9018B-18ZSP	
Size	Document Number: LSS-1	Rev: 1
Date: Wednesday, February 22, 2012	Sheet 47 of 105	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

JV10-CS

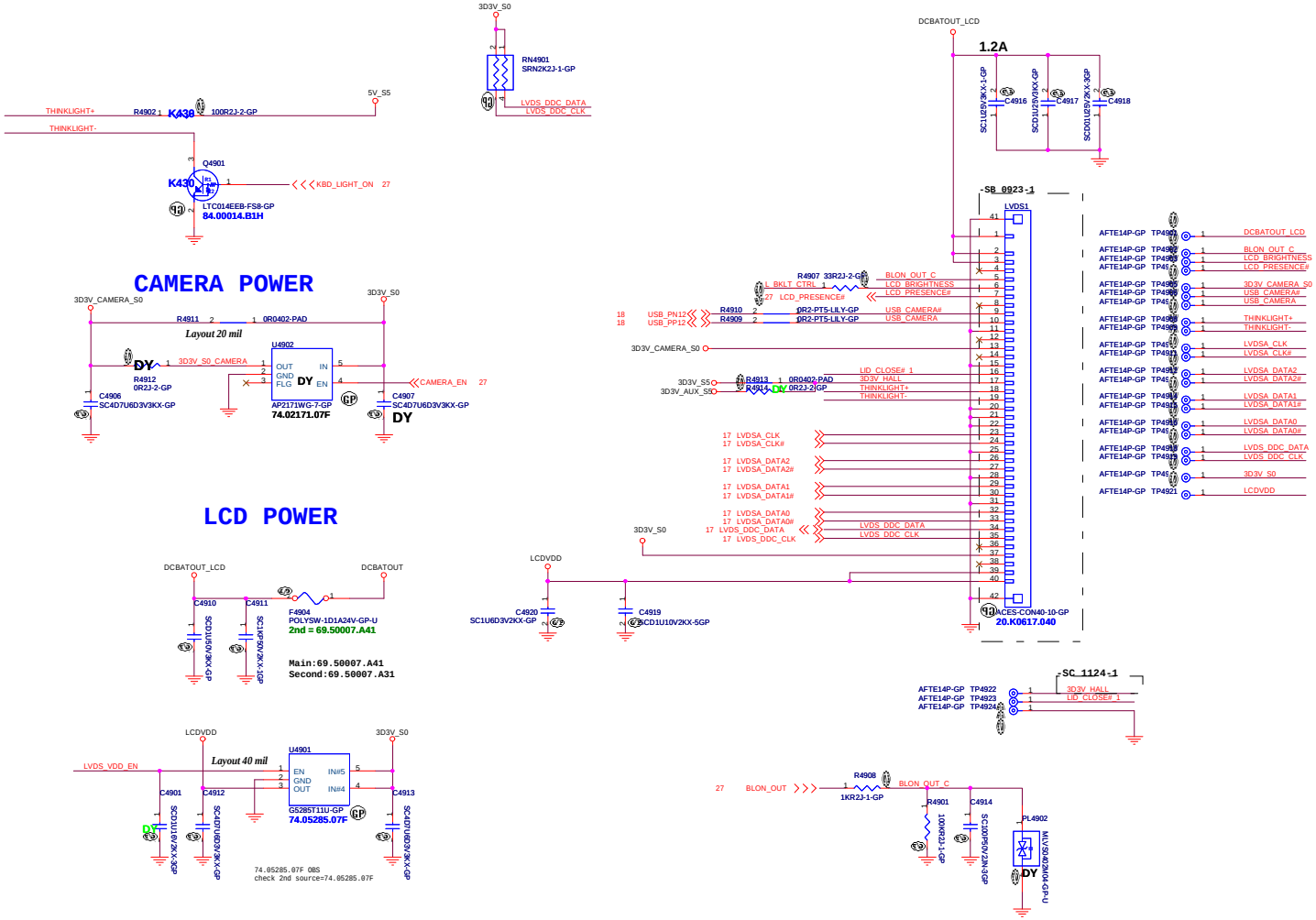
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VCCSA_TPS51461	
Size	Document Number LSS-1	Rev 1
Date: Wednesday, February 22, 2012	Sheet 48 of 105	

SSID = VIDEO

LVDS connector

LCD / Inverter Connector

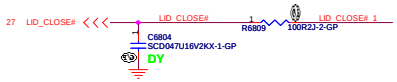


CAMERA POWER

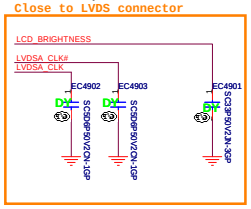
LCD POWER

Panel BL brightness/Power En/BL En

HALL SENSE



For EMI request
Close to LVDS connector



<Variant Name>

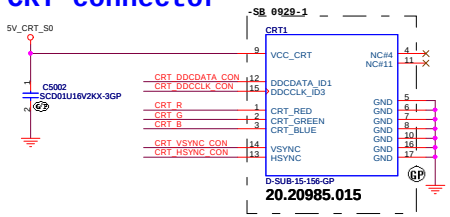
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

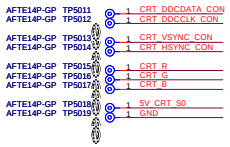
Title: LCD Connector

Size	Document Number	Rev
Custom	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 49 of 105

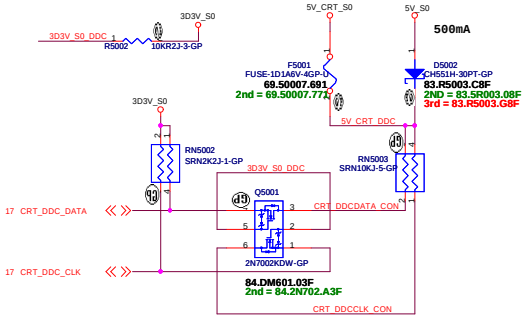
CRT connector



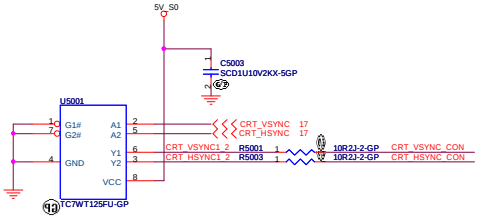


CRT DDCDATA & DDCCLK level shift

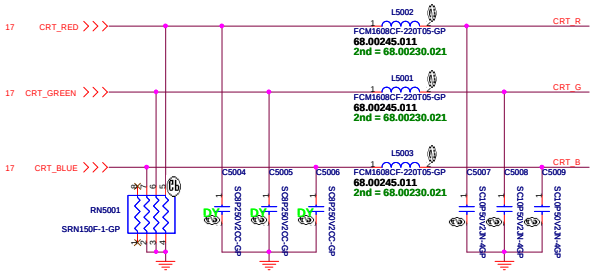
Pull High 5V Design on CRT Board

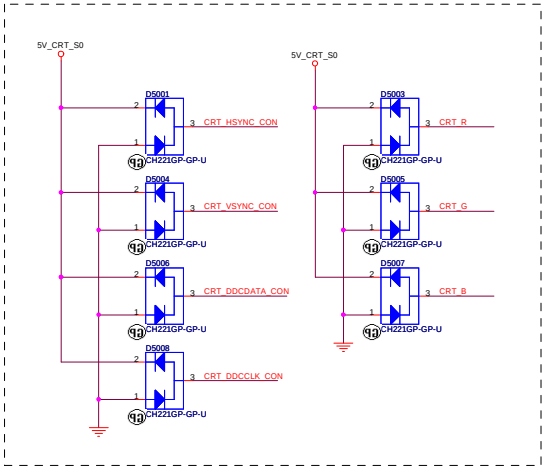


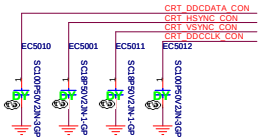
CRT Hsync & Vsync level shift



CRT RGB







<Variant Name>

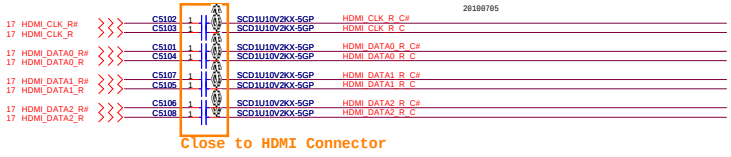
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

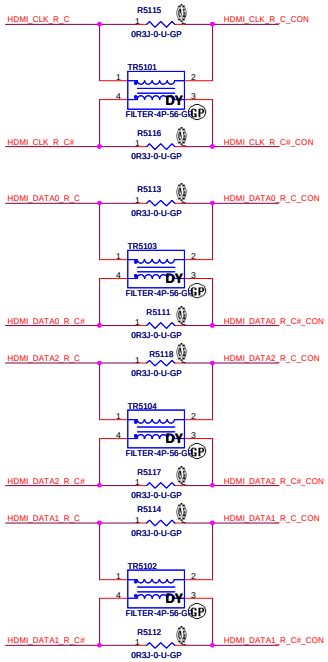
Title: CRT Connector
Size: A2
Document Number: LSS-1
Rev: 1
Date: Wednesday, February 22, 2012
Sheet 50 of 105

SSID = VIDEO

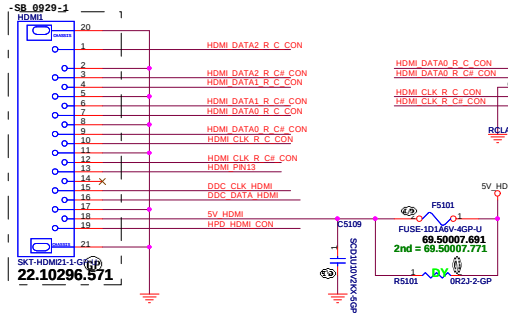
HDMI Passive Level Shifter

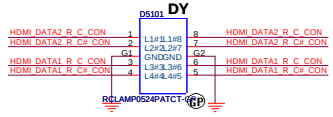
Close to HDMI Connector

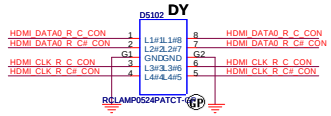


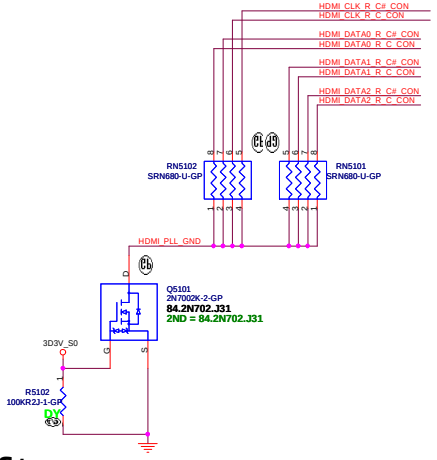


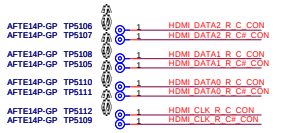
HDMI CONNECTOR

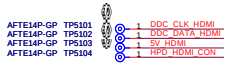


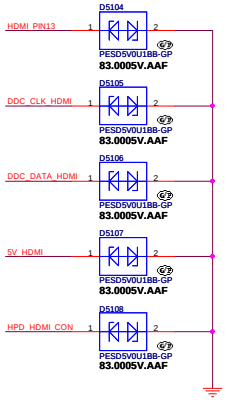




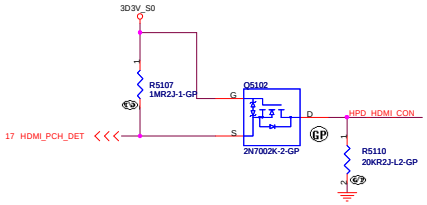


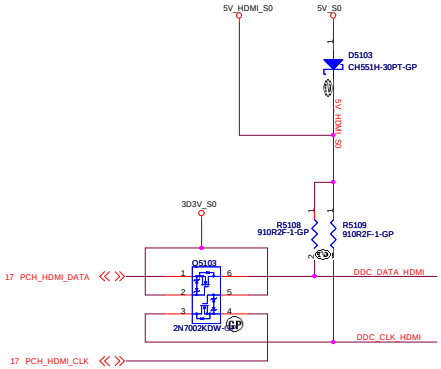






HDMI DDC Passive Level Shifter





<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A2 | Document Number: LSS-1 | Rev: 1

Date: Wednesday, February 22, 2012 | Sheet 51 of 105

BLANK

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***eDP***		
Size: A4	Document Number: **LSS-1**	Rev: **1**
Date: Friday, February 10, 2012	Sheet 52 of 105	

BLANK

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	LSS-1	1

Date: Friday, February 10, 2012 Sheet 53 of 105

BLANK

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

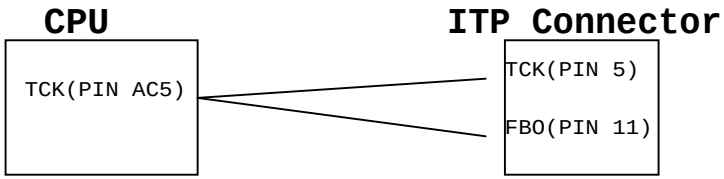
Size	Document Number	Rev
A4	LSS-1	1

Date: Friday, February 10, 2012 Sheet 54 of 105

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max), others place near CPU side.

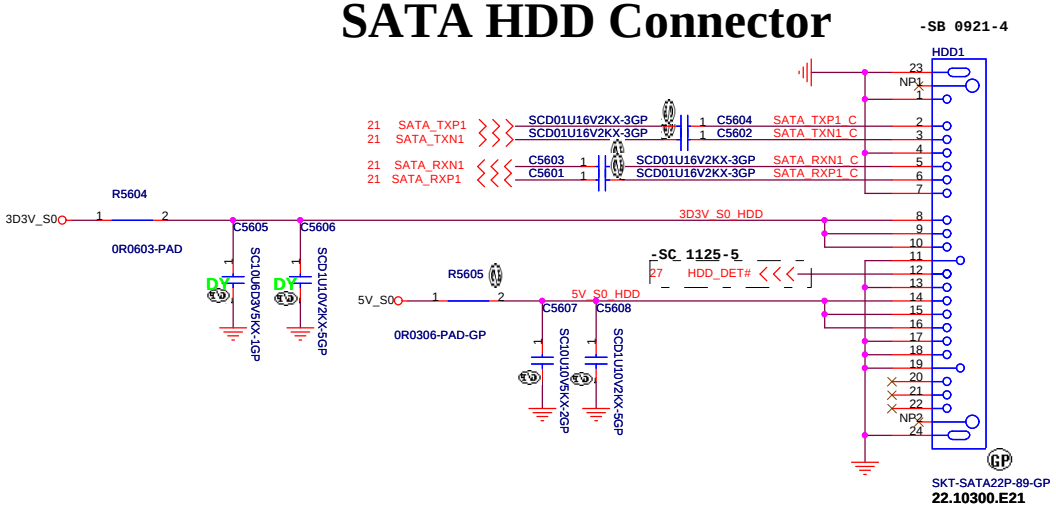


<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ITP*		
Size: A4	Document Number: **LSS-1**	Rev: **1**
Date: Friday, February 10, 2012	Sheet 55 of 105	

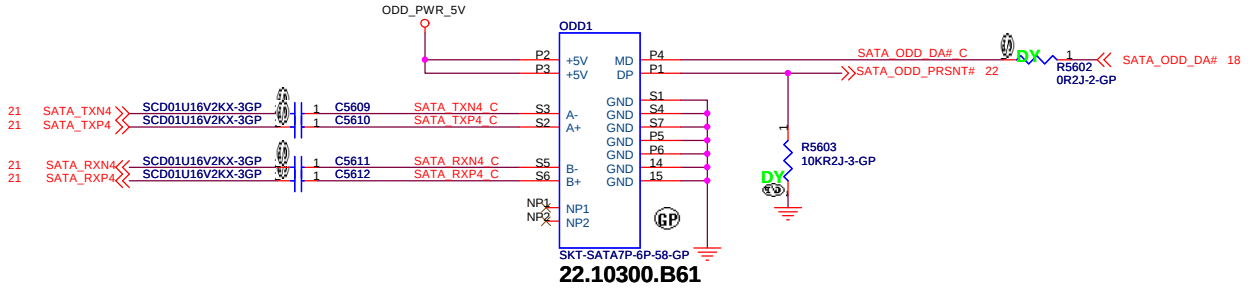
SATA HDD Connector



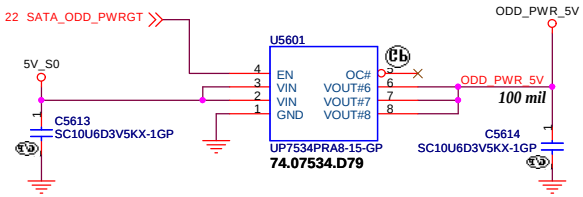
ODD Connector

SATA_RX- and SATA_RX+ Trace Length match within 20 mil

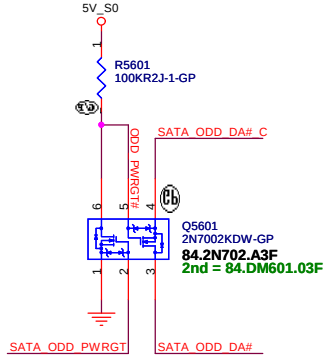
Mars:
Exchange ODD and ESATA differential pair each other.

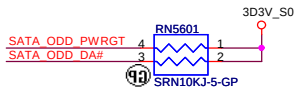


SATA Zero Power ODD



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON





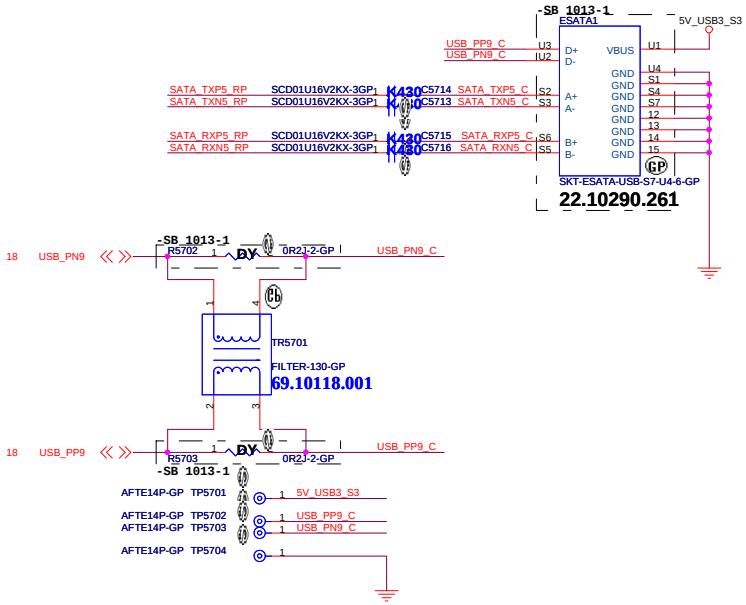
SUPPORT ZERO SATA ODD

Current limit
Active High
typ =>2A

<Variant Name>

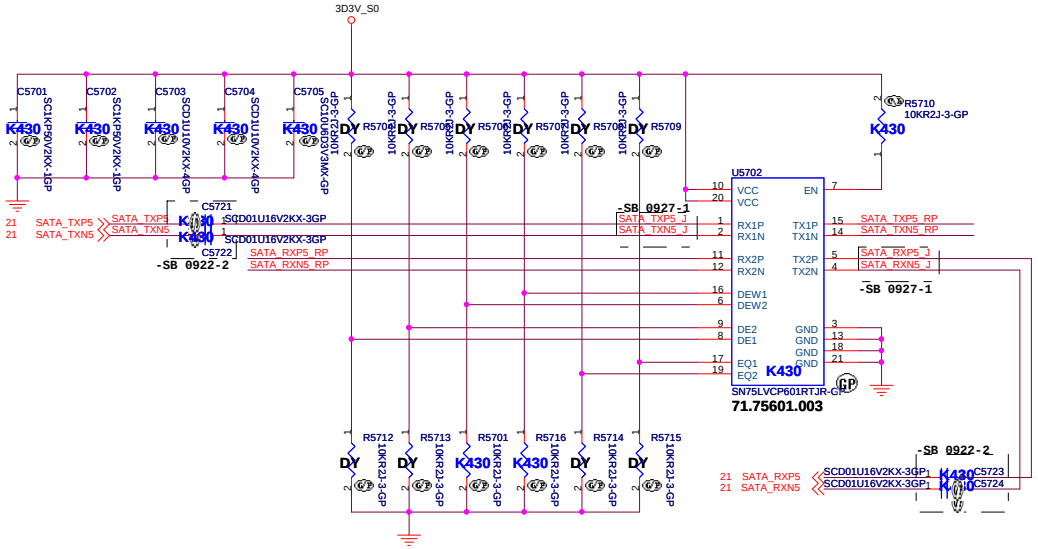
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD/ODD		
Size: A3	Document Number: LSS-1	Rev: 1
Date: Wednesday, February 22, 2012	Sheet 56 of 105	



ESATA	
NAME	TYPE
S1	GND
S2	A+
S3	A-
S4	GND
S5	B-
S6	B+
S7	GND

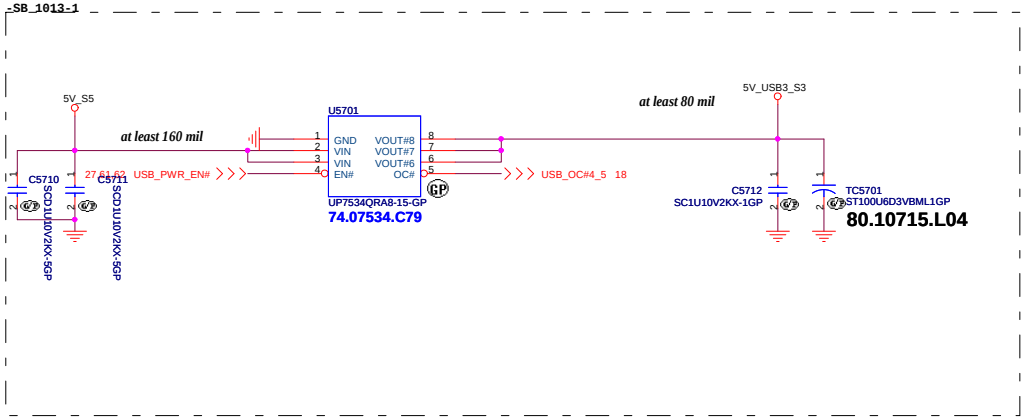
USB	
NAME	TYPE
U1	VBUS
U2	D-
U3	D+
U4	GND



ESATA Repeater

ESD Protection

POWER



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA or USB20

Size	Document Number	Rev
Custom	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 57 of 105

Int. Mono Analog MIC for B series

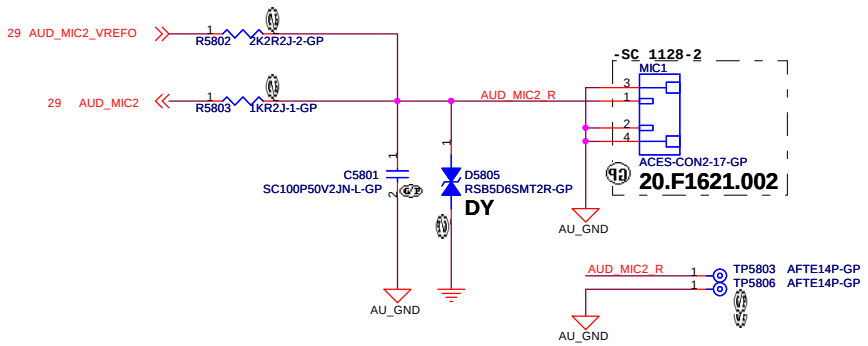
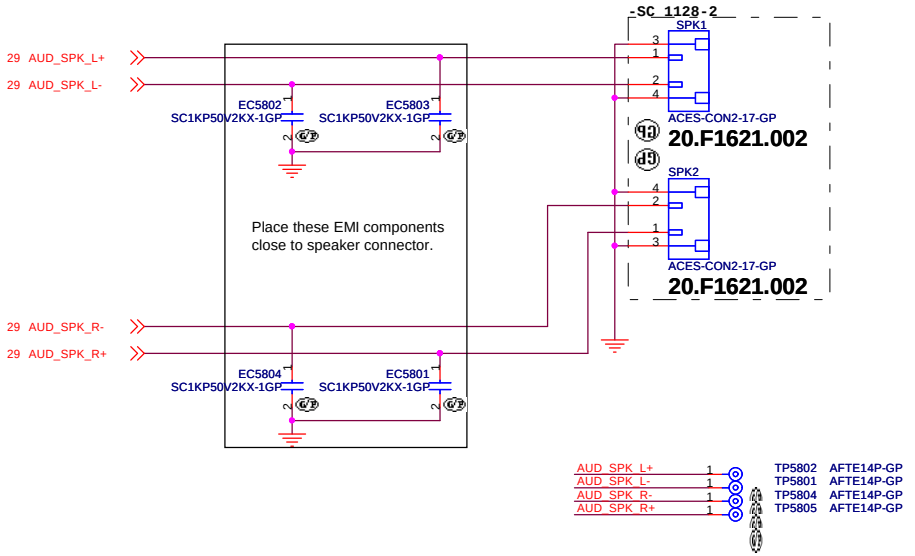
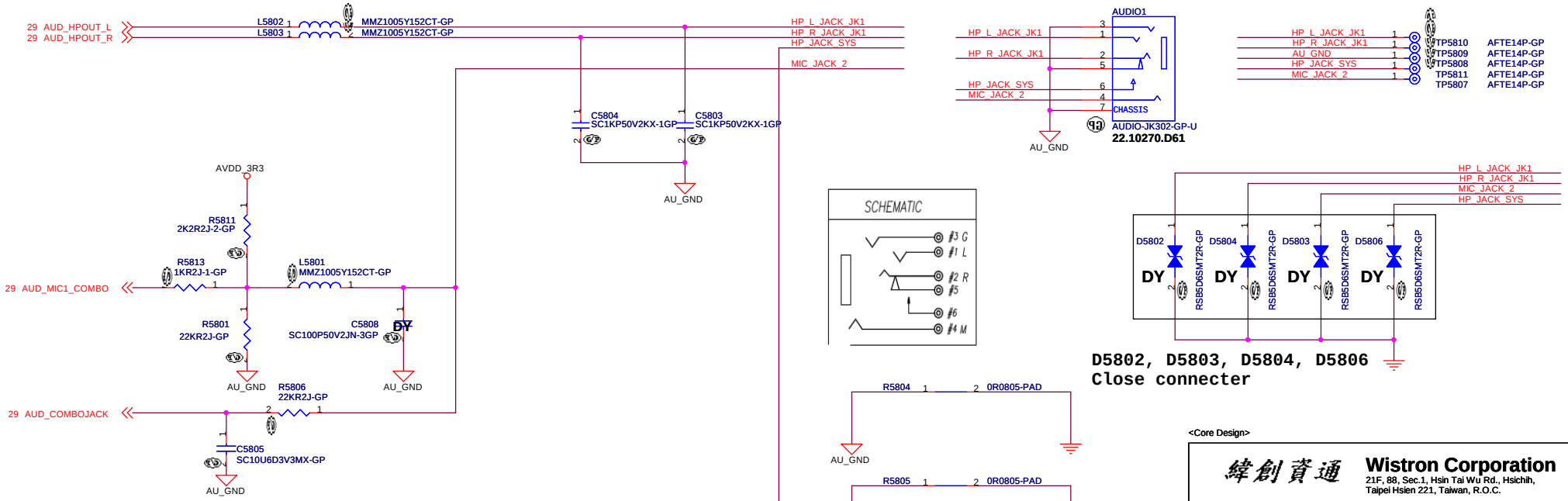


Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.BAF
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0AF
NXP	PESD5V0S1BB	N/A	83.0005V.0AF

INTERNAL STEREO SPEAKERS





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

Size: A3 | Document Number: LSS-1 | Rev: 1

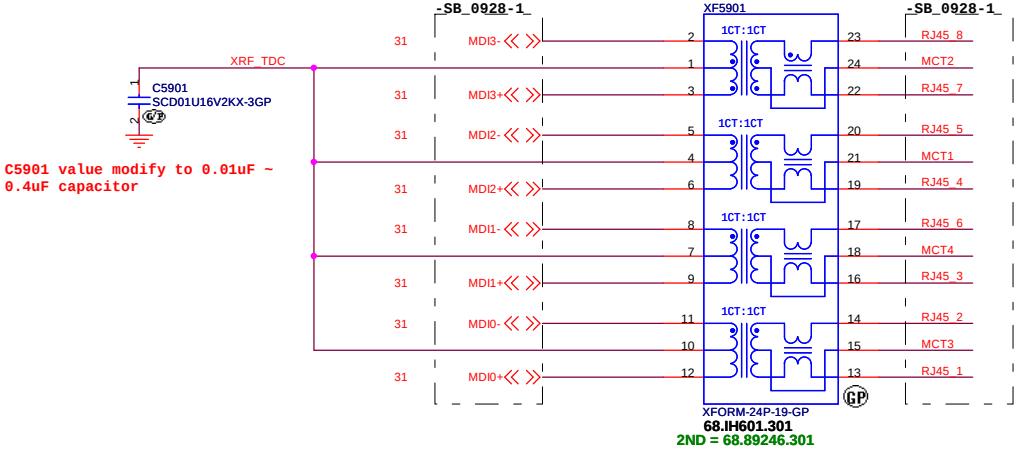
Date: Wednesday, February 22, 2012 | Sheet 58 of 105

FOR CO-LAY

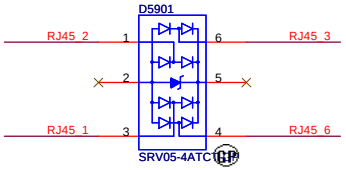
GIGA Lan Transformer

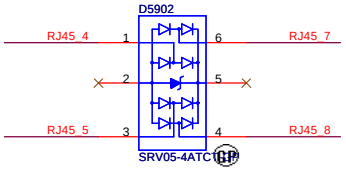
TVS
83.00005.BAE
DIODE ARR SRV05-4.TCT SOT-23-6

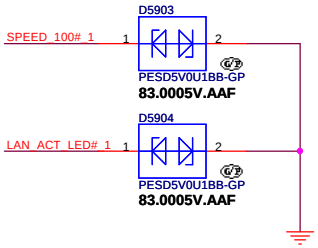
83.09904.AAE
DIODE ESD AZC099-04S SOT23-6L

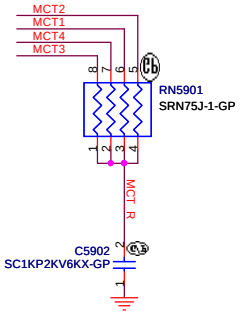


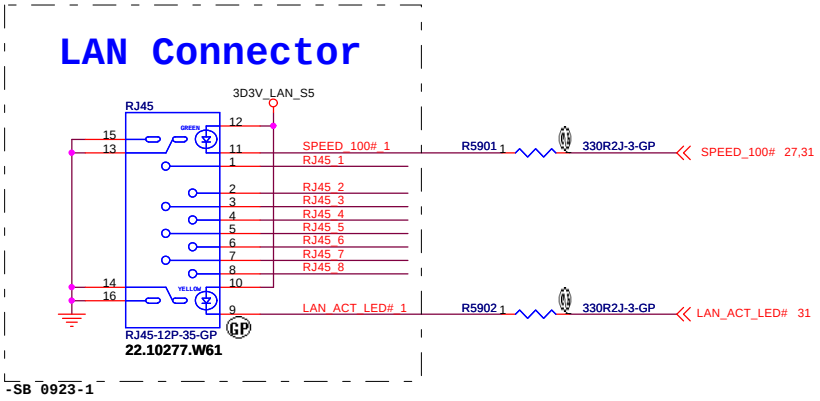
1st
68.IH601.301(Taimag) for 1000
68.HH035.301(Taimag) for 10/100
2nd
68.2413S.30A(Lankom) for 1000
68.H6441.301(Lankom) for 10/100

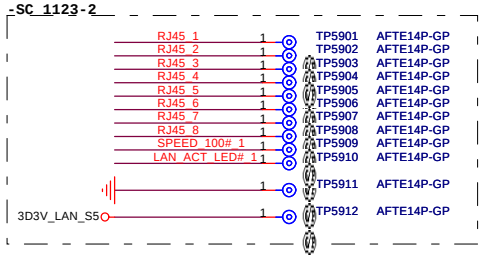


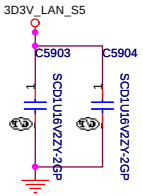










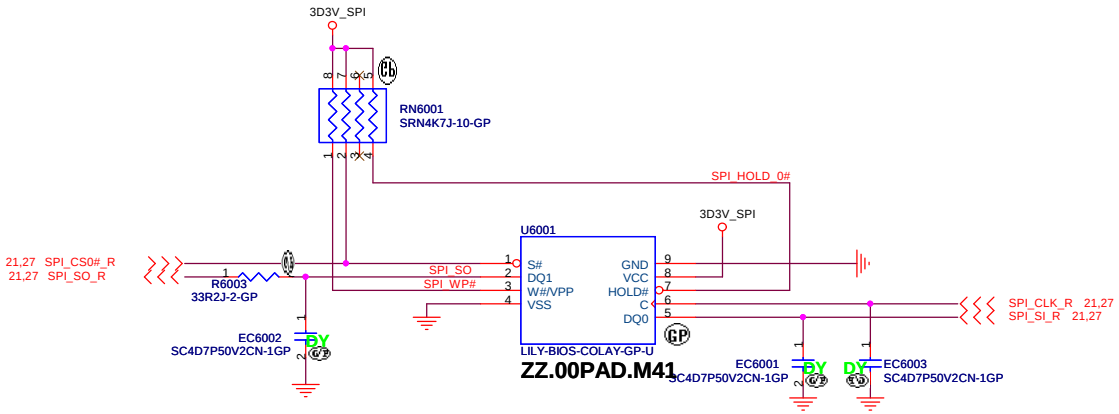


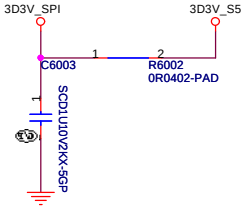
<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *RJ45 / Transformer*		
Size: A3	Document Number: LSS-1	Rev: 1
Date: Wednesday, February 22, 2012	Sheet 59 of 105	

SSID = Flash.ROM

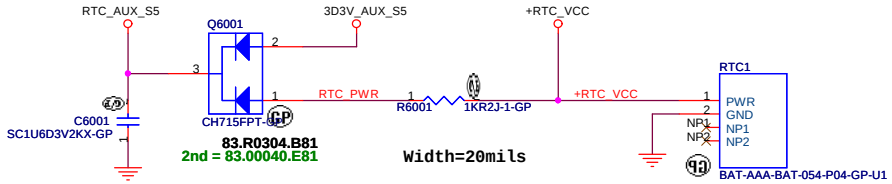
SPI FLASH ROM (8M byte) for PCH

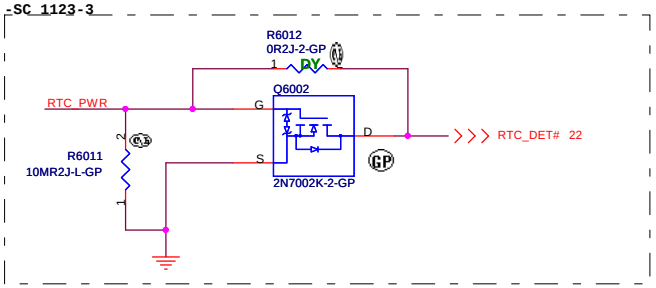


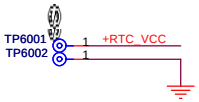


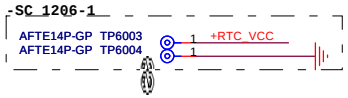
SPI FLASH ROM (8M byte) for PCH

SSID = RBATT





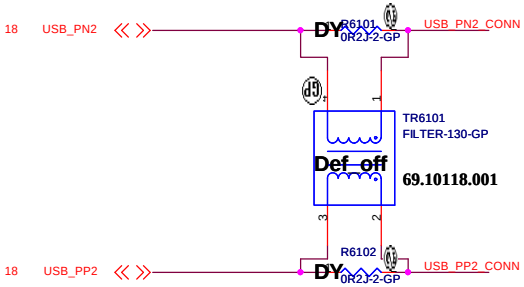


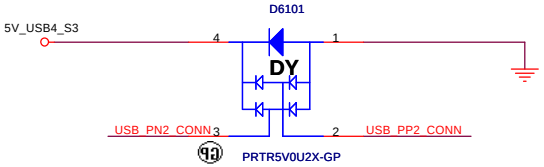


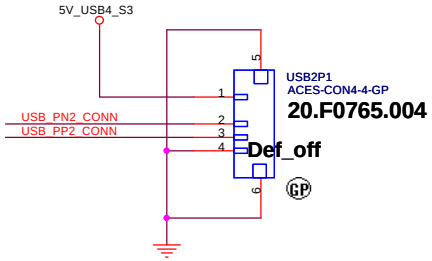
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

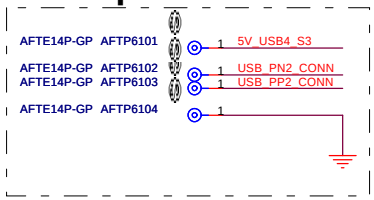
Title: *Flash/RTC*		
Size: A3	Document Number: LSS-1	Rev: 1
Date: Wednesday, February 22, 2012	Sheet 60 of 105	





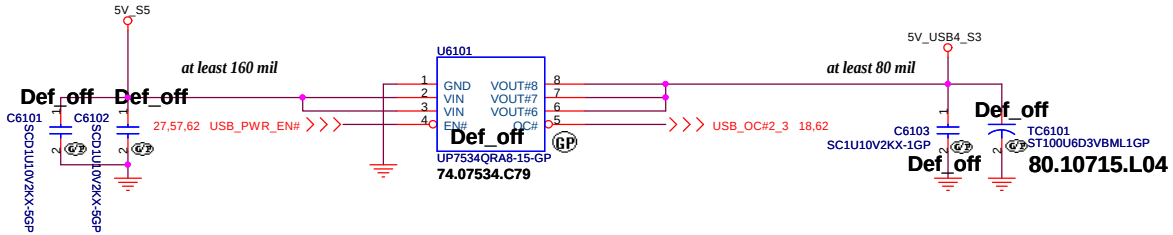


test point at bottom side



Only USB2.0

POWER



<Core Design>

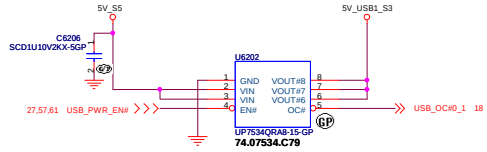
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Connector***

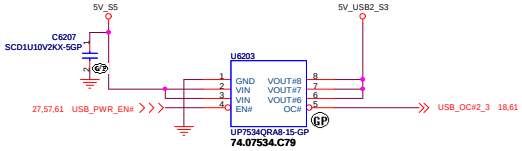
Size	Document Number	Rev
A3	LSS-1	1

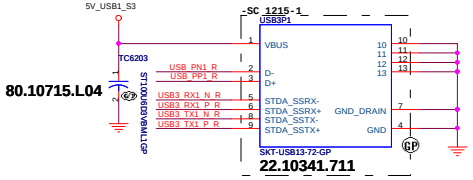
Date: Wednesday, February 22, 2012 Sheet 61 of 105

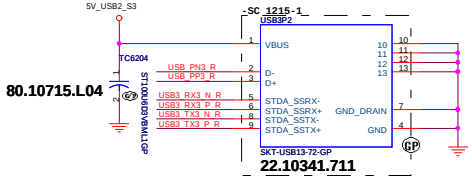
USB3.0 Port1

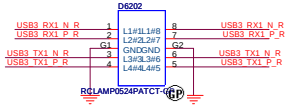


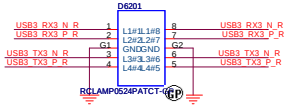
USB3.0 Port2

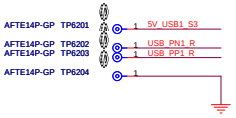


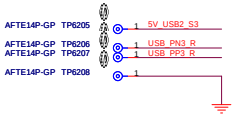


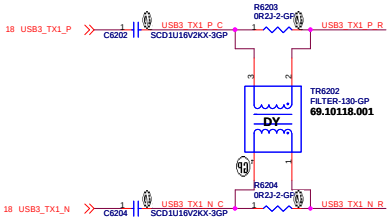


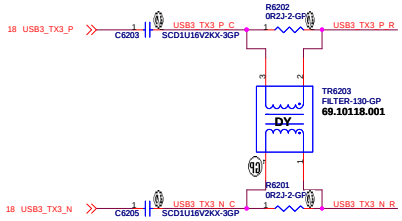


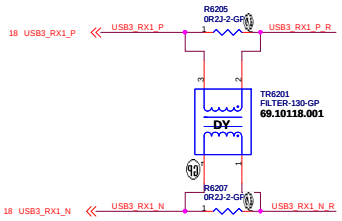


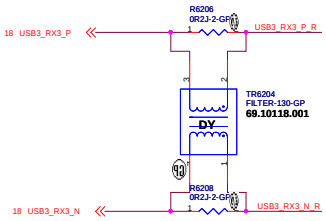


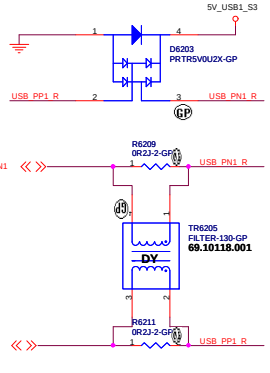


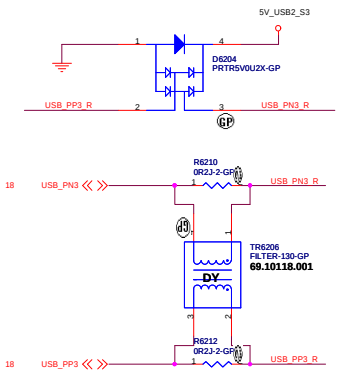












<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0 Port*2

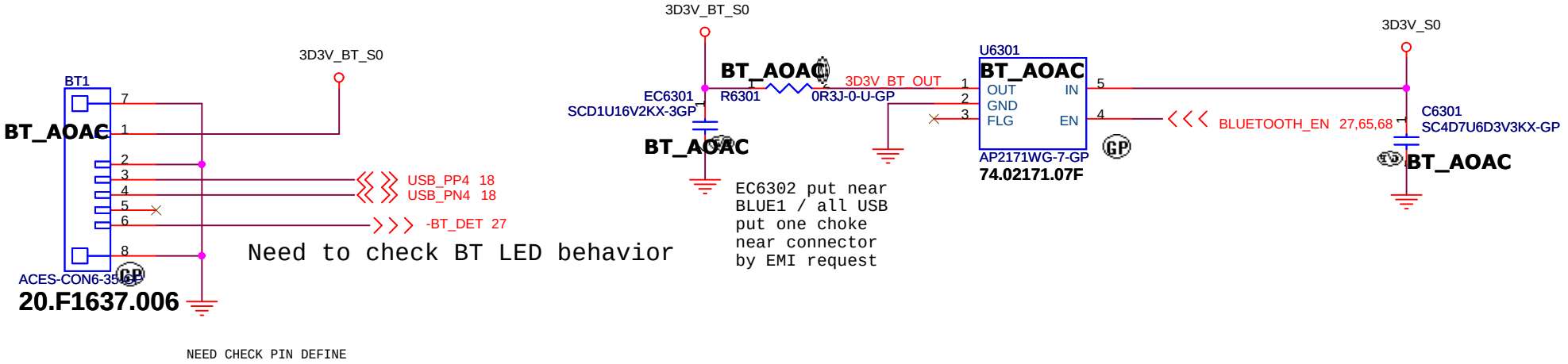
Size: A2 | Document Number: LSS-1 | Rev: 1

Date: Wednesday, February 22, 2012 | Sheet 62 of 105

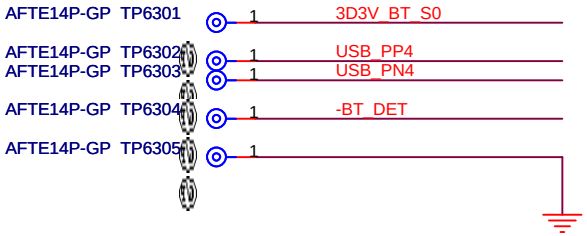
SSID = User.Interface

-SB 1013-2

Bluetooth conn.



	BT CONN.	WLAN CONN.
BT1	**ASM**	**DY**
R6301	**ASM**	**DY**
U6301	**ASM**	**DY**
C6301	**ASM**	**DY**
RN1803	**DY**	**ASM**
RN1804	**ASM**	**DY**



<Variant Name>

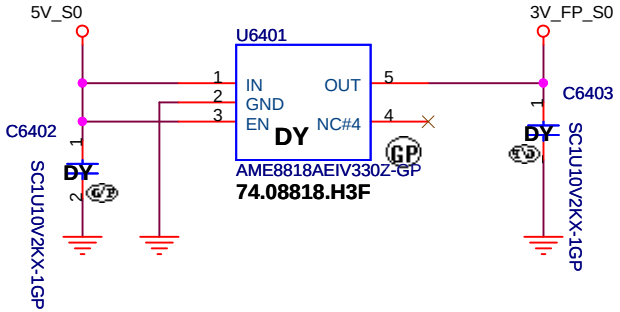
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

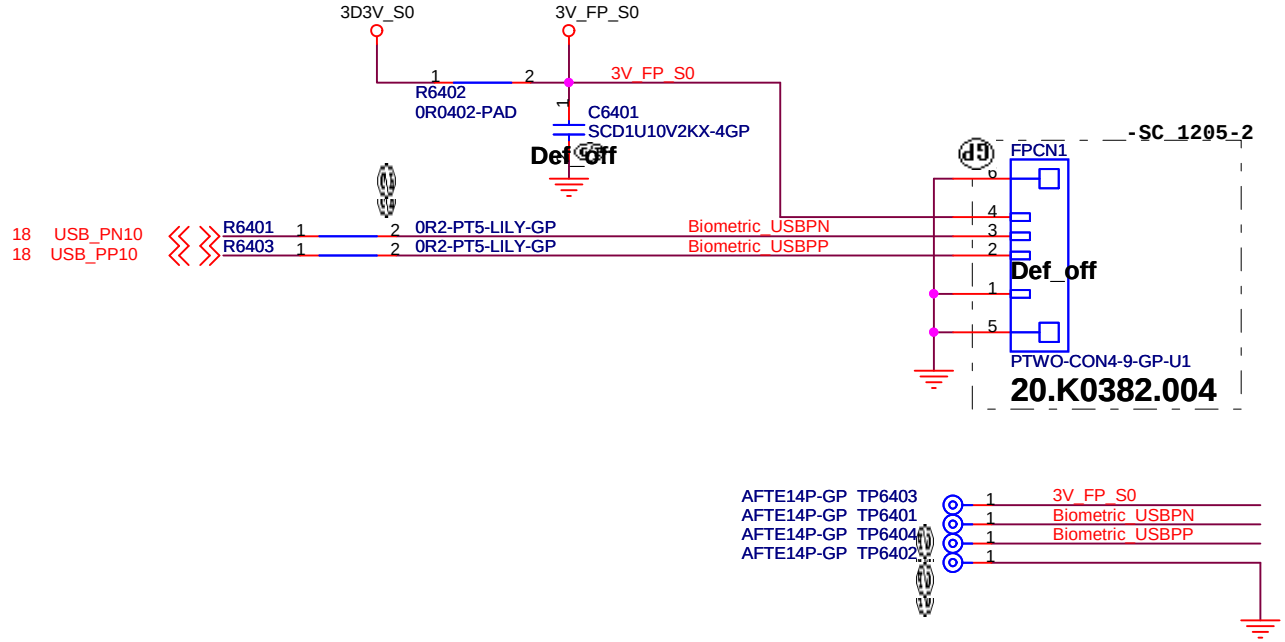
Size	Document Number	Rev
A4	**LSS-1**	**1**

Date: Wednesday, February 22, 2012 Sheet 63 of 105

3.3V FP LDO



Finger Printer Connector



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

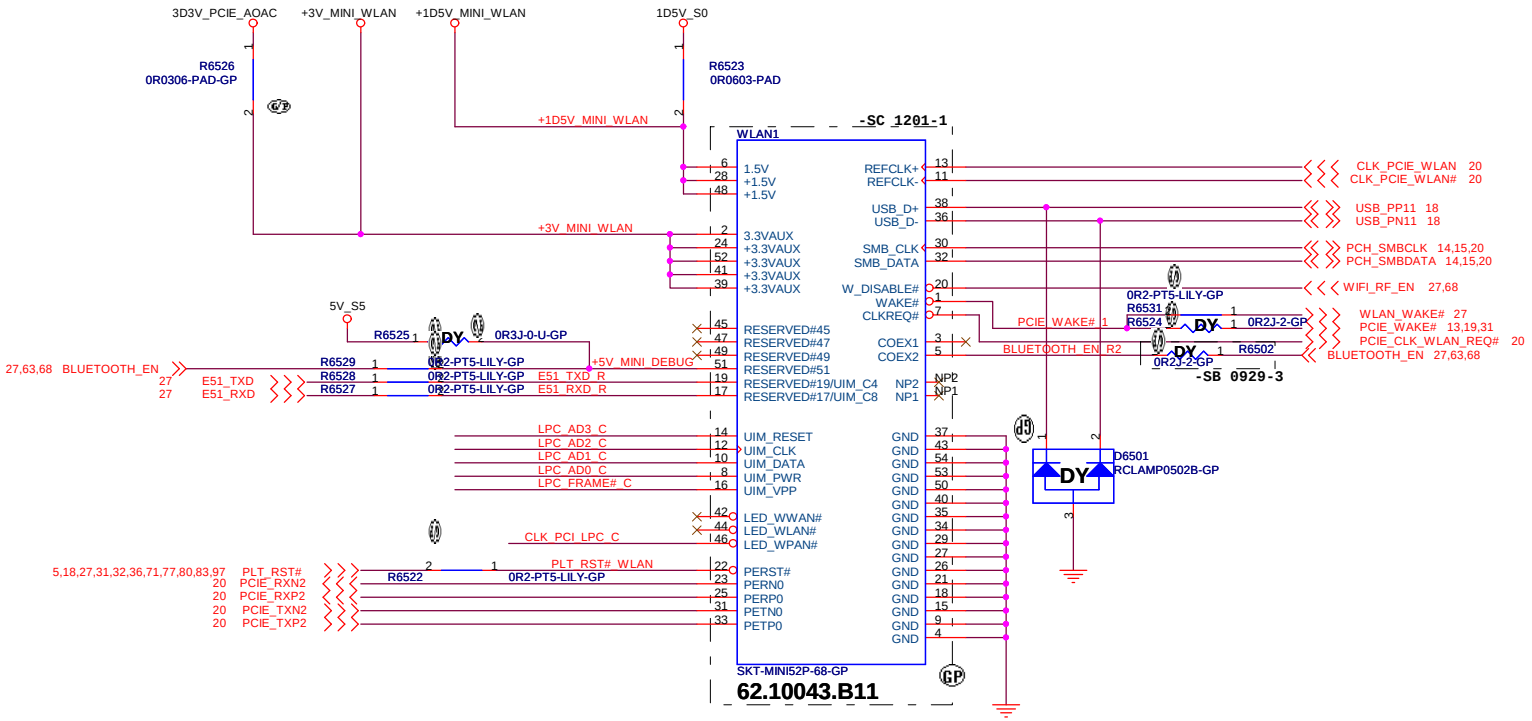
Title: ***Finger Printer Connector***

Size	Document Number	Rev
A4	LSS-1	1

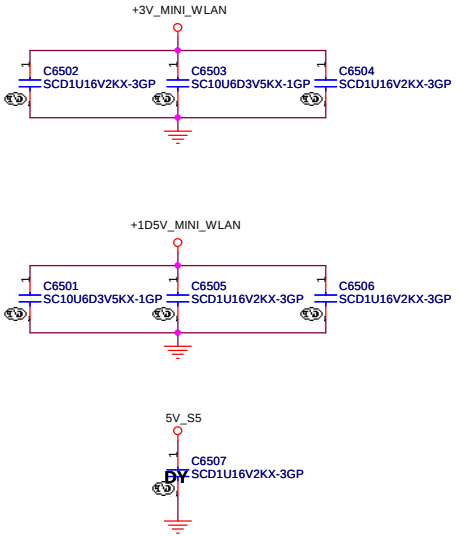
Date: Wednesday, February 22, 2012 Sheet 64 of 105

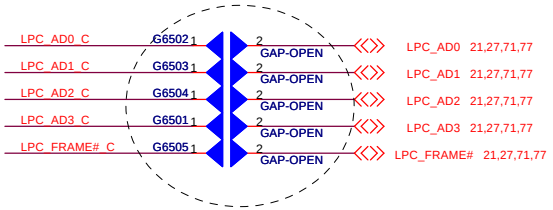
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

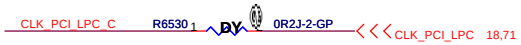


Place near MINI Card CONN





G6506~G6511
placememt close WLAN1
in bottom side



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

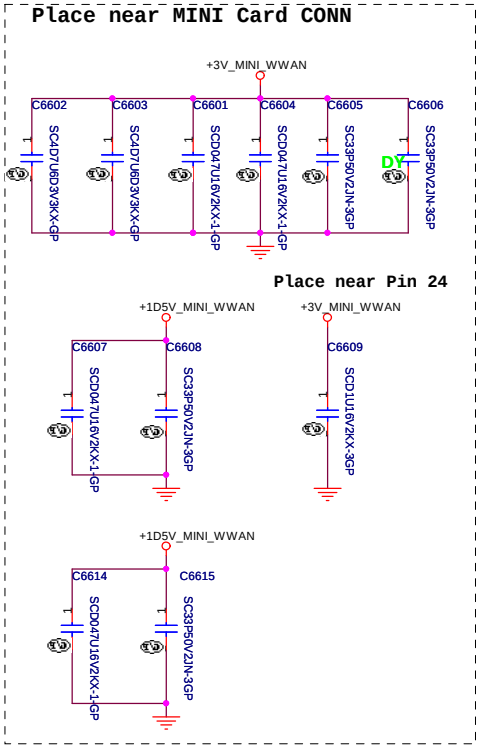
Title: ***MINICARD(WLAN)/ITP CONN***

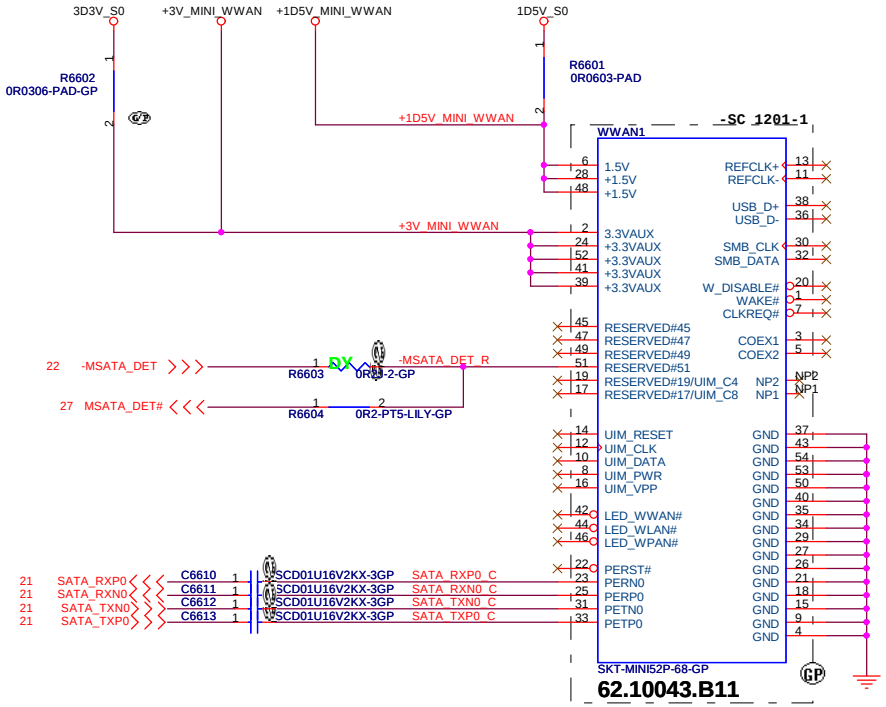
Size	Document Number	Rev
A3	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 65 of 105

SSID = Wireless

Mini Card Connector(WWAN)





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size	Document Number	Rev
A3	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 66 of 105

BLANK

<Variant Name>

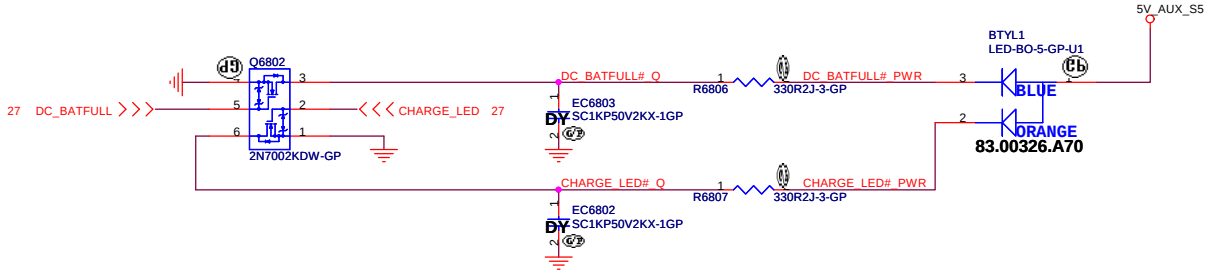
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

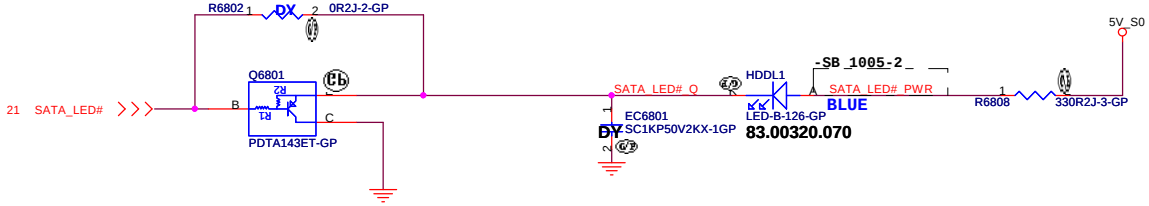
Title: ***Reserved***

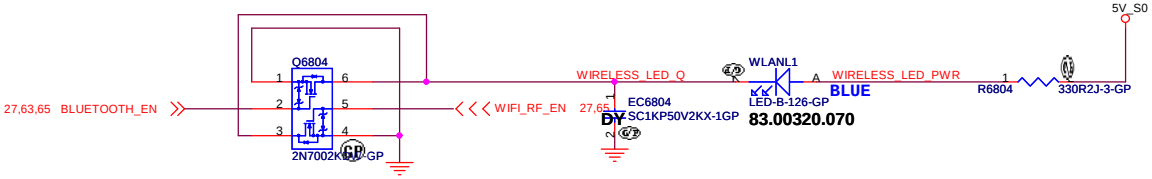
Size	Document Number	Rev
A4	LSS-1	1

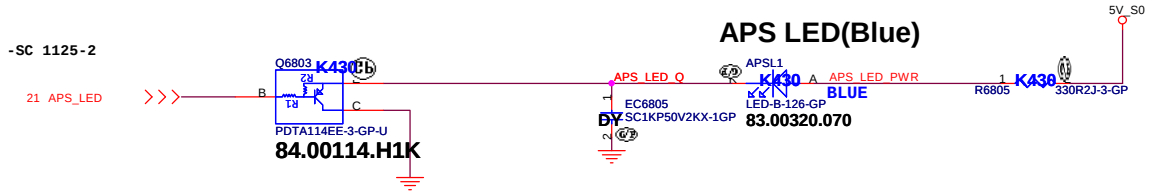
Date: Friday, February 10, 2012 Sheet 67 of 105

SSID = User.Interface









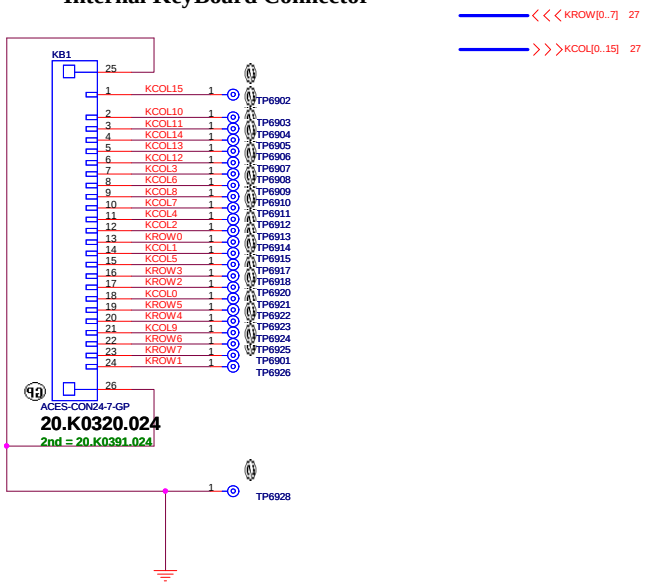
APS
LK430 : YES
LE430 : N/A
LK230 : YES

bom LA47

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LED Bard/Power Button***	
Size: Custom	Document Number: **LSS-1**	Rev: **1**
Date: Wednesday, February 22, 2012	Sheet 68 of 105	

SSID = KBC

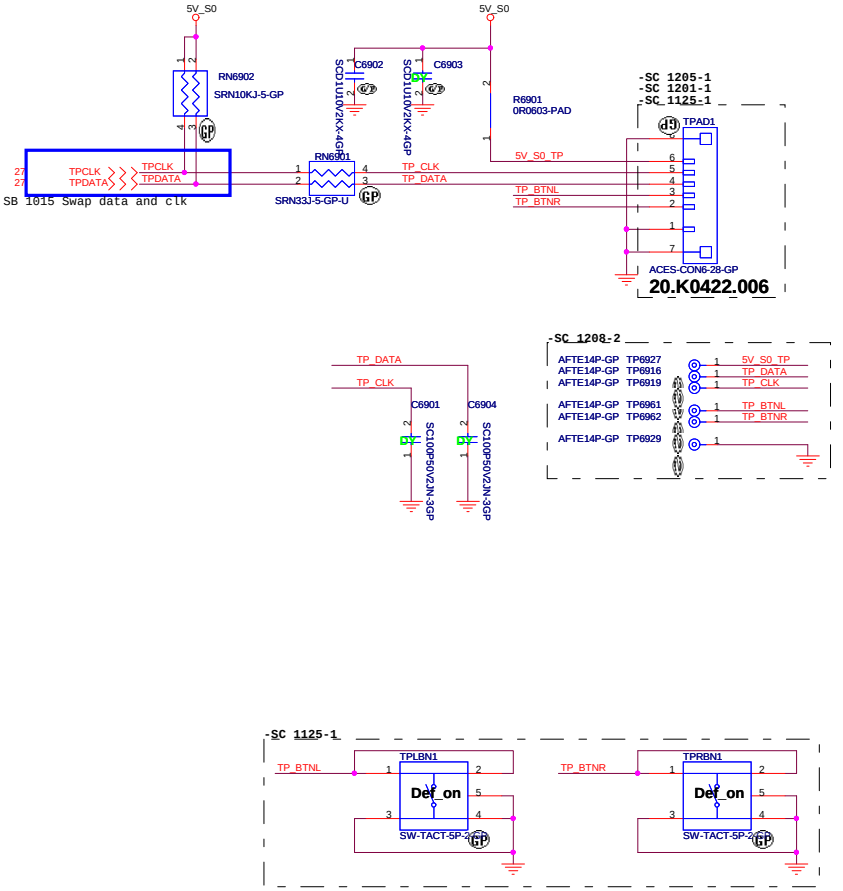
Internal KeyBoard Connector



* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	S1	S2	S3	S4	S5	S6	S7	S8

SSID = Touch.Pad



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**TOUCH PAD CONNECTOR**
Size: Custom	Document Number: LSS-1
Rev	1
Date: Wednesday, February 22, 2012	Sheet 69 of 105

<Variant Name>

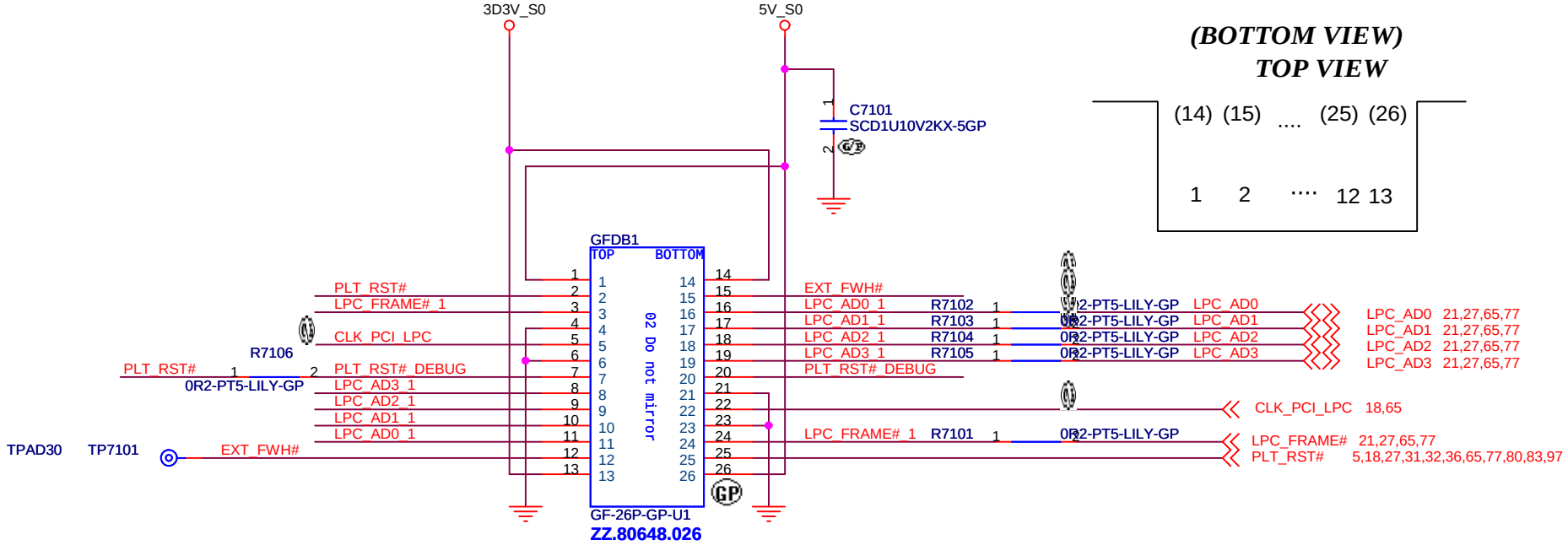
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size	Document Number	Rev
A4	**LSS-1**	**1**

Date: Friday, February 10, 2012 Sheet 70 of 105



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

Size	Document Number	Rev
A4	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 71 of 105

BLANK

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	LSS-1	1

Date: Friday, February 10, 2012 Sheet 72 of 105

BLANK

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	LSS-1	1

Date: Friday, February 10, 2012 Sheet 73 of 105

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CARD Reader CONN***

Size	Document Number	Rev
A2	LSS-1	1

Date: Friday, February 10, 2012 Sheet 74 of 105

BLANK

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***New Card***		
Size: A4	Document Number: **LSS-1**	Rev: **1**
Date: Friday, February 10, 2012	Sheet 75 of 105	

BLANK

<Variant Name>

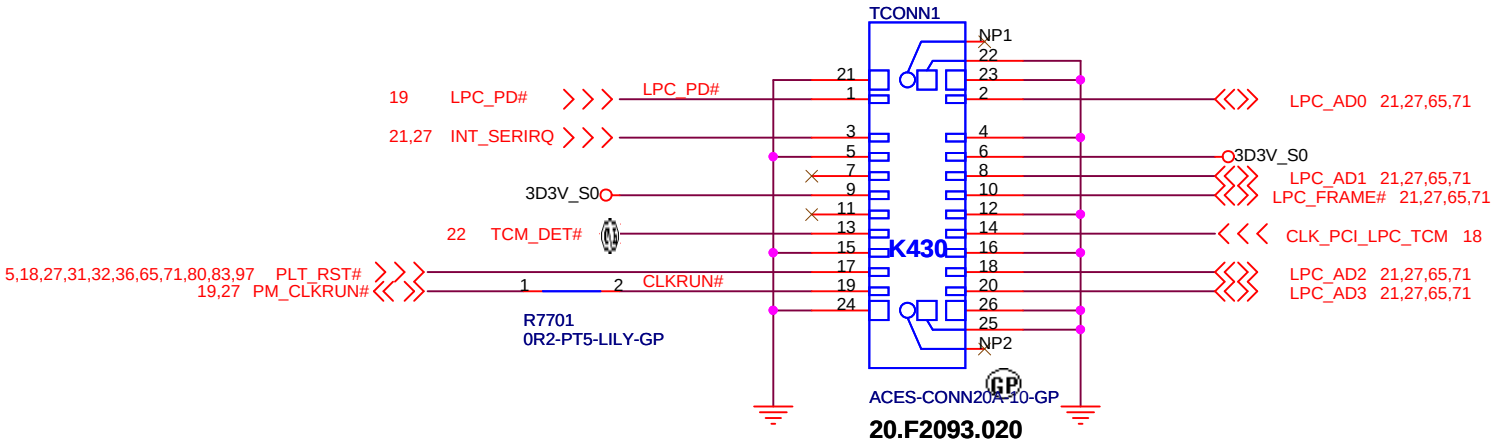
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LSS-1	1

Date: Friday, February 10, 2012 Sheet 76 of 105

TCM
LK430 : YES
LE430 : N/A
LK230 : YES



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 77 of 105

BLANK

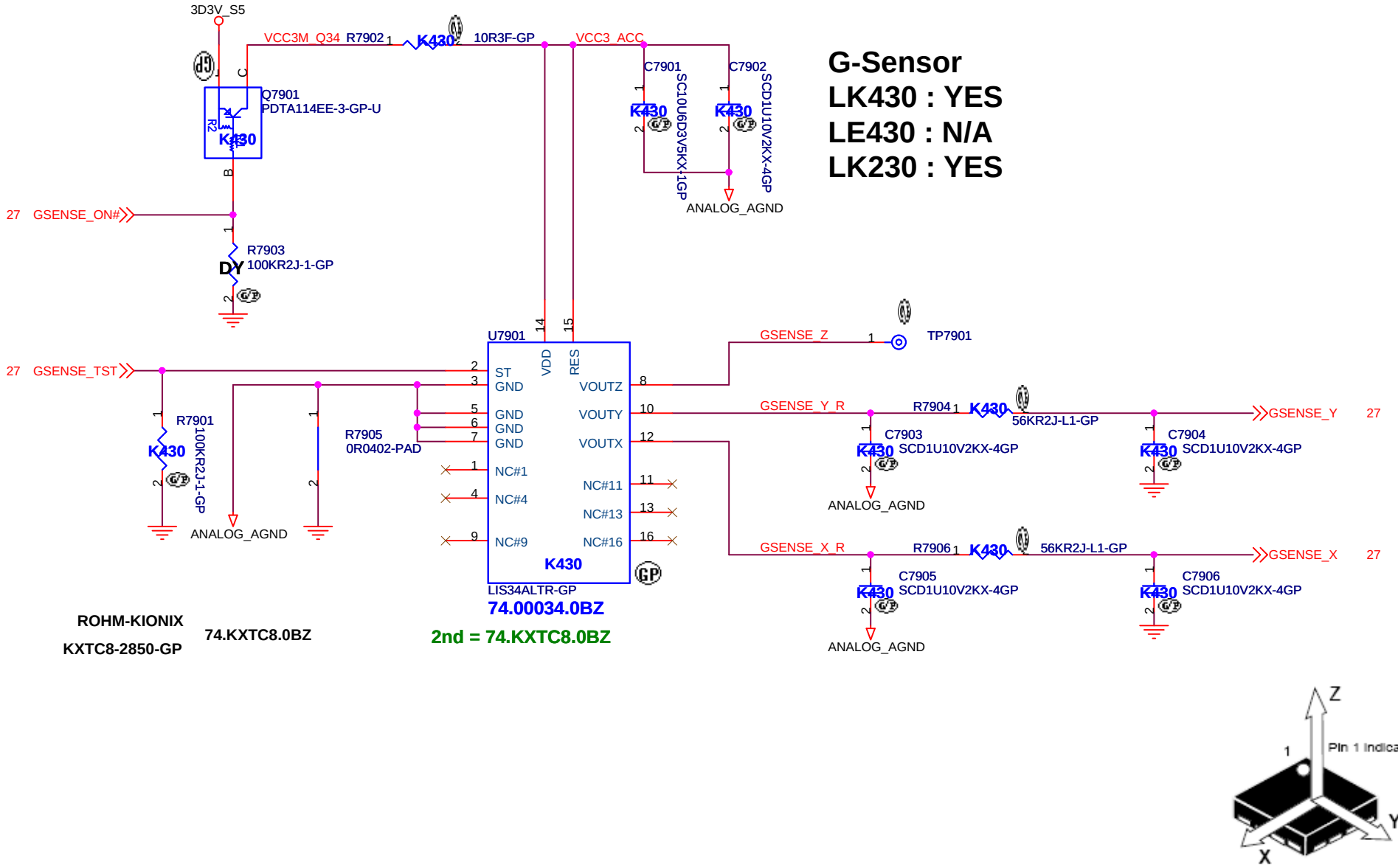
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LSS-1	1

Date: Friday, February 10, 2012 Sheet 78 of 105



G-Sensor
LK430 : YES
LE430 : N/A
LK230 : YES

<Variant Name>

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **G-Sensor**

Size	Document Number	Rev
A4	**LSS-1**	**1**

Date: Wednesday, February 22, 2012 Sheet 79 of 105

RFID

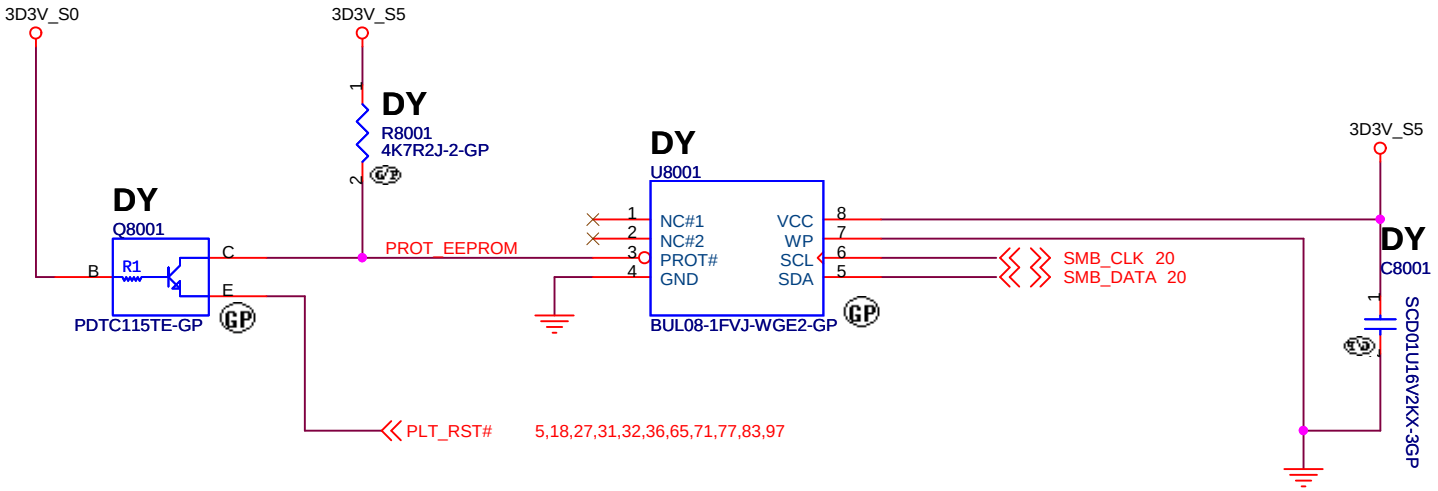


Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015TEB	N/A	84.00015.B1H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

Size	Document Number	Rev
A4	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 80 of 105

BLANK

<Variant Name>

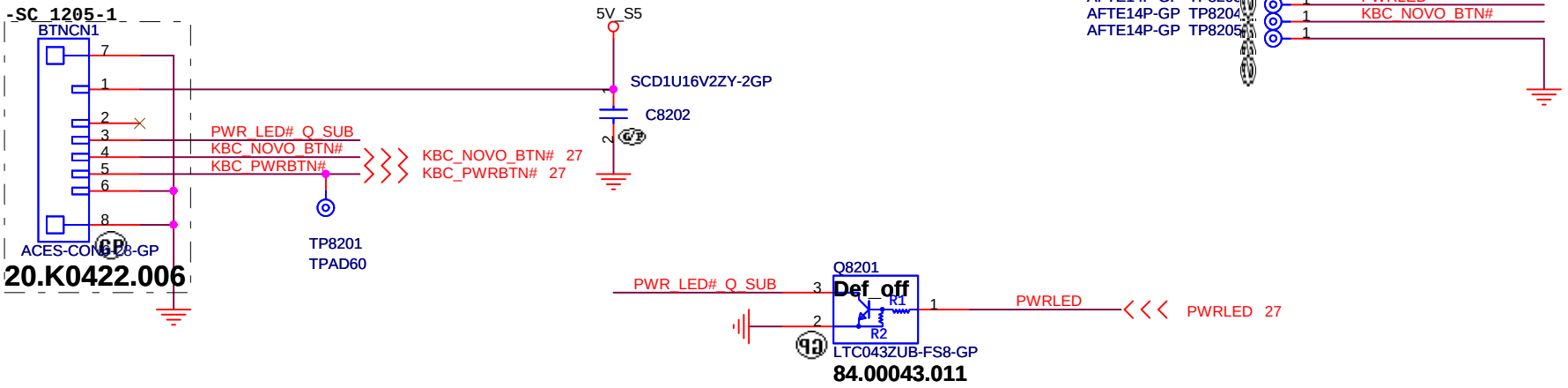
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

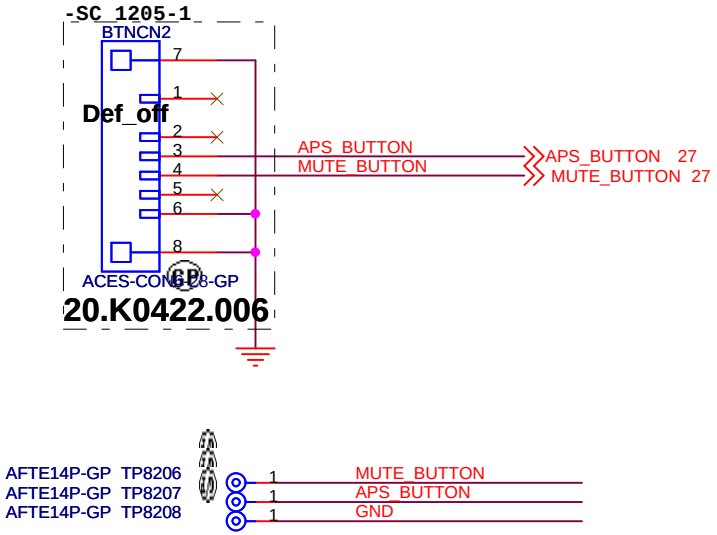
Size	Document Number	Rev
A4	LSS-1	1

Date: Friday, February 10, 2012 Sheet 81 of 105

POWER BUTTON BOARD



BUTTON BOARD



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

Size	Document Number	Rev
A4	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 82 of 105

4 PEG_TXP[15..0]
4 PEG_TXN[15..0]
4 PEG_RXP[15..0]
4 PEG_RXN[15..0]

VGA1A
1 OF 17
N13P-NS-A1
N13P-NS-A1-GP

PEX_WAKE# AJ11
PEX_RST# AJ12
NV_PEG_CLKREQ# AK12 PEX_CLKREQ#
20 CLK_PCIE_VGA AL13 PEX_REFCLK
20 CLK_PCIE_VGA# AK13 PEX_REFCLK#

PEG_RXP0 C8309 SCD22U10V2KX-1GP PEG_C_RXP0 AK14 PEX_TX0
PEG_RXN0 C8310 SCD22U10V2KX-1GP PEG_C_RXN0 AJ14 PEX_TX0#
PEG_TXP0 AN12 PEX_RX0
PEG_TXN0 AM12 PEX_RX0#
PEG_RXP1 C8311 SCD22U10V2KX-1GP PEG_C_RXP1 AH14 PEX_TX1
PEG_RXN1 C8317 SCD22U10V2KX-1GP PEG_C_RXN1 AG14 PEX_TX1#
PEG_TXP1 AN14 PEX_RX1
PEG_TXN1 AM14 PEX_RX1#
PEG_RXP2 C8316 SCD22U10V2KX-1GP PEG_C_RXP2 AK15 PEX_TX2
PEG_RXN2 C8321 SCD22U10V2KX-1GP PEG_C_RXN2 AJ15 PEX_TX2#
PEG_TXP2 AP14 PEX_RX2
PEG_TXN2 AP15 PEX_RX2#
PEG_RXP3 C8322 SCD22U10V2KX-1GP PEG_C_RXP3 AL16 PEX_TX3
PEG_RXN3 C8323 SCD22U10V2KX-1GP PEG_C_RXN3 AK16 PEX_TX3#
PEG_TXP3 AN15 PEX_RX3
PEG_TXN3 AM15 PEX_RX3#
PEG_RXP4 C8324 SCD22U10V2KX-1GP PEG_C_RXP4 AK17 PEX_TX4
PEG_RXN4 C8325 SCD22U10V2KX-1GP PEG_C_RXN4 AJ17 PEX_TX4#
PEG_TXP4 AN17 PEX_RX4
PEG_TXN4 AM17 PEX_RX4#
PEG_RXP5 C8326 SCD22U10V2KX-1GP PEG_C_RXP5 AH17 PEX_TX5
PEG_RXN5 C8327 SCD22U10V2KX-1GP PEG_C_RXN5 AG17 PEX_TX5#
PEG_TXP5 AP17 PEX_RX5
PEG_TXN5 AP18 PEX_RX5#
PEG_RXP6 C8328 SCD22U10V2KX-1GP PEG_C_RXP6 AK18 PEX_TX6
PEG_RXN6 C8329 SCD22U10V2KX-1GP PEG_C_RXN6 AJ18 PEX_TX6#
PEG_TXP6 AN18 PEX_RX6
PEG_TXN6 AM18 PEX_RX6#
PEG_RXP7 C8333 SCD22U10V2KX-1GP PEG_C_RXP7 AL19 PEX_TX7
PEG_RXN7 C8334 SCD22U10V2KX-1GP PEG_C_RXN7 AK19 PEX_TX7#
PEG_TXP7 AN20 PEX_RX7
PEG_TXN7 AM20 PEX_RX7#
PEG_RXP8 C8335 SCD22U10V2KX-1GP PEG_C_RXP8 AK20 PEX_TX8
PEG_RXN8 C8336 SCD22U10V2KX-1GP PEG_C_RXN8 AJ20 PEX_TX8#
PEG_TXP8 AP20 PEX_RX8
PEG_TXN8 AP21 PEX_RX8#
PEG_RXP9 C8337 SCD22U10V2KX-1GP PEG_C_RXP9 AH20 PEX_TX9
PEG_RXN9 C8338 SCD22U10V2KX-1GP PEG_C_RXN9 AG20 PEX_TX9#
PEG_TXP9 AN21 PEX_RX9
PEG_TXN9 AM21 PEX_RX9#
PEG_RXP10 C8339 SCD22U10V2KX-1GP PEG_C_RXP10 AK21 PEX_TX10
PEG_RXN10 C8340 SCD22U10V2KX-1GP PEG_C_RXN10 AJ21 PEX_TX10#
PEG_TXP10 AN23 PEX_RX10
PEG_TXN10 AM23 PEX_RX10#
PEG_RXP11 C8341 SCD22U10V2KX-1GP PEG_C_RXP11 AL22 PEX_TX11
PEG_RXN11 C8342 SCD22U10V2KX-1GP PEG_C_RXN11 AK22 PEX_TX11#
PEG_TXP11 AP23 PEX_RX11
PEG_TXN11 AP24 PEX_RX11#
PEG_RXP12 C8343 SCD22U10V2KX-1GP PEG_C_RXP12 AK23 PEX_TX12
PEG_RXN12 C8344 SCD22U10V2KX-1GP PEG_C_RXN12 AJ23 PEX_TX12#
PEG_TXP12 AN24 PEX_RX12
PEG_TXN12 AM24 PEX_RX12#
PEG_RXP13 C8345 SCD22U10V2KX-1GP PEG_C_RXP13 AH23 PEX_TX13
PEG_RXN13 C8346 SCD22U10V2KX-1GP PEG_C_RXN13 AG23 PEX_TX13#
PEG_TXP13 AN26 PEX_RX13
PEG_TXN13 AM26 PEX_RX13#
PEG_RXP14 C8347 SCD22U10V2KX-1GP PEG_C_RXP14 AK24 PEX_TX14
PEG_RXN14 C8301 SCD22U10V2KX-1GP PEG_C_RXN14 AJ24 PEX_TX14#
PEG_TXP14 AP26 PEX_RX14
PEG_TXN14 AP27 PEX_RX14#
PEG_RXP15 C8351 SCD22U10V2KX-1GP PEG_C_RXP15 AL25 PEX_TX15
PEG_RXN15 C8352 SCD22U10V2KX-1GP PEG_C_RXN15 AK25 PEX_TX15#
PEG_TXP15 AN27 PEX_RX15
PEG_TXN15 AM27 PEX_RX15#

1D05V_VGA_S0
2900mA
PEX_IOVDD AG19 AG21 AG22 AG24 AH21 AH25
C8302 SCU1U10V2KX-1GP
C8303 SCU1U10V2KX-1GP
C8304 SCU10U6D3V3MX-GP
C8305 SCU10U6D3V5MX-GP
C8306 SCU10U6D3V3MX-GP
C8307 SCD22U6D3V5MX-3GP
C8308 SCD22U6D3V5MX-3GP

1D05V_VGA_S0
PEX_IOVDDQ AG13 AG15 AG16 AG18 AG25 AH15 AH18 AH26 AH27 AJ27 AK27 AL27 AM28 AN28
C8312 SCU1U10V2KX-1GP
C8318 SCU1U10V2KX-1GP
C8319 SC4D7U6D3V3KX-GP
C8313 SCU10U6D3V5MX-GP
C8320 SC4D7U6D3V3KX-GP
C8314 SCD22U6D3V5MX-2GP
C8315 SCD22U6D3V5MX-2GP

3D3V_VGA_S0
210mA
PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
C8330 SCD1U10V2KX-5GP
C8331 SC4D7U6D3V3KX-GP
C8332 SC4D7U6D3V3KX-GP

VGA_CORE
R8304 100R2F-L1-GP-U
VDD_SENSE L4 VGA_SENSE → VGA_SENSE 92
GND_SENSE L5 GND_SENSE → GND_SENSE 92
R8305 100R2F-L1-GP-U
NC#P8 P8

R8306 DY 200R2F-4-GP
PEX_TSTCLK_OUT AJ26
PEX_TSTCLK_OUT# AK26

1D05V_VGA_S0
120ohm@100MHz ESR=0.05 150mA
L5804 BLM18PG121SN1D-GP
PEX_PLLVDD AG26
C8348 X7R SCU1U10V2KX-5GP
C8349 X5R SCU1U10V2KX-3GP
C8350 X5R SCD47U6D3V5KX-3GP
C8348 under GPU.
C8349, C8350 & L8504 near GPU.

TESTMODE AK11 GPU_TESTMODE
R8308 10KR2J-3-GP
PEX_TERMP AP29
R8301 2K49R2F-GP
PEX_TERMP

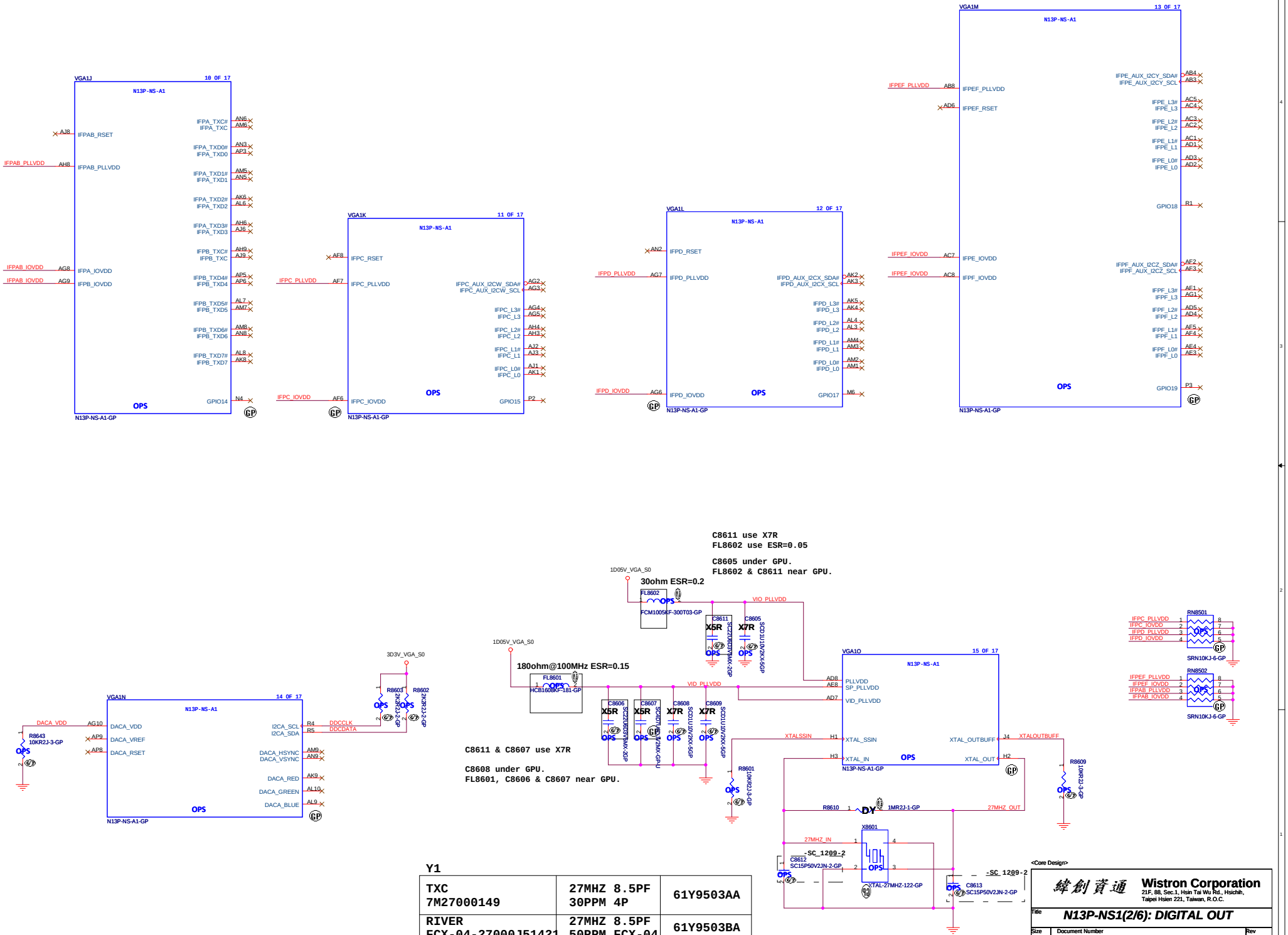
3D3V_VGA_S0
R8307 10KR2J-3-GP
Q8310 2N7002K-2-GP
NV_PEG_CLKREQ#
PEG_CLKREQ# 20
84.2N702.I31
2ND = 84.2N702.031

R8323 DY 0R2J-2-GP
18 DGPU_HOLD_RST#
5,18,27,31,32,36,65,71,77,80,97 PLT_RST#
U8301 74LVC1G08GW-1-GP
3D3V_S5
C8385 SCD1U10V2KX-5GP
PEX_RST#
R8314 100KR2J-1-GP
73.01G08.L04
2nd = 73.7SZ08.DAH

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N13P-NS1(1/6): PEG I/F
Size: C
Document Number: LSS-1
Rev: 1
Date: Wednesday, February 22, 2012
Sheet 83 of 105



Y1

TXC 7M27000149	27MHZ 8.5PF 30PPM 4P	61Y9503AA
RIVER FCX-04-27000J51421	27MHZ 8.5PF 50PPM FCX-04	61Y9503BA

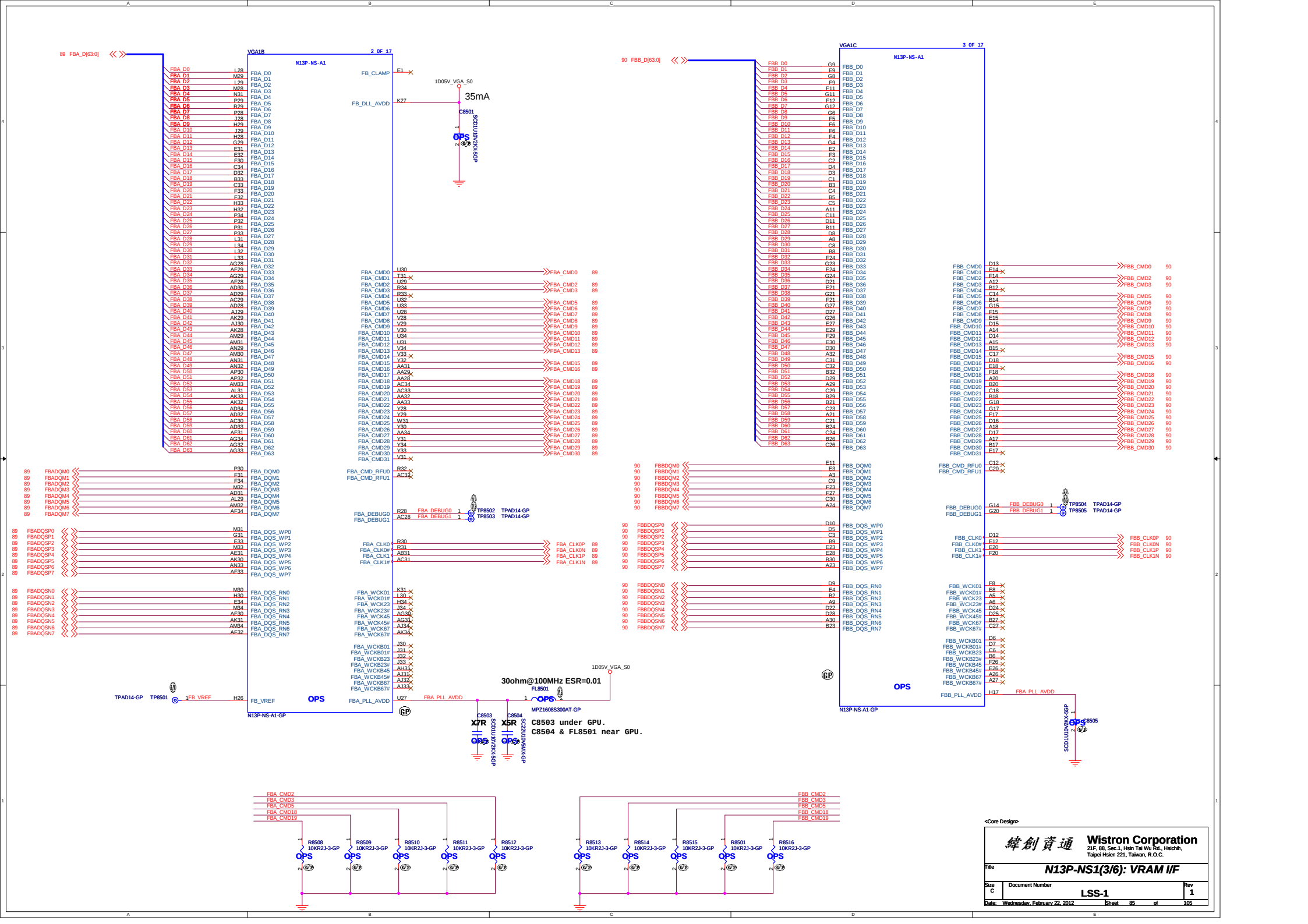
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***N13P-NS1(2/6): DIGITAL OUT***

Size	Document Number	Rev
C	LSS-1	1

Date: Tuesday, February 14, 2012 Sheet 84 of 105



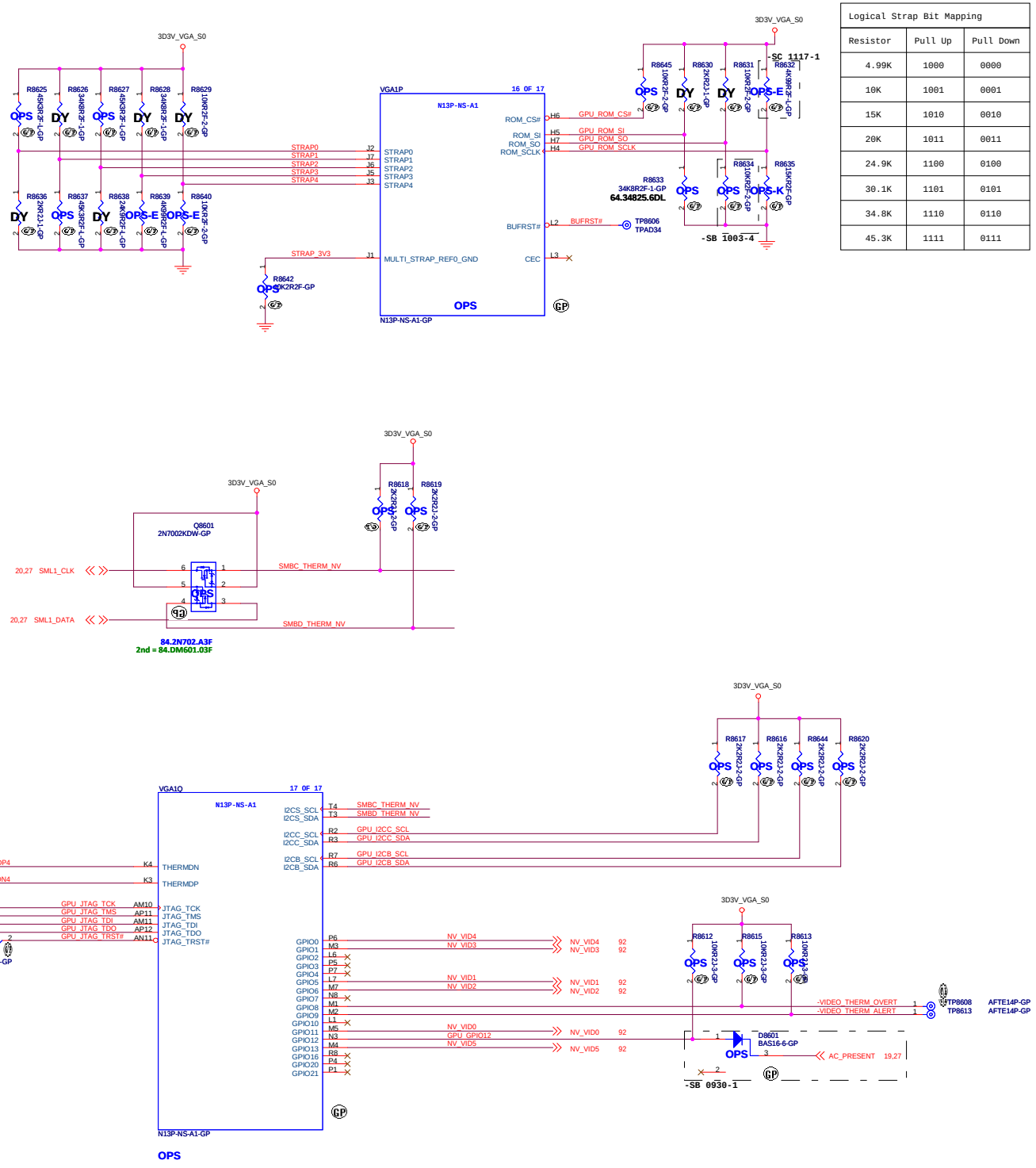
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N13P-NS1(3/6): VRAM I/F

Size	Document Number	Rev
C	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 85 of 105



Logical Strap Bit Mapping		
Resistor	Pull Up	Pull Down
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

GPU_ROM_SI				
Type	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
Hynix (64x16) (0x2)	0	0	1	0
Samsung (64x16) (0x3)	0	0	1	1
Hynix (128x16) (0x6)	0	1	1	0
Samsung (128x16) (0x7)	0	1	1	1

GPU_ROM_SCLK				
Type	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
N13P-NS1	0	0	1	0
Type	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
N13M-GE1	1	0	0	0

GPU_ROM_SO				
Type	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
N13P-NS1	0	0	0	1
Type	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
N13M-GE1	0	1	0	1

STRAP0				
Type	USER[3]	USER[2]	USER[1]	USER[0]
EDID Panel	1	1	1	1

STRAP1				
Type	GGIO_PAD_CFG_ADR[3]	GGIO_PAD_CFG_ADR[2]	GGIO_PAD_CFG_ADR[1]	GGIO_PAD_CFG_ADR[0]
N13P-NS1	0	1	1	1
Type	GGIO_PAD_CFG_ADR[3]	GGIO_PAD_CFG_ADR[2]	GGIO_PAD_CFG_ADR[1]	GGIO_PAD_CFG_ADR[0]
N13M-GE1	0	1	1	0

STRAP2				
Type	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
N13P-NS1	1	1	1	1
Type	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
N13M-GE1	1	0	0	0

STRAP3_N13M-GE1 ONLY				
Type	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
EDID Panel	0	0	0	0

STRAP4_N13M-GE1 ONLY				
Type	Reserved	Reserved	PCIE_MAX_SPEED	DP_PLL_VDD33V
EDID Panel	0	0	0	1

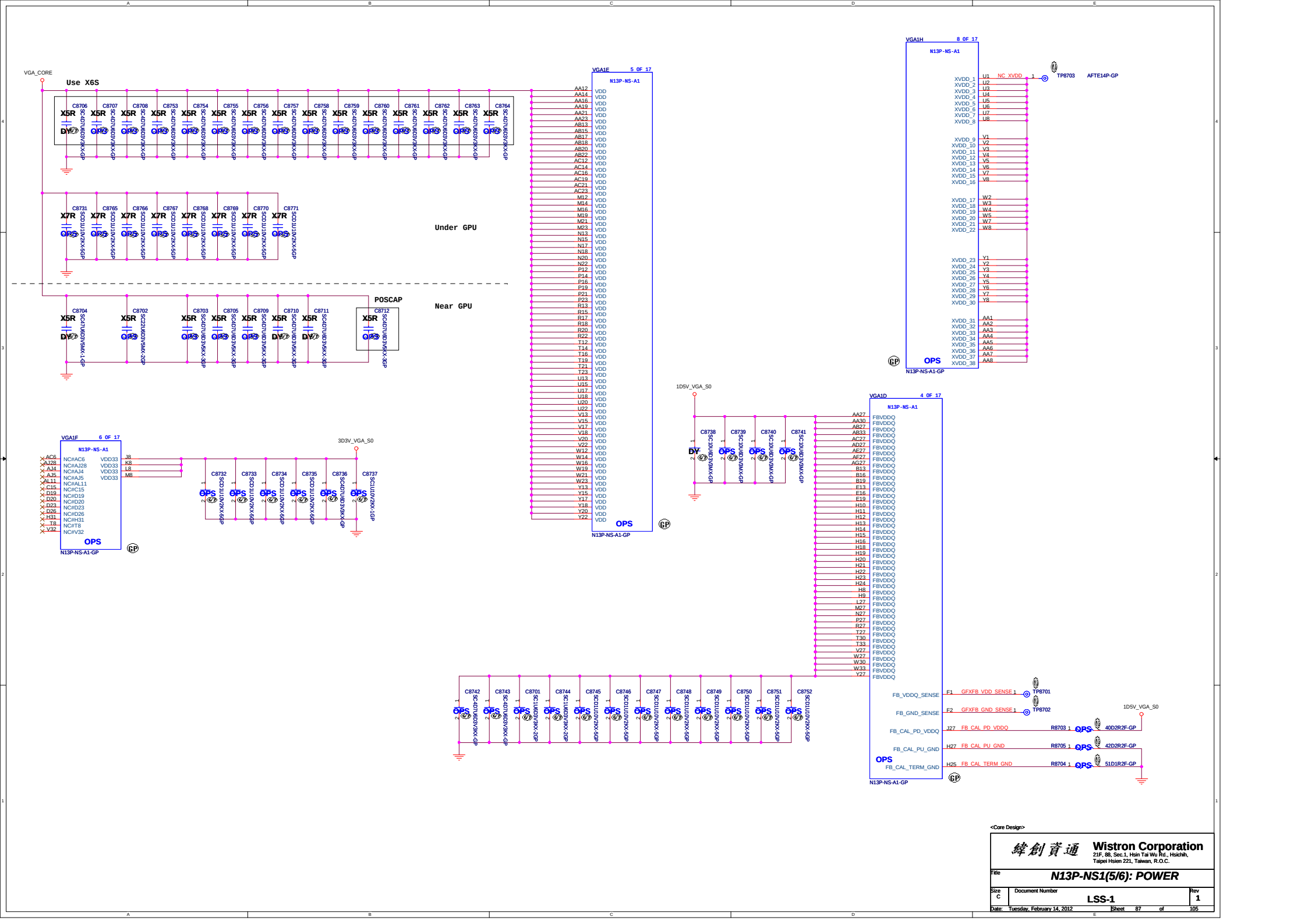
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N13P-NS1(4/6): GPIO

Size	Document Number	Rev
C	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 86 of 105



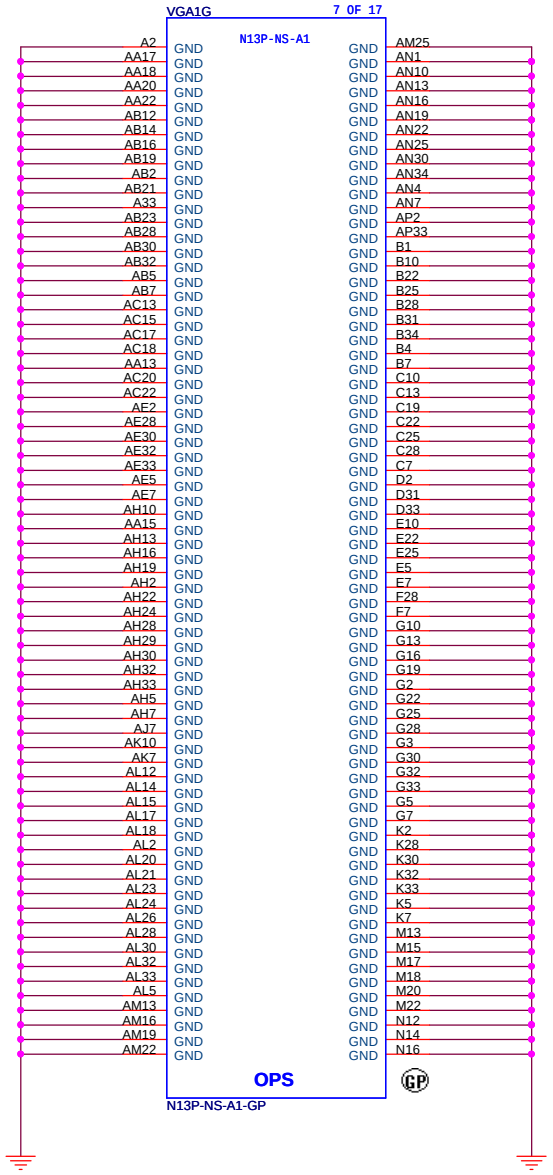
<Core Design>

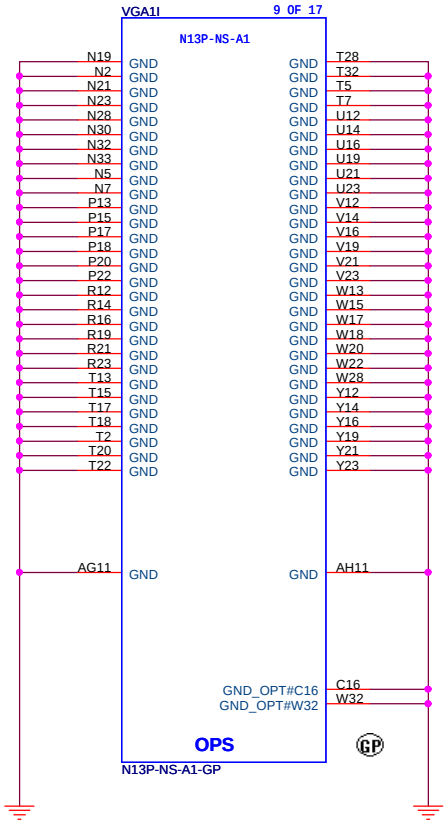
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N13P-NS1(5/6): POWER

Size	Document Number	Rev
C	LSS-1	1

Date: Tuesday, February 14, 2012 Sheet 87 of 105





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N13P-NS1(6/6): GND

Size	Document Number	Rev
B	LSS-1	1

Date: Tuesday, February 14, 2012 Sheet 88 of 105

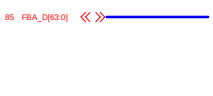
TABLE
DDR3 VIDEO MEMORY

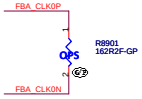
	HYNIX 1GBITS (64Mx16)	SAMSUNG 1GBITS (64Mx16)
U100 U111 U99 U108 U107 U110 U105 U109	H5TQ1G63DFR-11C	K4W1G1646G-BC11

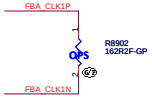
LOGIC

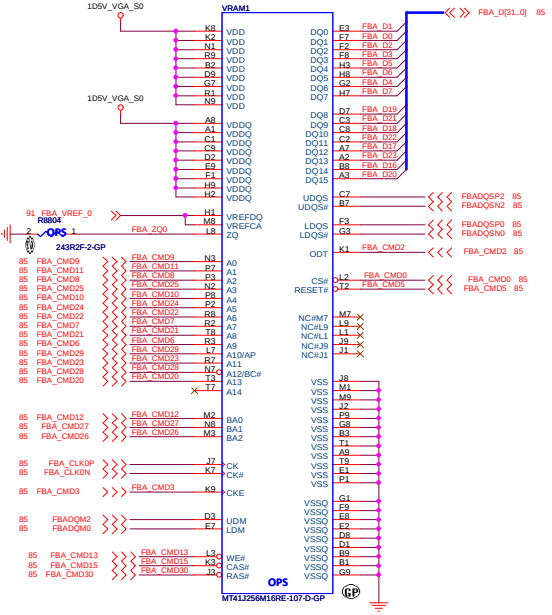
FB CMD mapping Mode D-N12x

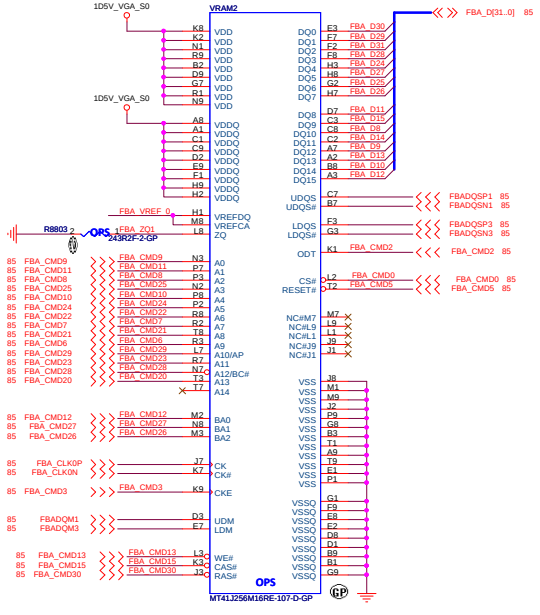
Use Micron MT41J256M16RE-107-D for Layout placement

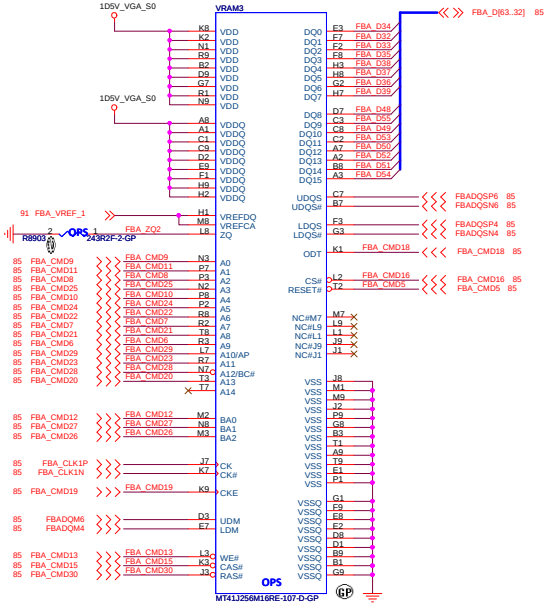


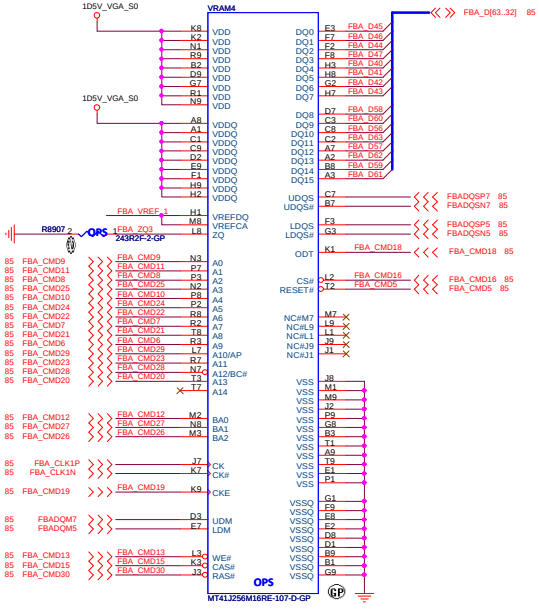




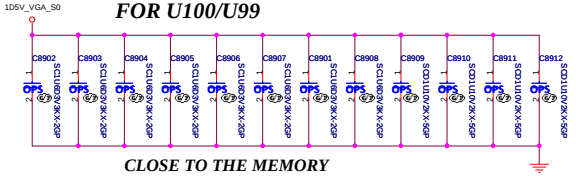






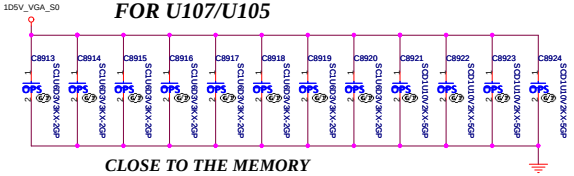


FOR U100/U99



CLOSE TO THE MEMORY

FOR U107/U105



CLOSE TO THE MEMORY

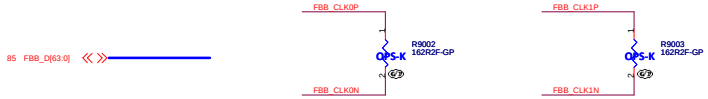
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

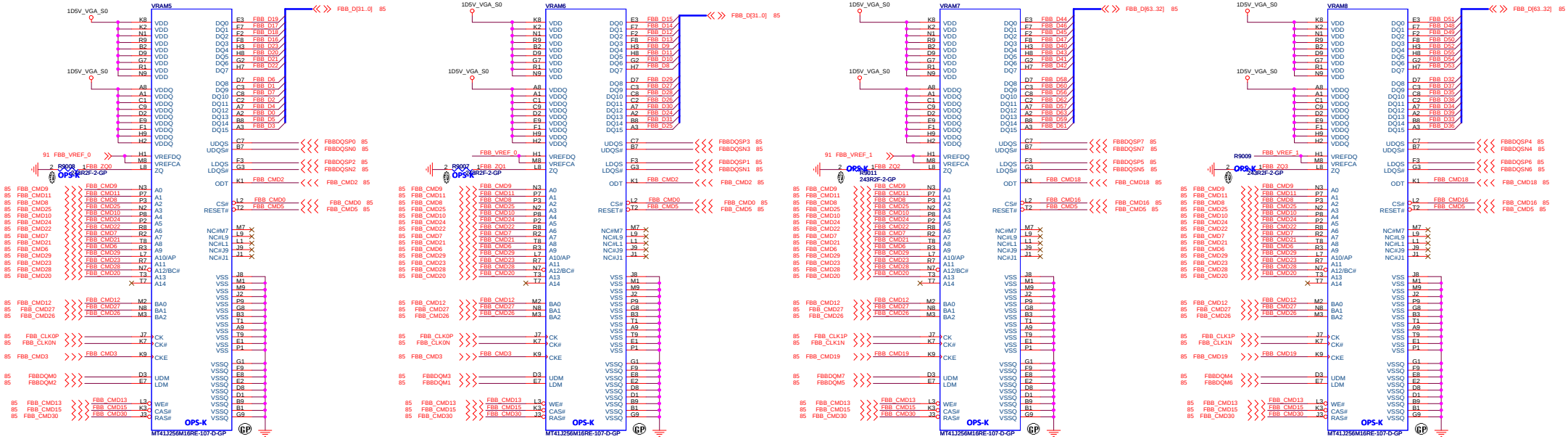
Title: VRAM CHANNEL-A

Size: Custom | Document Number: LSS-1 | Rev: 1

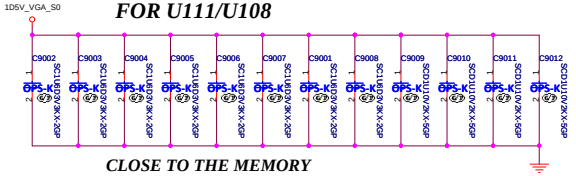
Date: Wednesday, February 22, 2012 | Sheet 89 of 105



FB CMD mapping Mode D-N12x

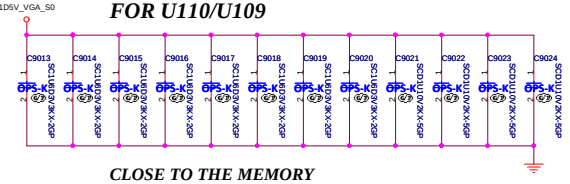


FOR U111/U108



CLOSE TO THE MEMORY

FOR U110/U109



CLOSE TO THE MEMORY

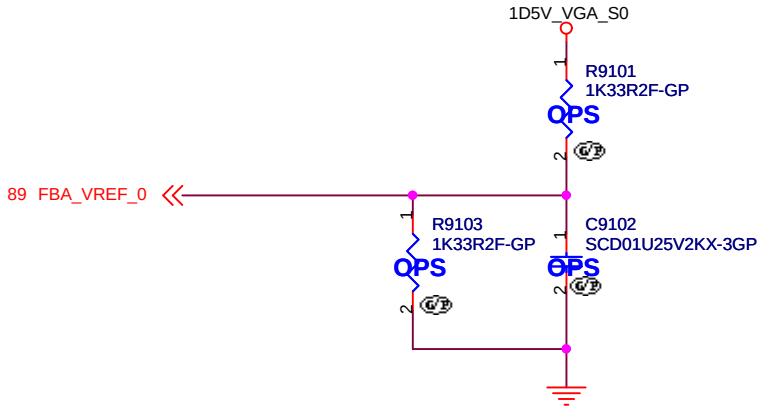
<Core Design>

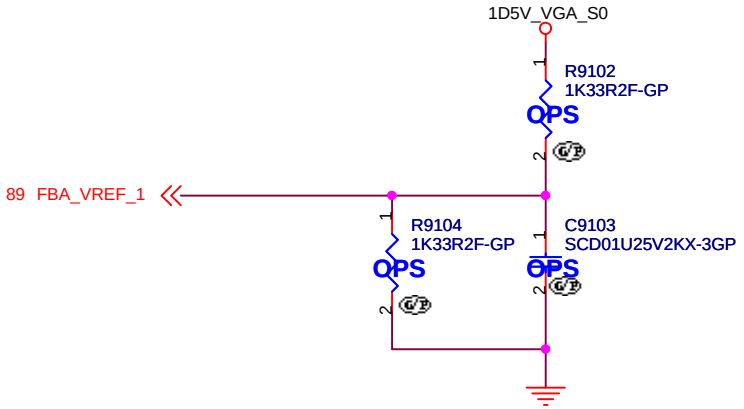
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

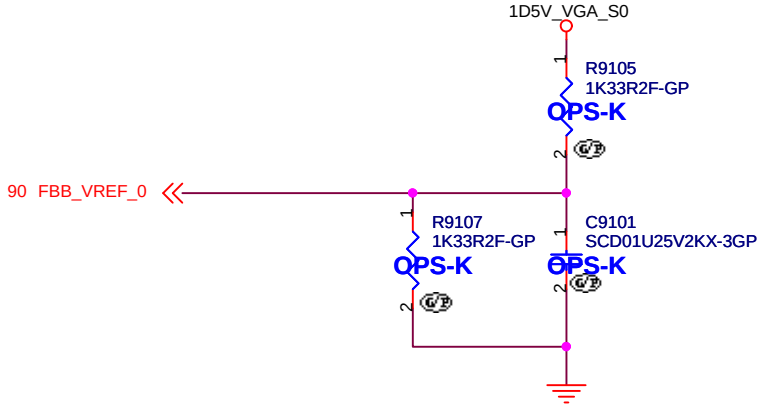
Title: VRAM CHANNEL-B

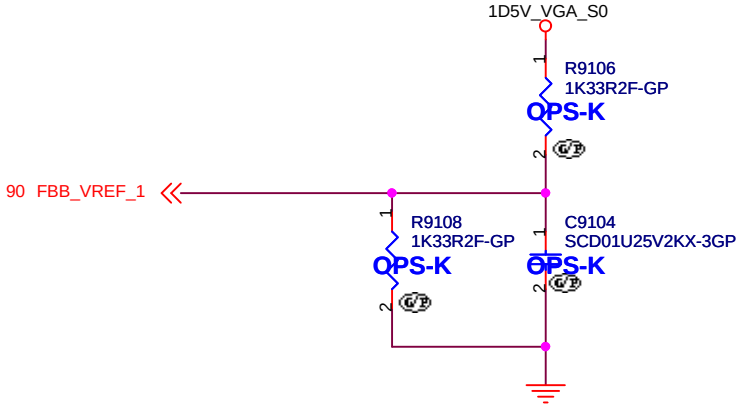
Size: Custom | Document Number: LSS-1 | Rev: 1

Date: Wednesday, February 22, 2012 | Sheet 90 of 105









<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VIDEO MEMORY TERMINATION***

Size	Document Number	Rev
A4	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 91 of 105

SSID = PWR.Plane.Regulator_GFX

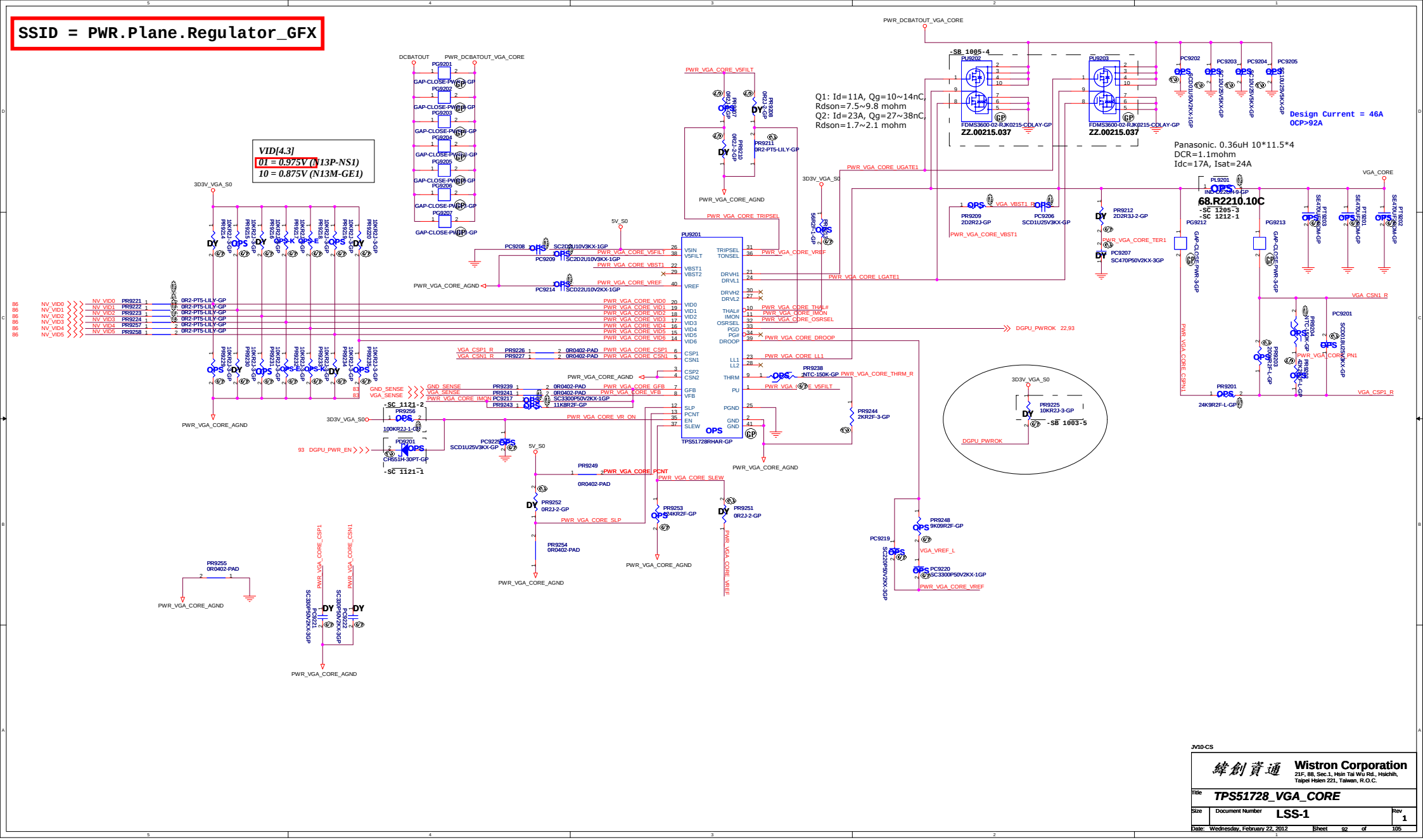
VID[4.3]
01 = 0.975V (N13P-NS1)
10 = 0.875V (N13M-GE1)

Q1: Id=11A, Qg=10~14nC,
Rdson=7.5~9.8 mohm
Q2: Id=23A, Qg=27~38nC,
Rdson=1.7~2.1 mohm

Design Current = 46A
OCP>92A

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

68.R2210.10C
-SC 1205-3
-SC 1212-1

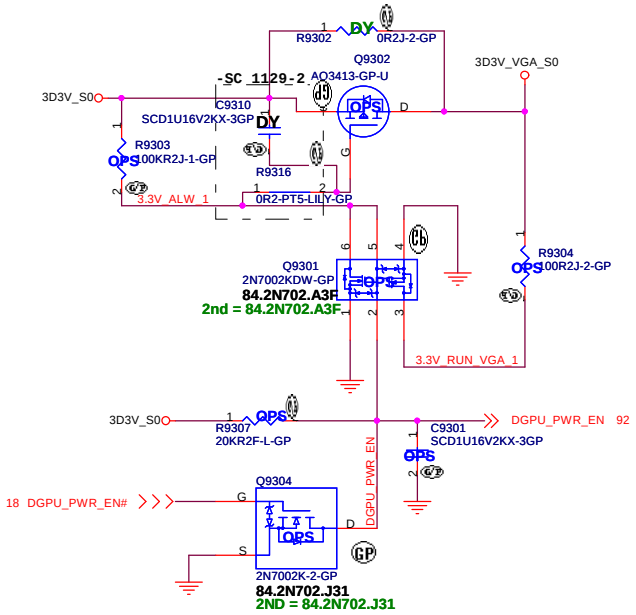


JV10-CS

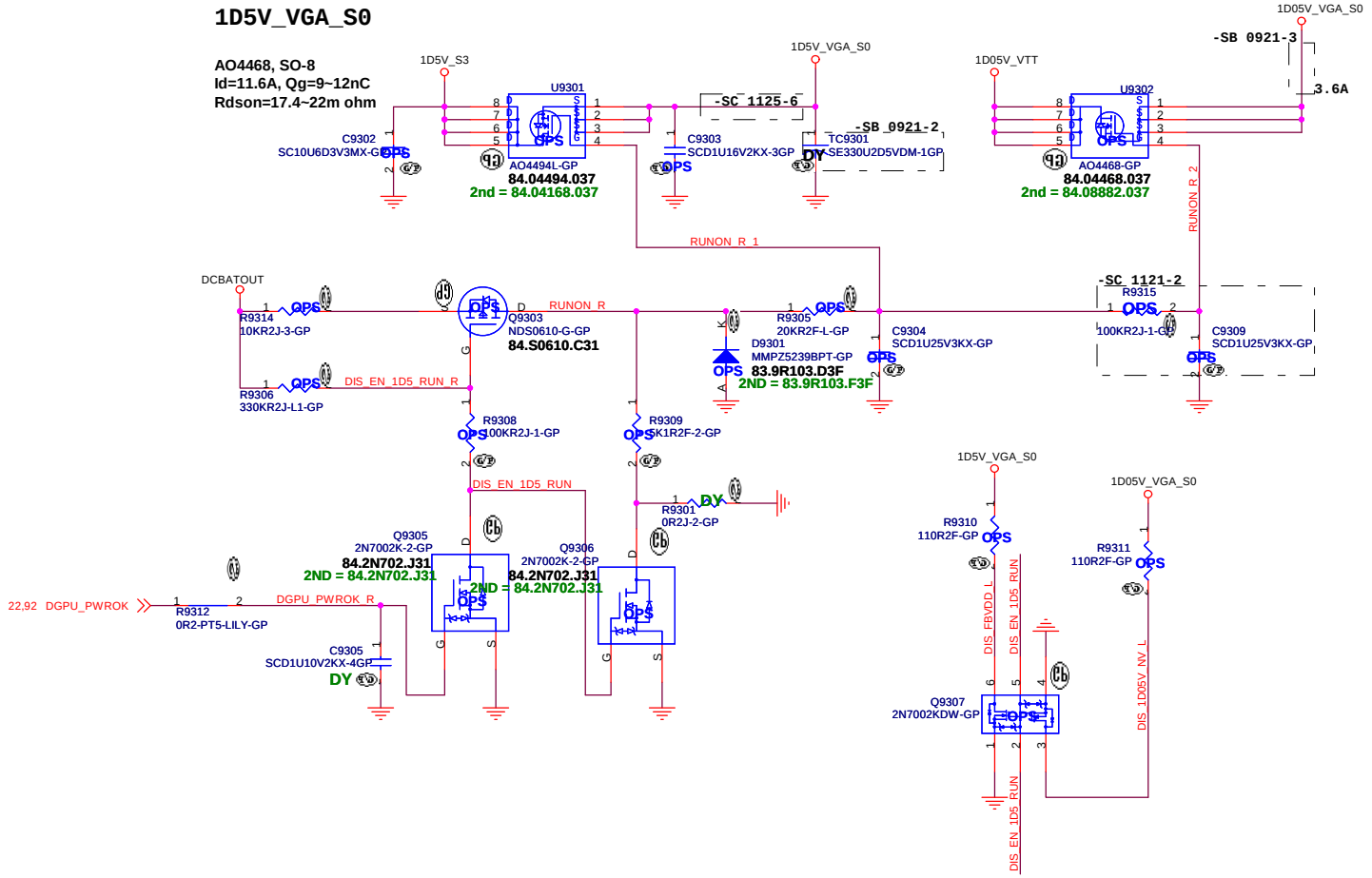
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51728_VGA_CORE**
Size: Document Number: **LSS-1** Rev: 1
Date: Wednesday, February 22, 2012 Sheet 92 of 105

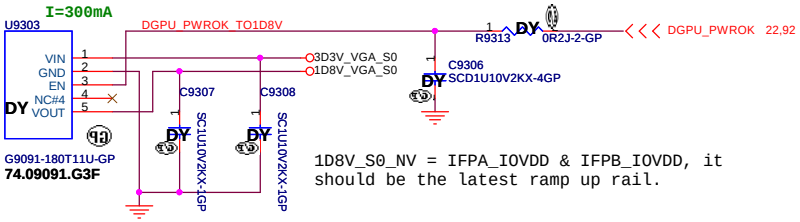
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0



+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DISCRETE VGA POWER**		
Size: A3	Document Number: **LSS-1**	Rev: 1
Date: Wednesday, February 22, 2012	Sheet 93 of 105	

5 4 3 2 1

D

C

B

A

BLANK

<Variant Name>

緯創資通

Wistron Corporation

21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: <Title>		
Size: A4	Document Number: LSS-1	Rev: 1
Date: Friday, February 10, 2012	Sheet 94 of 105	

BLANK

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LSS-1	1

Date: Friday, February 10, 2012 Sheet 95 of 105

BLANK

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
TOUCH PANEL

Size	Document Number	Rev
A4	**LSS-1**	**1**

Date: Friday, February 10, 2012 Sheet 96 of 105

CPU boss

H4 HOLE256R142-GP ZZ.00PAD.801
H5 HOLE256R142-GP ZZ.00PAD.801
H6 HOLE256R142-GP ZZ.00PAD.801
H7 HOLE256R142-GP ZZ.00PAD.801

VGA boss

H1 HOLE256R142-GP ZZ.00PAD.801
H2 HOLE256R142-GP ZZ.00PAD.801
H3 HOLE256R142-GP ZZ.00PAD.801

TCM STD-OFF

H8 STF217R115H121-GP 34.4Y801.011 DY
H9 STF217R115H121-GP 34.4Y801.011 DY
-SC 1208-1

Mini PCI STD-OFF -SC 1128-1

H10 STF256R117H119-GP 34.4B502.001 HALF
H12 STF256R117H119-GP 34.4B502.001 LONG
H11 STF256R105H158-GP 34.4T301.001
H13 STF256R105H158-GP 34.4T301.001

Check test point

3D3V_S0		TP9702
3D3V_AUX_S5		TP9703
3D3V_S5		TP9704
5V_S5		TP9705
19,27 PM_PWRBTN#		TP9706
5,22 H_CPUPWRGD		TP9701
27,36 S5_ENABLE		TP9707
5,18,27,31,32,36,65,71,77,80,83 PLT_RST#		TP9708

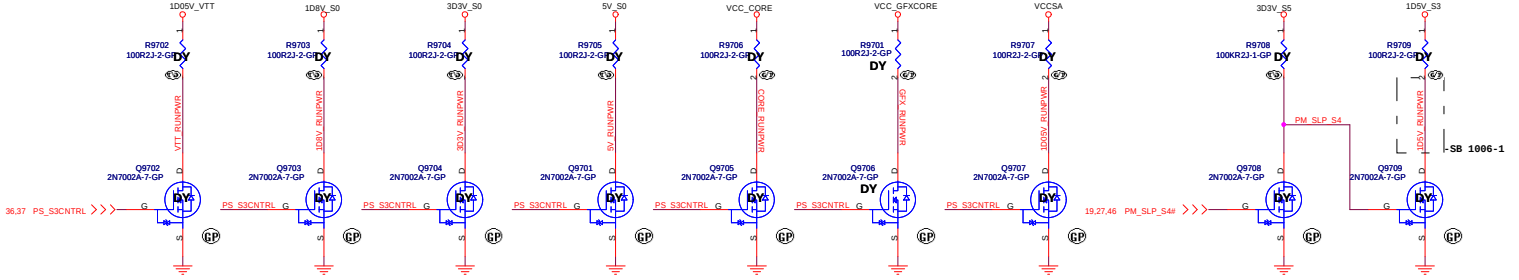
Test Point放在Dimm Door打開可量測處

SPR1 SPRING-53-GP-U 34.4B433.001
SPR2 SPRING-53-GP-U 34.4B433.001

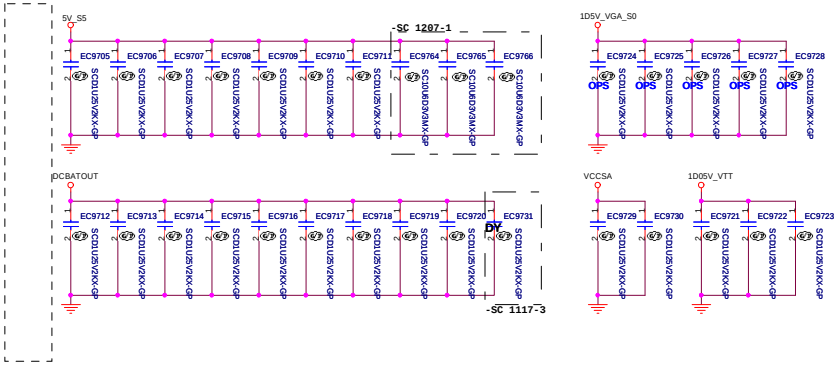
Structure boss

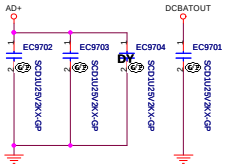
H14 HOLE315X315R91-S1-GP ZZ.00PAD.581
H15 HOLE315X315R91-S1-GP ZZ.00PAD.581
H16 HOLE315X315R91-S1-GP ZZ.00PAD.581
H17 HOLE315X315R91-S1-GP ZZ.00PAD.581
H18 HOLE315X315R91-S1-GP ZZ.00PAD.581
H19 HOLE237R95-GP ZZ.00PAD.921
H20 HOLE237R95-GP ZZ.00PAD.921
H21 HOLE237R95-GP ZZ.00PAD.921
H22 HOLE237R95-GP ZZ.00PAD.921
H23 HOLE237R95-GP ZZ.00PAD.921
H24 HOLE237R95-GP ZZ.00PAD.921

For Discharge

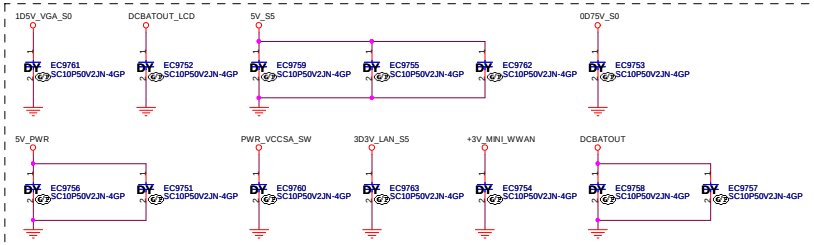


EMI





RF -SB 0928-2



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A2 | Document Number: LSS-1 | Rev: 1
Date: Wednesday, February 22, 2012 | Sheet 97 of 105

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Change History***

Size	Document Number	Rev
A4	LSS-1	1

Date: Friday, February 10, 2012 Sheet 98 of 105

5 4 3 2 1

D

C

B

A

(Blanking)

<Variant Name>

緯創資通

Wistron Corporation

21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: <Title>		
Size: A4	Document Number: LSS-1	Rev: 1
Date: Monday, February 20, 2012	Sheet 99 of 105	

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A4	LSS-1	1

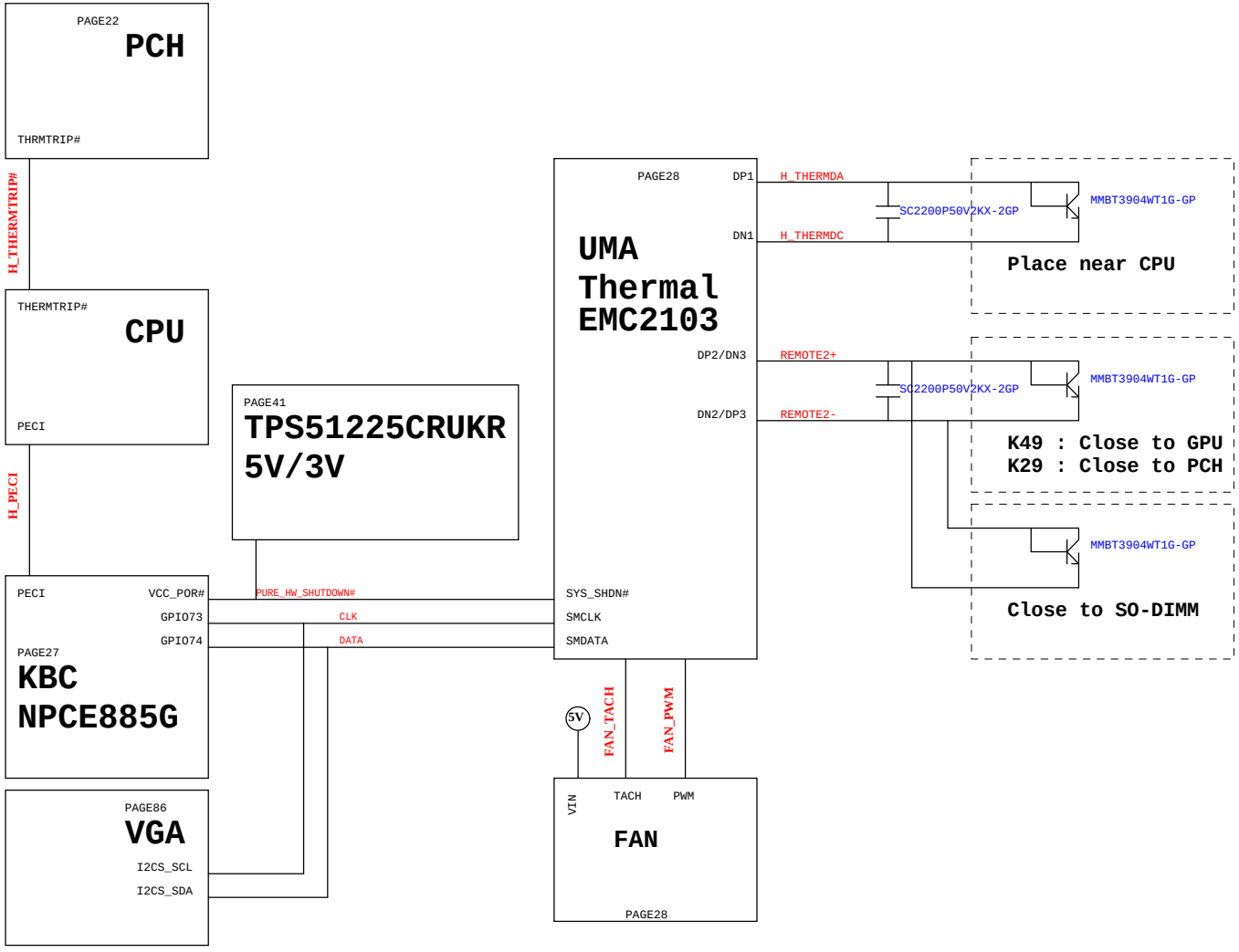
Date: Monday, February 20, 2012 Sheet 100 of 105

(Blanking)

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SMBUS Block Diagram***	
Size A4	Document Number **LSS-1**	Rev **1**
Date: Monday, February 20, 2012	Sheet 101 of 105	

Thermal Block Diagram



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	LSS-1	1

Date: Wednesday, February 22, 2012 Sheet 102 of 105

Change notes - Page 1

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
SB	09/21	1	27	Change R2739 from 10KR to 20KR	PCB version goes into SB.	EE
		2	93	Move TC9301 to connect R9314 pin1 side	Place capacitor closer to electric load.	EE
		3	93	Delete R9315	Layout space constraint.	EE
		4	56	Delete TP5601 and connect HDD1 pin18 to GND	Remove unused test point.	EE
		5	42	Add PR4271 0-ohm resistor	Link power good signal of VCORE VRM.	EE
	09/22	1	37	Add R3731 and reserve R3732 0-ohm resistor	Follow Intel S3 power reduction circuit.	EE
		2	57	Add C5721~C5724 0.01uF 0402 capacitor	Follow Intel eSATA with repeater design guide.	EE
	09/23	1	49,59	Modify connector for LVDS1, RJ45	Drawing updated by ME.	ME
		2	42	Update PU4201 symbol	Revision change by vendor.	Power
	09/27	1	57	Rename duplicated net name	Existed net name suffix "_C", change to "_J".	EE
		2	45	Delete power gap between source and high-side MOS	Layout space constraint.	EE
	09/28	1	59	Swap net on transformer	Smoothen layout routing.	EE
		2	97	Reserve RF required capacitors	Request by RF team.	RF
	09/29	1	50,51	Change CRT1 and HDMI1 connector	ME drawing update.	ME
		2	42,43,44	Empty PC4201,PC4228,PC4229; stuff 0.1uF capacitor on PC4303,PC4317,PC4402; PC4236 change to 56pF; PC4238 change to 220pF; PR4201 to 21.5R; PR4210 to 475R; PR4215 to 15.8KR; PR4222 to 60.4KR; PR4227 to 56.2KR; PR4232,PR4256 to 499R; PR4235 to 30.1KR; PR4236 to 1.78KR; PR4237 to 845R; PR4238 to 1.3KR; PR4239 to 0R; PR4249 to 7.87KR; PR4255 to 30.1KR; PR4264 to 20KR; PR4246 to 715R; PC4213 to 4700pF	Request by Power Team.	Power
		3	65	Change R6502, short-pad to 0R-0402 and default empty	Reserve for future bluetooth module feature.	EE
	09/30	1	86	Add D8601 and connect net "AC_PRESENT"	Inform GPU about system power status.	EE
		2	38	Change connector "DCIN1"	ME design change.	ME
	10/3	1	68	Change part reference from "BTYL0" to "BTYL2"	To prevent OrCAD system bug on BOM creation.	EE
		2	36	Remove U3604 U3605 and related net	Remove defect power enable circuit.	EE
		3	45	Change PR4502 to 1KR, PC4502 to 0.1uF	Delay enable sequence for 1.05V power resume from S3.	Power
		4	86	Change R8634 from 30.1KR to 10KR	Set GPU strap following vendor debug result.	EE
		5	92	Set R9225 default empty	Double pull-up with R2223.	EE
		6	24	Change net name from 1D05V_VTT_VCCASW to 1D05V_VTT	Connect to 1D05V_VTT.	EE
	10/4	1	19,22	Empty R1923,R1924, move R2220 PU 3D3V_S5	Follow Intel design checklist and power sequence.	EE
		2	33	Remove TP3312 and connect chassis to GND	Better signal shielding.	EE
		3	22	Seperate RN2203, R2231 PU 3D3V_S0, R2232 PU 3D3V_S5	Follow Intel design checklist.	EE
	10/5	1	18	Stuff R1817, 8.2KR	Follow Intel design checklist.	EE
		2	68	Rename net "DC_BATFULL#_PWR" to "SATA_LED#_PWR"	Correct LED lighting behavior.	EE
		3	45	Empty PC4502 PR4507, stuff PR4506 as 8.87KR, PR4508 as 10KR, and PR4502 as 0R	Fine tuned 1.05V power sequence.	Power
		4	92	Change PU9202 PU9203 footprint	Change footprint for multiple component sources.	Power

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size: A3 | Document Number: LSS-1 | Rev: 1

Date: Friday, February 10, 2012 | Sheet 103 of 105

Change notes - Page 2

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
SB	10/6	1	97	Change net name from "3D3V_RUNPWR" to "1D5V_RUNPWR"	Duplicated net name.	EE
	10/7	1	38,40	Change PU3801 PU4001 PU4002 PU4004 PU4005	Change by Power Team request.	Power
		2	45	Change PR4506 to 18KR and PR4508 to 20KR	Change by Power Team request.	Power
		3	28	Empty R2811 and stuff R2810	Solve T8 shutdown can't be performed issue.	Power
	10/11	1	41	Change PL4101	Change by Power Team request.	Power
	10/13	1	57	Stuff selected parts	Stuff parts for E49 USB2.0 port function.	EE
		2	63	Stuff selected parts	Stuff parts for Bluetooth module function.	EE
		3	20	Stuff RN2016	dGPU can be acknowledged when RN2016 stuffed.	EE
SC	11/17	1	86	Change R8632 from 15KR to 4.99KR	nVidia specificaiton updates strap setting.	EE
		2	9	Rename net N11126255 to 1D5V_S0_VDDQ	Give regular name to power net.	EE
		3	97	Add EC9731 0.1uF, 25V	Request by EMC team.	EMC
	11/21	1	92	Add diode PD9201	For VGA_CORE enable signal discharge circuit.	EE
		2	92,93	Change PR9256 to 100KR, add R9315 100KR, C9309 0.1uF	Fine tune GPU power sequence.	EE
	11/23	1	49	Add R4913 R4914 0R power shunt	Reserved for hall effect sensor power source.	EE
		2	59	Add AFTP5901 - AFTP5912	Place AFTP for manufactory.	EE
		3	22,59	Add RTC battery detect circuit.	For factory manufacturing process.	EE
	11/24	1	49	Change TP4922 net name from 3D3V_S5 to 3D3V_HALL	Follow AFTP rule.	EE
	11/25	1	69	Add switch TPLBN1 and TPRBN1, and change TPAD1	Requested by ME.	ME
		2	21,68	Modify APS LED circuit	Modify design to follow VB480.	EE
		3	27,65	Add net "WLAN_WAKE#" and related circuit	To support wake on wireless LAN function.	EE
		4	27	Add net "RJ45_DET#" circuit	For EC to sense RJ45 cable stuff or not.	EE
		5	27,56,66	Add HDD and mSATA detect circuit	For EC to sense devices stuff or not.	EE
		6	93	Remove R9314 10mR	Reduce voltage drop on power rail 1D5V_VGA_S0.	EE
	11/28	1	97	Modify mini-card stand-off hole	Requested by ME.	ME
		2	58	Change SPK1 and MIC1, add SPK2	Requested by ME.	ME
	11/29	1	13	Reserve R1351	Reserved for AOAC power	EE
		2	93	Reserve C9310 and R9316 soft start circuit	Reserved for power tunning.	EE
	11/30	1	68	Change BTYL1	Downsize LED height for factory request.	EE
		2	31	Modify L3101	Downsize and follw project LGN-1.	EE
	12/01	1	65,66,69	Change TPAD1, WLAN1, and WWAN1	ME changed.	ME
	12/05	1	69,82	Change TPAD1, BTNCN1, and BTNCN2	ME changed.	ME
		2	64	Reverse FPCN1 pin define	Reverse pin define to match ME cable define.	EE
		3	43,44,92	Change PL9201, PU4301, PU4302, and PU4401	Changed by Power Team Request.	Power
		4	41	PR4102 110K to 78.7K,PR4101 150K to 127K	Adjust Over Current Protection parameter by Power Team.	Power
		5	42,46	PR4602 9.76K to 8.06K, PR4264 20K to 17.8K	Adjust 1.5V OCP, and fine tune VCORE load line.	Power

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size: A3 | Document Number: LSS-1 | Rev: 1

Date: Friday, February 10, 2012 | Sheet 104 of 105

Change notes - Page 3

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
SC	12/05	6	27	Reserve R2747 and R2748 pull-up resistors	Follow LGN-1 for LED issue.	EE
		7	27	Add R2731 (63.10034.1DL) & C2712 (78.10134.1FL)	Follow LGN-1 for AD_OFF issue.	EE
	12/06	1	39	Add AFTE,TP3909 TP3803 TP3804 TP6003 TP6004	Add by AFTE request to meet DFX	AFTE
	12/07	1	97	Add EC9764 EC9765 EC9766	Add by EMC team request.	EMC
		2	40	Change PU4003 pin 14 to connect to GND	Power team design change to ease noise coupling.	Power
		3	41	Change PU4103 from TPS51225 to TPS51225C	Power team changes to use new version IC.	Power
	12/08	1	97	Change H8, H9 part	Change by ME request.	ME
		2	69	Modify to use AFTE Test Point	Add by AFTE request to meet DFX.	AFTE
		3	22	Add more NCTF test points	For more NCTF test points.	EE
	12/09	1	31	Change L3101 part number	The same part with different feeding direction for SMT	EE
		2	20	Change C2007 C2008 C8612 C8613 to 15pF	Changed by vendor measurement report.	EE
		3	24	Stuff C2401	Occupy the location to follow CRB.	EE
		4	22	Empty R2214	Leave vacancy for nominal voltage level.	EE
	12/12	1	92	Change PL9201 part number	Change by Power Team request.	Power
	12/15	1	62	Change USB3P1 and USB3P2 part number	Change by ME request to use blue color USB connector.	ME
-1	1/02	1	8,9	Change capacitor to 22uF	To solve Volterra power lose issue.	Power

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size: A3 | Document Number: LSS-1 | Rev: 1

Date: Friday, February 10, 2012 | Sheet 105 of 105