G-Note Montevina Block Diagram

PCB STACK UP
8L

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU CORE(ISL6266A) pg 45

CPU Penryn
478P (uPGA)/35W
pg 4~5

CPU THERMAL SENSOR pg 5

FSB 667/800/1066

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

CLOCK GEN
SLG8SP568/
ICS9LPRS393(QFN68)
pg 3

VCCP +1.5V AND GMCH
1.05V(RT8204)
pg 43

DDRIII-SODIMM1 pg 11~12
DDRIII-SODIMM2 pg 11~12
DDRIII 800/1066 MT/s

DDR III (TPS51116REGR)
1.5VSUS/SMDDR_VTERM
/SMDDR_VREF
pg 42

NORTH BRIDGE
Cantiga
pg 6~10

27MHz

VGACORE(MAX8792ETD+T)
pg 46

PCI-Express 16X

AMD
M92-S2 XT
pg 13~19

HDMI pg 26
CRT pg 24
LCD CONN pg 25

DMI LINK

32.768KHz

SATA - HDD pg 30
SATA - CD-ROM pg 30
SATA0 300MB
SATA1 300MB

SOUTH BRIDGE
ICH-9M
pg 20~23

USB2.0

USB2.0 Ports X3 pg 30
USB+eSATA Port X1 pg 30
BlueTooth CON. pg 32
Fingerprint CON. pg 32
Camera CON. pg 25
WWAN Socket pg 36
SIM Card Socket pg 36

PCI-E

X3 Mini PCI-E Card X 2
(WLAN/ WiMAX) pg 36
(UWB) pg 37

X1 LAN (10/100/1G) REALTEK RTL8111DL pg 29
25MHz
RJ45 CON. pg 29

X1 PCI Express Card Socket pg 34

X1 Card-Reader Controller JMB385 pg 27
Memory CardReader 7-in-1 pg 27

Azalia

AUDIO CODEC
(ALC269Q)
pg 28

Internal Speakers. pg 28

Internal Digital Array MIC. pg 28
External MIC. pg 28
HEADPHONE JACK pg 28

SYSTEM POWER(ISL6237) pg 44
SYSTEM CHARGER(ISL88731A) pg 41

32.768KHz
LPC

EC (ITE)
(IT8502E/JX)
pg 39

Keyboard Touch Pad pg 31
G-SENSOR(LIS244ALTR) pg 33

FAN pg 31
SPI EEPROM pg 39

G-Note Montevina
Quanta Computer Inc.

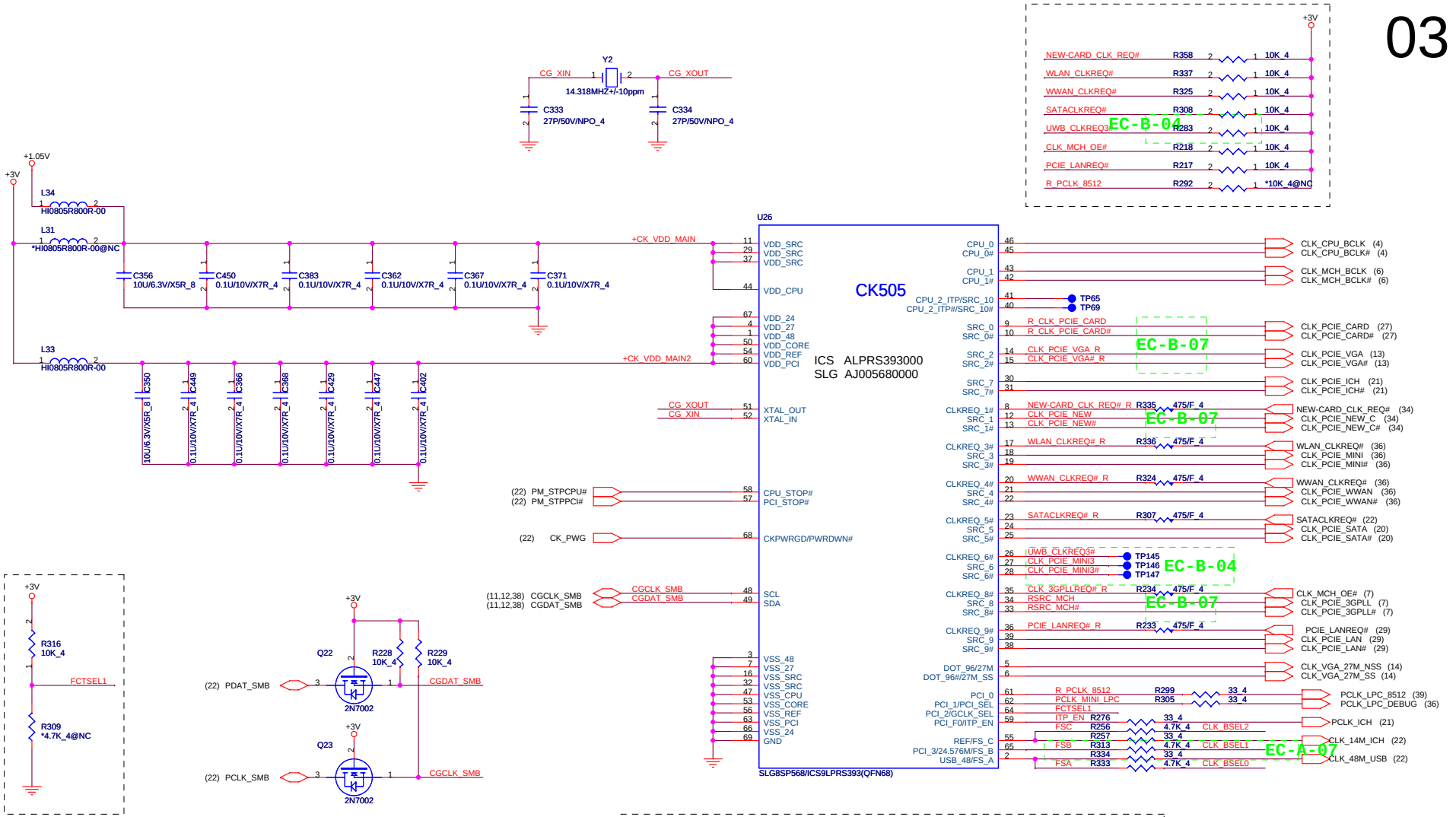
Size	Document Number	Rev
Custom	Block Diagram	2A
Date: Tuesday, March 03, 2009	Sheet 1 of 55	

Will chang after circuit finished

02

Power States

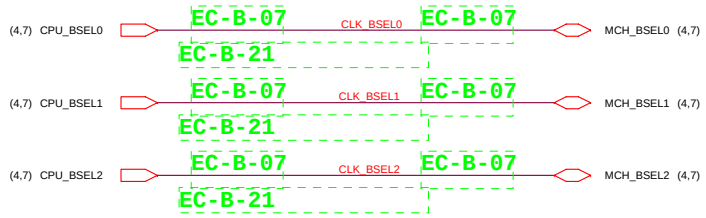
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+19V	25,40,41,42,43,44,45,46,47	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	20,23,39	RTC		S0~S5
3VPCU	+3.3V	20,25,29,31,37,39,40,41,44	8051 POWER		S0~S5
5VPCU	+5V	27,30,37,40,41,42,43,44,45,46,47	LCD/CHARGE POWER		S0~S5
+15V	+15V	25,40,44,47	LARGE POWER	5VPCU	S0~S5
LANVCC	+3.3V	29,40	LAN POWER	LAN_ON	
5VSUS	+5V	25,30,37,40,43,45,46	SLP_S5# CTRLD POWER	SUSON	
3VSUS	+3.3V	21,22,34,35,36,39,40,45	SLP_S5# CTRLD POWER	SUSON	
1.8VSUS	+1.8V	40,43,47	SODIMM POWER	SUSON	
+0.9V_DDR_VTT	+0.9V		SODIMM POWER	MAINON	
+5V	+5V	23,24,25,26,28,30,31,39,40,41	SLP_S3# CTRLD POWER	MAINON	
+3V	+3.3V	3,5,7,10,11,12,14,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,47	SLP_S3# CTRLD POWER	MAINON	
+1.8V	+1.8V	14,15,16,17,18,19,47	VGA POWER	MAINON	
+1.5V	+1.5V	5,10,20,21,22,23,34,35,36,40,43	CALISTOGA/ICH8 POWER	MAINON	
+1.05V	+1.05V	3,4,5,6,7,9,10,20,23,40,43,45	CPU/CALISTOGA/ICH8 POWER	MAINON	
VCC_CORE	+0.7V~+1.77V	4,5,40,45	CPU CORE POWER	VRON	
LCDVCC	+3.3V	25	LCD Power	INT_DISP_ON & EXT_LVDS_DIGON	
+5VHDD	+5V	30	HDD Power	MAINON	
MBATV	+10V~+17V	39,41	MAIN BATTERY	D/C#	



GCLK_SEL = FCTSEL1

FCTSEL1 (PIN64)	PIN5	PIN6
0	DOT96	DOT96#
1	27Mout-NSS	27Mout-SS

CPU Clock select

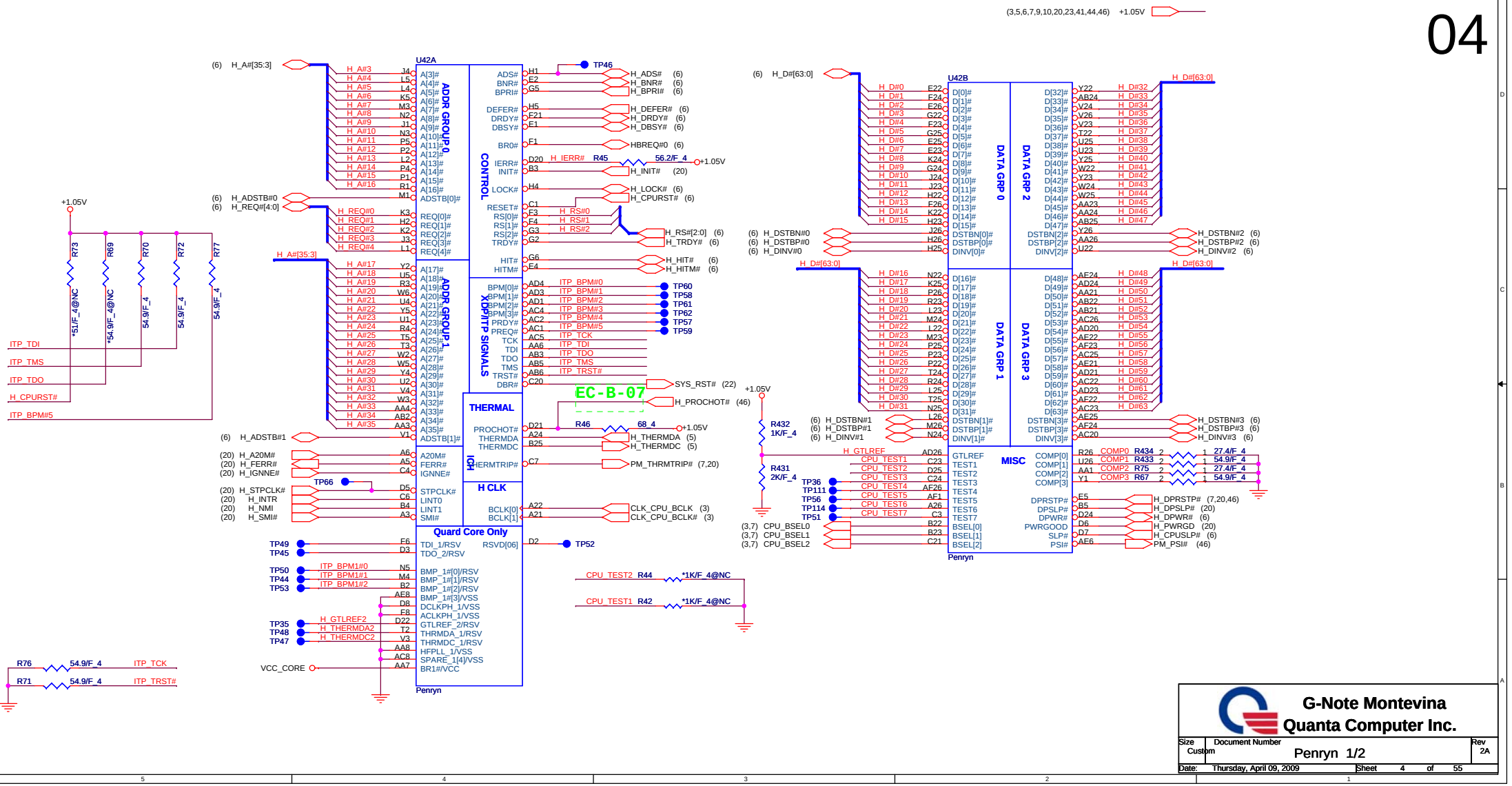


FSC	FSB	FSA	CPU	SRC	PCI
0	0	0	266.6	100	33
0	0	1	133.3	100	33
0	1	0	200.0	100	33
0	1	1	166.6	100	33
1	0	0	Reserved		
1	0	1	Reserved		
1	1	0	Reserved		
1	1	1	Reserved		

G-Note Montevina
Quanta Computer Inc.

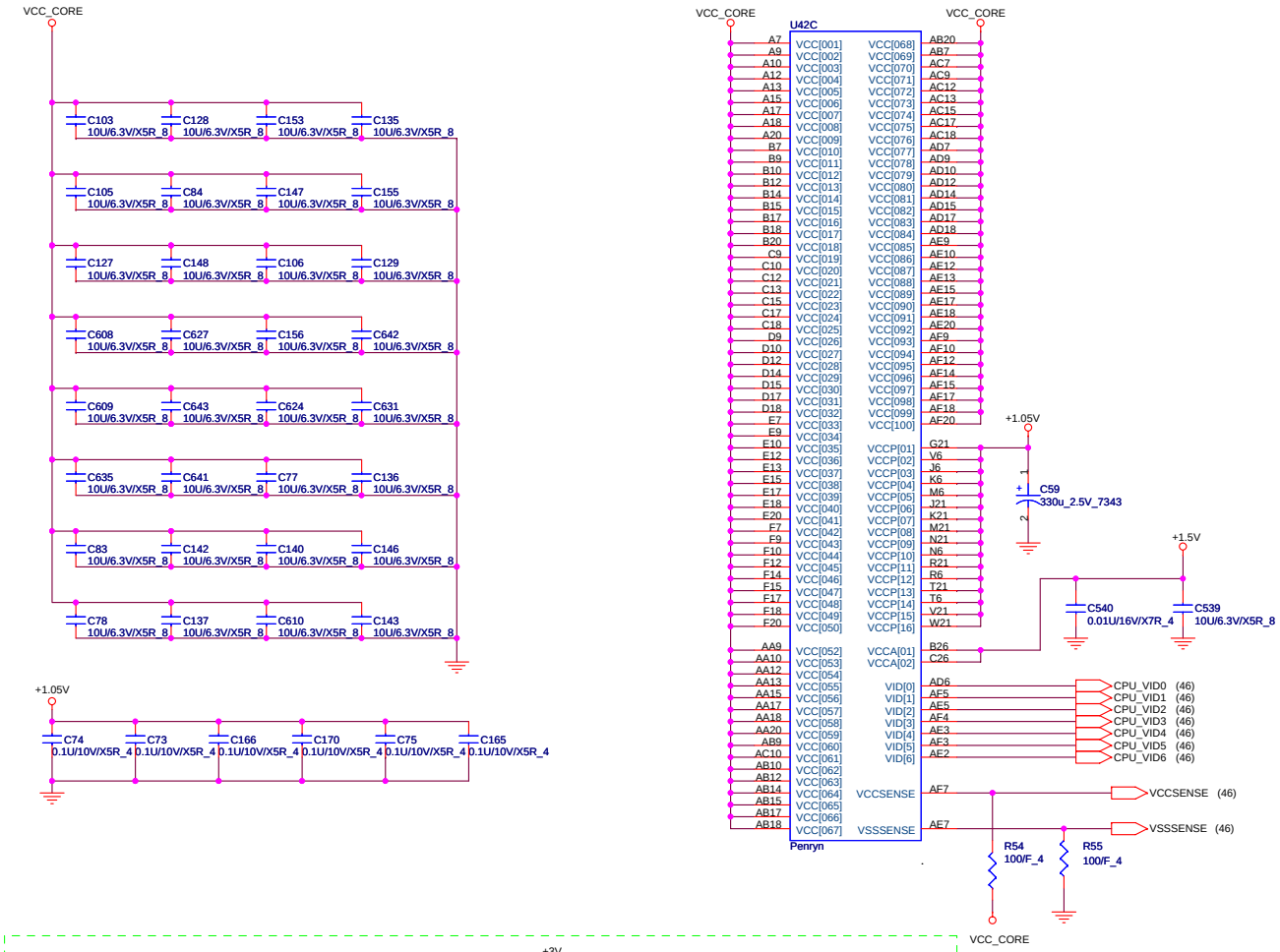
Size	Document Number	Rev
Custom	CLOCK_GEN(SLG8SP568)	2A

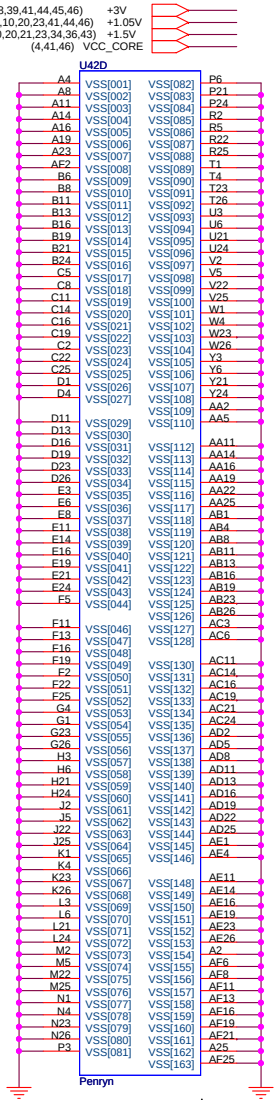
Date: Thursday, April 09, 2009 Sheet 3 of 55

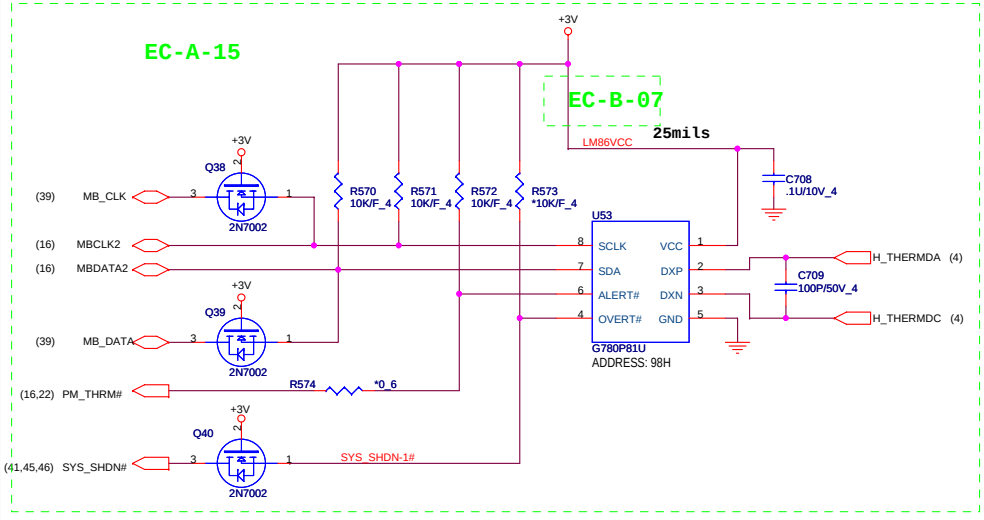


G-Note Montevina
Quanta Computer Inc.

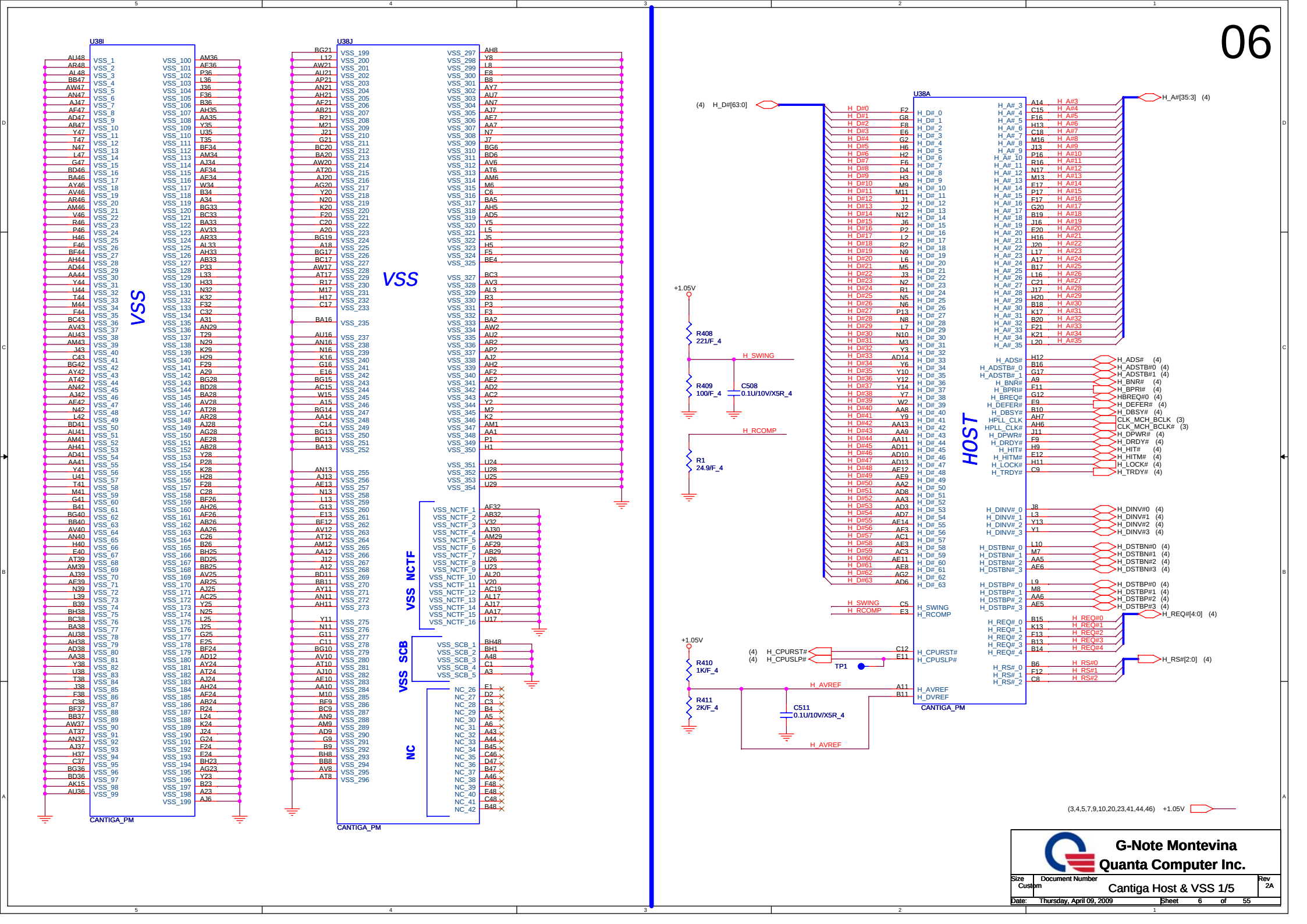
Size	Document Number	Rev
Custom	Penryn 1/2	2A
Date: Thursday, April 09, 2009	Sheet 4 of 55	







G-Note Montevina			
Quanta Computer Inc.			
Size: Custom	Document Number: Penryn & TH Monitor 2/2		Rev: 2A
Date: Thursday, April 09, 2009		Sheet 5 of 55	


06
U38I
VSS
CANTIGA_PM
U38J
VSS
VSS NCTF
VSS SCB
NC
CANTIGA_PM
U38A
HOST
CANTIGA_PM
(4) H_D#[63:0]
H_A#[35:3] (4)
+1.05V
R408 221/F_4
H_SWING
R409 100/F_4
C508 0.1U/10V/X5R_4
H_RCOMP
R1 24.9/F_4
R410 1K/F_4
R411 2K/F_4
(4) H_CPURST#
(4) H_CPUSLP#
TP1
H_AVREF
C511 0.1U/10V/X5R_4
H_ADS# (4)
H_ADSTB#0 (4)
H_ADSTB#1 (4)
H_BNR# (4)
H_BPRI# (4)
HBREQ#0 (4)
H_DEFER# (4)
H_DBSY# (4)
CLK_MCH_BCLK (3)
CLK_MCH_BCLK# (3)
H_DPWR# (4)
H_DRDY# (4)
H_HIT# (4)
H_HITM# (4)
H_LOCK# (4)
H_TRDY# (4)
H_DINV#0 (4)
H_DINV#1 (4)
H_DINV#2 (4)
H_DINV#3 (4)
H_DSTBN#0 (4)
H_DSTBN#1 (4)
H_DSTBN#2 (4)
H_DSTBN#3 (4)
H_DSTBP#0 (4)
H_DSTBP#1 (4)
H_DSTBP#2 (4)
H_DSTBP#3 (4)
H_REQ#[4:0] (4)
H_RS#[2:0] (4)
(3,4,5,7,9,10,20,23,41,44,46) +1.05V
G-Note Montevina
Quanta Computer Inc.
Size Custom
Document Number
Cantiga Host & VSS 1/5
Rev 2A
Date: Thursday, April 09, 2009
Sheet 6 of 55

MCH_CFG_5 DMIx2 selection

Low: DMIx2
High: DMIx4 (Default)

MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)

MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reversed

MCH_CFG_6 iTPM Host Interface

Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)

MCH_CFG_7 Intel (R) Management Engine Crypto

Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

(3,5,10,11,12,14,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,36,37,38,39,41,44,45,46) +3V
(9,10,11,12,41,43,47) 1.5VSUS
(3,4,5,6,9,10,20,23,41,44,46) +1.05V
(3,4,5,6,9,10,20,23,41,44,46) +1.05V_PEG

PEG_TX#[15:0] → PEG_TX#[15:0] (13)
PEG_TX[15:0] → PEG_TX[15:0] (13)
PEG_RX#[15:0] → PEG_RX#[15:0] (13)
PEG_RX[15:0] → PEG_RX[15:0] (13)

U38B — CANTIGA_PM

RSVD: M36 RSVD1, N36 RSVD2, R33 RSVD3, T33 RSVD4, AH9 RSVD5, AH10 RSVD6, AH12 RSVD7, AH13 RSVD8, K12 RSVD9, T24 RSVD14, B31 RSVD15, E32 RSVD16, M1 RSVD17, AY21 RSVD20, BG23 RSVD22, BF23 RSVD23, BH18 RSVD24, BF18 RSVD25

ME JTAG: TP32 AL34 ME_JTAG_TCK, TP27 AK34 ME_JTAG_TDI, TP26 AN35 ME_JTAG_TDO, TP19 AM35 ME_JTAG_TMS

CFG: (3,4) MCH_BSEL0 → T25 CFG_0; (3,4) MCH_BSEL1 → R25 CFG_1; (3,4) MCH_BSEL2 → P25 CFG_2
TP3 MCH_CFG_3 P20 CFG_3; R420 *2.2K_4@NC MCH_CFG_4 P24 CFG_4; R19 *2.2K_4@NC MCH_CFG_5 C25 CFG_5; R17 *2.2K_4@NC MCH_CFG_6 N24 CFG_6; MCH_CFG_7 M24 CFG_7
TP5 MCH_CFG_8 F21 CFG_8; R14 *2.2K_4@NC MCH_CFG_9 C23 CFG_9; R18 *2.2K_4@NC MCH_CFG_10 C24 CFG_10
TP7 MCH_CFG_11 N21 CFG_11; R13 *2.2K_4@NC MCH_CFG_12 P21 CFG_12; R12 *2.2K_4@NC MCH_CFG_13 T21 CFG_13
TP4 MCH_CFG_14 R20 CFG_14; TP2 MCH_CFG_15 M20 CFG_15; R15 *2.2K_4@NC MCH_CFG_16 L21 CFG_16
TP6 MCH_CFG_17 H21 CFG_17; TP14 MCH_CFG_18 P23 CFG_18; MCH_CFG_19 R28 CFG_19; R21 *2.2K_4@NC MCH_CFG_20 T28 CFG_20; +3V R20 *2.2K_4@NC

PM: (22) PM_SYNC# → R29 PM_SYNC#; (4,20,46) H_DPRSTP# → B7 PM_DPRSTP#; (11,12) PM_EXTTS#0 → PM_EXTTS#0 N33 PM_EXT_TS#_0; PM_EXTTS#1 → P32 PM_EXT_TS#_1; (22,46) DELAY_VR_PWRGOOD → AT40 PWROK; R5 100/F_4 RST_IN# MCH → AT11 RSTIN#; (21) PLT_RST-R# R11 *0_4@NC → T20; (4,20) PM_THRMTRIP# → R32 DPRSLPVR; (22,46) DPRSLPVR

NC: BG48 NC_1, BF48 NC_2, BD48 NC_3, BC48 NC_4, BH47 NC_5, BC47 NC_6, BE47 NC_7, BH46 NC_8, BF46 NC_9, BG45 NC_10, BH44 NC_11, BH43 NC_12, BH5 NC_13, BH6 NC_14, BC4 NC_15, BH3 NC_16, BF3 NC_17, BH2 NC_18, BG2 NC_19, BE2 NC_20, BG1 NC_21, BF1 NC_22, BD1 NC_23, BC1 NC_24, F1 NC_25, A47 NC_26

DDR CLK/ CONTROL/COMPENSATION:
SA_CK_0 AP24 → M_A_CLK0 (11); SA_CK_1 AT21 → M_A_CLK1 (11); SB_CK_0 AV24 → M_B_CLK0 (12); SB_CK_1 AU20 → M_B_CLK1 (12)
SA_CK#_0 AR24 → M_A_CLK0# (11); SA_CK#_1 AR21 → M_A_CLK1# (11); SB_CK#_0 AU24 → M_B_CLK0# (12); SB_CK#_1 AV20 → M_B_CLK1# (12)
SA_CKE_0 BC28 → M_A_CKE0 (11); SA_CKE_1 AY28 → M_A_CKE1 (11); SB_CKE_0 AY36 → M_B_CKE0 (12); SB_CKE_1 BB36 → M_B_CKE1 (12)
SA_CS#_0 BA17 → M_A_CS#0 (11); SA_CS#_1 AY16 → M_A_CS#1 (11); SB_CS#_0 AV16 → M_B_CS#0 (12); SB_CS#_1 AR13 → M_B_CS#1 (12)
SA_ODT_0 BD17 → M_A_ODT0 (11); SA_ODT_1 AY17 → M_A_ODT1 (11); SB_ODT_0 BF15 → M_B_ODT0 (12); SB_ODT_1 AV13 → M_B_ODT1 (12)
SM_RCOMP BG22 SM_RCOMP R421 80.6/F_4; SM_RCOMP# BH21 SM_RCOMP# R419 80.6/F_4
SM_RCOMP_VOH BF28 SM_RCOMP_VOH; SM_RCOMP_VOL BH28 SM_RCOMP_VOL
SM_VREF AV42 SMVREF_MCH; SM_PWROK AR36 SM_PWROK; SM_REXT BF17 SM_REXT R10 499/F_4; SM_DRAMRST# BC36 → DDR3_DRAMRST# (11,12)
1.5VSUS → R27 15K/F_4; R28 18.7K/F_4; DDR3_PWG (43)

CLK:
DPLL_REF_CLK B38 DREFCLK; DPLL_REF_CLK# A38 DREFCLK#; DPLL_REF_SSCLK E41 DREFSSCLK; DPLL_REF_SSCLK# F41 DREFSSCLK#
PEG_CLK F43 → CLK_PCIE_3GPLL (3); PEG_CLK# E43 → CLK_PCIE_3GPLL# (3)

DMI:
DMI_RXN_0 AE41 DMI_TXN0; DMI_RXN_1 AE37 DMI_TXN1; DMI_RXN_2 AE47 DMI_TXN2; DMI_RXN_3 AH39 DMI_TXN3 → DMI_TXN[3:0] (21)
DMI_RXP_0 AE40 DMI_TXP0; DMI_RXP_1 AE38 DMI_TXP1; DMI_RXP_2 AE48 DMI_TXP2; DMI_RXP_3 AH40 DMI_TXP3 → DMI_TXP[3:0] (21)
DMI_TXN_0 AE35 DMI_RXN0; DMI_TXN_1 AE43 DMI_RXN1; DMI_TXN_2 AE46 DMI_RXN2; DMI_TXN_3 AH42 DMI_RXN3 → DMI_RXN[3:0] (21)
DMI_TXP_0 AD35 DMI_RXP0; DMI_TXP_1 AE44 DMI_RXP1; DMI_TXP_2 AE46 DMI_RXP2; DMI_TXP_3 AH43 DMI_RXP3 → DMI_RXP[3:0] (21)

GRAPHICS VID:
GFX_VID_0 B33 GFXVR_VID_0 → TP109; GFX_VID_1 B32 GFXVR_VID_1 → TP107; GFX_VID_2 G33 GFXVR_VID_2 → TP25; GFX_VID_3 F33 GFXVR_VID_3 → TP28; GFX_VID_4 E33 GFXVR_VID_4 → TP24
GFX_VR_EN C34 GFXVR_EN → TP110

ME:
CL_CLK AH37 CL_CLK0 (22); CL_DATA AH36 CL_DATA0 (22); CL_PWROK AN36 ECPWROK (22,39); CL_RST# AJ35 CL_RST#0 (22); CL_VREF AH34 MCH_CLVREF
0.35 V; +1.05V → R41 1K/F_4; R40 499/F_4; C70 0.1U/10V/X5R_4

MISC:
DDPC_CTRLCLK N28 DDPC_CTRLCLK → TP9; DDPC_CTRLDATA M28 DDPC_CTRLDATA → TP13
SDVO_CTRLCLK G38 R30 4.7K_4@NC; SDVO_CTRLDATA E36 R29 4.7K_4@NC → +3V
CLKREQ# K36 → CLK_MCH_OE# (3); ICH_SYNC# H36 → MCH_ICH_SYNC# (22)
TSATN# B12 MCH_TSATN R4 56.2/F_4 → +1.05V

HDA:
HDA_BCLK B28 → TP104; HDA_RST# B30 → TP108; HDA_SDI B29 → TP105; HDA_SDO C29 → TP106; HDA_SYNC A28 → TP103

U38C — CANTIGA_PM

LVDS:
TP20 INT_DPST_PWM L32 L_BKLT_CTRL; TP23 INT_LVDS_BLON C32 L_BKLT_EN; TP21 L_CTRL_CLK M32 L_CTRL_CLK
TP29 L_CTRL_DATA M33 L_CTRL_DATA; TP30 INT_EDIDCLK K33 L_DDC_CLK; TP22 INT_EDIDDATA J33 L_DDC_DATA
TP12 INT_DISP_ON M29 L_VDD_EN; TP122 LVDS_IBG C44 LVDS_IBG; TP121 LVDS_VBG B43 LVDS_VBG; E37 LVDS_VREFH; E38 LVDS_VREFL
TP117 LA_CLK# C41 LVDSA_CLK#; TP119 LA_CLK C40 LVDSA_CLK; TP113 LB_CLK# B37 LVDSB_CLK#; TP112 LB_CLK A37 LVDSB_CLK
TP123 LA_DATAN0 H47 LVDSA_DATA#_0; TP42 LA_DATAN1 E46 LVDSA_DATA#_1; TP41 LA_DATAN2 G40 LVDSA_DATA#_2; TP115 LA_DATAN3 A40 LVDSA_DATA#_3
TP124 LA_DATAP0 H48 LVDSA_DATA_0; TP43 LA_DATAP1 D45 LVDSA_DATA_1; TP40 LA_DATAP2 F40 LVDSA_DATA_2; TP116 LA_DATAP3 B40 LVDSA_DATA_3
TP118 LB_DATAN0 A41 LVDSB_DATA#_0; TP34 LB_DATAN1 H38 LVDSB_DATA#_1; TP39 LB_DATAN2 G37 LVDSB_DATA#_2; TP31 LB_DATAN3 J37 LVDSB_DATA#_3
TP120 LB_DATAP0 B42 LVDSB_DATA_0; TP38 LB_DATAP1 G38 LVDSB_DATA_1; TP37 LB_DATAP2 F37 LVDSB_DATA_2; TP33 LB_DATAP3 K37 LVDSB_DATA_3

TV:
TV_COMP1 F25 TVA_DAC; TV_Y/G1 H25 TVB_DAC; TV_C/R1 K25 TVC_DAC
H24 TV_RTN
TP16 TV_DCONSEL0 C31 TV_DCONSEL_0; TP17 TV_DCONSEL1 E32 TV_DCONSEL_1

VGA:
INT_CRT_BLU E28 CRT_BLUE; INT_CRT_GRN G28 CRT_GREEN; INT_CRT_RED J28 CRT_RED; G29 CRT_IRTN
TP18 CRT_DDC_CLK H32; TP15 HSYNC_INT J29 CRT_HSYNC; TP10 CRTIREF E29 CRT_TVO_IREF; TP11 VSYNC_INT L29 CRT_VSYNC

PCI-EXPRESS GRAPHICS:
PEG_COMPI T37 PEG_COMP R25 49.9/F_4; PEG_COMPO T36; +1.05V_PEG
PEG_RX#_0 H44 PEG_RX#0; PEG_RX#_1 J46 PEG_RX#1; PEG_RX#_2 L44 PEG_RX#2; PEG_RX#_3 L40 PEG_RX#3; PEG_RX#_4 N41 PEG_RX#4; PEG_RX#_5 P48 PEG_RX#5; PEG_RX#_6 N44 PEG_RX#6; PEG_RX#_7 T43 PEG_RX#7; PEG_RX#_8 U43 PEG_RX#8; PEG_RX#_9 Y43 PEG_RX#9; PEG_RX#_10 Y48 PEG_RX#10; PEG_RX#_11 Y36 PEG_RX#11; PEG_RX#_12 AA43 PEG_RX#12; PEG_RX#_13 AD37 PEG_RX#13; PEG_RX#_14 AC47 PEG_RX#14; PEG_RX#_15 AD39 PEG_RX#15
PEG_RX_0 H43 PEG_RX0; PEG_RX_1 J44 PEG_RX1; PEG_RX_2 L43 PEG_RX2; PEG_RX_3 L41 PEG_RX3; PEG_RX_4 N40 PEG_RX4; PEG_RX_5 P47 PEG_RX5; PEG_RX_6 N43 PEG_RX6; PEG_RX_7 T42 PEG_RX7; PEG_RX_8 U42 PEG_RX8; PEG_RX_9 Y42 PEG_RX9; PEG_RX_10 W47 PEG_RX10; PEG_RX_11 Y37 PEG_RX11; PEG_RX_12 AA42 PEG_RX12; PEG_RX_13 AD36 PEG_RX13; PEG_RX_14 AC48 PEG_RX14; PEG_RX_15 AD40 PEG_RX15
PEG_TX#_0 J41 C_PEG_TX#0 C561 0.1U/10V/X5R_4 PEG_TX#0; PEG_TX#_1 M46 C_PEG_TX#1 C586 0.1U/10V/X5R_4 PEG_TX#1; PEG_TX#_2 M47 C_PEG_TX#2 C563 0.1U/10V/X5R_4 PEG_TX#2; PEG_TX#_3 M40 C_PEG_TX#3 C596 0.1U/10V/X5R_4 PEG_TX#3; PEG_TX#_4 M42 C_PEG_TX#4 C565 0.1U/10V/X5R_4 PEG_TX#4; PEG_TX#_5 R48 C_PEG_TX#5 C588 0.1U/10V/X5R_4 PEG_TX#5; PEG_TX#_6 N38 C_PEG_TX#6 C567 0.1U/10V/X5R_4 PEG_TX#6; PEG_TX#_7 T40 C_PEG_TX#7 C598 0.1U/10V/X5R_4 PEG_TX#7; PEG_TX#_8 U37 C_PEG_TX#8 C569 0.1U/10V/X5R_4 PEG_TX#8; PEG_TX#_9 U40 C_PEG_TX#9 C600 0.1U/10V/X5R_4 PEG_TX#9; PEG_TX#_10 Y40 C_PEG_TX#10 C571 0.1U/10V/X5R_4 PEG_TX#10; PEG_TX#_11 AA46 C_PEG_TX#11 C590 0.1U/10V/X5R_4 PEG_TX#11; PEG_TX#_12 AA37 C_PEG_TX#12 C592 0.1U/10V/X5R_4 PEG_TX#12; PEG_TX#_13 AA40 C_PEG_TX#13 C558 0.1U/10V/X5R_4 PEG_TX#13; PEG_TX#_14 AD43 C_PEG_TX#14 C594 0.1U/10V/X5R_4 PEG_TX#14; PEG_TX#_15 AC46 C_PEG_TX#15 C556 0.1U/10V/X5R_4 PEG_TX#15
PEG_TX_0 J42 C_PEG_TX0 C560 0.1U/10V/X5R_4 PEG_TX0; PEG_TX_1 L46 C_PEG_TX1 C585 0.1U/10V/X5R_4 PEG_TX1; PEG_TX_2 M48 C_PEG_TX2 C562 0.1U/10V/X5R_4 PEG_TX2; PEG_TX_3 M39 C_PEG_TX3 C595 0.1U/10V/X5R_4 PEG_TX3; PEG_TX_4 M43 C_PEG_TX4 C564 0.1U/10V/X5R_4 PEG_TX4; PEG_TX_5 R47 C_PEG_TX5 C587 0.1U/10V/X5R_4 PEG_TX5; PEG_TX_6 N37 C_PEG_TX6 C566 0.1U/10V/X5R_4 PEG_TX6; PEG_TX_7 T39 C_PEG_TX7 C597 0.1U/10V/X5R_4 PEG_TX7; PEG_TX_8 U36 C_PEG_TX8 C568 0.1U/10V/X5R_4 PEG_TX8; PEG_TX_9 U39 C_PEG_TX9 C599 0.1U/10V/X5R_4 PEG_TX9; PEG_TX_10 Y39 C_PEG_TX10 C570 0.1U/10V/X5R_4 PEG_TX10; PEG_TX_11 Y46 C_PEG_TX11 C589 0.1U/10V/X5R_4 PEG_TX11; PEG_TX_12 AA36 C_PEG_TX12 C591 0.1U/10V/X5R_4 PEG_TX12; PEG_TX_13 AA39 C_PEG_TX13 C582 0.1U/10V/X5R_4 PEG_TX13; PEG_TX_14 AD42 C_PEG_TX14 C593 0.1U/10V/X5R_4 PEG_TX14; PEG_TX_15 AD46 C_PEG_TX15 C581 0.1U/10V/X5R_4 PEG_TX15

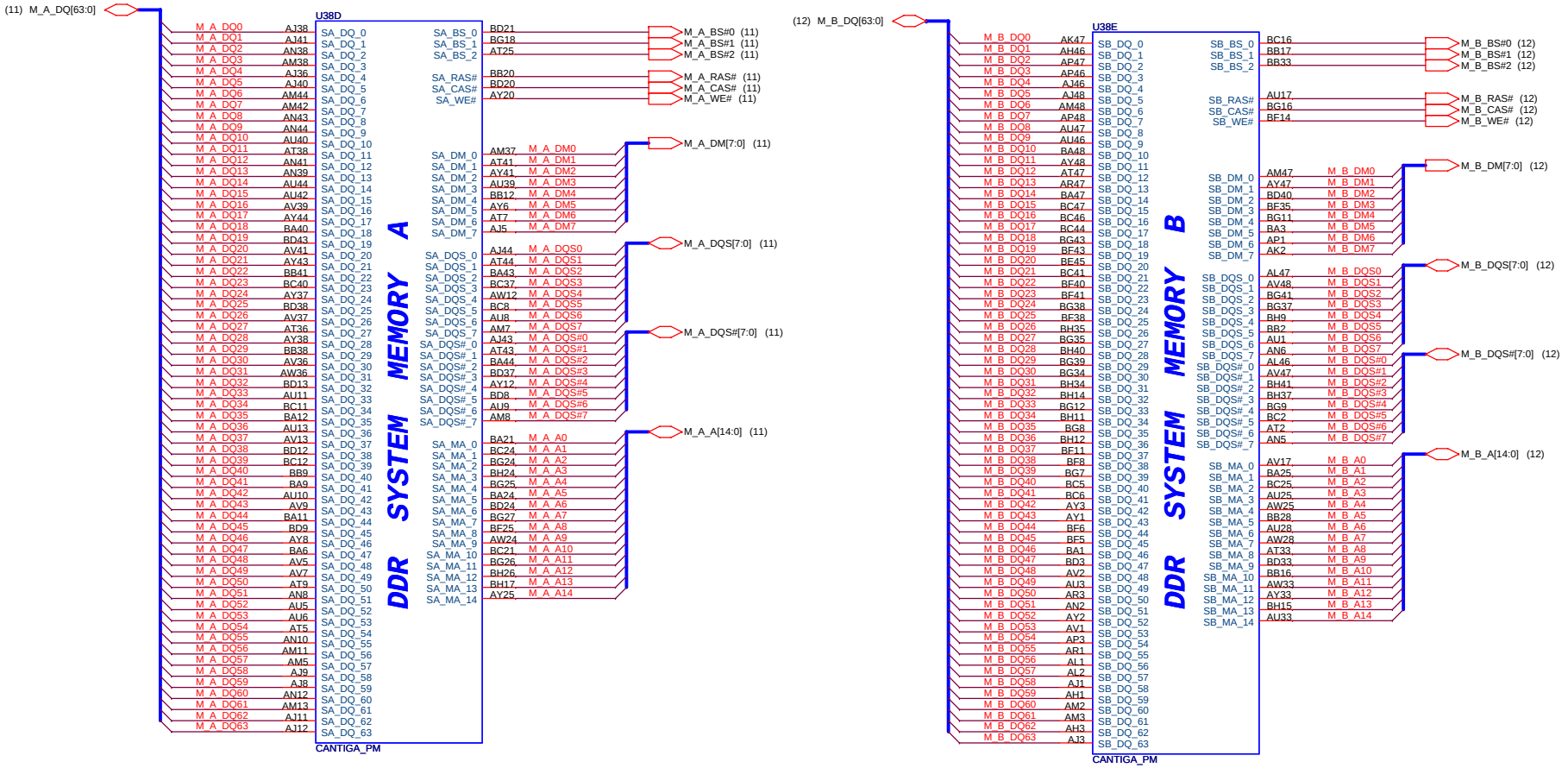
1.5VSUS → R422 1K/F_4; SM_RCOMP_VOH → C529 0.01U/16V/X7R_4, C528 2.2U/6.3V/X5R_6 → R424 3.01K/F_4
SM_RCOMP_VOL → C525 0.01U/16V/X7R_4, C524 2.2U/6.3V/X5R_6 → R423 1K/F_4

1.5VSUS → R35 1K/F_4@NC; SMVREF_MCH → C67 0.1U/10V/X5R_4, C66 470P/50V/X7R_4 → R34 *1K/F_4@NC
EC-B-07
SMDDR_VREF (11,12,43)

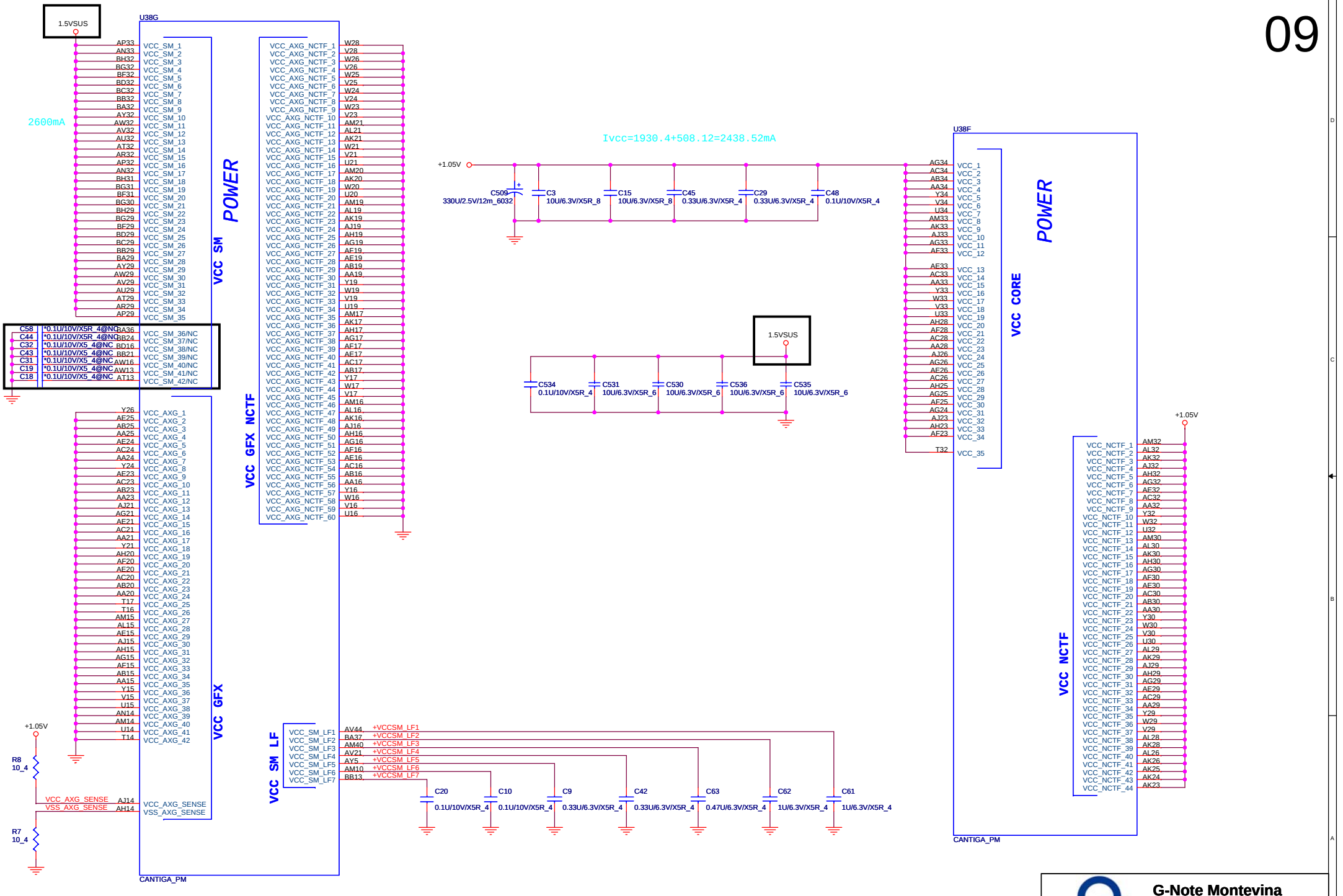
G-Note Montevina
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga DMI/DISP 2/5	2A

Date: Thursday, April 09, 2009 Sheet 7 of 55



G-Note Montevina Quanta Computer Inc.			
Size: Custom	Document Number: Cantiga DDR3 3/5		Rev: 2A
Date: Thursday, April 09, 2009	Sheet 8 of 55		



G-Note Montevina Quanta Computer Inc.			
Size: Custom	Document Number: Cantiga Vcc 4/5		Rev: 2A
Date: Thursday, April 09, 2009	Sheet 9 of 55		

+1.05V (3,4,5,6,7,9,20,23,41,44,46)
+3V (3,5,7,11,12,14,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,36,37,38,39,41,44,45,46)
+1.5V (5,20,21,23,34,36,43)
+1.05V_PEG (3,4,5,6,7,9,20,23,41,44,46)

U38H

POWER

CRT: VCCA_CRT_DAC_1 (B27), VCCA_CRT_DAC_2 (A26), VCCA_DAC_BG (A25), VSSA_DAC_BG (B25)

PLL: VCCA_DPLLA (F47, +1.05V_DPLLA), VCCA_DPLLB (L48, +1.05V_DPLLB, 24mA), VCCA_HPLL (AD1, +1.05V_HPLL, 139.2mA), VCCA_MPLL (AE1, +1.05V_MPLL)

LVDS: VCCA_LVDS (J48), VSSA_LVDS (J47)

A PEG: VCCA_PEG_BG (AD48, +1.5V_PEG_BG, 414uA, EC-B-07, +1.5V, C572 0.1U/10V/X5R_4, 50mA), VCCA_PEG_PLL (AA48, C55 0.1U/10V/X5R_4, +1.05V_PEGPLL, 747.5mA)

A SM: VCCA_SM_1 (AR20, +1.05V_A_SM), VCCA_SM_2 (AP20), VCCA_SM_3 (AN20), VCCA_SM_4 (AR17), VCCA_SM_5 (AP17), VCCA_SM_6 (AN17), VCCA_SM_7 (AT16), VCCA_SM_8 (AR16), VCCA_SM_9 (AP16)

A CK: VCCA_SM_CK_1 (AP28, +1.05V_A_SM_CK, 37.95mA), VCCA_SM_CK_2 (AN28), VCCA_SM_CK_3 (AP25), VCCA_SM_CK_4 (AN25), VCCA_SM_CK_5 (AN24), VCCA_SM_CK_NCTF_1 (AM28), VCCA_SM_CK_NCTF_2 (AM26), VCCA_SM_CK_NCTF_3 (AM25), VCCA_SM_CK_NCTF_4 (AL25), VCCA_SM_CK_NCTF_5 (AM24), VCCA_SM_CK_NCTF_6 (AL24), VCCA_SM_CK_NCTF_7 (AM23), VCCA_SM_CK_NCTF_8 (AL23)

TV: VCCA_TV_DAC_1 (B24), VCCA_TV_DAC_2 (A24)

HDA: VCC_HDA (A32, 35mA)

D TV/CRT: VCCD_TVDAC (M25, 120uA), VCCD_QDAC (L28, +1.5V_QDAC, 157.2mA), VCCD_HPLL (AF1, +1.05V_MPLL, 50mA), VCCD_PEG_PLL (AA47, +1.05V_PEGPLL, 60.31mA)

LVDS: VCCD_LVDS_1 (M38), VCCD_LVDS_2 (L37)

VTT: VTT_1 (U13) … VTT_25 (U1), 852mA, +1.05V, C21 0.47U/6.3V/X5R_4, C17 2.2U/6.3V/X5R_6, C46 4.7U/6.3V/X5R_6, C13 4.7U/6.3V/X5R_6

AXF: VCC_AXF_1 (B22), VCC_AXF_2 (B21), VCC_AXF_3 (A21), 150mA

SM CK: VCC_SM_CK_1 (BF21), VCC_SM_CK_2 (BH20), VCC_SM_CK_3 (BG20), VCC_SM_CK_4 (BF20)

HV: VCC_TX_LVDS (K47, 118.8mA), VCC_HV_1 (C35), VCC_HV_2 (B35), VCC_HV_3 (A35, +3V_HV, 105.3mA), C537 0.1U/10V/X5R_4

PEG: VCC_PEG_1 (V48), VCC_PEG_2 (U48), VCC_PEG_3 (V47), VCC_PEG_4 (U47), VCC_PEG_5 (U46), 1782mA, +1.05V_PEG, +1.05V

DMI: VCC_DMI_1 (AH48), VCC_DMI_2 (AF48), VCC_DMI_3 (AH47), VCC_DMI_4 (AG47), +1.05V_RXR_DMI, C54 4.7U/6.3V/X5R_6, C60 *330u/2.5V_7343@NC, C56 10U/6.3V/X5R_8

VTTLF: VTTLF1 (A8), VTTLF2 (L1), VTTLF3 (AB2), +VTTLF_CAP1, +VTTLF_CAP2, +VTTLF_CAP3, 456mA, +1.05V, EC-B-07, C557 0.1U/10V/X5R_4

CANTIGA_PM

+1.05V_AXF, EC-B-07, +1.05V, C515 1U/6.3V/X5R_4, C514 10U/6.3V/X5R_8

+1.5VSUS_SM_CK, L54 1uH/230mA_6, 1.5VSUS, C519 10U/6.3V/X5R_6, C522 0.1U/10V/X5R_4, R416 1/F_6, +1.5VSUS_SM_CK_L, C520 10U/6.3V/X5R_6

+1.05V, D13 RB501V-40, +1.05V_HV_MCH, R412 10_4, +3V_HV, +3V, EC-B-07, C538 0.1U/10V/X5R_4

+1.05V, EC-B-07, +1.05V_HPLL, C4 4.7U/6.3V/X5R_6, C1 0.1U/10V/X5R_4, +1.05V_MPLL, L1 HCB1608KF-181T15_6, +1.05V_MCH_PLL, R2 0.5/F_6, C11 10U/6.3V/X5R_8, C8 0.1U/10V/X5R_4

+1.5V, EC-B-07, +1.5V_QDAC, C47 0.1U/10V/X5R_4, C49 0.01U/16V/X7R_4

+1.05V, EC-B-07, C23 10U/6.3V/X5R_8, C37 10U/6.3V/X5R_8, C5 *220U/2.5V_3528@NC, C36 10U/6.3V/X5R_8, C41 4.7U/6.3V/X5R_6, C30 1U/6.3V/X5R_4

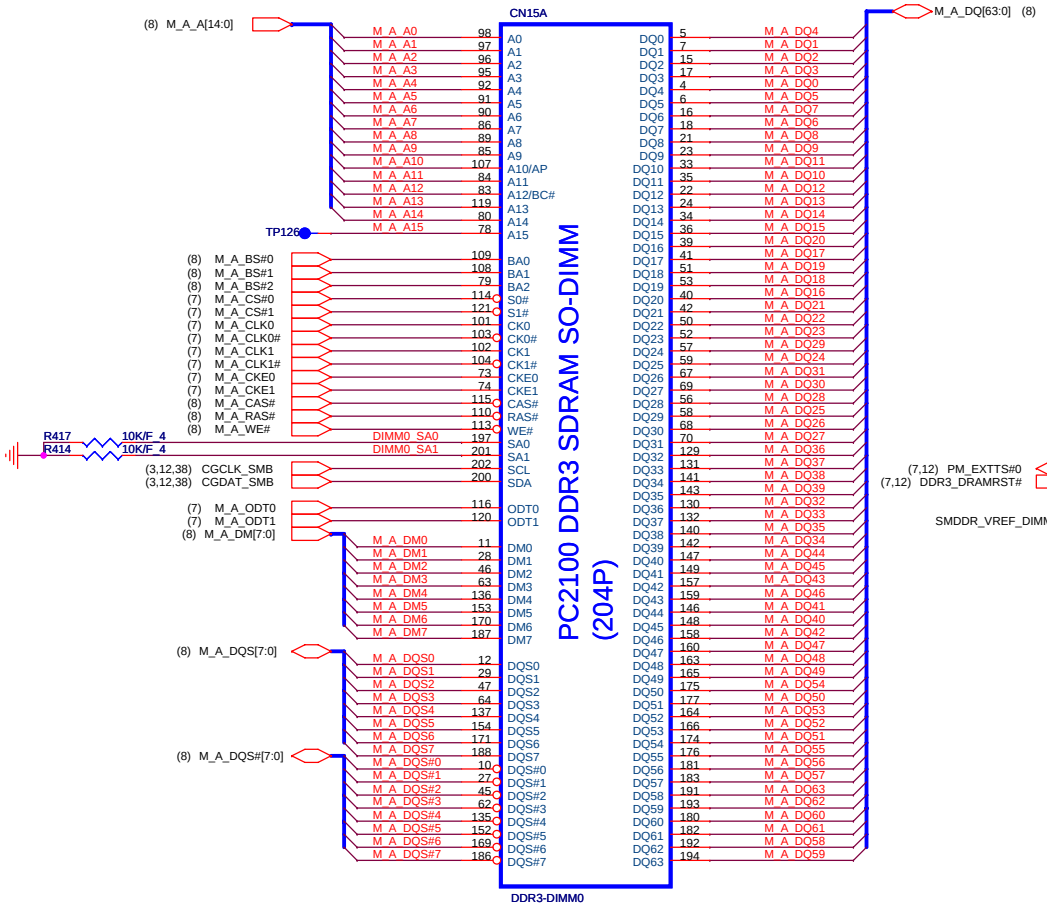
+1.05V, EC-B-07, +1.05V_A_SM_CK, C50 2.2U/6.3V/X5R_6, C52 10U/6.3V/X5R_8, C53 0.1U/10V/X5R_4

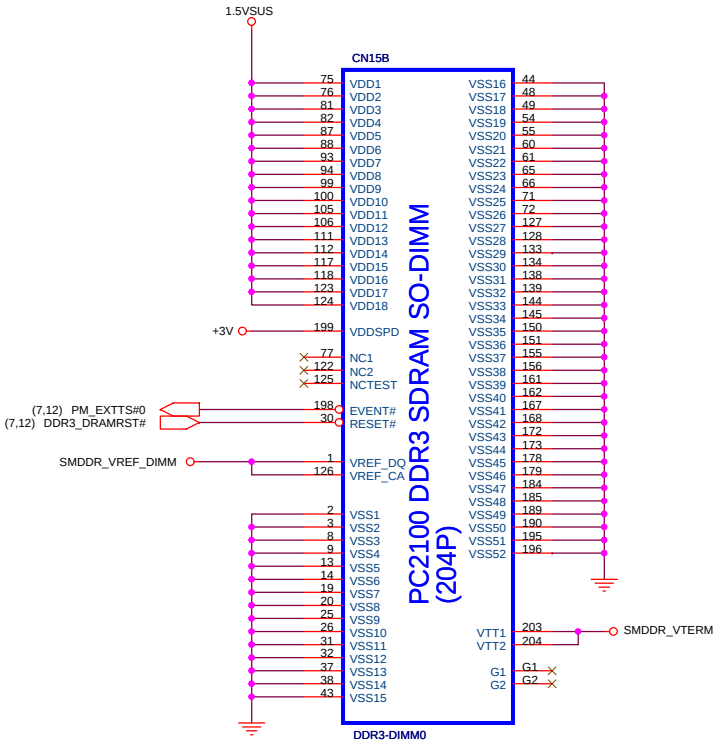
+1.05V, L3 HCB1608KF-181T15_6, +1.05V_PEGPLL, R23 1/F_6, C51 10U/6.3V/X5R_8

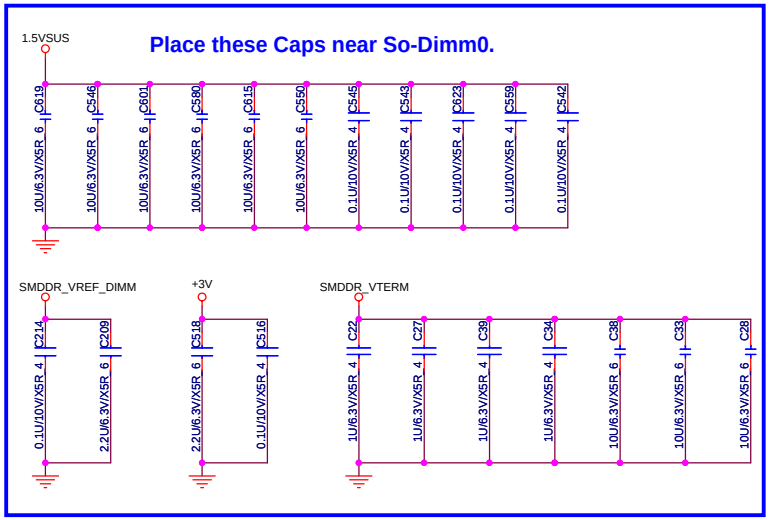
C7 0.1U/10V/X5R_4, C57 0.1U/10V/X5R_4

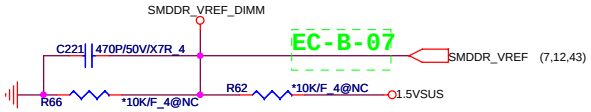
+VTTLF_CAP1, +VTTLF_CAP2, +VTTLF_CAP3, C2 0.47U/6.3V/X5R_4, C6 0.47U/6.3V/X5R_4, C510 0.47U/6.3V/X5R_4

G-Note Montevina Quanta Computer Inc.		
Size: Custom	Document Number: Cantiga Power 5/5	Rev: 2A
Date: Thursday, April 09, 2009	Sheet 10 of 55	

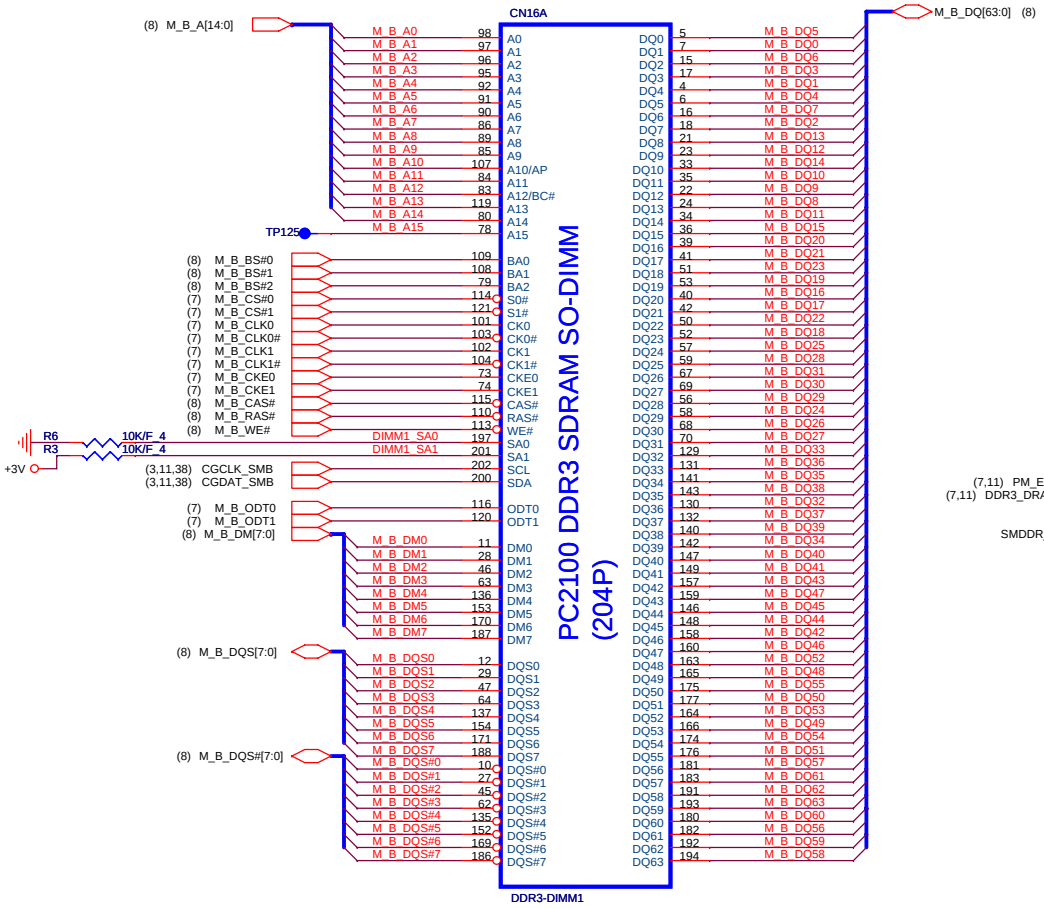


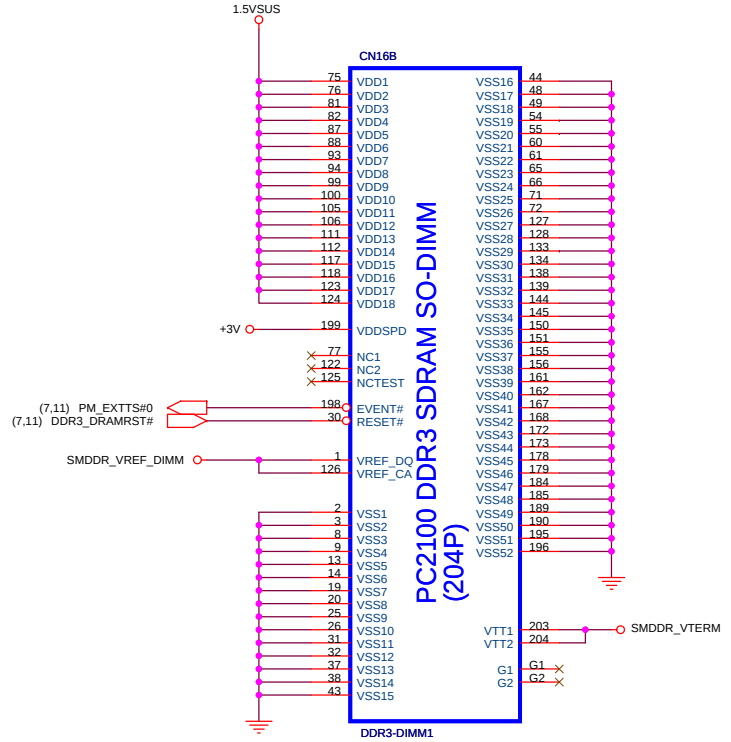


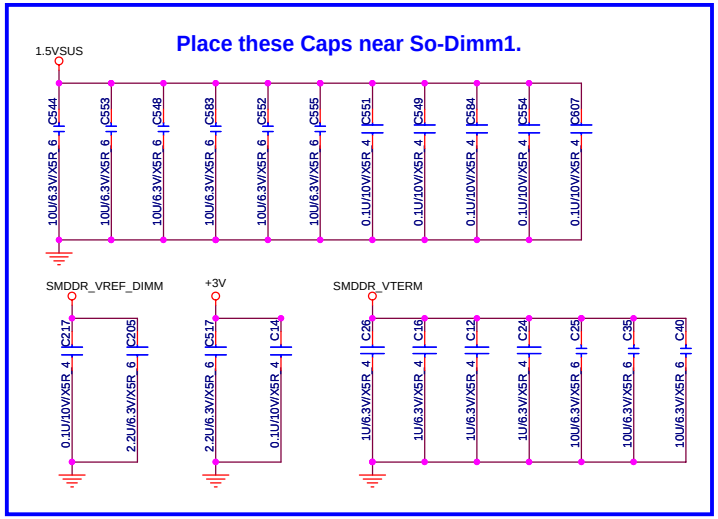




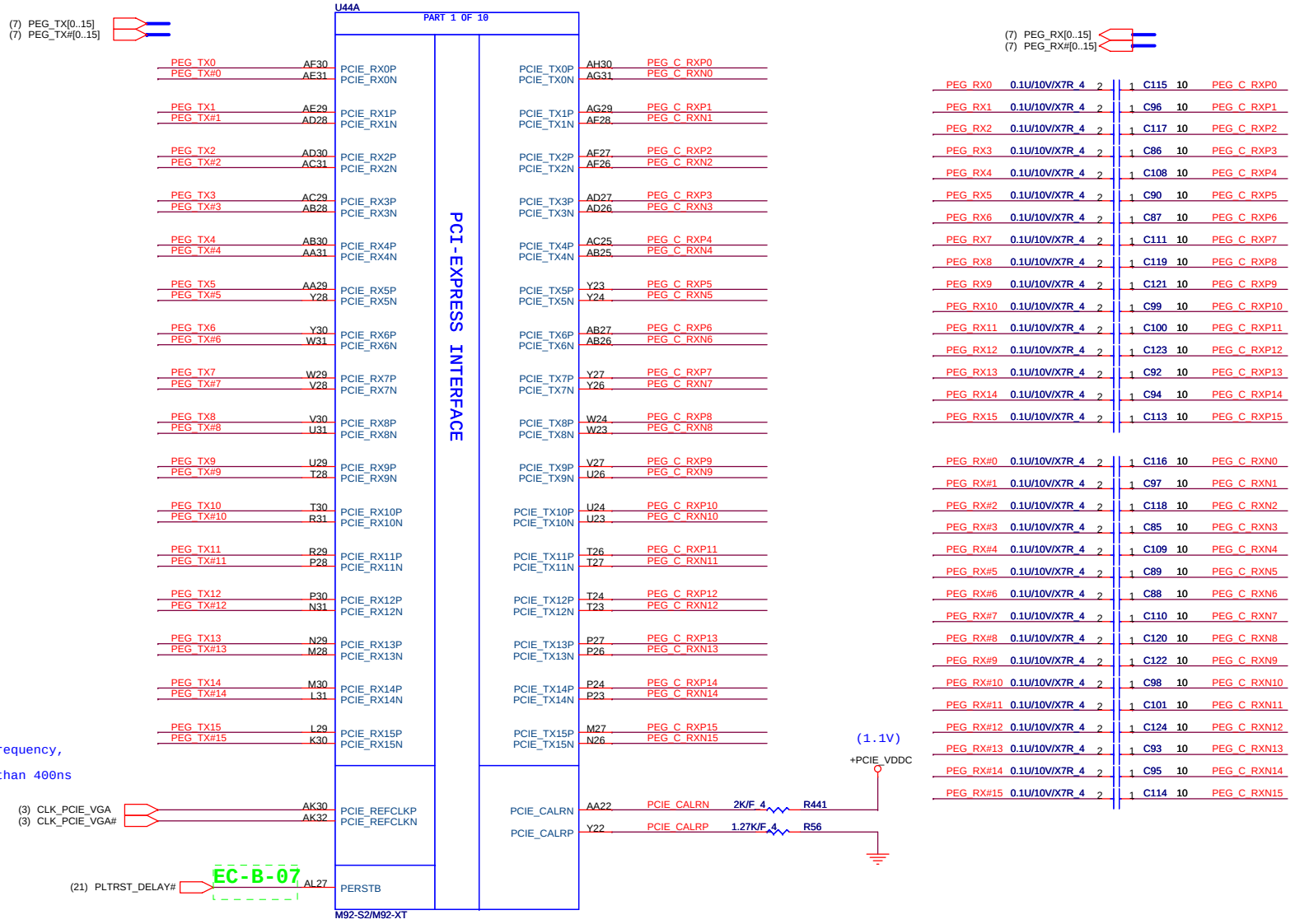
G-Note Montevina Quanta Computer Inc.		
Size: Custom	Document Number: DDR3 DIMM-0(H=5.2)	Rev: 2A
Date: Thursday, April 09, 2009	Sheet 11 of 55	







G-Note Montevina Quanta Computer Inc.		
Size: Custom	Document Number: DDR3 DIMM-1(H=9.2)	Rev: 2A
Date: Thursday, April 09, 2009	Sheet 12 of 55	



G-Note Montevina
Quanta Computer Inc.

Size	Document Number	Rev
A3	M92-XT_PCIE	2A
Date: Thursday, April 09, 2009	Sheet 13 of 55	

MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

Remove 512MB

Change to 256MB

Memory Straps	RAM_TYPE_CFG3_R	RAM_TYPE_CFG2_R	RAM_TYPE_CFG1_R	RAM_TYPE_CFG0_R
900MHz 128MB(32M*32) Hynix H5RS1H23MFR-11C	0	0	0	0
900MHz 128MB(32M*32) Qimonda HYB18H1G321AF-11	0	0	0	1
900MHz 128MB(32M*32) Qimonda HYB18H1G321A2F-11	0	0	1	1
800MHz 128MB(32M*32) Samsung K4J10324QD-HC12	0	1	0	0

GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	G NOTE Setting
GPIO0	GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable) 0 : Default, (Driver Controlled Gen2) 1 : Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO_5_AC_BATT 0 : Battery saving mode = 0.0 V 1 : AC (Performance mode) = 3.3 V	1
GPIO6	ATI Internal use only	0
GPIO8	ATI reserved configuration straps.	0
GPIO9	VGA Disable 0 - VGA Controller capacity enabled 1 - The device will not recognized as the system's VGA controller	0
GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
HSYNC VSYNC	AUD[1:0] 00 - No audio function 01 - Audio for DisplayPort and HDMI if adapter is detectd 10 - Audio for DisplayPort only 11 - Audio for both DisplayPort and HDMI	1 1

DIS only

Layout Note:
Place 150 ohm termination resistors close to ATI CHIP.

A2VSSQ connect to GND by a via directly

A2VSSQ connect to GND by a via directly

Spread Spectrum

If U4, the discrete spread spectrum chip is not used, then pop R48 in order to pull-down XTALOUT for EMI reasons.

	S0
-1.75% (DOWN)	0

G-Note Montevina	
Quanta Computer Inc.	
Size: Custom	Document Number: M92-XT_IO
Rev: 2A	
Date: Thursday, April 09, 2009	Sheet 14 of 55

layout note: close to VDDR1#[1:17]

+1.8V

C197 0.01U/25V/X7R_4 C638 0.01U/25V/X7R_4 C179 0.01U/25V/X7R_4 C161 0.01U/25V/X7R_4 C287 0.01U/25V/X7R_4 C229 0.1U/10V/X7R_4 C284 0.1U/10V/X7R_4 C213 0.1U/10V/X7R_4 C296 0.1U/10V/X7R_4

C228 1U/6.3V/X5R_4 C644 1U/6.3V/X5R_4 C295 1U/6.3V/X5R_4 C212 1U/6.3V/X5R_4 C230 1U/6.3V/X5R_4 C181 0.1U/10V/X7R_4

(1.1V) +PCIE_VDDC (PCIE_VDDC 1.1V @ 1A)

C605 10U/6.3V/X5R_6 C576 1U/6.3V/X5R_4 C577 0.1U/10V/X7R_4

C604 10U/6.3V/X5R_6 C578 1U/6.3V/X5R_4 C575 0.1U/10V/X7R_4

+1.8V

C251 10U/6.3V/X5R_6 C634 10U/6.3V/X5R_6 C657 10U/6.3V/X5R_6

U44D

PART 4 OF 10

POWER

VDDR1#1 H13
VDDR1#2 H16
VDDR1#3 H19
VDDR1#4 J10
VDDR1#5 J23
VDDR1#6 J24
VDDR1#7 J9
VDDR1#8 K10
VDDR1#9 K23
VDDR1#10 K24
VDDR1#11 K9
VDDR1#12 L11
VDDR1#13 L12
VDDR1#14 L13
VDDR1#15 L20
VDDR1#16 L21
VDDR1#17 L22

PCIE_VDDR#1 AB23
PCIE_VDDR#2 AC23
PCIE_VDDR#3 AD24
PCIE_VDDR#4 AE24
PCIE_VDDR#5 AE25
PCIE_VDDR#6 AE26
PCIE_VDDR#7 AF25
PCIE_VDDR#8 AG26

PCIE_VDDC#1 L23
PCIE_VDDC#2 L24
PCIE_VDDC#3 L25
PCIE_VDDC#4 L26
PCIE_VDDC#5 M22
PCIE_VDDC#6 N22
PCIE_VDDC#7 N23
PCIE_VDDC#8 N24
PCIE_VDDC#9 R22
PCIE_VDDC#10 T22
PCIE_VDDC#11 U22
PCIE_VDDC#12 V22

VDDC#1 AA15
VDDC#2 M11
VDDC#3 M12
VDDC#4 N15
VDDC#5 N17
VDDC#6 R13
VDDC#7 R16
VDDC#8 R18
VDDC#9 R21
VDDC#10 T12
VDDC#11 T15
VDDC#12 T17
VDDC#13 T20
VDDC#14 U13
VDDC#15 U16
VDDC#16 U18
VDDC#17 U21
VDDC#18 V15
VDDC#19 V17
VDDC#20 V20
VDDC#21 V21
VDDC#22 Y13
VDDC#23 Y16
VDDC#24 Y18
VDDC#25 Y21

VDDCI#1 M13
VDDCI#2 M15
VDDCI#3 M16
VDDCI#4 M17
VDDCI#5 M18
VDDCI#6 M20
VDDCI#7 M21
VDDCI#8 N20

VDD_CT#1 AA20
VDD_CT#2 AA21
VDD_CT#3 AB20
VDD_CT#4 AB21

VDDR3#1 AA17
VDDR3#2 AA18
VDDR3#3 AB17
VDDR3#4 AB18

VDDR4#1 AA11
VDDR4#2 AA12
VDDR4#3 Y11
VDDR4#4 Y12

VDDR5#1 U11
VDDR5#2 U12
VDDR5#3 V11
VDDR5#4 V12

VDDRHA L17
VSSRHA L16

M92-S2/M92-XT

+1.8V

C297 1U/6.3V/X5R_4 C190 0.1U/10V/X7R_4 C294 1U/6.3V/X5R_4 C167 0.01U/25V/X7R_4 C247 10U/6.3V/X5R_6

(1.1V) +PCIE_VDDC

C579 1U/6.3V/X5R_4 C611 1U/6.3V/X5R_4 C612 1U/6.3V/X5R_4 C154 1U/6.3V/X5R_4 C614 1U/6.3V/X5R_4 C613 1U/6.3V/X5R_4 C157 1U/6.3V/X5R_4 C606 10U/6.3V/X5R_6

+1.8V

L57 BLM15BD121SN1D

+VDD_CT

C602 10U/6.3V/X5R_6 C158 0.1U/10V/X7R_4 C180 1U/6.3V/X5R_4 C164 1U/6.3V/X5R_4 C162 0.1U/10V/X7R_4

+3.3V_DELAY

C183 1U/6.3V/X5R_4 C160 1U/6.3V/X5R_4 C168 0.1U/10V/X7R_4 C184 0.1U/10V/X7R_4

+1.8V

C652 1U/6.3V/X5R_4 C649 0.1U/10V/X7R_4 C245 1U/6.3V/X5R_4 C290 0.1U/10V/X7R_4

+1.8V

L55 BLM15BD121SN1D

+VDDRH1

C574 1U/6.3V/X5R_4 C573 1U/6.3V/X5R_4

(0.9~1.2V) +VCC_GFX_CORE

C211 0.1U/10V/X7R_4 C273 1U/6.3V/X5R_4

+BBP

(0.9~1.2V) +VDDCI

U44E

PART 5 OF 10

GND

PCIE_VSS#1 AA27
PCIE_VSS#2 AB24
PCIE_VSS#3 AB32
PCIE_VSS#4 AC24
PCIE_VSS#5 AC26
PCIE_VSS#6 AC27
PCIE_VSS#7 AD25
PCIE_VSS#8 AD32
PCIE_VSS#9 AE27
PCIE_VSS#10 AF32
PCIE_VSS#11 AG27
PCIE_VSS#12 AH32
PCIE_VSS#13 K28
PCIE_VSS#14 K32
PCIE_VSS#15 L27
PCIE_VSS#16 M32
PCIE_VSS#17 N25
PCIE_VSS#18 N27
PCIE_VSS#19 P25
PCIE_VSS#20 P32
PCIE_VSS#21 R27
PCIE_VSS#22 T25
PCIE_VSS#23 T32
PCIE_VSS#24 U25
PCIE_VSS#25 U27
PCIE_VSS#26 V32
PCIE_VSS#27 W25
PCIE_VSS#28 W26
PCIE_VSS#29 W27
PCIE_VSS#30 Y25
PCIE_VSS#31 Y32

GND#1 A3
GND#2 A30
GND#3 AA13
GND#4 AA16
GND#5 AB10
GND#6 AB15
GND#7 AB6
GND#8 AC9
GND#9 AD6
GND#10 AD8
GND#11 AE7
GND#12 AG12
GND#13 AH10
GND#14 AH28
GND#15 B10
GND#16 B12
GND#17 B14
GND#18 B16
GND#19 B18
GND#20 B20
GND#21 B22
GND#22 B24
GND#23 B26
GND#24 B6
GND#25 B8
GND#26 C1
GND#27 C32
GND#28 E28
GND#29 F10
GND#30 F12
GND#31 F14
GND#32 F16

GND#33 F18
GND#34 F2
GND#35 F20
GND#36 F22
GND#37 F24
GND#38 F26
GND#39 F6
GND#40 F8
GND#41 G10
GND#42 G27
GND#43 G31
GND#44 G8
GND#45 H14
GND#46 H17
GND#47 H2
GND#48 H20
GND#49 H6
GND#50 J27
GND#51 J31
GND#52 K11
GND#53 K2
GND#54 K22
GND#55 K6
GND#56 M6
GND#57 N11
GND#58 N12
GND#59 N13
GND#60 N16
GND#61 N18
GND#62 N21
GND#63 P6
GND#64 P9
GND#65 R12
GND#66 R15
GND#67 R17
GND#68 R20
GND#69 T13
GND#70 T16
GND#71 T18
GND#72 T21
GND#73 T6
GND#74 U15
GND#75 U17
GND#76 U20
GND#77 U3
GND#78 U9
GND#79 V13
GND#80 V16
GND#81 V18
GND#82 V6
GND#83 Y10
GND#84 Y15
GND#85 Y17
GND#86 Y20
GND#87 Y6
GND#88 T11
GND#89 R11

VSS_MECH#1 A32
VSS_MECH#2 AM1
VSS_MECH#3 AM32

M92-S2/M92-XT

+BBP

Q10 SI2301BDS-T1-E3

C272 1U/6.3V/X5R_4

+1.8V

Q9 2N7002W-7-F

(0.9~1.2V) +VCC_GFX_CORE

R122 100K_4 +5V

(14) BB_ENA

Q8 2N7002W-7-F

R121 10K_4

layout note: close to VDDC#[1:25]

(0.9~1.2V) +VCC_GFX_CORE

C185 1U/6.3V/X5R_4 C201 1U/6.3V/X5R_4 C202 1U/6.3V/X5R_4 C210 1U/6.3V/X5R_4 C177 1U/6.3V/X5R_4

C199 1U/6.3V/X5R_4 C207 1U/6.3V/X5R_4 C196 1U/6.3V/X5R_4 C176 1U/6.3V/X5R_4 C193 1U/6.3V/X5R_4 C206 1U/6.3V/X5R_4 C200 1U/6.3V/X5R_4 C204 1U/6.3V/X5R_4

(0.9~1.2V) +VCC_GFX_CORE

C174 10U/6.3V/X5R_6 C186 10U/6.3V/X5R_6 C188 10U/6.3V/X5R_6

(0.9~1.2V)

(0.9~1.2V) +VDDCI

C194 0.1U/10V/X7R_4 C208 0.1U/10V/X7R_4 C182 1U/6.3V/X5R_4 C203 1U/6.3V/X5R_4 C187 10U/6.3V/X5R_6

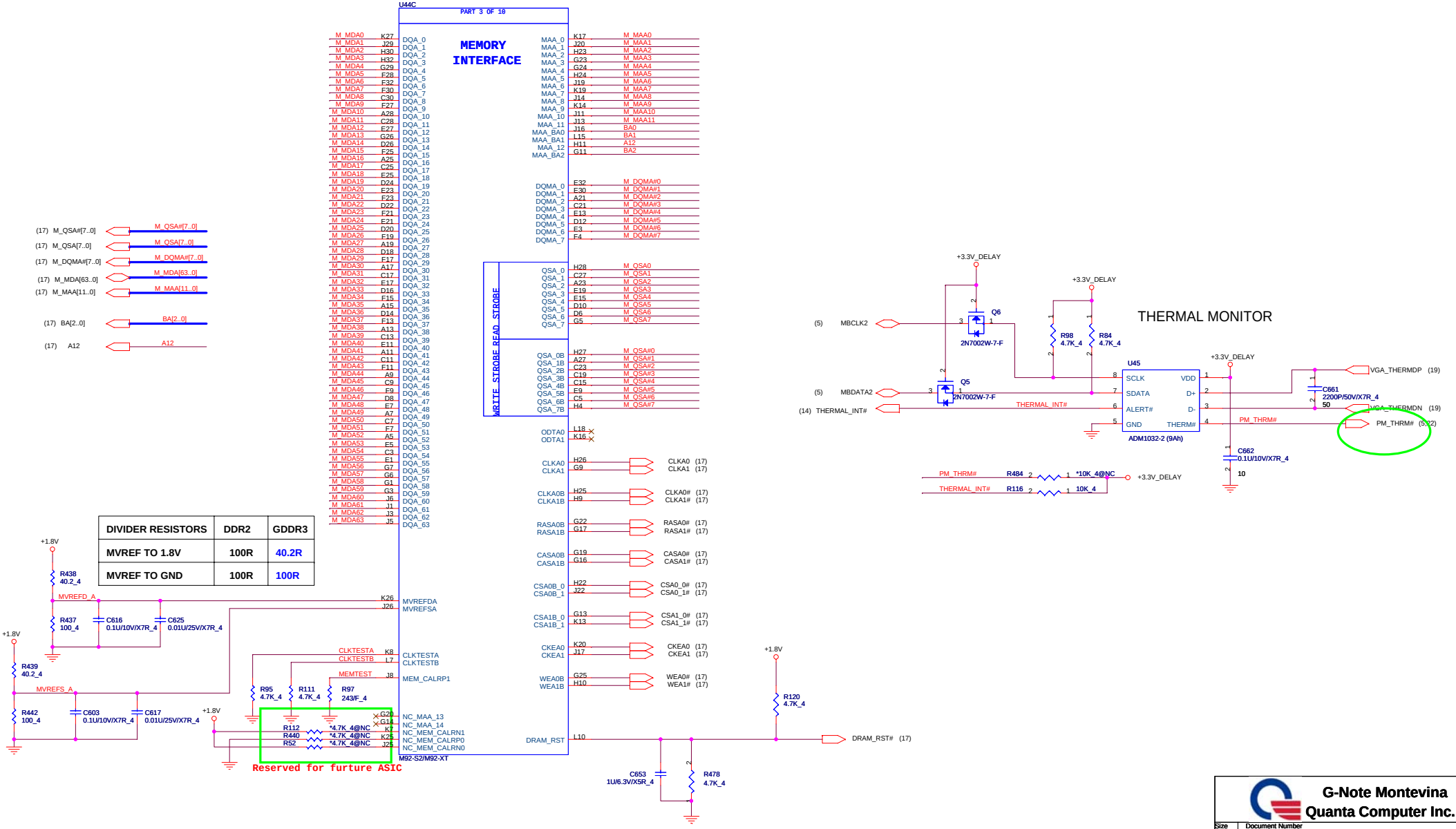
L17 BLM18EG221SN1D

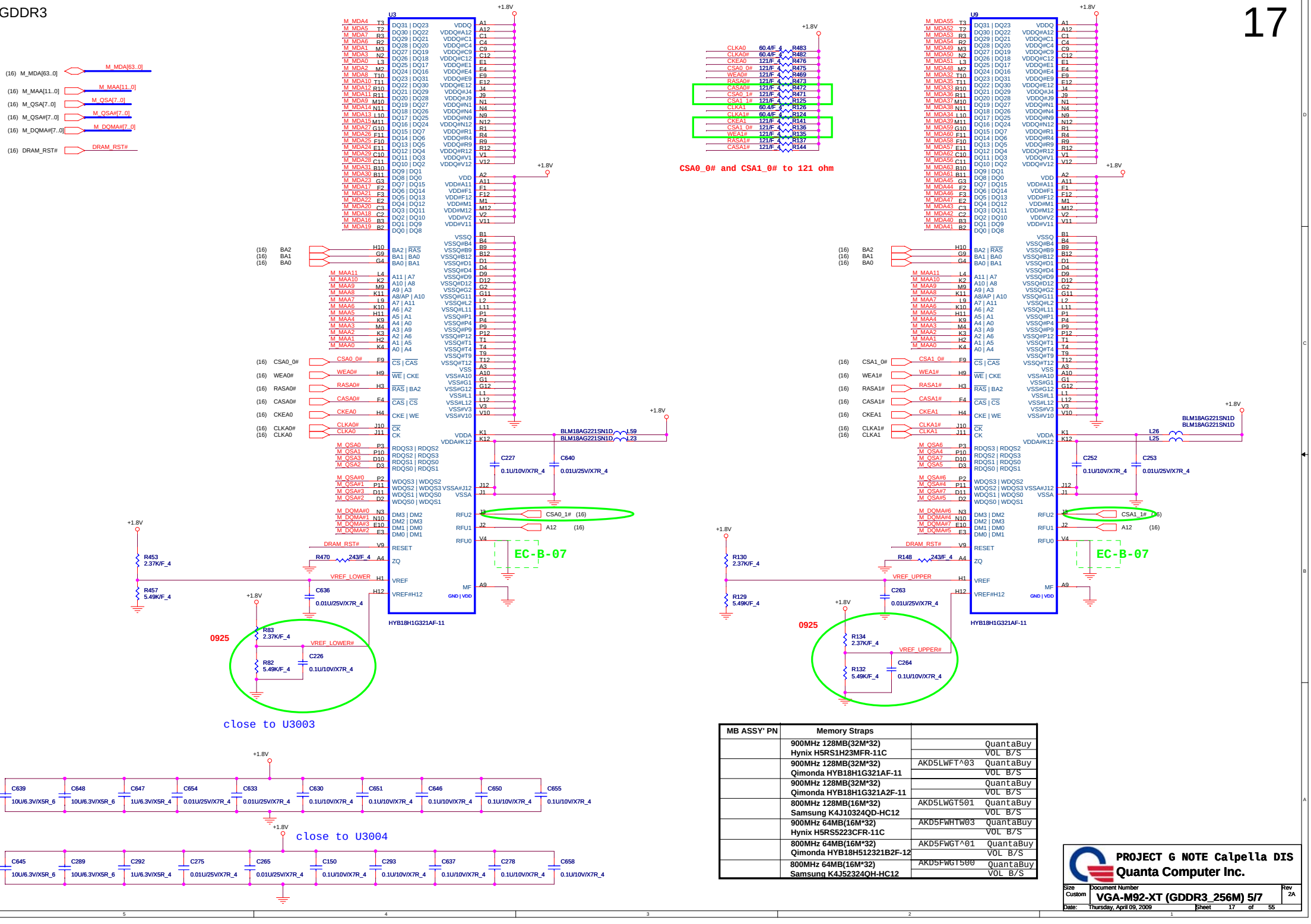
+VCC_GFX_CORE

G-Note Montevina
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M92-XT_POWER/GND	2A
Date: Thursday, April 09, 2009	Sheet 15 of 55	

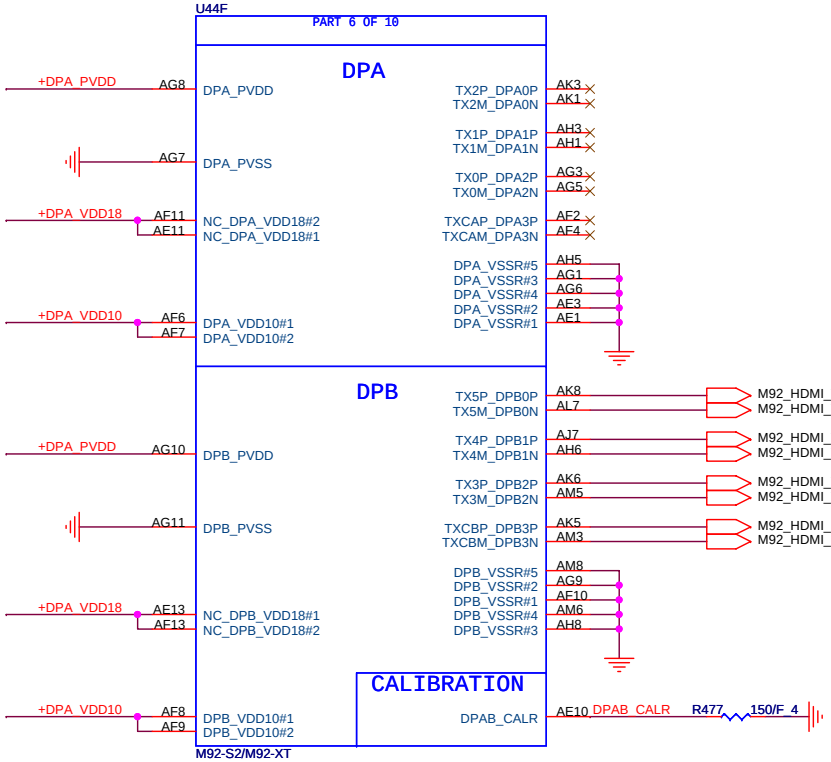
MEMORY INTERFACE



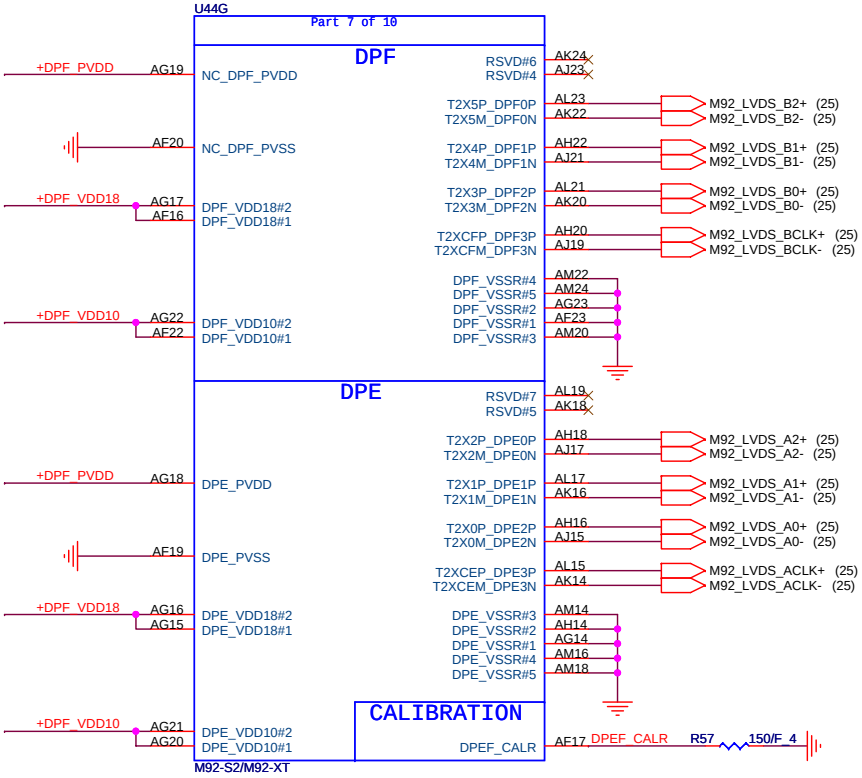


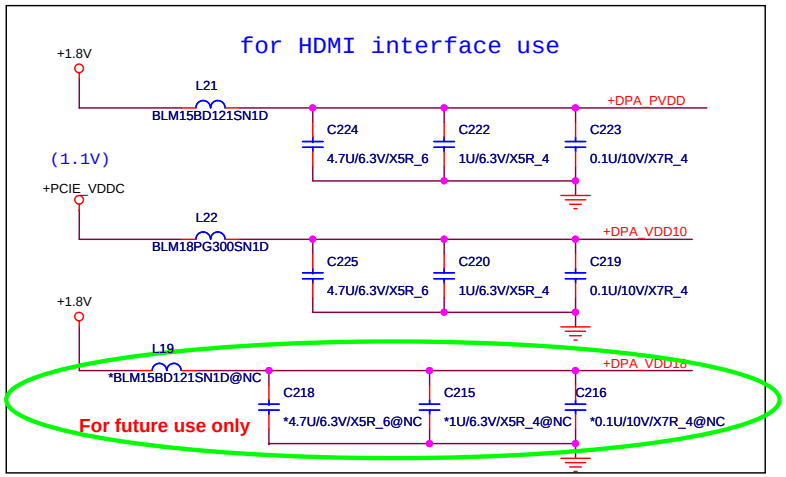
MB ASSY' PN	Memory Straps	
	900MHz 128MB(32M*32) Hynix H5RS1H23MFR-11C	QuantaBuy VOL B/S
	900MHz 128MB(32M*32) Qimonda HYB18H1G321AF-11	AKD5LWFT^03 QuantaBuy VOL B/S
	900MHz 128MB(32M*32) Qimonda HYB18H1G321A2F-11	QuantaBuy VOL B/S
	800MHz 128MB(16M*32) Samsung K4J10324QD-HC12	AKD5LWGT501 QuantaBuy VOL B/S
	900MHz 64MB(16M*32) Hynix H5RS5223CFR-11C	AKD5FWHTW03 QuantaBuy VOL B/S
	800MHz 64MB(16M*32) Qimonda HYB18H512321B2F-12	AKD5FWGT^01 QuantaBuy VOL B/S
	800MHz 64MB(16M*32) Samsung K4J52324QH-HC12	AKD5FWGT500 QuantaBuy VOL B/S

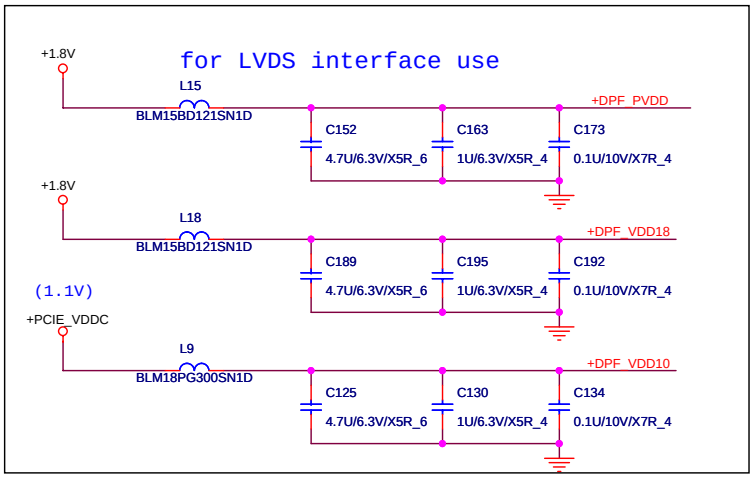
TMDP(HDMI) INTERFACE



LVDS INTERFACE



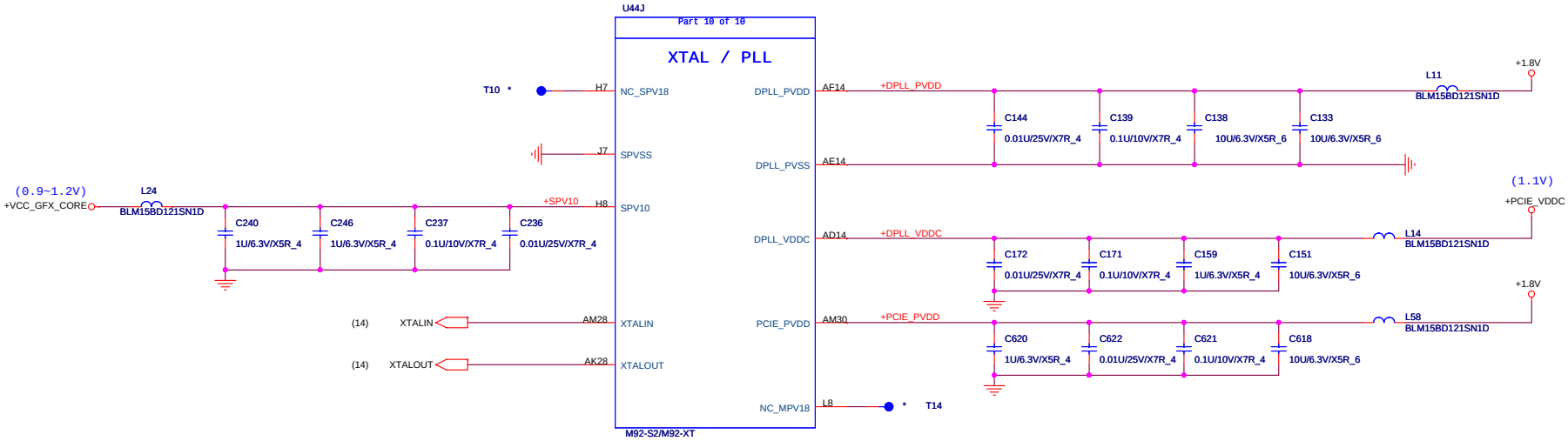


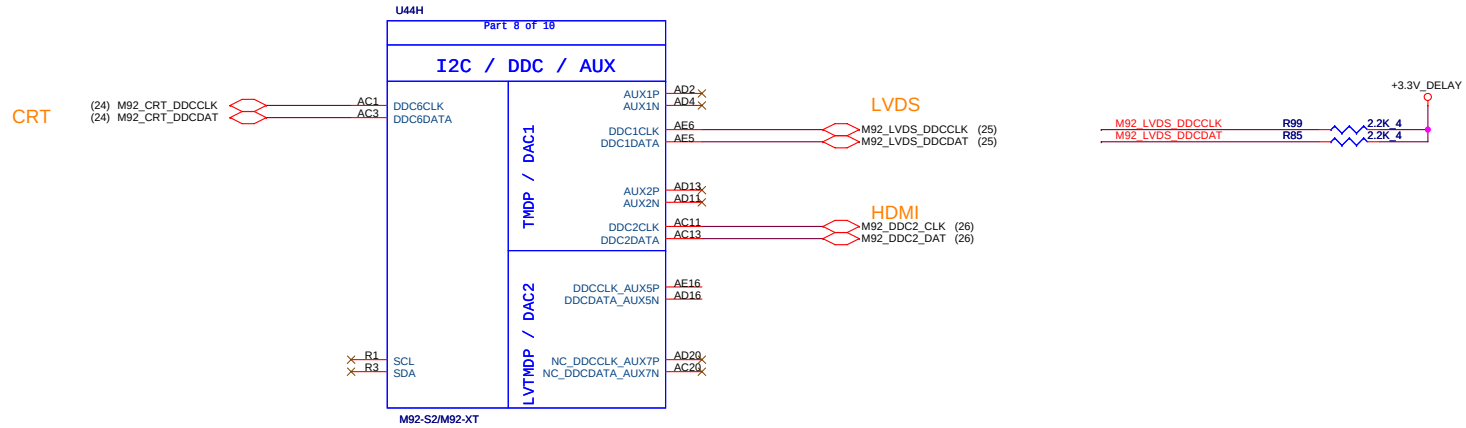


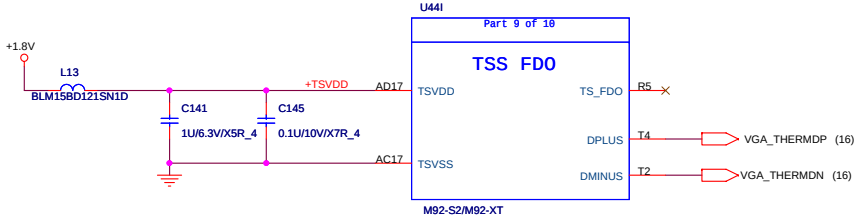
G-Note Montevina
Quanta Computer Inc.

Size	Document Number	Rev
B	M92-XT_TMDP I/F	2A

Date: Thursday, April 09, 2009 Sheet 18 of 55



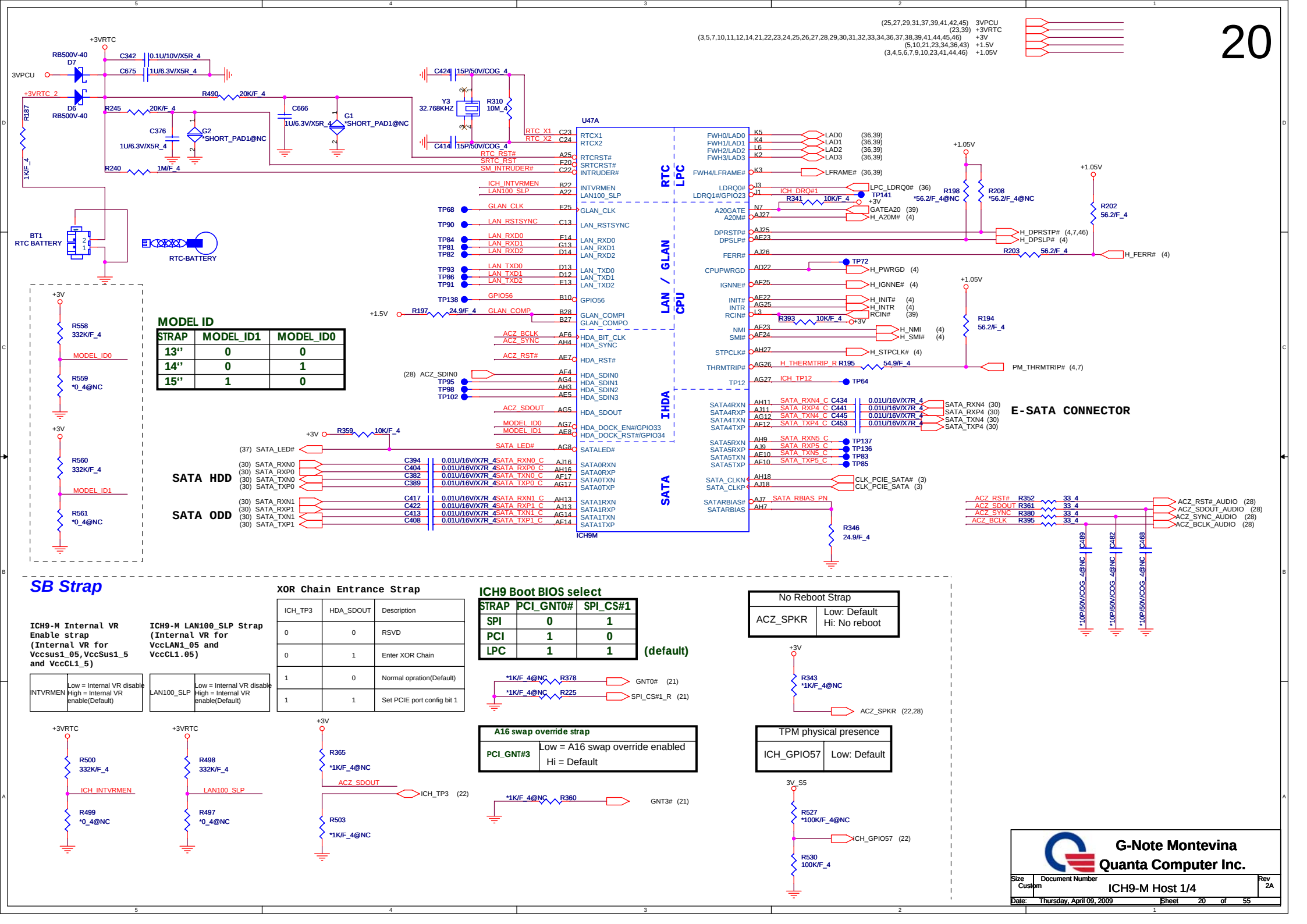




G-Note Montevina
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M92-XT_XTAL/PLL/I2C	2A

Date: Thursday, April 09, 2009 Sheet 19 of 55


U47A
ICH9M
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
MODEL ID
STRAP MODEL_ID1 MODEL_ID0
13'' 0 0
14'' 0 1
15'' 1 0
E-SATA CONNECTOR
SATA HDD
SATA ODD
SB Strap
ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)
INTVRMEN Low = Internal VR disable High = Internal VR enable(Default)
ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)
LAN100_SLP Low = Internal VR disable High = Internal VR enable(Default)
XOR Chain Entrance Strap
ICH_TP3 HDA_SDOUT Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal opration(Default)
1 1 Set PCIE port config bit 1
ICH9 Boot BIOS select
STRAP PCI_GNT0# SPI_CS#1
SPI 0 1
PCI 1 0
LPC 1 1
(default)
No Reboot Strap
ACZ_SPKR Low: Default Hi: No reboot
A16 swap override strap
PCI_GNT#3 Low = A16 swap override enabled Hi = Default
TPM physical presence
ICH_GPIO57 Low: Default
G-Note Montevina
Quanta Computer Inc.
ICH9-M Host 1/4
Size Custom
Rev 2A
Date: Thursday, April 09, 2009
Sheet 20 of 55

(5,10,20,23,34,36,43) +1.5V
(3,5,7,10,11,12,14,20,22,23,24,25,26,27,28,29,30,31,32,33,34,36,37,38,39,41,44,45,46) +3V
(22,27,34,39,41,43,46,47) 3VSUS

CARD-READER

MINI CARD PCI-E(WWAN)

MINI CARD PCI-E(WLAN)

EXPRESS CARD (NEW CARD)

PCIE-LAN

EC-B-04

EC-B-04

EC-A-06

U47D — ICH9M

PCI-Express

Direct Media Interface

SPI

USB

U47B — ICH9M

PCI

Interrupt I/F

USB Connector
USB Connector
Finger Printer
BLUETOOTH
CAMERA MODULE
USB Connector
USB Connector
NEW CARD
WWAN Min-Card
WLAN Min-Card

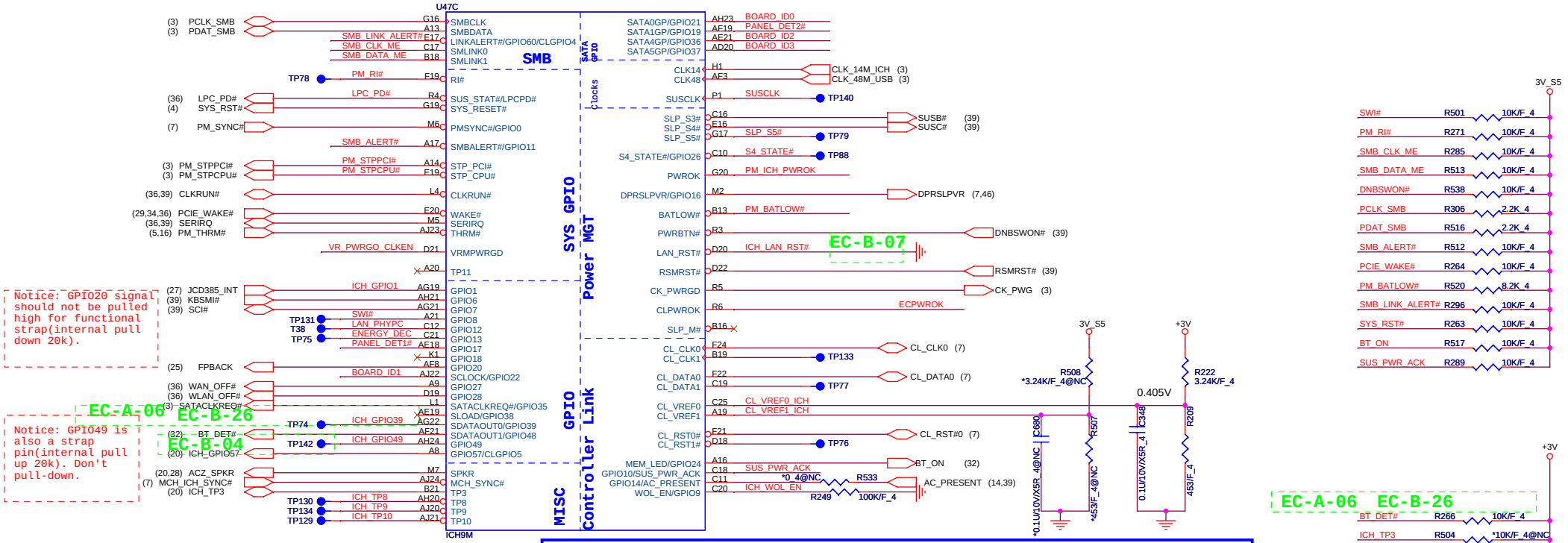
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTE#, F#, G#	RICOH R5C847

G-Note Montevina
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M PCIE 2/4	2A

Date: Thursday, April 09, 2009 Sheet 21 of 55

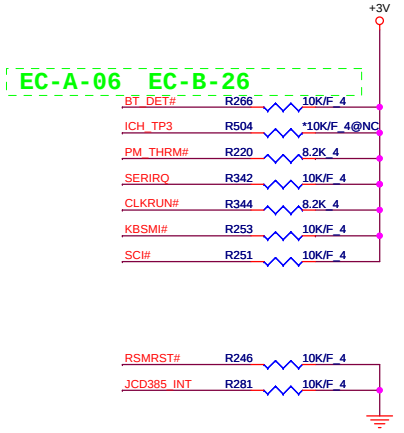
(5,10,20,21,23,34,36,43) +1.5V
(3,5,7,10,11,12,14,20,21,23,24,25,26,27,28,29,30,31,32,33,34,36,37,38,39,41,44,45,46) +3V
(20,21,23,41) 3V_S5
(21,27,34,39,41,43,46,47) 3VSUS

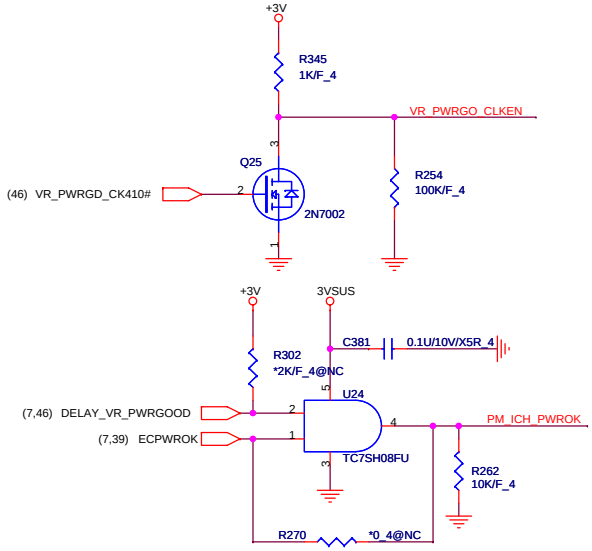


Notice: GPIO20 signal should not be pulled high for functional strap(internal pull down 20k).

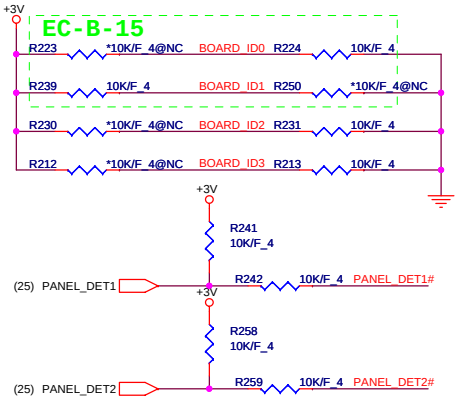
Notice: GPIO49 is also a strap pin(internal pull up 20k). Don't pull-down.

EC-A-06 EC-B-26
EC-B-04





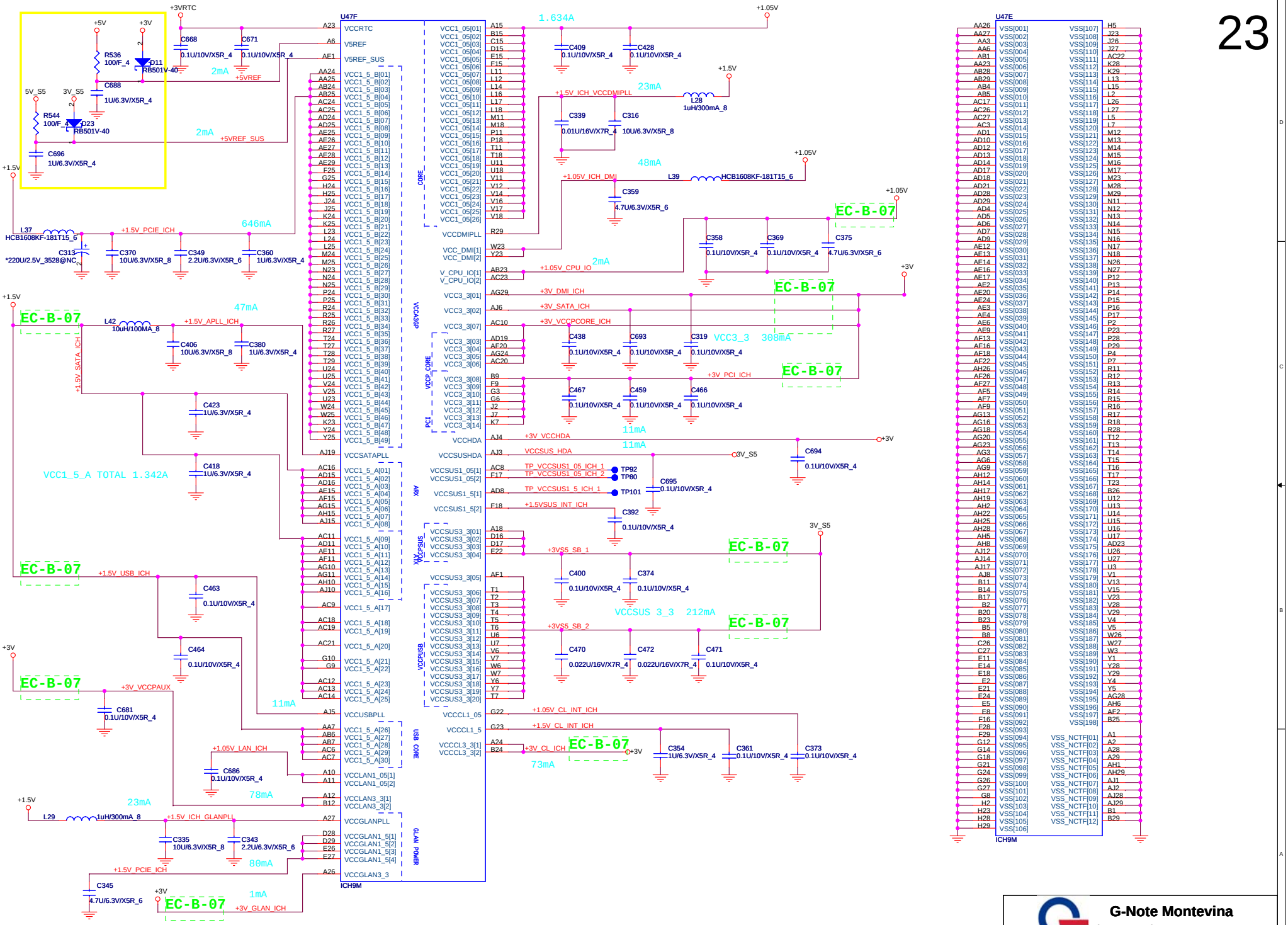
Board ID For Function	ID3 GPIO37	ID2 GPIO36	ID1 GPIO22	ID0 GPIO21
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	0	1	1
SOVP	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1



Model ID	PANEL_DET2	PANEL_DET1
13"	0	0
14"	0	1
15"	1	0
Default	1	1

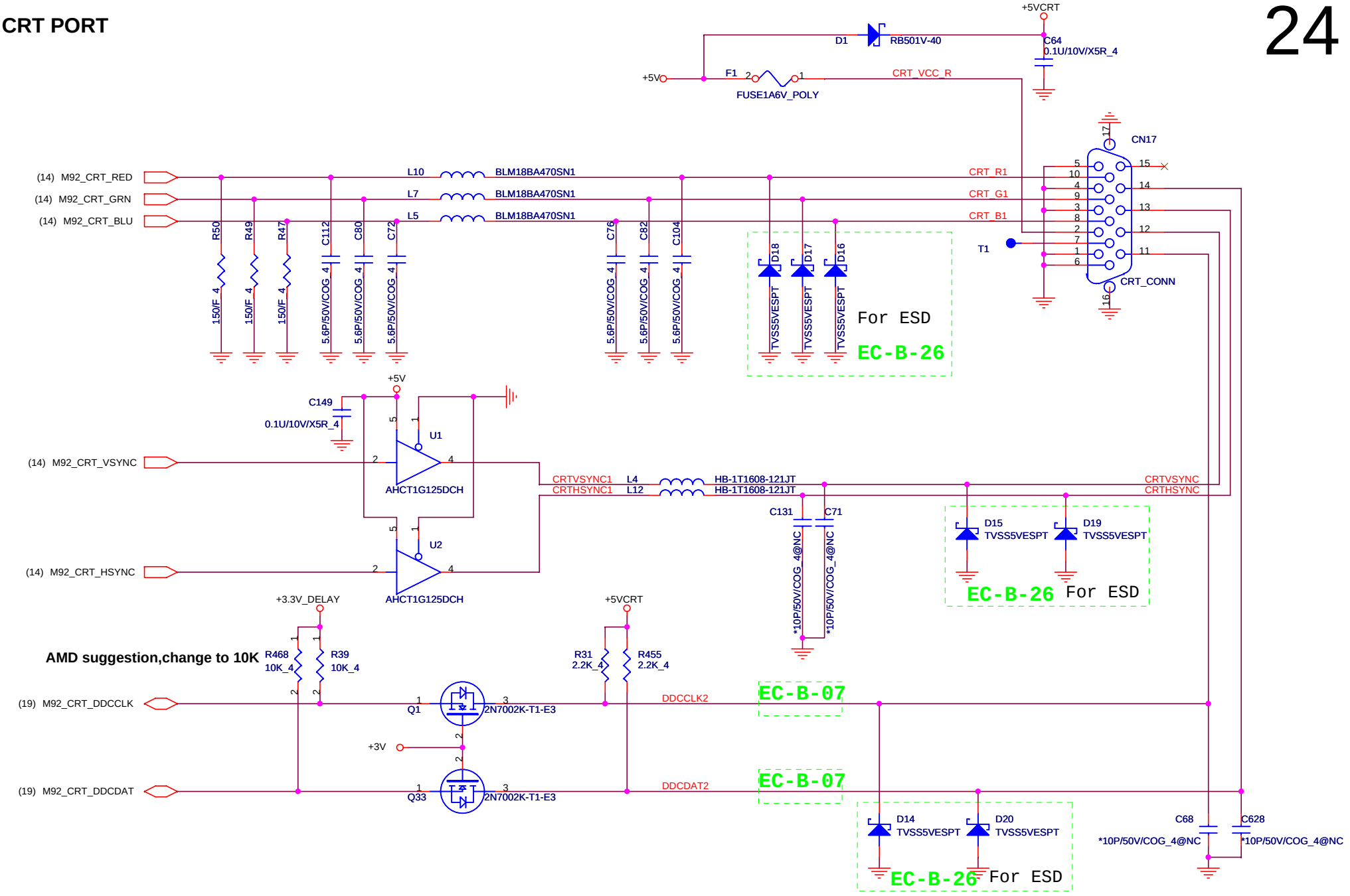
G-Note Montevina
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M GPIO 3/4	2A
Date: Thursday, April 09, 2009	Sheet 22 of 55	



Company	G-Note Montevina Quanta Computer Inc.
Size	Custom
Document Number	ICH9-M Power 4/4
Rev	2A
Date:	Friday, March 06, 2009
Sheet	23 of 55

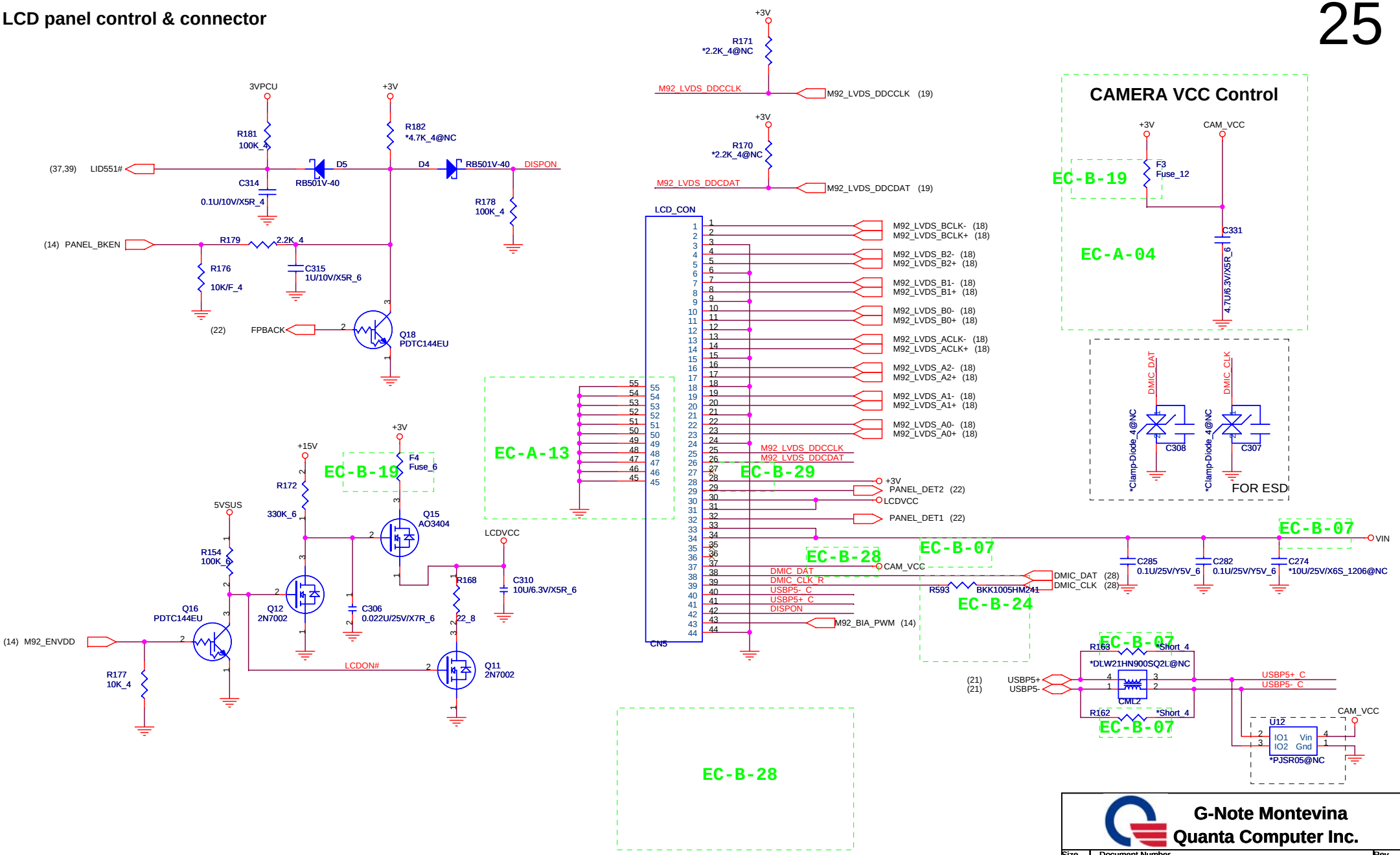
CRT PORT



G-Note Montevina
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT CON	2A
Date: Thursday, April 09, 2009	Sheet 24 of 55	

LCD panel control & connector



G-Note Montevina Quanta Computer Inc.		
Size B	Document Number LCD/LID/CAM CON	Rev 2A
Date: Thursday, April 09, 2009	Sheet 25 of 55	

HDMI PORT

(18) M92_HDMI_TX2+ — C332 0.1U/10V/X7R_4 — M92_HDMI_TX2+_R
(18) M92_HDMI_TX2- — C330 0.1U/10V/X7R_4 — M92_HDMI_TX2-_R
(18) M92_HDMI_TX1+ — C344 0.1U/10V/X7R_4 — M92_HDMI_TX1+_R
(18) M92_HDMI_TX1- — C340 0.1U/10V/X7R_4 — M92_HDMI_TX1-_R
(18) M92_HDMI_TX0+ — C355 0.1U/10V/X7R_4 — M92_HDMI_TX0+_R
(18) M92_HDMI_TX0- — C352 0.1U/10V/X7R_4 — M92_HDMI_TX0-_R
(18) M92_HDMI_CLK+ — C364 0.1U/10V/X7R_4 — M92_HDMI_CLK+_R
(18) M92_HDMI_CLK- — C372 0.1U/10V/X7R_4 — M92_HDMI_CLK-_R

R191 499/F_4 M92_HDMI_TX2+_C
R188 499/F_4 M92_HDMI_TX2-_C
R205 499/F_4 M92_HDMI_TX1+_C
R199 499/F_4 M92_HDMI_TX1-_C
R226 499/F_4 M92_HDMI_TX0+_C
R215 499/F_4 M92_HDMI_TX0-_C
R236 499/F_4 M92_HDMI_CLK+_C
R243 499/F_4 M92_HDMI_CLK-_C

+3V — Q24 2N7002W-7-F

L30: M92_HDMI_TX2+_R / M92_HDMI_TX2-_R → M92_HDMI_TX2+_C / M92_HDMI_TX2-_C
*EXC24CG240U@NC
R192 *Short_4
R189 *Short_4
EC-B-07

L32: M92_HDMI_TX1+_R / M92_HDMI_TX1-_R → M92_HDMI_TX1+_C / M92_HDMI_TX1-_C
*EXC24CG240U@NC
R206 *Short_4
R200 *Short_4
EC-B-07

L35: M92_HDMI_TX0+_R / M92_HDMI_TX0-_R → M92_HDMI_TX0+_C / M92_HDMI_TX0-_C
*EXC24CG240U@NC
R227 *Short_4
R216 *Short_4
EC-B-07

L38: M92_HDMI_CLK+_R / M92_HDMI_CLK-_R → M92_HDMI_CLK+_C / M92_HDMI_CLK-_C
*EXC24CG240U@NC
R237 *Short_4
R244 *Short_4
EC-B-07

+3.3V_DELAY
R184 10K_4
R185 10K_4
(19) M92_DDC2_CLK
(19) M92_DDC2_DAT
Q20 FDV301N — HDMI_CLK
Q21 FDV301N — HDMI_DAT

U18 *RClamp0514M_AG@NC
M92_HDMI_TX2+_C / M92_HDMI_TX2-_C
M92_HDMI_TX1+_C / M92_HDMI_TX1-_C
U21 *RClamp0514M_AG@NC
M92_HDMI_TX0+_C / M92_HDMI_TX0-_C
M92_HDMI_CLK+_C / M92_HDMI_CLK-_C
U22 *RClamp0514M_AG@NC
HDMI_DAT / HDMI_CLK
HDMIC_5V / HP_DET
VCC GND

For ESD
Layout note:Place close to HDMI Conn

EC-B-18
+5V
R247 2.2K_4
R248 2.2K_4
F2 — HDMIC_5V — FUSE1A6V_POLY

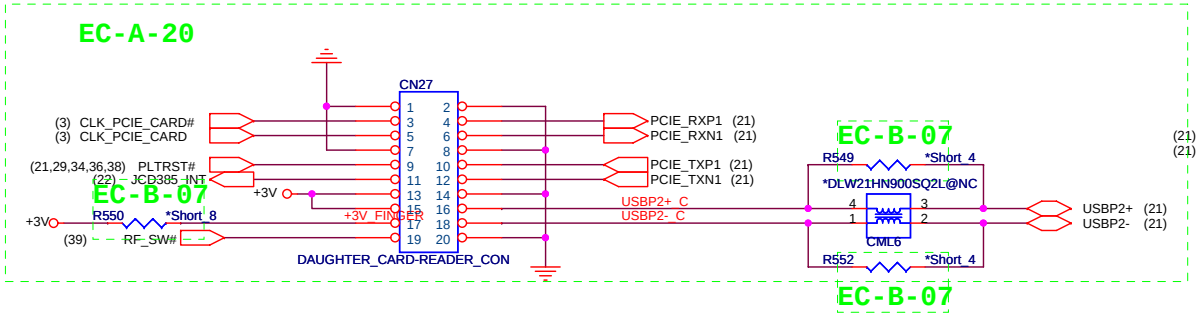
CN21 — ABA-HDM-018-K01
SHELL1 SHELL2 GND
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET
M92_HDMI_TX2+_C / M92_HDMI_TX2-_C / M92_HDMI_TX1+_C / M92_HDMI_TX1-_C / M92_HDMI_TX0+_C / M92_HDMI_TX0-_C / M92_HDMI_CLK+_C / M92_HDMI_CLK-_C

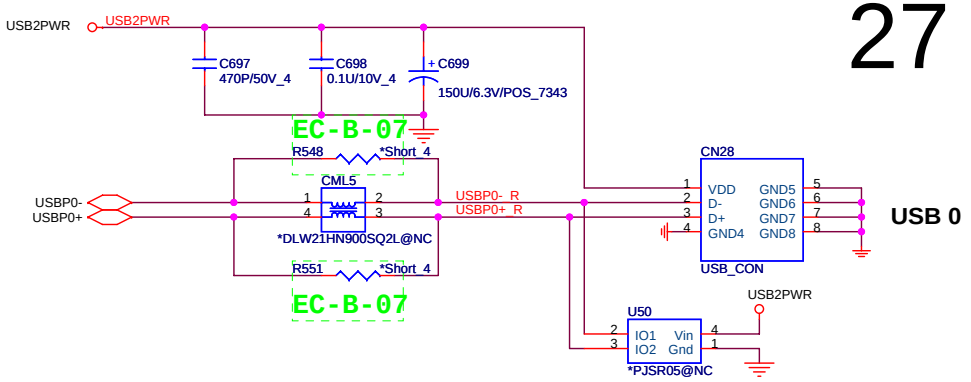
EC-A-17
+3.3V_DELAY
(14) M92_HDMI_HPD
R581 10K_4
R582 10K_4
Q41 MMST3904-7-F
Q42 DTC114TUAT106
HP_DET
R583 100K_4

G-Note Montevina
Quanta Computer Inc.

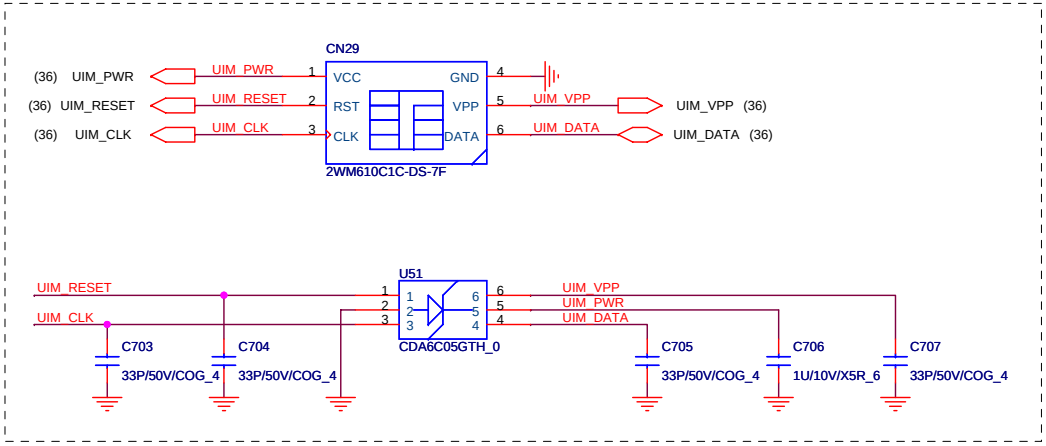
Size	Document Number	Rev
Custom	HDMI PORT	2A
Date: Thursday, April 09, 2009	Sheet 26 of 55	

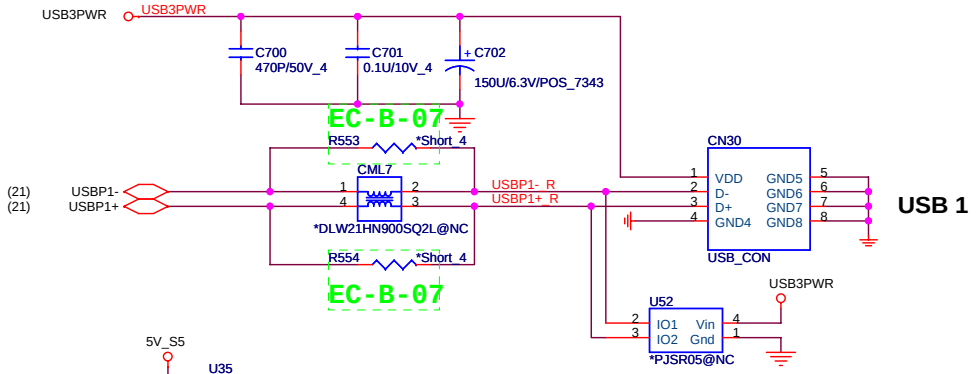
WIRE TO BOARD CONN CARD READER & FINGERPRINT



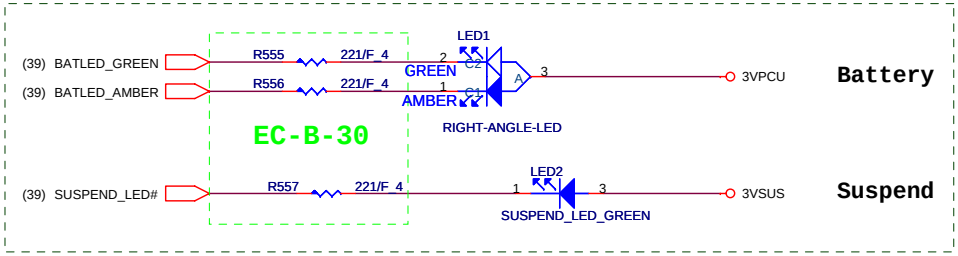


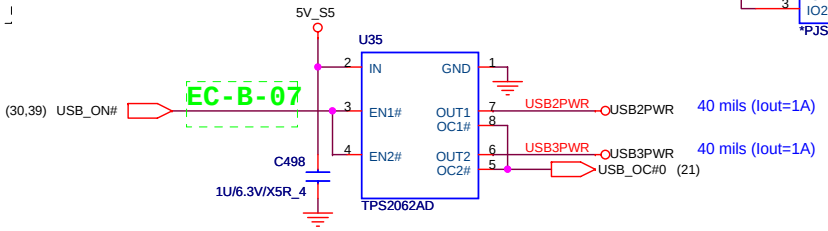
SIM Card CONN





FRONT LEDs

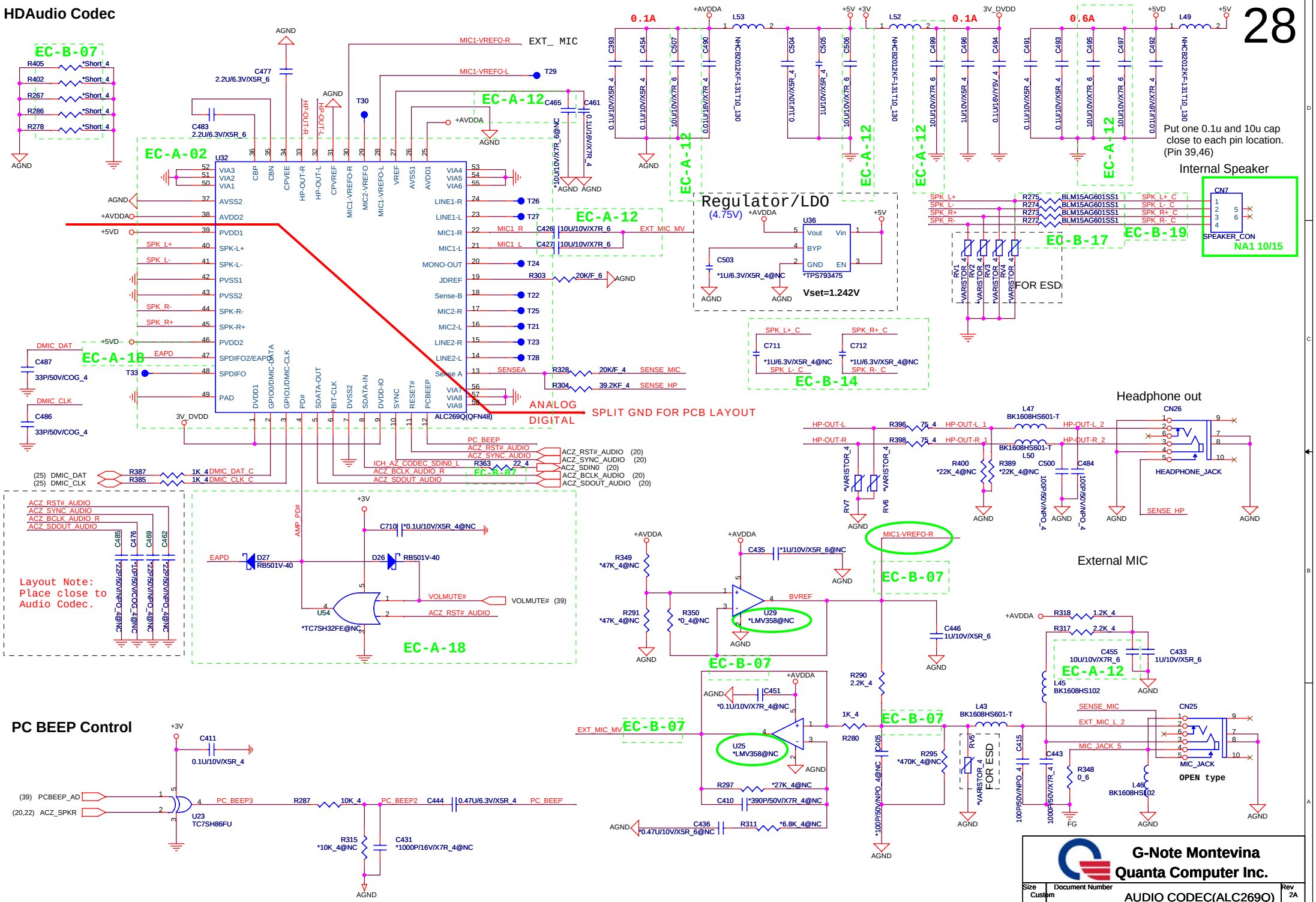




PROJECT :G NOTE
Quanta Computer Inc.

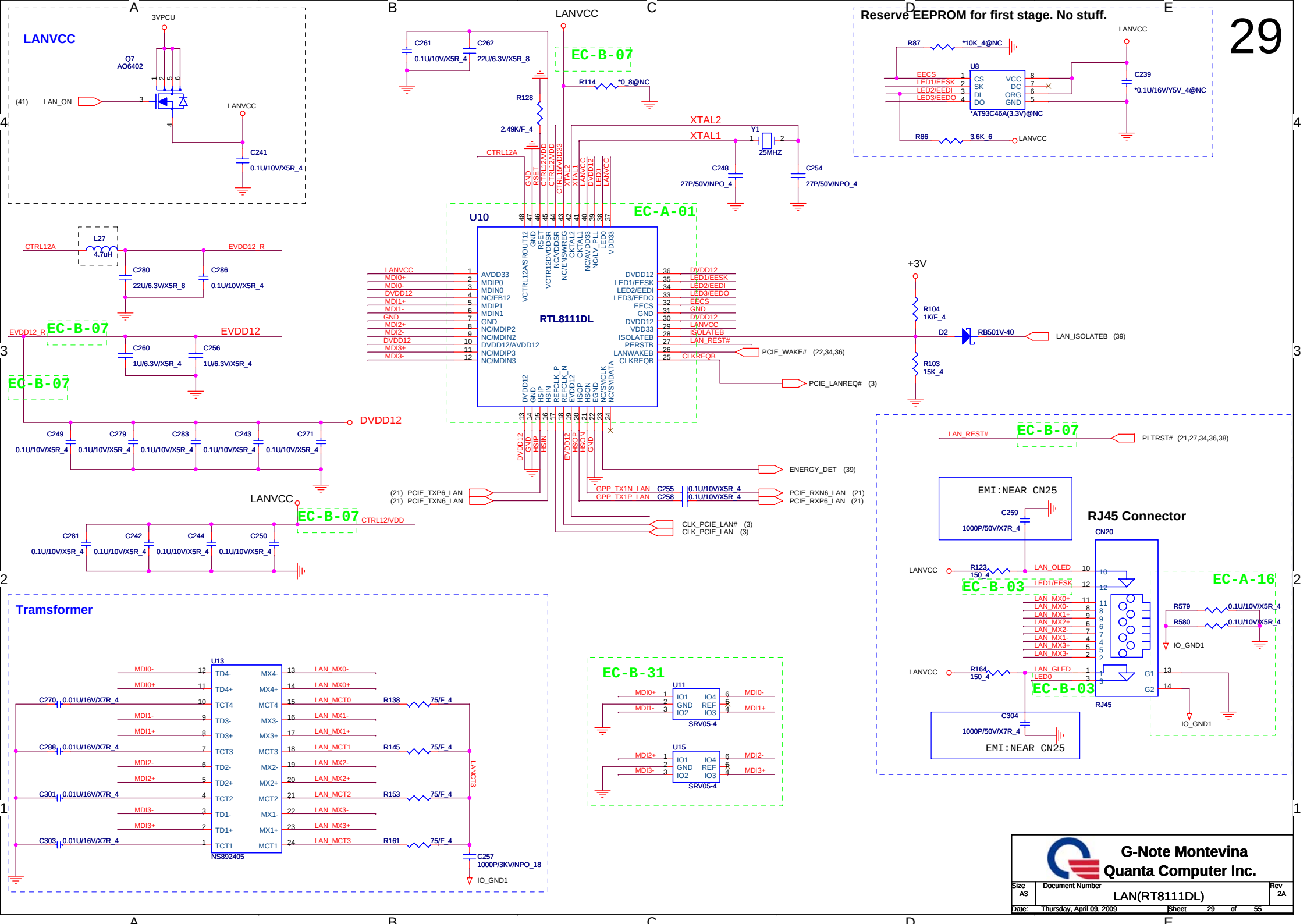
Size	Document Number	Rev
Custom	USB X2/SIM_CARD/LEDs/RF	2A
Date: Thursday, April 09, 2009	Sheet 27 of 55	

HDAudio Codec



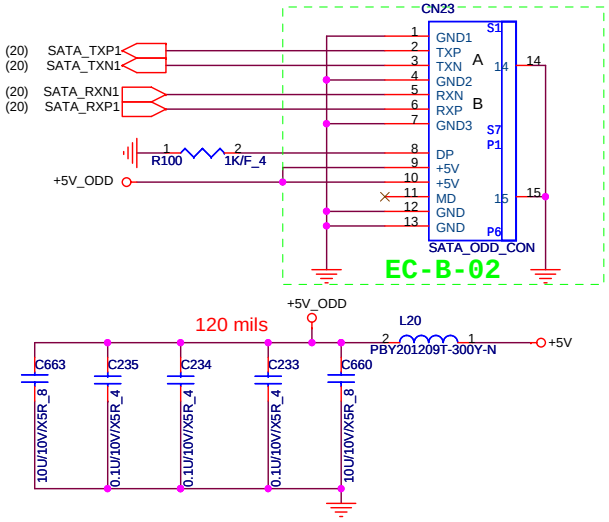
Size	Custom
Document Number	AUDIO CODEC(ALC269Q)
Rev	2A
Date:	Thursday, April 09, 2009
Sheet	28 of 55

G-Note Montevina
Quanta Computer Inc.

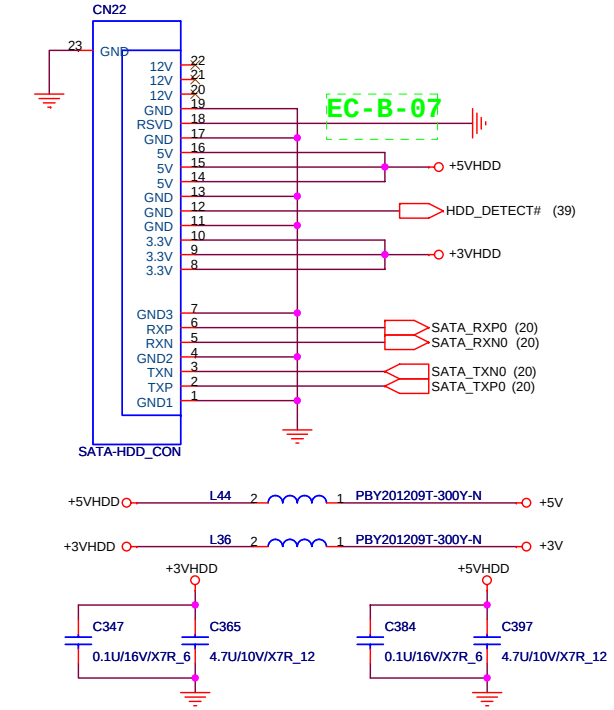


G-Note Montevina	Quanta Computer Inc.
Size: A3	Document Number: LAN(RT8111DL)
Rev: 2A	
Date: Thursday, April 09, 2009	Sheet 29 of 55

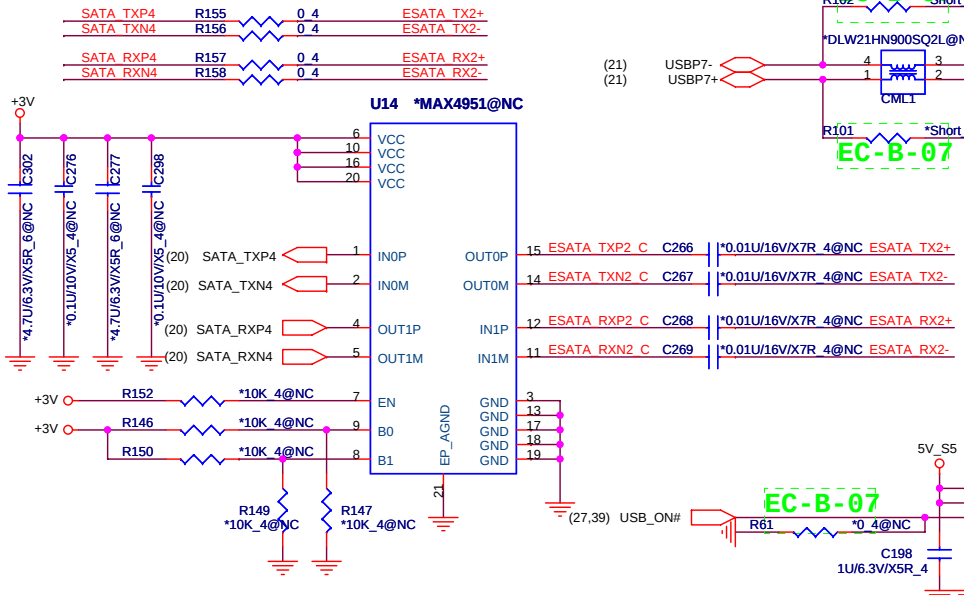
SATA CD-ROM



SATA-HDD

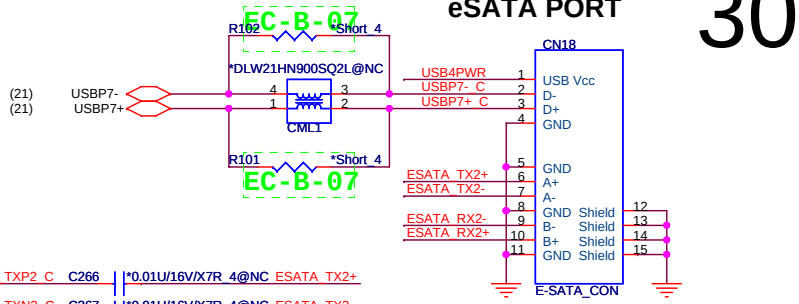


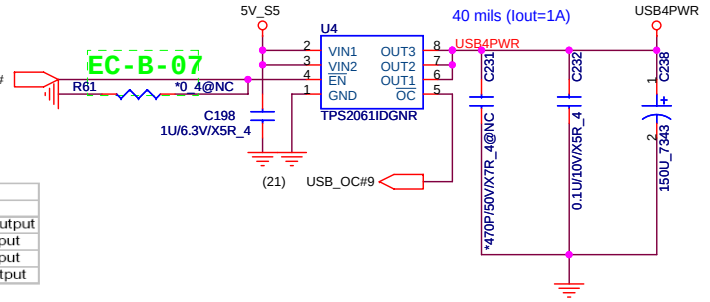
E-SATA RE-DRIVER

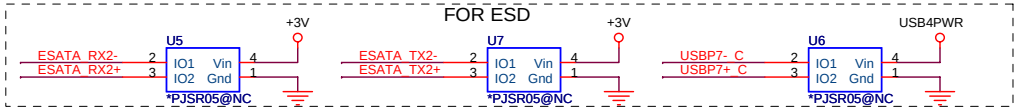


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

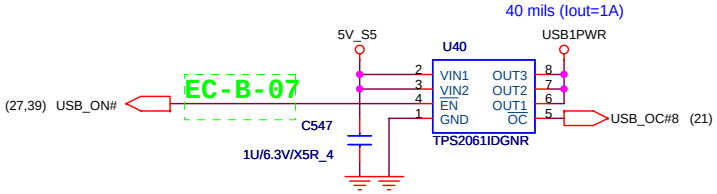
eSATA PORT



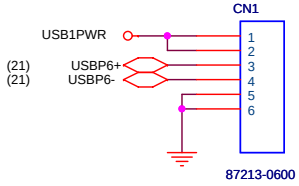




USB x1(on board)



REAR_USB/B connector



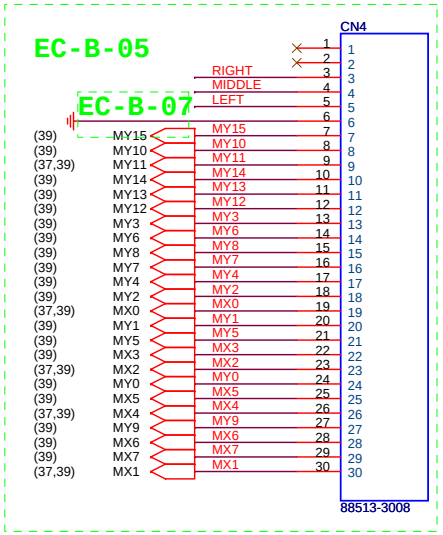
G-Note Montevina
Quanta Computer Inc.

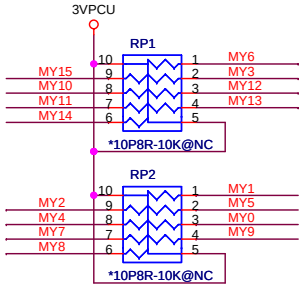
Size	Document Number	Rev
B	SATA HDD/ ODD/ eSATA/USB	2A

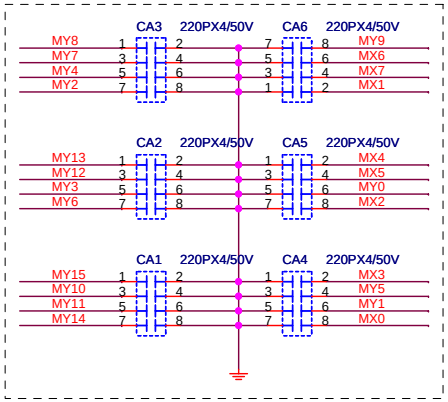
Date: Thursday, April 09, 2009 Sheet 30 of 55

FAN, K/B, T/P & Track Point

KEYBOARD connector

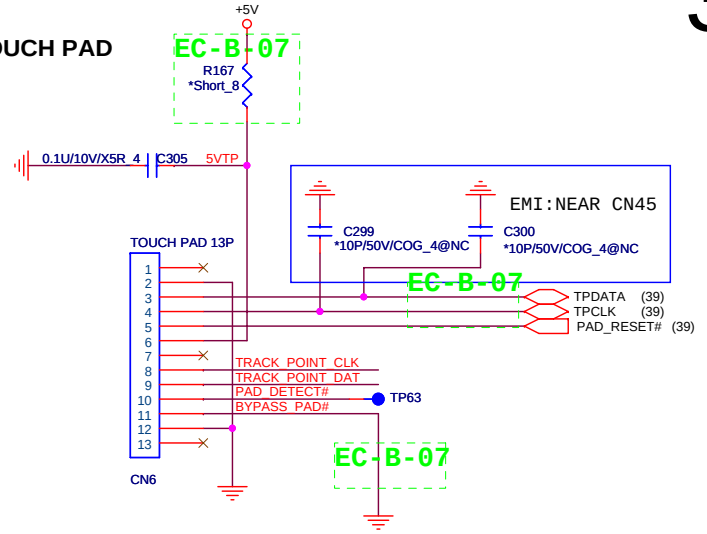




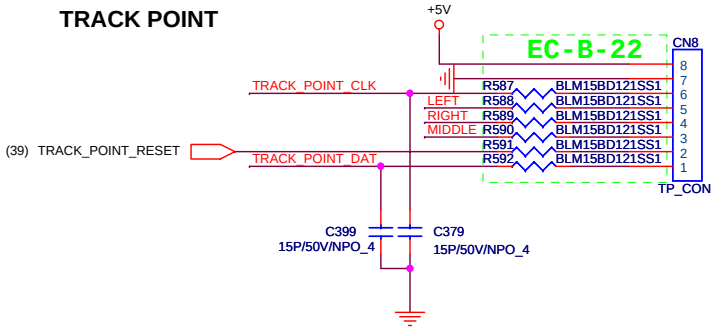


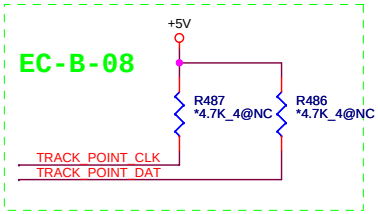
For EMI request

TOUCH PAD

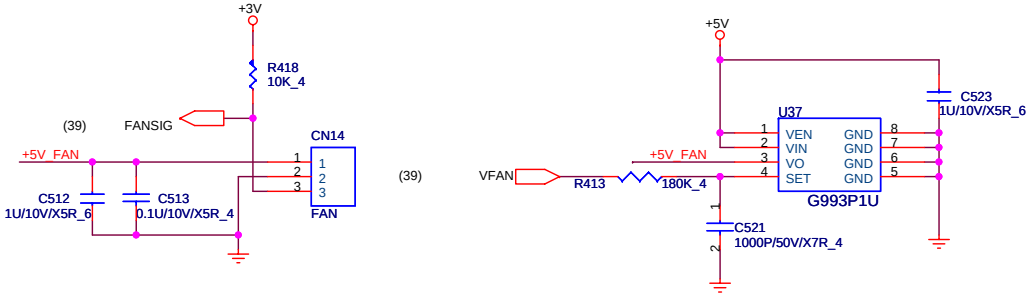


TRACK POINT



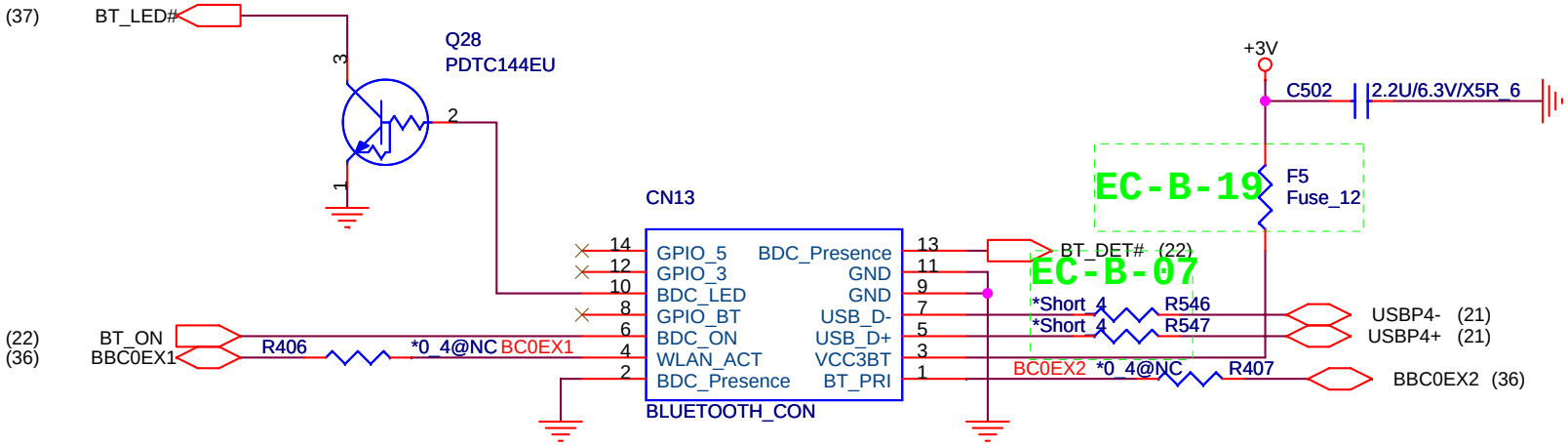


FAN Controller



G-Note Montevina Quanta Computer Inc.		
Size B	Document Number KB/ TP/ FAN Control	Rev 2A
Date: Thursday, April 09, 2009	Sheet 31 of 55	

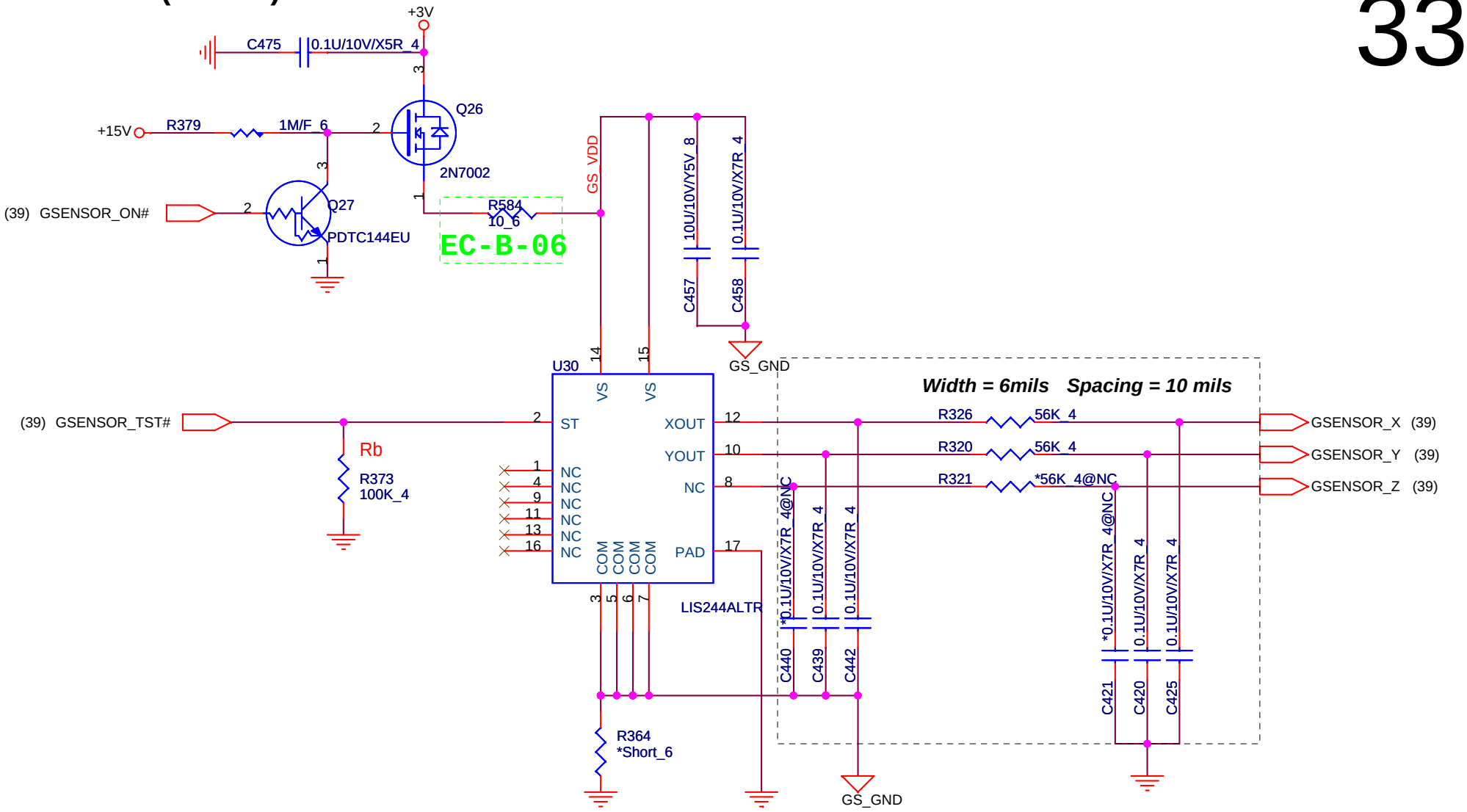
BLUETOOTH



G-Note Montevina Quanta Computer Inc.		
Size: A	Document Number: B/T	Rev: 2A
Date: Thursday, April 09, 2009	Sheet 32 of 55	

G-SENSOR (2-Axial)

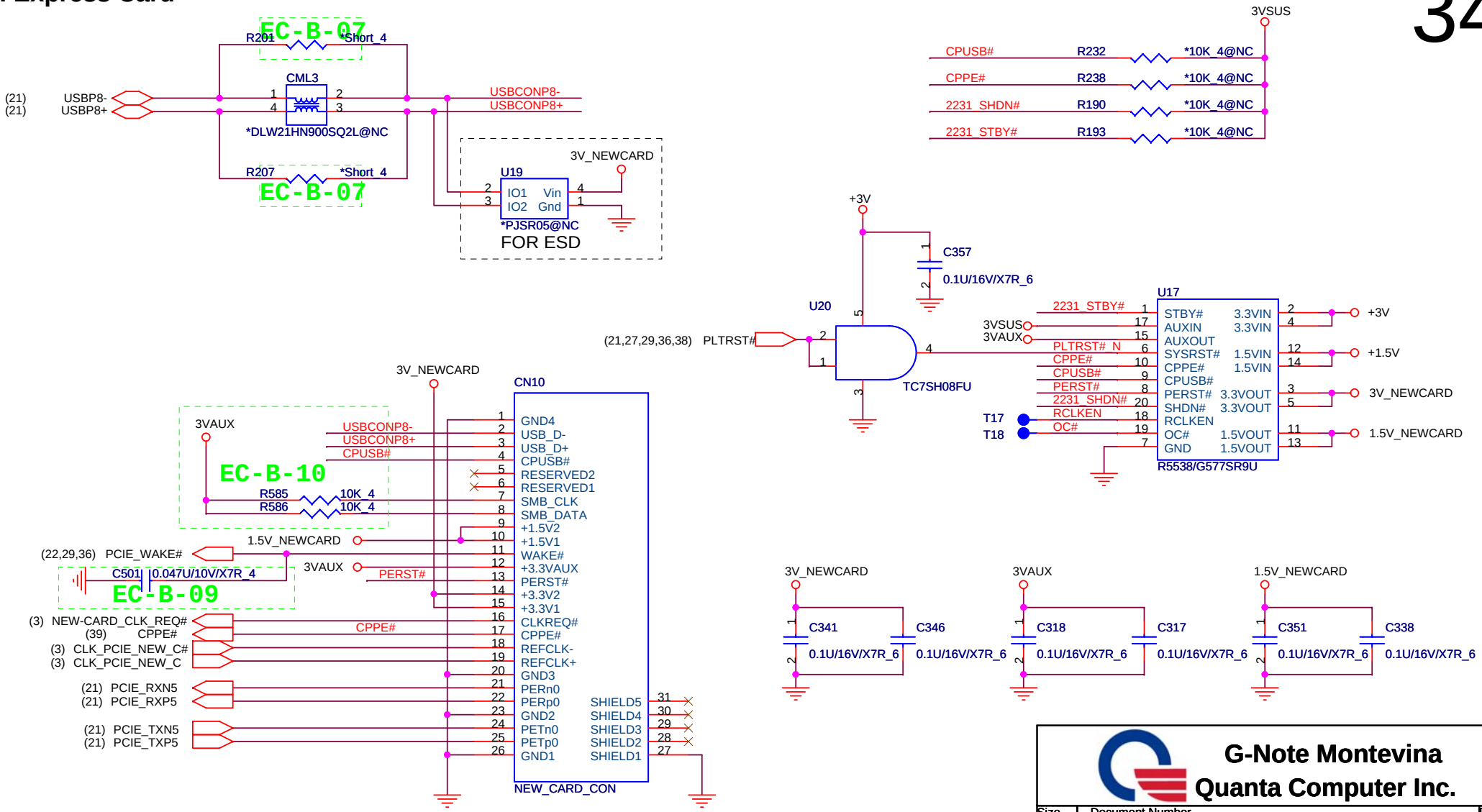
33



G-Note Montevina Quanta Computer Inc.		
Size: A	Document Number: G-SENSOR	Rev: 2A
Date: Thursday, April 09, 2009	Sheet 33 of 55	

PCI Express Card

34



G-Note Montevina
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCI Express Card	2A
Date: Thursday, April 09, 2009	Sheet 34 of 55	

Mini PCI-E Card

EC-B-04

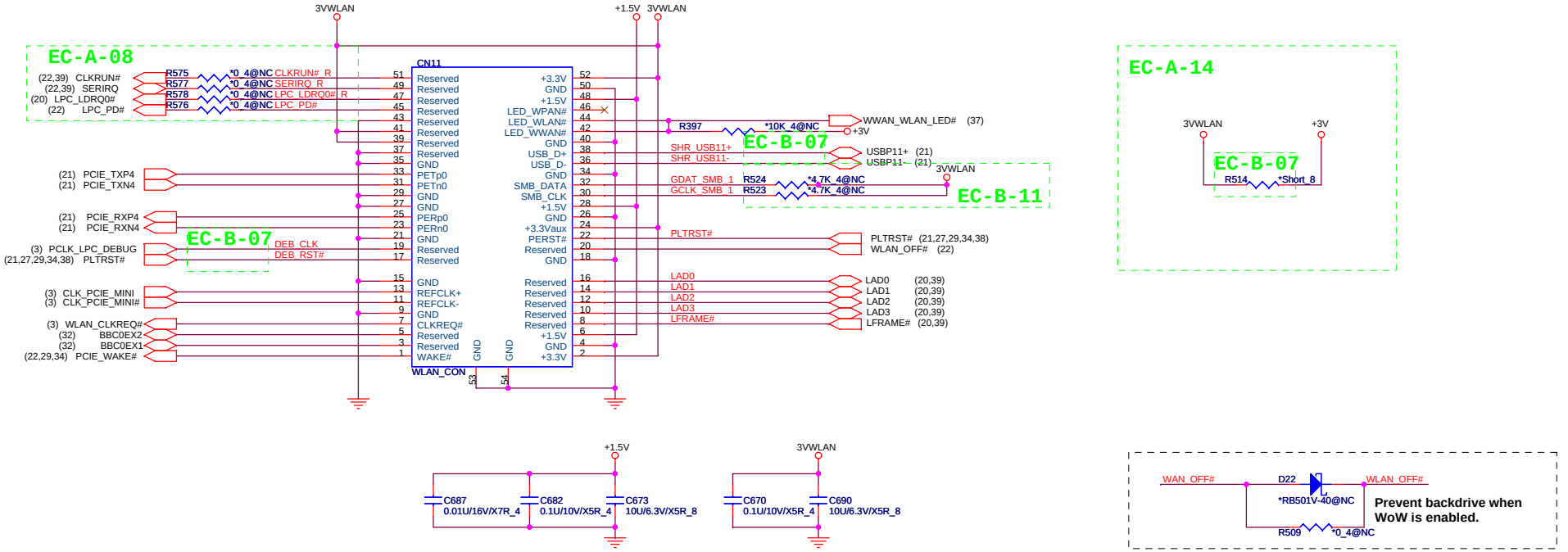
35

G-Note Montevina
Quanta Computer Inc.

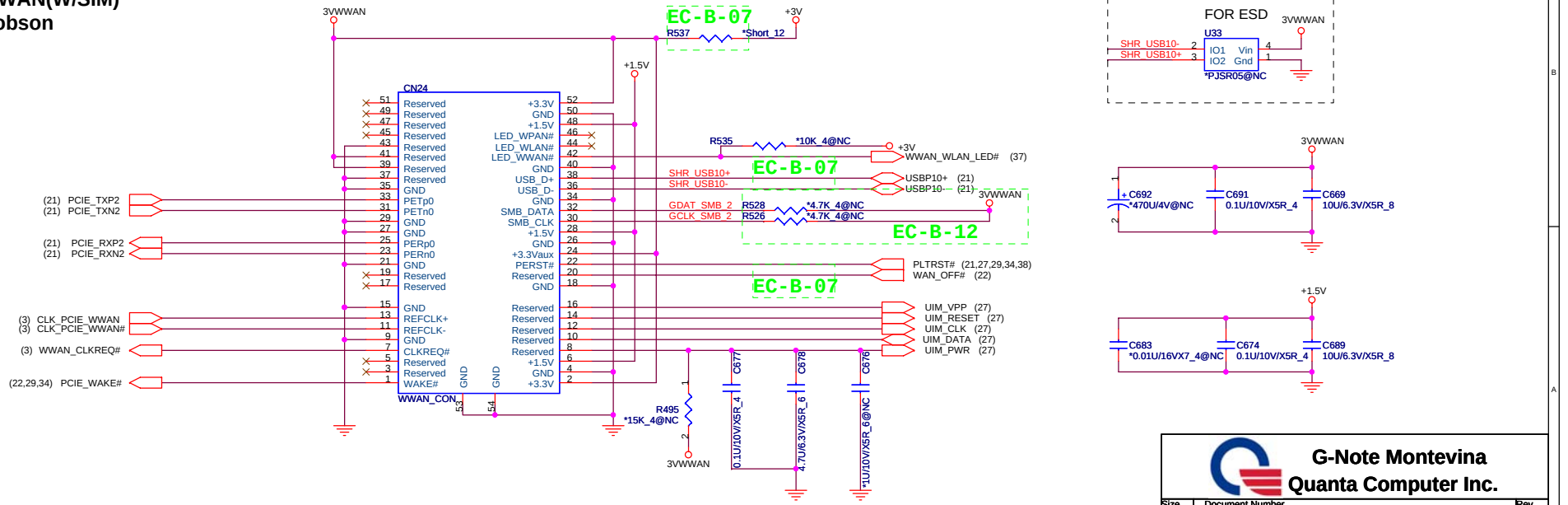
Size	Document Number	Rev
A	Mini PCI-E Card	2A

Date: Friday, March 06, 2009 Sheet 35 of 55

Mini PCI-E Card (F2)
(WLAN/ WiMAX)



Mini PCI-E Card (F1)
WWAN(W/SIM)
Robson

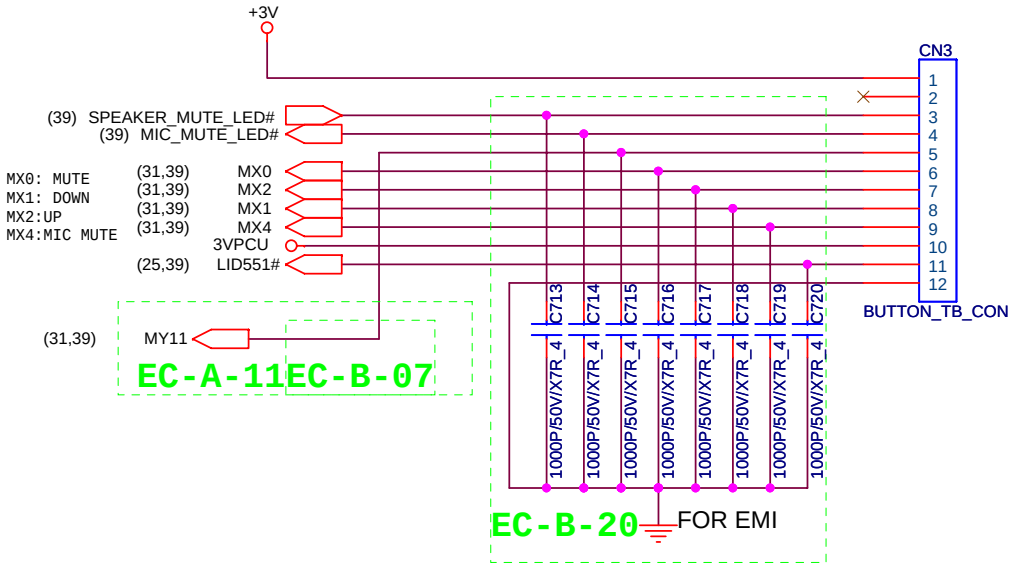


G-Note Montevina
Quanta Computer Inc.

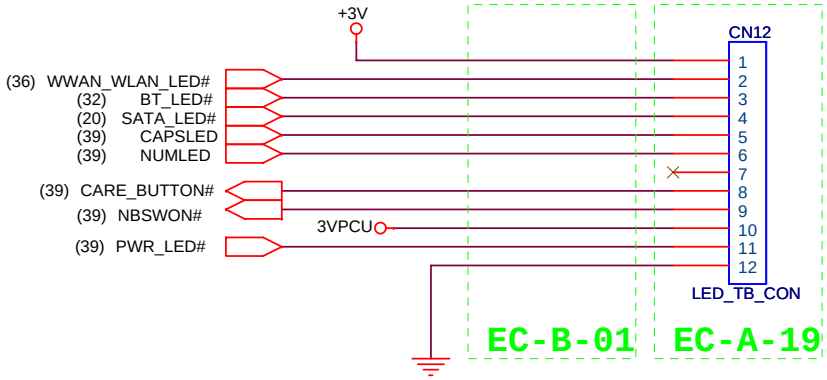
Size	Document Number	Rev
Custom	WLAN & WWAN Slot	2A
Date: Thursday, April 09, 2009	Sheet 36 of 55	

Daughter Boards for LEDs & Ports

FFC TO KBD LEFT SIDE CONNECTOR



FFC TO LED RIGHT SIDE CONNECTOR

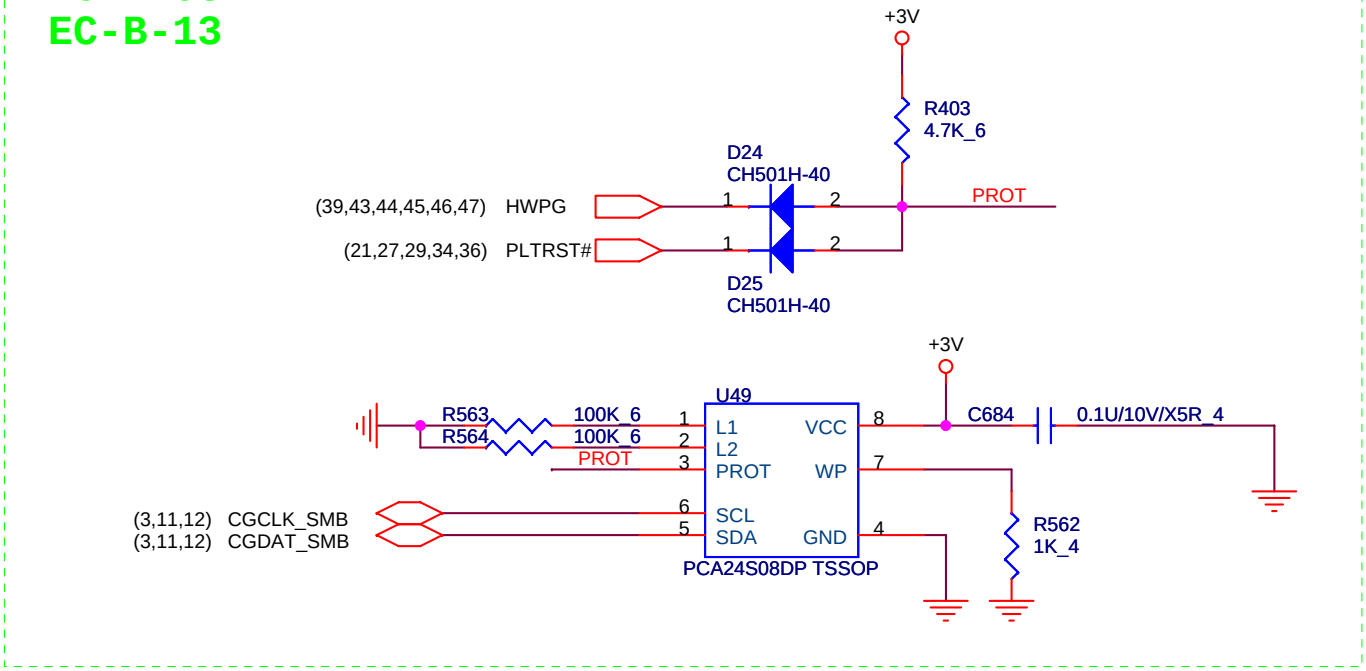


LOGO LED

EC-B-28

G-Note Montevina Quanta Computer Inc.		
Size: Custom	Document Number: Daughter Boards	Rev: 2A
Date: Thursday, April 09, 2009	Sheet 37 of 55	

EC-A-03
EC-B-13



G-Note Montevina
Quanta Computer Inc.

Size	Document Number	Rev
A	RFID EEPROM	2A

Date: Thursday, April 09, 2009 Sheet 38 of 55

IT8502E

(For PLL Power)

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

R609	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

GM/PM Board ID

POWER SWITCH/ CARE BUTTON

RF ON/OFF SWITCH

16Mbit (2M Byte), SPI

SST AKE28FP0K07
MX AKE37FP0Z13

MX25L1605A

Quanta Computer Inc.	G-Note Montevina
Size: Custom	Document Number: KBC IT8502E
Rev: 2A	
Date: Thursday, April 09, 2009	Sheet 39 of 55

3mm minicard nut

HOLE10 H-TC197BC142D102P2

HOLE12 H-TC197BC142D102P2

7mm minicard nut

HOLE26 H-TC236BC102D63P2

HOLE27 H-TC236BC102D63P2

PAD

GP1 *Spad-spe1np

GP2 *spad-c181np

GP3 *Spad-re197x216np

GP4 *H-TSHBC276I2_7D91P2-1

GND1

GP5 *SPAD-SPE3NP

Hole for CPU support

HOLE20 *H-C142D142N

HOLE21 *H-C142D142N

HOLE23 *H-C142D142N

HOLE24 *H-C142D142N

VGA nut

HOLE22 H-TC197BC158D122P2

THER_GND

HOLE25 H-TC197BC158D122P2

THER1_GND

Bluetooth nut

HOLE14 H-TC217BC154D118P2

Card reader board nut

HOLE28 h-tc189bc157d122p2

HOLE29 h-c189d122pt

HOLE2 *H-C276D91P2

HOLE5 *H-C276D91P2

HOLE6 *H-C276D91P2

HOLE9 *H-C276D91P2

HOLE15 *H-C276D91P2

HOLE16 *H-C276I107D91P2

GND1

HOLE17 *H-C276D91P2

HOLE18 *H-C276D91P2

HOLE31 *H-C276D91P2

HOLE8 *h-tshapebc276d91p2

HOLE1 *H-TC276BC216D91P2

HOLE4 *H-C91D91N

HOLE7 *H-C298D298N

HOLE3 *H-C79D79N

HOLE19 *H-C79D79N

HOLE30 *H-C98D98N

HOLE32 *h-tc236bc217d87p2

HOLE33 *h-tc236bc217d87p2

HOLE34 *spad-c323np

HOLE37 *spad-c276np

HOLE38 *H-C276D87P2

HOLE39 *H-C276D87P2

HOLE40 *spad-c276np

HOLE41 *spad-c276np

HOLE35 *H-C87D87N

HOLE43 *O-GC3-1

HOLE44 *O-GC3-2

HOLE45 *O-GC3-3

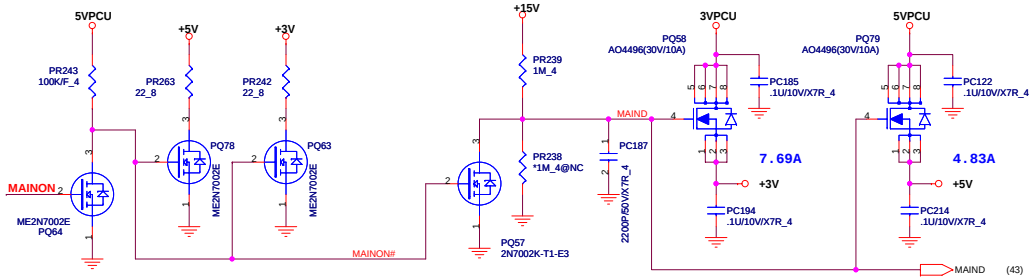
HOLE46 *O-GC3-4

G-Note Montevina
Quanta Computer Inc.

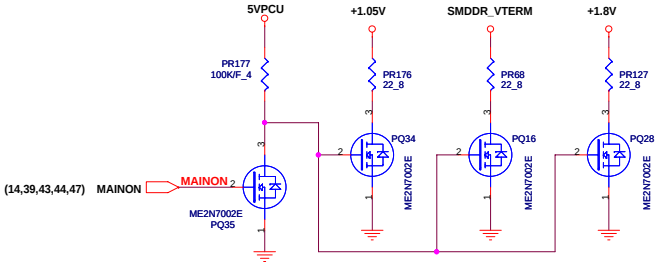
Size	Document Number	Rev
A	SCREW HOLE	2A
Date: Friday, April 03, 2009	Sheet 40 of 55	

DISCHARGE

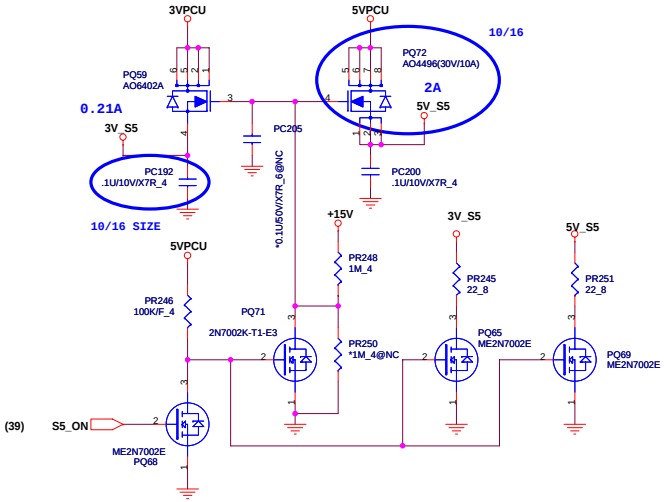
+3V, +5V



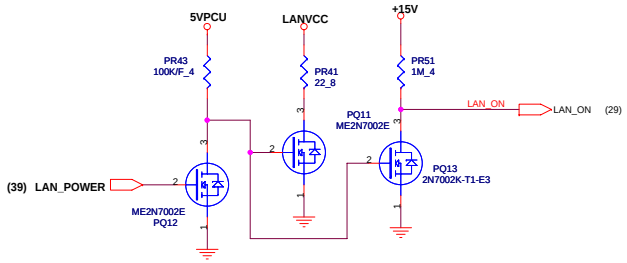
+1.8V, +1.05V, SMDDR_VTERM



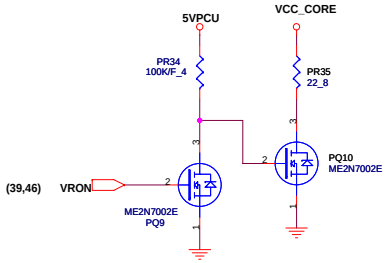
3V_S5, 5V_S5

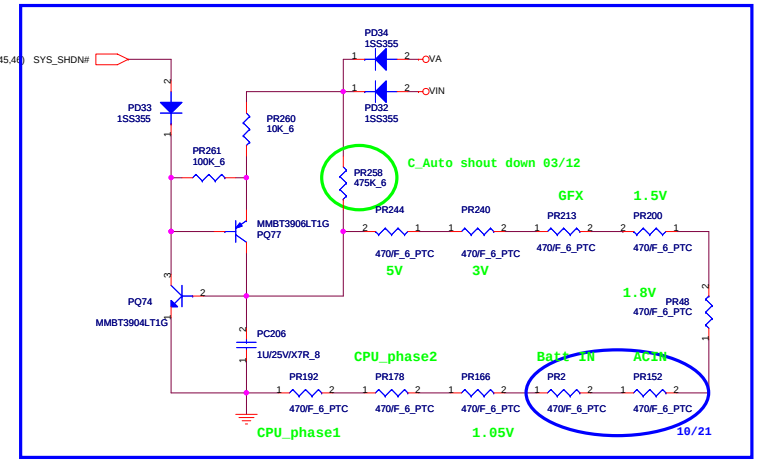


LANVCC

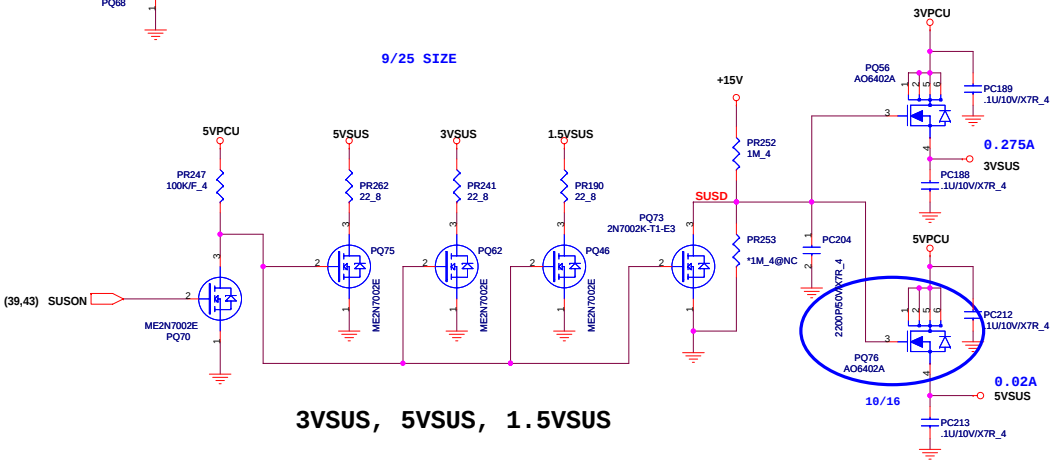


VCC_CORE



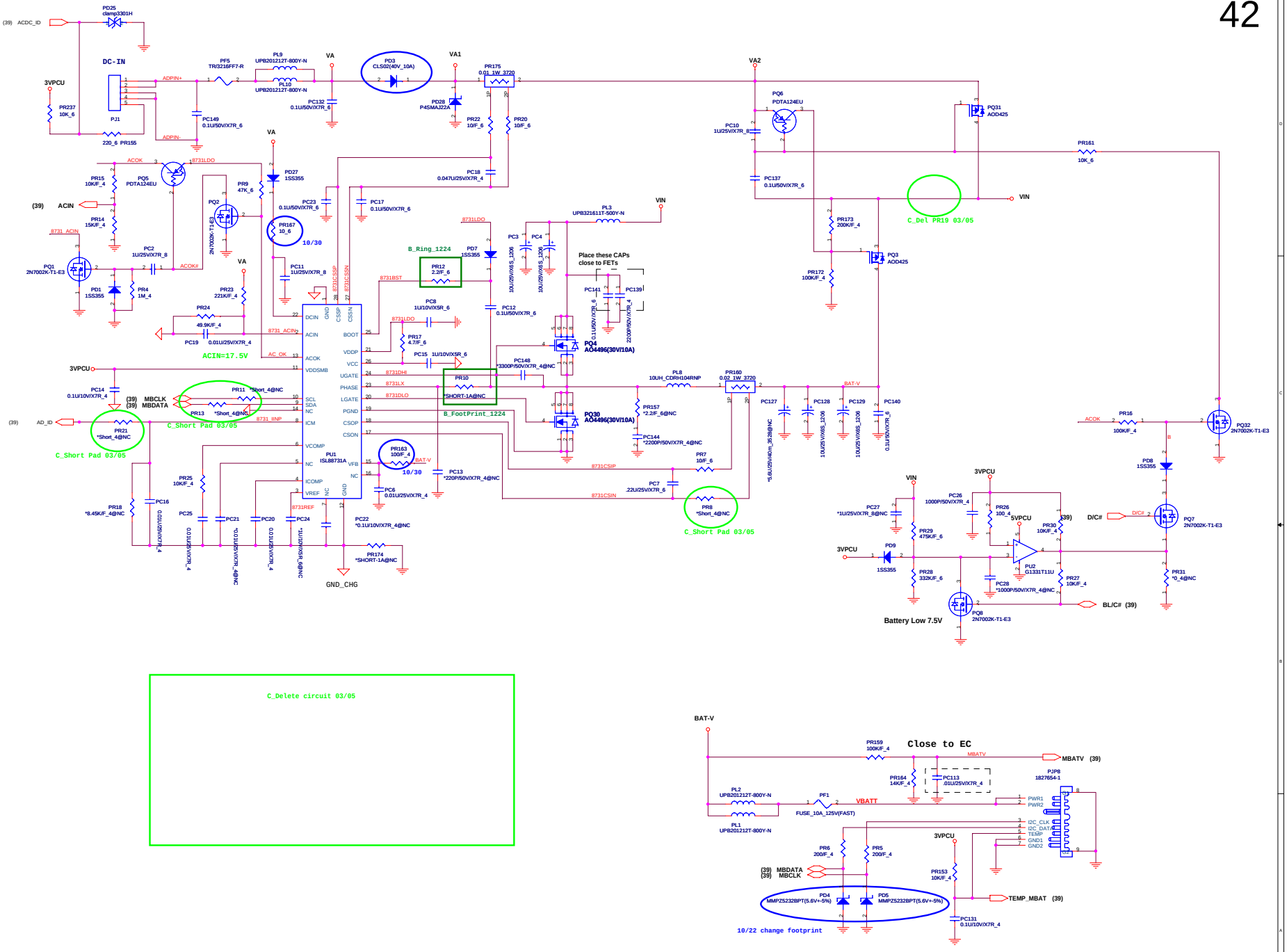


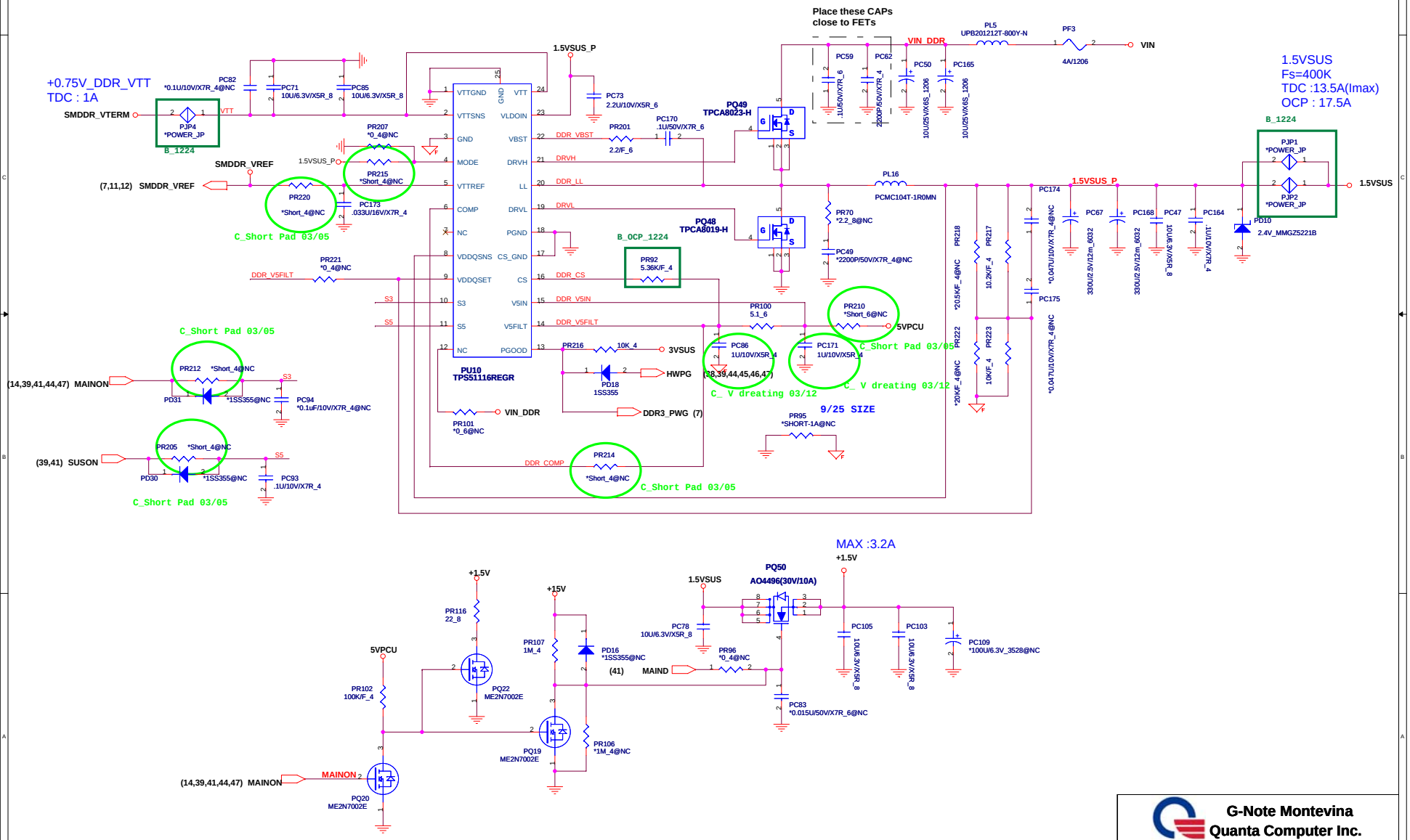
3VSUS, 5VSUS, 1.5VSUS

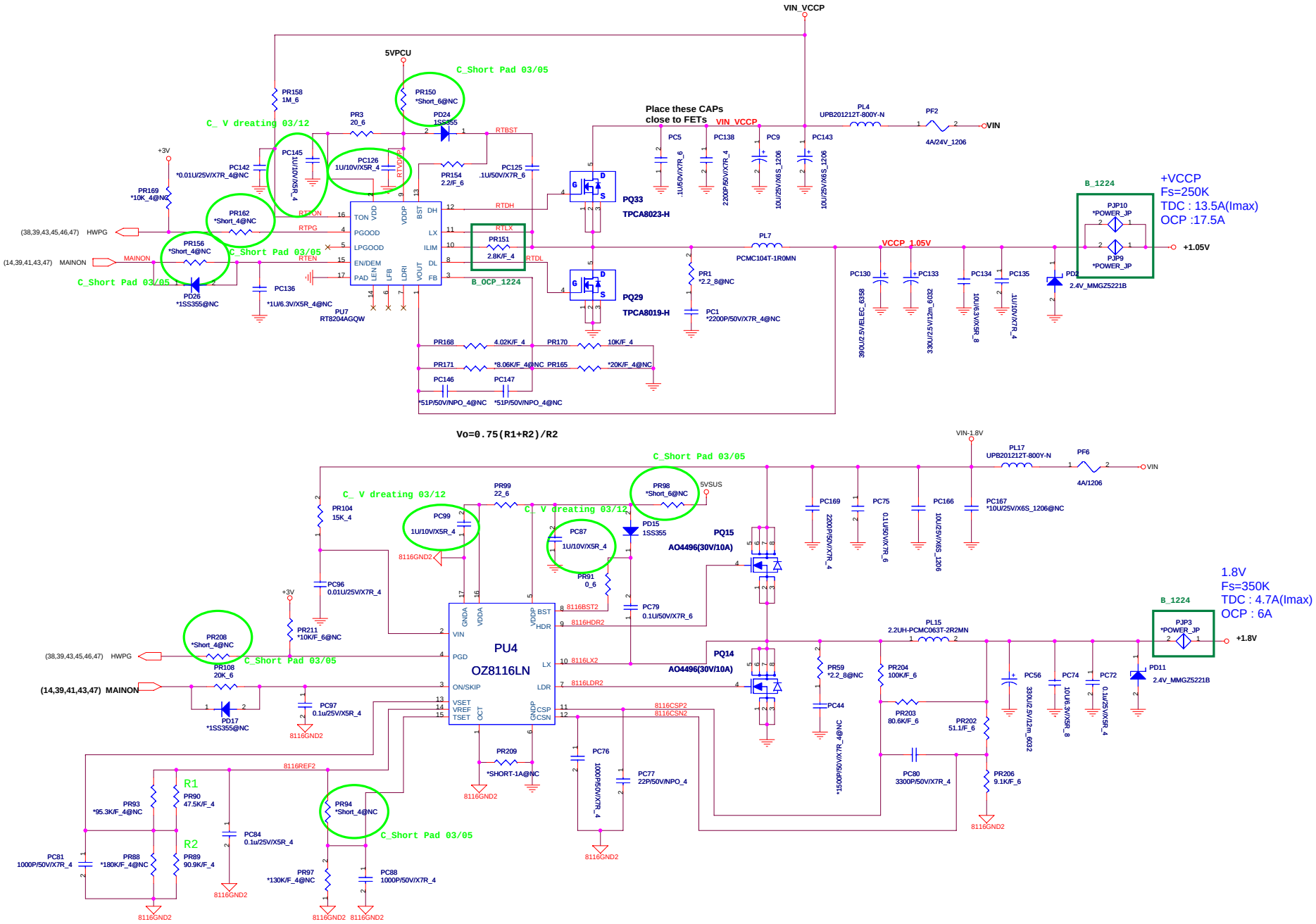


G-Note Montevina
Quanta Computer Inc.

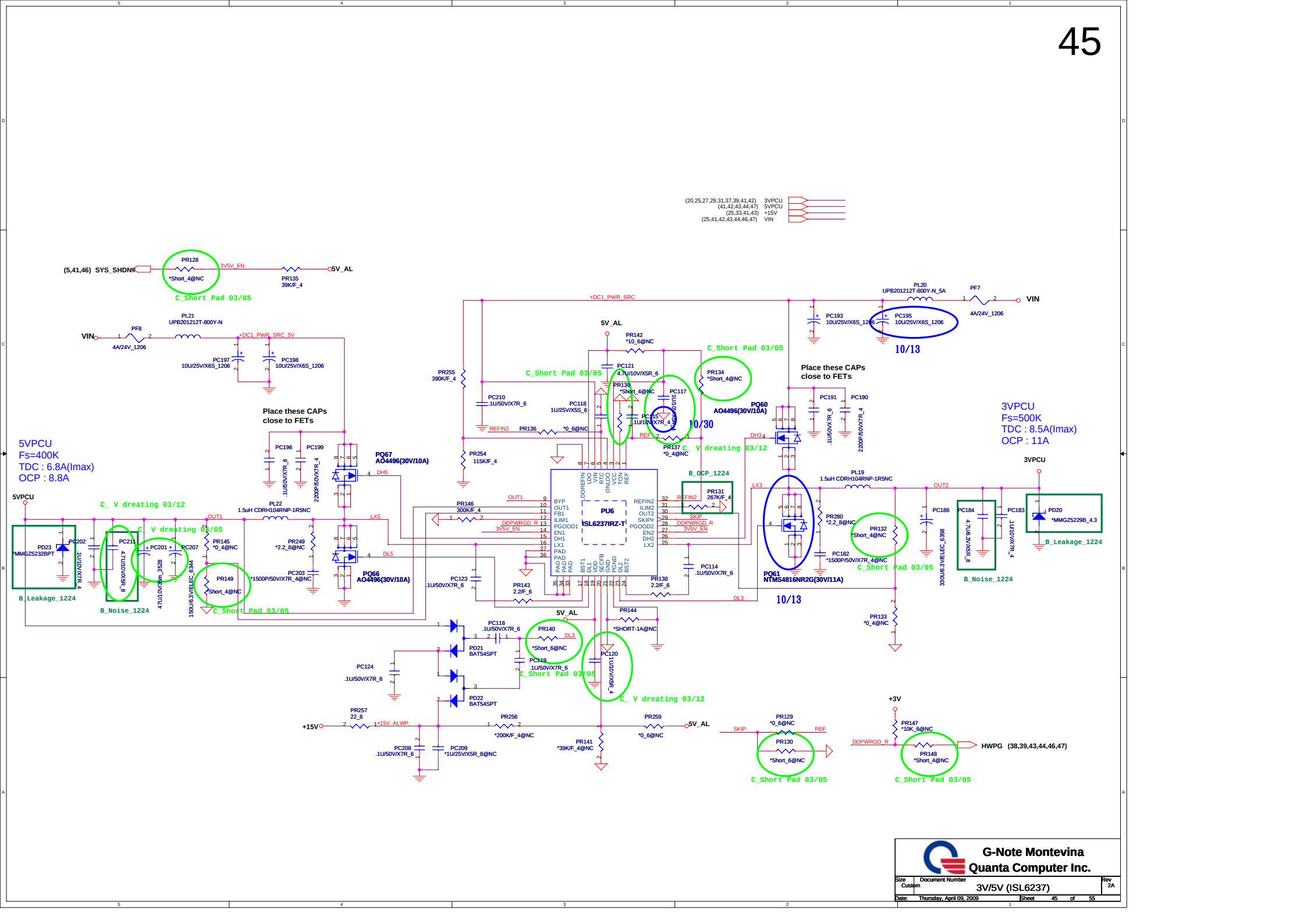
Size	Document Number	Rev
Custom	Discharge	2A
Date: Thursday, April 09, 2009	Sheet 41 of 55	


DC-IN
3VPCU
VA
VA1
VA2
VIN
ACIN
ACOK
8731LDO
B_Ring_1224
B_FootPrint_1224
Place these CAPs close to FETs
C_Del PR19 03/05
ACIN=17.5V
C_Short Pad 03/05
C_Short Pad 03/05
C_Short Pad 03/05
C_Delete circuit 03/05
Close to EC
Battery Low 7.5V
10/22 change footprint
GND_CHG
ISL88731A
PU1
PQ4 AO4496(30V/10A)
PQ30 AO4496(30V/10A)
PQ6 PDTA124EU
PQ5 PDTA124EU
PQ1 2N7002K-T1-E3
PQ2 2N7002K-T1-E3
PQ3 AOD425
PQ31 AOD425
PQ32 2N7002K-T1-E3
PQ7 2N7002K-T1-E3
PQ8 2N7002K-T1-E3
PD1 1SS355
PD27 1SS355
PD7 1SS355
PD8 1SS355
PD9 1SS355
PD3 CLS02(40V_10A)
PD28 P4SMAJ22A
PD4 MMPZ5232BPT(5.6V+-5%)
PD5 MMPZ5232BPT(5.6V+-5%)
PJ1
PJP8 1827654-1
PU2 G1331T11U
PF1 FUSE_10A_125V(FAST)
PF5 TR/3216FF7-R
PL1 UPB201212T-800Y-N
PL2 UPB201212T-800Y-N
PL3 UPB321611T-600Y-N
PL8 10UH_CDRH104RNP
PL9 UPB201212T-800Y-N
PL10 UPB201212T-800Y-N
PR10 *SHORT-1A@NC
PR174 *SHORT-1A@NC
PR175 0.01_1W_3720
PR160 0.02_1W_3720
PR11 *Short_4@NC
PR13 *Short_4@NC
PR21 *Short_4@NC
PR8 *Short_4@NC
PR237 10K_6
PR155 220_6
PR149 0.1U/50V/X7R_6
PR132 0.1U/50V/X7R_6
PR22 10/F_6
PR20 10/F_6
PR18 0.047U/25V/X7R_4
PR161 10K_6
PR173 200K/F_4
PR172 100K/F_4
PR167 10_6
PR15 10K/F_4
PR14 15K/F_4
PR9 47K_6
PR23 221K/F_4
PR24 49.9K/F_4
PR19 0.01U/25V/X7R_4
PR12 2.2/F_6
PR17 4.7/F_6
PR157 *2.2/F_6@NC
PR7 10/F_6
PR163 100/F_4
PR159 100K/F_4
PR164 14K/F_4
PR153 10K/F_4
PR6 200/F_4
PR5 200/F_4
PR16 100K/F_4
PR26 100_4
PR27 10K/F_4
PR28 332K/F_6
PR29 475K/F_6
PR30 10K/F_4
PR31 *0_4@NC
PC1 2U/25V/X7R_8
PC2 1U/25V/X7R_8
PC3 10U/25V/X6S_1206
PC4 10U/25V/X6S_1206
PC6 0.01U/25V/X7R_4
PC7 .22U/25V/X7R_6
PC8 1U/10V/X5R_6
PC10 1U/25V/X7R_8
PC11 1U/25V/X7R_8
PC12 0.1U/50V/X7R_6
PC13 *220P/50V/X7R_4@NC
PC14 0.1U/10V/X7R_4
PC15 1U/10V/X5R_6
PC16 0.01U/25V/X7R_4
PC17 0.1U/50V/X7R_6
PC18 0.047U/25V/X7R_4
PC20 0.01U/25V/X7R_4
PC21 *0.01U/25V/X7R_4@NC
PC22 *0.1U/10V/X7R_4@NC
PC23 0.1U/50V/X7R_6
PC24 *1U/10V/X5R_4@NC
PC25 0.01U/25V/X7R_4
PC26 1000P/50V/X7R_4
PC27 *1U/25V/X7R_8@NC
PC28 *1000P/50V/X7R_4@NC
PC113 .01U/25V/X7R_4
PC127 *5.6U/25V/Al/ch_6.3X6@NC
PC128 10U/25V/X6S_1206
PC129 10U/25V/X6S_1206
PC131 0.1U/10V/X7R_4
PC137 0.1U/50V/X7R_6
PC139 220P/50V/X7R_4
PC140 0.1U/50V/X7R_6
PC141 0.1U/50V/X7R_6
PC144 *2200P/50V/X7R_4@NC
PC148 *3300P/50V/X7R_4@NC
8731_ACIN
8731_BNP
8731REF
8731CSIP
8731CSIN
8731BST
8731DHI
8731LX
8731DLO
AC_OK
ADPIN+
ADPIN-
ACDC_ID
AD_ID
MBCLK
MBDATA
MBATV
VBATT
BAT-V
TEMP_MBAT
BLIC# (39)
D/C#
5VPCU
G-Note Montevina
Quanta Computer Inc.
Charger (ISL88731A)
Size: Custom
Document Number
Rev 2A
Date: Thursday, April 09, 2009
Sheet 42 of 55

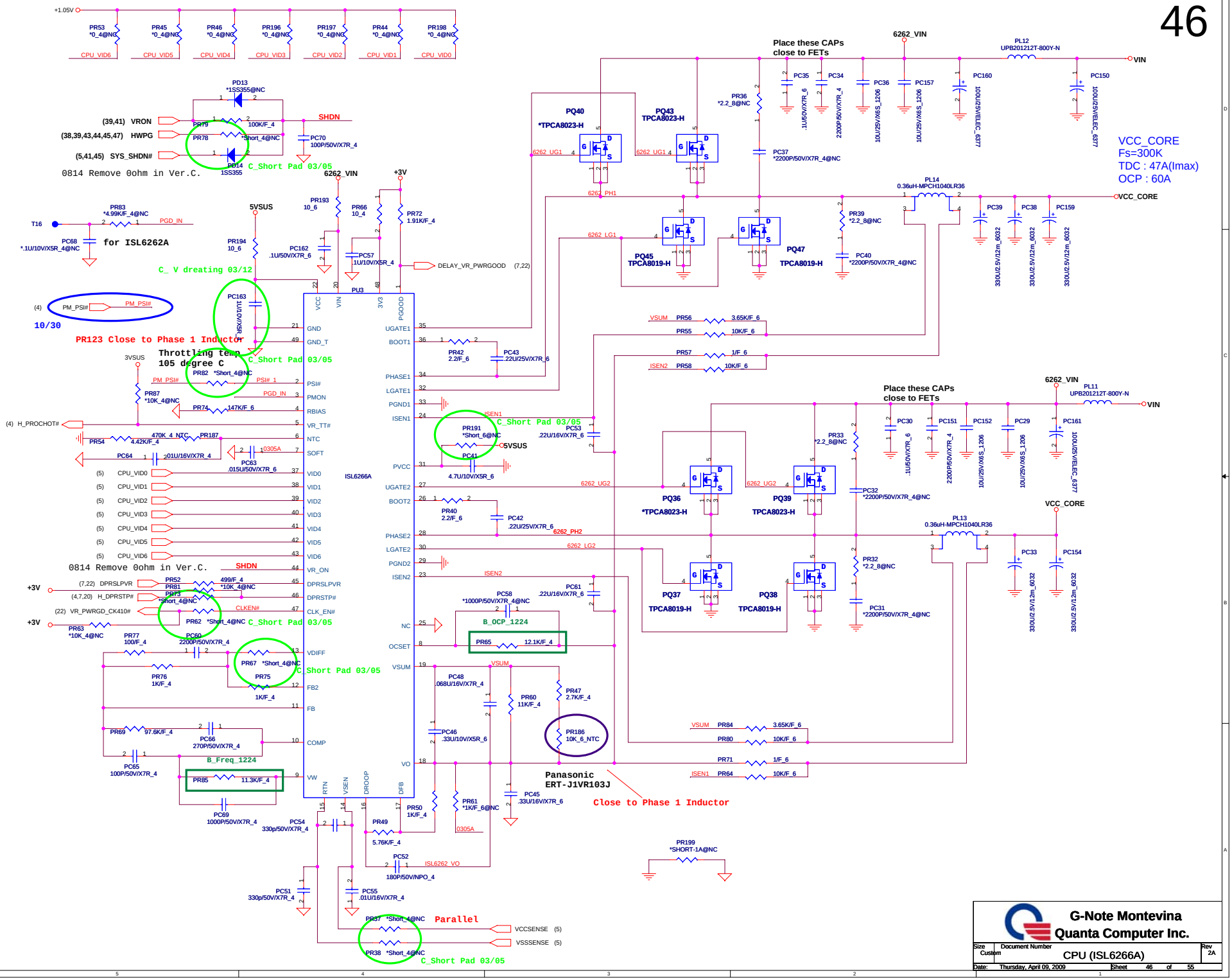

+0.75V_DDR_VTT
TDC : 1A
SMDDR_VTERM
SMDDR_VREF
(7,11,12) SMDDR_VREF
1.5VSUS_P
Place these CAPs close to FETs
VIN_DDR
VIN
4A/1206
1.5VSUS
Fs=400K
TDC :13.5A(Imax)
OCP : 17.5A
PU10 TPS51116REGR
PQ49 TPCA8023-H
PQ48 TPCA8019-H
PL5 UPB201212T-800Y-N
PL16 PCMC104T-1R0MN
PD10 2.4V_MMGZ5221B
C_Short Pad 03/05
B_1224
B_OCP_1224
(14,39,41,44,47) MAINON
(39,41) SUSON
(38,39,44,45,46,47)
3VSUS
HWPG
DDR3_PWG (7)
C_ V dreating 03/12
9/25 SIZE
MAX :3.2A
5VPCU
+1.5V
+15V
PQ50 AO4496(30V/10A)
PQ22 ME2N7002E
PQ19 ME2N7002E
PQ20 ME2N7002E
(41) MAIND
MAINON
G-Note Montevina
Quanta Computer Inc.
DDR3 (TPS51116REGR)
Thursday, April 09, 2009
Sheet 43 of 55



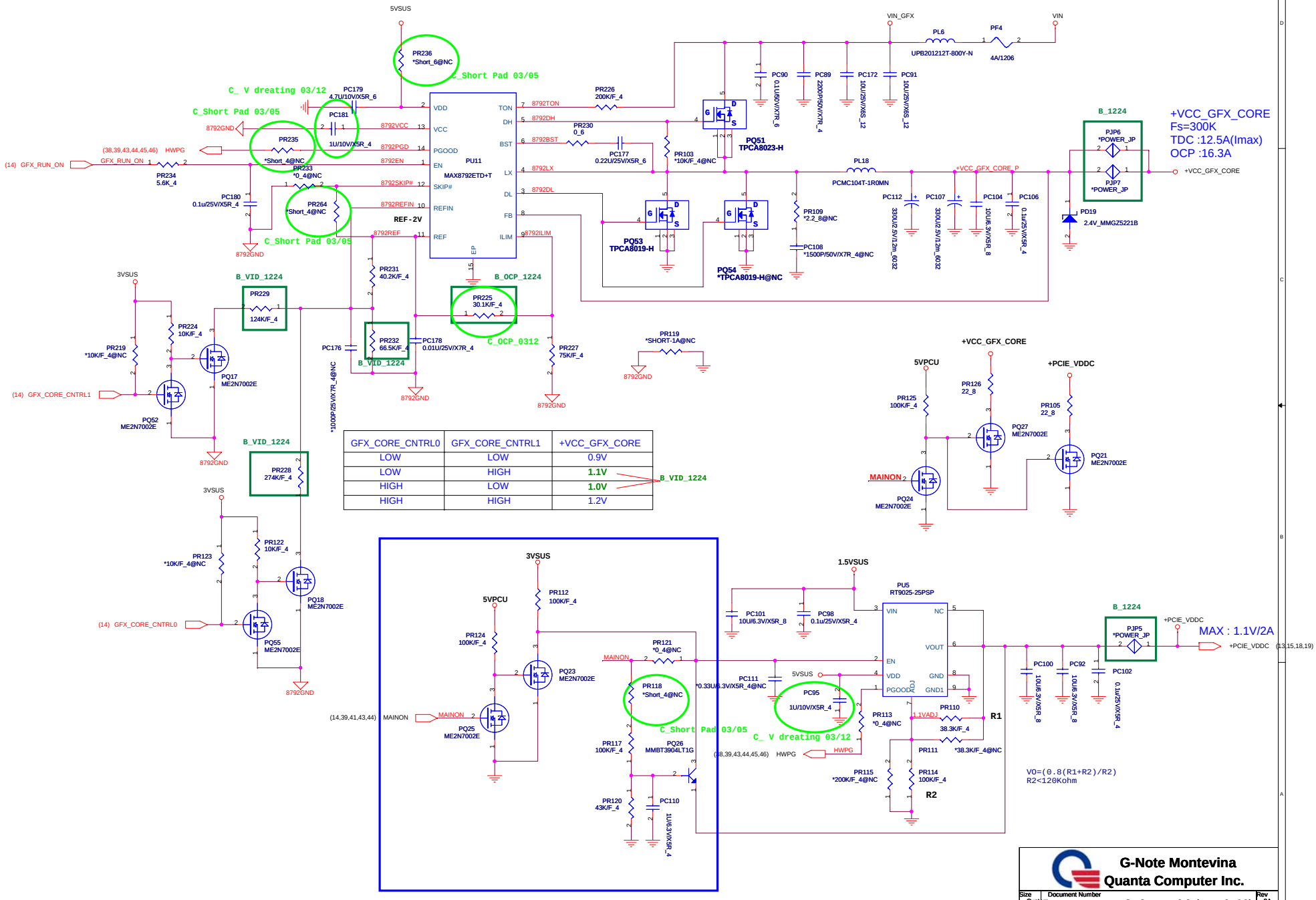
Quanta Computer Inc.	G-Note Montevina	
Size: Custom	Document Number: 1.0V / 1.8V (RT8204)	Rev: 2A
Date: Thursday, April 09, 2009	Sheet 44 of 55	



G-Note Montevina	
Quanta Computer Inc.	
Size: Custom	Document Number: 3V/5V (ISL6237)
Rev: 2A	
Date: Thursday, April 09, 2009	Sheet 45 of 55



Company	G-Note Montevina Quanta Computer Inc.
Size	Custom
Document Number	CPU (ISL6266A)
Rev	2A
Date:	Thursday, April 09, 2009
Sheet	46 of 55



GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
LOW	HIGH	1.1V
HIGH	LOW	1.0V
HIGH	HIGH	1.2V

B_VID_1224

Quanta Computer Inc.	G-Note Montevina
Size: Custom	Document Number: DIS_GFX_VCC (MAX8792)
Rev: 2A	
Date: Thursday, April 09, 2009	Sheet 47 of 55

Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
1A		DV	Initial release		

Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP

CAPACITOR

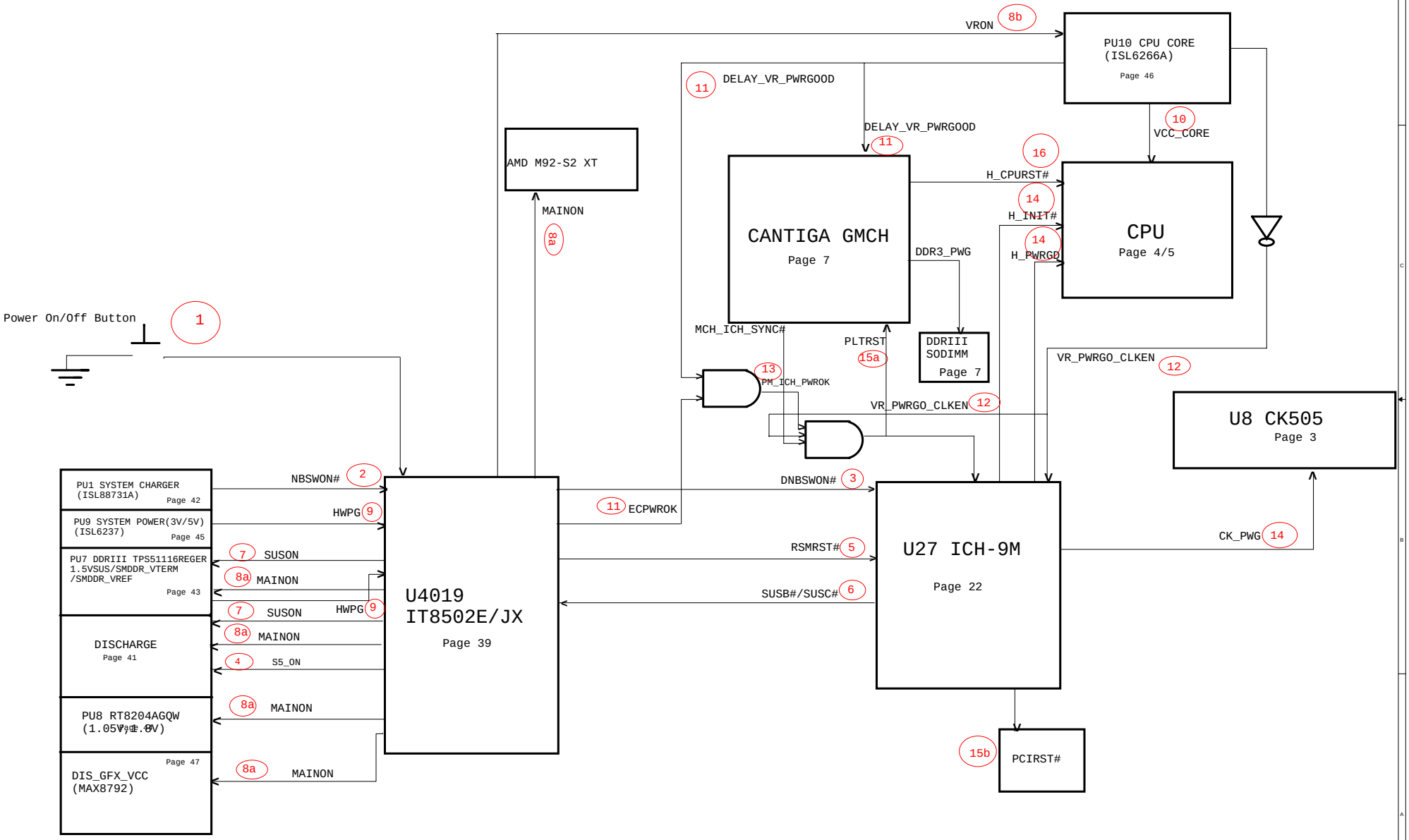
Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

G NOTE SKU TABLE

Location					

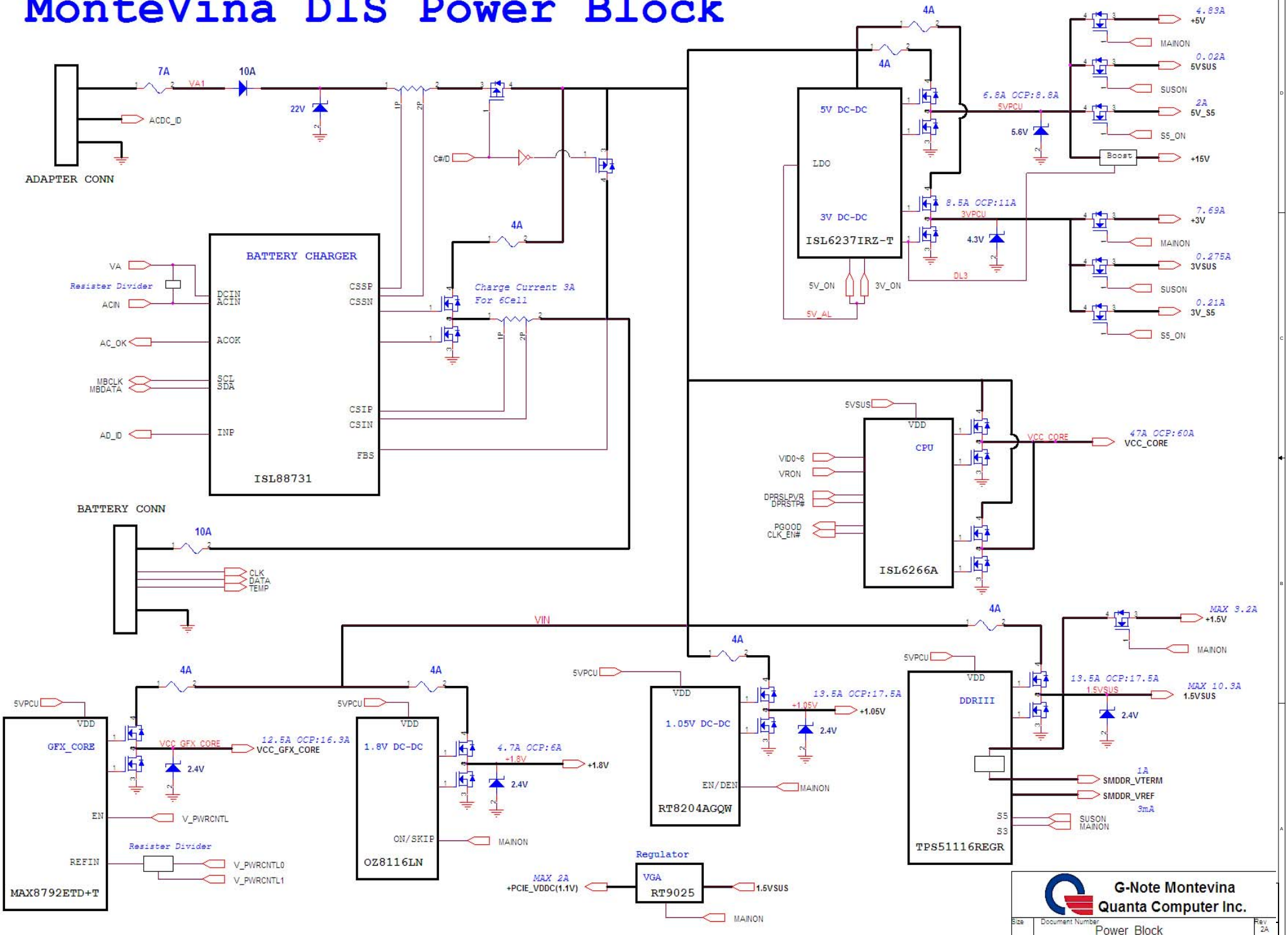
G NOTE SKU TABLE

Location					Page



G-Note Montevina Quanta Computer Inc.			
Size	Document Number		Rev
	Power Sequence Block		2A
Date: Tuesday, March 03, 2009		Sheet 50 of 55	

MonteVina DIS Power Block



G-Note Montevina Quanta Computer Inc.			
Size	Document Number Power Block		Rev 2A
Date: Tuesday, January 20, 2009		Sheet 51 of 52	

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-01	42	12/24	PR10	Change Footprint
EC-A-02	42	12/24	PR12	Change to 2.2 ohm reduce phase ring
EC-A-03	42	12/24	PD6	Delete Footprint
EC-A-04	43	12/24	PJP1,PJP2,PJP4	Change Footprint
EC-A-05	43	12/24	PR92	Change to 5.36K for OCP
EC-A-06	44	12/24	PR151	Change to 2.8K for OCP
EC-A-07	44	12/24	PJP3,PJP9,PJP10	Change Footprint
EC-A-08	45	12/24	PR131	Change to 267K for OCP
EC-A-09	45	12/24	PC134,PC211	Change to 4.7u reduce H.F. noise reduce
EC-A-10	45	12/24	PD20,PD23	NA to reduce leakage current
EC-A-11	46	12/24	PR65	Change to 12.1K for OCP
EC-A-12	46	12/24	PR85	Change to 11.3K for frequency 300KHz
EC-A-13	47	12/24	PJP5,PJP6,PJP7	Change Footprint
EC-A-14	47	12/24	PR225	Change to 80.6K for OCP
EC-A-15	47	12/24	PR228,PR229,PR232	Change for VID point setting

	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
2008	EC-A-01	29	12/08	U10	Change LAN IC footprint from (LQFP48-9X9-4)0.4 to (LQFP48-9X9-5)0.5 pitch
	EC-A-02	28	12/08	U32	Change Codec IC footprint to qfn48-7x7-5-58p-0_9h.(Add 9 via at the center PAD of original IC footprint)
	EC-A-03	38	12/08	U49	Change U49 schematic by adding R562,R563,R564 and D24 to solve F4 error code issue.
	EC-A-04	25	12/08	R196	Delete CCD_ON which was use to control CAM_VCC by change R196 from depop to pop and delete U16,C353,R204,R211,R219,R221.
	EC-A-05	14	12/08	R399	Add R399 to pull low CPIO_19_CTF according to AMD FAE suggestion.
	EC-A-06	22	12/08	R347	Replace CCD_ON with HDD_DETECT#, original HDD_DETECT# will cause FF error code while attached HDD.
	EC-A-07	03	12/08	R313	Change to 4.7Kohm To solve N.B. cannot get correct FSB frequency selection (error coed 02)
	EC-A-08	36	12/08	CN11	Add CLKRUN#,SERIRQ,LPC_LDRQ0#,LPC_PD#
	EC-A-09	39	12/08	R565,R566	Add adapter selection board ID by adding R565 an R566.
	EC-A-10	25	12/08	Q13	Change Q13 connection.
	EC-A-11	37	12/08	R567,R568	Add optional resistor between MY11 and MY13
	EC-A-12	28	12/11	C465,C426,C427, C506,C507,C499, C495,C497,C455	Change footprint from 0805 to 0603 per mechanical request.
	EC-A-13	25	12/19	CN5	Connect LCD connector shielding to GND for better EMI performance.
	EC-A-14	36	12/23	C679,Q35,Q36A, Q36B,R506,R510, R511,R519,R521	Delete redundunt schematic to save space for layout.
	EC-A-15	05	12/23	C708,C709,Q38, Q39,Q40,R569, R570,R571,R572, R573,R574,U53	Change thermal sensor.
	EC-A-16	29	12/23	R579,R580	Add IO_GND1 for LAN connector per EMI request.
	EC-A-17	26	12/24	R581,R582,R583, Q41,Q42	Change HP_DET schematic for better ESD protection and prevent floating
	EC-A-18	28	12/30	U54,D26,D27, C710	Add new schematic to prevent "POP' sound.
	EC-A-19	37	12/30	CN12	Add CN12 for 14" PCB due to mechanical design limit.
2009	EC-A-20	27	01/07	CN27	Change pin define of CN27 by intercept GND pin between differential pair per EMI request.

A stage

B stage

	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
2009	EC-B-01	37	02/24	CN2	Delete CN2(extra right button/b connector)
	EC-B-02	30	02/24	CN19	Delete CN23 (extra ODD connector)
	EC-B-03	29	02/24	CN20	Swap PIN3 and PIN14 to correct the LED behavior.
	EC-B-04	3 21 35	02/26	C664,C665,C667, C672,C685,CN9, R488,R489,R491, R492,R494,R496, R515,U46,C324, C325,RP4,R293	Delete one minicard slot per customer request.
	EC-B-05	30	02/26	CN4	Reverse the pin define of KB connector for the conveninece of assembly.
	EC-B-06	33	02/26	R584	Insert 10 ohm resister(10_6) between FET and VDD(G-sensor) for Analog noise reduction.
	EC-B-07	03 10 13 14 17 22 23 24 25 27 28 29 30 31 32 36 39	02/27	C403,L2,L56,R322, R105,R113,R127,R131, R133,R142,R143,R151, R159,R16,R160,R167, R180,R186,R579,R261, R269,R329,R339,R355, R356,R214,R22,R252, R255,R267,R550,R278, R282,R284,R286,R294, R312,R314,R33,R332, R338,R340,R547,R351, R353,R354,R367,R377, R401,R402,R405,R415, R429,R435,R436,R454, R493,R502,R505,R514, R518,R522,R567,R568 R525,R529,R531,R534, R537,R580,R543,R545, R546,R9,R38,R65,RP3, RP4,RP5,RP6,RP7, R569,R48,R362,R92, R119,R32,R36,R444, R447,R485R162,R163, R189,R192,R200,R206, R216,R227,R237,R244, R548,R549,R551,R552, R553,R554,R60,R101, R102,R364,R201,R207	Delete redundant 0 ohm or change it to short pad in the circuit.

2009

B stage

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-B-08	31	03/03	R486,R487	Add but no assembly
EC-B-09	34	03/03	C501	Add
EC-B-10	34	03/03	R585,R586	Disconnect SMB and change it to pull high 10K to 3VAUX
EC-B-11	36	03/03	R523,R524	Change to 4.7K and pull high to 3VWLAN
EC-B-12	36	03/03	R526,R528	Change to 4.7K and pull high to 3VWWAN
EC-B-13	38	03/03	C684,D24,D25, R403,R562,R563, R564,U49	Change RFID IC package to TSSOP.
EC-B-14	28	03/04	C711,C712	Reserve 1u capacitor between L+,L- and R+,R- for EMI
EC-B-15	22	03/04	R223,R224, R239,R250	Change board ID for SIT stage.
EC-B-17	28	03/06	R272,R273,R274, R275	Add R272,R273,R274,R275 for EMI
EC-B-18	26	03/06	D21	
EC-B-19	25 32	03/12	F3,F4,F5	
EC-B-20	37	03/09	C713,C714,C715, C716,C717,C718, C719,C720	Add capacitor for EMI
EC-B-21	03	03/09	R357,R323,R279	Due cpu clock already fix,so delete redundant parts.
EC-B-22	31	03/10	R587,R588,R589, R590,R591,R592	Add EMI filter for RF
EC-B-23	44	03/16	PD17	Assembly PD17 to correct VGA graphic power off sequence.
EC-B-24	25	03/12	R593,C311,C312	Add bead for EMI
EC-B-26	24	03/17	D14,D15,D16, D17,D18,D19, D20	Change CRT ESD protection from Switching Diode to Transient Voltage Suppressors.
EC-B-27	22,39	03/30	R347	Change HDD_DETECT# connection from ICH9 to KBC
EC-B-28	25,37 39	04/07	Q17,Q19,R169, R174,R175	Delete LOGO Led for cost down
EC-B-29	25 39	04/07	R541,C309,Q13, Q14,R165,R166	Delete THINK light for cost down
EC-B-30	27	04/08	R555,R556,R557	Fine tune battery and suspend LED brightness
EC-B-31	29	04/10	U11,U15	Replace TVS between transformer and LAN IC for Hi-pot test

G-Note Montevina
Quanta Computer Inc.

Size	Document Number	Rev
B	EC list	2A

Date: Thursday, April 09, 2009 Sheet 55 of 55