KL5A Intel Huron River Platform with Discrete GFX

01

FAN / THERMAL
EMC2103-2

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DDRIII-SODIMM2
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Dual Channel DDR3
800/1067/1333 1.5V

DDR SYSTEM MEMORY

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SandyBridge 0.61
rPGA 988
PCI-E
FDI DMI
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Graphics Interfaces

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nVIDIA
N12M-GS 533p
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1.5VSUS, 0.75VSMDDR_VTERM,1.5V
1.5V_GPU,1.5V_CPU

REGULATOR
+1.05V_VTT,+1.8V

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3VPCU, 5VPCU, +15V
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VGA Core Discrete
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FDI DMI

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AUDIO CODEC
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	22,33,35,36,37,39,40,41,42	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	07,08,11,12,32	RTC		S0~S5
+3VPCU	+3.3V	07,08,22,23,25,30,31,32,34,35,37,38	ITE8052 POWER	3V5V_EN	S0~S5
+5VPCU	+5V	25,34,35,36,37,38,39,40,41	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	22,25,27,34,36,37,38,41	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	23,34	LAN POWER	LAN_ON	
+5V_S5	+5V	11,22,25,27,28,34	PCH SUS POWER	S5_ON	S0~S3
+3V_S5	+3.3V	03,07,08,09,10,11,27,28,31,32,34	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0~S3
GFX_CORE	+0.9V~+1.2V	15,34,39	VGA CORE POWER	MAINON	S0
+0.75V_DDR_VTT	+0.75V	5,14,32	DDR3 SODIMM REFERENCE POWER	SYS_PWROK	S0
+5V	+5V	07,08,11,20,21,24,25,29,30,31,32,34,35,42	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	07,08,09,10,11,13,14,15,20,21,22,23,24,25,26,27,28,29,31,32,34,35,39,40,41,42	SLP_S3# CTRLD POWER	MAINON	S0
+1.8V	+1.8V	05,08,11,34,38	LVDS,NVM POWER	MAINON	S0
+1.5V	+1.5V	11,25,27,34	Mini PCIe,Express Card POWER	MAINON	S0
+1.05V_PCH	+1.05V	03,05,07,08,09,11,34,36,41	PCH CORE POWER	MAINON	S0
+VCC_CORE		05,34,42	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	22	LCD Power	INT_LVDS_VDDEN	S0
BAT-V	+10V~+17V	35	MAIN BATTERY	CHG_PBATT	S0~S5

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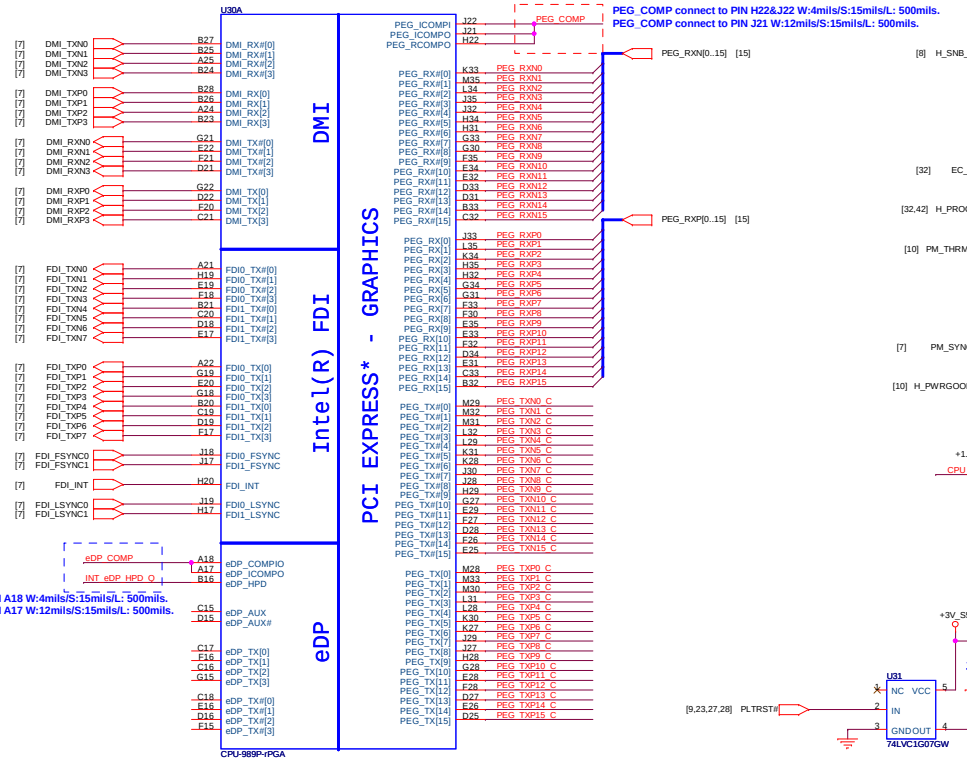
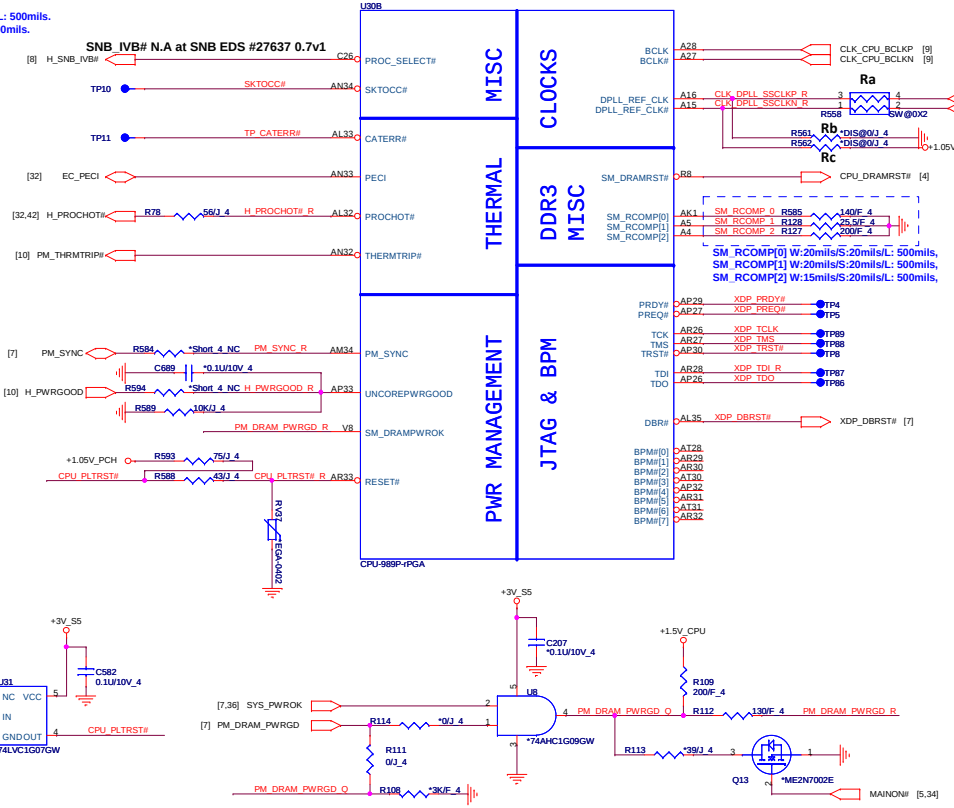
Sandy Bridge Processor (DMI,PEG,FDI)



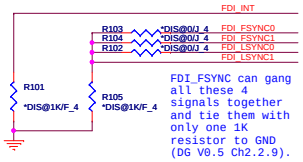
Sandy Bridge Processor (CLK,MISC,JTAG)



	DIS only	SW/UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

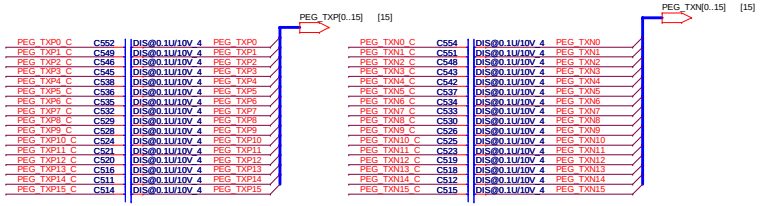
03

FDI Disable

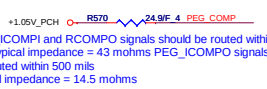


FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 (UMA Non-stuff)



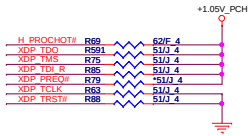
DP & PEG Compensation



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)



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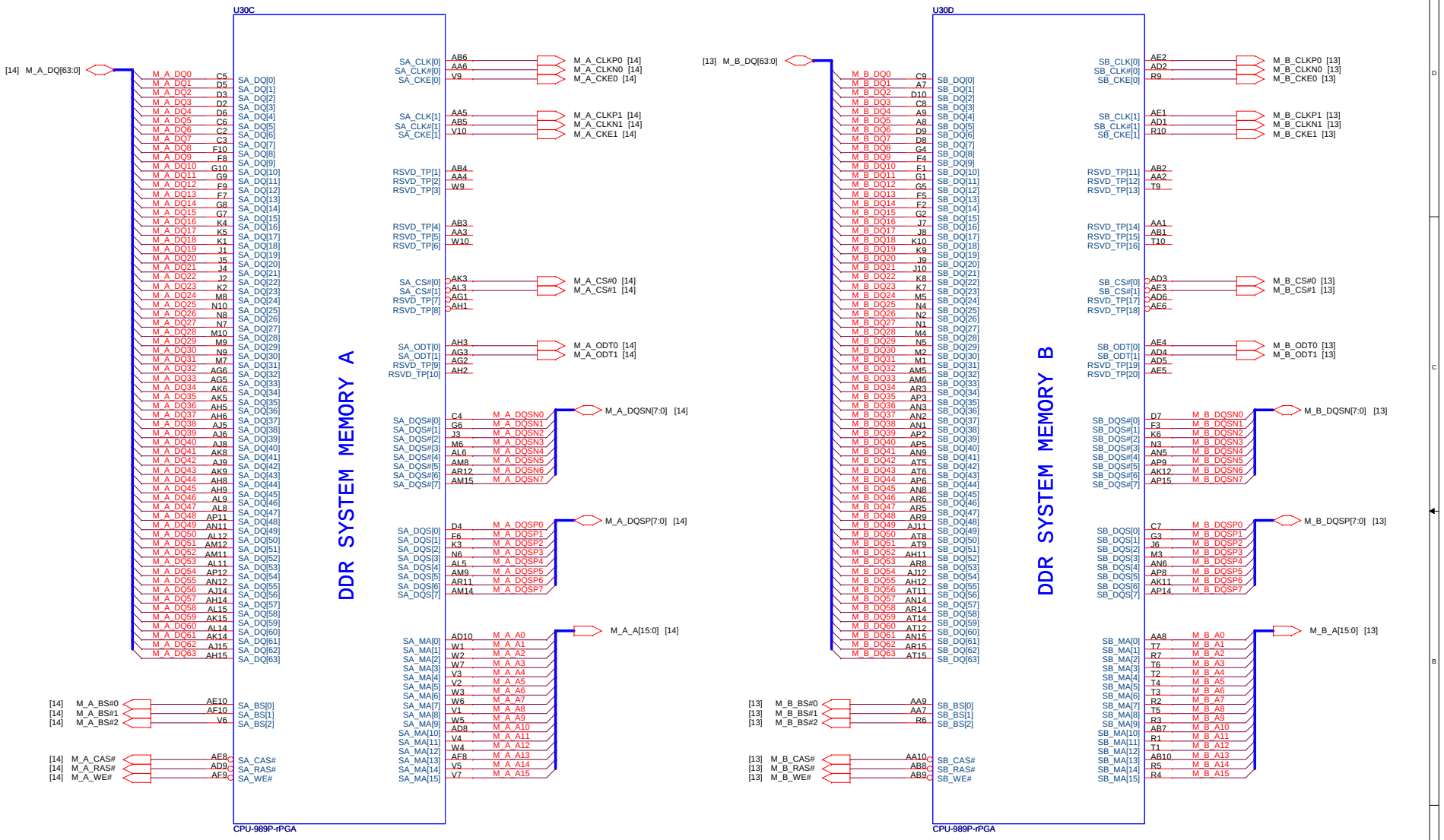
Sandy Bridge Processor (DDR3)



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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power

SNB 45W:55A,36A(TDP)

22uF x 32

22uF x 3 (Non-stuff)

CPU VTT

SNB 45W:8.5A

22uF x 10

22uF x 6 (Non-stuff)

CPU VGT

SNB 45W:24A

22uF x 12

22uF x 4 (Reserved)

CPU VCCPL

SNB 45W:1.2A

330uF/7mohm x 1

10uF x 1

1uF x 2

CPU MCH

SNB 45W: 10A

330uF/6mohm x 1

10uF x 6

CPU SA

SNB 45W: 6A

330uF/7mohm x 1

10uF x 3

Reserved

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK — Close to VR

SVID DATA — Close to VR

SVID ALERT

Place PU resistor close to CPU

4.5A

3/26 DB add for Intel. Placement close to CPU.

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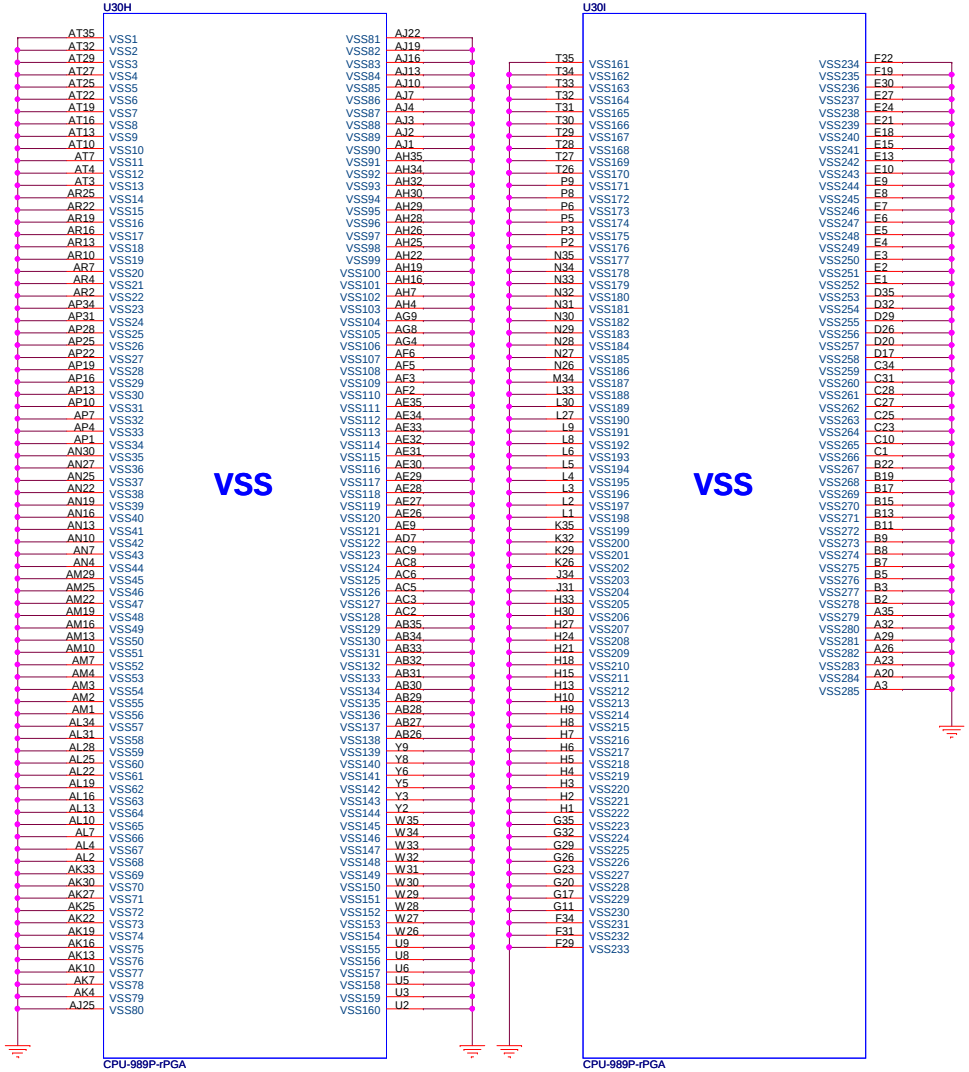
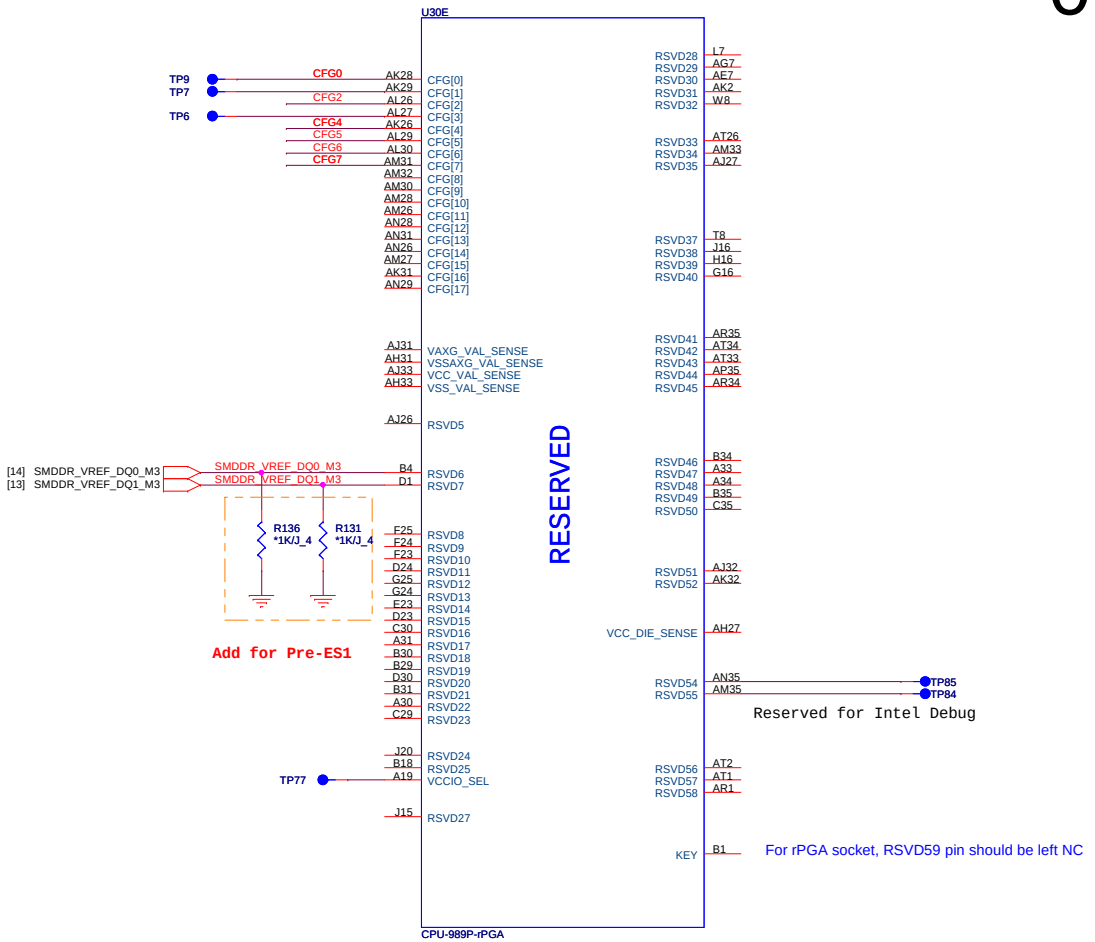
Sandy Bridge Processor (GND)



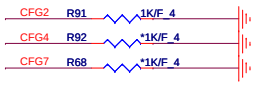
Sandy Bridge Processor (RESERVED, CFG)

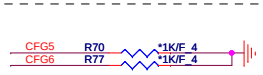


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training





CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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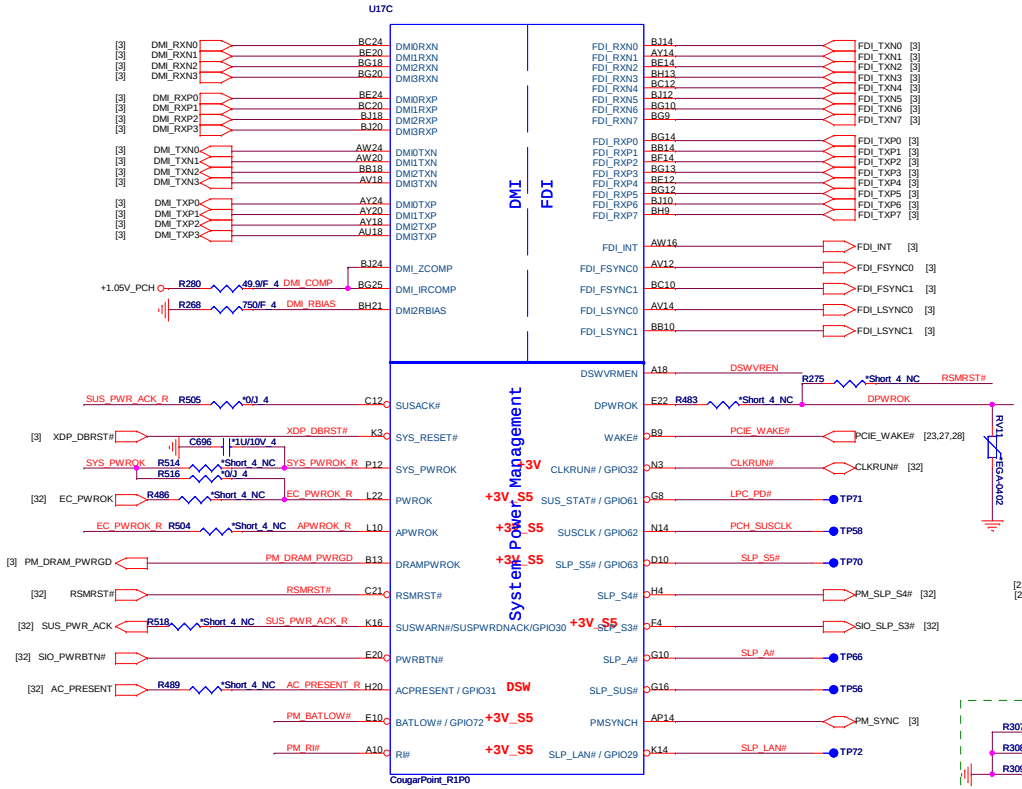
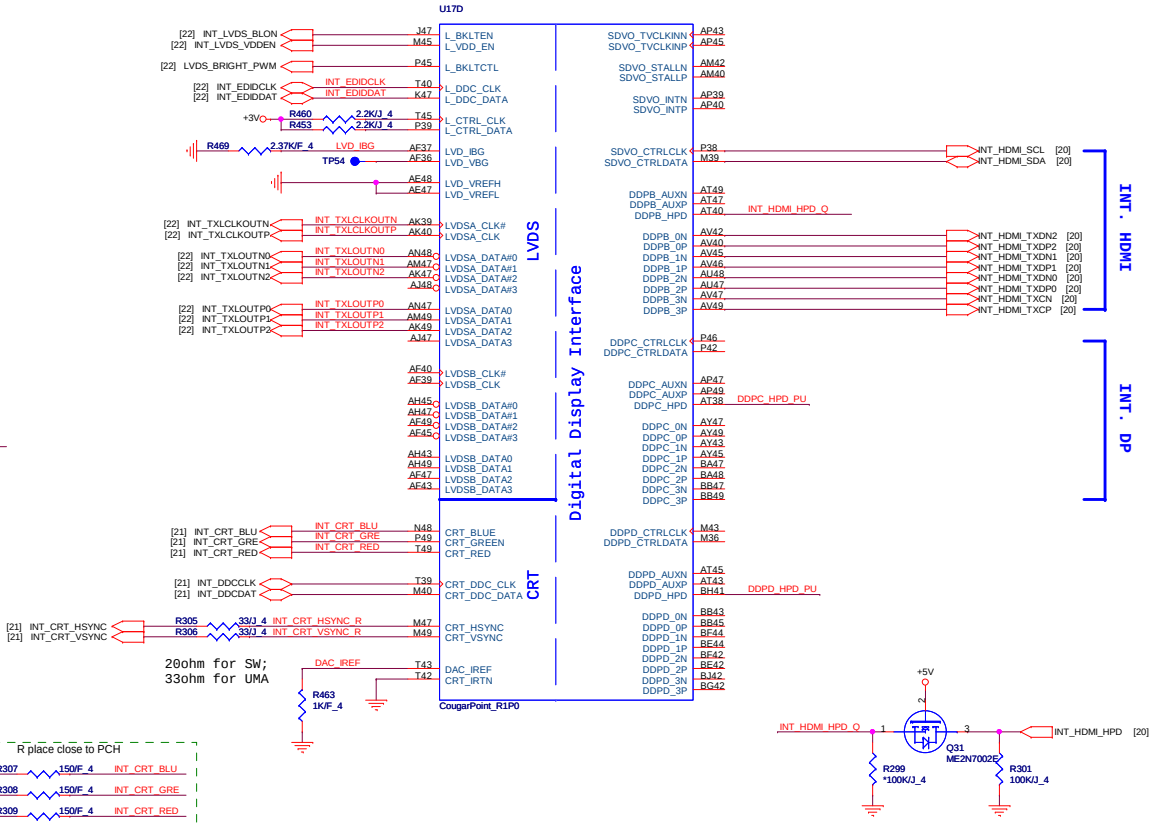
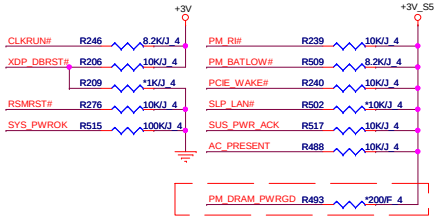
Cougar Point (DMI,FDI,PM)



Cougar Point (LVDS,DDI)

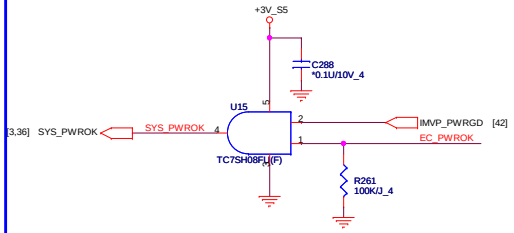


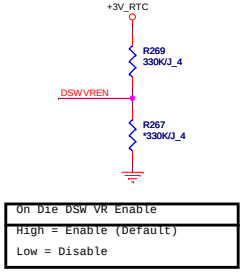
PCH Pull-high/low(CLG)



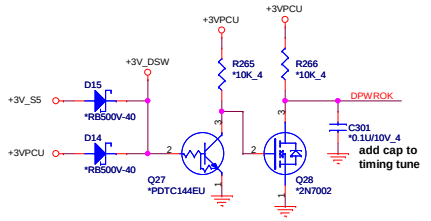
3/16 Change topology; 200ohm PU to +3V_S5

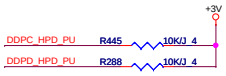
System PWR_OK(CLG)





DPWROK FOR DSW





Follow PDG eDP disable guide

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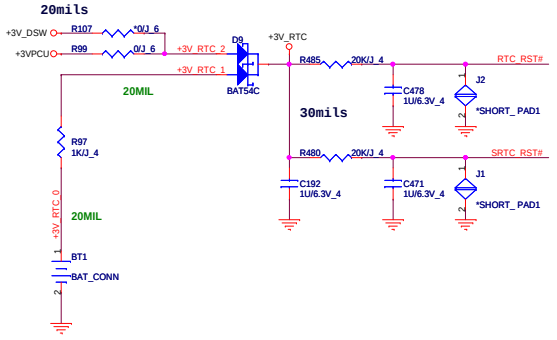
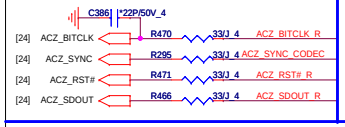
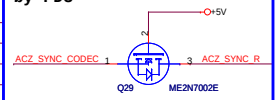
RTC Circuitry(RTC)



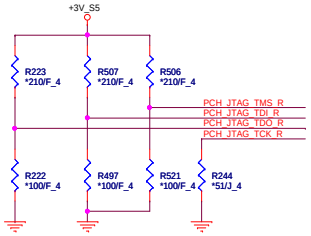
HDA Bus(CLG)



To Separate Codec Sync by PD3

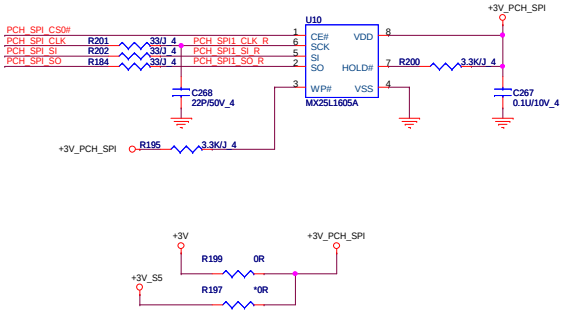


PCH JTAG Debug (CLG)



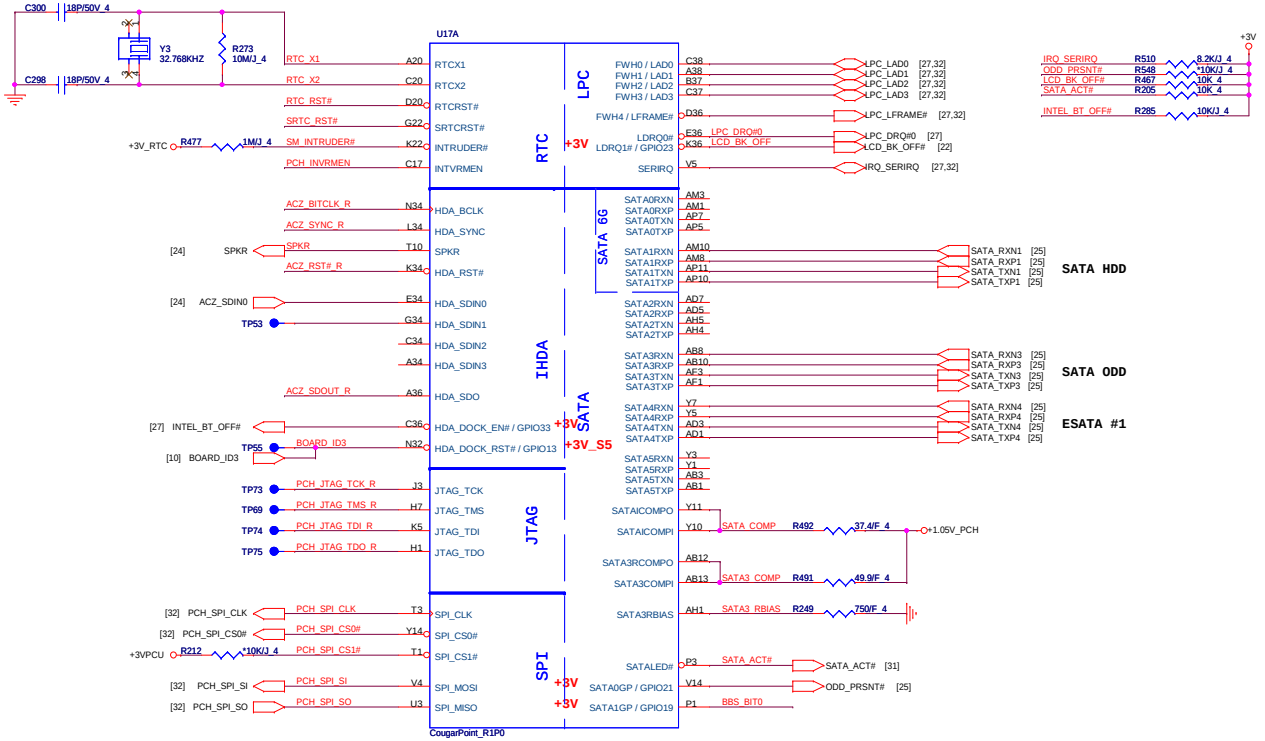
PCH Dual SPI (CLG)

MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031



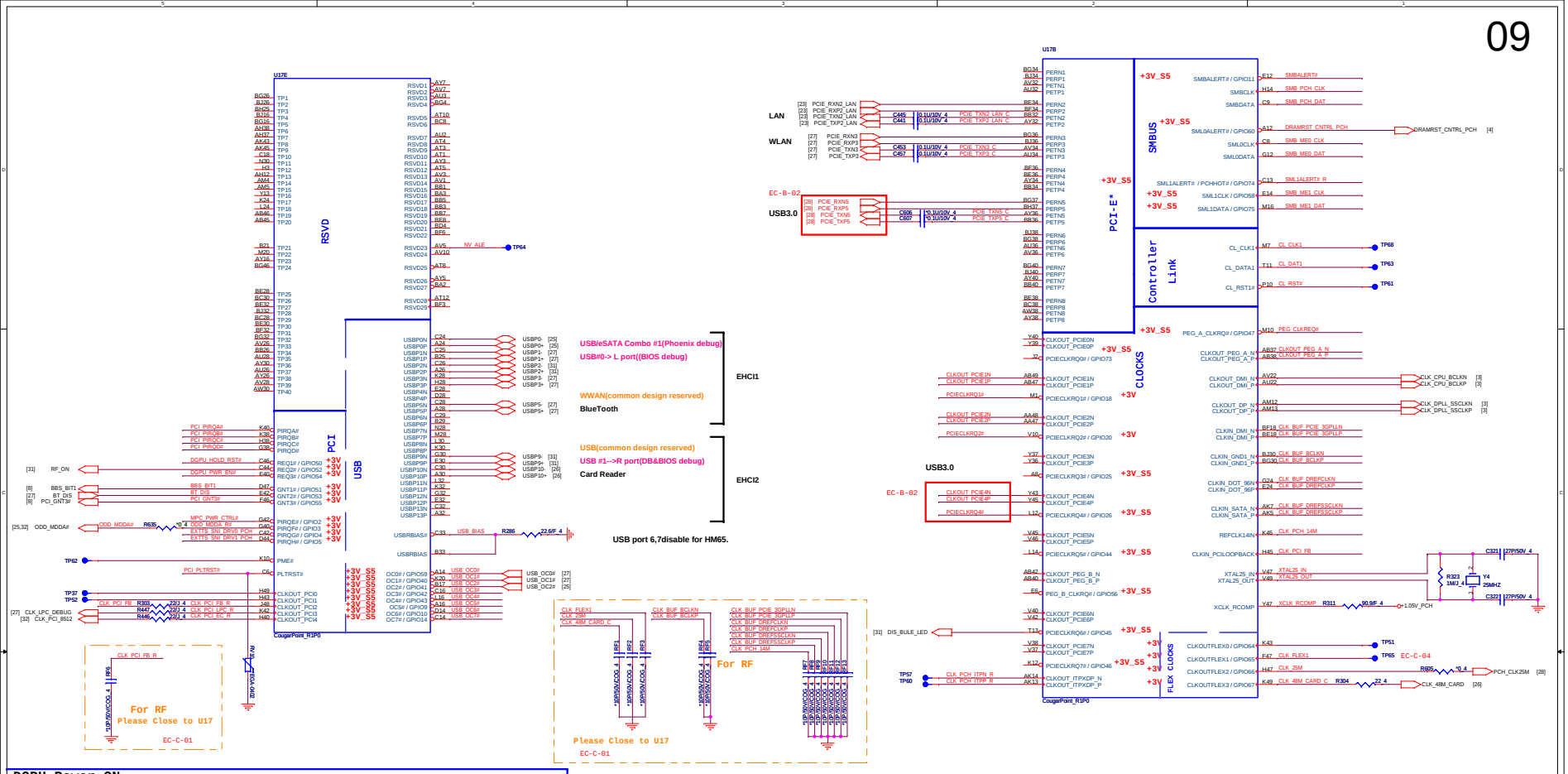
PCH2(CLG)

Cougar Point (HDA,JTAG,SATA)

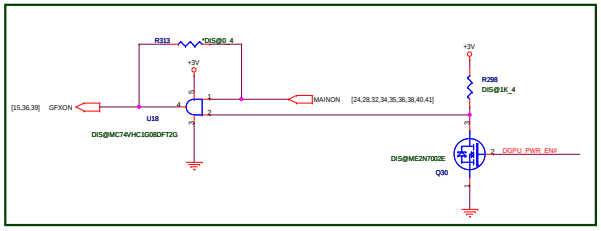


PCH Strap Table

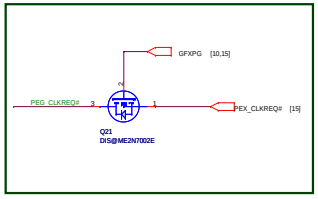
Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R529 *1K/J_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R450 *1K/J_4 PCI_GNT3# [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R272 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R448 *1K/J_4 BBS_BIT1 [9] R247 *1K/J_4 BBS_BIT0
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 R468 *1K/J_4 ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R238 2.2K/J_4 +1.8V R252 4.7K/J_4 DF_TVS [10] H_SNB_IVB# [3]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R523 *1K/J_4 PLL_ODVR_EN [10]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R296 1K/J_4 ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R203 *1K/J_4 PCH_SPI_SI
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	



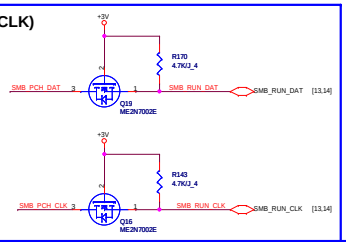
DGPU Power ON



PEG CLK detect



SMBus(CLK)



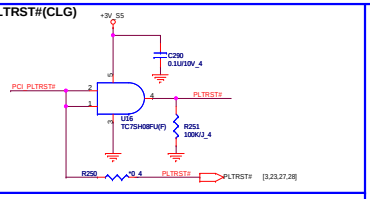
CLK Gen(CLK)

02/20 DEL for Pre-ES1

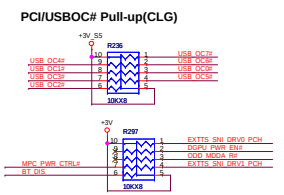
CPU_CLK select(CLK)

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

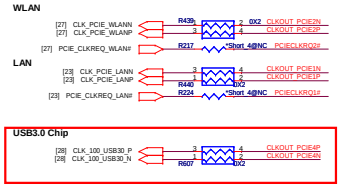
PLTRST#(CLG)



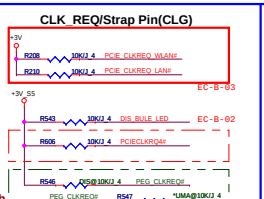
PCI/USBOC# Pull-up(CLG)



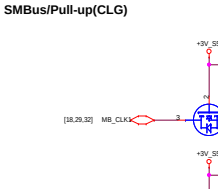
WLAN / LAN / USB3.0 Chip



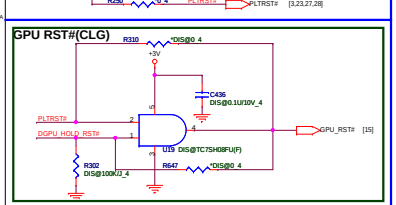
CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



GPU RST#(CLG)



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Cougar Point (GPIO,VSS_NCTF,RSVD)

U17F

S_GPIO R496 100_4 T7 BMBUSY# / GPIO0 +3V
[28,32] EC_EXT_SMI# EC_EXT_SMI# A42 TACH1 / GPIO1 +3V
BOARD_ID1 H36 TACH2 / GPIO6 +3V
[32] EC_EXT_SCI# EC_EXT_SCI# E38 TACH3 / GPIO7 +3V
TP103 ICC_EN# C10 GPIO8 +3V_S5
[27] LAN_DISABLE# LAN_DISABLE# C4 LAN_PHY_PWR_CTRL / GPIO12 +3V_S5
HOST_ALERT#1_R G2 GPIO15 +3V_S5
BOARD_ID0 U2 SATA4GP / GPIO16 +3V
GFXPG_R D40 TACH0 / GPIO17 +3V
BIOS_REC T5 SCLOCK / GPIO22 +3V
USB30_ID E8 GPIO24 / MEM_LED +3V_S5
GPIO27 E16 GPIO27 DSW
EC-B-06 [8] PLL_ODVR_EN R501 *Short_4_NC P8 GPIO28 +3V_S5
SYSTEM_ID K1 STP_PCI# / GPIO34 +3V
[27] BT_ON# BT_ON# K4 GPIO35 +3V
TP67 GPIO36 V8 SATA2GP / GPIO36 +3V
FDI_OVRVLTG M5 SATA3GP / GPIO37 +3V
MFG_MODE N2 SLOAD / GPIO38 +3V
DGPU_PRSNT# M3 SDATAOUT0 / GPIO39 +3V
TEST_SET_UP V13 SDATAOUT1 / GPIO48 +3V
[29,32] TEMP_ALERT# V3 SATA5GP / GPIO49 +3V
SV_DET D6 GPIO57 +3V_S5

GPIO

TACH4 / GPIO68 C40 CPU_ID
TACH5 / GPIO69 B41 R291 1.5K/F_4 +3V
TACH6 / GPIO70 C41 COLOR_ENGINE_DET R608 10K_4
TACH7 / GPIO71 A40 BOARD_ID2 EC-B-01

CPU/MISC

A20GATE P4 EC_A20GATE [32]
PECI AU16 TP59
RCIN# P5 EC_RCIN# EC_RCIN# [32]
PROCPWRGD AY11 H_PWRGOOD [3]
THRMTRIP# AY10 PCH_THRMTRIP# R499 390/J_4 PM_THRMTRIP# [3]
INIT3_3V# T14
DF_TVS AY1 DF_TVS [8]

TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37

3/16 Connected to GND
DG rev0.9

NCTF

VSS_NCTF_1 A4
VSS_NCTF_2 A44
VSS_NCTF_3 A45
VSS_NCTF_4 A46
VSS_NCTF_5 A5
VSS_NCTF_6 A6
VSS_NCTF_7 B3
VSS_NCTF_8 B47
VSS_NCTF_9 BD1
VSS_NCTF_10 BD49
VSS_NCTF_11 BE1
VSS_NCTF_12 BE49
VSS_NCTF_13 BF1
VSS_NCTF_14 BF49
VSS_NCTF_15 BG2
VSS_NCTF_16 BG48
VSS_NCTF_17 BH3
VSS_NCTF_18 BH47
VSS_NCTF_19 BJ4
VSS_NCTF_20 BJ44
VSS_NCTF_21 BJ45
VSS_NCTF_22 BJ46
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ6
VSS_NCTF_25 C2
VSS_NCTF_26 C48
VSS_NCTF_27 D1
VSS_NCTF_28 D49
VSS_NCTF_29 E1
VSS_NCTF_30 E49
VSS_NCTF_31 F1
VSS_NCTF_32 F49

CougarPoint_R1P0

GPIO Pull-up/Pull-down(CLG)

LAN_DISABLE# R242 10K/J_4 +3V_S5
EC_EXT_SMI# R293 10K/J_4
EC_EXT_SCI# R462 10K/J_4
EC_A20GATE R519 10K/J_4
EC_RCIN# R508 10K/J_4
TEMP_ALERT# R227 10K/J_4
BT_ON# R522 10K/J_4 +3V
GPIO27 R487 10K/J_4
GFXPG_R R228 DIS@10K/J_4

USB30 ID: 0-->Support
1-->Nonsupport

USB30_ID

EC-B-11

R645 *10K/J_4 USB30_ID R646 10K/J_4 +3V_S5

Board ID

EC-B-04, EC-B-11

Board ID For Function	SYSTEM_ID GPIO34	ID2 GPIO71	ID1 GPIO6	ID0 GPIO16	ID3 GPIO13
SDV	0	0	0	0	0
SIV	0	0	0	1	0
SIT	0	0	1	0	0
SVT	0	0	1	1	0
SOVP	0	0	0	0	1

Board ID use below GPIO:
BOARD_ID0
BOARD_ID1
BOARD_ID3

ID2: 0-->6 layer
1-->8 layer

System ID: 0-->KL5
1-->KL6

CPU_ID: 0-->35W
1-->45W

R248 *10K/J_4 BOARD_ID0 R226 10K/J_4
R464 10K/J_4 BOARD_ID1 R461 *10K/J_4
R289 10K/J_4 BOARD_ID2 R290 *10K/J_4
R641 10K/J_4 CPU_ID R642 *10K/J_4
R229 10K/J_4 SYSTEM_ID R230 *10K/J_4
R655 10K/J_4 BOARD_ID3 R644 *10K/J_4 +3V_S5
BOARD_ID3 [8]

R214 *DIS@0_4 +3V
GFXPG_R GFXPG_R
U14
DIS@MC74VHC1G08DFT2G
HWPG [32,36,37,38,40,41,42]
GFXPG [9,15]

SV_SET_UP
High = Strong (Default)

TEST_SET_UP R540 10K/J_4 R541 *0/J_4 +3V

R520 *10K/J_4 SV_DET R525 100K/J_4 +3V

SGPIO

S_GPIO R513 10K/J_4 R500 *0/J_4 +3V

HOST_ALERT#1_R R243 1K/J_4 +3V_S5

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

	Optimus	UMA
Stuff	R539	R527
No Stuff	R527	R539

R527 *UMA@10K/J_4 DGPU_PRSNT# R539 DIS@100K/J_4 +3V

R534 100K/J_4 FDI_OVRVLTG R537 *1K/F_4 +3V

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

GPIO36 R636 *200K/F_4 +3V

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS_REC R528 10K/J_4 R524 *0/J_4 +3V

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST

MFG_MODE R204 10K/J_4 R225 *0/J_4 +3V

PROJECT KL5A
Quanta Computer Inc.

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Custom	Cougar Point 4/6	1A

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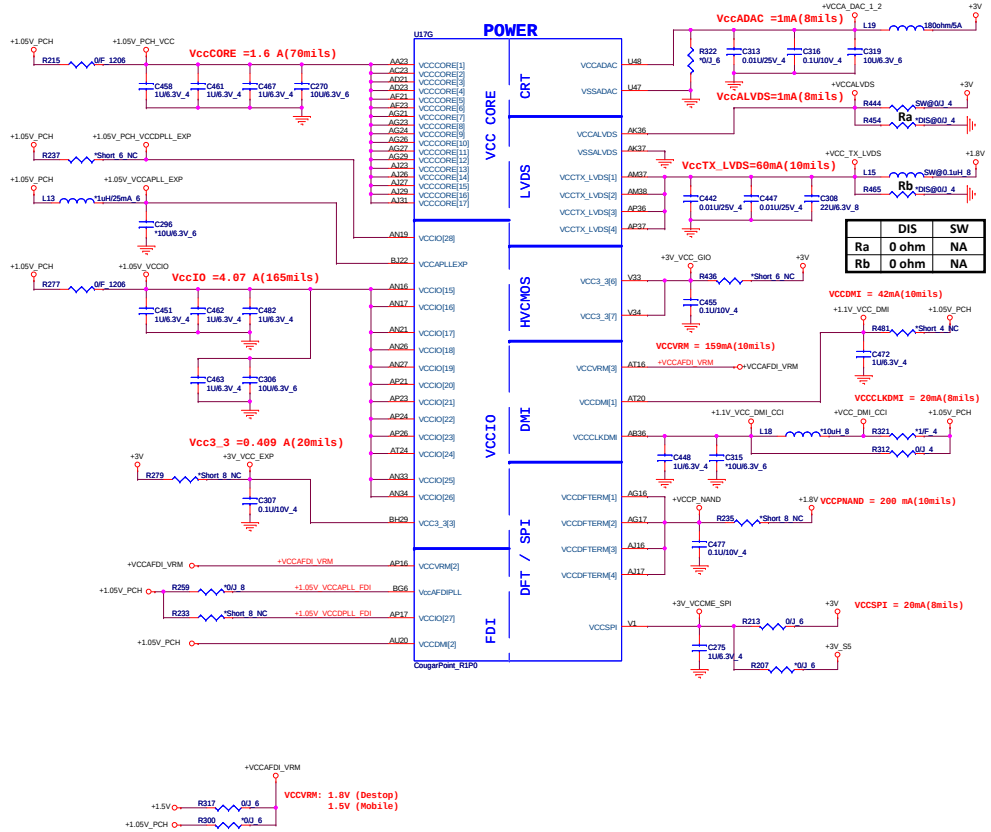
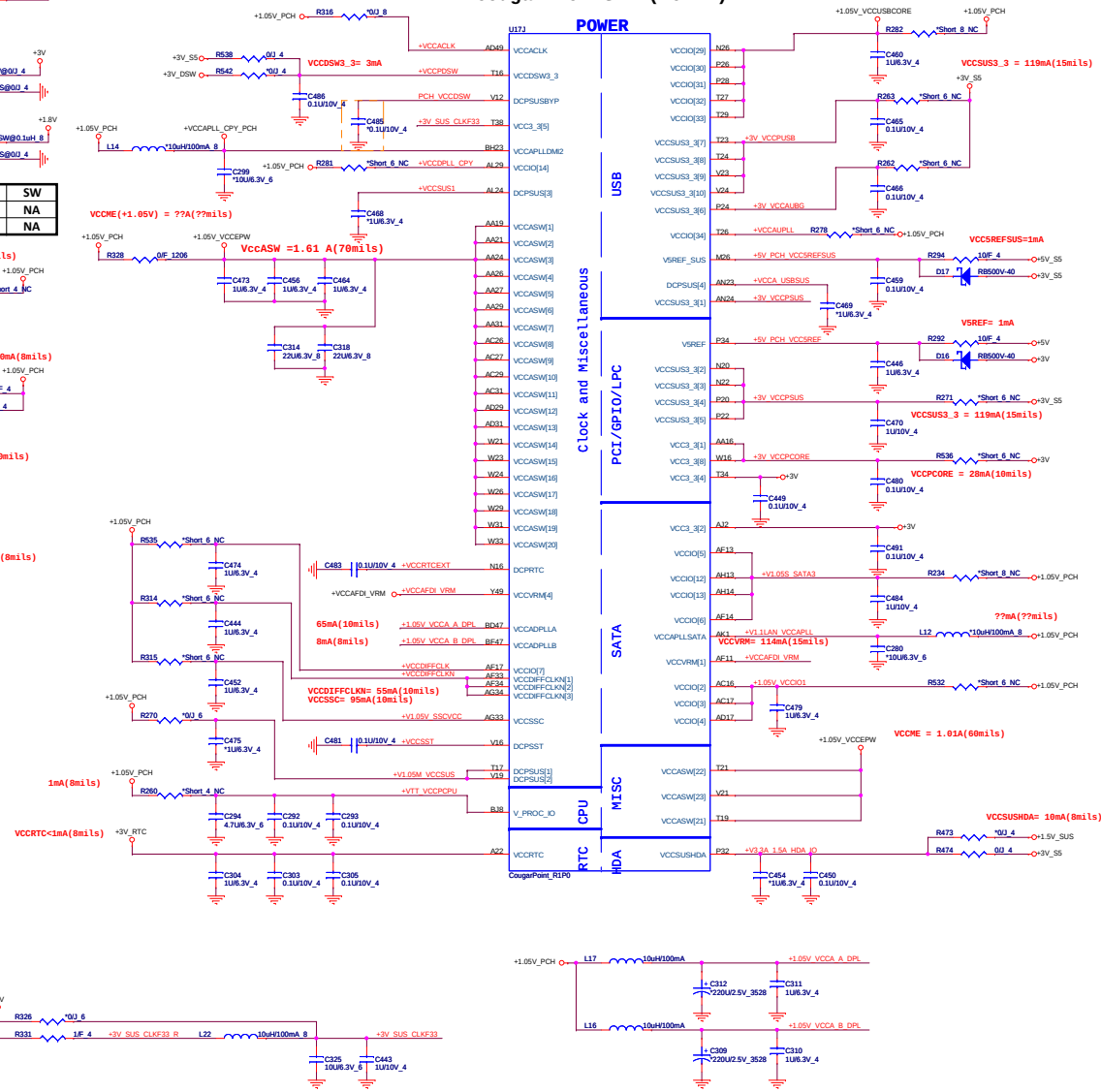
COUGAR POINT (POWER)



Cougar Point-M (POWER)



PROJECT KL5A
Quanta Computer Inc.
Size: Custom
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Rev: 1A
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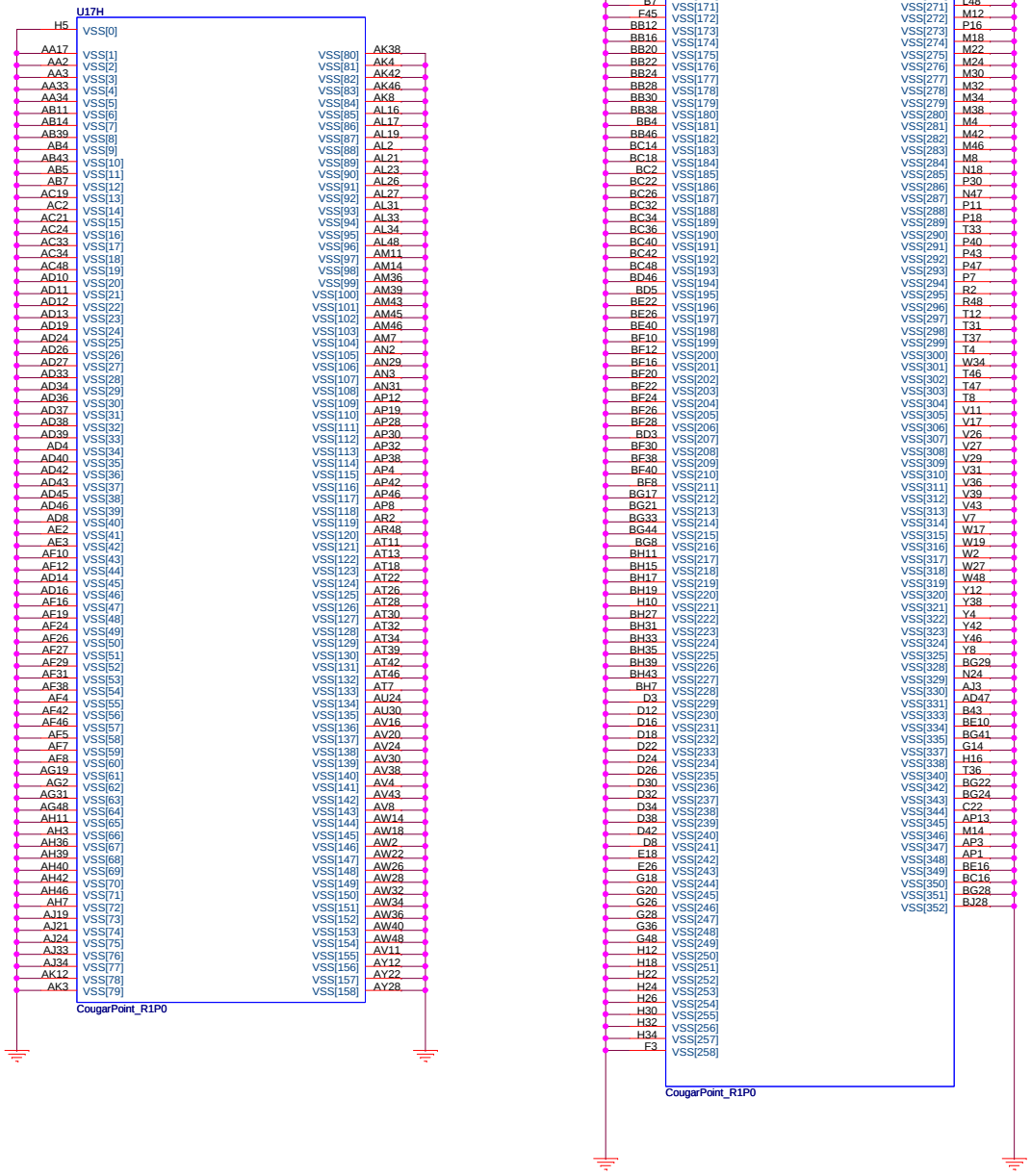
IBEX PEAK-M (GND)



PROJECT KL5A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cougar Point 6/6	1A
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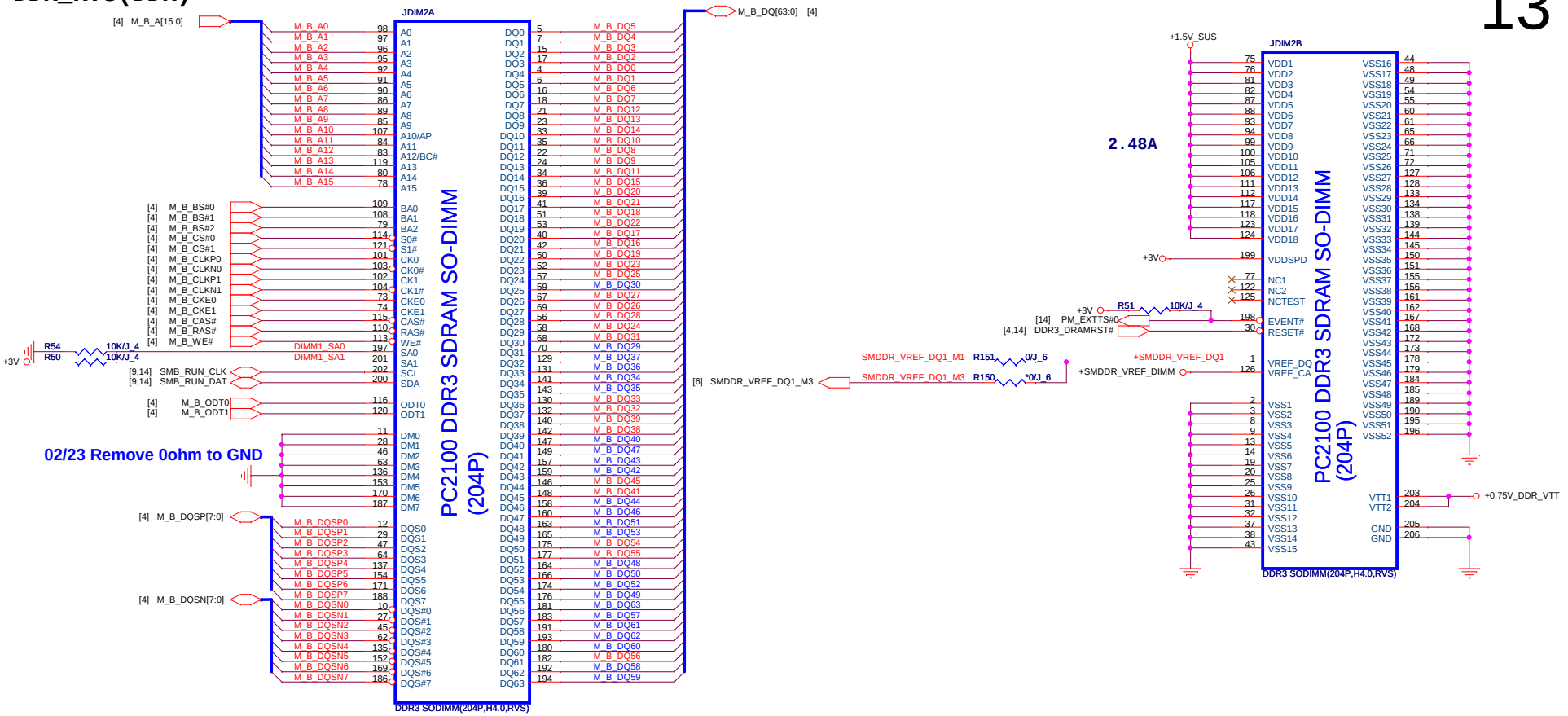
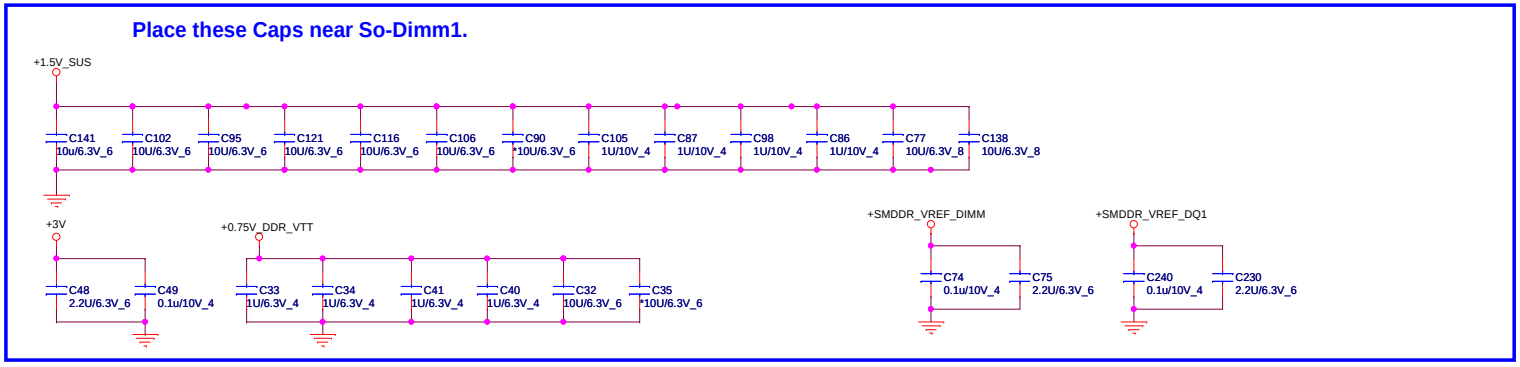
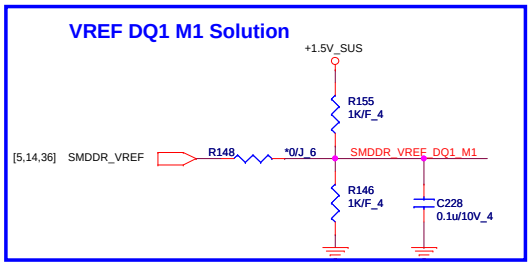
DDR_RVS(DDR)







	STD 4H	STD 8H
FOX	DGMK4000090	DGMK4000122
LTK	DGMK4000005	DGMK4000087
SUY	DGMK4000181	DGMK4000182
SKT	DGMK0000120	DGMK4000139
Standard 8H type:DDR-C-2013310-204p-1		

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRIII SO-DIMM-0	1A

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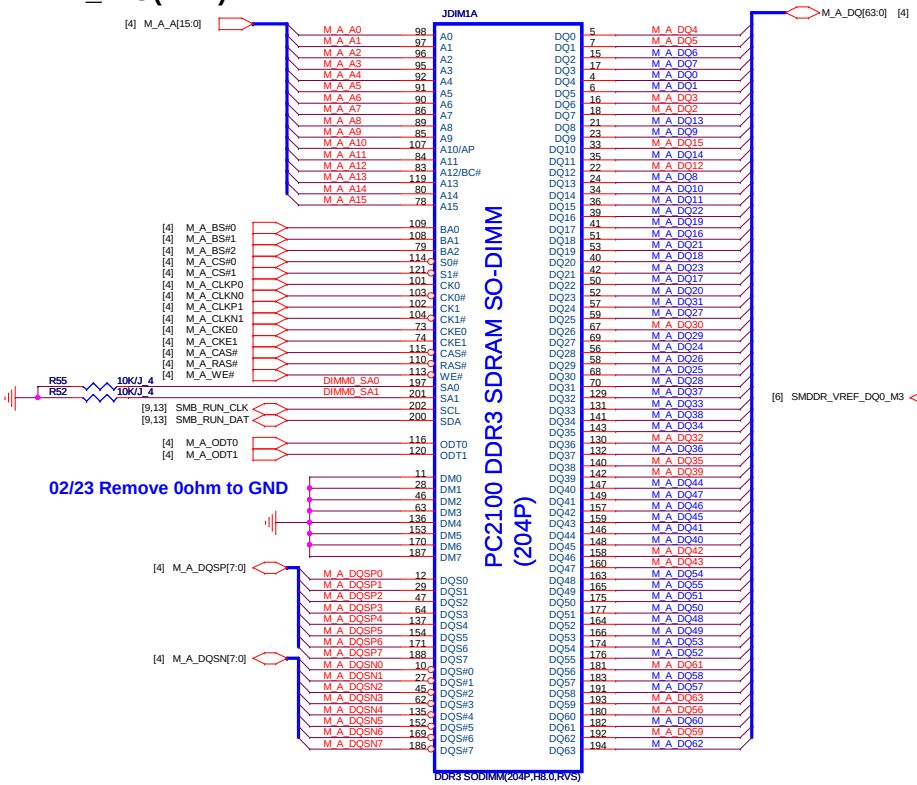
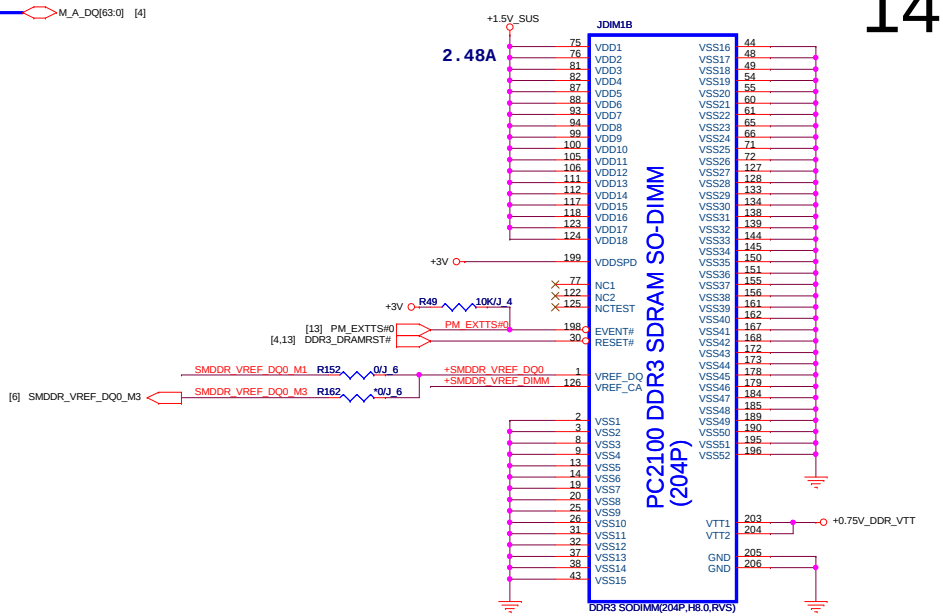
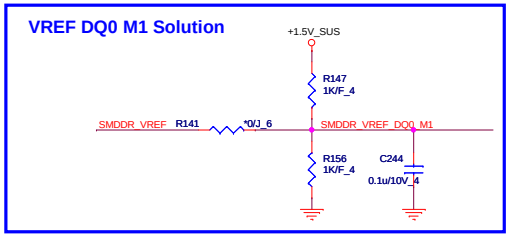
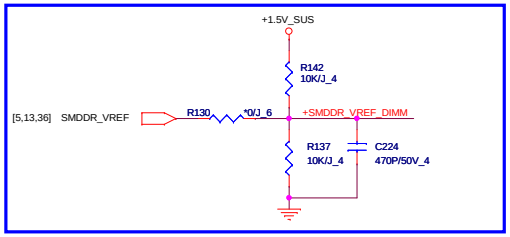
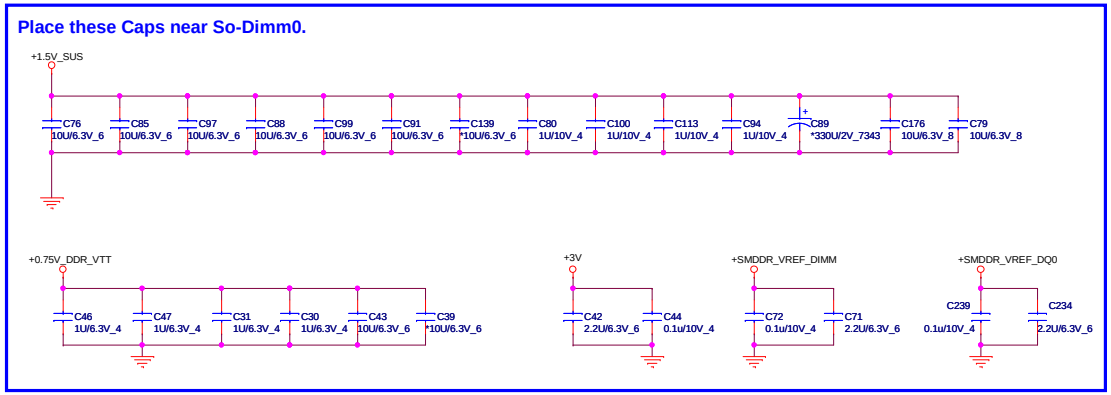
DDR_RVS(DDR)











PROJECT KL5A			
Quanta Computer Inc.			
Size: Custom	Document Number: DDRIII SO-DIMM-1		Rev: 1A
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power up sequence

3.55A

16.82A

80mA

110mA
12~16 mils

U28A
N12M
1/13 PCI_EXPRESS

PLACE NEAR BALLS
PLACE UNDER BALLS
GFX_CORE

For PCIE clock request signal 07/05

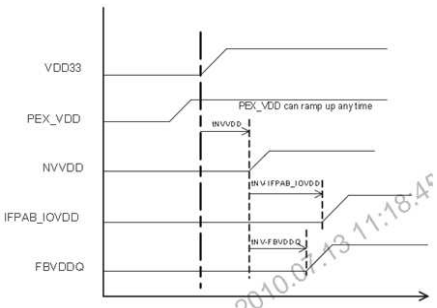
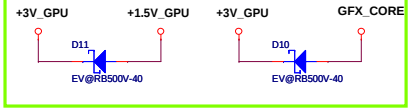


Figure 3.12 Recommended Power Sequencing Order

DGPU_PWR_EN# = GFXON >> +1.05_GFX_PCIE
>> +3V_GPU_EN >> +3V_GPU
>> NVVDD =NVVDD_PG
>> +1.5_GPU >> +1.8V_GPU

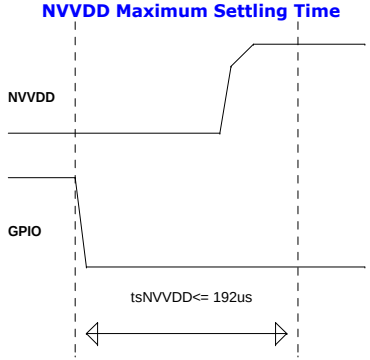
For power-down sequency



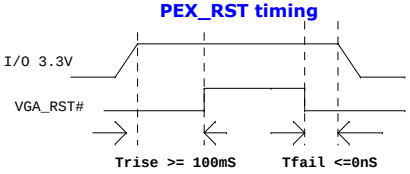
The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:

- NVVDD <= VDD33+0.5 V
- FBVDDQ <= VDD33+0.5 V

NVVDD Maximum Settling Time



PEX_RST timing



PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N12M(PCIE I/F) 1/5	1A

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EC-C-00

2.63A

+1.5V_GPU

U28B
N12M

2/13 FRAME_BUFFER

C235 EV@0.01U/16V/X7R_4
C237 EV@0.01U/16V/X7R_4
C248 EV@0.01U/16V/X7R_4
C227 EV@0.047U/10V/X7R_4
C245 EV@0.047U/10V/X7R_4
C229 EV@0.047U/10V/X7R_4
C232 EV@4.7U/6.3V/X5R_6

FBVDDQ_01 A13
FBVDDQ_02 B13
FBVDDQ_03 C13
FBVDDQ_04 D13
FBVDDQ_05 D14
FBVDDQ_06 E13
FBVDDQ_07 F13
FBVDDQ_08 F14
FBVDDQ_09 F15
FBVDDQ_10 F16
FBVDDQ_11 F17
FBVDDQ_12 F19
FBVDDQ_13 F22
FBVDDQ_14 H23
FBVDDQ_15 H26
FBVDDQ_16 J15
FBVDDQ_17 J16
FBVDDQ_18 J18
FBVDDQ_19 J19
FBVDDQ_20 L19
FBVDDQ_21 L23
FBVDDQ_22 L26
FBVDDQ_23 M19
FBVDDQ_24 N22
FBVDDQ_25 U22
FBVDDQ_26 Y22

(FBA_D8) FBA_D0 D22 VMA_DQ0
(FBA_D10) FBA_D1 E24 VMA_DQ1
(FBA_D9) FBA_D2 E22 VMA_DQ2
(FBA_D11) FBA_D3 D24 VMA_DQ3
(FBA_D12) FBA_D4 D26 VMA_DQ4
(FBA_D13) FBA_D5 D27 VMA_DQ5
(FBA_D14) FBA_D6 C27 VMA_DQ6
(FBA_D15) FBA_D7 B27 VMA_DQ7
(FBA_D31) FBA_D8 A21 VMA_DQ8
(FBA_D30) FBA_D9 B21 VMA_DQ9
(FBA_D29) FBA_D10 C21 VMA_DQ10
(FBA_D28) FBA_D11 C19 VMA_DQ11
(FBA_D26) FBA_D14 C18 VMA_DQ12
(FBA_D27) FBA_D14 D18 VMA_DQ13
(FBA_D25) FBA_D14 B18 VMA_DQ14
(FBA_D24) FBA_D15 C16 VMA_DQ15
(FBA_D22) FBA_D16 E21 VMA_DQ16
(FBA_D23) FBA_D17 F21 VMA_DQ17
(FBA_D20) FBA_D18 D20 VMA_DQ18
(FBA_D21) FBA_D19 F20 VMA_DQ19
(FBA_D18) FBA_D20 D17 VMA_DQ20
(FBA_D19) FBA_D21 F18 VMA_DQ21
(FBA_D16) FBA_D22 D16 VMA_DQ22
(FBA_D17) FBA_D23 E16 VMA_DQ23
(FBA_D3) FBA_D24 A22 VMA_DQ24
(FBA_D4) FBA_D25 C24 VMA_DQ25
(FBA_D0) FBA_D26 D21 VMA_DQ26
(FBA_D2) FBA_D27 B22 VMA_DQ27
(FBA_D1) FBA_D28 C22 VMA_DQ28
(FBA_D6) FBA_D29 A25 VMA_DQ29
(FBA_D5) FBA_D30 B25 VMA_DQ30
(FBA_D7) FBA_D31 A26 VMA_DQ31
(FBA_D37) FBA_D32 U24 VMA_DQ32
(FBA_D39) FBA_D33 V24 VMA_DQ33
(FBA_D38) FBA_D35 V23 VMA_DQ34
(FBA_D35) FBA_D35 R24 VMA_DQ35
(FBA_D36) FBA_D36 T23 VMA_DQ36
(FBA_D34) FBA_D37 R23 VMA_DQ37
(FBA_D33) FBA_D38 P24 VMA_DQ38
(FBA_D32) FBA_D39 P22 VMA_DQ39
(FBA_D55) FBA_D40 AC24 VMA_DQ40
(FBA_D53) FBA_D41 AB23 VMA_DQ41
(FBA_D54) FBA_D42 AB24 VMA_DQ42
(FBA_D51) FBA_D43 W24 VMA_DQ43
(FBA_D52) FBA_D44 AA22 VMA_DQ44
(FBA_D50) FBA_D45 W23 VMA_DQ45
(FBA_D49) FBA_D46 W22 VMA_DQ46
(FBA_D48) FBA_D47 V22 VMA_DQ47
(FBA_D59) FBA_D48 AA25 VMA_DQ48
(FBA_D58) FBA_D49 W27 VMA_DQ49
(FBA_D57) FBA_D50 W26 VMA_DQ50
(FBA_D56) FBA_D51 W25 VMA_DQ51
(FBA_D60) FBA_D52 AB25 VMA_DQ52
(FBA_D61) FBA_D53 AB26 VMA_DQ53
(FBA_D62) FBA_D54 AD26 VMA_DQ54
(FBA_D63) FBA_D55 AD27 VMA_DQ55
(FBA_D46) FBA_D56 V25 VMA_DQ56
(FBA_D42) FBA_D57 R25 VMA_DQ57
(FBA_D45) FBA_D58 V26 VMA_DQ58
(FBA_D47) FBA_D59 V27 VMA_DQ59
(FBA_D43) FBA_D60 R26 VMA_DQ60
(FBA_D44) FBA_D61 T25 VMA_DQ61
(FBA_D40) FBA_D62 N25 VMA_DQ62
(FBA_D41) FBA_D63 N26 VMA_DQ63

[19] FBA_CMD0 G24 FBA_CMD0
FBA_CMD1 F27 FBA_CMD1
[19] FBA_CMD2 F25 FBA_CMD2
[19] FBA_CMD3 F26 FBA_CMD3
[19] FBA_CMD4 G26 FBA_CMD4
[19] FBA_CMD5 G27 FBA_CMD5
[19] FBA_CMD6 G25 FBA_CMD6
[19] FBA_CMD7 J25 FBA_CMD7
[19] FBA_CMD8 J24 FBA_CMD8
[19] FBA_CMD9 H24 FBA_CMD9
[19] FBA_CMD10 H22 FBA_CMD10
[19] FBA_CMD11 J26 FBA_CMD11
[19] FBA_CMD12 G22 FBA_CMD12
[19] FBA_CMD13 G23 FBA_CMD13
[19] FBA_CMD14 J22 FBA_CMD14
[19] FBA_CMD15 J27 FBA_CMD15
[19] FBA_CMD16 M24 FBA_CMD16
FBA_CMD17 L24 FBA_CMD17
[19] FBA_CMD18 J23 FBA_CMD18
[19] FBA_CMD19 K23 FBA_CMD19
[19] FBA_CMD20 K22 FBA_CMD20
[19] FBA_CMD21 M23 FBA_CMD21
[19] FBA_CMD22 K24 FBA_CMD22
[19] FBA_CMD23 M27 FBA_CMD23
[19] FBA_CMD24 N27 FBA_CMD24
[19] FBA_CMD25 M26 FBA_CMD25
[19] FBA_CMD26 K26 FBA_CMD26
[19] FBA_CMD27 K27 FBA_CMD27
[19] FBA_CMD28 K25 FBA_CMD28
[19] FBA_CMD29 M25 FBA_CMD29
[19] FBA_CMD30 L22 FBA_CMD30

[19] VMA_CLK0 VMA_CLK0 F24 FBA_CLK0
[19] VMA_CLK0# VMA_CLK0# F23 FBA_CLK0*
[19] VMA_CLK1 VMA_CLK1 N24 FBA_CLK1
[19] VMA_CLK1# VMA_CLK1# N23 FBA_CLK1*

+1.5V_GPU R164 EV@40.2/F_4 FB_CAL_PD_VDDQ B15 FB_CAL_PD_VDDQ
R175 EV@40.2/F_4 FB_CAL_PU_GND A15 FB_CAL_PU_GND
R169 EV@60.4/F_4 FB_CAL_TERM_GND B16 FB_CAL_TERM_GND

+1.5V_GPU R129 *EV@60.4/F_4 FBA_DEBUG M22 FBA_DEBUG0
10mA
For debug only

+1.05V_GFX_PCIE
15mils width 25mA
L8 EV@BLM18PG300SN1D(30,1A)_6 +FB_PLLAVDD R19 FB_PLLAVDD
PLACE UNDER BALLS
C681 EV@0.1U/10V/X7R_4 T19 FB_DLLAVDD
C682 EV@1U/16V/X7R_6
C683 EV@10U/6.3V/X7R_8 AC19 FB_PLLAVDD (NC)
PLACE NEAR BALLS

(DQM1) FBA_DQM0 C26 VMA_DM0
(DQM3) FBA_DQM1 B19 VMA_DM1
(DQM2) FBA_DQM2 D19 VMA_DM2
(DQM0) FBA_DQM3 D23 VMA_DM3
(DQM4) FBA_DQM4 T24 VMA_DM4
(DQM6) FBA_DQM5 AA23 VMA_DM5
(DQM7) FBA_DQM6 AB27 VMA_DM6
(DQM5) FBA_DQM7 T26 VMA_DM7

(WP1) FBA_DQS_WP0 C25 VMA_WDQS0
(WP3) FBA_DQS_WP1 A19 VMA_WDQS1
(WP2) FBA_DQS_WP2 E19 VMA_WDQS2
(WP0) FBA_DQS_WP3 A24 VMA_WDQS3
(WP4) FBA_DQS_WP4 T22 VMA_WDQS4
(WP6) FBA_DQS_WP5 AA24 VMA_WDQS5
(WP7) FBA_DQS_WP6 AA26 VMA_WDQS6
(WP5) FBA_DQS_WP7 T27 VMA_WDQS7

(RN1) FBA_DQS_RN0 D25 VMA_RDQS0
(RN3) FBA_DQS_RN1 A18 VMA_RDQS1
(RN2) FBA_DQS_RN2 E18 VMA_RDQS2
(RN0) FBA_DQS_RN3 B24 VMA_RDQS3
(RN4) FBA_DQS_RN4 R22 VMA_RDQS4
(RN6) FBA_DQS_RN5 Y24 VMA_RDQS5
(RN7) FBA_DQS_RN6 AA27 VMA_RDQS6
(RN5) FBA_DQS_RN7 R27 VMA_RDQS7

FB_VREF A16 +FB_VREF1 TP76

EV@U_GPU_GB1_64

[19] VMA_DQ[63..0]
[19] VMA_DM[7..0]
[19] VMA_WDQS[7..0]
[19] VMA_RDQS[7..0]

FBA_CMD0 R139 EV@10K/F_4
FBA_CMD3 R568 EV@10K/F_4
FBA_CMD16 R158 EV@10K/F_4
FBA_CMD19 R161 EV@10K/F_4
FBA_CMD20 R135 EV@10K/F_4

U28I
N12M

13/13 GND_NC

AC11 GND_01
AC14 GND_02
AC17 GND_03
AC2 GND_04
AC20 GND_05
AC23 GND_06
AC26 GND_07
AC5 GND_08
AC8 GND_09
AE11 GND_10
AE14 GND_11
AE17 GND_12
AF2 GND_13
AF20 GND_14
AF23 GND_15
AF26 GND_16
AF5 GND_17
AF8 GND_18
B11 GND_19
B14 GND_20
B17 GND_21
B2 GND_22
B20 GND_23
B23 GND_24
B26 GND_25
B5 GND_26
B8 GND_27
E11 GND_28
E17 GND_30
E2 GND_31
E20 GND_32
E23 GND_33
E26 GND_34
E5 GND_35
E8 GND_36
H2 GND_37
H5 GND_38
J11 GND_39
J14 GND_40
J17 GND_41
K19 GND_42
K9 GND_43
L11 GND_44
L12 GND_45
L13 GND_46
L14 GND_47
L15 GND_48
L16 GND_49
L17 GND_50
L2 GND_51
L5 GND_52
M12 GND_53
M13 GND_54
M14 GND_55
M15 GND_56
M16 GND_57
P19 GND_58
P2 GND_59
P23 GND_60
P26 GND_61
P5 GND_62
P9 GND_63
T12 GND_64
T13 GND_65
T14 GND_66
T15 GND_67
T16 GND_68
U11 GND_69
U12 GND_70
U13 GND_71
U14 GND_72
U15 GND_73
U16 GND_74
U17 GND_75
U2 GND_76
U23 GND_77
U26 GND_78
U5 GND_79
V19 GND_80
V9 GND_81
W11 GND_82
W14 GND_83
W17 GND_84
Y2 GND_85
Y23 GND_86
Y26 GND_87
Y5 GND_88

NC_01 C15
NC_02 D15
PGOOD J5 R649 EV@10K/F_4

EV@U_GPU_GB1_64

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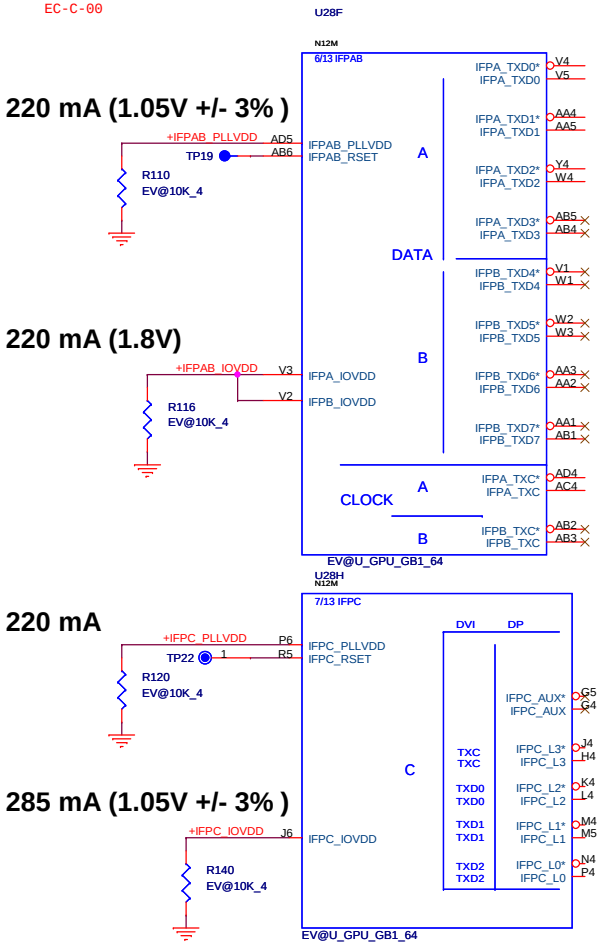


The following guidelines only apply to a fully unused IFP macro:

- Pull down IFPxy_IOVDD with 10 kΩ resistor
- Pull down IFPxy_PLLVDD with 10 kΩ resistor
- The other IO pins can be NC
- It is also recommended that footprints for both a 10 kΩ resistor to ground and a 10 kΩ resistor to power be implemented as stuffing options to allow for flexibility in design options

The circuit shown in Figure 6.12 shows the connection for an unused IFP macro.

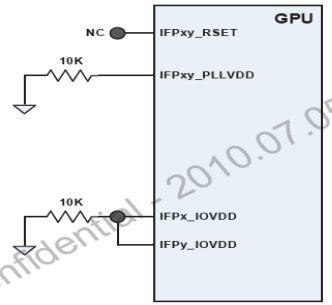
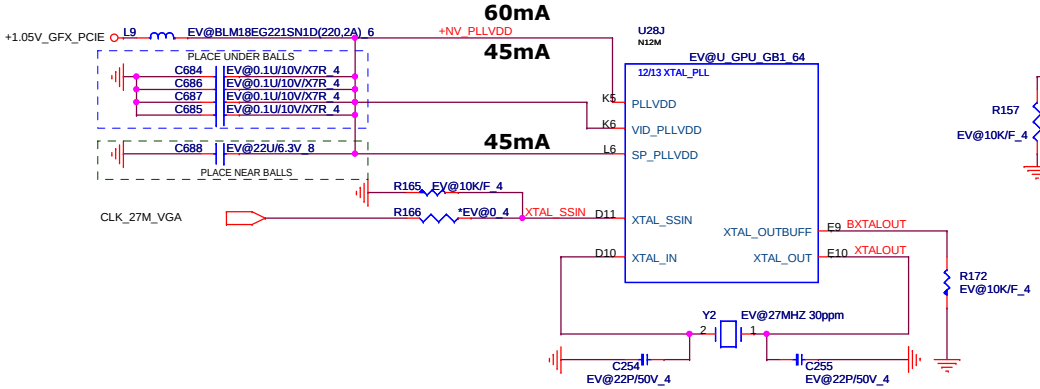


Figure 6.12 Unused IFP Interface

7.4 Unused DAC Interface

To disable a DAC interface:

- Pull down the DACx_VDD with a 10 kΩ resistor
- The other DAC IO pins (including DACx_VREF, DACx_RSET) can be NC



STUFF PDs on XTALSSIN and
XTALOUTBUFF WHEN EXT_SS
Install it when not connected to Spread spectrum device

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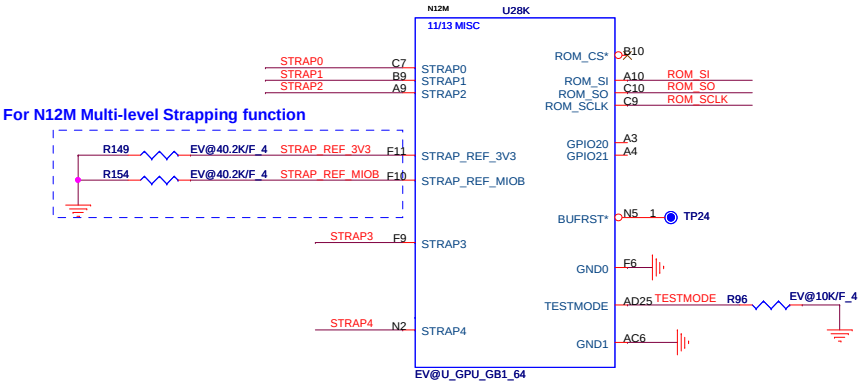
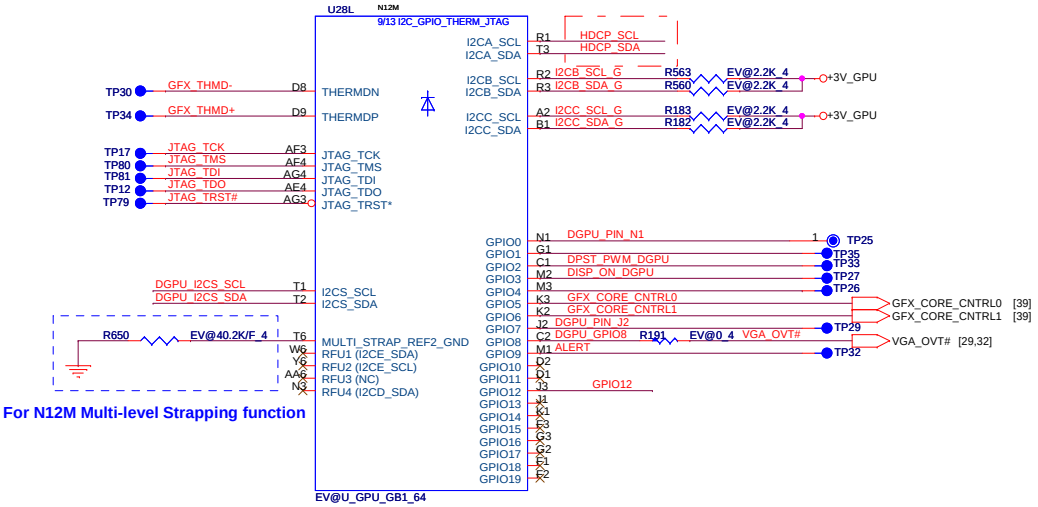
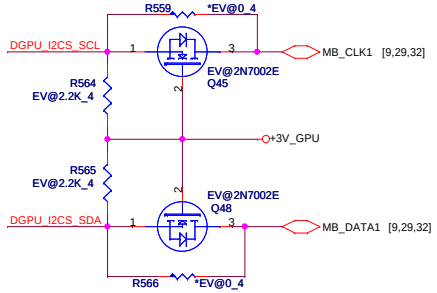
nV FAE suggest that the device ID
for N12M-GS-S is 0x1054.-0909



9.5 Unused I2C Pins

For unused dedicated (non-AUX) I2C pins, pull-up both the I2Cx_SCL, I2Cx_SDA, to 3.3 V using 2.2 kΩ resistors.routing.





CHIP	PCI_DEVID:	STRAP2
N12M-GS	0x1054	0100 PU 45K/F

VRAM Type	RAMCFG[0..3]	ROM_SI
Hynix AKD5LZGTW11	0x0A75	0010 PD 15K/F
Samsung AKD5EGGT501	0x0A70	0011 PD20 K/F
Hynix AKD5MGGTW00	0x0A75	0110 PD 34.8K/F
Samsung AKD5MGGT505	0x0A70	0111 PD 45.3K/F

GPU Type	STRAP0	STRAP1	STRAP3	STRAP4	ROM_SO	ROM_SCLK
N12M-GS	PU 45.3K/F	PD 34.8K/F	PD 4.99K/F	PD 20K/F	PU 10K/F	PU 15K/F

Logical Strap Bit Mapping

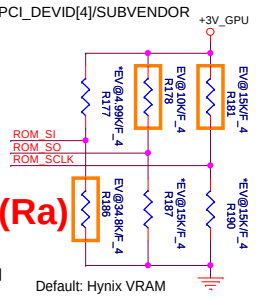
Rv	PU-VDD	PD-GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

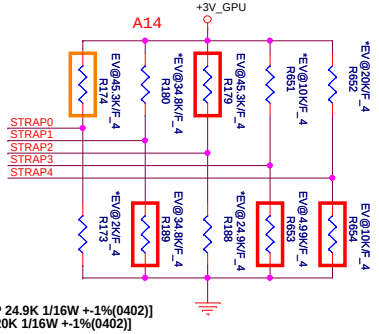
N12M-GS

PCI_DEVID[4]/SUBVENDOR

(Ra)

Default: Hynix VRAM





4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30K/F_4: CS33002FB13 [RES CHIP 30K 1/16W +-1%(0402)]
34.8K/F_4: CS33482FB22 [RES CHIP 34.8K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

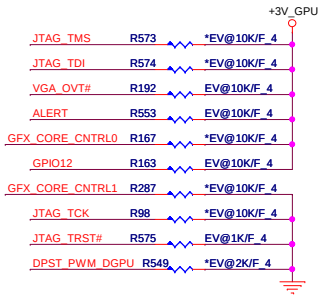
24.9K/F_4: CS32492FB16 [RES CHIP 24.9K 1/16W +-1%(0402)]
20K/F_4: CS32002FB29 [RES CHIP 20K 1/16W +-1%(0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO N12M-GS	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	1001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1111
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V	0011

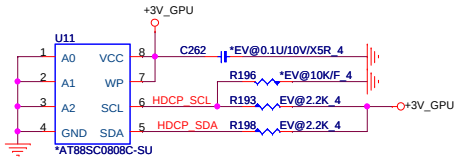
VRAM Configuration Table

(Ra)

	RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
	0000		Reserved		
	0001				
AKD5LZGTW11 AKD5EGGT501	0010	DDR3 64Mx16x4, 128bit, 512MB,800MHz	Hynix	H5TQ1G63DFR-12C	PD 15K/F
	0011	DDR3 64Mx16x4, 128bit, 512MB,800MHz	Samsung	K4W1G1646G-BC12	PD 20K/F
	0101		Reserved		
	0110				
AKD5MGGTW00	0110	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Hynix	H5TQ2G63BFR-12C	PD 34.8K/F
AKD5MGGT505	0111	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Samsung	K4W2G1646C-HC12	PD 45.3K/F



HDCP ROM



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP

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CHANNEL A: 512MB/1024MB DDR3

[16] VMA_DQ[63..0]
[16] VMA_DM[7..0]
[16] VMA_WDQS[7..0]
[16] VMA_RDQS[7..0]

U12 / U27 / U9 / U29 — 96-BALL SDRAM DDR3 — EV@VRAM_DDR3

Should be 240 Ohms +-1%

R185 EV@243/F_4 (U12)
R533 EV@243/F_4 (U27)
R126 EV@243/F_4 (U9)
R567 EV@243/F_4 (U29)

R211 EV@162/F_4 (VMA_CLK0 / VMA_CLK0#)
R118 EV@162/F_4 (VMA_CLK1 / VMA_CLK1#)

R530 EV@1.33K/F_4 (VREFC_VMA1) — R531 EV@1.33K/F_4 — C493 EV@0.1U/10V/X5R_4
R218 EV@1.33K/F_4 (VREFD_VMA1) — R219 EV@1.33K/F_4 — C274 EV@0.1U/10V/X5R_4
R555 EV@1.33K/F_4 (VREFC_VMA3) — R554 EV@1.33K/F_4 — C507 EV@0.1U/10V/X5R_4
R159 EV@1.33K/F_4 (VREFD_VMA3) — R160 EV@1.33K/F_4 — C247 EV@0.1U/10V/X5R_4

+1.5V_GPU decoupling:
C496 C211 C510 C180 EV@1U/6.3V/X5R_4
C179 C286 C508 C522 C250 EV@0.1U/10V/X5R_4
C499 C256 C498 C206 EV@1U/6.3V/X5R_4
C236 C495 C527 C272 C285 EV@0.1U/10V/X5R_4
C251 C263 C513 C501 EV@1U/6.3V/X5R_4
C246 C260 C531 C258 C500 EV@0.1U/10V/X5R_4
C506 C497 C505 C517 EV@1U/6.3V/X5R_4
C494 C257 C271 C226 C273 EV@0.1U/10V/X5R_4

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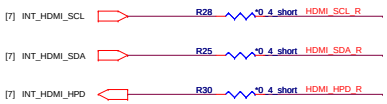
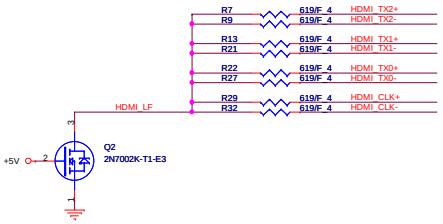
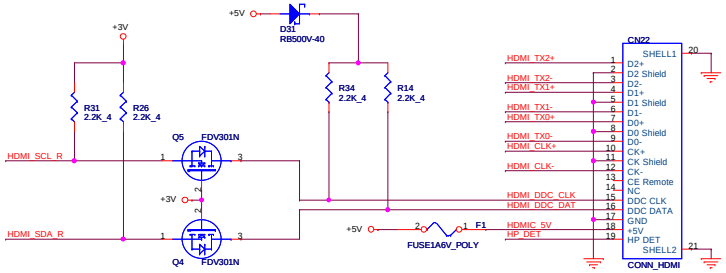
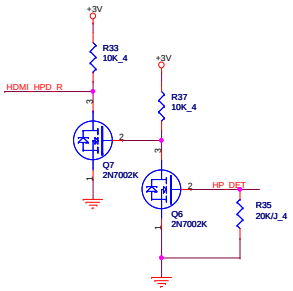
UMA Only / HDMI

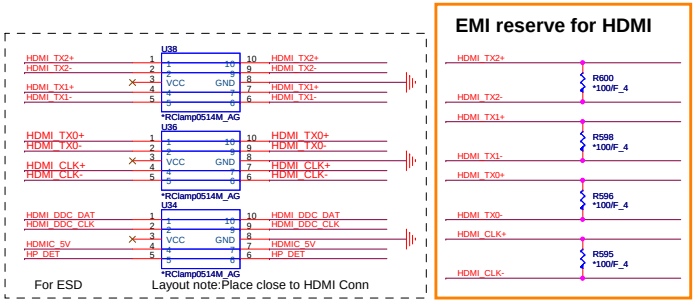






HDMI Hot-PLUG to EC and GPU





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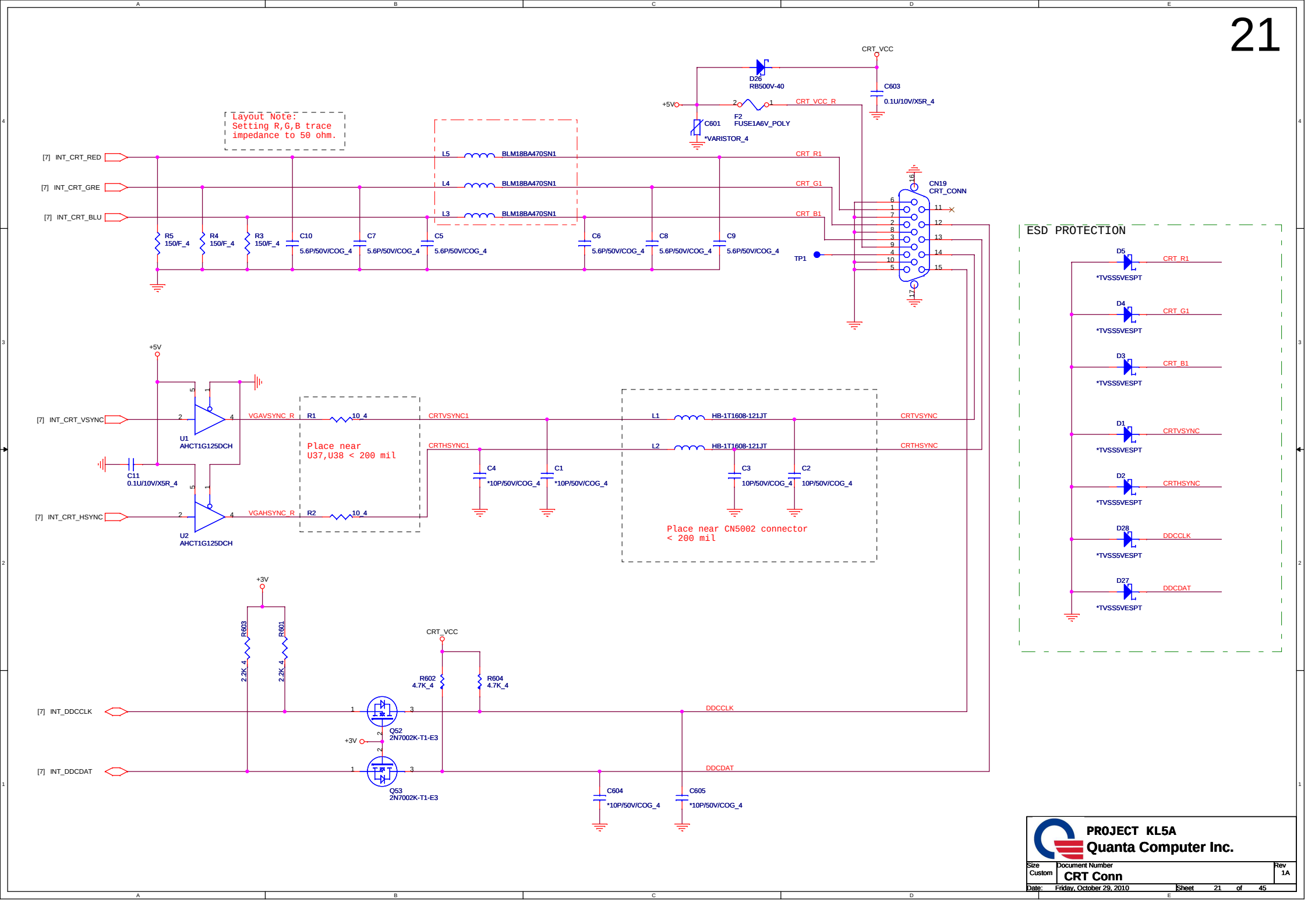

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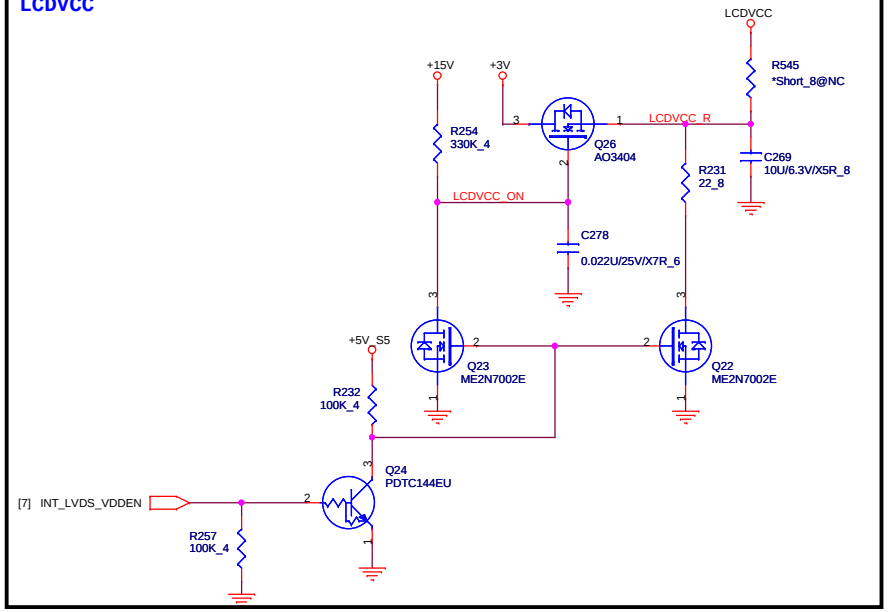
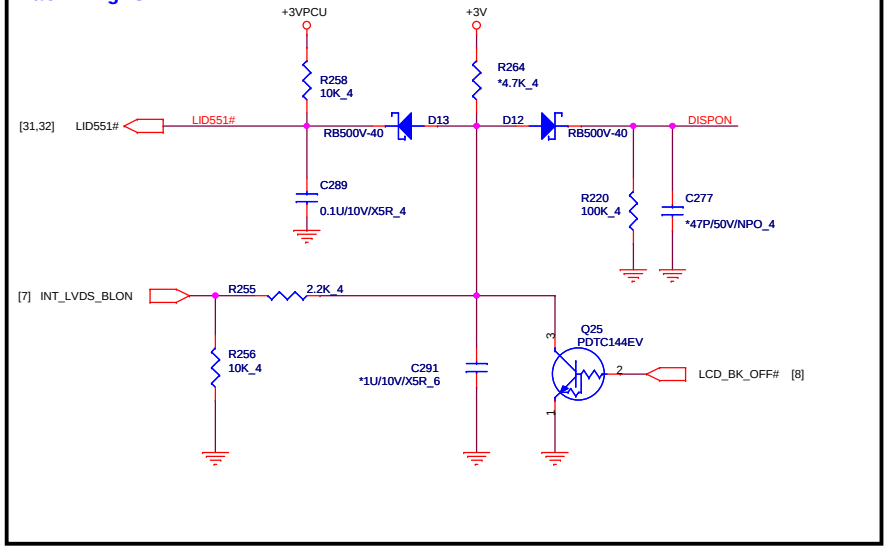
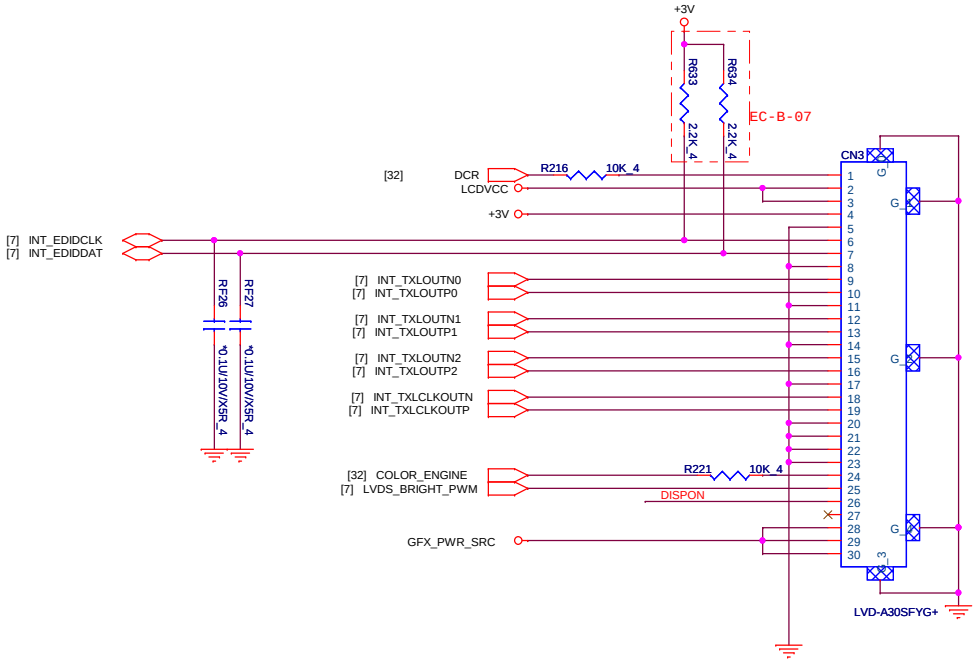
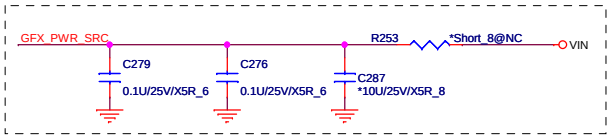
LCDVCC



Back light







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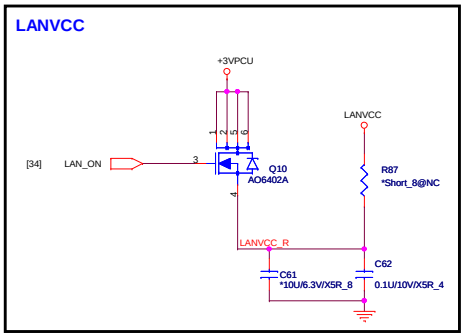
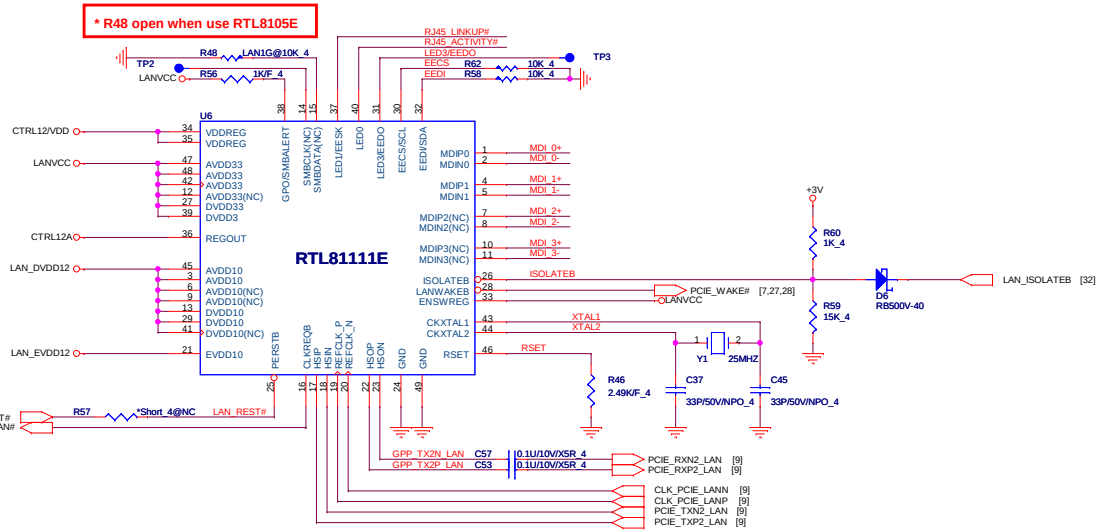
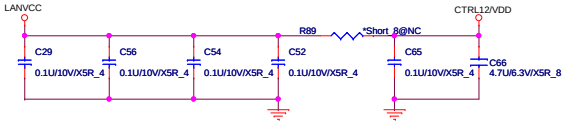
LANVCC



*** R48 open when use RTL8105E**

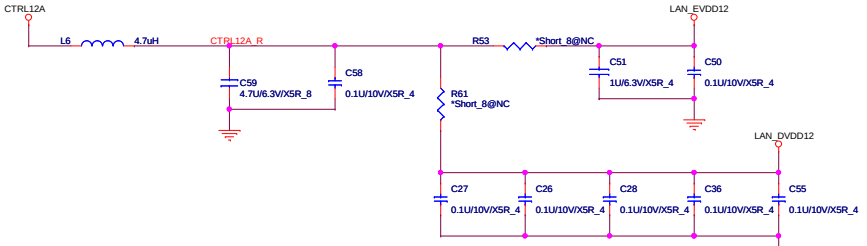




* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.

Place C5113 ,C5094 closed to U5006 pins44,45.

* C5116 and C5273 are for U5006 EVDD12 pin 19.

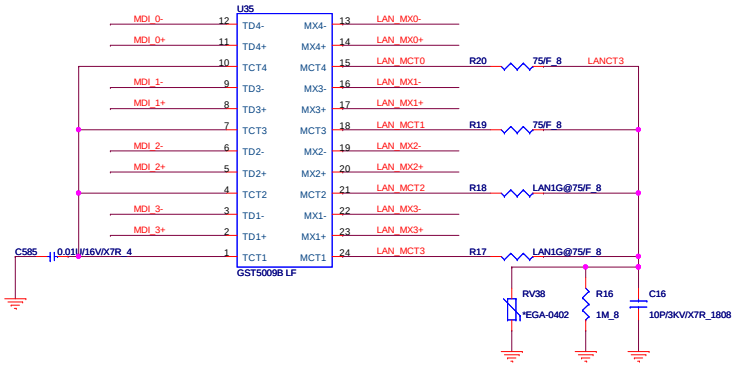


* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

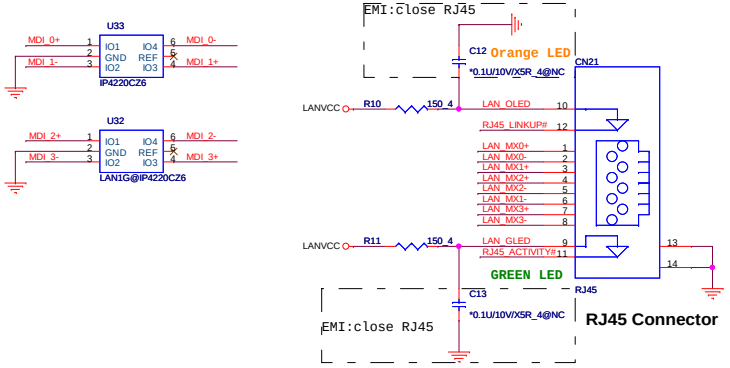
Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.

Layout:All termination signal should have 20 mil trace

Tramsformer



RJ45 Connector



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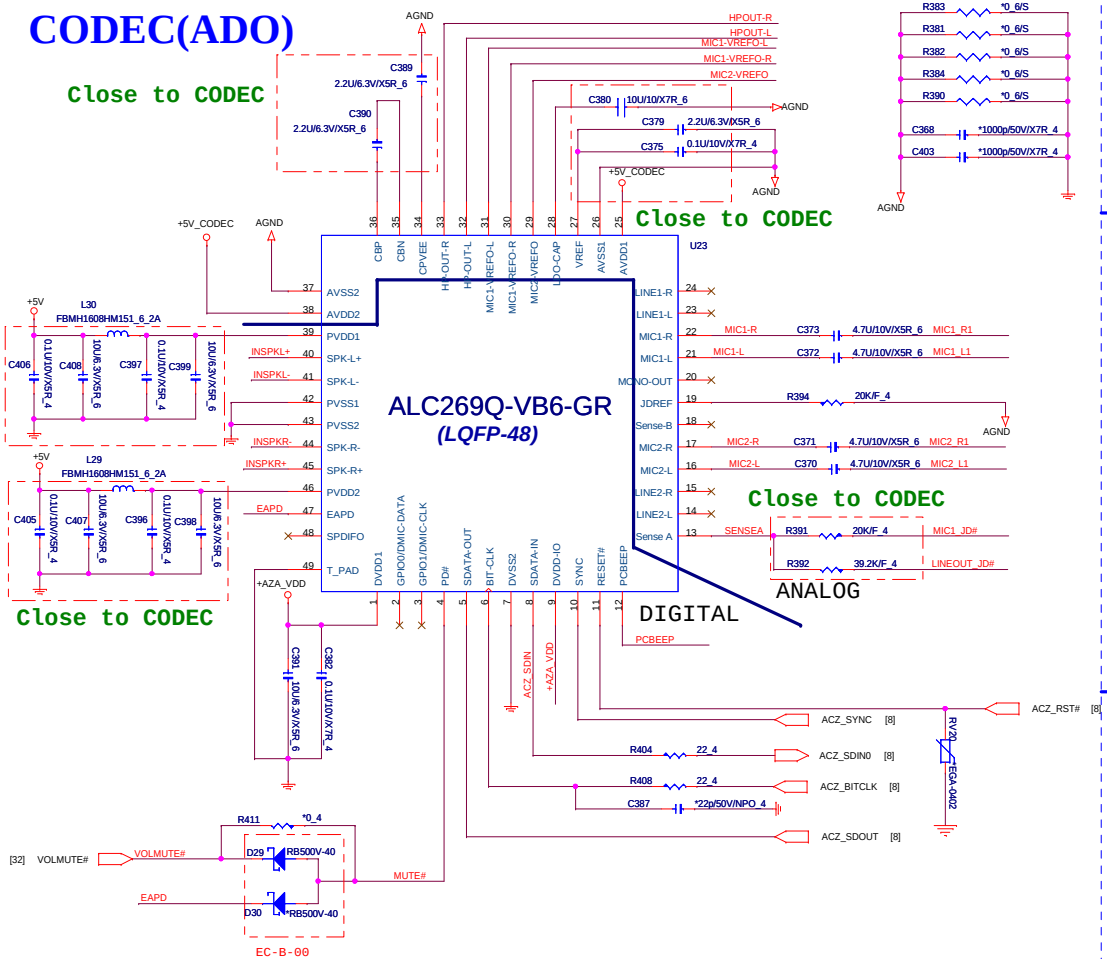
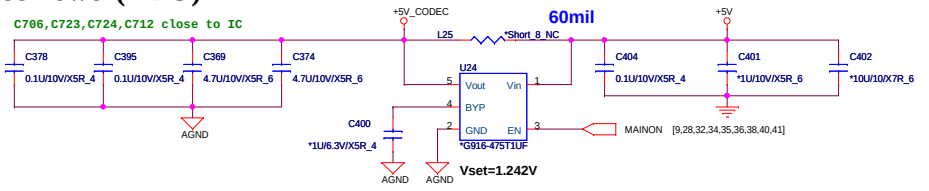
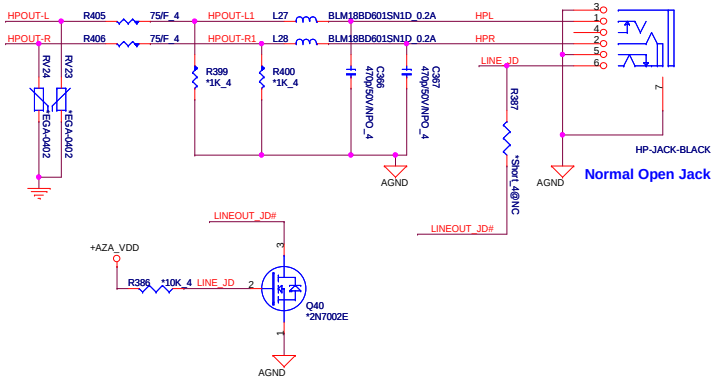
CODEC(ADO)



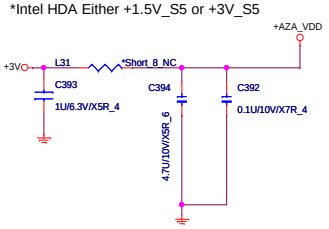
Codec Power(ADO)



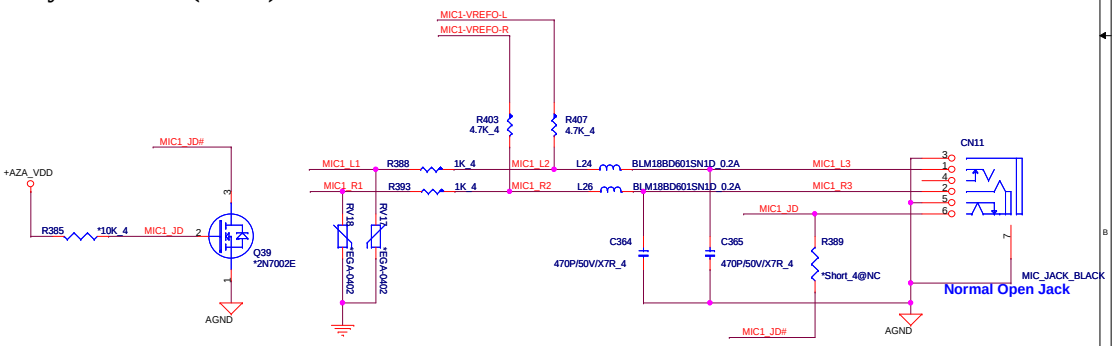
Earphone(AMP)



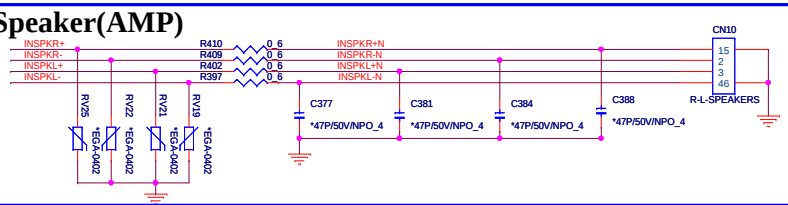
HDA Power(ADO)



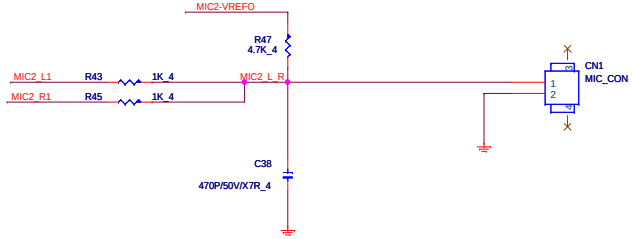
System MIC(AMP)



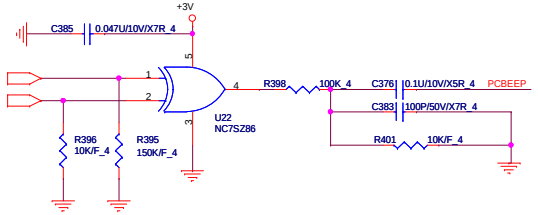
Speaker(AMP)



INTERNAL MIC



PC BEEP



PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ALC269/MIC/Line out	1A

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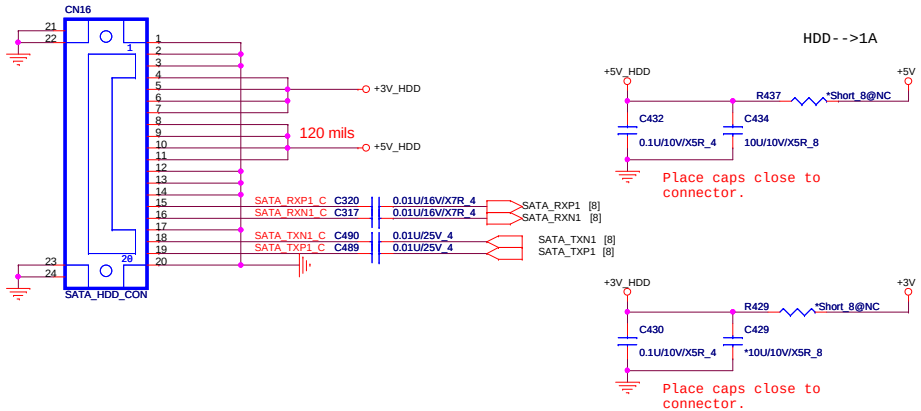
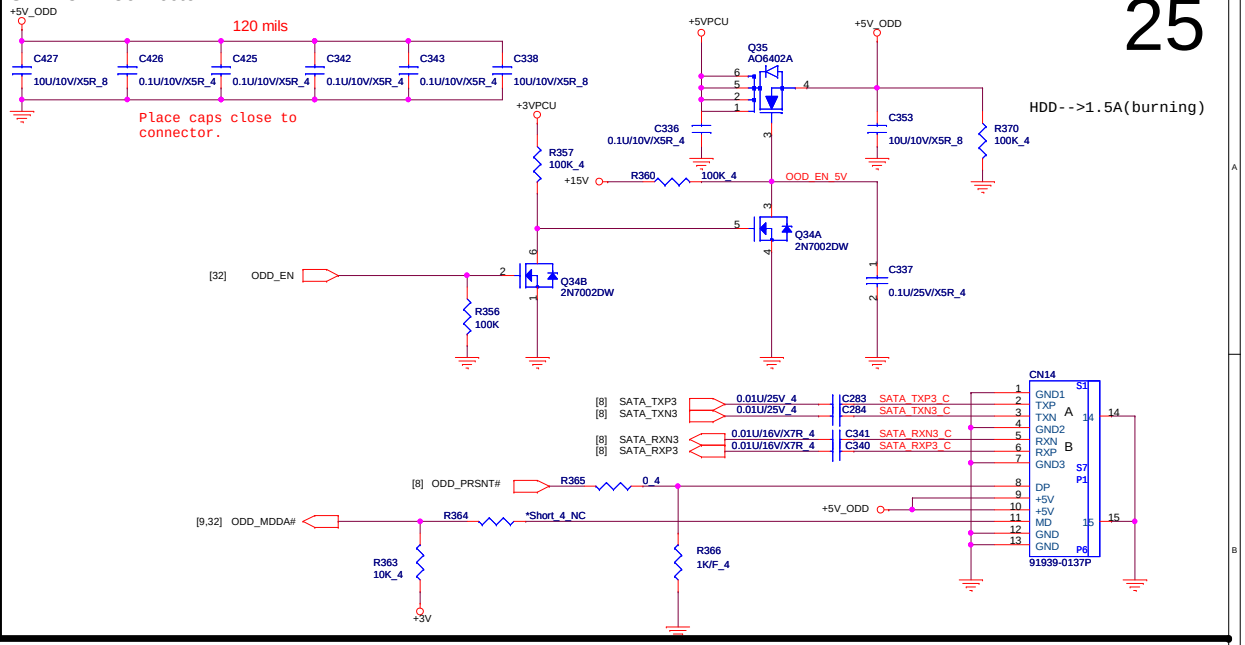
SATA HDD Connector.

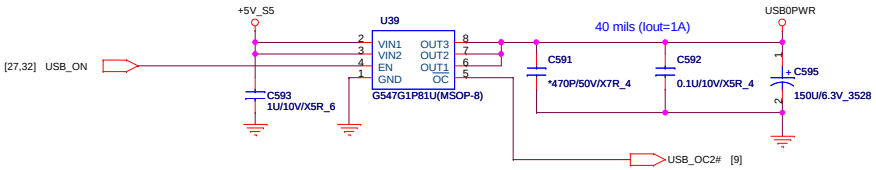


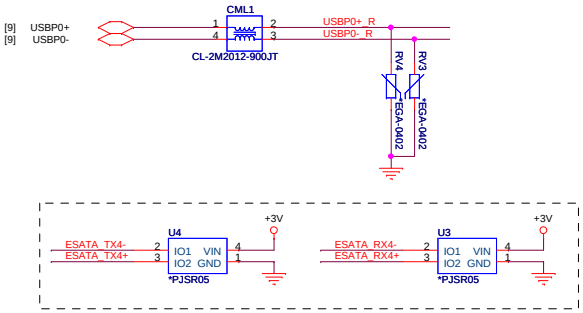
SATA ODD Connector.



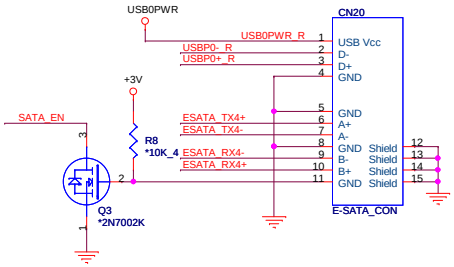
USB + E-SATA

Modify to GMT H-active

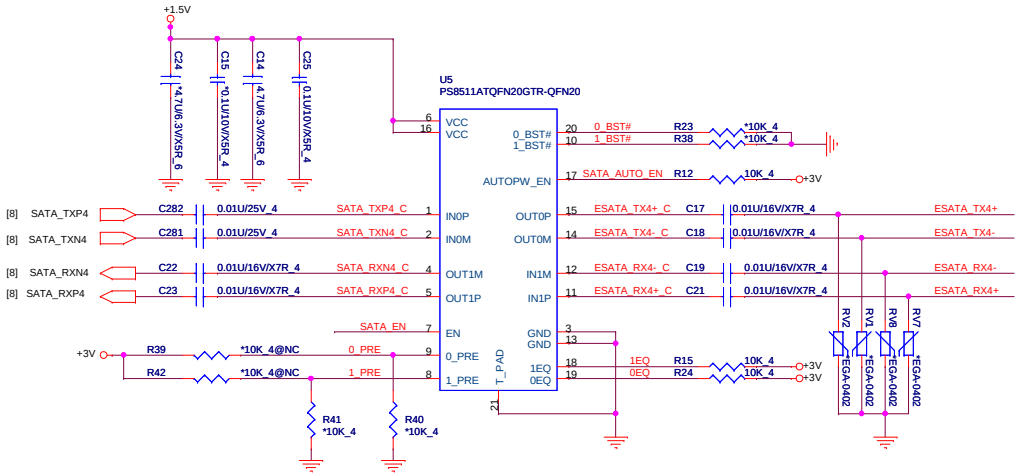




USB 0



E-SATA RE-DRIVER



Layout: Locate this IC near to conn 2~3 inch,and it can away PCH above 10 inch.

Straps notice:
1. SATA 3G-->600mV ; 0/1 BST#-->H
2. If input length is over 7 inch ; 0/1EQ-->H

Int.PH(150Kohm) : EN,0/1_BST#
Int.PL(150Kohm) : AUTO_EN,0/1EQ,0/1_PRE

EN	AUTO_EN	0/1EQ	0/1EQ	0/1_BST#	0/1_BST#	0/1_PRE	0/1_PRE	Function
0	X	X	X	X	X	X	X	Standby
1	0	X	X	X	X	X	X	disable auto power saving
1	1	X	X	X	X	X	X	enable auto power saving
1	X	0	X	X	X	X	X	Short and medium length
1	X	X	1	X	X	X	X	Long length
1	X	X	X	0	X	X	X	Output :800~1200 mVpp
1	X	X	X	X	1	X	X	Output :400~700 mVpp
1	X	X	X	X	X	0	X	Pre-emphasis disabled
1	X	X	X	X	X	X	1	Pre-emphasis enabled

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/ESATA/CD-ROM	1A

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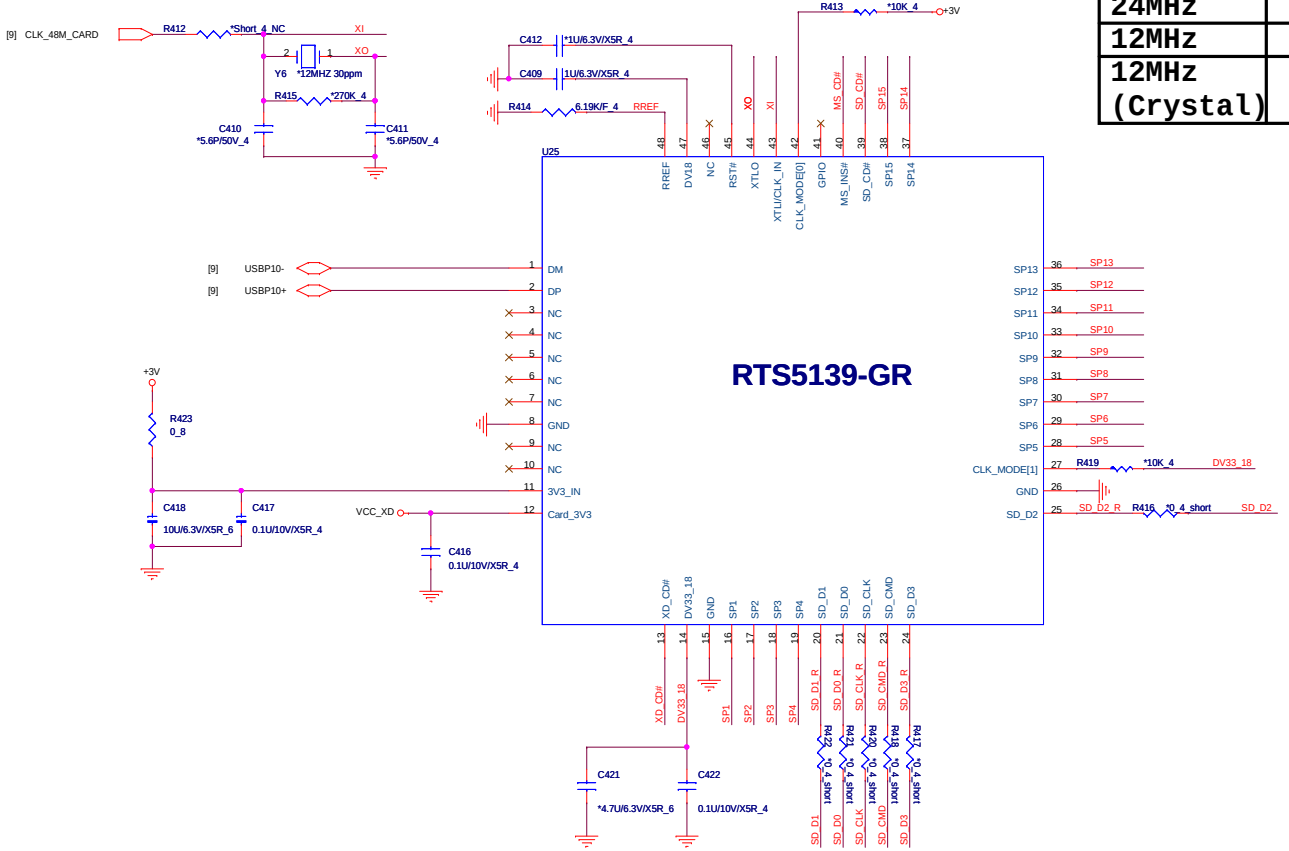
Clock Mode strap	R9287	R9307
48MHz	×	×
24MHz	×	○
12MHz	○	×
12MHz (Crystal)	○	○

Note:

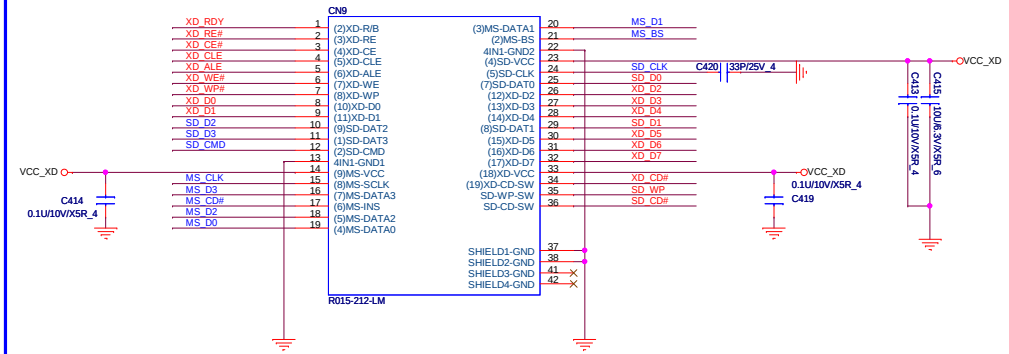
SD/MMC	MS	XD
SP1 SD_D7		XD_RDY
SP2 SD_D6		XD_RE#
SP3 SD_D5		XD_CE#
SP4 SD_D4		XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15 SD_WP		XD_D7

For RTS5139
SD,MS 4bit only



EC-B-05

7 IN1 CARD CONN
XD,MMC/SD,MS/MSP



PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Card Reader (RTS5159)	1A

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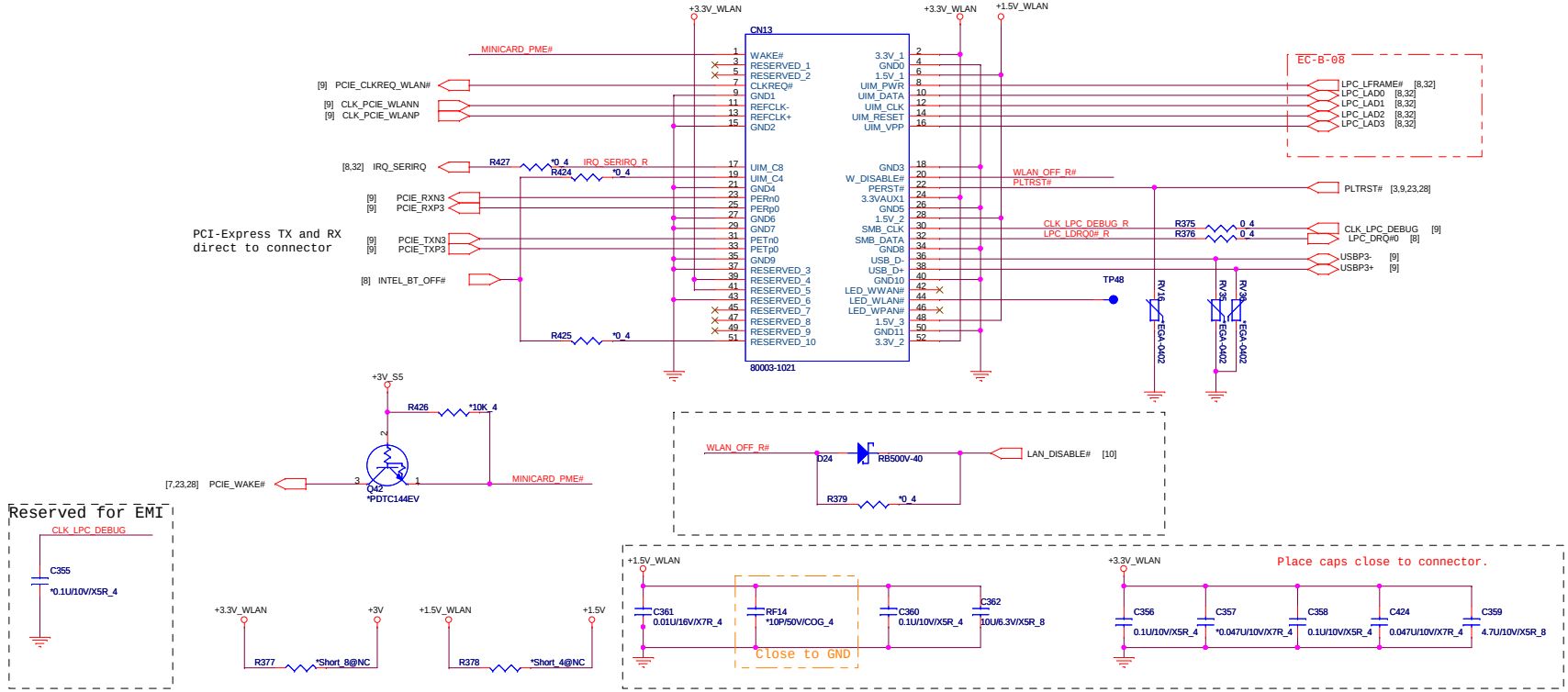
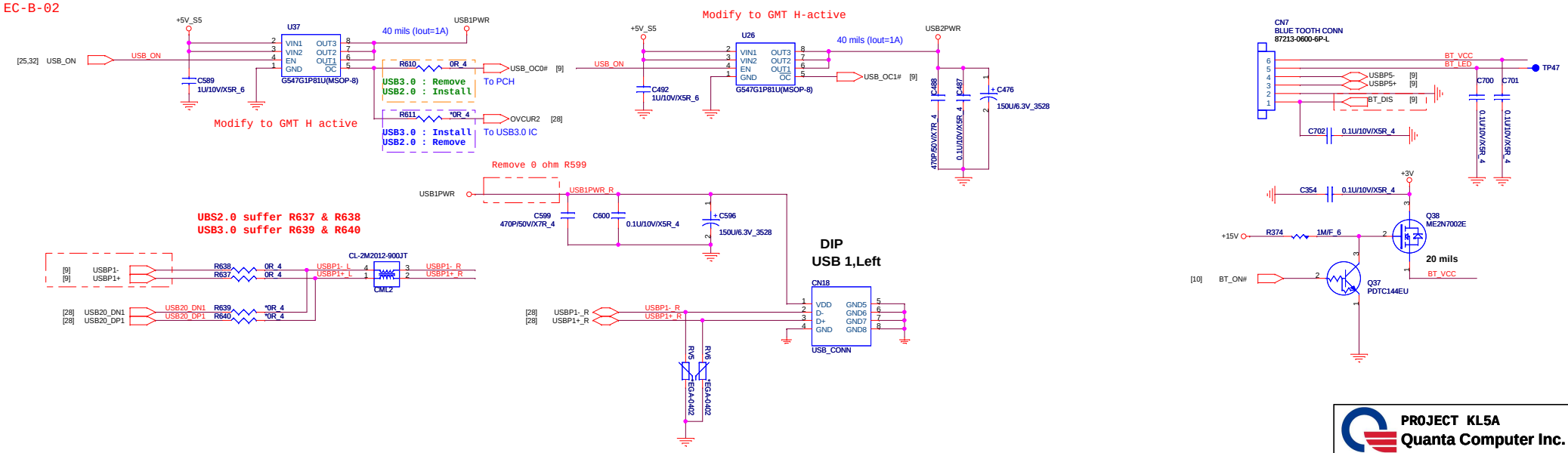
MiniCard WLA connector



USB2.0*1

EC-B-02



BLUETOOTH

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB2.0*1/WLAN/BT	1A

Date: Friday, October 29, 2010 Sheet 27 of 45

SPI Flash ROM

U40 EN25F05-100GIP

Copy From ZN7

U41 VL800 / VL801 QFN88

VL800 4PORT
VL801 2PORT

Remove power for VL801

For debug only.
Don't connect to system SMBus

Near PCIEx Slot

C608, C610 need close to pin8, 9 of CN23

ESD

U42 *RClamp0544.TBT msop10-4_9-5

USB3.0 PORT1

CN23 USB3.0 CONN

C608, C610 close to CN23

SUY USB3.0: DFHS09FR063
SUY USB2.0: DFHS04FR455

X'tal 25MHz

Y7 25MHz/20pF/30ppm

Crystal foot print must be reserved in case 25MHz clock from clock generator is not stable enough.

For +3V_S5 (Power for wake up)

For +3V_RUN

For +1.05_SUS (Power for wake up)

Power sequence for Host.

Power circuit (+1.05_SUS) For USB3.0

U43 G9661-25ADJF12U

Vout =0.8(1+R1/R2)

For USB3.0

Remove SUSD turn on switch (From PCU to SUS)
(Used +3V_S5 power plane)

PROJECT	KL5A
Quanta Computer Inc.	
Size	C
Document Number	USB3.0 *1
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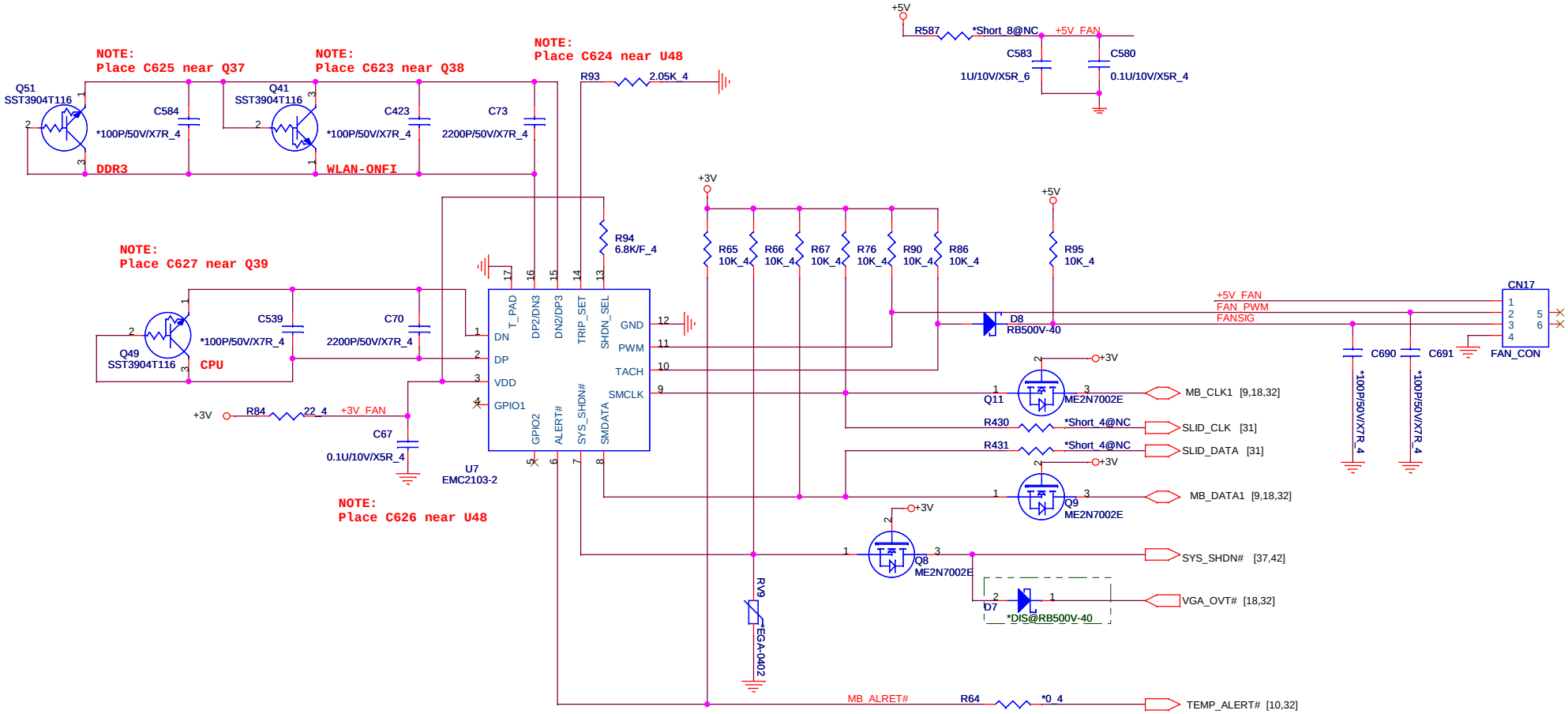
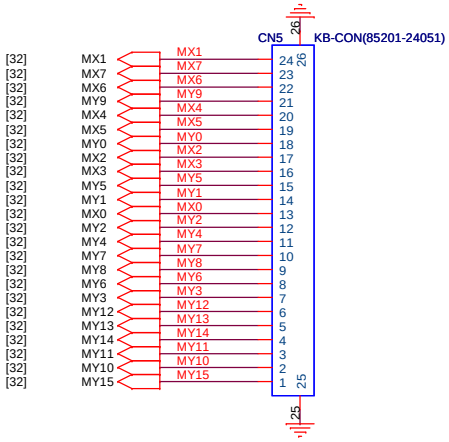
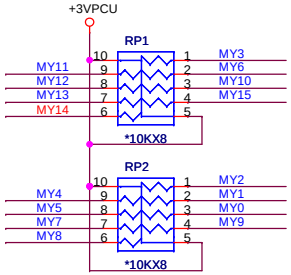
FAN CONTROL

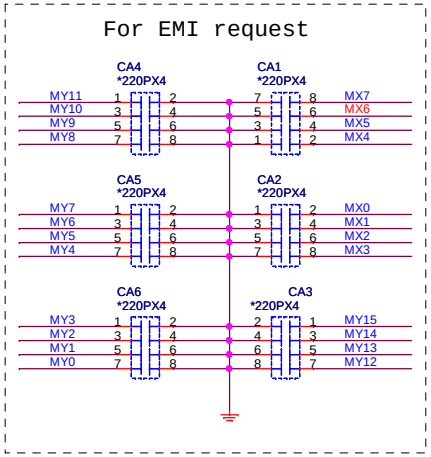


PROJECT KL5A Quanta Computer Inc.		
Size B	Document Number FAN /THERMAL	Rev 1A
Date: Friday, October 29, 2010	Sheet 29 of 45	

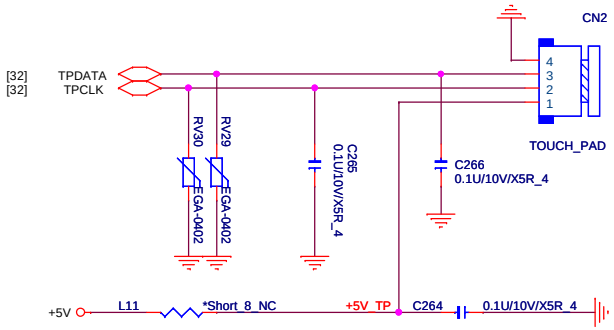
KEYBOARD







Touch pad



PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	K/B, T/P	1A
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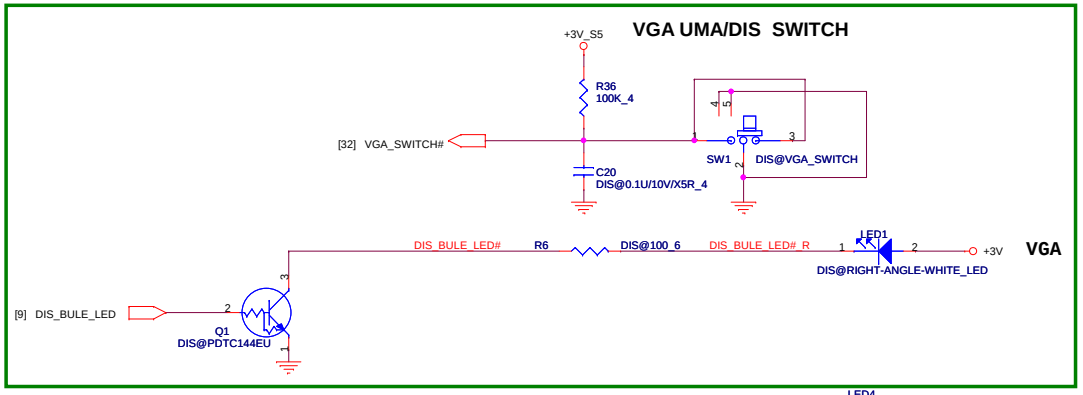

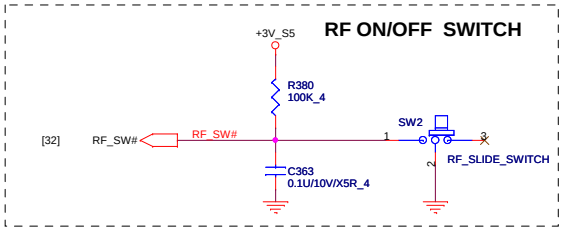

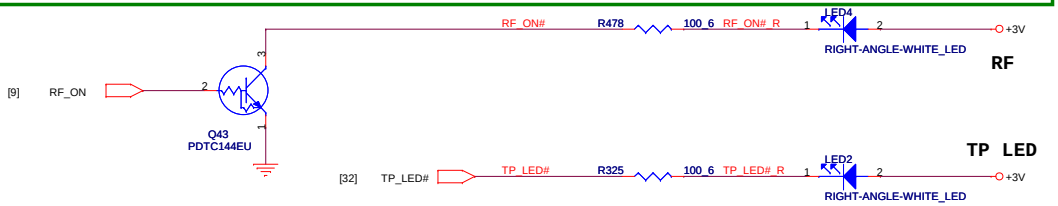

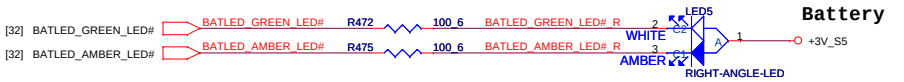

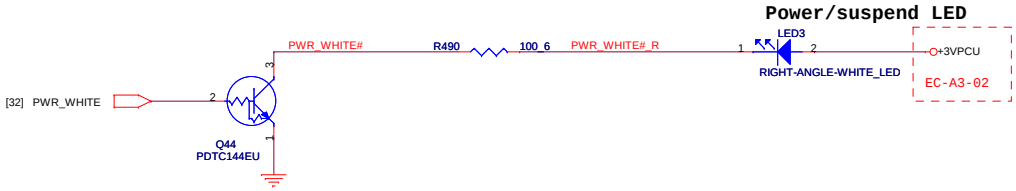

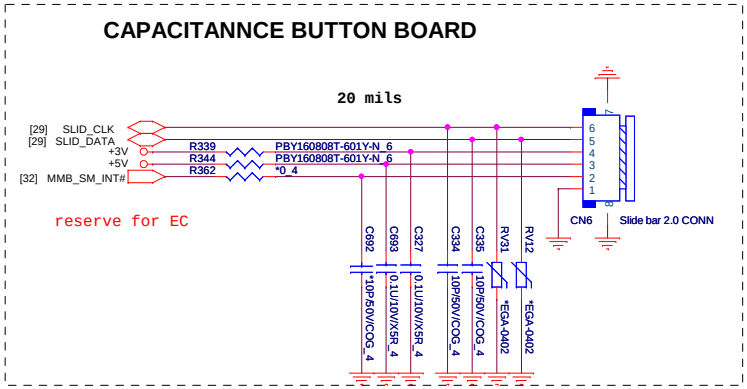

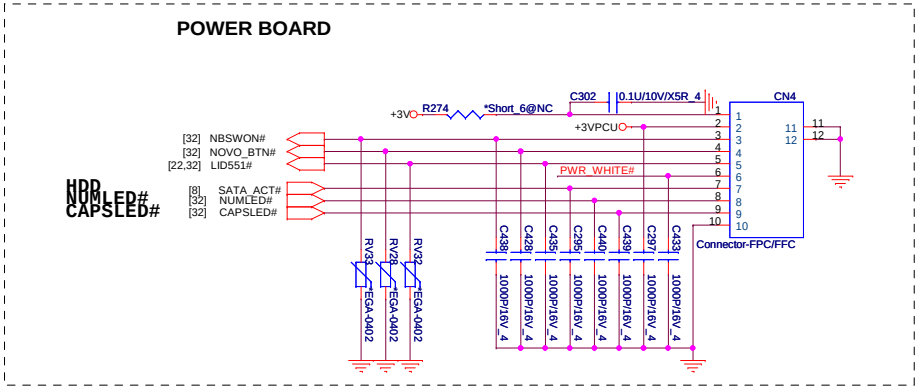

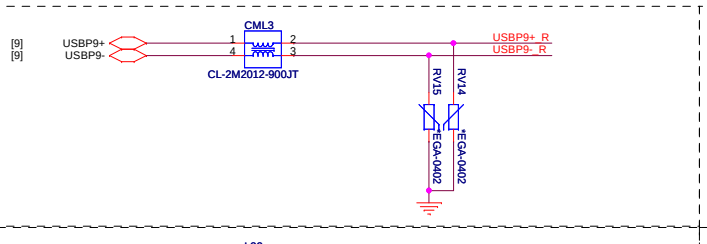

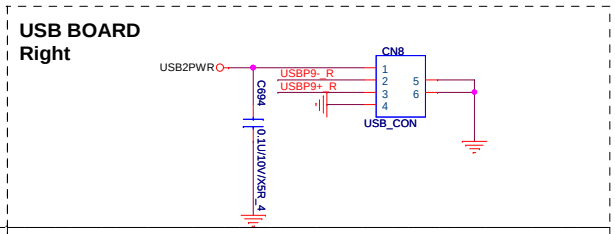

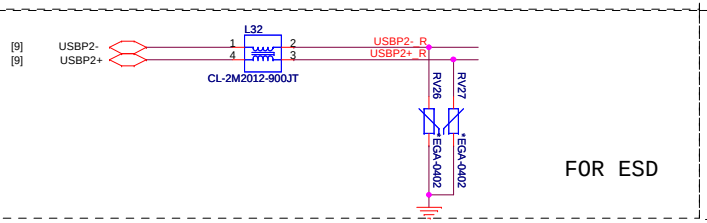

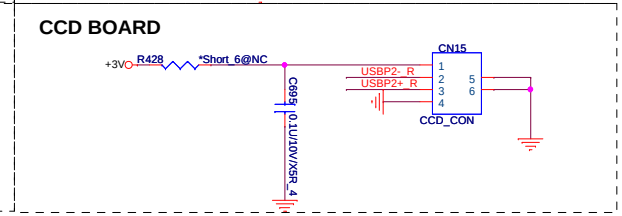

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	B TO B CON/LED	1A
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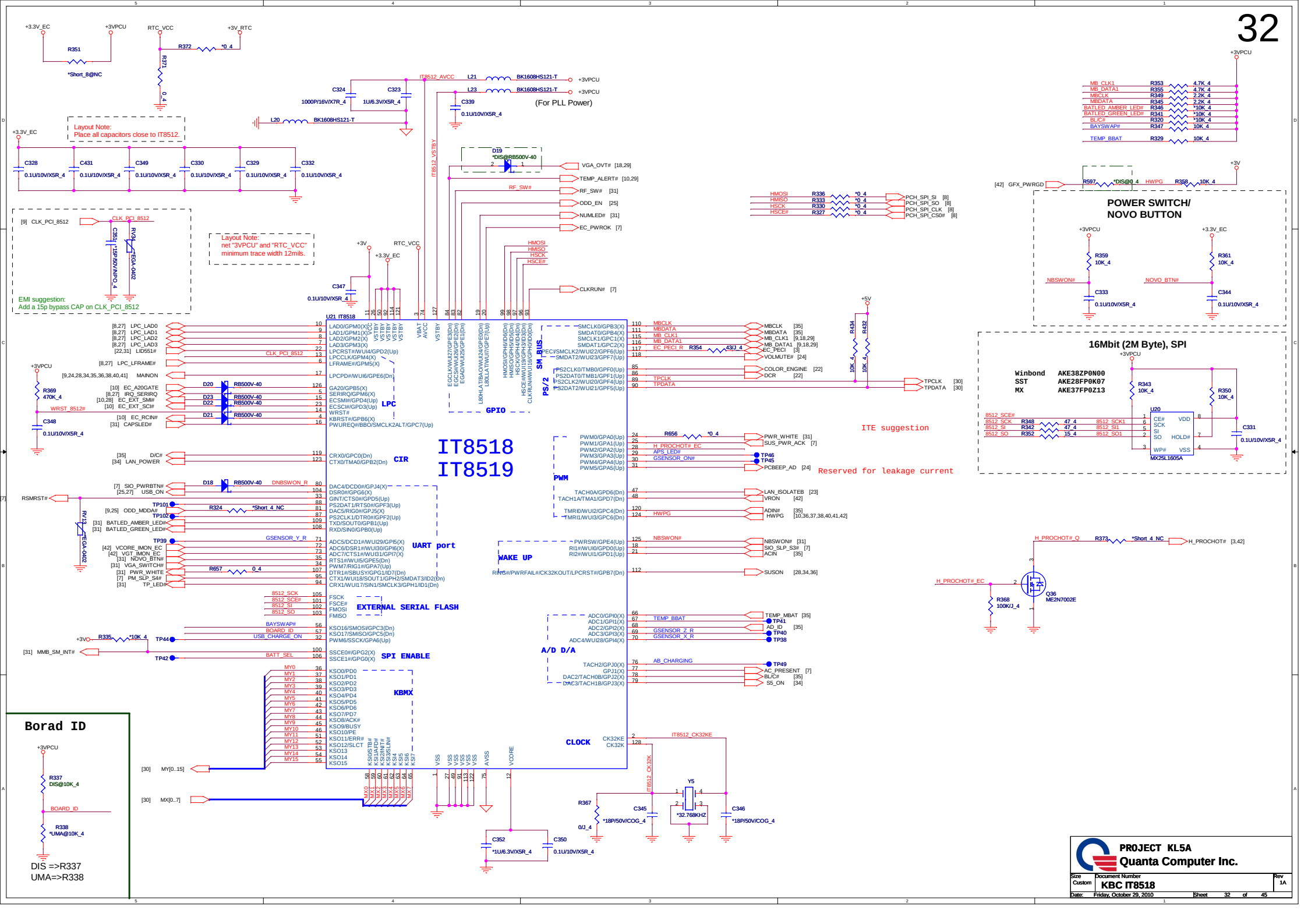
IT8518
IT8519
U21 IT8518
LPC
GPIO
SM BUS
PS/2
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
CIR
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512
(For PLL Power)
ITE suggestion
Reserved for leakage current
POWER SWITCH/
NOVO BUTTON
16Mbit (2M Byte), SPI
Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13
Borad ID
DIS =>R337
UMA=>R338
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Quanta Computer Inc.
KBC IT8518
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Screw for ME

WLAN

HOLE11 C142D102N
HOLE10 C142D102N

SMT GUIDE H=4mm	PN: MBIM3001010
SMT NUT H=4mm	PN: MBIM3002010

VGA

HOLE13 C41D2N
HOLE12 DIS@C41D2N

SMT NUT H=5.1mm	PN: MBKL6001010

ME-other holes

圓型螺孔(8個衛兵孔)*7 for ESD

HOLE8, HOLE5, HOLE1, HOLE7, HOLE2, HOLE9 — *holes_p_r276d118

Connect to AGND for ESD

AGND

HOLE6 *C41D2N
HOLE4 *C41D2N
HOLE3 *C41D2N
NPTH

CPU BKT

BKT1 (PTH) 4 3 2
cpu-bracket 1

non-connect GND for ESD

Pad for Layout mask

PAD1 *PAD1
PAD2 *PAD2
PAD3 *PAD3
PAD4 *PAD4
PAD5 *PAD5
PAD6 *PAD6
PAD7 *PAD7

EMI

VIN
EC31 2 0.1U/50V/X7R_6
EC51 2 0.1U/50V/X7R_6
EC81 2 0.1U/50V/X7R_6
EC18 2 0.1U/50V/X7R_6
EC13 2 0.1U/50V/X7R_6
EC12 2 0.1U/50V/X7R_6
EC15 2 0.1U/50V/X7R_6
EC14 2 0.1U/50V/X7R_6
EC11 2 0.1U/50V/X7R_6

+VCC_GFX
EC22 2200P/50V/X7R_4
EC23 0.1U/25V/X5R_4

ESD

EC-B-10

VIN
EC20 1 2 0.1U/50V/X7R_6
EC21 1 2 0.1U/50V/X7R_6

VIN +VCC_CORE
SC19 *0.1U/25V/X5R_4

VIN
SC24 *0.1U/25V/X5R_4
SC25 *0.1U/25V/X5R_4

VIN +1.5V_SUS
SC4 0.1U/25V/X5R_4
SC5 0.1U/25V/X5R_4
SC23 0.1U/25V/X5R_4

VIN +1.5V_GPU
SC21 0.1U/25V/X5R_4
SC22 0.1U/25V/X5R_4

VIN +5V_S5
SC26 0.1U/25V/X5R_4
SC27 0.1U/25V/X5R_4

GFX_CORE +1.5V_SUS
SC1 *0.1U/10V_4

GFX_CORE +1.5V_GPU
SC14 *0.1U/10V_4

+0.85V +1.05V_PCH
SC6 *0.1U/10V_4
SC7 *0.1U/10V_4
SC8 *0.1U/10V_4
SC10 *0.1U/10V_4
SC12 *0.1U/10V_4

+1.5V_SUS
SC2 *0.1U/10V_4
SC13 *0.1U/10V_4
SC17 *0.1U/10V_4
SC18 *0.1U/10V_4

+0.85V
SC3 *0.1U/10V_4

+1.05V_PCH
SC9 *0.1U/10V_4
SC15 *0.1U/10V_4
SC16 *0.1U/10V_4

+1.05V_PCH +1.5V_SUS
SC11 *0.1U/10V_4

+VCC_CORE
SC20 *0.1U/10V_4

VIN +5V
SC28 *0.1U/25V/X5R_4

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
B	Screw hole/EMI/ESD	1A

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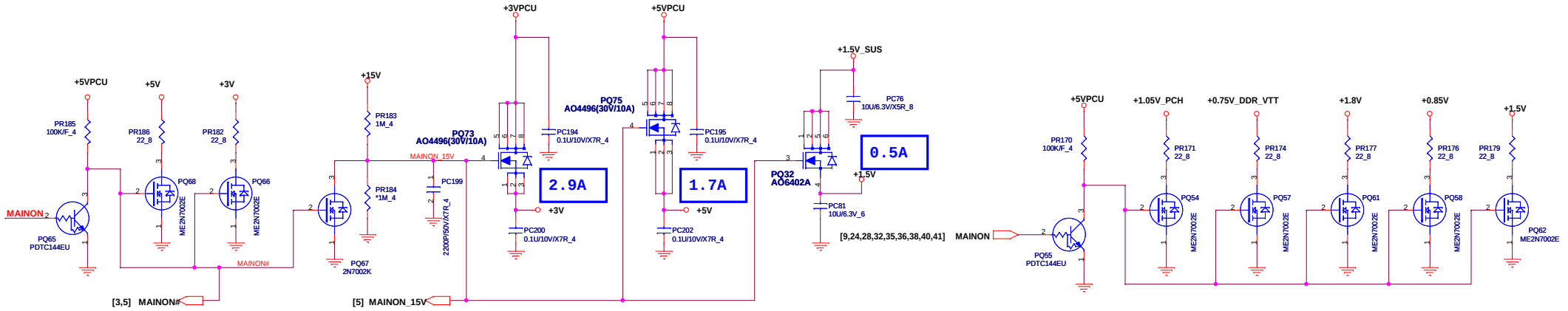
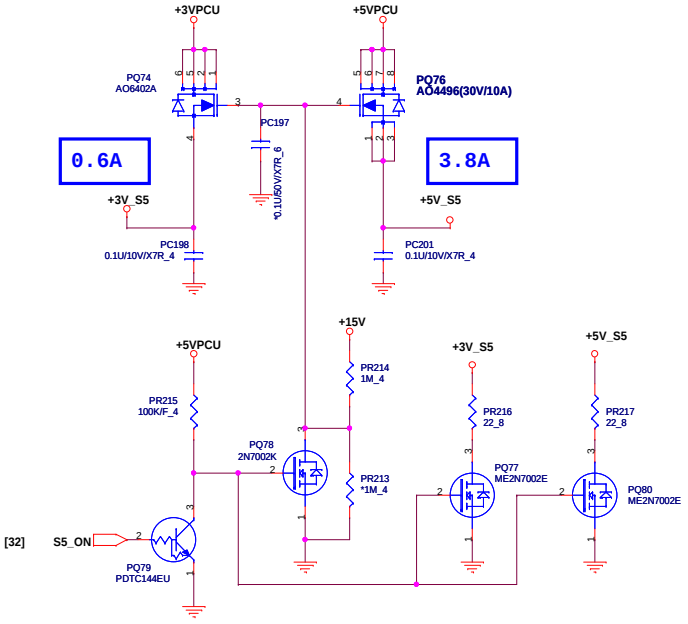
DISCHARGE

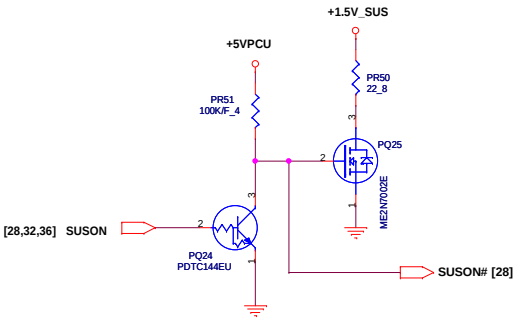
+3V, +5V,1.5V



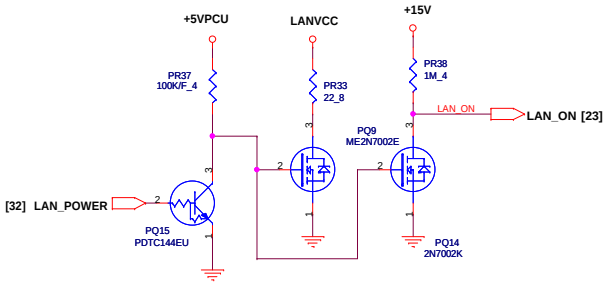
3V_S5, 5V_S5

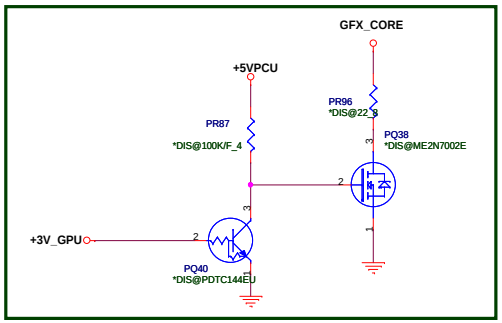


B-00



LANVCC





PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	1A

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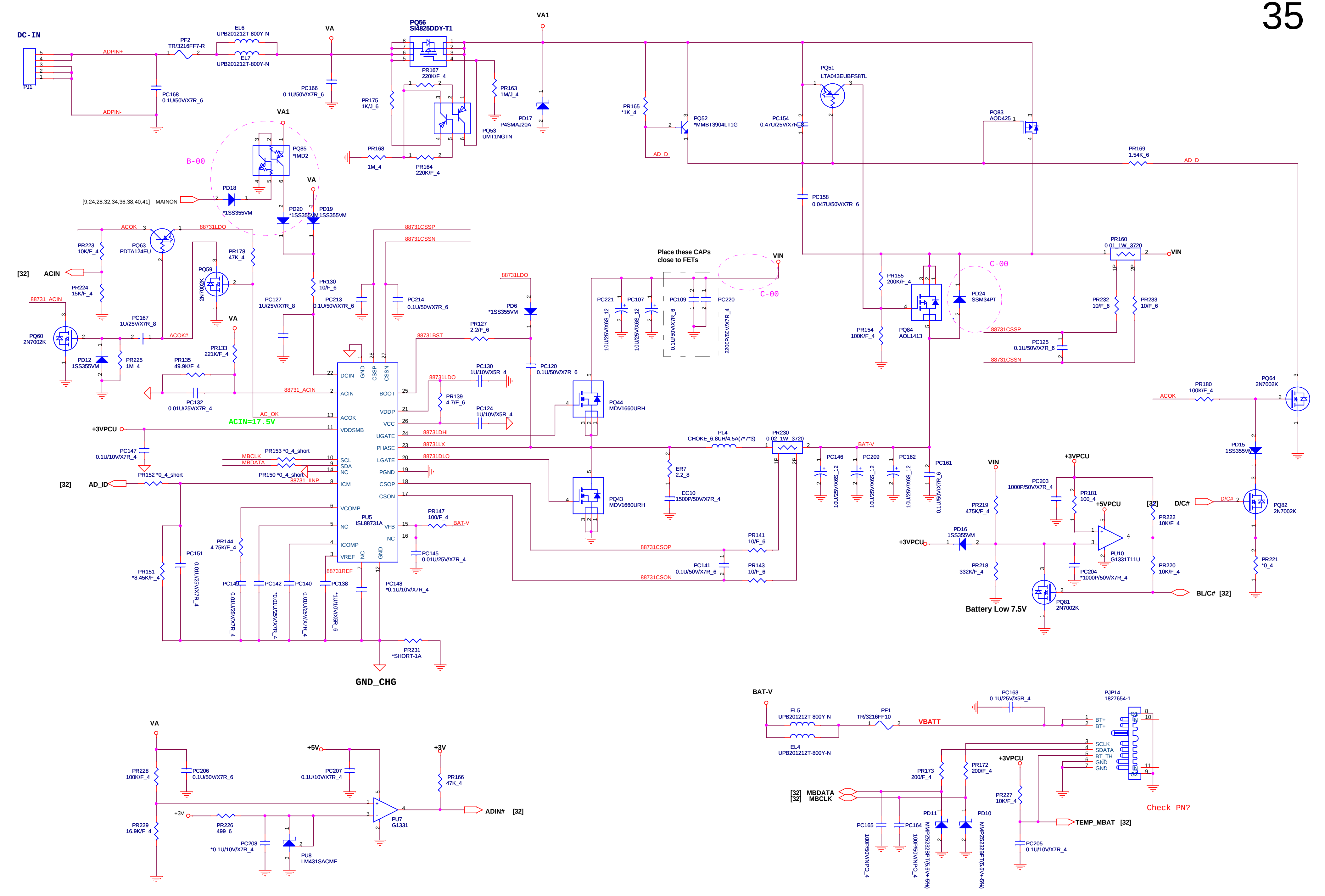

PROJECT KL5A	Quanta Computer Inc.	
Size: Custom	Document Number: Charger (ISL88731A)	Rev: 1A
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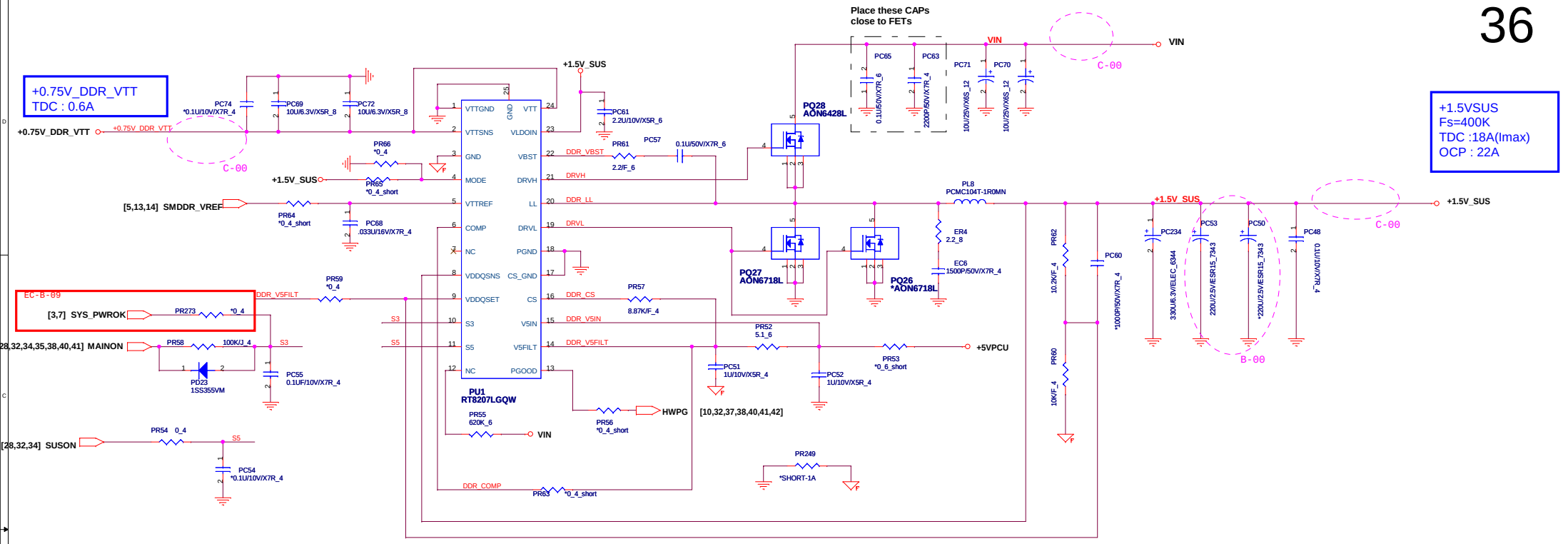

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3/0.75V(RT8207LGQW)	1A

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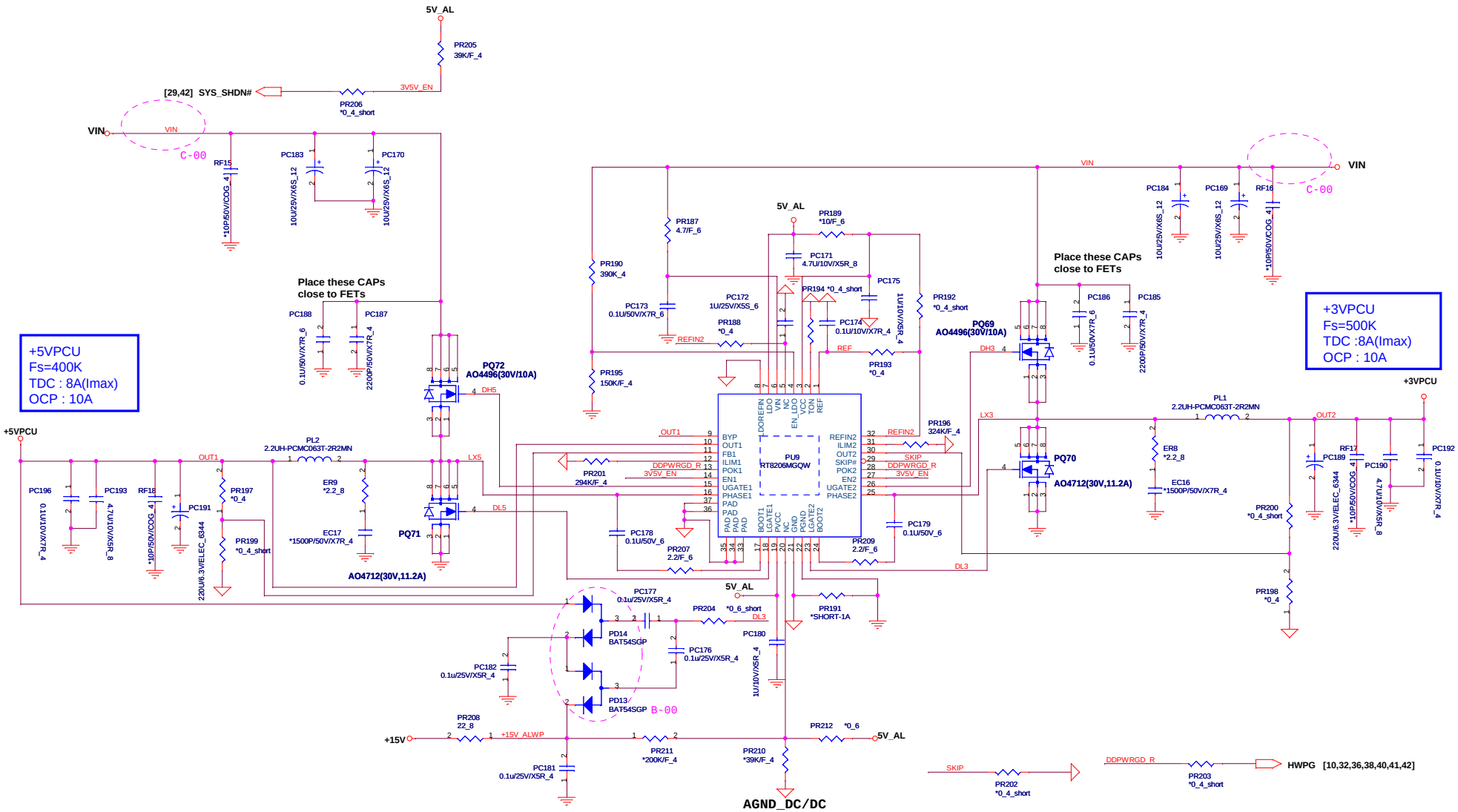
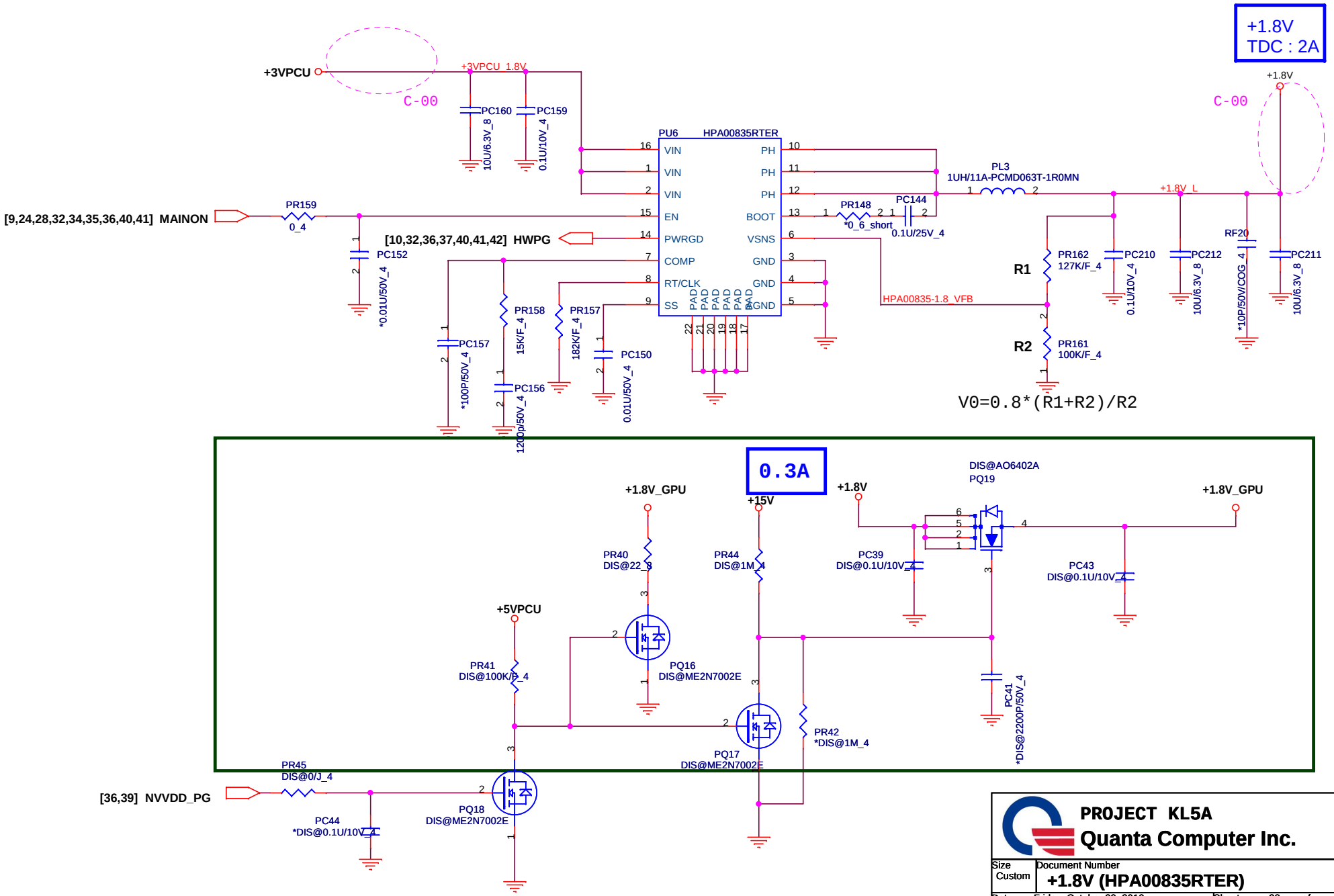


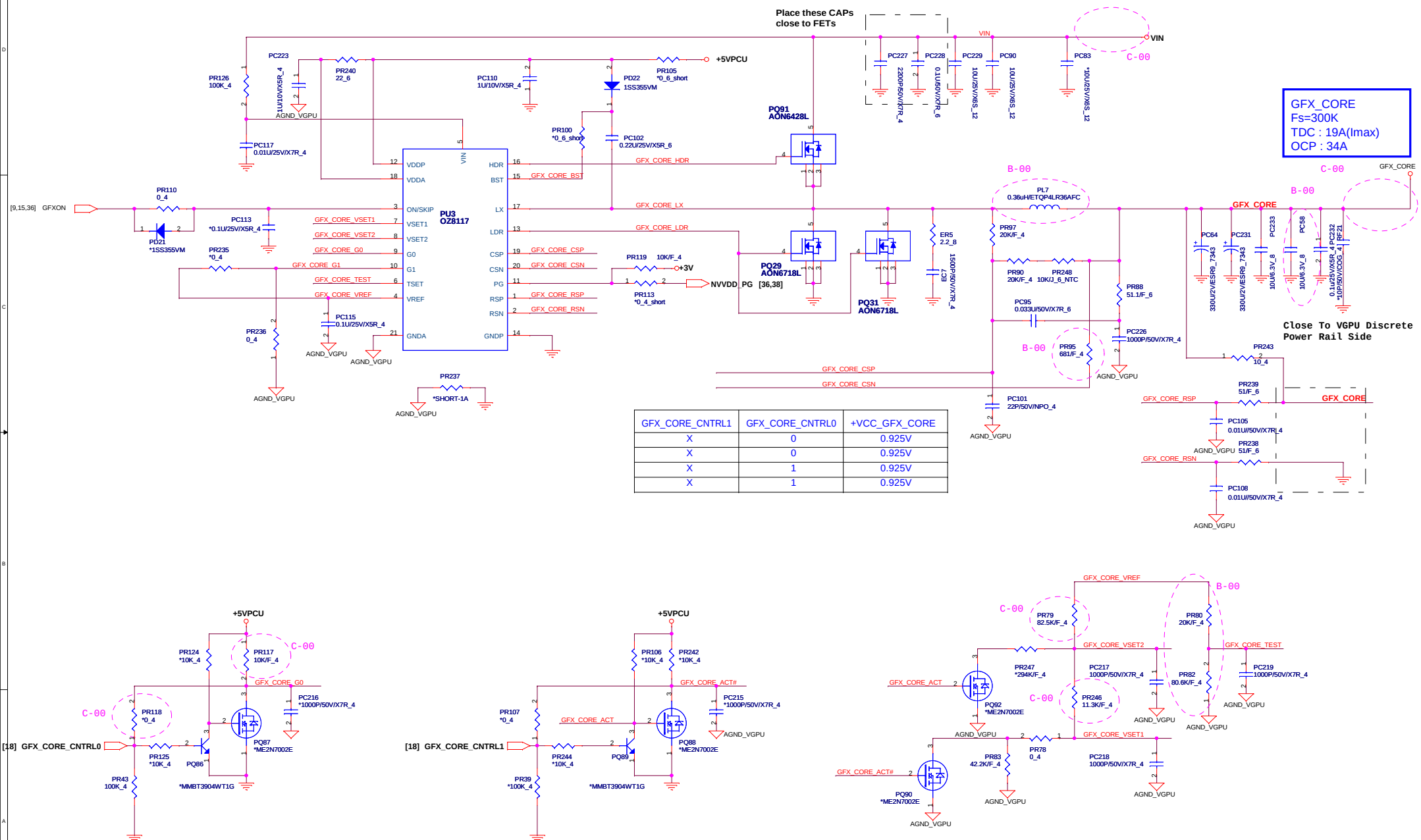
PROJECT KL5A			
Quanta Computer Inc.			
Size: Custom	Document Number: 3V/5V (RT8206MGQW)		Rev: 1A
Date: Friday, October 29, 2010	Sheet 37 of 45		



PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.8V (HPA00835RTER)	1A

Date: Friday, October 29, 2010 Sheet 38 of 45



GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VCC_GFX_CORE
X	0	0.925V
X	0	0.925V
X	1	0.925V
X	1	0.925V

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGPU_CORE (OZ8117)	1A

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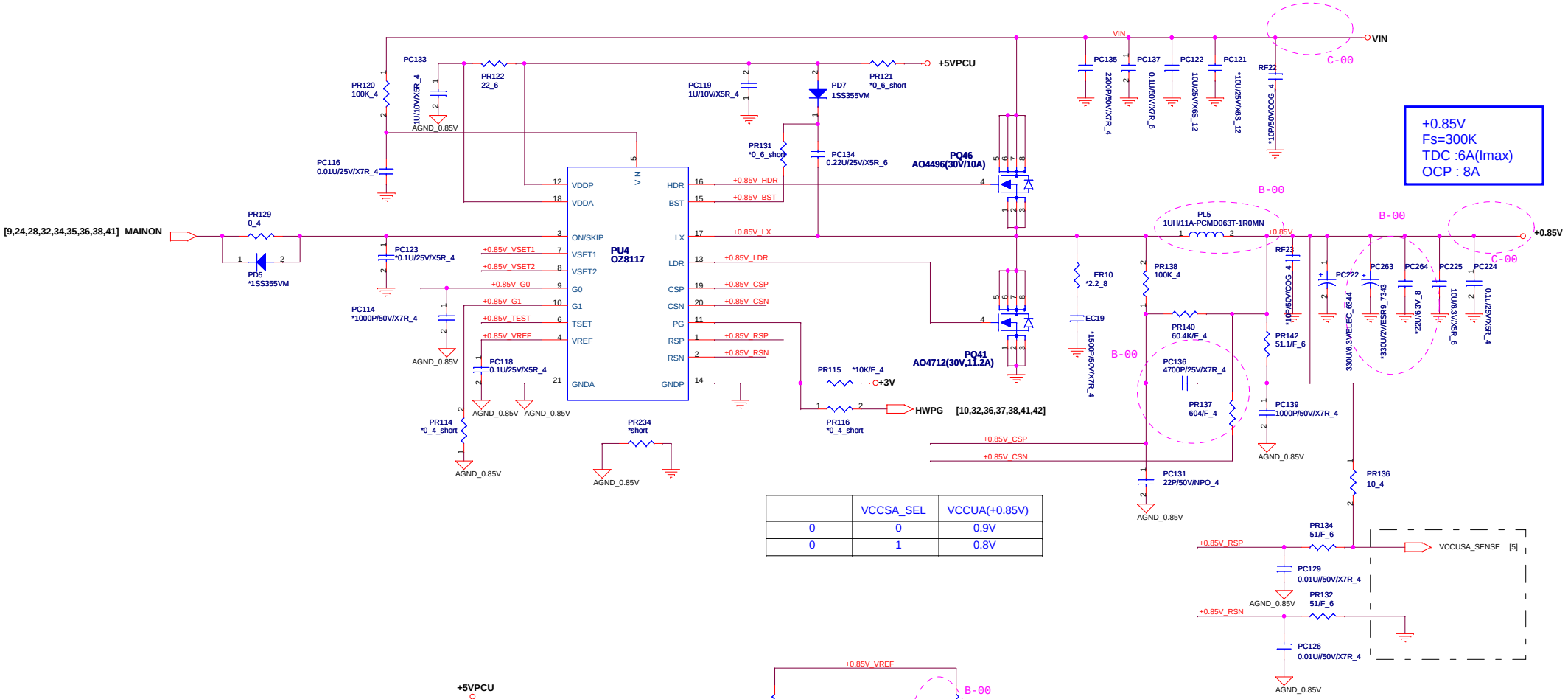

	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+0.85V (OZ8117)	1A

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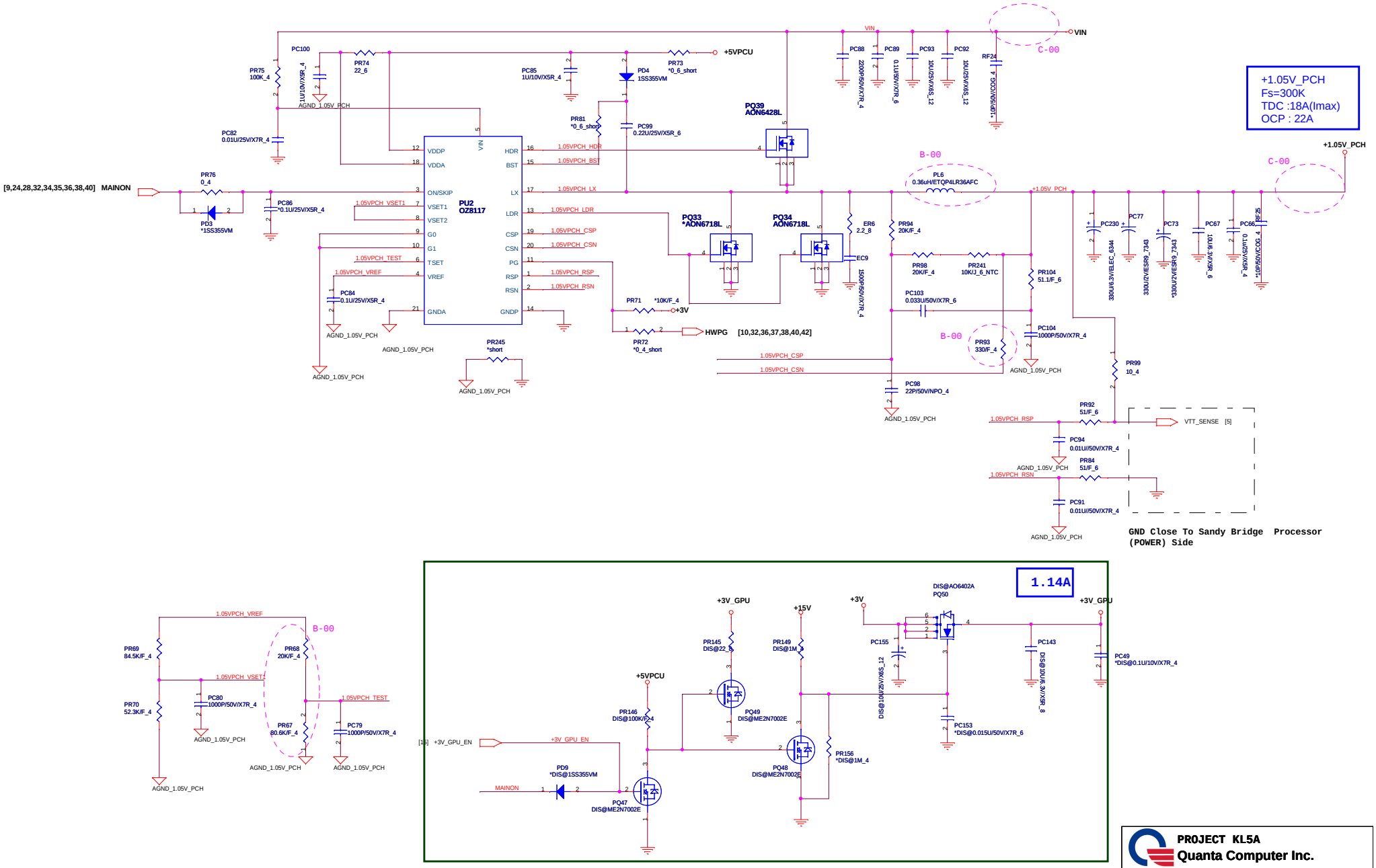
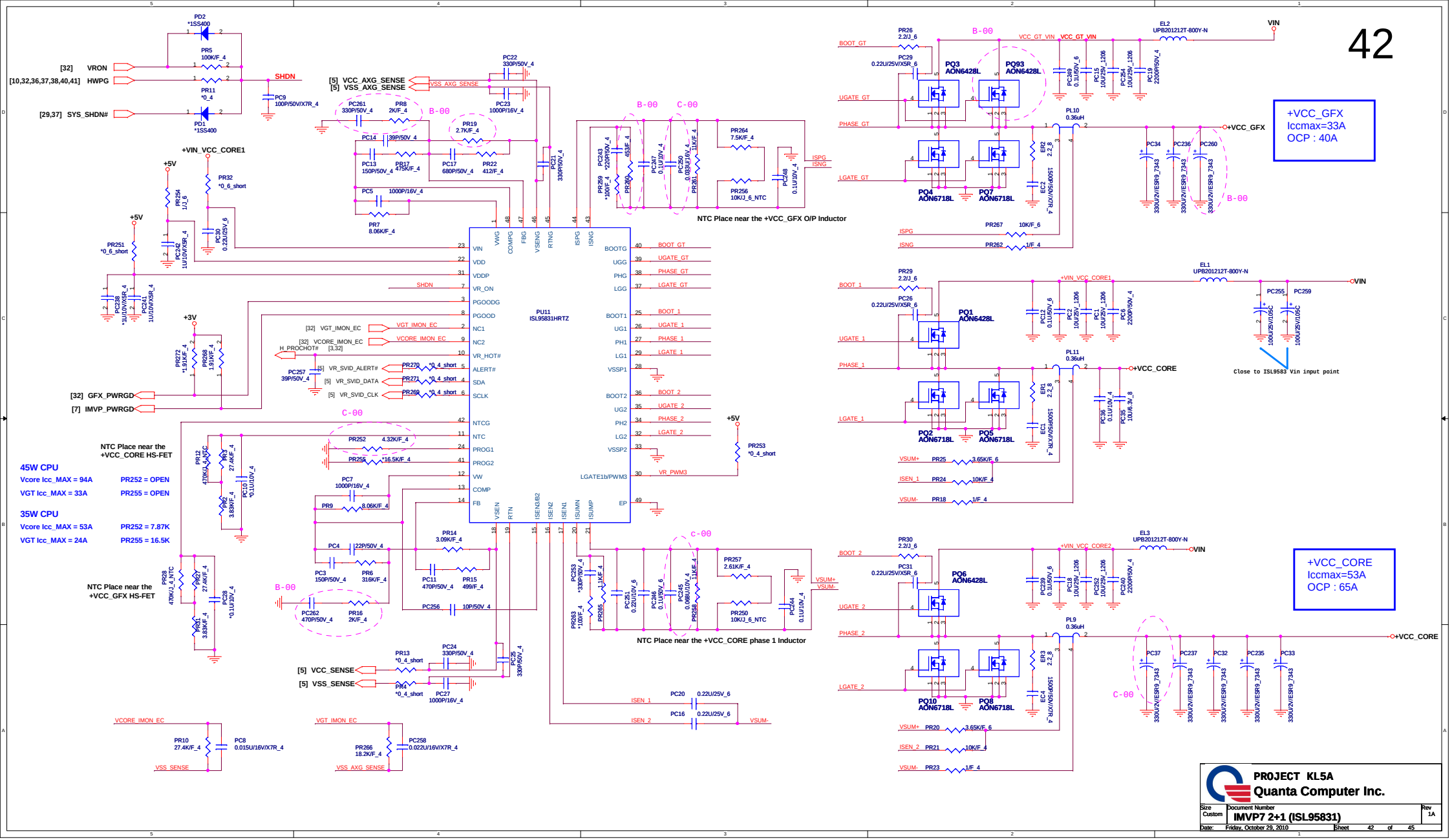

+1.05V_PCH
Fs=300K
TDC :18A(Imax)
OCP : 22A
PU2
OZ8117
PQ39
AON6428L
PQ33
*AON6718L
PQ34
AON6718L
PL6
0.36uH/ETQP4LR36AFC
[9,24,28,32,34,35,36,38,40] MAINON
+5VPCU
VIN
+3V
HWPG [10,32,36,37,38,40,42]
B-00
C-00
GND Close To Sandy Bridge Processor (POWER) Side
1.14A
+3V_GPU
+15V
DIS@AO6402A
PQ50
PROJECT KL5A
Quanta Computer Inc.
+1.05_PCH (OZ8117)
Friday, October 29, 2010
Sheet 41 of 45


PU11
ISL95831HRTZ
VIN
VDD
VDDP
VR_ON
PGOODG
PGOOD
NC1
NC2
VR_HOT#
ALERT#
SDA
SCLK
NTCG
NTC
PROG1
PROG2
VW
COMP
FB
VSEN
RTN
ISEN3/B2
ISEN2
ISEN1
ISUMN
ISUMP
VWG
COMPG
FBG
VSENG
RTNG
ISPG
ISNG
BOOTG
UGG
PHG
LGG
BOOT1
UG1
PH1
LG1
VSSP1
BOOT2
UG2
PH2
LG2
VSSP2
LGATE1b/PWM3
EP
SHDN
VRON
HWPG
SYS_SHDN#
GFX_PWRGD
IMVP_PWRGD
VGT_IMON_EC
VCORE_IMON_EC
H_PROCHOT#
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
VCC_AXG_SENSE
VSS_AXG_SENSE
VCC_SENSE
VSS_SENSE
+VIN_VCC_CORE1
+5V
+3V
NTC Place near the +VCC_GFX O/P Inductor
NTC Place near the +VCC_CORE phase 1 Inductor
NTC Place near the +VCC_CORE HS-FET
NTC Place near the +VCC_GFX HS-FET
45W CPU
Vcore Icc_MAX = 94A
VGT Icc_MAX = 33A
PR252 = OPEN
PR255 = OPEN
35W CPU
Vcore Icc_MAX = 53A
VGT Icc_MAX = 24A
PR252 = 7.87K
PR255 = 16.5K
+VCC_GFX
Iccmax=33A
OCP : 40A
+VCC_CORE
Iccmax=53A
OCP : 65A
Close to ISL9583 Vin input point
PROJECT KL5A
Quanta Computer Inc.
IMVP7 2+1 (ISL95831)
Friday, October 29, 2010
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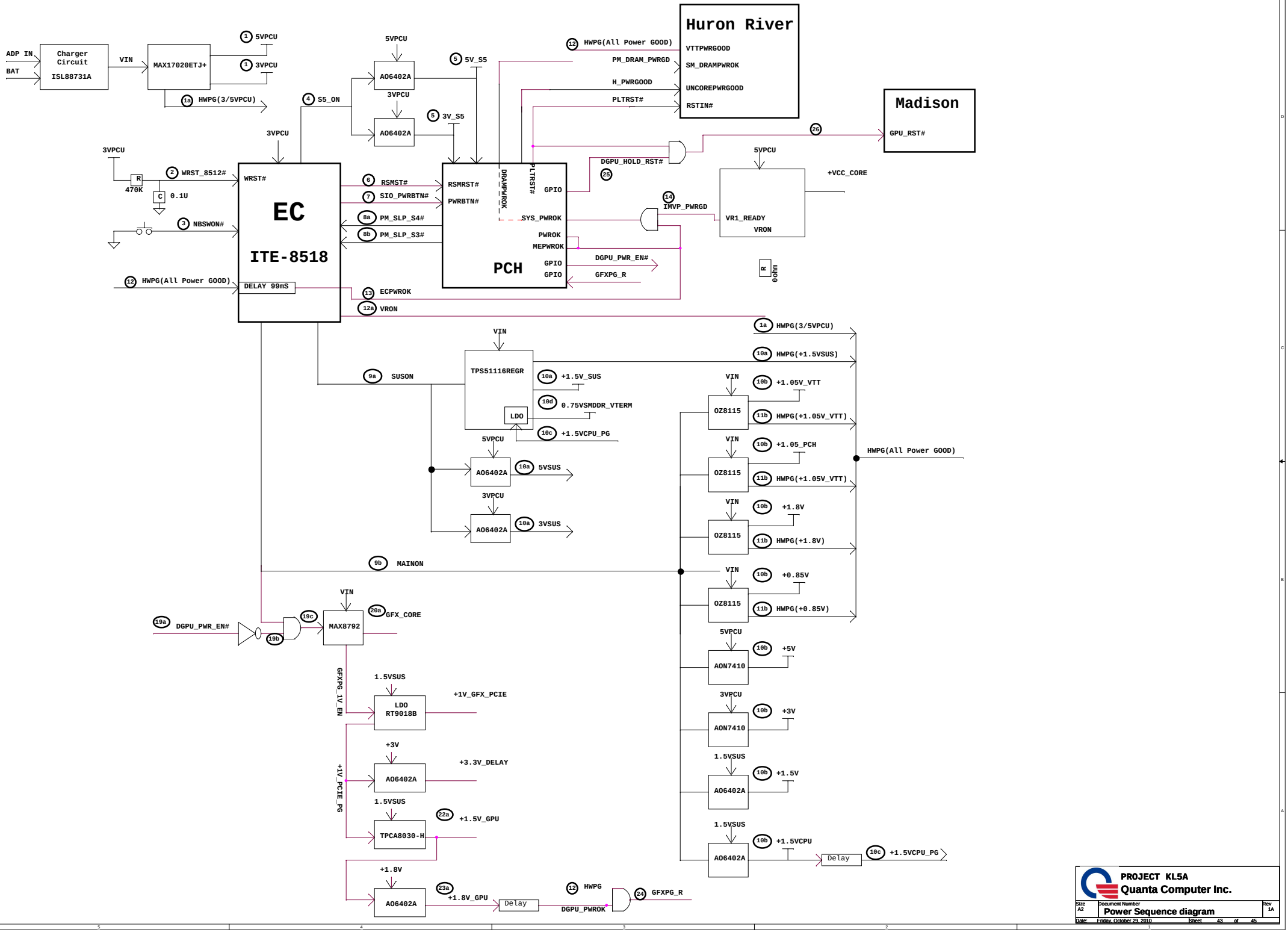
Huron River
VTTPWRGOOD
SM_DRAMPWROK
UNCOREPWRGOOD
RSTIN#
PM_DRAM_PWRGD
H_PWRGOOD
PLTRST#
HWPG(All Power GOOD)
Madison
GPU_RST#
ADP IN
BAT
Charger Circuit
ISL88731A
VIN
MAX17020ETJ+
5VPCU
3VPCU
HWPG(3/5VPCU)
S5_ON
AO6402A
5V_S5
3V_S5
EC
ITE-8518
WRST#
WRST_8512#
NBSWON#
RSMST#
SIO_PWRBTN#
PM_SLP_S4#
PM_SLP_S3#
DELAY 99mS
ECPWROK
VRON
PCH
RSMRST#
PWRBTN#
DRAMPWROK
PLTRST#
GPIO
SYS_PWROK
PWROK
MEPWROK
DGPU_HOLD_RST#
IMVP_PWRGD
DGPU_PWR_EN#
GFXPG_R
VR1_READY
+VCC_CORE
R 470K
C 0.1U
R 0ohm
TPS51116REGR
LDO
+1.5V_SUS
0.75VSMDDR_VTERM
+1.5VCPU_PG
SUSON
5VSUS
3VSUS
MAINON
OZ8115
+1.05V_VTT
+1.05_PCH
+1.8V
+0.85V
HWPG(+1.5VSUS)
HWPG(+1.05V_VTT)
HWPG(+1.8V)
HWPG(+0.85V)
HWPG(All Power GOOD)
AON7410
+5V
+3V
MAX8792
GFX_CORE
DGPU_PWR_EN#
GFXPG_1V_EN
+1V_PCIE_PG
LDO RT9018B
+1V_GFX_PCIE
+3.3V_DELAY
TPCA8030-H
+1.5V_GPU
+1.8V_GPU
Delay
DGPU_PWROK
HWPG
GFXPG_R
+1.5V
+1.5VCPU
+1.5VCPU_PG
PROJECT KL5A
Quanta Computer Inc.
Size A2
Document Number
Power Sequence diagram
Rev 1A
Date: Friday, October 29, 2010
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KL5A / Z370 Huron River Schematic EC Tracking Record A (for SDV --> SIV,B)August 5, 2010

EC #	Page	CMVC#	Description	Date	Part Affected
B-00	24		Separate D25 to two single Diodes.	0816,1100	D25
B-01	10,22		Add Color Engine detect pin(PCH GPIO 70).	0816,1100	U17
B-02	9,27,28		Reserve USB3.0 solution for LC request.	0816,1500	U41
B-03	9		Modify PH of PCIE_CLKREQ_WLAN/LAN# to +3V for avoiding leakage current.	0816,1500	U17
B-04	10		Make Board ID table for BIOS control.	0816,1500	
B-05	26		Modify sch of card reader.	0818,1500	U25, CN9
B-06	10		NC R526 for boot issue.	0824,1500	R526
B-07	22		Add 2.2K PH for LVDS EDID used.	0824,1500	R633, R634
B-08	27		Correct the debug pin defition	0825,1400	CN13
B-09	36		Add SYS_PWROK connect to the net "S3" for S3 issue	0825,1400	PU1
B-10	33		Add some capacitors for ESD	0902,1900	SC1,SC2,,SC3,SC4,SC5, SC6,SC7,SC8,SC9,SC10, SC11,SC12,SC13,SC14,SC15, SC16,SC17,SC18,SC19,SC20, SC21,SC22,SC23,SC24,SC25, SC26,SC27,C28
B-11	10		add USB30_ID at GPIO24 & add GPIO13 for ID3	0907,1200	U17

PROJECT KL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC Tracking Record A	1A

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KL5A / Z370 Huron River Schematic EC Tracking Record B (for SIV to SIT)September 8, 2010

EC #	Page	CMVC#	Description	Date	Part Affected
C-00	15-19		GPU change to N12M-GS	0908,1000	U28
C-01	9,22,27, 37,38,39, 40,41		Add RF soultion	0913,1300	RF1,RF2,RF3,RF4,RF5, RF6,RF7,RF8,RF9,RF10, RF11,RF12,RF13,RF14,RF15, RF16,RF17,RF18,RF20,RF21, RF22,RF23,RF24,RF25,RF26, RF27
C-02	31		Change LED3 power from +3V_S5 to +3VPCU for Power LED always bright	0925,1100	LED3
C-03	3,4,7,8, 10,20,23 ,24,		Remove 0 ohm	1011,1700	R87,R253,R217,R224,R274, R339,R344,R351,R375,R376, R377,R378,R387,R397,R402, R409,R410,R423,R424,R425, R428,R429,R437,R430,R431, R545,R587
C-04	9		Remove U13 for delete 27Mhz clock signal form PCH	1015,1400	U13

PROJECT KL5A

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Custom	EC Tracking Record A3	1A
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