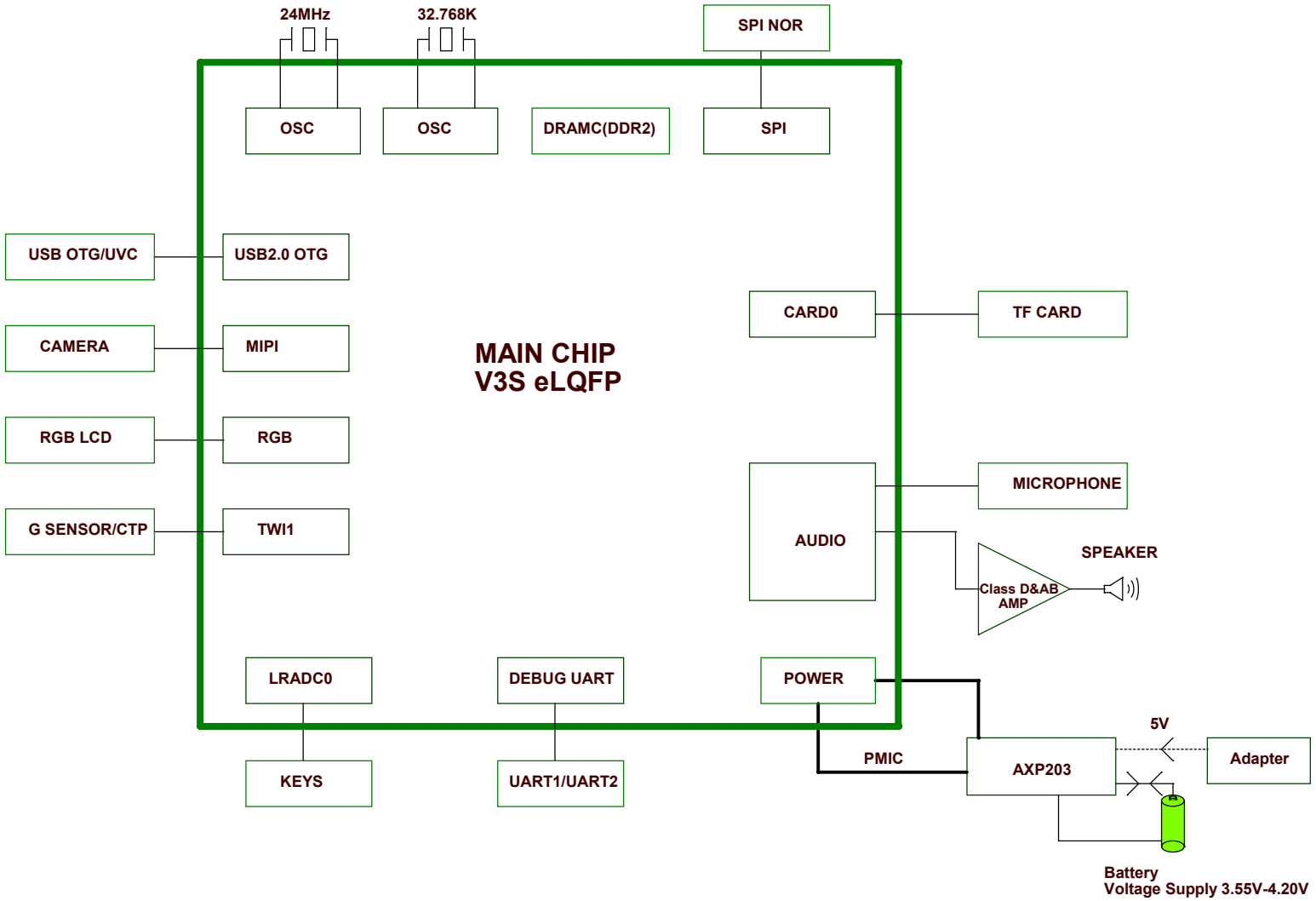
BLOCK DIAGRAM



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Design Name: GAME_V3X_V1_0		
Size: A3	Page Name: BLOCK DIAGRAM	Rev: 0.1
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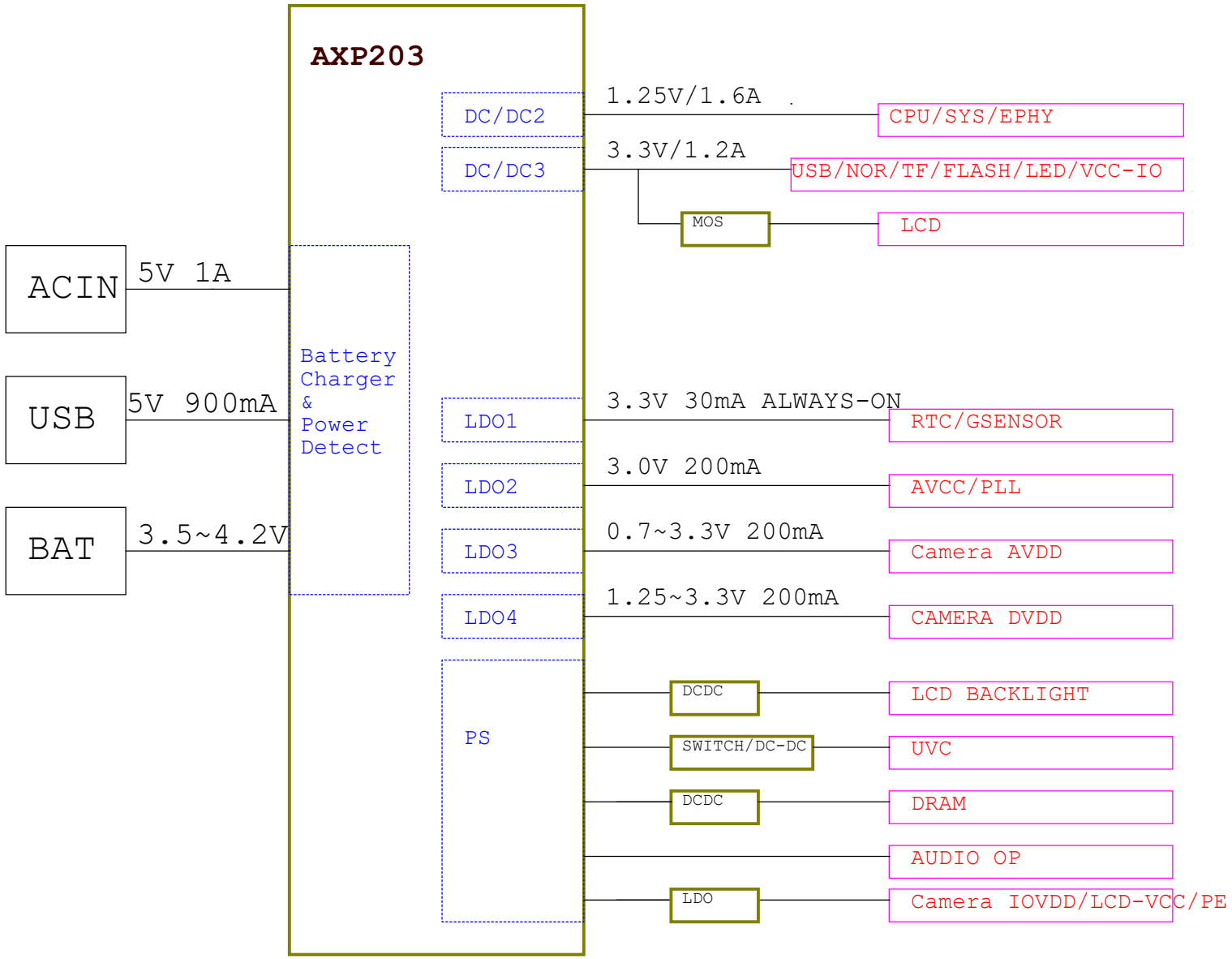
POWER TREE



AllWinner Technology Co.,Ltd		
Design Name: GAME_V3X_V1_0		
Size: A3	Page Name: POWER TREE	Rev
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GPIO ASSIGNMENT

PIN	Define	CFG	Function
PB0	CTP-WAKE	1	CTP
PB1	CTP-INT	0	
PB2	LCD-BL-EN	1	LCD
PB3	LCD-PWR-EN	1	
PB4	PWM0	2	
PB5	PA-SHDN	1	AUDIO
PB6	TWI0-SCK	2	PMU
PB7	TWI0-SDA	2	
PB8	TWI1_SCK	2	G-SENSOR
PB9	TWI1_SDA	2	

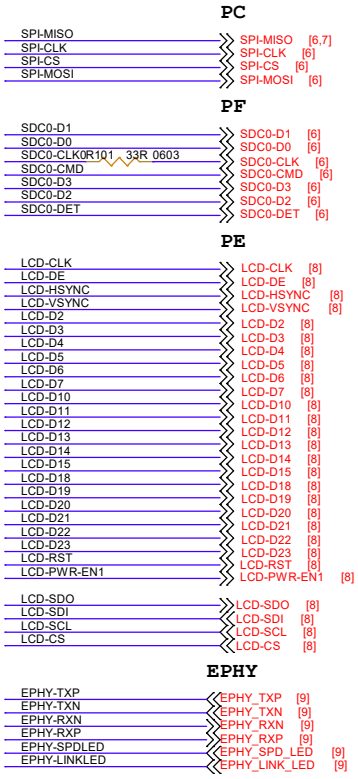
PIN	Define	CFG	Function
PC0	SPI0_MISO	3	NOR/ NAND
PC1	SPI0_CLK	3	
PC2	SPI0_CS	3	
PC3	SPI0_MOSI	3	

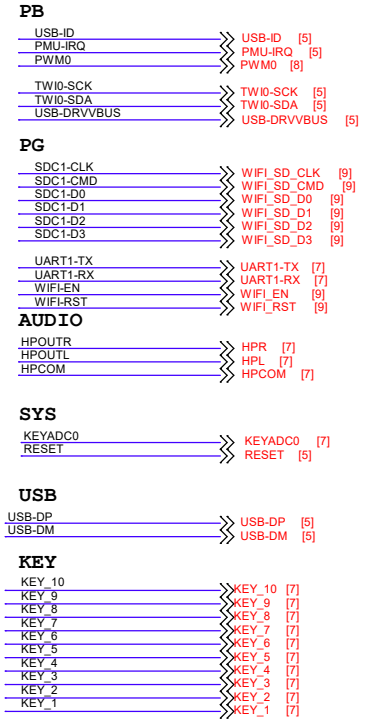
PIN	Define	CFG	Function
PE0	LCD_CLK	3	LCD
PE1	LCD_DE	3	
PE2	LCD_HSYNC	3	
PE3	LCD_VSYNC	3	
PE4	LCD_D2	3	
PE5	LCD_D3	3	
PE6	LCD_D4	3	
PE7	LCD_D5	3	
PE8	LCD_D6	3	
PE9	LCD_D7	3	
PE10	LCD_D8	3	
PE11	LCD_D11	3	
PE12	LCD_D12	3	
PE13	LCD_D13	3	
PE14	LCD_D14	3	
PE15	LCD_D15	3	
PE16	LCD_D18	3	
PE17	LCD_D19	3	
PE18	LCD_D20	3	
PE19	LCD_D21	3	
PE20	CSI-MIPI-MCLK	3	MIPI
PE21	CSI-SDA	2	
PE22	CSI-SCK	2	
PE23	LCD_D22	3	LCD
PE24	LCD_D23	3	

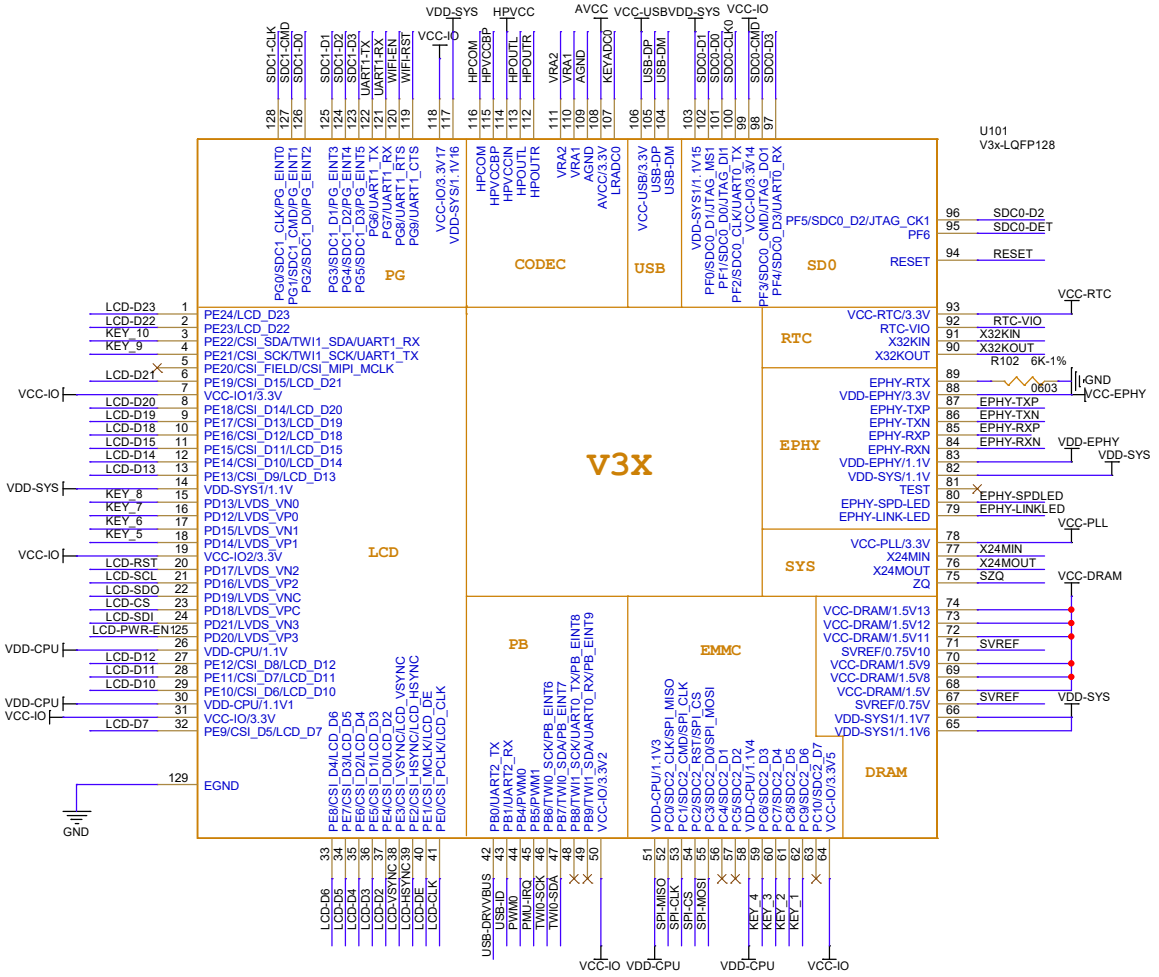
PIN	Define	CFG	Function
PF0	SDC0-D1	2	TF CARD
PF1	SDC0-D0	2	
PF2	SDC0-CLK	2	
PF3	SDC0-CMD	2	
PF4	SDC0-D3	2	
PF5	SDC0-D2	2	
PF6	SDC0-DET	0	

PIN	Define	CFG	Function
PG0	MIPI-CSI-RESET	1	GPIO
PG1	MIPI-CSI-PWDN	1	
PG2	GS-INT	0	
PG3	USB-DRVVBUS	1	
PG4	USB-ID	0	
PG5	PMU-IRQ	0	

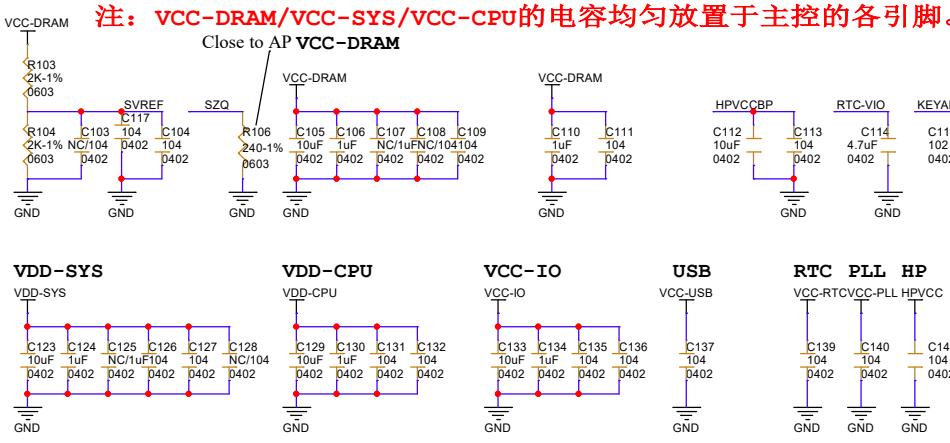
CPU

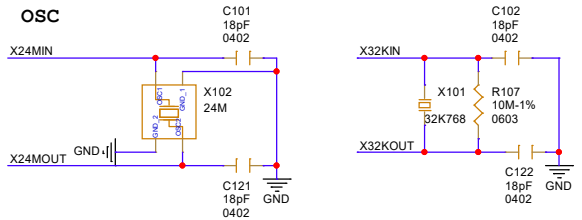






注：VCC-DRAM/VCC-SYS/VCC-CPU的电容均匀放置于主控的各引脚。





AllWinner Technology Co.,Ltd	
Design Name	GAME_V3X_V1_0
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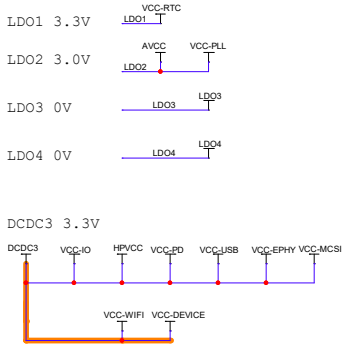
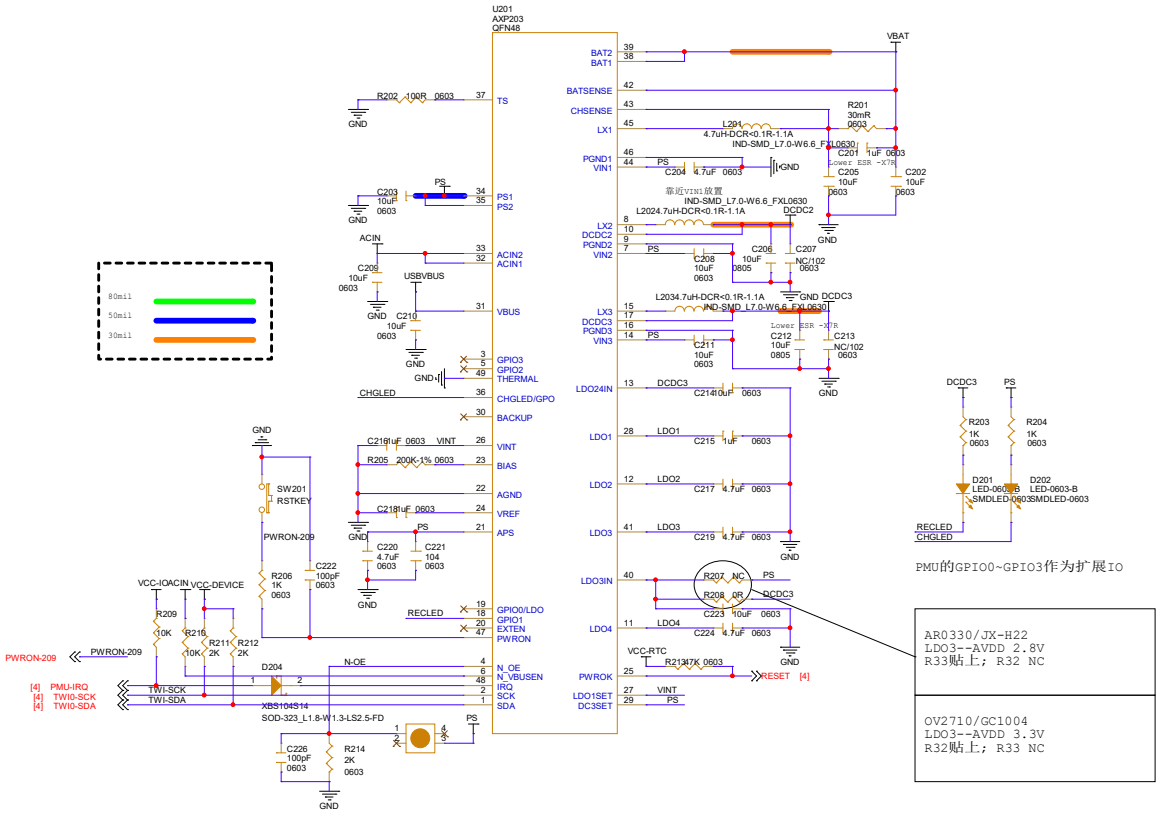
POWER

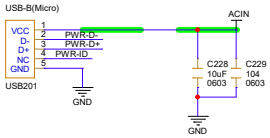


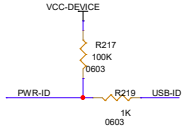


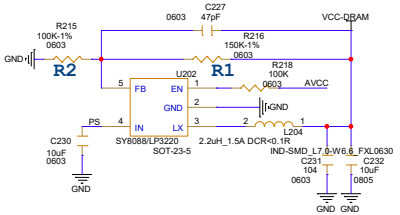
PMU的GPIO0~GPIO3作为扩展IO

AR0330/JX-H22 LDO3--AVDD 2.8V R33贴上; R32 NC
OV2710/GC1004 LDO3--AVDD 3.3V R32贴上; R33 NC

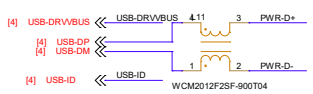
5V DC INPUT

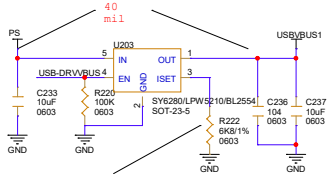




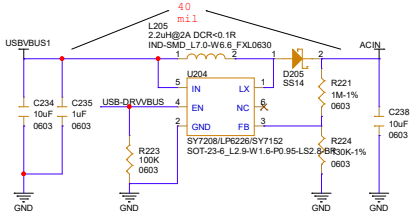


Vout = 0.6*(1+R1/R2)=1.5V





Ilim (A)=6800/Rset (ohm)



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Design Name: GAME_V3X_V1_0			
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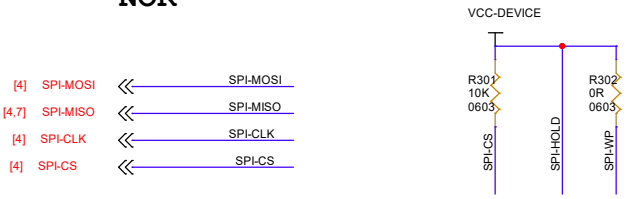
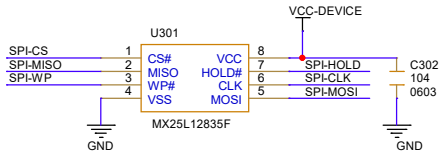
Flash

NOR

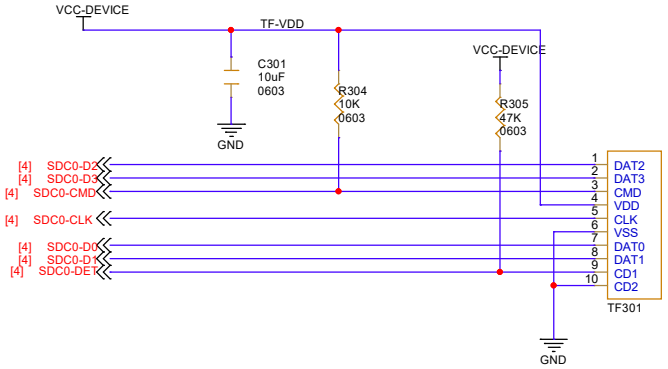




U7 Mount MX25L12835F

SD CARD

CARD0



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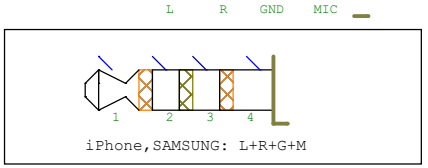
KEY/AUDIO/DEBUG

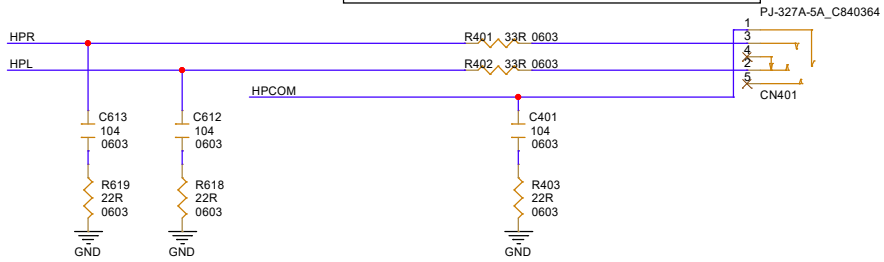
Head Phone

[4] HPR
[4] HPL
[4] HPCOM

HPR
HPL
HPCOM

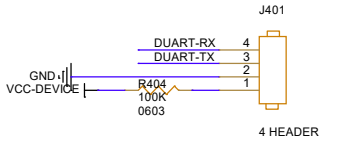
Differential pairs





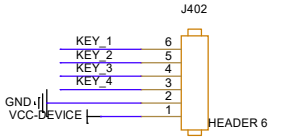
[4] UART1-RX
[4] UART1-TX

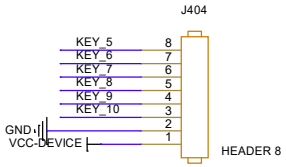
DUART-RX
DUART-TX



[4] KEY_1
[4] KEY_2
[4] KEY_3
[4] KEY_4
[4] KEY_5
[4] KEY_6
[4] KEY_7
[4] KEY_8
[4] KEY_9
[4] KEY_10

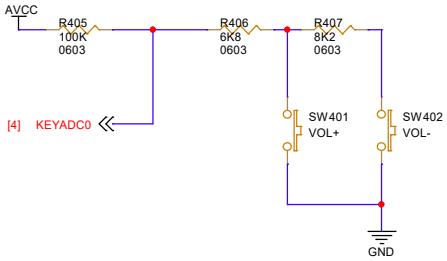
KEY_1
KEY_2
KEY_3
KEY_4
KEY_5
KEY_6
KEY_7
KEY_8
KEY_9
KEY_10



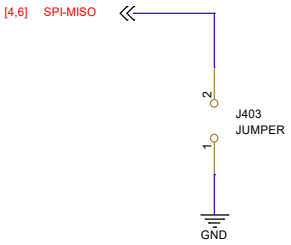


KEY

注：每隔0.2V一个按键



注：预留作为PCBA烧录时使用，
整机不能有该按键；
整机升级需使用组合键。



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Size: A3	Page Name: USB/WIFI/KEY/GSENSOR	Rev
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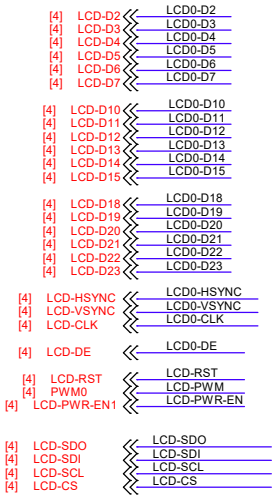
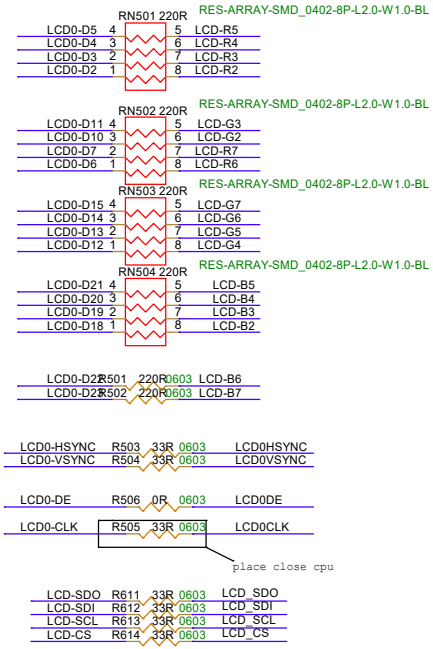
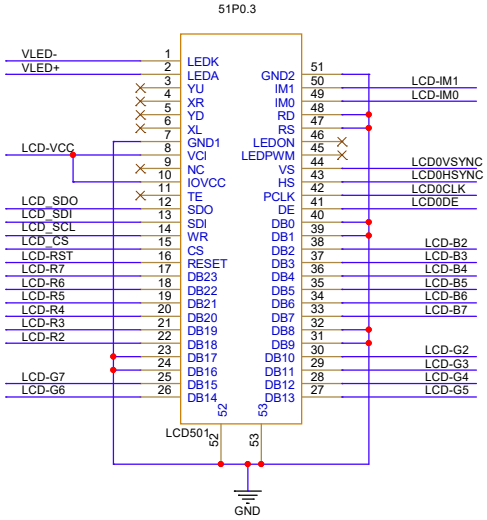
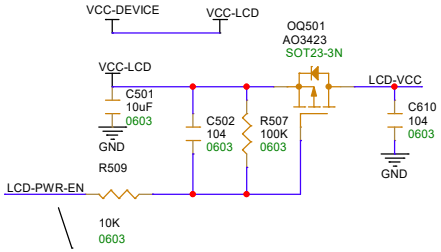
OPTION:RGB LCD

4.3" 480*272

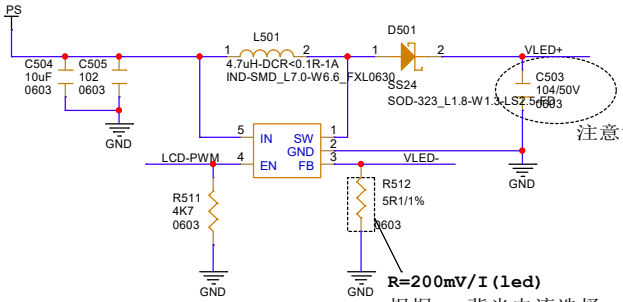






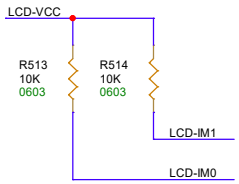


负逻辑，LCD-PWR低电平时，
LCD-VDD打开。



注意背光电路的输出端电容耐压值为50V

根据LCD背光电流选择



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Design Name: GAME_V3X_V1_0		
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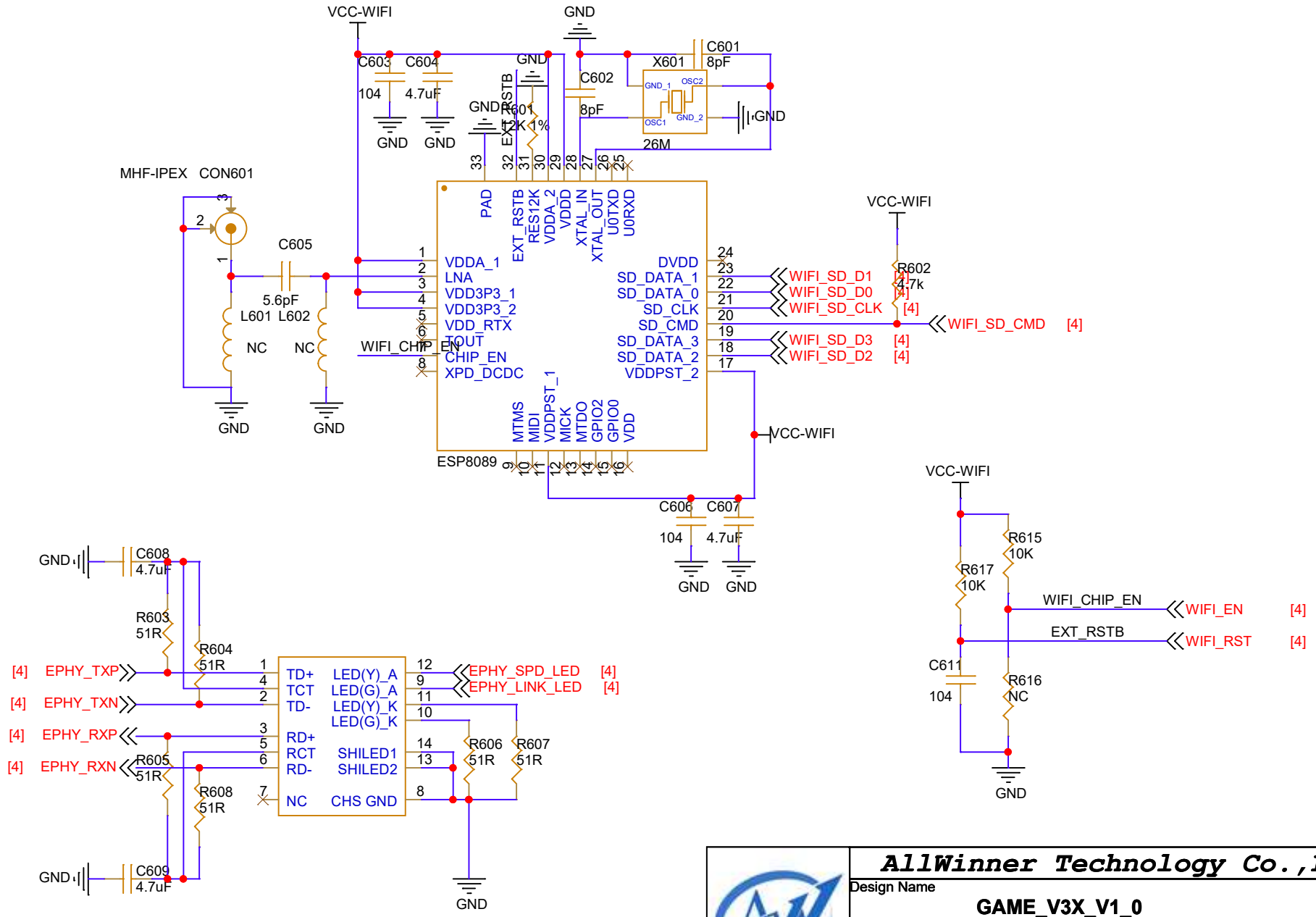

AllWinner Technology Co.,Ltd		
Design Name: GAME_V3X_V1_0		
Size: A	Page Name: ETHERNET	Rev
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