
STM32
CubeMX

1. Description

1.1. Project

Project Name	STM32MP157DAA
Board Name	custom
Generated with:	STM32CubeMX 6.0.1
Date	10/21/2020

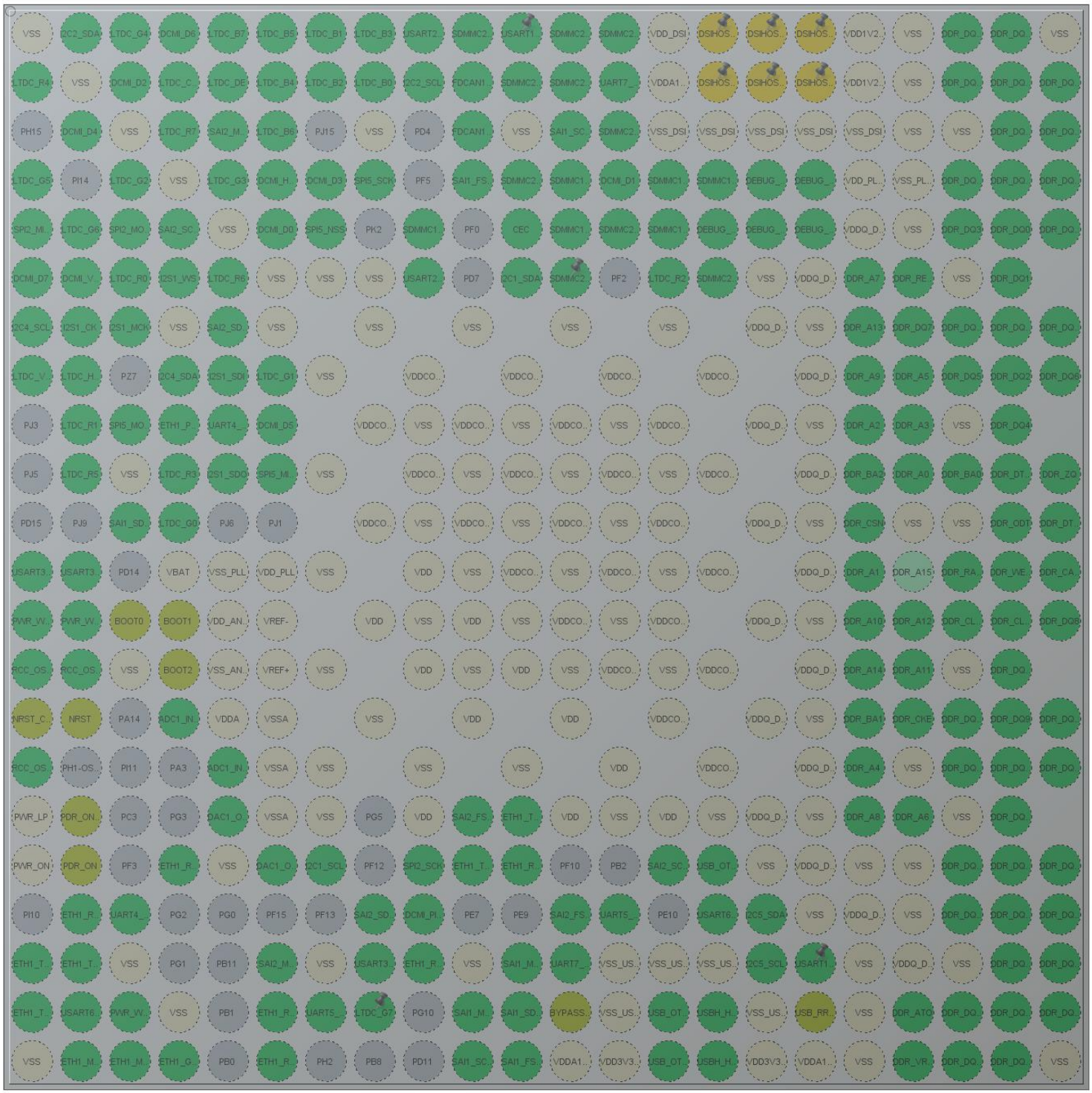
1.2. MCU

MCU Series	STM32MP1
MCU Line	STM32MP157
MCU name	STM32MP157DAAx
MCU Package	LFBGA448
MCU Pin number	448

1.3. Core(s) information

Core(s)	ARM Cortex-A7 ARM Cortex-M4

2. Pinout Configuration



LFBGA448 (Top view)

3. Pins Configuration

Pin Number LFBGA448	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A2	PH5	I/O	I2C2_SDA	
A3	PH4	I/O	LTDC_G4	
A4	PE13	I/O	DCMI_D6	
A5	PK6	I/O	LTDC_B7	
A6	PK4	I/O	LTDC_B5	
A7	PJ13	I/O	LTDC_B1	
A8	PD10	I/O	LTDC_B3	
A9	PD5	I/O	USART2_TX	
A10	PE3	I/O	SDMMC2_CK	
A11	PA9	I/O	USART1_TX	
A12	PB3	I/O	SDMMC2_D2	
A13	PB14	I/O	SDMMC2_D0	
A14	VDD_DSI	Power		
A15	DSIHOST_D0N *	MonoIO	DSIHOST_D0N	
A16	DSIHOST_CKN *	MonoIO	DSIHOST_CKN	
A17	DSIHOST_D1N *	MonoIO	DSIHOST_D1N	
A18	VDD1V2_DSI_PHY	Power		
A19	VSS	Power		
A20	DDR_DQ20	MonoIO	DDR_DQ20	
A21	DDR_DQ23	MonoIO	DDR_DQ23	
A22	VSS	Power		
B1	PH10	I/O	LTDC_R4	
B2	VSS	Power		
B3	PH11	I/O	DCMI_D2	
B4	PE14	I/O	LTDC_CLK	
B5	PK7	I/O	LTDC_DE	
B6	PK3	I/O	LTDC_B4	
B7	PJ14	I/O	LTDC_B2	
B8	PJ12	I/O	LTDC_B0	
B9	PF1	I/O	I2C2_SCL	
B10	PD1	I/O	FDCAN1_TX	
B11	PD3	I/O	SDMMC2_D7	
B12	PB15	I/O	SDMMC2_D1	
B13	PA8	I/O	UART7_RX	
B14	VDDA1V8_DSI	Power		

Pin Number LFBGA448	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
B15	DSIHOST_D0P *	MonoIO	DSIHOST_D0P	
B16	DSIHOST_CKP *	MonoIO	DSIHOST_CKP	
B17	DSIHOST_D1P *	MonoIO	DSIHOST_D1P	
B18	VDD1V2_DSI_REG	Power		
B19	VSS	Power		
B20	DDR_DQ19	MonoIO	DDR_DQ19	
B21	DDR_DQ16	MonoIO	DDR_DQ16	
B22	DDR_DQS2N	MonoIO	DDR_DQS2N	
C2	PH14	I/O	DCMI_D4	
C3	VSS	Power		
C4	PE15	I/O	LTDC_R7	
C5	PE0	I/O	SAI2_MCLK_A	
C6	PK5	I/O	LTDC_B6	
C8	VSS	Power		
C10	PD0	I/O	FDCAN1_RX	
C11	VSS	Power		
C12	PE5	I/O	SAI1_SCK_A	
C13	PB4	I/O	SDMMC2_D3	
C14	VSS_DSI	Power		
C15	VSS_DSI	Power		
C16	VSS_DSI	Power		
C17	VSS_DSI	Power		
C18	VSS_DSI	Power		
C19	VSS	Power		
C20	VSS	Power		
C21	DDR_DQS2P	MonoIO	DDR_DQS2P	
C22	DDR_DQM2	MonoIO	DDR_DQM2	
D1	PI0	I/O	LTDC_G5	
D3	PH13	I/O	LTDC_G2	
D4	VSS	Power		
D5	PE11	I/O	LTDC_G3	
D6	PH8	I/O	DCMI_HSYNC	
D7	PE1	I/O	DCMI_D3	
D8	PK0	I/O	SPI5_SCK	
D10	PG15	I/O	SAI1_FS_A	
D11	PG6	I/O	SDMMC2_CMD	
D12	PD2	I/O	SDMMC1_CMD	
D13	PC7	I/O	DCMI_D1	
D14	PC9	I/O	SDMMC1_D1	

Pin Number LFBGA448	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
D15	PC11	I/O	SDMMC1_D3	
D16	JTDI	MonoIO	DEBUG_JTDI	
D17	JTCK-SWCLK	MonoIO	DEBUG_JTCK-SWCLK	
D18	VDD_PLL2	Power		
D19	VSS_PLL2	Power		
D20	DDR_DQ22	MonoIO	DDR_DQ22	
D21	DDR_DQ17	MonoIO	DDR_DQ17	
D22	DDR_DQ18	MonoIO	DDR_DQ18	
E1	PI2	I/O	SPI2_MISO	
E2	PI1	I/O	LTDC_G6	
E3	PI3	I/O	SPI2_MOSI	
E4	PE12	I/O	SAI2_SCK_B	
E5	VSS	Power		
E6	PH9	I/O	DCMI_D0	
E7	PK1	I/O	SPI5_NSS	
E9	PE6	I/O	SDMMC1_D2	
E11	PA15	I/O	CEC	
E12	PC12	I/O	SDMMC1_CK	
E13	PC6	I/O	SDMMC2_D6	
E14	PC8	I/O	SDMMC1_D0	
E15	NJTRST	MonoIO	DEBUG_JTRST	
E16	JTDO-TRACESWO	MonoIO	DEBUG_JTDO-SWO	
E17	JTMS-SWDIO	MonoIO	DEBUG_JTMS-SWDIO	
E18	VDDQ_DDR	Power		
E19	VSS	Power		
E20	DDR_DQ3	MonoIO	DDR_DQ3	
E21	DDR_DQ0	MonoIO	DDR_DQ0	
E22	DDR_DQ21	MonoIO	DDR_DQ21	
F1	PI7	I/O	DCMI_D7	
F2	PI5	I/O	DCMI_VSYNC	
F3	PI15	I/O	LTDC_R0	
F4	PZ3	I/O	I2S1_WS	
F5	PH12	I/O	LTDC_R6	
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	PF4	I/O	USART2_RX	
F11	PB7	I/O	I2C1_SDA	
F12	PB9	I/O	SDMMC2_D5	

Pin Number LFBGA448	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F14	PC10	I/O	LTDC_R2	
F15	PE4	I/O	SDMMC2_D4	
F16	VSS	Power		
F17	VDDQ_DDR	Power		
F18	DDR_A7	MonoIO	DDR_A7	
F19	DDR_RESETN	MonoIO	DDR_RESETN	
F20	VSS	Power		
F21	DDR_DQ1	MonoIO	DDR_DQ1	
G1	PZ4	I/O	I2C4_SCL	
G2	PZ0	I/O	I2S1_CK	
G3	PZ6	I/O	I2S1_MCK	
G4	VSS	Power		
G5	PI6	I/O	SAI2_SD_A	
G6	VSS	Power		
G8	VSS	Power		
G10	VSS	Power		
G12	VSS	Power		
G14	VSS	Power		
G16	VDDQ_DDR	Power		
G17	VSS	Power		
G18	DDR_A13	MonoIO	DDR_A13	
G19	DDR_DQ7	MonoIO	DDR_DQ7	
G20	DDR_DQM0	MonoIO	DDR_DQM0	
G21	DDR_DQS0N	MonoIO	DDR_DQS0N	
G22	DDR_DQS0P	MonoIO	DDR_DQS0P	
H1	PI13	I/O	LTDC_VSYNC	
H2	PI12	I/O	LTDC_HSYNC	
H4	PZ5	I/O	I2C4_SDA	
H5	PZ1	I/O	I2S1_SDI	
H6	PJ8	I/O	LTDC_G1	
H7	VSS	Power		
H9	VDDCORE	Power		
H11	VDDCORE	Power		
H13	VDDCORE	Power		
H15	VDDCORE	Power		
H17	VDDQ_DDR	Power		
H18	DDR_A9	MonoIO	DDR_A9	
H19	DDR_A5	MonoIO	DDR_A5	
H20	DDR_DQ5	MonoIO	DDR_DQ5	

Pin Number LFBGA448	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
H21	DDR_DQ2	MonoIO	DDR_DQ2	
H22	DDR_DQ6	MonoIO	DDR_DQ6	
J2	PJ0	I/O	LTDC_R1	
J3	PJ10	I/O	SPI5_MOSI	
J4	PG12	I/O	ETH1_PHY_INTN	
J5	PI9	I/O	UART4_RX	
J6	PI4	I/O	DCMI_D5	
J8	VDDCORE	Power		
J9	VSS	Power		
J10	VDDCORE	Power		
J11	VSS	Power		
J12	VDDCORE	Power		
J13	VSS	Power		
J14	VDDCORE	Power		
J16	VDDQ_DDR	Power		
J17	VSS	Power		
J18	DDR_A2	MonoIO	DDR_A2	
J19	DDR_A3	MonoIO	DDR_A3	
J20	VSS	Power		
J21	DDR_DQ4	MonoIO	DDR_DQ4	
K2	PJ4	I/O	LTDC_R5	
K3	VSS	Power		
K4	PJ2	I/O	LTDC_R3	
K5	PZ2	I/O	I2S1_SDO	
K6	PJ11	I/O	SPI5_MISO	
K7	VSS	Power		
K9	VDDCORE	Power		
K10	VSS	Power		
K11	VDDCORE	Power		
K12	VSS	Power		
K13	VDDCORE	Power		
K14	VSS	Power		
K15	VDDCORE	Power		
K17	VDDQ_DDR	Power		
K18	DDR_BA2	MonoIO	DDR_BA2	
K19	DDR_A0	MonoIO	DDR_A0	
K20	DDR_BA0	MonoIO	DDR_BA0	
K21	DDR_DTO1	MonoIO	DDR_DTO1	
K22	DDR_ZQ	MonoIO	DDR_ZQ	

Pin Number LFBGA448	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
L3	PD6	I/O	SAI1_SD_A	
L4	PJ7	I/O	LTDC_G0	
L8	VDDCORE	Power		
L9	VSS	Power		
L10	VDDCORE	Power		
L11	VSS	Power		
L12	VDDCORE	Power		
L13	VSS	Power		
L14	VDDCORE	Power		
L16	VDDQ_DDR	Power		
L17	VSS	Power		
L18	DDR_CSN	MonoIO	DDR_CSN	
L19	VSS	Power		
L20	VSS	Power		
L21	DDR_ODT	MonoIO	DDR_ODT	
L22	DDR_DTO0	MonoIO	DDR_DTO0	
M1	PD8	I/O	USART3_TX	
M2	PD9	I/O	USART3_RX	
M4	VBAT	Power		
M5	VSS_PLL	Power		
M6	VDD_PLL	Power		
M7	VSS	Power		
M9	VDD	Power		
M10	VSS	Power		
M11	VDDCORE	Power		
M12	VSS	Power		
M13	VDDCORE	Power		
M14	VSS	Power		
M15	VDDCORE	Power		
M17	VDDQ_DDR	Power		
M18	DDR_A1	MonoIO	DDR_A1	
M20	DDR_RASN	MonoIO	DDR_RASN	
M21	DDR_WEN	MonoIO	DDR_WEN	
M22	DDR_CASN	MonoIO	DDR_CASN	
N1	PI8	I/O	PWR_WKUP4	
N2	PC13	I/O	PWR_WKUP3	
N3	BOOT0	Boot		
N4	BOOT1	Boot		
N5	VDD_ANA	Power		

Pin Number LFBGA448	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
N6	VREF-	Power		
N8	VDD	Power		
N9	VSS	Power		
N10	VDD	Power		
N11	VSS	Power		
N12	VDDCORE	Power		
N13	VSS	Power		
N14	VDDCORE	Power		
N16	VDDQ_DDR	Power		
N17	VSS	Power		
N18	DDR_A10	MonoIO	DDR_A10	
N19	DDR_A12	MonoIO	DDR_A12	
N20	DDR_CLKP	MonoIO	DDR_CLKP	
N21	DDR_CLKN	MonoIO	DDR_CLKN	
N22	DDR_DQ8	MonoIO	DDR_DQ8	
P1	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
P2	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
P3	VSS	Power		
P4	BOOT2	Boot		
P5	VSS_ANA	Power		
P6	VREF+	Power		
P7	VSS	Power		
P9	VDD	Power		
P10	VSS	Power		
P11	VDD	Power		
P12	VSS	Power		
P13	VDDCORE	Power		
P14	VSS	Power		
P15	VDDCORE	Power		
P17	VDDQ_DDR	Power		
P18	DDR_A14	MonoIO	DDR_A14	
P19	DDR_A11	MonoIO	DDR_A11	
P20	VSS	Power		
P21	DDR_DQ10	MonoIO	DDR_DQ10	
R1	NRST_CORE	Reset		
R2	NRST	Reset		
R4	ANA0	MonoIO	ADC1_INP0	
R5	VDDA	Power		
R6	VSSA	Power		

Pin Number LFBGA448	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
R8	VSS	Power		
R10	VDD	Power		
R12	VDD	Power		
R14	VDDCORE	Power		
R16	VDDQ_DDR	Power		
R17	VSS	Power		
R18	DDR_BA1	MonoIO	DDR_BA1	
R19	DDR_CKE	MonoIO	DDR_CKE	
R20	DDR_DQ13	MonoIO	DDR_DQ13	
R21	DDR_DQ9	MonoIO	DDR_DQ9	
R22	DDR_DQS1N	MonoIO	DDR_DQS1N	
T1	PH0-OSC_IN	I/O	RCC_OSC_IN	
T5	ANA1	MonoIO	ADC1_INP1	
T6	VSSA	Power		
T7	VSS	Power		
T9	VSS	Power		
T11	VSS	Power		
T13	VDD	Power		
T15	VDDCORE	Power		
T17	VDDQ_DDR	Power		
T18	DDR_A4	MonoIO	DDR_A4	
T19	VSS	Power		
T20	DDR_DQ11	MonoIO	DDR_DQ11	
T21	DDR_DQM1	MonoIO	DDR_DQM1	
T22	DDR_DQS1P	MonoIO	DDR_DQS1P	
U1	PWR_LP	Power		
U2	PDR_ON_CORE	MonoIO		
U5	PA5	I/O	DAC1_OUT2	
U6	VSSA	Power		
U7	VSS	Power		
U9	VDD	Power		
U10	PC0	I/O	SAI2_FS_B	
U11	PG11	I/O	ETH1_TX_CTL	
U12	VDD	Power		
U13	VSS	Power		
U14	VDD	Power		
U15	VSS	Power		
U16	VDDQ_DDR	Power		
U17	VSS	Power		

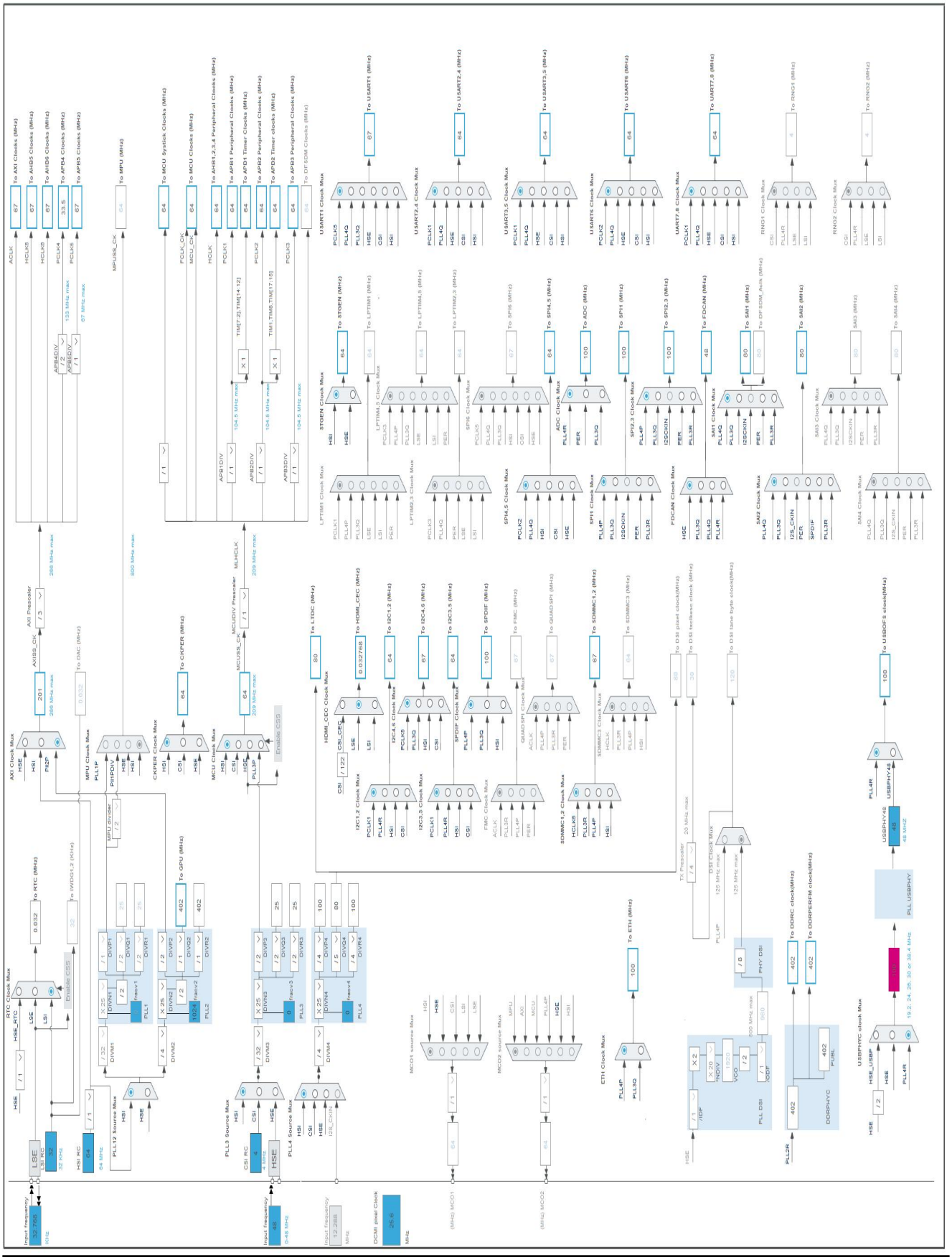
Pin Number LFBGA448	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
U18	DDR_A8	MonoIO	DDR_A8	
U19	DDR_A6	MonoIO	DDR_A6	
U20	VSS	Power		
U21	DDR_DQ14	MonoIO	DDR_DQ14	
V1	PWR_ON	Power		
V2	PDR_ON	MonoIO		
V4	PA1	I/O	ETH1_RX_CLK	
V5	VSS	Power		
V6	PA4	I/O	DAC1_OUT1	
V7	PF14	I/O	I2C1_SCL	
V9	PB10	I/O	SPI2_SCK	
V10	PB13	I/O	ETH1_TXD1	
V11	PH6	I/O	ETH1_RXD2	
V14	PD13	I/O	SAI2_SCK_A	
V15	OTG_VBUS	MonoIO	USB_OTG_HS_VBUS	
V16	VSS	Power		
V17	VDDQ_DDR	Power		
V18	VSS	Power		
V19	VSS	Power		
V20	DDR_DQ12	MonoIO	DDR_DQ12	
V21	DDR_DQ15	MonoIO	DDR_DQ15	
V22	DDR_DQ24	MonoIO	DDR_DQ24	
W2	PH7	I/O	ETH1_RXD3	
W3	PA13	I/O	UART4_TX	
W8	PF11	I/O	SAI2_SD_B	
W9	PA6	I/O	DCMI_PIXCLK	
W12	PD12	I/O	SAI2_FS_A	
W13	PB6	I/O	UART5_TX	
W15	PG9	I/O	USART6_RX	
W16	PA12	I/O	I2C5_SDA	
W17	VSS	Power		
W18	VDDQ_DDR	Power		
W19	VSS	Power		
W20	DDR_DQ25	MonoIO	DDR_DQ25	
W21	DDR_DQ31	MonoIO	DDR_DQ31	
W22	DDR_DQ30	MonoIO	DDR_DQ30	
Y1	PC2	I/O	ETH1_TXD2	
Y2	PE2	I/O	ETH1_TXD3	
Y3	VSS	Power		

Pin Number LFBGA448	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
Y6	PH3	I/O	SAI2_MCLK_B	
Y7	VSS	Power		
Y8	PG8	I/O	USART3_DE	
Y9	PA7	I/O	ETH1_RX_CTL	
Y10	VSS	Power		
Y11	PG7	I/O	SAI1_MCLK_A	
Y12	PE8	I/O	UART7_TX	
Y13	VSS_USBHS	Power		
Y14	VSS_USBHS	Power		
Y15	VSS_USBHS	Power		
Y16	PA11	I/O	I2C5_SCL	
Y17	PA10	I/O	USART1_RX	
Y18	VSS	Power		
Y19	VDDQ_DDR	Power		
Y20	VSS	Power		
Y21	DDR_DQS3P	MonoIO	DDR_DQS3P	
Y22	DDR_DQS3N	MonoIO	DDR_DQS3N	
AA1	PG13	I/O	ETH1_TXD0	
AA2	PG14	I/O	USART6_TX	
AA3	PA0	I/O	PWR_WKUP1	
AA4	VSS	Power		
AA6	PC5	I/O	ETH1_RXD1	
AA7	PB12	I/O	UART5_RX	
AA8	PB5	I/O	LTDC_G7	
AA10	PF7	I/O	SAI1_MCLK_B	
AA11	PF6	I/O	SAI1_SD_B	
AA12	BYPASS_REG1V8	MonoIO		
AA13	VSS_USBHS	Power		
AA14	USB_DM2	MonoIO	USB_OTG_HS_DM	
AA15	USB_DP1	MonoIO	USBH_HS1_DP	
AA16	VSS_USBHS	Power		
AA17	USB_RREF	MonoIO		
AA18	VSS	Power		
AA19	DDR_ATO	MonoIO	DDR_ATO	
AA20	DDR_DQ29	MonoIO	DDR_DQ29	
AA21	DDR_DQ28	MonoIO	DDR_DQ28	
AA22	DDR_DQM3	MonoIO	DDR_DQM3	
AB1	VSS	Power		
AB2	PA2	I/O	ETH1_MDIO	

Pin Number LFBGA448	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
AB3	PC1	I/O	ETH1_MDC	
AB4	PG4	I/O	ETH1_GTX_CLK	
AB6	PC4	I/O	ETH1_RXD0	
AB10	PF8	I/O	SAI1_SCK_B	
AB11	PF9	I/O	SAI1_FS_B	
AB12	VDDA1V8_REG	Power		
AB13	VDD3V3_USBHS	Power		
AB14	USB_DP2	MonoIO	USB_OTG_HS_DP	
AB15	USB_DM1	MonoIO	USBH_HS1_DM	
AB16	VDD3V3_USBFS	Power		
AB17	VDDA1V1_REG	Power		
AB18	VSS	Power		
AB19	DDR_VREF	MonoIO	DDR_VREF	
AB20	DDR_DQ27	MonoIO	DDR_DQ27	
AB21	DDR_DQ26	MonoIO	DDR_DQ26	
AB22	VSS	Power		

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32MP157DAA
Project Folder	F:\STM32\STM32MP157DAA
Toolchain / IDE	EWARM V8.32
Firmware Package Name and Version	STM32Cube FW_MP1 V1.2.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls ARM Cortex-A7

Rank	Function Name	IP Instance Name

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ETZPC_Init	ETZPC
5	MX_IPCC_Init	IPCC
6	MX_SPI5_Init	SPI5

Rank	Function Name	IP Instance Name
7	MX_SPI2_Init	SPI2
8	MX_UART4_Init	UART4

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32MP1
Line	STM32MP157
MCU	STM32MP157DAAx
Datasheet	DS12504_Rev3

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

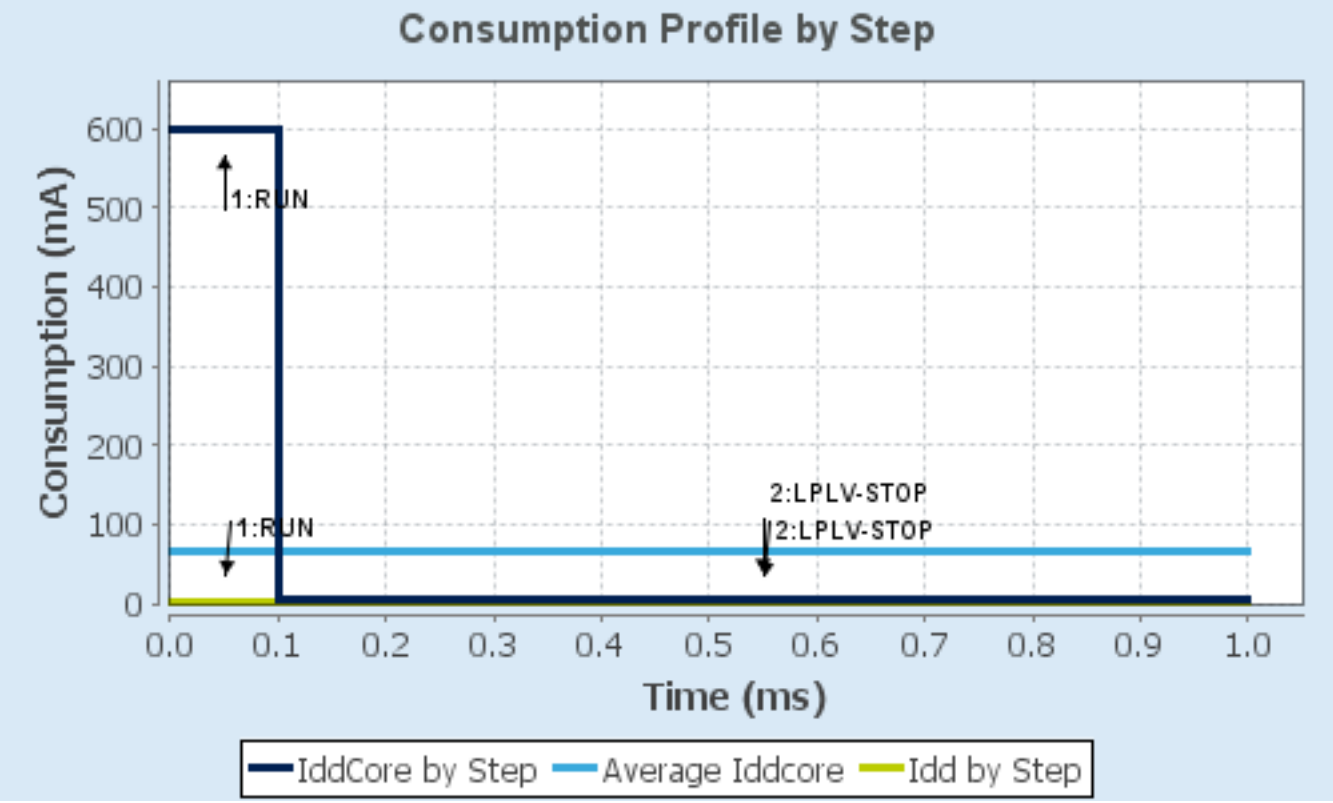
6.4. Sequence

Step	Step1	Step2
Mode	RUN	LPLV-STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Vdd Core	1.38	0.85
MPU0 Mode	P0RUN	P0STOP
MPU1 Mode	P1RUN	P1STOP
MCU Mode	CRUN	CSTOP
Fetch Type	SRAM	NA
MPU0/MPU1 Frequency	800 MHz	0 Hz
Clock Configuration	HSE HSI LSI PLL ALL_IPs_ON	ALL CLOCKS OFF
MCU Frequency	210 MHz	0 Hz
AXI Frequency	264 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Idd Core	600 mA	6.05 mA
Idd	3.7 mA	0.83 mA
Duration	0.1 ms	0.9 ms
DMIPS	0.0	0.0
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	65.44 mA
Battery Life	22 days, 21 hours	Average DMIPS	0.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
600
500
400
300
200
100
0
1:RUN
1:RUN
2:LPLV-STOP
2:LPLV-STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
IddCore by Step
Average Iddcore
Idd by Step

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN0 Single-ended

IN1: IN1 Single-ended

7.1.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. BSEC

mode: Activated

7.3. DAC1

OUT1 mode: Connected to external pin only

OUT2 mode: Connected to external pin only

7.3.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None
DAC High Frequency	Mode Disable
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None
DAC High Frequency	Mode Disable
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.4. DCMI

DCMI: Slave 8 bits External Synchro

7.4.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure

Power Domain:

Mode Config:

Pixel clock polarity	Active on Falling edge
Vertical synchronization polarity	Active Low
Horizontal synchronization polarity	Active Low
Frequency of frame capture	All frames are captured
JPEG mode	Disabled

Interface Capture Config:

Byte Select Mode	Interface captures all received bytes
Line Select Mode	Interface captures all received lines

7.5. DDR

DDR Type

DDR Type: DDR3 / DDR3L

Width

Width: 32bits

Density for DDR3(L) 32bits

Density for DDR3(L) 32bits: 8Gb

7.5.1. Parameter Settings:

Core(s) Settings:

Context(s): Boot loader
Cortex-A7 secure
Cortex-A7 non secure

Initialized Context: Cortex-A7 non secure

Power Domain:

SYSTEM PARAMETERS:

DDR subsystem frequency	402.0
Speed Bin Grade	DDR3-1066G / 8-8-8
Impedance During Read	Ron 40 ohm / ODT = 80 ohm (Default)
Impedance During Write	Ron 53 ohm / ODT = 60 ohm (Default)
Address Mapping configuration	Row - Bank - Column
Relaxed Timing mode	false
Temperature case over 85°C support	false
Burst Length (BL)	8

7.5.2. DDR tuning:

Core(s) Settings:

Context(s):	Boot loader Cortex-A7 secure Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

BYTE 0:

Byte Lane 0 - Slave DLL phase	0
Byte Lane 0 - DQS gating phase select fine tuning	2
Byte Lane 0 - DQS gating system latency fine tuning	0
Byte Lane 0 - DQS delay fine tuning	3
Byte Lane 0 - DQS# delay fine tuning	3
Byte lane 0 – DQ delay for bit 0 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 0 – DQ delay for bit 1 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 0 – DQ delay for bit 2 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 0 – DQ delay for bit 3 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 0 – DQ delay for bit 4 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 0 – DQ delay for bit 5 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 0 – DQ delay for bit 6 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 0 – DQ delay for bit 7 fine tuning (both DQS/DQS# clock)	0xF

BYTE 1:

Byte Lane 1 - Slave DLL phase	0
Byte Lane 1 - DQS gating system latency fine tuning	2
Byte Lane 1 - DQS gating system latency fine tuning	0
Byte Lane 1 - DQS delay fine tuning	3
Byte Lane 1 - DQS# delay fine tuning	3
Byte lane 1 – DQ delay for bit 0 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 1 – DQ delay for bit 1 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 1 – DQ delay for bit 2 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 1 – DQ delay for bit 3 fine tuning (both	0xF

DQS/DQS# clock)	
Byte lane 1 – DQ delay for bit 4 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 1 – DQ delay for bit 5 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 1 – DQ delay for bit 6 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 1 – DQ delay for bit 7 fine tuning (both DQS/DQS# clock)	0xF

BYTE 2:

Byte Lane 2 - Slave DLL phase	0
Byte Lane 2 - DQS gating phase select fine tuning	2
Byte Lane 2 - DQS gating system latency fine tuning	0
Byte Lane 2 - DQS delay fine tuning	3
Byte Lane 2 - DQS# delay fine tuning	3
Byte lane 2 – DQ delay for bit 0 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 2 – DQ delay for bit 1 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 2 – DQ delay for bit 2 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 2 – DQ delay for bit 3 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 2 – DQ delay for bit 4 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 2 – DQ delay for bit 5 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 2 – DQ delay for bit 6 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 2 – DQ delay for bit 7 fine tuning (both DQS/DQS# clock)	0xF

BYTE 3:

Byte Lane 3 - Slave DLL phase	0
Byte Lane 3 - DQS gating phase select fine tuning	2
Byte Lane 3 - DQS gating system latency fine tuning	0
Byte Lane 3 - DQS delay fine tuning	3
Byte Lane 3 - DQS# delay fine tuning	3
Byte lane 3 – DQ delay for bit 0 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 3 – DQ delay for bit 1 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 3 – DQ delay for bit 2 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 3 – DQ delay for bit 3 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 3 – DQ delay for bit 4 fine tuning (both	0xF

DQS/DQS# clock)	
Byte lane 3 – DQ delay for bit 5 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 3 – DQ delay for bit 6 fine tuning (both DQS/DQS# clock)	0xF
Byte lane 3 – DQ delay for bit 7 fine tuning (both DQS/DQS# clock)	0xF

7.6. DEBUG

Debug: JTAG (5 pins)

7.7. ETH1

Mode: RGMII (Reduced GMII)

mode: ETH PHY_INTN

7.8. ETZPC

mode: Activated

7.9. FDCAN1

Mode: FD

7.9.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Basic Parameters:

Frame Format	FD mode without BitRate Switshing
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Prescaler	1
Nominal Sync Jump Width	1
Nominal Time Seg1	2
Nominal Time Seg2	2
Data Prescaler	1
Data Sync Jump Width	1

Data Time Seg1	1
Data Time Seg2	1
Message Ram Offset	0
Std Filters Nbr	0
Ext Filters Nbr	0
Rx Fifo0 Elmts Nbr	0
Rx Fifo0 Elmt Size	8 bytes data field
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	8 bytes data field
Rx Buffers Nbr	0
Rx Buffer Size	8 bytes data field
Tx Events Nbr	0
Tx Buffers Nbr	0
Tx Fifo Queue Elmts Nbr	0
Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	8 bytes data field

7.10. GIC

7.11. GPIO

7.12. GPU
mode: Activated

7.13. HDMI_CEC
mode: Activated
7.13.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Configuration parameters:

Signal Free Time	2.5, 4 or 6 nominal data bit periods
Rx tolerance	Standard tolerance
Signal Free Time option	SFT timer starts when Transmission Start Of Message is set by software
Listening mode	Receive all messages

Address parameters:

Logical address 0	Disable
Logical address 1	Disable
Logical address 2	Disable
Logical address 3	Disable
Logical address 4	Disable
Logical address 5	Disable
Logical address 6	Disable
Logical address 7	Disable
Logical address 8	Disable
Logical address 9	Disable
Logical address 10	Disable
Logical address 11	Disable
Logical address 12	Disable
Logical address 13	Disable
Logical address 14	Disable
Received data buffer name	cec_receive_buffer

Error handling:

Stop reception on bit rising error	Reception is stopped
Generate error bit on bit rising error	No error bit generation
Generate error bit on long bit period error	No error bit generation
Avoid error bit generation on error detection in broadcast	Error bit generation

7.14. HSEM

mode: Activated

7.15. I2C1

I2C: I2C

7.15.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0

Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.16. I2C2

I2C: I2C

7.16.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.17. I2C4

I2C: I2C

7.17.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 secure
Initialized Context:	Cortex-A7 secure
Power Domain:	

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x108083C5 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.18. I2C5

I2C: I2C

7.18.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0

Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.19. I2S1

Mode: Full-Duplex Master

mode: Master Clock Output

7.19.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Generic Parameters:

Transmission Mode	Mode Master Transmit
Communication Standard	I2S Philips
Data and Frame Format	16 Bits Data on 16 Bits Frame
Selected Audio Frequency	16 KHz
Real Audio Frequency	**16.276 KHz ***
Error between Selected and Real	**1.72 % ***

Clock Parameters:

Clock Source	PLL I2SR Clock
Clock Polarity	Low
First Bit	Firstbit Msb
Ws Inversion	Ws Inversion Disable
Io Swap	Io Swap Disable
Data24 Bit Alignment	Data 24 Bit Alignment Right
Fifo Threshold	Fifo Threshold 01 Data
Master Keep Io State	Master Keep Io State Disable
Slave Extend Fre Detection	Slave Extend Fre Detection Disable

7.20. IPCC

mode: Activated

7.21. LTDC

Display Type: RGB888 (24 bits)

7.21.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Synchronization for Width:

Horizontal Synchronization Width	8
Horizontal Back Porch	7
Active Width	640
Horizontal Front Porch	6
HSync Width	7
Accumulated Horizontal Back Porch Width	14
Accumulated Active Width	654
Total Width	660

Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	2
Active Height	480
Vertical Front Porch	2
VSync Height	3
Accumulated Vertical Back Porch Height	5
Accumulated Active Height	485
Total Height	487

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Not Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

7.21.2. Layer Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

Number of Layers:

Number of Layers	2 layers

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	0
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	0
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	0
Layer 1 - Window Vertical Start	0
Layer 1 - Window Vertical Stop	0

Pixel Parameters:

Layer 0 - Pixel Format	ARGB8888
Layer 1 - Pixel Format	ARGB8888

Blending:

Layer 0 - Alpha constant for blending	0
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant
Layer 1 - Alpha constant for blending	0
Layer 1 - Default Alpha value	0
Layer 1 - Blending Factor1	Alpha constant
Layer 1 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image	0

Width)	
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	0
Layer 1 - Color Frame Buffer Start Adress	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	0
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	0

7.22. PWR

mode: Wake-Up 1

mode: Wake-Up 3

mode: Wake-Up 4

7.23. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.23.1. Parameter Settings:

Core(s) Settings:

Context(s):	Boot ROM Boot loader Cortex-A7 secure Cortex-A7 non secure Cortex-M4
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Spread spectrum mode:

PLL1 CSG mode	DISABLED
PLL2 CSG mode	DISABLED
PLL3 CSG mode	DISABLED
PLL4 CSG mode	DISABLED

RCC Parameters:

TIM Group1 Prescaler Selection	Disabled
TIM Group2 Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator medium high drive capability

CSI Calibration Value	16
HSI Calibration Value	16
HSI clock calibration feature	Enable
CSI clock calibration feature	Enable
Periodic calibration Value	60

System Parameters:

VDD voltage (V)	3.3

PLL1 configuration:

User defined configuration	FALSE

7.24. RTC

mode: Activate Clock Source

7.24.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 secure Cortex-A7 non secure
Initialized Context:	Cortex-A7 secure
Power Domain:	

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

7.25. SAI1

Mode: Master with Master Clock Out

Mode: Master with Master Clock Out

7.25.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

SAI A:

Synchronization Inputs	Asynchronous

Protocol	Free
Audio Mode	Master Transmit
Frame Length	8 bits
Data Size	24 Bits
Slot Size	DataSize
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
First Bit	MSB First
Frame Synchro Active Level Length	1
Frame Synchro Definition	Start Frame
Frame Synchro Polarity	Active Low
Frame Synchro Offset	First Bit
First Bit Offset	0
Number of Slots	1
Slot Active Final Value	0x00000000
Slot Active	Neither
Clock Source	SAI PLL Clock
Master Clock Divider	Enabled
Audio Frequency	192 KHz
Real Audio Frequency	**156.25 KHz ***
Error between Selected	**-18.61 % ***
Clock Strobing	Falling Edge
Fifo Threshold	Empty
Output Drive	Disabled
Master Clock Over Sampling	Disabled

SAI B:

Synchronization Inputs	Asynchronous
Protocol	Free
Audio Mode	Master Transmit
Frame Length	8 bits
Data Size	24 Bits
Slot Size	DataSize
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
First Bit	MSB First
Frame Synchro Active Level Length	1
Frame Synchro Definition	Start Frame
Frame Synchro Polarity	Active Low
Frame Synchro Offset	First Bit
First Bit Offset	0

Number of Slots	1
Slot Active Final Value	0x00000000
Slot Active	Neither
Clock Source	SAI PLL Clock
Master Clock Divider	Enabled
Audio Frequency	192 KHz
Real Audio Frequency	**156.25 KHz ***
Error between Selected	**-18.61 % ***
Clock Strobing	Falling Edge
Fifo Threshold	Empty
Output Drive	Disabled
Master Clock Over Sampling	Disabled

7.26. SAI2

Mode: Master with Master Clock Out

Mode: Master with Master Clock Out

7.26.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

SAI A:

Synchronization Inputs	Asynchronous
Protocol	Free
Audio Mode	Master Transmit
Frame Length	8 bits
Data Size	24 Bits
Slot Size	DataSize
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
First Bit	MSB First
Frame Synchro Active Level Length	1
Frame Synchro Definition	Start Frame
Frame Synchro Polarity	Active Low
Frame Synchro Offset	First Bit
First Bit Offset	0
Number of Slots	1

Slot Active Final Value	0x00000000
Slot Active	Neither
Clock Source	SAI PLL Clock
Master Clock Divider	Enabled
Audio Frequency	192 KHz
Real Audio Frequency	**156.25 KHz ***
Error between Selected	**-18.61 % ***
Clock Strobing	Falling Edge
Fifo Threshold	Empty
Output Drive	Disabled
Master Clock Over Sampling	Disabled

SAI B:

Synchronization Inputs	Asynchronous
Protocol	Free
Audio Mode	Master Transmit
Frame Length	8 bits
Data Size	24 Bits
Slot Size	DataSize
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
First Bit	MSB First
Frame Synchro Active Level Length	1
Frame Synchro Definition	Start Frame
Frame Synchro Polarity	Active Low
Frame Synchro Offset	First Bit
First Bit Offset	0
Number of Slots	1
Slot Active Final Value	0x00000000
Slot Active	Neither
Clock Source	SAI PLL Clock
Master Clock Divider	Enabled
Audio Frequency	192 KHz
Real Audio Frequency	**156.25 KHz ***
Error between Selected	**-18.61 % ***
Clock Strobing	Falling Edge
Fifo Threshold	Empty
Output Drive	Disabled
Master Clock Over Sampling	Disabled

7.27. SDMMC1

Mode: SD 4 bits Wide bus

7.27.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMCCLK clock divide factor	0

7.28. SDMMC2

Mode: MMC 8 bits Wide bus

7.28.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMCCLK clock divide factor	0

7.29. SPI2

Mode: Full-Duplex Master

7.29.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4

Initialized Context:	Cortex-M4
Power Domain:	

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	4
Baud Rate	**25.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.30. SPI5

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.30.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	4
Baud Rate	**16.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.31. SYS

Timebase Source: SysTick

7.32. TAMP

mode: Activated

7.33. UART4

Mode: Asynchronous

7.33.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.34. UART5

Mode: Asynchronous

7.34.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.35. UART7

Mode: Asynchronous

7.35.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable

MSB First	Disable

7.36. USART1

Mode: Asynchronous

7.36.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.37. USART2

Mode: Asynchronous

7.37.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.38. USART3

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

7.38.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration
Polarity	High
Assertion Time	0
Deassertion Time	0

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.39. USART6

Mode: Asynchronous

7.39.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.40. USBH_HS1
mode: USB Host controller

7.41. USB_OTG_HS
High Speed: OTG/Dual_Role_Device Type C
mode: Activate_VBUS

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
ADC1	ANA0	ADC1_INP0	Analog mode	n/a	n/a		Cortex-A7 non secure	
	ANA1	ADC1_INP1	Analog mode	n/a	n/a		Cortex-A7 non secure	
DAC1	PA5	DAC1_OUT2	Analog mode	n/a	n/a		Cortex-A7 non secure	
	PA4	DAC1_OUT1	Analog mode	n/a	n/a		Cortex-A7 non secure	
DCMI	PE13	DCMI_D6	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PH11	DCMI_D2	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PH14	DCMI_D4	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PH8	DCMI_HSYNC	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PE1	DCMI_D3	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PC7	DCMI_D1	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PH9	DCMI_D0	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PI7	DCMI_D7	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PI5	DCMI_VSYNC	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PI4	DCMI_D5	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PA6	DCMI_PIXCLK	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
DDR	DDR_DQ20	DDR_DQ20	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ23	DDR_DQ23	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ19	DDR_DQ19	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ16	DDR_DQ16	n/a	n/a	n/a		Boot loader Cortex-A7	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
							secure	
	DDR_DQS2N	DDR_DQS2N	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQS2P	DDR_DQS2P	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQM2	DDR_DQM2	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ22	DDR_DQ22	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ17	DDR_DQ17	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ18	DDR_DQ18	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ3	DDR_DQ3	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ0	DDR_DQ0	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ21	DDR_DQ21	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A7	DDR_A7	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_RESETN	DDR_RESETN	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ1	DDR_DQ1	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A13	DDR_A13	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ7	DDR_DQ7	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQM0	DDR_DQM0	n/a	n/a	n/a		Boot loader Cortex-A7 secure	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	DDR_DQS0N	DDR_DQS0N	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQS0P	DDR_DQS0P	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A9	DDR_A9	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A5	DDR_A5	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ5	DDR_DQ5	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ2	DDR_DQ2	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ6	DDR_DQ6	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A2	DDR_A2	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A3	DDR_A3	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ4	DDR_DQ4	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_BA2	DDR_BA2	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A0	DDR_A0	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_BA0	DDR_BA0	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DTO1	DDR_DTO1	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_ZQ	DDR_ZQ	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_CSN	DDR_CSN	n/a	n/a	n/a		Boot loader Cortex-A7	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
							secure	
	DDR_ODT	DDR_ODT	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DTO0	DDR_DTO0	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A1	DDR_A1	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_RASN	DDR_RASN	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_WEN	DDR_WEN	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_CASN	DDR_CASN	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A10	DDR_A10	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A12	DDR_A12	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_CLKP	DDR_CLKP	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_CLKN	DDR_CLKN	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ8	DDR_DQ8	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A14	DDR_A14	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A11	DDR_A11	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ10	DDR_DQ10	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_BA1	DDR_BA1	n/a	n/a	n/a		Boot loader Cortex-A7 secure	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	DDR_CKE	DDR_CKE	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ13	DDR_DQ13	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ9	DDR_DQ9	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQS1N	DDR_DQS1N	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A4	DDR_A4	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ11	DDR_DQ11	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQM1	DDR_DQM1	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQS1P	DDR_DQS1P	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A8	DDR_A8	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_A6	DDR_A6	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ14	DDR_DQ14	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ12	DDR_DQ12	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ15	DDR_DQ15	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ24	DDR_DQ24	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ25	DDR_DQ25	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ31	DDR_DQ31	n/a	n/a	n/a		Boot loader Cortex-A7	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
							secure	
	DDR_DQ30	DDR_DQ30	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQS3P	DDR_DQS3P	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQS3N	DDR_DQS3N	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_ATO	DDR_ATO	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ29	DDR_DQ29	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ28	DDR_DQ28	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQM3	DDR_DQM3	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_VREF	DDR_VREF	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ27	DDR_DQ27	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
	DDR_DQ26	DDR_DQ26	n/a	n/a	n/a		Boot loader Cortex-A7 secure	
DEBUG	JTDI	DEBUG_JTDI	n/a	n/a	n/a		Cortex-A7 non secure	
	JTCK-SWCLK	DEBUG_JTCK-SWCLK	n/a	n/a	n/a		Cortex-A7 non secure	
	NJTRST	DEBUG_JTRST	n/a	n/a	n/a		Cortex-A7 non secure	
	JTDO-TRACESWO	DEBUG_JTDO-SWO	n/a	n/a	n/a		Cortex-A7 non secure	
	JTMS-SWDIO	DEBUG_JTMS-SWDIO	n/a	n/a	n/a		Cortex-A7 non secure	
ETH1	PG12	ETH1_PHY_INTN	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PG11	ETH1_TX_CTL	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PA1	ETH1_RX_CLK	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PB13	ETH1_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure	
	PH6	ETH1_RXD2	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PH7	ETH1_RXD3	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PC2	ETH1_TXD2	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure	
	PE2	ETH1_TXD3	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure	
	PA7	ETH1_RX_CTL	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PG13	ETH1_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure	
	PC5	ETH1_RXD1	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PA2	ETH1_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PC1	ETH1_MDC	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure	
	PG4	ETH1_GTX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	High		Cortex-A7 non secure	
	PC4	ETH1_RXD0	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
FDCAN1	PD1	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PD0	FDCAN1_RX	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
HDMI_CEC	PA15	CEC	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 non secure	
I2C1	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PF14	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 non secure	
I2C2	PH5	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PF1	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 non secure	
I2C4	PZ4	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 secure	
	PZ5	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 secure	
I2C5	PA12	I2C5_SDA	Alternate Function	No pull-up and no pull-	Low		Cortex-A7 non	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
			Open Drain	down			secure	
	PA11	I2C5_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low		Cortex-A7 non secure	
I2S1	PZ3	I2S1_WS	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PZ0	I2S1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PZ6	I2S1_MCK	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PZ1	I2S1_SDI	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PZ2	I2S1_SDO	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
LTDC	PH4	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PK6	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PK4	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PJ13	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PD10	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PH10	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PE14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PK7	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PK3	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PJ14	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PJ12	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PE15	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PK5	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PI0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PH13	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PE11	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PI1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PI15	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PH12	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PC10	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PI13	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PI12	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PJ8	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PJ0	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PJ4	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PJ2	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PJ7	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PB5	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
PWR	PI8	PWR_WKUP4	n/a	n/a	n/a		Cortex-A7 secure* Cortex-A7 non	
	PC13	PWR_WKUP3	n/a	n/a	n/a		Cortex-A7 secure* Cortex-A7 non	
	PA0	PWR_WKUP1	n/a	n/a	n/a		Cortex-A7 secure* Cortex-A7 non	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a		Boot ROM Boot loader Cortex-A7	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a		Boot ROM Boot loader Cortex-A7	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a		Boot ROM Boot loader Cortex-A7	
SAI1	PE5	SAI1_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PG15	SAI1_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PD6	SAI1_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PG7	SAI1_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PF7	SAI1_MCLK_B	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PF6	SAI1_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PF8	SAI1_SCK_B	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PF9	SAI1_FS_B	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
SAI2	PE0	SAI2_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PE12	SAI2_SCK_B	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PI6	SAI2_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PC0	SAI2_FS_B	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PD13	SAI2_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PF11	SAI2_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PD12	SAI2_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PH3	SAI2_MCLK_B	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
SDMMC1	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PE6	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-A7 non secure	
	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
SDMMC2	PE3	SDMMC2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-A7 non secure	
	PB3	SDMMC2_D2	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PB14	SDMMC2_D	Alternate Function	No pull-up and no pull-	Medium		Cortex-A7 non	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
		0	Push Pull	down			secure	
	PD3	SDMMC2_D7	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PB15	SDMMC2_D1	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PB4	SDMMC2_D3	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PG6	SDMMC2_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PC6	SDMMC2_D6	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PB9	SDMMC2_D5	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
	PE4	SDMMC2_D4	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	
SPI2	PI2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-M4	
	PI3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-M4	
	PB10	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-M4	
SPI5	PK0	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-M4	
	PK1	SPI5_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-M4	
	PJ10	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-M4	
	PJ11	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-M4	
UART4	PI9	UART4_RX	Alternate function	No pull-up and no pull-down	n/a		Cortex-M4	
	PA13	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	
UART5	PB6	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PB12	UART5_RX	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
UART7	PA8	UART7_RX	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PE8	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PA10	USART1_RX	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PF4	USART2_RX	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
	PD9	USART3_RX	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PG8	USART3_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
USART6	PG9	USART6_RX	Alternate function	No pull-up and no pull-down	n/a		Cortex-A7 non secure	
	PG14	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	
USBH_HS1	USB_DP1	USBH_HS1_DP	n/a	n/a	n/a		Cortex-A7 non secure	
	USB_DM1	USBH_HS1_DM	n/a	n/a	n/a		Cortex-A7 non secure	
USB_OTG_HS	OTG_VBUS	USB_OTG_HS_VBUS	n/a	n/a	n/a		Cortex-A7 non secure	
	USB_DM2	USB_OTG_HS_DM	n/a	n/a	n/a		Cortex-A7 non secure	
	USB_DP2	USB_OTG_HS_DP	n/a	n/a	n/a		Cortex-A7 non secure	
Single Mapped Signals	DSIHOST_D0N	DSIHOST_D0N	n/a	n/a	n/a			
	DSIHOST_CKN	DSIHOST_CKN	n/a	n/a	n/a			
	DSIHOST_D1N	DSIHOST_D1N	n/a	n/a	n/a			
	DSIHOST_D0P	DSIHOST_D0P	n/a	n/a	n/a			
	DSIHOST_CKP	DSIHOST_CKP	n/a	n/a	n/a			
	DSIHOST_D1P	DSIHOST_D1P	n/a	n/a	n/a			

* Initialized context

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SAI1_A	DMA1_Stream1	Memory To Peripheral	Low
SAI1_B	DMA1_Stream2	Memory To Peripheral	Low
SAI2_A	DMA1_Stream3	Memory To Peripheral	Low
SAI2_B	DMA1_Stream4	Memory To Peripheral	Low
DCMI	DMA1_Stream0	Peripheral To Memory	Low

SAI1_A: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Word
Memory Data Width:	Word

SAI1_B: DMA1_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Word
Memory Data Width:	Word

SAI2_A: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Word
Memory Data Width:	Word

SAI2_B: DMA1_Stream4 DMA request Settings:

Mode:	Normal

Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Word
Memory Data Width:	Word

DCMI: DMA1_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Word

8.3. MDMA configuration

nothing configured in DMA service

8.4. NVIC configuration

8.4.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
RCC global interrupt	unused		
SPI2 global interrupt	unused		
UART4 global interrupt	unused		
FPU global interrupt	unused		
SPI5 global interrupt	unused		
IPCC RX1 occupied interrupt	unused		
IPCC TX1 free interrupt	unused		
HSEM interrupt 2	unused		
Cortex-A7 send event interrupt through EXTI line 66	unused		
RCC wake-up interrupt	unused		

8.4.2. NVIC Code generation

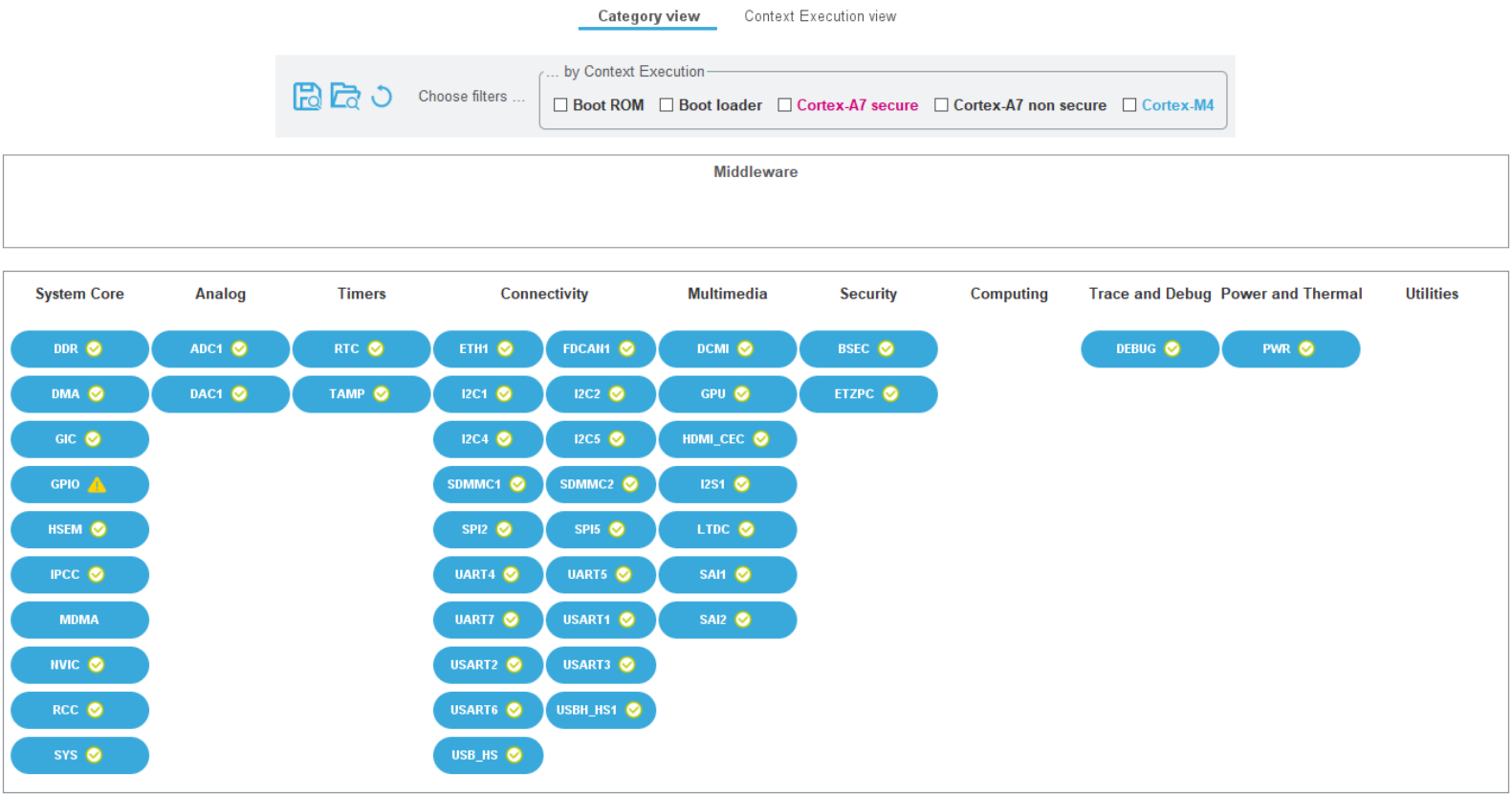
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Pre-fetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	true	false
Debug monitor	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true

*** User modified value**

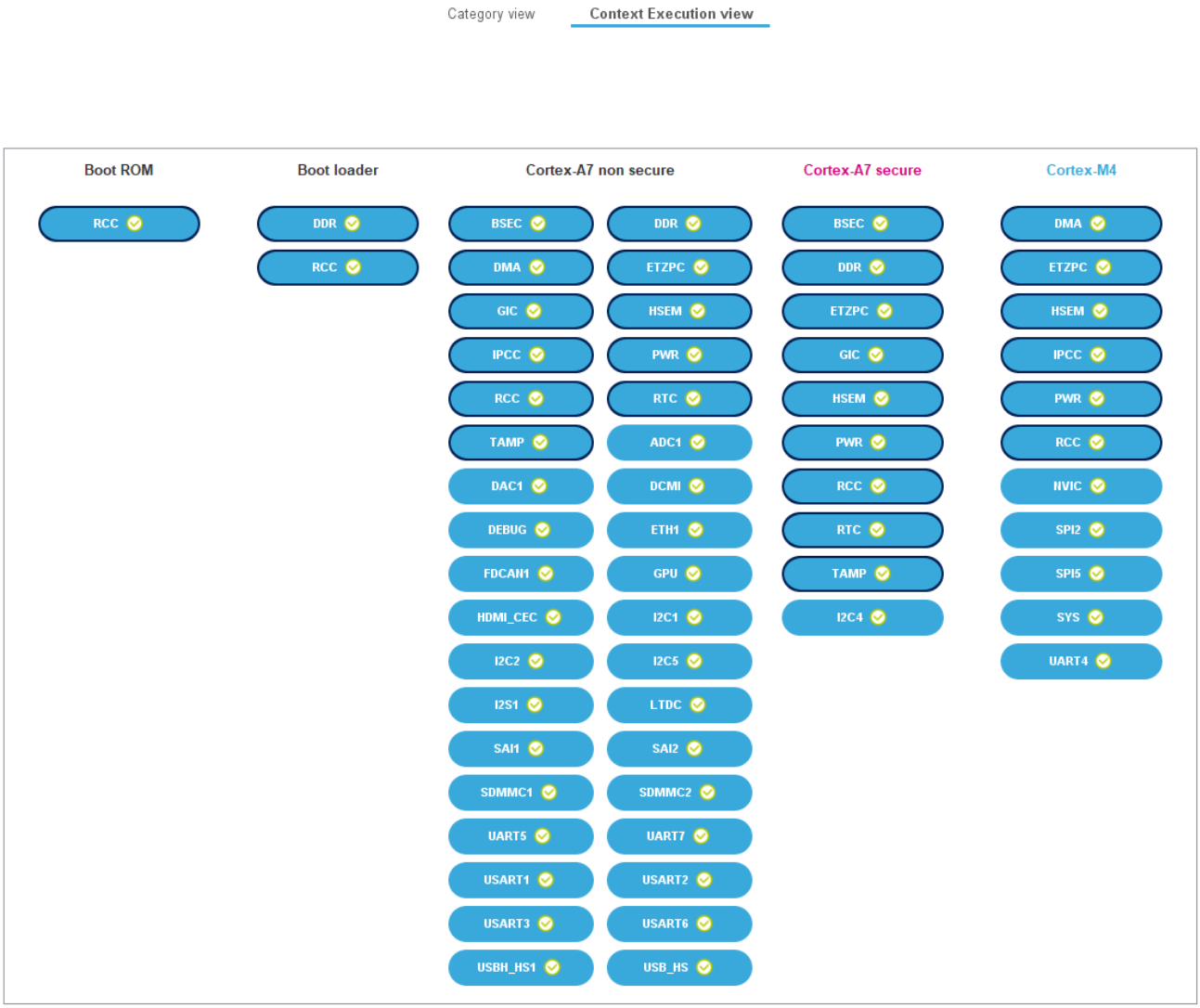
9. System Views

9.1. Category view

9.1.1. Current



9.2. Context Execution view



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00489389.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00327659.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00596687.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00516256.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00389996.pdf
Application note	http://www.st.com/resource/en/application_note/DM00449434.pdf
Application note	http://www.st.com/resource/en/application_note/DM00462392.pdf
Application note	http://www.st.com/resource/en/application_note/DM00505673.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00560967.pdf
Application note	http://www.st.com/resource/en/application_note/DM00595472.pdf
Application note	http://www.st.com/resource/en/application_note/DM00561921.pdf
Application note	http://www.st.com/resource/en/application_note/DM00589815.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00564136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00681502.pdf