Qiaochu Zhang

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EDUCATION

University of Southern California, Los Angeles, CA, USA 2017 - 2023
Ph.D. in Electrical Engineering, GPA: 3.93/4.00
Advisor: Prof. Mike Shuo-Wei Chen

Fudan University, Shanghai, China 2013 - 2017
B.S. in Physics, Ranking: 2/121, GPA: 3.72/4.00

RESEARCH INTERESTS

- High-performance digital-intensive mixed-signal circuit design, including data converters, all digital phase-locked loops, analog computing platforms, etc.
- Machine-learning-based computer-aided design algorithms.
- Circuits and systems using emerging devices and materials, such as memristors, 2D materials, etc.

HONORS AND AWARDS

2022-2023 IEEE Solid-State Circuits Society Predoctoral Achievement Award	2022
ISSCC 2023 Student Travel Grant Award	2022
Ming Hsieh Institute Ph.D. Scholar, University of Southern California	2021 - 2022
Provost's Fellowship, University of Southern California	2017 - 2020
Top Student in National Talented Student Training Program, Ministry of Education, China	2017
Outstanding Graduate, Fudan University	2017
Honor Student, Fudan University	2015 - 2017
Hong Kong Caring Sponsored Scholarship, Fudan University	2014

PUBLICATIONS

1. **Qiaochu Zhang**, Hsiang-Chun Cheng, Shiyu Su, and Mike Shuo-Wei Chen, "Fractional-N Digital MDLL with Injection-Error Scrambling and Calibration", *IEEE Journal of Solid-State Circuits* (Accepted)
2. Shiyu Su*, **Qiaochu Zhang***, and Mike Shuo-Wei Chen, "A 2GS/s 8.5-Bit Time-Based ADC Using a Segmented Stochastic Flash TDC", in *2023 IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2023 (* equal contribution)
3. **Qiaochu Zhang**, Hsiang-Chun Cheng, Shiyu Su, and Mike Shuo-Wei Chen, "A Fractional-N Digital MDLL with Injection-Error Scrambling and Background Third-Order DTC Delay Equalizer Achieving –67dBc Fractional Spur", in *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2023
4. **Qiaochu Zhang***, Shiyu Su*, and Mike Shuo-Wei Chen, "A Cost-Efficient Fully Synthesizable Stochastic Time-to-Digital Converter Design Based on Integral Nonlinearity Scrambling", in *2022 59th IEEE/ACM Design Automation Conference (DAC)*, Jul. 2022 (* equal contribution)
5. **Qiaochu Zhang**, Shiyu Su, Cheng-Ru Ho, and Mike Shuo-Wei Chen, "A Fractional-N Digital MDLL with Background Two-Point DTC Calibration", *IEEE Journal of Solid-State Circuits*, Jan. 2022
6. **Qiaochu Zhang**, Shiyu Su, Cheng-Ru Ho, and Mike Shuo-Wei Chen, "A Fractional-N Digital MDLL with Background Two-Point DTC Calibration Achieving -60dBc Fractional Spur", in *IEEE International Solid-State Circuits Conference*

(ISSCC), Feb. 2021

7. **Qiaochu Zhang**, Shiyu Su, Juzheng Liu, and Mike Shuo-Wei Chen, "CEPA: CNN-based Early Performance Assertion Scheme for Analog and Mixed-Signal Circuit Simulation", in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2020
8. Mayank Palaria, Shiyu Su, Hsiang-Chun Cheng, Rezwan A. Rasul, **Qiaochu Zhang**, Soumya Mahapatra, Chong Fatt Law, Sushmit Hossain, Ryan Bena, Wei Wu, Quan Nguyen, Mike Shuo-Wei Chen, "Analog Kalman Filter with Integration and Digitization via a Shared Thyristor-Based VCO for Sensor Fusion in 65 nm CMOS", in *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Sep. 2023.
9. Hsiang-Chun Cheng, Shiyu Su, Mayank Palaria, **Qiaochu Zhang**, Ce Yang, Sushmit Hossain, Ryan Bena, Buyun Chen, Zerui Liu, Juzheng Liu, Rezwan Rasul, Quan Nguyen, Wei Wu, Mike Shuo-Wei Chen, "A Memristor-Based Analog Accelerator for Solving Quadratic Programming Problems", in *2023 IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2023
10. Shiyu Su, **Qiaochu Zhang**, Juzheng Liu, Mohsen Hassanpourghadi, Rezwan Rasul, and Mike Shuo-Wei Chen, "TAFA: Design Automation of Analog Mixed-Signal FIR Filters Using Time Approximation Architecture", in *IEEE/ACM 27th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022
11. Shiyu Su, **Qiaochu Zhang**, Mohsen Hassanpourghadi, Juzheng Liu, Rezwan Rasul, and Mike Shuo-Wei Chen, "Analog/Mixed-Signal Circuit Synthesis Enabled by the Advancements of Circuit Architectures and Machine Learning Algorithms", in *IEEE/ACM 27th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022
12. Mohsen Hassanpourghadi, Shiyu Su, Rezwan Rasul, Juzheng Liu, **Qiaochu Zhang**, and Mike Shuo-Wei Chen, "Circuit Connectivity Inspired Neural Network for Analog Mixed-Signal Functional Modeling", in *2021 58th IEEE/ACM Design Automation Conference (DAC)*, Dec. 2021
13. Juzheng Liu, Shiyu Su, Meghna Madhusudan, Mohsen Hassanpourghadi, Samuel Saunders, **Qiaochu Zhang**, Rezwan Rasul, Yaguang Li, Jiang Hu, Arvind Kumar Sharma, Sachin S. Sapatnekar, Ramesh Harjani, Anthony Levi, Sandeep Gupta, and Mike Shuo-Wei Chen, "From Specification to Silicon: Towards Analog/Mixed-Signal Design Automation using Surrogate NN Models with Transfer Learning", in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2021
14. Juzheng Liu, Mohsen Hassanpourghadi, **Qiaochu Zhang**, Shiyu Su, and Mike Shuo-Wei Chen, "Transfer Learning with Bayesian Optimization-Aided Sampling for Efficient AMS Circuit Modeling", in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2020
15. Mohsen Hassanpourghadi, **Qiaochu Zhang,** Praveen Sharma, Jaewon Nam, Shiyu Su, Subhajit Chowdhury, Jagannathan Sathyamoorthy, Walter Unglaub, Fangzhou Wang, Mike Shuo-Wei Chen, Sandeep Gupta, Anthony Levi, Wes Hansford, William Taylor, "Automated Analog Mixed Signal IP Generator for CMOS Technologies", in *Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, Mar. 2019.
16. Wu Zan, **Qiaochu Zhang**, Hu Xu, Fuyou Liao, Jing Wan, Jianan Deng, Hao Zhu, Lin Chen, Qingqing Sun, Shijin Ding, Peng Zhou, Wenzhong Bao and David Wei Zhang, "Large Capacitance and Fast Polarization Response of Thin Polymer Electrolyte Dielectrics by Spin-Coating for Two Dimensional MoS_2 Devices", *Nano Research*, Dec. 2017
17. Xiongfei Song, Zhongxun Guo, **Qiaochu Zhang**, Peng Zhou, Wenzhong Bao and David Wei Zhang, "Progress of Large-Scale Synthesis and Electronic Device Application of Two-Dimensional Transition Metal Dichalcogenides", *Small*, Jul. 2017

RESEARCH EXPERIENCE

University of Southern California

Bio-inspired hybrid computing platform for micro air vehicles (MAVs) 2021 - present

Sponsor: **IARPA**, Microelectronics in Support of Artificial Intelligence (MicroE4AI) program.

- Implemented a LP/QP solver using CMOS circuits and memristors for MAV flight control application, achieving high computational accuracy and low latency.
- Implemented compact and low power data converters for the computing platform of MAV control.

- Published one paper in ***CICC*** and one paper in ***ESSCIRC***.

High-speed time-based stochastic analog-to-digital converters (ADCs) 2021 - present
Sponsor: **IARPA**, Microelectronics in Support of Artificial Intelligence (MicroE4AI) program; **DARPA**, Posh Open-Source Hardware (POSH) program; **GlobalFoundries**.

- Explored stochastic ADC architectures that can achieve high dynamic range, occupy small power/area, and be synthesized by digital tools.
- Implemented an 8.5-bit 2 GS/s ADC prototype in 65 nm CMOS with a synthesizable stochastic time-to-digital converter (TDC) and a high-speed linear voltage-to-time converter (VTC).
- Implemented a 12-bit 100 MS/s TDC prototype in 12 nm FinFET with dithering and an approximated adder.
- Published one paper in ***DAC*** and one paper in ***CICC***.

All digital injection-locked phase-locked loops (PLLs) 2018 - present
Sponsor: **DARPA**, Posh Open-Source Hardware (POSH) program; **NSF**, Spectrum Efficiency, Energy Efficiency, and Security (SpecEES) program.

- Explored ring oscillator-based injection locked PLL architectures and associated DSP algorithms for achieving low noise and low spur at the same time.
- Implemented a PLL prototype in 65 nm CMOS that achieves –67 dBc fractional spur using injection error scrambling and third order DTC delay equalizer.
- Implemented a PLL prototype in 65 nm CMOS that achieves –60 dBc fractional spur using two-point DTC error calibration and a dithered TDC with adaptive comb-filter-assisted dither removal technique.
- Published two papers in ***ISSCC*** and two papers in ***JSSC***.

Computer-aided design for analog and mixed-signal circuits 2017 - 2022
Sponsor: **DARPA**, Posh Open-Source Hardware (POSH) program; **GlobalFoundries**.

- Utilized convolutional neural network (CNN) to quickly predict circuit performance using a short duration of transient waveform, achieving a much higher accuracy and speed compared with a human designer.
- Applied transfer learning and Bayesian optimization-aided sampling to reduce the training dataset size when dealing with post-layout iteration and technology migration.
- Constructed neural network structures reflecting the circuit topologies for improving modeling accuracy.
- Explored design automation flow for large circuit blocks from specification to layout.
- Published three papers in ***ICCAD***, one paper in ***DAC***, two papers in ***ASP-DAC***, and one paper in ***GOMACTech***.

Fudan University

High-performance MoS_2 transistor based integrated circuits 2016 - 2017
Sponsor: National Key Research and Development Program; Natural Science Foundation of Shanghai.

- Fabricated high performance MoS_2 transistors with ionic thin film electrolyte for foldable electronic applications.
- Modeled the frequency response of MoS_2 transistors and tuned the fabrication process based on simulation results.
- Demonstrated logic circuits using the MoS_2 transistors.
- Published one paper in ***Nano Research*** and one paper in ***Small*** and defended as the undergraduate thesis.

TEACHING EXPERIENCE

Teaching Assistant, **EE631 Mixed-Signal Integrated Circuits**, USC Spring 2022

- Graduate-level course with 18 master and PhD students.
- Led discussion sessions, held office hours, designed curriculum, and graded homework.

Teaching Assistant, **EE536B Advanced Mixed-Signal Circuit Design**, USC Spring 2020

- Graduate-level course with 15 master and PhD students.
- Led discussion sessions, held office hours, designed curriculum, and graded homework.
- Introduced machine-learning-based CAD tools in an analog circuit design class for the first time at USC.

SERVICE

Organizer, Ming Hsieh Institute Seminar Series on Integrated Systems, USC Fall 2021
- Organized eight seminars delivered by professors/engineers from other institutions (20+ audiences each seminar).

Co-organizer, Ming Hsieh Institute Research Festival, USC Fall 2021
- Organized poster sessions for PhD students from ECE department (90+ presenters).

Mentor, USC-Tsinghua undergraduate researcher program Summer 2019
- Mentored an undergraduate intern from Tsinghua University, whose research results were used in an *ICCAD* paper.

Peer reviewer
- IEEE Journal of Solid-State Circuits 2020 - present
- IEEE Transactions on Circuits and Systems I: Regular Papers 2020 - present
- IEEE Transactions on Circuits and Systems II: Express Briefs 2021 - present
- IEEE Solid-State Circuits Letters 2020 - present
- IEEE Access 2021 - present

SELECTED TALKS AND POSTERS

"A Fractional-N Digital MDLL with Injection-Error Scrambling and Background Third-Order DTC Delay Equalizer Achieving –67dBc Fractional Spur", AMD-Xilinx, San Jose, CA, Host: Yohan Frans 2023
"A Fractional-N Digital MDLL with Injection-Error Scrambling and Background Third-Order DTC Delay Equalizer Achieving –67dBc Fractional Spur", NXP, San Jose, CA, Host: Sai-Wang (Rocco) Tam 2023
"Towards High-Performance Integrated Systems: Innovations in Circuit Architecture, Design Methodology, and Device Technology", Intel Labs, Hillsboro, OR, Host: Stefano Pellerano 2023
"A fractional-N digital MDLL with injection error scrambling and background third-order DTC delay equalizer", 12th Research Festival, USC 2022
"A fractional-N digital MDLL with background two-point DTC calibration", 11th Research Festival, USC 2021
"Towards more efficient analog and mixed-signal circuits: architecture and optimization innovations", MHI scholar Competition, USC 2021
"Analog and mixed-signal parameter search engine", Advanced Course: Advanced Mixed-Signal Circuit Design, USC 2020
"An automated PLL design using neural networks", 9th Research Festival, USC 2018

REFERENCES

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