

CAGE NO.

DWG NO.

SH

REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

Asynchronous RN sets Q=logi111  
NEED clock to be HIGH TO hold this value!!

Flip tgate0 I4 sideways for LVS

The diagram illustrates a D flip-flop circuit implemented using LVS components. The circuit includes a D input, a clock input (CK), and a Q output. The internal logic consists of several inverters (I10, I11, I12, I17, I18, I19, I20), NAND gates (I12, I18, I20), and OR gates (I10, I11, I12, I17, I18, I19, I20). The circuit is powered by VP and VM. The output Q is connected to a bus labeled 'ZS'.

UPDATED  
Jan 1 19:50:40 2016

DRAWN

CHECKED

CHECKED

ISSUED

df fs

SIZECAGE NO.DWG NO.

REV

SCALE

SHEET

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