Module: Delay Block in 65nm CMOS

Description:

A delay line is an essential circuit block and is frequently used in circuit designing. In this design a voltage controlled delay line is implemented. The delay of the single element is controlled by the externally applied voltage and this gives a coarse grain control on the delay adjustment. Besides the design also has fine grain skew adjustment provisions. The simplified circuit diagram of the delay element is:

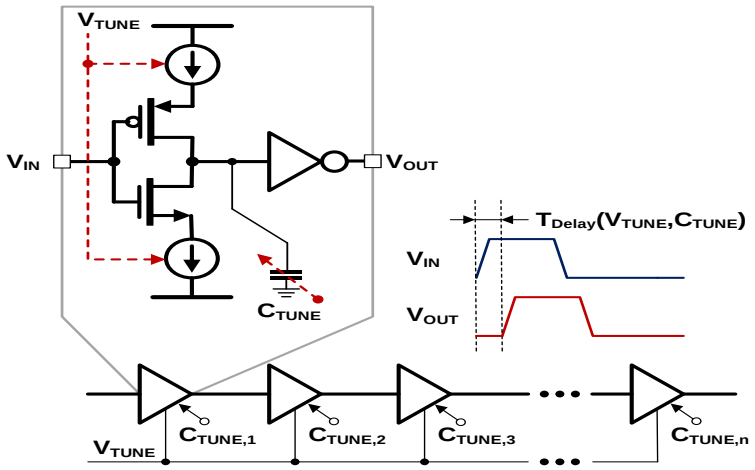
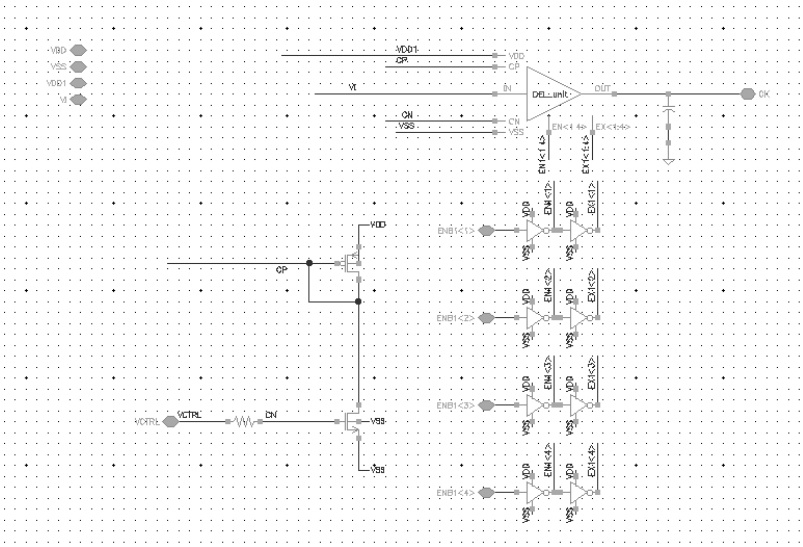


Figure 1: Simplified circuit diagram for the single Delay element

The figure shows the simplified circuit diagram for the single delay element. The Delay element has 2 types of control – coarse delay adjustment and the fine skew adjustment. The coarse delay adjustment is done by changing the current and the fine skew adjustment is done by changing the capacitors (CTUNE).

Top Cell Name: delay_block_cell

Schematic:



Parameterized Module:

Here a single delay element has been parameterized. The parameters are basically the knobs that a user can control in order to get the desired metric i.e. in this example the delay of the delay element or the power consumption of each element for a given sizing. The regression model used the delay element is:

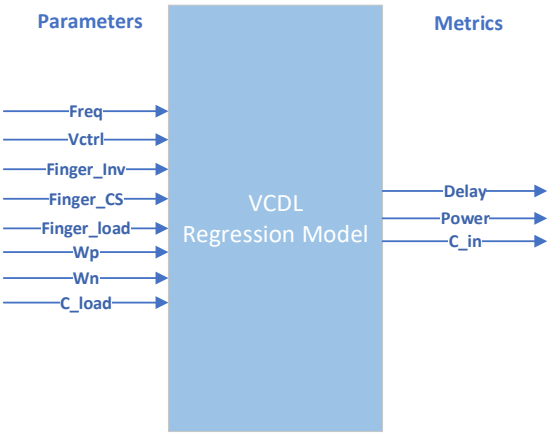


Figure 2: Regression model for the Delay Element

For this module the design metrics and the design parameters are as follows:

Design Parameters	
Parameters	Symbols
Input Signal Frequency	Freq
Control Voltage	Vctrl
# fingers of the inverter transistors	Finger_inv
#fingers of the current source transistors	Finger_cs
#fingers of the CTUNE transistors	Finger_load
Load Capacitance	C_load
Width of NMOS	Wn
Width of PMOS	Wp

Table-I. Design parameters for the delay element

Design Metrics	
Metrics	**Symbols**
Delay of the single delay element	Delay
Power Consumption	Power
Input Capacitance	C_in

Table-II. Design metrics for the Delay element

Designer's knowledge is always used to choose the circuit parameters wisely. The chosen parameters over here are: 1) Fingers of the Inverter Transistors (NMOS and PMOS) – both the transistors must be sized together in order to ensure equal rise and fall time, 2) Fingers of the current source transistors(PMOS and NMOS sized together) , 3) Fingers of the C_{tune} transistors, 4) Input signal Frequency – for observing the frequency range over which the delay line is functional, 5) Control Voltage for changing the delay and finally 6) Load Capacitance for capturing the next stage loading effect.

Module characterization

Based on previous analysis and the knowledge from known good design, we can define the search space. The table below shows the summary.

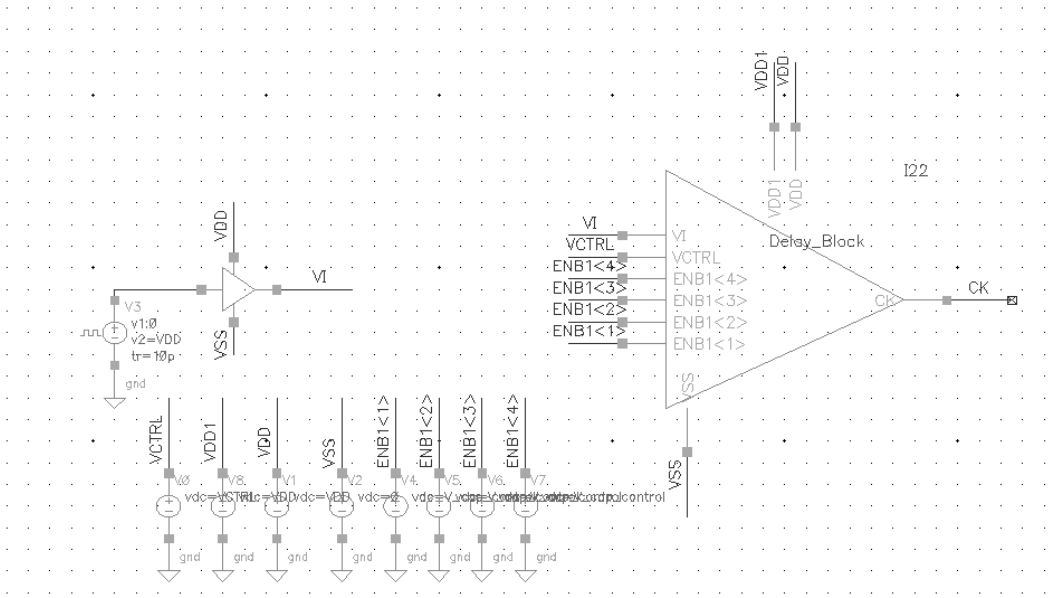
Design Parameters		
Parameters	Symbols	Search Range
Input Signal Frequency	freq	[500MHz, 1GHz, 2GHz]
Control Voltage	Vctrl	[0.5-0.9]V
# fingers of the inverter transistors	finger_inv	[1,4]
#fingers of the current source transistors	finger_cs	[1,4]
#fingers of the CTUNE transistors	Finger_load	[1,4]
Load Capacitance	C_load	[10fF-80fF]
Width of NMOS	Wn	[200nm-800nm]
Width of PMOS	Wp	[400nm-1600nm]

Table-III. Design parameters search space for the VCDL module.

Pin Configuration of the module:

Pin Configuration	
Pin Names	Function
VI	Input Signal
VSS	Ground
VDD, VDD1	Supply Voltage
VCTRL	Delay Control
ENB1<1:4>	Skew Control
CK	Output

Test Bench:



Test Bench Netlist: delayblock_pd.scs; delayunitipcap.scs

Neural Network Model:

H5 File: Delay_Element.h5

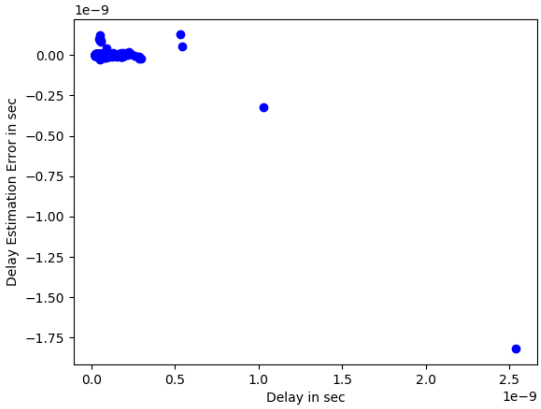
JSON File: Delay_Element.json

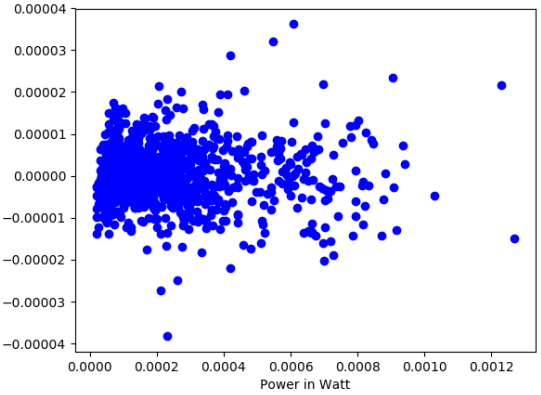
Input Normalization File: scX_Delay_element.pkl

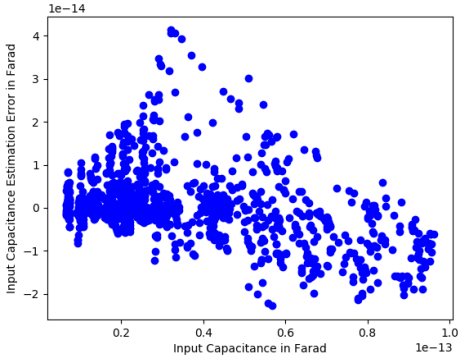
Output Standardization File: scY_Delay_element.pkl

Simulation Result:

Estimation Error for different Metrics:







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