Module: Telescopic Cascode Operational Amplifier

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Date: 1st May 2019

Module Description: Telescpoic Cascode Operational Amplifier utilizes the cascode topology on the pull down and pull up at the same time to achieve high gain and high speed, while sacrifices the swing and input common mode range.

Top Cell Name: AMP_CASCODE65_v1

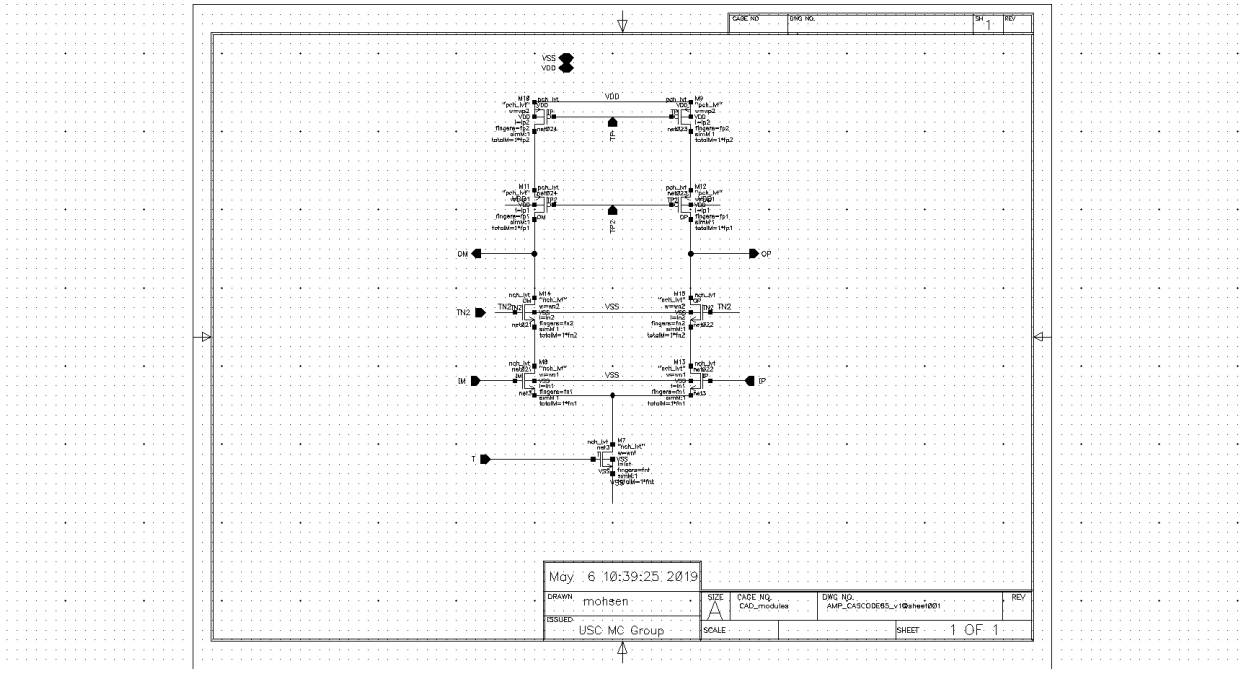
Technology: TSMC 65nm CMOS

PINS:

Pin Lists	
VDD	Supply Voltage
VSS	Ground
TP, TP2, TN2, T	Bias voltages
IM, IP	Input Differential Voltage
OM, OP	Output Differential Voltage

Schematic Netlists: ATC_v1.scs

Schematic figures:



Testbenches: ATC_test.scs

Parameters:

Parameters	Symbols
Top PMOS # of Fingers	$fp2$
Top PMOS Length (m)	$lp2$
Mid PMOS # of Fingers	$fp1$
Mid PMOS Length (m)	$lp1$
Mid NMOS # of Fingers	$fn2$
Mid NMOS Length (m)	$ln2$
Bot NMOS # of Fingers	$fn1$
Bot NMOS Length (m)	$ln1$
Sink NMOS # of Fingers	fnt
Sink NMOS Length (m)	lnt
Sink NMOS Bias (V)	$vttt$
Common Mode Voltage (V)	$vcmin$
Mid NMOS Bias (V)	$vtn2$
Mid PMOS Bias (V)	$vtp2$
Output Capacitive Load (F)	cl

Metrics:

Metrics	Symbols
DC Power Consumption (W)	power
Output Swing Voltage (V)	swing
Common mode voltage gain (dB)	avcm
Differential gain (dB)	avd
Input Capacitance (F)	cin
Unity Gain Bandwidth (Hz)	gbw
Output Noise (V^2/Hz)	outnoise

Neural Network Model:

The H5 file: reg_ATC65.h5

The Json File: model_ATC65.json

The Input Normalization File: scX_ATC65.pkl

The Output Standardization File: scY_ATC65.pkl

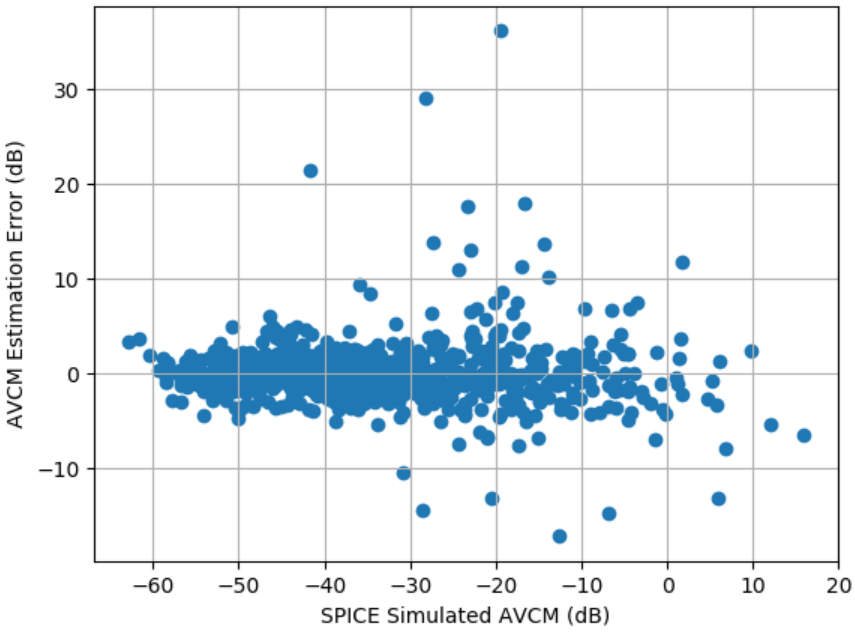
The input characterization range of the Model:

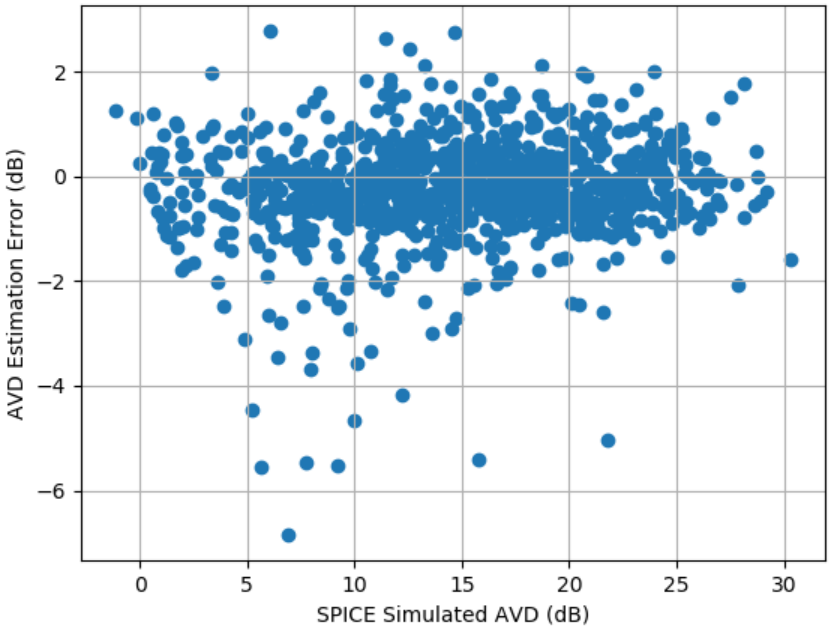
Design parameters	
Symbols	Characterization Range
$\boldsymbol{fp2}$	$4,5,\ldots,200$
$\boldsymbol{lp2}$	$[60nm, 200nm]$
$\boldsymbol{fp1}$	$2,5,\ldots,100$
$\boldsymbol{lp1}$	$[60nm, 200nm]$
$\boldsymbol{fn2}$	$2,5,\ldots,100$
$\boldsymbol{ln2}$	$[60nm, 200nm]$
$\boldsymbol{fn1}$	$2,5,\ldots,100$
$\boldsymbol{ln1}$	$[60nm, 200nm]$
$\boldsymbol{fnt}$	$4,5,\ldots,200$
$\boldsymbol{lnt}$	$[120nm, 400nm]$
$\boldsymbol{vttt}$	$[0.35V, 0.6V]$
$\boldsymbol{vcmin}$	$[0.6V, 0.8V]$
$\boldsymbol{vtn2}$	$[0.7V, 0.95V]$
$\boldsymbol{vtp2}$	$[0.05V, 0.3V]$
$\boldsymbol{cl}$	$[1fF, 10pF]$

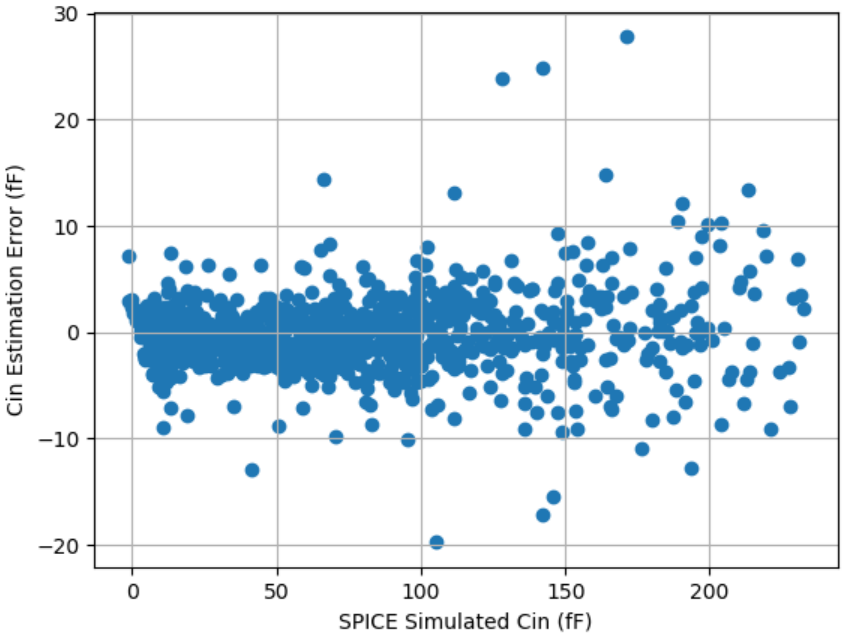
Another parameter ranges:

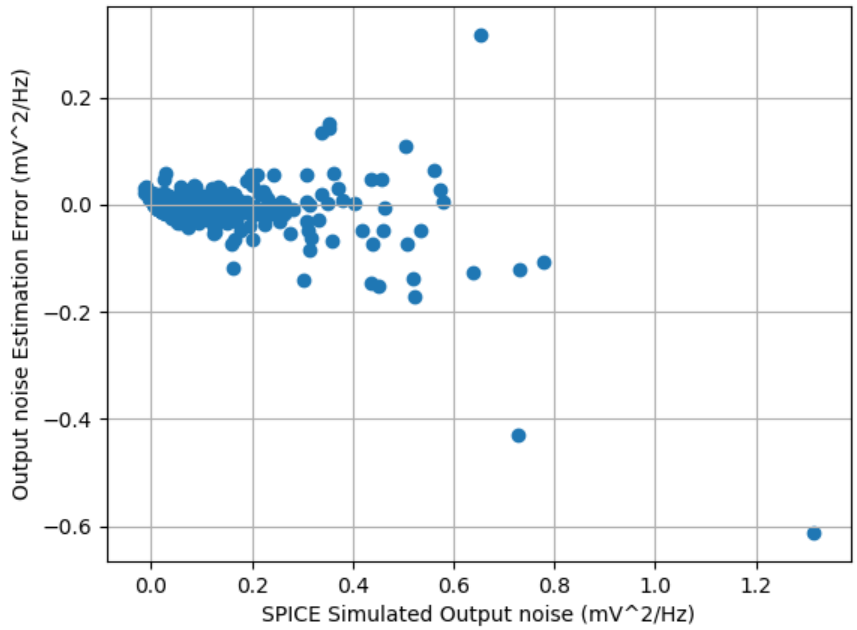
Design parameters		
Symbols	Description	Characterization Range
VDD	Supply Voltage	$1V$
$wp2$	Top PMOS Width	$800nm$
$wp1$	Mid PMOS Width	$800nm$
$wn1$	Mid NMOS Width	$800nm$
$wn2$	Bot NMOS Width	$800nm$
wnt	Sink NMOS Width	$800nm$
rl	Output loading resistance	$1\ G\Omega$
$vcmn$	Loading DC voltage	0.6
$vcmo$	Output Common Mode Voltage	1.2

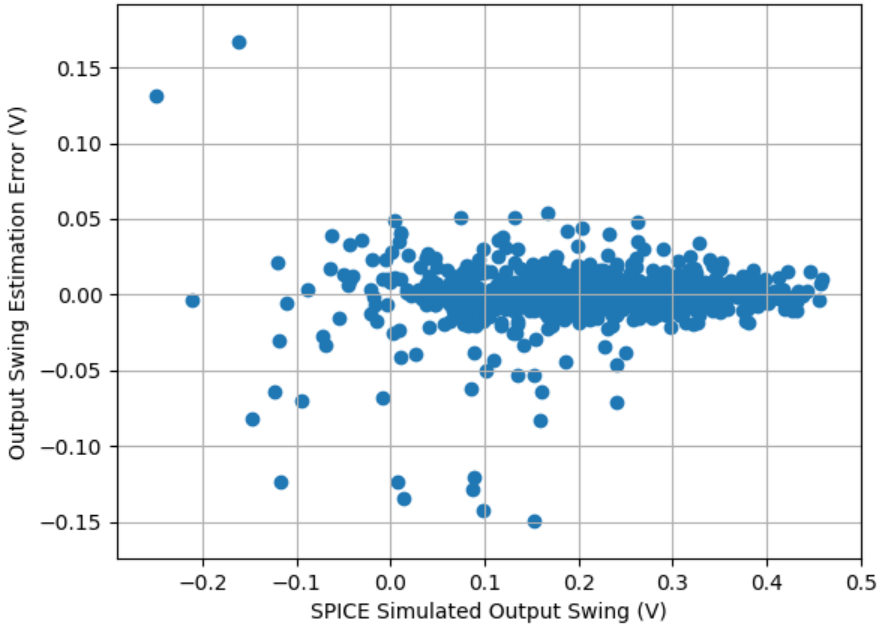
The estimation error over the metrics:

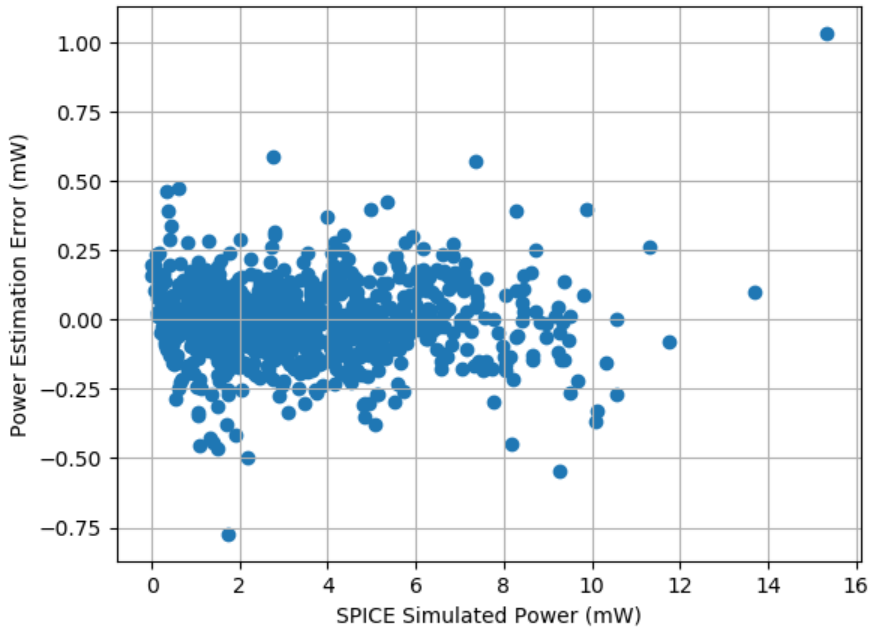

AVCM Estimation Error (dB)
30
20
10
0
−10
−60
−50
−40
−30
−20
−10
0
10
20
SPICE Simulated AVCM (dB)

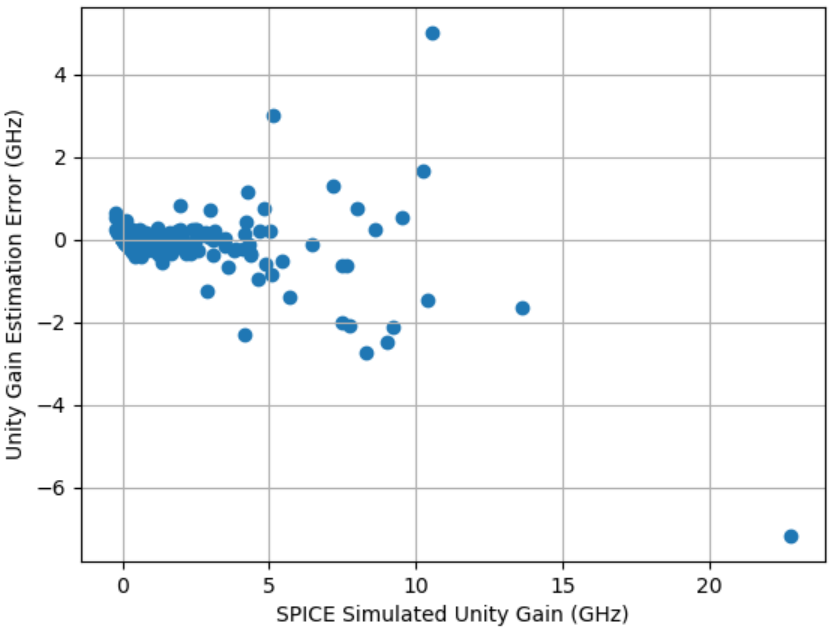

AVD Estimation Error (dB)
2
0
−2
−4
−6
0
5
10
15
20
25
30
SPICE Simulated AVD (dB)


30
20
10
0
−10
−20
0
50
100
150
200
Cin Estimation Error (fF)
SPICE Simulated Cin (fF)


Output noise Estimation Error (mV^2/Hz)
0.2
0.0
−0.2
−0.4
−0.6
0.0
0.2
0.4
0.6
0.8
1.0
1.2
SPICE Simulated Output noise (mV^2/Hz)


Output Swing Estimation Error (V)
0.15
0.10
0.05
0.00
−0.05
−0.10
−0.15
−0.2
−0.1
0.0
0.1
0.2
0.3
0.4
0.5
SPICE Simulated Output Swing (V)


Power Estimation Error (mW)
SPICE Simulated Power (mW)
1.00
0.75
0.50
0.25
0.00
−0.25
−0.50
−0.75
0
2
4
6
8
10
12
14
16


Unity Gain Estimation Error (GHz)
SPICE Simulated Unity Gain (GHz)
4
2
0
−2
−4
−6
0
5
10
15
20