

Module: Telescopic Cascode Operational Amplifier

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Module Description: Telescopic Cascode Operational Amplifier utilizes the cascode topology on the pull down and pull up at the same time to achieve high gain and high speed, while sacrifices the swing and input common mode range.

Top Cell Name: VCO_Dtype1_65

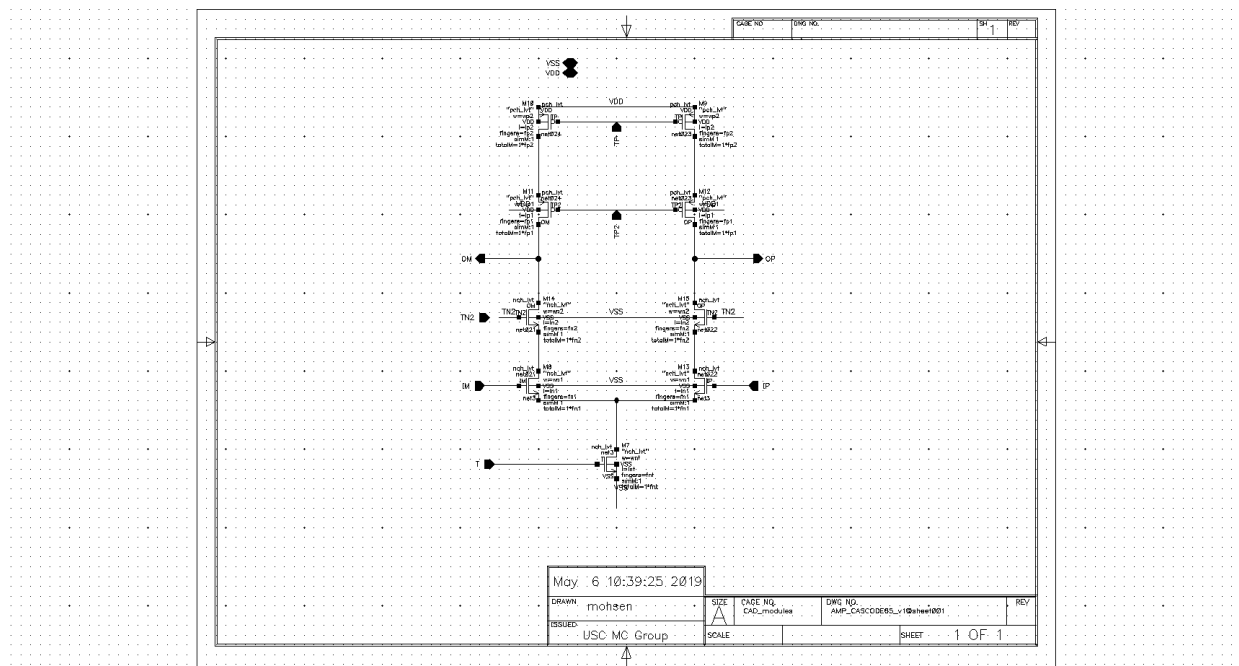
Technology: TSMC 65nm CMOS

PINS:

Pin Lists	
VDD	Supply Voltage
VSS	Ground
TP, TP2, TN2, T	Bias voltages
IM, IP	Input Differential Voltage
OM, OP	Output Differential Voltage

Schematic Netlists: ATC_v1.scs

Schematic figures:



Testbenches: ATC_test.scs

Parameters:

Parameters	Symbols
Top PMOS # of Fingers	$fp2$
Top PMOS Length (m)	$lp2$
Mid PMOS # of Fingers	$fp1$
Mid PMOS Length (m)	$lp1$
Mid NMOS # of Fingers	$fn2$
Mid NMOS Length (m)	$ln2$
Bot NMOS # of Fingers	$fn1$
Bot NMOS Length (m)	$ln1$
Sink NMOS # of Fingers	fnt
Sink NMOS Length (m)	lnt
Sink NMOS Bias (V)	$vttt$
Common Mode Voltage (V)	vcm_{in}
Mid NMOS Bias (V)	$vtn2$
Mid PMOS Bias (V)	$vtp2$
Output Capacitive Load (F)	cl

Metrics:

Metrics	Symbols
DC Power Consumption (W)	power
Output Swing Voltage (V)	swing
Common mode voltage gain (dB)	avcm
Differential gain (dB)	avd
Input Capacitance (F)	cin
Unity Gain Bandwidth (Hz)	gbw
Output Noise (V ² /Hz)	outnoise

Neural Network Model:

The H5 file: reg_ATC65.h5

The Json File: model_ATC65.json

The Input Normalization File: scX_ATC65.pkl

The Output Standardization File: scY_ATC65.pkl

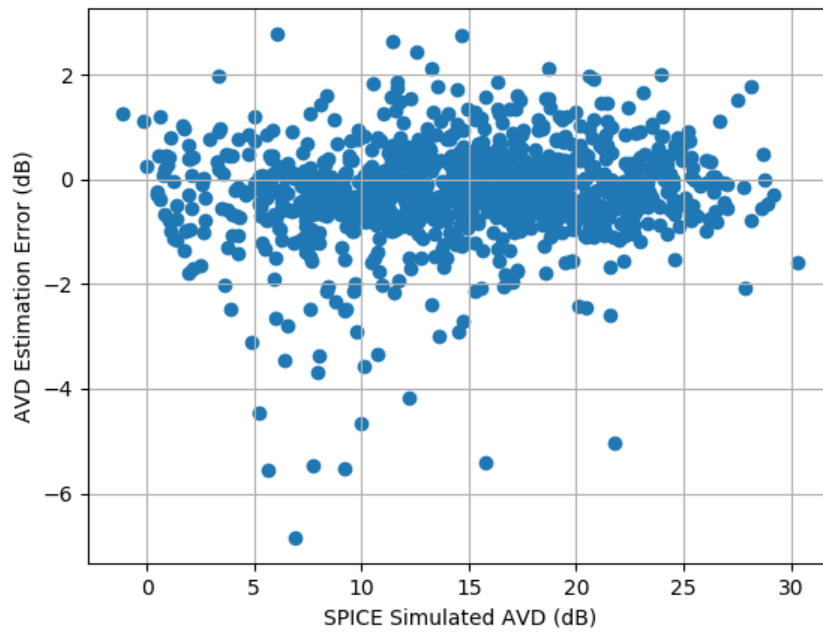
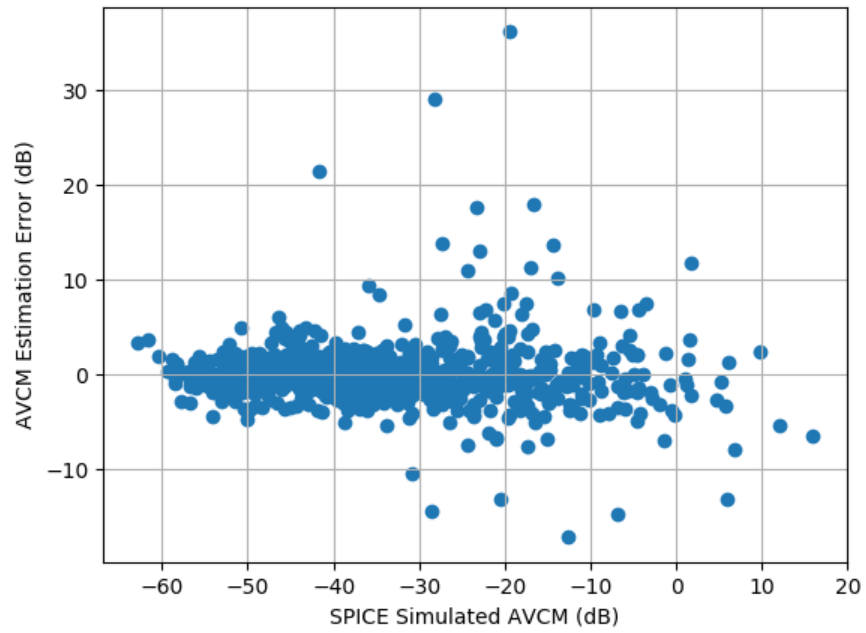
The input characterization range of the Model:

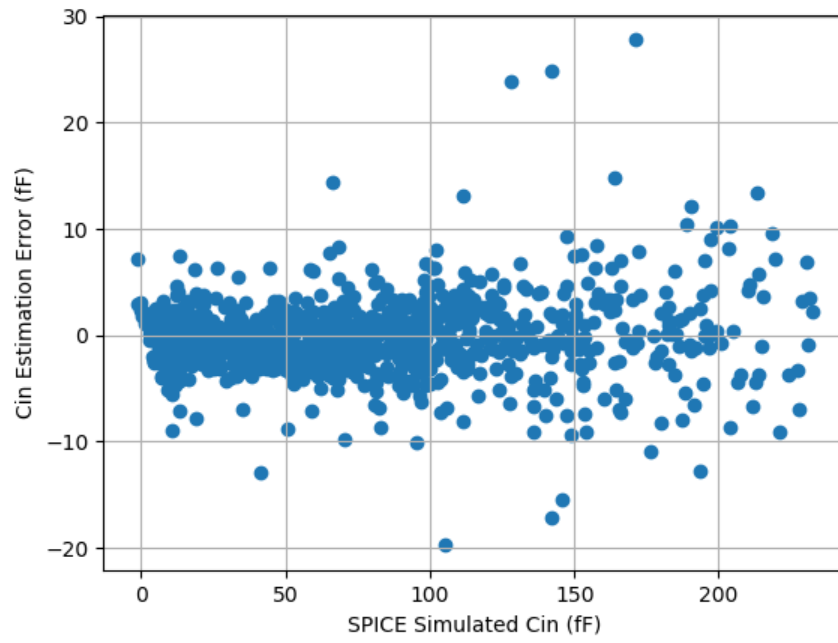
Design parameters	
Symbols	Characterization Range
<i>fp2</i>	4,5, ..., 200
<i>lp2</i>	[60nm, 200nm]
<i>fp1</i>	2,5, ..., 100
<i>lp1</i>	[60nm, 200nm]
<i>fn2</i>	2,5, ..., 100
<i>ln2</i>	[60nm, 200nm]
<i>fn1</i>	2,5, ..., 100
<i>ln1</i>	[60nm, 200nm]
<i>fnt</i>	4,5, ..., 200
<i>lnt</i>	[120nm, 400nm]
<i>vttt</i>	[0.35V, 0.6V]
<i>vcmin</i>	[0.6V, 0.8V]
<i>vtn2</i>	[0.7V, 0.95V]
<i>vtp2</i>	[0.05V, 0.3V]
<i>cl</i>	[1fF, 10pF]

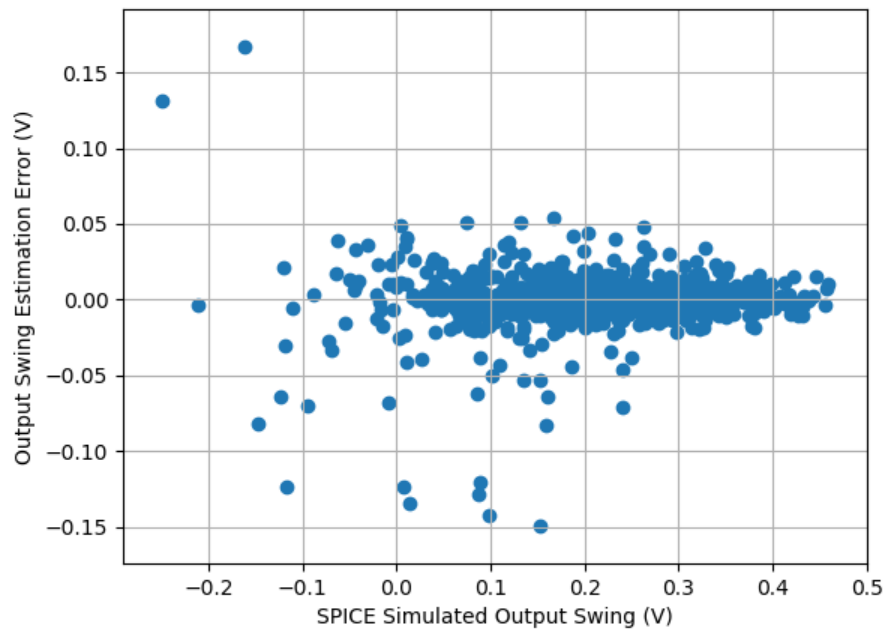
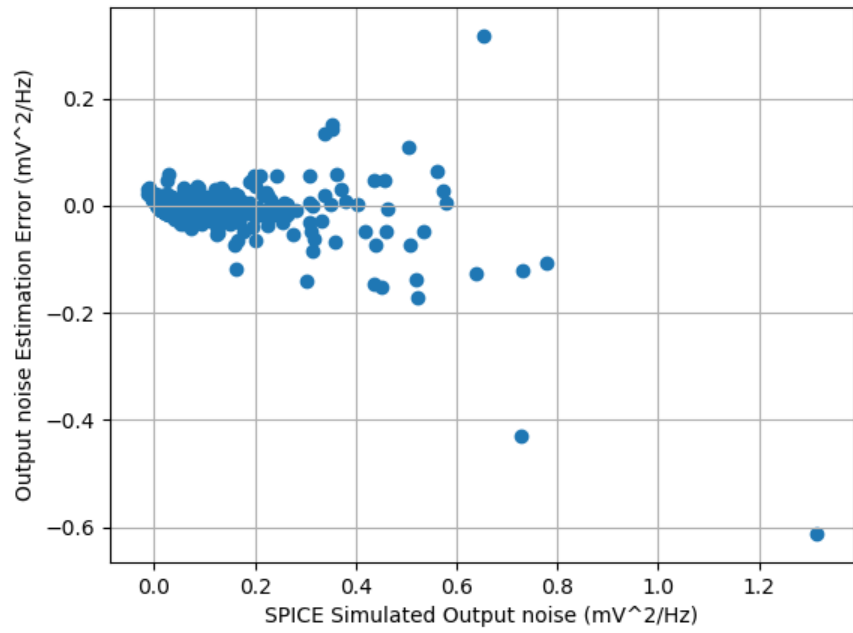
Another parameter ranges:

Design parameters		
Symbols	Description	Characterization Range
<i>VDD</i>	Supply Voltage	1V
<i>wp2</i>	Top PMOS Width	800nm
<i>wp1</i>	Mid PMOS Width	800nm
<i>wn1</i>	Mid NMOS Width	800nm
<i>wn2</i>	Bot NMOS Width	800nm
<i>wnt</i>	Sink NMOS Width	800nm
<i>rl</i>	Output loading resistance	1 GΩ
<i>vcmn</i>	Loading DC voltage	0.6
<i>vcmo</i>	Output Common Mode Voltage	1.2

The estimation error over the metrics:







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