Module: Pseudo-differential VCO type1 (used in VCO-based ADC)

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Module Description: Pseudo-differential VCO utilizes five resistor based cross-coupled inverters and ring-oscillator based topology. The architecture has 10 different nodes positive and negative side and one input.

Top Cell Name: VCO_Dtype1_65

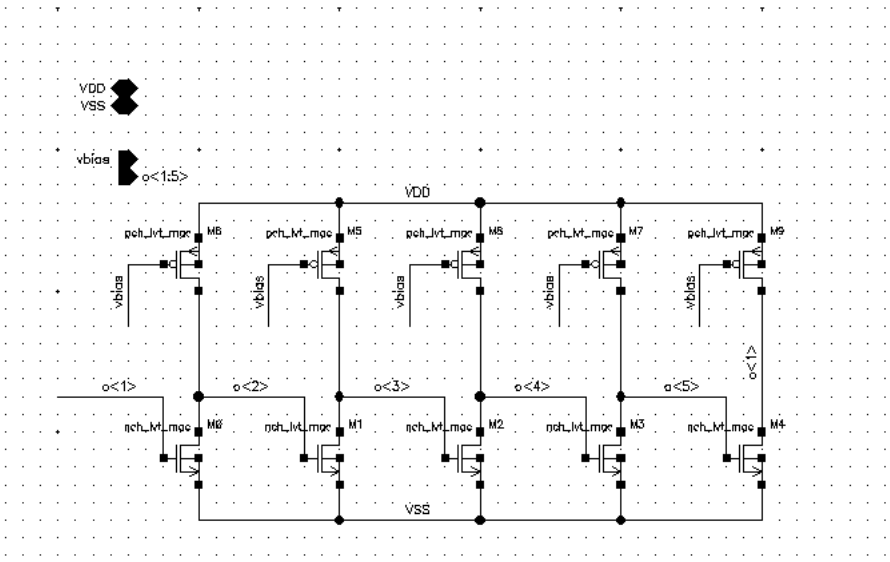
Technology: TSMC 65nm CMOS

PINS:

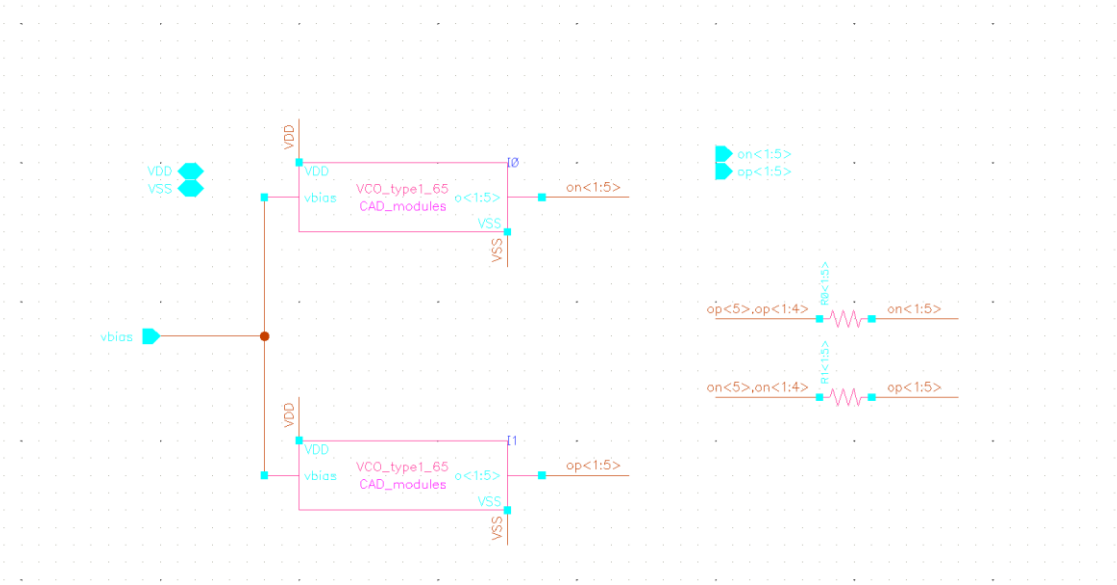
Pin Lists	
VDD	Supply Voltage
VSS	ground
Vbias	Input voltage node
on<1:5>	Five output from the negative side VCO
op<1:5>	Five output from the positive side VCO

Schematic Netlists: VCO5_type1.scs

Schematic figures:



Module: Pseudo-differential VCO (type1)



Testbenches: VCO5_type1_test.scs

Parameters:

Parameters	Symbols
NMOS transistors width (m)	$wnnn$
NMOS transistors # of fingers	$fnnn$
PMOS transistors width (m)	$wppp$
PMOS transistors # of fingers	$fppp$
Resistors (ohm)	$rres$

Metrics:

Metrics	Symbols
Maximum input range at pin vbias (V)	Input
Power Consumption (mW)	Power
Minimum VCO frequency (Hz)	Fmin
Maximum VCO frequency (Hz)	Fmax

Neural Network Model:

The H5 file: reg_vco65.h5

The Json File: model_vco65.json

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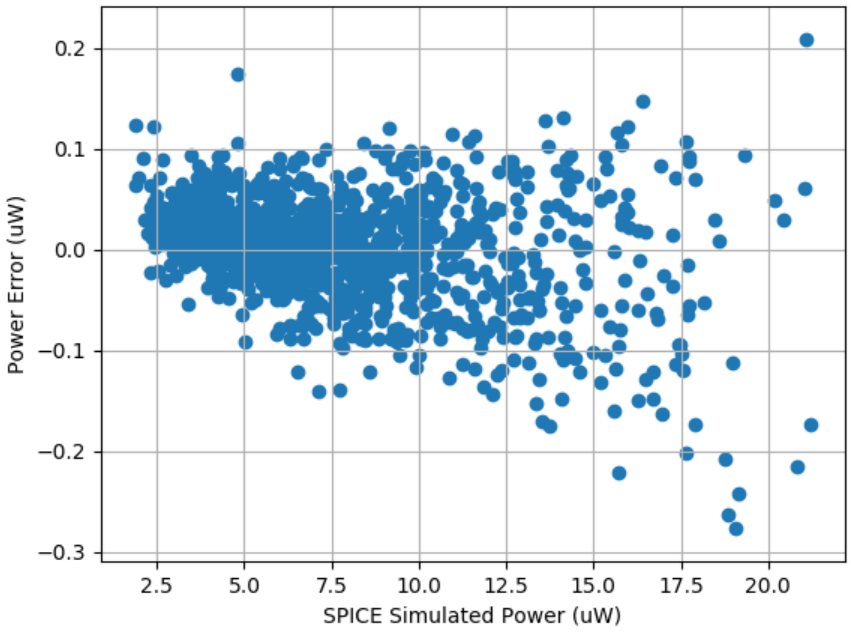
The Input Normalization File: scX_vco65.pkl

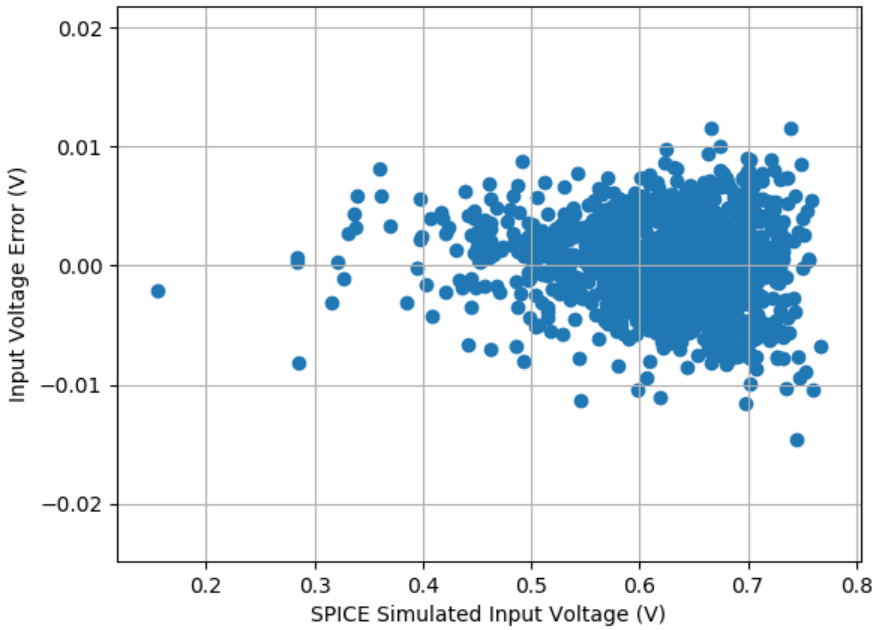
The Output Standardization File: scY_vco65.pkl

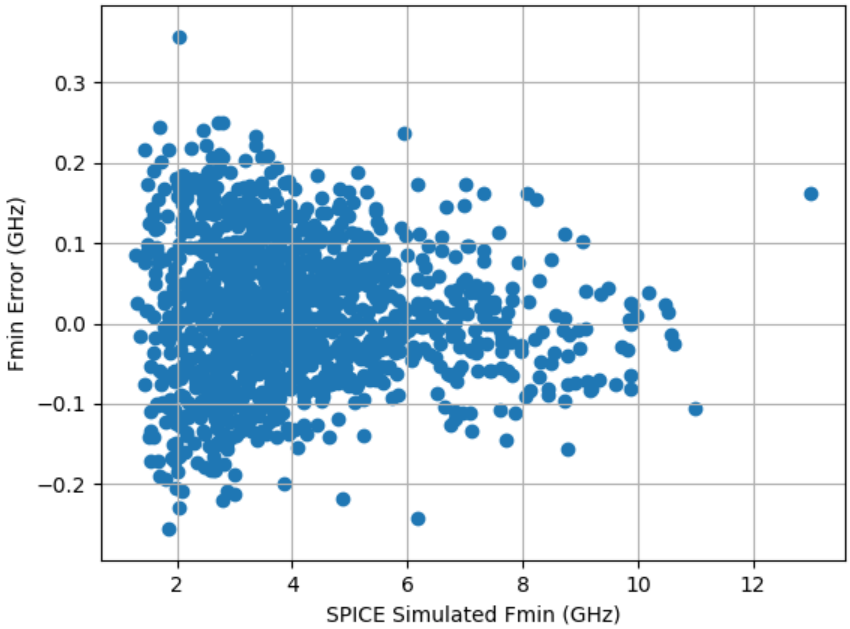
The input characterization range of the Model:

Design parameters	
Symbols	Characterization Range
$\boldsymbol{wnnn}$	$[0.2\mu m, 1.2\mu m]$
$\boldsymbol{fnnn}$	$2,3,4,\dots,14$
$\boldsymbol{wppp}$	$[0.2\mu m, 1.2\mu m]$
$\boldsymbol{fppp}$	$2,3,4,\dots,14$
$\boldsymbol{rres}$	$[500\ \Omega, 2000\ \Omega]$
VDD	1 V

The estimation error over the metrics:




0.02
0.01
0.00
−0.01
−0.02
Input Voltage Error (V)
0.2
0.3
0.4
0.5
0.6
0.7
0.8
SPICE Simulated Input Voltage (V)


0.3
0.2
0.1
0.0
−0.1
−0.2
Fmin Error (GHz)
2
4
6
8
10
12
SPICE Simulated Fmin (GHz)

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