

Date: May 4, 2019

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AMPSE: VCO Based ADC in TSMC 65nm CMOS

I. Introduction

In this design a 1GS/s, 6-bit, VCO-based ADC has been implemented. DLL is a commonly used design block for generating multi-phase clocks. The block diagram representation of the design is as follows:

ADC Architecture:

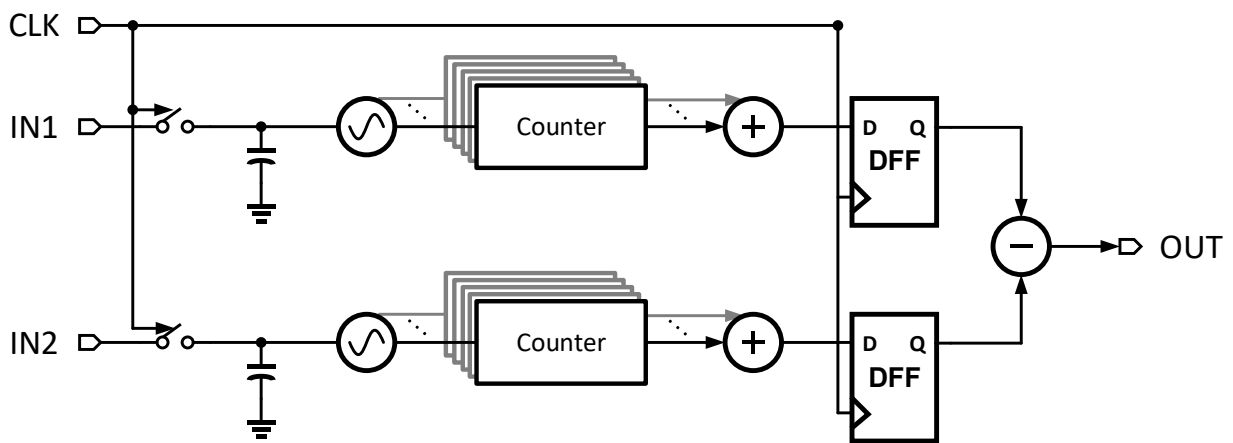
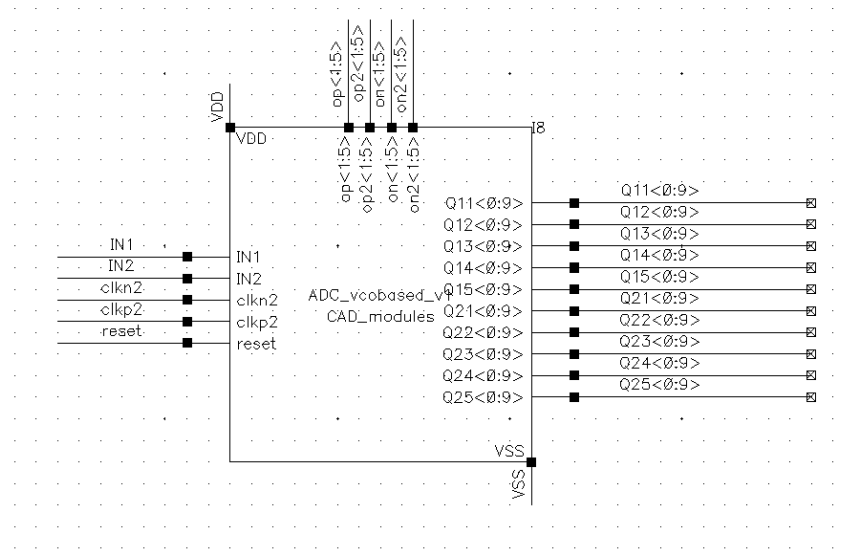


Figure 1: Architecture of VCO-based ADC with AMPSE

The main analog modules in this design are:

- VCO
- Track and Hold
- Buffers

Description:



The Top-level cell: ADC_vcobased_v1.scs

Pin Configuration:

Pin Name	Specification	Pin Type
VDD	Power Supply, 1.0 V	Supply
VSS	Ground	Ground
clkn, clkp	Input Clock	Input
IN1, IN2	Differential Analog Input	Input
reset	Reset	Input
o<0:9>	Output digital codes	Output

Description of the Cell Library:

The tabular description below corresponds to design hierarchy.

#	Category	CellName	Description	Figure
1		ADC_vcobased_v1	Top level	VCO_ADC_1.png
2	ADC_vcobased_v1	VCO_Dtype1_65	Pseudo differential VCO	VCO_ADC_2.png
3		TH65_TG_v1	Track and Hold	VCO_ADC_4.png
4		counter_vco_v2	10-bit Counter	VCO_ADC_7.png
5		INV65_v3	Track and Hold's driver	VCO_ADC_5.png
6		diff2sing_v1	Differential to single ended output.	VCO_ADC_6.png
7	VCO_Dtype1_65	VCO_type1_65	VCO	VCO_ADC_3.png
8	counter_vco_v2	counter_onehot2bit	2-bit counter for up to 20GHz clock frequency	VCO_ADC_8.png
9		counter_bin4bit	4-bit counter for up to 10GHz clock frequency	VCO_ADC_10.png
10	counter_onehot2bit	TSPC4LVT	TSPC D-flipflop	VCO_ADC_9.png
11	Testbench	test_VCO65_v1	Testbench for VCO based ADC	VCO_ADC_11.png

Test Bench:**Locking time evaluation:**

1. test_VCO65_v1(cell_name): Testbench for VCO-based ADC operation

Simulation Results:

Design Corners: Process Corners, -55C to 125C, Vdd nominal +/- 10%

Typical Current consumption specifications from 1V supply at room temperature: (TBD)