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ECE 529

Final Project: Carry Ripple Adder Implementation
using Data Driven Dynamic Logic

05/10/2013

Abstraction

This paper provides some implementation examples of a 4-bit carry ripple adder (CRA) depending on Data-Driven Dynamic logic based structures. In this design, the 4-bit CRA is designed depend on two different logic expressions and based on two techniques: D3L and SPD3L respectively. Then, by comparing the performance of these four designs, a best design can be choose from them. Moreover, a discussion about the differences between these two techniques will be provided.

Keywords: D3L, SPD3L, 4-bit CRA

1 Introduction

As the fast development of integrated circuit technology, we concentrate our researches increasingly on increasing speed and reducing power dissipation when implementing specific logic functions. One well-known method is Domino dynamic logic, which makes a circuit much faster than conventional logic. However, it comes with large dynamic power consumption. In this paper, I am going to use two new techniques: D3L [1] and SPD3L [2]. The basic thought of D3L is using a combination of inputs as the dynamic signal which will not affect the logic accuracy of the whole circuit and make the design work as it is in dynamic logic. However, it makes the capacitance for charge much larger and reduces the speed of a circuit. As a result, we involve SPD3L, in which D3L are separated into difference part to reduce the charging capacitance. The description in detail will be provided in next part.

2 Background

Before we start the project, the principle of different logic technique will be provided in this part to make the thought of our design clear. In addition, the principle of a 4_bit adder will also be introduced.

2.1 Logic method

2.1.1 D3L

As described in [1], any function that can be expressed as:

$$F = (I_{1,1} \dots I_{k,1}) + \dots + (I_{1,m} \dots I_{n,m})$$

can be implemented with D3L logic by picking any one of the inputs in every AND part. We can use these signals as a clock signal in conventional dynamic logic. The structure figure is in Figure 1.

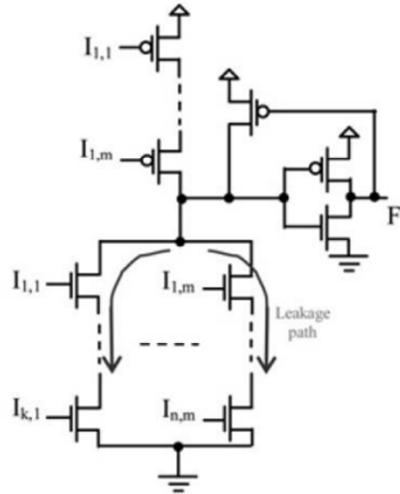


Figure 1

In this method, we see that without a pre-charging dynamic node, the dynamic power will be decreased to a large extent. Moreover, even in the recharge phase, in logic correctness can still be guaranteed for most cases.

2.1.2 SPD3L

It can be seen in figure 1 that in PUN, all PMOS transistors are in series, which will lead to a very large pre-charging capacitance. That's the reason we use SPD3L [2]. As we can see from figure 2, this circuit is generated by splitting the PDN to AND parts with their selecting signal in PUN. Since there is only one PMOS in PUN, the capacitance could be very small, which leads to faster speed and less power dissipation.

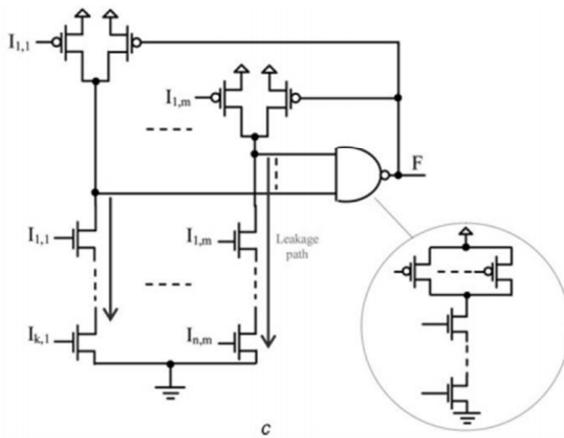


Figure 2

In the end, a normal NAND gate is attached to generate the output of the circuit to keep the logic correctness of this design. Moreover, more keeper transistors have to be used in this structure, but these transistors must be very small to make the logic correct. In terms of sizing, more details will be provided in adder design description section.

2.2 4-bit CRA

In this paper, we just implement the simplest 4_bit carry propagation adder or carry ripple adder.

The structure of a carry ripple adder is shown below: (Figure 3)

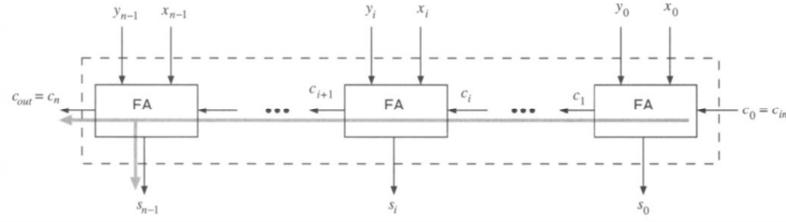


Figure 3

It shows that the sum result of this adder is generated bit by bit due to the delay of carries. When implementing, some details are different from the structure above, but the basic principle is the same.

3 Architectural Exploration of Adders

As what has been discussed above, the main purpose of the project is finishing the 4 bit carry ripple adder using two different logic methods. In this design, two logic expressions are provided for implementation:

1. $S = A \oplus B \oplus C_i$ and $C_{out} = (AB + BC_i + AC_i)$
2. $P = (A \oplus B); G = AB; S = P \oplus C_i; C_{out} = G + PC_i$

I will design the schematic of these two logic expressions with two methods that are described above. As a result, there are four designs in total. The design details are provided in this part. Then I verify their correctness in section 4 and compare the performance of them in section 5. Here is how I design this implementation.

3.1 Basic elements

Firstly, some basic logic gates will be used in this design, as it is shown below:

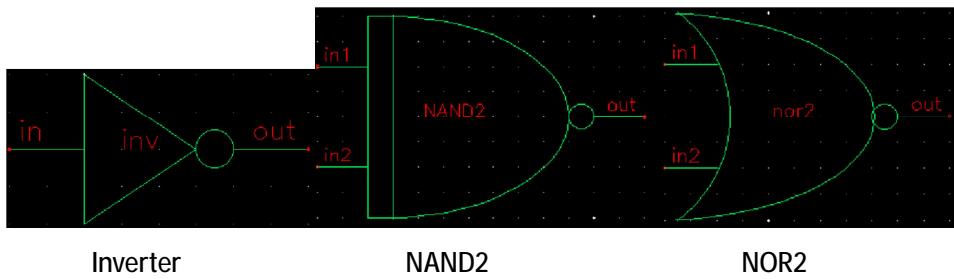


Figure 4

They are all designed and transistors sized based on conventional logic method. Inverters are used for any invert function, especially for D3L logic. NAND2 is used in SPD3L logic. In this design, there is no more than two ways for SPD3L, so NAND with two inputs is enough. NOR2 is used for gate control function. The reason for this is that in some cases, the pre-charge signals are inverted with each other, which means they cannot be zero at the same time that makes the circuit impossible to be pre-charged. The purpose of the gate controlling is to add a pre-charge signal that will force both inputs to zero in pre-charge phase. To achieve this, I use the circuit below and save it as a module named Pr_ctrl:

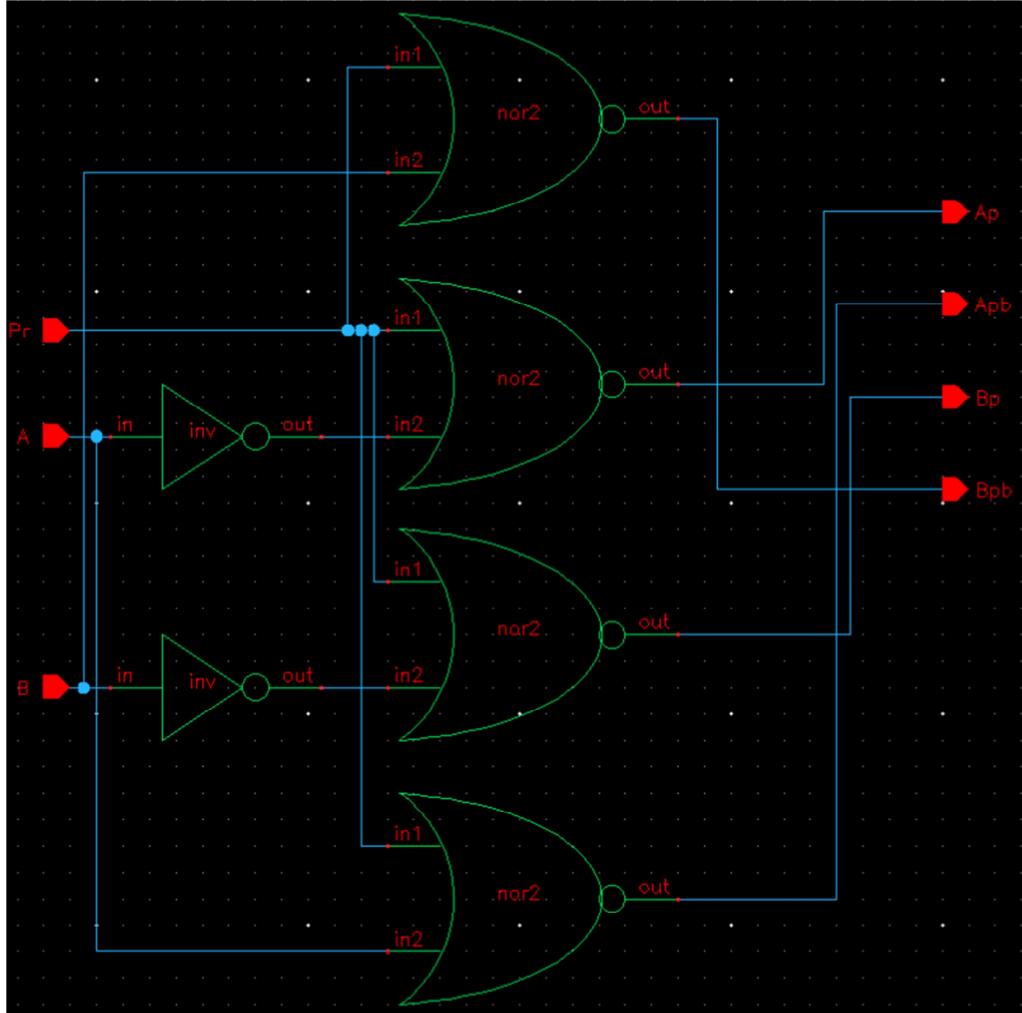


Figure 5

The logic in this circuit can be described as:

$$\begin{aligned} Ap &= \overline{Pr + \bar{A}} \\ Apb &= \overline{Pr + A} \\ Bp &= \overline{Pr + \bar{B}} \\ Bpb &= \overline{Pr + B} \end{aligned}$$

Because I just use A and B as pre-charge signal, this structure will be used just for A and B to generate pre-charge signals. They are all controlled by Pr . More specifically, when $Pr=1$, all the signals will be set to 0, when $Pr=0$, $Ap=A$, $Apb=\bar{A}$, $Bp=B$, $Bpb=\bar{B}$.

3.2 Sizing

In terms of sizing, especially for D3L and SPD3L logic schematic, the principle is simple that it is almost the same with the transistor sizing issue in conventional logic method. The only difference is that we size the keeper transistors to its smallest size. The size of every transistor can be seen in every schematic figure. However, I will no longer talk about sizing issue below because there are too many circuits.

3.3 Adder Implementation

3.3.1 Logic 1 with D3L

The key part of a 4-bit CRA is a Full Adder (FA), so when talk about this design; we concentrate most on Full Adder design.

For logic 1, the module connection in FA can described as below:

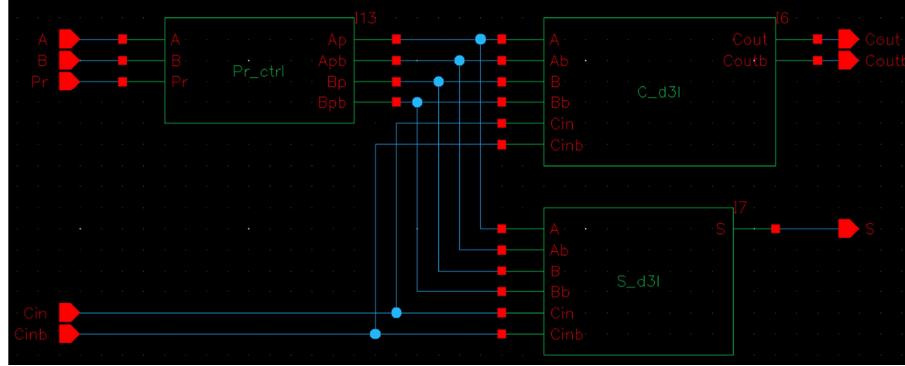


Figure 6

Notice that no inverted S needed so we just output S. C and inverted C are both needed because they are essential for the input of next stage in a cascade structure.

In this structure, C_d3l is shown below:

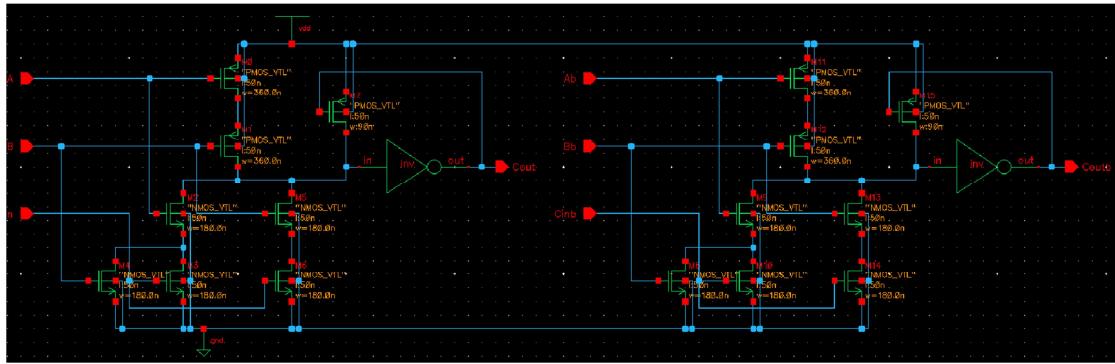


Figure 7

It has the logic $Cout = AB + ACin + BCin$ and $Coutb = \bar{A}\bar{B} + \bar{A}Cin + \bar{B}Cin$. A clear screenshot is included in the attached file. In this figure, the structure can be seen clearly that A B Ab Bb are selected as the pre-charge signal and Cout and Coutb are generated separately.

S_d3l is:

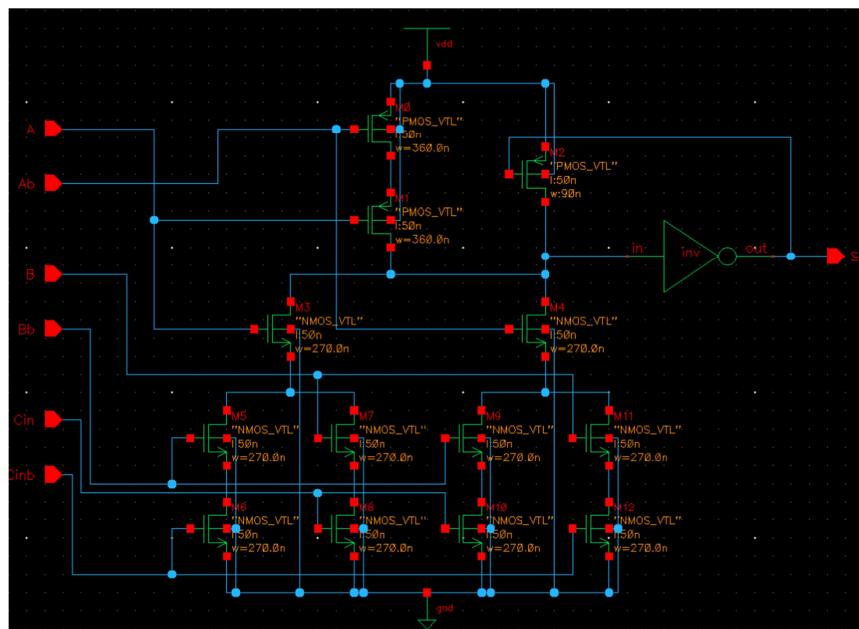


Figure 8

Use A and inverted A to pre-charge and only S is output

3.3.2 Logic 1 with SPD3L

The connection of a SPD3L full adder is the same with D3L. Just change S_d3l to S_sp, C_d3l to C_sp. The C_sp is:

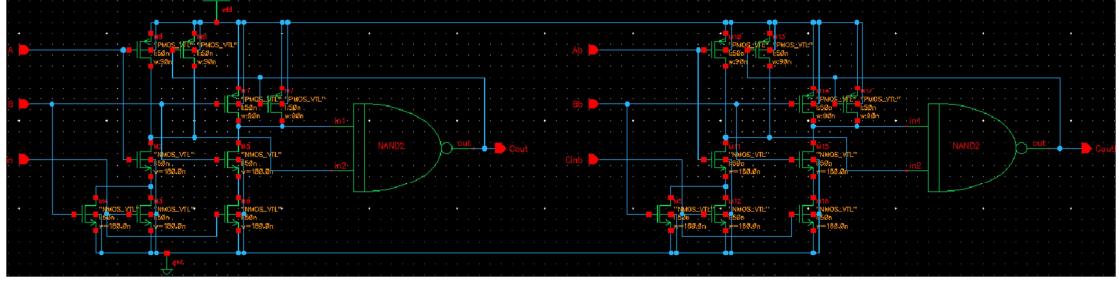


Figure 9

Comparing to C_d3l, the PDNs are the same. The differences focus on PUN. Every pre-charge signal connects to the part it controls exclusively, which is the same as what has been described in the principle. In this case, one more keeper is added for each part and a NAND2 is used for each part to generate output.

With the same principle, S_sp can be:

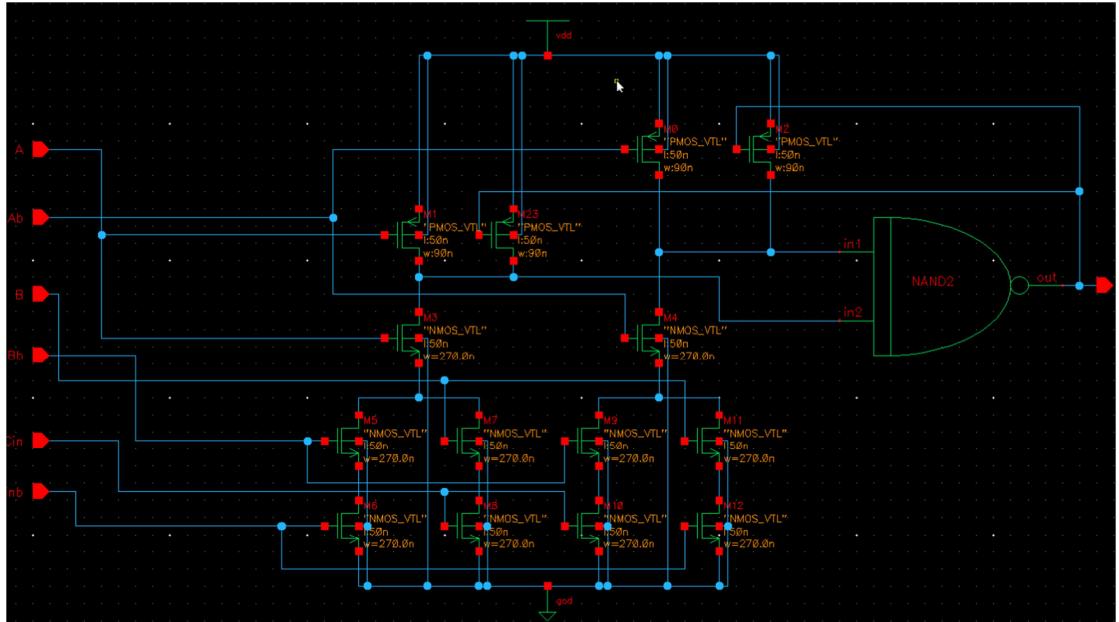


Figure 10

3.3.3 Logic 2 with D3L

According to the logic function, the module connection for a FA in D3L could be:

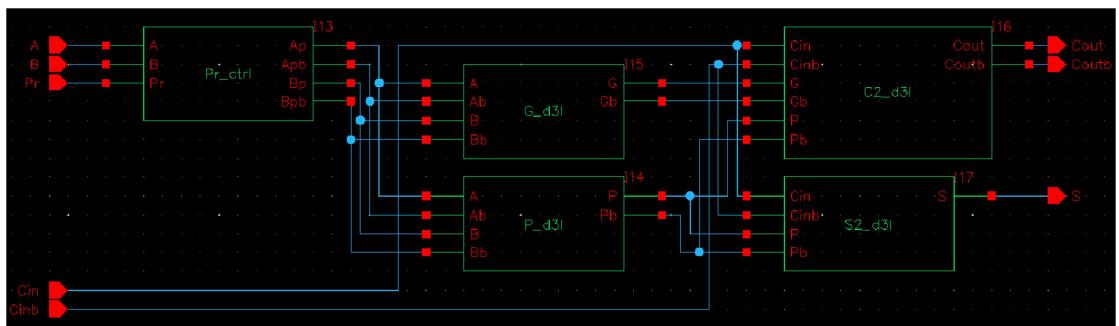


Figure 11

Notice that P and Pb, G and Gb should all be generated. This is not only because they are all used in next stage circuit, but also because they are pre-charge signals that should be able to be set to 0 in pre-charge phase. The solution to generate P and Pb, G and Gb separately. The actual schematic will be provided below.

G_d3l:

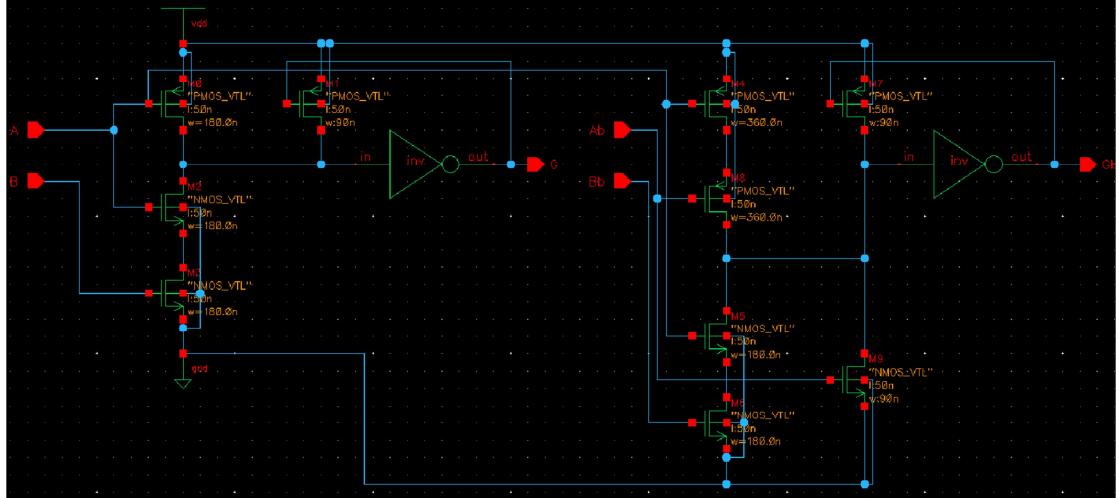


Figure 12

The logic expression is:

$$G = AB, \quad Gb = A * b + A * Bb$$

The structure to generate G and Gb cannot be the same, so the final structure is shown above. Actually $Gb = \bar{A} + \bar{B}$ is the simplest expression, but I just use A and Ab as pre-charge signal in this part.

The P_D3l is:

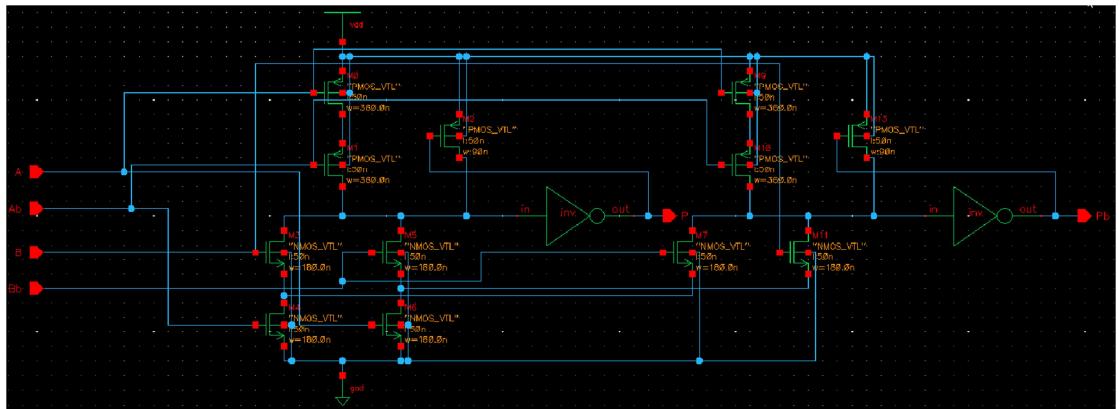


Figure 13

The logic expression is:

$$P = A \oplus B, \quad Pb = \overline{A \oplus B}$$

This is a normal D3L XOR gate with dual outputs. Again it is generated from the principle above by generating signals based on their logic expression respectively.

C2_d3l:

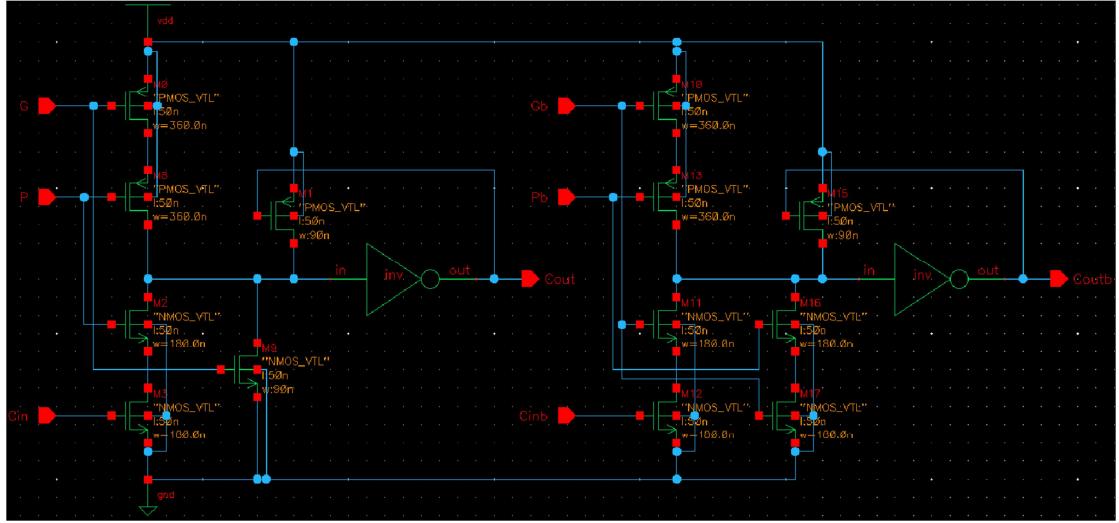


Figure 14

The logic expression is:

$$\text{Cout} = \text{G} + \text{PCin}, \quad \text{Coutb} = \text{Gb} * \text{Cinb} + \text{Pb} * \text{Gb}$$

It is build depending on the same principle, $\text{Gb} * \text{Cinb} + \text{Pb} * \text{Gb}$ is get from the inverted function of Cout.

Finally the S2_d3l is:

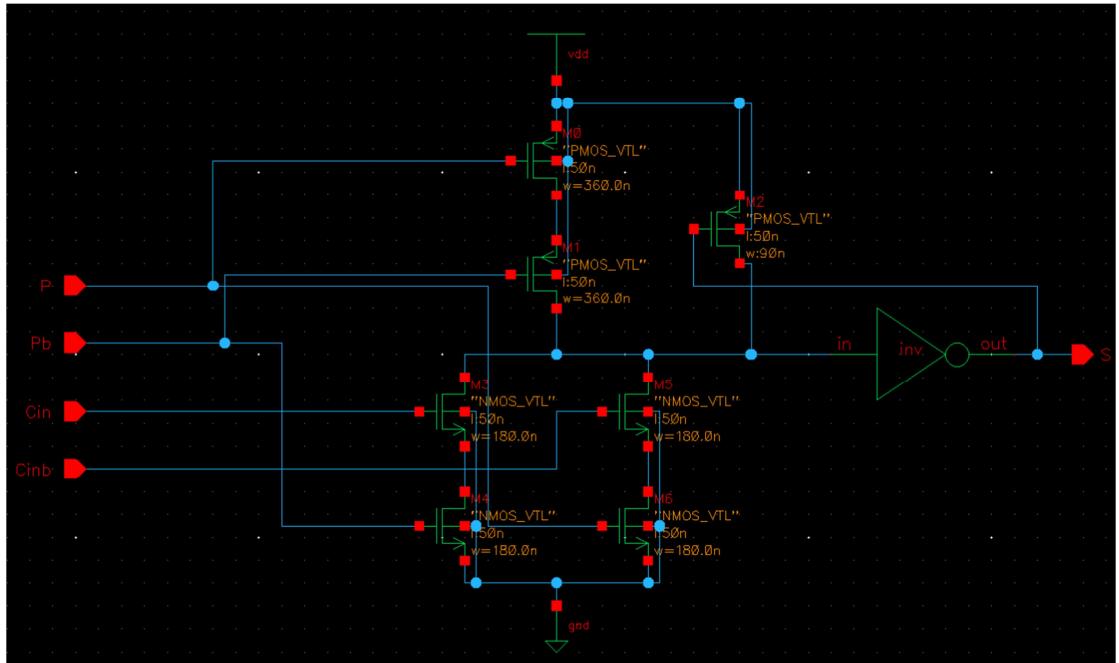


Figure 15

The Function is $S = P \oplus \text{Cin}$ with single output.

3.3.3 Logic 2 with SPD3L

With the same procedure to generate SPD3L logic that I used above, I can get all the schematics of SPD3L for Logic 2 easily. The module connection is the same, and the schematics are shown below:

G_sp:

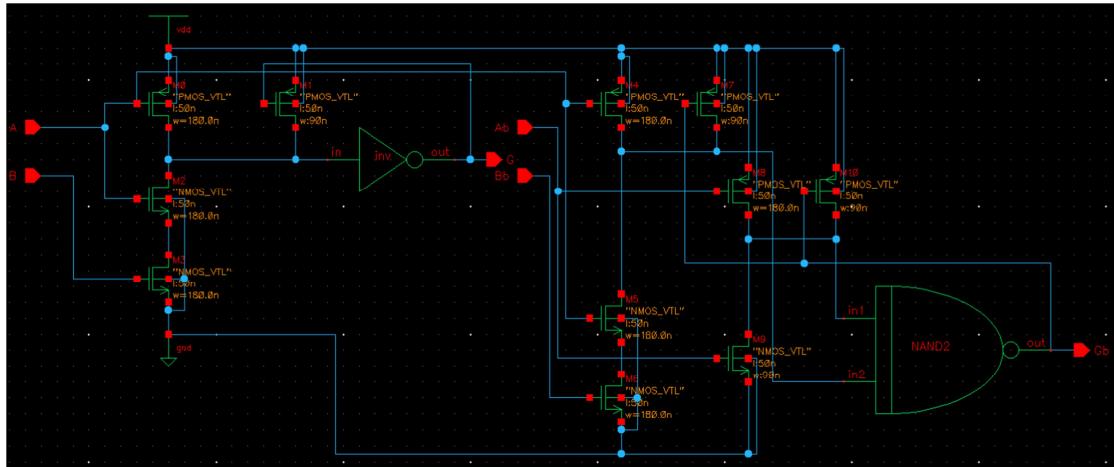


Figure 16

P_sp:

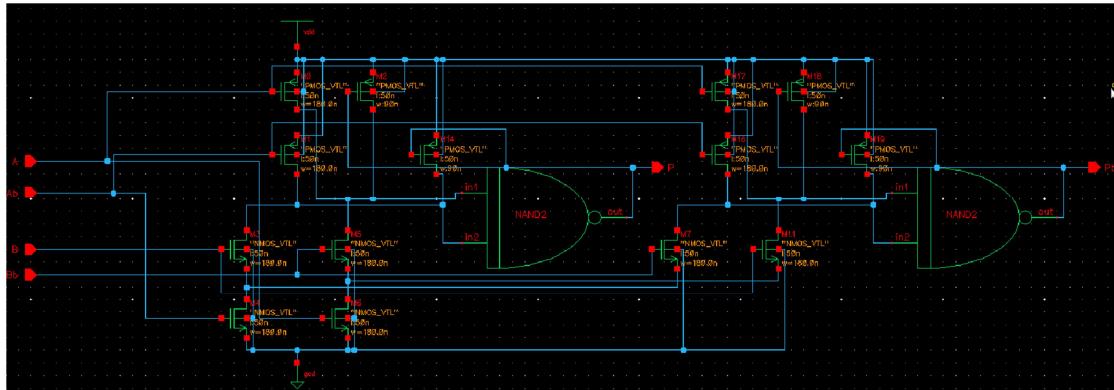


Figure 17

C2_sp:

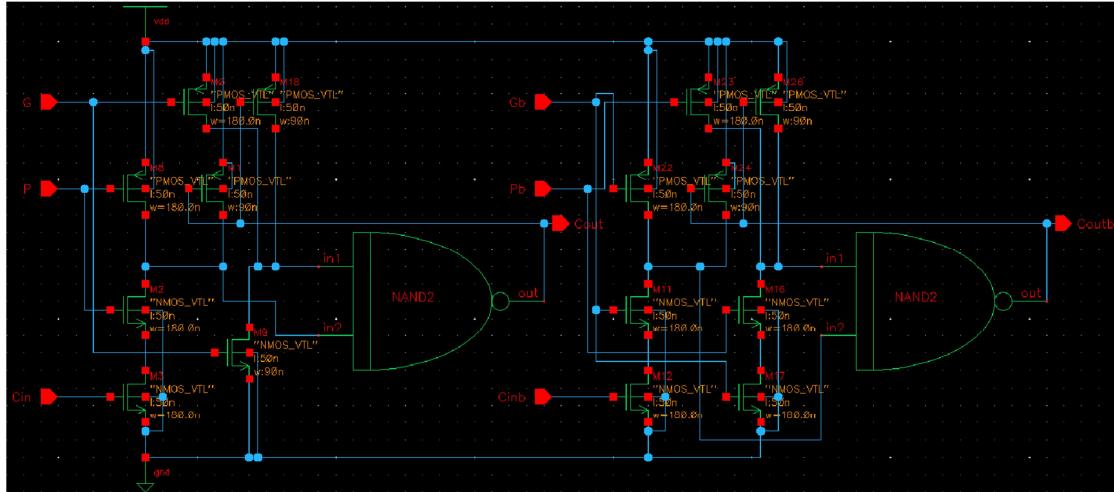


Figure 18

S2_sp:

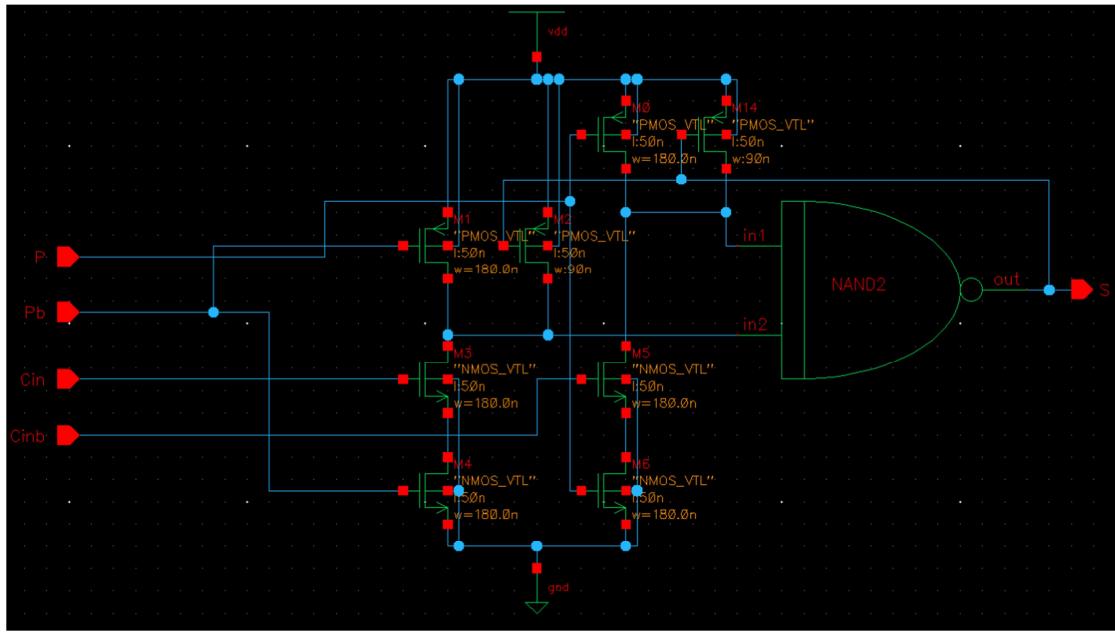


Figure 19

4 Functional Validation and Verification

4.1 FA Verification

Hspice is used to verify the function of all the schematics in this design. By ADE process, we can get the netlist of them. These are .sp file. By modify these files, we can set up different input to see the correctness of the output. All the .sp files that are used in this design are provided in the attached files.

In order to test a FA, I assert the input signals as below for all the Fas in different logic and method:

```
v0 vdd! 0 DC=1.1
v8 pr 0 PULSE 0 1.1 0 50e-12 50e-12 450e-12 1e-9
v7 cinb 0 PULSE 1.1 0 0 50e-12 50e-12 3.95e-9 8e-9
v6 cin 0 PULSE 0 1.1 0 50e-12 50e-12 3.95e-9 8e-9
v5 b 0 PULSE 0 1.1 0 50e-12 50e-12 1.95e-9 4e-9
v1 a 0 PULSE 0 1.1 0 50e-12 50e-12 950e-12 2e-9
c2 cout 0 1e-15
c1 coutb 0 1e-15
c0 s 0 1e-15
```

Thought this is not very clear about the input, after running it through FA1_d3l, which is a D3L full adder with logic 1, we can see it very clearly in the waveform below:

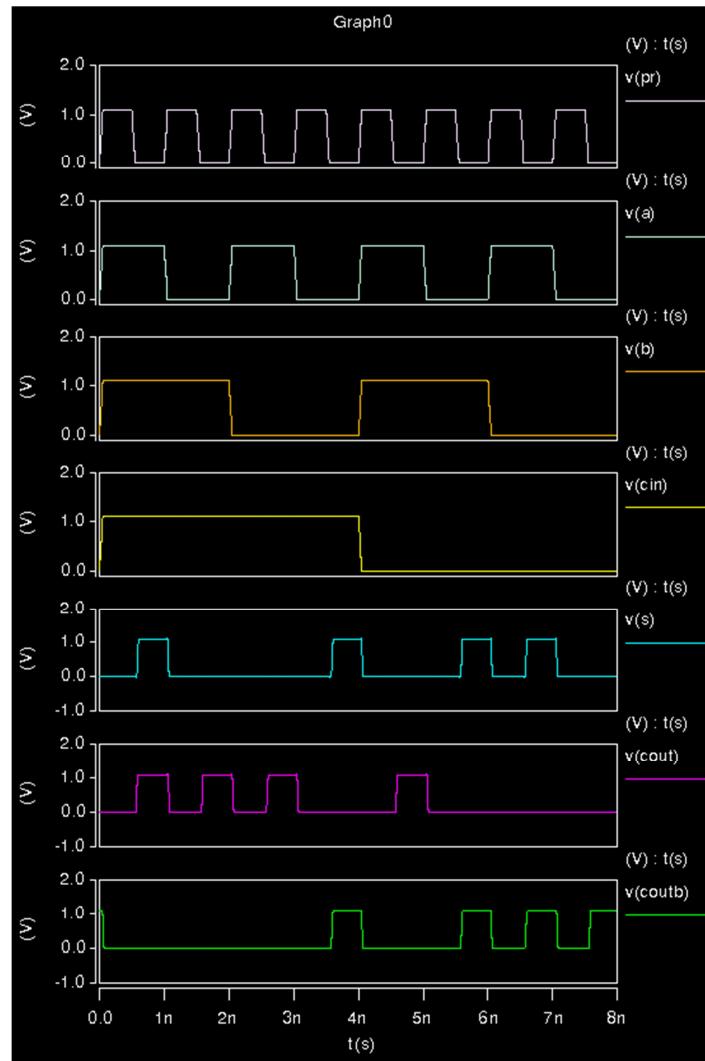


Figure 20

A, B and Cin are set to different frequency to generate all the possible combinations of the input. The period of Pr is 1ns, A is 2ns, B is 4ns, Cin is 8ns, which guarantees that there is a pre-charge phase and an evaluating phase in every nanosecond. It is clear the output is correct.

For other full adders the results are all proved to be correct. All result wave forms can be found in Appendix.

4.2 4-bit adders Verification

4-bit adder structure is shown below:

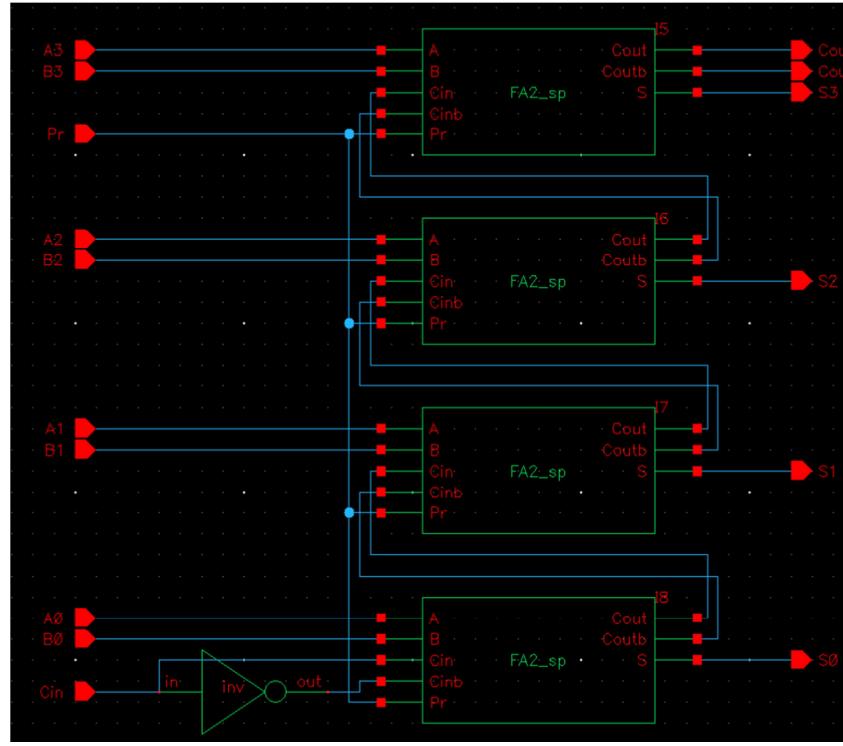


Figure 21

The key to verify the function of a 4-bit adder is to see the result depending on a specific input combination. In this design, I use the input below:

```
v10 cin 0 DC=1.1
v9 b3 0 DC=1.1
v8 b2 0 DC=1.1
v7 b1 0 DC=0
v6 b0 0 DC=1.1
v5 a3 0 DC=1.1
v4 a2 0 DC=1.1
v3 a1 0 DC=0
v2 a0 0 DC=0
v0 vdd! 0 DC=1.1
v1 pr 0 PULSE 0 1.1 0 50e-12 50e-12 450e-12 1e-9
c5 s3 0 1e-15
c4 cout 0 1e-15
c3 coutb 0 1e-15
c2 s0 0 1e-15
c1 s1 0 1e-15
c0 s2 0 1e-15
```

Which implies that A=1100, B=1101, Cin=1. The correct result should be S=1010, Cout=1.

By using the netlist file of adder41_d3l, which is the logic 1 4-bit adder in D3L logic, I get the wave form below:

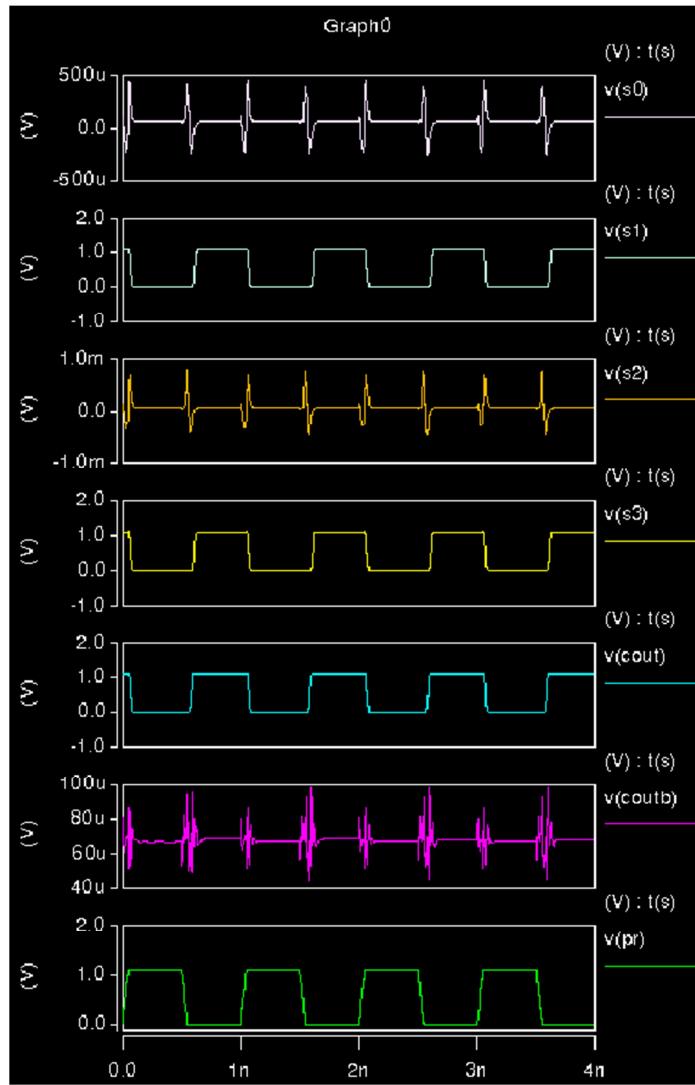


Figure 22

It implies that S=1010, Cout=1, which is the correct answer. All the result wave forms are provided as Appendix.

5 Result

In order to judge the performance for different design, we practically focus on power issue and delay. In terms of power, we can use Hspice to measure it directly by adding some measurement commands into the .sp file. Here I use:

.PRINT TRAN POWER

.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 4E-9

.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 4E-9

What is more, we have another method by using Nanosim. We can make a comparison between the results of these two methods.

To get a better result, I choose the test input in power issues to be A=1111, B=1111, Cin=1, which may lead to a worst power case.

Then, in terms of delay, it is essential to find the worst propagation chain that has the largest delay. In conventional method, we use Cin to Cout, but in this case, the delay chain may be cut off since Cout is just controlled by A and B in some cases. For example, when A=1 B=1, then the result node is certainly being charged which means Cout may no longer waiting for Cin. In this paper, I choose FALL (Pr) to RISE (S3) as a measurement using commands below since S3 can always have a long propagation chain.

```
.measure tpdr
+ TRIG v(pr) VAL='0.55' FALL=1
+ TARG v(s3) VAL='0.55' RISE=1
```

Actually in the test for the worst power case, I get the wave from below:

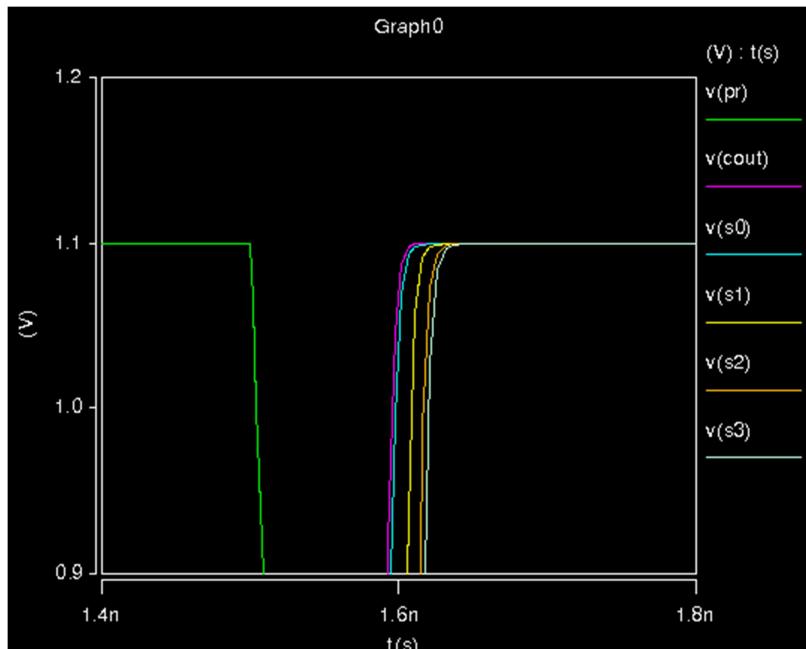


Figure 23

It means s3 is the lowest output in this case.

After measurements, the result can be concluded in Table 1:

		Hspice		Nanosim
		delay(ps)	Max Power (uW)	Avg Power (uW)
4-bit carry ripple adder	Logic 1 D3L	85.78	1047	88.88 89.84
	Logic 1 SPD3L	83.22	993.9	93.70 94.79
	Logic 2 D3L	117.9	1220	138.3 140.67
	Logic 2 SPD3L	104.6	1215	123.5 125.88

Table 1

Firstly, the power results in different methods are almost the same, which indicate this is a

correct result. Then, it is clear that in both logic1 and 2, SPD3L does increase the speed but not for sure in terms of power. Moreover, logic 1 is much better than logic 2 in terms of both timing and power. As a result, I choose SPD3L in logic 1 to be the best design for a 4-bit carry ripple adder since it is the fastest with not very large power consumption.

All the full reports are attached as Appendix.

6 Conclusion and future work

In this project, I finished the design of a 4-bit carry ripple adder in two logic expressions and in two new logic methods: D3L and SPD3L. I checked the logic correctness for this design and discussed about the performance of it related to power and timing issue. Finally, I make a choice between different logics and methods.

However, the power effect is not clear which means the optimization for this design is not enough. We can try different structure and different logic on it to search for a better design.

References

- [1] Ramin Rafati Sied Mehdi Fakhraie Kenneth Carless Smith, “A 16-Bit Barrel-Shifter Implemented in Data-Driven Dynamic Logic (D3L)”, IEEE Transactions On Circuits And Systems—I: Regular Papers, Vol. 53, No. 10, October 2006.
- [2] F. Frustaci M. Lanuzza P. Zicari S. Perri P. Corsonello, “Low-power split-path data-driven dynamic logic”, IET Circuits Devices Syst., 2009, Vol. 3, Iss. 6, pp. 303–312

Appendix I Netlist Files

All .sp files are attached with this project.

Appendix II Screenshots

Because all the screenshots are too large to be shown clear enough here, so all the picture files have been put into the attached files.

Appendix III Full report

t1_d3l_measure.mt0:

```
$DATA1 SOURCE='HSPICE' VERSION='F-2011.09-SP2 32-BIT'  
.TITLE '** generated for: hspiced'  
avgpwr          maxpwr          tpdr          temper  
alter#  
 8.888e-05      1.047e-03      8.578e-11      2.500e+01  
1
```

t1_sp_measure.mt0:

```
$DATA1 SOURCE='HSPICE' VERSION='F-2011.09-SP2 32-BIT'  
.TITLE '** generated for: hspiced'  
avgpwr          maxpwr          tpdr          temper  
alter#  
 9.370e-05      9.939e-04      8.322e-11      2.500e+01  
1
```

t2_d3l_measure.mt0:

```
$DATA1 SOURCE='HSPICE' VERSION='F-2011.09-SP2 32-BIT'  
.TITLE '** generated for: hspiced'  
avgpwr          maxpwr          tpdr          temper  
alter#  
 1.383e-04      1.220e-03      1.179e-10      2.500e+01  
1
```

t2_sp_measure.mt0:

```
$DATA1 SOURCE='HSPICE' VERSION='F-2011.09-SP2 32-BIT'  
.TITLE '** generated for: hspiced'  
avgpwr          maxpwr          tpdr          temper  
alter#  
 1.235e-04      1.215e-03      1.046e-10      2.500e+01  
1
```

Power1.log:

```
-----  
| | NanoSim Version F-2011.09-SP2 | |  
| | SN:20120217-linux | |  
| | Machine Name: saturn.ece.iit.edu | |  
| | Copyright (c) 2011 Synopsys Inc., All Rights Reserved. | |  
| |-----
```

Built by nsmgr on Fri Feb 17 01:57:23 PST 2012
Sat May 11 06:11:29 CDT 2013

Command line options: -nspice ./t1_d3l.sp -C ./power.cfg -o ./power

The 32-bit version of the simulator is running.

Initializing system messages took 0.000 s

LICENSE Information:

-- Key: TIMEMILL__NSADDON
-- Version: 2011.09

Installing interactive/configuration commands ...

Installing commands took 0.010 s

Start netlist compilation at Sat May 11 06:11:30 2013

Compiling "t1_d3l.sp" (SPICE)

Compiling "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include" (SPICE)

Compiling

"./apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTG.inc"
(SPICE)

Compiling

"./apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTG.inc"
(SPICE)

Compiling

"./apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTL.inc"
(SPICE)

Compiling

"./apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTL.inc"

```
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTH.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTH.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_THKOX.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_THKOX.inc"
(SPICE)
```

Parsing netlist finished in 0 seconds

Circuit temperature from netlist : 25.000

Netlist compilation will be case insensitive.

All letters will be converted to lower case.

Building instance tree finished in 0 seconds

Finish netlist compilation at Sat May 11 06:11:30 2013

Netlist compilation took 0.020 s

NOTICE:Techfile Voltage (*nanosim tech="voltage") set to 1.1V ...

This simulation uses HSPICE models

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'nmos_vtg'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'nmos_vth'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'nmos_vtl'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'pmos_vtg'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'pmos_thkox'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'pmos_vtl'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104432:MISC MODEL PROBLEM: ** warning** associated with encrypted blocks were suppressed

Building node/element arrays took 1.570 s

Reading configuration files ...

;This is a GUI generated file.

;It is overwritten and updated for each run.

```
set_sim_eou sim=7 model=7 net=7
set_inst_cmd * set_sim_eou sim=7 model=7 net=7
report_ckt_leak no=* p_path n_path nc_vdd nc_gnd to_vdd to_gnd static_leak stuck_at_1
stuck_at_0 partial_off_p partial_off_n forward_bias_p forward_bias_n
report_block_powr erdal show_details=1 track_gnd=1 track_power=1 track_wasted=1
split_wasted=1 *
report_node_powr m0
print_node_logic *
```

Reading configuration files took -0.000000 s

WARNING:NanoSim:0x211080eb:report_node_powr: UNABLE TO FIND NODE "m0".

WARNING:NanoSim:0x21108427:Output current waveform sampling resolution (= 1e-09 A) is smaller than the simulation current resolution (= 1e-06 A).

# of CMOS elements	:	222
# of dc voltage sources	:	10
# of independent sources	:	1
# of elements	:	239
# of used elements	:	229
# of nodes	:	129
# of subckt	:	8
# of top-level instances	:	18
# of capacitors from netlist	:	6
# of Ground CAPS from netlist	:	0
# of Coupling CAPS from netlist	:	6
# of Coupling CAPS from netlist and converted diodes	:	6

# of Coupling CAPS kept (see .fcap file)	:	6
# of Coupling CAPS put into SMS Mode	:	0
# of Coupling CAPS split to ground	:	0

Circuit partitioning ...

Among 1 stages, there are:

- 0 pwl stages
- 0 grouped pwl stages
- 1 analog stages
- 0 NR stages
- 0 grouped analog stages
- 0 rc stages
- 0 ud stages
- 0 ADFMI functional model stages
- 117 nodes in the largest pwl stage
- 0 nodes in the largest digital stage

1 stages (1 pwl/analog stages) with 100-149 nodes

Among 129 nodes, there are:

- 0 pwl nodes
- 129 analog (accurate) nodes
- 0 rc nodes
- 0 ud nodes

- 0 cut nodes
- 0 mem_cut nodes
- 129 no_clamp nodes
- 117 nodes in stages
- 12 voltage source nodes
- 11 constant nodes
- 0 NR nodes

Among 239 elements, there are:

- 228 elements in stages
- 6 pwl elements
- 0 synchronous elements
- 0 SMS elements
- 222 analog (accurate) elements
- 0 rc elements
- 0 ud elements

0 ADFMI functional model elements

0 VERILOGA model elements

0 behavioral model elements

228 mna elements

0 NR elements

0 mos transistors identified as keepers

222 mos transistors need Subthreshold current

0 keepers removed

0 keepers reduced

Circuit partitioning took 0.010 s

Executing static power analysis ...

Static power analysis took -0.000 s

Constructing matrix ...

Matrix ordering and construction took -0.000 s

Profiling block-number for individual report_block_powr configuration commands (1 cmd's totally)

Cmd 1: 1 blocks from "report_block_powr erdal show_details=1 track_gnd=1 track_power=1 track_wasted=1 split_wasted=1 * "

Processing block power (number of blocks: 1) ...

After reading configuration file(s), 129 signals are identified to be printed:

129 logic signals

Statistics of memory used for signal printing:

16201896 bytes allocated in total, including:

56008 bytes allocated for node current/voltage/logic signals

8084908 bytes allocated additionally for node current signals

8060980 bytes allocated additionally for element branch current signals

Levelizing stages ...

Levelizing stages took 0.000 s

DC initialization ...

Finishing initialization (level 0 -- 0)

0 dynamic stages assigned in DC Initialization

Number of residual dc events scheduled : 0

Number of ic nodes scheduled : 0

DC initialization took 0.100 s

Simulation begins in pwl mode ...

Simulation ends at 4.000 ns

Simulation took 13.830 s

Current information calculated over the intervals:

0.00000e+00 - 4.00010e+00 ns

Block: erdal

Number of nodes in block : 117

Number of elements in block : 228

Number of block supply nodes : 10

Number of block ground nodes : 1

Number of block biput nodes : 0

Number of block input nodes : 1

Number of block output nodes : 0

Number of block stages : 1

Number of block partial stages : 0

Average supply current : -81.671113 uA

RMS supply current : 233.060789 uA

Average ground current : 81.332467 uA

RMS ground current : 224.755546 uA

Average input current : 0.336806 uA

RMS input current : 80.917518 uA

Average output current : 0.000000 uA

RMS output current : 0.000000 uA

Average biput current : 0.000000 uA

RMS biput current : 0.000000 uA

Average capacitive current : -82.363278 uA

RMS capacitive current : 222.931871 uA

Average wasted current : -10.835059 uA

RMS wasted current : 46.958439 uA

Average static wasted current: -0.000537 uA

RMS static wasted current : 0.021475 uA

Average dynamic wasted current : -10.834522 uA

RMS dynamic wasted current : 46.958434 uA

Wasted current percentage : 11.625807%

Average block power : 89.838225 uW

RMS block power : 256.366868 uW

Supply node currents:

Node: b3

Average current : -0.000191 uA

RMS current : 0.190234 uA

Node: b2

Average current : -0.000203 uA

RMS current : 0.191226 uA

Node: a3

Average current : -0.000171 uA

RMS current : 0.190443 uA

Node: cin

Average current : 0.000153 uA

RMS current : 0.376017 uA

Node: b1

Average current : -0.000186 uA

RMS current : 0.191421 uA

Node: b0

Average current : -0.000186 uA

RMS current : 0.186593 uA

Node: a2

Average current : -0.000169 uA

RMS current : 0.190660 uA

Node: a1

Average current : -0.000180 uA

RMS current : 0.190746 uA

Node: a0

Average current : -0.000177 uA

RMS current : 0.188833 uA

Node: vdd!

Average current : -81.669801 uA

RMS current : 233.107625 uA

Ground node currents:

Node: 0
Average current : 81.332467 uA
RMS current : 224.755546 uA

Input node currents:

Node: pr
Average current : 0.336806 uA
RMS current : 80.917518 uA

Simulation time resolution : 1.000e-04 ns
Print time resolution : 1.000e-04 ns
Number of PWL matrix solutions : 3551
Number of PWL MOS model lookups : 762769
Number of time steps : 3523
Number of iterations : 0
Number of rejected time steps : 0

Global simulation parameters used:

SPD	0.006875V	ASPD	0.00275V
SIM_DESV	0.006875V	SIM_AESV	0.00275V
VDS_MIN	1e-06V	AVDS_MIN	1e-11V
SSC (steady state current)	0.0001uA		
SUBI (subthreshold current)	0.001uA		
DC CURRENT		0.01uA	
16.0 real	15.6 user	0.1 sys	

Signal data is saved in ./power.out

Total number of errors reported in the .err file (./power.err): 88

Please use the viewerror utility to view the detailed error messages

Summary of Errors

=====

T_CODE(8):

D_CODE (3): 23
D_CODE (4): 28
D_CODE (5): 4
D_CODE (6): 3
D_CODE (8): 8
D_CODE (9): 22

Power2.log:

```
-----  
|  
|      NanoSim Version F-2011.09-SP2  
|      SN:20120217-linux  
|      Machine Name: saturn.ece.iit.edu  
| Copyright (c) 2011 Synopsys Inc., All Rights Reserved.  
|  
-----
```

Built by nsmgr on Fri Feb 17 01:57:23 PST 2012
Sat May 11 06:16:51 CDT 2013

Command line options: -nspice ./t1_sp.sp -C ./power.cfg -o ./power

The 32-bit version of the simulator is running.

Initializing system messages took 0.000 s

LICENSE Information:

-- Key: TIMEMILL__NSADDON
-- Version: 2011.09

Installing interactive/configuration commands ...

Installing commands took 0.020 s

Start netlist compilation at Sat May 11 06:16:51 2013

Compiling "t1_sp.sp" (SPICE)
Compiling "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include" (SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTG.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTG.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTL.inc"
(SPICE)
Compiling

```
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTL.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTH.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTH.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_THKOX.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_THKOX.inc"
(SPICE)
```

Parsing netlist finished in 0 seconds

Circuit temperature from netlist : 25.000

Netlist compilation will be case insensitive.
All letters will be converted to lower case.
Building instance tree finished in 0 seconds

Finish netlist compilation at Sat May 11 06:16:51 2013

Netlist compilation took 0.020 s
NOTICE:Techfile Voltage (*nanosim tech="voltage") set to 1.1V ...

This simulation uses HSPICE models

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'nmos_vtg'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'nmos_vth'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'nmos_vtl'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'pmos_vtg'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'pmos_thkox'): tox, toxp, and dtox all given and tox != toxp + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'pmos_vtl'): tox, toxp, and dtox all given and tox != toxp + dtox; dtox ignored...

WARNING:NanoSim:0x21104432:MISC MODEL PROBLEM: ** warning** associated with encrypted blocks were suppressed

Building node/element arrays took 1.350 s

Reading configuration files ...

;This is a GUI generated file.

;It is overwritten and updated for each run.

```
set_sim_eou sim=7 model=7 net=7
set_inst_cmd * set_sim_eou sim=7 model=7 net=7
report_ckt_leak no=* p_path n_path nc_vdd nc_gnd to_vdd to_gnd static_leak stuck_at_1
stuck_at_0 partial_off_p partial_off_n forward_bias_p forward_bias_n
report_block_powr erdal show_details=1 track_gnd=1 track_power=1 track_wasted=1
split_wasted=1 *
report_node_powr m0
print_node_logic *
```

Reading configuration files took 0.000000 s

WARNING:NanoSim:0x211080eb:report_node_powr: UNABLE TO FIND NODE "m0".

WARNING:NanoSim:0x21108427:Output current waveform sampling resolution (= 1e-09 A) is smaller than the simulation current resolution (= 1e-06 A).

# of CMOS elements	:	258
# of dc voltage sources	:	10
# of independent sources	:	1
# of elements	:	275
# of used elements	:	265
# of nodes	:	141
# of subckt	:	9
# of top-level instances	:	18
# of capacitors from netlist	:	6
# of Ground CAPS from netlist	:	0
# of Coupling CAPS from netlist	:	6

# of Coupling CAPS from netlist and converted diodes	:	6
# of Coupling CAPS kept (see .fcap file)	:	6
# of Coupling CAPS put into SMS Mode	:	0
# of Coupling CAPS split to ground	:	0

Circuit partitioning ...

Among 1 stages, there are:

- 0 pwl stages
- 0 grouped pwl stages
- 1 analog stages
- 0 NR stages
- 0 grouped analog stages
- 0 rc stages
- 0 ud stages
- 0 ADFMI functional model stages
- 129 nodes in the largest pwl stage
- 0 nodes in the largest digital stage

1 stages (1 pwl/analog stages) with 100-149 nodes

Among 141 nodes, there are:

- 0 pwl nodes
- 141 analog (accurate) nodes
- 0 rc nodes
- 0 ud nodes

- 0 cut nodes
- 0 mem_cut nodes
- 141 no_clamp nodes
- 129 nodes in stages
- 12 voltage source nodes
- 11 constant nodes
- 0 NR nodes

Among 275 elements, there are:

- 264 elements in stages
- 6 pwl elements
- 0 synchronous elements
- 0 SMS elements
- 258 analog (accurate) elements
- 0 rc elements

0 ud elements
0 ADFMI functional model elements
0 VERILOGA model elements
0 behavioral model elements

264 mna elements
0 NR elements
0 mos transistors identified as keepers
258 mos transistors need Subthreshold current
0 keepers removed
0 keepers reduced

Circuit partitioning took 0.000 s

Executing static power analysis ...

Static power analysis took 0.000 s

Constructing matrix ...

Matrix ordering and construction took 0.000 s

Profiling block-number for individual report_block_powr configuration commands (1 cmd's totally)

Cmd 1: 1 blocks from "report_block_powr erdal show_details=1 track_gnd=1 track_power=1 track_wasted=1 split_wasted=1 * "

Processing block power (number of blocks: 1) ...

After reading configuration file(s), 141 signals are identified to be printed:

141 logic signals

Statistics of memory used for signal printing:

16202040 bytes allocated in total, including:

56008 bytes allocated for node current/voltage/logic signals

8084908 bytes allocated additionally for node current signals

8061124 bytes allocated additionally for element branch current signals

Levelizing stages ...

Levelizing stages took 0.000 s

DC initialization ...

Finishing initialization (level 0 -- 0)

0 dynamic stages assigned in DC Initialization

Number of residual dc events scheduled : 0

Number of ic nodes scheduled : 0
DC initialization took 0.140 s

Simulation begins in pwl mode ...
Simulation ends at 4.000 ns

Simulation took 17.770 s

Current information calculated over the intervals:

0.00000e+00 - 4.00010e+00 ns

Block: erdal

Number of nodes in block : 129
Number of elements in block : 264
Number of block supply nodes : 10
Number of block ground nodes : 1
Number of block biput nodes : 0
Number of block input nodes : 1
Number of block output nodes : 0
Number of block stages : 1
Number of block partial stages : 0

Average supply current : -86.168480 uA
RMS supply current : 247.301823 uA

Average ground current : 85.832500 uA
RMS ground current : 236.316789 uA

Average input current : 0.334279 uA
RMS input current : 81.235262 uA

Average output current : 0.000000 uA
RMS output current : 0.000000 uA

Average biput current : 0.000000 uA
RMS biput current : 0.000000 uA

Average capacitive current : -84.267438 uA
RMS capacitive current : 222.395140 uA

Average wasted current : -13.535713 uA
RMS wasted current : 56.827435 uA

Average static wasted current: -0.000579 uA
RMS static wasted current : 0.023150 uA

Average dynamic wasted current : -13.535134 uA
RMS dynamic wasted current : 56.827431 uA

Wasted current percentage : 13.839751%

Average block power : 94.785328 uW
RMS block power : 272.032006 uW

Supply node currents:

Node: b3
Average current : -0.000190 uA
RMS current : 0.191830 uA
Node: b2
Average current : -0.000197 uA
RMS current : 0.193003 uA
Node: a3
Average current : -0.000190 uA
RMS current : 0.192828 uA
Node: cin
Average current : 0.000158 uA
RMS current : 0.493495 uA
Node: b1
Average current : -0.000196 uA
RMS current : 0.194697 uA
Node: b0
Average current : -0.000195 uA
RMS current : 0.187737 uA
Node: a2
Average current : -0.000198 uA
RMS current : 0.192964 uA
Node: a1
Average current : -0.000195 uA
RMS current : 0.193254 uA
Node: a0
Average current : -0.000190 uA
RMS current : 0.191577 uA
Node: vdd!
Average current : -86.167087 uA

RMS current : 247.320930 uA

Ground node currents:

Node: 0
Average current : 85.832500 uA
RMS current : 236.316789 uA

Input node currents:

Node: pr
Average current : 0.334279 uA
RMS current : 81.235262 uA

Simulation time resolution : 1.000e-04 ns
Print time resolution : 1.000e-04 ns
Number of PWL matrix solutions : 4309
Number of PWL MOS model lookups : 1071185
Number of time steps : 4277
Number of iterations : 0
Number of rejected time steps : 409

Global simulation parameters used:

SPD	0.006875V	ASPD	0.00275V
SIM_DESV	0.006875V	SIM_AESV	0.00275V
VDS_MIN	1e-06V	AVDS_MIN	1e-11V
SSC (steady state current)	0.0001uA		
SUBI (subthreshold current)	0.001uA		
DC CURRENT		0.01uA	
20.0 real	19.3 user	0.1 sys	

Signal data is saved in ./power.out

Total number of errors reported in the .err file (./power.err): 96

Please use the viewerror utility to view the detailed error messages

Summary of Errors

=====

T_CODE(8):

D_CODE (3): 23
D_CODE (4): 28
D_CODE (6): 3
D_CODE (8): 20
D_CODE (9): 22

Power3.log:

```
-----  
|  
|      NanoSim Version F-2011.09-SP2  
|      SN:20120217-linux  
|      Machine Name: saturn.ece.iit.edu  
| Copyright (c) 2011 Synopsys Inc., All Rights Reserved.  
|  
-----
```

Built by nsmgr on Fri Feb 17 01:57:23 PST 2012
Sat May 11 06:18:39 CDT 2013

Command line options: -nspice ./t2_d3l.sp -C ./power.cfg -o ./power

The 32-bit version of the simulator is running.

Initializing system messages took 0.010 s

LICENSE Information:

-- Key: TIMEMILL__NSADDON
-- Version: 2011.09

Installing interactive/configuration commands ...

Installing commands took 0.010 s

Start netlist compilation at Sat May 11 06:18:40 2013

Compiling "t2_d3l.sp" (SPICE)
Compiling "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include" (SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTG.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTG.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTL.inc"
(SPICE)
Compiling

```
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTL.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTH.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTH.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_THKOX.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_THKOX.inc"
(SPICE)
```

Parsing netlist finished in 0 seconds

Circuit temperature from netlist : 25.000

Netlist compilation will be case insensitive.
All letters will be converted to lower case.
Building instance tree finished in 0 seconds

Finish netlist compilation at Sat May 11 06:18:40 2013

Netlist compilation took 0.030 s
NOTICE:Techfile Voltage (*nanosim tech="voltage") set to 1.1V ...

This simulation uses HSPICE models

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'nmos_vtg'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'nmos_vth'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'nmos_vtl'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'pmos_vtg'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'pmos_thkox'): tox, toxp, and dtox all given and tox != toxp + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'pmos_vtl'): tox, toxp, and dtox all given and tox != toxp + dtox; dtox ignored...

WARNING:NanoSim:0x21104432:MISC MODEL PROBLEM: ** warning** associated with encrypted blocks were suppressed

Building node/element arrays took 1.340 s

Reading configuration files ...

;This is a GUI generated file.

;It is overwritten and updated for each run.

```
set_sim_eou sim=7 model=7 net=7
set_inst_cmd * set_sim_eou sim=7 model=7 net=7
report_ckt_leak no=* p_path n_path nc_vdd nc_gnd to_vdd to_gnd static_leak stuck_at_1
stuck_at_0 partial_off_p partial_off_n forward_bias_p forward_bias_n
report_block_powr erdal show_details=1 track_gnd=1 track_power=1 track_wasted=1
split_wasted=1 *
report_node_powr m0
print_node_logic *
```

Reading configuration files took 0.000000 s

WARNING:NanoSim:0x211080eb:report_node_powr: UNABLE TO FIND NODE "m0".

WARNING:NanoSim:0x21108427:Output current waveform sampling resolution (= 1e-09 A) is smaller than the simulation current resolution (= 1e-06 A).

# of CMOS elements	:	306
# of dc voltage sources	:	10
# of independent sources	:	1
# of elements	:	323
# of used elements	:	313
# of nodes	:	169
# of subckt	:	10
# of top-level instances	:	18
# of capacitors from netlist	:	6
# of Ground CAPS from netlist	:	0
# of Coupling CAPS from netlist	:	6

# of Coupling CAPS from netlist and converted diodes	:	6
# of Coupling CAPS kept (see .fcap file)	:	6
# of Coupling CAPS put into SMS Mode	:	0
# of Coupling CAPS split to ground	:	0

Circuit partitioning ...

Among 1 stages, there are:

- 0 pwl stages
- 0 grouped pwl stages
- 1 analog stages
- 0 NR stages
- 0 grouped analog stages
- 0 rc stages
- 0 ud stages
- 0 ADFMI functional model stages
- 157 nodes in the largest pwl stage
- 0 nodes in the largest digital stage

1 stages (1 PWL stages) with 150-199 nodes

Among 169 nodes, there are:

- 0 pwl nodes
- 169 analog (accurate) nodes
- 0 rc nodes
- 0 ud nodes

- 0 cut nodes
- 0 mem_cut nodes
- 169 no_clamp nodes
- 157 nodes in stages
- 12 voltage source nodes
- 11 constant nodes
- 0 NR nodes

Among 323 elements, there are:

- 312 elements in stages
- 6 pwl elements
- 0 synchronous elements
- 0 SMS elements
- 306 analog (accurate) elements
- 0 rc elements

0 ud elements
0 ADFMI functional model elements
0 VERILOGA model elements
0 behavioral model elements

312 mna elements
0 NR elements
0 mos transistors identified as keepers
306 mos transistors need Subthreshold current
0 keepers removed
0 keepers reduced

Circuit partitioning took 0.000 s

Executing static power analysis ...

Static power analysis took 0.000 s

Constructing matrix ...

Matrix ordering and construction took 0.000 s

Profiling block-number for individual report_block_powr configuration commands (1 cmd's totally)

Cmd 1: 1 blocks from "report_block_powr erdal show_details=1 track_gnd=1 track_power=1 track_wasted=1 split_wasted=1 * "

Processing block power (number of blocks: 1) ...

After reading configuration file(s), 169 signals are identified to be printed:

169 logic signals

Statistics of memory used for signal printing:

16202208 bytes allocated in total, including:

56008 bytes allocated for node current/voltage/logic signals

8084884 bytes allocated additionally for node current signals

8061316 bytes allocated additionally for element branch current signals

Levelizing stages ...

Levelizing stages took 0.000 s

DC initialization ...

Finishing initialization (level 0 -- 0)

0 dynamic stages assigned in DC Initialization

Number of residual dc events scheduled : 0

Number of ic nodes scheduled : 0
DC initialization took 0.160 s

Simulation begins in pwl mode ...
Simulation ends at 4.000 ns

Simulation took 26.520 s

Current information calculated over the intervals:

0.00000e+00 - 4.00010e+00 ns

Block: erdal

Number of nodes in block : 157
Number of elements in block : 312
Number of block supply nodes : 10
Number of block ground nodes : 1
Number of block biput nodes : 0
Number of block input nodes : 1
Number of block output nodes : 0
Number of block stages : 1
Number of block partial stages : 0

Average supply current : -127.879046 uA
RMS supply current : 311.240016 uA

Average ground current : 127.538895 uA
RMS ground current : 305.071708 uA

Average input current : 0.338173 uA
RMS input current : 81.050944 uA

Average output current : 0.000000 uA
RMS output current : 0.000000 uA

Average biput current : 0.000000 uA
RMS biput current : 0.000000 uA

Average capacitive current : -116.886774 uA
RMS capacitive current : 286.793335 uA

Average wasted current : -29.102092 uA
RMS wasted current : 99.498752 uA

Average static wasted current: -0.001137 uA
RMS static wasted current : 0.045499 uA

Average dynamic wasted current : -29.100955 uA
RMS dynamic wasted current : 99.498742 uA

Wasted current percentage : 19.934460%

Average block power : 140.666950 uW
RMS block power : 342.364018 uW

Supply node currents:

Node: b3
Average current : -0.000205 uA
RMS current : 0.199273 uA

Node: b2
Average current : -0.000205 uA
RMS current : 0.199273 uA

Node: a3
Average current : -0.000218 uA
RMS current : 0.204300 uA

Node: cin
Average current : 0.000952 uA
RMS current : 1.896768 uA

Node: b1
Average current : -0.000205 uA
RMS current : 0.199273 uA

Node: b0
Average current : -0.000206 uA
RMS current : 0.199271 uA

Node: a2
Average current : -0.000218 uA
RMS current : 0.204300 uA

Node: a1
Average current : -0.000218 uA
RMS current : 0.204300 uA

Node: a0
Average current : -0.000220 uA
RMS current : 0.204300 uA

Node: vdd!
Average current : -127.878302 uA

RMS current : 311.426084 uA

Ground node currents:

Node: 0
Average current : 127.538895 uA
RMS current : 305.071708 uA

Input node currents:

Node: pr
Average current : 0.338173 uA
RMS current : 81.050944 uA

Simulation time resolution : 1.000e-04 ns
Print time resolution : 1.000e-04 ns
Number of PWL matrix solutions : 5555
Number of PWL MOS model lookups : 1597135
Number of time steps : 5523
Number of iterations : 0
Number of rejected time steps : 612

Global simulation parameters used:

SPD	0.006875V	ASPD	0.00275V
SIM_DESV	0.006875V	SIM_AESV	0.00275V
VDS_MIN	1e-06V	AVDS_MIN	1e-11V
SSC (steady state current)	0.0001uA		
SUBI (subthreshold current)	0.001uA		
DC CURRENT		0.01uA	
29.0 real	28.1 user	0.1 sys	

Signal data is saved in ./power.out

Total number of errors reported in the .err file (./power.err): 51

Please use the viewerror utility to view the detailed error messages

Summary of Errors

=====

T_CODE(8):

D_CODE (3): 1
D_CODE (4): 32
D_CODE (6): 1
D_CODE (9): 17

Power4.log:

```
-----  
|  
|      NanoSim Version F-2011.09-SP2  
|      SN:20120217-linux  
|      Machine Name: saturn.ece.iit.edu  
| Copyright (c) 2011 Synopsys Inc., All Rights Reserved.  
|  
-----
```

Built by nsmgr on Fri Feb 17 01:57:23 PST 2012
Sat May 11 06:19:43 CDT 2013

Command line options: -nspice ./t2_sp.sp -C ./power.cfg -o ./power

The 32-bit version of the simulator is running.

Initializing system messages took 0.010 s

LICENSE Information:

-- Key: TIMEMILL__NSADDON
-- Version: 2011.09

Installing interactive/configuration commands ...

Installing commands took 0.010 s

Start netlist compilation at Sat May 11 06:19:43 2013

Compiling "t2_sp.sp" (SPICE)

Compiling "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include" (SPICE)

Compiling

"./apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTG.inc"
(SPICE)

Compiling

"./apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTG.inc"
(SPICE)

Compiling

"./apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTL.inc"
(SPICE)

Compiling

"./apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTL.inc"

```
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTH.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTH.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_THKOX.inc"
(SPICE)
Compiling
"/apps/FreePDK45/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_THKOX.inc"
(SPICE)
```

Parsing netlist finished in 0 seconds

Circuit temperature from netlist : 25.000

Netlist compilation will be case insensitive.

All letters will be converted to lower case.

Building instance tree finished in 0 seconds

Finish netlist compilation at Sat May 11 06:19:43 2013

Netlist compilation took 0.030 s

NOTICE:Techfile Voltage (*nanosim tech="voltage") set to 1.1V ...

This simulation uses HSPICE models

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'nmos_vtg'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'nmos_vth'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'nmos_vtl'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'pmos_vtg'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'pmos_thkox'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104430:SUSPICIOUS MODEL PARAMETER VALUE: Warning (model 'pmos_vtl'): tox_e, tox_p, and dtox all given and tox_e != tox_p + dtox; dtox ignored...

WARNING:NanoSim:0x21104432:MISC MODEL PROBLEM: ** warning** associated with encrypted blocks were suppressed

Building node/element arrays took 1.120 s

Reading configuration files ...

;This is a GUI generated file.

;It is overwritten and updated for each run.

```
set_sim_eou sim=7 model=7 net=7
set_inst_cmd * set_sim_eou sim=7 model=7 net=7
report_ckt_leak no=* p_path n_path nc_vdd nc_gnd to_vdd to_gnd static_leak stuck_at_1
stuck_at_0 partial_off_p partial_off_n forward_bias_p forward_bias_n
report_block_powr erdal show_details=1 track_gnd=1 track_power=1 track_wasted=1
split_wasted=1 *
report_node_powr m0
print_node_logic *
```

Reading configuration files took 0.000000 s

WARNING:NanoSim:0x211080eb:report_node_powr: UNABLE TO FIND NODE "m0".

WARNING:NanoSim:0x21108427:Output current waveform sampling resolution (= 1e-09 A) is smaller than the simulation current resolution (= 1e-06 A).

# of CMOS elements	:	378
# of dc voltage sources	:	10
# of independent sources	:	1
# of elements	:	395
# of used elements	:	385
# of nodes	:	193
# of subckt	:	11
# of top-level instances	:	18
# of capacitors from netlist	:	6
# of Ground CAPS from netlist	:	0
# of Coupling CAPS from netlist	:	6
# of Coupling CAPS from netlist and converted diodes	:	6

# of Coupling CAPS kept (see .fcap file)	:	6
# of Coupling CAPS put into SMS Mode	:	0
# of Coupling CAPS split to ground	:	0

Circuit partitioning ...

Among 1 stages, there are:

- 0 pwl stages
- 0 grouped pwl stages
- 1 analog stages
- 0 NR stages
- 0 grouped analog stages
- 0 rc stages
- 0 ud stages
- 0 ADFMI functional model stages
- 181 nodes in the largest pwl stage
- 0 nodes in the largest digital stage

1 stages (1 PWL stages) with 150-199 nodes

Among 193 nodes, there are:

- 0 pwl nodes
- 193 analog (accurate) nodes
- 0 rc nodes
- 0 ud nodes

- 0 cut nodes
- 0 mem_cut nodes
- 193 no_clamp nodes
- 181 nodes in stages
- 12 voltage source nodes
- 11 constant nodes
- 0 NR nodes

Among 395 elements, there are:

- 384 elements in stages
- 6 pwl elements
- 0 synchronous elements
- 0 SMS elements
- 378 analog (accurate) elements
- 0 rc elements
- 0 ud elements

0 ADFMI functional model elements
0 VERILOGA model elements
0 behavioral model elements

384 mna elements
0 NR elements
0 mos transistors identified as keepers
378 mos transistors need Subthreshold current
0 keepers removed
0 keepers reduced

Circuit partitioning took 0.000 s

Executing static power analysis ...
Static power analysis took 0.000 s

Constructing matrix ...
Matrix ordering and construction took 0.010 s
Profiling block-number for individual report_block_powr configuration commands (1 cmd's totally)
Cmd 1: 1 blocks from "report_block_powr erdal show_details=1 track_gnd=1 track_power=1 track_wasted=1 split_wasted=1 *"
Processing block power (number of blocks: 1) ...

After reading configuration file(s), 193 signals are identified to be printed:

193 logic signals

Statistics of memory used for signal printing:
16202496 bytes allocated in total, including:
 56008 bytes allocated for node current/voltage/logic signals
 8084884 bytes allocated additionally for node current signals
 8061604 bytes allocated additionally for element branch current signals

Levelizing stages ...
Levelizing stages took 0.000 s
DC initialization ...

Finishing initialization (level 0 -- 0)
0 dynamic stages assigned in DC Initialization

Number of residual dc events scheduled	: 0
Number of ic nodes scheduled	: 0

DC initialization took 0.200 s

Simulation begins in pwl mode ...

Simulation ends at 4.000 ns

Simulation took 31.960 s

Current information calculated over the intervals:

0.00000e+00 - 4.00010e+00 ns

Block: erdal

Number of nodes in block : 181

Number of elements in block : 384

Number of block supply nodes : 10

Number of block ground nodes : 1

Number of block biput nodes : 0

Number of block input nodes : 1

Number of block output nodes : 0

Number of block stages : 1

Number of block partial stages : 0

Average supply current : -114.432538 uA

RMS supply current : 290.454128 uA

Average ground current : 114.094941 uA

RMS ground current : 283.276947 uA

Average input current : 0.335662 uA

RMS input current : 81.210586 uA

Average output current : 0.000000 uA

RMS output current : 0.000000 uA

Average biput current : 0.000000 uA

RMS biput current : 0.000000 uA

Average capacitive current : -101.351269 uA

RMS capacitive current : 250.142241 uA

Average wasted current : -25.132652 uA

RMS wasted current : 90.153599 uA

Average static wasted current: -0.001334 uA

RMS static wasted current : 0.053374 uA

Average dynamic wasted current : -25.131317 uA

RMS dynamic wasted current : 90.153583 uA

Wasted current percentage : 19.870235%

Average block power : 125.875791 uW

RMS block power : 319.499541 uW

Supply node currents:

Node: b3

Average current : -0.000197 uA

RMS current : 0.195250 uA

Node: b2

Average current : -0.000196 uA

RMS current : 0.195250 uA

Node: a3

Average current : -0.000201 uA

RMS current : 0.186936 uA

Node: cin

Average current : 0.000881 uA

RMS current : 1.964833 uA

Node: b1

Average current : -0.000196 uA

RMS current : 0.195250 uA

Node: b0

Average current : -0.000198 uA

RMS current : 0.195251 uA

Node: a2

Average current : -0.000202 uA

RMS current : 0.186935 uA

Node: a1

Average current : -0.000202 uA

RMS current : 0.186937 uA

Node: a0

Average current : -0.000201 uA

RMS current : 0.186935 uA

Node: vdd!

Average current : -114.431824 uA

RMS current : 290.576578 uA

Ground node currents:

Node: 0

Average current	:	114.094941 uA
RMS current	:	283.276947 uA

Input node currents:

Node: pr

Average current	:	0.335662 uA
RMS current	:	81.210586 uA

Simulation time resolution	:	1.000e-04 ns
Print time resolution	:	1.000e-04 ns
Number of PWL matrix solutions	:	5684
Number of PWL MOS model lookups	:	2038194
Number of time steps	:	5652
Number of iterations	:	0
Number of rejected time steps	:	894

Global simulation parameters used:

SPD	0.006875V	ASPD	0.00275V
SIM_DESV	0.006875V	SIM_AESV	0.00275V
VDS_MIN	1e-06V	AVDS_MIN	1e-11V
SSC (steady state current)	0.0001uA		
SUBI (subthreshold current)	0.001uA		
DC CURRENT		0.01uA	
34.0 real	33.4 user	0.1 sys	

Signal data is saved in ./power.out

Total number of errors reported in the .err file (./power.err): 66

Please use the viewerror utility to view the detailed error messages

Summary of Errors

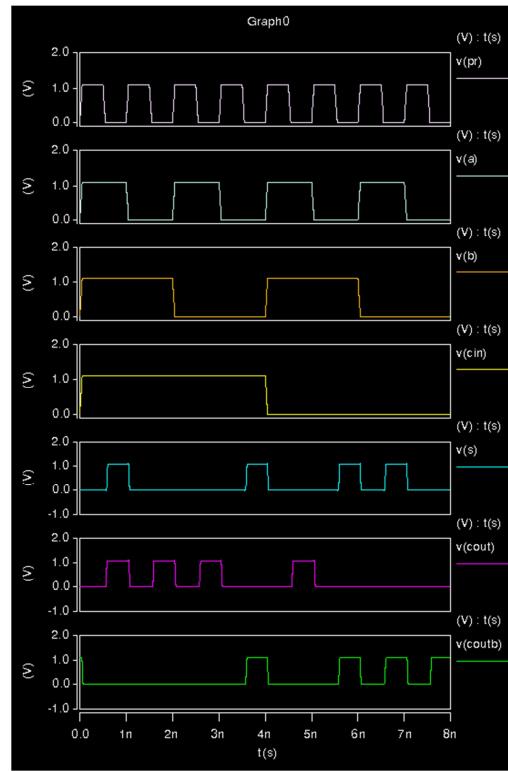
=====

T_CODE(8):

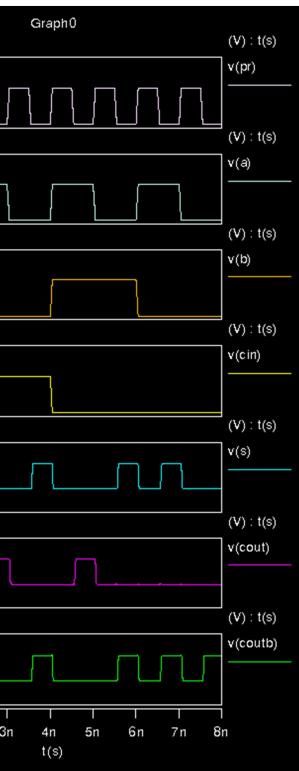
D_CODE (3):	1
D_CODE (4):	27
D_CODE (6):	9
D_CODE (8):	12
D_CODE (9):	17

Appendix IV Waveform

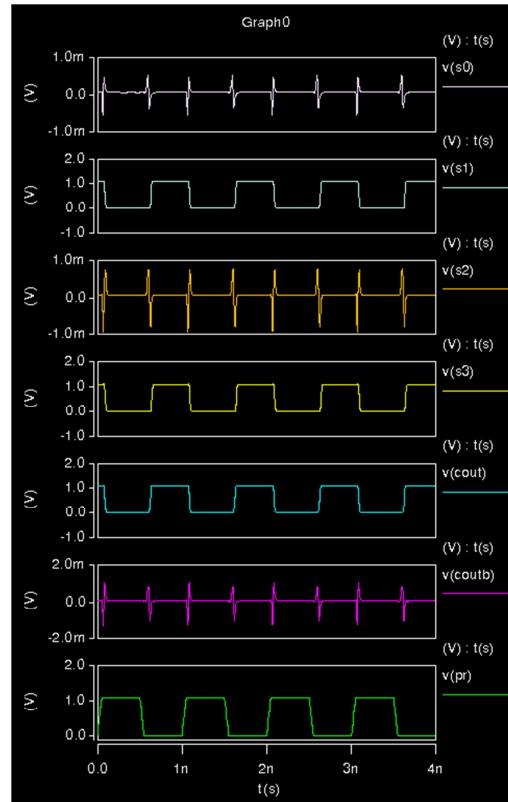
FA1:



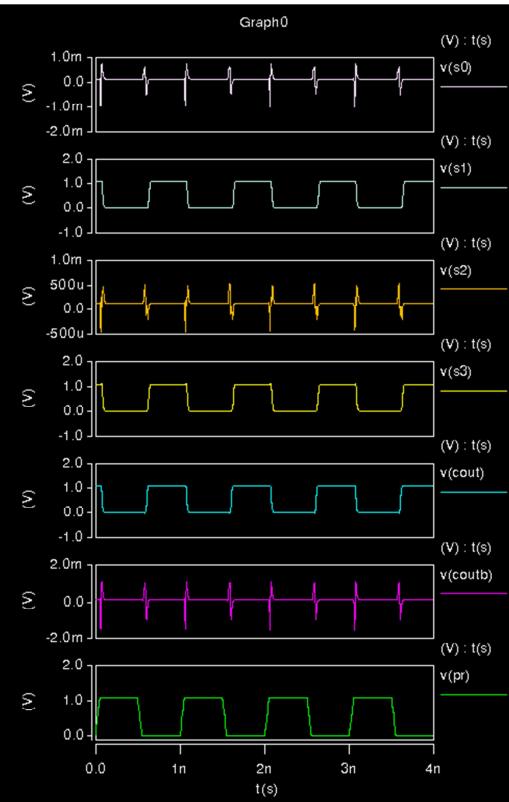
FA2:



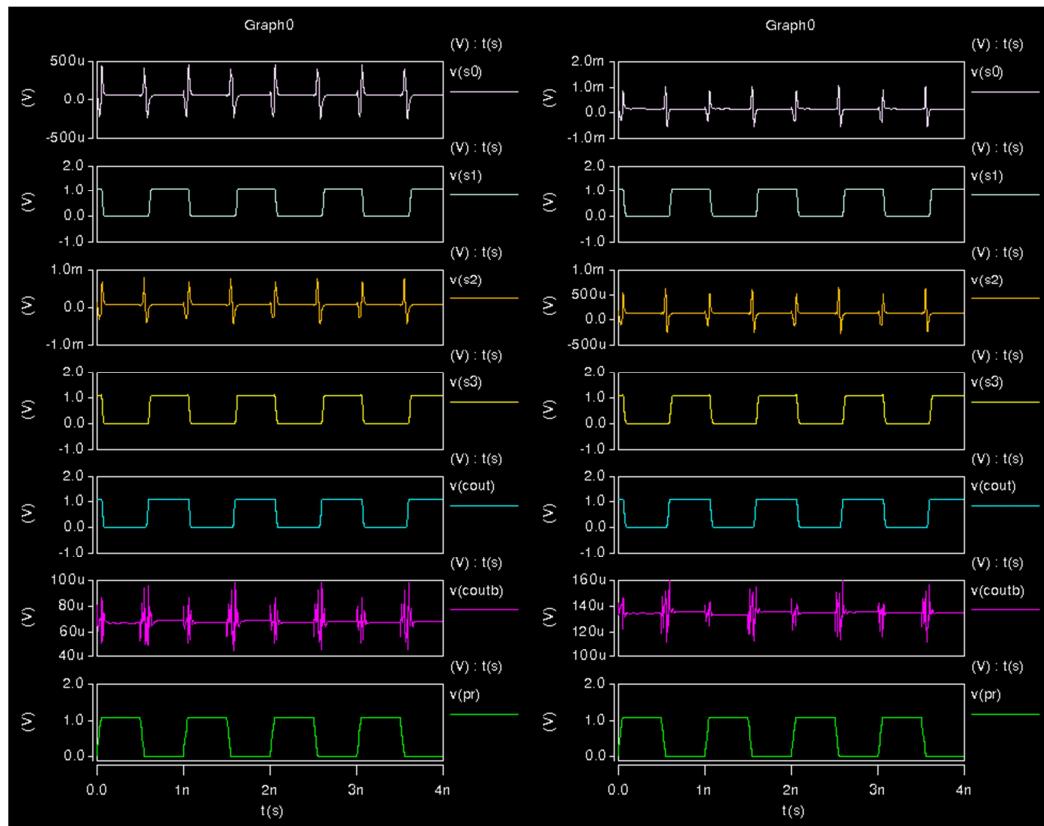
FA3:



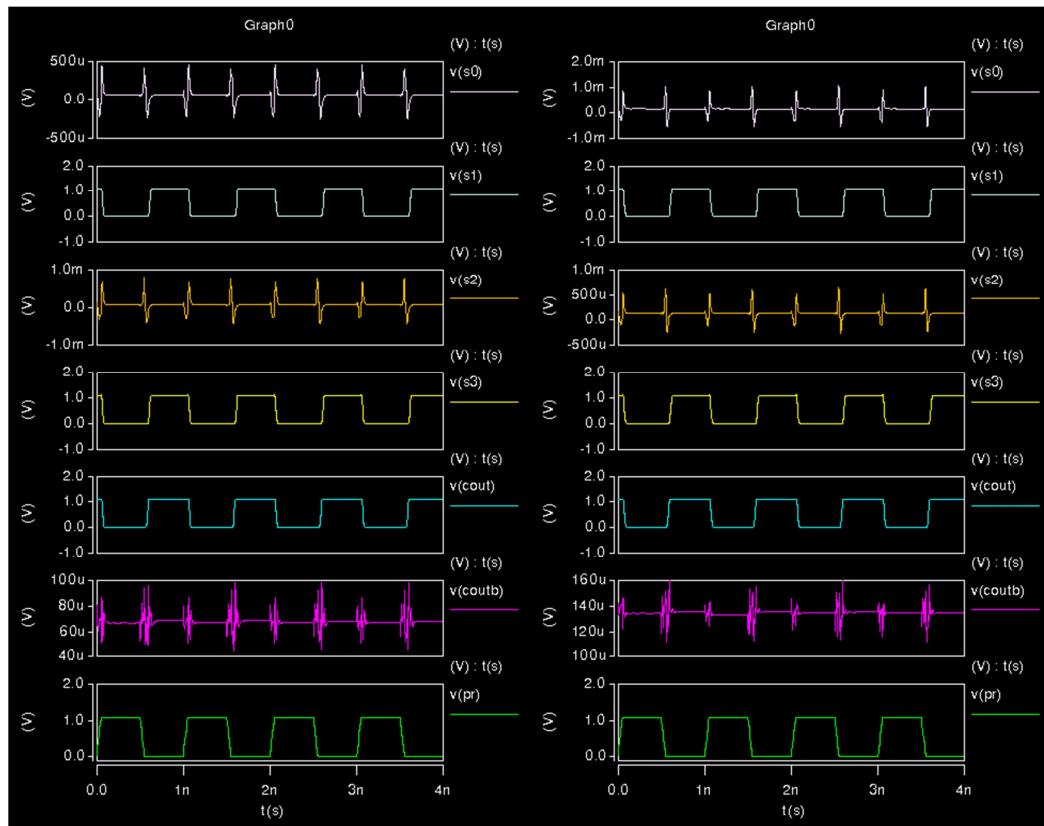
FA4:



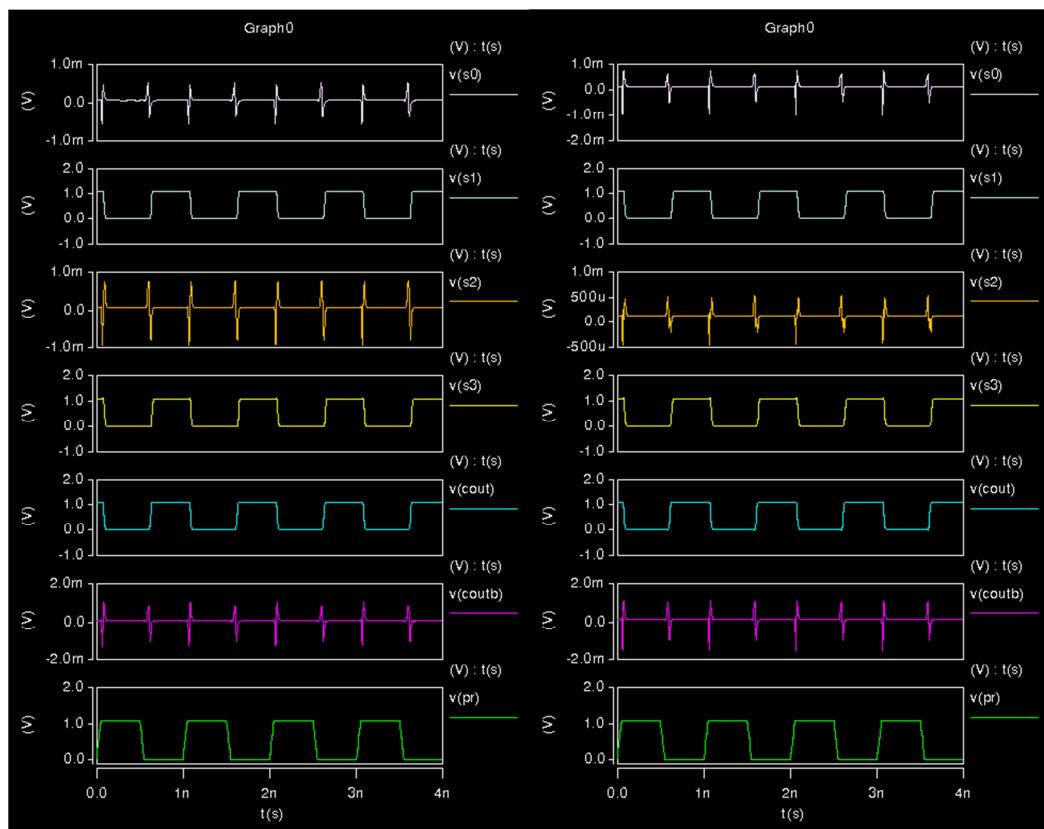
Func1:



Func2:



Func3:



Func4:

