TCP Offload Engine PoC Sharing

xu, jia

Sharing

TCP Offload Engine PoC

Xu,Jia

Agenda

- Overall Architecture
- Convertion Flow
- HLS tuning

Introduction

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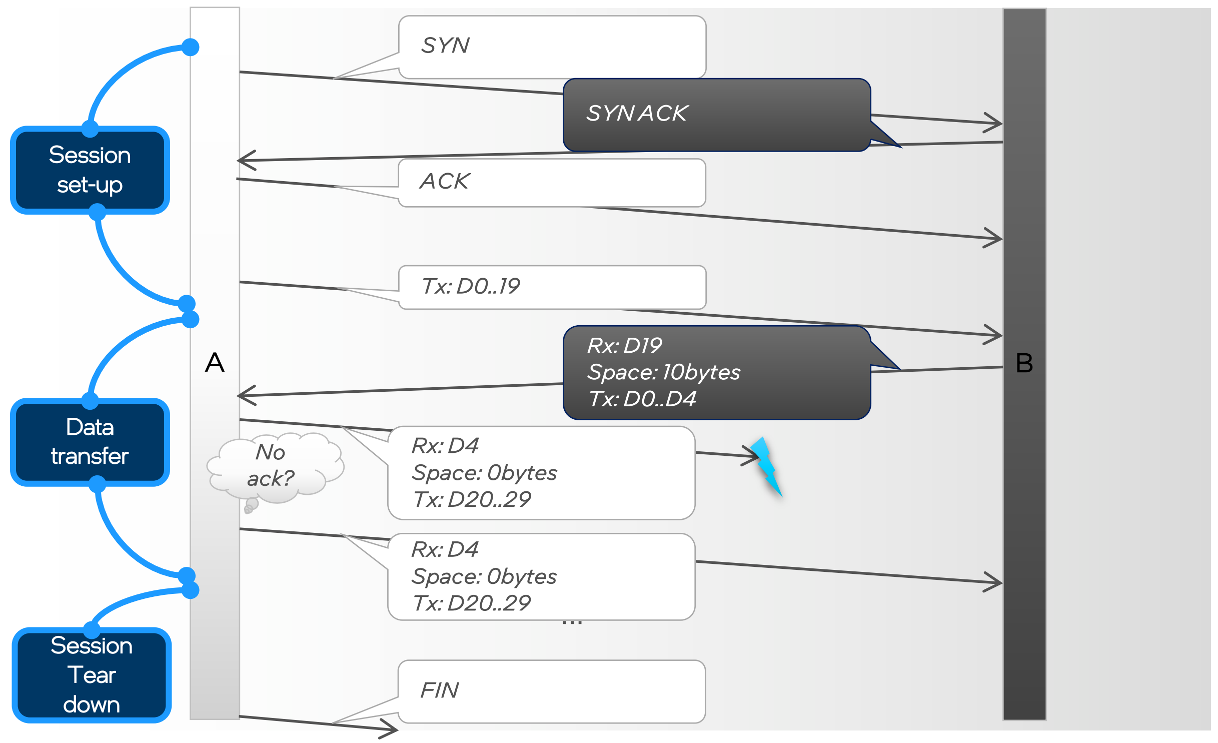
Overall Architecture

Introduction

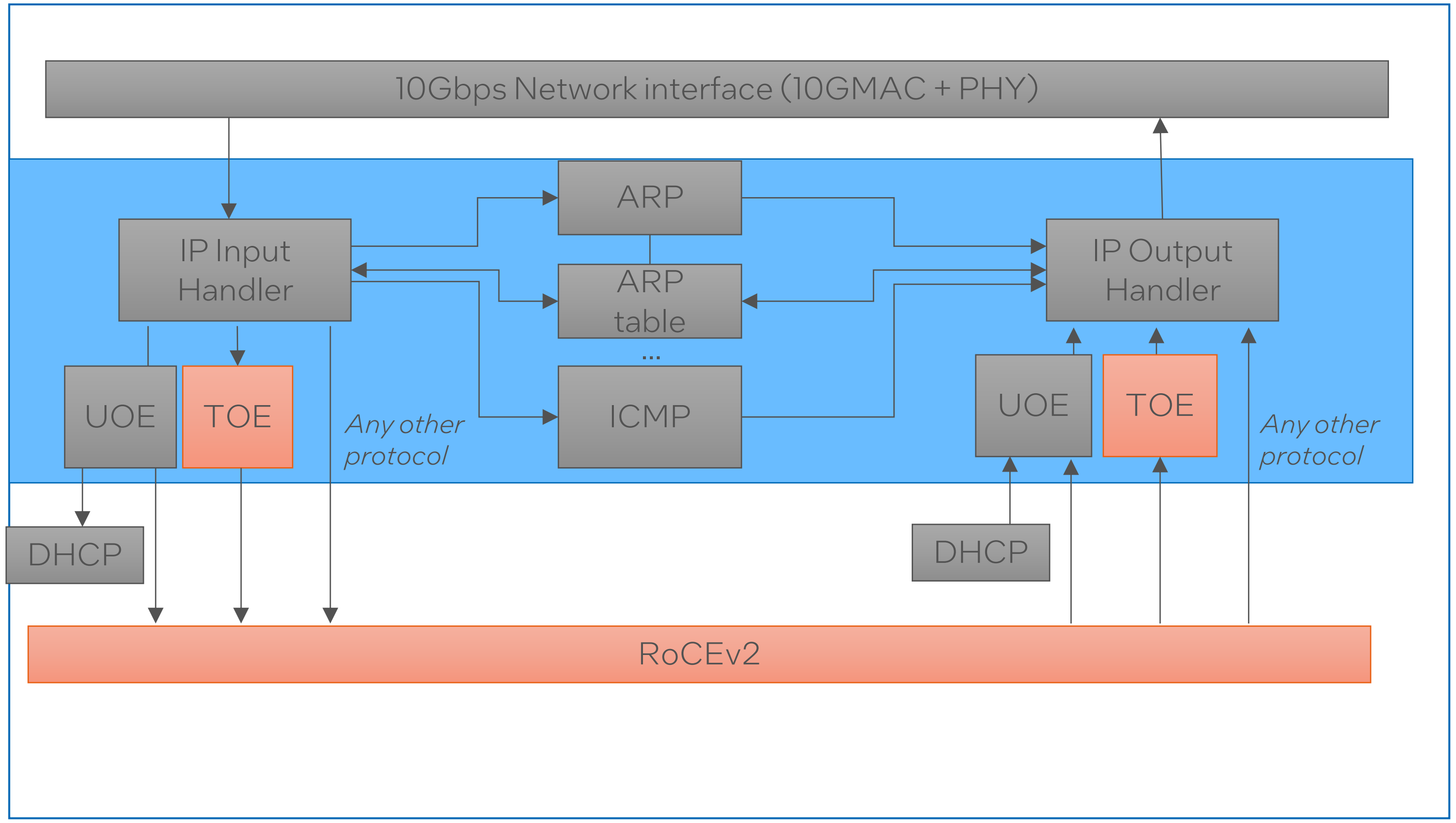


How TCP/IP work

1. Session Setup:
    1. Client sends SYN to server.
    2. Server responds with SYN-ACK.
    3. Client sends ACK, establishing the connection.
2. Data Transfer:
    1. Client and server exchange data using TCP segments.
    2. Sender sends segments; receiver acknowledges them.
3. Session Tear Down:
    1. Either side initiates connection closure with FIN segment.
    2. Receiver acknowledges FIN with ACK.
    3. Receiver also sends FIN.
    4. Sender acknowledges FIN with ACK.
    5. Connection enters TIME_WAIT state.
    6. After TIME_WAIT, connection is closed.

Overall Architecture

Network stack



IP input Heandler:
- MAC Protocol Parsing
- IP checksum verification
- IP Protocol Parsing
- Split Streams

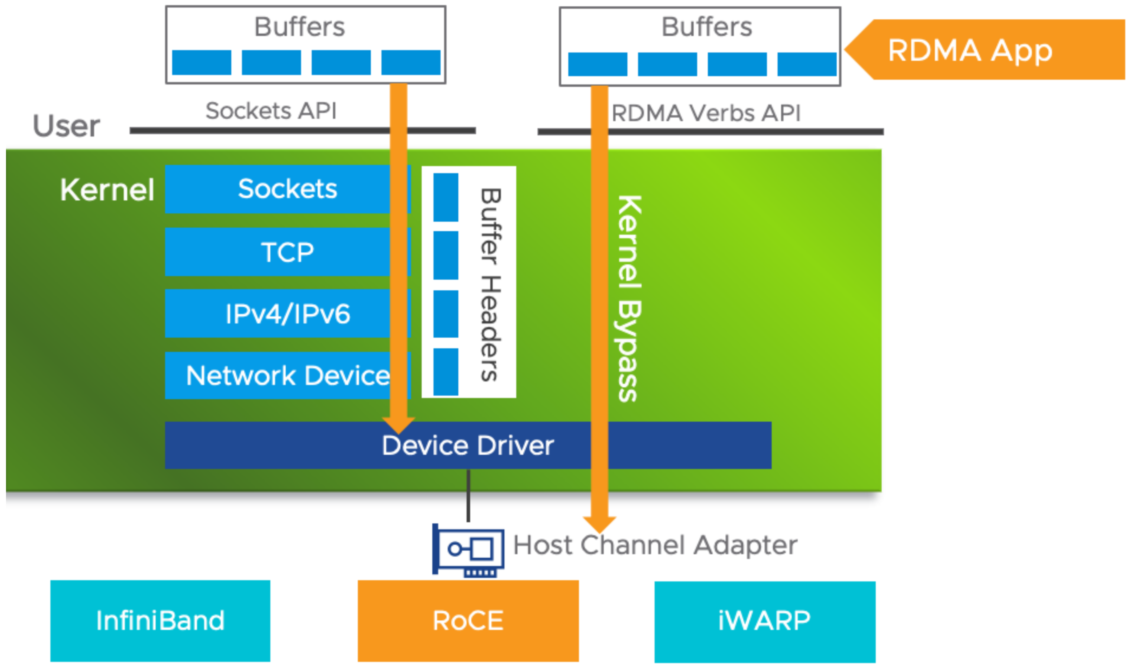
ARP table
- Handling ARP requests and storing MAC-IP tuples

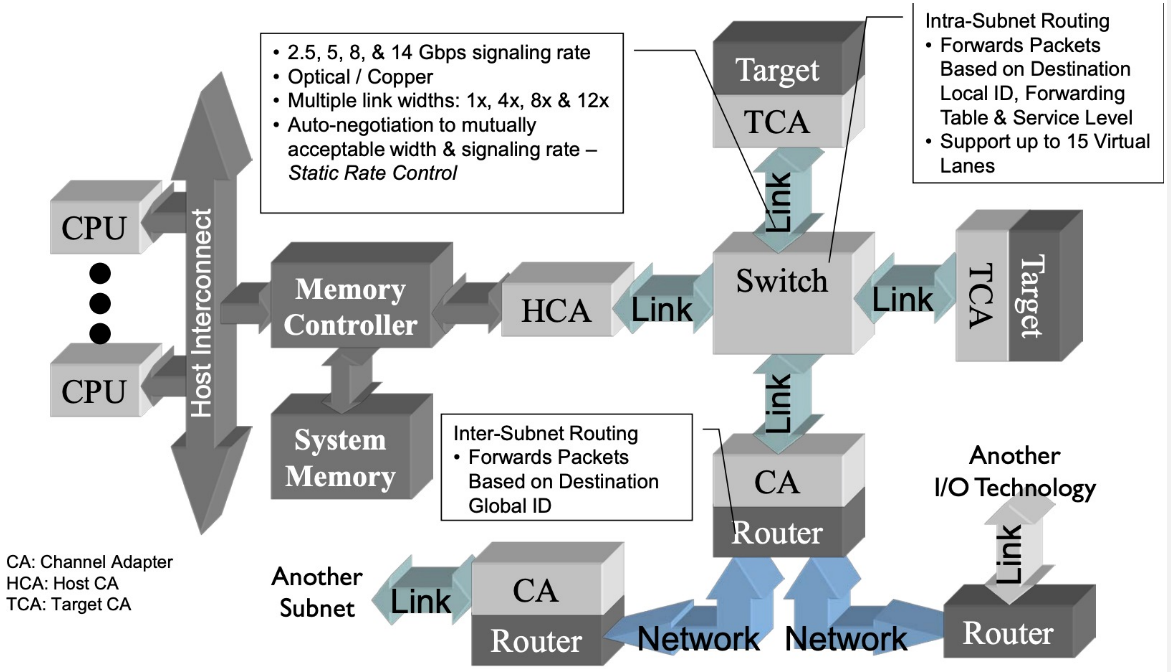
IP output handler
- Constructing MAC frame
- IP checksum computation
- MAC Lookup in ARP Table
- Merge Streams

ICMP
- Handling ARP requests and storing MAC-IP tuples

Overall Architecture

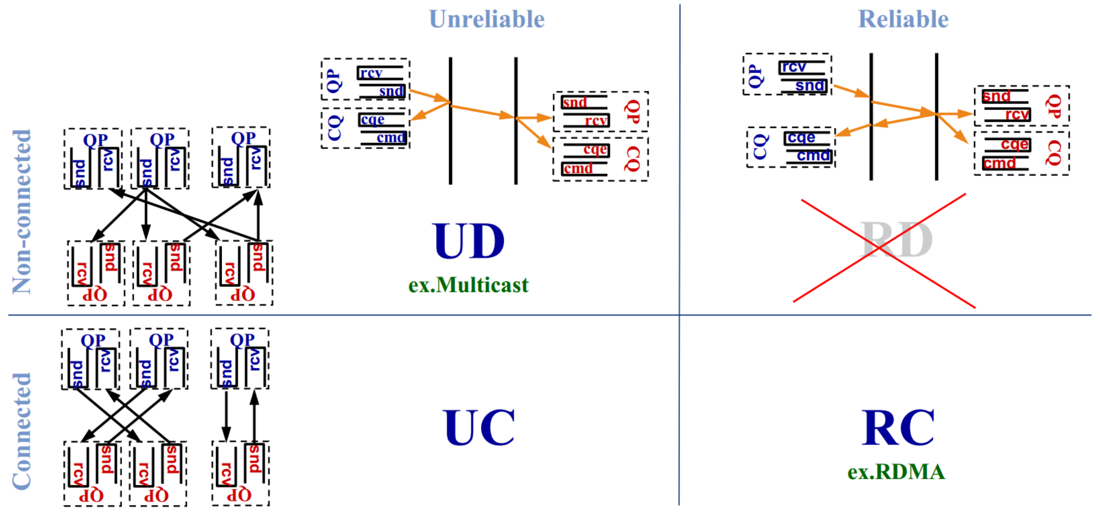
RDMA brief

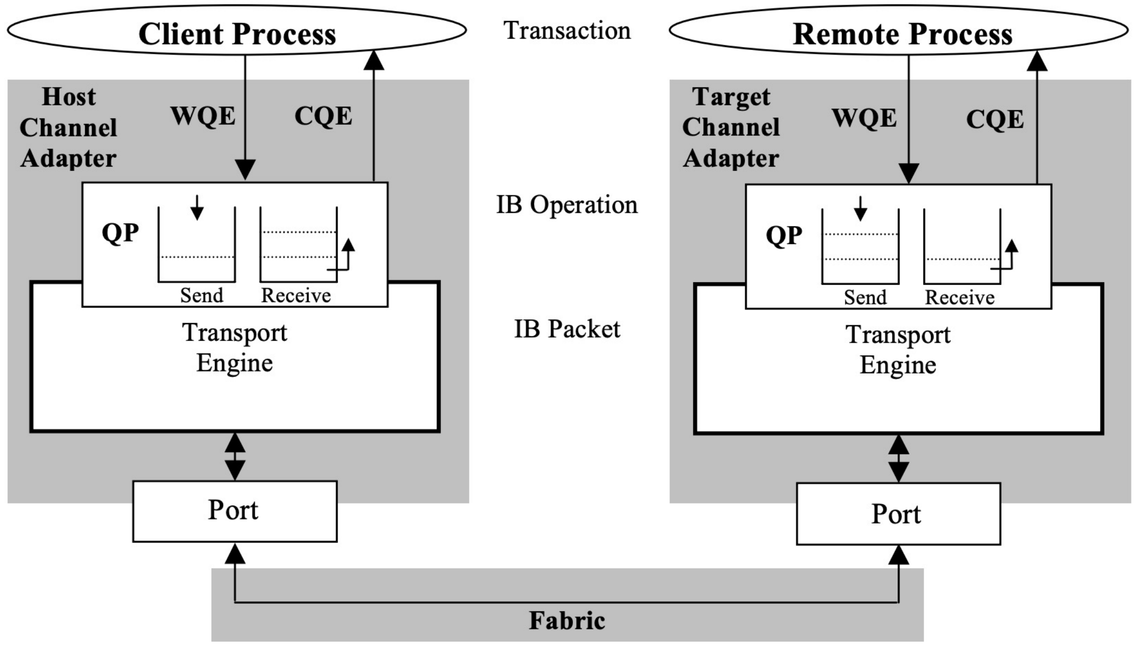


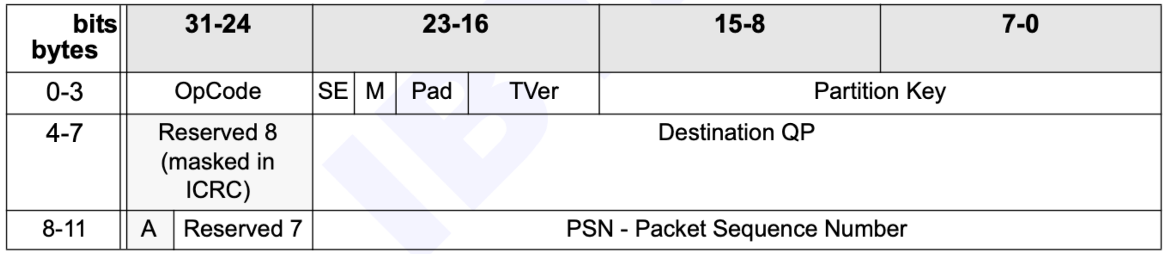

• 2.5, 5, 8, & 14 Gbps signaling rate
• Optical / Copper
• Multiple link widths: 1x, 4x, 8x & 12x
• Auto-negotiation to mutually acceptable width & signaling rate – Static Rate Control
Intra-Subnet Routing
• Forwards Packets Based on Destination Local ID, Forwarding Table & Service Level
• Support up to 15 Virtual Lanes
CPU
CPU
Host Interconnect
Memory Controller
System Memory
HCA
Link
Target
TCA
Link
Switch
Link
TCA
Target
Link
Inter-Subnet Routing
• Forwards Packets Based on Destination Global ID
CA
Router
Another I/O Technology
Link
CA: Channel Adapter
HCA: Host CA
TCA: Target CA
Another Subnet
Link
CA
Router
Network
Network
Router

Overall Architecture

RDMA brief



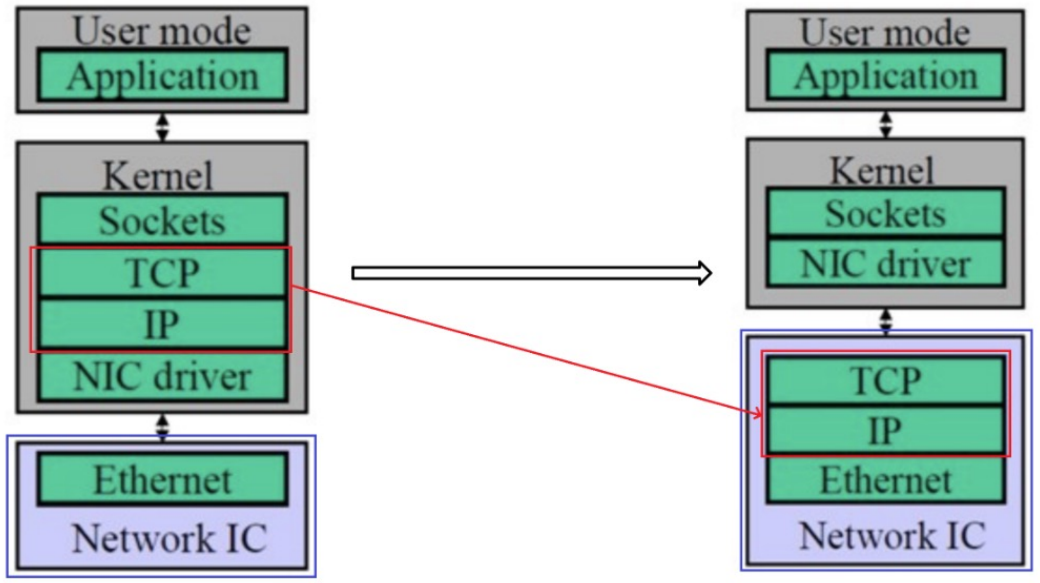


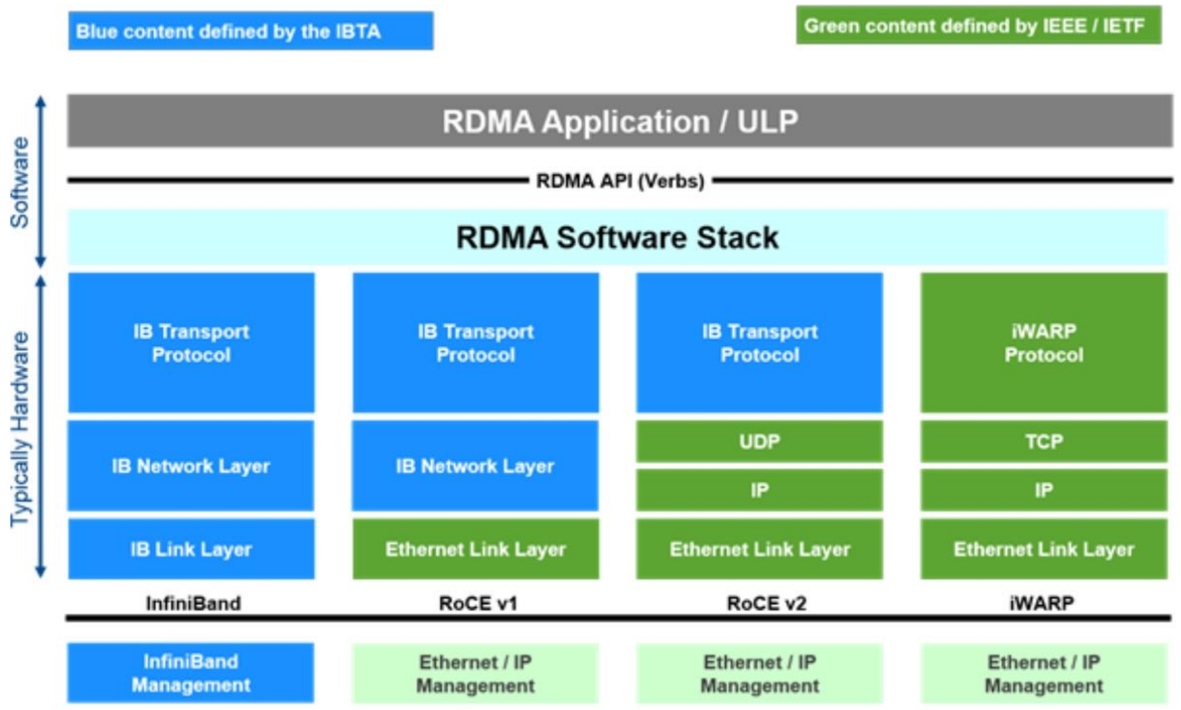


bits / bytes	31-24	23-16	15-8	7-0
0-3	OpCode	SE | M | Pad | TVer	Partition Key	
4-7	Reserved 8 (masked in ICRC)	Destination QP		
8-11	A | Reserved 7	PSN - Packet Sequence Number		

Overall Architecture

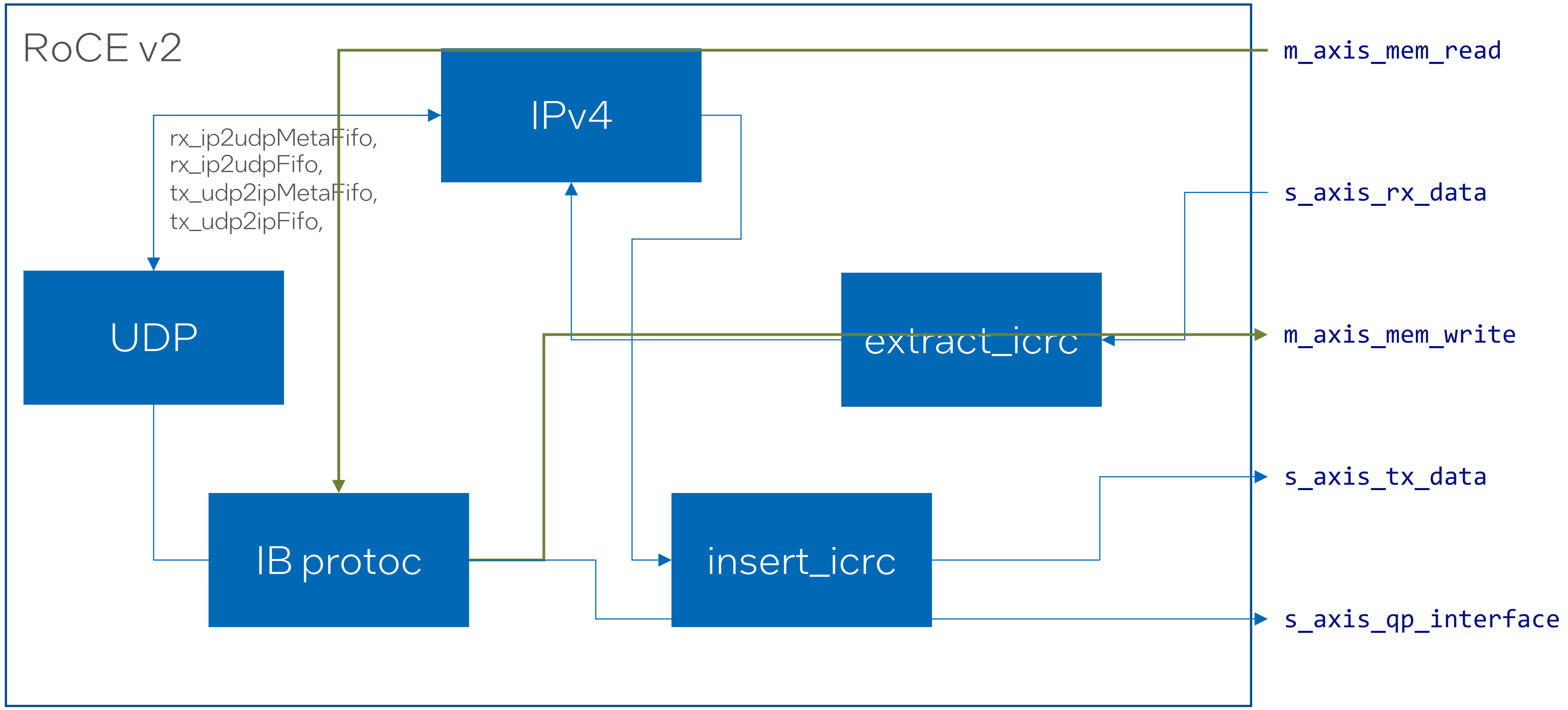
RDMA brief





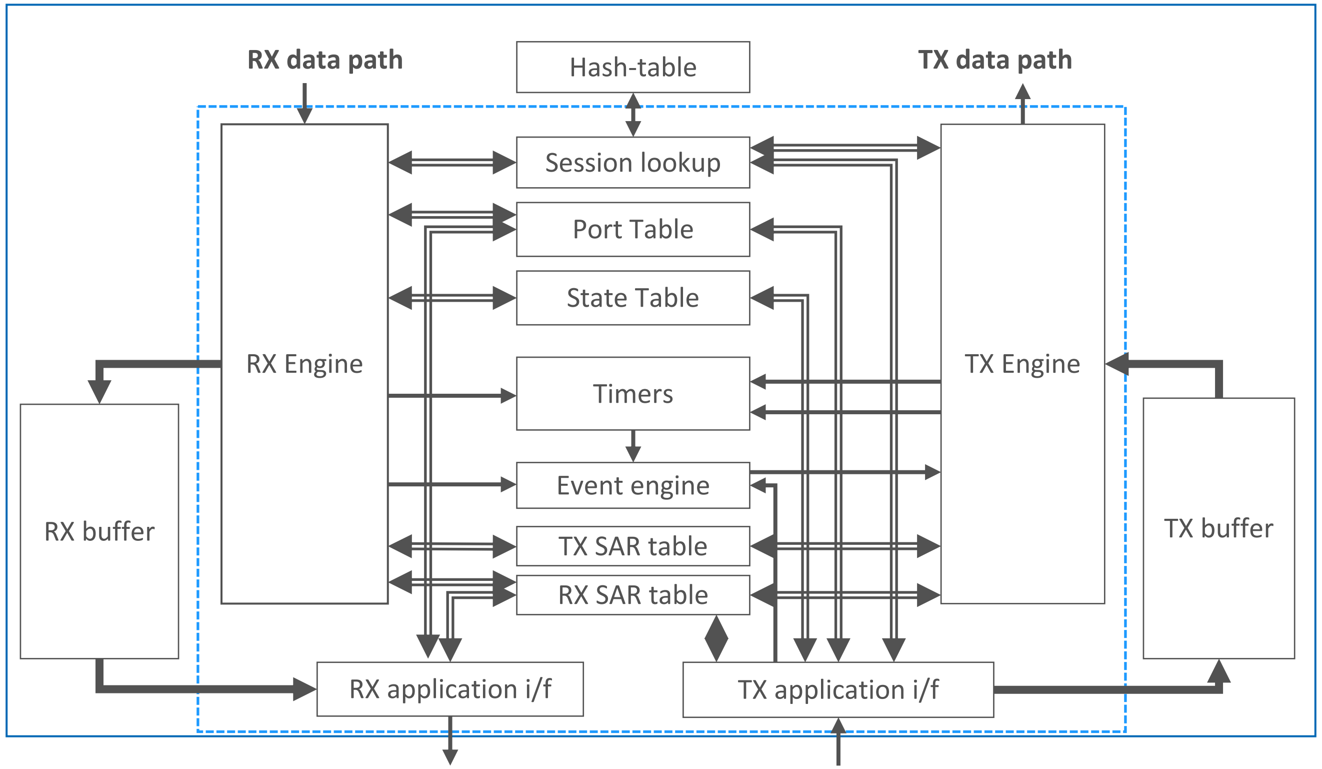
Overall Architecture

RoCE v2 Architecture



Overall Architecture

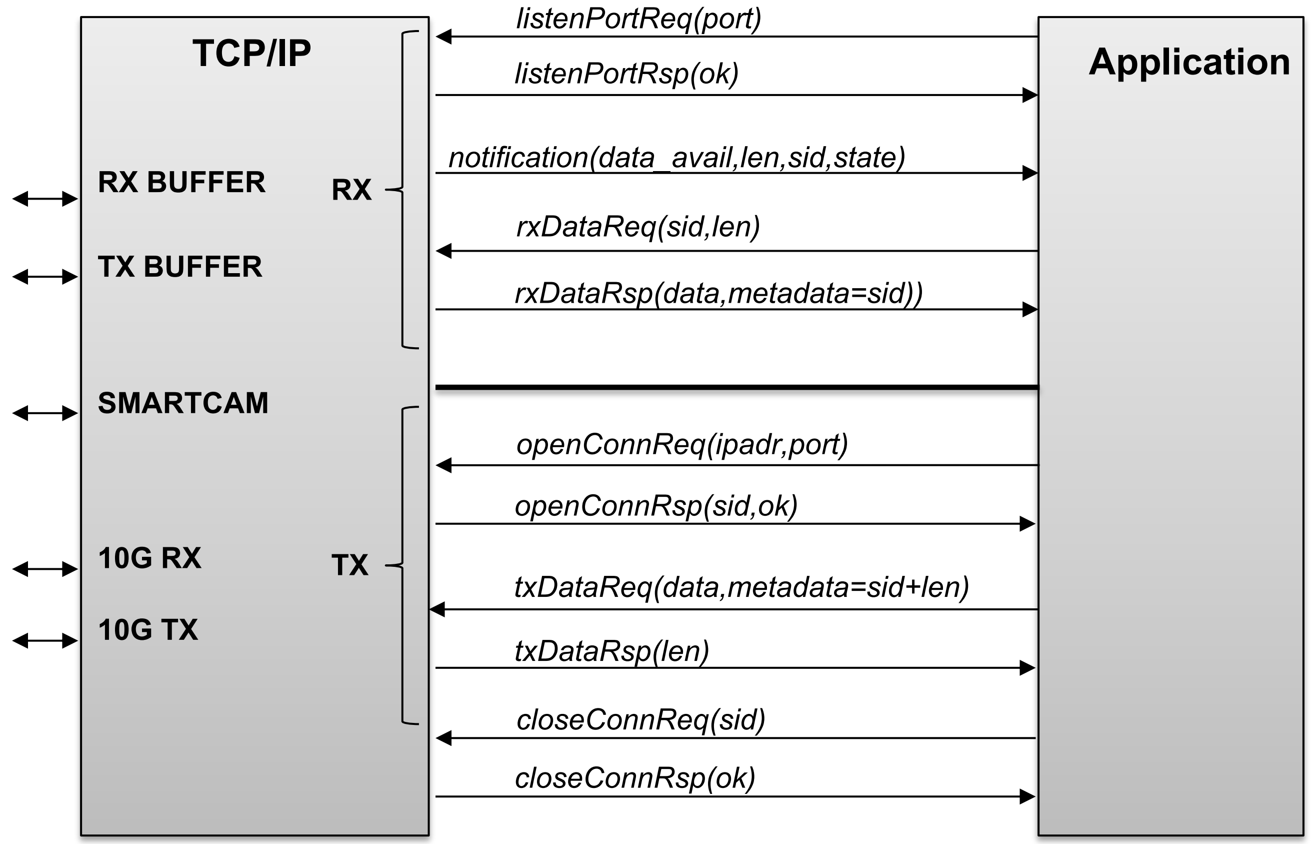
TOE architecture

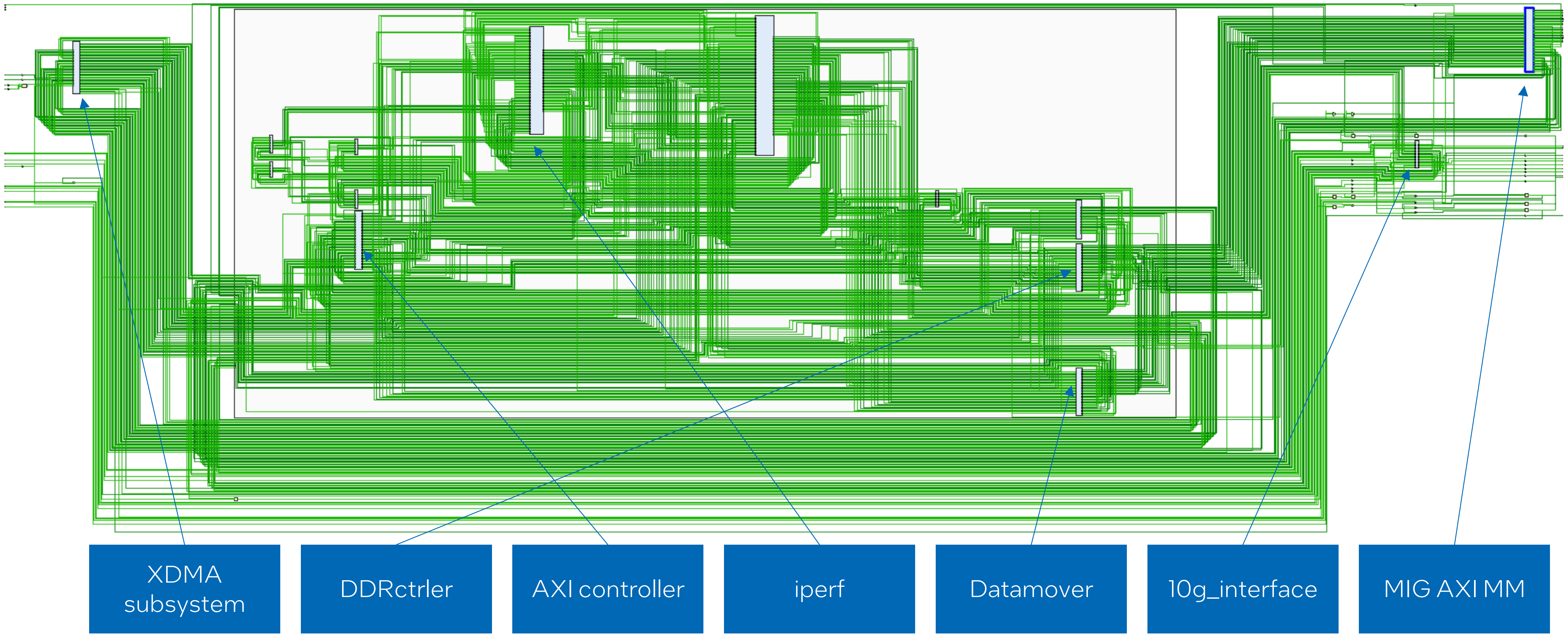


Session lookup - Keeps Track of used and listening IP port
Event engine - Propagates Events through the system
Timers - for retransmission, probing, closing
State Table - Stores the state of each session: CLOSED, SYN-RECV, SYN-SENT, ESTABLISHED….
SAR Tables - storing the information of the TCP receive & send window
TX buffer - To support 10K sessions data is buffered in DDR memory (1.3Gbyte)
RX buffer – using streams.

Overall Architecture

TOE architecture




XDMA subsystem
DDRctrler
AXI controller
iperf
Datamover
10g_interface
MIG AXI MM

Overall Architecture

Performance

Latency / Line of Code

- **Latency (1B payload):**
  - TCP Offload Engine:
    - Rx path: 1.1µs
    - Tx path: 0.8 µs
  - UDP Offload Engine:
    - Rx path: 118 ns
    - Tx path: 92.4 ns
- **Line of code:**

HLS	IP Handler	ARP Server	MAC/IP Encoder	ICMP Server	TOE non-OOO	TOE OOO	UOE	Total
LoC	1592	462	370	534	5985	6441	736	**10142**

TCP/UDP Offload Resource Use

- **All results are post-synthesis with Vivado 2014.2**

	Network Interface	Memory Interface	TCP/IP Stack	Total	Available on V7690T
FF	5581	57637	28713	**95873 11.1%**	**866400 100%**
LUT	5321	43591	28706	**81884 18.9%**	**433200 100%**
BRAM	8	36	441	**471 32.0%**	**1470 100%**

Breakdown (TCP/IP)

	IP Handler	ARP Server	ARP Smart CAM	MAC/IP Encode	ICMP Server	DHCP Client	Session Smart CAM	TOE non-OOO	TOE OOO	UOE
FF	1119	1251	1907	721	1568	505	2065	15504	17638	1939
LUT	1036	607	1653	566	1573	468	2112	14897	18698	1993
BRAM	3	6	42.5	9	12	0	57.5	250.5	304	16

HLS design

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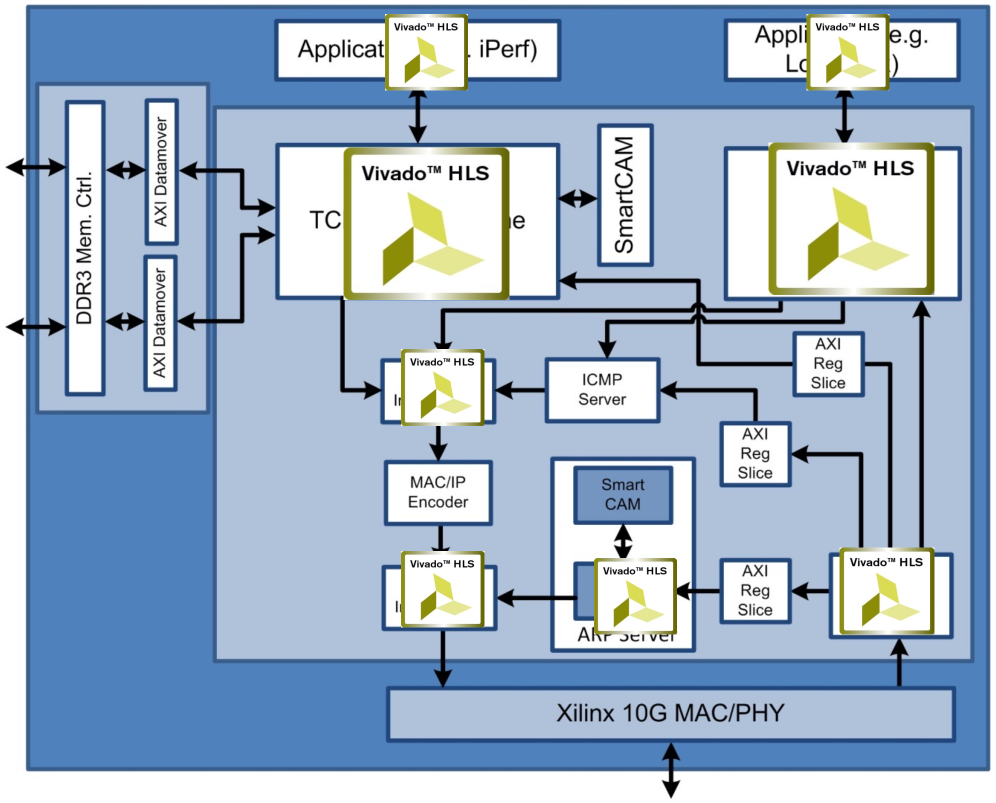
HLS design

components



```
├── constraints
├── hdl
│   ├── 7series
│   │   ├── adm7v3
│   │   └── vc709
│   │       └── clock_control
│   ├── common
├── hls
│   ├── arp_server
│   ├── arp_server_subnet
│   ├── dhcp_client
│   ├── echo_server_application
│   ├── ethernet
│   ├── ethernet_frame_padding
│   ├── hash_table
│   ├── ib_transport_protocol
│   │   ├── multi_queue
│   │   └── retransmitter
│   ├── icmp_server
│   ├── iperf
│   ├── iperf_client
│   ├── iperf_udp
│   ├── ip_handler
│   ├── ipv4
│   ├── ipv6
│   ├── mac_ip_encode
│   ├── rocev2
│   ├── toe
│   │   ├── ack_delay,close_timer
│   │   ├── event_engine
│   │   ├── port_table
│   │   ├── probe_timer
│   │   ├── retransmit_timer
│   │   ├── rx_app_stream_if
│   │   ├── rx_sar_table
│   │   ├── session_lookup_controller
│   │   ├── state_table
│   │   ├── tx_app_if,rx_app_if
│   │   ├── tx_app_interface
│   │   ├── tx_app_stream_if
│   │   ├── tx_engine,rx_engine
│   │   └── tx_sar_table
│   ├── udp
└── ip
```

HLS design

Convertion flow

Arbitry precision integer.

1. In the search bar, type the following regular expression:
2. type ap_uint<([^>]+)>
3. in the replace bar type:
4. type ac_int<$1, false>

ap_int assignment.

1. for RHS
a) in search bar: = ([a-z . _]+)\(([^,]+),\s+([^\)]+)\);
b) in replace bar: = $1.template slc<($2) - ($3) + 1>($3);
2. for LHS
a) in search bar: ([a-z . _]+)\(([^,]+),\s*([^\)]+)\)\s+= ([^;]+);
b) in replace bar: $1.set_slc($3, $4);

HLS design

Convertion flow

intel HLS

ihc::stream_in
ihc::stream_out

Function API	Description
T read()	Blocking read call to be used from within the component
T tryRead(bool &success)	Non-blocking read call to be used from within the component. The success bool is set to true if the read was valid. That is, the Avalon® - ST valid signal was high when the component tried to read from the stream.The emulation model of tryRead() is not cycle-accurate, so the behavior of tryRead() might differ between emulation and simulation.

vivado HLS

hls::stream

```
func1()
{
  while(!s.empty()) {
  s.read();
  }
}
func1()
{
  while(!tlast) {
    s1.read()
  }
}
```

HLS design

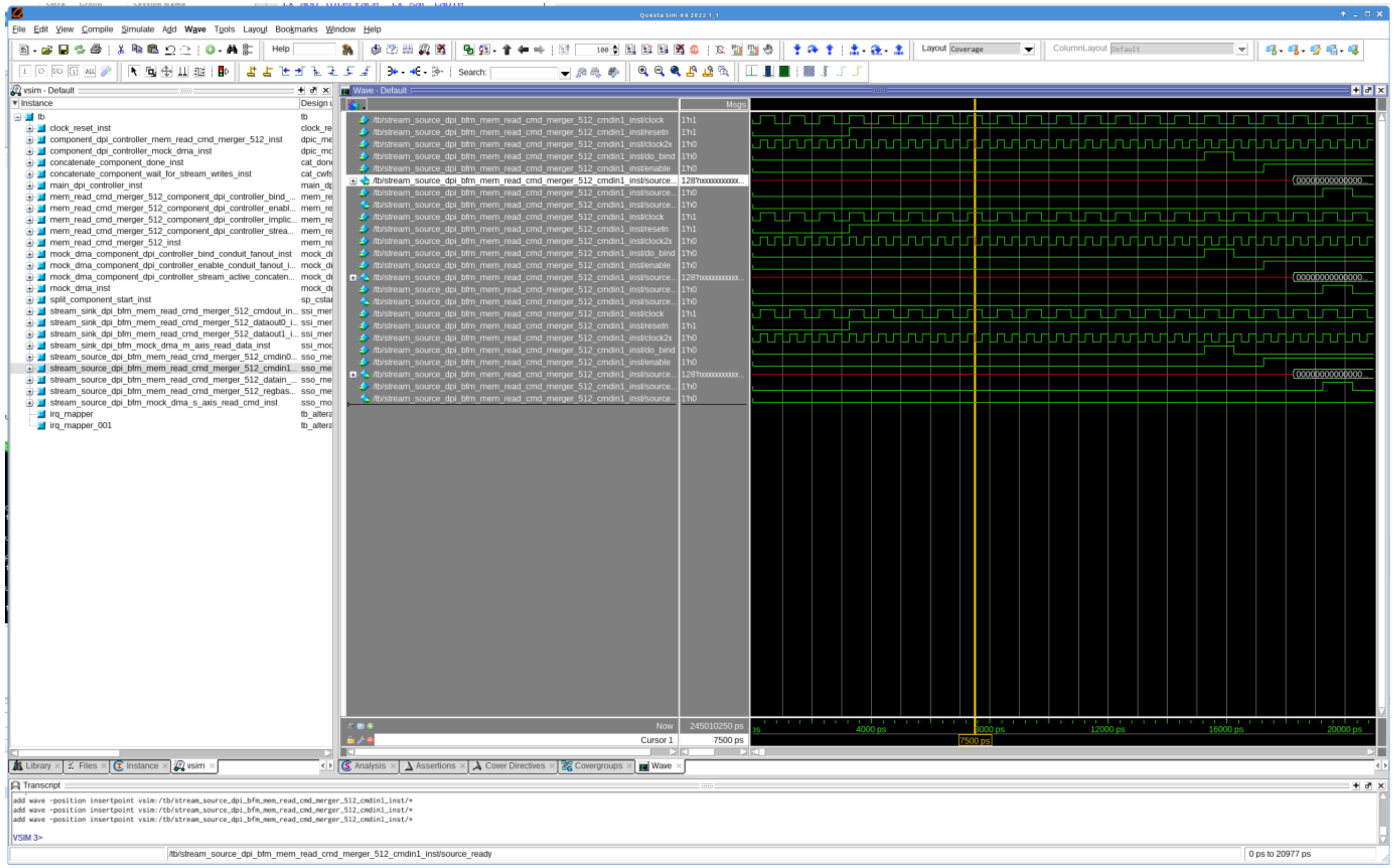
```
template <class PipeName, class T, int depth>
class hls_stream
{
private:
                bool valid, wr_buffer_full;
                T latest_data,  wr_buffer;
                ihc::pipe<PipeName, T, depth> member_pipe;
public:
                hls_stream(){
    valid = 0;
    wr_buffer_full = 0;
  }
  bool empty()
  {
    bool empty = !valid;
    return empty;

  }
  void pulse(){
    if(valid == 0)
      latest_data = member_pipe.read(valid);
  }
  T read()
  {
    valid = 0;
    return latest_data;
  }
  void flush(){
    if(wr_buffer_full){
      bool succ = 0;
      member_pipe.write(wr_buffer, succ);
      if (succ)
      {
        wr_buffer_full = 0;
      }else{
        wr_buffer_full = 1;
      }

    }
  }
  bool full(){
    return wr_buffer_full;
  }

  bool write(T data)
  {
    if (!wr_buffer_full)
    {
      wr_buffer_full = true;
      wr_buffer = data;
      return true;
    }else{
      return false;
    }

  }
};
```

HLS tuning

dEBUG

HLS tuning

Debug - simulation



```
vsim - Default
Instance                                                              Design unit
tb                                                                    tb
  clock_reset_inst                                                    clock_re
  component_dpi_controller_mem_read_cmd_merger_512_inst               dpic_me
  component_dpi_controller_mock_dma_inst                              dpic_mc
  concatenate_component_done_inst                                     cat_done
  concatenate_component_wait_for_stream_writes_inst                   cat_cwfs
  main_dpi_controller_inst                                            main_dp
  mem_read_cmd_merger_512_component_dpi_controller_bind_...           mem_re
  mem_read_cmd_merger_512_component_dpi_controller_enabl...           mem_re
  mem_read_cmd_merger_512_component_dpi_controller_implic...          mem_re
  mem_read_cmd_merger_512_component_dpi_controller_strea...           mem_re
  mem_read_cmd_merger_512_inst                                        mem_re
  mock_dma_component_dpi_controller_bind_conduit_fanout_inst          mock_di
  mock_dma_component_dpi_controller_enable_conduit_fanout_i...        mock_di
  mock_dma_component_dpi_controller_stream_active_concaten...         mock_di
  mock_dma_inst                                                       mock_di
  split_component_start_inst                                          sp_cstar
  stream_sink_dpi_bfm_mem_read_cmd_merger_512_cmdout_in...            ssi_mer
  stream_sink_dpi_bfm_mem_read_cmd_merger_512_dataout0_i...           ssi_mer
  stream_sink_dpi_bfm_mem_read_cmd_merger_512_dataout1_i...           ssi_mer
  stream_sink_dpi_bfm_mock_dma_m_axis_read_data_inst                  ssi_moc
  stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin0...             sso_me
  stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1...             sso_me
  stream_source_dpi_bfm_mem_read_cmd_merger_512_datain_...            sso_me
  stream_source_dpi_bfm_mem_read_cmd_merger_512_regbas...             sso_me
  stream_source_dpi_bfm_mock_dma_s_axis_read_cmd_inst                 sso_mo
  irq_mapper                                                          tb_altera
  irq_mapper_001                                                      tb_altera
```

```
Wave - Default
                                                                        Msgs
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/clock     1'h1
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/resetn    1'h1
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/clock2x   1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/do_bind   1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/enable    1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/source... 128'hxxxxxxxxxx...
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/source... 1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/source... 1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/clock     1'h1
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/resetn    1'h1
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/clock2x   1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/do_bind   1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/enable    1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/source... 128'hxxxxxxxxxx...
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/source... 1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/source... 1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/clock     1'h1
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/resetn    1'h1
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/clock2x   1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/do_bind   1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/enable    1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/source... 128'hxxxxxxxxxx...
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/source... 1'h0
/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/source... 1'h0

Now       245010250 ps
Cursor 1  7500 ps
```

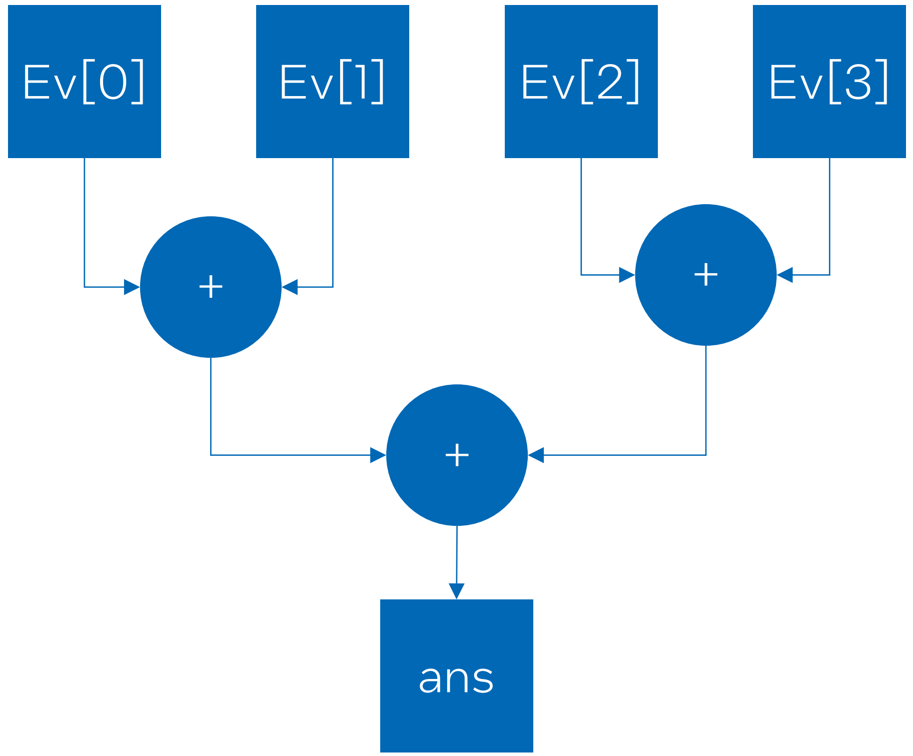
```
Transcript
add wave -position insertpoint vsim:/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/*
add wave -position insertpoint vsim:/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/*
add wave -position insertpoint vsim:/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/*

VSIM 3>
```

/tb/stream_source_dpi_bfm_mem_read_cmd_merger_512_cmdin1_inst/source_ready

HLS tuning

Optimize ii

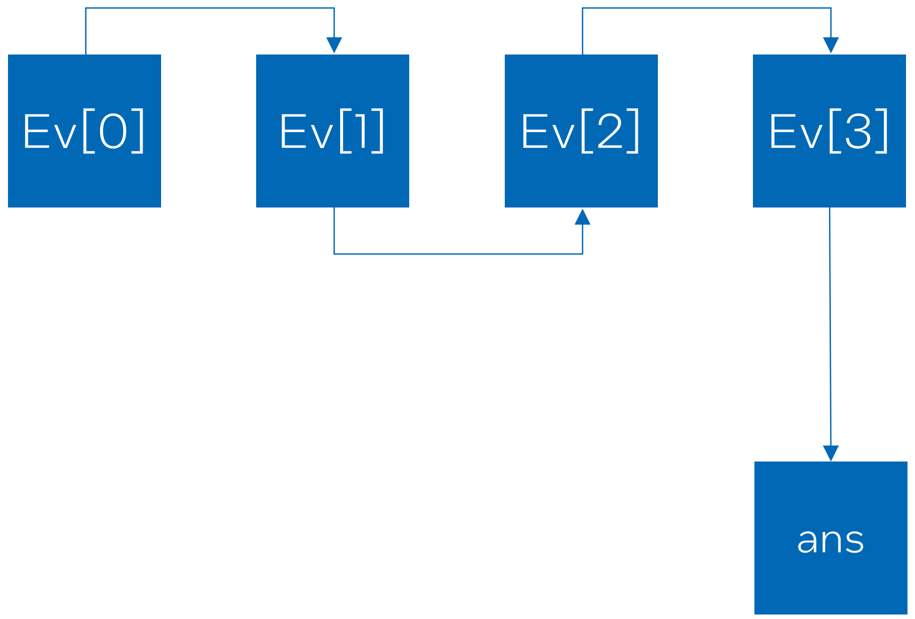
```
switch (state)
{
case RECEIVE:
    ev = input.tryRead(success);
    result = 0;
    #pragma unroll
    for(int i = 0; i < N; i++){
        result += ev[i];
    }
    state = PROCESS;
    break;
default:
    break;
```



HLS tuning

Optimize ii

```
switch (state)
{
case RECEIVE:
    ev = input.tryRead(success);
    result = 0;
    result = ev[0];
    state = PROCESS;
    counter = N - 1;
    break;
case PROCESS:
    #pragma unroll
    for(int i = 0; i < N-1; i++){
        ev[i] = ev[i+1];
    }
    result += ev[0];
    counter --;
    if(counter == 0) state = RECEIVE;
```



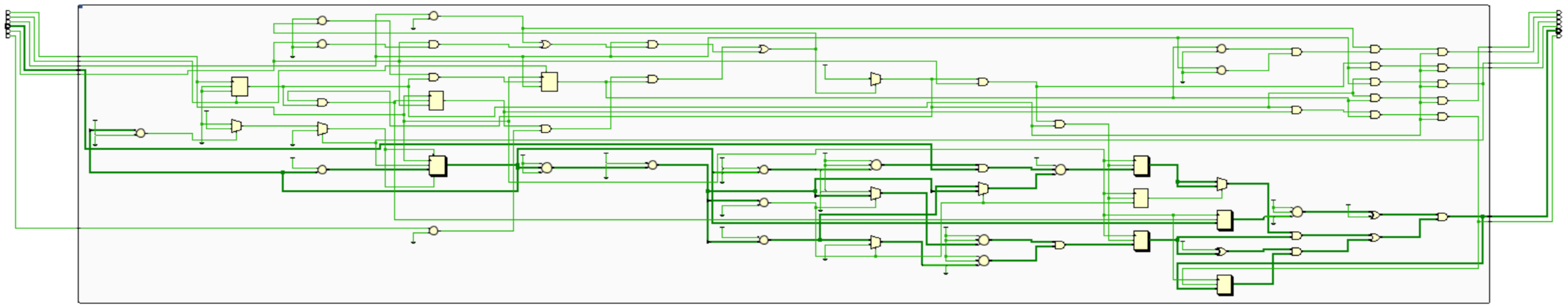
HLS tuning

example

```
static ap_uint<32> ad_pointer = 0;
    //static ap_uint<4> ad_readCounter = 0;
    ap_uint<32> ev;
    static int offset = 1;
    if (!input.empty())
    {
        ev = input.read();

        ad_pointer(WIDTH-1, WIDTH - (offset*8)) = ev(offset*8-1, 0);
        ad_pointer(WIDTH - (offset*8) -1, 0) = 0;

        output.write(ad_pointer);
    }
    if(offset < 4) offset++;
    else offset = 1;
```

HLS tuning

example



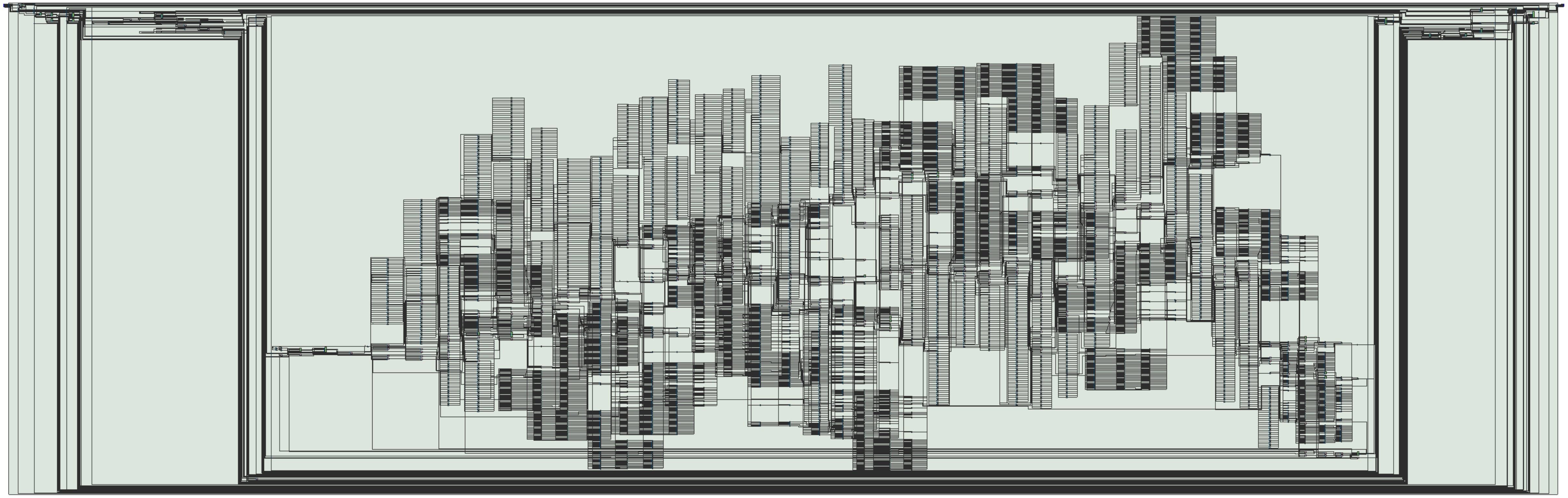
HLS tuning

example

```
static ac_int<32, false>   ad_pointer = 0;
//static ac_int<4, false>   ad_readCounter = 0;
ac_int<32, false> ev;

static int offset = 1;
bool success;
ev = input.tryRead(success);
if (success)
{
    #pragma unroll
    #pragma ivdep
    for (int i = 0; i < WIDTH; i++)
    {
        if(i < offset*8) ad_pointer[i + WIDTH - (offset*8)] = ev[i];
        else ad_pointer[i] = 0;
    }

    output.write(ad_pointer);
}
if(offset < 4) offset++;
else offset = 1;
```

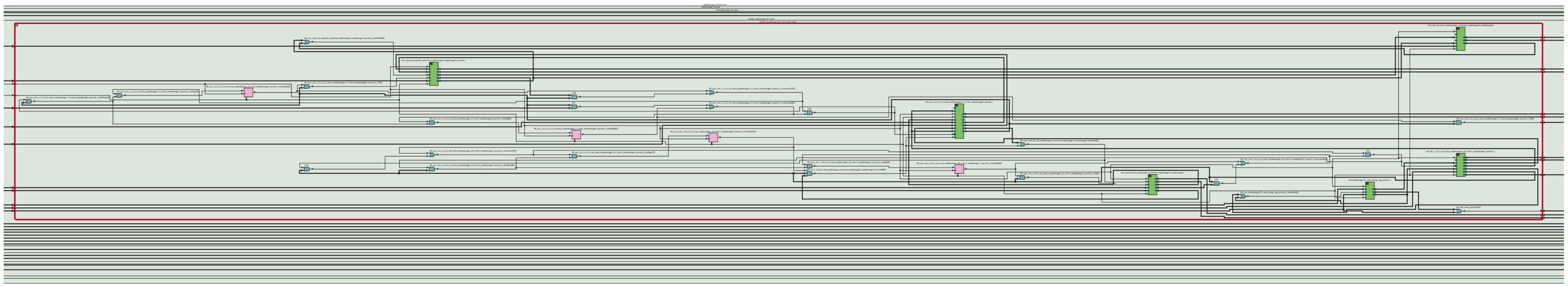
HLS tuning

example



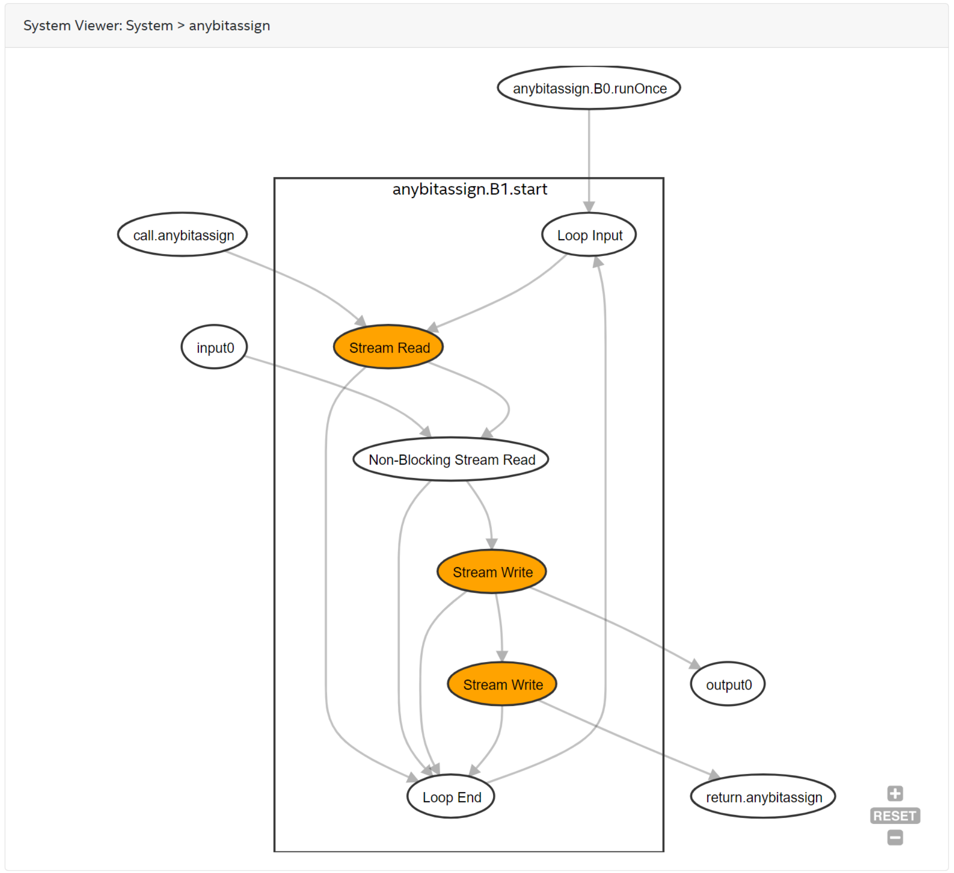
HLS tuning

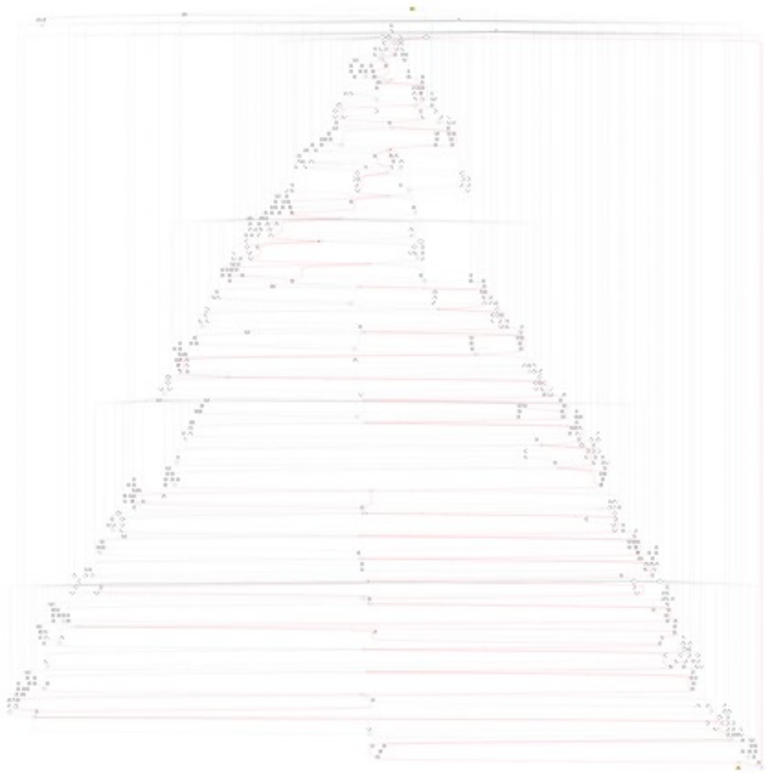
example



HLS tuning

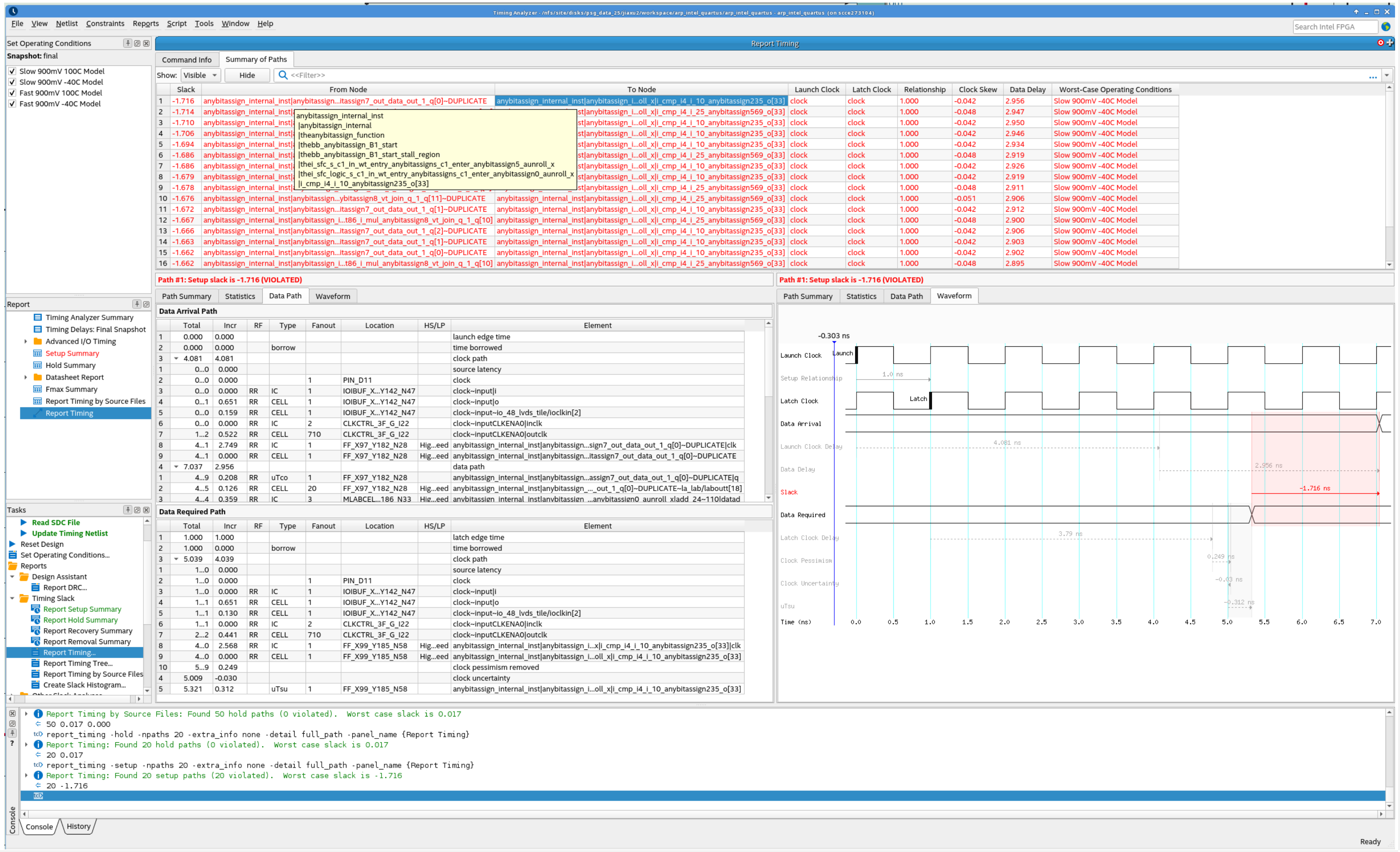
example





HLS tuning

Frequency



Path #1: Setup slack is -1.716 (VIOLATED)

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay	Worst-Case Operating Conditions
1	-1.716	anybitassign_internal_inst|anybitassign...itassign7_out_data_out_1_q[0]~DUPLICATE	anybitassign_internal_inst|anybitassign_i...oll_x|i_cmp_i4_i_10_anybitassign235_o[33]	clock	clock	1.000	-0.042	2.956	Slow 900mV -40C Model
2	-1.714	anybitassign_internal_inst|	st|anybitassign_i...oll_x|i_cmp_i4_i_25_anybitassign569_o[33]	clock	clock	1.000	-0.048	2.947	Slow 900mV -40C Model
3	-1.710	anybitassign_internal_inst|	st|anybitassign_i...oll_x|i_cmp_i4_i_10_anybitassign235_o[33]	clock	clock	1.000	-0.042	2.950	Slow 900mV -40C Model
4	-1.706	anybitassign_internal_inst|	st|anybitassign_i...oll_x|i_cmp_i4_i_10_anybitassign235_o[33]	clock	clock	1.000	-0.042	2.946	Slow 900mV -40C Model
5	-1.694	anybitassign_internal_inst|	st|anybitassign_i...oll_x|i_cmp_i4_i_10_anybitassign235_o[33]	clock	clock	1.000	-0.042	2.934	Slow 900mV -40C Model
6	-1.686	anybitassign_internal_inst|	st|anybitassign_i...oll_x|i_cmp_i4_i_25_anybitassign569_o[33]	clock	clock	1.000	-0.048	2.919	Slow 900mV -40C Model
7	-1.686	anybitassign_internal_inst|	st|anybitassign_i...oll_x|i_cmp_i4_i_10_anybitassign235_o[33]	clock	clock	1.000	-0.042	2.926	Slow 900mV -40C Model
8	-1.679	anybitassign_internal_inst|	st|anybitassign_i...oll_x|i_cmp_i4_i_10_anybitassign235_o[33]	clock	clock	1.000	-0.042	2.919	Slow 900mV -40C Model
9	-1.678	anybitassign_internal_inst|	st|anybitassign_i...oll_x|i_cmp_i4_i_25_anybitassign569_o[33]	clock	clock	1.000	-0.048	2.911	Slow 900mV -40C Model
10	-1.676	anybitassign_internal_inst|anybitassign...ybitassign8_vt_join_q_1_q[11]~DUPLICATE	anybitassign_internal_inst|anybitassign_i...oll_x|i_cmp_i4_i_25_anybitassign569_o[33]	clock	clock	1.000	-0.051	2.906	Slow 900mV -40C Model
11	-1.672	anybitassign_internal_inst|anybitassign...itassign7_out_data_out_1_q[1]~DUPLICATE	anybitassign_internal_inst|anybitassign_i...oll_x|i_cmp_i4_i_10_anybitassign235_o[33]	clock	clock	1.000	-0.042	2.912	Slow 900mV -40C Model
12	-1.667	anybitassign_internal_inst|anybitassign_i...t86_i_mul_anybitassign8_vt_join_q_1_q[10]	anybitassign_internal_inst|anybitassign_i...oll_x|i_cmp_i4_i_25_anybitassign569_o[33]	clock	clock	1.000	-0.048	2.900	Slow 900mV -40C Model
13	-1.666	anybitassign_internal_inst|anybitassign...itassign7_out_data_out_1_q[2]~DUPLICATE	anybitassign_internal_inst|anybitassign_i...oll_x|i_cmp_i4_i_10_anybitassign235_o[33]	clock	clock	1.000	-0.042	2.906	Slow 900mV -40C Model
14	-1.663	anybitassign_internal_inst|anybitassign...itassign7_out_data_out_1_q[1]~DUPLICATE	anybitassign_internal_inst|anybitassign_i...oll_x|i_cmp_i4_i_10_anybitassign235_o[33]	clock	clock	1.000	-0.042	2.903	Slow 900mV -40C Model
15	-1.662	anybitassign_internal_inst|anybitassign...itassign7_out_data_out_1_q[0]~DUPLICATE	anybitassign_internal_inst|anybitassign_i...oll_x|i_cmp_i4_i_10_anybitassign235_o[33]	clock	clock	1.000	-0.042	2.902	Slow 900mV -40C Model
16	-1.662	anybitassign_internal_inst|anybitassign_i...t86_i_mul_anybitassign8_vt_join_q_1_q[10]	anybitassign_internal_inst|anybitassign_i...oll_x|i_cmp_i4_i_25_anybitassign569_o[33]	clock	clock	1.000	-0.048	2.895	Slow 900mV -40C Model

```
anybitassign_internal_inst
 |anybitassign_internal
 |theanybitassign_function
 |thebb_anybitassign_B1_start
 |thebb_anybitassign_B1_start_stall_region
 |thei_sfc_s_c1_in_wt_entry_anybitassigns_c1_enter_anybitassign5_aunroll_x
 |thei_sfc_logic_s_c1_in_wt_entry_anybitassigns_c1_enter_anybitassign0_aunroll_x
 |i_cmp_i4_i_10_anybitassign235_o[33]
```

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	HS/LP	Element
1	0.000	0.000						launch edge time
2	0.000	0.000		borrow				time borrowed
3	4.081	4.081						clock path
1	0...0	0.000						source latency
2	0...0	0.000			1	PIN_D11		clock
3	0...0	0.000	RR	IC	1	IOIBUF_X...Y142_N47		clock~input|i
4	0...1	0.651	RR	CELL	1	IOIBUF_X...Y142_N47		clock~input|o
5	0...0	0.159	RR	CELL	1	IOIBUF_X...Y142_N47		clock~input~io_48_lvds_tile/ioclkin[2]
6	0...0	0.000	RR	IC	2	CLKCTRL_3F_G_I22		clock~inputCLKENA0|inclk
7	1...2	0.522	RR	CELL	710	CLKCTRL_3F_G_I22		clock~inputCLKENA0|outclk
8	4...1	2.749	RR	IC	1	FF_X97_Y182_N28	Hig...eed	anybitassign_internal_inst|anybitassign...sign7_out_data_out_1_q[0]~DUPLICATE|clk
9	4...1	0.000	RR	CELL	1	FF_X97_Y182_N28	Hig...eed	anybitassign_internal_inst|anybitassign...itassign7_out_data_out_1_q[0]~DUPLICATE
4	7.037	2.956						data path
1	4...9	0.208	RR	uTco	1	FF_X97_Y182_N28		anybitassign_internal_inst|anybitassign...assign7_out_data_out_1_q[0]~DUPLICATE|q
2	4...5	0.126	RR	CELL	20	FF_X97_Y182_N28	Hig...eed	anybitassign_internal_inst|anybitassign_..._out_1_q[0]~DUPLICATE~la_lab/laboutt[18]
3	4...4	0.359	RR	IC	3	MLABCEL...186_N33	Hig...eed	anybitassign_internal_inst|anybitassign_...anybitassign0_aunroll_xladd_24~110|datad

Data Required Path

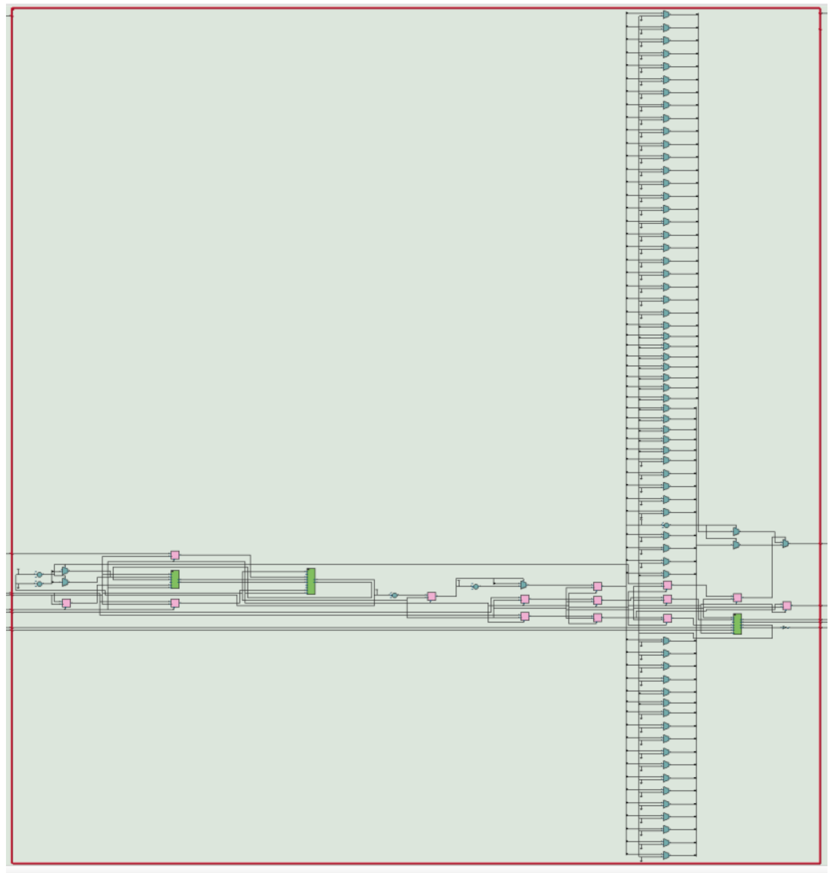
	Total	Incr	RF	Type	Fanout	Location	HS/LP	Element
1	1.000	1.000						latch edge time
2	1.000	0.000		borrow				time borrowed
3	5.039	4.039						clock path
1	1...0	0.000						source latency
2	1...0	0.000			1	PIN_D11		clock
3	1...0	0.000	RR	IC	1	IOIBUF_X...Y142_N47		clock~input|i
4	1...1	0.651	RR	CELL	1	IOIBUF_X...Y142_N47		clock~input|o
5	1...1	0.130	RR	CELL	1	IOIBUF_X...Y142_N47		clock~input~io_48_lvds_tile/ioclkin[2]
6	1...1	0.000	RR	IC	2	CLKCTRL_3F_G_I22		clock~inputCLKENA0|inclk
7	2...2	0.441	RR	CELL	710	CLKCTRL_3F_G_I22		clock~inputCLKENA0|outclk
8	4...0	2.568	RR	IC	1	FF_X99_Y185_N58	Hig...eed	anybitassign_internal_inst|anybitassign_i...x|i_cmp_i4_i_10_anybitassign235_o[33]|clk
9	4...0	0.000	RR	CELL	1	FF_X99_Y185_N58	Hig...eed	anybitassign_internal_inst|anybitassign_i...oll_x|i_cmp_i4_i_10_anybitassign235_o[33]
10	5...9	0.249						clock pessimism removed
4	5.009	-0.030						clock uncertainty
5	5.321	0.312		uTsu	1	FF_X99_Y185_N58		anybitassign_internal_inst|anybitassign_i...oll_x|i_cmp_i4_i_10_anybitassign235_o[33]

```
Report Timing by Source Files: Found 50 hold paths (0 violated).  Worst case slack is 0.017
50 0.017 0.000
tcl> report_timing -hold -npaths 20 -extra_info none -detail full_path -panel_name {Report Timing}
Report Timing: Found 20 hold paths (0 violated).  Worst case slack is 0.017
20 0.017
tcl> report_timing -setup -npaths 20 -extra_info none -detail full_path -panel_name {Report Timing}
Report Timing: Found 20 setup paths (20 violated).  Worst case slack is -1.716
20 -1.716
tcl>
```

HLS tuning

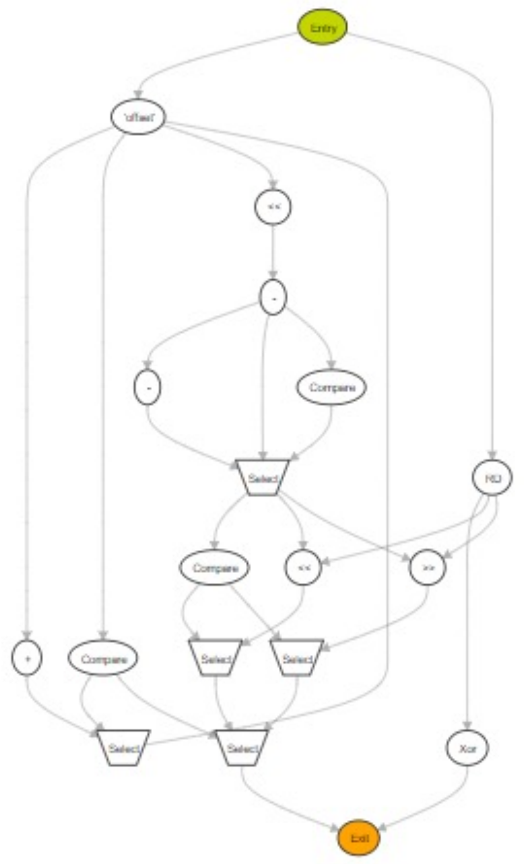
example

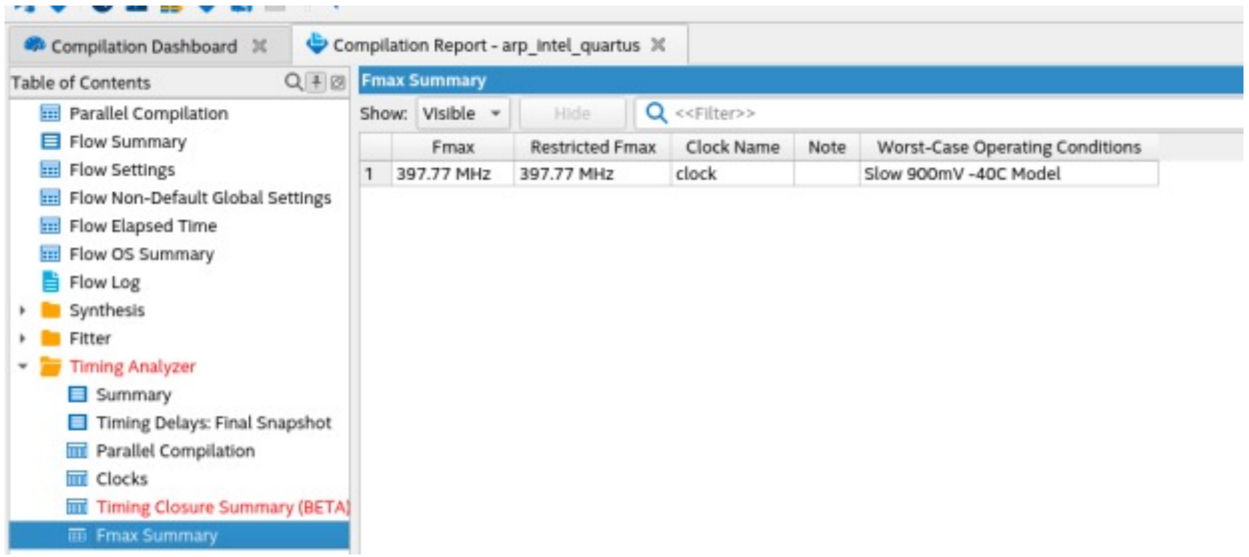
```
static ac_int<32, false>   ad_pointer = 0;
    //static ac_int<4, false>   ad_readCounter = 0;
    ac_int<32, false> ev;

    static int offset = 1;
    bool success;
    ev = input.tryRead(success);
    if (success)
    {
        ad_pointer = ac_int<32, false>(ev << (WIDTH - (offset*8)));

        output.write(ad_pointer);
    }
    if(offset < 4){
        offset++;
    }else{
        offset = 1;
    }
```



HLS tuning

example





Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note	Worst-Case Operating Conditions
1	397.77 MHz	397.77 MHz	clock		Slow 900mV -40C Model

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