

Université Libre de Bruxelles

# Automated System Partitioning for Efficient 3D Circuit Integration

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Work presentation

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# Why

## Why do we want 3D IC

- Moore's Law falters
- Always more features for the same footprint

## When do we want it

By the end of the decade

## Who works on it

- Sung Kyu Lim, GTCAD lab, Georgia Tech
- George Karypis (METIS), University of Minnesota
- And more...

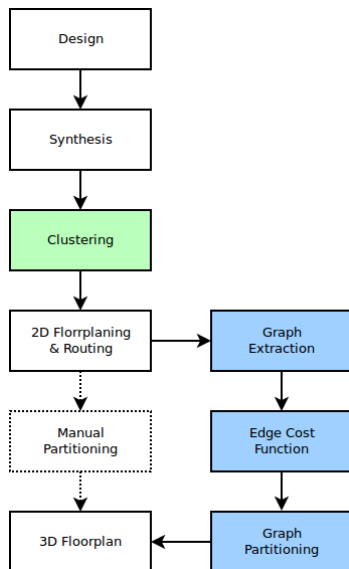
## Monolithic

- Lack of methodologies
- Thermal dissipation problems
- Manufacturing difficulties

## Stacked

- Base on 2D design
- Separate die manufacturing
- Die stacking

# Design flow



# Objectives

- Reduce interconnect length
- Reduce critical path length
- Reduce interconnect amount

### Definition 1 (Disjoint Partitions, [2])

A  $k$ -tuple  $P = (p_0, \dots, p_{k-1})$  with each  $p_i$  a set of vertices such that

$$\bigcup_{i=0}^{k-1} p_i = V \text{ with } \bigcap_{i=0}^{k-1} p_i = \emptyset$$

## Definition 2 (k-Way Partitioning)

[2] A function of the form  $\delta$

### Definition 3 (Hypergraph)

[2]



## Definition 4 (Cut)

[2]

## Definition 5 (Sum of External Degrees)

As presented by [1]:

$$\sum_{i=1}^k |E(P_i)|$$

## Definition 6 (Scaled Cost)

[1]

## Definition 7 (Absorption)

[1]

## Definition 8 (k-Way Hypergraph Partitioning Problem)

[2]

- [1] George Karypis and Vipin Kumar.  
hMETIS - A hypergraph partitioning package - Version 1.5.3.  
page 20, 1998.
- [2] David A. Papa and Igor L. Markov.  
Hypergraph Partitioning and Clustering.  
In Teofilio F. Gonzalez, editor, *Handbook of Approximation Algorithms and Metaheuristics*, chapter 61. Chapman & Hall/CRC, 2007.