Wirelength-driven Partitioning for 3D IC Stacking

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***Abstract*—The idea is to use the wire-length as a weight, rather than as a control measure.**

***Index Terms*—IEEE, IEEEtran, journal, LaTeX, paper, template.**

I. Introduction

THE litterature is quite extensive as to how the vias and the modules should be placed in a 3D IC architecture, but scarce on the wire length gain when going from a 2D to a 3D architecture. Even though it's frequently considered, it's considered as a control mesure rather than a primary objective ([1]). However, wire length influences key parameters such as latency, IR-drop and clock frequency.

II. Method

A. Hypergraph Definition

A hypergraph $\mathcal{H} = (\mathcal{V}, \mathcal{N})$ is a finite set of vertices $\mathcal{V}$ and nets $\mathcal{N}$ [2]. Each net $n_i \in \mathcal{N}$ connects a subset of $\mathcal{V}$ into a complete graph.

B. Hypergraph Extraction

As for power-aware partitioning, the scheme used is not able to create unbalanced partitions. One way to trick it is to force a fake node on the low power density partition. Such a dummy node with an arbitrary power density and a negligeable area would not jeopardize the symmetry area-wise, but would tip the balance power-wise.

C. Hypergraph Partitioning

The most widely used scheme to partition problems of this size is the k-way multilevel partitioning. In this approach, three phases are successively processed: coarsening (1), initial partitioning (2) and uncoarsening (3).

As for the partitioning, we used an implementation of Kernighan-Lin/Fiduccia-Mattheysses heuristic.

III. Conclusion

This paper is awesome.
Period.

References

[1] D. H. Kim, R. O. Topaloglu, and S.-K. Lim, "Block-level 3D IC design with through-silicon-via planning," *Design Automation Conference (ASP-DAC), 2012 17th Asia and South Pacific*, vol. 1, pp. 335–340, 2012.

[2] A. Bretto, *Hypergraph Theory*. Springer International Publishing, 2013.