Quick review of EU-supported 3D-IC projects

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CoolCube™

In the past few years, the CEA LETI has been working on a new way to integrate transistors in 3D: Clermidy et al. [2015], Michailos et al. [2016], Brunet et al. [2016], Vinet et al. [2016], Batude et al. [2015]. Their goal is to manufacture 3D monolithic chips using an innovative stacking techniques. However, they still face the problem of partitioning and gates repartition on the tiers.

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FP7 Projects:

- **FAB2ASM**: *Efficient and Precise 3D Integration of Heterogeneous Microsystems from Fabrication to Assembly*[2].
- **JEMSIP_3D**: *Joint Equipment and Materials for System-in-Package and 3D-Integration*[3].
- **NANOPACK**: *Nano Packaging Technology for Interconnect and Heat Dissipation*[4].
- **ELITE**: *Extended Large (3D) Integration TEchnology*[5].

Horizon 2020 projects:

- **TAKE5**: *Technology Advances and Key Enablers for 5 nm*[6]. This projects aims at the development of the 5nm node. Even though scaling is worth exploring, the 3D integration path is not to be left aside.

[1] http://cordis.europa.eu/project/rcn/111144_fr.html
[2] http://cordis.europa.eu/project/rcn/94309_en.html
[3] http://cordis.europa.eu/project/rcn/201936_en.html
[4] http://cordis.europa.eu/project/rcn/85245_en.html
[5] http://cordis.europa.eu/project/rcn/85238_en.html
[6] http://cordis.europa.eu/project/rcn/203403_en.html

References

P. Batude, C. Fenouillet-Beranger, L. Pasini, V. Lu, F. Deprat, L. Brunet, B. Sklenard, F. Piegas-Luce, M. Casse, B. Mathieu, O. Billoint, G. Cibrario, O. Turkyilmaz, H. Sarhan, S. Thuries, L. Hutin, S. Sollier, J. Widiez, L. Hortemel, C. Tabone, M. P. Samson, B. Previtali, N. Rambal, F. Ponthenier, J. Mazurier, R. Beneyton, M. Bidaud, E. Josse, E. Petitprez, O. Rozeau, M. Rivoire, C. Euvard-Colnat, A. Seignard, F. Fournel, L. Benaissa, P. Coudrain, P. Leduc, J. M. Hartmann, P. Besson, S. Kerdiles, C. Bout, F. Nemouchi, A. Royer, C. Agraffeil, G. Ghibaudo, T. Signamarcheix, M. Haond, F. Clermidy, O. Faynot, and M. Vinet. 3DVLSI with CoolCube process: An alternative path to scaling. *Digest of Technical Papers - Symposium on VLSI Technology*, 2015-August:T48–T49, 2015. ISSN 07431562. doi: 10.1109/VLSIT.2015.7223698.

L. Brunet, P. Batude, C. Fenouillet-Beranger, P. Besombes, L. Hortemel, F. Ponthenier, B. Previtali, C. Tabone, A. Royer, C. Agraffeil, C. Euvrard-Colnat, A. Seignard, C. Morales, F. Fournel, L. Benaissa, T. Signamarcheix, P. Besson, M. Jourdan, R. Kachtouli, V. Benevent, J. M. Hartmann, C. Comboroure, N. Allouti, N. Posseme, C. Vizioz, C. Arvet, S. Barnola, S. Kerdiles, L. Baud, L. Pasini, C. M. V. Lu, F. Deprat, A. Toffoli, G. Romano, C. Guedj, V. Delaye, F. Boeuf, O. Faynot, and M. Vinet. First demonstration of a CMOS over CMOS 3D VLSI CoolCube integration on 300mm wafers. *Digest of Technical Papers - Symposium on VLSI Technology*, 2016-Septe:11–12, 2016. ISSN 07431562. doi: 10.1109/VLSIT.2016.7573428.

F. Clermidy, O. Billoint, H. Sarhan, and S. Thuries. Technology scaling: The CoolCube paradigm. *2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, S3S 2015*, pages 2–5, 2015. doi: 10.1109/S3S.2015.7333504.

J. Michailos, P. Coudrain, A. Farcy, N. Hotellier, S. Cheramy, S. Lhostis, E. Deloffre, Y. Sanchez, A. Jouve, F. Guyader, E. Saugier, V. Fiori, P. Vivet, M. Vinet, C. Fenouillet-Beranger, F. Casset, P. Batude, F. Breuf, Y. Henrion, B. Vianne, L. M. Collin, J. P. Colonna, L. Benaissa, L. Brunet, R. Prieto, R. Velard, and F. Ponthenier. New challenges and opportunities for 3D integrations. *Technical Digest - International Electron Devices Meeting, IEDM*, 2016-February:8.5.1–8.5.4, 2016. ISSN 01631918. doi: 10.1109/IEDM.2015.7409655.

M. Vinet, P. Batude, C. Fenouillet-Beranger, L. Brunet, V. Mazzochi, C. M. V. Lu, F. Deprat, J. Micout, B. Previtali, P. Besombes, N. Rambal, F. Andrieu, O. Billoint, M. Brocard, S. Thuries, G. Berhault, C. L. Dos Santos, G. Cibrario, F. Clermidy, D. Gitlin, and O. Faynot. Opportunities brought by sequential 3D CoolCube integration. *European Solid-State Device Research Conference*, 2016-Octob:226–229, 2016. ISSN 19308876. doi: 10.1109/ESSDERC.2016.7599627.