3DIC Partitioning

Turning integrated circuits 3D

Quentin Delhaye

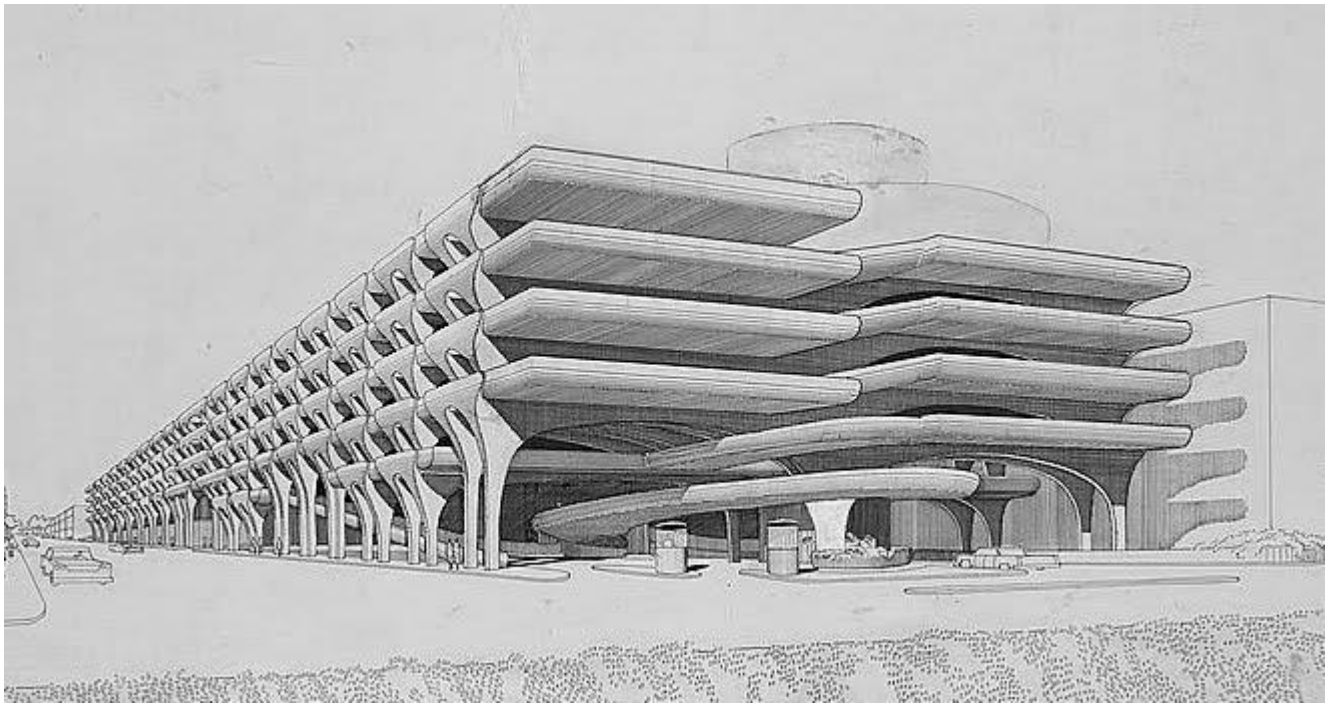
beams

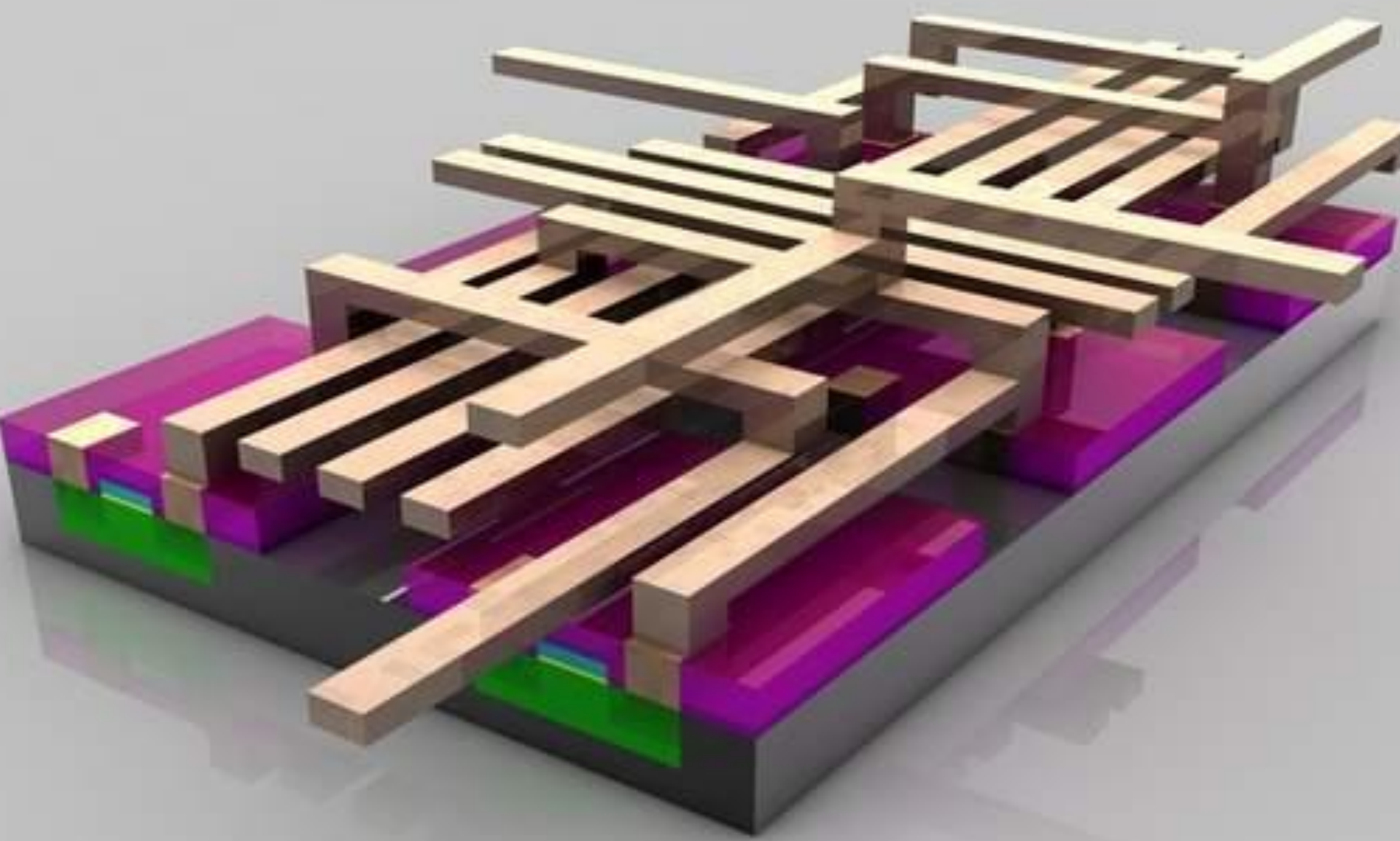
Fit as much as you can

Shrink the car

Physical limitation

Go 3D

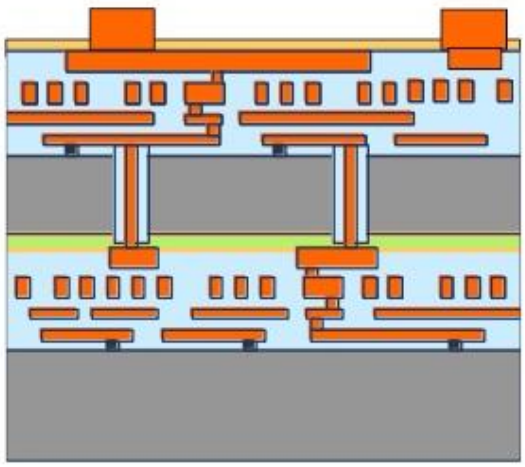




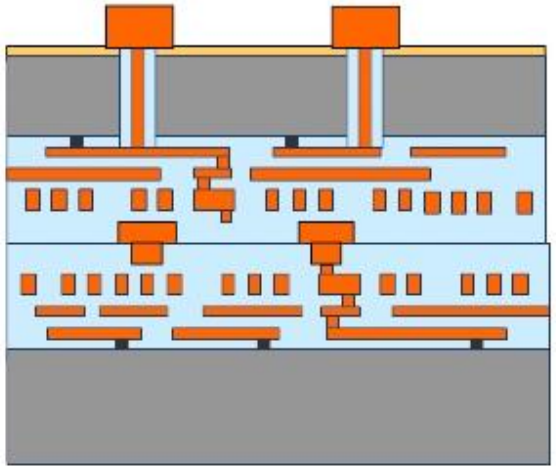
Planar 2D IC

Planar 2D IC: only one transistor layer

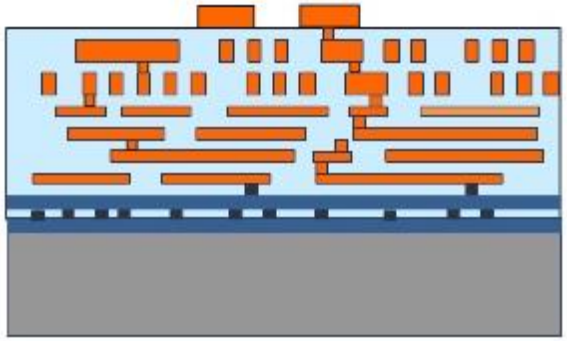
What is a 3D IC?



Face-to-Back (past)

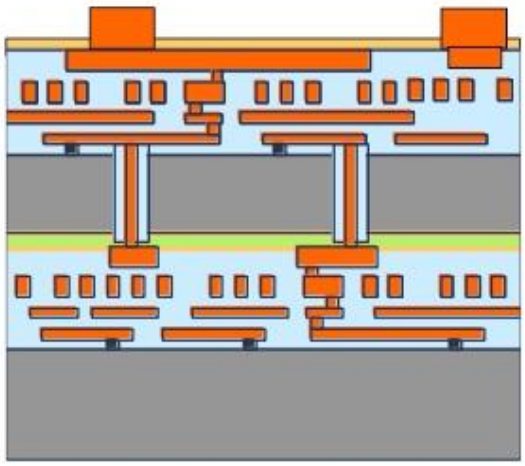


Face-to-Face (present)

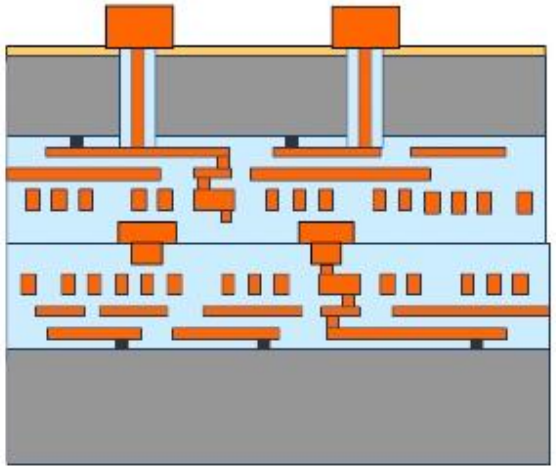


Transistor-on-transistor (future)

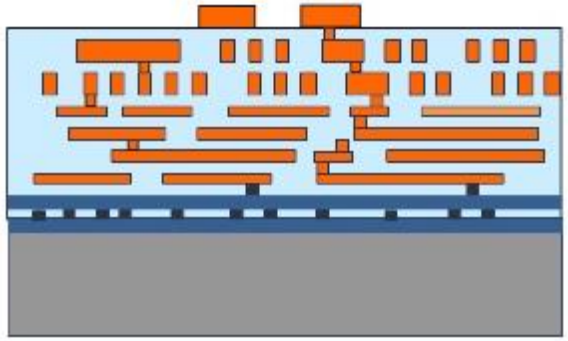
What is a 3D IC?



Face-to-Back (past)



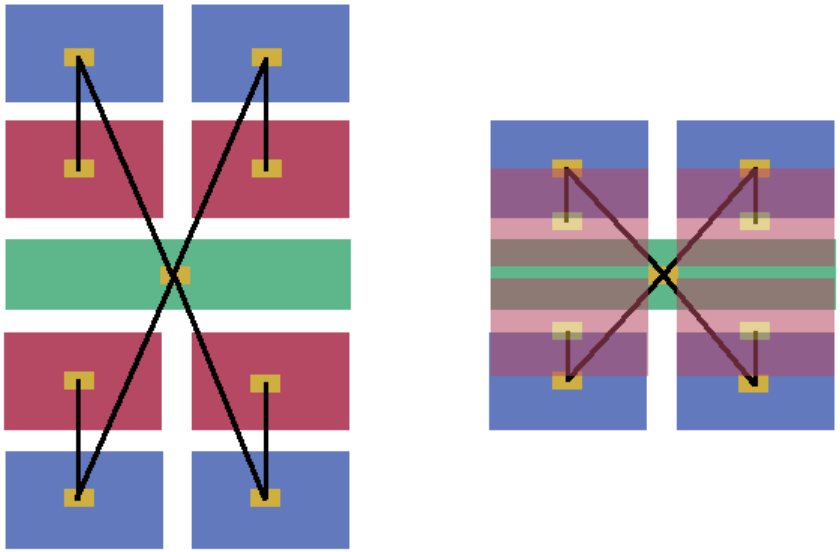
Face-to-Face (present)



Transistor-on-transistor (future)

Somebody needs to decide what goes where

3D benefit: shorter connections



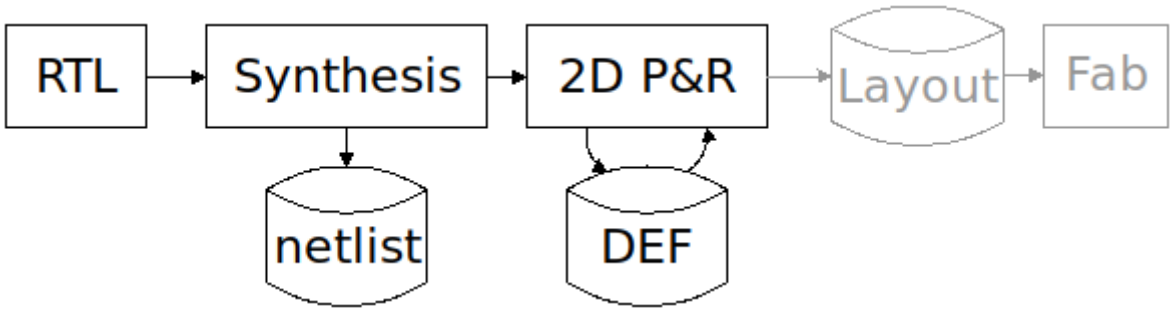
Increased performance

Decreased system power consumption

Improved area utilisation

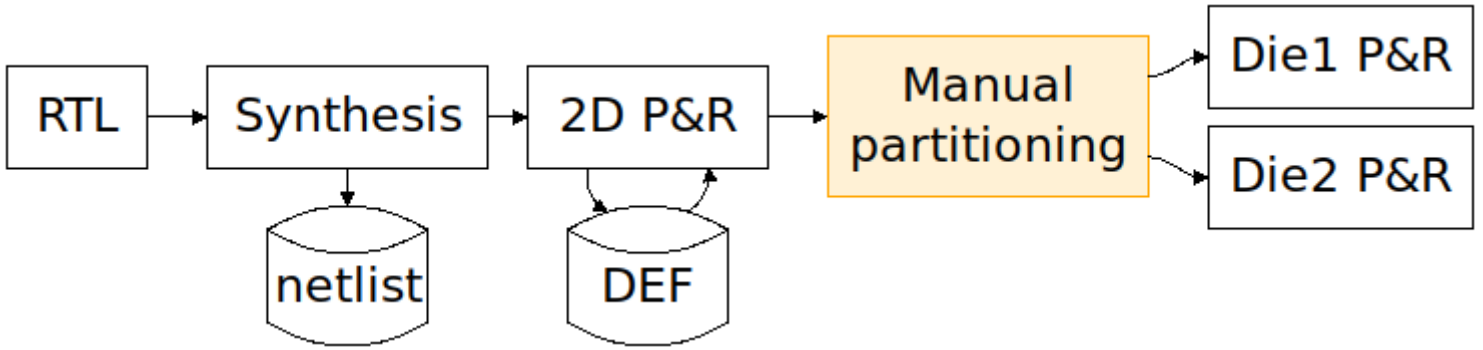
2D flow...

Place and route (P&R): QRouter, Graywolf, FGR, ...

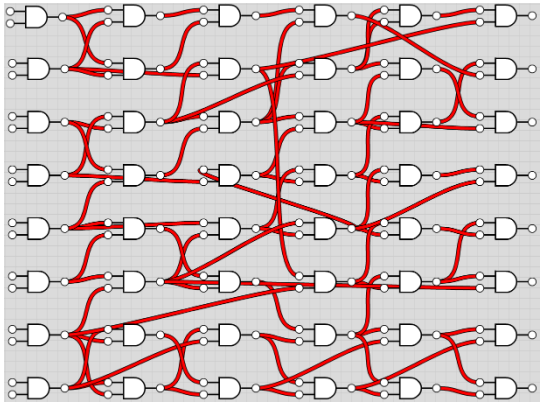


… Extended to 3D

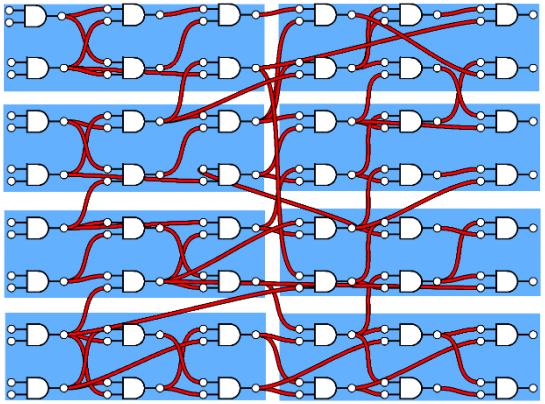
Pick which standard cell or module goes where



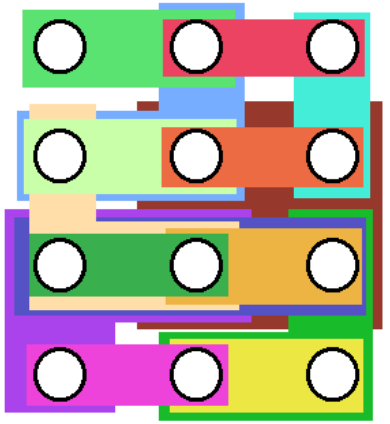
Steps to go 3D



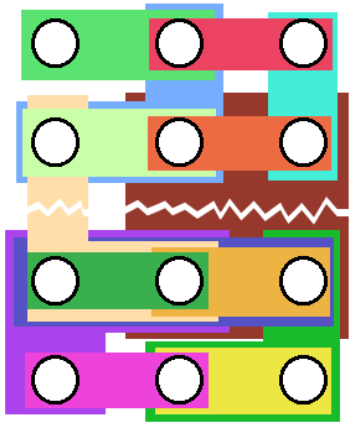
Clustering



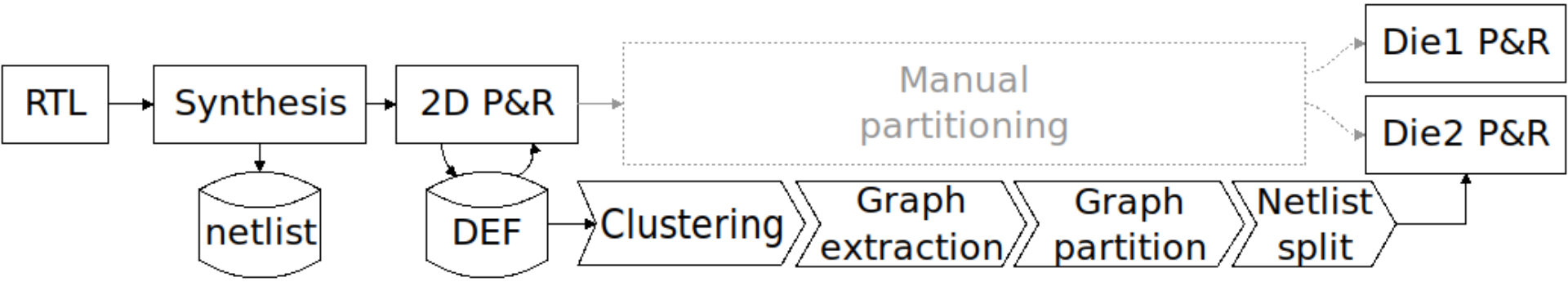
Hypergraph



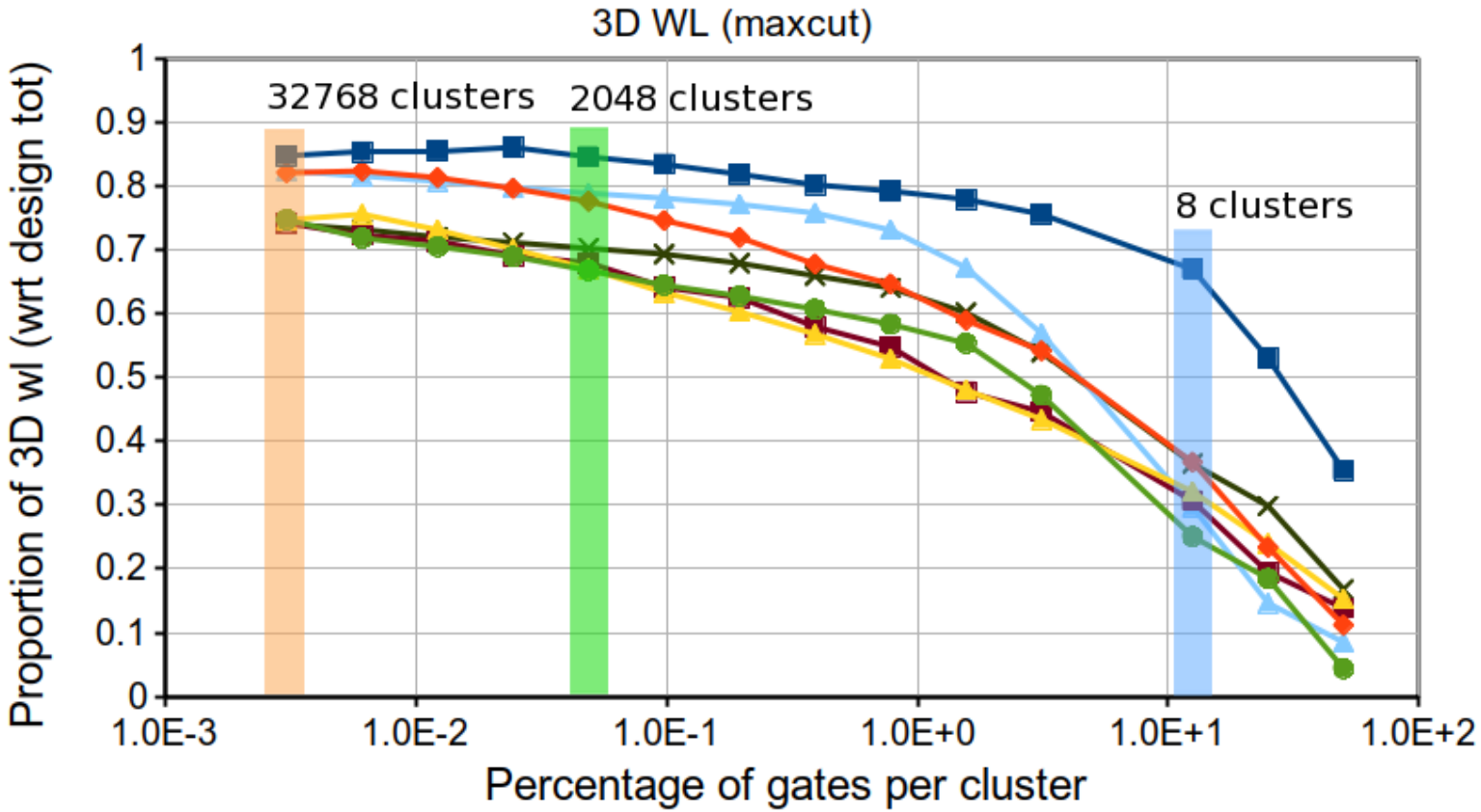
Partitioning



Automated 3D flow



There is an optimum grain



Automated 3DIC partitioning