Progress (2015-11-30)

Status

- According to B. Fortz, the size of the trees would require metaheuristics.
- Brief exploration of MH (SA, TS, GA), sent to B. Sartori.
- Need to dive into METIS to understand the type of algo used.

Highlights

- Meeting with B. Fortz (very interested in the project).

Low points

- Slide deck is late.

	Planned	Due Date	Status
Slide deck	07/12	23/11	Late

Université Libre de Bruxelles

Automated System Partitioning for Efficient 3D Circuit Integration

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Work presentation

Quentin Delhaye

Why

Why do we want 3D IC

- Moore's Law falters
- Always more features for the same footprint

When do we want it

By the end of the decade

Who works on it

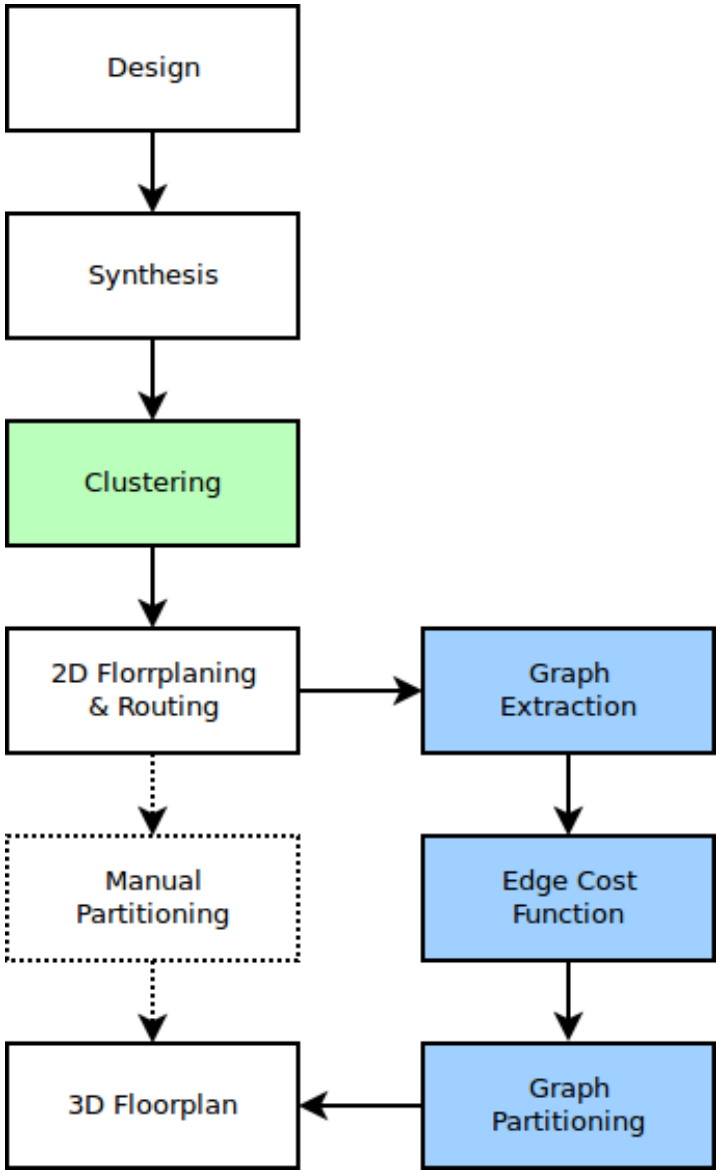
- Sung Kyu Lim, GTCAD lab, Georgia Tech
- George Karypis (METIS), University of Minnesota
- And more...

3D IC

Monolithic
- Lack of methodologies
- Thermal dissipation problems
- Manufacturing difficulties

Stacked
- Base on 2D design
- Separate die manufacturing
- Die stacking

Design flow


Design
Synthesis
Clustering
2D Florrplaning & Routing
Graph Extraction
Manual Partitioning
Edge Cost Function
3D Floorplan
Graph Partitioning

Objectives

- Reduce interconnect length
- Reduce critical path length
- Reduce interconnect amount