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3D-Stacked Integrated Circuits: How Fine Should System Partitioning be?

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In the next 15 minutes

Correlation between MAX-cut and 3D nets

Study of an optimal partitioning grain

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Correlation between **MAX-cut** and **3D** nets

Study of an optimal **partitioning grain**

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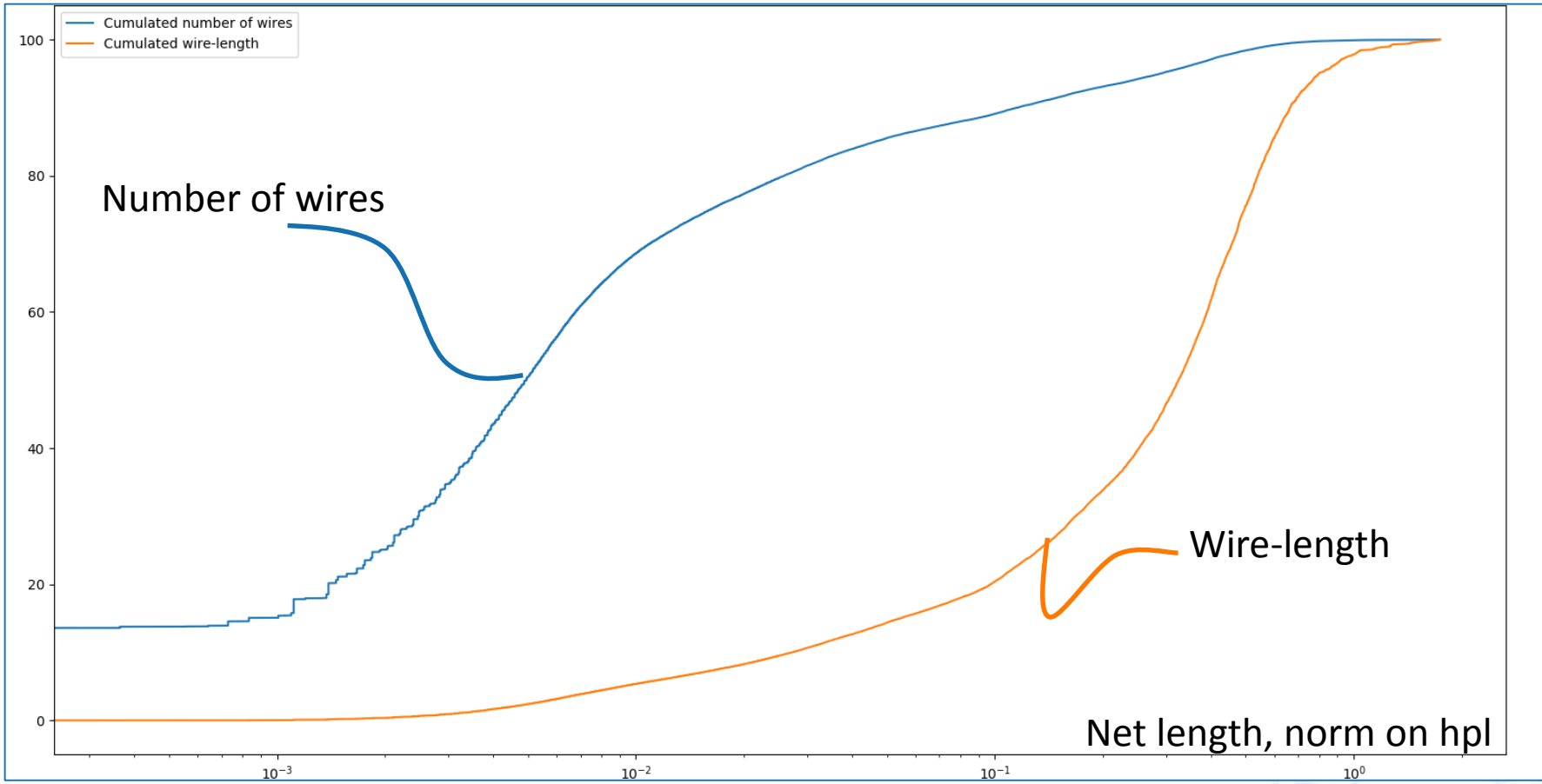
What is inside a 2D IC?



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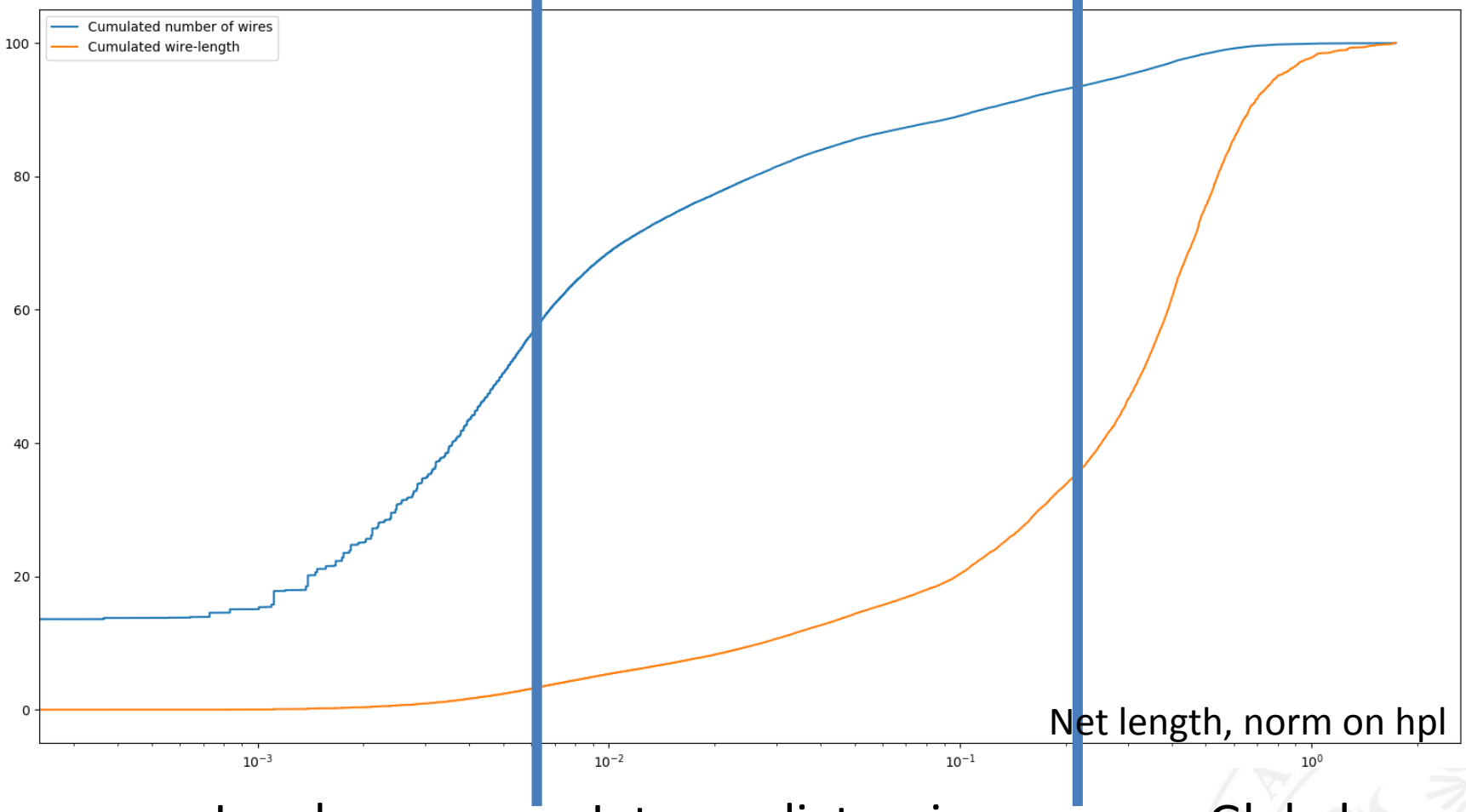

Local | Intermediate wires | Global

3D flavours

	3D-SIC	3D-SOC		3D-IC
Wiring	Global	Intermediate	Local	Local
Partition	Die	Clusters	Std cells	Transistors
3D Tech	Die stacking	W2W bonding	Active layer bonding or deposition	

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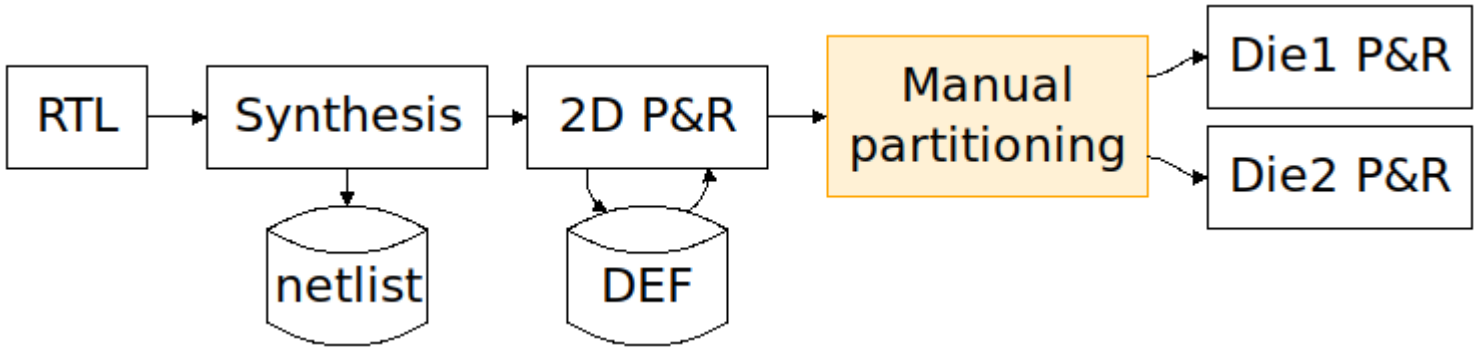
Next level challenges: clustering and partitioning

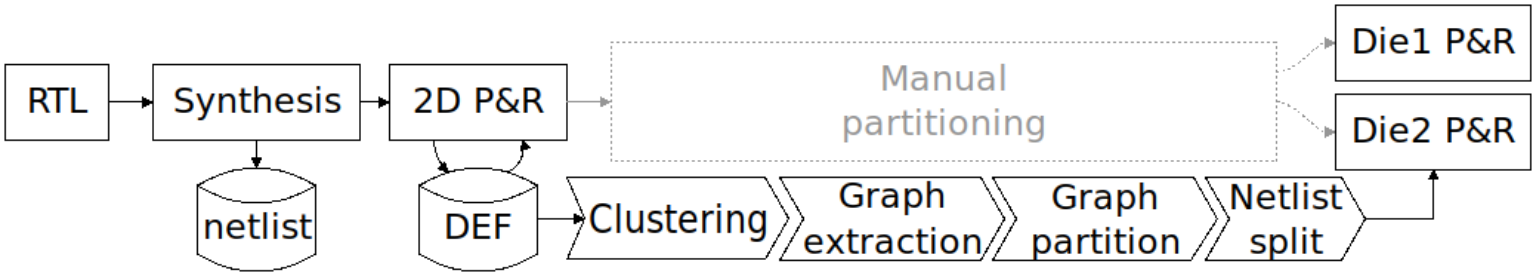
Focus on the clustering

- What would be a good clustering method?
- What would be an ideal clustering grain?

Method: Global flow



Method: Global flow



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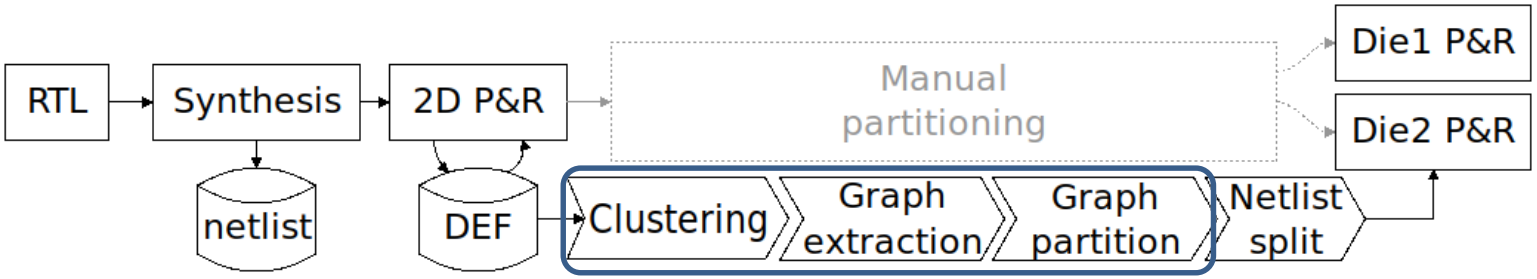

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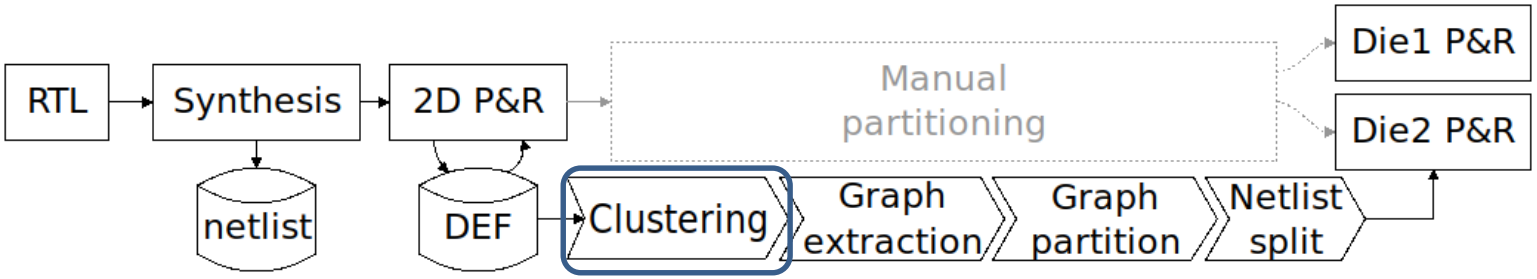

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Method: Clustering

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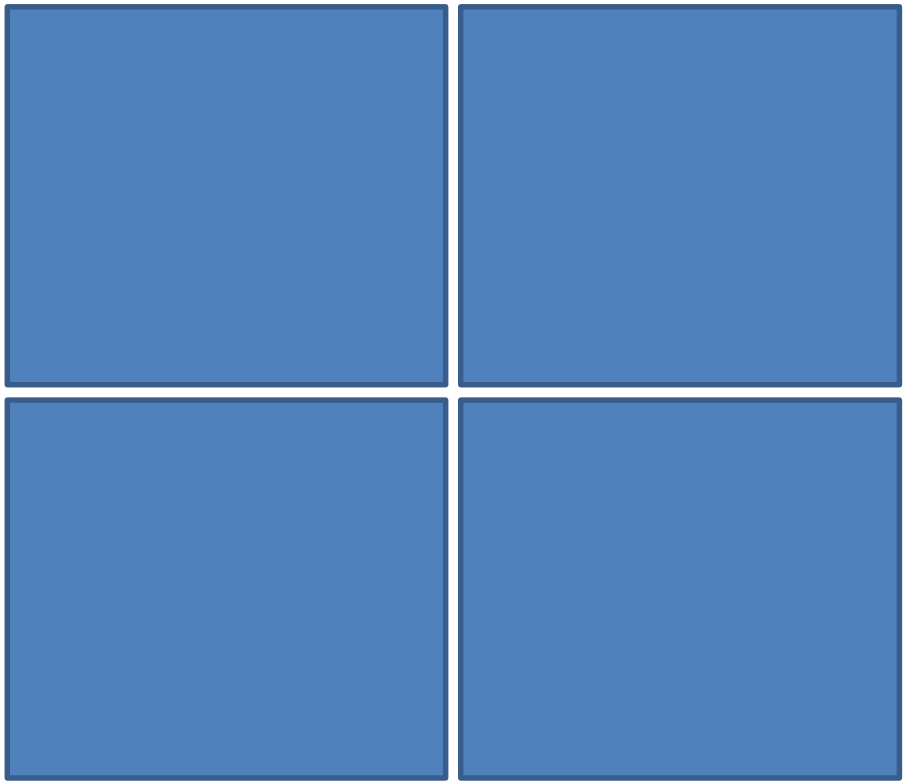


Method: Partitioning

Bipartition the graph: Min/max-cut

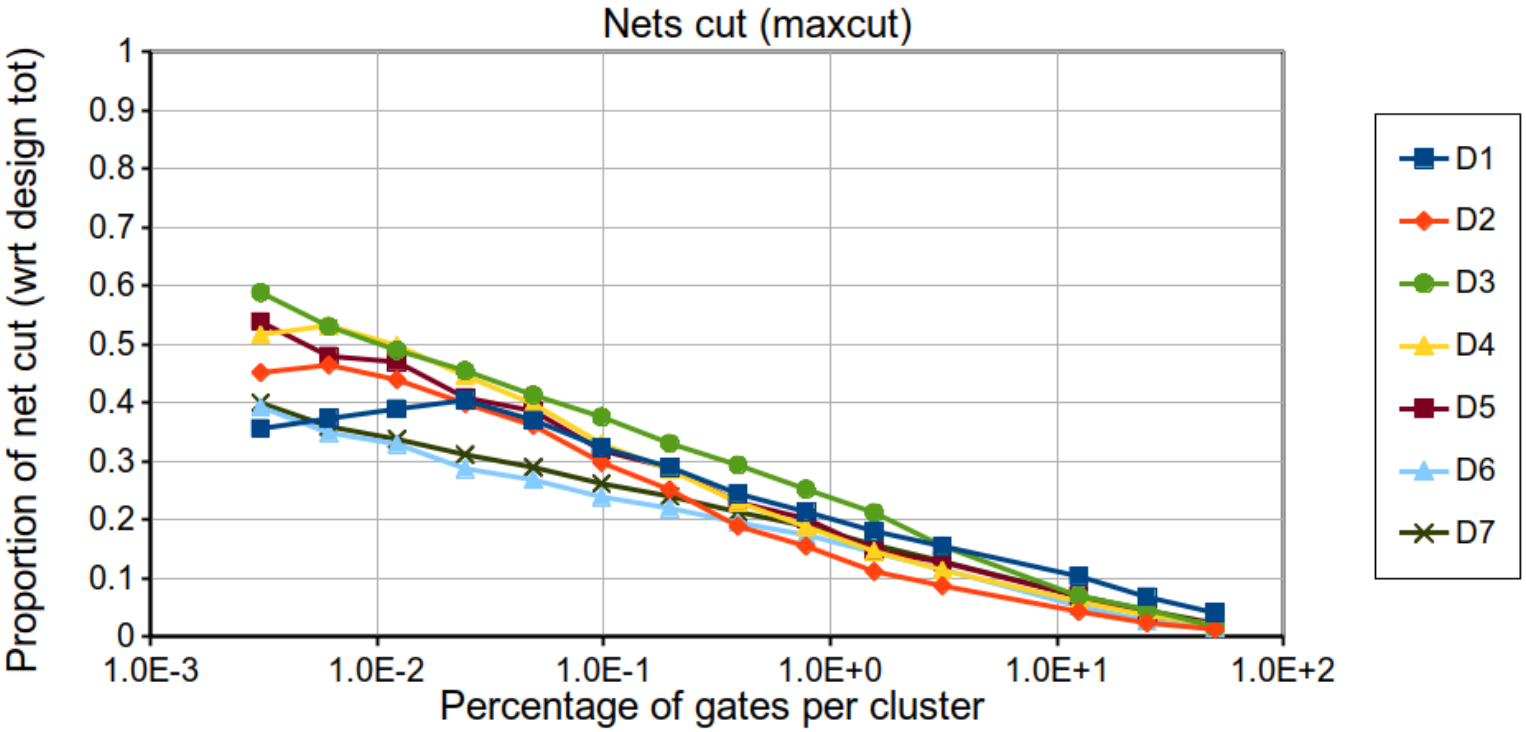
Min or max cutsize:

- Number of nets
- Total wire-length
- Average wire-length

Designs

Design	Gates	Nets	Wire-length (norm)
D1	42,471	49,633	2,101
D2	121,580	137,171	2,050
D3	185,777	200,999	2,860
D4	220,587	234,373	4,318
D5	289,812	306,118	5,312
D6	694,082	773,679	12,606
D7	808,199	883,295	16,722

Results: clustering grain



Cut as little as possible, stay low on the Y-axis

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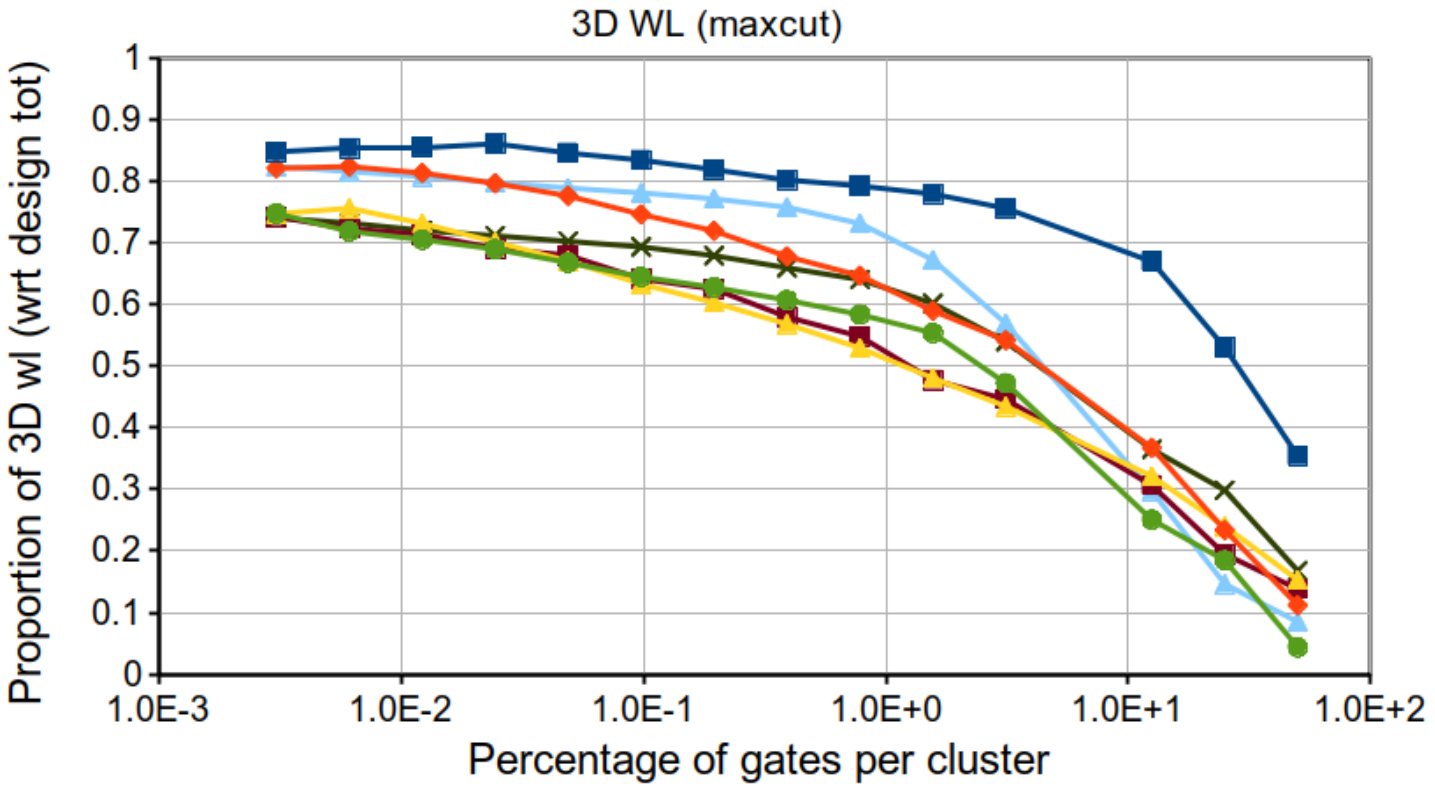
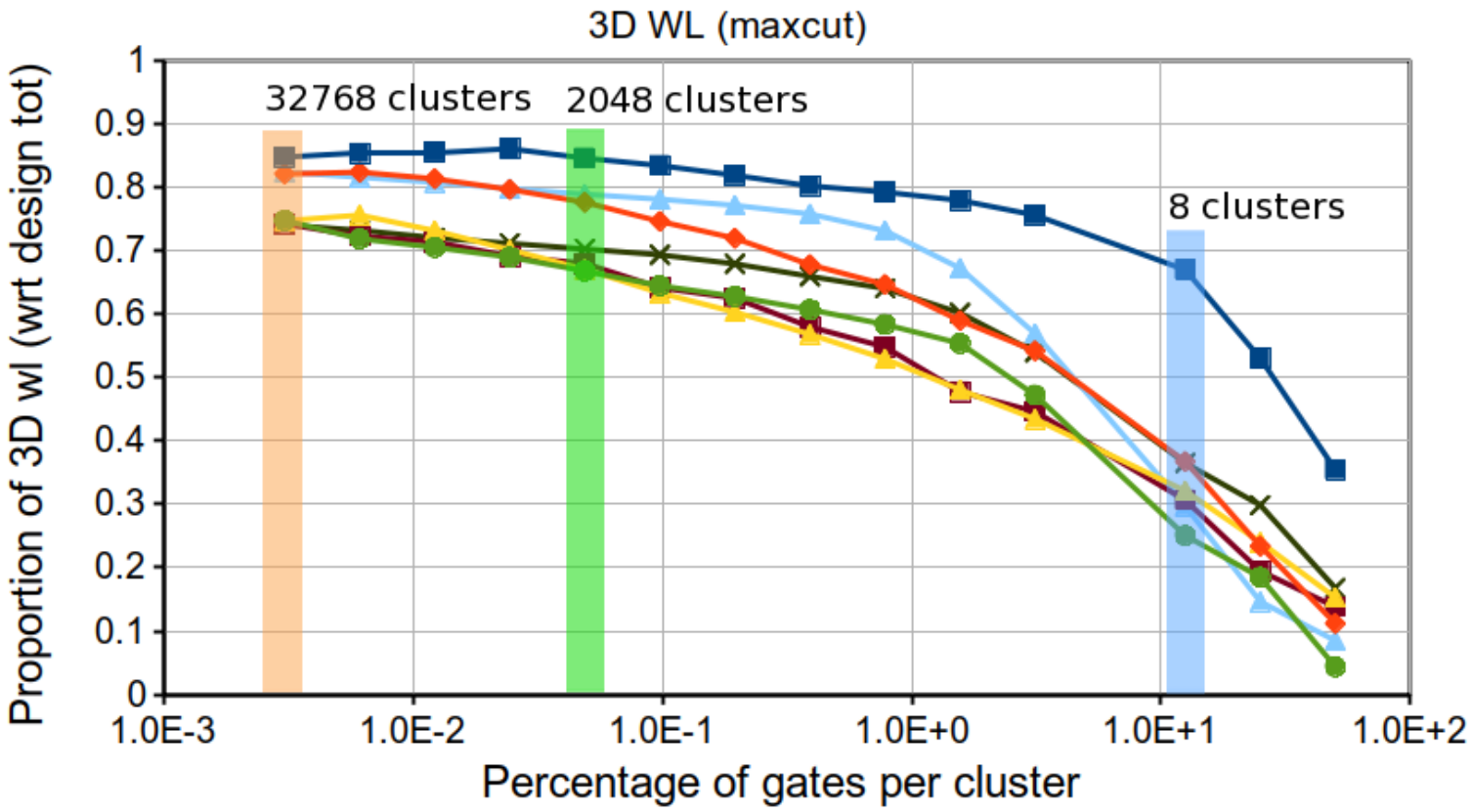
Results: clustering grain



Cut as long as possible, get high on the Y-axis

Results: clustering grain



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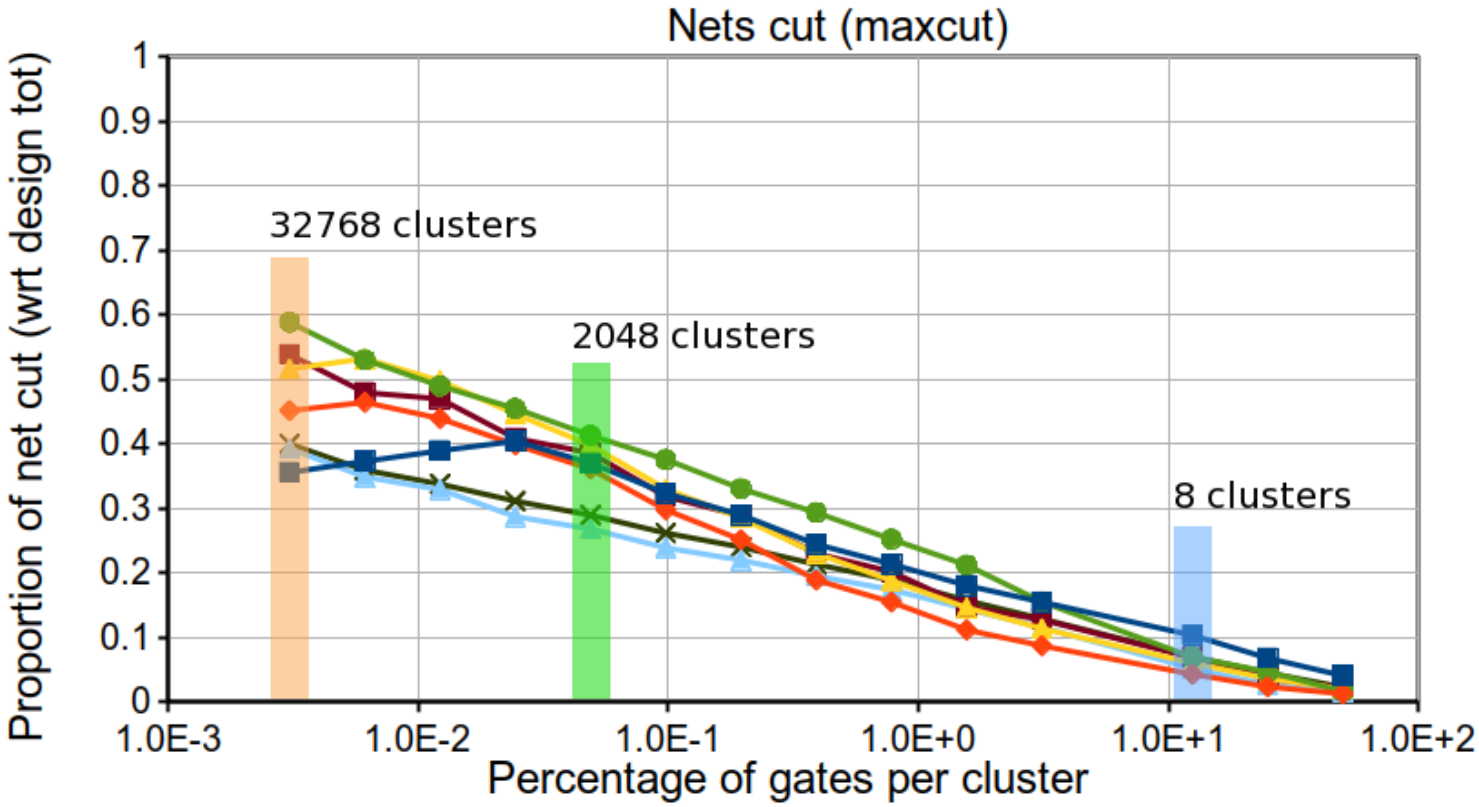
Results: clustering grain



Results: clustering grain

	Percentage of nets cut			Percentage of 3D WL		
Clusters	8	2048	32768	8	2048	32768
Average	7.00%	35.00%	49.00%	37.00%	73.00%	78.00%
Std dev	2.00%	5.00%	7.00%	13.00%	6.00%	4.00%

Future work

- New partitioning metrics: gate dispersion
- New clustering methods: heuristics on progressive wire-length
- Fully automated toolchain

- 3D SIC
- 3D SoC
- 3D IC