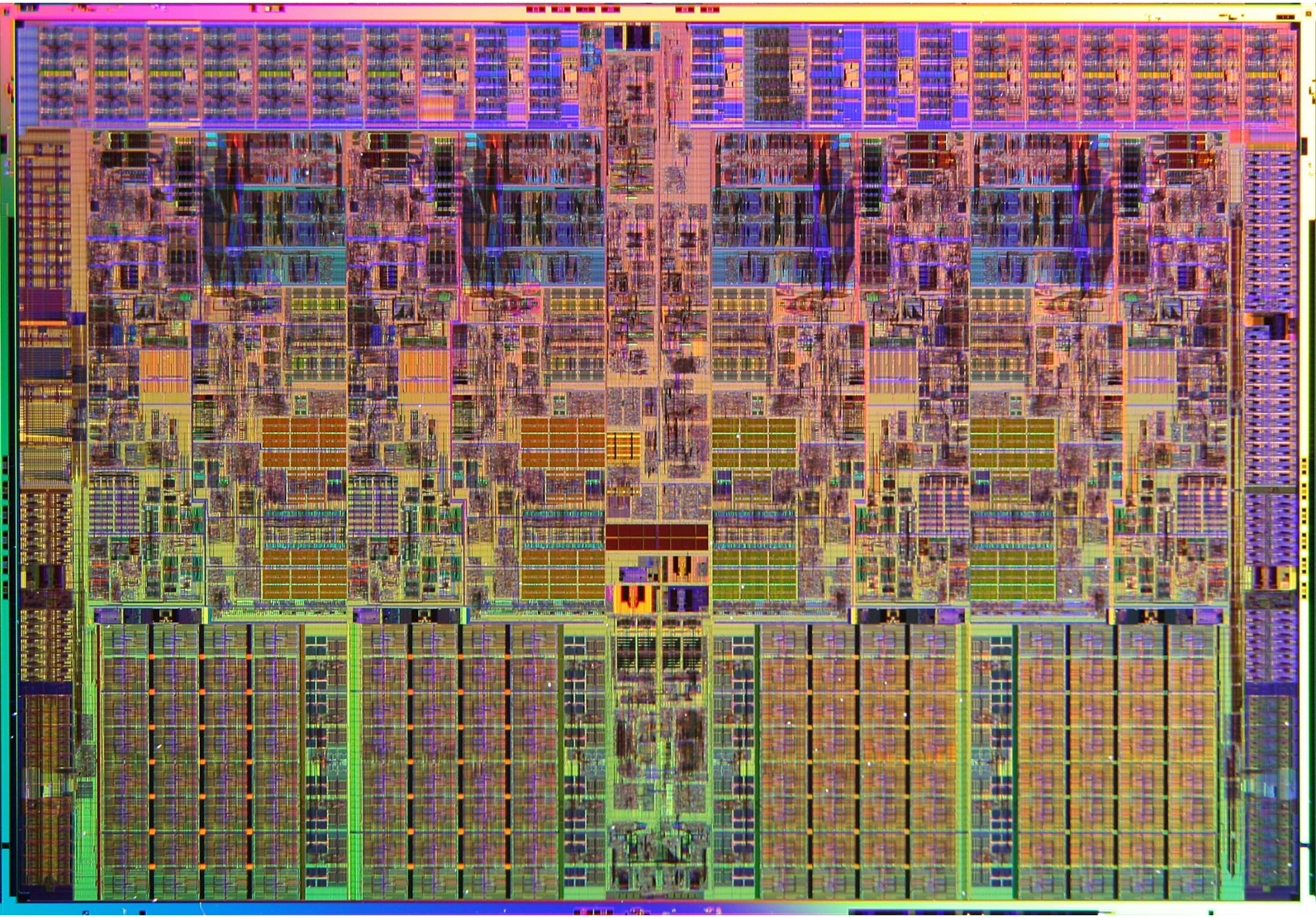
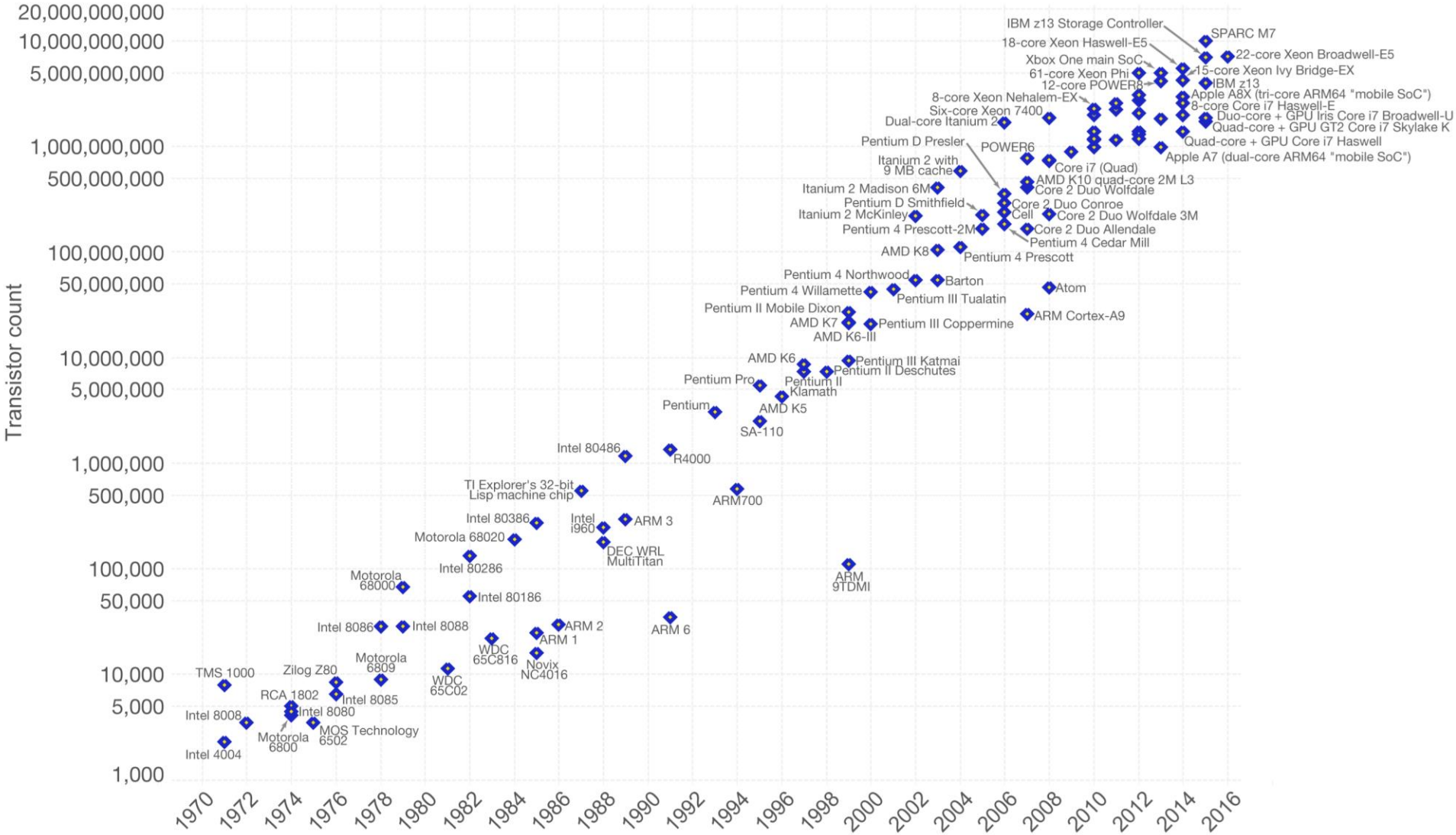
3D Integrated Circuits



Moore's Law


Transistor count
20,000,000,000
10,000,000,000
5,000,000,000
1,000,000,000
500,000,000
100,000,000
50,000,000
10,000,000
5,000,000
1,000,000
500,000
100,000
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10,000
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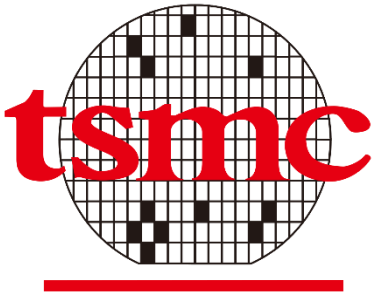
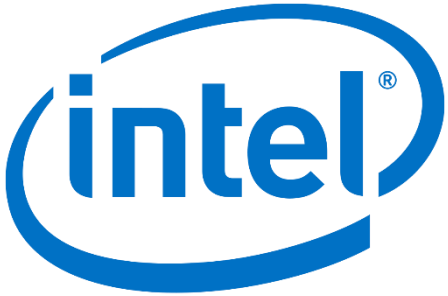
1970
1972
1974
1976
1978
1980
1982
1984
1986
1988
1990
1992
1994
1996
1998
2000
2002
2004
2006
2008
2010
2012
2014
2016
IBM z13 Storage Controller
SPARC M7
18-core Xeon Haswell-E5
22-core Xeon Broadwell-E5
Xbox One main SoC
15-core Xeon Ivy Bridge-EX
61-core Xeon Phi
12-core POWER8
IBM z13
Apple A8X (tri-core ARM64 "mobile SoC")
8-core Xeon Nehalem-EX
8-core Core i7 Haswell-E
Six-core Xeon 7400
Duo-core + GPU Iris Core i7 Broadwell-U
Dual-core Itanium 2
Quad-core + GPU GT2 Core i7 Skylake K
Pentium D Presler
Quad-core + GPU Core i7 Haswell
POWER6
Apple A7 (dual-core ARM64 "mobile SoC")
Itanium 2 with 9 MB cache
Core i7 (Quad)
AMD K10 quad-core 2M L3
Itanium 2 Madison 6M
Core 2 Duo Wolfdale
Pentium D Smithfield
Core 2 Duo Conroe
Itanium 2 McKinley
Cell
Core 2 Duo Wolfdale 3M
Pentium 4 Prescott-2M
Core 2 Duo Allendale
Pentium 4 Cedar Mill
AMD K8
Pentium 4 Prescott
Pentium 4 Northwood
Barton
Atom
Pentium 4 Willamette
Pentium III Tualatin
Pentium II Mobile Dixon
ARM Cortex-A9
AMD K7
Pentium III Coppermine
AMD K6-III
AMD K6
Pentium III Katmai
Pentium II Deschutes
Pentium Pro
Pentium II Klamath
Pentium
AMD K5
SA-110
Intel 80486
R4000
TI Explorer's 32-bit Lisp machine chip
ARM700
Intel 80386
Intel i960
ARM 3
Motorola 68020
DEC WRL MultiTitan
Intel 80286
ARM 9TDMI
Motorola 68000
Intel 80186
Intel 8086
Intel 8088
ARM 2
ARM 1
ARM 6
WDC 65C816
Motorola 6809
Novix NC4016
TMS 1000
Zilog Z80
WDC 65C02
RCA 1802
Intel 8085
Intel 8008
Intel 8080
MOS Technology 6502
Motorola 6800
Intel 4004

Do you know them?





Together, they dominate...

Over 73% of the market.

Together, they make...

Over $46 billions in revenue.

Together, they lead...

The technology race
and state-of-the-art techniques.

TOP 4 Foundries

Market domination

Stellar revenue

Technology leaders

Rock’s Law is killing the market

Double the manufacturing cost every two years.

Past $15 billions for the previous node.

GF drops out

“GlobalFoundries is putting its 7nm finFET program on hold indefinitely and has dropped plans to pursue technology nodes beyond 7nm.”

Extend Moore’s Law

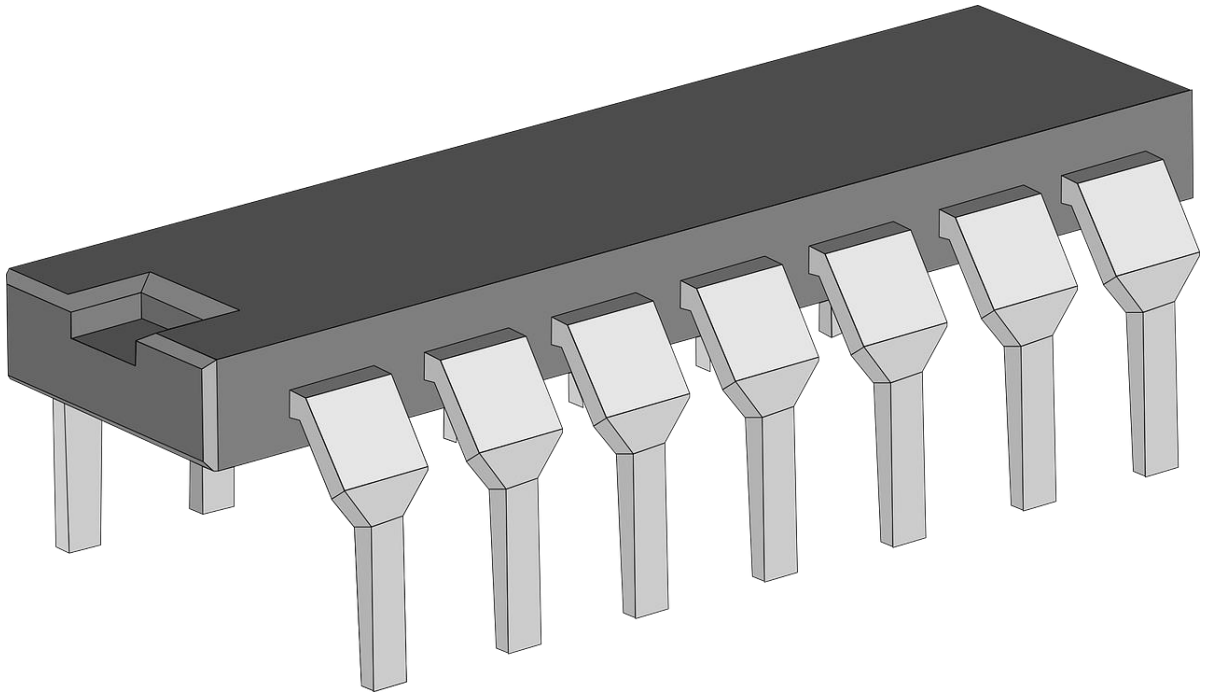
New transistors topologies

New materials

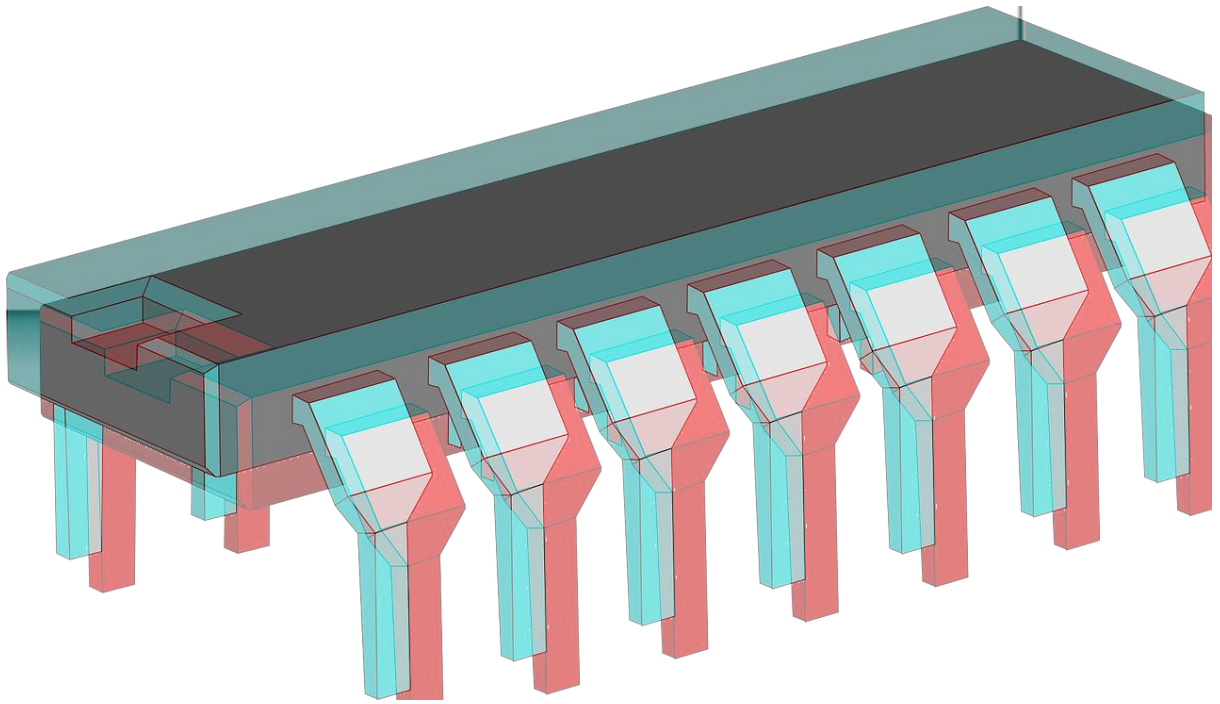
Heterogeneous integration

3D integration

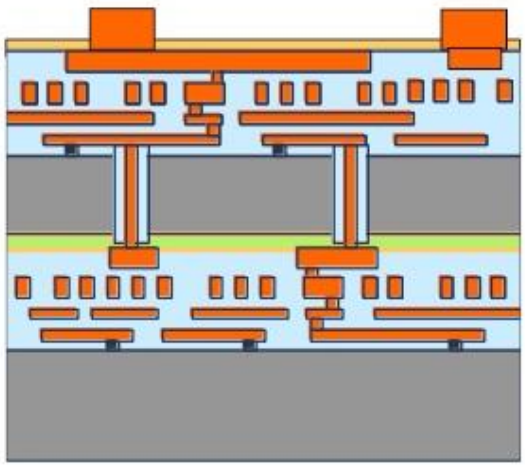
What is a 3D IC?



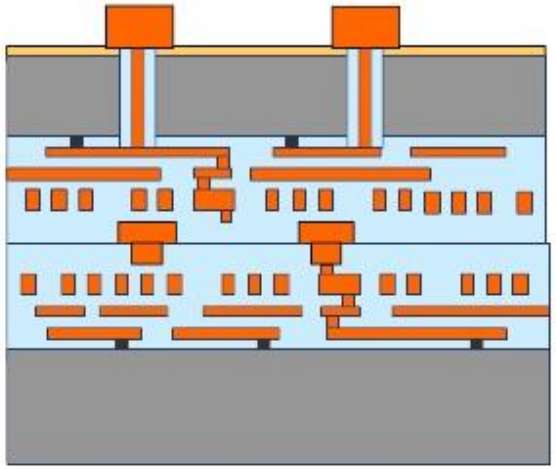
What is a 3D IC?



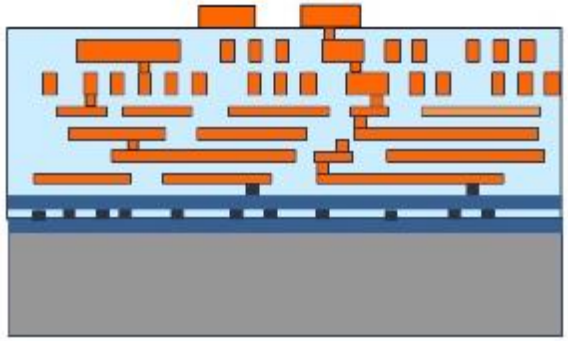
What is a 3D IC?



Face-to-Back (past)



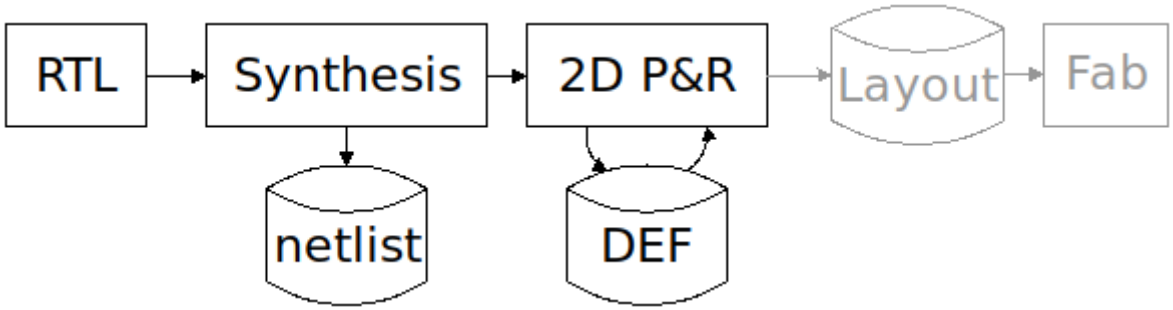
Face-to-Face (present)



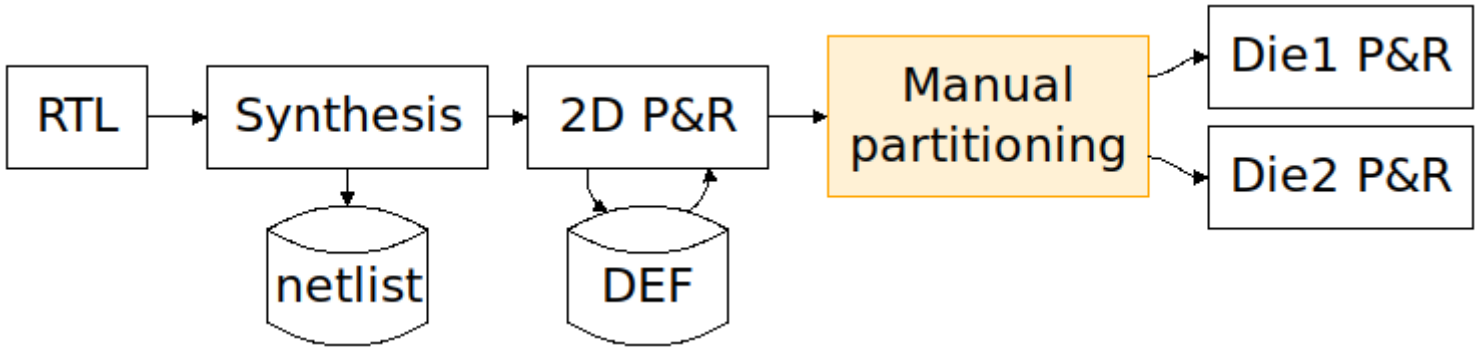
Transistor-on-transistor (future)

Somebody needs to decide what goes where

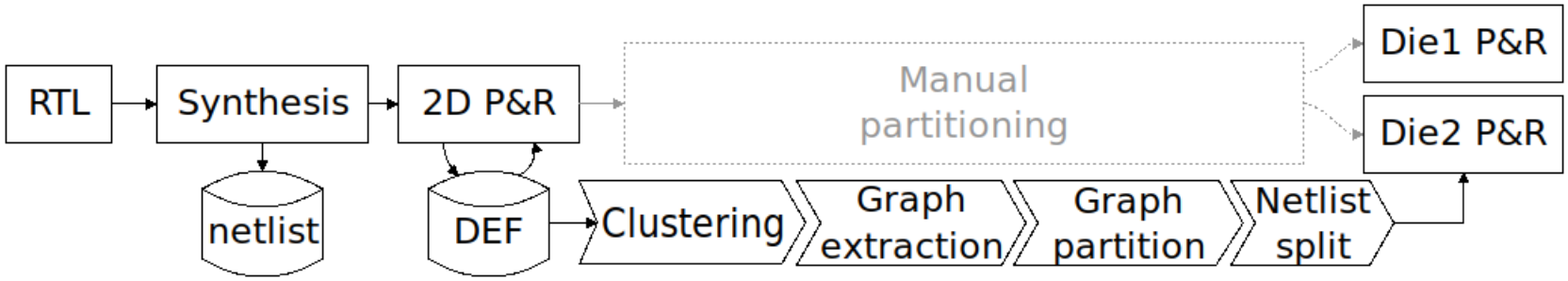
How do we design a 2D IC?



How do we design a 3D IC?



How can we do it better?



Two main challenges

Clustering

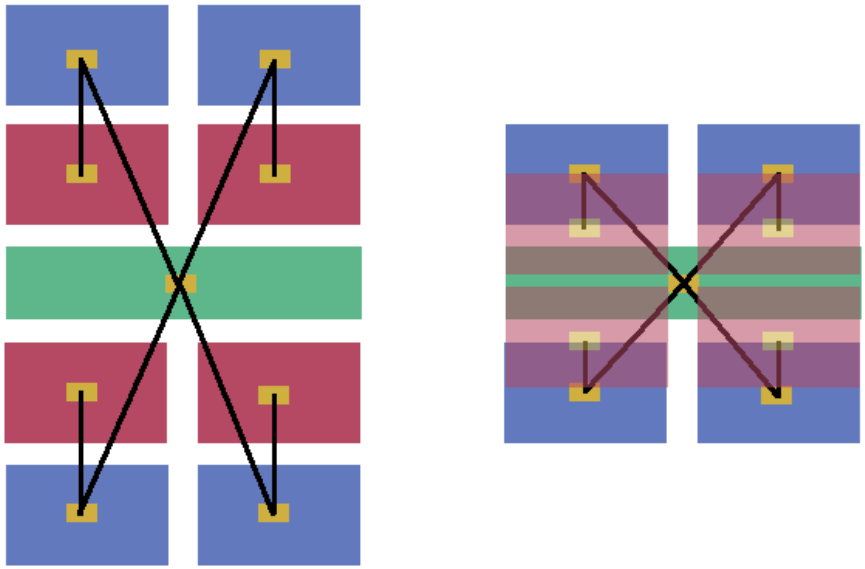
- Grouping gates together

Partitioning

- Splitting the design

Why bother clustering?

The aim is to shorten the connections.



Why bother clustering?

The aim is to shorten the connections.

Can you see the risk in **not** clustering?

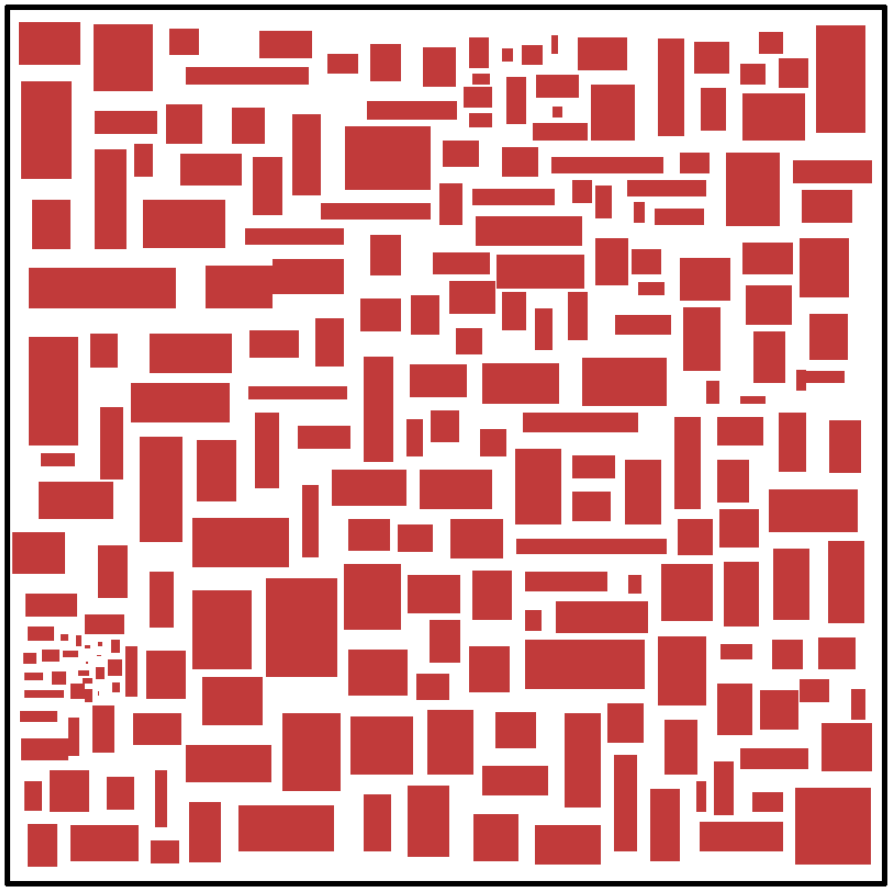
Why bother clustering?

The aim is to shorten the connections.

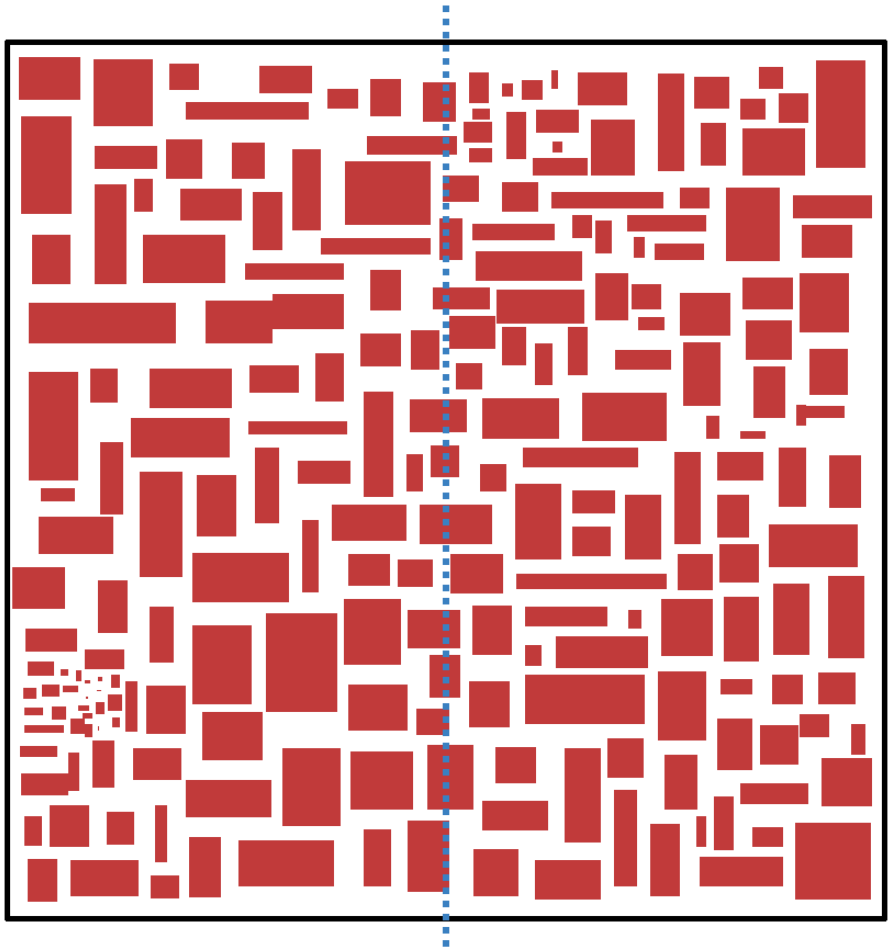
Can you see the risk in **not** clustering?

Do not cut short wires. Hide Them. Please.

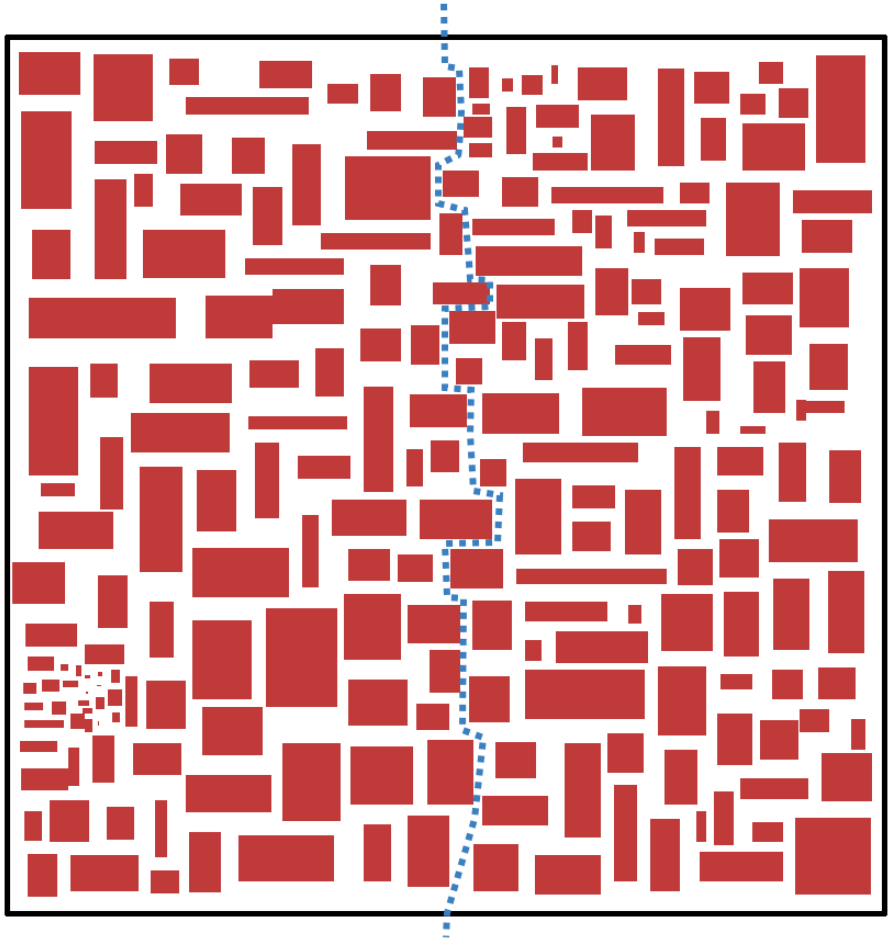
Clustering:
Hierarchical geometric



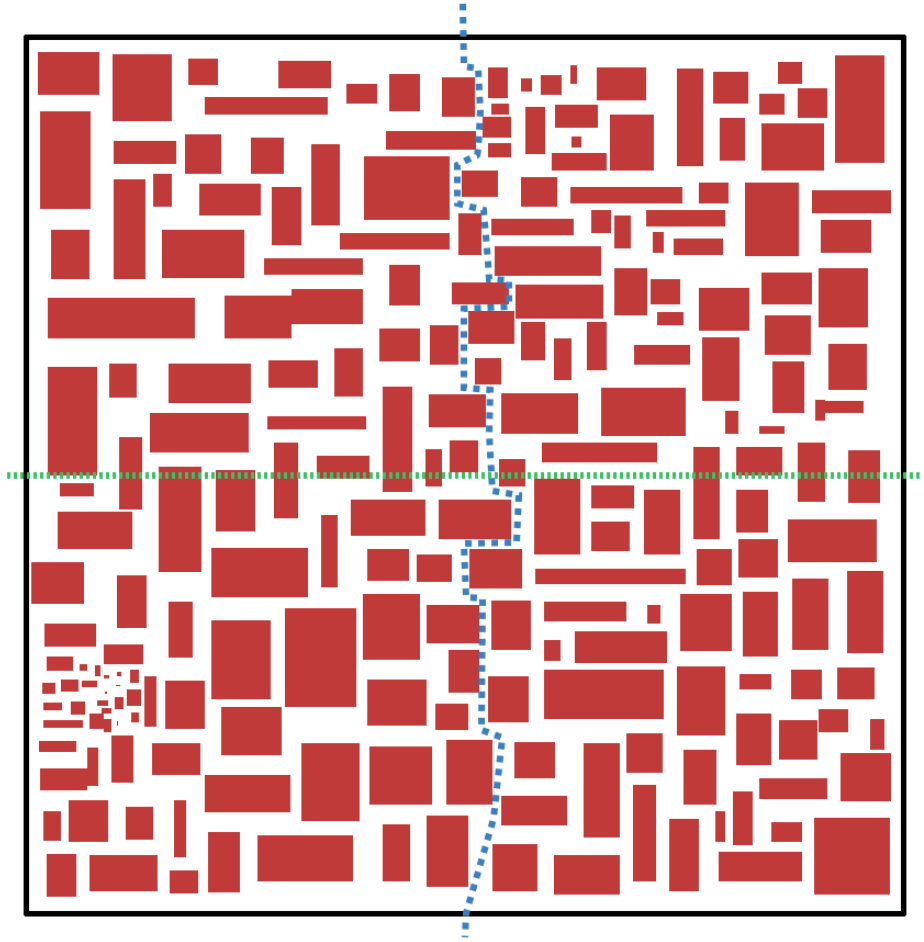
Clustering:
Hierarchical geometric



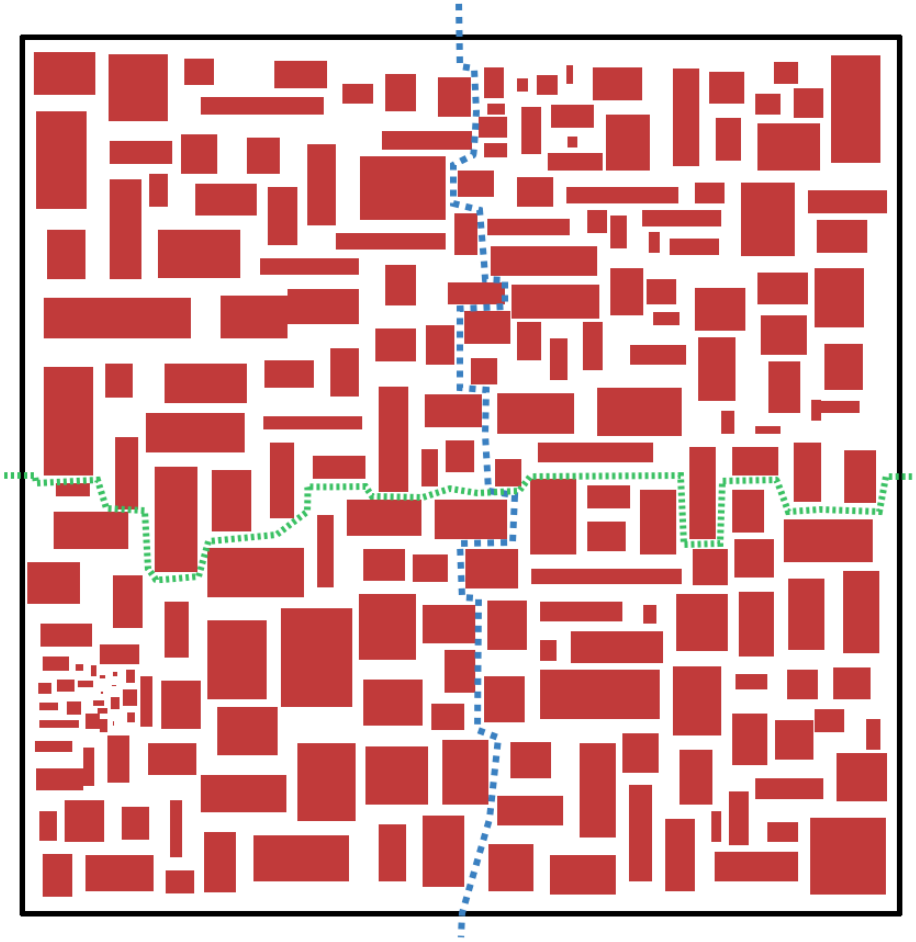
Clustering:
Hierarchical geometric



Clustering:
Hierarchical geometric



Clustering:
Hierarchical geometric



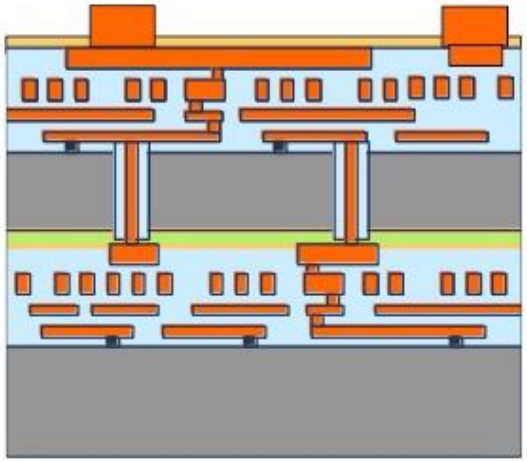
Clustering: Progressive wire-length

1) Cluster the gates connected by very short wires
2) Check if the system is still “balanced bi-partitionable”
3) ???
4) Forget about this method because it’s broken

→ Cluster phagocytosis

Partitioning: MIN-cut

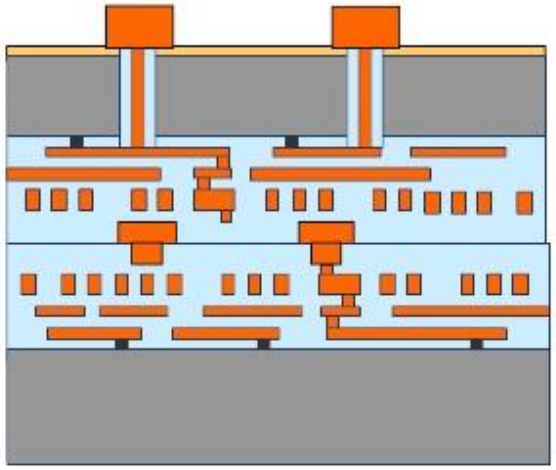
Cut as few nets as possible



Minimize 3D connections

Partitioning: MAX-cut

Cut as many nets as possible



Maximize 3D connections (if you clustered cleverly!)

Let’s summarize all this

Traditional 2D ICs are in need of a paradigm shift.

3D is an alternative path to keep Moore going.

Clustering and partitioning are not trivial and matter.

What do you think?

Does it make sense to design 3D ICs based on 2D information?

Can you think of a nice way to cluster the design?

Do you have an opinion about IC manufacturing socio-ecological impact?