Clustering and Partitioning for 3D architectures

Research progress committee

September 2018

General problem statement

- How to enable 3D integration for existing 2D architectures?
- Why do we need to explore the 3D path? (Moore, Rock, pitch)

Specific problem statement

- Is there a way to tell if a design is fit to go 3D, just based on a preliminary analysis?
- The problem is twofold:
  - Partitioning
  - Clustering
- Reduce wirelength by bringing the gates closer to each other.

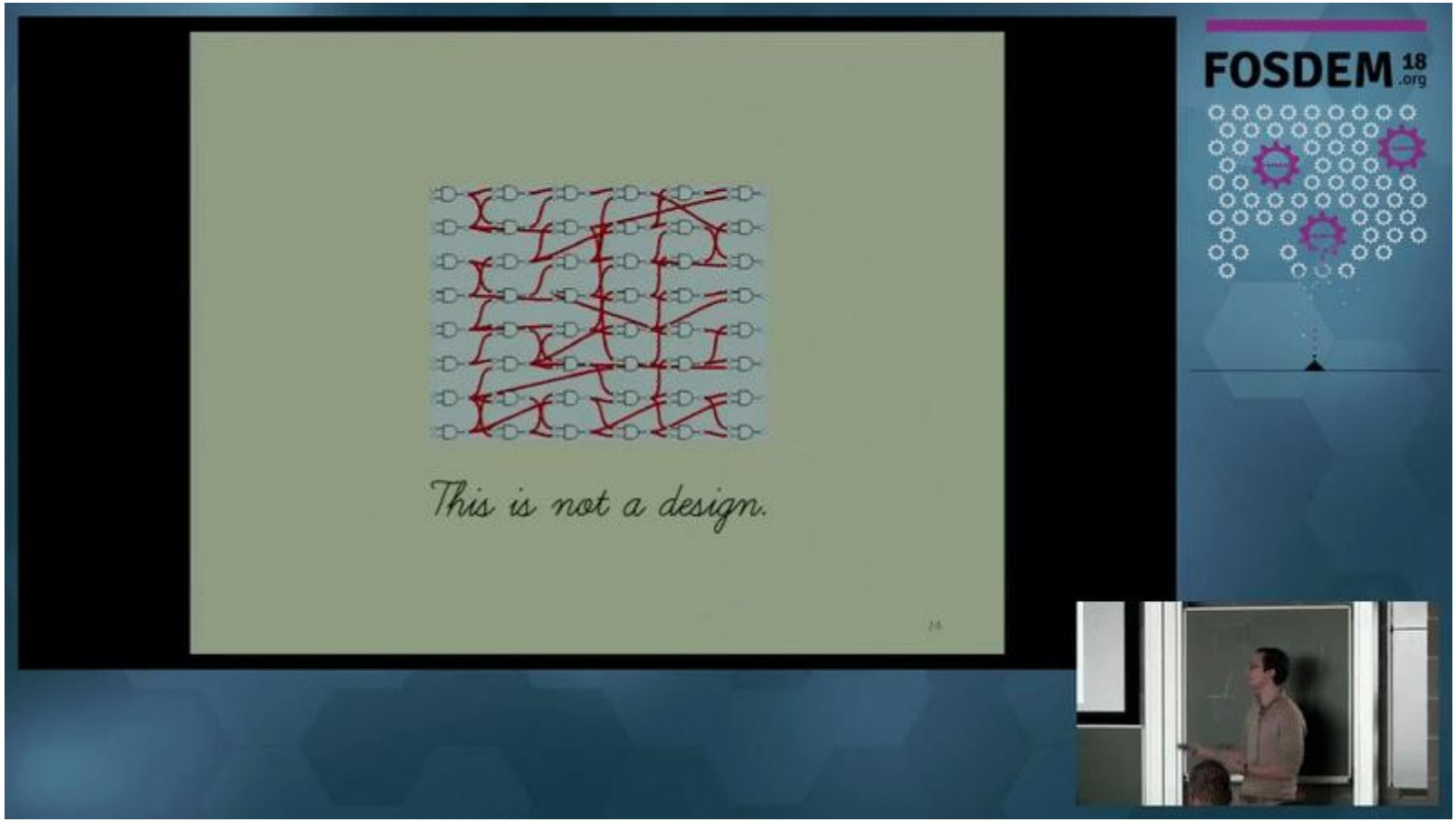
Past work overview

- Mincut
- Geometric clustering

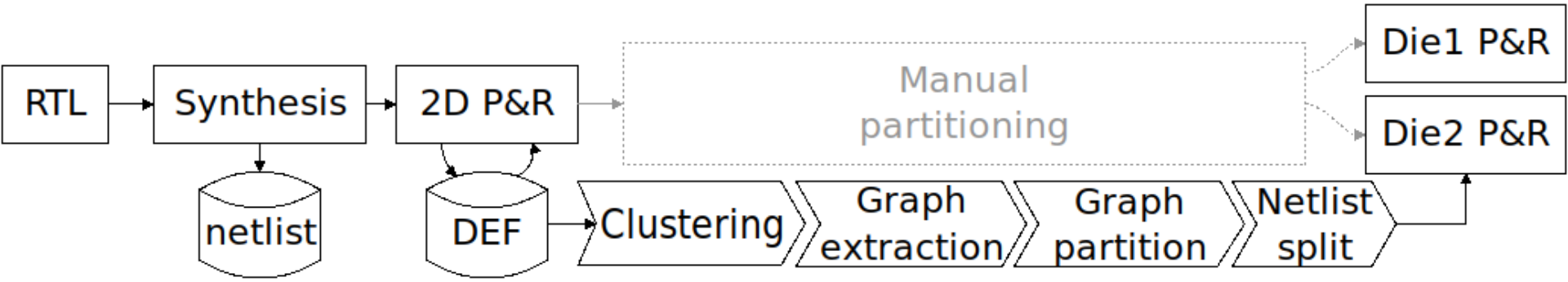
2017-2018 contributions and results

- Maxcut (circut)
- New clustering methods
  - Random
  - Progressive wire-length
  - Hierarchical geometric
- New reference design: LDPC 4x4, serial and full
- Partitionement arbitraire
- Amélioration des performances

Fosdem 2018



Automated 3D flow



ICECS 2018

- What kind of conference?
- “3D-Stacked Integrated Circuits: How Fine Should System Partitioning Be?”
- Notification of acceptance September 20th
- Venue: December 10th to 12th

Planning

- Maxcut on hypergraph
- Do we need to implement an algorithm?
- Design experiments to highlight the difference between graph and hypergraph partitioning paradigm
- K-way partitioning
- Progressive WL: find tiping point in term of % of max WL.