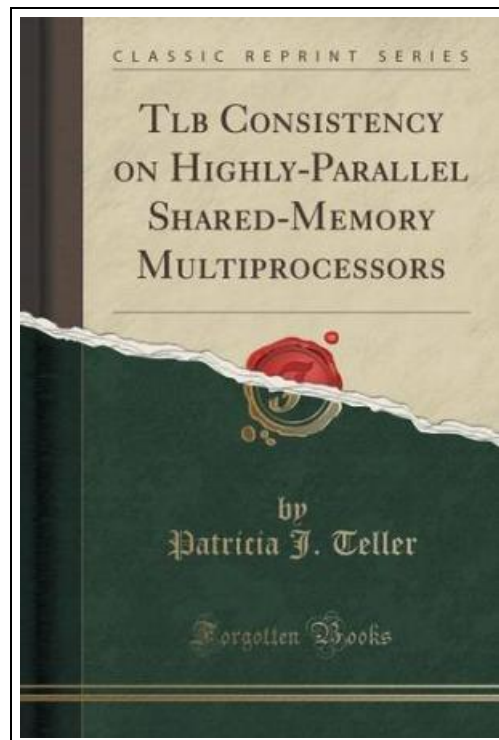


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Forgotten Books, United States, 2015. Paperback. Condition: New. Language: English . Brand New Book ***** Print on Demand *****. Excerpt from **Tlb Consistency on Highly-Parallel Shared-Memory Multiprocessors** Multiprocessors that store the same shared data in different private caches must ensure these caches have consistent copies. Almost all known solutions to this cache consistency problem are only suitable for architectures with a few tens of processors (PEs). Efficient solutions to the TLB (translation lookaside buffer) consistency problem, a special case of the cache consistency problem, can be found for highly-parallel, shared-memory multiprocessors (HPSMMs) with many hundreds of PEs for the following reasons: the number of references to address translation information per modification is very large; the cache for storing translation information can be present anywhere on the path from the PEs to memory; when the memory mapping needs to be modified, one can often select which translation information to change; and obsolete mapping information can be used until permanent changes must be made. We present three general methods that exploit these features and can be used on HPSMMs to maintain TLB consistency. Tradeoffs are discussed and are related to overall system performance. Some interesting issues inherent to the TLB consistency problem and the support of a demand-paged virtual memory system on a HPSMM are also presented. Our methods demonstrate the use of alternative implementations of the classical readers-writers algorithm. 1. Introduction To match the relatively high speed of the CPU with the relatively low speed of a large, modest-cost memory, most computer systems use a hierarchical memory, where higher levels are faster but smaller. By exploiting the principle of locality (4), the average delay for memory access is little more than that of the fastest level. Most parallel programs exhibit locality of reference to shared code and many exhibit significant locality...



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