CEG3155: DGD 3

Questions

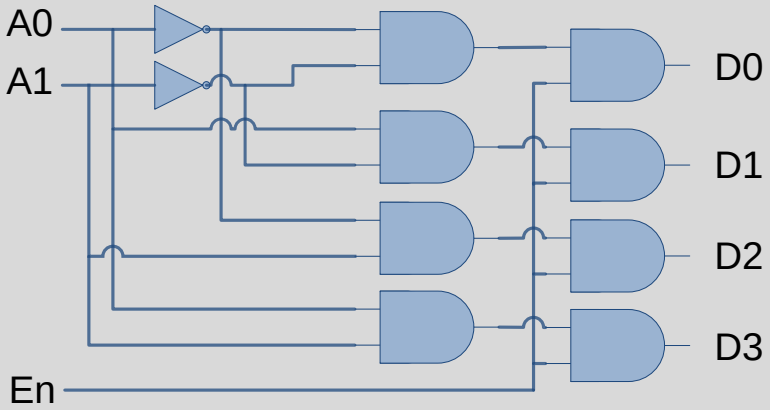
Question 1

a) Convert the structural VHDL code shown below into schematic.
b) Fill the truth table for the schematic from part a).

```
1  -- 2-to-4 Line Decoder; structural VHDL Description
2  library ieee;
3  use ieee.std_logic_1164.all
4
5  entity decoder_2_4_w_enable is
6      port(
7          EN, A0, A1 : in std_logic;
8          D0, D1, D2, D3 : out std_logic
9      );
10 end decoder_2_to_4_w_enable;
11
12 architecture structural1_1 of decoder_2_to_4_w_enable is
13     component NOT1
14         port(
15             in1: in std_logic;
16             out1: out std_logic
17         );
18     end component;
19
20     component AND2
21         port(
22             in1, in2: in std_logic;
23             out1: out std_logic
24         );
25     end component;
26
27     signal A0_n, A1_n, N0, N1, N2, N3: std_logic;
28     begin
29         g0: NOT1 port map (in1 => A0, out1 => A0_n);
30         g1: NOT1 port map (in1 => A1, out1 => A1_n);
31         g2: AND2 port map (in1 => A0_n, in2 => A1_n, out1 => N0);
32         g3: AND2 port map (in1 => A0, in2 => A1_n, out1 => N1);
33         g4: AND2 port map (in1 => A0_n, in2 => A1, out1 => N2);
34         g5: AND2 port map (in1 => A0, in2 => A1, out1 => N3);
35         g6: AND2 port map (in1 =>EN, in2 => N0, out1 => D0);
36         g7: AND2 port map (in1 => EN, in2 => N1, out1 => D1);
37         g8: AND2 port map (in1 => EN, in2 => N2, out1 => D2);
38         g9: AND2 port map (in1 => EN, in2 => N3, out1 => D3);
39 end structural_1;
40
```

EN	A1	A0	D0	D1	D2	D3

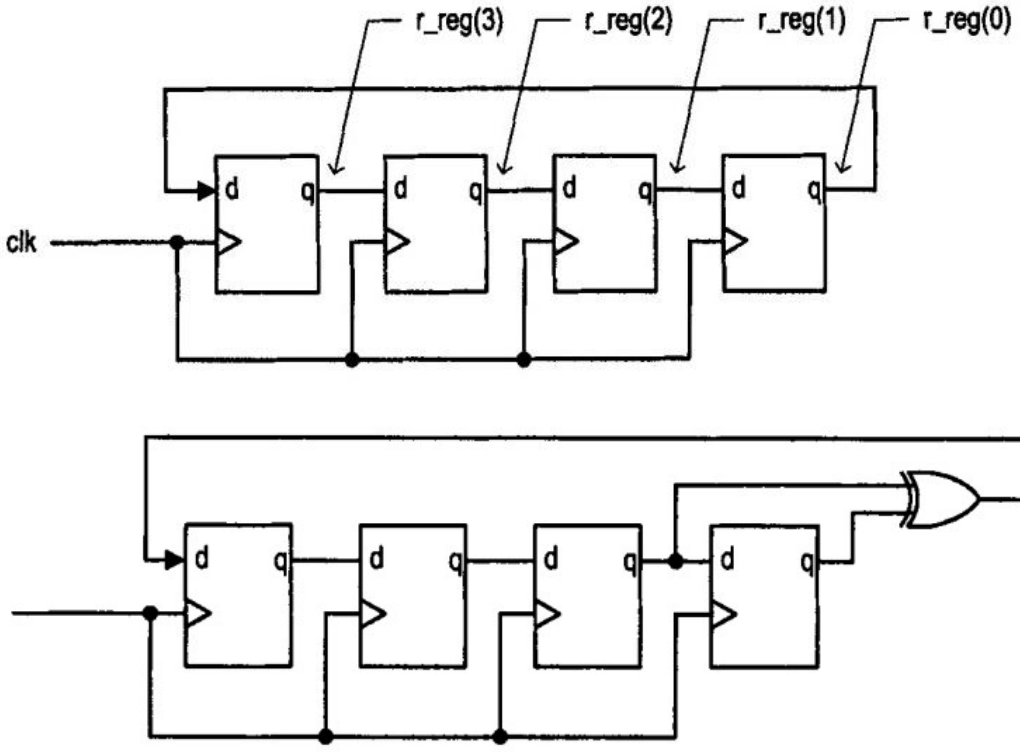
Solution



EN	A1	A0	D0	D1	D2	D3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Question 2

Assume the initial value of the counters is "1000". How many different states each counter performs?

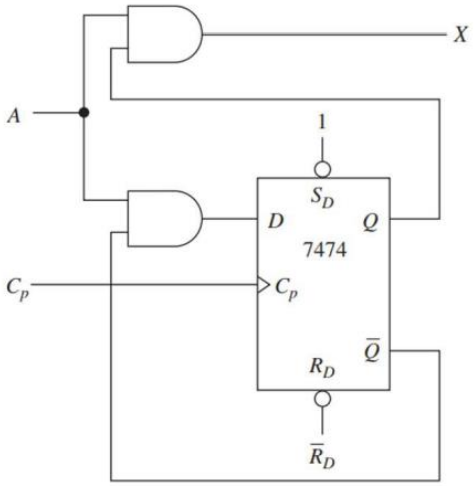


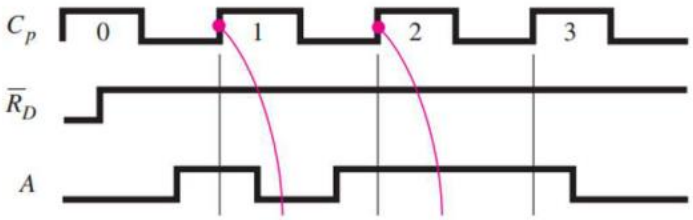
Solution

a) 1000 → 0100 → 0010 → 1001 → 1100 → 0110 → 1011 → 0101 → 1010 → 1101 → 1110 → 1111 → 0111 → 0011 → 0001 → **1000** (15 states).
b) 1000 → 0100 → 0010 → 0001 → 1000 (4 states).

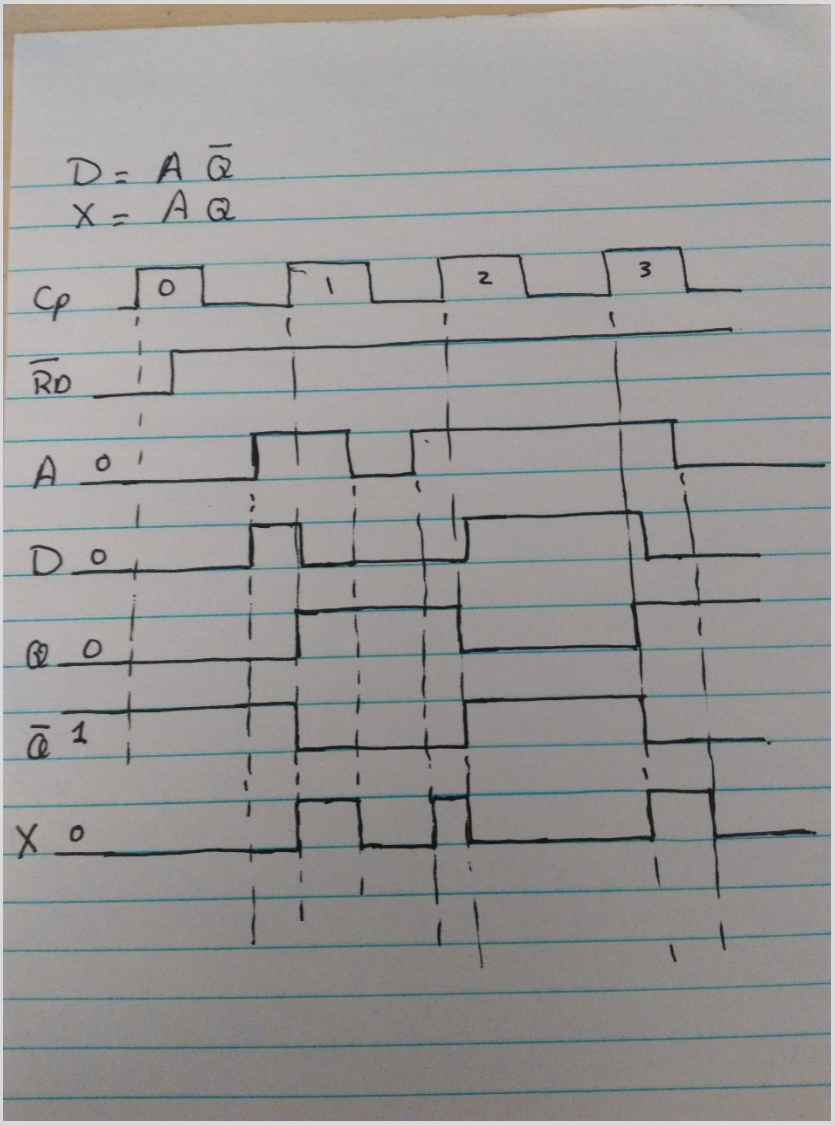
Question 3

The D flip-flop shown in figure below is a positive edge-triggered flip-flop. For given waveforms at the input, sketch D, Q and X.



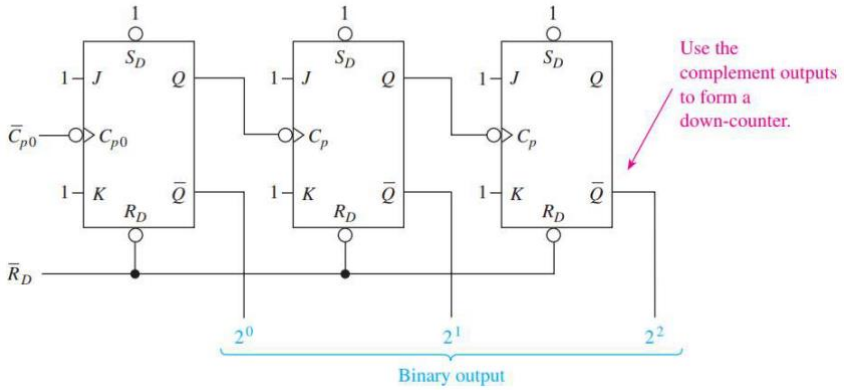


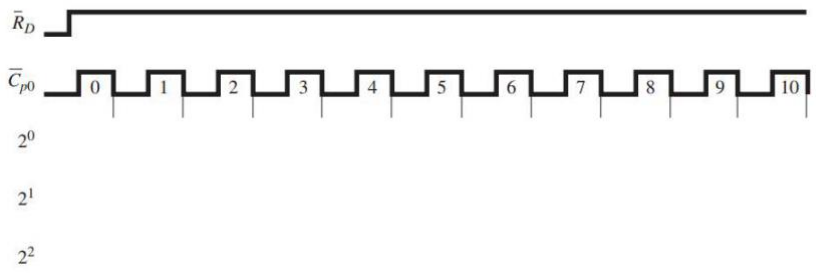
Solution



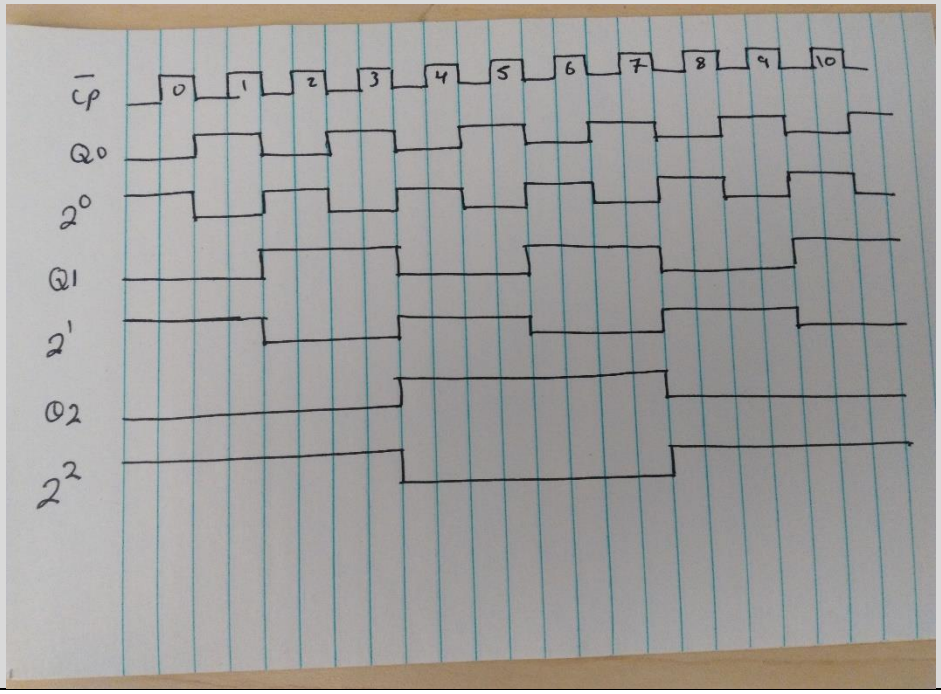
Question 4

Draw timing diagrams for the counter below:





Solution



Question 5 (Chu 4.6)

We wish to design a shift-left circuit manually. The inputs include a, which is an 8-bit signal to be shifted, and ctrl, which is a 3-bit signal specifying the amount to be shifted. Both are with the std_logic_vector data type. The output y is an 8-bit signal with the std_logic_vector data type. Use concurrent signal assignment statements to derive the circuit and draw the conceptual diagram.

Solution

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity shift_left is
5     port(
6        a: in std_logic_vector(7 downto 0);
7        ctrl: in std_logic_vector(2 downto 0);
8        y: out std_logic_vector(7 downto 0)
9     );
10 end shift_left ;
11
12 architecture beh_arch of shift_left is
13 begin
14    with ctrl select
15       y <= a                          when "000",
16            a(6 downto 0) & "0"        when "001",
17            a(5 downto 0) & "00"       when "010",
18            a(4 downto 0) & "000"      when "011",
19            a(3 downto 0) & "0000"     when "100",
20            a(2 downto 0) & "00000"    when "101",
21            a(1 downto 0) & "000000"   when "110",
22            a(0) & "0000000"           when others; -- 111
23 end beh_arch ;
```