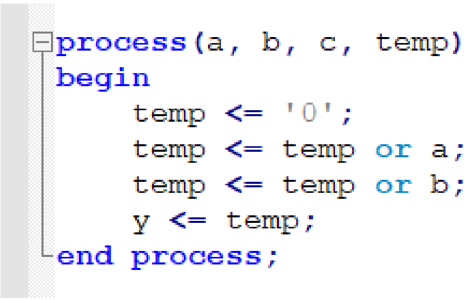
CEG3155: DGD 2

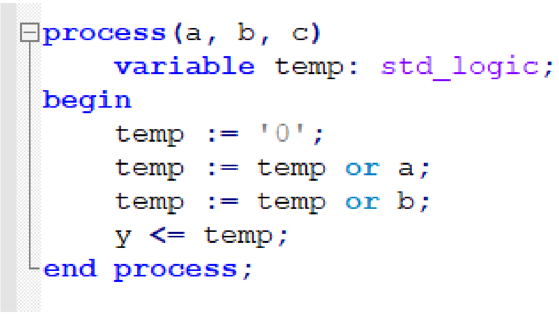
Questions

Question 1

Explain the difference in the output of these two pieces of code. Assume that a, b, c and y are signals. Temp is a signal in the code on the left and it is a variable in the code on the right.

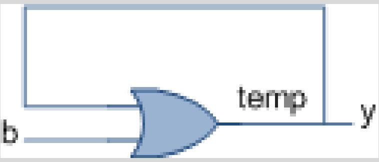


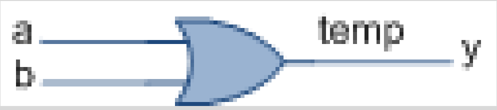
```
process(a, b, c, temp)
begin
    temp <= '0';
    temp <= temp or a;
    temp <= temp or b;
    y <= temp;
end process;
```



```
process(a, b, c)
    variable temp: std_logic;
begin
    temp := '0';
    temp := temp or a;
    temp := temp or b;
    y <= temp;
end process;
```

Solution





Question 2

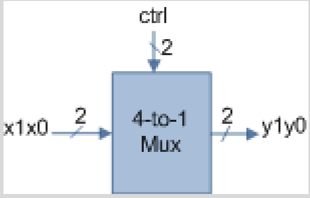
Consider a 2-by-2 switch. It has two input ports, x0 and x1, and a 2-bit control signal, ctrl. The input ports are routed to output ports y0 and y1 according to the ctrl signal. The function table is specified below.

a) Draw the conceptual diagram.
b) Use concurrent signal assignment statements to derive the circuit.

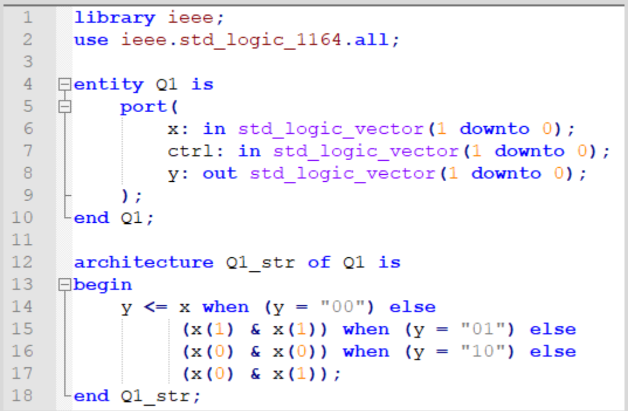
Input	**Output**	**Function**
ctrl	**y1 y0**	
00	x1 x0	Pass
01	x1 x1	Broadcast x1
10	x0 x0	Broadcast x0
11	x0 x1	Cross

Solution

a)



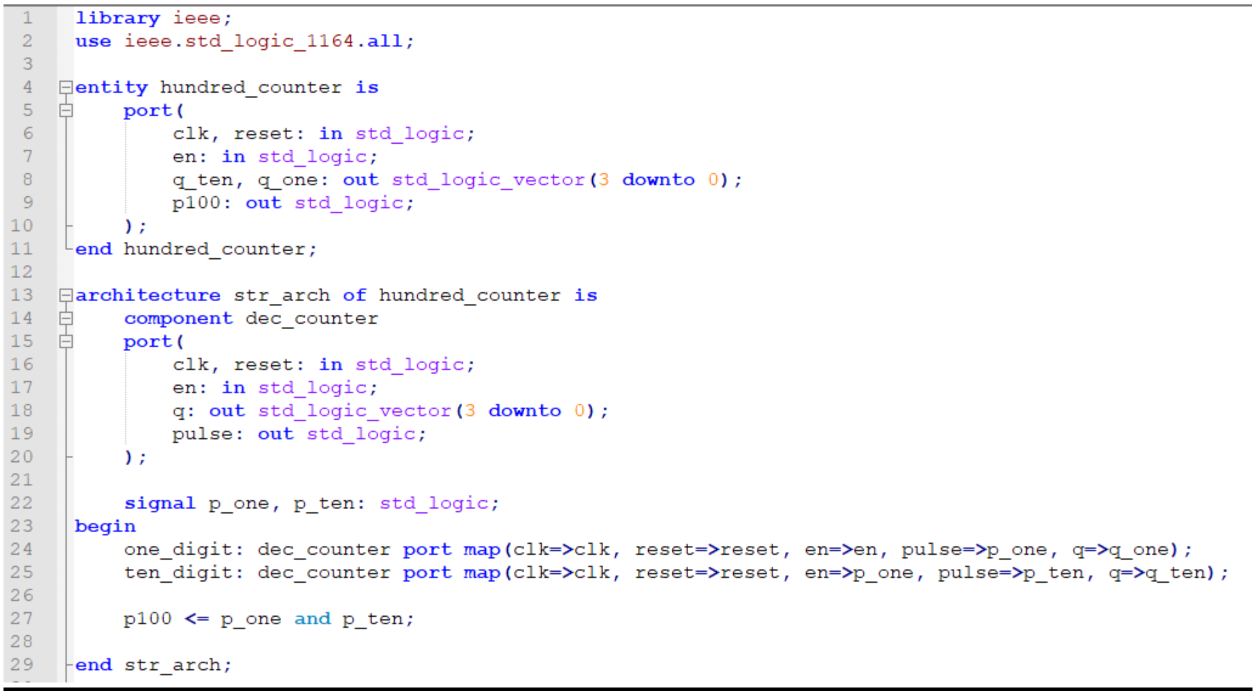
b)



```
library ieee;
use ieee.std_logic_1164.all;

entity Q1 is
    port(
        x: in std_logic_vector(1 downto 0);
        ctrl: in std_logic_vector(1 downto 0);
        y: out std_logic_vector(1 downto 0)
    );
end Q1;

architecture Q1_str of Q1 is
begin
    y <= x when (y = "00") else
         (x(1) & x(1)) when (y = "01") else
         (x(0) & x(0)) when (y = "10") else
         (x(0) & x(1));
end Q1_str;
```

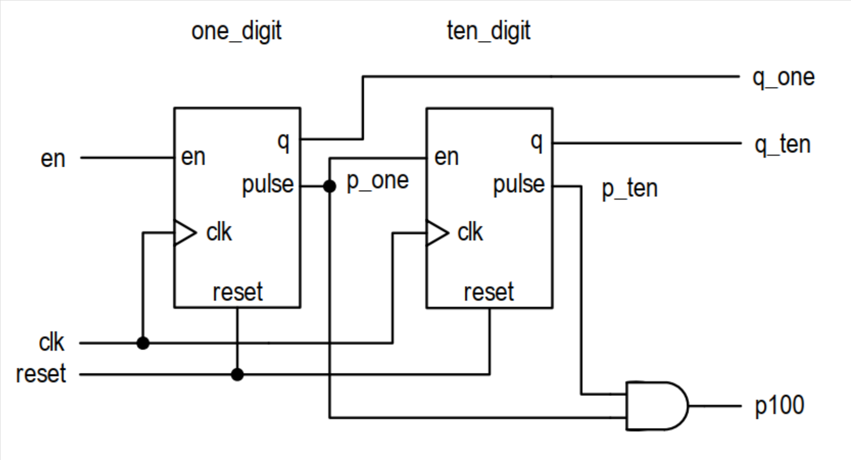
Question 3 (Problem 2.7)

The VHDL structural description of a circuit is shown below. Derive the block diagram according to the code.



```
library ieee;
use ieee.std_logic_1164.all;

entity hundred_counter is
    port(
        clk, reset: in std_logic;
        en: in std_logic;
        q_ten, q_one: out std_logic_vector(3 downto 0);
        p100: out std_logic;
    );
end hundred_counter;

architecture str_arch of hundred_counter is
    component dec_counter
    port(
        clk, reset: in std_logic;
        en: in std_logic;
        q: out std_logic_vector(3 downto 0);
        pulse: out std_logic;
    );

    signal p_one, p_ten: std_logic;
begin
    one_digit: dec_counter port map(clk=>clk, reset=>reset, en=>en, pulse=>p_one, q=>q_one);
    ten_digit: dec_counter port map(clk=>clk, reset=>reset, en=>p_one, pulse=>p_ten, q=>q_ten);

    p100 <= p_one and p_ten;

end str_arch;
```

Solution



Question 4 (Problem 3.7)

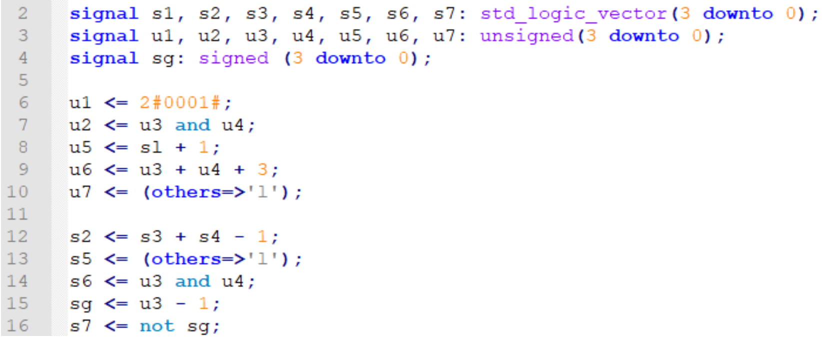
Assume that a and y are 8-bit signals with the std_logic_vector (7 downto 0) data type. We want to perform (a mod 8) and assign the result to y. Write a signal assignment statement using only the & operator.

Solution

$$y <= "00000"\ \&\ a(2\ downto\ 0);$$

Question 5 (Problem 3.11)

Determine whether the following signal assignment is syntactically correct. If not, use the proper conversion function and type casting to correct the problem.



```
signal s1, s2, s3, s4, s5, s6, s7: std_logic_vector(3 downto 0);
signal u1, u2, u3, u4, u5, u6, u7: unsigned(3 downto 0);
signal sg: signed (3 downto 0);

u1 <= 2#0001#;
u2 <= u3 and u4;
u5 <= s1 + 1;
u6 <= u3 + u4 + 3;
u7 <= (others=>'1');

s2 <= s3 + s4 - 1;
s5 <= (others=>'1');
s6 <= u3 and u4;
sg <= u3 - 1;
s7 <= not sg;
```

Solution

use ieee.numeric_std.all;

Wrong: u1 <= 2#0001#;
u1 <= "0001";

Wrong: u2 <= u3 and u4;
u2 <= unsigned(std_logic_vector(u3) and std_logic_vector(u4));

Wrong: u5 <= s1 + 1;
u5 <= unsigned(s1) + 1;

Wrong: s2 <= s3 + s4 -1;
s2 <= std_logic_vector((unsigned(s3) + unsigned(s4) - 1));

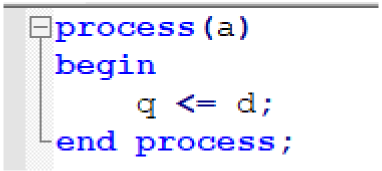
Wrong: s6 <= u3 and u4;
s6 <= std_logic_vector(u3) and std_logic_vector(u4);

Wrong: sg <= u3 - 1;
sg <= signed(u3) - 1;

Wrong: s7 <= not sg;
s7 <= not std_logic_vector(sg);

Question 6 (Problem 5.1)

Consider a circuit described by the following code segment:



```
process(a)
begin
    q <= d;
end process;
```

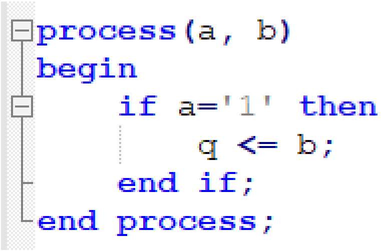
a) Describe the operation of this circuit.
b) Does this circuit resemble any real physical component?

Solution

a) When 'a' changes, 'q' takes the value of 'd', and keeps the value otherwise.
b) The circuit functions like the D-FF. However, it changes with both edges of 'a', while the D-FF changes with either rising or falling edge of the clock.

Question 7 (Problem 5.2)

Consider the following code segment:



```
process(a, b)
begin
    if a='1' then
        q <= b;
    end if;
end process;
```

a) Describe the operation of this circuit.
b) Draw the conceptual diagram of this circuit.

Solution

a) When a is '1', q takes the value of b. If a is '0', q keeps its previous value.

b)