CEG3155: DGD 8

Question 1

Let the propagation delay of an xor cell be 4 ns, and the setup time and clock-to-q delay of the register be 2 and 3 ns respectively. Determine the maximum clock frequency of a 4-bit LFSR.

Question 2 (Chu 8.11)

Consider the block diagram of the decade counter in Figure 8.13. Let T_{cq} and T_{setup} of the DFF be 1 and 0.5 ns, and the propagation delays of the incrementor, comparator and multiplexer be 5, 3 and 0.75 ns respectively. Assume that no further optimization will be performed during synthesis. Determine the maximal clock rate.

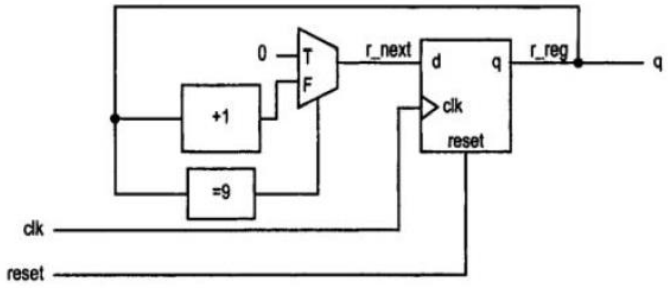
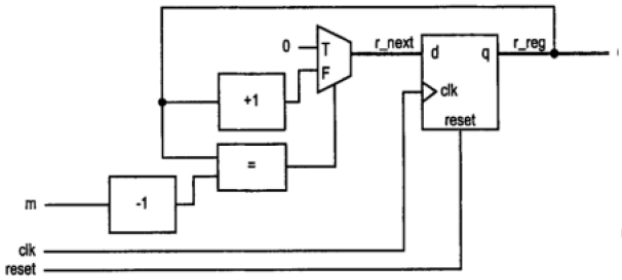


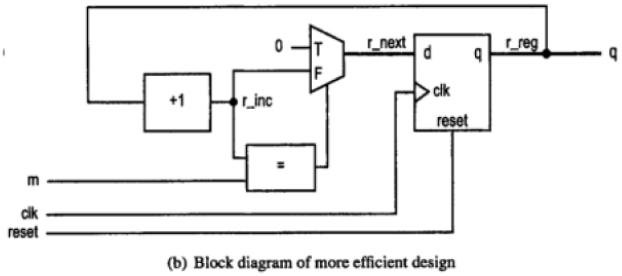
Figure 8.13 Conceptual diagram of a decade counter.

Question 3 (Chu 8.12)

Consider the two block diagrams of the programmable mod-m counter in Figure 8.14. Assume that no further optimization will be performed during synthesis. Use the timing information in Problem 8.11 to determine the maximal clock rates of the two configurations.



(a) Block diagram of initial design



(b) Block diagram of more efficient design

Question 4

Odd/Even Parity Detector

Consider a logic circuit that counts the number of ones in a bit serial input stream. If the circuit asserts its output when the input contains an odd number of ones, it is called odd parity. If it asserts its output when the input contains an even number of ones, it is called even parity. Use FSM to design an odd parity detector circuit.

Question 5

Blinking light

This problem concerns a circuit that must turn a light on and off, remaining on during T1 clock periods and off during T2 clock periods. An important desired feature is that when the circuit is enabled it must start from a state with the light on (to prevent the user from thinking that the circuit is not working when large transition times are involved).

a) Design the FSM.
b) Write a VHDL to describe the operation of the circuit.