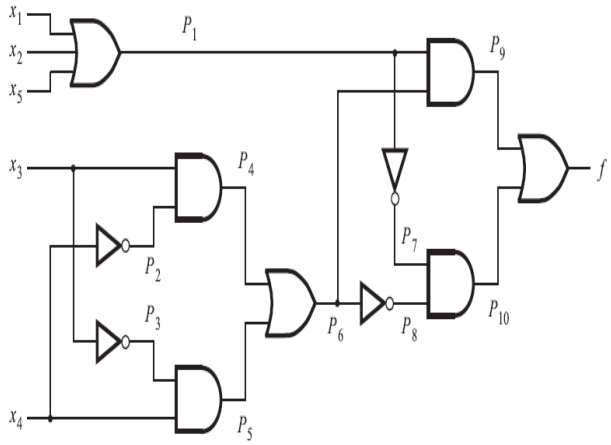
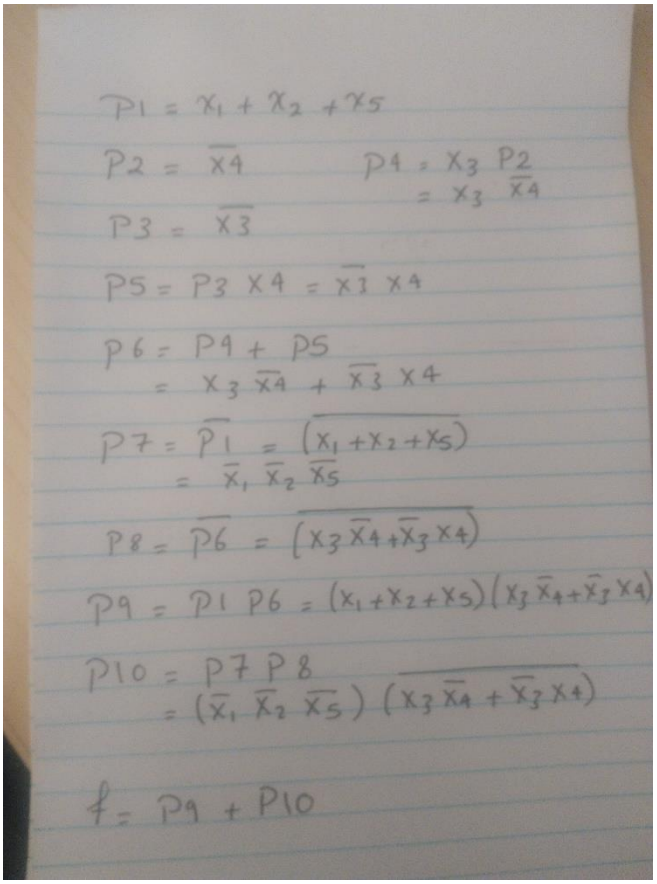
CEG3155: DGD 6

Solution of Quiz

Question1: For the circuit shown in Figure 1, write the expression of the output signal ***f***.





Question 2:

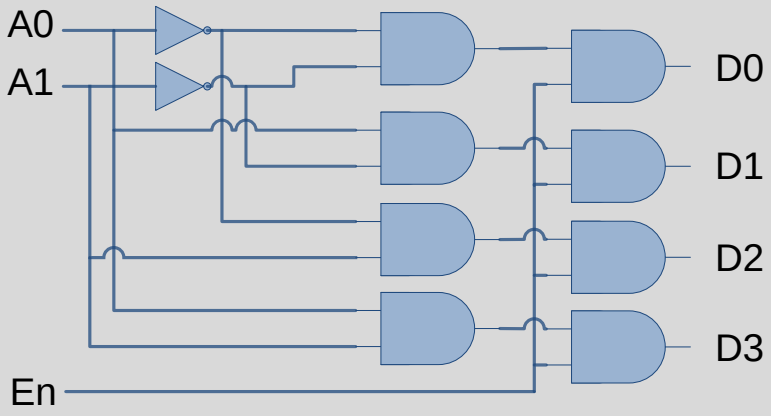
a) Convert this structural VHDL code into schematic (similar problem and its block diagram are shown in Figure 2 on page 3 for even-parity detector).

```
1  -- 2-to-4 Line Decoder; structural VHDL Description
2  library ieee;
3  use ieee.std_logic_1164.all
4
5  entity decoder_2_4_w_enable is
6      port(
7          EN, A0, A1 : in std_logic;
8          D0, D1, D2, D3 : out std_logic
9      );
10 end decoder_2_to_4_w_enable;
11
12 architecture structural1_1 of decoder_2_to_4_w_enable is
13     component NOT1
14         port(
15             in1: in std_logic;
16             out1: out std_logic
17         );
18     end component;
19
20     component AND2
21         port(
22             in1, in2: in std_logic;
23             out1: out std_logic
24         );
25     end component;
26
27     signal A0_n, A1_n, N0, N1, N2, N3: std_logic;
28     begin
29         g0: NOT1 port map (in1 => A0, out1 => A0_n);
30         g1: NOT1 port map (in1 => A1, out1 => A1_n);
31         g2: AND2 port map (in1 => A0_n, in2 => A1_n, out1 => N0);
32         g3: AND2 port map (in1 => A0, in2 => A1_n, out1 => N1);
33         g4: AND2 port map (in1 => A0_n, in2 => A1, out1 => N2);
34         g5: AND2 port map (in1 => A0, in2 => A1, out1 => N3);
35         g6: AND2 port map (in1 =>EN, in2 => N0, out1 => D0);
36         g7: AND2 port map (in1 => EN, in2 => N1, out1 => D1);
37         g8: AND2 port map (in1 => EN, in2 => N2, out1 => D2);
38         g9: AND2 port map (in1 => EN, in2 => N3, out1 => D3);
39 end structural_1;
40
```

b) Fill the truth table for the schematic from part a)

Solution

The conceptual diagram can be using logic gates or blocks that indicate the type of gate. Both solutions are correct.



EN	A1	A0	D0	D1	D2	D3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Chapter 6

Question 1 (Chu 6.3)

One way to specify a combinational circuit is to describe its function by a truth table, in which we list all possible input combinations and their desired output values. Assume that the circuit has n inputs.

a) What is the size (number of the rows) of the table?
b) What is the problem with this approach?

Solution

a) 2^n
b) The number of rows grows exponentially.

Question 2 (Chu 6.4)

Assume that a and b are 3-bit inputs (let a be $a_2a_1a_0$ and b be $b_2b_1b_0$).

a) Determine the Boolean expression for the relational operation a > b.
b) Assume that b is a constant and that b = "101". Determine the Boolean expression again.
c) Assume that a is a constant and that a = "101". Determine the Boolean expression again.

Solution

a) $a_2b_2' + (a_2 \oplus b_2)'\, a_1b_1' + \ (a_2 \oplus b_2)'(a_1 \oplus b_1)'a_0b_0'$
b) $a_2\, a_1$
c) $b_2' + \ b_0'\, b_2\, b_1'$