CEG3155: DGD 7

Chapter 7

Question 1 (Chu 7.1)

Consider an arithmetic circuit that can perform four operations: (a+b), (a-b), (a+l) and (a-1), where a and b are 16-bit unsigned numbers and the desired operation is specified by a 2-bit control signal, ctrl.

a) Design the circuit using two adders, one incrementor and one decrementor. Derive the VHDL code.
b) Design the circuit using only one adder. Derive the VHDL code.

Question 2 (Chu 7.2)

Design a circuit that converts an 8-bit signed input to 8-bit sign-magnitude output (where the MSB is the sign bit and the remaining 7 bits are magnitude). Use a minimal number of relational and arithmetic operators in your design. Draw the top-level diagram and derive the VHDL code.

Question 3 (Chu 7.4)

Consider a 16-bit shifting circuit that can perform rotating right or rotating left. Use selected signal assignment statements to implement the shifting function.

a) Design the circuit using one rotate-right circuit, one rotate-left circuit and one 2-to-1 multiplexer to select the desired result. Derive the VHDL code.
b) Design the circuit using one rotate-right circuit with a pre- and post-processing reversing circuit. The reversing circuit either passes the original input or reverses the input bit-wise (e.g., if a 4-bit input $a_3a_2a_1a_0$ is used, the reversed output becomes $(a_0a_1a_2a_3)$). Derive the VHDL code.

Question 4 (Chu 7.8)

Design a 16-bit rotate-left shifting circuit using the multilevel structure discussed in Section 7.4.4.

Example (Section 7.4.4):

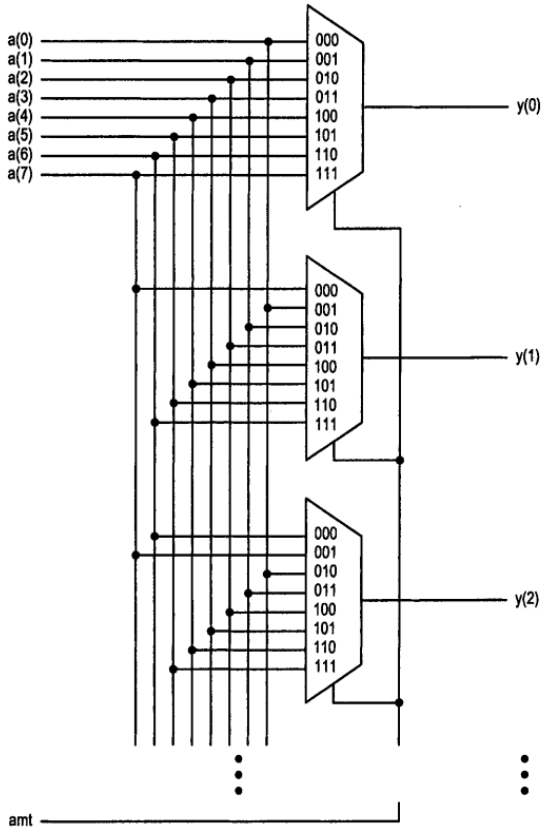
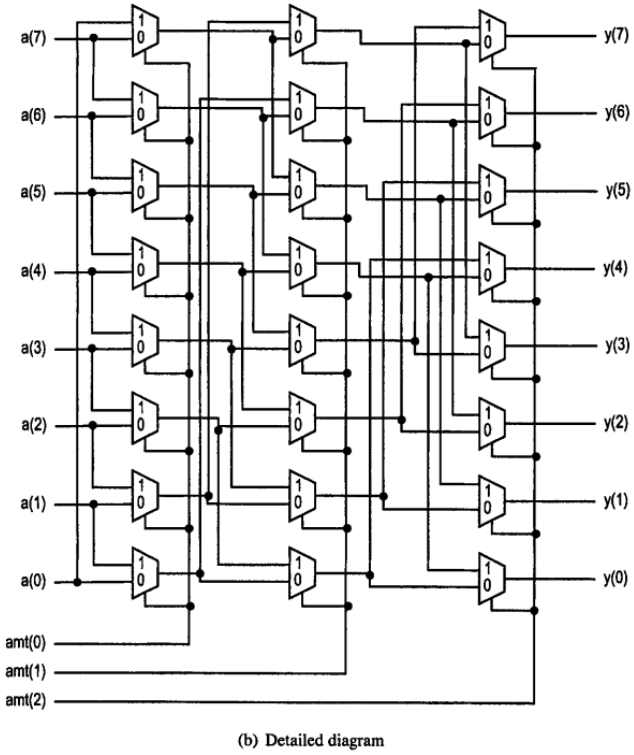
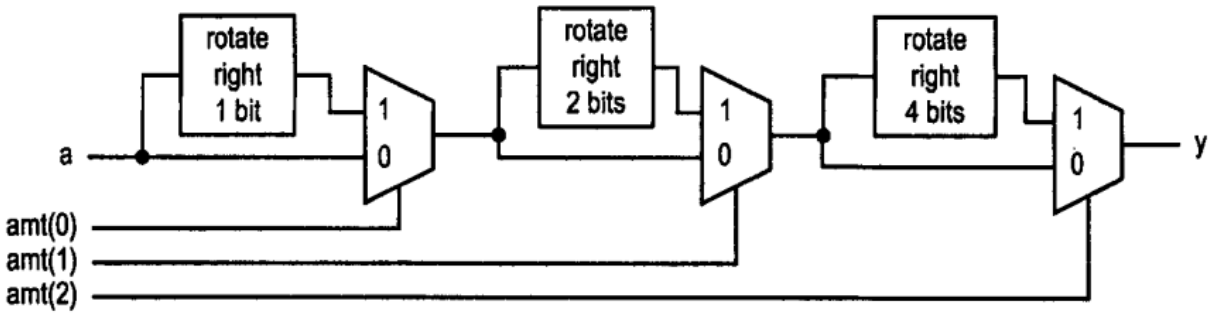


Figure 7.11 Barrel shifter using a single level of 8-to-1 multiplexers.



(b) Detailed diagram

Figure 7.12 Barrel shifter using three levels of 2-to-1 multiplexers.



(a) Block diagram