**CEG3155 Digital systems II**

**Lab2**

**Chapter 2 (HDL Based Designs)**

**Chapter 3 (Hierarchical Design)**

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**University of Ottawa**

**Faculty of Engineering**

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**Student Number:**

**Purpose of the lab:**

Chapter 2

• to understand the basic structure of a VHDL description;

• to model a simple digital circuit in VHDL;

• to follow the VHDL design flow;

• to simulate and test a digital circuit designed in VHDL;

• to prototype a circuit described in VHDL, using an FPGA board

Chapter 3

• to identify and comprehend the use of components in VHDL;

• to understand the concept of hierarchical design, and its implementation in VHDL;

• to add a component to the proposed case study;

• to simulate and test both, the original and the modified version of the case study;

• to prototype the case study using an FPGA board.

**Equipment and supplies:**

* + **Quartus II (web edition)**
  + **Model Slim**
  + **Altera DE2-115 Board with USB Slater**
  + **Probe**
  + **Coaxial cable**
  + **Ribbon cable**
  + **Wires**

**Theoretical PART**

**1. Presentation of the lab problem in a nutshell:**

Create the half-adder circuit shown in Fig. 2.3 using the VHDL design entry editor;

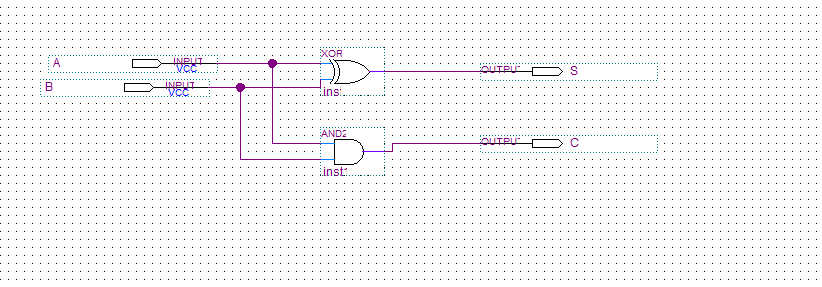
• Perform the synthesis;

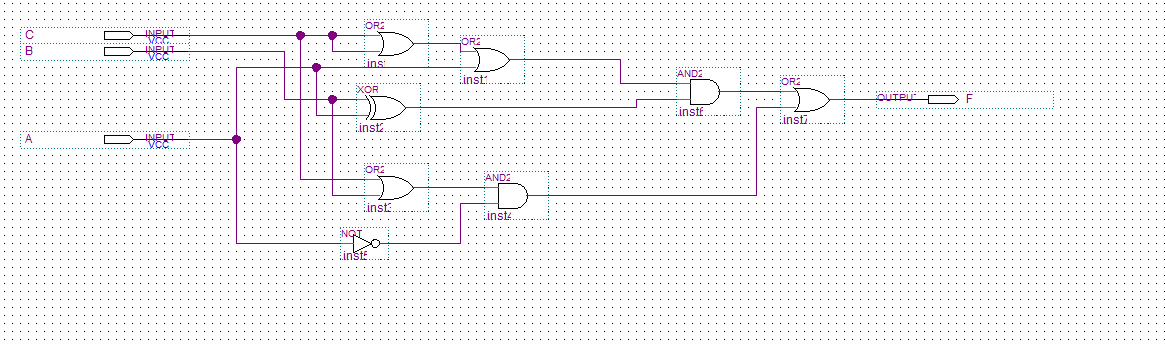
• Fix simulation and synthesis errors;

• Prototype and test the half-adder circuit in the FPGA board

And complete component C3 and its port mapping.

**DESIGN PART**





1. **Presentation of the design for C3**

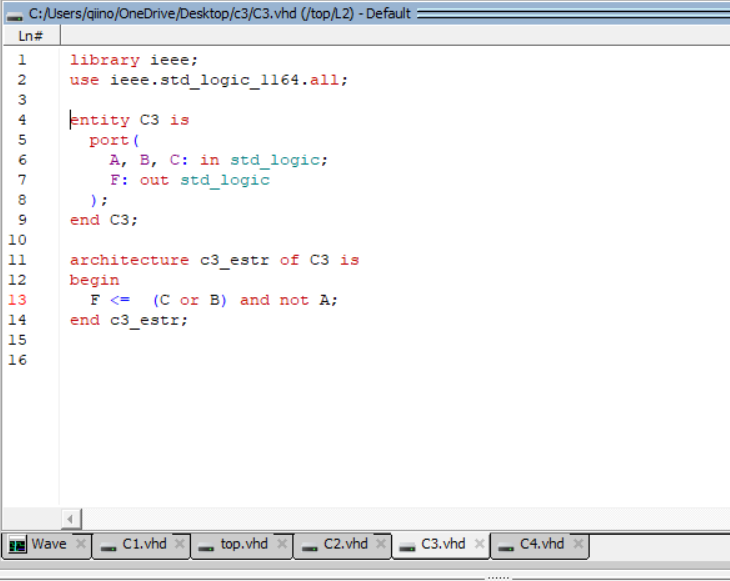
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Figure1: screenshot of C3.vhd

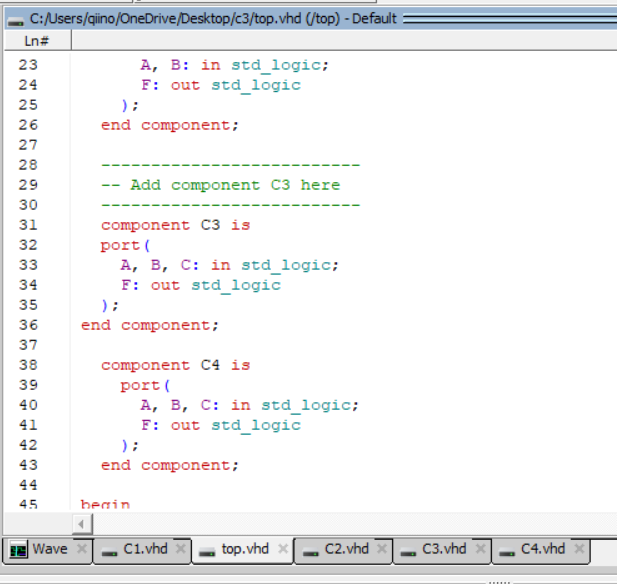
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Figure2: screenshot of top.vhd

**Simulation and Verification Part**

1. **Shown simulation/synthesis results for PARTI**

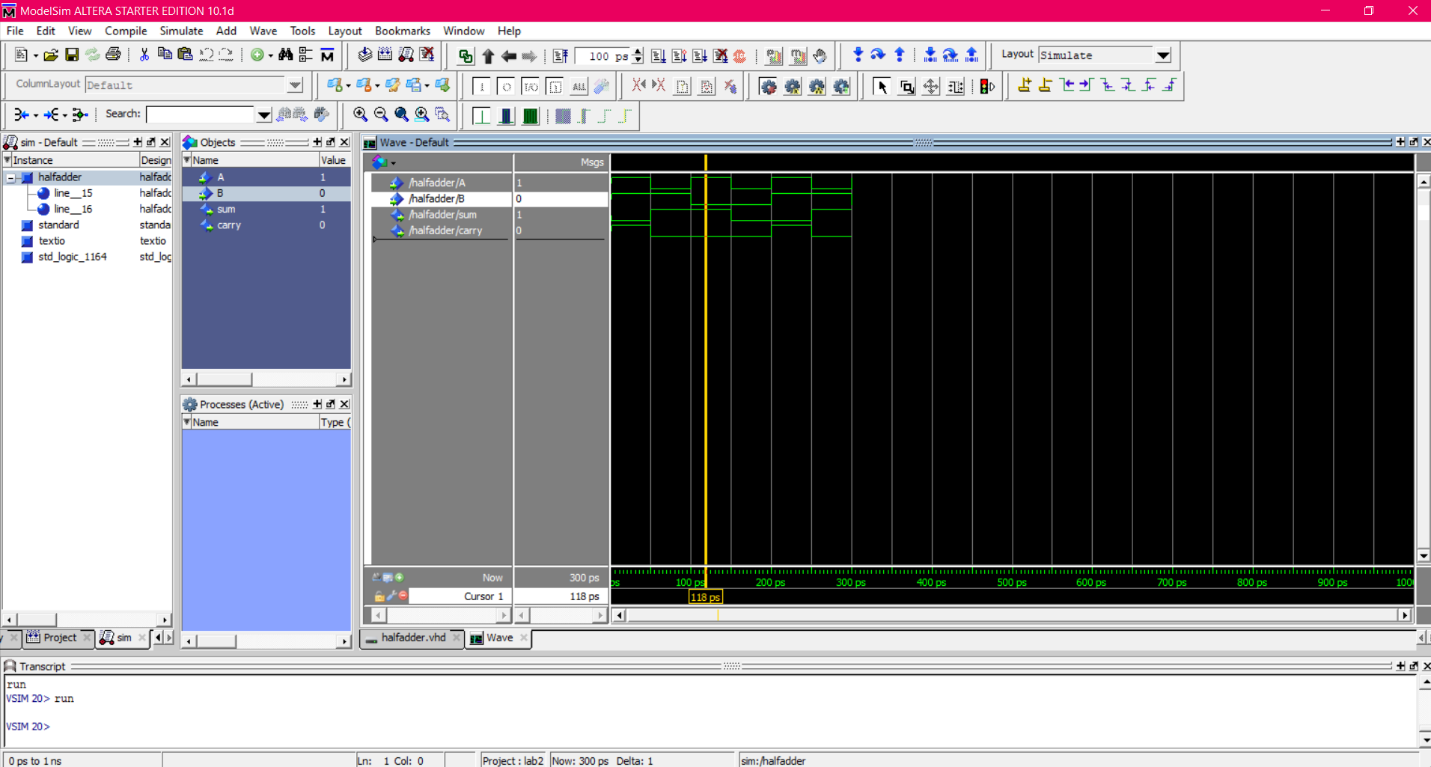
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Figure 3: Screenshot of the waveform for the PART I

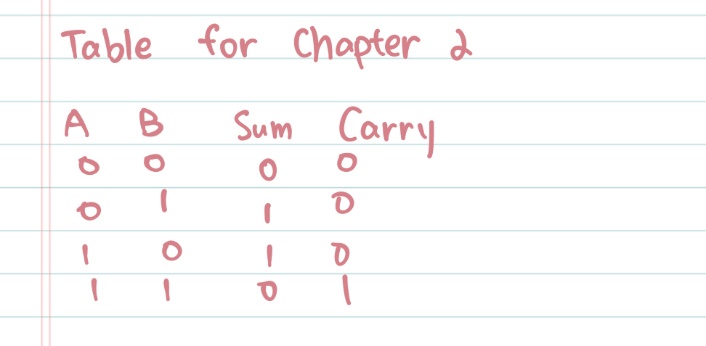
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Table1:Test cases of half adder

**2. Shown simulation/synthesis results for PART II**

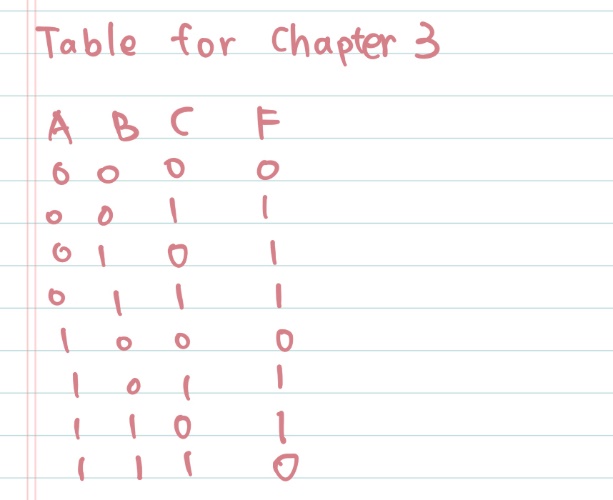
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Table 2: Test cases

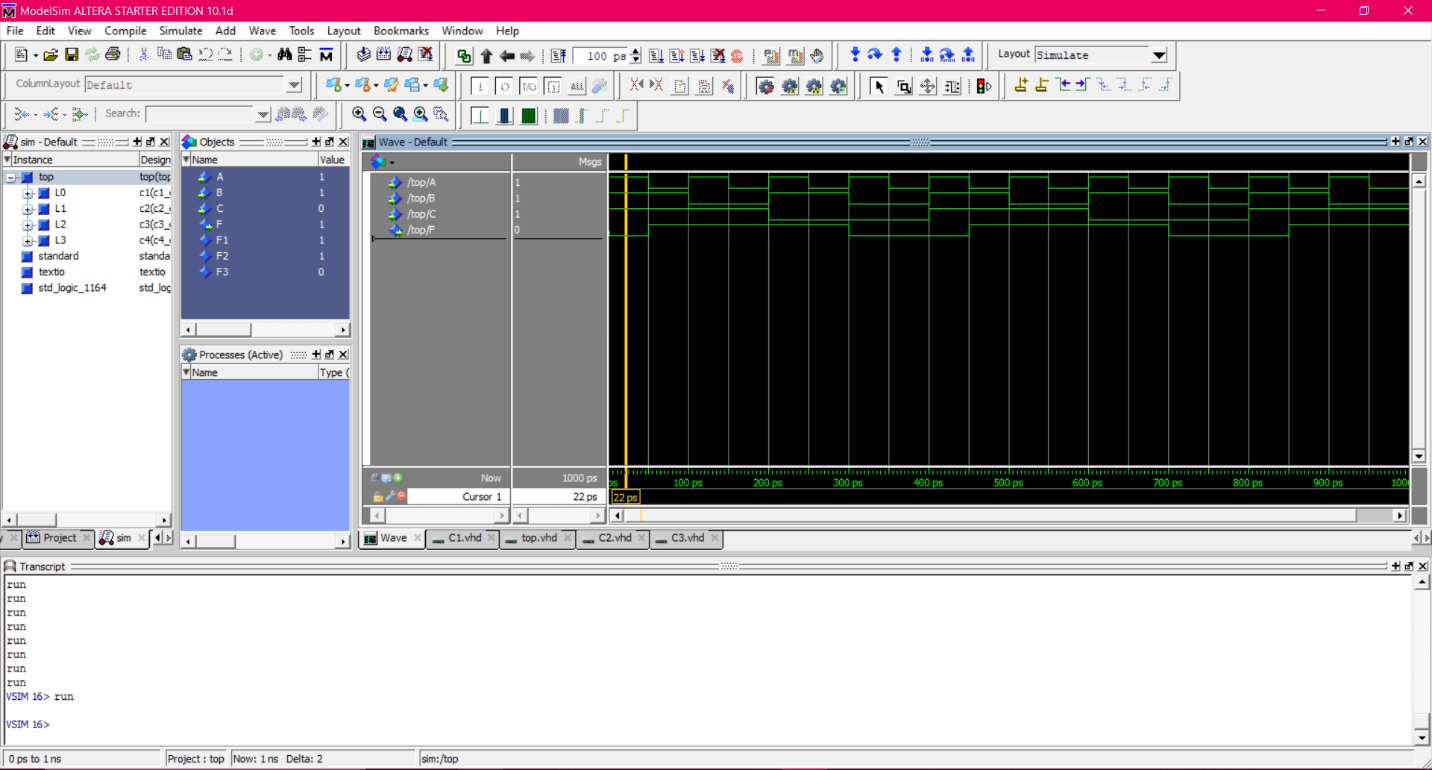
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Figure 4: Screenshot of the waveform for the PART II

Comment:

After it shows successful, checked with the prelab results. All of the inputs and output matches. In all, theoretical data matches experimental data and laws had been verified. Everything worked as expected.

**Discussion and Conclusions**

The design on the task was implemented on Model Slim software and Quartus II software. The results of outputs are as expected. From this lab, student can gain understanding of a complete FPGA design flow and VHDL language. Giving a briefly review of the Model slim and Quartus II software and practicing the knowledge learnt in class were the main point of this lab. During the lab, there are a few problems occurred while compiling the project on Quartus II and they were managed to be solved by asking for help from teaching assistance and following the instructions carefully.