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Soft Error Mechanisms, Modeling and Mitigation

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To
My Wife,
Neziha Cufadar

Preface

With advances in CMOS technology, nanometer circuits are increasingly becoming more sensitive to soft errors caused by single event particles. Most textbook published in the area considered single event transients (SET) as the main cause of radiation-induced transient failure of combinatorial circuits. This book provides the reader with new knowledge on various radiation soft error mechanisms that are not mentioned in similar textbooks. These mechanisms include soft delays, radiation-induced clock jitter and pulses, and single event (SE) coupling noise and delay effects.

The text discusses various hardening techniques for combinational logic, and describes two mitigation techniques in detail: "dynamic threshold technique" and "transmission gate technique with varied gate and body bias."

Hardening techniques developed for combinational logic have long ignored interconnect coupling effects. Hence, various mitigation strategies to eliminate SE coupling effects are also discussed.

As technologies advance, the coupling effects increasingly cause SE transients to contaminate electronically unrelated circuit paths which can in turn increase the "Single Event Susceptibility" of CMOS circuits. In order to complement the soft error hardening process, coupling effects among interconnects need to be considered in the single event hardening and analysis of CMOS logic gates due to technology scaling effects. Hence, after identifying the contribution of SE coupling on single event error rate, the text focuses on the modeling of SE crosstalk noise, delay, and speedup effects and presents closed-form expressions for single event crosstalk noise, delay, and speedup effects.

Another aspect looked at in this text is the reliability of low-power energy-efficient designs. As designers address leakage power consumption via optimizations, they need to be aware of the impact on soft error robustness. Clever design choices need to be made that reduce static power consumption and improve soft error reliability at the same time. An analysis is presented on some power optimization techniques and strategies on good design choices are given.

Contents

Chapter 1
Introduction

The International Technology Roadmap for Semiconductors (2013 Edition) has identified signal integrity in chips as one of the major challenges [1]. Transient errors created by voltage drops in power supply, signal cross-coupling effects, and terrestrial radiation cause increasing reliability issues and compromise the security in unpredictable ways.

Due to the shrinking of feature size and reduced noise margins, nanoscale circuits have become increasingly more susceptible to interferences coming from these multiple noise sources. Among these noise sources, radiation-induced soft errors in commercial nanometer CMOS technologies have become a growing concern [2].

Soft errors in memory have been a very well studied problem at terrestrial level [3]. However, due to increasing clock frequencies and diminishing device sizes, soft errors are now increasingly affecting CMOS logic. For 45 nm technologies and below, researchers has predicted that the majority of the observed radiation induced soft errors will be due to transients that will occur in combinational logic (CL) circuits [2].

As scaling of today's process technologies continues, circuits become increasingly become more vulnerable to radiation-induced soft errors in nanoscale CMOS technologies. The reduced node capacitances, supply voltages coupled with increasingly denser chips are raising soft error rates and making them an important design issue. Increasing clock frequencies also increase circuit vulnerabilities to these transients as the chance to capturing these transients also increases.

1.1 Terrestrial Radiation Sources, Single Event Transients and Soft Error Generation

At ground level, soft errors are mainly induced by alpha particles emitted from trace radioactive impurities in the device materials, interaction of low-energy thermal neutrons with certain boron isotopes in the device, and reaction of high-energy cosmic neutrons (>1 MeV) with silicon and other device materials.

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Neutron induced soft errors are generated by secondary charged particles which are created in neutron-silicon atom collisions. Since a neutron does not carry any charge, it does not induce ionization by itself in silicon [3]. When high energy neutrons strike an integrated circuit, some neutrons pass through without affecting operations of the semiconductor device, but some neutrons collide with nuclei in the silicon lattice [4, 5]. The result of this interaction is the creation of secondary particles, which in turn create a trail of electron–hole pairs. Although alpha particles are directly ionizing, the energy of the secondary ions produced by high-energy neutron reactions can be much higher than that of alpha particles [6].

The alpha particles are emitted mostly due to radioactive decay of uranium and thorium impurities located within the chip packaging. Linear Energy Transfer (LET) is the measure of energy that is transferred in the material when an ionizing particle passes through it. Most alpha particles have energies of between 3 and 7 MeV (mega or million electron-volts). Since it takes only about 3.6 eV to generate an electron–hole pair in the substrate, a 4 MeV alpha particle striking the sensitive node within a combinational logic (CL) can generate more than a million electron hole pairs within its particle track due to ionization mechanism (Fig. 1.1). The sensitive areas mentioned here are usually the depletion regions of transistor drains or reverse-biased p-n junctions. These would include the drain/well and drain/substrate junctions in CMOS transistors.

Under the electric field, these free carriers can drift creating a transient current pulse. The current later results in a charge collection at the struck electric node. It has been shown that the transient current consists of a fast drift and funnelling component and a slower contribution from charge diffusion in the silicon substrate.

The amount of the charge collected at a particular node (Q_{col}), depends on various parameters such as device size, bias conditions, doping level, characteristics of the particle hit, and its trajectory. The collected charge results in a voltage transient at the struck node. This transient, also named as Single Event Transient (SET), can travel through a series of logic gates and finally may reach to a storage element under certain conditions. If the generated pulse arrives at the storage

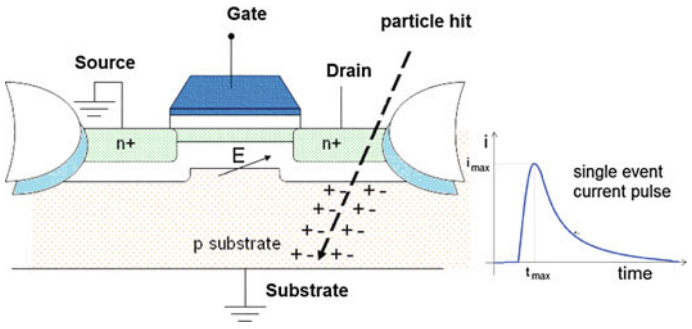

Fig. 1.1 Transient current pulse generation due to particle hit on sensitive node

element during its latching window, incorrect data can be stored resulting in soft error or a Single Event Upset (SEU).

When the collected charge Q_{col} at a given node exceeds the critical charge Q_{crit} of that node, the generated SET then can propagate and may reach to storage elements under certain conditions. In its simplest term, critical charge of a node is defined as $Q_{crit} = C_{node} * V_{DD}/2$, where C_{node} is the node capacitance. It is usually assumed that a glitch amount reaching half the power supply voltage can propagate through the receiver gate.

There are three masking effects that can prevent soft error generation: electrical, logical and temporal masking effects. In order for an SET to end up in a soft error:

- The transient pulse generated should have sufficient amplitude and width such that it propagates along the succeeding gates without significant attenuation. Hence, electrical masking should not be present.
- The logic path the pulse takes should be enabled by logic inputs. In another words, there should not be any logical masking.
- The latching clock edge should be present during the presence of the SET pulse at the input of the storage element. This means no temporal masking should exist.

Figure 1.2 below shows all these criteria have been satisfied: i.e. first a sufficient transient pulse is generated at particle site such that it propagates through many stages without any attenuation. There is no logical masking as the second input of NOR gate is tied to logic 0. The pulse arrives during latching edge of the clock pulse; finally soft error is generated due to absence of temporal masking.

Unfortunately, all these masking effects are gradually diminishing with newer generation technologies. With scaling down of devices, the node capacitances reduce, and as a result, electrical masking effects are less due to reduced critical charge. In newer designs, the SET pulses are very comparable to logic pulses. Logical masking is less effective as the logic depth in CL reduces in newer technologies. Temporal masking also reduces as increasing clock frequencies increase the chance of a latching edge being present for registering the data.

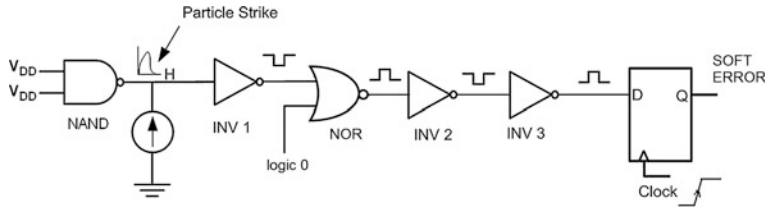

Fig. 1.2 The propagation of single event transient and generation of soft error

1.2 Circuit Level Modeling of a Radiation Particle Strike

The interaction of an ionized particle with a reverse biased junction of a device results in a current pulse which is traditionally represented using a double exponential waveform [3]. The expression for this current pulse is given by:

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta}\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right) \tag{1.1}$$

where,

Q is the charge (positive or negative) deposited by the particle strike, τ_α is the collection time constant of the p-n junction, τ_β is the ion-track establishment time constant. The time constants τ_α and τ_β are dependent on process technology. The values for τ_α is typically in the range 50–100 ps. On the other hand, τ_β values usually a few picoseconds [7].

In circuit simulations, an independent current source is connected between the drain and body terminals of a mosfet transistor as seen in Fig. 1.3.

Depending on logic state, either drain/well and drain/substrate junctions of off CMOS transistors would be vulnerable to a strike. Figure 1.4 below shows the equivalent circuit of the inverter given in Fig. 1.3. When input is at logic high, the PMOS transistor would be off and susceptible to a radiation strike at its drain terminal.

In circuit simulations, the effect of a PMOS transistor hit or a "p-hit" would be simulated by a current source taken in upwards direction. Similarly, for a logic low input, the NMOS transistor would be susceptible. Hence, the current source is drawn in downwards direction to simulate the effect of an NMOS transistor hit or an "n-hit".

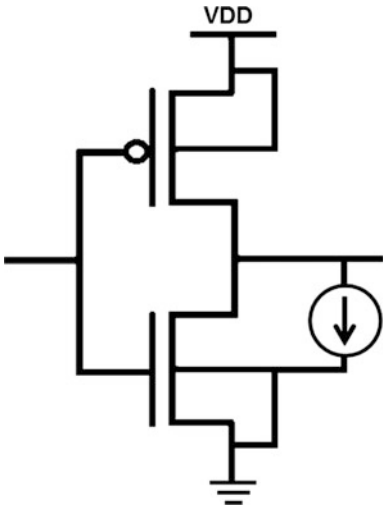

Fig. 1.3 Circuit level modeling using an independent current source

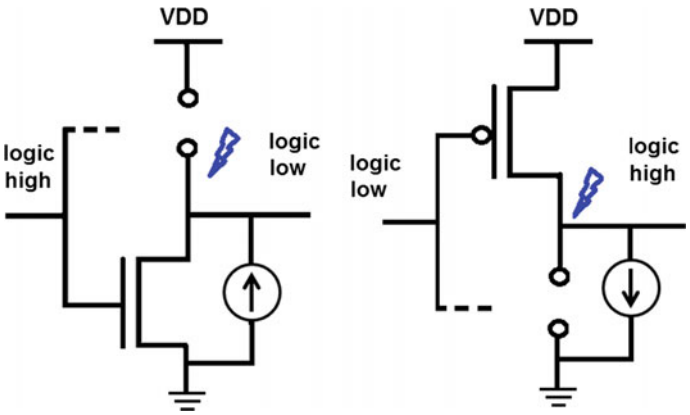

Fig. 1.4 The equivalent circuits for a p-hit (*left*) and a n-hit (*right*)

One way to represent the double exponential waveform (1.1) in Spice simulations is to use the simple exponential (EXP) function. The double exponential function in (1.1) can easily be represented using two saturated exponential functions:

$$e^{-t/\tau_\alpha} - e^{-t/\tau_\beta} = \left(1 - e^{-t/\tau_\beta}\right) - \left(1 - e^{-t/\tau_\alpha}\right) \tag{1.2}$$

Hence, circuitwise, this is equivalent to two current sources placed in parallel as shown in Fig. 1.5. In this figure, $I_{\max}$ shows the maximum value of current pulse is given by $I_{\max} = Q/(\tau_\alpha - \tau_\beta)$.

For ground level the max LET of such particles is approximately at 15 MeV cm^2/mg assuming high-energy atmospheric neutrons [8]. A particle with an LET of 1 MeV cm^2/mg deposits around 10 fC/μm along its track; hence an upper bound of 150 fC/μm charge density can be calculated. The collected charge, on the other hand, can be found by multiplying the charge density with the charge collection depth. For newer technologies, the charge collection depth is mostly 1 μm, hence the maximum deposited charge can be assumed as 150 fC at commercial level.

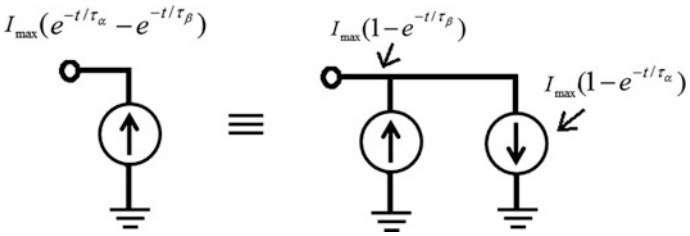

Fig. 1.5 Double exponential representation using two parallel current sources

The classical double exponential current pulse model given by (1.1) is often used in simulations to represent transient currents induced due to radiation. However, the affected area in a CMOS integrated circuit due to an ion strike has changed as device feature size has decreased with technology scaling [9]. Previously, the single event charge due to these strikes only affected the hit node which was mostly the drain-substrate junction of the hit transistor. For newer technologies such as 65 nm and beyond, however, a single event strike may affect multiple nodes (nearby devices) and nearby well contacts. As a result, a "plateau" in the single event current pulse following the prompt response will be observed especially with higher LET pulses [9–11].

Hence, for deep sub-micron technologies (DSM), the waveform of the corresponding SET produced by the current source does not reproduce that predicted using TCAD (Technology Computer-Aided Design) based device simulations and can lead to different SET amplitudes especially for higher LET (>10 MeV) particles [9].

It has been reported that, for higher LETs (>10 MeV), the current pulses have a plateau region in addition to the double exponential waveshape [9, 12]. Hence, the use of ideal double exponential current source alone is not sufficiently accurate, although double exponential current sources still provide a reasonable first-order estimate as a base function model [13].

A mixed-mode simulator may be used to correctly model to model Single Event effects. This simulator combines device level model with standard circuit-level SPICE models and creates a unified simulation environment. This allows selected components in a circuit to be modeled at the device level (i.e. off-biased n-channel transistor in the struck CMOS inverter) while the rest of the circuit is modeled at the circuit level. One advantage would be the direct calculation of voltage and current pulses induced in the struck device by a given particle strike. The limitation of mixed-mode simulator would be the size of the circuit that can be modeled which is usually limited to less than 25 circuit elements.

TCAD based methods also require large computation times although they can achieve a great level of accuracy. It is desirable to model particle strikes as current sources that can be easily injected on circuit nodes for performing quick SPICE simulations.

Researchers have also suggested the use of a combined approach where device simulations are first used to characterize current pulses for ion strikes and then these pulses are later used as inputs to Spice simulations to emulate ion strikes [14, 15].

For this purpose, the data obtained from device simulations are fitted to a double exponential pulse model (given in 1.3) with appropriate characteristic parameters. This model assumes that the SE current pulse exhibits an exponential behavior during its rise and decay. It was previously reported that the rising behavior closely resembles an exponential waveform [15] although there is a slight mismatch during the decaying phase. However, the mismatch during the falling phase usually can be ignored.

The double exponential model given in (1.3) is composed of an exponential function accounting for the rise in magnitude of the resulting single-event current and another exponential function modeling the decay in magnitude of this current.

$$I(t) = \begin{cases} I_{\max}\left(1 - e^{-t/\tau_1}\right) & \text{if} \quad t < t_d \\ I_{\max} e^{-(t-t_d)/\tau_2} & \text{if} \quad t \geq t_d \end{cases} \tag{1.3}$$

where,

τ_1 and τ_2 are the rise and the fall time constants of ion-induced current pulse, respectively. I_{max} is its magnitude, and t_d is the delay time for the falling exponential that controls the duration of the plateau effect. These values are computed using TCAD simulations of ion strikes in the drain junctions for different LETs.

1.3 Soft Error Rate

The chip soft-error rate (SER) is usually defined by the Failure-In-Time (FIT) or by Mean-Time-To-Failure (MTTF). One FIT is equivalent to 1 failure in 1 billion device hours of operation. MTTF, on the other hand, is inversely related to FIT. For example, a FIT rate of 1000 is equivalent to 114 years (10^9/(1000 × 24 × 365)).

It has been reported that advanced processors with large multimegabit-embedded SRAM can easily have soft failure rates in excess of 50,000 FIT at terrestrial level. The same error rate can also be achieved for standard high-density ASIC designs at 90 nm and below in [16].

For single-chip consumer applications, this error rate may not still be important for most designers, but for high-reliability systems composed of multi-chip assemblies such a rate becomes intolerable.

1.3.1 Error Rate Calculation Using Simulation Method

The calculation of logic SER is a difficult task as there are many factors that needs to be incorporated such as the energy and timing of the particle, the node area and input vector. Several SER estimation methods have been proposed. This section discusses the simulation method as it is a very accurate one.

In calculating the SER of logic, the simulation is performed for all possible inputs of the circuit, thus, considering them equally probable. The estimation should account for the fact that a particle strike is equally likely to create both positive and negative charge. The simulation method usually assumes uniform distribution of charge collection from $-Q_{max}$ to Q_{max}, where Q_{max} is the maximum charge collection possible for a given technology. It is also assumed that each node in the circuit is equally to be hit by a particle. On the other hand, the final

formulation should account for differing active node areas. Finally, transients are assumed to occur at equidistant times in a clock cycle.

The simulation method is based on the "inject and evaluate" approach. Faults are injected in the circuit in the form of a current source and simulated to check for errors. The flowchart shown in Fig. 1.6 explains the procedure. First, we select a circuit node and place the current source, and then an input pattern is chosen. Following this, a particular charge level is then applied at a particular timing instant. The output is checked for an error. We can have many different time instances by dividing the clock cycle. Once we are done with all time instances, a different charge level is adjusted. Once we are done with all charge levels, a new input pattern can be applied. After we complete all input patterns, then we can select a new circuit node, and repeat the process until we are done. At the end of the process, we count all errors and weight them noting differing node areas. After counting all faults or errors, we can obtain the probability of failure of the circuit (POFC) from which the SER can be calculated. Larger node areas have more change of getting hit compared to smaller ones and hence this need to be taken into account in the calculation.

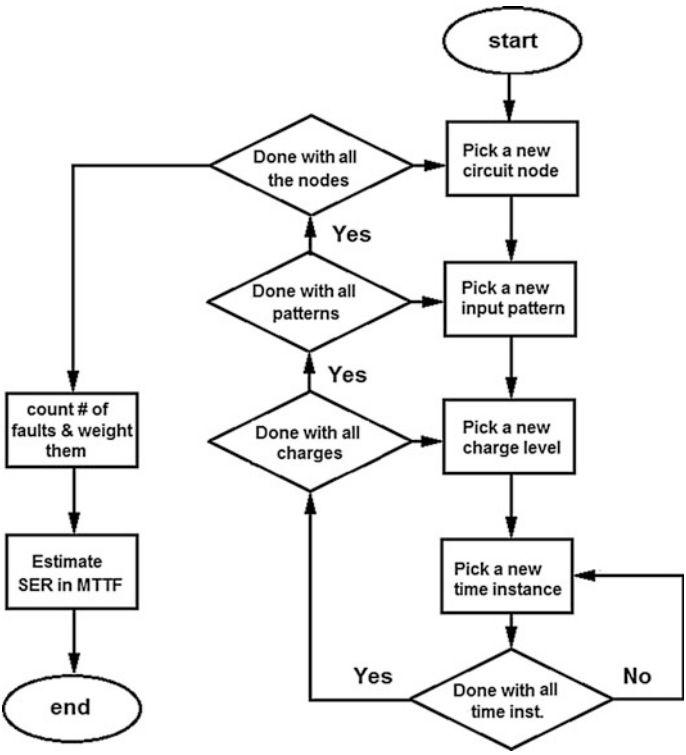

Fig. 1.6 SER calculation using simulation

POFC is a measure of the conditional probability of error given that a particle hits the circuit. The probability of failure for a circuit, POFC is given by:

$$POFC = \sum_{i=1}^{n} w_i \overline{\varepsilon_i}, \quad \text{with} \quad w_i = \frac{A_i}{\sum_{i=1}^{n} A_i} \tag{1.4}$$

Here, A_i is the area of the node i, n is number of nodes and $\overline{\varepsilon_i}$ is given as:

$$\overline{\varepsilon_i} = \frac{1}{k} \sum_{i=1}^{k} \varepsilon_i \tag{1.5}$$

where,

$$\varepsilon_i = \begin{cases} 1, & \text{if the injection into node } i \text{ results in a fault} \\ 0, & \text{no fault} \end{cases}$$

k = (# of input combinations) * (# of charge injection levels) * ((# of input patterns).

Assuming, the particle density at sea level (New York) is approximately 100,000/cm^2/yr, MTTF can be calculated probability from *POFC*:

$$MTTF = \frac{1}{POFC \times Area\ of\ circuit \times 100{,}000} \tag{1.6}$$

The number of simulations to be performed can be quite large since $k * n$ simulations will be needed to get an accurate SER estimation. With the large number of input patterns and nodes to be simulated, the simulation time can be quite time consuming. Hence, in order to reduce runtime, simulations are performed for only randomly selected input combinations from which a reasonably accurate SER estimate can still be obtained [17].

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Chapter 2
Mitigation of Single Event Effects

2.1 Hardening Techniques

The radiation hardening techniques can be applied at various levels; therefore it can be classified as system level, device level and circuit level mitigation. System-level techniques deal with soft errors at the system architecture level. Device-level hardening requires fundamental changes to the underlying fabrication technology used to manufacture ICs. Finally, circuit-level techniques rely on changes in the circuit design to reduce soft error sensitivity. This focus of this chapter will be on circuit level soft error mitigation methodologies after a brief discussion on system and device level techniques.

2.2 System Level Techniques

System level hardening techniques generally add redundancy in design to achieve error detection/tolerance ability [1]. For logic circuits, the triple-modular redundancy (TMR) can be implemented at the system board level. In TMR technique, the hardware is replicated three times and a majority voting logic is used to ignore any corrupt value. Although, this comes with a large hardware overhead burden, but this option is sometimes preferred by the system engineer.

The system level hardening technique for memory circuits involves in adding a parity bit to the memory word [2]. When a word is written to the memory, the parity generator produces a parity value and appends to the data. In its simplest form, error detection consists of adding a single bit to store the parity of each data word. Upon retrieval of data, a check compares the parity of the stored data with that of its parity bit.

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If a single error has occurred, the data parity won't match the bit parity. An additional circuit is needed to correct the error. The check also won't reveal a double error because the parity will match. Designers typically achieve error correction by adding extra bits to each data vector and encoding the data so that the information distance between any two possible data vectors is at least three. There are many methods available to correct the errors, like the hamming codes. However, the use of these methods may result in severe area and power penalties.

2.3 Device Level Techniques

Device level hardening techniques aim to reduce and mitigate charge collection at the site of particle strike. This is achieved by implementing a change in the fabrication process. Some device level hardening techniques includes adding a doping layer to confine the charge collection efficiency of the substrate. Silicon on Insulator (SOI) process is also assumed to provide circuits that are immune to radiation hits [3].

In a conventional bulk technology, charge deposition occurs within the first few micrometers of the body. In a standard bulk CMOS process technology, the p-type body of an NMOS transistor is held at the ground voltage.

In an SOI device, the collection volume is reduced by the fact that the active device is fabricated in a thin silicon layer that is dielectrically isolated from the substrate. The source, body, and drain regions of transistors are insulated from the substrate by an insulating layer of silicon dioxide (SiO_2) (Fig. 2.1). The body of each transistor is typically left unconnected and that results in floating body. In a SOI transistor, the charge deposition path is limited compared to a bulk device.

The SOI process technology can reduce the capacitance at the source and drain junctions greatly by eliminating the depletion regions extending into the substrate. Less collection volume usually means less sensitivity to SE particle hits.

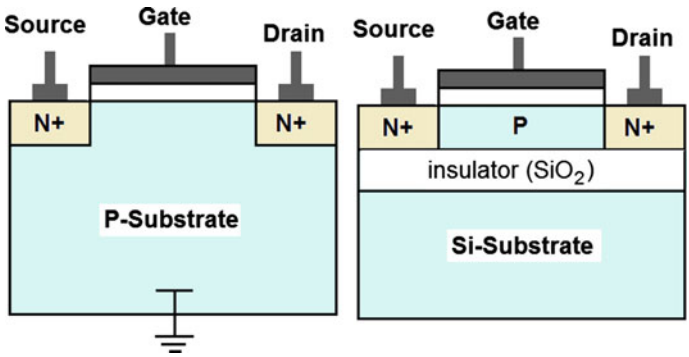

Fig. 2.1 Bulk transistor versus SOI transistor

A higher speed is also obtained in an SOI transistor compared to its bulk counterpart due to reduced parasitic capacitances. The decrease in junction capacitance also reduces overall power consumption.

2.4 Circuit Level Hardening Techniques

Circuit level hardening techniques introduce a change in a circuit design to mitigate single event effects. In general, circuit level mitigation techniques for single event effects must either filter or dissipate the collected charge or provide some form of redundancy to prevent a single event upset from corrupting data.

The most common way to reduce the soft error rate of a circuit is to increase the node capacitance by adding a capacitor at that particular node [4, 5]. As mentioned in Chap. 1, the critical charge of a particular node, in its simplest term, can be defined as $Q_{crit} = C_{node} * V_{DD}/2$, where C_{node} is the node capacitance (Here, it is assumed that SET noise amplitude of $V_{DD}/2$ crosses the noise margin of the subsequent gate). Therefore, increasing the node capacitance raises the critical charge of that particular node and can make that node more robust to radiation. The capacitance method, however, imposes large area and power penalty due to added capacitor.

Spatial redundancy techniques such as triple modular redundancy (TMR) circuits triplicate the logic to be protected and use a voting circuit to filter out the transient (Fig. 2.2) [5, 6]. Under normal conditions, all copies of the CL circuit produce the same value. However a particle strike on one of the logic copies can cause a different output value to be produced. The voting circuitry generates a valid result only if at least two calculations agree; hence the false output in one of the outputs will be eliminated. It has been assumed here that the probability of the particle strike on two circuits at the same time is very low and hence is neglected.

The TMR method uses the same circuitry irrespective of the magnitude of transient that is to be mitigated and can be cumbersome. This method causes large area overhead (>200 %) due triplication.

Logic duplication along with a buffer gate is also proposed to mitigate SETs [7]. In this case, the CL is duplicated and sent to the buffer element to filter out the unwanted transient (Fig. 2.3). The buffer gate output only changes when both inputs

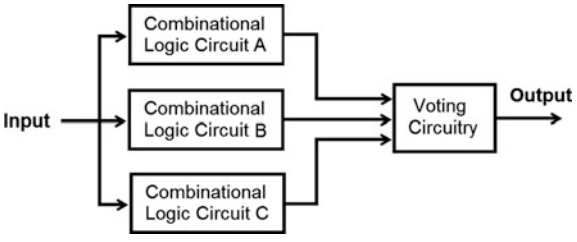

Fig. 2.2 Spatial TMR technique

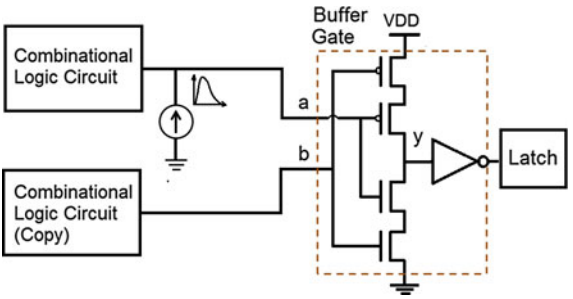

Fig. 2.3 Logic duplication with buffer element to eliminate SETs

agree; hence a wrong value produced on one of the CL outputs is eliminated. This circuit is implemented at the input of each latch input to filter out the transients before they get captured.

The operation of the buffer gate is as follows: The buffer gate, also named as C-element (or Muller C-element), consists of two PMOS and two NMOS transistors in series as pull-up and pull-down networks, respectively. The buffer gate only responds when both inputs are same. As an example, when both inputs are at logic 0, both PMOS transistors are "ON" and pull output y value to logic 1. The inverter then generates a logic 0 which is then input to the latch element. Similarly, for logic 1 on both inputs, the two NMOS transistors turn on, and the output of the buffer gate would become a logic 1. In both cases, correct data arrives at the latch input. In the case of an unwanted SET pulse, inputs would differ and one of the PMOS or NMOS transistors in either pull-up or pull-down network would be OFF. This would cause output of the buffer gate to float or stay in high impedance state. In other words, output of the buffer gate would not change and hence the latch would keep its previous data. In logic duplication method, the area overhead would be less than the TMR technique, however, still remains large due to duplication.

While spatial redundancy techniques separate data signals in space, temporal redundancy techniques separates data signals in time in order to filter out SETs. Temporal methods sample the data with different delays and use a voting circuit to eliminate the SET [8, 9].

Before going into further detail let's discuss on the simple latch design shown in Fig. 2.4. We can create a simple latch using than a 2-input MUX (multiplexer) with its output fed back to one of its inputs and the select line controlled by the clock signal. When clock signal is low, the previous data is retained. When clock activates, the data on the second input determines the latch output. However, this simple design is susceptible to soft errors as any SET noise arriving at the data input may cause wrong data to be stored.

We can create a soft error resistant (hardened) version of Fig. 2.4 using temporal redundancy technqiue. The configuration shown in Fig. 2.5 consists of three separate data paths having different delays, a voting circuit, and a 2-input multiplexer connected in a feedback loop. Here, the second and the third data paths incorporate time delays of ΔT and $2\Delta T$, respectively, where ΔT is selected equal to the duration of maximum SET width that is to be eliminated.

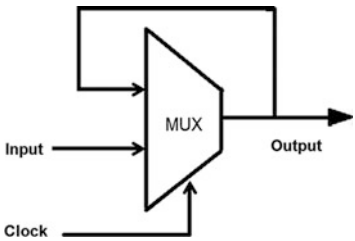

Fig. 2.4 A simple latch using 2 × 1 multiplexer

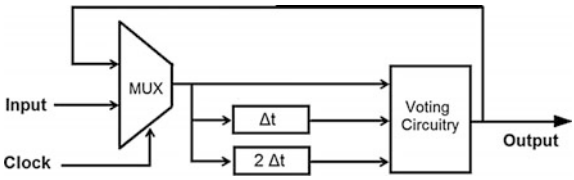

Fig. 2.5 Triple-path temporal redundancy in a hardened latch

When an SET arrives at the first input of voting circuitry, the outputs of second and third paths are still unchanged. Since the majority of the sampling is fed back to the MUX, the transient will be eliminated. After ΔT seconds, the SET becomes available at the second input of the majority voter. However, since the first and the third inputs are stable, the voter circuitry again eliminates the transient. By using the single MUX at three separate times, we effectively obtain the equivalent of triple spatial redundancy without the large area penalty.

This technique, however, has the disadvantage of waiting 2ΔT time to complete the calculation which reduces the operating frequency. It was calculated that for a ΔT of 100 ps, the upper limit on operating frequency is 2.5 GHz [6]. However, often the SET width can be larger than 100 ps which limits the usefulness of this technique. Hence, temporal redundancy technique limits the circuit operating speed due to inherent delay needed for calculation.

A technique combining both temporal and spatial schemes has also been proposed in [10]. In this method, the circuit consists of two paths of differing delays between the combinational circuit output and the latch input as shown in Fig. 2.6. The first path does not delay the signal at all, while the second path delays the signal by t_{critical}.

The buffer circuit functions only when both the inputs are identical. Hence, if the SET pulsewidth is less than t_{critical}, it gets filtered otherwise propagates through the buffer gate.

Another popular technique used in SET mitigation is the driver sizing technique. Sizing of a gate's transistors increases device capacitance and drive current to decrease device vulnerability to soft errors [11]. First, the increased output capacitance increases the critical charge Q_{crit} value of the hit node thereby stabilizing the node against SET effects. Second, larger drive strengths (increased drive

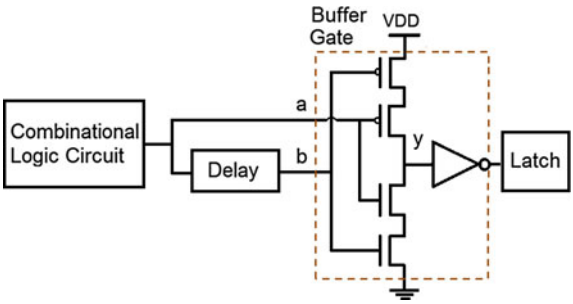

Fig. 2.6 Double path temporal redundancy with a buffer gate

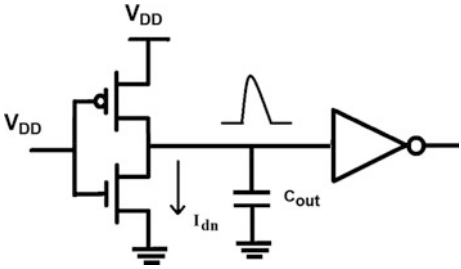

Fig. 2.7 Driver sizing technique applied to the hit gate transistors

current) of NMOS and PMOS transistors can quickly dissipate the collected charge and reduce the vulnerability to ionizing particles.

Consider the logic inverter shown in Fig. 2.7. A logic high value is applied at the input which turns off the PMOS transistor making it susceptible to radiation strikes due to its reverse-biased p-n junction. Any charge deposited on the output capacitance C_{out} must be discharged through the ON NMOS transistor. By increasing the width-to-length ratios of the inverter transistors, the maximum drain current I_{dn} can be increased so that a net change in capacitor voltage due to an ion strike is dissipated before it is propagated by the next logic stage.

The disadvantages of driver sizing technique are the power and area penalties associated with increasing the size and quiescent currents of many of the circuit components.

The Cascode Voltage Switch Logic (CVSL) gates have also been proposed for increasing soft error tolerance [12]. The CVSL consists of two storage nodes; the function and its complement. The output nodes are connected in a feedback loop by the PMOS transistors resulting in higher tolerance to SET pulses compared to CMOS. The NMOS transistors, on the other hand, are connected to the inputs. Figure 2.8 shows a CVSL NOR gate design.

CVSL gates may result in increased circuit delays unless there is high number of inputs. This is due to the fact that a CVSL gate in a way acts as a 2-stage gate due to feedback connection [12]. Hatano has examined the performance of a 4-stage CVSL XOR chain and compared it to CMOS implementation. He found out that the

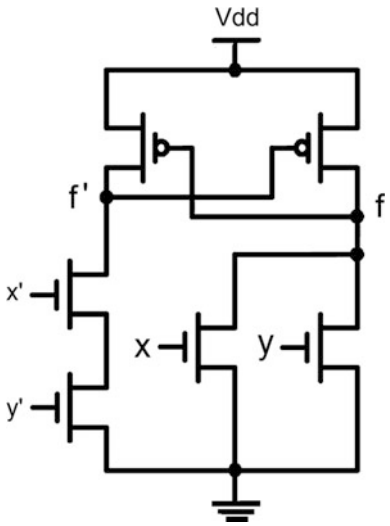

Fig. 2.8 CVSL NOR gate structure

CVSL gate can act 2.5 times slower than its CMOS counterpart [13]. The CVSL gate also requires complement of input variable which increase circuit area.

2.5 Summary

This chapter covered various circuit level SET mitigation techniques. Spatial redundancy techniques such as TMR and logic duplication result in large area overheads and this mostly prohibits their use. Temporal methods suffer from performance overheads due to need to wait for the computation. In addition, temporal methods require delay elements which may be area costly in order to provide time filtering. Researchers suggested either the use of a large capacitor or an inverter string to use as the delay element [14]. The number of inverters required in the inverter string can sometimes be large even for a moderate SET duration that is to be eliminated.

Among all circuit level techniques considered, driver sizing provides the optimal solution in mitigating the SE Transients. The delay overhead is small and manageable while the area overhead is "small to moderate" depending on the charge level that needs to be mitigated.

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Chapter 3
Transmission Gate (TG) Based Soft Error Mitigation Methods

3.1 Basic TG Filtering Technique and Tunable Transient Filter

In order to harden a CL against soft erros using a small area overhead, researchers have also proposed SET filtering techniques based on a transmission gate (TG) design or pass transistors. The previous work in [1] has utilized the low-pass filtering characteristics of TGs at CL outputs to mitigate SETs before they reach to latch elements. In this basic TG technique, the pass transistors forming the TG are made always conducting by tying the gates of PMOS and NMOS transistors to V_{SS} (ground) and V_{DD} (power supply), respectively.

While data signals can pass through the circuit with little change, the magnitude of transient pulses are reduced by the circuits. This technique becomes most efficient under the constraint that a two-stage TG configuration is utilized where the size of the second stage taken four times bigger than the first stage as shown in Fig. 3.1. In this case, the magnitude of transient pulses is reduced by 60 % which has been claimed to be sufficient. Unfortunately, the method cannot eliminate SET pulses, when the SET pulses with large magnitude occur.

Later, the tunable transient filter (TTF) design which achieved better filtering ability has been proposed [2]. A TTF design consists of two inverters and a number of TGs (or filter gates) added in between these inverters as shown in Fig. 3.2. The number of TGs or N, is determined based on the SET duration to be suppressed. It was claimed that this technique mitigated SETs better compared to the basic TG technique due to the fact that the input signal drives the input of filter gates. The hardware overhead of TTF technique, however, depends on the size of the glitch being suppressed as the number of pass gates required increase linearly with the glitch-width [2].

S. Sayil, *Soft Error Mechanisms, Modeling and Mitigation*,
DOI 10.1007/978-3-319-30607-0_3

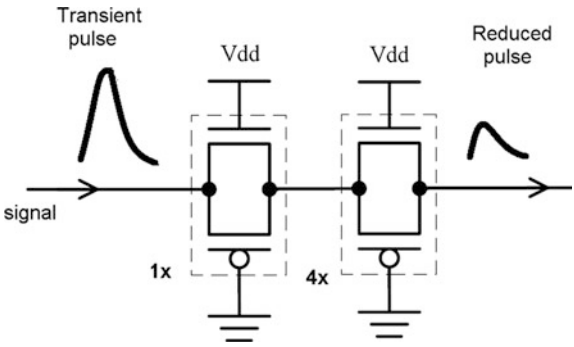

Fig. 3.1 TGs acting as low pass filters

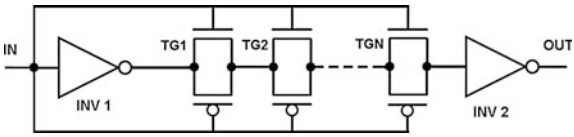

Fig. 3.2 TGs acting as low pass filters

3.2 TG with Varied Gate Bias for Soft Error Mitigation

In order to turn a TG, an NMOS gate voltage (V_{GN}) of V_{DD} and a PMOS gate voltage (V_{GP}) of 0 V are normally used. However, a TG can be still turned on with a V_{GN} less than V_{DD} and a V_{GP} greater than 0 V as long as the gate to source-voltage (source-gate) voltage is greater than V_{TN} ($|V_{TP}|$), where V_{TN} and V_{TP} are NMOS and PMOS transistor threshold voltages, respectively. The new scheme with varied gate voltage offers improved filtering characteristics when compared to basic TG and TTF configurations.

This new methodology is based on applying different gate biases on the TG pass transistors depending on the SET duration that needs to be mitigated [3]. In comparing this technique with the basic TG method [1], the setup shown in Fig. 3.3 has been utilized. In this setup, the propagated SETs were modeled using trapezoidal waveforms having rise and fall times of 15 ps at the input of the TG. This approximation was done merely for simulation convenience as various TG based techniques are compared. In simulations, the width of the trapezoidal waveform Δ_{SET} was measured about 0.5 V_{DD}. This circuit was designed in 45 nm process technology using Predictive Technology Model (PTM) [4] and simulated using Spice.

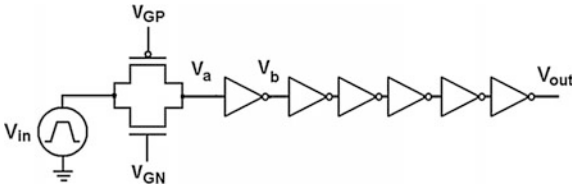

Fig. 3.3 Simulation set-up using an inverter string

In Fig. 3.3, V_a and V_b denote the output voltages of the TG stage and first inverter, respectively. An SET pulse duration of 100 ps has been selected and applied using the V_{in} voltage source.

For the basic TG method, the V_{GN} = 1.2 V (V_{DD}), and V_{GP} = 0 V combination has been applied. As for the new method, the gate voltages of NMOS and PMOS transistors are symmetrically varied from their respective values using $V_{GN} = V_{DD} - \Delta V$ and $V_{GP} = \Delta V$, where $\Delta V > 0$. In simulations, ΔV value has been increased in steps of 0.1 V until SET mitigation has taken place. In these simulations, the threshold voltages for the NMOS and PMOS transistors were at 0.62 V/−0.58 V, respectively.

Figure 3.4 compares the output voltages of basic TG gate scheme and the proposed method for ΔV = 0.5 V. Referring to Fig. 3.4a, it is clear that the basic TG method cannot mitigate the transient. On the other hand, the gate bias with V_{GN} = 0.7 V and V_{GP} = 0.5 V mitigates the 100 ps SET pulse as shown in Fig. 3.4b as the voltage V_b remain almost unchanged near V_{DD}.

The strong filtering effect can be attributed to increased resistance of the TG due to reduced gate-source (source-gate) voltages of NMOS (PMOS) pass transistors.

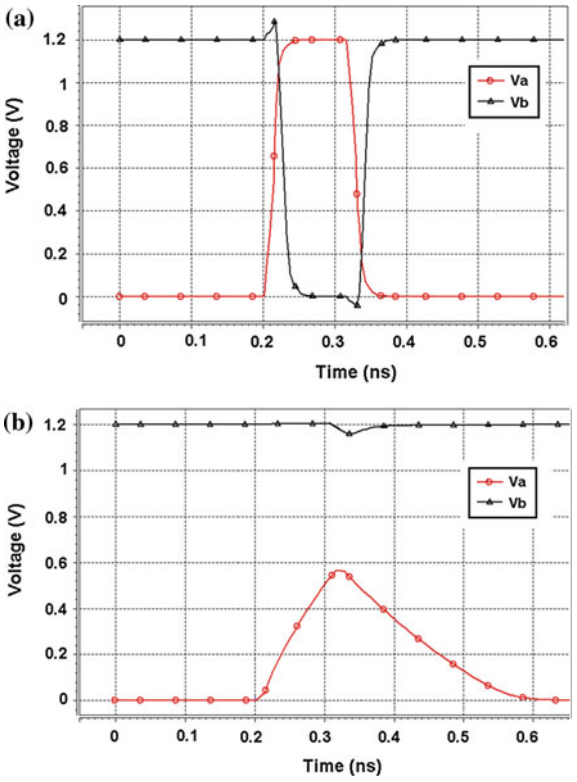

Fig. 3.4 TG output waveforms for **a** V_{GN} = 1.2 V and V_{GP} = 0 V and **b** V_{GN} = 0.7 V and V_{GP} = 0.5 V

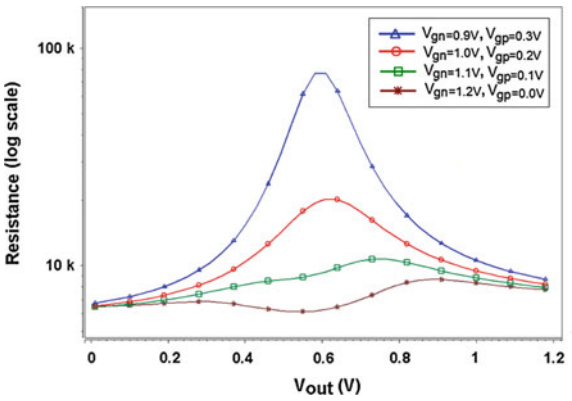

Fig. 3.5 The TG resistance versus output voltage

Figure 3.5 shows the TG resistance as a function of output voltage when gate voltages (V_{GN}, V_{GP}) are varied up to 0.3 V in steps of 0.1 V. By adjusting the individual pass transistor's gate voltages, it should be possible to eliminate various SET pulse durations.

The gate voltages of the TG can be provided off-chip using I/O pads. If this is not possible, the gate voltages need to be generated internally using some extra hardware. In generating the TG gate voltages, a simple voltage divider circuit consisting of serially connected transistors can be used [5].

Figure 3.6 shows a configuration where a supply voltage-divider with diode-connected NMOS transistors operating in saturation region is used to obtain the gate-bias voltages for the TG. In this case, the sizes of M1 and M2 transistors

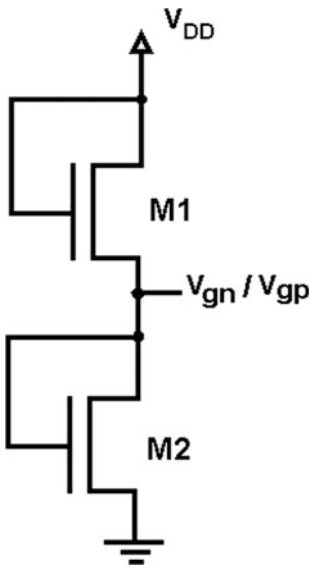

Fig. 3.6 The NMOS voltage divider circuit

Table 3.1 Gate voltages needed to mitigate various SET durations

Δ_{SET} (ps)	Gate voltages V_{GN}/V_{GP} (V) needed	Signal duration (ps) positive/negative pulse
50	0.89/0.36	56/58
75	0.76/0.47	92/95
100	0.71/0.52	128/134
125	0.67/0.55	161/169
150	0.65/0.57	200/208
175	0.64/0.58	232/237
200	0.63/0.59	265/268

need be adjusted to give desired values of gate voltages. The area overhead for the bias circuit is expected to be small.

Table 3.1 shows the gate voltage combinations needed to mitigate certain SET durations up to 200 ps using HSpice simulations. In finding these gate voltages, both positive and negative SET waveforms have been considered.

For a TG filter designed, we can determine the maximum width of propagated SETs that can be mitigated, and the minimum width for signals that can be preserved. The difference in these two values can be defined as the TG filter margin [2].

Referring to Table 3.1, the filter margin varies between 12 % up to 33 % of the maximum mitigated SET duration Δ_{SET}, indicating the clean cutoff properties of the proposed TG filter.

A comparison has also been made between the new TG method (with varied gate voltage) and the basic TG and TTF design techniques in terms of area. For the basic TG technique, a single stage cannot eliminate the SET pulse. Hence, a two-stage configuration has been considered during simulations. In finding the minimum possible area, various sizes were examined for the basic TG method. These were: 1X−1X, 1X−4X, 1X−8X, and 4X−4X, where 1X indicates a minimum size TG (or inverter) in 45 nm technology. For the TTF design, the number of filter gates (or TGs) is increased until SET has been mitigated.

The histogram in Fig. 3.7 shows the result of this comparison. When eliminating a 200 ps SET pulse, the new method requires only 1X circuit area, while basic TG

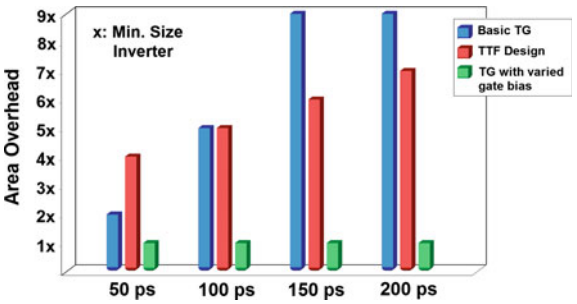

Fig. 3.7 Area overheads for basic TG, TTF and the new technique for various SET widths

and TTF techniques require 9X and 7X area overheads, respectively. It was also observed that the hardware overhead for basic TG and TTF techniques was dependent on the glitch that needs to be suppressed. The number of TGs required increase mostly in proportion to the glitch-width. However, the hardware overhead remains at 1X for the proposed TG method for the SET durations considered.

Previous work has shown that SET pulse-widths can be as large as 1 ns in 90 nm bulk technologies [6]. However, for newer technologies such as 65 nm, SET pulse-widths reported are only up to 200 ps [7] except for the case that there is an elevated temperature [8]. It was reported also that for 45 nm SOI technology, the SET pulse-widths that occur in CL are mostly below or close to 200 ps [9]. Hence, we should be able to eliminate most SET pulses by just using a single TG stage by controlling the gate voltages in newer technologies.

3.3 Effect of Body-Biasing on TG Mitigation Ability

For mitigating larger SET durations (>200 ps), a two-stage TG configuration can be hired. In this configuration, gate voltages on the first stage is kept constant at the largest ΔV variation, while for the second stage these voltages are adjusted to eliminate larger durations. The simulation results show that up to 580 ps SET duration can be filtered using a 2-stage configuration.

Alternatively, the same mitigation capability can also be obtained using only one TG stage if the body bias of individual pass transistors can be adjusted.

The Variable Threshold (VTCMOS) scheme [10] is one of the popular leakage power reduction techniques. In VTCMOS, a zero body-bias is applied to the transistors during the active mode. However, during standby periods, the body bias is connected to a voltage greater than V_{DD} for a PMOS and to a voltage lower than V_{SS} for the NMOS transistor to cut-off the leakage current as in Fig. 3.8.

The reverse body-bias applied during standby increases the transistor threshold [11] and in turn increases transistor on-resistance. Using this property, the mitigation property of proposed TG method can be further enhanced by controlling the body bias effect

Table 3.2 shows the effect of body biasing on SET pulse mitigation ability. Here, V_{BN} and V_{BP} indicate the body-bias voltages of NMOS and PMOS transistors, respectively. Although, body biasing has little effect improving SET mitigation ability for the basic TG configuration (first row), it increases the SET mitigation capability considerably for the proposed technique. For example, using body bias voltage combination of V_{BN} = 1.7 V and V_{BP} = −0.5 V (instead of the conventional V_{BN} = 1.2 V and V_{BP} = 0 V), increases filtered SET duration from 150 to 454 ps.

The body-bias technique can easily be implemented in SOI technology. However, for bulk CMOS, a triple-well CMOS technology is required [11].

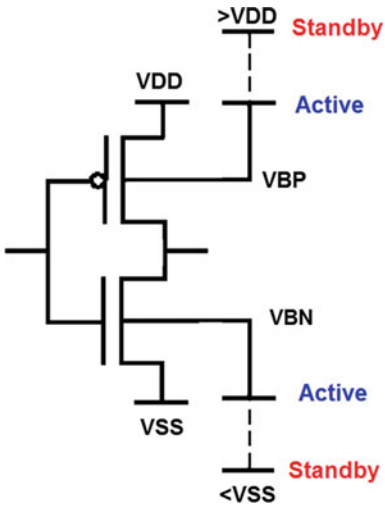

Fig. 3.8 VTCMOS technique applied to an inverter

Table 3.2 Effect of body biasing on TG mitigation

Gate bias V_{GN}/V_{GP} (V)	Maximum Δ_{SET} (ps)	
	V_{BN} = 1.2 V V_{BP} = 0 V	V_{BN} = 1.7 V V_{BP} = −0.5 V
1.2/0	38	39
0.89/0.36	50	66
0.76/0.47	75	135
0.71/0.52	100	220
0.67/0.55	125	330
0.65/0.57	150	454
0.64/0.58	175	510
0.63/0.59	200	598

3.4 Temporal Sampling Application

The new TG methodology can also be adopted in a temporal sampling scheme. Referring to buffer-gate method discussed in Chap. 2 (Fig. 2.6), authors suggest the use of either an inverter string or two inverters with a capacitance in between to generate the signal delay of $t_{critical}$. The use of a capacitance results in large area and power overheads. If a string of inverters is used, the number of inverters required can also be large making it area inefficient. Simulations show that 16-minimum sized inverters are needed to mitigate a 200 ps SET pulse in 45 nm technology.

However, the delay element can efficiently be implemented using a single TG with varying gate and body bias (see Fig. 3.9). The delay of the TG can be controlled by varying the gate and body bias. It only takes 1X area to produce a delay up to 600 ps using the proposed TG method.

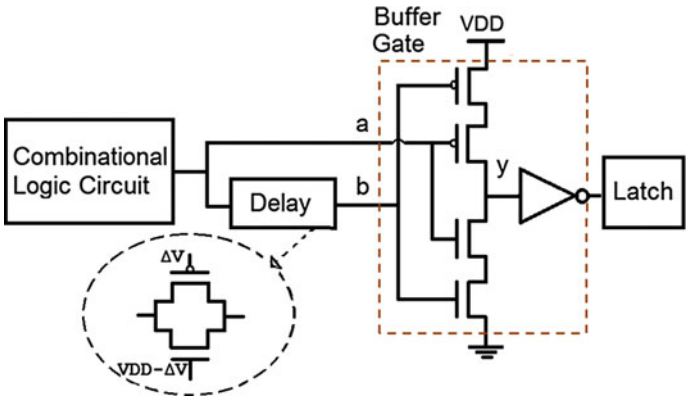

Fig. 3.9 TG with varying gate and body bias serving as a delay element

3.5 TG Mitigation Method Combined with Driver Sizing

The delay penalty of proposed method is proportional to SET pulse duration that needs to be eliminated. For faster designs, the delay penalty may become unacceptable. In this case, the TG technique can be combined with driver sizing method in mitigating the SETs. In this case, the task of SET suppression is shared between the TG and the driver sizing and the delay penalty is kept low.

In the combine method, driver sizing is used partially to suppress propagated SET at the strike site while the TG suppresses the remaining glitch. In order to keep delay penalty manageable, the TG delay can be controlled using different gate biases for the pass transistors. This would be determined depending on the available time-slack. For example, if time-slack for a circuit is 83 ps, then the V_{GN}/V_{GP} combination of 0.76/0.47 (see Table 3.1) can be used since the TG delay overhead at this combination is approximately 75 ps. While TG can only mitigate up to 75 ps SET duration compared to its maximum 200 ps capability, its delay overhead will be less. The combine approach still results in area savings compared to driver-sizing applied alone in mitigating SETs. The TG can be placed anywhere along the path in mitigating the glitch remaining after sizing. For some certain critical paths, driver-sizing technique may need to be applied alone if there is not enough time-slack.

For simulations, first consider the full-adder circuit given in Fig. 3.10. Here, the critical and non-critical paths consist of gates 2–4–6–7–9–10 and gates 13–14, respectively. Before any TG insertion, the critical and non-critical path delays are calculated as 92 and 38 ps, respectively. Assuming the delay specification is 150 ps, the available slacks are 58 and 112 ps for critical and non-critical paths, respectively.

In simulations, all gates were taken as minimum size with power supply voltage chosen as 1.2 V. The hit locations were selected at nodes close to primary inputs

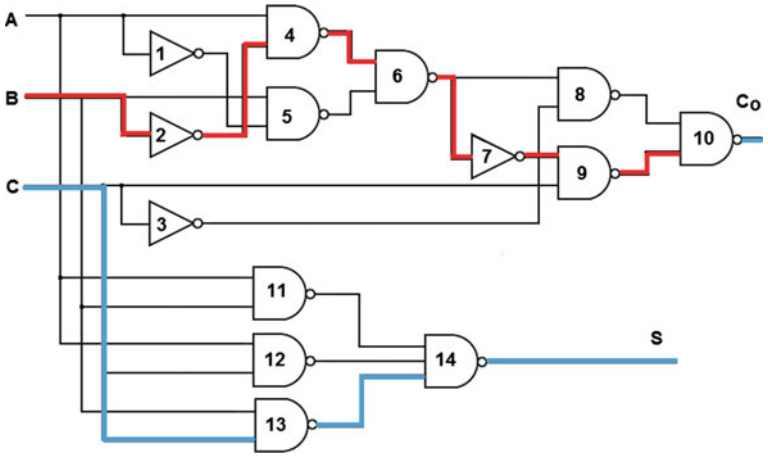

Fig. 3.10 Full-adder circuit

(e.g. output of gate 2) and an erroneous signal due to an SET was propagated to the output for observation. Three charge levels at 25, 50, and 100 fC were applied. An SE hit was simulated at the output of selected gates using a double exponential current pulse given earlier (see Eq. 1.1).

The time constants τ_α and τ_β in the double exponential equation, were selected as 100 and 5 ps, respectively based on [12]. In simulation, the double-pole representation has been used as an approximation to waveforms seen in mixed-mode simulations.

The combine method has been compared to the driver sizing technique in [12] using the full-adder circuit. The basic TG (with V_{GN} = 1.2 V andV_{GP} = 0 V) along with driver sizing is also included in the comparison. Table 3.3 shows the area and delay overheads for all these techniques. For driver sizing, gate transistors are sized up until soft error at the output is completely eliminated. As for the combine method, gate voltage combination was first determined based on the available time-slack and then sizing was done on hit gate's transistors..

Referring to Table 3.1, the gate voltage V_{GN}/V_{GP} combination of 0.89/0.36 may be used in the TG for the critical path, since the allowed time-slack is 58 ps. However, we can fine tune the V_{GN}/V_{GP} combination further considering the fact that driver sizing actually causes a speed-up effect. Hence, instead, a stronger TG filter with 0.83/0.41 gate voltage combination can be used for the critical-path. This value was determined using a simulation. This was done for obtaining a better area efficiency.

For the non-critical path, the available slack is 112 ps; hence this allows the use of 0.71/0.52 for V_{GN}/V_{GP}. Again, exploiting the driver sizing speedup effect, the gate voltage V_{GN}/V_{GP} combination of 0.67/0.55 could be used in the combine method instead for the non-critical path in order to get better area efficiency of the method.

Table 3.3 Area and delay overheads for driver sizing, basic TG and the combine method

Deposited charge	Critical path					
	Driver sizing only		Combine method (proposed TG + sizing)		Basic TG + sizing	
	Area overhead	Delay overhead (ps)	Area overhead	Delay overhead (ps)	Area overhead	Delay overhead (ps)
25 fC	7X	−9	**6X**	**55**	7X	12
50 fC	13X	−8	**10X**	**56**	13X	10
100 fC	25X	−9	**20X**	**56**	24X	10
Deposited charge	Non-critical path					
	Driver sizing only		Combine method (proposed TG + sizing)		Basic TG + sizing	
	Area overhead	Delay overhead (ps)	Area overhead	Delay overhead (ps)	Area overhead	Delay overhead (ps)
25 fC	14X	−14 ps	**10X**	**103**	14X	9
50 fC	22X	−14 ps	**15X**	**104**	20X	9
100 fC	34X	−14 ps	**23X**	**104**	31X	9

Referring to Table 3.3, the area savings is around 20 % for critical path (excluding 25 fC), and about 32 % for non-critical path when combine approach is used. For non-critical path, more available slack translates into more mitigation ability for the TG and better area efficiency was obtained. The delay penalty of the combine method was around 56, and 100 ps for critical and non-critical paths, respectively. The simulation results also showed that the use of basic TG technique along with driver sizing did not offer important area savings. Hence, results show the advantage of the combine method over the basic TG method.

In comparing the combine method to driver sizing and basic TG techniques further, different benchmark circuits such as 4-bit-carry-look-ahead-adder circuit [13], 74L85 4-Bit Magnitude Comparator, and 74181 4-Bit ALU have been used. The delay specification for each circuit is assumed to be at 35 % more than the critical path delay.

Table 3.4 shows the results obtained for all circuits examined. At each charge level, first and second numbers show the area overheads for driver sizing and the basic TG & driver sizing method, respectively. The third entry (shown in bold) indicates the area overhead for the combine method. The simulations were done for both critical and non-critical paths.

Compared to the conventional driver sizing technique, the combine approach on the average saves 26 % circuit area for critical paths, and about 40 % for non-critical paths. Better area savings obtained should be due to increased stages and SET attenuation in benchmark circuit. The delay overhead is around 70 and 125 ps for critical and non-critical paths.

Table 3.4 Area overheads for driver sizing, basic TG with sizing and combine method for test circuits (area overheads are shown in the same order)

Deposited charge	4-bit CLA adder		74L85 Comparator		74181 4-Bit ALU	
	Critical path driver sizing	Non-critical path	Critical path driver sizing	Non-critical path	Critical path driver sizing	Non-critical path
25 fC	10X	12X	9X	14X	8X	12X
	10X	12X	9X	13X	8X	12X
	8X	**8X**	**7X**	**7X**	**6X**	**7X**
50 fC	20X	24X	27X	37X	32X	34X
	19X	23X	25X	33X	29X	31X
	14X	**14X**	**20X**	**24X**	**25X**	**21X**
100 fC	61X	72X	63X	70X	54X	69X
	57X	66X	59X	64X	50X	65X
	44X	**45X**	**42X**	**40X**	**40X**	**39X**

In summary, the new TG based technique with varied gate voltage offers improved SET filtering characteristics compared to basic TG and Tunable Transient Filter designs.

The delay penalty of proposed method is proportional to SET pulse-width that needs to be eliminated. For faster designs, the technique can be combined with the driver sizing method in mitigating the SETs to keep delay penalty manageable. In this combine method, the driver sizing is used partially mitigate the propagated SET at the strike site while the TG suppresses the remaining transient glitch.

In comparison to driver sizing taken alone, this combine approach saves considerable circuit area. In combination with driver sizing, the proposed TG method has potential to reduce soft error rate in combinational circuit using smaller area overhead.

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Chapter 4
Single Event Soft Error Mechanisms

4.1 Introduction

It has been reported that advanced processors with large multimegabit-embedded SRAM can easily have soft failure rates in excess of 50,000 FIT at terrestrial level [1]. The same error rate can also be achieved for standard high-density ASIC designs at 90 nm and below in [2].

For single-chip consumer applications, this error rate may not still be important for most designers, but for high-reliability systems composed of multi-chip assemblies such a rate becomes intolerable [1]. Hence, for mission-critical or high-reliability applications such as military, avionics [3], medical systems [4], etc., other sources for such errors also need to be included in reliability analysis in addition to SETs. These additional error sources include SE soft delays [5], radiation induced clock jitters and clock pulses [6], SE crosstalk noise pulses [7–9], and finally the SE crosstalk delay [10] that has been reported relatively recently.

All these errors occur under specific conditions: Soft delay effect occurs when high-energy particle hits the drain node of a CMOS gate's transistor while signal at the output is transitioning. SE clock jitter occurs when particles inject charge onto clock circuit nodes during clock edge present. An energetic particle strike on clock circuit nodes can also create a "false clock pulse" which can be interpreted as a legitimate clock pulse. At last, the SE crosstalk noise and crosstalk delay effects occur via interconnect cross-coupling. The interconnect coupling effects can cause SETs to contaminate electronically unrelated circuit paths which can in turn increase the "SE susceptibility" of CMOS circuits.

With newer technologies the severity of these mechanisms increase as transistor sizes reduces and working frequencies increase.

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4.2 Soft Delay Error

In addition to SETs, radiation induced soft delay effects are also on the rise in newer circuit designs. Soft delay can be described as the amount of delay induced on a CMOS gate due to high-energy particle strike on its sensitive region, which happens only during signal switching [5]. For this, a high-energy particle should hit the sensitive node such as drain node of a CMOS gate's transistor while signal transition is taking place at the output. Then, the current generated due to particle hit can then pull down the signal in the opposite direction causing longer transition time. Incorrect data storage may occur if the delayed signal violates the timing requirements of the storage elements. In other words, a soft delay error (SDE) is created.

As an example, consider the circuit given in Fig. 4.1. A input pulse with a fall time of 200 ps has been connected to the input of the first inverter. While output Vo_1 transitions in a rising fashion, the NMOS transistor turns OFF and become susceptible to a particle strike. If a high energetic particle strikes node Vo_1 during this phase of transition, the generated current on NMOS transistor drain due to an SE hit (shown with the current source) can pull the signal in negative direction causing longer transition times. The delay effect is observable at the output of the succeeding gate(s), if the path is logically enabled.

The SPICE results for the time profile of the node voltages at Vo_1 and Vo_3 for 65 nm technology is shown in Fig. 4.2. Two inverters were used after the first inverter to filter out the distortion caused by the SE pulse. All inverters are taken as minimum size inverters. It was also assumed that the particle hit occurs near $V_{DD}/2$ for maximum delay effect. For a deposited charge of 100 fC, the soft delay amount (extra delay induced) at the output of the last inverter is more than 300 ps.

For high-reliability designs, SDEs must also be considered in the analysis in addition to SETs as the two error mechanisms are different in the way that they are masked.

For a logic circuit, three masking effects exist which prevent an SET from propagating and being latched by a memory element: logical, electrical, and latch-window masking. On the other hand, soft delay effects can only be masked by logical and latch-window masking. Hence, electrical masking effect does not apply

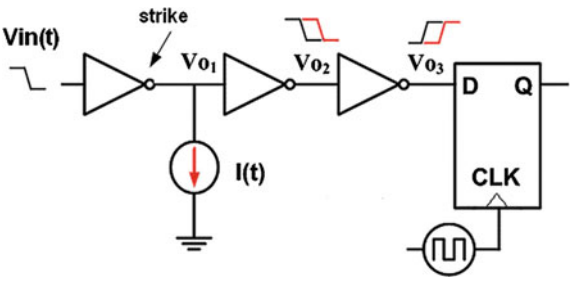

Fig. 4.1 Soft delay caused by a particle hit during rising transition on V_{o1}

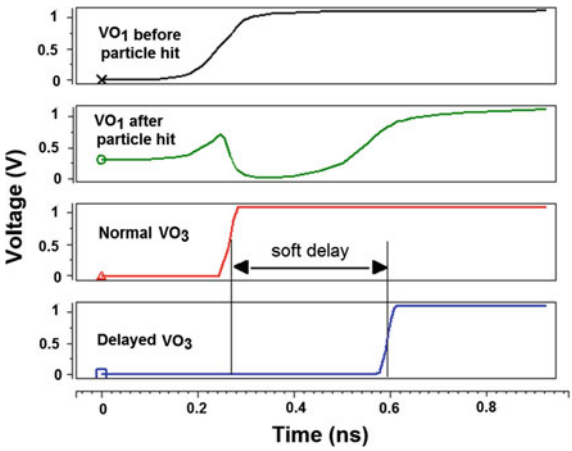

Fig. 4.2 Waveforms for 65 nm inverter chain obtained from SPICE simulations

to soft delay. If a signal is once delayed then it can propagate to circuit output(s) through functionally sensitized path(s) without any attenuation of the delay.

The critical charge for an SDE can be defined as the minimum charge collected due to a particle strike that produces sufficient delay such that the delayed signal arrives during the setup time of the storage element.

Gill et al. [5] have compared SET and soft delay sensitivities of various benchmark circuits for a maximum Linear Energy Transfer (LET) of 20 MeV. The results for some benchmark circuits indicated that a higher number of nodes were sensitive to soft delay effects than SETs due to absence of electrical masking in soft delay propagation.

It was reported that the soft delay effect will become more pronounced in newer technologies due to reduced circuit node capacitances [5]. Researchers have suggested the use of driver sizing technique in mitigating these soft delay effects, but this happens with the cost of some area and power penalties.

4.3 Radiation Induced Clock Jitter and Clock Pulse

The SE induced clock jitter, occurs when particles inject charge onto clock circuit nodes during the time clock edge is present [6]. As a result, clock edge moves back and forth causing wrong data to be eventually stored.

Figure 4.3 shows an example of a clock jitter in a flip-flop (FF) configuration where the signals IN, OUT and CLK denote input, output and clock signals respectively of the flip-flop. Figure 4.3a shows the FF output waveform when there is no clock upset i.e. in the absence of SE induced noise and Fig. 4.3b illustrates the same waveform after the occurrence of a clock jitter due to radiation. In the latter case, output signal OUT is delayed by T1 due to induced clock jitter. Assuming the output signal "OUT" is connected to another storage element, incorrect data storage

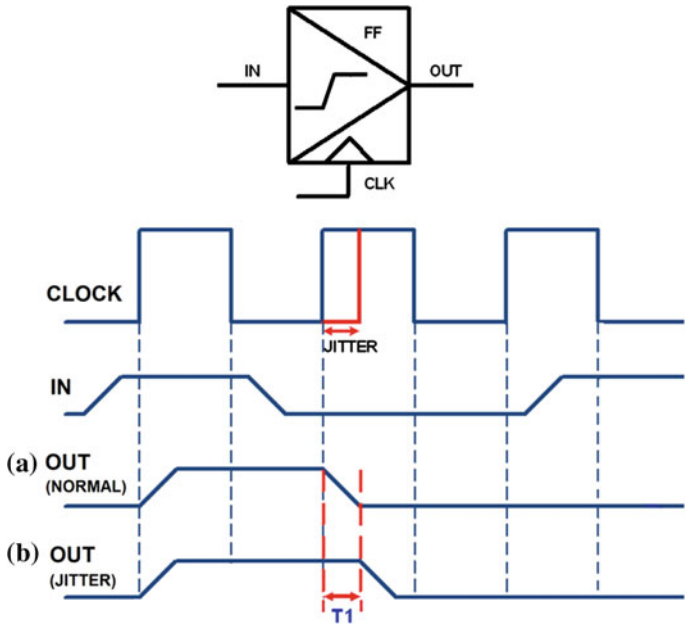

Fig. 4.3 SE induced clock jitter: Output waveform with no upset (**a**), and with jitter (**b**)

may occur if the delayed output signal arrives during the set-up time of the receiving sequential.

In addition to "clock jitter", an energetic particle strike can also create a "false clock pulse" on clock circuit nodes during when there is no clock pulse present. This effect is also known as "radiation induced race" [6]. If the pulse generated carries sufficient magnitude and width, it can be mistaken for a real clock signal. Finally, early latching of data may occur resulting in wrong data storage.

Figure 4.4 shows to the output of flip-flop when a False Clock Pulse is induced on the clock node due to SE hit driver. As a result, the data arrives early by a time T2 as shown. This early latching of data may result in wrong data storage.

In mitigating the SE Clock Pulse and Jitter effects, hardened pulse generators and pulse latches can be utilized as reported in [6].

4.4 Single Event Crosstalk Noise

4.4.1 Introduction

Researchers mostly ignored CL interconnects in single event analysis of CMOS circuits and focused only on the propagation of SET pulses through logic gates without regards to interconnects between them. With increasing coupling effects, an

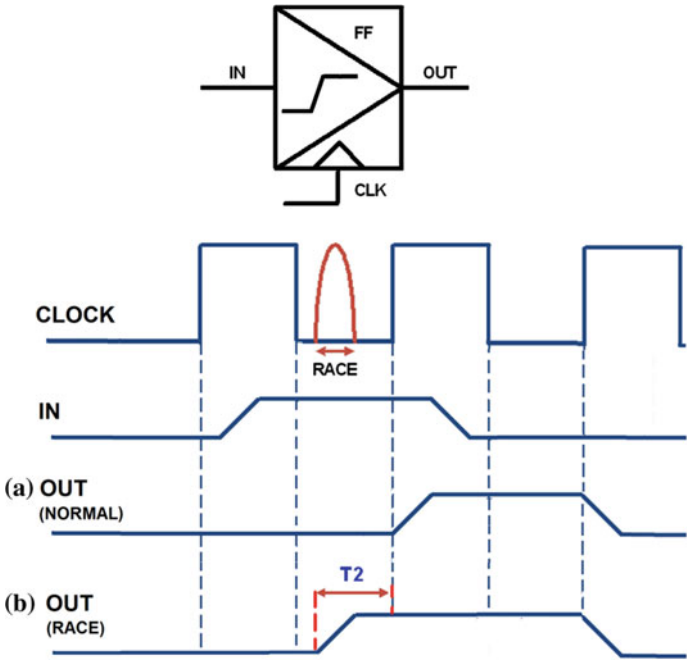

Fig. 4.4 SE induced clock race: Output waveform with no upset (**a**), and with race (**b**)

SET pulse generated on a circuit node is no longer limited to the logic path existing between the hit node and a latch. The interconnect coupling effects can cause SETs to contaminate electronically unrelated circuit paths which can in turn increase the circuit SE susceptibility.

With advances in technology scaling, increasing cross coupling effects occur due to reduced spacing and increased aspect (thickness to width) ratio of interconnects. The interaction caused by parasitic coupling between wires, that is known as crosstalk, may cause undesired effects such as positive and negative glitches, overshoot, undershoot, signal delays or even delay reduction [11, 12]. If crosstalk effects on the *victim net* (affected line) are large, they can propagate into storage elements that are connected to victim line and can cause logic errors.

A crosstalk glitch occurs when there is a voltage transition in one or more of several coupled lines. In this case, other non-switching or victim wires suffer a voltage perturbation or a glitch. If the crosstalk glitch generated on the victim line is large and propagates into a storage element during its latching window, incorrect data storage will occur. Until relatively recently, only normal signal switching on *aggressor* (affecting) lines were responsible for such crosstalk events. As technology scaling continues, SE transient effects generated on an aggressor line due to a particle hit may also create increasing coupling noise effects. It was also shown that an SET on aggressor line can cause larger crosstalk effects than a normal switching crosstalk after a certain deposited charge [7].

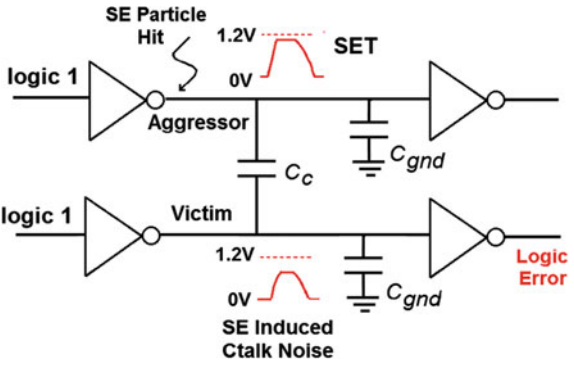

Fig. 4.5 Crosstalk noise caused by an SE particle on aggressor line

In order to demonstrate how single event crosstalk noise (SECN) occurs, first consider the circuit shown in Fig. 4.5. This setup shows the aggressor-victim pair with its drivers and receivers. Since the both driver inputs are held at logic 1 (1.2 V), the outputs are normally at logic 0. An SE hit at the drain of OFF PMOS transistor of the aggressor driver causes output to go to logic 1 for some duration. The SET voltage created then affects victim line via coupling capacitor C_c, inducing SE Crosstalk noise on the victim. The positive glitch created causes incorrect switching of victim receiver giving a logic error.

As this example show, SE hits can generate cross-coupling effects that can violate noise margins of gates connected to the affected line and may result in logic errors. Serious effects may occur if the affected line is somewhat important such as a clock line. Crosstalk noise effects on a clock network may have multiple effects on areas much farther from the originating source of the SE crosstalk point. An upset can be interpreted as a clock edge potentially causing many different bits to be stored incorrectly (multiple upsets). Due to the large area covered by clocking interconnects there is a higher probability that coupling from neighboring interconnects can have an impact on clocking network [13].

In addition, Triple-Modular Redundancy (TMR) circuits that are used to eliminate Single Event Errors on CL are also susceptible to crosstalk at the inputs of voters. It was shown in [14] that an undesired coupling among voter inputs can invalidate the data. This may be possible since the interconnections between functional units and voters tend to be long and hence sensitive to crosstalk. If coupling effects are strong, an SET in one redundant circuit may result in the error appearing on the voting circuit more than once which can cause data corruption.

It has been shown that SETs can produce crosstalk effects that induce logic level state changes for interconnects as small as 100 μm on technologies 90 nm and lower [9]. Another work has experimentally measured the SE induced crosstalk in a 90 nm process and proved the existence of the problem [15].

Hence, the cross-coupling effects among interconnects need to be considered in *SE analysis*, *modeling* and *hardening* of CMOS combinational logic gates due to technology scaling effects that increase both SE susceptibility and crosstalk effects.

4.4.2 Analysis Single Event Crosstalk

This section first analyzes SE crosstalk effects and then compares to normal switching crosstalk to see if these effects important. The earlier work in [7] has studied crosstalk effects induced by SE transients for various interconnect lengths and deposited charges up to 1 pC. However, as for the interconnect, a simple lumped RC modeling has been used which may not be very accurate.

In the simple lumped RC model, the total resistance of the wire is lumped into one single resistance R and similarly the global capacitance of the wire is combined into a single capacitor C. However, this provides a very rough approximation of the actual transient behavior of interconnect.

The accuracy of the simple lumped RC model can be improved by dividing the total line capacitance into two equal parts, as shown in Fig. 4.6. This representation is named as the π-model representation [16].

More accurate representation of a distributed RC circuit can be obtained by using multiple-π segments. In an N-π representation, the total resistance and capacitance values of each π-segment are given as R/N and C/N, respectively. Since the capacitors are split equally on each side, the ground capacitors are calculated as C/2 N for each π-segment. The capacitor values at intermediate nodes would be doubled due to the neighboring π segment (Fig. 4.7).

Accuracy of the model increases as the number of segments increase, and the transient behavior approaches that of a distributed *RC* line. Kawaguchi and Sakurai have reported that the error in simulating delay of the distributed RC line by using 5-π segment is less than 1 % for almost all cases [17].

Researchers often use the 10-π model, to represent the distributed RC line in Spice simulations when comparing the accuracy of closed form expressions for

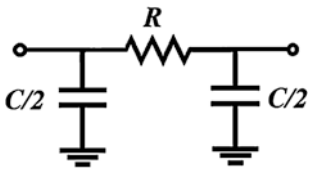

Fig. 4.6 π-model representation

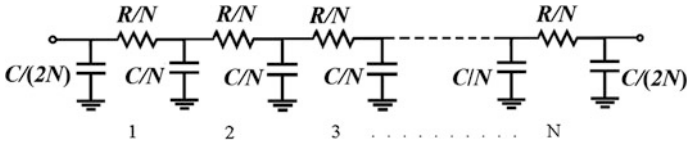

Fig. 4.7 N segment π-model representation

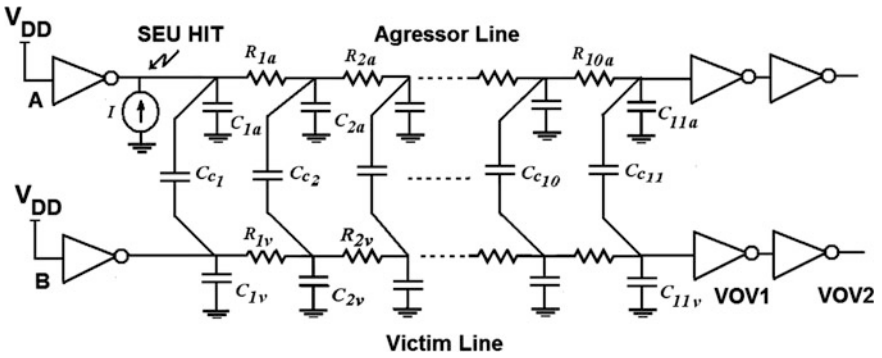

Fig. 4.8 Experimental setup for SECN

crosstalk [18, 19]. Therefore, the 10-π model is considered as the distributed line model in simulation analysis.

In the SE crosstalk analysis presented, a 10-π model (10-π segments) with distributed coupling capacitances is used for every 100 μm of wire to represent the RC distributed behavior (see Fig. 4.8).

Inductance effects in on-chip interconnects becomes increasingly important with smaller rise times and lower wire resistance especially in global interconnects. However for most on-chip lines or interconnects, capacitive effects are still the dominant factor [11, 12]. Hence, in the analysis, inductance effects are ignored and capacitive coupling is assumed as the dominant mechanism for crosstalk.

Two parallel interconnects on the intermediate layer in 65 nm technology are considered with wire dimensions taken as follows: the width (W), spacing (S) is 0.14 μm, and wire thickness T is 0.35 μm [20]. A wire length of 500 μm is chosen for the intermediate wire.

It is also assumed that aggressor and victim driver sizes are 0.26μm/0.13μm (W_p/W_n) and the loads at the end of the wires are minimum sized identical inverters. Here, the receiver gates are taken as minimum size in order to maximize the crosstalk noise effects. At the end of the line, receiver gates act as load capacitances and contribute to the stability of aggressor and victim lines. Hence, smaller driver sizes are selected to maximize the crosstalk noise.

In the experimental setup shown in Fig. 4.8, both the aggressor and victim driver inputs are connected to "logic high". In this case, normally aggressor driver output would be at "logic low", however it would be taken to "logic high" if there is a sufficient SE hit charge on output node of the aggressor driver.

An SE hit was simulated at the output of the first inverter using a double exponential current pulse that is given by:

$$I(t) = \frac{Q}{t_\alpha - t_\beta}\left(e^{-t/t_\alpha} - e^{-t/t_\beta}\right) \tag{4.1}$$

where,

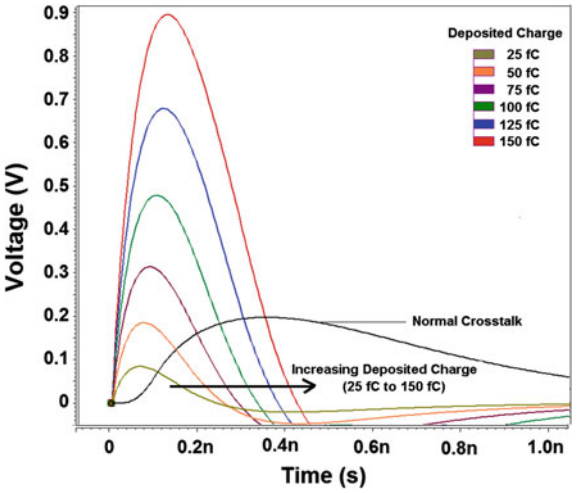

Fig. 4.9 Switching induced versus SE crosstalk noise at varying deposited charge

Q is the charge (positive or negative) deposited by the particle strike, t_α is the collection time constant of the p-n junction, t_β is the ion-track establishment time constant.

The time constants t_α and t_β are dependent on process technology and are taken as 100 and 5 ps, respectively based on [21]. Alternatively, the single exponential current model given in [22] may also be used. Researchers in [23, 24] mention that the single pole model can be replaced by double exponential current pulse model for SEUs without loss of generality. The double pole representation has been used here as an approximation to waveforms seen in mixed-mode simulations.

Figure 4.9 compares the SE induced coupling noise to the normal aggressor switching induced crosstalk on the victim line for a V_{DD} of 1.2 V. Varying deposited charges in between 25–150 fC were selected in simulations.

Referring to Fig. 4.9, the SE crosstalk amplitude can easily exceed normal crosstalk amplitude for SEU hit charges above 60 fC and can reach amplitudes as large as four times the regular crosstalk noise amplitude. Besides increasing charge levels, one reason is due to the fact that an SET waveform transitions much rapidly compared to normal aggressor waveform, and in turn induces more coupling noise on the victim line. In summary, although a given net passes the normal crosstalk noise check, it may still pose a threat if SE crosstalk effects are not properly considered.

The effect of different wire lengths has also been examined. For a fixed deposited charge, when the wire length is decreased, the SE coupling noise width decreases and becomes less comparable to regular crosstalk noise width. For longer lengths, the width of the noise pulse has increased. For both cases, the SE crosstalk noise amplitude, on the other hand, remained relatively constant.

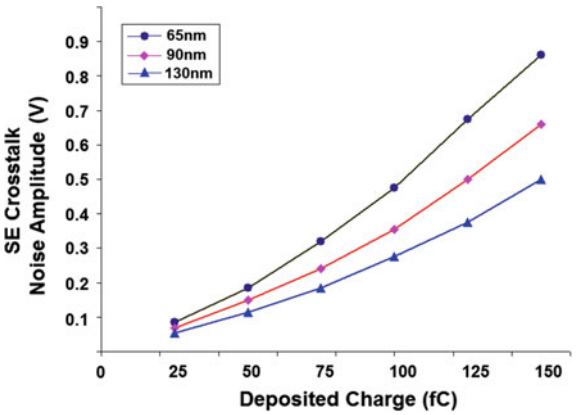

Fig. 4.10 SE induced crosstalk amplitude versus technology

Figure 4.10 shows the effect of various deposited charges on SECN magnitude. The results here are shown for 130, 90 and 65 nm technologies. Figure indicates that SE crosstalk amplitude increases in proportion to the deposited charge in all three technologies and shows the vulnerability of circuits to SECN as feature sizes scale down. A 125 fC hit charge causes crosstalk noise amplitude of 380 mV in 130 nm technology, while the same charge causes a noise amplitude of 675 mV in 65 nm technology node.

4.4.3 Comparison Between SECN and SET Effects

In order to compare SET to SE crosstalk, we have used the circuit shown in Fig. 4.11 for SET simulation and the set-up shown in Fig. 4.8 for SECN simulation. Referring to Fig. 4.11, as in SE crosstalk simulation, the hit driver has been sized at 2X while the following inverters have been taken as minimum size (1X) inverters, similar to victim line end inverters in Fig. 4.8.

An SE hit has been simulated at the output of the first inverter using a double exponential source and the hit charges needed to cause switching on the following

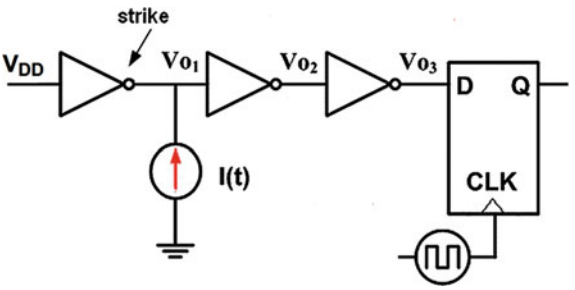

Fig. 4.11 SET simulation setup

Table 4.1 Minimum hit charges needed for SET and SE crosstalk propagation

SE Effect (nm)	130	90	65
SET (fC)	26.8	21.4	17.5
SECN (fC)	165.4	137.4	113.1

inverters have been determined. Then similarly in Fig. 4.8, the victim receiver waveforms V_{OV1} and V_{OV2} have been observed for switching activity and required minimum deposited charges needed on the aggressor driver output have been determined. Table 4.1 shows the results obtained for all three technologies.

In all three technologies considered, the SE crosstalk effect requires approximately six times more deposited charge in order to cause switching on the receiver gate, but when this happens, multiple SEU effects occur. For example, a 120 fC deposited charge in 65 nm technology results in switching of both aggressor and victim receivers.

In order to study the effect of SE crosstalk on circuit reliability, the error rate (SER) or probability contribution should be identified. For this, the ALU and ACCU (Adder/Accumulator) modules from AM2901 4-bit microprocessor bit-slice have been selected for SER simulations. Although the AM2901 bit-slice is dated, the selected modules include large number of nodes and many gates. For example, the ALU module itself contains 83 gates, 12 input and 10 outputs and 276 SE vulnerable nodes [25].

Due to large number of the simulations that need to be completed, only 90 and 65 nm technologies are considered. The circuit has been laid out in 90 and 65 nm technologies using Microwind CMOS layout design and simulation tool. The minimum allowable spacing between wires has been taken during the routing process. All circuit parasitic information has been extracted and the resulting Spice file has been simulated with and without considering the SECN effects. In calculating the SER without any crosstalk effects, the cross-coupling capacitances among wires have been ignored during simulations.

The simulation methodology assumes that, with a particle strike, positive or negative charges up to 150 fC are equally likely to be generated. Different charge injection levels from 10 to 150 fC have been evaluated. It is also assumed that no timing window masking occurs, i.e., once an SET reaches at one of the circuit's outputs, it has been assumed that soft error condition is generated.

The simulations are also performed for only randomly selected input combinations from which a reasonably accurate SER estimate can be obtained [26]. Assuming, the particle density at sea level (New York) (around 100,000/cm^2/yr), MTTF was calculated using probability *POFC* (see Sect. 1.3.1).

Figure 4.12 shows the calculated SER values of the ALU and ACCU modules for 90 and 65 nm technologies considered. For both technologies, the probability of failure increases as SECN effects are included. As a result, the MTTF values reduce with coupling.

The MTTF values for the test circuits decreases on the average by 11.6, and 13.7 %, respectively, for 90 and 65 nm technologies when coupling effects are

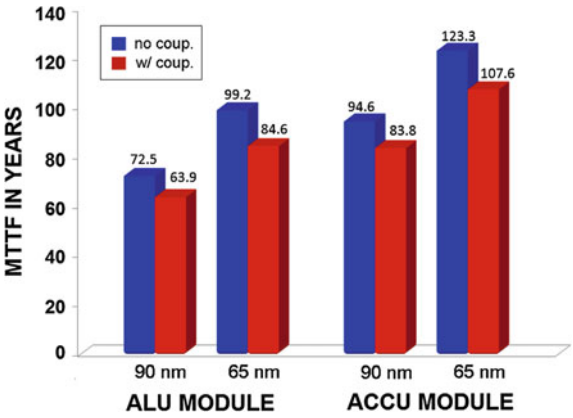

Fig. 4.12 SE crosstalk contribution to SER

included. This indicates that SECN effects increase circuit sensitivity to radiation and hence need to be incorporated in reliability analysis especially for mission-critical applications.

Referring the Fig. 4.12 we can also notice that the MTTF values increase in 65 nm technology for the same circuitry. The reduction in circuit size offsets the effect of increased circuit sensitivity in 65 nm. The circuit area is about 50 % smaller compared to 90 nm technologies, as a result, the probability of failure decreases in 65 nm.

4.5 Single Event Crosstalk Delay Effects

Single event transients generated on the affecting wire (due to particle hits on driver transistors) may also cause increased signal delays on neighboring (victim) wires via cross-coupling effects if these lines are in switching. The delay change at victim receiver inputs can later translate into setup time violations on the storage elements that are connected to these receivers.

4.5.1 Analysis Single Event Coupling Delay

If an SET on aggressor wire causes delay increase on the victim line via coupling effects, this effect is called as SE induced Crosstalk Delay or SECD [10].

In the example shown in Fig. 4.13, an SE particle hits the output node of aggressor driver and causes a voltage transient in positive direction. The transient then spreads into the victim line via coupling capacitance and causes a signal slowdown as shown on the victim line shown.

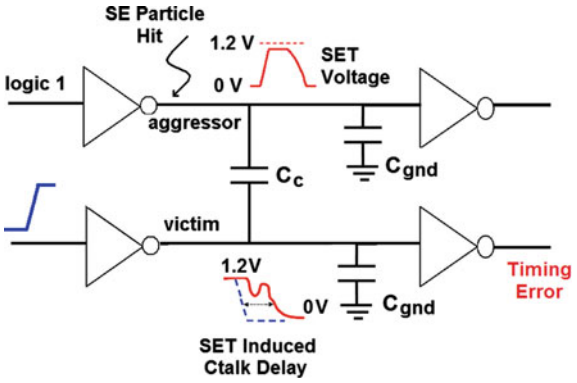

Fig. 4.13 SE crosstalk delay (lumped wire model is for demonstration only)

The increase in interconnect delay due to the SET coupling can affect circuit performance as delay changes may later violate the setup time requirements of logic storage circuits connected to these receivers. It will be also shown later that SE crosstalk delay effect can exceed the normal crosstalk delay above a certain deposited charge. The circuit may experience timing violations even after mitigation measures are taken to minimize normal crosstalk delay. During layout optimization, the wires might be spaced out enough to prevent timing violations caused by normal aggressor switching. However, the protection taken may not be sufficient, as delay caused by SE crosstalk effect can be larger.

In the analysis, a 10-π model with distributed coupling capacitances is used for every 200 μm of wire to represent the RC distributed behavior. The same 500 μm long interconnect system and driver sizes discussed earlier in Sect. 4.4.2 have been considered in simulations. The inductance effects have been ignored and capacitive coupling has been assumed as the dominant mechanism for crosstalk. A rising pulse waveform with a 100 ps rise time has been applied to victim driver while aggressor driver was kept at V_{DD} as shown in Fig. 4.14. An SE hit charge of 150 fC has been

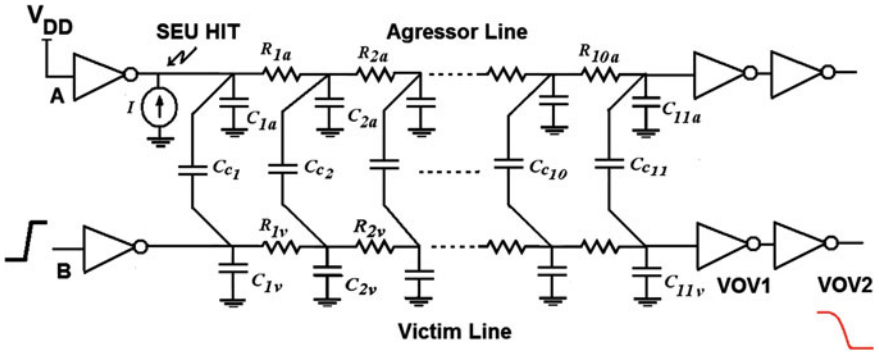

Fig. 4.14 Simulation setup used for SE induced crosstalk noise

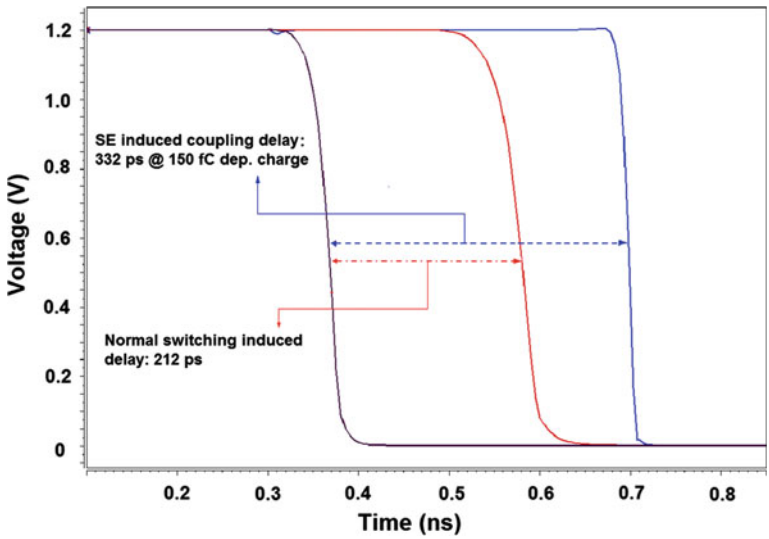

Fig. 4.15 SE induced coupling delay versus switching induced delay at output node V_{OV2}

simulated at the end of the aggressor driver to examine the effect of SET on victim line delay. Two inverters have been used to filter out the distortion on victim line and the delay is measured at V_{OV2}.

When comparing the SECD to the normal aggressor switching induced delay, the SE current source has been removed and aggressor driver is switched in opposite direction to the victim. In order to have maximum delay effect on victim line, aggressor slew rate has been selected two times larger than victim slew rate [27].

Figure 4.15 shows various delays calculated for the circuit at the output node "V_{OV2}" shown in Fig. 4.14. The victim line delay without any crosstalk effect (no aggressor switching or SE transient) is taken as reference to calculate the induced delay for each case. It can be seen from the figure that above a certain SE hit charge; an SET can induce larger delays on the neighboring wire compared to a regular crosstalk delay. At a 150 fC of deposited charge on aggressor driver, the induced delay on output node was more than 50 % larger than the delay induced by normal aggressor switching. During layout optimization, the wires might be spaced out enough to prevent timing violations caused by normal aggressor switching. However, the protection may not be sufficient, as the delay caused by SE coupling can be larger.

Figure 4.16 shows the effect of various deposited charge on SECD for all three technologies considered. From the figure, we observe that the delay increases in proportion to deposited charge in all three technologies.

For newer technologies, the same hit charge can cause larger crosstalk delays. For example, a 100 fC of deposited charge induces 153 ps victim line delay in

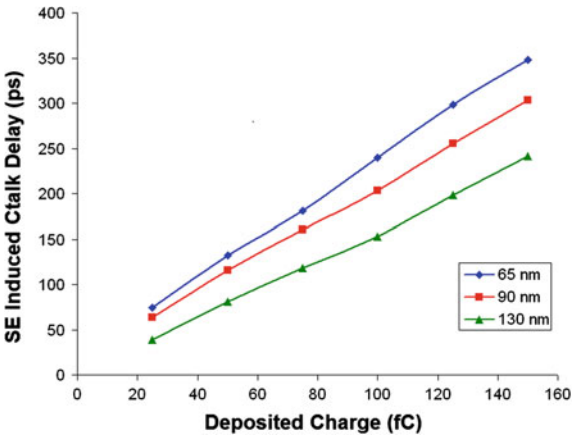

Fig. 4.16 SE induced coupling delay versus deposited charge in 130, 90 and 65 nm technologies

130 nm technology while the same charge can induce 240 ps delay in 65 nm. The effect of SECD increases as device sizes scale down.

4.5.2 Comparison Between SE Crosstalk Delay and Soft Delay

In order to compare soft delay to SE crosstalk delay, the set-up shown in Fig. 4.11 has been utilized for soft delay simulation and the results are compared to that of SECD.

Referring to Fig. 4.11, a rising pulse waveform with a 100 ps rise time has been connected to the input of the first inverter (instead of V_{DD}) for soft delay simulation. An input pulse with a rise time of 100 ps has been connected to the input of the first inverter. The hit driver has been sized at 2X with the second and third inverters taken as minimum size inverters. These inverters filter out the distortion caused by the SE pulse and the delay is measured finally at V_{O3}. For soft delay simulation, an SE hit has been injected at the output of the first inverter (V_{O1}) around halfway the falling signal transition in order to maximize the induced delay amount.

In order to analyze the SECD, we consider the same the set-up shown in Fig. 4.14. A rising pulse waveform with a 100 ps rise time again has been applied to victim driver while aggressor driver was kept at V_{DD}. An SE hit charge of up to 150 fC has been simulated at the end of the aggressor driver to examine the effect of SET on victim line delay. Similar to soft delay setup, the aggressor and victim driver sizes were taken at 2X size (W_p/W_n = 0.26 μm/0.13 μm) and the loads at the end of the wires was minimum sized 1X inverters. Two inverters have also been used to filter out the distortion on victim line and the delay is measured at V_{OV2}.

Figures 4.17, 4.18 and 4.19 shows the resulting SE crosstalk and soft delays for 130, 90 and 65 nm technologies considered.

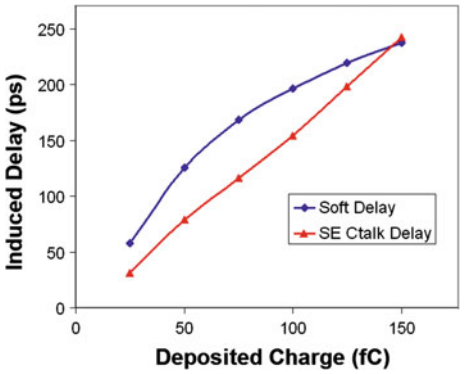

Fig. 4.17 SE induced crosstalk delay versus soft delay for 130 nm technology

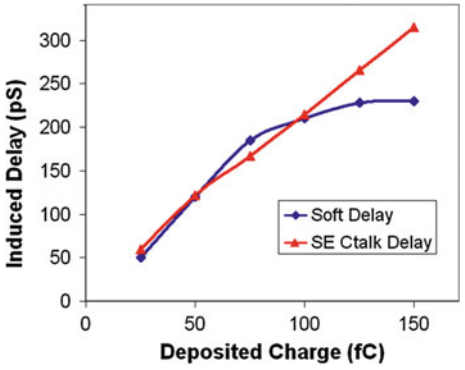

Fig. 4.18 SE induced crosstalk delay versus soft delay for 90 nm technology

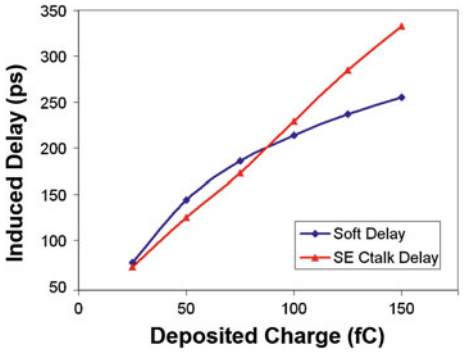

Fig. 4.19 SE induced crosstalk delay versus soft delay for 65 nm technology

These plots indicate that the SE induced coupling delay is quite comparable to the soft delay effect in all three technologies considered. As the deposited charge value increases, soft delay increase seems to slow down. This delay saturation effect was also observed in inverter and NAND gates considered in [5].

It was also observed that, after a particular deposited charge, the SECD exceeds the soft delay amount in all three technologies considered. These charges were at 145, 105 and 85 fC for 130, 90 and 65 nm technologies, respectively.

In contrast to soft delay case, the presence of interconnect coupling effectively transfers the deposited charge to neighbor line and hence delay saturation effects was not observed for terrestrial charge levels considered.

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Chapter 5
Modeling Single Event Crosstalk Noise in Nanometer Technologies

5.1 Introduction

For high-reliability, mission critical applications, such as military or medical systems, SE crosstalk effects must also be in reliability analysis included in addition to SETs. In addition, a given net may pass the normal crosstalk noise check, but it may still pose a threat if SE crosstalk effects are not properly considered as discussed in previous chapter.

Although, previous works studied the SE crosstalk to some extent, there has been little work in the modeling of SE crosstalk effects. With modeling of SECN, not only computational time efficiency could be obtained, but also researchers could gain insight into the effects of SE pulse transients on the crosstalk noise. With closed-form expressions, the crosstalk pulse dependency on various design parameters can be observed via sensitivity expressions obtained.

Traditional SPICE simulators can be used to estimate crosstalk effects in signal lines. While results are accurate, due to millions of nets to be handled, these simulations are time inefficient [1–3].

The method explained here uses an accurate 4-π model for interconnect and correctly models the loading effect of neighboring lines and net tree branches noting the resistive shielding effect. The dominant pole approximation is used in moderation which resulted in increased accuracy of model.

5.2 The 4-π Template for Single Event Crosstalk Modeling

The SE crosstalk model to be discussed here models both the victim and aggressor nets using the 2-π circuits, and hence the naming of this model is called the 4-π interconnect model [2–4].

S. Sayil, *Soft Error Mechanisms, Modeling and Mitigation*,
DOI 10.1007/978-3-319-30607-0_5

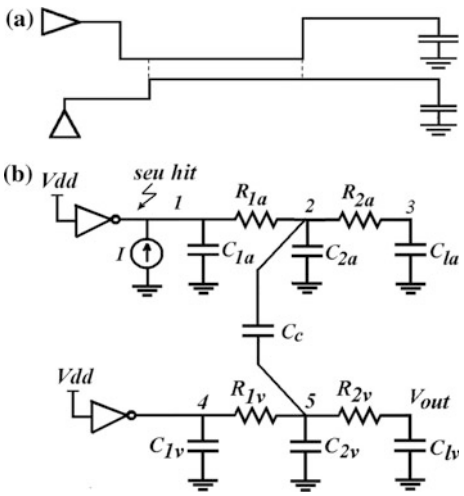

Fig. 5.1 The 4-π SECN model for coupled interconnects

In this model, RC parameter values are calculated based on technology and the geometric information from Fig. 5.1a. The coupling node (node 2) is set to be the center of the coupling portion of the victim net. We assume the upstream and downstream resistance/capacitance at node 2 to be R_{1a}/C_{ua} and R_{2a}/C_{da}, respectively. Similarly for victim net, let's assume upstream and downstream resistance/capacitance at node 5 to be R_{1v}/C_{uv} and R_{2v}/C_{dv}, respectively. Then, for aggressor and the victim line:

$$C_{1a} = C_{ua}/2, C_{2a} = (C_{ua} + C_{da})/2 \quad \text{and,} \quad C_{la} = C_{da}/2 + C_{lda}$$
$$C_{1v} = C_{uv}/2, C_{2v} = (C_{uv} + C_{dv})/2 \quad \text{and,} \quad C_{lv} = C_{dv}/2 + C_{ldv}$$

where,

C_{lda} and C_{ldv} represent the load capacitances for aggressor and victim lines, respectively.

For most on-chip lines or interconnects, capacitive effects are still the dominant factor hence inductance is ignored in the modeling.

The current source in Fig. 5.1 represents an SE hit at the output of aggressor driver. The classical double exponential current pulse model is often used in simulations to represent transient currents induced due to radiation. The modeling approach here is based on a combined approach where device simulations are first used to characterize current pulses for ion strikes and then these pulses are later used as inputs to HSPICE simulations to emulate ion strikes [5, 6].

For this purpose, the data obtained from device simulations are fitted to a double exponential pulse model [given in (5.1)] with appropriate characteristic parameters. This model assumes that the SE current pulse exhibits an exponential behavior during its rise and decay. The SE crosstalk noise amplitude, on the other hand, is determined mainly by the rising edge of the SET waveform which occurs in picoseconds; hence the effect that this mismatch has during the falling phase has been ignored.

The double exponential model given in (5.1) is composed of an exponential function accounting for the rise in magnitude of the resulting single-event current and another exponential function modeling the decay in magnitude of this current.

$$I(t) = \begin{cases} I_{\max}(1 - e^{-t/\tau_1}) & \text{if } t < t_d \\ I_{\max} e^{-(t-t_d)/\tau_2} & \text{if } t \geq t_d \end{cases} \tag{5.1}$$

where,

τ_1 and τ_2 are the rise and the fall time constants of ion-induced current pulse, respectively. I_{max} is its magnitude, and t_d is the delay time for the falling exponential that controls the duration of the plateau effect.

These values are computed using TCAD simulations of ion strikes in the drain junctions for different LETs up to 15 MeV.

Referring to Fig. 5.1, it has been assumed that both victim and aggressor driver inputs are at logic 1 and a positive charge deposition occurs on aggressor driver output due to an SE strike. Figure 5.2 shows the new equivalent after including the holding resistances of both drivers.

The effective resistances R_{da} and R_{dv} model the holding resistances of aggressor and victim drivers, respectively [4]. Each holding resistance models the effect of on transistors (NMOS) that dissipate the charge and restore the node to its original logic value.

The victim driver can be represented approximately by its pull-down network resistance (NMOS transistor holding resistance) since it stays in the linear region [7, 8]. However, the same may not true for the aggressor driver. Even for fairly low LET particles, an SET can easily exceed V_{DD}-V_{TN} and reach to supply voltage level as often predicted by device simulations. In this case, the NMOS transistor exits from its linear region and enters into saturation region.

In this case, using DC analysis, the holding resistance can be pre-characterized using stable input (V_{DD}), with the output voltage sweeping from 0 to V_{DD} [9]. If the output voltage is taken at V_{DD}, the largest value of holding resistance is obtained from this simulation. If this value is utilized in calculation, it would cause an overestimation of the SE crosstalk noise since the SET waveform changes and not

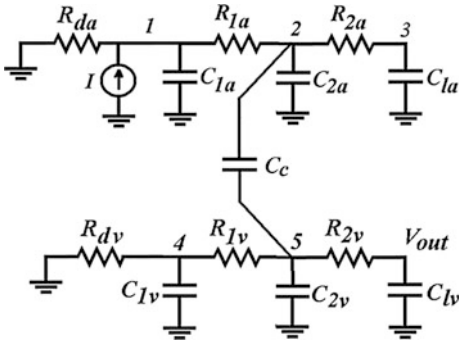

Fig. 5.2 SE crosstalk calculation using the 4-π template circuit

fixed at V_{DD}. In SE crosstalk modeling, the medium value of the holding resistance has been selected as an approximation, which is taken at the mid-point of the 0 to V_{DD} range [9].

The multiline crosstalk model proposed in [10] has been adopted for SE crosstalk estimation in this method. In this model, the loading effects of non-switching (passive) aggressors and aggressor tree branches are correctly modeled using equivalent capacitances. The model is advantageous over techniques which simply use lumped capacitors as in [2] at coupling/branching point. These equivalent capacitance values are derived noting the aggressor waveform and the resistive shielding effect.

The line where the SET generates due to particle strike is taken as the active aggressor, while any other nets coupled to the victim are considered as passive aggressor lines. It is also assumed that none of the lines switch during particle hit so that SE crosstalk noise is generated.

5.3 Modeling of Passive Aggressors

A victim line may be coupled to many passive aggressors. A passive aggressor follows victim waveform and contributes to the stability of the victim line and hence simply cannot be taken as a coupling capacitor at victim coupling point. The equivalent load capacitance at the victim coupling point becomes less than coupling capacitance and can be formulated using coupling/branching admittance concept [10, 11]. The equivalent capacitance formula for a passive aggressor is derived assuming an exponential aggressor waveform at node V.

For this, the passive aggressor is first reduced to the simple circuit shown in Fig. 5.3, where:

$$R'_a = R_{th} + R_{1a} \tag{5.2}$$

$$C'_a = C_{2a} + C_{la} + (R_{th}^2/(R_{th} + R_{1a})^2)C_{1a} \tag{5.3}$$

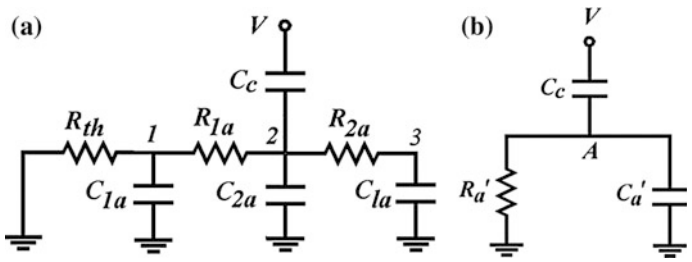

Fig. 5.3 A passive aggressor net coupled to the victim line

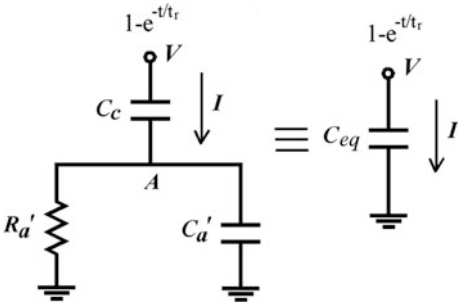

Fig. 5.4 Passive aggressor line reduction

Then, for matching purposes, the victim waveform is assumed to be a normalized exponential voltage. Referring to Fig. 5.4, the currents coming from victim node should be same both cases:

$$I = C_c\left[\frac{dV_V(t)}{dt} - \frac{dV_A(t)}{dt}\right] = C_{eq}\frac{dV_V(t)}{dt} \tag{5.4}$$

Assuming zero initial condition and an exponential waveform, we can calculate the equivalent capacitance, C_{eq} by integrating (5.4) over $0 \le t \le 5t_r$ interval (where t_r is the exponential rise time constant). Here, it is assumed that the exponential waveform reaches its final value at $t = 5t_r$. Then, the equivalent capacitance value for a passive aggressor is given by:

$$C_{eq} = C_c[1 - V_A(5t_r)] \tag{5.5}$$

Now, considering left part of Fig. 5.4, we can also write a KCL equation at node A, giving:

$$C_c\left[\frac{dV_V(t)}{dt}\right] = (C_c + C'_a)\frac{dV_A(t)}{dt} + \frac{V_A(t)}{R'_a} \tag{5.6}$$

$$V_A(t) = \frac{C_c R'_a}{t_r - R'_a(C_c + C'_a)}\left[e^{-\frac{t}{t_r}} - e^{\frac{-t}{R'_a(C_c + C'_a)}}\right] \tag{5.7}$$

Inserting $V_A(5t_r)$ in (5.5), C_{eq} formula is given as:

$$C_{eq} = C_c\left[1 + \frac{C_c R'_a}{t_r - R'_a(C'_a + C_c)} \cdot e^{\frac{-5t_r}{R'_a(C'_a + C_c)}}\right] \tag{5.8}$$

A passive aggressor coupled to the victim line can now be represented by an equivalent capacitor using (5.8) and this capacitor updates the value of C_{2v} at node 5 (see Fig. 5.2). Finally, the circuit would reduce to the one in Fig. 5.2.

5.4 RC Trees and Branch Reduction

There can be aggressor net branches at the branching point. The capacitance seen at the branching node is less than the total branch capacitance due to resistive shielding effect [10], and hence needs to be correctly formulated. For this, the tree branches are reduced to a simple π-model following the moment matching method as demonstrated in [11]. This model is then reduced to an equivalent branching capacitance C_{eq-br} (Fig. 5.5) considering an exponential waveform on input node A.

For this, we can equate the currents on node A for both circuits:

$$C_{eq-br}\frac{dV_A(t)}{dt} = C_a\frac{dV_A(t)}{dt} + C_b\frac{dV_B(t)}{dt} \tag{5.9}$$

Assuming a rising exponential voltage at input node and zero initial condition, we can obtain an equivalent branching capacitance after integrating both sides of above equation over $0 \le t \le 5t_r$ time interval:

$$C_{eq-br} = C_a + C_b V_B(5t_r) \tag{5.10}$$

Then, after applying KCL theorem on node B, one obtains:

$$\frac{dV_B(t)}{dt} + \frac{V_B(t)}{RC_b} = \frac{1 - e^{-t/tr}}{RC_b} \tag{5.11}$$

After solving the differential equation and inserting $t = 5t_r$

$$V_B(5t_r) = 1 + \frac{RC_b}{t_r - RC_b}e^{-5t_r/RC_b} \tag{5.12}$$

Finally, this value can be inserted in (5.10) giving the formulation:

$$C_{eq-br} = C_a + C_b\left[1 + \frac{RC_b}{t_r - RC_b}e^{-5t_r/RC_b}\right] \tag{5.13}$$

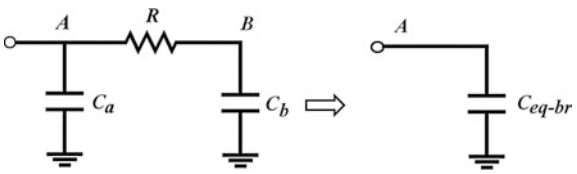

Fig. 5.5 Passive aggressor line reduction

5.5 Aggressor Waveform at the Coupling Node

In the model, the aggressor waveform at the coupling node is first calculated and then entered to the transfer function between the coupling node and the victim output to obtain victim noise voltage. In order to calculate aggressor coupling node waveform correctly on node 2 (see Fig. 5.2), the victim loading effect needs to be included. For this, the victim line is first reduced into an equivalent capacitor C_{eqv} using the quiet aggressor/victim net reduction techniques as summarized in Sect. 5.3.

Following C_{eqv} calculation, a source transformation is also implemented on aggressor input giving the final circuit shown in Fig. 5.6. As shown in this figure, the voltage source resulting from source transformation has been represented using two voltage sources in series.

For convenience in formulation, an alternative version of Eq. (5.1) has been utilized in calculations:

$$I(t) = I_{\max}(1 - e^{-t/\tau_1}) - I_{\max}(1 - e^{-(t-t_d)/\tau_2})u(t - t_d) \quad \text{for t} > 0 \tag{5.14}$$

The sources V_{in1} and V_{in2} are then given as:

$$V_{in1} = I_{\max}R_{da}(1 - e^{-t/\tau_1}) \tag{5.15}$$

$$V_{in2} = -I_{\max}R_{da}(1 - e^{-(t-t_d)/\tau_2})u(t - t_d) \tag{5.16}$$

respectively.

We consider one input at a time (V_{in1} or V_{in2}) using Superposition to find the coupling node waveform. For this, the aggressor branches after the coupling point are also reduced to an equivalent capacitance C_{req} using the tree branch reduction techniques given earlier (see Fig. 5.7). The equivalent branching capacitance for V_{in1} (C_{req-1}) is given by:

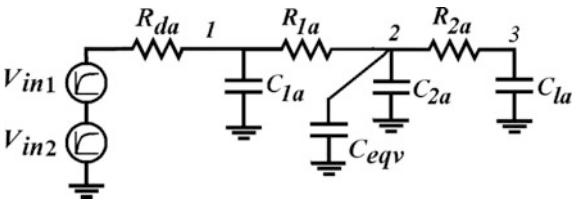

Fig. 5.6 Decoupled aggressor line for coupling node voltage calculation

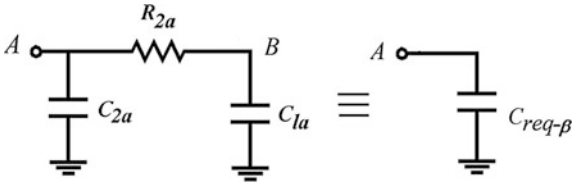

Fig. 5.7 Tree branch reduction on right part of aggressor net

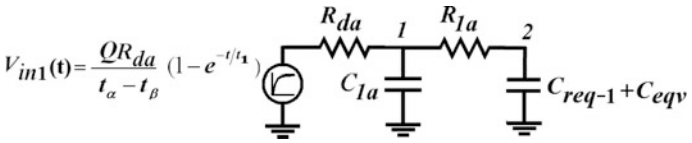

Fig. 5.8 Aggressor waveform calculation at the coupling node

$$C_{req-1} = C_{2a} + C_{la}\left[1 + \frac{R_{2a}C_{la}}{\tau_1 - R_{2a}C_{la}} e^{\frac{-5\tau_1}{R_{2a}C_{la}}}\right] \tag{5.17}$$

Figure 5.8 shows the resulting circuit for coupling node voltage calculation (shown for V_{in1} input). The transfer function between the input and coupling node 2 is calculated as:

$$\frac{V_2(s)}{V_{in}(s)} = \frac{1}{st_{a1} + 1} \tag{5.18}$$

where,

$$t_{a1} = C_{1a}R_{da} + (C_{eqv} + C_{req-1})(R_{da} + R_{1a})$$

Note that t_{a1} in fact is the Elmore delay between the input and Node 2. Finally, the delayed waveform at coupling node for the first input is calculated to be:

$$V_2'(t) = I_{\max}R_{da}(1 - e^{-t/\tau_{1n}}) \tag{5.19}$$

where,

$$\tau_{1n} = \tau_1 + t_{a1}$$

Similarly, the delayed waveform at coupling node due to V_{in2} (Fig. 5.6) can be calculated as:

$$V_2''(t) = -I_{\max}R_{da}(1 - e^{-(t-t_d)/\tau_{2n}})u(t - t_d) \tag{5.20}$$

where,

$$\tau_{2n} = \tau_2 + t_{a2},$$

and,

$$t_{a2} = C_{1a}R_{da} + (C_{eqv} + C_{req-2})(R_{da} + R_{1a})$$

Finally, the coupling waveform is given by:

$$\begin{aligned} V_2(t) &= V_2'(t) + V_2''(t) \\ V_2(t) &= I_{\max} R_{da}(1 - e^{-t/\tau_{1n}}) - I_{\max} R_{da}(1 - e^{-(t-t_d)/\tau_{2n}})u(t - t_d) \end{aligned} \tag{5.21}$$

5.6 Noise Voltage Formulation

In output voltage formulation, the aggressor waveform at coupling location is entered to the transfer function to calculate victim noise as shown in Fig. 5.9.

Referring to Fig. 5.9, we have,

$$\frac{1}{Z_1} = \frac{1}{R_d} + sC_{1v} \tag{5.22}$$

$$\frac{1}{Z_2} = \frac{1}{R_{2v} + 1/sC_{lv}} + sC_{2v} + \frac{1}{Z_1 + R_{1v}} \tag{5.23}$$

$$V_5(s) = \frac{Z_2}{Z_2 + 1/sC_c} V_2(s) \tag{5.24}$$

$$V_{out}(s) = \frac{1}{sC_{lv}R_{2v} + 1} V_5(s) \tag{5.25}$$

After inserting (5.24) in (5.25), we hire dominant pole approximation method to reduce complexity of the transfer function [12, 13] and obtain:

$$\frac{V_{out}(s)}{V_2(s)} = \frac{s\tau_x}{s\tau_v + 1} \tag{5.26}$$

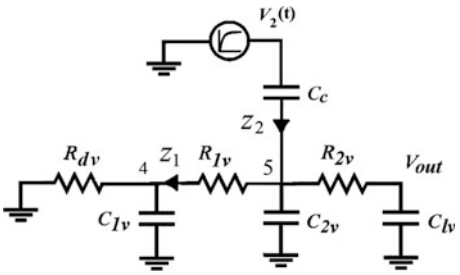

Fig. 5.9 Output voltage calculation after coupling node waveform

where,

$$\tau_v = R_d(C_c + C_{1v} + C_{2v} + C_{lv}) + R_{1v}(C_c + C_{2v} + C_{lv}) + R_{2v}C_{lv}$$

and,

$$\tau_x = (R_d + R_{1v})C_c$$

Finally coupling node waveform in (5.21) can be inserted in (5.26) to obtain the V_{out} expression:

$$V_{out}(s) = \frac{s\tau_x I_{\max} R_{da}}{(s\tau_v + 1)}\left(\frac{1 - e^{-st_d}}{s} - \frac{1}{s + 1/\tau_{1n}} + \frac{e^{-st_d}}{s + 1/\tau_{2n}}\right) \tag{5.27}$$

In time domain, the victim output noise waveform would be:

$$V_{out}(t) = I_{\max} R_{da}\tau_x\left[\frac{e^{-t/\tau_{1n}} - e^{-t/\tau_v}}{\tau_{1n} - \tau_v} + \frac{e^{-(t-t_d)/\tau_v} - e^{-(t-t_d)/\tau_{2n}}}{\tau_{2n} - \tau_v} * u(t - t_d)\right] \tag{5.28}$$

Noise peak has been traditionally used as a metric to determine if the noise is at an acceptable level. In order to calculate the noise peak, the derivative of (5.28) should be set zero to find the time instant where the maximum occurs. However, the above equation contains three exponential terms and hence it becomes difficult to find a closed-form expression for amplitude. On the other hand, one can obtain a function $f(t)$ which can be used in Newton's iteration method to solve for the t_{peak} where noise peak V_{peak} occurs:

$$f(t) = \frac{dV_{out}}{dt} = \frac{I_{\max} R_{da}\tau_x}{\tau_v}\left[\frac{\tau_{1n}e^{-t/\tau_v} - \tau_v e^{-t/\tau_{1n}}}{\tau_{1n}^2 - \tau_v\tau_{1n}} + \frac{e^{-(t-t_d)/\tau_v} - e^{-(t-t_d)/\tau_{2n}}}{\tau_{2n}^2 - \tau_v\tau_{2n}} * u(t - t_d)\right] = 0 \tag{5.29}$$

Then, t_{peak} can be found using:

$$t_{peak_{k+1}} = t_{peak_k} - f(t_{peak_k})/f'(t_{peak_k}) \tag{5.30}$$

This method converges very rapidly after little iteration. The noise peak voltage V_{peak} is found after inserting t_{peak} in (5.28).

A similar victim noise expression can also be obtained for the case that a negative particle strike occurs at the output of aggressor driver. In this case, since both driver inputs are at logic 0, the holding resistances of PMOS transistors should be utilized in noise formulation.

5.7 Summary of the Model

The following steps summarize for the proposed model:

1. Determine the particle LET based on the environment, obtain current pulses from device simulations. Find the rise and the fall time constants τ_1, and τ_2, the delay time t_d, and current magnitude I_{max} of the current source.
2. Calculate the equivalent capacitance value $C_{eq\text{-}a}$ for each passive aggressor that is coupled to victim line. This capacitor is then placed in parallel at victim coupling node.
3. Reduce any aggressor tree branches using an equivalent branching capacitance $C_{eq\text{-}br}$ at branching point.
4. Repeat the same procedure in step (2) for the victim line, and find an equivalent capacitance value $C_{eq\text{-}v}$. This capacitor updates the value of C_{2a} at the active aggressor coupling point. The formula for $C_{eq\text{-}v}$ is slight variation of (5.8).
5. Calculate the new time constants τ_{1n} and τ_{2n} at aggressor coupling point.
6. Calculate other time constants τ_x and τ_v.
7. Using the iteration formula, find the time that noise peak occurs, which is t_{peak}.
8. Finally obtain V_{peak} after inserting t_{peak} in (5.28) and decide whether the noise is important or not.

5.8 Validation of the Model

The model has been tested using over 1000 randomly generated cases to simulate real-time cases in 65 nm technology. The SE crosstalk model has been coded in C++ environment and results are verified by comparing to HSPICE outputs. While the proposed model used a 4-π template, HSPICE simulation utilized a 20-π representation to model the distributed behavior. In Spice modeling, the coupling capacitances were also distributed.

Two parallel interconnects on intermediate layer that are driven by 2X size inverters have been assumed. It was also assumed that the loads at the end of wires are identically sized inverters. Various interconnect spacing, length and widths were examined. Interconnect lengths were varied from 200 μm up to 2 mm with coupling portion changed. Some of these nets also included some tree branches. The parameter values for these test circuits have been derived using interconnect model

Table 5.1 Experimental results obtained for the first 25 cases

Case #	Q_{dep} (fF)	R_{agg} (Ω)	R_{vic} (Ω)	C_{agg} (fF)	C_{vic} (fF)	C_c (fF)	Noise (mV) HSPICE	Noise (mV) model	|Error %|
1	100	400	500	29	37	50	0.443	0.471	6.32
2	150	350	450	31	40	45	0.670	0.708	5.67
3	75	380	490	30	41	45	0.374	0.407	8.82
4	94	210	225	12	14	27	0.483	0.520	7.66
5	65	225	260	14	17	30	0.368	0.375	1.90
6	90	900	900	64	64	112	0.647	0.667	3.09
7	125	364	357	21	20	48	0.740	0.760	2.70
8	50	350	350	23	23	42	0.380	0.329	13.42
9	120	452	450	27	27	57	0.734	0.746	1.63
10	46	184	232	13	14	23	0.350	0.376	7.43
11	95	356	451	22	27	44	0.533	0.576	8.07
12	39	310	359	30	32	40	0.355	0.361	1.69
13	90	420	455	31	39	52	0.447	0.412	7.83
14	85	290	320	19	23	37	0.410	0.413	0.73
15	83	445	482	23	28	55	0.426	0.446	4.69
16	70	900	900	54	54	113	0.609	0.616	1.15
17	135	421	402	25	24	51	0.859	0.872	1.51
18	90	352	450	25	30	45	0.506	0.520	2.77
19	85	347	413	24	31	43	0.490	0.520	6.12
20	145	690	670	49	43	83	0.792	0.821	3.66
21	25	525	560	35	41	66	0.203	0.180	11.33
22	35	125	130	11	14	16	0.140	0.155	10.71
23	89	190	210	13	15	23	0.492	0.509	3.46
24	150	460	475	31	40	55	0.710	0.755	6.34
25	65	592	592	37	37	73	0.489	0.508	3.89
Average % error for first 30 cases									**5.3 %**

given in [14]. The simulated deposited charges, Q_{dep}, were selected in the range 20–150 fC.

Table 5.1 shows the SE Crosstalk noise calculation results for the first 25 cases. In this table, R_{agg}/C_{agg} and R_{vic}/C_{vic} denote aggressor and victim line resistance/capacitance, respectively. Finally, C_c indicates the coupling capacitance values taken for each case.

For 25 test cases considered, the proposed model has an average error of 5.3 % when compared to HSPICE. For all cases shown, the percent error stays less than 15 %.

Figure 5.10 below shows the histogram of SE crosstalk noise calculation error for 1000 different aggressor-victim pair. For most of the cases, the percent error stays less than 15 %.

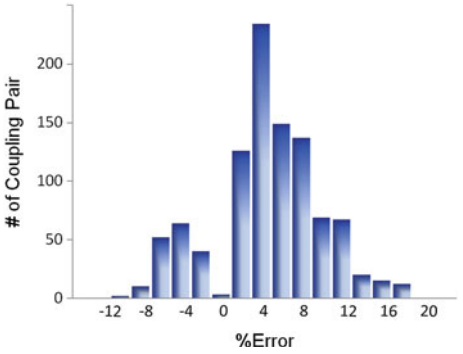

Fig. 5.10 Histogram of SECN noise prediction error

Table 5.2 The percentage of nets that fall into the error ranges

Error range	V_{peak} (%)
Within ±5 %	61.70
Within ±10 %	88.65
Within ±15 %	97.33
Avg. Error	6.16

In Table 5.2, the percentage of nets that fall into the given error ranges has been given. For example, about 89 % of nets have errors less than 10 % when predicting the noise peak voltage. On the other hand, around 97 % of all nets have errors less than 15 %.

According to calculation results, for most of the test cases, the proposed model tends to slightly overestimate the SE crosstalk noise. This might be due to the use of medium value of the holding resistance which might be still overestimating. Another reason for the error might be due the use of dominant pole approximation since the reduction causes some information loss on the transfer function.

For all test cases considered, the proposed model has an average error of 6.16 % when compared to HSPICE. The CPU time for these test circuits ranges from 0.025 to 0.30 ms on a 3.0 GHz Pentium IV machine which suggests that the model calculation is at least a 1000X faster than HSPICE.

5.9 Summary

This chapter introduced a fast SE crosstalk noise estimation method for use in design automation tools. Normally, SPICE simulators can be used to estimate crosstalk effects in signal lines. However, due to density of interconnect lines, these simulations are time-inefficient.

This method uses an accurate 4-π model for interconnect and correctly models the loading effect of neighboring lines and net tree branches noting the resistive

shielding effect. The dominant pole approximation was used in moderation which resulted in increased accuracy of model.

A logical extension of this work would incorporate non-linear characteristics of drivers in the model especially for large charge injection levels.

For deposited charge levels considered in terrestrial environment, the derived SE crosstalk noise expressions show very good results in comparison to HSPICE results.

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Chapter 6
Modeling of Single Event Coupling Delay and Speedup Effects

6.1 Single Event Coupling Delay Prediction

It was previously shown that Single Event Crosstalk effects can introduce circuit delays that can exceed normal signal switching induced delay after a certain deposited charge. During layout optimization, the wires might be spaced out enough to prevent timing violations caused by normal aggressor switching. The protection taken, however, may not be sufficient, as delay caused by SE crosstalk effect can be larger.

SPICE simulators often used to estimate delay effects in signal lines. While results are accurate, large density of interconnect lines prohibits the use of these simulations. A time-efficient and yet accurate crosstalk delay estimation alternative is often needed to ensure acceptable signal integrity in a limited design cycle time so that one can quickly verify if a given wire routing solution will not lead to timing failures caused by the coupled noise.

Circuit designers are usually interested in worst case delays. This section focuses on prediction of worst-case SECD that can be induced on a victim line due to an SET on an aggressor line.

The amount of delay induced on the victim line due to coupling is strongly dependent on how the SET waveform on the aggressor line is aligned with respect to the victim waveform. However, one is also interested in obtaining worst delays so large number of nets can be screened quickly before any mitigation is needed.

For worst-case delay calculation method discussed here, the circuit is first linearized by replacing the drivers by its holding resistances. Once the circuit is linearized, the linear superposition principle can be applied [1]. The voltage waveform on the victim line is first obtained assuming there is no SET present on the aggressor line. Then, the victim net is assumed to be quiet and the SE crosstalk noise (SECN) induced on victim net (due to an SET on aggressor line) is calculated. Finally, the SECN waveform is aligned with the noiseless victim waveform to obtain a composite waveform for worst-case delay calculation (Fig. 6.1).

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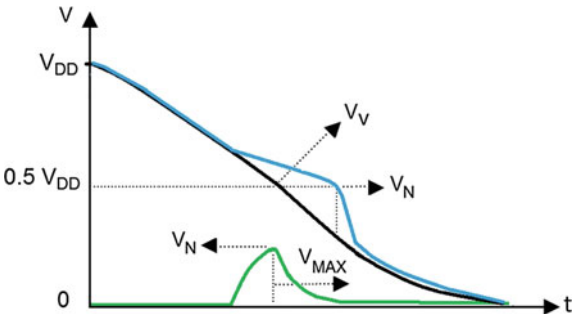

Fig. 6.1 Worst-case SECD calculation model

When calculating for the worst-case delay, we assume a noiseless monotonic victim waveform V_V that starts to fall from V_{DD} with a slope of S_V and reaches to zero. We also consider an SECN signal V_N of arbitrary shape with a maximum height of $V_{\max}$ and whose initial and final values are zero, as shown in Fig. 6.1.

Let us assume the worst-case delay occurs at time t_{wcd}. Then at t_{wcd}, the value of composite waveform obtained by superposing the noise-free victim waveform and the SECN must be equal to $V_{DD}/2$:

$$V_{DD} - t_{wcd}|S_V| + V_N(t_{wcd}) = V_{DD}/2 \tag{6.1}$$

Since t_{wcd} corresponds to the largest delay possible, the largest value of V_N should correspond to $V_{\max}$. Then, we obtain:

$$t_{wcd} = \frac{V_{DD}/2 + V_{\max}}{|S_V|} \tag{6.2}$$

In other words, the worst-case victim line delay, t_{wcd} occurs when the noiseless victim waveform $(V_{DD} - t_{wcd}|S_V|)$ reaches $(V_{DD}/2) - V_{\max}$ [1]. This also agrees with the results of original work by Dartu and Pileggi [2].

6.1.1 Calculating Maximum Value of Crosstalk Noise V_M

In order to calculate the maximum value of crosstalk noise needed for T_{WCD} calculation, the SE crosstalk model discussed in Chap. 5 has been adopted. In this model [3], the loading effects of non-switching (passive) aggressors and aggressor tree branches are correctly modeled using equivalent capacitances noting the resistive shielding effect.

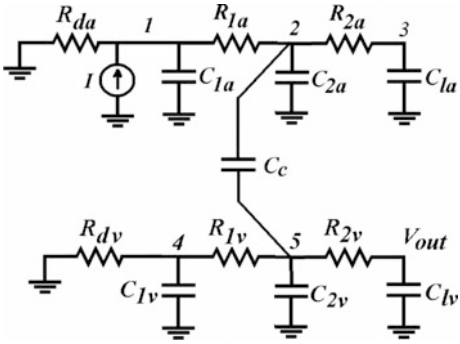

Fig. 6.2 The 4-π template circuit used in calculating the maximum value of SECN

The SE crosstalk model uses a 4-π interconnect model in which both the victim and aggressor nets are modeled using the 2-π circuits. Figure 6.2 shows the 4-π template used in noise calculation (copied from Chap. 5 for convenience). The RC parameter values are calculated based on technology and the geometric information.

In the model, the victim driver is represented approximately by NMOS transistor holding resistance R_{dv}. As for the aggressor driver, the medium value of the holding resistance (R_{da}) has been used as an approximation.

After some formulations (details are omitted, see Chap. 5 for details), SE crosstalk noise waveform is expressed as:

$$V_{out}(t) = I_{\max} R_{da} \tau_x \left[\frac{e^{-t/\tau_{1n}} - e^{-t/\tau_v}}{\tau_{1n} - \tau_v} + \frac{e^{-(t-t_d)/\tau_v} - e^{-(t-t_d)/\tau_{2n}}}{\tau_{2n} - \tau_v} * u(t - t_d) \right] \quad (6.3)$$

where,

τ_1 and τ_2 are the rise and the fall time constants of ion-induced current pulse

I_{max} is the magnitude of the ion-induced current pulse

t_d is the delay time that controls the duration of the plateau effect

$$\tau_{1n} = \tau_1 + t_{a1} \quad \text{and} \quad \tau_{2n} = \tau_2 + t_{a2}$$

τ_1 and τ_2 are the rise and the fall time constants of ion-induced current pulse

$$\tau_x = (R_d + R_{1v}) C_c \text{ and}$$
$$\tau_v = R_d(C_c + C_{1v} + C_{2v} + C_{lv}) + R_{1v}(C_c + C_{2v} + C_{lv}) + R_{2v} C_{lv}$$

In order to calculate the noise peak (V_{max}) needed for worst-case delay calculation, the derivative of (6.3) should be set zero to find the time instant where the maximum occurs. Since above equation contains three exponential terms, an iteration method such as Newton's method can be hired. For this, one can obtain a

function $f(t)$ which can be used in Newton's iteration method to solve for the t_{max} where noise peak V_{max} occurs:

$$f(t) = \frac{dV_{out}}{dt} = \frac{I_{\max} R_{da} \tau_x}{\tau_v} \left[\frac{\tau_{1n} e^{-t/\tau_v} - \tau_v e^{-t/\tau_{1n}}}{\tau_{1n}^2 - \tau_v \tau_{1n}} + \frac{e^{-(t-t_d)/\tau_v} - e^{-(t-t_d)/\tau_{2n}}}{\tau_{2n}^2 - \tau_v \tau_{2n}} * u(t-t_d) \right] = 0 \tag{6.4}$$

The time the maximum noise occurs, t_{peak} can be found using:

$$t_{peak_{k+1}} = t_{peak_k} - f(t_{peak_k}) / f'(t_{peak_k}) \tag{6.5}$$

This method converges very rapidly after little iteration. The noise peak voltage V_{max} is found after inserting t_{peak} in (6.3).

6.1.2 Summary of the Worst Case SECD Calculation Model

The following steps summarize for the proposed worst-case delay estimation model [4]:

1. Determine the victim-end waveform assuming there is no particle hit that occurs on the aggressor driver and calculate the victim waveform slope.
2. Calculate the maximum value of crosstalk noise. First, determine the particle LET based on the environment, then obtain current pulses from device simulations. Find the rise and the fall time constants τ_1, and τ_2, the delay time t_d, and current magnitude I_{max} of the current source.
3. Calculate the equivalent capacitance value for each passive aggressor that is coupled to victim line. This capacitor is then placed in parallel at victim coupling node. Reduce any aggressor tree branches and obtain an equivalent branching capacitance at branching point.
4. Repeat the same procedure in step (3) for the victim line, and find an equivalent capacitance value.
5. Calculate the time constants τ_{1n} and τ_{2n} at aggressor coupling point, and find constants τ_x and τ_v.
6. Using the iteration formula (6.4), find the time that noise maximum occurs, which is t_{max}. Obtain the maximum value of SE crosstalk noise V_{max} after inserting t_{peak} in (6.3).
7. Finally, determine the worst-case SE crosstalk delay using (6.2).

6.1.3 Validation of the Worst Case SECD Calculation Model

The proposed model has been tested using over 1000 randomly generated cases to simulate real-time cases in 65 nm technology. The SECD model has been coded in C++ environment and results are verified by comparing to HSPICE simulation outputs. While the proposed model used a 4-π model, HSPICE simulation utilized a 20-π representation with distributed coupling capacitors to approximate the distributed behavior.

Two intermediate level parallel interconnects are selected which are driven by 2X size inverters. It was also assumed that the loads at the end of wires are identically sized inverters. Various interconnect spacing, length and widths were examined. Interconnect lengths were varied from 200 μm up to 2 mm with coupling portion changed. Some of these nets also included some tree branches. The parameter values for these test circuits have been derived using interconnect parameters given in [5]. The simulated deposited charges, Q_{dep}, were selected in the range 20–150 fC.

Figure 6.3 shows the histogram of worst-case SECD calculation error for 1000 different aggressor-victim pair. For almost all of the cases, the percent error remains less than 15 %.

Table 6.1 shows the percentage of nets that fall into the given error ranges has been given. For example, about 84 % of nets have errors less than 10 % when predicting the worst-case SE crosstalk delay. On the other hand, around 97 % of all nets have errors less than 15 %.

According to calculation results, for most of the test cases, the proposed model tends to slightly overestimate worst-case SECD. This might be due to the use of medium value for the aggressor holding resistance. Another reason for the error might be due the loss caused by dominant pole approximation.

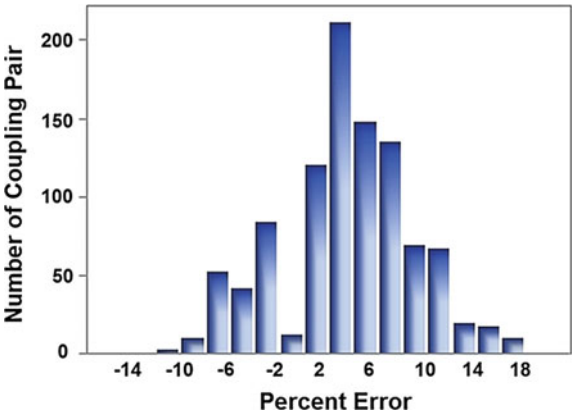

Fig. 6.3 Histogram of worst-case SECD (t_{wcd}) error

Table 6.1 The percentage of nets that fall into the error ranges

Error range	% of nets
Within ±5 %	57.1
Within ±10 %	83.5
Within ±15 %	96.8
Avg. Error	6.32

For the test cases considered, the proposed model has an average error of 6.32 % when compared to HSPICE. The CPU time for these test circuits ranges from 0.038 to 0.28 ms on a Pentium Dual Core CPU (2.27 GHz) processor which suggests that the model calculation is at least a 1000 times faster than HSPICE.

6.1.4 Section Summary

This section introduced a worst-case SECD estimation method for use in design automation tools. The proposed method uses an accurate 4-π model for interconnect and correctly models the loading effect of neighboring lines and net tree branches noting the resistive shielding effect.

For the deposited charge levels considered in terrestrial environment, the derived worst-case SECD model shows very good results in comparison to HSPICE results. Results show that average error for noise peak is about 6.3 % while allowing for very fast analysis compared to HSPICE.

6.2 Single Event Crosstalk Speedup

This section introduces the signal speedup effects caused by SE crosstalk. After studying the effect of technology scaling on SE speedup effects, it proposes a best-case delay estimation methodology for use in design automation tools.

The crosstalk speed-up effects occur when an aggressor switches in the same direction to the victim line but lot faster [6]. Maximum victim line signal speed-up occurs when aggressor finishes its transition before victim reaches to 50 % of its maximum value.

In the case of an SE Crosstalk Speed-up (SECS), a positive SET on an aggressor line couples to the victim line when victim lines is having a rising transition [7]. Similarly, a negative SET on an aggressor can cause a signal speed-up during victim line's falling phase of transition. In Fig. 6.4, an SE particle hit at the drain of OFF PMOS transistor of the inverter driver causes the output to go towards logic 1 (or V_{DD}) for some pulse duration. The SET created, in turn, spreads into the victim line via coupling capacitance and causes a speedup effect on the rising victim line waveform. As a result, victim line signal switches sooner than it would. This effect

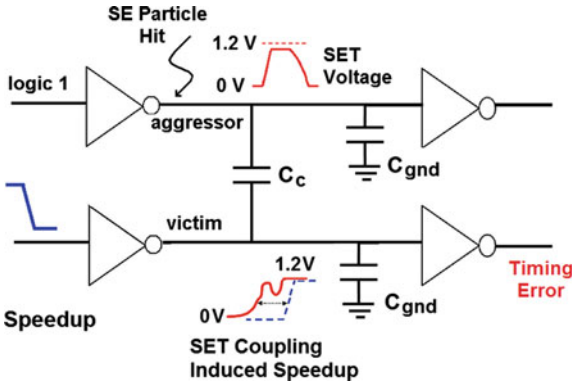

Fig. 6.4 SE crosstalk speedup (Lumped model is for demonstration only)

can be named as SE crosstalk speedup or SECS. The decrease in interconnect delay due to SET coupling can affect circuit performance as the speedup effects may later violate hold time requirements of logic storage circuits connected to these receivers.

In order to study the effect of technology scaling on SECS, two parallel interconnects that are on the intermediate layer has been considered. The wire length chosen was 1000 μm. In simulations, a 10-π model with distributed coupling capacitances was used for every 100 μm of wire to represent the RC distributed behavior (see Fig. 6.5). It is also assumed that aggressor and victim driver sizes are two times the minimum size and the loads at the end of the wires are minimum sized identical inverters.

The wire dimensions taken were as follows [5]: For 90 nm technology, the width (W), spacing (S) is 0.2 μm, and wire thickness T is 0.45 μm. For 65 nm technology, the dimensions were W = S = 0.14 μm, and T = 0.35 μm. Finally, for 45 nm technology, W = S = 0.1 μm, and T = 0.24 μm.

In order to analyze the SE induced crosstalk speedup, a falling pulse waveform with a 100 ps fall time has been applied to victim driver while aggressor driver was kept at V_{DD} as shown in Fig. 6.5. Normally, aggressor driver output would be at

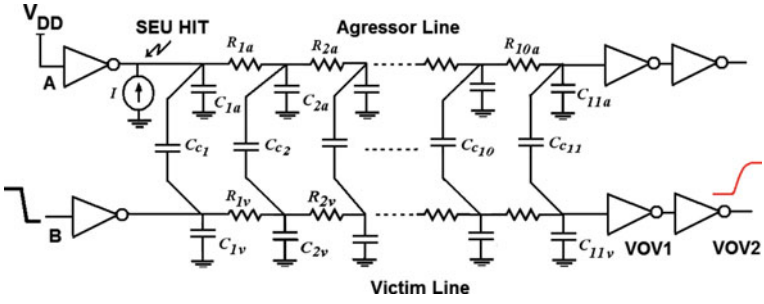

Fig. 6.5 Setup used for SE coupling induced speedup

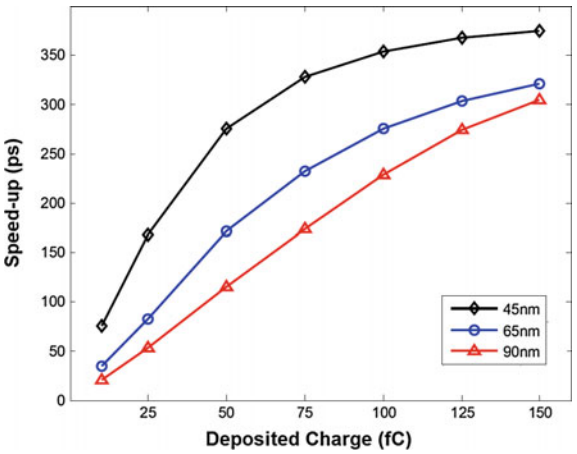

Fig. 6.6 SE crosstalk speedup versus technology

"logic low" but it would be taken to "logic high" if there is a sufficient SE hit charge on output node of the driver.

An SE hit is simulated at the output of the aggressor driver using a double exponential current pulse in our analysis here. The hit charge was increased up to 150 fC for three technologies considered. At the end of the victim line, two inverters have been used to filter out the distortion on victim line and the signal delay is measured at V_{OV2}.

Figure 6.6 shows the effect of various deposited charges on SECS for 90, 65, and 45 nm technologies. For newer technologies, the same hit charge can cause larger signal speedup effect. As an example, a 100 fC of deposited charge causes a signal speedup of 229 ps in 90 nm technology while the same charge can induce 353.5 ps speedup in 45 nm. The effect of SECS increases as device sizes further scale down, therefore this effect will become even more important in smaller technologies.

6.3 Best-Case SE Crosstalk Delay Calculation

The amount of speedup induced on the victim line due to coupling is strongly dependent on how the SET waveform on the aggressor line is aligned with respect to the victim waveform. However, one is also interested in obtaining best-case delays so large number of nets can be screened quickly before any mitigation is needed.

In calculating the best-case delay, the circuit can first be linearized by replacing drivers by its holding resistances. Once the circuit is linearized, the linear superposition principle can be applied as in the case of worst case crosstalk delay estimation [1, 2]. The voltage waveform on the victim line is first obtained assuming there is no SET present on the aggressor line. Then, the victim net is assumed to be quiet and the SE crosstalk noise (SECN) induced on victim net

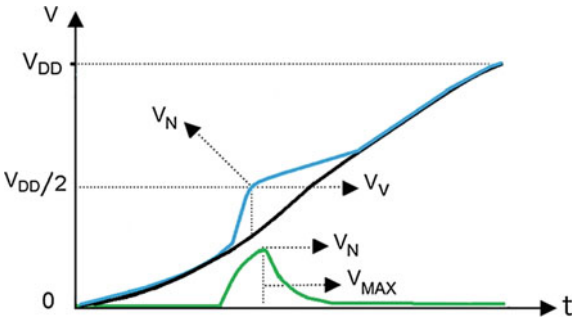

Fig. 6.7 Best-case delay estimation model

(due to an SET on aggressor line) is calculated (green waveform). Finally, the SECN waveform is aligned with the noiseless victim waveform (shown with blue) to obtain a composite waveform for best-case delay calculation (Fig. 6.7).

When calculating for the best-case delay, we assume a noiseless monotonic victim waveform V_V that starts to rise from 0 with a slope of S_V and reaches to V_{DD}. We also consider an SECN signal V_N of arbitrary shape with a maximum height of V_{max} and whose initial and final values are zero, as shown in Fig. 6.7.

Let us assume the best-case delay occurs at time t_{bcd}. Then at t_{bcd}, the value of composite waveform obtained by superposing the noise-free victim waveform and the SECN must be equal to $V_{DD}/2$:

$$t_{bcd}S_V + V_N(t_{bcd}) = V_{DD}/2 \tag{6.6}$$

Since t_{bcd} corresponds to the largest speedup possible, the largest value of V_N should correspond to V_{max}. Then, we obtain:

$$t_{bcd} = \frac{V_{DD}/2 - V_{max}}{S_V} \tag{6.7}$$

In other words, best-case victim line delay t_{bcd} occurs when the noiseless victim waveform $t_{bcd} \cdot S_V$ reaches $V_{DD}/2 - V_{max}$.

6.3.1 Summary of the Proposed SECS Prediction

The following steps summarize for the proposed best-case delay estimation model:

1. Determine the victim-end waveform assuming there is no particle hit that occurs on the aggressor driver and calculate the victim waveform slope.
2. Calculate the maximum value of SECN noise after inserting t_{peak} from (6.5) into (6.3).

(a) For this, determine particle LET, and obtain current pulses from device simulations. Find the rise and fall time constants τ_1, and τ_2, delay time t_d, and current magnitude I_{max} of the current source.
(b) Determine the holding resistances of aggressor and victim drivers using pre-characterization.
(c) Calculate an equivalent capacitance $C_{eq\text{-}a}$ for each passive aggressor coupled to victim line. This capacitor is then placed in parallel at victim coupling node. Reduce any aggressor tree branches if needed.
(d) Repeat the same procedure in step 2(c) for the victim line, and find an equivalent capacitance value $C_{eq\text{-}v}$. This capacitor updates the value of C_{2a} at the active aggressor coupling point (see Fig. 6.2).
(e) Calculate the new time constants τ_{1n} and τ_{2n} at aggressor coupling point, and find constants τ_x and τ_v.
(f) Using the iteration formula (6.4), find the time that noise maximum occurs, which is t_{max}. Then, obtain the maximum value of SE crosstalk noise V_{max} after inserting t_{peak} in (6.3).

3. Finally, determine the best-case SE crosstalk delay amount using (6.7).

6.3.2 Validation of the Proposed Model

The proposed model has been validated using over 1000 randomly generated cases to simulate real-time cases in 45 nm technology. The SECS model has been coded in C++ environment and results are verified by comparing to HSPICE simulation outputs. While the proposed model used a 4-π model, HSPICE simulation utilized a 20-π representation with distributed coupling capacitors to approximate the distributed behavior.

Two parallel interconnects on intermediate layer has been taken that are driven by 2X size inverters. It was also assumed that the loads at the end of wires are identically sized inverters. Various interconnect spacing, length and widths were examined. Interconnect lengths were varied from 200 μm up to 2 mm with coupling portion changed. Some of these nets also included some tree branches. The parameter values for these test circuits have been derived using interconnect parameters given in [5]. The simulated deposited charges, Q_{dep}, were selected in the range 10–150 fC.

Figure 6.8 shows the histogram of best-case delay calculation error for 1000 different aggressor-victim pair. For most cases, the percent error remains less than 15 %.

In Table 6.2, the percentage of nets that fall into the given error ranges has been given. For example, about 72 % of nets have errors less than 10 % when predicting the best-case SE crosstalk delay. On the other hand, around 93 % of all nets have

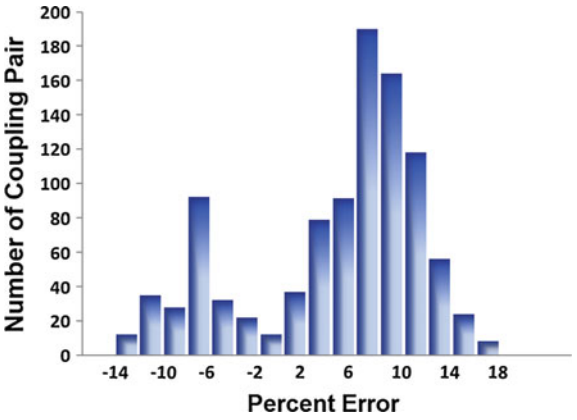

Fig. 6.8 Histogram of best-case delay (t_{bcd}) error

Table 6.2 The percentage of nets that fall into the error ranges

Error range	% of nets
Within ±5 %	3.4
Within ±10 %	71.8
Within ±15 %	93.2
Avg. Error	8.42

errors less than 15 %. For the 1000 test cases considered, the proposed model has an average error of 8.42 % when compared to HSPICE.

According to calculation results, the proposed model tends to slightly overestimate best-case delay for most cases. This might be due to the use of medium value for the aggressor holding resistance. Another reason for the error might be due the loss caused by dominant pole approximation which was used during crosstalk noise formulation.

The effect of using different holding resistances on best-case SECD calculation has also been studied for the first 100 cases. When using the largest value of holding resistance, the average error has increased to 13.8 %. The speedup effects were mostly overestimated when using the largest value. On the other hand, the average error for the medium value of holding resistance was only 8.62 % for the cases considered. The smallest value of holding resistance, on the other hand, increased the average error value to 11.4 %. The use of the smallest value of holding resistance (output voltage taken at 0) underestimated the speed-up effect for most cases.

In summary, the proposed model has an average error of 8.42 % when compared to HSPICE. The CPU time for these test circuits ranges from 0.042 to 0.27 ms on a Pentium Dual Core CPU (2.27 GHz) processor which suggests that the model calculation is at least a 1000X faster than HSPICE.

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Chapter 7
Single Event Upset Hardening of Interconnects

7.1 Introduction

With increased coupling effects among interconnects, SE Transients can contaminate electronically unrelated circuit paths which can in turn increase the "Single Event Susceptibility" of CMOS circuits to Single Event Transients.

As mentioned in Chap. 4, the coupling effects produced by SE hits can violate noise margins of gates connected to the affected line and may result in logic errors. Serious effects may occur if the affected line is somewhat important such as a clock line [1]. In addition, triple modular redundancy (TMR) circuits used to eliminate SE errors on CL are also susceptible to crosstalk at the inputs of voters [2]. This is possible because interconnects between functional units and voters tend to be long and sensitive to crosstalk.

Many design techniques have been proposed to mitigate Single Event Upset (SEU) problems in combinational logic (CL). Spatial redundancy techniques such as Triple Modular Redundancy (TMR) method triplicate the CL that is to be protected and uses a voting circuit to filter out the transient [3]. In driver sizing technique, the gate which drives a set of gates is resized for hardening [4, 5]. The sizing of the hit gate's transistors eliminates lower energy radiation from producing transients, because of the raised critical charge for the gate.

Temporal methods sample the data with different delays and produce the output to a voting circuit [3]. The voting circuit outputs the majority of the inputs to filter out the glitch. Other techniques use different circuit layouts at the gate and transistor levels to reduce the chance of a SE to become a transient [6]. Nevertheless, even these designs leave a vulnerable spot to other SE effects: The interconnect.

In general, standard measures to immunize a circuit against crosstalk such as wire sizing, spacing and driver sizing should be also effective for SE crosstalk noise and delay mitigation. This chapter investigates applicability of existing crosstalk reduction techniques on hardening of SE Crosstalk noise and delay.

S. Sayil, *Soft Error Mechanisms, Modeling and Mitigation*,
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7.2 SE Crosstalk Mitigation Techniques

The techniques considered here include aggressor and victim driver sizing, wire spacing and wire sizing techniques. The applicability of shielding technique is also discussed in this section.

7.2.1 Aggressor Driver Sizing

In mitigating the switching induced crosstalk effects, aggressor and victim driver sizing are among the popular methods used for mitigation. In case of an aggressor driver, if it is sized down, its effective transconductance decreases, and cannot transition as fast due to its large resistance. As a result, noise amount induced on victim line would be less [7].

Figure 7.1 shows the effect of decreasing aggressor driver size (inverter) on switching induced crosstalk noise (normal crosstalk) for an intermediate level wire in 65 nm technology.

As aggressor driver is sized down, the amount of induced crosstalk noise on victim decreases. This is valid for normal signal switching induced crosstalk, and the same may not hold true for SE crosstalk.

However, sizing down an aggressor driver reduces the critical charge needed for an SE hit to produce transients. Hence, it causes increasing SE crosstalk effects in CL logic. For reducing SE effects, the aggressor driver transistors should be sized up instead to reduce SE Transients at aggressor gate output. Larger drive strengths of NMOS and PMOS quickly dissipates the collected charge, reduces the vulnerability to Single Event particles. This also reduces the induced Single Event crosstalk.

Figure 7.2 shows how increasing the transistor size in aggressor driver can help mitigate SE induced crosstalk.

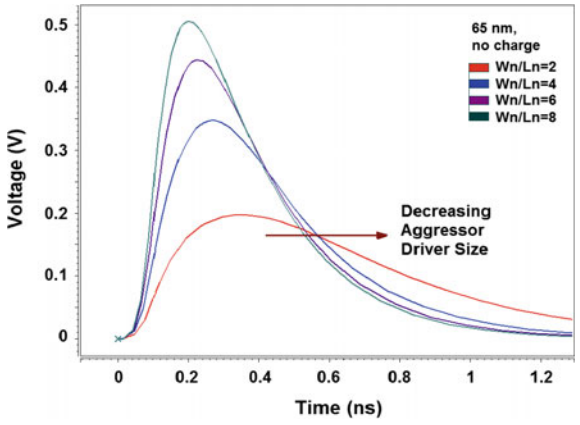

Fig. 7.1 The effect of decreasing aggressor driver size normal crosstalk

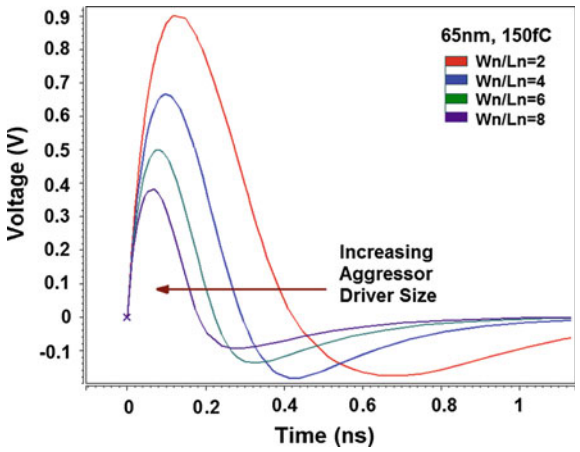

Fig. 7.2 The effect of increasing aggressor driver size on SE crosstalk

By comparing Figs. 7.1 and 7.2, we can conclude that sizing up of an aggressor driver causes reduction in SE induced crosstalk, but leads to large increases in normal aggressor switching induced crosstalk. Since aggressor sizing has different effects for normal and SE induced crosstalk, aggressor sizing cannot be used to control SE crosstalk.

7.2.2 Victim Driver Sizing

Victim driver sizing methodology is an effective means to reduce SE crosstalk. It reduces both SE crosstalk [7] and normal switching induced crosstalk [8]. After sizing up the victim driver, the driver holding resistance reduces while the output capacitance increases. The increased victim output capacitance contributes to stability of the victim line. In the case of a crosstalk glitch, the increased drive current (of victim driver) due to reduced holding resistance helps mitigate the SE crosstalk noise faster.

Figure 7.3 shows the effect of victim driver sizing on SE crosstalk noise amplitude for 130, 90 and 65 nm technologies for a deposited charge level of 150 fC. When victim driver size doubled, the crosstalk noise amplitude reduces by as large as 36 %.

In conventional crosstalk analysis, among two neighboring wires that are coupled, the signal line which is switching more often than the other is usually taken as the aggressor line while the other net is taken as victim. However, one might want to also consider the situation where a victim net can also become an aggressor from the opposite standpoint.

When the driver of a victim is upsized for reducing noise at the victim net, the noise it will induce on the neighboring aggressor wire may increase due to stronger effect of victim driver. In other words, the noise induced on the aggressor line

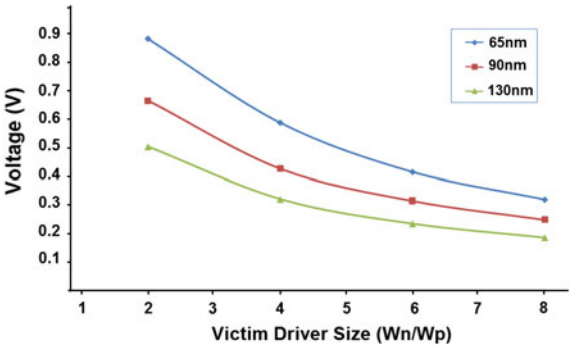

Fig. 7.3 The effect of victim driver sizing on SECN amplitude for 65, 90 and 130 nm technologies

should be checked against receiver threshold to make sure that noise peak value is below recommended threshold level.

In the optimization algorithm described here a 4-π template based noise model has been used for crosstalk estimation [9]. In the 4-π model, both victim and the aggressor net are modeled using the 2-π circuits and input waveforms are modeled using realistic exponential waveforms.

In the model shown in Fig. 7.4, the drivers are represented by linear resistors using the method described in [10]. Hence, effective resistances R_d and R_{th} model the victim and aggressor drivers respectively. Note also the fact that driver resistances are inversely proportional to transistor channel widths. Other RC parameters are calculated based on technology and the geometric information from Fig. 7.4a.

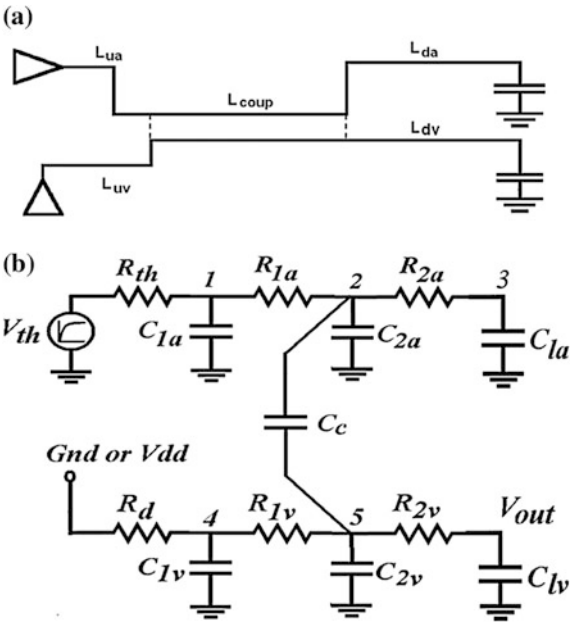

Fig. 7.4 The 4-π model for two coupled interconnects

Referring to Fig. 7.4b, both aggressor and victim lines can be divided into three parts: interconnect portion before coupling location (L_{ua}, L_{uv}), coupling location (L_{coup}) and interconnect portion after coupling location (L_{da}, L_{dv}). The coupling node (nodes 2 and 5) is set to be the center of the coupling portion, and is $L_{ua} + L_{coup}/2$ away from aggressor driver and $L_{uv} + L_{coup}/2$ away from the victim driver.

Based on above information and the technology parameters, we estimate the upstream and downstream resistance/capacitance values at nodes 2 and 5, respectively for each wire. Let's assume the upstream and downstream resistance/capacitance at node 2 be R_{1a}/C_{ua} and R_{2a}/C_{da} respectively (the total resistance/capacitance values of aggressor net for left and right segments). Similarly for victim net, the upstream and downstream resistance/capacitance at node 5 can be defined as R_{1v}/C_{uv} and R_{2v}/C_{dv} respectively. Then, for aggressor and the victim, we have:

$$C_{1a} = C_{ua}/2,\ C_{2a} = (C_{ua} + C_{da})/2 \text{ and, } C_{la} = C_{da}/2 + C_{lda}$$
$$C_{1v} = C_{uv}/2,\ C_{2v} = (C_{uv} + C_{dv})/2 \text{ and, } C_{lv} = C_{dv}/2 + C_{ldv}$$

Here, C_{lda} and C_{ldv} represent the load capacitances for aggressor and victim lines respectively.

Referring to Fig. 7.4, assuming an exponential source present at the input (with a rise time constant of t_r), the noise peak can be calculated (details can be found in [9]):

$$V_{peak} = \frac{\tau_x}{\tau_v}\left(\frac{t_r}{\tau_v}\right)^{t_r/(\tau_v - t_r)} \tag{7.1}$$

where,

$$\tau_x = (R_d + R_{1v})C_c$$
$$\tau_v = (R_d + R_{1v} + R_{2v})C_{lv} + (R_d + R_{1v})(C_{2v} + C_c) + R_d C_{1v} + R_{th}C_{1a} + (R_{th} + 2R_{1a})(C_{2a} + C_{eq-v}) + (R_{th} + 2R_{1a} + 2R_{2a})C_{la}$$

$C_{eq\text{-}v}$ is the equivalent victim capacitance seen at aggressor coupling node.

A similar formula can also be derived for the case that victim is switching and acting as an aggressor for the neighboring wire.

The maximum value of victim noise occurs when there is a strong aggressor driver (large driver) and a weak victim driver. This is usually the worst-case scenario for the noise received at victim receiver. In this case, when the same victim driver acts as aggressor, the amount of noise induced on the aggressor line will be relatively low due to large driver size of the previous aggressor. The larger drive strengths of aggressor transistors can quickly dissipate the coupled charge. Hence, an optimization may be possible using victim driver sizing. Assuming an aggressor-victim line pair, the optimization steps are summarized as follows:

1. Calculate noise peak voltages at both the victim and the aggressor lines using the formula (7.1) given above and calculate the "noise slack" for each wire. Here, "noise slack" is defined as the difference between "allowed and actual noise". Allowed noise is the threshold of the receiver gate and may be different for each wire.
2. In order to mitigate victim noise, change the victim driver size starting from "1X" up to "10X the previous victim driver size" and calculate the slack for the aggressor and the victim line. When the slack for victim line is positive, stop the sizing process, and check the aggressor slack. The first part of the optimization procedure is finished when both aggressor and victim slacks are positive.
3. If noise on the aggressor line is above allowed threshold (slack < 0), then victim driver size may have been increased more than needed. Repeat Step 2 by increasing victim driver slowly, i.e. in steps of 0.5X initial victim driver size or smaller. For most cases, it requires a few iterations for optimization to be done.
4. In the second part of the optimization procedure, the SE crosstalk noise at the victim is checked. (Here, it is assumed that the aggressor node have more diffusion area, making it a better collector than the victim driver node. So the strikes are modeled on the aggressor driver). After victim driver is sized for normal crosstalk (steps 1–3), if the noise slack for SE crosstalk is still negative, increase the victim driver size until "SE crosstalk noise slack" is positive. Check aggressor slack and adjust step size if necessary.

Closed form expressions for SE crosstalk noise have been developed assuming drivers can be represented by linear resistors.

Hashimoto and Onodera [11] suggested a driver-sizing algorithm where the goal is to minimize the sum of squared noise voltages at the aggressor and victim. When this optimization was applied to victim driver sizing method, it resulted in larger driver sizes than needed. This means larger power dissipation and IC temperature. In above algorithm, however, the sizing process ends once positive noise slacks for both victim and the aggressor lines have been obtained.

In verifying the above model, 100 cases are generated in 90 nm technology where various interconnect length, width; spacing and driver strengths are examined. In simulations the SE hit charge is taken as 200 fC.

In terms of SE crosstalk, the width of SE crosstalk pulse was observed to be usually smaller than the width of normal crosstalk pulse on the victim, so it quickly dissipated with victim driver sizing compared to normal crosstalk. In all 100 cases examined, it has been observed that after mitigating normal crosstalk, the single event crosstalk were below threshold. Hence, sizing up a victim driver can reduce both SE induced crosstalk and normal crosstalk effectively.

It is stated in [12] that in some cases, transistor sizing alone may not solve all noise violations. In this case, optimization step 3 fails. Although this was not observed, in such cases, spacing between wires may have to be increased along with transistor sizing to avoid this problem.

The effect of victim driver sizing on SE crosstalk delay has also been studied. Figure 7.5 shows the results obtained for three technologies considered. The results

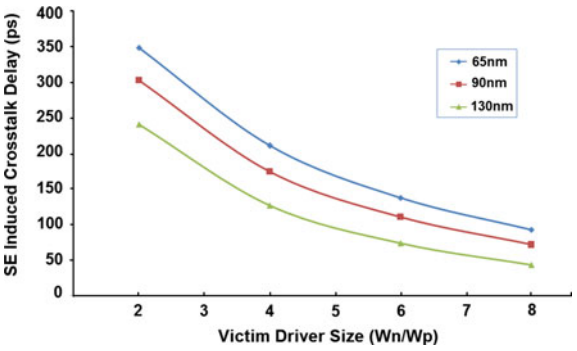

Fig. 7.5 The effect of victim driver sizing on SECD for 65, 90 and 130 nm technologies considered

show that SE crosstalk delay decrease with the increasing victim driver size. When victim driver size doubled, the SE crosstalk delay amount reduces by 38, 43 and 47 % for 65, 90 and 130 nm technologies, respectively.

7.2.3 Wire Sizing

As a wire width is changed, its resistance and capacitance values also vary. Larger wire size (width) means reduced wire resistance and increased ground capacitance all of which contribute to victim stability [13]. For example, if victim driver is holding the victim line at steady (i.e. GND), it will be more effective holding it and the noise induced will be less. Figure 7.6 shows the SECN for different wire widths examined. At W = 4 W_{min}, the crosstalk noise amplitude reduces by 56 %.

Although wire sizing method reduces crosstalk noise, it increases ground capacitance of the victim line. As for SE coupling delay mitigation, the wire sizing method does not offer any solution due to the fact that the increase in ground

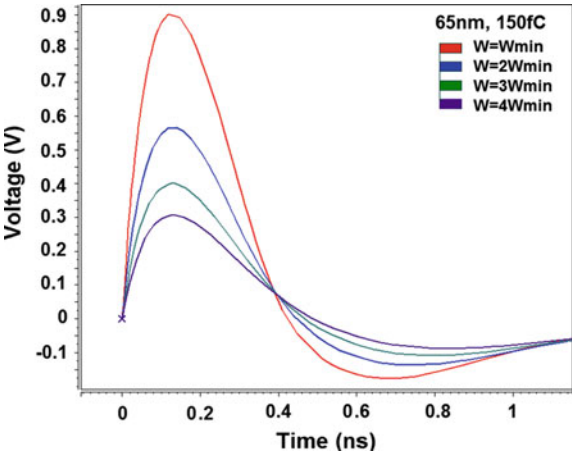

Fig. 7.6 The effect of wire sizing on SE crosstalk

capacitance dominates the overall circuit delay. As the wire width is increased, the SECD increases [14].

7.2.4 Wire Spacing

For a fixed wire width, if we increase wire spacing to its neighbors, its coupling capacitance decreases. Considering a parallel plate relation between the wire and its neighbor, there is an inverse relation between the distance d and the capacitance C, which is expressed by $C = \varepsilon_o A/d$ where A is the area of the plate and ε_o is the permittivity. The increased spacing between wires translates into reduced SE crosstalk noise on the victim line.

With wire spacing, the ground capacitance of the victim increases some due to fact that some electric fields cannot reach the neighbor wire, instead they now contribute to ground capacitance.

Figure 7.7 shows the effect of spacing on SE induced crosstalk. The simulation is first performed with minimum spacing which is defined as S = W, then the spacing is increased in multiples of W. Result shows that wire spacing is the most effective means for controlling the SE crosstalk but this comes with burden of using large routing area hence results in large area penalty.

Figure 7.8 shows the effect of spacing on total victim line delay. The simulation is performed with minimum spacing which is defined as $S = W$ (the wire width), then the spacing is increased in multiples of W. The effect of spacing on SE crosstalk delay is observed for a fixed deposited charge of 150 fC on the aggressor driver. Result shows that wire spacing technique is very effective in reducing the victim delay in all three technologies.

The mitigation, however, occurs with some large area penalty because of the waste of routing resources.

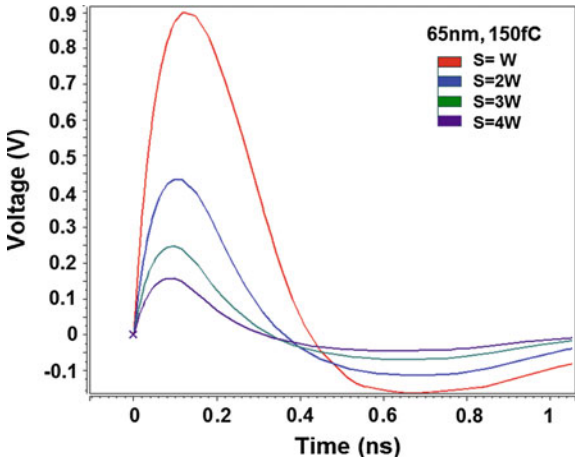

Fig. 7.7 The effect of wire spacing on SE crosstalk

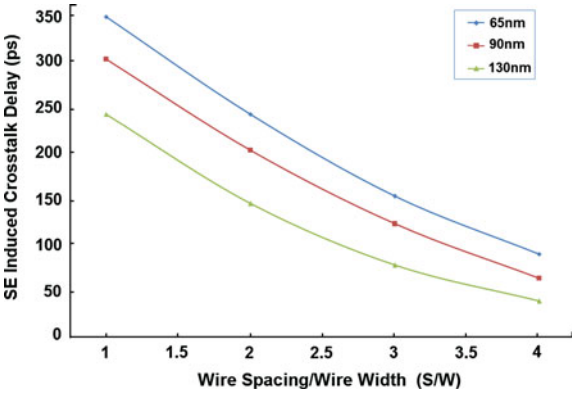

Fig. 7.8 The effect of wire spacing on SECD for 65, 90 and 130 nm technologies considered

7.2.5 Shielding Method

In the shielding technique, a voltage supply or ground interconnect can be inserted between the aggressor and victim interconnects to reduce the SE crosstalk. Since V_{DD} and ground lines are routed for powering the logic and test circuits; it may be manageable to reroute these power interconnects to provide shielding for interconnect impacted by SE crosstalk noise.

This approach does have the drawback of increasing the victim total ground capacitance and can have increased delay effects on victim.

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Chapter 8
Soft-Error Aware Power Optimization

8.1 Introduction

The increasing use of portable devices and higher demand on battery life has made power consumption even more important in nanoscale circuit designs. Leakage currents have increased drastically with each technology scaling and become a major contributor to total chip power consumption. Three major types of leakage mechanisms exist: subthreshold leakage, gate leakage, and reverse-biased junction leakage current. The most important one is the subthreshold leakage current which flows between the source and drain of a MOSFET transistor when the transistor is in sub-threshold region, or weak-inversion region. The aggressive scaling of oxide thickness results in a tunneling current through the transistor gate insulator giving rise to gate leakage component. The leakage current, on the other hand, occurs in drain-substrate and source-substrate junction due to band-to-band-tunneling (BTBT) mechanism [1].

In order to meet these challenges, there have been several efforts extending from the circuit level to the architectural level at reducing the leakage current and leakage power. Circuit mechanisms include adaptive substrate biasing, dynamic supply scaling, dynamic frequency scaling, and supply gating [2, 3].

As circuit designers try to address the excessive power consumption problem, they need to be also aware of the impact of the power optimizations on circuit SE robustness. With diminishing transistor sizes, circuit node capacitances and transistor drive currents continuously reduce. At the same time the increasingly denser chips raise soft error rates making them an important design issue.

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For mission-critical or high-reliability applications such as military, avionics [4], medical systems [5], etc., where reliability is as important as energy efficiency, designers need to make clever design choices that reduce static power consumption and improve soft error reliability of the newer designs [6].

8.2 Power Optimization and Reliability

In order to reduce power consumption in chips, one common approach has been the scaling of the power supply voltage. However, this should be accompanied by threshold voltage reduction in order to keep circuit speed and high current drive to avoid performance penalties. On the other hand, the threshold voltage reduction results in great amount of increase on the sub-threshold leakage current [7].

One solution is the use of the dual-threshold technique. Dual threshold CMOS exploits the delay slack in non-critical paths to reduce leakage power. In the dual-threshold methodology, designers assign a low threshold voltage to timing-critical path devices and a high threshold voltage to non-critical path transistors. The high threshold transistors reduce the subthreshold current, while low threshold transistors are used to achieve high performance on critical paths. The different threshold devices can be provided by the fabrication process by varying different parameters: e. g. changing the channel doping profile, the body bias etc.

While this method results in a high subthreshold leakage current for the critical path transistors, it can significantly reduce the overall leakage.

Degalahal et al. [8] have analyzed the effect of increasing threshold (used for leakage power reduction on non-critical paths) on circuit soft error rate and found that increasing threshold voltages can cause devices to slow down, which in turn increase CL circuit susceptibility to SETs.

Voltage scaling is a very common technique to reduce dynamic and leakage power consumption. In supply scaling, multiple supply voltages are used where critical and non-critical paths of the design are clustered and powered by higher and lower voltages, respectively. The work in [8] also found that critical charge values reduce as voltage reduces for adder circuits considered. Hence, circuits with reduced supply voltages become more susceptible to soft errors.

Some researchers also used power optimization technique to make circuits robust to radiation. For increasing CL soft error tolerance, Dhillon et al. have proposed a technique [9] that used optimal assignment of gate sizes, supply voltages, and threshold voltages while meeting timing constraints. Later work [10] has suggested an algorithm that employs voltage assignment (dual-V_{DD}) for SEU robustness. However, both techniques obtained potentially large power overheads.

Finally, the work in [11] has presented a power-aware methodology for soft error hardening using dual supply voltages. In this methodology, a higher supply voltage is assigned to the gates that have large error impact and contribute most to the overall SER.

8.3 Analyzing the Effect of Threshold on SEU and Soft Delay Errors

For advanced technologies, circuit scaling causes reduced supply voltages, transistor drive currents and shrinking node capacitances. All these factors can contribute to increased circuit sensitivity to SETs in CL due to reduced critical charge. In addition to SETs, SE soft delay effects also increasingly occur with newer technologies. The soft delay effects must also be considered in the analysis in addition to SETs as the two error mechanisms are different in the way that they are masked. For a CL circuit, SETs can be masked by logical masking, electrical masking, and latch window masking. For soft delay error (SDE), on the other hand, electrical masking does not apply. If a signal is once delayed then it can propagate to the circuit output through functionally sensitized path without any attenuation of the delay.

Gill et al. have compared SET and soft delay sensitivities of various benchmark circuits for a maximum LET of 20 MeV and found out that a higher number of nodes were sensitive to soft delay effects than SET due to absence of electrical masking effect for SDE [12].

Hence, this section studies the effect of transistor threshold for both soft error and soft delay tolerance. For this, a string of six inverters shown in Fig. 8.1 has been used in order to analyze the effect of threshold voltage on SET and soft delay effects. For SETs, the input of the first inverter is tied to logic 1, and for soft delay measurements, to a switching input waveform. In the analysis, the 65 nm technology with parameters obtained using the Predictive Technology Model in [13] has been considered.

An SE hit was simulated at the output of the first inverter using a double exponential current pulse [14] that is given by:

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta}\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right) \tag{8.1}$$

where,

Q is the charge (positive or negative) deposited by the particle strike, τ_α is the collection time constant of the p-n junction, τ_β is the ion-track establishment time constant.

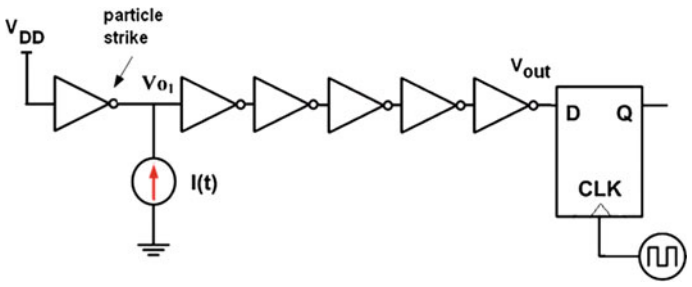

Fig. 8.1 The inverter string used in HSpice simulations

The time constants τ_α and τ_β are dependent on process technology and are taken as 100 and 5 ps, respectively based on [15]. This double pole representation has been used as an approximation to waveforms seen in mixed-mode simulations.

When the collected charge Q_{col} at a particular node exceeds the critical charge Q_{crit} of that node, the generated transient voltage can propagate and may be latched, resulting in a soft error. The critical charge here can be defined as the minimum charge collected due to a particle hit that can cause a change in circuit output. In all our simulations for critical charge, it was assumed that no masking effects occur, hence the circuits have been setup in such a way to prevent masking effects. In order to determine the critical charge, the deposited charge is slowly increased until an SET appears at the output of inverter string which cause a bit flip in storage element. For each pulse received at the output, the timing of the pulse has been varied to see if latching occurs for that particular pulse.

Since the aim here is to examine the effect of decreasing threshold on circuit SET, the threshold voltage value has been modified via vth_0 parameter using *delvto* option in Hspice. The results obtained for the inverter string can be seen in Fig. 8.2. In this simulation, the nominal threshold voltage for the NMOS transistor is $V_{th} = 0.29$ V.

The results show that a 100 mV reduction from normal threshold value increases Q_{crit} by 33 %. This indicates that if threshold voltage can be reduced, the circuit robustness to SETs could be increased as the critical charge value of a node becomes larger. On the other hand, increasing threshold values decrease circuit tolerance to SETs. This confirms the results of Degalahal et al. [8].

For studying the effect of threshold on soft delay effect, a pulse signal has been connected to the input of the first inverter in the inverter string shown in Fig. 8.1. A radiation hit has been injected roughly halfway during a falling transition (for

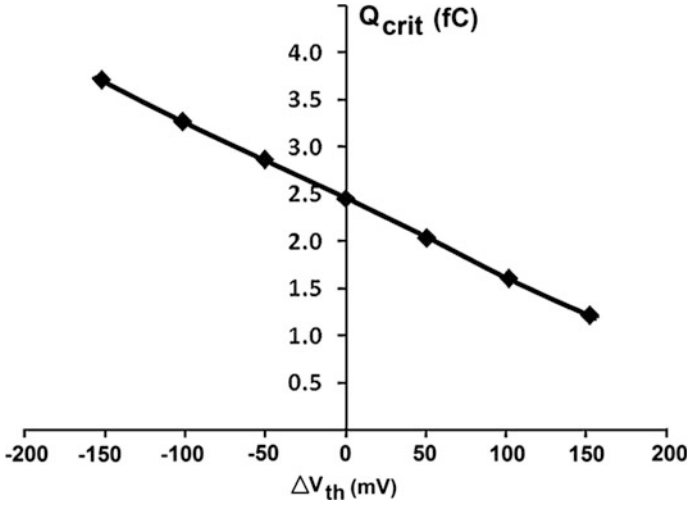

Fig. 8.2 Change in *Qcrit* with change in device threshold

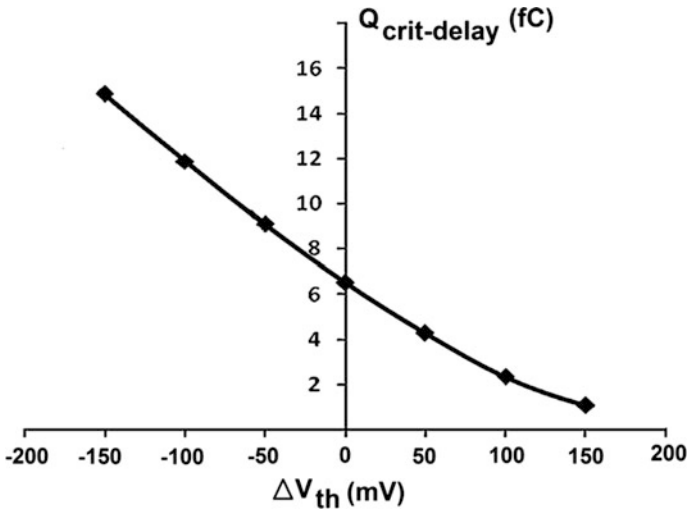

Fig. 8.3 Change in $Q_{crit\text{-}delay}$ with change in device threshold

maximum delay) at the output of the first inverter using double exponential current source and the delay change has been observed.

For soft delay calculation, the 50 % delay at the output V_{out} is first recorded in the presence of an SE charge. The delay measurement is then repeated with SE current source removed (no SE charge). The difference between the two delays is recorded as a "soft delay" at the output of the inverter string.

The critical charge for an SDE, $Q_{crit\text{-}delay}$ can be defined as the minimum charge collected due to a particle strike that produces sufficient delay such that the delayed signal arrives during the setup time of the storage element. In order to determine $Q_{crit\text{-}delay}$, the deposited charge is slowly increased until latching occurs at the storage element.

Figure 8.3 shows the effect of threshold voltage on the critical charge $Q_{crit\text{-}delay}$ for the inverter circuit. The result shows that circuit robustness to soft delay effect can be increased with decreasing threshold voltage

8.4 Body-Bias Techniques

8.4.1 Reverse Body-Bias

In an n-well CMOS bulk technology, the p-substrate and n-wells are typically biased to the ground and power supply, respectively. However, with separate substrate biasing possibility (triple-well CMOS and SOI technologies), one can reduce subthreshold leakage during standby mode in portable applications.

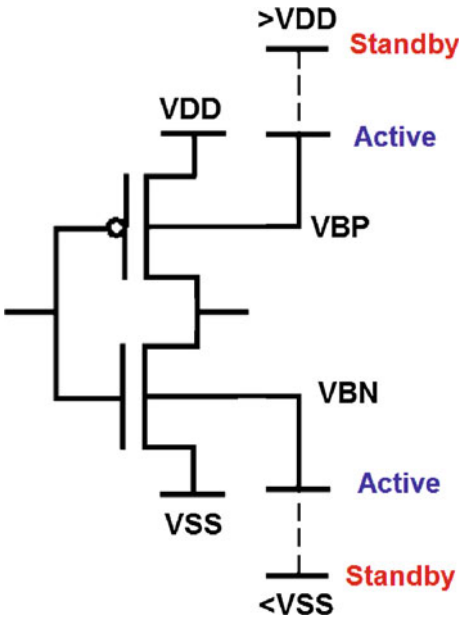

Fig. 8.4 VTCMOS technique applied to an inverter

In Variable Threshold CMOS (VTCMOS) technique, a zero body-bias is applied to the transistors during the active mode. However, during standby periods, the body bias is connected to a voltage greater than V_{DD} for a PMOS and to a voltage lower than V_{SS} for the NMOS transistor to cut-off the leakage current as in Fig. 8.4 (repeated here for convenience purposes from Chap. 3).

In many cases, the highest performance of the circuit may not be required at all times. Hence, dynamic threshold (V_{th}) scaling (DVTS) scheme uses body biasing to adjust the threshold voltage based on the performance demand. This technique uses the same VTCMOS concept. However, it modifies threshold based on circuit performance demand. The low threshold is provided via zero body bias, when the highest performance is required. In the case of slow performance demand, the threshold is increased via reverse body bias to minimize the leakage.

Based on the previous analysis in Sect. 8.3, reverse body bias should reduce circuit tolerance to radiation as the transistor threshold will be increased. The work in [16] studied the effect of body bias and found out that reverse body biasing can cause CL soft error rateto increase.

8.4.2 Forward Body-Bias

Operating the transistors of a digital logic in the sub-threshold region has been proposed for low power consumption. However, the power supply voltage reduction should be followed by threshold voltage reduction in order avoid performance

penalties and to maintain high current drive. Sub-threshold leakage current, on the other hand, increases as threshold voltages reduces.

One solution proposed to solve this problem is the dynamic threshold technique that applies an active body-bias to MOSFETs [17, 18]. In this technique, transistors are normally high threshold transistors. Hence, when they are off, minimal leakage current flows. In the case that a transistor switches, a forward body bias is applied which reduces the switching transistor threshold. This increases the on transistor drive current drive and hence improves circuit performance.

In a DTMOS logic gate, all transistor gates are tied to their substrates (Fig. 8.5). The high speed operation is provided by forward bias to switching transistors, while low leakage is obtained by applying zero bias to other transistors. Specifically, the body-source junction is "forward biased" (at less than 0.6 V) forcing the threshold voltage to drop.

Because of low threshold voltage during the logic transition and high threshold voltage during the off-state, the dynamic threshold circuit operates at high speed with low power. The DTMOS technique allows the use of ultra-low voltages (0.6 V and below) and is considered a promising candidate [17, 18] for low-power and

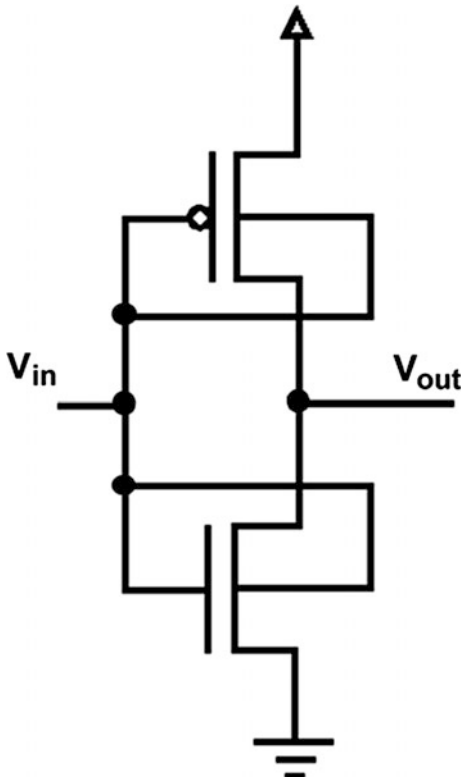

Fig. 8.5 DTMOS technique applied to an inverter

high-speed circuit devices since it can improve the circuit speed without increasing the stand-by power consumption.

Our analysis in Sect. 8.3 indicated that decreasing threshold voltage increases the critical charge of logic circuits thus providing more robustness to SETs and to soft delay effects. In a normal DTMOS scheme, the body-source junction is "forward biased" (at less than 0.6 V), forcing the threshold voltage to drop and hence DTMOS gate should be more tolerant to SEUs and soft delay effects compared to normal body-tie configuration [7]. The detailed DTMOS analysis will be covered in the next chapter.

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Chapter 9
Dynamic Threshold Technique for Soft Error and Soft Delay Mitigation

9.1 Various DTMOS Configurations

As mentioned in the Chap. 8, dynamic threshold MOS (DTMOS) technique can address the subthreshold leakage problem. Normally, power supply voltage reduction is usually followed by threshold voltage reduction in order avoid performance penalties. On the other hand, the subthreshold leakage current increases as threshold voltages reduce. The DTMOS technique addresses this problem. In the dynamic threshold technique high threshold transistors are normally used, hence minimal leakage current flows when these transistors are in off state. In the case a transistor switches, forward body bias is applied to the transistors and this reduces the transistor threshold [1, 2]. Hence, the switching transistor would have its current drive increased hence circuit performance would improve with forward body biasing.

In a standard DTMOS logic gate, all transistor body terminals are connected to gate terminals as shown in Fig. 9.1. The forward bias applied to switching transistors provides high speed operation while the zero bias applied on the off transistors provides low leakage current. Specifically, the body-source junction is "forward biased" (at less than 0.6 V), forcing the threshold voltage to drop.

Various DTMOS inverter schemes have been proposed to improve standard DTMOS logic inverter. In order to reduce standby leakage current, Chung et al. have proposed a scheme with minimum size small auxiliary transistors [3]. The subsidiary transistors increase the current drive by managing the body bias as shown in Fig. 9.2. The input load of the inverter circuit is reduced since the output charges are used to raise the body potential of the main transistors.

Later Gil et al. proposed another scheme with subsidiary transistors (Fig. 9.3) that achieved better performance in terms of speed [4].

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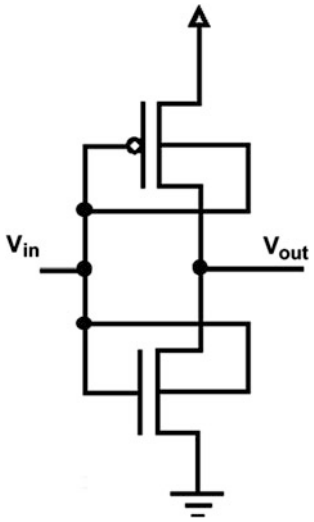

Fig. 9.1 DTMOS technique applied to an inverter

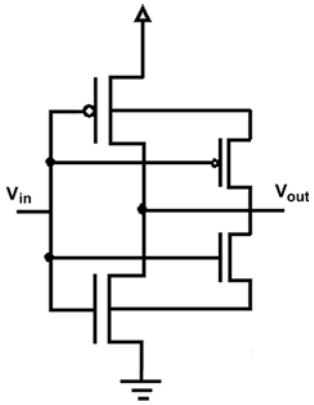

Fig. 9.2 DTMOS with auxiliary transistors [3]

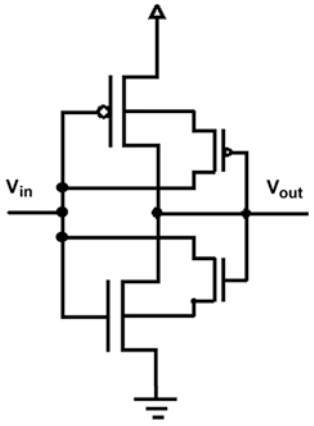

Fig. 9.3 Another DTMOS using auxiliary transistors [4]

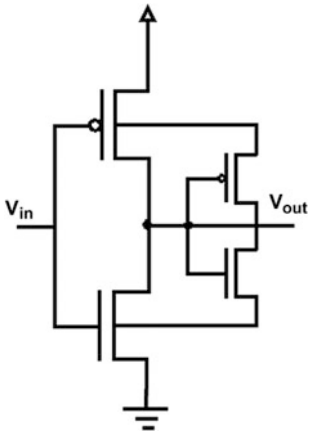

Fig. 9.4 DTMOS with subsidiary device gates tied to main transistor's drain [5]

Figure 9.4 illustrates another scheme of DTMOS subsidiary transistors, but this time the gates of subsidiary devices are tied to main transistor's drain instead of gate [5].

This configuration performs best in terms of power-delay product when compared to previous schemes, namely, the standard DTMOS scheme, and circuits of Figs. 9.3 and 9.4.

Finally, in the configuration shown in Fig. 9.5, transistor drains are tied directly to substrates. Soleimani et al. [6] reported even better power efficiency using this style of DTMOS, although stability with respect to temperature has been reported as problematic compared to standard DTMOS configuration.

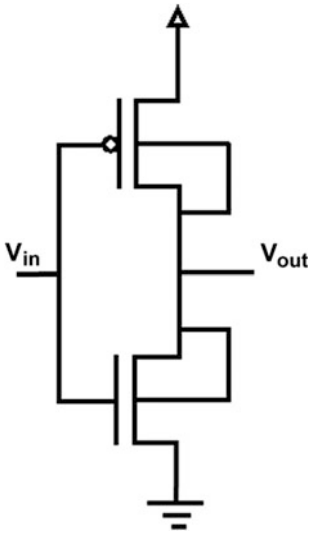

Fig. 9.5 DTMOS configuration where drains tied to substrates [6]

9.2 Comparison of DTMOS Configurations

In this section, the dynamic threshold based schemes just discussed have been compared for their tolerance to SET and soft delay effects. These methods are widely used for high speed and low power operations. Results are then compared to that of conventional configuration where transistor body terminals connected to source terminal.

In the comparison, five different circuits including benchmark circuits have been utilized. These circuits are a 6-stage inverter chain, an ISCAS-85 c17 and a c432 benchmark circuit, a full Adder module in ISCAS-85 c6288 and finally the ALU module from AM2901 4-bit microprocessor bit-slice. Although it is dated, the ALU module alone contains 83 gates, 12 input and 10 outputs and 276 SE vulnerable nodes [7].

In these configurations, the power supply voltage was taken as 0.6 V and the gate sizes have been assumed as minimum size. The hit locations for these circuits were selected at nodes close to primary inputs. For example, in the c17 benchmark circuit shown in Fig. 9.6, node "n2" was selected as the hit location and an erroneous signal due to an SET was propagated to the output for observation.

An SE hit was simulated at the output of the first inverter using a double exponential current pulse [8] that is given by:

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta}\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right) \tag{9.1}$$

where,

Q is the charge (positive or negative) deposited by the particle strike, τ_α is the collection time constant of the p-n junction, τ_β is the ion-track establishment time constant.

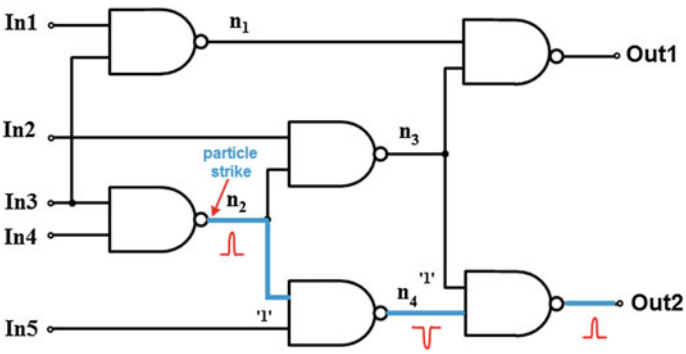

Fig. 9.6 SET Propagation in ISCAS-85 c17 Circuit

The time constants τ_α and τ_β are dependent on process technology and are taken as 100 ps and 5 ps, respectively based on [9]. The double pole representation has been used as an approximation to waveforms seen in mixed-mode simulations.

In all simulations for critical charge, it has been assumed that no masking effects occur, hence the circuits have been setup in such a way to prevent masking effects. In order to determine the critical charge, the deposited charge is slowly increased until an SET appears at the output.

For soft delay calculation, the 50 % delay at the circuit output is first recorded in the presence of an SE charge. The delay measurement is then repeated with SE current source removed (no SE charge). The difference between the two delays is recorded as a "soft delay" at the output.

The critical charge for an SDE, $Q_{crit\text{-}delay}$ is defined as the minimum charge collected due to a particle strike that produces sufficient delay such that the delayed signal arrives during the setup time of the storage element. In order to determine $Q_{crit\text{-}delay}$, the deposited charge is slowly increased until latching occurs at the storage element.

The minimum (critical) soft delay required at the output to produce a SDE normally varies based on signal arrival time at storage element input. In simulations for $Q_{crit\text{-}delay}$, a critical delay of 200 ps was assumed for simulation convenience as vulnerability of different DTMOS configurations is compared. The minimum charge that created the critical delay has been recorded as critical charge $Q_{crit\text{-}delay}$.

The results for the critical charge simulation can be seen in Table 9.1. The first row shows the critical charge values for soft errors (SEU) and soft delay errors (SDE) when using a normal body tie design. For all four circuits considered, the body tie design achieves the smallest critical charge amongst all techniques and hence becomes the most vulnerable in terms of SET and soft delay effects. Compared to normal body tie design, all techniques improve critical charge, yet the standard DTMOS technique shows superior characteristics in terms of SEU robustness due to highest critical charge in all cases.

The critical charge value needed for soft errors in standard DTMOS configuration is approximately 50 % more than what is required for normal body tie scheme for most cases, and hence is more robust in terms of SEU tolerance.

The reason can be explained as follows: Referring to Fig. 9.1, when the input to the DTMOS inverter is low, the body for PMOS transistor is low and hence the body of the PMOS transistor gets a forward bias with respect to source terminal. Since this increases the drivability of the PMOS transistor, a negative SET at the output can be easily dissipated due to increased PMOS transistor current drive. A similar explanation can be made for the case that the input is high and a positive SET is present at the inverter output.

For soft delay error, the critical charge values for the standard DTMOS scheme is more than 60 % higher almost in all cases compared to the normal body tie configuration. This can also be explained by referring to the inverter shown in Fig. 9.1. If we assume the input waveform is a rising from logic low to high, a positive charge deposited by an SE particle on the output may result in a delay increase or soft delay on the output falling waveform. When input rises from low to

Table 9.1 Critical charge values for various dynamic threshold inverter schemes

Configuration	6-stage inverter		c17 ISCAS-85		ISCAS-85 c432		ISCAS-85 c6288		AM2901 ALU module	
	Q_{crit} (fC)	$Q_{crit\text{-}del}$ (fC)	Q_{crit} (fC)	$Q_{crit\text{-}del}$ (fC)	Q_{crit} (fC)	$Q_{crit\text{-}del}$ (fC)	Q_{crit} (fC)	$Q_{crit\text{-}del}$ (fC)	Q_{crit} (fC)	$Q_{crit\text{-}del}$ (fC)
Normal body tie	2.46	6.51	1.70	2.07	2.63	6.51	2.58	6.34	2.03	1.99
Standard DTMOS	3.72	11.05	2.64	4.56	3.76	10.30	3.79	10.86	3.01	3.74
Figure 9.2 [3]	3.27	7.96	2.31	2.65	3.42	8.14	3.48	7.82	2.87	2.53
Figure 9.3 [4]	3.53	8.33	2.50	2.55	3.59	7.94	3.64	7.98	3.44	2.56
Figure 9.4 [5]	2.66	10.00	1.80	3.55	2.84	9.42	2.84	9.46	2.16	2.84
Figure 9.5 [6]	3.22	9.39	2.12	3.24	3.34	9.26	3.36	8.81	2.56	3.02

high, the body of the NMOS transistor follows the input and as a result it gets a forward bias. This causes the output waveform to switch more rapidly and results in a reduced soft delay.

9.3 Soft Error and Soft Delay Hardening Using DTMOS

Many circuit level techniques have been proposed by researchers to mitigate SETs in in CL. Driver sizing technique, for example, increases device capacitance and drive current to decrease device vulnerability to SEUs. Larger drive strengths of NMOS and PMOS transistors quickly dissipate the collected charge and reduce the vulnerability to single event particles [10]. However, hardening against soft delay errors (SDEs) is also necessary in addition to SET hardening as soft delay effects will also be more pronounced in newer technologies due to reduced circuit node capacitances. Gill et al. suggested the use of driver sizing technique in mitigating the soft delay effects, but this happens with the burden of increasing area and power penalties [11].

The proposed hardening technique is based on the combined use of the standard DTMOS scheme along with driver sizing [12]. This combined approach results in considerable area saving compared to driver sizing alone. This is possible since a standard DTMOS gate is more SE robust compared to a conventional one.

In sizing simulation, the 6-stage inverter chain consisting of conventional inverters is first considered and various deposited charges in between 10–150 fC have been applied. For each charge level, the necessary hit inverter size to eliminate the soft error and soft delay effect are determined. For SET induced errors, the gate transistors are sized up until the soft error at the output is completely eliminated. For soft delay reduction, the hit driver has been sized up such that the delay is reduced to less than 200 ps. The same process has then been carried out for the standard DTMOS inverters.

Finally, the above procedure was repeated for all four example circuits, and necessary gate sizes were determined to eliminate soft error and soft delay error effects.

Table 9.2 shows the results obtained for all four circuits examined. The first column level indicates the deposited charge levels. For simplicity, the sizing has been done using whole driver sizes. In this table, for each circuit, there are two entries at each charge level. The first entry indicates the size needed in driver sizing only method and the second (bold) entry represent DTMOS gate sizes.

In order to visualize this better, the average driver size (of all five circuits) needed to mitigate soft errors and SDEs at a particular hit charge was also determined and then compared to DTMOS result as shown in Fig. 9.7. For each error effect, the blue or dark bar represents the sizing needed for a conventional driver gate and the orange bar (light color shown next to it) represents the needed driver size in DTMOS configuration.

Table 9.2 Gate sizes required for soft error and soft delay mitigation at various deposited charges

Depth charge (fC)	6-stage inverter		c17 ISCAS-85		ISCAS-85 c432		ISCAS-85 c6288		AM2901 ALU module	
	SEU	SDE	SEU	SDE	SEU	SDE	SEU	SDE	SEU	SDE
10	5X	2X	7X	4X	4X	2X	4X	2X	5X	4X
	3X	**1X**	**5X**	**2X**	**3X**	**1X**	**3X**	**1X**	**4X**	**3X**
25	11X	3X	17X	9X	10X	4X	9X	4X	11X	11X
	7X	**2X**	**11X**	**4X**	**7X**	**2X**	**6X**	**3X**	**8X**	**6X**
50	21X	6X	34X	17X	19X	7X	17X	7X	20X	23X
	15X	**4X**	**22X**	**8X**	**14X**	**4X**	**11X**	**5X**	**16X**	**11X**
100	42X	12X	67X	34X	38X	13X	33X	13X	36X	47X
	29X	**7X**	**44X**	**15X**	**28X**	**9X**	**17X**	**9X**	**29X**	**23X**
150	62X	18X	100X	50X	57X	19X	50X	19X	51X	83X
	43X	**11X**	**66X**	**22X**	**42X**	**13X**	**21X**	**14X**	**42X**	**33X**

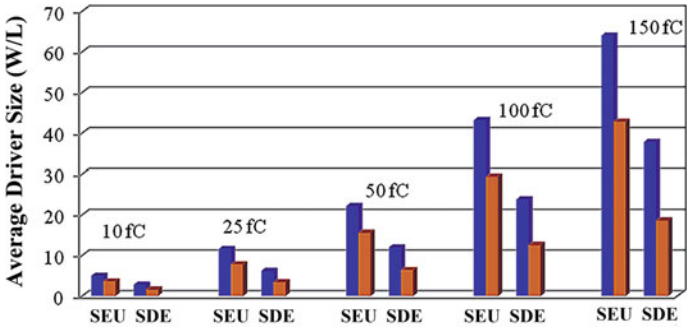

Fig. 9.7 Average driver sizes needed for SEU and SDE mitigation in conventional and DTMOS driver configurations: Dark (*blue*) bar to the left represents the gate size needed for conventional driver; the light bar (*orange*) shown next to it shows the gate size needed for DTMOS driver configuration

Results show that the standard DTMOS technique can be used along with gate sizing in mitigating the SETs and soft delays using considerably less area overhead than conventional driver sizing [12]. Compared to the conventional driver sizing technique in [10], the combine approach saves about 30 % in circuit area in SET mitigation, and results in approximately 50 % area savings in soft delay error mitigation.

9.4 Summary

This chapter presented an analysis on various DTMOS schemes for their soft error tolerance using various benchmark circuits including AM2901 microprocessor bit-slice. The analysis results indicate that all DTMOS configurations increase circuit robustness to SE induced soft errors and delay effects due to increased transistor current drive. The standard DTMOS configuration, however, shows superior characteristics in terms of SEU robustness due to highest critical charge in all cases. To exploit this effect, this technique can be combined with driver sizing technique to mitigate SETs and soft delay effects with lot more area efficiency than driver sizing technique used alone.

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