

# RADIATION EFFECTS AND SOFT ERRORS IN INTEGRATED CIRCUITS AND ELECTRONIC DEVICES

Editors

R. D. Schrimpf

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# **RADIATION EFFECTS AND SOFT ERRORS IN INTEGRATED CIRCUITS AND ELECTRONIC DEVICES**

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Editors

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## Preface

Electronic devices in space, defense, medical, and power systems may be exposed to various types of radiation, including high-energy photons and energetic particles (electrons, protons, neutrons, and ions). The radiation may produce effects in the electronics ranging from temporary loss of data to catastrophic failure. The specific effects produced depend strongly on the specific technology and the radiation environment. Most systems designed for use in radiation environments are designed conservatively using electronic parts that are at least several generations behind the current state of the art. However, the demand for higher performance and reduced time from design to deployment has increased the pressure to use advanced technologies. The effects of radiation in some advanced technologies are poorly understood, or in some cases, completely unknown. In addition, highly scaled devices may be sensitive to the naturally occurring radiation at the earth's surface, even though the atmosphere provides significant protection.

This volume discusses radiation effects at the material, device, and circuit levels. The emphasis is on effects produced by the cumulative energy deposited by the radiation (total ionizing dose effects) and transient effects caused by single ionizing particles (single-event effects). Bipolar (Si and SiGe), metal-oxide-semiconductor (MOS), and compound semiconductor technologies are considered. In addition to considering the specific issues associated with high-speed devices and technologies, the background material necessary to understand radiation effects at a more general level also is included.

The volume opens with a description of single-event effects, with an emphasis on high-speed devices and test procedures. These include papers by Normand on single event effects in avionics and on the ground, by Baumann on soft errors in commercial integrated circuits, and by McMorrow, Melinger, and Knudson on III-V semiconductor electronics. In addition, the investigation of single-event transients in high-speed circuits with a pulsed laser is described by Fouillat, Pouquet, Lewis,

Buchner, and McMorrow. Design techniques for improving radiation tolerance are discussed, including layout approaches, circuit design issues, and error correction. Heidergott describes system level single event upset mitigation strategies; Holman discusses radiation-tolerant design for high performance mixed-signal integrated circuits; and Nowlin, Bailey, Turfler, and Alexander describe a total-dose hardening-by-design approach for high-speed mixed-signal CMOS integrated circuits.

Radiation effects in several specialized areas are considered, including high-energy physics experiments (Faccio), optocouplers (Reed, Marshall, and LaBel), charge-coupled device imagers and CMOS active pixel sensors (Hopkinson and Mohammadzadeh), power devices (Shenai, Galloway, and Schrimpf), silicon-on-insulator electronics (Cristoloveanu and Ferlet-Cavrois), and silicon-germanium heterojunction bipolar transistors (Cressler). Descriptions of total-dose and displacement-damage effects in bipolar devices and circuits are provided in papers by Schrimpf and by Barnaby. The volume closes with papers discussing hardness assurance issues (Pease), basic mechanisms of total ionizing dose effects in MOS devices (Cester and Paccagnella; Rashkeev, Fleetwood, Schrimpf, and Pantelides; and Oldham), and dosimetry (Dusseau and Gasiot).

Radiation effects is a changing and evolving discipline; new issues and effects are identified as devices become smaller and new technologies are introduced. We have endeavored to provide descriptions of the basic phenomena required to understand radiation effects, as well as define important issues relevant to advanced technologies.

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## CONTENTS

Preface	v
Single Event Effects in Avionics and on the Ground <i>E. Normand</i>	1
Soft Errors in Commercial Integrated Circuits <i>R. C. Baumann</i>	15
Single-Event Effects in III-V Semiconductor Electronics <i>D. McMorrow, J. S. Melinger, and A. R. Knudson</i>	27
Investigation of Single-Event Transients in Fast Integrated Circuits with a Pulsed Laser <i>P. Fouillat, V. Pouget, D. Lewis, S. Buchner, and D. McMorrow</i>	43
System Level Single Event Upset Mitigation Strategies <i>W. F. Heidergott</i>	57
Radiation-Tolerant Design for High Performance Mixed-Signal Circuits <i>W. T. Holman</i>	69
A Total-Dose Hardening-By-Design Approach for High-Speed Mixed-Signal CMOS Integrated Circuits <i>N. Nowlin, J. Bailey, B. Turfler, and D. Alexander</i>	83
Radiation Issues in the New Generation of High Energy Physics Experiments <i>F. Faccio</i>	95
Space Radiation Effects in Optocouplers <i>R. A. Reed, P. W. Marshall, and K. A. Label</i>	117
Radiation Effects in Charge-Coupled Device (CCD) Imagers and CMOS Active Pixel Sensors <i>G. R. Hopkinson and A. Mohammadzadeh</i>	135
The Effects of Space Radiation Exposure on Power MOSFETs: A Review <i>K. Shenai, K. F. Galloway, and R. D. Schrimpf</i>	161
Introduction to SOI MOSFETs: Context, Radiation Effects, and Future Trends <i>S. Cristoloveanu and V. Ferlet-Cavrois</i>	181

Total-Dose and Single-Event Effects in Silicon-Germanium Heterojunction Bipolar Transistors <i>J. D. Cressler</i>	205
Gain Degradation and Enhanced Low-Dose-Rate Sensitivity in Bipolar Junction Transistors <i>R. D. Schrimpf</i>	219
Total Dose Effects in Linear Bipolar Integrated Circuits <i>H. J. Barnaby</i>	235
Hardness Assurance for Commercial Microelectronics <i>R. L. Pease</i>	259
Ionizing Radiation Effects on Ultra-Thin Oxide MOS Structures <i>A. Cester and A. Paccagnella</i>	279
Hydrogen at the Si/SiO <sub>2</sub> Interface: From Atomic-Scale Calculations to Engineering Models <i>S. N. Rashkeev, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides</i>	291
Switching Oxide Traps <i>T. R. Oldham</i>	297
Online and Realtime Dosimetry Using Optically Stimulated Luminescence <i>L. Dusseau and J. Gasiot</i>	321

## SINGLE EVENT EFFECTS IN AVIONICS AND ON THE GROUND

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Single event effects in electronics caused by the atmospheric neutrons have been an issue for systems using large blocks of random access memory (RAM) in avionics applications as well as those on the ground. At ground level there are two main sources of single event effects, alpha particles from the packaging materials as well as the neutrons, but at aircraft altitudes, where the neutron flux is about 300 times higher than the ground, the alpha particles make a negligible contribution. We review the trends over the last 5-10 years in the response of COTS computer systems to single event effects, taking into the response of devices as well as fault tolerant measures incorporated into the systems.

**Keywords:** Single event effect, single event upset, avionics, single event burnout, cosmic ray neutrons, atmospheric neutrons, aircraft altitudes

### 1. Introduction

We can distinguish four generally distinct environments in which man has placed his technologically developed hardware: under the sea, on land, in the atmosphere via airplanes and balloons and in space. For three of these environments, land, atmosphere and space, when the man-made objects have included microelectronics, what has been observed is that the naturally occurring ionizing radiation field within these environments has interacted with the electronics, causing malfunctions. These effects in microelectronics are called single event effects (SEEs), and they have been discussed in numerous review papers<sup>1,2</sup>. A single event effect requires that the energy deposited by a single ionizing particle interacting with a microelectronics device be sufficient to cause it to malfunction. Single event upset (SEU), in which the deposited energy causes a single bit to flip its logic state, is the most common form of SEE, and the one for which most data has been accumulated.

In space, the potential for the electronics to undergo SEE from the naturally occurring ionizing radiation environment is widely known and accepted. Thus government and industry standards have been written to assure that the possibility of SEE in the electronics of spacecraft systems be formally addressed following accepted testing and analysis procedures. Elements of these standards or their equivalent have been incorporated into the requirements of almost all satellite programs. In addition, within the radiation effects community several thousand technical papers have been written covering: 1) occurrences of SEE effects in satellites, 2) the results of laboratory SEE tests to simulate the responses of electronics to the space environment and 3) methodologies to calculate the SEE rate of occurrence.

### 2. Similarities between SEE in Avionics and on the Ground

However, when it comes to SEE on the ground and in aircraft, the situation is drastically different. Until the mid-1990s there had been very limited recognition of the possibility and impact of single event effects in ground-based or airplane-based electronics. Only within the last five years have standards been, or are in the process of being, written that address SEE in electronics on the ground and in avionics.

## **2.1 SEU at ground level**

For ground level applications, JESD89, “Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices,”<sup>3</sup> was issued in 2001, after work was begun on it in the middle of 1999. In this case, NASA, which had the experience of SEE in space for almost two decades, was instrumental in working with the microelectronics vendors through SEMATECH and organizing the working group that produced JESD89. The Symposium On Space Radiation Effects On Terrestrial Electronics, spearheaded by NASA and sponsored by NASA along with the electronics industry (SEMATECH and SRC) in October, 1997, was a key activity that started the process of an organized and industry-wide approach. Previous to this, microelectronics companies had conducted their own proprietary research on SEU, also called soft errors, on an individual basis, often spending millions of dollars<sup>4</sup>.

However, based on this old approach, the possibility of SEU in microelectronics was known to only a few hundred people. By the late 1990s more technical papers on this topic had begun to appear, such as an entire issue of IBM Journal of Research and Development<sup>4</sup> and in a few papers each year at the International Reliability Physics Symposium<sup>5</sup>. In all of these, the actual upset rates recorded on the ground were never given in absolute units, until a paper written by someone from outside the microelectronics industry provided such measured SEU rates<sup>6</sup>. Nevertheless, this topic received a great deal more attention when it was written up in the popular press. Thus, in an article in Forbes magazine of November, 2000<sup>7</sup>, it was reported that Sun servers were having problems with dozens of machines crashing due to bit flips in the SRAM used for the L2 cache memory which were caused by cosmic rays or alpha particles. Sun Microsystems received a great deal of adverse publicity and hundreds of thousands of people became aware of the fact the cosmic rays can cause errors in memory chips. In this case, the problem was amplified because Sun initially blamed the vendor of the SRAMs. However, knowledgeable people in the industry knew that the real mistake was Sun’s solution to SEU in the L2 cache through parity protection, the cheapest way, but with the consequence of system shutdowns whenever a parity miscompare occurred<sup>8</sup>.

## **2.2 SEU in avionics**

With regard to avionics the situation is generally similar. A standard on the topic was begun at the end of 2001 by Technical Committee 107 within the IEC (International Electrotechnical Commission), with the title of TC107-AR “AVIONICS INDUSTRY-Standard for the Accommodation of Atmospheric Radiation Effects (SEE) Within Avionics Electronic Equipment”.

Beginning in the late 1980s, SEE in avionics had evolved from a series of interesting anecdotal incidents (relying exclusively on overall pilot observations) to accepted fact<sup>9</sup>. Following a series of proprietary flight experiments by IBM on aircraft in which upsets in a large array of SRAMs were measured, a joint IBM-Boeing study sponsored by DNA and NRL, collected actual in-flight upset data recorded in the CC-2E flight computer on military aircraft. This study, completed in 1992<sup>10</sup>, demonstrated that SEUs are real, that the measured in-flight rates correlate with the atmospheric neutron flux, and that the rates can be calculated using laboratory SEU data.

Since the IBM-Boeing study more technical papers have been written on SEE in avionics, including a review article<sup>9</sup>, but the number of papers on this topic has been just a few a year. Most of these papers have focused on methodologies for calculating the SEU rate and laboratory measurements in devices, so that the number of papers since Ref. 9 in which actual in-flight upsets in avionics have been measured are very rare<sup>11, 12</sup>. Similar to the situation with SEU on the ground, the possibility of SEUs in avionics has received more attention in trade magazines, such as EE Times<sup>13</sup>. Although EE Times has about 15% of the circulation of Forbes, the EE Times article, with the overly dramatic title "Engineer calls off-the-shelf components 'unsafe' for aircraft," did inform thousands of engineers and computer scientists of SEE in avionics as a potential threat. This isn't the first time that articles have appeared in trade magazines that put unrealistic emphasis on the potential problems with SEE in avionics and ignored the built-in fault tolerant features that protect against them.

Nevertheless, the fundamental issue that is in common regarding SEE in electronics used in aircraft and on the ground (sea level) is that the same kind of radiation field is largely responsible for the effects in both environments, and the same types of devices and circuit boards are involved. The first factor is that the radiation environment causing the SEE, primarily the high-energy neutrons created by the interaction of the cosmic rays with the atmosphere, is the same. These are often called atmospheric neutrons or cosmic ray neutrons. The intensity or flux level is about 300 times higher at aircraft altitudes than it is on the ground (sea level), but the energy spectrum is essentially identical. This is discussed further in section 4. For the same reason, accelerated laboratory testing of devices to estimate their SEE rate in both environments have used the same facilities. The neutron beam at the WNR (Weapons Neutron Research) facility within LANSCE (Los Alamos Neutron Science Center), which has an energy spectrum very similar to that of the atmospheric neutrons, has been utilized over the last 10 years for both ground level and avionics applications<sup>14</sup>. One hour in the WNR beam is equivalent to 1E5-1E6 hours at aircraft altitudes, depending on the beam intensity at the time of testing (3E7-3E8 hours at sea level). The second factor is the types of devices that are used are essentially the same, and this is largely dictated by the reality of using commercial-off-the-shelf (COTS) electronics and circuit boards for nearly all applications on the ground and in aircraft.

### **3. Differences Between SEE in Avionics and on the Ground**

Although there are strong similarities between SEE in avionics and on the ground, there are also differences. The differences derive mainly from the fact that the atmospheric neutron flux is so much higher at aircraft altitudes than it is on the ground. In addition, there is a second SEE effect, different from SEU, that is relevant on the ground in high voltage devices, but which to date, has not been an issue in aircraft.

#### ***3.1 Comparison of SEU mechanisms in electronics, neutrons and alpha particles***

At ground level there are really three sources of radiation that cause the SEUs, the high energy cosmic ray neutrons previously discussed, the thermal neutron component of the cosmic ray neutrons and alpha particles from the microelectronics package. The high-energy cosmic ray neutrons of concern are those with  $E > 10$  MeV, for which the neutron cross section in Si for reactions giving rise to energetic recoils is significant, since it is the energy deposited by recoils that cause the SEUs.

Thermal neutrons are those with energies centered at 0.025 eV, (comparable to the energy at room temperature) which is about 8 orders of magnitude lower than the high-energy neutrons. Thermal neutrons can be significant because they have a very high probability of interacting with certain isotopes, like B<sup>10</sup>. When a B<sup>10</sup> nucleus reacts with a thermal neutron, two reaction products are created, an alpha particle and a Li<sup>7</sup>, which have a combined 2.3 MeV of energy that can be deposited. If this energy is deposited within the sensitive volume of a microelectronic device, it can lead to a single event upset (SEU). Based on the testing of a small number of memories with a neutron source that included a thermal neutron component, some devices were found to be more susceptible to SEU from the thermal neutrons than from fission neutrons ( $E_{avg} \sim 1$  MeV, not nearly as high as the atmospheric neutrons), and a few were less susceptible<sup>15</sup>. It depended on the concentration and location of the B<sup>10</sup> within a particular device. Thus, thermal neutrons are a second source of ionizing radiation that can cause SEU in devices. Based on the best available calculations of the complex spectrum of cosmic-ray neutrons at various altitudes<sup>16</sup>, the ratio of thermal/>10 MeV neutrons is much higher on the ground than it is at aircraft altitudes. However, this may change when accurate account is taken of the contribution of the aircraft structure in producing thermal neutrons. Thus, on the ground, the thermal neutrons may be a larger contributor to the SEU rate, compared to that from the > 10 MeV neutrons, than they are at aircraft altitudes, but this conclusion may change once an accurate assessment is made of the thermal neutrons produced inside an aircraft.

It has been known that alpha particles contribute to the SEU rate on the ground for more than 20 years. When SEUs were first discovered in microelectronics on the ground<sup>17</sup> during the late 1970s, the cause was alpha particles emitted from the IC package. The actual source was uranium and thorium impurities found in trace amounts in the various production and packaging materials that emit alpha particles. Once this was recognized, several steps were taken to greatly reduce the problem, with the main one being that alpha particle detectors scanned all raw materials used in the IC manufacturing process. All materials having an emitted alpha particle flux above a threshold level were rejected. During the 1980s and early 1990s this worked very well. However, as packaging technologies changed and solder bumps were incorporated into newer style packages, the alpha problem re-emerged as solder became a packaging component. However, specially purified solder to minimize alpha emitters has been available, and the movement to utilize lead-free solder by IC vendors may reduce the problem. Thus for current devices, the SEU rate contribution on the ground due to alphas may be appreciable, comparable to that due to neutrons, in those devices with packages having standard solder bumps.<sup>18</sup>

The SEU rate from alphas remains the same on the ground and at aircraft altitudes. On the other hand, the high-energy (>10 MeV) neutrons are 300 times higher in the atmosphere compared to the ground. Thus, even if the SEU contribution from the alpha particles relative to the contribution from high-energy neutrons is significant on the ground, in the atmosphere, the SEU contribution from alpha particles is small enough to be neglected, and the entire focus placed on the high-energy neutrons.

### **3.2 Other SEE Effects in Low Voltage Devices**

It should also be noted that there are other single event effects that can be induced by > 10 MeV neutrons in low voltage ICs, including single event latchup (SEL), single event transient (SET), single event hard error (SHE) and multiple bit upset (MBU). These will

be summarized very briefly. Although many of these effects were measured primarily with high energy protons, as indicated in section 5, they are assumed to apply to high energy neutrons as well.

Many CMOS devices are susceptible to SEL from heavy ions. A small number of these have also been tested with beams of energetic protons and neutrons, and a few have been shown to be susceptible SEL from the protons and neutrons. Refs. 19 and 20 list a total of seven devices with proton SEL cross sections. Unfortunately, two very recent proton-induced latchup cross sections have been published for SRAMs<sup>21,22</sup> and these proton-induced SEL cross sections both exceed the largest previous proton SEL value<sup>19</sup>. There is thus a clear need to track the SEL susceptibility of new and emerging devices by energetic neutrons and protons.

An SEU-related event in some devices can lead to the generation of a single event transient (SET) that a device may interpret as a new bit of information. These transients are spurious signals or voltages, induced by the deposition of charge by a single particle that can propagate through the circuit path during one clock cycle. Most SET tests have been performed using beams of heavy ions, but SET has also been induced in linear devices with high-energy proton beams<sup>23,24</sup> hence the atmospheric neutrons can also cause this kind of effect. It has long been known that heavy ions can cause "stuck bits" in RAMs, events often referred to as single hard errors (SHE). These hard errors are due to very localized total dose effects in the gate oxide of sensitive transistors. More recently the first occurrence of SHE by protons in a laboratory test was published, indicating that in newer devices<sup>25</sup>, protons, and hence atmospheric neutrons, are capable of inducing stuck bits. Some RAM devices are also susceptible to multiple bit upset, MBU, in which more than one bit is upset by a single particle. In general, MBUs can be expected to involve more than a single logic word, however, with MBUs, energetic particles may also upset two or more bits in a single word, depending on the physical arrangement and size, and the distribution of the memory cells within a device. Generally, the MBU rate by protons or neutrons is at most 1-2% of the SEU rate, but some devices can be much more susceptible to MBU than others, even if they have similar SEU rates<sup>26</sup>.

### **3.3 SEE effects in high voltage devices**

The high-energy neutrons within the atmospheric neutron spectrum have also been shown to induce a different effect, single event burnout (SEB), in high voltage devices<sup>27</sup>. These devices include power MOSFETs and IGBTs (insulated gate bipolar transistors), but also higher voltage devices (>2000V) such as diodes and thyristors<sup>28</sup>.

It has been found most helpful to utilize the Kuboyama model<sup>29</sup> to understand the complex mechanism involved in SEB. Although it was developed to describe the SEB caused by heavy ions, it has been adapted to apply, in qualitative terms, to SEB caused by high-energy neutrons and protons (see Ref. 28 for further details). The main result is that the key to SEB susceptibility is the operating voltage. In all of the testing that has been carried out in which power MOSFETs and higher voltage devices (diodes and IGBTs) have been exposed to beams of high-energy neutrons and burnout measured<sup>27,28</sup>, there is always a threshold value for the drain-to-source voltage,  $V_{ds}$ , which must be exceeded in order for SEB to occur. Therefore, the best way of ensuring that high voltage devices are not susceptible to neutron-induced SEB is to operate devices at a sufficiently reduced voltage compared to their rated voltage, called derating. Good design practice, having

nothing to do with radiation effects, dictates that power MOSFETs be operated at a derated condition. However, it appears that additional derating is likely needed in order to adequately reduce the sensitivity of high voltage devices to SEB.

A number of power MOSFETs have been tested with beams of protons and energetic neutrons for SEB, and the results of these, the passing V<sub>ds</sub> values, have been tabulated<sup>27,28,30</sup>. Relying on these measured results and commonly used derating factors, we can generalize that, based on those devices that were tested, atmospheric neutrons are likely to induce SEB only in power devices rated at >400V. If the devices are derated and operated at a V<sub>ds</sub> of < 300V, the probability of an SEB should be low enough for SEB to be a negligible concern.

At the present time, avionics systems do not operate at voltages > ~270V DC. Although internal trade studies for future avionics systems have considered operation at much higher voltages, there are several distinct disadvantages to such high voltage operation. These include both SEB and arcing and corona effects, which pose major obstacles before such high voltage operation can be considered feasible. Nevertheless, because the higher voltage operation may lead to an overall reduction in system weight, there is a possibility of aircraft buses operating at voltages > 270 V, which will require careful consideration of SEB effects in the high voltage electronics.

At the ground level, the situation is different; very high voltage devices have been used for many years. The main application of these devices has been for controlling electric motors on trains, with such designs being common in Europe but not in the US. Thus the problem first surfaced in the field in Europe during the early 1990s when burnout failures of newly developed devices were experienced on trains. European and Japanese manufacturers of the high voltage semiconductors were puzzled by these failures, which had not occurred previously. The failure mode was investigated in great detail by the vendors and a variety of causes were proposed<sup>31</sup>. After a series of laboratory tests, including simultaneous testing in laboratories located on a rooftop and in a salt mine, at the end the cause was found to be the energetic cosmic ray neutrons at ground level<sup>31</sup>, even though their flux is very low (~20 n/cm<sup>2</sup>hr, E > 10 MeV).

Afterwards we demonstrated that accelerated testing with the WNR neutron beam at the LANSCE could be used to assess the SEB susceptibility of high voltage devices<sup>28</sup>. By measuring the SEB neutron cross section in the beam and normalizing to the neutron flux level on the ground (~20 n/cm<sup>2</sup>hr), the required reliability (FIT rate, number of failures in 1E9 device-hours) could be determined as a function of the applied voltage. This agreed with measured values from field failure data<sup>28, 32</sup>. Since then, manufacturers of very high voltage devices have been using the WNR beam to measure the susceptibility of new device designs to SEB, and obtain the required curve of the FIT rate as a function of applied voltage. In the US new designs for control systems are being developed that utilize the same kind of very high voltage devices, such as IGBTs and diodes rated at > 2000V. These systems are being considered for advanced solid-state induction modulators and klystron power supply systems at high-energy accelerator facilities, and also for advanced MRI (magnetic resonance imaging) equipment and related imaging controls. These devices, and the more standard power MOSFETs and IGBTs that American manufacturers are now designing for voltages > 1000V, will all be susceptible

to SEB by the atmospheric neutrons. This is a failure mode that such vendors will need to pay attention to as the devices are put into the field.

#### 4. Atmospheric and Ground Level Environments

The atmosphere is composed of a mixture of particles created by the interaction of the continuous stream of primary galactic cosmic rays (GCR) with the nitrogen and oxygen atoms in the atmosphere, and so are called secondary cosmic rays. As the primary GCR particles, mainly very high-energy protons, bombard the atmosphere, they create a cascade of secondary, tertiary, etc. particles. Thus, for each primary cosmic ray entering, many more secondary particles are created. At a very approximate level, the flux of incoming primary GCR at the top of the atmosphere is  $\sim 0.1$  particle/cm<sup>2</sup>-sec, and at aircraft altitudes, the flux of all secondary particles is  $\sim 100$  particle/cm<sup>2</sup>-sec. The density of the lower portion of atmosphere is high enough that most of the particles are absorbed, so that at sea level the flux of secondary particles is reduced to  $\sim 1$  particle/cm<sup>2</sup>-sec<sup>33</sup>.

The flux of secondary particles is not uniform around the earth due to the effect of the earth's magnetic field, which is strongest at the equator and weakest at the geomagnetic poles. In addition, the space weather can have a significant effect on the production of secondary cosmic rays due to several different effects. First, the activity on the sun follows an approximately 11 year solar cycle, such that during solar minimum conditions, the GCR particles propagate to earth more easily; thus the flux of secondary particles in the atmosphere is higher. In addition, occasional eruptions on the sun, (solar flares and coronal mass ejections), lasting hour-to-days, send out a stream of charged particles, which, when they reach the earth, generate additional secondary particles in the atmosphere like the GCR. The various factors involved and measurements of the particles have been discussed in greater detail in a variety of sources<sup>4,9,34</sup>.

Of the various secondary cosmic rays, three can induce SEU, neutrons, protons and pions (the pi-meson particles, with a rest mass of  $\sim 140$  MeV, that are involved in holding the nucleus together), and of these, the neutrons have the highest flux both in the atmosphere and on the ground. Three aspects of the neutrons are of main interest: 1) the energy spectrum, 2) the flux variation with altitude and 3) variation with latitude. The energy distribution of the atmospheric neutrons is usually presented by plotting the differential flux (flux per unit energy) as a function of energy. In Figure 1 we plot four neutron spectra at an altitude of approximately 40,000 ft. These include the original measurements made by Wilmot Hess in 1959<sup>35</sup>, a calculation by T. Armstrong<sup>16</sup>, a fit to measurement by made by NASA Ames<sup>36</sup> and 1997 DOE measurements in an ER-2 aircraft<sup>37</sup>. A fit to the NASA Ames data has been used in the past<sup>9</sup> as one component of an overall simplified model of the atmospheric neutrons. However, this data applies only up to an energy of 300 MeV, so a modification has been made to the model for E>300 MeV. The modified spectrum is given, with E in MeV, as:

$$\frac{dN}{dE} = \begin{cases} 0.346E^{-0.922} \times \exp[-0.0152(\ln E)^2] & E < 300\text{MeV} \\ 340E^{-2.2} & E > 300\text{MeV} \text{ n/cm}^2 \text{ sec MeV} \end{cases} \quad (1)$$

When this differential flux is integrated for E> 10 MeV, the integrated neutron flux is  $\sim 5600$  n/cm<sup>2</sup>hr. At ground level the flux is approximately a factor of 300 lower than at 40,000 ft, thus on the ground, the flux for E> 10 MeV is  $\sim 20$  n/cm<sup>2</sup>hr.

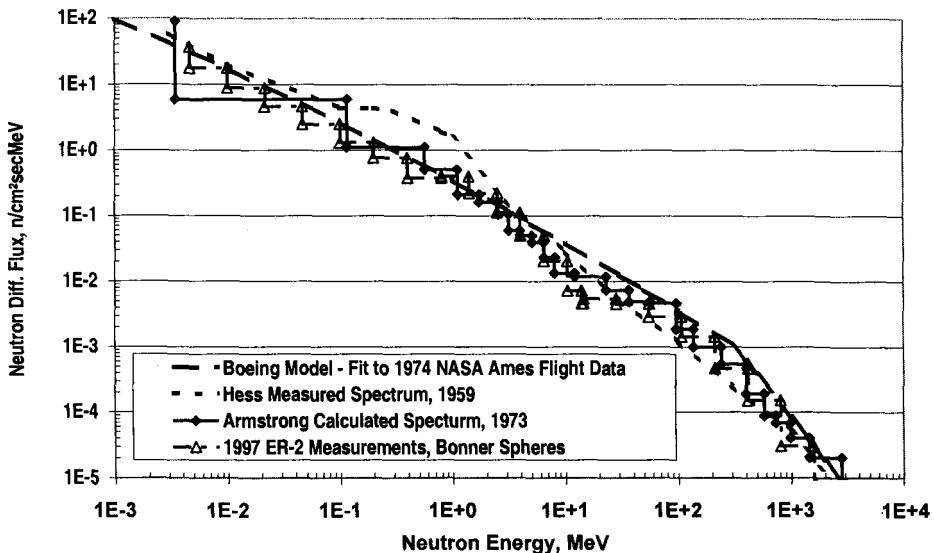


Fig. 1 Energy Spectrum of Atmospheric Neutrons at 40,000 Feet

Models for the altitude and latitude variation of the atmospheric neutron flux have been presented<sup>9</sup> and are still applicable. There are two main models, a simplified Boeing model<sup>38</sup>, and a more accurate NASA model<sup>39</sup> that is currently called AIR. To use the NASA model, a distribution of the vertical rigidity cutoff (a measure of the effect of the earth's magnetic field in deflecting the incoming GCR particles) around the globe is needed. Ref. 3 provides a tabulation of the rigidity cutoff data, and how to interpolate it for any arbitrary point (as function of geographical latitude and longitude).

For energies up to about 500 MeV, the secondary protons in the atmosphere comprise about 25% of the flux of the neutrons, thus the effect of the secondary protons in causing SEE in electronics can be included within SEE rates due to the neutrons since these two particles have very similar SEE cross sections in devices. The energy spectrum and altitude and latitude variations of the proton flux have been given previously<sup>9</sup>. In the atmosphere the pion flux is only a small fraction of the neutron and proton flux and so it can be neglected. More specifically, for energies  $\leq 1$  GeV, the pion/proton ratio is estimated to be  $\sim 0.1$ <sup>34</sup> which applies at both aircraft altitudes and at ground level.

## 5. SEE Data in devices

The key to being able to deal with single event effects in avionics is to quantify the single event effect rate that might be expected in an avionics box. Once an estimate can be made of the event rate, appropriate measures can be considered to accommodate the event. If the event rate is low enough, a decision might be made to ignore it. If it is high enough, a variety of fault tolerant measures can be considered for incorporation, such as error correction and detection (EDAC) or redundancy. SEU, multiple bit upset (MBU, more than one bit being upset at the same time) and single event function interrupt (SEFI, SEU in a complex device such that a control path is corrupted, leading the part to improperly functioning) are the three SEE effects that present the largest potential threat to aircraft avionics. They are listed in order of decreasing likelihood. At a simplified

level, the SEU rate depends on the number of bits in a device, and in most cases the bits serve as memories, registers or latches. The kinds of devices that contain the largest number of bits are random access memories, microprocessors and field programmable gate arrays (FPGAs). When the SEU rate at aircraft altitudes or on the ground is considered on a per bit basis, the SEU rate is similar for these various kinds of devices to within a range of 1-3 orders of magnitude.

The SEU response of a device to a beam of particles is characterized as the SEU cross section, which is the number of upsets divided by the fluence of particles ( $\text{p/cm}^2$ , particle flux integrated over the exposure time) to which the device was exposed. Thus the cross section is given in units of  $\text{cm}^2/\text{device}$  or  $\text{cm}^2/\text{bit}$ . Various scientific and engineering organizations around the world carry out such SEU tests in order to characterize the SEU response of devices to the different particles. The vast majority of these tests are performed for electronics that are being considered for use in space. Therefore, most of the tests are with heavy ion particle beams, and some are with proton beams. A much smaller number are performed using neutron beams for aircraft or ground level applications.

For particle energies  $> 50$  or  $100$  MeV, SEU cross sections measured with protons and neutrons are very similar, and can be taken to be essentially the same, although at lower energies this isn't true. The main difference is that the proton SEU cross sections are measured using monoenergetic proton beams, whereas it is difficult to achieve a beam of neutrons of a single energy. Proton beams are available at a number of high-energy accelerators around the world. The main source available for exposing devices with a simulated atmospheric neutron environment is the WNR facility at LANL. The relationship between WNR SEU cross sections and monoenergetic proton and neutron SEU cross sections has previously been shown for three older SRAMs<sup>20</sup>. It appears the WNR SEU cross section is nearly equal to the monoenergetic proton and neutron SEU cross section for  $E \geq 100$  MeV<sup>20</sup>.

Thus even though the best SEU data is from measurements in the WNR beam, the largest source of SEU data that can be used as a substitute for the WNR SEU cross sections are proton SEU cross sections at  $E > 100$  MeV. Recognizing this, tabulations were compiled in 1997 of SEU cross sections,  $\text{cm}^2/\text{bit}$ , applicable to avionics, that were derived from WNR and proton ( $E > 200$  MeV) measurements for both SRAMs and DRAMs<sup>40</sup>. The conclusion reached is that, based on the data that had been compiled, the SEU susceptibility of both SRAMs and DRAMs has been decreasing over time<sup>40</sup>. For SRAMs the SEU sensitivity was decreasing slowly, but for DRAMs the SEU sensitivity was decreasing much more rapidly.

Because of the usefulness of this compilation (SEU cross section/bit as a function of the date of the device) in understanding trends in the SEU susceptibility, we have updated the two curves for SRAMs and DRAMs. The updating consisted of plotting all of the original data, and then adding data from a variety of more recent sources. The SRAM data is shown in Figure 2. Two fits are shown in the figure, the first is from the original paper and the second is a trend curve derived from SER (Soft Error Rates) for ground level applications<sup>41</sup>. Most of the data appears to be centered around a SEU cross section of  $1\text{E}-13 \text{ cm}^2/\text{bit}$ , but more broadly within a band of a factor of 3-0.33 of this value, thus within the band of  $3\text{E}-14$ - $3\text{E}-13 \text{ cm}^2/\text{bit}$ . The trend curve (transformed from the ground-

level SER data by Ziegler<sup>41</sup> which isn't shown) also exhibits the same tendency, i.e., for most devices there appears to be an asymptotic value of the SEU cross section within the band of  $1E-14$ - $1E-13$  cm<sup>2</sup>/bit.

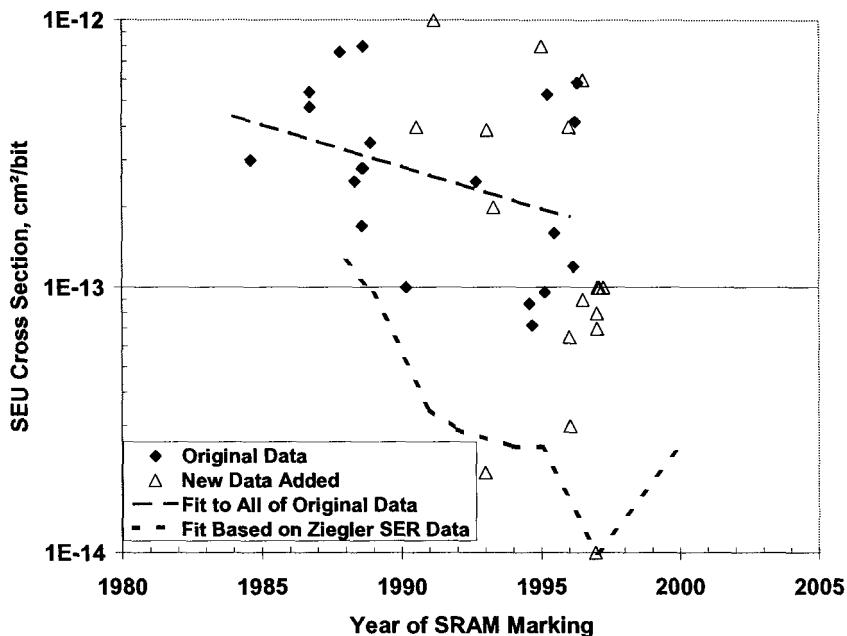


Fig. 2. SEU Cross Section in SRAMs as Function of Manufacture Date

The conclusion regarding the approximate asymptotic behavior of SRAMs over time with respect to their SEU susceptibility from atmospheric neutrons should be treated with caution. It is derived primarily from the data in Figure 2, but there is no way to determine how representative the parts used in the figure are for all SRAMs that may be used in avionics or ground level applications. However, it serves as a useful starting point.

With DRAMs the situation is different. The steep decline of the SEU cross section with year of DRAM production is enhanced by including more recent data. In this case, as microelectronic technologies have been modified to enable individual devices to hold an increasing number of bits, the result for SEU susceptibility is a continuing decline in that susceptibility on a per bit basis. As new capacitor geometries have been implemented, the same capacitance in a smaller chip area, the SEU cross section per bit has decreased. This is seen in Figure 3, which shows the original data (mainly 4Mb and 16Mb DRAMs) along with SEU results from more recent tests<sup>41</sup> (mainly 64-256 Mb DRAMs). It also shows that the stacked capacitance (SC) design used by most DRAM vendors is effective in lowering the SEU susceptibility, but that the more ambitious trench internal capacitance (TIC) design used only by IBM and another vendor, is even more effective.

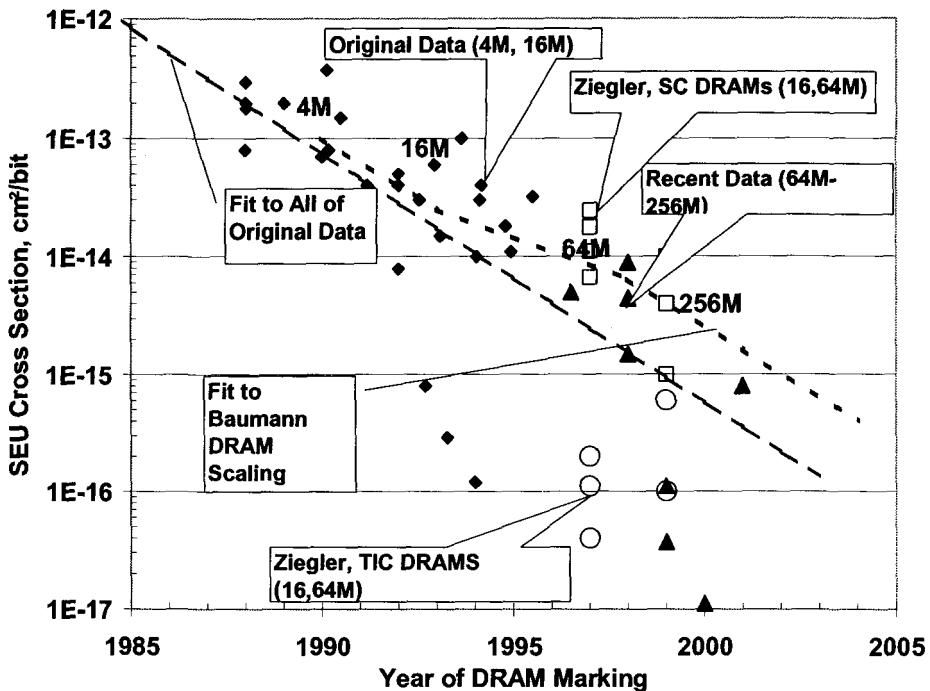


Fig. 3 SEU Cross Section in DRAMs as Function of Manufacture Date

Two trend lines are shown in the Figure 3. One is the original fit to original the data, and the second (Baumann curve<sup>18</sup>) is derived from a trend analysis of other data (SC DRAMs). The slope of the decrease of the SEU cross section with year from the Baumann curve is similar to that from the original data. The main point to be derived from these trend lines is that the SEU per bit cross section has continued to decrease as the size of the DRAM has increased, which appears to be related to the new DRAM technologies that have been developed to achieve the higher density memories.

Independent of the decreasing trend of the SEU cross section per bit in DRAMs as shown in Figure 3, in most applications, the occurrence of SEU in the DRAMs that constitute main memory is protected by EDAC. However, there are also other SEE effects in DRAMs that should be considered, namely their susceptibility to multiple bit upset, stuck bits (single hard errors) and SEFI. The new larger DRAMs appear to be susceptible to these effects, however, the SEE cross sections and therefore the SEE rates are quite low compared to SEU rates.

This review has focused primarily on the SEE response of individual devices, necessarily ignoring system effects which can be very significant. Not all the bits of a device are used in circuit or systems applications, and even for those that are used, if a SEU occurs, it may not affect the operation of the circuit. In addition, fault tolerant measures such as EDAC and various forms of redundancy, can be used to protect overall circuits from SEUs in individual devices. These are issues that need to be dealt with separately.

An alternative to spatial redundancy is *temporal* redundancy in which the same hardware or software elements are used in consecutive operations, using diversity in time to provide results which may be compared using similar comparator/detection, and correction techniques discussed above for spatial redundancy. The technique is dependent upon the requirement for known error-free conditions on the input signals or variables used in the operations; either independent detection and correction must be provided to inputs, or the use of *alternating logic* techniques or *complementing functions* must be utilized to provide tolerance to input signal or variable errors. Alternating logic utilizes a class of boolean functions which are self dual, i.e. they satisfy the property  $f(x_1, x_2, \dots, x_n) = f(x_1, x_2, \dots, x_n)$ . Recomputing with shifted operands (RESO) is applicable to certain problems in which the shifting of inputs forms a complementing function that produces known relationship in outputs that may be utilized in detection and correction.

In older technologies single event transient pulses would not propagate along a path of combinatorial logic gates and the limited clocking frequency reduced the probability of sampling an incorrect logic state during the presence of a transient. The bandwidth of advanced technologies supports propagation of such pulses, and high clock frequencies provide ample opportunity for clocking of errant results into memory elements. The use of static spatial redundancy as a fault tolerance technique for single event upsets in memory elements (latches, flip-flops, and RAM), along with temporal redundancy as a mitigation provision against single event transients in combinatorial logic has been proposed for advanced technology devices.<sup>23</sup> The combined scheme uses temporal triple mode redundancy by sampling the output of combinatorial logic at three different times, storing the individual result in three different latch or flip-flop elements, and majority voting the latched result. By ensuring that the separation between clock edges is greater than the duration of a transient pulse emerging from the combinatorial logic, the transient can corrupt only one of the three values. Majority voting of static triple mode spatial redundancy ensures that upset of individual latches or flip-flops will also be corrected through action of the majority vote logic.

### **3.3 System error detection, containment and recovery**

Whereas the fault detection capabilities of hardware based schemes such as modular redundancy are good, fault detection is the most difficult aspect of fault tolerance to achieve in applications oriented fault tolerance using algorithms, or software based fault detection, due to the elusive nature of the signature of most faults. A fault that results in a fail-stop consequence enables obvious opportunity for detection; most conditions of compromised system state produce signatures that are difficult to discern. Once detection is accomplished, recovery may be as complete and efficient as necessary to restore normal system operation.<sup>24</sup>

The ability to apply software fault tolerance techniques relies on specific properties of the problems being addressed by processor operations and are embodied in the *constraint predicate*. Three defined predicate subclasses formulate the constraint predicate: *progress*, *feasibility*, and *consistency*. The *progress* predicate utilizes the notion that there exist steps in the sequence of process operations and that the decomposition of the process into a finite number of operations blocks provides opportunity for testability at these intermediate points in

the process. The *feasibility* predicate implies constraints that are apparent from the nature of the problem on which the processor is operating. Contained within this notion is the property of boundary conditions as constraints from which to generate a good predicate; testable results must be within the solution space of the problem as defined by the boundary conditions. *Consistency* conditions imply the ability to infer validity in intermediate or final results from input variables and previous intermediate or final process results. Consistency tests are a powerful technique; entire constraint predicates have been developed using only consistency conditions.

### Error Detection

*Application-oriented fault tolerance* is a software solution to the problem of error detection and recovery; the software components are called *assertions*. The application of a set of metrics to a problem specification results in software assertions that may be embedded in the program code; assertions having the form “if not ASSERTION then ERROR”. The extent of error detection is determined by the perceptiveness of the *assertions* to discern a compromised state of program execution. The recovery capability of the fault tolerance provision is determined by the response that is embodied in the *error* branch path. Applications-oriented fault tolerance works on the principle that testing of a program’s intermediate results for conformance to specification ensures that the end result will be within specification, and that if an error does not manifest itself in failure, then the fault is of no consequence or interest.<sup>25</sup>

Several *acceptance test* techniques employed in detecting the presence of faults are *N-version programming*, *self-checking software*, *recovery blocks*, and the *watchdog coprocessor*. *N-version programming* is intended as a provision to detect defects in software design, coding, and integration. Parallel or sequential execution of programs and comparing the results provides opportunity for fault detection, much in the same way as modular redundancy does for hardware fault detection provisions.<sup>26</sup>

The *self-checking software* technique has aspects of functionality, control flow, and data in order to provide error detection. The functional and data aspects examine the reasonableness of the results, and may include an assessment of the input variables in performing acceptance testing of algorithm results. The capability provided by seemingly ad-hoc techniques in assessing the reasonableness of algorithm results is a powerful technique in the detection of computation errors. The control aspect includes checks on the execution flow from entry point to exit points in algorithm blocks, and only valid paths between the algorithm blocks are permitted. One approach to establishing the correctness of high-level control flow uses information (structure labeling) that is embedded in the syntax of the program text. The introduction of path tags to check the validity of the sequencing of blocks and block-tags to verify that execution of blocks proceeded properly from entry to exit points are examples of such structure labels. Each block contains a unique signature, and upon entry the block-tag is set to the value of the signature. The block-tag is verified upon exit from the routine to confirm that the block was not entered in any manner except the valid entry point. The path-tag is then set to the value of the next block signature, which is checked on entry into all blocks. Similar control checking of program iterative execution loops for illegal entry, completion, and branch related loop termination is utilized.

The *recovery block* approach uses acceptance tests in the form of checksums and other bounds checking on computation results to detect the presence of errors. The recovery block notion in this provision is that subsequent executions of the process using the same or different algorithms provide a recovery path from which acceptable results may be generated. The recovery block is a language construct supporting the incorporation of program redundancy into a fault tolerant program. The syntax of recovery block incorporation may take the form: *ensure T by B<sub>1</sub> else by B<sub>2</sub>, . . . else by B<sub>n</sub> else error*. T denotes the acceptance test, B<sub>1</sub> denotes the primary try block, and B<sub>n</sub> denotes the alternate try blocks. The T acceptance test is a logical expression representing the criterion for determining the acceptability of the execution results of the try blocks.<sup>27</sup>

Another attempt at monitoring the behavior of a system is the use of a *watchdog coprocessor*. Most embedded processor systems use a hardware watchdog timer to detect halts to processor execution or errors in program control flow that are detected through failure of the software execution to reset the timer within the prescribed period of time. The watchdog coprocessor extends the notion from the simple hardware timer to the use of an additional processor to check the results of primary on-line processor elements. An active watchdog may implement interaction with the on-line processor as simple as an “I’m OK” message or heartbeat monitor that the watchdog expects to receive within a prescribed window. If not received within the valid window, the watchdog interprets this result that the on-line processor control flow is disrupted and asserts interrupt or reset of the on-line processor. The watchdog may execute concurrently with the on-line processor, or it may operate off-line and pre-compute results for subsequent acceptance testing. It invokes decisions on the integrity of the system based on assertions about the main process, assuming that faults either disrupt program control flow, corrupt database contents, or produce incorrect numerical results.

One specialized application of information redundancy to computational problems is *Algorithm Based Fault Tolerance* (ABFT). In this approach, some attribute of the function being performed is exploited with the use of information or time redundancy to achieve error detection, correction, or recovery. Most ABFT techniques developed to date address computational problems that exhibit structure and regularity which can be exploited to develop informational redundancy, such as matrix computations, sorting, Fast Fourier Transforms (FFT), QR factorization, singular value decomposition, least squares minimization, and other signal processing applications. Although the term “algorithm based” potentially implies a software implementation, these techniques are directly applicable to hardware-based implementation of the algorithms.<sup>28</sup>

#### *Containment of Error Propagation*

To minimize the impact to system operations and the extent of recovery operations, and to enhance the probability of successful system recovery, errors must be confined to the maximum extent possible to the module or subsystem in which the fault occurred. Typically, error containment boundaries are hierarchically defined, with errors confined at the lowest level possible. Containment boundaries can be established by subsystems checking either their own outputs, or by validating all input information. If error detection is activated but error recovery is not supported, the subsystem process is typically halted to prevent error propagation.

### Reconfiguration and Recovery

If an unmasked fault has propagated in a system, a recovery period is needed to correct the system. Most recovery schemes restore system operation to a previous correct state or recovery point. A processor is rolled back to a recovery point by restoring the processor state and key variables to a known good condition, invalidating cache memory (which is likely to have been corrupted by error propagation) and forcing cache data to be restored from protected main memory. A checkpoint is a copy of an application's state that is stored in a protected region of the system. When a failure is detected, the application's state is rolled back to the saved previous checkpoint and execution resumed at that point. Backward error recovery can be defined as the capability of a system to return to a consistent state that existed before it failed; a checkpoint is then defined as a consistent state from which the execution can be restarted.<sup>21</sup>

#### **3.4. Validation and verification of fault tolerance**

Several approaches have been utilized to assess the effects of faults in processor systems and for validating fault handling mechanisms, including analytical modeling, experimental techniques (hardware pin faults, memory corruption, and ion irradiation), simulation modeling (register transfer level, gate level, and op-code level simulation) and fault emulation (memory, bus, and register transfer level). Use of analytical modeling is problematic due to the very large nature of the problem, and the simplifying assumptions that make the analysis tractable are regarded as compromising the usefulness of the technique and the validity of the results. Experimental techniques involve monitoring the behavior of a system while faults are introduced and recording the error detection and correction/recovery performance of the system. This approach requires the use of an accelerating agent to produce sufficient faults to gather statistically valid measurements on the fault tolerant performance of the system. In addition to the ability to quantify fault tolerance, experimental techniques provide the capability to study the consequences of faults that escape detection or are not afforded complete correction or recovery.

Two primary methods have been utilized to perform fault injection: simulation based methods and physical injection provisions. Simulation based methods provide the capability to establish the time of occurrence, location and type of fault, and the transient or permanent characteristics of the fault. Physical injection of faults utilizes charged particles, such as heavy-ion fission fragments from a Californium-252 source, or the use of a heavy ion or proton accelerator to produce single event faults. Most fault injection experiments are not designed around a formalized methodology; designers typically develop customized approaches to validate each system. Complexity of most systems results in the need to perform many experiments to achieve statistical confidence in the validation and verification result. Several simulation based fault injection tools address the need for accelerated fault injection and measurement processes; Messaline, Fiat, Ferrari, Focus, Depend, and React are the ones most discussed in the literature.<sup>29-32</sup>

Validation and verification of system performance utilizes the results of physical and/or simulated fault injection experiments to assess the coverage of faults that produce undesired system response and the ability of detection and recovery provisions to assure proper system operation. These results are utilized in analysis of system performance, often using techniques such as Markov process modeling, to make assertions regarding the fault tolerant performance and availability of the system.

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## RADIATION-TOLERANT DESIGN FOR HIGH PERFORMANCE MIXED-SIGNAL CIRCUITS

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Modern semiconductor processes can provide significant intrinsic hardness against radiation effects in digital and analog circuits. Current design techniques using commercial processes for radiation-tolerant integrated circuits are summarized, with an emphasis on their application in high performance mixed-signal circuits and systems. Examples of “radiation hardened by design” (RHBD) methodologies are illustrated for reducing the vulnerability of circuits and components to total dose, single-event, and dose-rate effects.

**Keywords:** radiation hardened by design; radiation-tolerant integrated circuits; mixed-signal circuit design, silicon-on-insulator processes, silicon-germanium, total dose effects, single event effects, dose rate effects.

### 1. Introduction

The technical advances and economic growth of the commercial semiconductor industry since the late 1960's have resulted in a fundamental transformation in the design of radiation-tolerant analog, digital, and mixed-signal circuits. The end of the Cold War and the exponential growth of the consumer and business markets have dramatically affected the radiation-hardened IC market. The current demand for radiation-hardened integrated circuits is only a tiny fraction of the overall market for high performance commercial mixed-signal circuits and systems, and government funding for radiation-hardened IC process development and support has been slashed. As a result, most semiconductor manufacturers have abandoned the radiation-hardened IC market in favor of the much larger and more profitable commercial market. Few design engineers today can rely on the availability of specialized radiation-hardened IC processes, and those processes that are still available are generally years behind commercial processes in terms of performance.

This situation has led to the development of *radiation hardened by design* (RHBD) techniques, in which designers utilize existing commercial processes for the fabrication of radiation-tolerant mixed-signal circuits and systems. Modern submicron CMOS processes, silicon-on-insulator (SOI) processes, and BiCMOS processes can provide design engineers with significant (and often serendipitous) tolerance to radiation effects in custom integrated circuits. The RHBD philosophy combines this intrinsic radiation tolerance with appropriate

component choices, layout methodologies, and circuit topologies to enhance the radiation tolerance of complex digital and analog systems at the expense of integrated circuit power, area, and/or maximum operating frequency. This paper provides a broad overview of common RHBD methodologies and components for radiation-tolerant integrated circuits, with particular emphasis on the mitigation of single-event and total-dose effects in high performance digital circuits, analog circuits, and mixed-signal systems.

## 2. Radiation Mechanisms in Mixed-Signal Integrated Circuits

Radiation mechanisms in digital and analog circuits are generally divided into three broad categories: *total dose* effects resulting from oxide charge trapping and/or displacement damage induced by  $\gamma$ , proton, or neutron irradiation, *single-event* effects caused by charged particle strikes, and *dose-rate* (*a.k.a.* prompt dose) effects caused by photocurrent generation throughout the entire circuit from very high dose rates over very short time durations. Total dose effects include increased leakage currents, MOSFET threshold voltage shifts, and BJT current gain degradation (resulting in increased base currents). Single-events effects due to charge generation across p-n junctions can result in soft errors, circuit latchup, or component burnout. Dose-rate effects can result in latchup, burnout, or rail-span collapse with resulting data loss. For a design engineer, the relative importance of each of these mechanisms will depend upon the intended application. Integrated circuits for strategic military applications will emphasize immunity to dose-rate effects. Mixed-signal circuits for high altitude aircraft or low earth orbit (LEO) satellites may only require hardening against single-event effects. Circuits for interplanetary probes will require hardening against both total dose and single-event effects.

The intrinsic radiation response of a given IC process will dominate the design of any RHBD circuit. For example, reduced feature size typically results in increased tolerance to total dose effects. Deep submicron CMOS processes have gate oxide thicknesses on the order of 10 Å or less, resulting in relatively little charge trapping. Low to moderate total dose exposure in a 0.13  $\mu\text{m}$  bulk CMOS process may result in negligible effects in most digital circuits, whereas the same exposure amounts in an older 2  $\mu\text{m}$  CMOS process would result in rapid failure of the same circuits. Furthermore, many mitigation techniques that are appropriate for one type of radiation mechanism will have no influence on other mechanisms, or may even exacerbate their effects. Consequently, there is no optimum design methodology for RHBD integrated circuits. Every new design and every new generation of advanced IC processes may require reassessment and modification of existing RHBD techniques.

## 3. Process, Component, and Layout Choices for Hardened-by-Design Circuits

The evolution of semiconductor processes has resulted in a growing emphasis in “system on chip” applications where digital, analog, and even RF circuits are combined together on the same substrate. Circuit designers now have access to three categories of high-performance IC processes that are suitable for mixed-signal RHBD applications. Bulk CMOS, silicon-on-

insulator (SOI), and BiCMOS processes have distinctly different advantages and disadvantages in terms of economics, mixed-signal performance, and radiation response. Deep submicron bulk CMOS processes are widely available, relatively inexpensive, and can provide good inherent immunity to total dose effects provided leakage current paths are eliminated. SOI processes are intrinsically harder than CMOS against single event and prompt dose effects but will still exhibit total dose leakage currents. On the other hand, neither CMOS nor SOI processes will provide optimum low-noise or high-frequency analog circuit performance due to the lack of bipolar transistors. Modern BiCMOS processes combine deep submicron MOSFETs with high-frequency low-noise bipolar (preferably SiGe) transistors, enabling designers to combine analog, digital, and RF circuits on the same substrate. However, BiCMOS processes suffer from the radiation vulnerabilities of CMOS combined with the total dose degradation of bipolar transistors. In general, the inherent single-event immunity of SOI processes has tended to make them more desirable for many applications, but CMOS and BiCMOS processes also remain popular choices for RHBD integrated circuits due to economic constraints or analog performance requirements.

Regardless of the choice of process, the RHBD philosophy dictates that certain types of “rad soft” components and device layouts should be avoided for any design.<sup>1</sup> Components such as pinched resistors, diffused resistors, MOS capacitors, surface Zener diodes, and lateral PNP transistors are inherently vulnerable to radiation effects and should either be replaced with harder components (e.g. poly-poly or poly-metal capacitors instead of MOS capacitors), hardened with appropriate layout techniques (i.e. using a gated lateral PNP transistor), or simply not used at all.

The layout of a component can dramatically affect its radiation response regardless of the process. In some cases the conscientious use of standard commercial layout techniques will improve radiation tolerance. For example, analog and digital circuit designers usually avoid MOSFET transistor layouts with large gate widths (relative to gate lengths) to prevent switching delays due to signal propagation times along the width of the transistor. Instead, folded MOSFET layouts composed of interconnected “fingers” are utilized to provide multiple contacts along each gate and also reduce drain/source capacitances up to 50% via shared diffusions between adjacent fingers. However, sharing drain and source diffusions also reduces charge-collection effects by reducing p-n junction cross-sectional areas.

In other cases, radiation-hardened components require non-standard or extremely conservative layout techniques when compared to commercial designs. For example, leakage currents resulting from total dose exposure can flow between adjacent n-type diffusions in most semiconductor processes. Even in deep submicron IC processes with very thin gate oxides, thicker field oxides will accumulate sufficient trapped charge to create leakage paths as total dose increases. In standard NMOS transistor layouts, this leakage current will flow from drain to source at the edges where the gate polysilicon overlaps the field oxide. As shown in Figure 1, the use of edgeless or re-entrant NMOS layouts ensures that source and drain diffusions are strictly separated by polysilicon over thin oxide, thereby eliminating this leakage path at the cost of increased intrinsic capacitance and layout area.<sup>2</sup> Similarly, leakage currents between n-type diffusions of adjacent NMOS transistors can be controlled by the aggressive use of p-type channel stops or guard rings (structures already available in bulk processes) to interrupt any potential leakage path. The use of guard rings also provides the

additional benefit of preventing latchup due to ion strikes or photocurrent effects in parasitic bipolar structures. However, the extensive use of channel stops and guard rings will require additional layout area for RHBD circuits as compared to standard commercial circuit designs.<sup>2</sup>

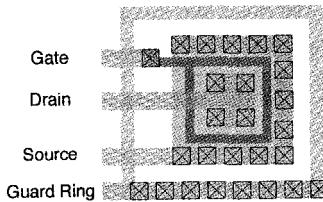


Fig. 1. An edgeless NFET with a rectangular gate layout that eliminates leakage paths between source and drain.

When compared to CMOS and BiCMOS processes, SOI processes provide the advantage of dielectric isolation for individual transistors and the elimination of leakage paths between n-diffusions in adjacent transistors. SOI processes require no guard rings and are inherently immune to CMOS-style latchup mechanisms. This same dielectric isolation also dramatically reduces susceptibility to single event upsets and prompt dose photocurrents by reducing the available p-n junction area for charge collection. In addition, the SOI buried oxide layer limits charge collection in a thin, dielectrically-bounded silicon layer. However, edgeless NMOS transistor layouts and/or body ties are still necessary to eliminate drain-to-source leakage within individual transistors. Body ties are also useful in partially depleted SOI processes to inhibit “single device” latchup due to the parasitic bipolar device present in the source-bulk-drain structure of the SOI MOSFET.<sup>3,4</sup> Finally, SOI MOSFETs can be vulnerable to back-channel leakage, i.e. leakage at the bottom of the channel due to accumulated charge in the buried oxide layer beneath the transistor.<sup>5</sup> Designers of RHBD circuits must ensure that back-channel leakage effects have been characterized or compensated for, as a commercial semiconductor process is typically not created with total dose hardness in mind.

#### 4. Total Dose Hardening

The importance of total dose effects to mixed-signal circuit designers has diminished somewhat as integrated circuit processes have evolved over the past three decades, leading to thinner process layers with fewer defects. For example, SiO<sub>2</sub> layers will tend to trap holes as high-energy photons create hole-electron pairs, and the higher-mobility electrons diffuse out of the oxide. Additional charge traps will also form at defects in silicon-SiO<sub>2</sub> interfaces. As a result, MOSFET threshold voltages will typically exhibit a negative shift with increasing total dose. In the early seventies MOSFET gate oxides were thick and of relatively poor quality, resulting in significant charge trapping and very large threshold voltage ( $V_T$ ) shifts. In a total dose environment NFETs would quickly become depletion mode devices and be impossible to turn off, while PFETs would become impossible to turn on as the magnitude of  $V_{TP}$  grew larger than the magnitude of the power supply voltage.

In contrast, relatively little charge trapping occurs in the very thin, high-quality gate oxides of modern submicron CMOS processes. It has therefore become practical to create digital cell libraries for bulk CMOS technologies that are tolerant of total doses up to several hundred krad [Si].<sup>2,6</sup> These cell libraries utilize edgeless NMOS layouts and guard rings to minimize leakage currents while ignoring the small shifts in  $V_T$ . The use of NAND cells over NOR cells may also be preferable in RHBD digital libraries, as the overall performance of series-connected NFETs and parallel-connected PFETs in NAND arrays will be less affected by small changes in  $V_T$ .<sup>2</sup>

In analog and mixed-signal circuits the situation is somewhat different. In deep submicron processes, MOSFET parameters such as transconductance and intrinsic noise are generally not strongly affected by cumulative total dose.<sup>7</sup> Some transconductance degradation and intrinsic noise increases will be observed in individual transistors, but in modern processes total doses as high as 30 Mrad [SiO<sub>2</sub>] may be tolerated.<sup>8</sup> However, even small parametric changes may lead to failure in circuits such as high-resolution analog-to-digital converters, as these changes can be multiplied by large voltage gains.<sup>9</sup> Unlike digital circuits, analog circuits can also be dramatically affected by shifts in internal bias points due to increasing total dose.

In analog circuits where precise component matching is required, relatively small differences in MOSFET threshold voltage shifts can result in circuit failures.<sup>10</sup> Because total dose effects are bias-dependent, two matched transistors will degrade at different rates if biased at different average voltages. When multiplied by a large voltage gain, increasing radiation-induced offsets between MOSFETs can cause failures in differential amplifiers, comparators, and bias circuits. For example, the cascode amplifier circuit shown in Figure 2(a) uses transistors M2 and M6 to establish a bias current, but the two transistors have different gate-source voltages. In a radiation environment the threshold voltages of M2 and M6 will steadily diverge until input transistor M1 is driven into non-saturated operation. The solution (Figure 2(b)) is to replace M6 with transistors M7 through M11 that operate at identical  $V_{GS}$  values, thereby significantly hardening the entire circuit to changes in  $V_T$ .<sup>10</sup>

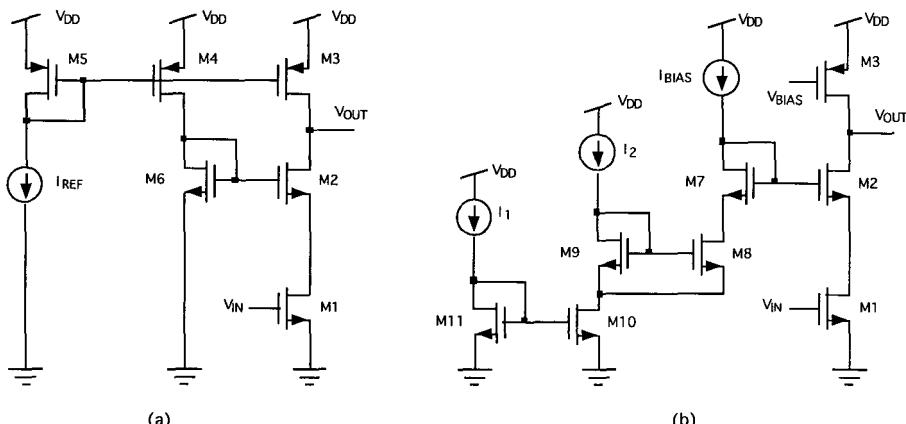


Fig. 2. (a) A standard CMOS bias circuit configuration versus (b) an RHBD configuration with matched  $V_{GS}$  values.

More sophisticated circuit techniques can also be utilized to maintain the functionality of high-performance analog circuits.<sup>10</sup> Switched capacitor circuits can be used to cancel or balance radiation-induced offset voltages in amplifiers and comparators. Charge pump circuits and bulk-source biasing circuits can be used to compensate for changes in threshold voltages in processes where transistor wells can be individually isolated. However, it is important to realize that these techniques usually compensate for the symptoms of total dose degradation at the system or circuit level, rather than reversing or preventing degradation at the component level. As a result, an analog circuit may operate normally until a critical threshold of total dose exposure is reached, at which point the circuit will fail catastrophically as voltage headroom or gain falls below a required minimum value.

Increased total dose in bipolar junction transistors results in increased noise and degraded  $\beta$  (or increased base current). As minority carrier devices, BJTs are also susceptible to displacement damage from proton or neutron irradiation. Circuit techniques such as base current compensation and cascoding can be used to compensate for some of these effects at the cost of increased circuit area or decreased voltage headroom.<sup>1</sup> However, recent experimental results have shown that SiGe heterojunction bipolar transistors can provide far superior total dose tolerance when compared to conventional silicon BJTs.<sup>11</sup> Analog and RF circuits such as bandgap references and voltage controlled oscillators fabricated in a commercial 0.25  $\mu\text{m}$  SiGe BiCMOS process have demonstrated minimal performance degradation at proton fluences as high as  $5 \times 10^7 \text{ p/cm}^2$ .

Some advanced bipolar processes also exhibit enhanced low dose radiation sensitivity (ELDRS) effects, where a given dose at a very low dose rate has a greater cumulative effect than the same dose at higher dose rates.<sup>12</sup> Consequently, a bipolar integrated circuit that is tested at typical laboratory dose rates of 10-100 rad(Si)/s may exhibit far less damage than an identical circuit operating in an actual space environment with a dose rate of 0.01 rad(Si)/s or less. BiCMOS (or bipolar) processes should be carefully characterized for ELDRS effects to accurately predict the performance degradation of mixed-signal circuits in low dose rate environments.

## 5. Single-Event Effect Hardening

The mitigation of single-event effects (SEEs) has taken on growing importance as feature sizes have decreased. Thirty years ago, typical IC feature sizes were on the order of 5 to 10  $\mu\text{m}$ . Today CMOS processes with 0.13  $\mu\text{m}$  gate lengths are commercially available, and manufacturers expect to move to 0.045  $\mu\text{m}$  feature sizes by the year 2010.<sup>13</sup> Hundreds or thousands of transistors operating at frequencies of several GHz can now be placed in the same area once occupied by a single transistor operating at a few MHz, and the same ion energies that had little effect thirty years ago can result in severe voltage transients over multiple circuit nodes today. The use of lightly-doped epitaxial layers in submicron CMOS processes has tended to mitigate single-event effects in digital circuits by reducing charge collection and preventing latchup<sup>14,15</sup>, but shrinking features sizes are now forcing commercial manufacturers to address single-event effects as terrestrial radiation sources become a significant source of soft errors in ground-based applications.

The effect of an ion strike on any given node of a mixed-signal circuit is dictated by the basic capacitance equation

$$\Delta q = C \cdot \Delta V \quad (1)$$

where  $\Delta q$  is the collected charge due to an ion strike,  $C$  is the effective capacitance of the node, and  $\Delta V$  is the resulting change in node voltage. The minimum value of  $C$  has decreased with the square of shrinking feature size while the range of  $\Delta q$  values has remained relatively constant. As a result, the average nodal  $\Delta V$  perturbation has increased in modern processes. In addition, IC power supply voltages have steadily decreased along with feature sizes, making the proportional effect of  $\Delta V$  even greater. Modern circuit topologies that rely upon the temporary storage of charge on a floating capacitor (e.g. DRAM, dynamic logic gates, or switched capacitor circuits) become particularly vulnerable as feature size decreases.<sup>16,17</sup> (It should be noted that total-dose compensation circuits that rely on switched capacitors for error cancellation may also be vulnerable to single-event errors.) In general, circuit-level mitigation techniques for single-event effects must either filter or dissipate the collected charge or provide some form of circuit redundancy to prevent a single event upset from corrupting data.

The operating frequency of a mixed-signal circuit will also determine its susceptibility to single-event effects, as illustrated by the fundamental equation

$$\Delta q = \Delta t \cdot I \quad (2)$$

where  $\Delta t$  is the time needed to dissipate charge from an affected node, and  $I$  is the maximum charging or discharging current available to that node. As the clock frequency of a digital circuit increases, the clock period  $T$  decreases. As  $T$  approaches  $\Delta t$  and then becomes smaller than  $\Delta t$ , the probability of a single event upset propagating through the remainder of the circuit increases. In general, the higher the operating frequency of a circuit, the more likely a single-event effect will result in a significant output transient or soft error, although limited exceptions may occur in some dynamic logic circuits.<sup>16-19</sup>

The principle of *charge dissipation* can be applied to digital or analog circuits to reduce  $\Delta t$  by increasing the maximum charging or discharging current  $I$  at critical nodes.<sup>16</sup> Consider the digital inverter shown in Figure 3, where the logic “high” input voltage turns on the NFET and turns off the PFET. Any charge deposited on the equivalent output capacitance  $C_{OUT}$  must be discharged through the NFET. By increasing the width-to-length ratios of the inverter transistors, the maximum drain current  $I_D$  can be increased so that a net change in capacitor voltage due to an ion strike is dissipated before the subsequent logic stage can propagate the resulting voltage transient as a bit error.<sup>16</sup> Similarly, bias currents in analog circuits can be increased to provide improved charge dissipation and minimize single-event effects in critical analog signal paths. The disadvantages of charge dissipation are the power and area penalties associated with increasing the size and quiescent currents of many of the circuit components.

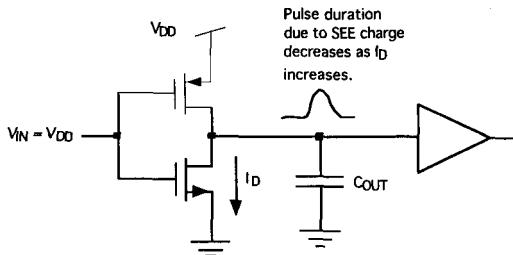


Fig. 3. The principle of charge dissipation as applied to digital circuits.

A related technique for SEE mitigation in mixed-signal circuits is *temporal filtering*.<sup>16</sup> As shown in Figure 4, this method involves adding resistance and/or capacitance at critical circuit nodes to reduce transient response and provide a low-pass filter effect to fast single-event voltage pulses. For example, temporal filtering has been used to harden SRAM cells against soft errors through the addition of resistors in the latch feedback paths.<sup>16</sup> However, the significant area and speed penalties of added resistance and capacitance severely limit the use of temporal filtering in high-performance integrated circuits.

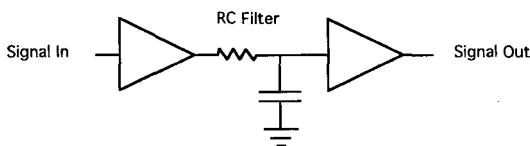


Fig. 4. Temporal (low-pass) filtering to reduce transient response to single-event effects.

In digital circuits, *spatial redundancy* and *temporal redundancy* techniques (or a combination of both) are commonly used to eliminate single-event errors.<sup>16</sup> An example of spatial redundancy is a triple-redundant combinational logic circuit that uses a voting circuit to generate a valid result only if at least two calculations agree. As shown in Figure 5, spatial triple-mode redundancy can be implemented using three physically separated data paths to prevent any single ion strike from upsetting more than one set of logic circuits. Triple-redundant circuits provide excellent SEE immunity at the expense of circuit area, provided the voting circuit is also hardened against errors.

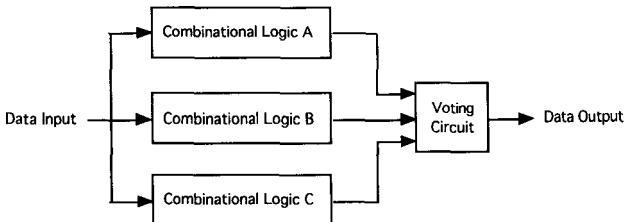


Fig. 5. Spatial triple-mode redundancy in RHBD digital circuits.

Spatial redundancy can also be applied at the gate level through the use of additional transistors, data storage elements, or data paths to ensure that two or more simultaneous SEEs must occur to propagate or store a soft error in a combinational circuit or data latch. The DICE (dual interlocked storage cell)<sup>20</sup> design is a popular example of an SEU-hardened data latch. Spatial redundancy can be applied to CMOS or SOI digital circuits, although some gate-level techniques require that individual MOSFET bulks be isolated from each other.<sup>16,21</sup> Regardless of the application or process, spatially redundant circuits will inevitably require significant area and/or performance penalties. On the other hand, spatial redundancy has no inherent maximum operating frequency.

Just as spatial redundancy can separate identical data signals in space, temporal redundancy separates identical data signals in time in order to filter out single event upsets. Figure 6 shows an SEU-resistant data latch with three separate data paths, a voting circuit, and a 2-input multiplexer connected in a feedback loop.<sup>18</sup> Two of three data paths to the voting circuit incorporate time delays of  $\Delta T$  and  $2\Delta T$ , respectively, where  $\Delta T$  is equal to the time required to dissipate the largest expected charge of an ion strike.

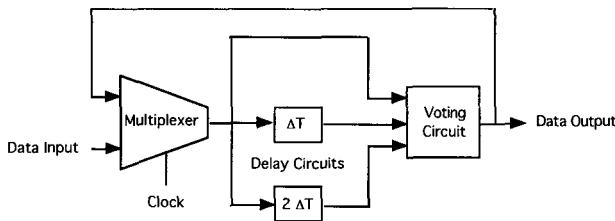


Fig. 6. Triple-path temporal redundancy in an SEU-hardened latch.

The main penalty of temporal redundancy is the inherent latency of waiting  $2\Delta T$  seconds to complete a calculation. At operating frequencies below 50 MHz this latency is relatively small, but as clock speeds increase the delay quickly becomes a significant percentage of the overall latency of the circuit.<sup>18</sup> Given a  $2\Delta T$  value of 200 ps, temporal redundancy techniques will put an upper limit of 2.5 GHz on the maximum operating frequency of any individual signal path or data latch. Operating frequencies in excess of 3 GHz are already common in high-performance microprocessors, so temporal redundancy may prove less useful as even faster commercial processes become available.

Analog and RF circuits provide very different challenges for SEE hardening when compared to digital circuits. Spatial and temporal redundancy techniques are unsuitable for removing transients from analog/RF signal paths, as no practical means of constructing a voting circuit to compare analog outputs has been demonstrated. Furthermore, short-channel effects dictate that most analog MOS transistors cannot take advantage of deep submicron gate lengths.<sup>22</sup> Charge dissipation or temporal filtering techniques combined with appropriate component layouts may be the only practical alternatives. In addition, the choice of circuit topology can dramatically affect an analog circuit's response to single event transients. For example, cascode circuit configurations can increase voltage gain and small-signal output resistance at the expense of reduced voltage overhead. However, that reduced voltage overhead may result in much longer recovery times if transistors are more easily forced into

undesired operating regions by an ion strike.<sup>1</sup> It should also be noted that some mixed-signal circuit topologies are inherently immune to single-event effects. For example, oversampled data converter topologies such as sigma-delta A/D converters are resistant to single-event effects in the analog front end, since any SETs will simply be converted into out-of-band noise by the oversampling process.<sup>23</sup>

At the system level, RHBD circuit designers should keep in mind that few circuits or signal paths are equally affected by single-event effects in digital or analog circuits. Some circuit nodes will be SEE-insensitive due to their intrinsic capacitance or resistance, and some signal paths may be blocked or attenuated in such a way that SEEs do not propagate and become latched as data errors.<sup>16</sup> On the other hand, single-event effects in global signals such as clocks, bias voltages, and reference voltages can create errors throughout the entire system. A careful analysis to identify the most critical nodes or signal paths, and to selectively harden them, can result in significant improvements in radiation hardness while minimizing layout, power, and speed penalties for the overall system.

Another concern for the designer is the occurrence of single-event latchup in SOI integrated circuits. SOI processes are not subject to the destructive power supply rail-to-rail latchup effects of CMOS and BiCMOS processes, but they can suffer from localized latchup effects (i.e. single event snapback) where a low resistance path forms between the drain and source of a single SOI MOSFET.<sup>3,4</sup> Although the current levels are generally not immediately destructive, device burnout may eventually occur if the latchup is not reversed.<sup>27</sup> In such cases the only remedy may be to cycle the power of the affected circuit to restore the transistor to normal operation. Consequently, a radiation-tolerant SOI circuit may require the inclusion of a robust power reset function<sup>24</sup> to ensure that a single-event latchup does not render a remotely operated satellite or sensor permanently inoperative. It should also be noted that the use of body ties can reduce or eliminate single event snapback, but at the cost of layout area.

## 6. Dose-Rate Effect Hardening

Of the three categories of radiation effects, relatively little information is available in the open literature concerning the modeling and mitigation of dose-rate effects due to the strategic defense applications of circuits that typically encounter this phenomenon. Furthermore, the design of dose-rate hardened circuits generally requires good simulation tools and device models in order to obtain satisfactory model-to-hardware correlation. However, some general design principles are commonly utilized to prevent certain types of circuit failure in dose-rate environments. For example, *rail span collapse* is a dose-rate failure mechanism caused by the simultaneous generation of photocurrents throughout an integrated circuit.<sup>25</sup> As shown in Figure 7, these currents result in large transient voltage drops across the power supply and ground rails. At the very ends of the rails the voltage drops can be so large that the power supply voltage falls below  $V_T$  over a portion of the circuit, leading to complete signal or data loss. Rail span collapse can be avoided by widening and distributing power supply rails so as to minimize these voltage drops over any given portion of the integrated circuit.

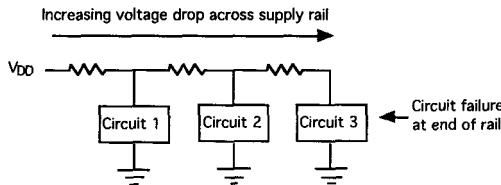


Fig. 7. Rail span collapse results from voltage drops caused by prompt dose photocurrents throughout an IC.

Even if rail span collapse is avoided, dose-rate photocurrents can still result in large transient voltage pulses at circuit nodes connected to reverse-biased *p-n* junctions. In digital circuits such pulses may be large enough to change the values of stored bits in data registers. In many cases the technique of *photocurrent compensation* is applied to such critical circuit nodes. By balancing the total photocurrent entering a node with the total photocurrent exiting a node, the net perturbation at the node is minimized, but at the cost of increased circuit area and increased transient currents flowing between the power supply rails. Figure 8 illustrates a photocurrent compensation technique using dummy devices created using bipolar transistors.<sup>26</sup> If transistor Q1 and the dummy transistor have identical geometries, the induced collector-base photocurrent of Q1 will be equal to the collector-base photocurrent of the dummy transistor, resulting in a net current change of zero for the base node of Q1.

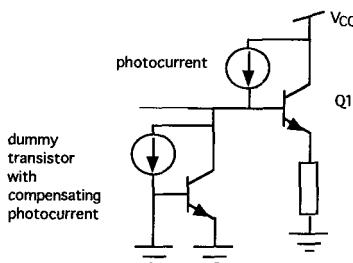


Fig. 8. Dummy transistors can be used to provide photocurrent compensation.

Photocurrent compensation can also be accomplished in CMOS and partially depleted SOI processes by carefully balancing the cross-sectional areas of the reverse-biased drain-bulk and source-bulk junctions for all NFET and PFET transistors connected to a given node. Again, the goal of this technique is to balance all currents entering or exiting a node, and thereby minimize the voltage transient. The drawback of this approach is that it may require undersizing PFET width-to-length ratios compared to NFET width-to-length ratios, resulting in unbalanced transient rise and fall times.

## 7. Conclusion

Unless current trends in semiconductor manufacturing and government funding change dramatically, the philosophy of “radiation hardening by design” will almost certainly grow in

importance for mixed-signal integrated circuit design as IC feature sizes move to 0.09  $\mu\text{m}$  and below. RHBD circuits inevitably require penalties in power, area, or speed when compared to commercial applications, but the use of commercial IC processes will allow design engineers to maintain acceptable performance differentials rather than be left behind by the relentless march of Moore's Law. The overall performance/cost ratio of an RHBD circuit will not match that of a commercial design, but an RHBD circuit fabricated in a commercial IC process can still provide improved speed and functionality in a smaller die area when compared to a circuit fabricated using a specialized radiation-hardened IC process that is one or more generations behind commercial processes in terms of feature size and performance.<sup>6</sup>

Furthermore, help may be on the horizon for RHBD designers in terms of the mitigation of single-event effects. As feature sizes shrink, semiconductor manufacturers must inevitably resolve the issue of soft errors resulting from terrestrial radiation sources. Given the area and speed penalties of spatial and temporal redundancy, manufacturers will have an enormous financial incentive to either intrinsically harden commercial processes against single-event effects or develop new circuit techniques to mitigate their effects with minimal performance penalties. Consequently, the primary focus of future RHBD research may shift to dose-rate hardening over the next decade, with significant total-dose and single-event hardening intrinsically provided by commercial processes and/or automatically incorporated into analog and digital circuits using standard computer-aided design tools.

In the longer term (20 to 30 years) the future of RHBD methodologies is not so clear. Eventually digital components will shrink to molecular or atomic scale, and individual proton, neutron, or ion strikes may not degrade, but rather destroy individual transistors or entire subcircuits. Barring the introduction of new shielding or packaging technologies, some form of dynamic self-repair or reconfiguration of complex digital circuits will be needed. Again, the need to improve manufacturing yields and prevent operational failures will probably force commercial manufacturers to take the lead in solving these problems.

In addition, there is currently no indication that analog and RF circuits will be able to take advantage of the same components and processes that digital circuits will eventually use. The need for high transconductance, low 1/f noise, and high output resistance already puts severe limits on the minimum gate lengths of MOS transistors used in analog circuits.<sup>22</sup> Even today, an analog circuit with a few hundred components may require more chip area than a digital circuit with millions of transistors. Analog and RF circuits may not be compatible or even possible in digital processes employing proposed exotic components such as fullerene molecules, quantum dots, or biological proteins as computational elements. Consequently, future RHBD techniques may evolve in two divergent directions, with analog and digital designers required to work in completely different IC technologies and employ fundamentally different RHBD techniques to implement mixed-signal systems.

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## A TOTAL-DOSE HARDENING-BY-DESIGN APPROACH FOR HIGH-SPEED MIXED-SIGNAL CMOS INTEGRATED CIRCUITS

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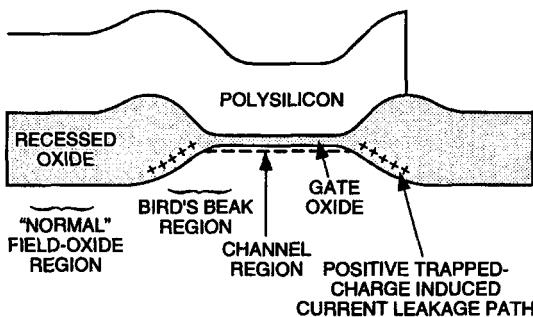
This paper describes design choices and tradeoffs made when designing total-dose hardness into an advanced CMOS integrated circuit. Closed geometry transistors are described and compared, emphasizing their radiation tolerant performance. Speed and area tradeoffs incurred in circuit design when using such closed geometry transistors are illustrated in the design of an advanced IEEE 1394 cable physical layer mixed-signal interface chip.

**Keywords:** Total-dose, CMOS design, radiation hardening, closed-geometry transistors, mixed-signal.

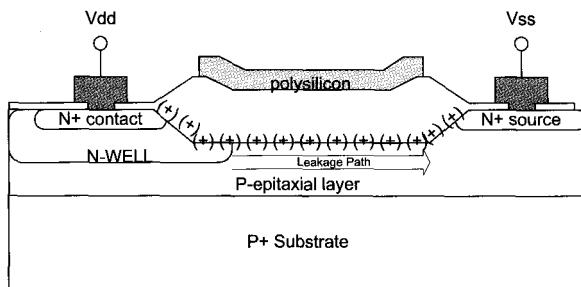
### 1. Introduction

Total ionizing dose can result in degradation in microcircuit performance (increased propagation delay times, lower maximum clock rates, reduced output drive, lower noise margins, increased leakage, and catastrophic failure). Radiation hardened parts can be achieved by identifying the mechanisms responsible for radiation effects in microcircuits and implementing electrical and layout design solutions to minimize them. These solutions must be consistent with typical semiconductor processing so that resulting microcircuits can be fabricated in commercial foundries. This approach trades off area and circuit density for radiation hardness.

In a typical CMOS fabrication process, as illustrated in Figure 1, the transition between the isolation or field oxide and the thin, gate oxide produces a parasitic transistor that is susceptible to total ionizing dose effects.<sup>1</sup> The silicon dioxide in this region



**Figure 1.** MOS transistor cross section (McLean and Oldham, 1987).<sup>1</sup> The current leakage path is perpendicular to the plane of the page.



**Figure 2.** N-well to n<sup>+</sup> source leakage path (Mavis and Alexander, 1997).<sup>2</sup> The positive charges induced in the field oxide by total ionizing radiation are indicated by (+)-symbols.

(known as the bird's beak) is under mechanical stress produced by the dynamics of the oxide growth process and the transition from thin to thick oxide. In this transition region, the oxide is of variable thickness and experiences a relatively high electric field from the combination of polysilicon gate bias and the fringing fields from the source-to-drain bias. When this region is exposed to ionizing radiation, significant hole trapping occurs so that edge leakage currents will appear at the device terminals. At increasing doses, more of the edge parasitic transistor will become involved in the conduction path, and the leakage will quickly rise to become roughly equivalent to the on-state current of the intrinsic transistor. Edge leakage effects are typically manifested as a rapid increase in supply current with increasing total dose, as the parasitic edge transistors shunt the source-to-drain current around the intrinsic transistor. They may also produce functional failure as the composite N-channel becomes permanently "on".

Another total-ionizing-dose-induced leakage mechanism is associated with the field oxide (FOX) that provides isolation between adjacent transistors. An illustration of the structure of the parasitic FOX transistor is shown in Figure 2.<sup>2</sup> The leakage paths are formed when positive charge is trapped in the field oxide and inverts the surface of the P-type material.<sup>3</sup> Two types of leakage paths are possible. The first is between the n-well (typically connected to the positive power supply, V<sub>DD</sub>), and an n<sup>+</sup> source (typically connected to ground or the negative supply, V<sub>SS</sub>). The leakage path connects V<sub>DD</sub> to V<sub>SS</sub>, producing a change in supply current with increasing radiation. Second, field oxide leakage paths can also span the n<sup>+</sup> source/drain regions between adjacent N-channel transistors. This will also increase the V<sub>DD</sub> to V<sub>SS</sub> leakage current.<sup>2</sup>

Typical designs of integrated circuits (ICs) hardened against total-dose radiation use closed-geometry NMOS transistors and guard rings to eliminate the radiation-induced leakage currents.<sup>2,4-10</sup> While the guard rings also aid in hardening ICs against heavy-ion-induced single-event latchup, other circuit techniques, outside the scope of this paper, are sometimes employed to further harden designs against single-event effects.<sup>12,13</sup> These radiation hardening layout and design techniques introduce design penalties in area and speed.<sup>6</sup> This paper compares the total-dose tolerance of closed-geometry transistors and illustrates the speed and area tradeoffs encountered in advanced CMOS processes. The design of an IEEE 1394 cable physical layer mixed-signal interface chip using closed-geometry transistors is described and further illuminates some of the performance tradeoffs encountered in hardening by design.

## 2. Closed Geometry Transistors

There are two basic layout configurations for closed-geometry transistors. The first design is called variously annular, re-entrant, or edgeless. Sometimes, it is referred to by the shape of the gate, as a circular, square, rectangular, or octagonal gate transistor.<sup>8,9</sup> A typical structure is shown in Figure 3 and illustrates how the gate polysilicon layer forms a ring around the transistor drain node. Conventional “two-edged” NMOS transistors are susceptible to radiation-induced leakage currents along the active diffusion edges between the source and drain.<sup>1,11</sup> This design has no active diffusion edges overlapped by polysilicon that separates the source from the drain (as implied in Figure 1), and it is therefore free of such leakage currents. The selection of source or drain as the internal, enclosed node is left as a design choice. The usual choice is to place the drain on the inside, since this minimizes the drain area and thus the drain-to-substrate capacitance. However, the electric field density has a  $1/r$ -like dependence.<sup>8,9</sup> Therefore, the selection of drain as the internal node can introduce excessively high fields and be a potential reliability problem.<sup>7</sup> For this reason, when the process design rules allow, 90-degree inside corners are usually avoided, and these annular transistors will have the corners beveled at 45 degrees, as shown. This layout also has limitations in terms of minimum effective width W (limited by contact size and space requirements), maximum channel length L (L and W are not independent, due to the radial nature of conduction), and current handling capability of the enclosed contacts (adding more contacts increases W which increases drain current which may in turn require more contacts). Note too, this device is characterized by an effective device width defined by a geometric combination of inner and outer perimeters (effective radii).<sup>8,9</sup>

The second type of closed geometry transistor may be called ringed-source and is illustrated in Figure 4. In this case, rather than being radial, the channel is more nearly transverse as in a standard two-edged transistor. Here the polysilicon overlaps the active diffusion around the source to eliminate the radiation-induced source-to-drain leakage path (the  $n^+$  source diffusion is now not adjacent to the field oxide edge). Now W can be made smaller than in the annular case, there is no limit for L, and contacts can be added as needed to carry the current without increasing W (by extending the source away from the channel). However, there is now a large parasitic MOS gate-to-source capacitance due to the excess polysilicon that encloses the source. This parasitic gate still inverts the surface, but it does not contribute significantly to drain current. This excess polysilicon can also have significant resistance associated with it, especially in large devices. Again, the designer has the option of enclosing either the drain or the source, and sometimes for compactness, stacked transistors may alternate between enclosed drains and enclosed sources. In this case, when the drain is enclosed, the parasitic gate-to-drain capacitance of the excess polysilicon (absent in the annular transistor) appears as a Miller capacitance when referred to the input. The combination of Miller capacitance (excess parasitic capacitance multiplied by the gain of the transistor) and the excess polysilicon resistance in large transistors can introduce a significant RC delay into a circuit. For this reason, the usual choice is to enclose the source. In addition, these transistors are best used as small width (W) devices.

A feature common to both designs is the ring of  $p^+$  diffusion that encloses each transistor. This ring has an important dual role, as a channel stop and a guard ring. As a channel stop, it isolates adjacent NMOS transistors, interrupting the possible inversion layer that can be induced by the total-dose in  $p^-$  regions under the field or shallow trench oxides (Figure 2). It also eliminates the  $n$ -well-to- $n^+$ -source leakage path of Figure 2. As

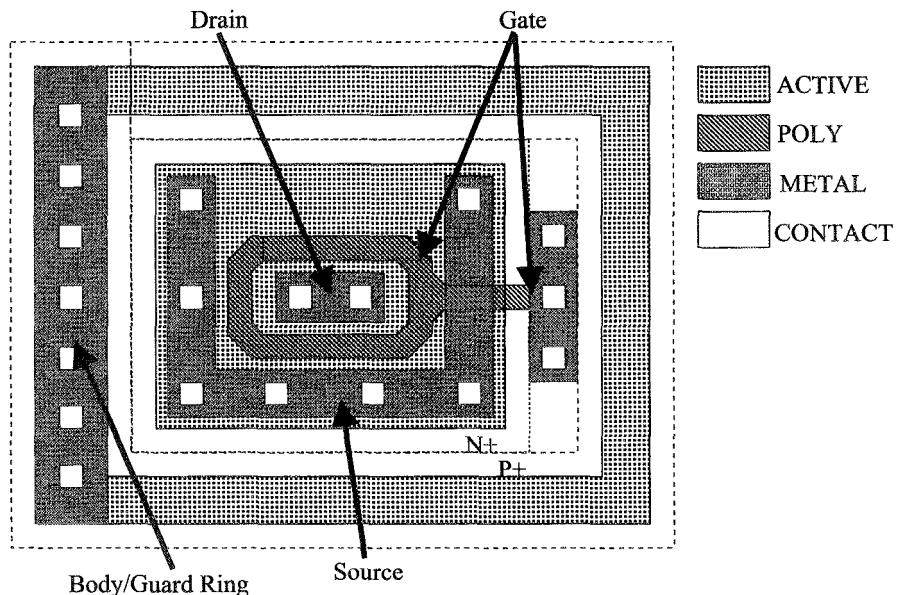


Figure 3. Annular Closed-Geometry NMOS Transistor Layout.

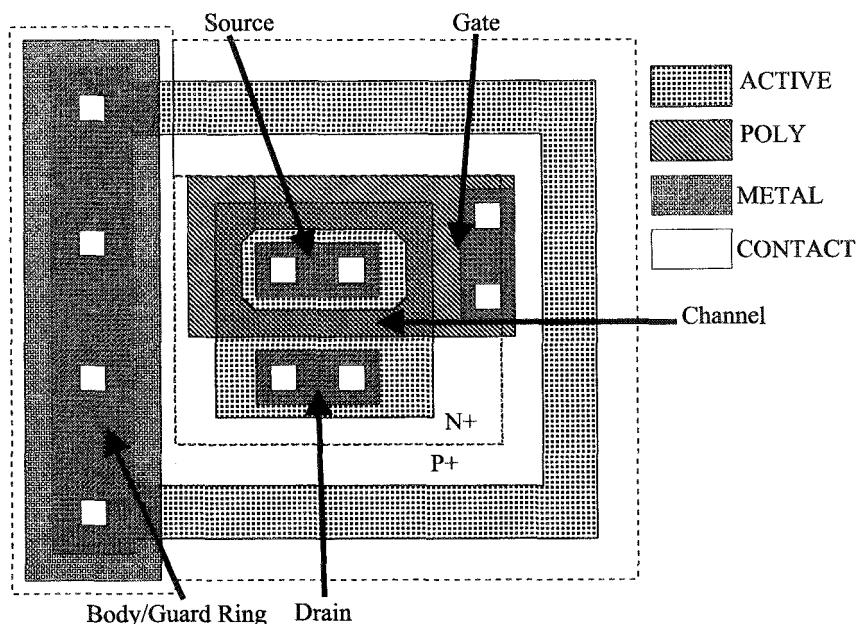


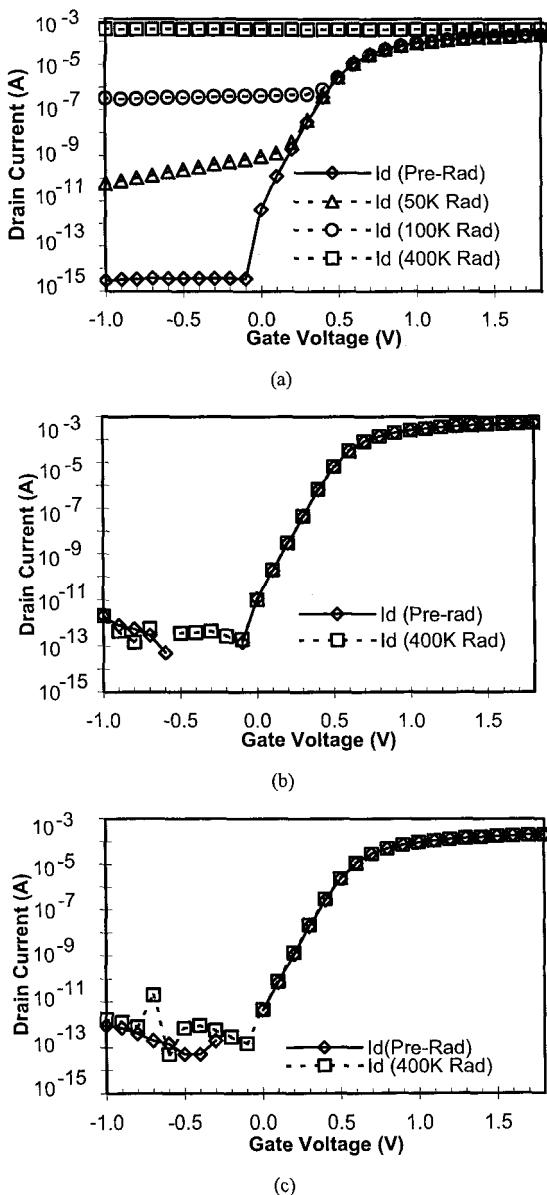
Figure 4. Ringed-Source NMOS Transistor Layout.

a guard ring, it maintains the well or substrate bias (depending on process) through the low resistance p<sup>+</sup> diffusion. This prevents latch-up of the four-layer structures that exist between adjacent NMOS and PMOS transistors. Design hardening approaches may also enclose PMOS transistors in n<sup>+</sup> guard rings to maintain uniform bias in the n<sup>-</sup> regions and further protect against latch-up.

We have designed, fabricated, and tested sets of annular and ringed-source transistors in several different modern commercial foundry processes ranging from 0.6μm to 0.18μm feature sizes. These transistors have been tested for their total-dose radiation tolerance, and in all processes, we have observed hardness levels significantly above conventional two-edged NMOS transistors. Examples of the total-dose hardness of these transistors are illustrated in Figure 5 for the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18μm process. The devices, fabricated in early 2002, were irradiated with 50keV x-rays at a dose rate of 165rad(SiO<sub>2</sub>)/s. The drain current as a function of gate voltage (drain voltage constant at 0.1V) is shown for pre-irradiation and post-irradiation measurements of (a) a conventional two-edged NMOS (W/L=1.2/0.2), (b) an annular transistor (W/L≈3.8/0.2), and (c) a ringed-source transistor (W/L≈1.2/0.2). The widths of the closed-geometry transistors are approximated as the average of the inside and outside edge perimeters of the channels and represent the minimum achievable transistor dimensions in the process technology. Notice the minimum annular transistor has a W/L nearly three times larger than the minimum ringed-source transistor. This is confirmed by observing the saturation drain current in Figure 5(b) is nearly three times larger than in Figure 5(c). Also, the approximation for W of the ringed-source transistor is reasonably accurate since the pre-irradiation saturation drain current is nearly the same as that for the two-edged transistor. This also validates the assumption that the excess (ring) polysilicon does not contribute to drain current.

The effects of total-dose are clearly seen in the two-edged transistor (Figure 5(a)) where significant leakage current is observed at 50krad(SiO<sub>2</sub>) and the device is completely shorted out at 400krad(SiO<sub>2</sub>). The closed-geometry transistors show no increased leakage current even after 400krad(SiO<sub>2</sub>). Other authors have reported total-dose results of two-edged transistors in the commercial TSMC 0.18μm process showing higher levels of hardness.<sup>14</sup> These other data are taken from lots run at different times in the process history of a commercial process that is not controlled for its total-ionizing-dose hardness levels. This illustrates an additional advantage of design hardening. Radiation hardening by design depends only weakly on the natural or intrinsic process hardness, which may vary significantly with process changes or random variations.

The use of these transistors in the design of a digital library design element, such as a two-input NOR gate, is illustrated in Figure 6. Four gate designs are shown using (from left to right) annular transistors, ringed-source transistors, and conventional two-edged transistors for both a 0.18μm and a 0.25μm process. The annular-transistor gate design conservatively uses a guard ring around the PMOS, but this is eliminated in the ring-source design to achieve more aggressive design scaling. In addition, the annular design does not employ 45-degree inside gate corners so that it can be easily used in processes where such poly beveling is forbidden by design rule. While these 0.18μm Hardened-By-Design (HBD) gates are 25-50% larger in area than the standard (two-edged) cell in the same technology, they are smaller in area than the standard cell in the 0.25μm technology. Commercial designs in a given process can therefore be realized as design-hardened versions in about the same silicon area using the next-generation process technology.



**Figure 5.** Total-dose response of a conventional, two-edged transistor (a), an annular transistor (b), and a ringed-source transistor (c). Bias conditions during irradiation:  $VG=VDD=1.8V$ ;  $VS=VD=VB=VSS=GND$ . 50keV x-rays at 165rad( $\text{SiO}_2$ )/s. Doses are given in krad( $\text{SiO}_2$ ).

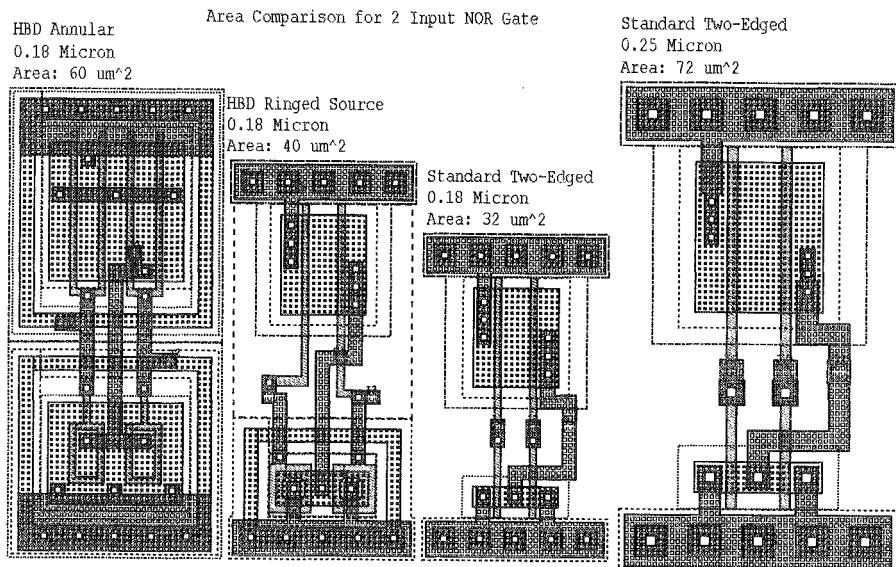


Figure 6. HBD Area Comparison for a Two-Input NOR Gate.

### 3. Circuit Application—Functional Description

We have recently used these transistors together with Dual Interlocked storage CEll (DICE) latches<sup>12</sup> to design a total-dose tolerant and SEU (Single Event Upset) immune version of an IEEE 1394 Cable PHysical Layer (CPHY) interface chip. The design was actually the mixed-signal portion, designated APHY (for the Analog functions of the PHysical Layer). We used the annular transistors in the high-speed digital portions of the chip (latches, registers, encode and decode logic). For the digital block, area was not critical, but speed was (the ringed-source transistors switch slower than the annular transistors due to their added capacitance). The analog portions of the design were implemented using the ringed-source transistors to minimize area. Our design was a three-port implementation operating at 100MB/s. This was a 5V part designed to withstand total ionizing dose radiation in excess of 300krad(SiO<sub>2</sub>). It was fabricated through MOSIS in the AMI Semiconductor (AMIS) C5N 0.5μm commercial process. The design was achieved in a 3.6mm×4.9mm area with 96 I/O pads. A die photograph of the chip is shown in Figure 7.

A functional block diagram of the APHY chip is shown in Figure 8. The Analog Block interfaces directly with the channels (TPA/TPB) on the physical cable and uses comparators and transceivers to sense and transmit the encoded data stream. These analog circuits are differential drivers for sending data on the cable, differential receivers for receiving data on the cable, a sub-circuit for generating cable bias current, and comparators for arbitration signals and cable connect detect. The Phase Locked Loop (PLL) uses a 24.576MHz crystal input to generate the internal 98.304MHz clock. Digital

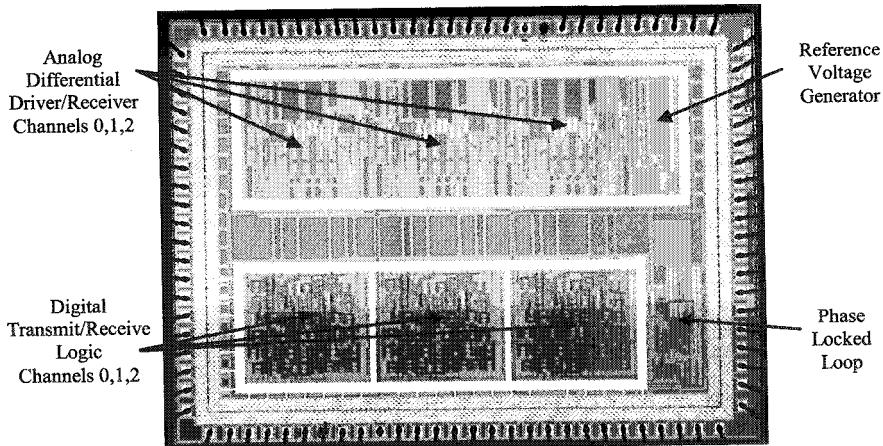


Figure 7. 1394 APHY Die Photograph.

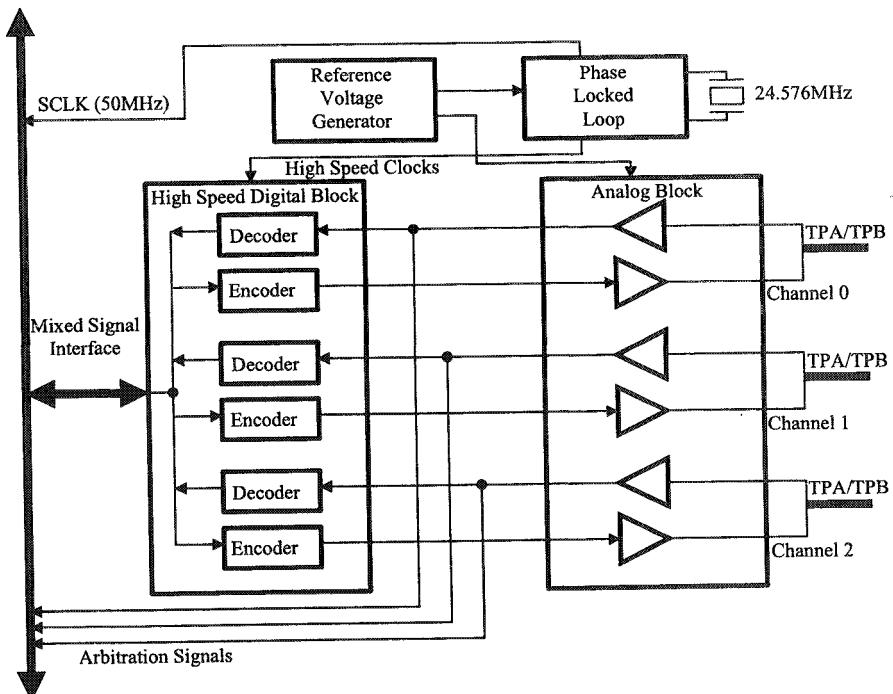


Figure 8. IEEE 1394 Analog PHYSical layer (APHY) Functional Block Diagram.

logic is then used to create the internal 49.152MHz clock and a SCLK output for the DPHY (the Digital portion of the CPHY). The reference voltage generator feeds the reference voltage to the PLL and the differential drivers and cable bias generator in the analog block. The High-Speed Digital Block decodes the received data or encodes the data to be transmitted. Registers latch the data and store it for communication to the Mixed Signal Interface. The Encoder encodes the 2-bit digital data stream from the DPHY to create the digital inputs for the analog block. Next, the Decoder sub-circuit receives data from the analog block, decodes it and synchronizes the data to the internal 49.152MHz clock (3 instances, one for each of the three ports).

#### 4. Performance of HBD APHY Circuit

The key performance challenge in the design of the APHY circuit was in the phase-locked loop. Achieving the target voltage-controlled oscillator (VCO) maximum frequency was strongly dependent on the type of transistor used and which node was enclosed. Figure 9 shows the circuit schematic for the VCO. The NMOS stacks of MN5-MN7 and MN6-MN8 were initially realized using ringed-drain transistors for layout convenience (the drain was enclosed by the polysilicon, rather than the source). These transistors were drawn large ( $W=75\mu m$  for MN7 and MN8 and  $W=150\mu m$  for MN5 and MN6) to reduce single-event-upset effects in the VCO by increasing the node capacitance (this increases the critical charge required in an ion strike to upset or change the node voltage state).<sup>4,13</sup> Figure 10 shows simulation results for three different cases of VCO performance. The top trace shows the result when standard device models are used for the ringed-source (ringed-drain) transistors in the VCO. The maximum oscillator frequency was 177MHz in this case. However, when the parasitic components (R and C) of the excess polysilicon are included as suggested by the model of Figure 11, the maximum VCO frequency drops to 90MHz. Measurements of the VCO with this design also showed a 90MHz maximum oscillator frequency. This was observed by noting the maximum frequency at which the PLL would maintain lock. The model of Figure 11 includes the polysilicon resistance in series with the excess gate capacitance, modeled as the voltage dependent capacitance of a MOS capacitor between the gate and the source. The parameters for these parasitic elements are computed on the basis of the active area under the polysilicon, thus the parasitic elements will have values differing from the elements of the active transistor. Now, when the parasitic MOS capacitor appears in the drain as in MN5, MN6, MN7 or MN8, for example, the RC delay of these parasitic components is significant. Redesigning the VCO circuit to replace the ringed-drain transistors with annular transistors (without the parasitic Miller capacitance) restored the maximum oscillator frequency to 162MHz (even with the RC parasitic components included in the models of all other ringed-source transistors). This is shown in the bottom trace of Figure 10. These results illustrate the potential speed tradeoffs that may be encountered in total-dose hardening a design and suggest the feasibility of attaining both the speed and radiation tolerance requirements in an advanced IC.

#### 5. Conclusions

We have demonstrated the feasibility of realizing advanced, high-speed digital and analog functions in a monolithic integrated circuit using radiation-hardened-by-design techniques. The area penalties were not prohibitive and speed penalties were readily overcome by an appropriate application of closed-geometry transistors. It was seen that

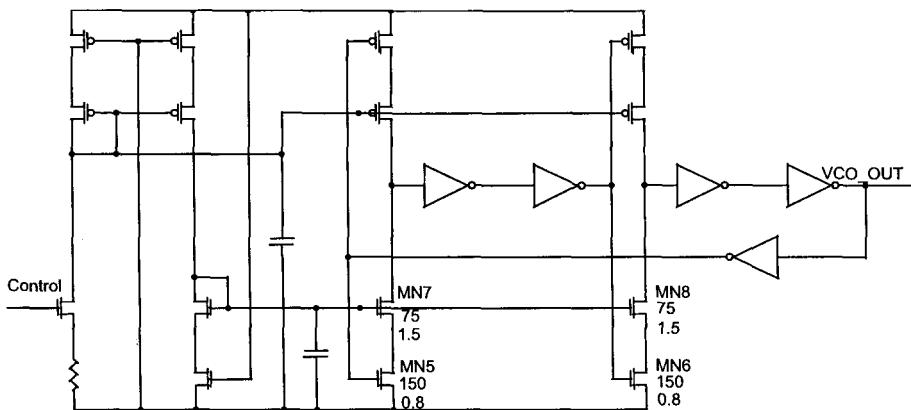


Figure 9. Schematic of VCO.

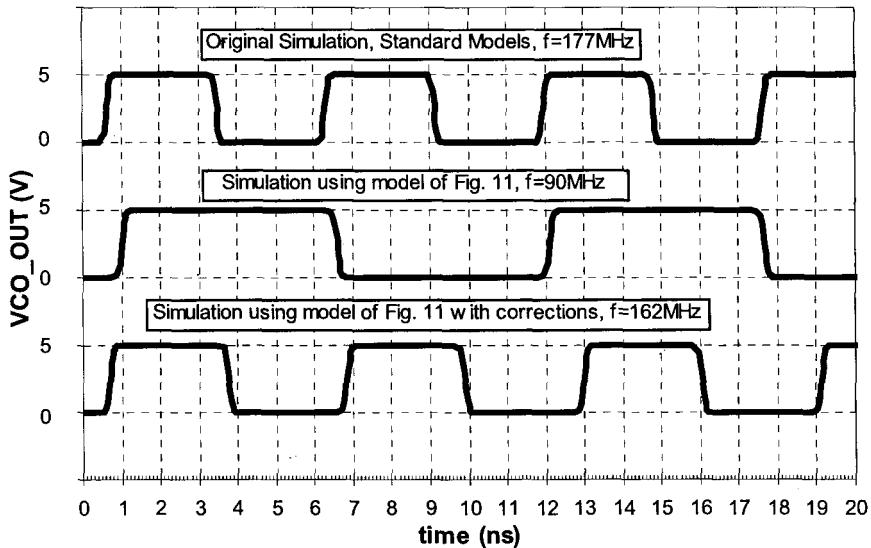


Figure 10. Simulated VCO Output Voltage showing impact of hardened by design techniques.

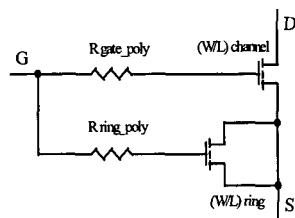


Figure 11. Possible model for simulating effects of ringed-source parasitic components.

parasitic polysilicon resistance could play a significant role in degrading circuit performance, especially if coupled with the Miller-effect multiplication of the parasitic gate-to-drain capacitance.

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## RADIATION ISSUES IN THE NEW GENERATION OF HIGH ENERGY PHYSICS EXPERIMENTS

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**Abstract**—With the construction of the Large Hadron Collider at the European Center for Nuclear Research (CERN), the radiation levels at large High Energy Physics (HEP) experiments are significantly increased with respect to past experience. The approach the HEP community is using to ensure radiation tolerance of the electronics installed in these new generation experiments is described. Particular attention is devoted to developments that led to original work: the estimate of the SEU rate in the complex LHC radiation environment and the use of hardness by design techniques to achieve radiation hardness of ASICs in a commercial CMOS technology.

Keywords—radiation effects, enclosed layout transistors, radiation tolerance, SEU estimate

### 1. Introduction

The increasing use of embedded electronics components together with the increase in particle energy and beam intensity render the new generation of High Energy Physics (HEP) experiments considerably more vulnerable to radiation effects. In this respect, as in many others related to size and complexity, the most demanding example in the HEP community is the Large Hadron Collider (LHC) with its giant experiments. The LHC is the new particle collider that is being constructed at the European Center for Nuclear Research (CERN) located in Geneva, Switzerland. Scheduled to become operational in 2007 this circular machine with a radius of 4.3 km will accelerate bunches of protons up to 7 TeV and collide them head-on in the center of large detector systems built with different technologies to measure the tracks and energies of the various collision products.

Particle collisions at such energy are expected to produce momentarily conditions that allow physicists to progress in the understanding of the deepest structure of matter, but this happens with such a low probability that a very large number of collisions is required to observe a few such interesting events. The vast majority of such collisions will not be interesting to study, but will anyway produce particles that will travel through the detectors surrounding the collision point. The job of the detectors, with some intelligence provided by a large amount of integrated electronics, is to enable the physicists to selectively observe and study only those very rare collisions enlarging man's understanding of the universe. The other collisions will merely produce a radiation background posing a hazard for the reliability of the experiments.

Compared with previous HEP experiments, the novelty resides both in the intensity of the background, due to the very high collision rate, and in the massive use of electronic components inside the detector system, where they are exposed directly to the radiation background. This on-detector electronics is necessary to select potentially interesting collision events and only transfer meaningful detector data (eliminating most of the background) for analysis off-detector. In practice, the devices sensitive to radiation effects are larger in number and types, and the radiation background is considerably more intense, which results in unprecedented radiation concerns for the HEP community.

This paper aims at summarizing these radiation issues. Focus will be on the two largest LHC experiments, but similar problems (though on a smaller scale) have been encountered in other HEP experiments around the world. In particular, original or unusual developments will be highlighted in which either the requirements or the solutions chosen differ from those typical in the space and nuclear radiation effects communities.

## 2. The Radiation Environment

### 2.1. The LHC experiments

Four HEP experiments will be positioned around the LHC ring, corresponding to four particle collision points. Each experiment is actually a large detector system made up of several sub-detector systems. The most challenging in terms of radiation effects are the two general-purpose systems called ATLAS (A Toroidal LHC ApparatuS) and CMS (Compact Muon Solenoid), designed to study p-p collision events. Bunches of protons will circulate in opposite directions in the LHC ring and will be focused at the center of these two large detectors where they will cross at a frequency of 40 MHz. An average of 20 p-p collisions will occur at every bunch crossing. Each of the detectors is built to cover all the solid angle around the collision point, and designed in layers surrounding it, each layer having a different detection function. This is shown in Figure 1 for the CMS experiment. The cylindrical detector layers, called the “barrel” portion of the experiment, surround the collision point. The barrel is closed by detector end-caps in the forward region (at low angle with respect to the beam pipe).

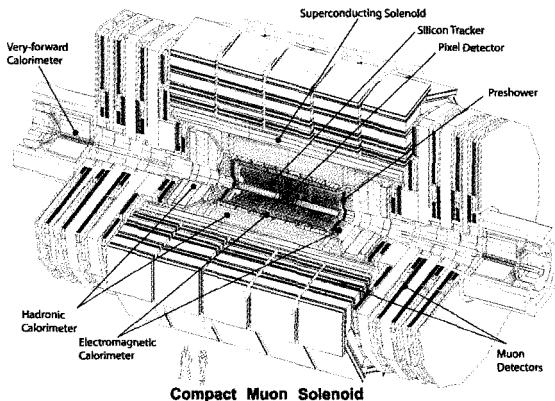


Figure 1: View of the CMS experiment

The innermost sub-detector, called the “tracker”, is used to reconstruct the trajectory of charged particles coming from the interaction point. Particle tracks are naturally denser close to the collision point, therefore requiring detectors able to spatially resolve the tracks with very high precision. This task is performed by pixel detectors, where each sensitive element might be as small as  $500 \times 50 \mu\text{m}$  and the readout electronics is bump-bonded to the sensor with the same small pitch. This close to the collision point, the radiation environment is at its most intense, and radiation hardness of both detectors and electronics is indispensable. To limit the radiation-induced damage to the silicon detectors, all the equipment must be kept constantly at low temperature (around  $-10^\circ\text{C}$ ), imposing strict constraints on the power budget

of the electronics.<sup>1</sup> Because of the electronic functions required, the limited power and space budget and the radiation levels, all electronics installed in this sub-detector is custom-developed (Application Specific Integrated Circuits, ASICs).

The “Electromagnetic CALorimeter” (ECAL) is the sub-detector that particles meet after the tracker in their flight away from the collision point. Its purpose is to measure the energy of electrons and photons with high precision. Space constraints are more relaxed than in the tracker, and also the radiation background is less severe. The “Hadronic CALorimeter” (HCAL) is the following layer, and its aim is to measure the energy of hadrons (such as protons, neutron and pions) produced by the p-p collisions. Finally, the “Muon Detector” measures the trajectory and energy of the muons, particles interacting so weakly that they can cross all the other detector layers. The whole experiment is immersed in an intense magnetic field (2 to 4 T) produced by a complex and massive system of magnets.

The experiments are located in large underground caverns (all the LHC machine sits at a depth varying from 70 to 150 m), and a very large fraction of the control, power and data acquisition electronics is installed inside the cavern and exposed to a radiation field.

## **2.2. The radiation environment**

The radiation environment of ATLAS and CMS is determined by the p-p collisions at their center. The main difference between the two detectors is the presence of the massive return yoke for the magnetic field that in CMS is embedded in the muon detector system and effectively shields the muon detectors electronics and the experimental cavern from particles produced in the calorimeters. As a consequence, the CMS radiation levels in these regions are about an order of magnitude lower.

The inner tracker is exposed to a primary particle flux from the interaction region – mainly composed of pions – and to neutron albedo emerging from the calorimeters. Already in the outer tracker, the charged hadron flux is significantly reduced and neutrons emitted from the surrounding ECAL dominate the particle environment. Neutrons, with practically isotropic distribution, actually dominate the environment also of all other regions of the experiment.

The charged hadron energy distribution covers the range between about 1 MeV and 10 GeV. The spectrum is peaked at around 200-300 MeV and remains almost invariant in shape from the tracker to the outer periphery of the experimental cavern, the absolute fluxes changing meanwhile by 6 orders of magnitude. The neutron distribution has instead a substantial flat low-energy component typically only 1 order of magnitude lower than the peak at 1 MeV. This contributes significantly to displacement damage effects. The neutron spectrum has another peak at around 60-100 MeV, and extends at high energy up to about 1-10 GeV depending on the location.

Table 1 summarizes the radiation levels foreseen in different regions of ATLAS as cumulative doses and fluences over the 10 years expected lifetime of the LHC. These numbers have been obtained with sophisticated simulation tools developed specifically for this purpose. In each region, the field is characterized by three parameters: TID level, fluence of neutrons above 100 keV and fluence of all hadrons above 20 MeV. They are reference levels for ionization, displacement damage and Single Event Effects respectively. All numbers in the table are expressed as maximum levels in the corresponding region of the experiment.

## **2.3. Main radiation issues**

Due to the absence of heavy ions in the experiments’ radiation environment, some issues typical of space applications only apply marginally to the two main LHC experiments. For

instance, Single Event Latchup (SEL) or Single Event Gate Rupture (SEGR) are observed with very low frequency – if at all – in proton irradiation tests. Therefore, these effects have very low probability in the hadron-dominated LHC particle environment. On the other hand, the abundance of neutrons with energy higher than 100 keV renders displacement damage a much more relevant concern than for space applications.

To illustrate the radiation issues and how to address them, it is appropriate to distinguish two regions of the experiments. In the inner region, namely the tracker and some parts of the ECAL (the forward end-cap), the TID levels are so high that it is unthinkable to use commercial electronics. In this region, all electronics is implemented by custom-developed ASICs, manufactured in technologies and with techniques that enable them to stand tens of Mrad of total dose. In this case, all radiation concerns are tackled at the development stage: appropriate technology or design techniques are chosen to achieve TID and displacement damage hardness, to prevent destructive SEEs and to minimize the rate and/or impact of soft errors such as Single Event Upset, Transient or Functional Interrupt (SEU, SET or SEFI). This approach will be illustrated in more detail in section 4.

In the outer region of the experiment and in the experimental cavern most of the electronics functions are implemented with commercial devices, which have no guarantee on radiation effects. Overall, the TID level in this outer region varies between less than 1 krad (most often, in particular for CMS) to more than 25 krad. If in the latter case both cumulative and SE effects have to be carefully addressed, the major concern for the former (about 1 krad) environment is certainly represented by SEEs in general, and in particular by the Burnout (SEB) of power devices. Not only is this a destructive event, hence with permanent effects, but also it affects devices often distributing power to relatively large systems, consequently their failure has a large impact. SEB has been observed frequently in proton and neutron tests<sup>2, 3</sup>, and will certainly threaten power devices in the LHC experiments. The problems encountered in employing Commercial Off The Shelf (COTS) electronics in a radiation environment are well known in the space community. The approach suggested in the HEP community to deal with these problems<sup>4</sup> is not substantially different from what is known already, therefore it will not be addressed by this paper. Instead, the next section will describe the estimation of the SEU rate in the LHC hadron-dominated particle environment, a problem that is common to all the regions of the experiments and that has led to the development of an original computational method.

Table 1: Foreseen radiation levels in the ATLAS experiment, integrated over the scheduled LHC lifetime of 10 years.

<i>Detector region</i>	<i>TID [rad]</i>	<i>Neutrons 1 MeV equiv. [cm<sup>-2</sup>]</i>	<i>Ch. hadrons E&gt;21 MeV [cm<sup>-2</sup>]</i>
Innermost tracker (barrel)	$2.7 \cdot 10^7$	$4.7 \cdot 10^{14}$	$5.4 \cdot 10^{14}$
Outer tracker (barrel)	$5.1 \cdot 10^6$	$1.9 \cdot 10^{14}$	$9.3 \cdot 10^{13}$
ECAL (barrel)	$1.1 \cdot 10^4$	$3.1 \cdot 10^{12}$	$6.0 \cdot 10^{11}$
HCAL (barrel)	$1.0 \cdot 10^3$	$4.3 \cdot 10^{11}$	$1.0 \cdot 10^{11}$
Muon detector (forward)	$3.4 \cdot 10^4$	$1.2 \cdot 10^{13}$	$1.9 \cdot 10^{12}$
Experimental cavern	$1.7 \cdot 10^3$	$6.5 \cdot 10^{10}$	$1.5 \cdot 10^{10}$

### 3. SEU Rate Estimate in the LHC

In the early days of the LHC electronics developments, the HEP community devoted little attention to SEEs, in particular to non-destructive events such as SEUs. This was both for historical reasons (lack of experience in the community) and for the absence of heavy ions in the LHC environment. It was generally believed that the SEU concerns in the space community were largely due to the presence of heavy ions in space. Moreover, the LHC radiation environment was at the time typically only described in terms of TID and 1-MeV neutron equivalent fluence. Detailed information on the energy spectra of particles, a determinant parameter in evaluating the SEE risks, was not generally available. To change this situation, it was necessary to develop a computational method to estimate the SEU rates in the very special LHC radiation environment, and thus draw attention to the non-negligible error rates as well as providing the HEP community with a tool to extrapolate test results available in the literature that normally refer to mono-energetic proton or heavy ion beams. This method has been developed by Huhtinen and Faccio<sup>5</sup>, and the main points will be summarized.

In the LHC environment, an energy deposition sufficient to induce SEU is only possible through the interaction of the hadrons with nuclei in the electronics circuit, the hadrons themselves not having enough Linear Energy Transfer (LET,  $dE/dx$ ) to directly deposit the required charge. Such interaction typically produces a shower of secondary particles and one nuclear recoil, but in some cases there can be several fragments. The recoils normally have low energy, therefore a limited range – implying that they have to be produced locally to be effective in inducing SEU. The difficulty in estimating the error rate resides in the necessity of computing the probability of nuclear interaction, covering all reaction channels, and the amount of ionizing energy deposited by all fragments in the Sensitive Volume (SV, the volume where deposited charge can be collected by the sensitive node and contribute to the SEU). For this purpose, a powerful simulation tool was employed, based on the use of the FLUKA simulation package<sup>6</sup> for the explicit generation of nuclear fragments for neutrons with energy above 20 MeV. For lower energy neutrons, comprehensive neutron cross-section data are available and the fragment generation was made using the information contained in the ENDFB-VI cross-section tabulations. The fragments generated either way were then transported through silicon and, whenever one of them entered a predefined SV, a detailed accounting for its energy loss by ionization was done with a modified version of the TRIM code.<sup>7</sup> Although mainly focused on interaction of hadrons with silicon nuclei, the work also checked for possible contributions from interactions in heavier elements (such as tungsten, quite frequently used in CMOS technologies) and from the interactions of thermal neutrons with boron dopants, finding that neither should dominate the error rates in the LHC.

The result of the simulation is a curve giving the probability per unit fluence to have within the SV an ionizing deposition greater than or equal to any given energy value, such as curve “P” in Figure 2. This probability is therefore expressed in  $\text{cm}^2$  and refers to the individual SV simulated. The simulation can be run for any environment, from mono-energetic protons hitting the device along one direction, like in typical SEU laboratory tests, to the complicated mixed hadron environment of the LHC.

Each electronic circuit can have a different sensitivity to SEUs, and the error estimate must somehow contain this information to lead to meaningful results. In the developed method, this is achieved with the introduction of the SV size (area and depth) and of the critical energy  $E_{\text{crit}}$  for upset. An error can occur only if the energy deposited by the fragments in the SV is larger than  $E_{\text{crit}}$ . The SV has been chosen for simplicity to be a parallelepiped whose vertical

dimension (depth) was varied between 0.5 and 2  $\mu\text{m}$  – finally the depth of 0.5  $\mu\text{m}$  was chosen as it most often lead to the best fit with experimental data. The area of the SV and the critical energy can be obtained for each device when heavy ion irradiation data are available. This information must be combined with the probability curve obtained with the simulation for a unitary area SV ( $1\mu\text{m}^2$ ) to finally compute the error rate for the device in any environment.

A pictorial image of this process is shown in Figure 2. The curve "S", characterizing the sensitivity of the device, is the Weibull fit to the heavy ions experimental points, whilst the curve "P" is the above described probability from simulation for a SV 0.5  $\mu\text{m}$  deep and with a sensitive area of  $1\mu\text{m}^2$ . The Weibull function typically describes the sensitivity of the device (cross-section, therefore sensitive area) as a function of the LET of the heavy ions. To be able to plot both curves on the same scale (energy deposited in the SV) it is necessary to translate the heavy ion LET into deposited energy, which can be done assuming the LET is constant across the SV. The energy deposited by the ion is therefore in first approximation the product of the LET by the depth of the SV.

The shaded area intersection of curves P and S is proportional to the cross-section of the device in the desired environment, which can be computed by binning the intersection energy range and performing the following summation over all energy bins:

$$\Sigma = \sum_i P_i \frac{s_{i+1} - s_i}{A} \quad (1)$$

where  $\Sigma$  is the desired cross-section,  $P_i$  is the probability at the end of the energy bin (not to under-estimate the sensitivity),  $s_i$  is the heavy ion cross-section at the beginning of the energy bin, and A is the area of the SV in the simulation ( $1\mu\text{m}^2$ ). Multiplying the obtained cross-section  $\Sigma$  by the particle flux ( $\text{cm}^{-2}\text{s}^{-1}$ ), the result expresses the error rate (per device per unit time) in the radiation environment of interest.

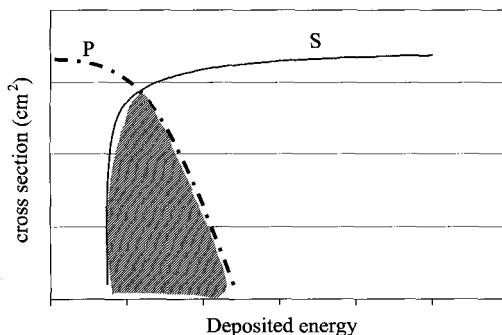


Figure 2: The shaded area is proportional to the cross-section of the device described by the sensitivity curve S (Weibull fit) in the environment described by the probability curve P (from simulation).

The full method has been tested with data available in the literature – mostly published data in the IEEE Transactions on Nuclear Science – for several classes of devices (SRAMs, DRAMs and a microprocessor). For the 18 devices selected, both the heavy ion and the proton cross-section curves as measured in experiments were available. The test consisted in calculating the proton cross-section with the simulation method using the Weibull fit to the heavy ion points as only input, then comparing the result with the available measured proton cross-section. The ratio of the simulation versus experimental results varied between 0.5 and

2.3, a very satisfactory result. The same test was repeated for 4 devices for which also the experimental cross-section for 14 MeV neutrons was available, obtaining in this case a ratio varying between 1 and 4.1. At this low energy of the hadrons, the energy distribution of the produced fragments drops sharply at high energy, and the correctness of the simulation result is much more sensitive to the choice of the sensitive depth.

Having gained confidence in the simulation method, it was possible to compare the SEU cross-section of the same device in different hadron environments: proton, pion and neutron beams from 20 MeV to 10 GeV, isotropic neutron and proton environments from 3 to 200 MeV. The result is summarized in Table 2 for one example device, and several interesting observations can be made:

- (i) Neutrons and protons of the same energy produce almost identical upset rates above 20 MeV.
- (ii) Simulations for isotropic and monodirectional (beam) irradiation show negligible differences in the upset rate.
- (iii) Elastic scattering gives a minor contribution to the SEU rate.
- (iv) Above 60 MeV, the upset rate depends little on the hadron energy. This is true for devices with relatively low LET threshold (hence  $E_{\text{crit}}$ ), which are the most sensitive and the large majority. This might be different for devices with LET threshold above about 8-10 MeVcm<sup>2</sup>mg<sup>-1</sup>. Figure 3 illustrates how the probability curves for 60 and 200 MeV protons have very similar values for  $E_{\text{crit}}$  values around 0.2-1.5 MeV (corresponding to 1.7-12.5 MeVcm<sup>2</sup>mg<sup>-1</sup> for a 0.5 μm deep SV). It also appears that the probability curve for the foreseen environment of the CMS tracker is similar to the two proton curves.
- (v) For 200 MeV pions we observe twice the upset rate of protons of the same energy. This is due to the higher pion inelastic cross-section for reaction with silicon at energy around 200-300 MeV (delta resonance). Experimental measurements have reported contradictory results in this respect: sometimes identical SEU cross-sections for pions and protons have been measured <sup>8</sup>, and sometimes a factor of 5 difference has been reported <sup>9</sup>. The factor of two in our simulation could not therefore be confirmed by experimental results.

Table 2: SEU cross-section, normalized to the 200 MeV proton value ( $8.4 \times 10^{-7} \text{ cm}^2$ ), for a sample device in different hadron environments, from reference <sup>5</sup>. The calculation has been made for a 1x1x1 μm SV. The device is the Texas Instruments SMJ44100 4M DRAM, with a  $\text{LET}_{\text{th}}$  of 1.39 MeVcm<sup>2</sup>mg<sup>-1</sup> <sup>10</sup>.

<i>Particle</i>	<i>Direction</i>	<i>Total σ</i>	<i>Elastic σ</i>
10 GeV proton	Beam	1.2	0.006
200 MeV proton	Beam	1.0	0.011
200 MeV neutron	Beam	0.97	0.007
200 MeV pion	Beam	2.0	0.012
60 MeV proton	Beam	1.05	0.028
20 MeV proton	Beam	0.45	0.10
20 MeV neutron	Beam	0.46	0.022
200 MeV proton	Isotropic	1.03	0.010
20 MeV neutron	Isotropic	0.43	0.099
14 MeV neutron	Isotropic	0.44	0.041
3.1 MeV neutron	Isotropic	2e-7	---

The above observations can be used to recommend an appropriate qualification test procedure for components to be used in the LHC experiments. The simulation of the full LHC environment has shown that, for all example devices used, the upset rates in all regions of the experiments will be dominated by the contribution of hadrons with energy above 20 MeV. With neutron and protons being equally effective in inducing SEU, and with small energy dependence of the upset rate above 60 MeV, it is clearly recommended to use the widely available mono-energetic protons as preferred test source. Additionally, the monodirectional beams typical of cyclotron proton sources well simulate the almost isotropic environment of the LHC<sup>a</sup>. Therefore, a reasonable estimate of the SEU rate in most locations around the LHC can be obtained by using a 60-200 MeV proton beam to irradiate the candidate devices. Only for inner trackers, where the particle environment will be dominated by pions, this might be too optimistic by a factor of 2-5 at most.

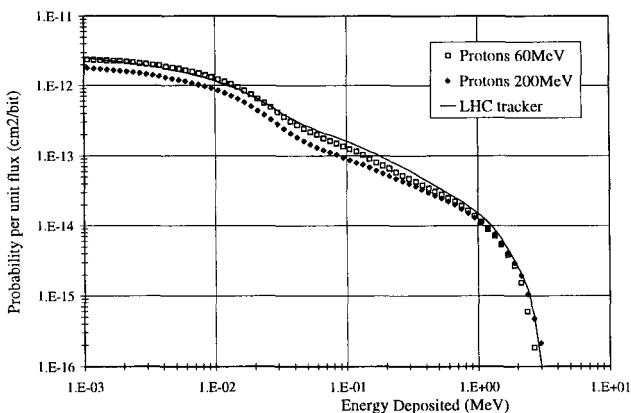


Figure 3: Energy deposition probabilities, for a  $1 \times 1 \times 1 \mu\text{m}$  SV, for protons of 60 and 200 MeV and for the CMS tracker environment. The curves show the probability to have within the SV an ionizing deposition greater or equal to the indicated “Energy Deposition” value.

#### 4. Radiation-Hard ASICs Design

##### 4.1. ASICs design in dedicated rad-hard processes

In the inner region of the LHC experiments, where TID levels are expected to largely exceed 500 krad, the electronics functions have to be performed by radiation-hard ASICs. In the early days of the Research and Development (R&D) for the LHC, the only possible solution seemed to be the use of a dedicated radiation-hard technology. This happened at the beginning of the 90s, when several such technologies were still available both in Europe and in the United States. The R&D efforts concentrated in assessing the use of some of these technologies<sup>11,12,13</sup> for the particular LHC requirements: mixed analog-digital circuits with strict specifications on the noise performance, relatively large volumes (hundreds of wafers) in comparison with the markets these technologies were usually serving. It soon turned out that there were difficulties in following this approach: the required performance in terms of low noise and high radiation

<sup>a</sup> Neutrons, largely dominating the particle environment as from the outer tracker, are originated from interaction of primary hadrons with the detector materials and have therefore practically isotropic flux.

hardness (10 Mrad for the inner tracker) were difficult to be met regularly in the low-volume manufacturing foundries. The resulting low yield further increased the cost per circuit, which was already high for these dedicated radiation-hard processes. The shrinking of the global demand of these technologies as from the first half of the 90s, and the interruption of governmental funds to maintain them, obliged most companies to withdraw access to the processes for ASIC design, or sometimes even to close the manufacturing lines.

Essentially, the only radiation-hard process still in use today for circuit design for the LHC is the BiCMOS DMILL process.<sup>14</sup> This technology was developed in the early 90s and was tailored to satisfy also the LHC requirements. Though several devices planned to be available have been abandoned during the development (CJFETs and PNP bipolar transistors), this SOI technology offers CMOS and NPN bipolar transistors. The process, originally developed at CEA-LETI (Grenoble, France), was industrially transferred to ATMEL (formerly TEMIC) and is used for a number of ASICs amongst which the highest volume demand is for the readout electronics for the ATLAS tracker (about 900 wafers).<sup>15</sup> Although the process is qualified and guaranteed for 10 Mrad and  $10^{14}$  neutrons/cm<sup>2</sup>, for some applications with very tight power consumption requirements it was necessary to assess the radiation tolerance of the ASICs for every production lot. Such a time-consuming procedure has been setup and is at present carried out at the wafer level with an X-ray generator (for TID).

#### 4.2. Hardness by design using commercial technologies

Another approach, based on the use of commercial CMOS technologies, has recently become popular in the HEP community and at this time most of the LHC ASICs are designed this way. Research in the 80s demonstrated that radiation effects in laboratory SiO<sub>2</sub> layers decrease quadratically with the oxide thickness, and even more sharply when the thickness is reduced below about 10 nm.<sup>16,17</sup> When scaling down CMOS processes following what is known as Moore's law<sup>18</sup>, the gate oxide thickness of the transistors is also decreased. A study of radiation effects in several technology generations<sup>19,20</sup> demonstrated that these commercial-grade gate oxides followed the expected behavior, as shown in Figure 4. It appears that the 5-6 nm gate oxide of the quarter micron technology node that started to become available around 1996-97 is appropriate for multi-Mrad applications.

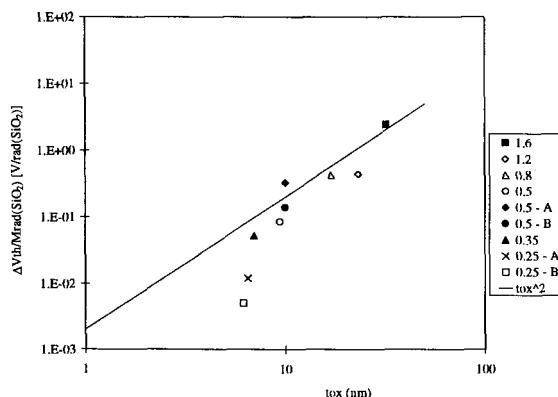


Figure 4: The threshold voltage shift of commercial-grade transistors from several technology generations follows the expected trend, sharply decreasing below the  $t_{ox}^{-2}$  law for a thickness of around 10 nm. Some data are from.<sup>21</sup>

Unfortunately, the lateral and isolation oxide thickness does not need to scale down, and despite the introduction of the Shallow Trench Isolation (STI) process around the  $0.25\text{ }\mu\text{m}$  technology node this represents the weak point, in terms of TID tolerance, of modern submicron CMOS.<sup>22</sup> Radiation-induced charge trapping in the thick lateral oxide induces source-drain leakage currents in NMOS transistors.<sup>23</sup> Trapping in the isolation oxide can open leakage current paths between n+ diffusions at different potential (transistor to transistor or Nwell to transistor leakage), as shown in Figure 5. These leakage currents at first increase the current consumption of the still functional circuit, until failure occurs at some point typically in the 10-100 krad TID range.

It is nevertheless possible, with the use of custom layout techniques, to prevent the opening of these leakage current paths.<sup>24</sup> Enclosed Layout Transistors (ELT, sometimes called “edgeless transistors”) are very effective in eliminating any source-drain leakage and were in fact already used in the early days of the CMOS processes to this aim.<sup>25</sup> The absence of any thick oxide between the source and drain diffusion, a consequence of the enclosed layout where the drain (or source) is completely surrounded by the thin gate oxide, is the reason for that. In Figure 6, the comparison between the standard and enclosed layout transistors clearly illustrates the hardness improvement of ELTs. Another layout technique, namely the systematic use of guardrings, serves the purpose of cutting the leakage current paths under the isolation oxide. In this approach, a heavily doped p ring separates all n+ diffusions (Nwell included) at different potential. The charges trapped in the isolation oxide in Figure 5 can invert the surface of the low-doped p substrate, hence opening a conductive channel between adjacent n+ diffusions, but they cannot invert the heavily doped p guardring, which effectively cuts the leakage path.

The combined use of ELTs and guardrings, called “radiation tolerant layout technique”, has been known for some time<sup>24</sup>, but only with the availability of deep submicron technologies, with naturally radiation tolerant gate oxides, could it enable the development of ASICs capable of surviving in multi-Mrad environments. An R&D effort at CERN<sup>26</sup> has deeply studied this approach and developed the tools necessary for ASICs design in a selected commercial quarter micron technology that is now widely used by the HEP community.

Compared to the use of a dedicated rad-hard technology, the use of a commercial technology brings advantages in terms of low cost, high yield, high speed, low power consumption and high density. The typical commercial foundry has a throughput of a few thousands wafers per week, which is a guarantee for high yield and process reproducibility. Moreover, despite the use of the cumbersome ELTs and guardrings, that considerably decrease the design density, the integration density that can be achieved with this approach is still considerably higher than for dedicated radiation-hard processes, which are typically at least two technology generations late.<sup>27</sup> Overall, the cost difference for the same performance – whenever the same performance can be achieved – is very large.

Since radiation hardness is achieved because of the small gate oxide thickness, which is necessarily very well controlled in these modern processes, the good performance in a radiation environment is expected to be reliably obtained across the full production cycle of any ASIC.

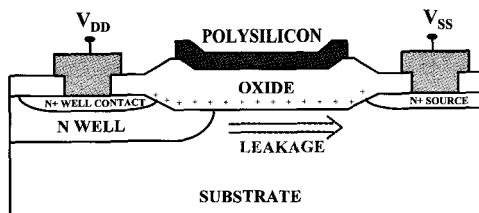


Figure 5: Radiation-induced leakage path under the isolation oxide. In this case, the current flows between an N-well and an n+ diffusion (source or drain of a NMOS transistor). The polysilicon line, in this example used to route a signal as a "level-0" metal, acts as an equivalent gate for the parasitic transistor where the leakage current flows.

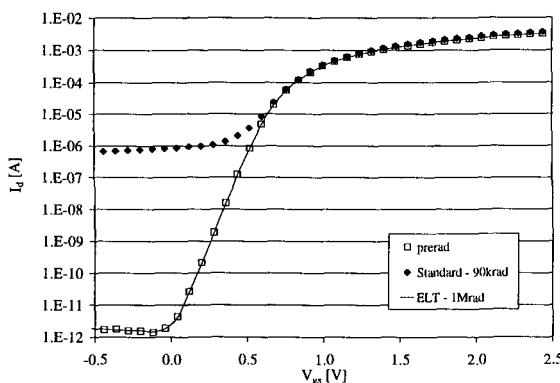


Figure 6: The effectiveness of ELT in eliminating source-drain leakage currents is demonstrated in a  $0.25\text{ }\mu\text{m}$  CMOS technology for transistors with  $\text{W}/\text{L} = 10/0.25$ . Drain-source bias is 2.5V, the maximum  $\text{V}_{\text{dd}}$  in this technology. Devices were biased in the worst-case condition during irradiation.

In the R&D phase, and later in prototype circuits for the LHC, the effectiveness of this approach with the selected  $0.25\text{ }\mu\text{m}$  technology has been demonstrated: all of the circuits irradiated to TID levels varying between 10 and 30 Mrad have continued to work with unchanged performance.<sup>28,29,30,31,32,33</sup> These circuits contain a very wide range of analog and digital functions, including low-noise amplifiers, high speed (1.6 Gbit/s) digital optical transmitters, PLLs and DLLs, analog memories, 10-bit ADCs, optical receivers and 60 kgate digital circuits. The degradation in the static parameters of individual transistors summarized in Table 3 is useful to appreciate the magnitude of the radiation effects.

Since the used technology, as all other modern CMOS technologies, is not sensitive to displacement damage for fluences below  $10^{15}\text{ n/cm}^2$  (and possibly even well above this level), displacement effects will not be discussed in the following sections.

Table 3: Degradation of the static parameters of NMOS and PMOS transistors in the quarter micron technology, after 30 Mrad( $\text{SiO}_2$ ) and annealing.<sup>34</sup> Annealing was at  $100^\circ\text{C}$  for 168 hours, under worst case bias.

Parameter	NMOS	PMOS
$\Delta V_{\text{th}}$	+ 45 mV	- 55 mV
Mobility degradation	- 6 %	- 2 %

#### 4.3. Drawbacks of the hardness by design approach

The use of the radiation tolerant layout technique introduced a number of complications as compared to the standard design flow in a commercial process. In the first place, a model for the effective size (width  $W$  and length  $L$ ) of ELTs had to be developed, since it was not known how to account for the 4 transistor “corners”.<sup>35,36</sup> The possible variations of the enclosed shape being almost without limitation, we defined one “standard” shape (see Figure 7) and only model that. Moreover, these peculiar transistors are not source-drain symmetrical, and as a consequence the output conductance is higher when the central electrode is the drain.<sup>27</sup> These characteristics are not integrated in the SPICE simulation model, and the development of a custom model was far beyond the available resources. Therefore, we had to integrate a series of work-arounds in the simulation flow to accurately predict the circuit response when using ELTs.

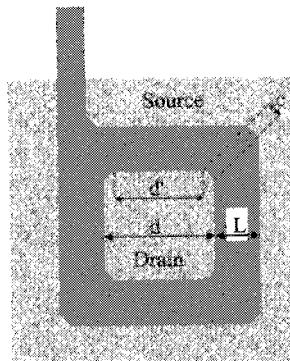


Figure 7: The enclosed shape that was chosen as “standard” and modeled has corners cut such that the length “ $c$ ” is the same irrespective of the gate length  $L$ .

Logic blocks and circuits are normally designed using commercially available libraries, but none existed using ELTs and guardrings. Therefore, we had to build our own “radiation-tolerant LHC library” – and fully characterize it – for that purpose.<sup>37</sup> Because of the limited resources available, the number of gates and I/Os in the library is certainly not comparable with commercial libraries, but it is sufficient for our purposes (the largest digital circuit, a 36 mm<sup>2</sup> chip for the control of the CMS tracker, contained 60 thousand gates).

Finally, there is a large density penalty to pay when using ELTs and guardrings, a factor between 1.5 and 3.5 for the digital cells in our library – possibly larger for complex blocks. This penalty was not critical for most of our circuits, and is the price to pay for radiation hardness. On the other hand, as mentioned above, the alternative approach of using dedicated rad-hard technologies leads – when comparing technologies generations available at a given time – to even lower densities.

#### 4.4. Noise and matching of ELTs

Noise performance is of paramount importance in the design of low-noise front-end circuits for particle detectors, because it determines the minimum detectable signal from the sensor. It was therefore essential to study the noise characteristics of the quarter micron process chosen for LHC circuit design, and in particular their evolution with TID.<sup>38</sup> Measurements were performed on NMOS and PMOS transistors in weak, moderate and strong

inversion in the frequency range 200 Hz – 30 MHz. The inversion regions more interesting for readout of particle detectors are weak and moderate: the input transistor of readout amplifiers has a large W/L ratio to match the detector capacitance, hence it works very close to weak inversion for maximum  $g_m/I_d$  and minimum power for a given transconductance. A typical noise spectrum, for an enclosed NMOS transistor, is shown in Figure 8.

PMOS transistors have a smaller 1/f noise, a result generally common to all technologies, but also the 1/f noise measured on NMOS is acceptable for the low-noise application foreseen, provided a channel length larger than 0.5  $\mu\text{m}$  is chosen.<sup>38</sup> More relevant to our applications is the white noise performance, which has been measured as very good since the excess noise factor – expressing the ratio between the measured and the theoretical noise levels – is very close to 1 for all transistors in moderate and weak inversion. Irradiation up to 100 Mrad with X-rays only increases the white noise by 15% for NMOS and 7% for PMOS (in  $\text{V}/\text{Hz}^{1/2}$ ). The chosen technology therefore certainly appeared to satisfy, even after irradiation, the low-noise requirements for particle readout electronics.

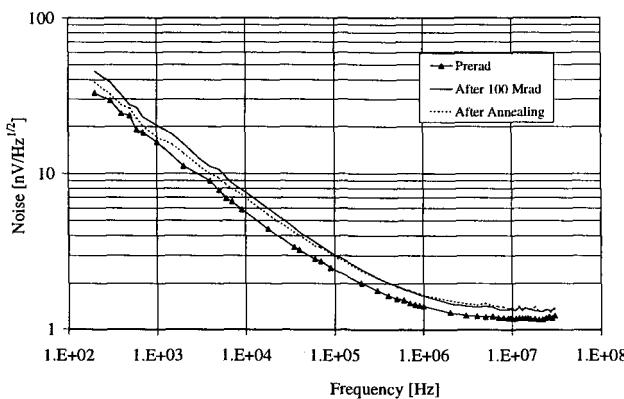


Figure 8: Noise spectrum of an enclosed NMOS transistor with  $\text{W}/\text{L}=200/0.5 \mu\text{m}$ .

Another critical parameter for analog design is the matching of transistors of identical geometry<sup>39,40</sup>: circuit blocks such as differential pairs and current mirrors heavily rely on device matching. For these reasons matching is a subject widely studied, but no literature on irradiation effects on matching was known to us, and certainly the matching of ELTs had never been studied before. A dedicated set of test structures has been designed in the quarter micron technology to explore this field, and though eventually several aspects where not understood, a thorough picture was obtained.<sup>41</sup> The results that are detailed in the following have not been widely published so far.

Matching being a statistical property, it is necessary to measure a large number of transistors to get meaningful results. This is normally done at the wafer level, which complicates the irradiation procedure. To this purpose, we used an X-ray source (with a tungsten target to produce 10 keV fluorescent lines as in reference<sup>42</sup>) and a semi-automatic wafer prober. With this setup, it was possible to keep the transistors under bias during irradiation with the help of a probe card, and to collimate the X-rays on the biased devices only. This procedure was repeated by stepping across all positions in the wafer at room temperature up to a total dose of 1.5 Mrad( $\text{SiO}_2$ ) and using a dose rate of 17 krad( $\text{SiO}_2$ )/min. The typical worst-case bias condition was chosen: all terminals grounded for PMOS

transistors, and Vdd potential to the NMOS transistor gate (2.5 V, all other terminals being grounded).<sup>43</sup> After irradiation, the wafer was annealed with devices unbiased at 100°C for a week and matching was measured again.

Matching is measured on transistor pairs, where the two transistors have been laid out carefully to be completely identical – same geometry, same environment, same connections to the terminals. The two transistors of each of our pairs were statically measured to extract the threshold voltage  $V_{th}$  and the current factor  $\beta$ . We calculated the difference  $\Delta V_{th}$  and the relative difference  $\Delta\beta/\beta$  for the pair, and repeated that for 90 identical pairs integrated regularly in the wafer, obtaining two distributions. The sigma values of these distributions give respectively the mismatch of the threshold voltage and of the current factors for the transistor pair under study (given size and shape). This procedure was repeated on a series of transistor pairs with different size to study the mismatch dependence on the transistor gate area. These data were plotted, as usually done in matching studies,<sup>40</sup> as a function of the square root of the inverse of the gate area, as shown in Figure 9 for the threshold voltage of regular NMOS transistors. The slope of these curves,  $A_{V_{th}}$  and  $A_{\Delta\beta/\beta}$  respectively, is a good indicator of the matching performance. It has been found that  $A_{V_{th}}$  scales with the gate oxide thickness  $t_{ox}$ , and in technologies with good matching performance the value of  $A_{V_{th}}/t_{ox}$  is 1 mV·μm/nm, whilst  $A_{\Delta\beta/\beta}$  is typically about 1-3 %·μm.<sup>44</sup>

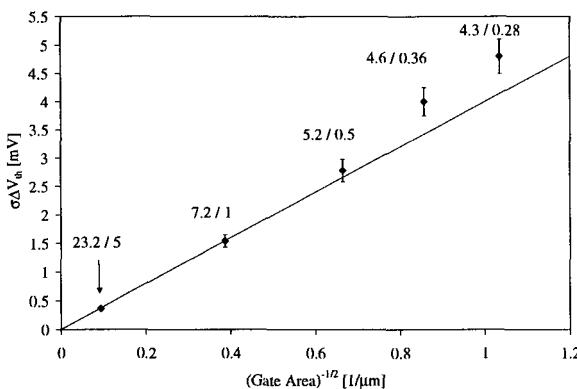


Figure 9: Threshold voltage matching of NMOS transistors with standard layout in the studied quarter micron technology, from reference.<sup>41</sup> The W/L ratio of the measured transistors is indicated.

Before irradiation, for regular NMOS and PMOS transistors in the chosen quarter micron technology the slopes were well within the expected range for a 5.5 nm gate oxide thickness: 4 and 3.7 mV·μm/nm for the threshold voltage of NMOS and PMOS transistors respectively, and about 1 %·μm for the current factor. However, for NMOS ELTs instead the experimental points in the same plots do not follow a straight line, as can be seen in Figure 10 for the threshold voltage in the case in which the enclosed diffusion is used as the transistor drain. The experimental points can be fitted with the following equation (for the threshold voltage, but similarly for the current factor):

$$\sigma_{\Delta V_{th}} = \sqrt{\frac{A_{V_{th}}^2}{WL} + \sigma_0^2} \quad (2)$$

The values of  $A_{V_{th}}$  and  $\sigma_0$  used in the fit of Figure 10 are 4.3 mV $\mu\text{m}$  and 1 mV, the slope being actually very close to the value of 4 measured for standard NMOS transistors. It appears that in the case of ELTs there is an additional mismatch source, independent of the gate area and never observed before in standard transistors. Experiments showed that the relative contribution of the additional source, quantified by  $\sigma_0$ , depends on the size/shape of the drain electrode. This can be seen in Figure 10, where the two circular symbols represent two ELTs with the same gate area as those on the curve fitting equation (2), but with the surface of the inner diffusion (here used as the drain) four times larger. It can also be seen in Figure 11, where the two curves are for the same transistors with drain chosen as the inner and outer diffusion respectively. In the latter case, the value of  $\sigma_0$  decreases to 0.5 mV. This peculiar behavior has not been understood yet, and is even more difficult to explain considering that the extraction of the parameters has been performed in the linear region of operation of the transistor (low electric field in the drain region).

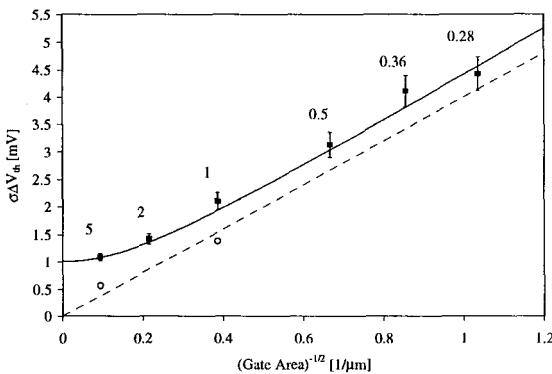


Figure 10: Threshold voltage matching of ELT NMOS transistors with the inner diffusion used as the drain, from reference.<sup>41</sup> The gate length of the measured transistors is indicated close to the points. The white circles represent two transistors with larger area of the inner diffusion, and the error bars are not indicated. The dotted line is the fit for the standard layout transistors.

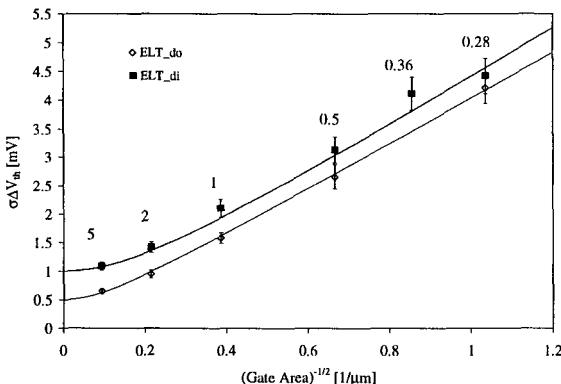


Figure 11: Comparison of the threshold voltage matching of the same ELT pairs with the inner (ELT\_di) or the outer (ELT\_do) diffusion used as the drain, from reference.<sup>41</sup> The gate length of the measured transistors is indicated close to the points.

While the current factor matching experimental points can be fitted with an equation similar to (2), with  $A_{\Delta\beta/\beta} = 1.3 \text{ \%}\mu\text{m}$  and  $\sigma_0 = 0.3 \text {\%}$ , the matching in this case does not depend on which diffusion is chosen as drain nor on the size of the inner diffusion.

Irradiation affects in a different manner the threshold voltage matching of PMOS and NMOS transistors, whilst for both devices the current factor matching is unaffected, in agreement with the very low degradation of the transconductance. As shown in Figure 12, the TID of 1.5 Mrad( $\text{SiO}_2$ ) mildly influences the threshold voltage matching of PMOS transistors. For NMOS transistors, instead, the slope  $A_{V_{th}}$  increases to  $5.4 \text{ mV}\mu\text{m}$ , an increase of 45% meaning that another mechanism begins to dominate the mismatch performance (Figure 12). Such a large increase cannot be correlated with any other irradiation effect measured on the same transistors, in terms of static parameters (threshold voltage, subthreshold slope, transconductance) or noise. In practical terms, this means that NMOS differential pairs will degrade their matching (hence their offset) with TID to an extent larger than for PMOS transistors.

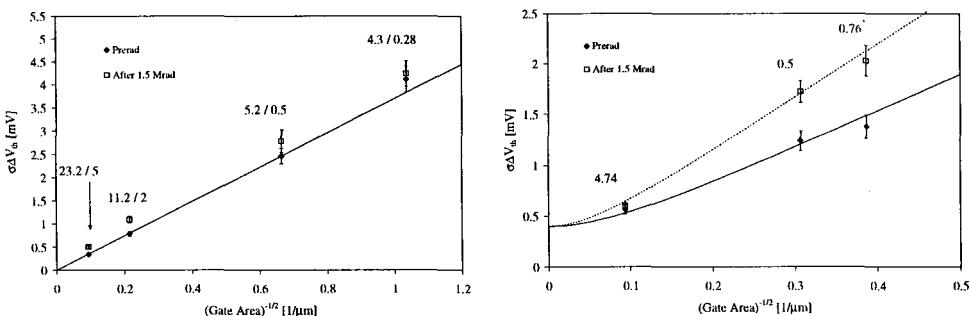


Figure 12: Irradiation up to 1.5 Mrad( $\text{SiO}_2$ ) mildly influences the threshold voltage matching performance of PMOS transistors (left).<sup>41</sup> This is not the case for NMOS ELT devices (right), where the inner diffusion is used as the drain.<sup>41</sup>

#### 4.5. Single Event Effects

In the LHC experiments, SEE will threaten the reliable performance of ASICs designed with the above-described hardness by design approach. SEGR is not considered to be an issue in the LHC hadron environment, because this effect does not appear to be a threat for modern commercial deep submicron circuits even in the presence of heavy ions.<sup>45,46</sup> The main causes of concern are therefore SEL and SEU.

SEL sensitivity has been shown to decrease in modern deep submicron processes due to the combination of several favorable technological choices such as retrograde wells and STI isolation.<sup>47</sup> Moreover, device simulation has pointed out the effectiveness of guardrings in substantially decreasing SEL susceptibility.<sup>48</sup> Considering that our designs employ both a deep submicron process and guardrings, and because the environment is relatively "benign" due to the absence of heavy ions, we did not expect SEL to be a real concern. In fact, digital test circuits designed using cells from our "radiation tolerant" library have been irradiated at room temperature and nominal supply voltage (2.5 V) with heavy ions of LET up to  $89 \text{ MeVcm}^2\text{mg}^{-1}$ , and no latch-up has been observed.<sup>49</sup> Moreover, two prototype ICs for the LHC have been exposed to heavy ions up to an LET of 59 and  $110 \text{ MeVcm}^2\text{mg}^{-1}$  respectively, without any SEL.<sup>50,51</sup> Proton and pion irradiations at different energy have also been performed on several prototype ICs as a routine qualification procedure, and no latch-up has ever been reported. All

the above contributes to rule out the SEL concern for circuits developed using our hardness by design approach.

Concerning SEU, both the frequency and system impact of this type of single event effect depend too closely on the circuit and system architecture to be able to generalize. Nevertheless, it can be said that the penalty paid in terms of density and power consumption when using ELTs turned out to be an advantage in terms of SEU sensitivity. The use of enclosed geometry for NMOS transistors sets a lower limit to the gate width (about  $3.3\text{ }\mu\text{m}$  in our case), since the gate has to completely surround the minimum size drain. In digital cells, the PMOS transistor has to be sized correspondently large to match the driving strength of the NMOS. As a result, both the node capacitance (proportional to the gate area) and the current drive of the transistors (proportional to the aspect ratio  $W/L$ ) are considerably larger than for the minimum size transistors achievable with standard layout. This has two consequences: on one hand the threshold charge for upset increases, and on the other hand the saturation cross-section, proportional to the area of the sensitive node, also increases. In the hadron-dominated LHC particle environment, with LET of the generated fragments limited to below about  $15\text{ MeVcm}^2\text{mg}^{-1}$ , the increase in the threshold has by far the larger impact, and the error rate decreases.

The simple flip-flop cell (DFF) in our library has an LET threshold for upset close to  $14\text{ MeVcm}^2\text{mg}^{-1}$ ,<sup>49</sup> very high with respect to typical values for designs in a quarter micron process. The same trend has been confirmed on an SRAM cell, for which we have measured a LET threshold of  $5.4\text{ MeVcm}^2\text{mg}^{-1}$ .<sup>52</sup> With such high thresholds to start with, and in a particle environment dominated by hadrons, it is possible to slightly modify the design of the cells when it is necessary to decrease the SEU sensitivity. For instance, in the case of the DFF mentioned above, a slight modification of the transistor size or of the capacitive load of the nodes is sufficient to decrease the foreseen error rate in the LHC by a factor of  $10$ .<sup>52</sup> This approach has been followed occasionally for critical elements of some LHC ASICs. Alternatively, designers have looked for cells with equivalent functionality but smaller sensitivity, developed specifically to be SEU tolerant. Several types of such custom cells are available in the literature,<sup>53,54</sup> and most often they have been used to protect the content of critical registers. In other cases, the Triple Modular Redundancy (TMR) approach has been used, where each bit of information is stored in three identical cells, and a voting between the three ensures the correct value is output. Finally, Error Detection And Correction (EDAC) in transmission protocols is very frequently used to decrease the Bit Error Rate of the systems, and efficiently corrects for errors due to both noise and radiation.

## 5. Conclusions

With the new generation of physics experiments, the HEP community is facing unprecedented radiation concerns. Not only do the foreseen radiation levels range up to tens of Mrad, but the required volumes of radiation tolerant electronics and the complexity of the detector systems make reliable operation a very difficult objective. The particle composition of the radiation environment – dominated by charged and neutral hadrons over a wide energy range – also complicates the estimate of the SEE rate in the LHC experiments.

This paper has summarized the main radiation issues for reliable operation of detector electronics in the LHC experiments, focusing on two original developments: a novel computational method to estimate SEU rates, and a radiation tolerant layout approach for ASIC design.

To reliably estimate SEU rates in an environment composed of hadrons with a wide energy spectrum, it was necessary to develop a computational method based on the use of software packages developed by the HEP community and containing all the information concerning the nuclear interaction of hadrons with silicon nuclei. Although several radical assumptions have to be made, in particular on the size and shape of the volume in which the charge effectively contributing to SEU is deposited, comparison with experimental benchmarks has shown that this method leads to reliable rate predictions. Lessons learned during the development were used to propose a standard radiation qualification protocol – based on the use of monoenergetic proton beams of 60-200 MeV – for the LHC electronics components.

A large number of ASICs in relatively large volumes (for the typical applications in which radiation hardness is required) are needed for the inner parts of the LHC experiments. The use of radiation tolerant layout techniques, coupled with the natural hardness of the thin gate oxide of a quarter micron CMOS technology, is the solution which has most often been chosen by the LHC ASIC designers. Advantages and drawbacks of this approach have been investigated, and all the tools necessary to efficiently design ASICs with this methodology have been developed for the chosen commercial CMOS process: models for the special enclosed layout transistors, a small digital library and all software tools necessary for the typical design flow. All aspects related to precise low-noise analog design, such as noise and matching, have been investigated and eventually the radiation tolerance of all prototypes has proven to be largely sufficient for LHC applications.

The HEP community has devoted so far a considerable effort to solve the problems related to the reliability of the electronics that will be installed in the radiation environment of the LHC experiments. Most of these were not in the field of expertise of the community, and required therefore a long learning phase. Although progress has certainly been made, and technical solutions are at present generally well recognized, a large amount of work remains to be done in producing, testing, qualifying and assembling the electronics components in reliable electronics systems. This task will surely continue to demand a large effort from the community in the few remaining years before the first proton beam will circulate in the LHC tunnel.

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## SPACE RADIATION EFFECTS IN OPTOCOUPLES

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Assessing the risk of using optocouplers in satellite applications offers challenges that incorporate those of commercial off-the-shelf devices compounded by hybrid module construction techniques. In this paper, we discuss these challenges with regard to radiation-induced effects, e.g., single event transients in the photodiodes and displacement damage effects in light emitting diodes. Radiation-induced effects can depend on several important variables including circuit application, radiation environment, annealing, temperature, and others. Despite the ominous list of test variables above, it is possible to make a conservative estimate of optocoupler performance in the space radiation environment. However, these predictions could result in an overestimation of on-orbit performance by an order of magnitude or more.

**Keywords:** Optocouplers; space radiation; single event transients; displacement damage.

### 1.0 Introduction

Optocouplers operate on the principle that light can be emitted, transmitted, and absorbed by a semiconductor to communicate signals optically. The optical signal electrically isolates the microelectronic circuits on either side of the optocoupler—a primary use for optocouplers. **Figure 1** shows a schematic representation of an optocoupler.

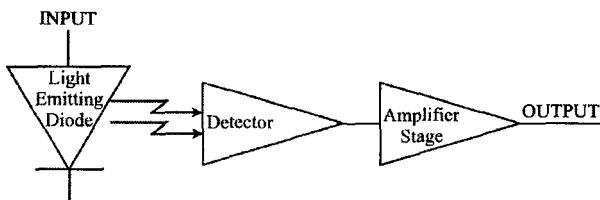


Fig. 1. Representative optocoupler design. The receiver side contains a detector and possibly a simple amplification stage.<sup>7</sup>

Optocouplers use a light emitter—typically a Light-Emitting Diode (LED)—to provide an internal optical signal to a photodetector and amplifier (or phototransistor). There is no direct electrical connection between the LED and output; this results in a very high degree of isolation between the electrical signal that drives the LED and the output of the amplifier. Optocouplers—which implement an optical link and isolation function within a single package—are strictly commercial off-the-shelf (COTS) devices. Past studies have shown that optocoupler performance is adversely affected by both radiation-induced permanent damage and single event effects.<sup>1-12</sup> The components that make up an optocoupler rely on carefully grown, well-defined microscopic structures that can have very low tolerance for slight changes in their characteristics. When a component is exposed to radiation, the radiation transfers some of its energy to the component materials, changing the local material properties. This can have significant effects on component functionality and/or parametrics with the end result depending on the type of radiation and where within the optocoupler the energy deposition occurred.

In this paper we will review the Single Event Transient (SET), Total Ionizing Dose (TID) and Displacement Damage (DD) effects that occur when an optocoupler is exposed to a radiation environment. **Table 1** lists components used to make up optocouplers and the performance degradation mechanisms that are most important for each. We will briefly consider these radiation effects and how these effects may degrade optocoupler performance. Single-event transients in photodetectors and amplification circuitry will be discussed first, then we will describe permanent degradation (TID and DD) of optocoupler parameters.

**Table 1.** Dominant performance degradation mechanism for each component of an optocoupler.

LED	DD
Photodetector	TID, SET
Amplification Circuit	TID, SET
Coupling Medium	TID

## 2.0 Optocoupler Types Addressed in This Paper

This paper will focus on radiation-induced effects in high-bandwidth digital signal isolators and current transfer optocouplers. While the degradation mechanisms described below can cause performance reduction or failure in other types of optocouplers, we will not specifically address these in this paper.

**Figure 2** shows an x-ray image taken of a typical current transfer optocoupler. The optocoupler contains an LED (white dashed box outline), transmission medium (outlined with black dashed line), and phototransistor (solid white box outline). The LED's function is to convert the electrical signal into an optical format. The role of the transmission medium is to transfer the optical signal from the transmitter to the receiver. The optical receiver's (in this case a phototransistor) purpose is to convert the optical signal back into an electrical signal. The optical signal is detected by the phototransistor, its output current is related to the intensity of the optical signal.

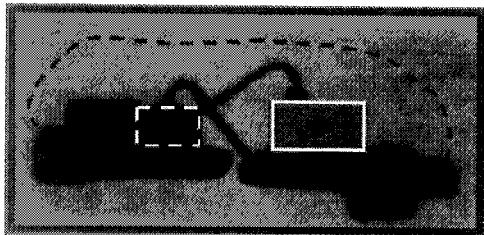


Fig. 2 X-ray image of a simple current transfer optocoupler.

**Figure 3** shows a typical design for a high bandwidth digital signal isolator. Like the current transfer optocoupler, these types of couplers have an emitter, transmission medium (not shown) and a receiver. However, in this case the receiver is a photodiode followed by an amplification circuit.

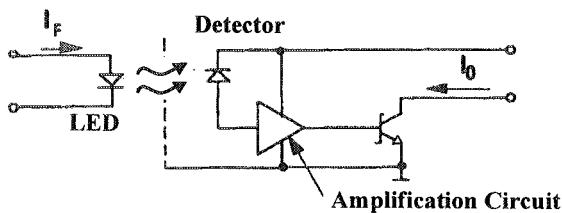


Fig. 3 Typical high bandwidth digital signal isolators design.

Optocouplers, because of their COTS orientation, typically use low-cost design approaches that target high-yield above minimum performance levels. Optocouplers are hybrid devices, and while some vendors are attuned to the specialized needs of the aerospace community, most are not. Traceability of internal components is not the rule, and as a result (as we will see later) device-to-device and lot-to-lot variability in radiation response is common.

### 3.0 Physical Mechanisms of Particle-Induced Transient Effects

#### 3.1. Introduction

Single event error mechanisms for optocouplers are fundamentally different from conventional microelectronics. The most SET sensitive element is usually the optoelectronic photodetector. The problem is exacerbated by the fact that detector elements are often large area diode structures with diameters of several hundred microns.

Also, an optocoupler's detector diode is commonly incorporated monolithically using conventional bipolar processing methods. The importance of this arises from the fact that the p-n junction found in bipolar processes does not collect charge primarily via drift from

a fully depleted intrinsic region. Instead, in bipolar p-n junctions, diffusion from the field-free substrate bulk may be a significant source of both the optically detected signal, as well as the charge deposited by the ionizing particle. Characteristics of optocoupler cross-section measurements consistent with charge collection via diffusion were first noted by LaBel, et al.<sup>6</sup>, and this was examined by Reed, et al.<sup>7</sup> and Johnston, et al.<sup>8,11</sup> with indications that diffusion lengths approaching 50  $\mu\text{m}$  could be possible.

### 3.2 Single Event Transients

An ionizing particle generates electron-hole pairs along its path as it passes through a material, resulting initially in a line charge distribution with equal numbers of holes and electrons. Because the operation of active optocoupler components is governed by the controlled injection of charge into the depletion layers of p-n junctions, the uncontrolled charge injection resulting from ionization can produce a self-recoverable false-signal on the output of the optocoupler. These false signals are known as SETs. Particles incident on either the photodetector or amplification circuitry can produce SETs, but the photodetector is typically much more sensitive. Proton-induced SETs in high-bandwidth optocouplers (like those in **Figure 3**) were reported first by LaBel, et al. following an investigation of onboard flight anomalies due to single particle effects in optocouplers used on the Hubble Space Telescope (HST).<sup>6</sup>

Protons can generate ionization by either direct means—in which the proton itself generates the charge—or by indirect means—in which the products of a proton-nucleus collision generate the charge. Either of these event types can induce an SET at the output of an optocoupler. For most microelectronics, direct proton ionization generates far too little charge to be an SET concern. However, the high sensitivity of some photodetectors contained in optocouplers means that direct proton ionization cannot be ignored. **Figure 4** shows, in pictorial form, the fact that both direct and indirect ionization can induce an SET at the output of an optocoupler. The long path length through the photodetector at grazing angles plays a critical role for the case of direct ionization, while the location of the reaction and its products plays a critical role for the indirect ionization case. Indirect ionization tends to dominate the device response for protons incident normal to the large diode surface, while direct ionization tends to dominate for grazing angle events. Quantifying how each event type impacts the overall circuit performance depends on the detector geometry, the amplification circuitry, and the sensitivity of the circuitry that is affected by the output of the optocoupler.

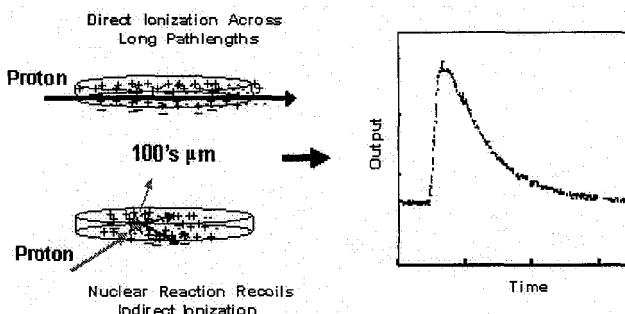


Fig. 4 Protons can generate charge in a device by either direct or indirect ionization. If sufficient ionization is generated, a single-event transient (SET) may result.

**Figure 5** plots the cross-section (number of events divided by the proton fluence) for generating an SET on the output of an optocoupler. Except for grazing angles, the cross-section is constant and presumed to be dominated by nuclear elastic and inelastic interaction recoils. The SET cross-section for protons at near-grazing incidence (90 degrees on this chart) is more than an order of magnitude higher than the cross-section for normally incident protons—this despite the fact that the physical device cross-section is actually lower for grazing-incidence protons. The enhancement around grazing angle is due to direct ionization from protons, and suggests a low charge threshold and LET dependence for the error cross-section.

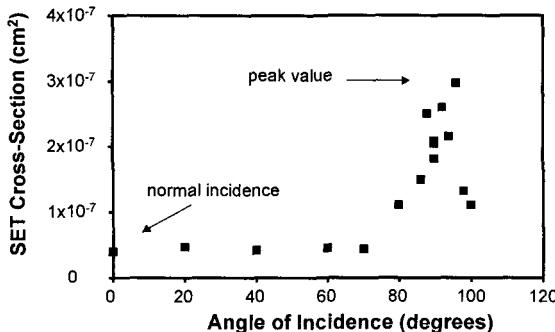


Fig. 5 The SET cross-section for protons incident on a photodiode increases dramatically as the protons approach grazing incidence—an indication that direct ionization is becoming important.<sup>7</sup>

**Figure 6** shows an example of the increase in SET cross-section with the incident angle for the Agilent HCPL5231 optocoupler for three different proton energies. At 60 MeV, the angular dependence is very weak, but for the lower energies the effect is stronger. For 42 MeV protons, the cross-section at grazing incidence is a factor of 10 higher than the cross-section at normal incidence. For 31 MeV protons, the grazing incidence cross-section increases by nearly two orders of magnitude. This dependence indicates that transients caused by direct ionization by protons traversing the diameter of the photodiode dominate at grazing incidence.<sup>7,10</sup> Johnston and coworkers explored the possibility of elastic scattering as the cause for the angular dependence.<sup>11</sup> But, by examining the lower proton energy (higher LET) response of 6N134 optocouplers from two manufacturers and showing the cross-section increase at grazing angles could be as much as 3 orders of magnitude at a proton energy of 15 MeV, Johnston et al. agreed with the conclusion that the angular dependence was due to direct ionization.<sup>8</sup>

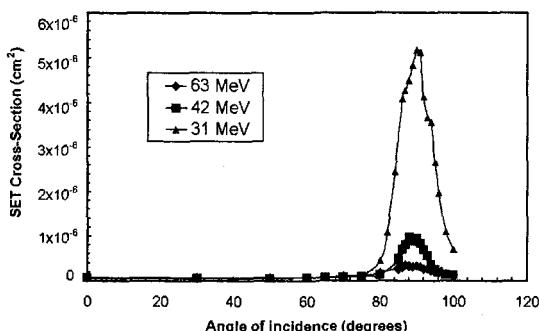


Fig. 6 Effect of incident angle on cross-section of the Agilent HCPL5231 optocoupler for various proton energies.<sup>10</sup>

The initial work by LaBel, et al. correctly identified the sensitivity in high-bandwidth ( $> \sim 5$  MHz) devices, and described the role of direct ionization from protons in the optocoupler's internal receiver photodetector.<sup>6</sup> The error condition results from deposition of charge in the detector that leads to a transient that propagates during the "off" state of the device. Errors can occur when ions initiate transients with sufficient pulse width and voltage amplitude, provided the optocoupler amplifier stage is of sufficient bandwidth to propagate the signal to the optocoupler output.

### 3.3 Heavy Ion-Induced Transients

It is generally accepted that any device that is SET sensitive to protons can also be upset by heavy ions. Optocouplers are not an exception to this ideology. However, because of the monolithic construction of the detector circuitry, as the heavy ion Linear Energy Transfer (LET) is increased, other portions of the design can become sensitive. Johnston et al., investigated the response of the HP 6N134 to heavy ions and showed that in addition to the photodiode, amplifier stage circuitry could be susceptible to ion-induced transients, and transients with longer time signatures would result.<sup>11</sup>

### 3.4 Final Comments on Transient Effects

High-bandwidth optocouplers have demonstrated a significant enhancement in their SET response that can be directly attributed to direct ionization from protons. The degree of enhancement is a strong function of proton LET. At oblique angles, the proton induced error rates are dominated by nuclear elastic and inelastic reaction recoils. The combination of mechanisms poses a significant challenge when calculating space-radiation error rates. In Galactic Cosmic Ray (GCR) dominated environments, the contributions to the gain stages cannot be ignored, and the temporal response of the error may vary.

Also, we note that Reed et al. noticed a significant part-to-part variability in the transient error sensitivity, as indicated in **Figure 7**.<sup>10</sup> Presumably, this follows from the COTS nature of the manufacturing process and part-to-part variability in the gain stages. This has implications for the confidence interval appropriate for a predicted space radiation-induced error rate.

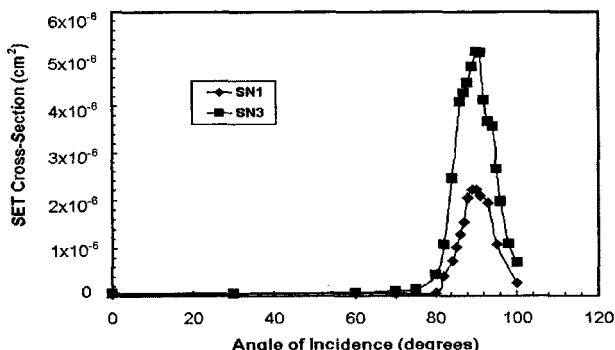


Fig. 7 Example of part-to-part dispersion observed during proton SET characterization of the Agilent HCPL5231.<sup>10</sup>

An assessment of the status of methods and tools to predict space radiation-induced error rates in optocouplers indicates that we are presently limited to factor of 3-5 estimates, and then only with data-intensive characterization efforts. Presently, no single tool exists that is appropriate for the full range of variables associated with these problems, but prospects are excellent for the development of a unified tool. Presently, assessments are under way at NASA Goddard Space Flight Center to examine the suitability of tools such as Geant4, MCNPX, NOVICE, and other expert-level Monte Carlo-based tools for various detector-related SEE concerns.<sup>14,15,16</sup> In parallel, assessments are being made to evaluate the role of charge diffusion and the requirements for simulation tools to assess its role in bipolar microelectronic devices and in detectors. Until the related studies are completed, it is difficult to define the next step required for a solution to rate prediction for optocouplers. Unfortunately, at least in the interim, we expect that these solutions will require comparatively sophisticated computer codes with expert interactions before more user-friendly tools can be made available, at least when better than order-of-magnitude estimates are desired.

## **4.0 Physical Mechanisms for Permanent Degradation**

### **4.1 Introduction**

There are two classes of long-term radiation-induced damage: total ionizing dose (TID) and displacement damage (DD). Electrical performance degradation of an optocoupler occurs when the material properties of one of its components are altered during radiation exposure by one or both of these damage mechanisms.

Damage from TID is caused when electron-hole pairs generated by ionizing radiation are trapped in oxides near the active regions. This will gradually change the performance of an optocoupler component, with the level of change depending on the total ionizing energy absorbed—that is, on the TID.<sup>17,18</sup> Generally, TID changes the characteristics of the materials that make up a component, resulting in gradual parametric degradation and changes in functionality. In most cases, the basic cause of TID degradation is the trapping of charge in a medium (e.g., a field oxide or in an optical medium.)

DD, on the other hand, has a different damage mechanism. The level of performance of active optocoupler components depends on the number of defects in the crystalline lattice—a more pristine lattice will have better performance. The lattice can be damaged when an energetic particle, such as a neutron, electron, proton or heavy ion displaces one or more nuclei within the crystalline lattice, possibly creating electrically active defects. As this damage to the crystalline lattice increases, the device can degrade parametrically, and eventually stop functioning all together. For the most part, because protons are penetrating, strongly interacting and abundant, the proton environment is predominant in considerations of DD effects in shielded space applications. The 1999 Nuclear and Space Radiation Effects Conference (NSREC) Short Course explores DD effects in further detail.<sup>19</sup>

What follows in this section is a brief description of DD effects in LEDs, effects of TID on the passive transmission media, and an examination of the effects of TID and DD on the photodetectors and amplification circuit.

High-bandwidth optocouplers simply stop transferring data once one or more of their components have experienced sufficient performance degradation. So, in this section, we present radiation effects on low band-width devices (current transfer optocouplers), which better demonstrates the basic mechanisms for optocoupler degradation.

#### **4.2 Permanent Degradation in LEDs**

The role of the LED in an optocoupler is to convert current signals into light. For these devices, we are generally more concerned with permanent degradation due to DD. TID is often a second order effect.<sup>3,20,21</sup>

LEDs produce light by means of radiative recombination of injected minority carriers with majority carriers in the depletion region. As such, any damage that decreases the efficiency of radiative recombination or introduces competing processes will degrade device performance. Irradiation by heavy particles such as protons and neutrons can displace nuclei from the crystalline lattice, causing DD. These defects can serve as sites for nonradiative recombination, decreasing the efficiency of the light source.<sup>3</sup> See the 2000 NSREC Short Course for a detailed discussion on DD effects in LEDs.<sup>22</sup>

Displacement damage decreases the LED output power, which in turn can reduce the output current of the photodetector. For current transfer applications, this results in a decrease in the device output current, eventually leading to device failure. For data transfer applications, this will result in inability of the device to transmit data.

Displacement damage in the LED is believed to be the dominant mechanism for most optocoupler failures when exposed to proton-rich environments.

#### **4.3 TID Degradation of Transmission Media**

Although charged particles traversing an optical medium can generate photons, these processes are too weak and the path lengths traversed too short for these events to interfere with signals. For this reason, with respect to transmission media, we are generally more concerned with permanent, cumulative degradation resulting from TID.

Ionizing radiation causes charge to become trapped by defects in the optical medium, creating color centers. Once the color centers form, light transmission efficiency is degraded as the color centers absorb signal photons. The degradation, however, need not be permanent. As is the case for trapped charge in microelectronics, color centers can heal by annealing. The processes of formation and annealing of color centers take place in competition, and optical medium degradation depends on the relative rates of these mechanisms.

Light absorption in the medium will result in a decrease in the photodetector output current for current transfer applications. For data transfer applications, the device ability to transmit data will be compromised. We note that for most, if not all, optocouplers the signal path lengths through the coupling medium are relatively short (<0.5 cm), so these losses due to TID are likely negligible for most optocouplers.

#### **4.4 Permanent Damage in Optical Detectors**

Optical detectors in optoelectronic devices function by detecting the photocurrent generated by a photon with energy greater than the semiconductor bandgap. For this reason, any damage to the semiconductor that changes its global properties, or that degrades the semiconductor's ability to carry a current will potentially compromise the detector's efficiency.

As TID accumulates, photodetectors degrade, with leakage currents increasing up to several orders of magnitude for doses up to 1 Mrad(Si). DD can degrade carrier lifetime, which reduces responsivity and gain, thereby changing the output current. Both TID and DD increase background noise.

While there are several degradation mechanisms for photodetectors when exposed to a radiation environment, many detectors show remarkable robustness to surviving space radiation environments.

#### 4.5 Permanent Degradation of CTR

TID and DD can severely degrade the performance of an optocoupler. The most studied effect is how radiation degrades Current Transfer Ratio (CTR), defined as the ratio of the output current ( $I_C$ ) to the input current ( $I_F$ ) (See **Figure 8**).

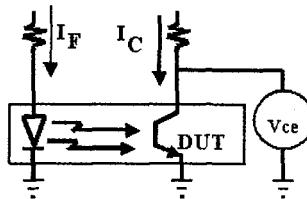
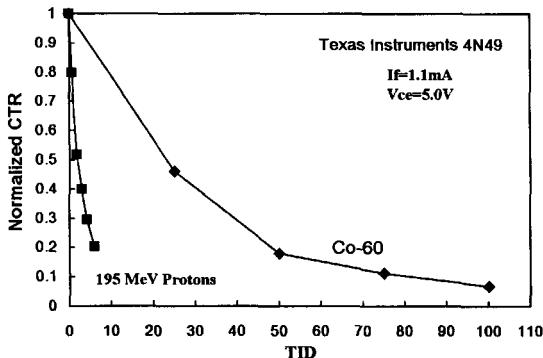


Fig. 8 Schematic showing experimental setup for measure CTR degradation.

Assessing radiation degradation of CTR is complicated by several factors that include anneal and temperature effects, lack of understanding of how physical degradation mechanisms manifest themselves as device failures, part to part variability, and others. Some of these concerns need to be addressed when estimating radiation exposure levels, others during the testing phase, and others must be considered in combination with radiation-induced degradation estimates to give overall performance. We will give a brief review of several of these complications.

##### 4.5.1 Gamma Rays versus Protons

The observed radiation-induced degradation results from a combination of ionizing dose and displacement damage mechanisms, each affecting the individual optocoupler components differently.<sup>4,7</sup> **Figure 9** compares CTR degradation for gamma-ray exposures of a Texas Instruments (TI) 4N49 to that for 195 MeV proton exposures. Proton irradiations cause significantly larger degradation than gamma-ray exposures at equivalent doses. This type of optocoupler response is due to the greater amount of displacement damage occurring for protons.<sup>4</sup>

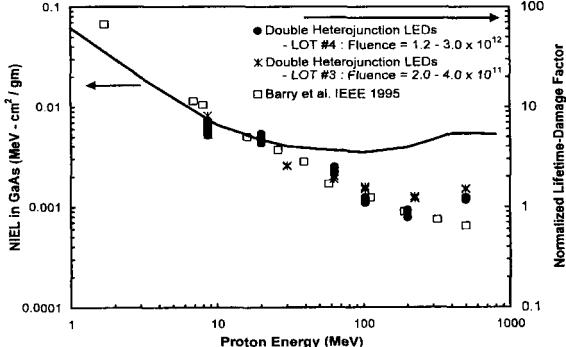
Fig. 9 Gamma and 195 MeV proton irradiations of Texas Instruments 4N49.<sup>7</sup>

#### 4.5.2 Proton Energy

The rate of degradation not only depends on the radiation type, but also on the energy of the protons used during testing. This energy dependence is not well understood, making it very difficult to estimate the amount of degradation that would occur when the device is exposed to a spectrum of proton energies—the energy of the protons in space radiation environments can vary by over an order of magnitude.

In this section we will review radiation degradation results on LEDs—for most optocouplers, the LED is the most sensitive component to displacement damage—to qualitatively show how the damage factor could depend on proton energy and to demonstrate the lack of consistency between the damage factor and Non-Ionizing Energy Loss (NIEL).

**Figure 10** plots the normalized lifetime-damage factors ( $K$ ) for single heterojunction LEDs to NIEL as calculated by Burke et al.<sup>24,25</sup> (solid curve), as well as experimental results on amphotERICALLY doped<sup>26</sup>, double-heterojunction<sup>27</sup>, and single-heterojunction<sup>27</sup> LEDs. For this plot, the NIEL values are normalized to the values at 10 MeV. There is an inconsistency between the experimentally-determined damage factors for LEDs and theoretical calculations for NIEL.

Fig. 10 Lifetime-damage-factor measurements for double-heterojunction devices (scaled to the right abscissa), normalized to agree with calculated NIEL values (solid line—scaled to the left abscissa) for 10 MeV protons.<sup>27</sup>

Significant error could occur in a calculation that uses NIEL to determine an equivalent fluence for a single test energy, where this equivalent fluence is expected to produce an equivalent amount of damage to that produced by a spectrum of particles with varying energy.

For example, **Figure 11** compares equivalent test fluences for 50 MeV or 200 MeV protons for a five-year satellite mission in a 600 km x 90 degree circular orbit about the earth. The equivalent fluence is given for NIEL and for the trend given by experimental data in **Figure 10**. The figure clearly shows how disastrous it could be if NIEL is used to compute the equivalent test fluence for this mission. Normalizing using NIEL correlation at 200 MeV would lead to underestimation of the damage by a factor of 7 for 50 mils of Al shielding. However, normalizing using NIEL at 50 MeV shows a factor of 3 underestimation, which is less dramatic, but significant nonetheless.

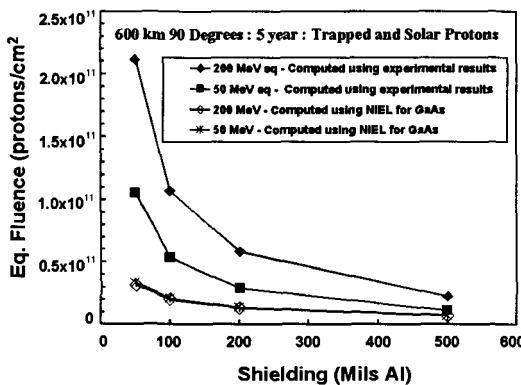


Fig. 11 On-orbit degradation for a mission can be predicted with a given fluence of protons, regardless of energy—provided displacement damage is proportional to NIEL.<sup>27</sup>

#### 4.5.3 Application specific testing

A testing approach that is targeted towards a specific application is necessary to accurately determine the degradation expected for that application.<sup>5,7</sup> For example, the data represented by solid filled symbols connected by solid lines in **Figure 12** show a comparison of the CTR degradation at two different loads (RL) for the same device ( $V_{CE}=0.3\text{V}$  for both loads). The CTR for the case where the load was 2.7 ohm degraded by almost 50% of its original value after an exposure of  $1 \times 10^{11}$  protons/cm<sup>2</sup>, while the degradation for a 1.0 kohm load was only 8%.

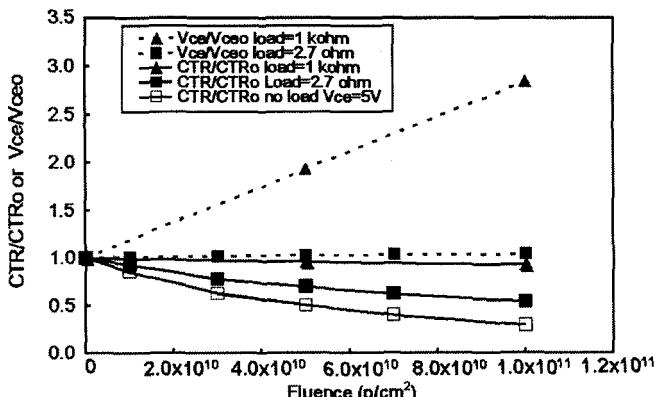


Fig. 12 Plot of either normalized CTR (solid lines) or normalized  $V_{CE}$  (dashed lines) for a 4mA forward current. This shows the load dependence on the radiation response. It also demonstrates that testing at a fixed  $V_{CE}$  would significantly over predict the CTR degradation.<sup>7</sup>

The dashed lines in **Figure 12** show the radiation-induced change of photodetector collector-emitter voltage ( $V_{CE}$ ) with fluence for each load. For the 2.7 ohm load case  $V_{CE}$  remained constant at 0.3 V. In the case where the load is 1.0 kohm,  $V_{CE}$  increased with increasing fluence. Radiation degraded the output of the LED, as evident in the 2.7 ohm loading, but for the 1.0 kohm loaded case, the output degradation was compensated by an increase of the emitter-collector voltage. These data clearly show that an erroneous estimation of CTR degradation could occur if application specific testing was not carefully performed.

Finally, the data represented by the unfilled squares in **Figure 12** show the CTR degradation for a fixed  $V_{CE}$  of 5 V. The last data point on this curve shows that the CTR has degraded to 29% of the original value. Compare this to 92% of the original value when  $V_{CE}$  was allowed to change (1 kohm load). Data collected at  $V_{CE} = 5$  V over predicts the degradation in the 1 kohm load case by a factor of 4.6. Several publicly accessible databases and journals give data collected at fixed  $V_{CE}$ . If these data are used for certain applications, they could significantly over predict the degradation.

#### 4.5.4 Part-to-Part Variability in Radiation Response

Since optocouplers are typically COTS hybrids, it is not surprising that they often exhibit large part-to-part variability. Some of this variation is due to the complication of having several different components that can be sensitive to various effects. **Figure 13** shows data collected on three Mitel 3C91C optocouplers. At certain fluences there is over a factor of two variation in the response to radiation. This optocoupler is manufactured as a radiation-hardened product, and the internal components were all selected from the same device lot. These hybrids do not contain a light pipe to guide the light between the LED and the detector, so the variation must be due to the differences in the response of one of the active components.

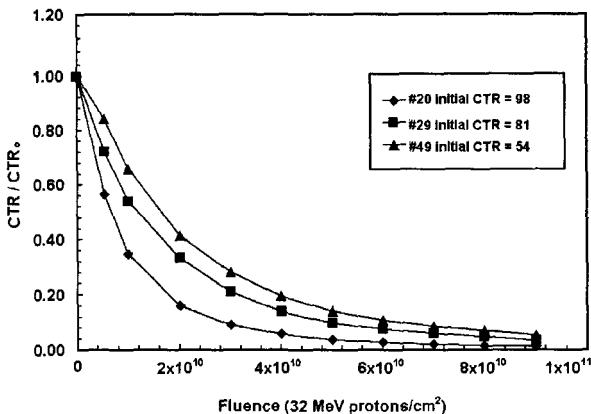


Fig. 13 Demonstration of part-to-part variability of CTR degradation within a single lot.<sup>10</sup>

Another reason for part-to-part variations (and the most difficult to characterize) is the flexibility the vendor has in selecting the components internal to the optocoupler. **Figure 14** gives CTR degradation data from two lots of the Micropac 4N49. These data show as much as an order of magnitude variation in the sensitivity between the two “lots”. As with all COTS devices, knowledge of the manufacturing process is very limited, adding a significant risk to using these types of devices.

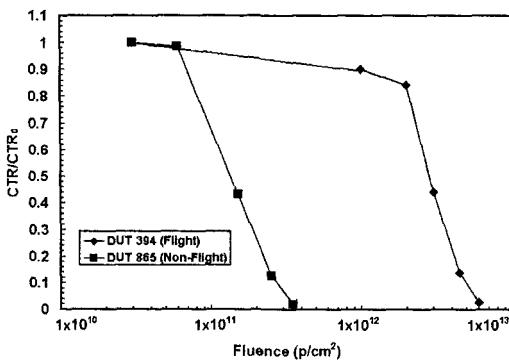


Fig. 14 Demonstration of lot-to-lot variability of CTR degradation.<sup>10</sup>

#### 4.5.5 Anneal of Displacement Damage

Injection current annealing of displacement damage-induced degradation of LED light output was first reported by Barnes et al. and then further discussed by Johnston et al.<sup>3,12</sup> Annealing has also been observed in optocouplers.<sup>10</sup> **Figure 15** shows the recovery of the collector current under two annealing currents (1 mA and 10 mA) for three measurement forward currents (1, 5, and 10 mA) for an Isolink 4N49. The data connected with the solid lines were obtained after the device was annealed at 10 mA (unfilled symbols), while the data represented by the filled symbols were taken at 1 mA annealing forward current. The collector

current is normalized to the pre-irradiation values. The abscissa is the amount of charge in coulombs that has passed through the LED during the annealing period. For annealing at 10 mA, the time to reach 1800 coulombs is 50 hours, while the time to reach this charge at 1 mA is 20.8 days. The recovery factor shown in the legend gives the ratio of the collector current after 1800 coulombs anneal to post-irradiation (prior to the anneal step) values for the collector current.

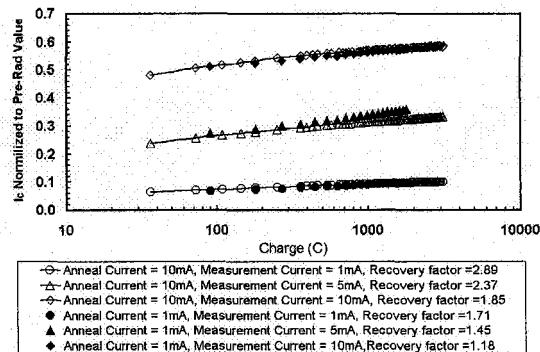


Fig. 15 Injection current annealing effect on collector current at two forward currents for three application currents.<sup>10</sup>  
The data is normalized to the pre-irradiation collector currents.<sup>10</sup>

First note that for the annealing conditions between 100 and 1800 coulombs, the amount of recovery is approximately the same for the 1 and 10 mA annealing conditions for all three test conditions. This implies that an accelerated annealing test could be used for these annealing periods, reducing the time to determine the amount of recovery by a factor of 10. If this accelerated annealing approach could be generalized, then one could use it to estimate the annealing occurring over long mission times. However, in order to generalize this accelerated annealing test, more data on other part types are needed. Also, for missions with long annealing times, studies out to greater integral charge values will be required. This accelerated annealing approach should be studied in more detail before being implemented in a risk assessment approach.

The second interesting point that these data show is the collector-current recovery-factor (the ratio of the annealed collector current to the post-irradiation value) is dependent on the forward current used for the measurement and the annealing current. The recovery factor is also dependent on the anneal time. All of these are application-dependent issues.

Annealing should be minimized while collecting CTR degradation data over the test fluence. This can be best achieved if the optocoupler “on-time” (when the LED is illuminating the photodetector) is minimized and the forward current is minimized.

#### 4.5.6 Temperature Effects Impact CTR

Temperature effects must also be considered when determining the likelihood of optocoupler survival when exposed to a radiation environment.<sup>10</sup> The data in Figure 16 shows that for an Isolink 4N49 there is a 30 to 40% decrease in the CTR when the device is warmed from room temperature (~23°C) to 100°C.

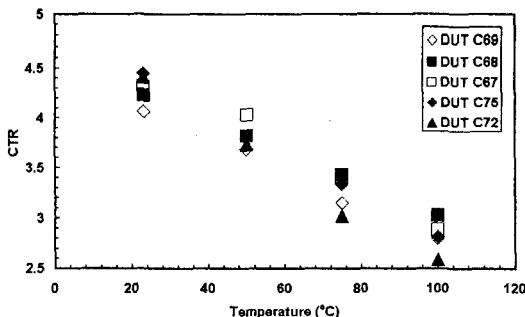


Fig. 16 Temperature effects on CTR for an Isolink 4N49 optocoupler.<sup>10</sup>

#### 4.6 Final Comments on Permanent Degradation

Despite the ominous list of nightmares above it is possible to take a conservative approach for estimating optocoupler CTR degradation when exposed to space radiation. This approach is outlined by Reed et al.<sup>10</sup> The risk assessment techniques described by Reed require significant margin, as much as a factor of 50 for certain scenarios.<sup>10</sup>

### 5.0 Conclusions

Space radiation-induced performance degradation of optocouplers was first reported in 1996 and 1997. In 1996, Rax et. al reported on the first inflight anomaly that was reportedly caused by CTR degradation of a 4N49 optocoupler.<sup>4</sup> The following year LaBel et. al reported on the first space flight anomaly that could be traced to transient effects in a 6N134 high-bandwidth optocoupler.<sup>6</sup> Since that time a significant amount of effort has been put into solving some of the mysteries that exist when assessing the space worthiness of optocouplers. The overriding result that has come out of this research is that there is no “quick-fix”, “one-size fits all” solution. Every optocoupler must be assessed against the environment that it will be exposed to and the function that it will be performing. We hope that, by using the information provided in this paper and good engineering judgment, radiation effects experts can work their way through the difficult problem of space-qualifying an optocoupler.

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## RADIATION EFFECTS IN CHARGE-COUPLED DEVICE (CCD) IMAGERS AND CMOS ACTIVE PIXEL SENSORS

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This review concerns radiation effects in silicon Charge-Coupled Devices (CCDs) and CMOS active pixel sensors (APSs), both of which are used as imagers in the visible region. Permanent effects, due to total ionizing dose and displacement damage, are discussed in detail, with a particular emphasis on the space environment. In addition, transient effects are briefly summarized. Implications for ground testing, effects mitigation and device hardening are also considered. The review is illustrated with results from recent ground testing.

*Keywords:* CCD; APS; radiation; damage

### 1. Introduction

This review looks at radiation effects in silicon charge-coupled device (CCD) imagers. It also makes a comparison with effects in CMOS active pixel sensors (APSs) - which are emerging as a rival technology for many applications, particularly where low cost or high radiation tolerance are needed.

Both the CCD and the APS consist of an array of imaging detectors (pixels), either photodiodes or MOS capacitors (photogates). The main difference is in the way the collected photo-generated charge is readout. In the CCD the charge is transferred from one pixel to the next (and eventually to an output amplifier) by splitting the gate electrodes into several phases (usually 2, 3 or 4) and clocking these phases in an appropriate pattern (figure 1 shows a schematic structure and figure 2 a typical clocking pattern). In contrast, the active pixel sensor uses CMOS shift registers and transistor switches to connect each pixel in turn to the output. In order to buffer the detector from the high capacitance of the address lines it is necessary to have an amplification stage in each pixel (hence the term 'active'); usually there will also be an amplifier associated with each column. Figure 3 shows a simplified schematic. With the flexibility offered by CMOS fabrication it is often possible to include additional features, such as an analog-to-digital convertor (ADC) on-chip.

CCD formats (number and size of pixels) vary widely, from small (e.g. 14 x 14 pixels) detectors for high speed tracking or wavefront sensing to large (e.g. 9216 x 9216 pixels<sup>1</sup>) for scientific imaging. Large format APS arrays (e.g. 13.85 million pixel) are also starting to become available.<sup>2</sup> CCDs and APSs are extremely sensitive detectors for visible photons either in 2-D formats for use in 'cameras', or as 1-D (linear) devices for spectroscopy or scanning applications. Many of these applications will involve exposure to particle or gamma radiation. For example, military, scientific (e.g. high energy physics) and space (star trackers, acquisition and tracking sensors, astronomical and Earth observation instruments).

The sensitivity, which makes these solid state array detectors so useful, also makes them vulnerable to radiation-induced performance changes. Both types of imager suffer from the permanent effects of:

- total ionizing dose (due to charged particles, x-rays and gamma rays).  
This affects the MOS structures (producing a charging of the gate insulator and build-up of interface traps)
- displacement damage (usually due to heavy particles such as protons and neutrons).  
This creates defects in the crystal lattice, and hence dark current generation and charge trapping centers.

In addition, devices will show transient 'events' due to ionizing radiation which deposits charge in the photodetectors. Although these transient events will cause contamination in an image, they are short-lived and only occur in the exposure in which they were generated.

CCD design and operation have recently been reviewed in books by Janesick<sup>3</sup> and Theuwissen.<sup>4</sup> Radiation effects in CCDs have been discussed in<sup>5, 6, 7</sup> and<sup>8</sup>. In the following sections the topics of total ionizing dose damage, displacement damage and transient effects will be discussed in turn. In each section suggestions will be made concerning implications for ground testing, effects mitigation and device hardening.

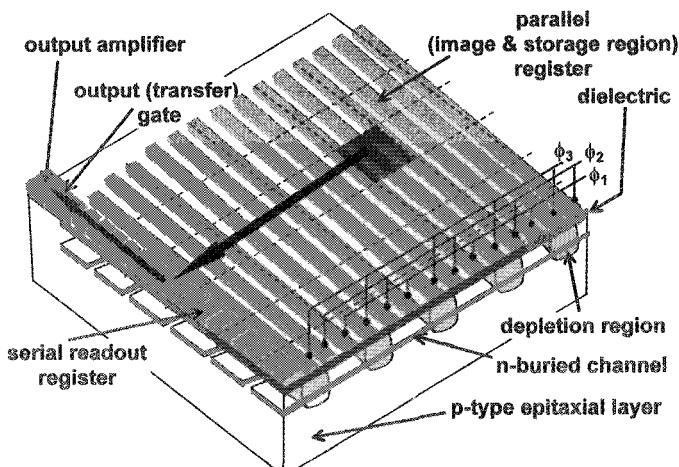


Fig. 1. Schematic of a typical 3-phase n-buried channel CCD.

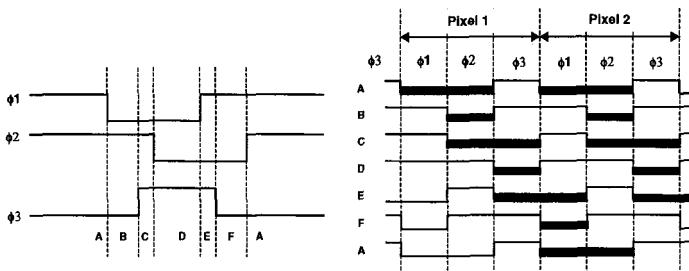


Fig. 2. Typical clocking pattern for a 3-phase CCD. The thick lines indicate stored charge.

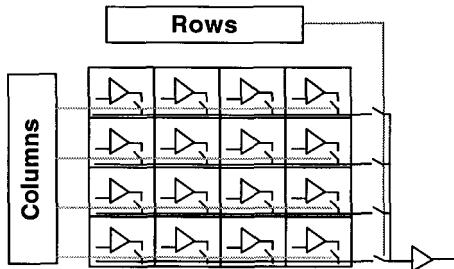


Fig. 3. Simplified schematic of a CMOS active pixel sensor.

## 2. Damage due to Total Ionizing Dose (TID)

Both CCDs and APSs use dielectric layers, such as silicon dioxide, to isolate gate electrodes from each other and from the silicon. In the case of the CCD the gate isolation is typically a dual layer of  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$  (which acts as an etch-stop during processing of the CCD electrodes). The total thickness is of order 150 nm. For an APS the gate oxides in typical CMOS processes are thinner (on the order of a few nm) but field oxide isolations can be similarly thick. Ionizing radiation causes the generation of electron-hole pairs in these layers, the number of pairs increasing linearly with the thickness. A fraction of the charge will become trapped in the dielectric and another fraction will release hydrogen and induce interface traps. The basic mechanisms of total dose damage have been reviewed by, for example, Braunig and Wulf<sup>9</sup> and Schwank.<sup>10</sup> Damage prediction is straightforward since it is usually proportional to total ionizing dose, measured in rd(Si) or Gy(Si) - independent of the type of radiation - though saturation effects can sometimes be seen at high doses (of order 1 Mrd). In general, the response of MOS circuits is sensitive to the dose rate of the irradiation (e.g. in rd/s) and there are time dependent effects (such as annealing of trapped holes and slow build up of interface traps). In CCD imagers and APSs these dose rate effects are not usually pronounced, though they can sometimes be observed.

The gate dielectrics have a capacitance (decreasing with thickness) and so the trapped charge produces a shift in the 'effective' voltage applied to the gate (known as the flatband voltage shift). The other effect of permanent ionization damage, as mentioned above, is the build-up of interface traps and this increases dark current generation at those regions of the

surface (that is, the Si/SiO<sub>2</sub> boundary) that are depleted. The surface has to be depleted because generation processes (which take place by carrier emission) only dominate over recombination (capture) processes when the free carrier concentrations are significantly less than their thermal equilibrium values.<sup>11</sup>

## **2.1. Radiation-induced surface dark current due to TID**

Interface traps have energy levels within the silicon bandgap and act as centers for the generation of surface dark current in both CCDs and APSs. In a full frame or frame transfer CCD the generation is at the depleted surface under the active clock phase (held high in an n-channel CCD so as to collect charge) and in an APS (or an interline transfer or a linear CCD) at the depleted surface of the photodiode (or, with some types of APS, under the photogate). The build-up of interface traps can be a slow process, for example involving the diffusion of hydrogen through the oxide. After a cobalt-60 irradiation CCD dark current is often found to increase (by a factor of 2 or 3) over time periods of several weeks or months, though it can be accelerated by baking at 100°C for 168 hours (as is done for routine MOS device testing for 'rebound', as in ECSS Basic Specification 22900 and MIL-STD-883 method 1019.4<sup>12</sup>). In fact 168 hours may not always be needed and a 24 hour bake can be sufficient.<sup>13</sup> The final value for the increase, for the image region of a frame transfer CCD, is typically  $\sim 1 \text{ nA/cm}^2/\text{krd(Si)}$  at 20°C, assuming 20 μm x 20 μm pixels (corresponding to  $\sim 2.5 \times 10^4$  electrons/pixel/s). Some early CCDs, with thick oxide channel stop isolations, showed much larger reverse annealing<sup>14,15</sup> but this is rarely a problem today.

The dark current increase is often more for biased devices than for unbiased, but bias dependence depends on the device details. The dark current is normally fairly uniform across the CCD (though there will be statistical pixel-to-pixel fluctuations).

For regions of the CCD which are masked so as to form a storage region (in a frame transfer CCD) or to form dark reference pixels, the radiation-induced surface dark current can be increased (by a factor  $\sim 2$  or 3) because of hydrogen incorporated into surface layers during processing. Sometimes a CCD is fitted with an external (non-deposited) store shield for this reason. In addition, hydrogen (or a similar interface trap enhancing species) can be generated at the periphery of the device, outside the active region and can sometimes diffuse in to give an increased dark current in the first and last columns. Hence it is advisable to avoid using these regions in any image processing.

Fortunately, for many applications, the above discussion will not be applicable because the CCD can be operated in inverted mode where surface dark current is negligible. In this mode (sometimes called multi-phase pinned or MPP), all the clock low levels are lowered with respect to the substrate voltage to the point where the surface becomes inverted and holes from the substrate and channel stop regions migrate to the surface and keep the interface traps filled. Usually the surface dark current will then be negligible, although if the surface is not completely inverted (e.g. if regions at the edge of a pixel are left non-inverted) then the dark current will be slightly increased. As will be discussed in the next section, if the total dose is large, usually several tens of krd(Si), then the flatband voltage shift can be high enough for the surface to become non-inverted. In this case the full surface dark current will appear.

A drawback of using MPP mode is that an implant is needed to create a potential well for

storing the charge when all the clocks are low. This results in a reduced full well capacity (unless special 'advanced MPP' structures are used). A compromise solution is to not have an MPP implant but to operate all the clock phases except one in inverted mode and to periodically swap the phase which is used as a barrier. If the holes under this phase are trapped for longer than the time between swaps then the dark current is significantly reduced. This is known as dynamic dark charge suppression or dither clocking and has been described by Burke and Gajar.<sup>16</sup> As the hole trapping time increases as the CCD temperature is decreased, the reduction in surface dark current tends to be larger. This dynamic suppression happens naturally during continuous readout of the storage region of a frame transfer CCD.

In linear and interline transfer CCDs, which use photodiode detector elements, the inverted mode can still be used and the detectors are usually referred to as 'pinned photodiodes'.

In CMOS active pixel sensors it is not possible to invert the surface but the radiation induced dark current is still very small. With photogate structures the surface dark current is reduced because the gate oxide is thin. A value of 1-2 pA/cm<sup>2</sup>/krd(Si) has been reported<sup>17</sup> for one such device at room temperature. If a photodiode is used then this can have a small area (provided that it can be arranged to collect charge from the whole pixel area) and the surface dark current is again reduced.<sup>18</sup> In one case<sup>19</sup> it has been observed that the dark current, though small, is non-uniform across the array (see figure 4). Again, values of 1-2 pA/cm<sup>2</sup>/krd(Si) are typical for biased devices: a value of 310,000 electrons/pixel/s (3 nA/cm<sup>2</sup>) was found after 5.3 Mrd<sup>19</sup> at 20°C and slightly lower values were found by Bogaerts et al.<sup>20</sup>

Surface dark current varies strongly with temperature, hence cooling the detector is an effective way of improving performance. An empirical relation for the change is

$$\text{Dark current} = \text{constant} \times \exp(-E_{\text{act}}/kT) \quad (1)$$

Where the activation energy,  $E_{\text{act}}$ , is in the range 0.63 - 0.65eV (though for dither clocked devices the effective activation energy will be increased).

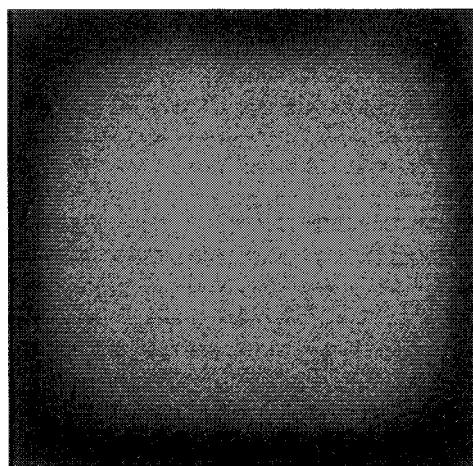


Fig. 4. Dark current for a CMOS APS (Fiffactory STAR-250, 25 μm x 25 μm pixels) after 100 krd(Si) biased cobalt-60 irradiation, giving a peak increase (center of chip) of 0.42 nA/cm<sup>2</sup> at 25°C

## 2.2. Flatband voltage shift

The result of an ionizing radiation-induced flatband shift is to change the effective voltages applied to the device. In a typical 'commercial' CCD the flatband shift is roughly 0.1 V/krd(Si) when the device is biased during irradiation and a half to one quarter that when not biased (the difference being due to the effect of electric field on charge yield and transport in the dielectric). This shift will tend to increase the clock voltage differential (relative to substrate) at which the surface becomes inverted and will also tend to make the output node less attractive to clocked charge and to change the operating point of the output amplifier (which may alter the gain).

Figure 5 shows the shift in inversion point for a typical CCD. If the clock low voltage is not selected appropriately then it is possible for the device to come out of inversion mode after a high total dose and then to exhibit increased dark current.

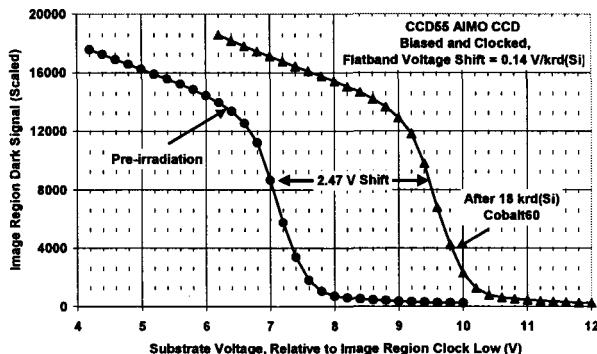


Fig. 5. Shift in inversion point for an advanced inverted mode (AIMO) CCD55 from E2V Technologies, UK, after 18 krd(Si) cobalt-60. The dark current has been scaled so that the pre-and post radiation dark currents are comparable.

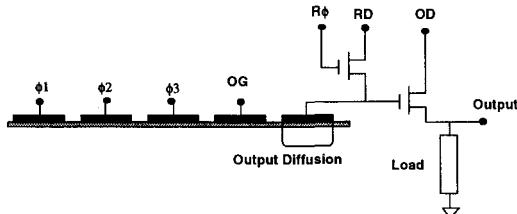


Fig. 6. Output circuit for a typical CCD

Figure 6 shows a typical CCD output circuit. The effect of total dose will depend on the CCD design and the allowed voltage margin. For TID higher than  $\sim 10$  krd(Si) it is common for the output bias voltages ( $V_{OD}$  and  $V_{RD}$ ) to need increasing and sometimes for the readout clocks to be lowered (or else charge cannot pass over the output gate (OG) into the amplifier - resulting in a complete loss of imaging capability). As a 'rule of thumb', 1-2 V voltage shift can be accommodated by choosing optimal biases prior to irradiation (which may be different from the datasheet values) and 2-4 V shift requires bias adjustment during irradiation.

CCD hardening is possible by thinning the dielectric (though this may have an adverse affect on device yield) or by using a hardened oxide process. Use of a dual  $\text{SiO}_2/\text{Si}_3\text{N}_4$  dielectric can be advantageous since electrons trapped in the nitride can balance the charge from holes trapped in the oxide.

For a CMOS APS the gate oxide flatband voltage shifts will be much smaller because of the thinness of the oxide and are generally not an issue. For example, a 5.3 Mrd biased cobalt-60 irradiation of one device<sup>19</sup> showed only 80 mV shift. A change in APS responsivity was found in one case<sup>20</sup>, probably due to TID effects.

### **2.3. Parasitic leakage currents in CMOS APS devices**

For APS devices a much more important effect than gate oxide flatband voltage shift is the possibility that thick field oxide isolation regions can become inverted and so provide a parasitic leakage path leading to increased power consumption. The area of depleted silicon at the surface may also increase leading to greater thermal dark current. As for all oxide effects, there is the possibility of post-irradiation annealing.

Fortunately, even in commercial devices, it is possible to choose radiation tolerant CMOS libraries for device layout and so achieve 'hardening by design'.<sup>21</sup> By incorporating enclosed 'gate all around' transistors it is possible to eliminate field oxide leakage effects. Examples of such devices have been referred to above<sup>17,19</sup>. The drawback is that special device structures will reduce the sensitive area (the fill factor) of the device and hence the signal-to-noise performance. A fill factor of 45% can still be achieved in some cases (e.g. the APS in<sup>19,20</sup>).

At the same time, it is possible to harden against single event latch-up (SEL) by using a thin epitaxial layer, guard rings and frequent body ties. SEL has not been observed in the hardened device studied by Marshall et al.<sup>22</sup> (at a maximum LET of 106 MeV/mg/cm<sup>2</sup>), nor in the STAR-250 APS (maximum LET of 68 MeV/mg/cm<sup>2</sup>). The drawback of using a thin epitaxial layer is a reduction in red response (for a front illuminated device).

### **2.4. Testing for total ionizing dose effects**

Total dose testing of detector arrays is almost always carried out using cobalt-60 sources. Since characterizing the detector can be time consuming, it is useful to use a low dose rate (e.g. in the range 1-10 krd/hour) so that any short-term annealing does not affect the measurements. Fortunately, post-irradiation annealing tends to take place over weeks and months after irradiation and is, in any case, small for flatband voltage shift. Any reverse annealing of surface dark current can be accelerated by a bake at 100°C, as mentioned above.

Total dose damage is dependent on the irradiation bias and it is usual for both biased and unbiased devices to be tested (with biased usually being worst case).

## **3. Displacement Damage**

Displacement damage is caused by particles which collide with the silicon atoms within the crystal lattice of the detector array and create vacancy-interstitial pairs. Most of these will recombine after the collision but some will migrate through the lattice and form stable defects

such as the divacancy, V<sub>2</sub> (two vacancy complex) and the E-center (phosphorous-vacancy complex).<sup>23</sup> These defects have energy levels within the silicon bandgap and can act as dark current generation centers (in CCDs and active pixel sensors) and minority carrier traps (which cause degradation in charge transfer efficiency in CCDs). Most of a particle's energy loss occurs by ionization, only about 0.1% goes into producing displacements.

The collision process takes place by the initial particle (e.g. a proton or a neutron) displacing a silicon atom and creating what is known as a primary knock-on atom or PKA. The recoil energy given to the PKA depends on the particle type and energy and can be worked out from the kinematics of the collision. For protons and neutrons the maximum energy, T<sub>max</sub> that can be transferred to the PKA is given by<sup>23,24</sup>

$$T_{\max} = \frac{4Mm}{(m+M)^2} E = 0.133E \quad (2)$$

where E is the kinetic energy of the incident proton, m the proton mass and M the mass of a silicon atom. For low energy protons (less than a few tens of MeV) most of the interactions are via elastic Coulombic (Rutherford) scattering and most of the protons carry on in the forward direction, imparting very little energy to the PKA. In fact the probability of creating a PKA with energy T is proportional to 1/T<sup>2</sup><sup>24</sup> so that the energy spectrum of the proton-induced PKAs falls sharply with increasing energy and the average PKA energy is low (in fact it stays ~ 200 eV for a wide range of proton energies<sup>23</sup>). This means that the PKAs generally do not have enough energy to displace other silicon atoms, a process which requires a PKA energy of several keV (Wood et al.<sup>25</sup> give a value 1-2 keV and Lindstroem<sup>26</sup> has recently quoted 5 keV). Hence proton elastic collisions tend to produce isolated defects.

As the incident proton energy increases above ~ 10 MeV there is an increasing chance of an inelastic collision (nuclear spallation reaction). These produce higher energy PKAs which can in turn displace other silicon atoms to produce a cascade of defects. If the PKA energy exceeds about 12 keV then multiple cascades can be formed. In these cascades and multiple cascades the lattice defects tend to be grouped together in clusters. Displacements will carry on taking place (with the production of vacancy/interstitial pairs) until the energy of the silicon atom(s) falls below the threshold energy for displacements (which, for silicon is ~ 20-25 eV<sup>23</sup>).

Electrons always produce isolated point defects since they can only impart a very small energy to the PKA and the same is true for cobalt-60 gamma rays where the displacement damage is primarily due to the production of Compton electrons having a maximum energy of only 1 MeV.

Neutron irradiation, on the other hand, gives a PKA spectrum which is much flatter. In fact, at low neutron energies the collisions approximate to hard sphere interactions, leading to a perfectly flat spectrum up to the maximum transmitted energy given in equation (2). This means that neutrons tend to give much more cluster damage than do protons. It may seem, therefore, that the nature of the displacement damage will depend on the particle type and energy. However, as Wood et al.<sup>25</sup> first showed, all cascade damage is very similar, independent of how many cascades or sub-cascades there are. It may still be, though, that the defects created in clusters are different from isolated point defects. Nevertheless, the usual next step is to assume that the nature of *all* defects is independent of whether they are isolated

or in clusters and this leads to the important hypothesis that damage is proportional to the total energy (per particle per  $\text{cm}^2/\text{g}$ ) that goes into displacements - known as the non-ionizing energy loss, or NIEL.

The vacancies and interstitials produced are mobile and will migrate through the lattice. Roughly 90% will recombine, leaving no permanent effect but, as mentioned above, the remainder can form stable defects. Although the number of these stable defects is difficult to predict from first principles, we can expect that the final damage will always be proportional to the amount of initial damage and also to the electrical effect on the device. Hence NIEL scaling implies that we have a universal relation:

$$\text{device damage} = k_{\text{damage}} \times \text{displacement damage dose} \quad (3)$$

Where  $k_{\text{damage}}$  is a damage constant dependant on the device and the parameter affected and the displacement damage dose (DD) is the product of the NIEL and the particle fluence. DD plays the same role for displacement damage as total dose does for ionization damage<sup>27</sup>. In the case where there is a spectrum of particle energies the DD has to be calculated by integrating over the particle differential energy spectrum,  $d\phi(E)/dE$  (and summing the contributions from the different particle types if there are more than one):

$$DD = \int NIEL(E) \frac{d\phi(E)}{dE} dE \quad (4)$$

Since the device effects will normally depend on the characteristics of the defects involved, NIEL scaling will only be valid if the concentration of the dominant defect (for the parameter concerned) is similar for both point and cluster damage. Huhtinen<sup>28</sup> has recently shown that this is valid for the divacancy but it might be expected (for example) that higher order vacancy defects ( $V_3$ ,  $V_4$  or  $V_5$ ) may be more common in cluster regions (and relatively more numerous after neutron damage). Nevertheless, NIEL scaling is always a good first step in allowing for the incident particle spectrum.

NIEL in silicon has been computed as a function of energy by several authors. Figure 7 shows a compilation of the available data. The proton data of Dale et al.<sup>29</sup> is a slightly revised version of earlier work by Burke<sup>30</sup> and has been extrapolated to higher energies by Huhtinen and Arnio.<sup>31</sup> This data is in good agreement with recent Monte Carlo simulations by Jun.<sup>32</sup> Other work by Akkerman et al.<sup>33</sup> gives somewhat higher values below 30 MeV but lower values above 60 MeV. The neutron data is from ASTM E 722-94.<sup>34</sup> Recent work by the authors suggests that bulk damage in CCDs more closely follows the Dale et al. curve.

Akkerman et al.<sup>33</sup> have also calculated the NIEL due to cobalt-60 gamma rays. Behind a few mm of Aluminum shielding, when the NIEL has reached an equilibrium value, they give a NIEL value of  $1.07 \cdot 10^{-7} \text{ MeV}\cdot\text{cm}^2/\text{g}$ .

The NIEL concept is particularly useful if ground testing is performed at one energy (e.g. 10 MeV) and results need to be extrapolated to the use environment (e.g. space). Rather than being quoted in  $\text{keV}\cdot\text{cm}^2/\text{g}$  (or  $\text{MeV}\cdot\text{cm}^2/\text{g}$ ), the displacement damage dose is often given as an equivalent fluence of 10 MeV protons or as the displacement damage cross section, in  $\text{MeVmb}$  ( $100 \text{ MeVmb} = 2.144 \text{ keV}\cdot\text{cm}^2/\text{g}$ ).

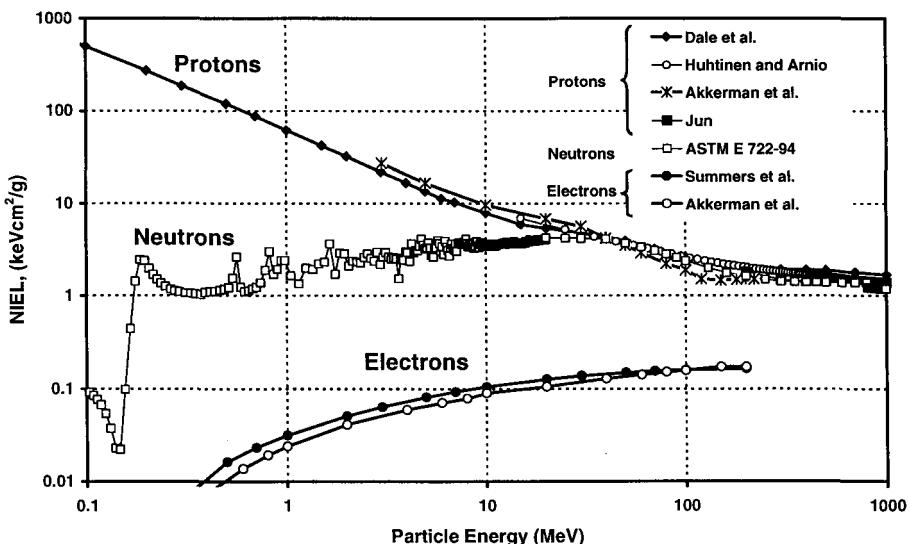


Figure 7 NIEL data for protons, neutrons and electrons in silicon

### 3.1. Bulk Dark Current

As mentioned above, displacement damage causes the formation of dark current generation centers in the silicon bandgap. These lie in the bulk of the depletion region (rather than at the surface) and give rise to what is known as bulk dark current. The most effective defects (giving the highest dark current) have an energy close to mid gap. The bandgap in silicon is 1.1 eV and so common radiation-induced defects such as the divacancy and the E center, which have energies of  $\sim 0.44$  eV below the conduction band can be important (though any defect at  $\sim 0.55$  eV would be more effective). The main feature of displacement damage induced bulk dark current is that it is very nonuniform as illustrated in figure 8. To characterize this dark current it is necessary to measure the distribution of pixel values.

Two typical examples from recent CCD measurements are shown in figure 9. The histograms have a broad tail extending to large signals. Although the mean dark signal increase due to displacement damage is  $\sim 8,000$  electrons/pixel/s, the largest dark current 'spikes' are an order of magnitude greater. These large amplitude signals are due to inelastic proton collisions which deposit a large amount of energy and also to those elastic collisions which happen to occur in a region which has a high electric field. The second mechanism tends to be more important in CCDs and is known as field enhancement.<sup>35,36</sup> The presence of a high electric field ( $\sim 10^5$  V/cm) lowers the potential barrier for a defect to emit charge (either directly or via phonon-assisted tunneling) and so increases the generation rate. A characteristic of this mechanism is that the activation energy for dark current generation is lowered. Normally bulk generation will have roughly the same activation energy as surface generation (i.e. 0.63-0.65 eV, as mentioned above) but the brightest (field enhanced) pixels

can have activation energies as low as 0.4 eV. This means that they change more slowly with temperature and are relatively more pronounced at low temperatures (that is, the dark images get more nonuniform).

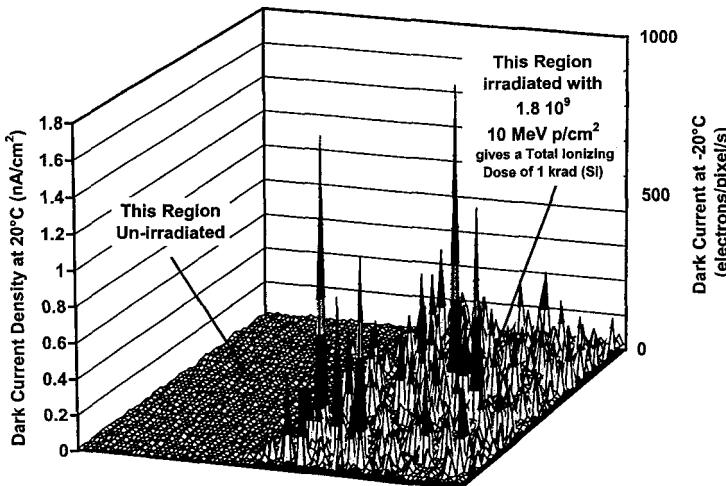


Figure 8 Dark current spikes in a proton-irradiated Atmel TH7895 CCD

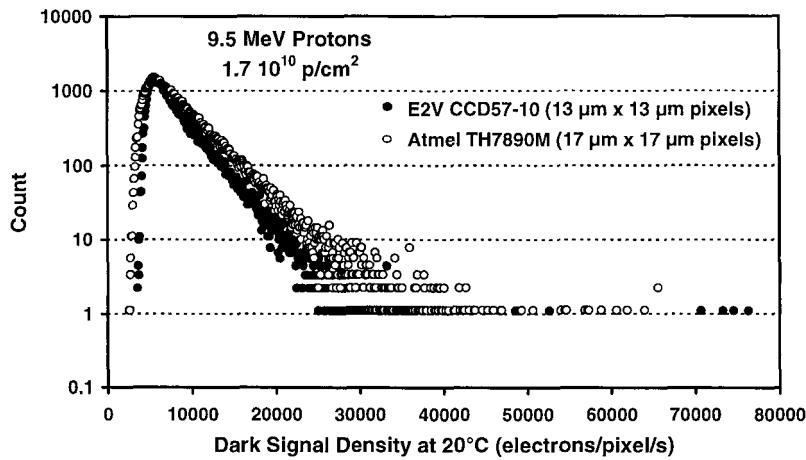


Figure 9 Histograms of dark current density for two types of CCD

Although the mean bulk dark current is determined by the displacement damage dose, the shape of the distribution of pixel-to-pixel variations (dark signal nonuniformity or DSNU) cannot, since it depends on the variations in the distribution of PKA energies (and hence on the incident particle type and energy) and on the variations in the electric field within a pixel (since this affects the proportion of defects that are influenced by field enhancement). Dale et

al.<sup>29</sup> have used the CUPID Monte Carlo code to model the damage cascades in detail and found good agreement with dark current histograms for low field devices. Such simulations are needed in cases where the incident particle energy is high enough that the range of a typical PKA can take it outside its original sensitive volume (e.g. for protons > 60MeV and pixel dimension ~ 10 µm). Otherwise, an analytical formalism developed by Marshall et al.<sup>37</sup> can be used (see also Robbins<sup>38</sup>). In this, the elastic and inelastic collisions are treated separately. With the cross sections for these reactions ( $\sigma_e$  and  $\sigma_i$ ) and an estimate of the sensitive volume (V), the number of interactions (N) in the sensitive volume can be calculated from

$$N = \sigma p \phi V N_A / A \quad (5)$$

Where  $p$  and  $A$  are the density and atomic mass of silicon,  $N_A$  is Avagadro's number and  $N$  can be calculated for elastic or inelastic collisions (depending on the cross section used). For example, for 63 MeV protons  $\sigma_e$  and  $\sigma_i$ , are 318 and 0.52 barns,<sup>37</sup> so that the number of elastic and inelastic collisions in a 900 µm<sup>3</sup> volume (e.g. 15 µm x 15 µm x 4 µm) for a fluence of 2  $10^{10}$  p/cm<sup>2</sup> are 300 and 0.5 respectively. Thus there are far more elastic collisions than inelastic. On the other hand the inelastic collisions deposit roughly three orders of magnitude more energy. The probability density function (pdf) for the energy deposited in a single inelastic collision is highly skewed towards the higher energies and Marshall et al. modeled this with a two parameter gamma function with mean and variance determined from their calculations of PKA spectra (updated values are tabulated in Dale et al.<sup>29</sup>). The n-fold convolution of this distribution then represents the pdf for n collisions within the sensitive volume. Elastic collisions are modeled by a Gaussian distribution, again with a mean and variance determined from the PKA spectra (Robbins<sup>38</sup> found that he could obtain a better fit to experimental CCD data using a gamma distribution). The final distribution is then a weighted sum of the elastic pdf and the pdfs for 1,2, 3 etc. inelastics. Comparing this with the dark current histogram allows an estimate of the conversion factor between damage energy and dark current:  $k_{\text{dark}}$ .

In many cases the analytical model gives a good fit to experimental data but this will not be so when field enhancement is significant. Hence it is not usually possible to predict the distribution of the brightest dark current spikes – and it is these which will usually determine the cosmetic quality and scientific usefulness of the images. In practice it is found for CCDs that the maximum dark current of these dark current spikes is in the range 4-10 nA/cm<sup>2</sup> at 20°C. If the electric field distribution can be estimated (and hence the distribution of field enhancement factors) then this can be used to form a weighted sum of the pdfs for each field value. This has been done by Bogaerts et al.<sup>39</sup> for a CMOS active pixel sensor where, as in CCDs, field enhancement can be an important factor.

With an APS there is some scope either to change the pixel geometry to reduce the electric fields or simply to reduce the applied voltage. Figure 10 shows a case where dark current spikes can be reduced to a low level (comparable with the fixed pattern noise) by reducing the pixel bias in a photodiode APS. Note that the data were obtained at a very high fluence of 1.7  $10^{11}$  9.5 MeV protons/cm<sup>2</sup>. For low Earth orbits the fluence will be an order of magnitude lower and dark current nonuniformity is negligible.

The same damage factor ( $k_{\text{dark}}$ ) discussed above can also be used to relate the average bulk

dark charge with the displacement damage dose. Srour et al.<sup>40</sup> have recently compiled data for different devices, radiation sources and silicon dopings, and suggested that either the divacancy or a multivacancy complex is responsible for bulk dark current generation and defined a universal damage constant of  $(1.9 \pm 0.6) \times 10^5$  carriers/cm<sup>3</sup>sec per MeV/g at 300K and 1 week after irradiation (after a large fraction of any annealing has taken place). This value is in good agreement with measurements on CCDs, but to use it requires a knowledge of the depletion volume. and, The evidence suggests that the primary defect in CCDs is not the divacancy since the dark current anneals at temperatures of 150°C or below,<sup>41</sup> but a vacancy or an interstitial complex is still a possibility.

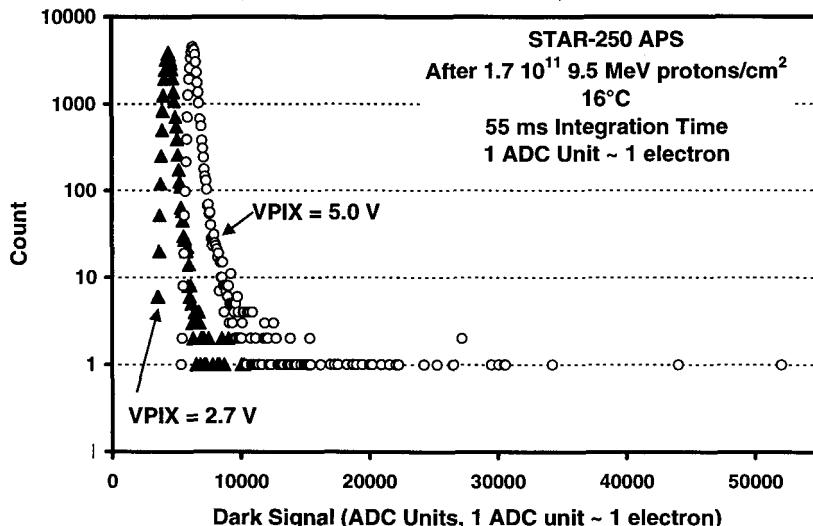


Figure 10 Histograms of dark current density for a STAR-250 APS at nominal and reduced pixel bias.

### 3.2 Random Telegraph Signals

An effective method to reduce dark signal nonuniformity is to reduce the device temperature (using a thermoelectric cooler or by passively radiating to space). However, for space applications, there is usually a significant cost and mass incentive to operate the sensor close to room temperature and to obtain calibration images to subtract out the dark current. Unfortunately, a feature of displacement damage is that the dark current generating defects often tend to have a bistable or metastable nature so that the dark current switches level, giving the appearance of a random telegraph signal (or RTS) as in figure 11. This makes the usefulness of dark calibration uncertain. RTS behavior has been studied in CCDs,<sup>42,43</sup> APSs<sup>44</sup> and IR imagers.<sup>45,46</sup> A significant effort is required to fully characterize a complete device and, so far, only small numbers of pixels have studied and the defect(s) responsible have not yet been identified. Based on the limited experimental work done to date one can make the following tentative conclusions:

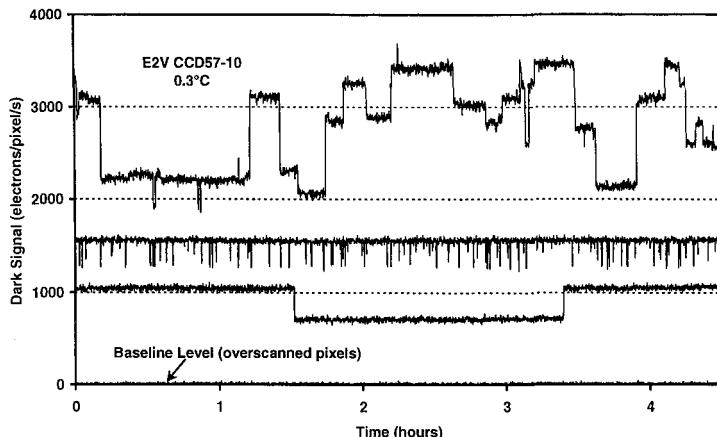


Figure 11 Examples of random telegraph behavior in CCD dark current

- RTS effects are seen in all proton irradiated CCDs and APSs over a range of proton energies (at least 1.5 to 60 MeV).
- In CCDs, the probability for an RTS defect in a pixel is  $\sim 0.000016$  per incident 10 MeV proton and seems to scale with NIEL (though it is not clear whether the elastic NIEL or the total NIEL gives the best fit). Thus, with  $20 \mu\text{m} \times 20 \mu\text{m}$  pixels and a fluence of  $10^{10}$  10 MeV p/cm $^2$ ,  $\sim 40\%$  of pixels will show RTS effects. In the APS that was studied<sup>39</sup> the occurrence probability was much lower because of the small area of the photodiodes.
- There is a wide range of switching amplitudes, but in a CCD they are typically 500 to 20,000 electrons/pixel/s at 5°C. Most large fluctuations occur for pixels with a high pedestal level, but not always – some large dark current spikes do not show RTS effects. The amplitudes decrease with cooling as expected (activation energy  $\sim 0.6$  eV)
- There is also a wide range in time constants – near room temperature they range from seconds to hours (i.e. 4 orders of magnitude), but are mostly of order several minutes.
- The time constants for existing in the high and low dark current states are usually roughly comparable but not always – some pixels show ‘spiking’ - that is, short excursions to either the low or high state.
- The time constants increase as the device is cooled. In CCDs the activation energy is typically 0.9 to 1.6 eV but Bogaerts et al. measured  $\sim 0.6$  eV for their APS. The fact that some defects switch very fast at room temperature means that RTS effects can still be seen (with time constants of several hours) even at -40°C.

### 3.3 Charge Transfer Degradation

The other main effect of displacement damage in CCDs is that defects are created in the buried channel and these will trap charge as it is moved through the CCD during readout and release it some time later, usually into a following charge packet. This causes a smearing of the image and is characterized by the charge transfer inefficiency (CTI), which is the fraction

of charge that is trapped during each pixel transfer. (1-CTI) is the charge transfer efficiency or CTE. In active pixel sensors the signal is read directly from the pixel and so this effect does not occur. This is one of the main advantages of the APS in a proton or neutron environment.

For a trap located at an energy,  $E_t$ , below the conduction band and with a capture cross section,  $\sigma_n$ , the capture and emission times,  $\tau_c$  and  $\tau_e$ , are given by:<sup>47</sup>

$$\tau_c = 1/\sigma_n v_{th} n_s \quad (6)$$

$$\tau_e = \exp(E_t/kT)/\sigma_n X_n v_{th} N_c \chi \quad (7)$$

where  $n_s$  is the signal density,  $v_{th}$  is the average thermal velocity for electrons,  $N_c$  is the effective density of states in the conduction band,  $T$  is the absolute temperature, and  $k$  is Boltzmann's constant.  $X_n$  is the 'entropy factor' associated with the entropy change for electron emission from the trap, and  $\chi$  is a factor to allow for any field enhanced emission (which affects trap emission time as well as dark current generation).

The capture time depends inversely on the signal density and will be shortest in the center of a charge packet where the density is highest. If charge is transferred through a pixel faster than it can be captured, then CTE will not be degraded and we have a CTI 'capture factor' given by

$$\text{CTI capture factor} = (1 - \exp[-t_c/\tau_c]) \quad (8)$$

where  $t_c$  is a characteristic transfer time. If the charge packets of are moved through a pixel on average timescales,  $t_s$ , shorter than these emission times, then traps will be filled by the first ('sacrificial') packet readout, but will still be filled when subsequent packets arrive. The CTI 'emission factor' is then given by:

$$\text{CTI emission factor} = (1 - \exp[-t_s/\tau_e]) \quad (9)$$

Equation (6) indicates that the capture time is only weakly dependent on the temperature whereas  $\tau_e$ , in equation (7), varies exponentially.

The effect of displacement damage on CTI depends on the complex interplay between the movement of charge and the trapping and release of carriers by the defect centers. Hence CTI does not have a single value but depends on the dimensions of the buried channel, clocking rate, temperature, signal level (including background charge) and, of course, on the nature and concentration of the traps themselves. Hence it is found that the CTI damage factor,  $k_{CTI}$ , (expressed as the CTI change per equivalent MeV proton/cm<sup>2</sup> or, alternatively, per unit displacement damage dose) can vary by several orders of magnitude though, other things being equal, it is always largest for small signals and small backgrounds (since a given trap concentration will then have a proportionately larger effect). Hence space astronomy missions such as the Hubble Space Telescope<sup>48</sup> and the Chandra<sup>49</sup> X-ray observatory have been significantly affected even though the proton fluence is low (in the latter case the damage was unexpectedly high due to low energy protons which reached some CCDs by scattering off the X-ray mirrors<sup>50</sup>).

Usually the CTI in the vertical (column) direction is the most important because the pixels are moved more slowly and there is more time for charge trapping. Figure 12 shows some typical results. Over recent years, several investigations<sup>51,52,53,54,55,56,57,58,59</sup> have produced CTI data for a variety of CCDs, particularly for the low signal/low background case where a typical  $k_{CTI}$  is  $\sim 4 \cdot 10^{-13}/10$  MeV proton/cm<sup>2</sup> for a 20μm x 20μm pixel at 10 ms line move rate. This data can sometimes give a confusing variation in CTI values. However these variations are reduced if some simple scaling is applied to allow for the different experimental conditions. Because the CTI (for a given trap concentration) will increase in proportion to the

volume of silicon, it will tend to increase with pixel size – and the pixel area can be used as an approximate scaling factor (though the actual volume of the buried channel will give more accurate scaling if it is known). Figure 13 (from<sup>60</sup>) shows how the CTI can change with the dwell time within a pixel (which is determined by the line move rate). For a frame transfer CCD it has to be borne in mind that both fast (frame transfer) and slow (readout) line moves are involved and typically there will be a factor ~3 difference between the CTI at the two rates (though this factor is slightly signal and background dependent). The implications for star tracker applications have been previously discussed<sup>61</sup> along with the improvement in performance that can be gained by increasing the background level ('fat zero') – though at the expense of increasing the Poisson (shot) noise. CTI has also been seen to vary with temperature, decreasing by a factor 2 when the temperature decreases from -20 to -50°C.<sup>62</sup>

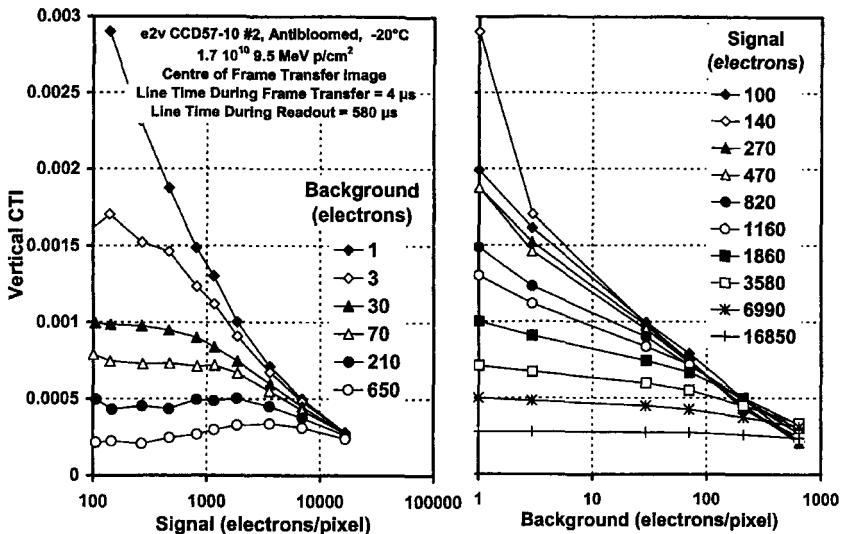


Figure 12 Vertical CTI for a typical buried channel CCD (pixel size 13 μm x 13μm, with antiblooming structures).

From the above discussion we see that CTI values can be scaled to allow predictions for different applications but the accuracy is probably a factor of 2 at best. Hence it is recommended to perform proton testing for the actual device operating conditions whenever possible. Even if the CTI is known, the effect on imaging performance still has to be calculated. Several authors<sup>63,64</sup> have developed models for predicting CCD performance for particular operating conditions. Care has to be taken, however, when extrapolating results.

CTI damage starts to have a major impact at equivalent 10 MeV proton fluences of around  $10^{10}$  p/cm<sup>2</sup> or above. For space astronomy missions where the CCD can be cooled to low temperatures, there is the possibility to keep the trapping centers permanently filled either by special clocking sequences<sup>65</sup> or by using injection of an artificial charge packet ahead of the signal.<sup>66,67</sup> These techniques rely on knowing the emission time of the traps. Figure 14 shows experimental data on the variation of emission time with temperature for the dominant trap at moderately high temperatures for a variety of CCDs. Since the trap has an energy level ~0.44 eV it is believed to be the E center and this is supported by annealing data.<sup>41,67</sup>

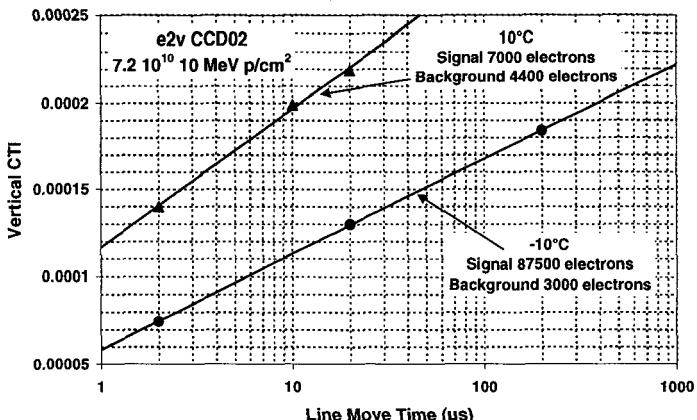


Figure 13 Illustration of the variation of vertical CTI with line move time

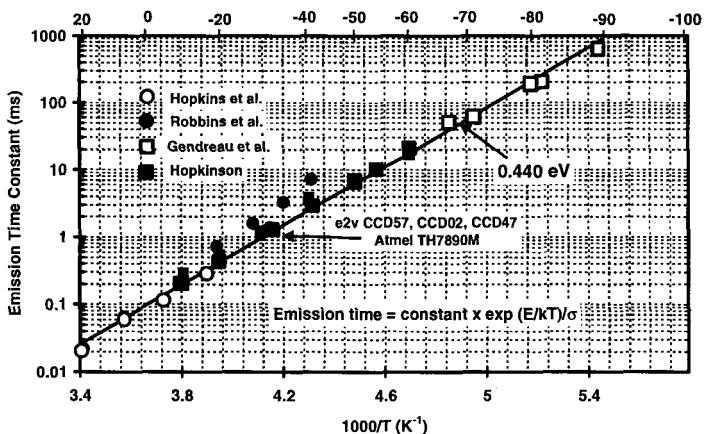


Figure 14 Trap emission time versus temperature

At low temperatures ( $\sim -100^\circ\text{C}$ ) when the 0.44 eV trap can be kept filled, there are other traps that come into play. Traps with energies around 0.23 and 0.33 eV have been found by several authors but not positively identified.<sup>57,61,55</sup> At lower temperatures still, the A center (oxygen-vacancy complex) which has an energy level of 0.17 eV, becomes important.

Some of the methods used to mitigate the effects of CTI degradation, such as fat zero and charge injection, have been discussed above. A further possibility is to heat the CCD to a temperature where the traps anneal out. Unfortunately, temperatures above  $100^\circ\text{C}$  are needed and this is not normally practicable. Another solution is to use a p-type buried channel rather than n-type. The dominant dopant is then boron rather than phosphorous and the E center should not be present. This has been discussed by Spratt<sup>68</sup> et al. and Hopkinson,<sup>69</sup> though the improvement in CTI was inconclusive. Recent results<sup>70</sup> indicate that p-channel CCDs do indeed have a definite advantage for proton environments, but such devices are not routinely

fabricated by commercial CCD manufacturers (though for special applications, such as space astronomy, it can be possible for devices to be custom-built).

Care in measuring CTI is important if consistent results are to be obtained. Methods include use of X-ray sources, optical spots and optical flat fields (extended pixel edge response, EPER and first pixel response, FPR). These have been discussed (for example) in<sup>3</sup>. Some devices are now made with an injection gate and this can be used to inject test signals for CTI measurement. The injected signal appears to have low (sub-Poisson) noise<sup>71</sup> and so can be used to produce a background charge (at zero) level to reduce CTI.

### **3.4 Testing for displacement damage effects**

Most CCD displacement damage data have been obtained using proton accelerators with the devices irradiated at room temperature. This can be done with the CCDs biased or unbiased and the available evidence suggests that the bias condition does not make a significant difference. The particle flux is typically  $\sim 10^8$  p/cm<sup>2</sup>/s – much higher than in space – but this does not appear to affect the displacement damage (significant effects have only been seen when the flux becomes an order of magnitude higher<sup>72</sup>). The protons will also produce ionization (total dose) damage and this is known to be dose rate (i.e. flux) dependent. Hence proton beams are not good simulators for total dose damage. When testing dark current (total dose does not affect CTE) the two damage components need to be carefully separated and allowed for separately (with the ionization component tested using cobalt-60 gamma rays).

At room temperature it is usually observed that some annealing takes place immediately after irradiation<sup>73</sup> and in the first few weeks. After that the damage is permanent (unless the device is deliberately heated). Unless otherwise stated, it is usually safe to assume that test results are for devices that have been stored for several weeks at room temperature so that the short term annealing has been completed. There is some evidence from space astronomy missions that cooled CCDs show an annealing of the dark current spikes when heated to near room temperature.<sup>48,74</sup> This implies that irradiation when cold gives greater damage than when at room temperature. There is also evidence of CTI changes after cold irradiation.<sup>75</sup> However, very little work on low temperature irradiations has so far been performed.

## **4. Transient Events**

Transient events are produced by the ionization of silicon atoms along the tracks of charged particles. The energy deposited depends on the product of the ionizing energy loss,  $dE/dx$ , of the particle and the track length. Approximately one electron-hole pair is created for every 3.65 eV ionizing energy deposited. In a space environment the main concern is usually transients caused by primary protons and by secondary particles produced by proton interactions with shielding material.<sup>76,77</sup> Heavy ion transients from cosmic rays will also occur, though in greatly reduced numbers compared with proton events. To take an example, Hopkinson et al.<sup>6</sup> showed that, for a polar Earth orbit at 800 km altitude and the 10 mm aluminum shielding, the average flux during transit through the South Atlantic Anomaly (SAA) is  $\sim 1500$  protons/cm<sup>2</sup>/s. In some applications, for example missions to Jupiter or its moons, electron events may also be important.<sup>78</sup>

Minimum ionizing particles create  $\sim 80$  electron hole pairs / $\mu\text{m}$  so that, for a typical CCD charge collection depth of 20  $\mu\text{m}$ , a proton transient will generate at least 1,600 electrons and each particle strike results in a significant signal. There will be some variation in the amount of charge deposited in each pixel.<sup>6</sup> This is primarily because, in a space environment, there are variations in the proton energy and path length. There is also a statistical spread in the charge deposited, even for mono-energetic beams.

Lomheim et al.<sup>79</sup> have carried out an experimental investigation of single particle transient signals from mono-energetic protons and heavy ions incident at various incident angles to a Kodak KAF-1400 CCD. The results were in agreement (to within 20%) with the signal charge expected for a particular ion track length including contributions from the pixel depletion and diffusion volumes. McCarthy et al.<sup>80</sup> have performed a similar investigation (using protons in the range 50 to 300 MeV) for a deep depletion CCD, specially designed for X-ray astronomy. They found that in many cases the proton events could be distinguished from their X-ray signals. However, in general, the large spread in the amount of charge deposited in a CCD makes it very difficult to discriminate against proton transients. Another way of mitigating the effects is to use a thinner active volume so that the track lengths are shorter, but this will reduce the detector responsivity for wavelengths absorbed deep in the device. Instruments (e.g. star trackers) which continuously stare at a scene will often have software which discriminates against signals that are only present for a single image frame. If the observing situation allows, this is the best way of ensuring a tolerance to transient effects.

## 5. Future Work

The high performance of CCDs makes them vulnerable to even low doses of radiation and, since the radiation effects vary with operating conditions, a continuing effort is needed to characterize devices for particular applications. In addition there are some fundamental aspects, particularly relating to displacement damage, where further work is needed. For example, the mechanisms of dark current fluctuations (random telegraph signals) have not been investigated enough to make accurate predictions of the effects on images or the calibration strategies that are needed. Also, the full inventory of defects, that affect dark current and charge transfer inefficiency, has not been identified. Modeling and prediction of proton-induced CTI remains a major concern for many missions.

The CMOS active pixel sensor is emerging as a good alternative to the CCD. Although these do not suffer from CTI degradation and gate oxide effects can usually be neglected, a substantial test effort is still needed to fully characterize these devices for radiation effects since they can still be prone to parasitic leakage effects (total ionizing dose) and to increases in dark signal. In addition there are the possibilities of single event latch-up or functional interrupt and for degradation in the performance of on-chip circuitry (e.g. ADCs).

## Acknowledgements

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## THE EFFECTS OF SPACE RADIATION EXPOSURE ON POWER MOSFETS: A REVIEW

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Power MOSFETs are a commonly used device for many switching and power control applications. Their upper frequency limit spans a fairly broad range, from 1 MHz to 10 MHz. These devices are frequently used in spaceborne electronic systems where they encounter radiation exposure during operation. This paper reviews the current technology, its high frequency capability, the future trends for power MOSFET technology, and the degradation that the power VDMOS technology experiences in the space radiation environment.

Keywords: MOSFETs, power MOSFETs, radiation effects, space radiation, VDMOS.

### 1. Introduction

The electrical characteristics of power metal-oxide-semiconductor (MOS) field-effect-transistors (FETs) make them of interest for use in space systems where they may be exposed to radiation. Power MOSFETs, in general, have higher switching speeds than their power bipolar transistor counterparts.<sup>1</sup> Power MOSFETs also have a negative temperature coefficient of carrier mobility, which reduces the potential for thermal runaway, second breakdown, and power hogging in parallel devices when compared to bipolar transistors.<sup>1</sup> In addition, power MOSFETs have simpler input drive requirements than bipolar transistors.<sup>1</sup>

The space radiation environment can be very detrimental to electronic components. For example, the natural space radiation environment of the earth consists of (1) trapped particles in the magnetic field of the earth - primarily protons and electrons; and (2) cosmic rays - heavy ions or protons of solar or galactic origin.<sup>2</sup> There are high-energy photons, protons, heavy ions, and electrons that can cause total-dose ionizing radiation damage and high-energy protons, neutrons, and heavy ions that can cause displacement damage. The high-energy protons and heavy ions can introduce dense charge filaments along the path of the particle through an electronic device that can interact with sensitive regions of the device to trigger catastrophic failure mechanisms. The concentrations and types of ions vary significantly with altitude and inclination of angle of an orbit, recent solar activity, and the amount of protective shielding. These variations make it difficult to specify a typical space environment.<sup>3</sup> Also, the precise environment (total ionizing dose and high-energy protons and heavy ions) encountered by a specific electronic system will be highly dependent on the mission.

This paper will briefly discuss the characteristics of power MOSFETs with an emphasis on the vertical double-diffused (VDMOS) technology that is widely used commercially. Switching speed constraints will also be discussed. With this background, the effects of radiation on power MOSFETs will be introduced and reviewed based on a large body of work appearing in the literature.

## 2. Power MOSFET Technologies

### 2.a. Current commercial technology

The VDMOS transistor is a special type of MOS transistor well suited to power applications. Figure 1 shows the basic structure of a VDMOS power transistor.<sup>1</sup> The device is termed double-diffused because, typically, both the source and the body are defined using the polysilicon gate as a mask. The gate and source are self-aligned processes in commercial products. However, in some radiation hardened power MOSFETs, these processing steps may not be self-aligned. Usually then, the channel length is determined by the difference in lateral diffusion of the dopants, rather than by photolithography limitations, and thus, the channel is not uniformly doped. Contact to the drain is made on the bottom surface of the silicon chip, rather than on the top surface as in a lateral MOSFET. The thick epitaxial drain region is required to drop the large drain to source voltages that the power transistor must support while operating in the *OFF* state. When turned *ON* with an appropriate gate bias, an inversion layer forms along the p<sup>-</sup> surface forming a channel between the n<sup>+</sup> source region and the n<sup>-</sup> epi drain region allowing current to flow. In practice, a large number of devices (or cells) are connected in parallel to create a wide effective channel while retaining the short channel lengths of each individual cell. The large width allows large currents to flow when placed in the *ON* state.

The on-resistance of a VDMOS transistor is one of its most important parameters because it limits the amount of current flow that can be conducted by the device before the power dissipation within the device induces junction temperatures that lead to device failure. Therefore, the on-resistance should be as low as possible. Another important parameter is the maximum blocking voltage. This is the maximum voltage applied between the source and drain contacts with zero gate-source voltage that does not lead to breakdown.

Due to its many attractive features, there has been a concerted effort to optimize the design, structure, and process technology of VDMOSFETs in terms of the on-state resistance. The on-resistance of a VDMOSFET is primarily defined by the resistance of the low-doped epitaxial layer. By increasing the doping in the epi-layer, the on-resistance can be reduced. However, the breakdown voltage of the device is inversely proportional to the epi-layer doping, so a compromise between on-resistance and breakdown voltage must be found. In addition, the thickness of the epi-layer must increase with the desired breakdown voltage in order to accommodate the depletion region, further increasing the on resistance. For low breakdown voltage devices ( $\leq 100\text{V}$ ), the parasitic resistances (drain-substrate resistance, channel, source, contact, electrode, etc.) must be considered.

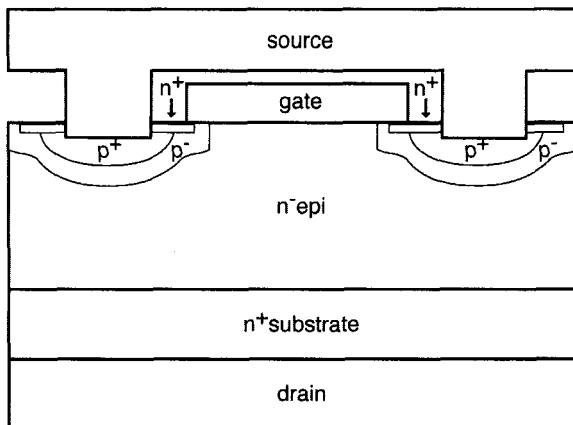


Fig.1. The basic structure of a VDMOS transistor.

In one approach to reduce the on-resistance, the n-doping concentration in the epi-layer is increased uniformly. To retain the voltage blocking capability, the additional n-doping must be compensated by appropriate p-doping. Several different configurations are possible. Figure 2 shows a configuration where the doping concentration of the n<sup>-</sup> epi-layer has been increased. To compensate, the higher n-doping concentration a vertical p<sup>-</sup> doped area is placed below the source contact.<sup>4,5</sup> Because of the higher doping concentration, the resistance of the n epi-layer is lower than in the original device (compare to Figure 1). Width and concentration of the vertical p<sup>-</sup> doped area have to be chosen in such a way that the space charge region in the OFF state can be accommodated.

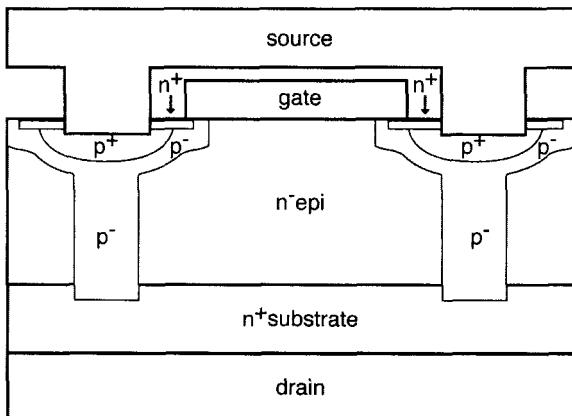


Fig. 2. Modified device structure to reduce on-resistance with increased doping concentration in the epi-layer and an additional vertical p<sup>-</sup> doped area under the source.

Most VDMOS processes use a poly-silicon gate structure rather than the metal-gate type. If the resistance of the gate structure is high, the switching time of the device is increased, thereby reducing its upper operating frequency. Compared to a metal gate, a poly-silicon gate has a higher gate resistance. This property accounts for the frequent use of metal-gate MOSFETs in very high-frequency (typically more than 20 MHz) applications, and poly-silicon gate MOSFETs in higher-power, but lower-frequency systems. Power MOSFETs are usually faster than power bipolar devices because they do not rely on injection of excess minority carriers that must be supplied by the forward biased junction to turn the device on and then removed to turn the device off. An equivalent circuit model shown in Figure 3 indicates the components that have the greatest effect on the switching characteristics of a MOSFET.<sup>6</sup>  $R_G$  is the distributed resistance of the gate and is approximately inversely proportional to active area.  $L_S$  and  $L_D$  are source and drain lead inductances and are around a few tens of nano-Henry (nH).<sup>6</sup>

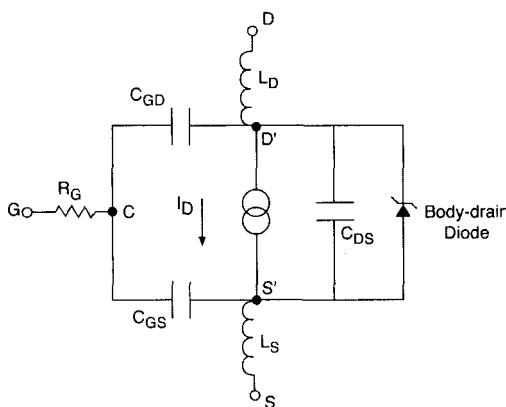


Fig. 3. Equivalent circuit showing components that have the greatest effect on MOSFET switching.

Since the effective resistance and capacitance of the gate terminal control the frequency response of a MOSFET, a rough estimate can be made of the maximum operating frequency of the MOSFET. The resistance ( $R_G$ ) depends on the sheet resistance of the poly-silicon gate overlay structure. One of the dynamic characteristics of a power MOSFET that can therefore affect its switching performance is its parasitic capacitance. There are three main capacitance parameters of a power MOSFET, namely, gate-to-drain capacitance  $C_{GD}$ , gate-to-source capacitance  $C_{GS}$ , and drain-to-source capacitance  $C_{DS}$ .  $C_{GS}$  and  $C_{GD}$  are voltage-dependent capacitors while  $C_{DS}$  is nearly constant. Gate-to-drain capacitance,  $C_{GD}$ , is a nonlinear function of voltage and is the most important parameter because it provides a feedback loop between the output and the input of the circuit.  $C_{GD}$  is also called the Miller capacitance because it causes the total dynamic input capacitance to become greater than the sum of the static capacitances. A combination of these parameters determines the typical input and output capacitance parameters:  $C_{ISS}$  ( $C_{GD} + C_{GS}$ ),  $C_{OSS}$  ( $C_{GD} + C_{DS}$ ) and  $C_{RSS}$  ( $C_{GD}$ ). The value of  $C_{ISS}$  is closely related to chip size; the larger the die area, the greater the capacitance value. The switching performance of a device is determined by the time required to establish voltage changes across capacitances. Since the RC combination of the input circuit must be charged and discharged by the driving circuit, and since the capacitance value dominates, chips with a

larger die area will have slower switching times than smaller chips. In general, the upper frequency limit of most power MOSFETs spans a fairly broad range, from 1 MHz to 10 MHz.

### **2.b. Future trends in power MOSFET technology**

The focus in power MOSFET design has been to minimize the on-resistance of the MOSFETs, improve the reverse recovery characteristics and increase the reverse voltage blocking capability of the MOSFETs.<sup>5</sup> New device structures have been proposed for the reduction in on-state resistance. Prominent technologies today are the MDMESH<sup>TM</sup> from ST Microelectronics, CoolMOS<sup>TM</sup> from Infineon Technologies, and the SuperJunction FET from International Rectifier, each of which is based on the charge balance concept.<sup>7,8</sup> These devices have a smaller die area than their equivalent conventional MOSFET counterparts and substantially less output capacitance. Results indicate an improvement in the body-drain diode switching recovery behavior. This tends to minimize the losses in switching converter applications.

Silicon carbide (SiC) power MOSFETs are also the subject of active research. SiC offers significant advantages for power-switching devices because the critical field for avalanche breakdown is about ten times higher than in silicon. SiC power devices have made remarkable progress in the past five years, demonstrating currents in excess of 100 A and blocking voltages in excess of 19,000 V.

Several SiC devices have demonstrated performance figures that far exceed comparable silicon devices and, unlike silicon, the theoretical performance limits for SiC do not impose any near-term constraints on continued progress.<sup>9</sup> SiC wafers are commercially available in 75-mm diameters with micropipe densities below 10 cm. This permits high-yield fabrication of transistors and diodes with 20 A capability as single devices and 100 A or higher capability in modules. SiC wafers are expected to continue to increase in size and improve in quality in coming years.<sup>10</sup> SiC power devices will first appear in specialized commercial applications where silicon devices cannot effectively compete. One such application is freewheeling rectifiers in motor control circuits, where SiC Schottky or p-i-n diodes will displace conventional silicon p-i-n diodes. Substitution of SiC diodes in these systems provides significant systems advantages due to greatly reduced switching losses. Further into the future, SiC transistors and thyristors may begin to displace silicon insulated gate bipolar transistors (IGBTs). It is not clear at this point whether these SiC transistors will be MOSFETs, junction field effect transistors (JFETs), or bipolar junction transistors (BJTs). JFETs and BJTs have fewer materials issues and are easier to fabricate than SiC MOSFETs, but MOSFETs ultimately offer the greatest advantages over silicon IGBTs because of their high input impedance and low dynamic power dissipation. However, considerable development work is needed to bring SiC MOSFETs to their potential.

### 3. Total Dose Ionizing Radiation Effects on Power MOSFETs

#### 3.a. *Ionizing radiation effects basics*

The topic of total ionizing dose radiation effects in MOS systems has been actively studied for several decades.<sup>11,12</sup> When the dielectric films (assumed to be SiO<sub>2</sub>) in a power MOS device are exposed to ionizing radiation, electron-hole pairs are created. These electron-hole pairs either recombine or begin a transport process through the dielectric under the influence of the applied fields. In a gate oxide with positive bias on the gate, the electrons are quickly swept to the gate and collected. The holes experience a stochastic transport process to the oxide - silicon (SiO<sub>2</sub>-Si) interface where a fraction is trapped in deep hole-traps in close proximity to the interface. These trapped holes give rise to the fixed oxide charge N<sub>ot</sub>.<sup>13</sup>

In addition to the fixed oxide charge, interface traps are produced at the SiO<sub>2</sub>-Si interface. Interface traps are formed when radiation-generated holes liberate protons in the oxide that transport to the SiO<sub>2</sub>-Si interface, where they de-passivate dangling bonds. Good reviews of the current state of understanding of radiation-induced interface traps in MOS devices are available.<sup>11,12,14</sup>

Interface traps are manifested as energy levels within the silicon band-gap. The occupancy of these levels depends on the potential at the SiO<sub>2</sub>-Si interface. It is usually assumed that states lying above mid-gap are acceptor-like, while those below mid-gap are donor-like. When charged, the interface traps give rise to the interface trapped charge N<sub>it</sub>. Both N<sub>it</sub> and N<sub>ot</sub> are considered as areal concentrations at the SiO<sub>2</sub>-Si interface measured in number of charges per square centimeter. The technique introduced by McWhorter and Winokur is the most frequently used to separate the relative contributions of oxide trapped charge N<sub>ot</sub> and interface trapped charge N<sub>it</sub> in device electrical behavior.<sup>15</sup>

The interface and oxide trapped charge introduced into device dielectrics by ionizing radiation leads directly to degradation of MOS device characteristics. The most commonly observed and reported effect is a shift in threshold voltage; however, ionizing radiation will also lead to mobility degradation, increase in leakage currents, and reduction of breakdown voltage.

#### 3.b. *Effects on threshold voltage*

For a MOSFET exposed to ionizing radiation, the gate oxide will contain trapped charge, which is normally positive, and charge in interface traps. In n-channel enhancement-mode MOSFETs with the gate bias above threshold, interface traps contribute negative charge. The threshold voltage shift for an n -channel MOSFET can be expressed as:

$$\Delta V_T = \frac{-q}{C_{ox}} \Delta N_{ot} + \frac{q}{C_{ox}} \Delta N_{it} = \Delta V_{ot} + \Delta V_{it}$$

where  $q$  is the electron charge and  $C_{ox}$  is the gate oxide capacitance per unit area. The threshold voltages of n-channel MOSFETs normally exhibit a negative shift following exposure to ionizing radiation, due to a net build-up of positive trapped charge in the gate oxide. This positive oxide trapped charge can be partially compensated by the build-up of negative interface trapped charge. For p-channel devices, the charge in interface traps is predominantly positive, as is the oxide trapped charge. Figure 4 is a schematic of the shift in threshold voltage for both n-channel and p-channel MOSFETs.<sup>16</sup> For a device that has been radiation hardened, the threshold voltage may not change significantly to levels of several Mrad(Si); however, a non-hardened n-channel device could become depletion mode at a few tens of krad(Si). Reducing the gate oxide thickness usually improves the total dose tolerance, but also decreases the maximum voltage that can be applied to the gate and may increase susceptibility to single event gate rupture as described below. The rate at which the threshold voltage changes with dose is very technology-dependent and in some n-channel devices the threshold voltage may recover, depending on the relative magnitudes of oxide charge and interface charge as a function of dose. This is schematically illustrated in Figure 5 where the threshold shift for an n-channel device is decomposed into its oxide trapped charge component and interface trapped charge component.<sup>15</sup>

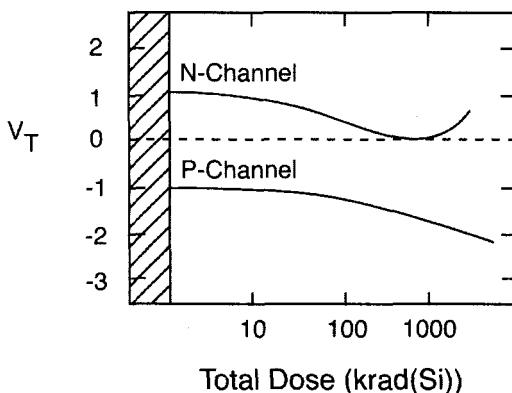


Fig. 4. Schematic representation of the threshold voltage for n- and p- channel MOSFETs as a function of total ionizing radiation dose. After ref. 16.

The effects of  $N_{ot}$  and  $N_{it}$  on device behavior can be somewhat complicated in the natural space environment. Both interface and oxide trapped charge may exhibit complex temporal behavior. Oxide trapped charge anneals with time and temperature, while interface traps often require long periods of time following irradiation in which to form. This behavior is particularly important for space applications. Because of the long time over which the total ionizing dose is accumulated, significant in-situ annealing of oxide trapped charge and buildup of interface traps may occur. As the positive oxide trapped charge anneals and the negatively charged interface traps form in an n-channel device, the threshold voltage may begin to increase. In some devices exposed to ionizing

radiation at dose rates approaching those in natural space, the threshold voltages may actually shift to levels more positive than their pre-irradiation values.<sup>17-20</sup> This phenomenon is most commonly encountered in radiation-hardened devices because they have been engineered to balance the densities of interface and oxide trapped charge.

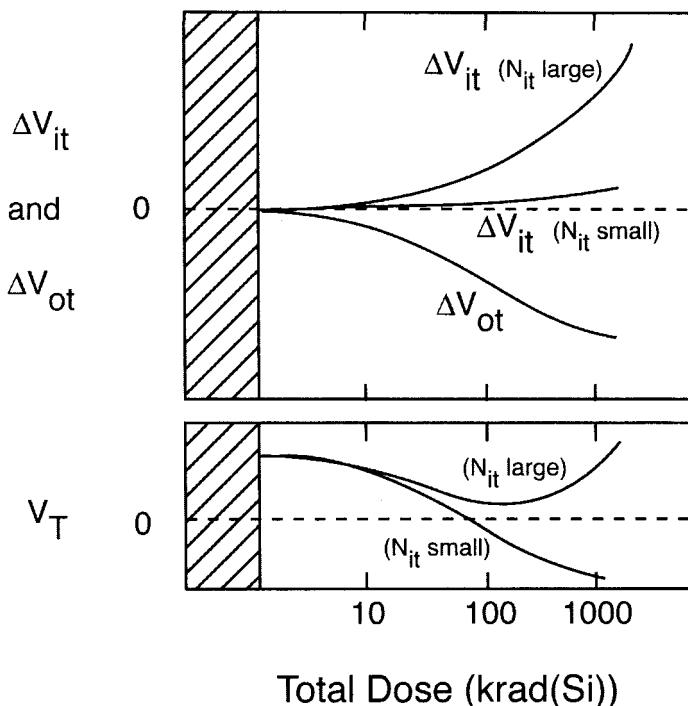


Fig. 5. Schematic representation of the decomposition of threshold voltage shift into components due to oxide trapped charge and interface trapped charge. After ref. 16.

Figure 6 illustrates this effect for power VDMOS transistors exposed to radiation from a Co-60 radiation source at dose rates approaching those encountered in natural space.<sup>20</sup> The IRH-254 is a radiation hardened device while the IRF-440 is an "off-the-shelf" commercial device. Both device types were biased at +9 V on the gate during exposure. The interesting point is that at "space-like" dose rates the threshold voltage of the hardened devices increased with total dose. The same effect has been observed for n-channel devices designed for rad-hard CMOS circuits.<sup>19</sup> In contrast, the threshold voltage of the unhardened devices decreased monotonically and did not exhibit significant dose rate dependence.

Thus far, the discussion has considered power MOSFETs exposed to ionizing radiation with constant bias. Experiments have shown that the threshold voltage shift for n-channel MOSFETs alternately biased on and off does not correspond to the average of the threshold shifts observed for devices biased continuously on or off.<sup>21,22</sup> For simulated space radiation conditions, the threshold shift of both hardened and unhardened power

MOSFETs operated under switching conditions to simulate a switched mode power supply did not exhibit recovery to pre-rad levels.<sup>22</sup>

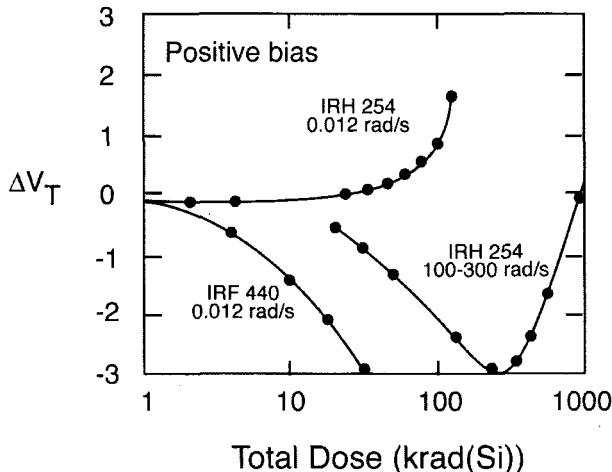


Fig. 6. Threshold voltage shift versus total ionizing dose for positively biased power MOSFETs. After ref. 20.

### 3.c. Effects on channel mobility

The threshold voltage is not the only parameter affected by ionizing radiation. Radiation-induced charge significantly degrades the channel mobility in MOSFETs.<sup>23,24</sup> Figure 7 illustrates the mobility degradation for a power VDMOS device. The following expression has been used to describe the effect on mobility of adding an incremental number of interface traps:<sup>23</sup>

$$\mu = \mu_0 (1 + \alpha \Delta N_{it})^{-1}$$

where  $\Delta N_{it}$  is the increase in interface-trapped charge density resulting from radiation,  $\mu_0$  is the pre-irradiation mobility, and  $\alpha$  is an empirical parameter. A typical value for  $\alpha$  might be  $5 \times 10^{-12} \text{ cm}^2$ . Oxide trapped charge has a measurable but smaller effect on mobility degradation than interface trapped charge.<sup>24</sup>

Mobility degradation in MOSFETs can lead to significant reduction in transconductance and in current-drive capability.<sup>22</sup> The problems with drive and saturated transconductance are compounded in devices that exhibit an increase in threshold voltage when irradiated at low dose-rates. The maximum current that a device can provide at fixed gate voltage depends on the carrier mobility and the difference between the gate voltage and the threshold voltage. In unhardened devices, the threshold voltage shift is usually negative and failure occurs when the device becomes depletion mode. In hardened devices, the threshold shift may be positive and lack of current drive may be the failure mode.

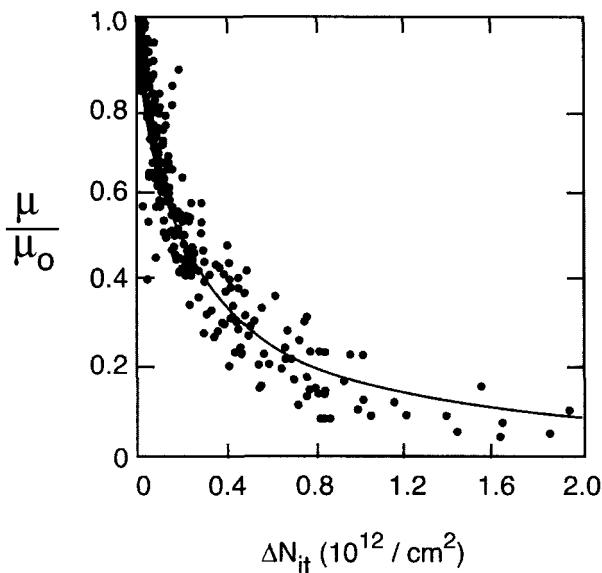


Fig. 7: Reduction in mobility versus radiation induced interface trapped charge for a typical VDMOS transistor. After ref. 16.

### 3.d. Effects on breakdown voltage

The maximum breakdown voltage obtainable for a p-n junction of specified doping concentration occurs for a planar structure.<sup>25</sup> In actual devices utilizing planar diffusion technology, however, the high-voltage junction must intersect the surface at some finite position. The resulting junction curvature compresses the equipotential lines where the junction bends to the surface and increases the peak electric field. Junction-termination structures are used in power devices to reduce the peak electric field and to allow the breakdown voltage to approach its ideal one-dimensional value. The most commonly used termination methods are field rings and field plates.

Avalanche multiplication is the physical mechanism that causes the primary breakdown of high-voltage reverse-biased p-n junctions. The most important factor that influences the magnitude and location of the peak electric field in planar semiconductor technology is the method used to terminate the junction.<sup>25-27</sup> The objective of the different termination methods is to reduce the peak electric field either at the surface or at the curved junction regions in the bulk.

The drain-source breakdown voltage of power MOSFETs is strongly affected by ionizing radiation.<sup>28-31</sup> This is a result of the introduction of trapped oxide and interface charge in the field oxide. These trapped charges alter the potential at the surface of the junction and, in turn, become a part of the junction termination. The effect of ionizing radiation on the functioning of junction termination structures and thus power MOSFET breakdown

voltage has been successfully modeled.<sup>30,31</sup> In general, the breakdown voltage of n-channel devices decreases with total dose, while that of p-channel devices may increase.

#### 4. Single Event Radiation Effects

##### 4.a. Single event radiation effects basics

The natural space radiation environment contains high-energy protons and heavy ions that can introduce transient, dense charge filaments along the path of the ion through an electronic device that can interact with sensitive regions of the device to trigger single event effects.<sup>2,3</sup>

The sensitivity of a semiconductor device to single-event effects is expressed as the ratio of the number of events to the total particle fluence. The resulting ratio is referred to as the cross-section since it has units of  $\text{cm}^2$ . Laboratory cross-section data are often presented as a function of linear energy transfer (LET), which is related to the energy of the incident ion. The energy loss of the incident ion is expressed in terms of LET with typical units of  $\text{MeV}\cdot\text{cm}^2/\text{mg}$ .<sup>32</sup> The energy loss results in the creation of electron-hole pairs along the ion track. There are two key parameters from such data: the saturation cross-section,  $\sigma_{\text{sat}}$ , and the threshold LET,  $L_{\text{th}}$ . The saturation cross-section is related to the total area of the sensitive regions of the component, and the threshold LET is a measure of the critical, or minimum, charge required to trigger the event. These parameters are essential in estimating the single-event error rate for a particular environment. In Figure 8, the concepts of saturation cross-section and threshold LET are illustrated.

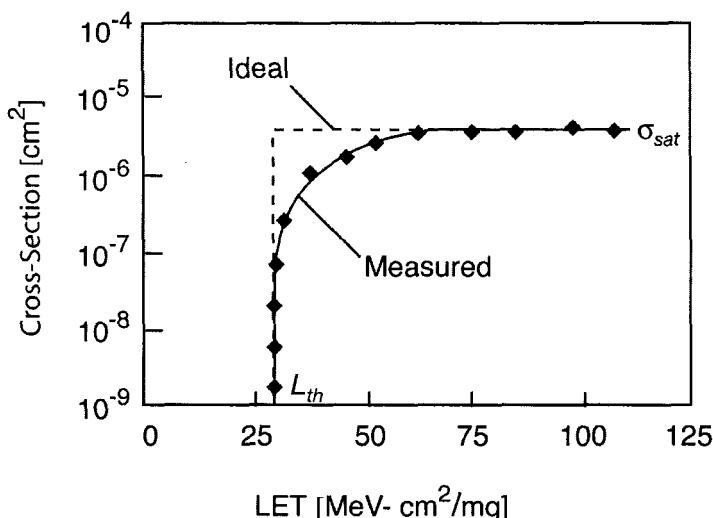


Fig. 8. A typical measured and ideal cross-section curve plotted against the LET of the incident ion.

Two single-event effects are of particular interest for power MOSFETs: single-event burnout (SEB) and single-event gate rupture (SEGR). These are catastrophic failure mechanisms that are initiated by the passage of a heavy ion through sensitive regions of the device structure. SEB of power MOSFETs was first reported by Waskiewicz, *et. al.* and SEGR of power MOSFETs was first reported by Fischer.<sup>35,36</sup>

#### 4.b. Single event burnout

Recall that the VDMOS power transistor is capable of conducting large currents when turned *ON* and withstanding large voltages when turned *OFF*. A schematic cross-section of an n-channel VDMOS power transistor appears in Figure 1. Note the parasitic npn bipolar junction transistor (BJT) inherent to the DMOS structure. The source, body, and drain regions of the MOSFET comprise the emitter, base, and collector regions of the parasitic BJT, respectively. During normal operation of the power MOSFET, this parasitic BJT is always turned off due to the common source-body metallization that shorts out the base-emitter junction.

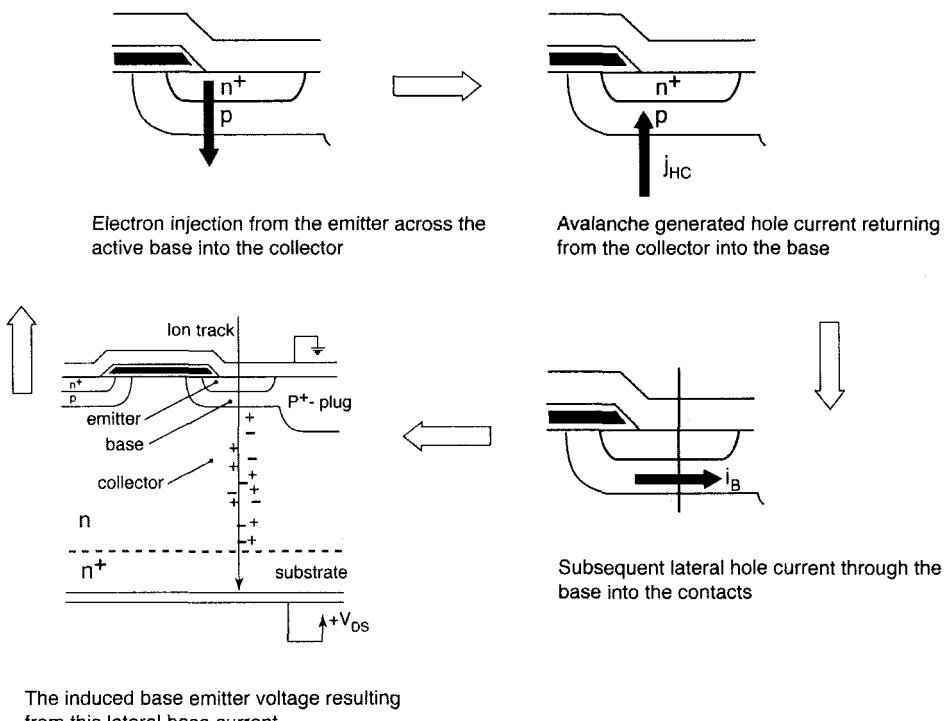


Fig. 9. SEB Triggering Mechanism

As shown in Figure 9, SEB is triggered when a heavy ion passes through a power MOSFET that is biased in the *OFF* state (blocking a high drain-source voltage). Transient currents generated by the heavy ion turn on the parasitic BJT of the power MOSFET.<sup>37</sup> Due to a regenerative feedback mechanism, collector currents in the parasitic BJT increase to the point where thermal failure creates a *permanent* short between the source and drain, rendering the MOSFET useless. A key component of the regenerative feedback mechanism is avalanche-generated hole current in the collector region of the BJT. SEB of p-channel power MOSFETs has not been reported in the literature. While p-channel power MOSFETs may be susceptible to SEB, it is less probable than for n-channel devices because the impact ionization rate for holes is less than that for electrons, making the magnitude of avalanche-generated currents lower than for n-channel devices.

A considerable amount of data related to single event burnout has appeared in the literature including the results on a space experiment.<sup>38-40</sup> A typical cross section for SEB is shown in Figure 10. In addition, numerous papers have been published to elucidate the physical effects and provide simulation and modeling of SEB.<sup>37,41-45</sup> The references here are not inclusive; however, these will point the interested reader to many other results.

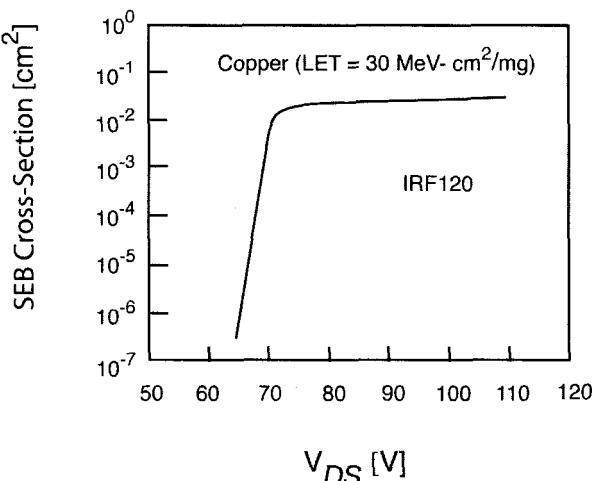


Fig. 10. Typical SEB cross-section versus VDS for a power MOSFET exposed to a mono-energetic copper ion beam giving a LET of 30 MeV·cm<sup>2</sup>/mg. After ref 39.

#### 4.c. Single event gate rupture

Although SEB and single-event gate rupture (SEGR) are both caused by the passage of a heavy ion through the device, the failure mechanisms are altogether different. Recall, SEB occurs when the parasitic BJT is turned on and the regenerative feedback mechanism is triggered. SEGR, on the other hand, is caused by heavy-ion-induced localized dielectric breakdown of the gate oxide.<sup>46,47</sup> In Figure 11, a DMOS device is shown with an incident ion track in the gate-drain overlap (neck) region. Under appropriate bias conditions, accumulation of charge in the silicon (generated by the heavy ion) at the Si-SiO<sub>2</sub> interface in the gate-drain overlap region (*i.e.*, the neck region) can

result in sufficiently high electric fields across the gate oxide to cause a localized gate rupture (*i.e.*, localized dielectric breakdown). In addition, the charge generated in the oxide briefly reduces the breakdown field of the oxide. Subsequent gate to drain current results in a thermal runaway condition, melting a *permanent* short between the gate and drain and rendering the MOSFET useless.

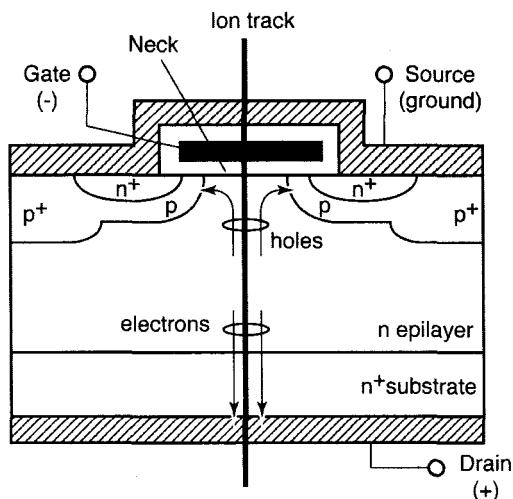


Fig. 11. SEGR is initiated when an incident ion passes through the gate-drain overlap region of the VDMOS power transistor.

Wheatley *et. al.* obtained an extensive matrix of the gate to source biases,  $V_{GS}$ , and drain to source biases,  $V_{DS}$ , necessary to induce SEGR in a particular power MOSFET structure exposed to mono-energetic heavy ions at a given LET.<sup>48</sup> Over 400 transistors from the same wafer lot and heavy ions with LETs that ranged from 0 to 83 MeVcm<sup>2</sup>/mg were used in the study (an LET of zero means no ion was incident and represents the control case for the experiment). Figure 12 schematically depicts their results. Later Titus *et. al.* extended their matrix and included gate oxide dependence.<sup>49</sup> Also, Nichols *et. al.* provided SEGR data for a variety of commercially available power MOSFETs.<sup>50</sup> Work has also been done by Titus *et. al.* to predict SEGR failures in commercial space systems.<sup>51</sup>

Due to the destructive nature of SEGR, it is difficult to display data as a cross-section (see Figure 10). SEGR data have usually been displayed as in Figure 12. The single-event cross-section is the ratio of the total number of events to the total ion fluence. In the case of SEGR, the total number of events is one and the ion fluence is the number of ions required to trigger SEGR. An example of an SEGR cross-section is given in Figure 13.<sup>52</sup>

The single-event gate rupture phenomenon has been successfully modeled using two-dimensional device simulations.<sup>45,53-55</sup> Technologies have been developed that reduce SEGR susceptibility.<sup>56</sup> Again, the references given here for SEGR are not inclusive; however, they will point the interested reader to many other results.

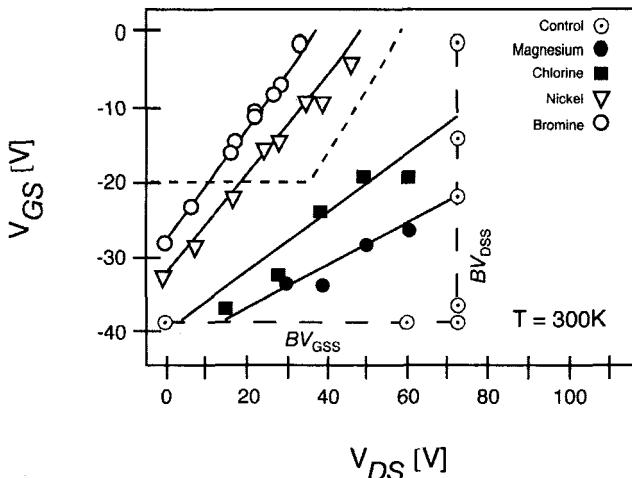


Fig. 12. SEGR experimental data after ref. 48 Bromine (LET = 37.3); Nickel (LET = 27); Chlorine (LET = 11.5), Magnesium (LET = 6).

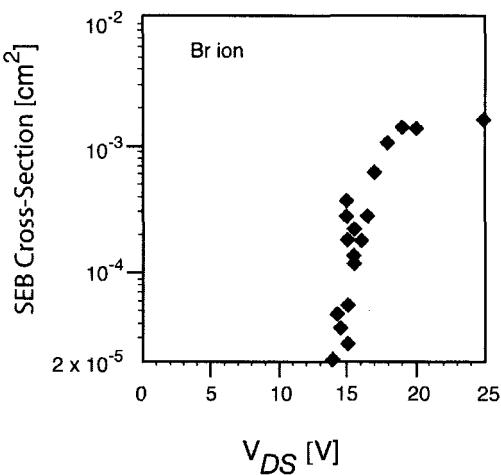


Fig. 13. Measured SEGR cross-section versus drain-source bias after ref. 52.

## 5. Conclusions

Power MOSFET technology is important to both military and civilian spaceborne efforts. It has a number of advantages over power bipolar technologies. This paper has briefly reviewed the current technology, its high frequency capability, and the future trends for power MOSFET technology. In addition, it has delineated a number of the susceptibilities that the power VDMOS technology has in the space environment. These susceptibilities

that the power VDMOS technology has in the space environment. These susceptibilities must be considered when designing circuits for spaceborne systems utilizing these devices.

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## INTRODUCTION TO SOI MOSFETs: CONTEXT, RADIATION EFFECTS, AND FUTURE TRENDS

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The context of SOI technology is briefly presented in terms of wafer fabrication, configuration/performance of SOI devices, and operation mechanisms in partially and fully depleted MOSFETs. Typical radiation effects, induced by single particles and cumulated dose, are evoked: BOX degradation, parasitic bipolar action, coupling effects, transistor latch, and back-channel conduction. The future of SOI is tentatively explored, by discussing the further scalability of SOI-MOSFETs as well as the innovating architectures proposed for the ultimate generations of SOI transistors.

*Keywords:* SOI; radiation; transistor.

### 1. Introduction

Silicon-On-Sapphire (SOS) was the initial Silicon On Insulator (SOI) technology, developed for the fabrication of radiation-hard circuits. Four decades of research in material science and device physics resulted in new types of SOI structures and integrated circuits with high performance.<sup>1,2</sup> The basic SOI concept is to dielectrically separate, using a buried oxide (BOX), the active device volume from the Si substrate. The adjustability of the film thickness is actually the main asset of the SOI technology in terms of enhanced performance and superior scalability. It is hard to imagine the CMOS scaling beyond the 25–35 nm generation without making use of thin-film SOI MOSFETs.<sup>3,4,5,6</sup>

Although interest in SOI expanded from the niche of radiation-hard devices to the mainstream microelectronics, the integrated circuits continue to be exposed to radiations.<sup>7,8</sup> The natural environment, from high altitudes to ground level, involves a significant flux of heavy and light particles, which contribute to degrade

the component reliability. This implies that the relevance of radiation effects is accentuated as the SOI centroid was shifted from defense and space electronics towards commercial components.

The aim of this paper is to provide an introduction to SOI, with particular focus on radiation effects, which can be used to decode more specialized publications. In sections 2, we briefly present the current status of the SOI technology. The typical mechanisms of operation of fully and partially depleted MOSFETs are addressed in section 3. Section 4 contains an overview of the main radiation effects in SOI MOSFETs. More detailed analysis and systematic data is available in other papers of this special journal issue. In section 5, we attempt to give a flavor of the future trends in SOI.

## 2. Current Status of SOI Technology

### 2.1. Prime merits of SOI devices

SOI circuits consist of single-device silicon islands, dielectrically isolated from each other and from the underlying substrate (Fig. 1). The lateral isolation offers more compact design and simplified technology than in bulk silicon: there is no need of wells or interdevice trenches. In addition, the vertical isolation prevents the *latch-up* mechanism which is detrimental in bulk-Si.

The source/drain regions normally extend down to the buried oxide (BOX) so that the junction surface is minimized. The leakage current and the off-state power dissipation are therefore reduced. The junction capacitance, which governs the switching speed as well as the dynamic power dissipation, is also dramatically improved. The limited cross-section of the junctions enables SOI circuits, especially fully depleted CMOS, to operate in a wider temperature range and to be less affected by short-channel effects (section 5).

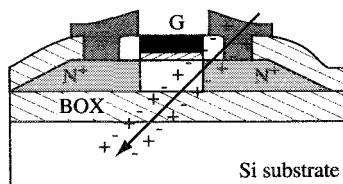


Fig. 1. Schematic architecture of an SOI MOSFET under radiation.

It is in the highly competitive domain of low-power & low-voltage circuits that SOI is most attractive. SOI offers a quasi-ideal subthreshold slope (60 mV/decade at room temperature), hence the opportunity to shrink the threshold voltage below 0.3 V. Frequencies beyond 150 GHz and delay times below 10 ps/stage<sup>9,10</sup> have been

reached and operation at 0.5–0.9 V has been demonstrated. It has been repeatedly proven that SOI circuits operate 20–30 % faster, in other words the SOI generation ( $n$ ) and the *next* bulk-Si generation ( $n+1$ ) perform comparably. We do not include specific examples because new records are frequently set, their ephemeral existence reflecting the health and progress of SOI technology.

As far as the reliability is concerned, SOI MOSFETs are extremely robust to *transient* radiation effects because the charge collection volume is, in principle, proportional to the film thickness. We will see in the following sections that the *permanent* radiation-induced damage in the BOX is the main issue. The integrity of the gate oxide is another problem which can be solved by reducing the defect density in the film. SOI MOSFETs are rather resistant to hot carrier damage because the electric-field peak is lower than in bulk Si. Another difference with bulk-Si MOSFETs is the impact of electrostatic discharge (ESD) and the design solutions to eliminate the charge from the isolated body.

Besides the fully and partially depleted MOSFETs, the family of SOI devices also includes bipolar and high-voltage DMOS transistors (with lateral configuration), smart power devices, 3-D circuits, optical switches, waveguides and modulators, microwave transistors on high resistivity SOI wafers, etc.<sup>1,2</sup> Most innovative devices make use of the possibility to (i) combine bulk-Si power devices with low-power control SOI MOSFETs on a single chip containing localized SOI regions, (ii) adjust the thickness of the Si overlay and buried oxide, and (iii) implement metal layers or additional gates underneath the BOX. SOI is also an ideal material for microsensors and MEMS, where very thin membranes are fabricated by using the interface between the BOX and substrate as a perfect etch-stop mark.

## 2.2. SOI materials

The market of device-grade SOI wafers is currently shared by Unibond and SIMOX. Unibond process uses the deep implantation of hydrogen to generate a plane of microcavities in an oxidized wafer.<sup>11</sup> After bonding to a second wafer and annealing, this plane allows the wafers to separate naturally (Smart-Cut), leaving a thin SOI film (Fig. 2c). Eltran wafers are also prepared by bonding, except that the splitting is defined by a sacrificial layer of porous silicon, on which the Si film has been epitaxied.<sup>12</sup> In these bonding processes, only the wafer which provides the Si film needs to be premium quality. The multiple slicing and recyclability of these wafers is a key economic argument.

Unibond and Eltran are very flexible and can both provide, in 300 mm wafers, unlimited combinations of BOX and film thickness. The BOX and film-BOX interface have thermal-oxide quality. The bonding interface is more defective and more receptive to radiation effects. In particular, electron-paramagnetic resonance studies in Unibond have shown the presence of hydrogen-related defects near the bonding region.<sup>13</sup> However, the bonding interface has a minor impact on the device performance because it is located underneath the BOX. As far as the *active*

interface is concerned, the density of interface states that may be induced by the released hydrogen is not significant up to very high total doses (about 1 Mrad). The electrical properties being excellent, it is not clear whether the film quality can reflect the impact of either implanted hydrogen (Unibond) or epitaxy on porous Si (Eltran). Stress effects in ultra-thin structures also need evaluation.

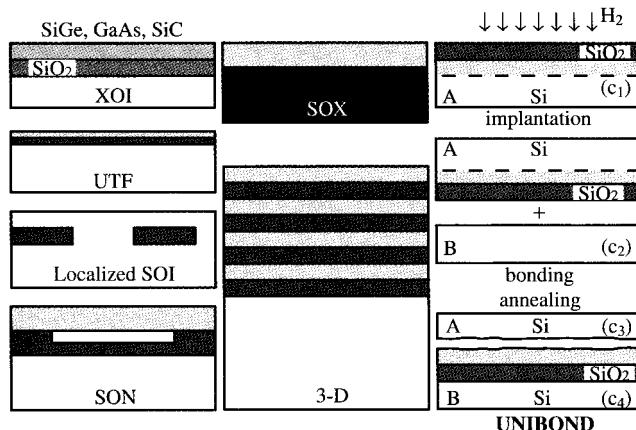


Fig. 2. Unibond process (c<sub>1</sub>-c<sub>4</sub>) and innovative SOI-like structures: *other* semiconductor on insulator (XOI), ultra-thin film and buried oxide (UTF), interrupted BOX, silicon on nothing (SON), silicon on *other* dielectric (SOX), 3-D Si-BOX 'super-lattices'.

SIMOX is synthesized by deep implantation of large doses of oxygen and high temperature annealing, which results in a BOX with special microstructure. Typical defects are interface traps, hole and electron traps in the BOX, the latter being activated by exposure to radiation.<sup>14,15,16,17</sup> The quality of the BOX and interfaces has dramatically been improved and the defects in the film have been erased, except the threading dislocations. The trend is to achieve thinner films (< 100 nm) and BOX (< 150 nm) by reducing the implant energy and dose, and also by adding special implantation/anneal steps (ITOX and new Ibis/IBM materials).

SOS material is still handicapped by the mediocre quality of the epitaxial Si film and interface. SOS hardly survives for the benefit of radiation-hard and RF circuits, for which the presence of an 'infinite' dielectric substrate is an ideal solution. Silicon on Nothing (SON) has recently been proposed as a solution for synthesizing *localized* SOI-like structures within a bulk-Si wafer (Fig. 2).<sup>18</sup> Several other SOI materials have temporarily emerged and disappeared:<sup>1</sup> silicon on zirconia, FIPOS (*Full Isolation by Porous Oxidized Silicon*), ZMR (*Zone Melting Recrystallization*), *Epitaxial Lateral Overgrowth* (ELO or other acronyms) is still being considered for 3-D integration and double-gate MOSFETs.

The fabrication of very advanced devices will require not only extremely thin SOI films but also a new class of SOI-like materials (Fig. 2). Using bonding techniques, the silicon film can be replaced by other semiconductors (SiGe, III-V or II-VI compounds, etc) with attractive optical and electrical properties. Alternatively, the BOX can be traded in for other types of insulators (sapphire, diamond, glass, flexible plastic, air) which may offer improved thermal dissipation, enhanced RF performance, new optical functions, and portability.

The large variety of SOI structures makes the signature of radiation-induced defects to differ according to the conditions of synthesis. The pseudo-MOS transistor ( $\Psi$ -MOSFET) is a simple and elegant method to monitor the generation of BOX, film and interface defects during *radiation*.<sup>19,20</sup> SOI is a natural upside-down MOS structure, where the Si substrate acts as a gate terminal and can be biased to induce a conduction channel (inversion or accumulation) at the interface. The BOX plays the role of a gate oxide and the Si film represents the transistor body. Low-pressure probes are placed on the film and form source and drain point contacts (Fig. 3).<sup>19</sup>

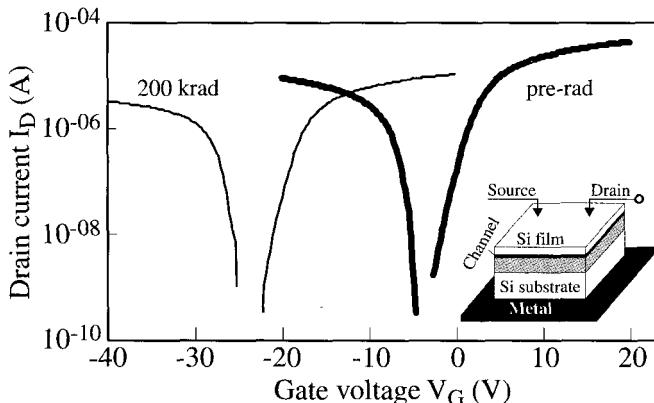


Fig. 3. Configuration of the pseudo-MOS transistor and typical  $I_D(V_G)$  characteristics in a thin SOI film, before and after radiation.

Very pure MOSFET-like characteristics are produced. In strong inversion/accumulation and ohmic region, the drain current is given by

$$I_{DS} = f_g \mu C_{ox} V_D (V_G - V_{T,FB}) \quad (1)$$

where  $f_g \simeq 0.75$  is the aspect ratio. The slope of  $I_D/\sqrt{g_m}$  vs.  $V_G$  curves yields the mobility of electrons and holes, whereas the intercept with the  $V_G$  axis gives the threshold ( $V_T$ ) or the flat-band ( $V_{FB}$ ) voltage.<sup>20</sup>

The density of traps at the film–BOX interface is calculated from the subthreshold slope in weak inversion, the fixed charge density from  $V_{FB}$ , and the film doping from the difference  $V_T - V_{FB}$ . The carrier lifetime can be evaluated by recording the transient drain current after the gate is pulsed in strong inversion.

### 3. Operation Mechanisms in SOI MOSFETs

#### 3.1. Fully depleted MOSFETs

In fully depleted MOSFETs, the depletion region covers the whole transistor body and does not extend with gate bias. Interface coupling causes the front-gate measurements to depend on the back gate bias  $V_{G_2}$  as well as on BOX thickness and interface defects. Totally different  $I_D(V_{G_1})$  relations describe the complex characteristics of the front-channel transistor (Fig. 4).

**Threshold voltage.** In depletion regime, the threshold voltage  $V_{T_1}^{dep}$  decreases linearly with  $V_{G_2}$  between two plateaus corresponding respectively to accumulation and inversion at the back interface (Fig. 4d):<sup>21</sup>

$$V_{T_1}^{dep} = V_{T_1}^{acc} - \frac{C_{si} C_{ox_2} (V_{G_2} - V_{G_2}^{acc})}{C_{ox_1} (C_{ox_2} + C_{si} + C_{it_2})} = V_{T_1}^{acc} - k_1 (V_{G_2} - V_{G_2}^{acc}) \quad (2)$$

where  $C_{si}$ ,  $C_{ox}$ ,  $C_{it}$  are the capacitances of the fully-depleted film, oxide, and interface traps, respectively. The subscripts 1 and 2 hold for the front or the back channel parameters. They can be interchanged in order to account for the variation of the back-channel threshold voltage  $V_{T_2}$  with the front-gate voltage  $V_{G_1}$ . Usually,  $C_{ox_2}$  and  $C_{it_2}$  are much smaller than  $C_{si}$ , hence the slope  $k_1$  of the  $V_{T_1}(V_{G_2})$  curve can be approximated by the ratio of the front-gate oxide and buried oxide thickness  $k_1 \approx t_{ox_1}/t_{ox_2}$ .

**Subthreshold slope.** The front-channel subthreshold swing  $S_1$  is given by:

$$S_1 = 2.3 \frac{kT}{q} \left( 1 + \frac{C_{it_1}}{C_{ox_1}} + \alpha_1 \frac{C_{si}}{C_{ox_1}} \right) \quad (3)$$

For depletion at the back interface, the coupling coefficient  $\alpha_1$

$$\alpha_1 = \frac{C_{ox_2} + C_{it_2}}{C_{si} + C_{ox_2} + C_{it_2}} < 1 \quad (4)$$

accounts for the influence of back interface traps  $C_{it_2}$  and BOX thickness  $C_{ox_2}$ .<sup>22</sup>

By accumulating the back channel, the front inversion channel becomes decoupled from back interface defects but, in turn, coefficient  $\alpha_1$  tends to unity (as in bulk-Si or partially-depleted MOSFETs), causing an overall degradation of the swing (Fig. 4e).

The above equations are valid only when the buried oxide is thick enough so that substrate effects occurring underneath the BOX can be ignored. Otherwise, 3-interface models become necessary. The general trend is that the subthreshold slope improves for thinner silicon films and thicker BOX.

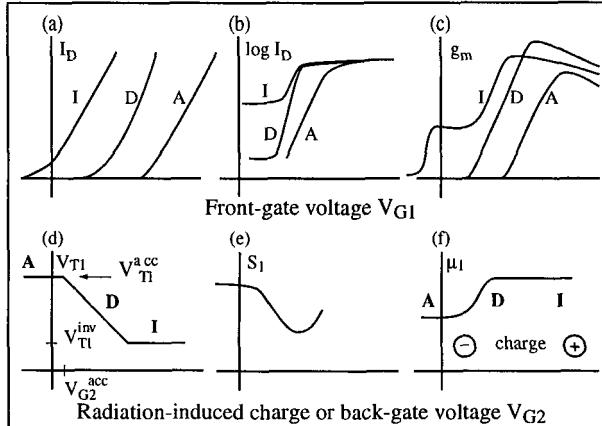


Fig. 4. Generic front-channel characteristics of a fully-depleted n-channel SOI MOSFET for different conditions at the back interface: accumulation (A), depletion (D), and inversion (I). The top characteristics are: (a)  $I_D(V_{G1})$  in strong inversion, (b)  $\log I_D(V_{G1})$  in weak inversion, and (c) transconductance  $g_m(V_{G1})$ . The bottom curves indicate the variation of the corresponding parameter with radiation dose (or back gate bias): (d) threshold voltage, (e) subthreshold swing, and (f) electron mobility.

**Transconductance.** In strong inversion and ohmic region, the transconductance is

$$g_{m1} = \frac{C_{ox1} W V_D}{L} \cdot \frac{\mu_1}{[1 + \theta_1(V_{G1} - V_{T1}(V_{G2}))]^2} \quad (5)$$

where  $\mu_1$  is the mobility of front channel carriers, and  $\theta_1$  is the mobility attenuation coefficient.

The complicated transconductance curves in fully depleted MOSFETs (Fig. 4c) are explained by the influence of the back gate bias on front-channel threshold voltage (Eq.(2)), and carrier mobility. The effective mobility and transconductance are maximum for depletion at the back interface (Fig. 4f), due to combined effects of reduced vertical field and series resistances.<sup>23</sup>

The distortion of the transconductance (curve I, Fig. 4c) reflects the activation of the back channel: increasing  $V_{G1}$  reduces the back threshold voltage and opens the back channel, while the front interface is still depleted.<sup>23</sup>

### 3.2. Partially depleted MOSFETs

In partially-depleted SOI MOSFETs, a neutral region subsists and cancels the interface coupling effects. When the body is grounded, most of the standard  $I_D(V_G, V_D)$  equations developed for bulk-Si MOSFETs apply. In contrast, if body contacts are not supplied, several *floating-body* effects arise.

The *kink effect* is triggered by majority carriers, which are generated by impact ionization and accumulate in the body: the body potential is gradually increased and the threshold voltage is lowered. The kink results in excess drain current and low-frequency noise.<sup>24</sup>

In weak inversion and for high drain bias, a similar positive feedback is responsible for negative resistance regions, *hysteresis* in log  $I_D(V_G)$  curves, and eventually transistor *latch* (see Fig. 9).

The charging of the body also leads to the forward biasing of the source-to-body junction and to a parasitic bipolar effect. The activation of the *parasitic bipolar transistor* yields more current but causes premature breakdown.

Transient currents are other typical floating body effects. A drain current *overshoot* occurs when the gate is turned on. Majority carriers are expelled from the depletion region and collect in the body, so increasing the potential. Equilibrium is reached through electron-hole recombination, which makes the drain current decrease gradually with time. A reciprocal *undershoot* is observed when the gate is switched from strong to weak inversion: the current increases with time as the generation process of majority carriers allows the depletion depth to shrink. In advanced MOSFETs, the transients are remarkably reduced, either by the proximity of source and drain junctions which efficiently remove the majority carriers, or by the gate tunneling current.<sup>25</sup>

During high-frequency switching of integrated circuits, the transistor body does not always succeed to reach equilibrium. The charging and discharging of the body is an iterative process which may cause *history* and *memory* effects as well as dynamic instabilities.

Partially-depleted transistors with dynamic threshold (DT-MOSFETs) are very attractive for low-voltage/low-power CMOS circuits. The gate and body are interconnected: increasing the gate voltage in weak inversion causes a simultaneous raise in body potential and a gradual decrease in threshold voltage (dynamic  $V_T$ ). The gate-charge coupling is excellent and results in improved subthreshold slope, current, transconductance, and short-channel effects.

#### 4. Radiation Effects on SOI MOSFETs

The radiation effects, critical for space applications, also appear at the ground level. The charge stored in elementary nodes decreases with technology integration, down to a few femto-coulomb, and can be easily upset by the radiation deposited charge. Charge is deposited by either direct or indirect ionizing effect.<sup>26</sup> The heavy charged particles encountered in the space environment produce a direct ionizing effect by interaction with the electronic corage of atoms. On the other hand, the light particles, protons in space and neutrons in the atmospheric environment, induce an indirect ionizing effect through their nuclear interaction with silicon nucleus or other chemical elements of the chip. The charge is then deposited by the produced recoil heavy charged particles along their track in the device.

Depending on the struck region and the applied electric field, the charges are separated and induce either transient or permanent damage:

- (i) **Soft Errors.** Charges are swiftly transported to elementary transistor terminals and give rise to a parasitic transient current. If this current is high enough, permanent damage (gate rupture, burnout) can occur. In most cases, the deposited charge induces a Single Event Upset (SEU), *i.e.*, a local change of the logic information contained in DRAMs and SRAMs. These SEUs are ‘soft errors’ as the memory cell can be re-written without permanent damage.
- (ii) **Cumulated Dose.** The cumulative charge deposited in the insulators tends to build a trapped charge density, which causes a permanent shift of device parameters (threshold voltage, off and on currents). Thick oxide parts, mainly lateral isolations and buried oxides, are particularly sensitive to radiation-induced trapped charge.

#### **4.1. Parasitic conduction and impact of radiations**

When an ionizing particle crosses the drain region of a bulk-Si MOSFET, a typical funneling phenomenon occurs. It consists in the distortion of the drain junction electric field along the particle track, which induces a collection of the generated charges on several microns. The funneling can activate the parasitic latch-up structure (between junctions, wells, and substrate) which is inherent to bulk devices. In SOI transistors, the total dielectric isolation suppresses the latch-up structure, reduces the role of the drain junction, and limits the collection to the charges generated in the thin silicon film only. However, this advantage is mitigated by several parasitic structures, typical to SOI transistors.<sup>27</sup>

- (i) *The parasitic bipolar transistor* can be triggered under irradiation, when parasitic charges accumulate in the body and forward bias the body-source diode. To avoid the bipolar onset, the body is tied to the source so that the generated charge is evacuated.<sup>28,29,30</sup> The body ties are space consuming. Other solutions are Ge implantation to reduce the majority carrier lifetime,<sup>31</sup> partial trenches,<sup>32</sup> BUSFET.<sup>33</sup>
- (ii) *The parasitic back-gate transistor* is triggered under cumulative dose effect. Usually, a net positive charge is trapped, leading to a possible parasitic conduction in N-channel MOSFETs.
- (iii) *The lateral parasitic transistor* is activated by charge trapping in the lateral isolation (LOCOS, STI), and induces a leakage current on the transistor edges.<sup>34</sup> A similar structure also exists in irradiated bulk devices.<sup>35</sup>

The front-gate oxide is so thin that the dose effect is negligible. We will see next that more important is the difference between fully or partially depleted architectures in terms of SEU and total dose sensitivity.

#### 4.2. Single event effects

The parasitic bipolar action is effective when the body is left floating. After an ionizing particle strikes, the electron-hole pairs generated in the body are separated by the local electric field. Minority carriers drift towards the drain, while majority carriers tend to accumulate in the body. They contribute to forward bias the body-source junction, and to trigger the parasitic bipolar.

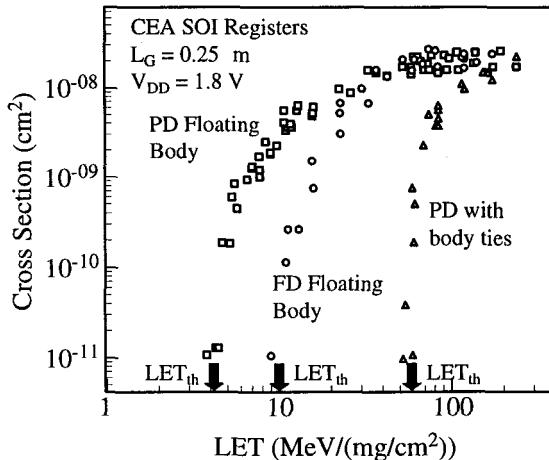


Fig. 5. Heavy ion cross-section versus effective Linear Energy Transfer (LET) in typical SOI circuits (registers). The graph shows the improvement achieved by using body ties.<sup>27,38</sup>

The bipolar current amplifies the charge collection.<sup>36,37</sup> The total collected charge,  $Q_{coll}$ , corresponds to the amplification of the irradiation deposited charge  $Q_{dep}$ . A soft error may arise if  $Q_{coll}$  is higher than the (minimum) critical charge,  $Q_{crit}$ , able to upset a memory cell:

$$Q_{coll} = (1 + \beta) \times Q_{dep} \geq Q_{crit} \quad (6)$$

where  $\beta$  is the bipolar gain. The higher  $\beta$ , the lower  $Q_{dep}$  able to induce an upset.  $Q_{dep}$  is defined with the Linear Energy Transfer (LET) of the ion, when crossing the sensitive region. In normal incidence, the deposited charge in the silicon film is given by:

$$LET[MeV \cdot mg^{-1}cm^2] \times t_{si}[\mu m] = Q_{dep}[pC] \times 96.9 \quad (7)$$

where  $t_{si}$  is the film thickness and the conversion factor 96.9 is valid in silicon.

For analysis of the device sensitivity, components are tested with different LET particles (Figure 5). The sensitive cross-section  $\sigma$  is deduced from the number of errors  $N_{err}$ , and the total particle fluence. The cross-section can be normalized

by the number of bits for memories or registers, which enables the comparison of components with different complexity. The cross section then represents the sensitive surface of the memory (or register) cell.

$$\sigma [cm^2] = N_{err}/(Fluence[cm^{-2}] \times Bits) \quad (8)$$

Figure 5 shows the sensitivity of fully and partially depleted devices. The threshold LET or  $LET_{th}$  corresponds to the lowest deposited charge able to induce an upset:  $Q_{dep} = Q_{crit}/(1+\beta)$ . Fully depleted circuits are less sensitive than the equivalent partially depleted ones.<sup>27,38</sup> This is due to a thinner silicon layer and a lower bipolar gain for the fully depleted devices.

The adjunction of body ties allows to reduce the bipolar amplification and to increase the threshold LET. It is an efficient method for both fully and partially depleted devices.<sup>27,39</sup>

The bipolar amplification can even lead to snap-back.<sup>40</sup> The impact ionization in the drain region generates additional carriers, which maintain the body-source junction forward biased, so that the transistor can not return instantly to its initial off-state.

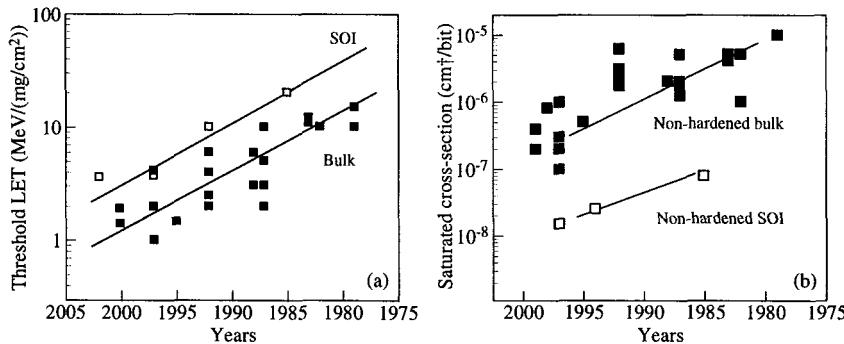


Fig. 6. (a) Threshold LET and (b) saturated cross-sections in non-hardened SOI and bulk-Si circuits as a function of the technology generation. The data is extracted from literature on SOI and bulk SRAMs.<sup>39,41,42,43,44,45,46,47,48</sup>

Only few references compare standard thin SOI (non-hardened and without body ties) with bulk devices of the same generation. A compilation of experimental data obtained on SOI and bulk devices shows that commercial SOI (without body ties) and bulk circuits have a rather similar threshold LET (Fig. 6a).<sup>39,41,42,43,44,45,46,47,48</sup> On the other hand, SOI has a significantly lower sensitive cross-section (Fig. 6b).<sup>41</sup> For the 2000 generation node, an SOI device has a typical cross-section of about  $1\mu m^2/\text{bit}$ , which is one order of magnitude lower than in bulk. Furthermore, technology down-scaling induces a decrease of both the cross-

section and the threshold LET of SOI and bulk devices. This is consistent with respectively a more compact design and a reduced critical charge with integration.

In SOI, it is commonly admitted that the sensitive cross-section is reduced to the gate surface which covers the body region. However, recent micro-beam experiments on a  $0.35\text{ }\mu\text{m}$  SOI technology showed that the drain region can also be sensitive to high LET particle strikes.<sup>49</sup> Actually the drain doping has been shown to be the key parameter of the SOI drain sensitivity.<sup>38</sup> When the drain is not strongly doped down to the buried oxide, the generated charge does not recombine completely. Subsisting charges are drifted towards the body region where they contribute to the bipolar amplification effect. The drain sensitivity can be avoided by carefully tailoring the doping profile.

#### 4.3. Total dose effects

The typical effect in SOI is the charge accumulation in the BOX. Back-channel measurements provide a direct insight into the BOX defects responsible for radiation-induced degradation. The two main types of buried oxides, SIMOX and UNIBOND, present similar qualitative trapping properties:

- (i) An uniform trap density in the volume of the BOX.<sup>50</sup> This special feature is presumably due to the high temperature anneal ( $1100^\circ\text{C}$  for UNIBOND,  $1350^\circ\text{C}$  for SIMOX) that ends the SOI substrate process. By contrast, in conventional thermal oxides, the trap density is located near the oxide-silicon interface.
- (ii) A positive charge trapping, partially compensated, especially at high radiation dose, by electron trapping. The trapping centers are due to structural defects, like constraint or dangling bonds, oxygen vacancies, silicon clusters, etc.<sup>51</sup>

The contributions of both species, holes and electrons, have been demonstrated by back-channel measurements.<sup>14</sup> Figure 7 reveals several distinct mechanisms according to the bias applied to the back gate during exposure to radiations. For positive bias, radiation-induced electron-hole pairs are separated by the field and the holes are driven towards the upper interface of the BOX. A net positive charge is build-up, yielding a very large decrease in the back-channel threshold voltage  $V_{T_2}$ . For zero bias, most of the electron-hole pairs recombine instantly, hence  $V_{T_2}$  shift is attenuated. But, for negative bias, the pairs again separate and the holes are attracted to the bottom BOX interface. The positive charge effect still dominates for low doses, whereas beyond 100 krad a rebound is observed. The large increase in  $V_{T_2}$  accounts for electron trapping near the film-BOX interface, which modifies the surface potential as well as the series resistance of the transistor.<sup>14</sup>

In *partially-depleted* devices, charge trapping in the BOX induces the parasitic conduction of the back-gate transistor, as illustrated in Figure 8. Under usual bias conditions (back gate grounded), the leakage current is observed in n-type MOS transistors, due to a net positive trapped charge in the buried oxide. Above a threshold dose (300 krad(SiO<sub>2</sub>) in Fig. 8), the back-channel transistor is clearly

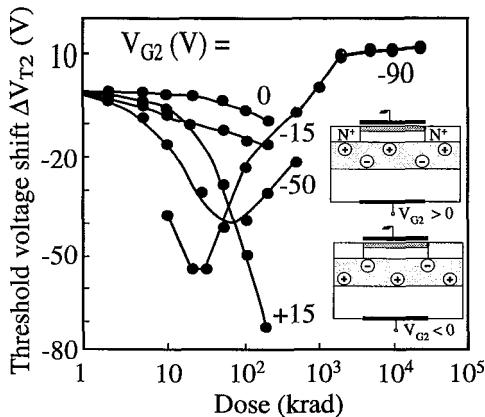


Fig. 7. Radiation-induced shift of the back-channel threshold voltage in a SIMOX MOSFET.<sup>14</sup>

conducting even for  $V_{G2} = 0$ . The parasitic current flows at the bottom interface of the silicon film (Fig. 8a), and adds to the main transistor current. In partially depleted devices, such a ‘leakage’ current cannot be controlled by the front gate (no coupling action); this prevents the main transistor from switching off (Fig. 8b).

Below the threshold dose, the neutral region can in principle protect the front channel from the detrimental impact of radiation-induced damage in the BOX. This is not totally true, because several subtle mechanisms can arise. For example, a positive charge in the BOX will lower the series resistance of LDD regions, increasing the impact ionization rate and the body charging. As a consequence, hysteresis and latch can be activated during radiation. The transient and history effects are also modified as soon as the generation-recombination rate in the volume or at the BOX and sidewall interfaces is increased.

*Fully-depleted* devices are characterized by the strong coupling effect between the front and the back gate transistor. Carriers flowing at one interface are influenced by the presence of defects at the opposite interface. This *defect coupling* is responsible for an apparent degradation of the front-channel characteristics, which is actually due to radiation-induced damage in the BOX. For example, the generation of back interface traps alters the threshold voltage and subthreshold swing according to Eqs.(2) and (3).

When irradiating fully depleted devices, the trapped charge in the BOX acts as a build-in positive back-gate voltage. It induces a strong shift of the front-channel threshold voltage (for example as in Fig. 4a,d).<sup>52,53</sup> As long as the transistor remains in full depletion mode,  $\Delta V_{T1}$  is directly proportional to the back-channel threshold voltage shift induced by charge trapping into the BOX:  $\Delta V_{T1} \simeq k_1 \Delta V_{T2}$  (see Eq.(2)). In addition, the build-up of a fixed charge in the BOX can result in

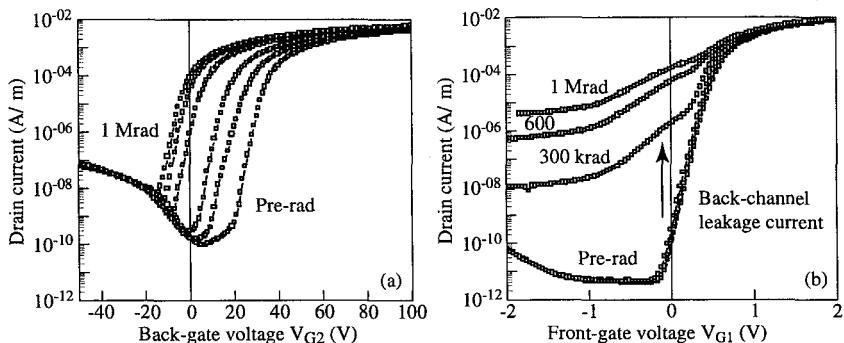


Fig. 8. Drain current versus back gate (a) and front gate (b) bias in a partially depleted n-channel SOI MOSFET, at low drain bias and after several doses of radiation. The transistor was in off-state during radiation. The trapping of positive charges in the BOX induces a negative shift of the back-channel threshold voltage. The back channel current increases the apparent leakage current of the front-channel transistor.<sup>27</sup>

a modification of the back surface potential (accumulation, depletion or inversion), changing the mode of operation of the front channel, as shown in Figure 4. The transconductance may also be affected by the modulation of the series resistance.

An apparent solution to improve the radiation hardness of fully-depleted transistors is to use a thinner BOX. However, the coupling coefficient is enhanced and the front transistor becomes more sensitive to the charge trapped in the BOX. This is why a thinner BOX does not significantly improve the radiation hardness of fully depleted devices.<sup>34</sup> A more effective solution is to use a hardened buried oxide, with a low trap density.<sup>54,55</sup>

Total dose deposition can also result in a transistor latch effect. Figure 9 shows the static characteristics  $I_D(V_{G1})$ , at high drain bias, for irradiated SOI transistors.<sup>56</sup> For a 'critical' dose, a hysteresis phenomenon appears in the sub-threshold region of both partially and fully depleted devices. Below the critical dose, no leakage current is visible on the  $I_D(V_{G1})$  curves at high drain voltage, whereas above the critical dose the transistor is latched. The strong 'leakage' current causes circuit failure. Again, the latch can be effectively suppressed, in partially and fully depleted devices, by (i) lowering the drain voltage, (ii) designing body ties, and (iii) using thinner buried oxides.

#### 4.4. Hardness assurance: worst case bias and irradiation source

The worst-case bias conditions have been described for transistors processed on SIMOX and Unibond wafers.<sup>57,58</sup> Similar conclusions have been reached. Biasing has been studied by systematic measurements and by modeling the total-dose-induced charge trapping in the buried oxide (Fig. 10).<sup>58</sup>

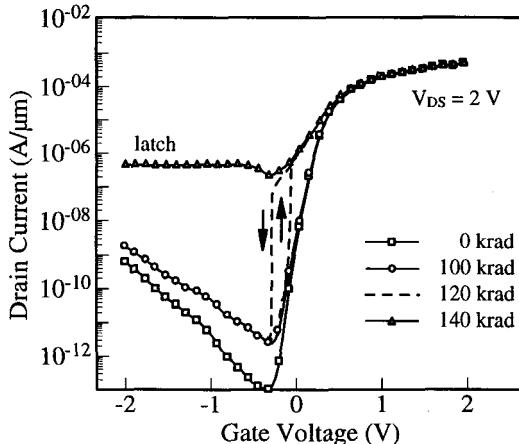


Fig. 9. Onset of a hysteresis on the current-voltage characteristics of a partially depleted SOI MOSFET, during exposure to radiation.<sup>56</sup>

For floating body transistors, the worst case corresponds to the off-state (drain at the supply voltage, other terminals grounded). The distribution of trapped charges in the BOX or at the back interface becomes laterally inhomogeneous. More trapping occurs on the drain side, where the field is larger. This inhomogeneity can be revealed by performing tests in reverse-mode (by exchanging the roles of the source and drain).<sup>59</sup>

For transistors with body ties, the worst case rather corresponds to the "transmission-gate" (TG) state (encountered for example in SRAM cell access transistors), where both the source and drain are biased, while the other terminals are grounded. Additional experiments and simulations have shown the impact of the transistor geometry (gate length, buried oxide thickness) and doping profiles. In very short-channel devices, the fringing fields from drain and source to the body (inset of Fig. 11), modify the potential distribution in the BOX, even leading to a modification of the worst-case configuration.

The radiation source impacts on the total dose response of the SOI transistors. The two main irradiation sources actually used to study the total dose hardness of integrated technologies, Co-60 or 10 keV X-rays, have different signatures. Depending on the bias and the device architecture, a difference by a factor of two can be obtained on the back-gate threshold voltage shift between X-rays and Co-60. The main conclusion drawn by Schwank *et al*<sup>60</sup> is that laboratory X-rays sources more closely simulate a rich proton environment (like on low earth orbits), while Co-60 gamma irradiation provides a better modeling for rich electron environment (high orbits).

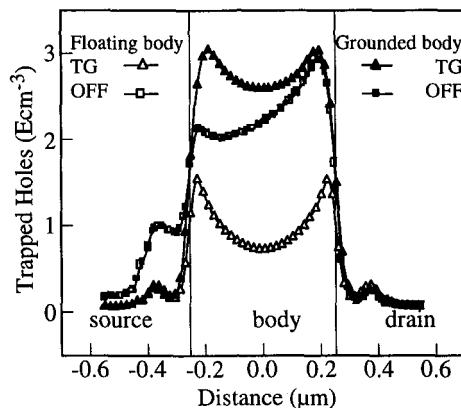


Fig. 10. Simulated distribution of trapped holes in the BOX, 6 nm under the interface. The n-channel MOSFETs are either floating or grounded body, with TG bias or no bias ( $L = 0.5 \mu\text{m}$ , 1 Mrad ( $\text{SiO}_2$ ) dose).<sup>58</sup>

## 5. Future Trends

Several factors impeded the earlier commercial development of SOI circuits: extra cost of SOI wafers, unavailability of dedicated libraries for design and, more importantly, the fabulous progress of bulk-Si technology. There was no real need for an alternative technology such as SOI, before now when the frontiers of Si become imminent. SOI offers two avenues to break the 10-nm gate-length barrier: more or less conventional scaling and new paradigm in device architecture.

### 5.1. Scalability of SOI MOSFETs

The scaling rules for bulk-Si MOSFETs require tremendous doping levels, which adversely affect the carrier mobility, junction capacitances, and circuit speed. Fortunately, the scaling rules and design windows are different for fully-depleted SOI transistors, where additional parameters (film and BOX thickness, substrate doping and biasing) are available for device optimization.

The minimum channel length of SOI MOSFETs, where the short-channel effects are maintained at a tolerable level, is  $L \simeq 3\lambda$ . The ‘intrinsic’ length  $\lambda$ , calculated by solving the Poisson equation, can be dramatically reduced by using ultra-thin Si films.<sup>61</sup> More importantly, below a critical film thickness (15 nm in Fig. 11), the doping becomes irrelevant and the film can be left undoped for the benefit of the carrier mobility.<sup>62,63</sup> However, for light doping, metal gates with selected work function, will be needed to adjust the threshold voltage.

Besides charge sharing and *drain-induced barrier lowering* (DIBL), a serious short-channel effect is the lateral penetration of the electric field into the BOX

and underlying substrate (Fig. 11). This fringing field is responsible for an increase in the potential at the film-BOX interface, via the *drain-induced virtual substrate biasing* (DIVSB). Due to interface coupling, the front-channel threshold voltage is lowered and the subthreshold swing is degraded.

The fringing fields in the BOX can be remarkably attenuated by using thin oxides or low-K insulators. Counter effects of thin BOX are the increase in parasitic capacitances and interface coupling effects. A Ground-Plane (GP), located underneath a relatively thin (50 nm) BOX, has the merit to suppress the field penetration and the depletion region in the substrate.<sup>63</sup>

The ideal architecture of sub-50-nm-long FD MOSFETs will combine very thin films, low doping, moderately thin buried insulators, mid-gap gate, elevated source and drain terminals to reduce series resistances, and perhaps a ground-plane. We can expect that fully depleted, single-gate MOSFETs will reach the limit of 20-nm-long and 5-nm-thick bodies.<sup>5,64</sup>

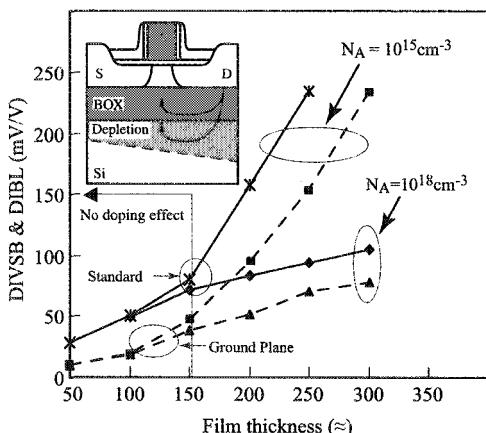


Fig. 11. Threshold voltage roll-off, including standard DIBL and fringing field (DIVSB) effects, versus film thickness for various doping levels and architectures (with and without a ground plane).

## 5.2. Innovative transistors

Double-Gate (DG) SOI MOSFETs are recognized as the final metamorphosis of the MOS transistor. The ideal DG architecture is symmetrical and the two gates are interconnected. A compact variant (GAA: Gate-All-Around) consists of a unique gate that surrounds a ‘suspended’ Si membrane (body of the transistor).<sup>2</sup> DG-MOSFETs were fabricated by Delta process, epitaxial lateral overgrowth, wafer bonding, FinFET process, tunnel epitaxy, SON, and other impressive technologies ... still apart from the mainstream CMOS technology.<sup>3,65,66,67</sup>

The DG concept has initially been demonstrated on conventional fully-depleted SOI MOSFETs by simultaneously biasing the front and back gates with  $V_{G_2} - V_{T_2} = (t_{ox2}/t_{ox1})(V_{G_1} - V_{T_1})$ , such as to compensate for the asymmetry of the two oxides. The formation of front and back inversion channels causes, by continuity, the spreading of minority carriers in the volume of a thin SOI film.<sup>68</sup> This *volume inversion* results in enhanced drain current and transconductance. The total inversion charge in DG-mode is roughly twice the inversion charge in SG-mode and the subthreshold swing is ideal (60 mV/decade at room temperature). The important point is that the minority carriers flow in the middle of the film and experience less surface scattering, hence the mobility,<sup>69,70</sup> radiation hardness,<sup>2,71</sup> and 1/f noise are improved. Measurements in 3-nm-thick transistor reveal an outstanding increase, by more than 200%, in transconductance for DG-mode.<sup>4</sup>

The two gates collaborate to ensure an excellent control of the potential and inversion charge, so that short-channel effects (DIBL, DIVSB, punchthrough) are highly reduced. The channel length can be remarkably shorter in DG, as compared to single gate (SG) transistors: 15–30 nm long DG-MOSFETs have already been demonstrated.<sup>67,72</sup> Numerical simulations including quantum effects, band-to-band tunneling, and direct source-to-drain tunneling indicate excellent characteristics for 2–8 nm DG-MOSFETs.<sup>6</sup> The body thickness should be roughly 1/3 of its length.

A fascinating 4-gate accumulation-mode transistor, G<sup>4</sup>-FET, has recently been demonstrated.<sup>73</sup> Apart from the standard front and back MOS gates, there are two lateral P–N junctions (side gates) which control the effective width of the body. The conductive path is therefore modulated by mixed MOS–JFET effects: from a tiny wire, surrounded by depletion regions, to a strongly accumulated body. Each gate has the capability of switching the transistor on and off which opens new perspectives for mixed-signal applications, quaternary logic schemes, and quantum wire physics. Preliminary measurements have shown that the G<sup>4</sup>-FET can be rather immune to radiation effects.

## 6. Conclusions

SOI is no longer just a technology to alleviate radiation effects in defense or space circuits; SOI devices now operate in a non radiation-free world and they better survive. Knowledge and experience accumulated so far in radiation-hard devices is valuable, however this needs to be updated with fresh information collected in commercial (non rad-hard) devices fabricated with state of the art SOI technology.

Future work will gradually focus on fully depleted SOI MOSFETs—with tunneling gate oxide, ultra-thin Si film and rather thin BOX—which are more talented than partially depleted transistors in the CMOS scaling competition. Exciting opportunities for research are also offered by multiple-gate transistors with two, three or four channels. Finally, the conventional SOI structure is rapidly evolving by absorbing other technologies and materials (strained Si, SiGe or Ge films as well as various dielectrics) with still unknown radiation properties.

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## TOTAL-DOSE AND SINGLE-EVENT EFFECTS IN SILICON-GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS

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We present an overview of radiation effects in silicon-germanium heterojunction bipolar transistors (SiGe HBT). We begin by reviewing SiGe HBTs, and then examine the impact of ionizing radiation on both the *dc* and *ac* performance of SiGe HBTs, the circuit-level impact of radiation-induced changes in the transistors, followed by single-event phenomena in SiGe HBT circuits. While ionizing radiation degrades both the *dc* and *ac* properties of SiGe HBTs, this degradation is remarkably minor, and is far better than that observed in even radiation-hardened conventional Si BJT technologies. This fact is particularly significant given that no intentional radiation hardening is needed to ensure this level of both device-level and circuit-level tolerance (typically multi-Mrad TID). SEU effects are pronounced in SiGe HBT circuits, as expected, but circuit-level mitigation schemes will likely be suitable to ensure adequate tolerance for many orbital missions. SiGe HBT technology thus offers many interesting possibilities for space-borne electronic systems.

**Keywords:** SiGe; silicon-germanium; HBT; heterojunction bipolar transistor; radiation effects; total-dose; single event effects; SEU.

### 1. Introduction

At present, there are two recent but rapidly growing thrusts within the space community: 1) the use of commercial-off-the-shelf (COTS) parts whenever possible for space-borne systems as a cost-saving measure; and 2) the use of system-on-a-chip integration to lower chip counts and system costs, as well as simplify packaging and lower total system launch weight. The "holy-grail" in the realm of space electronics can thus be viewed as a conventional terrestrial IC technology with a system-on-a-chip capability, which is also radiation-hard as fabricated, without requiring any additional process modifications or layout changes. It is within this context that we discuss SiGe HBT technology as potentially such a "radiation-hard-as-fabricated" IC technology with possibly far-ranging implications for the space community.

### 2. The SiGe HBT

While the basic idea of using SiGe alloys to bandgap-engineer Si devices dates to the 1950s, the synthesis of defect-free SiGe films proved surprisingly difficult, and device-quality SiGe films were not successfully produced until the mid-1980s. Because of the difference in lattice constants between Si and Ge, SiGe strained layers are subject to a fundamental stability criterion limiting their thickness for a given Ge concentration. Introducing Ge into Si has a number of consequences for devices. First and most important, because Ge has a larger lattice constant than Si, the energy bandgap of Ge is smaller than that of Si (0.66 eV vs 1.12 eV), and thus SiGe will have a bandgap smaller than that of Si, making it a suitable candidate for bandgap engineering in Si. The compressive strain associated with SiGe alloys produces an additional bandgap shrinkage, and the net result is a bandgap reduction of approximately 75 meV for each 10% of Ge introduced. This Ge-induced "band offset" occurs predominantly in the valence band, making it conducive for use in tailoring *n*p*n* bipolar transistors. Because a

practical SiGe film must be very thin if it is to remain stable and hence defect free, it is a natural candidate for use in the base region of a bipolar transistor (which by definition must be thin to achieve high-frequency operation). The SiGe HBT represents the first practical bandgap-engineered transistor in the Si material system.<sup>1</sup>

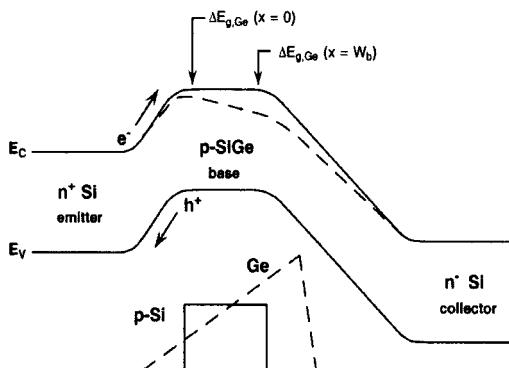


Fig. 1. Energy band diagram for a Si BJT and graded-base SiGe HBT, biased in forward active mode.

To intuitively understand how these band edge changes affect the operation of the SiGe HBT, first consider the band diagram of the device (Fig 1.). The introduction of Ge into the base region has two tangible *dc* consequences: 1) the potential barrier to injection of electrons from emitter into the base is decreased. Intuitively, this will yield exponentially more electron injection for the same applied  $V_{BE}$ , translating into higher collector current and hence higher current gain, provided the base current remains unchanged. Given that band edge effects generally couple strongly to transistor properties, we naively expect a strong dependence of  $J_C$  on Ge content. Of practical consequence, the introduction of Ge effectively decouples the base doping from the current gain, thereby providing device designers with much greater flexibility than in Si BJT design. If, for instance, the intended circuit application does not require high current gain, we can effectively trade the higher gain induced by the Ge band offset for a higher base doping level, leading to lower net base resistance, and hence better dynamic switching and noise characteristics. 2) The presence of a finite Ge content in the CB junction will positively influence the output conductance of the transistor, yielding higher Early voltage, even at constant base doping.

The introduction of Ge into the base region also has important consequences for *ac* device operation, since the Ge-gradient-induced drift field across the neutral base is aligned in a direction (from collector to emitter) such that it will accelerate the injected minority electrons across the base. We are thus able to add a large drift field component to the electron transport, effectively speeding up the diffusive transport of the minority carriers and thereby decreasing the base transit time. Even though the band offsets in SiGe HBTs are typically small by III-V technology standards, the Ge grading over the short distance of the neutral base can translate into large electric fields. For instance, a linearly graded Ge profile with a modest peak Ge content of 10%, graded over a 50-nm neutral base width, yields  $75 \text{ mV} / 50 \text{ nm} = 15 \text{ kV/cm}$  electric field, sufficient to accelerate the electrons to near saturation velocity. Because the base transit time typically

limits the frequency response of a Si BJT, we would expect that the frequency response should be significantly improved by introducing this Ge-induced drift field.

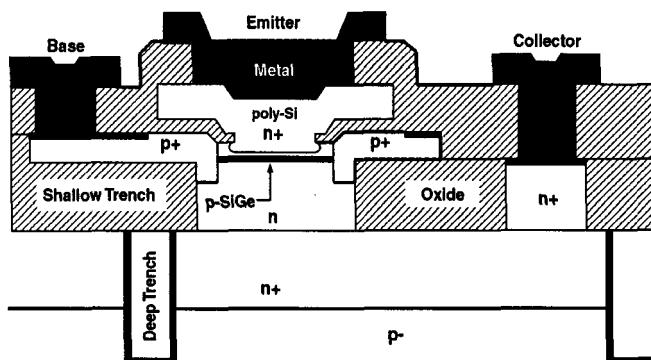


Fig. 2. Schematic cross-section of a representative first generation SiGe HBT, drawn through first metal.

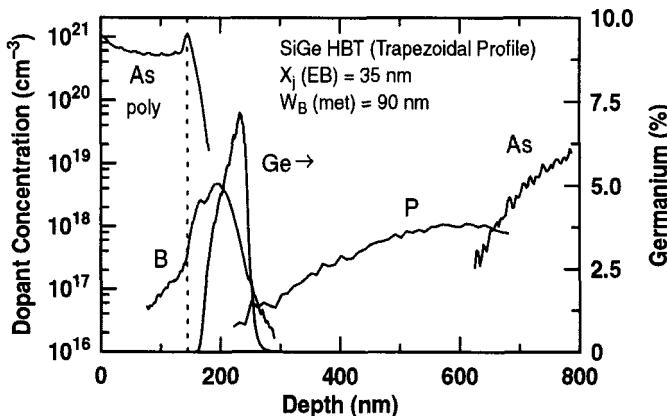


Fig. 3. Measured SIMS doping profile of a first generation SiGe HBT.

Perhaps most importantly, SiGe HBTs can be quite easily teamed with best-of-breed Si CMOS to form a monolithic SiGe HBT BiCMOS technology. While this might seem at first glance to be a mundane advantage, it is in fact a fundamental enabler for SiGe's long-term success, provided SiGe HBTs can be realized without an excessive cost penalty compared to standard Si ICs. The integration of SiGe HBTs with Si CMOS is also the fundamental departure point between SiGe technology and III-V technologies. If SiGe technology is to be successful in the long haul, it must bring to the table the RF and analog performance advantages of the SiGe HBT, and the low-power logic, integration level, and memory density of Si CMOS, into a single cost-effective IC that enables SoC integration (i.e., SiGe HBT BiCMOS). Typically, SiGe HBTs (often with multiple breakdown voltages) exist as an "adder" to a basic CMOS IC building-block core, to be swapped in or out as the application demands, without excessive cost burden. Typical state-of-the-art SiGe HBT BiCMOS technologies generally have a roughly 20% adder in mask count compared to generic digital CMOS, and are viewed by many as an acceptable

compromise between performance benefit and cost, depending on the application. Fig. 2 and Fig. 3 show a schematic cross-section and doping profile of a first generation SiGe HBT.

### 3. Radiation Response of SiGe HBTs

The typical response of a SiGe HBT to irradiation can be seen in Fig. 4, which shows typical measured Gummel characteristics of a SiGe HBT, both before and after exposure to protons.<sup>2-6</sup> As expected, the base current increases after a sufficiently high proton fluence due to the production of G/R trapping centers, and hence the current gain of the device degrades. There are two main physical origins of this degradation. The base current density is inversely proportional to the minority carrier lifetime in the emitter, so that a degradation of the hole lifetime will induce an increase in the base current. In addition, ionization damage due to the charged nature of the proton fluence produces interface states and oxide trapped charges in the spacer layer at the emitter-base junction. These G/R centers also degrade  $I_B$ , particularly if they are placed inside the EB space charge region, where they will yield an additional non-ideal base current component (non- $kT/q$  exponential voltage dependence). By analyzing a variety of device geometries, it can be shown that the radiation-induced excess base current is primarily associated with the EB spacer oxide at the periphery of the transistor, as naively expected, and is hence the radiation response is dominated by ionization damage rather than displacement damage.<sup>1</sup> The degradation of the current gain as a function of collector current for the pre-irradiated sample, and after exposure to three proton fluences, is shown in Fig. 5. For fluences up to  $1 \times 10^{13} \text{ p/cm}^2$  the peak current gain at  $10 \mu\text{A}$  does not show a visible degradation, and at  $1 \times 10^{14} \text{ p/cm}^2$ , a degradation of only about 8% compared to the pre-irradiated device is observed. This suggests that these SiGe HBTs are robust to TID for typical orbital proton fluences for realistic circuit operating currents above roughly  $100 \mu\text{A}$  without any additional radiation hardening. These results are significantly better than for conventional diffused or even ion-implanted Si BJT technologies (even radiation-hardened ones).

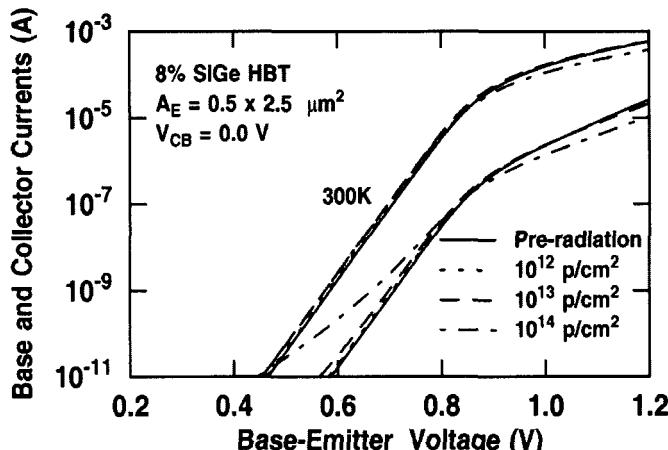


Fig. 4. Measured current-voltage characteristics of a SiGe HBT before and after proton exposure.

Of particular interest is the inference of the spatial location of the proton-induced traps in these devices.<sup>4</sup> The existence of proton-induced traps in the EB space charge region is clearly demonstrated by the G/R-induced increase in the non-ideal base current component shown in the Gummel characteristics. The existence of radiation-induced traps in the collector-base space charge region was verified by measuring the inverse mode Gummel characteristics of the device (emitter and collector leads swapped). In this case the radiation-induced traps in the CB junction now act as G/R centers in the inverse EB junction, with a signature non-kT/q exponential slope. 2-D simulations were calibrated to both measured data for the pre- and post-irradiated devices at a collector-base voltage of 0.0 V. In order to obtain quantitative agreement between the simulated and measured irradiated results, traps must be located uniformly throughout the device, and additional interface traps must be located around the emitter-base spacer oxide edge. Most of the radiation-induced recombination occurs inside the EB space charge region, leading to a non-ideal base current, as expected.

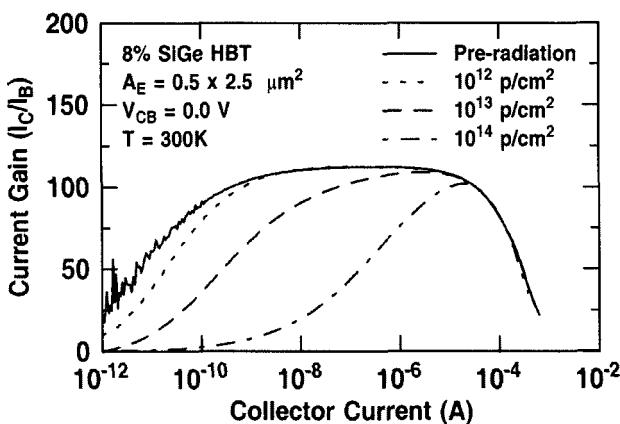


Fig. 5. Measured current gain versus bias current of a SiGe HBT as a function of proton fluence.

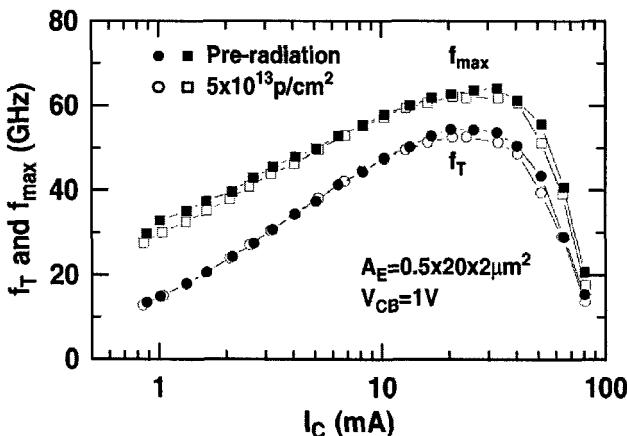


Fig. 6. Measured cutoff frequency versus bias current of a SiGe HBT after proton irradiation.

To assess the impact of radiation on the *ac* performance of the transistors, the S-parameters were measured to 40 GHz both before and after proton exposure.<sup>7</sup> From the measured S-parameters, the transistor cutoff frequency and maximum oscillation frequency were extracted (Fig. 6). Only a slight degradation in  $f_T$  and  $f_{max}$  is observed, the latter being expected from the minor increase of the base resistance with irradiation, due to either carrier removal, mobility / lifetime changes, or both. The broadband noise performance of SiGe HBTs is critical for space-borne transceivers and communications platforms. As shown in Fig. 7 the minimum noise figure ( $NF_{min}$ ) degrades only slightly at 2.0 GHz after an extreme proton fluence of  $5 \times 10^{13} \text{ p/cm}^2$  (from 0.95 dB to a still-excellent value of 1.07 dB, a 12.6% degradation).

We note that careful comparisons between identically fabricated SiGe HBTs and Si BJTs (same device geometry and wafer lot, but without Ge in the base for the epitaxial-base Si BJT), show that the extreme level of total dose tolerance of SiGe HBTs is not *per se* due to the presence of Ge.<sup>4</sup> That is, the proton response of both the epitaxial base SiGe HBT and Si BJT are nearly identical. We thus attribute the observed radiation hardness to the unique and inherent structural features of the device itself, which from a radiation standpoint can be divided into three major aspects: 1) in these epitaxial base structures, the extrinsic base region is very heavily doped ( $> 5 \times 10^{19} \text{ cm}^{-3}$ ) and located immediately below the EB spacer oxide region, effectively confining any radiation-induced damage, and its effects on the EB junction; 2) the EB spacer, known to be the most vulnerable damage point in conventional BJT technologies, is thin ( $< 0.20 \mu\text{m}$  wide) and composed of an oxide/nitride composite, the latter of which is known to produce an increased level of radiation immunity; 3) the active volume of these transistors is very small ( $W_E = 0.5 \mu\text{m}$ , and  $W_b < 150 \text{ nm}$ ), and the emitter, base, and collector doping profiles are quite heavily doped, effectively lessening the impact of displacement damage. We also note that these SiGe HBTs compare very favorably in both performance and radiation hardness with (more expensive) GaAs HBT technologies that are often employed in space applications requiring both very high speed and an extreme level of radiation immunity.<sup>8</sup>

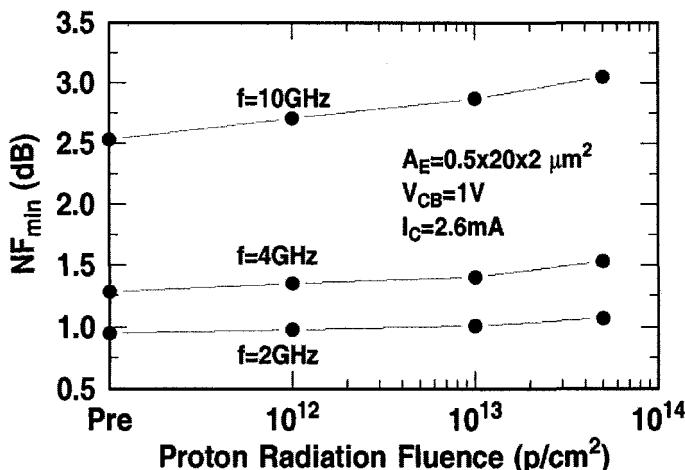


Fig. 7. Measured broadband noise performance of a SiGe HBT as a function of proton fluence.

Within the past few years, a pronounced low-dose-rate sensitivity to gamma irradiation that is not screened by the current test methods for ionizing radiation has been observed in Si bipolar technologies. The enhancement in device and circuit degradation at low gamma dose rates has come to be known as "Enhanced Low Dose Rate Sensitivity" (ELDRS).<sup>9-10</sup> The ELDRS effect was first reported in 1991, which demonstrated that existing radiation hardness test assurance methodologies were not appropriately considering worst case conditions. The physical origins underlying ELDRS have been hotly debated for years, and numerous mechanisms proposed. Recent attempts to understand ELDRS include a model suggesting that the lower net radiation induced trapped charge density at high-dose-rates is a result of a space charge phenomenon, caused by delocalized hole traps which occur in heavily damaged oxides such as bipolar base oxides. These traps can retain holes on a timescale of seconds to minutes, causing a buildup of positive charge in the oxide bulk during high-dose-rate irradiation. This is in contrast to low-dose-rate irradiation, where the irradiation time is much longer, effectively allowing the holes in the trap centers to be detrapped. Thus, in the high-dose-rate case, the larger total trapped hole density forces holes near the interface to be trapped closer to the interface, where they can be compensated by electrons from the silicon. This lowers the resultant net trapped charge density.<sup>11</sup>

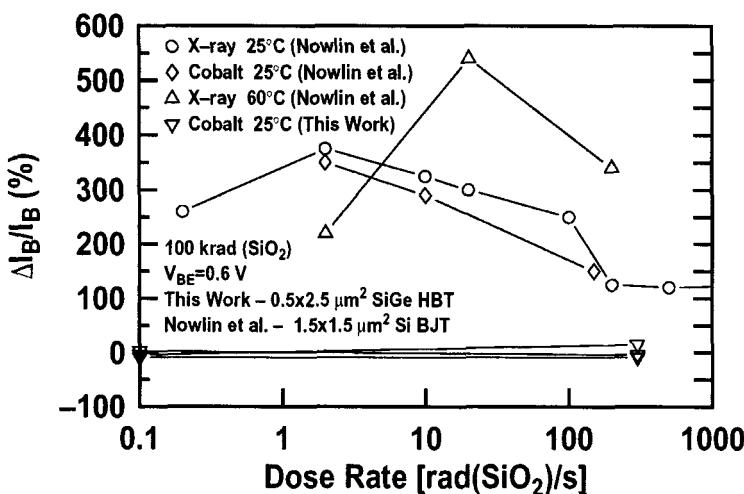


Fig. 8. Low dose gamma data comparing SiGe HBT ELDRS response with other Si BJT technologies.

To assess ELDRS in SiGe technology, low-dose-rate (0.1 rad(Si/sec) and high-dose-rate (300 rad(Si/sec) experiments were conducted using Cobalt-60.<sup>12</sup> As can be seen in Fig. 8, low-dose-rate effects in these SiGe HBTs were found to be nearly nonexistent, in striking contrast to reports of strong ELDRS in conventional Si bipolar technologies. We attribute this observed hardness to ELDRS to the same mechanisms responsible for the overall radiation hardness of the technology, and is likely more structural in nature than due to any unique advantage afforded by the SiGe base. Interestingly, an anomalous decrease in base current was also found in these devices at low-dose-rates, suggesting that a new physical phenomenon is present at low-dose-rates in these devices.

#### 4. SiGe HBT Circuit Tolerance

For the successful deployment of SiGe technology into space-based systems, circuit-level radiation hardness is clearly more important than device-level hardness. As presented above, the TID device degradation is minor in the bias range of interest to most actual circuits (typically  $I_C > 100 \mu\text{A}$ ). In order to assess the impact of radiation exposure on actual SiGe HBT circuits, we have compared two very important, yet very different circuit types, one heavily used in analog ICs (the bandgap reference circuit), and one heavily used in RFICs (the voltage controlled oscillator).<sup>13-14</sup> Each circuit represents a key building block for realistic SiGe ICs that might be flown in space. Each of these SiGe HBT circuits was designed using fully calibrated SPICE models, layed-out, and then fabricated on the same wafer to facilitate unambiguous comparisons. In addition, because any realistic RF IC must also necessarily include passive elements such as monolithic inductors and capacitors, we have also investigated the effects of proton exposure on an RF LC bandpass filter. As can be seen from the data (Table 1), the impact of even extreme proton fluences has minimal effect on either the output voltage or temperature sensitivity of BGRs, the phase noise or tuning range of VCO's or passive elements, and is indicative of the overall robustness of this SiGe technology for analog and RF circuit applications.

Table 1. Comparison of SiGe HBT Circuit Performance Before and After Proton Exposure.

SiGe HBT Circuit	Parameters	Pre-radiation	After $5 \times 10^{13} \text{ p/cm}^2$	Units
Bandgap Reference	$V_{cc}$	3.0	3.0	V
	$I_{cc}$	0.773	0.767	mA
	$V_{out}$ at 300K	1.37416	1.372096	V
	Stability (-55 to 85°C)	81.2	81.7	ppm/°C
Voltage Controlled Oscillator	Frequency	5.0	5.0	GHz
	$V_{cc}$	3.3	3.3	V
	$I_{cc}$	22.5	22.5	mA
	Output Power	-5.0	-5.5	dBm
	Phase Noise	-112.5	-111.8	dBc/Hz
	Tuning Range	4,595-5,452	4,623-5,470	MHz
LC Bandpass Filter	Frequency	1.9	1.9	GHz
	Filter Q (@ 3dB BW)	7.6	7.6	-
	Insertion Loss	16.8	16.8	dB
	L	2.5	2.5	nH
	Inductor Q	7.4	7.4	-
	C	6.0	6.0	pF
	Capacitor Q	58	58	-

#### 5. Single Event Effects in SiGe HBTs

Clearly, a space-qualified IC technology must demonstrate sufficient SEU immunity to support high-speed circuit applications as well as possess TID tolerance. It is well known that even III-V technologies that have significant TID tolerance often suffer from poor SEU immunity, particularly at high data rates. Recently, high-speed SiGe HBT digital logic circuits were found to be vulnerable to SEU at even low LET values.<sup>15-16</sup> In addition, successfully employed III-V HBT circuit-level hardening schemes using the current-sharing hardening (CSH) technique were found to be ineffective for these SiGe HBT logic circuits (Fig. 9). To understand single event effects in SiGe HBTs, one must

use calibrated 2-D/3-D device simulation to assess the charge collection characteristics of SiGe HBTs. These device-level simulation results can then be coupled to circuit-level modeling to better understand circuit-level mitigation approaches.

From a device perspective, it is important to first assess the transistor charge collection characteristics as a function of terminal bias, load condition, substrate doping, and ion strike depth.<sup>17-18</sup> Bias and loading conditions were chosen to mimic representative circuit conditions within an actual ECL/CML digital circuit. Fig. 10 shows the charge collected by the collector versus time for different RC loads. The base and emitter terminals were grounded, the substrate bias was -5.2 V, the collector was connected to ground through an RC load, and the substrate doping was  $5 \times 10^{15} \text{ cm}^{-3}$ . A uniform LET of 0.1 pC/ $\mu\text{m}$  (equivalent to 10 MeV $\cdot\text{cm}^2/\text{mg}$ ) over 10  $\mu\text{m}$  depth was used, which generates a total charge of 1.0 pC. The results clearly show that charge collection is highly dependent on the transistor load condition (i.e., circuit topology). As the load resistance increases, the collector-collected charge decreases. Note, however, that the emitter-collected charge increases correspondingly. The underlying physics is that more electrons exit through the emitter, instead of the collector. A larger load resistance presents a higher impedance to the electrons at the collector, and thus more electrons exit through the emitter. The collector of the adjacent device only collects a negligible amount of charge, despite the transient current spikes of the strike. Nearly all of the electrons deposited are collected by the collector and the emitter, although the partition between emitter and collector collection varies with the load condition. The impact on the SiGe base layer on the charge collection properties is a secondary effect.

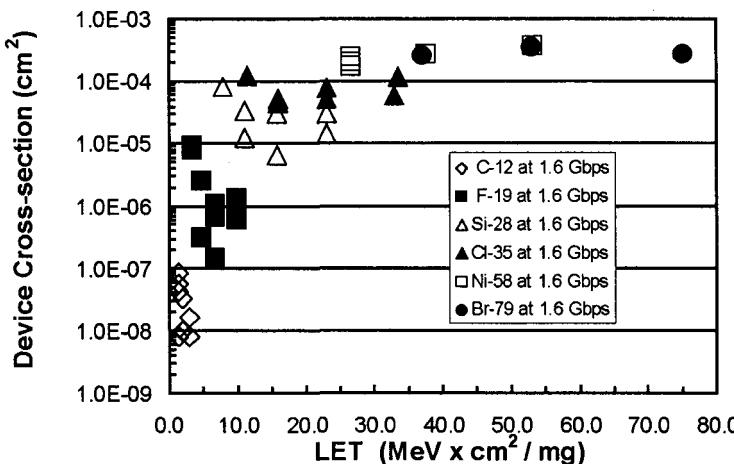


Fig. 9. Measured single event upset tolerance for first generation SiGe HBT digital circuits.

To better understand circuit-level SEU response, we combined these simulated charge-time profiles with circuit-level modeling in three different SiGe circuit architectures.<sup>19</sup> Circuit A is a straightforward ECL implementation of the standard rising edge-triggered flip-flop logic. Circuit B is the unhardened version of the D flip-flop used in the shift register results shown in Fig. 10. Circuit B uses fewer transistors and thus less power than circuit A, and is also faster than circuit A, allowing operation at higher clock rates. Because of these advantages, circuit B is very popular in high-speed bipolar digital circuit design. The circuit consists of a master stage and a slave stage. The master stage

consists of a pass cell, a storage cell, a clocking stage, and a biasing control. The slave stage has a similar circuit configuration. Circuit C is the current-sharing hardened version of circuit B. (Refer to reference<sup>1</sup> for circuit level schematics for A, B, and C.) The circuit was used as a basic building block of the 32-stage shift-register data shown in Fig. 9. In this case, the current source transistor is divided into 5 paths, and these paths are maintained separately through the clocking stage and through the pass and storage cells. In essence, the input and output nodes of five copies of the switching circuits, including the controlling switch, clock, master and storage cells, are connected in parallel. The load resistance is shared by all the current paths.

The quasi-3D simulated SEU-induced transient currents were activated on one of the sensitive transistors in the respective circuits. The SEU currents were activated at 5.46 nsec (within the circuit hold time), immediately after the clock goes from low to high, a sensitive time instant for SEU-induced transient currents to produce an upset at the output. The input data is an alternating "0" and "1" series with a data rate of 2 Gbit/sec. Under these conditions, circuit A shows no upset at all, while circuits B and C show 5 and 3 continuous bits of data upset, respectively (Fig. 11). These results suggest that circuit A has the best SEU tolerance, while circuit C, the CSH hardened version, has better SEU tolerance than its unhardened companion version, circuit B. Circuit A, which shows no data upset at a switching current of 1.5 mA, does in fact show an upset when the switching current is lowered to 0.6 mA. This is consistent with our earlier observation that increasing switching current is effective in improving SEU performance for circuit C.

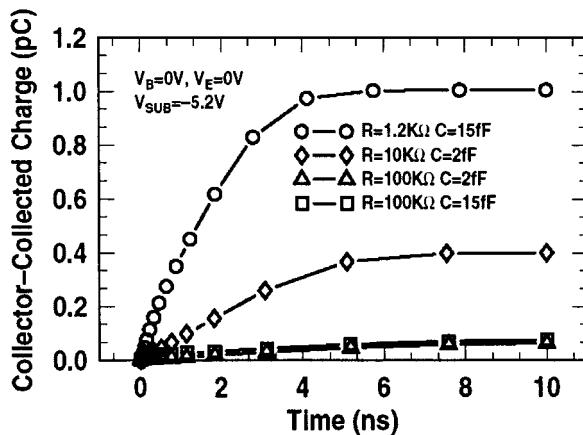


Fig. 10. Simulated charge collection characteristics of a SiGe HBT.

The fundamental reason for the observed better SEU tolerance of circuit A than for circuits B and C is that only one of the two outputs of the emitter-coupled pair being hit is affected by the ion-strike SEU current transients. As long as the differential output is above the logic switching threshold, the output remains unaffected, and no upset occurs. The collector voltage of the switching transistor decreases upon ion strike (compared to without SEU), however, and no upset is observed at the output, simply because the differential output remains above or below the relevant switching threshold (Fig. 12). These results suggest that circuit-level mitigation techniques can be used in SEU hardening of SiGe HBT logic, albeit at some level of additional power dissipation and circuit complexity.

## 6. Summary

While ionizing radiation degrades both the *dc* and *ac* performance of SiGe HBTs, this degradation is remarkably minor, even for extreme levels of radiation exposure, and is far better than that observed in even radiation-hardened conventional Si BJT technologies. This fact is particularly significant given that no intentional radiation hardening is needed to ensure this level of both device-level and circuit-level tolerance (typically multi-Mrad TID). SEU effects are pronounced in SiGe HBT circuits, as expected, but circuit-level mitigation schemes will likely be suitable to ensure adequate tolerance for many orbital missions. SiGe HBT technology thus offers many interesting possibilities for space-borne electronic systems.

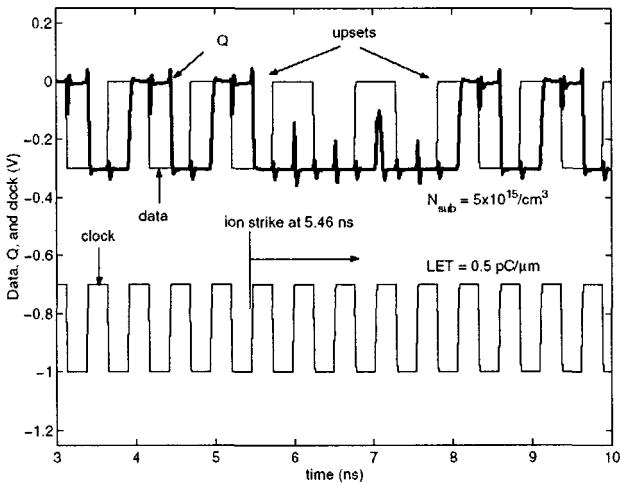


Fig. 11. Simulated SEU response of a SiGe HBT using circuit B architecture, showing upsets.

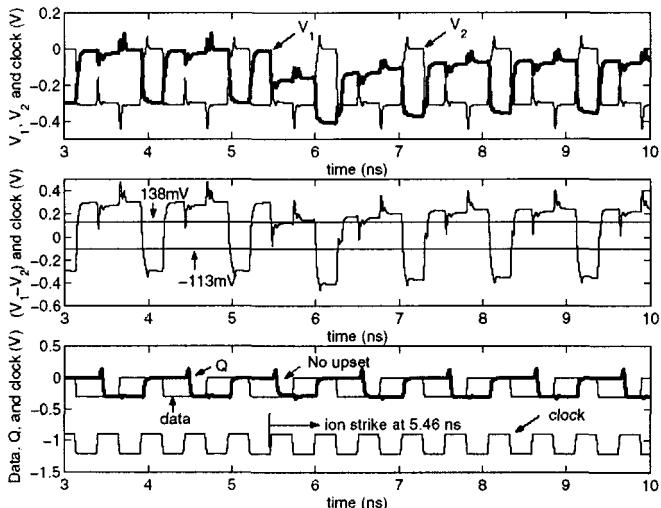


Fig. 12. Simulated node voltages of circuit A under after an ion strike.

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## GAIN DEGRADATION AND ENHANCED LOW-DOSE-RATE SENSITIVITY IN BIPOLAR JUNCTION TRANSISTORS

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The current gain of irradiated bipolar junction transistors decreases due to increased recombination current in the emitter-base depletion region and the neutral base. This recombination current depends on the interaction of two factors: (1) decreased minority-carrier lifetime at the Si/SiO<sub>2</sub> interface or in the bulk Si and (2) changes in surface potential caused by charge in the oxide. In *npn* transistors, these two factors both result in increased base current, while in *pnp* devices, positive charge in the oxide moderates the increase in base current due to surface recombination. In some technologies, the amount of degradation that occurs at a given total dose increases as the dose rate decreases. This enhanced low-dose-rate sensitivity results from space-charge effects produced by slowly transporting holes and protons in the oxide that covers the emitter-base junction.

*Keywords:* Gain degradation, excess base current, total dose, bipolar transistors.

### 1. Introduction

Bipolar junction transistors (BJTs) have important applications in which they may be exposed to radiation, including space systems, defense systems, and high-energy particle accelerators. The principle effect of total ionizing dose and displacement damage on bipolar transistors is an increase in the number of defects that participate in Shockley-Read-Hall recombination (either at the Si/SiO<sub>2</sub> interface or in the Si bulk), resulting in increased base current and decreased current gain.<sup>1, 2</sup> In addition to gain degradation, bipolar integrated circuits also may suffer from device-to-device or collector-to-emitter leakage current caused by radiation-induced inversion under isolation oxides.<sup>3-7</sup> In circuits in which the absolute value of the current gain is not important as long as it exceeds some minimum value, radiation-induced leakage current may be the dominant failure mechanism. In this paper, the mechanisms responsible for gain degradation are described. In addition, possible explanations of the Enhanced Low-Dose-Rate Sensitivity (ELDRS) of gain degradation that is observed in many bipolar technologies are explored.

Bipolar and BiCMOS technologies are particularly important for analog, radio-frequency (RF), and mixed-signal integrated circuits. Much of the recent work on BJTs has focused on development of high-speed transistors ( $f_T > 50$  GHz) for RF integrated circuits. In particular, BJTs based on silicon-germanium (SiGe) and gallium arsenide (GaAs) technologies show much promise for use in the fast-growing wireless communications market.<sup>8</sup> However, much of the market for BJTs remains in the traditional silicon-based analog integrated circuit area.

Bipolar transistors have advantages over MOSFETs in the areas of speed,<sup>9</sup> linearity, transconductance,<sup>10</sup> and current drive.

Bipolar and MOS (metal oxide semiconductor) technologies each have important roles in the microelectronics industry. For digital integrated circuits, MOS technology is favored because of its high packing density, low power dissipation, and flexible logic. The most frequently used bipolar analog integrated circuits include operational amplifiers, voltage regulators, phase-locked loops, analog-to-digital converters (ADCs), and digital-to-analog converters (DACs).<sup>11</sup>

BiCMOS integrated circuits combine bipolar and MOS transistors on a single substrate. In principle, each device type can be used for the applications at which it excels. In the case of bipolar transistors, the most desirable features are switching speed, current drive per unit area, noise performance, analog capability, and I/O speed.<sup>12</sup> In contrast, CMOS (complementary MOS) offers better power dissipation, noise margins, packing density, and digital-circuit complexity.<sup>12</sup> The bipolar and MOS transistors in BiCMOS technologies are both affected by radiation and thus the unique radiation-induced degradation characteristics of both device types (gain degradation, leakage currents, threshold-voltage shifts, surface-mobility degradation, breakdown-voltage changes, etc.) must be considered. However, BiCMOS technologies exhibiting very high levels of radiation tolerance have been developed.<sup>13, 14</sup>

## 2. Device Structures

### 2.1. Conventional *npn* BJTs

A cross-sectional view of a traditional *npn* BJT is shown in Figure 1. The dashed line in this figure indicates the portion of the device that is most sensitive to ionizing radiation. This example illustrates a junction-isolated device, although recessed oxides and trenches are often used in modern technologies.

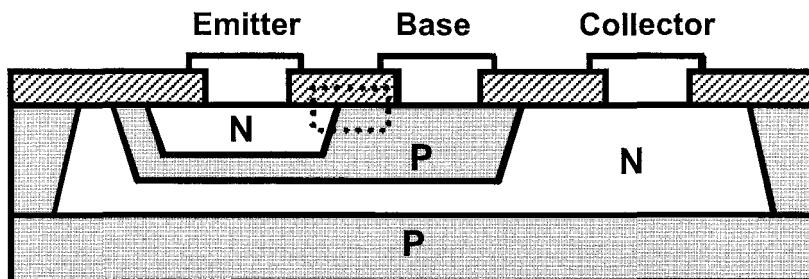


Figure 1 Cross-sectional view of a conventional *npn* BJT. The dashed line indicates the portion of the device that is most sensitive to ionizing radiation.

Polysilicon-emitter *npn* BJTs have significant advantages over crystalline-emitter devices,<sup>15, 16</sup> including smaller device size, reduced parasitics, and high current gain. Transistors with  $f_t = 30$  GHz and no special hardening techniques maintained good performance to a total dose of 100 krad or a neutron fluence of  $5 \times 10^{13} \text{ cm}^{-2}$ .<sup>17</sup>

### 2.2. Vertical, lateral, and substrate *pnp* BJTs

There are three basic types of *pnp* bipolar transistors that are used in integrated circuits. Vertical PNP transistors are similar in structure to vertical *npn* devices. Lateral *pnp* (LPNP)

transistors have the active region of the device at the silicon surface and the current flows laterally between emitter and collector regions that are both at the surface. Substrate *pnp* devices have a vertical current-flow pattern, but the substrate serves as the collector for the device. Figure 2 shows qualitative cross sections of lateral and substrate *pnp* transistors. The lightly-doped *n*-type base can be quite sensitive to radiation, particularly at the oxide interface.

Vertical *pnp* transistors are usually relatively radiation-hard compared to vertical *npn* devices.<sup>18, 19</sup> In contrast, lateral and substrate *pnp* transistors tend to be relatively soft.<sup>20-22</sup> The total dose required to degrade lateral devices to half of their normalized current gain may be as much as 50 times less than that needed to observe current gain degradation of the same extent in vertical devices.<sup>23</sup>

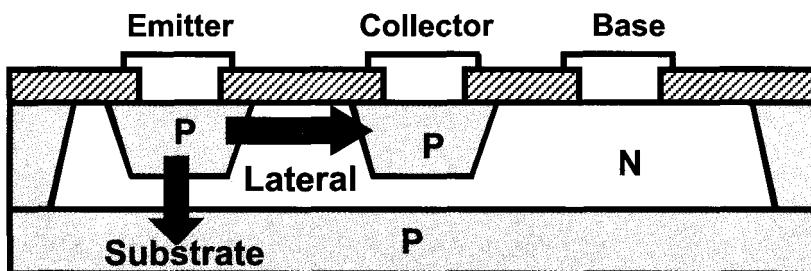


Figure 2 Representative cross-sections of lateral and substrate *pnp* transistors. The arrows indicate the current-flow paths for each type of device. The lightly-doped *n*-type base can be quite sensitive to radiation, particularly at the oxide interface.

### 3. Transistor-Level Degradation

#### 3.1. Current components

The collector current in an *npn* BJT operating in the forward-active region consists of electrons that are injected from the forward-biased emitter-base junction, diffuse across the neutral base, and are swept through the collector depletion region by the electric field. If all of the electrons injected into the base reach the collector, the collector current density is equal to the diffusion current of electrons in the neutral base:

$$J_C = \frac{qD_{nB}n_{B0}}{W_B} \exp\left(\frac{qV_{BE}}{kT}\right), \quad (1)$$

where  $J_C$  is the collector current density,  $D_{nB}$  is the electron diffusivity in the base,  $n_{B0}$  is the equilibrium electron concentration in the base,  $W_B$  is the neutral base width,  $V_{BE}$  is the base-emitter voltage, and  $kT/q$  is the thermal voltage.

The main components of base current in an *npn* BJT are back-injection of holes from the base to the emitter ( $J_{B1}$ ), recombination in the emitter-base depletion region ( $J_{B2}$ ), and recombination in the neutral base ( $J_{B3}$ ). In most situations, the back-injection component of the base current dominates. However, for devices that have been exposed to ionizing radiation, both  $J_{B2}$  and  $J_{B3}$  increase, with  $J_{B2}$  normally dominating. When the degradation is dominated by displacement damage,  $J_{B2}$  and  $J_{B3}$  both may increase significantly. The back-injected hole-current density from the base to the emitter,  $J_{B1}$ , is a diffusion current:

$$J_{B1} = \frac{qD_{pE}p_{E0}}{L_{pE}} \exp\left(\frac{qV_{BE}}{kT}\right), \quad (2)$$

where  $D_{pe}$  is the hole diffusivity in the emitter,  $p_{E0}$  is the equilibrium hole concentration in the emitter, and  $L_{pE}$  is the diffusion length for holes in the emitter. This assumes that the back-injected hole concentration decays exponentially with distance from the edge of the emitter-base depletion region. Analogous equations describe the operation of *pnp* transistors, with the roles of holes and electrons interchanged.

### 3.2. Recombination in the emitter-base depletion region

The primary effect of ionizing radiation-induced oxide trapped charge and interface traps is usually an increase in the base current resulting from enhanced recombination in the emitter-base depletion region. The amount by which the base current increases above its pre-irradiation value is called the excess base current (defined as  $\Delta I_B = I_B - I_{B0}$ , where  $I_{B0}$  is the pre-irradiation base current). The recombination-rate increase occurs mainly where the depletion region intersects the Si/SiO<sub>2</sub> interface, due to formation of interface traps that serve as recombination centers (the surface recombination velocity increases with the interface-trap density). When a BJT is exposed to energetic particles, displacement damage occurs in the bulk Si. The resulting defects reduce the minority-carrier lifetime.

The recombination rate is a function of position within the depletion region, exhibiting a strong peak where  $n = p$ . The ideality factor (defined as  $n_B$  in  $\exp(qV/n_B kT)$ ) is 2 for recombination occurring at this peak and 1 for the ideal component of the base current. However, the recombination rate must be integrated throughout the depletion region to obtain the contribution of recombination to the base current. The excess base current due to surface recombination thus has an ideality factor between 1 and 2, which combines the effects of the different spatial locations at which the recombination takes place. However, it is a reasonable approximation in many cases to assume that the radiation-induced excess base current is dominated by the peak recombination rate, which leads to the results.<sup>2</sup>

$$J_{B2,surf} \propto v_{surf} \exp\left(\frac{qV}{2kT}\right) \quad (3)$$

and

$$J_{B2,bulk} \propto \frac{1}{\tau_d} \exp\left(\frac{qV}{2kT}\right), \quad (4)$$

where  $J_{B2,surf}$  and  $J_{B2,bulk}$  are the base current densities due to recombination in the depletion region where it intersects the Si/SiO<sub>2</sub> interface and in the depletion region in the bulk silicon, respectively,  $v_{surf}$  is the surface recombination velocity, and  $\tau_d$  is the minority-carrier lifetime in the depletion region. Since the base current due to recombination in the depletion region increases more slowly with voltage than the back-injected ( $J_{B1}$ ) component of the base current, its effect is greatest at low emitter-base voltages.

### 3.3. Recombination in the neutral base

When minority carriers are injected from the emitter into the neutral base, some of them recombine before they reach the collector junction. This neutral-base recombination may take place in either the bulk Si or at the Si/SiO<sub>2</sub> interface (if the Si surface is neutral, as determined by the charge in the oxide or the bias on any electrodes lying over the base region). The fraction of carriers that recombine is small in most unirradiated devices, but it may become sig-

nificant following irradiation. In a BJT operating in the forward-active region, the distribution of minority carriers in the neutral base is approximately triangular and the total amount of minority-carrier charge (electrons, in this case) stored in the base is:

$$Q_B = \frac{1}{2} q W_B n_B(0) = \frac{q W_B n_{B0} \exp\left(\frac{qV_{BE}}{kT}\right)}{2}. \quad (5)$$

If the average lifetime of minority carriers in the neutral base is  $\tau_B$ , the base current density required to supply the recombination process is:

$$J_{B3} = \frac{Q_B}{\tau_B} = \frac{q W_B n_{B0} \exp\left(\frac{qV_{BE}}{kT}\right)}{2\tau_B}. \quad (6)$$

Unlike recombination in the emitter-base depletion region, which exhibits an ideality factor close to 2, the ideality factor associated with recombination in the neutral base is 1. When the device is irradiated, this component of the current increases since the lifetime in the base decreases. For ionizing radiation, the surface lifetime decreases due to interface-trap formation, but the bulk lifetime remains approximately constant. For displacement damage, the bulk lifetime decreases.

### 3.4. Current gain

The common-emitter current gain ( $\beta$ ) is defined as the ratio of the collector current to the base current:

$$\beta = \frac{I_C}{I_B}. \quad (7)$$

In a simple one-dimensional BJT, the peak pre-irradiation current gain can be estimated as the ratio of Eq. (1) to Eq. (2):

$$\beta = \frac{D_{nB} n_{B0} L_{pE}}{D_{pE} D_{E0} W_B} = \frac{D_{nB} N_{DE} L_{pE}}{D_{pE} N_{AB} W_B}, \quad (8)$$

where  $N_{DE}$  is the emitter doping and  $N_{AB}$  is the base doping. This simple estimate of the current gain does not include effects associated with either high or low bias levels. At high bias levels, the current gain is lower than the peak value due to high-level injection effects<sup>24, 25</sup> and the Kirk effect.<sup>26</sup> At low levels, the current gain is lower because of recombination in the emitter-base depletion region. When a BJT is irradiated, the base current increases because of increased recombination in the emitter-base depletion region and the neutral base. However, the collector current typically remains relatively constant, causing the current gain to decrease.<sup>27, 28</sup> An example Gummel plot (log  $I_C$  and  $I_B$  vs.  $V_{BE}$ ) is shown in Figure 3. For this device, the collector current remains virtually unchanged except at very low bias levels, while the base current increases significantly. This causes a large reduction in the current gain, especially at low bias levels where the base current increases most rapidly. The current gain of an irradiated *n*p*n* BJT is plotted vs.  $V_{BE}$  in Figure 4. The actual total dose levels that correspond to a given amount of degradation in a particular device type depend strongly on the technology used to fabricate the device; significant degradation may occur at total doses as low as 10

krad(SiO<sub>2</sub>) in very soft technologies, while other technologies may exhibit relatively little degradation at 1 Mrad(SiO<sub>2</sub>).

Increased recombination in the emitter-base depletion region does not reduce the collector current at a given bias level because the number of carriers injected into the base depends only on the doping of the base and the applied bias. If recombination increases in the depletion region, the emitter and base currents increase, but the collector current remains constant. However, when injected carriers recombine in the neutral base, they do not reach the collector junction and the collector current decreases.

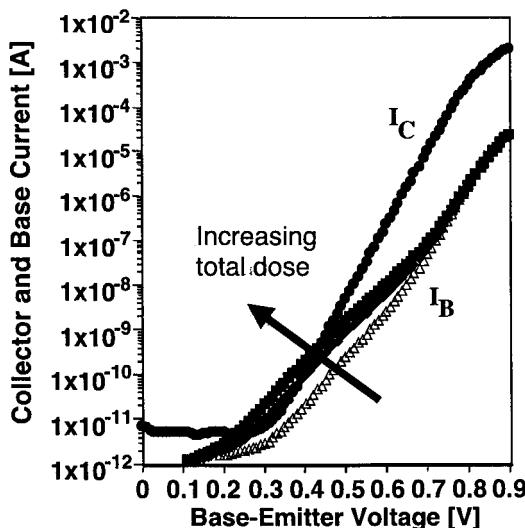


Figure 3 Collector and base current vs. base-emitter voltage for an irradiated *npn* BJT.

Early studies of gain degradation in BJTs focused on displacement damage. In these studies, it was shown that the change in the current gain due to neutron irradiation could be described by:<sup>29-31</sup>

$$\frac{1}{\beta} = \frac{1}{\beta_0} + \frac{K_1 \Phi_n}{2\pi f_T} \quad (9)$$

where  $K_1$  is a constant of proportionality and  $\Phi_n$  is the neutron fluence. This equation is equivalent to saying that the base current is inversely proportional to the minority-carrier lifetime in the emitter-base depletion region or the neutral base. The same type of relationship holds for displacement damage introduced by other particles, including heavy ions, protons, and electrons.<sup>32</sup>

In space systems, high-energy protons constitute a large part of the radiation to which devices are subjected. In addition to ionizing-dose effects, protons also cause displacement damage. The device-level effects due to these two types of damage are not simply additive; they interact in a complicated fashion.<sup>33</sup> It has been shown that proton irradiation can cause linear integrated circuits to fail at much lower total-dose levels than can be tolerated for  $\gamma$  irradiation.<sup>34</sup> In some parts, the proton irradiation produced different failure mechanisms than those that occurred for  $\gamma$  irradiation, including catastrophic failures.

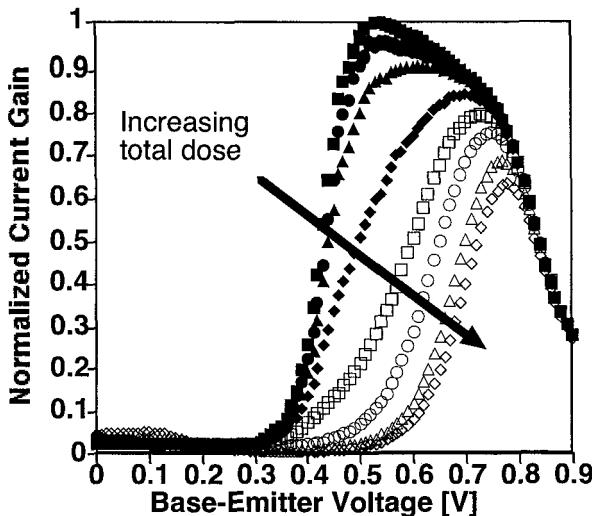


Figure 4 Normalized current gain vs. base-emitter voltage for an *n*p*n* BJT irradiated to various total doses.

The increase in surface recombination velocity is approximately proportional to the density of recombination centers at the silicon/silicon dioxide interface that covers the emitter-base junction. Traps with energies near the middle of the silicon bandgap are the most effective. Thus, the recombination centers are not precisely the same as the interface traps ( $N_{it}$ ) that are used to describe threshold-voltage shifts in MOS technologies. In discussions of irradiated MOSFETs,  $N_{it}$  usually refers to the total areal density of interface traps with energies between midgap and threshold. The increase in surface recombination velocity is often the dominant factor in determining the amount of radiation-induced gain degradation.

Since the net charge introduced into the oxide by ionizing radiation ( $N_{ox}$ ) is positive, the depletion region spreads on the *p*-side of a *pn* junction. For *n*p*n* transistors, the surface of the relatively lightly doped *p*-type base region becomes depleted. The recombination rate is maximized when the electron and hole populations are equal; this condition occurs at a point within the depletion region.

The increased recombination occurs around the edge of the emitter, so the amount of excess base current caused by surface recombination is proportional to the perimeter of the emitter.<sup>35</sup> Device layouts with large perimeter-to-area ratios increase the sensitivity to ionizing radiation because the excess base current (proportional to emitter perimeter) is large relative to the ideal component of the base current (proportional to emitter area).

Ionizing radiation also may change the effective doping concentration in *p*-type regions due to deactivation of acceptor atoms. This can affect the gain of *n*p*n* transistors by changing the number of electrons injected into the base or increasing the sensitivity to radiation-induced charge in the oxide.<sup>36</sup>

Vertical *pnp* transistors are relatively radiation hard compared to vertical *n*p*n* devices because positive radiation-induced trapped charge tends to accumulate the *n*-type base, reducing the width of the emitter-base depletion region. The positive charge depletes the *p*-type emitter, but the effect is typically small because of the high emitter doping.

In lateral *pnp* BJTs, the excess base current scales with the surface recombination velocity, which increases approximately in proportion to the number of interface traps. However,

this increase is moderated by the effects of positive charge in the oxide over the base. This positive charge accumulates the surface of the base, suppressing surface recombination. Thus, the effects of radiation-induced positive oxide charge and increased surface recombination velocity oppose each other. This may lead to a sublinear dependence of excess base current on total dose. In addition, lateral *pnp* BJTs with lightly doped emitters are more sensitive to total ionizing dose than those with more heavily doped emitters.<sup>37</sup> In the lightly doped devices, the depletion region is able to spread into the emitter, increasing the surface area where recombination may occur in the same fashion as occurs in *npn* BJTs.

Lateral *pnp* transistors are affected more significantly by ionizing radiation than substrate *pnp* transistors, since the current flow pattern in the LPNP devices is lateral and directly under the oxide where the recombination centers occur, while the current flow path in the SPNP devices is vertical. The current flow path in a lateral *pnp* BJT is illustrated in Figure 2.

If the surface of an LPNP BJT is depleted, then the radiation-induced recombination centers are most effective and the increase in base current is large. However, the surface potential in the base region can be controlled by placing a gate over the neutral base region. The surface recombination rate can be reduced by biasing the gate so that the surface of the base is accumulated, rather than depleted.<sup>28, 38, 39</sup> An emitter-tied field plate can be obtained by simply extending the emitter metallization over the base;<sup>28</sup> this can be accomplished at no increase in device or process complexity. If the gate can be biased independently, this offers much more flexibility in controlling the amount of radiation-induced degradation. If the gate bias is negative during irradiation, the electric field in the oxide is directed from the silicon to the gate, minimizing the degradation due to positively charged holes and protons. However, this bias condition maximizes the recombination rate for a given defect density. The ideal situation is to adjust the gate bias dynamically so that it is negative when the device is not operating and positive when the device is operating.<sup>39</sup> This reduces the amount of defect buildup during non-operational periods and reduces the effects of the defects when the device operates. This technique is most effective for devices that have long periods of time when they are exposed to radiation but are not operating. There also is additional layout complexity due to the independent gate electrodes.

Since the gain degradation in lateral *pnp* transistors is caused by radiation-induced interface traps, the radiation tolerance can be improved by reducing interface-trap buildup. This was demonstrated by implanting high doses of arsenic into the oxide that covered the neutral base of *pnp* transistors.<sup>40</sup> Both interface-trap density and radiation-induced current-gain degradation were smaller in devices that were fabricated with the implanted oxide.

## 4. Enhanced low-dose-rate sensitivity (ELDRS)

### 4.1. Overview

For some bipolar transistors, the amount of degradation at a given total dose depends on the rate at which the dose is accumulated, with more degradation occurring at lower dose rates.<sup>18, 41-49</sup> This phenomenon is referred to as Enhanced Low-Dose-Rate Sensitivity (ELDRS). The amount of degradation typically varies most rapidly with dose rate somewhere between 0.1 and 10 rad(SiO<sub>2</sub>)/s and is often approximately independent of dose rate for low and high dose rates. However, dose-rate sensitivity is very technology-dependent, so whether or not a given technology exhibits ELDRS and if so, the specific range of dose rates over which it occurs, are difficult to predict.

Laboratory testing is frequently conducted at dose rates of 50 rad(SiO<sub>2</sub>)/s or higher in order to complete the tests in a reasonable amount of time. However, this is significantly above

the dose rates at which ELDRS typically occurs. In contrast, dose rates in space systems vary dramatically depending on orbit and shielding, but values below 0.01 rad(SiO<sub>2</sub>)/s are typical. This can lead to overestimation of device lifetime if high dose rate tests are used to predict space-system behavior. Figure 5 is an illustrative plot of the normalized current gain vs. dose rate for a particular lateral *pnp* BJT, showing that the device response varies significantly in the range of dose rates between the space environment and typical laboratory tests.

ELDRS is typically observed only in relatively low quality oxides irradiated at low electric fields. Oxides covering the base region of BJTs frequently satisfy these conditions because they may be thick, may not have an electrode covering the oxide, and may have been used as an implant mask.

Developing hardness-assurance and test methods that are able to deal with the ELDRS effect has been a major challenge for radiation-effects researchers in recent years.<sup>45, 47, 48, 50-52</sup> Although accelerated test methods have been proposed,<sup>53, 54</sup> low-dose-rate testing is still advisable in critical applications.

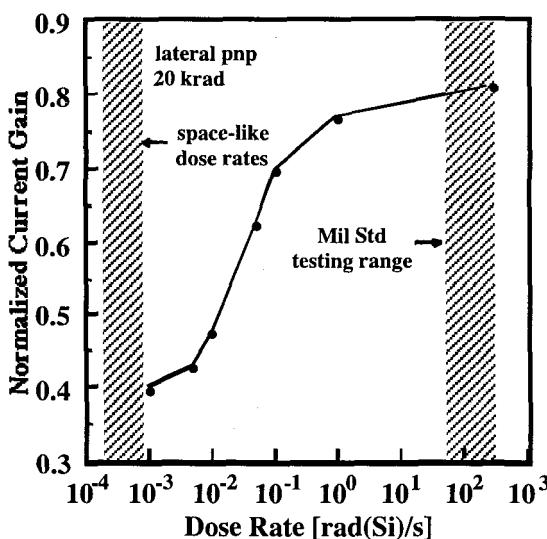


Figure 5 Normalized current gain vs. dose rate for a lateral *pnp* BJT irradiated to a total dose of 20 krad(Si) as a function of dose rate. The amount of degradation increases at low dose rates approaching those encountered in space (illustration courtesy of S. Witczak).

#### 4.2. True dose-rate effects

Although the total-dose response of MOS integrated circuits frequently depends on dose rate, the effects in MOS ICs are usually time-dependent effects rather than true dose-rate effects.<sup>55-61</sup> A true dose-rate effect occurs when a physical process responsible for the degradation depends on a quantity that is related to the dose rate. An example is a space-charge effect in which the presence of more charge at high dose rates changes the electric field, affecting the number of carriers surviving initial recombination and their subsequent transport. A time-dependent effect is one in which the same response can be obtained by waiting for a period of time following irradiation at the higher dose rate equal to the amount of time that is required to reach the same total dose by irradiation at the lower dose rate. The densities of oxide-

trapped charge ( $N_{ot}$ ) and interface-trapped charge ( $N_{it}$ ) both change following irradiation in many devices; typically,  $N_{ot}$  decreases due to annealing and  $N_{it}$  increases as slowly-transporting protons reach the interface. Both true dose-rate and time-dependent effects have been observed in bipolar devices, but it was the identification of a true dose-rate effect that was initially surprising.<sup>41</sup>

The ELDRS effect has been observed in both *npn* and *pnp* BJTs. An illustration of the excess base current vs. dose rate for an *npn* BJT is shown in Fig. 6.<sup>48</sup> This device was irradiated to a total dose of 40 krad(Si) and the base current was measured at  $V_{BE} = 0.6$  V. For this device type, the ELDRS appears to saturate near 0.005 rad(Si)/s. The degradation at this dose rate is approximately five times that which occurs at higher dose rates.

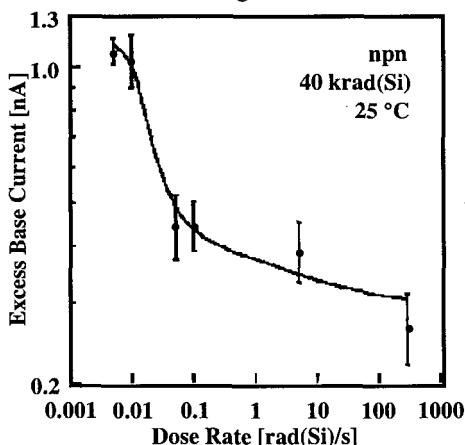


Figure 6 Excess base current vs. dose rate for an *npn* BJT measured at a total dose of 40 krad(Si) and  $V_{BE} = 0.6$  V (after<sup>48</sup>).

#### 4.3. Physical models

It has been suggested that ELDRS in BJTs is related to space-charge effects due to slowly-transporting holes.<sup>49, 50, 62-65</sup> The space charge that exists at higher dose rates retards the transport of holes (and also protons) to the interface. A critical dose rate exists at which the space charge has a significant effect on the electric field in the oxide. At dose rates far above or far below this, the charge buildup is nearly independent of dose rate. The transition between the two regions results in an S-shaped curve of excess base current vs. dose rate, as observed experimentally. Since both holes and hydrogen ions are affected by the space charge, this model applies to the dose-rate dependence observed experimentally in the buildup of both oxide charge and interface traps.<sup>65</sup>

At low dose rates, the net positive oxide charge and the interface-trap density are both found to be greater in some bipolar base oxides.<sup>62</sup> Thermally-stimulated current (TSC) measurements showed that the increased net positive oxide charge was due to increased electron compensation, rather than reduced hole trapping.

It also has been suggested that ELDRS may be a delayed reaction rate effect.<sup>66, 67</sup> This has been described by a model that assumes that the degradation results from interaction of two species, with different times required for the species to reach the Si/SiO<sub>2</sub> interface.<sup>66, 67</sup>

The ELDRS phenomenon also may depend on the thermal history of the devices<sup>68</sup> and the presence (or absence) of passivation layers on the die.<sup>69</sup> Both of these issues may be related to the packaging process. Although the physical mechanisms responsible for these effects have not been identified conclusively, hydrogen and mechanical strain induced by the passivation layer both may play important roles.

## 5. Conclusions

Bipolar transistors play a variety of important roles in systems where they are exposed to radiation. Although most of the parts currently deployed are fabricated in traditional Si technologies with vertical *npn* and lateral *pnp* transistors, there are exciting new applications for high-speed technologies utilizing heterojunction bipolar transistors. Understanding radiation effects at both the device and circuit levels is essential for fielding radiation-tolerant systems.

When BJTs are exposed to radiation, the base current increases and the current gain decreases. Increased recombination in the emitter-base depletion region is the main mechanism responsible for the increased base current. In *npn* BJTs, the degradation is due to the combined effects of increased surface recombination velocity due to radiation-induced interface traps and changes in surface potential caused by oxide trapped charge. In *pnp* transistors, the base current increases due to the increased surface recombination velocity, but the increase is moderated by the oxide trapped charge since it moves the base surface toward accumulation. Typically lateral *pnp* transistors are softer than vertical *npn* transistors because the current path is near the Si/SiO<sub>2</sub> interface.

Many bipolar technologies degrade more at low dose rates than at high dose rates for a given total dose. This ELDRS phenomenon is a difficult hardness-assurance challenge because testing at standard laboratory dose rates overestimates the radiation hardness of the parts in space systems. Methods of predicting the low-dose-rate response using laboratory dose rates, including irradiation at high temperature, have been proposed. While these methods have been reasonably successful at identifying technologies that suffer from ELDRS, it is still difficult to identify a single test for all bipolar technologies.

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## TOTAL DOSE EFFECTS IN LINEAR BIPOLAR INTEGRATED CIRCUITS

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**Abstract.** Electronics systems that operate in space or strategic environments can be severely damaged by exposure to ionizing radiation. Space-based systems that utilize linear bipolar integrated circuits are particularly susceptible to radiation-induced damage because of the enhanced sensitivity of these circuits to the low rate of radiation exposure. The phenomenon of enhanced low-dose-rate sensitivity (ELDRS) demonstrates the need for a comprehensive understanding of the mechanisms of total dose effects in linear bipolar circuits. The majority of detailed bipolar total dose studies to date have focused on radiation effects mechanisms at either the process or transistor level. The goal of this text is to provide an overview of total dose mechanisms from the circuit perspective; in particular, the effects of transistor gain degradation on specific linear bipolar circuit parameters and the effects of circuit parameter degradation on select linear bipolar circuit applications.

**Keywords:** Bipolar junction transistor, linear bipolar circuit, operational amplifier, voltage comparator, voltage regulator, total ionizing dose, enhanced low-dose-rate sensitivity, current gain, base current, Co-60  $\gamma$ -rays, irradiation bias, input transistor, input bias current, input offset voltage, input offset current, maximum output drive current

### 1. Introduction

In 1962, radiation-induced degradation in a discrete bipolar junction transistor (BJT) was identified as the cause of failure in the newly-deployed communications satellite Telstar<sup>1</sup>. At that time the primary failure mechanism was determined to be related to the ionization of an unspecified gas within the encapsulated part's package<sup>2</sup>. The excess charge generated by ionization was transported to the device surface, causing deterioration in the transistor's electrical characteristics. Although gas-filled packages are still used today (most hermetic packages are back-filled with nitrogen), ionized gas has rarely been identified as the primary failure mechanism in irradiated bipolar parts. Instead, radiation-induced ionization in the oxide layers, which are used ubiquitously in conventional bipolar processes, is the primary source of concern for the long-term reliability of systems that operate in harsh radiation environments and utilize BJTs and linear bipolar circuits.

Modern satellite and strategic systems rely heavily on linear bipolar parts for numerous subsystem functions, including signal amplification, voltage regulation, and the conversion of information between analog and digital. Among the most widely used linear part types in these systems are: operational amplifiers, voltage comparators, and voltage regulators. Linear bipolar circuits manufactured in conventional processes are especially attractive to both system designers and program managers because of their versatility and low cost. Indeed, a standard commercial-off-the-shelf quad operational amplifier can be purchased for about \$1.

Designers of systems operating in space and/or nuclear environments must balance these advantages with the sensitivity of bipolar components to several radiation threats. The class of significant radiation effects on linear bipolar circuits includes single event transients (time-dependent variations in the voltage or current at an analog circuit's external ports that are caused by the passage of heavy ions through a sensitive node)<sup>3</sup> and displacement damage (degradation to electrical characteristics caused by radiation induced damage to the semiconductor bulk)<sup>4-6</sup>. However, since its first observation on the Telstar satellite over four decades ago, radiation-induced ionization damage to bipolar components has generally been considered the most significant threat to linear bipolar circuits operating in radiation environments.

The numerous physical mechanisms of total ionizing dose (TID) damage in bipolar components have been investigated for over four decades<sup>7</sup>. The research has ranged from the study of the basic physics of radiation defect buildup and transistor response<sup>8-21</sup> to the identification, analysis, and characterization of circuit-level response mechanisms<sup>22-32</sup>. Research in the past decade has primarily focused on the phenomenon of enhanced low-dose-rate sensitivity (ELDRS). In 1991, it was reported that the amount of radiation-induced parametric degradation in a bipolar device was dependent on the dose rate at which the TID accumulated, with more degradation occurring at lower dose rates<sup>12, 33</sup>. Since there exist radiation environments (e.g., space) where electronic components are irradiated at low dose rates, ELDRS is a real problem for systems designed with linear bipolar circuits. Indeed, the costs in time and resources for qualifying bipolar parts to operate in low-dose-rate environments are often prohibitive. The data in Figure 1 illustrate ELDRS for various linear bipolar circuits. As the figure indicates, the relative amount of damage, normalized to a dose rate of 50 rad(Si)/s, increases for most of the parts as the dose rate is decreased. In this data set, all of the parts have been irradiated to 50 krad(Si). The data also show that ELDRS is a function of part type. The researchers who first reported these data in 1994 correlated the polarity of sensitive transistors in the circuit (i.e., pnp or npn BJTs) with the circuit's low-dose-rate sensitivity. It was suggested that linear bipolar parts designed with pnp devices in sensitive regions of the circuit topology were likely to show more ELDRS than other parts<sup>25</sup>. While transistor polarity continues to be considered a mechanism for TID effects and ELDRS in bipolar circuits, in the past few years the origins of low-dose-rate sensitivity have begun to be related more to fabrication variables, such as the post-processing thermal cycles and the type and quality of circuit passivation materials<sup>34-36</sup>.

Concern regarding ELDRS in BJTs has been the driving force behind TID research in linear bipolar circuits. Understanding response mechanisms related to temperature stress and post-irradiation annealing have also been areas of active research. However, this paper will focus on describing TID mechanisms at circuit and application levels rather than investigating dose rate, thermal, or annealing effects in bipolar devices. These discussions will be supported by specific examples. The text is organized into three sections: 1) an overview of total dose effects in bipolar devices and circuits, 2) a description and analysis of total dose effects on the critical specification parameters of operational amplifiers and voltage comparators, and 3) a description and analysis of total dose effects on the critical specification parameters of voltage regulators. The latter two sections will consider how radiation-induced degradation in circuit parameters can affect the performance of linear circuit applications as well as examine how

parametric response to TID is affected by circuit topology, bias conditions, and other design variables. The discussions will be supported by detailed analyses of the TID degradation mechanisms of three commercially available linear bipolar circuits: the LM101 operational amplifiers, the LM111 voltage comparator, and the LM117 voltage regulator. These circuits were selected for analysis primarily because the methods used to test these parts and their unique radiation responses provide insights into total dose effects in most conventional linear bipolar integrated circuits.

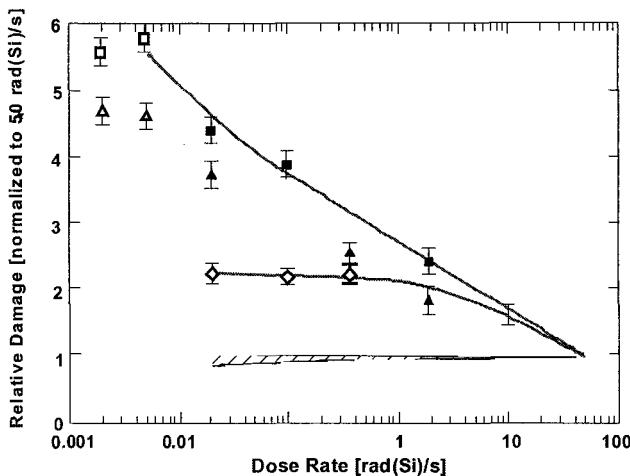


Figure 1. Relative damage vs. dose rate for irradiation to 50 krad(Si) for several linear ICs<sup>25</sup>.

## 2. Overview of Total Ionizing Dose Effects

### A. Bipolar Junction Transistors

Total ionizing dose effects in bipolar technologies are primarily characterized by the buildup of two types of defects within an integrated circuit's oxide layers (fixed net positive-oxide-trapped-charge) or at the semiconductor-oxide interface (interface traps)<sup>2</sup>. The principal result of these defects is a reduction of common emitter current gain ( $\beta$ ) of the BJTs integrated into the linear bipolar circuit. Common emitter gain, the primary figure of merit for bipolar devices, is defined as the ratio of collector current ( $I_C$ ) to base current ( $I_B$ ), i.e.,  $\beta = I_C/I_B$ .

The curves in Figure 2 exemplify the effects of ionization defects on transistor current gain. These data show the degradation in current gain vs. base-emitter voltage for a vertical NPN BJT exposed to various total dose levels<sup>15</sup>. The primary cause of reduced current gain in irradiated BJTs (of both polarities) is an increase in base current ( $I_B$ ) due to increased recombination via the radiation-induced oxide defects<sup>9, 15, 18</sup>. In npn transistors, TID has a negligible impact on collector current<sup>15</sup>. This is indicated on the Gummel curves ( $I_C$  and  $I_B$  vs. base-emitter voltage) in Figure 3. These data correspond to those presented in Figure 2. Studies have demonstrated that the collector current in pnp transistors can show small but measurable reductions upon radiation exposure<sup>21, 37</sup>

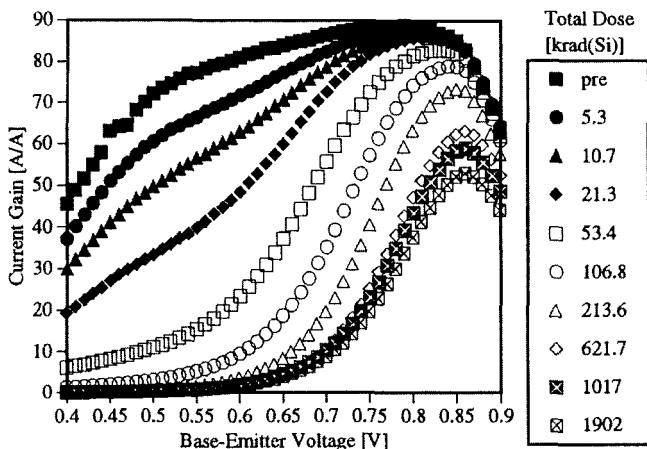


Figure 2. Current gain vs. base-emitter voltage for NPN BJTs exposed to various levels of TID<sup>15</sup>.

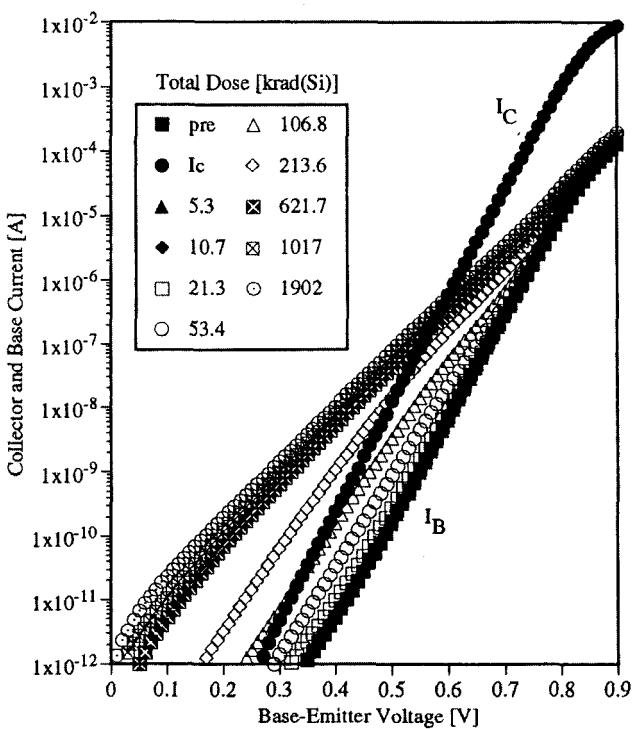


Figure 3.  $I_C$  and  $I_B$  vs. base-emitter voltage (Gummel curves). Data correspond to the gain curves in Figure 2<sup>15</sup>.

#### B. Operational Amplifiers and Voltage Comparators

Reduced current gain can have a significant impact on critical linear bipolar circuit parameters. For operational amplifiers and voltage comparators, the most sensitive specification parameters to TID are typically: input bias current ( $I_b^+$  and  $I_b^-$ ), input offset

current ( $I_{os}$ ), and input offset voltage ( $V_{os}$ ). The two input bias currents and the offset voltage are shown as independent sources in the idealized amplifier/comparator model in Figure 4.  $I_b^+$  and  $I_b^-$  are modeled as ideal current sources from the non-inverting and inverting input nodes ( $V^+$  and  $V^-$ ), respectively, and  $V_{os}$  is an ideal voltage source between the actual, external non-inverting node ( $V^+$ ) and the ideal non-inverting node ( $V_I$ ). The input offset current is not represented on the figure because it is simply the magnitude of the difference between  $I_b^+$  and  $I_b^-$ .

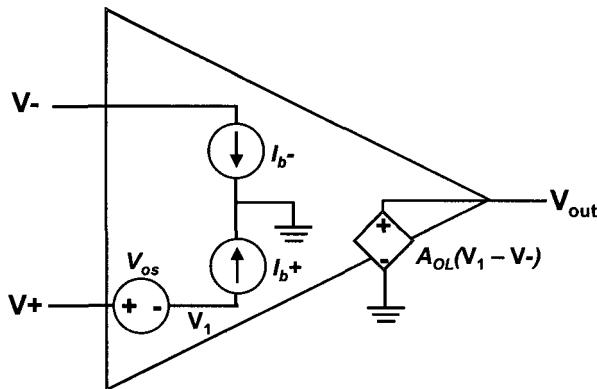


Figure 4. Circuit model of operational amplifier/voltage comparator. DC current sources represent references for input bias currents and dc voltage source represents reference for input offset voltage.

All linear components designed with bipolar differential amplifier input stages (e.g., operational amplifiers and voltage comparators) require some input bias current to operate. However, these currents are designed to be very low and matched ( $I_{os} \approx 0A$ ) in order to achieve high circuit input impedance and prevent signal distortions (due to non-linearities) and loss of dynamic range (due to offsets). For standard commercial-off-the-shelf bipolar amplifier/comparator circuits, a nominal value for input bias current is 10 nA. Maximum specifications are rarely higher than 100 nA<sup>38</sup>. Exposure to ionizing radiation often causes significant increases in input bias current. This effect is observed in Figure 5<sup>29</sup> in which the input bias current for LM124 operational amplifiers is plotted vs. total dose at various dose rates. In these tests, irradiations were performed with a Co-60  $\gamma$ -ray source. The figure indicates that, even at a standard laboratory dose rate of 100 rad(Si)/s, input bias current increases above its maximum specification (50 nA) before the exposure level reaches 100 krad(Si). The data also demonstrate the LM124 exhibits enhanced, low-dose-rate sensitivity. Indeed, at the lowest dose rate (1 mrad(Si)/s), the part reaches its specification limit before 10 krad(Si).

A monotonic increase in bias current is typically a signature of gain degradation in a circuit's input transistors. In most bipolar operational amplifiers and voltage comparators, the input bias currents are the base currents of the respective input transistors. Thus, if other dc operating point voltages and currents remain fixed as a function of total dose, radiation-induced increases in input transistor base current will lead directly to a monotonic increase in input bias current at the circuit level. In a subsequent section of this paper, it will be shown that input bias current does not always increase monotonically with total dose. In some

circuits, the topology is such that gain degradation in non-input BJTs can also have an impact on the bias current degradation.

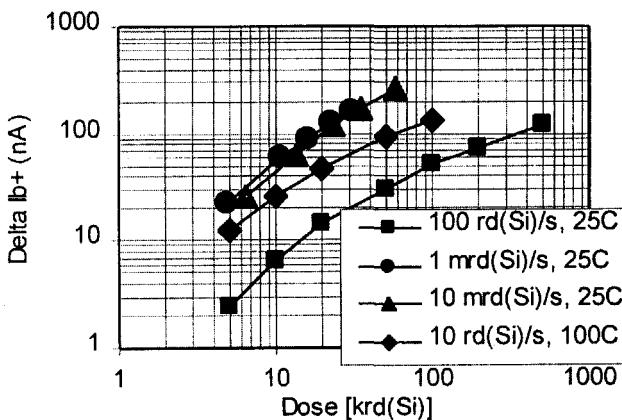


Figure 5. LM124 average increase in  $I_{b+}$  vs. dose<sup>29</sup>

Ionizing radiation can also affect the offset parameters,  $V_{os}$  and  $I_{os}$ . Offset errors can further affect the functionality of circuit applications, particularly in mixed-signal applications that require large dynamic ranges (e.g., bit resolution in analog-to-digital converters). Radiation-induced drifts in offset parameters are often signatures of an imbalance in the rate of degradation in BJTs designed to operate as matched pairs. For example, if the current gain in an emitter-coupled input transistor pair (of an amplifier/comparator input stage) degrades unevenly such that there exists a non-negligible gain differential,  $\Delta\beta$ , then the input bias current offset will degrade to

$$I_{os} = I_b \left( \frac{\Delta\beta}{\beta} \right), \quad (1)$$

where  $I_b$  is the average input bias current ( $(I_b^- + I_b^+)/2$ )<sup>39</sup>. Non-uniform degradation arises when different dc bias conditions are applied to matched transistors during radiation exposure<sup>29, 40</sup>. This effect is illustrated in Figure 6, where the increase in the input offset current of a LM139 voltage comparator is plotted vs. total dose for different dose rates. In this experiment, the parts were exposed in Co-60 sources under large differential input voltage bias conditions. As with the  $I_b$  data of the LM124,  $I_{os}$  for the biased LM139 exhibits a low-dose-rate effect.

Degradation of input offset voltage is strongly dependent on irradiation bias conditions. However, unlike input offset current, a deterioration in  $V_{os}$  is most likely not dependent on gain degradation in the input transistors of amplifiers and comparators. Although the exact causes of radiation-induced offset voltage degradation have yet to be precisely identified, likely mechanisms include: 1) unbalanced gain degradation in transistors used to form the active loads for the input stage differential amplifier(s)<sup>39</sup> and 2) unbalanced degradation in the devices used to form the circuit's output stage. The susceptibility of the output stage amplifier to biased irradiations will be discussed in detail in section 3.

The effect of total dose irradiations on the  $V_{os}$  parameter is shown in Figure 7. The figure

plots the increase in offset voltage vs. total dose for an LM111 voltage comparator, biased with a large differential input voltage during radiation exposure. As with the previous radiation responses shown in Figures 5 and 6, the  $V_{os}$  parameter of this circuit also demonstrates ELDRS.

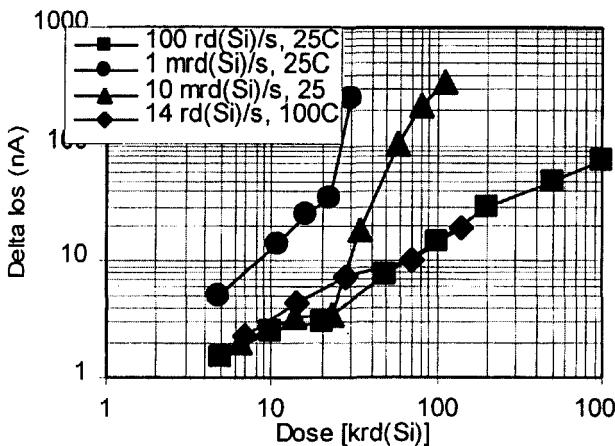


Figure 6. LM139 average increase in  $I_{os}$  vs. dose.<sup>29</sup>

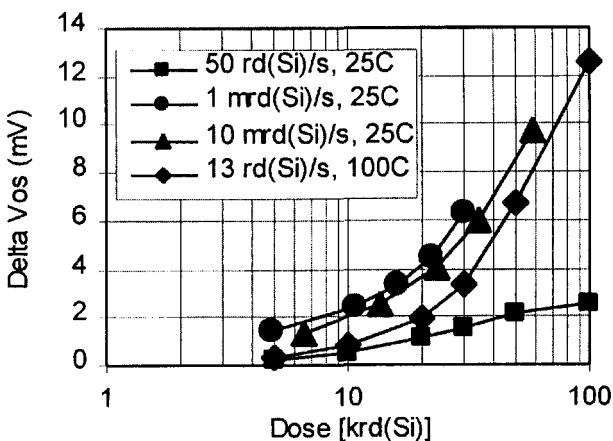


Figure 7. LM111 average increase in  $V_{os}$  vs. total dose.<sup>29</sup>

### C. Voltage Regulators

The function of a voltage regulator is to provide a constant voltage,  $V_{out}$ , to a load,  $I_o$ . In many regulator circuits, an unregulated, potentially variable voltage  $V_{in}$  serves as both the regulator input and one of the power supply rails. Voltage regulators are commonly used in ac-to-dc converter applications such as power supplies. Their function in these applications is to remove time-dependent ripples in voltage signals in order to generate dc voltages that are stable with input voltage, load, and temperature.<sup>39</sup> A typical voltage regulator application is shown in Figure 8. In this adjustable configuration, the output voltage is set by an internal

band-gap voltage reference ( $V_{ref}$ ) and an adjustable voltage divider determined by external resistors  $R_x$  and  $R_y$ <sup>29</sup>.

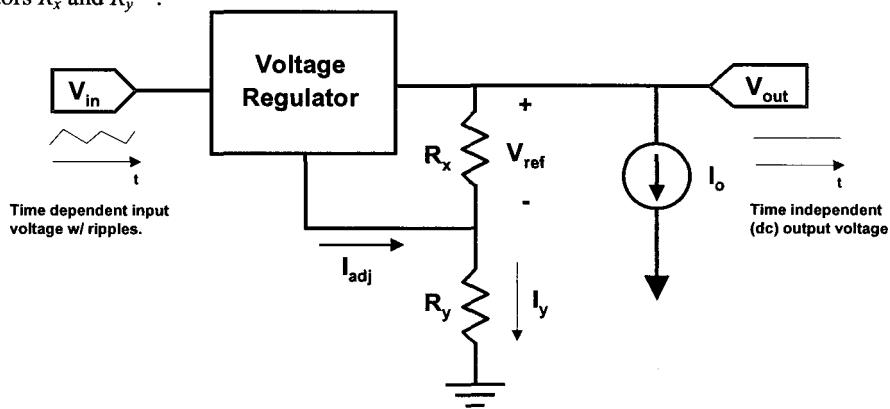


Figure 8. Typical adjustable voltage regulator configuration<sup>38</sup>

In normal operation, the adjust pin current is small ( $I_{adj} \approx 50 \mu\text{A}$ ) relative to the current through resistor  $R_y$  ( $1 \text{ mA} < I_y < 4 \text{ A}$ ), and thus the relationship between the output and reference voltage can be approximated as

$$V_{out} = V_{ref} \frac{R_x + R_y}{R_x}. \quad (2)$$

Degradation in the regulated output voltage is caused by radiation-induced alterations to the critical regulator parameters,  $I_{adj}$ ,  $V_{ref}$ , and the maximum output drive current. Figure 9 plots the change in  $I_{adj}$  as a function of total dose for LM117 voltage regulators exposed to Co-60  $\gamma$ -rays at a dose rate of 150 rad(Si)/s. The adjust current response to TID is non-monotonic with dose. In a 1996 study on the LM117, it was determined that the behavior of  $I_{adj}$  with dose was a function of multiple BJT degradation mechanisms in the four transistors that constitute the internal bandgap reference (i.e., gain degradation in the two lateral pnp devices and both gain degradation and collector-to-emitter leakage in the two vertical npn devices<sup>22</sup>).

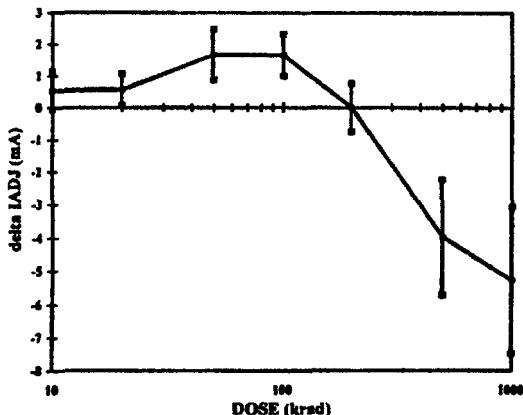


Figure 9. Adjust pin current vs. total dose for LM117 adjustable voltage regulator<sup>22</sup>.

In Figure 10, the change in  $V_{ref}$  is plotted vs. total dose for an HS117 voltage regulator, for biased and unbiased parts, irradiated at two different dose rates. The parts were irradiated with Co60  $\gamma$ -rays at dose rates of 61, 0.25 (high temperature), and 0.05 rad/s. These data, originally reported in 1998, indicate the HS117 circuit exhibits a significant ELDRS effect, but only when no bias is applied during radiation exposure<sup>41</sup>. This response is consistent with the prevailing model for low-dose-rate effects in bipolar parts, which suggests a low electric field across a BJT oxide is a necessary condition for ELDRS<sup>14</sup>. This condition exists when a part is unbiased since there exist no externally applied voltages across the any of the circuit's oxide layers that are ionized during radiation exposure.

Voltage regulators are designed to maintain stable output voltages while driving a range of load currents. Minimum load currents are nominally between of 1 and 10 mA. Maximum output drive currents ( $I_o(max)$ ) range between 0.5 and 4 A. Loads above  $I_o(max)$  will result in a drop in  $V_{out}$  (loss of regulation). The ability of a voltage regulator to supply current to large loads is dependent on the current gain of the regulator circuit's output transistor(s). Thus, if the output device(s) is susceptible to TID gain degradation,  $I_o(max)$  will show significant deterioration, as illustrated in Figure 11<sup>42</sup>. This data set, obtained from measurements on Co-60 irradiated 29372 low-dropout voltage regulators, shows  $I_o(max)$  to be both total dose and dose rate sensitive. The output transistor of the 29372 circuit is a large multiple emitter lateral pnp transistor. Numerous studies on radiation effects on lateral pnp (lppn) BJTs have shown these devices to be particularly vulnerable to gain degradation from TID<sup>9, 18, 31</sup>. This is due to the fact that, as they are lateral structures, the primary path for current in lppn BJTs is near the semiconductor-oxide interface, in close proximity to radiation-induced defects<sup>9</sup>.

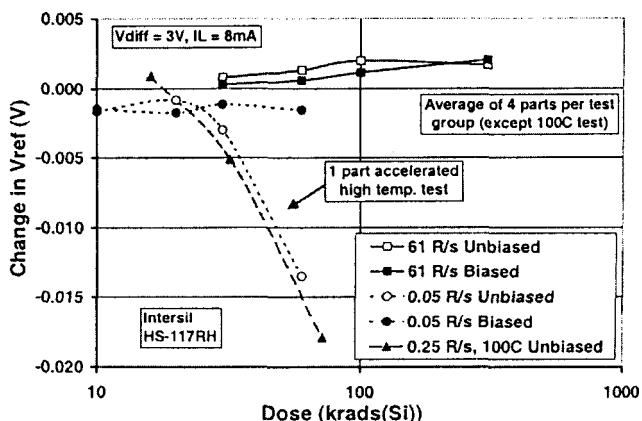


Figure 10. Change in  $V_{ref}$  vs. dose for an HS117 voltage regulator exposed at high and low-dose-rates at two bias conditions (biased and unbiased)<sup>41</sup>.

In this section we have attempted to provide a general overview of TID effects in bipolar devices and circuits. In bipolar transistors, exposure to TID reduces the current gain primarily by increasing the base recombination current. Because of mechanisms related to the low electric fields across bipolar oxide layers, parametric degradation in BJTs is often enhanced when devices are exposed at low dose rates. Linear circuits fabricated with BJTs (e.g., operational amplifiers, voltage comparators, and voltage regulators) are, by extension, also

susceptible to radiation-induced parametric degradation and ELDRS. These effects are illustrated in the data sets presented above.

In the next two sections, TID effects on critical circuit specification parameters for selected linear bipolar parts will be discussed. These discussions will include examples of how radiation-induced parametric degradation at the circuit-level may effect subsystem applications and approaches used in identifying TID degradation mechanisms at the circuit-level.

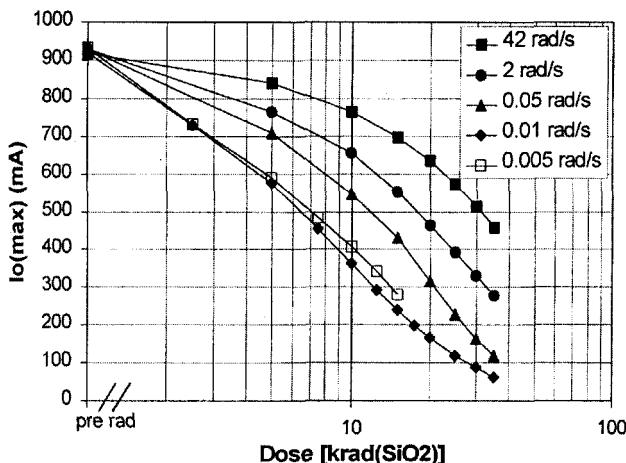


Figure 11.  $I_o(\max)$  vs. dose for a 29372 low-dropout regulator at several dose rates, showing low-dose-rate sensitivity.<sup>42</sup>

### 3. Total Ionizing Dose Effects on Operational Amplifiers and Voltage Comparators

#### A. Effects of Input Bias Current Degradation on a Current-to-Voltage Converter

Figure 12 shows the schematic for a widely-used operational amplifier application: the current-to-voltage (IV) converter. Circuits similar to the IV converter can be found in many mixed signal applications, such as R2R ladder D/A converters. In this application, the current into or out of a device-under-test,  $I_{DUT}$ , is converted to a voltage,  $V_O$ , so that it may be sampled digitally. The ideal relationship between the  $I_{DUT}$  and  $V_O$  is

$$V_O = -I_{DUT} R_{fb}, \quad (3)$$

where  $R_{fb}$  is the feedback resistor. If the digital electronics of a system are capable of sampling voltages between 5 mV and 5V (e.g., a 12 bit A/D converter), a 100 k $\Omega$  feedback resistor will enable the measurement of currents between 50 nA (5 mV) and 50 uA (5 V). If  $I_{DUT}$  is equal to 100 nA, the converter will ideally generate an output voltage of 10 mV. This sample voltage can then be used to calculate  $I_{DUT}$  using Equation 3. This ideal operation is illustrated schematically in Figure 11a. If the input bias current of the operational amplifier increases significantly, it will cause the IV converter to have a measurable offset error:

$$\Delta V_O = \Delta I_b R_{fb}. \quad (4)$$

This will cause the measured output voltage to be reduced to  $V_O - \Delta V_O$ , and unless circuitry is

built into the system to correct for this continuously degrading offset, the current will be computed as  $I_{DUT} - \Delta I_b$ . Input bias current degradation of over 50 nA, which is possible after 10 krad of exposure at a 1 mrad/s dose rate – or less than four months in space<sup>30</sup> – will make it impossible to be more than 50 % accurate in current measurements below 100 nA.

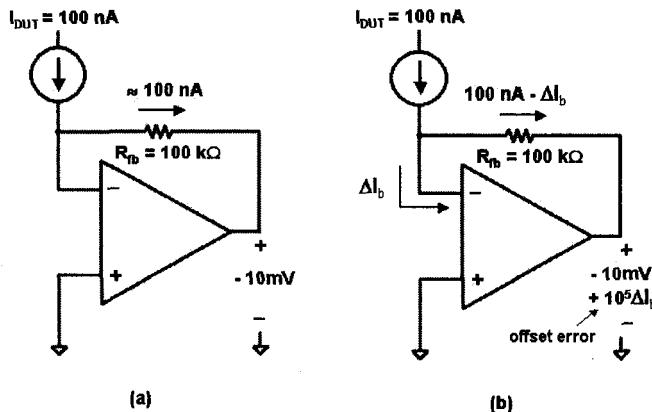


Figure 12. Schematics of current-to-voltage converter applications show a) ideal operation and b) operation with offset error which is increased by radiation-induced input bias current degradation.

Radiation-induced offset errors and loss of dynamic range are very common in mixed signal applications that rely on low input bias current in their operational amplifiers. Problems associated with input bias current degradation may be avoided by using linear bipolar circuits with JFET transistor inputs<sup>40</sup>.

#### B) Radiation Response of Input Bias Current in an LM111 Voltage Comparator

Most radiation response measurements of bipolar operational amplifiers and voltage comparators have indicated input bias current increases monotonically with TID exposure<sup>24-30, 40, 43</sup>. However, TID data on LM111 voltage comparators reported in 1999 showed that input bias current exhibited a downward trend or “recovery” for doses above 100 krad(SiO<sub>2</sub>)<sup>23</sup>. Figure 13 shows the input bias current radiation response characteristics for Co-60-irradiated LM111 voltage comparators at two dose rates. Once again, this linear bipolar circuit exhibits enhanced low-dose-rate sensitivity.

The authors of this LM111 study demonstrated, through electrical measurements on isolated circuit transistors, parameter extraction, and SPICE simulations, that increased input bias current ( $I_{IB}$ ) was due to degradation in the circuit’s input transistors and that “recovery” was due to gain degradation in *non-input* devices integrated into the LM111 internal circuitry<sup>23</sup>. Figure 14a shows the equivalent, single-ended subcircuit schematic for the differential input stage of the LM111 comparator. Figure 14b shows, along with the high dose rate data, the simulated subcircuit  $I_{IB}$  characteristics with total dose. The figure demonstrates that the simulations reproduce the non-monotonic characteristics of the experimental data<sup>23</sup>. A detailed breakdown of the numerous circuit mechanisms underlying the radiation response of

the LM111 input bias current was presented by Barnaby *et al.* in their 1999 paper. A brief summary of their conclusions is as follows:

Under some basic assumptions, the change in  $I_{IB}$  can be approximated as

$$\Delta I_{IB} \approx K \left[ \frac{I_{SE1(\text{pre})} \Delta V_{eb1}}{n_e V_T} + \Delta I_{SE1} \left( 1 + \frac{\Delta V_{eb1}}{n_e V_T} \right) \right], \quad (5)$$

where  $K$  is a proportionality constant,  $\Delta V_{eb1}$  is the radiation-induced change in the forward bias across the emitter base junction of Q1 (this is assumed to be 50 mV or less),  $n_e$  is the base-emitter leakage ideality factor of Q1,  $I_{SE1(\text{pre})}$  is the pre-irradiated value for the base-emitter leakage current of Q1, and  $\Delta I_{SE1}$  is the radiation-induced change in the leakage current for Q1<sup>44</sup>.  $\Delta I_{SE1}$  increases monotonically with total dose. This is caused by increased carrier recombination within the emitter-base depletion region of the input device, Q1<sup>9, 15, 18</sup>. As indicated by Equation 5, increasing  $\Delta I_{SE1}$  in turn increases  $I_{IB}$ . Therefore, gain degradation in the LM111 input structures causes the monotonic increase in  $I_{IB}$  below 100 krad(SiO<sub>2</sub>).

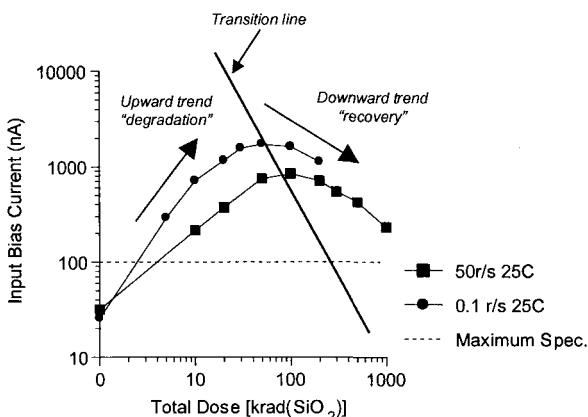


Figure 13. Input bias current radiation response for LM111 comparator at 50 and 0.1 rad(SiO<sub>2</sub>)/s. These data indicate ELDRS and parametric "recovery" at high doses. The maximum specification is 100 nA<sup>23</sup>.

The "recovery" in the response at doses above 100 krad(SiO<sub>2</sub>) was determined to be caused by the effects of gain degradation in transistors Q2 and Q3. Degradation in Q3 leads to an increase in  $I_{b3}$ . Degradation in Q2 leads to a decrease in  $I_{c2}$ . The combined effect of radiation on these two dc current components steals collector current away for the input transistor Q1. This causes  $V_{eb1}$  to decrease and, as indicated in Equation 5, causes a reduction in  $I_{IB}$ . Gain degradation in non-input devices thus compensates for increased base current in the LM111 input device and leads to a partial recovery in the input bias current response at high doses<sup>23</sup>.

One of the most important conclusions that can be drawn from this analysis is that TID degradation mechanisms at the circuit level can be significantly more complex than the responses of individual transistors. Analysis and separation of these higher-order circuit mechanisms typically require pre- and post-irradiation transistor parameter extraction and SPICE simulation. The scanning electron microscope has also been used extensively to

characterize circuit-level TID mechanisms.

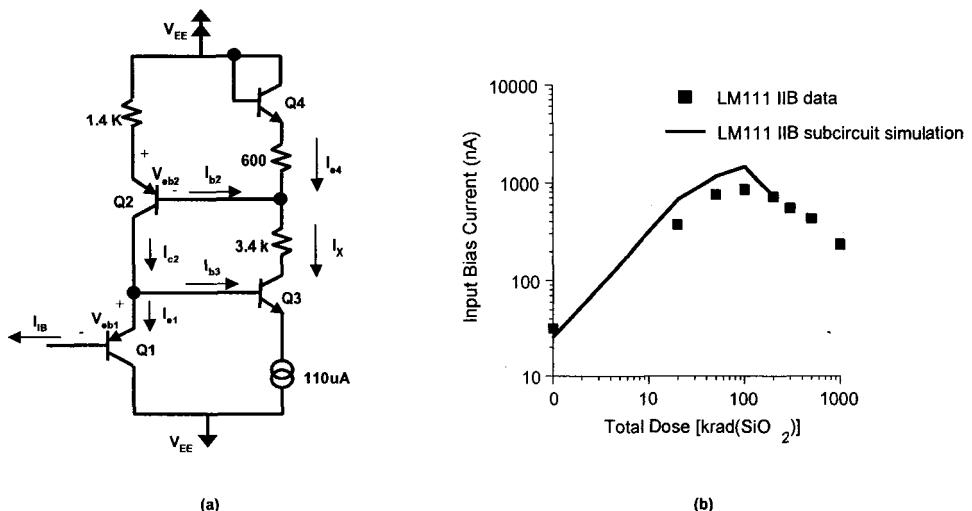


Figure 14. (a) Equivalent, single-ended subcircuit schematic for the differential input stage of the LM111 comparator and (b) simulated and experimental input bias current radiation response. The simulations model the upward ("degradation") trend at low doses and subsequent downward ("recovery") trend at high doses<sup>23</sup>.

### C. S.E.M. Irradiation of LM101 Operational Amplifier

As mentioned previously, irradiation bias can have a significant impact on the radiation response of bipolar devices and circuits (e.g., Figure 10). Moreover, as demonstrated above, parametric degradation in linear bipolar circuits may be the result of complex interactions between several degraded devices. Understanding how the radiation response of individual devices and subcircuits contribute to the overall circuit response is in many instances a difficult task that is further complicated by additional variables such as irradiation bias conditions. Several studies have used scanning electron microscopes (SEMs) to help separate and characterize circuit-level TID mechanisms<sup>31, 45</sup>. In this section, SEM irradiation data on LM101 operational amplifiers is discussed.

As long as the electron energy is set to an appropriate level, a SEM can cause ionization damage that may be correlated to the damage caused by high-energy photons (e.g., Co-60  $\gamma$ -rays). In the SEM data presented below, the electron energy was set to 40 keV. The electron flux was set to  $1.88 \times 10^{10}$  e/cm<sup>2</sup>s, which was equivalent to a dose rate of 2.5 krad(Si)/s (i.e.,  $7.5 \times 10^6$  e/cm<sup>2</sup>s – 1 rad(Si)).

Figures 15 through 18 plot the increased input bias current ( $\Delta I_{IB}$ ) and offset voltage ( $\Delta V_{OS}$ ), for LM101 operational amplifiers irradiated by 40 keV SEM electrons. For the data shown in Figure 15, whole LM101 chips were exposed without an externally applied bias. Under these conditions,  $\Delta I_{IB}$  increases linearly with total dose to a level well above the maximum specification of 75 nA after 1 Mrad equivalent of electron irradiations, while  $\Delta V_{OS}$  does not increase significantly (less than 5% of the 2 mV specification). Figure 16 shows the radiation response of whole chips biased during SEM exposures. The results are similar to those shown in Figure 15 up to 100 krad(SiO<sub>2</sub>). However, above 100 krad(SiO<sub>2</sub>), there is a

sharp increase in  $\Delta V_{OS}$  and a significant upward shift in  $\Delta I_{IB}$ .

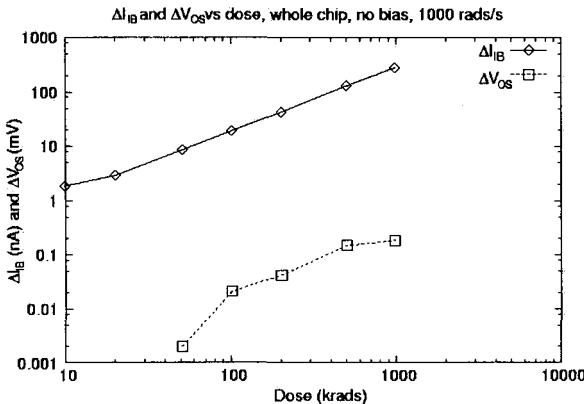


Figure 15. Increased input bias current and offset voltage in unbiased LM101 operational amplifiers irradiated by 40 keV SEM electrons. Data show bias current degrades and offset voltage does not degrade in response to exposure.

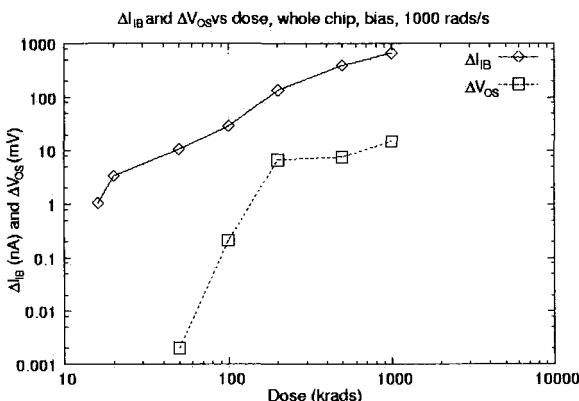


Figure 16. Increased input bias current and offset voltage in biased LM101 operational amplifier irradiated by 40 keV SEM electrons. Data show bias current degrades and offset voltage does not degrade in response to exposure.

In order to identify circuit-level mechanisms that underlie the bias dependence of the operational amplifier's radiation response, localized SEM irradiations were performed on two subcircuits of the LM101: the input npn transistor emitter-coupled-pair and the output stage. In Figure 17, the parametric responses are plotted for localized irradiations on the input transistors. In Figure 18,  $\Delta I_{IB}$  and  $\Delta V_{OS}$  are plotted for localized irradiations on the LM101 output stage.

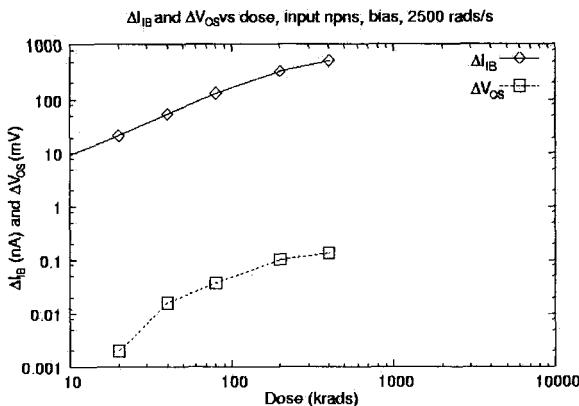


Figure 17. Increased input bias current and offset voltage in biased localized irradiations of the input transistors of LM101 operational amplifiers. Data show bias current degrades and offset voltage does not degrade in response to input transistor exposure.

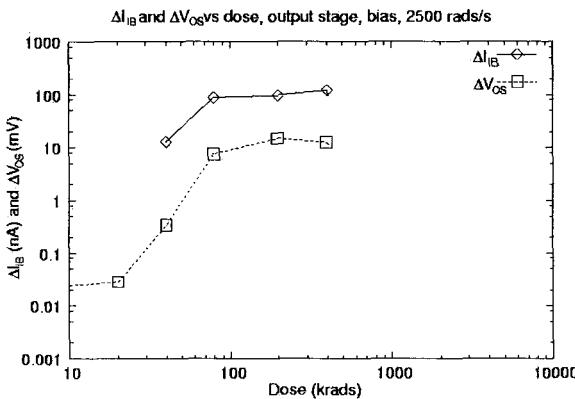


Figure 18. Increased input bias current and offset voltage in biased localized irradiations of the output stage of LM101 operational amplifiers. Data show both bias current degrades and offset voltage after 100 krad(SiO<sub>2</sub>).

The results of these localized SEM irradiations effectively demonstrate numerous TID mechanisms for the LM101 circuit. First of all, the response to localized irradiations on the input transistors demonstrates gain degradation in these devices causes deterioration in  $\Delta I_B$  but not in  $\Delta V_{OS}$ . Second, the fact that  $\Delta I_B$  degraded similarly when either the whole chip was irradiated under no bias, or when only the input devices were irradiated under bias, indicates that the gain degradation in input transistors does not depend significantly on bias. Lastly, above 100 krad(Si), gain degradation in the BJTs of the output stage caused an abrupt increase in  $\Delta V_{OS}$ , as well as additional degradation in  $\Delta I_B$ . The results confirm offset voltage is dependent on irradiation bias and is only a function of degradation in *non-input* structures. An additional and surprising result is that input bias current shows additional degradation due to deterioration in output stage components. All of these results are consistent with claims made in section 2B regarding the circuit-level mechanisms of parametric degradation in operational amplifiers and voltage comparators. These experimental results demonstrate that the

identification of the complex interactions between individual circuit-level radiation response mechanisms can be facilitated by the use of localized insitu SEM irradiations.

#### 4. Total Ionizing Dose Effects on Voltage Regulator

##### A. Effects of $I_o(\max)$ Degradation on Mixed Signal Regulator Application

Voltage regulators are used extensively in mixed signal applications. Figure 19 shows an application used for generating digitally selected regulated output voltages<sup>38</sup>. The regulator in this circuit is the 29372 low-dropout regulator. The output voltage,  $V_{out}$ , is fixed by inputs  $d_2$ ,  $d_1$ , and  $d_0$ . Small divider resistors are chosen to minimize output resistance ( $R_2 = 25\Omega$ ,  $R_1 = 6\Omega$ ). Figure 20 illustrates the ideal response of  $V_{out}$  and  $I_o$  to the four unique digital input sequences – (0,0,0), (0,0,1), (0,1,1), (1,1,1). When all of the inputs are low, the voltage output is 6.2V. One high input produces an output of 11.2V. Two high inputs generate 16.2 volts of regulated output. When all three inputs are switched high, the output is maximized at 21.2V.

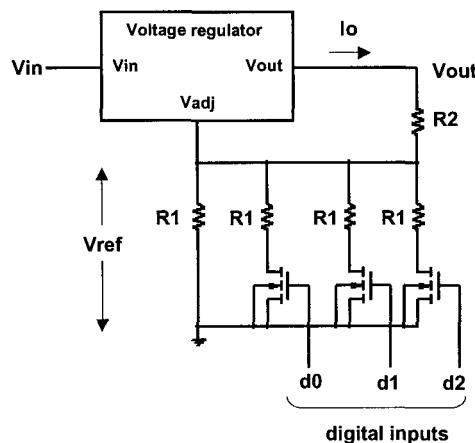


Figure 19. Voltage regulator application: a 3-bit digitally-controlled analog waveform generator<sup>38</sup>.

For this application, the output voltage can be approximated as

$$V_{out} \cong V_{ref} \frac{R1 + NR2}{R1}, \quad (6)$$

where  $V_{ref}$  ( $\approx 1.2V$ ) is the fixed reference voltage and  $N$  is related to the sum of the digital inputs states (i.e.,  $N = 1 + d_2 + d_1 + d_0$ ). Using Equation 6 and the relationship between  $V_{ref}$  and  $I_o$ , it can be shown that

$$V_{out} \leq I_o(\max) \left( \frac{R1}{N} + R2 \right). \quad (7)$$

The voltage output is therefore limited by the maximum output drive current of the regulator. The data presented in section 2C demonstrated how  $I_o(\max)$  of the 29372 low-dropout regulator degrades in response to ionizing radiation exposure. Indeed, Figure 11 shows  $I_o(\max)$  can drop as much as 90% after TID exposures of less than 40 krad(SiO<sub>2</sub>). Figure 21 illustrates the simulated effect of  $I_o(\max)$  degradation on the operation of the circuit. Figure

21a indicates that if  $I_o(\max)$  drops to 0.6 mA, the voltage set by the (1,1,1) sequence (i.e.,  $N = 4$ ) will degrade to 15.9V. As Figure 21b demonstrates, if the maximum output drive current drops to 0.2 mA, aside from the trivial condition (0,0,0), no digital input sequences generate the desired regulated outputs. These simulated responses are consistent with the Equation 7 and clearly demonstrate how deterioration in circuit specification parameters can affect specific types of regulator applications.

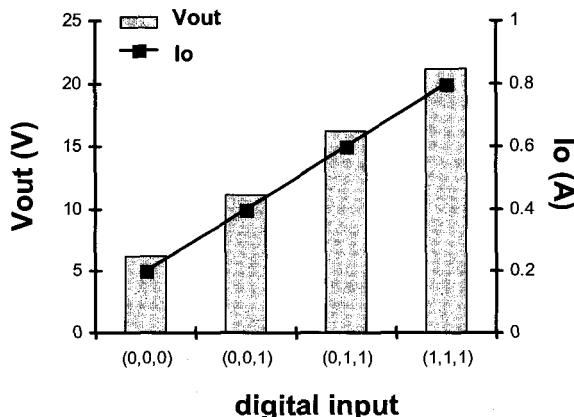


Figure 20. Simulated ideal response of  $V_{out}$  and  $I_o$  to the four unique digital input sequences.

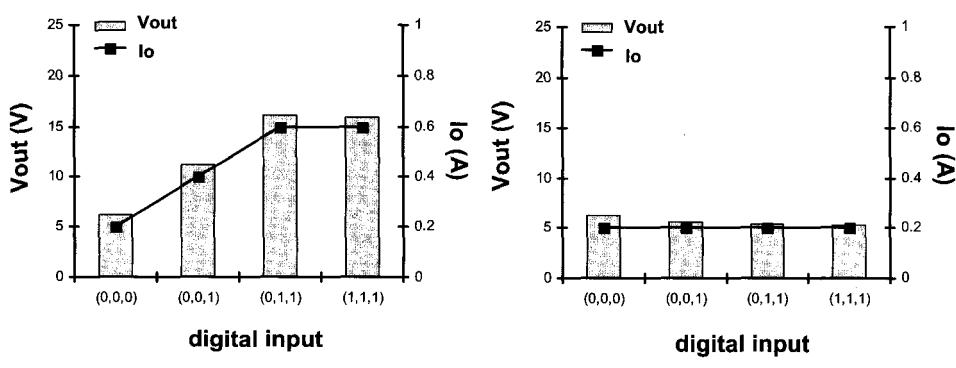


Figure 21. a) Simulated response of  $V_{out}$  and  $I_o$  to digital inputs when  $I_o(\max)$  is limited to 0.6 mA. b) Simulated response of  $V_{out}$  and  $I_o$  to digital inputs when  $I_o(\max)$  is limited to 0.2 mA.

### B. Output Voltage Drift in LM117 Voltage Regulator

Radiation experiments on a LM117 voltage regulator indicated there was significant non-monotonic drift in the output voltage ( $V_{out}$ ) in response to Co-60 irradiations at a standard laboratory dose rate of 150 rad(Si)/s. The results of these tests were originally presented in a 1996 study <sup>22</sup>. Some of the conclusions were discussed in section 2C. Through the use of

analysis techniques similar to those used in the analysis on the LM111 TID response above (section 3B), the irregular output response of the irradiated LM117 regulator was effectively reproduced by circuit simulation, as shown in Figure 22. SPICE simulation enabled researchers to identify three competing circuit-level TID mechanisms for the LM117 radiation response. All three mechanisms were associated with degradation in the four transistors of the circuit's bandgap reference. Figure 23a shows the ideal topology the LM117's bandgap voltage reference, which is a version of the Brokaw cell<sup>46</sup>. This subcircuit is composed of two lateral pnp BJTs (Q3 and Q4) which form a current mirror to drive equal currents ( $I_o$ ) through the npn transistors (Q1 and Q2).  $I_o \approx 25 \mu A$  is

$$I_o \approx \frac{\Delta V_{be}}{R_1}, \quad (8)$$

where  $\Delta V_{be}$  is the base-emitter voltage differential between Q1 and Q2. The constant, supply-independent, reference voltage ( $V_{ref} \approx 1.25V$ ) is the sum of voltage drops across the base-emitter junction of Q1 ( $V_{bel} \approx 0.65V$ ) and the resistor R2 ( $2I_oR_2 \approx 0.6V$ ). The relationship between the output voltage and  $V_{ref}$  is expressed in Equation 2.

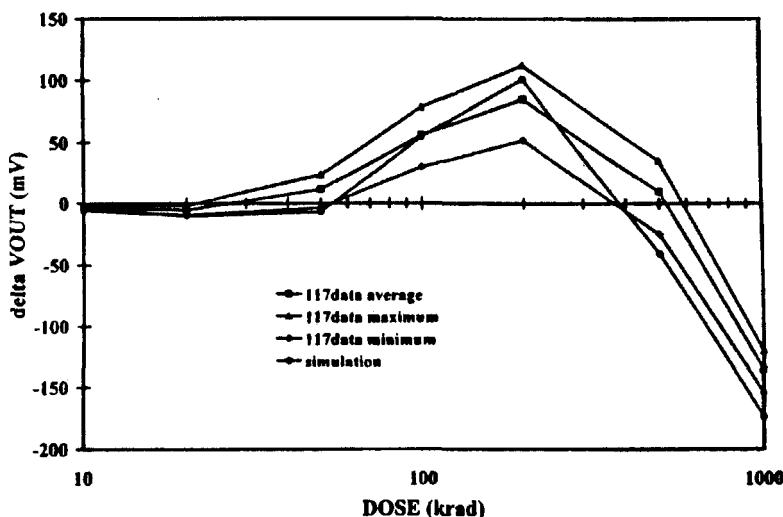


Figure 22. Increased input bias current and offset voltage in biased localized irradiations of the output stage of LM101 operational amplifiers. Data show both bias current degrades and offset voltage after 100 krad(SiO<sub>2</sub>)<sup>22</sup>.

TID degradation mechanisms for  $V_{ref}$  (and  $V_{out}$ ) were identified as: 1) collector-to-emitter leakage in the two npn devices, 2) gain degradation in the two npn devices, and 3) gain degradation in the two pnp transistors<sup>22</sup>. A brief summary of these mechanisms is as follows:

1) *Collector-to-emitter leakage (increased  $V_{out}$ ):* The increased  $V_{ref}$  (and  $V_{out}$ ) is caused by a radiation-induced channel that develops in the p-type base of Q2. The channel establishes a resistive path ( $R_{leak}$ ) between the collector-to-emitter, as shown in Figure 23b. The leakage path increases  $\Delta V_{be}$  between Q1 and Q2, thereby increasing  $I_o$ ,  $V_{ref}$ , and  $V_{out}$ <sup>22</sup>.

2) *Gain degradation in the pnp transistors (decreased  $V_{out}$ )*: Radiation-induced excess base current in transistors Q3 and Q4 reduces the collector currents of Q4 and Q1 ( $I_o - \Delta I_o$ ). This reduces both  $V_{be1}$  and the voltage drop across R2, causing the  $V_{ref}$  and  $V_{out}$  to decrease with TID exposure<sup>22</sup>.

3) *Gain degradation in the npn transistors (decreased  $V_{out}$ )*: Simulations indicate that  $I_o$  remains unchanged with radiation-induced gain degradation in transistors Q1 and Q2. However, gain degradation does cause a reduction in  $V_{be1}$ . Moreover, because of the differences in emitter geometries, the emitter current of Q1 drops relative to Q2. The combined decrease in  $V_{be1}$  and voltage drop across R1 (reduced emitter current of Q1) causes  $V_{ref}$  and  $V_{out}$  to decrease<sup>22</sup>.

The combined effects of these three circuit-level mechanisms cause the highly nonlinear response in the output characteristics of the LM117 voltage regulator. Through detailed hand analysis, supported by SPICE simulations, each mechanism and its effect on the circuit response can be characterized independently. This type of analysis can provide insight into potential low-cost hardening techniques for future linear integrated circuit designs.

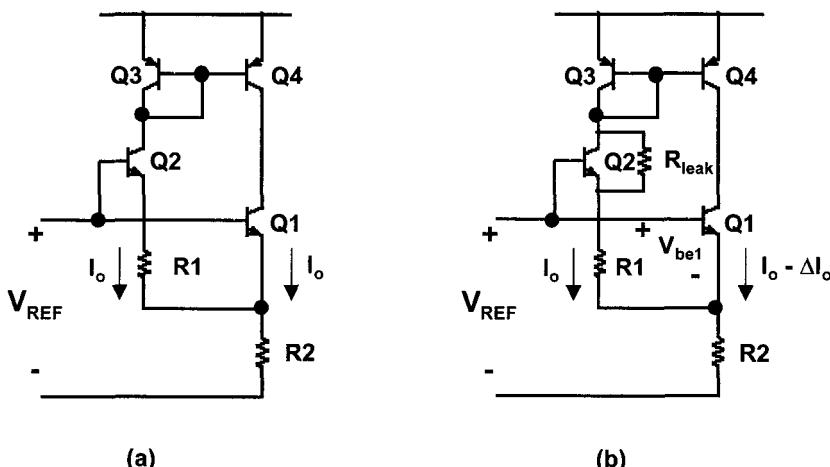


Figure 23. a) Ideal topology of Brokaw cell band-gap regulator<sup>46</sup> and b) the effects of radiation-induced gain degradation on band-gap regulator, i.e., collector-to-emitter leakage path and changes to  $V_{BE1}$  and  $\Delta I_o$ <sup>22</sup>.

## 5. Conclusions

This paper presents a comprehensive overview of TID effects in bipolar linear integrated circuits. However, unlike many studies in this field that focus primarily on basic TID mechanisms at either the process or transistor level, this text discusses the effects of TID from the circuit perspective, particularly the effects of transistor gain degradation on specific circuit parameters and the effects of circuit parameter degradation on select linear bipolar circuit applications.

Of course, it would be impossible to discuss and analyze on how TID exposure affects all

linear bipolar circuits and their applications. Readers interested in obtaining more data on this topic should consult recently compiled compendiums of total dose effects on bipolar linear circuits found in references<sup>43, 47</sup>. The data and analysis shown in this text is provided to give a perspective on how systems are threatened by ionizing radiation if they utilize linear bipolar circuits to perform critical subsystem functions such as signal amplification, voltage regulation, and mixed signal processing. It should be noted that the author is by no means recommending bipolar linear parts be avoided when designing systems that operate in radiation environments; nevertheless, system designers must be aware of the hazards, especially those hazards that may be difficult to measure effectively, such as the enhanced sensitivity of circuit parameters to radiation exposures at low-dose-rates.

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## HARDNESS ASSURANCE FOR COMMERCIAL MICROELECTRONICS

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An approach to hardness assurance for commercial microelectronics is presented based on hardness assurance guidelines developed by the US Department of Defense in the late 1970s and early 1980s. Modifications are made to accommodate commercial variability in radiation response and frequent changes in design and process.

**Keywords:** radiation hardness assurance, radiation testing, total dose, displacement damage, single event effects, dose rate response, latchup, neutrons, heavy ions, protons

### 1. Introduction

Many electronic systems must operate either in the presence of a radiation environment or with the possible threat of a radiation environment. Examples of systems operating in the presence of radiation include spacecraft, high altitude avionics, nuclear power plant instrumentation, high-energy particle accelerator detectors, and nuclear waste management robotics. Many military systems must be prepared for the threat of nuclear weapon induced radiation, even though they may not otherwise be exposed to radiation. Earth satellites, including both commercial and military, are exposed to the natural space radiation environment and face the threat of radiation from high altitude or space based nuclear weapon detonations. For all of these systems some form of radiation hardening will normally be performed in the system design phase. This hardening may take the form of system level techniques such as shielding or using un-powered spares for ionizing radiation, the use of terminal protection devices for electromagnetic pulse mitigation, error detection and correction or triple modular redundancy for single event upset, and power supply re-cycling for dose rate induced latchup protection. However, one of the primary approaches to radiation design hardening is electronic piece-part selection. In the past the US military invested a significant amount of funding to develop microelectronic parts that were able to withstand high levels of radiation. Hence the piece-part selection for many hardened systems included a high number of radiation-hardened parts. While investment in radiation hardened microelectronic technology continues, although at a much lower level than in the past, many of the radiation hard parts that were developed in the past are no longer available. Many former suppliers of radiation hardened microelectronic parts have ceased production of hard parts because the demand is low and much greater profits can be made in the commercial markets. In addition the state-of-the-art of radiation-hardened parts is usually several generations behind the

commercial state-of-the-art and many systems demand a better, faster, cheaper approach. This has lead, by necessity, to the widespread use of commercial microelectronics in systems that have radiation requirements.

Hardness assurance includes those activities required to guarantee that the hardened system design will remain hard in *production* and that fielded systems will be able to withstand the radiation environments that they were designed to meet. In a general sense hardness assurance covers all activities at the system level, sub-system level, board level and piece-part level to maintain all elements of the hardened design. However, since the topic of this paper is hardness assurance of commercial microelectronics, only piece-part hardness assurance will be considered herein.

In the mid 1970s the US Defense Nuclear Agency (now known as the Defense Threat Reduction Agency, DTRA) began a program to develop all of the documentation necessary to support piece-part hardness assurance, HA. The group responsible for carrying out this effort is the Space Parts Working Group (SPWG) Hardness Assurance Committee (HAC). This group was comprised of representatives from the Department of Defense, DoD, and the National Aeronautical and Space Agency, NASA, and their contractors. Electrical test methods and dosimetry standards were developed through the American Society for Testing and Materials, ASTM, and most radiation environment test methods and hardness assurance guidelines were developed as military standards and handbooks. The first 10 years of this effort is described in a summary review paper.<sup>1</sup> The following definition was adopted by the working group: "Piece-part hardness assurance consists of the procedures, controls, and tests used to insure that a purchased piece-part has a response to nuclear-induced stresses that is within known and acceptable limits."<sup>1</sup> If we eliminate the word "controls" and substitute the word radiation for "nuclear" the definition applies to commercial microelectronics today. While the focus of the DNA funded piece-part HA program was on mature hardened technologies, the methodology developed is generic and applies to any microelectronic piece-parts, whether commercial, radiation tolerant, or radiation hard, as we will attempt to demonstrate.

## **2. Piece-part HA Methodology Overview**

The general approach to piece-part HA is illustrated in the flow diagram of Fig. 1 taken from reference 2. The starting point for the piece-part HA program is part categorization shown in the center of the figure.

Each microelectronic part in the system is categorized in one of four categories based on its application, radiation requirements, radiation response data and assigned probability of survival and confidence level. The four categories are as follows:

- (i) Not acceptable- corrective action required,
- (ii) Hardness Critical Category 1 (HCC-1)- radiation lot acceptance testing required on every lot,
- (iii) Hardness Critical Category 2 (HCC-2)- radiation sample testing required on a periodic basis,
- (iv) Hardness Non-Critical (HNC)- no further radiation testing required.

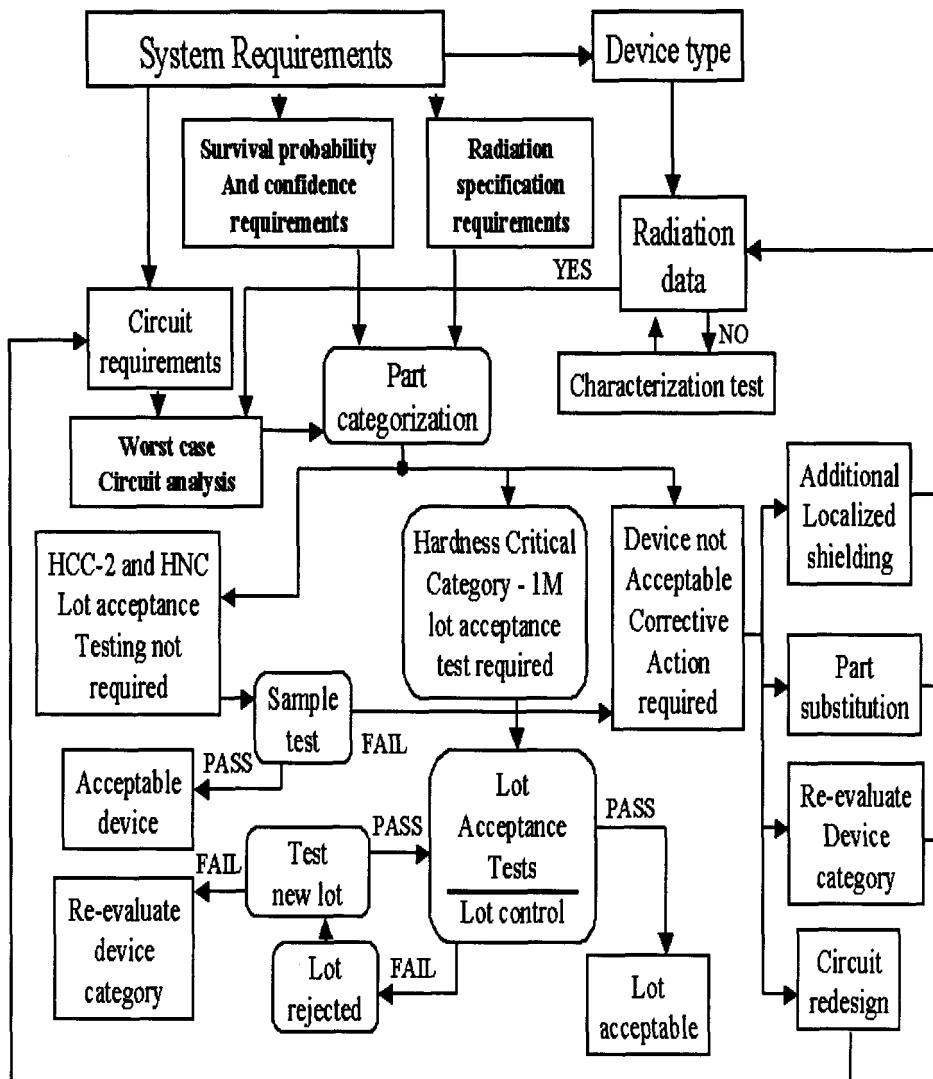


Fig. 1. Piece-part hardness assurance flow diagram from reference 2.

The method used to determine the category for each part in each application is based on the concept of radiation design margin. The radiation design margin, RDM, is defined as the mean of the radiation failure level,  $R_{mf}$ , divided by the radiation specification,  $R_{spec}$ , for the part.

The first issue to address is the determination of  $R_{mf}$ . There are three types of failures in microelectronic parts, parametric, functional and catastrophic. Catastrophic failure (permanent damage) can occur for some devices in the form of, for example, heavy ion or proton induced gate oxide rupture or latchup induced burnout. For these cases the failure definition is obvious. For parametric or functional failure, the failure definition depends on the application of the part, its criticality to the system mission and the radiation environment. For some radiation environments, such as long-term ionizing radiation effects (total dose) and displacement damage, electrical parameters usually degrade monotonically with increasing radiation dose or fluence. Failure is defined as an unacceptable change in a parameter critical for system operation. Functional failure can also occur in microcircuits from total dose or displacement damage when the internal parameter degradation prevents proper circuit operation. This is usually more of an issue for digital circuits rather than linear or mixed-signal circuits. For other environments, such as transient ionization (dose rate) or single event effects (SEE) from protons or heavy ions, there is usually functional failure (upset or latchup) but very little parametric degradation. Again, failure must be defined by the application of the part for each radiation environment based on an evaluation by the system designer to identify critical electrical parameters and allowed changes as well as the criticality of the part. A failure definition is required for each part in each application for each environment.

Once a failure definition is established a mean failure level can be determined based on one of several methods, including electrical screens, model based predictions or sample radiation testing. *In most cases the preferred method will be sample radiation testing.*

The most desirable method of determining the radiation failure level of a part would be based on a pre-irradiation electrical parameter value. However there are only a few cases where a reliable correlation exists between the radiation failure level and the value of a pre-irradiation electrical parameter, and those are for discrete devices and not microcircuits. For example a semi-empirical relation exists between the unity gain cutoff frequency of a bipolar transistor and the neutron induced degradation of current gain.<sup>3</sup> Another example is the correlation between pre-irradiation 1/f noise and channel resistance and the radiation induced increase in oxide trapped charge and interface traps, respectively, for total dose effects in MOSFETs.<sup>4</sup> However, for the vast majority of part types and radiation environments, no correlation has been found between pre-irradiation parameter values and radiation failure levels.

The prediction of radiation failure levels, based on radiation response models, is possible in some cases but it requires detailed information about the process flow and the circuit design and layout. For commercial microelectronic parts this information is seldom available, hence this approach is not considered viable if the RDM is to be known within, say, a factor of two for RDMs below 10. However, prediction of failure levels may be acceptable in cases where the RDMs are quite large and prediction is based on the knowledge of the process technology, the failure mechanisms and an historical set of data. Examples are displacement damage in CMOS circuits for non-ionization energy loss (NIEL) equivalent neutron fluence below  $10^{13} \text{ n}(1 \text{ MeV eq.})/\text{cm}^2$ , latchup in silicon-

on-insulator (SOI) parts, and single event transients in bipolar linear circuits from protons or neutrons below 20 MeV. In these and other cases, prediction can be used to put part types in the HNC category.

The most reliable method of determining the mean failure level is based on sample radiation data. There are a number of radiation effects databases that have been compiled and are available to the public, including the DTRA supported Electronics Radiation Response Information Center (ERRIC) database (<http://erric.dasiac.com>), the NASA Jet Propulsion Lab (JPL) database (<http://radnet.jpl.nasa.gov>) and the NASA Goddard Space Flight Center (GFSC) database (<http://radhome.gsfc.nasa.gov>). Most of the data in the ERRIC database are on neutron and total dose effects and most of the data in the NASA databases are on total dose and SEE. Other sources include system contractor and/or government test reports and the IEEE Radiation Effects Data Workshop Record that includes workshop papers from the annual IEEE Nuclear and Space Radiation Effects Conference held in July. While published data exist on many commercial part types one has to be very careful using the data for the following reasons:

- (i) Many of the data are on older date code parts and may not be applicable to parts manufactured today,
- (ii) Sample sizes are often quite small,
- (iii) The test parameters may not be the ones that are critical for the application being evaluated,
- (iv) The test conditions (bias and load) may not be worst case for the intended application.

The use of database data for commercial parts is especially risky since process, circuit design and layout may change frequently (and without notice), which may affect the radiation response. If data are not available or are insufficient for one of the above reasons, then sample radiation tests must be run to determine the mean failure level.

### **3. Radiation Testing to Determine $R_{mf}$**

To provide the radiation test data for the purpose of categorization the data should be taken to best simulate operating conditions and radiation environments that will be encountered in the system application. This can often be a challenge since the part may have many applications and may see extremes of operating biases, frequencies and temperatures. For this reason testing is usually done for a worst-case application, which is often different for different environments and sometimes even for different parameters for the same environment. For example, if a part is being tested for heavy ion SEE, the worst case bias for upset may be at the minimum supply voltage whereas for latchup it is the maximum supply voltage and operating temperature. The full range of applications and operating conditions should be considered when designing the radiation test.

The radiation environments encountered by the system can vary widely in particle type, energy, flux and fluence. For example in an earth orbit a satellite may encounter trapped protons and electrons in the Van Allen belts, heavy ions and high-energy photons from cosmic radiation and high fluxes of protons from solar flares. Instead of trying to accurately simulate each of these radiation environments, radiation testing is performed

to measure the response of the microelectronic parts to different types of *effects*. These effects are associated with a characteristic of the environment. For total dose the effect is proportional to the ionization energy loss in the material measured in rads, where 1 rad is defined as 100 ergs/gm material. For commercial microelectronics the material of concern is usually silicon dioxide, so the measurement is rad(SiO<sub>2</sub>). For transient ionization the effects are proportional to the dose rate measured in rad(Si)/s. For displacement damage from protons and electrons the effects on the part are proportional to the non-ionization energy loss or NIEL.<sup>5</sup> For SEE from heavy ions the important factor is the linear energy transfer or LET, measured in MeV-cm<sup>2</sup>/mg or pC/ $\mu$ m. However, for proton induced SEE the important factor is the proton energy. Using these concepts, based on years of research in the radiation effects community, the testing can be performed using radiation sources that are not identical to the actual environment but can produce the desired *effect*. For example, total dose effects are usually simulated in the laboratory using Co-60 or Cs-137 photons rather than electrons or protons (the main source of ionization damage in space). While electrons and protons of the appropriate energies are available from various types of accelerators in the laboratory, it is much cheaper and easier to use Co-60 sources. ASTM standards address the measurement of the absorbed dose from Co-60 irradiation in rad(SiO<sub>2</sub>).<sup>6,7</sup> Transport codes are available to calculate the absorbed dose in SiO<sub>2</sub> from the space environment.<sup>8</sup> While there is commonality for ionizing radiation between the space and laboratory environment through the measure of absorbed dose, a problem arises with respect to the flux or dose rate. As shown in Fig. 2,<sup>9</sup> in space the *average* dose rate can vary between about 10<sup>-3</sup> rad/s to less than 10<sup>-4</sup> rad/s whereas typical laboratory dose rate are orders of magnitude higher. The instantaneous dose rate in space varies from about 1 rad/s to near zero. The default dose rate for the US military test standard is 50-300 rad/s whereas in the European standard there are two ranges of dose rate, 2-10 and 0.1 to 0.01 rad/s. There are two issues that must be addressed because of differences in the response of microcircuits at different dose rates. One is labeled "time dependent effect" and the other "true dose rate effect". Time dependent effects refer to those processes that occur following irradiation, e.g. annealing or compensation of trapped charge and buildup of interface traps. True dose rate effects occur in thick oxides at low electric field and are thought to be a result of space charge in the oxide that builds up at high dose rate but not at low dose rate.<sup>10,11</sup> True dose rate effects are a problem for many bipolar linear circuits.<sup>12</sup> Time dependent effects are treated with a post irradiation elevated temperature anneal (incorporated in the test standard for CMOS parts used in space)<sup>13,14</sup> and true dose rate effects are treated either with a sufficiently low dose rate irradiation (undesirable for high specification doses) or with an elevated temperature irradiation.<sup>15,16</sup> In March 2003 the US military standard test method for total dose testing was revised to include low dose rate or elevated temperature irradiation tests for bipolar linear and mixed-signal parts.<sup>14</sup>

While Co-60 does a good job of simulating the ionization effects of electrons and protons, it does not simulate displacement damage effects. Another radiation source is required to simulate the displacement damage, such as neutrons from a nuclear reactor. However, if the ionization and displacement damage effects of protons are to be

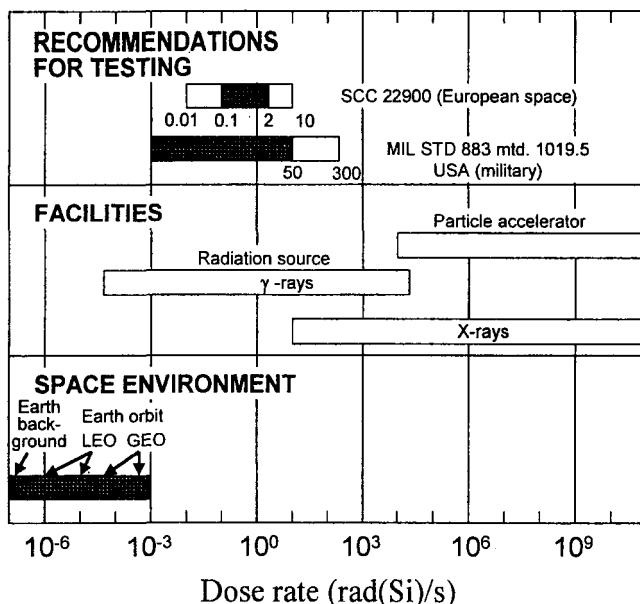


Fig. 2. Typical dose rates in space compared to laboratory facilities and test standards.<sup>9</sup> (© 2002 IEEE)

simulated in the laboratory using a combination of Co-60 and neutrons then the irradiations have to be performed consecutively on the same samples since the effects are interactive and not simply additive.<sup>17</sup> When neutrons are used as an irradiation source for displacement damage and compared to other forms of irradiation through the common factor NIEL, the neutron fluence must be expressed in the form of 1 MeV equivalent silicon damage fluence. This is done by integrating the differential neutron fluence as a function of neutron energy with the silicon cross section for displacement damage as a function of neutron energy. Using this notation the space particle environment (electrons, protons and heavy ions) can be expressed as a 1 MeV eq neutron flux or fluence through the calculation of NIEL. Displacement damage from space radiation affects primarily silicon solar cells, bipolar linear devices and circuits and opto-electronics.

Laboratory tests to simulate single event effects in space are performed on the basis of LET for heavy ions and proton energy for protons. Although LET is the primary factor relating SEE in space to the laboratory it is not the only factor. In space the heavy ions are very energetic, having energies that range up to several GeV per nucleon. At these energies the particles can penetrate the skin of the spacecraft, the microcircuit package and the entire chip. In the laboratory the accelerators used for heavy ion testing are either in the range of 1-10 MeV/nucleon or 10-100 MeV/ nucleon. For the high LET particles, even with the package lids removed the ions may only penetrate the top few microns of the chip. While this can be a problem for some circuits, e.g. bipolar linear circuit and power MOSFETs, the lower energy ions are adequate for simulating the effects of the higher energy space particles for many circuit types.<sup>18</sup>

Proton energies in space can range up to a few hundred MeV. These energies are easily simulated with laboratory accelerators. Attempts have been made to establish

correlation between proton induced SEE and heavy ion induced SEE so that data taken in one environment can be used to imply microcircuit response in the other environment.<sup>19</sup> However, while this may work for some circuit types it is not universal.<sup>20</sup>

For the transient ionization (dose rate) environment, encountered primarily for a nuclear weapon event, the response (upset, latchup and/or burnout) is both a function of the dose rate and the pulse width. Hence the mean failure level is usually determined for both a very short pulse width, say, 10-20 ns, to cover the short pulse high dose rate regime and a wide pulse, say a few  $\mu$ s, to cover the equilibrium, wide pulse regime. The short pulse response can be measured using a flash x-ray machine or an electron linear accelerator (LINAC) while the wide pulse response usually requires a LINAC.

While we have discussed the issues with performing laboratory radiation tests to simulate the response to actual radiation environments, we have not discussed the requirements for part selection and sampling. This is a very important aspect of the categorization process that is often ignored. The test samples must be representative of the parts that will actually be used in the fielded systems. This is especially important if the parts are to be considered HNC since these parts will not be tested any further and system contractors are motivated to get as many parts in this category as possible, because of the cost savings. Because of the wide range of radiation responses that can be expected from the same part type from different manufacturers, each vendor's part must be considered a different part type. Also because the radiation response may change when the design, layout or process is modified, and there are no controls on these factors for a commercial part, samples must be drawn from multiple lots over a period of time. If this is not possible then lot sample testing must be performed and the part must be categorized as HCC-1. Sample sizes per lot should be a minimum of 5-10. This will be discussed in more detail in a later section.

#### 4. Determination of $R_{\text{spec}}$

Since we are interested in establishing a value of RDM for each part we also must determine the radiation environment that each part will see during the mission. The radiation environment can vary widely within a system depending on how much material there is between the microcircuit chip and the radiation source. In the case of a spacecraft parts that are buried in the center of an electronic sub-system may get considerably less dose than a solar cell that is placed outside the spacecraft. Although the radiation environment should be determined for each application of each part type, a conservative approach is usually taken initially by assuming the radiation environment is the free field environment. The only problem with this assumption is that for some cases the radiation environment at the part may actually exceed the free field environment because of dose enhancement.<sup>21</sup> This problem is usually ignored since there are a number of built-in safety factors in the failure definition, the "worst case" radiation test conditions and the categorization criteria. If the part is found to be unacceptable because of the value of RDM based on a free field calculation of the environments then the environment is transported through the spacecraft material to the part location to get a better estimate of the environment. As discussed in the previous section the radiation environment must be

represented using the same factors that are used in the testing. For the space environment the total dose is represented by rads (dose) and rad/s (dose rate), the heavy ion environment by the LET fluence, and the displacement damage by the 1 MeV eq. neutron fluence. The proton environment is usually expressed as a proton flux or fluence vs. proton energy. Codes are available both for estimating various components of the space radiation environment for given missions and for transporting the environments through various densities and thicknesses of materials.<sup>8</sup>

## 5. Categorization

As mentioned previously there are four HA categories for microelectronic parts, unacceptable, HCC-1, HCC-2 and HNC. There are two methods for determining what category a part is placed in based on RDM.

### 5.1 Design margin breakpoint method

The first method was developed for systems with moderate radiation requirements and has been applied by the military mostly for manned systems. It has been named the design margin breakpoint (DMBP) method and is based on historic radiation data for older parts with many part types lumped together for each radiation environment. This DMBP method is shown in Fig. 3. The breakpoints in this method are very conservative and for commercial microelectronic parts would probably be considered unrealistic.

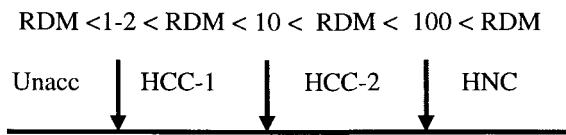


Fig. 3. HA categories using DMBP method.

For example using this method, if one wanted to avoid performing any further testing for total dose for a mission with a 20 krad specification (typical of many NASA missions), a part would have to demonstrate an average failure dose of 2 Mrad. Even periodic testing would be required for parts with an average failure dose of 200 krad. The breakpoint between unacceptable and HCC-1 is given as 1-2. If RDM equals 1 then half of the population would fail at the specification level. This is clearly unacceptable. However, if RDM equals 2 then a large % of the population may pass the specification level depending on the statistical distribution. While the DMBP method may be useful for certain military systems using radiation tolerant or hard parts, it is not recommended for systems using a large percentage of commercial parts.

### 5.2 Part categorization criteria method

The second method for categorization is based on the statistical distribution of the radiation failure levels and is called the Part Categorization Criteria (PCC) method. The breakpoints for this method are shown in Fig. 4.

RDM < 1-2 < RDM < PCC1 < RDM < PCC2 < RDM



Fig. 4. HA categories using PCC method.

The application of this method requires knowledge of the distribution of radiation failure levels. This issue has been addressed for many part types in many environments and there is no general consensus about the nature of the distribution. Several parametric distributions, such as normal, lognormal and Weibull have been investigated as well as a non-parametric distribution. While it is not universal, the lognormal distribution is usually assumed. The lognormal distribution is favored because the values are always positive, it is easy to work with and it fits reasonably well for many part types in many environments. Assuming a lognormal distribution the geometric mean,  $R_{mf} = \exp\{\text{ave}[\ln(R_{fail})]\}$ , and standard deviation,  $s[\ln(R_{fail})]$ , are calculated for each set of test samples from the natural logarithms of the radiation failure levels,  $R_{fail}$ . The PCC is then calculated from the following relation:

$$\text{PCC} = \exp\{K_{TL} * s[\ln(R_{fail})]\}.$$

Assuming that PCC1 is just equal to PCC in the above equation, if  $\text{RDM} < \text{PCC1}$  then the part is category HCC-1.  $K_{TL}$  is the one-sided tolerance limit factor and is a function of the sample size,  $n$ , the probability of survival,  $P_s$ , and the confidence level,  $C$ . Plots of  $K_{TL}$  vs. sample size for various values of  $P_s$  are shown in Fig. 5 for a confidence level of 0.90 (90%), which is the usual specified value of  $C$ .

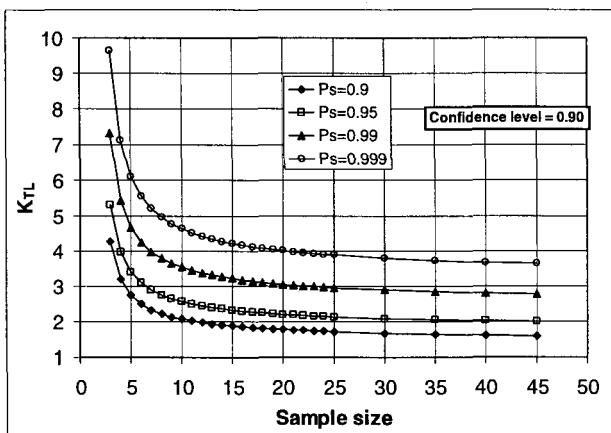


Fig. 5.  $K_{TL}$  vs. sample size for various values of  $P_s$  for  $C = 0.90$ .

Many space systems require a high level of survival probability since a part failure can mean the failure of the mission and repair and/or replacement is usually not an

option. If we require, for example, a  $P_S$  of 0.999 with a C of 0.9, then for a sample size of 15 (5 each from three lots)  $K_{TL}$  is about 4.2. This means that for the part to avoid lot sample testing the average failure level minus 4.2 standard deviations must be greater than the specification radiation level.

The decision as to whether periodic sample testing or no further testing is to be performed is based on what we have called PCC2. If a part has a sufficient RDM then, in principle, lot acceptance is not required. Under the categorization system developed for mature parts, the assumption is that in those cases where many lots of a part type will be purchased over a long period of time, some parts should be periodically checked to assure that the RDM and standard deviation of the failure levels is maintained. It is unlikely that this approach will be workable for commercial part types since most commercial parts would not be considered mature in the sense of long-term stability without changes in process or design. Therefore for commercial parts the HCC-2 category can be eliminated and a safety margin can be used to establish the breakpoint between HCC-1 and HNC. The system program office should do the assignment of the breakpoint. However a reasonable number would be 2PCC1 as the breakpoint between HCC-1 and HNC. Another approach might be to increase the  $P_S$  requirement. For example, if the system required a  $P_S$  of 0.999, then the breakpoint between HCC-1 and HNC could be set using a PCC calculated for a  $P_S$  of 0.9999.

The breakpoint between HCC-1 and unacceptable was addressed for the DMBP method. With the PCC method this breakpoint is the same. The actual value of this breakpoint will be set by the system HA engineers and will usually be determined by how much risk they are willing to take in rejecting lots. For those parts that are found to be unacceptable there are several options, as shown in Fig. 1. One may add shielding to reduce the radiation environment at the part level or, if free field environments were used, perform a calculation of the actual environment at the part location. This may lower the value of  $R_{spec}$ . One may perform additional radiation testing if the original sample sizes were too low. One may also re-evaluate the application of the part to see if the failure definition is realistic or too conservative or if a design change can relax the failure definition. If none of these approaches result in the part being re-categorized as acceptable, then the part must be replaced with one that is acceptable. In summary, for commercial parts the PCC method should be used. The PCC-2 category should be eliminated and the breakpoint between HCC-1 and HNC should be set somewhat higher than PCC1.

## 6. Lot Acceptance Testing

For all of those parts that are category HCC-1 radiation lot sample testing must be performed on each lot. The first issue that must be addressed is the definition of a lot. As a minimum for commercial parts the lot is defined as a date code lot, i.e. all parts assembled in the same week. While this may include parts from more than one process lot, if the test samples are chosen randomly, and the sample size is sufficient, then the probability is good that parts from all the process lots will be represented in the test sample. It is much better to define a lot as a process or wafer lot where possible. For

example, if parts are purchased in die form, because of special packaging requirements, they can usually be purchased from a single process or wafer lot. The lot sample test approach can take two forms, a test by attributes or a variables data test.

### 6.1 Test by attributes

The test by attributes is also known as a go/no-go test. In this type of test the test samples are randomly selected from the lot and subjected to the radiation test at the specification level. Based on the failure criteria (parametric or functional) an accept/reject (go/no-go) decision is made for each sample. This test requires a very large sample size to establish a high  $P_S$ . As an example for a sample size of 11 and an accept number of zero (no failures), the lot tolerance percent defective, LTPD, would be 20, corresponding to a  $P_S$  of only 0.80, for a confidence level of 0.9. To achieve a  $P_S$  of 0.999 (LTPD of 0.1), as in our earlier example, a sample of 2303 with no failures would be required. To overcome this problem of high sample size, which is clearly unacceptable, overtesting may be used.<sup>22</sup> An overtest is a test at a higher level than the specification level where the overtest factor is the ratio of the test level ( $R_{test}$ ) to the specification level. Procedures have been developed for calculating an overtest factor based on sample size, accept number,  $P_S$  and C. However, to apply this approach one must make an estimate of the *maximum* standard deviation of the radiation failure levels for the part type and environment. For a lognormal distribution the maximum standard deviation is calculated from the logarithms of the radiation failure levels,  $\sigma[\ln(\max)]$ . For purposes of illustration let us assume that  $\sigma[\ln(\max)]$  is 0.5. Table 1 is a list of the overtest factors that would be required for  $P_S = 0.999$  and  $C = 0.9$  as a function of sample size for zero failures.

Table 1. Overtest factors vs. sample size

Sample size (n)	Overtest factor ( $R_{test}/R_{spec}$ )
5	3.97
10	3.11
11	3.02
15	2.75
20	2.53

For our example of a test to the specification level, we see that an overtest of 11 parts at roughly three times the specification level will give us the same  $P_S$  and C as a test of 2303 samples at the specification level (assuming  $\sigma[\ln(\max)] = 0.5$ ).

### 6.2 Test by variables data

The variables data test method is the same approach that we discussed for categorization using the PCC method. One usually assumes a lognormal distribution of radiation failure levels and calculates a geometric mean and standard deviation. If  $\exp\{\text{ave}[\ln(R_{fail})] - K_{TL} * s[\ln(R_{fail})]\}$  is greater than the specification level then the lot passes, otherwise it fails.

There are a number of cases where this seemingly straightforward approach does not work well. For example the test approach most often used to determine a failure level in environments such as total dose and displacement damage is called the step-stress approach. In the step-stress approach the parts are taken to discrete radiation levels and are measured to determine parametric change or functional failure. If the parts pass at one level and fail functionally at the next higher level some means of interpolating the failure level must be established. If some parts fail at the first level and others pass at the highest level then one must extrapolate to a failure level, which entails a considerable risk of error. Methods have been developed to handle these situations<sup>23,24</sup> but additional tests should be run to completely bound the failure levels for all samples. Another approach that may be used in the case of parametric failures is to base the accept/reject criterion on parametric changes at a fixed radiation level, either at the specification level or higher. This approach is valid only if the variation of the parameter with the radiation environment is linear. If the response is sub-linear then the results will be conservative. However, if the response is super-linear, as is the case with abrupt failures, then the approach is non-conservative and should not be used. Another class of exceptions is where the maximum level that can be reached by the laboratory radiation source is insufficient to cause failure in any of the test samples. In this case the overtest method should be used and a value of  $\sigma[\ln(\max)]$  must be assumed.

### 6.3 An example

An example is provided to illustrate the procedure in performing a lot acceptance test based on the variables data method. This example is taken from real data from a semiconductor manufacturer. The part type is a commercial LM117 adjustable voltage regulator, which is used in many space systems. The critical parameter that determines the failure criterion is the reference voltage,  $V_{ref}$ , with a nominal value of 1.25V. The failure definition will be taken as  $V_{ref}$  dropping below the minimum specification value of 1.2V. The worst-case bias for this part is for dc operation with a maximum input voltage. A sample of 18 parts from the same wafer lot (6 each from three different wafers) is irradiated in a step-stress test and the value of  $V_{ref}$  is measured at 3, 10, 30 and 50 krad. Let us assume the specification dose for this part is 7 krad and a  $P_S$  of 0.99 is required at a confidence level of 90%. Figure 6 is a plot of  $V_{ref}$  vs. dose for the 18 samples with the scale expanded to show the behavior near the failure level of 1.2V (1200 mV).

The failure doses are interpolated graphically from the lines crossing 1200 mV. A plot of the inverse cumulative probability distribution of the  $\ln(\text{failure dose})$  is given in Fig. 7 for the 18 samples. This function (inverse cumulative distribution) has a mean of zero and a standard deviation of 1, as shown in the plot.

If the distribution is lognormal then the data will fall on a straight line when plotted as  $\ln(\text{failure dose})$ . We can see from Fig. 7 that the assumption of lognormal is reasonable. For a  $P_S$  of 0.99 and confidence of 0.9 the  $K_{TL}$  is 3.1. The geometric mean failure dose is found to be 9.3 (10.9 krad) and the standard deviation 0.18. The value of  $\exp\{\text{ave}[\ln(R_{fail})] - K_{TL} * s[\ln(R_{fail})]\}$  is 6.15 krad so the lot fails the 7 krad requirement.

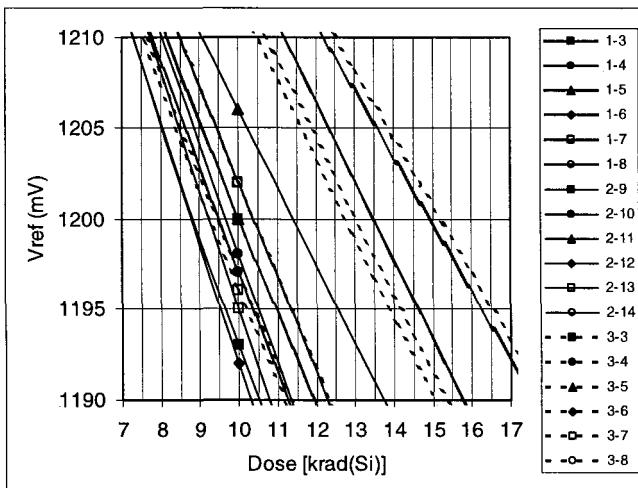
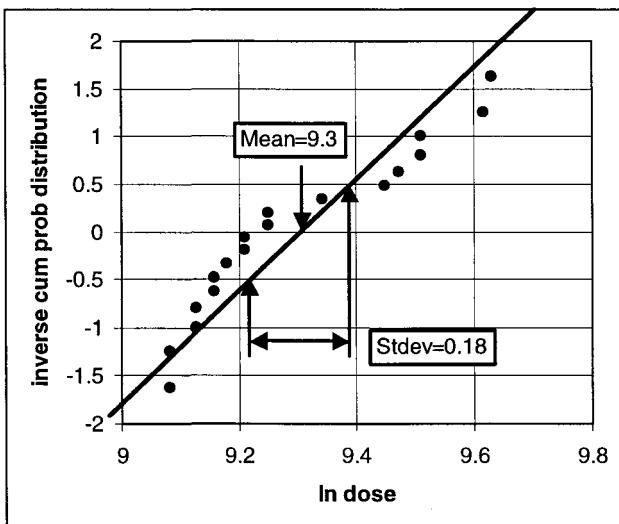


Fig. 6. Vref vs. dose for LM117 adjustable voltage regulator.

Fig. 7. Inverse normal cumulative distribution vs.  $\ln$  failure dose for 18 samples of an LM117 voltage regulator.

#### 6.4 Radiation screens

Radiation screens (100% radiation tests) have been used as a substitute for lot acceptance testing in some cases. For a radiation screen to be acceptable it must be repeatable and non-destructive since the irradiated parts will be used in the flight hardware. An attempt to develop a screen for total dose was only partially successful.<sup>25</sup> Two approaches were tried: 1) irradiate to a low dose to engender a measurable parameter change and extrapolate to a parametric failure level, and 2) irradiate to the specification dose,

determine if the part passes or fails, and if it passes, anneal out the degradation at elevated temperature. Since total dose degradation is often very non-linear the extrapolation technique did not work for many parts. Also because the anneal temperature must be restricted for reliability reasons, the irradiate-and-anneal method was not successful. One case where radiation screens have been successful is for dose rate induced latchup. All parts are given a dose rate pulse of radiation to a specified dose and if they latch-up they are eliminated from the lot. This approach has been used on several military systems. Of course in those cases where radiation screens are employed, the sample lot acceptance test does not apply since an accept/reject decision is made on every sample on the basis of the screen test.

## **7. Modifications to the HA Methodology to Accommodate Commercial Parts**

While the original US military developed piece-part hardness assurance methodology was designed to address mature radiation tolerant/radiation hard parts, the HA approach is generic and does not require extensive modification to apply to commercial parts. The concept of categorization based on RDM should apply to any electronic piece-part and any type of system with radiation requirements. However some of the details require modification in dealing with commercial parts, which do not have controls over processes, circuit designs and layouts that may affect radiation response. For this reason data in databanks are unlikely to meet the criteria for being representative of the lot(s) that will be used in fielded systems. If it can be determined that the databank data are from lots that are manufactured with the same process, circuit design and layout as those that will be purchased for system use then they may be used if they meet the additional criteria of using appropriate test conditions, electrical measurements and sample sizes. If not then characterization data will have to be taken on samples that are representative of lots that will be used in fielded systems. For those cases where there is a lifetime buy of the parts, including tests samples, system hardware and replacement parts (if required) all from the same lot, then the characterization test becomes, by default, the lot acceptance test. In this case there are only two categories, acceptable or not acceptable.

The other modification for commercial parts would be in the method for categorization. The DMBP method is not recommended even with a change in the breakpoints, since there is insufficient historical radiation data on commercial parts to support generic breakpoints. The PCC method should be used with the elimination of HCC-2 and a re-definition of the breakpoint between HCC-1 and HNC. The category of HCC-2 has always been a gray area with somewhat imprecise definitions for the breakpoints between HCC-1 and HCC-2 as well as HCC-2 and HNC. It makes some sense when a product will be on the market for many years and a long life system will be using the part in relatively high volume for many lots and many years. However, such a case will probably never occur for commercial parts. Even the CMOS digital small scale ICs and the bipolar linear circuits that have been available for many years undergo die shrinks and process modifications that change radiation response. Therefore, for commercial microelectronics only three categories are required with a modification to the breakpoint between HCC-1 and HNC as suggested above.

While it may seem difficult to get commercial parts into the HNC category, there are many microcircuit technologies in many radiation environments that can be placed in the HNC category based on an understanding of mechanisms, modeling/analysis or historical data. Some examples were given in section II. There are many other cases where it is reasonable to place certain parts in the HNC category based on the radiation level, the failure definition or the criticality of their use in the system.

Many commercial parts, e.g. linear and mixed-signal circuits, large complex application specific integrated circuits (ASICS) and processors, display multiple failure mechanisms and complex radiation responses such as true dose rate response, sensitivity to pre-irradiation elevated temperature stress (PETS), and time dependent effects for the “total dose” environment. For the high energy particle and heavy ion environments there are numerous possible effects including single event upset (SEU), single event latchup (SEL), single event transients (SET), single event functional interrupt (SEFI), single event gate rupture (SEGR) and single event burnout (SEB), any combination of which may occur in a single microcircuit. These multiple failure mechanisms must be addressed by the radiation test method and do not affect the overall HA methodology. For example high energy protons cause both total dose degradation and displacement damage in many commercial bipolar linear circuits. To test for degradation from both of these effects the same set of test samples would need to be exposed to both an ionizing radiation source, e.g. Co-60, and a displacement damage source, e.g. neutrons, unless the tests were performed with a proton source.<sup>26</sup> Another example is rebound in CMOS circuits where the total dose tests must be performed on the same samples in two steps, an initial irradiation to look for oxide trapped charge induced failures, followed by an additional irradiation and an elevated temperature anneal to look for interface trap related failures.<sup>14</sup> In the case where multiple effects may occur from the same radiation exposure, e.g. heavy ion induced SEU and SEL, and the total fluence must be restricted because of ionization induced degradation, two set of test samples may be required. One set would be tested at room temperature with  $V_{CC}$  at the minimum value and the other set tested at an elevated temperature with  $V_{CC}$  at the maximum.

Several forms of high speed microcircuits, such as emitter coupled logic (ECL), GaAs and other 3-5 technologies and SiGe heterojunction bipolar transistor (HBT) technologies, are very radiation tolerant for certain radiation environments and effects (displacement damage and often total dose). In those cases where it can be demonstrated that the parts are HNC at the specification level, no radiation lot sample testing is required. However, when radiation lot sample testing is required, the high speed part types are treated as any other part type in terms of the HA methodology. In the case of SiGe HBTs, the microcircuits are often fabricated in a BiCMOS technology and it is the CMOS portion of the circuit that dominates the radiation response.<sup>27</sup>

## **8. Conclusion**

From the 1960s through the 1980s military systems had a significant share of the microelectronics market and had influence with the semiconductor manufacturers. During this time many radiation hardened process technologies and families of parts were

developed and made available to hardened systems. Hardness assurance test methods and guideline documents were developed and a general HA methodology was established with funding from DTRA. In the 1990s, with the commercial microelectronics industry experiencing exponential growth and the military portion of the market rapidly decreasing, many of the producers of radiation-hardened parts left the hardened parts market. Many commercial parts are now being used in systems that have radiation requirements. Because of this, a piece-part hardness assurance approach is required to deal with these parts. We have presented the hardness assurance approach developed for the US military and have argued that, with minor modifications, it is applicable for commercial microelectronics.

## 9. Acknowledgements

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## IONIZING RADIATION EFFECTS ON ULTRA-THIN OXIDE MOS STRUCTURES

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We have briefly reviewed the most important degradation mechanisms affecting ultra-thin gate oxides after exposure to ionizing irradiation. The increase of the gate leakage current seems the most crucial issue for device lifetime, especially for non-volatile memory and dynamic logic. The build-up of positive charge in the oxide and the subsequent threshold voltage shift, which was the major concern for thicker oxide, are no longer appreciable in today's devices due to the reduced oxide thickness permitting a fast recombination of trapped holes with electrons from interfaces. Among the leakage currents affecting thin oxides we have considered here the Radiation Induced Leakage Current (RILC) and the Radiation Soft Breakdown (RSB). RILC is observed after irradiation with a low Linear Energy Transfer (LET) radiation source and comes from a trap-assisted tunneling of electrons mediated by the neutral traps produced by irradiation. RILC depends on the applied bias during irradiation and the maximum is measured when devices are biased in flat band. Contrarily to RILC, RSB is observed after irradiation with high LET ions and derives from the formation of several conductive paths across the oxide corresponding to the ion hits. RSB conduction is explained by the theory of the Quantum Point Contact as also proposed for the electrically induced Soft breakdown. Finally, we present some preliminary results, which indicate that although the direct effects of irradiation (in terms of gate leakage current increase) are small for oxide thinner than 3nm, it is possible that these devices may experience an accelerated wear-out and/or breakdown after subsequent electrical stress relative to a fresh (not irradiated) device.

*Keywords:* MOS devices; radiation effect; CMOS device reliability; Soft Breakdown; oxide wear-out.

### 1. Introduction

It is well known that exposure to ionizing radiation degrades the electrical properties of solid-state electronics. The effects of  $\gamma$ -rays, x-rays, electron, proton, heavy ion exposure on MOS devices characteristics have been the topic of several works, books, and review articles over the past two decades.<sup>1-4</sup> In principle, the main effect of an ionizing particle is the generation of electron-hole pairs along the particle track, in a number and density depending on the particle type and energy and on the material characteristics. The energy lost in ionization processes is usually measured by the Linear Energy Transfer<sup>5</sup> (LET) parameter with dimension  $\text{MeV}\cdot\text{g}^{-1}\cdot\text{cm}^2$ . In irradiated MOS structures, carriers generated in the silicon substrate may produce transient phenomena possibly leading to soft error but also to catastrophic consequences such as Latch Up, mainly due to charge collection at reverse biased junctions: these phenomena will not be considered in this work. Instead we'll examine the radiation effects on the gate oxide layers, where the majority of the radiation generated carriers are promptly recombined shortly after thermalization. Some are left behind: while

electrons can be rapidly swept out by the oxide field owing to their high mobility, slow residual holes may be trapped in pre-existing defects or in radiation induced defects inside the oxide. The resulting positive charge trapped in the gate oxide has been the main reliability concern in irradiated MOS along with the radiation induced Si/SiO<sub>2</sub> interface defects, related as well to radiation induced hole trapping and defect generation. As a consequence substantial threshold voltage ( $V_T$ ) shift and transconductance ( $g_m$ ) reduction have been measured as the typical results of exposing MOSFETs to ionizing radiation. CMOS hardening technologies were developed ad hoc to prevent or limit the occurrence of these degradation phenomena, permitting the use of hardened MOS IC's in radiation harsh environments.

In parallel, Moore's law itself was playing an underground role in enhancing the radiation tolerance of CMOS components, a role appeared only in recent years. In fact, shrinking the device dimensions following Moore's law can be accomplished only by the parallel thinning of the gate oxide to preserve the transistor current driving capability<sup>6,7</sup>. How the gate oxide thinning could enhance the device radiation tolerance was foreseen in the pioneer work by Saks and Ancona.<sup>8</sup> In fact, being the electron tunneling distance around 3 nm in SiO<sub>2</sub>, when the oxide thickness reaches 6 nm or less the radiation induced oxide positive charge is easily recombined or neutralized by electrons tunneling from the gate and/or Si substrate. This oxide thickness was approximately reached at the CMOS technological node of 0.25 μm, and the first results reporting the excellent radiation tolerance of quarter-micron CMOS components soon appeared.<sup>9,10</sup> Positive charge accumulation in the thick field oxide is not removed for both LOCOS and shallow trench isolation and it may produce the onset of the parasitic nMOSFETs between source and drain. However, this problem can be successfully circumvented by using enclosed (gate-all-around) transistor layouts and proper guard-rings.<sup>9</sup> For these devices nominal radiation tolerance over 10 Mrad(Si) were measured, i.e., exceeding by far the typical requests even for long space missions. Following the CMOS technological evolution the gate oxide thickness has now reached 2 nm or so, becoming even less sensitive to positive charge trapping problems.

If radiation induced charge trapping problems have been overcome owing to the gate oxide transparency to electrons, this characteristic has become the weak point from a reliability viewpoint. Ionizing radiation (as well as electrical stresses) can in fact produce defects acting not as trapping centers but as the agents of leakage paths across the gate oxide driving an excess gate current. Gate leakage adversely affects the overall circuit power consumption, which has been often taken as the key parameter for reliability predictions. Different leakage currents developed depending on the oxide thickness and radiation LET. In this work, we have reviewed the main issues of Radiation Induced Leakage Current (RILC) and Radiation Soft-Breakdown (RSB), as well as the long term wear out of irradiated oxides. In section 2 we have analyzed the RILC conduction mechanism, its dependence on the applied bias during irradiation and the growth kinetics with the total dose. In section 3 we summarize the main aspects of RSB: the conduction mechanism, the dependence on applied bias during irradiation, the gate current noise, and the temperature dependence. Finally, in section 4 we present the radiation induced wear-out and breakdown of gate oxides, which derives from the combined effect of irradiation plus a successive electrical stress.

## 2. Radiation Induced Leakage Current

Radiation Induced Leakage Current was firstly observed in oxides with thickness in the range of 4-8 nm.<sup>11</sup> The gate current density-oxide field characteristics ( $J_g$ - $E_{ox}$ ) of a 6-nm oxide are shown in Fig. 1a before and after irradiation with 8 MeV electrons, whose LET is 1.8 MeV·g<sup>-1</sup>·cm<sup>2</sup>. The main effect of irradiation is the increase of the low-field gate current, observed between  $E_{ox}$ =3MV/cm and  $E_{ox}$ =6MV/cm in Fig. 1a. The oxide trapped charge in the irradiated MOS capacitors is negligible, as deduced from the overlap of the high-field characteristics (over 6 MV/cm) of irradiated and unirradiated devices, corresponding to the Fowler-Nordheim electron tunneling regime.<sup>12,13</sup> RILC can be evaluated as the excess current  $J_e$  arises after stress:

$$J_e = J_g - J_0 \quad (1)$$

where  $J_g$  and  $J_0$  are the gate current density after and before the stress, respectively.

RILC shares several characteristics with the SILC (Stress Induced Leakage Current) produced by electrical stresses at high oxide fields.<sup>14-18</sup> As for SILC, RILC has been attributed to a trap-assisted tunneling of electrons across the oxide, mediated by neutral traps generated by irradiation.<sup>14,15</sup> An analytical model of RILC has been developed for ultra-thin oxides submitted to ionizing radiation, based on the solution of the Schrödinger equation for a simplified oxide band structure.<sup>19,20</sup> Here RILC occurs through a two-step process (see Fig. 1b): first, an electron tunnels into the oxide defect from the cathode conduction band edge. Then, the electron tunnels out the trap after having lost approximately 1.5eV<sup>19,20</sup>, in agreement with previous findings for SILC.<sup>14,15</sup> Consequently, the final process results to be an inelastic trap assisted tunneling. The mathematical support of the model is quite heavy and even the final analytical expression of the tunneling current is pretty complex. They show that the RILC is definitely field dependent and that the same trap parameters (energy position, cross section) can be used independently of the total dose, indicating that similar defects are generated at the beginning of, during, and at the end of irradiation. Noticeably, only defects close to the center of the oxide thickness can contribute to the excess gate leakage, owing to the decrease of the cumulative tunneling probability for defects near to the interfaces.<sup>20</sup>

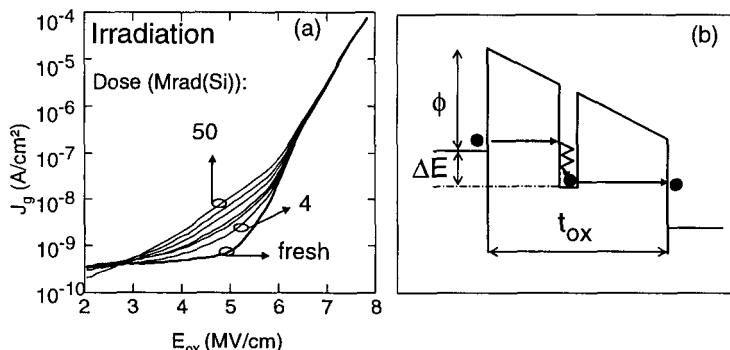


Fig. 1.  $J_g$ - $E_{ox}$  a) curves measured before (fresh) and after irradiation for various doses ranging from 4 to 50 Mrad(Si); b) Simplified band structure for the inelastic trap assisted tunneling mediating RILC. [From: M. Ceschia, et al. IEEE – Trans. Nucl. Sci. (45) 1998 - © 1998 IEEE]

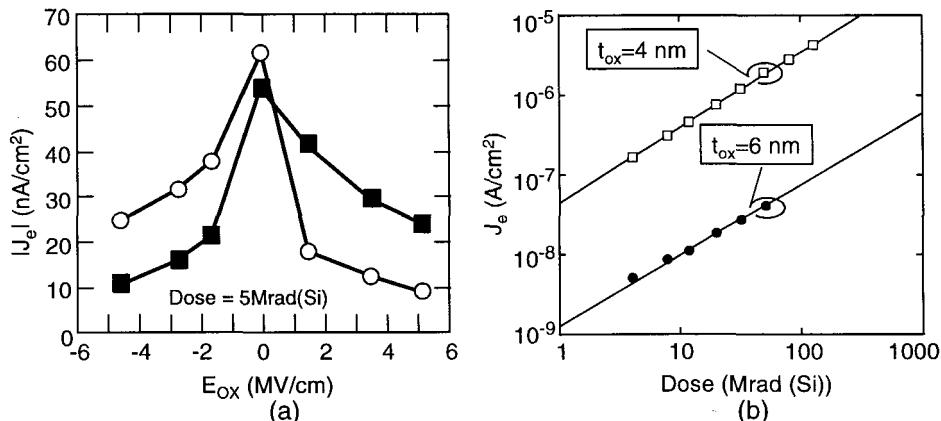


Fig. 2. a) Excess current read at  $|E_{\text{ox}}| = 5 \text{ MV/cm}$  for different gate voltages applied during irradiation for  $t_{\text{ox}}=4 \text{ nm}$  ( $\circ$ =positive RILC;  $\blacksquare$ =negative RILC); b) RILC kinetics (negative excess current) for  $t_{\text{ox}}=4 \text{ nm}$  and  $6 \text{ nm}$ . [From: M. Ceschia, et al. IEEE – Trans. Nucl. Sci. (45) 1998 - © 1998 IEEE]

Even though traps involved in RILC conduction are neutral, RILC depends on the oxide field applied during irradiation, as illustrated in Fig. 2a for  $t_{\text{ox}}=4 \text{ nm}$ .<sup>19</sup> RILC is read at  $|E_{\text{ox}}|=5 \text{ MV/cm}$ . Positive RILC is higher than the negative one on capacitors negatively biased during irradiation. The opposite holds true on devices positively biased when irradiated. Such difference disappears and RILC is the maximum when the oxide field is close to zero during irradiation. These results show that the trap distribution is controlled by the oxide field during irradiation. This fact cannot be explained if neutral traps were directly generated by the impinging 8-MeV electrons, as in case of knock-on displacement damage of the oxide lattice, for instance. Neutral defects should be homogeneously generated in the oxide layer, and any effect due to the oxide field should be negligible. Instead, charged precursors must be involved in a field sensitive generation process of RILC defects. Neutral defects may result from the neutralization of an  $E'$  centers after capturing a hole.<sup>21,22</sup> In other words, a neutral electron trap could result from a hole capture at a weak Si-Si covalent bond, which may relax into a  $\text{Si}^- \text{Si}^+$  neutral amphoteric defect after the hole compensation. Even though holes appear as the first candidate for generating neutral defects, the possible role of hydrogen in principle cannot be neglected.<sup>23</sup> In fact, ionizing radiation can easily break the weak bonds of bonded H atoms, which can migrate under an electric field and be trapped in different sites, possibly generating again neutral defects in the oxide and/or leaving electron traps in the original site.

Remarkably, RILC can be generated even at zero applied oxide field (it is maximum at  $E_{\text{ox}}=0$ ) indicating that high oxide fields are not necessary to produce the neutral defects, but only instrumental to inject energetic electrons (and holes) during high field stresses producing SILC.

RILC intensity grows with the defect density and consequently with the irradiation dose. Fig. 2b shows the RILC growth kinetics as a function of the total dose for 4-nm and 6-nm oxide irradiated with 8 MeV electrons. RILC is measured at  $E_{\text{ox}}=6 \text{ MV/cm}$ . For a given radiation dose, the excess current is much higher in the 4-nm oxides, owing to the higher

tunneling probability across the barrier, which is thinner than in the 6-nm oxide. RILC data can be well fitted by using the following relation:<sup>19</sup>

$$J_e = K_R \cdot \text{Dose}^{\beta} \quad (2)$$

where  $\beta \approx 0.9$  for  $t_{ox}=6$  nm and  $\beta \approx 0.94$  for  $t_{ox}=4$  nm, while  $K_R$  is a constant that depends on the read-out gate voltage and oxide thickness. Approximately, RILC grows linearly with the radiation dose, indicating that the oxide defect density follows a linear growth rate as well. This characteristic is strikingly different from that observed for SILC produced by electrical stresses: in fact, SILC tends to saturate at high stress fields, indicating that the defect generation mechanisms slow down when a high defect density is reached in the oxide layer.<sup>18</sup> Instead, radiation induced defects increase at a rate independent of the density of defects that are already present in the oxide, and the resulting leakage currents are higher than those achievable by electrical stresses. In other words, it is possible to generate more oxide defects by ionizing radiation than by electrical stress, where maximum density is limited by the phenomena of dielectric breakdown. However, radiation induced breakdown is not generally observed for low LET radiation sources (i. e., low energy electrons or gamma rays) even at large total doses, but is observed for high LET heavy ions as discussed in the following section.

### 3. Radiation Soft Breakdown

Recently it was shown that Radiation Soft Breakdown (RSB) can be produced in oxides thinner than 4-nm after exposure to high LET ions ( $>40\text{MeV}\cdot\text{mg}^{-1}\cdot\text{cm}^2$ ).<sup>24-28</sup> RSB derives from the residual damage of dense ion tracks across the oxide and appears similar to the Soft Breakdown produced by electrical stresses<sup>29-31</sup>. RSB has been observed even after small ion fluences where the corresponding conductive paths are likely distributed on the device surface reproducing the ion hit distribution. The dependence of the excess gate current on the LET of the incident particles is summarized in Fig. 3 for the total dose of 0.6 Mrad(Si) for Ag ions (Fig. 3a) and 80 Mrad(Si) for Si ions (Fig. 3b) in 4-nm oxides. While ions with  $\text{LET} < 20\text{ MeV}\cdot\text{mg}^{-1}\cdot\text{cm}^2$  can produce only RILC, ions with  $\text{LET} > 40\text{ MeV}\cdot\text{mg}^{-1}\cdot\text{cm}^2$  (approximately) can induce RSB. From the analysis of the results for electrons and Si ions, RILC seems to be not sensitive to LET variation for a given radiation dose. Instead, RSB occurs only for high LET values and increases with LET. In fact, only ion tracks generating high density of e-h pairs can produce high density of oxide defects, resulting in conductive paths across the oxide through neighboring defects.

In contrast with RILC, which is associated to a tunneling process across a single trap, RSB conduction can be successfully explained on the basis of the Quantum Point Contact (QPC) model.<sup>28</sup> The QPC model was first introduced for electrically induced oxide Hard Breakdown and SB.<sup>32,33</sup> The basic idea beyond the QPC picture is that the conduction is strongly localized and electrons flow through a single conductive path. In the case of radiation, each ion crossing the oxide has a non-zero probability of generating a RSB leakage path.

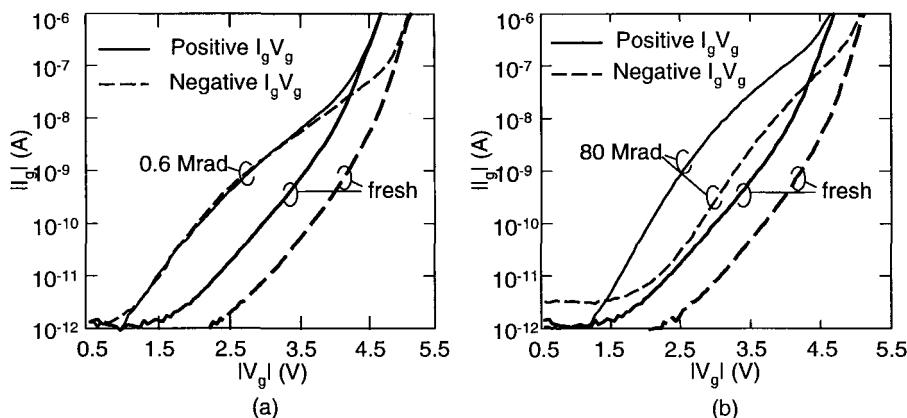


Fig. 3. a) Positive and negative  $I_g$ - $V_g$  before and after: a) 257 MeV Ag irradiation ( $LET = 52.2 \text{ MeV}\cdot\text{mg}^{-1}\cdot\text{cm}^2$ ); b) 158 MeV Si irradiation ( $LET = 2.5 \text{ MeV}\cdot\text{mg}^{-1}\cdot\text{cm}^2$ ) [From: M. Ceschia, et al. IEEE - Trans. Nucl. Sci. (47) 2000 - © 2000 IEEE]

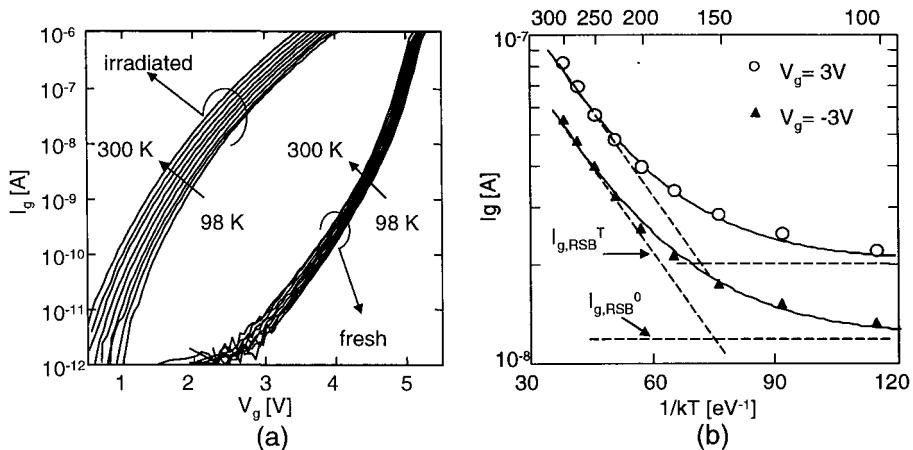


Fig. 4. a)  $I_g$ - $V_g$  curves before and after irradiation measured at temperatures ranging between 98K and 300K in a MOS capacitor with  $t_{ox} = 4 \text{ nm}$ . [From: A. Cester, et al. Apl. Phys Lett. (79) 2001 - © 2001 American Institute of Physics]

b) RSB current measured at  $V_g = \pm 3\text{V}$  as a function of temperature in the same device. The experimental data are well fitted by solid lines representing Eq.(3). Dashed curves correspond to the temperature dependent and independent current components. [From: A. Cester, et al. IEEE - Trans. Nucl. Sci. (48) 2001 - © 2001 IEEE]

Based on the QPC model, the lateral dimension of the breakdown paths is so small that the momentum in the direction perpendicular to propagation is quantized. If the path is narrow enough, the ground sub-band  $E_0$  is above the Fermi level at the cathode, and the conduction can only take place by tunneling across an effective 1-dimensional potential barrier, whose height is just  $E_0$ . This barrier is not material-related, but its height cannot be larger than that of the Si/SiO<sub>2</sub> system because electrons would be otherwise no longer laterally confined.<sup>33</sup> This model leads to the exponential relation for the gate current across a single SB spot:

$$I_g = A \cdot \exp[B \cdot (V_g - V_0)] \quad (3)$$

The parameters A and B have been related to the height and thickness of the local barrier in the breakdown path. The offset voltage  $V_0$  is due to some potential drop in the substrate. In case of RSB, where several spots can be activated after irradiation, Eq. 3 should be modified accordingly as:

$$I_g = N \cdot A \cdot \exp[B \cdot (V_g - V_0)] \quad (4)$$

N being the number of active spots.<sup>34</sup> Noticeably, RSB is dependent on the gate voltage, as well illustrated in Fig.3a, while RILC is controlled by the oxide field, and an offset appears between positive and negative curves as in Fig.3b.

RSB depends on the measurement temperature. For instance, Fig. 4 shows nine  $I_g$ - $V_g$  measurements taken at different temperatures after irradiation with  $32 \cdot 10^9$  Ag ions/cm<sup>2</sup> (LET = 52.2 MeV·mg<sup>-1</sup>·cm<sup>2</sup>) on a 4-nm oxide. The corresponding  $I_g$ - $V_g$  characteristics before irradiation are plotted for comparison. Fig. 4b shows the RSB current measured at a constant gate voltage  $V_g = \pm 3$ V in the same device of Fig. 4a. In fresh devices the gate leakage current derives from electron tunneling, which is a direct tunneling across a trapezoidal potential barrier for  $V_g < 4$ V and a Fowler-Nordheim tunneling across a triangular barrier for  $V_g > 4$ V. Being controlled by the direct or FN tunneling, the fresh  $I_g$ - $V_g$  characteristics are almost independent on temperature and the different curves almost overlap in Fig.4a. The temperature effect is larger on the RSB current, which decreases at low temperature but it is still orders of magnitude larger than in non-irradiated devices. From these results the gate current can be (at least empirically) modeled as the superposition of two contributions, corresponding to two the dashed lines in Fig.4b:<sup>30</sup>

$$I_{gRSB}(T) = I_{gRSB,0} + I_0 \cdot \exp(-E_a/kT) \quad (5)$$

$I_{gRSB,0}$  is the temperature-independent component, while the second term is the temperature-dependent component following the usual exponential law for thermal activation. The activation energy  $E_a$  has been estimated around  $E_a = 0.057 \pm 0.005$  eV, independent on the measurement gate voltage.<sup>30</sup> Such low  $E_a$  value reflects the weak temperature dependence of tunneling-based phenomena. Hence, the increase of the device temperature during normal operation will be accompanied by a limited increase of the RSB current. For instance, a RSB current of 1  $\mu$ A at room temperature (300 K) reaches only 1.5  $\mu$ A at 375K, in 4-nm oxides.

One of the main features of the RSB conduction is the noisy behavior, which is never observed in case of low LET irradiation (that is, in case of RILC). In Fig. 5 we have plotted the gate current measured at  $V_g = -2.7$ V in a 4-nm oxide after irradiation with 257 MeV I ions (LET = 61.6 MeV·mg<sup>-1</sup>·cm<sup>2</sup>). The RSB current approximately behaves as a multi-level Random Telegraph Noise (RTN).<sup>30</sup> Such fluctuations correspond to the activation/inactivation of conductive paths inside the radiation induced oxide damaged areas.

By zooming the gate current a “small” Random Telegraph Noise (RTN) appears superimposed to the main “large” fluctuations (see the two zooms in Fig. 5), pointing out to the complex nature of the radiation induced weak spots. Mixed “large” and “small” RTN fluctuations have been obtained for different oxide thicknesses, radiation doses, measurement polarities, and sampling frequencies. Noticeably, “small” fluctuations occur much more frequently than “large” ones, and both are usually attributed to an electron trapping/detrapping process.

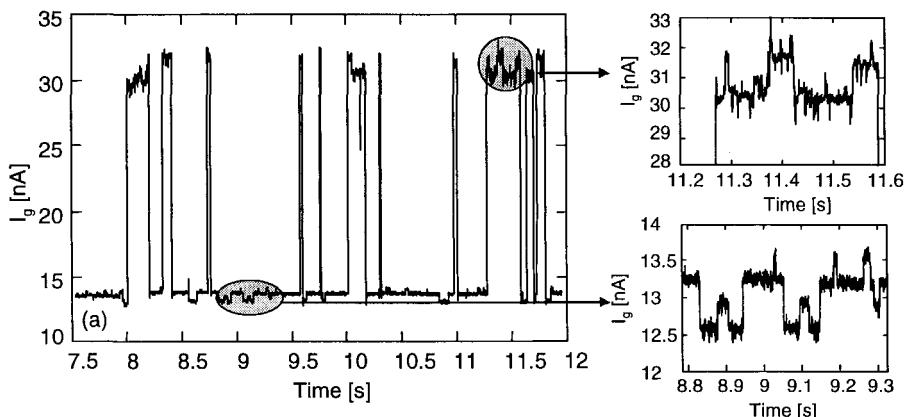


Fig. 5. Gate current measured at  $V_g = -2.7$  V as a function of measurement time in a 4-nm oxide after  $7 \cdot 10^6$  I ions/cm<sup>2</sup>. Sampling frequency was 4 kHz. [From: A. Cester, et al. IEEE – Trans. Nucl. Sci. (48) 2001 - © 2001 IEEE]

The correlation between switching frequency and fluctuation amplitude is not clear at present, but this result may provide further understanding of the microscopic nature of the RSB spot. In fact, it is reasonable to assume that fast fluctuations can be attributed to electron trapping/detrapping in shallow traps, hence characterized by fast trapping/detrapping kinetics. On the contrary, deep traps could be responsible for the slow fluctuations due to their longer capture and emission time. The current fluctuations are either “slow and large” or “fast and small”: this suggests that shallow electron traps should modify the conductance of the RSB spot much less than slow deep traps. In a simple view, this indicates that deep traps could reside in a central region of the RSB spot, which can be effectively clogged by a trapped electron resulting in larger RSB current variations. Instead, shallow traps should be located peripherally with respect to the RSB spot, where their impact on the driven current is relatively modest.

RILC and RSB may negatively impact the device reliability. For instance they surely hamper the data retention in memory cell such as Flash EPROM or DRAM and can be the origin of read disturbs of non-volatile memories<sup>35</sup>. Nevertheless, RILC and RSB have been demonstrated not to be an enhanced failure mode of significance for Very Large Scale Integration (VLSI) static logic.<sup>36</sup> Those observations were based on the assumption that the device operation integrity is basically preserved owing to the small gate leakage. In addition the impact of RILC and RSB is further decreased due to the enhanced tunneling current featured by the thinner oxide (<3nm) employed in today and future technologies. Moreover, the RSB probability appears extremely low in space missions. These conclusions are basically true for RSB itself, nevertheless recent studies have shown that RSB is an indication that other problems are about to occur, as we will discuss in the next section. Furthermore, the RSB impact on the performance of MOSFETs with tiny gate area, proper of the new decanometer CMOS generation, is still an open issue worth to be investigated. In fact, the gate area involved in RSB may become a significant fraction of the whole gate area, thus affecting the overall MOSFET electrical characteristics, such as drain current and transconductance.

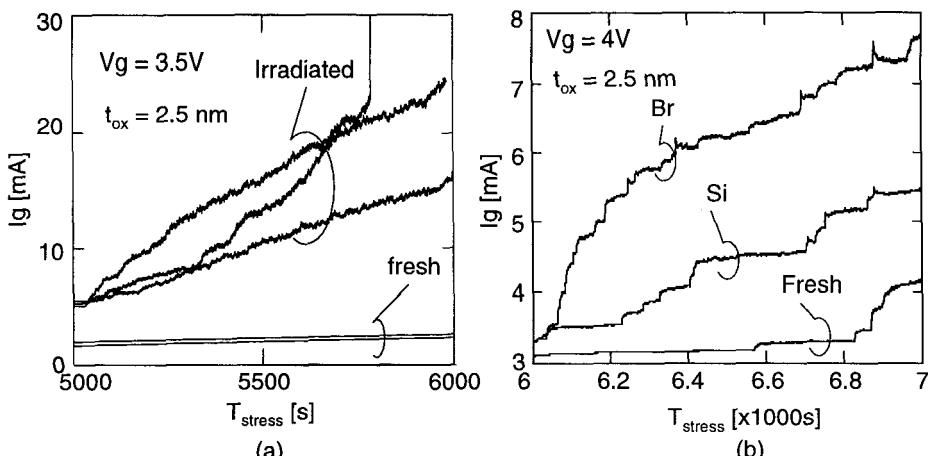


Fig. 6. Gate current evolution during Constant Voltage Stress for: a) three fresh and three irradiated devices with  $6.5 \cdot 10^7 \text{ I ions/cm}^2$ ; b) gate current evolution for a fresh and two irradiated devices ( $6.5 \cdot 10^7 \text{ Si and Br ions/cm}^2$ ).

#### 4. Radiation Induced Wear-Out and Breakdown

Recently, it has been reported that radiation is not the only concern when considering long term device reliability, as gate oxides are subjected to high electric fields during normal circuit operations. Oxide wear-out due to the applied oxide fields is usually investigated on large area MOS capacitors through accelerated electrical stresses at fields higher than those of normal device operation. The cumulative effect of ionizing radiation and accelerated electrical stresses has been considered a few times in literature<sup>11,37-39</sup>, mainly for oxides irradiated with low LET radiation ( $\gamma$ -rays, electrons, X-rays). It was found that radiation damage does not significantly impact the oxide reliability parameters, such as time-to-breakdown and time-zero-breakdown, at least for relatively high oxide thickness ( $>12\text{nm}$ ). In case of RILC, a modification due to irradiation was reported for the growth kinetics of the excess current during electrical stresses after  $\gamma$ -irradiation.<sup>11</sup>

Some fundamental differences appear under high-LET-ion irradiation. In this case an anomalous and accelerated wear-out appears when Constant Voltage Stress (CVS) is applied to an irradiated device. The effect of irradiation on the wear-out of the oxide insulating properties is illustrated in Fig. 6, where we present the gate current evolution during a CVS at  $V_g = 3.5 \text{ V}$  in a MOS capacitor with gate area of  $10^2 \text{ cm}^2$ . Here we show the comparison between three fresh and irradiated devices with  $6.5 \cdot 10^7 \text{ I ions/cm}^2$ .

For irradiated devices the current increase is fast and no clear SB event can be identified, while a progressive degradation of the oxide insulating characteristics appears. Instead, no appreciable degradation can be seen in the three fresh devices. Similar behavior has been observed for different ions (Si, Br, I, and Au) and the degradation rate has been found increasing with increasing LET.

The progressive degradation can be attributed either to the enlargement of a single weak spot driving most of current, or to the sequential opening of several small weak spots, which

appears to be more likely. In case of a single spot we should expect some SB-like signatures, such as discrete current jumps and random telegraph signal noise, which are not observed indeed. Heavy ion irradiation can instead enhance the defect production during electrical stresses in several weak points corresponding to the ion hits (65000 ions hit the oxide surface), so that electrons injected during CVS require less energy to generate defects and produce some SB leakage paths.

These results have important reliability implications. From the point of view of device application in radiation environments we may pose the fundamental question of the RSB impact on the CMOS circuit performance. Could RSB be a concern for space applications? In principle it shouldn't, at low doses and for thin gate oxides. Anyway, it is not clear if even the low level damage will act (or less) as the seed for further oxide degradation due to electrical stress during the device operating life. On one side this opens the question of the RSB impact on long term failure predictions of irradiated oxides.

## 5. Conclusions

In this work we have reviewed some of the basic degradation mechanisms affecting ultra-thin gate oxides. Positive charge trapping is no longer a real concern for device lifetime, since the reduced oxide thickness enhances the probability that holes, generated by ionizing radiation and then captured in the oxide, are easily recombined by electrons injected from the interfaces. More serious problem comes from the neutral trap generation inside the oxide, which contribute to increase the gate leakage current. Different leakage currents have been observed after irradiation mainly dependent on the Linear Energy Transfer (LET) of radiation sources. Among them:

- Radiation Induced Leakage Current (RILC) is generally observed after irradiation with  $\gamma$ -rays, electrons, X-rays and ions with low LET mainly and derives from a trap assisted tunneling through the defects generated by irradiation.
- Radiation Soft Breakdown, deriving from the formation of several localized conductive path where the ions hit the oxide surface. On the contrary of RILC, RSB is characterized by a multi-level Random Telegraph Noise.

The non-zero gate current surely hampers the long-term reliability of non-volatile memories and can affect circuits such as dynamic logic. Even though effect of the gate leakage currents, which add up to the tunneling current of a fresh device, can be pretty small and might not be a real concern for the majority of logic circuits, heavy ion irradiation can generate weak and rich-defect regions corresponding to the ion hits. Such regions may act as a seed for further degradation during a subsequent electrical stress, leading to an accelerated wear-out and/or breakdown, and seriously hampering the device lifetime.

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## HYDROGEN AT THE Si/SiO<sub>2</sub> INTERFACE: FROM ATOMIC-SCALE CALCULATIONS TO ENGINEERING MODELS

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Two contrasting behaviors have been observed for H in Si/SiO<sub>2</sub> structures: a) Radiation experiments established that protons released in SiO<sub>2</sub> migrate to the Si/SiO<sub>2</sub> interface where they induce new defects; b) For oxides exposed first to high-temperature annealing and then to molecular hydrogen, mobile positive charge believed to be protons can be cycled to and from the interface by reversing the oxide electric field. First-principles density functional calculations identify the atomic-scale mechanisms for the two types of behavior and conditions that are necessary for each. Using the results of the atomic-scale calculations we develop a model for enhanced interface-trap formation at low dose rates due to space charge effects in the base oxides of bipolar devices. We find that the hole trapping in the oxide cannot be responsible for all the Enhanced Low-Dose-Rate Sensitivity (ELDRS) effects in SiO<sub>2</sub>, and the contribution of protons is also essential. The dynamics of interface-trap formation are defined by the relation between the proton mobility (transport time of the protons across the oxide) and the time required for positive-charge buildup near the interface due to trapped holes. The analytically estimated and numerically calculated interface-trap densities are found to be in very good agreement with available experimental data.

**Keywords:** bipolar transistors; radiation effects; interface phenomena; space technology.

### 1. Introduction

The transport and reactions of hydrogen-related species play critical roles in determining the ionizing radiation response and long-term reliability of metal-oxide-semiconductor (MOS) and bipolar microelectronic technologies.<sup>1</sup> As a consequence of device processing, hydrogen is present in abundant quantities in bound forms in the oxide, the polysilicon gates and metal interconnects. When a MOS device is irradiated, hydrogen is released and transports to the Si/SiO<sub>2</sub> interface where it can induce new defects.<sup>2–4</sup> When significant densities of oxygen vacancies are present near the interface, generated protons do not react with the interface, and they can be moved back into the oxide by reversing the electric field.<sup>5</sup> Here we describe the results of our recent first-principles density-

functional calculations that allowed us to identify atomic-scale mechanisms that are responsible for this behavior.<sup>6-9</sup> Using these results we develop a model for enhanced interface-trap formation at low dose rates in bipolar devices.<sup>10</sup> This result illustrates how the atomic-scale calculations may be used in developing engineering models.

## 2. Interaction between hydrogen and the Si/SiO<sub>2</sub> interface (atomic-scale calculations)

Hydrogen is released and migrates through the oxide as a proton because H<sup>0</sup> is not a stable charge state. Our calculations also show that neutral hydrogen is not stable in the interfacial region as well.<sup>7,8</sup> This means that a proton arriving at the interface interacts with the hydrogen passivated dangling bond (Si-H) directly, without being neutralized by an electron from the Si

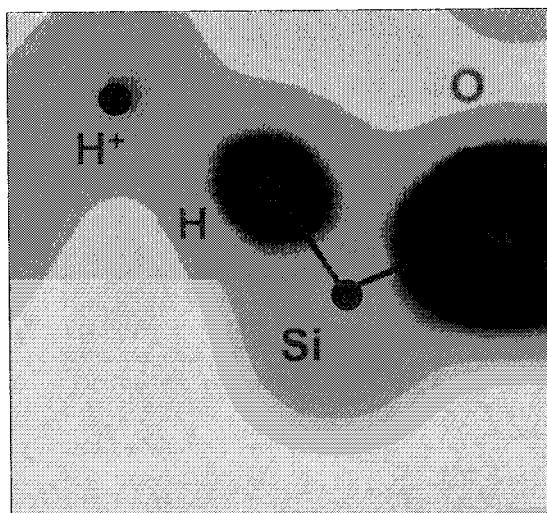


Fig. 1. Electronic density via density functional theory when a proton approaches a Si-H bond at or near Si/SiO<sub>2</sub> interface (after Refs. 7 and 8).

side of the interface as was suggested in some works (Fig. 1). The Si-H bond is highly polar, with about 1.6 electrons located near the H atom, and this negatively charged part of the dipole interacts with the proton directly, forming an H<sub>2</sub> molecule and leaving the positively charged defect (dangling bond without an electron) located at the Si atom. The energy level of this defect is located within the Si band gap, i.e., its charge state can be manipulated by the potential at the interface.

The behavior of H<sup>+</sup> is different at interfaces with different local coordination. At an abrupt interface without suboxide bonds (a Si-Si bond at the SiO<sub>2</sub> side of the interface), the proton does not feel any energy barrier higher than 1 eV (Fig. 2a). It can penetrate into Si or return back into the oxide. However, it probably would prefer to migrate

laterally at the interface because the migration energy for such a motion is extremely low (0.3-0.5 eV) before it reacts with some hydrogen passivated dangling bond in a way described above and creates a new defect. A suboxide bond can trap a proton in a position with a very asymmetric barrier (Fig. 2b). The proton would prefer to return back in the oxide, rather than to penetrate into Si.

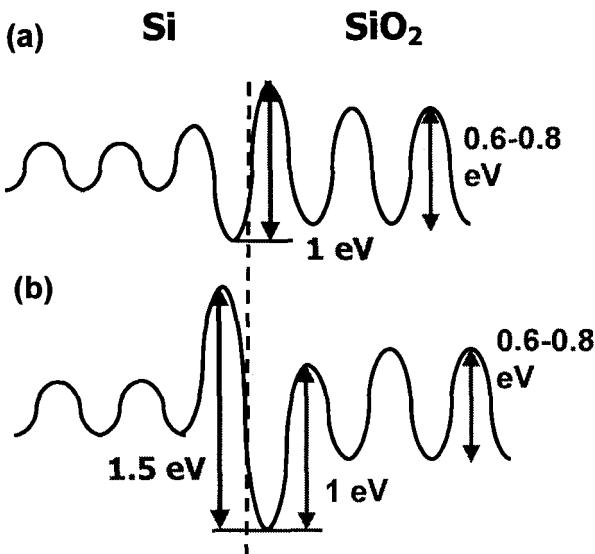


Fig. 2. A schematic for the proton potential energy across the Si/SiO<sub>2</sub> interface (shown by the dashed line): a) for an abrupt intrinsic interface; b) for an interface with a Si-Si suboxide bond.

Therefore, in the samples with a high density of suboxide bonds the flood of protons gets captured by the suboxide bonds, enabling one to observe cycling between the two interfaces when the electric field in the oxide is periodically reversed.<sup>5</sup>

### 3. Enhanced interface-trap formation for low dose rates (physical model)

The radiation-induced gain degradation of many types of bipolar transistors (BJTs) is greater at low dose rates than at high rates. The enhanced low dose rate sensitivity (ELDRS) is an important problem for space systems, and much work has been done to develop hardness-assurance methods that take ELDRS into account.<sup>11</sup> The dose-rate dependence of interface-trap formation can be modeled as a space-charge effect in the oxide.<sup>12,13</sup> It has been suggested that a key element is the difference in transport rates for holes and protons in SiO<sub>2</sub>.<sup>4</sup> The fact that at least two different types of radiation-induced trapped positive charge can be observed in high quality gate oxides has been shown experimentally by Freitag et al.<sup>14,15</sup>

Recently, we developed a physical model for the ELDRS phenomenon using differential rate equations for electrons, holes, and protons plus Poisson's equation.<sup>10</sup> Fortunately, in some important cases analytical solutions describing the dynamics of

the system may be obtained. The information about the physical mechanisms responsible for radiation-induced interface defect formation was taken from first-principles calculations.<sup>6-9</sup> The proton transport and interfacial reactions described above have been incorporated into a multiple-trapping-detrapping (MTD) code (ECORCE) similar to the one used to study the contribution of oxide trapped charge to ELDRS described by Graves et al.<sup>16</sup> For simplicity (and for convenience of comparison with analytic models), we describe the transport of holes and protons using drift-diffusion equations; a refined model that incorporates dispersive proton motion gives only quantitative changes of the final results and does not provide any new effects.

Interface-trap formation (related to proton reactions at the Si-SiO<sub>2</sub> interface) at high dose rates is reduced due to hole-related positive charge buildup in the Si-SiO<sub>2</sub> interfacial region. The mobility of holes is much higher than the mobility of protons, and the trapped holes can form an electrostatic barrier that prevents the protons from reaching the interface and generating interface traps. At low dose rates, the charge buildup process is reduced, relative to charge transport processes, and both holes and protons can reach the interface and participate in oxide- and interface-trap formation. Our analytical and numerical calculations are in reasonable agreement with available experimental data (Fig. 3).

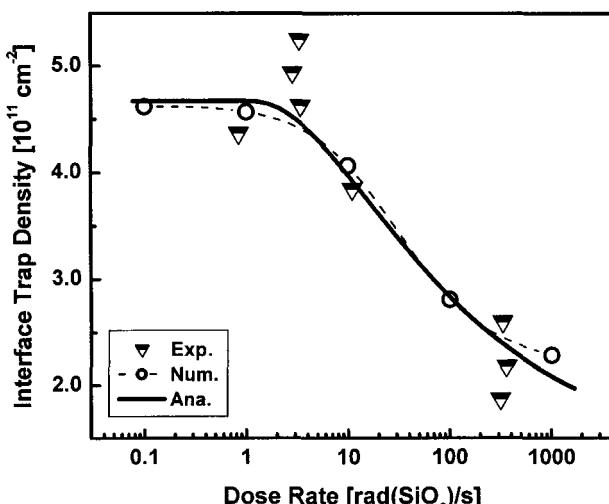


Fig. 3. Experimental (Ref. [12]), analytical and simulated interface trap density as a function of dose rate for an Analog Devices' RF25 capacitor irradiated to a total dose of 200 krad(SiO<sub>2</sub>). The hole and proton mobility used in the simulator were  $\mu_p = 1 \times 10^{-5} \text{ cm}^2/\text{Vs}$  and  $\mu_{H^+} = 1 \times 10^{-11} \text{ cm}^2/\text{Vs}$ . Interface trap build-up in the flatband to midgap energy range of the silicon band-gap arises from the contribution of 10% of the protons reaching the interface. The applied electric field is zero in numerical simulations and 0.01 MV/cm in analytical calculations

They also explain the dependence of the positive charge buildup on the mobility of the carriers and on the external electric field. Figure 4 shows the results of simulations for a range corresponding to practical electric fields observed by the transistors built with the RF25 process, e.g. a typical  $V_{BE} = 0.6$  V operating bias

would apply a field of 0.1 MV/cm over the base oxide. When the electric field becomes larger, the ELDRS effects become less pronounced because at larger fields it is harder to reach the field reversal regime. This means that all the generated positive charges will reach the interfacial region, where they get a chance to react and create an oxide- or interface- trap. In this case, the concentration of radiation-induced traps is independent of the dose rate.

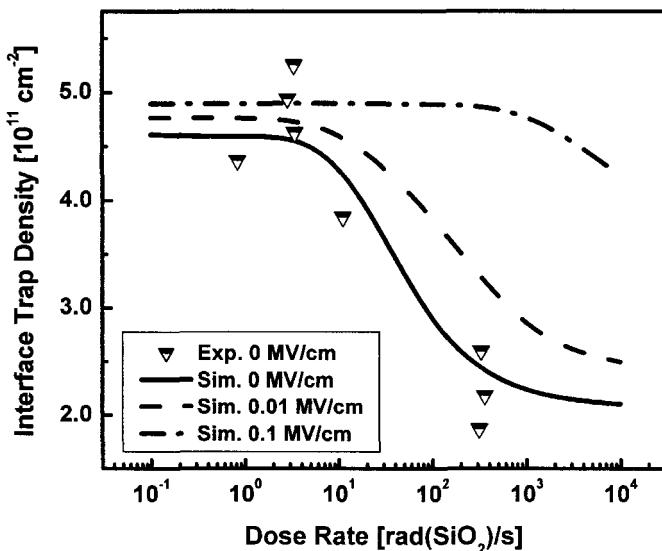


Fig. 4. Experimental (Ref. [12]) interface trap density as a function of dose rate for an Analog Devices' RF25 capacitor irradiated to a total dose of 200 krad(SiO<sub>2</sub>). Simulations have been done for different values of the applied electric field. The hole and proton mobility used in the simulator were  $\mu_P = 1 \times 10^{-5} \text{ cm}^2/\text{Vs}$  and  $\mu_{H^+} = 1 \times 10^{-11} \text{ cm}^2/\text{Vs}$ .

#### 4. Conclusion

Using results of first-principles atomic-scale calculations we have developed an analytical model of enhanced low dose rate effects in bipolar base oxides and compared its results with one-dimensional simulations. Our results strongly reinforce the idea that space-charge limited transport of both holes and protons is critical to an understanding of ELDRS effects in bipolar-base oxides. Also, they illustrate the usefulness of first-principles calculations in developing engineering models.

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## SWITCHING OXIDE TRAPS

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Positive oxide trapped charge is one of the main factors determining the radiation response of a CMOS device. The most widely accepted model for oxide-trapped charge is the dipole model, originally proposed by Lelis et al. The annealing of radiation-induced positive trapped charge proceeds (usually) via the tunneling of electrons, which form metastable dipoles, compensating the trapped positive charge without removing it. Under appropriate bias, these compensating electrons can tunnel back to the Si substrate, restoring the trapped positive charge. The experimental work leading to the development of this model is summarized. By now there is a large body of experimental and theoretical work by others, confirming and extending the original model. In particular, the relevance of the model to some electron trapping studies has been shown, and its application to the larger topic of oxide reliability is discussed.

Keywords: radiation effects, oxide trap charge, oxide reliability

### 1. Introduction

We consider radiation-induced charge trapping in  $\text{SiO}_2$  dielectric layers, primarily from the point of view of CMOS devices. However,  $\text{SiO}_2$  insulators are used in many other ways, and the same defects occur in other contexts. The key studies, which determined the nature of the oxide charge traps, were done primarily on gate oxides in CMOS devices, because that was the main radiation problem in CMOS at one time. There are two major reviews of radiation-induced oxide charge trapping already in the literature, which discuss the subject in far greater detail than is possible here. The first of these was by McLean et al.<sup>1</sup> in 1989, and the second, ten years later, was intended as an update, because of additional, new work that had been reported.<sup>2</sup>

Basically, the picture that has emerged is that ionizing radiation creates electron-hole pairs in the oxide, and the electrons have much higher mobility than the holes. Therefore, the electrons are swept out of the oxide very rapidly by any field that is present, leaving behind any holes that escape the initial recombination process.<sup>1</sup> These holes then undergo a polaron hopping transport toward the Si/ $\text{SiO}_2$  interface (under positive bias).

Near the interface, some fraction of them fall into deep, relatively stable, long-lived hole traps. See reference 1 and its bibliography for more details on the charge generation, recombination and transport processes. The nature and annealing behavior of these hole traps is the main focus of this paper, and of reference 2, Chapter 2. One of the main points in this discussion will be that some of these traps form dipoles, which exchange charge reversibly with the Si substrate. This process introduces a source of instability into the transistor threshold voltages, which could be important in complex high-speed circuits. These circuits depend critically on precise threshold control, and often on precise threshold matching for their performance. Any source of variation or instability, therefore, has the potential to degrade performance, or even to cause outright functional failure.

## 2. The Interfacial Transition Layer

The presence of hole traps in the oxide is a fundamental consequence of the oxidation process by which the oxide is grown. There is a nonstoichiometric transition layer in the oxide near the Si/SiO<sub>2</sub> interface, due to the incomplete oxidation of the Si. An early discussion of this layer was provided by Deal et al.<sup>3</sup> in a 1967 review article, which was based on work done even earlier. Basically, Si right at the interface cannot be oxidized completely because of the lattice mismatch, so there is always some excess Si. As oxide grows, the interface moves, so the excess Si, in effect, moves into the oxide, where it is eventually consumed. But new excess Si is always being formed at the interface, so a steady state concentration profile of excess Si is eventually established in the interfacial region, with stoichiometric SiO<sub>2</sub> in the bulk oxide. Deal et al. concluded that there were positively charged defects associated with the excess Si, with energy levels apparently outside the Si bandgap. Etchback experiments showed these defects to be within 20 nm of the interface (and the total oxide thickness was much greater in those days). Of course, in present-day samples, the total oxide thickness is typically much less than 20 nm, so this picture has to be modified somewhat. But the process-induced positive charge described by Deal et al. is very consistent with our present understanding of radiation-induced trapped positive charge, except that it was not induced by radiation. Deal et al. also noted that low temperature oxidation increased the concentration of excess Si at the interface, and high temperature annealing tended to reduce it. We will discuss process dependences later, but we note that radiation hardened oxides often use low temperature oxidation and low temperature annealing, both conditions which increase the excess Si concentration.

Later, Grunthaner et al. performed a series of XPS (x-ray photoemission spectroscopy) studies to determine the physical and chemical properties of this interface layer, which they summarized in a review article.<sup>4</sup> They also summarized dozens of

experiments by others which also supported the idea that there is a unique, nonstoichiometric transition layer with excess Si (or oxygen deficiency, depending on one's point of view) with a high degree of local strain (see bibliography of reference 4).

### 3. Early Spectroscopic Studies

Spectroscopic studies on quartz and bulk glasses have identified a large number of paramagnetic defects, which could be studied by electron spin resonance measurements. Of these, the one that correlates with radiation-induced oxide positive charge trapping, is the so-called E' center. This correlation was first shown by Lenahan and Dressendorfer,<sup>5</sup> and later confirmed by others. The E' center was first detected by Weeks<sup>6</sup> in  $\alpha$ -quartz, and associated with a single oxygen vacancy by others. At first, the idea that the center was due to a single oxygen vacancy was controversial, until Feigl et al.<sup>7</sup> showed that it was correct. The basic idea is illustrated in Fig 1. Two Si atoms are joined by a weak, strained Si-Si bond, where an oxygen atom should be, and each is back-bonded to three oxygen atoms. When a positive charge is captured, the Si-Si bond is broken, and the lattice relaxes. The new idea introduced by Feigl et al. was that the lattice relaxation is asymmetrical. The positively charged Si relaxes back into the plane of its oxygens, or even past it,<sup>8</sup> so that it puckers in the opposite direction. The neutral Si, with an unpaired electron in one orbital, relaxes toward the vacancy. Then Lenahan and Dressendorfer showed that oxide trapped charge, measured as  $\Delta V_{MG}$ , the voltage shift at midgap, was removed at the same rate as the E' signal in a series of isochronal annealing measurements, shown in Fig. 2. The correlation between these two measurements is strong evidence that the E' signal and positive oxide charge are due to the same defect, and the correlation has been observed repeatedly on different samples by now.

### 4. Annealing Studies

Although oxide trapped charge is sometimes referred to as "fixed" charge, this description is correct only in a relative sense. That is, radiation-induced oxide trapped charge is stable on the time scale of many experiments, but it undergoes a long-term annealing process, which has a complex dependence on time, temperature, and applied field. The annealing process can proceed by either of two mechanisms, tunneling or thermal excitation. The tunneling process can be analyzed in terms of a tunneling front, as illustrated in Fig. 3.<sup>9, 10</sup> The probability of tunneling to a particular trap site is an exponential function of the barrier height and the depth of the trap in the oxide, there will be position in the oxide at any given time, where the holes to the right will have been neutralized, and the holes to the left will remain. This position, called the tunneling front, is actually about 0.2 nm wide, and moves into the oxide with a velocity of about 0.2 nm

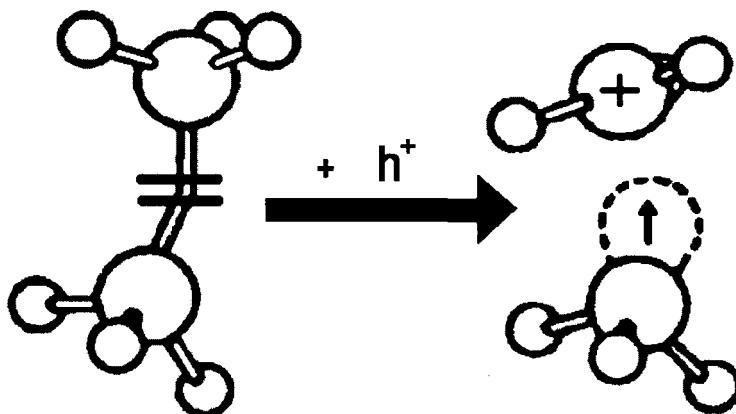


Figure 1. Oxygen vacancy acting as a hole trap.

per decade of time, according to model predictions. This  $\ln t$  dependence provides an analytical basis for the  $\ln t$  annealing behavior observed empirically in many MOS oxides.

Thermally activated annealing occurs when a carrier is thermally excited from the  $\text{SiO}_2$  valence band to the trap level, neutralizing the trap. Both the tunneling front model, and the thermal emission model were combined in an elegant fashion by McWhorter et al.,<sup>11</sup> which is illustrated in Fig. 4. Basically, they show both a tunneling front and a thermal activation front, where the position of both fronts varies as  $\ln t$ . Clearly, both mechanisms can lead to  $\ln t$  annealing behavior, but they require different trap energy distributions to do so. For a trap with a single, discrete energy level, the tunneling process will predict a straight-line  $\ln t$  annealing response, if the distribution of traps is uniform with increasing depth into the oxide. This result is often observed in unhardened, commercial oxides. If the spatial distribution of traps is peaked at the interface, and drops off with increasing depth in the oxide, the slope of the annealing curve will decrease with increasing time, which is often observed in hardened gate oxides. To predict  $\ln t$  annealing by the thermal process, one has to assume a uniform distribution of trap states across the bandgap (as McWhorter has done in Fig. 4), rather than a discrete energy level. The distribution of trap states as a function of energy level in the bandgap has been measured for many oxides, and there are well-defined peaks rather than a uniform distribution. But the peaks have a finite width, so the assumption of a uniform distribution may be justified in a limited range, but not in general. The response of all oxides is temperature independent at room temperature and over a reasonable range of higher temperatures. If one raises the temperature enough, the

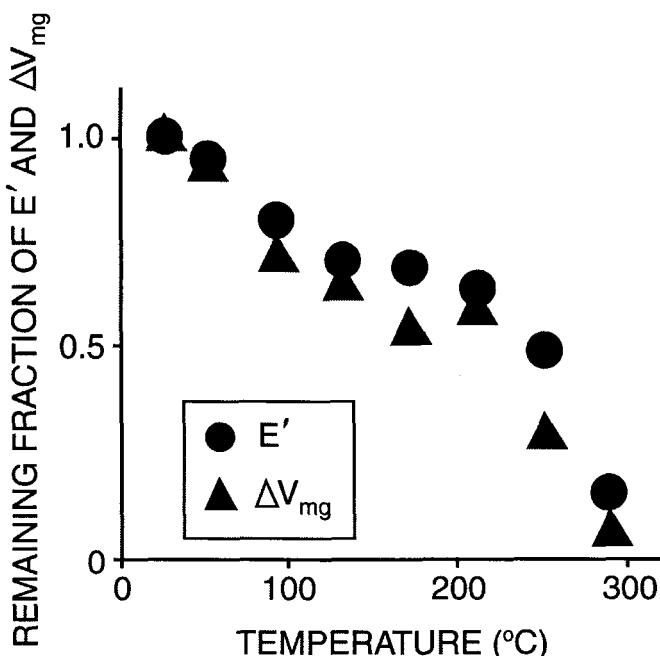


Figure 2. Correlation between  $E'$  signal and trapped positive charge in annealing experiments, after ref. [5], copyright American Inst. of Physics, reproduced by permission.

thermally activated process will become important sooner or later in all oxides. The temperature at which thermal activation becomes important varies from one oxide to another. In some oxides thermal activation is important even before 100 °C. In others, the response remains independent of temperature well above 100 °C. But by 200 °C, all oxides will undergo significant thermal annealing in a short time.

## 5. Negative Bias Annealing and the Oxygen Vacancy Dipole Model

Although the annealing process for trapped holes had been studied, and understood to a degree, the literature contained little discussion of what happened at the atomic level during annealing. Many researchers seem to have assumed, without saying so specifically, that an electron tunneled to a trapped hole, neutralized it, and reformed the broken Si-Si bond, so that the damage to the oxide was completely removed. A critical result, shown in Fig. 5,<sup>12</sup> forced many new studies, and eventually led to many new insights. Schwank et al. annealed an irradiated sample at +10V and 100 °C for about a week, until all the trapped positive charge (as determined by  $\Delta V_{MG}$ ) had annealed. Then they reversed the bias, to negative 10V, and continued annealing at 100 °C. Within about a day, nearly half of the “annealed” positive charge was restored. This result indicated

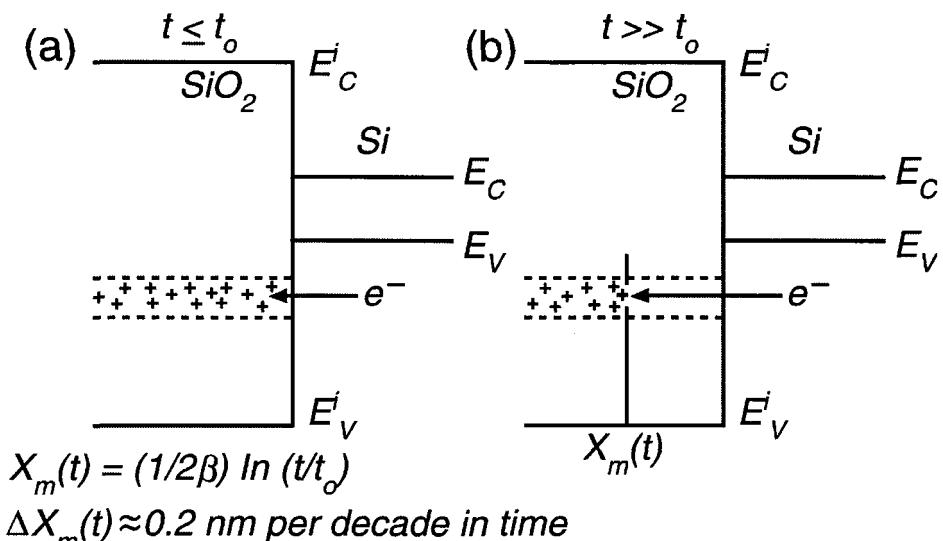


Figure 3. Tunneling front analysis; at any time there is a position where trapped positive charge to the right has been neutralized by electron tunneling, and trapped charge to the left remains.<sup>2</sup>

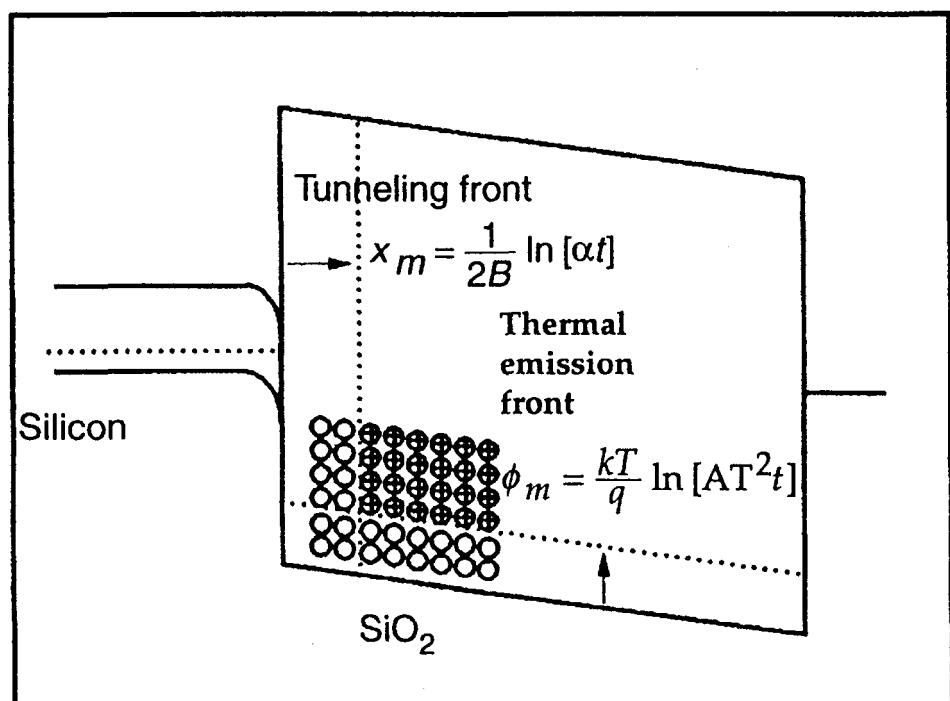


Figure 4. Annealing by the tunneling front and the thermal activation front, combined,<sup>11</sup> copyright IEEE, reproduced by permission.

that the annealing process involved some kind of compensation process, because the defects were neutralized without being removed (and unirradiated controls showed no such instability). Eventually, Lelis et al.<sup>13, 14</sup> carried out a careful study of this effect.

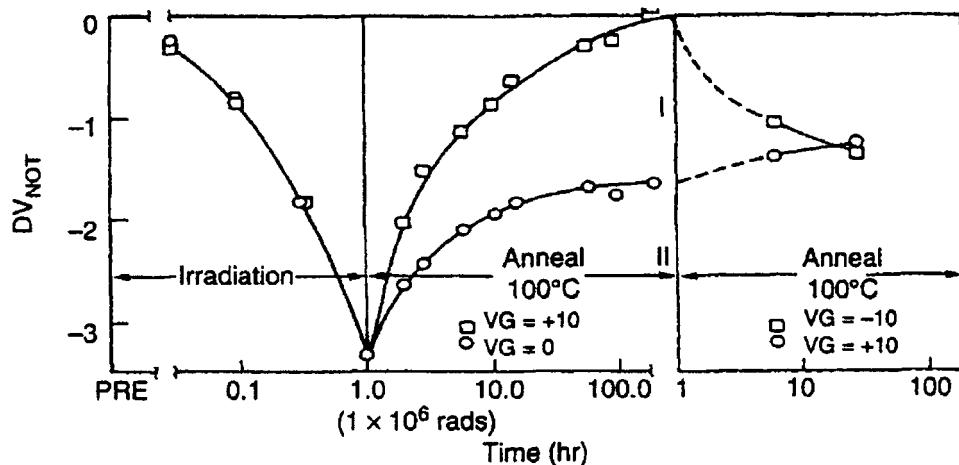


Figure 5. Trapped hole annealing results, showing that annealed holes are not really removed,<sup>12</sup> copyright IEEE, reproduced by permission.

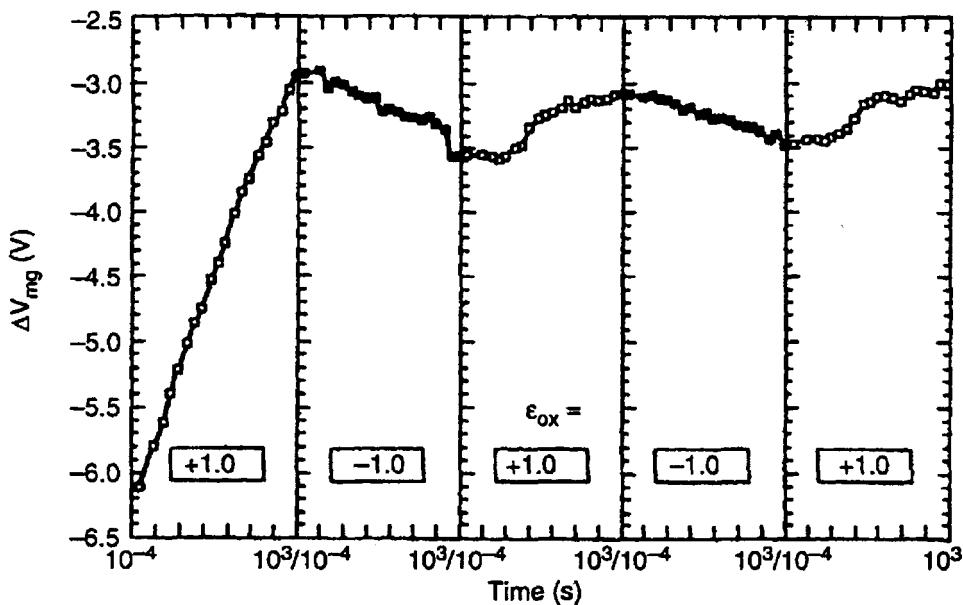


Figure 6. Alternate positive and negative bias annealing, showing reversible annealing over multiple cycles.<sup>14</sup>

One of their key results is shown in Fig. 6, which was obtained by irradiating a hardened oxide with a short Linac pulse, and annealing with the applied field alternately  $\pm 1\text{MV/cm}$ . The negative bias reverse annealing amounts to about 0.5V, which is significant, but it is clearly only a fraction of the total annealing. They interpreted these results as indicating two different processes – a permanent “true” annealing, and a reversible compensation process, where trapped charge was neutralized without being removed. The charge transfer seemed to be more or less constant over several cycles, and roughly logarithmic with time. These observations were taken to mean that charge was tunneling in and out of a hole trap defect in a more or less reversible way. The model proposed by Lelis et al. to explain these results is illustrated in Fig. 7. They proposed that the electron tunneling into the hole trap goes to the neutral side of the E' center, creating a dipole structure, a positively charged Si adjacent to a negatively charged Si. In the interface region where the E' centers are found, there is a high degree of local strain because the lattice mismatch between the Si substrate and the oxide is being accommodated. Therefore, one would expect a distribution of separation distances between the Si atoms in the E' centers. Lelis et al. suggested that if the positive and negative Si atoms were close together, the coulomb attraction would be sufficient to pull them together, reforming the broken bond, resulting in true annealing. If the relaxation were greater, so that the Si atoms were far apart, then the dipole would be stable, or at least metastable, and it could exchange charge with the substrate in a reversible manner, as in Fig. 6. Other results,<sup>15</sup> not shown here, also suggested that if one cycled charge long enough, some of the dipoles would undergo true annealing – that is, even if the Si atoms were relatively far apart, random thermal vibration might eventually bring them close enough together to reform the broken Si-Si bond. Lelis et al. also noted that there was significant variation from one oxide to another in the amount of negative bias reverse annealing. The only unhardened, commercial oxide in their initial set of samples had almost no reversible annealing, and the hardened oxides all had a significant amount. This pattern held when other oxides were tested later. We will return to this point later, in Section 10.

The dipole hypothesis proposed by Lelis et al. was attractive because it explained complex annealing behavior, true annealing and reversible annealing, in terms of a single defect that was already well known. It was consistent with the existing spectroscopic data,<sup>5</sup> which showed only a single defect contributing to the hole trapping. The ESR technique detects unpaired electron spins, and the unpaired spins are eliminated in the dipole structure as the positive charge is compensated. In fact, the spectroscopic data was one thing that led Lelis et al. to propose dipoles instead of having the electron tunnel to the positive Si, without reforming the broken bond. Then the number of unpaired spins would increase, not decrease, as the positive charge was compensated. Almost immediately, independent experiments by other groups began to provide experimental

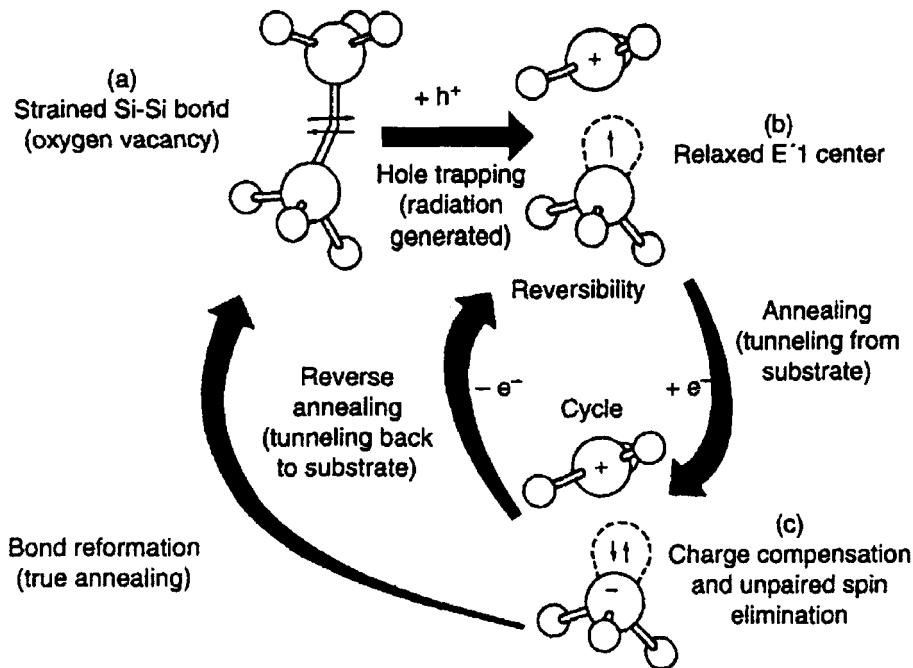


Figure 7. Model for hole trapping, permanent or “true” annealing, and reversible compensation processes.<sup>14</sup>

results that could be interpreted as supporting the dipole hypothesis, and we will discuss some of these in the next several sections. But we note that it was also controversial for several years. Three different groups presented papers which, at least implicitly, criticized it.<sup>16-19</sup> We cannot discuss these papers fully here, but reference 2 contains a relatively complete discussion. Freitag et al.<sup>16, 17</sup> and Edwards<sup>18</sup> concluded that the electrical switching behavior was due to some other (unknown) defect, not to E' centers. And Warren et al.<sup>19</sup> concluded it was too early to say where the electron tunneling into the hole trap went (in 1994, six years and many confirming experiments later), that the topic needed further study. The experiment that settled these controversies was reported by Conley et al.<sup>20, 21</sup> in 1995, seven years after the first dipole model paper by Lelis et al. It is discussed in Section 9, below.

## 6. TSC Studies

There have been numerous TSC (thermally stimulated current) measurements on MOS devices, because the technique is a good way to determine the energy levels of trapped charges. Two of these studies are particularly relevant here. The first of these was done

by Shanfield et al.<sup>22</sup> in 1988, about the same time as the first paper by Lelis et al., but not published in the open literature until later. Shanfield et al. used capacitor samples from the same source as some of the transistors used by Lelis et al., and they obtained results very consistent with those of Lelis et al. That is, they found significant compensation in the hardened oxide, but not in the unhardened oxide. The key point is that in a TSC measurement, one measures the current flow of charge freed by thermal excitation. If both electrons and holes are trapped, the current reflects the sum of these two components. In a C-V measurement, the voltage shift reflects the net trapped charge – that is, the difference between the trapped electrons and holes. If  $Q_{TSC} > Q_{CV}$ , then it is evidence for significant electron trapping. In the hardened oxide, where Lelis et al. had seen significant charge switching, the TSC results also indicated significant electron trapping. In the unhardened oxide, where Lelis et al. had seen no switching, and no evidence of compensation, Shanfield et al. saw no evidence for compensation in the TSC results, either. For this reason, the Shanfield et al. experiments were the first independent confirmation of the Lelis et al. model, in the sense that the model could easily explain the results, but they were difficult to explain with any other model.

Later, Fleetwood et al.<sup>23</sup> did another TSC measurement, intended to repeat and extend the Shanfield et al. work. They measured TSC as a function of applied bias, and confirmed that space charge effects had been significant in the work on unhardened oxides by Shanfield et al. They used samples from a different source than Shanfield et al. or Lelis et al., but also had a hardened gate oxide, and a very soft, thick field oxide. They found significant compensation in the hardened oxide ( $Q_{TSC} > Q_{CV}$ ), but not in the soft oxide ( $Q_{TSC} = Q_{CV}$ , within experimental uncertainty). The Fleetwood et al. experiment was the third time a different group had reported the same basic result, compensation in hard oxides but not in soft oxides, and for the second source of samples. We will discuss this further in Section 10.

## 7. 1/f Noise Measurements

Many authors have used 1/f noise to characterize radiation damage in MOS devices, starting with Scofield et al.<sup>24</sup> in 1989. They concluded that 1/f noise correlated with oxide-trapped charge, not with interface trapped charge. This conclusion may have been surprising to some initially, but it has since been confirmed by others. Scofield et al. cited the first paper by Lelis et al.<sup>13</sup> to support the idea that there is an electron trap associated with the hole trap that can exchange charge with the substrate. Fleetwood et al.<sup>25</sup> have recently presented further analysis, DFT (Density Functional Theory) modeling, which suggests several possible mechanisms which may account for different experimental observations. They note that capture cross sections inferred from 1/f noise, hole trapping, and trapped hole neutralization are all about the same, and the energy

levels for the defects are also about the same; all of which suggests that the defects actually are the same. They argue that the  $E_{\gamma}^{\prime}$  and the  $E_{\delta}^{\prime}$  can both contribute to 1/f noise. They distinguish between the  $E_{\gamma 4}^{\prime}$  and the  $E_{\gamma 5}^{\prime}$ , where the  $E_{\gamma 4}^{\prime}$  has the neutral silicon atom puckered, and back-bonded to a fourth Si. The  $E_{\gamma 5}^{\prime}$  is similar, except that a nearest neighbor Si is also close enough to interact, which shifts the energy levels so that the complex no longer forms a stable dipole. They suggest that the noise is mediated by lattice relaxation, as the structure shifts back and forth between these two configurations, it gains and loses the dipole electron. The  $E_{\delta}^{\prime}$ , or dimer, may account for an unexplained observation, namely, that pre-irradiation 1/f noise correlated with post-irradiation hole trapping. If the oxygen vacancy precursor loses an electron to the substrate, it would create an  $E_{\delta}^{\prime}$  center initially, which could alternately gain and lose an electron, which would also be mediated by lattice relaxation. These ideas from the modeling have not been tested experimentally, but they provide plausible explanations for a number of observations.

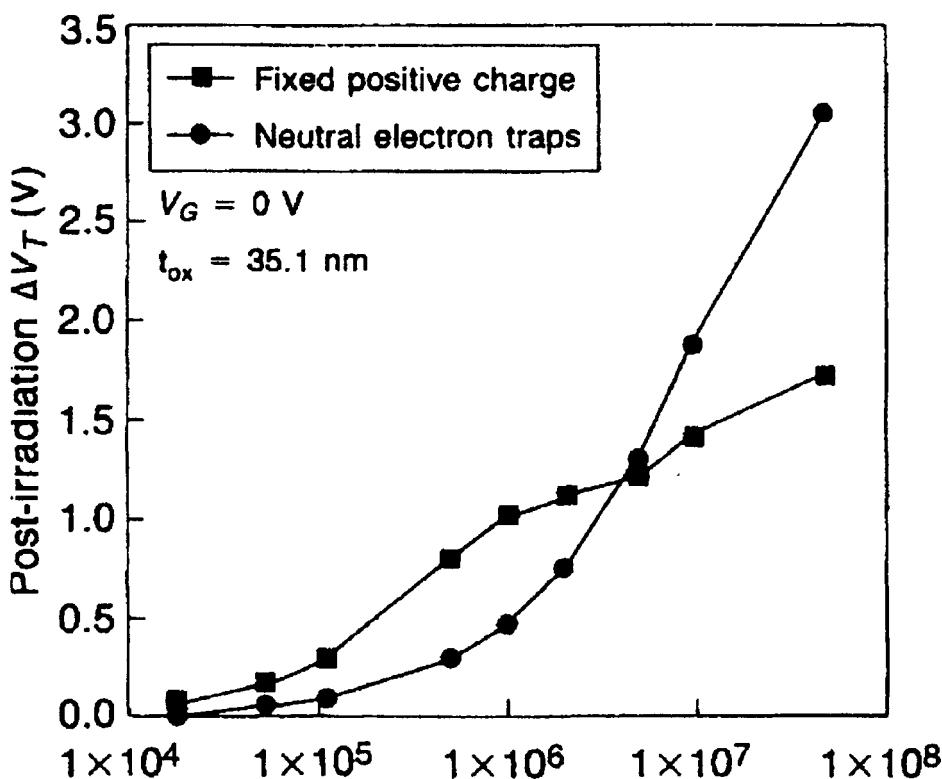


Figure 8. Positive trapped charge and neutral centers as a function of dose in rad ( $\text{SiO}_2$ ).<sup>32</sup> copyright Electrochemical Society, reproduced by permission.

## 8. Neutral Electron Traps

Electron trapping in oxides exposed to intense radiation during processing, either by electron beam or x-ray lithography, or by plasma etching, ion implantation, reactive ion etch (RIE), or other processes, has been studied for more than 25 years. Early studies<sup>26-28</sup> showed that radiation in processing created large amounts of positive charge, which could be annealed fairly easily. But after the positive charge was removed, large numbers of neutral centers remained. These neutral centers could trap electrons during normal device operation, and they were very difficult to remove.<sup>29, 30</sup> An important early insight was provided by Aitken, who suggested the traps were dipolar in nature – the positive end of the dipole capturing electrons, and the negative end capturing holes. He also suggested that a distribution of separation distances between the ends of the dipole would lead to a wide range of field strengths, explaining why electron capture cross sections vary by orders of magnitude, even when measured by the same experimenter on the same sample. (The idea that electron traps and hole traps have a common origin was later supported by Aslam,<sup>31</sup> who showed that process steps that increase the density of one also increase the density of the other.) In 1980, when Aitken suggested a dipole, there was no dipolar structure that could be suggested, that seemed to be relevant. However, Lelis et al. did eventually propose one. An experimental study was eventually done by Walters et al.,<sup>32</sup> to test the idea that the dipole structure proposed by Lelis et al. was the neutral trapping center proposed by Aitken. One of their key results is shown in Fig. 8. He measured positive charge trapping, and electron trapping as a function of dose, using optically assisted electron injection. Positive charge is observed to buildup first, but the number of positive centers starts to saturate around  $10^6$  rads. In terms of the dipole model, this means that electron-hole pairs are being created in a region with a significant density of trapped positive charges, which recombine with the electrons to form dipoles. The relative saturation means that the positive charges are being consumed almost as fast as they are created, but then the number of neutral centers is growing rapidly. Then, as they continued to inject electrons, the amount of electron trapping increased very rapidly, becoming the dominant effect by  $10^7$  rads. Walters performed the experiment in Fig. 8 with no bias applied during irradiation, but he also irradiated with bias. And he found that positive bias, which increases hole trapping, also increased the formation of neutral centers. He also found that the spatial distribution of neutral centers was the same as the distribution of hole traps, within his experimental resolution. For these reasons, he concluded that the dipole structure proposed by Lelis et al. was the neutral electron trap. Under appropriate experimental conditions, the positive end of the dipole could capture a second electron, making the whole complex net negatively charged. These results were a significant confirmation of the dipole model, and also a significant extension of it. Certainly, the fact that another group had used the model to make a prediction, and that was tested and confirmed experimentally was important

independent support for the dipole model. And by showing the connection of the dipole model to electron trapping, it was shown to be relevant to processing and reliability problems outside the traditional radiation effects area. Walters was the first to propose any specific structure for an electron trap, so his work was a breakthrough in that area.

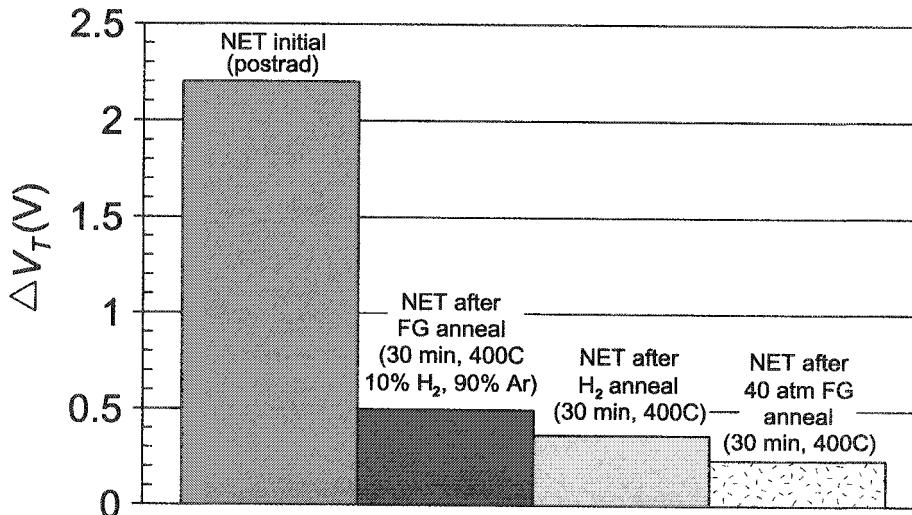


Figure 9. Annealing of neutral electron traps by exposure to hydrogen.<sup>2</sup>

Efforts to anneal neutral electron traps have mostly involved attempts to passivate the centers by annealing in hydrogen rich ambients. Results of some of these experiments are summarized in Fig. 9.<sup>29,30</sup> For the oxides in these experiments ( $t_{ox} = 35$  nm), the initial NET density was about  $1.3 \times 10^{12}/\text{cm}^2$ . The samples were then exposed to a series of annealing experiments, where each test involved more hydrogen than the one before, the number of unpassivated defects was reduced in a consistent manner. But even after extreme measures (annealing in 50 atm forming gas, which is equivalent to 5 atm pure hydrogen), more than  $10^{11}/\text{cm}^2$  NET remained. The simplest view of how these results fit together is illustrated in Fig. 10.<sup>2</sup> Parts a, b, and c are the same as Fig. 7; part d is the electron trap, as described by Walters; and part e is the neutral electron trap (dipole) passivated by reaction with hydrogen. The experimental difficulty in getting the hydrogen passivation reaction to go to completion suggests that the passivation and depassivation reactions are in equilibrium, and the depassivation reaction is strong enough that the defects are never fully passivated.

In a wafer that has been through a CMOS process, one would expect a large number of trapped holes (part b in Fig. 10) at some point, because radiation is so common in CMOS processing. (In fact, DeLaus<sup>33</sup> made the comment that the most severe radiation environment most parts ever see, is in the process line.) High temperature processing

will neutralize these by exciting carriers from the valence band, leaving a high concentration of dipole states (part c). Many of these will be passivated, forming Si-H bonds (part e), because hydrogen-rich ambients are commonly used in processing. But the reaction is not efficient enough to passivate them all, so many NETs will remain, which can subsequently trap electrons (part d). The arrows between part c of Fig. 10, and parts d and e, run in both directions because other work by Thompson and Nishida,<sup>34</sup> and by Hsu et al.<sup>35</sup> Thompson and Nishida studied the detrapping of trapped electrons as a function of temperature and applied field, and showed that the traps are shallow, and relatively easy to empty. Hsu et al. also showed that in hot electron injection experiments there is a trap filling process, and a trap creation process. That is, there are pre-existing traps which can be filled, consistent with the transition from part c to part d in Fig. 10. And if the injected electrons are energetic enough, they can create "new" traps, by breaking a Si-H bond, for example (10(e) to 10(c) or 10(d)). The dipole model, together with follow-up experiments by others, provides a framework, then, which can be very useful for interpreting a variety of reliability physics experiments. We will discuss this further in Section 11.

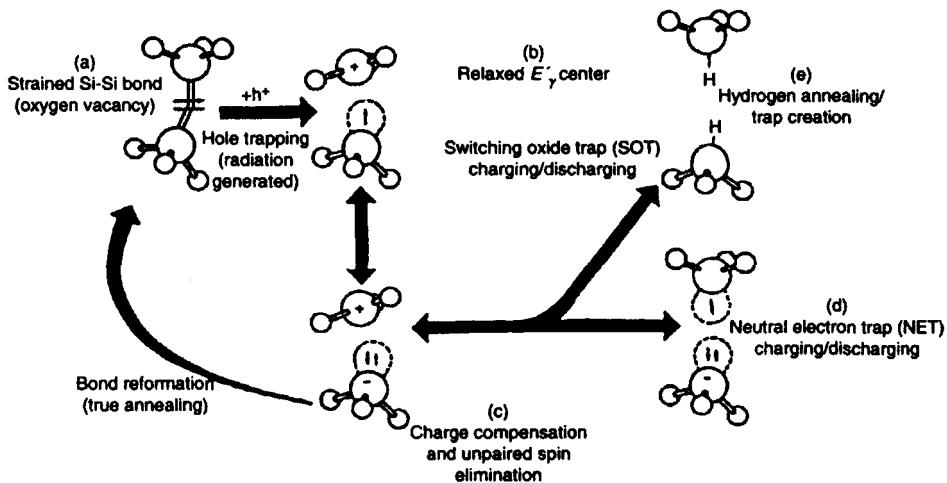


Figure 10. Schematic representation of hole traps, dipoles (compensated hole traps), NETs, and hydrogen annealed NETs.<sup>2</sup>

## 9. Recent Spectroscopic and Theoretical Studies

Two ESR spectroscopic studies and two theoretical modeling efforts bearing on the Lelis et al. dipole model have been published, several years after the model was originally published. The first of these was by Warren et al.,<sup>19</sup> which concluded that the "fixed"

oxide charge and the switching oxide charge were probably both  $E'_\gamma$  centers. Of course, this conclusion is completely consistent with the dipole model, but we should note that Warren et al. did not accept this idea. They pointed out that Edwards<sup>18</sup> had argued that the dipole configuration was energetically unfavorable, because of the electron-electron repulsive energy. And that Fleetwood had studied the charge exchange process, without reaching a conclusion on exactly where electrons tunnel to, when they tunnel into a hole trap. For these reasons, they concluded it was premature to specify the exact location of the tunneling electron, and that the question should be studied further.

The second ESR study was by Conley et al.,<sup>20, 21</sup> who monitored the  $E'_\gamma$  signal during a series of alternating bias anneals. The samples were irradiated under positive bias, then annealed unbiased for a few days, then annealed again under alternating bias, negative bias first.

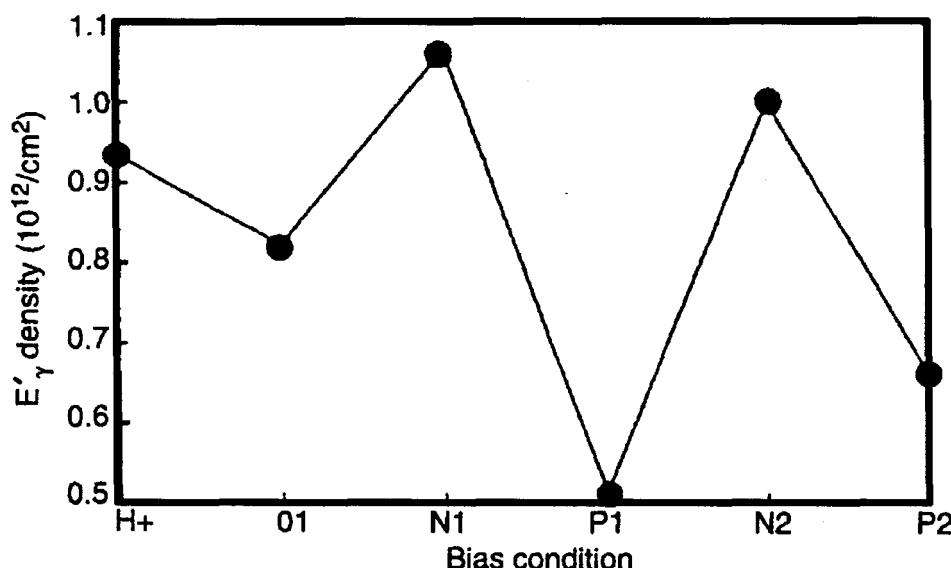


Figure 11.  $E'_\gamma$  density during alternating positive and negative bias annealing.<sup>20, 21</sup>

Typical results are shown in Fig. 11. The  $E'_\gamma$  signal increases under negative bias, and decreases under positive bias, the same as positive oxide trapped charge in electrical measurements by Lelis et al., and others. This result is very strong evidence for the dipole model, because the unpaired spin detected by ESR and the positive charge detected electrically are increasing or decreasing together, even though they reside on different Si atoms. The dipole model is the only model that has been proposed, which is consistent with this result. (We note that Fleetwood et al.<sup>36</sup> has also proposed hemi- $E'$  centers as possible trap structures – in effect, half an  $E'$  center. The trouble with these structures is that they have an unpaired spin in the neutral state, not in the charged state.

In Fig. 11, they would have valleys where the peaks are, and peaks where the valleys are. Fleetwood later agreed these centers are not consistent with the results in Fig. 11.<sup>37)</sup> From this result, it is clear that the dipole structure of Lelis et al. is the dominant switching oxide trap, or border trap. Of course, it is always possible that other structures will later be shown to produce small, second order effects.

Two recent theoretical studies have also supported the Lelis et al. model. The first of these was by Karna et al.,<sup>38</sup> who concluded, based on first principles quantum mechanical calculations, that the E' center can take two forms. The first of these is the E<sub>δ</sub>' center, which is a dimer structure where the hole is delocalized – spread over both Si atoms. This structure is symmetrical, with the Si atoms not relaxing far away from each other. When an electron tunnels to this structure, the broken bond reforms, and the trap is permanently annealed. The second form is the E<sub>γ</sub>', where the Si atoms relax asymmetrically, and one of them ends up puckered away from the other, back-bonded to another oxygen atom. The electron-electron repulsion energy means this state has a higher energy than the ground state, but it forms metastable dipoles. This calculation was the first to provide a theoretical explanation for stable dipoles.

The second theoretical study was by Nicklaw et al.,<sup>39</sup> who used density functional theory (DFT), a different mathematical method, but reached very similar conclusions. The main difference is that, depending on the positions of nearby Si neighbors, the E<sub>γ</sub>' can assume two configurations, and only one of them produces a metastable dipole.

Taken together, these four follow-up studies by different groups have provided strong additional support for the dipole model of Lelis et al.

## 10. Process Dependencies

As we have noted already, some soft, commercial oxides seem to have no significant charge switching, or compensation, while hardened oxides generally do. In fact, Conley et al.<sup>21</sup> reported that test chips from three high volume commercial process lines (Texas Instruments (TI), National Semiconductor, and Micron) had been evaluated, and none showed any significant radiation-induced switching oxide traps. This is despite the fact these are all relatively soft oxides, with a high density of other oxide traps. On the other hand, three hardened oxides ((TI), Sandia National Laboratories, and IBM/Loral/BAE) all did show switching behavior by a significant fraction of their oxide traps. The TI example is particularly instructive, since the hardened and unhardened oxides were from the same split lot, and differed in only one process step (the post-oxidation anneal, or POA). See reference 2 for a full discussion, but the main difference was that the hardened oxide received a POA at a lower temperature. The different annealing responses of these two oxides are shown in Fig. 12, where we have plotted  $\Delta V_T/t_{ox}^2$  because the oxide thicknesses are different. If one compares the response at a hundred

seconds, or at a thousand seconds, the hardened oxide has about an order of magnitude smaller shift. But at earlier times the difference between the oxides is smaller, and if one extrapolates back to the end of the radiation pulse (4  $\mu$ s), it is possible there is no difference at all in the trapping of the two oxides. This conclusion depends on how one extrapolates, or whether one believes the extrapolation, but there is clearly less difference earlier than there is later, because the hard oxide recovers faster. These results suggest there is actually little or no difference in the number of oxide traps in the hard and soft oxides, but they are closer to the interface in the hard oxide, and so are neutralized by tunneling electrons more quickly. Recall that the hard oxide in Fig. 12 has significant negative bias reverse annealing, or charge switching, and the soft oxide has essentially none; and that these oxides differ in only one process step. So the process change that makes the hard oxide hard also introduces the radiation-induced negative bias instability, and increases the annealing rate.

We note that Deal<sup>40</sup> discussed a process-induced negative bias instability, which he attributed to excess Si near the interface. This was originally an important commercial reliability problem, but Deal showed that the instability could be eliminated by a high temperature (at the oxidation temperature) POA in an inert ambient, as was done on the unhardened oxide here. He inferred that the effect of the high temperature anneal was to remove the excess Si from the interface region. The reason high temperature anneals have been a fixture in commercial processes since Deal's early work is that he (and others later) showed it did remove excess Si from the interface region, eliminating an important instability. It is important to realize that excess Si in the interface region is an important commercial reliability problem, even in the absence of radiation. But in the results in Fig. 12, the hard oxide is hard because the instability has been built back in by eliminating the normal POA. It has been argued<sup>41</sup> that high temperature annealing steps increase the excess Si concentration at the interface by reducing the oxide. While this is certainly true if the temperature is high enough, it seems not to be a significant effect at the temperatures used in these oxides. Instead, the effect of the high temperature POA seems to be to cause the oxygen vacancies to diffuse into the oxide, away from the interface, making them less active. But they still contribute to radiation damage for a long time in the soft oxide, because they are so stable. For a more complete discussion, see Chapter 2 of reference 2, and its bibliography.

## 11. Reliability Physics and Electron Trap Creation

We have already introduced the subject of electron trap creation, citing Hsu et al.<sup>35</sup> Their work was consistent with earlier work by DiMaria,<sup>42</sup> who showed that when electrons are heated above about 2 eV by the field, Si-H bonds start to be broken. Although the average electron energy never reaches 9 eV, there is a high-energy tail to the distribution above 9 eV, which gives rise to impact ionization. The important application of these

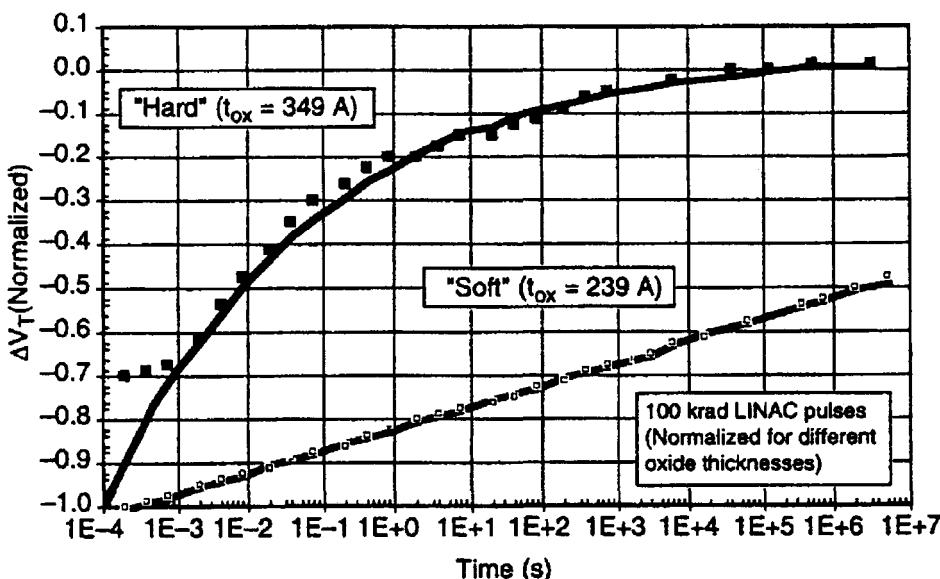


Figure 12. Normalized post-irradiation responses of "hard" and "soft" oxides, which differ only in one process step (POA).<sup>21</sup>

results is in breakdown studies. Generally, the oxide is considered to go through a wear-out phase, during which trapped charge builds up, followed by breakdown. At one time, there was some controversy over the details of the wear-out process, with some authors arguing that impact ionization led to positive charge buildup as the dominant mechanism.<sup>43, 44</sup> Others<sup>45, 46</sup> argued against impact ionization, and for a buildup of stable electron traps as the main cause of breakdown. More recently, it has become clear that both positive and negative charge buildups can occur, and both can cause breakdown. The work by DiMaria shows that both processes can occur at the same time. The basic idea is that charge builds up near the injecting electrode, usually the Si substrate. Then a very high field develops between the oxide trapped charge and the image charges at the interface. When the field becomes large enough, avalanche multiplication starts, which leads to local heating, which destroys the oxide. Clearly, both polarities of charge can develop large space charge fields, and both can be explained in different aspects of the same oxygen vacancy defect complex we have already described. The oxygen vacancy model presented here may not explain all the breakdown results in the literature, but it seems to provide a framework, which can account for many of the known results.

## 12. Oxide Traps as Interface Traps

A discussion of interface traps is beyond the scope of this paper, but there is one area where the dipole model helped to resolve a controversy about radiation-induced interface traps. There was a school of thought in the 1980s and early 1990s, which supported that idea that interface traps arose from a defect conversion process, that oxide traps somehow were converted to interface traps.<sup>47-51</sup> One weakness of this argument is that no one was ever able to propose a plausible mechanism for the conversion process. In a review paper, Oldham et al.<sup>52</sup> summarized other arguments against this idea, concluding that hole removal and interface trap formation had different time dependences, different field dependences, and different temperature dependences. Except for the fact that both processes increased with increasing dose, they appeared to be completely independent. Oldham et al. did, however, offer a new explanation of experimental results, which had been offered to support the defect conversion idea. They pointed out that no defect conversion was really necessary – oxide traps that remained oxide traps could account for the observations. The Lelis et al. dipole model, and the charge transfer mechanisms built into it, could account for the results. The fundamental question was how to define an interface trap. Most researchers took an interface trap to be a state in the Si band-gap in equilibrium with the substrate, meaning that it responded to small voltage changes, such as the 15 mV AC probe voltage in a high frequency CV measurement. Oxide traps (dipoles) do not respond to small voltage changes because they are not in equilibrium with the substrate, but they do respond to large voltage changes (e.g., from accumulation to inversion, or the reverse). For this reason, oxide traps were being interpreted as interface traps in some experiments.

A few years after Oldham et al. presented this discussion, Fleetwood<sup>53</sup> proposed that oxide traps with these electrical properties should be called “border traps.” At that time, the first Lelis et al. paper proposing the dipole model had been in the literature four years, and was already well-known. Now ten more years have passed, and the dipole model is still the only experimentally confirmed model for border traps (or for switching oxide traps, as we have usually preferred to call them here).

## 13. Oxide Thickness and Scaling

In the history of the semiconductor industry, scaling to smaller feature sizes has been a pervasive theme – almost everything has depended on it. One consequence of scaling has been that the gate oxide has become thinner every year, and thinner oxides are less sensitive to radiation damage. From  $Q=CV$ , one would predict that  $\Delta V_T$  is proportional to  $t_{ox}^{-2}$ . McGarrity<sup>54</sup> estimated the hardening that could be achieved by thinning the oxide, without special processing. The most important deviation from the thickness squared

dependence is that below about 10 nm,  $\Delta V_T$  falls off even faster than  $t_{ox}^{-2}$  would predict.<sup>55,56</sup> Almost all the trapped positive charge is neutralized by tunneling electrons, because the tunneling distance is a large fraction of the total thickness, and tunneling from both electrodes is significant. Present day gate oxides are so thin, that gate oxide hardening is no longer a practical problem. The main radiation problem now is in the isolation structures. In oxide isolation structures, the same defects and the same physical mechanisms determine the response, but there are differences because all the mechanisms have complex time dependences, field dependences, and temperature dependences. For example, the fields are lower, which means the yield of charge from recombination is less, the transport is slower, thicker oxide also means slower transport and so on. Generally, the response of LOCOS (LOCal Oxidation of Silicon) field oxides varies widely,<sup>57, 58</sup> probably because the processing varies widely. STI (shallow trench isolation) structures are replacing LOCOS, but have not been studied as much.<sup>59</sup>

One area where the dipole model has been used effectively is in understanding the ELDRS (enhanced low dose rate sensitivity) of some bipolar isolation oxides. ELDRS is at least partly due to space charge effects, and to different degrees of compensation (dipole formation) at different dose rates.<sup>60, 61</sup>

One radiation effect in the gate oxide has been reported, which is a consequence of gate oxide thinning – RILC (radiation induced leakage current).<sup>62</sup> This leakage current is thought to be a form of trap-assisted tunneling, where an electron tunnels from the substrate to a trap in the oxide. Then it tunnels from the trap to the other electrode, contributing to gate oxide leakage. Of course, the oxygen vacancy dipole model is an obvious candidate for the trap state. The same effect is observed when electrical stresses, rather than radiation, generate a trapped hole or a dipole state. Then it is called SILC (stress-induced leakage current).<sup>63</sup>

#### 14. Conclusions

The oxygen vacancy dipole model, proposed by Lelis et al., was developed in response to radiation experiments showing what was first called negative bias reverse annealing. But it has been confirmed in numerous other experiments, and extended by other groups. The later work by Walters, showing the connection with neutral centers and electron trapping is especially significant. The dipole model is the basis for a comprehensive model of oxide charge trapping (of both polarities), applicable to many oxide reliability problems. Although the model grew out of radiation effects studies, it is now of interest to a much wider community, for this reason.

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## ONLINE AND REALTIME DOSIMETRY USING OPTICALLY STIMULATED LUMINESCENCE

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A new generation of Optically stimulated materials has been synthesized at the University Montpellier II. The very high sensitivity of these phosphors, the short time constant of the luminescence and the perfectly separated spectra enable many applications in real time and online dosimetry. Dosimetry can be considered as real-time when the dose change between two measurements is considered as low enough . For satellite applications, we have developed an integrated sensor to measure the dose received orbit by orbit. In radiotherapy, OSL has been used to control the dose deposited during intra-operative *in-vivo* irradiation. At CERN, we have proposed an online system to monitor the dose simultaneously in about one hundred locations inside the Compact Muon Solenoid (CMS) experiment.

*Keywords:* Optically stimulated luminescence, Real time Dosimetry.

## 1. Introduction

Electronic devices, like biological cells, are in a less extend sensitive to ionizing radiation. In Metal Oxide Semiconductor Field Effect Transistors (MOSFET), the irradiation results in a shift of the threshold voltage. In BJTs (Bipolar Junction Transistors) the current gain decreases drastically.<sup>1</sup> In biological cells, radiation is known to damage DNA. Wherever radiation can be found, it is then useful to quantify its effect, hence to measure the dose deposited, in order to appreciate possible negative consequences. In the first attempts to measure the dose deposited by ionizing radiation, the use of calorimeters is very common. This absolute dosimetry consisted in measuring the temperature elevation of a given mass of an absorber material.<sup>2</sup> This system could be qualified as real time dosimetry but presented a few limitations, mainly due to the volume of the calorimeter itself. For low doses, the elevation of the temperature due to the irradiation was too low or too slow compared to thermal diffusion and hence, could not be measured. In the 60's a step forward was taken with Solid State Dosimetry. The synthesis of luminescent charge trapping materials enabled the development of small volume detectors. Two possibilities were offered to trigger the luminescence: (1) Thermo Luminescence (TL) consisted in heating the material, the energy necessary to release the carriers being brought by phonons; (2) The Optically Stimulated Luminescence process consisting in flashing the dosimeter with an appropriate wavelength while recording the luminescence emitted in a different wavelength.<sup>3</sup> In this case the energy was brought by photons. OSL, which didn't require the heating of the sample, was definitely faster and easier to use than TL. Unfortunately, the sensitivity of the OSL materials available at that time, in the Gy range, didn't allow applications in personnel dosimetry ( $\mu\text{Gy}$  to  $\text{mGy}$  range). Therefore, TL was chosen to become the reference in dosimetry. At that stage, due to the use of heavy reading apparatus that could only provide a delayed measurement of the dose, it was no longer a question of Real Time dosimetry. In the 80's, a new generation of OSL materials were synthesized at the University of Montpellier.<sup>4</sup> Rare-earth-doped alkaline sulphides had been known for a long time for their Optically Stimulated Luminescent (OSL) properties.<sup>5</sup> Primarily devoted to infrared-visible conversion purposes, they were later studied intensively for applications in radiation dosimetry. The Sulphides synthesized at the University of Montpellier drastically increased the sensitivity, allowing photon dose measurements as low as  $10\mu\text{Gy}$ , with a 7 orders of magnitude dynamic range.<sup>6</sup> They have been printed on films, which made it possible to record not only an image, but a map of the dose deposited in a complex geometry.<sup>7</sup> Later, with the progress of photonic devices, these sulphides enabled the integration of an OSL coupled dosimeter-reader. The device, no larger than a sugar cube has the performance to compete with TLDs but can be read and reset online.<sup>8</sup> This article is a synthesis of the research led at the University of Montpellier on Online and Real-time Dosimetry using OSL. In section 2, the quantities used in dosimetry are reviewed. The concepts of "Real Time" and Online Dosimetry are also defined on the basis of practical examples and the main dosimeters are presented. Section 3 is devoted to Optically Stimulated Luminescence. After a brief review of the basic mechanism, the guidelines for designing an OSL dosimeter will be defined. Section 4 and 5 present three examples of achievement, the monitoring of the dose received by a satellite orbit by orbit, the in-vivo measurement of the dose deposited during a radiotherapy treatment and the online control of the dose delivered by the surrounding area of the Large Hadrons collider (LHC) accelerator at CERN.

## 2. Definitions

### 2.1. Dose

The key parameter of the radiation effects is the dose  $D$ , defined as the ratio  $dE$  over  $dm$ , where  $dE$  is the mean energy transferred by ionising radiation to a mass  $dm$  of a matter.<sup>9</sup>

$$D = \frac{dE}{dm} \quad (\text{Gy}) \quad (1)$$

The unit of dose ( $\text{J}\cdot\text{kg}^{-1}$ ), is the gray (Gy); the rad, is still being used in the radiation effect community and is equivalent to a cGy. Table 1 provides the range of doses corresponding to different cases of exposure and their subsequent effects.

Table 1. Range of doses corresponding to different exposure and their subsequent effects.

Dose	Typical exposure	Number of Electron-hole pairs created and Typical Effect observed	
1 mGy	A chest X-Ray or a year in the natural background	$10^{12} / \text{cm}^3$ effect on insulators (charge trapping) Minor risk on biological Cells	
4 Gy		$4 \cdot 10^{15} / \text{cm}^3$ Transitory effects on semi-conductors	Single exposure lethal dose : leading after one month to death in 50% percent of the cases .
10Gy-20Gy	Dose delivered to a tumour during radiotherapy		
10-100Gy	Annual dose received by a satellite		
100 Gy		Voltage shift induced in the threshold of a power MOSFET  The current gain of a BJT may be cut down by a factor of 10	
1MGy	Dose expected in some Sub detectors at CERN	Mechanical properties of the materials are altered.	

The dose rate is defined as the derivative of the dose versus time. is expressed in  $\text{Gy}\cdot\text{s}^{-1}$  or in  $\text{rad}\cdot\text{s}^{-1}$ .

$$\dot{D} = \frac{dD}{dt} \quad (\text{Gy}\cdot\text{s}^{-1}) \quad (2)$$

The TID (Total Ionising Dose) as previously defined, does not depend on time. However, the effect of the same TID will be strongly dependant on the dose rate. For example, it has been shown that the degradation of the current gain in a BJTs will be several orders of magnitude higher if the dose is delivered at a very low dose rate.<sup>10</sup> Hence the concepts of "Real Time" and "On-line" dosimetry that will be covered in the following subsection.

## 2.2. Real time and online dosimetry

Wherever radiation can be found in order to quantify its effect, dose measurement can help to appreciate the possible negative consequences. The most commonly used passive dosimeters are TLDs (Thermo Luminescent Dosimeters) and radiological films.<sup>11</sup> They both provide an accurate value of the dose after an *a posteriori* processing. TLDs require a heavy and power consuming reader, the films chemical processing. This delayed reading is not a problem as long as the dose expected is low enough not to jeopardize the exposed people or the irradiated devices. The typical applications are: (1) personnel dosimetry that aims at verifying that the workers are not exposed to a dose that is not compatible with the principle of precaution; (2) quality control of irradiation facilities, in order to make sure that the dose actually delivered corresponds to the calibration and calculation. (3) long term monitoring of the dose in exposed or contaminated areas. Film and TID dosimetry is often associated with a device monitoring the flux of particles, acting as an advanced warning in case of a sudden increase in the dose rate.

Whenever the risk of over exposure is identified, delayed reading of the previous dosimeter may lead to a "too bad, too late" result which is not acceptable. Moreover, it is not always possible to reach the dosimeters after irradiation. Remote monitoring of the dose is called online dosimetry. The term "real-time" dosimetry implies that the dose is known at any instant of the on-going irradiation. However this terminology is often extended to the case of a recurrent measurement when the dose rate is low enough compared to the sampling period. These concerns are well illustrated by the following examples.

In hospital radiotherapy units, the physicians calculate the optimum dose to deliver to the tumour. Exceeding this dose is harmful to the patients health and leads to unnecessary exposure of the surrounding sound tissues. This is especially true with newly developed techniques such as intra-operative radiotherapy.<sup>12</sup> Real time dosimetry allows the physician to deliver step by step irradiation and stop exactly when the optimum dose has been reached.

The current trend in reducing the weight of satellites combined with new missions, more exposed to radiation than in the past, and the use of Commercial off the Shelf devices' may result in an increased vulnerability of systems to radiation effects in flight.<sup>13</sup> In space, knowledge of the dose received by onboard equipment is crucial to evaluate the degradation of the devices and optimise the life-time of the satellite. The space radiation environment, with its complex fluxes of particles, its low dose rate modulated by sudden increases due to solar events, is difficult to reproduce on the ground. Some techniques have been developed to predict the behaviour of electronic devices irradiated in flight, but they all rely on models of a fluctuating radiative environment.<sup>14</sup> Several recently published works put forward the way to idea that the dose received by the devices should be monitored in flight on commercial low orbit satellites.<sup>15 16 17</sup> In the case of a satellite, dosimetry has to be performed in real-time to give an advanced warning when the TID jeopardizes the onboard equipment. But in this case, dosimetry also has to be performed "online" since there is no reach a TLD or a film after the satellite is launched.

Another example of online real-time dosimetry can be found in highly radioactive areas such as

those surrounding nuclear cores. Due to the high dose rate and high contamination, it may be no longer possible to reach the dosimeter after irradiation. Here again, the dose has to be monitored online and in quasi real time.<sup>18</sup>

### **2.3 Online dosimeters**

The purpose of this section is not to provide an exhaustive catalogue of online dosimeters, but rather to give a few examples of well known detectors to compare with the OSL dosimeters.

#### *2.3.1 The Ion chamber*

The principle of the vacuum chamber was described by Greening in 1954. This theory is applicable to a cavity where pressure is so low that any gas ionisation is insignificant relative to the electron transfer between the electrodes.<sup>19</sup> Ion chambers are widely used to calibrate irradiation facilities and all other relative dosimeters. The field of application is limited by the cost, the dimensions, and the use of an electrometer to measure the charge collected which is not practical.

#### *2.3.2 The Radfets*

P-channel Metal Oxide Semiconductor (PMOS) transistors are the most commonly used devices to monitor the dose in flight. They rely on the trapping of charges in thick oxides. MOS dosimeters, stacked or not, constitute dose-integrating sensors.<sup>20</sup> On the basis of a minimum readable shift in the threshold voltage, (typically  $1\text{mV.cGy}^{-1}$ ), they allow the measurement of the dose integrated over two or three orders magnitude range.<sup>21</sup> On the one hand, the permanent shift in the threshold voltage makes it possible to keep the information that can be read at any time during the flight. On the other hand, as the oxide is charged, it becomes difficult to make out small additional variations in the dose. Some attempts at performing a thermal reset of the oxide trapped charge have been performed. Recent results on MOS devices have shown that variations in operating conditions (dose rate, temperature) induce changes in the device signal to dose response.<sup>22</sup>

#### *2.3.3 UVPROMs*

More recently, a new sophisticated type of dosimeter quantifying the flip of UVPROM memory cells has been presented and flown on the MPTB satellite. The small size of the cells makes the UVPROM very suitable for micro dosimetry. A statistical approach has been developed which provides an accurate measurement of the macroscopic dose.<sup>23</sup> The overall sensitivity of the device is typically one Gy. In flight, the UVPROMS integrate doses in the range of 1Gy-1000Gy.

### 3. Generalities on the OSL

#### 3.1. Basic mechanism

Optically Stimulated Luminescence results from a process starting with the irradiation of an insulator or a wide band gap semiconductor, as shown in (1) on Fig. 1. Ionising radiation creates in the material a large amount of trapped carriers. Some charges remain trapped on localized defects after irradiation for a time period depending on the temperature and the activation energy of the traps. Stimulating the material optically (2) will provide the energy necessary to release the trapped charge. A subsequent radiative recombination may be observed (3) as shown in Figure 1. Quantifying the amount of emitted light makes it possible to evaluate the energy absorbed by the dosimeter. It is interesting to note that, from an external point of view, OSL can be considered as an anti Stokes phenomenon since the wavelength stimulation is greater than the wavelength of the luminescence.

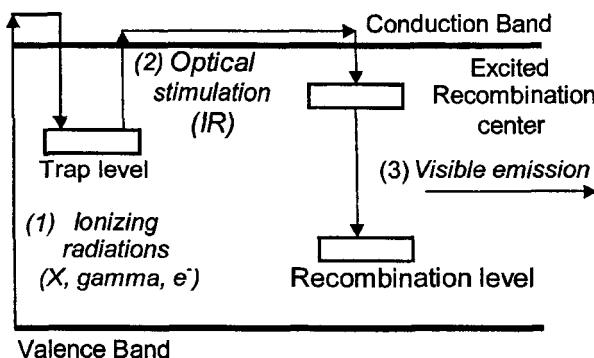


Fig. 1. Basic mechanism of the optically stimulated luminescence.

#### 3.2 The OSL materials

##### 3.2.1 The main families of OSL materials.

Several families of materials have been identified as emitting Optically Stimulated Luminescence. They differ by their chemical and optical properties and not all of them are appropriate for an application in dosimetry. The intrinsic ability to store charges for a large period of time and the efficiency of the luminescence is the major criterion for selecting OSL materials. This efficiency is strongly dependant on the dopants and their concentration. The major families, known for their high luminescence yield are listed in table 2 along with their excitation, stimulation and emission wavelengths.

Table 2. Summary of the major OSL materials and their characteristic wavelengths

Material	Stimulation (nm)	Emission (nm)
MgS:Ce,Sm	800 => 1500	500 => 700
SrS:Ce, Sm		
BaFX, X= Cl, Br, I	470 => 630	350 => 450
NaCl:Cu	400 => 500	325 => 375
KCl:Eu	450 => 650	400 => 450
KBr:In	500 => 700	400 => 600
RbBr:Ti	600 => 800	300 => 450
RbI:In	600 => 800	350 => 450
$\alpha$ -Al <sub>2</sub> O <sub>3</sub>	300 => 450	350=> 500

Another important criterion can be deduced from table 2, the separation of the stimulation and the emission spectra. An overlap in the spectra makes it difficult or is impossible to discriminate the emission from the stimulation. It is the case for example for the  $\alpha$ -Al<sub>2</sub>O<sub>3</sub>. Solutions have been found implying that the dosimeter is stimulated with a high intensity laser pulse on the edge of the spectrum. The low cross section is then compensated by the power of the laser. Another technique consists in stimulating the Al<sub>2</sub>O<sub>3</sub> with a pulsed laser and recording the luminescence between the pulses. Both techniques lead to heavy reading systems, comparable in size to a TLD reader.<sup>24</sup> Nevertheless OSL reduces the reading time by a factor of 100 compared to thermo luminescence.

### 3.2.2 Lenard's family

The rare-earth-doped alkaline sulfides (MgS, CaS, BaS, SrS and BaS) have been identified by the German physicist P. Lenard as efficient phosphors<sup>5</sup>. They exhibit both TL and OSL. Primarily devoted to infrared-visible conversion, they were later studied intensively for applications in radiation dosimetry.<sup>25</sup> A new generation of Sulphides has been synthesized at the University of Montpellier that make it possible to reach for the first time a sensitivity in the range of 10 $\mu$ Gy.<sup>4</sup> The saturation has recently been investigated and found occur at 500Gy, ensuring a 7 orders of magnitude dynamic range. The stimulation wavelength, optimum at 1 $\mu$ m is easy to discriminate from the emission spectrum stretching from 450 to 650 nm.

### 3.3 Guidelines to the design of an OSL dosimeter

Any system based on OSL requires, besides the sensitive OSL phosphor, two additional devices, a stimulation source and a photo-detector, as shown on Fig. 2. The role of the stimulation source is to provide the energy necessary to de-trap the carriers.

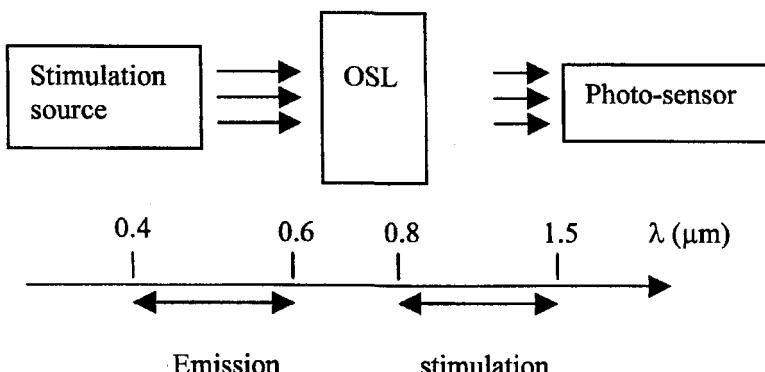


Fig. 2. generic structure of an OSL dosimeter using rare earth doped sulphides.

The sulphides doped with cerium and samarium used in this work allow a wide range of stimulation wavelength from 0.8 to 1.5 microns. Various systems can be used to collect the luminescence depending on the application targeted, providing they make it possible to discriminate the stimulation from the luminescence. From this point of view, silicon detectors are not suitable. In previously published works, stimulating the sample with a solid state laser emitting a 1.3 micron wavelength and collecting the OSL with a photo-multiplier tube (PMT) made it possible to discriminate emission from stimulation.<sup>6</sup> A typical emission spectrum of a calcium sulphide doped cerium samarium is given on figure 3. Such an emission is right in the PMT high sensitivity range and far away from the stimulating wavelength located at one micron and up.

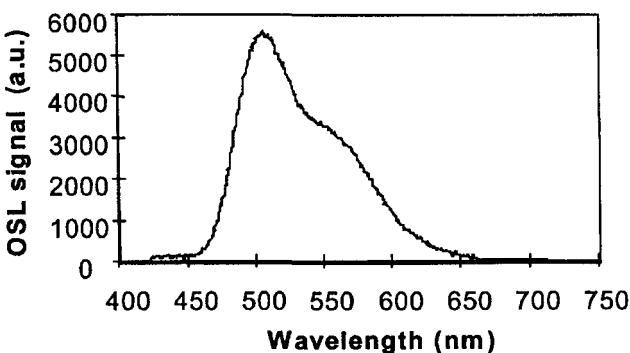


Fig. 3. Emission spectrum of the CaS:Ce,Sm.

### 3.4 The OSL Signal

Fig. 4 represents the typical signal shape of an OSL signal. The stimulation is switched on after 100ms which results in a quick luminescence. The decay of the signal can be easily modelled by considering a simple reaction rate equation providing an exponential solution.

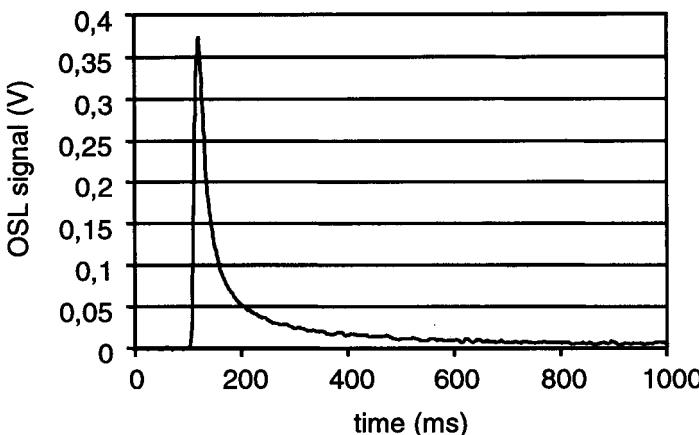


Fig. 4. typical shape of an OSL signal recorded with a GaAsP photodiode for a dose of 2mGy.

Let us consider irradiated OSL material, in which  $N$  charges have been trapped during the irradiation process. The number of charges depends on the dose  $D$  and thus is noted  $N(D)$ . Under a constant stimulation flux  $F$ , an OSL signal (function of the time  $t$ ) is observed. The OSL signal is noted  $S_{osl}(t)$ . The general shape of this signal has already been presented in Figure 4. Since the response of the OSL to a stimulation is obtained within a nanosecond the rise time of the luminescence can be considered as negligible.<sup>26</sup> In fact, it only depends on the time constant of the input amplifier stage. It is then reasonable to assume that the peak value of the signal is obtained for  $t=0$ . The decay of the OSL signal is then modeled with an exponential law,

$$S_{osl}(t) = K.N(D).F. \exp(-\sigma.F.t), \quad (3)$$

where  $K$  is a constant that depends on both the material and the detection set-up.  $\sigma$  is the cross section of the stimulated detrapping process. The time constant of the decay is then given by

$$\tau = \frac{1}{\sigma.F}. \quad (4)$$

At  $t = 0$ , the peak value of the signal is given by

$$S_{osl}(0) = S_{peak} = K.N(D).F \quad , \quad (5)$$

and is directly proportional to the dose D as long as the stimulation flux remains constant. Let us consider now the integrated OSL signal. It is given by integrating Eq.(2). It comes

$$\int_0^{\infty} S_{osl}(t).dt = \frac{K}{\sigma} .N(D) . \quad (6)$$

The value given by Eq. (6) is no longer dependant on the stimulation flux but only proportional to the total amount of charge trapped within the material. In the following section, three examples of OSL online dosimeters are presented.

#### 4. An OSL Sensor for Space Application

The University Montpellier II is developing a radiation sensor for the CNES (Centre National d'Etudes Spatiales).<sup>27</sup> The guideline for this project are to measure the dose deposited orbit by orbit, which implies a sensitivity in the mGy range (by cycling irradiation, reading and reset)? Nevertheless, the eventuality of a sudden increase in the dose rate due to a solar event has to be taken into account, which requires, a wide dynamic range. Any equipment flying in space has to conform to requirements in terms of weight, consumption and hardness assurance. From this point of view, PMT were left aside in the design of the integrated sensor. Regular silicon photodiodes, were not considered either, since their extreme sensitivity to infrared light doesn't allow proper discrimination of the stimulation light from the OSL signal. Hence, wide gap composite material photodiodes such as GaAsP or GaP were preferred. A simple surface mount light emitting diode provides stimulation.

##### 4.1 Basic structure

The basic cell of the OSL sensor is designed as the very simple structure presented in Figure 2, in which the OSL layer is directly sandwiched between the light emitting diode, LED, and the photodiode. Most of the infrared stimulation is absorbed by the OSL layer. The power consumption is limited to the current needed to bias the LED during stimulation, that is 50mA during 20 seconds under a 2V Bias voltage. The whole sensor can fit in a sugar cube volume. Figure 5. presents a OSL sensor, integrating also the read out circuitry and a feed back loop to control the current in the LED. The basic external circuitry needed to operate the sensor consists only of a dual operational amplifier that converts the current delivered by the photodiode into voltage. The signal is then amplified and digitised. A voltage source, triggered by a logic input is also needed to operate the stimulation source. Let us note that in the case of not hardened circuit, or for sensor test this additional circuitry can be shielded. The degradation of the LED emission can be compensated by increasing the forward current through a feedback loop.<sup>28</sup> Adapted rad-hard devices have been developed.

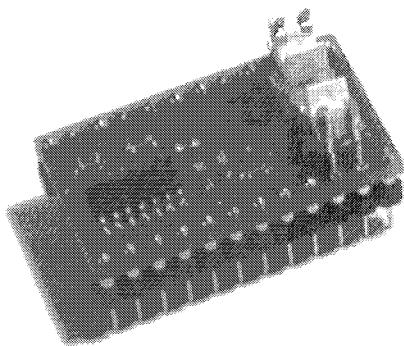


Fig. 5 . compact OSL sensor integrating the reading circuitry for direct PCB mount.

#### **4.2 Calibration**

A first series of experiments have been performed using a  $^{60}\text{Co}$  source in which irradiation and reading occur sequentially. The sensor is positioned on a tray in the irradiation field. The external reading circuitry remaining outside the exposed area. During irradiation, the system is switched off in order to avoid transient effects. From this point of view, the OSL device can be considered as a passive detector. During the reading phase, a dedicated circuit is switched on and the stimulation source operated. The OSL signal recorded is presented in Figure 4. Both the maximum and the total OSL emission are measured to monitor the dose. During the reading, the whole OSL layer is exposed to intense IR stimulation flux that completely resets the material after 10 seconds. The curve presented in Figure 6. was recorded by increasing the dose step by step, varying both the distance source to sample and the exposure time to explore a 3 orders of magnitude range of doses. The present prototype was developed to record the OSL in the 1 mGy to 1Gy Range. For higher doses the gain will have to be lowered to avoid the saturation of operational amplifier. The response is found to be linear on the investigated range of the dose. So far, the OSL Sensor has flown on the International Space Station as a part of , a radiation detection module designed by the CNES. An OSL Sensor has been integrated to the nano-satellite CUBESAT SACRED (Study on the Action of Cosmic Rays on Electronic Devices) experiment of ALCATEL Space. CNES is also planning to fly an improved version of the OSL on PROBA II.

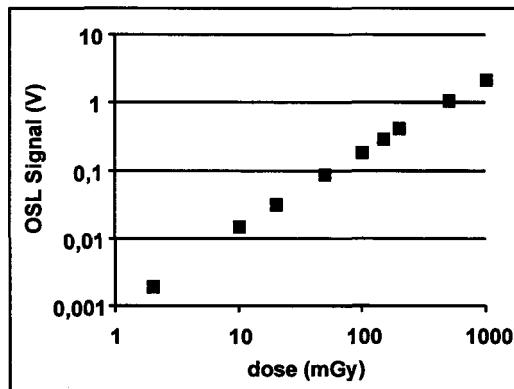


Fig. 6. Calibration curve of the OSL integrated sensor.

## 5. Remote Online OSL Dosimetry using optical fibers

In the previous example, the dosimeter benefits from a printed circuit board mount. Both the sensor and the electronics are exposed to radiation, the problem of the radiation induced damage is supposedly being addressed. It is not always possible or practical to use a sensor integrating both the OSL and the reading circuitry. The reason can be either a very harsh radiative environment, or the necessity to minimize the size of the sensor. In both cases, the use of optical fibres can provide an elegant solution. In this section, two examples of online dosimetry using OSL and optical fibres will be presented. The first application proposes a solution to the real-time monitoring of the dose delivered to a tumour during an Intra Operative Radio Therapy treatment. The second application addresses the measurement of very high doses in the hot environment of the Compact Muon Solenoid, one of the four experiments of the LHC at CERN.

### 5.1 In vivo dosimetry: principle and specific requirements

Intra-operative radiotherapy consists in irradiating the tumoural bed, *in vivo* during surgery. The aim of this technique is to eliminate the local residual abnormal cells while avoiding unnecessary exposure of the sound tissues. After removing the tumour, the surgeon and the radiotherapist install a cylindrical localizer in order to focus the electron beam straight on the tumoural volume as shown in Figure 7. After the irradiation is completed, the patient is carried back to the block and the surgery continues. The irradiation is carried out with electrons. A low energy, a few MeV, is preferred since the target area is directly in contact with the localizer not in depth. The dose delivered is typically a few tens of Gy. The dose rate is typically 200 or 300 monitor units per minute (1MU is equivalent to a cGy if the accelerator is correctly calibrated). The optimum dose is computed by the physician, but a step by step monitoring of the dose actually delivered is necessary to make sure this dose is reached but not overstepped.

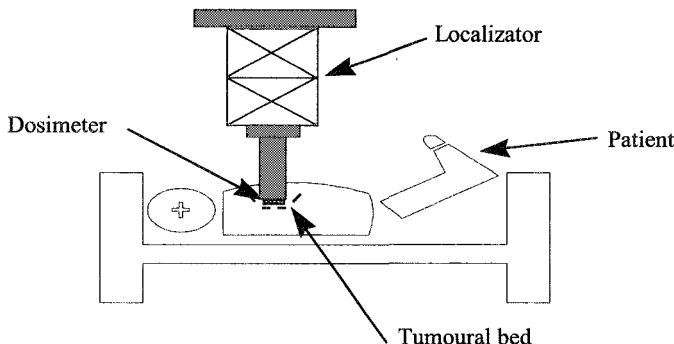


Fig. 7. configuration for an intra-operative radiotherapy treatment.

### 5.1.1. Specifications

Measuring the dose during the irradiation implies that the sensor is inserted below the localiser. The first mandatory concern is, of course, the detector size which has to be as small as possible. The dose is measured in the human tissue which effective atomic number  $Z$  is close to 7.2. As a consequence, the effective  $Z$  of the dosimeter will have to be as close as possible to this value in order not to affect the measurement. The energy deposited in the sensor has to come from secondary electrons emitted in the surrounding tissue and not in the sensor itself. Very small sensors, providing that their dimension is negligible compared to the mean free path of the secondary electrons, have an effective response close to the response of the surrounding material. (Bragg-Gray theorem). This assertion has two immediate consequences: (1) Metals or any other high  $Z$  material are prohibited for the design of the sensor (2) The sensor has to be small enough to verify the Bragg Gray Conditions.

### 5.1.2 Experiments

A prototype of online dosimeter was developed and tested at the Val d'Aurelle Hospital in Montpellier. The bloc diagram is described on figure 8-a. The OSL sensitive crystal, a cylinder of 1mg of magnesium sulphide, is enclosed in a polyethylene cap and positioned at the extremity of a multimode optical fibre. The role of the fibre is: (1) to lead the infrared stimulation provided by a fibered laser diode ; (2) convey the OSL signal toward a PMT. The different wavelengths are injected and sorted out in the fibre by means of optical couplers and filters. The OSL signal is then digitised and recorded. The sensitivity of the prototype was investigated using a  $^{60}\text{Co}$  source at the University of Montpellier. The sensor is completely reset after measurement by a 3s intense stimulation. The minimum detectable dose was estimated to  $100\mu\text{Gy}$ . The dynamic range, limited in this arrangement only by the saturation of the output amplifier, covers 5 orders of magnitude. The use of  $^{60}\text{Co}$  was imposed by the impossibility to deliver low doses precisely with therapy electrons accelerators (5 to 20 M eV) at the hospital. Although the total dose delivered during the treatment

usually rises up to tens of Gy, it is important to note that the OSL is meant to measure incremental doses in the cGy range. The curve presenting the response of the sensor as a function of the dose is presented on figure 8-b. As usually, we have to pay a special attention to the stability of the whole irradiated system with total dose.

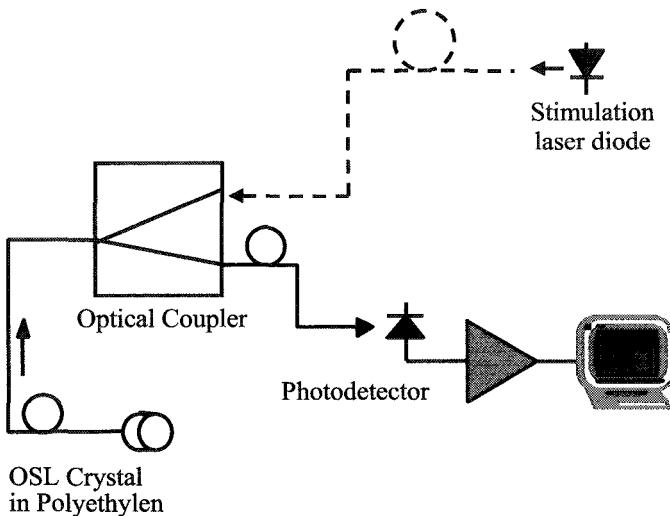


Fig. 8-a. block diagram of the OSL online dosimeter

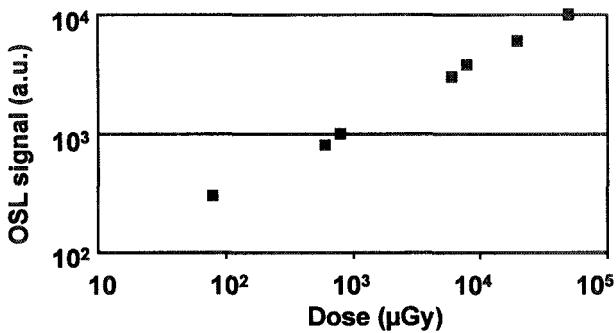


Fig. 8-b. Calibration curve of the OSL online dosimeter

## **5.2 Monitoring of the dose deposited by the LPI 500 MeV electron beam with an online OSL sensor.**

### **5.2.1 The CMS environment**

The radiation environment encountered in CERN experiments such as the Compact Muon Solenoid (CMS) differs completely from the previous medical and space, applications of the OSL dosimeters. In the Pixel sub detector of CMS, the total dose integrated over a 10 year period is estimated to 2 MGy with a particle fluence of  $10^{14}$  per  $\text{cm}^2$ . In addition, the risk of accidental radiation bursts (that can damage the sub-detectors) due to beam-loss or bad tuning has also to be taken into account. Considering this potential risk and the uncertainties in the calculation, the idea of implementing a radiation monitoring system has to be considered. The present work was initiated by the CMS group who provided the beam time.

### **5.2.2 Specific Modifications of the system**

In the medical application presented in section 5.1, the mandatory parameters where the sensitivity and the size of the sensor. Those requirement led to the choice of a PMT to collect the signal, and a single fibre carrying both the stimulation and the OSL signal. However, the optical coupler introduces a 10db attenuation on both wavelength. In the case of the dosimetry system proposed for CMS, very different specifications led to very different choices.<sup>29</sup>

First of all, the aim of this system is to measure the dose simultaneously in different locations of the detector. The number of sensor to be used is estimated in the order of one hundred, for CMS only, hence the necessity to simplify the system and reduce its cost. The range of dose to measure is also much higher and can reach 1MGy in the Pixel sub detector. To take into account those specificities, the system was modified as presented in figure 9. The sensor itself consists of an OSL crystal and an infrared LED positioned at the same extremity of a 50m long optical fibre. The LED provides the wavelength necessary for the optically stimulated reading. The resulting luminescence is collected by means of the optical fibre and guided toward a photo-multiplier tube. Due to the optical fibre, the photo-multiplier can be moved outside the irradiation area to prevent any radiation-induced damage. It is important to note that this design makes it possible to suppress the optical coupler, hence the 10db of attenuation. As a result, the signal intensity is now compatible with the use of a simple photodiode, similar to those used in the integrated sensor.

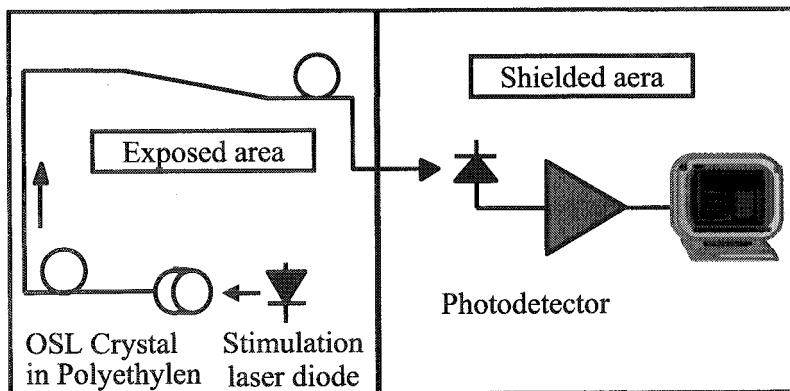


Fig. 9. Bloc diagram of the modified online system

### 5.2.3 Experimental results

During the irradiation period, 33 scans were performed at CERN with the LPI 500MeV electron beam. The typical fluence per scan was  $1.8 \cdot 10^{13}$  electrons per  $\text{cm}^2$ . The total dose delivered at each scan was estimated to 160Gy. OSL was read after each scan and the response recorded on a digital scope. The diagram on Fig.10 presents the evolution of both the OSL peak and the signal integrated over the reading period.

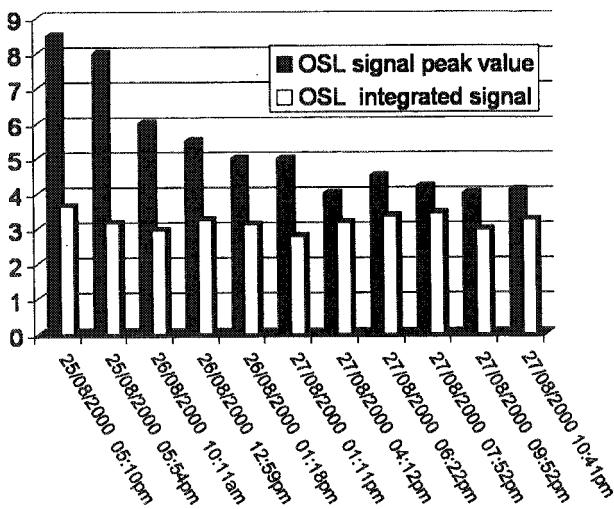


Fig. 10. Evolution of the peak integrated signal recorded during a series of irradiation runs at CERN with the 500MeV electrons of the LPI facility. The total dose for each run is 160Gy.

The online dosimeter developed for the remote monitoring of electron irradiation was designed in a way that exposes the stimulation LED as well as the OSL itself. The results presented in fig.10 indicate that the integrated signal remains constant within the uncertainties of the dose delivered, whereas the peak maximum is cut down by a factor of two after 5kGy. This result, demonstrates the decrease in the LED emission due to the displacement damage effect. It is in agreement with the model presented in section 3.3 where the peak value of the OSL is directly bound to the stimulation intensity whereas the total amount of luminescence recorded only depends on the total dose.<sup>29</sup>

The OSL dosimetry has been recommended for the CMS dosimetry. The system actually proposed consists of about one hundred OSL crystals connected individually to the same amount of photodiodes by optical fibers. The reading is performed sequentially, by stimulating a given detector and multiplexing the signals toward a central data acquisition system.

## **6. Conclusion**

A new generation of Optically stimulated materials has been synthesized at the University Montpellier II. The very high sensitivity of these phosphors, the quick time constant of the luminescence (less than 1ns) and the stimulation perfectly separated spectra enable many applications in real time and online dosimetry. We have developed an integrated sensor to measure the dose received orbit by orbit by a satellite. In radiotherapy, OSL has been used to control the dose deposited during intra-operative *in-vivo* irradiations. At CERN, we have proposed an online system to monitor the dose simultaneously in about 100 locations inside the Compact Muon Solenoid CMS experiment. Our OSL materials have also found many other applications shaped as films. They have made possible the mapping of a dose in complex geometries with a resolution of 50 $\mu$ m. OSL films have been used for the quality control of radio-surgery devices like the Gamma Knife. Beam profiles can be easily recorded with a variety particles ranging from protons, electrons, photons, and pions. Recently, the OSL materials have been adapted to neutron dosimetry. The future of the OSL relies on the fabrication of thin layer directly on active pixel sensors, or any other fast photo detector that could take advantage of the ns time constant, to push further the limits of what we call the real time dosimetry.

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