# **Schematic**

IC1 battery charger part number is LTC4162-L42 this variant is non-programmable with Maximum Power Tracking enabled by default. Therefore Pins 12,13,14 is unused.

SMBALERT (Pin 12), SCL (Pin 13), SDA (Pin 14), DVCC(Pin 15) not used safe to leave it floating.

### **Input Solar Current Regulation:**

**CLN (Pin 4)** negative terminal of the sense resistor **RSNSI**

**CLP (Pin 5)** positive terminal of **RSNSI**

32 mV is default sense threshold from datasheet.

Power dissipation:

**Chosen resistor:** PE1206FRM070R06L

* ±75ppm/°C changes less with temperature fluctuations more precise.
* 0.25W, 1/4W more than calculated power dissipation.

### **Battery Current Measurement:**

**CSN (Pin 20)** negative terminal **RSNSB**

**CSP (Pin 21)** positive terminal **RSNSB**

Chosen battery is 1100 mAh LiPo cell. Max Charge 0.5C but using standard Charge 0.2C for safety and battery longevity.

Recommended Maximum Discharge Current: 0.5C = 550mA

### **Battery Temperature (NTC Thermistor) Measurement:**

**NTC (Pin 10)** Thermistor input. Monitor the battery temperature.

**NTCBIAS (Pin 9)** thermistor output. The LTC4162 applies 1.2V to this pin during NTC measurement and expects a thermistor β value of 3490K.

A low drift bias resistor **RNTCBIAS** is required from NTCBIAS to NTC.

**RNTCBIAS** should be a 1% or better resistor

**RNTCBIAS** must be value equal to the value of thermistor **RNTC** at 25°C

**RNTC** connects to NTC and GND.

**Chosen Thermistor:** 103AT-2

### **Cell Count:**

One battery so both **CELLS0 (Pin 17) and CELLS1 (Pin 18):** connect to **INTVCC (Pin 2)**.

### **Oscillator Synchronization:**

### **Alternate Thermistors and Biasing:**

### **Boost Capacitor:**

**BOOST (Pin 1)**

low ESR surface mount ceramic type

rated to at least 6.3V

value of 22nF.

**SW (Pin 25, 26)** pins deliver power from the VOUT pins to the battery.

Inductor connected from SW to a sense resistor at CSP.

### **Switching Frequency (RT Resistor):**

LTC4162 has been optimized to run at 1.5MHz with an RT value of 63.4kΩ.

### **Inductor:**

### Choosing inductor for use with the LTC4162's internal buck regulator. **VIN** is 5.5V because it is maximum chosen solar panel outputs.

Ferrite cores for their very low core loss at frequencies above 100kHz which is the operating frequency of the LTC4162.

But ferrite cores saturate hard. If over the rated current, inductance drops suddenly which is bad for ripple and regulation.

Therefore, inductor must have saturation current at least 30% higher than max charge current.

**Chosen inductor: MLZ2012M1R0HT000**

* 100mOhm DCR good efficiency
* 700mA saturation current
* 1 µH±20%

**VOUT, BATSENS+, INTVCC and VCC2P5 Bypass Capacitors:**Capacitors determine important parameters, such as regulator control loop stability and input voltage ripple. MLCC for low ESR and ESL.

**BATSENS+ (Pin 19):** 10 µF, 1206, at least 6.3 V for Clean battery sensing

**VOUT (Pin 27, 28):** 22 µF, 1206, at least 10 V

**INTVCC (Pin 2):** 4.7 µF, at least 6.3 V

**VCC2P5 (Pin 8):** 1.0 µF, at least 4 V

### **INFET and BATFET MOSFET:**

The LTC4162 requires two external N-channel MOSFETs for input and battery power path control: INFET and BATFET.

Selected based on gate drive voltage, voltage rating, on-resistance, and power dissipation.

LTC4162 provides a 5 V gate drive for both MOSFETs.

**VGS** must fully conduct at 5 V

Low **RDS(ON)**to obtain the desired **VDS**. Keeps power dissipation low at full current.

INFET Connects/isolates the power source (VIN) from the charger.

* INFET **VDSS** must handle VBAT max 4.2V

BATFET Connects/isolates the battery from VOUT (system load)

* BATFET **VDSS** must handle VIN max 5.5V

**Chosen MOSFET: IRLML6344**

* Full enhancement at ~2.25V
* VDSS max 30 V
* Low **RDS(ON)**29 mΩ

Power dissipation (worst case solar panel):

Very low well within the thermal capacity of IRLML6344.

### **Battery Leads:**

Battery is connected with battery leads. This introduces parasitic resistance due to wire length and connector impedance, which cause a voltage drop under load or charge current, leading to inaccurate voltage sensing by the charger.

Therefore 10 µF ceramic capacitor is placed near the BATSENS+ pin to stabilize sensing and filter high-frequency noise.

### **Solar Panel Input Impedance Correction:**

Solar panels have different behaviour based on lighting and voltage region.

When the LTC4162 tries to track the maximum power point of the solar panel. It varies the load to find where power = voltage × current is highest. Maximum power point is the knee of the I-V curve. Left of MPP is constant current region. Right of MPP is constant voltage region.

A diagram of a voltage

AI-generated content may be incorrect.

In its constant voltage region is has low impedance and in its constant current region very high impedance.

To stabilise the LTC4162’s behaviour need a RC circuit. 100 µF to 1000 µF capacitor to ground after the resistor. Capacitor should be polymer electrolytic or solid tantalum at 16 V rated cap because chosen panel is 5.5V. Also need small ceramic capacitor 0.1 µF in parallel for high frequency filtering. 2.5 Ω resistor in series.

### **Battery and Input Voltage Hot Plugging:**

Hot plugging (sudden connection) a battery or solar panel can cause Large inrush current and Voltage overshoot at **VOUT (Pin 27, 28)**.

**VOUT (Pin 27, 28):** 10 µF MLCC, polymer electrolytic or solid tantalum 100 µF to 1000 µF, TVS diode.

### **LTC4162-L protection:**

To protect the LTC4162 charger and system from potential reverse voltage connection at the solar panel input, the MAX40200 is used between the panel and the charger’s VIN pin.

Unlike Schottky diodes the MAX40200 ensures minimal loss.