

Intelligent Design of Electronic Assets (IDEA)

&

Posh Open Source Hardware (POSH)

Andreas Olofsson

Program Manager, DARPA/MTO

Proposers Day
Mountain View, CA
9/22/17





Proposers day agenda

Start	End	Item
8:00 AM	8:15 AM	ERI Introduction
8:15 AM	9:00 AM	IDEA Program
9:00 AM	9:30 AM	POSH Program
9:30 AM	9:45 AM	Proposal Guidance
9:45 AM	9:55 AM	Morning Break
9:55 AM	10:45 AM	DARPA Contracting
10:45 AM	10:50 AM	DARPA Commercialization
10:50 AM	12:05 AM	IDEA and POSH Q&A
12:05 PM	12:45 PM	Lunch
12:45 PM	5:00 PM	One on One Meetings



Afternoon meeting schedule (1/2)

Start	End	Potential Performer
12:45 PM	12:55 PM	Qualcomm
12:55 PM	1:05 PM	Qualcomm
1:05 PM	1:15 PM	CMU
1:15 PM	1:25 PM	University of Minnesota
1:25 PM	1:35 PM	Princeton
1:35 PM	1:45 PM	IBM
1:45 PM	1:55 PM	NVIDIA
1:55 PM	2:05 PM	UCB
2:05 PM	2:15 PM	Intrinsix
2:15 PM	2:25 PM	ISI
2:25 PM	2:35 PM	Arteris
2:35 PM	2:50pm	Afternoon Break

Future meetings or teleconferences with the PM may be requested through email to HR001117S0054@darpa.mil

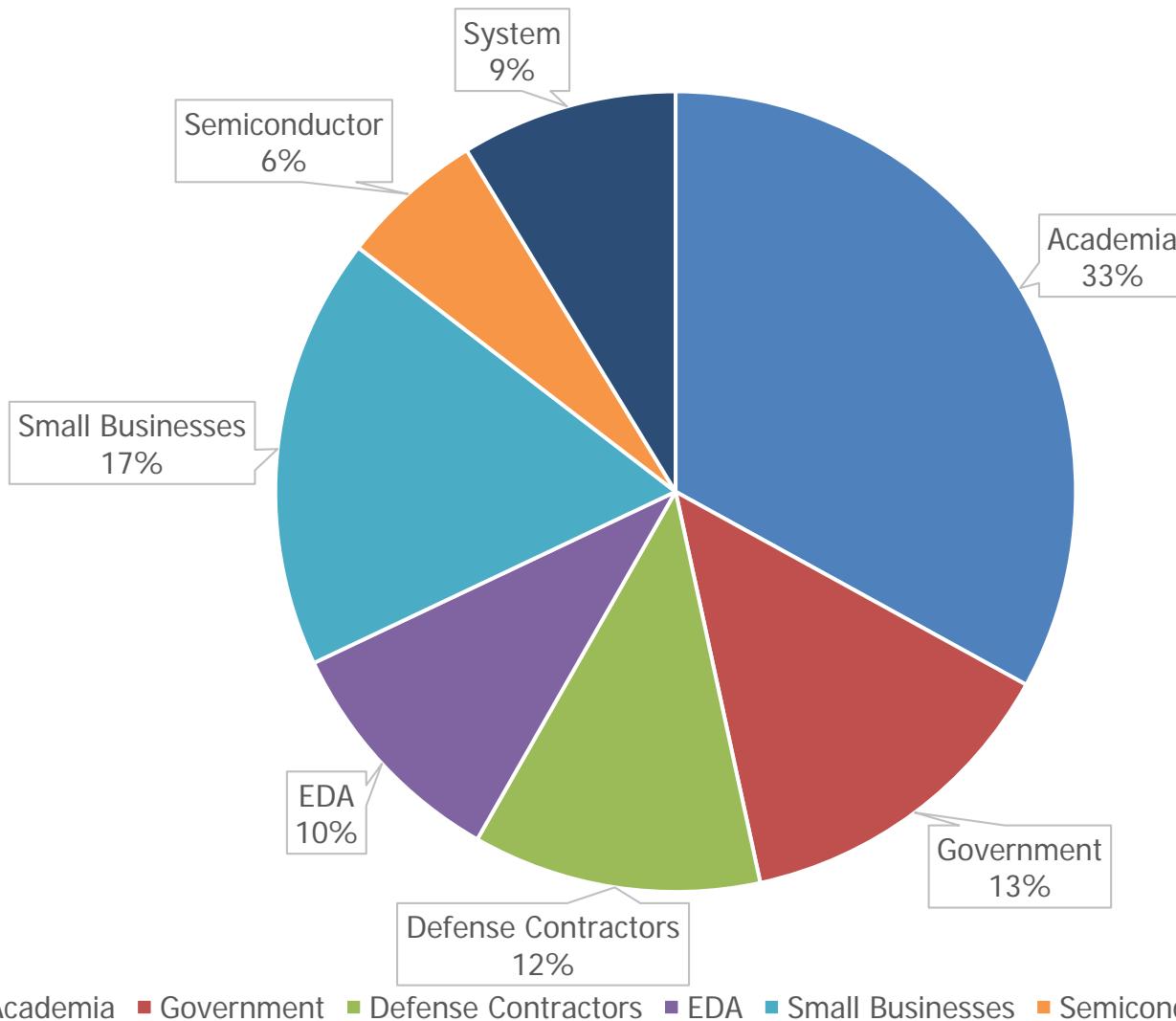


Afternoon meeting schedule (2/2)

Start	End	Potential Performer
2:50 PM	3:00 PM	Stanford
3:00 PM	3:10 PM	SRI International
3:10 PM	3:20 PM	Rockwell/Stanford/Totic
3:20 PM	3:30 PM	Stanford
3:30 PM	3:40 PM	USC
3:40 PM	3:50 PM	Banpil Photonics
3:50 PM	4:00 PM	JITx
4:00 PM	4:10 PM	Princeton
4:10 PM	4:20 PM	Accelerated Tech
4:20 PM	4:30 PM	Cadence
4:30 PM	4:40 PM	UCB
4:40 PM	4:50 PM	Berkeley National Lab
4:50 PM	5:00 PM	Close

Future meetings or teleconferences with the PM may be requested through email to HR001117S0054@darpa.mil

Attendance summary





Question & Answer session

- Answers to questions will be made available as a new attachment to the BAA
- Questions may be submitted at a later date to HR001117S0054@darpa.mil

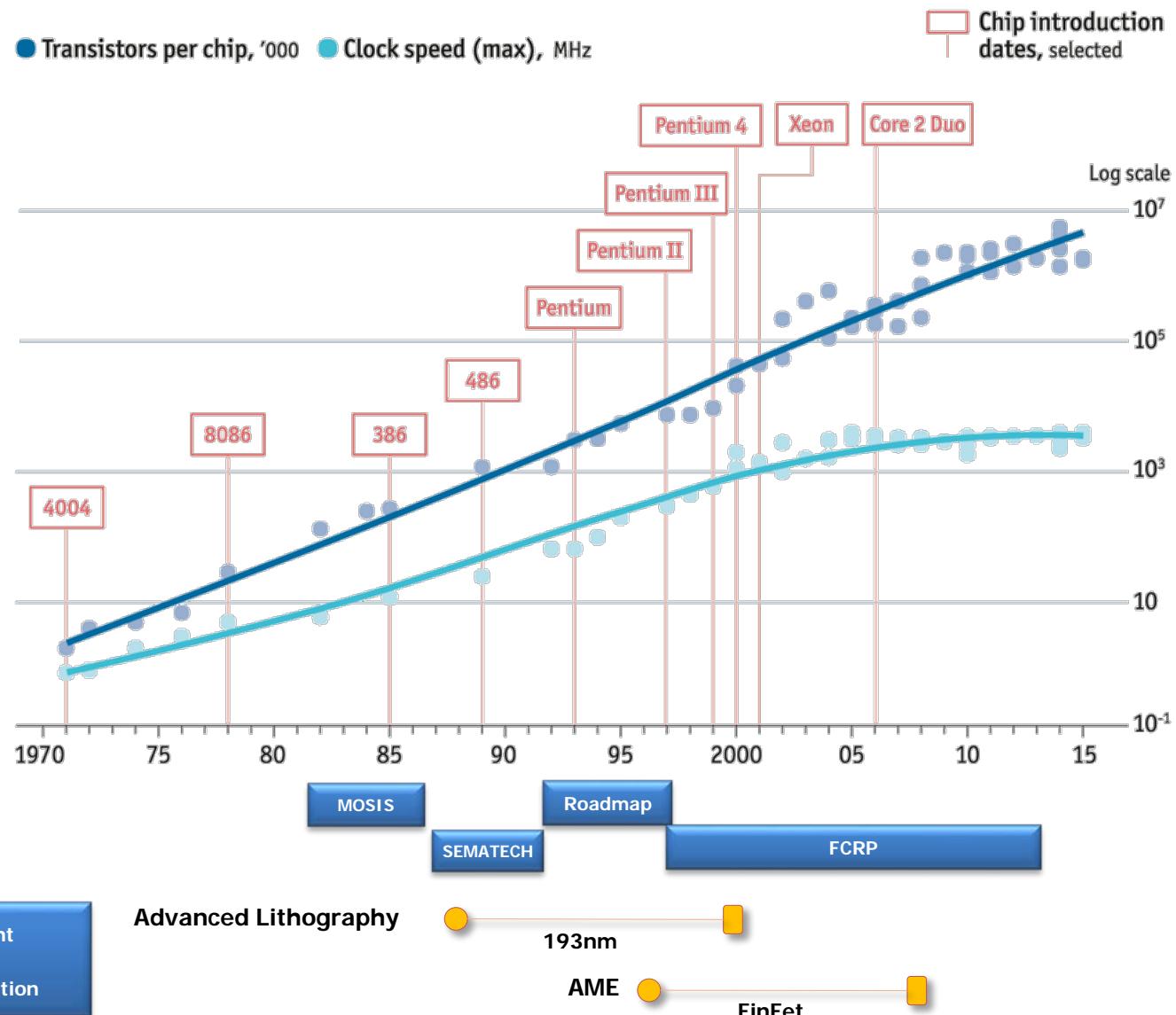


Electronic Resurgence Initiative (ERI)

Introduction

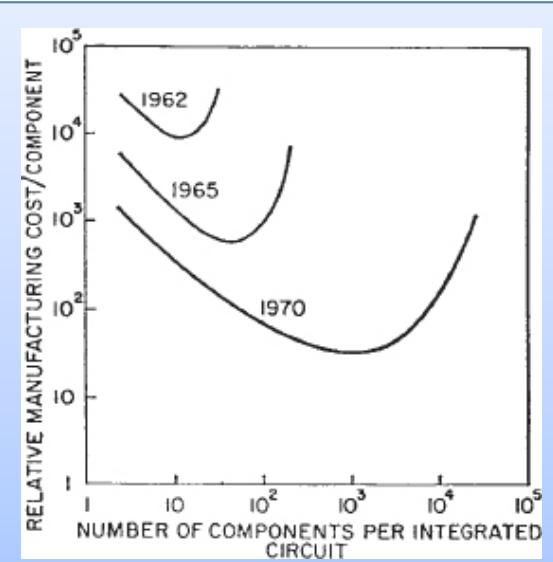


The miracle of Moore's Law has taken us incredibly far...





Page 2 set us on a 50 year journey



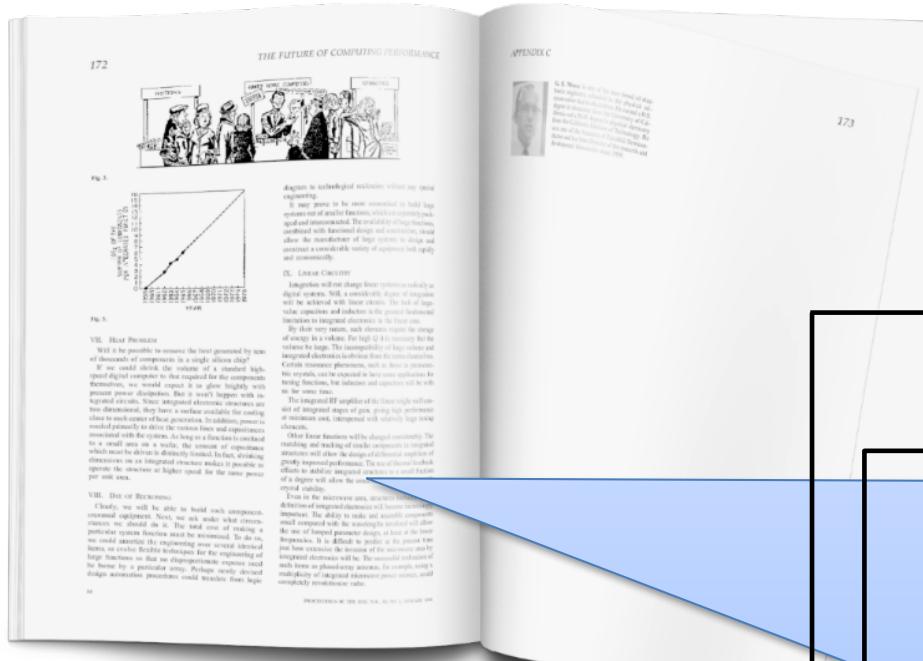
Electronics, April 19, 1965: Cramming More Components onto Integrated Circuits; Gordon Moore

P.1

"...The complexity for minimum component costs has increased at a rate of roughly a factor of two per year (see graph)..."



...but it's time to turn to "Page 3"



Electronics, April 19, 1965: Cramming More Components onto Integrated Circuits; Gordon Moore

P.3

Architecture

Maximizing specialized functions

Design

Quickly enabling specialization

Materials & Integration

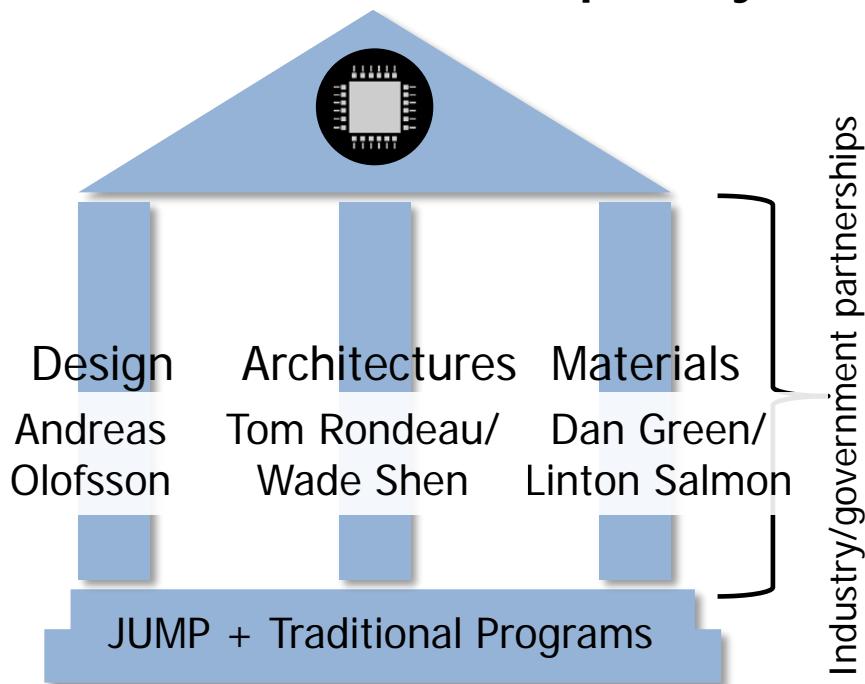
Adding separately packaged novel materials and using integration to provide specialized computing

VIII. DAY OF RECKONING

Clearly, we will be able to build such component-crammed equipment. Next, we ask under what circumstances we should do it. **The total cost of making a particular system function must be minimized.** To do so, we could amortize the engineering over several identical items, or **evolve flexible techniques for the engineering of large functions** so that no disproportionate expense need be borne by a particular array. Perhaps **newly devised design automation procedures could translate from logic diagram to technological realization** without any special engineering.

It may prove to be **more economical to build large systems out of smaller functions, which are separately packaged** and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

2025 – 2030 National Electronics Capability



\$141M in Current Efforts (FY18)
\$75M of New Page 3 Funding (FY18)

Resting on a foundation of existing research programs are newly formulated thrusts that all sum into the Electronics Research Initiative, a four-year push with anticipated annual investments in the \$200 million range.

Page 3 Investments

- **Design**

How do we lower the design barrier to specialization?

- **Architectures**

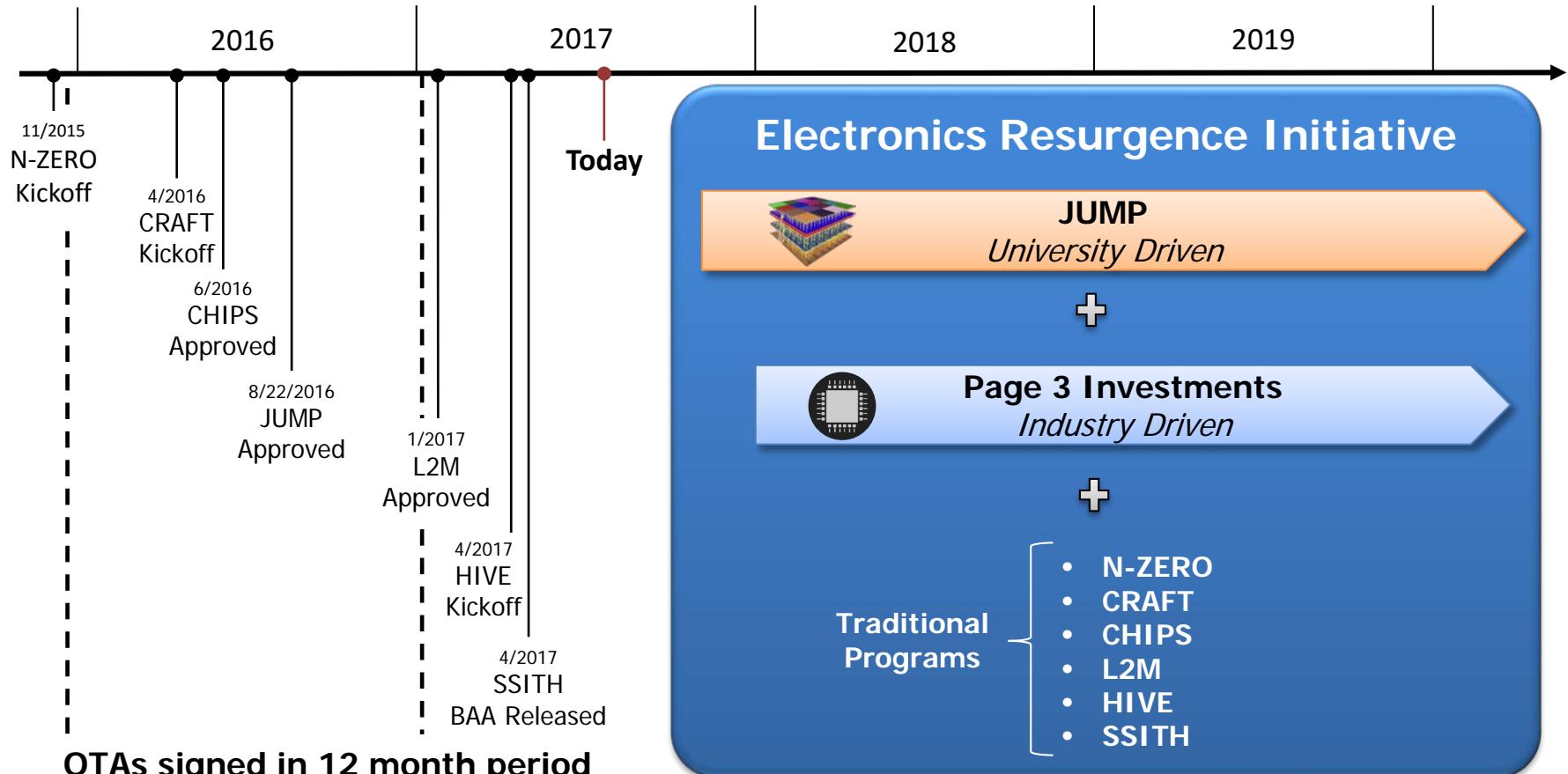
How do we manage the complexity of specialization with new architectures?

- **Materials**

How do we integrate new materials for specialized functions?



Recent DARPA investments and momentum



A horizontal list of company names involved in DARPA investments, grouped into two columns:

Intel	Qualcomm	Rambus	XILINX	Micron
Cadence	Keysight Technologies	NVIDIA	Flexlogix Technologies, Inc	



ERI “Page 3” program service announcement

Materials & Integration

- *Monolithic Integration of an SoC in Three Dimensions (3DSoC)*, Linton Salmon
- *Framework for Novel Compute (FRANC)*, Daniel Green

Architecture:

- *Software Defined Hardware (SDH)*, Wade Shen
- *Domain-Specific System on Chip (DSSoC)*, Thomas Rondeau

Design

- *Intelligent Design of Electronic Assets (IDEA)*, Andreas Olofsson
- *Posh Open Source Hardware (POSH)*, Andreas Olofsson

Press Release: <http://www.darpa.mil/news-events/2017-09-13>

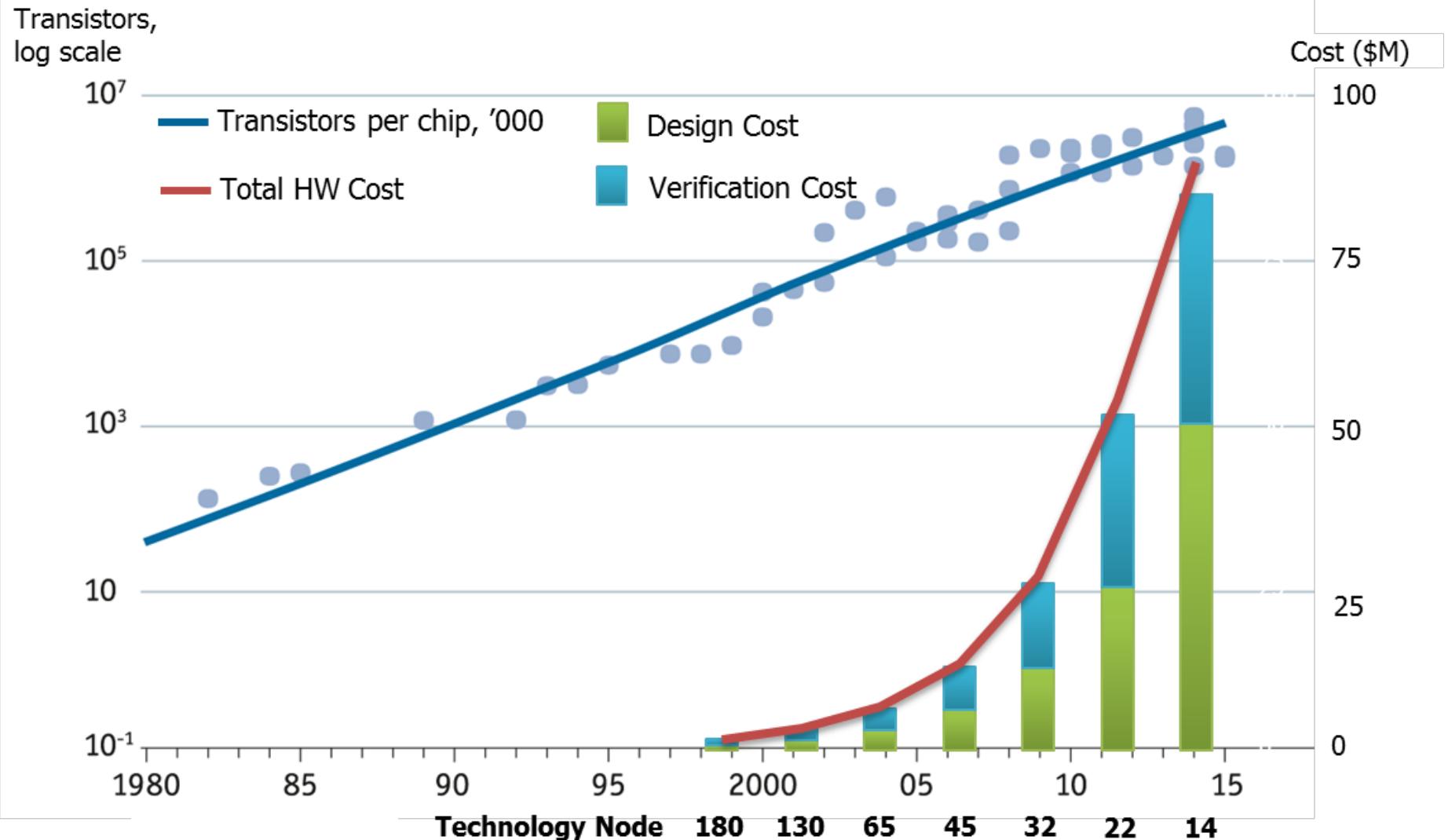
Proposers Day: <https://www.fbo.gov/spg/ODA/DARPA/CMO/DARPA-SN-17-75/listing.html>

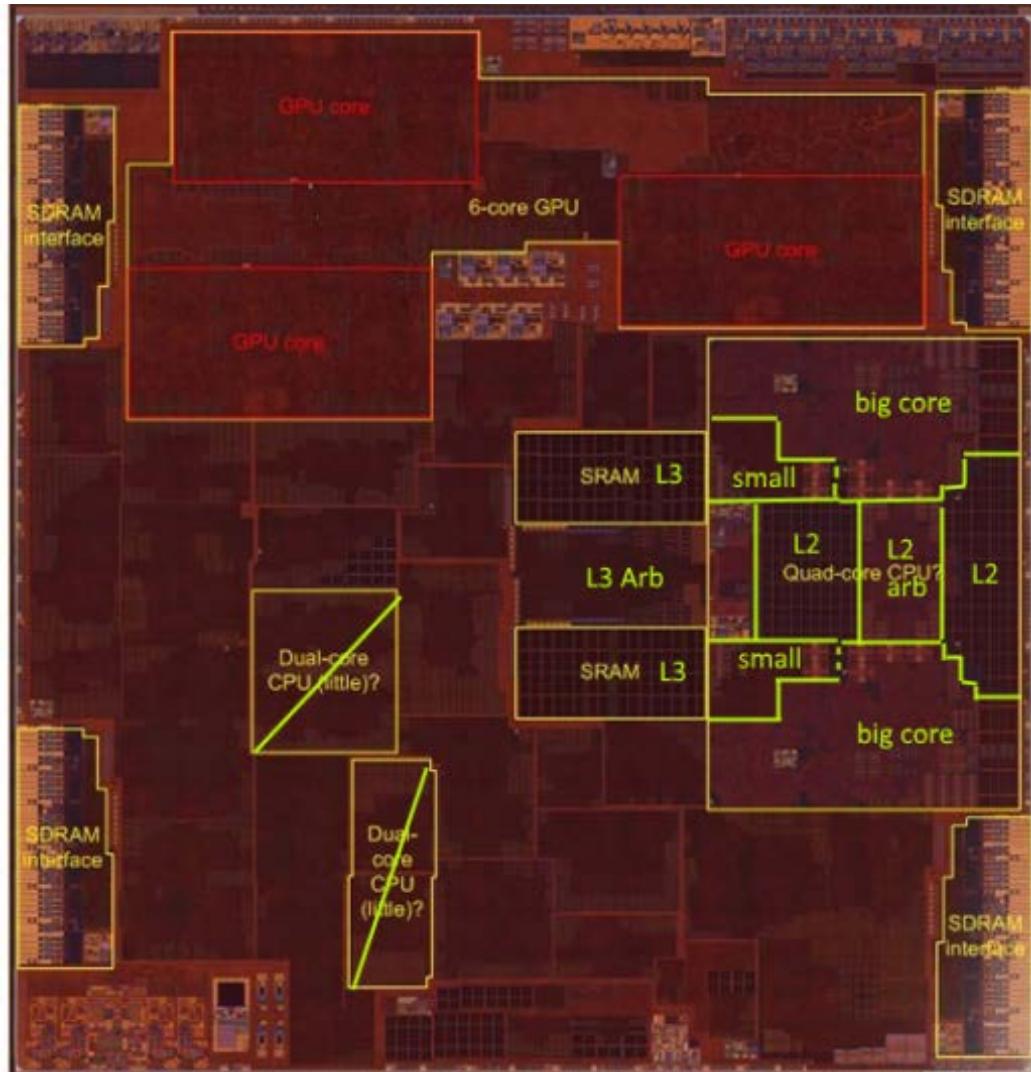
Design BAAs: <https://www.fbo.gov/spg/ODA/DARPA/CMO/HR001117S0054/listing.html>



Lowering The Hardware Innovation Barrier

The curse of Moore's Law



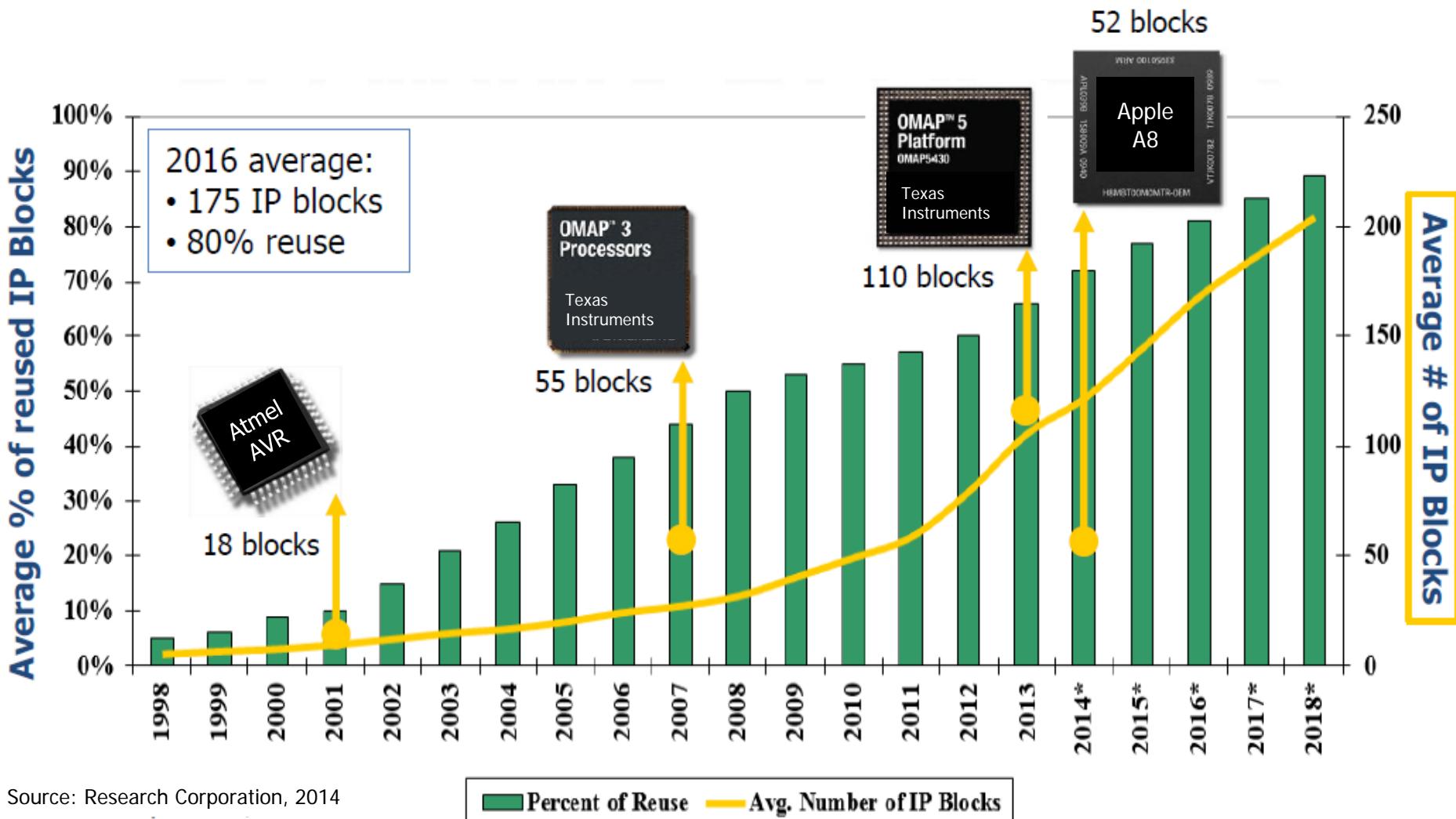


Source: TechInsights/Chipworks

Q: How much does it cost to produce 10,000 125mm² SoCs at 16nm?

A: <\$2M

Root cause: complexity growth

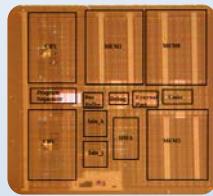


Source: Research Corporation, 2014

Percent of Reuse — Avg. Number of IP Blocks

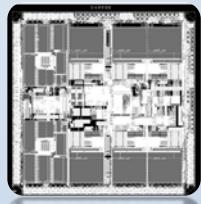
My personal chip history

Transistors/Hour



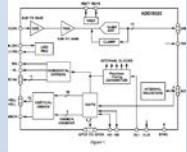
TS101

130nm
1 CPU
45M xtors
30Eng*24M



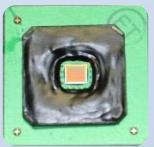
TS201

130nm
1 CPU
50M xtors
100Eng*24M



AD9020

350nm
1 CPU
<1M xtors
1Eng*3M



E1

65nm
16 CPUs
50M xtors
1Eng*2M



E2

65nm
16 CPUs
50M xtors
3Eng*3M



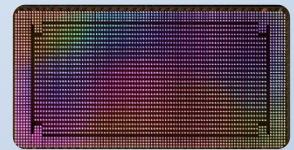
E3

65nm
16 CPUs
50M xtors
3Eng*3M



E4

28nm
64 CPUs
200M xtors
3Eng*12M



E5

16nm
1024 CPUs
4.5B xtors
1Eng*12M

1999

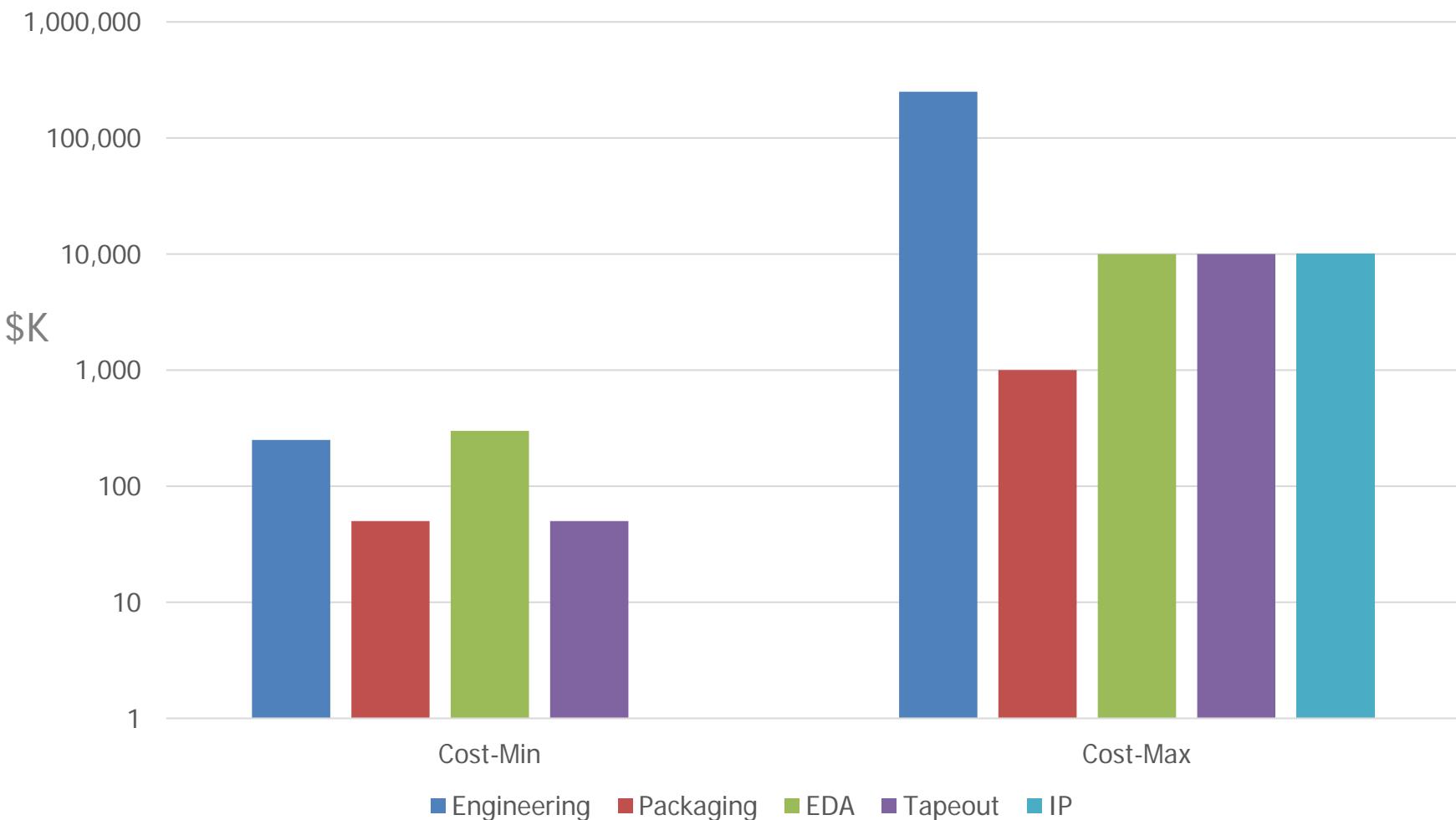
<http://www.analog.com>
<http://www.adapteva.com>
<http://www.ieee.org>

2007

Distribution Statement "A" (Approved for Public Release, Distribution Unlimited)

2016

Actual chip design costs



Source: A. Olofsson, "An Introduction to Semiconductor Economics", Oct 3, 2014

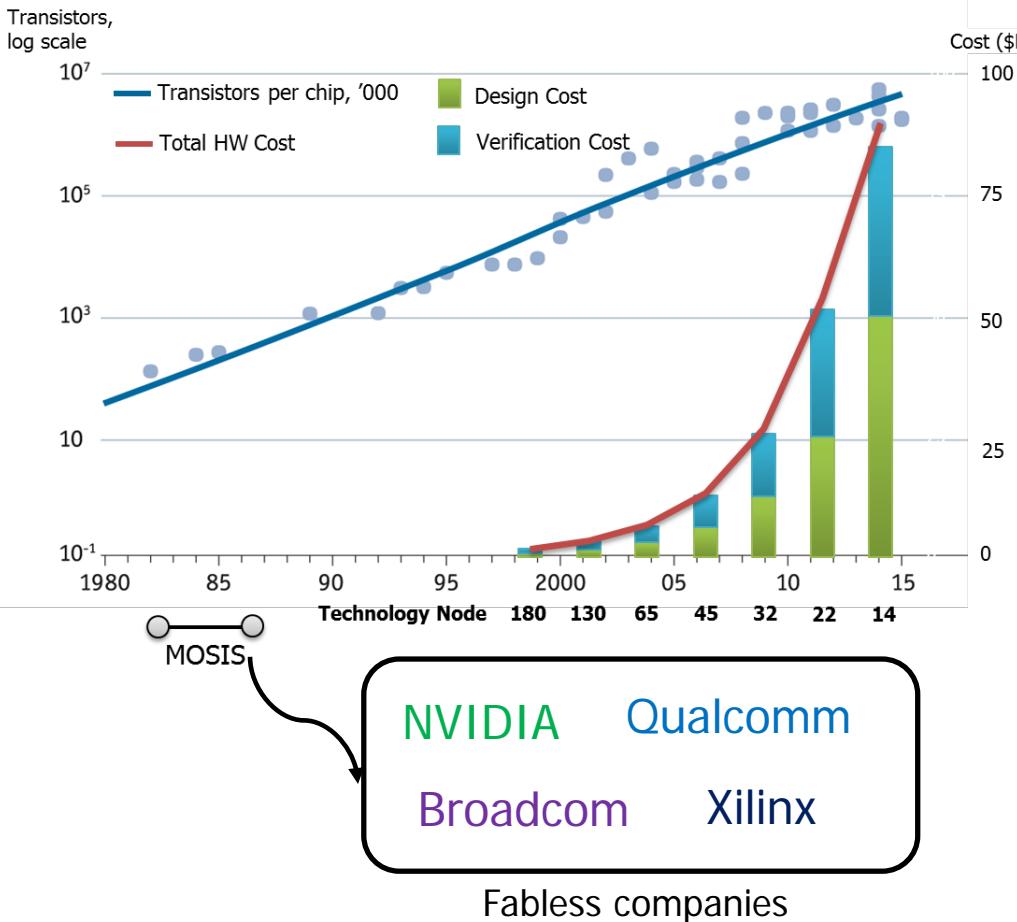


Cost of disrupting the industry

Challenge	Industry	Hurdle	Cost	Future
IP	\$5B	Risk	\$1M+	\$0?
EDA	\$10B	Complexity	\$1M+	\$0?
Engineering	\$20B?	Time	9 months	24hrs?
Packaging	\$13B	Logistics	\$50K	\$0?
Manufacturing	\$40B	Logistics	\$2M+	\$1,000?

Source: A. Olofsson, "Open Source Chip Design", OH Summit, Philadelphia, 2015

Lowering barriers to hardware innovation



New procedures for physical design and verification will lower the design barrier, enabling rapid specialization

Intelligent Design of Electronic Assets (IDEA)

- No human in the loop" 24-hour layout generation for mixed signal integrated circuits, systems-in-package, and printed circuit boards. Machine generated layout of electrical circuits and systems

Posh Open Source Hardware (POSH)

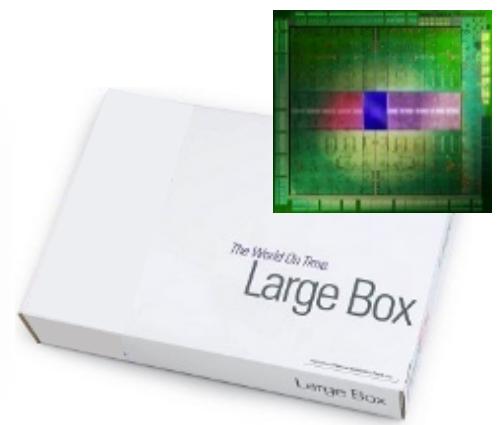
- An open source System on Chip (SoC) design and verification eco-system that enables cost effective design of ultra-complex SoCs.

The 1980's DARPA MOSIS effort removed fab cost and fab access barriers and launched the fabless industry. The ERI Design effort will address today's design complexity and cost barriers, creating the environment needed for the next wave of US semiconductor innovation.



My DARPA dream

```
$ git clone https://github.com/darpa/idea  
$ git clone https://github.com/darpa/posh  
$ cd posh  
$ make soc42
```





What if it works?



Intelligent Design of Electronic Assets (IDEA)

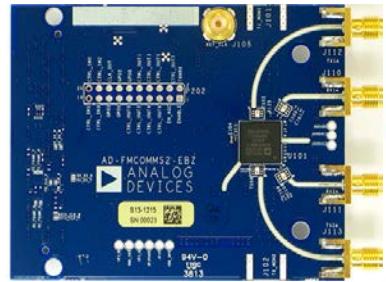


IDEA Objective

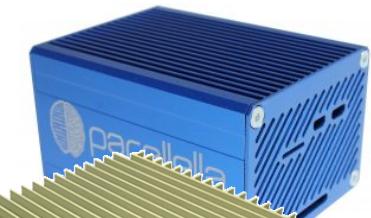
IDEA aims to create a “no human in the loop” 24 hour turnaround layout generator for System-On-Chips, System-In-Packages, and Printed Circuit Boards.



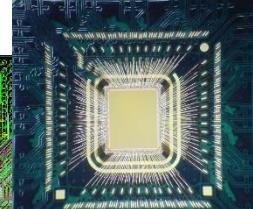
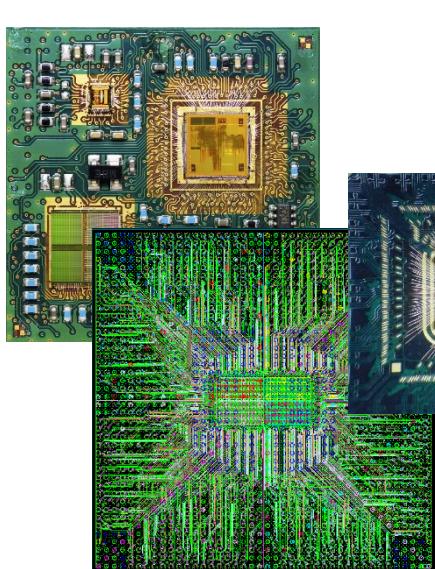
Can we replace manual labor with machines?



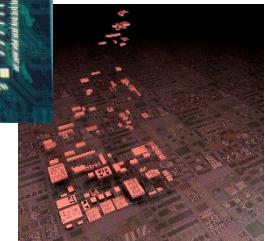
Boards



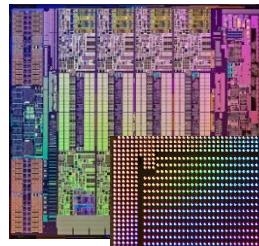
Boxes



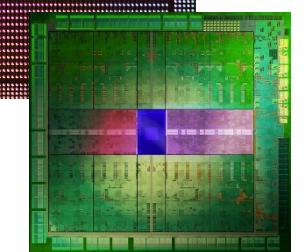
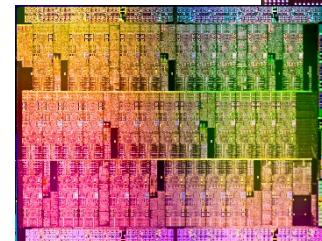
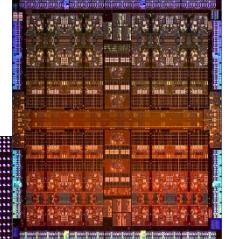
Packages



Machine-Generated Physical Objects



Chips



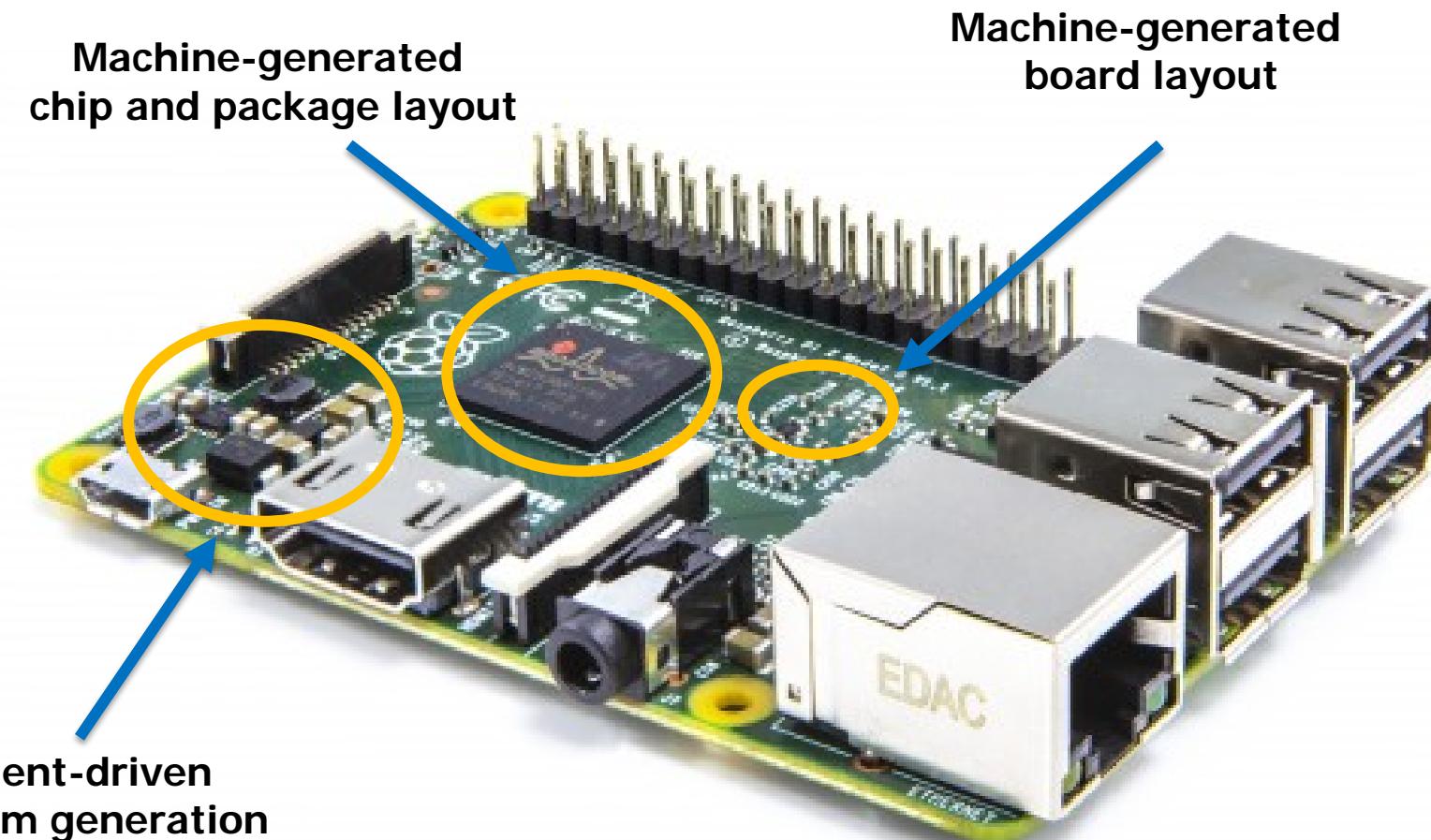
Sources: Axis, Adapteva

Sources: Intel, Oracle, NVIDIA

Distribution Statement "A" (Approved for Public Release, Distribution Unlimited)

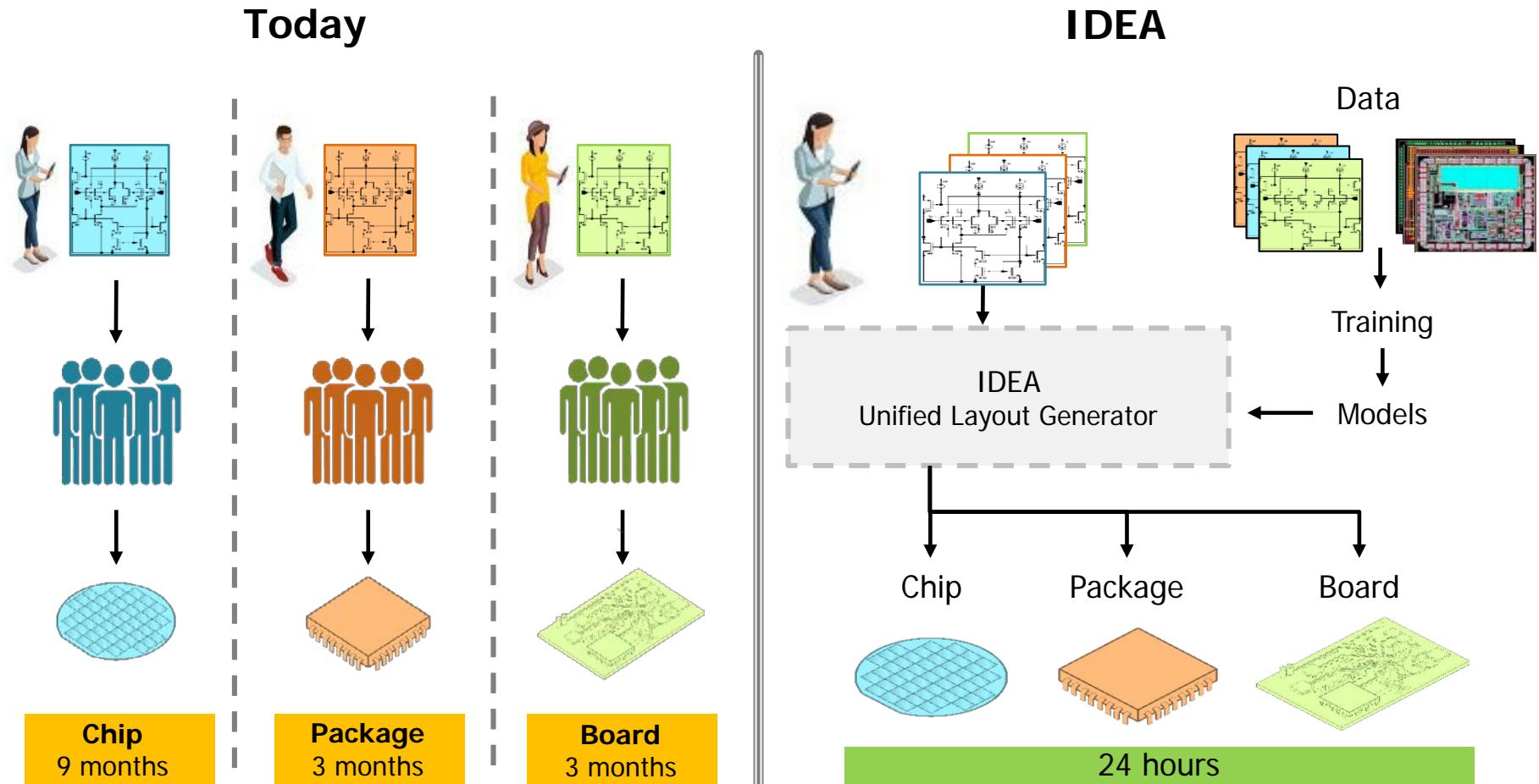
High level objectives

IDEA will completely automate the layout of electrical circuits and systems



Sources: Raspberry Pi

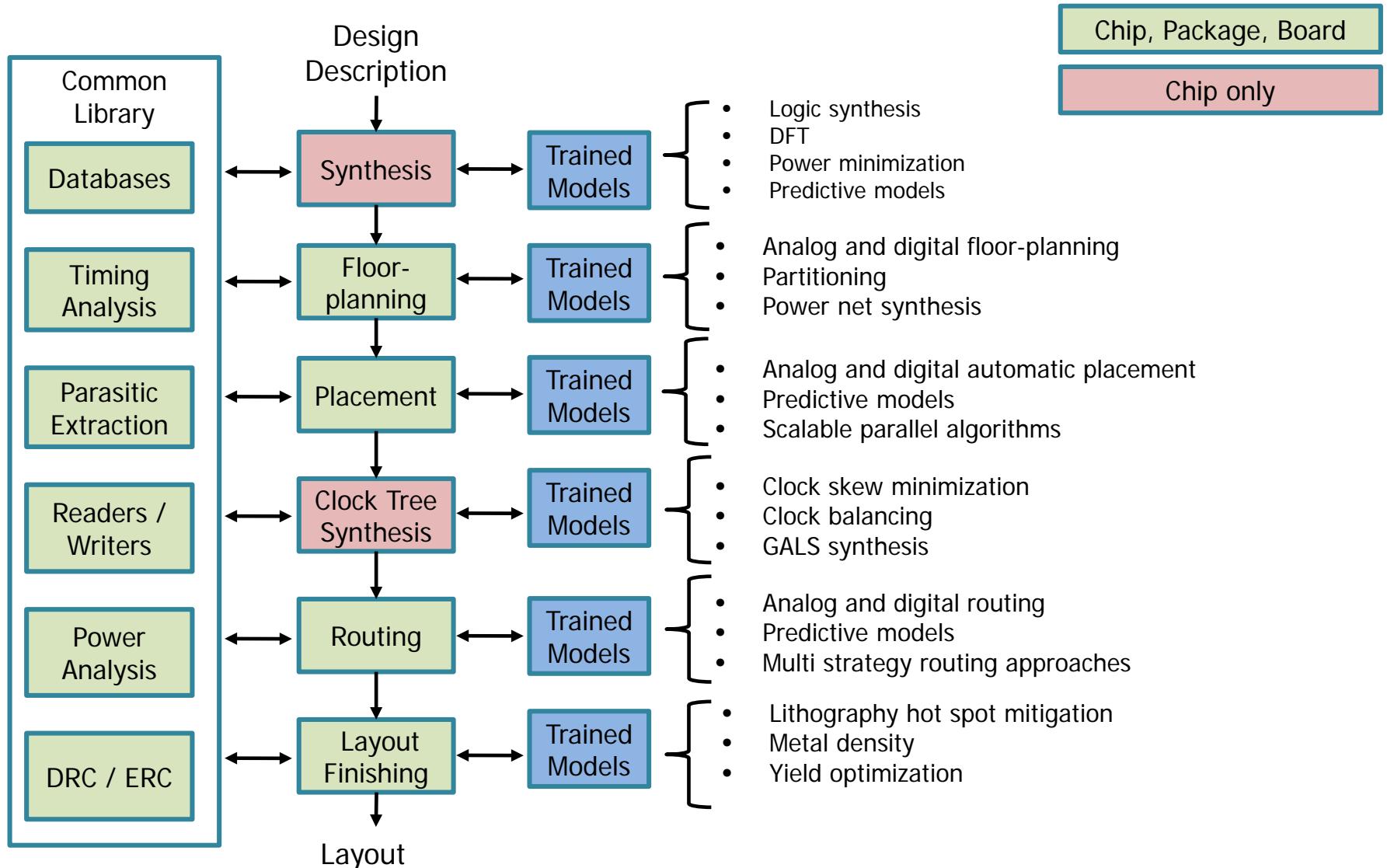
A unified electrical circuit layout generator



- Knowledge embedded in humans
- Limited knowledge reuse
- Reliance on scarce resources

- Knowledge embedded in software
- 100% automation
- 24 hour turnaround

Open EDA modularity

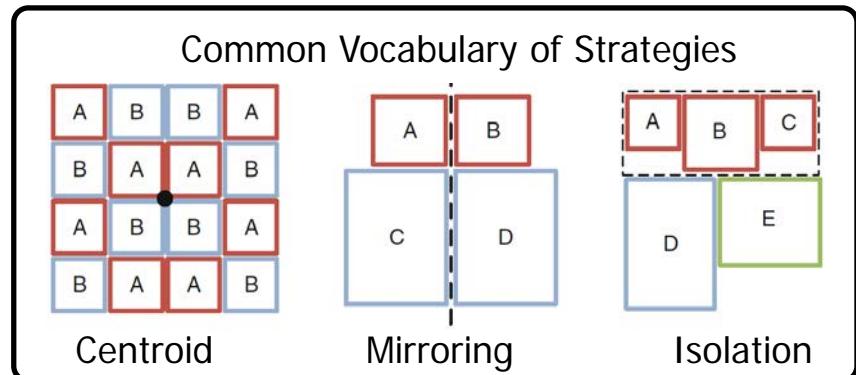
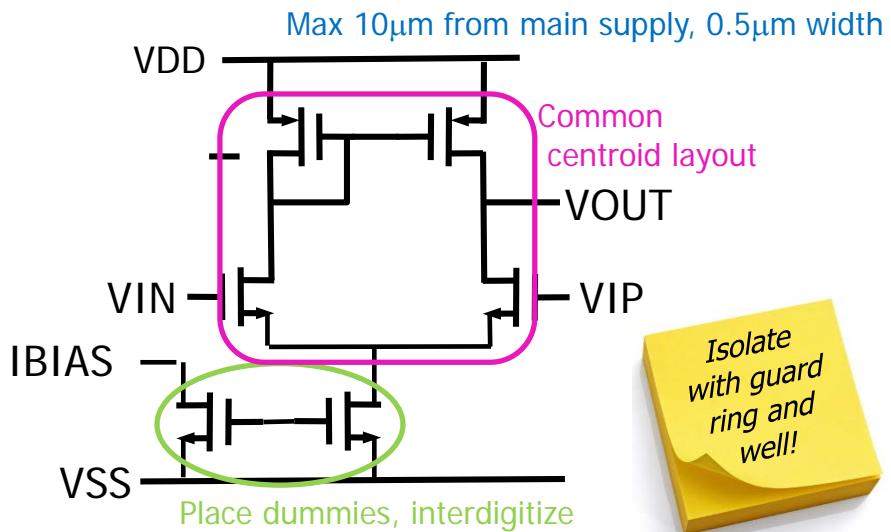




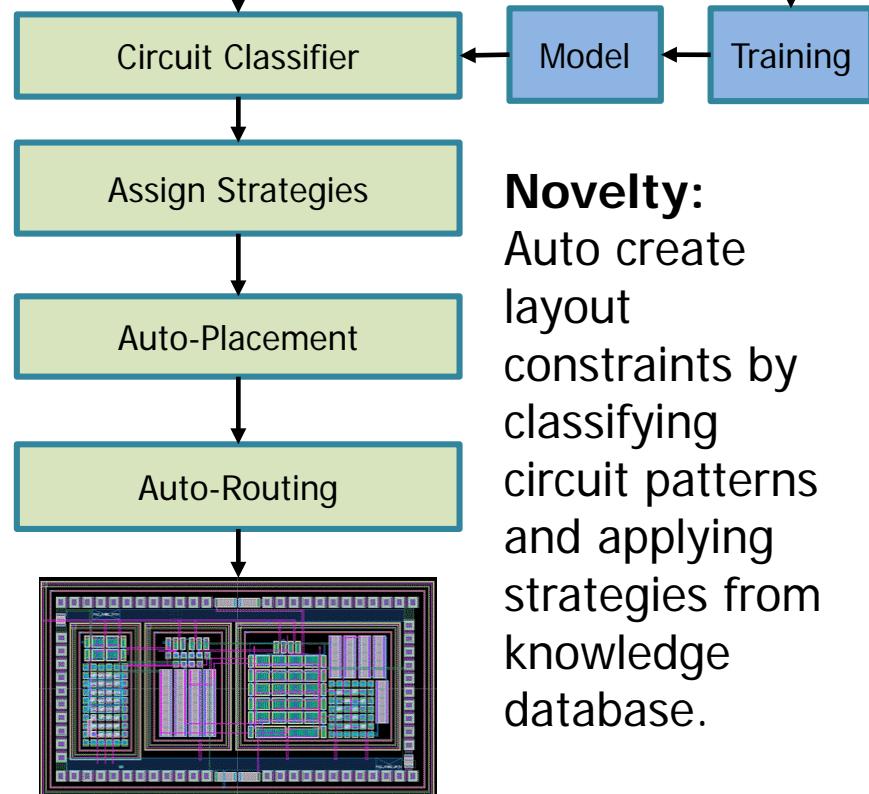
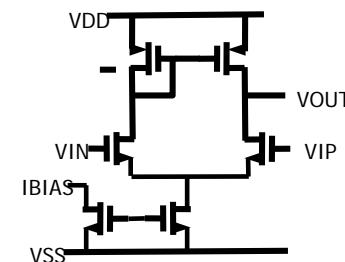
Fully automated digital AND analog layout!

Today

Designer provides manual constraints to layout person (or tool)



IDEA

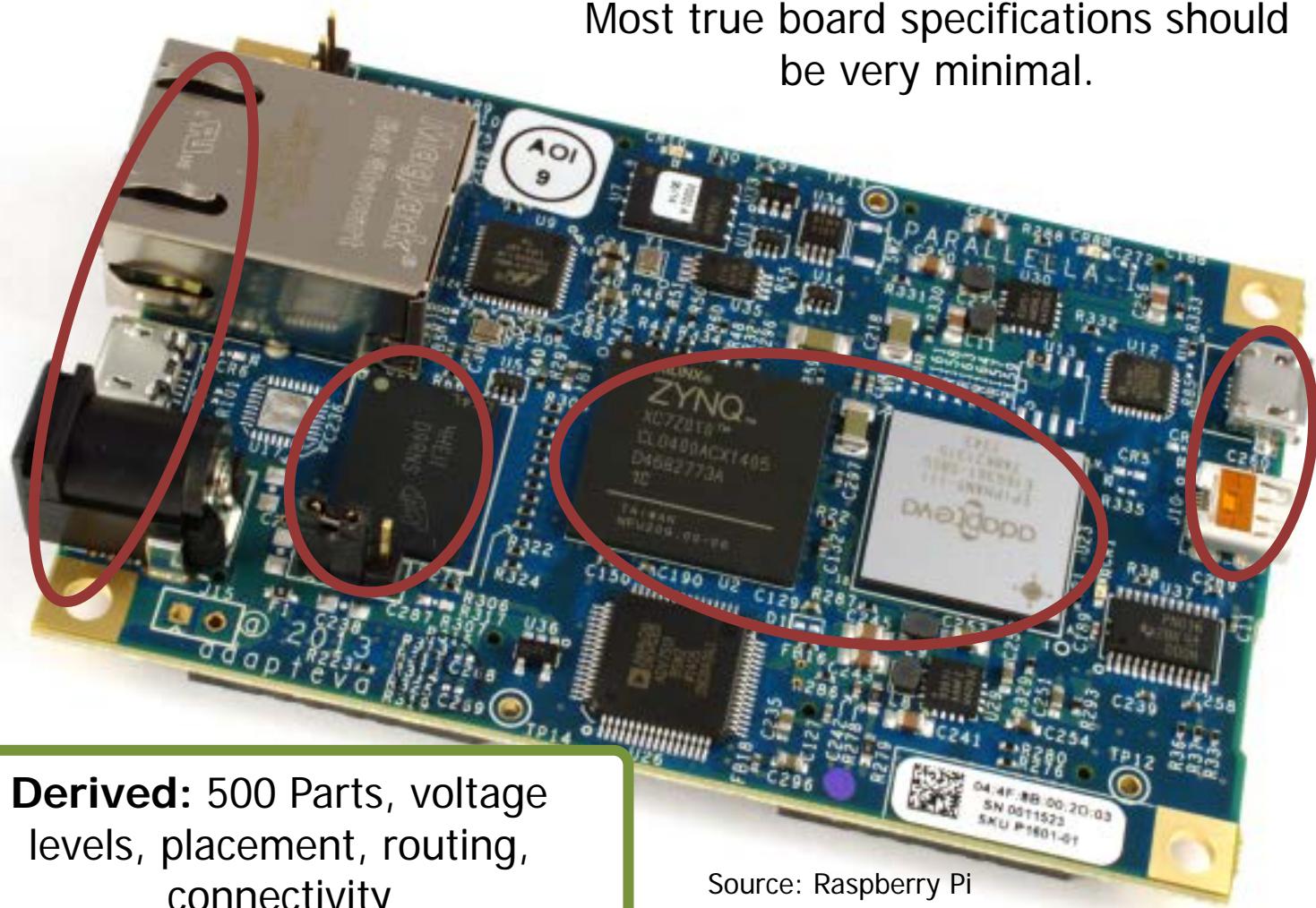


Novelty:
Auto create layout constraints by classifying circuit patterns and applying strategies from knowledge database.

True Specs:

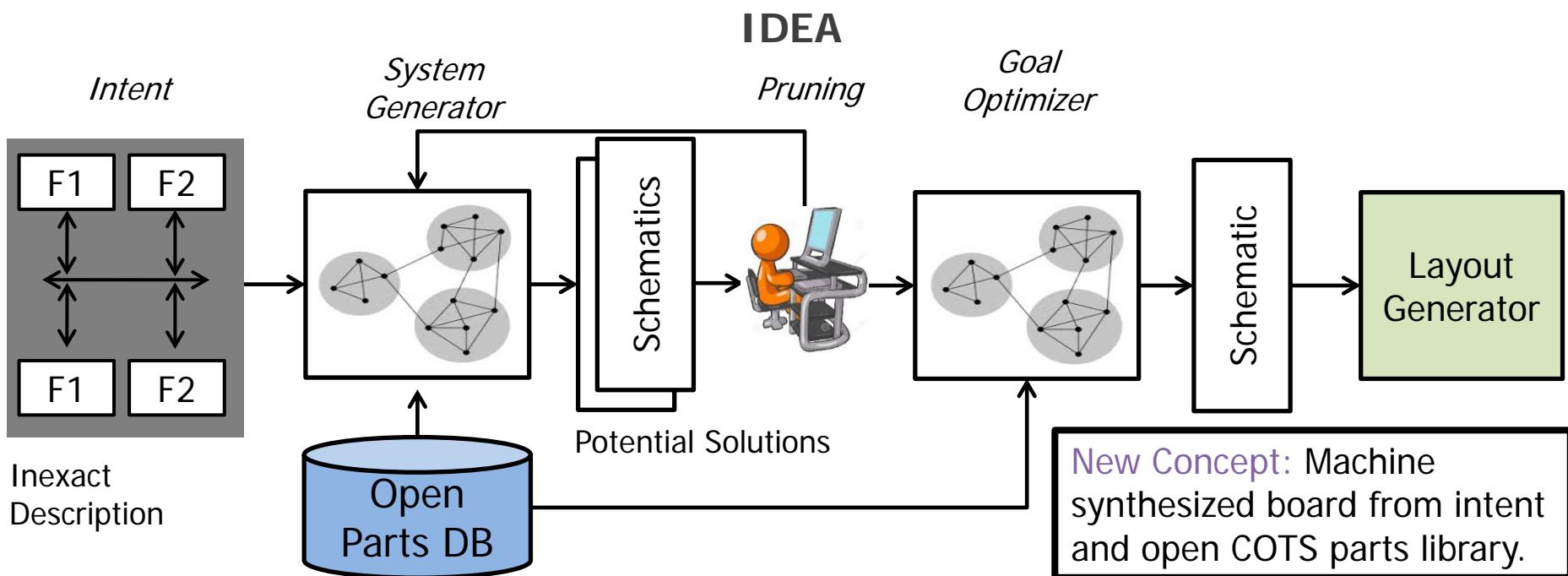
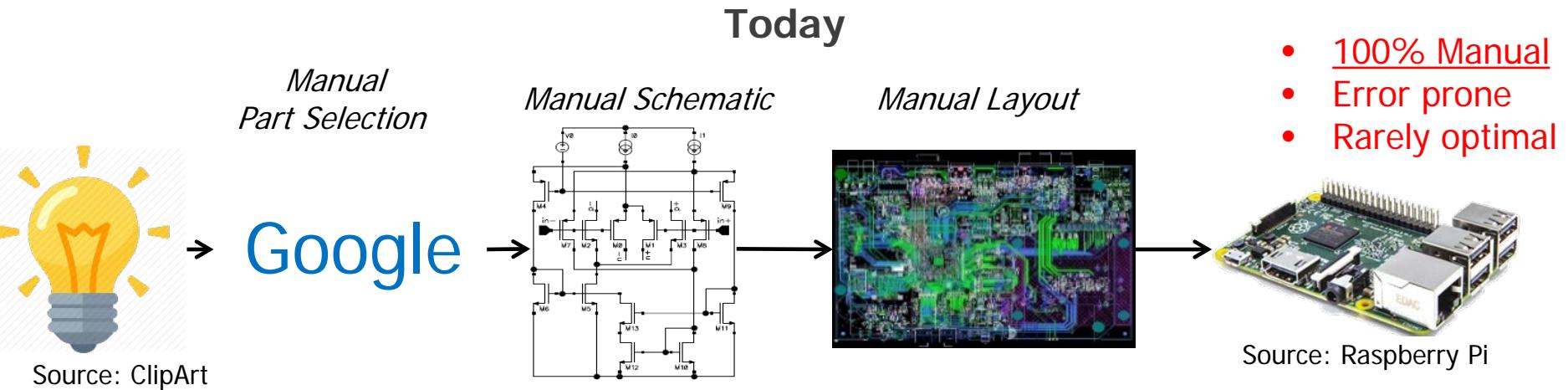
- 5V
- Ethernet
- USB
- HDMI
- 1GB RAM
- 128MB Flash
- FPGA
- 20 GFLOPS
- ARM A9

Intent: Specify what, not how!
Most true board specifications should
be very minimal.



Source: Raspberry Pi

Reinventing board development





An open 5M+ component IC database

Today

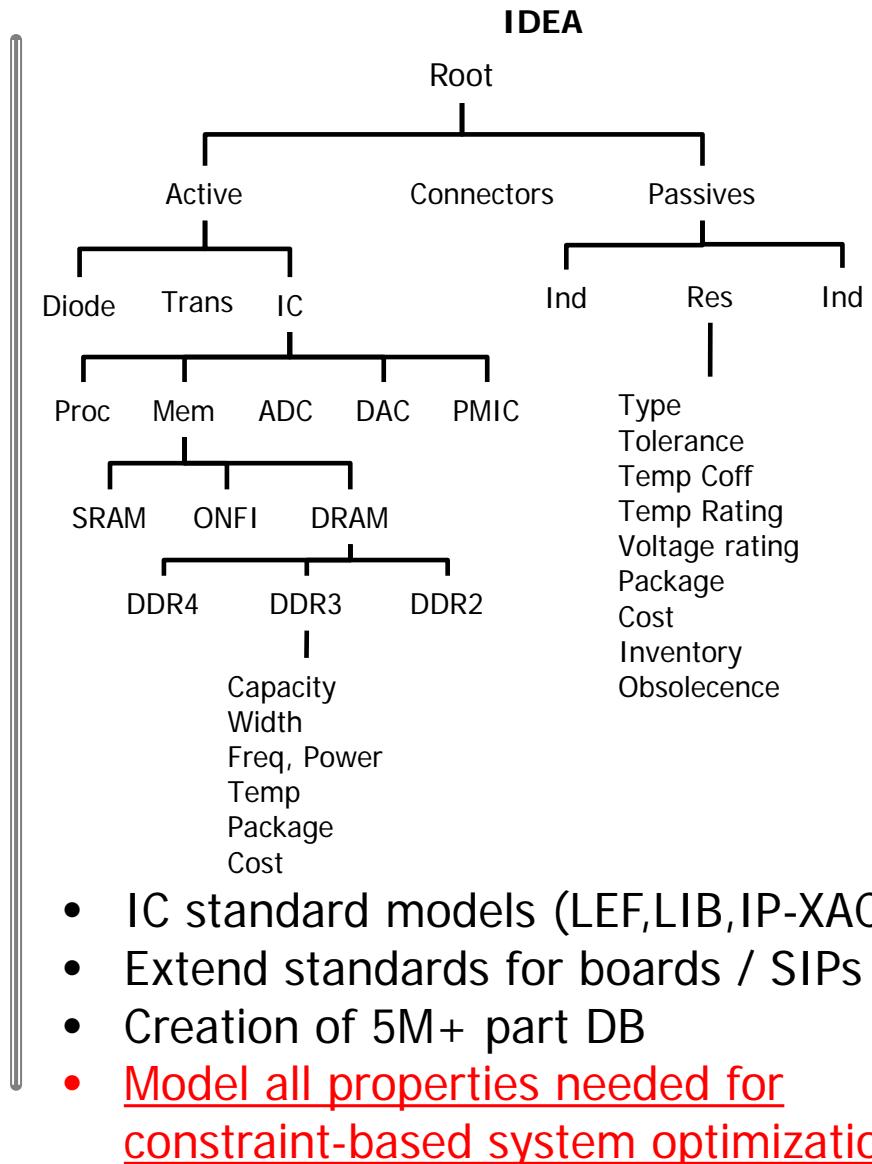
Texas Instruments
TPS65216x Power Management for ARM® Cortex™-A/B/A/B SoCs and FPGAs
Product Family Search & Technical Documents Tools & Resources Support & Documentation Reference Design

XILINX
DS191 (v1.18 April 2017)
Zynq-7000 All Programmable SoC (Z-7030, Z-7035, Z-7045, and Z-7100): DC and AC Switching Characteristics Product Specification

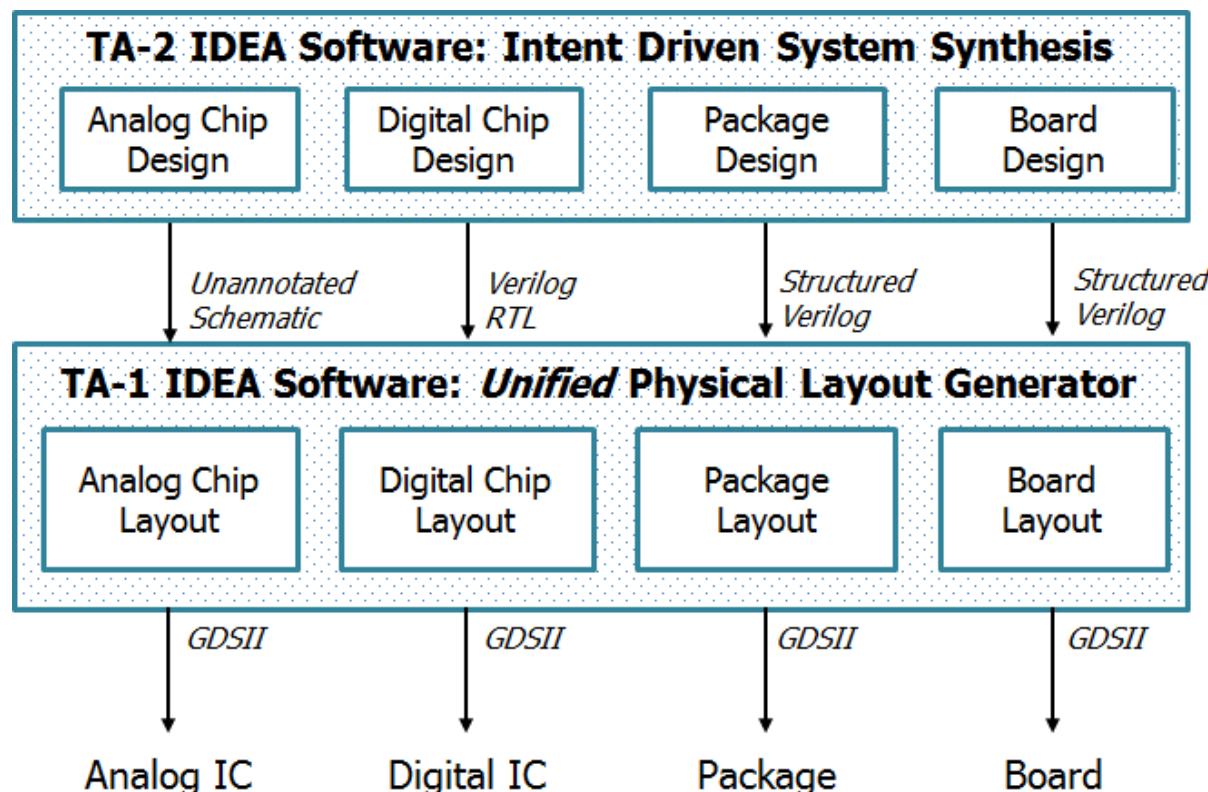
ANALOG DEVICES
RF Agile Transceiver AD9361
Data Sheet
FEATURES
• 2 x 2 transceiver with integrated 12-bit DACs and ADCs
• 16-bit parallel I/O up to 6 Gbps
• 16-bit parallel I/O down to 6 Gbps
• High dynamic range receiver
• Linearized channel bandwidths (200 MHz to 6 GHz)
• 16-bit DACs and ADCs with 14-bit resolution
• Internal receiver calibration
• Internal receiver noise cancellation
• Internal receiver noise floor
• TX receiver -1dB flatness grade (±0.5 dB) over the entire operating frequency range
• TX receiver -1dB flatness grade (±0.5 dB) over the entire operating frequency range
• 16-bit DAC maximum linearity (±0.5 dB) over the entire operating frequency range
• 16-bit ADC maximum linearity (±0.5 dB) over the entire operating frequency range
• 16-bit DAC digital interface
• 16-bit ADC digital interface
• Analog-to-digital conversion system
• Frequency synthesis and local oscillator
• Frequency synthesis and local oscillator
• General Description
GENERAL DESCRIPTION
The RF Agile Transceiver is a high performance, high linearity, and radio frequency (RF) lightwave transceiver designed for use in 5G and 6G wireless radio applications. Its programmability allows it to support multiple standards and frequencies. The RF Agile Transceiver is a complete transceiver solution that includes a TX and RX channel, a local oscillator, and a reference clock. The device contains a 10 foot wire and a flexible metal shielded housing designed for a compact form factor. The RF Agile Transceiver is designed for use in a wide range of applications, including base stations, small cells, and mobile devices. It features a high dynamic range analog-to-digital converter (ADC) and a digital-to-analog converter (DAC). The ADC has a sampling rate of 12.8 GSPS and the DAC has a sampling rate of 12.8 GSPS. The RF Agile Transceiver also features a high dynamic range receiver (RDR) and a high dynamic range transmitter (HDT). The RDR has a sampling rate of 12.8 GSPS and the HDT has a sampling rate of 12.8 GSPS. The RF Agile Transceiver is designed for use in a wide range of applications, including base stations, small cells, and mobile devices. It features a high dynamic range analog-to-digital converter (ADC) and a digital-to-analog converter (DAC). The ADC has a sampling rate of 12.8 GSPS and the DAC has a sampling rate of 12.8 GSPS. The RF Agile Transceiver also features a high dynamic range receiver (RDR) and a high dynamic range transmitter (HDT). The RDR has a sampling rate of 12.8 GSPS and the HDT has a sampling rate of 12.8 GSPS.

Source: data sheets from Xilinx, Analog Devices

- 5M+ parts in circulation
- Information embedded in datasheets and reference designs
- No standard models
- Automatic optimization not possible



- **TA1: Machine Generated Physical Layout:** Development of a unified physical layout generator for digital and analog SoCs, SiPs, and PCBs
- **TA2: Intent Driven System Synthesis:** Development of an intent-driven, correct-by-construction system generator





IDEA does NOT seek proposals for:

- Investigatory research that does not deliver useful software
- New manufacturing processes and technologies
- Architectures that simply reduce or remove the need for physical layout
- Development of high level languages, compilers, and generators for Boolean logic design



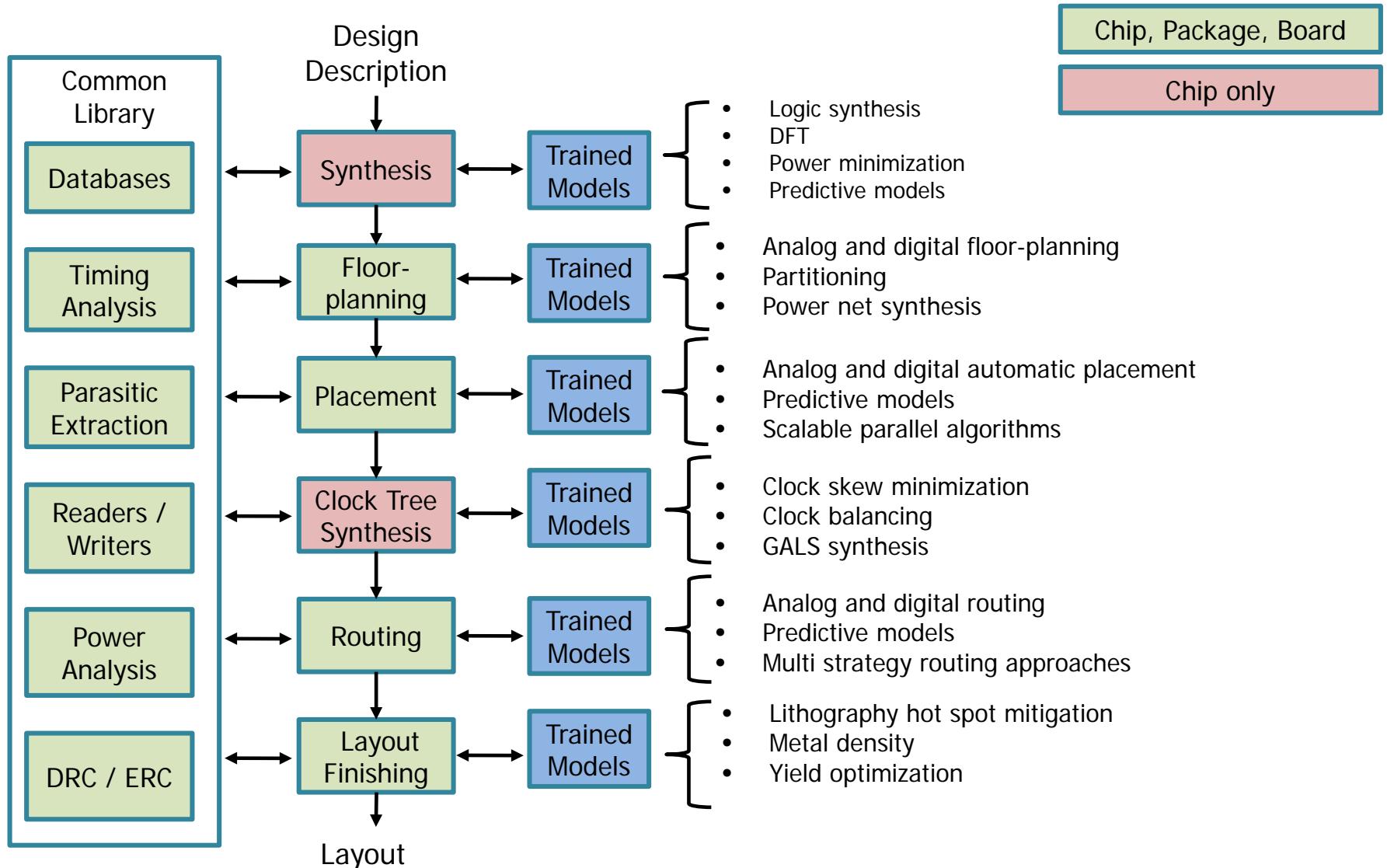
Required:

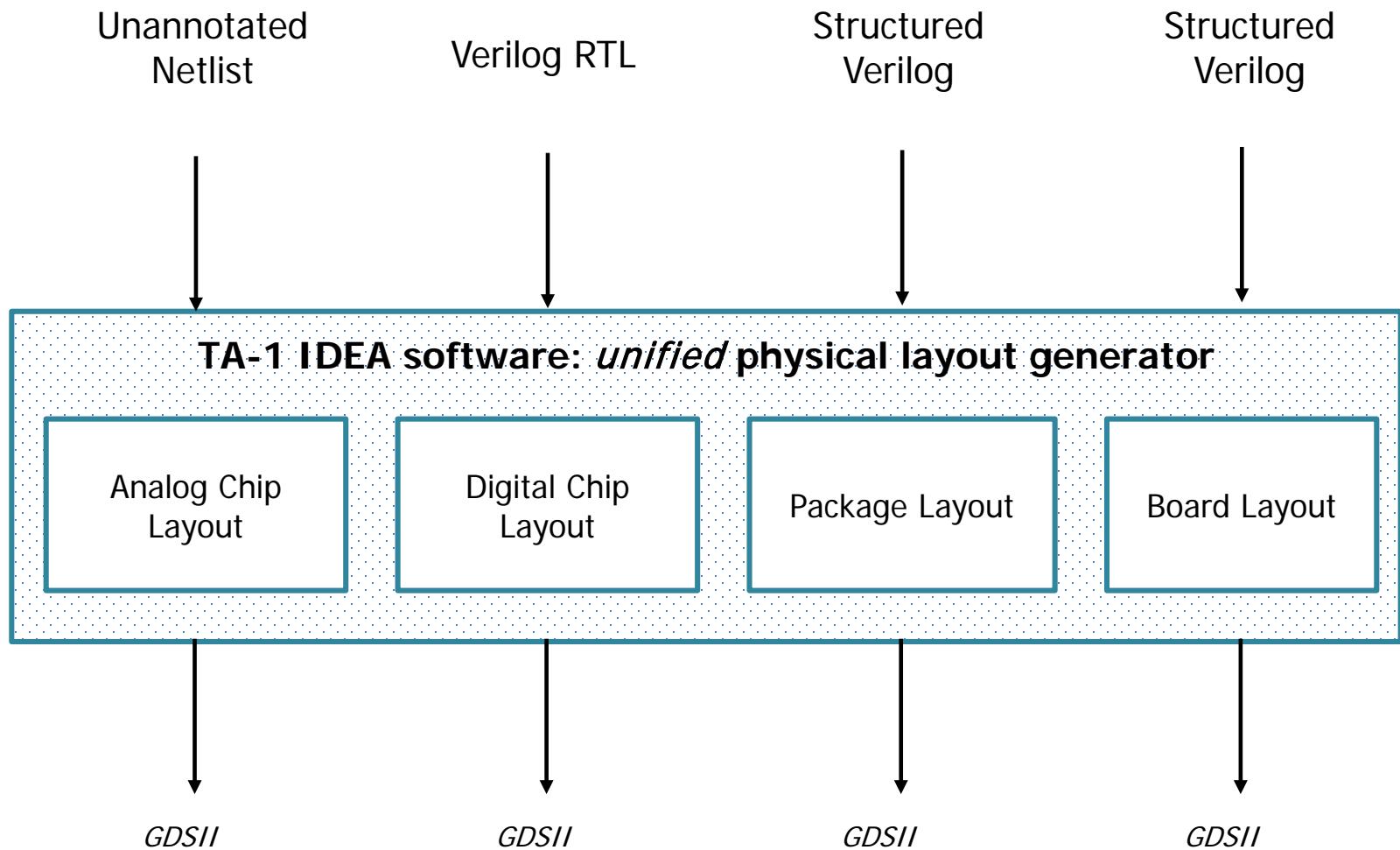
- A collaborative statement submitted with proposal
- Collaboration with other program performers
- Twice a year software integration exercises
- Interoperable software modules
- Open module interfaces

Strongly encouraged:

- Publishing code and results early and often
- Permissive (non-viral, non proprietary) open source licensing

TA1 notional flow







TA1 minimum viable product

- Analog, digital, and mixed signal design
- Asynchronous and synchronous digital design styles
- Clock gating
- Automated pipeline retiming
- Multiple clock domains
- Multiple voltage domains
- Power gating and adaptive voltage scaling
- Scan insertion (DFT)
- Physical design hierarchy
- Large designs (>100M placed instances)
- Flip-chip, micro-bumps, and wire-bond packaging
- 2.5D Systems-in-Package
- Advanced PCB manufacturing technologies, consistent with technologies used for 2017 smartphone manufacturing



TA1 subtasks

Common Infrastructure:

- Databases, processing
- Cloud infrastructure
- Timing Analysis
- Parasitic Extraction
- Readers/Writers
- Power and signal integrity analysis

Layout Generator:

- Logic Synthesis
- Floor-planning
- Placement
- Clock tree synthesis
- Detailed routing
- Layout finish

Design Advisors:

- Layout of 100m² SoC at 14nm using IDEA flow



TA1 metrics

Technical Area	Metrics	Phase 1	Phase 2
IDEA TA-1: Machine Generated Physical Layout	SoC Benchmarks	Government furnished benchmarks 14nm CMOS PDK	Government furnished benchmarks 7nm & 14nm CMOS PDK
	Board Benchmarks	BeagleBone Black	Open Compute Server
	SiP Benchmarks	Government furnished benchmarks	Government furnished benchmarks
	Benchmark $PPA_{IDEA}/PPA_{Traditional}$	0.5	1
	Package Complexity	Up to 2 die, 2.5D	Up to 1024 die, 2.5D
	Automation	100%	
	Turnaround time	24 hours	
	Deliverable	Software, license, software documentation	



IDEA benchmarks

IDEA TA1 will be verified against a set of open, government furnished benchmark suites:

- OpenPiton (<http://parallel.princeton.edu/openpiton/#infosec>)
- RISC_V Rocket Chip (<https://github.com/freechipsproject/rocket-chip>)
- BeagleBone (<https://beagleboard.org/black>)
- Facebook Wedge Board (<https://opencompute.org>)
- BaseJump Wirebond Ball Grid Array (BGA) package (<http://bjump.org/>)
- Additional benchmarks to be developed by a USG/FFRDC

Evaluations of software will be conducted throughout the program by a system evaluator (such as an FFRDC)

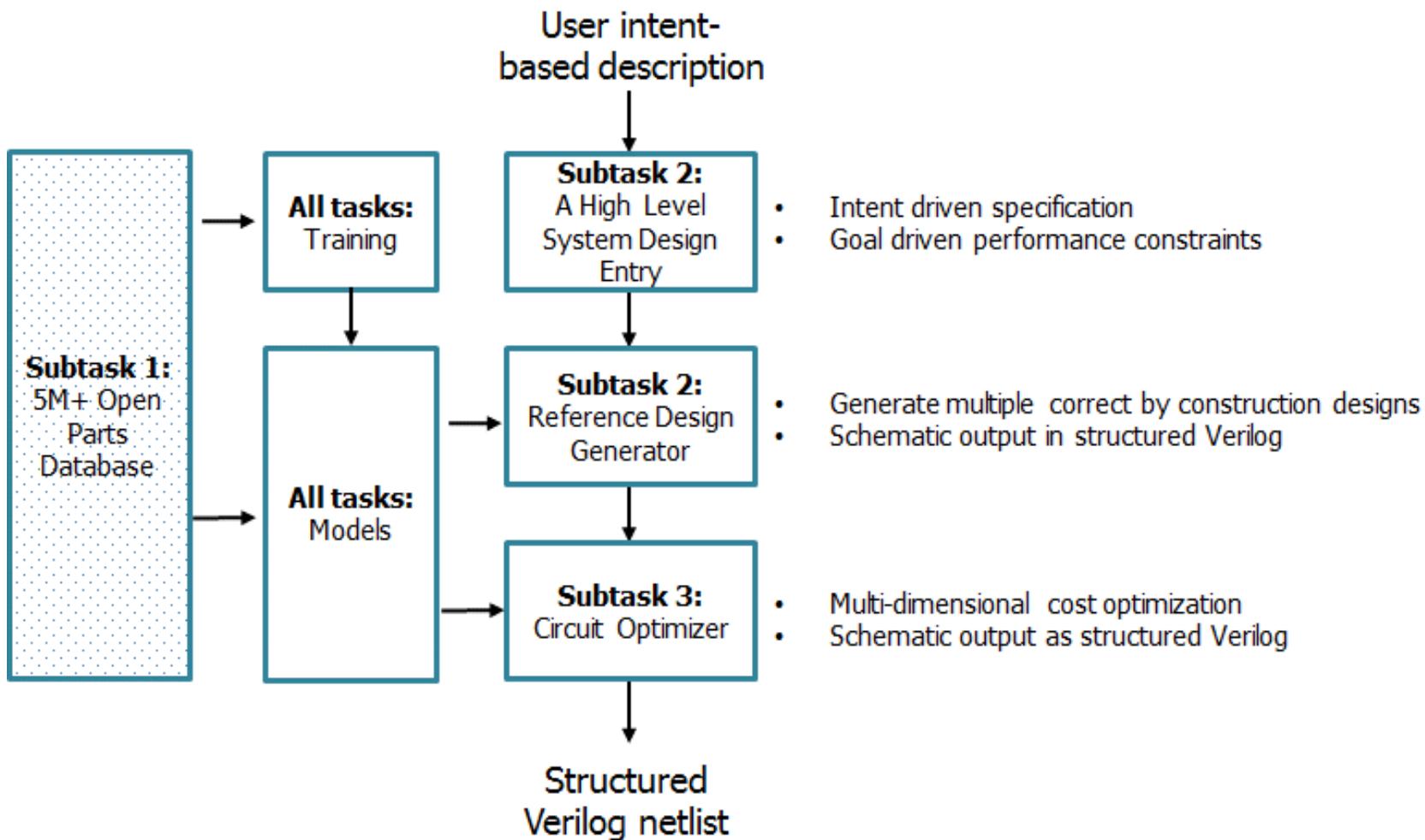


Phase 1: Exploratory Research (Year 1/2)

- Develop no human in the loop layout generator that achieves 50% of peak PPA
- Codify state of the art designer knowledge
- Demonstrate application of machine learning to automated physical design
- Create an annotated high quality dataset of circuits and layouts
- Collaborate on IDEA standards and APIs
- Support for 14nm, 28nm, 65nm, and 180nm CMOS

Phase 2: Optimization and System Demonstration (Year 3/4)

- Develop no human in the loop layout generator that achieves 100% of peak PPA
- Advance state of the art in ML as applied to layout generators
- Extend technology support to 7nm
- Expand datasets and demonstrate PPA improvements through learning
- Increase the number of IDEA platform users





TA2 subtasks

- **Open Parts Database**
 - Automated data mining of existing corpus of datasheets, designs, app notes
 - Capacity to support 5M+ parts
 - Support for SoCs, SiPs, and PCBs
 - Standard models (GDSII, LEF, LIBERTY, IP-XACT)
- **System Generator:**
 - Intent driven high level system generator
 - Structured Verilog netlist output
- **Circuit Optimizers**
 - Structured Verilog netlist input
 - Optimized system netlist based on multiple criteria such as cost, weight, power, size, reliability, and system compliance.



TA2 metrics

Technical Area	Metrics	Phase 1	Phase 2
TA-2: Intent Driven System Synthesis	SoC Benchmark	SoC with 10 IPs	SoC with 100 IPs
	PCB Benchmark	BeagleBone Black	Open Compute Board
	SiP Benchmark	Establish pathway to SiP generation	Demonstrated fully automated layout of SiPs with >100 chiplets and >100,000 nets
	Benchmark $\text{PPA}_{\text{IDEA}}/\text{PPA}_{\text{Traditional}}$	0.5	1
	Automation	100%	
	Turn around time	24 hours	
	Deliverable	Software, license, documentation	



Phase 1: Exploratory Research (Year 1/2)

- Develop architecture and concepts for intent-driven system generators
- Develop initial software for intent driven synthesis
- Create vast library of COTS parts
- Use existing commercial layout tools to create physical layouts of the structured Verilog netlist produced by Phase 1 system generator.

Phase 2: Optimization and System Demonstration (Year 3/4)

- Manufacture and test boards designed in Phase 1
- Integrate TA2 system generator with TA1 layout generator
- Manufacture and deliver boards designed using end to end IDEA flow
- Optimize software to achieve 100% of PPA
- Drive widespread adoption of IDEA platform



TA1/TA2 deliverables

Phase	IDEA TA-1	IDEA TA-2
1	<ul style="list-style-type: none">• Layout generator software and any required licenses• Trained models• Documentation• GDSII database• Reports as defined in BAA	<ul style="list-style-type: none">• System synthesis software and any required licenses• Trained Models• Documentation• Library of open COTS components• Reports as defined in BAA
2	<ul style="list-style-type: none">• Layout generator software and any required licenses• Trained Models• Documentation• SoC, SiP, and PCB• Reports as defined in BAA	<ul style="list-style-type: none">• System synthesis software and any required licenses• Trained Models• Documentation• Library of Open COTS components• Board hardware• Reports as defined in BAA



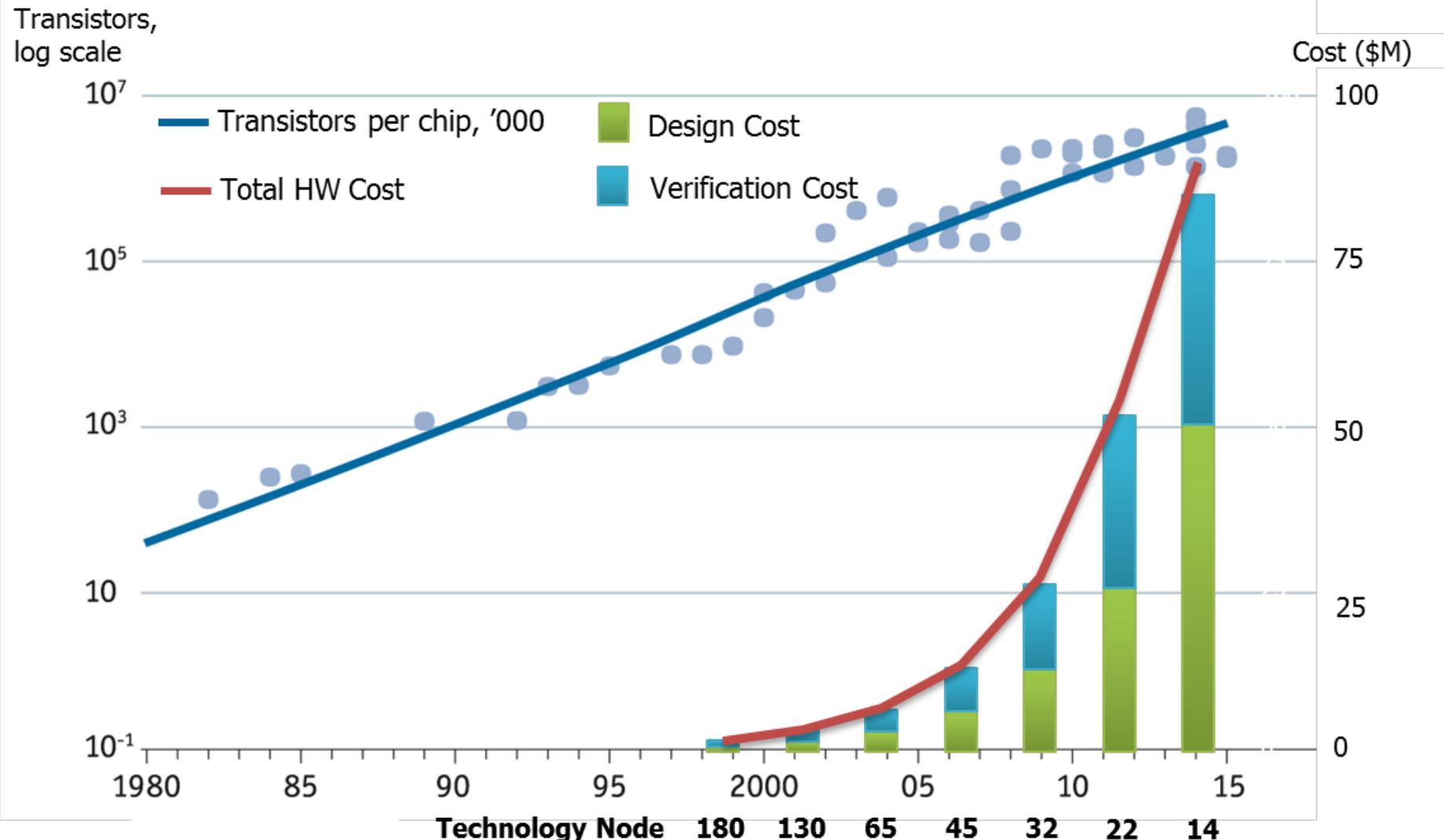
Posh Open Source Hardware (POSH)



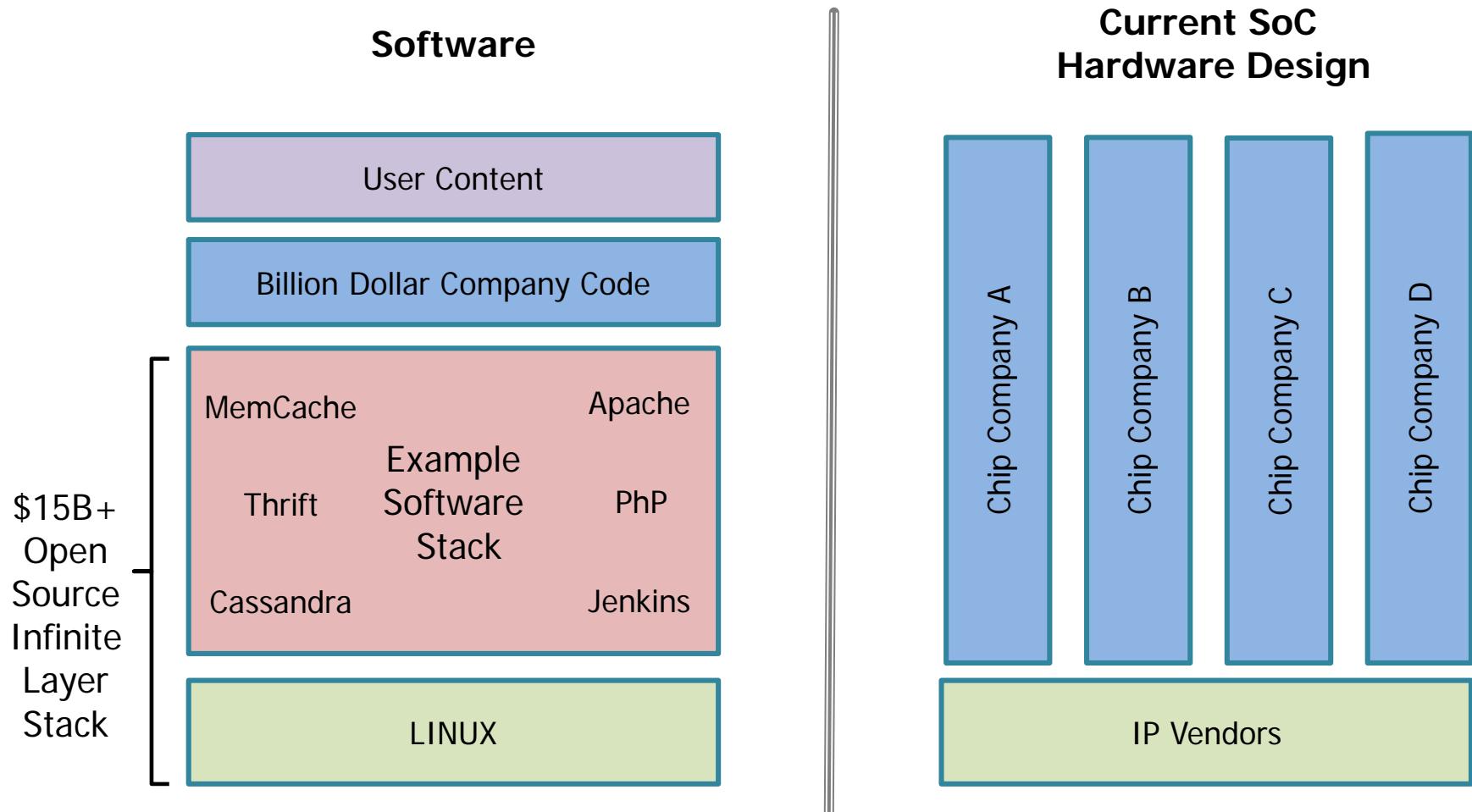
POSH objective

POSH aims to create an open source SoC design and verification ecosystem that will enable the cost effective design of ultra-complex SoCs.

We need a solution to design AND verification costs!



Reinventing the Hardware IP stack



Can a distributed and deeply layered open source development model work for SoC design?



How is Hardware different from Software?

	Software	Hardware
Programmers	Millions	Thousands
Debugging	Hard	Near impossible
Writing Code	Easy	Hard
Reading Code	Hard	Very hard
Cost of bugs	Low	Very high

What technologies are needed to make open source hardware viable?



The state of open source hardware

Open
Cores

RISC-V

GitHub

Open
Compute
Project

FOSSi
Foundation

Still a long way to go...



Hurdles to open source hardware development

- **Work-force**
 - Motivated high quality developers
- **Time**
 - Mostly equates to money (\$\$\$)
- **Development Costs**
 - Ideally zero (Laptop + GCC)
- **Integration Costs**
 - Without emotional rewarding feedback, open source projects die
- **Collaboration framework**
 - Linux patches, mailing lists, IRC, github, etc
 - Standards (C, JAVA, Verilog)



What about OpenCores?

Open Cores

- **1180 projects** (different IP-blocks)
- **283578 registered users**
- **1783 new registered users** during last month (August)
- **~500 000 page views** every month
- **~80 000 visitors** every month
- **~5:30** (min:sec) Average time at website
- **~6 page views** per visitor (average)

Common Issues:

- Documentation
- Quality!
- Abandoned projects
- Lack of collaboration
- License Terms

Registered OpenCores users



283578

[OpenCores statistics](#)

Last updated projects

- [ODESS Multicore Project](#)
- [NoC based MPSoC](#)
- [PCIe Gen3x8 DMA for virtex7](#)
- [UART to Bus](#)
- [AUTO DATA-RATE CHECKER](#)
- [SpaceWireSystemC](#)
- [UART 16550 core](#)
- [MPEG2 Video decoder](#)



Most popular projects

- [USB Host Core](#)
- [I2C controller core](#)
- [NEO430 Processor \(MSP430-compatible\)](#)
- [SPI Master/Slave Interface](#)
- [Ethernet 10GE Low Latency MAC](#)
- [I2C master/slave Core](#)
- [Reed Solomon Decoder \(204,188\)](#)
- [SPI Verilog Master & Slave modules](#)



What about GitHub?

Repositories Developers Trending: this week

[mntmn / amiga2000-gfxcard](#) ★ Unstar
MNT VA2000, an Open Source Amiga Graphics Card (Zorro II/III), written in Verilog
Verilog ★ 817 ⚡ 31 Built by

[VerticalResearchGroup / miaow](#) ★ Unstar
An open source GPU based off of the AMD Southern Islands ISA.
Verilog ★ 364 ⚡ 83 Built by

[cliffordwolf / picorv32](#) ★ Unstar
PicoRV32 - A Size-Optimized RISC-V CPU
Verilog ★ 314 ⚡ 71 Built by

[parallella / oh](#) ★ Unstar
Silicon proven Verilog library for IC and FPGA designers
Verilog ★ 242 ⚡ 86 Built by

[kramble / FPGA-Litecoin-Miner](#) ★ Star
A litecoin script miner implemented with FPGA on-chip memory.
Verilog ★ 162 ⚡ 75 Built by

[analogdevicesinc / hdl](#) ★ Star
HDL libraries and projects
Verilog ★ 151 ⚡ 379 Built by

- ## Common Issues:
- Documentation
 - Quality!
 - Modularity
 - Portability
 - License Terms



POSH program structure

- **TA-1: Hardware Assurance Technology:** Development of hardware assurance technology appropriate for signoff quality validation of deeply hierarchical analog and digital circuits of unknown origin.
- **TA-2: Open Source Hardware Technology:** Development of design methods, standards, and critical IP components needed to kick-start a viable open source SoC eco-system.
- **TA-3: Open Source System-On-Chip Demonstration:** Demonstration of open source hardware viability through the design of a state of the art open source System-On-Chip.



Required:

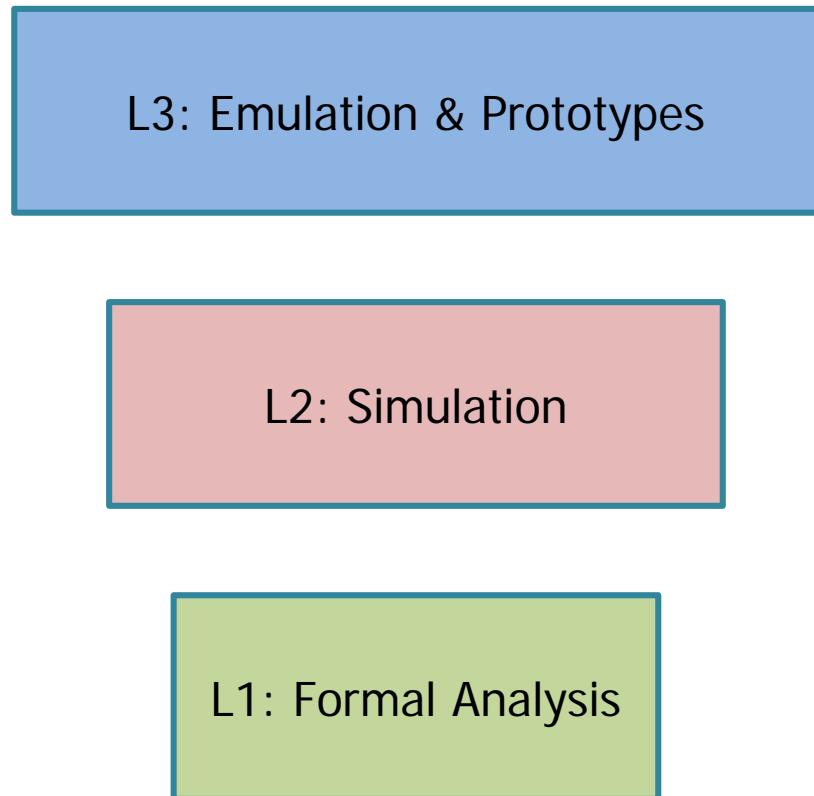
- A collaborative statement submitted with proposal
- Collaboration with other program performers
- Twice a year software integration exercises
- Interoperable software modules
- Open module interfaces

Strongly encouraged:

- Publishing code and results early and often
- Permissive (non-viral, non proprietary) open source licensing

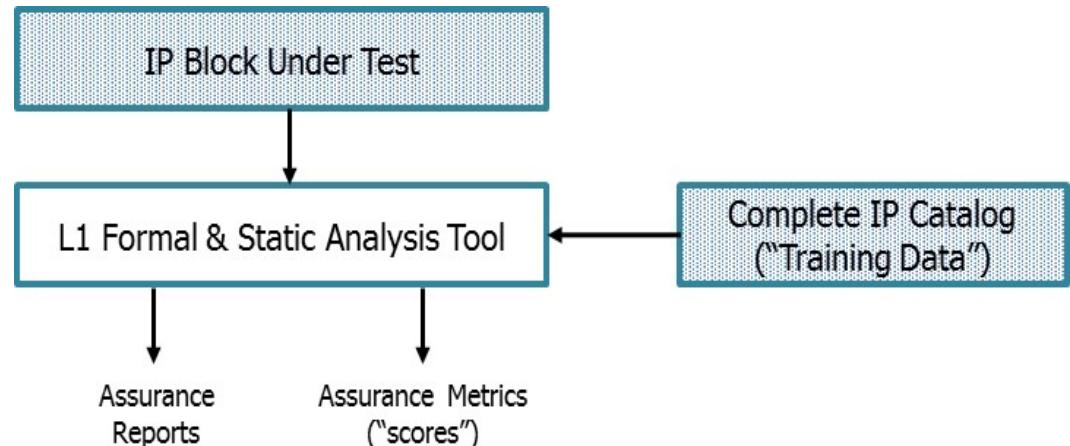
Level	Description
L3	Accessible open API hardware emulation and prototyping platforms
L2	Scalable open API mixed accuracy simulation tools
L1	Formal tools for assessing relative and absolute quality of hardware library modules

Increasing levels of assurance ↑



Inputs:

- Source code
- Configuration/constraints
- Documentation
- Minimal testbench
- Driver software/firmware



Outputs:

- Absolute and relative hardware assurance analysis

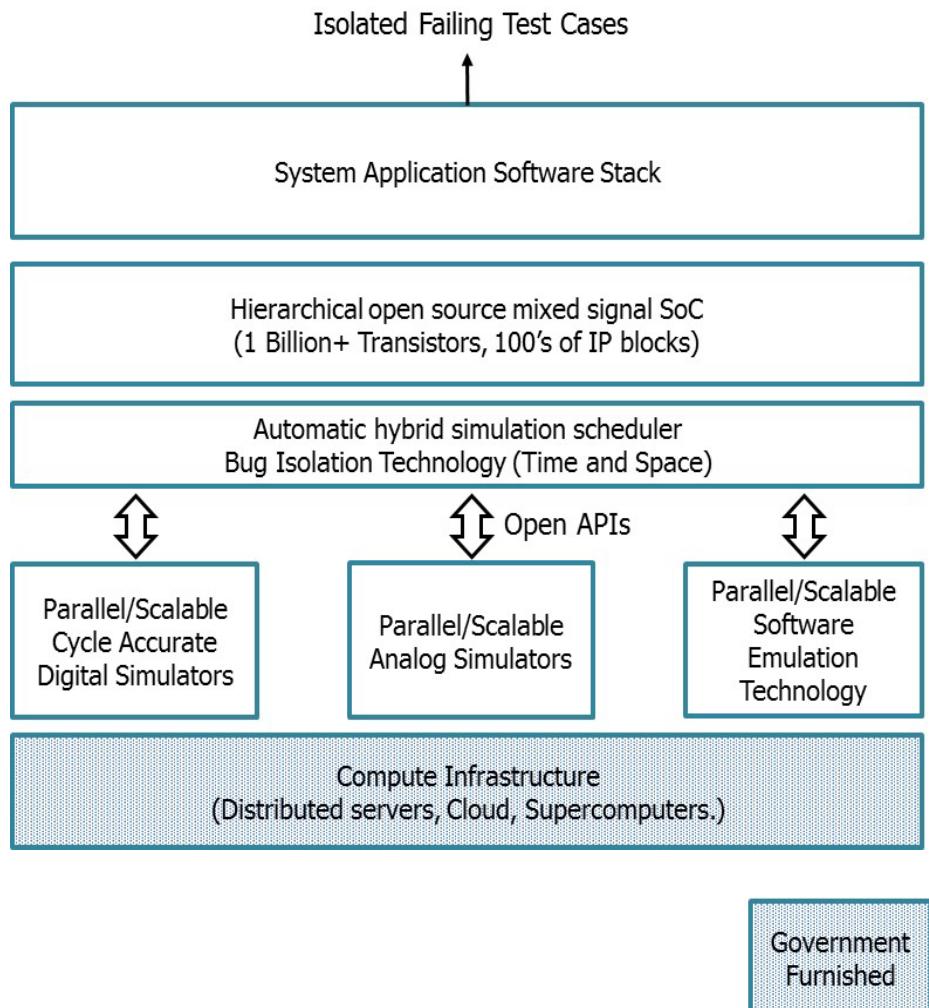
Metrics

- Functionality, security, performance, power, complexity, etc

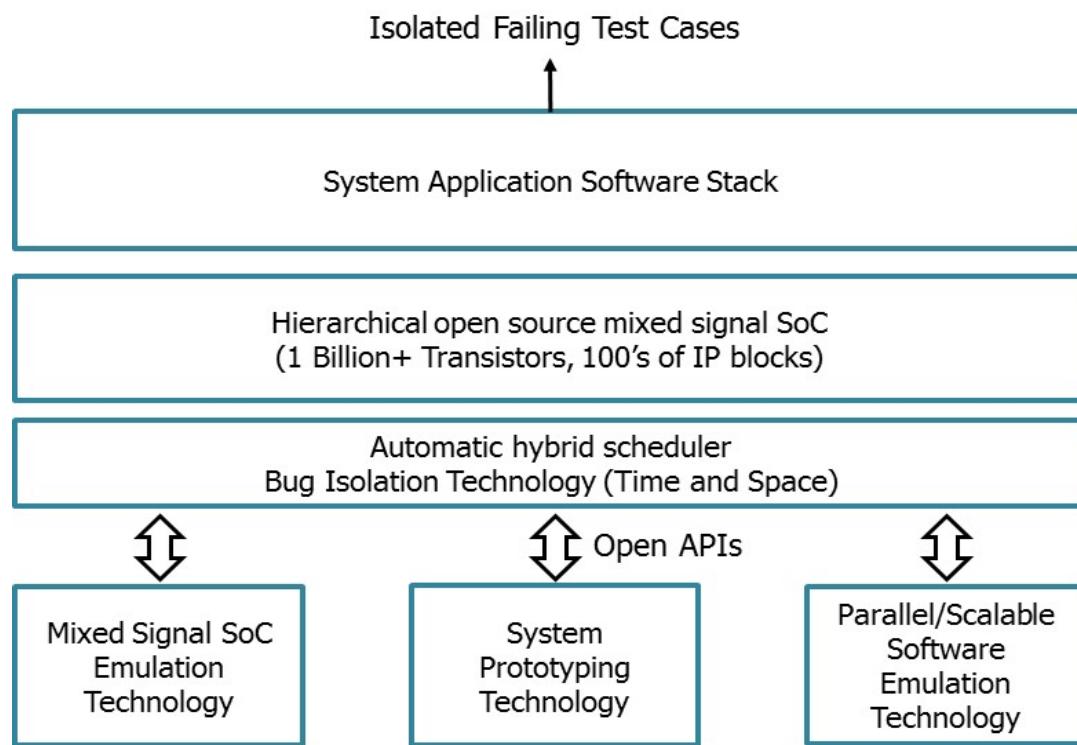
Examples:

- Symbolic analysis
- Static analysis
- Machine learning

- Open “Plug and Play” APIs
- Scalable to 1000’s of servers
- 1MHz speed for loosely coupled systems
- Transparent co-simulation
- Automated fidelity/speed tuning
- Automated test case extraction
- Debug assist technology appropriate for open source SoC design



- Open “plug and play” APIs
- Mixed signal emulation
- Accessible to open source community
- Transparent integration with QEMU and cycle accurate simulators





Phase 1: Exploratory Research (Year 1/2)

- Explore novel approaches to L1, L2, L3 sub-tasks
- Benchmarking against existing corpus of open source designs
- Release cost effective L1,L2,L3 hardware assurance software appropriate for open source development

Phase 2: Optimization and Deployment (Year 3/4)

- Advance Phase 1 software to enable support of 1 billion transistor mixed signal SoCs
- Simulation speeds of 1MHz
- Mixed signal emulation and prototyping of full systems
- Deliver software and hardware developed in TA1



TA2: open source technology

Digital Circuit IP Blocks
FPGA Fabric
Multi-core 64-bit RISC-V processor sub-system
GPU (OpenGL ES 3.0)
PCI Express Controller
Ethernet Controller
Memory Controllers
USB 3.0 Controller
MIPI Camera Serial Interface controller
CPU Subsystem
H264 encoder/decoder
AES256 encrypt/decrypt
SHA-2/SHA-3 accelerator
Secure Digital Controller
High Definition Multimedia Interface
Serial ATA Controller
JESD204B Controller
NAND Flash Controller
CAN Controller

Mixed Signal Circuit IP Blocks	Description
Standard I/O interfaces PHYs	DDR, PCIe, SATA, USB, XAUI, CPRI
PLL	Range: 10MHz – 10GHz
DLL	Range: 10Mhz – 10GHz
Analog to Digital Converters	Range: 1 – 10,000 MSPS
Digital to Analog Converters	Range: 1 – 10,000 MSPS
Voltage Regulators	Input: 1.8V – 12V, Output 0.25V – 1.8V
Monitor circuits	Temperature, voltage, process

How can we cost effectively develop and maintain a high quality catalog of portable open source digital and analog components?



Digital IP Blocks:

- Source code
- User documentation
- Self-testing testbench
- Driver software/firmware

Analog IP Blocks:

- ASCII based source (netlist/schematics)
- Verilog-A model
- User documentation
- Self-testing testbench
- PDK independent support from process nodes from 14nm to 180nm
- Driver software/firmware



Phase 1: Exploratory Research (Year 1/2)

- Develop PDK independent analog and digital open source IP modules
- Demonstrate cost effective open source design of digital and analog circuits
- Demonstrate decoupling of design sources from PDK data
- Demonstrate portability from 14nm to 180nm
- Deliver circuit source code, test-bench, models, and documentation

Phase 2: Optimization and System Demonstration (Year 3/4)

- Provide maintenance support and improvements for open source IP blocks created in Phase 1



TA3: open source system-on-chip demonstration

- Design a state of the art open source mixed signal 100mm² SoC
- Design an interesting AND important capability!
- Perform early testing of TA1 and TA2 technology
- Integrate majority of TA2 IP blocks in design
- Design any specialized components required for SoC
- Demonstrate a 10X+ SWAP-C improvement over existing COTS solutions
- DARPA will provide fabrication support through MPWs



Phase 1: SoC Design and Verification (Year 1/2)

- Work with POSH TA2 performers to define standards for open source IP
- Complete architecture exploration and design of a 100mm² open source 14nm SoC
- Validate SoC using technology from POSH TA1
- Deliver source code and documentation for SoC
- Complete physical design of SoC and deliver GDSII database ready for manufacturing

Phase 2: Optimization and System Demonstration (Year 3/4)

- Demonstrate a 10X SWAP-C improvement over existing COTS solutions
- Tapeout of Phase 1 SoC
- Post-silicon validation of SoC
- Modify SoC based on lessons learned during post-silicon validation
- Complete physical design and tapeout of 2nd generation SoC



POSH deliverables

Phase	POSH TA-1	POSH TA-2	POSH TA-3
1	<ul style="list-style-type: none">• Software and any required licenses• Training Models• Documentation• Reports as defined below	<ul style="list-style-type: none">• IP Blocks• Supporting documentation• Reports as defined below	<ul style="list-style-type: none">• Specialized IP blocks• GDSII database ready for manufacturing• Reports as defined below
2	<ul style="list-style-type: none">• Software and any required licenses• Training Models• Documentation• Reports as defined below	<ul style="list-style-type: none">• IP Blocks• Supporting documentation• Reports as defined below	<ul style="list-style-type: none">• SoC, package and board (hardware)• Reports as defined below

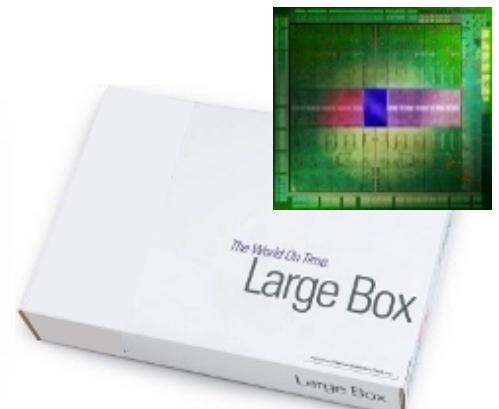


Conclusion



Are you awake?

```
$ git clone https://github.com/darpa/idea  
$ git clone https://github.com/darpa/posh  
$ cd posh  
$ make soc42
```





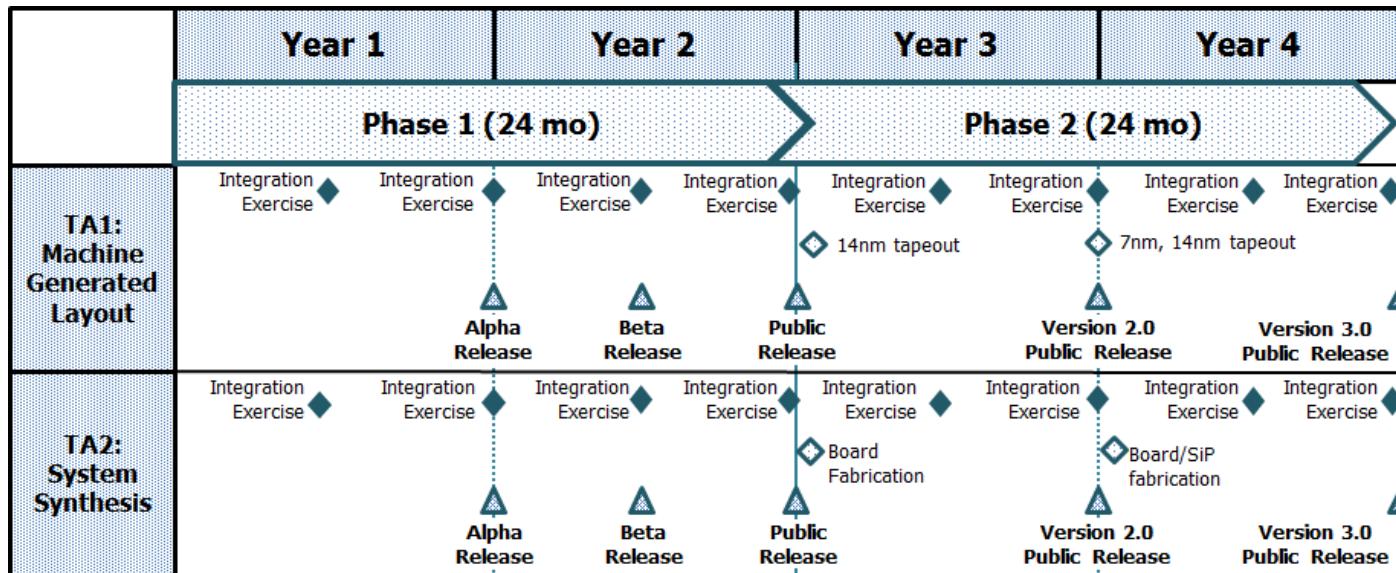
Proposal Evaluation Criteria and Proposal Guidance



Program and technical areas

- This BAA is not like other DARPA BAAs. The ERI Page 3 Design BAA includes two separate programs: POSH and IDEA
- POSH and IDEA will operate independent of each other and should be considered separate programs
- Proposers MUST submit separate proposals if proposing to both IDEA and POSH
- All work in the IDEA and POSH programs will be unclassified
- For the purposes of this BAA, DARPA will consider proposals from the same organization with different CAGE codes to be separate organizations
- While proposers may submit proposals for multiple technical areas within one proposal, the decision as to which technical area to consider for award is at the discretion of the Government

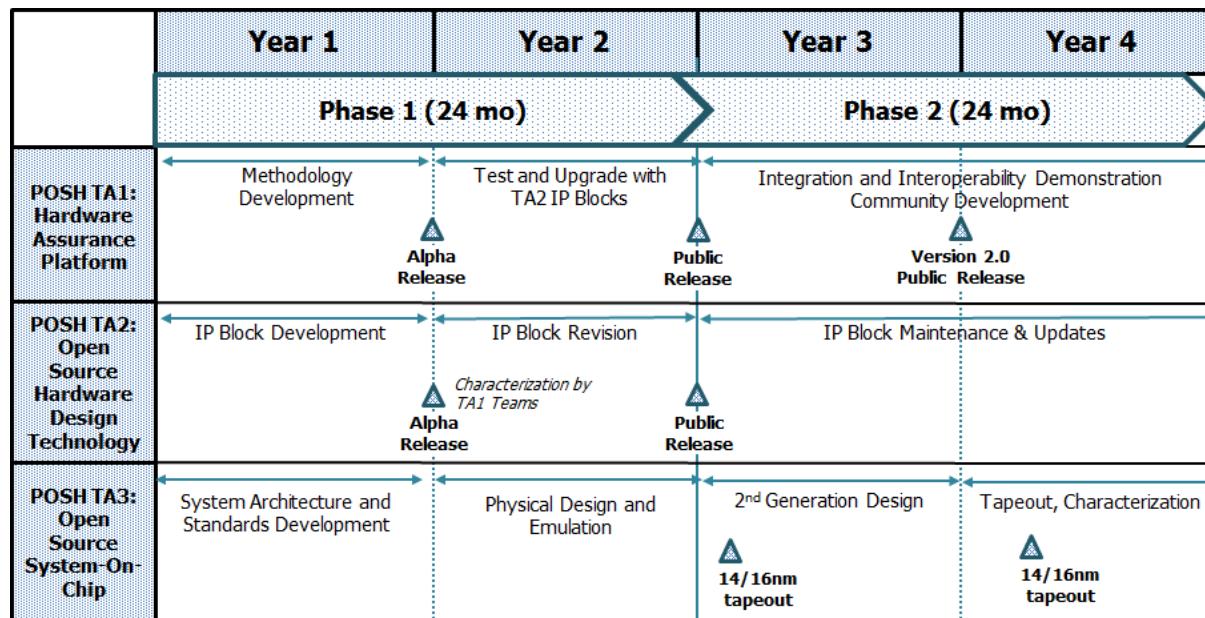
- The goal of IDEA is to create a national capability
 - Teams will be required to deliver high quality, working software that meets the program goals of automated physical design for SoCs, packages and boards
 - Proposers should design their proposed technical effort to meet the IDEA schedule
 - Deliverables will include software, required licenses, trained models, and accompanying documentation
 - Other deliverables include quarterly technical reports and participation in biannual integration exercises



Abridged text – See BAA for full text of schedule and deliverables

POSH program schedule & deliverables

- The goal of POSH is to create a national capability and enable an open source ecosystem
- Proposers should design their proposed technical effort to meet the POSH schedule
- Teams will be required to deliver high quality, working software (TA1), IP blocks (TA2, TA3), and/or hardware (TA3)
- Deliverables will include software, required licenses, trained models, and accompanying documentation (TA1) and SoC, package and board (TA3)
- Other deliverables include quarterly technical reports and participation in biannual integration exercises



Abridged text – See BAA for full text of schedule and deliverables



Biannual integration exercises

- One week long software integration exercises will occur twice per year throughout the duration of both the POSH and IDEA program
- All performers will be required to attend and collaborate with other performers to develop a high quality platform
- These exercises are intended to facilitate integration onto the POSH or IDEA platform and ensure interoperability between software modules
- Interaction and collaboration early and outside of the integration exercises will be highly encouraged
- Performance at these exercises will influence program evaluations and phase decisions



Publications

- The DoD does not restrict publication of fundamental research
- Proposers should indicate in their proposal whether they believe the scope of the research included in their proposal is fundamental or not
 - The Government will make the final decision
- Contracts for non-fundamental research will include a clause requiring DARPA review and potential edits prior to publication
- Publication is highly encouraged since this stimulates technology adoption research
- Proposals may include a budget for development and presentation of academic or trade publications



Funding of phase 2

- Both POSH and IDEA include a base Phase 1 and option Phase 2
- The proposed planning and costing by Phase (and by Task) provides DARPA with convenient times to evaluate funding options and technical progress
- Progression into Phase 2 is not guaranteed; factors that may affect Phase 2 funding decisions
 - Availability of funding
 - Cost of proposals selected for funding
 - Demonstrated performance relative to program goals
 - Compatibility with other TAs and performers
 - Interaction with government evaluation teams
 - Compatibility with potential DoD applications



Proposal evaluation criteria for IDEA and POSH

*Proposals will be evaluated based on the following criteria. Evaluation criteria for these BAAs are clearly defined in the documents. **Do not assume that they are similar to other DARPA BAAs:***

1. Overall scientific and technical merit
 2. Potential Contribution and Relevance to the DARPA Mission of Supporting National Security
 3. Impact on the Overall Electronics Landscape
 4. Cost Realism
-
- The following pages contain selected tips on how to satisfy the evaluation criteria
 - **Read the BAA** for complete guidance on technical and cost proposals
 - Ensure technical proposal does not exceed 20 page limitation; submission to multiple technical areas does not increase page count



1. Overall scientific and technical merit

- The proposed technical approach is innovative, feasible, achievable, and complete. The proposed solution is clearly in line with the program goals.
- A specific technical solution path is proposed along with arguments why the proposed approach is expected to be successful and will be an improvement on the State of the Art. Analysis and trades are presented explaining why the proposed approach was selected and why alternatives were not proposed.
- Task descriptions and technical elements are complete and in a logical sequence leading to an endpoint supporting POSH or IDEA goals. Proposed task elements have measureable milestones that will aid DARPA in tracking progress. Deliverables and cross-performer interfaces are clearly defined and support the Program structure.
- The proposal identifies major technical risks and includes planned risk mitigation efforts.



Proposal tips 1.0 – IDEA and POSH

- Propose a specific solution path rather than a menu of potential approaches
- Explain why the proposed approach was selected over alternatives
- Explain why the proposed approach is feasible
- Provide quantitative arguments why the proposed approach is expected to meet Program performance goals
- Explain how collaboration will be achieved across teams
- Explain your ability to interact with and respond to feedback from the evaluation team



Proposal tips 1.1 - IDEA

All TAs:

- Discuss how complete automation for ALL aspects of design (chip, package AND board) will be accomplished
- Proposers are encouraged to propose to one or as many subtasks are appropriate for their solution
- Explain how you will collaborate with other performers
- Machine learning is of high interest; teams will benefit from proven experience with machine learning and delivery of high quality software

TA1: Machine Generated Physical Layout

- If proposing a solution for backend physical design software, describe interfaces and approach to achieving interoperability
- If proposing a solution for the SoC Design Advisor subtask, discuss the proposed SoC functionality and how it improves on the SoA

TA2: Intent Driven System Synthesis

- Explain how the proposed approach will automate front end physical design for packages and boards and will be applicable to a diverse set of circuits
- If developing the COTs library, describe the number and types of parts proposed



Proposal tips 1.1 - POSH

All TAs

- Discuss how you will demonstrate the enablement of an open source community
- Proposers are not required to submit to all TAs

TA1: Hardware Assurance Technology

- Describe how you will create platforms appropriate for open source hardware development
- Explain how you will work with other TA2 performers to validate open source IP

TA2: Open Source Hardware Technology

- Explain how the designed IP approach is suitable for open source hardware design
- Discuss how you will incorporate feedback from the TA1 validation tool
- Describe, and separately cost, each proposed IP block. Proposers are encouraged to submit designs for multiple IP blocks

TA3: Open Source System-on-Chip Demonstration

- Describe how you will use and tailor IP blocks created by TA2 performers to create a high performance SoC



2. Potential contribution and relevance to the DARPA mission of supporting national security

The potential contributions of the proposed effort are relevant to the national technology base. Specifically, DARPA's mission is to make pivotal early technology investments that create or prevent strategic surprise for U.S. National Security.

Proposal Tip: Consider the perspective of the proposal reviewer that must describe how your proposal contributes to the DARPA mission



3. Impact on the overall electronics landscape

- The proposed approach presents a technology to address rising costs and growing complexities of leading edge circuit design
- The proposed technology has the maturity to impact semiconductor design between 2025-2030
- The potential contributions will provide a foundational contribution to US National Security
- The underlying capability will provide sustainable performance scaling



4. Cost realism

- Funding the proposed effort would not consume a disproportionate fraction of the Program budget.
 - DARPA recognizes that undue emphasis on cost may motivate proposers to offer solutions that are unlikely to fulfill POSH or IDEA goals, or to staff the effort with junior personnel. DARPA discourages such cost strategies.
- The proposed staffing and schedule is consistent with the proposed tasking and technical milestones.
- The proposed costs are realistic for the technical and management approach and accurately reflect the technical goals and objectives of the solicitation. The proposed costs are consistent with the proposer's Statement of Work and reflect a sufficient understanding of the costs and level of effort needed to successfully accomplish the proposed technical approach. The costs for the prime proposer and proposed subawardees are substantiated by the details provided in the proposal.
- The proposal identifies major cost and schedule risks and includes planned risk mitigation efforts.

Ensure editable spreadsheets are delivered as part of the cost volume

Abridged text – See BAA for full text of evaluation criteria 4



Proposal tips – 4

All TAs

- Phases 1 and 2 must be separately planned and priced
- Include a detailed breakdown of technical tasking, with cost and schedule for each sub-task
- All subtasks must be separately planned and priced
- Thoroughly substantiate the cost of any proposed computational hardware purchases
- ALL proposers should include costs to attend biannual, one week long, software integration exercises
- CMOS fabrication runs will be arranged by the government and cost should not be included in the cost proposal



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