Novel RRAM-enabled 1T1R synapse capable of low-power STDP via burst-mode communication and real-time unsupervised machine learning

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Introduction: Resistive switching memory (RRAM) is generating widespread interest as new technology for artificial synapses in bio-inspired neuromorphic systems [1,2]. Recently, two-transistor/one-resistor (2T1R) synapses capable of spike-timing dependent plasticity (STDP) at low power by decoupling integration and fire current paths have been presented [2,3]. *Here we present a new synapse based on one-transistor/one-resistor (1T1R) structure performing spike-timing dependent plasticity (STDP) with lower area than 2T1R. We show STDP functionality and robust learning by both deterministic and stochastic synapses. We demonstrate 10^5 reduction of power consumption thanks to burst operation and 86% efficiency of MNIST handwritten-digit classification.*

RRAM and synaptic characteristics. Our RRAM device consists of a Si-doped HfO_2 layer with TiN bottom electrode (BE) and Ti top electrode (TE) [4]. 1T1R structures (Fig. 1a) were used to characterize RRAM devices and synapses by applying pulses to the TE and gate nodes and monitoring TE voltage and RRAM current by an oscilloscope (Fig. 1b [4]). Fig. 1c shows the bistable I-V curve in response to bipolar triangular pulses for set ($V > 0$) and reset ($V < 0$). The pulse-width t_P was 1 ms, while the compliance current I_C was adjusted to 50 μA by tuning the gate voltage V_G. Set transition takes place at $V_{set} > 0$, while the negative sweep for reset was stopped at $V_{stop} < 0$ (Fig. 1c [4]).

The same 1T1R structure was adopted as the plastic synapse for neuromorphic computing. Fig. 2a shows the fundamental block in our neuromorphic network, consisting of a pre-synaptic neuron (PRE), a 1T1R synapse and a post-synaptic neuron (POST). The 1T1R synapse is a simplified version of the 2T1R synapse [2,3] and is capable of both spike transmission and synaptic plasticity via STDP. The PRE spike is applied to the gate of the 1T1R, while the top electrode (TE) is controlled by the post-synaptic neuron (POST). The 1T1R current excited by the PRE spike flows into the POST where it is integrated, eventually inducing fire as the internal POST voltage exceeds a threshold [5]. The PRE spike consists of a 10 ms gate voltage V_G pulse followed by 10 ms-wait period (Fig. 2b), while TE voltage V_{TE} is continuously held constant by POST. At the fire event, POST delivers a pair of positive-negative spikes. For positive delay ($0 < \Delta t < 10$ ms) between PRE and POST spikes (Fig. 2b), the positive POST spike V_{TE+} induces set process in the RRAM, corresponding to synaptic potentiation. For negative delay (-10 ms $< \Delta t < 0$), instead, the negative POST spike V_{TE-} induces a reset process and synaptic depression. This allows for STDP behavior as shown by the measured relative conductance change R_0/R for various initial RRAM resistance R_0 as a function of Δt in Fig. 3a. Potentiation and depression occur at $\Delta t > 0$ and $\Delta t < 0$, respectively. The measured STDP is nicely reproduced in Fig. 3b by our analytical RRAM model [6].

Neuromorphic computing. STDP in the 1T1R synapse enables visual pattern learning as illustrated in Fig. 4: input spikes are delivered by the PRE layer of N retina neurons (N = 28x28) to a single POST via N synapses (a). Either a pattern (b) or random noise (c) is submitted at each epoch with equal probability of 50% (period = 10 ms) (d), causing integration/fire in the POST (e) and consequent synaptic change according to Fig. 3. Fig. 5 shows the calculated synapse conductance (or weight) during learning at increasing time, assuming random initial R_0. Pattern synapse weights increase while background synapse weights decrease as a result of potentiation and depression, respectively. Learning takes approximately 300 ms (30 epochs) for a 28x28 MNIST character in Fig. 5.

Stochastic learning. Learning efficiency was evaluated as a function of voltage V_{TE+} and V_{TE-} of the POST spikes in Fig. 6. As V_{TE+} is increased above V_{set}, the probability for set transition increases, thus resulting in stochastic potentiation [7]. Similarly, increasing $|V_{TE-}|$ causes partial reset with increasingly strong depression of background synapses. Fig. 6 shows the learning probability P_{learn} (a) and the error probability P_{err} (b) as a function of V_{TE+} and $|V_{TE-}|$ in a colour map, where P_{learn} is the number of fire events following the presentation of a pattern, divided by the total number of pattern presentations, while P_{err} is the number of fire events following the presentation of noise, divided by the total number of noise presentations. The best performance is obtained at large V_{TE+} and $|V_{TE-}|$, as also summarized by Fig. 6c showing P_{learn} and P_{err} as a function of V_{TE+} for $V_{TE-} = -1.6$ V and for various number of RRAMs per synapse. These results indicate that *robust learning in bistable synapses can be achieved without necessarily requiring stochastic set/reset and multiple cells per synapse* [1]. Fig. 6d shows P_{learn} as a function of noise pixel density, indicating an optimum P_{learn} at 9% density of noise spikes.

Power management. On-line learning may find application as on-chip intelligence in distributed smart sensors, for which low-power operation is mandatory. Fig. 7 shows the energy per epoch and power consumption P due to integration and fire in Fig. 2b. Fire contributes the largest power, due to a relatively long spike (t_P = 1 ms, Fig. 2b) and high current (I_C = 50 μA, Fig. 1c). Reducing the spike pulse-width to 100 ns allows a decrease of P by almost 10^4. Fire power can be further decreased by adopting even shorter t_P and smaller I_C.

Integration power can be reduced by the burst-mode operation in Fig. 8a: instead of a DC voltage, V_{TE} pulses (100 ns pulse-width, 10 ms period) are applied to induce integration, thus resulting in a 10^5 reduction of integration power. Burst mode also allows to reduce the integration capacitance, hence area, by the same magnitude. Fig. 8b summarizes P reduction by decreasing t_P and adopting burst mode.

Pattern learning and classification. We simulated learning and classification of handwritten digits from the MNIST database. Fig. 9 illustrates the fully-connected perceptron network for simultaneous learning of 10 digits (a) and the corresponding synaptic weights after learning (b). Fig. 10a shows the calculated P_{learn} and the efficiency P_{class} of correctly classifying 10^4 unlearnt digits, as a function of the number of digits submitted for learning. Results indicate a constant $P_{learn} \approx 82\%$, while P_{class} increases to about 86% after submitting $2.5x10^4$ digits for learning. Fig. 10b shows a breakdown of P_{class} per each digit, showing excellent digit recognition. These results support robust unsupervised learning and classification by RRAM synapses.

Conclusions. We present a new electronic synapse for neuromorphic computing consisting of a 1T1R structure based on HfO_2 RRAM technology, and capable of STDP and pattern learning. Power consumption is reduced by adopting short POST spike and burst-mode integration. MNIST classification shows promising learning and classification efficiency. These results support RRAM as an enabling technology for low-power neuromorphic hardware.

References

[1] S. Yu, *et al.*, Adv. Mater. 25, 1774 (2013).
[2] Z.-Q. Wang, *et al.*, Front. Neurosci. 8:438 (2015).
[3] S. Kim, *et al.*, IEDM Tech. Dig. 443 (2015).
[4] S. Balatti, *et al.*, IEEE Trans. Electron Devices 62, 1831 (2015).
[5] E. Chicca, *et al.*, Proc. IEEE 102, 1367 (2014).
[6] S. Ambrogio, *et al.*, IEEE Trans. Electron Devices 61, 2378 (2014).
[7] S. Balatti, *et al.*, IEEE JETCAS 5, 214 (2015).

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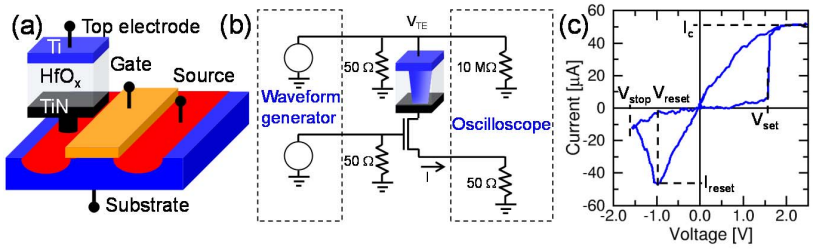

Fig. 1 Schematic illustration of the 1T1R structure used in this work (a), experimental setup (b) and measured I-V curve showing the definition of parameters V_{set}, V_{reset}, V_{stop}, I_C and I_{reset} (c). The RRAM stack includes a Si-doped HfO_x switching layer, a Ti cap layer and TiN BE.

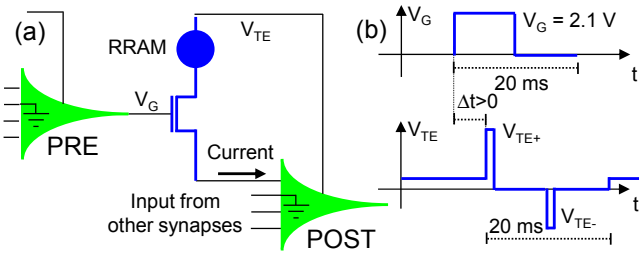

Fig. 2 Scheme of the 1T1R synapse with PRE and POST (a) and spike signals for V_G and V_{TE} at the basis of STDP (b). A V_G spike from PRE induces a current integrated by POST, eventually leading to fire. At fire, V_{TE} induces potentiation ($\Delta t > 0$) or depression ($\Delta t < 0$), resulting in STDP.

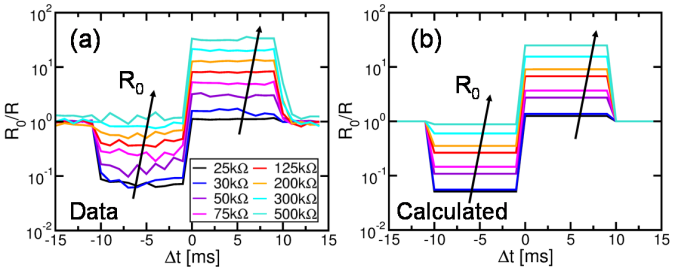

Fig. 3 STDP characteristics, namely change of conductance R_0/R as a function of Δt defined in Fig. 2b, obtained from data (a) and calculations (b). Data were collected from 1T1R RRAM devices as in Fig. 1, while calculations were done with an analytical model implemented in Simulink. The change of conductance was measured/calculated for increasing initial resistance R_0.

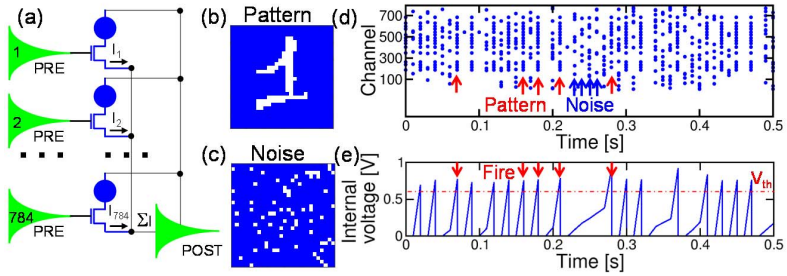

Fig. 4 Schematic layout of the 2-layer, fully-connected neuromorphic network to demonstrate pattern learning (a), input visual pattern (b), typical noise (c), channel-by-channel spiking activity from PRE (d) and corresponding internal voltage in POST showing fire events upon reaching threshold voltage V_{th} (e).

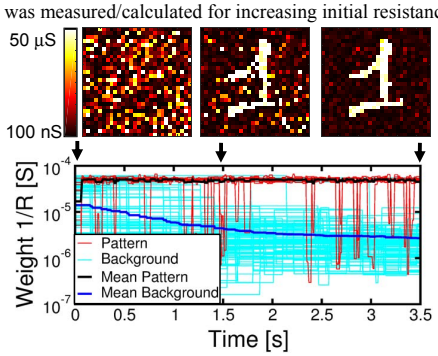

Fig. 5 Evolution of synaptic weights for pattern (red) and background (cyan) with the corresponding synapse weight maps at 0, 1.5 and 3.5 s.

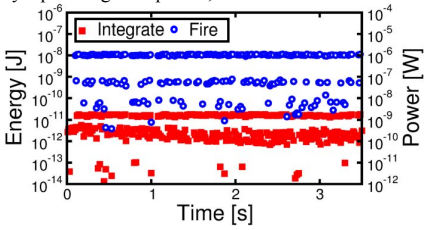

Fig. 7 Calculated evolution of energy/power consumption due to integration (red) and fire (blue) during the learning process in Fig. 5.

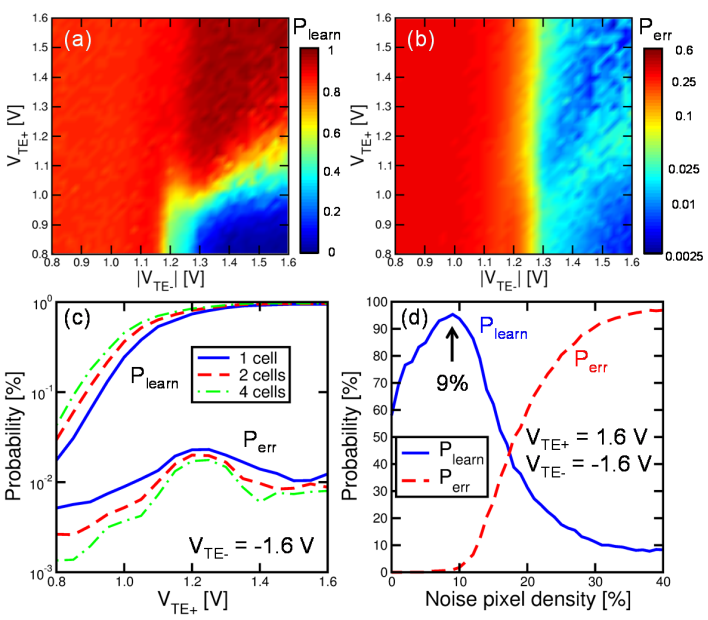

Fig. 6 Color maps showing P_{learn} (a) and P_{err} (b) as a function of V_{TE+} and V_{TE-} in Fig. 2b. P_{learn} and P_{err} are also shown as a function of V_{TE+} for V_{TE-} = -1.6 V (c), for 1, 2 and 4 RRAM cells per synapse. Maximum P_{learn} is achieved for noise input density of about 9%.

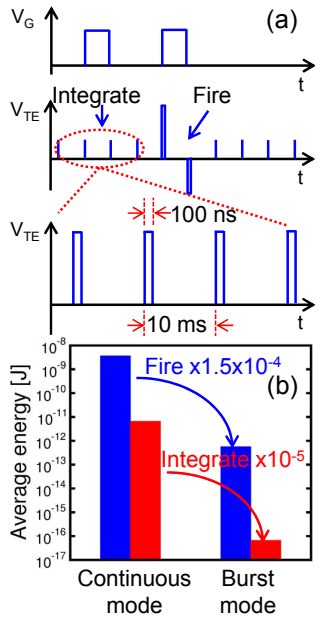

Fig. 8 Energy consumption for continuous V_{TE} and t_P = 1 ms, compared to burst-mode V_{TE} and t_P = 100 ns, indicating strong reduction of energy dissipation.

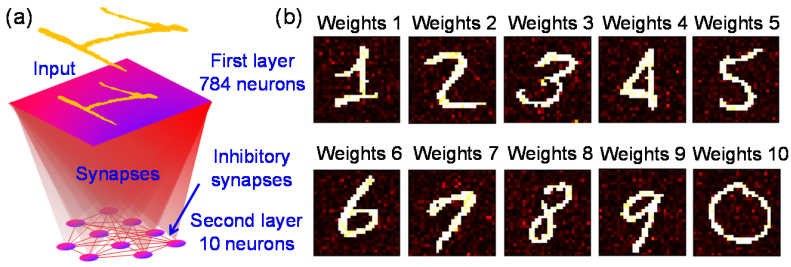

Fig. 9 Schematic illustration of the 2-layer network adopted for the multi-pattern learning (a) and synapse weights after learning (b). The second layer consists of 10 neurons interconnected by inhibitory synapses, allowing for differentiating learning of multiple digits.

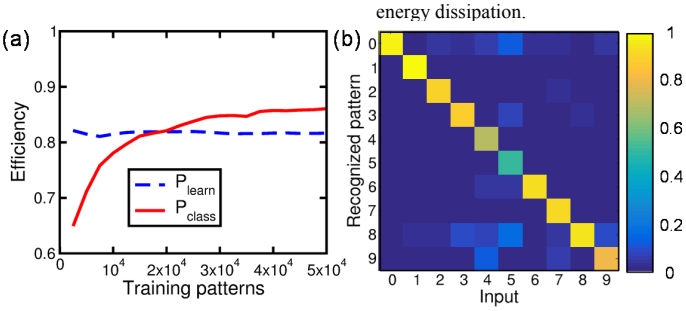

Fig. 10 Efficiency of learning (P_{learn}) and classification (P_{class}) as a function of the number of training digits (a) and color plot of efficiency in classifying digits into 10 possible patterns (b). After learning $5x10^4$ digits, 10^4 new digits were submitted to the PRE, while the correspondingly firing POSTs were collected for classification. Correct classification along the diagonal was obtained in most cases.