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A Vertical Organic Transistor Architecture for Fast Nonvolatile Memory

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Following the conventional hard-disk and silicon memory technologies that have revolutionized the modern electronics world,[1] organic nonvolatile memories have been emerging as a promising data-storage technology for specific applications that need to be mechanically flexible and robust as well as portable.[2–7] Among the many approaches, chargeable organic transistor memory (COTM) which exploits the electrical bistability originating from the modulation of channel conductance by charge trapping in the gate dielectric systems confers unique advantages such as nondestructive data read-out, circuit architectural compatibility, single transistor realization, and reliable switching characteristic.[2,5,6] Among the tremendous research progress over the past decades, much attention has been focused on exploring architectures based on floating gates[8–21] and chargeable electrets[22–27] using different materials systems, including small molecule, conjugated polymer as well as oxide semiconductors. Substantial improvements in flexibility,[9,19,28] memory window (MW) and retention, capability of multibit storage,[25] and realization of new functionalities, for example, pressure sensors integrated into memory arrays[19] have been achieved. An important aspect of memory operation that has received comparatively little attention has been writing speed, which is an important specification for not only the feasibility of potential high-end applications such as organic solid-state drives and fast organic sensors (where the incorporated memory units need to record the fast signals from the sensor) but also the fundamental, scientific understanding of the physics of charge transfer from an organic semiconductor into different gate dielectrics.

The writing timescales reported for COTMs based on chargeable gate systems range from microseconds to seconds.[8–27] In terms of writing speed polymer electret-based architectures tend to outperform floating-gate devices as the latter inevitably comprise relatively thick tunneling dielectrics to ensure reliable isolation of the floating gates. Notably, most reported COTMs are based on planar transistor configurations with typically micrometer channel lengths and unipolar semiconductors, which fundamentally limit achievable operating speed: In such configurations the timescale for both write and read operation is limited by the lateral transport of carriers along the channel, which is slow because of the low mobility of charges in organic semiconductors. Furthermore, in unipolar materials if the one memory state, say the erase (E) operation, is based on threshold voltage shifts (V_{Th}) induced by relatively mobile majority carriers while the transistor is in its ON state, then the other memory state obtained during the programming (P) cycle is slow because it relies on very low mobility minority carrier transport during the transistor OFF state.[29,30] Therefore, apart from the development of favorable chargeable materials systems, novel device configurations are needed that allow downscaling of channel lengths and fast ambipolar charge accumulation within the layer adjacent to the chargeable gate. Straightforward downscaling of channel length in a planar ambipolar transistor is challenging because the OFF current in such devices tends to be high and the high symmetry of *I*–*V* characteristic increases the risk of accidentally writing the desired OFF state into the ON state after many P/E operations, when V_{Th} is expected to exhibit variations because P and E operations may not be perfectly compensated with each other. This is particularly relevant for low-voltage memory operation. For highly reliable memory operation it is preferable to maintain quasi-unipolar *I*–*V* characteristics in spite of the prerequisite of employing ambipolar materials for high speed electron/hole injection.

Here, we report a new memory architecture based on a short channel, vertical organic transistor (VOT) comprising a bilayer of a high-performance ambipolar conjugated copolymer based on diketopyrrolopyrrole (DPP) in contact with a polymer electret gate dielectric and a unipolar pentacene layer on top that maintains quasi unipolar *I*–*V* characteristics. The vertical device is defined precisely by a photolithographic process compatible with organic materials.[31] We demonstrate fast memory operation within 150 ns (P) and 50 ns (E).

A schematic illustration of the memory designed in this work is shown in **Figure 1**a. A first dielectric layer of aluminum oxide, that acted as a control dielectric, was grown by atomic layer deposition (ALD) on a prepatterned gold gate followed by a second, spin-coated dielectric layer of poly(2-vinylnaphthalene) (PVN) (chemical structure seen in Figure S1, Supporting Information). PVN is a widely used polymer electret that allows efficient and fast trapping of both positive and negative charge carriers.[23] The thickness of both layers was kept small (AlO_x—40 nm, PVN—12 nm). The small PVN thickness is expected to lead to relatively poor retention charateristics[32] but is necessary to enable low voltage operation. Both the AlO_x and PVN films exhibit smooth surfaces with root-mean-square (rms) roughness below 1 nm (Figure S2, Supporting Information). The ambipolar polymer semiconductor, poly(*N*-alkyl-diketopyrrolo-pyrrole dithienylthieno [3, 2-b] thiophene)

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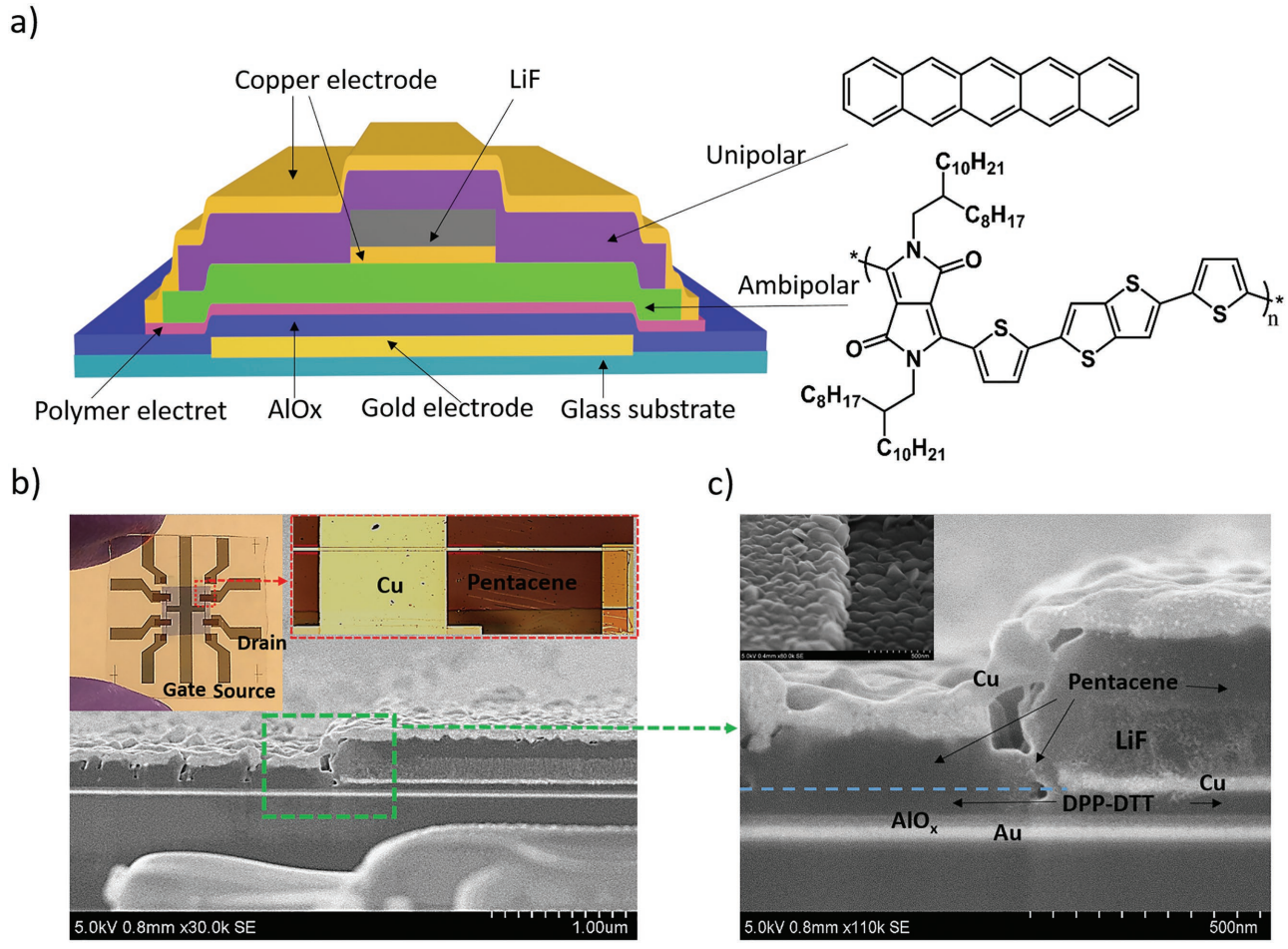

Figure 1. a) (Left) Schematic, cross-sectional diagram of the vertical transistor memory architecture and (right) molecular structures of pentacene and DPP-DTT. b) SEM image of the device cross-section prepared by FIB, insets: photographs of device, (left) whole substrate containing four devices, and (right) single device. c) Zoomed-in SEM images of the area marked in green in (b), inset: SEM image of pentacene film across the edge of the source electrode before depositing the top drain electrode.

(DPP-DTT) (chemical structure in Figure 1a) was spin coated onto a silicon substrate that had been pretreated with octadecyltrichlorosilane (OTS) modification. We use DPP-DTT because it is a high mobility ambipolar polymer that allows achieving high carrier mobilities on the order of 1 cm^2 $(V\ s)^{-1}$ for both electron and hole carriers. The film thickness was 35 nm. Afterward the DPP-DTT film was printed onto PVN through a stamp-printing method using PDMS (polydimethylsiloxane) (see in Figure S3, Supporting Information). This complicated deposition process was necessary, as DPP-DTT is not soluble in any solvents that are orthogonal for PVN and direct spin coating of DPP-DTT onto PVN would have led to swelling/dissolution of the underlying PVN layer. The source electrode was then formed by evaporating metallic copper (20 nm) and insulating lithium fluoride (LiF, 100 nm) on top of the DPP-DTT substrate and patterning these layers by an orthogonal, fluorosolvent-based photolithography technique that does not degrade organic materials (see Figures S3 and S5, Supporting information). The fabrication process was finalized by depositing an 80 nm layer of pentacene as the vertical transport layer and a 20 nm layer of copper as the top drain electrode by thermal evaporation through shadow masks (see photographs inserted in Figure 1b). We used copper as the source electrode to ensure reasonably balanced electron and hole injection into DPP-DTT. Sample cross-section was prepared by focused ion beam (FIB) and imaged by high-resolution scanning electron microscope (SEM). The SEM results are presented in Figure 1b,c, showing that the multilayer structure of the device is well defined in accordance with the schematic diagram in Figure 1a.

Vertical organic transistors have been attractive because their ultrashort channel length (L_C) defined in our case by the combined thickness of the DPP-DTT and pentacene layers enables high current output. Different operating mechanisms have been proposed to explain various architectures of VOTs.[33–42] Our device is inspired by the architecture recently reported by Kleemann et al.[41] We will now explain the transistor operation with reference to **Figure 2**a,d. When a negative bias is applied to both the gate and drain, holes are injected from the source into the ambipolar DPP-DTT layer and form a hole accumulation layer at the DPP-DTT/PVN interface. Across the contact injection area of the source the drain–source current (I_D) flows laterally along the interface and is subsequently

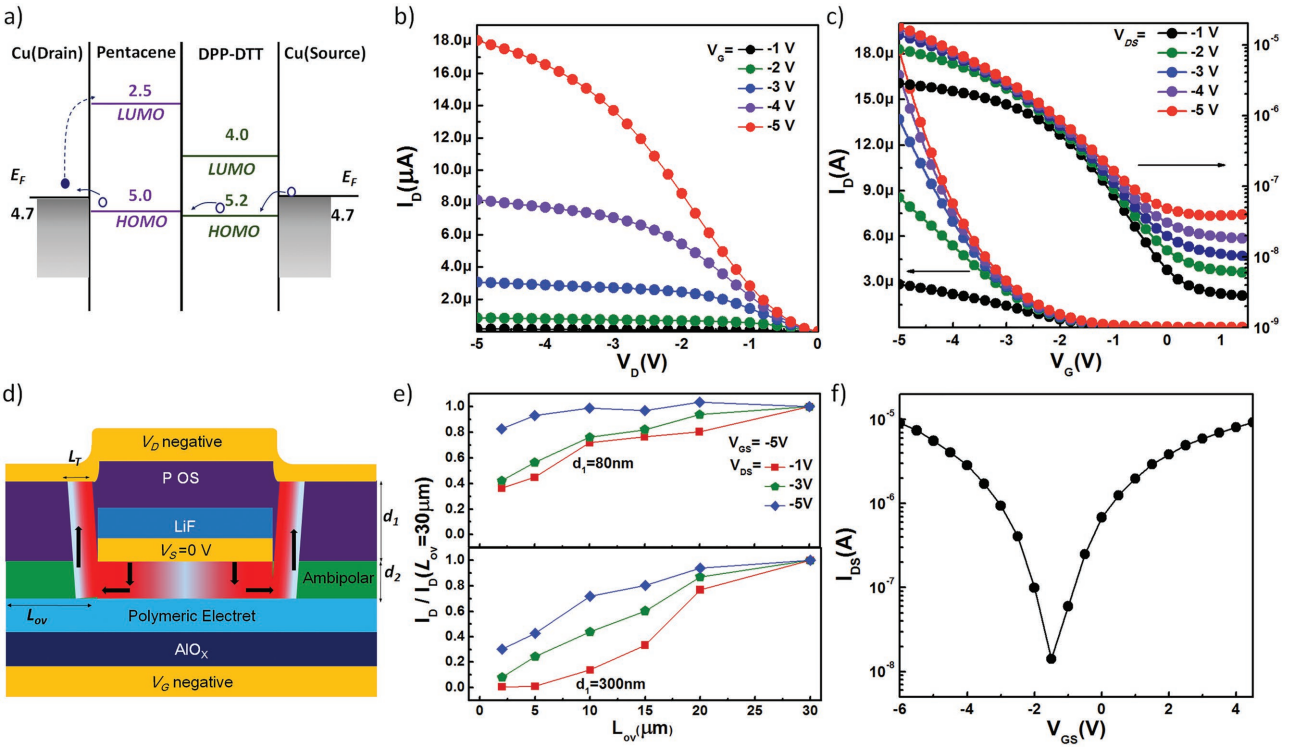

Figure 2. a) Energy diagram illustrating the relevant energy barriers encountered by holes (hollow sphere) and electrons (solid sphere) of DPP-DTT/pentacene vertical memory, referred as AVM (ambipolar vertical memory). b,c) Output and transfer characteristics of AVM with 80 nm pentacene. d) Schematic illustration of spatial current distribution in red. e) Reduction of the drain current measured at $V_{GS} = -5$ V when L_C is scaled from 30 to 2 μm. Different source–drain biases are marked in different colors. The top plot represents AVM comprising 80 nm pentacene, while the bottom plot is for a device with 300 nm pentacene. f) Transfer characteristics of DPP-DTT lateral ambipolar device on PVN (12 nm)/AlO_x (40 nm)/Au, with top copper electrodes patterned by photolithography and DPP-DTT transferred onto PVN by stamp printing.

transported vertically through the pentacene layer and collected by the drain. Note that the highest occupied molecular orbitals (HOMO) of DPP-DTT and pentacene are well matched to facilitate the vertical transport in the p-type regime. On the other hand, when keeping the drain voltage unchanged and switching the gate to a positive bias, the current I_D should be transported into electron flow from drain to source. However, this is suppressed by the large electron injection barrier (φ_e) (≈1.8 eV) between the drain and pentacene (Figure 2a). Therefore, our design is expected to exhibit a quasi-unipolar p-type characteristic despite the use of an ambipolar semiconductor in contact with the gate dielectric. Figure 2c shows the measured transfer characteristics of the device, which are indeed unipolar, p-type. This is in contrast to conventional planar devices with DPP-DTT as the active semiconductor layer, which exhibit clear ambipolar characteristics (Figure 2f). The ON/OFF ratio of the vertical device is nearly 10^3 between $V_G = -5$ and 0 V. Although this is clearly smaller than values of 10^6–10^8 which can be achieved in state-of-the-art planar devices with unipolar semiconductors, it is comparable to that of the ambipolar DPP-DTT planar devices. When the drain–source bias (V_{DS}) increases from –1 to –5 V, the OFF current increases by nearly one order of magnitude, indicating that the OFF current is modulated by V_{DS}. The moderately low OFF current is attributed to the LiF layer which acts as a blocking dielectric substantially reducing the area for leakage current between drain and source and suppresses the short-channel effect in our device as reported in refs. [41] and [43]. Note that the edge of copper layer (source) might be covered by LiF at least partially, since the postevaporation of a relatively thick LiF layer on top of a thin copper layer before lift-off might result in diffusion of LiF molecules around thin copper edge during deposition, and this could contribute to reducing the OFF current. It is found in Figure 2c and in the output characteristics of Figure 2b that I_D is relatively limited at low drain biases. This suggests that the vertical resistance from DPP-DTT to the drain through pentacene plays a dominating role in determining the current. A larger drain bias is required to drive a large I_D through the vertical channel.

The motivation of our work is to achieve fast memory operation. To realize this, it is important to characterize and minimize L_T (defined as a characteristic length of current spatial distribution near the drain contact, illustrated in Figure 2d). The larger L_T the more lateral current flow along the DPP-DTT/PVN interface is involved in device operation which is expected to lengthen the effective channel length and slow down device operation. Herein, we studied the evolution of I_D ($V_G = -5$ V) when L_{ov} (defined as the overlapping between gate and drain, excluding the part beneath source, shown in Figure 2d) was scaled from 30 to 2 μm. Figure 2e shows how I_D degrades when L_{ov} is reduced. However, this degradation can be significantly suppressed by increasing the drain bias or by reducing the pentacene thickness. This suggests that a large drain bias facilitates

vertical transport and causes the vertical current profile to narrow. The lowering of the pentacene thickness contributes to reduction of vertical resistance with respect to lateral resistance, and thereby benefit the minimization of L_T, referring to the charge crowding model.[44–47] This suggests that in terms of our memory, reducing the pentacene thickness and employing large drain bias is an effective, controllable way for L_T shortening. The results in Figure 2e show that in the memory devices built with a thin layer of pentacene ≈80 nm and operated with $V_G = -5$ V, $V_D = -5$ V nearly 80% of I_D is confined in a short region, $L_T \approx 2$ µm. In contrast, a large bulk resistance associated with a thick (300 nm) pentacene layer spreads out the vertical transport channel over 10's of micrometers. The L_T under the drain can be further downscaled through further optimization approaches, for example doping of the semiconductor bulk to enhance the conductivity of the vertical transport layer and doping of the contacts to reduce contact resistance effects, as reported in lateral transistor studies.[48,49] Additionally, it should be noted that the current profile under the source is also likely to play a role, as it determines the transport path for carriers injected from the source toward L_T region after injection. However, this is not further investigated here, as the source contacts are fabricated in an identical manner for both vertical and lateral architectures, though we emphasize that narrowing the injection area underneath the source, reducing current crowding though contact resistance optimization is also likely to result in further speed improvements.

We first present in **Figure 3** the high-speed writing performance of our DPP-DTT/pentacene vertical memory. We refer to this structure as AVM (ambipolar vertical memory) to distinguish it from the more conventional lateral device architectures using either pentacene or DPP-DTT to which we refer as ULM (unipolar lateral memory, structure shown in Figure S6, Supporting Information) and ALM (ambipolar lateral memory, structure shown in Figure S6, Supporting Information), respectively. In the following section we will discuss the mechanism for the fast writing behavior with reference to **Figure 4**. A typical memory transfer loop is shown in Figure 3a, where the scanning of V_G produces considerable V_{Th} shifts with the same polarity as the applied V_G manifesting themselves as a large anticlockwise hysteresis (Note that the observation of some electron current at positive gate voltages here is due to the large positive gate biases compared to Figure 2c). The bias time for each V_G point in this scan is on the order of ten milliseconds, which is more than long enough for carrier accumulation at the interface and carrier injection into the PVN electret. Such dual V_G scan within ±16 V produces a large MW comprising a positive V_{Th} shift around 6.1 V ($\Delta V_{Th+} \approx 6.1$ V, logic 1) and negative shift around −7.7 V ($\Delta V_{Th-} \approx -7.7$ V, logic 0) with respect to the initial characteristics. Note that the positive V_{Th} shift enables nondestructive read-out, since it allows logic 1 to be read at $V_G = 0$ V. MWs induced by high speed writing were characterized by applying short voltage pulses with dual polarities at the gate. Importantly the measurements were taken in high vacuum (10^{-6} Torr) to avoid suppression of writing speed by ambient gases.[29,32] In Figure 3b, our AVM device demonstrates fast response where $\Delta V_{Th+} \approx 3.61$ and $\Delta V_{Th-} \approx -3.13$ V is induced by 150 ns pulses at $V_G = 35$ V (P) and 50 ns pulses

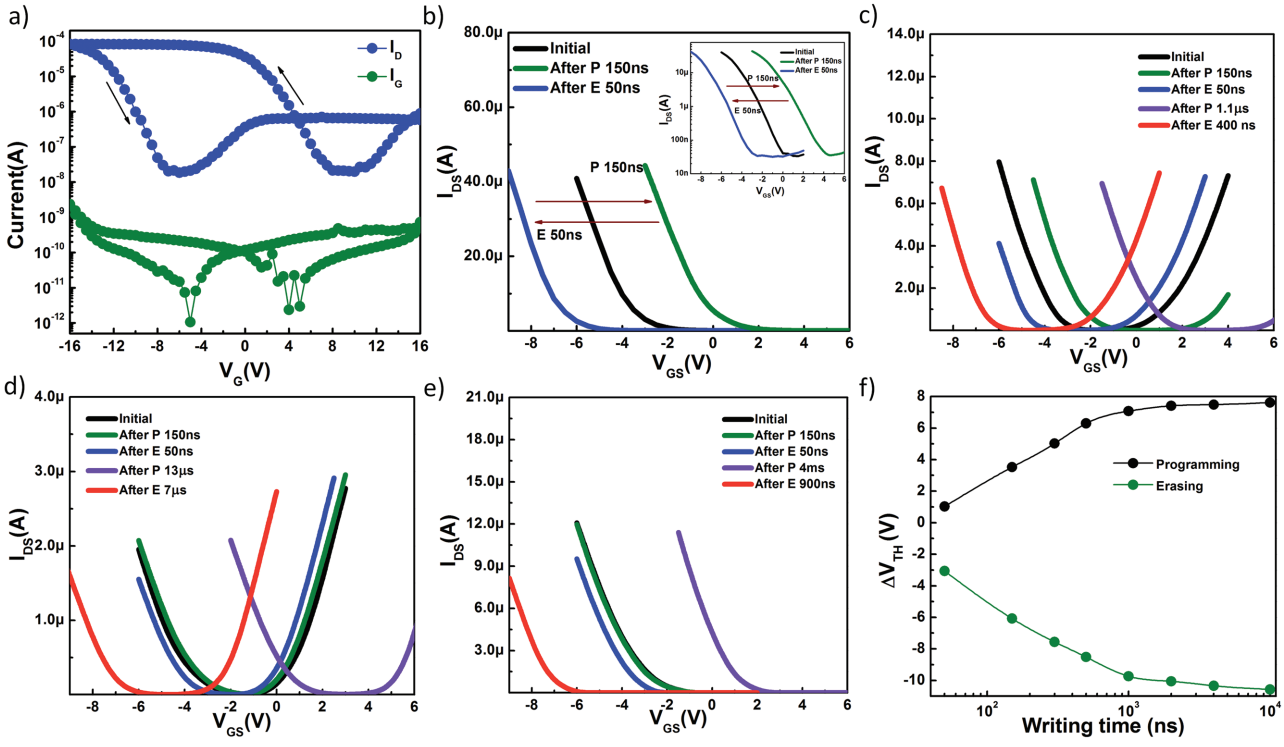

Figure 3. a) Memory transfer loop of AVM. b) Shift of transfer curve of AVM after 150 ns programming and 50 ns erasing. Corresponding shifts of transfer curve for ALM with channel length of c) 20 µm and d) 200 µm and e) for a 20 µm ULM. f) Writing time dependence of threshold voltage shifts of AVM.

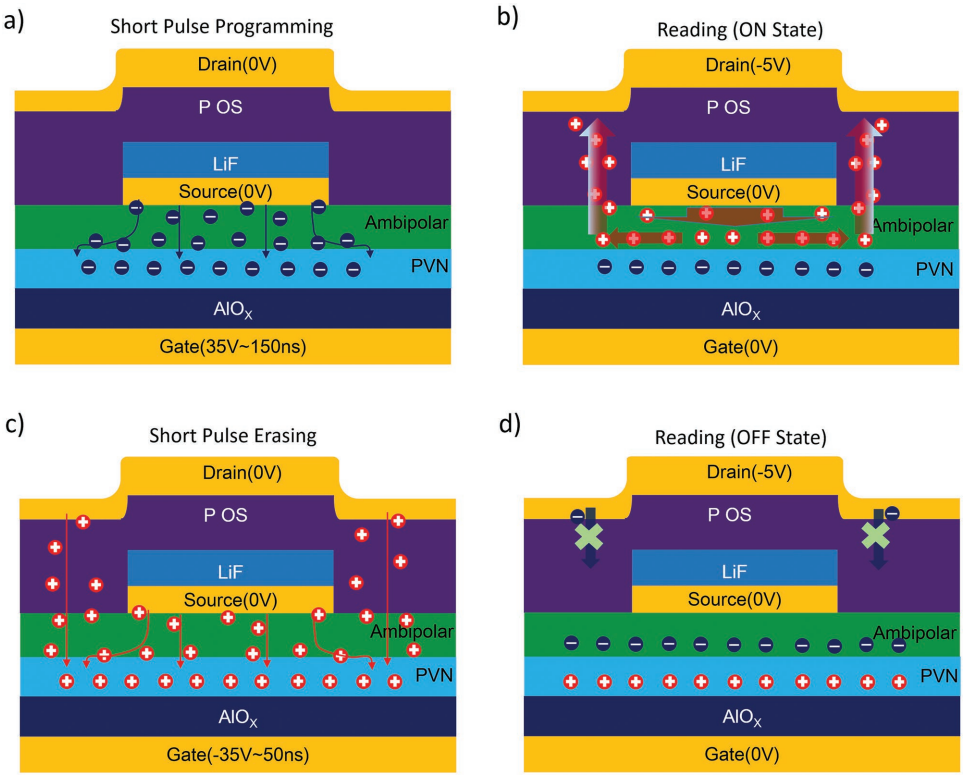

Figure 4. Schematic illustrations of different phases of memory operation. a) Programming process, where L_T region is negatively charged by fast electron accumulation from source during 150 ns at $V_{GS} = 35$ V; b) on state reading at $V_{GS} = 0$ V and $V_{DS} = -5$ V; c) erasing process, where L_T region is positively charged by fast hole accumulation from source and drain during 50 ns at $V_{GS} = -35$ V; d) OFF state reading at $V_{GS} = 0$ and $V_{DS} = -5$ V.

at $V_G = -35$ V (E), respectively. Application of nanosecond pulses with $V_G = \pm 35$ V did not cause breakdown of the 40 nm aluminum oxide, though breakdown was sometimes observed when prolonged pulses approximately milliseconds at these voltages were applied. This superior insulating performance of our alumina oxide reflects the high quality of the ALD deposited films. In order to verify the speed advantage of our design, we also fabricated conventional DPP-DTT and pentacene lateral transistor memories with the same gate dielectric thicknesses as reference devices. The corresponding transfer curve shifts under 150 ns P ($V_G = 35$ V)/50 ns E ($V_G = -35$ V) are presented in Figure 3c–e (device mobility is shown in Table S1, Supporting Information). Compared to $\Delta V_{Th+} \approx 3.61$ V/$\Delta V_{Th-} \approx -3.13$ V in AVM, significantly smaller $\Delta V_{Th+} \approx 1.32$ V/$\Delta V_{Th-} \approx -1.08$ V (Figure 3c) and $\Delta V_{Th+} \approx 0.23$ V/$\Delta V_{Th-} \approx -0.39$ V (Figure 3d) are obtained for DPP-DTT lateral memories (ALM) with channel lengths $L_C = 20$ and 200 µm, respectively. The most commonly used pentacene lateral memory (ULM) with $L_C = 20$ µm demonstrates exhibits negligible ΔV_{Th+} and $\Delta V_{Th-} \approx -0.55$ V (Figure 3e) for such short writing pulses. To achieve comparable ΔV_{Th} of around 3 V which AVM achieves in 150 ns (P) and 50 ns (E), respectively, a much longer writing time is needed for these lateral devices. For the lateral devices we need ≈1.1 µs (P)/≈400 ns (E) for $L_C = 20$ µm ALM (Figure 3c), ≈13 µs (P)/≈7 µs (E) for $L_C = 200$ µm ALM (Figure 3d), and ≈4 ms (P)/≈900 ns (E) for 20 µm ULM (Figure 3e) to achieve comparable shifts. The prolonged P/E process of 200 µm ALM devices over 20 µm ones reflects the effect of the lateral transport delay. The dramatically slower P process of 20 µm ULM with respect to 20 µm ALM devices results from the slow electron accumulation in unipolar pentacene devices compared to ambipolar DPP-DTT devices. Both of these speed limiting effects are minimized in our AVM design which gives the fastest P/E response as demonstrated above. We also note that despite the reasonably balanced electron/hole mobility in DPP-DTT, the erasing process occurs faster than the programming one in both AVM and ALMs. One possible reason for this is that there is likely to be a difference in the source contact injection barrier for electrons and holes. The energy level diagram in Figure 2a suggests that the hole injection barrier which is determined by the offset between the Fermi level of copper and the HOMO level of DPP-DTT is smaller than the corresponding electron injection barrier determined by the offset between the copper Fermi level and the LUMO (lowest unoccupied molecular orbital) level of DPP-DTT. This is consistent with the P process being slower than the E process; however, a possible, alternative explanation will be discussed in the other part of the following. We also characterized the writing time dependence of MWs (Figure 3f) by measuring ΔV_{Th} after applying writing pulses with different pulse duration to the AVM. The increase of ΔV_{Th+} and ΔV_{Th-} over t_p (programming time) and t_e (erasing time) is found to initially follow a logarithmic relationship that is common for Fowler–Nordheim tunneling.[32] For writing time exceeding about 1 µs ΔV_{Th} tends to saturate possibly because we are reaching a charging limit in the polymer electret due to a columnar charge blocking effect. In summary, our AVM design enables significant improvement

in P/E speed, and the systematic comparison between vertical and lateral architectures confirms the beneficial effect of channel length shortening and high-speed ambipolar accumulation on memory speed.

We now discuss the mechanism for fast writing with reference to Figure 4. In principle, the writing time needed for the effective gate modulation region to be sufficiently charged is determined by the scale of L_T and the speed of carrier accumulation at the DPP-DTT/PVN interface. We have shown above that the effective length L_T of the interface region extending beyond the edge of the source electrode to which the vertical current flow is confined is on the order 2 µm. Together with fast carrier accumulation in DPP-DTT, it enables that within $t_p \approx 150$ ns V_G (35 V), the short PVN region beneath L_T can be reached by electrons injected from the source and negatively charged under the spontaneous tunneling electrical field (E_T), as shown in Figure 4a. Subsequently, this negatively charged state can be read by measuring the current at $V_G = 0$ V, $V_D = -5$ V, as drawn in Figure 4b, where considerable hole current is flowing due to the negative trapped charge density Q_t within the PVN under L_T region, representing the logic state 1. Figure 4c illustrates the fast erasing operation, where one process (similar to programming) is that within $t_e \approx 50$ ns PVN under L_T region is positively charged by the fast accumulation of holes from the source. A second contributing pathway is likely to be the hole injection into PVN from the drain though pentacene, which is potentially fast due to the short distance (≈120 nm), high hole mobility, and favorable energy alignment (Figure 2a). It is possible that the combination of the two pathways is in fact the reason that erasing is faster than programming, and not the above-mentioned difference in injection barriers of electrons and holes. As shown in Figure 4d, the reading of this logic 0 state at $V_G = 0$ V, $V_D = -5$ V involves measuring the electron current through the channel which is very small due to the significant electron injection barrier at the interface between the copper drain and pentacene (Figure 2a). Note that such process of logic 0 writing can be ensured even if V_{Th} is accidentally overerased to some extent, owning to the relatively broad OFF current modulation region in the quasi-unipolar I–V characteristics as shown in Figure 2c compared with ambipolar one in Figure 2f.

To further investigate the contribution of the two mechanisms to the erasing process, we reconducted the ΔV_{Th} measurements with same writing pulses as Figure 3b (150 ns 35 V/50 ns −35 V), but set the drain to floating to avoid charge injection from the drain. The results are demonstrated in Figure S4 (Supporting Information), with respect to the V_{Th} shifts in Figure 3b, ΔV_{Th+} is approximately comparable, while ΔV_{Th-} is apparently reduced by ≈1.3 V. This reduction of ΔV_{Th-} indicates that the fast erasing functionality does in fact arise from injection from both source and drain, as shown in Figure 4c, while the comparable values of ΔV_{Th+} confirms the negligible contribution from electron injection from the drain during the fast programming process, as shown in Figure 4a.

Finally, we have characterized memory retention performance (**Figure 5**). After 150 ns programming, the ΔV_{Th+} shows relatively poor stability over time, it relaxes rapidly from 3.5 to 2.1 V within the first 40 min. Subsequently, the relaxation rate was gradually reduced, ΔV_{Th+} decreased to 1.4 V during the subsequent 140 min. It took about two days for ΔV_{Th+} to

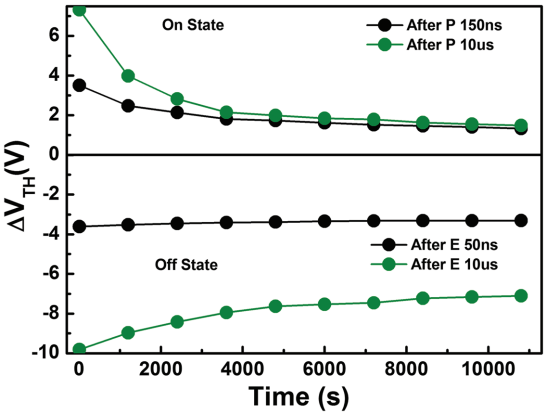

Figure 5. AVM retention characteristics after 150 ns programming, 50 ns erasing (black), and after 10 µs programming and erasing (green).

completely vanish. In contrast, after 50 ns erasing, the relaxation of ΔV_{Th-} is surprisingly slow, only 0.3 V degradation was observed after 180 min. The memory retains nearly half of its initial ΔV_{Th-} value even after one week. A similar trend is observed in the case where programming and erasing pulses are prolonged to 10 µs. The results suggest that the faster dissipation of trapped charge in PVN for electrons than for holes may not be associated with the injection depth but could reflect different trapping mechanisms for electrons and holes in PVN that have not been understood yet. According to the literature, the nonideal retention performance can be much improved by increasing the thickness of PVN owning to deep trapping.[23,26,50] Nevertheless, practical applications are in favor of low-power operations, which suggests that it will be necessary to develop better electret materials that can achieve fast but more stable charge trapping in ultrathin films.

In summary, we developed a new vertical transistor architecture for memory applications, which incorporates down-scaled gate modulation, fast ambipolar accumulation, and quasi-unipolar transport to achieving a significant improvement in the speed of reliably switching between 0 and 1 states. By minimizing the charging delays associated with long channel length and avoiding slow minority carrier accumulation, our design provides a route to realizing fast chargeable gate systems that could meet the requirements for fast organic-based memories that will be needed for a wide range of flexible electronic applications, such as identification tagging at standard compatible frequencies or rapid sensor signal monitoring. Our vertical transistor memory architecture can be applied to new polymer electret materials that will need to be developed in the future to improve, in particular, the retention characteristics of thin polymer electret films and potentially also to different memory effects, such as ferroelectric transistor memories.

Experimental Section

20 nm Au/3 nm Cr were patterned on clean glass substrates by standard lithography as the gate electrode, followed by deposition of 40 nm aluminum oxide grown by ALD as the control dielectric. A solution of PVN solution in toluene (3 mg mL^{-1}) was spin coated on top of the alumina layer at room temperature (3000 rpm for 30 s) and

annealed at 100 °C for 5 min to form the chargeable electret dielectric. The DPP-DTT film was spin coated (1500 rpm for 15 s) onto an OTS-treated silicon substrate from a solution in 1,2-dichlorobenzene solution (5 mg mL^{-1}) and then transferred onto the PVN substrate by PDMS stamp printing.[51] A copper source electrode and a LiF dielectric were patterned onto DPP-DTT by a bilayer lithography process using fluoride resist OSCoR 4000 (Orthogonal Inc.) as a bottom, protecting layer and a S1813 (Microposit) resist layer on top, seen in Figure S5 (Supporting Information). After depositing copper (20 nm) and LiF (100 nm), the whole resist layer was removed by lifting off OSCoR 4000 in a fluoride solvent, HFE (3 M), to form a vertical wall for pentacene channel which was afterward thermal deposited through shadow mask in high vacuum (10^{-6} Torr). A detailed process flow of the lithographic patterning can be found in Figure S5 (Supporting Information). The fabrication process was finalized by depositing the top copper electrode through shadow mask. The electrical measurements were taken with an Agilent 4156 C and Keithley 4200 SCS in vacuum chamber and in the dark environment. Pulses were generated by a 4220-PGU unit (the rise time (10–90%), fall time (90–10%), and the peak duration time (90% to the peak then down to 90%) for 35 V 150 ns is about 60, 65, and 95 ns, while that for −35 V 50 ns is about 60, 60, and 30 ns). AFM (atomic force microscopy) images were performed using a Veeco Multi-Mode SPM (scanning probe microscopy). The SEM images were taken with a Hitachi S-5500 and cross-section samples were prepared by FEI-FIB 200.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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