Back Gated Multilayer InSe Transistors with Enhanced Carrier Mobilities via the Suppression of Carrier Scattering from a Dielectric Interface

*Wei Feng, Wei Zheng, Wenwu Cao, and PingAn Hu**

Graphene-like two-dimensional (2D) layered semiconductors hold great promise for next generation nanoelectronics devices after the silicon era. These 2D layered semiconductors exhibit structural characteristics of unique dimensionality, ultrathin thickness and atomic flatness, which are attractive for miniaturization and high performance of electronic devices.[1] 2D structure offers compatibility to silicon based COMS processing, such as photolithography for large-scale fabrication. Ultrathin thickness allows better electrostatic control of electrical conductivity, and significant device downscaling for high density integration. Atomically flat surface together with the absence of dangling bonds make 2D semiconductors free from carrier scattering caused by surface roughness, so that 2D semiconductors based transistors could outperform silicon devices in scaling limitation.[1] A number of studies have been made in field effect transistors (FET), a central building element for logic circuit, by exploiting monolayer or few-layer 2D semiconductors as transport channel.[1–8] So far, 2D layered materials used in FETs fabrication are mainly transition metal dichalcogenides (TMDs) of 2D molybdenum disulfide (MoS_2) and selenium tungsten (WSe_2).[1–8] However, it has been demonstrated that MoS_2 is an undesirable material for high performance electronics applications because of heavier electron effective mass ($m^* = 0.45\ m_0$) and low room temperature mobility of 50 ~ 200 $cm^2V^{-1}s^{-1}$.[3] The reported ultrathin MoS_2 channels show low carrier mobility of μ ~ 1–50 $cm^2V^{-1}s^{-1}$. Several strategies have been demonstrated to improve the performance of ultrathin MoS_2 FETs, including exploiting high k dielectrics[2] or decreasing the contact barrier.[6] Multilayer MoS_2 on Al_2O_3 substrate show improved mobility of μ > 100 $cm^2V^{-1}s^{-1}$ and good sub-threshold swings.[4] Encapsulating MoS_2 in high-K dielectric[2] or a polymer electrolyte enhanced the mobility up to ~160 $cm^2V^{-1}s^{-1}$.[5] With PMMA/Al_2O_3 bilayer dielectric, the mobility of multilayer MoS_2 FETs is increased to 500 $cm^2V^{-1}s^{-1}$, however, the intrinsic mechanism for this mobility improvement is still not well understood.[7] Very recently, two-terminal measurements of few-layer black phosphorus FETs show a carrier mobility of 284 $cm^2V^{-1}s^{-1}$ at room temperature,[10] which is much higher than that of MoS_2 FETs.[1–9] However, few layer black phosphorus is less stable than graphene and MoS_2.[10] In general, it is very challenging to enhance carrier mobilities of layered semiconductor devices.

The performance of 2D layered semiconductor FETs can be significantly influenced by the interface of dielectric/2D semiconductors, where exist various carrier scattering centers and charge traps.[11–14] In addition to the intrinsic acoustic phonon scattering of 2D layer materials, interfacial Coulomb impurities (CIs), surface roughness (SR) and surface polar phonon scattering (SPP) from the adjacent dielectric can all impact the carrier transport in the electronic devices.[11–14] Especially interfacial Coulomb impurities from the substrate can become the leading carrier scatter in ultrathin layered semiconductor channels, which significantly decrease the mobilities of FETs because the distance between CIs and carriers are largely shortened in ultrathin materials.[9] Conventionally used dielectric substrates of oxide layers, such as SiO_2, Al_2O_3, HfO_2 etc., have a lot of hydroxyl groups and other charge traps at the surface,[10–12] which contribute to the CIs or SSP scattering and the reduction of carrier mobilities. The carrier mobilities of 2D semiconductor based FETs may be improved by the suppression or even elimination of CIs or SPP scattering from the support substrate. It has been demonstrated that the performance (mobilities, stability) of graphene FETs are efficiently enhanced by coating organic self-assembled monolayers (SAM) onto the dielectric layer of substrate.[14,15]

Indium selenide (InSe) is a typical lamellar semiconductor belonging to III–VI group compounds. The β-phase and γ-phase are two common forms of InSe, possessing a layered crystal structure. Bulk InSe is composed of vertically stacked Se-In-In-Se sheets and each sheet is weakly bound to its neighboring sheets by van der Waals force (**Figure 1**a Inset). Similar to the fabrication of monolayer or few-layer MoS_2 or other graphene-like 2D semiconductors (GaSe,[16] GaS,[17] GaTe,[18] few-layer InSe nanosheets can be mechanically extracted from the parent bulk structure. InSe has lighter electron effective mass ($m^* = 0.143m_0$),[19] and show a high carrier mobility

W. Feng, W. Zheng, Prof. P. A. Hu
State Key Laboratory of Robotics and System
Harbin Institute of Technology
Harbin 150080, China
E-mail: hupa@hit.edu.cn
Prof. W. W. Cao
Condensed Matter Science and Technology Institute
Harbin Institute of Technology
Harbin
Prof. W. W. Cao
Department of Mathematics and Materials Research Institute
the Pennsylvania State University
University Park, Pennsylvania 16802, USA
W. Feng
School of Materials Science and Engineering
Harbin Institute of Technology
Harbin 150080, China

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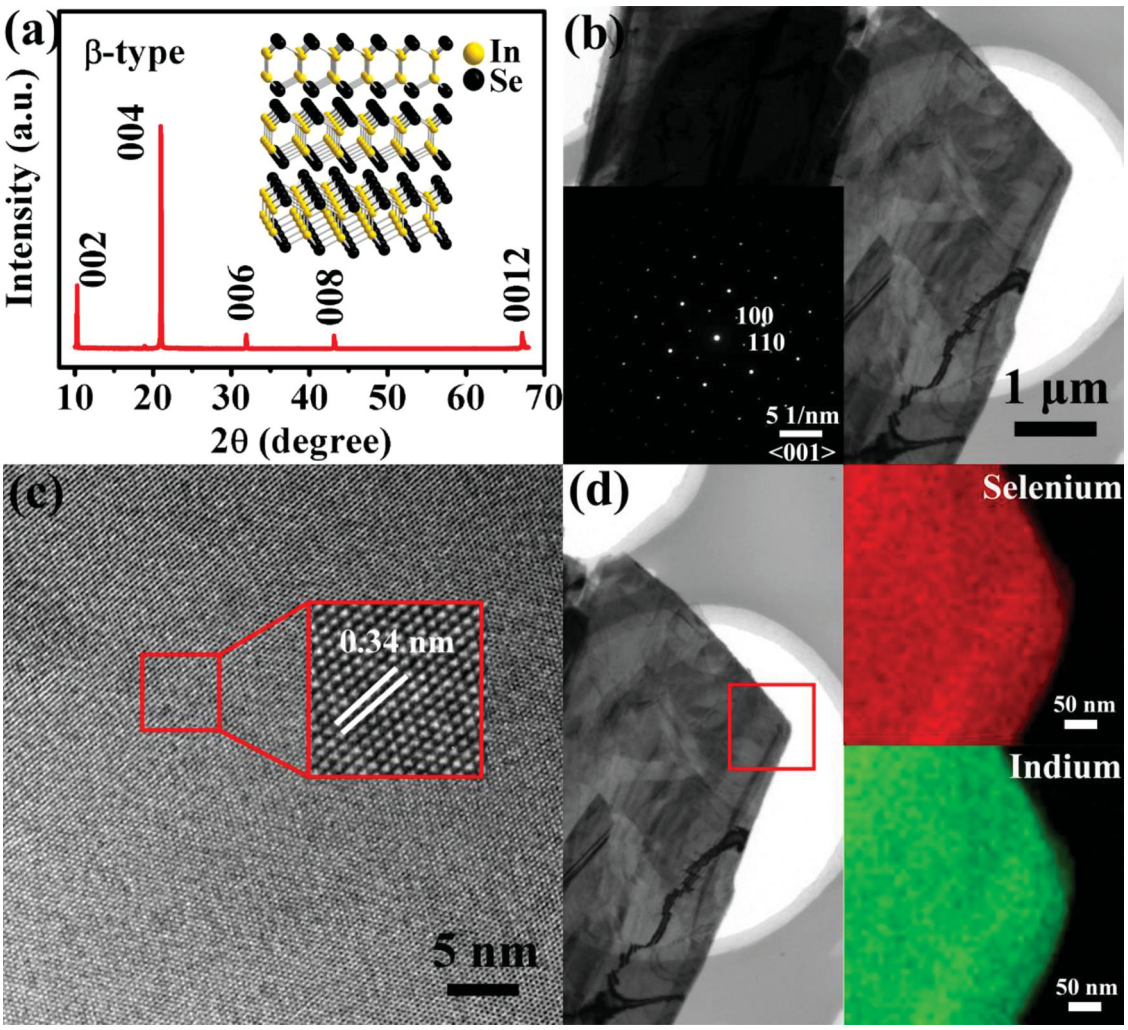

Figure 1. Characterization of InSe sheet: (a) XRD pattern of InSe sheet. Inset: InSe crystal structure. (b) TEM images of multilayer InSe at low magnification. Inset: the corresponding SAED pattern. (c) HTEM image for few layer InSe. Inset: the corresponding reverse Fourier transform pattern. (d) Elements mapping images.

of ~10^3 $cm^2V^{-1}s^{-1}$,[20] which makes them potential material for high mobility electronic devices. Other features favorable for high performance nano-electronic devices include the absence of dangling bonds and high thermal stability up to 660 °C. Recently, the thickness dependent photoluminescent properties of exfoliated InSe nanosheets have been demonstrated, showing a strong quantum confinement effect.[21] Multilayer InSe photodetectors on rigid and flexible substrate show broadband photodetection from visible to near-infrared region with high responsivity.[22,23] Although photodetectors based on InSe have been demonstrated, investigation on the application of InSe in electronic devices, such as InSe FETs is limited up to date.

Here, we discovered that carrier scattering from chemical impurities of hydroxyl groups and absorbed water molecules at oxidized dielectric plays a central role in determining the mobilities of 2D layered semiconductor based FETs, and the suppression of this carrier scattering can significantly enhance their performance. Further, we demonstrate high performance multilayer InSe transistors on poly-(methyl methacrylate) (PMMA)/Al_2O_3 bilayer dielectric with a room-temperature mobility >1000 $cm^2V^{-1}s^{-1}$, which is comparable to that of strained-silicon thin-film (mobility 1000 $cm^2V^{-1}s^{-1}$).[24] This improved ultrahigh carrier mobility are obtained due to the suppression of interfacial coulomb impurities scattering or SPP at interface of oxidized dielectric substrate after coating with PMMA. The transistors show high current on/off ratios of 1×10^8, low standby power dissipation and robust current saturation in a board voltage range. We found that this carrier scattering shows a thickness-dependent impact on the mobilities of multilayer InSe FETs, and more strong impact on the mobilities inside thinner InSe FETs. All these fascinating traits make multilayer InSe an attractive candidate material for high performance nano-electronic devices.

The synthesized bulk InSe samples were characterized by X-ray diffraction (XRD), and transmission electron microscopy (TEM). Since the properties of InSe strongly depend on its crystal structure, it is important to confirm the crystallographic phase of synthesized InSe sample. Figure 1a shows a typical XRD pattern of the hexagonal crystal structure of β-InSe, which is determined by the standard data file (PDF34–1431). Only

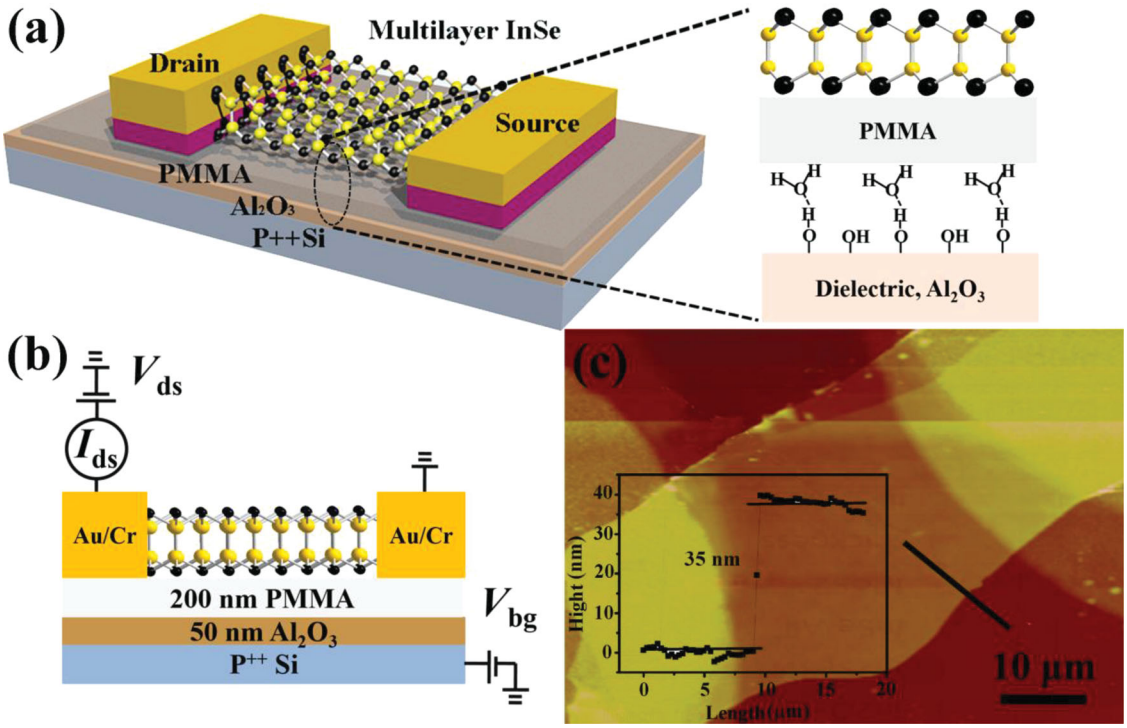

Figure 2. (a) Schematic of back-gate multilayer InSe FETs consisting of PMMA/Al_2O_3 back gate insulator, Au/Cr electrodes (40/20 nm). (b) Cross-sectional view of structure of the two-contact model. (c) Corresponding atomic force microscopy of multilayer InSe FETs. Inset: corresponding height profile of 35 nm.

peaks for hexagonal crystal structure of β-InSe appear without any other impurities peaks, suggesting high crystalline purity of as-synthesized InSe crystal. In Figure 1b, a low magnification TEM image of InSe nanosheet together with an inset for the selected area electron diffraction pattern (SEAD) provides another evidence for the formation of single phase crystalline β-InSe flakes with an orientation along the [100] zone axis. High-resolution TEM image shown in Figure 1c with an inset obtained by reverse Fourier transform shows the perfect crystallinity of InSe nanosheets with a hexagonal lattice spacing of 3.4 Å. The chemical composition of the as-prepared sample is composed of indium (In) and Selenide (Se) with an atomic ratio of ~1:1 measured by X-ray energy-dispersive spectrum (EDS) (Figure S1, Supporting Information). Furthermore, the element distribution within the marked area inside InSe nanosheets was characterized by using the composition mapping operation, indicating that In and Se are homogeneously distributed over the product (Figure 1d displays). All above evidence confirmed that the synthesized InSe has a good and uniform β-type crystal structure. The InSe nanosheets are exfoliated from bulk InSe crystal and transferred to p++Si substrate that was coated with a 200 nm/50 nm PMMA/Al_2O_3 (or 50 nm Al_2O_3, 300 nm SiO_2 and 200 nm/300 nm PMMA/SiO_2). Photoluminescence emission spectra for different thickness InSe nanosheets were measured and shown in Figure S2-a. The bandgap exhibits a thickness-dependent characteristic as shown in Figure S2-b. The peak position shows a strong blue-shift of 285 meV to higher photon energies when decreasing the thickness from 50 nm to 6 nm, which is attributed to quantum confinement effect.[21] However, FETs fabricated using InSe with a thickness range of 30–40 nm show the highest carrier mobility (see more details in Figure 5). Therefore, the thickness in the range of 30–40 nm is chosen to fabricate our devices. After identifying the position of InSe nanosheets by optical microscopy, chromium/gold (Cr/Au) contacts are made on the nanosheets (more details see supplementary information). We choose Al_2O_3 and PMMA as the bilayer dielectric. The PMMA layer can be conveniently fabricated,[7] which was used for screening interfacial Coulomb impurities, such as hydroxyl groups, water and other chemical absorptions, resulting in improved performance. A 3D schematic of multilayer InSe back-gated FETs is shown in **Figure 2**a with a magnified area of InSe-PMMA/Al_2O_3 interface. The cross-sectional view of the device is shown Figure 2b, indicating a three-terminal configuration. A typical AFM image of the device is shown in Figure 2c, the width and length are 20 μm and 23 μm, respectively. The thickness of channel is close to 35 nm as identified by AFM.

We measured the electrical characteristics of multilayer InSe FETs by applying a drain-source voltage (V_{ds}) and gate voltage (V_g) in the configuration displayed in Figure 2b. **Figures 3**a, 3b show the transfer and output characteristics of multilayer InSe FETs based PMMA/Al_2O_3 bilayer dielectric and single Al_2O_3 dielectric under ambient environment. A typical n-type channel conductance and a saturation regime under high V_{ds} are observed. All multilayer InSe devices show these features regardless of their channel thickness or dielectric layer (also see Figure 3e-3f, S4 and S5). with repeated V_g sweeps applied on the same multilayer InSe FET while keeping V_{ds} a constant, no obvious variation was observed, indicating that FETs are highly stable. The I_{ds}–V_{ds} behaviors agree with that of conventional

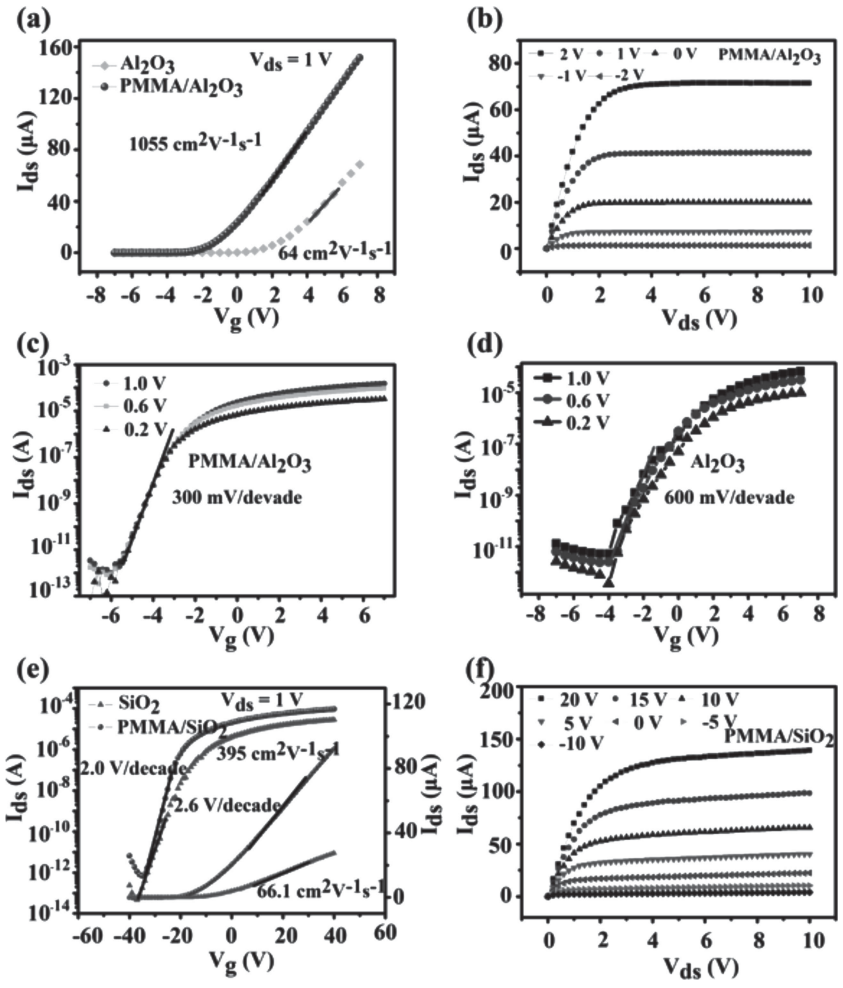

Figure 3. (a) Transfer characteristics of multilayer InSe transistor with polymer-assisted (200 nm/50 nm) PMMA/Al_2O_3 dielectric (red line, channel length is 20 μm, channel width is 25 μm and the thickness is 33 nm) and 50 nm Al_2O_3 dielectric (dark line, Channel length is 20 μm, channel width is 30 μm and thickness is 32 nm) at V_{ds} = 1 V. (b) The corresponding output characteristics of FETs with PMMA/Al_2O_3 dielectric. Measurements were performed under ambient environment. (c) Transfer characteristics for multilayer InSe transistor on PMMA/Al_2O_3 dielectric (200 nm/50 nm) measured at various V_{ds} (0.2, 0.6 and 1 V) on logarithmic scale. (d) Transfer characteristics for multilayer InSe transistor on Al_2O_3 dielectric (50 nm) measured at various V_{ds} (0.2, 0.6 and 1 V) on logarithmic scale. (e) Transfer characteristics of multilayer InSe transistor with polymer-assisted (200 nm/300 nm) PMMA/SiO_2 dielectric (red line, channel length is 20 μm, channel width is 13 μm and the thickness is 34 nm) and 300 nm SiO_2 dielectric (dark line, Channel length is 24 μm, channel width is 20 μm and thickness is 32 nm) at V_{ds} = 1 V on logarithmic (left axis) and linear scales (right axis). (f) The corresponding output characteristics of FETs based PMMA/SiO_2 bilayer dielectric.

long-channel NMOS transistor, showing a linear regime under low V_{ds} and a current saturation regime at high V_{ds}. This is an important feature for practical applications, including thin film transistors (TFTs) in OLED displays that work at the saturation current region. The saturation of drain current occurs in InSe FETs because of the conducting channel converting to "pinch-off" condition at high V_{ds}. The enlarged output curves in the small range of V_{ds} (–100 mV to 100 mV) are exhibited in Figure S3 (Supporting Information), the good linear characteristic indicates that our Au/Cr/InSe has ohmic contact and negligible contact resistance.

The field effect mobilities of multilayer InSe FETs can be extracted from the transfer curve (the date presented in Figure 3a) using the following equation:

$$\mu = \left[L/WC_i V_{ds} \right] \times \left[dI_{ds}/dV_g \right], \quad (1)$$

where L is the channel length of 23 μm, W is the channel width of 20 μm, and the C_i is the capacitance of 1.59×10^{-8} Fcm^{-2} and 1.59×10^{-7} Fcm^{-2} between the channel and back gate per unit area for PMMA/Al_2O_3 bilayer dielectrics and Al_2O_3 dielectrics, respectively. The field effect mobility of multilayer InSe FETs is calculated from two-contact configuration at room temperature to be 1055 $cm^2V^{-1}s^{-1}$ for PMMA/Al_2O_3 bilayer dielectric. Table S1 (Supporting Information) shows the comparison of key performance parameters of our device with various FETs (MoS_2,[2,4] WSe_2,[8] GaS[25] and silicon thin film.[24] The mobility of our transistors is comparable to that of strained 25 nm silicon thin-film, and is much higher than that of MoS_2, WSe_2 and GaS transistors, even higher than recently reported phosphorene device.[10] For example, the mobility of multilayer MoS_2 back-gated FETs on Al_2O_3 is ~100 $cm^2V^{-1}s^{-1}$,[4] and single-layer MoS_2 transistors with top-gated geometries ($HfO_2/MoS_2/SiO_2$) show a high mobility of 200 $cm^2V^{-1}s^{-1}$.[2] However, the fabrication process of strained silicon film is complex and not compatible with traditional microelectronics fabrication techniques. Our multilayer InSe FETs show comparable mobility with much easier fabrication process than strained silicon thin-film.

The subthreshold swing and current on/off ratio are also key parameters for the FETs. The subthreshold swing (*SS*) can be calculated using the following equation

$$SS = dV_g/d(\log I_{ds}) \quad (2)$$

and the current on/off ratio can be extracted by adopting ratio of maximum to minimum I_{ds} from transfer curves. As shown in Figure 3c, the calculated *SS* of multilayer InSe FETs based PMMA/Al_2O_3 bilayer dielectrics is 300 mV/decade, which is still higher than that of the theoretical value of 60 mV/decade. This may be attributed to the Coulomb scattering from the top surface of the channel.[2] For practical application in COMS-like digital circuits, the current on/off ratio value should exceed the value of 10^4–10^7.[26] In our case, the current on/off ratio is 1×10^8 for all applied gate voltages, and it is higher than that of multilayer MoS_2 back-gated FETs (10^6).[4]

It is notable that the performance of multilayer InSe FETs on bare Al_2O_3 dielectric layer is rapidly degraded. The mobility

is reduced to 64 $cm^2V^{-1}s^{-1}$ (Figure 3a green line), and the *SS* is increased to 600 mV/decade (Figure 3d). Because of the nature of layer materials, the surface of InSe nanosheets is lack of out of plane dangling bonds, while the relatively low mobility values and high subthreshold swings are due to interfacial Coulomb impurities or charge trap states from chemical groups, such as hydroxyl groups at Al_2O_3 surface. The existence of surface charge states at Al_2O_3 surface can significantly reduce the performance of back-gated FETs due to the scattering from these states, which have been demonstrated by graphene and MoS_2 FETs.[14,15] In our case, the performance improvement with PMMA/Al_2O_3 bilayer dielectric is mainly attributed to the reduction of interfacial Coulomb impurities because the PMMA is a defect-free polymer.

To further demonstrate that mobilities can be enhanced by our strategy, we also fabricated multilayer InSe FETs on bare SiO_2 and on PMMA/SiO_2 bilayer dielectric, respectively. The corresponding transfer and output curves of FETs based PMMA/SiO_2 bilayer dielectric and SiO_2 dielectric are shown in Figure 3e, 3f and Figure S5 (Supporting Information), respectively. The mobility and *SS* value of FETs on PMMA/SiO_2 bilayer dielectric are 395 $cm^2V^{-1}s^{-1}$ and 2.0 V/decade, and the mobility of FETs based SiO_2 is rapidly degraded to 66 $cm^2V^{-1}s^{-1}$ and *SS* value is increased to 2.6 V/decade. The performance of FETs based on PMMA-assisted SiO_2 is better than that of FETs based on SiO_2 dielectric. The results are similar to those from devices based on PMMA/Al_2O_3 dielectric and Al_2O_3 dielectric. All these results demonstrate that the performance of multilayer InSe back-gated FETs strongly depends on the properties of the dielectric layer used.

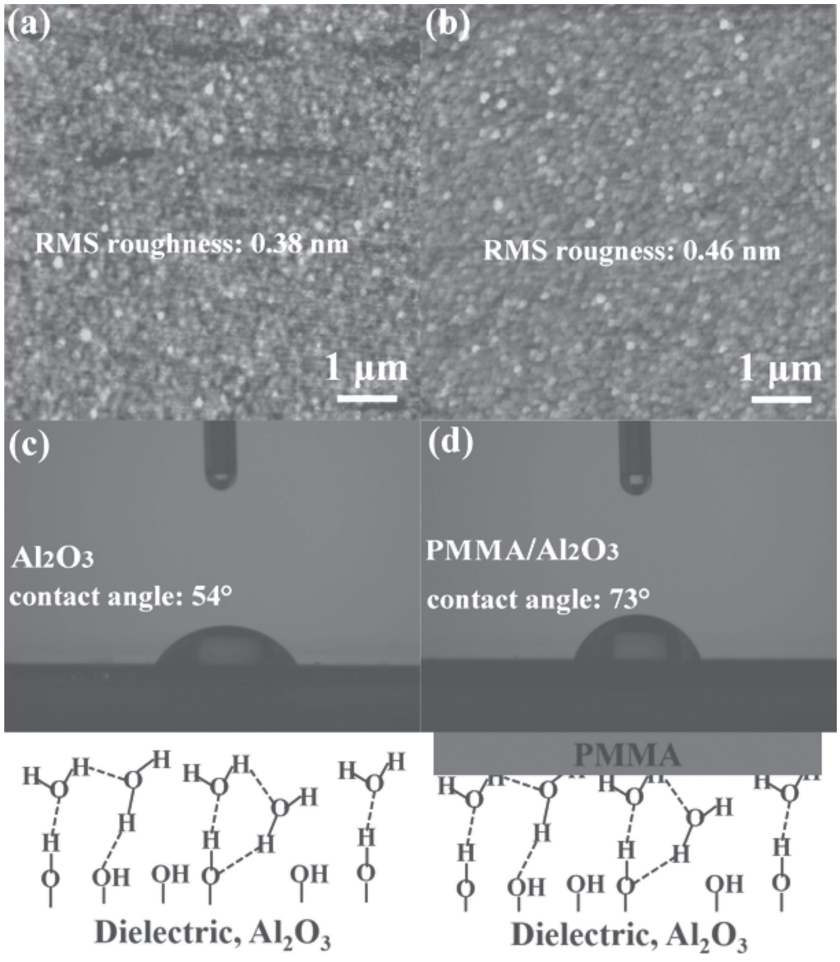

Figure 4. Tapping-mode AFM topographic images of dielectric (5 × 5 μm): (a) 50 nm Al_2O_3, (b) PMMA/Al_2O_3 (200/50 nm). The contact angle for (c) 50 nm Al_2O_3, (d) PMMA/Al_2O_3 (200/50 nm).

The coating of PMMA onto oxide dielectric is proven effective to improve the performance (mobilities, SS) of multilayer InSe FETs. PMMA has a lower dielectric constant than that of Al_2O_3 and SiO_2, so that the improvement in mobilities is not caused by increasing dielectric constant of the substrate. The roughness of both surfaces is measured by AFM to be ~0.38 nm for bare Al_2O_3 and 0.46 nm for PMMA/Al_2O_3 as shown in **Figure 4**a and 4b, which are almost the same. So the mobility increase is not caused by the roughness reduction of the dielectric surface after coating with PMMA. Contact angles for water on bare Al_2O_3 or SiO_2 substrate are 54° and 40° (Figure 4c, Figure S7 of Supporting Information), respectively, indicating that both oxidized surfaces are hydrophilic. When stored in ambient environment, the oxidized substrate surface (e.g., SiO_2 or Al_2O_3) has hydroxyl groups and is hydrated by a network of water molecules.[11–13] After coating with PMMA, the contact angles for water are changed to 73° for PMMA/Al_2O_3 and 71° for PMMA/SiO_2 (Figure 4d, Figure S7 of Supporting Information). Both substrates become less hydrophilic due to the screening of the hydroxyl groups on the surface. PMMA is a polar polymer consisting of polar molecular bone and groups, resulting in hydrophilic properties and small contact angle of water on PMMA film. To further understand the mobility improvement in light of the Mattiessen's rule,[27] the overall FET mobility μ is estimated using the following equation:

$$\mu = \left(1/\mu_{\text{int}} + \sum 1/\mu_{\text{i,ext}} \right)^{-1} \quad (3)$$

where μ_{int} is the mobility limited by InSe intrinsic scattering, such as structural defects and lognitudinal acoustic phonon scattering; μ_{ext} represents the mobility limited by extrinsic scattering from interfacial Coulomb impurities, surface roughness and surface polar phonon scattering. The μ_{int} values are similar for both InSe FETs with and without the PMMA coating layer since the same InSe was used in both devices. The FETs measurements show μ (PMMA) > μ (no PMMA), so that $(\mu_{CI}^{-1} + \mu_{SR}^{-1} + \mu_{SPP}^{-1})_{PMMA} < (\mu_{CI}^{-1} + \mu_{SR}^{-1} + \mu_{SPP}^{-1})_{no\ PMMA}$. Since $(\mu_{SR}^{-1})_{PMMA} \approx (\mu_{SR}^{-1})_{no\ PMMA}$ according to the surface roughness measurements in Figure 4 and Figure S7

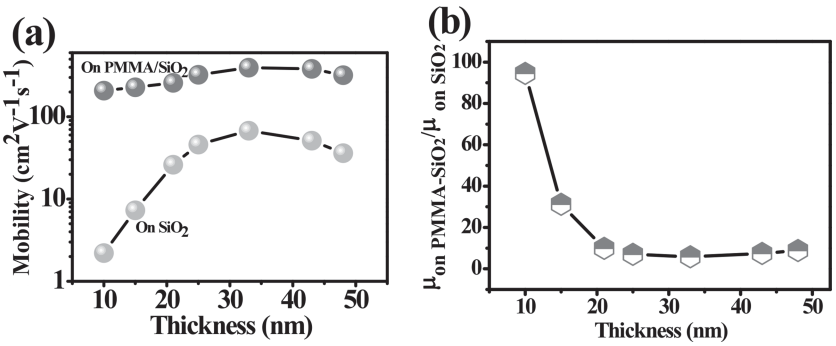

Figure 5. The impact of carrier scattering on the mobilies of different thickness InSe FETs: (a) The thickness-dependent mobilities of thin InSe FETs on SiO_2 or PMMA/SiO_2; (b) The ratio of the mobility on PMMA/SiO_2 dielectric over mobility on SiO_2 dielectric ($\mu_{on\ PMMA}/\mu_{on\ SiO2}$) as a function of InSe thickness.

(Supporting information), the mobility improvement is mainly due to the screening of hydroxyl groups, water or other chemical absorptions by the PMMA coating. All the above experiments and theoretical analysis proved that the improvement of carrier mobilities are mainly due to the suppression of carrier scattering caused by interfacial Coulomb impurities or SPP from hydroxyl groups, water or other chemical absorptions at the oxide surface.

Furthermore, we investigated the impact of carrier scattering at oxidized interface on the mobilities of different thickness InSe FETs. InSe FETs on SiO_2 and PMMA/SiO_2 are fabricated using an InSe layer with the thickness range of ~10–50 nm. The mobility rapidly increases as the InSe layer thickness changes from ~10 nm to 35 nm, then decreases with further channel thickness increasing (up to 50 nm). A peak mobility value occurs at 35 nm regardless of what dielectric was used (**Figure 5**a). The carrier scattering exhibits a thickness-dependent impact on the mobilities of the multilayer InSe FETs (Figure 5a). The mobilities for ~10 nm InSe FETs vary from 2.2 $cm^2V^{-1}s^{-1}$ on SiO_2 to 208 $cm^2V^{-1}s^{-1}$ on PMMA/SiO_2, showing a 94.5 time increase, while the mobilities for ~35 nm InSe devices increase from 67.6 $cm^2V^{-1}s^{-1}$ on SiO_2 to 395 $cm^2V^{-1}s^{-1}$ on PMMA/SiO_2, which just show a 5.8 times enhancement. The ratio of the mobility on PMMA/SiO_2 dielectric over mobility on SiO_2 dielectric ($\mu_{on\ PMMA}/\mu_{on\ SiO2}$) is used to quantify the impact of carrier scattering on different thickness InSe layers (Figure 5b). We found that the $\mu_{on\ PMMA}/\mu_{on\ SiO2}$ ratio varies from 94.5 for 10 nm-thick InSe to 8.8 for 50 nm-thick InSe. This indicates that Coulomb impurities (CIs) have more significant impact on thinner InSe layers, because the interaction distance between CIs and carriers inside thin InSe layer is much shortened, which enhanced carrier scatterings, leading to rapid degradation of carrier mobility. The observed thickness dependent mobilities of InSe nanosheets FETs (Figure 5a) can be well understood by a resistor network model as shown in Figure S6-c, which has been widely used to account for the thickness related transport properties of FETs based on multilayer graphene,[28] MoS_2[6] and black phosphorus.[29] Briefly, the metal source/drain contacts are connected only directly to the top InSe layer, while access to lower layers involves additional interlayer resistors (R_i is the interlayer conductivity). Back gating impacts the lowest layer most, and charge screening results in the decrease of charges on the top InSe layer. The absence of sufficient gate field screening effect and more intense carrier scatterings leads to a lower mobility in few layer thickness FETs, which explains the sharp decrease in mobility for InSe layer thickness below 35 nm. With the layer thickness increasing, the interlayer resistance will dominate the mobility. The current is injected form electrical contacts on the top, the finite interlayer resistance and edge resistance will force the current to flow through all layers, which are not impacted by gate field screening effect. Such effect will degrade the mobility of InSe thicker than 35 nm. Hence, taking the competing factors into consideration, there will be a peak mobility value at a finite layer thickness.

In conclusion, we have discovered that the carrier scattering from the chemical impurities (hydoxy groups and absorbed water molecules) at oxidized dielectric interface plays a significant role in determining the carrier mobilities of thin layer semiconductor FETs using multilayer InSe. The mobilities of back-gated multilayer InSe FETs can be largely enhanced through the suppression of CIs or SPP scattering at an oxidized dielectric interface. All InSe multilayer devices exhibit a high current on/off ratio of ~10^8 and robust current saturation over a large source-drain voltage window. The multilayer InSe back-gated FETs show a high room temperature electron mobility up to 1055 $cm^2V^{-1}s^{-1}$ at low operating gate voltage (V_g = 1 V) using PMMA/Al_2O_3 dielectric, which is comparable to strain silicon thin film and higher than that of MoS_2. Furthermore, we have found that Coulomb impurities (CIs) at oxide dielectric exhibit significant impact on thinner InSe layers, the ratio of the mobility on PMMA/SiO_2 dielectric over mobility on SiO_2 dielectric ($\mu_{on\ PMMA}/\mu_{on\ SiO2}$) varies from 94.5 for 10 nm-thick InSe to 8.8 for 50 nm-thick InSe. Our results provide a useful guideline for fabricating high performance FETs based on thin layered semiconductors.

Experimental Section

Thin layer InSe crystals were prepared by chemical vapor deposition (CVD) as described in Supporting Information. The layer thickness was determined by atomic force microscopy (AFM, Nanoscope IIIa Vecco). The structure and composition of multilayer InSe were identified by X-ray diffraction (XRD, DIFFRACTOMETER-6000 with Cu Ka radiation (λ = 0.1542 nm)) and transmission electron microscopy (TEM, Tacnai-G2 F30, accelerating voltage of 300 kV) attached with an energy-dispersion X-ray spectroscopy (EDS). Photoluminescence spectrums were measured by Raman microscopy (LabRAM XploRA, incident power of 1 mW, pumping wavelength of 532 nm). Electrical characterizations of transistors based on multilayer InSe were performed by using a semiconductor characterization system (Keithley 4200 SCS) with a Lakeshore probe station.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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