REV	Description	Date
V1.0	First Release	2016-7-12

AX7010/AX7020 Schematics

黑金ZYNQ硬件平台

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Page02	Block Diagram
Page03	Zynq-7000 JTAG & Bank0
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Page09	GPHY
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ALINX

Title: Zynq-7000 Cover Page

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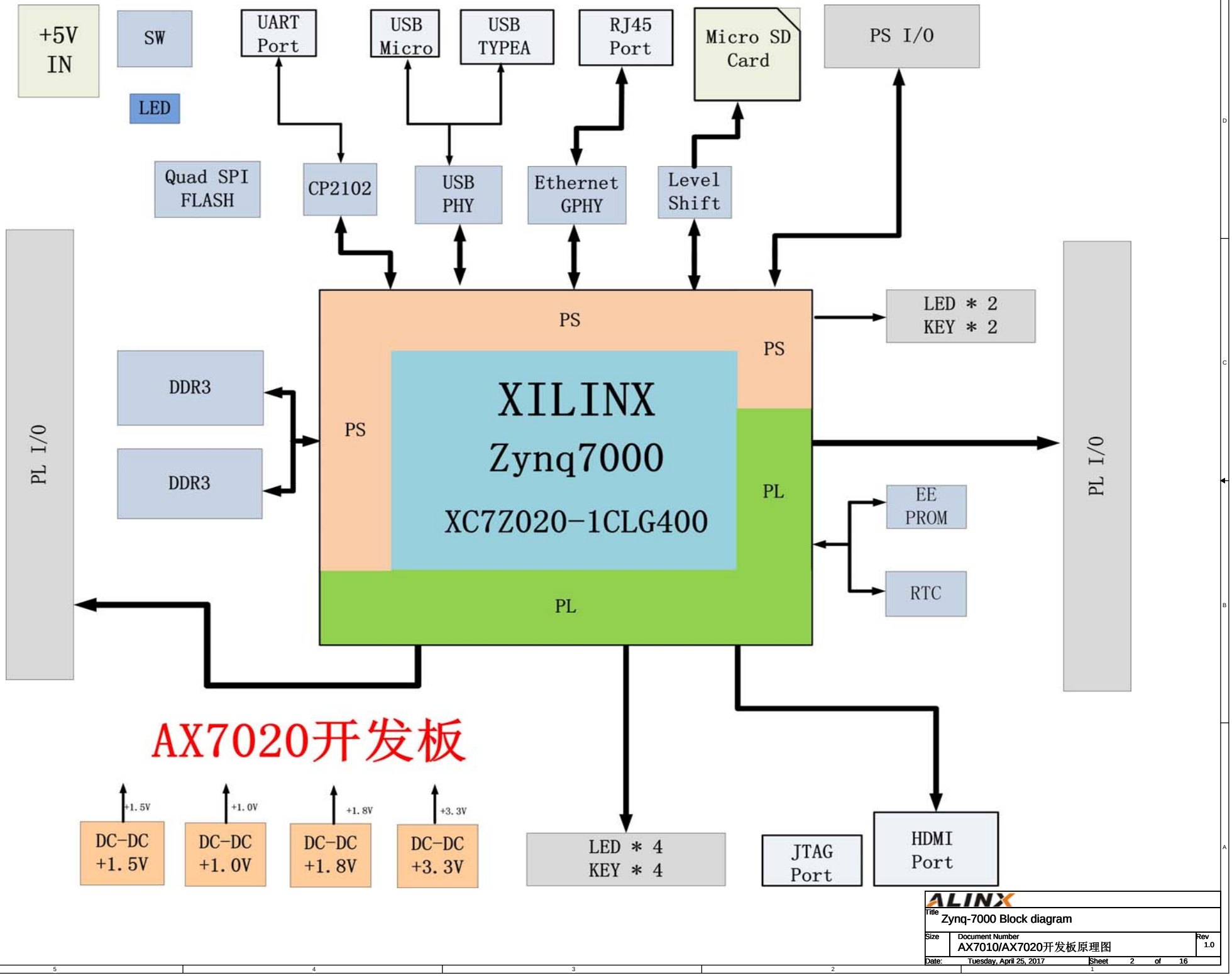

ALINX

Title	Zynq-7000 Block diagram
Size	
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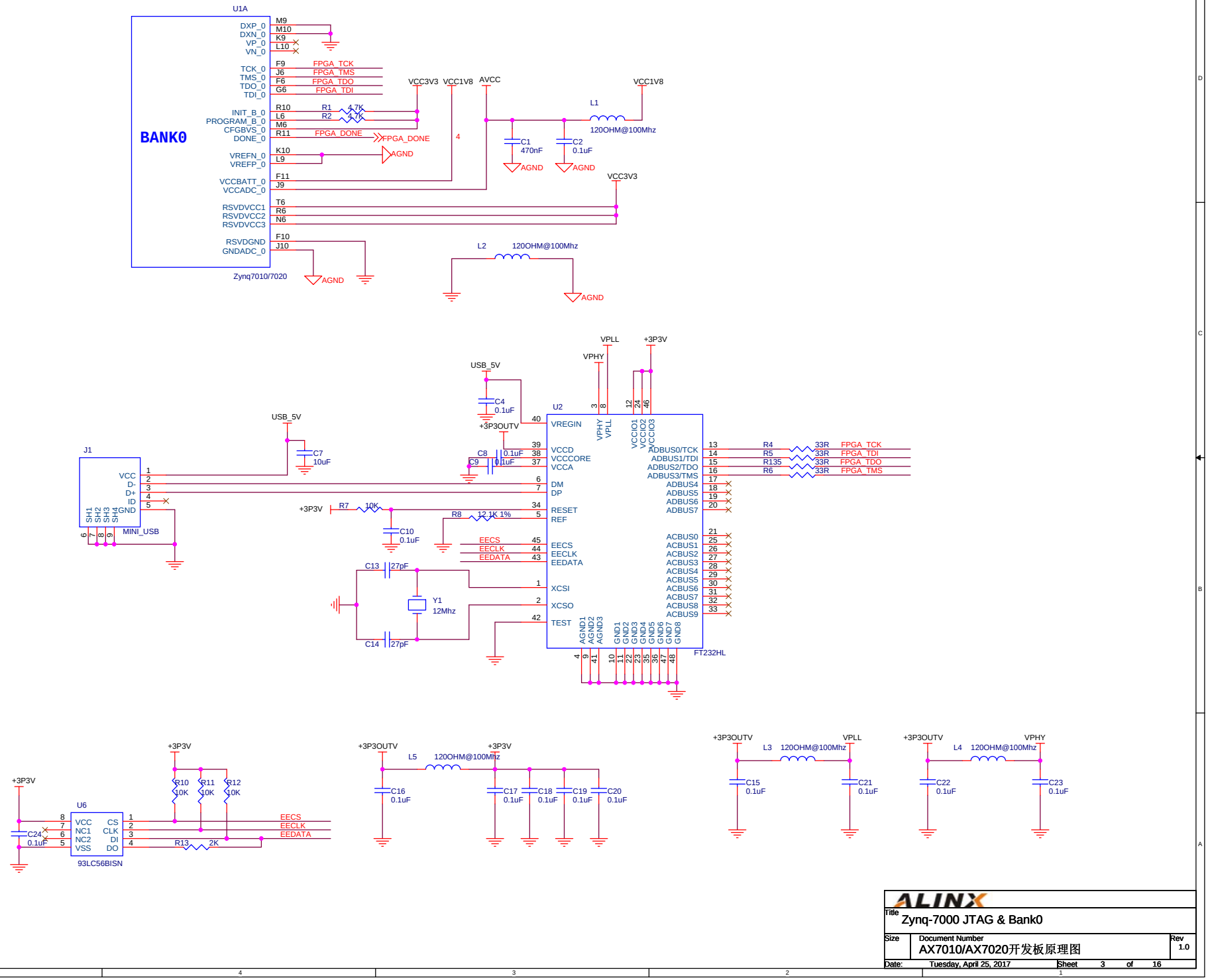

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Title	Zynq-7000 JTAG & Bank0
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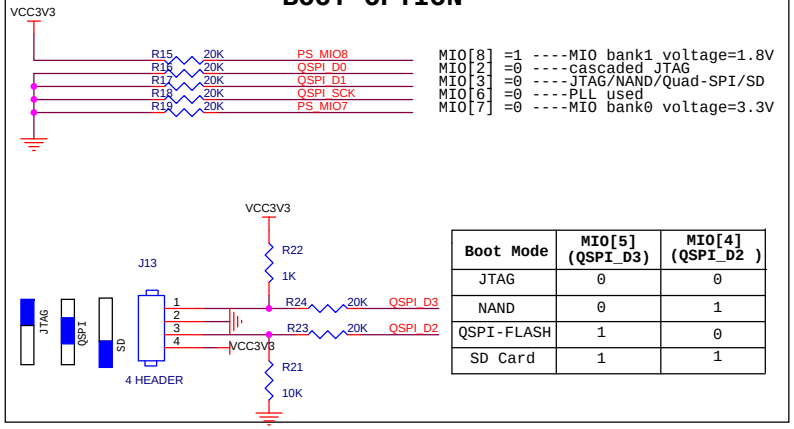
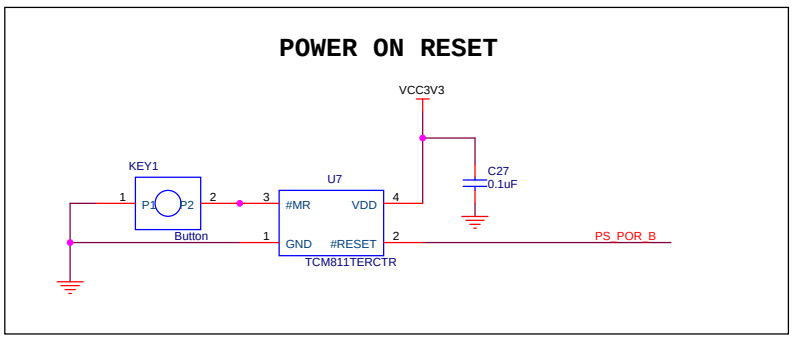
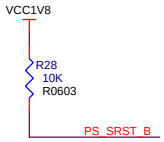
BOOT OPTION

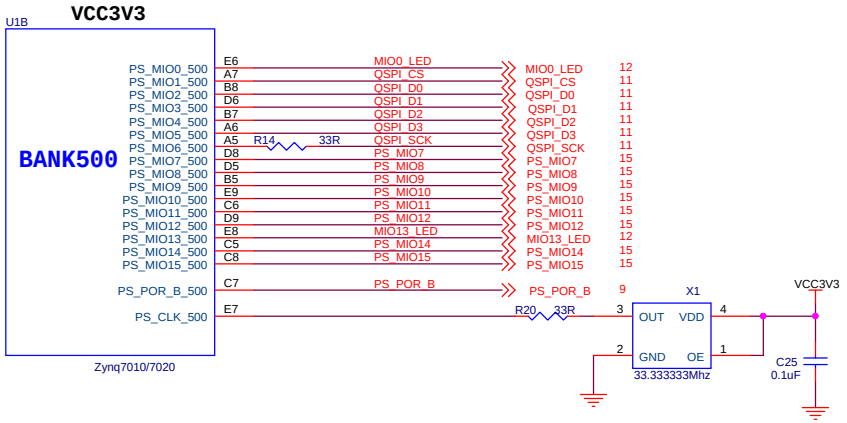


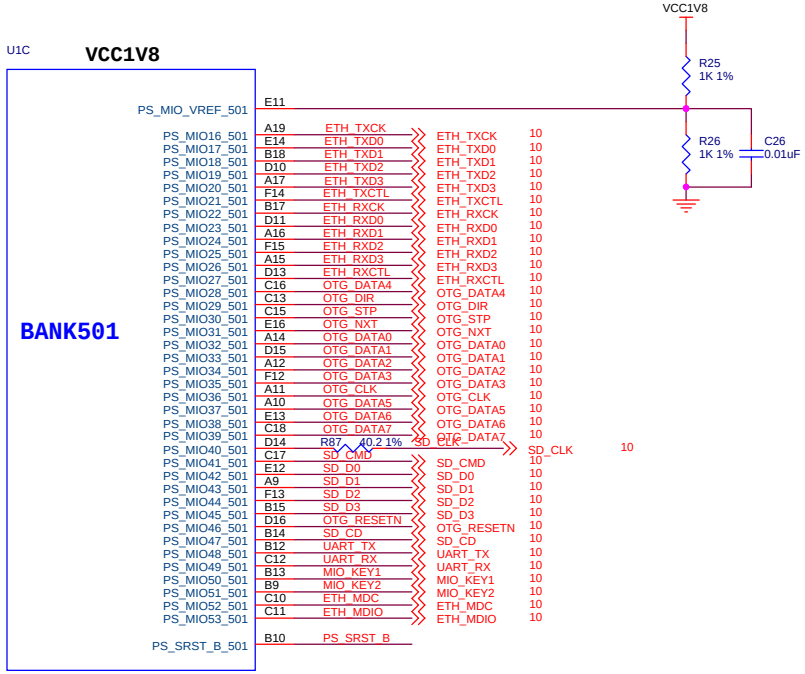
Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI-FLASH	1	0
SD Card	1	1

POWER ON RESET









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Title	Zynq-7000 PS MIO	
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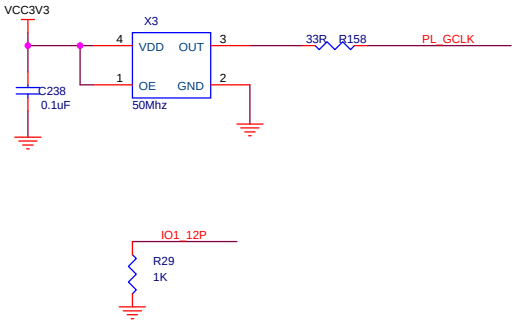

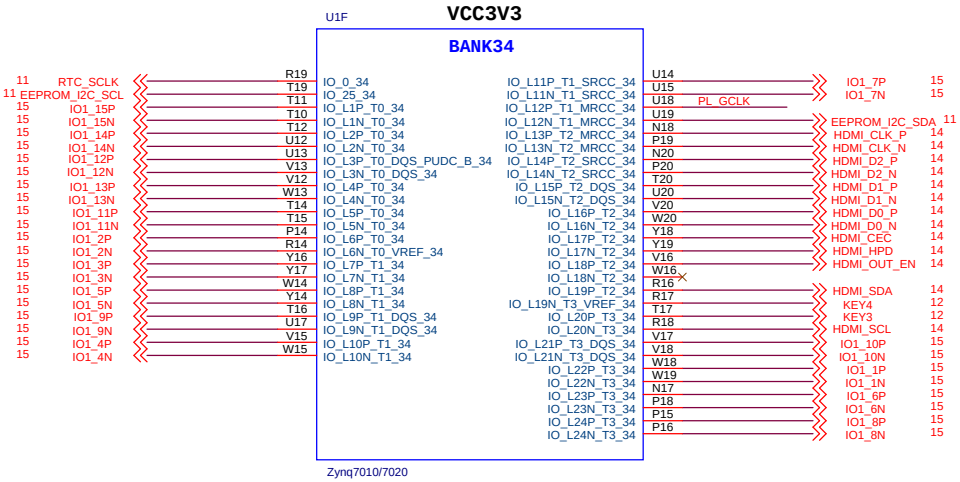

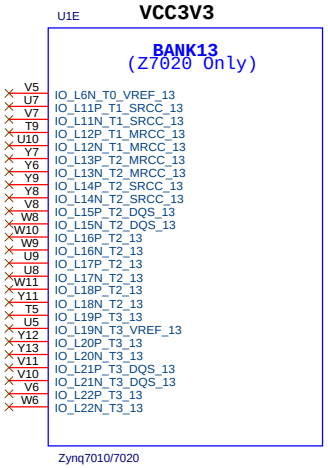

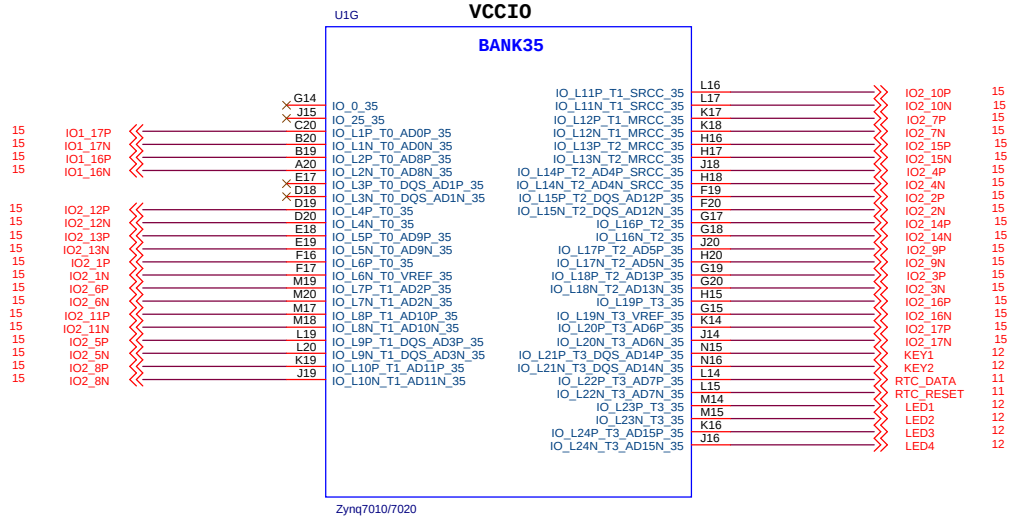

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Title: Zynq-7000 Bank13 & 34 & 35

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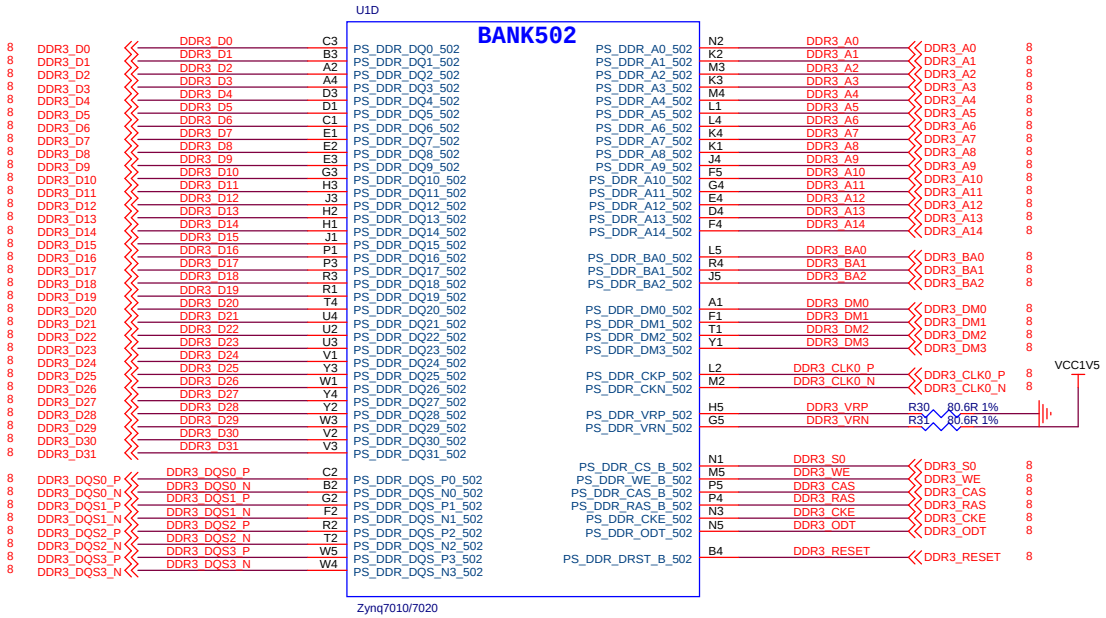

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Size	
Document Number	AX7010/AX7020开发板原理图
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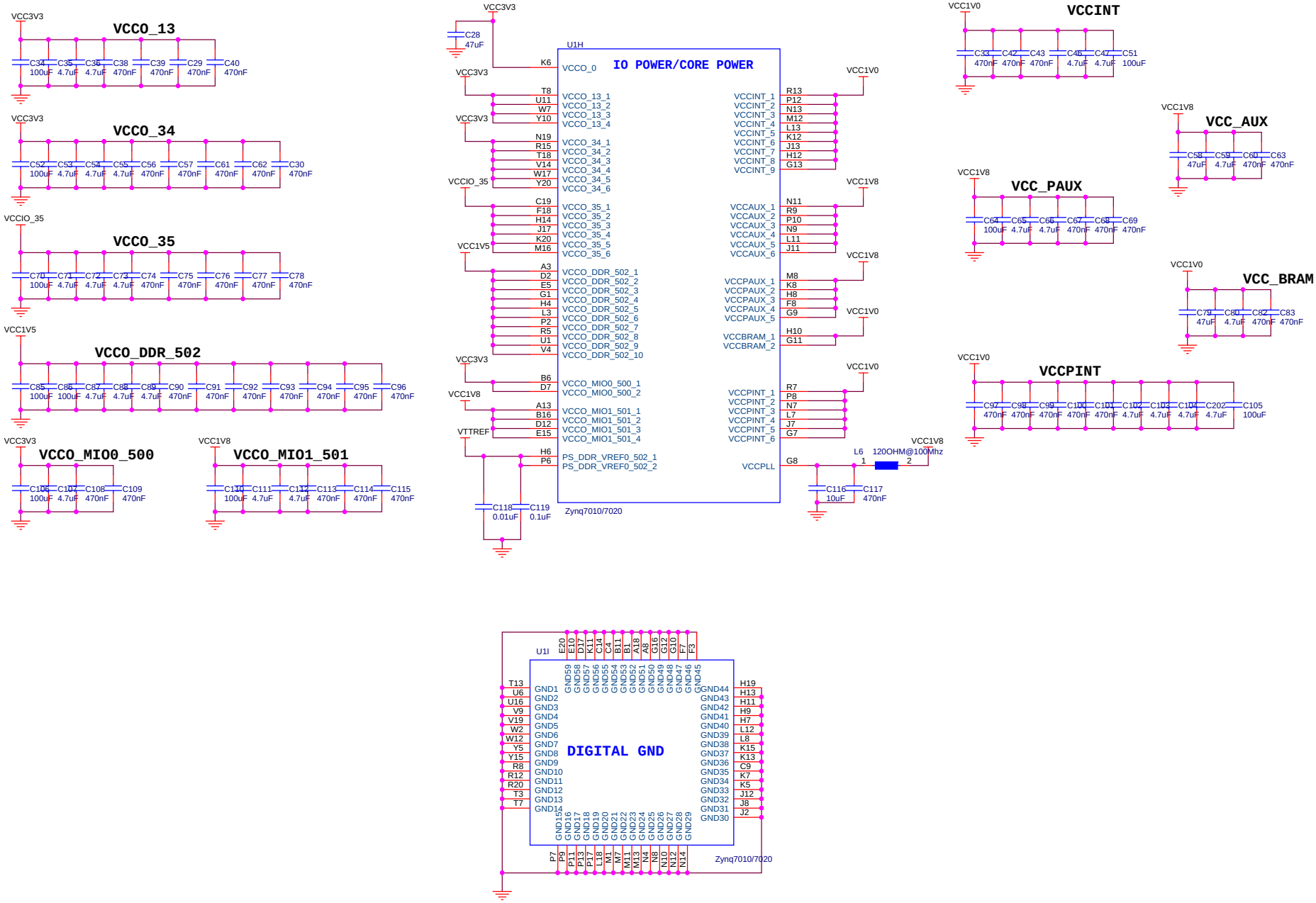

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Title: Zynq-7000 Cover Page

Size	Document Number	Rev
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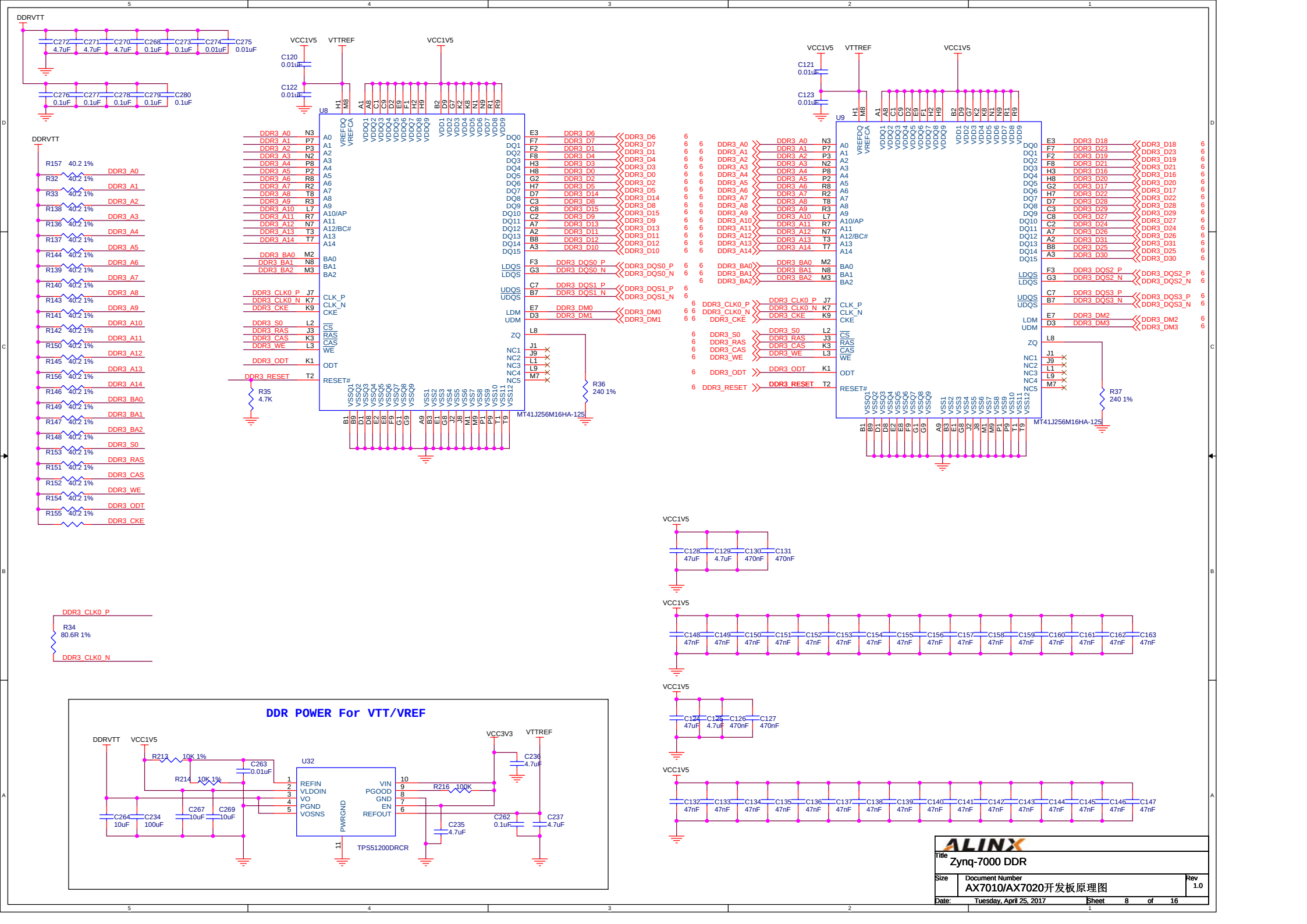
DDRVTT
C272 4.7uF
C271 4.7uF
C270 4.7uF
C268 0.1uF
C273 0.1uF
C274 0.01uF
C275 0.01uF
C276 0.1uF
C277 0.1uF
C278 0.1uF
C279 0.1uF
C280 0.1uF
VCC1V5
VTTREF
C120 0.01uF
C122 0.01uF
U8
MT41J256M16HA-125
R35 4.7K
R36 240 1%
C121 0.01uF
C123 0.01uF
U9
R37 240 1%
R157 40.2 1%
R32 40.2 1%
R33 40.2 1%
R138 40.2 1%
R136 40.2 1%
R137 40.2 1%
R144 40.2 1%
R139 40.2 1%
R140 40.2 1%
R143 40.2 1%
R141 40.2 1%
R142 40.2 1%
R150 40.2 1%
R145 40.2 1%
R156 40.2 1%
R146 40.2 1%
R149 40.2 1%
R147 40.2 1%
R148 40.2 1%
R153 40.2 1%
R151 40.2 1%
R152 40.2 1%
R154 40.2 1%
R155 40.2 1%
DDR3_A0
DDR3_A1
DDR3_A2
DDR3_A3
DDR3_A4
DDR3_A5
DDR3_A6
DDR3_A7
DDR3_A8
DDR3_A9
DDR3_A10
DDR3_A11
DDR3_A12
DDR3_A13
DDR3_A14
DDR3_BA0
DDR3_BA1
DDR3_BA2
DDR3_CLK0_P
DDR3_CLK0_N
DDR3_CKE
DDR3_S0
DDR3_RAS
DDR3_CAS
DDR3_WE
DDR3_ODT
DDR3_RESET
DDR3_CLK0_P
R34 80.6R 1%
DDR3_CLK0_N
C128 47uF
C129 4.7uF
C130 470nF
C131 470nF
C148 47nF
C149 47nF
C150 47nF
C151 47nF
C152 47nF
C153 47nF
C154 47nF
C155 47nF
C156 47nF
C157 47nF
C158 47nF
C159 47nF
C160 47nF
C161 47nF
C162 47nF
C163 47nF
C124 47uF
C125 4.7uF
C126 470nF
C127 470nF
C132 47nF
C133 47nF
C134 47nF
C135 47nF
C136 47nF
C137 47nF
C138 47nF
C139 47nF
C140 47nF
C141 47nF
C142 47nF
C143 47nF
C144 47nF
C145 47nF
C146 47nF
C147 47nF
DDR POWER For VTT/VREF
VCC3V3
VTTREF
R213 10K 1%
R214 10K 1%
C263 0.01uF
U32
TPS51200DRCR
R216 100K
C236 4.7uF
C235 4.7uF
C262 0.1uF
C237 4.7uF
C264 10uF
C234 100uF
C267 10uF
C269 10uF
ALINX
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Zynq-7000 DDR
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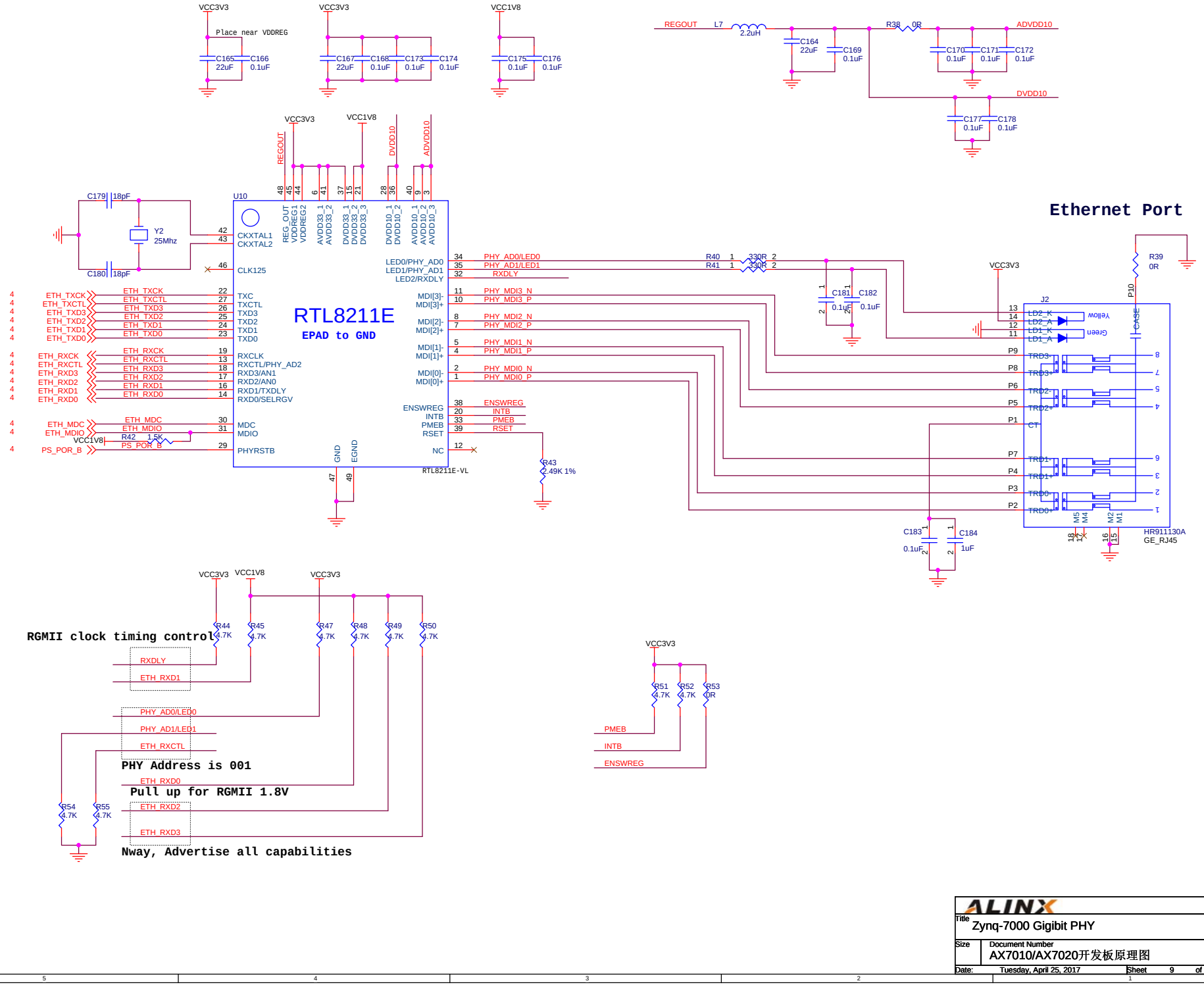
Ethernet Port
RTL8211E
EPAD to GND
RTL8211E-VL
RGMII clock timing control
PHY Address is 001
Pull up for RGMII 1.8V
Nway, Advertise all capabilities
HR911130A
GE_RJ45
Title
Zynq-7000 Gigibit PHY
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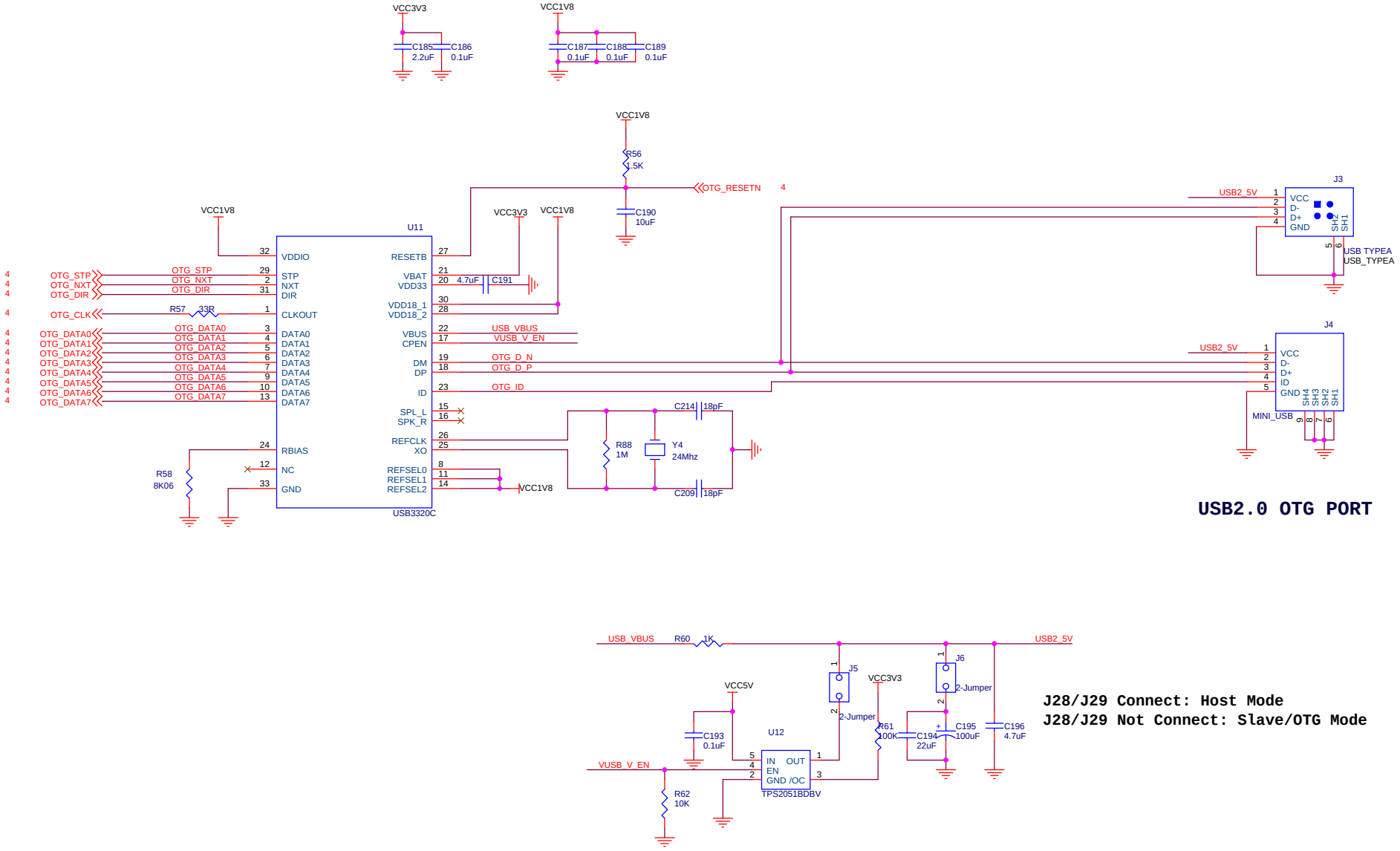

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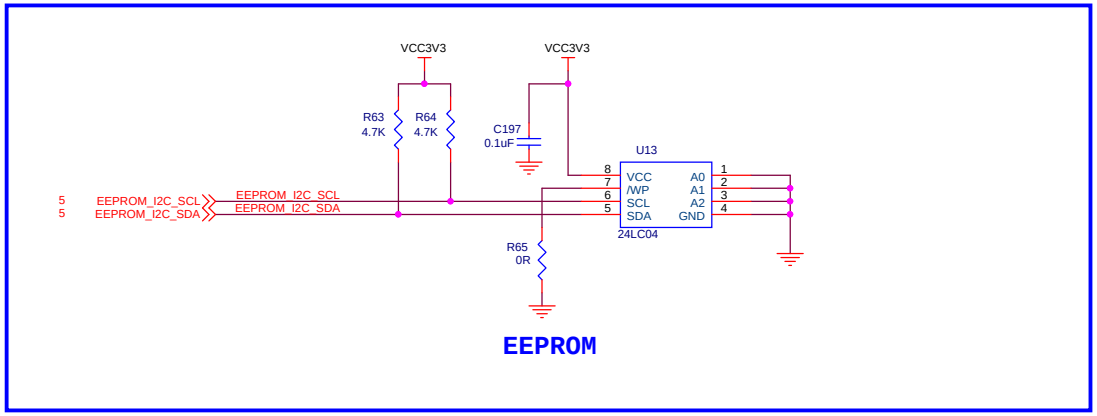

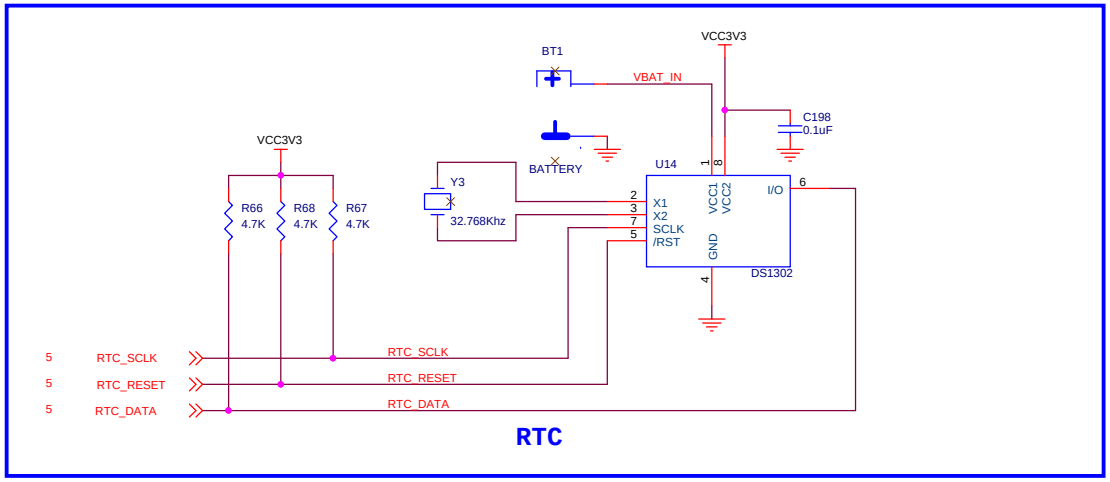

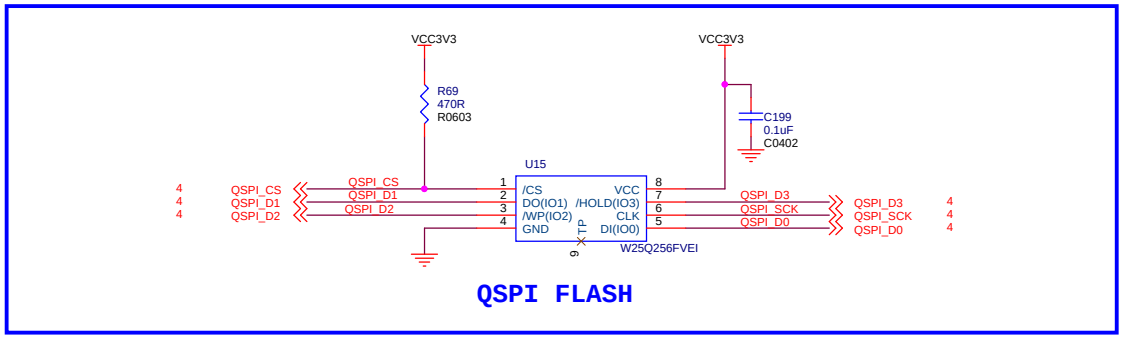

Title	Zynq-7000 QSPI & RTC & EEPROM	
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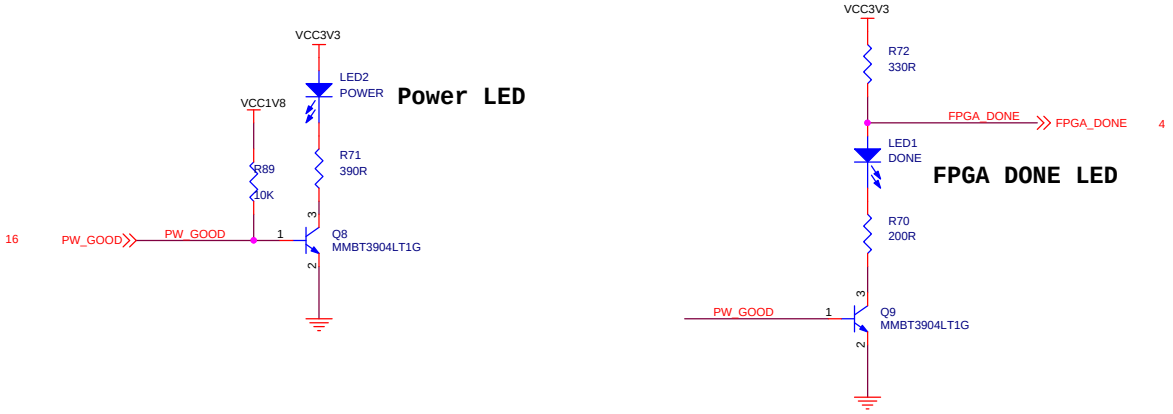

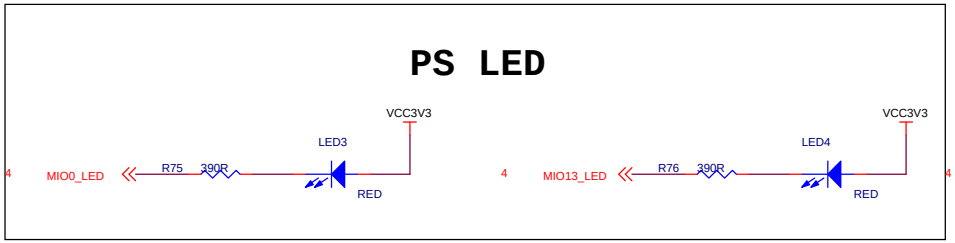

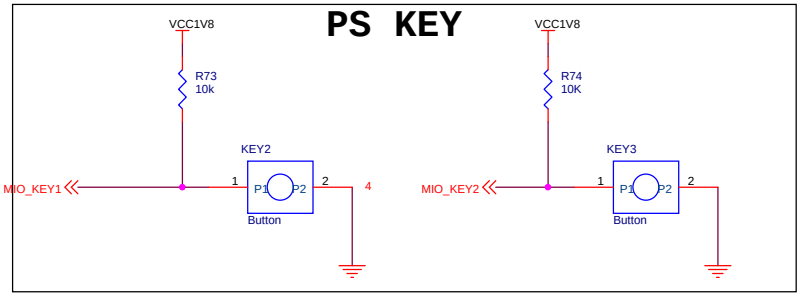

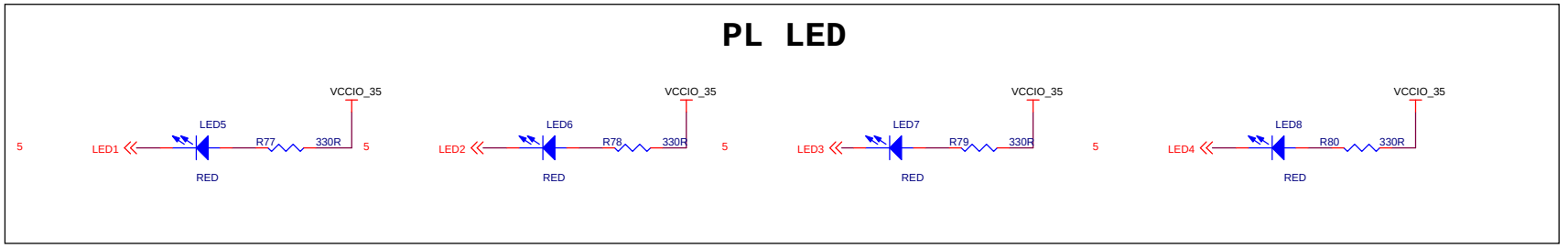

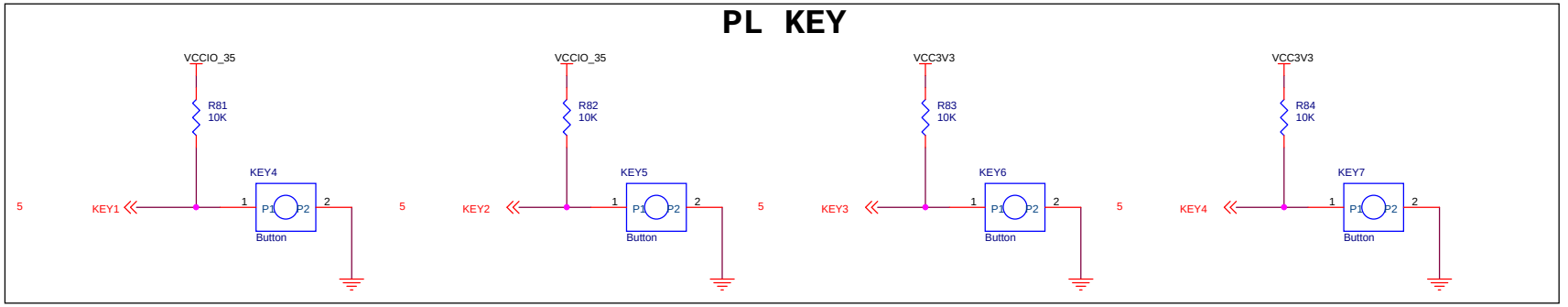

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Title	Zynq-7000 LED & KEY	
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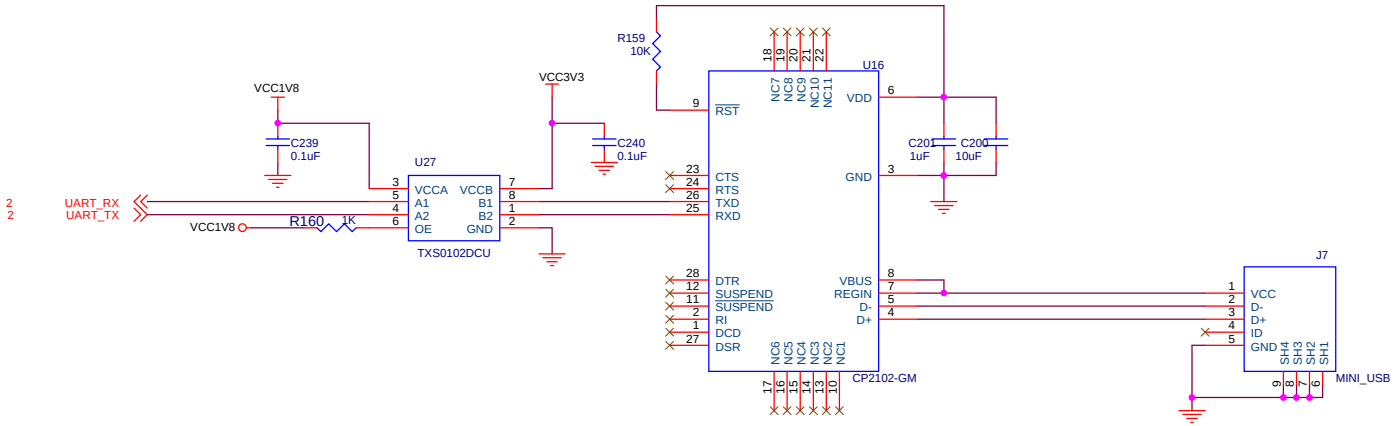
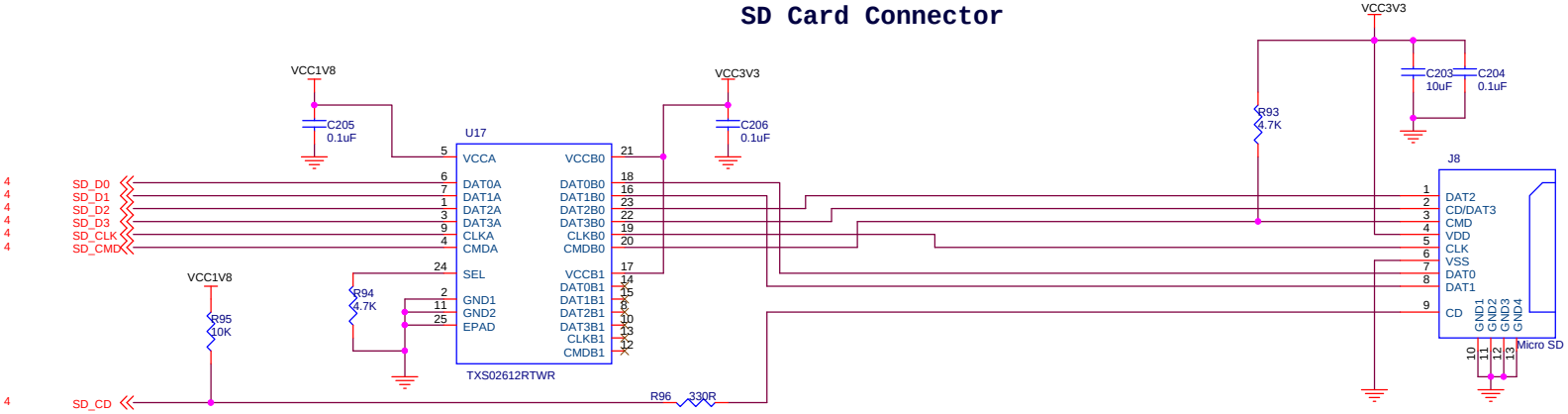
USB Uart



SD Card Connector



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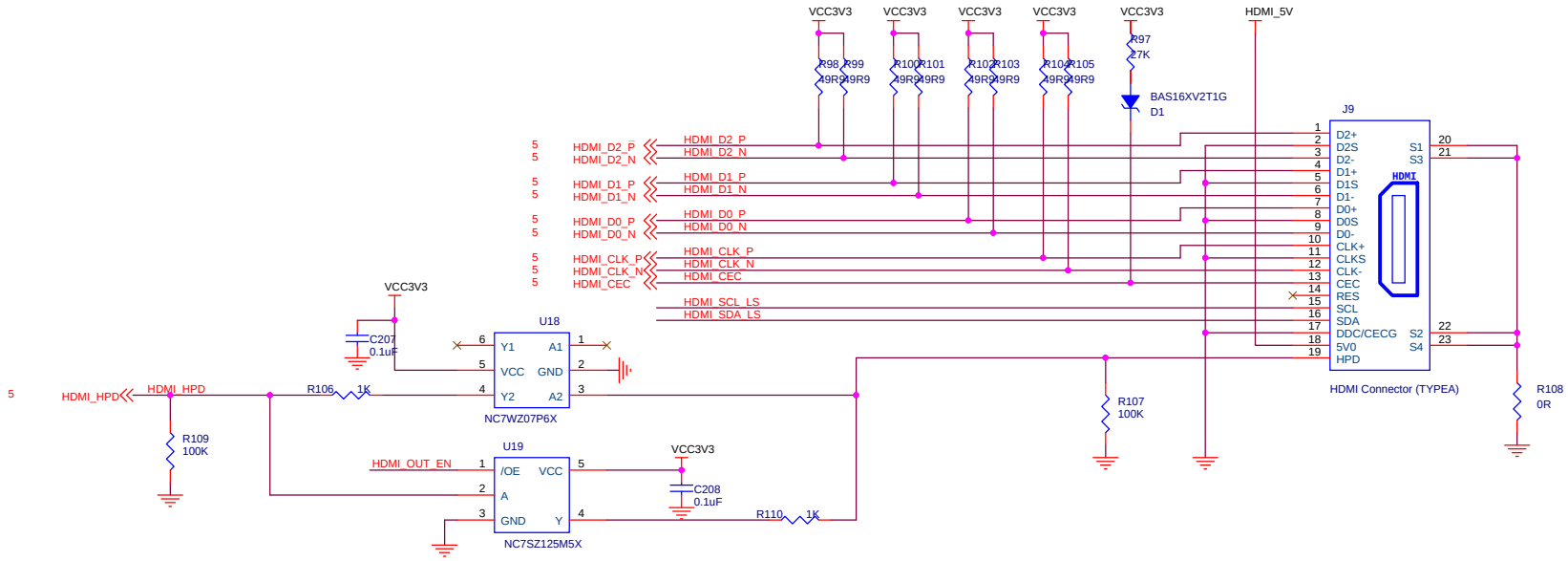

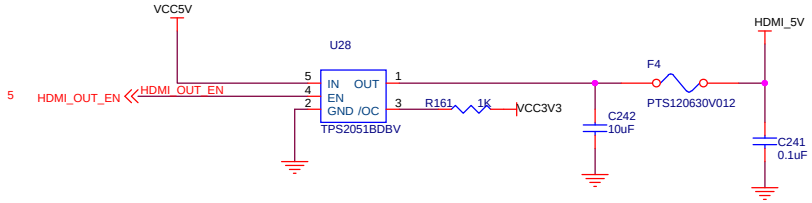

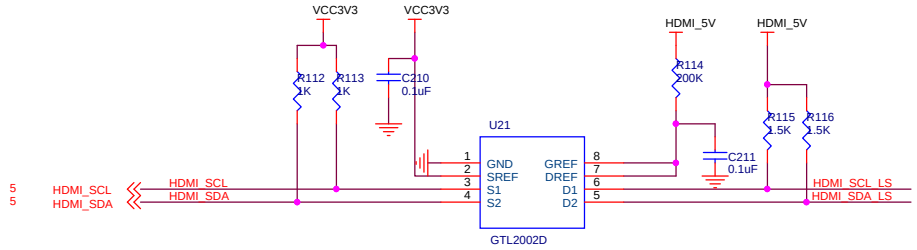

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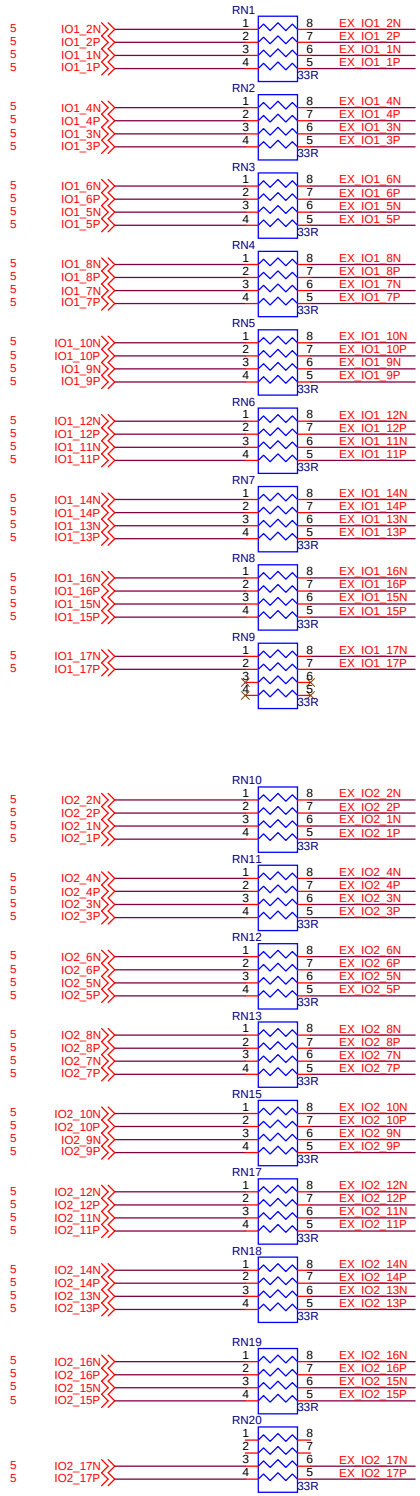
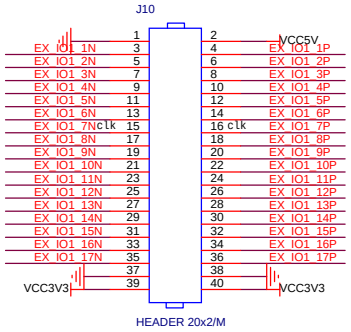
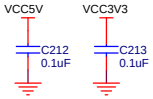
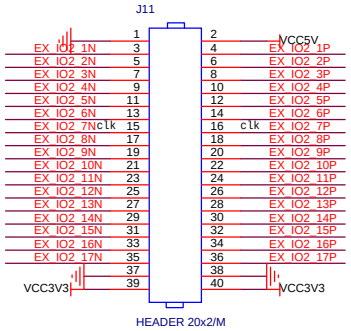
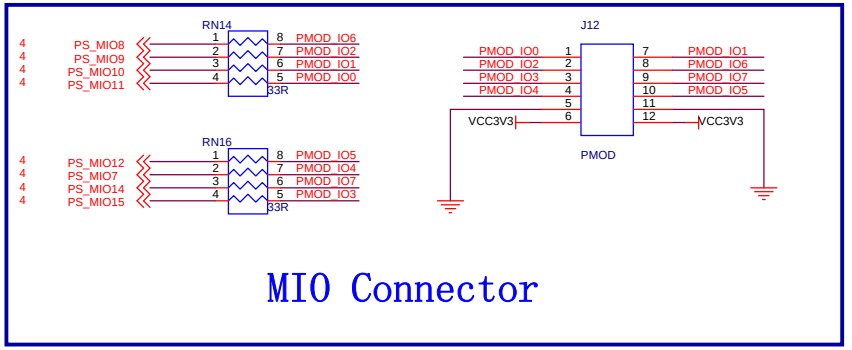


FPGA 40 PIN External IO









Title	Zynq-7000 LED & KEY & IO	
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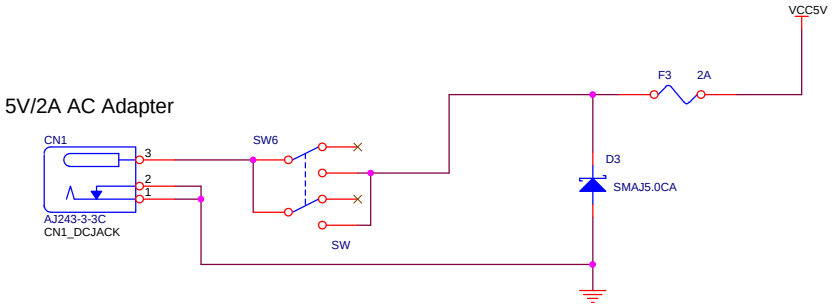
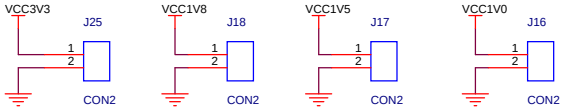
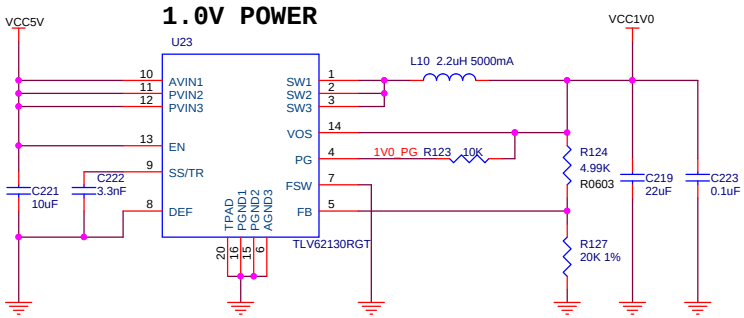
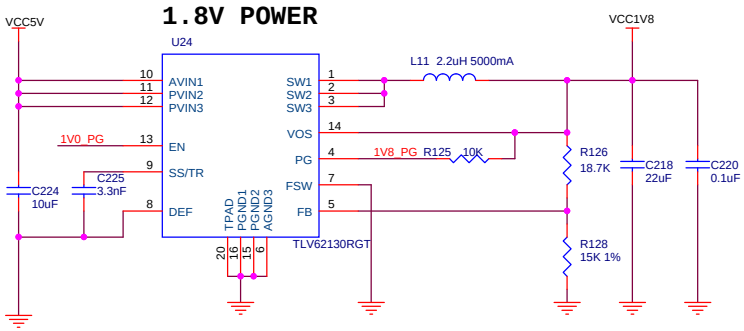
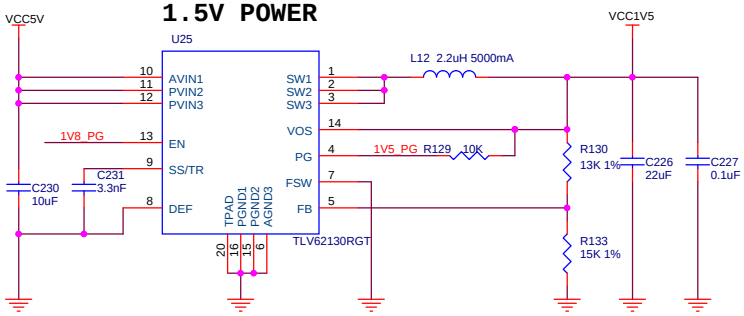
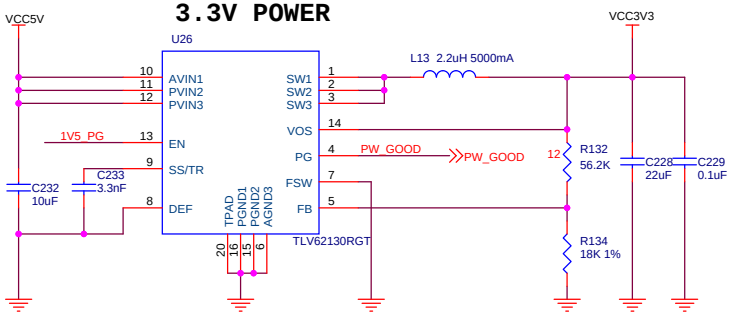






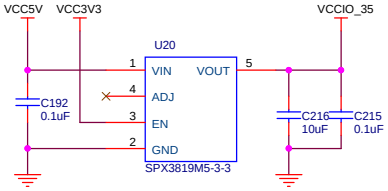






Power On Sequnce:

1.0V -> 1.8V -> 1.5 V -> 3.3V -> VCCIO



ALINX

Title	Power	
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