并行计算机体系结构
——cache 一致性实验报告

目录

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1. 实验要求

实现一种基于 WB 策略的一致性维护的 Cache 模拟器，该模拟器仅考虑 4 核的 CPU，且每个核只有一级 Cache，Cache 行长度为 64 字节，观察 CPU 读、写数据后各个核上 Cache 中数据状态的变化情况。
（1）输入参数为 trace0.txt、trace1.txt、trace2.txt 和 trace3.txt，分别表示核 0、核 1、核 2 和核 3 的数据访问文件。trace 文件为 ASCII 文本格式，每行代表一个数据的读、写操作，trace 文件可以包含很多行，可以根据需要自行设定多种场景进行全面测试，并且至少需要覆盖课堂上讲授的 3 种状态变化。
trace 文件格式举例，文件 trace0.txt
---
0 00007c71
0 00007951
1 00007b51

说明：该 trace 文件表示核 0：读（0）00007c71（地址）的数据，读（0）00007951（地址）的数据，写（1）00007b51（地址）的数据。
（2）输出为 4 个核读、写操作（只考虑课堂讲授的 4 种操作）后 Cache 中数据的状态（只考虑课堂讲授的 3 种状态）
作业提交：源代码、trace 文件、实验报告。报告中至少包含以下内容：
(a) 模拟器设计思想；
(b) 测试数据以及详细的测试报告；进行测试时，各个核至少要包括以下的测试场景：

	0	1	2	3
(i)	S	S	S	S
(ii)	S	S	I	I
(iii)	M	I	I	I
(iv)	I	S	S	S
(v)	I	I	M	I

2. 完成度和功能介绍:

本程序是 cache 一致性模拟器, 实现了基本的 cache 一致性模拟功能, 同时还有自行发挥的部分。

本程序使用**写回策略**，采用**作废法**，并使用**目录表法**保存一致性所需信息，cache 映射方式为**全相联映射**，替换策略为**随机替换**。

四个核心读取指令文件后采用轮询策略依次获取访问互联网络的权限，核 0 -> 核 1 -> 核 2 -> 核 3 -> 核 0 ……，依次执行各个核心的读写指令。

每个核心有两个 cacheline（采用参数定义，可更改），每个 cacheline 有 64Byte 容量，memory 地址从 0x00 到 0x575（512+63），memory 容量为 9*64 Byte（memory 容量参数定义，可更改）。

每个核心以及 memory 的状态都可实现 MSI 三状态的正确转换。有空闲 cacheline 时如发生读写，

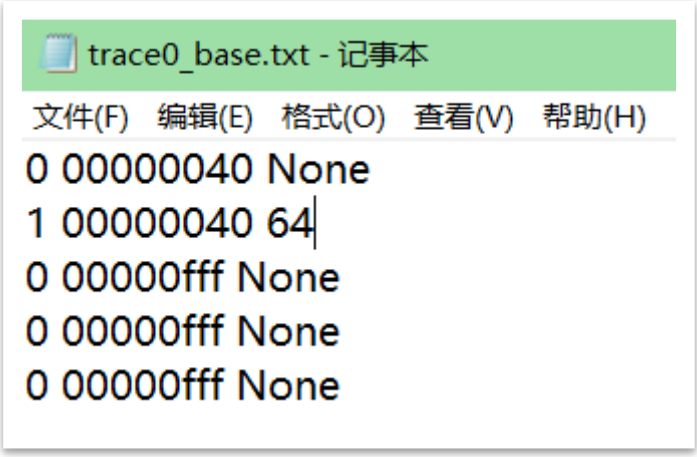
产生 cache 未命中，随后直接读写并处理一致性，cacheline 两行都写满时，再次对不同地址进行读写，则会产生 cache 未命中，会采用**随机策略替换**一条 cacheline，此时发生**写回操作**并释放对应 cacheline 空间，之后才会读取或者写入新数据到此 cacaheline。

3. 总体实现思路讲解：

a) 输入 trace 文件格式：

输入指令分为**读、写、无操作**三种类型，需按照如下格式设置：

读写标志位+读写地址+（数据），以空格分开



读指令：0+address+None 其中 None 无意义仅为格式统一，方便程序读取。

写指令：1+address+data 其中 data 为要写入 address 地址处的数据。

无操作指令：0/1+0xfff+“xxx”当地址为 DO_Nothing = 4096-1（0xfff）时候，认为此指令为无操作，相当于 pass，增加此指令的目的是方便测试时候控制每个核心的读写操作，使得部分核心在某一时刻无操作，以体现其他核心操作的结果（指令读取到程序内部后还会设置一个 block_addr，该地址以 64Byte 为块，方便存入 cache）。

b) Cache 和 memory 数据组成介绍：

```
11    cacheline_num = 2    #each core has 2 cachelines
12    cacheline_size = 64
13    memory_line_num = 9 #9 memory lines
14    DO_Nothing = 4096-1 # addr = 4095(0xfff) means do nothing
15    NOT_Used = 4096-1    # 4095  means cacheline is not used
```

Cache 行大小为 64Byte，每个核心有两个 cacheline（行数可以通过 cacheline_num 定义更改），cacheline 由 address、state、data 组成，如下图所示。当 cacheline 为 M/S 状态时，地址和数据有效并为相应数值，cacheline 为 I 状态时为无效，此时地址 address 需要为 NOT_Used = 4096-1（0xfff），且不关注数据值（**作废法**，作废时候更改 state 和 address，不更改 data）。

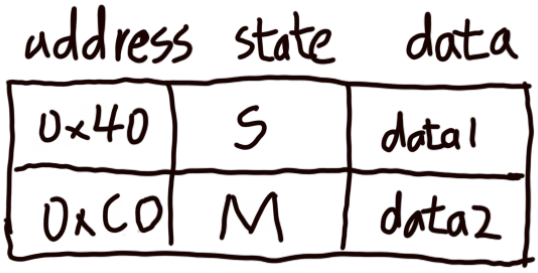


图 1：cache 示例，两行 cacheline

Memory 按照 64Byte 编为块地址，以方便显示，即位宽为 64 字节，长度为 9 块（可通过 memory_line_num 指定，但不能超过 0xfff，此地址被认为无操作）。为方便数据显示，本实验将对某个字节地址的读写，默认为对某个 64Byte 块的读写，地址上也采取了除 64 取整数的方式获取块地址（本身也是如此，部分字节数据改变，整个 64Byte 块数据也发生改变）。Memory 每块由 address、0、1、2、3 核 cache 标志位、memory 状态位、块数据组成，如下图所示。

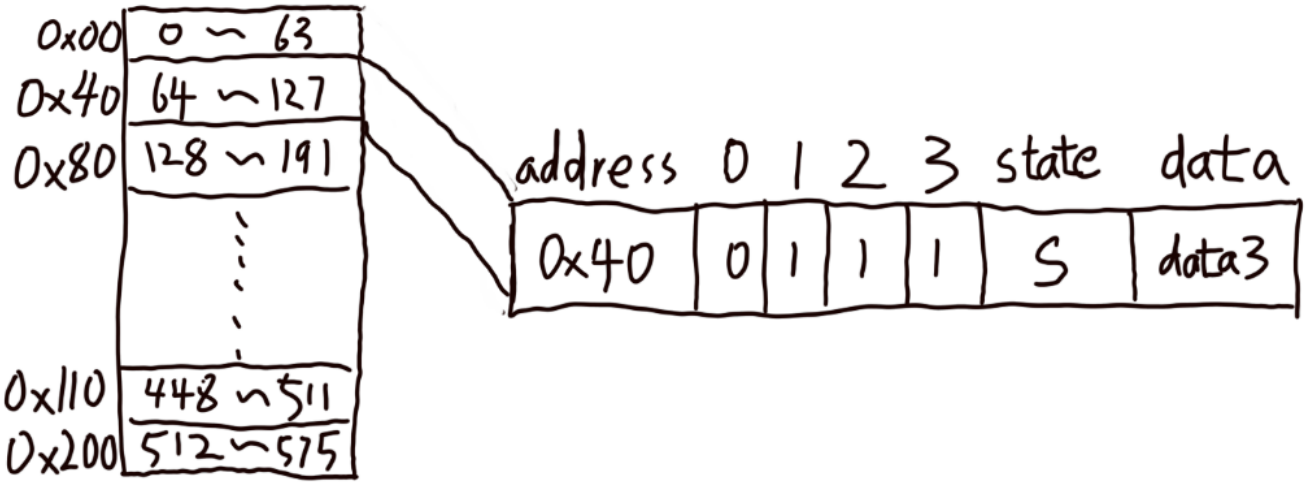


图 2：memory 中数据格式示例

c) 程序整体实现思路：

程序执行指令的方式为依次轮询各核心，直到执行完每一个 trace 文件中的指令：

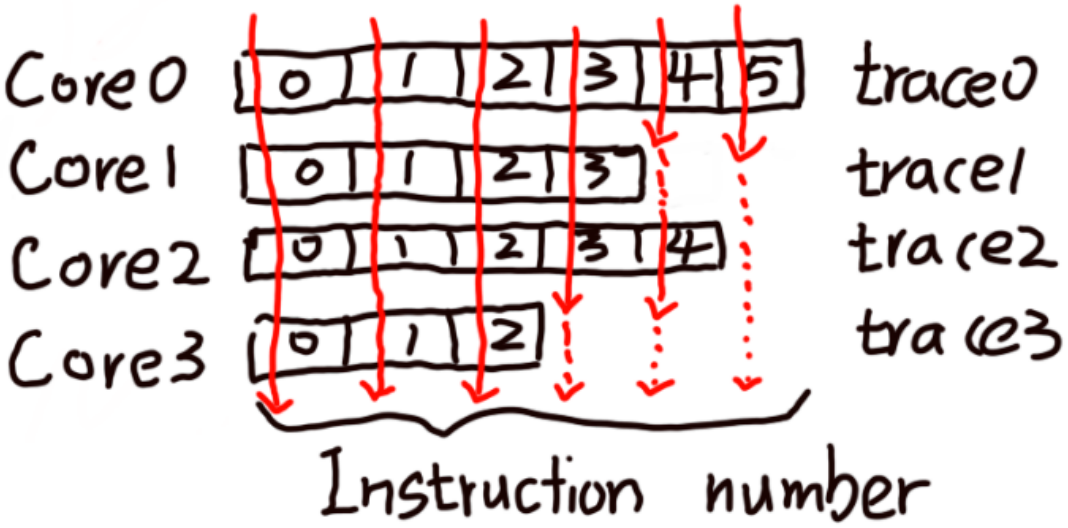


图 3：轮询示例（红色为程序执行顺序，从左右到从上到下）

当地址为 DO_Nothing = 4096-1（0xfff）时，会认为此条指令为无操作指令，直接跳过，不会调用指令处理函数。当地址不为 0xfff 时候则直接调用 dealwith 函数处理指令，并将指令和所属核心作为参数传递。

Dealwith()函数将对指令进行分类，分为三类，如下所示：

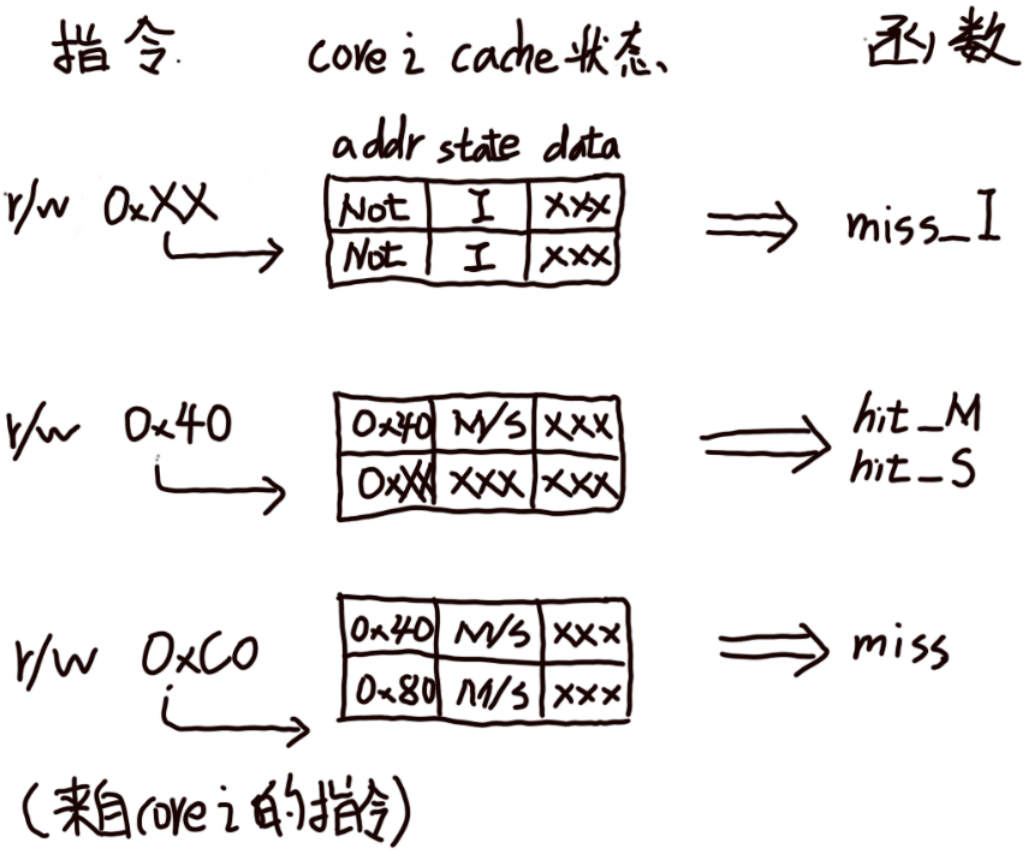


图 4：对指令的分类

当读写指令由核心 i 发出，且指令地址与核心 i 中的某行 cacheline 地址相同时，发生 cache 命中，此时被命中的 cacheline 状态只能为 M 或者 S（I 状态 address 为 0xfff，不会被命中），相应的指令处理函数 dealwith()会调用 hit_M()和 hit_S()函数具体处理 cache 状态和数据的变化。

当读写指令由核心 i 发出，且指令地址与核心 i 中的所有 cacheline 地址都不相同：

若存在 cacheline 未使用（地址为 0xfff），则调用 miss_I()函数处理此条指令，并将相应的状态为 I 的 cacheline 行号作为参数转递。

若全部 cacheline 均已被使用（被其他数据占用），则调用 miss()函数处理此条指令，miss()函数实现了随即替换策略，被替换 cacheline 被写回 memory，之后此行 cacheline 变为状态 I，然后转 miss()函数处理。

相应的 hit_M(), hit_S(), miss_I() 和 miss()函数主要完成的是对指令的执行，函数会遍历每个核心，当 core_k(指令发出核心)与遍历的核心是同一个是为本地操作，否则为远程操作，其内容包括对每个核心的地址更新，数据更新，cache 状态更新和 memory 标记更新，。

4. 代码流程图：

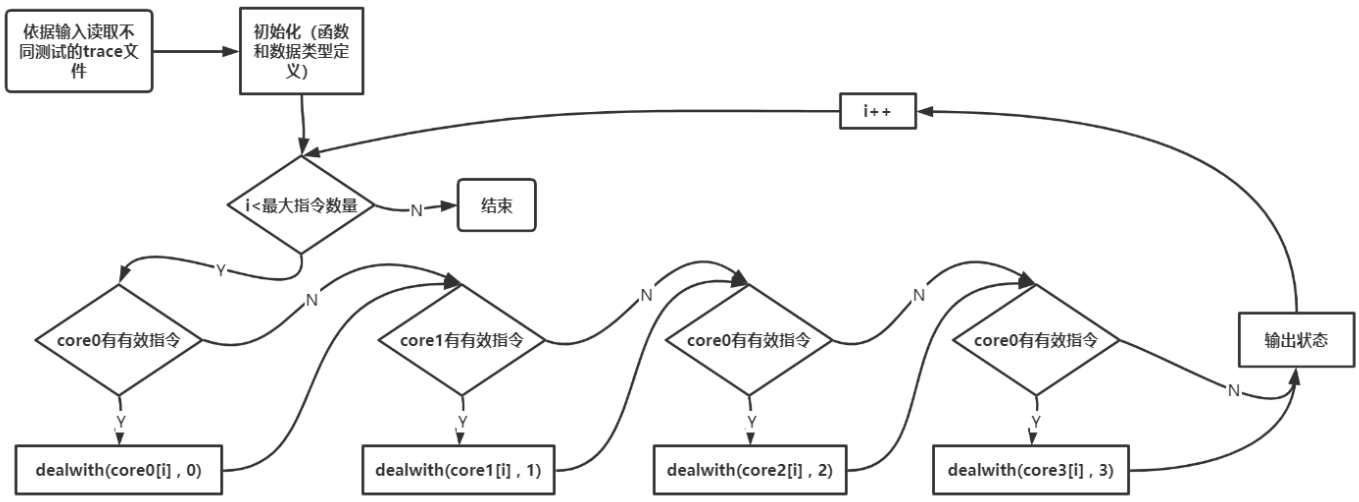


图 5：主程序代码流程图

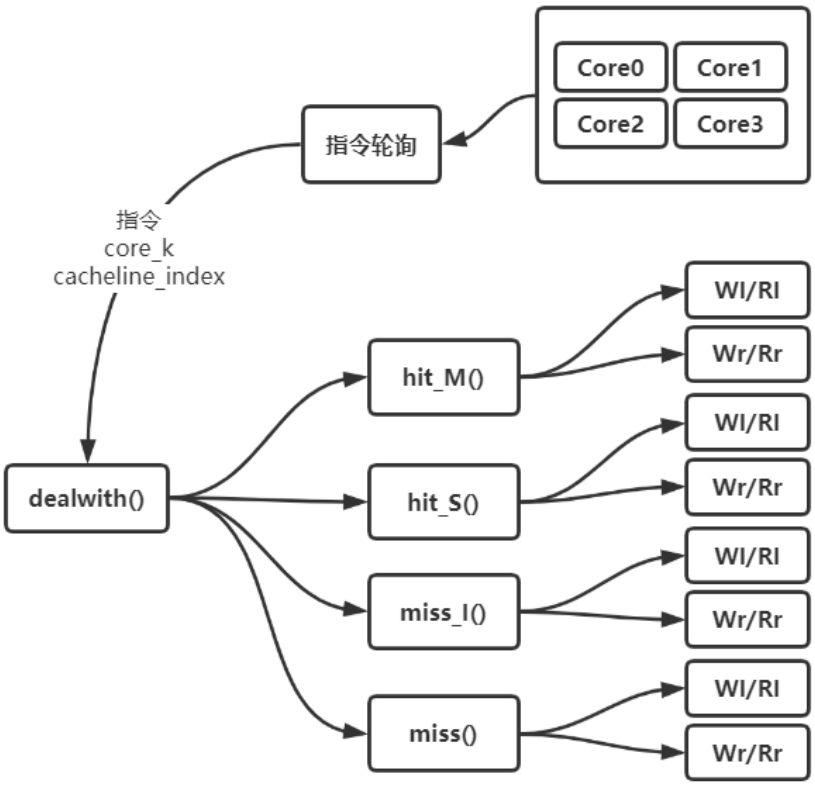


图 6：程序函数关系和调用次序

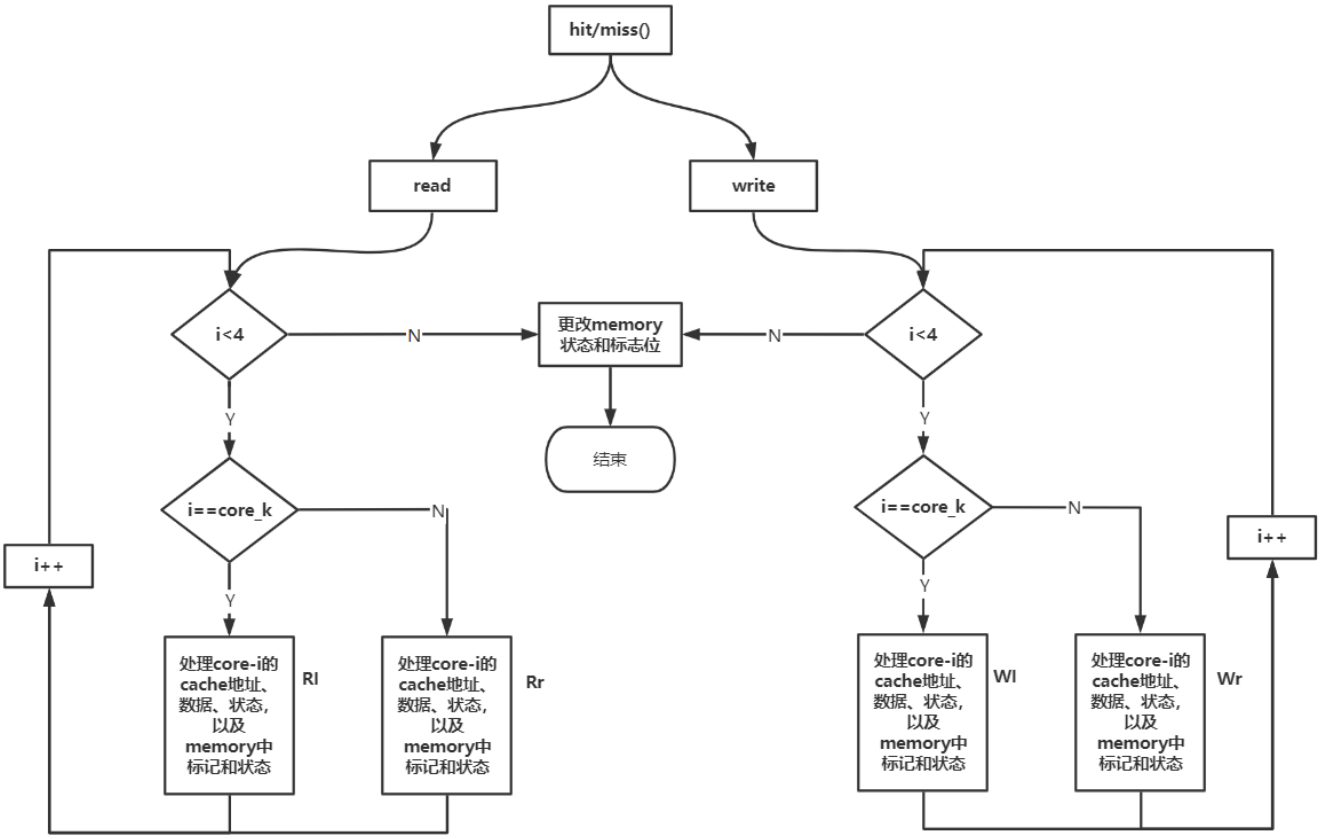


图 7：具体函数流程图

5. 使用方法以及注意事项（输入和输出）:

运行程序后会提示输入信息如下:

```
PS C:\Users\gmx\Desktop\parallel>  c:; cd 'c:\Users\gmx\Desktop\parallel'; & 'E:\Anaconda\python.exe' 'c:\Us
926500501\pythonFiles\lib\python\debugpy\launcher' '50703' '--' 'c:\Users\gmx\Desktop\parallel\cache.py'
Please input test name (base/test1/test2):
        base:basic test required in homework.
        test1:test for cache miss when cacheline is full(cacheline's state is M).
        test2:test for cache miss when cacheline is full(Only cacheline's state is S and memory's is S).
```

其中，输入 base，测试 hit_M() hit_S()的 miss_I()，此时会依次执行如下指令操作，每个核心执行完一条指令为一轮，中间显示操作后状态：

	指令操作	Core0	Core1	Core2	Core3
第一轮	每个核读 0x40	S	S	S	S
第二轮	0 核写 40 到 0x40	M	I	I	I
第三轮	1 核读 0x40	S	S	I	I
第四轮	2 核写 20 带 0x40	I	I	M	I
第五轮	1、3 核读 0x40	I	S	S	S

输入 test1，测试 miss()函数，且两个 cacheline 状态均为 M，执行如下操作：

	指令操作
第一轮	0 核读 0x40
第二轮	0 核读 0x80
第三轮	0 核读 0xC0

输入 test2，测试 miss()函数，且两个 cacheline 状态和相应的 memory 状态为 S，执行如下所示操作：

	指令操作
第一轮	0 核写 0 到 0x40
第二轮	0 核写 1 到 0x80
第三轮	0 核写 2 到 0xC0

以上的三个测试已经测试了逻辑相对复杂，操作相对密集的情况，均符合预期设计。

每轮询一次（执行四条指令）则会使用 print_state()函数输出一次 cache 和 memory 状态，当然也可以修改为每执行一条指令输出一次状态（去掉程序末尾部分注释）。

输出数据由四个核心的 cache 和 memory 组成，使用 prettytable 库优化了输出效果，阅读性很好。

!!! 请务必安装 prettytable 库，并导入，本实验中使用此库优化输出效果。

6. 测试数据和结果：

以下为 base 测试结果，分别显示了【S S S S】、【M I I I】、【S S I I】、【I I M I】和【I S S S】

```
base
+------------------------+
|     cache of core0     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   S   |  64  |
```

```
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core1     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   S   |  64  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core2     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   S   |  64  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core3     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   S   |  64  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------------------------------------------------------------+
|                                 Memory state                                  |
+---------+------------+------------+------------+------------+-------+------+
| address | core0_flag | core1_flag | core2_flag | core3_flag | state | data |
+---------+------------+------------+------------+------------+-------+------+
|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |
|   0x40  |     1      |     1      |     1      |     1      |   S   |  64  |
|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |
|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |
|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |
|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |
|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |
|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |
|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |
+---------+------------+------------+------------+------------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>>


+------------------------+
|     cache of core0     |
```

```
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   M   |  10  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core1     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   |  64  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core2     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   |  64  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core3     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   |  64  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------------------------------------------------------------+
|                                 Memory state                                  |
+---------+------------+------------+------------+------------+-------+------+
| address | core0_flag | core1_flag | core2_flag | core3_flag | state | data |
+---------+------------+------------+------------+------------+-------+------+
|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |
|   0x40  |     1      |     0      |     0      |     0      |   I   |  64  |
|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |
|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |
|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |
|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |
|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |
|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |
|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |
+---------+------------+------------+------------+------------+-------+------+
```

```
>>>>>>>>>>>>>>>>>>>>>>>>>>

+-------------------------+
|     cache of core0      |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   S   |  10  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------+
|     cache of core1      |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   S   |  10  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------+
|     cache of core2      |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   |  64  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------+
|     cache of core3      |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   |  64  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------------------------------------------------------------+
|                                 Memory state                                  |
+---------+------------+------------+------------+------------+-------+------+
| address | core0_flag | core1_flag | core2_flag | core3_flag | state | data |
+---------+------------+------------+------------+------------+-------+------+
|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |
|   0x40  |     1      |     1      |     0      |     0      |   I   |  64  |
|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |
|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |
|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |
|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |
```

```
|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |
|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |
|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |
+---------+------------+------------+------------+------------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+
|     cache of core0     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   |  10  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core1     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   |  10  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core2     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   M   |  20  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core3     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   |  64  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------------------------------------------------------------+
|                                 Memory state                                  |
+---------+------------+------------+------------+------------+-------+------+
| address | core0_flag | core1_flag | core2_flag | core3_flag | state | data |
+---------+------------+------------+------------+------------+-------+------+
|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |
|   0x40  |     0      |     0      |     1      |     0      |   I   |  64  |
```

```
|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |
|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |
|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |
|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |
|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |
|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |
|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |
+---------+------------+------------+------------+------------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+
|     cache of core0     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   |  10  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core1     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   S   |  20  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core2     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   S   |  20  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core3     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   S   |  20  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------------------------------------------------------------+
|                                 Memory state                                  |
+---------+------------+------------+------------+------------+-------+------+
```

```
| address | core0_flag | core1_flag | core2_flag | core3_flag | state | data |
+---------+------------+------------+------------+------------+-------+------+
|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |
|   0x40  |     0      |     1      |     1      |     1      |   I   |  64  |
|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |
|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |
|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |
|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |
|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |
|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |
|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |
+---------+------------+------------+------------+------------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
```

以下为 test1 测试结果。高亮了变化部分

```
test1
+-----------------------+
|     cache of core0    |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   S   |  64  |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-----------------------+
|     cache of core1    |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-----------------------+
|     cache of core2    |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-----------------------+
|     cache of core3    |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
```

```
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------------------------------------------------------------+
|                                Memory state                                   |
+---------+------------+------------+------------+------------+-------+------+
| address | core0_flag | core1_flag | core2_flag | core3_flag | state | data |
+---------+------------+------------+------------+------------+-------+------+
|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |
|   0x40  |     1      |     0      |     0      |     0      |   S   |  64  |
|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |
|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |
|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |
|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |
|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |
|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |
|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |
+---------+------------+------------+------------+------------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+
|     cache of core0     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   S   |  64  |
|   0x80  |   S   | 128  |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core1     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core2     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core3     |
+---------+-------+------+
```

address	state	data
0xfff	I	None
0xfff	I	None

>>>>>>>>>>>>>>>>>>>>>>>>>

Memory state						
address	core0_flag	core1_flag	core2_flag	core3_flag	state	data
0x0	0	0	0	0	M	0
0x40	1	0	0	0	S	64
0x80	1	0	0	0	S	128
0xc0	0	0	0	0	M	192
0x100	0	0	0	0	M	256
0x140	0	0	0	0	M	320
0x180	0	0	0	0	M	384
0x1c0	0	0	0	0	M	448
0x200	0	0	0	0	M	512

>>>>>>>>>>>>>>>>>>>>>>>>>

cache of core0

address	state	data
0xc0	S	192
0x80	S	128

>>>>>>>>>>>>>>>>>>>>>>>>>

cache of core1

address	state	data
0xfff	I	None
0xfff	I	None

>>>>>>>>>>>>>>>>>>>>>>>>>

cache of core2

address	state	data
0xfff	I	None
0xfff	I	None

```
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-----------------------+
|     cache of core3    |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------------------------------------------------------+
|                                Memory state                             |
+---------+-----------+-----------+-----------+-----------+-------+------+
| address | core0_flag | core1_flag | core2_flag | core3_flag | state | data |
+---------+-----------+-----------+-----------+-----------+-------+------+
|   0x0   |     0     |     0     |     0     |     0     |   M   |  0   |
|   0x40  |     0     |     0     |     0     |     0     |   M   |  64  |
|   0x80  |     1     |     0     |     0     |     0     |   S   | 128  |
|   0xc0  |     1     |     0     |     0     |     0     |   S   | 192  |
|  0x100  |     0     |     0     |     0     |     0     |   M   | 256  |
|  0x140  |     0     |     0     |     0     |     0     |   M   | 320  |
|  0x180  |     0     |     0     |     0     |     0     |   M   | 384  |
|  0x1c0  |     0     |     0     |     0     |     0     |   M   | 448  |
|  0x200  |     0     |     0     |     0     |     0     |   M   | 512  |
+---------+-----------+-----------+-----------+-----------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
```

以下为 test2 测试结果： **高亮了变化部分**

```
test2
+-----------------------+
|     cache of core0    |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   M   |  0   |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-----------------------+
|     cache of core1    |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-----------------------+
|     cache of core2    |
```

```
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core3     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------------------------------------------------------+
|                                Memory state                             |
+---------+------------+------------+------------+------------+-------+------+
| address | core0_flag | core1_flag | core2_flag | core3_flag | state | data |
+---------+------------+------------+------------+------------+-------+------+
|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |
|   0x40  |     1      |     0      |     0      |     0      |   I   |  64  |
|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |
|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |
|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |
|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |
|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |
|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |
|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |
+---------+------------+------------+------------+------------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+
|     cache of core0     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0x40  |   M   |  0   |
|   0x80  |   M   |  1   |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core1     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
```

```
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core2     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core3     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------------------------------------------------------------+
|                                Memory state                                   |
+---------+------------+------------+------------+------------+-------+------+
| address | core0_flag | core1_flag | core2_flag | core3_flag | state | data |
+---------+------------+------------+------------+------------+-------+------+
|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |
|   0x40  |     1      |     0      |     0      |     0      |   I   |  64  |
|   0x80  |     1      |     0      |     0      |     0      |   I   | 128  |
|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |
|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |
|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |
|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |
|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |
|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |
+---------+------------+------------+------------+------------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>


+------------------------+
|     cache of core0     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|   0xc0  |   M   |  2   |
|   0x80  |   M   |  1   |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core1     |
+---------+-------+------+
```

```
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core2     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+------------------------+
|     cache of core3     |
+---------+-------+------+
| address | state | data |
+---------+-------+------+
|  0xfff  |   I   | None |
|  0xfff  |   I   | None |
+---------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
+-------------------------------------------------------------------------------+
|                                Memory state                                   |
+---------+------------+------------+------------+------------+-------+------+
| address | core0_flag | core1_flag | core2_flag | core3_flag | state | data |
+---------+------------+------------+------------+------------+-------+------+
|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |
|   0x40  |     0      |     0      |     0      |     0      |   M   |  0   |
|   0x80  |     1      |     0      |     0      |     0      |   I   | 128  |
|   0xc0  |     1      |     0      |     0      |     0      |   I   | 192  |
|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |
|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |
|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |
|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |
|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |
+---------+------------+------------+------------+------------+-------+------+
>>>>>>>>>>>>>>>>>>>>>>>>>>
```

7. 实验总结

本次实验充分理解了 cache 一致性问题，对实现 cache 一致性的关键问题有了一定认识，通过编程，还对 cache 未命中的处理方式有了更加深刻的了解。

本实验仍然有局限性，限于时间只能实现随即替换策略和 cache 全相联映射方式。同时为了方便显示，本实验将对某个字节地址的读写，默认为对某个 64Byte 块的读写，地址上也采取了除 64Byte 取整数的方式获取块地址。

8. Python 代码（见 cache.py）