并行计算机体系结构

——cache一致性实验报告

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## 实验要求

实现一种基于WB策略的一致性维护的Cache模拟器，该模拟器仅考虑4核的CPU，且每个核只有一级Cache，Cache行长度为64字节，观察CPU读、写数据后各个核上Cache中数据状态的变化情况。

（1）输入参数为trace0.txt、trace1.txt、trace2.txt和trace3.txt，分别表示核0、核1、核2和核3的数据访问文件。trace文件为ASCII文本格式，每行代表一个数据的读、写操作，trace文件可以包含很多行，可以根据需要自行设定多种场景进行全面测试，并且至少需要覆盖课堂上讲授的3种状态变化。

trace文件格式举例，文件trace0.txt

---------------------

0 00007c71

0 00007951

1 00007b51

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说明：该trace文件表示核0：读（0）00007c71（地址）的数据，读（0）00007951（地址）的数据，写（1）00007b51（地址）的数据。

（2）输出为4个核读、写操作（只考虑课堂讲授的4种操作）后Cache中数据的状态（只考虑课堂讲授的3种状态）

作业提交：源代码、trace文件、实验报告。报告中至少包含以下内容：

(a) 模拟器设计思想；

(b) 测试数据以及详细的测试报告；进行测试时，各个核至少要包括以下的测试场景：

       0     1      2      3

(i)    S     S      S      S

(ii)   S     S      I      I

(iii)  M     I      I      I

(iv)   I     S      S      S

(v)    I     I      M      I

(c) 作业感悟

单独完成，严禁抄袭，未说明的地方可自行发挥，2周内提交。

## 完成度和功能介绍：

本程序是cache一致性模拟器，实现了基本的cache一致性模拟功能，同时还有自行发挥的部分。

本程序使用**写回策略**，采用**作废法**，并使用**目录表法**保存一致性所需信息，cache映射方式为**全相联映射**，替换策略为**随机替换**。

四个核心读取指令文件后采用轮询策略依次获取访问互联网络的权限，核0 -> 核1 -> 核2 -> 核3 -> 核0 ……，依次执行各个核心的读写指令。

每个核心有两个cacheline（采用参数定义，可更改），每个cacheline有64Byte容量，memory地址从0x00到0x575（512+63），memory容量为9\*64 Byte（memory容量参数定义，可更改）。

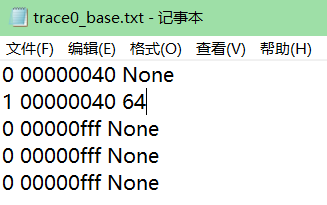
每个核心以及memory的状态都可实现MSI三状态的正确转换。有空闲cacheline时如发生读写，产生cache未命中，随后直接读写并处理一致性，cacheline两行都写满时，再次对不同地址进行读写，则会产生cache未命中，会采用**随机策略替换**一条cacheline，此时发生**写回操作**并释放对应cacheline空间，之后才会读取或者写入新数据到此cacaheline。

## 总体实现思路讲解：

* 1. 输入trace文件格式：

输入指令分为**读、写、无操作**三种类型，需按照如下格式设置：

读写标志位+读写地址+（数据），以空格分开

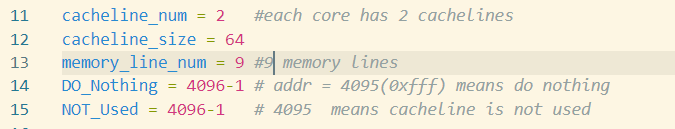


读指令：0+address+None其中None无意义仅为格式统一，方便程序读取。

写指令：1+address+data其中data为要写入address地址处的数据。

无操作指令：0/1+0xfff+“xxx” 当地址为DO\_Nothing = 4096-1（0xfff）时候，认为此指令为无操作，相当于pass，增加此指令的目的是方便测试时候控制每个核心的读写操作，使得部分核心在某一时刻无操作，以体现其他核心操作的结果（指令读取到程序内部后还会设置一个block\_addr，该地址以64Byte为块，方便存入cache）。

* 1. Cache和memory数据组成介绍：



Cache行大小为64Byte，每个核心有两个cacheline（行数可以通过cacheline\_num定义更改），cacheline由address、state、data组成, 如下图所示。当cacheline为M/S状态时，地址和数据有效并为相应数值，cacheline为I状态时为无效，此时地址address需要为NOT\_Used = 4096-1（0xfff），且不关注数据值（**作废法**，作废时候更改state和address，不更改data）。

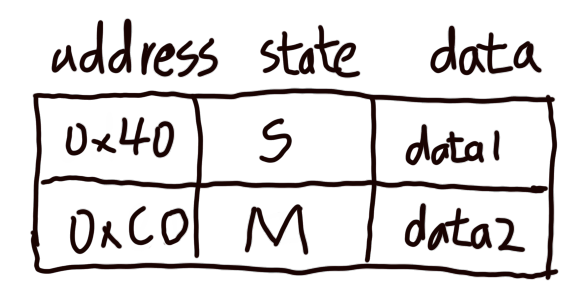


图 1：cache示例，两行cacheline

Memory按照64Byte编为块地址，以方便显示，即位宽为64字节，长度为9块（可通过memory\_line\_num指定，但不能超过0xfff，此地址被认为无操作）。为方便数据显示，本实验将对某个字节地址的读写，默认为对某个64Byte块的读写，地址上也采取了除64取整数的方式获取块地址（本身也是如此，部分字节数据改变，整个64Byte块数据也发生改变）。Memory每块由address、0、1、2、3核cache标志位、memory状态位、块数据组成，如下图所示。

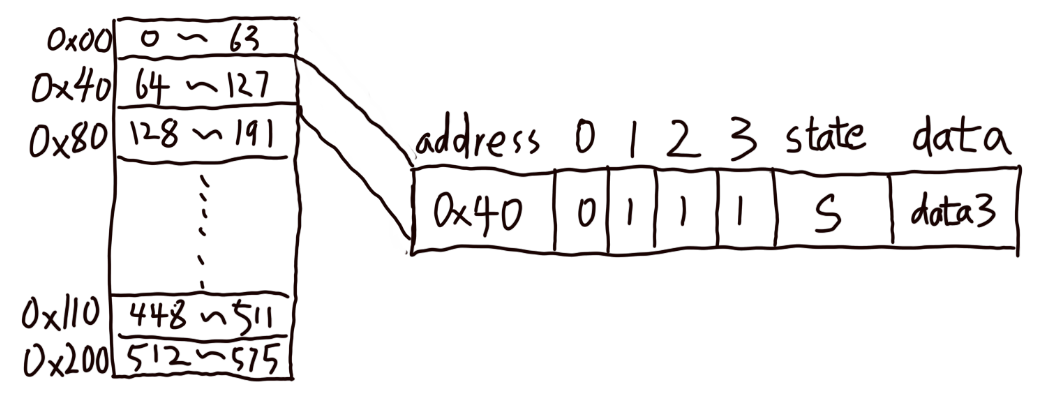


图 2：memory中数据格式示例

* 1. 程序整体实现思路：

程序执行指令的方式为依次轮询各核心，直到执行完每一个trace文件中的指令：

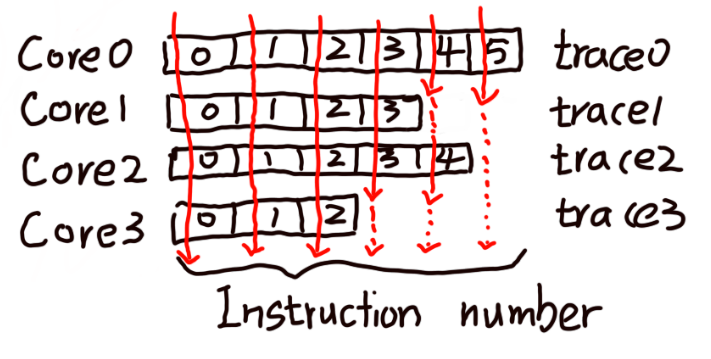


图 3：轮询示例（红色为程序执行顺序，从左右到从上到下）

当地址为DO\_Nothing = 4096-1（0xfff）时，会认为此条指令为无操作指令，直接跳过，不会调用指令处理函数。当地址不为0xfff时候则直接调用dealwith函数处理指令，并将指令和所属核心作为参数传递。

Dealwith()函数将对指令进行分类，分为三类，如下所示：

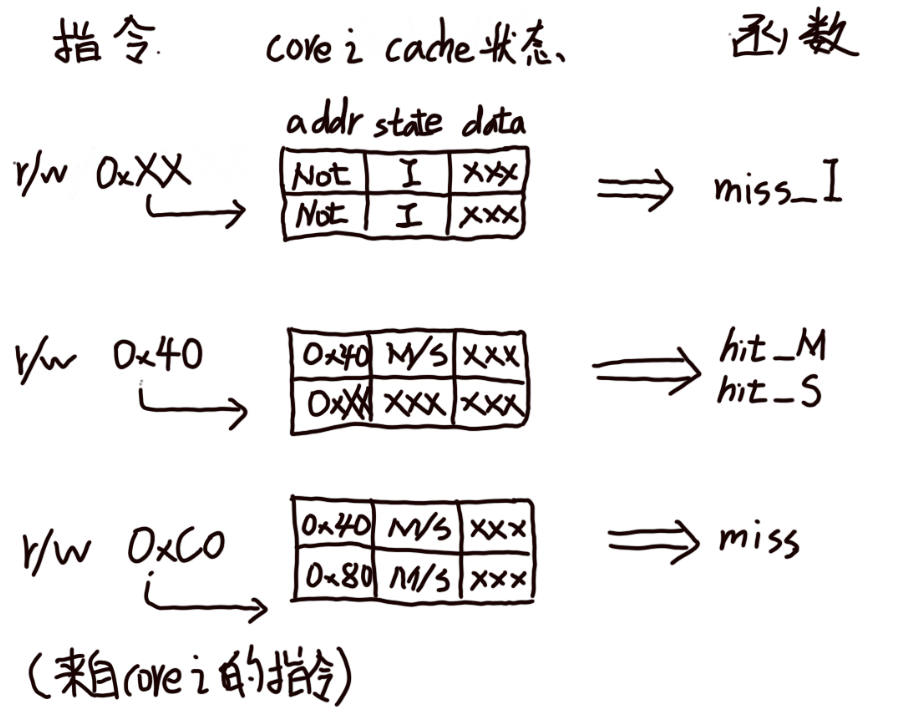


图 4：对指令的分类

当读写指令由核心i发出，且指令地址与核心i中的某行cacheline地址相同时，发生cache命中，此时被命中的cacheline状态只能为M或者S（I状态address为0xfff，不会被命中），相应的指令处理函数dealwith()会调用hit\_M()和hit\_S()函数具体处理cache状态和数据的变化。

当读写指令由核心i发出，且指令地址与核心i中的所有cacheline地址都不相同：

若存在cacheline未使用（地址为0xfff），则调用miss\_I()函数处理此条指令，并将相应的状态为I的cacheline行号作为参数转递。

若全部cacheline均已被使用（被其他数据占用），则调用miss()函数处理此条指令，miss()函数实现了随即替换策略，被替换cacheline被写回memory，之后此行cacheline变为状态I，然后转miss()函数处理。

相应的hit\_M()，hit\_S()，miss\_I() 和miss()函数主要完成的是对指令的执行，函数会遍历每个核心，当core\_k(指令发出核心)与遍历的核心是同一个是为本地操作，否则为远程操作，其内容包括对每个核心的地址更新，数据更新，cache状态更新和memory标记更新。

## 代码流程图：

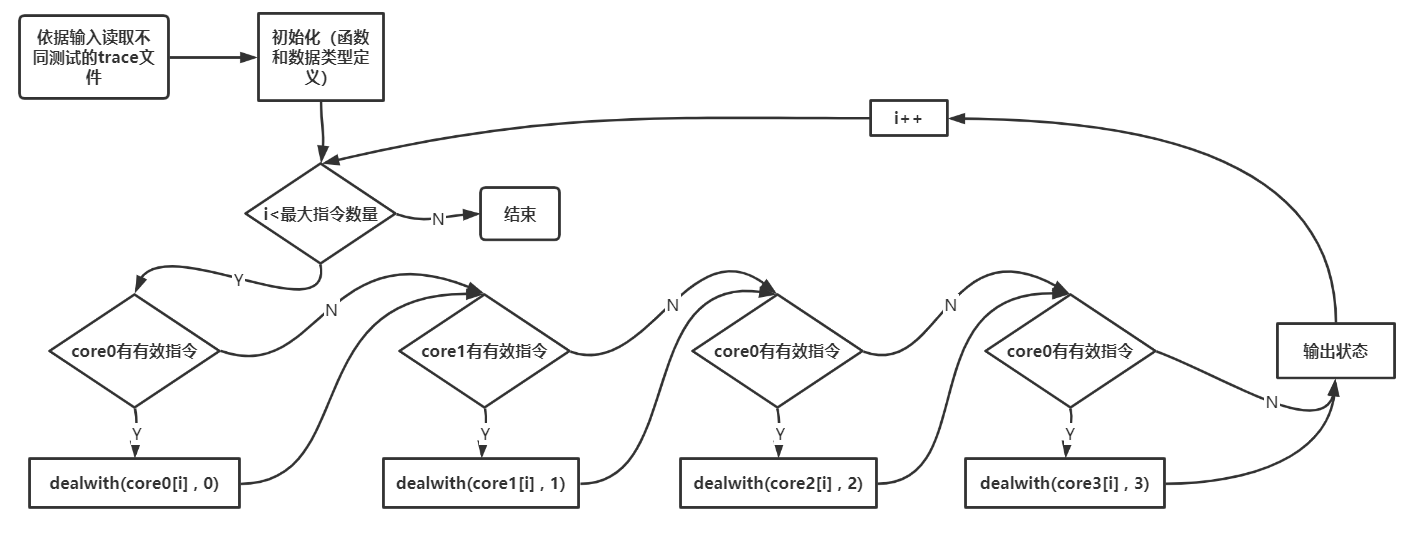


图 5：主程序代码流程图

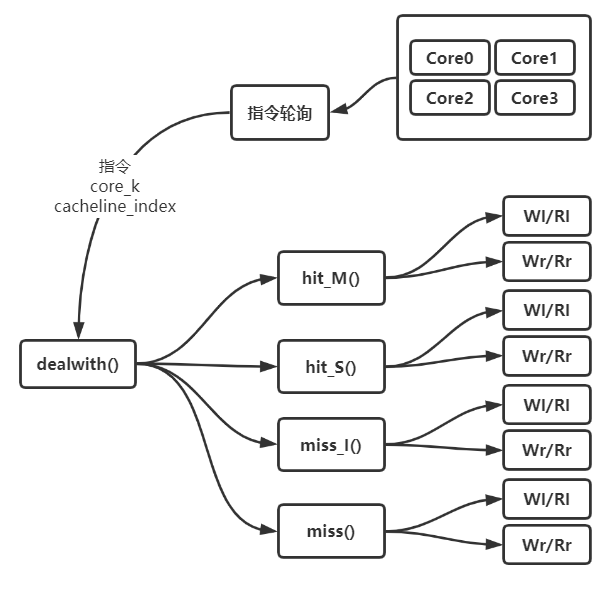


图 6：程序函数关系和调用次序

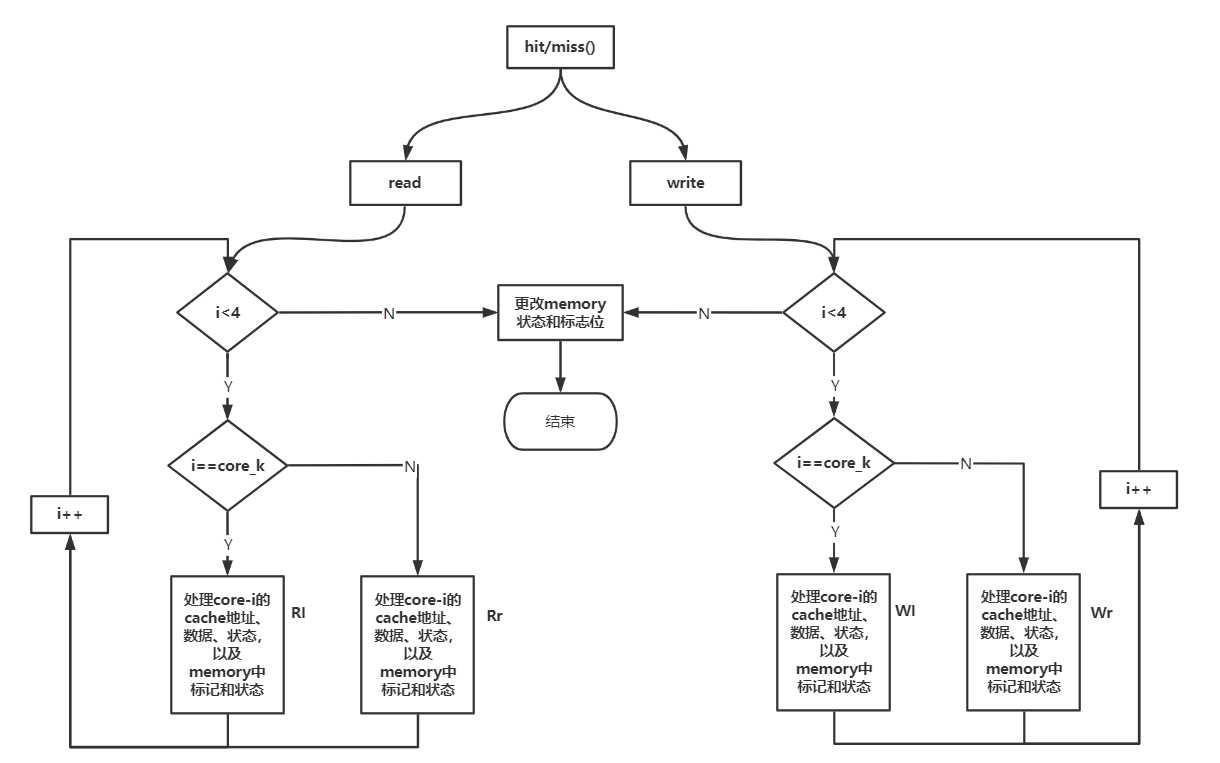
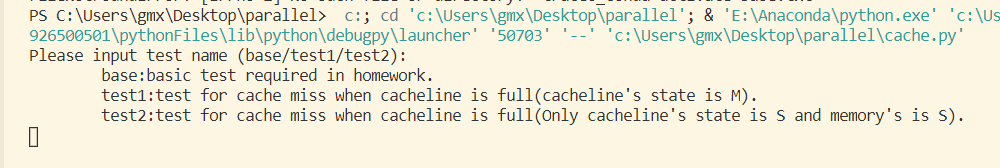


图 7：具体函数流程图

## 使用方法以及注意事项（输入和输出）：

运行程序后会提示输入信息如下：



其中，输入base，测试hit\_M() hit\_S()的miss\_I()，此时会依次执行如下指令操作，每个核心执行完一条指令为一轮，中间显示操作后状态：

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | 指令操作 | Core0 | Core1 | Core2 | Core3 |
| 第一轮 | 每个核读0x40 | S | S | S | S |
| 第二轮 | 0核写40到0x40 | M | I | I | I |
| 第三轮 | 1核读0x40 | S | S | I | I |
| 第四轮 | 2核写20带0x40 | I | I | M | I |
| 第五轮 | 1、3核读0x40 | I | S | S | S |

输入test1，测试miss()函数，且两个cacheline状态均为M，执行如下操作：

|  |  |
| --- | --- |
|  | 指令操作 |
| 第一轮 | 0核读0x40 |
| 第二轮 | 0核读0x80 |
| 第三轮 | 0核读0xC0 |

输入test2，测试miss()函数，且两个cacheline状态和相应的memory状态为S，执行如下所示操作：

|  |  |
| --- | --- |
|  | 指令操作 |
| 第一轮 | 0核写0到0x40 |
| 第二轮 | 0核写1到0x80 |
| 第三轮 | 0核写2到0xC0 |

以上的三个测试已经测试了逻辑相对复杂，操作相对密集的情况，均符合预期设计。

每轮询一次（执行四条指令）则会使用print\_state()函数输出一次cache和memory状态，当然也可以修改为每执行一条指令输出一次状态（去掉程序末尾部分注释）。

输出数据由四个核心的cache和memory组成，使用prettytable库优化了输出效果，阅读性很好。

！！！请务必安装prettytable库，并导入，本实验中使用此库优化输出效果。

## 测试数据和结果：

**以下为base测试结果，分别显示了【S S S S】、【M I I I】、【S S I I】、【I I M I】和【I S S S】**

base

+------------------------+

|     cache of core0     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   S   |  64  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core1     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   S   |  64  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core2     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   S   |  64  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core3     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   S   |  64  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+----------------------------------------------------------------------------+

|                                Memory state                                |

+---------+------------+------------+------------+------------+-------+------+

| address | core0\_flag | core1\_flag | core2\_flag | core3\_flag | state | data |

+---------+------------+------------+------------+------------+-------+------+

|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |

|   0x40  |     1      |     1      |     1      |     1      |   S   |  64  |

|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |

|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |

|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |

|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |

|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |

|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |

|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |

+---------+------------+------------+------------+------------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core0     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   M   |  10  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core1     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   |  64  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core2     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   |  64  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core3     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   |  64  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+----------------------------------------------------------------------------+

|                                Memory state                                |

+---------+------------+------------+------------+------------+-------+------+

| address | core0\_flag | core1\_flag | core2\_flag | core3\_flag | state | data |

+---------+------------+------------+------------+------------+-------+------+

|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |

|   0x40  |     1      |     0      |     0      |     0      |   I   |  64  |

|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |

|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |

|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |

|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |

|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |

|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |

|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |

+---------+------------+------------+------------+------------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core0     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   S   |  10  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core1     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   S   |  10  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core2     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   |  64  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core3     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   |  64  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+----------------------------------------------------------------------------+

|                                Memory state                                |

+---------+------------+------------+------------+------------+-------+------+

| address | core0\_flag | core1\_flag | core2\_flag | core3\_flag | state | data |

+---------+------------+------------+------------+------------+-------+------+

|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |

|   0x40  |     1      |     1      |     0      |     0      |   I   |  64  |

|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |

|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |

|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |

|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |

|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |

|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |

|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |

+---------+------------+------------+------------+------------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core0     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   |  10  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core1     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   |  10  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core2     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   M   |  20  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core3     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   |  64  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+----------------------------------------------------------------------------+

|                                Memory state                                |

+---------+------------+------------+------------+------------+-------+------+

| address | core0\_flag | core1\_flag | core2\_flag | core3\_flag | state | data |

+---------+------------+------------+------------+------------+-------+------+

|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |

|   0x40  |     0      |     0      |     1      |     0      |   I   |  64  |

|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |

|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |

|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |

|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |

|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |

|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |

|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |

+---------+------------+------------+------------+------------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core0     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   |  10  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core1     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   S   |  20  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core2     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   S   |  20  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core3     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   S   |  20  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+----------------------------------------------------------------------------+

|                                Memory state                                |

+---------+------------+------------+------------+------------+-------+------+

| address | core0\_flag | core1\_flag | core2\_flag | core3\_flag | state | data |

+---------+------------+------------+------------+------------+-------+------+

|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |

|   0x40  |     0      |     1      |     1      |     1      |   I   |  64  |

|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |

|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |

|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |

|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |

|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |

|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |

|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |

+---------+------------+------------+------------+------------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

**以下为test1测试结果。高亮了变化部分**

test1

+------------------------+

|     cache of core0     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   S   |  64  |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core1     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core2     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core3     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+----------------------------------------------------------------------------+

|                                Memory state                                |

+---------+------------+------------+------------+------------+-------+------+

| address | core0\_flag | core1\_flag | core2\_flag | core3\_flag | state | data |

+---------+------------+------------+------------+------------+-------+------+

|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |

|   0x40  |     1      |     0      |     0      |     0      |   S   |  64  |

|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |

|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |

|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |

|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |

|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |

|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |

|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |

+---------+------------+------------+------------+------------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core0     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   S   |  64  |

|   0x80  |   S   | 128  |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core1     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core2     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core3     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+----------------------------------------------------------------------------+

|                                Memory state                                |

+---------+------------+------------+------------+------------+-------+------+

| address | core0\_flag | core1\_flag | core2\_flag | core3\_flag | state | data |

+---------+------------+------------+------------+------------+-------+------+

|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |

|   0x40  |     1      |     0      |     0      |     0      |   S   |  64  |

|   0x80  |     1      |     0      |     0      |     0      |   S   | 128  |

|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |

|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |

|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |

|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |

|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |

|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |

+---------+------------+------------+------------+------------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core0     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0xc0  |   S   | 192  |

|   0x80  |   S   | 128  |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core1     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core2     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core3     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+----------------------------------------------------------------------------+

|                                Memory state                                |

+---------+------------+------------+------------+------------+-------+------+

| address | core0\_flag | core1\_flag | core2\_flag | core3\_flag | state | data |

+---------+------------+------------+------------+------------+-------+------+

|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |

|   0x40  |     0      |     0      |     0      |     0      |   M   |  64  |

|   0x80  |     1      |     0      |     0      |     0      |   S   | 128  |

|   0xc0  |     1      |     0      |     0      |     0      |   S   | 192  |

|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |

|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |

|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |

|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |

|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |

+---------+------------+------------+------------+------------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

**以下为test2测试结果： 高亮了变化部分**

test2

+------------------------+

|     cache of core0     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   M   |  0   |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core1     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core2     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core3     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+----------------------------------------------------------------------------+

|                                Memory state                                |

+---------+------------+------------+------------+------------+-------+------+

| address | core0\_flag | core1\_flag | core2\_flag | core3\_flag | state | data |

+---------+------------+------------+------------+------------+-------+------+

|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |

|   0x40  |     1      |     0      |     0      |     0      |   I   |  64  |

|   0x80  |     0      |     0      |     0      |     0      |   M   | 128  |

|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |

|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |

|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |

|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |

|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |

|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |

+---------+------------+------------+------------+------------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core0     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0x40  |   M   |  0   |

|   0x80  |   M   |  1   |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core1     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core2     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core3     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+----------------------------------------------------------------------------+

|                                Memory state                                |

+---------+------------+------------+------------+------------+-------+------+

| address | core0\_flag | core1\_flag | core2\_flag | core3\_flag | state | data |

+---------+------------+------------+------------+------------+-------+------+

|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |

|   0x40  |     1      |     0      |     0      |     0      |   I   |  64  |

|   0x80  |     1      |     0      |     0      |     0      |   I   | 128  |

|   0xc0  |     0      |     0      |     0      |     0      |   M   | 192  |

|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |

|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |

|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |

|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |

|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |

+---------+------------+------------+------------+------------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core0     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|   0xc0  |   M   |  2   |

|   0x80  |   M   |  1   |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core1     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core2     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+------------------------+

|     cache of core3     |

+---------+-------+------+

| address | state | data |

+---------+-------+------+

|  0xfff  |   I   | None |

|  0xfff  |   I   | None |

+---------+-------+------+

>>>>>>>>>>>>>>>>>>>>>>>>>>>>

+----------------------------------------------------------------------------+

|                                Memory state                                |

+---------+------------+------------+------------+------------+-------+------+

| address | core0\_flag | core1\_flag | core2\_flag | core3\_flag | state | data |

+---------+------------+------------+------------+------------+-------+------+

|   0x0   |     0      |     0      |     0      |     0      |   M   |  0   |

|   0x40  |     0      |     0      |     0      |     0      |   M   |  0   |

|   0x80  |     1      |     0      |     0      |     0      |   I   | 128  |

|   0xc0  |     1      |     0      |     0      |     0      |   I   | 192  |

|  0x100  |     0      |     0      |     0      |     0      |   M   | 256  |

|  0x140  |     0      |     0      |     0      |     0      |   M   | 320  |

|  0x180  |     0      |     0      |     0      |     0      |   M   | 384  |

|  0x1c0  |     0      |     0      |     0      |     0      |   M   | 448  |

|  0x200  |     0      |     0      |     0      |     0      |   M   | 512  |

+---------+------------+------------+------------+------------+-------+------+

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## 实验总结

本次实验充分理解了cache一致性问题，对实现cache一致性的关键问题有了一定认识，通过编程，还对cache未命中的处理方式有了更加深刻的了解。

本实验仍然有局限性，限于时间只能实现随即替换策略和cache全相联映射方式。同时为了方便显示，本实验将对某个字节地址的读写，默认为对某个64Byte块的读写，地址上也采取了除64Byte取整数的方式获取块地址。

## Python代码（见cache.py）