High-Level Model of c1908

Statistics: 33 inputs; 25 outputs; 880 gates

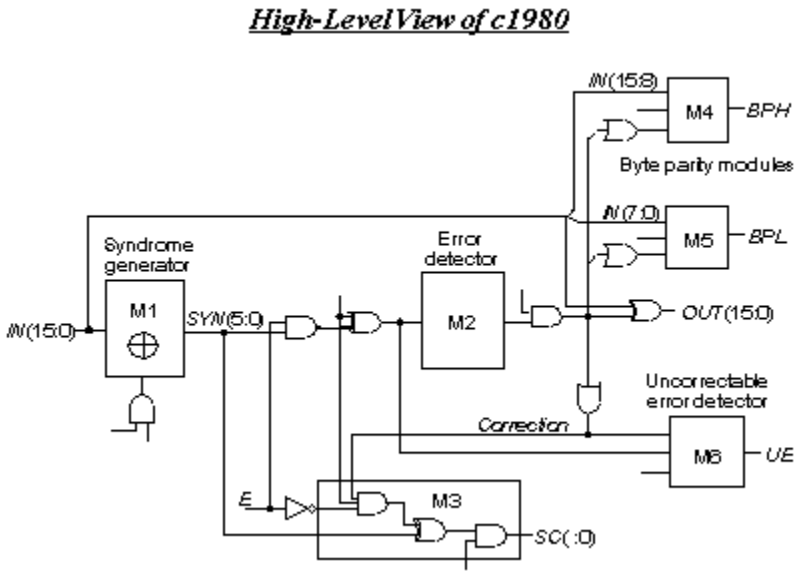
Function: 16-bit error detector/corrector

This is a 16-bit single-error-correcting and double-error-detecting (SEC/DED) circuit with some byte-error detection capability. It generates a 6-bit syndrome from the 16-bit data input IN, which is decoded to find the bit in error, if any. If an error is detected and the control inputs are set appropriately, error correction is performed. c1908 has an output indicating an uncorrectable error; this is set when more than one erroneous bit is detected. The circuit can also generate syndrome bits, which are sent out via the SC lines. The external syndrome lines make it possible to cascade several copies of c1908 so that detection and correction can be done for words of size greater than 16. This circuit is quite similar to the Advanced Micro Devices Am2960 16-bit error detection and correction unit.

Inputs/Outputs vs. Netlist Numbers

Models:

- I. Original ISCAS gate-level netlist
  - in ISCAS-89 format
  - in Verilog
- II. Verilog hierarchical netlist (functionally equivalent to I)
- III. Verilog flat netlist (flat version of II; functionally equivalent to I, but with minor structural differences)



Major Input/Output/Internal Signals:

- IN[15:0] (InDataBus): 16-bit data input

OUT[15:0] (OutDataBus): 16-bit data output

InCheckBits[5:0]: input check bits

SYN[5:0] (SynBits): 6-bit syndrome

SYN'[5:0] (NewSynBits): modified syndrome (used internally)

SC[5:0] (OutSynCheckBits): output syndrome or check bits

InExtSynBits[3:0]: external syndrome inputs (used in cascaded mode to handle word size >16)

BPH (ByteParHi), BPL (ByteParLo): Low- and high-byte parities

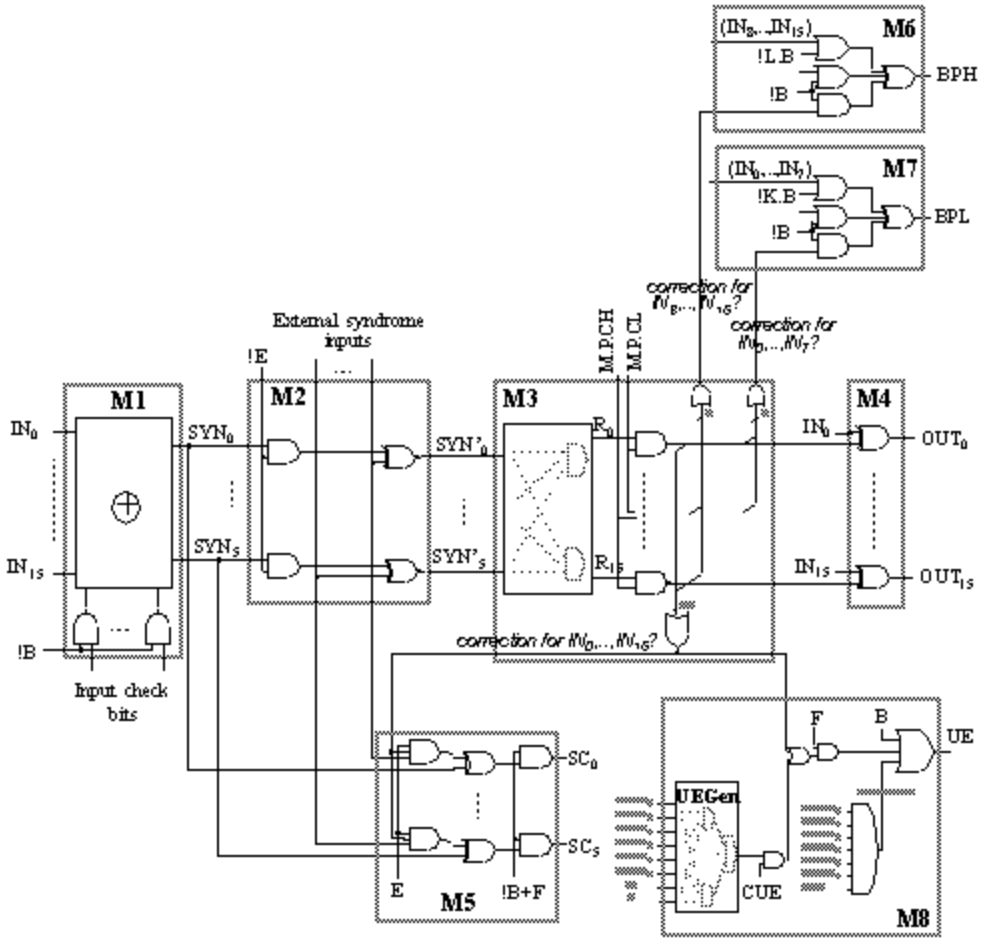
UE : uncorrectable error

E, B, F, G, H, K, L: control inputs

Internal control signals:

M = (H + E). InCheckBits[1]
P = (!G + E). InCheckBits[4]
CH = !(GH). (!K.BE + F. !B)
CL = !(GH). (!L.BE + F. !B)
CUE = !(GH). F. !B

Detailed Circuit Diagram of c1980



Modules:

- M1: generates a 6-bit syndrome (SYN[5:0])
- M2: may modify the syndrome with external inputs; outputs SYN'[5:0]
- M3: decodes the syndrome to identify the bit in error, if any
- M4: corrects the input bit in error
- M5: produces the output syndrome SC[5:0]
- M6-M7: calculate a parity bit for the high (M6) and low byte (M7)
- M8: asserts its output UE if an uncorrectable error is found in the input data bus

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Module M1 (SyndromeGenerator)

This module generates a 6-bit syndrome (SYN) from the 16-bit input data bus (IN) and 6 input check bits (InCheckBits). The input check bits are modified with the control inputs G and H as follows:

- Check bit #0 = InCheckBits[0].G
- Check bit #1 = InCheckBits[1].!H
- Check bit #2 = InCheckBits[2].!H
- Check bit #3 = InCheckBits[3]
- Check bit #4 = InCheckBits[4].G
- Check bit #5 = InCheckBits[5]

The syndrome bits are calculated according to a modified Hamming matrix shown below.

Output	Data bits (IN)																Check bits					
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**#0**	**#1**	**#2**	**#3**	**#4**	**#5**
SYN[0]	.	.	1	.	.	1	.	1	.	1	.	1	.	.	1	.	1	.	.	.	.	.
SYN[1]	.	1	.	.	1	.	.	1	1	.	1	.	.	1	1	1	.	1	.	.	.	.
SYN[2]	1	.	.	.	1	1	1	.	.	1	1	1	1	.	1	1	.	.	1	.	.	.
SYN[3]	1	1	1	1	.	.	.	.	.	1	1	1	1	1	1	1	.	.	.	1	.	.
SYN[4]	.	.	.	1	.	.	1	.	1	1	.	.	1	1	.	1	.	.	.	.	1	.
SYN[5]	1	1	1	1	1	1	1	1	1	1	.	.	.	.	1	1	.	.	.	.	.	1

Module M2 (ModifySyndrome)

This module is used to change the 6-bit syndrome (SYN) generated by M1. Its output is called SYN'[5:0] (NewSynBits) that also depends on the control input E, and another bus named *AllExtSynBits*. The definition of AllExtSynBits[5:0] is as follows:

- AllExtSynBits[3:0] = InExtSynBits[3:0] (primary inputs)
- AllExtSynBits[4] = InCheckBits[0].(!G + E)

- AllExtSynBits[5] = InCheckBits[2].(H + E)

The AllExtSynBits bus appears to be an external set of syndrome inputs that can override the syndrome (SYN) when E is set to 1. Otherwise the SYN' output is the XNOR of SYN and AllExtSynBits. The ability of c1908 to change the calculated syndrome is probably exercised when it is cascaded to handle words of size greater than 16. When E is set to 0 and AllExtSynBits are all 1's, the syndrome goes through M2 unchanged.

Module M3 (SyndromeDecode)

This module consists of 16 AND gates that decode the syndrome bits to identify the erroneous bit, if there is one. It matches the syndrome bits against the columns of the above Hamming matrix. The product term calculated by each AND gate is shown in the following table.

Output	SYN'[0]	SYN'[1]	SYN'[2]	SYN'[3]	SYN'[4]	SYN'[5]
R0	1	0	1	1	0	1
R1	0	1	0	1	0	1
R2	1	0	0	1	0	1
R3	0	0	0	1	1	1
R4	0	1	1	0	0	1
R5	1	0	1	0	0	1
R6	0	0	1	0	1	1
R7	1	1	0	0	0	1
R8	0	1	0	0	1	1
R9	1	0	1	1	1	1
R10	0	1	1	1	0	0
R11	1	0	1	1	0	0
R12	0	0	1	1	1	0
R13	0	1	0	1	1	0
R14	1	1	1	1	0	1
R15	0	1	1	1	1	1

If bit *i* is in error, then Ri will be set to 1, while all the others are 0. Notice that the rows of the above table are identical to the columns of the modified Hamming matrix.

Module M3 generates three additional signals called *CorrectionFlag*, *CorrectionFlagLo* and *CorrectionFlagHi* that are fed into modules M5, M6, M7 and M8. *CorrectionFlag* is the OR of R0-R15, which is set to 1 when any bit is in error. *CorrectionFlagLo* is the OR of R0-R7, which is set to 1 only when the lower byte includes the erroneous bit. Similarly, *CorrectionFlagHi* is the OR of R8-R15, which is set to 1 only when the upper byte includes the erroneous bit.

Module M8 (UncorrErrorGenerator)

When an error is found in the data input or check bits, this module identifies whether it is an uncorrectable one. For certain cases of multiple errors, correction is not possible, but its occurrence can be signaled so that the problem can be handled by other means. If such a case is found, the output of M8 is asserted. The

following term calculated by M8 evaluates to true when there is no error in any bit:

SYN'[0].SYN'[1].SYN'[2].SYN'[3].SYN'[4].SYN'[5].M.P

It is a sub-module named **UEGen** that detects if there is an uncorrectable error condition. There are 8 cases of uncorrectable error, each of which is calculated by an AND gate. The product terms for these 8 cases are given below.

-M-	-P-	SYN'[0]	SYN'[1]	SYN'[2]	SYN'[3]	SYN'[4]	SYN'[5]
1	1	1	1	1	1	0	1
1	1	1	1	1	0	1	1
1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1
1	1	0	1	1	1	1	1
1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1
0	1	1	1	1	1	1	1

Inputs	Netlist number
InDataBus[15:0] (IN)	146, 143, 140, 137, 134, 131, 128, 125, 122, 119, 116, 113, 110, 107, 104, 101
InCheckBits[5:0]	224, 221, 227, 210, 214, 217
InExtSynBits[3:0]	469, 472, 475, 478
E,B,F (control inputs)	902, 953, 952
G,H,K,L (control inputs)	234, 237, 898, 900

Outputs	Netlist number
OutDataBus[15:0] (OUT)	48, 45, 42, 39, 36, 33, 30, 27, 24, 21, 18, 15, 12, 9, 6, 3
OutSynCheckBits[5:0] (SC)	51, 66, 54, 57, 60, 63
ByteParHi (BPH)	72
ByteParLo (BPL)	69
UncorrError (UE)	75

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