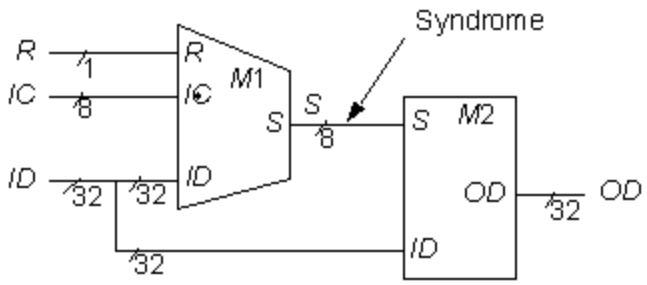
ISCAS-85 C499/C1355 32-Bit Single-Error-Correcting Circuit



Statistics: 41 inputs; 32 outputs; 202/546 gates; bus translations

Function: c499 was found to be a single-error-correcting circuit as shown above. The 41 inputs are combined to form an 8-bit internal bus S, which then combines with 32 primary inputs to form the 32 primary outputs. The boolean expressions defining S form the H matrix for a (40,32) Hamming code [See C. L. Chen and M. Y. Hsiao. Error-Correcting Codes for Semiconductor Memory Applications: A State-of-the-Art Review. IBM Journal of Research & Development, vol. 28, pp. 124-134, March 1984]. If H_ij (the element in row i and column j) is 1, then ID_j (or IC_j-32 if j > 31) is used in S_i . Module M2 contains the necessary correcting logic, so c499 can correct single-bit errors; however, no error-detection logic is present. The S lines are formulated to generate a unique syndrome for each input line in error. The syndromes are the column vectors of H. If syndrome i is seen, output OD_i is inverted. This is specified by the 32 output equations realized by M2.

The c1355 circuit has the same overall function as c499; it differs in that all XOR primitives of c499 are expanded to their four-NAND-gate equivalents.

Models:

- c499 ISCAS-85 netlist
- c499 Verilog hierarchical structural model
- c499/1355 Verilog hierarchical behavioral model
- c499 complete gate-level tests
- c1355 ISCAS-85 netlist
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